M1523: PCI-to-ISA Bus Bridge

Section 1: Introduction

1.1 Features

- Technology
  - 0.5 µm, triple-metal CMOS process
- Provides a bridge between the PCI bus and ISA bus
- PCI interface
  - Supports PCI Master and Slave Interface
  - Supports PCI Master and Slave initiated termination
  - PCI spec. 2.1 Compliant (Delay transaction support)
- Buffers
  - 8-byte bidirectional Line Buffers are provided for DMA/ISA Memory Read/Write cycles to PCI Bus.
  - 32-bit Posted Write Buffer is provided for PCI Memory Write and I/O data write (for sound card) to ISA bus.
- Provides steerable PCI interrupts for PCI device plug-and-play
  - Up to 8 PCI interrupts routing
  - Level to edge trigger transfer
- Enhanced DMA Controller
  - Provides 7 programmable channels, 4 for 8-bit data size, 3 for 16-bit data size
  - 32-bit addressability
  - Provides Compatible DMA transfers
  - Provides Type F transfers
- Interrupt Controller
  - Provides 14 interrupt channels
  - Independently programmable Level/Edge triggered channels
- Counter/Timers
  - Provides 8254 compatible timers for System timer, Refresh Request, Speaker Output use
- Keyboard controller
  - Built-in PS2/AT Keyboard controller
  - The specific I/O is used to save the external TTL buffer
- Distributed DMA support
  - Built-in Real timock
  - 128-byte CMOS RAM with 2µA standby current maximum
- Plug-and-Play Port supports
  - 1 programmable chip select
  - 2 Steerable Interrupt Request lines
- PMU interface
  - Supports CPU SMM mode, SMI feature
  - Supports programmable stop clock throttle
  - Supports the APM control
  - Provides External Suspend mode Switch/Turbo switch/Ring in switch
  - Provides 4 system states for power saving (On, Doze, Standby, Suspend)
  - Provides 3 timers from 1 second to 300 minutes to individually monitor VGA, MODE, IN status
  - Supports RTC alarm wake up control
- IDE interface
  - Built-in PCI IDE master controller
  - Supports PIO modes up to mode 5 timings, and multiword DMA mode 0, 1, 2
  - 8 x 32-bit pre-read & posted write buffers
  - Dedicated pins for ATA interface
- Supports up to 256 KB ROM size decode
- Reserved USB interface
- 208-pin PQFP package

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1.2 Functions

The M1523 is a bridge between PCI and ISA bus, providing full PCI and ISA compatible functions. The M1523 has Integrated System Peripherals (ISP) on chip and provides advanced features in the DMA controller. The keyboard controller, Real Time Clock and IDE Master Controller are also included in this chip. Furthermore, this chip supports the Advanced Programmable Interrupt controller (APIC) interface.

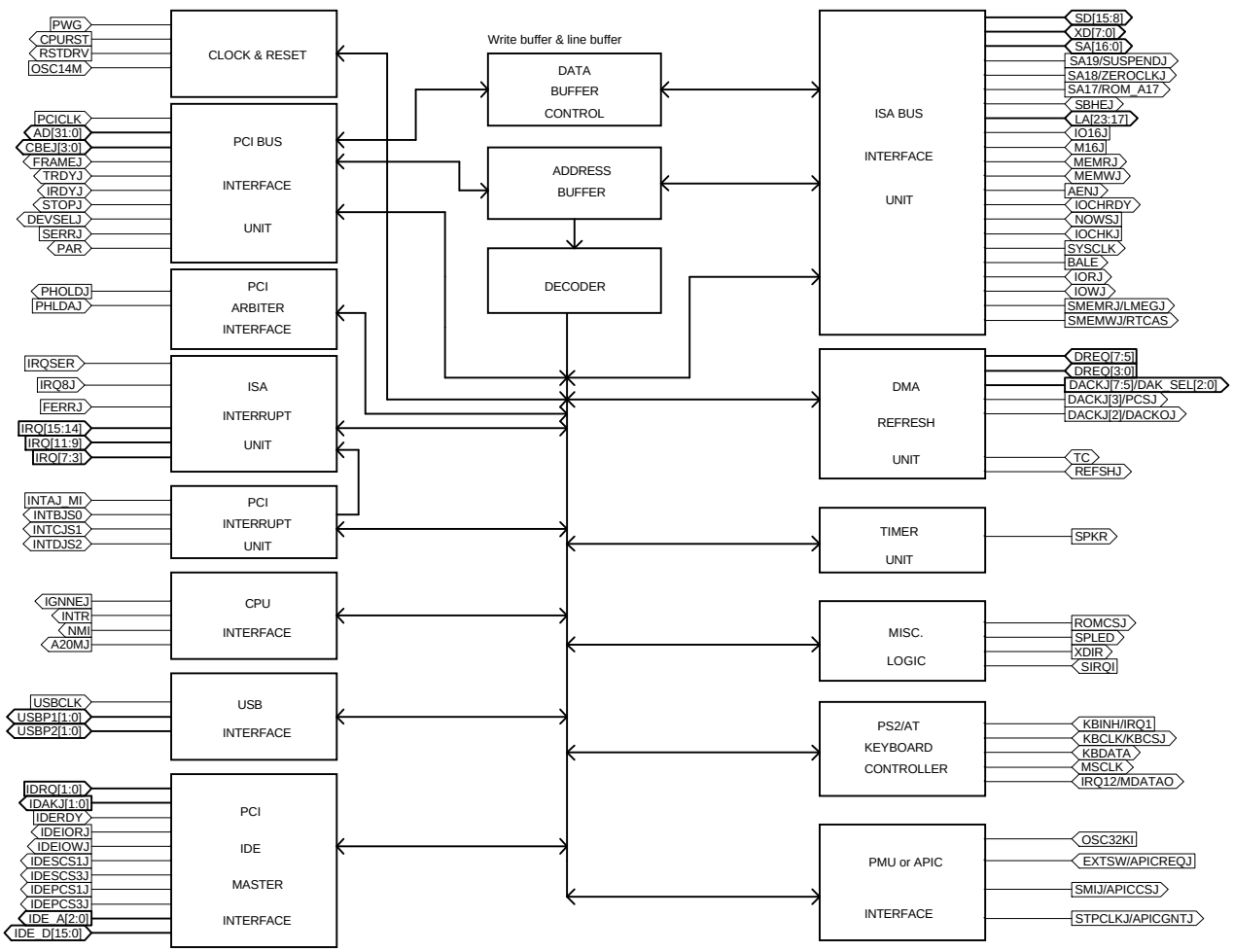
One eight byte bi-directional line buffer is provided for ISA/DMA Master memory read/writes. One 32-bit wide posted write buffer is provided for PCI memory write cycles to the ISA bus. Provides a PCI to ISA IRQ routing table, and level to edge trigger transfer.

The chip provides 2 extra IRQ lines and 1 programmable chip select for motherboard Plug-and-Play functions. The interrupt lines can be routed to any of the available ISA interrupts.

The on-chip IDE controller supports two IDE connectors for up to 4 IDE devices providing an interface for IDE hard disks and CD ROMs. The ATA bus pins are dedicated to improve the performance of IDE Master.

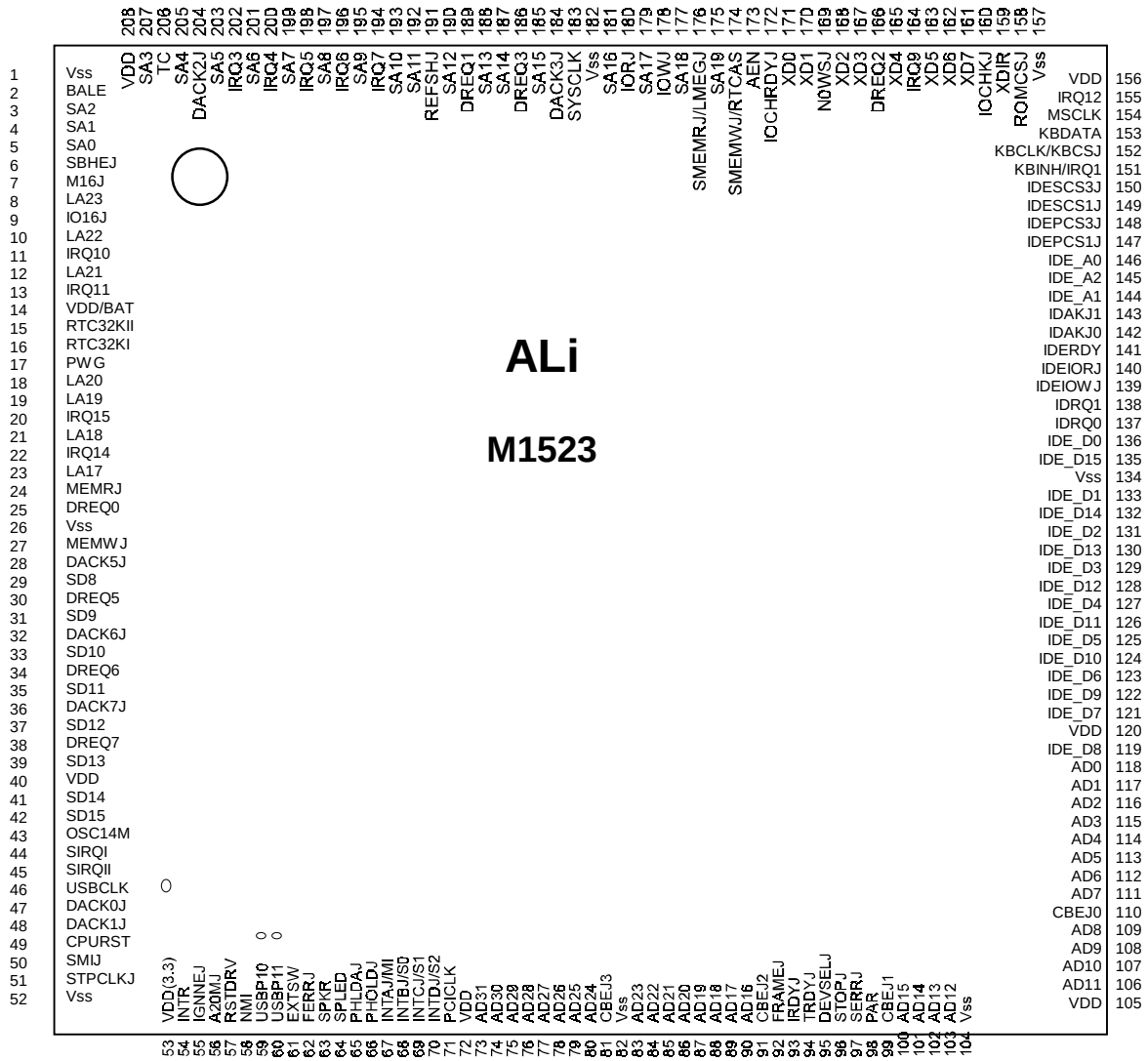
The M1523 supports Super Green for Intel and Intel compatible CPUs. It implements programmable hardware events, software event and external switches (for suspend/turbo/ring-in). The M1523 provides CPU clock control (STPCLKJ). The STPCLKJ can be active (low) or inactive (high) in turn by throttling control.

Functional Block Diagram



Section 2: Pin Description

2.1 Pin Diagram



2.2 Pin Description Table

Pin Name	Pin No.	Type	Description
Clock & Reset			
PWG	17	I	**Power-Good Input.** This signal comes from the power supply to indicate that power is available and stable.
CPURST	49	O	**CPU RESET** includes Cold & Warm reset 3.3V signal (connected to CPU INIT)
RSTDRV	57	O	**CPU cold reset.** 3.3V signal (connected to CPU RESET)
OSC14M	43	I	**14.318Mhz clock input**. This is used for 8254 timer clock.
PCI Interface			
PCICLK	71	I	**PCI clock** for internal PCI interface.
AD[31:0]	73-80, 83-90, 100-104, 106-109, 111-118	I/O	**Address and Data** are multiplexed on PCI bus. During the first clock of a PCI transaction, AD[31-0] contains a physical address. During subsequent clocks, AD[31-0] contains data.
C/BEJ[3:0]	81,91, 99,110	I/O	**Bus Command and Byte enable.** During address phase, CBEJ[3:0] define the Bus Command. During data phase, CBEJ[3:0] define the Byte Enables.
FRAMEJ	92	I/O	**Cycle Frame** is driven by current initiator to indicate the beginning and duration of an access.
DEVSELJ	95	I/O	**Device Select**. This indicates that the target device has decoded the address as its own cycle. This pin is an output pin when the M1523 acts as a PCI slave that has decoded address as its own cycle including subtractive decoding.
IRDYJ	93	I/O	**Initiator Ready** indicates the initiator's ability to complete the current data phase of the transaction.
TRDYJ	94	I/O	**Target Ready** indicates the target's ability to complete the current data phase of the transaction.
STOPJ	96	I/O	**Stop** indicates to the M1523 is requesting a master to stop the current transaction.
PAR	98	I/O	**Parity signal.** PAR is even parity and is calculated on AD[31:0] and CBEJ[3:0]. When the M1523 acts as a PCI master, it drives PAR one PCI clock after address phase for a read/write transaction and one PCI clock after data phase for a write transaction. When the M1523 acts as target, it drives PAR one PCI clock after data phase for a PCI master read transaction.
SERRJ	97	I	**System Error** may be pulsed active by any agent that detects a system error condition. When SERRJ is sampled low, the M1523 will assert NMI to interrupt the CPU.
PCI Interrupt Unit			
INTAJ_MI	67	I	**PCI interrupt input A** or PCI interrupt polling input.
INTBJ	68	I/O	**PCI interrupt input B** or polling select_0 output.
INTCJ	69	I/O	**PCI interrupt input C** or polling select_1 output.
INTDJ	70	I/O	**PCI interrupt input D** or polling select_2 output.
PCI Arbiter			
PHOLDJ	66	O	M1523 requests the ownership of the PCI bus. Hardware setting option Pull low : internal RTC is enabled Pull high : external RTC is used.
PHLDAJ	65	I	**PCI Hold Acknowledge**. When this pin is asserted, the M1523 owns the PCI bus.

Pin Description Table (continued)

Pin Name	Pin No.	Type	Description
CPU Interface (3.3V)			
IGNNEJ	55	O	**Ignore Numeric Error.** This pin is used as the ignore numeric coprocessor error.
INTR	54	O	**Interrupt request to CPU.** This is the interrupt signal generated by the internal 8259.
NMI	58	O	**Non-maskable interrupt.** This is non-maskable interrupt request to CPU.
A20MJ	56	O	**CPU A20 Mask.** This is the Address line 20 mask signal.
ISA Interface			
FERRJ/IRQ13	62	I	**Floating point error.** FERRJ input to generate IRQ13. When the coprocessor interface is disabled in configuration port 43h bit 6, the function of this pin is IRQ13.
IRQ12/MDATAO	155	B	**Mouse Interrupt request input/Mouse data output** when internal PS/2 keyboard is disabled, this pin is mouse interrupt input. Otherwise, this pin is mouse data output.
IRQ[15:14], IRQ[11:9], IRQ[7:3]	20,22,13, 11,164, 194,196, 200,202	I	**Interrupt Request signals.**
SD[15:8]	42,41,39, 37,35,33, 31,29	I/O	**ISA high byte Slot Data bus.** These lines are system data lines.
XD[7:0]	161-163, 165,167, 168, 170-171	I/O	**External Data bus** lines are connected to SD[7:0] by an external TTL LS245, whose direction is controlled by the M1523 output signal XDIR.
SA19	175	O	**ISA Slot Address Bus A19.**
SA18	177	O	**ISA Slot Address Bus A18.**
SA17	179	O	**ISA Slot Address Bus A17.**
SA[16:0]	181, 185, 187, 188, 190, 192, 193, 195, 197, 199, 201, 203, 205, 207, 3, 4, 5	I/O	**ISA Slot Address bus.** These lines are addresses connected to slot address.
SBHEJ	6	I/O	**ISA slot Byte high enable.** In a CPU or PCI master cycle, this signal is generated by BE3J-BE0J and the chip's internal control circuit. In a DMA cycle, it is generated by internal 8237. In a refresh cycle, it is generated by the internal refresh circuits. It is an input signal for ISA master cycle.
LA[23:17]	8,10,12, 18,19,21, 23	I/O	**ISA Latched Address bus.** They are input during ISA master cycle.
IO16J	9	I	**ISA 16-bit I/O device indicator.** This signal indicates the I/O device supports 16-bit transfers.
M16J	7	I/O	**ISA 16-bit memory device indicator.** This signal indicates the memory device supports 16-bit transfers.
MEMRJ	24	I/O	**ISA memory read.** This signal is an input during ISA master cycle.
MEMWJ	27	I/O	**ISA memory write.** This signal is an input during ISA master cycle.

Pin Description Table (continued)

Pin Name	Pin No.	Type	Description
AEN	173	O	**ISA I/O address enable.** Active high signal during DMA cycle to prevent I/O device from misinterpreting the DMA cycle as valid I/O cycle.
IOCHRDY	172	I/O	**ISA system ready.** This signal is an output during ISA/DMA master cycle.
NOWSJ	169	I	**ISA zero wait-state for input**. This signal terminates the CPU to ISA command instantly.
IOCHKJ	160	I	**ISA parity error.** M1523 will generate NMI to CPU when this signal is asserted.
SYSCLK	183	O	**ISA system clock.** This signal provides clocking function to ISA bus.
BALE	2	O	**Bus Address Latch Enable.** BALE is active throughout DMA and ISA master and refresh cycles.
IORJ	180	I/O	**ISA I/O read.** This signal is an input during ISA master cycle.
IOWJ	178	I/O	**ISA I/O write.** This signal is an input during ISA master cycle.
SMEMRJ/LMEGJ	176	O	**ISA system memory read.** When the internal RTC is enabled, this signal indicates that the memory read cycle is for an address below 1M byte address. Otherwise, this pin only indicates an address below 1M byte.
SMEMWJ/RTCAS	174	O	**ISA system memory write.** When the internal RTC is enabled, this signal indicates that the memory write cycle is for an address below 1M byte address. Otherwise, this pin is used as RTC address strobe.
DREQJ[7:5] DREQJ[3:0]	38,34,30, 186,166, 189,25	I	**DMA request** signals. These are DMA request input signals.
DACKJ[7:5]/ DAK_SEL[2:0] DACKJ[3]/PCSJ, DACKJ[2]/DACKO JDACKJ[1], DACKJ[0]	36,32, 28, 184, 204, 48, 47	O B O	When DACKJ polling mode is disabled, these pins are DACKJ[7:5,3:0](O). Otherwise, these pins are DAK_SEL[2:0](O) (connected to external MUX's select inputs), PCSJ(O) (programmable chip select), DACKOJ(O) (connected to external MUX's chip enable).
TC	206	O	**DMA end of process**. Hardware setting option: Pull low : Support external I/O APIC mode Pull high : Not support external I/O APIC
REFSHJ	191	I/O	**ISA Refresh cycle.** This signal is input during ISA master cycles, but an output during other cycles.
Timer			
SPKR	43	O	**Speaker output.** Hardware setting option : Pull low : Enable Internal KBC Pull high: Disable Internal KBC
Miscellaneous			
SPLED	44	O	**Speed LED output**. Hardware setting option: Pull low : Enable DMA DACKJ[7:5,3:0] polling mode Pull high: Disable DMA DACKJ[7:5;3:0] polling mode
ROMCSJ	158	O	**ROM & RTC chip select.** This signal must be pulled high for normal operation.
XDIR	159	O	**X-bus direction control**. Hardware setting option: must pull high.
KBINH/ IRQ1	151	I	**KB inhibit input** when the internal KBC is enabled **IRQ1 input** when the internal KBC is disabled
KBCLK/ KBCSJ	152	I/O	**KB interface CLK** when the internal KBC is enabled **KB Chip Select** when the internal KBC is disabled
KBDATA	153	O	**KB interface Data** when the internal KBC is enabled
MSCLK	154	O	**Mouse clock output** when the internal KBC is enabled.

Pin Description Table (continued)

Pin Name	Pin No.	Type	Description
RTC32KI	16	I	**RTC 32.768K Osc1**. This is crystal input and requires an external 32.768khz quartz crystal.
RTC32KII	15	I	**RTC 32.768K Osc2**. This is crystal input and requires an external 32.768khz quartz crystal.
SIRQI	44	I	**Steerable IRQ input 1**
SIRQII /IRQ8J	45	I	**Steerable IRQ input 2** when the internal RTC is enabled. RTC interrupt input when the internal RTC is disabled.
USBCLK	46	I	Universal serial bus clock pin (reserved).
USBP1[1:0]	59,60	B	Universal serial bus data pin (reserved).
Power Management			
EXTSW/ APICREQJ	61	I	**External SMI switch or APIC request input.** EXTSW is a falling edge triggered input to the M1523 showing that an external device is requesting the system to enter SMM mode. An external pullup should be placed on this signal if it is not used or it is not guaranteed to be always driven. When external APIC mode is enabled, this pin is APICREQJ.
SMIJ/ APICCSJ	50	O	**SMM interrupt or APIC chip select**. a synchronous output that is asserted by the M1523 in response to one of many enabled hardware or software events. When external APIC mode is enabled, this pin is APICCSJ.
STPCLKJ/ APICGNTJ	51	O	**Stop CPU clock request or APIC grant output**. STPCLKJ is connected directly to the CPU and is synchronous with PCI clock. When external APIC mode is enabled, this pin is APICGNTJ.
IDE Interface			
IDRQ[1:0]	138-137	I	**IDE DRQ request for IDE master.**
IDAKJ[1:0]	143-142	O	**IDE DACKJ for IDE master.**
IDERDY	141	I	**IDE ready.**
IDEIORJ	140	O	**IDE IORJ command.**
IDEIOWJ	139	O	**IDE IOWJ command.**
IDESCS1J	149	O	**IDE chip select for secondary channel 0**
IDESCS3J	150	O	**IDE chip select for secondary channel 1**
IDEPCS1J	147	O	**IDE chip select for primary channel 0**
IDEPCS3J	148	O	**IDE chip select for primary channel 1**
IDE_A[2:0]	145,144, 146	O	**IDE ATA address bus.**
IDE_D[15:0]	135,132, 130,128, 126,124, 122,119, 121,123, 125,127, 129,131, 133,136	I/O	**IDE ATA data bus.**
VCC & Vss			
VCC3	53	P	**Vcc 3.3V**
VCC5/ V_{BAT}	14	P	**RTC battery input**
VCC5	40, 72, 105, 120, 156, 208	P	**VCC 5.0V**(VDD)
Vss	1, 26, 52, 82, 104, 134, 157, 182	P	**Vss or Ground**.

2.3 Numerical Pin List

Pin No.	Type	Pin Name
1	P	Vss
2	O	BALE
3	B	SA2
4	B	SA1
5	B	SA0
6	B	SBHEJ
7	B	M16J
8	B	LA23
9	I	IO16J
10	B	LA22
11	I	IRQ10
12	B	LA21
13	I	IRQ11
14	P	VDDBAT
15	I	RTC32KII
16	I	RTC32KI
17	I	PWG
18	B	LA20
19	B	LA19
20	I	IRQ15
21	B	LA18
22	I	IRQ14
23	B	LA17
24	B	MEMRJ
25	I	DREQ0
26	P	VSS
27	B	MEMWJ
28	O	DACK5J
29	B	SD8
30	I	DREQ5
31	B	SD9
32	O	DACK6J
33	B	SD10
34	I	DREQ6
35	B	SD11
36	O	DACK7J
37	B	SD12
38	I	DREQ7
39	B	SD13
40	P	VDD
41	B	SD14
42	B	SD15
43	I	OSC14M
44	I	SIRQI
45	I	SIRQII
46		USBCLK
47	O	DACK0J
48	O	DACK1J
49	O	CPURST
50	O	SMIJ

Pin No.	Type	Pin Name
51	O	STPCLKJ
52	P	VSS
53	P	VDD3V
54	O	INTR
55	O	IGNNEJ
56	O	A20MJ
57	O	RSTDRV
58	O	NMI
59		USBP10
60		USBP11
61	I	EXTSW
62	I	FERRJ
63	B	SPKR
64	B	SPLED
65	I	PHLDAJ
66	B	PHOLDJ
67	I	INTAJ/MI
68	B	INTBJ/S0
69	B	INTCJ/S1
70	B	INTDJ/S2
71	I	PCICLK
72	P	VDD
73	B	AD31
74	B	AD30
75	B	AD29
76	B	AD28
77	B	AD27
78	B	AD26
79	B	AD25
80	B	AD24
81	B	CBEJ3
82	P	VSS
83	B	AD23
84	B	AD22
85	B	AD21
86	B	AD20
87	B	AD19
88	B	AD18
89	B	AD17
90	B	AD16
91	B	CBEJ2
92	B	FRAMEJ
93	B	IRDYJ
94	B	TRDYJ
95	B	DEVSELJ
96	B	STOPJ
97	I	SERRJ
98	B	PAR
99	B	CBEJ1
100	B	AD15

Numerical Pin List (continued)

Pin No.	Type	Pin Name
101	B	AD14
102	B	AD13
103	B	AD12
104	P	VSS
105	P	VDD
106	B	AD11
107	B	AD10
108	B	AD9
109	B	AD8
110	B	CBEJ0
111	B	AD7
112	B	AD6
113	B	AD5
114	B	AD4
115	B	AD3
116	B	AD2
117	B	AD1
118	B	AD0
119	B	IDE_D8
120	P	VDD
121	B	IDE_D7
122	B	IDE_D9
123	B	IDE_D6
124	B	IDE_D10
125	B	IDE_D5
126	B	IDE_D11
127	B	IDE_D4
128	B	IDE_D12
129	B	IDE_D3
130	B	IDE_D13
131	B	IDE_D2
132	B	IDE_D14
133	B	IDE_D1
134	P	VSS
135	B	IDE_D15
136	B	IDE_D0
137	I	IDRQ0
138	I	IDRQ1
139	O	IDEIOWJ
140	O	IDEIORJ
141	I	IDERDY
142	O	IDAKJ0
143	O	IDAKJ1
144	O	IDE_A1
145	O	IDE_A2
146	O	IDE_A0
147	O	IDEPCS1J
148	O	IDEPCS3J
149	O	IDESCS1J
150	O	IDESCS3J

Pin No.	Type	Pin Name
151	I	KBINH/IRQ1
152	B	KBCLK/KBCSJ
153	O	KBDATA
154	O	MSCLK
155	B	IRQ12/MDATAO
156	P	VDD
157	P	VSS
158	O	ROMCSJ
159	O	XDIR
160	I	IOCHKJ
161	B	XD7
162	B	XD6
163	B	XD5
164	I	IRQ9
165	B	XD4
166	I	DREQ2
167	B	XD3
168	B	XD2
169	I	NOWSJ
170	B	XD1
171	B	XD0
172	B	IOCHRDYJ
173	O	AEN
174	O	SMEMWJ/RTCAS
175	O	SA19
176	O	SMEMRJ
177	O	SA18
178	B	IOWJ
179	O	SA17
180	B	IORJ
181	B	SA16
182	P	VSS
183	O	SYSCLK
184	O	DACK3J
185	B	SA15
186	I	DREQ3
187	B	SA14
188	B	SA13
189	I	DREQ1
190	B	SA12
191	B	REFSHJ
192	B	SA11
193	B	SA10
194	I	IRQ7
195	B	SA9
196	I	IRQ6
197	B	SA8
198	I	IRQ5
199	B	SA7
200	I	IRQ4

Numerical Pin List (continued)

Pin No.	Type	Pin Name
201	B	SA6
202	I	IRQ3
203	B	SA5
204	O	DACK2J
205	B	SA4
206	O	TC
207	B	SA3
208	P	VDD

2.4 Alphabetical Pin List

Pin No.	Type	Pin Name
56	O	A20MJ
118	B	AD0
117	B	AD1
116	B	AD2
115	B	AD3
114	B	AD4
113	B	AD5
112	B	AD6
111	B	AD7
109	B	AD8
108	B	AD9
107	B	AD10
106	B	AD11
103	B	AD12
102	B	AD13
101	B	AD14
100	B	AD15
90	B	AD16
89	B	AD17
88	B	AD18
87	B	AD19
86	B	AD20
85	B	AD21
84	B	AD22
83	B	AD23
80	B	AD24
79	B	AD25
78	B	AD26
77	B	AD27
76	B	AD28
75	B	AD29
74	B	AD30
73	B	AD31
173	O	AEN
2	O	BALE
110	B	CBEJ0
99	B	CBEJ1
91	B	CBEJ2
81	B	CBEJ3
49	O	CPURST
47	O	DACK0J
48	O	DACK1J
204	O	DACK2J
184	O	DACK3J
28	O	DACK5J
32	O	DACK6J
36	O	DACK7J
95	B	DEVSELJ
25	I	DREQ0
189	I	DREQ1

Alphabetical Pin List (continued)

Pin No.	Type	Pin Name
166	I	DREQ2
186	I	DREQ3
30	I	DREQ5
34	I	DREQ6
38	I	DREQ7
61	I	EXTSW
62	I	FERRJ
92	B	FRAMEJ
93	B	IRDYJ
202	I	IRQ3
142	O	IDAKJ0
143	O	IDAKJ1
146	O	IDE_A0
144	O	IDE_A1
145	O	IDE_A2
136	B	IDE_D0
133	B	IDE_D1
131	B	IDE_D2
129	B	IDE_D3
127	B	IDE_D4
125	B	IDE_D5
123	B	IDE_D6
121	B	IDE_D7
119	B	IDE_D8
122	B	IDE_D9
124	B	IDE_D10
126	B	IDE_D11
128	B	IDE_D12
130	B	IDE_D13
132	B	IDE_D14
135	B	IDE_D15
140	O	IDEIORJ
139	O	IDEIOWJ
141	I	IDERDY
147	O	IDEPCS1J
148	O	IDEPCS3J
149	O	IDESCS1J
150	O	IDESCS3J
137	I	IDRQ0
138	I	IDRQ1
55	O	IGNNEJ
67	I	INTAJ/MI
68	B	INTBJ/S0
69	B	INTCJ/S1
70	B	INTDJ/S2
54	O	INTR
9	I	IO16J
160	I	IOCHKJ
172	B	IOCHRDYJ
178	B	IOWJ

Pin No.	Type	Pin Name
180	B	IORJ
194	I	IRQ7
196	I	IRQ6
198	I	IRQ5
200	I	IRQ4
164	I	IRQ9
155	B	IRQ12/MDATAO
11	I	IRQ10
13	I	IRQ11
22	I	IRQ14
20	I	IRQ15
151	I	KBINH/IRQ1
152	B	KBCLK/KBCSJ
153	O	KBDATA
23	B	LA17
21	B	LA18
19	B	LA19
18	B	LA20
12	B	LA21
10	B	LA22
8	B	LA23
7	B	M16J
154	O	MSCLK
24	B	MEMRJ
27	B	MEMWJ
58	O	NMI
169	I	NOWSJ
43	I	OSC14M
98	B	PAR
71	I	PCICLK
65	I	PHLDAJ
66	B	PHOLDJ
17	I	PWG
191	B	REFSHJ
158	O	ROMCSJ
57	O	RSTDRV
16	I	RTC32KI
15	I	RTC32KII
5	B	SA0
4	B	SA1
3	B	SA2
207	B	SA3
205	B	SA4
203	B	SA5
201	B	SA6
199	B	SA7
197	B	SA8
195	B	SA9
193	B	SA10
192	B	SA11

Alphabetical Pin List (continued)

Pin No.	Type	Pin Name
190	B	SA12
188	B	SA13
187	B	SA14
185	B	SA15
181	B	SA16
179	O	SA17
177	O	SA18
175	O	SA19
6	B	SBHEJ
29	B	SD8
31	B	SD9
33	B	SD10
35	B	SD11
37	B	SD12
39	B	SD13
41	B	SD14
42	B	SD15
97	I	SERRJ
44	I	SIRQI
45	I	SIRQII
176	O	SMEMRJ
174	O	SMEMWJ/RTCAS
50	O	SMIJ
63	B	SPKR
64	B	SPLED
51	O	STPCLKJ
96	B	STOPJ
183	O	SYSCLK
206	O	TC

Pin No.	Type	Pin Name
94	B	TRDYJ
46		USBCLK
59		USBP10
60		USBP11
40	P	VDD
72	P	VDD
120	P	VDD
156	P	VDD
105	P	VDD
208	P	VDD
53	P	VDD3V
14	P	VDDBAT
1	P	VSS
26	P	VSS
82	P	VSS
182	P	VSS
134	P	VSS
104	P	VSS
52	P	VSS
157	P	VSS
171	B	XD0
170	B	XD1
168	B	XD2
167	B	XD3
165	B	XD4
163	B	XD5
162	B	XD6
161	B	XD7
159	O	XDIR

2.5 Hardware Setup Control

XDIR : must Pull-high.

SPLED : Pull-low, DMA DACKJ[7:5,3:0] polling mode is enabled.
Pull-high, DMA DACKJ[7:5,3:0] polling mode is disabled.

SPKR : Pull-low, internal Keyboard controller is enabled.
Pull-high, internal Keyboard controller is disabled.

PHOLDJ : Pull-low, internal Real-Time Clock is enabled.
Pull-high, internal Real-Time Clock is disabled.

EOP : Pull-low, external I/O APIC mode is supported.
Pull-high, external I/O APIC mode is not supported.

ROMCSJ : must be pull-high.

Section 3: Function Description

3.1 PCI Command Set

The command types the M1523 supports in Slave mode are Interrupt Acknowledge, Special cycle, I/O read, I/O write, memory read, memory write, configuration read and configuration write and other multiple memory read/write cycles. When the M1523 acts as a PCI Master, it only performs memory Read/Write transfers. I/O Read/Write are not supported.

M1523 PCI Cycle Description

CBEJ	Command Type	as Target	as Initiator
0000	Interrupt	Yes	No
0001	Special Cycle	Yes - Note.1	No
0010	I/O Read	Yes	No
0011	I/O Write	Yes	No
0100	reserved	No	No
0101	reserved	No	No
0110	Memory Read	Yes	Yes
0111	Memory Write	Yes	Yes
1000	reserved	No	No
1001	reserved	No	No
1010	Configuration Read	Yes	No
1011	Configuration Write	Yes	No
1100	Memory Read Multiple	Yes - Note.2	No
1101	reserved	No	No
1110	Memory Read line	Yes - Note.2	No
1111	Memory Write and Invalidate	Yes - Note.3	No

Note 1 : The M1523 only decodes Stop Grant special cycle, and Shutdown special cycle. All other special cycles are ignored.
Note 2 : Treated as Memory read
Note 3 : Treated as Memory write

3.2 Description of PCI Slave

As a PCI slave, the M1523 will assert DEVSELJ signal to indicate it is the target of the PCI transaction. DEVSELJ is asserted when the M1523 positively or subtractively decodes the PCI transaction. The configuration cycle and interrupt acknowledge cycle and IDE I/O cycle are positively decoded. The timer and interrupt controller programming cycles are positively or subtractively decoded. All others are subtractively decoded.

A 32-bit posted write buffer is embedded to support PCI to ISA memory write cycles and delay transaction cycle. Multiple read/write transactions are not supported. Hence, any burst cycles decoded by the M1523 will be terminated by disconnecting semantics after the first data transaction has completed. The M1523 will retry any PCI initiated cycle when its internal buffer cycle is still active.

M1523 supports delay transaction and discard counter in compliance with PCI specification 2.1.

3.2.1 Posted Write Buffer

The PCI-to-ISA memory write cycles will be posted into the write buffer when it is enabled, and the buffer is scheduled to be written to the ISA bus. Any subsequent PCI cycles to the M1523 will be retried until the posted write buffer is empty. The buffer also optionally supports data I/O posted write cycle for sound cards.

The posted write buffer must be flushed and disabled before an ISA /DMA master owns the ISA and PCI bus. This rule eliminates the possibility of a deadlock caused by a committed ISA cycle. The buffer will also be flushed before granting an external APIC request.

3.3 PCI Master

3.3.1 M1523 as PCI Master

As a PCI Master, the M1523 only performs memory read/write transfers. I/O read/write are not supported. The M1523 will assert a master abort due to DEVSELJ timeout. The M1523 acts as a PCI Master when an ISA or DMA master accesses the PCI memory. The M1523 provides an 8-byte bi-directional line buffer for ISA/DMA Master memory read from or write to PCI bus. The line buffer is used to isolate the ISA bus slower devices from the PCI. Only an ISA/DMA master memory write or read cycle to PCI bus can be assembled /disassembled into line buffer. When line buffer is enabled, the ISA/DMA master can prefetch 2 Doublewords to the line buffer for read cycle. However, only 4 bytes are used in the buffer for write cycle.

In some cases, a strong ordering must be kept due to coherency problems, the line buffer might be disabled. When the line buffer is disabled, the reorder problem caused by assembly /disassembly will be avoided and guarantees read/write ordering.

3.3.2 Posted - Write Buffer Flush

Once an ISA/ DMA master begins a cycle on the ISA bus, the cycle cannot be backed off. It can only be held in wait states via IOCHRDY. In order to avoid deadlock situation, the PCI master post write buffer needs to be flushed before an ISA/ DMA master gets the ISA bus. When the ISA/ DMA master owns the ISA bus, the post write buffer will be disabled.

3.3.3 Line Buffer Management

When an ISA /DMA master reads from PCI memory, the M1523 prefetches 8 bytes of data into the line buffer. If there is a read "hit" from the line buffer, the "hit" bytes are marked as invalid. There are 3 conditions why the line buffer needs prefetching :

1. Line buffer is "Empty" when read.
2. Read "miss" to the line buffer.
3. Read the invalid byte from the line buffer.

When ISA/DMA master writes to PCI memory, the M1523 writes data to the line buffer. When the 4-byte buffer is full, it flushes data to the PCI bus. There are five conditions why the line buffer must flush its data :

1. Line buffer is full. Flush the line buffer and mark empty.

2. Write "miss" to the partially full 4-byte line. Flush the partially full line and mark as empty, then write to the empty line.

3. Write "hit" to the valid bytes. Flush it and mark as empty, then write to the empty line.

4. Read after write transaction and the line buffer is partially full. Flush the line buffer then do read prefetch.

5. Master has changed on DACKJ going inactive and last transaction is write and line buffer is partially full. Flush the line buffer.

3.4 Parity Support

As a master, the M1523 will generate address parity for read/write cycles, and data parity for write cycles. Parity check will work at read cycle. As a target, the M1523 will generate data parity for read cycles. PAR is even parity across AD[31:0] and CBEJ[3:0]. Even parity means that the number of 1's within the 36 bits and PAR is even. PAR has the same timing as AD[31:0] but delayed by one clock.

3.5 Address decoding

a. Positively decodes configuration cycle.
b. Positively or subtractively decodes interrupt acknowledge cycle
c. Positively decodes on-chip IDE access cycle
d. Positively or subtractively decodes internal I/O cycle (interrupt controller and timer counter)
e. Subtractively decodes DMA controller internal registers.
f. Others are subtractive decode

3.6 IDE Master Controller

a. Supports PCI bus mastering, transfer rate up to 132 Mbytes/sec. This significantly lightens the load of CPU's work burden.
b. Supports IDE PIO mode 0, 1, 2, 3, 4 & 5 timing and multiword DMA mode 0,1,2 on enhanced IDE specifications.
   This chip is capable of accelerated PIO data transfers as well as acting as a PCI bus master on behalf of an IDE DMA slave device. The M1523 provides an interface for two IDE connectors.
c. Supports compatible and native PCI mode
   Compatible mode is the default mode, native PCI mode will only be chosen by the BIOS.
d. 8 doubleword FIFO for posted-write or read-ahead buffer.
e. Programmable command and data transfer timing per drive for maximum flexibility. Operation of two harddisks is possible even if they have different PIO modes.
f. Supports concurrent operation on two ATA channels.
   M1523 simultaneously operates two drives.
g. Supports ATAPI CD-ROM concurrent operation.
   Simultaneous use of harddisks and CD-ROM is possible.
h. Dedicated ATA bus pins, no extra TTLs are needed.

3.7 Power Management

The M1523 Power management unit includes SMM, Stop clock control unit, APM, External SMI-switch control, Programmable counters for timeout event generation. The PMU strictly controls and dramatically reduces overall system power consumption. This is accomplished via the activity monitors which detect the system inactivity timer timeout, and signals the power-saving device to slow-down the clock frequency or remove the power sources from various peripherals. It provides 3 individual timers from a second to 300 minutes to monitor following activities:

1)the system states (ON/DOZE/STANDBY/SUSPEND)
2)VGA and a programmable memory region
3)the standard input devices(such as mouse, keyboard, com1, com2)

The M1523 can choose to monitor those combinations of each system state. It provides a LED flash control to indicate the system state status. The M1523 supports external SMI switch to enter suspend mode, or to wakeup system.

3.7.1 SMM event

M1523 supports Intel compatible SMM mode. It monitors the following events:

(1) Time-Out Events :
- Input-Device Time-Out
- VGA Device Access and General Memory Region Access Time-Out
- PMU - Mode Time-Out

(2) External Device Events :
- IRQ's Active
- DRQ's Active
- Input Devices Active
- External Suspend-Switch (or Turbo-switch or Ring in)
- RTC Alarm

(3) Software SMI Event

3.7.2 Stop Clock Control Logic

The STPCLKJ signal is asserted by software and will be de-asserted by optional IRQ, DRQ, NMI and SMI events. The M1523 provides a programmable counter for clock throttle feature. There are two configuration registers HI_TIME (69h) and LO_TIME (68h) to control the STPCLKJ high (inactive) period and low (active) period when no event occurs. That is, the STPCLKJ signal will be asserted by software first. After LO_TIME timer expires, it will be de-asserted. And after HI_TIME timer expires, it will be asserted again. The asserted and de-asserted controls will be toggled periodically until INTR, DRQ, NMI, or SMI event occurs.

3.7.3 APM

The APM (Advanced Power management interface) creates an interface to allow the OS to communicate with the SMM code. The M1523 provides the configuration port 56H Bit3 to generate the software STPCLKJ, and bit6 to generate the software SMIJ signal for the APM applications.

Section 4: Configuration Registers

4.1 Register Description (IDSEL= AD18)

4.1.1 Function 0: PCI to ISA Bridge Configuration Space

The indices before 40h are read-only.
All reserved bits are read as 0's

Index-Offset **Description**

Index 01h-00h(RO) Vendor ID
Value = 10B9h

Index 03h-02h(RO) Device ID
Value = 1523h

Index 05h-04h(RO) Command Byte(000Fh)

D0	I/O Space Enable (always '1');
D1	Memory Space Enable (always '1');
D2	Bus Master Enable (always '1');
D3	Special cycle Enable (always '1');
D4	Cacheing Command Enable (always '0');
D5-D15	reserved. Read as 0's ;

Index 07h-06h Status Byte (0200h)

D8-D0	reserved. Read as 0's;
D10-D9	M1523 DEVSELJ Timing This status of DEVSELJ decode timing as PCI spec. M1523 always generates DEVSELJ with medium timing Bit9='1', Bit10='0';
D11	Signal Target Abort when the M1523 acts as a slave. M1523 as a slave never generates a Target abort this bit is always 0;
D12	Receive Target Abort when M1523 acts as a master. This bit is set to a '1' when M1523 encounters a target abort condition. This is a read only bit and is cleared by writing a '1' to it.
D13	Receive Master Abort when M1523 acts as a master. This bit is set to a '1' when M1523 generates a transaction (except for Special Cycle) is terminated with master-abort. This is a read only bit and is cleared by writing a '1' to it.
D14	Signal System error. Always '0' ;
D15	Detected Parity Error. Always '0';

Index 08h(RO) Revision ID.(00h)

Index 0B-09h(RO) Class code. 0Bh=06h,
0Ah=01h, 09h=00h.

Index 0D-0Ch reserved

Index 0Eh(RO) Device Type.(80h) multi-function chip.

Index 3Fh-0Fh reserved

Index 40h PCI Control (00h)

D0	DMA Line Buffer 0 : disable 1 : enable
D1	ISA Master Line Buffer 0 : disable 1 : enable
D2	PCI-to-ISA Posted Write Buffer 0 : disable 1 : enable
D3	Delay transaction for PCI spec. 2.1 0 : disable 1 : enable
D4	ISA and PCI concurrent function 0 : disable 1 : enable when enabled, M1523 allows the PCI master to get the ownership of PCI bus when ISA bus master is active.
D5	Select ISA master to PCI Bus request method 0 : Bus request at each time ISA MASTER request the bus 1 : Bus request only MASTER assert command
D6	I/O posted-write buffer 0 : disable 1 : enable
D7	reserved.(must be 0)

Index 41h (00h)

D0 ISA I/O recovery feature
0 : disable ISA I/O recovery
1 : enable ISA I/O recovery

D1 On-Chip I/O recovery
0 : disable on-chip I/O recovery
1 : enable on-chip I/O recovery
Bit0 is used to enable ISA I/O recovery timer. Bit1 is used for M1523 internal I/O Port I/O recovery, but Bit0 must be 1 first.

D5-D2 I/O recovery period
0000 : 0 us
0001 : 0.25 us (2/ATCLK)
0010 : 0.5 us (4/ATCLK)
0011 : 0.75 us (6/ATCLK)
0100 : 1 us (8/ATCLK)
0101 : 1.25 us (10/ATCLK)
0110 : 1.5 us (12/ATCLK)
0111 : 1.75 us (14/ATCLK)
1000 : 2 us (16/ATCLK)
1001 : 2.25 us (18/ATCLK)
1010 : 2.5 us (20/ATCLK)
1011 : 2.75 us (22/ATCLK)
1100 : 3 us (24/ATCLK)
1101 : 3.25 us (26/ATCLK)
1110 : 3.5 us (28/ATCLK)
1111 : 3.75 us (30/ATCLK)

D6 PS/2 Mouse/AT Mouse select
0 : AT mouse (without latch)
1 : With PS/2 mouse (latch)

D6 is used to latch IRQ12, when IRQ12 goes high. And IRQ12 will be released when read Port 60H. If '0', IRQ12 will be compatible to AT definition. If '1', IRQ12 will be compatible to PS/2 definition.

D7 PS2 Keyboard present feature
0 : Without PS/2 keyboard(AT IRQ1, without latch)
1 : With PS/2 Keyboard (latch)

D7 is used to latch IRQ1, when IRQ1 goes high. And IRQ1 will be released when read Port 60H. If '0', IRQ1 will be compatible to AT definition. If '1', IRQ1 will be compatible to PS/2 definition. This bit is also used to select AT/PS2 internal Keyboard Controller.

Index 42h (00h)

D2-D0 ISA clock select
000 : 7.16 Mhz (OSC14M/2)
001 : PCICLK/2
010 : PCICLK/3
011 : PCICLK/4
100 : PCICLK/5
101 : PCICLK/6
110 : reserved
111 : reserved

D3 Decoupled refresh control
0 : Normal refresh
1 : Decoupled refresh

This bit is 0, refresh master will own ISA and PCI bus. When this bit is set to 1, refresh master will only own ISA bus.

D4 reserved.(must be 0)

D5 reserved.(must be 0)

D6 DMA High Page register
0 : disable.(24 bits addressing)
1 : enable.(32 bits addressing)

D7 Configuration Port read data mask function.
0 : Normal I/O read/write
1 : 0's are read from 40-FFh

Index 43h ISA Bus cycle control (00h)

D1-D0 16 bit ISA I/O command insert wait count
00 : normal 16-bit access
01 : insert 1-wait
10 : insert 2-wait
11 : insert 3-wait

D3-D2 16 bit ISA memory command insert wait count
00 : normal 16-bit access
01 : insert 1-wait
10 : insert 2-wait
11 : insert 3-wait

D5-D4 ISA Refresh period setting
00 : 15us refresh period
01 : 30us
10 : 60us
11 : 120us

D6 Coprocessor interface
This bit is used to support the coprocessor error reporting or as an external IRQ13 for pin FERRJ.
0 : disable (Pin FERRJ as IRQ13; IGNNEJ always 1)
1 : enable (Pin FERRJ as FERRJ)

D7 Port-92H RC/GATEA20 Selection
0 : Disable Port-92h
1 : Enable Port-92h

Index 44h (00h)

D3-D0 On-chip IDE master INTAJ routing when native mode is enable.

D3	D2	D1	D0	
0	0	0	0	Disable
0	0	0	1	IRQ9
0	0	1	0	IRQ3
0	0	1	1	IRQ10
0	1	0	0	IRQ4
0	1	0	1	IRQ5
0	1	1	0	IRQ7
0	1	1	1	IRQ6
1	0	0	0	reserved
1	0	0	1	IRQ11
1	0	1	0	reserved
1	0	1	1	IRQ12
1	1	0	0	reserved
1	1	0	1	IRQ14
1	1	1	0	reserved
1	1	1	1	IRQ15

D4 On-chip IDE master INTAJ level to edge transform
0 : disable.(bypass)
1 : enable.(level -> edge)

D5 ATA bus secondary IDE IRQ connected to IRQ15 or SIRQI define.
0 : IRQ connected to IRQ15 of motherboard
1 : IRQ connected to SIRQI of motherboard

D6 On chip I/O decode (except DMA I/O port is always subtractive)
0 : positive decode
1 : subtractive decode

D7 System software reset control
0 : When software reset, the CPURST is active but RSTDRV is inactive
1 : When software reset, both CPURST and RSTDRV are active

Index 45h (00h)

D0 Parity check
0 : disable
1 : enable

D1 reserved (must be 0)

D2 reserved (must be 0)

D3 Discard delay transaction counter
0 : disable
1 : enable

D4 reserved.(must be 0)

D5 reserved.(must be 0)

D6 reserved.(must be 0)

D7 PCI interrupt polling mode
0 : disable
1 : enable

Index 46h Software test mode setting (00h)

D3-D0 reserved (must be 0000b)

D4 IDE ATA bus pad control
0 : disable internal IDE
1 : use internal IDE
When external IDE chip is used on board, this bit must be '0'.
When on-chip internal IDE is used, this bit must be '1'.

D7-D5 reserved (must be 000b)

Index 47h BIOS chip select control (00h)

D0 ROM size define for ROM chip select decode
0 : 64 KB(000F0000-000FFFFF, FFFF0000 -FFFFFFFF)
1 : 128KB(000E0000-000EFFFF, 000F0000-000FFFFF, FFFF0000-FFFFFFFF).

D2-D1 Extended ROM region

D1 0 : disable;
1 : enable; ROMCSJ will be active when access memory FFFE0000-FFFEFFFF.

D2 0 : disable;
1 : enable; ROMCSJ will be active when accessing memory FFFC0000-FFFDFFFFh. This bit enlarges the ROM size to 256 KB.

D4-D3 Share memory VGA BIOS region decode

D3 0 : disable
1 : enable; ROMCSJ will be active when accessing memory 000C0000-000C7FFFh.

D4 0 : disable;
1 : enable;ROMCSJ will be active when accessing memory 000C8000-000CFFFFh.

D5 0 : disable
1 : enable;ROMCSJ will be active when access memory 000D0000-000DFFFFh.

D6 Flash ROM read/write control(write protest)
0 : disable;ROM chip select will be active only in memory read cycle.
1 : enable;ROM chip select will be active in memory read/write cycle.

D7 SA16 inverter control
0 : Normal SA16
1 : Invert SA16 when BIOSCSJ active

Index 48h PCI Interrupt to ISA IRQ routing table (00h)

D3-D0 INT-1 to ISA IRQ routing table

D7-D4 INT-2 to ISA IRQ routing table

INT1-INT8 Routing Table:D3-D0 or D7-D4

D3 D2 D1 D0 or D7 D6 D5 D4	
0 0 0 0	Disable
0 0 1 0	IRQ3
0 1 0 0	IRQ4
0 1 1 0	IRQ7
1 0 0 0	reserved
1 0 1 0	reserved
1 1 0 0	reserved
1 1 1 0	reserved
0 0 0 1	IRQ9
0 0 1 1	IRQ10
0 1 0 1	IRQ5
0 1 1 1	IRQ6
1 0 0 1	IRQ11
1 0 1 1	IRQ12
1 1 0 1	IRQ14
1 1 1 1	IRQ15

The BIOS should inhabit to set the reserved value. The reserved setting will disable the IRQ at the present design.

Index 49h PCI Interrupt to ISA IRQ routing table(00h)

D3-D0 INT-3 to ISA IRQ routing table

D7-D4 INT-4 to ISA IRQ routing table

Index 4Ah PCI Interrupt to ISA IRQ routing table(00h)

D3-D0 INT-5 to ISA IRQ routing table

D7-D4 INT-6 to ISA IRQ routing table

Index 4Bh PCI Interrupt to ISA IRQ routing table(00h)

D3-D0 INT-7 to ISA IRQ routing table

D7-D4 INT-8 to ISA IRQ routing table

Index 4Ch PCI INT to ISA Level to Edge transfer(00h)

D0 INT-1
D1 INT-2
D2 INT-3
D3 INT-4
D4 INT-5
D5 INT-6
D6 INT-7
D7 INT-8

0 : disable, PCI Level trigger INT will be bypassed as level trigger to internal interrupt controller.
1 : enable, PCI Level trigger INT will be transformed to Edge trigger to internal interrupt controller.

Index 48h to 4Ch are used to define 8 PCI INT channel's routing tables for ISA system. For PCI INT is level, not edge trigger. 4Ch index is used to enable each INT channel from level to edge transfer.

Index 4Dh Steerable IRQs SIRQI, SIRQII Interrupt to ISA IRQ routing table (00h)

D3-D0 SIRQI to ISA IRQ routing table
D7-D4 SIRQII to ISA IRQ routing table

Above Routing Table : D3-D0 or D7-D4

D3 D2 D1 D0 or D7 D6 D5 D4	
0 0 0 0	Disable
0 0 1 0	IRQ3
0 1 0 0	IRQ4
0 1 1 0	IRQ7
1 0 0 0	reserved
1 0 1 0	reserved
1 1 0 0	reserved
1 1 1 0	reserved
0 0 0 1	IRQ9
0 0 1 1	IRQ10
0 1 0 1	IRQ5
0 1 1 1	IRQ6
1 0 0 1	IRQ11
1 0 1 1	IRQ12
1 1 0 1	IRQ14
1 1 1 1	IRQ15

The BIOS should inhabit to set the reserved value. The reserved setting will disable the IRQ at the present design.

Index 4Fh-4Eh Programmable chip select (pin PCSJ) address define. (0002h)

D15-D2 define the programmable I/O port address A15-A2.

D1-D0
00 : only compare A15-A2 for chip select signal PCSJ.
01 : only compare A15-A3 for chip select signal PCSJ.
10 : disable. Chip select signal PCSJ is always inactive('1').
11 : only compare A15-A4 for chip select signal PCSJ.

Index 51h-50h I/O cycle Posted-write first port definition. (0000h)

D15
0 : disable
1 : enable

D14-D12 reserved

D11-D0 define the sound card first I/O port for post-write.

Index 53h-52h I/O cycle posted-write second port definition. (0000h)

D15
0 : disable
1 : enable

D14-D12 reserved

D11-D0 define the sound card second I/O port for post-write.

Index 54h Hardware setting status bits (Read only) (3Fh)

D0 reserved. (must be '1')

D1 SPLED hardware setting status.
0: Pull-low, DMA DACKJ[7:5,3:0] polling mode is enabled.
1: Pull-high, DMA DACKJ[7:5,3:0] polling mode is disabled.

D2 SPKR hardware setting status.
0: Pull-low, internal Keyboard controller is enabled.
1: Pull-high, internal Keyboard controller is disabled.

D3	PHOLDJ hardware setting status. 0: Pull-low, internal Real-Time Clock is enabled. 1: Pull-high, internal Real-Time Clock is disabled.
D4	TC hardware setting status. 0: Pull-low, external I/O APIC is supported. 1: Pull-high, external I/O APIC is not supported.
D7-D5	reserved

PMU Configuration Registers

Index 55h	TURBO Switch Command & Status register (1Ah)
D0	SMI acknowledge feature 0 : internal SMIACTJ inactivated 1 : internal SMIACTJ activated
D1	Software TURBO switch setting Control 0 : SW deturbo setting 1 : SW turbo setting
D2	Pin EXTSW used as HW TURBO switch 0 : disable HW TURBO switch 1 : enable HW TURBO switch
D3	HW TURBO switch status(ready only when D2 is '1') 0 : HW TURBO is in de-turbo status (OFF) 1 : HW TURBO is in turbo status (ON)
D4	TURBO performance status (Read Only) 0 : system is in de-turbo status (TURBO LED is OFF) 1 : system is in turbo status (TURBO LED is ON)
D7-D5	reserved.

Index 56h	(00h)
D1-D0	Power management system mode state 00 : ON 01 : DOZE 10 : STANDBY 11 : SUSPEND
D2	PMU ON/OFF 0 : disable PMU 1 : enable PMU This is used to disable/enable PMU controller.
D3	software incurs STPCLKJ control 0 : de-activate STPCLKJ 1 : activate STPCLKJ and this bit is reset to 0 when STPCLKJ is active
D4	DMA/PCI Master request de-assert STPCLKJ 0 : Enable.This event will deassert STPCLKJ. 1 : Disable. This event will not deassert STPCLKJ.
D5	INTR/NMI event deassert STPCLKJ 0 : Enable.This event will deassert STPCLKJ 1 : Disable. This event will not deassert STPCLKJ
D6	Software SMI 0 : Disable. Software de_asserts SMIJ 1 : Enable. Software activates SMIJ
D7	SMI event to incur active SMIJ 0 : disable 1 : enable

SMI CONTROL REGISTERS

Index 57h	Select following event to control system to enter ON, DOZE, STANDBY, SUSPEND mode if the selected event idle over the programmed time in port 5Fh, 64h, 65h respectively. (00h)
D0	reserved.
D1	VGA select (Mem AB region write, 3B0-3BFH write, 3C0-3CFH write)
D2	reserved.
D3	IRQ select
D6-D4	reserved.
D7	DRQ select

Index 58h	**(00h)**
D0	GP0 select 0 : not selected for detection 1 : selected for detection
D2-D1	Ring input counter count definition. 00 : 3 01 : 6 10 : 10 11 : 15
D4-D3	Ring input polarity definition.
D3	low to high transition 0 : disable 1 : enable. Low to high transition will generate an event count, the counter will increase by one.
D4	high to low transition 0 : disable 1 : enable. High to low transition will generate an event count, the counter will increase by one.
D5	Ring input event to generate SMIJ 0 : Disable. The event will not activate SMIJ. 1 : Enable. The event will activate SMIJ. After activating SMIJ, software should reset this bit to clear the event.
D6	External switch event to generate SMIJ. 0 : Disable. The event will not activate SMIJ. 1 : Enable. The event will activate SMIJ. After activating SMIJ, software should reset this bit to clear the event.
D7	TURBO switch event to incur active SMIJ. 0 : Disable. The event will not activate SMIJ. 1 : Enable. The event will activate SMIJ. After activating SMIJ, software should reset this bit to clear the event.

Index 59h	(00h)
D0	VGA timer time-out generates SMIJ 0 : Disable. If the event is idle over the programmed time in port 5Fh, SMIJ will not activate. 1 : Enable. If the event idle over the programmed time in port 5Fh, SMIJ will activate.
D4-D1	reserved.
D5	Mode timer time-out generates SMIJ 0 : Disable. If the event idle over the programmed time in port 64h, SMIJ will not activate. 1 : Enable. If the event idle over the programmed time in port 64h, SMIJ will activate.
D6	RTC alarm event (IRQ8J active) generate SMIJ. 0 : Disable. If the event occurs, SMIJ will not activate. 1 : Enable. If the event occurs, SMIJ will activate. After activating SMIJ, software should clear this bit to clear the event.
D7	IN timer time-out generates SMIJ 0 : Disable. If the event idle over the programmed time in port 65h, SMIJ will not activate. 1 : Enable. If the event idle over the programmed time in port 65h, SMIJ will activate.

Index 5Ah (00h)
After port 59h timeout event incurs active SMIJ, another SMIJ will be re-activated if the following selected event occurs.

D0 VGA access re-activates SMIJ
0 : disable
1 : enable

D2-D1 reserved

D3 GP0 access re-activate SMIJ
0 : disable
1 : enable

D4 reserved.

D5 IRQ active re-activate SMIJ
0 : disable.
1 : enable
After re-activating SMIJ, software should reset this bit to clear the event.

D6 DRQ active re-activate SMIJ
0 : disable
1 : enable
After re-activating SMIJ, software should reset this bit to clear the event.

D7 IN access re-activate SMIJ
0 : disable
1 : enable
After re-activating SMIJ, software should reset this bit to clear the event.

Index 5Bh SMIJ cause (00h)

D7(R/W) IRQ/NMI de-asserts STPCLKJ.
This bit will function only if port 56h bit5='1'.
0 : Any IRQ or NMI event will de-assert STPCLKJ regardless which event is selected in port 5Ch, 5Dh.
1 : Only selected IRQ or NMI event in ports 5Ch, 5Dh will de-assert STPCLKJ.

D6(R/W) DRQ/PHOLDJ de-asserts STPCLKJ.
This bit will function only if port 56h bit4='1'.
0 : Any DRQ or PHOLDJ event will de-assert STPCLKJ regardless which event is selected in port 5Eh.
1 : Only selected DRQ or PHOLDJ event in port 5Eh will de-assert STPCLKJ

D5 reserved.

D4-D0 cause (Read Only)

0 0 0 0 0	NONE
0 0 0 0 1	VGA timer time-out
0 0 0 1 0	reserved.
0 0 0 1 1	reserved.
0 0 1 0 0	reserved.
0 0 1 0 1	reserved.
0 0 1 1 0	Mode timer time-out
0 0 1 1 1	IN timer time-out
0 1 0 0 0	IRQ active
0 1 0 0 1	DRQ active
0 1 0 1 0	IN access
0 1 1 0 0	EXTSW active (external suspend switch input)
0 1 1 0 1	RTC alarm
0 1 1 1 1	Software SMI
1 0 0 0 1	VGA access (W A0000~BFFFFH, port 3B0~3BFh, port 3C0-3CFh)
1 0 0 1 0	reserved.
1 0 0 1 1	reserved.
1 0 1 0 0	GP0 access (R/W GP0 defined area)
1 0 1 0 1	reserved.
other	reserved

Index 5Ch IRQ event channel select (00h)
D0 IRQ0
D1 IRQ1
D2 NMI
D3 IRQ3
D4 IRQ4
D5 IRQ5
D6 IRQ6
D7 IRQ7
0 : not selected in the IRQ group event
1 : selected in the IRQ group event

Index 5Dh IRQ event channel select (00h)
D0 IRQ8
D1 IRQ9
D2 IRQ10
D3 IRQ11
D4 IRQ12
D5 IRQ13
D6 IRQ14
D7 IRQ15
0 : not selected in the IRQ group event
1 : selected in the IRQ group event

Index 5Eh DRQ event channel select (00h)
D0 DRQ0
D1 DRQ1
D2 DRQ2
D3 DRQ3
D4 PHOLDJ
D5 DRQ5
D6 DRQ6
D7 DRQ7
0 : not selected in the DRQ group event
1 : selected in the DRQ group event

The time base should be associated with time count to choose proper time interval for timeout counter. The relationship is

time count	time base			
	1s	10s	1min	10min
0	0	0	0	0
1	1	10	1	10
2	2	20	2	20
3	3	30	3	30
4	4	40	4	40
5	5	50	5	50
6	6	60	6	60
7	7	70	7	70
8	8	80	8	80
9	9	90	9	90
10	10	100	10	100
11	11	110	11	110
12	12	120	12	120
13	13	130	13	130
14	14	140	14	140
15	15s	150s	15m	150m

The minimum interval is 1 sec. The maximum period is 150mins. If Index 66h bit4 = 1, then the period is doubled.

Index 5Fh (00h)
D1D0 Time Base select for VGA timer
00 : 1sec
01 : 10sec
10 : 1min
11 : 10min

D2 Timer count/reset
0 : timer reset
1 : timer count

D3 reserved.

D7-D4 set the timeout period of VGA timer
VGA timer is reset when MEMW A0000-BFFFFh or IOR/W 3B0-3BFh,3C0-3CFH,
0 : timer disabled
1-15 : time count

Index 60h (00h)
D[7-0] defined GP0 memory address A[23-16]

Index 61h (00h)
D[7-0] defined GP0 memory address A[31-24]

Index 62h (00h)
D[7-0] defined GP0 memory address A[23-16] mask bits

Index 63h (00h)
D[7-0] defined GP0 memory address A[31-24] mask bits

Index 64h (00h)

D1D0 Time Base select for Mode (On, Doze, Standby, Suspend) timer
00 : 1s
01 : 10s
10 : 1min
11 : 10min

D2 Timer count/reset
0 : timer reset
1 : timer count

D3 reserved

D7-D4 set the time period for Mode transition (ex. ON mode to DOZE mode)
0 : timer disabled
1-15 : time count

Index 65h (00h)

D1D0 Time Base select for IN timer
00 : 1s
01 : 10s
10 : 1min
11 : 10min

D2 Timer count/reset
0 : timer reset
1 : timer count

D3 reserved

D7-D4 set the time-out period of IN timer
IN timer is reset by asserting IRQ1, IRQ12, IRQ3, IRQ4 as port 66h selected.
0 : timer disabled
1-15 : time count

Index 66h (00h)

D0 VGA event by monitoring memory write A0000H-B0000H
0 : not selected
1 : selected

D1 VGA event by monitoring I/O write 3B0h-3BFH, 3C0h-3CFh.
0 : not selected
1 : selected

D2 Clock throttle control
0 : disable
1 : enable

D3 GP0 memory region definition
0 : disable
1 : enable

D4 Double counter time base
0 : disable
1 : enable

D7-D5 IN event by monitoring IRQ1 (KB, always select) or IRQ12 (ps/2 mouse, option) or IRQ4 (com1,option) or IRQ3 (com2,option)

D5 IN monitor IRQ12
0 : not selected
1 : selected

D6 IN monitor IRQ4
0 : not selected
1 : selected

D7 IN monitor IRQ3
0 : not selected
1 : selected

Index 67h (00h)

D1-D0 External switch input event cause select

D0 low to high transition
0 : Disable
1 : Enable, i.e. a low to high transition will create an event.

D1 high to low transition
0 : Disable
1 : Enable, i.e. a high to low transition will create an event.

D4-D2 Mode LED control

D3-D2 LED clock period define
00 : 1.0 sec
01 : 2.0 sec
10 : 0.4 sec
11 : 0.8 sec

D4 LED
0 : disable.(default)
1 : enable.

D7-D5 reserved.

Index 68h (00h)
D7-D0 Clock throttle STPCLKJ low time definition
They define the asserted period of the STPCLKJ signal during clock throttle when 66h bit 2 = '1'.

D7-D0	low time
00000000	always low until trigger condition
00000001	1x16 us
00000010	2x16 us
00000011	3x16 us
.....	.....
11111111	255x16 us

Index 69h (00h)
D7-D0 Clock throttle STPCLKJ high time definition
They define the deasserted period of the STPCLKJ signal during clock throttle when 66h bit 2 = '1'.

D7-D0	high time
00000000	always high until another enable signal
00000001	1x16 us
00000010	2x16 us
00000011	3x16 us
.....	.....
11111111	255x16 us

Index 6Ah (Read only, 00h)

D4-D0 reserved.
D5 DOZE mode timer time-out status
D6 STANDBY mode timer time-out status
D7 SUSPEND mode timer time-out status

Index 6Bh (00h)

D[7:0] shadow I/O port for port 70H data
D[7:0]=I/O port 70h D[7:0]

When system asserts I/O write port 70H (RTC) command, the data are also kept in this index register. In SMI routine, system cannot write data into this port, but it can read back this port data which is the last data system written to port 70h. Before exiting SMI routine, system will write RTC port 70h the value coming from this index.

Index 6Ch APIC chip select address range define.

D7 reserved.

D6 This bit defines address bit 10 is decoded or not.
0 : bit 10 is decoded.
1 : bit 10 is 'don't care' when decode.

D5 ~D2 These 4 bits are compared with PCI address AD[15:12] respectively.

D1 ~D0 These 2 bits are compared with PCI address AD[11:10] respectively. But when D6 is '1', the AD[10] will not be compared.

Index 6Dh reserved

Index 6Eh ISP shadow I/O port select (00h)
The following is preliminary index for accessing shadow ISP ports:

D7-D5 --> select device
D4-D0 --> select device's ports

D7D6D5
000 : reserved
001 : 8254 programmable timer
010 : master 8259
011 : slave 8259
100 : master 8237
101 : slave 8237
110 : reserved
111 : reserved

Direct Memory Access - << 8237 >>

D4D3D2D1D0 :

0 0 0 0 0	master-37 channel[0] Mode register
0 0 0 0 1	master-37 channel[1] Mode register
0 0 0 1 0	master-37 channel[2] Mode register
0 0 0 1 1	master-37 channel[3] Mode register
0 0 1 0 0	master-37 Request register & Mask register combined
0 0 1 0 1	master-37 channel[0] Base Address register Low byte
0 0 1 1 0	master-37 channel[0] Base Address register High byte
0 0 1 1 1	master-37 channel[0] Base Word Count register Low byte
0 1 0 0 0	master-37 channel[0] Base Word Count register High byte
0 1 0 0 1	master-37 channel[1] Base Address register Low byte
0 1 0 1 0	master-37 channel[1] Base Address register High byte
0 1 0 1 1	master-37 channel[1] Base Word Count register Low byte
0 1 1 0 0	master-37 channel[1] Base Word Count register High byte
0 1 1 0 1	master-37 channel[2] Base Address register Low byte
0 1 1 1 0	master-37 channel[2] Base Address register High byte
0 1 1 1 1	master-37 channel[2] Base Word Count register Low byte
1 0 0 0 0	master-37 channel[2] Base Word Count register High byte
1 0 0 0 1	master-37 channel[3] Base Address register Low byte
1 0 0 1 0	master-37 channel[3] Base Address register High byte
1 0 0 1 1	master-37 channel[3] Base Word Count register Low byte
1 0 1 0 0	master-37 channel[3] Base Word Count register High byte
Others :	reserved

D4D3D2D1D0:

0 0 0 0 0	slave-37 channel[0] Mode register
0 0 0 0 1	slave-37 channel[1] Mode register
0 0 0 1 0	slave-37 channel[2] Mode register
0 0 0 1 1	slave-37 channel[3] Mode register
0 0 1 0 0	slave-37 Request register & Mask register combined
0 0 1 0 1	slave-37 channel[0] Base Address register Low byte
0 0 1 1 0	slave-37 channel[0] Base Address register High byte
0 0 1 1 1	slave-37 channel[0] Base Word Count register Low byte
0 1 0 0 0	slave-37 channel[0] Base Word Count register High byte
0 1 0 0 1	slave-37 channel[1] Base Address register Low byte
0 1 0 1 0	slave-37 channel[1] Base Address register High byte
0 1 0 1 1	slave-37 channel[1] Base Word Count register Low byte
0 1 1 0 0	slave-37 channel[1] Base Word Count register High byte
0 1 1 0 1	slave-37 channel[2] Base Address register Low byte
0 1 1 1 0	slave-37 channel[2] Base Address register High byte
0 1 1 1 1	slave-37 channel[2] Base Word Count register Low byte
1 0 0 0 0	slave-37 channel[2] Base Word Count register High byte
1 0 0 0 1	slave-37 channel[3] Base Address register Low byte
1 0 0 1 0	slave-37 channel[3] Base Address register High byte
1 0 0 1 1	slave-37 channel[3] Base Word Count register Low byte
1 0 1 0 0	slave-37 channel[3] Base Word Count register High byte
Others	reserved

Interrupt Controller << 8259 >>

D4D3D2D1D0 :

0 0 0 0 0	master-59 ICW1
0 0 0 0 1	master-59 ICW2
0 0 0 1 0	master-59 ICW3
0 0 0 1 1	master-59 ICW4
0 0 1 0 0	master-59 OCW1
0 0 1 0 1	master-59 reserved (OCW2)
0 0 1 1 0	master-59 OCW3
Others	reserved

D4D3D2D1D0 :

0 0 0 0 0	slave-59 ICW1
0 0 0 0 1	slave-59 ICW2
0 0 0 1 0	slave-59 ICW3
0 0 0 1 1	slave-59 ICW4
0 0 1 0 0	slave-59 OCW1
0 0 1 0 1	slave-59 reserved (OCW2)
0 0 1 1 0	slave-59 OCW3
Others	reserved

System Controller << 8254 >>

D4D3D2D1D0 :

0 0 0 0 0	Counter[0] Low byte
0 0 0 0 1	Counter[0] High byte
0 0 0 1 0	Counter[1] Low byte
0 0 0 1 1	Counter[1] High byte
0 0 1 0 0	Counter[2] Low byte
0 0 1 0 1	Counter[2] High byte
Others	reserved

Index 6Fh ISP shadow I/O select port data.(read only, 00h)

Index FFh-70h reserved

4.1.2 Function 1 : IDE master configuration registers

Before programming IDE master, the configuration register 46h bit4 of function 0 must be set to '1'.

Byte Index	Definition	R/W	Expected Value
1, 0	Vender ID	R	10B9H
3, 2	Device ID	R	5219H
5, 4	Command	R/W	0000H
7, 6	Status	R/W	0280H
8	Revision ID	R	20H
B, A, 9	Class Code	R	0101FAH
0EH	Header Type	R	00H
13H - 10H	Base Address Regs	R/W	000001F1H
17H - 14H	Base Address Regs	R/W	000003F5H
1BH - 18H	Base Address Regs	R/W	00000171H
1FH - 1CH	Base Address Regs	R/W	00000375H
23H - 20H	Base Address Regs	R/W	0000F001H
3CH	Interrupt Line	R/W	00000000H
3DH	Interrupt Pin	R/W	00000001H
3EH	Min_Gnt	R	00000002H
3FH	Max_Lat	R	00000004H

Index 50h R/W (00h)
CFG : Configuration register

Bit 0 enable internal IDE function
0 : disable(default)
1 : enable

Bit 1 read programming interface bits 6-4
0 : programming interface bits 6-4 are reserved (always 0)
1 : normal read (default)

Bit 2 reserved

Bit 3 CFG_BEJDEC
0 : decode 3F6H and 376H that only use address
1 : use byte enable decoding

Bit 4 Resolving INTA# select
force INTA# generate 2 pulse when there is 2 interrupt pending in the chip.
default to '1', enable.

Bit 5 only decodes the third byte of BASE2 and BASE4 during native mode
0 : all 4 bytes are master IDE's cycle (default)
1 : only the 3rd byte is master IDE's cycle

Index 51h R/W (00h)
reset and testing register

Bit 0 CFG_FIFO_TEST, FIFO test mode enable
0 : disable(default)
1 : enable

Bit 1 CFG_LATEST, latency timer test mode enable
0 : disable(default)
1 : enable

Bit 2 CFG_ATA_TEST, auto polling Test mode enable
0 : disable(default)
1 : enable

Bit 3 reserved

Bit 4 CFG_RSTCH1, soft reset
Writing a '1' to this bit will reset the ATASTATE and AUTOPOL1.
It generates a one cycle pulse only.

Bit 5 CFG_RSTCH2, soft reset
Writing a '1' to this bit will reset the ATASTATE and AUTOPOL2.
It generates a one cycle pulse only.

Bit 6 CFG_SOFTRST, soft reset
Writing a '1' to this bit will reset all the blocks except the configuration space. It generates a one cycle pulse only.

Bit 7: CFG_CHIPRST, chip reset
Writing a '1' to this bit will reset the whole chip as hardware reset.
It generates a one cycle pulse only.

Index 52h R/W (00h)
CFG_USE_CMDT and CFG_FIFO _DEPTH

Bit 3-0 CFG_USE_CMDT
bit 0 forces the drive 0 of primary channel to use command block timing register for data transfer
bit 1 forces the drive 1 of primary channel to use command block timing register for data transfer
bit 2 forces the drive 0 of secondary channel to use command block timing register for data transfer
bit 3 forces the drive 1 of secondary channel to use command block timing register for data transfer

Bit 6-4 CFG_FIFO_DEPTH
indicates FIFO depth by quadruple word count (8 bytes), and only 1 bit can be 1 in this field

Index 54h R/W (00h)
FIFO_SHLD0 FIFO threshold of primary channel drive 0

Bit 4-0 FIFO threshold register
Define when to start master transaction

Bit 7-6 Operation level
Define the slave operation level

Index 55h R/W (00h)
FIFO_SHLD1 FIFO threshold of primary channel drive 1

Bit 4-0 FIFO threshold register
Define when to start master transaction

Bit 7-6 Operation level
Define the slave operation level

Index 56h R/W (00h)
FIFO_SHLD2 FIFO threshold of secondary channel drive 0

Bit 4-0 FIFO threshold register
Define when to start master transaction

Bit 7-6 Operation level
Define the slave operation level

Index 57h R/W (00h)

FIFO_SHLD3 FIFO threshold of secondary channel drive 1

Bit 4-0 FIFO threshold register
Define when to start master transaction

Bit 7-6 Operation level
Define the slave operation level

Index 58h R/W (00h)
SLV_AST1: Primary channel address setup timing register

Bits 2-0 Address setup count
Default: 000 => 8 clks
001 => 1 clks
010 => 2 clks
011 => 3 clks
100 => 4 clks
101 => 5 clks
110 => 6 clks
111 => 7 clks

Bits 7-3 reserved

Index 59h R/W (00h)
SLV_CMDT1 Primary channel command block timing register

Bits 3-0 Command recovery count
Default: 0000 => 16 clks
0001 => 1 clks
0010 => 2 clks
0011 => 3 clks
0100 => 4 clks
0101 => 5 clks
0110 => 6 clks
0111 => 7 clks
1000 => 8 clks
1001 => 9 clks
1010 => 10 clks
1011 => 11 clks
1100 => 12 clks
1101 => 13 clks
1110 => 14 clks
1111 => 15 clks

Bits 7-4 Command active count
Default: 0000 => 16 clks
0001 => 1 clks
0010 => 2 clks
0011 => 3 clks
0100 => 4 clks
0101 => 5 clks
0110 => 6 clks
0111 => 7 clks
1000 => 8 clks
1001 => 9 clks
1010 => 10 clks
1011 => 11 clks
1100 => 12 clks
1101 => 13 clks
1110 => 14 clks
1111 => 15 clks

Index 5Ah R/W (00h)
SLV_DRWT0: Primary channel Drive 0 data read/write timing register

Bits 3-0 Data read/write recovery count
Default: 0000 => 16 clks
0001 => 1 clks
0010 => 2 clks
0011 => 3 clks
0100 => 4 clks
0101 => 5 clks
0110 => 6 clks
0111 => 7 clks
1000 => 8 clks
1001 => 9 clks
1010 => 10 clks
1011 => 11 clks
1100 => 12 clks
1101 => 13 clks
1110 => 14 clks
1111 => 15 clks

Bits 7-4 Data read/write active count
Default: 0000 => 16 clks
0001 => 1 clks
0010 => 2 clks
0011 => 3 clks
0100 => 4 clks
0101 => 5 clks
0110 => 6 clks
0111 => 7 clks
1000 => 8 clks
1001 => 9 clks
1010 => 10 clks
1011 => 11 clks
1100 => 12 clks
1101 => 13 clks
1110 => 14 clks
1111 => 15 clks

Index 5Bh R/W (00h)

SLV_DRWT1 Primary channel Drive 1 data read/write timing register

Bits 3-0 Data read/write recovery count
Default: 0000 => 16 clks
0001 => 1 clks
0010 => 2 clks
0011 => 3 clks
0100 => 4 clks
0101 => 5 clks
0110 => 6 clks
0111 => 7 clks
1000 => 8 clks
1001 => 9 clks
1010 => 10 clks
1011 => 11 clks
1100 => 12 clks
1101 => 13 clks
1110 => 14 clks
1111 => 15 clks

Bits 7-4 Data read/write active count
Default: 0000 => 16 clks
0001 => 1 clks
0010 => 2 clks
0011 => 3 clks
0100 => 4 clks
0101 => 5 clks
0110 => 6 clks
0111 => 7 clks
1000 => 8 clks
1001 => 9 clks
1010 => 10 clks
1011 => 11 clks
1100 => 12 clks
1101 => 13 clks
1110 => 14 clks
1111 => 15 clks

Index 5Ch R/W (00h)
SLV_AST2: Secondary channel address setup timing register

Bits 2-0 Address setup count
Default: 000 => 8 clks
001 => 1 clks
010 => 2 clks
011 => 3 clks
100 => 4 clks
101 => 5 clks
110 => 6 clks
111 => 7 clks

Bits 7-3 reserved

Index 5Dh R/W (00h)
SLV_CMDT2: Secondary channel command block timing register

Bits 3-0 Command recovery count
Default: 0000 => 16 clks
0001 => 1 clks
0010 => 2 clks
0011 => 3 clks
0100 => 4 clks
0101 => 5 clks
0110 => 6 clks
0111 => 7 clks
1000 => 8 clks
1001 => 9 clks
1010 => 10 clks
1011 => 11 clks
1100 => 12 clks
1101 => 13 clks
1110 => 14 clks
1111 => 15 clks

Bits 7-4 Command active count
Default: 0000 => 16 clks
0001 => 1 clks
0010 => 2 clks
0011 => 3 clks
0100 => 4 clks
0101 => 5 clks
0110 => 6 clks
0111 => 7 clks
1000 => 8 clks
1001 => 9 clks
1010 => 10 clks
1011 => 11 clks
1100 => 12 clks
1101 => 13 clks
1110 => 14 clks
1111 => 15 clks

Index 5Eh R/W (00h)

SLV_DRWT2: Secondary channel Drive 0 data read/write timing register

Bits 3-0 Data read/write recovery count
Default: 0000 => 16 clks
0001 => 1 clks
0010 => 2 clks
0011 => 3 clks
0100 => 4 clks
0101 => 5 clks
0110 => 6 clks
0111 => 7 clks
1000 => 8 clks
1001 => 9 clks
1010 => 10 clks
1011 => 11 clks
1100 => 12 clks
1101 => 13 clks
1110 => 14 clks
1111 => 15 clks

Bits 7-4 Data read/write active count
Default: 0000 => 16 clks
0001 => 1 clks
0010 => 2 clks
0011 => 3 clks
0100 => 4 clks
0101 => 5 clks
0110 => 6 clks
0111 => 7 clks
1000 => 8 clks
1001 => 9 clks
1010 => 10 clks
1011 => 11 clks
1100 => 12 clks
1101 => 13 clks
1110 => 14 clks
1111 => 15 clks

Index 5Fh R/W (00h)
SLV_DRWT3: Secondary channel Drive 1 data read/write timing register

Bits 3-0 Data read/write recovery count
Default: 0000 => 16 clks
0001 => 1 clks
0010 => 2 clks
0011 => 3 clks
0100 => 4 clks
0101 => 5 clks
0110 => 6 clks
0111 => 7 clks
1000 => 8 clks
1001 => 9 clks
1010 => 10 clks
1011 => 11 clks
1100 => 12 clks
1101 => 13 clks
1110 => 14 clks
1111 => 15 clks

Bits 7-4 Data read/write active count
Default: 0000 => 16 clks
0001 => 1 clks
0010 => 2 clks
0011 => 3 clks
0100 => 4 clks
0101 => 5 clks
0110 => 6 clks
0111 => 7 clks
1000 => 8 clks
1001 => 9 clks
1010 => 10 clks
1011 => 11 clks
1100 => 12 clks
1101 => 13 clks
1110 => 14 clks
1111 => 15 clks

Index 60-61h read only (00h)
MAS_PRD_CNTR: master byte counter for each PRD table entry

Index 62h read only (00h)
PI_LMTR_CNT: latency timer of PCI interface

Index 63h read only (00h)

Bit 0 PI_LTOUT
latency timer expired indication

Index 64-65h read only (0000h)
ATA_BYTECNTR: byte counter for counting in ATA state machine

Index 66h read only (00h)
ATA_SECCNTR: sector count counter for counting in ATA state machine

Index 67h read only (00h)
ATA_BLKCNTR: block size counter for counting in ATA state machine

Index 68h read only (00h)
SLV_BLKSZ0: block size register of device 0 on primary channel

Index 69h read only (00h)
SLV_BLKSZ1: block size register of device 1 on primary channel

Index 6Ah read only (00h)
SLV_BLKSZ2: block size register of device 0 on secondary channel

Index 6Bh read only (00h)
SLV_BLKSZ3: block size register of device 1 on secondary channel

Index 6Ch read only (00h)
SLV_CH1SEC: primary channel sector count register
This register is the duplicate of 1F2

Index 6Dh read only (00h)
SLV_CH2SEC: secondary channel sector count register
This register is the duplicate of 172

Index 6Eh read only (00h)
SLV_CH1CMD: primary channel command register
This register is the duplicate of 1F7

Index 6Fh read only (00h)
SLV_CH2CMD: secondary channel command register
This register is the duplicate of 177

Index 70h read only (00h)
SLV_CH1BCL: primary channel byte count low register
This register is the duplicate of 1F4

Index 71h read only (00h)

SLV_CH1BCH: primary channel byte count high register
This register is the duplicate of 1F5

Index 72h read only (00h)
SLV_CH2BCL secondary channel byte count low register
This register is the duplicate of 174

Index 73h read only (00h)
SLV_CH2BCH secondary channel byte count high register
This register is the duplicate of 175

Index 74h read only (00h)

Bits 5-0 FIFO_FLAG
Indicates how many words are in FIFO currently. It is binary coded.

Bit 6 FIFO_OVERWR
'1' means error condition occurred that FIFO is over written.
This bit must be cleared by reset.

Bit 7 FIFO_OVERRD
'1' means error condition occurred that FIFO is over read.
This bit must be cleared by reset.

Index 75h read only (00h)

Bit 0 Primary channel interrupt status
0 : no interrupt pending
1 : interrupt pending

Bit 1 Secondary channel interrupt status
0 : no interrupt pending
1 : interrupt pending

Bit 2 Primary channel drive select (the duplicate of 1F6 bit 4)
0 : select drive 0
1 : select drive 1

Bit 3 Secondary channel drive select (the duplicate of 176 bit 4)
0 : select drive 2
1 : select drive 3

Index 76h read only (00h)

Bit 2-0 Primary channel's status
bit 0 - error
bit 1 - DRQ
bit 2 - busy

Bit 6-4 Secondary channel's status
bit 4 - error
bit 5 - DRQ
bit 6 - busy

Index 78h R/W (00h)

Bit 7-0 IDE clock's frequency (default value is 33 = 21H)

4.2 DMA Register Description.

a. Command Register, the same as 82C37
b. DMA Channel Mode Register, the same as 82C37
c. DMA Channel Extended Mode Register,
Channels 0-3 port address - 040Bh
Channels 4-7 port address - 04D6h

Bit No.	Bit Name	Bit function	Def.
[1-0]	DMA Channel Select	00 Channel 0(4) select 01 Channel 1(5) select 10 Channel 2(6) select 11 Channel 3(7) select	XX
[3-2]	Reserved		00
[5-4]	DMA Cycle Timing Mode	00 Compatible Timing 01 Compatible Timing 10 Compatible Timing 11 Type F	00
[7-6]	Reserved		00

Compatible Timing : runs at 9 SYSCLKs (1080 nsec/single cycle) and 8 SYSCLKs (960 nsec/cycle) during the repeated portion of a BLOCK or DEMAND mode.

Type F Timing : runs at 3 SYSCLKs (360 nsec/single cycle) and 2 SYSCLKs (240 nsec/ cycle) during the repeated portion of a BLOCK or DEMAND mode.

d. DMA Request Register, the same as 82C37
e. Mask Resister-Write Single Mask Bit, the same as 82C37
f. Mask Register-Write All Mask Register Bits, the same as 82C37
g. Status Register, the same as 82C37
h. DMA Base and Current Address Register 8237 Compatible Segment
i. DMA Base and Current Byte/Word Count Register 8237 Compatible Segment
j. DMA Memory Low/High Page Register
DMA Memory Base Low Page Register
DMA Channel 0 port address - 087h
DMA Channel 1 port address - 083h
DMA Channel 2 port address - 081h
DMA Channel 3 port address - 082h
DMA Channel 5 port address - 08Bh
DMA Channel 6 port address - 089h
DMA Channel 7 port address - 08Ah
DMA Memory Base High Page Register
(Before using 32-bit addressing, index 42h bit6 must be set to '1')
DMA Channel 0 port address - 487h
DMA Channel 1 port address - 483h
DMA Channel 2 port address - 481h
DMA Channel 3 port address - 482h
DMA Channel 5 port address - 48Bh
DMA Channel 6 port address - 489h
DMA Channel 7 port address - 48Ah
These bits form the full 32-bit address for a DMA transfer.
k. Clear Byte Pointer Flip-Flop, the same as 82C37
l. Master Clear, the same as 82C37
m. Clear Mask Register, the same as 82C37

4.3 TIMER UNIT Register Description

a. Timer Control Word Register, the same as 82C54
b. Interval Timer Read Back Command, the same as 82C54
c. Interval Timer Status Byte Format, the same as 82C54
d. Counter Latch Command Register, the same as 82C54
e. Counter Access Ports, the same as 82C54

4.4 INTERRUPT UNIT Register Description

Initialization Command Word 1 (ICW1) :

Port 020h (W/O) -- INT Controller 1
Port 0A0h (W/O) -- INT Controller 2

Bit 0	0 : No ICW4 needed 1 : ICW4 is needed (M1523 must write 1)
Bit 1	0 : Cascade Controller(M1523 must write 0) 1 : Single Controller
Bit 2	reserved
Bit 3	0 : Edge triggered interrupts for all channels 1 : Level triggered interrupts for all channels
Bit 4	Must be 1
Bit 7-5	reserved

Initialization Command Word 2 (ICW2):

Port 021h (W/O) -- INT Controller 1
Port 0A1h (W/O) -- INT Controller 2

Bit 2-0	reserved
Bit 7-3	Interrupt Vector Address

Initialization Command Word 3 (ICW3):

Port 021h (W/O) -- INT Controller 1

M1523 must be programmed to 04h, indicating INT of CTRL-2 is cascaded to IRQ[2] of CTRL-1.

Bit 7-0	0 : IR Input does not have a slave 1 : IR Input has a slave

Port 0A1h (W/O) -- INT Controller 2

M1523 must be programmed to 02h, indicating CTRL-2 is cascaded to IRQ[2] of CTRL-1.

Bit 2-0	Slave identification code
Bit 7-3	must be 0h

Initialization Command Word 4 (ICW4):

Port 021h (W/O) -- INT Controller 1
Port 0A1h (W/O) -- INT Controller 2

Bit 0	0 : MCS-80/85 Mode 1 : 80x86 Mode (M1523 must write 1)
Bit 1	0 : Normal EOI 1 : Auto EOI
Bit 3-2	0x : Non Buffered Mode 10 : Buffer Mode/Slave 11 : Buffer Mode/Master
Bit 4	0 : Not Specially Fully Nested Mode 1 : Specially Fully Nested Mode
Bit 7-5	must be 0h

Operation Command Word 1 (OCW1):

Port 021h (R/W) -- INT Controller 1
Port 0A1h (R/W) -- INT Controller 2

Bit 7-0	0 : Reset IRQ<x> mask 1 : Set IRQ<x> mask

Operation Command Word 2 (OCW2):
Port 020h (W/O) -- INT Controller 1
Port 0A0h (W/O) -- INT Controller 2

Bit 2-0	L2,L1,L0 - Interrupt Level Select 000 : IRQ<0(8)> select 001 : IRQ<1(9)> select 010 : IRQ<2(10)> select 011 : IRQ<3(11)> select 100 : IRQ<4(12)> select 101 : IRQ<5(13)> select 110 : IRQ<6(14)> select 111 : IRQ<7(15)> select
Bit 4-3	Must be 00b to select OCW2
Bit 7-5	EOI,SL,R 000 : Rotate in Auto EOI Command(Clear) 001 : Non Specific EOI Command 010 : Set Priority Command * L2-L0 are used 011 : * Specific EOI Command 100 : Rotate in Auto EOI Command(Set) 101 : Rotate Non Specific EOI Command 110 : * Set Priority Command 111 : * Rotate on Specific EOI Command

Operation Command Word 3 (OCW3):

Port 020h (R/W) -- INT Controller 1
Port 0A0h (R/W) -- INT Controller 2

Bit 1-0	0x:No Action 10 : Buffer Mode/Slave 10 : Read IRQ Register 11 : Read IS Register
Bit 2	0 : No Poll Command 1 : Poll Command
Bit 4-3	Must be 01b to select OCW3
Bit 6-5	0x : No Action 10 : Reset Special Mask Mode 11 : Set Special Mask Mode
Bit 7	Reserved, must be 0b

Interrupt Unit Edge/Level Control Register (ELCR):

Port 04D0h (R/W) -- INT Controller 1
Port 04D1h (R/W) -- INT Controller 2

Bit 0	0 : IRQ<0(8)> Edge trigger 1 : IRQ<0(8)> Level trigger
Bit 1	0 : IRQ<1(9)> Edge trigger 1 : IRQ<1(9)> Level trigger
Bit 2	0 : IRQ<2(10)> Edge trigger 1 : IRQ<2(10)> Level trigger
Bit 3	0 : IRQ<3(11)> Edge trigger 1 : IRQ<3(11)> Level trigger
Bit 4	0 : IRQ<4(12)> Edge trigger 1 : IRQ<4(12)> Level trigger
Bit 5	0 : IRQ<5(13)> Edge trigger 1 : IRQ<5(13)> Level trigger
Bit 6	0 : IRQ<6(14)> Edge trigger 1 : IRQ<6(14)> Level trigger
Bit 7	0 : IRQ<7(15)> Edge trigger 1 : IRQ<7(15)> Level trigger

4.5 NMI Registers

NMI Enable/Disable and RTC Address register:

Port 70h	**(Write Only)**
Default value	0xxxxxxxb
Bit 6-0	RTC Memory addressing
Bit 7	0 : enable NMI interrupt 1 : disable all NMI sources

NMI Status and Control register(Port B):

Port 61h	**(R/W)**
Default value	00h
Bit 0 (R/W)	0 : Timer Counter 2 disable 1 : Timer Counter 2 enable
Bit 1 (R/W)	0 : Pin SPKR output is always '0'. 1 : Pin SPKR output is the Timer Counter 2 OUT signal value.
Bit 2 (R/W)	0 : System board error enable 1 : System board error disable and clear
Bit 3 (R/W)	0 : IOCHKJ NMI enable 1 : IOCHKJ NMI disable and clear
Bit 4 (R only)	Toggled from 0 to 1 or 1 to 0 following every refresh cycle
Bit 5 (R only)	Timer Counter 2 OUT status
Bit 6 (R only)	0 : No NMI Interrupt from IOCHKJ 1 : IOCHKJ is active and NMI requested To reset this interrupt, set bit 3 to 1.
Bit 7 (R only)	0 : No SERRJ from System Board 1 : SERRJ active, NMI requested To reset this interrupt, set bit 2 to 1.

4.6 FAST RC/GATE-A20 Registers.

Port 92h (R/W) Default value : 24h

Bit 0 0 : allow FAST RC to be pulsed
1 : FAST RC is pulsed active

Bit 1 Directly reflects the A20MJ signal
0 : A20MJ is driven inactive (low)
1 : A20MJ is driven active (high)

Bit 2 reserved (must be read as a 1)

Bit 3 reserved (must be read as a 0)

Bit 4 reserved (must be read as a 0)

Bit 5 reserved (must be read as a 1)

Bit 6 reserved (must be read as a 0)

Bit 7 reserved (must be read as a 0)

4.7 ISA Compatible Registers Summary :

The ISA compatible registers of the M1523 are summarized as below :

I/O Address	Attribute	Register Name
0000h	Read/Write	DMA1 (slave) CH0 Base and Current Address
0001h	Read/Write	DMA1 (slave) CH0 Base and Current Count
0002h	Read/Write	DMA1 (slave) CH1 Base and Current Address
0003h	Read/Write	DMA1 (slave) CH1 Base and Current Count
0004h	Read/Write	DMA1 (slave) CH2 Base and Current Address
0005h	Read/Write	DMA1 (slave) CH2 Base and Current Count
0006h	Read/Write	DMA1 (slave) CH3 Base and Current Address
0007h	Read/Write	DMA1 (slave) CH3 Base and Current Count
0008h	Read/Write	DMA1 (slave) Status(R)/Command(W)
0009h	Write-only	DMA1 (slave) Write Request
000Ah	Write-only	DMA1 (slave) Write Single Mask Bit
000Bh	Write-only	DMA1 (slave) Write Mode
000Ch	Write-only	DMA1 (slave) Clear Byte Pointer
000Dh	Write-only	DMA1 (slave) Master Clear
000Eh	Write-only	DMA1 (slave) Clear Mask
000Fh	Read/Write	DMA1 (slave) Read/Write All Mask Register Bits
0020h	Read/Write	INT_1 (master) Control Register
0021h	Read/Write	INT_1 (master) Mask Register
0040h	Read/Write	Timer Counter - Channel 0 Count
0041h	Read/Write	Timer Counter - Channel 1 Count
0042h	Read/Write	Timer Counter - Channel 2 Count
0043h	Read/Write	Timer Counter Command Mode Register
0060h	Read_access	Clear IRQ12 (for PS2), IRQ1 Latched Status
0060h	Read/Write	Keyboard Data Buffer

The ISA compatible registers of M1523 (continued)

I/O Address	Attribute	Register Name
0061h	Read/Write	NMI and Speaker Status and Control
0064h	Read/Write	Keyboard Status(R)/Command(W)
0070h	Write-only	CMOS RAM Address Port and NMI Mask Register
0071h	Read/Write	CMOS Data Register Port
0081h	Read/Write	DMA Channel 2 Page Register
0082h	Read/Write	DMA Channel 3 Page Register
0083h	Read/Write	DMA Channel 1 Page Register
0087h	Read/Write	DMA Channel 0 Page Register
0089h	Read/Write	DMA Channel 6 Page Register
008Ah	Read/Write	DMA Channel 7 Page Register
008Bh	Read/Write	DMA Channel 5 Page Register
008Fh	Read/Write	Refresh Address Register for Address 23 to 17
00A0h	Read/Write	INT_2 (slave) Control Register
00A1h	Read/Write	INT_2 (slave) Mask Register
00C0h	Read/Write	DMA2 (master) CH0 Base and Current Address
00C2h	Read/Write	DMA2 (master) CH0 Base and Current Count
00C4h	Read/Write	DMA2 (master) CH1 Base and Current Address
00C6h	Read/Write	DMA2 (master) CH1 Base and Current Count
00C8h	Read/Write	DMA2 (master) CH2 Base and Current Address
00CAh	Read/Write	DMA2 (master) CH2 Base and Current Count
00CCh	Read/Write	DMA2 (master) CH3 Base and Current Address
00CEh	Read/Write	DMA2 (master) CH3 Base and Current Count
00D0h	Read/Write	DMA2 (master) Status(R)/Command(W)
00D2h	Write-only	DMA2 (master) Write Request
00D4h	Write-only	DMA2 (master) Write Single Mask Bit
00D6h	Write-only	DMA2 (master) Write Mode
00D8h	Write-only	DMA2 (master) Clear Byte Pointer
00DAh	Write-only	DMA2 (master) Master Clear
00DCh	Write-only	DMA2 (master) Clear Mask
00DEh	Read/Write	DMA2 (master) Read/Write All Mask Register Bits
00F0h	Write-only	Coprocessor Error Ignored Register
040Bh	Write only	DMA1 Extended Mode Register
0481h	Read/Write	DMA CH2 High Page Register
0482h	Read/Write	DMA CH3 High Page Register
0483h	Read/Write	DMA CH1 High Page Register
0487h	Read/Write	DMA CH0 High Page Register
0489h	Read/Write	DMA CH6 High Page Register
048Ah	Read/Write	DMA CH7 High Page Register
048Bh	Read/Write	DMA CH5 High Page Register
04D0h	Read/Write	INT_1 (master) Edge/Level Control
04D1h	Read/Write	INT_2 (slave) Edge/Level Control
04D6h	Write only	DMA2 Extended Mode Register

Section 5: Programming Guide

5.1 PMU Programming Guide

EXAMPLE 1: VGA Timer TIME-OUT EVENTS

```
cfg_write(0x56,0x84);       /* Enable SMI and PMU function */
cfg_write(0x66,0x03);       /* Enable VGA monitor MW A,B segment,IOW 3B0-3BF,3C0-3CF*/
cfg_write(0x5F,0x27);       /* Set the time base of the VGA timer as 20 min */
cfg_write(0x59,0x01);       /* Select VGA time-out events for generating SMIJ*/
                            /* SMIJ is asserted when VGA timers time-out */
                            /* ---- Start SMI routine ---- */
cfg_write(0x55,0x01);       /* Assert SMIACTJ internally*/
cfg_write(0x56,00xxx1xxb);/* Deassert SMIJ */
cfg_read(0x5B);             /* To find out the SMI event is caused by which time-out event */
                            /* Assume that it's the VGA time-out in this example */
cfg_read(0x6A);             /* Read the time-out status */
cfg_write(0x55,0x00);       /* Deassert SMIACTJ internally*/
cfg_write(0x59,0x04);       /* Clear VGA time-out event */
cfg_write(0x5A,0x01);       /* Set VGA as a wake-up event since the VGA is in the power
                             saving mode currently */
cfg_write(0x56,0x84);       /* Enable SMI again */
RSM;                        /* End SMI routine */
```

EXAMPLE 2: MODE TRANSLATION

```
                            /* The DOZE, STANDBY, SUSPEND modes are defined by the BIOS */
cfg_write(0x56,0x84);       /* Enable SMI, PMU and set the system state at ON mode */
cfg_write(0x57,0x08);       /* Monitor IRQs in this example */
cfg_write(0x59,0x20);       /* Enable MODE timer */
cfg_write(0x64,0x67);       /* Set the time base of the MODE timer as 60 min */
                            /* SMIJ will be generated if no IRQ is active during 60 min */
                            /* ---- Start SMI routine ---- */
cfg_write(0x55,0x01);       /* Assert SMIACTJ internally*/
cfg_write(0x56,00xxx1xxb);/* Deassert SMIJ */
cfg_read(0x5B);             /* To read the SMI cause */
                            /* It should be the MODE timer time-out in this example */
cfg_read(0x6A);             /* Read the time-out status */
cfg_write(0x55,0x00);       /* Deassert SMIACTJ internally*/
cfg_write(0x59,0x00);       /* Clear MODE time-out event */
cfg_write(0x5A,0x80);       /* Set IN(stardard input) as a wake-up event */
cfg_write(0x56,0x84);       /* Enable SMI again */
RSM;                        /* End SMI routine */
```

EXAMPLE 3: EXTERNAL SWITCH

```
cfg_write(0x56,0x84);       /* Enable SMI and PMU function */
cfg_write(0x67,0x03);       /* Set external switch both low-to-high and high-to-low active */
cfg_write(0x58,0x00);       /* Clear external switch */
cfg_write(0x58,0x40);       /* Enable external switch */
                            /* SMI is generated when external switch is pushed */
                            /* ---- Start SMI routine ---- */
cfg_write(0x55,0x01);       /* Assert SMIACTJ internally*/
cfg_write(0x56,00xxx1xxb);/* Deassert SMIJ */
cfg_read(0x5B);             /* To find out the SMI event is caused by which time-out event */
                            /* It should be the external switch active in this example */
cfg_read(0x67);             /* Check the external switch status */
cfg_write(0x55,0x00);       /* Deassert SMIACTJ internally*/
cfg_write(0x58,0x00);       /* Clear external switch */
cfg_write(0x58,0x40);       /* Enable external switch */
cfg_write(0x5A,0x80);       /* Set the keyboard as a wake-up event */
cfg_write(0x56,0x84);       /* Enable SMI again */
RSM;                        /* End SMI routine */
```

EXAMPLE 4: USAGE OF THE IN GROUP

IN group is used to monitor the activity of the standard input devices.
IN group is defined as:

IRQ1: default for keyboard
IRQ12: optional for PS2 mouse(index_66_D5)
IRQ4: optional for COM1 mouse(index_66_D6)
IRQ3: optional for COM2 mouse(index_66_D7)

IN group timer time-out:

(1) Generate power control signal to turn off the screen
(2) Enter SMM by asserting SMIJ

IN group access:

(1) Generate power control signal to turn on the screen
(2) Enter SMM by asserting SMIJ

Hence, monitoring the IN group activity can be used to implement the function of the "screen saver". Besides, it won't impact the perforamnce of the running program, instead the whole power can be reduced dramatically.

EXAMPLE 5: SOFTWARE SMI EVENT

```
cfg_write(0x56,0xC4);       /* Enable SMI and PMU function, and enable software SMI */
                            /* SMIJ is asserted */
                            /* ---- Start SMI routine ---- */
cfg_write(0x55,0x01);       /* Assert SMIACTJ internally*/
cfg_read(0x5B);             /* Read SMI cause, it should be software SMI */
cfg_write(0x56,00xxx1xxb);/* Deassert SMIJ */
cfg_write(0x55,0x00);       /* Deassert SMIACTJ internally*/
cfg_write(0x56,0x84);       /* Enable SMI again */
RSM;                        /* End SMI routine */
```

5.2 PCI - Interrupt Mapping Programming Guide

Example 1

```
cfg_write (45h,1xxxxxxxb)  /*Enable PCI interrupt polling mode*/
                           /* Program INT-CNTL1 (Master 8259) */
io_write (20h,11h)         /* ICW1,edge trigger,cascade mode,ICW4 needed */
io_write (21h,08h)         /* ICW2,interrupt vector address */
io_write (21h,04h)         /* ICW3,IR2 input is slave */
io_write (21h,01h)         /* ICW4,not SFNM,Normal EOI,80x86 mode */

                           /* Program INT-CNTL2 (Slave 8259) */
io_write (A0h,11h)         /* ICW1,edge trigger,cascade mode,ICW4 needed */
io_write (A1h,70h)         /* ICW2,interrupt vector address */
io_write (A1h,02h)         /* ICW3,INTR is connected to IR2 of INT-CNTL1 */
io_write (A1h,01h)         /* ICW4,not SFNM,Normal EOI,80x86 mode */

                           /* Program Edge/Level Control Register(ELCR) */
io_write (04D0h,18h)       /* IRQ3,IRQ4 of is level trigger,others edge trigger */
io_write (04D1h,00h)       /* All IRQs of INT-CNTL2 are edge trigger*/
                           /* Program PCI Routing Table */
                           /* There are 8 PCI INT channels input to INTAJ_MI, selected by S2-S0 */
cfg_write (48h,01h)        /* Set INT-1 to IRQ3 ,INT-2 disable */
cfg_write (49h,30h)        /* INT-3 disable ,Set INT-4 to IRQ4*/
cfg_write (4Ah,75h)        /* Set INT-5 to IRQ6 ,INT-6 to IRQ5 */
cfg_write (4Bh,00h)        /* INT-7 disable ,INT-8 disable */

                           /* PCI INT to ISA edge transfer */
cfg_write (4Ch,30h)        /* INT-5,6  transfer level to edge trigger */
```

Example 2

```
cfg_write (45h,0xxxxxxxb)  /*Disable PCI interrupt polling mode*/
                           /* Program INT-CNTL1 (Master 8259) */
io_write (20h,11h)         /* ICW1,edge trigger,cascade mode,ICW4 needed */
io_write (21h,08h)         /* ICW2,interrupt vector address */
io_write (21h,04h)         /* ICW3,IR2 input is slave */
io_write (21h,01h)         /* ICW4,not SFNM,Normal EOI,80x86 mode */

                           /* Program INT-CNTL2 (Slave 8259) */
io_write (A0h,11h)         /* ICW1,edge trigger,cascade mode,ICW4 needed */
io_write (A1h,70h)         /* ICW2,interrupt vector address */
io_write (A1h,02h)         /* ICW3,INTR is connected to IR2 of INT-CNTL1 */
io_write (A1h,01h)         /* ICW4,not SFNM,Normal EOI,80x86 mode */

                           /* Program Edge/Level Control Register(ELCR) */
io_write (04D0h,40h)       /* IRQ6 of INT-CNTL1 is level trigger,others edge trigger */
io_write (04D1h,40h)       /* IRQ14 of INT-CNTL2 is level trigger,others edge trigger*/

                           /* Program PCI Routing Table */
                           /* There are only 4 PCI INT channels input to INTAJ,INTBJ,INTCJ,INTDJ */
cfg_write (48h,D7h)        /* Set INTAJ to IRQ6 ,Set INTBJ to IRQ14 */
cfg_write (49h,0Fh)        /* Set INTCJ to IRQ15 ,INTDJ disable */
                           /* PCI INT to ISA edge transfer */
cfg_write (4Bh,04h)        /* INTCJ transfer level to edge trigger */
```

Section 6: Electrical Characteristics

6.1 DC Specifications

Table 6-1. Absolute Maximum Ratings

case temperature under bias	0 °C to 70 °C
storage temperature	-40 °C to 125 °C
voltage on any pin with respect to ground	-0.5 V to 7 V (for 5V pins) -0.5 V to 4 V (for 3V pins)
supply voltage with respect to Vss	-0.5 V to 5.5 V (for 5V pins) -0.5 V to 3.6 V (for 3V pins)

Table 6-2. M1523 DC Specifications

Vcc_5V = 5V ± 5%, Vcc_3V = 3.3V ± 5%, T_{case} = 0 to +70°C					
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Notes**
V_{IL}	input low voltage	-	0.8	V	TTL level
V_{IH}	input high voltage	2.0	-	V	TTL level
V_{OL}	output low voltage	-	0.4	V	TTL level, at 8 mA load
V_{OH}	output high voltage	4.0 2.4	- -	V	TTL level, at 6 mA load (for 5V pins) TTL level, at 6 mA load (for 3V pins)
I_{LI}	input leakage current	-	0.05	µA	$0 \le V_{IN} \le V_{CC}$, for input without pull up and pull down
I_{IL}	input leakage current	-	400	µA	V_{IN} = 0.45V, for input with pull up
I_{IH}	input leakage current	-	50	µA	V_{IN} = 2.40V, for input with pull down
C_{IN}	input capacitance	-	10	pF	f = 1MHz, Vcc=0V, not 100% tested
C_O	output capacitance	-	10	pF	f = 1MHz, Vcc=0V, not 100% tested

6.2 AC Specifications

Table 6-3. PCI bus signals timing list (unit : ns)

Vcc_5V = 5V ± 5%, Vcc_3V = 3.3V ± 5%, T_{case} = 0 to + 70^{o}C, C_L = 0pF

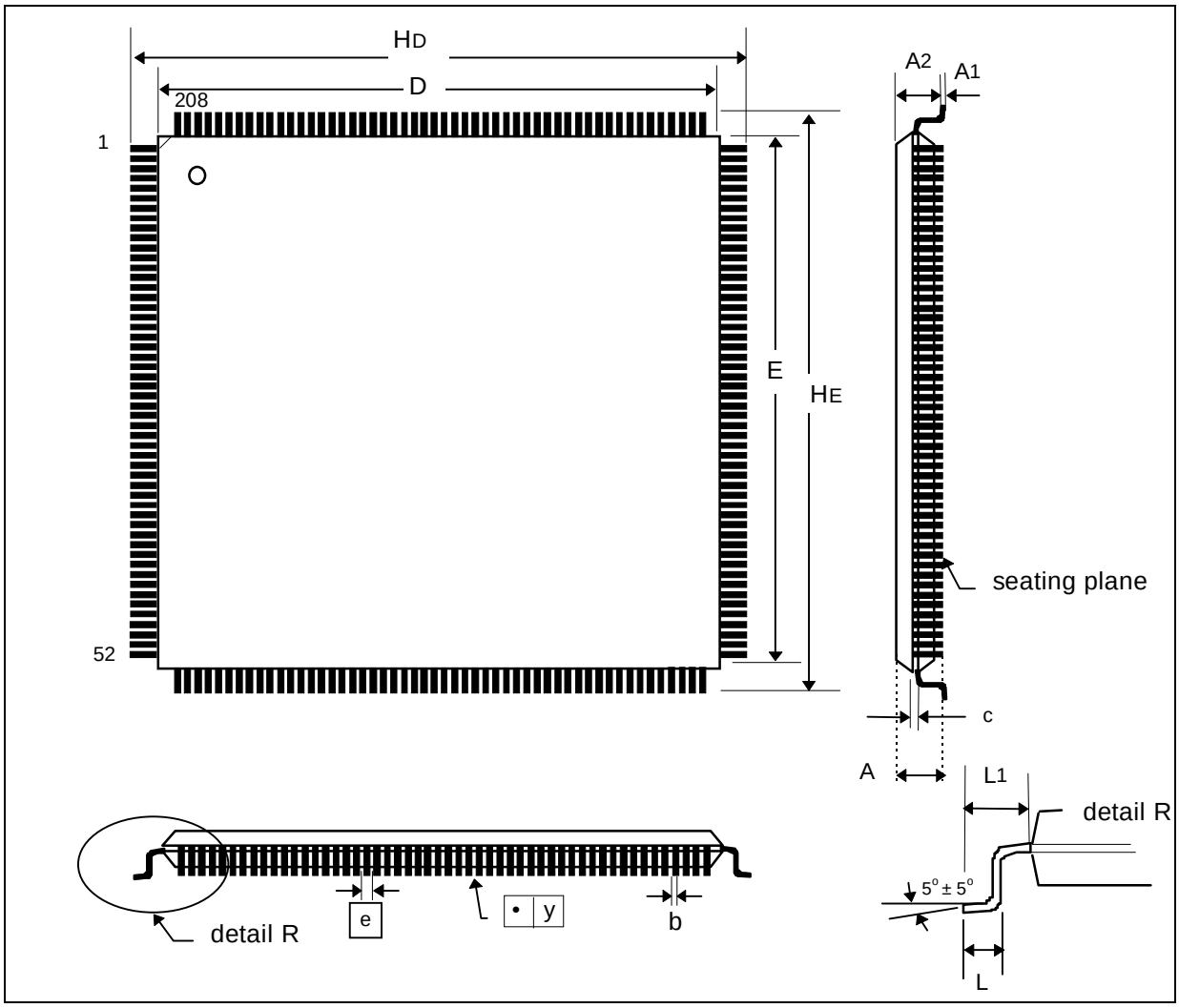
Timing (unit : ns)	Max.	Typical	Min.
Bussed signals :			
DEVSELJ :			
PCICLK to Signal Valid Delay	12.19	---	5.92
PCICLK to Signal Inactive Delay	8.78	---	4.13
TRDYJ :			
PCICLK to Signal Valid Delay	12.24	---	6.10
PCICLK to Signal Inactive Delay	9.14	---	4.31
STOPJ :			
PCICLK to Signal Valid Delay	12.00	---	5.96
PCICLK to Signal Inactive Delay	8.98	---	4.23
FRAMEJ :			
PCICLK to Signal Valid Delay	12.48	---	6.18
PCICLK to Signal Inactive Delay	9.44	---	4.44
IRDYJ :			
PCICLK to Signal Valid Delay	14.56	---	7.08
PCICLK to Signal Inactive Delay	11.04	---	5.22
PCICLK to Signal Float Delay	10.73	---	8.00
Point to point signals :			
PHOLDJ :			
PCICLK to Signal Active Delay	4.84	---	2.52
PCICLK to Signal Inactive Delay	5.01	---	2.54
CPU interface signals :			
SMIJ :			
CPUCLK to Signal Active Delay	9.67	---	---
CPUCLK to Signal Inactive Delay	10.49	---	---
STPCLKJ :			
CPUCLK to Signal Active Delay	8.97	---	---
CPUCLK to Signal Inactive Delay	8.94	---	---

Table 6-4. IDE interface

Vcc_5V = 5V ± 5%, Vcc_3V = 3.3V ± 5%, T_{case} = 0 to + 70^{o}C, C_L = 0pF

IDE interface	Max.(ns)	Typical	Min.(ns)
XIDEIOWJ delay from XPCICLK			
H to L	14.23	--	7.05
L to H	11.82	--	5.24
XIDEIORJ delay from XPCICLK			
H to L	14.71	--	7.29
L to H	12.19	--	5.42
XTRDYJ delay from XPCICLK			
H to L	14.32	--	7.03
L to H	11.18	--	5.26
XIDE_A[2:0] delay from XPCICLK			
H to L	14.54	--	7.20
L to H	14.46	--	7.16
XIDE_D[15:0] write data valid delay	20.20	--	9.88
IDE CYCLE read data valid delay	15.24	--	5.26

Section 7: Packaging Information



Symbol	Dimensions in Millimeters (nom)	Dimensions in Inches (nom.)
A	3.5 (max)	0.137 (max)
A_1	0.2 (min)	0.008 (min)
A_2	3.0	0.118
b	0.18	0.007
c	0.15	0.006
D	28.0	1.102
E	28.0	1.102
e	0.5	0.020
H_D	30.6	1.205
H_E	30.6	1.205
L_1	1.3	0.051
L	0.5	0.020
y	0.15 (max)	0.006 (max)

Feature comparison

Feature Comparison Table					
	TRITON-FX	**TRITON-VX**	**ALADDIN-II**	**ALADDIN-III**	**TRITON-II**
Host-MM Post WR buffer	8DW	16DW	16DW	16DW	16DW
Pipelined CPU bus	Yes	Yes	Yes	Yes	Yes
EDO (50MHz PCLK)	7-2-2-2	5-3-2-2	5-2-2-2	4-2-2-2	4-2-2-2
BEDO	No	No	No	(Yes)	No
SDRAM	No	Yes	No	(Yes)	No
Memory Bank/No UMA	5	4	6	8	8
Memory Bank/UMA	No	4	No	4/6	No
Memory Bank/SDRAM	No	4	No	4	4
UMA Protocol	No	Yes/ Proprietary	No	Yes/ Versatile	No
32-bit Memory Bus	No	No	No	Yes/Flexible	No
Host-PCI Latency	Slow	Slow	Middle	Fast	Fast
Cache Writeback Merge	No	No	No	Yes	---
L2 MESI	Yes	Yes	No	Yes	Yes
EDC	No	No	No	Yes	Yes
EDC/Nibble Mode	No	No	No	Yes	Yes
PCI-DRAM WR FIFO	13DW	18DW	24DW	20DW	20DW
PCI-DRAM RD FIFO	2DW	10DW	8DW	21DW	21DW
Link Bus	16Bits/External	16Bits/External	---	32Bits/Internal	32Bits/Internal
IDE Master Bus	Mux Bus	Mux Bus	Mux Bus	Dedicated Bus	---
Chip Count	4	4	4	2	2
Architecture/Concurrent/BW	Good	Good	Good	Excellent	Excellent

This material is recyclable.