Winter 1996

AMCC

Precision Clocking Products Data Book

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For Marketing and Application Information Contact:

Applied Micro Circuits Corporation
6195 Lusk Blvd.
San Diego, CA 92121-2793
(619) 450-9333
(800) 755-2622
Fax (619) 450-9885
http://www.amcc.com

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PRODUCT SELECTION GUIDES

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5V Supply-TTL I/O Clock Driver Products

	Output Frequency with Respect to Input Frequency					
P/N	Total Outputs	Number of Outputs ÷ 1	Number of Outputs ÷ 2	Number of Outputs ÷ 2 or 4	Special Features	Package
SC3500	20	10	5 ÷ 1 or 2	5	—	52 PQFP
SC3506	20	10	10	N/A	—	52 PQFP
SC3507	20	10	N/A	10	—	52 PQFP
SC3508	20	20	N/A	N/A	—	52 PQFP
SC3517	10	5	N/A	5	—	28 SOIC
SC3518	10	10	N/A	N/A	—	28 SOIC
SC3526	9	5	4	N/A	Sync Output	28 SOIC
SC3527	10	3	7	N/A	Selectable single or dual clock input.	28 SOIC
SC3528	10	10	N/A	N/A	—	28 SOIC
SC3529	10	10	N/A	N/A	Power Down	28 SOIC

5V Supply-LVTTL I/O Clock Driver Products

	Output Frequency with Respect to Input Frequency				
P/N	Total Outputs	Number of Outputs ÷ 1	Number of Outputs ÷ 2	Special Features	Package
SC3306	20	10	10		52 PQFP
SC3308	20	20	N/A		52 PQFP
SC3318	10	10	N/A		28 SOIC
SC3327	10	3	7	Selectable single or dual clock input.	28 SOIC
SC3367	14	7	7	Selectable single or dual clock input, 1 output early.	28 SOIC
SC3368	14	6	8	Selectable single or dual clock input.	28 SOIC

3.3V Supply-LVTTL I/O Clock Driver Products

	Output Frequency with Respect to Input Frequency				
P/N	Total Outputs	Number of Outputs ÷ 1	Number of Outputs ÷ 2	Special Features	Package
S3LV306	20	10	10		52 PQFP
S3LV308	20	20	N/A		52 PQFP
S3LV318	10	10	N/A		28 SOIC
S3LV368	14	6	8	Selectable single or dual clock input.	28 SOIC

5V/3.3V Clock Generator and Synthesizer Products

	Output Frequency Group with Respect to Input Frequency						
P/N	Description	Input Reference	Number	Type	Max. Freq.	Min. Delay Adjust Increment	Number of Selectable Output Relationships
S4402	Multiphase Clk Generator	TTL	6	TTL	80	3.2 ns	21
S4403	Multiphase Clk Generator	TTL	10	TTL	80	3.2 ns	21
S4405	Multiphase Clk Generator with PECL I/O	PECL/TTL	6 1	TTL PECL	80 160	3.2 ns —	21 —
S4406	Clock Generator with Delay Adj. & Invert	TTL	12	TTL	66	4 ns @ 66 MHz	7 x 4 Banks of 3 Outputs
S4501	Clock Multiplier	TTL	2	TTL	100	N/A	3
S4503	Clock Synthesizer	XTAL	2 1	TTL PECL	80 300	N/A	Multiply 2-32 Divide 2-16
S4505S	RAMBUS™ Compatible Clock Generator	XTAL	2	RAMBUS Compatible	270	N/A	1
S4LV406	3.3V Clock Generator	TTL	12	LVTTL	80	1.25 ns	7 x 4 Banks of 3 Outputs

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ATM and 100VG AnyLAN Interface Products

Product	Function	Operating Speed	Data Path	Package	Power Supply
S3011	SONET/ATM/ E-4 Tx	139/155 Mbit/s	8:1 bit	80 TEP	+5.0V
S3012	SONET/ATM/ E-4 Rx	139/155 Mbit/s	1:8 bit	80 TEP	+5.0V
S3020	ATM Tx	622 Mbit/s	8:1 bit	52 TEP	+5.0V
S3021	ATM Rx	622 Mbit/s	1:8 bit	52 TEP	+5.0V
S2100	100VG AnyLAN Transceiver	120 Mbit/s	4:1/1:4 bit	52 PQFP	+5.0V

See Network Interface Products data book.

Fibre Channel Products

Product	Function	Operating Speed	Data Path	Package	Power Supply
S2036	Open Fiber Control	266/531/1062 Mbit/s	N/A	28 SOIC	+5V
S2042	Fibre Channel Transmitter	266/531/1062 Mbit/s	10:1/20:1 bit	44 PQFP 52 TQFP	+3.3V
S2043	Fibre Channel Receiver	266/531/1062 Mbit/s	1:10/1:20 bit	44 PQFP 52 TQFP	+3.3V
S2044	GLM Compliant Fibre Channel Transmitter	266/531/1062 Mbit/s	10:1/20:1 bit	52 TQFP	+3.3V
S2045	GLM Compliant Fibre Channel Receiver	266/531/1062 Mbit/s	1:10/1:20 bit	52 TQFP	+3.3V
S2052	Fibre Channel Transceiver	266/531/1062 Mbit/s	10:1/1:10 bit	52 PQFP	+3.3V
S2060	8B/10B Encoder/Decoder	266/531/1062 Mbit/s	10 or 20 bit	120 PQFP	+3.3V

See Network Interface Products data book.

HIPPI Products

Product	Function	Operating Speed	Data Path	Package	Power Supply
S2020	HIPPI Source	800 Mbit/s	32 bit	225 PGA/ 208 TEP	-5.2/+5V
S2021	HIPPI Destination	800 Mbit/s	32 bit	225 PGA/ 208 TEP	-5.2/+5V

See Network Interface Products data book.

PCI Bus Products

Product	Function	Description
S5933	PCI Controller	32-Bit Add-on Bus

See S5933 PCI Controller data book.

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SONET/SDH Products

Product	Function	Operating Speed	Data Path	Package	Power Supply
S3005	SONET/E-4 Tx	139/155/622 Mbit/s	8:1 bit	68 LDCC 80 TEP	-4.5/5.0V
S3006	SONET/E-4 Rx	139/155/622 Mbit/s	1:8 bit	68 LDCC 80 TEP	-4.5/5.0V
S3014	CSU/CRU	155/622 Mbit/s	1 bit	44 PLCC	-5.2/+5.0V
S3015	E4/OC-3/STM-1 Interface Tx	139/155 Mbit/s	1 bit	52 TEP	+5V
S3016	E4/OC-3/STM-1 Interface Rx	139/155 Mbit/s	1 bit	52 TEP	+5V
S3017	SONET/SDH Tx	622 Mbit/s	8:1 bit	52 TEP	+5V
S3018	SONET/SDH Rx	622 Mbit/s	8:1 bit	52 TEP	+5V
S3019	SONET/SDH /ATM Transceiver	155/622 Mbit/s	1:8/8:1 bit	52 PQFP	+3.3V
S3022	SONET STPC	155/622 Mbit/s	1:8/8:1 bit	120 TEP	+5V
S3025	SONET/SDH CRU	155/622 Mbit/s	1 bit	16 PLCC	+5V

See Network Interface Products data book.

Crosspoint Switch Products

Product	Function	Operating Speed	Data Path	Package	Power Supply
S2016	Crosspoint Switch	1.5 Gbit/s	16 x16	120 TEP	+5V
S2024	Crosspoint Switch	600/800 Mbit/s	32x32	196 LDCC	-5.2/+5V
S2025	Crosspoint Switch	1.5 Gbit/s	32x32	196 LDCC	+5V

See Network Interface Products data book.

ASIC Products

Part Number	Technology	Equivalent Gates (Full Adder Method)	Number of I/O	Structured Array Blocks
Q20004	1 Micron Bipolar	671	28	None
Q20010	1 Micron Bipolar	1469	66	None
Q20025	1 Micron Bipolar	4032	100	None
Q20045	1 Micron Bipolar	6782	128	None
Q20080	1 Micron Bipolar	11242	162	None
Q20120	1 Micron Bipolar	18777	198	None
Q20P010	1 Micron Bipolar	928	34	1 GHz PLL
Q20P025	1 Micron Bipolar	3120	51	1 GHz PLL
Q20M100	1 Micron Bipolar	13475	195	RAM

See Network Interface Products data book.

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CORPORATE SUMMARY

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COMPANY OVERVIEW

AMCC defines, develops, manufactures and markets application specific standard products (ASSPs) and application specific integrated circuits (ASICs) for high speed, high performance network interface applications. Utilizing CMOS, BiCMOS and proprietary MicroPower Bipolar technology, AMCC provides precision clocking devices and interface solutions for PCI, ATM, SONET, and Fibre Channel standards.

Since 1979, AMCC has designed and produced five generations of semicustom bipolar ECL logic arrays and two generations of BiCMOS logic arrays. AMCC ASIC expertise includes its mixed ECL/TTL interface, phase-locked loop (PLL), precision vernier, skew control, high-speed VCO and controlled edge rate output.

AMCC Product Development Strategy

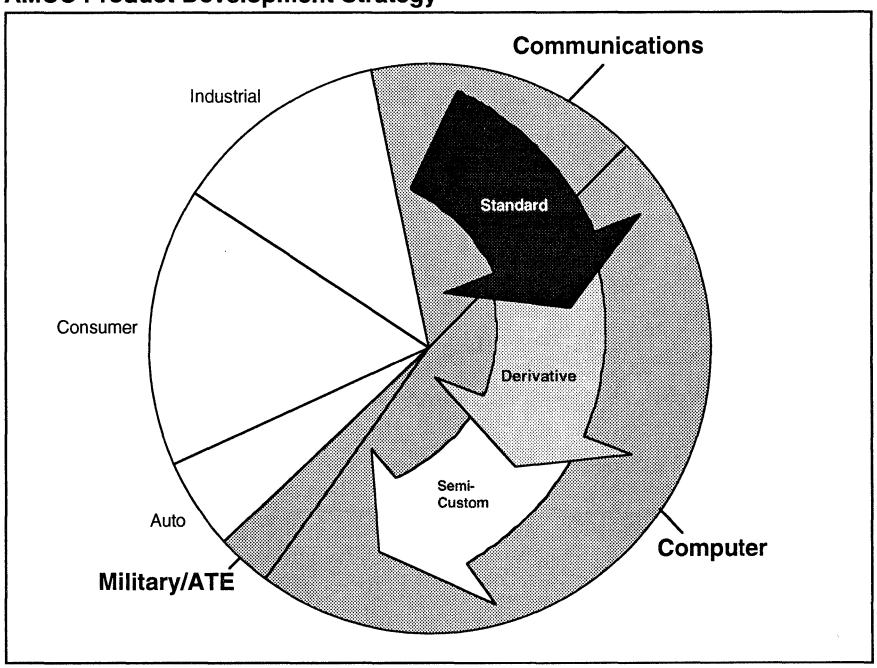
AMCC's product development strategy utilizes the company's expertise in the computer, communications, ATE and military markets. Initially ASSPs are defined based on key industry standards. Then, as additional applications are identified, derivative products based on the "cores" of the original devices are introduced. The "cores" are then also made available for high volume proprietary ASIC designs.

Network Interface Products

High performance network interface encompasses a wide range of applications, all requiring data transmission rates from >100 Mbit per second to over 1 Gbit per second, and beyond. These applications include computer data transmission, fiber-optic telecommunications transmission systems, digital video broadcasting and many more.

AMCC interface circuits, transmitter/receiver chip sets and switches are designed to implement emerging network technologies such as the ANSI or ITU approved Asynchronous Transfer Mode (ATM), Synchronous Optical Network (SONET), Fibre Channel, and High Performance Parallel Interface (HIPPI) telecommunications standards. Jitter, speed, power and size are critical design issues of these technologies. AMCC's devices are based on its unique bipolar process which has superior noise isolation characteristics that significantly reduce jitter. The inherent physical structure of the company's process makes 1 to 3 GigaHertz (GHz) data rates possible at relatively low power. The low device power consumption of AMCC's products helps to minimize the cost and size of packaging.

AMCC Product Development Strategy



Peripheral Component Interconnect (PCI) Bus Controllers

Increased bandwidth available on high speed networks creates a bottleneck at the desktop. One of the causes of this problem is the latency associated with connection to high speed peripheral equipment, including LANs and WANs. The 132 Megabyte per second backplane PCI bus breaks the bottleneck.

AMCC has developed the industry's first line of general purpose master/slave controllers for the PCI bus. These circuits provide a high performance single-chip interface for add-on boards and adapter cards.

Precision Clock and Timing Products

AMCC provides a growing line of precision clock and timing standard products for exacting system designs. AMCC has also tailored clock and timing devices to specific customer needs for high performance clock generation and distribution, clock synchronization and de-skewing, frequency synthesis, and pulse shaping applications. Offerings include low EMI, low skew clock drivers and low jitter clock generators for high performance server and workstation applications.

Strategic Partnerships

AMCC manufactures its own 1.0 micron BiCMOS and Bipolar wafers using proven processes. The Company follows a "semi-fabbed" manufacturing strategy and has reciprocal foundry relationships in place with major domestic and international semiconductor partners that provide for significant additional production capacity. Wafer purchases from strategic foundry partners both expand capacity and provide alternate sources. Additional high-volume assembly and test facilities are located offshore.

AMCC's "quick turn, semi-fabbed" manufacturing approach blends together the strengths of both the "fabbed" and "fabless" semiconductor strategies. Fabbed advantages include the security of total in-house control and time to market. Fabless advantages include multiple sourcing and allows the company to focus investment on new high performance products.

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AMCC COMMITMENT TO QUALITY

Quality is the degree to which a product meets a customer's expectations with regard to delivery time, cost, and performance to the requirements of the application.

Reliability is "...the probability of a product performing, without failure, a specified function under given conditions for a specified period of time."[1]

AMCC is committed to achieving the highest quality and reliability level in the integrated circuit products we provide. Every year for over a decade we have established industry-leading reliability and outgoing quality targets and then beat them.

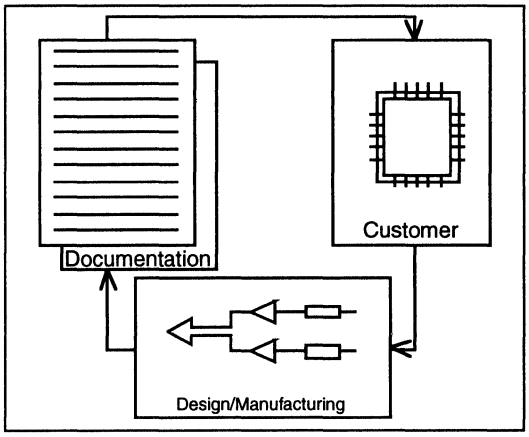
The quality and reliability philosophy at AMCC starts with the premise that for AMCC to continue to excel in the ever expanding market place, the quality expectations of customers must be met or exceeded.

Our team operating philosophy is to:

1) design in manufacturability and reliability during the new product development phase (plan);
2) build in quality at all manufacturing steps (do);
3) execute thorough product inspections, internal audits and reliability confirmation (check);
4) incorporate feedback from internal and external sources into continuous quality improvement programs (act).

Reliability and Manufacturability—Designed In From The Start

Reliability and manufacturability is designed in up front through a team infrastructure which focuses on active participation by Design, Manufacturing and Reliability Engineering throughout all phases of the design process. This includes extensive design verification through computer modeling and design validation by product characterization and application simulation. Final team design review and production readiness approval is required prior to release of products to production.



QA gates and subsequent feedback ensures quality confirmation of AMCC's final product in a continuous improvement program.

Quality Built In During Wafer Fabrication and Manufacturing

AMCC's manufacturing and quality teams employ documented operating procedures, work instructions, in-process inspections and SPC methodology to provide assurance of continued process control and compliance to specification.

Inspection, Audit and Reliability Confirmation

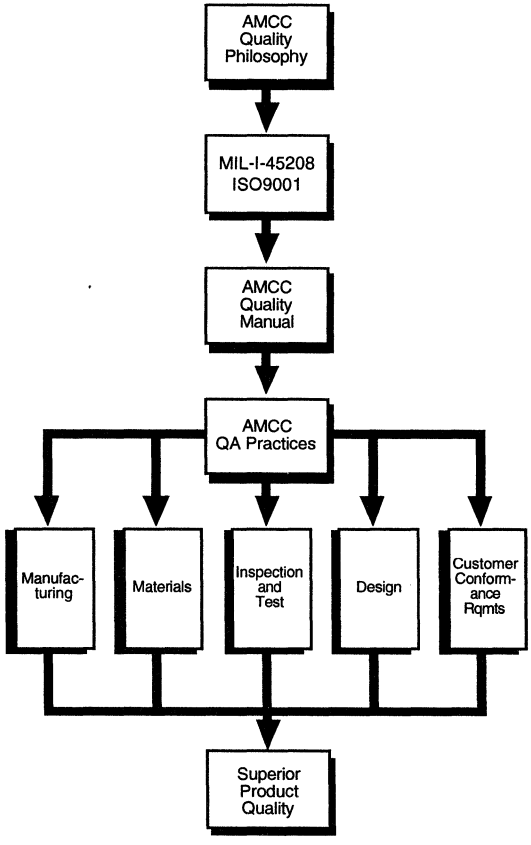
AMCC has strategically placed In-Process Quality Control (IPQC) gates, internal process/area audits and lot/time specific reliability monitors to verify performance against customer requirements and internal design/manufacturing process capabilities. Metrics generated by these activities are intended to provide continuous improvement feedback data for review and action as driven by senior management.

- Die visual and precap gate
- Final outgoing inspection gate
- Modified MIL-STD-105D sampling program
- Lot specific group A and B testing
- Ongoing reliability monitors
- SPC/Data metric review of key subcontractors
- Visual/mechanical and electrical outgoing indices and PPM goals
- Cost-of-quality pareto analysis

[1] JURAN

Continuous Quality Improvement Program

- Corporate-wide commitment driven by the Executive Staff
- A program plan that is flexible enough to comprehend dynamic customer inputs
- Statistical tools in place for analysis and action planning
- Weekly and monthly review meetings to share performance data
- Self examination consistent with elements in ISO9001 and the *Malcolm Baldridge National Quality Award*



AMCC QUALITY SYSTEM

The Quality System had been modeled after the stringent military requirements of MIL-I-45208, MIL-Q-9858 and MIL-I-38535 Appendix A. Heading into the 21st century, AMCC is now modifying its Quality System to also align with ISO9001. This will strengthen the closed loop improvement cycle by tying internal audits with corrective/preventative action though continuous management review.

AMCC's Quality System has the following components integrated throughout the factory to meet or exceed the above requirements.

- Quality Organization
- Quality Planning
- Management Review
- Contract Review
- Design Control
- Document and Data Control
- Purchasing
- Supplier Selection and Control
- Control of Customer Supplied Materials
- Product Identification and Traceability
- Operating Procedures
- Work Instructions
- Inspection and Test
- Inspection, Measurement and Test Equipment Calibration
- Inspection Status System
- Control of Nonconforming Material
- Corrective and Preventive Action
- ESD Safe Handling, Storage, Packaging, Preservation and Delivery Methods
- Records Retention and Maintenance
- Internal Process/Area Auditing System
- Training/Certification
- SPC and Statistical Techniques
- Failure Analysis

ISO9001 REGISTRATION

Based on the restructure of the Quality System to ISO9001 requirements and successful completion of internal and third-party audits, AMCC plans to be ISO registered by June of 1996. Please contact the factory for further details and schedule updates.

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PRODUCT QUALIFICATIONS

A qualification is a sequence of tests in which all parameters, including the reliability of the device are tested. It is this sequence of tests which **initially qualifies** the part to be released for production.

Thorough reliability testing is performed on new product and package families in order to ensure the expectations of our customers are met. These tests include environmental, mechanical and life testing performed in accordance with Military Standards, industrial accepted methods and AMCC Test Procedures. Contact the factory for specific details regarding your selected product/package combination.

AMCC provides MIL-STD-883 Methods 5005, 5008, and 5010 testing for our military customers on contract.

MIL-STD-883 Method 5005

"Qualification And Quality Conformance Procedures"

Method 5005 establishes qualification and quality-conformance inspection procedures for semiconductors to ensure that the quality of devices and lot conform with the requirements of the applicable procurement document. The full requirements of Group A, B, C, D, and E test and inspections are intended for use in initial device qualification—or requalification in the event of product or process change—and in periodic testing for retaining qualification.

Group A consists of electrical tests performed on an inspection lot which has already passed the 100% screening requirements. After a lot has passed the 100% screen tests, a random sample of parts is selected from the total population of devices to form the inspection lot. The inspection lot is then subjected to these Group A electrical tests.

Group B inspection tests are used to monitor the fabrication and assembly processes performed on each inspection lot.

Group C consists of a 1000-hour life test conducted to verify die integrity.

Group D verifies the material integrity and the reliability of the package.

Group E demonstrates the radiation hardness capability of the device. Performed on a generic basis by device type or as required for an application.

MIL-STD-883 Method 5010

"Test Procedures For Custom Monolithic Microcircuits"

This method establishes screening and quality conformance procedures for the testing of custom and semicustom monolithic semiconductors to verify Class B or Class S quality and reliability levels. Testing is performed in conjunction with other documentation such as MIL-I-38535 and an applicable detail specification. It establishes the design, material, performance, control, and documentation requirements needed to achieve prescribed levels of device quality and reliability. AMCC can support qualification using this method.

Until August of 1983, the qualification most commonly used was Method 5005. Since that time, the newer revision of MIL-STD-883 includes Method 5010, which is better suited for semicustom devices (logic arrays included). Either qualification is adequate, but it is desirable to use the 5010 qualification procedure in qualifying custom or semicustom devices.

Qualification Method 5005 VS. 5010

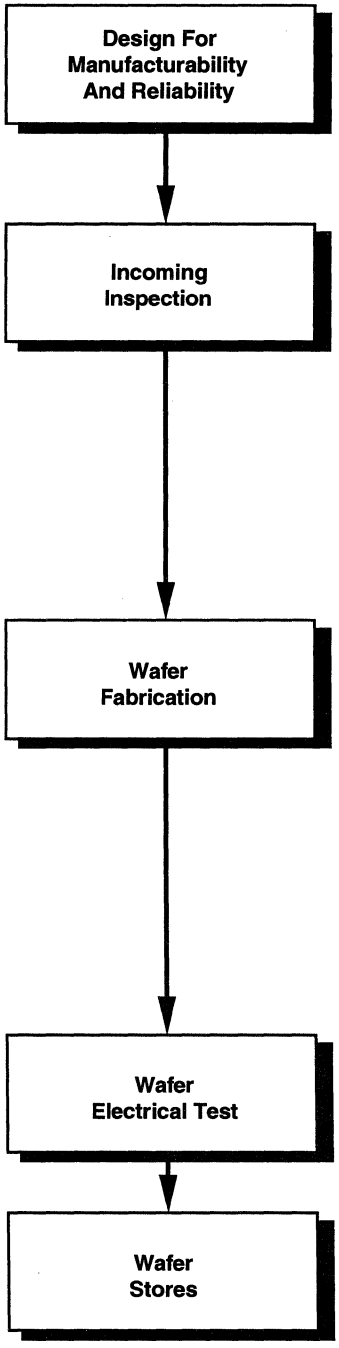
The primary difference between the two methods is in the Group D test. Method 5005 uses electrically-good devices, where method 5010 uses electrical rejects and package-only parts for environmental tests. In addition, Method 5010 is designed for smaller production releases (i.e., 2000 devices/year) while Method 5005 is designed for large production releases.

Generic Data

Under the provision of MIL-I-38535, a customer can elect to qualify using generic data (similar device/family). However, the provisions of the applicable contract should be reviewed. In most cases generic data will satisfy full qualification requirements.

Since many of the qualifications at AMCC are ongoing, generic data may be available for this purpose.

AMCC Product Assurance
Product Flow Detail



- Component Selection
  - Definition — Specification
  - Supplier: Selection — Qualification — Approval
  - Qualified Vendors List (QVL)

- Acceptance Documents and Operating Procedures
  - Purchase Order
  - Component/Material Specifications
  - Product Assurance and General Procedures
  - QVL
  - Sample Inspection of All Direct Materials

- Class 10 Clean Room — FED-STD-209
- Measurements in Adherence with MIL-STD-977
- SPC:
  - In-process Monitors
  - PCM Electricals
- SEM Inspection on All Military Lots
- QA Audits
  - CV Plots — Weekly (minimum)
  - DI Water — Weekly
    - Particle Counts
    - Bacteria Count
  - Airborne Particle Count — Weekly

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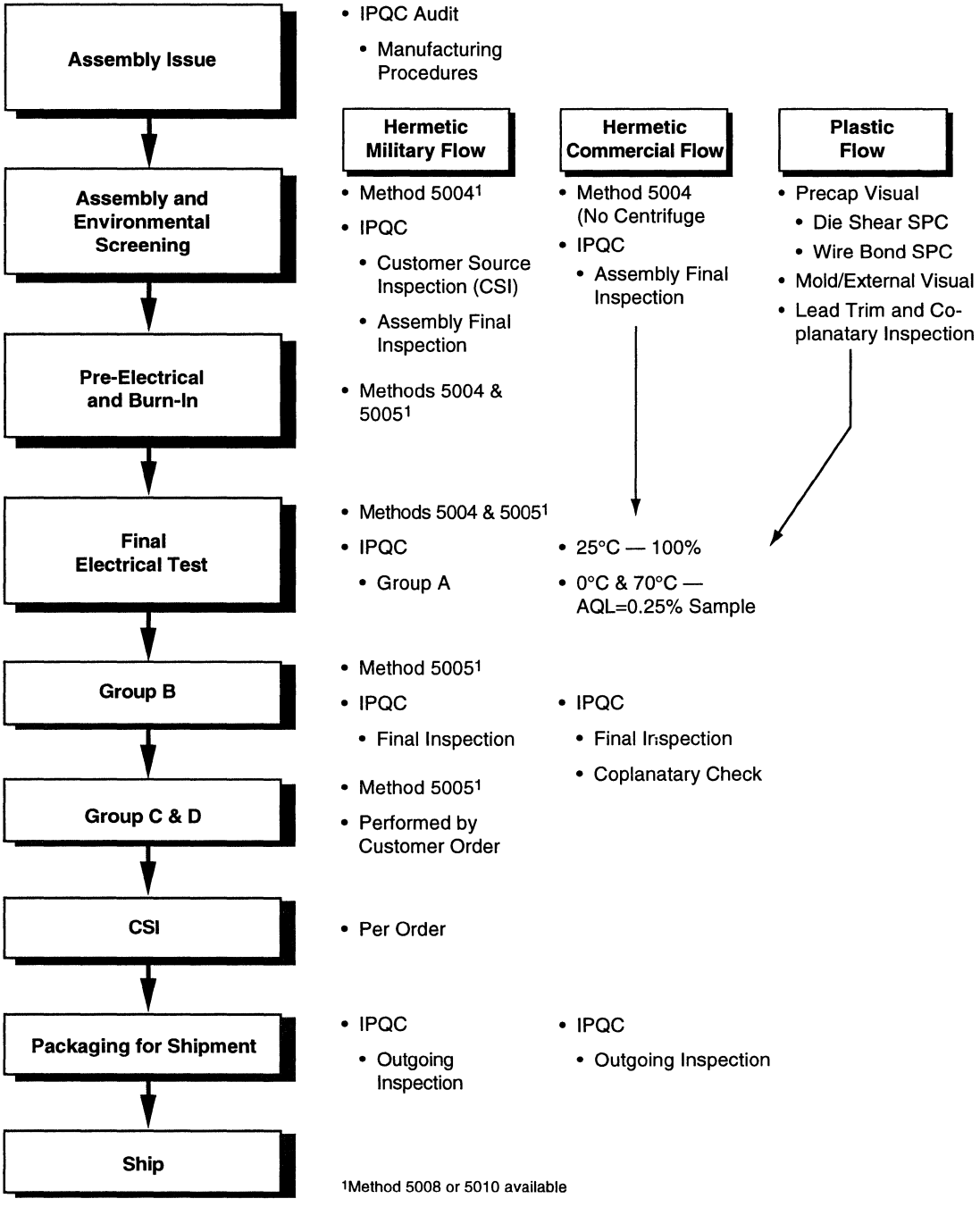
AMCC Product Assurance Product Flow Detail



[1]Method 5008 or 5010 available

AMCC'S RELIABILITY VIGIL

AMCC's internal reliability vigil consists of three phases:

- New/changed processes and material qualifications
- In-process Quality monitors
- Periodic operating life and environmental testing

New/Changed Wafer Processes and Material Qualifications

In order to initially release a device to production a standard set of MIL-STD-883 tests must be completed successfully. These tests include:

Wafer Process and Design

- Operating Life Method 1005
- ESD Characterization Method 3015
- Wire Bond Pull Method 2011
- Thermal Shock or Method 1011 or 1010 Temperature Cycling

Package and Related Materials

- Selected Subgroups of MIL-STD-883, Method 5005, Group B and D

AMCC adheres to MIL-I-38535 with regards to changes.

If changes to production released devices are determined to be major, the appropriate qualification testing must be successfully completed prior to change approval.

In-Process Quality Monitors

- CV plots
- Airborne particle count
- Bacteria, particle count, and resistivity on DI water
- ESD work stations and procedures
- In-line testing of process gases
- Temperature and humidity control
- SPC in wafer fabrication
- SEM of all military lots

Periodic Operating Life and Environmental Testing

- Performed on a product from each process family quarterly.
- 1000 hour operating life test (minimum), Method 5005, Group C.
- Temperature cycling per Method 1010, 100 cycles, condition C: –65°C/150°C
- Environmental testing per AMCC standard test procedures. Consult factory for further details.

Final Measure and Assurance of Quality

The cost of defects depends on when the failure occurs. For example, costs rise significantly as undetected defective ICs are integrated into systems. High quality parts cut costs substantially, and the extra quality built into every AMCC device means added value to our customers.

To achieve maximum quality, AMCC employs 100% testing of all devices, followed by stringent QA sampling.

AMCC performs QA sampling measurements at full specification temperature, both DC and AC, to achieve the tightest AQLs in the industry.

RADIATION HARDNESS

High energy radiation can cause structural changes in the silicon and silicon dioxide crystal lattice by displacing atoms from their normal crystal sites. These changes can be responsible for increased junction leakage, degraded transistor current gain (b), and increased parasitic Si/SiO2 interface leakage currents. The damage is generally induced by neutrons, X-rays, and gamma rays. The effects of the damage induced by this radiation can change both AC and DC parameters, affect functional performance, and, in severe cases, destroy the device.

Certain of AMCC's high performance products are inherently radiation resistant. The radiation resistance of AMCC IC's is the result of the small geometries, the structure of the fabrication process itself, and the use of ECL logic within the device. Contact your AMCC representative regarding radiation resistance characteristics associated with a specific product.

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5V CLOCK DRIVERS

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6195 Lusk Blvd., San Diego, CA 92121 • (619) 450-9333

The design of high speed TTL/CMOS systems is often made more challenging and more difficult than their ECL and GaAs counterparts due to the poor transmission line behavior of the TTL device inputs. Since inputs from either TTL or CMOS devices provide essentially no termination to a given signal path (transmission line), reflections at the end of the line are a certainty. Nowhere in a system is this more noticeable and disastrous than when it occurs on the system's clock. It is here that the wrong choice for the clock driver can cripple the chance for success of a design.

There are many contradictions imposed on the "ideal" TTL clock driver. For example, slower edge rates reduce undershoot, ringing and plateau effects at the expense of duty cycle, frequency and clock skew; while faster edge rates cause overshoot, noise injection, and greater EMI radiation while trying to improve frequency, duty cycle and clock skew.

AMCC has solved this dilemma with an output driver circuit that is best described as having two modes for controlling the clock edges. This patented method produces a fast, crisp edge during the transition phase of the output waveform and then immediately slows the edge and becomes a closer match to the impedance of the external PC board. Figure 1 shows the representative effect of the "dual slope" on the falling edge of the clock. The output driver circuit actually uses the reflected wave to determine the appropriate inflection point for the slope and virtually eliminates "ground bounce".

Figure 1. "Dual Sloped" Output Driver Eliminates "Ground Bounce"

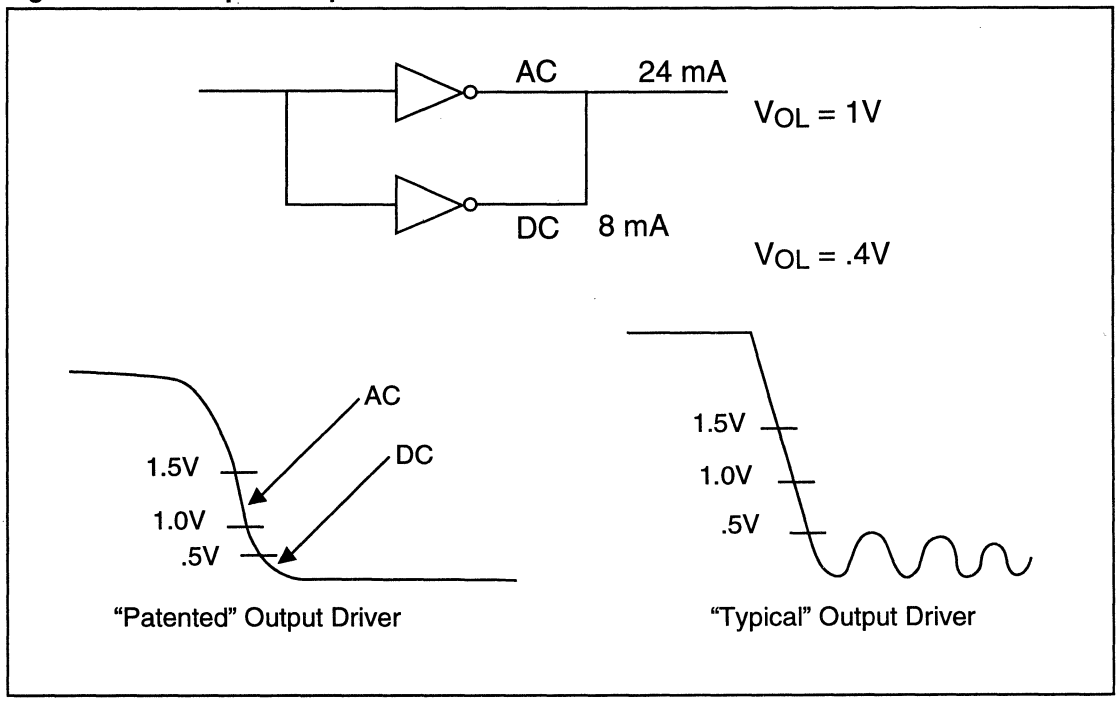


Figure 2 shows the representative effect of dynamically adjusting source series termination on the rising edge. By adjusting the built-in termination to individual loading environments, AMCC's clock drivers prevent "ringing" without the use of any additional onboard termination.

Figure 3 shows an unterminated 66MHz output of an SC35XX Series Driver. Conventional TTL output stages, with or without serial termination resistors, cannot attain both the **edge rates** *and* the **impedance matching** qualities achieved with the AMCC method.

Figure 2. Built-in, On-Chip Source (Series) Termination Minimizes "Overshoot"

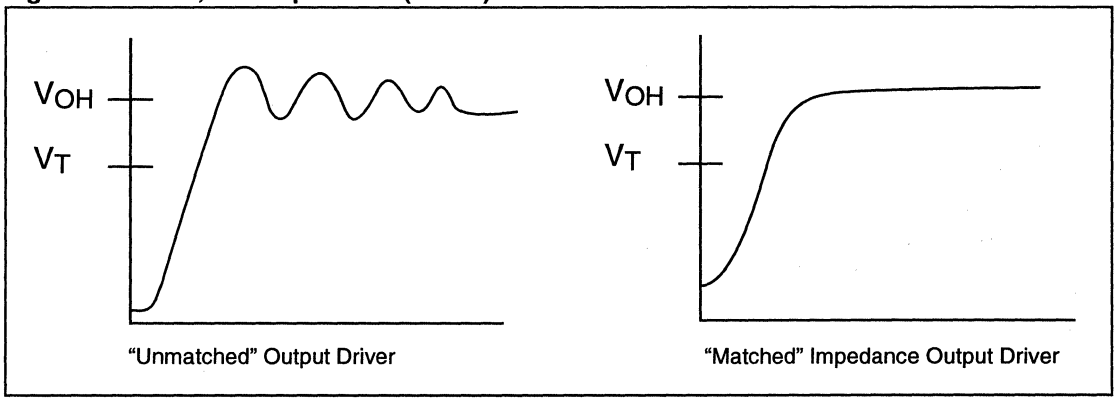
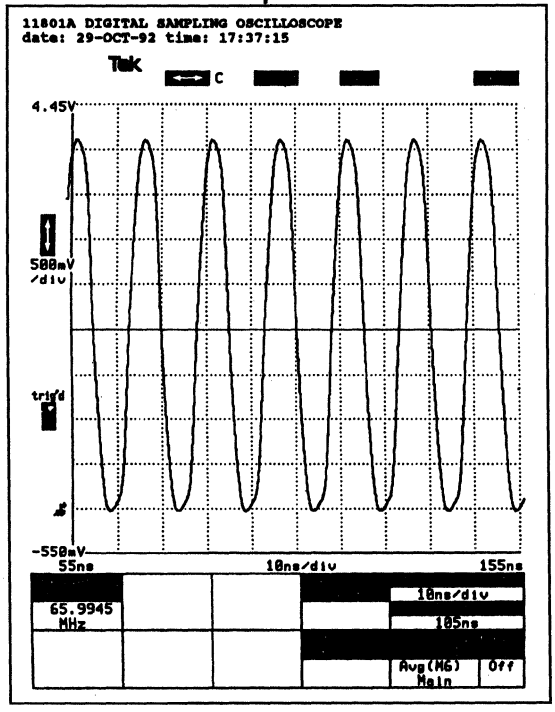


Figure 3.
SC35XX Driver with 20pF Load and 8" of Trace



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20-OUTPUT CLOCK DRIVERS

FEATURES

- **20 clock outputs:**
  - Grouped into banks of 5 or 10 outputs
  - Output frequency of each bank is user selectable
- **Leading edge skew for all outputs ≤0.5 ns**
- **Proprietary output drivers with:**
  - Complementary 24 mA peak outputs, source and sink
  - 50-75Ω source series termination
  - Dynamic drive adjustment to match load conditions
  - Edge rates less than 1.5 ns
- **Minimizes the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**
- **52-pin PQFP package**

APPLICATIONS

- **Compatible with Intel's Pentium™ processor**
- **Compatible with PowerPC™ processors**
- **PCI Bus clock distribution**
- **Workstation and server systems with high clock fanout**
- **Datacom and Telecom networks**

GENERAL DESCRIPTION

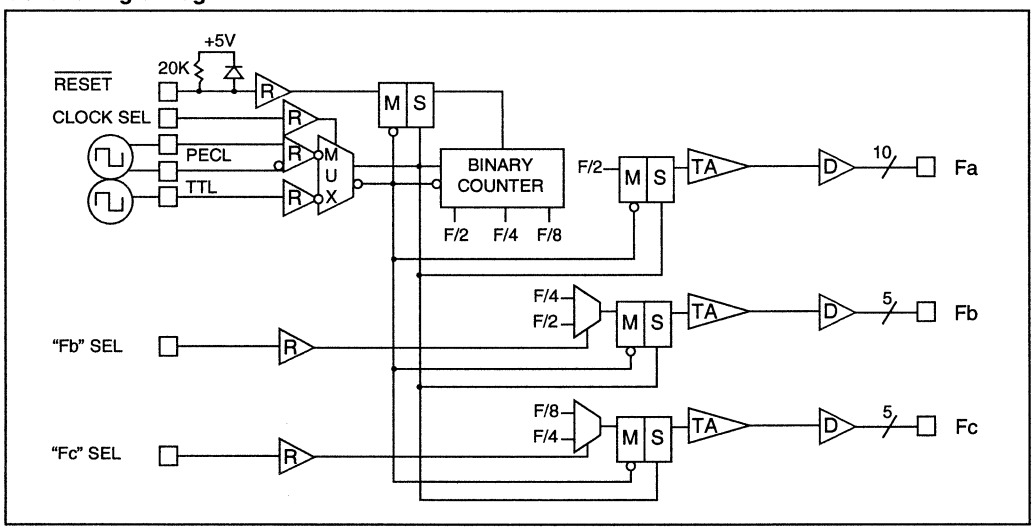
The SC3500, SC3506, SC3507, and SC3508 are precision clock fan out drivers. They accept a reference dock input from either a single-ended TTL source or a differential PECL frequency source. This reference clock input is distributed through dividers and buffers to the output clock drivers.

The 20 outputs are divided into groups of 5 or 10 outputs. The output frequency of each group can be F, F/2, F/4, or F/8, and is user selectable. Each of the clock driver products offers different combinations of divide ratios.

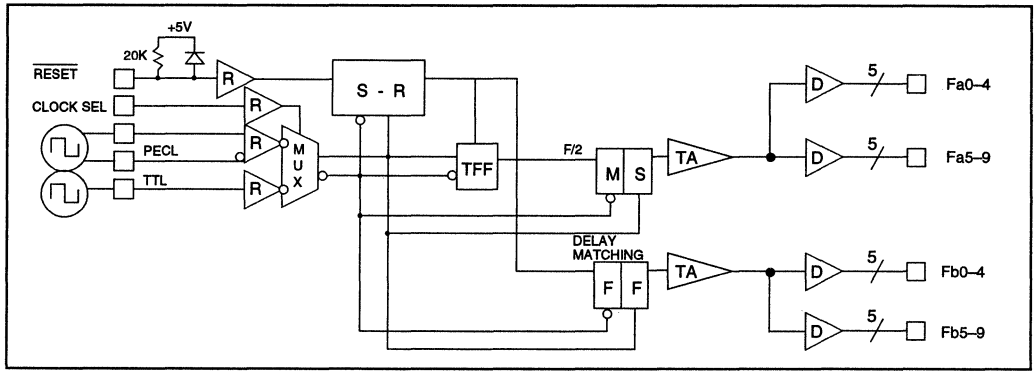
Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of ≈1.5V/ns to minimize simultaneous output switching noise and distortion.

3

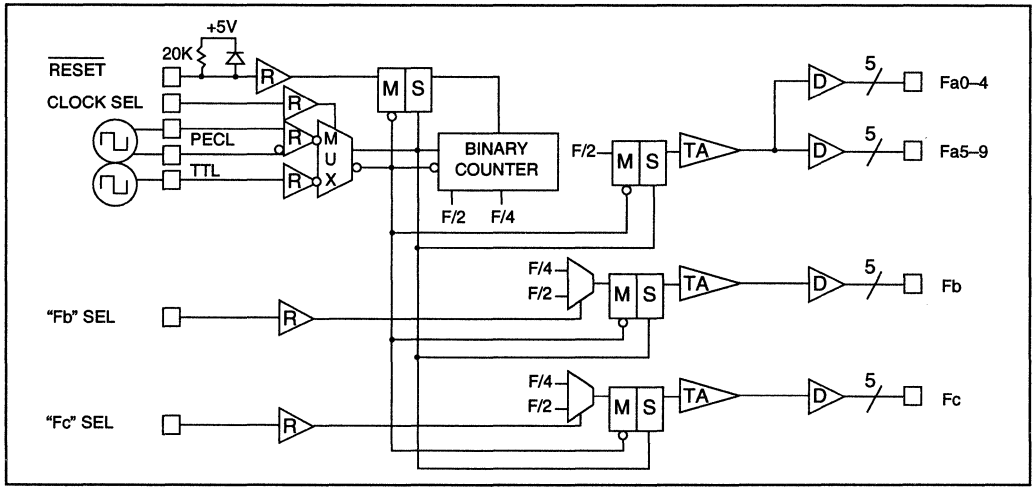
SC3500 Logic Diagram



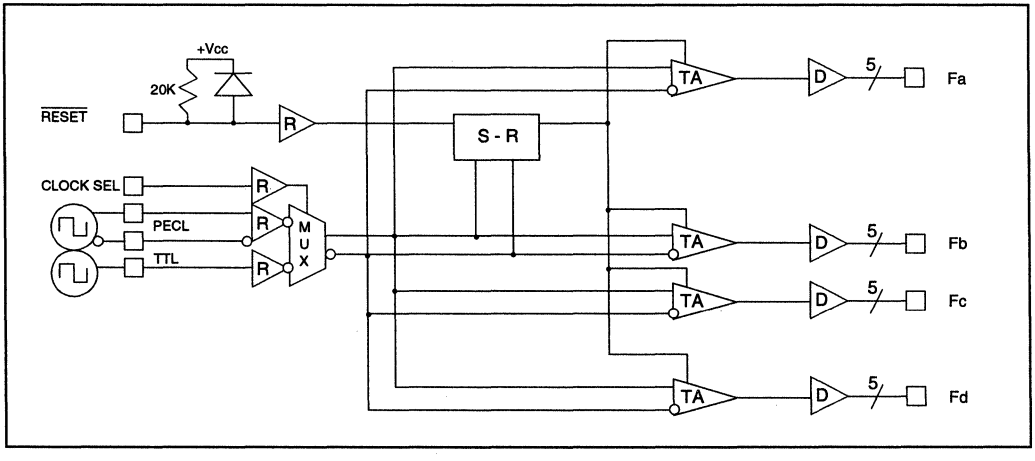
SC3506 Logic Diagram



SC3507 Logic Diagram



SC3508 Logic Diagram



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Absolute Maximum Ratings

Storage Temperature ..... -55° to +150°C
V_{CC} Potential to Ground ..... -0.5V to +7.0V
Input Voltage ..... -0.5V to +V_{CC}
Static Discharge Voltage ..... >1750V
Maximum Junction Temperature ..... +140°C
Latch-up Current ..... >200 mA
Operating Ambient Temperature ..... 0° to +70°C

Capacitance (package and die total)

Input Pins ..... 5.0 pF
TTL Output Pins ..... 5.0 pF

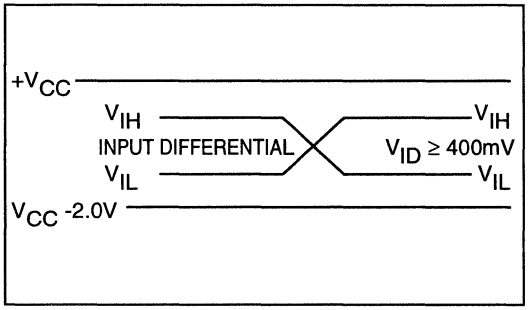
Electrical Characteristics

V_{CC} = +5.0V ± 5%, T_a = 0°C to +70°C (reference "AC Test/Evaluation Circuit")

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Voltage (PECL)	Differential Source–PECL	V_{IL} +0.4	+V_{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage (PECL)	Differential Source–PECL	V_{CC} -2.0	V_{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I_{IH}	Input HIGH Current (PECL)	V_{IN} = V_{CC} (max)		200	uA
	CLKSEL	V_{IN} = V_{CC} (max)		350	uA
	Reset	V_{IN} = 2.4V		-200	uA
	TTL, CSEL, BSEL	V_{IN} = 2.4V		15	uA
I_{IL}	Input LOW Current (PECL)	V_{IN} = V_{CC} -2.0V		15	uA
	CLKSEL	V_{IN} = 0.4V		50	uA
	Reset	V_{IN} = 0.5V		-325	uA
	TTL, CSEL, BSEL	V_{IN} = 0.4V		15	uA
V_{OH}	Output HIGH Voltage	F_{OUT} = 80MHz max C_L = 10pF	2.4		V
V_{OL}	Output LOW Voltage	F_{OUT} = 80MHz max C_L = 10pF		0.6	V
I_{OHS}[1]	Output HIGH Short Ckt Current	Output High, V_{OUT} = 0V Typ	-55		mA
I_{OLS}[1]	Output LOW Short Ckt Current	Output Low, V_{OUT} = V_{CC} Typ	55		mA
PWR	Static Core Power Dissipation	SC3500, 70°C, Typ Pwr=370 mW		600	mW
		SC3506, 70°C, Typ Pwr=350 mW		550	mW
		SC3507, 70°C, Typ Pwr=370 mW		600	mW
		SC3508, 70°C, Typ Pwr=340 mW		550	mW

1. Maximum test duration, one second.
2. The SC3500/06/07/08 features source series termination of approximately 40 Ohms to assist in matching 50–75 Ohm P.C. board environments.

PECL Differential Input Voltage Range



DC Characteristics

The outputs have been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high drive, totem pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the outputs will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V_{OH}	I_{OH} = -8mA	2.4V	
V_{OL}	I_{OL} = 4mA		0.6V

AC Specifications—Using "AC Test/Evaluation Circuit"

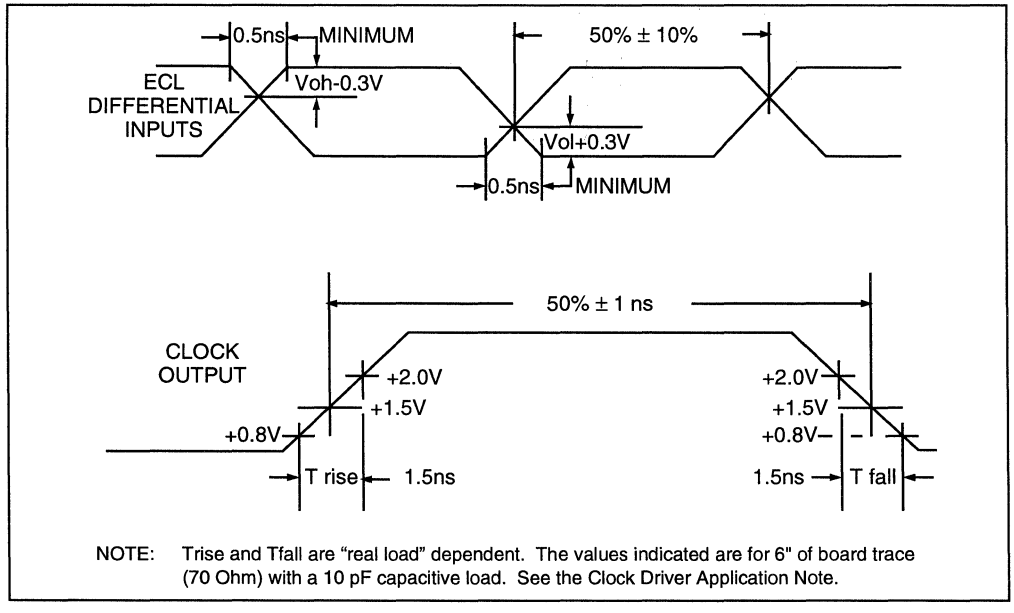
V_{CC} = +5.0V ± 5%, Ta = 0°C to +70°C, C_{LOAD} = 10pF

Parameter	SC3500	SC3506	SC3507	SC3508	Units
Maximum Skew Across All Outputs					
Options: Standard	1.0	1.0	1.0	1.0	ns
–1	0.5	0.5	0.5	0.5	
–2		0.5		0.5	
Maximum Skew Chip to Chip					
Options: Standard		—		—	
–1		—		—	
–2		1.0		1.0	
Maximum Skew within an Output Group	0.25	0.25	0.25	0.25	ns
Maximum Output Duty Cycle Asymmetry	±1.0	±1.0	±1.0		ns
Maximum TTL Input Frequency	80	80	80	80	MHz
Maximum PECL Differential Input Frequency	160	80	160	80	MHz
Maximum Rising/Falling Edge Rate	1.5	1.5	1.5	1.5	ns

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. Output Duty Cycle Asymmetry is defined as the Duty Cycle deviation from 50%, measured at 1.5V. Duty Cycle will be effected by voltage, temperature, and load (including the length of the PC trace). Only applies to divided outputs.
3. Typical skew derating factor for different loads is 50 ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
4. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pf capacitive load. See "AC Test/Evaluation Circuit." Synchronous outputs may be paralleled for higher loads.
5. Parameters guaranteed by design and characterization.

Threshold Crossing Characteristics



NOTE: Trise and Tfall are "real load" dependent. The values indicated are for 6" of board trace (70 Ohm) with a 10 pF capacitive load. See the Clock Driver Application Note.

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DESCRIPTION OF OPERATION (Refer to Logic Diagrams)

AMCC has developed a single-chip clock shape and 20-output fan-out device using AMCC's advanced BiCMOS process. This design has been optimized for clock symmetry and absolute minimum skew across all twenty outputs.

For highest performance this approach requires a clock source input from a crystal-controlled oscillator (XCO) located adjacent to this clock driver. This oscillator, operating between +5V and ground, can provide either differential ECL inputs (referenced to +5V, PECL) or TTL (CMOS) input levels to AMCC's Clock Driver. The input selection is accomplished via the "Clock Sel" input where a "HIGH" level activates the differential ECL input and a "LOW" activates the TTL input. This input clock will be fanned out to a divide-down counter and master-slave flip-flops for synchronization (refer to the Logic Diagrams).

The RESET input is provided to hold off or clear the outputs as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor (4.7uF = ~100 ms) is connected between this pin and ground, the device will respond with a "power up reset"—a delay in the clock outputs becoming active. At the onset of RESET (low) the outputs will go low following five falling edge clock inputs (four clock inputs for the SC3506 and SC3508). At the expiration of RESET (high) outputs will resume, after five falling edge clock inputs (four clock inputs for the SC3506 and SC3508), from a high (leading edge) count origin (see Figure 5, Reset To Output Timing in the Clock Driver Application Note).

The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion resulting from simultaneous switching of the 20 outputs. These outputs also feature series termination (~40 Ohms) to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50–75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance) and/or large peak voltage amplitudes (>3.5 Volts), two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current.

Power and ground are interdigitated with the outputs. Of the 52 package pins, 22 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance $+V_{CC}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see the Clock Driver Application Note for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance, and capacitance of the package and wire bonding is managed to insure that the clock driver will exhibit skews less than the specified maximum. A plastic 52-lead quad flat pack with .039" lead pitch is employed with an outer lead square footprint of approximately 0.7" per side.

SC3500/06/07/08 Product Selection Guide

	Output Frequency with Respect to Input Frequency					
P/N	Total Outputs	Number of Outputs ÷ 1	Number of Outputs ÷ 2	Number of Outputs ÷ 2 or 4	Special Features	Package
SC3500	20	10	5 ÷ 1 or 2	5	—	52 PQFP
SC3506	20	10	10	N/A	—	52 PQFP
SC3507	20	10	N/A	10	—	52 PQFP
SC3508	20	20	N/A	N/A	—	52 PQFP

SC3500 Output Clock Frequency Selection

"B" SEL	"C" SEL	XCO FREQ	Fa	Fb	Fc
LO	LO	F	F/2	F/4	F/8
HI	LO	F	F/2	F/2	F/8
LO	HI	F	F/2	F/4	F/4
HI	HI	F	F/2	F/2	F/4

Note: XCO is the input frequency for either the PECL Inputs or the TTL Input. Non-crystal oscillator sources may be used at the user's discretion. See the Clock Driver Application Note.

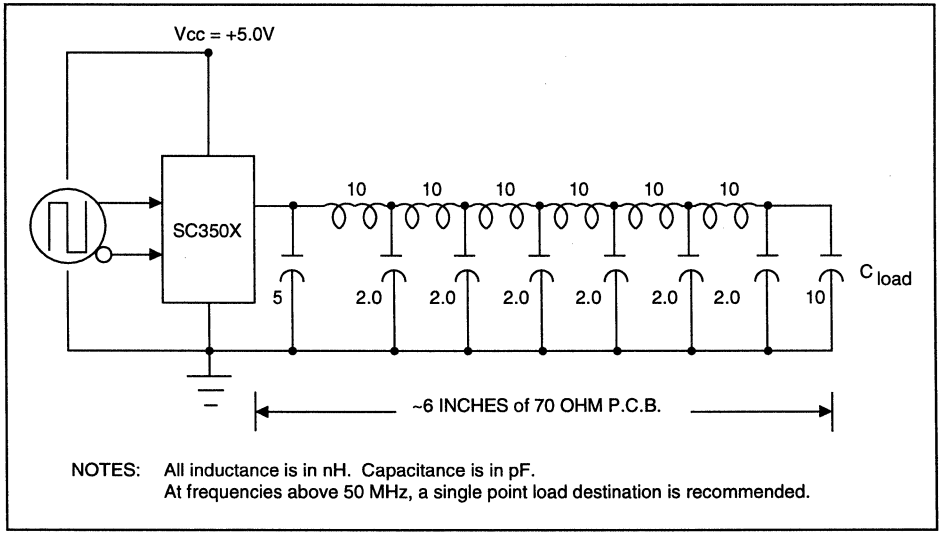
SC3507 Output Clock Frequency Selection

"B" SEL	"C" SEL	XCO FREQ	Fa1, Fa2	Fb	Fc
LO	LO	F	F/2	F/4	F/4
HI	LO	F	F/2	F/2	F/4
LO	HI	F	F/2	F/4	F/2
HI	HI	F	F/2	F/2	F/2

Note: XCO is the input frequency for either the PECL inputs or the TTL input. Non-crystal oscillator sources may be used at the user's discretion. See the Clock Driver Application Note.

SC3506 and SC3508 have no frequency selection capabilities.

AC Test/Evaluation Circuit



NOTES: All inductance is in nH. Capacitance is in pF.
At frequencies above 50 MHz, a single point load destination is recommended.

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Power Management

The overall goal of managing the power dissipated by the clock driver is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the clock driver is determined by the load that each output drives and the frequency that each output is running. The "Output Power Dissipation" table summarizes these dependencies (see the "AC Test/Evaluation Circuit", for complete load definition).

The output power must be added to the core power (600 mW) of the clock driver to determine the total power being dissipated by the clock driver. This total power is then multiplied by the clock driver's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the SC350X. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the clock driver is detailed in the 52-pin PQFP Thermal Dissipation vs. Airflow graph in the Package appendix at the end of this section.

For example: An application utilizes an clock driver with 8 Fa outputs driving 10 pF loads at 66 MHz, 3 Fb outputs driving 5 pF loads at 33 MHz and 2 Fc outputs driving 15 pF loads at 33 MHz. Total chip power is calculated as follows:

Core Power (SC3500)	= 600 mW
8 Fa, 10 pF, 66 MHz = (8 x 47 mW)	= 376 mW
2 Fa, no load, 66 MHz = (2 x 16 mW)	= 32 mW
3 Fb, 5 pF, 33 MHz = (3 x 19 mW)	= 57 mW
2 Fb, no load, 33 MHz = (2 x 12 mW)	= 24 mW
2 Fc, 15 pF, 33 MHz = (2 x 24 mW)	= 48 mW
3 Fc, no load, 33 MHz = (3 x 12 mW)	= 36 mW
Total Power	= 1173 mW

The design specifies a 70°C still air ambient. Referring to the 52-pin PQFP Thermal Dissipation vs. Airflow graph in the Package appendix, the Θ_{ja} for still air is 46.2°C/watt. The clock driver's junction temperature would then be:

70°C + (1.173 watts x 46.2°C/watt) = 124°C

Note this is below the 140°C maximum junction temperature.

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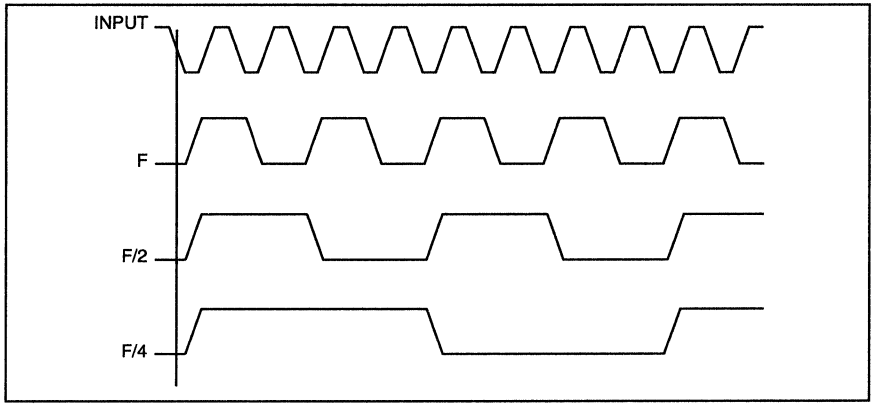
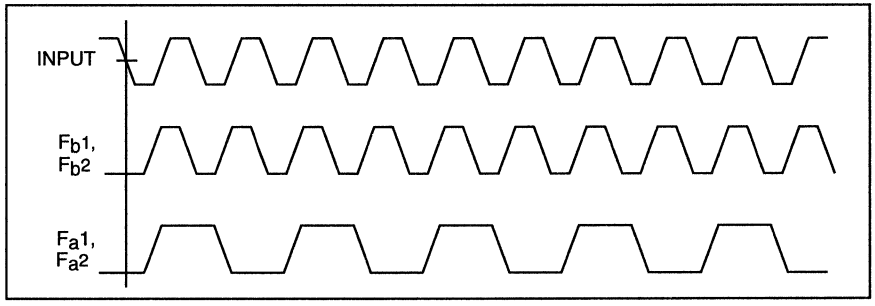
Output Power Dissipation

FREQUENCY	C_{LOAD}=5pF	C_{LOAD}=10pF	C_{LOAD}=15pF	C_{LOAD}=25pF	NO LOAD
80 MHz	42 mW	51 mW	61 mW	88 mW	18 mW
66 MHz	38 mW	47 mW	55 mW	75 mW	16 mW
50 MHz	28 mW	33 mW	39 mW	60 mW	14 mW
40 MHz	25 mW	30 mW	36 mW	52 mW	13 mW
33 MHz	19 mW	22 mW	24 mW	46 mW	12 mW
25 MHz	16 mW	18 mW	20 mW	32 mW	11 mW
20 MHz	14 mW	16 mW	18 mW	24 mW	10 mW

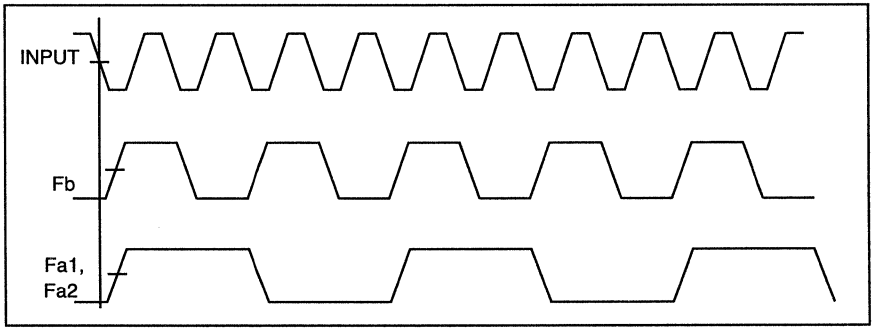
SC3500 Relative Output Timing



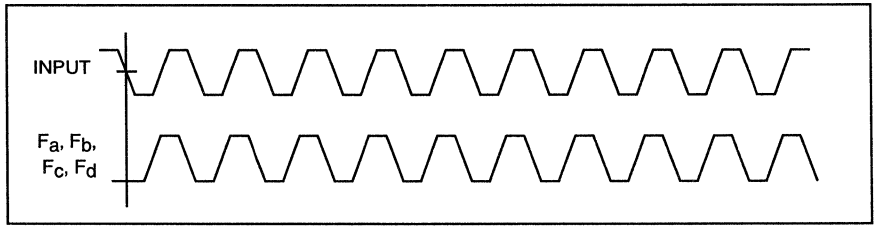
SC3506 Relative Output Timing



SC3507 Relative Output Timing



SC3508 Relative Output Timing



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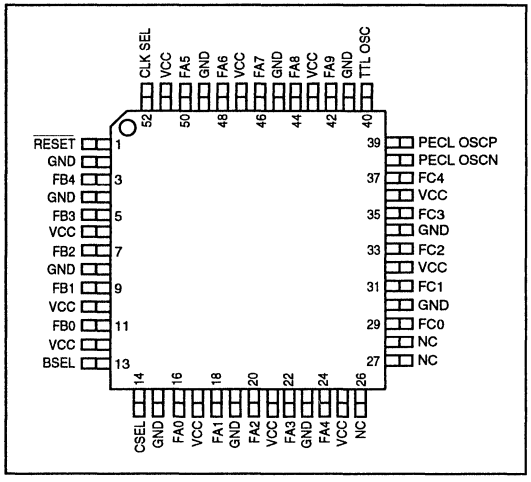
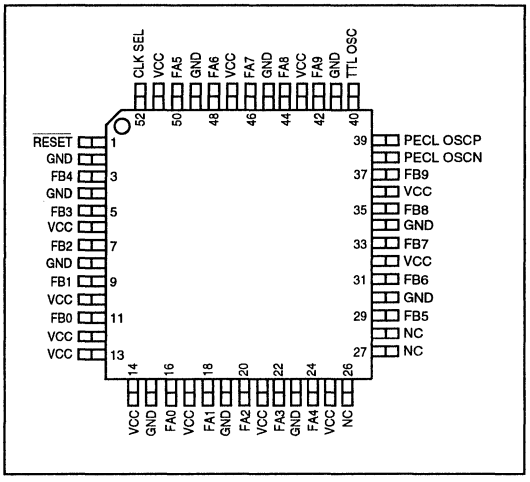
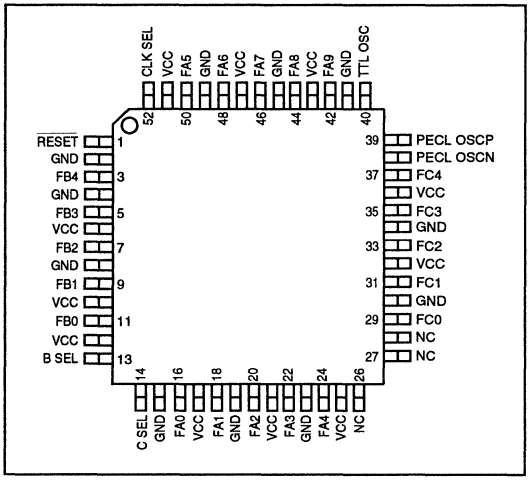
SC3500 Pinout



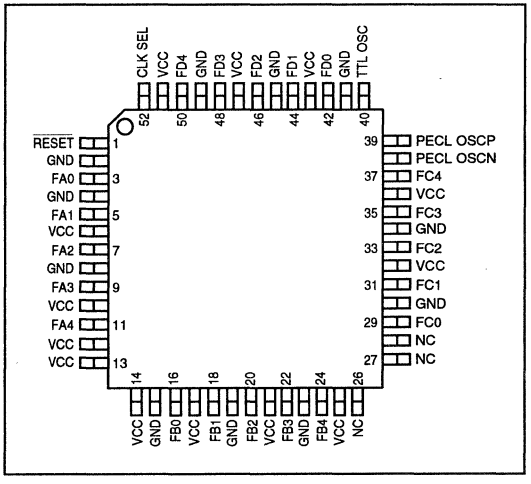
SC3506 Pinout



SC3507 Pinout



SC3508 Pinout



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Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Skew Option (if applicable)**
- **Optional Shipping Configuration**

SC350X **Q** **–1** **/TD**

Optional Shipping Configuration
Blank = 84-unit matrix tray
/D = dry pack
/TD = tape, reel and dry pack

Skew Option
Blank = 1.0 ns output-output skew
– 1 = 500 ps output-output skew
– 2 = 1.0 ns chip-to-chip skew

Package Option
Q = 52-pin Plastic Quad Flat Pack (PQFP)

Device Number

Example: SC350XQ–1/D
52-pin PQFP package, 500 ps output-output skew, shipped dry packed in the standard matrix tray.

Part Number	Standard	–1	–2
SC3500	✔	✔	N/A
SC3506	✔	✔	✔
SC3507	✔	✔	N/A
SC3508	✔	✔	✔

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FEATURES

- **Nine or Ten clock outputs:**
  - Outputs operate at frequencies, up to 80 MHz
  - Outputs grouped in two banks of five outputs on SC3517/18/28/29
  - Outputs grouped in a bank of four and a bank of five outputs on the SC3526
  - Outputs grouped in a bank of three and a bank of seven outputs on the SC3527
- **Leading edge skew for all outputs ≤0.35 ns**
- **Proprietary output drivers with:**
  - Complementary 24 mA peak outputs, source and sink
  - 50–75Ω source series termination
  - Dynamic drive adjustment to match load conditions
  - Edge rates less than 1.5 ns
- **Minimizes the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**
- **28-pin SOIC package**

APPLICATIONS

- **Compatible with Intel's Pentium™ processor**
- **Compatible with PowerPC™ processors**
- **PCI Bus clock distribution**
- **Workstation and server systems with high clock fanout**
- **Datacom and Telecom networks**

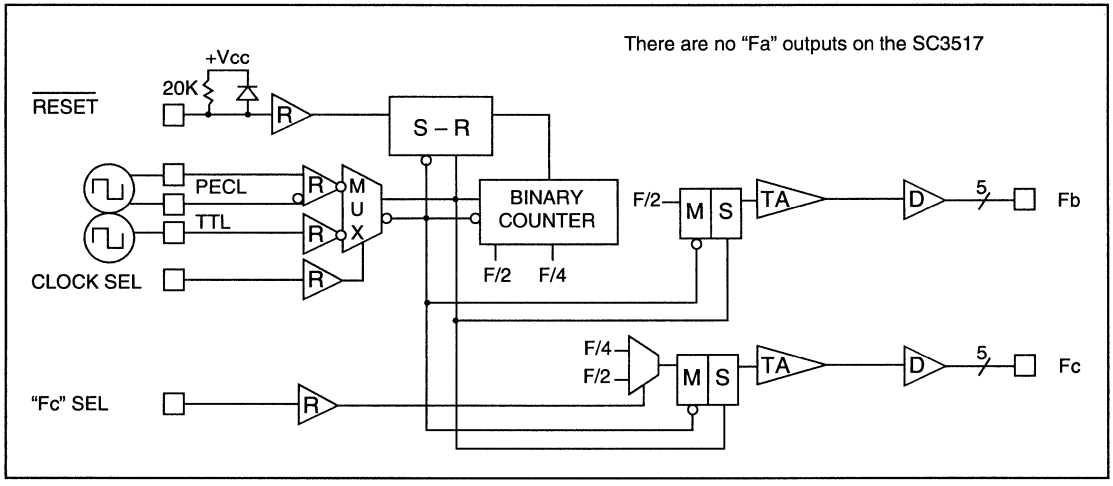
GENERAL DESCRIPTION

The SC3517, SC3518, SC3526, SC3527, SC3528 and SC3529 are precision low skew clock drivers with nine or ten outputs. They require a clock input from a single-ended TTL or an ECL differential source operating between +5V and ground. This reference frequency input is received and distributed to divide-by-two master-slave flip-flops or to the clock output drivers.

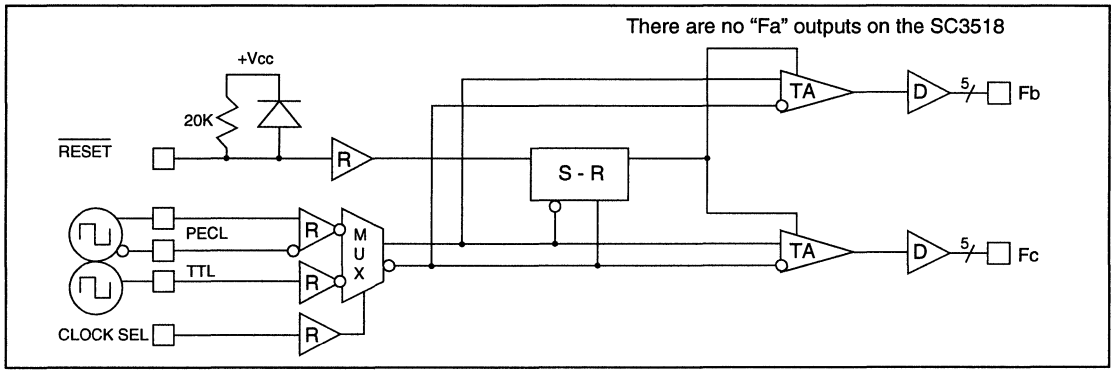
Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of ≈1.5V/ns to minimize simultaneous output-switching noise and distortion.

3

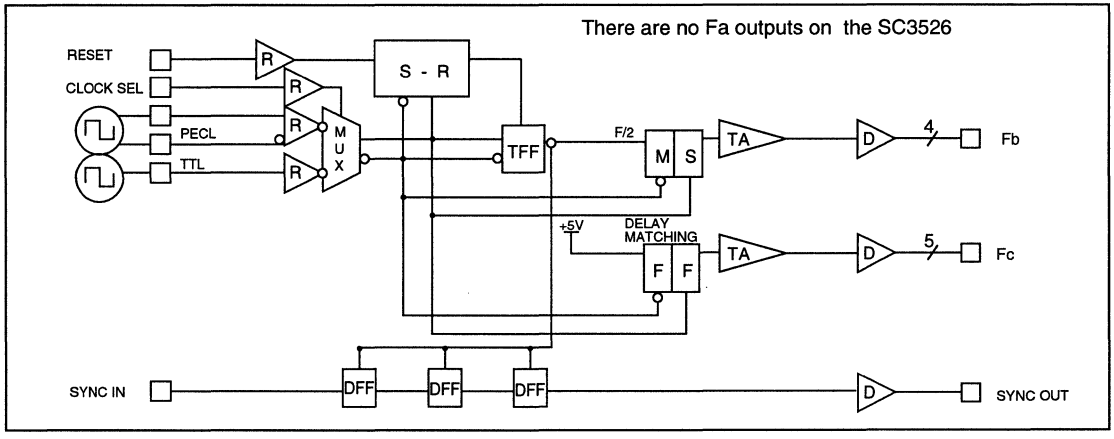
SC3517 Logic Diagram



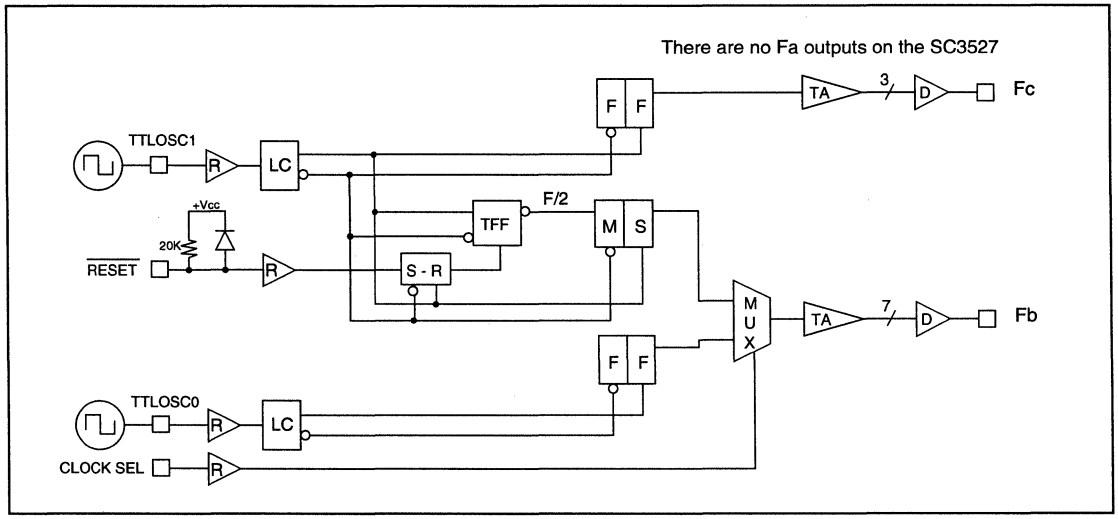
SC3518 Logic Diagram



SC3526 Logic Diagram



SC3527 Logic Diagram



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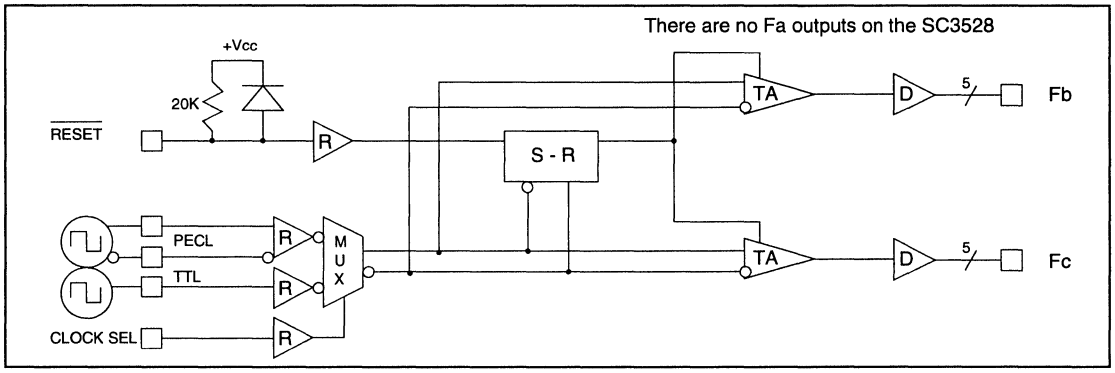
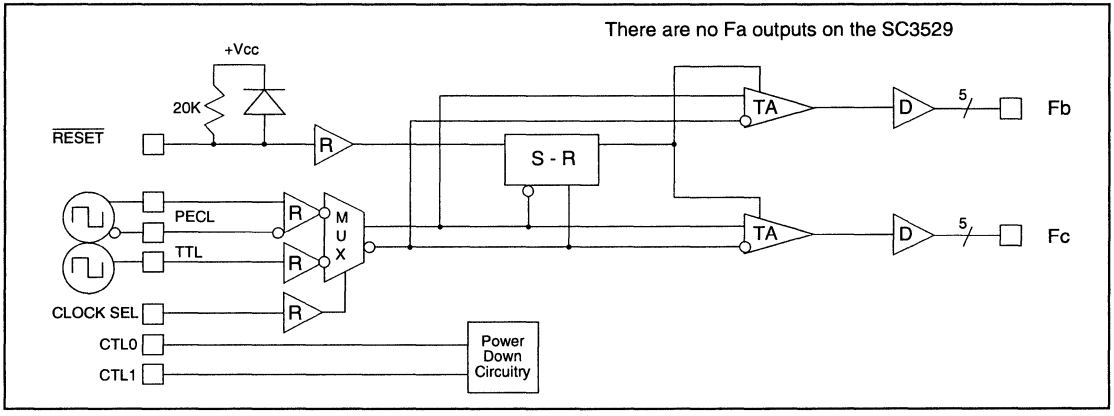
SC3528 Logic Diagram



SC3529 Logic Diagram



SC3517/18/26/27/28/29 Product Selection Guide

	Output Frequency with Respect to Input Frequency					
P/N	Total Outputs	Number of Outputs ÷ 1	Number of Outputs ÷ 2	Number of Outputs ÷ 2 or 4	Special Features	Package
SC3517	10	5	N/A	5	—	28 SOIC
SC3518	10	10	N/A	N/A	—	28 SOIC
SC3526	9	5	4	N/A	Sync Output	28 SOIC
SC3527	10	3	7	N/A	Selectable single or dual clock input.	28 SOIC
SC3528	10	10	N/A	N/A	—	28 SOIC
SC3529	10	10	N/A	N/A	Power Down	28 SOIC

Absolute Maximum Ratings

Storage Temperature ..... -55° to +150°C
V_{CC} Potential to Ground ..... -0.5V to +7.0V
Input Voltage ..... -0.5V to +V_{CC}
Static Discharge Voltage ..... >1750V
Maximum Junction Temperature ..... +140°C
Latch-up Current ..... >200 mA
Operating Ambient Temperature ..... 0° to +70°C

Capacitance (package and die total)

Input Pins ..... 5.0 pF
TTL Output Pins ..... 5.0 pF

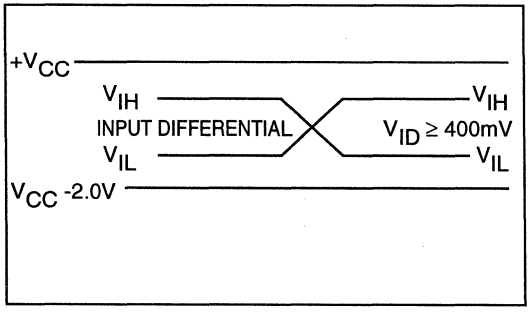
Electrical Characteristics

V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C (reference "AC Test/Evaluation Circuit")

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Voltage (PECL)	Differential Source–PECL	V_{IL} +0.4	+V_{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage (PECL)	Differential Source–PECL	V_{CC} -2.0	V_{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I_{IH}	Input HIGH Current (PECL)	V_{IN} = V_{CC} (max)		200	uA
	CLKSEL	V_{IN} = V_{CC} (max)		350	uA
	RESET	V_{IN} = 2.4V		-200	uA
	TTL, CSEL	V_{IN} = 2.4V		15	uA
I_{IL}	Input LOW Current (PECL)	V_{IN} = V_{CC} -2.0V		15	uA
	CLKSEL	V_{IN} = 0.4V		25	uA
	RESET	V_{IN} = 0.5V		-325	uA
	TTL, CSEL	V_{IN} = 0.4V		15	uA
V_{OH}	Output HIGH Voltage	F_{OUT} = 80MHz max C_L = 10pF	2.4		V
V_{OL}	Output LOW Voltage	F_{OUT} = 80MHz max C_L = 10pF		0.6	V
I_{OHS}[1]	Output HIGH Short Ckt Current	Output High, V_{OUT} = 0V Typ	-55		mA
I_{OLS}[1]	Output LOW Short Ckt Current	Output Low, V_{OUT} = V_{CC} Typ	55		mA
PWR	Static Core Power Dissipation	SC3517, 70°C, Typ Pwr=370 mW		600	mW
		SC3518, 70°C, Typ Pwr=250 mW		425	mW
		SC3526, 70°C, Typ Pwr=225 mW		375	mW
		SC3527, 70°C, Typ Pwr=350 mW		350	mW
		SC3528, 70°C, Typ Pwr=425 mW		425	mW
		SC3529, 70°C, Typ Pwr=250 mW		425	mW

1. Maximum test duration, one second.
2. The SC3517/18/26/27/28/29 features source series termination of approximately 40 Ohms to assist in matching 50–75 Ohm P.C. board environments.

PECL Differential Input Voltage Range



DC Characteristics

The outputs have been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high-drive, totem-pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the outputs will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V_{OH}	I_{OH} = -8mA	2.4V	
V_{OL}	I_{OL} = 4mA		0.6V

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AC Specifications — Using "AC Test/Evaluation Circuit"

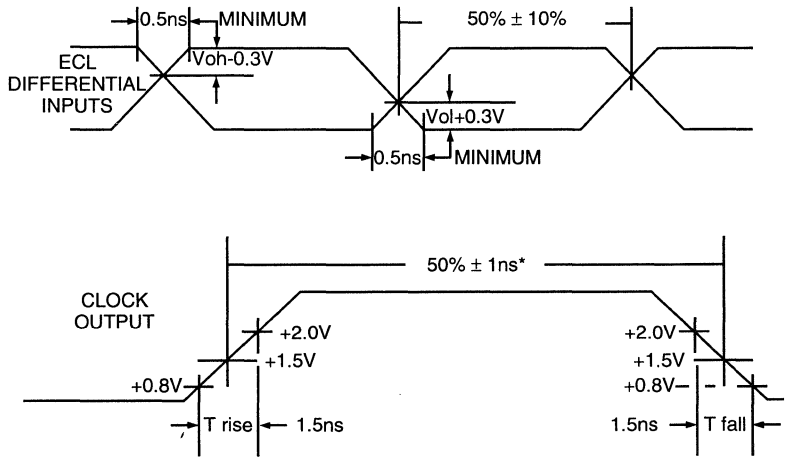
V_{CC} = +5.0V ± 5%, Ta = 0°C to 70°C, C_{LOAD} = 10pF

Parameter	SC3517	SC3518	SC3526	SC3527	SC3528	SC3529	Units
Maximum Skew Across All Outputs Options: Standard –1	 1.0 0.5	 — 0.5	 0.35 —	 —	 0.35	 0.35	 ns
Delay of Fb from Fc outputs (CLKSEL = 1) [Tdly]	—	—	—	Min. 50 Typ. 0.9 Max. 1.7	—	—	ps ns ns
Maximum Skew within an Output Group	0.25	0.25	—	Fb .50 Fc .35	—	—	ns
Maximum Output Duty Cycle Asymmetry	±1.0 ns	—	Min. 45% Max. 55%	Min. 45% Max. 55%	—	—	ns or %
Maximum TTL Input Frequency	80	80	80	80	80	80	MHz
Maximum PECL Differential Input Frequency	160	80	80	80	80	80	MHz
Maximum Rising/Falling Edge Rate	1.5	1.5	1.5	1.5	1.5	1.5	ns

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. Output Duty Cycle Asymmetry is defined as the Duty Cycle deviation from 50%, measured at 1.5V. Duty Cycle will be affected by voltage, temperature, and load (including the length of the PC trace).
3. Typical skew derating factor for different loads is 50 ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
4. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pf capacitive load. See "AC Test/Evaluation Circuit." Synchronous outputs may be paralleled for higher loads.
5. Parameters guaranteed by design and characterization.

Threshold Crossing Characteristics



NOTE: Trise and Tfall are "real load" dependent. The values indicated are for 6" of board trace (70 Ohm) with a 10 pF capacitive load. See the Clock Driver Application Note.

* Applies only to divide-by-two outputs.

DESCRIPTION OF OPERATION
(Refer to Logic Diagram)

AMCC has developed single-chip, nine or ten-output clock buffer drivers using AMCC's advanced BiCMOS process. These designs have been optimized for minimum skew.

The clock source input for these devices may operate between +5V and ground and can provide either differential ECL inputs (referenced to +5V, PECL) or single-ended TTL (CMOS) levels. This selection is accomplished by use of the CLKSEL pin, where logic LOW (or "float") selects TTL and logic HIGH selects PECL. On the SC3527, when CLKSEL is low (or floating) TTLOSC0 is used to drive the FB0-6 outputs, and when CLKSEL is high, both output groups use the TTLOSC1 reference input clock (see SC3527 Application Examples). This input clock will be fanned out to translation amplifiers and output drivers, refer to the preceding logic diagrams. The output duty cycle asymmetry becomes a function of the output driver slew rate into the AC load for divided outputs. For simple buffered (1x frequency) outputs, the output duty cycle asymmetry becomes a function of the input clock waveshape and the output driver slew rate into the AC load.

The RESET input is provided to hold off or clear the outputs, as may be required by the user's system. This pin may be logically driven from a TTL output. For the products with (pullup) resistors on the RESET input, a capacitor (4.7μF ≈ 100 ms) connected between this pin and ground will cause the device to respond with a "power-up reset"—a delay in the clock outputs becoming active. At the assertion of RESET the SC3518/28/29 outputs will go low following four falling edge clock inputs. The SC3527 outputs will go low after three falling edge clock inputs and the SC3517 output will go low after five falling edge clock inputs. At the deassertion of RESET, the SC3518/28/29 outputs will resume operation after four falling edge clock inputs. The SC3527 outputs will resume after three falling edge clock inputs and the SC3517 outputs will resume operation after five falling edge clock inputs.

The RESET input of the SC3526 operates in a different fashion. When RESET is held high (asserted), the FC0-4 outputs will continue to run while the FB0-3 outputs will be driven to a static high. When RESET is de-asserted, the FB0-3 outputs will be active after a fixed three-input clock delay, from a leading edge count origin.

The SC3526 also includes a synchronization circuit. The synchronization circuit provides three serial flip flops clocked by the internally generated F/2 (half reference frequency) clock which can be used to provide a three-stage metastability filter or a three-cycle delay of the F/2 outputs. The circuit receives its input from the SYNCIN input and feeds the D-input to the first flip-flop; the Q output of the flip-flop feeds the D-input of the second flip-flop which, in turn, feeds the third flip-flop. The Q output of the third flip-flop drives the SYNCOUT pin.

For the SC3529, the CTL0 and CTL1 inputs can be used to "power down" two, five, or ten of the SC3529's outputs. The control circuitry is designed to be synchronous with the reference clock to prevent duty cycle distortion during power-up or power-down sequencing.

When the inputs are configured (see "SC3529 Input Confiiguration table"), the appropriate outputs are driven to the minimum power state (LOW). With all outputs disabled, the power of the device is equal to its static dissipation of 250 mW.

The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion resulting from simultaneous switching of the 10 outputs. These outputs also feature series termination (~40 Ohms) to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50 to 75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance at higher frequencies) and/or large peak voltage amplitudes (>3.5 Volts), two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see the Clock Driver Application Note).

Power and ground are interdigitated with the outputs. Of the 28 package pins, 10 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance $+V_{CC}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see the Clock Driver Application Note for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance, and capacitance of the package and wire bonding is managed to ensure that the clock driver will exhibit skews less than the specified maximum. A plastic 28-lead small outline package with .050" lead pitch is employed with an outer lead rectangular footprint of approximately 0.7" by 0.4".

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SC3529 Input Configuration

CTL0	CTL1	FUNCTION
0	0	All Outputs enabled
0	1	FC0 – FC4 enabled
1	0	FB0 – FB1 enabled
1	1	All outputs disabled

SC3517 Output Clock Frequency Selection

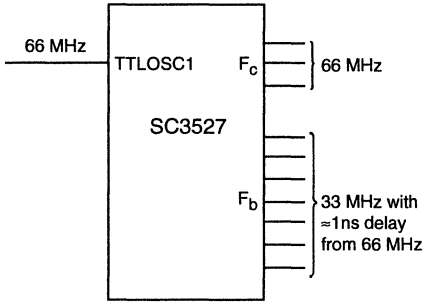
"C" SEL	XCO FREQ	Fb	Fc
LO	F	F/2	F/4
HI	F	F/2	F/2

Note: XCO is the input frequency for either the PECL Inputs or the TTL Input. Non–crystal oscillator sources may be used at the user's discretion. See the Clock Driver Application Note.

SC3527 Application Examples

Example 1.
Low Skew, Single Reference Frequency Mode

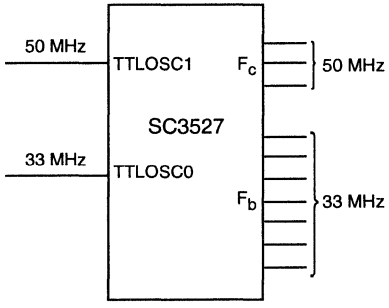
Three outputs at the primary frequency and seven outputs at half the primary frequency; each group internally synchronized. The 33 MHz outputs are delayed from the 66 MHz outputs by ≈1 ns.



CLKSEL = 1

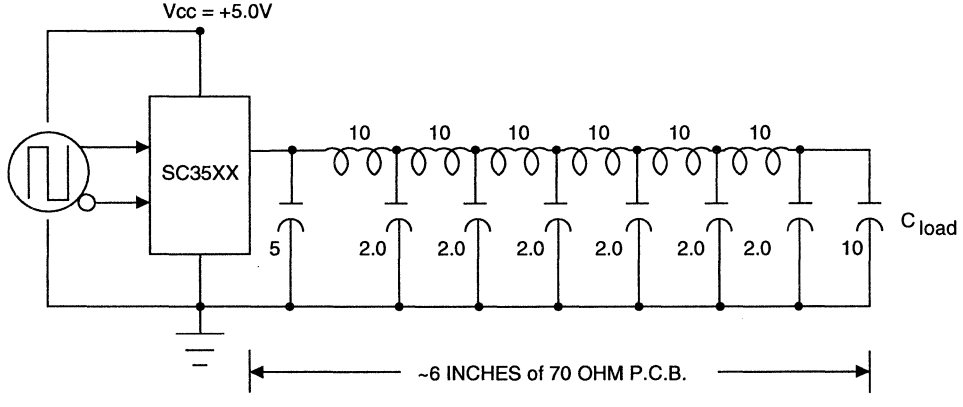
Example 2.
Dual Reference Frequency Mode, Asynchronous

Three outputs at the primary frequency and seven outputs at the secondary frequency with ≈1 ns internal delay at the F_b outputs.



CLKSEL = 0

AC Test/Evaluation Circuit



NOTES: All inductance is in nH. Capacitance is in pF.
At frequencies above 50 MHz, a single point load destination is recommended.

Power Management

The overall goal of managing the power dissipated by the clock driver is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the clock driver is determined by the load that each output drives and the frequency that each output is running. The "Output Power Dissipation" table summarizes these dependencies (see "AC Test/ Evaluation Circuit", for complete load definition).

The output power must be added to the core power (600 mW) of the clock driver to determine the total power being dissipated by the clock driver. This total power is then multiplied by the clock driver's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the clock driver. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the clock driver is detailed in the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix at the end of this section.

For example: An application utilizes a clock driver with 5 Fa outputs driving 10 pF loads at 66 MHz and 4 Fb outputs driving 15 pF loads at 33 MHz. Total chip power is calculated as follows:

Core Power (SC3517)	= 600 mW
5 Fa, 10 pF, 66 MHz = (5 x 47 mW)	= 235 mW
4 Fb, 15 pF, 33 MHz = (4 x 24 mW)	= 96 mW
1 Fb, no load, 33 MHz = (1 x 12 mW)	= 12 mW
	Total Power = 1173 mW

The design specifies a 70°C still air ambient. Referring to the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix, the Θ_{ja} for still air is 57.7°C/watt. The clock driver's junction temperature would then be:

70°C + (0.943 watts x 57.7°C/watt) = 124°C

Note this is below the 140°C maximum junction temperature.

Output Power Dissipation

FREQUENCY	C_{LOAD}=5pF	C_{LOAD}=10pF	C_{LOAD}=15pF	C_{LOAD}=25pF	NO LOAD
80 MHz	42 mW	51 mW	61 mW	88 mW	18 mW
66 MHz	38 mW	47 mW	55 mW	75 mW	16 mW
50 MHz	28 mW	33 mW	39 mW	60 mW	14 mW
40 MHz	25 mW	30 mW	36 mW	52 mW	13 mW
33 MHz	19 mW	22 mW	24 mW	46 mW	12 mW
25 MHz	16 mW	18 mW	20 mW	32 mW	11 mW
20 MHz	14 mW	16 mW	18 mW	24 mW	10 mW

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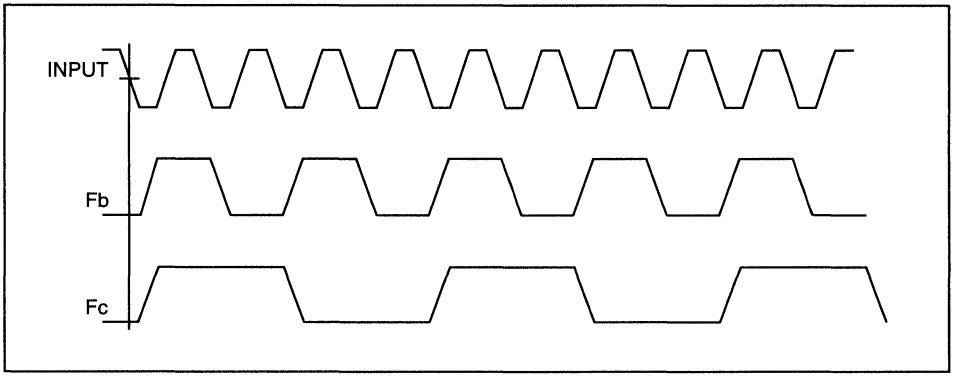
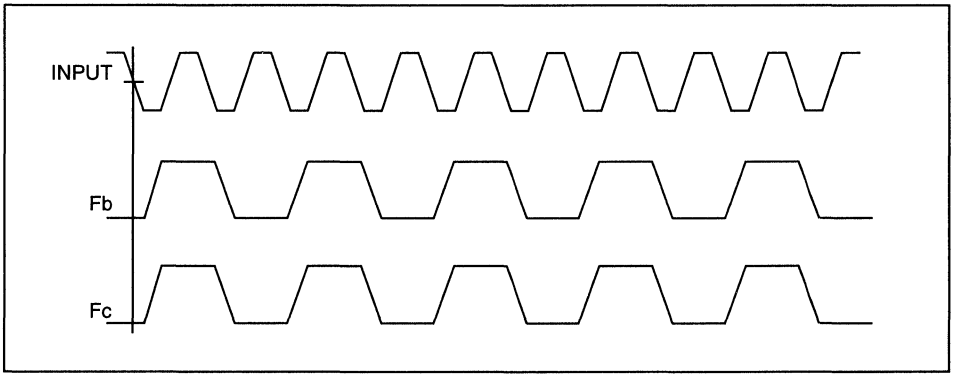
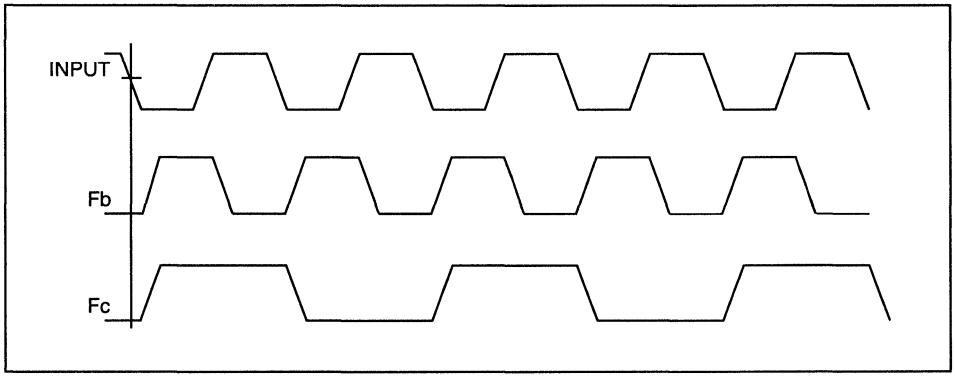
SC3517 Relative Output Timing



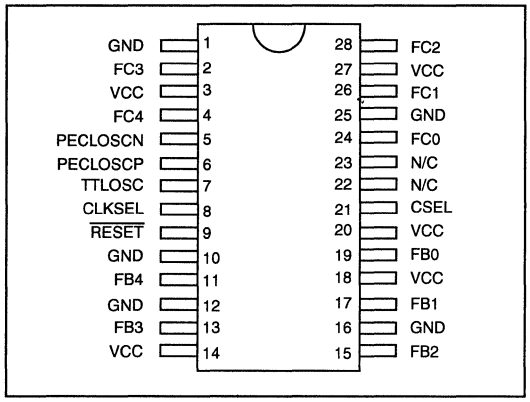
SC3518/28/29 Relative Output Timing



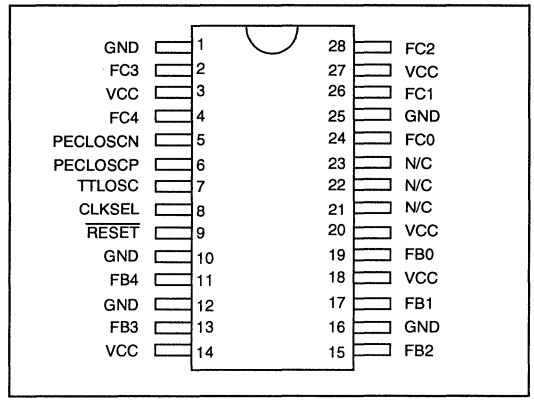
SC3526/27 Relative Output Timing



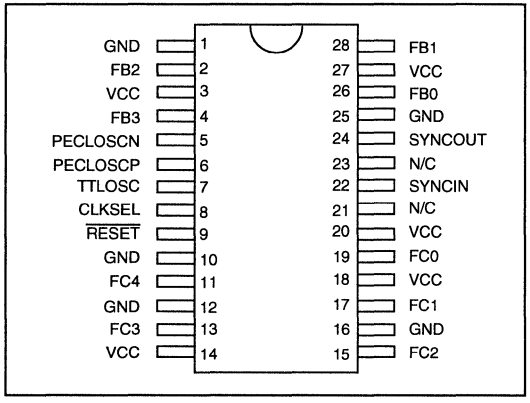
SC3517 Pinout



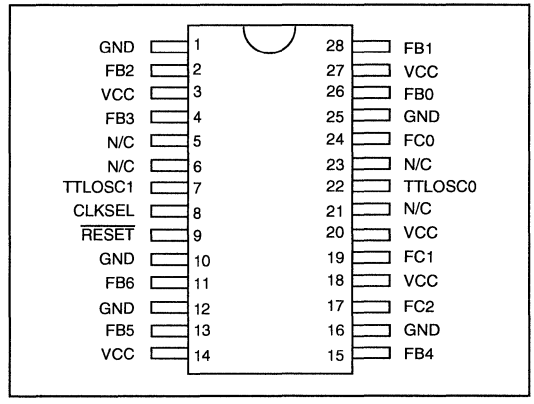
SC3518 Pinout



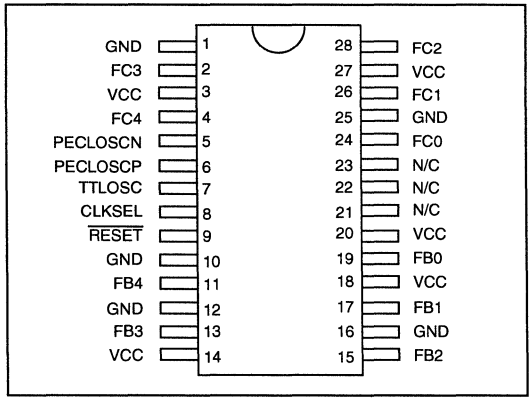
SC3526 Pinout



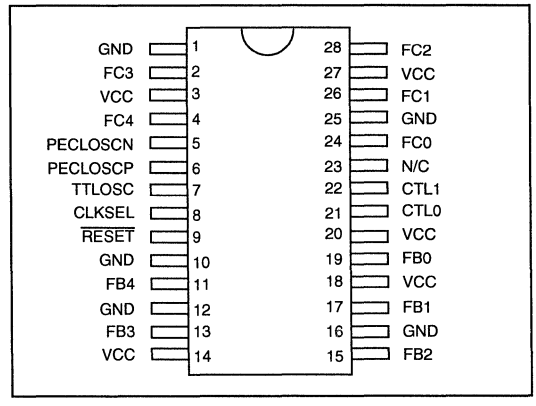
SC3527 Pinout



SC3528 Pinout



SC3529 Pinout



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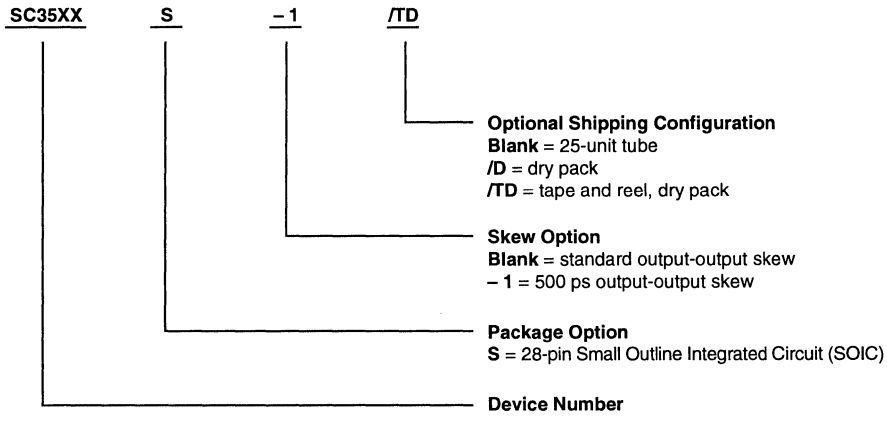
Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Skew Option (if applicable)**
- **Optional Shipping Configuration**



Example: SC35XXS–1/D
28-pin SOIC package, 500 ps output-output skew, shipped dry packed in the standard tube.

Part Number	Standard	–1
SC3517	✔	✔
SC3518	N/A	✔
SC3526	✔	N/A
SC3527	✔	N/A
SC3528	✔	N/A
SC3529	✔	N/A

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5V LVTTL I/O Clock Drivers

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CONTENTS

5V LVTTL I/O CLOCK DRIVERS

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20-OUTPUT LVTTL CLOCK DRIVERS

FEATURES

- **20 clock outputs:**
  - Ten or twenty outputs (SC3308) at primary frequency, up to 80 MHz
  - Ten outputs at 1/2 primary frequency (SC3306)
- **All outputs are leading edge synchronized to within ≤0.5 ns**
- **Proprietary output drivers with:**
  - Complementary 24 mA peak outputs, source and sink
  - 50–75Ω source series termination
  - Dynamic drive adjustment to match load conditions
  - Edge rates less than 1.5 ns
- **Output levels comply with JEDEC LVTTL standard**
- **+5V Vcc supply**
- **52 PQFP package**
- **Minimizes the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**

APPLICATIONS

- **Compatible with Intel's Pentium™ and Pentium Pro™ processors, and PowerPC™ 603/604 processors**
- **PCI Bus clock distribution**
- **Workstation and server systems with high clock fanout**
- **Datacom and Telecom networks**

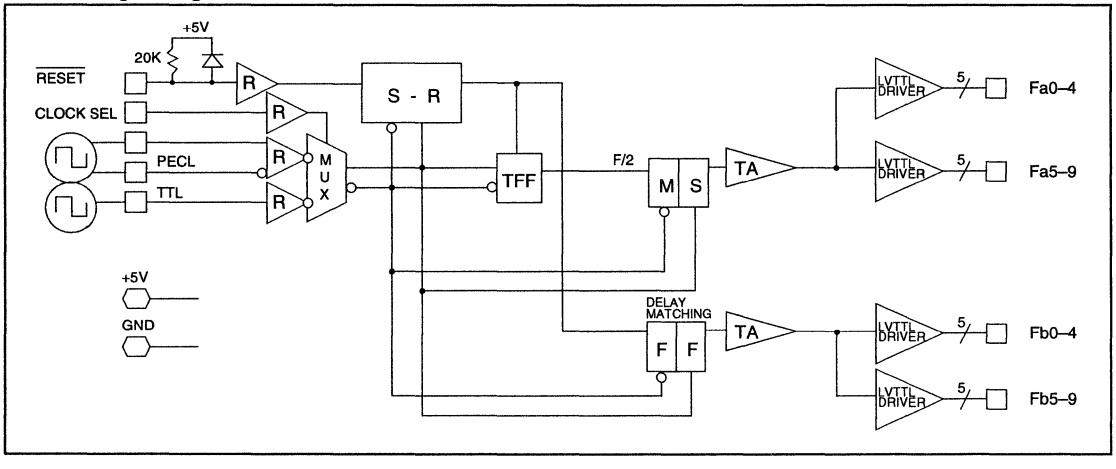
GENERAL DESCRIPTION

The SC3306 and SC3308 are precision low skew clock drivers with 20 outputs. These employ a clock input from a single-ended TTL or an ECL differential source operating between +5V and ground (PECL). This reference frequency input is received and distributed to divide-by-two or master-slave flip-flops. The resultant output is distributed to the clock output drivers. All outputs conform with JEDEC LVTTL levels.

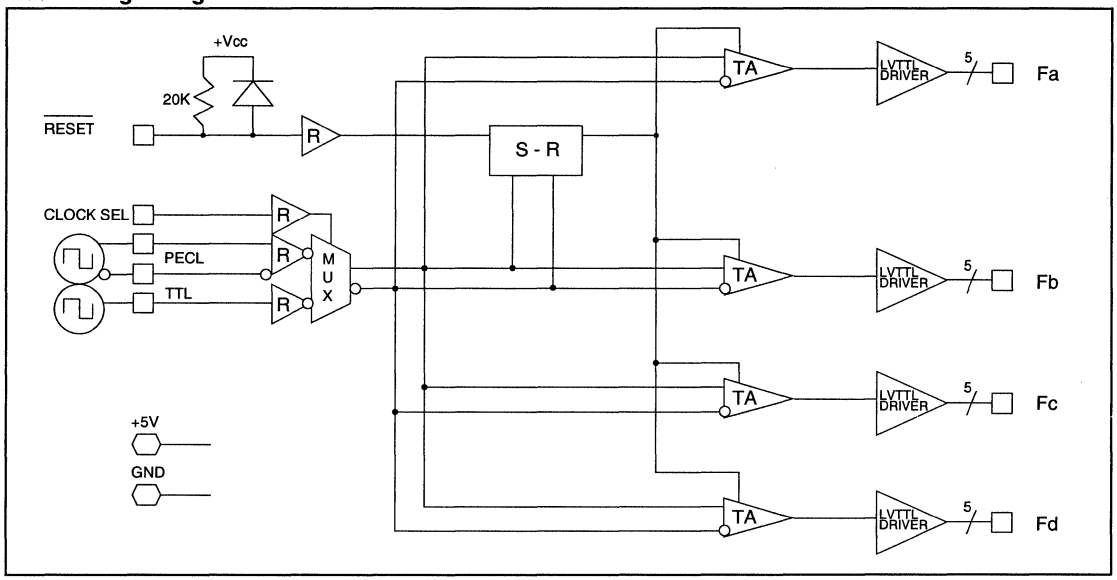
Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of ≈1.5V/ns to minimize simultaneous output-switching noise and distortion.

4

SC3306 Logic Diagram



SC3308 Logic Diagram



SC3306/08 Product Selection Guide

	Output Frequency with Respect to Input Frequency				
P/N	Total Outputs	Number of Outputs ÷ 1	Number of Outputs ÷ 2	Special Features	Package
SC3306	20	10	10		52 PQFP
SC3308	20	20	N/A		52 PQFP

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Absolute Maximum Ratings

Storage Temperature ..... -55° to +150°C
V_{CC} Potential to Ground ..... -0.5V to +7.0V
Input Voltage ..... -0.5V to +V_{CC}
Static Discharge Voltage ..... >1750V
Maximum Junction Temperature ..... +140°C
Latch-up Current ..... >200 mA
Operating Ambient Temperature ..... 0° to +70°C

Capacitance (package and die total)

Input Pins ..... 5.0 pF
TTL Output Pins ..... 5.0 pF

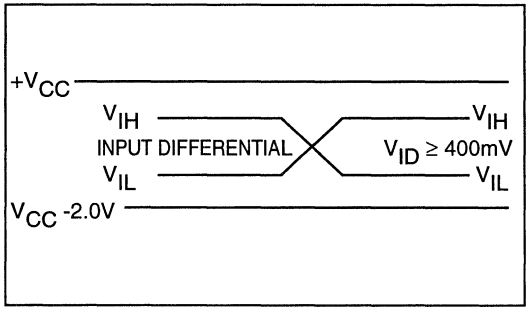
Electrical Characteristics

V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C (reference "AC Test/Evaluation Circuit")

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Voltage (PECL)	Differential Source–PECL	V_{IL} +0.4	V_{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage (PECL)	Differential Source–PECL	V_{CC} -2.0	V_{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I_{IH}	Input HIGH Current (PECL)	V_{IN} = V_{CC} (max)		200	uA
	CLKSEL	V_{IN} = V_{CC} (max)		350	uA
	RESET	V_{IN} = 2.4V		-200	uA
	TTL	V_{IN} = 2.4V		15	uA
I_{IL}	Input LOW Current (PECL)	V_{IN} = V_{CC} -2.0V		15	uA
	CLKSEL	V_{IN} = 0.4V		25	uA
	RESET	V_{IN} = 0.5V		-325	uA
	TTL	V_{IN} = 0.4V		15	uA
V_{OH}	Output HIGH Voltage	F_{OUT} = 80MHz, C_L = 10pF	2.3	3.65	V
V_{OL}	Output LOW Voltage	F_{OUT} = 80MHz, C_L = 10pF		0.4V	V
I_{OHS}[1]	Output HIGH Short Ckt Current	Output High, V_{OUT} = 0V Typ	-45		mA
I_{OLS}[1]	Output LOW Short Ckt Current	Output Low, V_{OUT} = V_{CC} Typ	55		mA
PWR	Static Core Power Dissipation	SC3306, 70°C, Typ Pwr=370mW		600	mW
		SC3308, 70°C, Typ Pwr=370mW		600	mW

1. Maximum test duration, one second.
2. The driver feature source series termination of approximately 40 Ohms to assist in matching 50–75 Ohm P.C. board environments.

PECL Differential Input Voltage Range



DC Characteristics

The outputs have been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high-drive, totem-pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the outputs will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V_{OH}	I_{OH} = -2mA	2.1V	
V_{OL}	I_{OL} = 2mA		0.6V

AC Specifications—Using "AC Test/Evaluation Circuit"

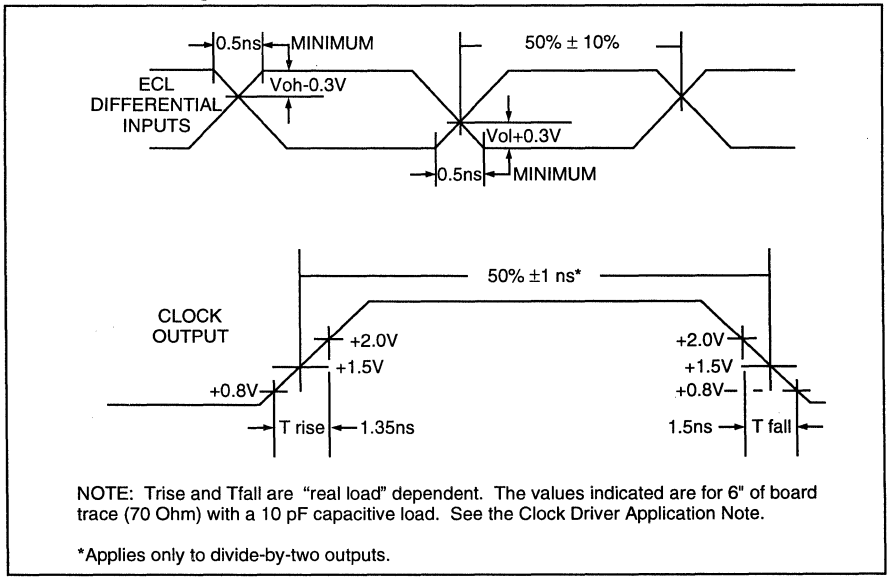
V_{CC} = +5.0V ± 5%, Ta = 0°C to +70°C, C_{LOAD} = 10pF

Parameter	SC3306	SC3308	Units
Maximum Skew Across All Outputs Options: Standard –1	 1.0 0.5	 1.0 0.5	ns
Maximum Skew within an Output Group	0.25	0.25	ns
Maximum Output Duty Cycle Asymmetry at 1.5V	±1.0	—	ns
Maximum TTL Input Frequency	80	80	MHz
Maximum PECL Differential Input Frequency	80	80	MHz
Maximum Rising/Falling Edge Rate	1.35/1.5	1.35/1.5	ns

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. Output symmetry follows input symmetry for the 1X outputs.
3. Asymmetry is defined as the deviation from a 50% duty cycle measured at 1.5V. Asymmetry will be affected by voltage, temperature, and load (including the length of the PC trace).
4. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
5. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "AC Test/Evaluation Circuit." Synchronous outputs may be paralleled for higher loads. The maximum rising edge rate is specified at 5.0V and must be derated at 1.4ns/V for V_{CC} <5.0V.
6. Parameters guaranteed by design and characterization or tested.

Threshold Crossing Characteristics



NOTE: Trise and Tfall are "real load" dependent. The values indicated are for 6" of board trace (70 Ohm) with a 10 pF capacitive load. See the Clock Driver Application Note.

*Applies only to divide-by-two outputs.

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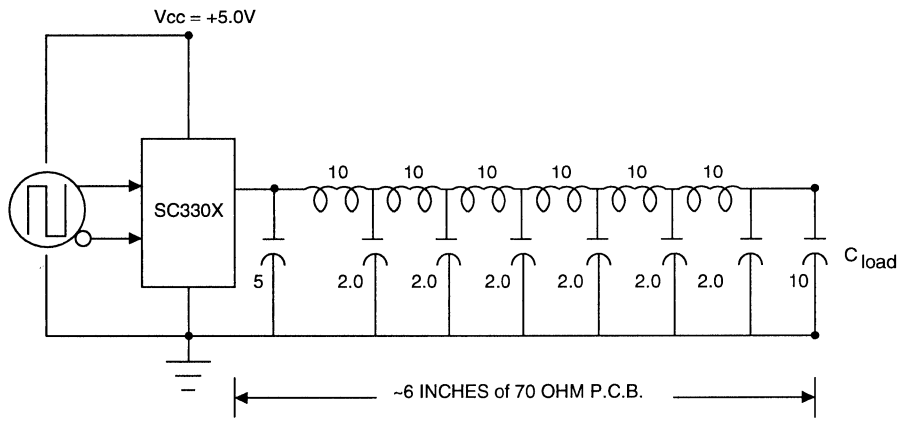
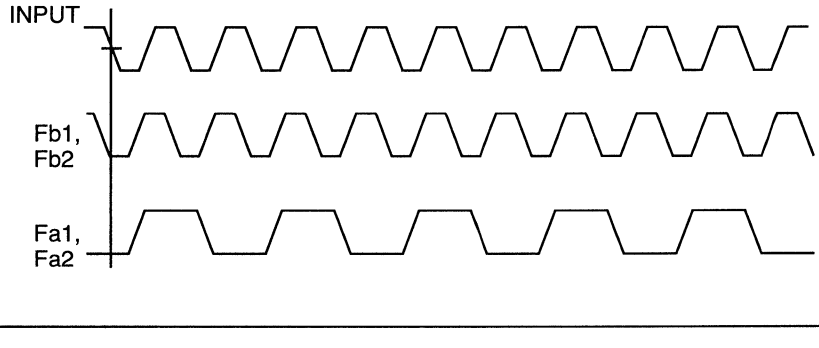
AC Test/Evaluation Circuit



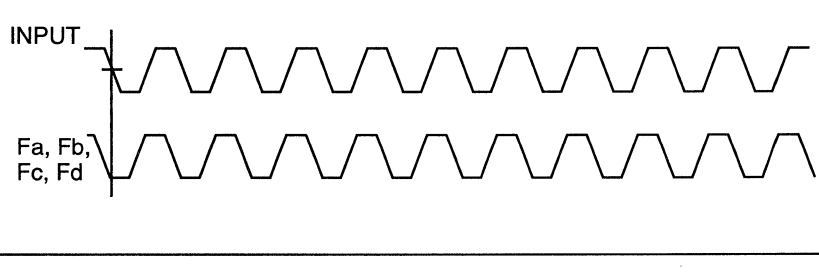
NOTES: All inductance is in nH. Capacitance is in pF.
At frequencies above 50 MHz, a single point load destination is recommended.

4

SC3306 Relative Output Timing



SC3308 Relative Output Timing



DESCRIPTION OF OPERATION
(Refer to Logic Diagram)

AMCC has developed the clock drivers using an advanced BiCMOS process. This design has been optimized for minimum skew across all twenty outputs.

For highest performance this approach requires a clock source input from a crystal-controlled oscillator (XCO) located adjacent to the clock driver. This oscillator can provide either differential ECL inputs (referenced to +5V, PECL) or TTL (CMOS) input levels to the clock driver. The input selection is accomplished via the "Clock Sel" input where a "HIGH" level activates the differential ECL input and a "LOW" activates the TTL input. This input clock will be fanned out to a toggle flip-flop or output flip-flops for synchronization, refer to Logic Diagrams. Using this methodology, the output duty cycle for the 1/2x outputs becomes largely a function of output driver slew rate into the AC load, and the duty cycle of the 1x outputs is a functions of the input clock waveshape and the output driver slew rate into the AC load.

The RESET input is provided to hold off or clear the outputs as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor (4.7uF = ~100 ms) is connected between this pin and ground, the device will respond with a "power up reset"—a delay in the clock outputs becoming active. At the onset of RESET (low) the outputs will go low following four falling-edge clock inputs. At the expiration of RESET (high) outputs will resume, after four falling-edge clock inputs, from a high (leading edge) count origin (see Figure 5, Reset To Output Timing, in the Clock Driver Application Note).

The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion resulting from simultaneous switching of the 20 outputs. These outputs also feature series termination to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50–75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance) and/or large peak voltage amplitudes, two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see the Clock Driver Application Note for Spice models).

Power and ground are interdigitated with the outputs. Of the 52 package pins, 22 are used for low impedance on-chip power distribution. Due to the simultaneously switching outputs, low impedance $+V_{CC}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see the Clock Driver Application Note for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance, and capacitance of the package and wire bonding is managed to ensure that the clock driver will exhibit skews less than the specified maximum. A plastic 52-lead quad flat pack with .039" lead pitch is employed with an outer lead square footprint of approximately 0.7" per side.

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Power Management

The overall goal of managing the power dissipated by the clock driver is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the clock driver is determined by the load that each output drives and the frequency that each output is running. The "Output Power Dissipation" table summarizes these dependencies (see "AC Test/ Evaluation Circuit", for complete load definition).

The output power must be added to the core power (600 mW) of the clock driver to determine the total power being dissipated by the clock driver. This total power is then multiplied by the clock driver's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the clock driver. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the clock driver is detailed in the 52-pin PQFP Thermal Dissipation vs. Airflow graph in the Package appendix at the end of this section.

For example: An application utilizes a clock driver with 8 Fb outputs driving 10 pF loads at 66 MHz, 3 Fa outputs driving 5 pF loads at 33 MHz and 2 Fa outputs driving 15 pF loads at 33 Mhz. Total chip power is calculated as follows:

Core Power	= 600 mW
8 Fb, 10 pF, 66 MHz = (8 x 33 mW)	= 264 mW
2 Fb, no load, 66 MHz = (2 x 11 mW)	= 22 mW
3 Fa1, 5 pF, 33 MHz = (3 x 13 mW)	= 39 mW
2 Fa1, no load, 33 MHz = (2 x 8 mW)	= 16 mW
2 Fa2, 15 pF, 33 MHz = (2 x 17 mW)	= 34 mW
3 Fa2, no load, 33 MHz = (3 x 8 mW)	= 24 mW
Total Power	= 999 mW

The design specifies a 70°C still air ambient. Referring to the 52-pin PQFP Thermal Dissipation vs. Airflow graph in the Package appendix, the Θ_{ja} for still air is 46.2°C/watt. The clock driver's junction temperature would then be:

70°C + (.999 watts x 46.2°C/watt) = 116°C

Note this is below the 140°C maximum junction temperature.

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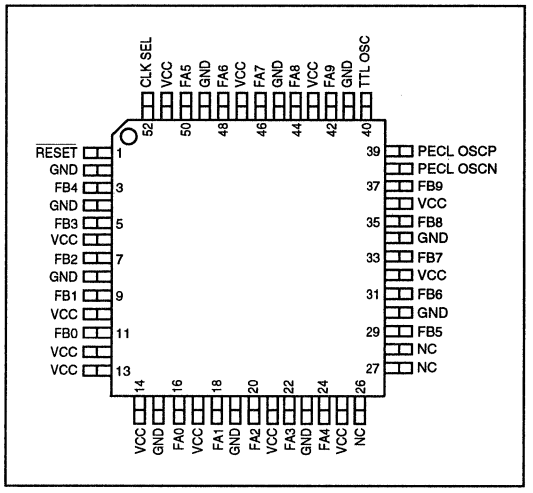
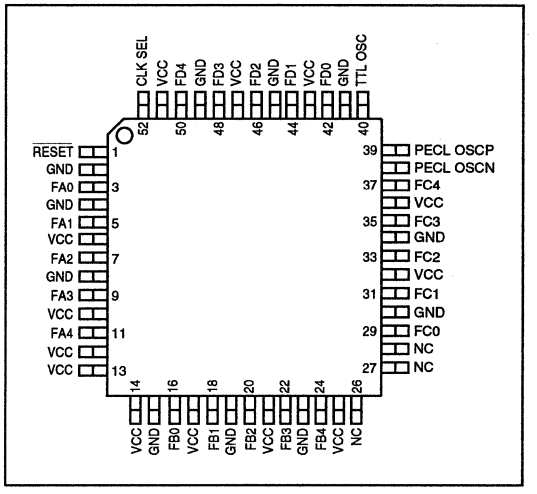
Output Power Dissipation

FREQUENCY	C_{LOAD}=5pF	C_{LOAD}=10pF	C_{LOAD}=15pF	C_{LOAD}=25pF	NO LOAD
80 MHz	29 mW	36 mW	43 mW	62 mW	13 mW
66 MHz	27 mW	33 mW	39 mW	53 mW	11 mW
50 MHz	20 mW	23 mW	27 mW	42 mW	10 mW
40 MHz	18 mW	21 mW	25 mW	36 mW	9 mW
33 MHz	13 mW	15 mW	17 mW	32 mW	8 mW
25 MHz	11 mW	13 mW	14 mW	22 mW	8 mW
20 MHz	10 mW	11 mW	13 mW	17 mW	7 mW

SC3306 Pinout



SC3308 Pinout



Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Skew Option (if applicable)**
- **Optional Shipping Configuration**

SC330X **Q** **–1** **/TD**

Optional Shipping Configuration
Blank = 84-unit matrix tray
/D = dry pack
/TD = tape, reel and dry pack

Skew Option
Blank = 1.0 ns output-output skew
–1 = 500 ps output-output skew

Package Option
Q = 52-pin Plastic Quad Flat Pack (PQFP)

Device Number

Example: SC330XQ–1/D
52-pin PQFP package, 500 ps output-output skew, shipped dry packed in the standard matrix tray.

Part Number	Standard	–1
SC3306	✔	✔
SC3308	✔	✔

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FEATURES

- **Ten or fourteen clock outputs**
  - Outputs operate at frequencies up to 80 MHz
  - Outputs grouped in two banks of five outputs on SC3318
  - Outputs grouped in a bank of three and a bank of seven outputs on the SC3327
  - Outputs grouped in a bank of six and a bank of seven outputs with a single early output on the SC3367
  - Outputs grouped in a bank of six and a bank of eight outputs on the SC3368
- **All outputs are leading-edge synchronized to within ≤0.5 ns**
- **Proprietary output drivers with:**
  - Complementary 24 mA peak outputs, source and sink
  - 50–75Ω source series termination
  - Dynamic drive adjustment to match load conditions
  - Edge rates less than 1.5 ns
- **Output levels comply with JEDEC LVTTL standard**
- **+5V V_{CC} Supply**
- **28 SOIC package**
- **Minimizes the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**

APPLICATIONS

- **Datacom and Telecom networks**
- **Compatible with PowerPC™ processors**
- **PCI Bus clock distribution**
- **Workstation and server systems with high clock fanout**
- **Compatible with Intel's Pentium™ and Pentium Pro™ processors**

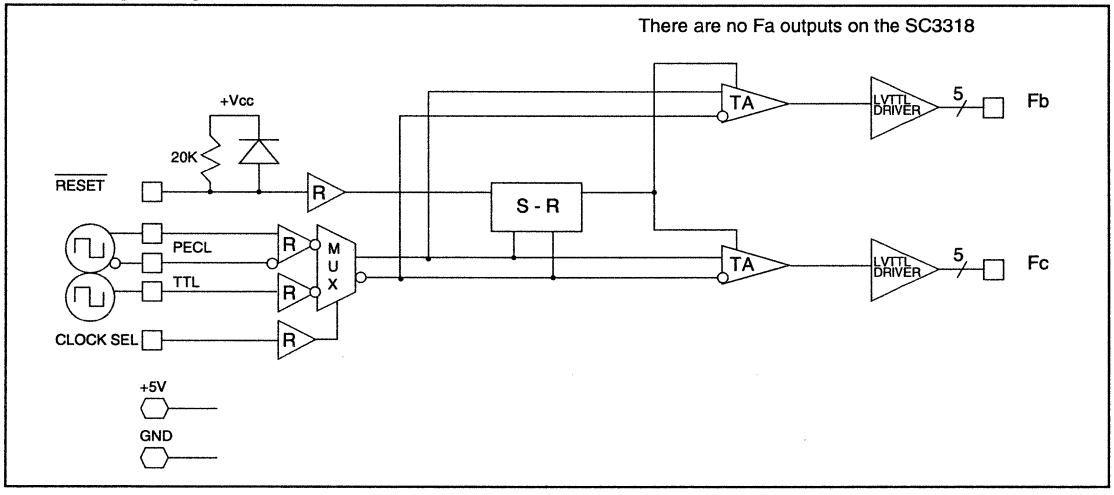
GENERAL DESCRIPTION

The SC3318, SC3327, SC3367 and SC3368 are minimum skew clock drivers with ten or fourteen outputs. They employ a clock input from a single-ended TTL or an ECL differential source operating between +5V and ground. This reference frequency input is received and distributed to the clock output drivers. All outputs are "clamped" to conform with JEDEC LVTTL levels.

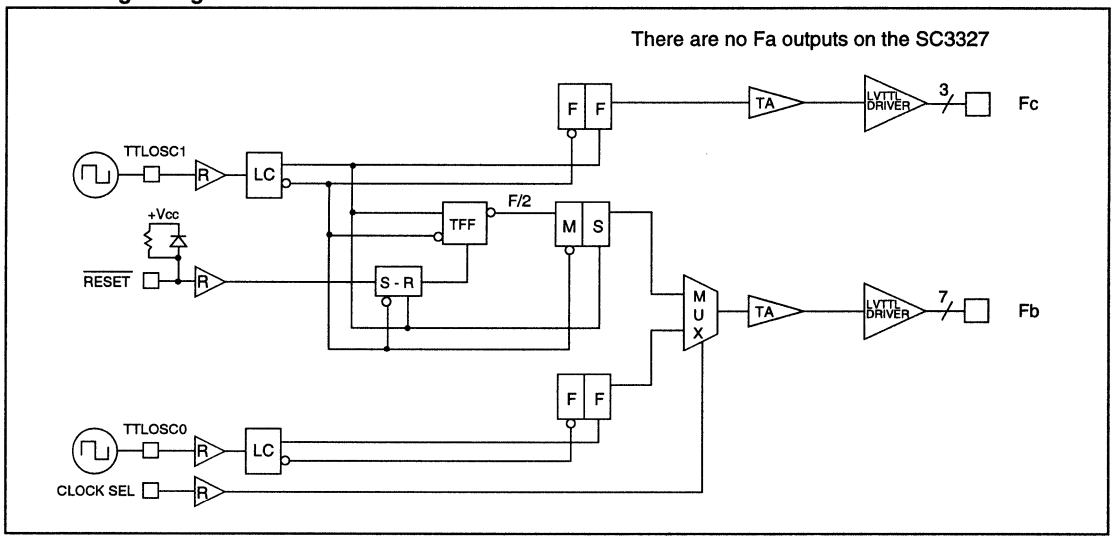
Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of ≈1.5V/ns to minimize simultaneous output-switching noise and distortion.

4

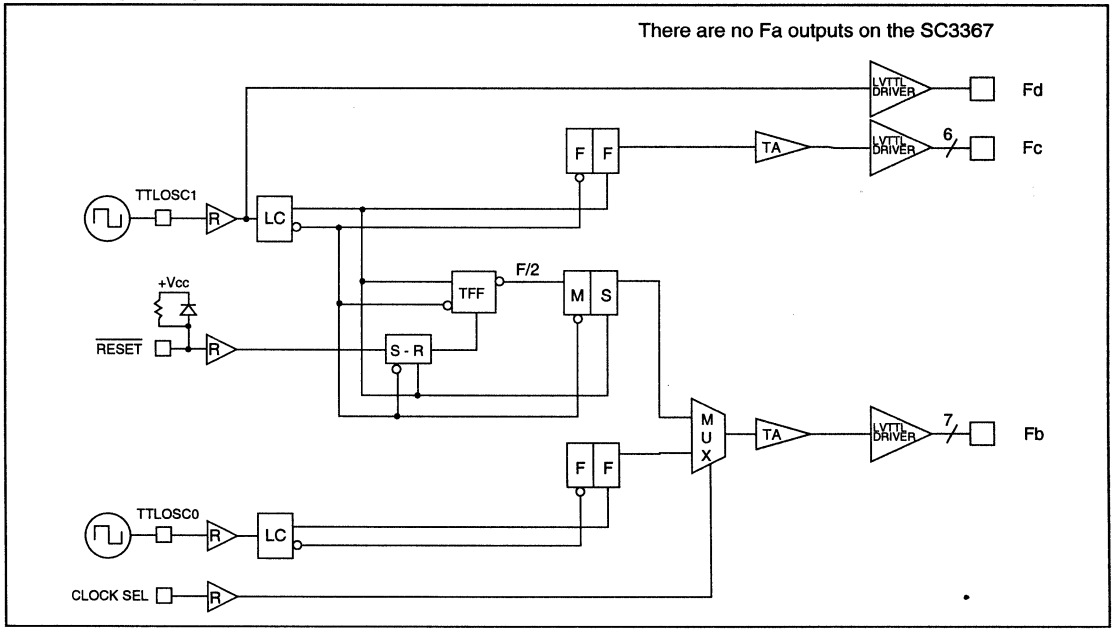
SC3318 Logic Diagram



SC3327 Logic Diagram



SC3367 Logic Diagram



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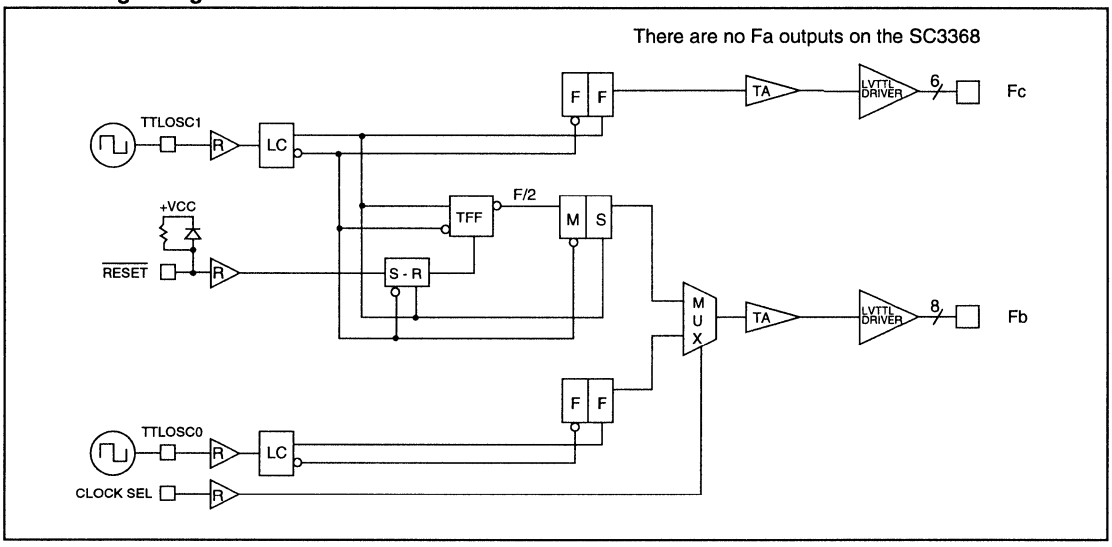
SC3368 Logic Diagram



4

SC3318/27/67/68 Product Selection Guide

	Output Frequency with Respect to Input Frequency				
P/N	**Total Outputs**	**Number of Outputs ÷ 1**	**Number of Outputs ÷ 2**	**Special Features**	**Package**
SC3318	10	10	N/A		28 SOIC
SC3327	10	3	7	Selectable single or dual clock input.	28 SOIC
SC3367	14	7	7	Selectable single or dual clock input, 1 output early.	28 SOIC
SC3368	14	6	8	Selectable single or dual clock input.	28 SOIC

Absolute Maximum Ratings

Storage Temperature ..... -55° to +150°C
V_{CC} Potential to Ground ..... -0.5V to +7.0V
Input Voltage ..... -0.5V to +V_{CC}
Static Discharge Voltage ..... >1750V
Maximum Junction Temperature ..... +140°C
Latch-up Current ..... >200 mA
Operating Ambient Temperature ..... 0° to +70°C

Capacitance (package and die total)

Input Pins ..... 5.0 pF
TTL Output Pins ..... 5.0 pF

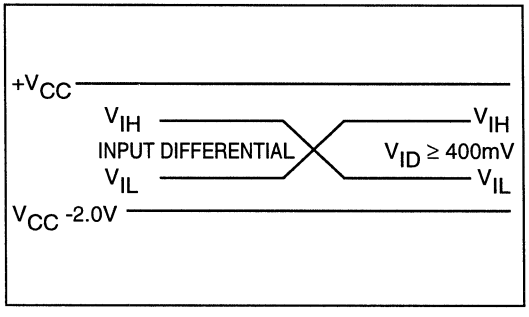
Electrical Characteristics

V_{CC} = +5.0V ± 5%, T_a = 0°C to + 70°C (reference "AC Test/Evaluation Circuit")

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Voltage (PECL)	Differential Source–PECL	V_{IL} +0.4	+V_{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage (PECL)	Differential Source–PECL	V_{CC} -2.0	V_{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I_{IH}	Input HIGH Current (PECL)	V_{IN} = V_{CC} (max)		200	uA
	CLKSEL	V_{IN} = V_{CC} (max)		350	uA
	RESET	V_{IN} = 2.4V		-200	uA
	TTL	V_{IN} = 2.4V		15	uA
I_{IL}	Input LOW Current (PECL)	V_{IN} = V_{CC} -2.0V		15	uA
	CLKSEL	V_{IN} = 0.4V		25	uA
	RESET	V_{IN} = 0.5V		-325	uA
	TTL	V_{IN} = 0.4V		15	uA
V_{OH}	Output HIGH Voltage	F_{OUT} = 80MHz, C_L = 10pF	2.3	3.65	V
V_{OL}	Output LOW Voltage	F_{OUT} = 80MHz, C_L = 10pF		0.4V	V
I_{OHS}[1]	Output HIGH Short Ckt Current	Output High, V_{OUT} = 0V Typ	-45		mA
I_{OLS}[1]	Output LOW Short Ckt Current	Output Low, V_{OUT} = V_{CC} Typ	55		mA
PWR	Static Core Power Dissipation	SC3318, 70°, Typ Pwr=340mW		550	mW
		SC3327, 70°, Typ Pwr=290mW		475	mW
		SC3367, 70°, Typ Pwr=250mW		400	mW
		SC3368, 70°, Typ Pwr=250mW		400	mW

1. Maximum test duration, one second.
2. The SC3318/27/67/68 features source series termination of approximately 40 Ohms to assist in matching 50–75 Ohm P.C. board environments.

PECL Differential Input Voltage Range



DC Characteristics

The outputs have been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high-drive, totem-pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the output will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V_{OH}	I_{OH} = -2mA	2.1V	
V_{OL}	I_{OL} = 2mA		0.6V

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AC Specifications—Using "AC Test/Evaluation Circuit"

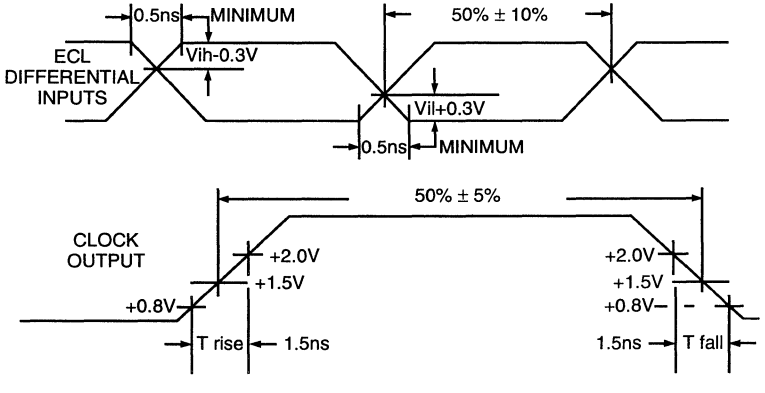
V_{CC} = +5.0V ± 5%, T_a = 0°C to 70°C, C_{LOAD} = 10pF

Parameter	SC3318	SC3327	SC3367	SC3368	Units
Maximum Skew Across Fb Outputs	250	700	500	500	ps
Maximum Skew Across Fc Outputs	250	500	250	250	ps
Maximum Skew Across Fb and Fc Outputs, CLKSEL=0			500	500	ps
Maximum Skew Across All Outputs Options: Standard –1	— 0.5				ns
Delay of Fb from Fc outputs (CLKSEL = 1) [Tdly or Tcb]	—	Min. 50 Typ. 0.9 Max 1.7	Min. 50 Typ. 0.5 Max. 1.0	Min. 50 Typ. 0.5 Max. 1.0	ps ns ns
Delay of Fc from Fd outputs [Tdc]	—		Min. 5 Typ. 6 Max. 7		ns ns ns
Maximum Output Duty Cycle Asymmetry		Min. 45% Max. 55%	Min. 45% Max. 55%	Min. 45% Max. 55%	%
Maximum TTL Input Frequency	80	80	80	80	MHz
Maximum TTL Output Frequency	80	80	80	80	MHz
Maximum PECL Differential Input Frequency	80				MHz
Maximum Rising/Falling Edge Rate	1.5	1.5	1.5	1.5	ns

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. Output Duty Cycle Asymmetry is defined as the duty cycle deviation from 50%, measured at 1.5V. Output Duty Cycle will also be affected by voltage and load (including the length of the PC trace).
3. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
4. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "AC Test/Evaluation Circuit." Synchronous outputs may be paralleled for high loads.
5. Parameters guaranteed by design and characterization or tested.

Threshold Crossing Characteristics



NOTE: Trise and Tfall are "real load" dependent. The values indicated are for 6" of board trace (70 Ohm) with a 10 pF capacitive load. See the Clock Driver Application Note.

DESCRIPTION OF OPERATION
(Refer to Logic Diagram)

AMCC has developed ten and fourteen-output clock buffer drivers using AMCC's advanced BiCMOS process. These designs have been optimized for minimum skew across all outputs.

The clock source input for these devices may operate between +5V and ground and can provide either differential ECL inputs (referenced to +5V, PECL) or single-ended TTL (CMOS) input levels to AMCC's Clock Drivers. This selection is accomplished by use of the CLKSEL pin (on the SC3318), where logic LOW (or "float") selects TTL and logic HIGH selects PECL. On the SC3327/67/68, CLKSEL chooses the source of the clock for the Fb outputs. When CLKSEL is low the TTLOSC0 input drives the Fb outputs and when CLKSEL is high a divide-by-two version of the TTLOSC1 input drives the Fb outputs. This input clock will be fanned out to translation amplifiers and output drivers, refer to the Logic Diagrams. The output duty factor asymmetry becomes largely a function of the input clock waveshape and the output driver slew rate into the AC load.

The RESET input is provided to hold off or clear the outputs, as may be required by the user's system. This pin may be logically driven from a TTL output. Optionally, if a capacitor (4.7uF = ~100ms) is connected between this pin and ground, the device will respond with a "power up reset"—a delay in the clock outputs becoming active. At the onset of RESET (low) the outputs will go low following four falling edge clock inputs (three falling edge clock inputs for the SC3327/67/68). At the expiration of RESET (high) the outputs will resume after four falling edge clock inputs (three falling edge clock inputs for the SC3327/67/68), from a high (leading edge) count origin. The reset function is only operational when CLKSEL=1.

The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion resulting from simultaneous switching of the outputs. These outputs also feature series termination (~40 Ohms) to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50 to 75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance at higher frequencies) and/or large peak voltage amplitudes, two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see the Clock Driver Application Note for spice models).

Power and ground are interdigitated with the outputs. Of the 28 package pins, 10 are used for low impedance on-chip power distribution. Due to the simultaneous switching of outputs, low impedance $+V_{CC}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see the Clock Driver Application Note for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance, and capacitance of the package and wire bonding is managed to insure that the clock drivers will exhibit skews less than the specified maximum. A plastic 28-lead small outline package with .050" lead pitch is employed with an outer lead rectangular footprint of approximately 0.7" by 0.4".

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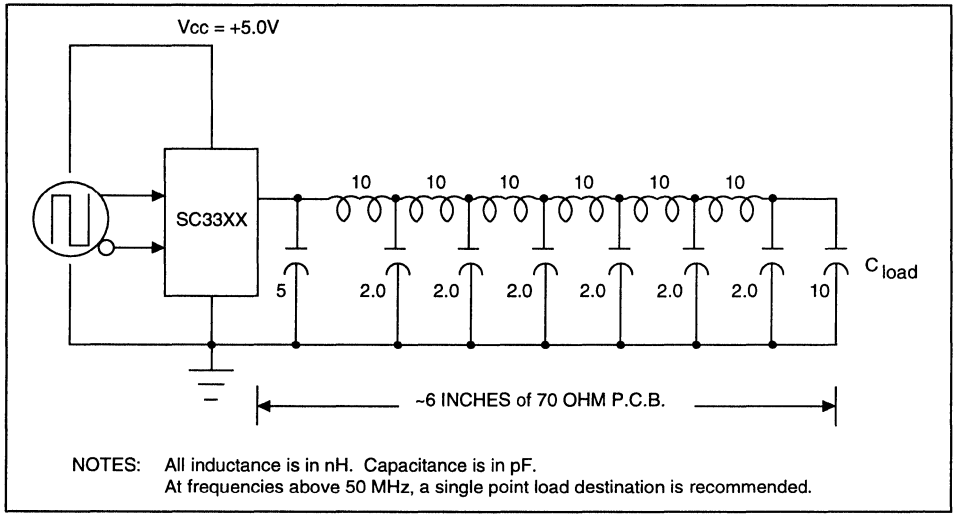
AC Test/Evaluation Circuit



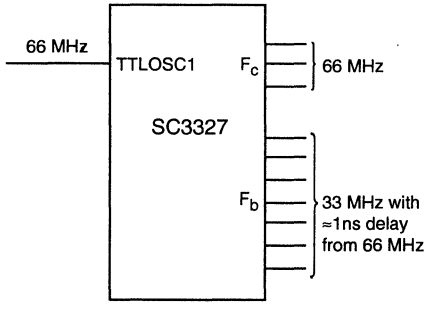
NOTES: All inductance is in nH. Capacitance is in pF.
At frequencies above 50 MHz, a single point load destination is recommended.

4

SC3327 Application Examples

Example 1.
Low Skew, Single Reference Frequency Mode

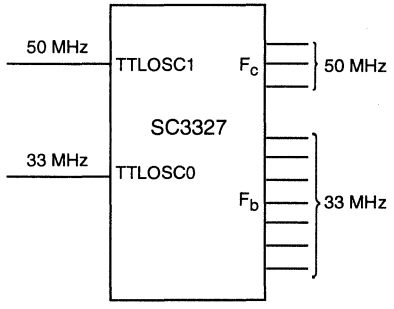
Three outputs at the primary frequency and seven outputs at half the primary frequency; each group internally synchronized. The 33 MHz outputs are delayed from the 66 MHz outputs by ≈1 ns.



CLKSEL = 1

Example 2.
Dual Reference Frequency Mode, Asynchronous

Three outputs at the primary frequency and seven outputs at the secondary frequency with ≈1 ns internal delay at the F_b outputs.

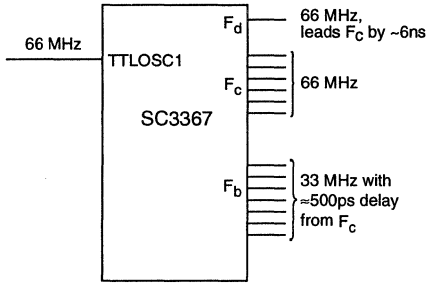


CLKSEL = 0

SC3367 Application Examples

Example 1.
Low Skew, Single Reference Frequency Mode

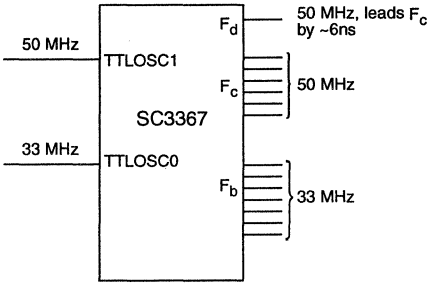
Seven outputs at the primary frequency and seven outputs at half the primary frequency; each group internally synchronized. The 33 MHz outputs are delayed from the 66 MHz outputs by ≈500 ps. F_d will lead F_c by ~6 ns.



CLKSEL = 1

Example 2.
Dual Reference Frequency Mode, Asynchronous

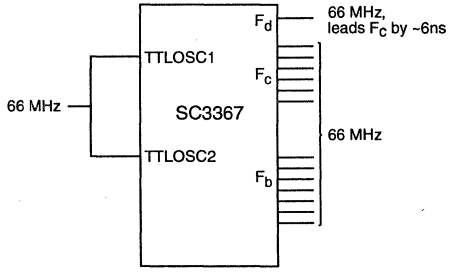
Seven outputs at the primary frequency and eight outputs at the secondary frequency. F_d will lead F_c by ~6 ns.



CLKSEL = 0

Example 3.
Single Reference Frequency Mode, Synchronous

Thirteen outputs will follow the input reference with a maximum skew of 500 ps across all outputs. F_d will lead F_c by ~6 ns.



CLKSEL = 0

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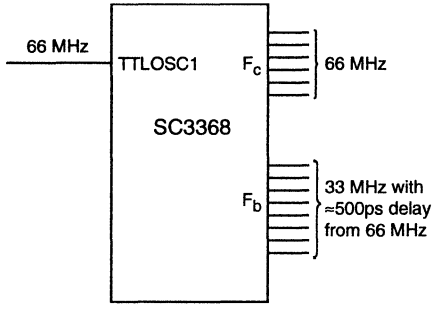
SC3368 Application Examples

Example 1.
Low Skew, Single Reference Frequency Mode

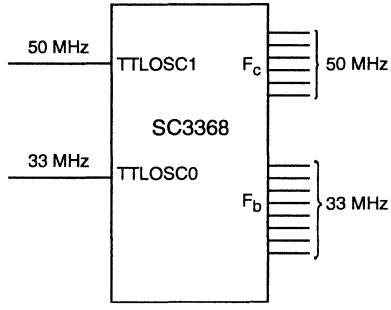
Six outputs at the primary frequency and eight outputs at half the primary frequency; each group internally synchronized. The 33 MHz outputs are delayed from the 66 MHz outputs by ≈500 ps.



CLKSEL = 1

Example 2.
Dual Reference Frequency Mode, Asynchronous

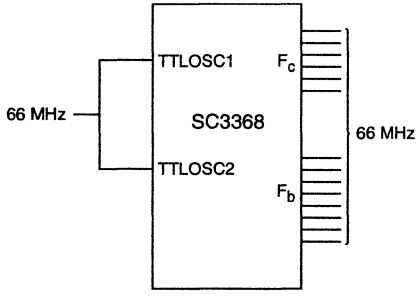
Six outputs at the primary frequency and eight outputs at the secondary frequency.



CLKSEL = 0

Example 3.
Single Reference Frequency Mode, Synchronous

All fourteen outputs will follow the input reference with a maximum skew of 500 ps across all outputs.



CLKSEL = 0

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Power Management

The overall goal of managing the power dissipated by the clock driver is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the clock driver is determined by the load that each output drives and the frequency that each output is running. The "Output Power Dissipation" table summarizes these dependencies (see "AC Test/ Evaluation Circuit", for complete load definition).

The output power must be added to the core power (550 mW) of the clock driver to determine the total power being dissipated by the clock driver. This total power is then multiplied by the clock driver's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the clock driver. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the clock driver is detailed in the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix at the end of this section.

For example: An application utilizes an clock driver with 8 outputs driving 10 pF loads at 66 MHz. Total chip power is calculated as follows:

Core Power (SC3318) = 550 mW

8 outputs, 10 pF, 66 MHz = (8 x 33 mW) = 264 mW
2 outputs, no load, 66 MHz = (2 x 11 mW) = 22 mW

Total Power = 836 mW

The design specifies a 70˚C still air ambient. Referring to the 28-pin SOIC Thermal Dissipation vs. Airflow graph in the Package appendix, the Θ_{ja} for still air is 57.7˚C/watt. The clock driver's junction temperature would then be:

70˚C + (0.836 watts x 57.7˚C/watt) = 118˚C

Note this is below the 140˚C maximum junction temperature.

Output Power Dissipation

FREQUENCY	C_{LOAD}=5pF	C_{LOAD}=10pF	C_{LOAD}=15pF	C_{LOAD}=25pF	NO LOAD
80 MHz	29 mW	36 mW	43 mW	62 mW	13 mW
66 MHz	27 mW	33 mW	39 mW	53 mW	11 mW
50 MHz	20 mW	23 mW	27 mW	42 mW	10 mW
40 MHz	18 mW	21 mW	25 mW	36 mW	9 mW
33 MHz	13 mW	15 mW	17 mW	32 mW	8 mW
25 MHz	11 mW	13 mW	14 mW	22 mW	8 mW
20 MHz	10 mW	11 mW	13 mW	17 mW	7 mW

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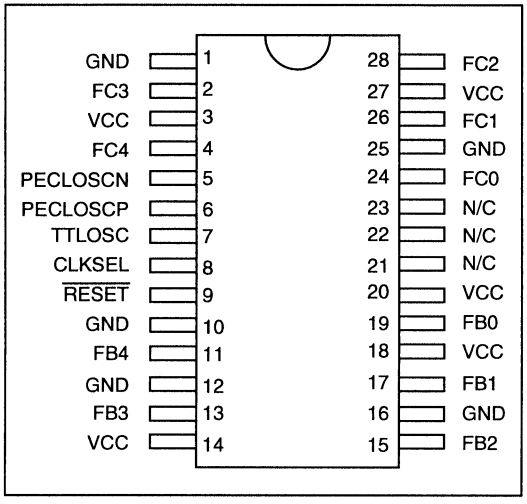
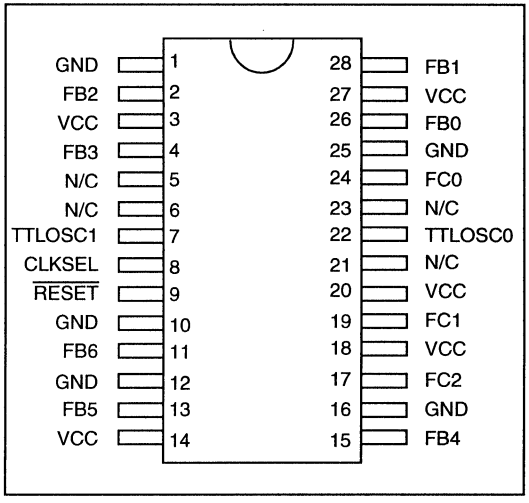
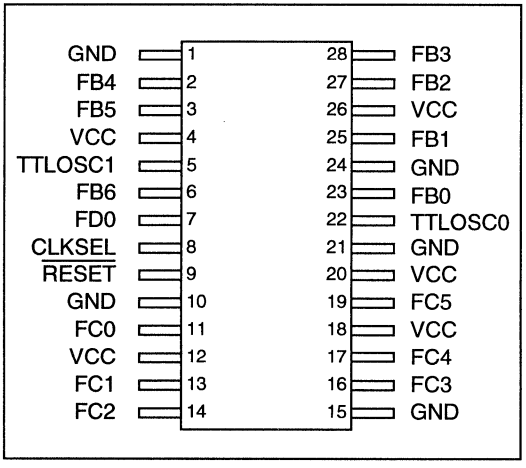
SC3318 Pinout



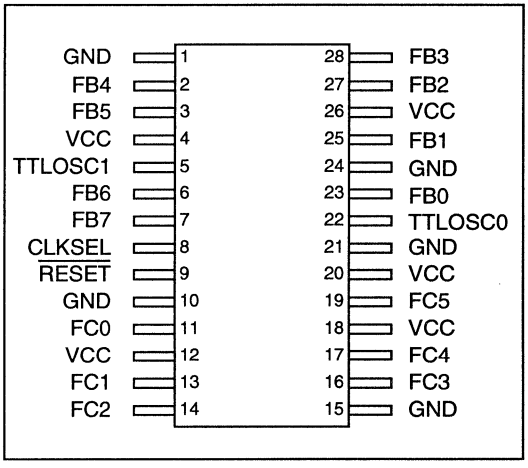
SC3327 Pinout



SC3367 Pinout



SC3368 Pinout



Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Skew Option (if applicable)**
- **Optional Shipping Configuration**

SC33XX **S** **–1** **/TD**

Optional Shipping Configuration
Blank = 25-unit tube
/D = dry pack
/T = tape, reel and dry pack

Skew Option
Blank = standard output-output skew
– 1 = 500 ps output-output skew

Package Option
S = 28-pin Small Outline Integrated Circuit (SOIC)

Device Number

Example: SC33XXS–1/D
28-pin SOIC package, 500 ps output-output skew, shipped dry packed in the standard tube.

Part Number	Standard	–1
SC3318	N/A	✔
SC3327	✔	N/A
SC3367	✔	N/A
SC3368	✔	N/A

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CONTENTS

3.3V CLOCK DRIVERS

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10, 14 AND 20-OUTPUT LVTTL CLOCK DRIVERS S3LV306/08/18/68

FEATURES

- **Ten, fourteen or twenty clock outputs:**
  - Outputs operate at primary frequency up to 100 MHz
  - Outputs grouped into four banks of five outputs on the S3LV306/08
  - Outputs grouped into two banks of five outputs on the S3LV318
  - Outputs grouped into one bank of six outputs and one bank of eight outputs on the S3LV368
- **All outputs are leading edge synchronized to within 350ps**
- **Proprietary output drivers with:**
  - Complementary 24 mA peak outputs, source and sink
  - 50–75Ω source series termination
  - Dynamic drive adjustment to match load conditions
  - Edge rates less than 1.5 ns
- **Output levels comply with JEDEC LVTTL standard**
- **+3.3V V_{CC}**
- **Minimizes the ground-bounce, overshoot, and ringing problems often encountered when using CMOS and Bipolar drivers**

APPLICATIONS

- **Compatible with Intel's Pentium™ and Pentium Pro™ processors, and PowerPC processors**
- **PCI Bus clock distribution**
- **Workstation and server systems with high clock fanout**
- **Datacom and Telecom networks**

GENERAL DESCRIPTION

The S3LV306, S3LV308, S3LV318, and S3LV368 are precision low skew clock drivers with 10, 14, or 20 outputs. They employ a clock input from a single-ended TTL or an ECL differential source operating between +3.3V and ground (PECL). This reference frequency input is received and distributed to symmetrical, divide-by-two, master-slave flip-flops. The resultant output is distributed to the clock output drivers. All outputs conform with JEDEC LVTTL levels.

The 20 outputs are divided into groups: some groups operate at the primary frequency, equal to the input; some groups may operate at one half of the primary input frequency.

Applied Micro Circuits Corporation (AMCC) uses proprietary complementary (source and sink) 24 mA peak output drivers. In addition to their drive capability, these circuits provide "source (series) termination" at the TTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of ≈1.5V/ns to minimize simultaneous output-switching noise and distortion.

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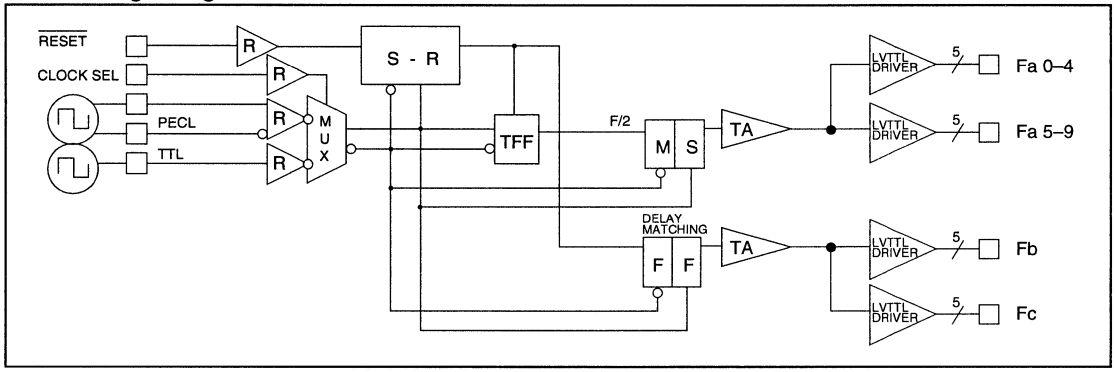
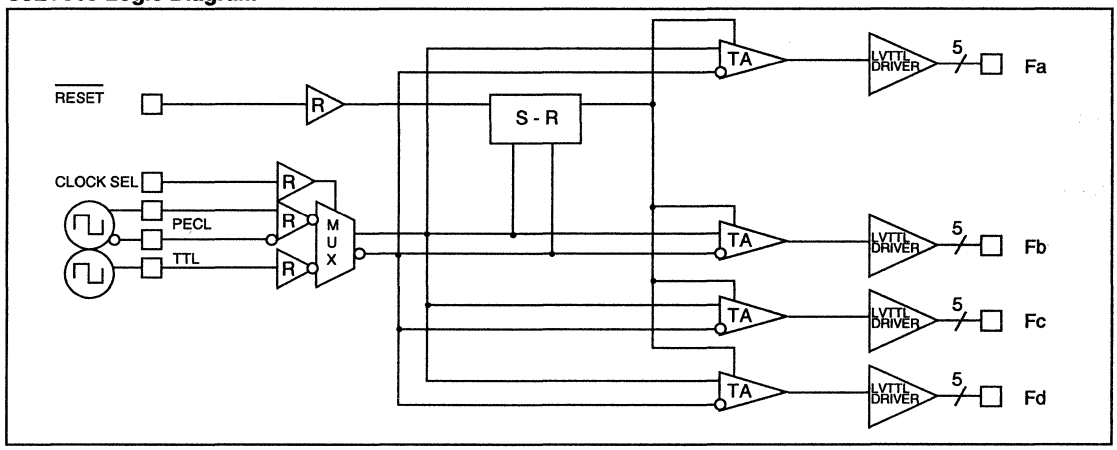
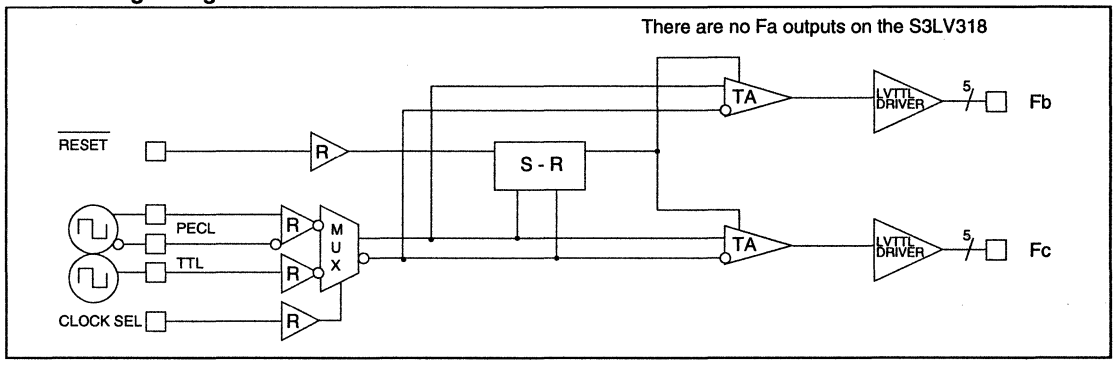
S3LV306 Logic Diagram



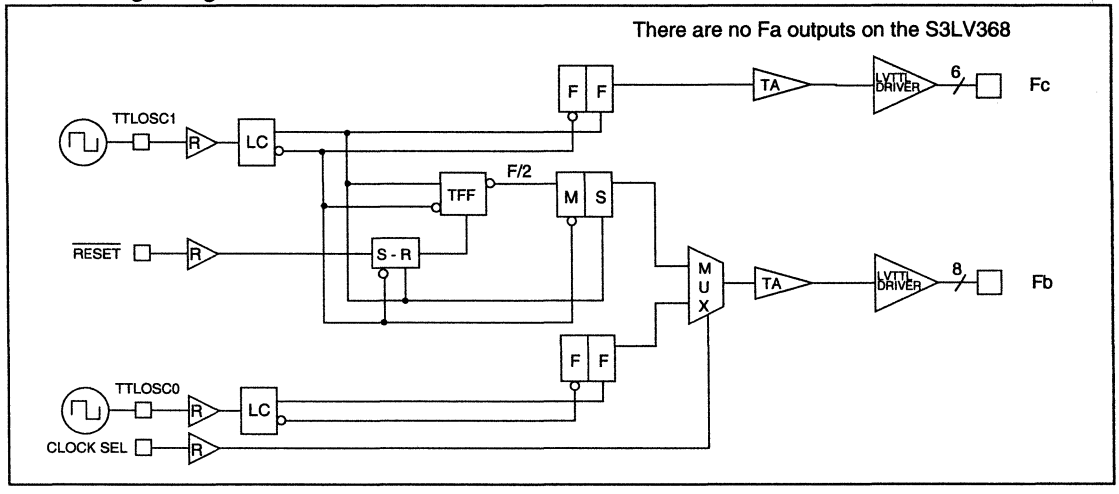
S3LV308 Logic Diagram



S3LV318 Logic Diagram



S3LV368 Logic Diagram



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Absolute Maximum Ratings

Storage Temperature ..... -55° to +150°C
V_{CC} Potential to Ground ..... -0.5V to +4.6V
Input Voltage ..... -0.5V to +V_{CC} +0.5
Static Discharge Voltage ..... >1750V
Maximum Junction Temperature ..... +140°C
Latch-up Current ..... >200 mA
Operating Ambient Temperature ..... 0° to +70°C

Capacitance (package and die total)

Input Pins ..... 5.0 pF
TTL Output Pins ..... 5.0 pF

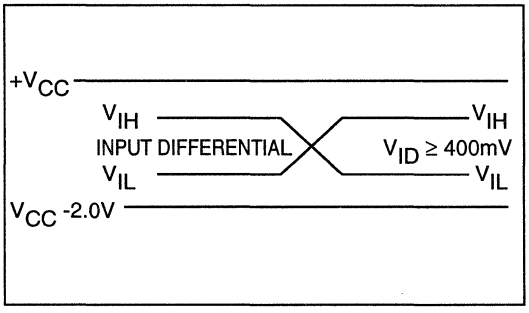
Electrical Characteristics

V_{CC} = 3.3V ±0.3V, T_a = 0°C to + 70°C (reference "AC Test/Evaluation Circuit")

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Voltage (PECL)	Differential Source–PECL	V_{IL} +0.4	V_{CC}	V
	Input HIGH Voltage (TTL)	All TTL Inputs	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage (PECL)	Differential Source–PECL	V_{CC} -2.0	V_{IH} -0.4	V
	Input LOW Voltage (TTL)	All TTL Inputs	-0.5	0.8	V
I_{IH}	Input HIGH Current (PECL)	V_{IN} = V_{CC} (max)		200	uA
	TTL	V_{IN} = 2.4V		15	uA
I_{IL}	Input LOW Current (PECL)	V_{IN} = V_{CC} -2.0V		15	uA
	TTL	V_{IN} = 0.4V		15	uA
V_{OH}	Output HIGH Voltage	F_{OUT} = 100MHz, C_L = 10pF	2.4	V_{CC} +0.3V	V
V_{OL}	Output LOW Voltage	F_{OUT} = 100MHz, C_L = 10pF		0.4V	V
I_{OHS}[1]	Output HIGH Short Ckt Current	Output High, V_{OUT} = 0V Typ	-55		mA
I_{OLS}[1]	Output LOW Short Ckt Current	Output Low, V_{OUT} = V_{CC} Typ	55		mA
PWR	Static Core Power Dissipation	S3LV306, 70°C, Typ Pwr 275 mW		450	mW
		S3LV308, 70°C, Typ Pwr 275 mW		450	mW
		S3LV318, 70°C, Typ Pwr 275 mW		450	mW
		S3LV368, 70°C, Typ Pwr 250 mW		400	mW

1. Maximum test duration, one second.
2. The S3LV306/08/18/68 features source series termination of approximately 40 Ohms to assist in matching 50–75 Ohm P.C. board environments.

PECL Differential Input Voltage Range



DC Characteristics

The outputs have been designed specifically for clock distribution. In the development of this product, AMCC has made several trade-offs between the historic "high-drive, totem-pole outputs" and AMCC's dynamically adjusting source series terminated outputs. As a result of this, the outputs will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V_{OH}	I_{OH} = -2mA	2.4V	
V_{OL}	I_{OL} = 2mA		0.4V

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AC Specifications—Using "AC Test/Evaluation Circuit"

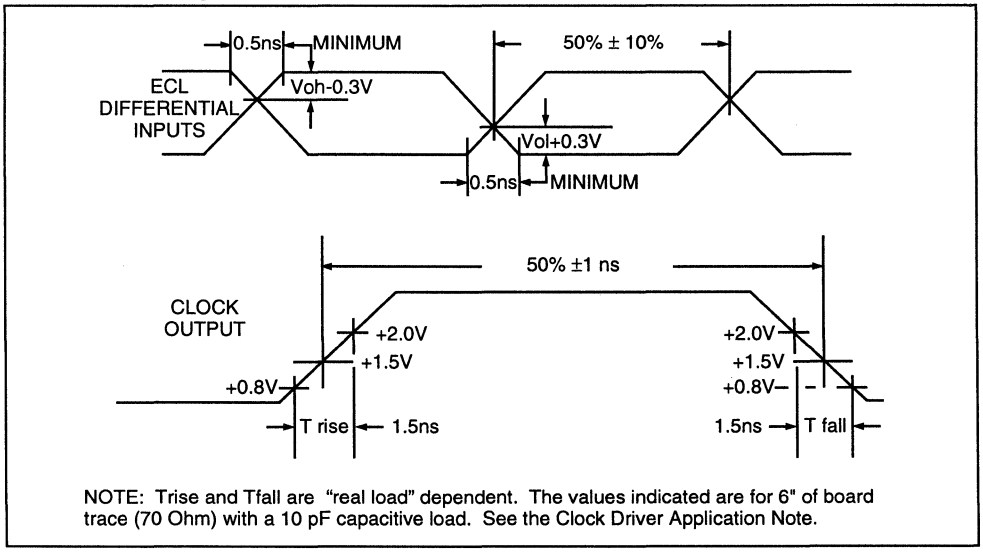
V_{CC} = 3.3V ± 0.3V, Ta = 0°C to +70°C, C_{LOAD} = 10pF

Parameter	S3LV306	S3LV308	S3LV318	S3LV368	Units
Maximum Skew Across Fb and Fc Outputs, CLKSEL=0				350	ps
Maximum Skew within an Output Group	250	250	250	250	ps
Maximum Skew Across All Outputs Options: Standard –1	 350	 350	 350		 ps
Delay of Fb from Fc outputs (CLKSEL = 1) [Tdly]				Min. 50 Typ. 500 Max. 1.0	ps ps ns
Maximum Output Duty Cycle Asymmetry	±1.0 ns	±1.0 ns	±1.0 ns	±1.0 ns	ns
Maximum TTL Input Frequency	100	100	100	100	MHz
Maximum TTL Output Frequency	100	100	100	100	MHz
Maximum PECL Differential Input Frequency	100	100	100		MHz
Maximum Rising/Falling Edge Rate	1.5	1.5	1.5	1.5	ns

Notes:

1. Skew is referenced to the rising edges of all outputs.
2. Output asymmetry applies to 1X and 1/2X outputs.
3. Asymmetry is defined as the deviation from a 50% duty cycle measured at 1.5V. Asymmetry will be affected by voltage, temperature, and load (including the length of the PC trace).
4. Typical skew derating factor for different loads is 50ps/pF at 1.5V threshold. For example, a 5pF load difference equals a 250 ps skew difference.
5. Edge rates are measured from 0.8V to 2.0V. Load consists of a 6" board trace (70 Ohm) with a 10 pF capacitive load. See "AC Test/Evaluation Circuit." Synchronous outputs may be paralleled for higher loads.
6. Parameters guaranteed by design and characterization or tested.

Threshold Crossing Characteristics



NOTE: Trise and Tfall are "real load" dependent. The values indicated are for 6" of board trace (70 Ohm) with a 10 pF capacitive load. See the Clock Driver Application Note.

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DESCRIPTION OF OPERATION
(Refer to Logic Diagram)

AMCC has developed a twenty-output fan-out device using an advanced BiCMOS process. This design has been optimized for clock symmetry and absolute minimum skew across all twenty outputs. Two harmonic clock frequency groups are provided.

For highest performance this approach requires a clock source input from a crystal-controlled oscillator (XCO) located adjacent to the clock drivers (S3LV306/08/18). This oscillator can provide either differential ECL inputs (referenced to +3.3V, PECL) or TTL (CMOS) input levels to the clock driver. The input selection is accomplished via the "Clock Sel" input where a "HIGH" level activates the differential ECL input and a "LOW" activates the TTL input. This input clock will be fanned out to a toggle flip-flop and/or to output flip-flops for synchronization. (Refer to the Logic Diagrams.) Using this methodology, the output duty cycle for the F/2 groups becomes largely a function of output driver slew rate into the AC load, and for F groups is determined by the input clock waveshape and the output driver slew rate into the AC load.

The clock source for the S3LV368 can be one or two TTL (CMOS) input clocks. This selection is accomplished by use of the CLKSEL pin, where logic LOW selects the dual reference frequency mode, and logic HIGH selects the single reference frequency mode (refer to the Application Examples).

The RESET input is provided to hold off or clear the outputs as may be required by the user's system. This pin may be logically driven from a TTL output. At the onset of RESET (low) the outputs will go low following four falling-edge clock inputs. At the expiration of RESET (high) outputs will resume, after four falling-edge clock inputs, from a high (leading edge) count origin (see Figure 5, Reset To Output Timing, in the Clock Driver Application Note).

The output drivers are rise and fall slew rate controlled to ~1.5V/ns to minimize noise and distortion resulting from simultaneous switching of the 20 outputs. These outputs also feature series termination to significantly reduce the overshoot and undershoot of non-terminated transmission lines. This will satisfy printed circuit line impedances of 50–75 Ohms terminated into 15 pF (two IC input package receiver pins). When applications require large load capacitance (>25pF with 50 Ohm P.C. board impedance) and/or large peak voltage amplitudes, two adjacent drivers may be paralleled, thereby halving the series resistance and doubling the peak current (see the Clock Driver Application Note for Spice models).

Power and ground are interdigitated with the outputs. Of the 52 package pins, 22 are used for low impedance on-chip power distribution. Due to the simultaneously switching outputs, low impedance $+V_{CC}$ and ground planes within the P.C. board are recommended, as well as substantial decoupling capacitance (see the Clock Driver Application Note #1 for recommendations).

The IC package and die layouts are tightly coupled to assure precise matching of all of the outputs. Collectively, the resistance, inductance, and capacitance of the package and wire bonding is managed to insure that the clock drivers will exhibit skews less than the specified maximum. A plastic 52-lead quad flat pack with .039" lead pitch is employed with an outer lead square footprint of approximately 0.7" per side.

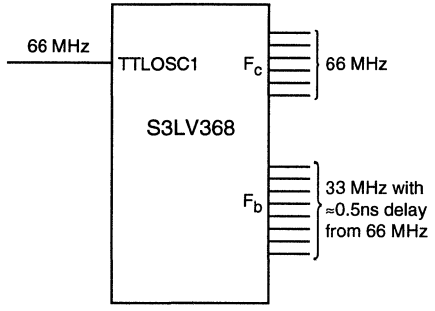
S3LV306/08/18/68 Product Selection Guide

	Output Frequency with Respect to Input Frequency				
P/N	Total Outputs	Number of Outputs ÷ 1	Number of Outputs ÷ 2	Special Features	Package
S3LV306	20	10	10		52 PQFP
S3LV308	20	20	N/A		52 PQFP
S3LV318	10	10	N/A		28 SOIC
S3LV368	14	6	8	Selectable single or dual clock input.	28 SOIC

S3LV368 Application Examples

Example 1.
Low Skew, Single Reference Frequency Mode

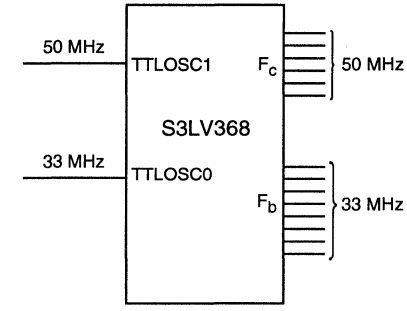
Six outputs at the primary frequency and eight outputs at half the primary frequency; each group internally synchronized. The 33 MHz outputs are delayed from the 66 MHz outputs by ≈0.5ns.



CLKSEL = 1

Example 2.
Dual Reference Frequency Mode, Asynchronous

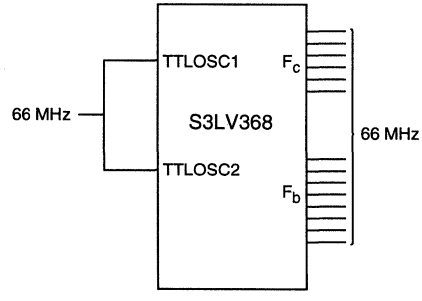
Six outputs at the primary frequency and eight outputs at the secondary frequency.



CLKSEL = 0

Example 3.
Single Reference Frequency Mode, Synchronous

All fourteen outputs will follow the input reference with a maximum skew of 350 ps across all outputs.



CLKSEL = 0

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Power Management

The overall goal of managing the power dissipated by the clock driver is to limit its junction (die) temperature to 140°C. A major component of the power dissipated internally by the clock driver is determined by the load that each output drives and the frequency that each output is running. The "Output Power Dissipation" table summarizes these dependencies (see "AC Test/Evaluation Circuit", for complete load definition).

The output power must be added to the core power (450 mW) of the clock driver to determine the total power being dissipated by the clock driver. This total power is then multiplied by the clock driver's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the clock driver. For greatest reliability, this junction temperature should not exceed 140°C. The thermal resistance for the clock driver is detailed in the 52-pin PQFP Thermal Dissipation vs. Airflow graph in the Package appendix at the end of this section.

For example: An application utilizes an clock driver with 8 Fb outputs driving 10 pF loads at 66 MHz, 3 Fa outputs driving 5 pF loads at 33 MHz and 2 Fa outputs driving 15 pF loads at 33 Mhz. Total chip power is calculated as follows:

Core Power (S3LV306)	= 450 mW
8 Fb, 10 pF, 66 MHz = (8 x 33 mW)	= 376 mW
2 Fb, no load, 66 MHz = (2 x 11 mW)	= 22 mW
3 Fa1, 5 pF, 33 MHz = (3 x 13 mW)	= 39 mW
2 Fa1, no load, 33 MHz = (2 x 8 mW)	= 16 mW
2 Fa2, 15 pF, 33 MHz = (2 x 17 mW)	= 34 mW
3 Fa2, no load, 33 MHz = (3 x 8 mW)	= 24 mW
Total Power	= 961 mW

The design specifies a 70°C still air ambient. Referring to the 52-pin PQFP Thermal Dissipation vs. Airflow graph in the Package appendix, the Θ_{ja} for still air is 46.2°C/watt. The clock driver's junction temperature would then be:

70°C + (.961 watts x 46.2°C/watt) = 114°C

Note this is below the 140°C maximum junction temperature.

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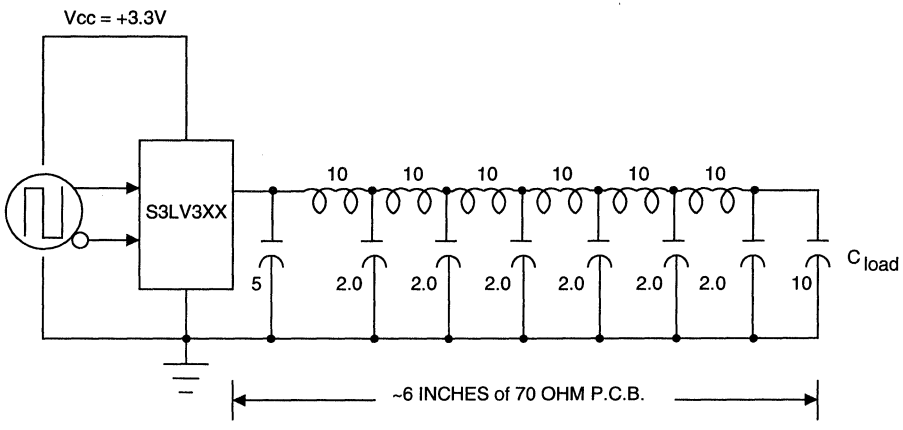
Output Power Dissipation

FREQUENCY	C_{LOAD}=5pF	C_{LOAD}=10pF	C_{LOAD}=15pF	C_{LOAD}=25pF	NO LOAD
100 MHz	33 mW	39 mW	47 mW	70 mW	15 mW
80 MHz	29 mW	36 mW	43 mW	62 mW	13 mW
66 MHz	27 mW	33 mW	39 mW	53 mW	11 mW
50 MHz	20 mW	23 mW	27 mW	42 mW	10 mW
40 MHz	18 mW	21 mW	25 mW	36 mW	9 mW
33 MHz	13 mW	15 mW	17 mW	32 mW	8 mW
25 MHz	11 mW	13 mW	14 mW	22 mW	8 mW
20 MHz	10 mW	11 mW	13 mW	17 mW	7 mW

AC Test/Evaluation Circuit



NOTES: All inductance is in nH. Capacitance is in pF.
At frequencies above 50 MHz, a single point load destination is recommended.

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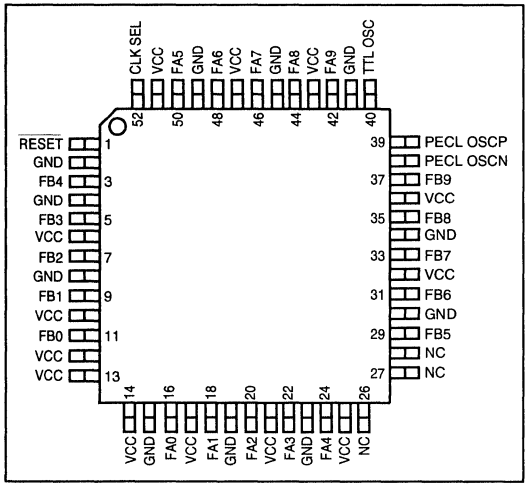
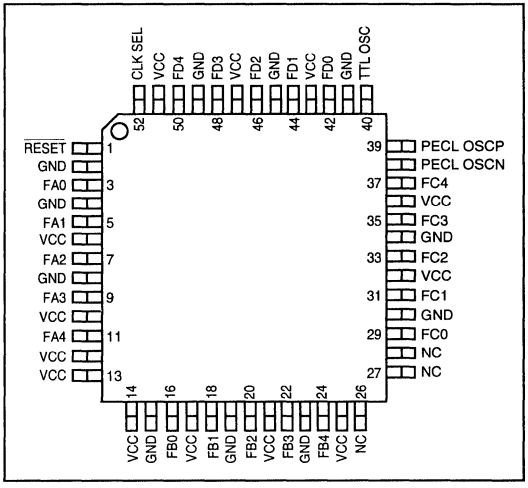
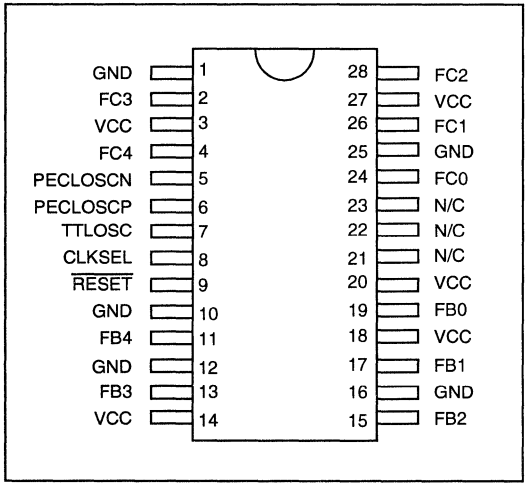
S3LV306 Pinout



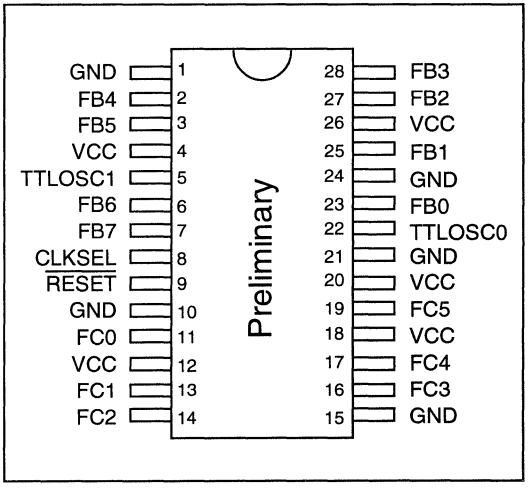
S3LV308 Pinout



S3LV318 Pinout



S3LV368 Pinout

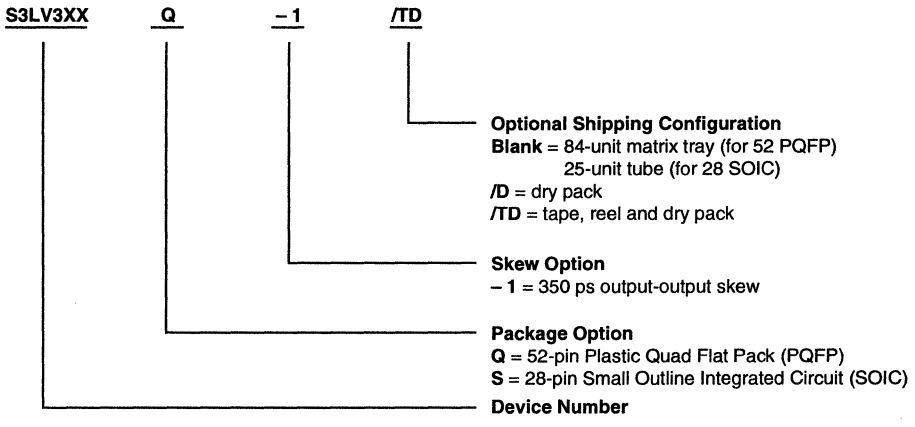


5

Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Skew Option (if applicable)**
- **Optional Shipping Configuration**



Example: S3LV3XXQ–1/D
52-pin PQFP package, 500 ps output-output skew,
shipped dry packed in the standard matrix tray.

Part Number	Standard	–1
S3LV306	✔	✔
S3LV308	✔	✔
S3LV318	✔	✔
S3LV368	Contact AMCC	

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The SC35XX Family of Clock Drivers have been designed to provide single chip solutions which ease clock distribution for TTL/CMOS I/O compatible microprocessor based systems.

All products have a generous supply (10 or 20) of the various derived frequency outputs to avoid overloading any one output. The outputs may also be used in parallel for driving particularly heavy loads. The availability of numerous clock outputs reduces the need to "daisy chain" or "branch" loads. The end benefit to the user is reduced clock skew with a high quality received wave form. By virtue of this single chip providing clock shape, clock edge alignment and clock fanout, the system designer's task is reduced to providing load balance and careful PC board layout.

The "Appnote" describes and discusses:

- Frequency Sources
- Skew Management
- Clock Waveform Signal Integrity
- Chip Power Estimations
- High Capacitance Loads
- Output Symmetry Compensation
- Reset Control and Timing
- Use of Multiple Clock Chips in a System-Primary and Secondary Distribution

FREQUENCY SOURCE

It is suggested that the basic Frequency Source be a low cost crystal-controlled oscillator (XCO). Frequency tolerance and stability are offered from 0.05% (500PPM) to 0.001% (10PPM), with 0.01% (100PPM) being readily available at competitive prices. These crystal oscillators should be acceptable over most operating temperature ranges. Only with large temperature fluctuations during operation would the higher priced temperature compensated crystal oscillator (TCXO) be suggested. TTL output devices are available up to 100 MHz with ECL output devices spanning the entire range of interest, from 30 to 200 MHz.

An appended list of domestic sources for these oscillators, including phone numbers is provided. While this list is not all inclusive, it will provide an initial reference (See Appendix A).

NOTE: The SC35XX PECL (Positive 5 -Volt ECL) Inputs are designed to interface with an ECL output oscillator operating at ground to +5.0 Volts. The oscillator's complementary emitter follower outputs may be "self-terminated" within the package by 200 to 500 Ohm pull down resistors to ground (-Vee) or they may be terminated discretely via resistors on the PC board. The oscillator should be placed close (<3") to the SC35XX driver.

CLOCK SKEW MANAGEMENT

The SC35XX has been designed to reduce the system level Clock Skew Management task to two basic design issues.

1) Balancing clock trace delays

Balancing clock trace delays requires the use of equal lengths of microstrip and stripline traces on each clock line

"Microstrip," which is a single surface conductor over a distributed ground or power plane, has a nominal propagation delay of approximately 150 pS per inch (see Figure 1).

"Stripline," which is a buried conductor sandwiched between two ground or power planes, has a nominal propagation delay of approximately 200 pS per inch.

To match clock trace lengths, when the receiving devices are differing "Manhattan" distances from the SC35XX drive, the PC trace must be lengthened to the closer loads. This can be accomplished by forming a "serpentine" path (Figure 2).

2) Matching the end-of-line load capacitance

Variations in the end-of-line lumped-load capacitance will increase or decrease the clock signal's rise and fall time. These changes will be approximately 0.5 ns per 10 pF over the range of 10 to 40 pF. Be sure to verify the receiving input package capacitance of all clock receptors. Typically, plastic flat packs have the lowest input pin capacitance and ceramic pin grid arrays (PGAs) have the highest. PGAs also have the disadvantage that their plated thru holes can add significant capacitance (up to 10 pF or more). This should be checked with a capacitance meter.

Figure 1

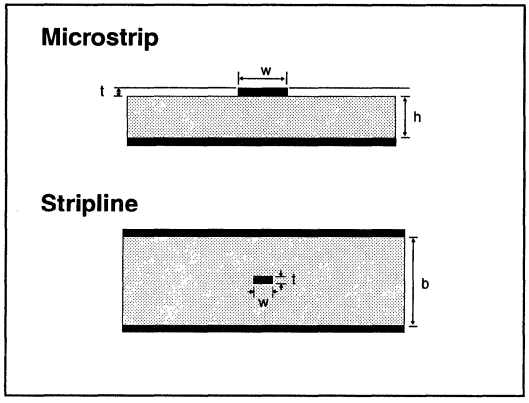
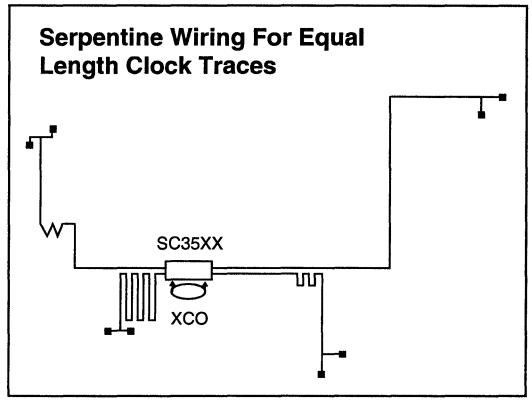


Figure 2



CLOCK WAVEFORM SIGNAL INTEGRITY

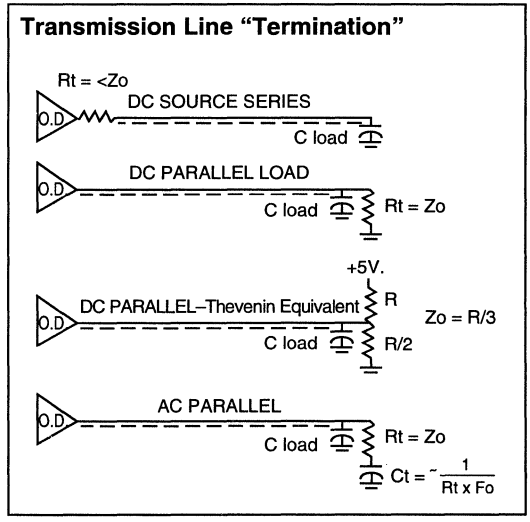
Clock waveform signal integrity refers to the control of noise margin and receiver threshold crossing distortions. DC margins for TTL I/O levels are often secondary when operating frequencies exceed 25 MHz. This is due to the overriding effects of "overshoot/undershoot" (i.e., ringing) or poorly terminated transmission lines causing reflections on the clock traces.

The effect of these reflections can be the presence of half or partial amplitude steps in the clock waveform appearing at intermediate "branched" or "daisy chained" load points. These partial amplitude steps can cause spurious triggering at these intermediate load points.

The TTL/CMOS clock output driver must provide a reasonably square voltage waveform from +0.5 to +3.5 Volts, as a minimum. Unfortunately, you must distribute this clock over a printed copper trace with variable inductance, capacitance and length, which may exhibit characteristic line impedance (Zo) anywhere from 50 to 200 Ohms. Add to this the variable of receiver(s) load capacitance and notice that the 50% duty cycle square wave that you started with has become distorted with ringing and undershoot. You should be aware that undershoot below about -1.0 Volt can draw substrate bias current at the receivers causing transient errors.

This leads to a need for controlled impedance clock traces with good termination. This is especially true when device clock frequencies are greater than 30 MHz while the high and low times of critical minimum widths and voltage levels are specified.

Figure 3



Termination is needed on lines that exhibit ringing and signal distortion. The ringing and distortion are caused by mismatched clock driver output impedance, line impedance, and load input impedance. The termination is used to match the line impedance to the driver or load impedance.

Several methods of line termination are available (refer to Transmission Line "Termination," Figure 3):

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A. DC parallel load termination is generally a Thevenin equivalent resistor pair across the +5 Volts and ground buses with the mid point tied to the end of each clock line. While the signal integrity results are good, the large power consumption, due to the large voltage applied to the low end of line resistance make this scheme a poor choice.

B. AC parallel load termination can be effective to "tune" each load network with a selected parallel resistor-capacitor pair at the end of each clock line to ground. If the load capacitance or line length varies appreciably, so must the R-C termination pair. As with any of the parallel termination schemes, you must provide external trace and component mounting locations at the end of every clock line. AC power dissipation is quite high using this method.

C. DC source series termination can be incorporated within the clock driver output, thereby eliminating the need for external components. Clock loads may only be placed at the end of the line. This series termination reduces the power dissipation.

NOTE: Use of any of the parallel or termination methods precludes the use of branch or "Y" wiring within the clock fanouts due to impedance splitting.

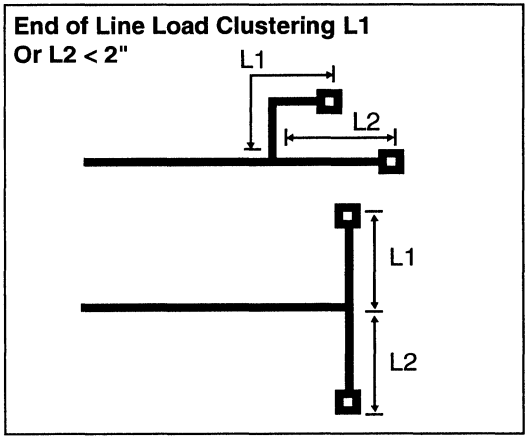
The following table compares these three described termination schemes.

	DC PARALLEL	AC PARALLEL	SERIES
EXTERNAL MOUNTING	YES	YES	NO
TUNING AT LOADS	NO	POSSIBLE	NO
DAISEY CHAIN	PENALTY	PENALTY	NO
LOAD CLUSTER AT END	DESIRED	DESIRED	REQ'D

The SC35XX helps the designer manage these clock termination in two ways. First, with a generous number of clock outputs (10 or 20) available, "daisy chained" or "branched" connected receivers can be avoided. Secondly, the source termination within the SC35XX output drivers is provided to terminate a lumped-load capacitance at the end of a 60–100 Ohm transmission line, without the addition of any discrete termination circuits.

While 100 Ohm traces are preferred, characteristic line impedances of 50 or 75 Ohms, may be necessary at an increase of power in the SC35XX's output drivers. These lower impedance PC board traces are generally dictated by manufacturing issues accompanying multiple signal, power, and ground layers in the PC board fabrication.

Figure 4



Remember that TTL type signal amplitudes, in the 2.5 to 4.0 Volt peak range, dissipate considerable AC (CV^2F) power. This AC power, coupled with the fact that the transmission line capacitance is at least twice as great at Zo=50 Ohms compared to Zo=100 Ohms, strongly suggests that the characteristic trace impedance of high frequency clock lines should be selected at 70 Ohms or above to reduce the clock distribution power. See Appendix B for equations.

NOTE: For series terminated lines, a maximum of two loads may be driven if the stub lengths are less than two inches in length. The capacitance of each pin is additive. See Figure 4.

SC35XX POWER DISSIPATION

With output frequencies above 50 MHz, the SC35XX's loading must be "managed" to limit its power dissipation to less than 1 Watt. This can be accomplished by minimizing the loading on each clock output or by connecting fewer of the clock outputs. In this case unused outputs still dissipate a minimum of power, which must be added into the total.

The SC35XX product data sheets detail all necessary power dissipation calculations.

NOTE: The capacitance of 70 Ohm transmission line is approximately 1.5 times that of 100 Ohm line for effective lengths up to one rise time or ~10 inches and, as mentioned above, with Zo=50 Ohms the capacitance is twice that of Zo=100 Ohms. The additional effective output load capacitance is approximately 8 pF for 70 Ohms at 10 inches as compared to 100 Ohms. See Appendix B for equations.

5

CAPACITIVE LOADS

Capacitive loads consist of four contributors:

- The "load" package itself, where a plastic flat pack may exhibit 4–8 pF loads, while a ceramic pin grid array may represent 8–15 pF loads.
- Plug in sockets can add 5–10 pF.
- Plated-through-holes and vias, in a dense multiplayer PC board may add as much as 5–15 pF.
- PC board trace impedance (as reviewed above)

AMCC strongly recommends that the user "balance" his loads. This will help to minimize skew at the various loads (the larger a load is, the slower the rise time of the clock). Where the user is not able to balance his loads, the skew will typically be derated at 50 ps/pF at the 1.5V threshold. (Example – one load is 5 pF heavier than all other loads – that load's clock will cross the 1.5V threshold 250 ps later than the others). A compensatory shortening of the higher capacitance load traces may be considered.

In addition to presenting capacitive loads, some microprocessors and co-processors require minimum peak clock amplitudes of 3.5 Volts or greater along with a minimum dwell time at a specified voltage level.

While each output driver of the SC35XX has been designed to handle a wide frequency-voltage-load range, they have also been designed to allow the parallel application of two (or more) adjacent drivers to a common load. By connecting two adjacent drivers to a common load, such as a microprocessor or co-processor, the user reduces the effective output series termination by half, while doubling the AC and static output current that can be supplied to that load.

RESET CONTROL

The reset control input is clocked into a 3 stage shift register in each driver to ensure that the asynchronous $\overline{\text{RESET}}$ input is synchronized to the input clock.

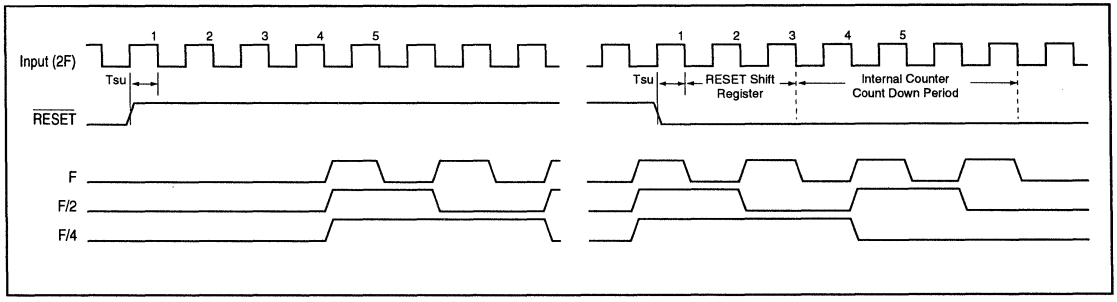
The outputs resume toggling when $\overline{\text{RESET}}$ is deasserted. On the fourth or fifth falling clock edge after the deassertion of $\overline{\text{RESET}}$, the outputs begin operating in a synchronous fashion.

When $\overline{\text{RESET}}$ is asserted, the internal counter is allowed to continue counting until each of its outputs is in the low state. At that point all the driver outputs will be in the low state, and they will be held low until $\overline{\text{RESET}}$ is deasserted. Since $\overline{\text{RESET}}$ may be asserted when the internal counter is in any state, there will be a delay of 0 to 7 clocks plus the 3 clock shift register before all the outputs will be disabled.

The designer may choose to use a simple "power on" reset function by using an external capacitor connected between the $\overline{\text{RESET}}$ pin and ground. When power is applied, the clock driver will be held in the disabled state until the capacitor is charged through the pull-up resistor on the $\overline{\text{RESET}}$ input.

NOTE: The above reset timing control applies to SC3500, SC3506, SC3507, SC3508, SC3517, SC3518, SC3528 and SC3529. If multiple outputs of ***SC35XX are to be reset resynchronized by a common $\overline{\text{RESET}}$ input to all, set up and hold time of $\overline{\text{RESET}}$ with respect*** *to the input clock of 3 ns must be accommodated.*

Figure 5. Reset to Output Timing



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USE OF MULTIPLE CLOCK CHIPS IN A SYSTEM

Many applications require greater than 20 clock outputs, and the use of multiple SC35XXs would be advantageous. The loads that receive these clocks may all reside on a large PC Board, or they may be distributed across a number of PC Boards interconnected via a backplane.

To effectively distribute these clocks requires the user to give some consideration to the strategy for distributing the SC35XX primary input clock. The objective is to get a low skew primary clock distributed to each SC35XX.

Remember that the SC35XX provides the option of two different types of primary clock inputs. For primary inputs over short distances and at frequencies of 50 MHz or less the single rail TTL input may be used. For "longer" distances and backplanes or where the primary frequencies exceed 50 MHz AMCC recommends that the user consider utilizing the "PECL" (Positive referenced 100K ECL input). In either case a single +5V power supply is the only power supply required.

The diagrams on the following pages summarize these recommendations.

The High Speed PECL distribution scheme utilizes the Motorola MC100E111 (Differential, 1:9, 50 ps Skew, ECL Driver) fed from the Crystal Oscillator (XCO). This primary fanout driver requires a pair of 240 Ohm pull down resistors to ground at its input pins. All of the output pairs should be source terminated by a 40 Ohm resistor in series and a 240 Ohm pull down (to ground) resistor at both legs of the differential PECL output. The differential primary fanout branches should be of equal length when routed to the receiving SC35XX.

Alternatively, the PECL backplane signal pairs can be parallel terminated at each SC35XX input by a thevenin equivalent 50–70 Ohm resistor to +3V. As an example, a 100 Ohm resistor to +5V and a complement 150 Ohm resistor to ground is equivalent to 60 Ohms to +3V.

There are two main advantages to these schemes.

1. Minimal Noise Generation

The high speed PECL Signals are limited to 0.8V in amplitude. This limits the potential crosstalk effects that they might have on surrounding signals, and limits their radiated energy (EMI).

2. High Noise Immunity

Since the PECL signals are differentially received at the SC35XX, any noise will appear in equal phase and amplitude on each of the differential signals. The SC35XX will reject this common mode noise at its receiver, providing excellent noise immunity.

The Low Speed TTL distribution scheme utilizes the SC3508 (TTL 1:20 Driver) fed from a crystal oscillator. Good clock distribution techniques should be followed. This includes avoiding "daisy chaining" or "branching" of the clock fanouts (greater than 2" stubs).

SUMMARY

The SC35XX greatly simplifies the task associated with distributing high performance clocks within today's systems. It accomplishes this by reducing the variables that the designer must contend with to these basic issues:

1) Keep each clock driver's loading light (SC35XX's large output count allows the clock loads to be distributed one load per clock output typically);

2) Balance the total load equally among all drivers;

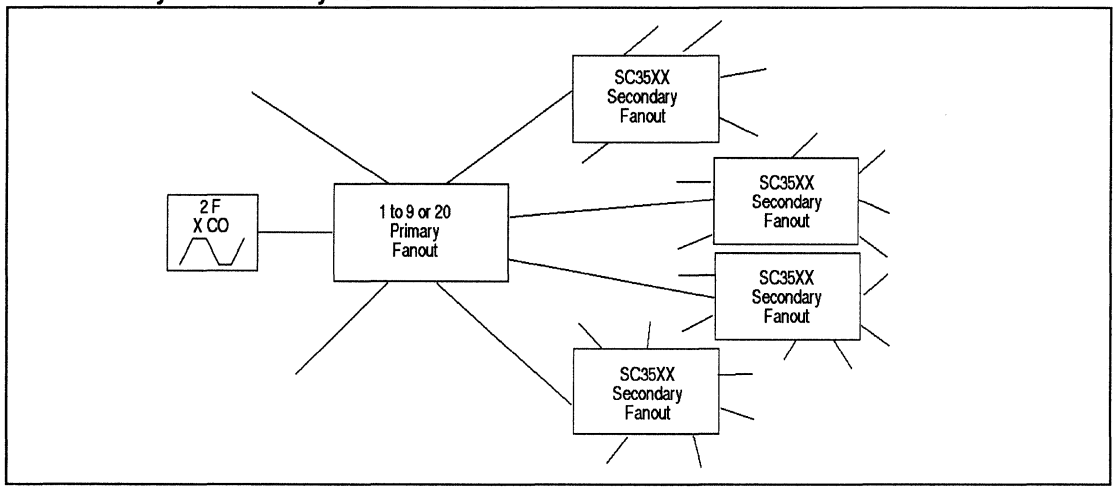
3) Keep clock trace lengths equal (Use serpentine traces to make all clock traces of equal length);

4) Be aware of and manage AC power dissipation in the SC35XX. Where possible make clock traces Zo=70 to 100 Ohms for minimal power dissipation;

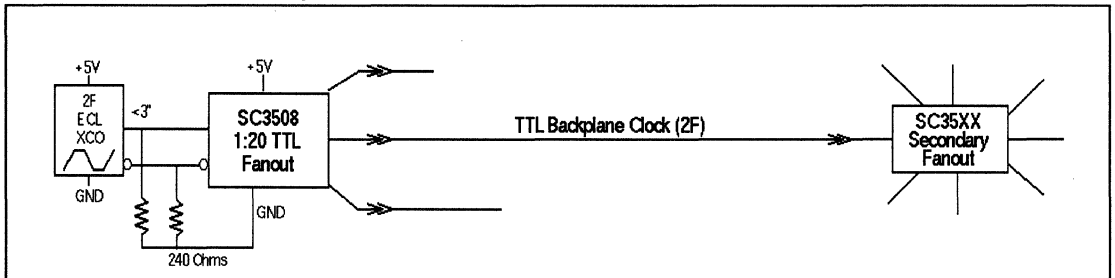
5) High capacitive loads at high frequencies can be supported by paralleling two adjacent SC35XX outputs;

6) Be generous with switching noise decoupling capacitors at the four sides of the SC35XX drivers, between the $+V_{CC}$ and ground planes. AMCC recommends a pair of 0.1 µF and 0.01 µF ceramic capacitors at each side of the SC35XX package. These decoupling capacitors should be placed on the same side of the board as the SC35XX, and very close to the power and ground package pins.

Basic Primary to Secondary Clock Fan-Out Tree



A Low Speed, TTL Primary Clock Fan-Out Path to the SC35XX



Note: An SC3508 primary to SC3508 secondary fanout is not recommended, due to the potential pulse width shrinkage of a 1X single-ended output feeding a second 1X driver without reshaping.

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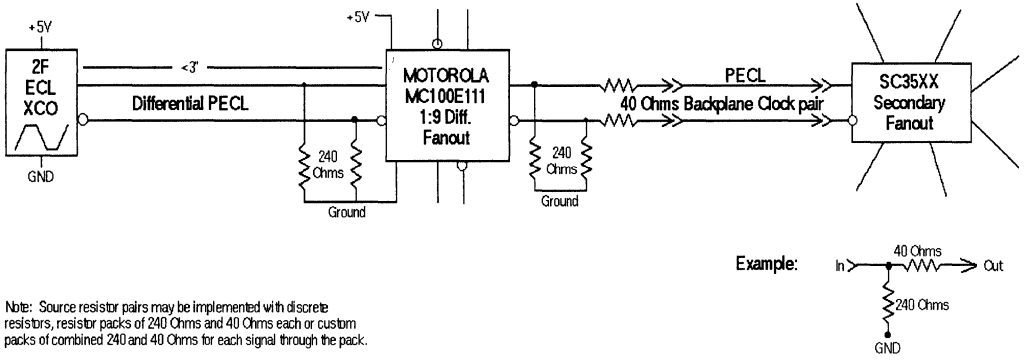
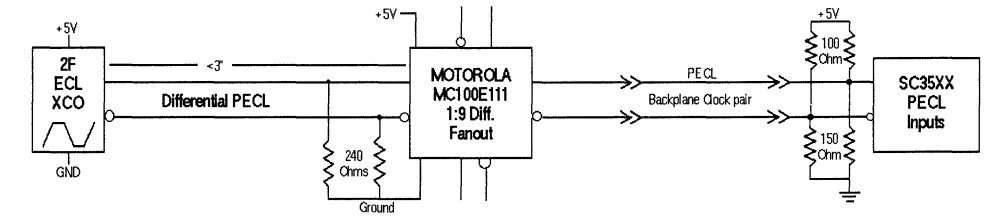
A High Speed Series Terminated PECL Primary Clock Fan-Out Path to the SC35XX



Note: Source resistor pairs may be implemented with discrete resistors, resistor packs of 240 Ohms and 40 Ohms each or custom packs of combined 240 and 40 Ohms for each signal through the pack.

Alternate PECL Primary Fanout Path to SC35XX With Parallel Termination at each SC35XX Input Pair



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APPENDIX-A

Crystal Controlled Oscillator Suppliers

MONITOR PRODUCTS, Oceanside, CA	619-433-4510
CTS, KNIGHTS DIVISION, Sandwich, IL	815-786-8411
ECLIPTEK, Fountain Valley, CA	714-963-4009
SARONIX, Palo Alto, CA	800-227-8974
STANDARD CRYSTAL, El Monte, CA	800-423-4578
CONNOR-WINFIELD, Aurora, IL	708-851-4722
ANDERSON ELECTRIC, Holidaysburg, PA	814-695-4428
CHAMPION TECHNOLOGIES, Franklin Park, IL	708-451-1000

APPENDIX-B

PC Board Transmission Line Equations

The characteristic impedance and propagation delay for printed circuit board traces are functions of the board material, physical board layout and board topology. Please refer to Figure 1 for referenced dimensions.

The following calculations assume G-10 glass-epoxy board material with an Er=4.7:

CHARACTERISTIC IMPEDANCE

$Zo = (Lo/Co)^{1/2}$

PROPAGATION DELAY

$Tpd = (Lo*Co)^{1/2}$ pS/inch, if units are in inches

MICROSTRIP TECHNOLOGY

$Zo = 35.2Ln[(6*h)/(0.8*w+t)]$

STRIPLINE TECHNOLOGY

$Zo = 27.7*Ln[(1.9*b)/(0.8*w+t)]$

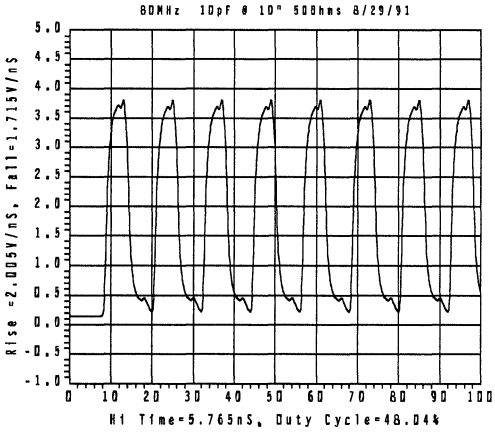
APPENDIX-C

Spice Simulation of Output Waveforms

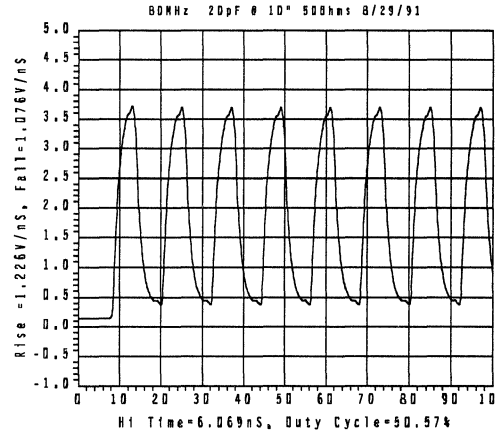
Modeled Frequency – 80MHz

(X-Axis is in ns)

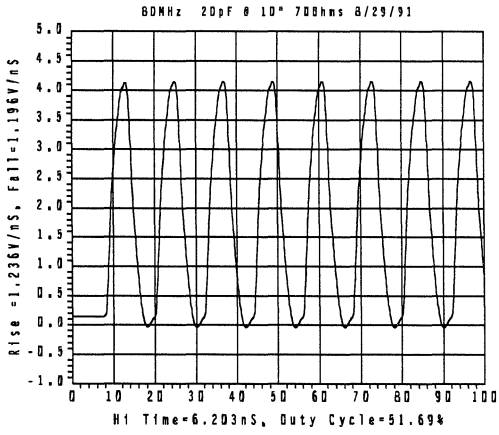
10 pF Load with 10" of Trace (Zo=50Ω)
Single Driver



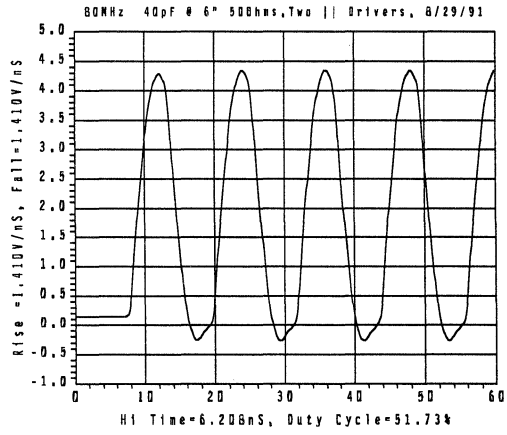
20 pF Load with 10" of Trace (Zo=50Ω)
Single Driver



20 pF Load with 10" of Trace (Zo=70Ω)
Single Driver



40 pF Load with 6" of Trace (Zo=50Ω)
Two Drivers in Parallel



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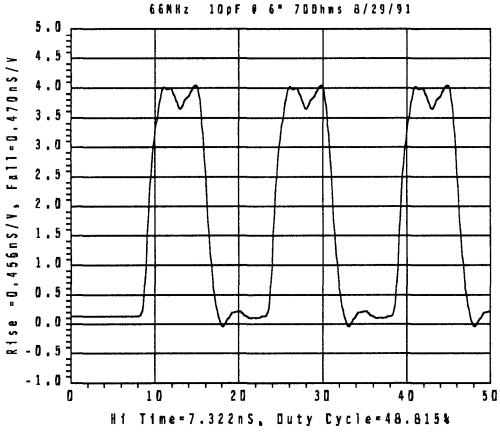
APPENDIX-C

Spice Simulation of Output Waveforms

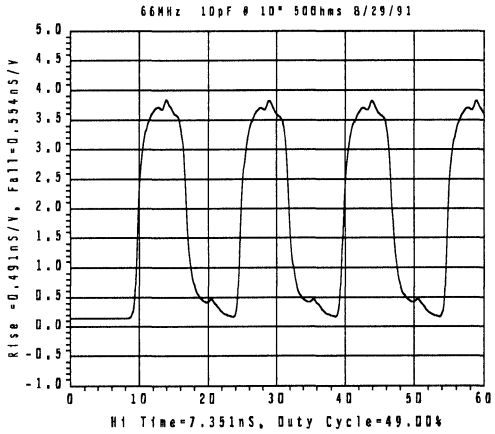
Modeled Frequency – 66MHz

(X-Axis is in ns)

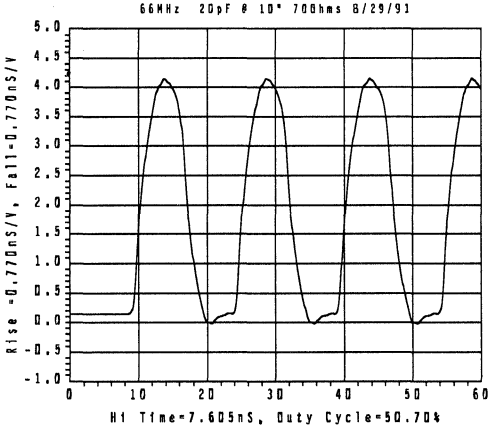
10 pF Load with 6" of Trace (Zo=70Ω)
Single Driver



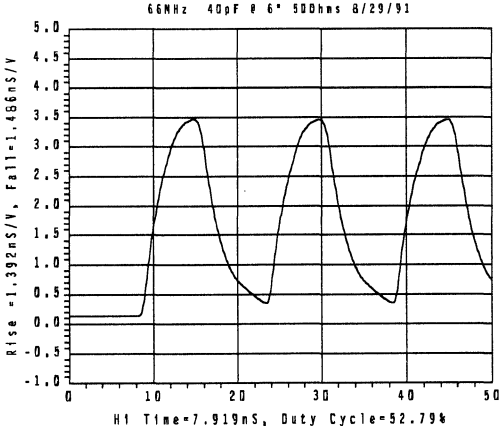
10 pF Load with 10" of Trace (Zo=50Ω)
Single Driver



20 pF Load with 10" of Trace (Zo=70Ω)
Single Driver



40 pF Load with 6" of Trace (Zo=50Ω)
Two Drivers in Parallel



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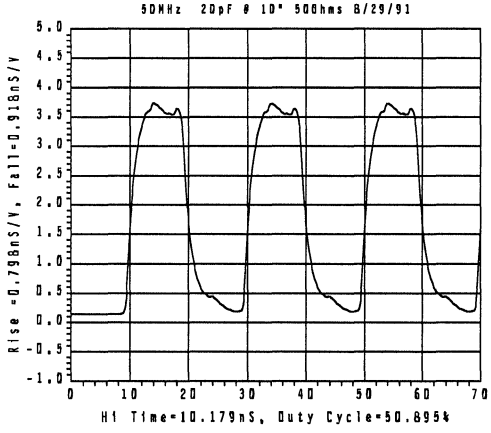
APPENDIX-C

Spice Simulation of Output Waveforms

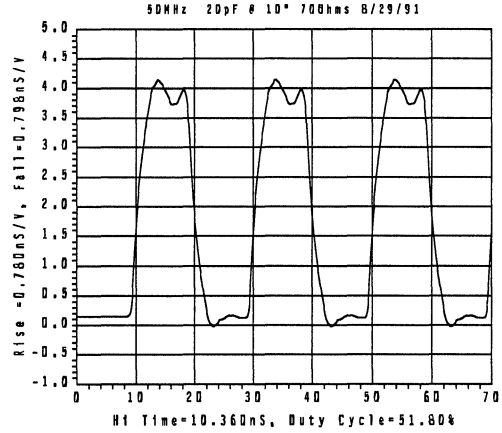
Modeled Frequency – 50MHz

(X-Axis is in ns)

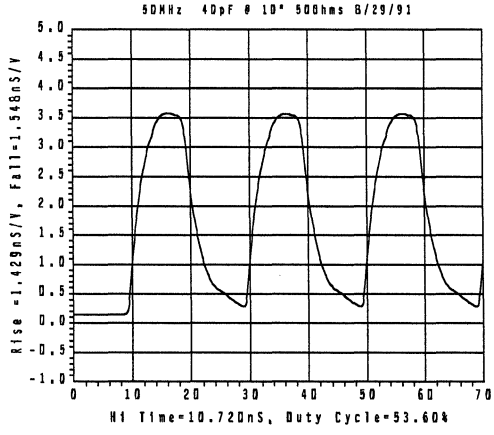
20 pF Load with 10" of Trace (Zo=50Ω)
Single Driver



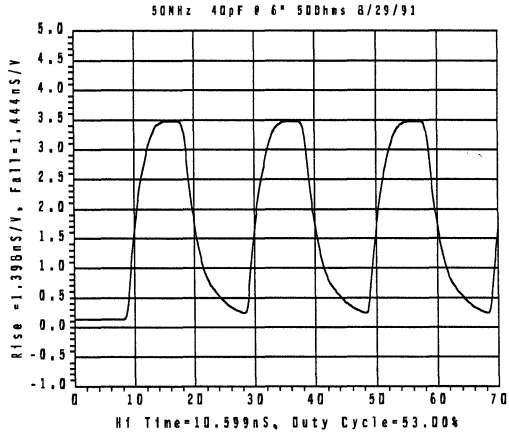
20 pF Load with 10" of Trace (Zo=70Ω)
Single Driver



40 pF Load with 10" of Trace (Zo=50Ω)
Single Driver



40 pF Load with 6" of Trace (Zo=50Ω)
Two Drivers in Parallel



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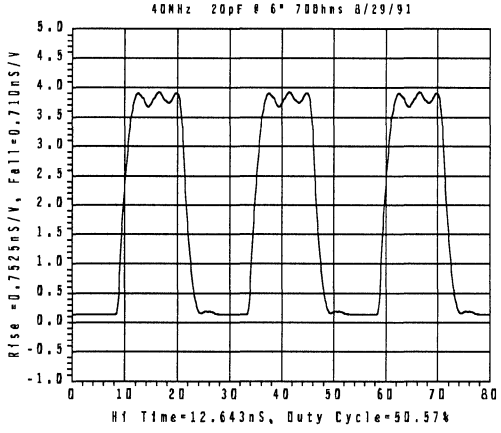
APPENDIX-C

Spice Simulation of Output Waveforms

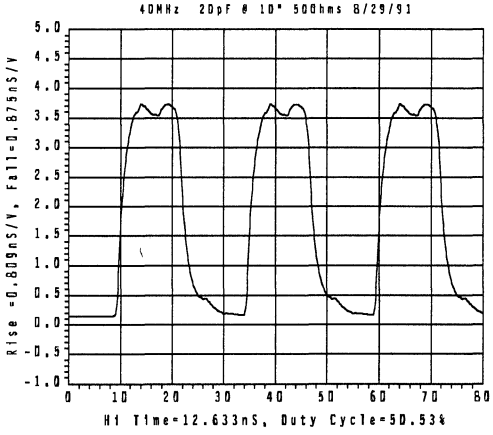
Modeled Frequency – 40MHz

(X-Axis is in ns)

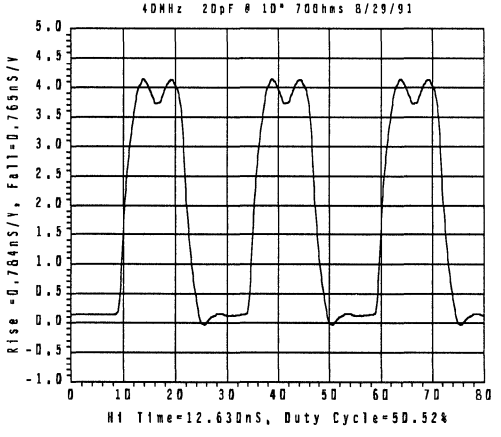
20 pF Load with 6" of Trace (Zo=70Ω)
Single Driver



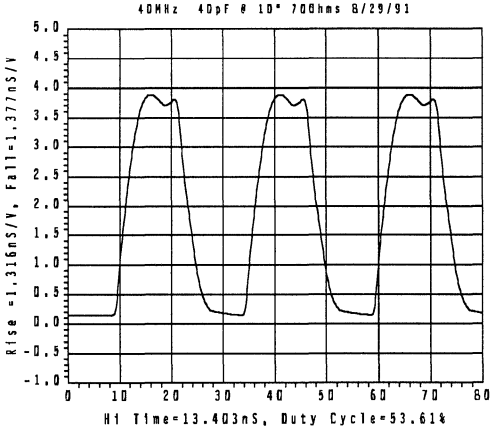
20 pF Load with 10" of Trace (Zo=50Ω)
Single Driver



20pF Load with 10" of Trace (Zo=70Ω)
Single Driver



40 pF Load with 10" of Trace (Zo=70Ω)
Single Driver



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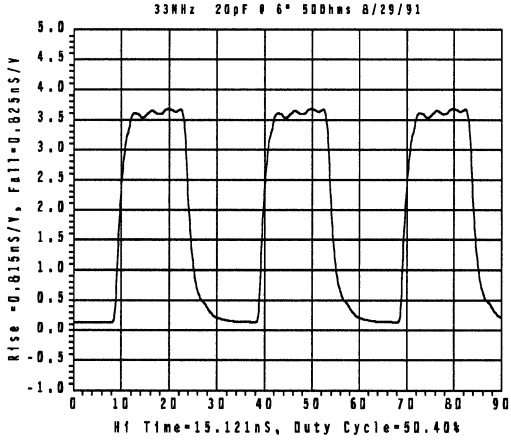
APPENDIX-C

Spice Simulation of Output Waveforms

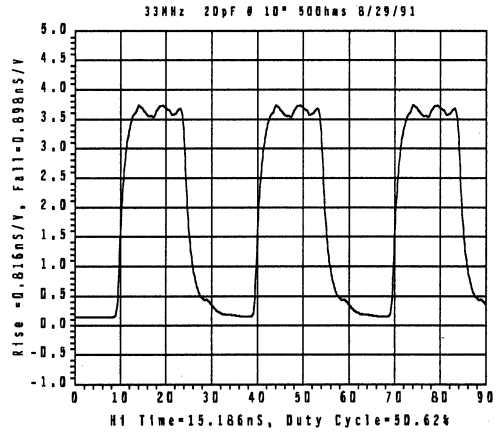
Modeled Frequency – 33MHz

(X-Axis is in ns)

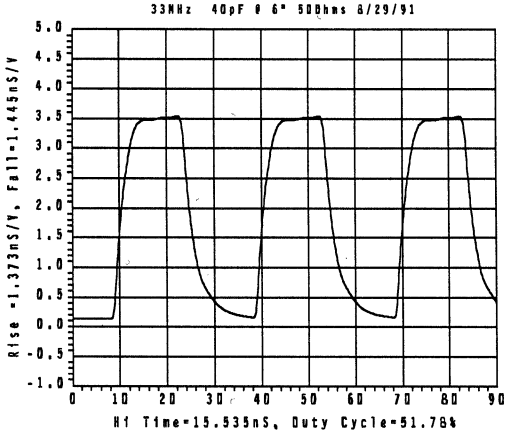
20 pF Load with 6" of Trace (Zo=50Ω)
Single Driver



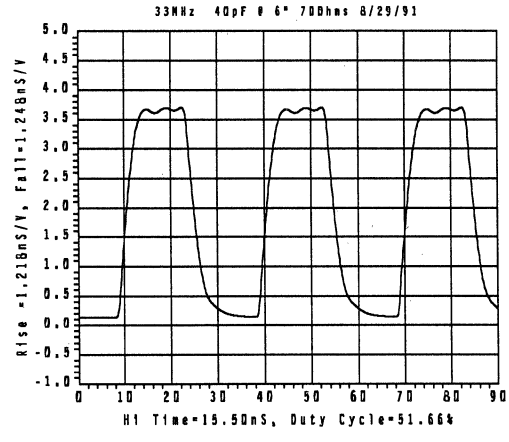
20 pF Load with 10" of Trace (Zo=50Ω)
Single Driver



40pF Load with 6" of Trace (Zo=50Ω)
Single Driver



40 pF Load with 6" of Trace (Zo=70Ω)
Single Driver



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Clock Design in Intel Pentium™ Processor Systems using the SC3508

M.K. Williams
Owner/Principal Consultant
Amherst Systems Associates

1. INTRODUCTION

The Pentium processor is the latest, high-performance entry in the X86 microprocessor family from Intel. There are 60- and 66-MHz versions. It operates on 64-bit data in two instruction pipelines with instruction prefetching and branch prediction. There is also on-board floating-point processing, as well as sophisticated data and instruction caching. These are all structural elements that, until very recently, were found exclusively in main-frame and supercomputer designs.

At the hardware level, Pentium designs also have a good deal in common with larger computer system designs. For example, the tighter timing margins and the higher clock and edge speeds of Pentium designs dictate the careful application of high-speed digital design methods. This includes employing design methods which preserve the fidelity of the clock pulse and effectively manage the tolerances present in the circuitry which distributes or receives the system clock.

The purpose of this application note is to clearly illustrate an approach to the design of the system clock for the Pentium using the AMCC SC3508. We will methodically work through a simple but representative example. In doing so, we will identify the important design decisions encountered in the design of a correctly timed system, and show methods for resolving them.

A Word About Specifications

In this document, we make use of a number of Pentium specifications. The reader is cautioned to verify any specifications with Intel prior to applying them, since they are all subject to change. It is also the responsibility of the designer to exercise sound engineering judgment to determine the suitability of how any particular specification or method is to be employed in his design.

2. DETERMINING YOUR DESIGN REQUIREMENTS

The first step in specifying the design of the clock for a Pentium, or any other system, is to clearly define what the design requirements are. Some of these will come from Intel specifications while others will be determined by aspects of the design, such as critical delay paths. In this section, we present some background on the

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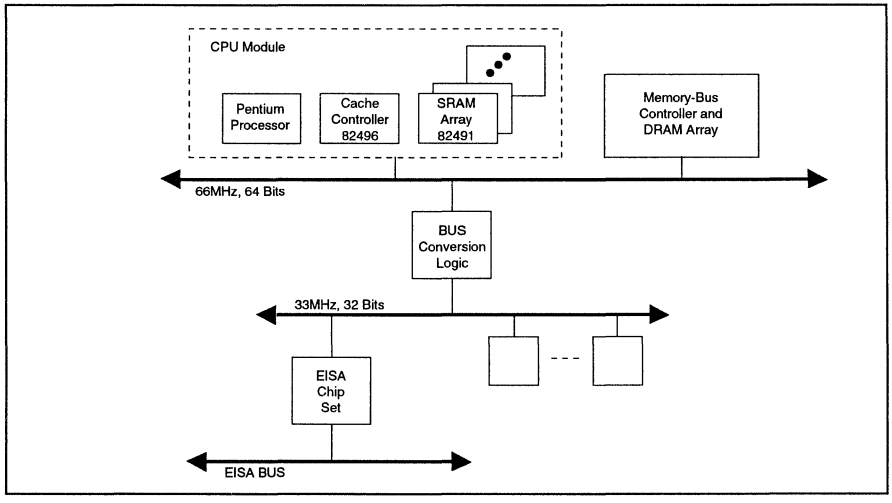
Figure 1.



mechanisms we are trying to manage and how to quantify the impact of those mechanisms on the design.

2.1. Timing-Environment Design: Fundamentals

The fundamental goal for any timing environment design is the specification of a *statistically stable* design. That is, it is assumed that the elements from which each system will be assembled will have some statistical distribution on their characteristic parameters (in our case, delay). Since many copies of the design will be fabricated, we must employ design methods which recognize this tolerancing and which ensure that every clock signal in each machine built arrives within the time interval predicted at design-time.

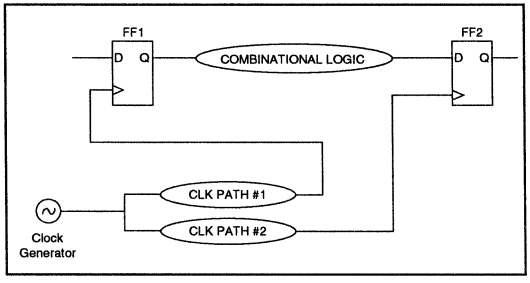
2.1.1. Basic Requirement on Clock-Arrival Time

We will use Figure 2, which shows a critical path, to illustrate the tolerancing effects we are concerned with controlling. Given that the two clock paths are built from components which have some statistical delay distribution, we can describe two pathological situations:

1. Clock-path 1 is slower than anticipated
2. Clock-path 2 is faster than anticipated

For the first case, FF1 is clocked late causing the data to arrive at FF2 after FF2 samples its input. The result is that the data is missed or the flip-flop enters a metastable state. The second case results in an equivalent situation by again clocking FF2 early relative to the arriving data. We can see from this simple example that any mechanism which causes the delay of a clock path to vary by more than the designer anticipated can result in a failure. Notice that it is *delay variation,* rather than the magnitude of the delay that results in timing failures.

Figure 2.



2.1.2. Basic Clock-Tolerancing Mechanisms

As we just saw, we must manage anything which can result in unequal or inconsistent arrival times of the clock at the load. This equates to two important design tasks:

1. Precisely balance the mean delay along every path from the clock generator to the clock loads.
2. Anticipate and manage those mechanisms which tend to alter the delay along these paths.

The merit of balanced mean delays for all clock paths is illustrated by Figure 3. Since the worst-case tolerance is computed from the earliest and latest arrivals, balancing the mean delays moderates the impact of any statistical delay variations.

We will use Figure 4 to illustrate the various tolerancing mechanisms we are attempting to manage. The figure shows a clock-buffer driving a transmission-line which terminates at some clock-input. This circuit is representative of a complete clock path for many Pentium systems (i.e. one-level buffering). Given Pentium speeds (66-MHz clock rates and fast clock edge rates),

Figure 3.

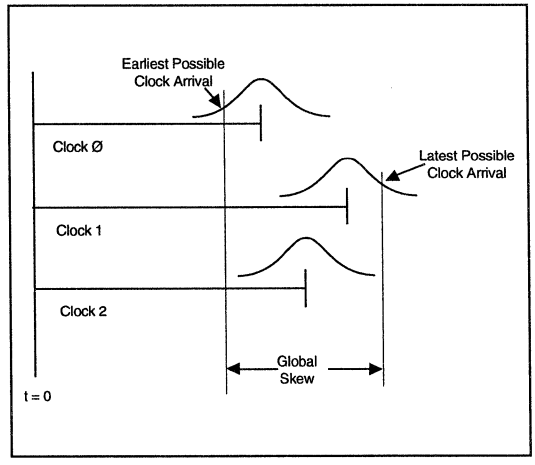


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Figure 4.

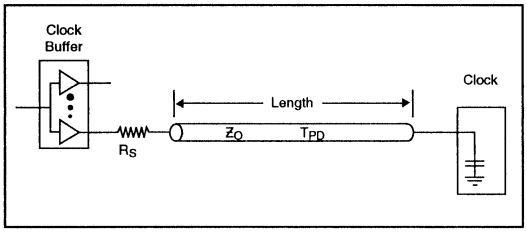
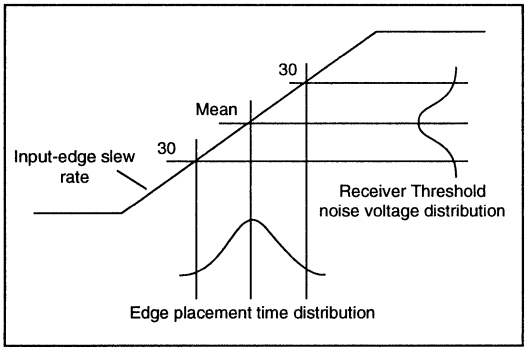


Figure 5.



a controlled-impedance interconnect is required. For this clock net, the expression for the variation in delay along the net is:

Tolerance = Intrinsic skew + Extrinsic skew + Jitter (1)

Where ,

Intrinsic Skew is the delay variation in the clock buffer. This is usually specified separately for part-to-part and pin-to-pin skew. Some clock buffers also specify skew within a group of clock-buffer outputs. Assuming a single-chip solution, we will use pin-to-pin.

Extrinsic Skew is delay variation attributable to effects in the interconnect.

Jitter is the cycle-to-cycle variation in the arrival-time of the clock. It is due primarily to noise in the power environment which, in turn, causes time-varying shifts in the input threshold of a device. The relationship between noise and edge-placement (jitter) is shown in Figure 5. For more information on jitter, see References 1 and 2.

Extrinsic skew is not a single mechanism. It is convenient to break it into three major components:

Extrinsic skew = ΔTOF + ΔDist_Del + MT (2)

Where,

ΔTOF is the **variation in the time of flight** of an undistorted signal. This is due primarily to variation in line lengths, and does not include additional delay variation attributable to edge degradation. This effect is addressed by equalizing all clock net lengths to that of the longest clock net.

ΔDist_Del is the **distortion-delay variation**. As a signal propagates, some of the high-end spectral content is attenuated. One prominent cause of this is the capacitance of the clock load. This results in a slower or degraded edge, and ultimately additional delay in reaching threshold voltage. Any variation in edge degradation (e.g. ΔC_L) results in a variation in delay. This is ΔDist_Del.

MT is the **manufacturing tolerance** on the delay. It ranges from one's of psec/in to mid-10's of psec/in.

The expression can be rewritten as:

$$\text{Tolerance} = \text{Int skew} + \Delta\text{TOF} + \Delta\text{Dist\_Del} + \text{MT} + \text{Jitter} \quad (3)$$

From transmission-line theory, we know that the propagation rate of a loaded transmission-line is:

$$T_{PD}' = T_{PD}\sqrt{1 + C_L/(L * C_0)} \quad (4)$$

Where,

- T_{PD} is the propagation rate of the unloaded transmission-line.
- C_L is the load capacitance (may be distributed)
- L is the length of the line
- C_0 is the intrinsic capacitance of the line

And the delay (time of flight plus distortion-delay) of a loaded transmission-line is simply:

$$LT_{PD}' = L*T_{PD}\sqrt{1 + C_L/(L * C_0)} \quad (5)$$

If we know the minimum and maximum values for C_L, we can compute the min and max delays for a given lossless transmission line (exclusive of manufacturing tolerances).

$$\Delta LT_{PD}' = L*T_{PD}(\sqrt{1 + C_{Lmax}/(L * C_0)} - \sqrt{1 + C_{Lmin}/(L * C_0)}) \quad (6)$$

And we can use the difference in these values to replace the second and third terms in expression (3):

$$\text{Tolerance} = \text{Int skew} + \Delta LT_{PD}' + \text{MT} + \text{Jitter} \quad (7)$$

We will use this expression to compute the tolerancing of various "tolerance groups" later in the example. One very important effect to note is that the preceding expression implies that clustering loads which have non-trivial load-capacitance variation on a single clock net will drive the $\Delta LT_{PD}'$ factor up and thus the overall tolerance.

2.1.3. Design Flow/Approach

There are a variety of approaches one can take:

Clocks first - Specify in detail the clock distribution and use resultant tolerances to compute delay margins on critical paths (Tcyc-Ttol = max Tpath).

Critical paths first - Design critical paths and use the resultant maximum delays to compute timing margins (Tcyc-Tpath=Ttol).

Most designers will take an approach that iterates between both styles, ensuring that both the timing and path delays are equally prioritized. In our example design, we are starting with critical-path information to determine timing margins, and then using the margin information to establish constraints on critical-path parameters (e.g. allowable load-capacitance variation on external loads). In detail, our decision-flow is as follows:

1. Determine allowable tolerances in CPU module.
2. Use critical path information to determine allowable clock tolerance (i.e. margin) on external loads.
3. From an inventory of clock loads, determine your slowest clock path in the system.
4. Starting with your tightest tolerance group (Pentium-82496), begin designing clock nets. Make each net approximately as long as that of the slowest path (previous step). As you progress through other tolerance groups, ensure you balance the mean delays.
5. From the unused margin for each group, develop constraints for each of the following:
   - Jitter
   - Manufacturing tolerances on net delays
   - Load-capacitance variation

Three-Level Tolerance Specifications

The Pentium specification dictates tolerances within the CPU module at three voltage levels (0.8, 1.5, and 2.0V). This was most likely done to combine tolerance management and pulse-fidelity into a common specification. However, designing for minimum tolerancing at multiple voltage levels can be very difficult. For clarity, we will design for minimum tolerancing at 1.5V and employ methods which ensure good pulse fidelity. This will ensure that the tolerances are satisfied at all three levels.

2.2. Specific Pentium System Design Requirements

The degree of difficulty for any timing-environment design is derivable from two aspects of the design — the number of board-level clock loads and the fraction of the cycle time allocated to clock tolerancing. Broadly speaking, a design becomes challenging when the number of loads exceeds 10 and the total tolerancing is restricted to 10 to 15% of the cycle time.

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For Pentium systems, the number of board-level clock loads varies according to the complexity of the design. For the most basic designs, the number of loads will be four to eight, primarily the Pentium processor and memory-bus controller. For very sophisticated designs (e.g. large server systems), with a second-level cache, as well as controllers for large interleaved memories and other synchronous devices, the number of board-level clock loads can exceed forty or more.

A typical 66-MHz design with a second-level cache will have 12 clock loads in the CPU module plus more loads for the memory bus controller (MBC) and other logic such as bus conversion. Therefore, depending upon how the MBC, etc. are implemented, a typical 66-MHz design will have 15 to 20 clock consumers.

The small fraction of the period alloted for tolerancing qualifies Pentium designs as quite challenging. At 66-MHz, the cycle time is 15 nsec. Clock tolerances within the CPU module are either 200 or 700 psec, and those external to it vary depending upon critical path delays to/from devices external to the CPU module. Stated another way, the tolerances within the CPU module are 1.3% and 4.7% of the cycle time.

For the rest of this section, we determine the various tolerances in a 66-MHz Pentium system with a second-level cache. The design requirements are configuration-specific and best considered in tolerance groups.

There are very few explicit clock requirements in the basic Pentium specification. Only clock stability (jitter) and pulse fidelity are specified.

Clock Stability (Jitter) - The Pentium clock must have a stability of better than +/- 250 psec. There are many metrics of frequency stability. While it does not explicitly state so, this specification refers to period-jitter. In a footnote to the specification, the distribution of the jitter in the jitter frequency spectrum excludes any peaking between 500kHz and 1/3 of the clock frequency (repetition rate).

Pulse Fidelity - The Pentium clock signal operates at TTL levels. The clock waveform must remain at the high and low levels for a minimum of 4 nsec, and the transition times must be less than 1.5 nsec. The Pentium specification dictates other clock waveform parameters beyond these. The reader is referred to the specification for complete information.

2.2.2. CPU Module

There are four possible configurations for the "CPU module". They are summarized in the following table.

Clock Speed (MHz)	Cache Size	Tolerance (psec)	Number of Loads
60 or 66	None	N/A	1 (CPU only)
66	256K	700	12 CPU, cache control, 10 SRAM
60	512K	800	20 CPU, cache control, 18 SRAM
60	256K	800	12 CPU, cache control, 10 SRAM

Layout Considerations Within CPU Module

There are flight-time specifications for various signal groups within the CPU module. For example:

Pentium - 82496: Only max flight times are specified (1.6 nsec is smallest value).

Pentium - 82491: Min and max flight times are specified (1 - 2.2 nsec range for 66-MHz).

These fight-times are critical, and it is likely that they will drive the placement of devices within the CPU module. That placement, in turn, will interact with clock tolerancing within the CPU module, since the distances from the clock driver to the clock loads determine certain tolerancing components. Specifically, interconnect tolerancing increases with the length of the

5

clock nets. For our example, we will use the configuration for the layout of the CPU module found in the Intel Pentium clock application note (Reference 8). There may be another approach (e.g. locating the clock driver in the center) that results in additional timing margin.

Pentium-82496 Tolerance Group: Two Loads at 200 psec Tolerance

This requirement is very tight and essentially unheard of in microprocessor systems. To meet this specification, both loads must be driven by the same pin of clock buffer. This eliminates the intrinsic skew component of the tolerance. By locating the Pentium and 82496 clock pins close to each other, and moving the branching point to the end of the transmission line (versus stubbing into two lines near the clock buffer), it is possible to minimize the manufacturing tolerance. The 200 psec tolerance thus splits between jitter and arrival time variation due to load capacitance variation.

Are there two different jitter specifications for the Pentium?

There can be some confusion in systems with second-level caches, since there appear to be two conflicting jitter specifications. This, however, is not the case:

> The Pentium clock specification states that the maximum allowable instability (jitter) on the clock to the Pentium processor is +/- 250 psec. Further restrictions as to how this energy can distribute across the jitter spectrum are also specified in a footnote.
>
> When the Intel CPU-Cache chip set is employed, the maximum tolerance between the clock signals driving the Pentium and the 82496 is limited to 200 psec. That is, for systems with second level-caches, the sum of the skew and the jitter between the clock signals driving the cache controller and the Pentium must be less than 200 psec.

Actually, there is no conflict in these specifications once you determine what they represent. The former jitter specification (+/- 250 psec) is established by the timing requirements of segments 100% internal to the Pentium. Any displacements larger than 250 psec run the risk of an internal Pentium timing failure. Furthermore, the requirements on the jitter spectrum are in place to prevent stimulating the resonant frequency of the loop filter in the internal PLL clock receiver. When jitter causes the PLL loop-filter to resonate, the signal out of the PLL (i.e. the internal clock) has more jitter on it than the signal driving into the PLL (i.e. the Pentium clock input), and is possibly larger than acceptable.

The latter specification (200 psec) governs the timing of segments between the Pentium and the 82496. When that specification is violated, timing failure on one of the paths which span both chips is likely.

How do you use this information?

In systems without second-level caching, the latter specification(200 psec) does not apply. Assuming there is sufficient margin on all paths external to the Pentium, system jitter must be less than +/- 250 psec and distributed in the jitter spectrum as specified in the footnote.

In systems with second-level caching, the 200 psec specification sets the upper limit on the jitter amplitude (jitter < 200 psec - Pentium/82496 skew). Furthermore, the jitter must distribute through the jitter spectrum as specified in the Pentium clock specification.

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Pentium-82491 & 82496-82491 Tolerance Groups: 10 SRAM (+2) Loads at 700 psec Tolerance

This group has many more clock loads, which necessitates driving the group by more than one pin of the clock buffer. Much of the margin obtained by increasing the tolerance specification to 700 psec is absorbed by the increased intrinsic skew. There will also be a more significant manufacturing tolerance contribution, since the SRAMs are more widely dispersed on the board and there will be more inches of interconnect in the clock nets that drive them.

Since we are forced to increase the intrinsic skew term of the total tolerance in this group, we want to use a point-to-point scheme (1 load/net). This reduces the range of load-capacitance variation and minimizes the ΔLT_{PD}'.

2.2.3. External Tolerance Groups

There will also be clock consumers external to the CPU module. In more complex Pentium designs, the number of loads in the external tolerance group can be several times the number of loads within the CPU module. The primary external clock loading will be in the memory bus controller (MBC). The tolerance requirements of this group will be dictated by the critical paths in this part of the design. Shortly, we will provide a simple example of computing that tolerance.

The majority of logic external to the CPU module is treated as memory. From a timing perspective, there are three distinct ways in which system memory can be configured:

1. Fully Synchronous
2. Divided Synchronous
3. Asynchronous

This impacts the clock as follows:

Fully synchronous systems: All clock inputs driven at 66-MHz

Divided-synchronous systems: All clock inputs in CPU module driven at 66-MHz, the memory-bus controller driven by both 66- and 33-MHz clocks, and all external devices driven by a 33-MHz clock.

Asynchronous systems: The CPU module and part of the MBC driven by 66-MHz clocks. A second, relatively-asynchronous clock (generated elsewhere in the system) drives part of the MBC and all external devices.

3. DESIGN EXAMPLE

3.1. Configuration

Our example system will be a fully synchronous 66-MHz system with a 256k second-level cache. It will use the Intel 82496 Cache Controller and 82491 Cache SRAMs. This configuration embodies many of the most challenging aspects of a Pentium clock design — the extremely tight tolerancing of the clocks within the CPU module, non-trivial load-capacitance variation, and determination of critical paths external to the CPU module. Furthermore, it will be extended to address other important design decisions — dual-frequency clocking and larger numbers of clock loads.

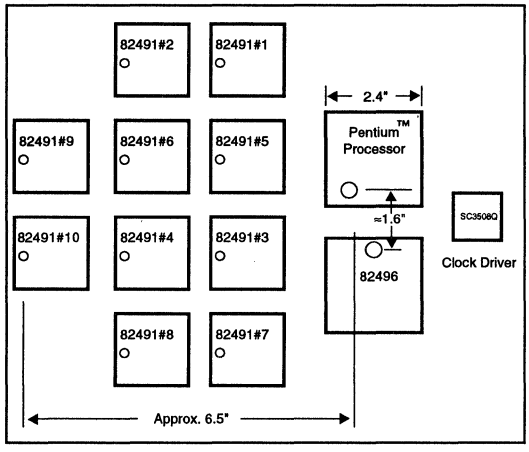
3.2. Preliminary Design Decisions

Before beginning to work through our example design, we will first describe some preliminary design decisions, and the impact they have on the system clock.

Clock-Buffer Selection - We are using an AMCC SC3508Q-1 clock buffer to drive the clock in this example. Our selection criteria for this part is based upon two factors. Specifically, that the SC3508Q-1 has twenty outputs and that the pin-to-pin skew for this part is less than 500 psec. In second-level cache systems, we have to drive 12 loads which have a non-trivial (relative to the tolerance requirement) amount of capacitive load variation. With 20 pins available from the SC3508Q-1, a single-IC point-to-point (i.e. one driver pin for each clock load) clock-distribution solution can be employed. If these loads had to be driven such that two or more SRAM inputs were clustered on a net, the arrival-time variation due to extrinsic skew and C_L effects (c.f. expressions 6 and 7) would exceed the allowed tolerance, even without factoring-in jitter.

Device Placement Within the CPU Module - We will use the placement suggested by Intel in Reference 8. Figure 6 shows that placement.

Figure 6.



Interconnect Environment - For our speeds and spectral content, we obviously need a controlled-impedance interconnect. The reader is referred to References 3 and 10 for detailed background information on this topic.

Microstrip vs stripline - We are routing all clock signals in microstrip, since the propagation rate is higher than that of stripline (146 psec/in for microstrip versus 182 psec/in for stripline). While the twenty or so clock nets may increase the level of radiated noise, the faster rates reduce the impact of interconnect manufacturing tolerances (5% of 146 is less than 5% of 182).

Parameters - Our example assumes a 70-ohm characteristic impedance. Higher values of Z_0 reduce the dynamic current available to charge the load capacitance. This, in turn, results in higher sensitivity to load capacitance variation. However, lower dynamic current also means less noise and therefore less jitter. The other parameters for our assumed interconnection environment follow.

Structure: Microstrip

Dielectric: 4.7 .012" thick

Conductor: .011" W x .0015"T copper

Properties:

C0 2.08 pF/in

L0 10.3 nH/in

Z0 70.4 ohms

Tpd 146.4 psec/in

Definition of External Loading and Tolerance - For any design, it is necessary determine the allowable clock tolerance on external critical paths. To do that, you have to identify the critical paths in the external circuitry. This may be quite difficult, given the large number of bus-transaction types, and that not all segments are 1-cycle long.

To simply illustrate what is required, we will assume we have identified the external critical path as shown in Figures 7 and 8. That is, the critical path runs from the fictitious Pentium output P5_OUT through two PLDs and into the fictitious inputs P5_IN and CC_IN. The delays through the PLDs have been arbitrarily assumed to be 3.5 and 3.2 nsec. For simplicity, we

Figure 7.

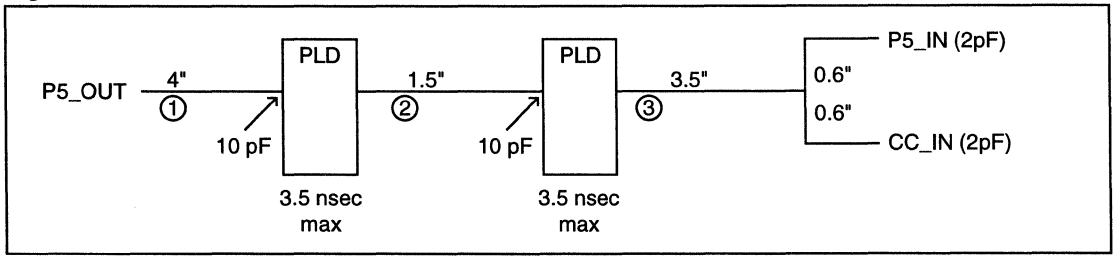


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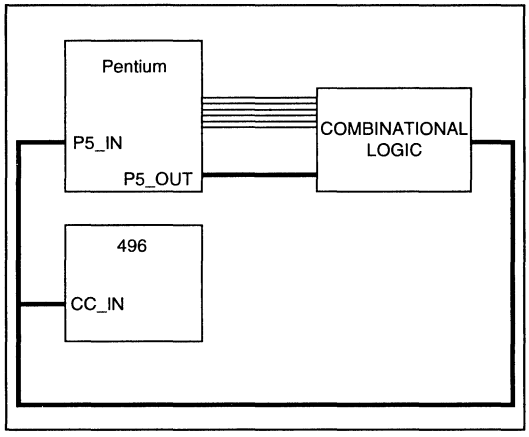
Figure 8.



assume P5_OUT is valid on the rising edge of the clock (add appropriate delay if this not the case for your system). Furthermore, we will assume the setup-time for both inputs is 5 nsec. Computing the path delay:

Segment 1

From our previous discussion, we can compute the delay of a loaded transmission line from expression (5). Using C_L = 10 pF (hopefully a maximum value), L = 4", and our previous values for the remaining variables, we have:

Delay(segment 1) = (4")(146.4ps/in)
$\sqrt{1 + (10pF)/(4" * 2.08pF/in)}$
= 868 psec

Segment 2

Using the same method, we compute:

Delay(segment 2) = 450 psec

Segment 3

For this segment, we analyze the capacitive effects of the two 0.6" segments as a single 1.2" segment with twice the load capacitance:

$LT_{PD}' = (3.5+.6)*(146.4)* \sqrt{1 + (2+2)/((3.5+1.2) * (2.08))}$

Delay(segment 3) = 713 psec

Computing the critical path delay, T_{CPD}:

T_{CPD} = Max gate delays +
Max net delays + MT^+ (8)

where, MT^+ is an estimate of the maximum positive manufacturing tolerance.

T_{CPD} = (3.5 + 3.2) + (.868+.450 + .713) +
9.6"(20 psec/in)
= 8.923 nsec

Computing the available clock tolerance, TOL_{EXT} :

$TOL_{EXT} = T_{CYC} - T_{CPD}$ - Setup-time (9)
= 15 - 8.923 - 5
= 1.077 nsec

We will make use of this figure later in the example.

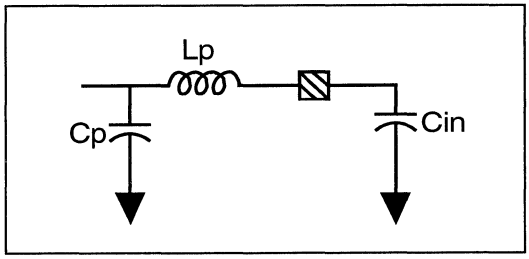
3.4. Inventory of Loading and Placement of Clock Loads

As the expressions illustrated earlier, variation in load-capacitance can be a principal contributor to clock tolerancing. We will see that in Pentium systems with second-level caching, this effect will dominate in the CPU module.

Loading in CPU Module

Intel has characterized the high-frequency behavior of the pins of the devices in the CPU module. Reference 7 provides models for all input pins in the CPU module (it also has output models). The model is shown in Figure 9. The values for the components are shown in Table 1. When analyzing various design approaches with a good simulation tool, these models will contribute to a more accurate answer. They are especially useful since minimum and maximum

Figure 9.



values are provided instead of typical values. However, since the model is a third-order low-pass filter which is driven by a transmission-line with its own distributed reactive components, we need to simplify it for our manual calculations here. Our transmission-line delay expressions employ a single, lumped load capacitance. So we need to estimate minimum and maximum values for input capacitance from the data in the table.

Table 1. Component Values for Input Pin Models

Device	Buffer Type	C_P (pF) Min/Max	L_P (nH) Min/Max	C_{IN} (pF) Min/Max
Pentium*	ER3	1.6/2.2	6.2/8.4	1.7/2.3
82496	ER8	1.4/1.9	5.8/7.9	2.4/3.3
82491	ER11	0.5/1.5	6.9/9.3	2.9/3.9

* Ignore 7pF maximum input capacitance rating from DC specification when using these models.

We are concerned about the time at which V_{IN}, the voltage across C_{IN}, charges up to threshold. An edge arriving at the pin on the transmission line can be considered as the sum of several sine-waves - the fundamental (66-MHz) and the harmonics (up to about 250-MHz). The elements of the filter attenuate or resist the high-end spectral components more than the lower ones, degrading the edge and delaying the time V_{IN} charges up to threshold. The fastest time will be when the high-end spectra is attenuated the least, the slowest time when it is attenuated the most. We can assume that the least attenuation will occur when both capacitors and the inductor are at minimum values. If we let the inductance go to zero, the capacitors are in parallel and we can simply add them. This assumption will result in a slightly faster estimate of the arrival time, since the inductor would limit some of the current which charges C_{IN}. The slowest time will occur when both capacitors and the inductor are at their maximum values. In this case, we can simplify, and still account for the effect of the inductor (resisting the passage of the current which charges C_{IN}), by letting the inductance go to zero but scaling C_{IN} up to increase the charging time. Our assumption is that scaling C_{IN} up by 50% will account for the elimination of the inductor. So our maximum value for the pin capacitance will be computed as:

$$\max C_{PIN} = \max C_P + 1.5(\max C_{IN}) \qquad (10)$$

The values we will use are shown in Table 2.

Table 2. Simplified Pin-Capacitance Values

Device	C_{MIN} (pF)	Typical C_L
Pentium	1.6 + 1.7 = 3.3	2.2 + 1.5(2.3) = 5.7
82496	1.4 + 2.4 = 3.8	1.9 + 1.5(3.3) = 6.9
82491	.5 + 2.9 = 3.4	1.5 + 1.5(3.9) = 7.4

Placement of Loads in CPU Module

Since we are assuming the placement suggested in Reference 8, we can derive the distance to loads from that. The shortest path from the clock driver to either the Pentium or 82496 clock pins is approximately 2 inches. The nearest and farthest 82491s to the clock buffer are approximately 5 and 7.5 inches, respectively.

Loading Outside CPU Module

Assumed placement and loading for the external clock loads is shown in Table 3. It is obvious from the table that either load 1 (largest capacitance value) or load 3 (most remote load) will be our worst case load. Note that we have assumed only typical values for C_L. We would obviously like to have min/max values, but this is usually not available.

Table 3. External Clock Loads

Load	Estimated Min Distance Clk buffer to load	Typical C_L
1	4"	10pF
2	5"	2pF
3	10"	5pF
4	5.5"	5pF
5	4"	2pF

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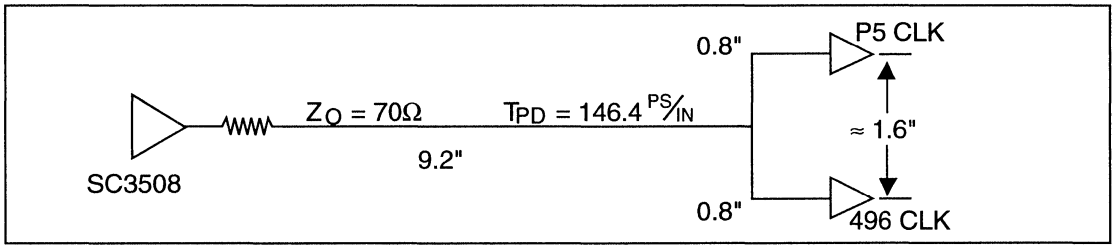
Figure 10.



3.5. Pentium/496 Tolerance Group

Requirement: 200 psec

Structure of Clock Net: This tolerance is sufficiently tight that both loads must be driven off the same pin of the clock buffer to eliminate extrinsic skew (500 psec for the SC3508Q-1). Examining the clock-load inventory from the previous section, we see that the longest clock net will probably be about 10". This will be our starting point for this and all subsequent nets. Nets can be serpentined to use up extra length. The layout of the CPU module tells us the two loads are about 1.6" apart. From this, we will assume the structure for our clock net as shown in Figure 10. The branching point for the stubs has been moved as far out on the transmission line as possible to reduce manufacturing tolerance effects between these two loads.

Analysis: For approximately 1.5 nsec transition times, the 9.2" segment of the line can be treated as a transmission line (i.e. an edge doesn't "know" about a load until it gets there). We can expect the edge to propagate down the 9.2" segment at the unloaded propagation rate, which is 146.4 psec/in. Therefore, we can analyze it and the stubs separately. The stubs are short enough to treat as equipotential nodes. We will treat the two loads as a single capacitive load equal to the sum of the two input capacitance ranges.

Net Delay = Delay of long segment + Stub delay

= 9.2" *Unloaded T_{PD} + Loaded stub delay

$= 1347 \text{ psec} + L*T_{PD}\sqrt{1 + C_L/(L * C_0)}$

where,

L = 0.8" for either stub

T_{PD} = Unloaded propagation rate = 146.4 psec/in

C_0 = 2.08 pF/in (computed earlier)

$3.3 \le C_L \le 5.7$ For Pentium input

$3.8 \le C_L \le 6.9$ For 82496 input

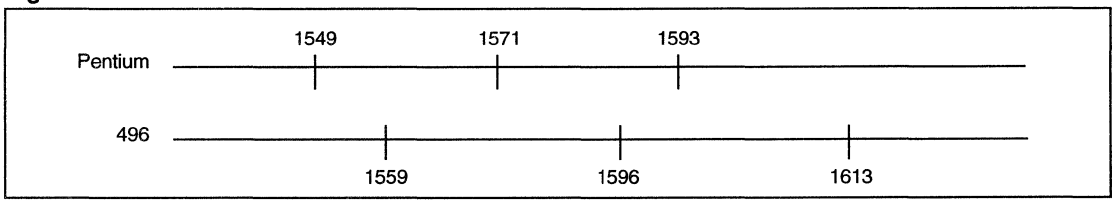
Computing the min and max delays for both paths (SC3508-Pentium and SC3508-82496), we have:

	Min	Max	Mean
Delay SC3508-Pentium	1549 1347+202	1593 1347+246	1571 1347+224
Delay SC3508-82496	1559 1347+212	1613 1347+266	1586 1347+239

Representing this graphically:

The difference between the earliest and latest arrivals is 1613-1549=64 psec. This leaves 200-64=136 psec margin for jitter and manufacturing tolerance on the stubs. We can improve this by aligning the mean delays. In this case, that means increasing the mean delay of the Pentium stub from 224 psec to 239 psec. And

Figure 11.



5

this is accomplished by lengthening the stub to the Pentium. Solving expression (5) for L, we find that a new Pentium stub length of 882 mils gives us the appropriate alignment.

	Min	Max	Mean
Delay SC3508-Pentium	1563	1609	1586
Delay SC3508-82496	1559	1613	1586

Tolerance: This is determined by the difference in arrival times. There are two cases (early Pentium/late 82496 and late Pentium/early 82496). Since we balanced the mean delays, both cases are identical.

Skew = 1613-1563 = 50 psec.

This should be guard-banded to accommodate manufacturing tolerances on the stubs. These tolerances will probably not be that large due to substantial tracking effects (i.e. these nets are all in the same area of the same layer of the same board). So we'll assume:

Guarded skew = **65 psec.**

This leaves 200-65 = **135 psec for jitter** so far. Remember that these figures are just for clocks in this tolerance group.

3.6. Pentium/82491 and 82496/82491 Tolerance Group

Requirement: 700 psec.

Structure of Clock Net: We will assume point-to-point for all SRAM nets to minimize C_L effects. The net will be as shown in Figure 12, with an approximate length of 10".

Analysis: Using

$$3.4 \le C_L \le 7.4 \quad \text{for 491s}$$

and forcing the mean delay to 1586 psec, we solve for a length of 9.621". The full set of delays is:

	Min	Max	Mean
Delay SC3508-82491	1523	1649	1586

Tolerance: If the difference between arrival-times at the 82491s and the 82496 are acceptable, then they will also be acceptable for the difference between the Pentium and the 82491's. This is, of course, because the mean delays are aligned and the arrival time spread is wider at the 82496 than at the Pentium. So we will analyze with respect to the 82496. Using expression (7):

$$\text{Tolerance} = \text{Int skew} + \Delta LT_{PD}' + MT + \text{Jitter} \qquad (7)$$

Substituting our 700 psec limit in for the tolerance

$$700 \text{ psec} \le 500 + \Delta LT_{PD}' + MT + \text{Jitter}$$

$$200 \text{ psec} \le \Delta LT_{PD}' + MT + \text{Jitter}$$

where,

$\Delta LT_{PD}'$ in this case is the worst case arrival time difference (due to C_L effects) between the 82496 and the 82491s. Again, we only have to compute one of the two possible cases due to symmetry.

$$\Delta LT_{PD}' = 1649 - 1559 = 90 \text{ psec}$$

Guard-banding this figure to accommodate manufacturing tolerances, we can assume

Guarded skew = 115 psec

Leaving 200 - 115 = 85 psec for jitter.

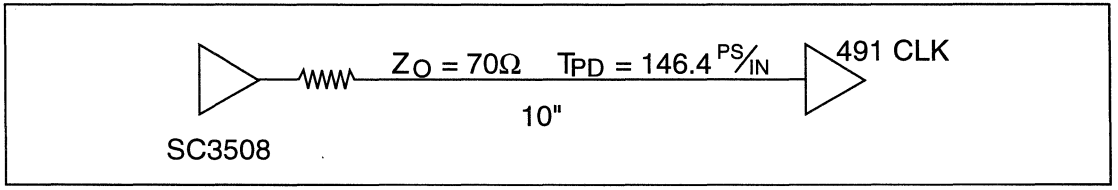
3.7. External Tolerance Group

Requirement: 1.077 nsec (computed earlier)

Structure of Clock Net: We will assume point-to-point for the external loads as well. This net will be identical to that shown in Figure 12.

Analysis: For this group, analysis will not yield the same quality result as it did for the preceding tolerance groups. The reason is that for this

Figure 12.



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group, it is highly likely that you can only get typical values for each load-type. Unfortunately, you require min/max information about load capacitance to compute arrival time variation. There are, however, some approaches that maximize the ability of the design to cope with uncharacterized tolerancing mechanisms. These include:

1. Point-to-point clock nets to minimize the C_L variation on any one net. Given that we have 20 outputs to work with on the clock buffer, this is not a problem for most Pentium designs.
2. Use the lowest possible Z_0 which produces the maximum dynamic current, and thus charges the load capacitance as fast as possible. Reference 2 elaborates on the sensitivity of tolerancing to transmission-line characteristic imedance and variation in load-capacitance.
3. Extending the "charge current" logic applied in the previous point to termination, it is generally advisable to select a termination scheme other than series. The SC3508Q-1 employed in our example design has integral series termination. However, the benefit of point-to-point distribution afforded by the SC3508Q-1's twenty output pins outweighs the impact of series termination.
4. Design each external clock net such that its delay, as computed with typical C_L values, is aligned with the mean delay value of the CPU module.
5. Bypass heavily and use other noise reduction methods to minimize clock jitter at that load, *and* devices it communicates with.

From our earlier computations, we know the maximum allowable tolerance for the external tolerance group is 1.077 nsec. This is the maximum arrival-time difference between either the Pentium and any external load, or the 82496 and any external load. Note that instead of treating all external clock loads identically, we could separately analyze for each load, if necessary.

Computing the mean delay for external load #3 first:

$$LT_{PD}' = L*T_{PD}\sqrt{1 + C_L/(L * C_0)} \qquad (5)$$

Where we will substitute:

$L = 10"$

$C_L = 5pF$ typical

We get a typical delay of 1631 psec. We need to adjust something so that this typical delay aligns with the mean in the CPU module of 1586 psec. We can add delay to all the other nets or possibly reduce the delay of this net. Let us assume we can take the latter approach by slightly repositioning the SC3508 relative to this load. To align the delays, the length of this net must be 9.698" (computed by forcing the loaded delay in (5) to be 1586 psec).

At this point, we may also want to consider reducing Z_0. Repeating the preceding for all the other external loads:

Load	Estimated Min Clock-Net Length	Typical C_L	Actual Length
1	4"	10pF	8.693"
2	5"	2pF	10.363"
3	10"	5pF	9.698"
4	5.5"	5pF	9.698"
5	4"	2pF	10.363"

3.8. Final Design Decisions and Summary

At this point we have "finished" the design of the clock nets. We still have some constraints to compute, which we will do in this section. However, in the event that an unachievable constraint results, it would be necessary to rework the layout of the loads and the lengths of the clock nets.

Jitter, Noise, and External C_L Constraints

The following summarizes the tolerancing for the nets we have just designed:

Tolerance Group	Intrinsic Skew (pin-pin) (psec)	Extrinsic Skew w/ mfg. tol (psec)	Tolerance Constraint (psec)	Jitter Constraint (psec)
Pentium-82496	0	65	200	135 200-65
Pentium-82491	500	< 115*	700	> 85 700-500-<115
82496-82491	500	115	700	85 700-500-115
82496-EX1	500	???	1077	???
82496-EX2	500	???	1077	???
82496-EX3	500	???	1077	???
82496-EX4	500	???	1077	???
82496-EX5	500	???	1077	???
82496-EX6	500	???	1077	???

* - By examination.

System Jitter Constraint - Given the complete information we have about the loads in the first two tolerance groups, we were able to compute jitter constraints. This was done using expression (7). While jitter can be considered to vary from location to location in a system, it is a much more manageable problem to assume it is uniform throughout the system. So, for our example, we will assume a jitter constraint of

System Jitter Constraint = Min(135, <85, 85)
= 85psec

Therefore, we will limit jitter to 85 psec on a system-wide basis. Given the 1077 - 500 = 577 psec of room we have for combined jitter and extrinsic tolerancing in the external tolerance group, it is not likely we will need to control jitter to a lower level. We will now use our jitter constraint to compute the extrinsic skew constraint on the external loads and an approximation on the noise level.

External Extrinsic Skew Constraint- Our limit on tolerancing in the external group due to load-capacitance variation and manufacturing tolerances on the net is:

1077 - 500 - 85 = 492psec

In the following table, we have computed the allowable variation on C_L. The analysis allocates 20 psec/in for manufacturing tolerances on each external net, computes an extrinsic skew constraint from that, and then a constraint on C_L.

Load	C_{TYP} (pF)	Length (in)	Mfg Tol @ 20 psec/in (psec)	Extrinsic Skew Limit (psec)	ΔC_L [2] (pF)
1	10	8.693	174	318	± 5.6
2	2	10.363	207	285	± 4.2
3	5	9.698	194	298	± 4.7
4	5	9.698	194	298	± 4.7
5	2	10.363	207	285	± 4.2

1. 492psec - MT
2. Computed from expression (6) by setting ΔLT_{PD}' equal to the extrinsinc skew limit, and forcing symmetric variation of the C_L value around the typical value. That is, letting

   $C_{Lmax} = C_{TYP} + C_L/2$ and,

   $C_{Lmin} = C_{TYP} - C_L/2$

The values from the right-most column are a constraint that we place on the clock inputs of the devices that receive the external clocks. In most cases, it is clear we have more than adequate margin on the low side.

System Noise Constraint - From Figure 5, we know that noise in the power environment and clock-signal transition-times interact directly with jitter. Budgeting jitter in a clock-distribution and reception network is complicated and a detailed treatment of that is beyond the scope of this note. In our example, we have a single device performing clock-distribution, and can assume all jitter is added at that point. An approximation of the maximum noise-voltage that the SC3508Q-1 can see at its power pins can be derived from:

$$\text{Max Jitter} \approx \text{Slew}_{max} * V_{noise(p\text{-}p)} \qquad (11)$$

where,

Slew_{max} is the slowest (largest) slew rate in nsec/volt.

$V_{noise(p\text{-}p)}$ is the peak to peak noise voltage.

This was "derived" by examination of Figure 5. Assuming the signal into the SC3508-1 climbs 4V in 5 nsec (typical for many crystal oscillators),

$0.085 \text{ nsec} = (5\text{nsec}/4\text{V}) * V_{noise(p\text{-}p)}$

$V_{noise(p\text{-}p)} = 68\text{mV}$

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This is an aggressive but achievable noise-voltage level at the pin of the SC3508Q-1. To achieve this, noise reduction methods must be used, such as including suitable bypass capacitors. A detailed discussion of noise-voltage reduction is beyond the scope of this note. Notice, however, that employing a crystal oscillator with faster edges increases the allowable noise voltage.

Configuring the SC3508Q-1

The data sheet provides detailed information on configuring the various inputs of the SC3508Q-1. The CLOCK SEL pin must be tied either low for a TTL source or high for an ECL source. Since the clock must toggle during power up (c.f. Section 2.2), the RESET input of the SC3508Q-1 can be tied high (inactive). Finally, source series termination is provided within the SC3508Q-1 to match the output drivers to lines with characteristic impedences in the range of 50 to 75 ohms. The patented output drivers also prevent undershoot and thereby reduce noise at the receiving chip input. The result is that the SC3508 provides 20 outputs with excellent signal integrity.

A Word About Serpentine Delays

Through out this design example we have assumed that the clock net lengths are matched. A typical method of accomplishing this to serpentine clock nets which need additonal length.

The reader is cautioned that serpentining can have an effect on the propagation rate of a net. In Reference 2, this effect is described and illustrated with measurement.

4. EXTENSIONS TO THE DESIGN EXAMPLE

Our example was for a "typical" Pentium system. There are two significant extensions that can be made to this example:

1. Divided synchronous systems
2. Larger systems

4.1. Divided Synchronous Systems

In a divided synchronous system, the CPU module (12 loads) runs at 66-MHz and all of the circuitry external to the CPU module runs at 33-MHz. The memory bus controller will need one or two copies of both clocks to coordinate communication between the two timing environments. If our example design were converted to a divided synchronous system, we would need to select a clock buffer capable of providing an appropriate number of copies both clock frequencies. The AMCC SC3500Q-1 can fill this role. The SC3500's outputs are arranged in three groups (10, 5, & 5 pins), each of which can be operated at various relationships to the input as follows:

Output Group	Relationship to Output
Fa	10 outputs at $F_{input}/2$ (max = 80 MHz)
Fb	5 outputs at $F_{input}/2$ or $F_{input}/4$
Fc	5 outputs at $F_{input}/4$ or $F_{input}/8$

Therefore, we can convert our example to a divided synchronous system using an SC3500 as follows:

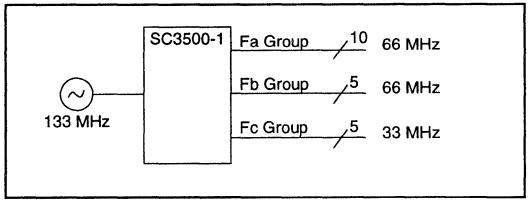
1. Drive the buffer with a 133MHz source.
2. Configure Fa and Fb groups for 66MHz (15 clock signals)

   11 loads in CPU module (as previous)

   4 clock signals available for MBC
3. Configure Fc group for 33-MHz (5 clock signals)

Figure 13 shows this configuration. The analysis of tolerancing for this new arrangement would be similar to what was shown in our original example.

Figure 13.



4.2. Larger Systems

When the number of loads in a system exceeds the number of pins on the clock buffer employed, it is necessary to move to a tree-structured clock-distribution network to fan out the signals. When this is the case, the tradeoffs and the analysis are more complicated. The most noteable effect is that part-to-part buffer tolerances come into play. In even larger systems, cascaded part-to-part tolerances come into play. A complete discussion of these issues goes beyond the scope of this note. References 1 and 2 cover this subject in more depth. We will, however, provide some guidelines:

1. Exploit locality (i.e. the commonality of clock paths) in signal groups where tolerancing requirements are tight. For example, drive all of the loads in the CPU module from a single SC3508Q-1 to keep the part-to-part tolerances out of tolerances expressions.
2. Align the mean delays of all clock paths.

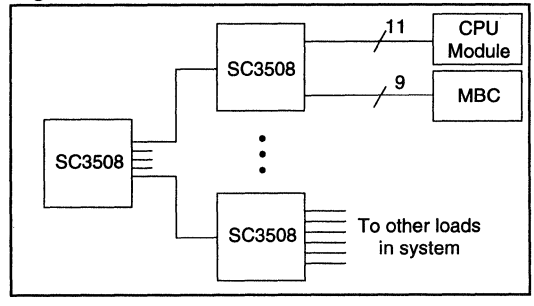
Figure 14 shows a mid-sized Pentium clock distribution network. It takes advantage of the reduced tolerancing among the outputs of the Fa group (250 psec).

5. SUMMARY

This note has presented a detailed example of clock-distribution in a typical Pentium design using AMCC's SC3508Q-1 clock driver. This example discussed the most important design decisions, and extended the example to other common design cases. As we saw, many of the timing-environment design methods previously necessary only in larger and faster computers are now necessary in Pentium systems.

Even with these constraints, this application note shows that the SC3508Q-1 can be used in Pentium systems to create a statistically stable design. With twenty outputs, a low-skew design, and its no-undershoot drivers, the SC3508Q-1 allows the engineer to design a clock distribution scheme that will satisfy the rigorous requirements of the Pentium chips.

Figure 14.



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6. REFERENCES

1. Williams, Michael K., "Distortion and Tolerance Mechanisms in High-Speed Clock Delivery", *Proc. 1993 Hewlett-Packard High-Speed Digital Symposium*, 1993, pp. 4-1 to 4-41. Also available as application note ASA 93-1 from Amherst Systems Associates.

2. Williams, Michael K., "Design Tradeoffs in High-Speed Clock Distribution and Reception", *Proc. 1993 Hewlett-Packard High-Speed Digital Symposium*, pp. 6-1 to 6-34. Also available as application note ASA 93-2 from Amherst Systems Associates.

3. Williams, Michael K., *High-Speed Digital Design: Principles and Practices*, Course notes, Amherst Systems Associates, 1993,

4. Williams, Michael K., "Timing Considerations in Clock Distribution Networks", *Proc. 1992 Hewlett-Packard High-Speed Digital Symposium*, pp. 2-1 to 2-21. Also available as application note ASA 92-2 from Amherst Systems Associates.

5. AMCC, Clock Driver Application Note #1, 1992, 14 pages.

6. Intel Corporation, *Pentium Processor User's Manual - Volume 1: Pentium Processor Data Book*, 1993.

7. Intel Corporation, *Pentium Processor User's Manual - Volume 2: 82496 Cache Controller and 82491 Cache SRAM Data Book*, 1993.

8. Lin, Derrick, and Jim Reilly, *Pentium Processor Clock Design*, Application Note AP-479, Intel Corporation, March 1993.

9. Jolly, Rich, *Clock Design in 50-MHz Intel486 Systems*, Application Note AP-453, Intel Corporation, 1991.

10. Blood, William R., Jr., *MECL System Design Handbook*, Fourth edition, Motorola Inc., 1988.

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Clock Driver Package Specifications 6

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CLOCK DRIVER PACKAGE SPECIFICATIONS

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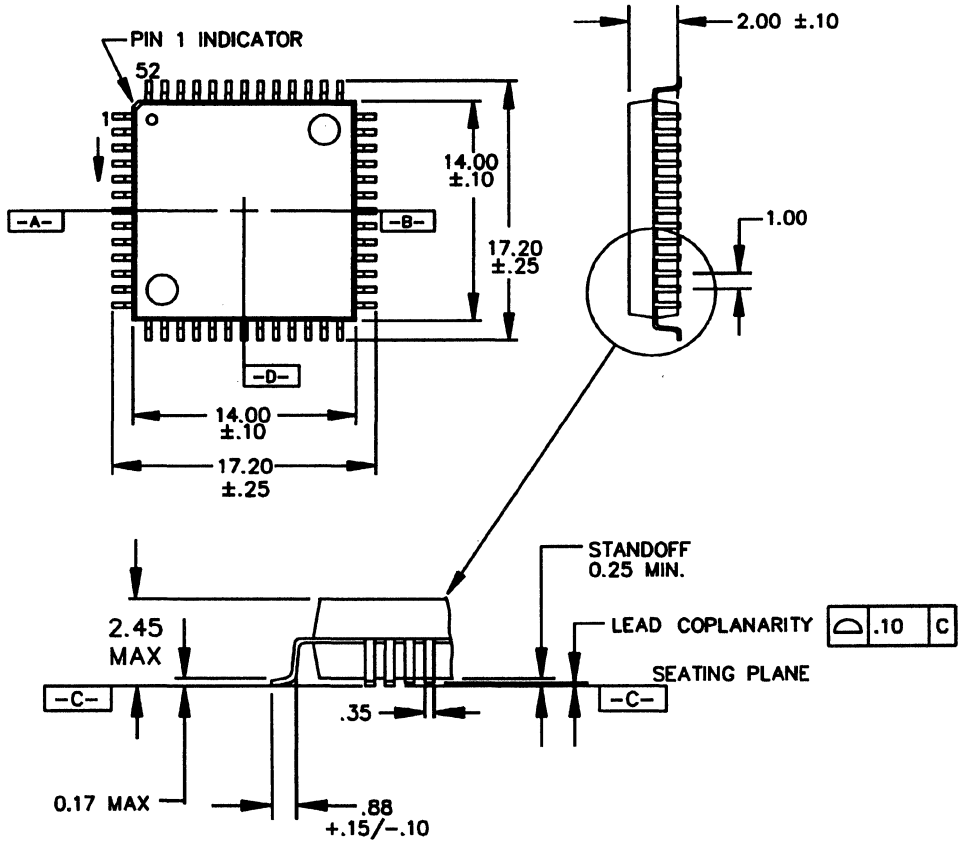
52 PQFP
14 x 14 x 2.0 x 3.2mm



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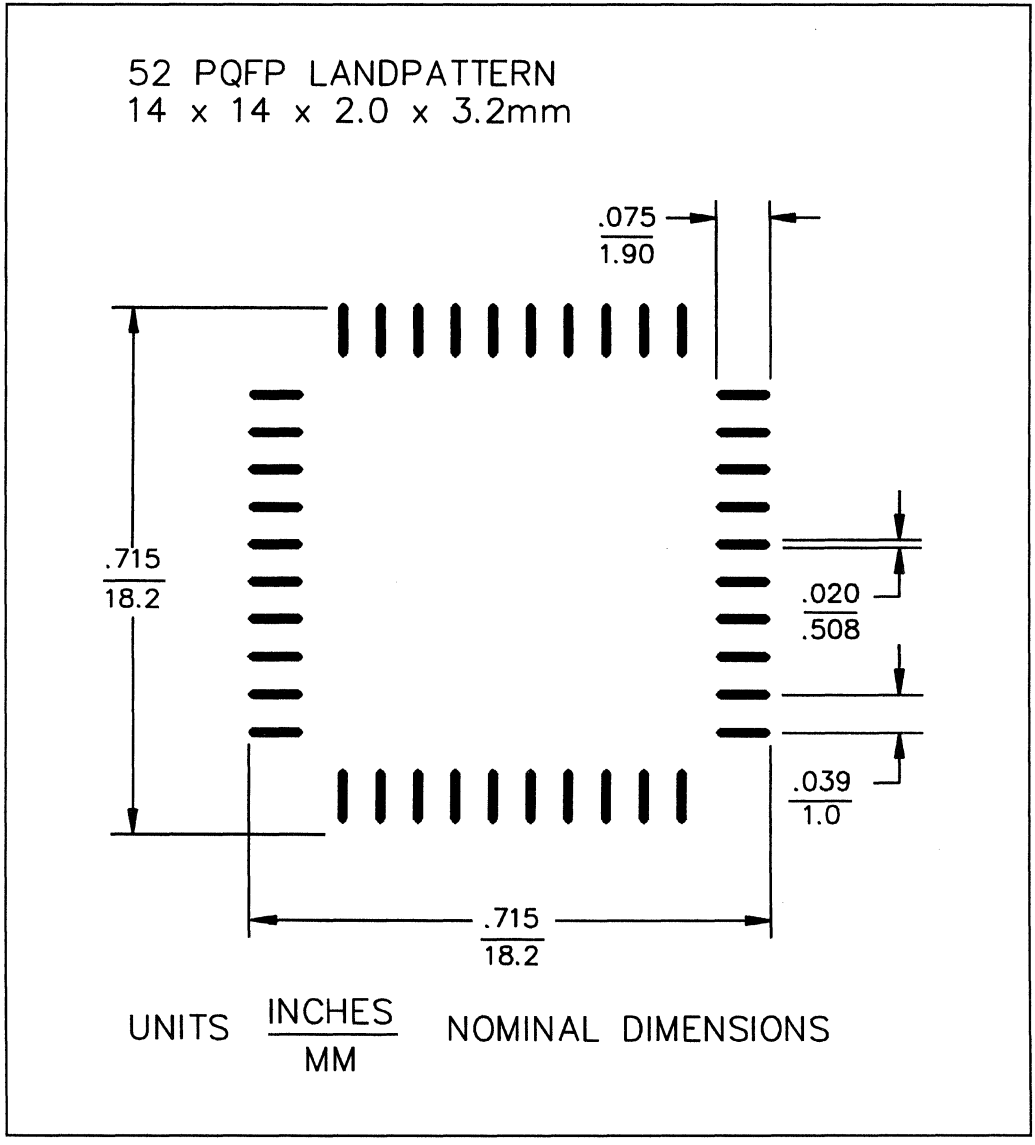

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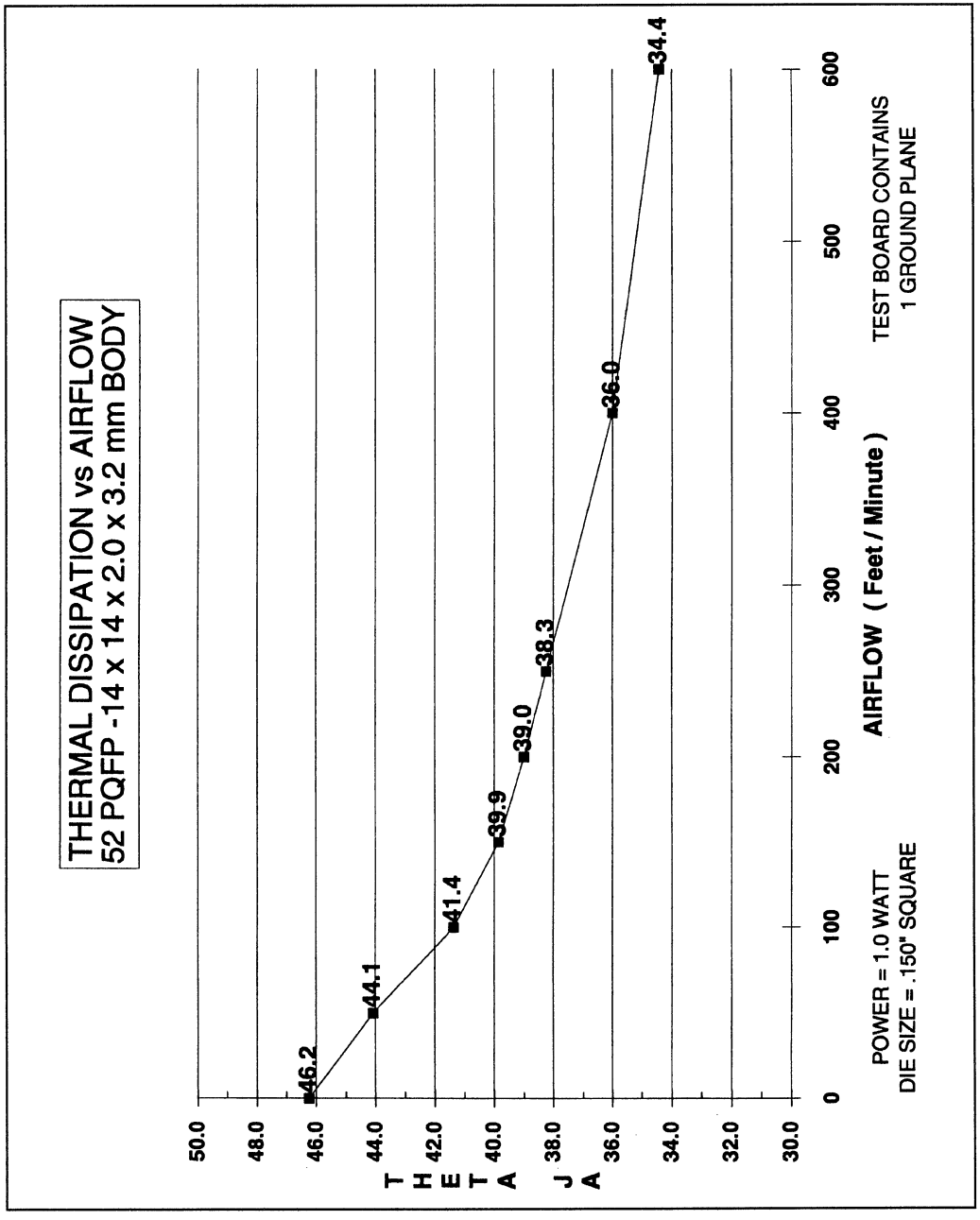
THERMAL DISSIPATION vs AIRFLOW
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THETA JA
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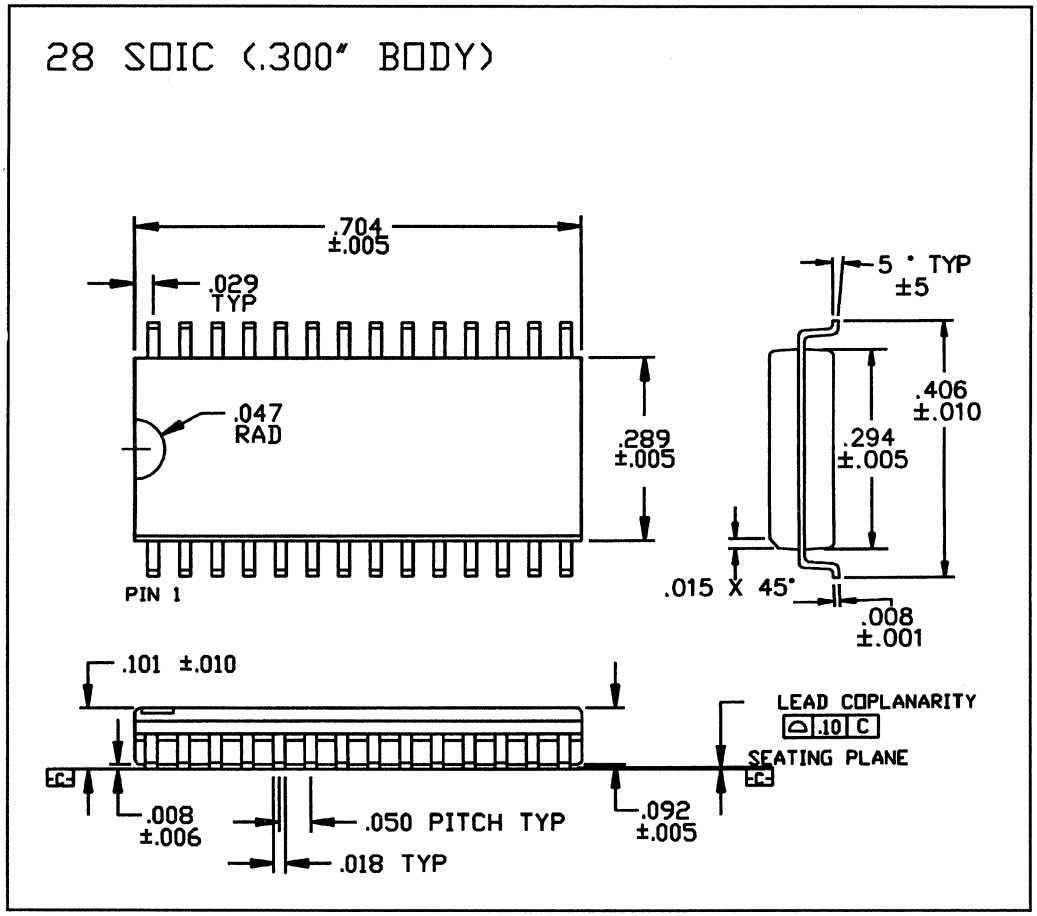
100
200
300
400
500
600
AIRFLOW (Feet / Minute)
POWER = 1.0 WATT
DIE SIZE = .150" SQUARE
TEST BOARD CONTAINS
1 GROUND PLANE

28-PIN SOIC MECHANICAL DIMENSIONS



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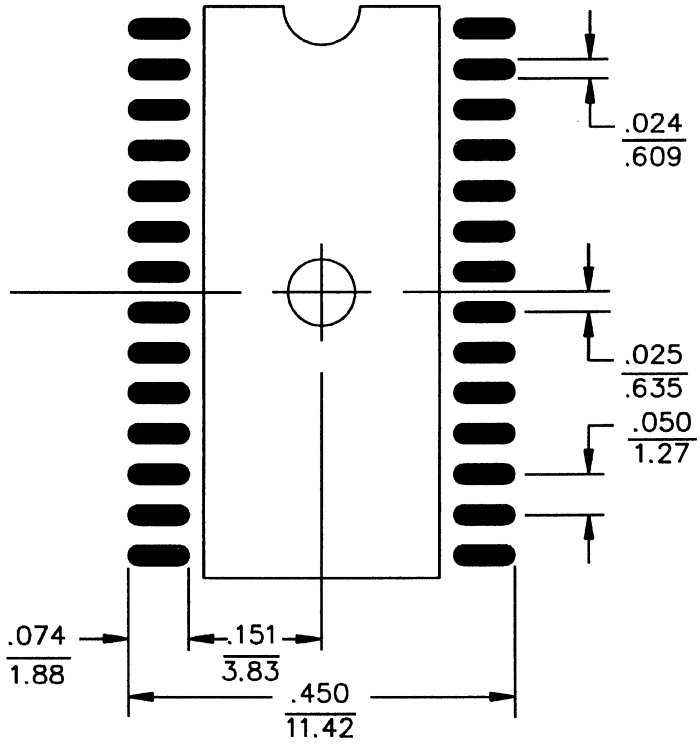
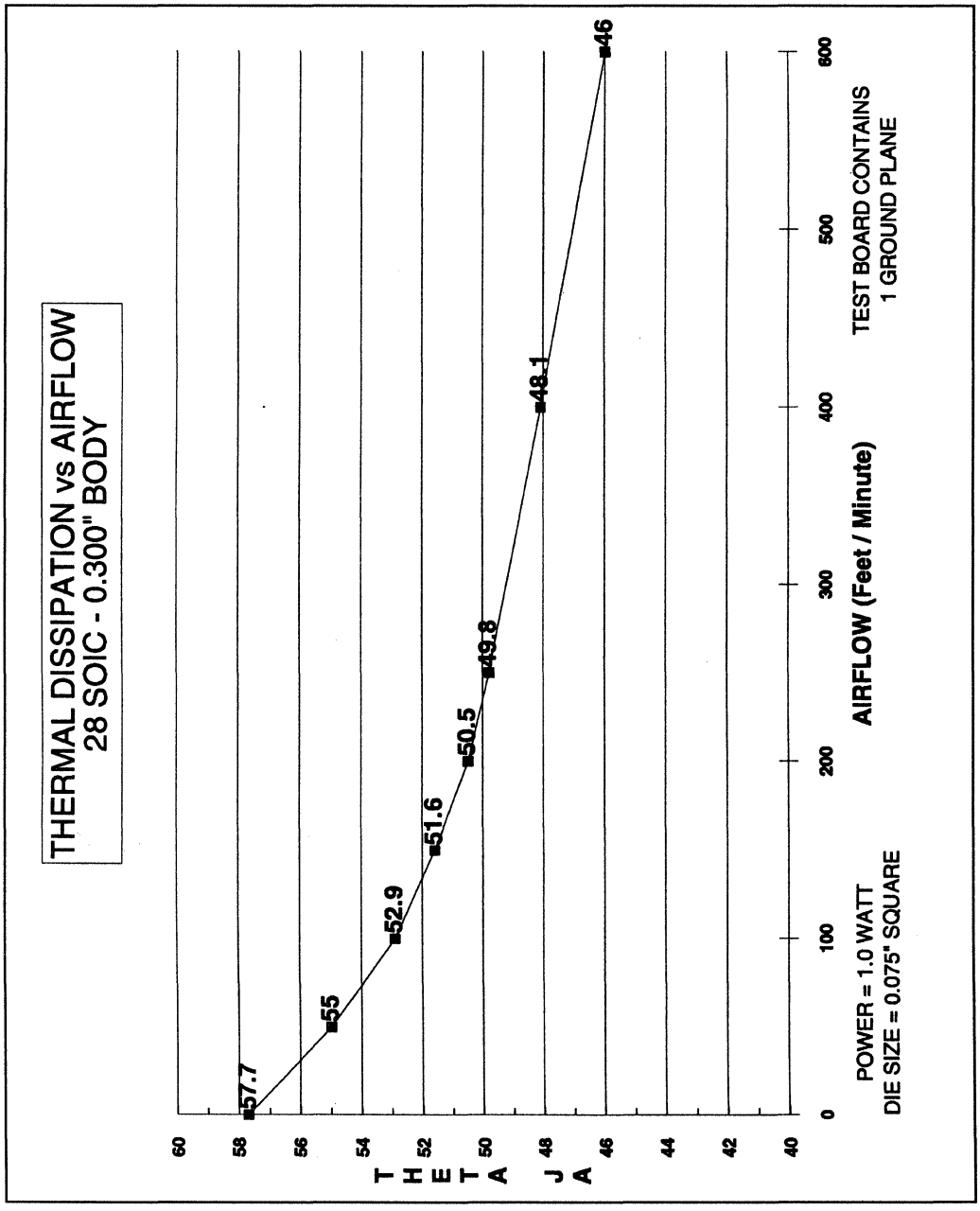
28 SOIC (.300" BODY) LANDPATTERN



UNITS $\frac{\text{INCHES}}{\text{MM}}$ NOMINAL DIMENSIONS

6

28-PIN SOIC MECHANICAL DIMENSIONS



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CONTENTS

5V CLOCK GENERATORS AND SYNTHESIZERS

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FEATURES

- Generates six clock outputs from 20 MHz to 80 MHz (the S4403 generates ten outputs and HFOUT generates 10MHz to 40MHz)
- 21 selectable phase/frequency relationships for the clock outputs
- Compensates for clock skew by allowing output delay adjustment down to 3.125 ns increments
- TTL outputs have less than 400 ps maximum skew
- Lock Detect output indicates loop status
- Internal PLL with VCO operating at 160 to 320 MHz
- Test Enable input allows VCO bypass for open-loop operation in board test
- Maximum 1.0 ns of phase error (750 ps from part to part)
- Proven 1.0 micron BiCMOS technology
- Single +5V power supply operation
- 28/44 PLCC packages

APPLICATIONS

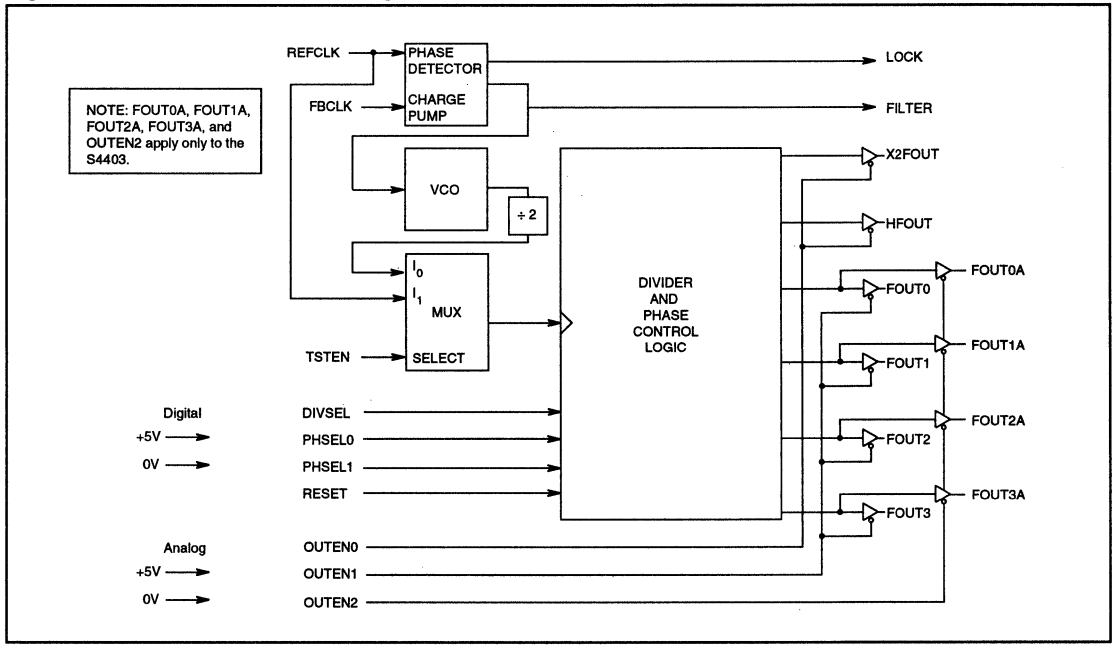
- CMOS ASIC Systems
- High-speed Microprocessor Systems
- Backplane Clock Deskew and Distribution

GENERAL DESCRIPTION

The S4402/S4403 BiCMOS clock generators allow the user to generate multiphase TTL clocks in the 10–80 MHz range with less than 400 ps of skew. Use of a single off-chip filter allows an entire 160–320 MHz phase-locked loop (PLL) to be implemented on-chip. Divide-by-two and times-two outputs allow the ability to generate output clocks at half, equal to, or twice the reference clock input frequency. By using the programmable divider and phase selector, the user can select from up to 21 different output relationships. The outputs can be phase-adjusted in increments as small as 3.125 ns to tailor the clocks to exact system requirements.

Implemented in AMCC's proven 1.0 micron BiCMOS technology, the S4402 generates six TTL outputs, while the S4403 provides those six plus four duplicates (FOUT0A–FOUT3A) for a total of ten. Output enables are provided for the various banks, allowing clock control for board and system tests.

Figure 1. Clock Generator Block Diagram



FUNCTIONAL DESCRIPTION

Frequency and Phase Controls

The S4402/S4403 clock generators provide multiple outputs that are synchronized in both frequency and phase to a periodic clock input. Two select pins and an external feedback path allow the user to phase-adjust the six outputs (FOUT0–FOUT3, HFOUT, and X2FOUT) relative to the input clock REFCLK, as well as control their frequency.

The DIVSEL input controls the programmable divider that follows the voltage controlled oscillator (VCO). This doubles the lock range of the PLL by allowing the user to select a VCO frequency divided by four (DIVSEL Low) or by eight (DIVSEL High).

The frequency of the four FOUT0–FOUT3 outputs (and the duplicate set of the four FOUT0A–FOUT3A outputs on the S4403) is determined by the REFCLK clock frequency and the output that is tied back to the FBCLK input. In addition, the X2FOUT TTL output provides a clock signal identical to the FOUT0 output in the divide-by-four mode, and twice the FOUT0 frequency (maximum frequency of 80 MHz) in the divide-by-eight mode. The HFOUT TTL output provides a clock signal that is in phase with the FOUT0 output, but at half the FOUT0 frequency in both the divide-by-four and divide-by-eight modes. Refer to the Output Select Matrix in Table 3 for the specific relationships.

Phase adjustments can be made in increments as small as 3.125 ns. The minimum phase delay between FOUT0–FOUT3 signals is a function of the VCO frequency. The VCO frequency can be determined by multiplying the output frequency by the divide-by ratio of four or eight, controlled by DIVSEL. The minimum phase delay t is equal to the period of the VCO frequency:

$$t = 1 / \text{VCO freq}$$

Since the VCO can operate in the 160 MHz to 320 MHz range, minimum phase delay values can range from 6.25 ns to 3.125 ns. Table 1 shows various FOUT/VCO frequencies and the associated phase resolution.

The PHSEL1 and PHSEL0 inputs allow the user to select several phase relationships among the four FOUT0–FOUT3 TTL clock outputs. These choices can be seen in Table 2, and the Output Select Matrix provided in Table 3 describes the 21 output configurations available to the user. The two "Select Pins" columns specify the signal levels on the pins PHSEL0 and PHSEL1. These are active High signals. The column entitled "Output Fed to FBCLK" indicates which output (FOUT0–FOUT3, HFOUT, or X2FOUT) is externally connected to the feedback input (FBCLK) to produce the resulting waveforms shown in the appropriate row in the table. The last seven columns specify the resulting phase and frequency relationships of each output to the user clock input (REFCLK). A negative value indicates the time by which the output rising edge precedes the input (REFCLK) rising edge. A positive value is the time by which the rising edge of the output follows the rising edge of the input clock.

Table 1. Example Phase Resolution

FOUT0–3 Freq	Divider Select	VCO Freq	Min Phase Resolution
80 MHz	4	320 MHz	3.125 ns
66 MHz	4	266 MHz	3.75 ns
50 MHz	4	200 MHz	5.0 ns
40 MHz	4	160 MHz	6.25 ns
40 MHz	8	320 MHz	3.125 ns
33 MHz	8	266 MHz	3.75 ns
25 MHz	8	200 MHz	5.0 ns
20 MHz	8	160 MHz	6.25 ns

Table 2. Phase Selections

PHSEL1	PHSEL0	Phase Relationship
0	0	All at same phase
0	1	FOUT0–FOUT3 outputs skewed by 90 degrees from each other
1	0	FOUT1 leads FOUT0 by minimum phase, FOUT2 lags FOUT0 by minimum phase, and FOUT3 lags FOUT0 by 90 degrees
1	1	FOUT1 lags FOUT0 by minimum phase, FOUT2 lags FOUT1 by minimum phase, and FOUT3 lags FOUT2 by minimum phase

Example:

In a typical system, designers may need several low-skew outputs, one early clock, one late clock, a clock at half the input clock frequency, and one at twice the input clock frequency. This system requirement can be met by setting PHSEL1 to 1, PHSEL0 to 0, and feeding back FOUT0 to the FBCLK input (Row 10 of Table 3). The result is that FOUT0 will be phase-aligned to REFCLK, FOUT1 will lead REFCLK by a minimum phase delay, FOUT2 will lag REFCLK by a minimum phase delay, FOUT3 will phase-lag REFCLK by 90°, HFOUT will be phase-aligned with REFCLK but at half the frequency, and X2FOUT will be either phase-aligned at the same frequency as the reference clock if DIVSEL = 0, or at twice the frequency if DIVSEL = 1.

Several other waveform examples and typical applications are provided on pages 7-8 and 7-9.

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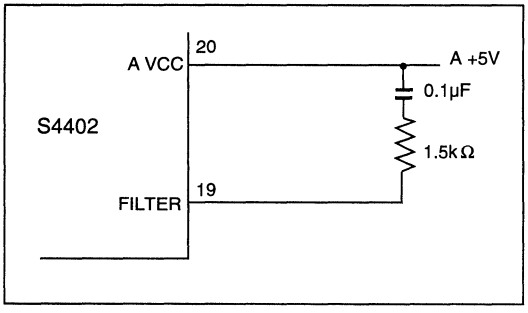
Enabling Outputs

The S4402 has two output-enable inputs that control which outputs toggle. (The S4403 has three output-enable inputs.) When held LOW, OUTEN0 controls the frequency doubler output X2FOUT and the half-frequency output HFOUT. OUTEN1 controls the FOUT0–FOUT3 outputs. The third input on the S4403, OUTEN2, controls the duplicate set of four outputs FOUT0A–FOUT3A. When an output enable pin is held High, its associated outputs are disabled and held in a High state.

Filter

The FILTER output is a tap between the analog output of the phase detector and the VCO input. This pin allows a simple external filter (Figure 2) to be included in the PLL. AMCC recommends the use of the filter component values shown. This filter was chosen for its ability to reduce the output jitter and filter out noise on the REFCLK input. The filter components should be in surface mounted packages with minimum lead inductance.

Figure 2. External PLL Filter



Reset

When the RESET pin is pulled low, all the internal states go to zero one clock cycle (from the VCO or REFCLK in the test mode) before the outputs go low. After the chip is reset, the PLL requires a resynchronization time of ≤5ms before lock is again achieved.

Lock Detect

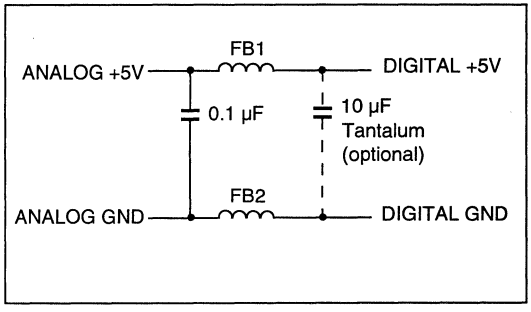
A lock detect function is provided by the LOCK output. When REFCLK and FBCLK are within 2–4 ns of each other, the PLL is in lock, and the LOCK output goes High.

Power Supply Considerations

Power for the analog portion of the S4402/S4403 chips must be isolated from the digital power supplies to minimize noise on the analog power supply pins. This isolation between the analog and digital power supplies can be accomplished with a simple external power supply filter (Figure 3). The analog power planes are connected to the digital power planes through single ferrite beads (FB1 and FB2) or inductors capable of handling 25 mA. The recommended value for the inductors is in the range from 5 to 100µH, and depends upon the frequency spectrum of the digital power supply noise. The ferrite beads should exhibit 75Ω impedance at 10 MHz.

Decoupling capacitors are also very important to minimize noise. The decoupling capacitors must have low lead inductance to be effective, so ceramic chip capacitors are recommended. Decoupling capacitors should be located as close to the power pins as physically possible. And the decoupling should be placed on the top surface of the board between the part and its connections to the power and ground planes.

Figure 3. External Power Supply Filter



Test Capabilities

The TSTEN input puts the S4402/S4403 into a test mode and allows users to bypass the VCO and provide their own clock through the REFCLK input. When TSTEN is High, the VCO is turned off and the REFCLK signal drives the divider/phase adjust circuitry, directly sequencing the outputs. The TSTEN and REFCLK inputs join the divider circuitry after the initial divide-by-two stage. Therefore, REFCLK is divided by two in the divide-by-four mode and divided by four in the divide-by-eight mode.

PIN DESCRIPTIONS

Input Signals

REFCLK. Frequency reference supplied by the user that, along with the output tied to the FBCLK input, determines the frequency of the FOUT0–FOUT3 outputs. Also replaces the VCO output when TSTEN is high (after first divide-by-two stage in divider phase control logic). See TSTEN.

FBCLK. Feedback clock that, along with the REFCLK input, determines the frequency of the FOUT0–FOUT3 outputs. One output is selected to feed back to this input. (See Table 3.)

DIVSEL. Controls the divider circuit that follows the VCO. When DIVSEL is low, the VCO frequency is divided by four. When DIVSEL is high, the VCO frequency is divided by eight. (See Tables 1 and 3.)

PHSEL0. This input, along with PHSEL1, allows selection of the phase relationship among the four FOUT0–FOUT3 outputs. See Tables 2 and 3 for the selection choices.

PHSEL1. Along with PHSEL0, allows selection of the phase relationship among the four FOUT0–FOUT3 outputs. See Tables 2 and 3 for the selection choices.

OUTEN0. Active Low. Output enable signal that controls which outputs toggle. Controls the frequency doubler output (X2FOUT) and the half-frequency output (HFOUT).

OUTEN1. Active Low. Output enable signal that controls which outputs toggle. Controls the FOUT0–FOUT3 outputs.

OUTEN2. (S4403 only.) Active Low. Controls the duplicate set of outputs to FOUT0–FOUT3 (FOUT0A, FOUT1A, FOUT2A, AND FOUT3A).

RESET. Active Low. Initializes internal states for test purposes.

TSTEN. Active High. Allows REFCLK to drive the divider phase adjust circuitry, after the first divide-by-two stage. Therefore, REFCLK is divided by two in the divide-by-four mode, and divided by four in the divide-by-eight mode, and used to directly sequence the outputs.

Output Signals

FILTER. A tap between the analog output of the phase detector and the VCO input. Allows a simple external filter (a single resistor and one capacitor) to be included in the PLL.

X2FOUT. Provides a clock signal identical to the FOUT0 output in the divide-by-four mode and twice the FOUT0 frequency (maximum of 80 MHz) in the divide-by-eight mode.

FOUT0. Clock output.

FOUT1. Clock output.

FOUT2. Clock output.

FOUT3. Clock output.

HFOUT. Provides a clock signal in phase with the FOUT0 output, but at half the FOUT0 frequency in both the divide-by-four and divide-by-eight modes.

LOCK. Goes high when REFCLK and FBCLK are within 2–4 ns of each other, demonstrating that the PLL is in lock.

FOUT0A. (S4403 only.) Clock output—duplicates FOUT0.

FOUT1A. (S4403 only.) Clock output—duplicates FOUT1.

FOUT2A. (S4403 only.) Clock output—duplicates FOUT2.

FOUT3A. (S4403 only.) Clock output—duplicates FOUT3.

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Table 3. Output Select Matrix

Configuration Number	Select Pins		Output Fed to FBCLK	Output Phase Relationships					÷4	÷8
	PHSEL1	PHSEL0		FOUT0	FOUT1	FOUT2	FOUT3	HFOUT	X2FOUT	
1	0	0	FOUT0–FOUT3	0	0	0	0	0/2	0	2(0)
2	0	0	HFOUT	2(0)	2(0)	2(0)	2(0)	0	2(0)	4(0)
3	0	0	X2FOUT (÷8)	0/2	0/2	0/2	0/2	0/4		0
4	0	1	FOUT0	0	Q	2Q	3Q	0/2	0	2(0)
5	0	1	FOUT1	–Q	0	Q	2Q	–Q/2	–Q	2(–Q)
6	0	1	FOUT2	–2Q	–Q	0	Q	–2Q/2	–2Q	2(–2Q)
7	0	1	FOUT3	–3Q	–2Q	–Q	0	–3Q/2	–3Q	2(–3Q)
8	0	1	HFOUT	2(0)	2(Q)	2(2Q)	2(3Q)	0	2(0)	4(0)
9	0	1	X2FOUT (÷8)	0/2	Q/2	2Q/2	3Q/2	0/4		0
10	1	0	FOUT0	0	–t	t	Q	0/2	0	2(0)
11	1	0	FOUT1	t	0	2t	Q+t	t/2	t	2(t)
12	1	0	FOUT2	–t	–2t	0	Q–t	–t/2	–t	2(–t)
13	1	0	FOUT3	–Q	–Q–t	–Q+t	0	–Q/2	–Q	2(–Q)
14	1	0	HFOUT	2(0)	2(–t)	2(t)	2(Q)	0	2(0)	4(0)
15	1	0	X2FOUT (÷8)	0/2	–t/2	t/2	Q/2	0/4		0
16	1	1	FOUT0	0	t	2t	3t	0/2	0	2(0)
17	1	1	FOUT1	–t	0	t	2t	–t/2	–t	2(–t)
18	1	1	FOUT2	–2t	–t	0	t	–2t/2	–2t	2(–2t)
19	1	1	FOUT3	–3t	–2t	–t	0	–3t/2	–3t	2(–3t)
20	1	1	HFOUT	2(0)	2(t)	2(2t)	2(3t)	0	2(0)	4(0)
21	1	1	X2FOUT (÷8)	0/2	t/2	2t/2	3t/2	0/4		0

Notes:
1. "0" implies the output is aligned with REFCLK.
2. "t" implies the output lags REFCLK by a minimum phase delay.
3. "Q" implies the output lags REFCLK by 90° of phase
4. "–t" implies the output leads REFCLK by a minimum phase delay.
5. "–Q" implies the output leads REFCLK by 90° of phase.
6. "2( )" implies the output is at twice the frequency of REFCLK.

7

Legend

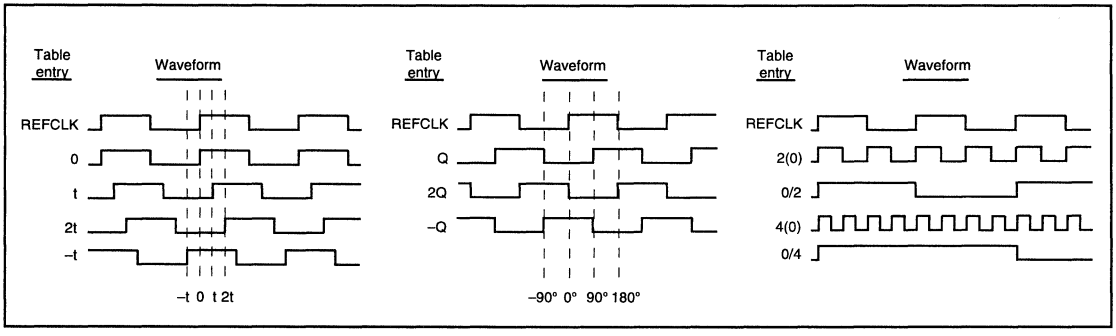
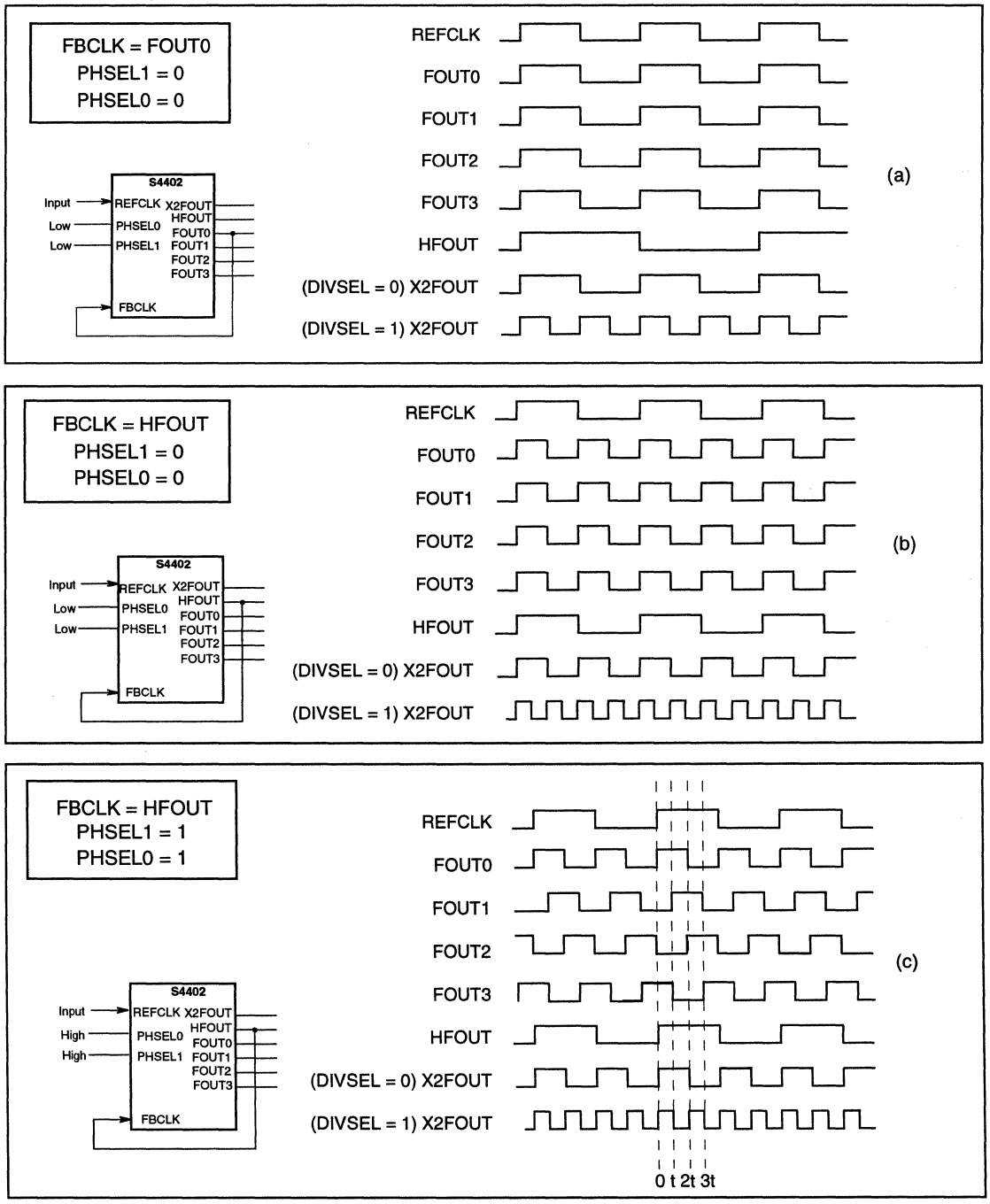


Figure 4. Configuration Examples



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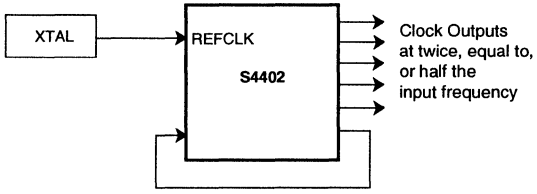
TYPICAL APPLICATIONS

The S4402/S4403 chips are designed to meet a large variety of system clocking requirements. Several typical applications are provided below.

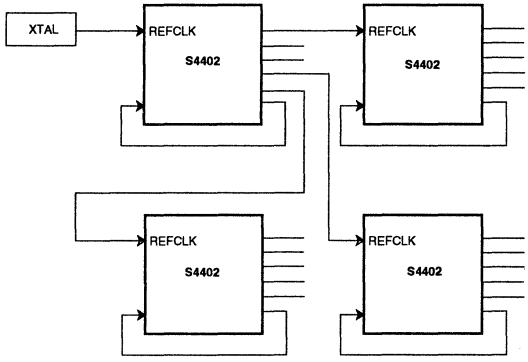
Application 1. High-Frequency, Low-Skew Clock Generation

One of the most basic capabilities of the S4402/S4403 devices is generating multiple phase-aligned low-skew clocks at various multiples of the input clock frequency. For example, in a multiple-board system a half-frequency clock can be generated for use across the backplane, where it is simpler to route a low-speed signal. This signal can then be doubled on the boards, and synchronization will be maintained.



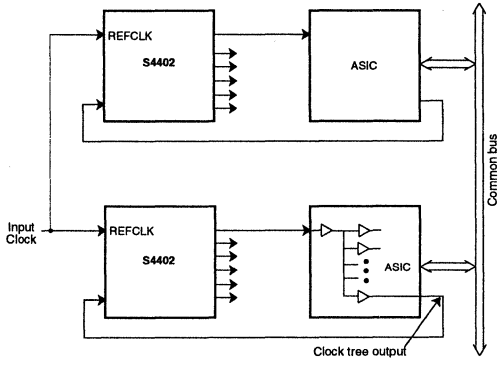
Application 2. Low-Skew Clock Distribution

One common problem in clocking high-speed systems is that of distributing several copies of a system clock while maintaining low skew throughout the system. The S4402/S4403 devices guarantee low skew among all the clocks in the system, as they have effectively zero delay between their input and output signals, with an output skew of less than 400 ps. The user can also adjust the phases of the outputs in increments as small as 3.125 ns, for load and trace length matching.



Application 3. Delay Compensation

Since the relative edges of the S4402/S4403 outputs can be precisely controlled, these chips can be used to compensate for different delays due to trace lengths or to internal chip delays, simplifying board layout and bus timing. In the example shown, the two ASICs have a difference of several nanoseconds in their propagation delays. The S4402s ensure that the output signals are aligned, so that the data valid uncertainty on the common bus is minimized.



7

ABSOLUTE MAXIMUM RATINGS

	Commercial
TTL Supply Voltage VCC (VEE = 0)	7.0 V
TTL Input Voltage (VEE = 0)	5.5 V
Operating Temperature	0°C to 70°C ambient
Operating Junction Temperature TJ	+ 130°C
Storage Temperature	–65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Commercial			Units
	Min	Nom	Max	
TTL Supply Voltage (VCC)	4.75	5.0	5.25	V
Operating Temperature	0 (ambient)	—	70 (ambient)	°C
Junction Temperature	—	—	130	°C

DC CHARACTERISTICS

Symbol	Parameter	DC Test Conditions		Min	Typ[1]	Max	Units
V_{IH}[2]	Input HIGH voltage	Guaranteed input HIGH voltage for all inputs		2.0			V
V_{IL}[2]	Input LOW voltage	Guaranteed input LOW voltage for all inputs				0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} = Min, I_{IN} = -18mA			-0.8	-1.2	V
V_{OH}	Output HIGH voltage	V_{CC} = Min	I_{OH} = -12mA[3] (COM)	2.4			V
			I_{OH} = -24mA[3] (COM)	2.0			V
V_{OL}	Output LOW voltage	V_{CC} = Min	I_{OL} = 24mA[3] (COM)			0.5	V
I_{IH}	Input HIGH current	V_{CC} = Min, V_{IN} = 2.4V	OUTEN2			-200	µA
			Other			50	µA
I_I	Input HIGH current at max	V_{CC} = Max, V_{IN} = V_{CC}				1.0	mA
I_{IL}	Input LOW current	V_{CC} = Min, V_{IN} = 0.5V	OUTEN2			-500	µA
			Other			-50	µA
I_{OS}[4]	Output short circuit current	V_{CC} = Max, V_{OUT} = 0V		-25		-100	mA
I_{CC}	Static	V_{CC} = Max	COM			70	mA
I_{CC}	Total I_{CC} (Dynamic and Static)	V_{LOAD} = 25pF at 50 MHz	COM			190	mA

1. Typical limits are at 25°C, V_{cc} = 5.0V.
2. These input levels should only be tested in a static, noise-free environment.
3. I_{OH}/I_{OL} values indicated are for DC test correlation. Actual dynamic currents are significantly higher and are optimized to balance rise and fall times.
4. Maximum test duration is one second.

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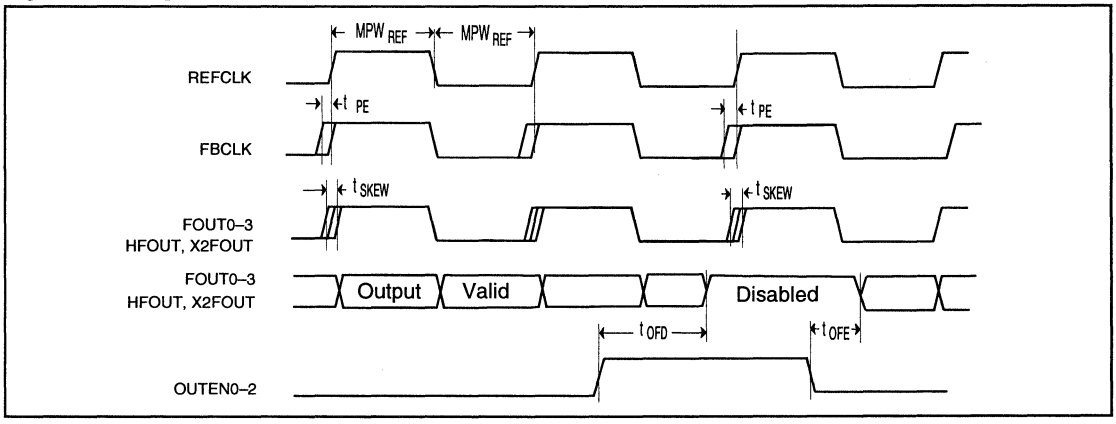
Table 4. AC Specifications

Symbol	Description	S4402/3-66		S4402/3-80		Units
		Min	Max	Min	Max	
f_{VCO}	VCO Frequency	160	266	160	320	MHz
f_{REF}	REFCLK Frequency	10	66	10	80	MHz
MPW_{REF}	REFCLK Minimum Pulse Width	7.0		6.0		ns
t_{PE}	Phase Error between REFCLK and FBCLK	-1.0	0	-1.0	0	ns
t_{PED}	Phase Error Difference from Part to Part[1]	0	750	0	750	ps
t_{SKEW}	Output Skew[2]	0	400	0	400	ps
t_{DC}	Output Duty Cycle[3]	45	55	45	55	%
f_{FOUT}	FOUT Frequency[4]	20	66	20	80	MHz
f_{HFOUT}	HFOUT Frequency[4]	10	33	10	40	MHz
f_{2XFOUT}	2XFOUT Frequency[4]	40	66	40	80	MHz
t_{PS}	Nominal Phase Shift Increment	3.75	6.25	3.125	6.25	ns
t_{PSJ}	Phase Shift Variation[5]	-250	+250	-250	+250	ps
t_{OFD}	Tpd OUTEN0–2 to FOUTs, Disable	2	7	2	7	ns
t_{OFE}	Tpd OUTEN0–2 to FOUTs, Enable	2	7	2	7	ns
t_{IRF}	Input Rise/Fall Time	1	3	1	3	ns
t_{ORF}	FOUT Rise/Fall Time[6]	0.5	1.5	0.5	1.5	ns
t_{LOCK}	Loop Acquisition Time[7]		5		5	ms
t_j	Clock Stability[8]		500		500	ps

1. Difference in phase error between two parts at the same voltage, temperature and frequency.
2. Output skew guaranteed for equal loading at each output.
3. Outputs loaded with 35pF, measured at 1.5V.
4. C_{LOAD} = 35 pF.
5. All phase shift increments and variation are measured relative to FOUT0 at 1.5V.
6. With 35 pF output loading (0.8 V to 2.0 V transition).
7. Depends on loop filter chosen. (Number given is for example filter.)
8. Clock period jitter with all FOUT outputs operating at 66 MHz and loaded with 25pF using loop filter shown. Parameter guaranteed, but not tested.

Figure 5. Timing Waveforms

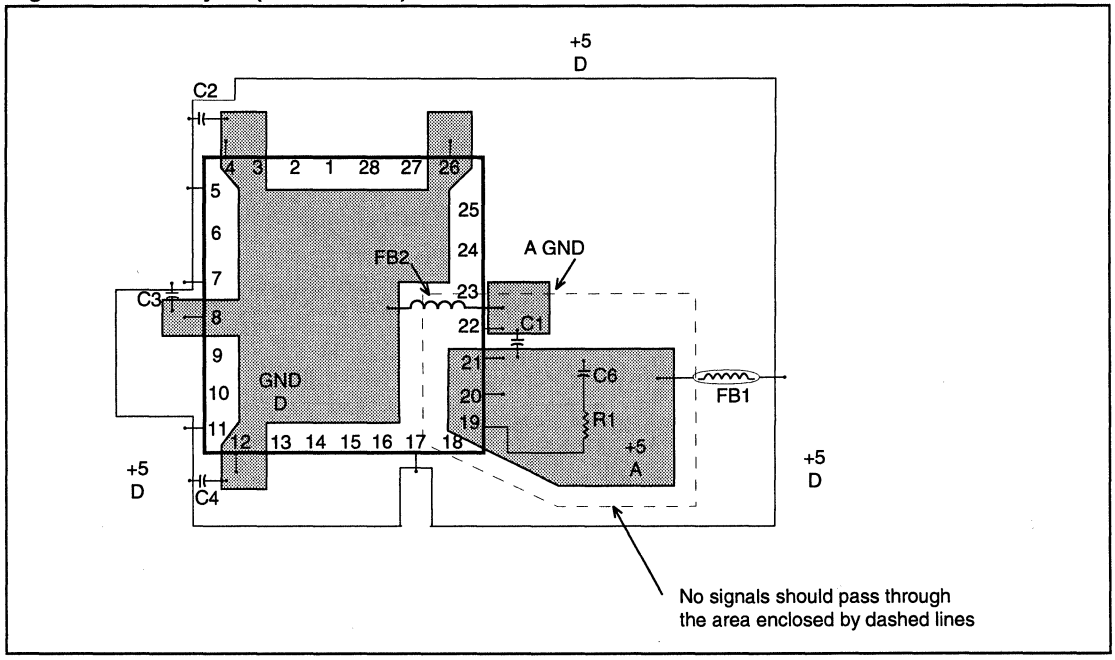


7

BOARD LAYOUT CONSIDERATIONS

- The S4402/S4403 chips are sensitive to noise on the Analog +5 V and Filter pins. Care should be taken during board layout for optimum results.
- All decoupling capacitors (C1–C4 = 0.1 µF) should be bypassed between VCC and GND, and placed as close to the chip as possible (preferably using ceramic chip caps) and placed on top of board between S4402/S4403 and the power and ground plane connections.
- No dynamic signal lines should pass through or beneath the filter circuitry area (enclosed by dashed lines in Figure 6) to avoid the possibility of noise due to crosstalk.
- The analog VCC supply can be a filtered digital VCC supply as shown below. The ferrite beads or inductors, FB1 and FB2, should be placed within three inches of the chip.
- The analog VCC plane should be separated from the digital VCC and ground planes by at least 1/8 inch.

Figure 6. Board Layout (S4402 shown)



Component	Description
C1–C4	0.1 µF ceramic capacitor
C6	0.1 µF ceramic capacitor
R1	1.5 K 10% resistor
FB1,FB2	Ferrite bead or inductor

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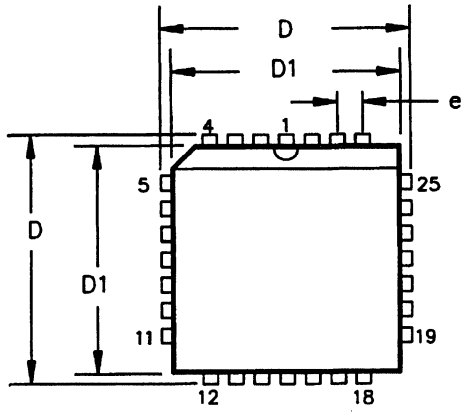
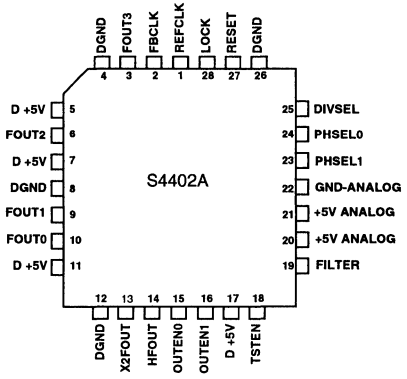
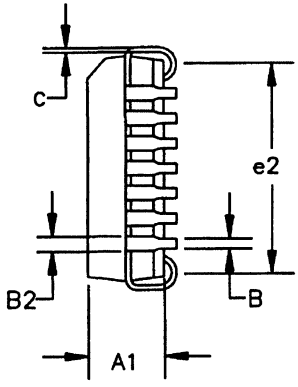
Figure 7. S4402 28 PLCC Package and Pinout







SYM	MIN	MAX
A1	.147	.157
B	.013	.021
B2	.026	.032
C	.007	.013
D	.487	.497
D1	.444	.459
e	.048	.052
e2	.410	.430

All dimensions nominal in inches.

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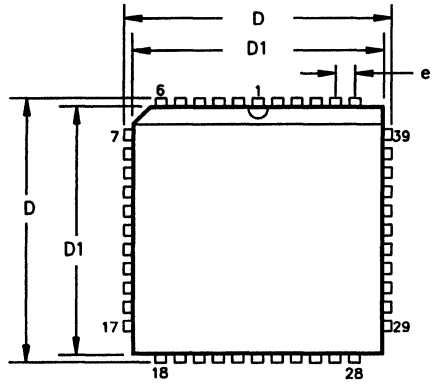
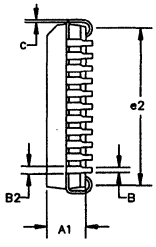
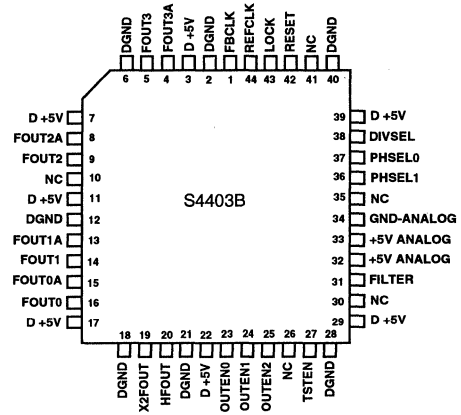
28 PLCC Thermal Resistance

Still Air	100 Linear Ft./Min	200 Linear Ft./Min
60°C/Watt	50°C/Watt	45°C/Watt

Figure 8. S4403 44 PLCC Package and Pinout







SYM	MIN	MAX
A1	.147	.157
B	.013	.021
B2	.026	.032
C	.007	.013
D	.687	.697
D1	.644	.659
e	.048	.052
e2	.610	.630

All dimensions nominal in inches.

Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Speed Option**
- **Optional Shipping Configuration**

S4402/03 **A** **– 66** **/TD**

Optional Shipping Configuration
Blank = tube
/D = dry pack
/TD = tape, reel and dry pack

Speed Option
– 66 = 66 MHz
– 80 = 80 MHz

Package Option
A = 28-pin PLCC (S4402)
B = 44-pin PLCC (S4403)

Device Number
S4402
S4403

Example: S4402A-66/D
28-pin PLCC package, shipped dry packed in the standard tube.

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BiCMOS PECL CLOCK GENERATOR S4405

FEATURES

- Generates six clock outputs from 20 MHz to 80 MHz (HFOUT operates from 10 MHz to 40 MHz)
- Allows PECL or TTL reference input
- Provides differential PECL output at up to 160 MHz
- 21 selectable phase/frequency relationships for the clock outputs
- Compensates for clock skew by allowing output delay adjustment down to 3.125 ns increments
- TTL outputs have less than 400 ps maximum skew
- Lock Detect output indicates loop status
- Internal PLL with VCO operating at 160 to 320 MHz
- Test Enable input allows VCO bypass for open-loop operation
- Maximum 1.0 ns of phase error (750 ps from part to part)
- Proven 1.0 micron BiCMOS technology
- Single +5V power supply operation
- 44 PLCC package

APPLICATIONS

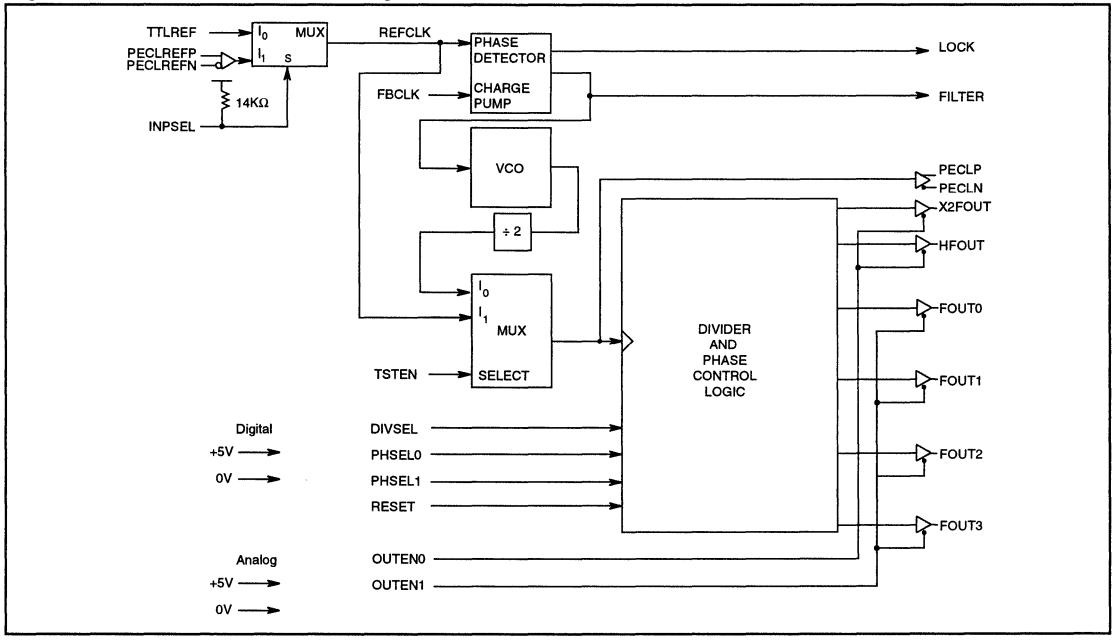
- CMOS ASIC Systems
- High-speed Microprocessor Systems
- Backplane Clock Deskew and Distribution

GENERAL DESCRIPTION

The S4405 BiCMOS clock generators allow the user to generate multiphase TTL clocks in the 10–80 MHz range with less than 400 ps of skew. Use of a simple off-chip filter allows an entire 160–320 MHz phase-locked loop (PLL) to be implemented on-chip. Divide-by-two and times-two outputs allow the ability to generate output clocks at half, equal to, or twice the reference clock input frequency. The reference is selectable to be either TTL or PECL. By using the programmable divider and phase selector, the user can select from up to 21 different output relationships. The outputs can be phase-adjusted in increments as small as 3.125 ns to tailor the clocks to exact system requirements.

Implemented in AMCC's proven 1.0 micron BiCMOS technology, the S4405 generates six TTL outputs and one differential PECL output. Output enables are provided for the various TTL banks, allowing clock control for board and system tests.

Figure 1. Clock Generator Block Diagram



FUNCTIONAL DESCRIPTION

This BiCMOS clock generator is designed to allow the user to generate TTL clocks, in the 10–80 MHz range, with less than 400 ps of skew. Implemented in AMCC's 1.0µ BiCMOS technology, the internal VCO, phase detector, and programmable divider and phase selector allow the user to tailor the TTL output clocks for his/her system needs. The internal VCO can operate between 160 to 320 MHz, and the programmability allows the user to generate TTL output clocks in the 10–80 MHz range, and a differential +5V referenced ECL output at 80–160 MHz.

The clock generator offers the user the ability to select the appropriate phase relationship among the four FOUT0–3 TTL clock outputs. The phase selection choices are shown in Table 2.

The clock generator also allows the user to choose the divide-by ratio between the VCO frequency and the frequency of the FOUT0–3 signals. The VCO frequency can be divided by 4 when DIVSEL is low, and divided by 8 when DIVSEL is high. The divide ratio between the VCO and the pseudo ECL outputs, PECLP and PECLN, is a fixed divide-by-2.

The clock generator also has two output enable inputs which can be used to control which outputs toggle. OUTEN0 controls the HFOUT and X2FOUT outputs, and OUTEN1 controls the FOUT0–3 outputs. When the output enables are high, the outputs are disabled, and held in a high state.

REFCLK can be driven by either the TTLREF or PECLREF inputs. The reference clock source is selected with the INPSEL input. When INPSEL is low, the TTLREF input is selected as the reference clock.

The FOUT0–3 outputs are the main TTL output clocks that the generator supplies. The frequency of these outputs is determined by the REFCLK clock frequency and the output clock that is tied to the FBCLK input. FOUT0–3 will be equal to REFCLK, half of REFCLK, or twice the frequency of REFCLK. The X2FOUT TTL output provides a clock signal that is identical to the FOUT0 output in the divide-by-4 mode, but twice the FOUT0 frequency (max. freq. of 66 MHz) in the divide-by-8 mode. The HFOUT TTL output provides a clock signal that is also in phase with the FOUT0 output, but at half the FOUT0 frequency.

FILTER is the analog signal from the phase detector going into the VCO. This pin is provided so a simple external filter (a single resistor and one capacitor) can be included in the phase-locked loop of the clock generator.

The LOCK output goes high when the reference clock and FBCLK are within 2–4 ns of each other. This output tells the user that the PLL is in lock.

Three pins are included for test purposes. TESTEN allows the chip to use the REFCLK signal instead of the VCO output to clock the chip. This is used during chip test to allow the counters and control logic to be tested independently of the VCO. The RESET pin initializes the internal counter flip-flops to zeros, but several clock cycles are necessary before the outputs go to a zero state.

The minimum phase delay between FOUT0–3 signals is a function of the VCO frequency. The VCO frequency can be determined by multiplying the output frequency by the divide-by ratio of four or eight. The minimum phase delay is equal to the period of the VCO frequency: M_p = 1/VCO freq. Since the VCO can operate in the 160 MHz to 320 MHz range, the range of minimum phase delay values is 6.25 ns to 3.125 ns. Table 1 shows various FOUT/VCO frequencies and the associated phase resolution.

The charge pump and VCO portion of the chip use a separate analog power supply. This supply is brought onto the chip through a distinct set of power and ground pins. This supply should be free of digital switching noise.

Example:

In a typical system, designers may need several low-skew outputs, one early clock, one late clock, a clock at half the input clock frequency, and one at twice the input clock frequency. This system requirement

Table 1. Example Phase Resolution

FOUT0–3 Freq	Divider Select	VCO Freq	Min Phase Resolution
80 MHz	4	320 MHz	3.125 ns
66 MHz	4	266 MHz	3.75 ns
50 MHz	4	200 MHz	5.0 ns
40 MHz	4	160 MHz	6.25 ns
40 MHz	8	320 MHz	3.125 ns
33 MHz	8	266 MHz	3.75 ns
25 MHz	8	200 MHz	5.0 ns
20 MHz	8	160 MHz	6.25 ns

Table 2. Phase Selections

PHSEL1	PHSEL0	Phase Relationship
0	0	All at same phase
0	1	Outputs skewed by 90 degrees from each other
1	0	FOUT1 leads FOUT0 by minimum phase, FOUT2 lags FOUT0 by minimum phase, and FOUT3 lags FOUT0 by 90 degrees
1	1	Outputs skewed by minimum phase (determined by the divider selection, and the VCO frequency) from each other.

Note: The PECL output is not affected by the phase select inputs.

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can be met by setting PHSEL1 to 1, PHSEL0 to 0, and feeding back FOUT0 to the FBCLK input (Row 10 of Table 3). The result is that FOUT0 will be phase-aligned to the reference clock, FOUT1 will lead the reference clock by a minimum phase delay, FOUT2 will lag the reference clock by a minimum phase delay, FOUT3 will phase-lag the reference clock by 90°, HFOUT will be phase-aligned with the reference clock but at half the frequency, and X2FOUT will be either phase-aligned at the same frequency as the reference clock if DIVSEL = 0, or at twice the frequency if DIVSEL = 1.

Enabling Outputs

The S4405 has two output-enable inputs that control which outputs toggle. When held LOW, OUTEN0 controls the frequency doubler output X2FOUT and the half-frequency output HFOUT. OUTEN1 controls the FOUT0–3 outputs. When an output enable pin is held High, its associated outputs are disabled and held in a High state.

Filter

The FILTER output is a tap between the analog output of the phase detector and the VCO input. This pin allows a simple external filter (Figure 2) to be included in the PLL. AMCC recommends the use of the filter component values shown. This filter was chosen for its ability to reduce the output jitter and filter out noise on the reference clock input.

Reset

When the RESET pin is pulled low, all the internal states go to zero, but the outputs will not go low until one clock cycle later (VCO/2 or period of the reference clock). After the chip is reset, the PLL requires a resynchronization time before lock is again achieved.

Lock Detect

A lock detect function is provided by the LOCK output. When the selected reference clock and FBCLK are within 2–4 ns of each other, the PLL is in lock, and the LOCK output goes High.

Power Supply Considerations

Power for the analog portion of the S4405 chips must be isolated from the digital power supplies to minimize noise on the analog power supply pins. This isolation between the analog and digital power supplies can be accomplished with a simple external power supply filter (Figure 3). The analog power planes are connected to the digital power planes through single ferrite beads (FB1 and FB2) or inductors capable of handling 25 mA. The recommended value for the inductors is in the range from 5 to 100µH, and depends upon the frequency spectrum of the digital power supply noise. The ferrite beads should exhibit 75Ω impedance at 10 MHz.

Decoupling capacitors are also very important to minimize noise. The decoupling capacitors must have low lead inductance to be effective, so ceramic chip capacitors are recommended. Decoupling capacitors should be located as close to the power pins as physically possible. And the decoupling should be placed on the top surface of the board between the part and its connections to the power and ground planes.

BOARD LAYOUT CONSIDERATIONS

- The S4405 is sensitive to noise on the Analog +5 V and Filter pins. Care should be taken during board layout for optimum results.
- All decoupling capacitors (C1–C4 = 0.1 µF) should be bypassed between VCC and GND, and placed as close to the chip as possible (preferably using ceramic chip caps) and placed on top of board between S4405 and the power and ground plane connections.
- No dynamic signal lines should pass through or beneath the filter circuitry area (enclosed by dashed lines in Figure 4) to avoid the possibility of noise due to crosstalk.

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Figure 2. External PLL Filter

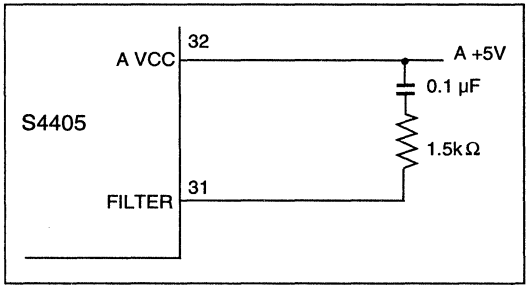
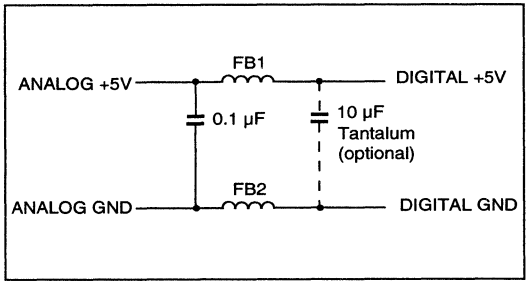


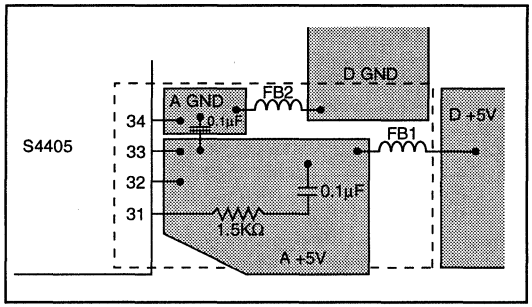
Figure 3. External Power Supply Filter



• The analog VCC supply can be a filtered digital VCC supply as shown below. The ferrite beads or inductors, FB1 and FB2, should be placed within three inches of the chip.

• The analog VCC plane should be separated from the digital VCC and ground planes by at least 1/8 inch.

Figure 4. Board Layout



Test Capabilities

The TSTEN input allows users to bypass the VCO and provide their own clock through the selected reference clock input. When TSTEN is High, the VCO is turned off and the REFCLK signal drives the divider/phase adjust circuitry, directly sequencing the outputs. The TSTEN and REFCLK inputs join the divider circuitry after the initial divide-by-two stage. Therefore, REFCLK is divided by two in the divide-by-four mode and divided by four in the divide-by-eight mode.

PIN DESCRIPTIONS

Input Signals

TTLREF. TTL. Frequency reference supplied by the user that, along with the output tied to the FBCLK input, determines the frequency of the FOUT0–FOUT3 outputs. INPSEL is used to select between this reference and the PECL reference PECLREFP/N.

PECLREFP/N. Differential PECL. Frequency reference supplied by the user. Selectable by the INPSEL input.

FBCLK. Feedback clock that, along with the reference clock input, determines the frequency of the FOUT0–FOUT3 outputs. One output is selected to feed back to this input. (See Table 3.)

DIVSEL. Controls the divider circuit that follows the VCO. When DIVSEL is low, the VCO frequency is divided by four. When DIVSEL is high, the VCO frequency is divided by eight. (See Tables 1 and 3.)

PHSEL0. This input, along with PHSEL1, allows selection of the phase relationship among the four FOUT0–FOUT3 outputs. See Tables 2 and 3 for the selection choices.

PHSEL1. Along with PHSEL0, allows selection of the phase relationship among the four FOUT0–FOUT3 outputs. See Tables 2 and 3 for the selection choices.

OUTEN0. Active Low. Output enable signal that controls which outputs toggle. Controls the frequency doubler output (X2FOUT) and the half-frequency output (HFOUT).

OUTEN1. Active Low. Output enable signal that controls which outputs toggle. Controls the FOUT0–FOUT3 outputs.

RESET. Active Low. Initializes internal states for test purposes.

TSTEN. Active High. Allows REFCLK to drive the divider phase adjust circuitry, after the first divide-by-two stage. Therefore, REFCLK can be divided by two in the divide-by-four mode, and divided by four in the divide-by-eight mode, and used to directly sequence the outputs.

INPSEL. Allows user to select between TTLREF and PECLREF reference frequencies. When INPSEL is High, the PECLREF input is selected.

Output Signals

FILTER. A tap between the analog output of the phase detector and the VCO input. Allows a simple external filter (a single resistor and capacitor) to be included in the PLL.

X2FOUT. Provides a clock signal identical to the FOUT0 output in the divide-by-four mode and twice the FOUT0 frequency (maximum of 80 MHz) in the divide-by-eight mode.

FOUT0. Clock output.

FOUT1. Clock output.

FOUT2. Clock output.

FOUT3. Clock output.

HFOUT. Provides a clock signal in phase with the FOUT0 output, but at half the FOUT0 frequency in both the divide-by-four and divide-by-eight modes.

PECLP/N. Differential PECL output, always one-half the VCO frequency.

LOCK. Goes high when the reference clock and FBCLK are within 2–4 ns of each other, demonstrating that the PLL is in lock.

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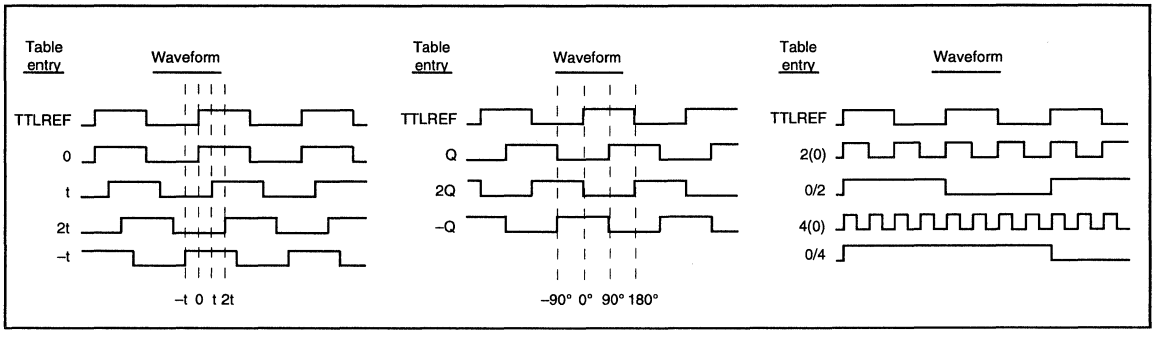
Table 3. Output Select Matrix

Configuration Number	Select Pins		Output Fed to FBCLK	Output Phase Relationships					÷4	÷8
	PHSEL1	PHSEL0		FOUT0	FOUT1	FOUT2	FOUT3	HFOUT	X2FOUT	
1	0	0	FOUT0–FOUT3	0	0	0	0	0/2	0	2(0)
2	0	0	HFOUT	2(0)	2(0)	2(0)	2(0)	0	2(0)	4(0)
3	0	0	X2FOUT (÷8)	0/2	0/2	0/2	0/2	0/4		0
4	0	1	FOUT0	0	Q	2Q	3Q	0/2	0	2(0)
5	0	1	FOUT1	–Q	0	Q	2Q	–Q/2	–Q	2(–Q)
6	0	1	FOUT2	–2Q	–Q	0	Q	–2Q/2	–2Q	2(–2Q)
7	0	1	FOUT3	–3Q	–2Q	–Q	0	–3Q/2	–3Q	2(–3Q)
8	0	1	HFOUT	2(0)	2(Q)	2(2Q)	2(3Q)	0	2(0)	4(0)
9	0	1	X2FOUT (÷8)	0/2	Q/2	2Q/2	3Q/2	0/4		0
10	1	0	FOUT0	0	–t	t	Q	0/2	0	2(0)
11	1	0	FOUT1	t	0	2t	Q+t	t/2	t	2(t)
12	1	0	FOUT2	–t	–2t	0	Q–t	–t/2	–t	2(–t)
13	1	0	FOUT3	–Q	–Q–t	–Q+t	0	–Q/2	–Q	2(–Q)
14	1	0	HFOUT	2(0)	2(–t)	2(t)	2(Q)	0	2(0)	4(0)
15	1	0	X2FOUT (÷8)	0/2	–t/2	t/2	Q/2	0/4		0
16	1	1	FOUT0	0	t	2t	3t	0/2	0	2(0)
17	1	1	FOUT1	–t	0	t	2t	–t/2	–t	2(–t)
18	1	1	FOUT2	–2t	–t	0	t	–2t/2	–2t	2(–2t)
19	1	1	FOUT3	–3t	–2t	–t	0	–3t/2	–3t	2(–3t)
20	1	1	HFOUT	2(0)	2(t)	2(2t)	2(3t)	0	2(0)	4(0)
21	1	1	X2FOUT (÷8)	0/2	t/2	2t/2	3t/2	0/4		0

Notes:
1. "0" implies the output is aligned with the reference clock.
2. "t" implies the output lags the reference clock by a minimum phase delay.
3. "Q" implies the output lags the reference clock by 90° of phase.
4. "–t" implies the output leads the reference clock by a minimum phase delay.
5. "–Q" implies the output leads the reference clock by 90° of phase.
6. "2( )" implies the output is at twice the frequency of the reference clock.
7. "/2" implies the output is at half the frequency of the reference clock.
8. The PECLN/P Differential PECL output is not affected by the PHSEL inputs.

7

Legend



ABSOLUTE MAXIMUM RATINGS

TTL Supply Voltage VCC (GND = 0)	7.0 V
TTL Input Voltage (GND = 0)	5.5 V
Operating Temperature	0°C to 70°C ambient
Operating Junction Temperature TJ	+ 130°C
Storage Temperature	–65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Nom	Max	Units
TTL Supply Voltage (VCC)	4.75	5.0	5.25	V
Operating Temperature	0 (ambient)	—	70 (ambient)	°C
Junction Temperature	—	—	130	°C

DC CHARACTERISTICS (TTL I/O)

Symbol	Parameter	DC Test Conditions		Min	Typ[1]	Max	Units
V_{IH}[2]	Input HIGH Voltage (TTL)	Guaranteed input HIGH voltage for all inputs		2.0			V
V_{IL}[2]	Input LOW Voltage (TTL)	Guaranteed input LOW voltage for all inputs				0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} = Min, I_{IN} = -18mA			-0.8	-1.2	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min	I_{OH} = -12mA[3]	2.4			V
			I_{OH} = -24mA[3]	2.0			V
V_{OL}	Output LOW Voltage	V_{CC} = Min	I_{OL} = 24mA[3]			0.5	V
I_{IH}	Input HIGH Current	V_{CC} = Min, V_{IN} = 2.7V				10	µA
I_I	Input HIGH Current at Max	V_{CC} = Max, V_{IN} = V_{CC}				1.0	mA
I_{IL}	Input LOW Current	V_{CC} = Min, V_{IN} = 0.5V	INPSEL			-300	µA
			Others			-50	µA
I_{OS}[4]	Output short circuit current	V_{CC} = Max, V_{OUT} = 0V		-25		-100	mA
I_{CC}	Static	V_{CC} = Max				95	mA
I_{CCT}	Total I_{CC} (Dynamic and Static)	C_{LOAD} = 25pF at 50 MHz				200	mA

DC CHARACTERISTICS (PECL I/O)

Symbol	Parameter	DC Test Conditions		Min	Typ[1]	Max	Units
V_{IH}[2]	Input HIGH Voltage (PECL)	Guaranteed input HIGH voltage for all inputs		V_{CC} –1145		V_{CC} –600	V
V_{IL}[2]	Input LOW Voltage (PECL)	Guaranteed input LOW voltage for all inputs		V_{CC} –2000		V_{CC} –1450	V
V_{OH}	Output HIGH voltage	V_{CC} = 5.0 V	Load = 50Ω to V_{CC} –2V	V_{CC} –1075		V_{CC} –650	V
V_{OL}	Output LOW voltage			V_{CC} –1980		V_{CC} –1585	V

1. Typical limits are at 25°C, V_{CC} = 5.0V.
2. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.
3. I_{OH}/I_{OL} values indicated are for DC test correlation. Actual dynamic currents are significantly higher and are optimized to balance rise and fall times.
4. Maximum test duration one second.

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Table 4. AC Specifications

Symbol	Description	S4405B-66		S4405B-80		Units
		Min	Max	Min	Max	
f_{VCO}	VCO Frequency	160	266	160	320	MHz
f_{REF}	REFCLK Frequency	10	66	10	80	MHz
MPW_{REF}	REFCLK Minimum Pulse Width	5.0		5.0		ns
t_{PE}	Phase Error between TTLREF and FBCLK	-1	0	-1	0	ns
t_{PEP}	Phase Error between PECLREF and FBCLK	-3	-1	-3	-1	ns
t_{PED}	Phase Error Difference from Part to Part[1]	0	750	0	750	ps
t_{SKEW}	Output Skew[2] (TTL)	0	400	0	400	ps
t_{DC}	Output Duty Cycle	45	55	45	55	%
f_{PECL}	PECLP/N Frequency	80	132	80	160	MHz
f_{FOUT}	FOUT Frequency[3] (TTL)	20	66	20	80	MHz
f_{HFOUT}	HFOUT Frequency[3]	10	33	10	40	MHz
f_{2XFOUT}	2XFOUT Frequency[3]	40	66	40	80	MHz
t_{PS}	Nominal Phase Shift Increment	3.75	6.25	3.125	6.25	ns
t_{OFD}	Tpd OUTEN0–2 to FOUTs, Disable	2	7	2	7	ns
t_{OFE}	Tpd OUTEN0–2 to FOUTs, Enable	2	7	2	7	ns
t_{IRF}	Input Rise/Fall Time	1	3	1	3	ns
t_{ORF}	FOUT Rise/Fall Time[4]	0.5	1.5	0.5	1.5	ns
t_{LOCK}	Loop Acquisition Time[5]		5		5	ms

1. Difference in phase error between two parts at the same voltage, temperature and frequency.
2. Output skew guaranteed for equal loading at each output.
3. C_{LOAD} = 35 pF.
4. With 35 pF output loading (0.8 V to 2.0 V transition).
5. Depends on loop filter chosen. (Number given is for example filter.)

Figure 5. Timing Waveforms

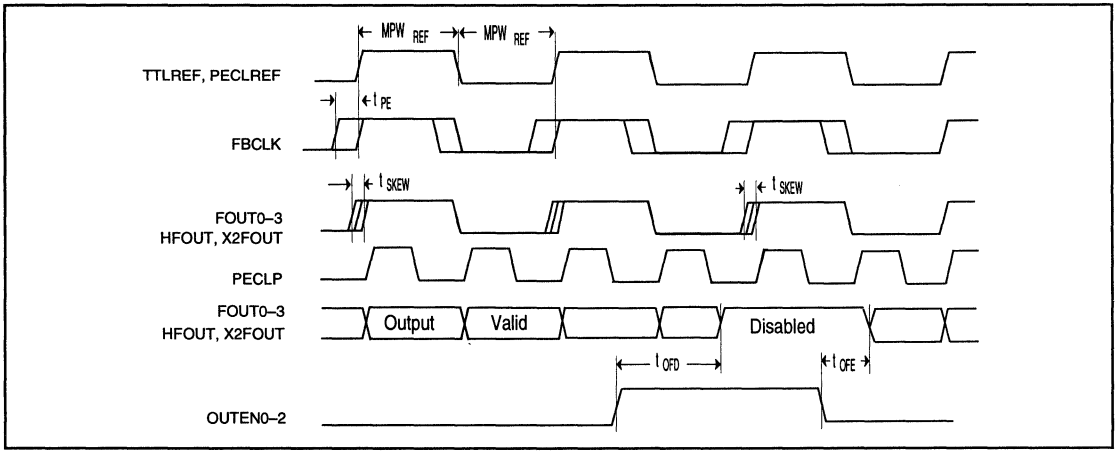
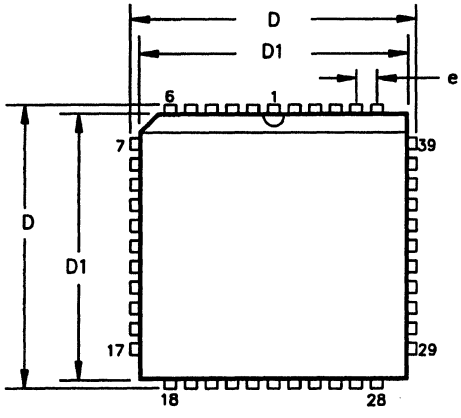
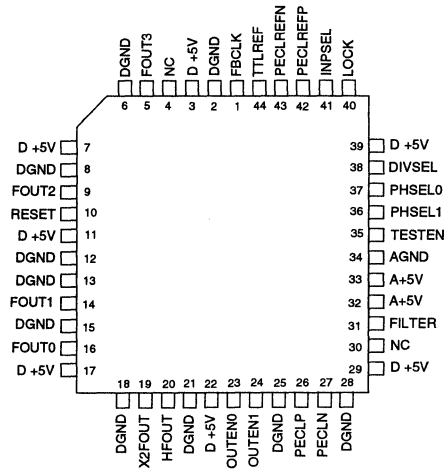
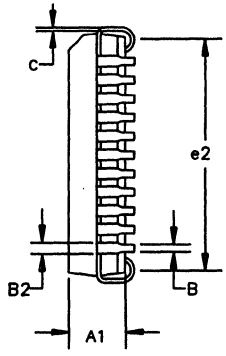


Figure 6. S4405 44 PLCC Package and Pinout







SYM	MIN	MAX
A1	.147	.157
B	.013	.021
B2	.026	.032
C	.007	.013
D	.687	.697
D1	.644	.659
e	.048	.052
e2	.610	.630

All dimensions nominal in inches.

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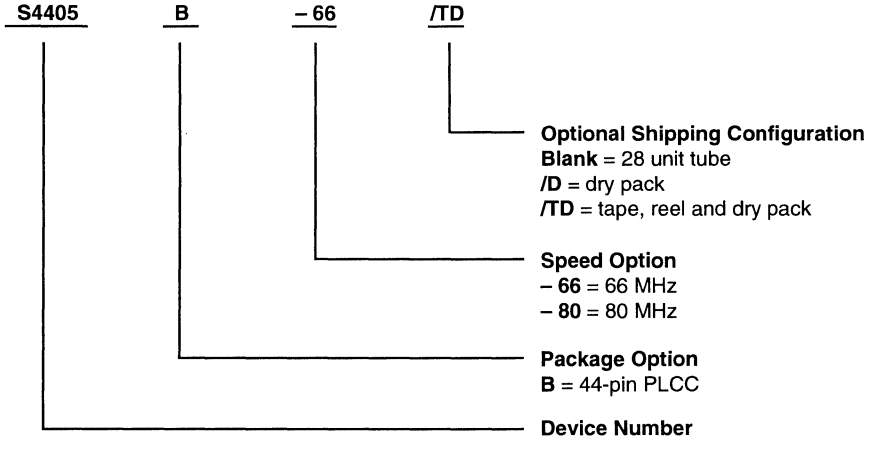
Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Speed Option (if applicable)**
- **Optional Shipping Configuration**



Example: S4405B–66/D
44-pin PLCC package, 66 MHz, dry packed in the standard tube.

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12-OUTPUT BiCMOS PLL CLOCK GENERATOR S4406

FEATURES

- Generates outputs from 10 MHz to 66 MHz
- Four groups of three outputs (12 outputs total)
- Eight user-selectable output functions for each group
- TTL compatible outputs, with <1.5-ns edge rates
- Performs clock doubling, dividing, invert, lead/lag placement
- Internal VCO running between 160 to 266 MHz
- 1.0µ BiCMOS technology
- Output skew less than 500 ps
- 52 PQFP package

APPLICATIONS

- High-performance microprocessor systems
- CMOS ASIC systems
- Backplane clock deskew and distribution
- Compatible with Intel's Pentium™ processor

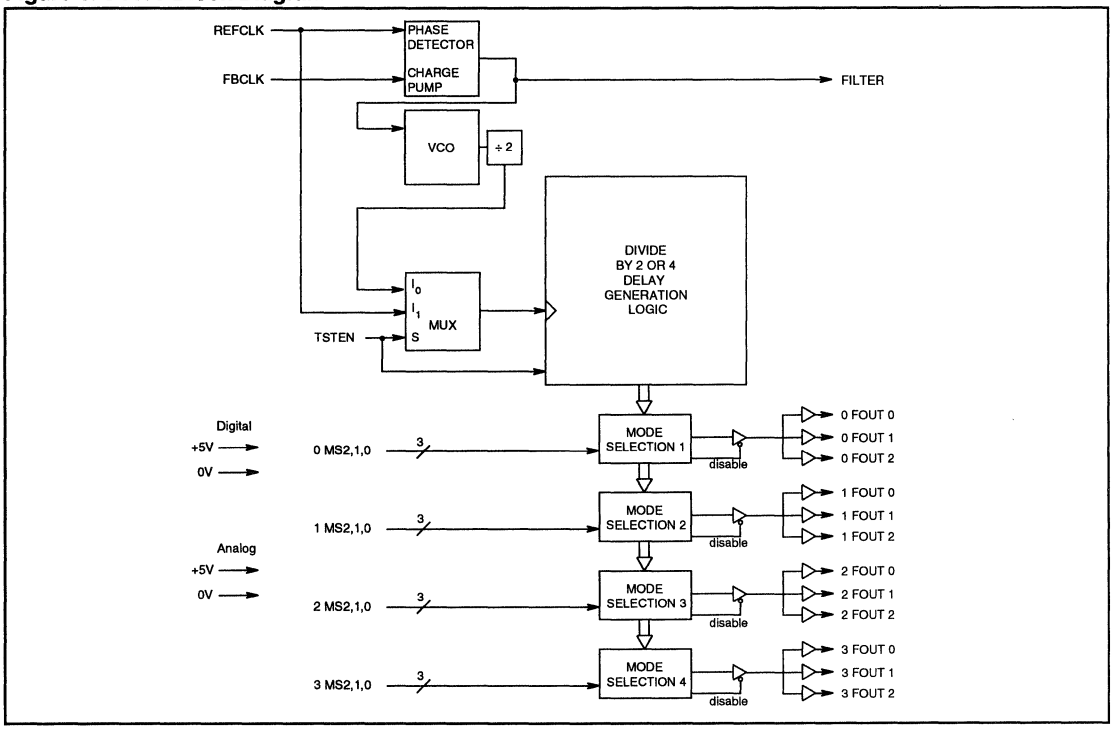
GENERAL DESCRIPTION

The S4406 BiCMOS clock generator provides 12 TTL outputs with less than 500 ps of skew. Implemented in AMCC's 1.0µ BiCMOS technology, the internal PLL and divider/delay selector logic allow the user to individually tailor the (4) TTL output groups to the system's needs. The internal VCO can operate between 160 to 266 MHz, and the programmability allows the user to generate output clocks in the 20–66 MHz range.

The S4406 offers the user the ability to select the appropriate phase and frequency relationship for each of the four groups of three TTL clock outputs.

In addition to clock doubling and inversion functions, the S4406 allows any output groups to lead or lag the others by the minimum phase delay of 3.75–6.25 ns.

Figure 1. S4406 Block Diagram



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FUNCTIONAL DESCRIPTION

The 12 xFOUT0–2 outputs are the main TTL output clocks that the generator supplies. The mode selection choices are shown in Table 1 and waveform definitions are given in Figure 2. The "x" represents the output group number (1–4). The frequency of these outputs is determined by the REFCLK clock frequency and the output clock that is tied to the FBCLK input (xFOUT0–2 can be equal to REFCLK, half of REFCLK, or twice the frequency of REFCLK).

Example:

In order to meet bus timing specifications for a typical system, designers may need three outputs at 66 MHz for the system clock and processor, a 33-MHz output for the cache controller, and a 33-MHz delayed output for a memory management unit. This system requirement can be met using the S4406 by setting the mode select pins for the first group of outputs (0MS2,1,0) to 111, the second group (1MS2,1,0) to 110, and the third group (2MS2,1,0) to 101. In this configuration, one of the 33-MHz outputs should be fed back to the FBCLK input. This example makes use of only three of the four output banks, leaving the fourth available for any other clock signals needed.

Table 1. Mode Selection Options

xMS2,1,0	MODE DESCRIPTION	xFOUT0,1,2
000	Disabled.	Logical Hi
001	All three outputs at the fundamental output frequency, but early by a minimum phase delay.	f – t
010	All three outputs at half the fundamental output frequency and inverted.	I /2
011	All three outputs at the fundamental output frequency and inverted.	I
100	All three outputs at half the fundamental output frequency, but delayed by a minimum phase delay.	f/2 + t
101	All three outputs at the fundamental output frequency, but delayed by a minimum phase delay.	f + t
110	All three outputs at half the fundamental output frequency.	f/2
111	All three outputs at the fundamental output frequency.	f

Note: If f is fed back, the fundamental frequency is equal to REFCLK.
If f/2 is fed back, the fundamental frequency is twice REFCLK.

Filter

FILTER is the analog signal from the phase detector going into the VCO. This pin is provided so a simple external filter (a single capacitor and resistor) can be included in the phase locked loop of the clock generator. See Figure 3.

Phase Delay

The minimum phase delay between xFOUT0–2 signals is a function of the VCO frequency. The VCO frequency can be determined by multiplying the fundamental output frequency by four, or half the fundamental frequency by eight. The minimum phase delay is equal to the period of the VCO frequency: t = 1/(VCO freq). Since the VCO can operate in the 160-MHz to 266-MHz range, the range of minimum phase delay values is 6.25 ns to 3.75 ns (See Table 2).

Figure 2. Waveform Definitions

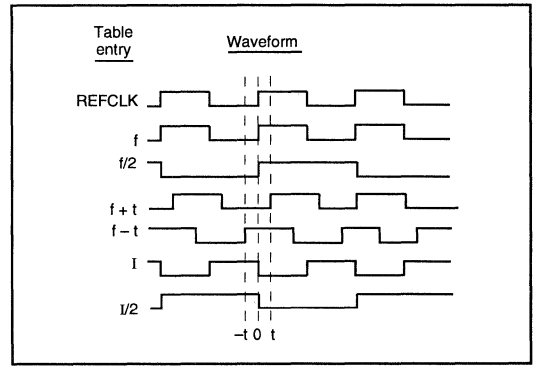
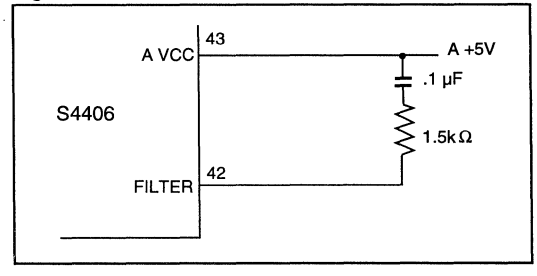


Figure 3. External PLL Filter



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Test Capabilities

TESTEN allows the chip to use the REFCLK input instead of the VCO output to clock the chip. This is used during chip test to allow the counters and control logic to be tested independently of the VCO. In addition, when TESTEN is brought High, an internal RESET pulse is generated. This initializes the internal counter flip-flops to zeros, and at the end of the next clock cycle, the outputs go to a zero state. TESTEN can also be used for board testing to allow the user to control the output clocks from the S4406 by inputting the board clock to the REFCLK input.

Table 2. VCO Operating Frequencies

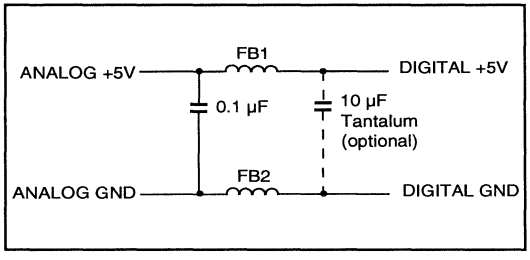
xFOUT0–2	VCO FREQ	MIN PHASE DELAY
66.6 MHz	266 MHz	3.750 ns
50 MHz	200 MHz	5.000 ns
40 MHz	160 MHz	6.250 ns
33.3 MHz	266 MHz	3.750 ns
25 MHz	200 MHz	5.000 ns
20 MHz	160 MHz	6.250 ns

The bank containing the output used as feedback must be in one of the f/2 modes to ensure the VCO is operating within its 160-266 MHz range.

Power Supply Considerations

Power for the analog portion of the S4406 chips must be isolated from the digital power supplies to minimize noise on the analog power supply pins. This isolation between the analog and digital power supplies can be accomplished with a simple external power supply filter (Figure 4). The analog power planes are connected to the digital power planes through single ferrite beads (FB1 and FB2) or inductors capable of handling 25 mA. The recommended value for the inductors is in the range from 5 to 100µH, and depends upon the frequency spectrum of the digital power supply noise.

Figure 4. External Power Supply Filter

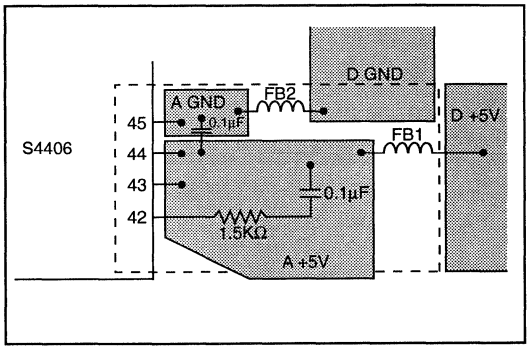


Decoupling capacitors are also very important to minimize noise. The decoupling capacitors must have low lead inductance to be effective, so ceramic chip capacitors are recommended. Decoupling capacitors should be located as close to the power pins as physically possible. And the decoupling should be placed on the top surface of the board between the part and its connections to the power and ground planes.

BOARD LAYOUT CONSIDERATIONS

- The S4406 chips are sensitive to noise on the Analog +5 V and Filter pins. Care should be taken during board layout for optimum results.
- All decoupling capacitors (C1–C4 = 0.1 µF) should be bypassed between VCC and GND, and placed as close to the chip as possible (preferably using ceramic chip caps) and placed on top of board between S4406 and the power and ground plane connections.
- No dynamic signal lines should pass through or beneath the filter circuitry area (enclosed by dashed lines in Figure 5) to avoid the possibility of noise due to crosstalk.
- The analog VCC supply can be a filtered digital VCC supply as shown below. The ferrite beads or inductors, FB1 and FB2, should be placed within three inches of the chip.
- The analog VCC plane should be separated from the digital VCC and ground planes by at least 1/8 inch.

Figure 5. Board Layout



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PIN DESCRIPTIONS

Input Signals

REFCLK. Frequency reference supplied by the user that, along with the output tied to the FBCLK input, determines the frequency of the outputs. Also replaces the VCO output when TSTEN is high (after first divide-by-two stage in divider phase control logic). See TSTEN.

FBCLK. Feedback clock that, along with the REFCLK input, determines the frequency of the outputs. One output is selected to feed back to this input.

TSTEN. Active High. Allows REFCLK to drive the divider phase adjust circuitry, after the first divide-by-two stage. Also, when brought High, generates an internal Reset pulse that initializes the internal counter flip-flops to zero.

xMS2,1,0. Mode selection inputs that allow selection of the phase and frequency relationship of each of the four banks of three clock outputs. The "x" represents the output group number (0–3). Refer to Table 1 for mode selection options.

Output Signals

FILTER. A tap between the analog output of the phase detector and the VCO input. Allows a simple external filter (a single resistor and one capacitor) to be included in the PLL.

xFOUT0–2. Clock signal outputs. Refer to Table 1 and Figure 4 for a description of output options.

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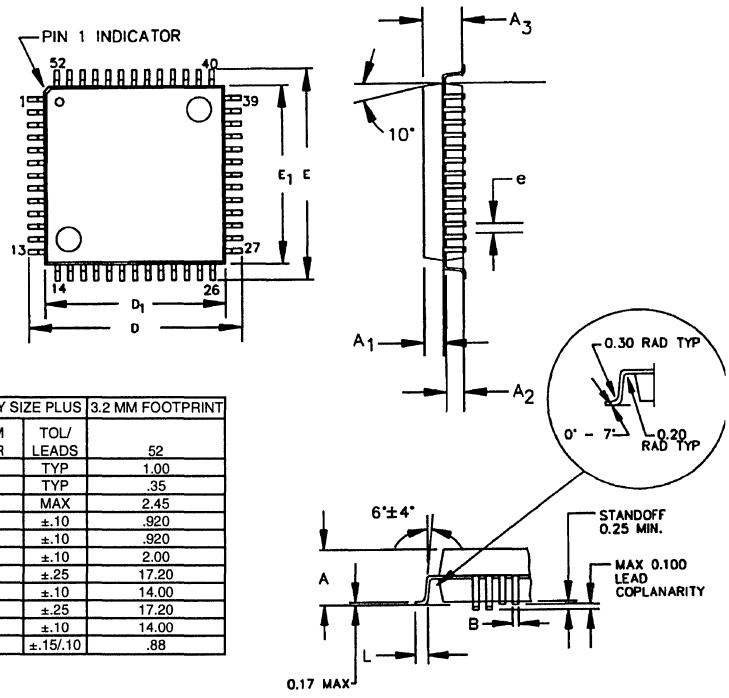
Figure 6. 52–pin PQFP Package



BODY SIZE PLUS	3.2 MM FOOTPRINT
DIM LTR	TOL/ LEADS	52
e	TYP	1.00
B	TYP	.35
A	MAX	2.45
A_1	±.10	.920
A_2	±.10	.920
A_3	±.10	2.00
D	±.25	17.20
D_1	±.10	14.00
E	±.25	17.20
E_1	±.10	14.00
L	±.15/.10	.88

All dimensions in mm.

DC CHARACTERISTICS

Symbol	Parameter	DC Test Conditions		Min	Typ[1]	Max	Units
V_{IH}[2]	Input HIGH Voltage	Guaranteed input HIGH voltage for all inputs		2.0			V
V_{IL}[2]	Input LOW Voltage	Guaranteed input LOW voltage for all inputs				0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} = Min, I_{IN} = -18 mA			-0.8	-1.2	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min	I_{OH} = -12 mA[3]	2.4			V
			I_{OH} = -24 mA[3]	2.0			V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 24 mA[3]				0.5	V
I_{IH}	Input HIGH Current	V_{CC} = Min, V_{IN} = 2.4V	4MS2,3MS2,1,0			-200	µA
			Other			50	µA
I_I	Input HIGH Current at Max	V_{CC} = Max, V_{IN} = V_{CC}				1.0	mA
I_{IL}	Input LOW Current	V_{CC} = Min, V_{IN} = 0.5V	4MS2,3MS2,1,0			-500	µA
			Other			-50	µA
I_{OS}[4]	Output short circuit current	V_{CC} = Max, V_{OUT} = 0V		-25		-100	mA
I_{CC}	Static	V_{CC} = Max				70	mA
I_{CCT}	Total I_{CC} (Dynamic and Static)	C_{LOAD} = 25 pF at 50 MHz				200	mA

1. Typical limits are at 25°C, V_{cc} = 5.0V.
2. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.
3. I_{OH}/I_{OL} values indicated are for DC test correlation. Actual dynamic currents are significantly higher.
4. Maximum test duration one second.

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ABSOLUTE MAXIMUM RATINGS

TTL Supply Voltage VCC (VEE = 0)	7.0 V
TTL Input Voltage (VEE = 0)	5.5 V
Operating Temperature	0°C to 70°C ambient
Operating Junction Temperature TJ	+ 130°C
Storage Temperature	–65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Nom	Max	Units
TTL Supply Voltage (VCC)	4.75	5.0	5.25	V
Operating Temperature	0 (ambient)	—	70 (ambient)	°C
Junction Temperature	—	—	130	°C

Table 3. AC Specifications

Symbol	Description	Min	Max	Units
f_{VCO}	VCO Frequency	160	266	MHz
f_{REF}	REFCLK Frequency	10	66	MHz
t_{IRF}	Input Rise/Fall Time	1	3	ns
MPW_{REF}	REFCLK Minimum Pulse Width	5.0		ns
t_{PE}	Phase Error between REFCLK and FBCLK	-1.0	0	ns
t_{PED}	Phase Error Difference from Part to Part[1]	0	750	ps
t_{SKEW}	Output Skew[2] across all outputs	0	500	ps
t_{SKEWA}	Output Skew[2] within any bank	0	250	ps
t_{DC}	Output Duty Cycle[3]	45	55	%
f_{FOUT}	FOUT Frequency[4]	10	66	MHz
t_{PS}	Nominal Phase Shift Increment[5]	3.75	6.25	ns
t_j	Clock Stability[6]		500	ps
t_{ORF}	FOUT Rise/Fall Time[7]	0.5	1.5	ns
t_{LOCK}	Loop Acquisition Time[8]		5	ms
t_{PSV}	Phase Shift Variation[5]	-250	+250	ps

1. Difference in phase error between two parts at the same voltage, temperature and frequency.
2. Output skew guaranteed for equal loading at each output.
3. Outputs loaded with 35 pF, measured at 1.5 V.
4. C_{LOAD} = 35 pF.
5. All phase shift increments and variation are measured relative to 0FOUT0 at 1.5 V.
6. Clock period jitter with all FOUT outputs operating at 66MHz loaded with 25 pF using loop filter shown. Parameter guaranteed, but not tested.
7. With 35 pF output loading (0.8 V to 2.0 V transition).
8. Depends on loop filter chosen. (Number given is for example filter.)

Figure 7. Timing Waveforms

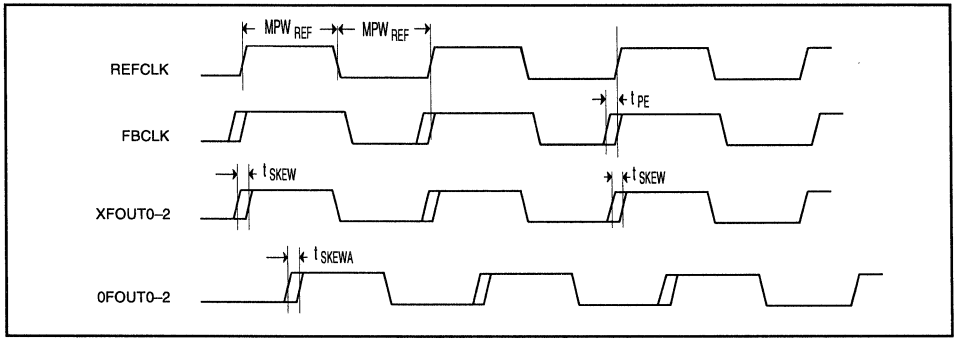

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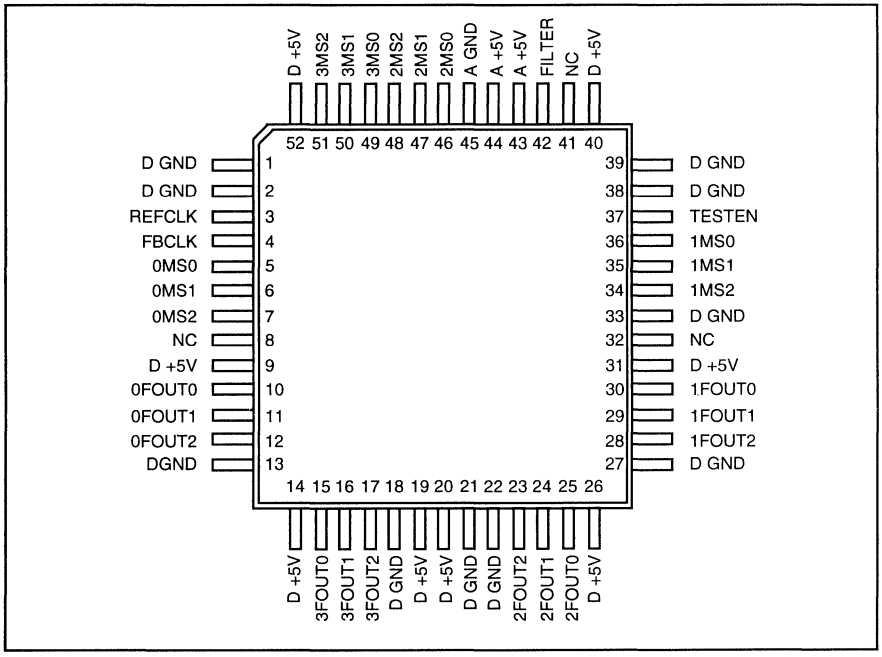
Figure 8. S4406 Pinout



Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Speed Option (if applicable)**
- **Optional Shipping Configuration**

S4406 **Q** **– 66** **/TD**

Optional Shipping Configuration
Blank = 84-unit matrix tray
/D = dry pack
/TD = tape, reel and dry pack

Speed Option
– 66 = 66 MHz

Package Option
Q = 52-pin Plastic Quad Flat Pack (PQFP)

Device Number

Example: S4406Q–66/D
52-pin PQFP package, 66 MHz, shipped dry packed in the standard matrix tray.

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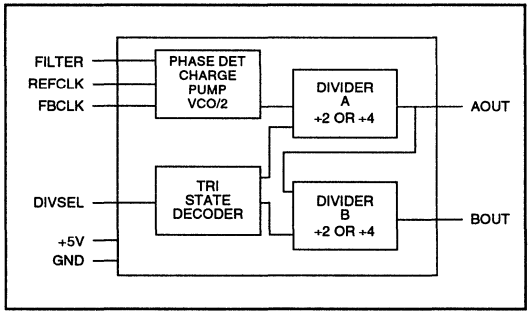
FEATURES

- Performs X2 and X4 Multiplication on Input Clock Frequency
- Eliminates the need for High Speed Crystals
- Simplifies Clock Routing by Reducing High-Speed Clock Traces
- Generates 2 TTL Outputs, 50 and 100 MHz max
- Output Skew ±200 ps max
- 160–400 MHz PLL
- Space Saving 8-pin SIP or SOIC
- Reduces System EMI Generation
- Less than 0.3 W at 80 MHz
- Proven 1.5 Micron BiCMOS Technology

APPLICATIONS

- "Deskewing" ASIC Devices
- RISC and High Performance Microprocessor Systems
- Clocking synchronous DRAMS and Memory Modules

Figure 1. S4501 Block Diagram



GENERAL

The S4501 has two clock inputs, REFCLK and FBCLK and two outputs AOUT and BOUT providing signals at 2X and 4X the REF frequency. The frequency of AOUT depends on DIVSEL and the choice of outputs (frequencies) fed back to the FBCLK input. See Figure 1.

The S4501 Clock Multiplier allows a 1/2 or 1/4 speed clock to be routed to the device which in turn produces 2X or 4X multiples to meet high speed clock requirements.

The S4501 can also be used as a "zero-delay" buffer to provide multiple frequency outputs in sync with the reference clock.

In applications requiring ASIC "deskewing," using an output of the ASIC as FBCLK to the S4501 allows that output (and others related to it) to be synchronized to the REFCLK to within ±500 ps. The S4501's PLL will then actively align the clock of the ASIC to compensate for its nominal propagation delay as well as any variation due to process or operating conditions.

Table 1. AC Performance Summary

Description	Min	Max	Units
Input Frequency	10	100	MHz
Phase Error	—	±500	ps
Output Skew		±200	ps
Output Freq.	10	100	MHz

Table 2. DC Performance Summary

Description	Min	Max	Units
Output Current	-24	+24	mA
Voh @ -16 mA	2.4		V
Vol @ +24 mA		0.5	V
I_{CC}		55	mA

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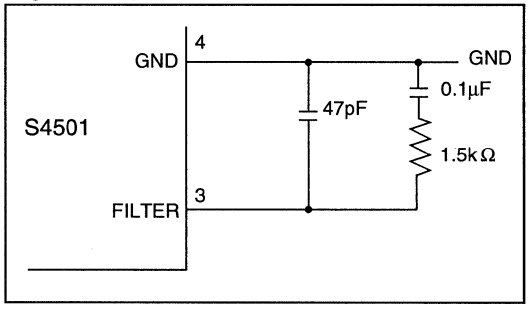
Filter

The FILTER output is a tap between the analog output of the phase detector and the VCO input. This pin allows a simple external filter (Figure 2) to be included in the PLL. AMCC recommends the use of the filter component values shown. This filter was chosen for its ability to reduce the output jitter and filter out noise on the REFCLK input. The filter components should be in surface mounted packages with minimum lead inductance.

Power Supply Considerations

Decoupling capacitors are also very important to minimize noise. The decoupling capacitors must have low lead inductance to be effective, so ceramic chip capacitors are recommended. Decoupling capacitors should be located as close to the power pins as physically possible. And the decoupling should be placed on the top surface of the board between the part and its connections to the power and ground planes.

Figure 2. External PLL Filter



PIN DESCRIPTIONS

Input Signals

REFCLK. Frequency reference supplied by the user that, along with the output tied to the FBCLK input, determines the frequency of the A and B outputs.

FBCLK. Feedback clock that, along with the REFCLK input, determines the frequency of the A and B outputs. One output is selected to feed back to this input. (See Table 3, DIVSEL is Tri-State Logic.)

DIVSEL. Controls the divider circuit that follows the VCO. Uses tri-state logic where low < GND + .5V, mid = $V_{CC}/2$, and high > V_{CC} - .5., (See Table 3, DIVSEL is Tri-State Logic.)

Output Signals

FILTER. A tap between the analog output of the phase detector and the VCO input. Allows a simple external filter (a single resistor and one capacitor) to be included in the PLL.

AOUT. TTL output. Frequency depends on VCO speed and DIVSEL level.

BOUT. TTL output. $^1/_2$ or $^1/_4$ the frequency of AOUT depending on DIVSEL level.

Table 3. DIVSEL is Tri-State Logic

DIVSEL	DIVIDER A	DIVIDER B	Where:
L	X/4	A/4	L=GND M=VCC/2 H=VCC X=VCO/2
M	X/4	A/2	
H	X/2	A/4	

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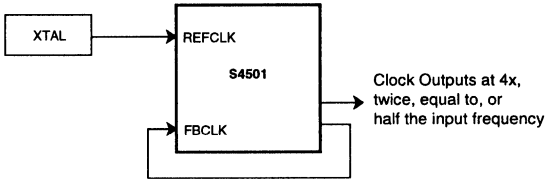
TYPICAL APPLICATIONS

The S4501 is designed to meet a large variety of system clocking requirements. Several typical applications are provided below.

Application 1. High-Frequency, Low-Skew Clock Generation

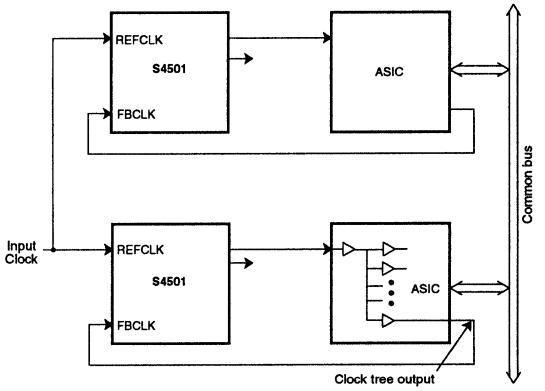
One of the most basic capabilities of the device is generating phase-aligned clocks at various multiples of the input clock frequency. For example, in a multiple-board system a half-frequency clock can be generated for use across the backplane, where it is simpler to route a low-speed signal. This signal can then be doubled on the boards, and synchronization will be maintained.



Application 2. Delay Compensation

Since the relative edges of the REFCLK and FBCLK inputs are precisely controlled, the S4501 can be used to compensate for different delays due to trace lengths or to internal chip delays, simplifying board layout and bus timing. In the example shown, the two ASICs have a difference of several nanoseconds in their propagation delays. The S4501 ensures that the output signals are aligned, so that the data valid uncertainty on the common bus is minimized.

Temperature and voltage effects on prop delays through the ASICs can also be minimized by the S4501's on-board PLL when in this configuration.



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Absolute Maximum Ratings	Commercial
TTL Supply Voltage VCC (VEE = 0)	7.0 V
TTL Input Voltage (VEE = 0)	5.5 V
Operating Temperature	0°C to 70°C ambient
Operating Junction Temperature TJ	+ 130°C
Storage Temperature	–65°C to +150°C

Recommended Operating Conditions

Parameter	Commercial			Units
	Min	Nom	Max	
TTL Supply Voltage (VCC)	4.75	5.0	5.25	V
Operating Temperature	0 (ambient)	—	70 (ambient)	°C
Junction Temperature	—	—	130	°C

DC Characteristics

Symbol	Parameter	DC Test Conditions		Min	Typ[1]	Max	Units
V_{IH}[2]	Input HIGH voltage	Guaranteed input HIGH voltage for all inputs		2.0			V
V_{IL}[2]	Input LOW voltage	Guaranteed input LOW voltage for all inputs				0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} = Min, I_{IN} = -18mA			-0.8	-1.2	V
V_{OH}	Output HIGH voltage	V_{CC} = Min	I_{OH} = -12mA[3] (COM)	2.4			V
			I_{OH} = -24mA[3] (COM)	2.0			V
V_{OL}	Output LOW voltage	V_{CC} = Min	I_{OL} = 24mA[3] (COM)			0.5	V
I_{IH}	Input HIGH current	V_{CC} = Min, V_{IN} = 2.4V				50	µA
I_I	Input HIGH current at max	V_{CC} = Max, V_{IN} = V_{CC}				1.0	mA
I_{IL}	Input LOW current	V_{CC} = Min, V_{IN} = 0.5V				-50	µA
I_{OS}[4]	Output short circuit current	V_{CC} = Max, V_{OUT} = 0V		-25		-100	mA
I_{CC}	Static	V_{CC} = Max	COM			50	mA
I_{CC}	Total I_{CC} (Dynamic and Static)	V_{LOAD} = 25pF at 50 MHz	COM			75	mA

1. Typical limits are at 25°C, V_{cc} = 5.0V.
2. These input levels should only be tested in a static, noise-free environment.
3. I_{OH}/I_{OL} values indicated are for DC test correlation. Actual dynamic currents are significantly higher and are optimized to balance rise and fall times.
4. Maximum test duration is one second.

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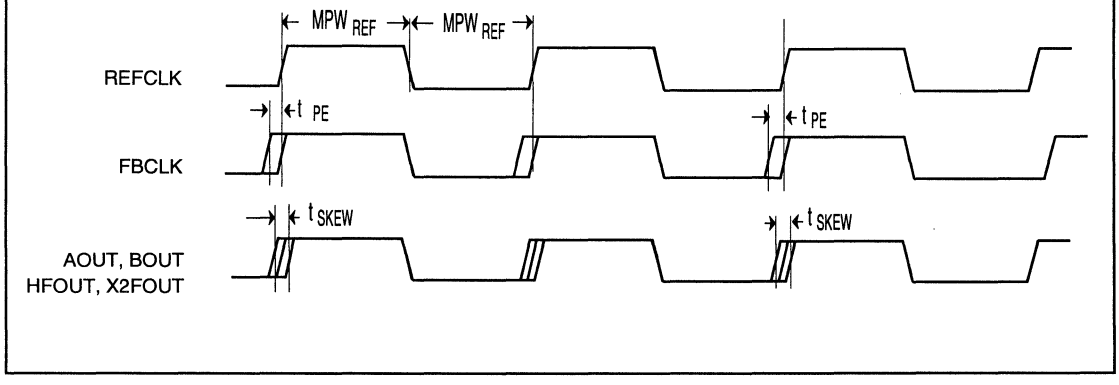
Table 4. AC Specifications

Symbol	Description	Min	Max	Units
f_{VCO}	VCO Frequency	160	400	MHz
f_{REF}	REFCLK Frequency	10	100	MHz
MPW_{REF}	REFCLK Minimum Pulse Width	4		ns
t_{PE}	Phase Error between REFCLK and FBCLK	-500	+500	ns
t_{PED}	Phase Error Difference from Part to Part[1]	0	750	ps
t_{SKEW}	Output Skew[2]	0	400	ps
t_{DC}	Output Duty Cycle[3]	45	55	%
f_{FOUT}	AOUT Frequency[4]	20	100	MHz
f_{HFOUT}	BOUT Frequency[4]	10	50	MHz
t_{IRF}	Input Rise/Fall Time	1	3	ns
t_{ORF}	AOUT, BOUT Rise/Fall Time[5]	0.5	1.5	ns
t_{LOCK}	Loop Acquisition Time[6]		5	ms
t_j	Clock Stability[7]		500	ps

1. Difference in phase error between two parts at the same voltage, temperature and frequency.
2. Output skew guaranteed for equal loading at each output.
3. Outputs loaded with 35pF, measured at 1.5V.
4. C_{LOAD} = 35 pF.
5. With 35 pF output loading (0.8 V to 2.0 V transition).
6. Depends on loop filter chosen. (Number given is for example filter.)
7. Clock period jitter with both outputs operating at 66 and 33 MHz, loaded with 25pF using loop filter shown. Parameter guaranteed, but not tested.

Figure 5. Timing Waveforms



7

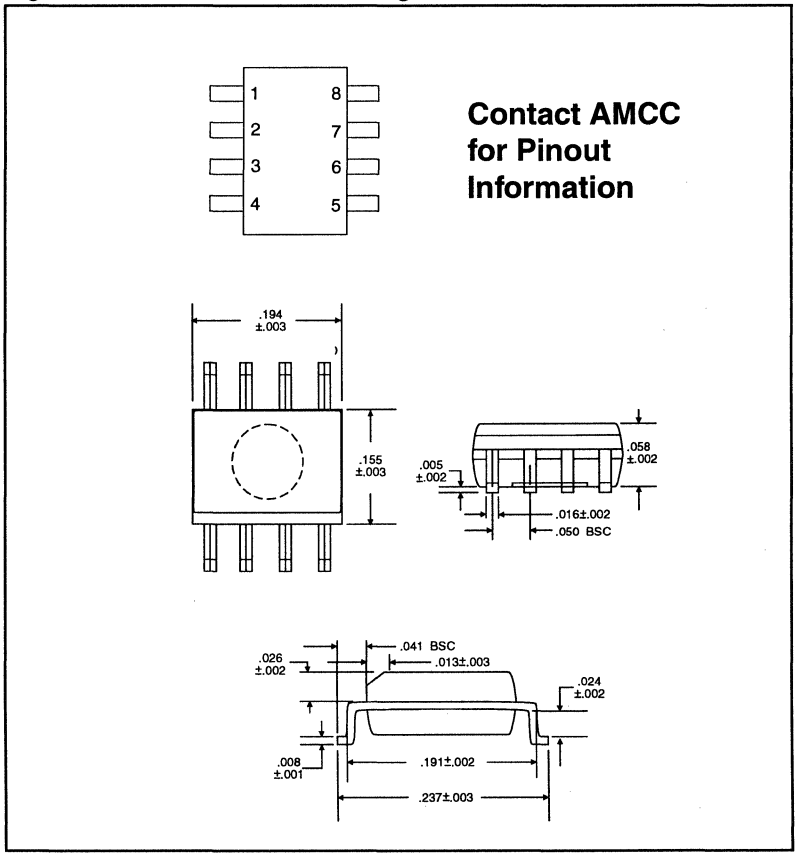
BOARD LAYOUT CONSIDERATIONS

• The S4501 is sensitive to noise on the +5V and Filter pins. Care should be taken during board layout for optimum results.

• All decoupling capacitors (0.1 µF) should be bypassed between VCC and GND, and placed as close to the chip as possible (preferably using ceramic chip caps) and placed on top of board between S4501 and the power and ground plane connections.

• No dynamic signal lines should pass through or beneath the filter circuitry area to avoid the possibility of noise due to crosstalk.

Figure 5. 8-Pin SOIC Pinout/Package



Ordering Information

GRADE	PLL CLOCK GENERATOR	PACKAGE
S–commercial	4501	S–8-pin SOIC

X — Grade
XXXX — Part number
X — Package

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BiCMOS CLOCK SYNTHESIZER S4503

FEATURES

- Multiplies input reference frequency by integers 2–32
- Digitally programmable output clock frequencies from 10 MHz to 300 MHz
- Two (2) groups of independent clock outputs
  - One group consists of differential PECL outputs
  - One group is a pair of TTL outputs
- Proprietary TTL output drivers with:
  - Complementary 24 mA peak outputs, source and sink
  - Source series termination
  - Edge rates less than 1.5 ns
- Low 250 ps reference typ clock jitter (PECL outputs), 400 ps max
- 1.1 mW or less power dissipation, frequency and load dependent
- 150 MHz to 300 MHz phase-locked loop VCO frequency range
- Advanced BiCMOS process technology
- Space saving 28 PLCC package

GENERAL DESCRIPTION

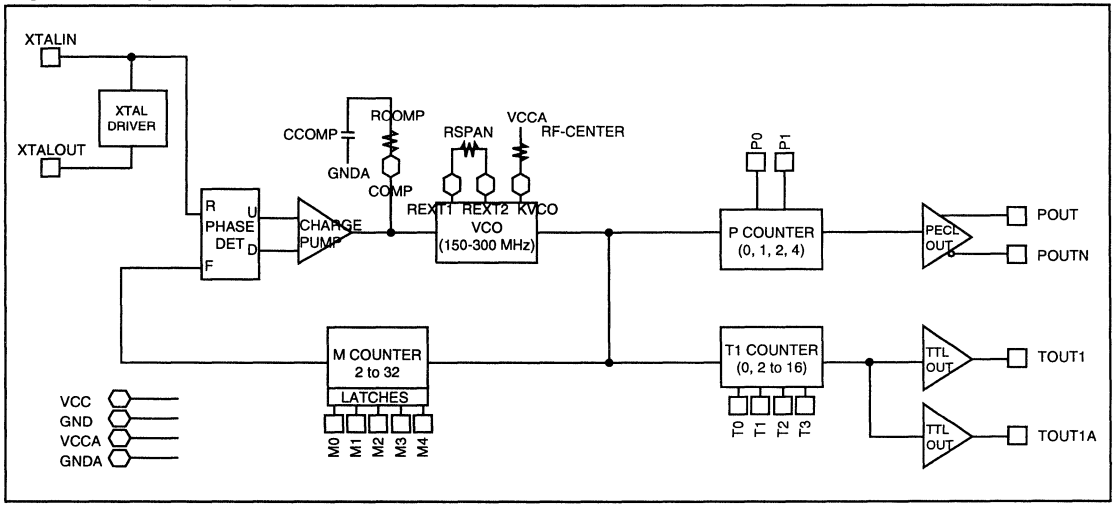
The S4503 is a clock synthesizer which utilizes phase-locked loop technology to provide two (2) independently selectable output frequencies in the 10 MHz to 300 MHz range. A reference input may be provided by either a low cost crystal or a TTL frequency source.

The first of the two (2) output frequency groups consists of a pair of differential PECL (Positive referenced ECL) outputs which will operate up to 300 MHz. The second group (TTL) consist of two outputs with selectable frequency, up to 80 MHz.

The final frequency for each group is digitally selected via three programmable counters. One counter is used to set the internal VCO frequency between 150 MHz to 300 MHz, and the others are used to divide the VCO frequency from 2 thru 16 (TTL) and 1, 2 or 4 (PECL).

All phase-locked loop elements are provided on chip with the exception of the passive components needed for the loop filter function and VCO.

Figure 1. Logic Diagram



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Absolute Maximum Ratings

Storage Temperature ..... -55°C to +150°C
V_{CC} Potential to Ground ..... -0.5V to +7.0V
Input Voltage ..... -0.5V to +V_{CC}
Static Discharge Voltage ..... >1750V
Maximum Junction Temperature ..... +130°C
Latch-up Current ..... >200 mA
Operating ambient temperature ..... 0°C to +70°C

Capacitance (package)

Input Pins ..... 5.0 pF
TTL Output Pins ..... 5.0 pF
PECL Output Pins ..... 5.0 pF

AC Characteristics

V_{CC} = +5.0V ± 5%, T_a = 0°C to +70°C

Symbol	Description	Conditions	MIN	MAX	Units
F_{VCO}	VCO Frequency		150	300	MHz
F_{XTL}	XTL Frequency, Fundamental	XTLIN to XTLOUT	5	25	MHz
F_{TTL}	TTL Input Frequency	Standard TTL Levels	5	80	MHz
P_{out}	PECL Out Frequency		37	300	MHz
T_{OUTn}	TTL Out Frequency	See Note 4	9	80	MHz
$T_{SKEW\ T\text{-}T}$	TTL to TTL Output Skew	TTL Leading Edges at +1.5V		250	ps
$T_{SYM\text{-}T}$	T_{OUT} Symmetry	Measured at 1.5V		±1.5	ns
$T_{SYM\text{-}P}$	PECL Out Symmetry	Measured at differential crossing points		±250	ps
T_J	PECL Clock Jitter, pk to pk			400	ps

Notes:
1. Max cycle to cycle jitter.
2. Output symmetry is the deviation from a 50% duty cycle.
3. All AC parameters are tested or guaranteed by characterization.
4. VCO frequency is limited to a maximum of 250 MHz when TTL outputs are used.

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Electrical Characteristics

V_{CC} = +5.0V ± 5%, T_a = 0°C to +70°C

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}(PECL)	Output HIGH Voltage, ECL	50 Ohms to V_{CC}-2V	V_{CC}-1075	V_{CC}-650	mV
V_{OL} (PECL)	Output LOW Voltage, ECL	50 Ohms to V_{CC}-2V	V_{CC}-1980	V_{CC}-1585	mV
V_{OH}(TTL)	Output HIGH Voltage	F_{OUT} = 80 MHz max, C_L = 10pF	2.4		V
V_{OL} (TTL)	Output LOW Voltage, TTL	F_{OUT} = 80 MHz max, C_L = 10pF		0.6	V
V_{IH} (TTL)	Input (TTL) HIGH Voltage	All TTL Inputs	2.0	V	V
I_{IL} (TTL)	Input (TTL) LOW Voltage	All TTL Inputs	-0.5	0.8	V
I_{OH}(PECL)	Output HIGH Current	50 Ohms to V_{CC}-2.0		25	mA
I_{OL}(PECL)	Output LOW Current	50 Ohms to V_{CC}-2.0		8	mA
I_{IH} (TTL)	Input HIGH Current	V_{in} = V_{CC}		200	uA
I_{IL} (TTL)	Input LOW Current	V_{in} ≤ 0.8		50	uA
I_{OHS}[1]	Output HIGH Short Current	Output High, V_{OUT}=0V, Typical	-55		mA
I_{OLS}[1]	Output LOW Peak Current	Output Low, V_{OUT}= V_{CC}, Typical	55		mA
I_{CC}	Supply Current	TTL Outputs to 20 pF @ 50 MHz		210	mA
POWER	Power Dissipation	TTL Outputs to 20 pF @ 50 MHz		1.1	W

1. Maximum test duration one second.
2. All DC parameters are tested or guaranteed by characterization.

The S4503 TTL outputs feature source series termination of approximately 40 Ohms to assist in matching 50–75 ohm P.C. board environments.

DC Characteristics

The S4503 has been designed specifically for clock distribution. In the development of this product, AMCC has made several modifications to the historic "high drive, totem pole outputs" producing AMCC's dynamically adjusting source series terminated outputs. As a result of this, the S4503 will dynamically source and sink a symmetrical 24 mA of current. In a DC state, it exhibits the following specifications:

	Conditions	Min	Max
V_{OH}	I_{OH} = -8 mA	2.4V	
V_{OL}	I_{OL} = 4 mA		0.6V

DESCRIPTION OF OPERATION (Refer to Logic Diagram)

The S4503 synthesizer employs a phase locked loop (PLL) which includes a "multiplying" counter to produce a high frequency internal reference oscillator from a low cost, low frequency crystal. This high frequency internal reference is the output of a votage controlled oscillator or VCO. This single VCO frequency is sub divided down to selectable TTL output frequencies. One positive (+5V) referenced complementary ECL (PECL) output (Pout) pair is also provided.

The M counter is a frequency "multiplying" feedback counter that divides down the VCO frequency, before applying it to the phase detector. Thus the VCO frequency is the product of the input reference (crystal) frequency and the M counter modulus. This divide down counter modulus is externally selected to any integer value from 2 to 32 by a five bit binary coded value, plus 1, entered into input latches via the preset input pins M0 through M4. The M0 to M4 inputs have the binary weight of $M0=2^0$ through $M4=2^4$. The M0-4 inputs are low or 0 if not connected. NOTE: an entry of all binary zeros will not count down and is, therefore, invalid. Designs that will load the M counter inputs from an external register that powers-up with the outputs in a hi-Z state will need to use external resistors to ensure the S4503 M counter inputs are never all zeros.

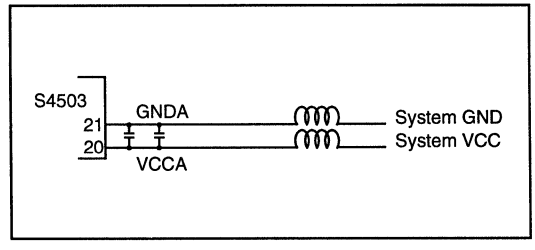
The output frequency divide down counters "P & T" each have individual select input pins which may be actively driven by CMOS/TTL outputs or strapped to +Vcc (as a 1) or non-connected as appropriate. Non-connected inputs are biased low or 0. When the binary coded value of zero is entered into these counter preselect inputs, their outputs are disabled, thereby saving AC output power. Note that the input frequency to the T counter (VCO frequency) is limited to 250 MHz. P counter will operate up to 300 Mhz. Output symmetry is very close to 50% duty cycle with both odd and even division modulus due to an odd division correction employed at the counter's output. Refer to the counter preset tables for the binary coded preselect input values to division modulus.

The TTL output drivers of the T counter are source series terminated by internal resistors of ~40 Ohms to avoid the need for external termination. This series termination was choosen to match 50 to 75 Ohm transmission line traces into end of line load capacitance of ~20 pF. Refer also to the AMCC Clock Driver Application Note #1. The complementary PECL output emitter followers can source 25 mA from +Vcc and should be externally terminated at the end of the transmission line into an equivalent 50 Ohm resistance to +Vcc - 2V.

The analog VCO circuitry requires some external passive loop filter components mounted very close to the required S4503 package pins. A VCO frequency centering resistor, RFcenter, is connected between KVCO and +VCCA, the analog +5V. A frequency span resistor, Rspan, is connected between pins REXT1 and REXT2. A loop filter series resistor-capacitor pair, RCOMP & CCOMP is connected between pin Comp and analog ground GNDA. Note that the analog ground (GNDA) and +5V (+VCCA) are to be isolated (decoupled) from the noisier digital and output power leads VCC and GND.

The input to the XTALIN pin will be a series resonant crystal of fundamental frequency from 5 to 25 Mhz. The external addition of series or shunt capacitance to "pull" the frequency is up to the user's discretion. An external series resistor may be required to limit the drive current from the XTALOUT pin with low ESR crystals.

When the XTALIN pin is driven by an external TTL clock source, the XTALOUT pin is not connected and the peak TTL amplitude should not exceed 3 volts. TTL output signals should be in the range of 5-80 MHz.



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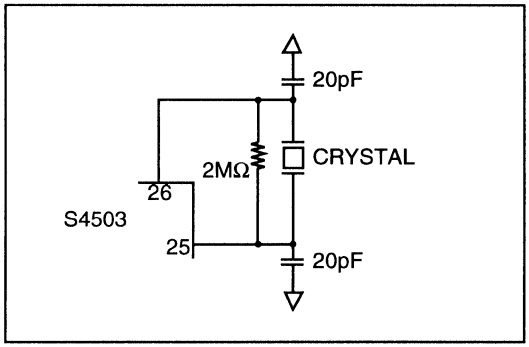
BOARD LAYOUT CONSIDERATIONS

To minimize the impact of board noise on the operation of the S4503, the following guidelines should be followed.

- The analog VCCA and GNDA need to be isolated from the digital supplies. This can be accomplished by creating small analog power and ground planes next to the S4503 under the filter and VCO components. These analog planes can be connected to the digital planes through wire jumpers, small inductors (5-100 uH), or ferrite beads. If the digital supply noise is too large (>100mV), the inductors or ferrite beads will be necessary.
- Decoupling capacitors of 0.1 and 0.01 uF are needed. Three pairs should be placed as close to the S4503 power and ground pins as possible. One pair should be used to decouple the analog VCC and GND, while the others are for the digital supplies. The Vtt supply will also need to be decoupled using 0.1 and 0.01 uF capacitors. These components should be surface mounted chip capacitors, to reduce the parasitic inductance.
- No dynamic signal lines should pass through or beneath the filter circuitry area, to avoid the possibility of noise due to crosstalk.
- The crystal oscillator will need to have a 2 M ohm shunt resistor connected between the terminals of the external crystal, and two 20 pF capacitors connected from each pin of the crystal to VCC (or GND). These components are necessary to ensure the oscillator will operate at the correct frequency.
- The loop filter and VCO components must be surface mounted to reduce the parasitic inductance, and the components are connected to the analog power and ground planes, rather than the digital planes.



FILTER AND VCO COMPONENT SELECTION

The S4503 is designed to operate over a wide range of VCO frequencies. Because of this, it is necessary to modify the values of Rspan and Rfcenter in order to get the best performance at a given frequency.

When operating the S4503 with the VCO in the 150–225 MHz region, the values for the VCO components are:

Rspan = 470 Ohms, Rfcenter = 390 Ohms

When operation the S4503 with the VCO in to 225–300 Mhz, the values for the VCO components are:

Rspan = 390 Ohms, Rfcenter = 820 Ohms

The loop filter components, Rcomp and Ccomp, do not change values at different frequencies. The correct values for these components are:

Rcomp = 2.7K Ohms, Ccomp = 0.1uF

All of the resistor values are 5% and 1/8 watt.

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Power Management

The overall goal of managing the power dissipated by the S4503 is to limit its junction (die) temperature to 130°C. A major component of the power dissipated internally by the S4503 is determined by the load that each TTL output drives and the frequency that each output is running. The following table summarizes these dependencies.

FREQUENCY	C_{LOAD}=5pF	C_{LOAD}=10pF	C_{LOAD} =15pF	C_{LOAD} =25pF	C_{LOAD} =40pF	NO LOAD
80 MHz	42 mW	51 mW	61 mW	88 mW	132 mW	18 mW
66 MHz	38 mW	47 mW	55 mW	75 mW	110 mW	16 mW
50 MHz	28 mW	33 mW	39 mW	60 mW	85 mW	14 mW
40 MHz	25 mW	30 mW	36 mW	52 mW	70 mW	13 mW
33 MHz	19 mW	22 mW	24 mW	46 mW	65 mW	12 mW
25 MHz	16 mW	18 mW	20 mW	32 mW	60 mW	11 mW
20 MHz	14 mW	16 mW	18 mW	24 mW	44 mW	10 mW

The above output power must then be added to the core power (700 mW) of the S4503 to determine the total power being dissipated by the S4503. This total power is then multiplied by the S4503's thermal resistance, with the result being added to the ambient temperature to determine the junction temperature of the S4503. For greatest reliability this junction temperature should not exceed 130°C. The thermal resistance for the S4503 soldered to a multi-layer PCB is as follows:

	Still Air	100 Lin Ft/Min	200 Lin Ft/Min
Thermal Resistance	50°C/Watt	45°C/Watt	40°C/Watt

Designing the S4503 for "Real Loads"

The S4503 is designed to provide clean clock transitions when presented with a realistic load. The assumptions are that the S4503 will be driving a selected length(s) of 70 Ohm (Zo) P.C. board trace terminated by a small number of end of line clustered TTL or CMOS input receiver pins. This end of line capacitive loading can cause overall impedance to drop to under 60 Ohms. Therefore, to a first approximation, this clock output driver will cleanly drive P.C. line lengths of 6" to 12" with capacitive loads ranging up to 20 pF at frequencies up to 80 MHz. Higher capacitive loads (greater than 25 pF) at high frequencies (greater than 50 MHz) may require the like output drivers to be strapped in parallel.

Within this general circuit model, AMCC has developed the Evaluation Circuit presented on the following page. This is a mid-point model and can be modified to reflect a specific end use. More details concerning this are presented in the Application Note.

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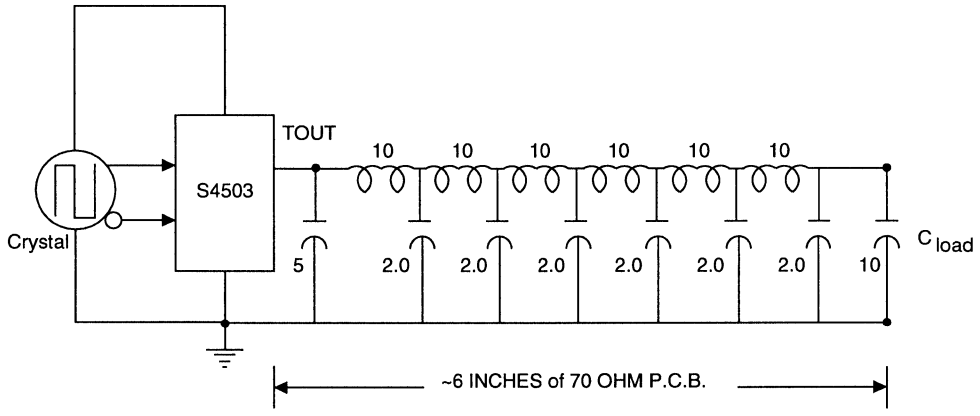
Evaluation Circuit



NOTES: All inductance is in nH. Capacitance is in pF
At frequencies above 50 MHz, a single point destination is recommended

S4503 M- Counter Division Table

M0	M1	M2	M3	M4	MODULUS
0	0	0	0	0	INVALID
1	0	0	0	0	2
0	1	0	0	0	3
1	1	0	0	0	4
0	0	1	0	0	5
1	0	1	0	0	6
0	1	1	0	0	7
1	1	1	0	0	8
0	0	0	1	0	9
1	0	0	1	0	10
0	1	0	1	0	11
1	1	0	1	0	12
0	0	1	1	0	13
1	0	1	1	0	14
0	1	1	1	0	15
1	1	1	1	0	16

M0	M1	M2	M3	M4	MODULUS
0	0	0	0	1	17
1	0	0	0	1	18
0	1	0	0	1	19
1	1	0	0	1	20
0	0	1	0	1	21
1	0	1	0	1	22
0	1	1	0	1	23
1	1	1	0	1	24
0	0	0	1	1	25
1	0	0	1	1	26
0	1	0	1	1	27
1	1	0	1	1	28
0	0	1	1	1	29
1	0	1	1	1	30
0	1	1	1	1	31
1	1	1	1	1	32

[Where: M(0:4) + 1 = MODULUS and M0 and M0 = 2^0, M1 = 2^1, M2 =2^2, M3 = 2^3, M4 = 2^4]

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S4503 Output Counter Division Table

P0	P1	P-MODULUS
0	0	DISABLED
1	0	1
0	1	2
1	1	4

T0	T1	T2	T3	T-1 MODULUS
0	0	0	0	DISABLED
1	0	0	0	2
0	1	0	0	3
1	1	0	0	4
0	0	1	0	5
1	0	1	0	6
0	1	1	0	7
1	1	1	0	8
0	0	0	1	9
1	0	0	1	10
0	1	0	1	11
1	1	0	1	12
0	0	1	1	13
1	0	1	1	14
0	1	1	1	15
1	1	1	1	16

VCO frequency is limited to a maximum of 250 MHz when TTL outputs are used.

Where T1 (0:3) + 1 = MODULUS and

$T0 = 2^0$

$T1 = 2^1$

$T2 = 2^2$

$T3 = 2^3$

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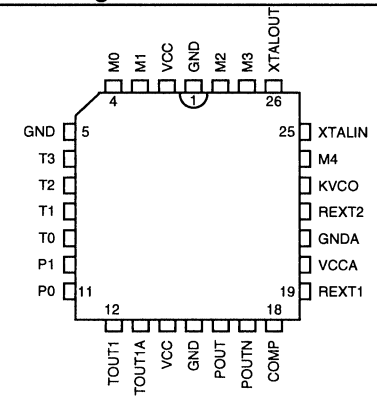
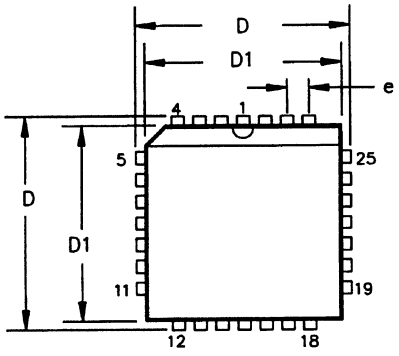
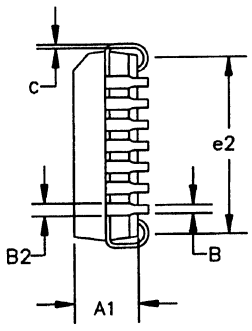
28 PLCC Package and Pinout



SYM	MIN	MAX
A1	.147	.157
B	.013	.021
B2	.026	.032
C	.007	.013
D	.487	.497
D1	.444	.459
e	.048	.052
e2	.410	.430





All dimensions nominal in inches.

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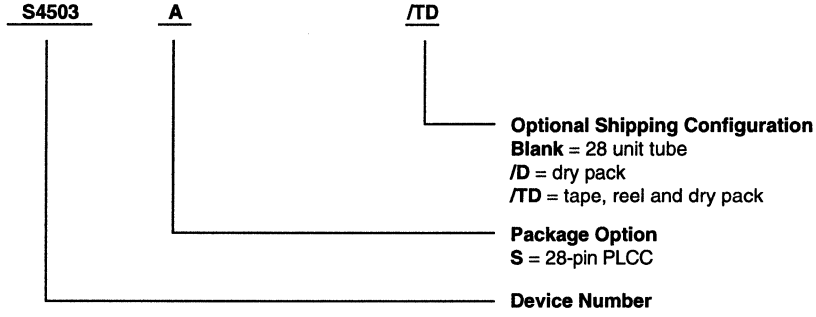
Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Optional Shipping Configuration**



Example: S4503A/D
28-pin PLCC package, shipped dry packed in the standard tube.

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INTRODUCTION

As today's personal computers (PC) and systems push into the 50Mhz realm and beyond, the minimization of system clock skew becomes more important. Clock skew eats into the effective clock period that is available to perform other tasks. Using generic driver chips and careful board layout, current systems can achieve about 4ns of system clock skew. A 4ns clock skew at 25Mhz is 10% of the clock period, while at 66Mhz this same 4ns skew eats up 26% of the system clock period. At 50Mhz and higher, the allowable clock skew is approximately 2ns–3ns. Clearly this requires a new method of clock generation and distribution.

The key to the reduction of clock skew lies in the development of PLL clock generators, low skew clock drivers, and understanding how to distribute and route the clock signals.

The S4402/S4403 use AMCC's 1.0 micron BiCMOS technology to generate 10–80Mhz multiphase TTL clocks with less than +/-200ps of skew. The S4402 offers 6 output drivers, four at the primary output frequency, one at two times the primary frequency, and one at half the primary frequency. The S4403 offers 10 output drivers: four pairs at the primary output frequency, one at twice the primary frequency, and one at half the primary frequency.

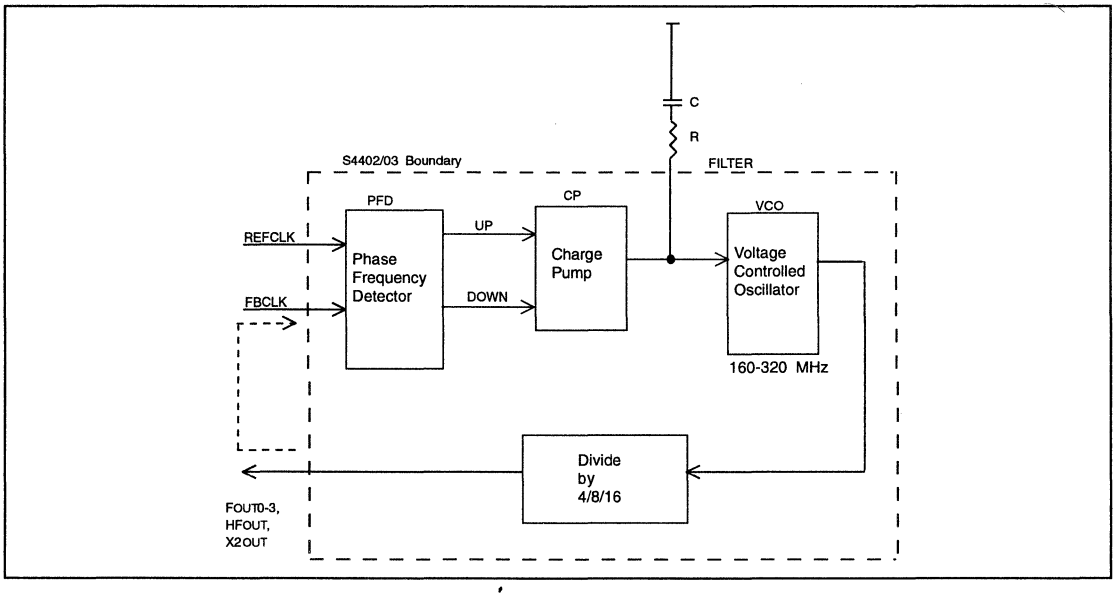
The phase relationships between the outputs are programmable. Four different output configurations are available to provide synchronous outputs, quadrature phase delay outputs, minimum phase delay outputs, and a mixture of minimum and quadrature phase delay outputs.

The times-two output and the half frequency output, allow the S4402/03 to multiply and divide the reference clock input for distribution to the system clock loads. This feature is very useful to eliminate the EMI problems of distributing high frequency clocks across the entire system.

PLL CLOCK GENERATOR OVERVIEW

The basic concepts of phase-locked loops are fairly simple. The diagram in Figure 1 shows the fundamental blocks of the S4402/03 PLL. The task of the PLL is to minimize the frequency and phase differences between the reference clock input (REFCLK) and the feedback clock input (FBCLK). In this case, the PLL clock generator can be considered a "zero delay" clock buffer.

Figure 1. Phase-Locked Loop of S4402/03



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The Phase Frequency Detector (PFD) compares the reference and feedback clocks and provides a signal to the Charge Pump (CP) that tells the charge pump to increase or decrease the voltage into the Voltage Controlled Oscillator (VCO). This in turn increases or decreases the oscillator frequency, thereby changing the frequency or phase of the feedback clock.

The CP converts the digital signals from the PFD into a change in voltage at the external filter pin. This change in voltage is supplied to the VCO input. The CP can provide very small changes in the VCO control voltage that will modify the phase of the VCO output, or it can provide larger changes in the control voltage to change the VCO frequency.

The VCO simply responds to the control voltage at its input and generates an output clock frequency which is proportional to the voltage at its input. This high frequency clock signal goes into the internal logic of the S4402/03 and is divided by four, eight, or sixteen before appearing at the various chip outputs.

By selecting one of the S4402/03 outputs as the feedback clock, the loop is closed, and the internal PLL will try to make the rising edge of the output connected to the feedback input line up with the rising edge of the reference clock input. Due to the closed loop nature of this action, delays between the reference clock output and the subsequent arrival of the feedback clock input can occur without causing the chip to lose lock. Therefore, an external buffer can be introduced into the loop, and an output from the buffer fed back to the feedback input. This provides a simple means of increasing the output drive capability of the S4402. Another option is to introduce an external counter into the loop, and connect an output from the counter into the feedback input. This allows the S4402/03 to accept a lower reference clock frequency.

The two most important specifications for PLL clock generators are phase error and output skew.

Phase error is defined as the delay between the reference input and the feedback input when the chip is locked. When an output is used to drive the feedback input, the phase error can also be specified as a propagation delay. The S4402/03 clock generators have a maximum phase error (across all temperatures, supply voltages, and frequencies) of 1.0ns. On a given chip there will be less than 1.0ns of delay between the REFCLK input and the FBCLK input. Furthermore, at a given frequency, temperature, and supply voltage, the maximum variation in phase error across all parts is less than 750ps. Plus, at a given frequency, the maximum variation in phase error across all parts, is less than 1.25ns, over any temperature and supply voltage difference. These are important specifications in determining total system clock skew.

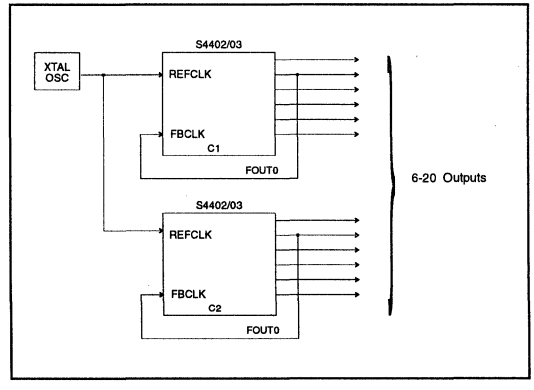
Output skew is defined as the delay between synchronous outputs. The S4402/03 clock generators have a maximum output skew of +/- 200ps. This means that with equal loading, all the rising outputs will switch within 400ps of each other.

CLOCK DISTRIBUTION ON A BOARD

The first few system clock skew examples are based upon the idea that all the clock loads are located within a single board.

The simplest configurations are that of a single S4402/03 or of multiple S4402/03s in parallel being driven from a single reference source. In Figure 2 the clock generators C1 and C2 are driven from the same crystal oscillator output. The clock skew associated with a single clock generator, such as C1 by itself, is simply the output skew specification of 400ps (+/- 200ps max).

Figure 2. Clock Distribution on a Board



In the case where the output from the crystal oscillator drives no additional chips on the board, except the clock generators, the total clock skew across all the S4402/03s can be calculated as:

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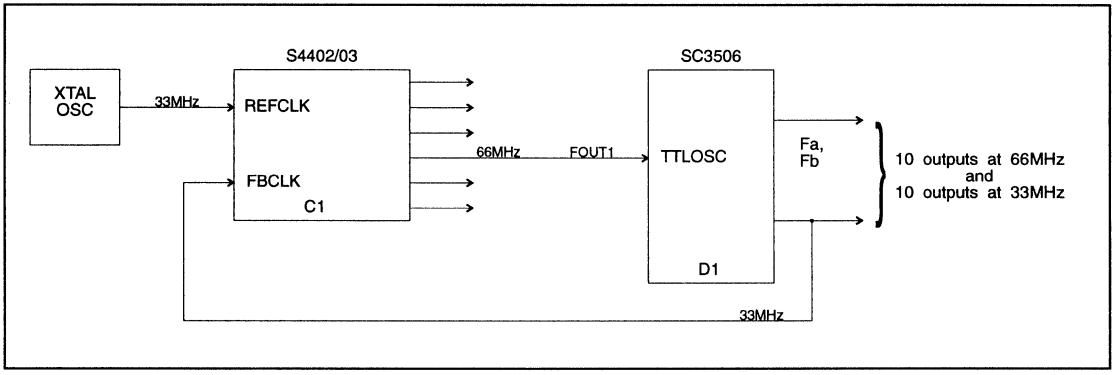
Figure 3. Clock Distribution on a Board: S4402 with an SC3506



Total skew = Tpev + Tskew
= 750ps + 400ps
Total skew = 1.150ns (max.)

where,

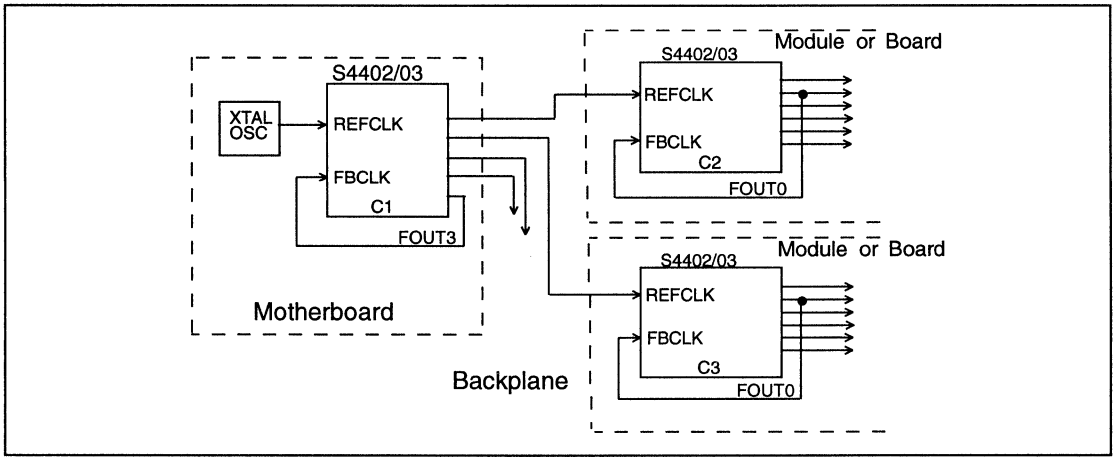
Tpev = the maximum variation in phase error across all parts at a given frequency, temperature and supply voltage.

Tskew = the maximum output skew on any part.

In this first example, the total clock skew across C1 and C2 depends upon the phase error and the output skew of each chip. Rather than use the total range of phase error for all possible frequencies, temperatures, and supply voltages, this configuration allows the use of the chip to chip variation in phase error. This is possible because the clock generators will be placed close to the crystal oscillator, and therefore experience the same temperature and power supply environment.

The second example, in Figure 3, shows the use of an S4402 clock generator to multiply the 33Mhz crystal oscillator output up to 66Mhz before applying it to the input of the SC3506 clock driver. This is accomplished by feeding back one of the divide-by-two outputs of the SC3506 to the FBCLK input of the S4402/03. This configuration allows the use of a slower crystal oscillator to generate 10 outputs at 66Mhz and 10 outputs at 33Mhz.

Figure 4. Clock Distribution Between Boards



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Because the output of the SC3506 is fed back to the FBCLK input of the S4402, the delay through the SC3506 is not important in the calculation of the total output clock skew. The total output clock skew is determined solely by the output skew specification of the SC3506, and is therefore, less than 500ps (max.) for the SC3506-1.

CLOCK DISTRIBUTION BETWEEN BOARDS

Most systems do not consist of a single board containing all the computing, memory, I/O, and display functions. A typical system configuration would likely have a central board that ties the system together (the motherboard), and a series of additional modules or expansion boards, that allow the user to update and upgrade the system.

Ideally, the master clock needs to be distributed to the synchronous logic on the motherboard, and each of the expansion boards, with no skew.

Figure 4 shows a configuration using an S4402/03 to distribute the master clock to the motherboard and the expansion boards. On each board or module, the master clock copy is received by another S4402/03, and distributed to the rest of the board.

The maximum clock skew between the motherboard clocks (outputs of C1) and the module clocks (outputs of C2 and C3) can be calculated as:

C1-to-C2 skew = Tskew(C1)
+ Tpemax(C2)
+ Tskew(C2)
= 400ps
+ 1.0ns
+ 400ps

C1-to-C2 skew = 1.80ns (max.),

where,

Tpemax(C2) = the maximum absolute value of phase error for C2.

Tskew(C1 or C2) = the maximum output skew for each chip.

The total system skew will be determined by the maximum skew across all the modules. This total system skew can be calculated, using the results of the C1-to-C2 skew calculation, as:

Total skew = C1-to-C2skew(max.)
– C1-to-C3skew(max.)
= 1.80ns
– C1-to-C3skew(max.)

C1-to-C3skew = Tpevfmin(C3)
+ Tskew(C3)
= [Tpemax(C3) – Tpevf]
+ Tskew(C3)
= [1.0ns - 1.25ns]
+ –400ps

C1-to-C3skew = –650ps (max.)

Total skew = 1.80ns – [–650ps]

Total skew = 2.45ns (max.)

where,

Tpevf = the maximum chip to chip variation in phase error at a given frequency, across all temperatures and supply voltages.

Tpevfmin(C3) = the most negative phase error of C3 versus C2, based upon a Tpevf variation between C2 and C3.

In this calculation, the objective is to determine the widest variation in output skew between the C2 and C3 clock generators. The calculations make use of the fact that at a given frequency, but with unequal temperatures and supply voltages, the maximum variation in phase error between any two parts is less than 1.25ns. This specification is used to make the maximum skew variation of C3 versus C1 be –650ps, when the maximum skew variation of C2 versus C1 is 1.80ns. With this, the maximum size of the output switching window around C1 is equal to 2.45ns.

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Figure 5. Clock Dividing and Multiplication for Distribution Between Boards

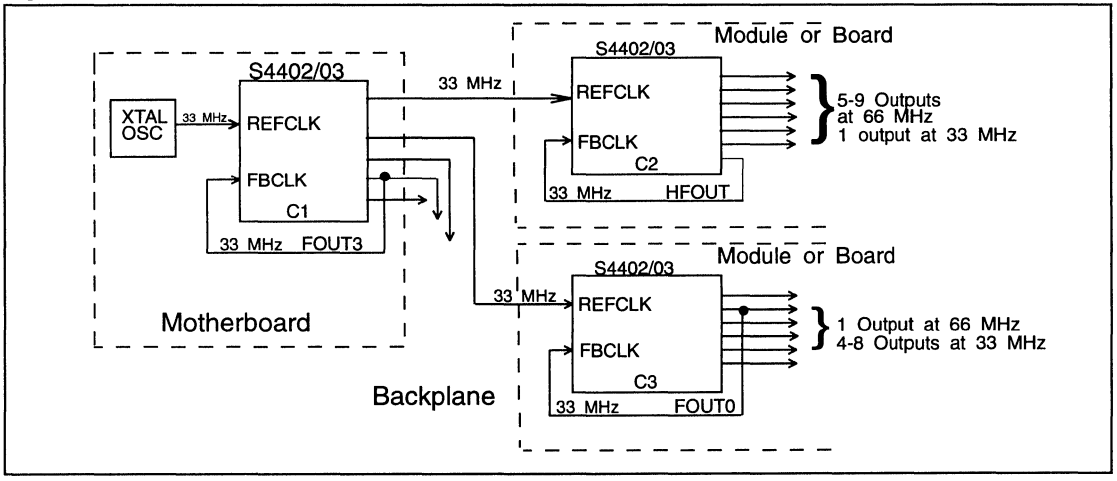


Figure 5 shows the use of the S4402/03 as a clock multiplier and divider in a board to board clock distribution scheme. In this example, the motherboard clock generator, C1, is used to distribute multiple copies of the crystal oscillator frequency of 33Mhz. These 33Mhz outputs are routed point to point down the backplane to each of the expansion boards or modules. In this manner, it is possible to route slower frequency outputs on the backplane, and reduce the crosstalk, signal noise, and EMI problems.

The S4402/03 chip on each module can be programmed to multiply the 33Mhz backplane clock signal to its previous 66Mhz value, or it can create a set of 33Mhz clock outputs. With this technique, each module or board can be selectively operated at the crystal oscillator frequency, 2X that frequency, or 1/2 the oscillator frequency.

In this application, the total system clock skew is also 2.45ns. The calculation of system clock skew in this example is the same as that for the previous example.

Figure 6 shows a special application of the S4402/03. In this application, data is to be synchronously transferred between boards in the system. The difficulty arises from the fact that in a system, the data delay from one board to the next varies depending upon location. This delay uncertainty, and the total system clock skew, combine to make the job of providing sufficient hold time, at the input register on each board, a difficult task.

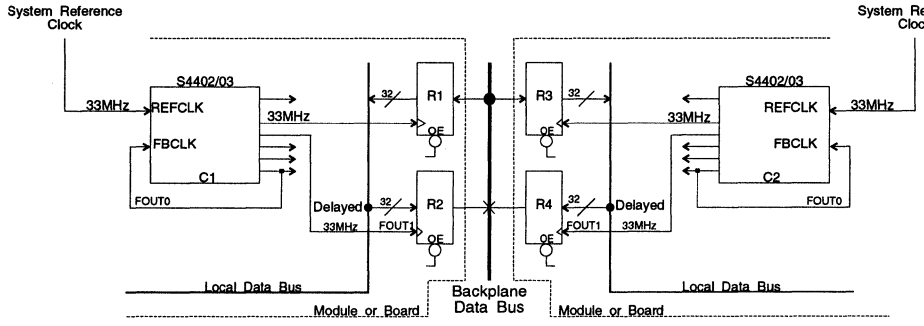
For this example, assume the system reference clock on each board is generated by an S4402/03 that is located in a central location, typically the motherboard. From a previous example (Figure 5), this gives a total system clock skew of 2.45ns.

Based upon this 2.45ns clock skew, a scenario can be drawn in which the data that is clocked out from one board reaches its neighbor before the neighboring card has stored the previous data into the input register with sufficient hold time. A solution to this problem is to delay the time at which data is clocked out of all the boards.

In this solution, the data is clocked into each input register, on a clock edge that is synchronous with the system reference clock. A short time later (3–6ns), new data is clocked out onto the backplane data bus. This will provide sufficient hold time at each board, provided that the delay between the two register clocks is at least equal to the system clock skew plus the hold time of the input register.

The example in Figure 6 uses registers with a hold specification between 0.5ns and 1.3ns. Based on these values, the delay between the register clocks on each board must be at least 2.95ns to 3.75ns. In the minimum phase mode of operation, the S4402/03 can be configured to provide 3.75ns delays between output clocks at 33Mhz, and is an ideal solution for this problem. FOUT0 is synchronous to the system reference clock, and is used to clock the input registers R1 and R3. FOUT1 is delayed from

Figure 6. Data Distribution Between Boards



FOUT0 by 3.75ns, and is used to clock the output registers R2 and R4. If additional delay is necessary, FOUT2 could replace FOUT1, and provide 7.5ns of delay between FOUT0 and FOUT2.

ASIC DESKEWING

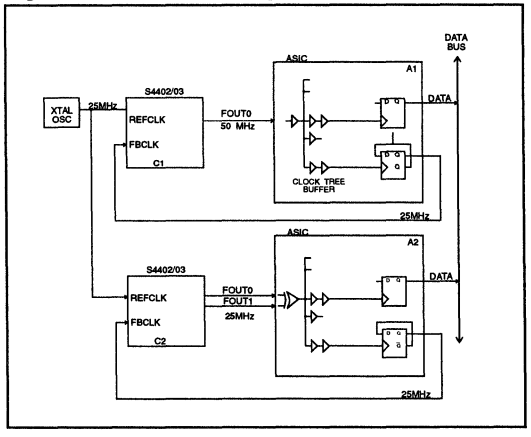
In systems where there are multiple ASICs sharing a common synchronous bus, great care must be taken to ensure that data transfers on the bus can happen as rapidly as possible. Each ASIC must be simulated to ensure that it's data setup, hold, and clock to data output times will work with each of the other chips. The designer must assume that each of the ASICs could be operating at any point on its performance curve; therefore, the propagation delays, setup, and hold times are increased to compensate for the variability of each of the ASICs. These increased specifications for each ASIC reduce the maximum attainable performance of the data bus by consuming a portion of the bus cycle time.

Figure 7 demonstrates a couple of ways to reduce the uncertainty of each ASIC's performance. In this figure, an S4402/03 is used to ensure that the output transitions of each ASIC occur synchronously to the system clock. If all the output transitions on the data bus occur at the same point in time, then the setup times for each ASIC can be minimized. With the clock to data output delays effectively reduced to zero, and the setup and hold times minimized, the available bus bandwidth is increased and data traffic can flow at a higher rate.

In the upper half, C1 takes a 25Mhz master clock and generates a 50Mhz clock for the ASIC A1. This 50Mhz clock is buffered through the ASIC's internal clock buffer tree, before clocking a divide by two output flip flop. This 25Mhz output clock is fed back to the S4402/03 chip and the rising edge of this signal is aligned to the rising edge of the 25Mhz master clock.

In the lower half, C2 takes the 25Mhz master clock and generates two 25Mhz outputs that are in quadrature (90 degrees out of phase with each other). These 25Mhz clocks are exclusive OR'ed inside the ASIC to create the 50Mhz internal clock for

Figure 7. ASIC Deskewing



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the ASIC. This 50Mhz internal clock is again buffered in the same way as the rest of the ASIC clocks, and then divided by two at the output, and aligned with the 25Mhz master clock.

For these two schemes to work correctly, the designer must do three things. The ASIC internal clock buffering must be matched. In other words, the delay from the point at which the buffer tree begins to expand sideways, to the point at which the clocks arrive at the clock input to the output flip flops, must be equal. The output flip flop macros and the delay from the flip flop output to the external pins, must also be equal. And the interconnect length between the ASICs and the S4402/03s must be minimized and equal.

GENERAL GUIDELINES FOR CLOCK DISTRIBUTION

For all of the examples described previously, there are a number of general design guidelines that need to be applied in order to achieve the best performance. These guidelines are:

1. Clock traces need to have equal lengths and impedance.
2. The clock traces must be treated as transmission lines, and therefore use controlled impedance traces.
3. The clock signal termination strategy must be decided early. Series termination will reduce the termination power requirement, but the loads must be clustered at the end of the clock line (<2" stubs).
4. Clock signal capacitive loads must be equal.
5. Do not heavily load the clock output drivers. With heavy loads, two outputs can be paralleled to increase the drive capability.
6. Clocks distributed across backplanes should be point to point connections. This will remove the transit time skew introduced as the signal propagates down the backplane past each board.
7. Be generous with decoupling capacitors. Each power and ground pin of the generators and drivers should be decoupled with 0.1uF ceramic chip capacitors.

SUMMARY

As shown, with careful design of the clocking scheme for a synchronous system, and the correct choice of clock generators and drivers, it is possible to reduce the system clock skew down to 0.4ns to 2.45ns.

The S4402/03 clock generator chips provide the user with the option to tackle the clock distribution problem in many different ways. The controlled output skew of less than 400ps, and the ability to generate clocks at frequencies up to 80Mhz, make the S4402 and S4403 the ideal choice for today's high performance systems.

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CONTENTS

3.3V CLOCK GENERATORS

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12-OUTPUT BiCMOS PLL CLOCK GENERATOR S4LV406

FEATURES

- Generates outputs from 25 MHz to 100 MHz
- Four groups of three outputs (12 outputs total)
- Eight user-selectable output functions for each group
- Proprietary output drivers with:
  - Dual-sloped falling edge
  - On-chip source series termination
  - LVTTL compatible outputs, with <1.5-ns edge rates
- Eliminates ground-bounce and undershoot problems encountered with Bipolar and CMOS drivers
- Performs clock doubling, dividing, invert, lead/lag placement
- Internal VCO running between 50 to 100 MHz
- On-chip loop filter
- Output skew less than 350 ps
- 52 PQFP package
- Operates from 3.3V VCC

APPLICATIONS

- High-performance microprocessor systems
- Compatible with Intel's Pentium™ processor

GENERAL DESCRIPTION

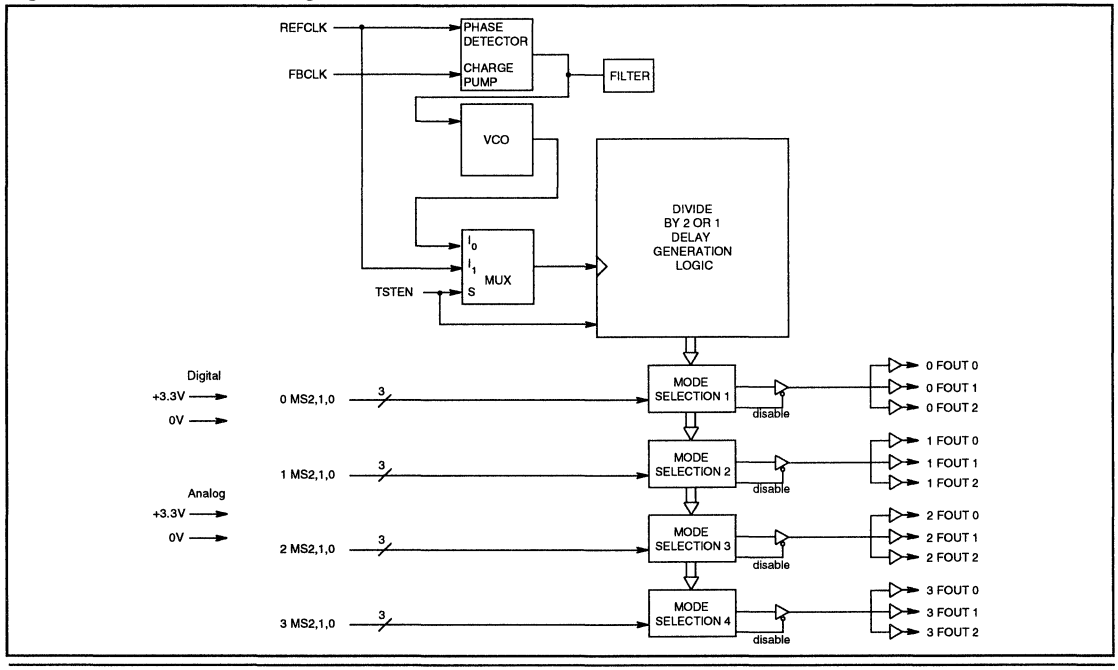
The S4LV406 BiCMOS clock generator provides 12 LVTTL outputs with less than 350 ps of skew. Implemented in AMCC's 1.0µ BiCMOS technology, the internal PLL and divider/delay selector logic allow the user to individually tailor the (4) LVTTL output groups to the system's needs. The internal VCO can operate between 50 to 100 MHz, and the programmability allows the user to generate output clocks in the 25–100 MHz range.

The S4LV406 offers the user the ability to select the appropriate phase and frequency relationship for each of the four groups of three LVTTL clock outputs.

In addition to clock doubling and inversion functions, the S4LV406 allows any output groups to lead or lag the others by the minimum phase delay of 1.25–2.50 ns.

The S4LV406 uses patented complementary (source and sink) 24 mA peak output drivers. These circuits provide "source (series) termination" at the LVTTL outputs that minimize over/undershoot without requiring on-board termination networks. They are designed for a maximum output slew rate of ≈1.5V/ns to minimize simultaneous output-switching noise, distortion, and EMI.

Figure 1. S4LV406 Block Diagram



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FUNCTIONAL DESCRIPTION

The 12 xFOUT0–2 outputs are the main LVTTL output clocks that the generator supplies. The mode selection choices are shown in Table 1 and waveform definitions are given in Figure 2. The "x" represents the output group number (1–4). The frequency of these outputs is determined by the REFCLK clock frequency and the output clock that is tied to the FBCLK input (xFOUT0–2 can be equal to REFCLK, half of REFCLK, or twice the frequency of REFCLK).

Example:

In order to meet bus timing specifications for a typical system, designers may need three outputs at 66 MHz for the system clock and processor, a 33-MHz output for the cache controller, and a 33-MHz delayed output for a memory management unit. This system requirement can be met using the S4LV406 by setting the mode select pins for the first group of outputs (0MS2,1,0) to 111, the second group (1MS2,1,0) to 110, and the third group (2MS2,1,0) to 101. In this configuration, one of the 33-MHz outputs should be fed back to the FBCLK input. This example makes use of only three of the four output banks, leaving the fourth available for any other clock signals needed.

Table 1. Mode Selection Options

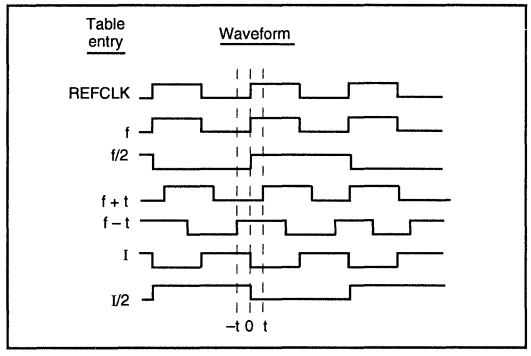
xMS2,1,0	MODE DESCRIPTION	xFOUT0,1,2
000	Disabled.	Logical Hi
001	All three outputs at the fundamental output frequency, but early by a minimum phase delay.	f – t
010	All three outputs at half the fundamental output frequency and inverted.	I /2
011	All three outputs at the fundamental output frequency and inverted.	I
100	All three outputs at half the fundamental output frequency, but delayed by a minimum phase delay.	f/2 + t
101	All three outputs at the fundamental output frequency, but delayed by a minimum phase delay.	f + t
110	All three outputs at half the fundamental output frequency.	f/2
111	All three outputs at the fundamental output frequency.	f

Note: If f is fed back, the fundamental frequency is equal to REFCLK. If f/2 is fed back, the fundamental frequency is twice REFCLK.

Phase Delay

The minimum phase delay between xFOUT0–2 signals is a function of the VCO frequency. The VCO frequency is equal to the fundamental output frequency. The minimum phase delay is equal to the period of the VCO frequency divided by 8: t = 1/(VCO freq x 8). Since the VCO can operate in the 50-MHz to 100-MHz range, the range of minimum phase delay values is 1.25 ns to 2.50 ns (See Table 2).

Figure 2. Waveform Definitions



Test Capabilities

TESTEN allows the chip to use the REFCLK input instead of the VCO output to clock the chip. By-passing the VCO and using REFCLK makes the S4LV406 into a programmable clock buffer, however, the programmable mode choices are limited. The VCO is needed to create the inversion and minimum phase delay modes. So when TESTEN is active, the only options are XMS2,1,0 = 000,110, and 111, for each bank of outputs.

Table 2. VCO Operating Frequencies

xFOUT0–2	VCO FREQ	MIN PHASE DELAY
100 MHZ	100 MHZ	1.25 ns
80 MHz	80 MHz	1.56 ns
66 MHz	66 MHz	1.89 ns
50 MHz	50 MHz	2.50 ns
33 MHz*	66 MHz	1.89 ns
25 MHz*	50 MHz	2.50 ns

* The bank containing the output used as feedback must be in one of the f/2 modes to ensure the VCO is operating within its 50-100 MHz range.

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Power Supply Considerations

Power for the analog portion of the S4LV406 chips must be isolated from the digital power supplies to minimize noise on the analog power supply pins. This isolation between the analog and digital power supplies can be accomplished with a simple external power supply filter (Figure 3). The analog power planes are connected to the digital power planes through single ferrite beads (FB1 and FB2) or inductors capable of handling 25 mA. The recommended value for the inductors is in the range from 5 to 100µH, and depends upon the frequency spectrum of the digital power supply noise. The ferrite beads should exhibit 75Ω impedance at 10 MHz.

Decoupling capacitors are also very important to minimize noise. The decoupling capacitors must have low lead inductance to be effective, so ceramic chip capacitors are recommended. Decoupling capacitors should be located as close to the power pins as physically possible. And the decoupling should be placed on the top surface of the board between the part and its connections to the power and ground planes.

Figure 3. External Power Supply Filter

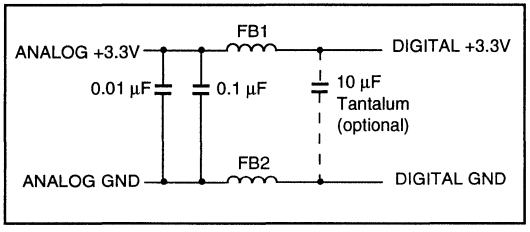
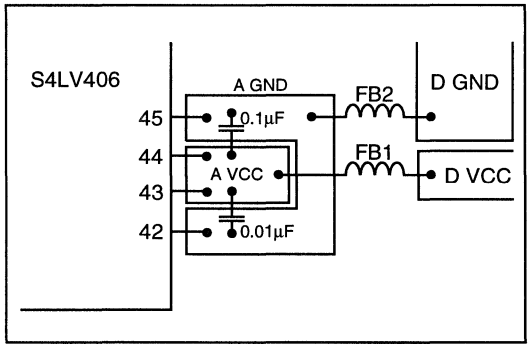


Figure 4. Board Layout



BOARD LAYOUT CONSIDERATIONS

• The S4LV406 chips are sensitive to noise on the Analog supplies. Care should be taken during board layout for optimum results.

• All decoupling capacitors (C1–C4 = 0.1 µF) should be bypassed between VCC and GND, and placed as close to the chip as possible (preferably using ceramic chip caps) and placed on top of board between S4LV406 and the power and ground plane connections.

• The analog VCC supply can be a filtered digital VCC supply as shown below. The ferrite beads or inductors, FB1 and FB2, should be placed within three inches of the chip. The analog decoupling capacitors must be placed within 1/8 inch of the analog supply pins on the top surface of the board.

• The analog VCC plane should be separated from the digital VCC and ground planes by at least 1/8 inch.

PIN DESCRIPTIONS

Input Signals

REFCLK. Frequency reference supplied by the user that, along with the output tied to the FBCLK input, determines the frequency of the outputs. Also replaces the VCO output when TSTEN is high. See TSTEN.

FBCLK. Feedback clock that, along with the REFCLK input, determines the frequency of the outputs. One output is selected to feed back to this input.

TSTEN. Active High. Allows REFCLK to drive the divider phase adjust circuitry, after the first divide-by-two stage. Also, when brought High, generates an internal Reset pulse that initializes the internal counter flip-flops to zero.

xMS2,1,0. Mode selection inputs that allow selection of the phase and frequency relationship of each of the four banks of three clock outputs. The "x" represents the output group number (0–3). Refer to Table 1 for mode selection options.

Output Signals

xFOUT0–2. Clock signal outputs. Refer to Table 1 and Figure 3 for a description of output options.

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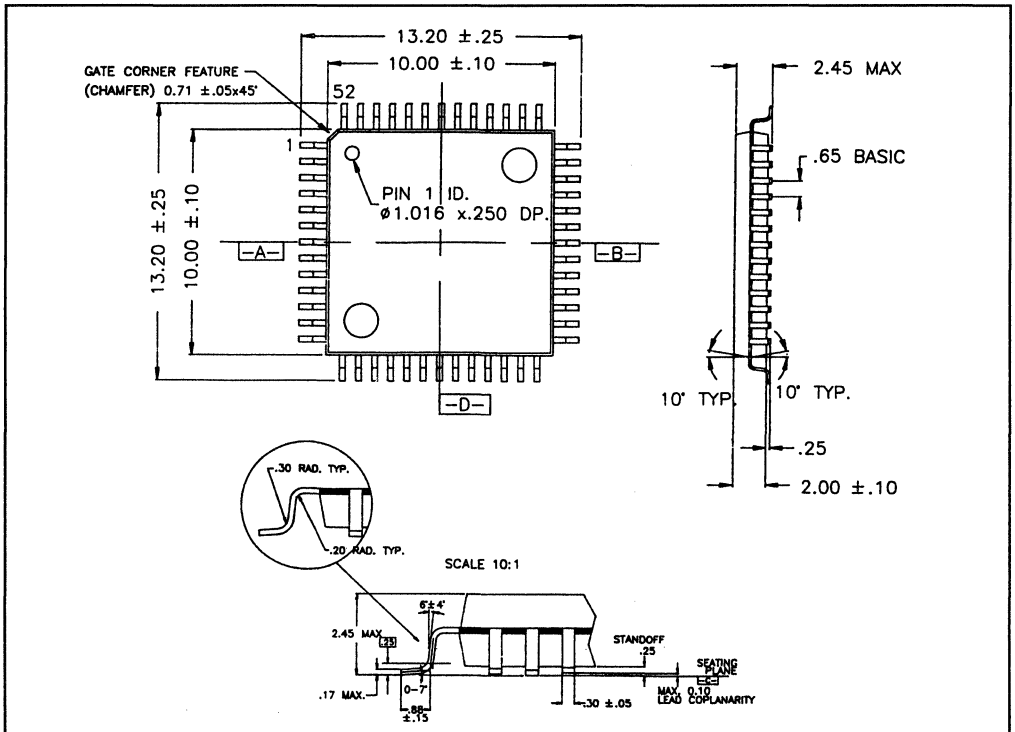
Figure 5. 52–pin PQFP Package



Dimensions are in mm. Dimensional tolerance shall be ±0.050 unless otherwise specified.

DC CHARACTERISTICS

Symbol	Parameter	DC Test Conditions	Min	Typ[1]	Max	Units
V_{IH}[2]	Input HIGH Voltage	Guaranteed input HIGH voltage for all inputs	2.0			V
V_{IL}[2]	Input LOW Voltage	Guaranteed input LOW voltage for all inputs			0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} = Min, I_{IN} = -18 mA		-0.8	-1.2	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min | I_{OH} = -2 mA[3]	2.4		V_{CC}+.3	V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 2 mA[3]			0.4	V
I_{IH}	Input HIGH Current	V_{CC} = Min, V_{IN} = 2.4V			50	µA
I_{IL}	Input LOW Current	V_{CC} = Min, V_{IN} = 0.5V			-50	µA
I_{OS}[4]	Output short circuit current	V_{CC} = Max, V_{OUT} = 0V	-55			mA
I_{CC}	Static	V_{CC} = Max			75	mA
I_{CCT}	Total I_{CC} (Dynamic and Static)	C_{LOAD} = 10 pF at 80 MHz			210	mA

1. Typical limits are at 25°C, V_{cc} = 3.3V.
2. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.
3. I_{OH}/I_{OL} values indicated are for DC test correlation. Actual dynamic currents are significantly higher. Includes 100mV for on-chip series termination.
4. Maximum test duration one second.

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ABSOLUTE MAXIMUM RATINGS

LVTTL Supply Voltage VCC	-0.5V to 4.6V
LVTTL Input Voltage	-0.5V to Vcc + 0.5V
Operating Temperature	0°C to 70°C ambient
Operating Junction Temperature TJ	+ 140°C
Storage Temperature	-55°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Nom	Max	Units
LVTTL Supply Voltage (VCC)	3.0	3.3	3.6	V
Operating Temperature	0 (ambient)	—	70 (ambient)	°C
Junction Temperature	—	—	140	°C

Table 3. AC Specifications

Symbol	Description	Min	Max	Units
f_{VCO}	VCO Frequency	50	100	MHz
f_{REF}	REFCLK Frequency	25	100	MHz
t_{IRF}	Input Rise/Fall Time	1	3	ns
MPW_{REF}	REFCLK Minimum Pulse Width	5.0		ns
t_{PE}	Phase Error between REFCLK and FBCLK	-250	+250	ps
t_{PED}	Phase Error Difference from Part to Part[1]	0	300	ps
t_{SKEW}	Output Skew[2] across all outputs	0	350	ps
t_{SKEWA}	Output Skew[2] within any bank	0	250	ps
t_{DC}	Output Duty Cycle[3]	45	55	%
f_{FOUT}	FOUT Frequency[4]	25	100	MHz
t_{PS}	Nominal Phase Shift Increment[5]	1.25	2.50	ns
t_j	Clock Stability[6]		250	ps
t_{ORF}	FOUT Rise/Fall Time[7]	0.5	1.5	ns
t_{LOCK}	Loop Acquisition Time[8]		5	ms
t_{PSV}	Phase Shift Variation[5]	-100	+100	ps

1. Difference in phase error between two parts at the same voltage, temperature and frequency.
2. Output skew guaranteed for equal loading at each output.
3. Outputs loaded with 10 pF, measured at 1.5 V.
4. C_{LOAD} = 10 pF.
5. All phase shift increments and variation are measured relative to 0FOUT0 at 1.5 V.
6. Clock period jitter with all FOUT outputs operating at 80MHz loaded with 10 pF. Parameter guaranteed, but not tested.
7. With 10 pF output loading (0.8 V to 2.0 V transition).
8. Depends on loop filter chosen. (Number given is for example filter.)

Figure 6. Timing Waveforms

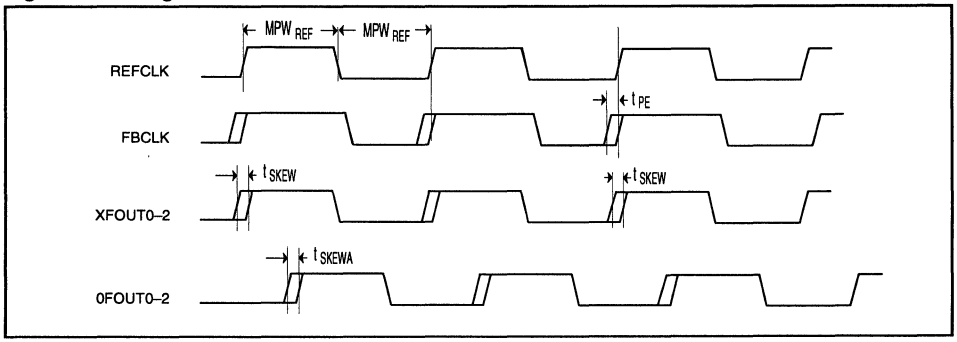

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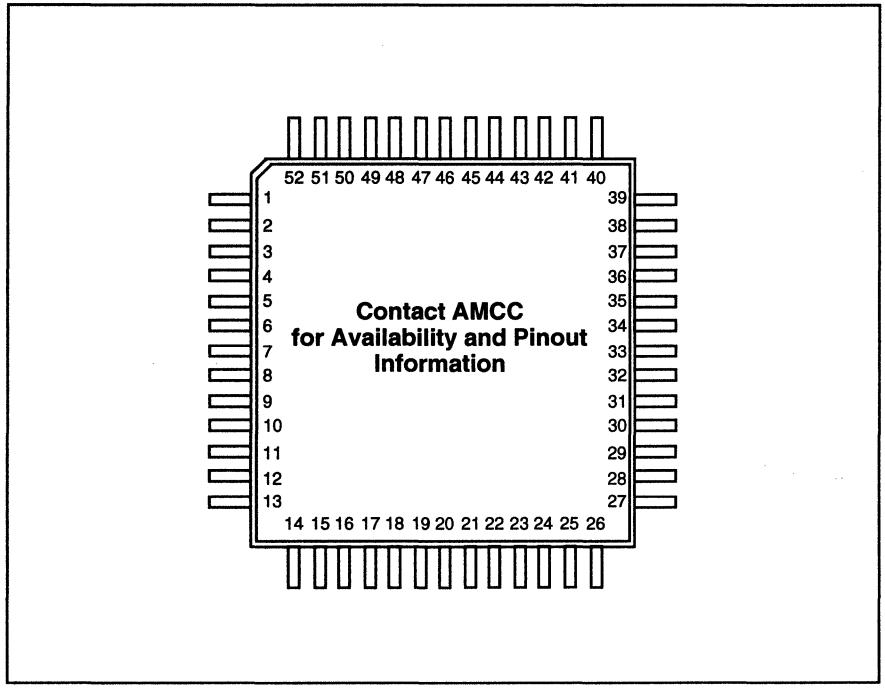
Figure 7. S4LV406 Pinout



Ordering Information

GRADE	PLL CLOCK GENERATOR	PACKAGE
S–Commercial	S4LV406	Q–52 PQFP

X	XXXX	X
Grade	Part number	Package

Applied Micro Circuits Corporation
6195 Lusk Blvd., San Diego, CA 92121 • (619) 450-9333

RAMBUS™ COMPATIBLE CLOCK GENERATOR S4505S

FEATURES

- Provides two Rambus compatible clock outputs from 240 to 270 MHz
- Uses low cost 14.318 MHz crystal as reference for 267 MHz output
- Low Jitter, <150 ps
- Output skew <100ps
- 45/55% duty cycle
- On-chip filter requires no external components
- Eight-pin, .150" SOIC
- Operates from a single 3.3V ±10% supply
- Series resonant input crystal requires no external components

APPLICATIONS—RDRAM BASED

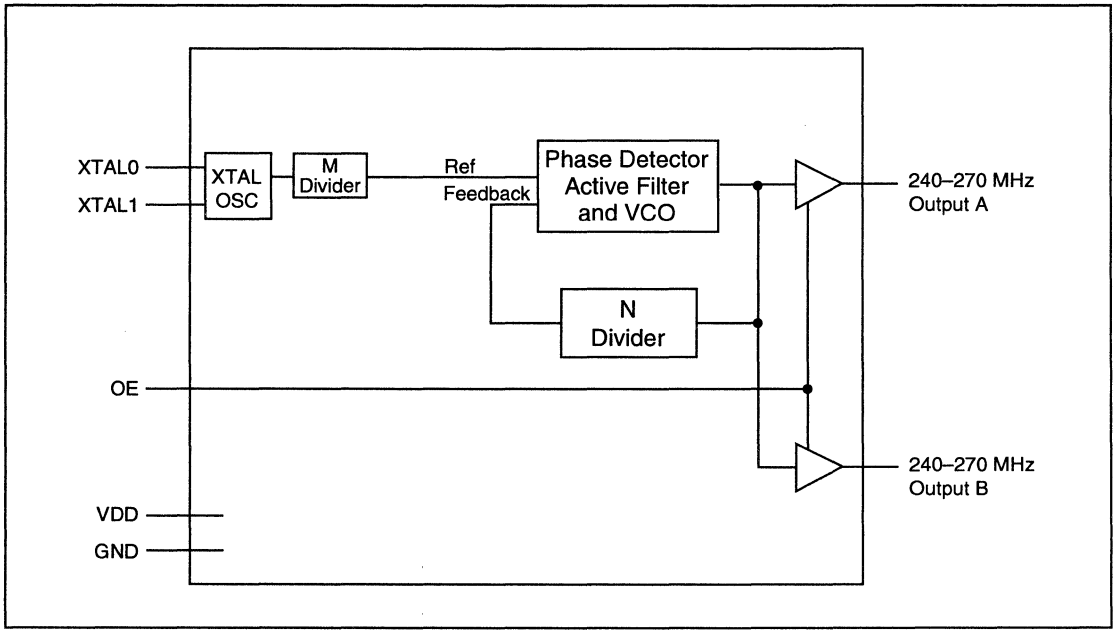
- Graphics Accelerators
- PC Memory
- Set-Top Boxes
- Games

DESCRIPTION

AMCC's advanced PLL technology allows the S4505S to provide two Rambus-compatible, 267 MHz clocks from a low cost 14.318 MHz crystal. Other reference crystals can be used to produce other output frequencies within the 240–270 MHz range. An external series resistor allows the output to be matched to the Rambus transmission line impedance needed for each application.

AMCC utilizes its high speed, low-jitter PLL technology developed for telecom and precision clocking applications to provide outputs which meet the low jitter and symmetrical duty cycle requirements of RAMBUS system clocks.

Figure 1. Block Diagram



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Absolute Maximum Ratings

Parameter	Description	Value	Unit
V_{DD}	Power supply vs. GND	-0.5 to +5.0	V
V_{IN}	Input voltage, and pin vs. GND	-0.5 to V_{DD} +0.5	V
Storage Temp.	Maximum temperature during storage	170°	°C

Note: Stresses greater than the absolute maximum ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated under the normal operating conditions is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Specifications (T_A = 0°C – 70°C, V_{DD} = 3.3 ± 0.3V)

Parameter	Description	Conditions	Min	Max	Unit
V_{IH}	Input HIGH voltage	OE Pin	2.0		V
V_{IL}	Input LOW voltage	OE Pin		0.8	V
I_{IH}	Input HIGH current	OE Pin		50	uA
I_{IL}	Input LOW current	OE Pin – Internal pull-up		300	uA
P_D	Power Dissipation	Dynamic		350	mW

Output Characteristics
All specifications are compatible with Rambus requirements.

Symbol	Description	Comments	Min	Typ	Max	Unit
Z_0	Line impedance	Rambus compatible	25		50	Ω
V_{TERM}	Line termination voltage	Rambus compatible	2.45		2.9	V
V_T	Switching threshold voltage	Rambus compatible	1.9		2.4	V
V_S	Output voltage swing	Rambus compatible	1.1		1.6	V

AC Specifications (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 3.3V ± 0.3V)
All specifications are compatible with Rambus requirements.

Symbol	Description	Test Condition	Min	Typ	Max	Unit
F_{XTAL}	Crystal frequency		12.86	14.318	14.46	MHz
F_{OUT}	Output frequency	Typ with 14.318 MHz input[1]	240	267	270	MHz
F_{ACC}	Frequency accuracy	Using 50 ppm crystal	-1500		+500	PPM
T_R, T_F	Output clock rise/fall time	20% to 80%	0.2		0.5	ns
T_{DC}	Duty cycle	STD Rambus System Load	45	50	55	%
T_{JPP}	Jitter, peak-to-peak			50	150	ps
T_{PU}	Power-up time	From OFF to clocks stable			10	ms
T_{SKEW}	Output A to B skew	Equal loads			100	ps

1. Output frequency multiplier is 56/3 times the input crystal frequency.

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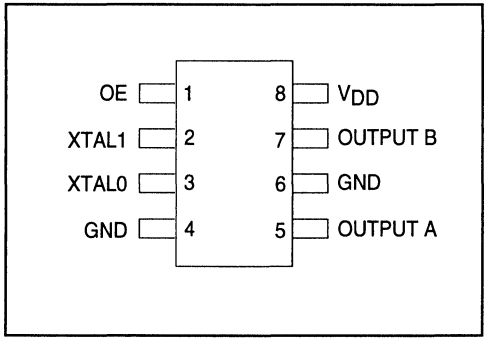
S4505S Pinout — 8-Pin SOIC



Pin Descriptions

Pin #	Description
1	Output enable, Active HIGH, Internal pull-up
2	Crystal connection, nominally 14.318 MHz for 267 MHz output
3	Crystal connection — Series Resonant
4, 6	Ground
5, 7	Output A, B — 240–270 MHz clock outputs, open drain — should be terminated externally to match Rambus specifications
8	Power — 3.3V ± 10%

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