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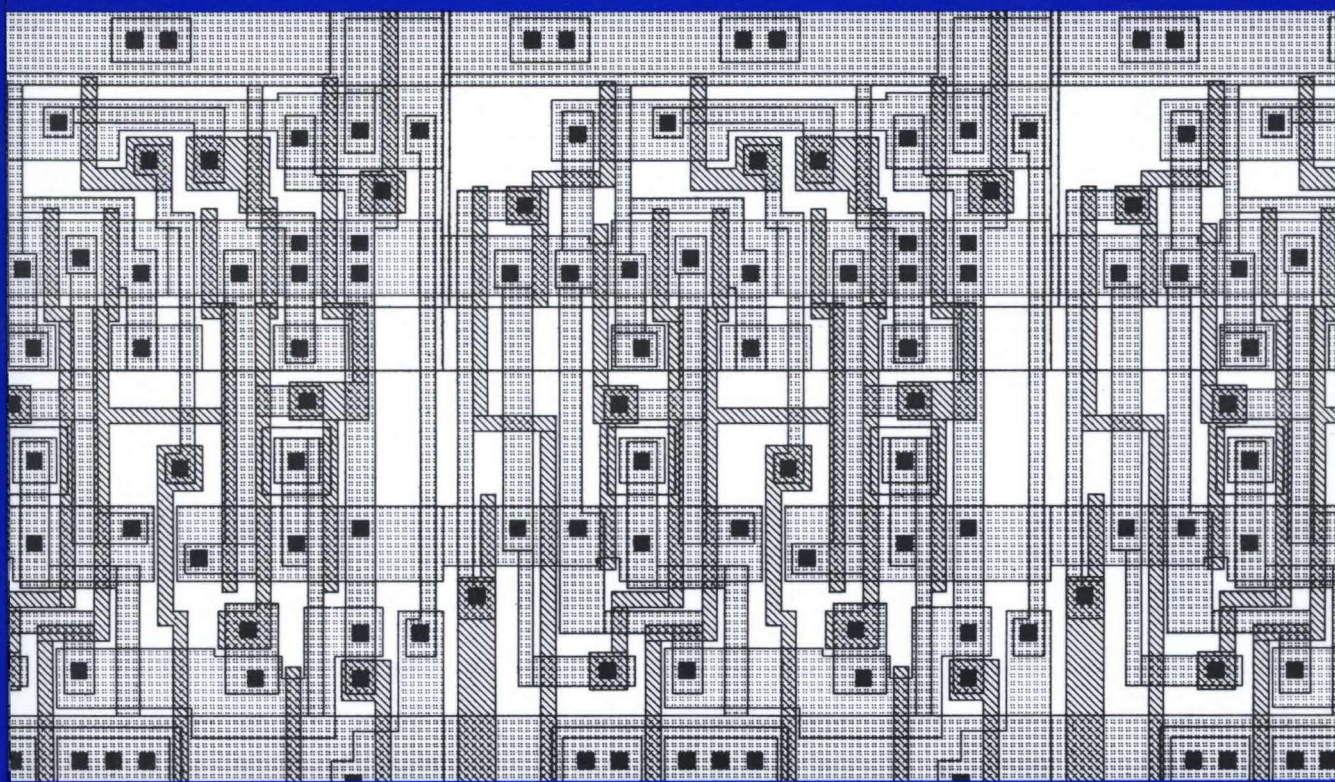

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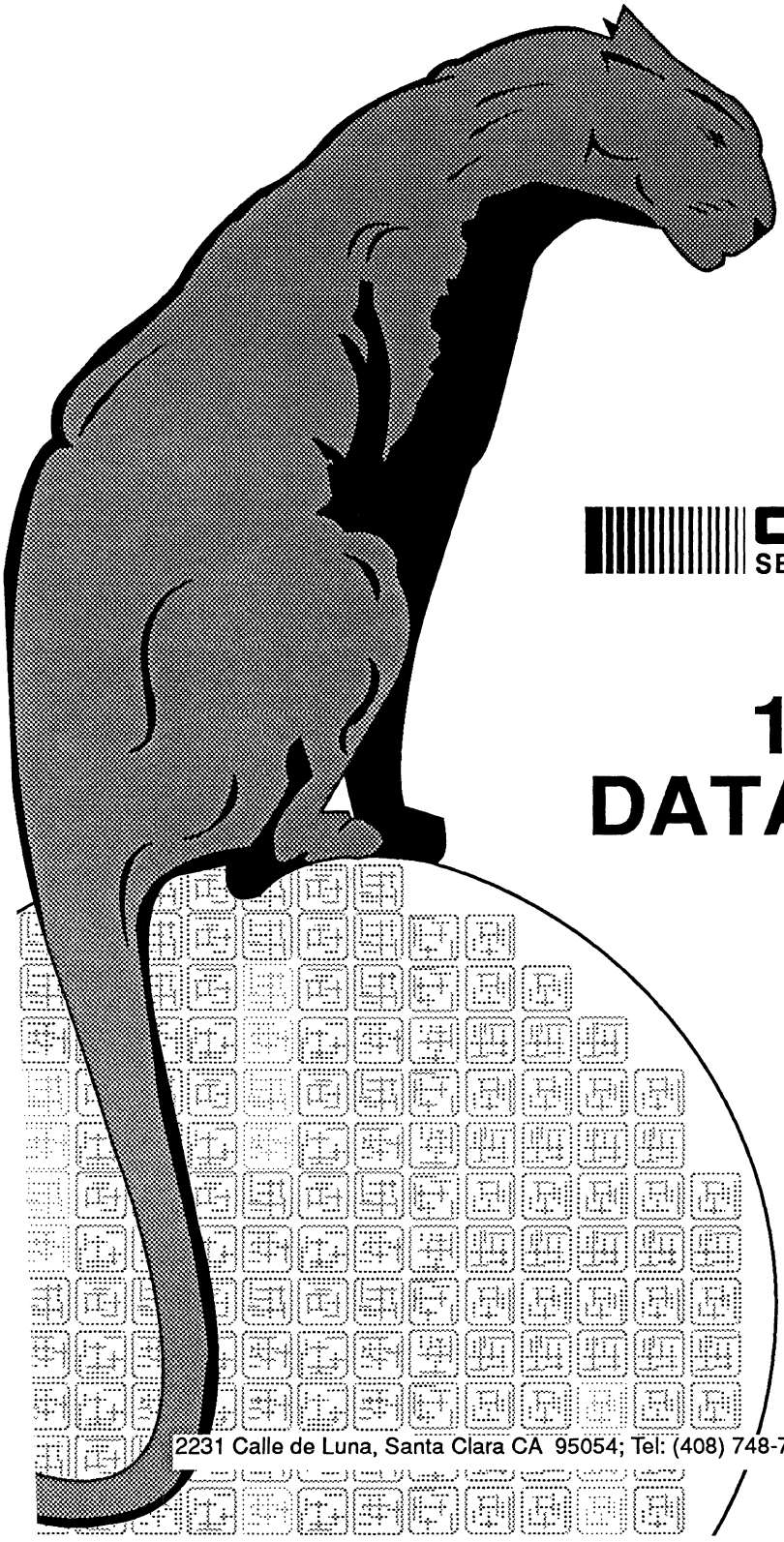

CATALYST
SEMICONDUCTOR, INC.

1989
DATA BOOK

2231 Calle de Luna, Santa Clara CA 95054; Tel: (408) 748-7700; Fax: (408) 980-9209

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President's Message

April 1989

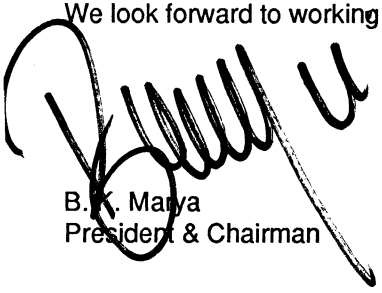
Dear Customer,

1989 is developing into an exciting year for us at Catalyst Semiconductor. During the past year we expanded at an unprecedented rate. We dramatically increased our production and the breadth of our product family offering, learning and improving as we grew to meet the challenge. Now we are positioned to support this accelerating growth rate. In 1989 we are introducing a number of new leading edge semiconductor products.

To ensure our customers the advantage of low-cost, high-volume manufacturing, we have established long-term strategic alliances with several major semiconductor manufacturers. These alliances give us access to some of the most advanced fabrication facilities in the world. We have defined strict quality control standards with these foundries, resulting in products of distinguished quality and reliability.

Catalyst Semiconductor is in the business of providing integrated circuits which enhance your electronic systems' performance, thereby giving you a competitive edge in your marketplace. In our view, you, our customer, have not simply purchased IC's; you've secured our commitment to your company and your business. Since our founding in 1985, we have found that relationships based on this commitment result in the development of trust, support and mutual prosperity. Such is the foundation of long-term corporate partnerships, and these are what the future of Catalyst is being designed to secure.

We look forward to working with you in a dynamic and rewarding relationship.



B.K. Manya
President & Chairman

PRODUCT SELECTION GUIDE

PARALLEL E²PROMs

CMOS

Device	Temp Range	Size (Organization)	Access Time (ns)	Package Types	Data Book Section
CAT28C16A	C,I	16K Bit (2Kx8)	200	Plastic DIP PLCC	3
CAT28C17A	C,I	16K Bit (2Kx8)	200	Plastic DIP PLCC	3
CAT28C64A	C,I	64K Bit (8Kx8)	120/150/200	Plastic DIP Small Outline	3
CAT28C65A	C,I	64K Bit (8Kx8)	120/150/200	Plastic DIP Small Outline	3
CAT28C256	C,I	256K Bit (32Kx8)	200/250/300	Plastic DIP	3

SERIAL E²PROMs

CMOS

Device	Temp Range	Compatibility	Size (Organization)	Maximum Clock Frequency	Package Types	Data Book Section
CAT93C46A	C,I	National 9346	1K Bit (64x16)	250KHz	Plastic DIP Small Outline	3
CAT93C46	C,I	National 9346	1K Bit (x8 or x16)[3]	250KHz	Plastic DIP Small Outline	3
CAT93C46H ★	C,I	National 9346	1K Bit (x8 or x16)[3]	250KHz	Plastic DIP Small Outline	3
CAT59C11	C,I	G.I. 5911	1K Bit (x8 or x16)[3]	250KHz	Plastic DIP Small Outline	3
CAT59C11A	C,I	G.I. 5911	1K Bit (x8 or x16)[3]	250KHz	Plastic DIP Small Outline	3
CAT59C11H★	C,I	G.I. 5911	1K Bit (x8 or x16)	250KHz	Plastic DIP Small Outline	3
CAT35C102[2]	C,I	National 9346 UPGRADE	2K Bit (x8 or x16)[3]	1MHz	Plastic DIP Small Outline	3
CAT35C202[2]	C,I	G.I. 5911 UPGRADE	2K Bit (x8 or x16)[3]	1MHz	Plastic DIP Small Outline	3
CAT33C104[1]	C,I	National 9346 UPGRADE	4K Bit (x8 or x16)[3]	250KHz	Plastic DIP Small Outline	3
CAT35C104[2]	C,I	National 9346 UPGRADE	4K Bit (x8 or x16)[3]	1MHz	Plastic DIP Small Outline	3

SECURE ACCESS SERIAL E²PROMs

CMOS

Device	Protocol	Size (Organization)	Temp Range	Maximum Clock Frequency	Package Types	Data Book Section
CAT33C704[1] CAT35C704	Synchronous	4K Bit (x8 or x16)[3]	C,I	5 MHz	Chip on Board Plastic DIP CERDIP Small Outline	4
CAT33C804[1] CAT35C804	UART Compatible					

PRODUCT SELECTION GUIDE

CMOS EPROMs

Device	Temp Range	Size (Organization)	Access Time (ns)	Package Types	Data Book Section
CAT27HC256	C	256K Bit (32Kx8)	55/70/90	CERDIP LCC	2
	I,M		70/90/120		
CAT27HC256L	C		55/70/90		
	I,M		70/90/120		
CAT27C210	C	1M Bit (64Kx16)	150/170/200/250	CERDIP	2

NMOS EPROMs

Device	Temp Range	Size (Organization)	Access Time (ns)	Package Types	Data Book Section
CAT2764A (OTP)	C	64K Bit (8Kx8)	150	Plastic DIP	2
CAT27128A (OTP)	C	128K Bit (16Kx8)	150	Plastic DIP	2
CAT27256 (OTP)	C	256K Bit (32Kx8)	170	Plastic DIP	2
CAT27512 (OTP)	C	512K Bit (64Kx8)	150/200	Plastic DIP PLCC	2
CAT27010 (OTP)	C	1M Bit (128Kx8)	150/170/200	Plastic DIP	2
CAT27010 (UV)			150	CERDIP	

CMOS NVRAMs

Device	Temp Range	Compatibility	Size (Organization)	Maximum Speed	Package Types	Data Book Section
CAT22C10	C,I	Xicor	256 Bit (64x4)	200/300ns	Plastic DIP	1
CAT22C12	C,I	Xicor	1K Bit (256x4)	200/300ns	Plastic DIP	1
CAT24C44	C,I	Xicor	256 Bit (16x16) Serial	1MHz	Plastic DIP	1

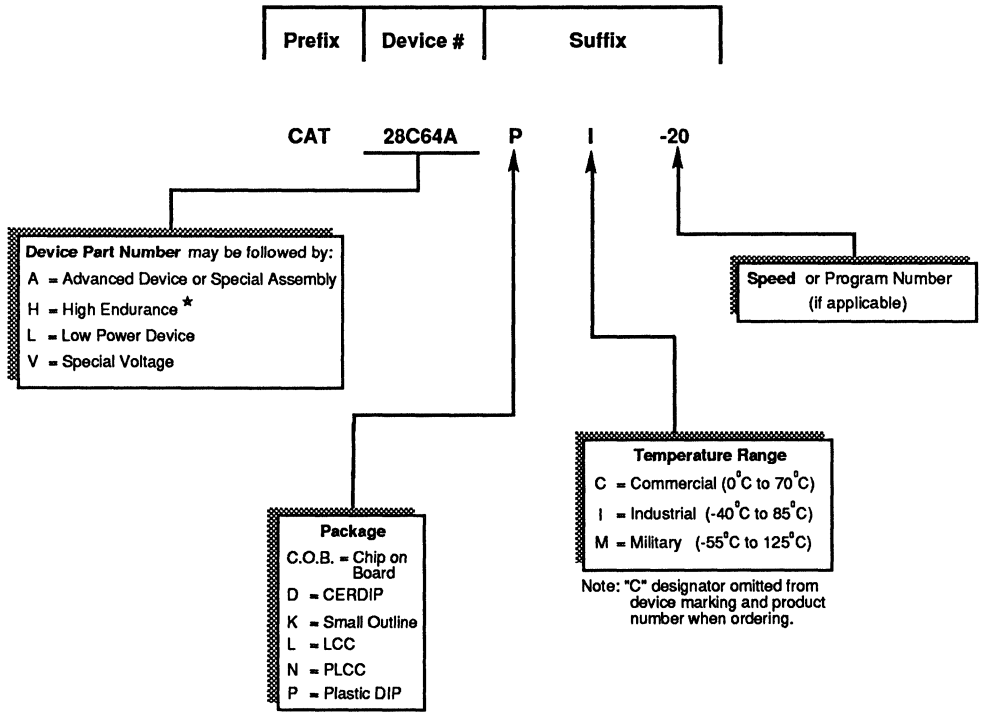
CMOS STATIC RAMs

Device	Temp Range	Size (Organization)	Access Time (ns)	Package Types	Data Book Section
CAT71C256 CAT71C256L	C	256K Bit (32Kx8)	85	Plastic DIP	5

1. 3-Volt-only device
2. Soon to be offered as High Endurance device *
3. User configurable

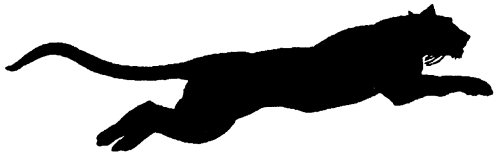
* High Endurance Device: minimum 100,000 write/erase cycles and 100 year data retention.

ORDERING INFORMATION



The device used in the example above is a CAT28C64API-20 (Plastic DIP, Industrial temperature, 200ns access time).

* **High Endurance Device: minimum 100,000 write/erase cycles and 100 year data retention.**



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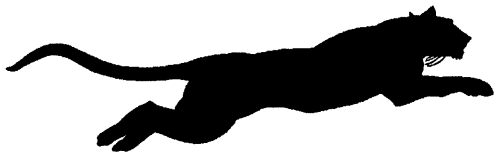
*High Endurance Device: minimum 100,000 read/erase cycles and 100 year data retention



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CATALYST INDUSTRIAL TEMPERATURE RANGE DEVICES

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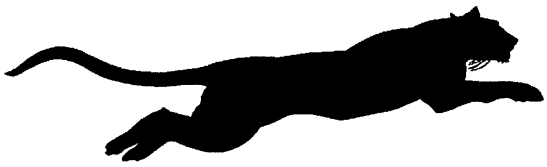
CATALYST MILITARY TEMPERATURE RANGE DEVICES



SECTION 1

NVRAMS

COMMERCIAL TEMPERATURE RANGE

INDUSTRIAL TEMPERATURE RANGE

CAT22C10
256-BIT (64x4) NONVOLATILE CMOS STATIC RAM

DESCRIPTION

The Catalyst CAT22C10 Nonvolatile Random Access Memory (NVRAM) is a 256-bit device with a 64x4 organization. It features fully static CMOS circuitry for very low power consumption. The active current is 40mA and the standby current is 30µA.

An internal E^2PROM array provides bit-by-bit back-up for the static RAM array. Store operations write data from the RAM array to the E^2PROM array. Recall operations write data from the E^2PROM array to the RAM array.

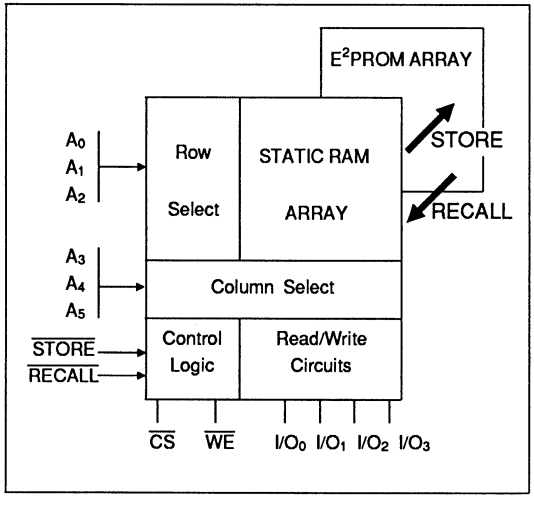
Data retention for each store cycle is specified for over 10 years, and over 10,000 store operations can be performed reliably. Unlimited recall operations, and read and write operations to the RAM are further specified.

The CAT22C10 has internal false store protection circuitry, which prohibits any store operation for V_{CC} less than 3.5V (typically) to ensure the integrity of the E^2PROM data. Other internal circuitry performs an automatic recall operation upon V_{CC} power-up.

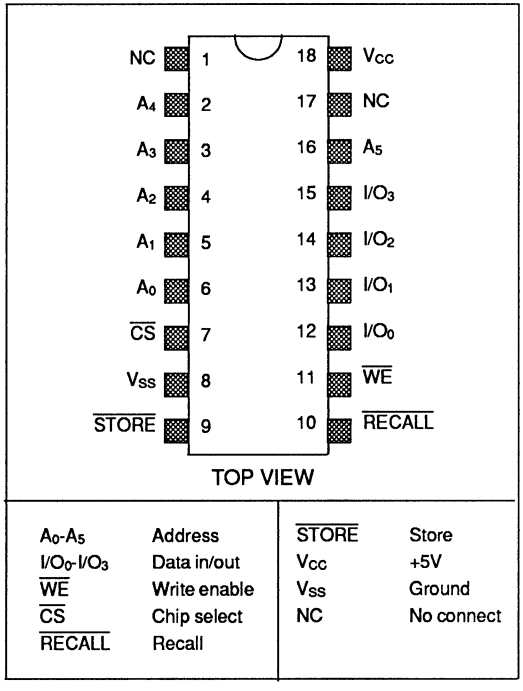
FEATURES

- CMOS technology - completely static operation
- Low current consumption
  - Active: 40mA max
  - Standby: 30µA max
- Single power supply (+5V ±10%)
- RAM access time 200ns, and 300ns
- Fully TTL and CMOS compatible
- JEDEC standard 18-pin 300-mil package
- Write protect circuit to preserve data on power-up and power-down
- Automatic recall on power-up
- 3-state output
- Short store pulse: 200ns
- Short recall pulse: 300ns
- False store protection below 3.5V operation level
- 10,000 nonvolatile store cycles per bit

BLOCK DIAGRAM



PIN CONFIGURATION



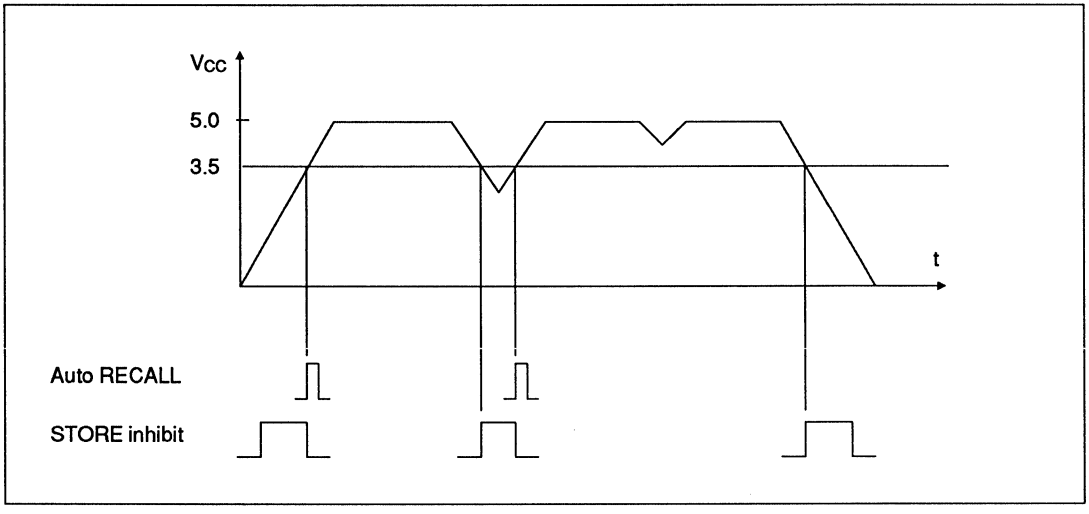
A_0-A_5	Address	STORE	Store
I/O_0-I/O_3	Data in/out	V_{CC}	+5V
WE	Write enable	V_{SS}	Ground
CS	Chip select	NC	No connect
RECALL	Recall		

MODES OF OPERATION

Input				Input/Output	Mode
$\overline{CS}$	$\overline{WE}$	$\overline{RECALL}$	$\overline{STORE}$		
H	-	H	H	Output high impedance	Standby
L	H	H	H	Output data	RAM Read
L	L	H	H	Input data	RAM Write
-	H	L	H	Output high impedence RECALL	(E^2PROM→RAM)
H	-	L	H	Output high impedence RECALL	(E^2PROM→RAM)
-	H	H	L	Output high impedence STORE	(RAM→E^2PROM)
H	-	H	L	Output high impedence STORE	(RAM→E^2PROM)

NOTES:

- $\overline{RECALL}$ signal has priority over $\overline{STORE}$ signal when both are applied at the same time
- $\overline{STORE}$ is inhibited when $\overline{RECALL}$ is active
- The auto recall is activated on power-up when V_{CC} reaches ≈3.5V
- The store operation is inhibited when V_{CC} is below ≈3.5V
- V_{CC} rise and fall time should be between 10ms and 1000ms



MAXIMUM RATINGS *

Storage temperature	-65°C to +150°C
Temperature under bias	-40°C to +85°C
Power supply (V_{CC})	-0.3 to +6V
Input voltage	-0.3 to +6V
Output voltage	0.0 to +6V
Output current	5mA
Lead temperature (soldering for 10 seconds)	260°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CCO}	Current consumption (operating)	All input = 5.5V T_A = 0°C All outputs unloaded		15	40	mA
I_{CCS}	Current consumption (standby)				30	µA
I_{LI}	Input current	$0 \le V_{IN} \le 5.5V$		0.1	10	µA
I_{LO}	Output leakage current	$0 \le V_{OUT} \le 5.5V$		0.1	10	µA
V_{IH}	High level input voltage		2.0		V_{CC}	V
V_{IL}	Low level input voltage		0.0		0.8	V
V_{OH}	High level output voltage	I_{OH} = -2mA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 4.2mA			0.4	V
V_{DH}	RAM data holding voltage	V_{CC}	1.5		5.5	V

CAPACITANCE

(T_A= 25°C, f = 1.0MHz, V_{CC} = 5V)

Symbol	Parameter	Conditions	Limits Typ. max.	Unit
$C_{I/O}$	Input/Output capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input capacitance	V_{IN} = 0V	6	pF

Note: These parameters are periodically sampled and are not 100% tested.

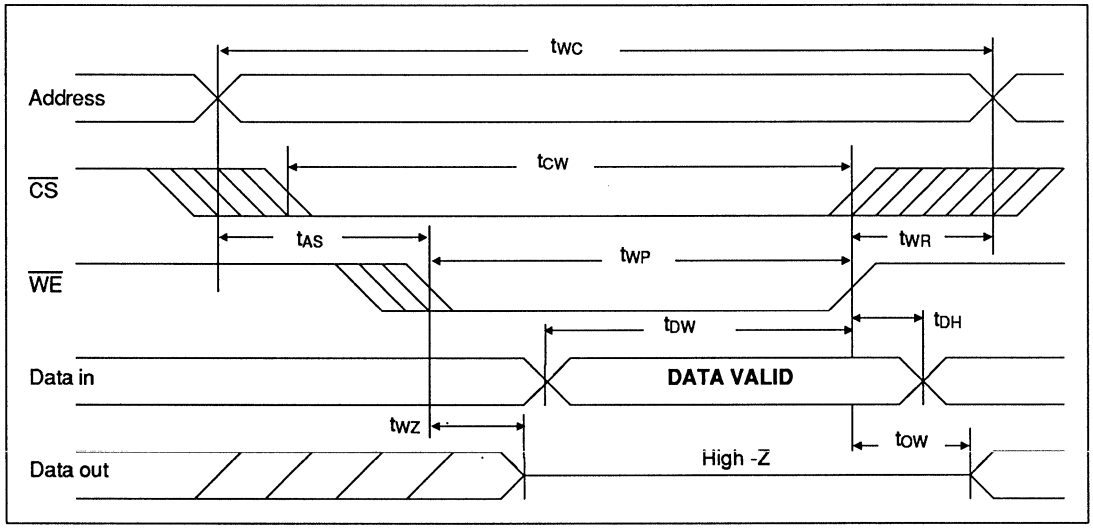
AC CHARACTERISTICS < Write Cycle>

(T_A = 0°C to +70°C)

Symbol	Parameter	Conditions	22C10-20 Min.	22C10-20 Max.	22C10-30 Min.	22C10-30 Max.	Units
t_{WC}	Write cycle time	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1 TTL gate V_{OH} = 2.2V V_{OL} = 0.65V V_{IH} = 2.2V V_{IL} = 0.65	200		300		ns
t_{CW}	$\overline{CS}$ write pulse width		150		150		ns
t_{AS}	Address set-up time		50		50		ns
t_{WP}	Write pulse width		150		150		ns
t_{WR}	Write recovery time		25		25		ns
t_{DW}	Data valid time		100		100		ns
t_{DH}	Data hold time		20		20		ns
t_{WZ}	Output disable time		10	100	10	100	ns
t_{OW}	Output enable time		10		10		ns

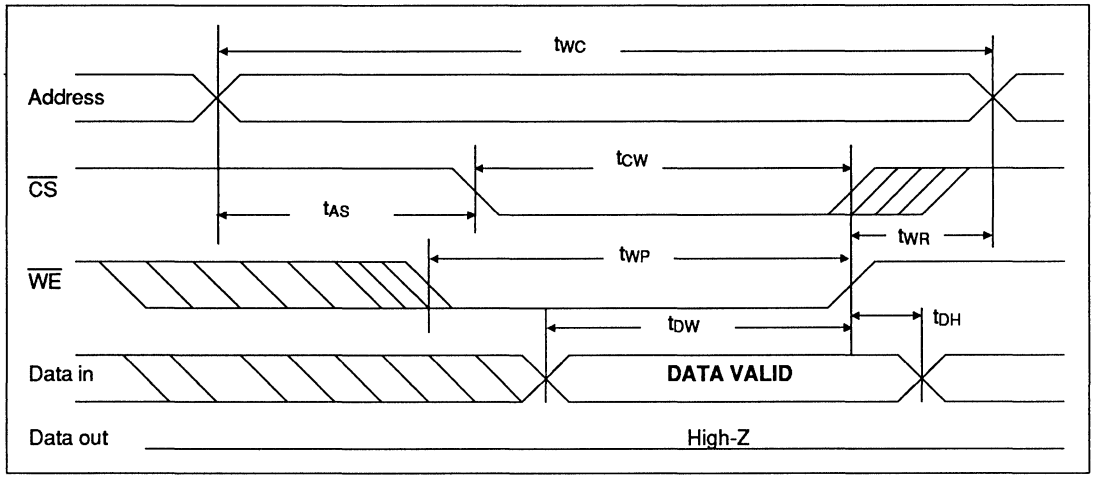
AC CHARACTERISTICS <Write Cycle>

(T_A = 0°C to +70°C)



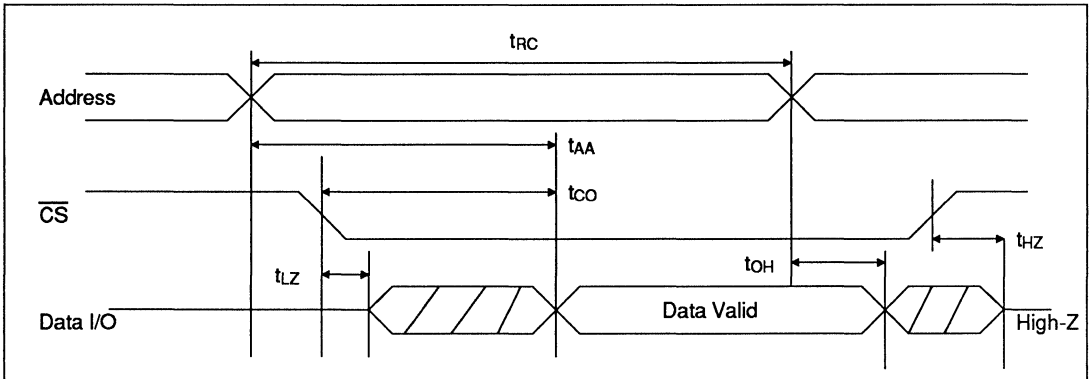
AC CHARACTERISTICS <Early Write Cycle>

(T_A = 0°C to +70°C)



AC CHARACTERISTICS <Read Cycle>

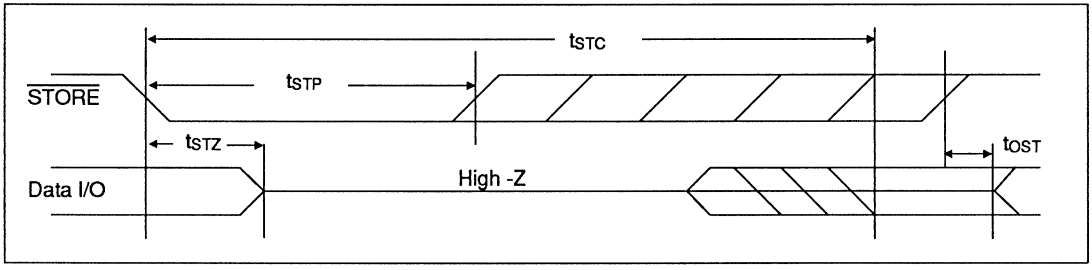
(T_A = 0°C to +70°C)



Symbol	Parameter	Conditions	22C10-20 Min.	22C10-20 Max.	22C10-30 Min.	22C10-30 Max.	Units
t_{RC}	Read cycle time	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1TTL gate V_{OH} = 2.2V V_{OL} = 0.65V V_{IH} = 2.2V V_{IL} = 0.65	200		300		ns
t_{AA}	Address access time			200		300	ns
t_{CO}	$\overline{CS}$ access time			200		300	ns
t_{OH}	Output data hold time		50		50		ns
t_{LZ}	$\overline{CS}$ enable time		10		10		ns
t_{HZ}	$\overline{CS}$ disable time		10	100	10	100	ns

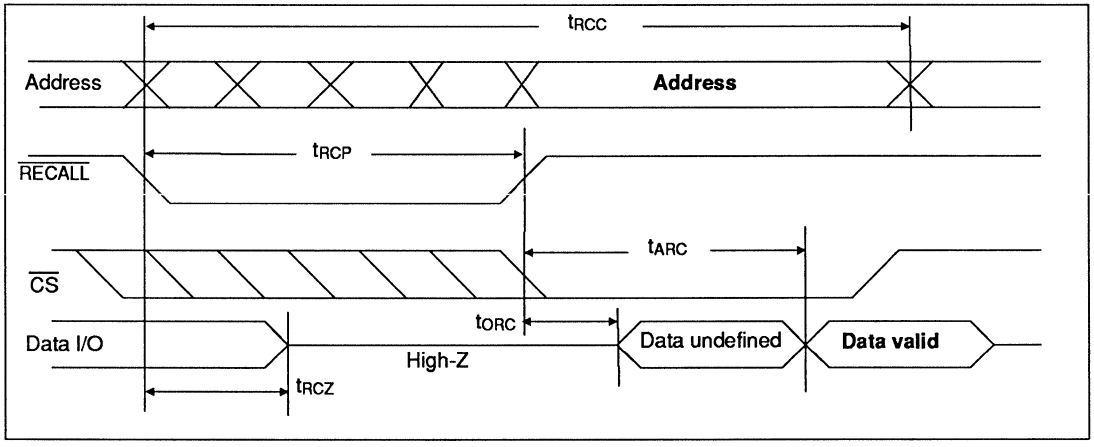
AC CHARACTERISTICS <Store Cycle>

Symbol	Parameter	Conditions	Min	Max	Units
t_{STC}	Store time	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1TTL gate V_{OH} = 2.2V, V_{OL} = 0.65V V_{IH} = 2.2V, V_{IL} = 0.65V		10	ms
t_{STP}	Store pulse width		200		ns
t_{STZ}	Store disable time			100	ns
t_{OST}	Store enable time		10		ns



AC CHARACTERISTICS <Recall Cycle>

Symbol	Parameter	Conditions	Min	Max	Units
t_{RCC}	Recall cycle time	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1TTL gate V_{OH} = 2.2V, V_{OL} = 0.65V V_{IH} = 2.2V, V_{IL} = 0.65V	1400		ns
t_{RCP}	Recall pulse width		300		ns
t_{RCZ}	Recall disable time			100	ns
t_{ORC}	Recall enable time		10		ns
t_{ARC}	Recall data access time			1100	ns



DEVICE OPERATION

The configuration of the CAT22C10 allows a common address bus to be directly connected to the address inputs, and the Input/Output (I/O) pins to be connected directly to a common I/O bus if it has less than 1 TTL load and 100pF capacitance. If not, the I/O path should be buffered.

When the chip select ($\overline{CS}$) goes low, the chip is activated. When $\overline{CS}$ is forced high, the chip goes into the standby mode and consumes very little current. With the nonvolatile functions inhibited, the device operates like a Static RAM. The Write Enable ($\overline{WE}$) selects a write operation when $\overline{WE}$ is low and a read operation when $\overline{WE}$ is high. In either of these modes, an array byte (4 bits) can be addressed uniquely by using the address lines (A_0 - A_5), and that byte will be read or written to through the Input/Output pins (I/O_0 - I/O_3).

The nonvolatile functions are inhibited by holding the $\overline{STORE}$ input and the $\overline{RECALL}$ high. When the $\overline{RECALL}$ input is taken low, it initiates a recall operation which transfers the contents of the entire E^2PROM array into the Static RAM. When the $\overline{STORE}$ input is taken low, it initiates a store operation which transfers the entire Static RAM array contents into the E^2PROM array.

STANDBY MODE

The chip select ($\overline{CS}$) input controls all of the functions of the CAT22C10. When a high level is supplied to the $\overline{CS}$ pin, the chip goes into the standby mode. In the mode the chip consumes 99.9% less power and the outputs are put into a high impedance state. Because I_{CCS} is less than 100µA in standby mode, the designer has the flexibility to use this part in battery operated systems.

READ

When the chip is enabled ($\overline{CS}$ = low), the nonvolatile functions are inhibited ($\overline{STORE}$ = high and $\overline{RECALL}$ = high). The Write Enable ($\overline{WE}$) can put the chip into the read mode when it is held high. In this mode, the data in the Static RAM array may be accessed by selecting an address on the input pins A_0 - A_5. This will occur when the outputs are connected to a bus which is loaded by no more than 100pF and 1 TTL gate. If the loading is greater than this, some additional buffering circuitry is recommended.

WRITE

Like the read mode, with the chip enabled and the nonvolatile functions inhibited, the Write Enable ($\overline{WE}$) will select the write mode when taken to a low level. In this mode, the address must be supplied for the byte to be written to. After the set-up time (t_{AS}), the input data must be supplied to pins I/O_0 - I/O_3. When these conditions, including the write pulse width time (t_{WP}) are met, the data will be written to the specified location in the static RAM. A write function may also be initiated from the standby mode by setting $\overline{WE}$ = low, inhibiting the nonvolatile functions, supplying valid addresses, and then taking $\overline{CS}$ low and supplying input data.

RECALL

At anytime, except during a store, taking the $\overline{RECALL}$ pin low will initiate a recall operation. This is independent of the state of $\overline{CS}$, $\overline{WE}$, or A_0-A_5. After the $\overline{RECALL}$ pin has been held low for the duration of the Recall Pulse Width (t_{RCP}), the recall will continue independent of any other inputs. During the recall, the entire content of the E^2PROM array is transferred to the Static RAM array. The first byte of data may be externally accessed after the recalled data access time from end of recall (t_{ARC}). After this, any other bytes may be accessed by using the normal read mode.

If $\overline{RECALL}$ is held low for the entire Recall Cycle time (t_{RCC}), the contents of the Static RAM may be immediately accessed by using the normal read mode. A recall operation can be performed an unlimited number of times without affecting the integrity of the data. A recall operation is automatically performed upon power-up (low to high transition) of V_{CC}.

The outputs I/O0-I/O3 will go into the high impedance state as long as the RECALL signal is held low.

STORE

At any time, except during a recall operation, taking the $\overline{\text{STORE}}$ pin low will initiate a store operation. This takes place independent of the state of $\overline{\text{CS}}$, $\overline{\text{WE}}$ or A_0-A_5. The $\overline{\text{STORE}}$ pin must be held low for the duration of the Store Pulse Width (t_{STP}) to ensure that a store operation is initiated. Once initiated, the $\overline{\text{STORE}}$ pin may be left low or taken high and the store operations will complete its transfer of the entire contents of the Static RAM array into the E^2PROM array within the Store Cycle time (t_{STC}). However, if a store operation is initiated during the write mode, the contents of the addressed Static RAM byte and its corresponding byte in the E^2PROM array will be unknown.

During the store operation, the outputs are in a high impedance state. At least 10,000 store operations can be performed reliably. The data which is written into the E^2PROM array during a store operation has a data retention time greater than 10 years.

DATA PROTECTION DURING POWER-UP AND POWER-DOWN

The CAT22C10 has on-chip circuitry which will prevent a store operation from occurring when V_{CC} falls below 3.5V. This function eliminates the potential hazard of a spurious signal from initiating a store operation when the system power is below 3.5V.

CAT22C10 I - Industrial Temperature
256-BIT (64x4) NONVOLATILE CMOS STATIC RAM

DESCRIPTION

The Catalyst CAT22C10I Nonvolatile Random Access Memory (NVRAM) is a 256-bit device with a 64x4 organization. It features fully static CMOS circuitry for very low power consumption. The active current is 40mA and the standby current is 30µA.

An internal E^2PROM array provides bit-by-bit back-up for the static RAM array. Store operations write data from the RAM array to the E^2PROM array. Recall operations write data from the E^2PROM array to the RAM array.

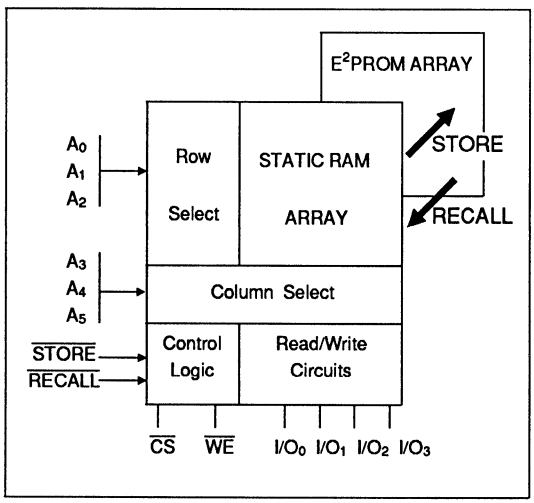
Data retention for each store cycle is specified for over 10 years, and over 10,000 store operations can be performed reliably. Unlimited recall operations, and read and write operations to the RAM are further specified.

The CAT22C10I has internal false store protection circuitry, which prohibits any store operation for V_{CC} less than 3.5V (typically) to ensure the integrity of the E^2PROM data. Other internal circuitry performs an automatic recall operation upon V_{CC} power-up.

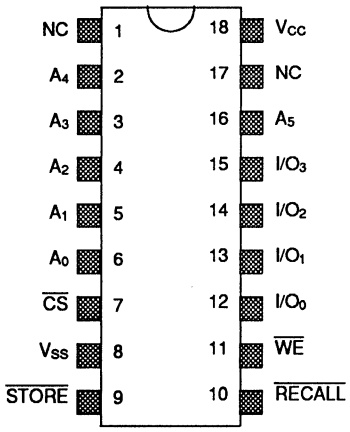
FEATURES

- CMOS technology - completely static operation
- Low current consumption
  - Active: 40mA max
  - Standby: 30µA max
- Single power supply (+5V ±10%)
- RAM access time 200ns, and 300ns
- Fully TTL and CMOS compatible
- JEDEC standard 18-pin 300-mil package
- Write protect circuit to preserve data on power-up and power-down
- Automatic recall on power-up
- 3-state output
- Short store pulse: 200ns
- Short recall pulse: 300ns
- False store protection below 3.5V operation level
- 10,000 nonvolatile store cycles per bit

BLOCK DIAGRAM



PIN CONFIGURATION



TOP VIEW

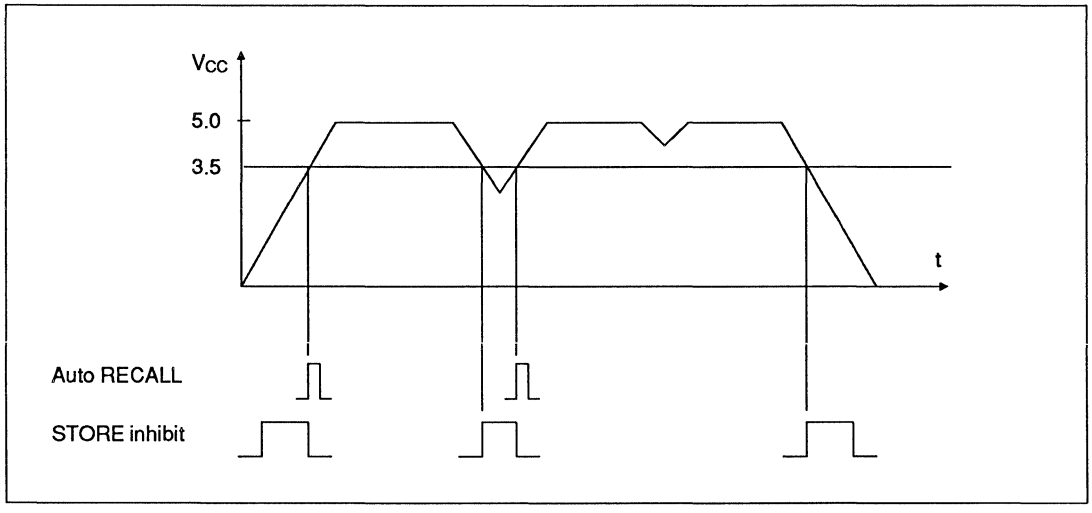
A_0-A_5	Address	STORE	Store
I/O_0-I/O_3	Data in/out	V_{CC}	+5V
WE	Write enable	V_{SS}	Ground
CS	Chip select	NC	No connect
RECALL	Recall		

MODES OF OPERATION

Input				Input/Output	Mode
$\overline{CS}$	$\overline{WE}$	$\overline{RECALL}$	$\overline{STORE}$		
H	-	H	H	Output high impedance	Standby
L	H	H	H	Output data	RAM Read
L	L	H	H	Input data	RAM Write
-	H	L	H	Output high impedence RECALL	($E^2PROM \rightarrow RAM$)
H	-	L	H	Output high impedence RECALL	($E^2PROM \rightarrow RAM$)
-	H	H	L	Output high impedence STORE	($RAM \rightarrow E^2PROM$)
H	-	H	L	Output high impedence STORE	($RAM \rightarrow E^2PROM$)

NOTES:

- $\overline{RECALL}$ signal has priority over $\overline{STORE}$ signal when both are applied at the same time
- $\overline{STORE}$ is inhibited when $\overline{RECALL}$ is active
- The auto recall is activated on power-up when V_{CC} reaches ≈3.5V
- The store operation is inhibited when V_{CC} is below ≈3.5V
- V_{CC} rise and fall time should be between 10ms and 1000ms



MAXIMUM RATINGS *

Storage temperature	-65°C to +150°C
Temperature under bias	-40°C to +85°C
Power supply (V_{CC})	-0.3 to +6V
Input voltage	-0.3 to +6V
Output voltage	0.0 to +6V
Output current	5mA
Lead temperature (soldering for 10 seconds)	260°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, CAT22C10I T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Limits Min.	Typ.	Max.	Unit
I_{CCO}	Current consumption (operating)	All input = 5.5V T_A = 0°C All outputs unloaded		15	40	mA
I_{CCS}	Current consumption (standby)				30	µA
I_{LI}	Input current	$0 \le V_{IN} \le 5.5V$		0.1	10	µA
I_{LO}	Output leakage current	$0 \le V_{OUT} \le 5.5V$		0.1	10	µA
V_{IH}	High level input voltage		2.0		V_{CC}	V
V_{IL}	Low level input voltage		0.0		0.8	V
V_{OH}	High level output voltage	I_{OH} = -2mA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 4.2mA			0.4	V
V_{DH}	RAM data holding voltage	V_{CC}	1.5		5.5	V

CAPACITANCE

(T_A= 25°C, f = 1.0 MHz, V_{CC} = 5V)

Symbol	Parameter	Conditions	Limits Typ. max.	Unit
$C_{I/O}$	Input/Output capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input capacitance	V_{IN} = 0V	6	pF

Note: These parameters are periodically sampled and are not 100% tested.

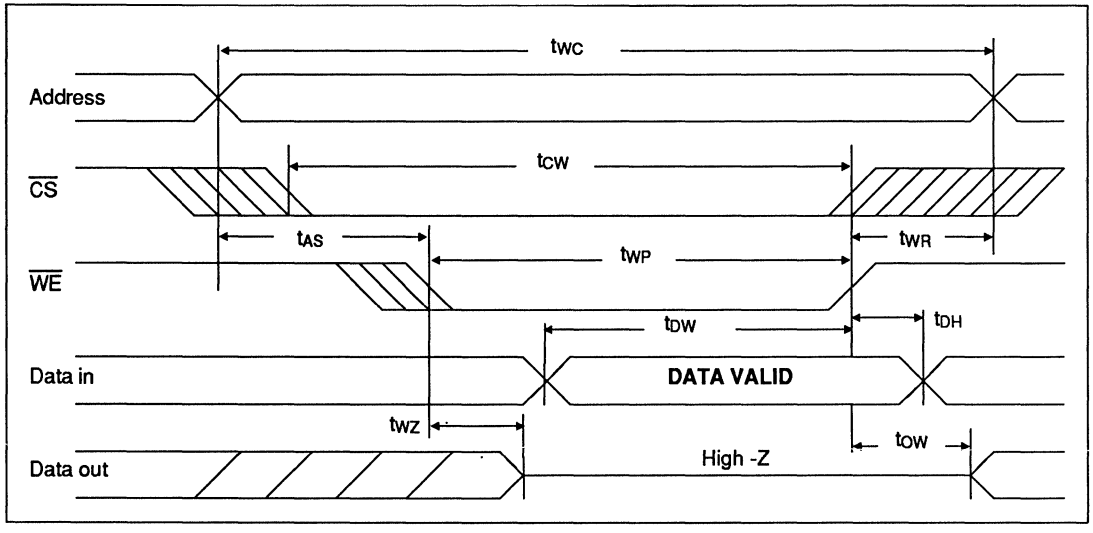
AC CHARACTERISTICS < Write Cycle>

(CAT22C10I T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	22C10I-20 Min.	22C10I-20 Max.	22C10I-30 Min.	22C10I-30 Max.	Units
t_{WC}	Write cycle time	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1 TTL gate V_{OH} = 2.2V V_{OL} = 0.65V V_{IH} = 2.2V V_{IL} = 0.65	200		300		ns
t_{CW}	$\overline{CS}$ write pulse width		150		150		ns
t_{AS}	Address set-up time		50		50		ns
t_{WP}	Write pulse width		150		150		ns
t_{WR}	Write recovery time		25		25		ns
t_{DW}	Data valid time		100		100		ns
t_{DH}	Data hold time		20		20		ns
t_{WZ}	Output disable time		10	100	10	100	ns
t_{OW}	Output enable time		10		10		ns

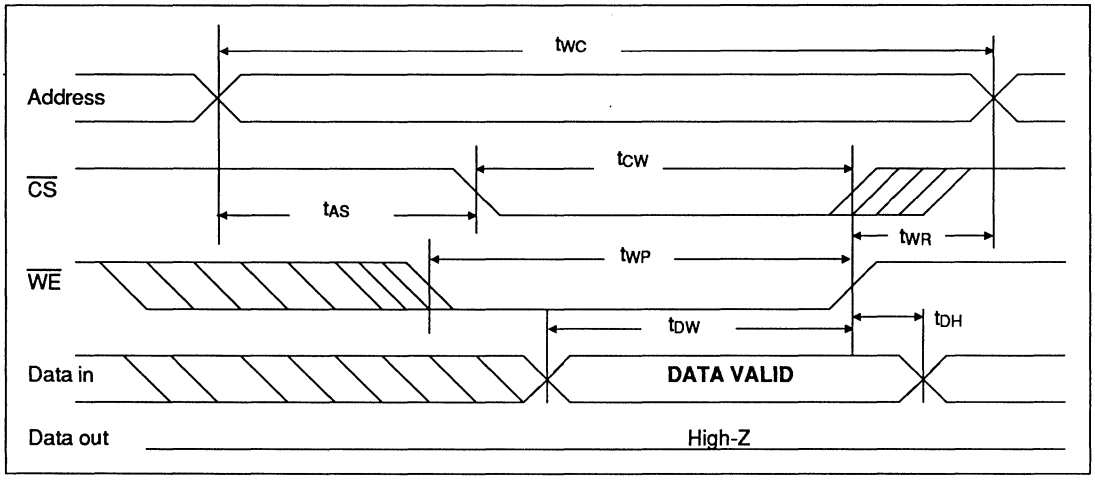
AC CHARACTERISTICS <Write Cycle>

(CAT22C10I T_A = -40°C to +85°C)



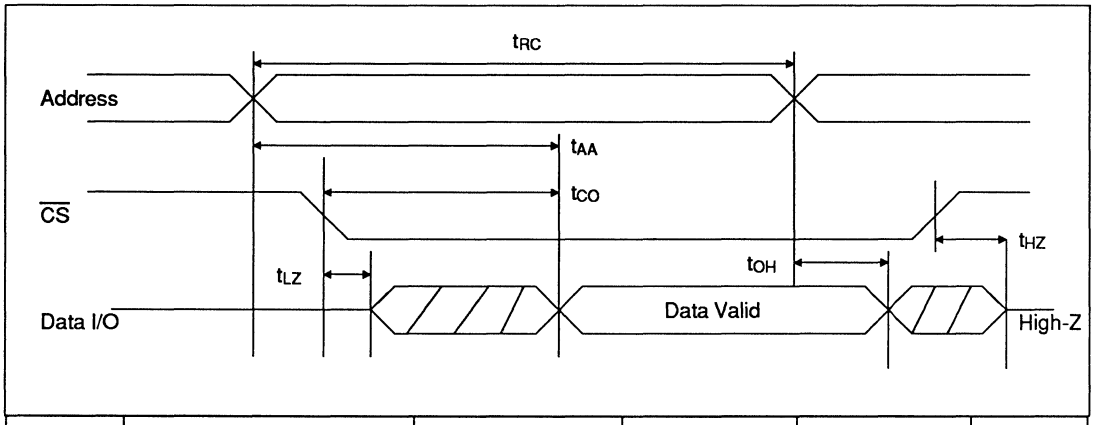
AC CHARACTERISTICS <Early Write Cycle>

(CAT22C10I T_A = -40°C to +85°C)



AC CHARACTERISTICS <Read Cycle>

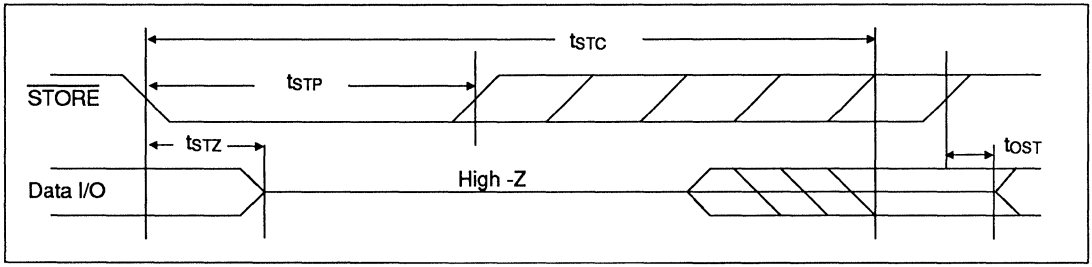
(CAT22C10I T_A = -40°C to +85°C)



Symbol	Parameter	Conditions	22C10I-20 Min.	22C10I-20 Max.	22C10I-30 Min.	22C10I-30 Max.	Units
t_{RC}	Read cycle time	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1TTL gate V_{OH} = 2.2V V_{OL} = 0.65V V_{IH} = 2.2V V_{IL} = 0.65	200		300		ns
t_{AA}	Address access time			200		300	ns
t_{CO}	$\overline{CS}$ access time			200		300	ns
t_{OH}	Output data hold time		50		50		ns
t_{LZ}	$\overline{CS}$ enable time		10		10		ns
t_{HZ}	$\overline{CS}$ disable time		10	100	10	100	ns

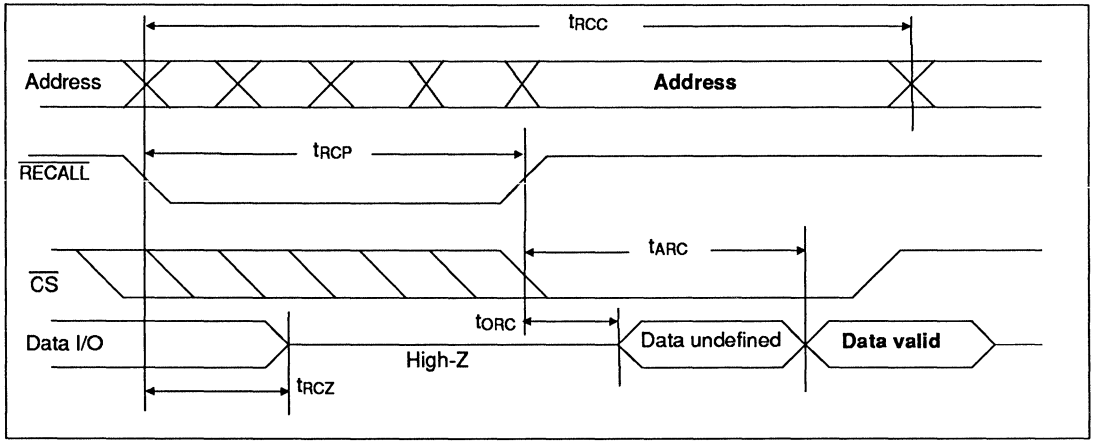
AC CHARACTERISTICS <Store Cycle>

Symbol	Parameter	Conditions	Min	Max	Units
t_{STC}	Store time	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1TTL gate V_{OH} = 2.2V, V_{OL} = 0.65V V_{IH} = 2.2V, V_{IL} = 0.65V		10	ms
t_{STP}	Store pulse width		200		ns
t_{STZ}	Store disable time			100	ns
t_{OST}	Store enable time		10		ns



AC CHARACTERISTICS <Recall Cycle>

Symbol	Parameter	Conditions	Min	Max	Units
t_{RCC}	Recall cycle time	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1TTL gate V_{OH} = 2.2V, V_{OL} = 0.65V V_{IH} = 2.2V, V_{IL} = 0.65V	1400		ns
t_{RCP}	Recall pulse width		300		ns
t_{RCZ}	Recall disable time			100	ns
t_{ORC}	Recall enable time		10		ns
t_{ARC}	Recall data access time			1100	ns



DEVICE OPERATION

The configuration of the CAT22C10I allows a common address bus to be directly connected to the address inputs, and the Input/Output (I/O) pins to be connected directly to a common I/O bus if it has less than 1 TTL load and 100pF capacitance. If not, the I/O path should be buffered.

When the chip select ($\overline{CS}$) goes low, the chip is activated. When $\overline{CS}$ is forced high, the chip goes into the standby mode and consumes very little current. With the nonvolatile functions inhibited, the device operates like a Static RAM. The Write Enable ($\overline{WE}$) selects a write operation when $\overline{WE}$ is low and a read operation when $\overline{WE}$ is high. In either of these modes, an array byte (4 bits) can be addressed uniquely by using the address lines (A_0 - A_5), and that byte will be read or written to through the Input/Output pins (I/O_0 - I/O_3).

The nonvolatile functions are inhibited by holding the $\overline{STORE}$ input and the $\overline{RECALL}$ high. When the $\overline{RECALL}$ input is taken low, it initiates a recall operation which transfers the contents of the entire E^2PROM array into the Static RAM. When the $\overline{STORE}$ input is taken low, it initiates a store operation which transfers the entire Static RAM array contents into the E^2PROM array.

STANDBY MODE

The chip select ($\overline{CS}$) input controls all of the functions of the CAT22C10I. When a high level is supplied to the $\overline{CS}$ pin, the chip goes into the standby mode. In the mode the chip consumes 99.9% less power and the outputs are put into a high impedance state. Because I_{CCS} is less than 100µA in standby mode, the designer has the flexibility to use this part in battery operated systems.

READ

When the chip is enabled ($\overline{CS}$ = low), the nonvolatile functions are inhibited ($\overline{STORE}$ = high and $\overline{RECALL}$ = high). The Write Enable ($\overline{WE}$) can put the chip into the read mode when it is held high. In this mode, the data in the Static RAM array may be accessed by selecting an address on the input pins A_0 - A_5. This will occur when the outputs are connected to a bus which is loaded by no more than 100pF and 1 TTL gate. If the loading is greater than this, some additional buffering circuitry is recommended.

WRITE

Like the read mode, with the chip enabled and the nonvolatile functions inhibited, the Write Enable ($\overline{WE}$) will select the write mode when taken to a low level. In this mode, the address must be supplied for the byte to be written to. After the set-up time (t_{AS}), the input data must be supplied to pins I/O_0 - I/O_3. When these conditions, including the write pulse width time (t_{WP}) are met, the data will be written to the specified location in the static RAM. A write function may also be initiated from the standby mode by setting $\overline{WE}$ = low, inhibiting the nonvolatile functions, supplying valid addresses, and then taking $\overline{CS}$ low and supplying input data.

RECALL

At anytime, except during a store, taking the $\overline{RECALL}$ pin low will initiate a recall operation. This is independent of the state of $\overline{CS}$, $\overline{WE}$, or A_0-A_5. After the $\overline{RECALL}$ pin has been held low for the duration of the Recall Pulse Width (t_{RCP}), the recall will continue independent of any other inputs. During the recall, the entire content of the E^2PROM array is transferred to the Static RAM array. The first byte of data may be externally accessed after the recalled data access time from end of recall (t_{ARC}). After this, any other bytes may be accessed by using the normal read mode.

If $\overline{RECALL}$ is held low for the entire Recall Cycle time (t_{RCC}), the contents of the Static RAM may be immediately accessed by using the normal read mode. A recall operation can be performed an unlimited number of times without affecting the integrity of the data. A recall operation is automatically performed upon power-up (low to high transition) of V_{CC}.

The outputs I/O0-I/O3 will go into the high impedance state as long as the RECALL signal is held low.

STORE

At any time, except during a recall operation, taking the $\overline{\text{STORE}}$ pin low will initiate a store operation. This takes place independent of the state of $\overline{\text{CS}}$, $\overline{\text{WE}}$ or A_0-A_5. The $\overline{\text{STORE}}$ pin must be held low for the duration of the Store Pulse Width (t_{STP}) to ensure that a store operation is initiated. Once initiated, the $\overline{\text{STORE}}$ pin may be left low or taken high and the store operations will complete its transfer of the entire contents of the Static RAM array into the E^2PROM array within the Store Cycle time (t_{STC}). However, if a store operation is initiated during the write mode, the contents of the addressed Static RAM byte and its corresponding byte in the E^2PROM array will be unknown.

During the store operation, the outputs are in a high impedance state. At least 10,000 store operations can be performed reliably. The data which is written into the E^2PROM array during a store operation has a data retention time greater than 10 years.

DATA PROTECTION DURING POWER-UP AND POWER-DOWN

The CAT22C10I has on-chip circuitry which will prevent a store operation from occurring when V_{CC} falls below 3.5V. This function eliminates the potential hazard of a spurious signal from initiating a store operation when the system power is below 3.5V.

CAT22C12
1024-BIT (256x4) NONVOLATILE CMOS STATIC RAM

DESCRIPTION

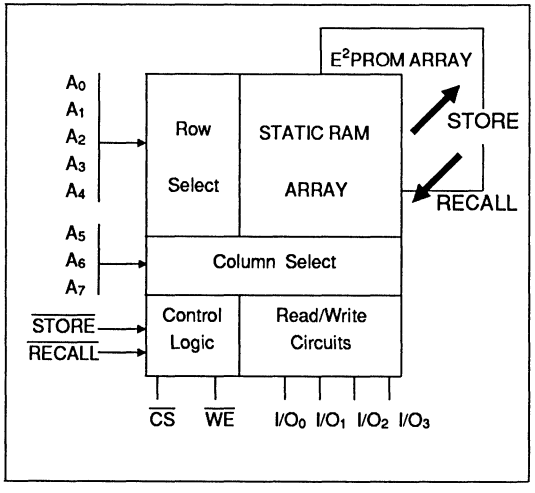
The Catalyst CAT22C12 Nonvolatile Random Access Memory (NVRAM) is a 1024-bit device with a 256x4 organization. It features fully static CMOS circuitry for very low power consumption. The active current is 50mA. and the standby current is 30µA.

An internal E^2PROM array provides bit-by-bit back-up for the static RAM array. Store operations write data from the RAM array to the E^2PROM array. Recall operations write data from the E^2PROM array to the RAM array.

Data retention for each store cycle is specified for over 10 years, and over 10,000 store operations can be performed reliably. Unlimited recall operations, and read and write operations to the RAM are further specified.

The CAT22C12 has internal false store protection circuitry, which prohibits any store operation for V_{CC} less than 3.5V (typically) to ensure the integrity of the E^2PROM data. Other internal circuitry performs an automatic recall operation upon V_{CC} power-up.

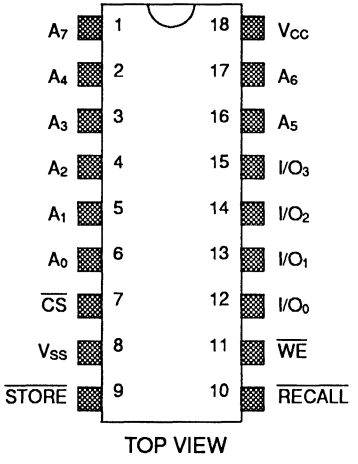
BLOCK DIAGRAM



FEATURES

- CMOS technology - completely static operation
- Low current consumption
  - Active: 50mA max
  - Standby: 30µA max
- Single power supply (+5V ±10%)
- RAM access time 200ns and 300ns
- Fully TTL and CMOS compatible
- JEDEC standard 18-pin 300-mil package
- Write protect circuit to preserve data on power-up and power-down
- Automatic recall on power-up
- 3-state output
- Short store pulse: 200ns
- Short recall pulse: 300ns
- False store protection below 3.5V operation level
- 10,000 nonvolatile store cycles per bit

PIN CONFIGURATION



TOP VIEW

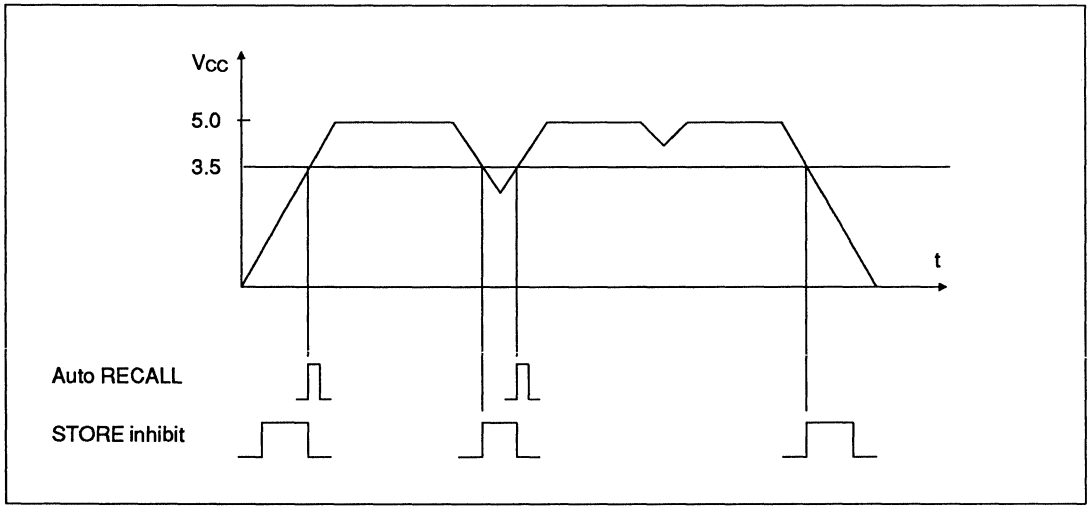
A_0-A_7	Address in	$\overline{STORE}$	Store
I/O_0-I/O_3	Data in/out	V_{CC}	+5V
$\overline{WE}$	Write enable	V_{SS}	Ground
$\overline{CS}$	Chip select	NC	No connect
$\overline{RECALL}$	Recall		

MODES OF OPERATION

Input				Input/Output	Mode
$\overline{CS}$	$\overline{WE}$	$\overline{RECALL}$	$\overline{STORE}$		
H	-	H	H	Output high impedance	Standby
L	H	H	H	Output data	RAM Read
L	L	H	H	Input data	RAM Write
-	H	L	H	Output high impedence RECALL	($E^2PROM \rightarrow RAM$)
H	-	L	H	Output high impedence RECALL	($E^2PROM \rightarrow RAM$)
-	H	H	L	Output high impedence STORE	($RAM \rightarrow E^2PROM$)
H	-	H	L	Output high impedence STORE	($RAM \rightarrow E^2PROM$)

NOTES:

- $\overline{RECALL}$ signal has priority over $\overline{STORE}$ signal when both are applied at the same time
- $\overline{STORE}$ is inhibited when $\overline{RECALL}$ is active
- The auto recall is activated on power-up when V_{CC} reaches ≈3.5V
- The store operation is inhibited when V_{CC} is below ≈3.5V
- V_{CC} rise and fall time should be between 10ms and 1000ms



MAXIMUM RATINGS *

Storage temperature	-65°C to +150°C
Temperature under bias	-40°C to +85°C
Power supply (V_{CC})	-0.3 to +6V
Input voltage	-0.3 to +6V
Output voltage	0.0 to +6V
Output current	5mA
Lead temperature (soldering for 10 seconds)	260°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, CAT22C12 T_A = 0°C to +70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CCO}	Current consumption (operating)	All input = 5.5V, T_A =0°C All outputs unloaded		15	50	mA
I_{CCS}	Current consumption (standby)				30	µA
I_{LI}	Input current	$0 \le V_{IN} \le 5.5V$		0.1	10	µA
I_{LO}	Output leakage current	$0 \le V_{OUT} \le 5.5V$		0.1	10	µA
V_{IH}	High level input voltage		2.0		V_{CC}	V
V_{IL}	Low level input voltage		0.0		0.8	V
V_{OH}	High level output voltage	I_{OH} = -2mA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 4.2mA			0.4	V
V_{DH}	RAM data holding voltage	V_{CC}	1.5		5.5	V

CAPACITANCE

T_A = 25°C, f = 1.0MHz, V_{CC} = 5V)

Symbol	Parameter	Conditions	Limits Typ. max.	Unit
$C_{I/O}$	Input/Output capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input capacitance	V_{IN} = 0V	6	pF

Note: These parameters are periodically sampled and are not 100% tested.

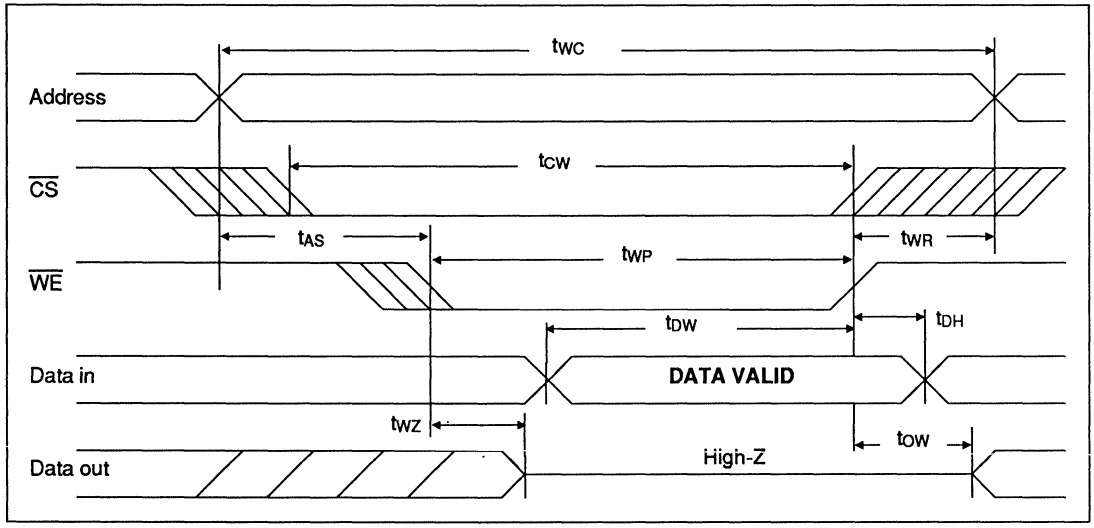
AC CHARACTERISTICS <Write Cycle>

(CAT22C12 T_A = 0°C to +70°C)

Symbol	Parameter	Conditions	22C12-20 Min.	22C12-20 Max.	22C12-30 Min.	22C12-30 Max.	Units
t_{WC}	Write cycle time	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1TTL gate V_{OH} = 2.2V V_{OL} = 0.65V V_{IH} = 2.2V V_{IL} = 0.65	200		300		ns
t_{CW}	CS write pulse width		150		150		ns
t_{AS}	Address set-up time		50		50		ns
t_{WP}	Write pulse width		150		150		ns
t_{WR}	Write recovery time		25		25		ns
t_{DW}	Data valid time		100		100		ns
t_{DH}	Data hold time		20		20		ns
t_{WZ}	Output disable time		10	100	10	100	ns
t_{OW}	Output enable time		10		10		ns

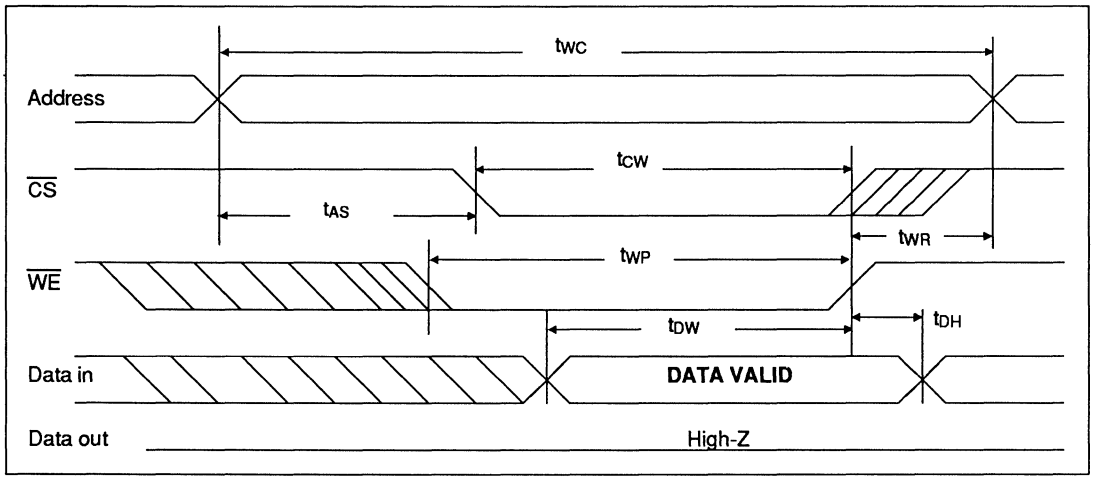
AC CHARACTERISTICS <Write Cycle>

(CAT22C12 T_A = 0°C to +70°C)



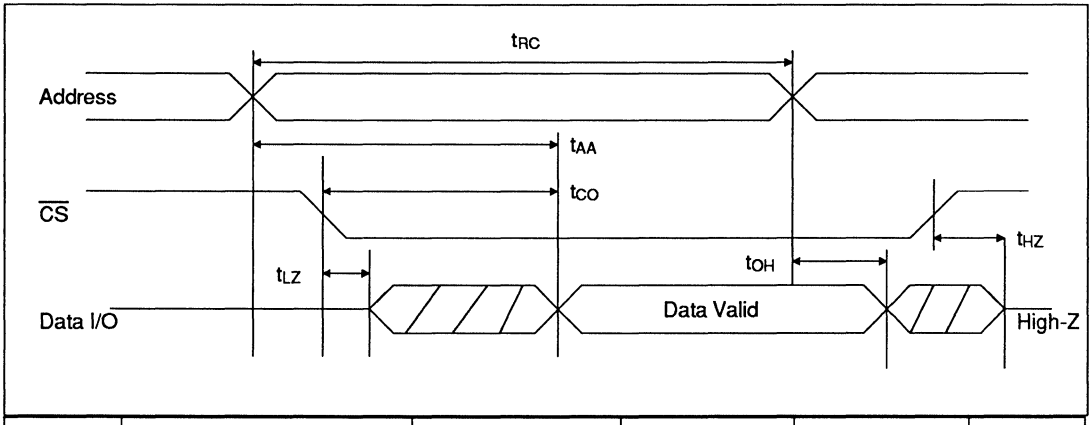
AC CHARACTERISTICS <Early Write Cycle>

(CAT22C12 T_A = 0°C to +70°C)



AC CHARACTERISTICS <Read Cycle>

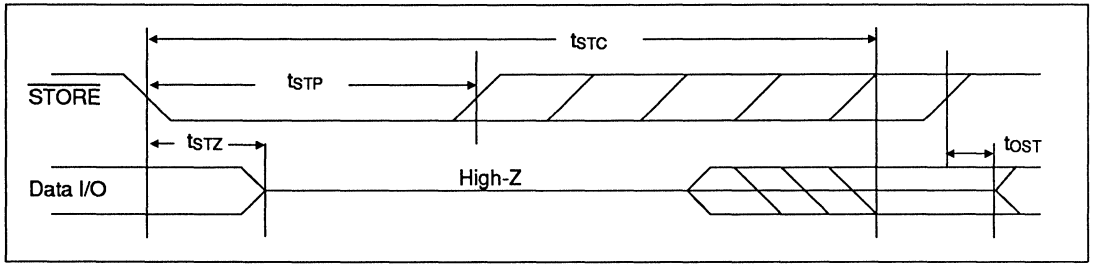
(CAT22C12 T_A = 0°C to +70°C)



Symbol	Parameter	Conditions	22C12-20 Min.	22C12-20 Max.	22C12-30 Min.	22C12-30 Max.	Units
t_{RC}	Read cycle time	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1TTL gate V_{OH} = 2.2V V_{OL} = 0.65V V_{IH} = 2.2V V_{IL} = 0.65	200		300		ns
t_{AA}	Address access time			200		300	ns
t_{CO}	$\overline{CS}$ access time			200		300	ns
t_{OH}	Output data hold time		50		50		ns
t_{LZ}	$\overline{CS}$ enable time		10		10		ns
t_{HZ}	$\overline{CS}$ disable time		10	100	10	100	ns

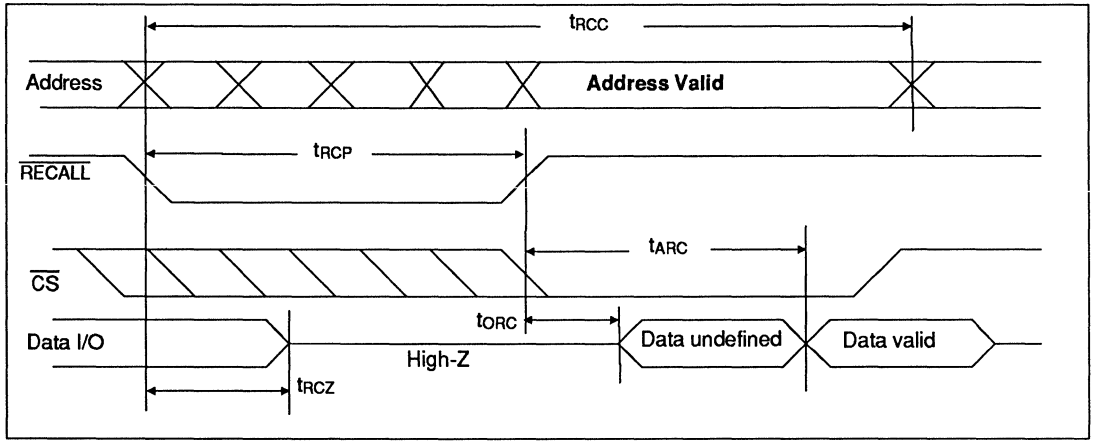
AC CHARACTERISTICS <Store Cycle>

Symbol	Parameter	Conditions	Min	Max	Units
t_{STC}	Store time	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1TTL gate V_{OH} = 2.2V, V_{OL} = 0.65V V_{IH} = 2.2V, V_{IL} = 0.65V		10	ms
t_{STP}	Store pulse width		200		ns
t_{STZ}	Store disable time			100	ns
t_{OST}	Store enable time		10		ns



AC CHARACTERISTICS <Recall Cycle>

Symbol	Parameter	Conditions	Min	Max	Units
t_{RCC}	Recall cycle time	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1TTL gate V_{OH} = 2.2V, V_{OL} = 0.65V V_{IH} = 2.2V, V_{IL} = 0.65V	1400		ns
t_{RCP}	Recall pulse width		300		ns
t_{RCZ}	Recall disable time			100	ns
t_{ORC}	Recall enable time		10		ns
t_{ARC}	Recall data access time			1100	ns



DEVICE OPERATION

The configuration of the CAT22C12 allows a common address bus to be directly connected to the address inputs, and the Input/Output (I/O) pins to be connected directly to a common I/O bus if it has less than 1 TTL load and 100pF capacitance. If not, the I/O path should be buffered.

When the chip select ($\overline{CS}$) goes low, the chip is activated. When $\overline{CS}$ is forced high, the chip goes into the standby mode and consumes very little current. With the nonvolatile functions inhibited, the device operates like a Static RAM. The Write Enable ($\overline{WE}$) selects a write operation when $\overline{WE}$ is low and a read operation when $\overline{WE}$ is high. In either of these modes, an array byte (4 bits) can be addressed uniquely by using the address lines (A_0 - A_7), and that byte will be read from or written to through the Input/Output pins (I/O_0 - I/O_3).

The nonvolatile functions are inhibited by holding the $\overline{STORE}$ and the $\overline{RECALL}$ high. When the $\overline{RECALL}$ input is taken low, it initiates a recall operation which transfers the contents of the entire E^2PROM array into the Static RAM. When the $\overline{STORE}$ input is taken low, it initiates a store operation which transfers the entire Static RAM array contents into the E^2PROM array.

STANDBY MODE

The chip select ($\overline{CS}$) input controls all of the functions of the CAT22C12. When a high level is supplied to the $\overline{CS}$ pin, the chip goes into the standby mode. In the mode the chip consumes 99.9% less power and the outputs are put into a high impedance state. Because I_{CCS} is less than 100µA in standby mode, the designer has the flexibility to use this part in battery operated systems.

READ

When the chip is enabled ($\overline{CS}$ = low), the nonvolatile functions are inhibited ($\overline{STORE}$ = high and $\overline{RECALL}$ = high). The Write Enable ($\overline{WE}$) can put the chip into the read mode when it is held high. In this mode, the data in the Static RAM array may be accessed by selecting an address on the input pins A_0 - A_7. This will occur when the outputs are connected to a bus which is loaded by no more than 100pF and 1 TTL gate. If the loading is greater than this, some additional buffering circuitry is recommended.

WRITE

Like the read mode, with the chip enabled and the nonvolatile functions inhibited, the Write Enable ($\overline{WE}$) will select the write mode when taken to a low level. In this mode, the address must be supplied for the byte to be written to. After the set-up time (t_{AS}), the input data must be supplied to pins I/O_0 - I/O_3. When these conditions, including the write pulse width time (t_{WP}), are met, the data will be written to the specified location in the static RAM. A write function may also be initiated from the standby mode by setting $\overline{WE}$ = low, inhibiting the nonvolatile functions, supplying valid addresses, and then taking $\overline{CS}$ low and supplying input data.

RECALL

At anytime, except during a store, taking the $\overline{RECALL}$ pin low will initiate a recall operation. This is independent of the state of $\overline{CS}$, $\overline{WE}$, or A_0-A_7. After the $\overline{RECALL}$ pin has been held low for the duration of the Recall Pulse Width (t_{RCP}), the recall will continue independent of any other inputs. During the recall, the entire content of the EEPROM array is transferred to the Static RAM array. The first byte of data may be externally accessed after the recalled data access time from End of Recall (t_{ARC}). After this, any other bytes may be accessed by using the normal read mode.

If $\overline{RECALL}$ is held low for the entire Recall Cycle time (t_{RCC}), the contents of the Static RAM may be immediately accessed by using the normal read mode. A recall operation can be performed an unlimited number of times without affecting the integrity of the data. A recall operation is automatically performed upon power-up (low to high transition) of V_{CC}.

The outputs I/O_0-I/O_3 will go into the high impedance state as long as the $\overline{RECALL}$ signal is held low.

STORE

At any time, except during a recall operation, taking the $\overline{\text{STORE}}$ pin low will initiate a store operation. This takes place independent of the state of $\overline{\text{CS}}$, $\overline{\text{WE}}$ or A_0-A_7. The $\overline{\text{STORE}}$ pin must be held low for the duration of the Store Pulse Width (t_{STP}) to ensure that a store operation is initiated. Once initiated, the $\overline{\text{STORE}}$ pin may be left low or taken high and the store operations will complete its transfer of the entire contents of the Static RAM array into the E^2PROM array within the Store Cycle time (t_{STC}). However, if a store operation is initiated during the write mode, the contents of the addressed Static RAM byte and its corresponding byte in the E^2PROM array will be unknown.

During the store operation, the outputs are in a high impedance state. At least 10,000 store operations can be performed reliably. The data which is written into the E^2PROM array during a store operation has a data retention time greater than 10 years.

DATA PROTECTION DURING POWER-UP AND POWER-DOWN

The CAT22C12 has on-chip circuitry which will prevent a store operation from occurring when V_{CC} falls below 3.5V. This function eliminates the potential hazard of a spurious signal from initiating a store operation when the system power supply is below 3.5V.

CAT22C12 I - Industrial Temperature
1024-BIT (256x4) NONVOLATILE CMOS STATIC RAM

DESCRIPTION

The Catalyst CAT22C12I Nonvolatile Random Access Memory (NVRAM) is a 1024-bit device with a 256x4 organization. It features fully static CMOS circuitry for very low power consumption. The active current is 50mA and the standby current is 30µA.

An internal E^2PROM array provides bit-by-bit back-up for the static RAM array. Store operations write data from the RAM array to the E^2PROM array. Recall operations write data from the E^2PROM array to the RAM array.

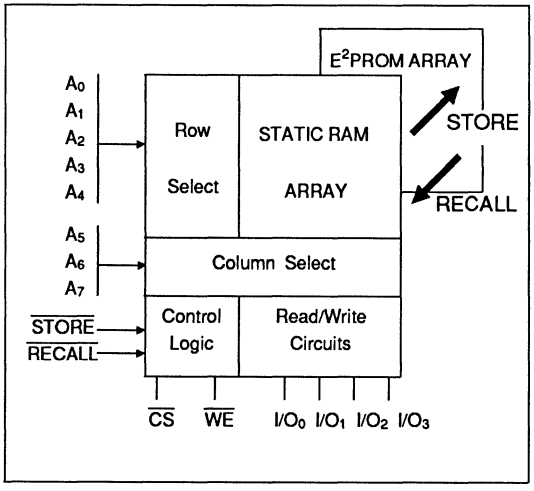
Data retention for each store cycle is specified for over 10 years, and over 10,000 store operations can be performed reliably. Unlimited recall operations, and read and write operations to the RAM are further specified.

The CAT22C12I has internal false store protection circuitry, which prohibits any store operation for V_{CC} less than 3.5V (typically) to ensure the integrity of the E^2PROM data. Other internal circuitry performs an automatic recall operation upon V_{CC} power-up.

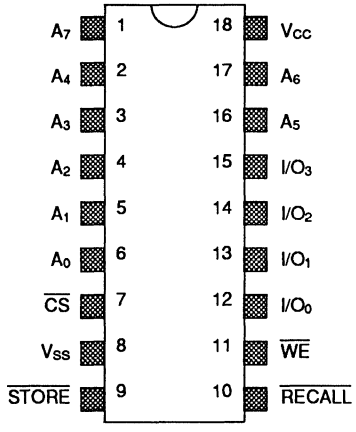
FEATURES

- CMOS technology - completely static operation
- Low current consumption
  - Active: 50mA max
  - Standby: 30µA max
- Single power supply (+5V ±10%)
- RAM access time 200ns and 300ns
- Fully TTL and CMOS compatible
- JEDEC standard 18-pin 300-mil package
- Write protect circuit to preserve data on power-up and power-down
- Automatic recall on power-up
- 3-state output
- Short store pulse: 200ns
- Short recall pulse: 300ns
- False store protection below 3.5V operation level
- 10,000 nonvolatile store cycles per bit

BLOCK DIAGRAM



PIN CONFIGURATION



TOP VIEW

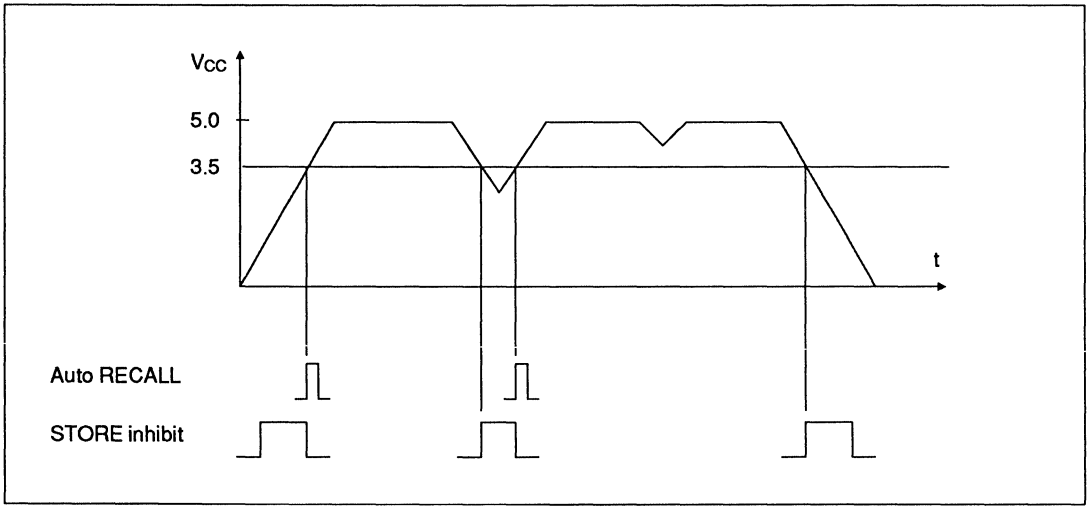
A_0-A_7	Address in	$\overline{STORE}$	Store
I/O_0-I/O_3	Data in/out	V_{CC}	+5V
$\overline{WE}$	Write enable	V_{SS}	Ground
$\overline{CS}$	Chip select	NC	No connect
$\overline{RECALL}$	Recall		

MODES OF OPERATION

Input				Input/Output	Mode
$\overline{CS}$	$\overline{WE}$	$\overline{RECALL}$	$\overline{STORE}$		
H	-	H	H	Output high impedance	Standby
L	H	H	H	Output data	RAM Read
L	L	H	H	Input data	RAM Write
-	H	L	H	Output high impedence RECALL	($E^2PROM \rightarrow RAM$)
H	-	L	H	Output high impedence RECALL	($E^2PROM \rightarrow RAM$)
-	H	H	L	Output high impedence STORE	($RAM \rightarrow E^2PROM$)
H	-	H	L	Output high impedence STORE	($RAM \rightarrow E^2PROM$)

NOTES:

- $\overline{RECALL}$ signal has priority over $\overline{STORE}$ signal when both are applied at the same time
- $\overline{STORE}$ is inhibited when $\overline{RECALL}$ is active
- The auto recall is activated on power-up when V_{CC} reaches ≈3.5V
- The store operation is inhibited when V_{CC} is below ≈3.5V
- V_{CC} rise and fall time should be between 10ms and 1000ms



MAXIMUM RATINGS *

Storage temperature	-65°C to +150°C
Temperature under bias	-40°C to +85°C
Power supply (V_{CC})	-0.3 to +6V
Input voltage	-0.3 to +6V
Output voltage	0.0 to +6V
Output current	5mA
Lead temperature (soldering for 10 seconds)	260°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, CAT22C12I T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Limits Min.	Typ.	Max.	Unit
I_{CCO}	Current consumption (operating)	All input = 5.5V, T_A = 0°C All outputs unloaded		15	50	mA
I_{CCS}	Current consumption (standby)				30	µA
I_{LI}	Input current	$0 \le V_{IN} \le 5.5V$		0.1	10	µA
I_{LO}	Output leakage current	$0 \le V_{OUT} \le 5.5V$		0.1	10	µA
V_{IH}	High level input voltage		2.0		V_{CC}	V
V_{IL}	Low level input voltage		0.0		0.8	V
V_{OH}	High level output voltage	I_{OH} = -2mA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 4.2mA			0.4	V
V_{DH}	RAM data holding voltage	V_{CC}	1.5		5.5	V

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V)

Symbol	Parameter	Conditions	Limits Typ. max.	Unit
$C_{I/O}$	Input/Output capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input capacitance	V_{IN} = 0V	6	pF

Note: These parameters are periodically sampled and are not 100% tested.

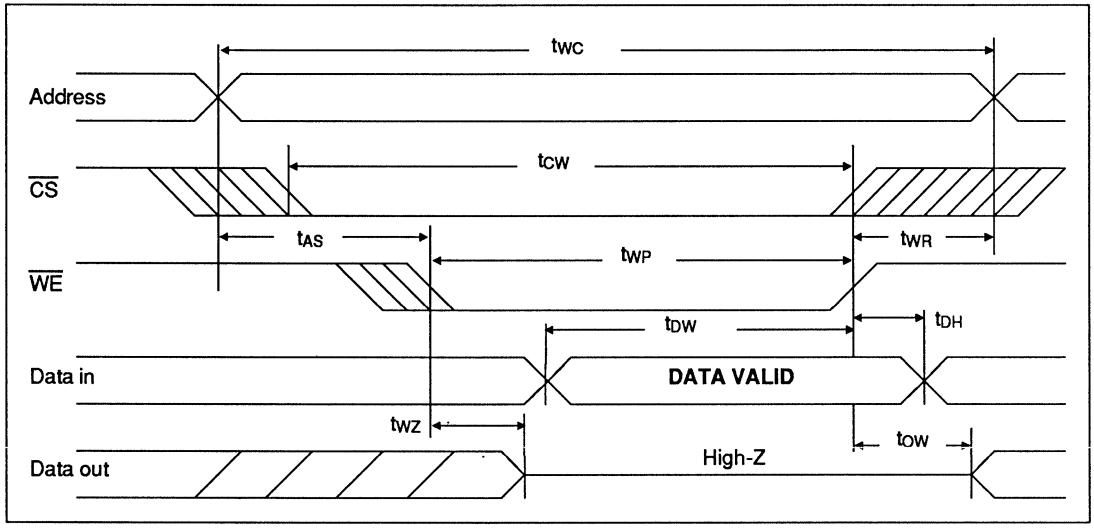
AC CHARACTERISTICS <Write Cycle>

(CAT22C12I T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	22C12I-20 Min.	22C12I-20 Max.	22C12I-30 Min.	22C12I-30 Max.	Units
t_{WC}	Write cycle time	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1TTL gate V_{OH} = 2.2V V_{OL} = 0.65V V_{IH} = 2.2V V_{IL} = 0.65	200		300		ns
t_{CW}	CS write pulse width		150		150		ns
t_{AS}	Address set-up time		50		50		ns
t_{WP}	Write pulse width		150		150		ns
t_{WR}	Write recovery time		25		25		ns
t_{DW}	Data valid time		100		100		ns
t_{DH}	Data hold time		20		20		ns
t_{WZ}	Output disable time		10	100	10	100	ns
t_{OW}	Output enable time		10		10		ns

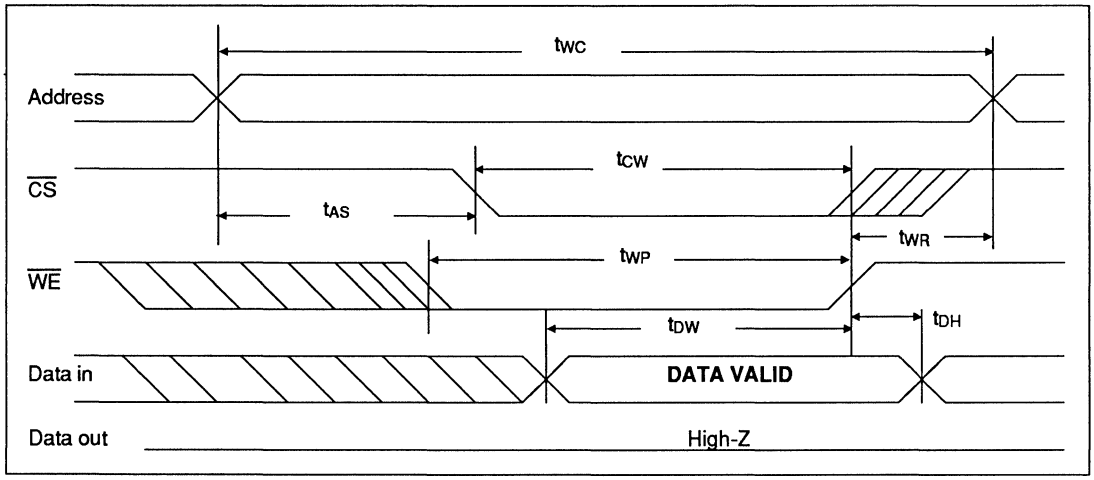
AC CHARACTERISTICS <Write Cycle>

(CAT22C12I T_A = -40°C to +85°C)



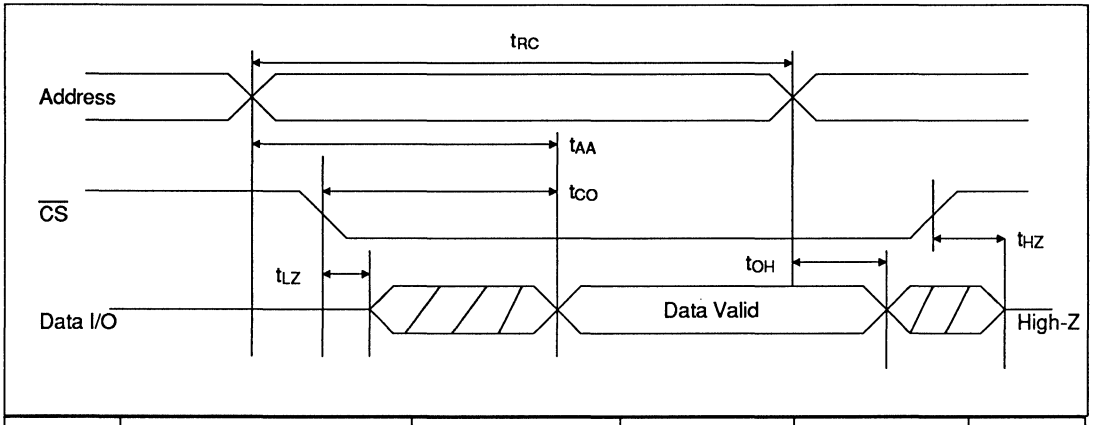
AC CHARACTERISTICS <Early Write Cycle>

(CAT22C12I T_A = -40°C to +85°C)



AC CHARACTERISTICS <Read Cycle>

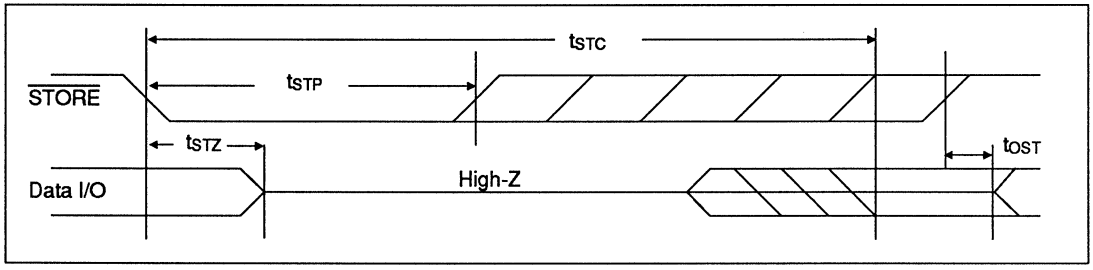
(CAT22C12I T_A = -40°C to +85°C)



Symbol	Parameter	Conditions	22C12I-20 Min.	22C12I-20 Max.	22C12I-30 Min.	22C12I-30 Max.	Units
t_{RC}	Read cycle time	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1TTL gate V_{OH} = 2.2V V_{OL} = 0.65V V_{IH} = 2.2V V_{IL} = 0.65	200		300		ns
t_{AA}	Address access time			200		300	ns
t_{CO}	$\overline{CS}$ access time			200		300	ns
t_{OH}	Output data hold time		50		50		ns
t_{LZ}	$\overline{CS}$ enable time		10		10		ns
t_{HZ}	$\overline{CS}$ disable time		10	100	10	100	ns

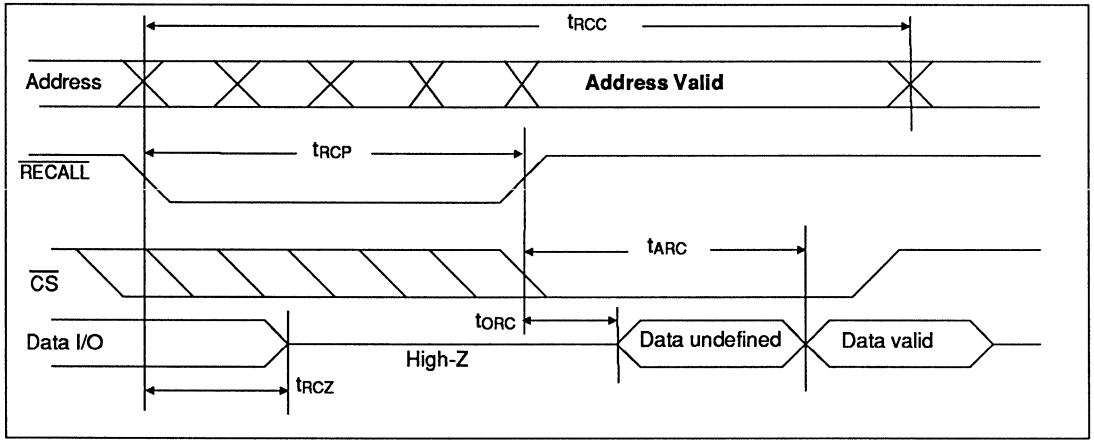
AC CHARACTERISTICS <Store Cycle>

Symbol	Parameter	Conditions	Min	Max	Units
t_{STC}	Store time	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1TTL gate V_{OH} = 2.2V, V_{OL} = 0.65V V_{IH} = 2.2V, V_{IL} = 0.65V		10	ms
t_{STP}	Store pulse width		200		ns
t_{STZ}	Store disable time			100	ns
t_{OST}	Store enable time		10		ns



AC CHARACTERISTICS <Recall Cycle>

Symbol	Parameter	Conditions	Min	Max	Units
t_{RCC}	Recall cycle time	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1TTL gate V_{OH} = 2.2V, V_{OL} = 0.65V V_{IH} = 2.2V, V_{IL} = 0.65V	1400		ns
t_{RCP}	Recall pulse width		300		ns
t_{RCZ}	Recall disable time			100	ns
t_{ORC}	Recall enable time		10		ns
t_{ARC}	Recall data access time			1100	ns



DEVICE OPERATION

The configuration of the CAT22C12I allows a common address bus to be directly connected to the address inputs, and the Input/Output (I/O) pins to be connected directly to a common I/O bus if it has less than 1 TTL load and 100pF capacitance. If not, the I/O path should be buffered.

When the chip select ($\overline{CS}$) goes low, the chip is activated. When $\overline{CS}$ is forced high, the chip goes into the standby mode and consumes very little current. With the nonvolatile functions inhibited, the device operates like a Static RAM. The Write Enable ($\overline{WE}$) selects a write operation when $\overline{WE}$ is low and a read operation when $\overline{WE}$ is high. In either of these modes, an array byte (4 bits) can be addressed uniquely by using the address lines (A_0 - A_7), and that byte will be read from or written to through the Input/Output pins (I/O_0 - I/O_3).

The nonvolatile functions are inhibited by holding the $\overline{STORE}$ and the $\overline{RECALL}$ high. When the $\overline{RECALL}$ input is taken low, it initiates a recall operation which transfers the contents of the entire E^2PROM array into the Static RAM. When the $\overline{STORE}$ input is taken low, it initiates a store operation which transfers the entire Static RAM array contents into the E^2PROM array.

STANDBY MODE

The chip select ($\overline{CS}$) input controls all of the functions of the CAT22C12I. When a high level is supplied to the $\overline{CS}$ pin, the chip goes into the standby mode. In the mode the chip consumes 99.9% less power and the outputs are put into a high impedance state. Because I_{CCS} is less than 100µA in standby mode, the designer has the flexibility to use this part in battery operated systems.

READ

When the chip is enabled ($\overline{CS}$ = low), the nonvolatile functions are inhibited ($\overline{STORE}$ = high and $\overline{RECALL}$ = high). The Write Enable ($\overline{WE}$) can put the chip into the read mode when it is held high. In this mode, the data in the Static RAM array may be accessed by selecting an address on the input pins A_0 - A_7. This will occur when the outputs are connected to a bus which is loaded by no more than 100pF and 1 TTL gate. If the loading is greater than this, some additional buffering circuitry is recommended.

WRITE

Like the read mode, with the chip enabled and the nonvolatile functions inhibited, the Write Enable ($\overline{WE}$) will select the write mode when taken to a low level. In this mode, the address must be supplied for the byte to be written to. After the set-up time (t_{AS}), the input data must be supplied to pins I/O_0 - I/O_3. When these conditions, including the write pulse width time (t_{WP}), are met, the data will be written to the specified location in the static RAM. A write function may also be initiated from the standby mode by setting $\overline{WE}$ = low, inhibiting the nonvolatile functions, supplying valid addresses, and then taking $\overline{CS}$ low and supplying input data.

RECALL

At anytime, except during a store, taking the $\overline{RECALL}$ pin low will initiate a recall operation. This is independent of the state of $\overline{CS}$, $\overline{WE}$, or A_0-A_7. After the $\overline{RECALL}$ pin has been held low for the duration of the Recall Pulse Width (t_{RCP}), the recall will continue independent of any other inputs. During the recall, the entire content of the EEPROM array is transferred to the Static RAM array. The first byte of data may be externally accessed after the recalled data access time from End of Recall (t_{ARC}). After this, any other bytes may be accessed by using the normal read mode.

If $\overline{RECALL}$ is held low for the entire Recall Cycle time (t_{RCC}), the contents of the Static RAM may be immediately accessed by using the normal read mode. A recall operation can be performed an unlimited number of times without affecting the integrity of the data. A recall operation is automatically performed upon power-up (low to high transition) of V_{CC}.

The outputs I/O_0-I/O_3 will go into the high impedance state as long as the $\overline{RECALL}$ signal is held low.

STORE

At any time, except during a recall operation, taking the $\overline{\text{STORE}}$ pin low will initiate a store operation. This takes place independent of the state of $\overline{\text{CS}}$, $\overline{\text{WE}}$ or A_0-A_7. The $\overline{\text{STORE}}$ pin must be held low for the duration of the Store Pulse Width (t_{STP}) to ensure that a store operation is initiated. Once initiated, the $\overline{\text{STORE}}$ pin may be left low or taken high and the store operations will complete its transfer of the entire contents of the Static RAM array into the E^2PROM array within the Store Cycle time (t_{STC}). However, if a store operation is initiated during the write mode, the contents of the addressed Static RAM byte and its corresponding byte in the E^2PROM array will be unknown.

During the store operation, the outputs are in a high impedance state. At least 10,000 store operations can be performed reliably. The data which is written into the E^2PROM array during a store operation has a data retention time greater than 10 years.

DATA PROTECTION DURING POWER-UP AND POWER-DOWN

The CAT22C12I has on-chip circuitry which will prevent a store operation from occurring when V_{CC} falls below 3.5V. This function eliminates the potential hazard of a spurious signal from initiating a store operation when the system power supply is below 3.5V.

CAT24C44

256-BIT (16x16) NONVOLATILE CMOS SERIAL STATIC RAM

DESCRIPTION

The Catalyst CAT24C44 nonvolatile RAM (NVRAM) is a 256-bit device with a 16 x 16 organization. It features fully static CMOS circuitry for very low power consumption. Active current is 10 mA and standby current is typically 5µA. An internal E^2PROM array provides bit-by-bit backup for the static RAM array. Store operations write data from the RAM to the E^2PROM array. Recall operations write data from the E^2PROM array by either hardware inputs or software commands.

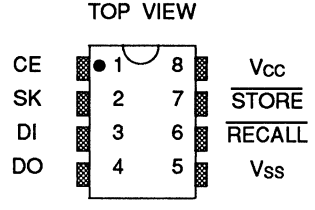
Data retention for each store cycle is specified for over 10 years and over 10,000 store operations can be performed reliably. There are unlimited recall operations from the E^2PROM along with unlimited read and write operations to the RAM.

The CAT24C44 has internal false store protection circuitry to prohibit store operations when V_{CC} is less than 3.5V (typ.). This ensures E^2PROM data integrity. Other internal circuitry performs an automatic recall upon power-up.

FEATURES

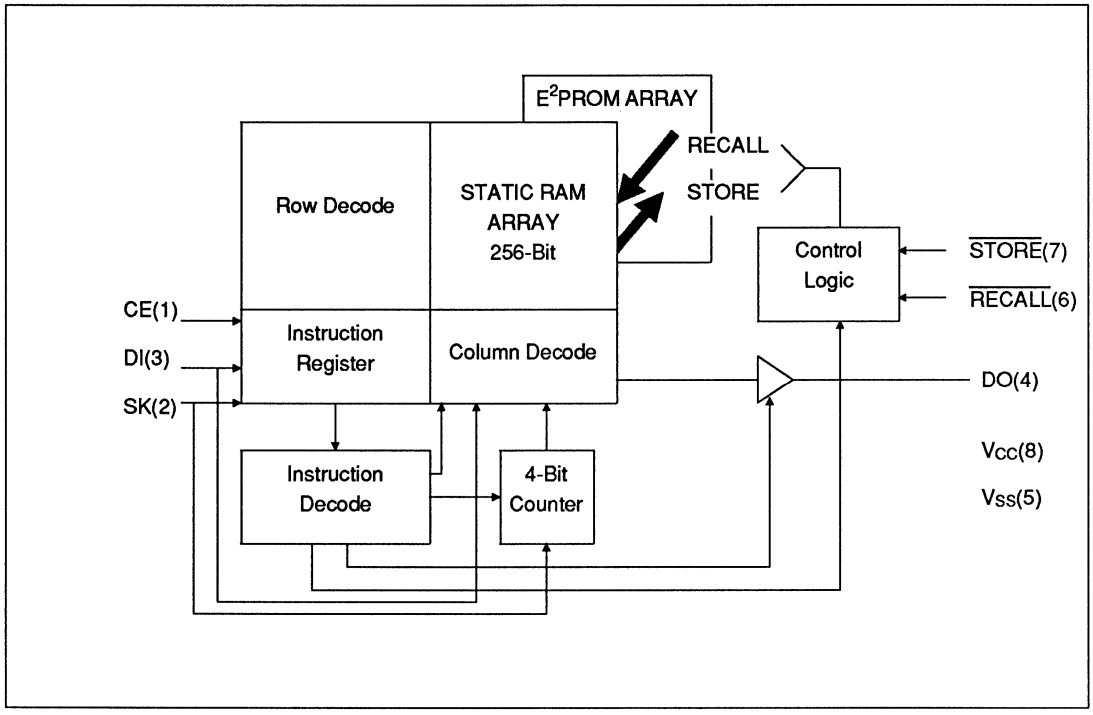
- CMOS technology, completely static operation
- Single 5V supply
- Low current consumption
  - Active: 10mA typ.
  - Standby: 5µA typ., operation
  - Sleep current 5µA typ.
- Software/hardware control of nonvolatile functions
- Fully TTL & CMOS compatible with high drive ability
- Write protection preserves data on power-up and power-down
- Auto-recall on power-up
- Serial port compatible (i.e. COPS™, 8051)
- 3-State output
- Short store pulse: 200ns
- Short recall pulse: 500ns
- False store protection below 3.5V operation level
- 10,000 nonvolatile store cycles ber bit.
- 8 pin low cost 300-mil package

PIN CONFIGURATION



SK	Serial Clock
DI	Serial Data Input
DO	Serial Data Output
$\overline{CE}$	Chip Enable
$\overline{RECALL}$	Recall
$\overline{STORE}$	Store
V_{CC}	+5V
V_{SS}	Ground

BLOCK DIAGRAM



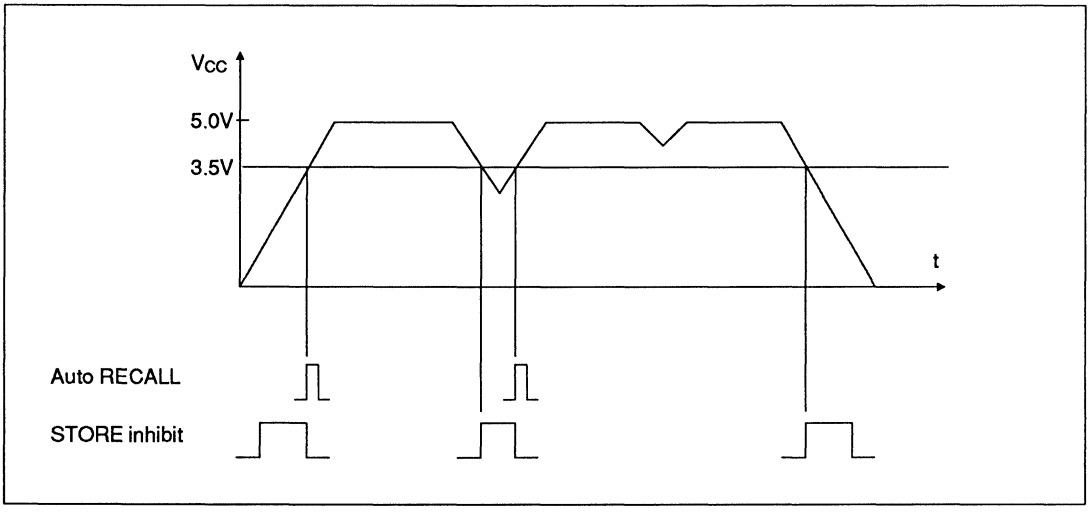
NONVOLATILE MODES OF OPERATION

Operation	$\overline{\text{STORE}}$	$\overline{\text{RECALL}}$	Inst.	Write Enable Latch	Previous RECALL
Hardware recall	1	0		X	X
Software recall	1	1	RCL	X	X
Hardware store	0	1		SET	TRUE
Software store	1	1	STO	SET	TRUE

X = Don't care

NOTES:

- The store operation has priority over all the other operations
- The auto recall is activated on power-up when V_{CC} reaches ≈3.5V
- The store operation is inhibited when V_{CC} is below ≈3.5V
- V_{CC} rise and fall time should be between 10ms and 100ms



MAXIMUM RATINGS *

Storage temperature . . . . . -65°C to +150°C
Temperature under bias . . . . . -50° C to +125°C
Power supply (V_{CC}) . . . . . -0.3 to +6V
Input voltage . . . . . -0.3 to V_{CC} +0.3V
Output voltage . . . . . 0.0 to +V_{CC}
Output current 5mA
Lead temperature . . . . . 260°C
(soldering for 10 seconds)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CCO}	Current consumption (operating)	$T_{I/O}$ = 0mA All inputs=V_{CC}, T_A =0°C		10	20	mA
I_{CCS}	Current consumption (stand-by)	Inputs=V_{CC} or V_{SS}		5	30	µA
I_{SL}	Sleep current	CE=V_{SS}		5	30	µA
I_{LI}	Input current	0 ≤ V_{IN} ≤ 5.5V		0.1	10	µA
I_{LO}	Output leakage current	0 ≤ V_{OUT} ≤ 5.5V		0.1	10	µA
V_{IH}	High level input voltage		2.0		V_{CC}	V
V_{IL}	Low level input voltage		0.0		0.8	V
V_{OH}	High level output voltage	I_{OH} = -2mA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 4.2mA			0.40	V
V_{DH}	Data holding voltage	V_{CC}	1.5		5.5	V

CAPACITANCE

(T_A = 25°C, f = 1.0MHz, V_{CC} = 5V)

Symbol	Parameter	Conditions	Limits Typ. max.	Unit
$C_{I/O}$	Input/Output capacitance	$V_{I/O}$ = 0V	8	pF
C_{IN}	Input capacitance	V_{IN} = 0V	6	pF

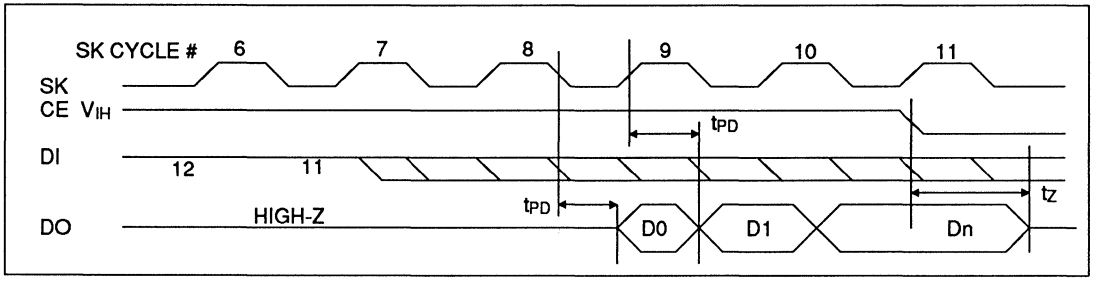
Note: These parameters are periodically sampled and are not 100% tested.

AC CHARACTERISTICS

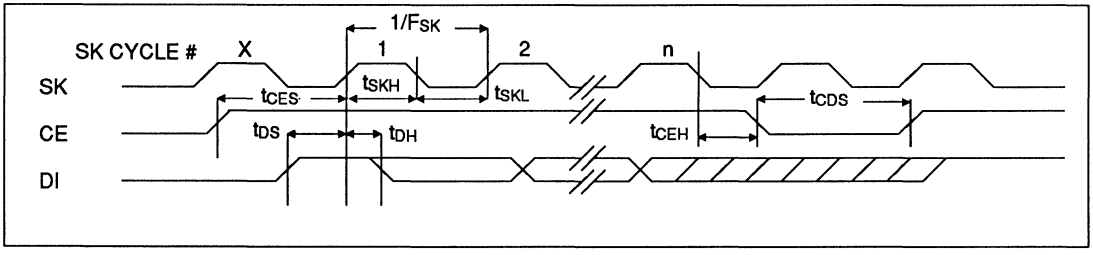
(T_A = 0°C to +70°C, V_{CC} = 5V ±10%)

Symbol	Parameter	Conditions	Min	Max	Units
F_{SK}	SK frequency	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1TTL gate V_{OH} = 2.2V, V_{OL} = 0.65V V_{IH} = 2.2V, V_{IL} = 0.65V Input rise and fall times = 10ns	DC	1.0	MHz
t_{SKH}	SK positive pulse width		400		ns
t_{SKL}	SK negative pulse width		400		ns
t_{DS}	Input data setup time		400		ns
t_{DH}	Input data hold time		80		ns
t_{PD}	SK data valid time			375	ns
t_Z	CE disable time			1.0	µs
t_{CES}	CE enable setup time		800		ns
t_{CEH}	CE enable hold time		400		ns
t_{CDS}	CE de-select time		800		ns

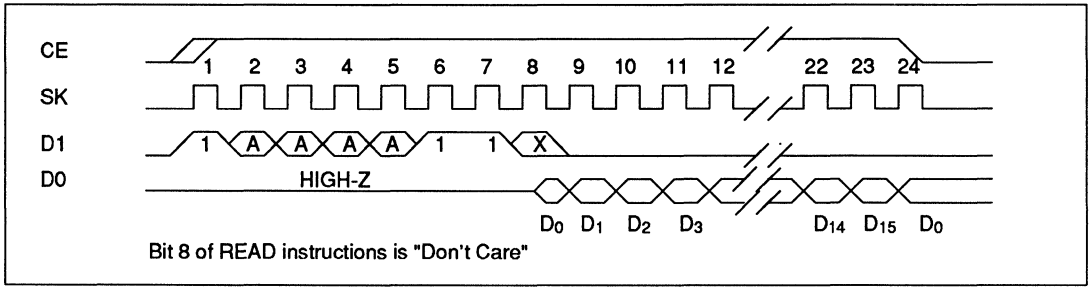
READ CYCLE



WRITE CYCLE

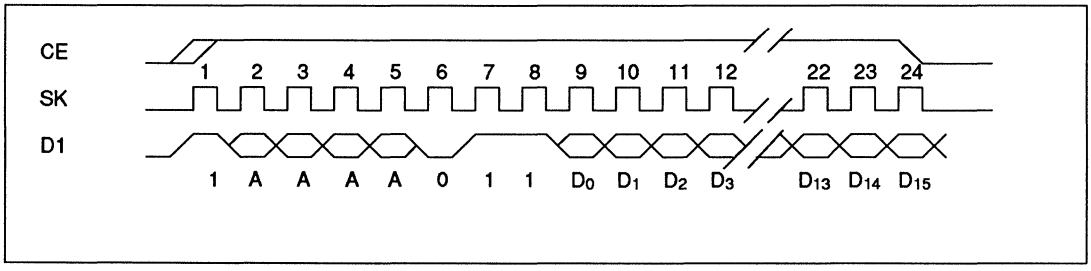


RAM READ



Bit 8 of READ instructions is "Don't Care"

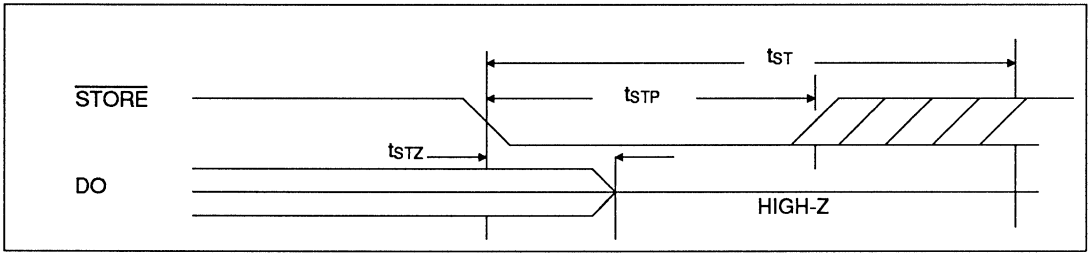
RAM WRITE



STORE CYCLE

Symbol	Parameter	Conditions	Min	Max	Units
t_{ST}	Store time	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1TTL gate V_{OH} = 2.2V, V_{OL} = 0.65V V_{IH} = 2.2V, V_{IL} = 0.65V		10	ms
t_{STP}	Store pulse width		200		ns
t_{STZ}	Store disable time			100	ns

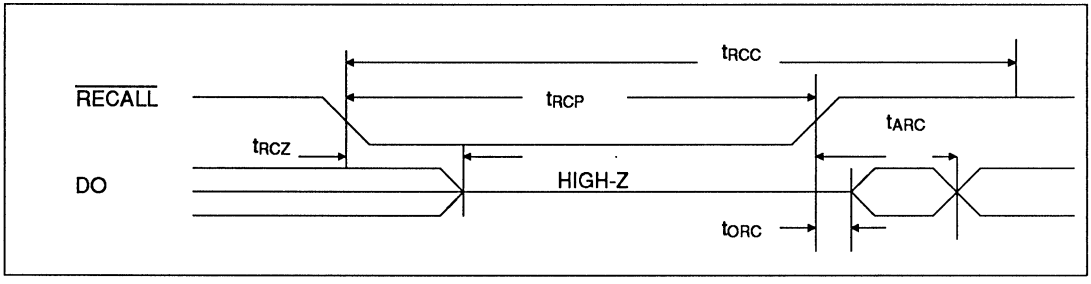
HARDWARE STORE



RECALL CYCLE

Symbol	Parameter	Conditions	Min	Max	Units
t_{RCC}	Recall cycle time	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1TTL gate V_{OH} = 2.2V, V_{OL} = 0.65V V_{IH} = 2.2V, V_{IL} = 0.65V	2500		ns
t_{RCP}	Recall pulse width		500		ns
t_{RCZ}	Recall disable time			500	ns
t_{ORC}	Recall enable time		10		ns
t_{ARC}	Recall data access time			1500	ns

RECALL CYCLE



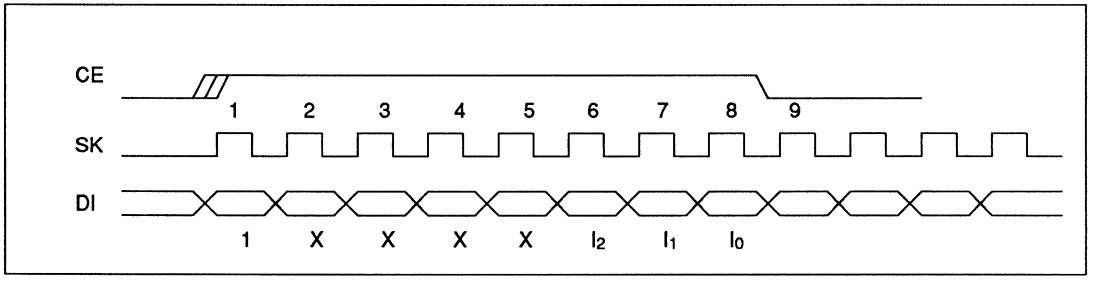
INSTRUCTION SET

Instruction	Format, I_2, I_1, I_0	Operation
WRDS	1XXXX000	Reset write enable latch
STO	1XXXX001	Store RAM data in E^2PROM
SLEEP	1XXXX010	Enter SLEEP mode
WRITE	1AAAA011	Write data into RAM address AAAA
WREN	1XXXX100	Set write enable latch (enables writes and stores)
RCL	1XXXX101	Recall E^2PROM data into RAM
READ	1AAAA11X	Read data from RAM address AAAA

X = Don't care

A = Address bit

NON-DATA OPERATIONS



DEVICE OPERATION

The CAT24C44 is a 256 bit nonvolatile CMOS serial static RAM intended for use with the COPS™ family of microcontrollers, or other standard microprocessors such as the 8048 or 8051. The CAT24C44 is organized as 16 registers by 16 bits. Seven 8 bit instructions control the device's operating modes, the RAM reading and writing, and the E^2PROM storing and recalling. It is also possible to control the E^2PROM store and recall functions in hardware with the $\overline{\text{STORE}}$ and $\overline{\text{RECALL}}$ pins. The CAT24C44 operates on a single 5V supply and will generate, on chip, the high voltage required during a RAM to E^2PROM storing operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin remains in a high impedance state except when outputting data from the device. The CE (chip enable) pin must remain high during the entire data transfer.

The format for all instructions sent to the CAT24C44 is one logical "1" start bit, 4 address bits (data read or write operations) or 4 "don't care" bits (device mode operations), and a 3 bit op code (see table above). For data write operations, the 8 bit instruction is followed by 16 bits of data. For data read instructions, DO will come out of the high impedance state and enable 16 bits of data to be clocked from the device. The 8th bit of the read instruction is a "don't care" bit. This is to eliminate any bus contention that would occur in applications where the DI and DO pins are tied together to form a common DI/O line. A word of caution while clocking data to

or from the device. If the CE pin is prematurely deselected while shifting in an instruction, that instruction will not be executed and the shift register internal to the CAT24C44 will be cleared. If there are more than or less than 16 SK clocks during a memory data transfer, an improper data transfer will result.

WREN/WRDS

The CAT24C44 powers up in the program disable state (the "write enable latch" is reset). Any programming after power-up or after a WRDS (RAM write/E^2PROM store disable) instruction must first be preceded by the WREN (RAM write/E^2PROM store enable) instruction. Once writing/storing is enabled, it will remain enabled until power to the device is removed, the WRDS instruction is sent, or an E^2PROM store has been executed (STO/$\overline{\text{STORE}}$). The WRDS (write/store disable) can be used to disable all CAT24C44 programming functions, and will prevent any accidental writing to the RAM, or storing to the E^2PROM. Data can be read normally from the CAT24C44 regardless of the "write enable latch" status.

SLEEP

The sleep mode places the CAT24C44 into a lower quiescent power mode. Internal RAM power is turned off, and any data that is written into the RAM area is lost. However, data from the last RAM to E^2PROM store operation is retained in the E^2PROM memory. The CAT24C44 will exit the sleep mode, and restore the RAM memory area by issuing either a hardware or software recall command.

RCL/$\overline{\text{RECALL}}$

Data is transferred from the E^2PROM data memory to RAM by either sending the RCL instruction, or by pulling the $\overline{\text{RECALL}}$ input pin low. Although the E^2PROM data is automatically transferred to RAM at power up, a recall operation must be performed before the E^2PROM store, or RAM write operations can be executed. Either recall operation will set the "previous recall latch" internal to the CAT24C44.

STO/$\overline{\text{STORE}}$

Data in the RAM memory area is stored in the E^2PROM memory either by sending the STO instruction or by pulling the $\overline{\text{STORE}}$ input pin low. As security against any inadvertent store operations, the following conditions must each be met before data can be transferred into nonvolatile storage:

a) The "previous recall latch" must be set. (See RCL/$\overline{\text{RECALL}}$)

b) The "write enable latch" must be set. (See WREN/WRDS)

A store operation command must be delivered to the device either by sending the STO instruction or by pulling the $\overline{\text{STORE}}$ input pin low.

During the store operation, all other CAT24C44 functions are inhibited. Upon completion of the store operation the "write enable latch" is reset. The device also provides false store protection whenever V_{CC} falls below a 3.5V level. If V_{CC} falls below this level, the store operation is disabled and the "write enable latch" is reset.

READ

Upon receiving a start bit, 4 address bits, and the 3 bit read command (clocked into the DI pin), the DO pin of the CAT24C44 will come out of the high impedance state and the 16 bits of data, located at the address location specified in the instructions, will be clocked out of the device. When clocking data from the device, the first bit clocked out (D0) is timed from the falling edge of the 8th clock, all succeeding bits (D1 - D15) are timed from the rising edge of the clock. (See Read Cycle timing diagram.)

WRITE

After receiving a start bit, 4 address bits, and the 3 bit WRITE command, the 16 bit word is clocked into the device for storage into the RAM memory location specified.

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CAT24C44 I - Industrial Temperature
256-BIT (16x16) NONVOLATILE CMOS SERIAL STATIC RAM

DESCRIPTION

The Catalyst CAT24C44I nonvolatile RAM (NVRAM) is a 256-bit device with a 16 x 16 organization. It features fully static CMOS circuitry for very low power consumption. Active current is 10 mA and standby current is typically 5µA. An internal E^2PROM array provides bit-by-bit backup for the static RAM array. Store operations write data from the RAM to the E^2PROM array. Recall operations write data from the E^2PROM array by either hardware inputs or software commands.

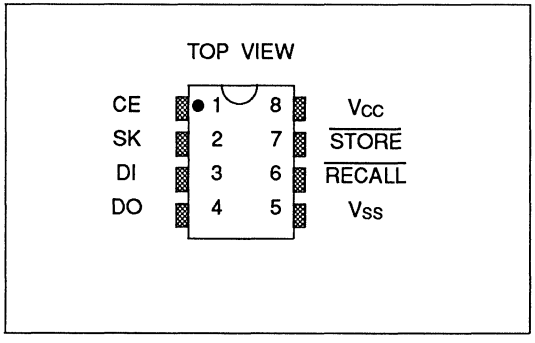
Data retention for each store cycle is specified for over 10 years and over 10,000 store operations can be performed reliably. There are unlimited recall operations from the E^2PROM along with unlimited read and write operations to the RAM.

The CAT24C44I has internal false store protection circuitry to prohibit store operations when V_{CC} is less than 3.5V (typ.). This ensures E^2PROM data integrity. Other internal circuitry performs an automatic recall upon power-up.

FEATURES

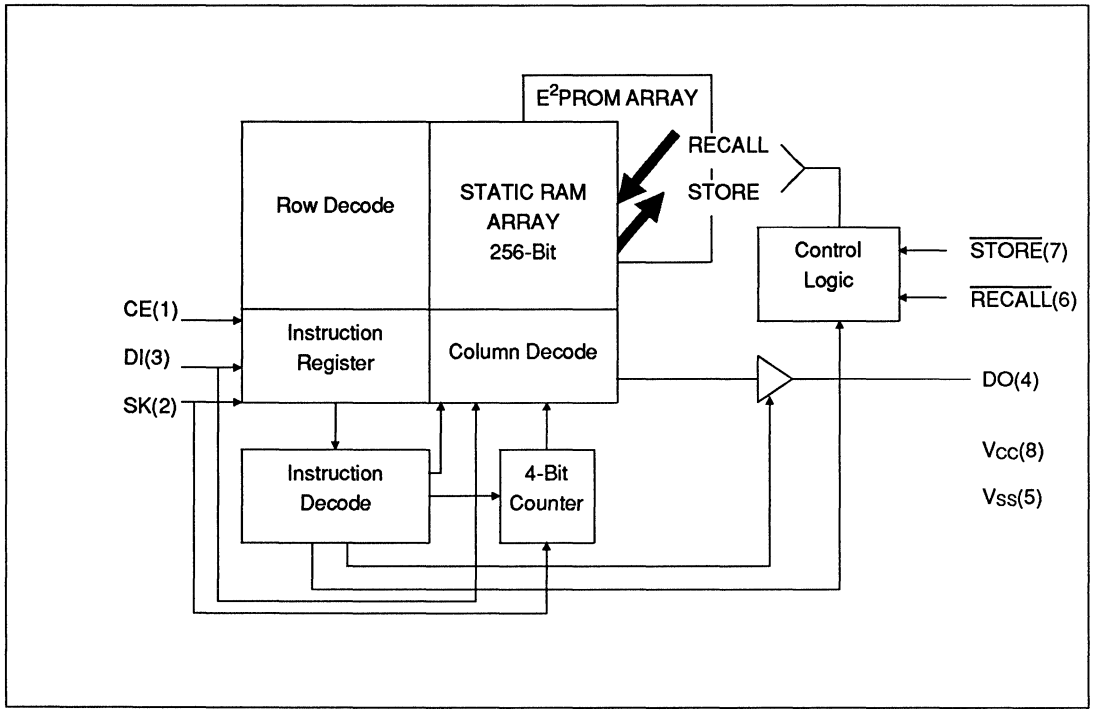
- CMOS technology, completely static operation
- Single 5V supply
- Low current consumption
  - Active: 10mA typ.
  - Standby: 5µA typ., operation
  - Sleep current 5µA typ.
- Software/hardware control of nonvolatile functions
- Fully TTL & CMOS compatible with high drive ability
- Write protection preserves data on power-up and power-down
- Auto-recall on power-up
- Serial port compatible (i.e. COPS™, 8051)
- 3-State output
- Short store pulse: 200ns
- Short recall pulse: 500ns
- False store protection below 3.5V operation level
- 10,000 nonvolatile store cycles ber bit.
- 8 pin low cost 300-mil package

PIN CONFIGURATION



SK	Serial Clock
DI	Serial Data Input
DO	Serial Data Output
$\overline{CE}$	Chip Enable
$\overline{RECALL}$	Recall
$\overline{STORE}$	Store
V_{CC}	+5V
V_{SS}	Ground

BLOCK DIAGRAM



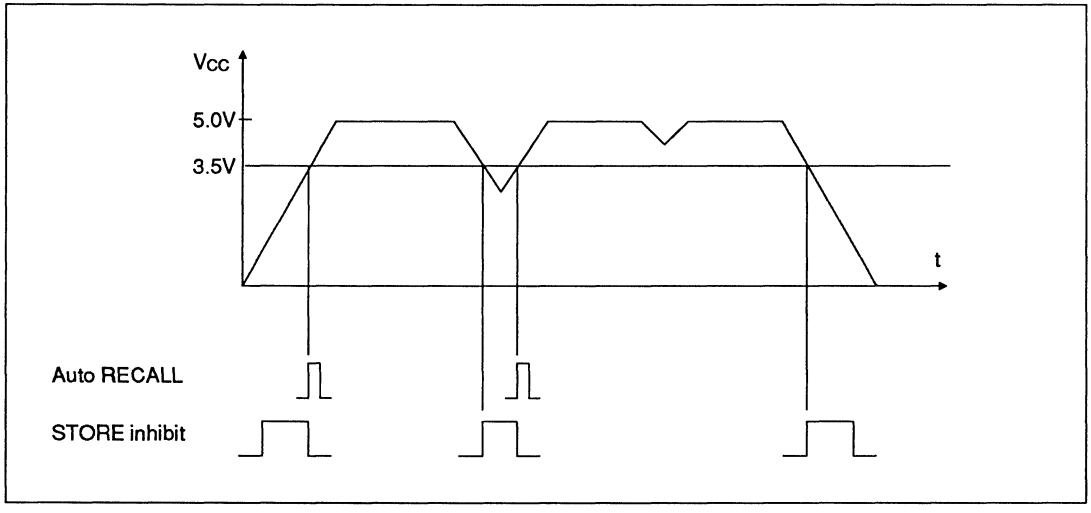
NONVOLATILE MODES OF OPERATION

Operation	$\overline{\text{STORE}}$	$\overline{\text{RECALL}}$	Inst.	Write Enable Latch	Previous RECALL
Hardware recall	1	0		X	X
Software recall	1	1	RCL	X	X
Hardware store	0	1		SET	TRUE
Software store	1	1	STO	SET	TRUE

X = Don't care

NOTES:

- The store operation has priority over all the other operations
- The auto recall is activated on power-up when V_{CC} reaches ≈3.5V
- The store operation is inhibited when V_{CC} is below ≈3.5V
- V_{CC} rise and fall time should be between 10ms and 100ms



MAXIMUM RATINGS *

Storage temperature . . . . . -65°C to +150°C
Temperature under bias . . . . . -50° C to +125°C
Power supply (V_{CC}) . . . . . -0.3 to +6V
Input voltage . . . . . -0.3 to V_{CC} +0.3V
Output voltage . . . . . 0.0 to +V_{CC}
Output current 5mA
Lead temperature . . . . . 260°C
(soldering for 10 seconds)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, CAT24C44I T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CCO}	Current consumption (operating)	$I_{I/O}$ = 0mA All inputs=V_{CC}, T_A =0°C		10	20	mA
I_{CCS}	Current consumption (stand-by)	Inputs=V_{CC} or V_{SS}		5	30	µA
I_{SL}	Sleep current	CE=V_{SS}		5	30	µA
I_{LI}	Input current	0 ≤ V_{IN} ≤ 5.5V		0.1	10	µA
I_{LO}	Output leakage current	0 ≤ V_{OUT} ≤ 5.5V		0.1	10	µA
V_{IH}	High level input voltage		2.0		V_{CC}	V
V_{IL}	Low level input voltage		0.0		0.8	V
V_{OH}	High level output voltage	I_{OH} = -2mA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 4.2mA			0.40	V
V_{DH}	Data holding voltage	V_{CC}	1.5		5.5	V

CAPACITANCE

(T_A = 25°C, f = 1.0MHz, V_{CC} = 5V)

Symbol	Parameter	Conditions	Limits Typ. max.	Unit
$C_{I/O}$	Input/Output capacitance	$V_{I/O}$ = 0V	8	pF
C_{IN}	Input capacitance	V_{IN} = 0V	6	pF

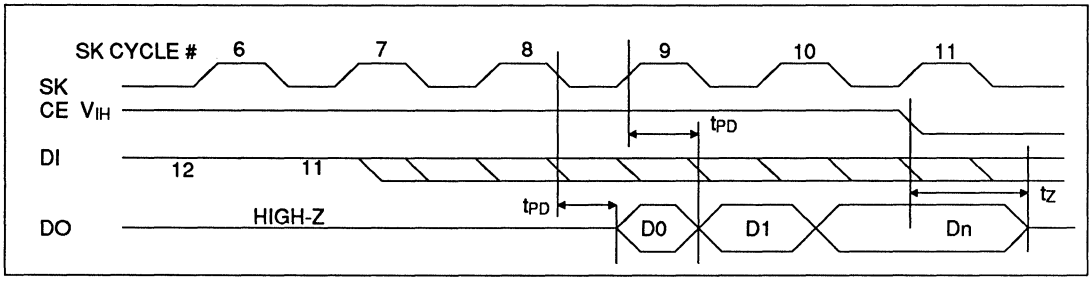
Note: These parameters are periodically sampled and are not 100% tested.

AC CHARACTERISTICS

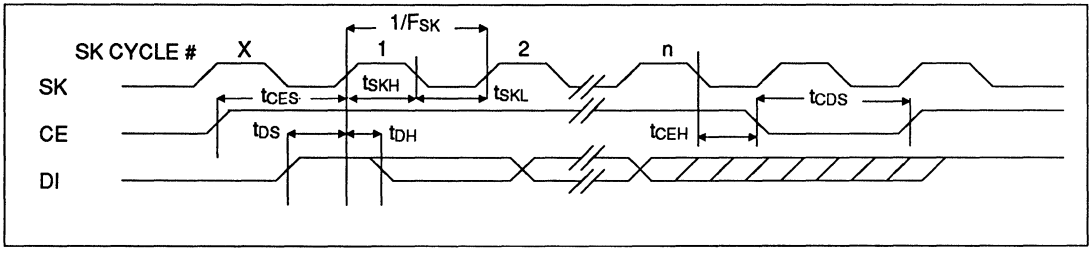
(CAT24C44I T_A = -40°C to +85°C, V_{CC} = 5V ±10%)

Symbol	Parameter	Conditions	Min	Max	Units
F_{SK}	SK frequency	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1TTL gate V_{OH} = 2.2V, V_{OL} = 0.65V V_{IH} = 2.2V, V_{IL} = 0.65V Input rise and fall times = 10ns	DC	1.0	MHz
t_{SKH}	SK positive pulse width		400		ns
t_{SKL}	SK negative pulse width		400		ns
t_{DS}	Input data setup time		400		ns
t_{DH}	Input data hold time		80		ns
t_{PD}	SK data valid time			375	ns
t_Z	CE disable time			1.0	µs
t_{CES}	CE enable setup time		800		ns
t_{CEH}	CE enable hold time		400		ns
t_{CDS}	CE de-select time		800		ns

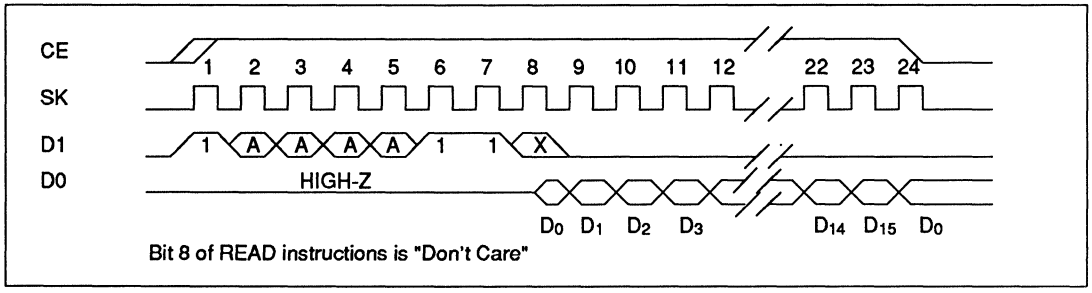
READ CYCLE



WRITE CYCLE

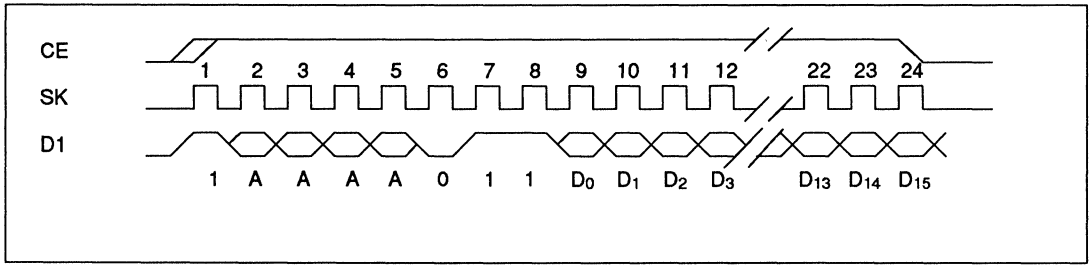


RAM READ



Bit 8 of READ instructions is "Don't Care"

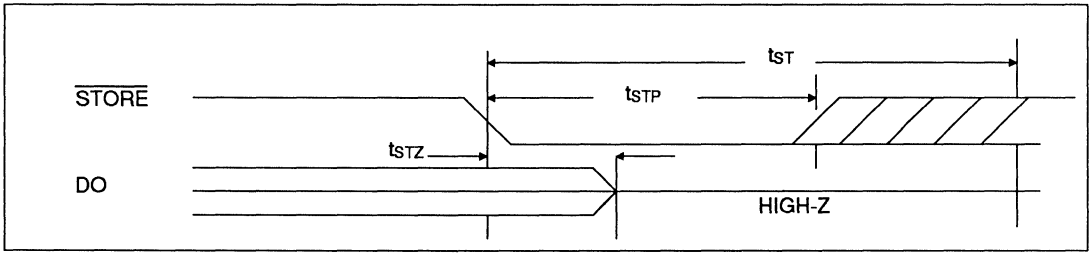
RAM WRITE



STORE CYCLE

Symbol	Parameter	Conditions	Min	Max	Units
t_{ST}	Store time	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1TTL gate V_{OH} = 2.2V, V_{OL} = 0.65V V_{IH} = 2.2V, V_{IL} = 0.65V		10	ms
t_{STP}	Store pulse width		200		ns
t_{STZ}	Store disable time			100	ns

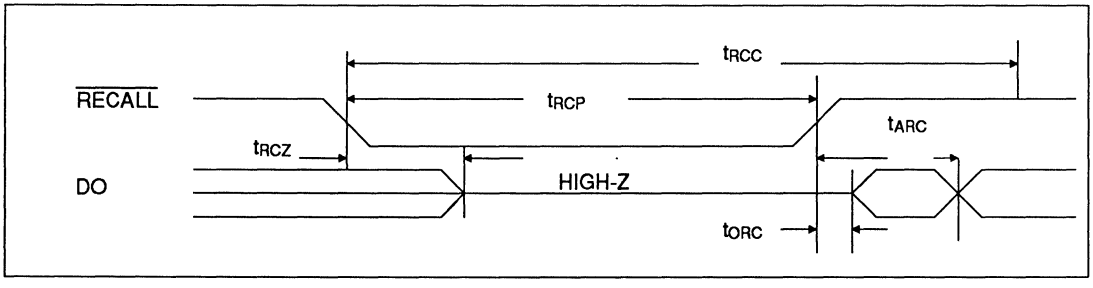
HARDWARE STORE



RECALL CYCLE

Symbol	Parameter	Conditions	Min	Max	Units
t_{RCC}	Recall cycle time	V_{CC} = 4.5 to 5.5V C_L = 100pF + 1TTL gate V_{OH} = 2.2V, V_{OL} = 0.65V V_{IH} = 2.2V, V_{IL} = 0.65V	2500		ns
t_{RCP}	Recall pulse width		500		ns
t_{RCZ}	Recall disable time			500	ns
t_{ORC}	Recall enable time		10		ns
t_{ARC}	Recall data access time			1500	ns

RECALL CYCLE



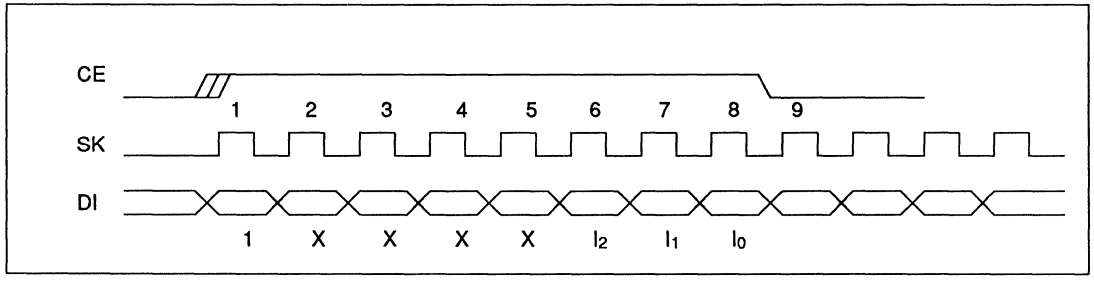
INSTRUCTION SET

Instruction	Format, I_2, I_1, I_0	Operation
WRDS	1XXXX000	Reset write enable latch
STO	1XXXX001	Store RAM data in E^2PROM
SLEEP	1XXXX010	Enter SLEEP mode
WRITE	1AAAA011	Write data into RAM address AAAA
WREN	1XXXX100	Set write enable latch (enables writes and stores)
RCL	1XXXX101	Recall E^2PROM data into RAM
READ	1AAAA11X	Read data from RAM address AAAA

X = Don't care

A = Address bit

NON-DATA OPERATIONS



DEVICE OPERATION

The CAT24C44I is a 256 bit nonvolatile CMOS serial static RAM intended for use with the COPS™ family of microcontrollers, or other standard microprocessors such as the 8048 or 8051. The CAT24C44I is organized as 16 registers by 16 bits. Seven 8 bit instructions control the device's operating modes, the RAM reading and writing, and the E^2PROM storing and recalling. It is also possible to control the E^2PROM store and recall functions in hardware with the $\overline{\text{STORE}}$ and $\overline{\text{RECALL}}$ pins. The CAT24C44 operates on a single 5V supply and will generate, on chip, the high voltage required during a RAM to E^2PROM storing operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin remains in a high impedance state except when outputting data from the device. The CE (chip enable) pin must remain high during the entire data transfer.

The format for all instructions sent to the CAT24C44I is one logical "1" start bit, 4 address bits (data read or write operations) or 4 "don't care" bits (device mode operations), and a 3 bit op code (see table above). For data write operations, the 8 bit instruction is followed by 16 bits of data. For data read instructions, DO will come out of the high impedance state and enable 16 bits of data to be clocked from the device. The 8th bit of the read instruction is a "don't care" bit. This is to eliminate any bus contention that would occur in applications where the DI and DO pins are tied together to form a common DI/O line. A word of caution while clock-

ing data to or from the device. If the CE pin is prematurely deselected while shifting in an instruction, that instruction will not be executed and the shift register internal to the CAT24C44I will be cleared. If there are more than or less than 16 SK clocks during a memory data transfer, an improper data transfer will result.

WREN/WRDS

The CAT24C44I powers up in the program disable state (the "write enable latch" is reset). Any programming after power-up or after a WRDS (RAM write/E^2PROM store disable) instruction must first be preceded by the WREN (RAM write/E^2PROM store enable) instruction. Once writing/storing is enabled, it will remain enabled until power to the device is removed, the WRDS instruction is sent, or an E^2PROM store has been executed (STO/$\overline{\text{STORE}}$). The WRDS (write/store disable) can be used to disable all CAT24C44I programming functions, and will prevent any accidental writing to the RAM, or storing to the E^2PROM. Data can be read normally from the CAT24C44I regardless of the "write enable latch" status.

SLEEP

The sleep mode places the CAT24C44I into a lower quiescent power mode. Internal RAM power is turned off, and any data that is written into the RAM area is lost. However, data from the last RAM to E^2PROM store operation is retained in the E^2PROM memory. The CAT24C44I will exit the sleep mode, and restore the RAM memory area by issuing either a hardware or software recall command.

RCL/$\overline{\text{RECALL}}$

Data is transferred from the E^2PROM data memory to RAM by either sending the RCL instruction, or by pulling the $\overline{\text{RECALL}}$ input pin low. Although the E^2PROM data is automatically transferred to RAM at power up, a recall operation must be performed before the E^2PROM store, or RAM write operations can be executed. Either recall operation will set the "previous recall latch" internal to the CAT24C44I.

STO/$\overline{\text{STORE}}$

Data in the RAM memory area is stored in the E^2PROM memory either by sending the STO instruction or by pulling the $\overline{\text{STORE}}$ input pin low. As security against any inadvertent store operations, the following conditions must each be met before data can be transferred into nonvolatile storage:

a) The "previous recall latch" must be set. (See RCL/$\overline{\text{RECALL}}$)

b) The "write enable latch" must be set. (See WREN/WRDS)

A store operation command must be delivered to the device either by sending the STO instruction or by pulling the $\overline{\text{STORE}}$ input pin low.

During the store operation, all other CAT24C44I functions are inhibited. Upon completion of the store operation the "write enable latch" is reset. The device also provides false store protection whenever V_{CC} falls below a 3.5V level. If V_{CC} falls below this level, the store operation is disabled and the "write enable latch" is reset.

READ

Upon receiving a start bit, 4 address bits, and the 3 bit read command (clocked into the DI pin), the DO pin of the CAT24C44I will come out of the high impedance state and the 16 bits of data, located at the address location specified in the instructions, will be clocked out of the device. When clocking data from the device, the first bit clocked out (D0) is timed from the falling edge of the 8th clock, all succeeding bits (D1 - D15) are timed from the rising edge of the clock. (See Read Cycle timing diagram.)

WRITE

After receiving a start bit, 4 address bits, and the 3 bit WRITE command, the 16 bit word is clocked into the device for storage into the RAM memory location specified.

COPS™ is a trademark of National Semiconductor Corporation.

SECTION 2

EPROMS

COMMERCIAL TEMPERATURE RANGE

INDUSTRIAL TEMPERATURE RANGE

MILITARY TEMPERATURE RANGE

CAT2764A OTP

8,196 x 8-BIT ONE-TIME PROGRAMMABLE ROM

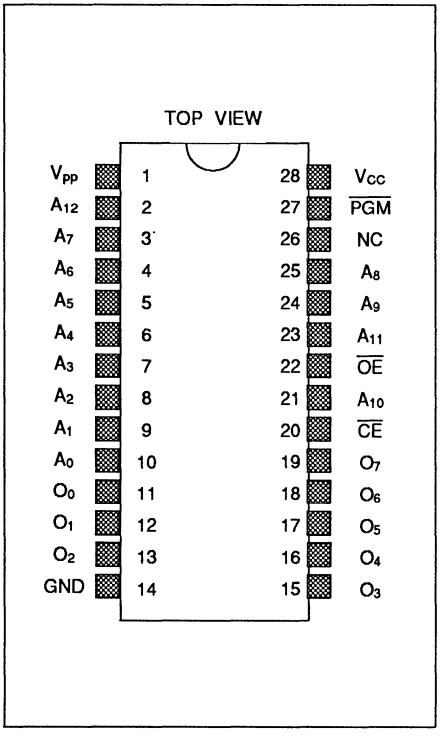
DESCRIPTION

The CAT2764A is a 8,192x8-bit One Time Programmable Read Only Memory (OTPROM). It is offered in a plastic package, ideally suited for high volume production. The fast access time of the CAT2764A allows it to be used in systems that utilize high performance microprocessors with no WAIT states. Two control lines eliminate bus contention in multiple bus microprocessor systems. The CAT2764A is manufactured using N-channel dual-poly silicon gate MOS technology and supplied in a 28-pin JEDEC approved package.

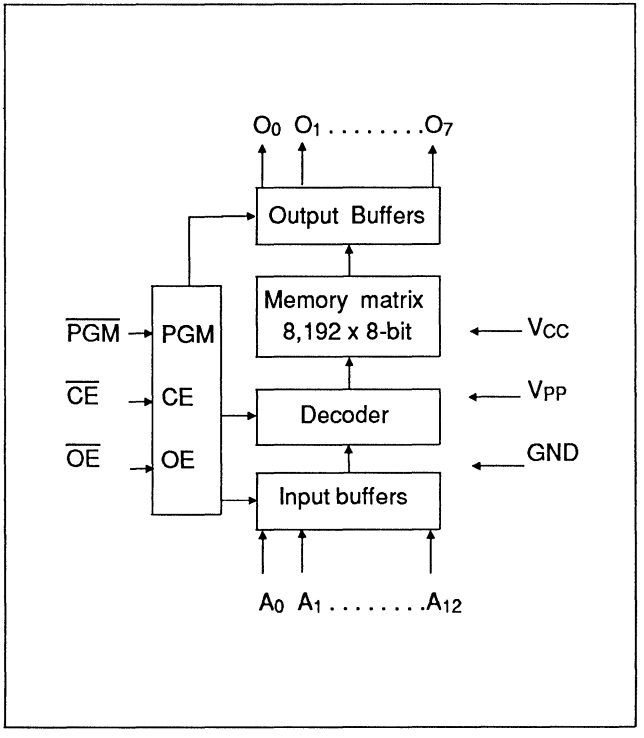
FEATURES

- 5V single power supply
- 8,192 words x 8-bit configuration
- Access time:
  - 150ns max (CAT2764A-15)
  - 200ns max (CAT2764A-20)
  - 250ns max (CAT2764A-25)
- Power consumption:
  - Active: 100mA max
  - Standby: 35mA max
- Fully static operation
- TTL compatible Input/Output (3-state output)

PIN CONFIGURATION



BLOCK DIAGRAM



FUNCTION TABLE

Pins / Mode	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	+5V	+5V	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{IH}	+5V	+5V	High impedance
Standby	V_{IH}	-	-	+5V	+5V	High impedance
Program	V_{IL}	V_{IH}	V_{IL}	+12.5V	+6V	D_{IN}
Program verify	V_{IL}	V_{IL}	V_{IH}	+12.5V	+6V	D_{OUT}
Program inhibit	V_{IH}	-	-	+12.5V	+6V	High impedance

The " - " means the value can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature under bias . . . . . 0°C ~ 70°C
Storage temperature . . . . . - 55°C ~ 125°C
All input/output voltages . . . . . - 0.6 ~ 13.5 V
V_{CC} supply voltage . . . . . - 0.6V ~ 7 V
Program voltage . . . . . - 0.6 ~ 14 V
Power assembly voltage . . . . . 1.5 W

(Voltages with respect to ground)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS <Read Operation>

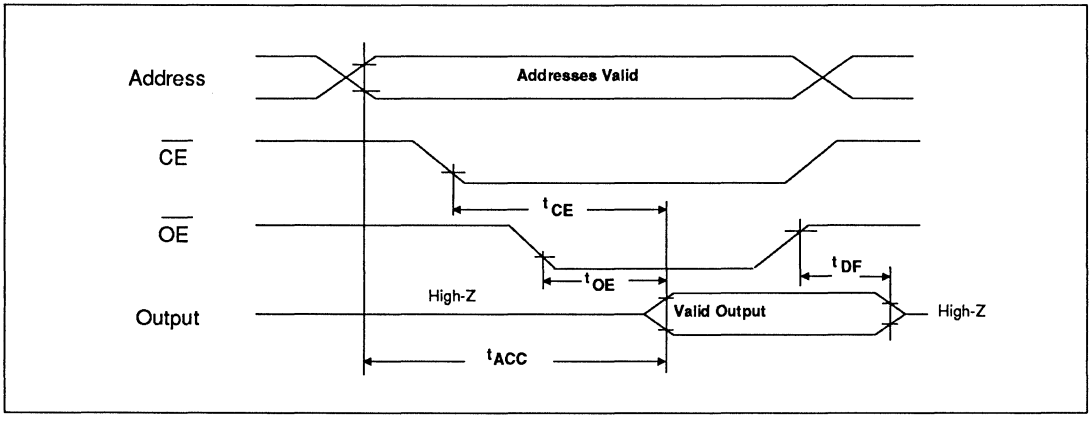
(V_{CC} = 5V ± 5%, V_{PP} = V_{CC}, voltages with respect to ground, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Units
			Min.	Typ.	Max.	
I_{LI}	Input leakage current	$V_{IN} = V_{IH}$ or V_{IL}	-	-	10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.25V	-	-	10	µA
I_{CC1}	V_{CC} power current (stand-by)	$\overline{CE} = V_{IH}$, outputs unloaded	-	-	35	mA
I_{CC2}	V_{CC} power current (operation)	$\overline{CE} = V_{IL}$, outputs unloaded	-	-	100	mA
I_{PP1}	Program power current	$V_{PP} = V_{CC}$	-	-	5	mA
V_{IH}	Input voltage "H" level	-	2.0	-	V_{CC}+1	V
V_{IL}	Input voltage "L" level	-	-0.1	-	0.8	V
V_{OH}	Output voltage "H" level	I_{OH} = -400µA	2.4	-	-	V
V_{OL}	Output voltage "L" level	I_{OL} = 2.1mA	-	-	0.45	V

AC CHARACTERISTICS <Read Operation>

(V_{CC} = 5V ± 5%, V_{PP} = V_{CC}, $\overline{PGM} = V_{IH}$, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	2764A-15		2764A-20		2764A-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACC}	Address access time	$\overline{CE} = \overline{OE} = V_{IL}$	-	150	-	200	-	250	ns
t_{CE}	$\overline{CE}$ access time	$\overline{OE} = V_{IL}$	-	150	-	200	-	250	ns
t_{OE}	$\overline{OE}$ access time	$\overline{CE} = V_{IL}$	-	60	-	70	-	100	ns
t_{DF}	Output disable time	$\overline{CE} = V_{IL}$	0	50	0	60	0	70	ns



DC CHARACTERISTICS <Programming Operation>

(V_{CC} = 5.75 - 6.5V, V_{PP} = 12.5V ± 0.5V, T_A = 25°C ± 5°C)

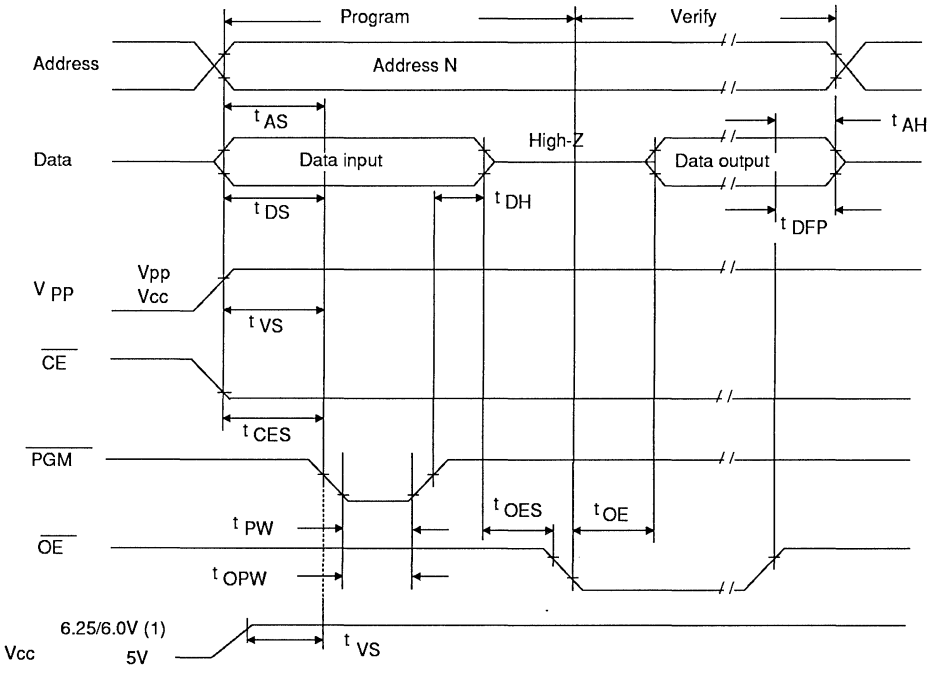
Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{LI}	Input leakage current	$V_{IN} = V_{IH}$ or V_{IL}	-	-	10	µA
I_{PP}	V_{PP} power current	$\overline{CE} = \overline{PGM} = V_{IL}$	-	-	50	mA
I_{CC}	V_{CC} power current	-	-	-	100	mA
V_{IH}	Input voltage "H" level	-	2.0	-	V_{CC}+1	V
V_{IL}	Input voltage "L" level	-	-0.1	-	0.8	V
V_{OH}	Output voltage "H" level	I_{OH} = -400µA	2.4	-	-	V
V_{OL}	Output voltage "L" level	I_{OL} = 2.1mA	-	-1.05	0.45	V

AC CHARACTERISTICS <Programming Operation>

(V_{CC} = 5.75 - 6.5V, V_{PP} = 12.5V ± 0.5V, T_A = 25°C ± 5°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{AS}	Address set-up time	-	2	-	-	µs
t_{OES}	$\overline{OE}$ set-up time	-	2	-	-	µs
t_{DS}	Data set-up time	-	2	-	-	µs
t_{AH}	Address hold time	-	0	-	-	µs
t_{DH}	Data hold time	-	2	-	-	µs
t_{DFP}	Output enable to output float delay	-	0	-	130	ns
t_{VS}	V_{PP} and V_{CC} power set-up times	-	2	-	-	µs
t_{PW}	$\overline{PGM}$ initial program pulse width	V_{CC} = 6V ±0.25V	0.95	1.0	1.05	ms
t_{PW}	High-speed initial program pulse width	V_{CC} = 6.25V ±0.25V	95	100	105	µs
t_{OPW}	$\overline{PGM}$ overprogram pulse width	V_{CC} = 6V ±0.25V	2.85	-	78.75	ms
t_{CES}	$\overline{CE}$ set-up time	-	2	-	-	µs
t_{OE}	Data valid from $\overline{OE}$	-	-	-	150	ns

TIMING <Programming Operation>



(1) Note: V_{CC} = 6.25 V ± 0.25V for Quick Pulse Programming™, 6.00V ± 0.25V for Intelligent Programming™.

Programming Mode

As shipped, all bits of the OTPROM are in the logic one state. The device is programmed by selectively writing logic zeros into the desired bit locations. To enter the programming mode, V_{CC} and V_{PP} must be adjusted to their programming levels, the device must be selected ($\overline{CE}$ = V_{IL}), outputs are disabled ($\overline{OE}$ = V_{IH}), and a program write pulse must be applied to the $\overline{PGM}$ pin. After the program write pulse, the programmed data may be verified by enabling the outputs ($\overline{OE}$ = V_{IL}) and comparing the written data to the read data. This device is compatible with the Intelligent Programming™ algorithm, and the Quick Pulse Programming™ algorithm. Intelligent Programming and Quick Pulse Programming are registered trademarks of Intel Corp. [9/87]

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

CAT27128A OTP

16,384 x 8-BIT ONE-TIME PROGRAMMABLE ROM

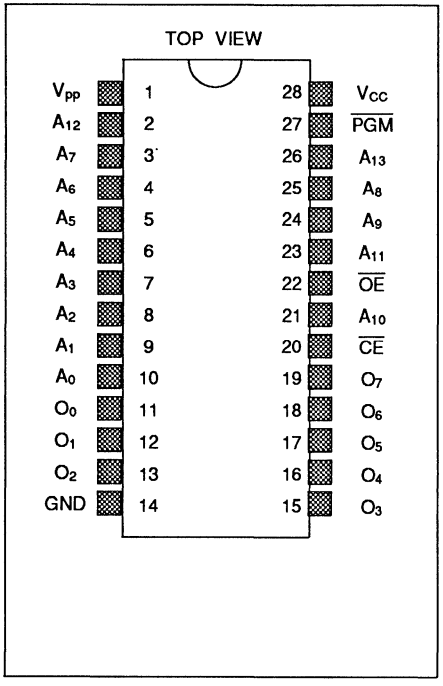
DESCRIPTION

The CAT27128A is a One Time Programmable Read Only Memory (OTPROM). It is offered in a plastic package, ideally suited for high volume production. The fast access time of the CAT27128A allows it to be used in systems that utilize high performance microprocessor systems. The CAT27128A is manufactured using N-channel dual-poly silicon gate MOS technology and supplied in a 28-pin JEDEC approved package.

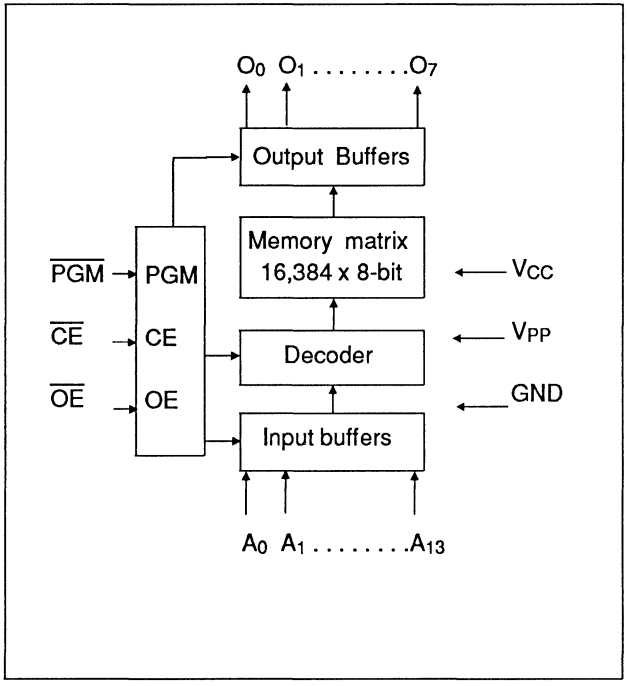
FEATURES

- 5V single power supply
- 16,384 words x 8-bit configuration
- Access time:
  - 150ns max (CAT27128A-15)
  - 200ns max (CAT27128A-20)
  - 250ns max (CAT27128A-25)
- Power consumption:
  - Active: 100mA
  - Standby: 35mA
- Fully static operation
- TTL compatible Input/Output (3-state output)

PIN CONFIGURATION



BLOCK DIAGRAM



FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	+5V	+5V	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{IH}	+5V	+5V	High impedance
Standby	V_{IH}	-	-	+5V	+5V	High impedance
Program	V_{IL}	V_{IH}	V_{IL}	+12.5V	+6V	D_{IN}
Program verify	V_{IL}	V_{IL}	V_{IH}	+12.5V	+6V	D_{OUT}
Program inhibit	V_{IH}	-	-	+12.5V	+6V	High impedance

The " - " means the value can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature under bias . . . . . 0°C ~ 70°C
Storage temperature . . . . . - 55°C ~ 125°C
All input/output voltages . . . . . - 0.6 ~ 13.5V
V_{CC} supply voltage . . . . . - 0.6V ~ 7V
Program voltage . . . . . - 0.6 ~ 14V
Power assembly voltage 1.5W

(Voltages with respect to ground)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS <Read Operation>

(V_{CC} = 5V ± 5%, V_{PP} = V_{CC} voltages with respect to ground, T_A = 0°C to 70°C)

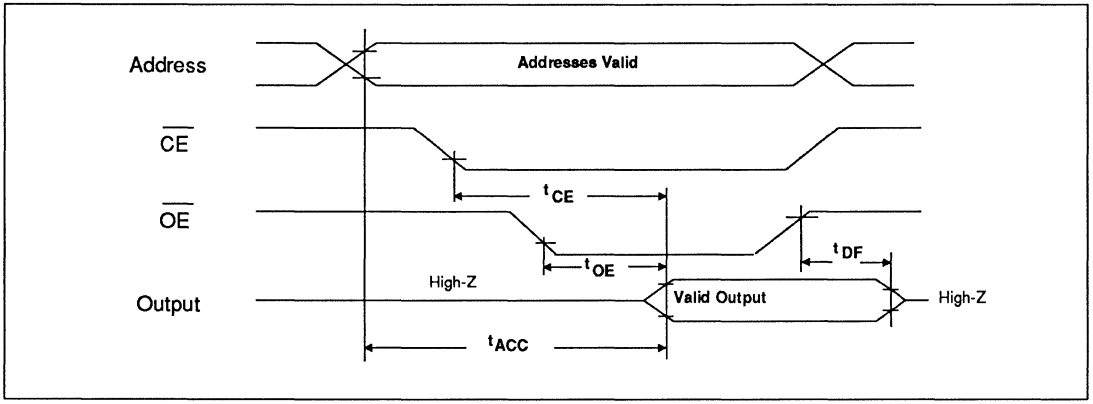
Symbol	Parameter	Conditions	Limits Min.	Typ.	Max.	Units
I_{LI}	Input leakage current	V_{IN} = V_{IH} or V_{IL}	-	-	10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.25V	-	-	10	µA
I_{CC1}	V_{CC} power current (standby)	$\overline{CE}$ = V_{IH}, outputs unloaded	-	-	35	mA
I_{CC2}	V_{CC} power current (operation)	$\overline{CE}$ = V_{IL}, outputs unloaded	-	-	100	mA
I_{PP1}	Program power current	V_{PP} = V_{CC}	-	-	5	mA
V_{IH}	Input voltage "H" level	-	2.0	-	V_{CC}+1	V
V_{IL}	Input voltage "L" level	-	-0.1	-	0.8	V
V_{OH}	Output voltage "H" level	I_{OH} = -400µA	2.4	-	-	V
V_{OL}	Output voltage "L" level	I_{OL} = 2.1mA	-	-	0.45	V

AC CHARACTERISTICS <Read Operation>

(V_{CC} = 5V ± 5%, V_{PP} = V_{CC}, $\overline{PGM}$ = V_{IH}, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	27128A-15 Min.	Max.	27128A-20 Min.	Max.	27128A-25 Min.	Max.	Unit
t_{ACC}	Address access time	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	-	150	-	200	-	250	ns
t_{CE}	$\overline{CE}$ access time	$\overline{OE}$ = V_{IL}	-	150	-	200	-	250	ns
t_{OE}	$\overline{OE}$ access time	$\overline{CE}$ = V_{IL}	-	60	-	75	-	100	ns
t_{DF}	Output disable time	$\overline{CE}$ = V_{IL}	0	50	0	60	0	70	ns

TIMING <Read Operation>



DC CHARACTERISTICS <Programming Operation>

(V_{CC} = 5.75 - 6.5V, V_{PP} = 12.5V ± 0.5V, T_A = 25°C ± 5°C)

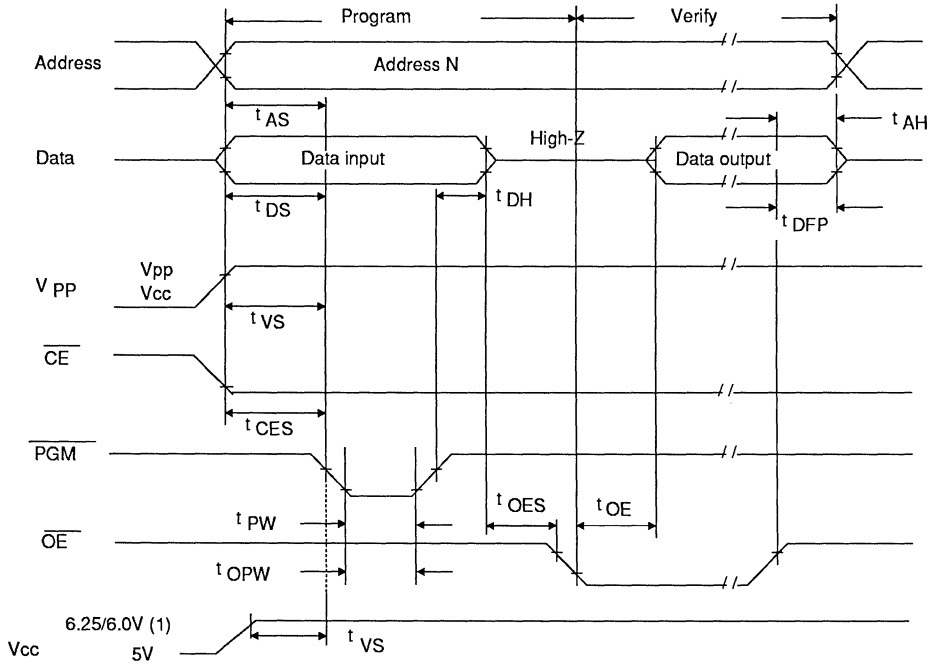
Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{LI}	Input leakage current	$V_{IN} = V_{IH}$ or V_{IL}	-	-	10	µA
I_{PP}	V_{PP} power current	$\overline{CE} = \overline{PGM} = V_{IL}$ All outputs unloaded	-	-	50	mA
I_{CC}	V_{CC} power current	All outputs unloaded	-	-	100	mA
V_{IH}	Input voltage "H" level	-	2.0	-	V_{CC}+1	V
V_{IL}	Input voltage "L" level	-	-0.1	-	0.8	V
V_{OH}	Output voltage "H" level	I_{OH} = -400µA	2.4	-	-	V
V_{OL}	Output voltage "L" level	I_{OL} = 2.1mA	-	-	0.45	V

AC CHARACTERISTICS <Programming Operation>

(V_{CC} = 5.75 - 6.5V, V_{PP} = 12.5V ± 0.5V, T_A = 25°C ± 5°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{AS}	Address set-up time	-	2	-	-	µs
t_{OES}	$\overline{OE}$ set-up time	-	2	-	-	µs
t_{DS}	Data set-up time	-	2	-	-	µs
t_{AH}	Address hold time	-	0	-	-	µs
t_{DH}	Data hold time	-	2	-	-	µs
t_{DFP}	Output enable to output float delay	-	0	-	130	ns
t_{VS}	V_{PP} and V_{CC} power set-up times	-	2	-	-	µs
t_{PW}	$\overline{PGM}$ initial program pulse width	V_{CC} = 6V ±0.25V	0.95	1.0	1.05	ms
t_{PW}	High-speed initial program pulse width	V_{CC} = 6.25V ±0.25V	95	100	105	µs
t_{OPW}	$\overline{PGM}$ overprogram pulse width	V_{CC} = 6V ±0.25V	2.85	-	78.75	ms
t_{CES}	$\overline{CE}$ set-up time	-	2	-	-	µs
t_{OE}	Data valid from $\overline{OE}$	-	-	-	150	ns

TIMING <Programming Operation>



(1) Note: V_{CC} = 6.25 V ± 0.25V for Quick Pulse Programming™, 6.00V ± 0.25V for Intelligent Programming™.

Programming Mode

As shipped, all bits of the OTPROM are in the logic one state. The device is programmed by selectively writing logic zeros into the desired bit locations. To enter the programming mode, V_{CC} and V_{PP} must be adjusted to their programming levels, the device must be selected ($\overline{CE}$ = V_{IL}), outputs are disabled ($\overline{OE}$ = V_{IH}), and a program write pulse must be applied to the $\overline{PGM}$ pin. After the program write pulse, the programmed data may be verified by enabling the outputs ($\overline{OE}$= V_{IL}) and comparing the written data to the read data. This device is compatible with the Intelligent Programming ™ algorithm, and the Quick Pulse Programming ™ algorithm. Intelligent Programming and Quick Pulse Programming are registered trademarks of Intel Corp. [9/87]

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

CAT27256 OTP

32,768 x 8-BIT ONE-TIME PROGRAMMABLE ROM

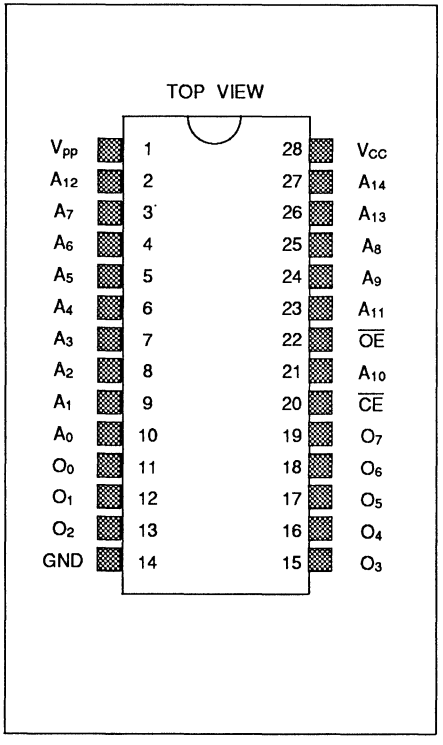
DESCRIPTION

The CAT27256 is a 32,768x8-bit One Time Programmable Read Only Memory (OTPROM). It is offered in a plastic package, ideally suited for high volume production. The fast access time of the CAT27256 allows it to be used in systems that utilize high performance microprocessors with no WAIT states. Two control lines eliminate bus contention in multiple bus microprocessor systems. The CAT27256 is manufactured using N-channel dual-poly silicon gate MOS technology and supplied in a 28-pin JEDEC-approved package.

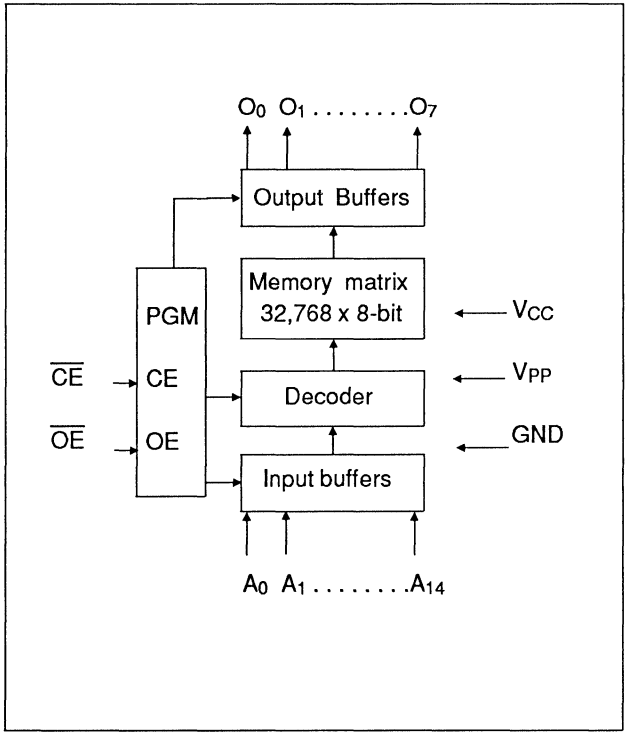
FEATURES

- 5V single power supply
- 32,768 words x 8-bit configuration
- Access time:
  - 170ns max (CAT27256-17)
  - 200ns max (CAT27256-20)
  - 250ns max (CAT27256-25)
- Power consumption:
  - Active: 100mA max
  - Standby: 35mA max
- Fully static operation
- TTL compatible Input/Output (3-state output)

PIN CONFIGURATION



BLOCK DIAGRAM



FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	+5V	+5V	D_{OUT}
Output disable	V_{IL}	V_{IH}	+5V	+5V	High impedance
Standby	V_{IH}	-	+5V	+5V	High impedance
Program	V_{IL}	V_{IH}	+12.5V	+6V	D_{IN}
Program verify	V_{IH}	V_{IL}	+12.5V	+6V	D_{OUT}
Program inhibit	V_{IH}	V_{IH}	+12.5V	+6V	High impedance

The " - " means the value can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature under bias . . . . . 0°C ~ 70 °C
Storage temperature . . . . . - 55°C ~ 125 °C
All input/output voltages . . . . . - 0.6 ~ 13.5V
V_{CC} supply voltage . . . . . - 0.6V ~ 7V
Program Voltage . . . . . - 0.6 ~ 14V
Power assembly voltage 1.5W

(Voltages with respect to ground)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS <Read Operation>

(V_{CC} = 5V ± 5%, V_{PP} = V_{CC} voltages with respect to ground, T_A = 0°C to 70°C)

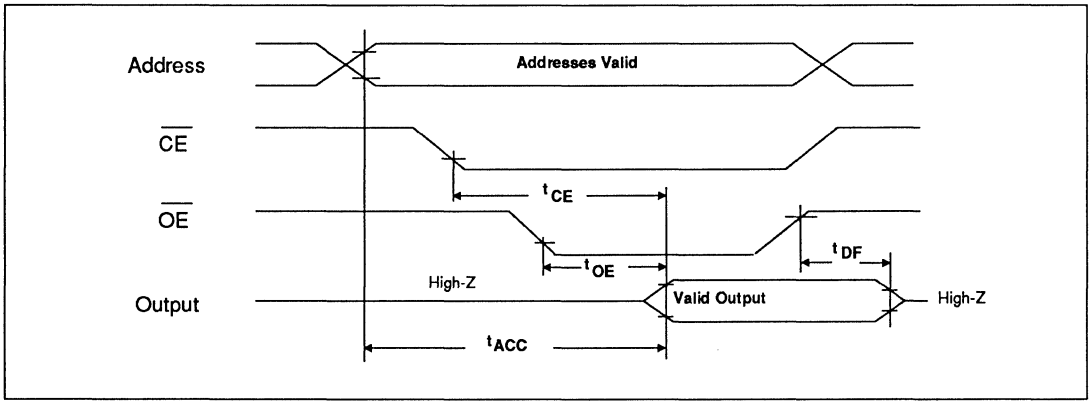
Symbol	Parameter	Conditions	Limits			Units
			Min.	Typ.	Max.	
I_{LI}	Input leakage current	V_{IN} = 5.25V	-	-	10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.25V	-	-	10	µA
I_{CC1}	V_{CC} power current (standby)	$\overline{CE}$ = V_{IH}	-	-	35	mA
I_{CC2}	V_{CC} power current (operation)	$\overline{CE}$ = V_{IL}	-	-	100	mA
I_{PP1}	Program power current	V_{PP} = V_{CC}	-	-	5	mA
V_{IH}	Input voltage "H" level	-	2.0	-	V_{CC}+1	V
V_{IL}	Input voltage "L" level	-	-0.1	-	0.8	V
V_{OH}	Output voltage "H" level	I_{OH} = -400µA	2.4	-	-	V
V_{OL}	Output voltage "L" level	I_{OL} = 2.1mA	-	-	0.45	V

AC CHARACTERISTICS <Read Operation>

(V_{CC} = 5V ± 5%, V_{PP} = V_{CC}, $\overline{PGM}$ = V_{IH}, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	27256-17		27256-20		27256-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACC}	Address access time	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	-	170	-	200	-	250	ns
t_{CE}	$\overline{CE}$ access time	$\overline{OE}$ = V_{IL}	-	170	-	200	-	250	ns
t_{OE}	$\overline{OE}$ access time	$\overline{CE}$ = V_{IL}	-	60	-	75	-	100	ns
t_{DF}	Output disable time	$\overline{CE}$ = V_{IL}	0	50	0	55	0	60	ns

TIMING <Read Operation>



DC CHARACTERISTICS <Programming Operation>

(V_{CC} = 5.75 - 6.5V, V_{PP} =12.5V ± 0.5V, T_A = 25°C ± 5°C)

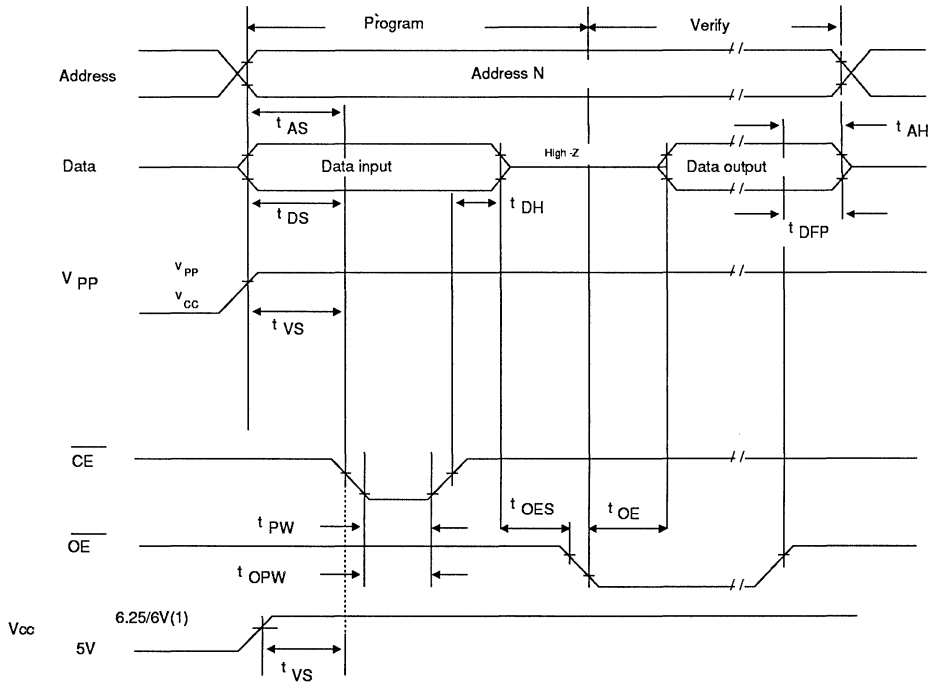
Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{LI}	Input leakage current	V_{IN} = 5.25V	-	-	10	µA
I_{PP}	V_{PP} power current	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	-	-	50	mA
I_{CC}	V_{CC} power current	-	-	-	100	mA
V_{IH}	Input voltage "H" level	-	2.0	-	V_{CC}+1	V
V_{IL}	Input voltage "L" level	-	-0.1	-	0.8	V
V_{OH}	Output voltage "H" level	I_{OH} = -400µA	2.4	-	-	V
V_{OL}	Output voltage "L" level	I_{OL} = 2.1mA	-	-	0.45	V

AC CHARACTERISTICS <Programming Operation>

(V_{CC} = 5.75 - 6.5V, V_{PP} = 12.5V ± 0.5V, T_A = 25°C ± 5°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{AS}	Address set-up time	-	2	-	-	µs
t_{OES}	$\overline{OE}$ set-up time	-	2	-	-	µs
t_{DS}	Data set-up time	-	2	-	-	µs
t_{AH}	Address hold time	-	0	-	-	µs
t_{DH}	Data hold time	-	2	-	-	µs
t_{DFP}	Output enable to output float delay	-	0	-	130	ns
t_{VS}	V_{PP} power set-up times	-	2	-	-	µs
t_{PW}	$\overline{CE}$ initial program pulse width	V_{CC} = 6V ±0.25V	0.95	1.0	1.05	ms
t_{PW}	$\overline{CE}$ program pulse width	V_{CC} = 6.25V ±0.25V	95	100	105	µs
t_{OPW}	$\overline{CE}$ overprogram pulse width	V_{CC} = 6V ±0.25V	2.85	-	78.75	ms
t_{OE}	Data valid from $\overline{OE}$	-	-	-	150	ns
t_{OE}	Data valid from $\overline{OE}$	-	-	-	150	ns

TIMING <Programming Operation>



(1) Note: V_{CC} = 6.25 V ± 0.25V for Quick Pulse Programming™, 6.00V ± 0.25V for Intelligent Programming™.

Programming Mode

As shipped, all bits of the OTPROM are in the logic one state. The device is programmed by selectively writing logic zeros into the desired bit locations. To enter the programming mode, V_{CC} and V_{PP} must be adjusted to their programming levels, outputs are disabled ($\overline{OE}$ = V_{IH}), and a program write pulse must be applied to the $\overline{CE}$ pin. After the program write pulse the programmed data may be verified by enabling the outputs ($\overline{OE}$=V_{IL}) and comparing the written data to the read data. This device is compatible with the Intelligent Programming™ algorithm, and the Quick Pulse Programming™ algorithm. Intelligent Programming and Quick Pulse Programming are registered trademarks of Intel Corp. [9/87]

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

CAT27HC256

32,768 x 8-BIT HIGH-SPEED CMOS EPROM

Preliminary

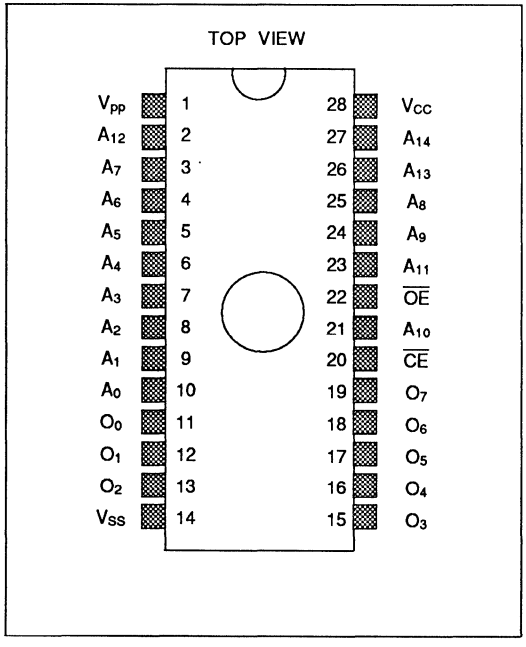
DESCRIPTION

The CAT27HC256 is a high speed 256K UV erasable and electrically reprogrammable EPROM ideally suited for high speed applications. Any byte can be accessed in less than 55ns, making this part compatible with high performance microprocessor systems by eliminating the need for speed-robbing wait states. The Quick Pulse algorithm reduces the time required to program this chip and ensures more reliable programming. The CAT27HC256 is used in applications where fast turnaround and pattern experimentation are important requirements. The CAT27HC256 is available in a 28-pin dual-in-line package with a transparent lid. This allows the user to expose the chip to ultraviolet light to erase the bit pattern, allowing a new pattern to be written into the device.

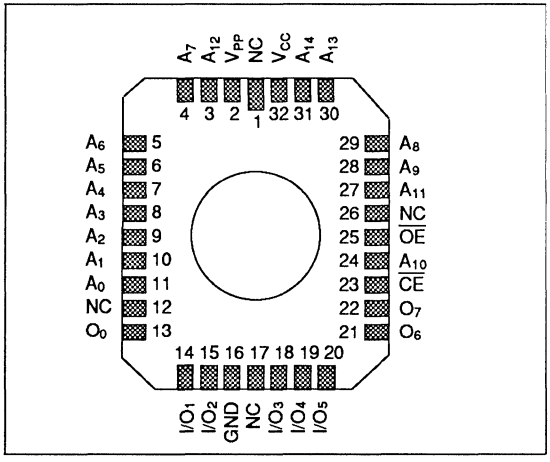
FEATURES

- Fast access time: 55/70/90/120 ns
- 5V single power supply - read mode
- 32,768 words x 8-bit configuration
- Low current requirements:
  - Active: 60mA max (CMOS levels)
  - Standby: 500µA (CMOS levels)
  - Standby: 2mA (TTL levels)
- High speed programming: 100µs/byte
- TTL compatible Input/Output
- 12.5V programming voltage
- JEDEC approved 28-pin DIP and 32-pin LCC
- Electronic signature
- Industrial and military temp. devices available

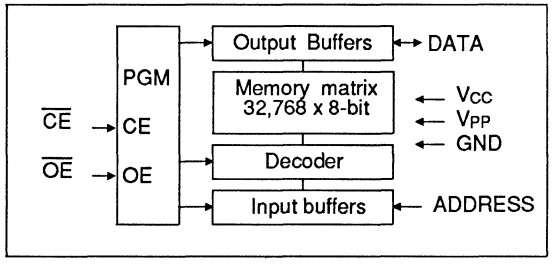
PIN CONFIGURATION 28-PIN DIP



PIN CONFIGURATION 32-PIN LCC



BLOCK DIAGRAM



FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	A_0 (10)	A_9 (24)	I/O
Read	V_{IL}	V_{IL}	V_{CC}	-	-	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{CC}	-	-	High Z
Stand-by	V_{IH}	-	V_{CC}	-	-	High Z
Program	V_{IL}	V_{IH}	V_{PP}	-	-	D_{IN}
Program verify	V_{IH}	V_{IL}	V_{PP}	-	-	D_{OUT}
Program inhibit	V_{IH}	V_{IH}	V_{PP}	-	-	High Z
Signature MFG.	V_{IL}	V_{IL}	V_{CC}	V_{IL}	V_H	31H
Signature device	V_{IL}	V_{IL}	V_{CC}	V_{IH}	V_H	40H

NOTES ON THE FUNCTION TABLE

Logic Levels: V_{IH} = TTL Logic 1 level
V_{IL} = TTL Logic 0 level
" - " = Logic "Do not care," V_{IH} or V_{IL}

Supply Voltage: V_{PP} = Programming / high-voltage
V_{CC} = Read / low-voltage
V_H = 12.0V ±0.5V

Read: Read mode: the content of the addressed memory byte is placed on the I/O pins O_0 to O_7

Output Disable: Device is selected (active mode), programming is disabled and O_0 to O_7 output buffers are tristated (PMOS and NMOS drivers turned-off)

Standby: Device is deselected, low power dissipation

Program: Byte programming mode: logic zeros in the bit pattern driving the O_0 to O_7 data input buffers are written into the respective memory cells of the addressed byte

Program Verify: Following a programming cycle, to verify the cell contents of the memory byte being programmed (not recommended as a normal read operation)

Program Inhibit: $\overline{CE}$ set to logic one and $\overline{OE}$ set to logic one prevents programming and deselects the device

Signature MFG: Signature mode with all other addresses at V_{IL}, code of IC manufacturer (Catalyst) output on I/O pins O_0 to O_7

Signature device: Signature mode with all other addresses at V_{IL}, code of IC type output on I/O pins O_0 to O_7

PIN CAPACITANCE

$T_A = 25^oC$, Freq = 1.0 MHz.

PARAMETER	TYPICAL	MAXIMUM	CONDITIONS
Input pin capacitance C_{IN}	4.0pF	6.0pF	V_{IN} = 0.0V
Output pin capacitance C_{OUT}	6.0pF	10.0pF	V_{OUT} = 0.0V
V_{PP} supply capacitance CV_{PP}		25.0pF	V_{PP} = 0.0V

ABSOLUTE MAXIMUM RATINGS

Temperature under bias	T_A	-10°C to +85°C
Storage temperature	Tstg	- 65°C to +125°C
All input/output voltages (except A_9)	V_{IN}, V_{OUT}	- 0.5V to V_{CC}+0.5V
Voltage on A_9		- 1.0V to +14.0V
Read supply voltage	V_{CC}	- 1.0V to +7.0V
Program voltage	V_{PP}	- 1.0V to +14.0V
Power dissipation, T_A = 25°C		1.0W
DC short-circuit current, output pin		20.0mA.
Max lead solder temp., 10 seconds		300°C

(Voltages with respect to ground)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SUPPLY CURRENT CHARACTERISTICS (AC and DC) (T_A = Commercial 0°C to 70°C)

Symbol	Parameter	Conditions	Standard	Limit
I_{CC}	V_{CC} active current (DC)	$\overline{OE}$ = $\overline{CE}$ = V_{IL}, V_{PP} = V_{CC} A_0 - A_{14} = V_{IL}	50mA	Max
I_{CC1}	V_{CC} active current (CMOS in @ 10MHz)	Inputs conform to V_{ILC} and V_{IHC}	60mA	Max
I_{CC2}	V_{CC} active current (TTL in @ 10MHz)	Inputs conform to AC test waveform (Fig. 1)	60mA	Max
I_{SB1}	V_{CC} standby current (CMOS in)	$\overline{CE}$ = V_{IHC}	40mA	Max
I_{SB2}	V_{CC} standby current (TTL in)	$\overline{CE}$ = V_{IH}	40mA	Max

DC CHARACTERISTICS <Read Operation> (V_{CC} = 5V ± 10%, T_A = Commercial 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Units
			Min.	Typ.	Max.	
I_{LI}	Input leakage current	V_{IN} = 5.5V	-	-	10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V	-	-	10	µA
I_{PP1}	V_{PP} leakage current	V_{PP} = 5.5V	-	-	10	µA
V_{IH}	Input high level TTL		2.0	-	V_{CC}+0.5	V
V_{IL}	Input low level TTL		-0.5	-	0.8	V
V_{OH}	Output voltage high level	I_{OH} = -1.0 mA	2.4	-	-	V
V_{OL}	Output voltage low level	I_{OL} = 4.0 mA	-	-	0.40	V
V_{ILC}	Input low level CMOS		-0.5	-	0.30	V
V_{IHC}	Input high level CMOS		V_{CC} -0.5	-	V_{CC} +0.5	V

NOTES:
- The maximum current values are with outputs O_0 to O_7 unloaded.
- V_{CC} must be applied simultaneously with or before V_{PP}, and removed simultaneously with or after V_{PP} .

AC CHARACTERISTICS <READ OPERATION>

(Temperature range: Commercial 0°C to 70°C)

Symbol	Parameter	V_{CC}±5%	27HC256-55/5		27HC256-70/5		27HC256-90/5		27HC256-120/5		Unit
		V_{CC}±10%	27HC256-55		27HC256-70		27HC256-90		27HC256-120		
			Min	Max	Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACC}	Address access time		-	55	-	70	-	90	-	120	ns
t_{CE}	$\overline{CE}$ to output delay		-	55	-	70	-	90	-	120	ns
t_{OE}	$\overline{OE}$ to output delay		-	30	-	35	-	40	-	50	ns
t_{OH} *	Output hold A, $\overline{OE}$, $\overline{CE}$		0	-	0	-	0	-	0	-	ns
t_{DF} *	$\overline{OE}$ high to out High-Z		0	30	0	35	0	40	0	50	ns

- Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer
- Input rise and fall times (10% to 90%) = 5ns
- Input pulse levels = 0.0V to 3.0 V
- Input and output timing reference = 0.8V and 2.0V

* These parameters are sampled and not 100% tested.

Fig. 1 AC Test Waveforms

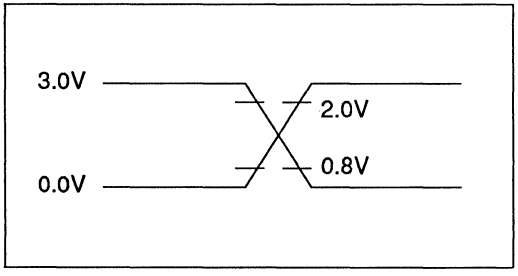
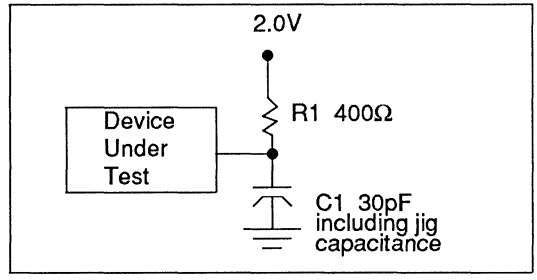
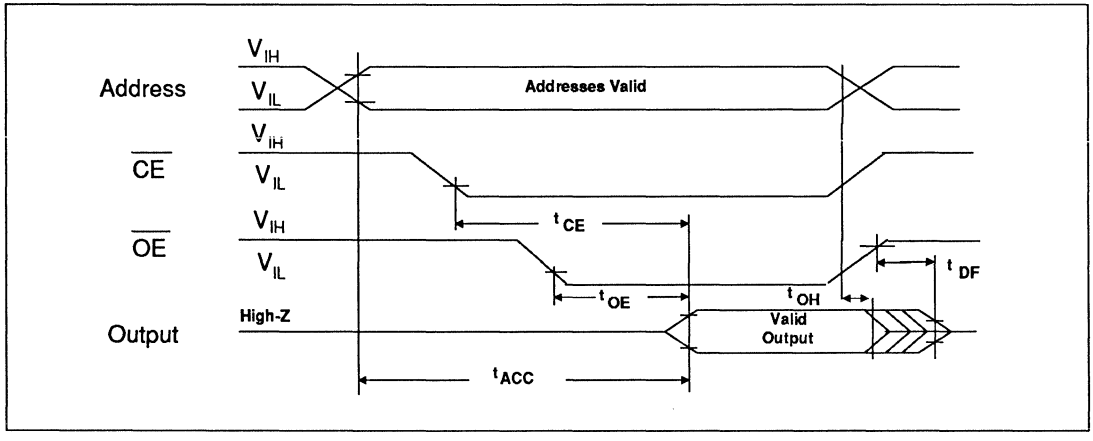


Fig. 2 Output Test Load



TIMING <Read Operation>



DC CHARACTERISTICS <Programming Operation>

$T_A = 25^oC \pm 5^oC$

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Low-voltage supply Quick Pulse algorithm	-	6	6.25	6.5	V
V_{CC}	Low-voltage supply Intelligent algorithm	-	5.75	6.0	6.25	V
V_{PP}	High-voltage supply Quick Pulse algorithm	-	12.50	12.75	13.0	V
V_{PP}	High-voltage supply Intelligent algorithm	-	12.0	12.5	13.0	V
I_{CCP}	V_{CC} supply current Program and Verify	-	-	-	80.0	mA
I_{PP}	V_{PP} supply current Program Operation	-	-	-	40.0	mA
I_{LI}	Input leakage current	V_{IN} = 5.25V	-	-	10.0	µA
I_{LO}	Output leakage current	V_{OUT} = 5.25V	-	-	10.0	µA
V_{IL}	Input Low-Level TTL	-	-0.50	-	0.80	V
V_{ILC}	Input Low-Level CMOS	-	-0.50	-	0.30	V
V_{OL}	Output Low-Level	I_{OL} = 4.0mA	-	-	0.40	V
V_{IH}	Input High-Level TTL	-	2.0	-	V_{CC}+0.50	V
V_{IHC}	Input High-Level CMOS	-	V_{CC}-0.50	-	V_{CC}+0.50	V
V_{OH}	Output High level	I_{OH} = -1.0 mA	2.4	-	-	V
V_H	High-Voltage INPUT for Signature Mode(s)	(See notes below)	11.5	-	12.50	V

NOTES:
- The maximum current values are with outputs O_0 to O_7 unloaded.
- V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

AC CHARACTERISTICS <Programming Operation>

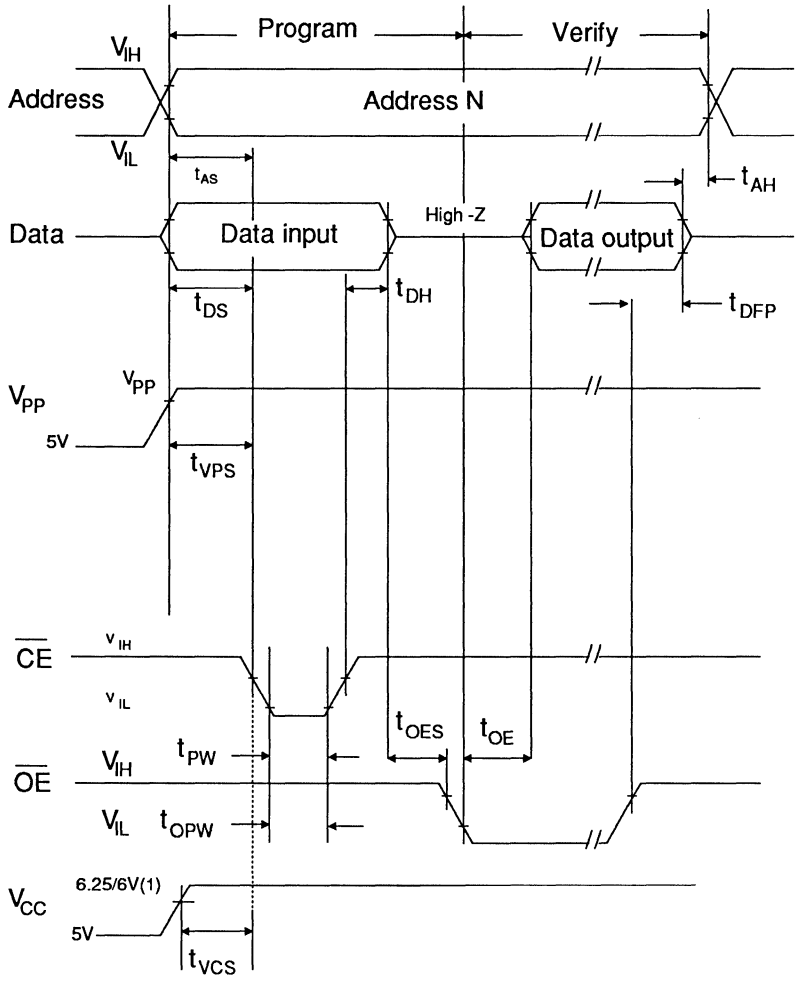
$T_A = 25°C \pm 5°C$

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{AS}	Address set-up time	-	2.0	-	-	µs
t_{OES}	$\overline{OE}$ set-up time	-	2.0	-	-	µs
t_{DS}	Data set-up time	-	2.0	-	-	µs
t_{AH}	Address hold time	-	0.0	-	-	µs
t_{DH}	Data hold time	-	2.0	-	-	µs
t_{VPS}	V_{PP} set-up time	-	2.0	-	-	µs
t_{VCS}	V_{CC} set-up time	-	2.0	-	-	µs
t_{PW}	$\overline{CE}$ pulse width Quick Pulse algorithm	-	95.0	100.0	105.0	µs
t_{PW}	$\overline{CE}$ pulse width Intelligent algorithm	-	0.95	1.0	1.05	ms
t_{OPW}	$\overline{CE}$ overprogram pulse width Intelligent algorithm	-	2.85	-	78.5	ms
t_{DFP}	$\overline{OE}$ high to Output High-Z	-	0.0	-	130	ns
t_{OE}	Data valid from $\overline{OE}$	-	-	-	150	ns

NOTES:
- Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer.
- Input Rise and Fall times (10% to 90%) = 20 ns.
- Input Pulse Levels = 0.0V to 3.0V.
- Input and Output Timing Reference = 0.80V and 2.0V.
- t_{DPF} is sampled and not 100% tested.

When programming the device a 0.1 microfarad capacitor is required between V_{PP} and V_{SS} to suppress spurious voltage transients which can damage the part.

TIMING <Programming Operation>



(1) Note: V_{CC} = 6.25V ±0.25V for Quick Pulse algorithm
6.0V ±0.25V for Intelligent Programming algorithm

Fig. 4 INTELLIGENT ALGORITHM

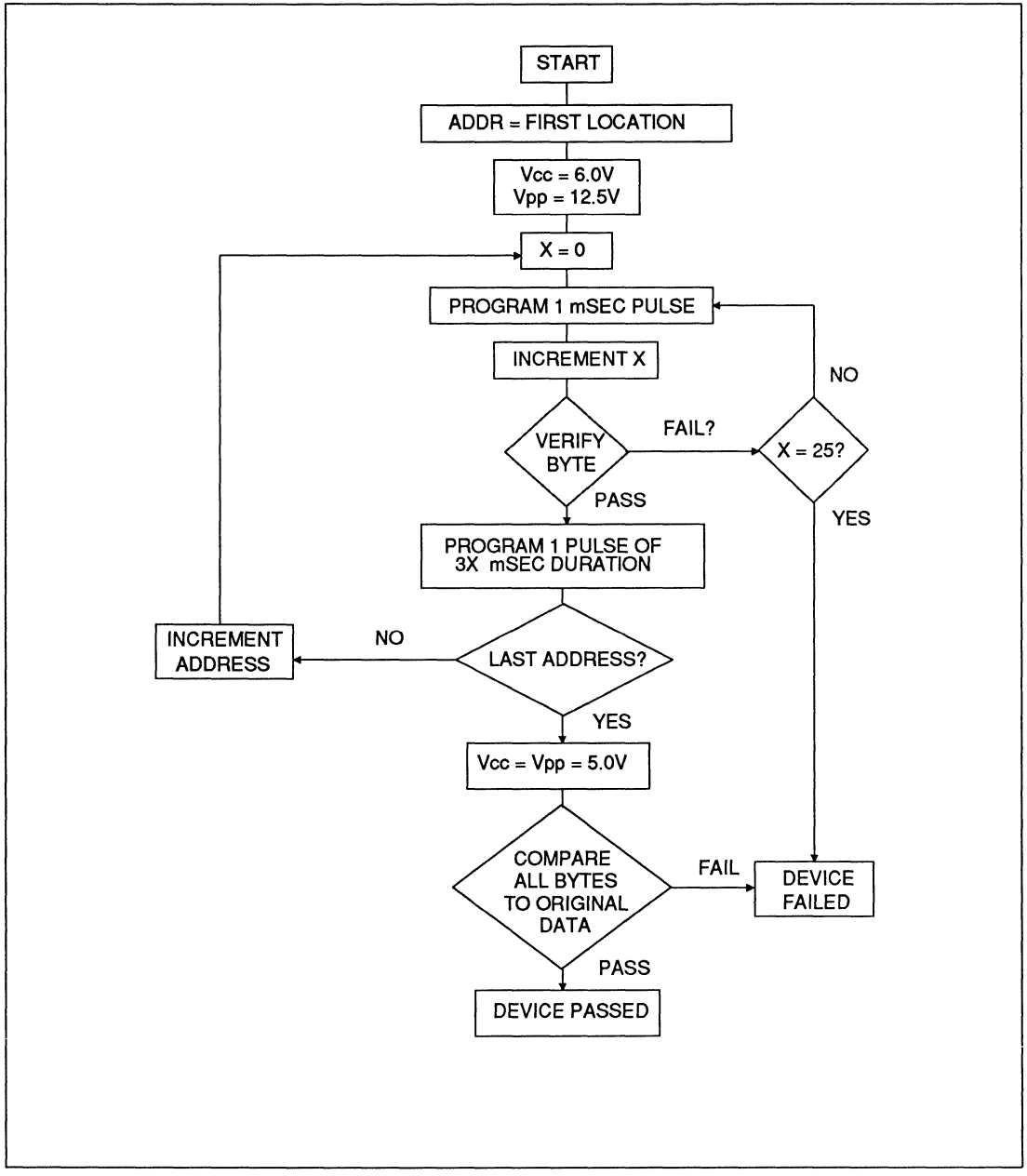
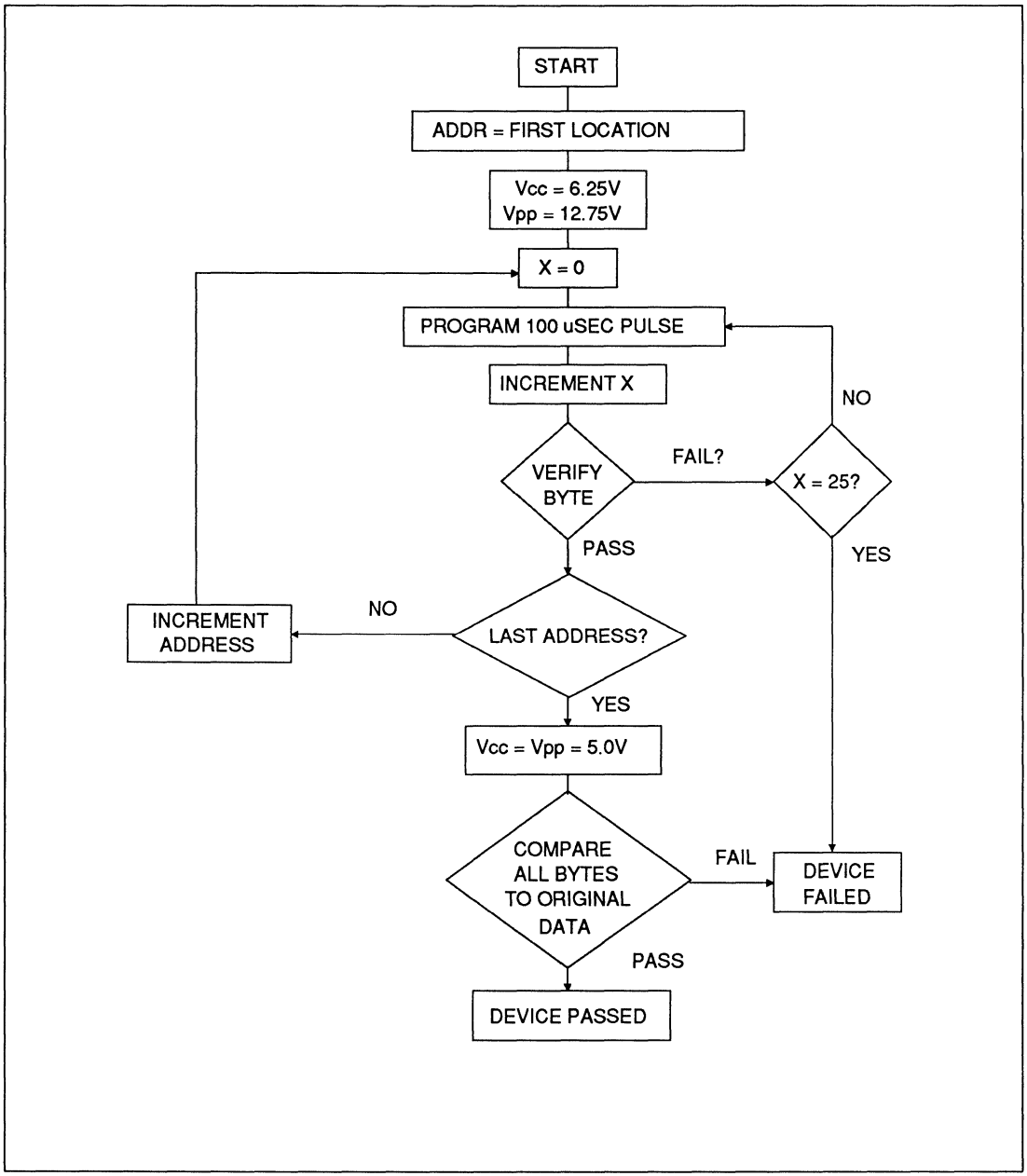


Fig. 5 QUICK PULSE ALGORITHM



READ OPERATION AND STANDBY MODES

Memory access for reading an address location is controlled by $\overline{CE}$ and $\overline{OE}$. Chip enable $\overline{CE}$ is used independently of all other input signals as the primary device selection. In the logic zero state (TTL level V_{IL}), $\overline{CE}$ powers up all inputs and enables internal circuitry. In the logic one state (CMOS level V_{IHC}) $\overline{CE}$ places the device in standby mode, all DC paths to ground are shut-off, and the power dissipation is reduced to a minimum. A logic one on Output Enable $\overline{OE}$ disables the output buffers and places the output pads in a high impedance state. Assuming that the address lines A_0 to A_{14} have been stable for a time equal to $T_{ACC} - T_{OE}$, the output data is available after a delay of T_{OE} from the falling edge of $\overline{OE}$.

SIGNATURE MODE

The Signature Mode allows one to identify the IC manufacturer and the type of the part. This mode is entered as a regular Read Mode by driving low the $\overline{CE}$ and $\overline{OE}$ inputs, and in addition driving the input address bit A_9 to high-voltage VH level with all other address lines at V_{IL}.

A V_{IL} on A_0 with all other addresses at V_{IL}, gives the binary code of the IC manufacturer on outputs O_0 to O_7.

CATALYST Code:
0 0 1 1 0 0 0 1 (31H)

A V_{IH} on A_0 with all other addresses at V_{IL}, gives the binary code of the device type on outputs O_0 to O_7.

27HC256 / 27HC256L Code:
0 1 0 0 0 0 0 0 (40H)

PROGRAMMING MODE

After a proper erasure operation, all bits of the EPROM are in the logic one state. The device is programmed by selectively writing logic zeros into the desired bit locations. The programming mode is entered by raising $\overline{CE}$ and $\overline{OE}$ to a high level and bringing the low voltage supply pin (V_{CC}), followed by the high voltage supply pin (V_{PP}), to their respective programming levels.

After the address inputs A_0 to A_{14} and data inputs O_0 to O_7 are stabilized, $\overline{CE}$ is switched from the logic one to logic zero state to perform the programming. The particular memory cells of the addressed byte, corresponding to the 0's of the input data bits, are then programmed.

A Program Verify cycle is performed after each byte is programmed to ensure that the zero bits have been correctly written. The byte verification cycle is initiated by keeping $\overline{CE}$ at V_{IH} and switching $\overline{OE}$ from V_{IH} to V_{IL}, while all other pin voltages remain unchanged. In most cases a single 100-microsecond programming cycle is sufficient to set a memory cell in the logic zero state. The Quick Pulse algorithm is recommended as the preferred device programming operation. The CAT27HC256 is also compatible with "Intelligent Programming."

The flow charts for both the algorithms are given in Fig.4 and Fig.5.

U.V. ERASURE OPERATION FOR CERDIP EPROMS

Direct exposure to fluorescent lamps such as those used in room light fixtures, can erase the CAT27HC256 EPROM in less than three years. When exposed to direct sun light the EPROM can be erased in less than a week.

The recommended erasure procedure is to expose the CAT27HC256 EPROM to a standard ultraviolet light with a wavelength of 2537 Angstroms. The integrated dose for proper erasure is 15 $Wsec/cm^2$. The erasure time with this dosage is approximately 15 to 60 minutes using an ultraviolet lamp with a 1200 $\mu W/cm^2$ power rating. The EPROM should be placed within 1 inch of the lamp tubes.

The maximum integrated dose a CAT27HC256 EPROM can be exposed to is 7258 $Wsec/cm^2$ (one week at 1200 $\mu W/cm^2$). Exposure of the device to higher U.V. doses may cause permanent damage and loss of functionality.

CAT27HC256L - Low Power

32,768 x 8-BIT HIGH-SPEED CMOS EPROM

Preliminary

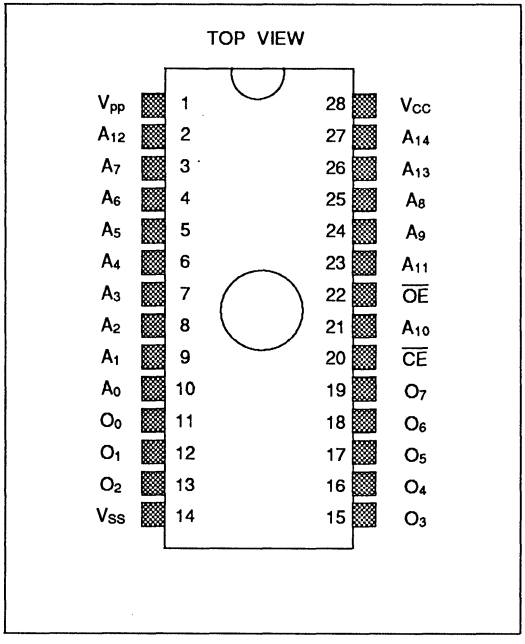
DESCRIPTION

The CAT27HC256L is a high speed 256K UV erasable and electrically reprogrammable EPROM ideally suited for high speed applications. Any byte can be accessed in less than 55ns, making this part compatible with high performance microprocessor systems by eliminating the need for speed-robbing wait states. The Quick Pulse algorithm reduces the time required to program this chip and ensures more reliable programming. The CAT27HC256L is used in applications where fast turnaround and pattern experimentation are important requirements. The CAT27HC256L is available in a 28-pin dual-in-line package with a transparent lid. This allows the user to expose the chip to ultraviolet light to erase the bit pattern, allowing a new pattern to be written into the device.

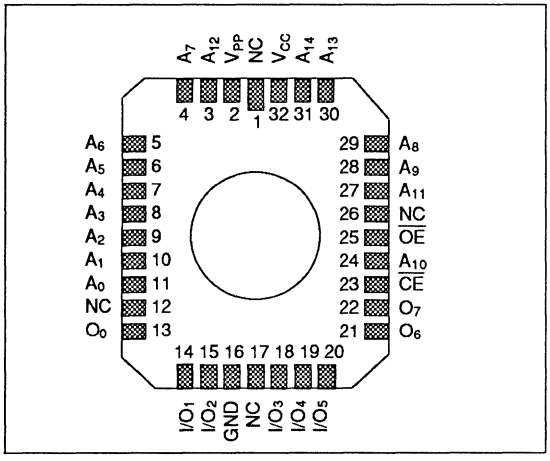
FEATURES

- Fast access time: 55/70/90/120 ns
- 5V single power supply - read mode
- 32,768 words x 8-bit configuration
- Low current requirements:
  - Active: 60mA max (CMOS levels)
  - Standby: 500µA (CMOS levels)
  - Standby: 2mA (TTL levels)
- High speed programming: 100µs/byte
- TTL compatible Input/Output
- 12.5V programming voltage
- JEDEC approved 28-pin DIP and 32-pin LCC
- Electronic signature
- Industrial and military temp. devices available

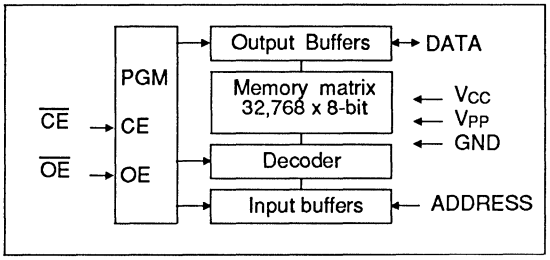
PIN CONFIGURATION 28-PIN DIP



PIN CONFIGURATION 32-PIN LCC



BLOCK DIAGRAM



FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	A_0 (10)	A_9 (24)	I/O
Read	V_{IL}	V_{IL}	V_{CC}	-	-	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{CC}	-	-	High Z
Stand-by	V_{IH}	-	V_{CC}	-	-	High Z
Program	V_{IL}	V_{IH}	V_{PP}	-	-	D_{IN}
Program verify	V_{IH}	V_{IL}	V_{PP}	-	-	D_{OUT}
Program inhibit	V_{IH}	V_{IH}	V_{PP}	-	-	High Z
Signature MFG.	V_{IL}	V_{IL}	V_{CC}	V_{IL}	V_H	31H
Signature device	V_{IL}	V_{IL}	V_{CC}	V_{IH}	V_H	40H

NOTES ON THE FUNCTION TABLE

Logic Levels: V_{IH} = TTL Logic 1 level
V_{IL} = TTL Logic 0 level
" - " = Logic "Do not care," V_{IH} or V_{IL}

Supply Voltage: V_{PP} = Programming / high-voltage
V_{CC} = Read / low-voltage
V_H = 12.0V ±0.5V

Read: Read mode: the content of the addressed memory byte is placed on the I/O pins O_0 to O_7

Output Disable: Device is selected (active mode), programming is disabled and O_0 to O_7 output buffers are tristated (PMOS and NMOS drivers turned-off)

Standby: Device is deselected, low power dissipation

Program: Byte programming mode: logic zeros in the bit pattern driving the O_0 to O_7 data input buffers are written into the respective memory cells of the addressed byte

Program Verify: Following a programming cycle, to verify the cell contents of the memory byte being programmed (not recommended as a normal read operation)

Program Inhibit: $\overline{CE}$ set to logic one and $\overline{OE}$ set to logic one prevents programming and deselects the device

Signature MFG: Signature mode with all other addresses at V_{IL}, code of IC manufacturer (Catalyst) output on I/O pins O_0 to O_7

Signature device: Signature mode with all other addresses at V_{IL}, code of IC type output on I/O pins O_0 to O_7

PIN CAPACITANCE
(T_A = 25°C, Freq = 1.0MHz)

PARAMETER	TYPICAL	MAXIMUM	CONDITIONS
Input pin capacitance C_{IN}	4.0pF	6.0pF	V_{IN} = 0.0V
Output pin capacitance C_{OUT}	6.0pF	10.0pF	V_{OUT} = 0.0V
V_{PP} supply capacitance CV_{PP}		25.0pF	V_{PP} = 0.0V

ABSOLUTE MAXIMUM RATINGS

Temperature under bias	T_A	-10°C to +85°C
Storage temperature	Tstg	- 65°C to +125°C
All input/output voltages (except A_9)	V_{IN}, V_{OUT}	- 0.5V to V_{CC}+0.5V
Voltage on A_9		- 1.0V to +14.0V
Read supply voltage	V_{CC}	- 1.0V to +7.0V
Program voltage	V_{PP}	- 1.0V to +14.0V
Power dissipation, T_A = 25°C		1.0W
DC short-circuit current, output pin		20.0mA.
Max lead solder temp., 10 seconds		300°C

(Voltages with respect to ground)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SUPPLY CURRENT CHARACTERISTICS (AC and DC) (T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Low Power	Limit
I_{CC}	V_{CC} active current (DC)	$\overline{OE}$ = $\overline{CE}$ = V_{IL}, V_{PP} = V_{CC} A_0 - A_{14} = V_{IL}	30mA	Max
I_{CC1}	V_{CC} active current (CMOS in @ 10MHz)	Inputs conform to V_{ILC} and V_{IHC}	60mA	Max
I_{CC2}	V_{CC} active current (TTL in @ 10MHz)	Inputs conform to AC test waveform (Fig. 1)	60mA	Max
I_{SB1}	V_{CC} standby current (CMOS in)	$\overline{CE}$ = V_{IHC}	500µA	Max
I_{SB2}	V_{CC} standby current (TTL in)	$\overline{CE}$ = V_{IH}	2mA	Max

DC CHARACTERISTICS <Read Operation> (V_{CC} = 5V ± 10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Units
			Min.	Typ.	Max.	
I_{LI}	Input leakage current	V_{IN} = 5.5V	-	-	10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V	-	-	10	µA
I_{PP1}	V_{PP} leakage current	V_{PP} = 5.5V	-	-	10	µA
V_{IH}	Input high level TTL		2.0	-	V_{CC}+0.5	V
V_{IL}	Input low level TTL		-0.5	-	0.8	V
V_{OH}	Output voltage high level	I_{OH} = -1.0 mA	2.4	-	-	V
V_{OL}	Output voltage low level	I_{OL} = 4.0 mA	-	-	0.40	V
V_{ILC}	Input low level CMOS		-0.5	-	0.30	V
V_{IHC}	Input high level CMOS		V_{CC} -0.5	-	V_{CC} +0.5	V

NOTES:
- The maximum current values are with outputs O_0 to O_7 unloaded.
- V_{CC} must be applied simultaneously with or before V_{PP}, and removed simultaneously with or after V_{PP} .

AC CHARACTERISTICS <READ OPERATION>

(Temperature range: 0°C to 70°C)

Symbol	Parameter	V_{CC}±5%	27HC256-55/5		27HC256-70/5		27HC256-90/5		27HC256-120/5		Unit
		V_{CC}±10%	27HC256-55		27HC256-70		27HC256-90		27HC256-120		
			Min	Max	Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACC}	Address access time		-	55	-	70	-	90	-	120	ns
t_{CE}	$\overline{CE}$ to output delay		-	55	-	70	-	90	-	120	ns
t_{OE}	$\overline{OE}$ to output delay		-	30	-	35	-	40	-	50	ns
t_{OH} *	Output hold A, $\overline{OE}$, $\overline{CE}$		0	-	0	-	0	-	0	-	ns
t_{DF} *	$\overline{OE}$ high to out High-Z		0	30	0	35	0	40	0	50	ns

- Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer
- Input rise and fall times (10% to 90%) = 5ns
- Input pulse levels = 0.0V to 3.0 V
- Input and output timing reference = 0.8V and 2.0V

* These parameters are sampled and not 100% tested.

Fig. 1 AC Test Waveforms

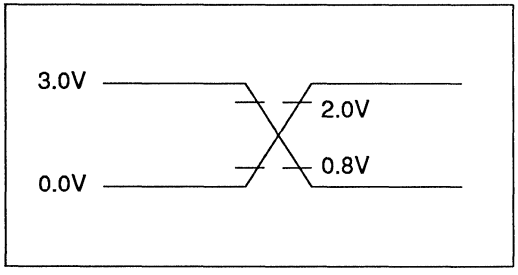
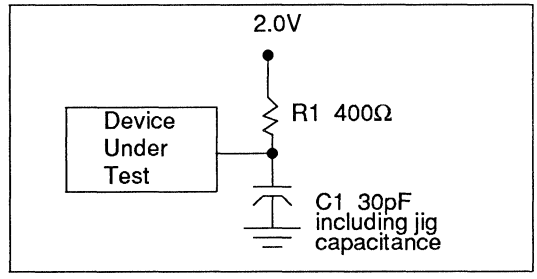
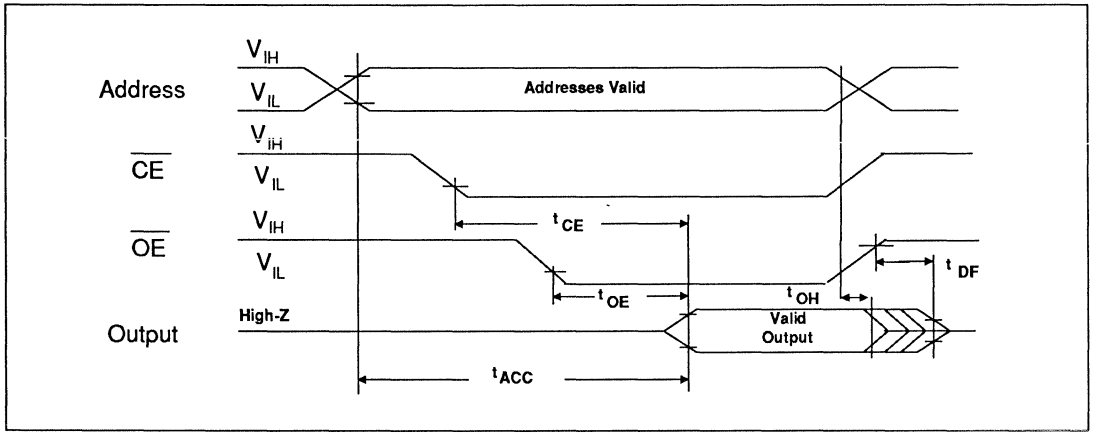


Fig. 2 Output Test Load



TIMING <Read Operation>



DC CHARACTERISTICS <Programming Operation>

$T_A = 25°C \pm 5°C$

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Low-voltage supply Quick Pulse algorithm	-	6	6.25	6.5	V
V_{CC}	Low-voltage supply Intelligent algorithm	-	5.75	6.0	6.25	V
V_{PP}	High-voltage supply Quick Pulse algorithm	-	12.50	12.75	13.0	V
V_{PP}	High-voltage supply Intelligent algorithm	-	12.0	12.5	13.0	V
I_{CCP}	V_{CC} supply current Program and Verify	-	-	-	80.0	mA
I_{PP}	V_{PP} supply current Program Operation	-	-	-	40.0	mA
I_{LI}	Input leakage current	V_{IN} = 5.25V	-	-	10.0	µA
I_{LO}	Output leakage current	V_{OUT} = 5.25V	-	-	10.0	µA
V_{IL}	Input Low-Level TTL	-	-0.50	-	0.80	V
V_{ILC}	Input Low-Level CMOS	-	-0.50	-	0.30	V
V_{OL}	Output Low-Level	I_{OL} = 4.0mA	-	-	0.40	V
V_{IH}	Input High-Level TTL	-	2.0	-	V_{CC}+0.50	V
V_{IHC}	Input High-Level CMOS	-	V_{CC}-0.50	-	V_{CC}+0.50	V
V_{OH}	Output High level	I_{OH} = -1.0 mA	2.4	-	-	V
V_H	High-Voltage INPUT for Signature Mode(s)	(See notes below)	11.5	-	12.50	V

NOTES:
- The maximum current values are with outputs O_0 to O_7 unloaded.
- V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

AC CHARACTERISTICS <Programming Operation>

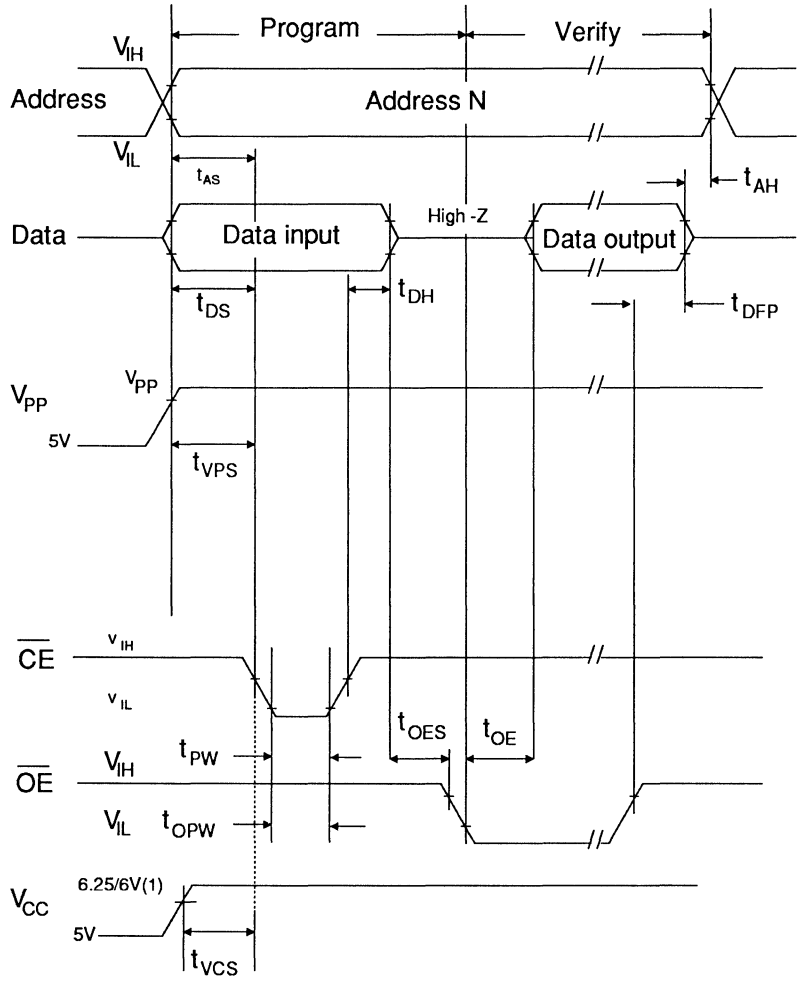
$T_A = 25^oC \pm 5^oC$

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{AS}	Address set-up time	-	2.0	-	-	µs
t_{OES}	$\overline{OE}$ set-up time	-	2.0	-	-	µs
t_{DS}	Data set-up time	-	2.0	-	-	µs
t_{AH}	Address hold time	-	0.0	-	-	µs
t_{DH}	Data hold time	-	2.0	-	-	µs
t_{VPS}	V_{PP} set-up time	-	2.0	-	-	µs
t_{VCS}	V_{CC} set-up time	-	2.0	-	-	µs
t_{PW}	$\overline{CE}$ pulse width Quick Pulse algorithm	-	95.0	100.0	105.0	µs
t_{PW}	$\overline{CE}$ pulse width Intelligent algorithm	-	0.95	1.0	1.05	ms
t_{OPW}	$\overline{CE}$ overprogram pulse width Intelligent algorithm	-	2.85	-	78.5	ms
t_{DFP}	$\overline{OE}$ high to Output High-Z	-	0.0	-	130	ns
t_{OE}	Data valid from $\overline{OE}$	-	-	-	150	ns

NOTES:
- Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer.
- Input Rise and Fall times (10% to 90%) = 20 ns.
- Input Pulse Levels = 0.0V to 3.0V.
- Input and Output Timing Reference = 0.80V and 2.0V.
- t_{DPF} is sampled and not 100% tested.

When programming the device a 0.1 microfarad capacitor is required between V_{PP} and V_{SS} to suppress spurious voltage transients which can damage the part.

TIMING <Programming Operation>



(1) Note: V_{CC} = 6.25V ±0.25V for Quick Pulse algorithm
6.00V ±0.25V for Intelligent Programming algorithm

Fig. 4 INTELLIGENT ALGORITHM

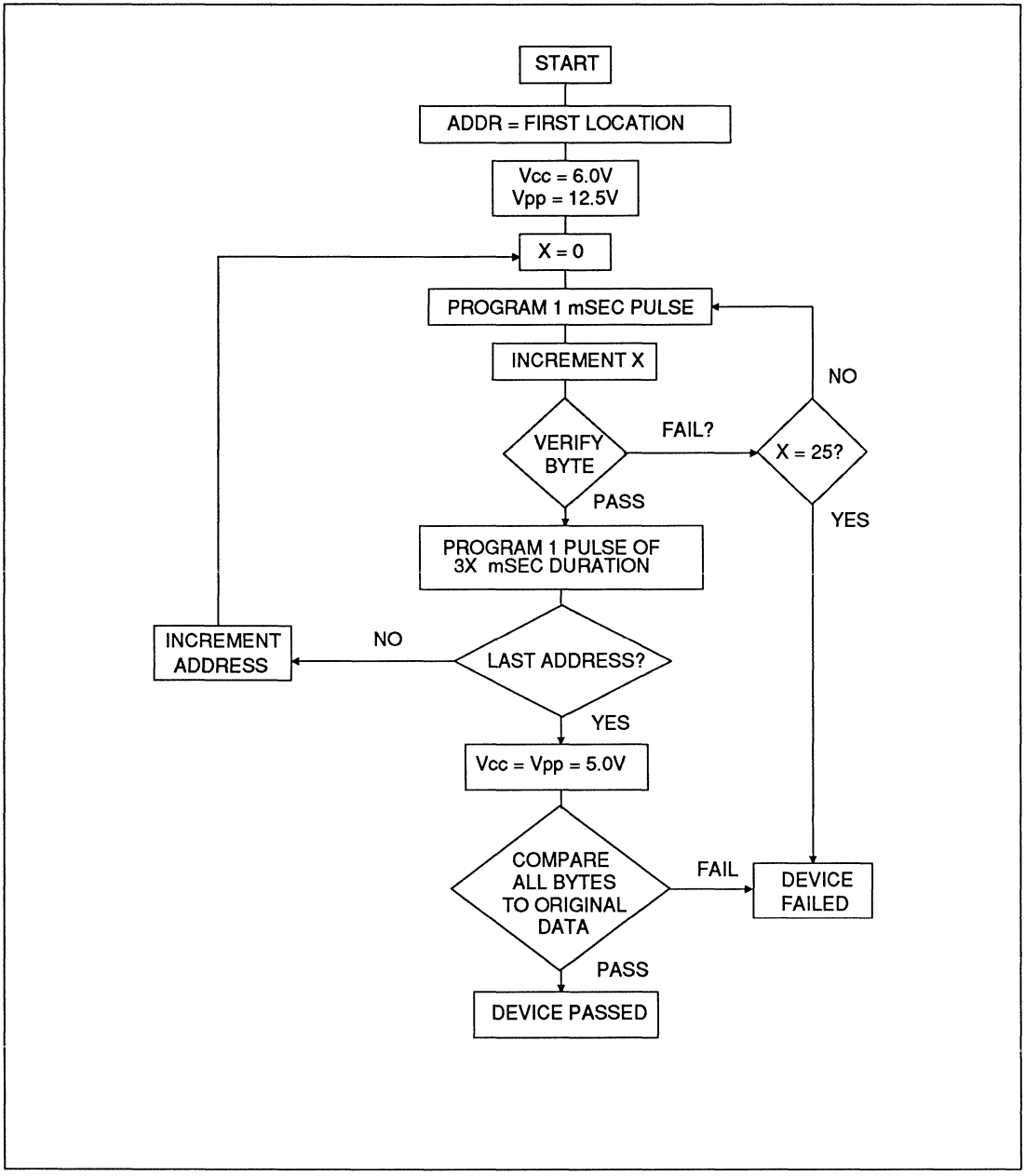
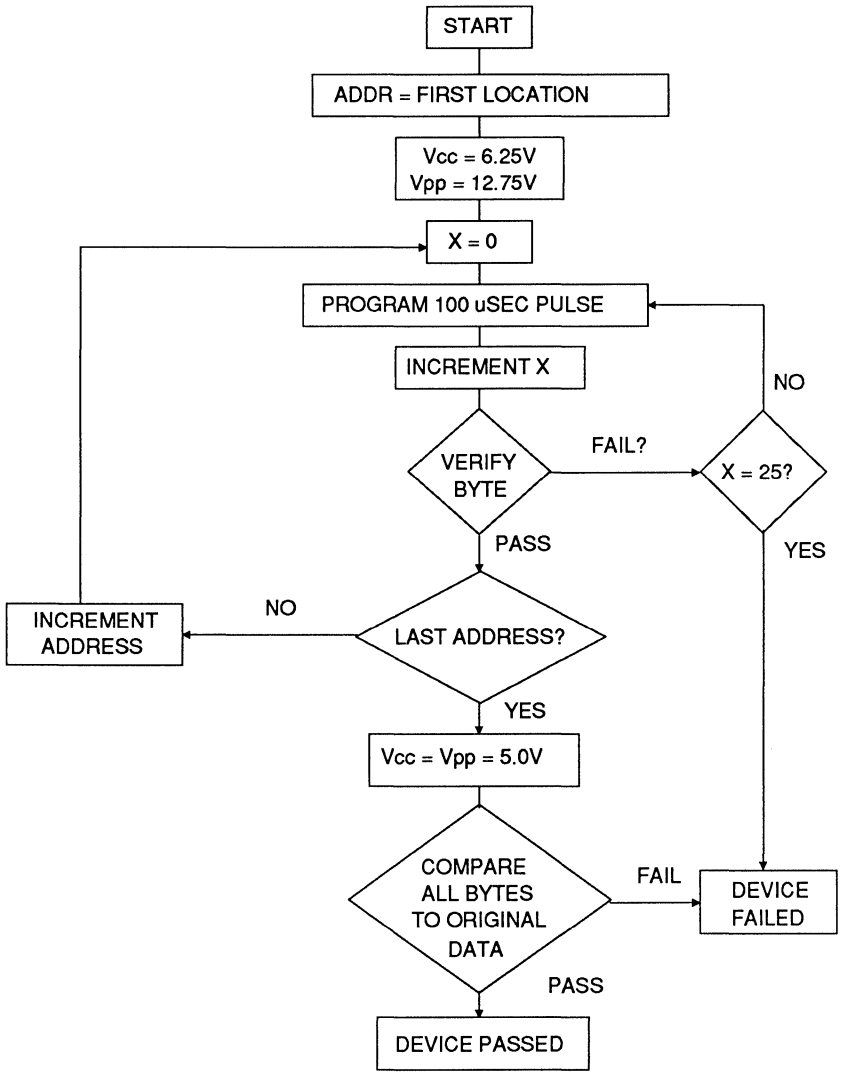


Fig. 5 QUICK PULSE ALGORITHM



READ OPERATION AND STANDBY MODES

Memory access for reading an address location is controlled by $\overline{CE}$ and $\overline{OE}$. Chip enable $\overline{CE}$ is used independently of all other input signals as the primary device selection. In the logic zero state (TTL level V_{IL}), $\overline{CE}$ powers up all inputs and enables internal circuitry. In the logic one state (CMOS level V_{IHC}) $\overline{CE}$ places the device in standby mode, all DC paths to ground are shut-off, and the power dissipation is reduced to a minimum. A logic one on Output Enable $\overline{OE}$ disables the output buffers and places the output pads in a high impedance state. Assuming that the address lines A_0 to A_{14} have been stable for a time equal to T_{ACC} - T_{OE}, the output data is available after a delay of T_{OE} from the falling edge of $\overline{OE}$.

SIGNATURE MODE

The Signature Mode allows one to identify the IC manufacturer and the type of the part. This mode is entered as a regular Read Mode by driving low the $\overline{CE}$ and $\overline{OE}$ inputs, and in addition driving the input address bit A_9 to high-voltage VH level with all other address lines at V_{IL}.

A V_{IL} on A_0 with all other addresses at V_{IL}, gives the binary code of the IC manufacturer on outputs O_0 to O_7.

CATALYST Code:
0 0 1 1 0 0 0 1 (31H)

A V_{IH} on A_0 with all other addresses at V_{IL}, gives the binary code of the device type on outputs O_0 to O_7.

27HC256 / 27HC256L Code:
0 1 0 0 0 0 0 0 (40H)

PROGRAMMING MODE

After a proper erasure operation, all bits of the EPROM are in the logic one state. The device is programmed by selectively writing logic zeros into the desired bit locations. The programming mode is entered by raising $\overline{CE}$ and $\overline{OE}$ to a high level and bringing the low voltage supply pin (V_{CC}), followed by the high voltage supply pin (V_{PP}), to their respective programming levels.

After the address inputs A_0 to A_{14} and data inputs O_0 to O_7 are stabilized, $\overline{CE}$ is switched from the logic one to logic zero state to perform the programming. The particular memory cells of the addressed byte, corresponding to the 0's of the input data bits, are then programmed.

A Program Verify cycle is performed after each byte is programmed to ensure that the zero bits have been correctly written. The byte verification cycle is initiated by keeping $\overline{CE}$ at V_{IH} and switching $\overline{OE}$ from V_{IH} to V_{IL}, while all other pin voltages remain unchanged. In most cases a single 100-microsecond programming cycle is sufficient to set a memory cell in the logic zero state. The Quick Pulse algorithm is recommended as the preferred device programming operation. The CAT27HC256 is also compatible with "Intelligent Programming."

The flow charts for both the algorithms are given in Fig.4 and Fig.5.

U.V. ERASURE OPERATION FOR CERDIP EPROMS

Direct exposure to fluorescent lamps such as those used in room light fixtures, can erase the CAT27HC256 EPROM in less than three years. When exposed to direct sun light the EPROM can be erased in less than a week.

The recommended erasure procedure is to expose the CAT27HC256 EPROM to a standard ultraviolet light with a wavelength of 2537 Angstroms. The integrated dose for proper erasure is 15 $Wsec/cm^2$. The erasure time with this dosage is approximately 15 to 60 minutes using an ultraviolet lamp with a 1200 $\mu W/cm^2$ power rating. The EPROM should be placed within 1 inch of the lamp tubes.

The maximum integrated dose a CAT27HC256 EPROM can be exposed to is 7258 $Wsec/cm^2$ (one week at 1200 $\mu W/cm^2$). Exposure of the device to higher U.V. doses may cause permanent damage and loss of functionality.

CAT27HC256I - Industrial Temperature

32,768 x 8-BIT HIGH-SPEED CMOS EPROM

Preliminary

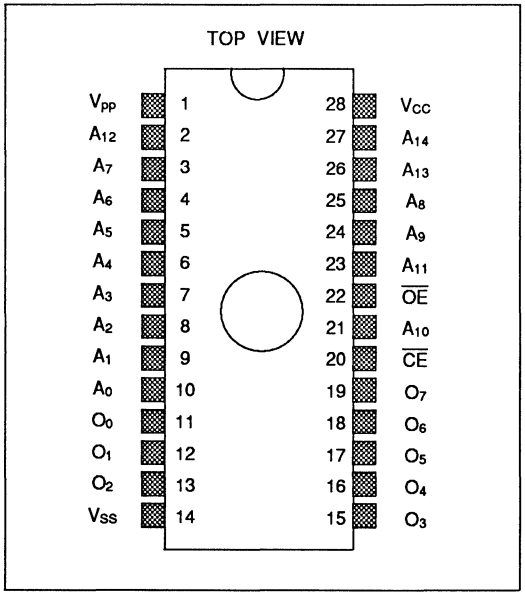
DESCRIPTION

The CAT27HC256I is a high speed 256K UV erasable and electrically reprogrammable EPROM ideally suited for high speed applications. Any byte can be accessed in less than 55ns making this part compatible with high performance microprocessor systems by eliminating the need for speed-robbing wait states. The Quick Pulse algorithm reduces the time required to program this chip and ensures more reliable programming. The CAT27HC256I is used in applications where fast turnaround and pattern experimentation are important requirements. The CAT27HC256I is available in a 28-pin dual-in-line package with a transparent lid. This allows the user to expose the chip to ultraviolet light to erase the bit pattern, allowing a new pattern to be written into the device.

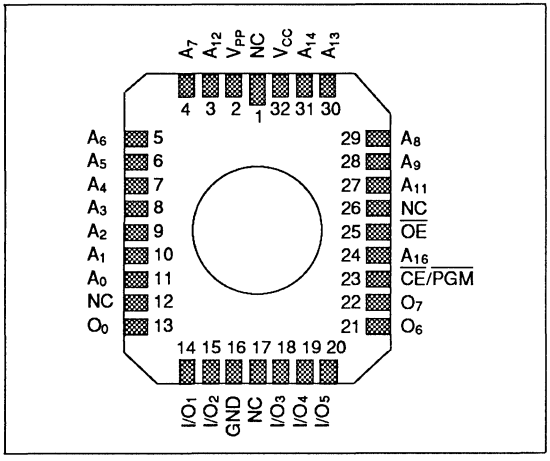
FEATURES

- Fast access time: 55/70/90/120ns
- 5V single power supply - read mode
- Low current requirements:
  - Active: 80mA max (CMOS levels)
  - Standby: 1mA max (CMOS levels)
- High speed programming: 100µs/byte
- TTL compatible Input/Output
- 12.5V programming voltage
- JEDEC approved 28-pin DIP and 32-pin LCC
- Electronic signature

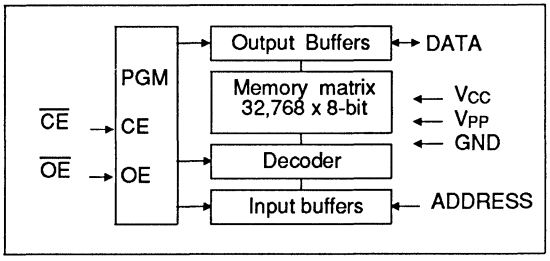
PIN CONFIGURATION 28-PIN DIP



PIN CONFIGURATION 32-PIN LCC



BLOCK DIAGRAM



FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	A_0 (10)	A_9 (24)	I/O
Read	V_{IL}	V_{IL}	V_{CC}	-	-	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{CC}	-	-	High-Z
Standby	V_{IH}	-	V_{CC}	-	-	High-Z
Program	V_{IL}	V_{IH}	V_{PP}	-	-	D_{IN}
Program verify	V_{IH}	V_{IL}	V_{PP}	-	-	D_{OUT}
Program inhibit	V_{IH}	V_{IH}	V_{PP}	-	-	High-Z
Signature MFG.	V_{IL}	V_{IL}	V_{CC}	V_{IL}	V_H	31H
Signature device	V_{IL}	V_{IL}	V_{CC}	V_{IH}	V_H	40H

NOTES ON THE FUNCTION TABLE

Logic Levels: V_{IH} = TTL Logic 1 level
V_{IL} = TTL Logic 0 level
" - " = Logic "Do not care," V_{IH} or V_{IL}

Supply Voltage: V_{PP} = Programming / high-voltage
V_{CC} = Read / low-voltage
V_H = 12.0V ±0.5V

Read: Read mode: the content of the addressed memory byte is placed on the I/O pins O_0 to O_7

Output Disable: Device is selected (active mode), programming is disabled and O_0 to O_7 output buffers are tristated (PMOS and NMOS drivers turned-off)

Standby: Device is deselected, low power dissipation

Program: Byte programming mode: logic zeros in the bit pattern driving the O_0 to O_7 data input buffers are written into the respective memory cells of the addressed byte

Program Verify: Following a programming cycle, to verify the cell contents of the memory byte being programmed (not recommended as a normal read operation)

Program Inhibit: $\overline{CE}$ set to logic one and $\overline{OE}$ set to logic one prevents programming and deselects the device

Signature MFG: Signature mode with all other addresses at V_{IL}, code of IC manufacturer (Catalyst) output on I/O pins O_0 to O_7

Signature device: Signature mode with all other addresses at V_{IL}, code of IC type output on I/O pins O_0 to O_7

PIN CAPACITANCE
(T_A = 25°C, Freq = 1.0MHz)

PARAMETER	TYPICAL	MAXIMUM	CONDITIONS
Input pin capacitance C_{IN}	4.0pF	6.0pF	V_{IN} = 0.0V
Output pin capacitance C_{OUT}	6.0pF	10.0pF	V_{OUT} = 0.0V
V_{PP} supply capacitance CV_{PP}		25.0pF	V_{PP} = 0.0V

ABSOLUTE MAXIMUM RATINGS

Temperature under bias	- 65°C to +135°C
Storage temperature	- 65°C to +135°C
All input/output voltages (except A_9)	- 0.5V to V_{CC}+0.5V
Voltage on A_9	- 1.0V to +14.0 V
Read supply voltage	- 1.0V to +7.0 V
Program voltage	- 1.0V to +14.0 V
Power dissipation, T_A = 25°C	1.0 W
DC short-circuit current, output pin	20.0 mA
Max lead solder temp., 10 seconds	300°C

(Voltages with respect to ground)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SUPPLY CURRENT CHARACTERISTICS (AC and DC)

(T_A = Industrial -40°C to 85°C)

Symbol	Parameter	Conditions	Standard	Limit
I_{CC}	V_{CC} active current (DC)	$\overline{OE} = \overline{CE} = V_{IL}$, $V_{PP} = V_{CC}$ $A_0 - A_{14} = V_{IL}$	55mA	Max.
I_{CC1}	V_{CC} active current (CMOS in @ 10MHz)	Inputs conform to V_{ILC} and V_{IHC}	80mA	Max.
I_{CC2}	V_{CC} active current (TTL in @ 10MHz)	Inputs conform to AC test waveform (Fig. 1)	80mA	Max.
I_{SB1}	V_{CC} standby current (CMOS in)	$\overline{CE} = V_{IHC}$	45mA	Max.
I_{SB2}	V_{CC} standby current (TTL in)	$\overline{CE} = V_{IH}$	45mA	Max.

DC CHARACTERISTICS <Read Operation>

(V_{CC} = 5V ± 10%, T_A = Industrial -40°C to 85°C)

Symbol	Parameter	Conditions	Limits			Units
			Min.	Typ.	Max.	
I_{LI}	Input leakage current	V_{IN} = 5.5V	-	-	10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V	-	-	10	µA
I_{PP1}	V_{PP} leakage current	V_{PP} = 5.5V	-	-	10	µA
V_{IH}	Input high level TTL		2.0	-	V_{CC}+0.5	V
V_{IL}	Input low level TTL		-0.5	-	0.8	V
V_{OH}	Output voltage high level	I_{OH} = -1.0 mA	2.4	-	-	V
V_{OL}	Output voltage low level	I_{OL} = 4.0 mA	-	-	0.40	V
V_{ILC}	Input low level CMOS		-0.5	-	0.30	V
V_{IHC}	Input high level CMOS		V_{CC} -0.5	-	V_{CC} +0.5	V

NOTES:
- The maximum current values are with outputs O_0 to O_7 unloaded.
- V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} .

AC CHARACTERISTICS <READ OPERATION>

(Temperature range: Industrial -40°C to 85°C)

Symbol	Parameter	V_{CC}±5%	27HC256-55/5		27HC256-70/5		27HC256-90/5		27HC256-120/5		Unit
		V_{CC}±10%	NOTE 1		27HC256-70		27HC256-90		27HC256-120		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACC}	Address access time		-	55	-	70	-	90	-	120	ns
t_{CE}	$\overline{CE}$ to output delay		-	55	-	70	-	90	-	120	ns
t_{OE}	$\overline{OE}$ to output delay		-	30	-	35	-	40	-	50	ns
t_{OH} *	Output hold A, $\overline{OE}$, $\overline{CE}$		0	-	0	-	0	-	0	-	ns
t_{DF} *	$\overline{OE}$ high to out High-Z		0	30	0	35	0	40	0	50	ns

- Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer
- Input rise and fall times (10% to 90%) = 5ns
- Input pulse levels = 0.0V to 3.0V
- Input and output timing reference = 0.8V and 2.0V

* These parameters are sampled and not 100% tested.

NOTE 1. The 55ns version is not currently available in military, low power or V_{CC} = ±10%

Fig. 1 AC Test Waveforms

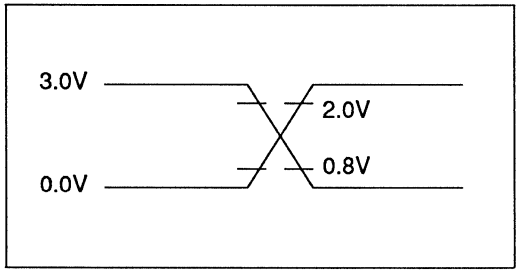
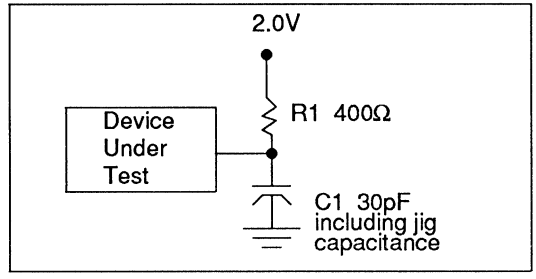
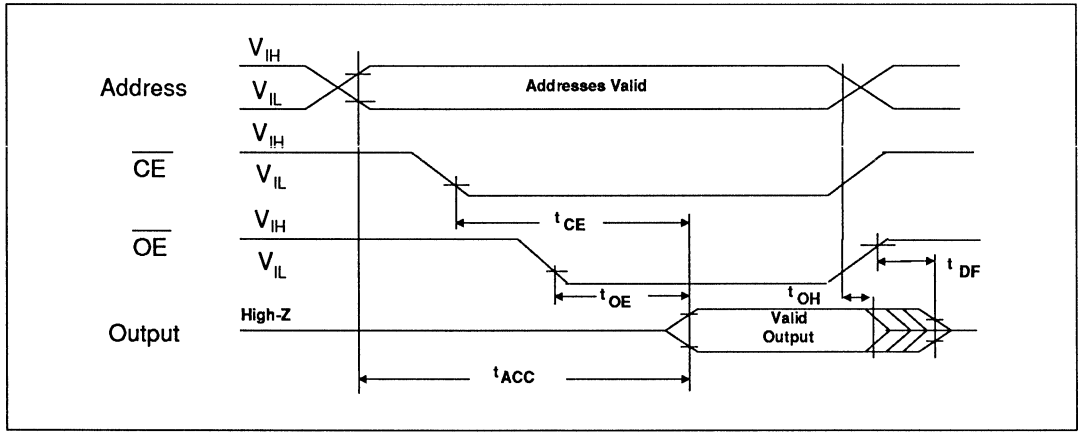


Fig. 2 Output Test Load



TIMING <Read Operation>



DC CHARACTERISTICS <Programming Operation>

(T_A = 25°C ± 5°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Low-voltage supply Quick Pulse algorithm	-	6	6.25	6.5	V
V_{CC}	Low-voltage supply Intelligent algorithm	-	5.75	6.0	6.25	V
V_{PP}	High-voltage supply Quick Pulse algorithm	-	12.50	12.75	13.0	V
V_{PP}	High-voltage supply Intelligent algorithm	-	12.0	12.5	13.0	V
I_{CCP}	V_{CC} supply current Program and Verify	-	-	-	45.0	mA
I_{PP}	V_{PP} supply current Program Operation	-	-	-	40.0	mA
I_{LI}	Input leakage current	V_{IN} = 5.25V	-	-	10.0	µA
I_{LO}	Output leakage current	V_{OUT} = 5.25V	-	-	10.0	µA
V_{IL}	Input Low-Level TTL	-	-0.50	-	0.80	V
V_{ILC}	Input Low-Level CMOS	-	-0.50	-	0.30	V
V_{OL}	Output Low-Level	I_{OL} = 4.0mA	-	-	0.40	V
V_{IH}	Input High-Level TTL	-	2.0	-	V_{CC}+0.50	V
V_{IHC}	Input High-Level CMOS	-	V_{CC}-0.50	-	V_{CC}+0.50	V
V_{OH}	Output High level	I_{OH} = -1.0mA	2.4	-	-	V
V_H	High-Voltage INPUT for Signature Mode(s)	(See notes below)	11.5	-	12.50	V

NOTES:

- The maximum current values are with outputs O_0 to O_7 unloaded.
- V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

AC CHARACTERISTICS <Programming Operation>

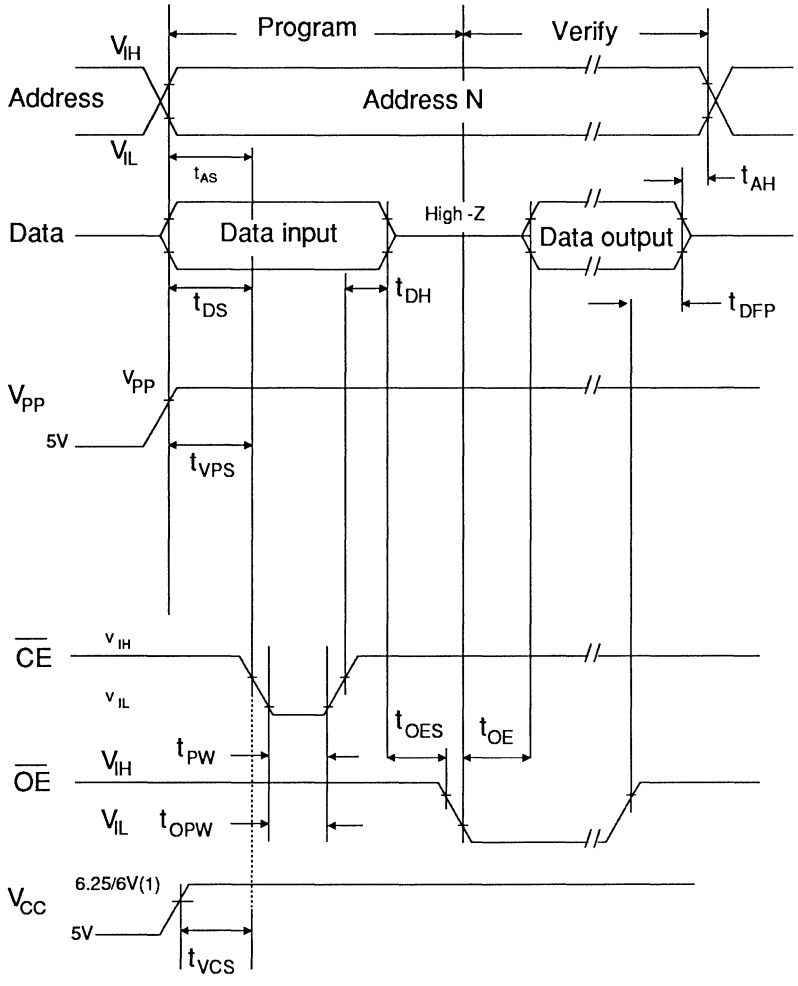
(T_A = 25°C ±5°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{AS}	Address set-up time	-	2.0	-	-	µs
t_{OES}	$\overline{OE}$ set-up time	-	2.0	-	-	µs
t_{DS}	Data set-up time	-	2.0	-	-	µs
t_{AH}	Address hold time	-	0.0	-	-	µs
t_{DH}	Data hold time	-	2.0	-	-	µs
t_{VPS}	V_{PP} set-up time	-	2.0	-	-	µs
t_{VCS}	V_{CC} set-up time	-	2.0	-	-	µs
t_{PW}	$\overline{CE}$ pulse width Quick Pulse algorithm	-	95.0	100.0	105.0	µs
t_{PW}	$\overline{CE}$ pulse width Intelligent algorithm	-	0.95	1.0	1.05	ms
t_{OPW}	$\overline{CE}$ overprogram pulse width Intelligent algorithm	-	2.85	-	78.5	ms
t_{DFP}	$\overline{OE}$ high to Output High-Z	-	0.0	-	130	ns
t_{OE}	Data valid from $\overline{OE}$	-	-	-	150	ns

NOTES:
- Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer.
- Input Rise and Fall times (10% to 90%) = 20ns.
- Input Pulse Levels = 0.0V to 3.0V.
- Input and Output Timing Reference = 0.80V and 2.0V.
- t_{DPF} is sampled and not 100% tested.

When programming the device a 0.1 microfarad capacitor is required between V_{PP} and V_{SS} to suppress spurious voltage transients which can damage the part.

TIMING <Programming Operation>



(1) Note: V_{CC} = 6.25V ±0.25V for Quick Pulse algorithm
6.00V ±0.25V for Intelligent Programming algorithm

Fig. 4 INTELLIGENT ALGORITHM

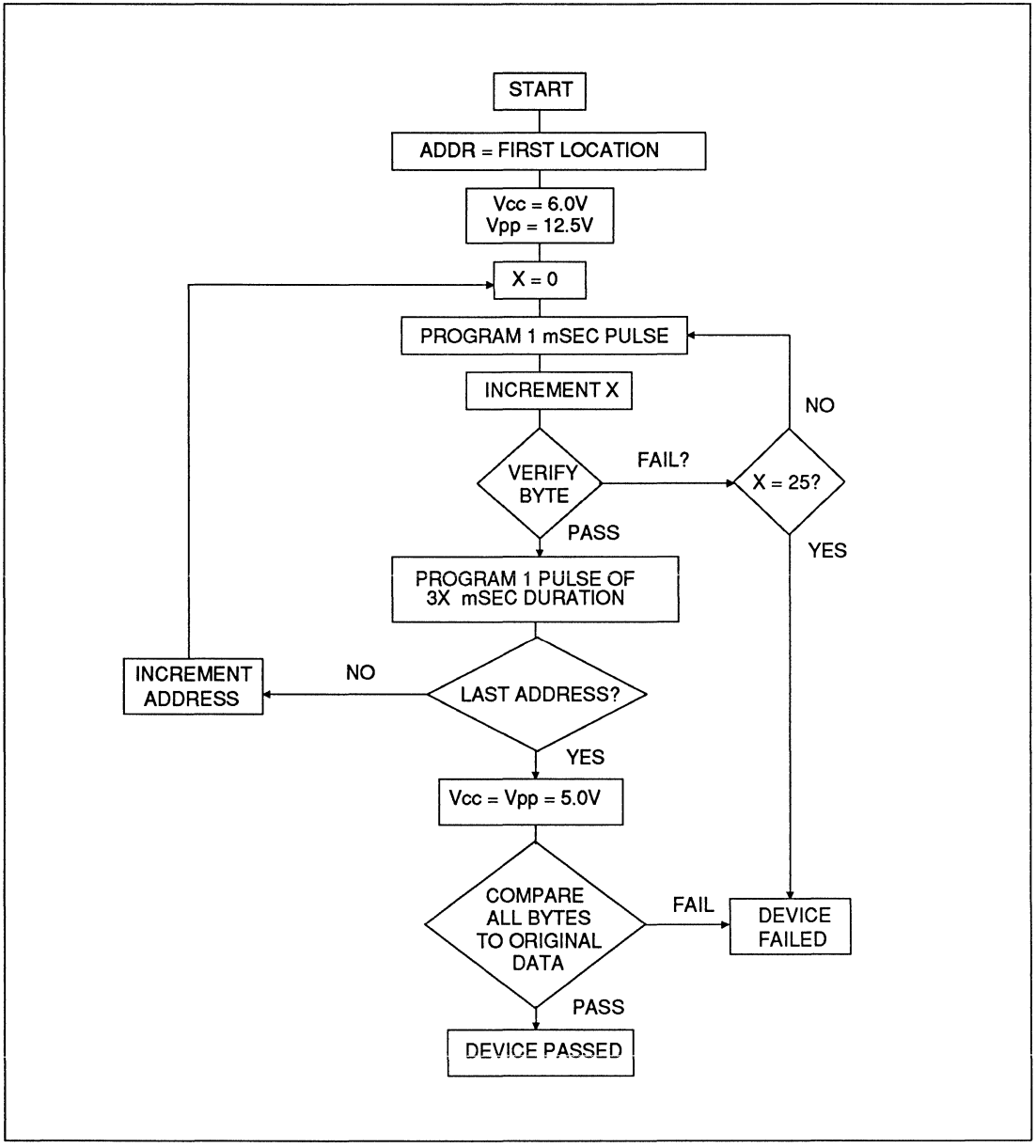
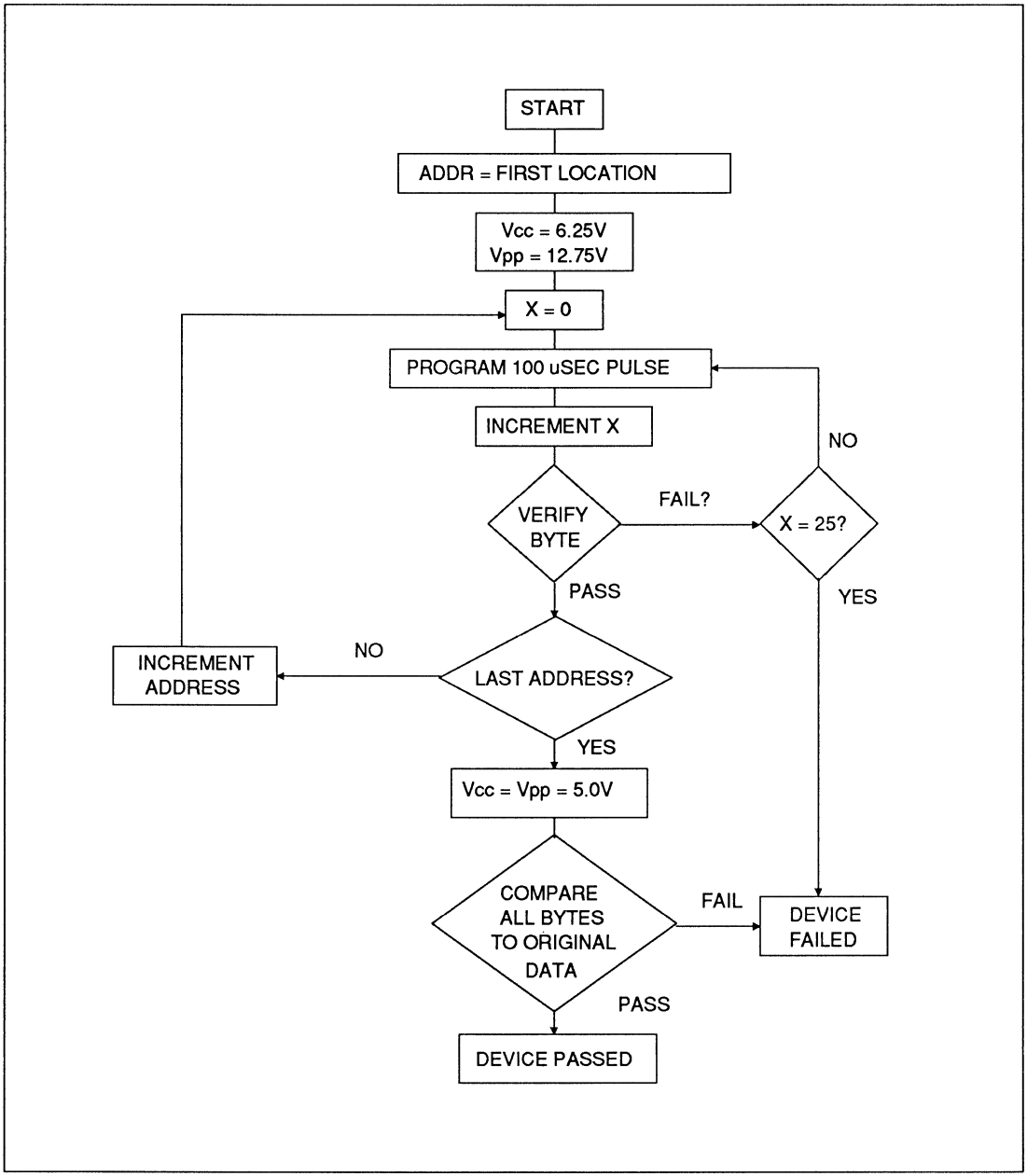


Fig. 5 QUICK PULSE ALGORITHM



READ OPERATION AND STANDBY MODES

Memory access for reading an address location is controlled by $\overline{CE}$ and $\overline{OE}$. Chip enable $\overline{CE}$ is used independently of all other input signals as the primary device selection. In the logic zero state (TTL level V_{IL}), $\overline{CE}$ powers up all inputs and enables internal circuitry. In the logic one state (CMOS level V_{IHC}) $\overline{CE}$ places the device in standby mode, all DC paths to ground are shut-off, and the power dissipation is reduced to a minimum. A logic one on Output Enable $\overline{OE}$ disables the output buffers and places the output pads in a high impedance state. Assuming that the address lines A_0 to A_{14} have been stable for a time equal to T_{ACC} - T_{OE}, the output data is available after a delay of T_{OE} from the falling edge of $\overline{OE}$.

SIGNATURE MODE

The Signature Mode allows one to identify the IC manufacturer and the type of the part. This mode is entered as a regular Read Mode by driving low the $\overline{CE}$ and $\overline{OE}$ inputs, and in addition driving the input address bit A_9 to high-voltage VH level with all other address lines at V_{IL}.

A V_{IL} on A_0 with all other addresses at V_{IL}, gives the binary code of the IC manufacturer on outputs O_0 to O_7.

CATALYST Code:
0 0 1 1 0 0 0 1 (31H)

A V_{IH} on A_0 with all other addresses at V_{IL}, gives the binary code of the device type on outputs O_0 to O_7.

27HC256 / 27HC256L Code:
0 1 0 0 0 0 0 0 (40H)

PROGRAMMING MODE

After a proper erasure operation, all bits of the EPROM are in the logic one state. The device is programmed by selectively writing logic zeros into the desired bit locations. The programming mode is entered by raising $\overline{CE}$ and $\overline{OE}$ to a high level and bringing the low voltage supply pin (V_{CC}), followed by the high voltage supply pin (V_{PP}), to their respective programming levels.

After the address inputs A_0 to A_{14} and data inputs O_0 to O_7 are stabilized, $\overline{CE}$ is switched from the logic one to logic zero state to perform the programming. The particular memory cells of the addressed byte, corresponding to the 0's of the input data bits, are then programmed.

A Program Verify cycle is performed after each byte is programmed to ensure that the zero bits have been correctly written. The byte verification cycle is initiated by keeping $\overline{CE}$ at V_{IH} and switching $\overline{OE}$ from V_{IH} to V_{IL}, while all other pin voltages remain unchanged. In most cases a single 100-microsecond programming cycle is sufficient to set a memory cell in the logic zero state. The Quick Pulse algorithm is recommended as the preferred device programming operation. The CAT27HC256I is also compatible with "Intelligent Programming."

The flow charts for both the algorithms are given in Fig.4 and Fig.5.

U.V. ERASURE OPERATION FOR CERDIP EPROMS

Direct exposure to fluorescent lamps such as those used in room light fixtures, can erase the CAT27HC256I EPROM in less than three years. When exposed to direct sunlight the EPROM can be erased in less than a week.

The recommended erasure procedure is to expose the CAT27HC256I EPROM to a standard ultraviolet light with a wavelength of 2537 Angstroms. The integrated dose for proper erasure is 15 $Wsec/cm^2$. The erasure time with this dosage is approximately 15 to 60 minutes using an ultraviolet lamp with a 1200 $\mu W/cm^2$ power rating. The EPROM should be placed within 1 inch of the lamp tubes.

The maximum integrated dose a CAT27HC256I EPROM can be exposed to is 7258 $Wsec/cm^2$ (one week at 1200 $\mu W/cm^2$). Exposure of the device to higher U.V. doses may cause permanent damage and loss of functionality.

CAT27HC256LI - Low Power Industrial Temperature

32,768 x 8-BIT HIGH-SPEED CMOS EPROM

Preliminary

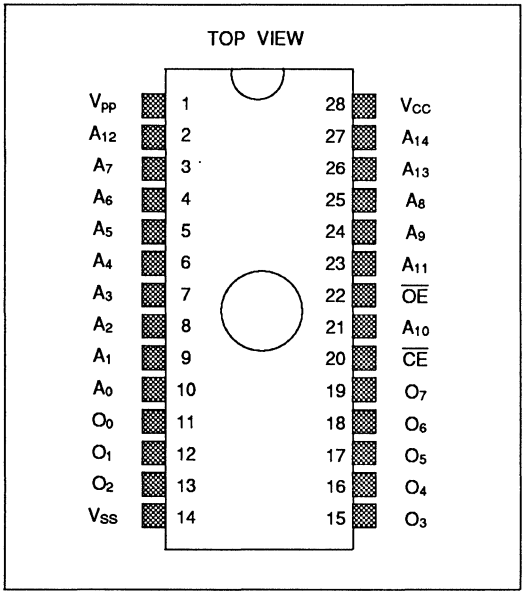
DESCRIPTION

The CAT27HC256LI is a high speed 256K UV erasable and electrically reprogrammable EPROM ideally suited for high speed applications. Any byte can be accessed in less than 55ns making this part compatible with high performance microprocessor systems by eliminating the need for speed-robbing wait states. The Quick Pulse algorithm reduces the time required to program this chip and ensures more reliable programming. The CAT27HC256LI is used in applications where fast turnaround and pattern experimentation are important requirements. The CAT27HC256LI is available in a 28-pin dual-in-line package with a transparent lid. This allows the user to expose the chip to ultraviolet light to erase the bit pattern, allowing a new pattern to be written into the device.

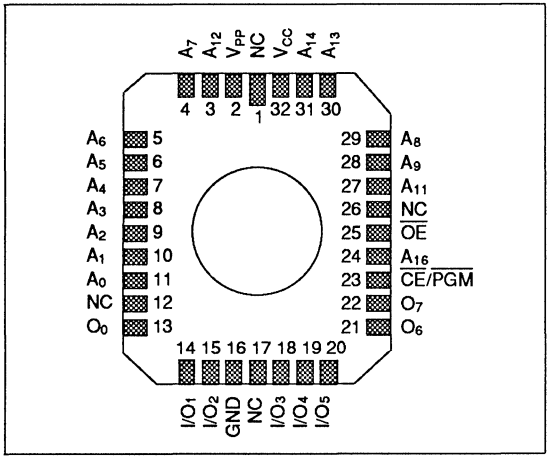
FEATURES

- Fast access time: 55/70/90/120ns
- 5V single power supply - read mode
- Low current requirements:
  - Active: 80mA max (CMOS levels)
  - Standby: 1mA max (CMOS levels)
- High speed programming: 100µs/byte
- TTL compatible Input/Output
- 12.5V programming voltage
- JEDEC approved 28-pin DIP and 32-pin LCC
- Electronic signature

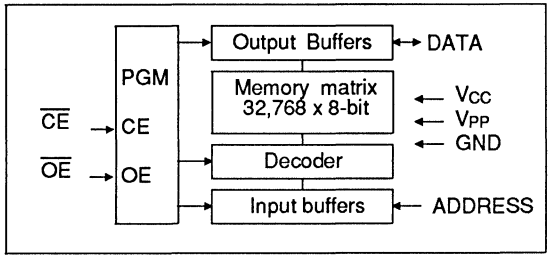
PIN CONFIGURATION 28-PIN DIP



PIN CONFIGURATION 32-PIN LCC



BLOCK DIAGRAM



FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	A_0 (10)	A_9 (24)	I/O
Read	V_{IL}	V_{IL}	V_{CC}	-	-	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{CC}	-	-	High-Z
Standby	V_{IH}	-	V_{CC}	-	-	High-Z
Program	V_{IL}	V_{IH}	V_{PP}	-	-	D_{IN}
Program verify	V_{IH}	V_{IL}	V_{PP}	-	-	D_{OUT}
Program inhibit	V_{IH}	V_{IH}	V_{PP}	-	-	High-Z
Signature MFG.	V_{IL}	V_{IL}	V_{CC}	V_{IL}	V_H	31H
Signature device	V_{IL}	V_{IL}	V_{CC}	V_{IH}	V_H	40H

NOTES ON THE FUNCTION TABLE

Logic Levels: V_{IH} = TTL Logic 1 level
V_{IL} = TTL Logic 0 level
" - " = Logic "Do not care," V_{IH} or V_{IL}

Supply Voltage: V_{PP} = Programming / high-voltage
V_{CC} = Read / low-voltage
V_H = 12.0V ±0.5V

Read: Read mode: the content of the addressed memory byte is placed on the I/O pins O_0 to O_7

Output Disable: Device is selected (active mode), programming is disabled and O_0 to O_7 output buffers are tristated (PMOS and NMOS drivers turned-off)

Standby: Device is deselected, low power dissipation

Program: Byte programming mode: logic zeros in the bit pattern driving the O_0 to O_7 data input buffers are written into the respective memory cells of the addressed byte

Program Verify: Following a programming cycle, to verify the cell contents of the memory byte being programmed (not recommended as a normal read operation)

Program Inhibit: $\overline{CE}$ set to logic one and $\overline{OE}$ set to logic one prevents programming and deselects the device

Signature MFG: Signature mode with all other addresses at V_{IL}, code of IC manufacturer (Catalyst) output on I/O pins O_0 to O_7

Signature device: Signature mode with all other addresses at V_{IL}, code of IC type output on I/O pins O_0 to O_7

PIN CAPACITANCE
(T_A = 25°C, Freq = 1.0MHz)

PARAMETER	TYPICAL	MAXIMUM	CONDITIONS
Input pin capacitance C_{IN}	4.0pF	6.0pF	V_{IN} = 0.0V
Output pin capacitance C_{OUT}	6.0pF	10.0pF	V_{OUT} = 0.0V
V_{PP} supply capacitance CV_{PP}		25.0pF	V_{PP} = 0.0V

ABSOLUTE MAXIMUM RATINGS

Temperature under bias	- 65°C to +135°C
Storage temperature	- 65°C to +135°C
All input/output voltages (except A_9)	- 0.5V to V_{CC}+0.5V
Voltage on A_9	- 1.0V to +14.0 V
Read supply voltage	- 1.0V to +7.0 V
Program voltage	- 1.0V to +14.0 V
Power dissipation, T_A = 25°C	1.0 W
DC short-circuit current, output pin	20.0 mA
Max lead solder temp., 10 seconds	300°C

(Voltages with respect to ground)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SUPPLY CURRENT CHARACTERISTICS (AC and DC)

(T_A = Industrial -40°C to 85°C)

Symbol	Parameter	Conditions	Low Power	Limit
I_{CC}	V_{CC} active current (DC)	$\overline{OE} = \overline{CE} = V_{IL}$, $V_{PP} = V_{CC}$ $A_0 - A_{14} = V_{IL}$	40mA	Max
I_{CC1}	V_{CC} active current (CMOS in @ 10MHz)	Inputs conform to V_{ILC} and V_{IHC}	80mA	Max
I_{CC2}	V_{CC} active current (TTL in @ 10MHz)	Inputs conform to AC test waveform (Fig. 1)	80mA	Max
I_{SB1}	V_{CC} standby current (CMOS in)	$\overline{CE} = V_{IHC}$	1mA	Max
I_{SB2}	V_{CC} standby current (TTL in)	$\overline{CE} = V_{IH}$	3mA	Max

DC CHARACTERISTICS <Read Operation>

(V_{CC} = 5V ± 10%, T_A = Industrial -40°C to 85°C)

Symbol	Parameter	Conditions	Limits			Units
			Min.	Typ.	Max.	
I_{LI}	Input leakage current	V_{IN} = 5.5V	-	-	10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V	-	-	10	µA
I_{PP1}	V_{PP} leakage current	V_{PP} = 5.5V	-	-	10	µA
V_{IH}	Input high level TTL		2.0	-	V_{CC}+0.5	V
V_{IL}	Input low level TTL		-0.5	-	0.8	V
V_{OH}	Output voltage high level	I_{OH} = -1.0 mA	2.4	-	-	V
V_{OL}	Output voltage low level	I_{OL} = 4.0 mA	-	-	0.40	V
V_{ILC}	Input low level CMOS		-0.5	-	0.30	V
V_{IHC}	Input high level CMOS		V_{CC} -0.5	-	V_{CC} +0.5	V

NOTES:

- The maximum current values are with outputs O_0 to O_7 unloaded.
- V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

AC CHARACTERISTICS <READ OPERATION>

(Temperature range: Industrial -40°C to 85°C)

Symbol	Parameter	V_{CC}±5%	27HC256-55/5		27HC256-70/5		27HC256-90/5		27HC256-120/5		Unit
		V_{CC}±10%	NOTE 1		27HC256-70		27HC256-90		27HC256-120		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACC}	Address access time		-	55	-	70	-	90	-	120	ns
t_{CE}	$\overline{CE}$ to output delay		-	55	-	70	-	90	-	120	ns
t_{OE}	$\overline{OE}$ to output delay		-	30	-	35	-	40	-	50	ns
t_{OH} *	Output hold A, $\overline{OE}$, $\overline{CE}$		0	-	0	-	0	-	0	-	ns
t_{DF} *	$\overline{OE}$ high to out High-Z		0	30	0	35	0	40	0	50	ns

- Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer
- Input rise and fall times (10% to 90%) = 5ns
- Input pulse levels = 0.0V to 3.0V
- Input and output timing reference = 0.8V and 2.0V

* These parameters are sampled and not 100% tested.

NOTE 1. The 55ns version is not currently available in military, low power or V_{CC} = ±10%

Fig. 1 AC Test Waveforms

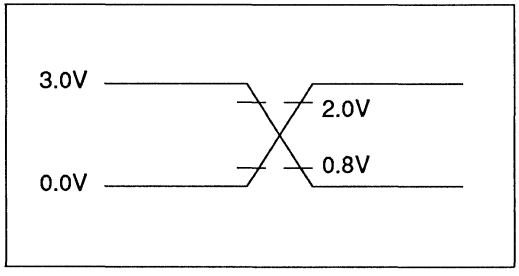
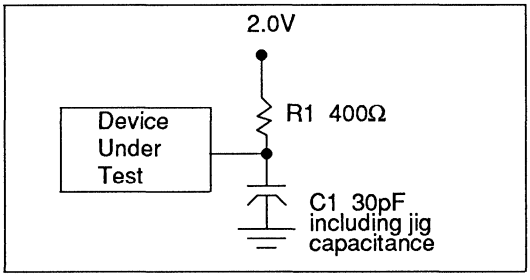
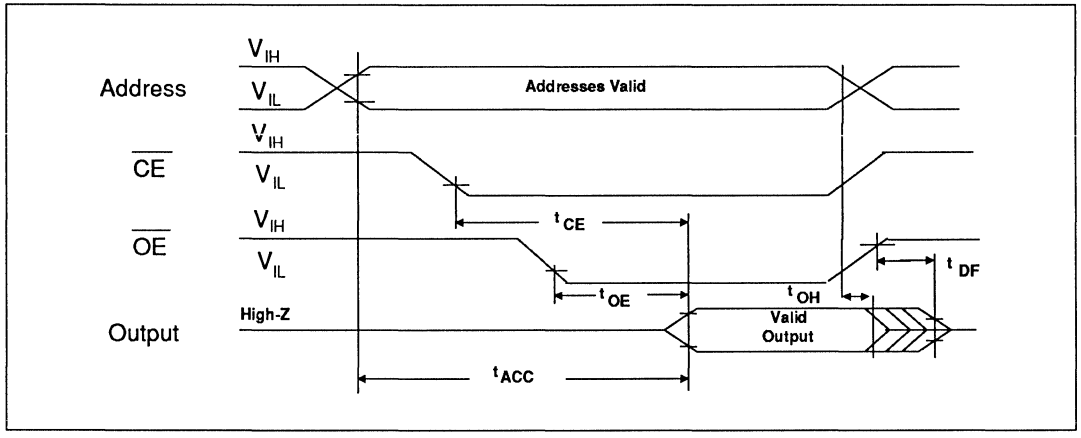


Fig. 2 Output Test Load



TIMING <Read Operation>



DC CHARACTERISTICS <Programming Operation>

(T_A = 25°C ± 5°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Low-voltage supply Quick Pulse algorithm	-	6	6.25	6.5	V
V_{CC}	Low-voltage supply Intelligent algorithm	-	5.75	6.0	6.25	V
V_{PP}	High-voltage supply Quick Pulse algorithm	-	12.50	12.75	13.0	V
V_{PP}	High-voltage supply Intelligent algorithm	-	12.0	12.5	13.0	V
I_{CCP}	V_{CC} supply current Program and Verify	-	-	-	80.0	mA
I_{PP}	V_{PP} supply current Program Operation	-	-	-	40.0	mA
I_{LI}	Input leakage current	V_{IN} = 5.25V	-	-	10.0	µA
I_{LO}	Output leakage current	V_{OUT} = 5.25V	-	-	10.0	µA
V_{IL}	Input Low-Level TTL	-	-0.50	-	0.80	V
V_{ILC}	Input Low-Level CMOS	-	-0.50	-	0.30	V
V_{OL}	Output Low-Level	I_{OL} = 4.0mA	-	-	0.40	V
V_{IH}	Input High-Level TTL	-	2.0	-	V_{CC}+0.50	V
V_{IHC}	Input High-Level CMOS	-	V_{CC}-0.50	-	V_{CC}+0.50	V
V_{OH}	Output High level	I_{OH} = -1.0mA	2.4	-	-	V
V_H	High-Voltage INPUT for Signature Mode(s)	(See notes below)	11.5	-	12.50	V

NOTES:

- The maximum current values are with outputs O_0 to O_7 unloaded.
- V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

AC CHARACTERISTICS <Programming Operation>

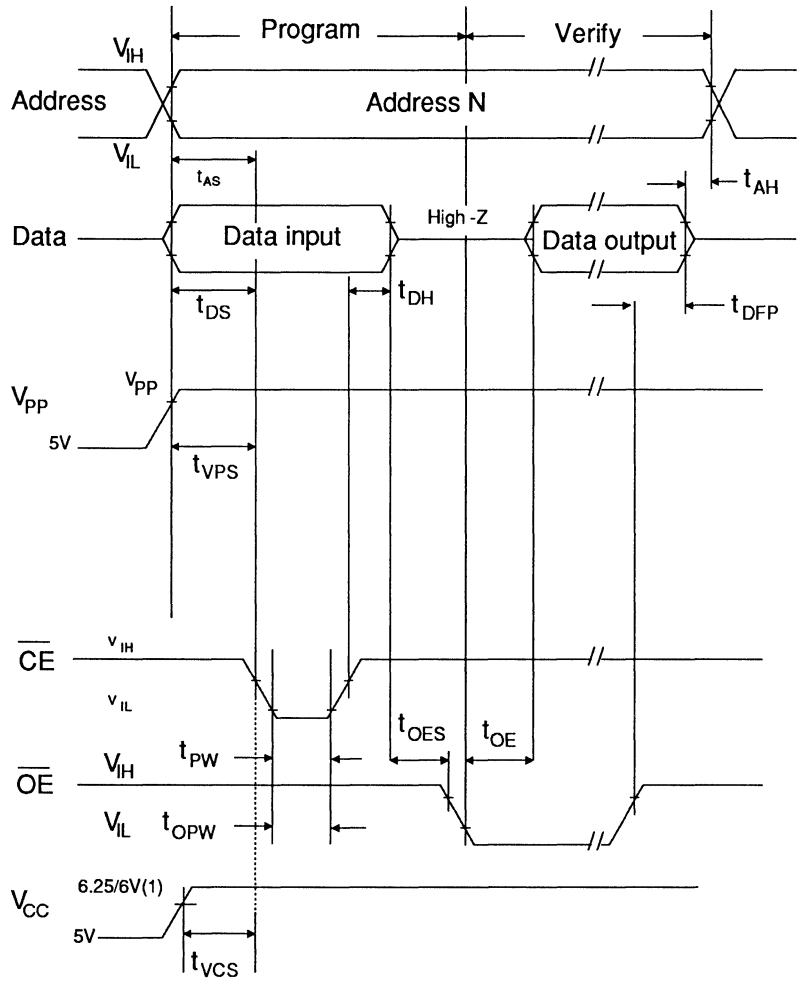
(T_A = 25°C ±5°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{AS}	Address set-up time	-	2.0	-	-	µs
t_{OES}	$\overline{OE}$ set-up time	-	2.0	-	-	µs
t_{DS}	Data set-up time	-	2.0	-	-	µs
t_{AH}	Address hold time	-	0.0	-	-	µs
t_{DH}	Data hold time	-	2.0	-	-	µs
t_{VPS}	V_{PP} set-up time	-	2.0	-	-	µs
t_{VCS}	V_{CC} set-up time	-	2.0	-	-	µs
t_{PW}	$\overline{CE}$ pulse width Quick Pulse algorithm	-	95.0	100.0	105.0	µs
t_{PW}	$\overline{CE}$ pulse width Intelligent algorithm	-	0.95	1.0	1.05	ms
t_{OPW}	$\overline{CE}$ overprogram pulse width Intelligent algorithm	-	2.85	-	78.5	ms
t_{DFP}	$\overline{OE}$ high to Output High-Z	-	0.0	-	130	ns
t_{OE}	Data valid from $\overline{OE}$	-	-	-	150	ns

NOTES:
- Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer.
- Input Rise and Fall times (10% to 90%) = 20ns.
- Input Pulse Levels = 0.0V to 3.0V.
- Input and Output Timing Reference = 0.80V and 2.0V.
- t_{DPF} is sampled and not 100% tested.

When programming the device a 0.1 microfarad capacitor is required between V_{PP} and V_{SS} to suppress spurious voltage transients which can damage the part.

TIMING <Programming Operation>



(1) Note: V_{CC} = 6.25V ±0.25V for Quick Pulse algorithm
6.00V ±0.25V for Intelligent Programming algorithm

Fig. 4 INTELLIGENT ALGORITHM

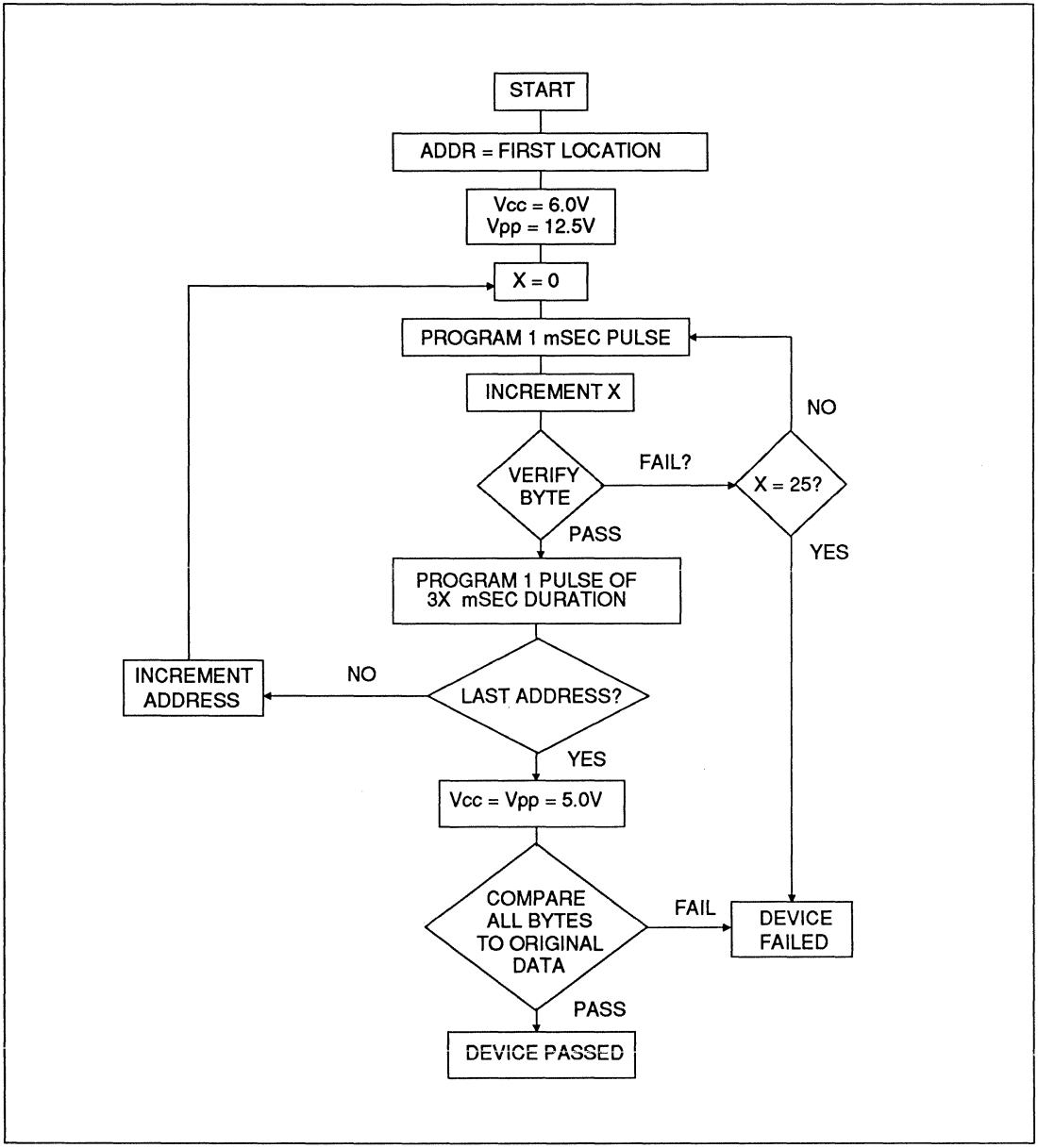
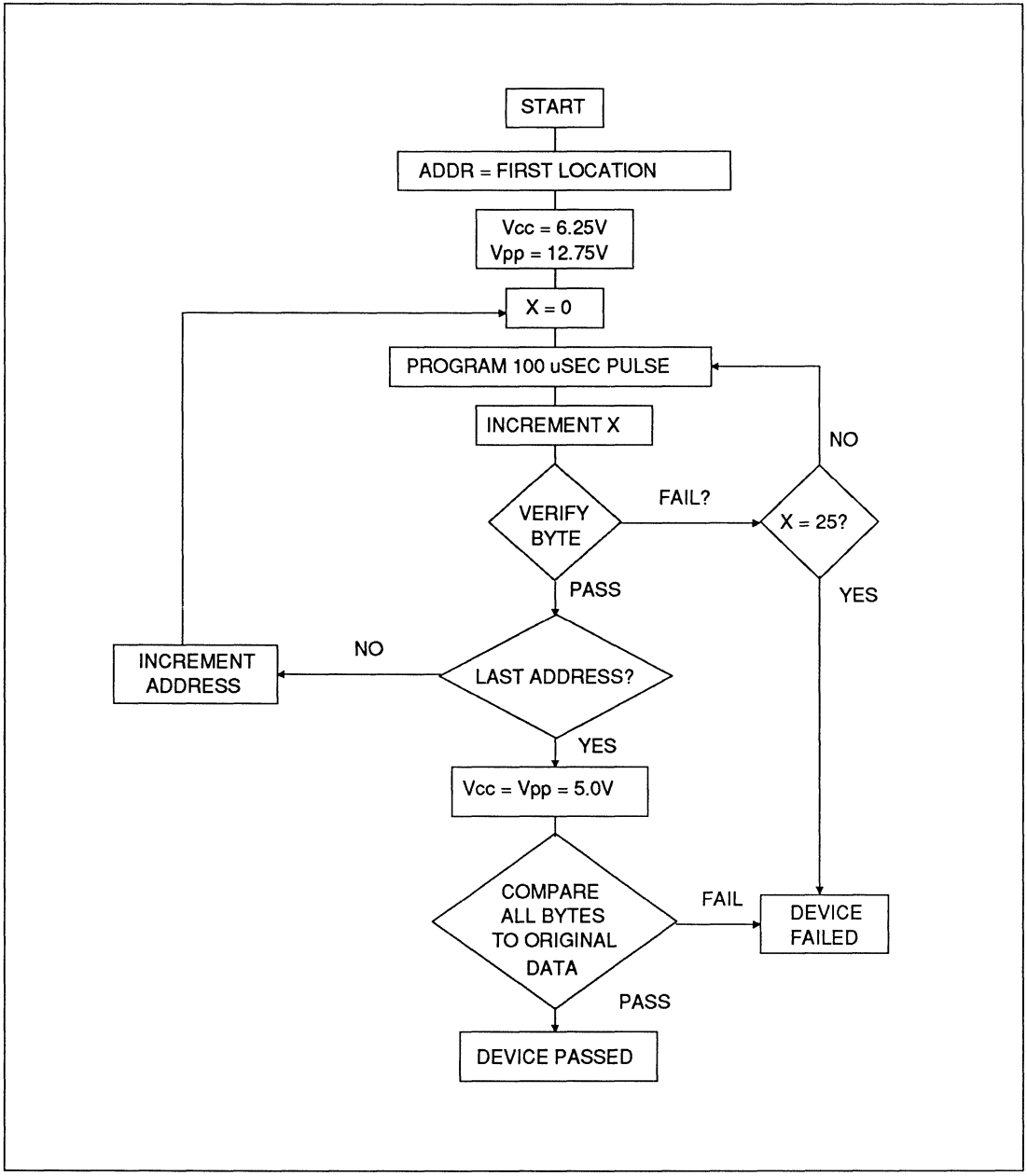


Fig. 5 QUICK PULSE ALGORITHM



READ OPERATION AND STANDBY MODES

Memory access for reading an address location is controlled by $\overline{CE}$ and $\overline{OE}$. Chip enable $\overline{CE}$ is used independently of all other input signals as the primary device selection. In the logic zero state (TTL level V_{IL}), $\overline{CE}$ powers up all inputs and enables internal circuitry. In the logic one state (CMOS level V_{IHC}) $\overline{CE}$ places the device in standby mode, all DC paths to ground are shut-off, and the power dissipation is reduced to a minimum. A logic one on Output Enable $\overline{OE}$ disables the output buffers and places the output pads in a high impedance state. Assuming that the address lines A_0 to A_{14} have been stable for a time equal to T_{ACC} - T_{OE}, the output data is available after a delay of T_{OE} from the falling edge of $\overline{OE}$.

SIGNATURE MODE

The Signature Mode allows one to identify the IC manufacturer and the type of the part. This mode is entered as a regular Read Mode by driving low the $\overline{CE}$ and $\overline{OE}$ inputs, and in addition driving the input address bit A_9 to high-voltage VH level with all other address lines at V_{IL}.

A V_{IL} on A_0 with all other addresses at V_{IL}, gives the binary code of the IC manufacturer on outputs O_0 to O_7.

CATALYST Code:
0 0 1 1 0 0 0 1 (31H)

A V_{IH} on A_0 with all other addresses at V_{IL}, gives the binary code of the device type on outputs O_0 to O_7.

27HC256 / 27HC256L Code:
0 1 0 0 0 0 0 0 (40H)

PROGRAMMING MODE

After a proper erasure operation, all bits of the EPROM are in the logic one state. The device is programmed by selectively writing logic zeros into the desired bit locations. The programming mode is entered by raising $\overline{CE}$ and $\overline{OE}$ to a high level and bringing the low voltage supply pin (V_{CC}), followed by the high voltage supply pin (V_{PP}), to their respective programming levels.

After the address inputs A_0 to A_{14} and data inputs O_0 to O_7 are stabilized, $\overline{CE}$ is switched from the logic one to logic zero state to perform the programming. The particular memory cells of the addressed byte, corresponding to the 0's of the input data bits, are then programmed.

A Program Verify cycle is performed after each byte is programmed to ensure that the zero bits have been correctly written. The byte verification cycle is initiated by keeping $\overline{CE}$ at V_{IH} and switching $\overline{OE}$ from V_{IH} to V_{IL}, while all other pin voltages remain unchanged. In most cases a single 100-microsecond programming cycle is sufficient to set a memory cell in the logic zero state. The Quick Pulse algorithm is recommended as the preferred device programming operation. The CAT27HC256LI is also compatible with "Intelligent Programming."

The flow charts for both the algorithms are given in Fig.4 and Fig.5.

U.V. ERASURE OPERATION FOR CERDIP EPROMS

Direct exposure to fluorescent lamps such as those used in room light fixtures, can erase the CAT27HC256LI EPROM in less than three years. When exposed to direct sunlight the EPROM can be erased in less than a week.

The recommended erasure procedure is to expose the CAT27HC256LI EPROM to a standard ultraviolet light with a wavelength of 2537 Angstroms. The integrated dose for proper erasure is 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 60 minutes using an ultraviolet lamp with a 1200 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes.

The maximum integrated dose a CAT27HC256LI EPROM can be exposed to is 7258 Wsec/cm^2 (one week at 1200 μW/cm^2). Exposure of the device to higher U.V. doses may cause permanent damage and loss of functionality.

CAT27HC256M - Military Temperature

32,768 x 8-BIT HIGH-SPEED CMOS EPROM

Preliminary

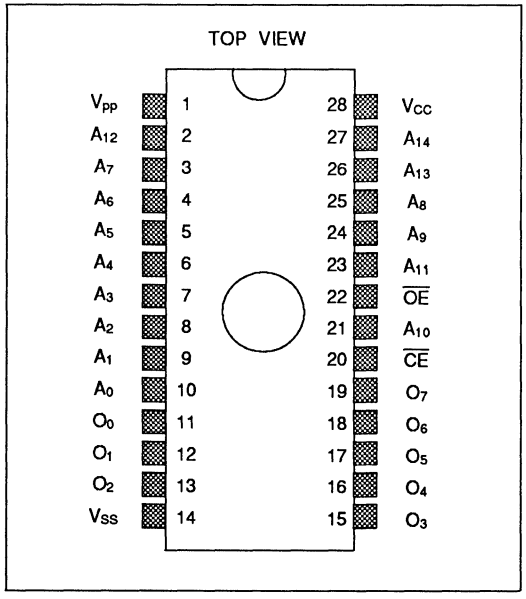
DESCRIPTION

The CAT27HC256M is a high speed 256K UV erasable and electrically reprogrammable EPROM ideally suited for high speed applications. Any byte can be accessed in less than 70ns making this part compatible with high performance microprocessor systems by eliminating the need for speed-robbing wait states. The Quick Pulse algorithm reduces the time required to program this chip and ensures more reliable programming. The CAT27HC256M is used in applications where fast turnaround and pattern experimentation are important requirements. The CAT27HC256LM is available in a 28-pin dual-in-line package with a transparent lid. This allows the user to expose the chip to ultraviolet light to erase the bit pattern, allowing a new pattern to be written into the device.

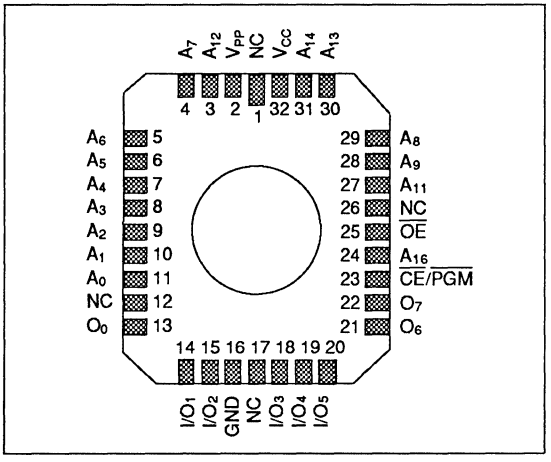
FEATURES

- Fast access time: 70/90/120ns
- 5V single power supply - read mode
- Low current requirements:
  - Active: 80mA max (CMOS levels)
  - Standby: 1mA max (CMOS levels)
- High speed programming: 100µs/byte
- TTL compatible Input/Output
- 12.5V programming voltage
- JEDEC approved 28-pin DIP and 32-pin LCC
- Electronic signature

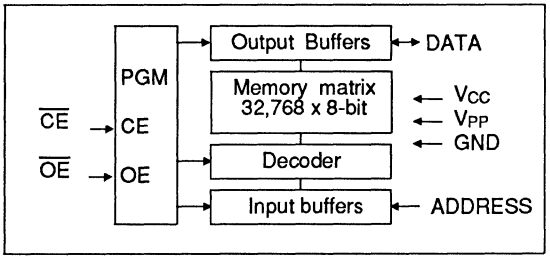
PIN CONFIGURATION 28-PIN DIP



PIN CONFIGURATION 32-PIN LCC



BLOCK DIAGRAM



FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	A_0 (10)	A_9 (24)	I/O
Read	V_{IL}	V_{IL}	V_{CC}	-	-	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{CC}	-	-	High-Z
Standby	V_{IH}	-	V_{CC}	-	-	High-Z
Program	V_{IL}	V_{IH}	V_{PP}	-	-	D_{IN}
Program verify	V_{IH}	V_{IL}	V_{PP}	-	-	D_{OUT}
Program inhibit	V_{IH}	V_{IH}	V_{PP}	-	-	High-Z
Signature MFG.	V_{IL}	V_{IL}	V_{CC}	V_{IL}	V_H	31H
Signature device	V_{IL}	V_{IL}	V_{CC}	V_{IH}	V_H	40H

NOTES ON THE FUNCTION TABLE

Logic Levels: V_{IH} = TTL Logic 1 level
V_{IL} = TTL Logic 0 level
" - " = Logic "Do not care," V_{IH} or V_{IL}

Supply Voltage: V_{PP} = Programming / high-voltage
V_{CC} = Read / low-voltage
V_H = 12.0V ±0.5V

Read: Read mode: the content of the addressed memory byte is placed on the I/O pins O_0 to O_7

Output Disable: Device is selected (active mode), programming is disabled and O_0 to O_7 output buffers are tristated (PMOS and NMOS drivers turned-off)

Standby: Device is deselected, low power dissipation

Program: Byte programming mode: logic zeros in the bit pattern driving the O_0 to O_7 data input buffers are written into the respective memory cells of the addressed byte

Program Verify: Following a programming cycle, to verify the cell contents of the memory byte being programmed (not recommended as a normal read operation)

Program Inhibit: $\overline{CE}$ set to logic one and $\overline{OE}$ set to logic one prevents programming and deselects the device

Signature MFG: Signature mode with all other addresses at V_{IL}, code of IC manufacturer (Catalyst) output on I/O pins O_0 to O_7

Signature device: Signature mode with all other addresses at V_{IL}, code of IC type output on I/O pins O_0 to O_7

PIN CAPACITANCE
(T_A = 25°C, Freq = 1.0MHz)

PARAMETER	TYPICAL	MAXIMUM	CONDITIONS
Input pin capacitance C_{IN}	4.0pF	6.0pF	V_{IN} = 0.0V
Output pin capacitance C_{OUT}	6.0pF	10.0pF	V_{OUT} = 0.0V
V_{PP} supply capacitance CV_{PP}		25.0pF	V_{PP} = 0.0V

ABSOLUTE MAXIMUM RATINGS

Temperature under bias	- 65°C to +135°C
Storage temperature	- 65°C to +135°C
All input/output voltages (except A_9)	- 0.5V to V_{CC}+0.5V
Voltage on A_9	- 1.0V to +14.0 V
Read supply voltage	- 1.0V to +7.0 V
Program voltage	- 1.0V to +14.0 V
Power dissipation, T_A = 25°C	1.0 W
DC short-circuit current, output pin	20.0 mA
Max lead solder temp., 10 seconds	300°C
(Voltages with respect to ground)	

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SUPPLY CURRENT CHARACTERISTICS (AC and DC)

(T_A = Military -55°C to 125°C)

Symbol	Parameter	Conditions	Standard	Limit
I_{CC}	V_{CC} active current (DC)	$\overline{OE}$ = $\overline{CE}$ = V_{IL}, V_{PP} = V_{CC} A_0 - A_{14} = V_{IL}	55mA	Max
I_{CC1}	V_{CC} active current (CMOS in @ 10MHz)	Inputs conform to V_{ILC} and V_{IHC}	80mA	Max
I_{CC2}	V_{CC} active current (TTL in @ 10MHz)	Inputs conform to AC test waveform (Fig. 1)	80mA	Max
I_{SB1}	V_{CC} standby current (CMOS in)	$\overline{CE}$ = V_{IHC}	45mA	Max
I_{SB2}	V_{CC} standby current (TTL in)	$\overline{CE}$ = V_{IH}	45mA	Max

DC CHARACTERISTICS <Read Operation>

(V_{CC} = 5V ± 10%, T_A = Military -55°C to 125°C)

Symbol	Parameter	Conditions	Limits			Units
			Min.	Typ.	Max.	
I_{LI}	Input leakage current	V_{IN} = 5.5V	-	-	10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V	-	-	10	µA
I_{PP1}	V_{PP} leakage current	V_{PP} = 5.5V	-	-	10	µA
V_{IH}	Input high level TTL		2.0	-	V_{CC}+0.5	V
V_{IL}	Input low level TTL		-0.5	-	0.8	V
V_{OH}	Output voltage high level	I_{OH} = -1.0 mA	2.4	-	-	V
V_{OL}	Output voltage low level	I_{OL} = 4.0 mA	-	-	0.40	V
V_{ILC}	Input low level CMOS		-0.5	-	0.30	V
V_{IHC}	Input high level CMOS		V_{CC} -0.5	-	V_{CC} +0.5	V

NOTES:

- The maximum current values are with outputs O_0 to O_7 unloaded.
- V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} .

AC CHARACTERISTICS <READ OPERATION>

(Temperature range: Military -55°C to 125°C)

Symbol	Parameter	Vcc±5%	27HC256-70/5		27HC256-90/5		27HC256-120/5		Unit
		Vcc±10%	27HC256-70		27HC256-90		27HC256-120		
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACC}	Address access time		-	70	-	90	-	120	ns
t_{CE}	$\overline{CE}$ to output delay		-	70	-	90	-	120	ns
t_{OE}	$\overline{OE}$ to output delay		-	35	-	40	-	50	ns
t_{OH} *	Output hold A, $\overline{OE}$, $\overline{CE}$		0	-	0	-	0	-	ns
t_{DF} *	$\overline{OE}$ high to out High-Z		0	35	0	40	0	50	ns

- Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer
- Input rise and fall times (10% to 90%) = 5ns
- Input pulse levels = 0.0V to 3.0V
- Input and output timing reference = 0.8V and 2.0V

* These parameters are sampled and not 100% tested.

Fig. 1 AC Test Waveforms

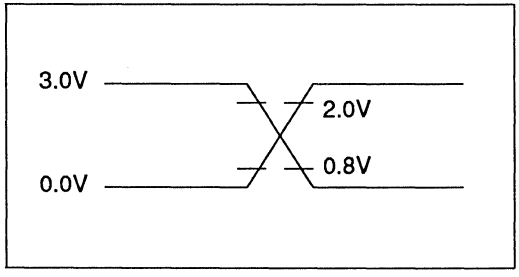
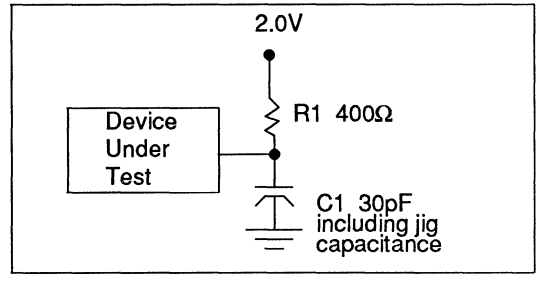
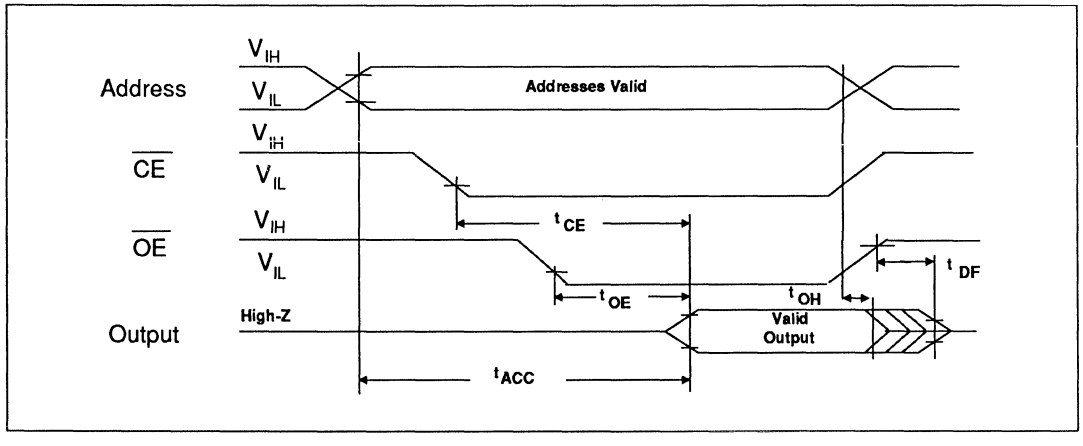


Fig. 2 Output Test Load



TIMING <Read Operation>



DC CHARACTERISTICS <Programming Operation>

(T_A = 25°C ± 5°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Low-voltage supply Quick Pulse algorithm	-	6	6.25	6.5	V
V_{CC}	Low-voltage supply Intelligent algorithm	-	5.75	6.0	6.25	V
V_{PP}	High-voltage supply Quick Pulse algorithm	-	12.50	12.75	13.0	V
V_{PP}	High-voltage supply Intelligent algorithm	-	12.0	12.5	13.0	V
I_{CCP}	V_{CC} supply current Program and Verify	-	-	-	80.0	mA
I_{PP}	V_{PP} supply current Program Operation	-	-	-	40.0	mA
I_{LI}	Input leakage current	V_{IN} = 5.25V	-	-	10.0	µA
I_{LO}	Output leakage current	V_{OUT} = 5.25V	-	-	10.0	µA
V_{IL}	Input Low-Level TTL	-	-0.50	-	0.80	V
V_{ILC}	Input Low-Level CMOS	-	-0.50	-	0.30	V
V_{OL}	Output Low-Level	I_{OL} = 4.0mA	-	-	0.40	V
V_{IH}	Input High-Level TTL	-	2.0	-	V_{CC}+0.50	V
V_{IHC}	Input High-Level CMOS	-	V_{CC}-0.50	-	V_{CC}+0.50	V
V_{OH}	Output High level	I_{OH} = -1.0mA	2.4	-	-	V
V_H	High-Voltage INPUT for Signature Mode(s)	(See notes below)	11.5	-	12.50	V

NOTES:

- The maximum current values are with outputs O_0 to O_7 unloaded.
- V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

AC CHARACTERISTICS <Programming Operation>

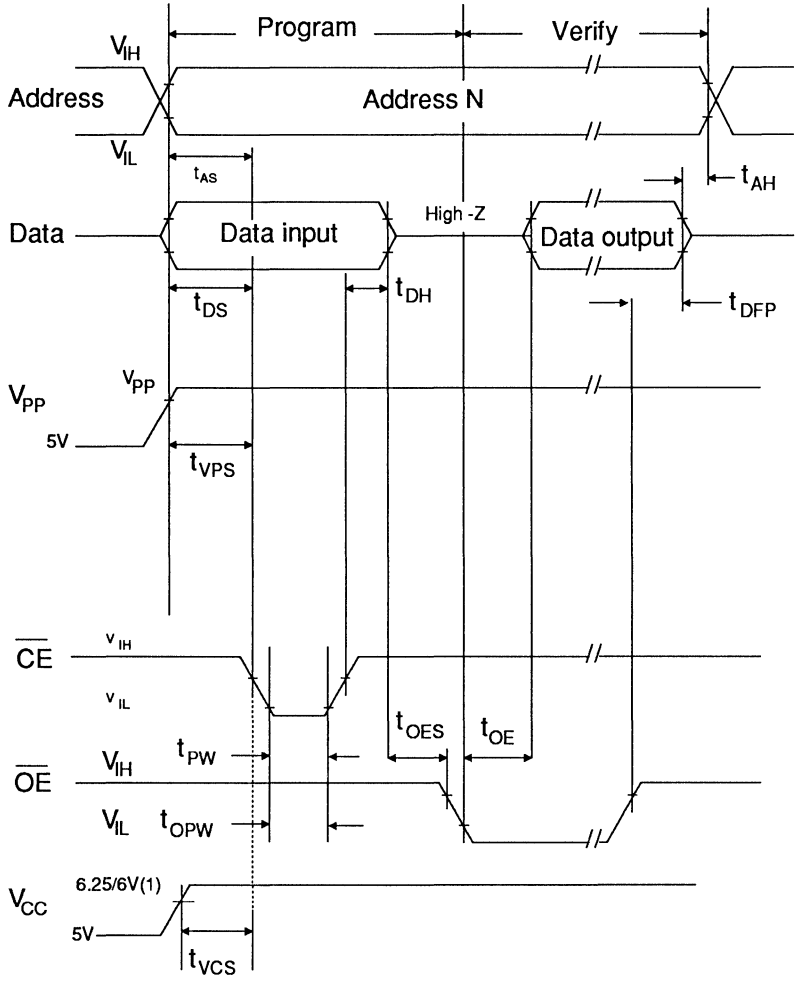
(T_A = 25°C ± 5°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{AS}	Address set-up time	-	2.0	-	-	µs
t_{OES}	$\overline{OE}$ set-up time	-	2.0	-	-	µs
t_{DS}	Data set-up time	-	2.0	-	-	µs
t_{AH}	Address hold time	-	0.0	-	-	µs
t_{DH}	Data hold time	-	2.0	-	-	µs
t_{VPS}	V_{PP} set-up time	-	2.0	-	-	µs
t_{VCS}	V_{CC} set-up time	-	2.0	-	-	µs
t_{PW}	$\overline{CE}$ pulse width Quick Pulse algorithm	-	95.0	100.0	105.0	µs
t_{PW}	$\overline{CE}$ pulse width Intelligent algorithm	-	0.95	1.0	1.05	ms
t_{OPW}	$\overline{CE}$ overprogram pulse width Intelligent algorithm	-	2.85	-	78.5	ms
t_{DFP}	$\overline{OE}$ high to Output High-Z	-	0.0	-	130	ns
t_{OE}	Data valid from $\overline{OE}$	-	-	-	150	ns

NOTES:
- Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer.
- Input Rise and Fall times (10% to 90%) = 20ns.
- Input Pulse Levels = 0.0V to 3.0V.
- Input and Output Timing Reference = 0.80V and 2.0V.
- t_{DPF} is sampled and not 100% tested.

When programming the device a 0.1 microfarad capacitor is required between V_{PP} and V_{SS} to suppress spurious voltage transients which can damage the part.

TIMING <Programming Operation>



(1) Note: V_{CC} = 6.25V ±0.25V for Quick Pulse algorithm
6.00V ±0.25V for Intelligent Programming algorithm

Fig. 4 INTELLIGENT ALGORITHM

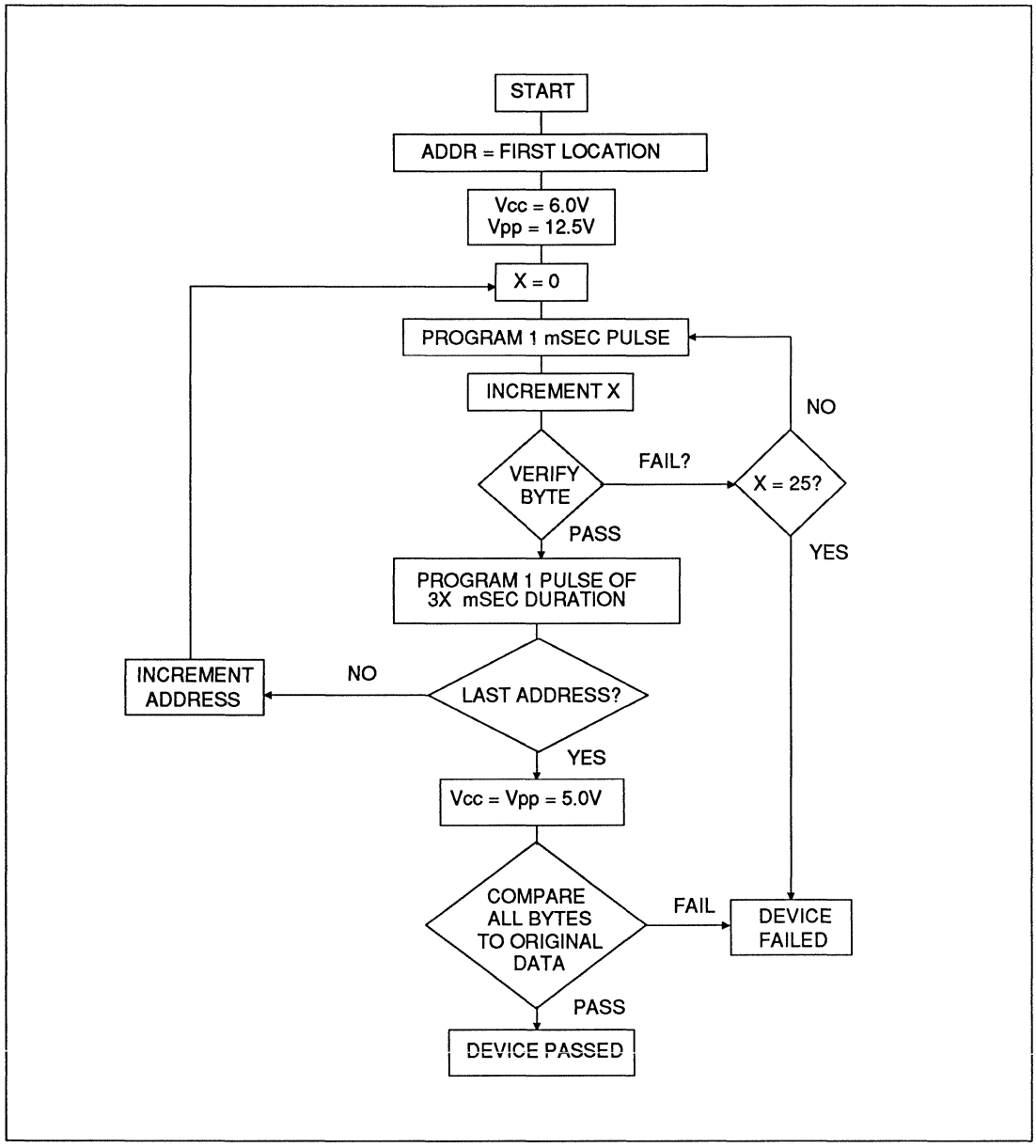
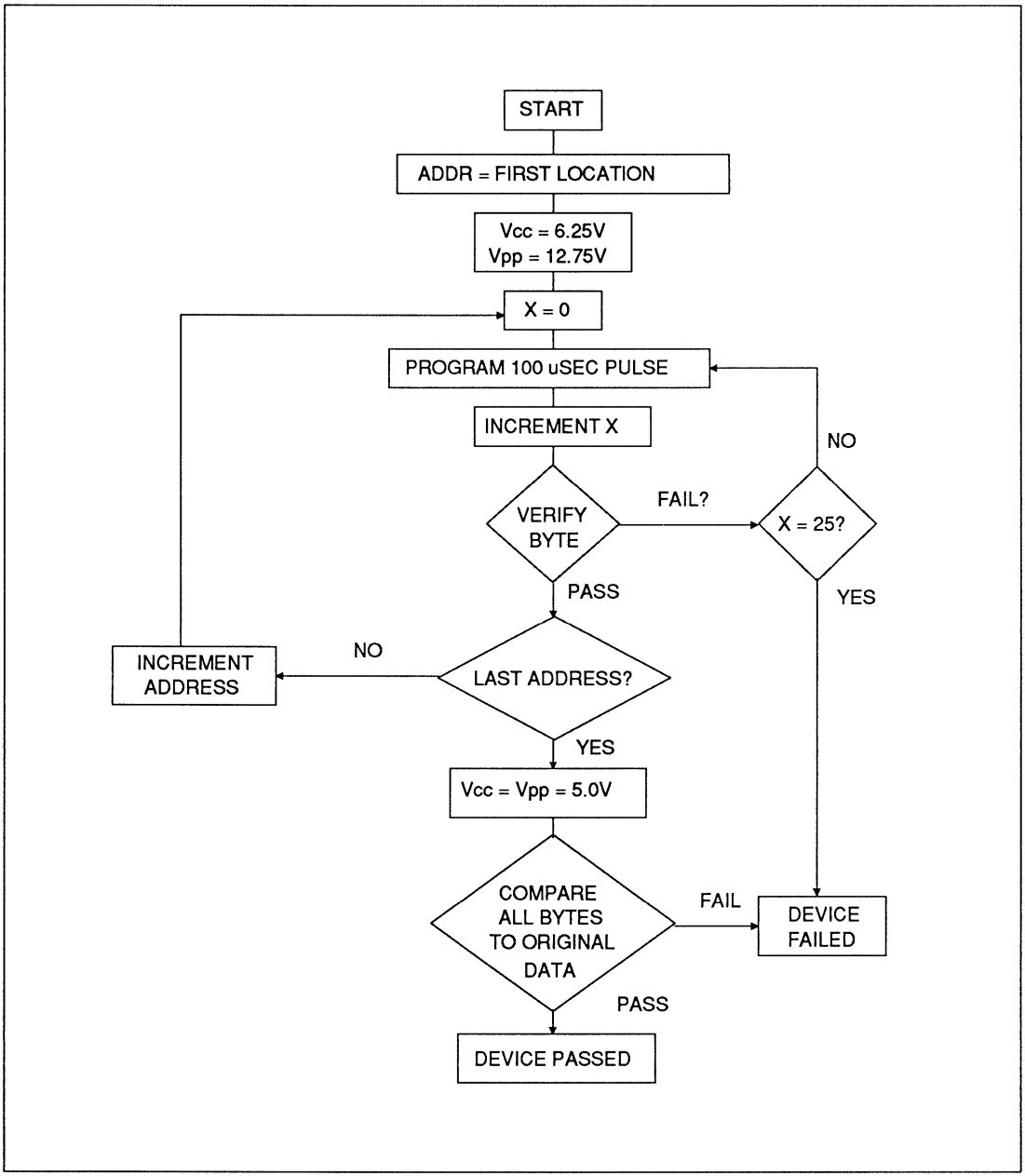


Fig. 5 QUICK PULSE ALGORITHM



READ OPERATION AND STANDBY MODES

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SIGNATURE MODE

The Signature Mode allows one to identify the IC manufacturer and the type of the part. This mode is entered as a regular Read Mode by driving low the $\overline{CE}$ and $\overline{OE}$ inputs, and in addition driving the input address bit A_9 to high-voltage VH level with all other address lines at V_{IL}.

A V_{IL} on A_0 with all other addresses at V_{IL}, gives the the binary code of the IC manufacturer on outputs O_0 to O_7.

CATALYST Code:
0 0 1 1 0 0 0 1 (31H)

A V_{IH} on A_0 with all other addresses at V_{IL}, gives the the binary code of the device type on outputs O_0 to O_7.

27HC256 / 27HC256L Code:
0 1 0 0 0 0 0 0 (40H)

PROGRAMMING MODE

After a proper erasure operation, all bits of the EPROM are in the logic one state. The device is programmed by selectively writing logic zeros into the desired bit locations. The programming mode is entered by raising $\overline{CE}$ and $\overline{OE}$ to a high level and bringing the low voltage supply pin (V_{CC}), followed by the high voltage supply pin (V_{PP}), to their respective programming levels.

After the address inputs A_0 to A_{14} and data inputs O_0 to O_7 are stabilized, $\overline{CE}$ is switched from the logic one to logic zero state to perform the programming. The particular memory cells of the addressed byte, corresponding to the 0's of the input data bits, are then programmed.

A Program Verify cycle is performed after each byte is programmed to ensure that the zero bits have been correctly written. The byte verification cycle is initiated by keeping $\overline{CE}$ at V_{IH} and switching $\overline{OE}$ from V_{IH} to V_{IL}, while all other pin voltages remain unchanged. In most cases a single 100-microsecond programming cycle is sufficient to set a memory cell in the logic zero state. The Quick Pulse algorithm is recommended as the preferred device programming operation. The CAT27HC256M is also compatible with "Intelligent Programming."

The flow charts for both the algorithms are given in Fig.4 and Fig.5.

U.V. ERASURE OPERATION FOR CERDIP EPROMS

Direct exposure to fluorescent lamps such as those used in room light fixtures, can erase the CAT27HC256M EPROM in less than three years. When exposed to direct sunlight the EPROM can be erased in less than a week.

The recommended erasure procedure is to expose the CAT27HC256M EPROM to a standard ultraviolet light with a wavelength of 2537 Angstroms. The integrated dose for proper erasure is 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 60 minutes using an ultraviolet lamp with a 1200 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes.

The maximum integrated dose a CAT27HC256M EPROM can be exposed to is 7258 Wsec/cm^2 (one week at 1200 μW/cm^2). Exposure of the device to higher U.V. doses may cause permanent damage and loss of functionality.

CAT27HC256LM - Low Power Military Temperature

32,768 x 8-BIT HIGH-SPEED CMOS EPROM

Preliminary

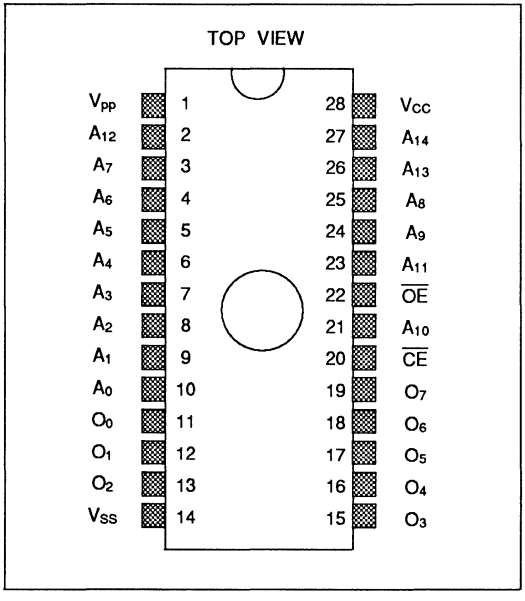
DESCRIPTION

The CAT27HC256LM is a high speed 256K UV erasable and electrically reprogrammable EPROM ideally suited for high speed applications. Any byte can be accessed in less than 70ns making this part compatible with high performance microprocessor systems by eliminating the need for speed-robbing wait states. The Quick Pulse algorithm reduces the time required to program this chip and ensures more reliable programming. The CAT27HC256LM is used in applications where fast turnaround and pattern experimentation are important requirements. The CAT27HC256LM is available in a 28-pin dual-in-line package with a transparent lid. This allows the user to expose the chip to ultraviolet light to erase the bit pattern, allowing a new pattern to be written into the device.

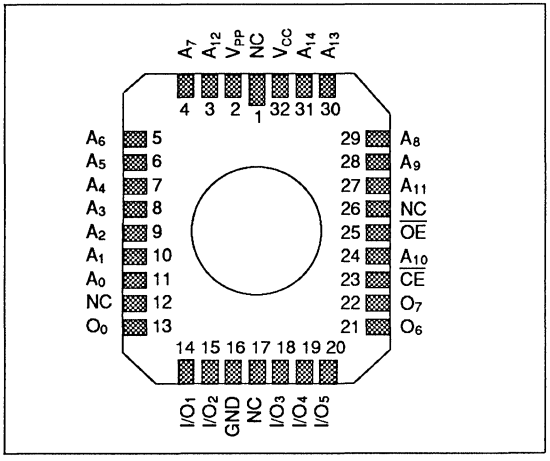
FEATURES

- Fast access time: 70/90/120ns
- 5V single power supply - read mode
- Low current requirements:
  - Active: 80mA max (CMOS levels)
  - Standby: 1mA max (CMOS levels)
- High speed programming: 100µs/byte
- TTL compatible Input/Output
- 12.5V programming voltage
- JEDEC approved 28-pin DIP and 32-pin LCC
- Electronic signature

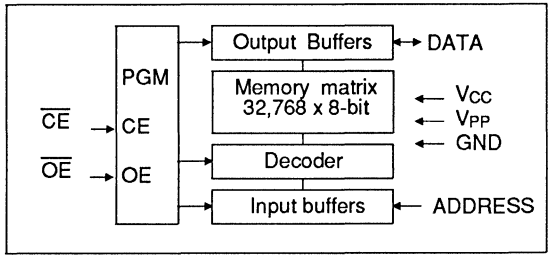
PIN CONFIGURATION 28-PIN DIP



PIN CONFIGURATION 32-PIN LCC



BLOCK DIAGRAM



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Read	V_{IL}	V_{IL}	V_{CC}	-	-	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{CC}	-	-	High-Z
Standby	V_{IH}	-	V_{CC}	-	-	High-Z
Program	V_{IL}	V_{IH}	V_{PP}	-	-	D_{IN}
Program verify	V_{IH}	V_{IL}	V_{PP}	-	-	D_{OUT}
Program inhibit	V_{IH}	V_{IH}	V_{PP}	-	-	High-Z
Signature MFG.	V_{IL}	V_{IL}	V_{CC}	V_{IL}	V_H	31H
Signature device	V_{IL}	V_{IL}	V_{CC}	V_{IH}	V_H	40H

NOTES ON THE FUNCTION TABLE

Logic Levels: **V_{IH}** = TTL Logic 1 level
V_{IL} = TTL Logic 0 level
" - " = Logic "Do not care," V_{IH} or V_{IL}

Supply Voltage: V_{PP} = Programming / high-voltage
V_{CC} = Read / low-voltage
V_H = 12.0V ±0.5V

Read: Read mode: the content of the addressed memory byte is placed on the I/O pins O_0 to O_7

Output Disable: Device is selected (active mode), programming is disabled and O_0 to O_7 output buffers are tristated (PMOS and NMOS drivers turned-off)

Standby: Device is deselected, low power dissipation

Program: Byte programming mode: logic zeros in the bit pattern driving the O_0 to O_7 data input buffers are written into the respective memory cells of the addressed byte

Program Verify: Following a programming cycle, to verify the cell contents of the memory byte being programmed (not recommended as a normal read operation)

Program Inhibit: $\overline{CE}$ set to logic one and $\overline{OE}$ set to logic one prevents programming and deselects the device

Signature MFG: Signature mode with all other addresses at V_{IL}, code of IC manufacturer (Catalyst) output on I/O pins O_0 to O_7

Signature device: Signature mode with all other addresses at V_{IL}, code of IC type output on I/O pins O_0 to O_7

PIN CAPACITANCE
(T_A = 25°C, Freq = 1.0MHz)

PARAMETER	TYPICAL	MAXIMUM	CONDITIONS
Input pin capacitance C_{IN}	4.0pF	6.0pF	V_{IN} = 0.0V
Output pin capacitance C_{OUT}	6.0pF	10.0pF	V_{OUT} = 0.0V
V_{PP} supply capacitance CV_{PP}		25.0pF	V_{PP} = 0.0V

ABSOLUTE MAXIMUM RATINGS

Temperature under bias	- 65°C to +135°C
Storage temperature	- 65°C to +135°C
All input/output voltages (except A_9)	- 0.5V to V_{CC}+0.5V
Voltage on A_9	- 1.0V to +14.0 V
Read supply voltage	- 1.0V to +7.0 V
Program voltage	- 1.0V to +14.0 V
Power dissipation, T_A = 25°C	1.0 W
DC short-circuit current, output pin	20.0 mA
Max lead solder temp., 10 seconds	300°C
(Voltages with respect to ground)	

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SUPPLY CURRENT CHARACTERISTICS (AC and DC)

(T_A = Military -55°C to 125°C)

Symbol	Parameter	Conditions	Low Power	Limit
I_{CC}	V_{CC} active current (DC)	$\overline{OE} = \overline{CE} = V_{IL}$, $V_{PP} = V_{CC}$ $A_0 - A_{14} = V_{IL}$	40mA	Max
I_{CC1}	V_{CC} active current (CMOS in @ 10MHz)	Inputs conform to V_{ILC} and V_{IHC}	80mA	Max
I_{CC2}	V_{CC} active current (TTL in @ 10MHz)	Inputs conform to AC test waveform (Fig. 1)	80mA	Max
I_{SB1}	V_{CC} standby current (CMOS in)	$\overline{CE} = V_{IHC}$	1mA	Max
I_{SB2}	V_{CC} standby current (TTL in)	$\overline{CE} = V_{IH}$	3mA	Max

DC CHARACTERISTICS <Read Operation>

(V_{CC} = 5V ± 10%, T_A = Military -55°C to 125°C)

Symbol	Parameter	Conditions	Limits			Units
			Min.	Typ.	Max.	
I_{LI}	Input leakage current	V_{IN} = 5.5V	-	-	10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V	-	-	10	µA
I_{PP1}	V_{PP} leakage current	V_{PP} = 5.5V	-	-	10	µA
V_{IH}	Input high level TTL		2.0	-	V_{CC}+0.5	V
V_{IL}	Input low level TTL		-0.5	-	0.8	V
V_{OH}	Output voltage high level	I_{OH} = -1.0 mA	2.4	-	-	V
V_{OL}	Output voltage low level	I_{OL} = 4.0 mA	-	-	0.40	V
V_{ILC}	Input low level CMOS		-0.5	-	0.30	V
V_{IHC}	Input high level CMOS		V_{CC} -0.5	-	V_{CC} +0.5	V

NOTES:
- The maximum current values are with outputs O_0 to O_7 unloaded.
- V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} .

AC CHARACTERISTICS <READ OPERATION>

(Temperature range: Military -55°C to 125°C)

Symbol	Parameter	V_{CC}±5%	27HC256-70/5		27HC256-90/5		27HC256-120/5		Unit
		V_{CC}±10%	27HC256-70		27HC256-90		27HC256-120		
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACC}	Address access time		-	70	-	90	-	120	ns
t_{CE}	$\overline{CE}$ to output delay		-	70	-	90	-	120	ns
t_{OE}	$\overline{OE}$ to output delay		-	35	-	40	-	50	ns
t_{OH} *	Output hold A, $\overline{OE}$, $\overline{CE}$		0	-	0	-	0	-	ns
t_{DF} *	$\overline{OE}$ high to out High-Z		0	35	0	40	0	50	ns

- Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer
- Input rise and fall times (10% to 90%) = 5ns
- Input pulse levels = 0.0V to 3.0V
- Input and output timing reference = 0.8V and 2.0V

* These parameters are sampled and not 100% tested.

Fig. 1 AC Test Waveforms

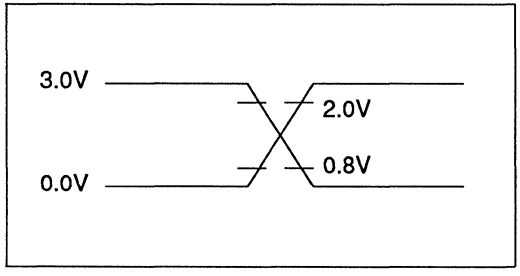
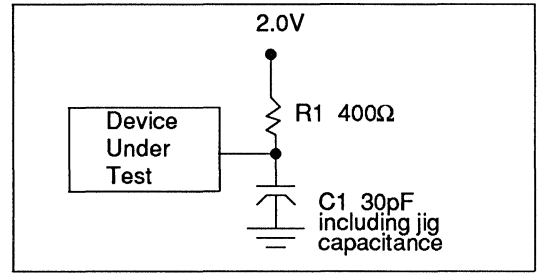
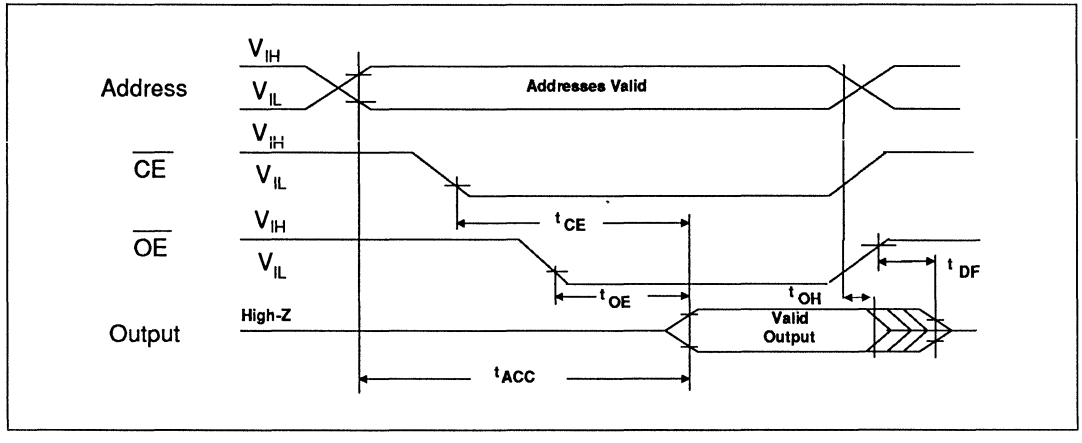


Fig. 2 Output Test Load



TIMING <Read Operation>



DC CHARACTERISTICS <Programming Operation>

(T_A = 25°C ±5°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Low-voltage supply Quick Pulse algorithm	-	6	6.25	6.5	V
V_{CC}	Low-voltage supply Intelligent algorithm	-	5.75	6.0	6.25	V
V_{PP}	High-voltage supply Quick Pulse algorithm	-	12.50	12.75	13.0	V
V_{PP}	High-voltage supply Intelligent algorithm	-	12.0	12.5	13.0	V
I_{CCP}	V_{CC} supply current Program and Verify	-	-	-	80.0	mA
I_{PP}	V_{PP} supply current Program Operation	-	-	-	40.0	mA
I_{LI}	Input leakage current	V_{IN} = 5.25V	-	-	10.0	µA
I_{LO}	Output leakage current	V_{OUT} = 5.25V	-	-	10.0	µA
V_{IL}	Input Low-Level TTL	-	-0.50	-	0.80	V
V_{ILC}	Input Low-Level CMOS	-	-0.50	-	0.30	V
V_{OL}	Output Low-Level	I_{OL} = 4.0mA	-	-	0.40	V
V_{IH}	Input High-Level TTL	-	2.0	-	V_{CC}+0.50	V
V_{IHC}	Input High-Level CMOS	-	V_{CC}-0.50	-	V_{CC}+0.50	V
V_{OH}	Output High level	I_{OH} = -1.0mA	2.4	-	-	V
V_H	High-Voltage INPUT for Signature Mode(s)	(See notes below)	11.5	-	12.50	V

NOTES:

- The maximum current values are with outputs O_0 to O_7 unloaded.
- V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

AC CHARACTERISTICS <Programming Operation>

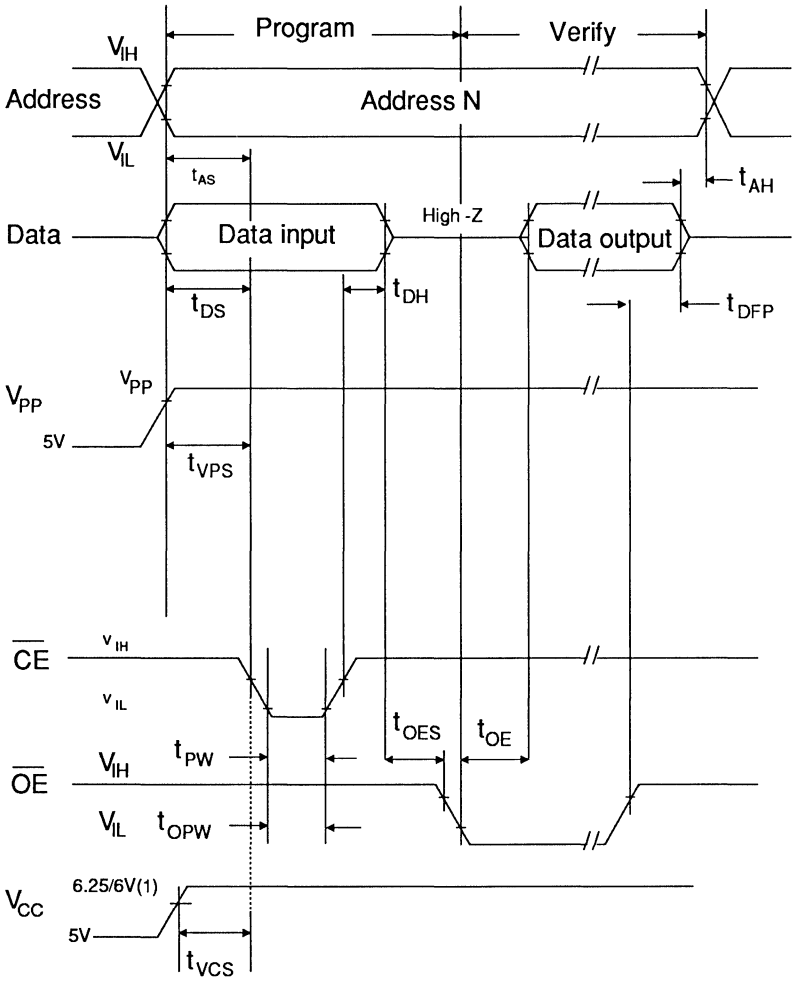
(T_A = 25°C ±5°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{AS}	Address set-up time	-	2.0	-	-	µs
t_{OES}	$\overline{OE}$ set-up time	-	2.0	-	-	µs
t_{DS}	Data set-up time	-	2.0	-	-	µs
t_{AH}	Address hold time	-	0.0	-	-	µs
t_{DH}	Data hold time	-	2.0	-	-	µs
t_{VPS}	V_{PP} set-up time	-	2.0	-	-	µs
t_{VCS}	V_{CC} set-up time	-	2.0	-	-	µs
t_{PW}	$\overline{CE}$ pulse width Quick Pulse algorithm	-	95.0	100.0	105.0	µs
t_{PW}	$\overline{CE}$ pulse width Intelligent algorithm	-	0.95	1.0	1.05	ms
t_{OPW}	$\overline{CE}$ overprogram pulse width Intelligent algorithm	-	2.85	-	78.5	ms
t_{DFP}	$\overline{OE}$ high to Output High-Z	-	0.0	-	130	ns
t_{OE}	Data valid from $\overline{OE}$	-	-	-	150	ns

NOTES:
- Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer.
- Input Rise and Fall times (10% to 90%) = 20ns.
- Input Pulse Levels = 0.0V to 3.0V.
- Input and Output Timing Reference = 0.80V and 2.0V.
- t_{DPF} is sampled and not 100% tested.

When programming the device a 0.1 microfarad capacitor is required between V_{PP} and V_{SS} to suppress spurious voltage transients which can damage the part.

TIMING <Programming Operation>



(1) Note: V_{CC} = 6.25V ±0.25V for Quick Pulse algorithm
6.00V ±0.25V for Intelligent Programming algorithm

Fig. 4 INTELLIGENT ALGORITHM

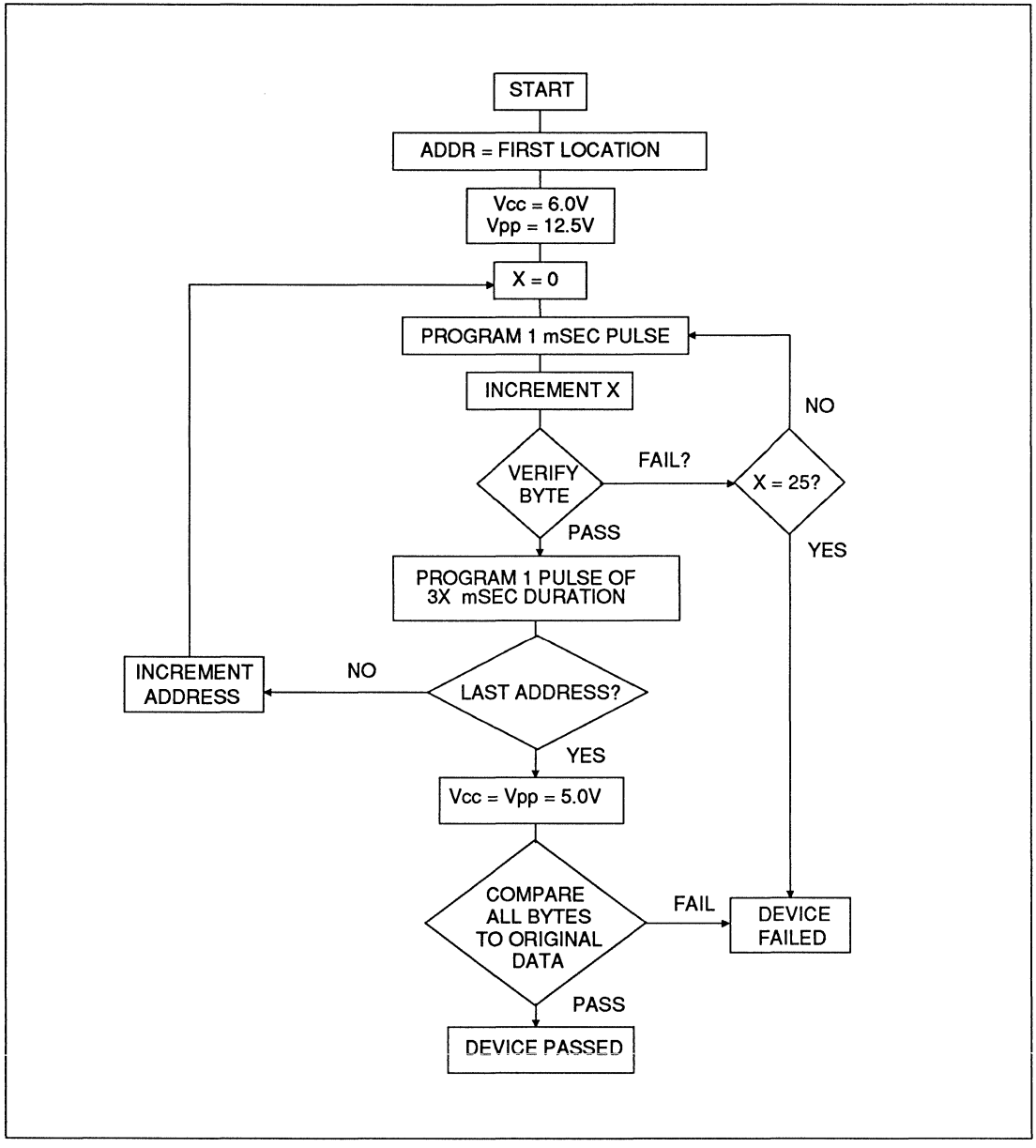
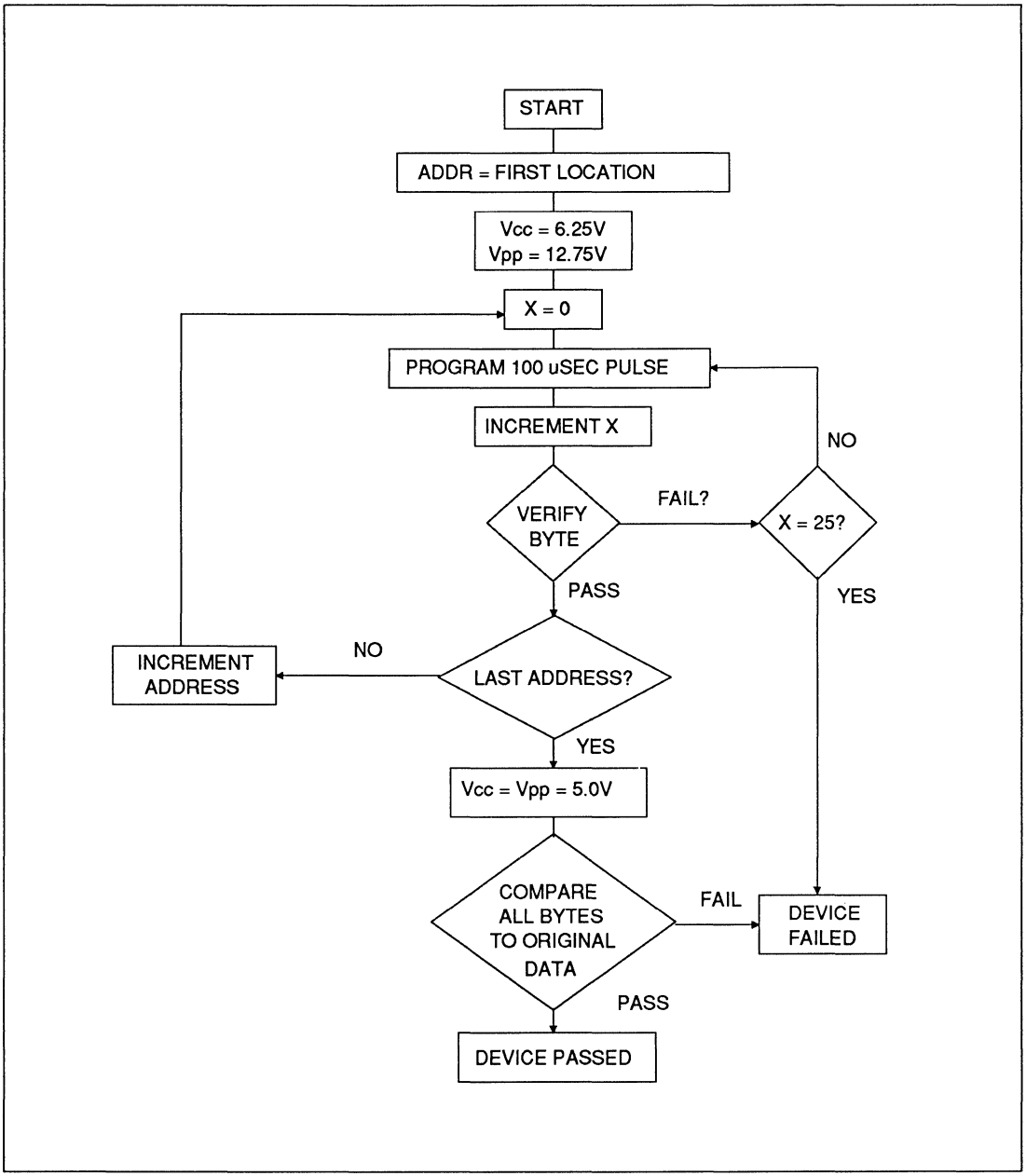


Fig. 5 QUICK PULSE ALGORITHM



READ OPERATION AND STANDBY MODES

Memory access for reading an address location is controlled by $\overline{CE}$ and $\overline{OE}$. Chip enable $\overline{CE}$ is used independently of all other input signals as the primary device selection. In the logic zero state (TTL level V_{IL}), $\overline{CE}$ powers up all inputs and enables internal circuitry. In the logic one state (CMOS level V_{IHC}) $\overline{CE}$ places the device in standby mode, all DC paths to ground are shut-off, and the power dissipation is reduced to a minimum. A logic one on Output Enable $\overline{OE}$ disables the output buffers and places the output pads in a high impedance state. Assuming that the address lines A_0 to A_{14} have been stable for a time equal to T_{ACC} - T_{OE}, the output data is available after a delay of T_{OE} from the falling edge of $\overline{OE}$.

SIGNATURE MODE

The Signature Mode allows one to identify the IC manufacturer and the type of the part. This mode is entered as a regular Read Mode by driving low the $\overline{CE}$ and $\overline{OE}$ inputs, and in addition driving the input address bit A_9 to high-voltage VH level with all other address lines at V_{IL}.

A V_{IL} on A_0 with all other addresses at V_{IL}, gives the the binary code of the IC manufacturer on outputs O_0 to O_7.

CATALYST Code:
0 0 1 1 0 0 0 1 (31H)

A V_{IH} on A_0 with all other addresses at V_{IL}, gives the the binary code of the device type on outputs O_0 to O_7.

27HC256 / 27HC256L Code:
0 1 0 0 0 0 0 0 (40H)

PROGRAMMING MODE

After a proper erasure operation, all bits of the EPROM are in the logic one state. The device is programmed by selectively writing logic zeros into the desired bit locations. The programming mode is entered by raising $\overline{CE}$ and $\overline{OE}$ to a high level and bringing the low voltage supply pin (V_{CC}), followed by the high voltage supply pin (V_{PP}), to their respective programming levels.

After the address inputs A_0 to A_{14} and data inputs O_0 to O_7 are stabilized, $\overline{CE}$ is switched from the logic one to logic zero state to perform the programming. The particular memory cells of the addressed byte, corresponding to the 0's of the input data bits, are then programmed.

A Program Verify cycle is performed after each byte is programmed to ensure that the zero bits have been correctly written. The byte verification cycle is initiated by keeping $\overline{CE}$ at V_{IH} and switching $\overline{OE}$ from V_{IH} to V_{IL}, while all other pin voltages remain unchanged. In most cases a single 100-microsecond programming cycle is sufficient to set a memory cell in the logic zero state. The Quick Pulse algorithm is recommended as the preferred device programming operation. The CAT27HC256LM is also compatible with "Intelligent Programming."

The flow charts for both the algorithms are given in Fig.4 and Fig.5.

U.V. ERASURE OPERATION FOR CERDIP EPROMS

Direct exposure to fluorescent lamps such as those used in room light fixtures, can erase the CAT27HC256LM EPROM in less than three years. When exposed to direct sunlight the EPROM can be erased in less than a week.

The recommended erasure procedure is to expose the CAT27HC256LM EPROM to a standard ultraviolet light with a wavelength of 2537 Angstroms. The integrated dose for proper erasure is 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 60 minutes using an ultraviolet lamp with a 1200 μW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes.

The maximum integrated dose a CAT27HC256LM EPROM can be exposed to is 7258 Wsec/cm^2 (one week at 1200 μW/cm^2). Exposure of the device to higher U.V. doses may cause permanent damage and loss of functionality.

CAT27512 OTP

65,536 x 8-BIT ONE-TIME PROGRAMMABLE ROM

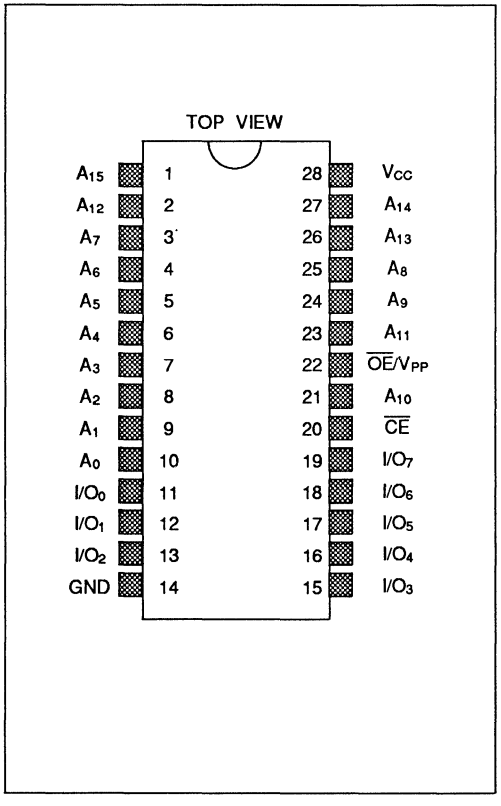
DESCRIPTION

The CAT27512 is a 65,536 x 8-bit One Time Programmable Read Only Memory (OTPROM). It is offered in both plastic DIP and PLCC packages ideally suited for high volume production. The fast access time of the CAT27512 allows it to be used in systems that utilize high performance microprocessors with no WAIT states. Two control lines eliminate bus contention in multiple bus microprocessor systems. The CAT27512 is manufactured using N-channel dual-poly silicon gate MOS technology and supplied in both 28-pin DIP and 32-pin PLCC JEDEC-approved packages.

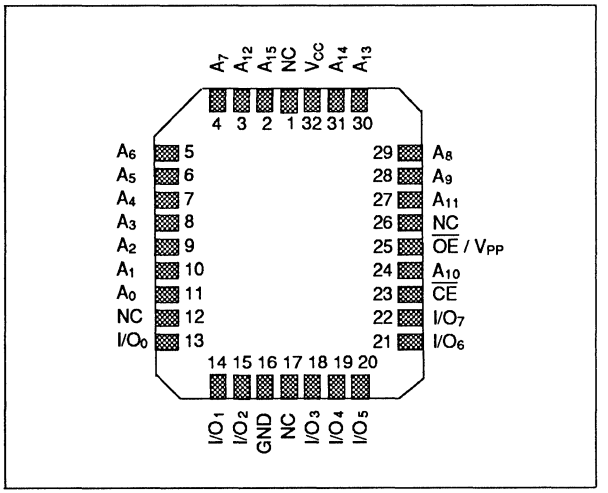
FEATURES

- 5V single power supply
- 65,536 words x 8-bit configuration
- Access time:
  - 150ns max (CAT27512-15)
  - 200ns max (CAT27512-20)
  - 250ns max (CAT27512-25)
- Current consumption:
  - Active: 100mA max
  - Standby: 30 mA max
- Fully static operation
- TTL compatible Input/Output
- 8 three-state output buffers
- Compatible with Quick Pulse™ programming
- 28-pin plastic DIP and 32-pin PLCC available

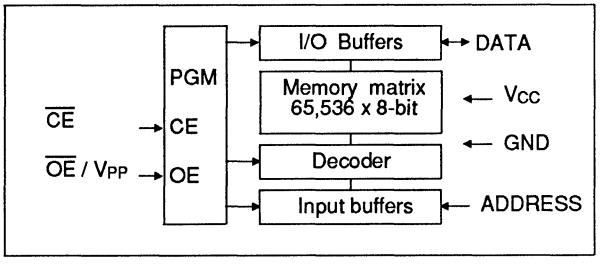
PIN CONFIGURATION 28-PIN DIP



PIN CONFIGURATION 32-PIN PLCC



BLOCK DIAGRAM



FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	+5V	D_{OUT}
Output disable	V_{IL}	V_{IH}	+5V	High impedance
Standby	V_{IH}	-	+5V	High impedance
Program	V_{IL}	12.5V	+6V	D_{IN}
Program inhibit	V_{IH}	12.5V	+6V	High impedance

The " - " means the value can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature under bias . . . . . 0°C ~ 70°C
Storage temperature . . . . . - 55°C ~ 125°C
All input/output voltages . . . . . - 0.6 ~ 13.5V
V_{CC} supply voltage . . . . . - 0.6V ~ 7V
Program voltage . . . . . - 0.6 ~ 14V
Power assembly voltage 1.5W

(Voltages with respect to ground)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS <Read Operation>

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C)

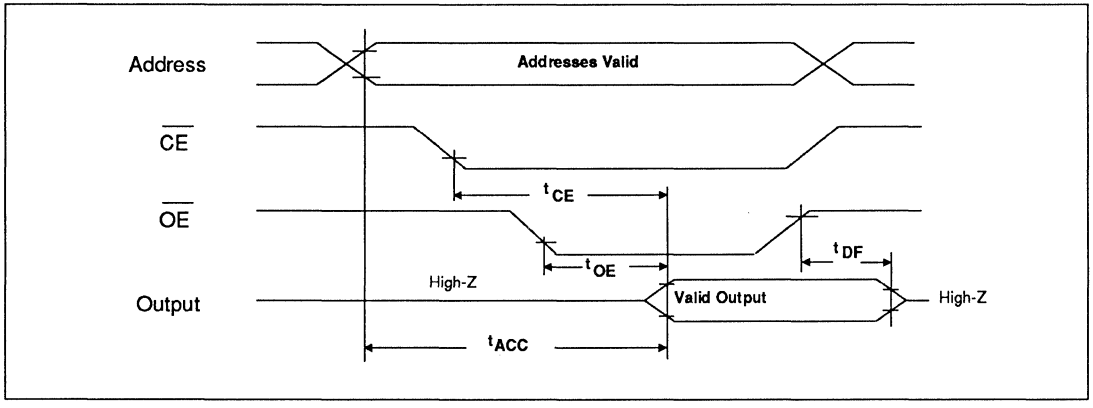
Symbol	Parameter	Conditions	Limits			Units
			Min.	Typ.	Max.	
I_{LI}	Input leakage current	V_{IN} = 5.25V	-	-	10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.25V	-	-	10	µA
I_{CC1}	V_{CC} power current (standby)	$\overline{CE}$ = V_{IH}	-	-	35	mA
I_{CC2}	V_{CC} power current (operation)	$\overline{CE}$ = V_{IL}	-	-	100	mA
V_{IH}	Input voltage "H" level	-	2.0	-	V_{CC}+1	V
V_{IL}	Input voltage "L" level	-	-0.1	-	0.8	V
V_{OH}	Output voltage "H" level	I_{OH} = -400µA	2.4	-	-	V
V_{OL}	Output voltage "L" level	I_{OL} = 2.1mA	-	-	0.45	V

AC CHARACTERISTICS <Read Operation>

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	27512-15		27512-20		27512-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACC}	Address access time	$\overline{CE}$ = $\overline{OE}/V_{PP}$ = V_{IL}	-	150	-	200	-	250	ns
t_{CE}	$\overline{CE}$ access time	$\overline{OE}/V_{PP}$ = V_{IL}	-	150	-	200	-	250	ns
t_{OE}	$\overline{OE}$ access time	$\overline{CE}$ = V_{IL}	-	70	-	70	-	100	ns
t_{DF}	Output disable time	$\overline{CE}$ = V_{IL}	0	55	0	55	0	60	ns

TIMING <Read Operation>



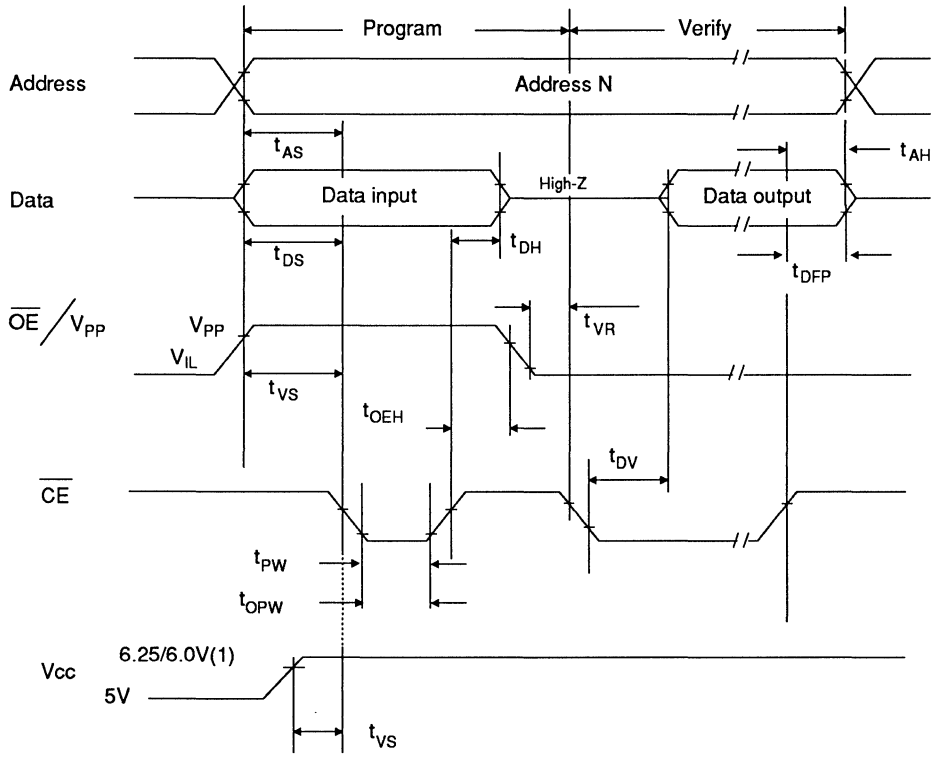
DC CHARACTERISTICS <Programming Operation>
(V_{CC} = 5.75 - 6.5V, V_{PP} = 12.5V ± 0.5V, T_A = 25°C ± 5°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{LI}	Input leakage current	V_{IN} = 5.25V	-	-	10	µA
I_{PP}	V_{PP} power current	$\overline{CE}$ = V_{IL}	-	-	50	mA
I_{CC}	V_{CC} power current	-	-	-	100	mA
V_{IH}	Input voltage "H" level	-	2.0	-	V_{CC}+1	V
V_{IL}	Input voltage "L" level	-	-0.1	-	0.8	V
V_{OH}	Output voltage "H" level	I_{OH} = -400µA	2.4	-	-	V
V_{OL}	Output voltage "L" level	I_{OL} = 2.1mA	-	-	0.45	V

AC CHARACTERISTICS <Programming Operation>
(V_{CC} = 5.75 - 6.5V, V_{PP} = 12.5V ±0.5V, T_A = 25°C ±5°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{AS}	Address set-up time	-	2	-	-	µs
t_{OEH}	$\overline{OE}$/V_{PP} hold time	-	2	-	-	µs
t_{DS}	Data set-up time	-	2	-	-	µs
t_{AH}	Address hold time	-	0	-	-	µs
t_{DH}	Data hold time	-	2	-	-	µs
t_{DFP}	$\overline{CE}$ enable to output float delay	-	0	-	130	ns
t_{VS}	V_{PP} power set-up time	-	2	-	-	µs
t_{PW}	$\overline{CE}$ initial program pulse width	V_{CC} = 6V ±0.25V	0.95	1.0	1.05	ms
t_{PW}	High speed initial program pulse width	V_{CC} = 6.25V ±0.25V	95	100	105	µs
t_{OPW}	$\overline{CE}$ overprogram pulse width	V_{CC} = 6V ±0.25V	2.85	-	78.75	ms
t_{DV}	Data valid from $\overline{CE}$	-	-	-	1	µs
t_{VR}	$\overline{OE}$/V_{PP} recovery time	-	2	-	-	µs

TIMING <Programming Operation>



(1) Note: V_{CC} = 6.25 V ± 0.25V for Quick Pulse Programming™, 6.00V ± 0.25V for Intelligent Programming™.

Programming Mode

As shipped, all bits of the OTPROM are in the logic one state. The device is programmed by selectively writing logic zeros into the desired bit locations. To enter the programming mode, V_{CC} and $\overline{OE}/V_{PP}$ must be adjusted to their programming levels, and a program write pulse must be applied to the $\overline{CE}$ pin. After the program write pulse the programmed data may be verified by enabling the outputs ($\overline{OE}$ / V_{PP} = V_{IL} and $\overline{CE}$ = V_{IL}) and comparing the written data to the read data. This device is compatible with the Intelligent Programming™ algorithm, and the Quick Pulse Programming™ algorithm. Intelligent Programming and Quick Pulse Programming are registered trademarks of Intel Corp. [9/87]

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

CAT27010

1M-BIT (128K x 8) UV EPROM

Preliminary

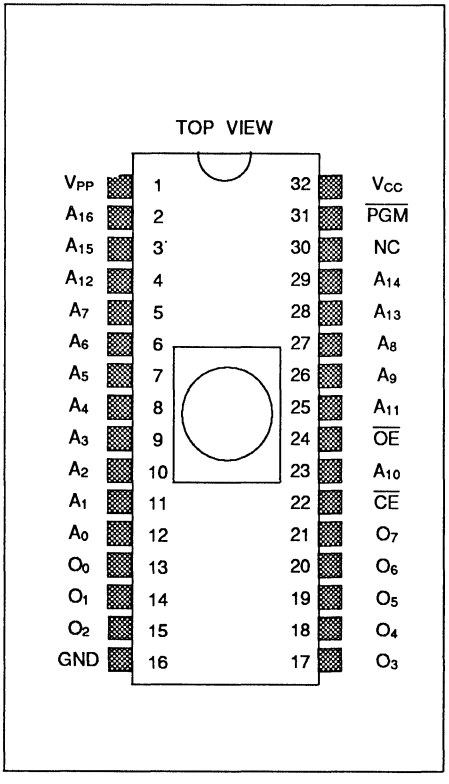
DESCRIPTION

The CAT27010 is an ultraviolet erasable and electrically programmable read-only memory. Its fast access time provides no-wait-state operation with high performance CPU's and its large capacity is ideal for storage of both sizable portions of operating systems and application software. Two control lines eliminate bus contention in multiple bus microprocessor systems. The Quick-Pulse programming algorithm reduces the time required to program the chip and ensures more reliable programming. The CAT27010 is manufactured using N-channel dual-poly silicon gate MOS technology and is supplied in a 32-pin package.

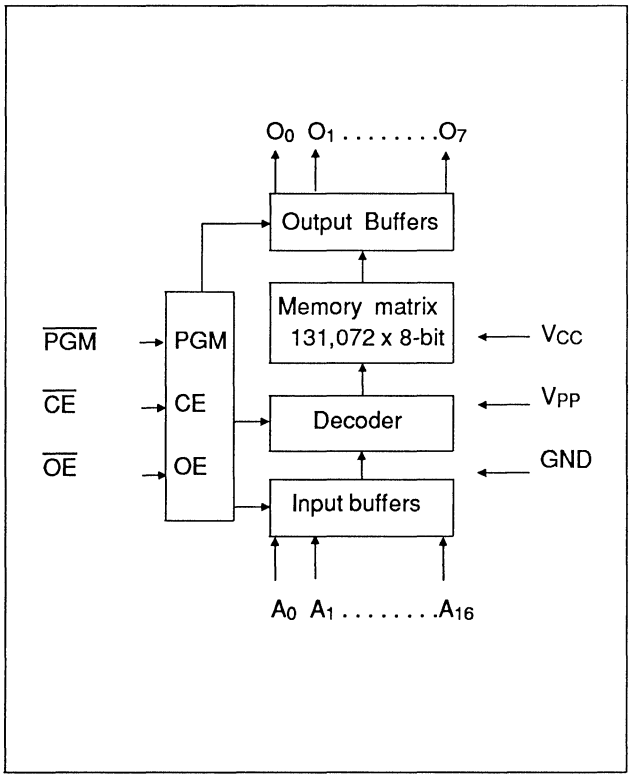
FEATURES

- 5V single power supply
- 131,072 words x 8-bit configuration
- Access time:
  - 120ns max (CAT27010-12)
  - 150ns max (CAT27010-15)
  - 200ns max (CAT27010-20)
- Power consumption:
  - Active: 100mA max
  - Standby: 35A max
- Fully static operation
- TTL compatible Input/Output
- One-Time Programmable option (OTP)

PIN CONFIGURATION



BLOCK DIAGRAM



FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (22)	$\overline{OE}$ (24)	$\overline{PGM}$ (31)	V_{PP} (1)	V_{CC} (32)	Outputs
Read	V_{IL}	V_{IL}	-	-	+5V	D_{OUT}
Output disable	V_{IL}	V_{IH}	-	-	+5V	High impedance
Standby	V_{IH}	-	-	-	+5V	High impedance
Program	V_{IL}	V_{IH}	V_{IL}	+12.75V	+6.25V	D_{IN}
Program verify	V_{IL}	V_{IL}	V_{IH}	+12.75V	+6.25V	D_{OUT}
Program inhibit	V_{IH}	-	-	+12.75V	+6.25V	High impedance

The "-" means the value can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature under bias . . . . . 0°C ~ 70°C
Storage temperature . . . . . - 55°C ~ 125°C
All input/output voltages . . . . . - 0.6V ~ 13.5V
V_{OUT} . . . . . -0.6V ~ 7V
V_{CC} supply voltage . . . . . - 0.6V~ 7V
Program Voltage . . . . . - 0.6V ~ 14V
Power assembly voltage 1.5W
(Voltages with respect to ground)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MEASUREMENT CONDITIONS

Input pulse level	0.45V and 2.4V
Input timing reference level	0.8V and 2.0V
Output load	1TTL gate + 100pF
Output timing reference level	0.8V and 2.0V

PROGRAMMING MODE

As shipped, all bits of the EPROM are in the logic one state. The device is programmed by selectively writing logic zeros into the desired bit locations. To enter the programming mode, V_{CC} and V_{PP} must be adjusted to their programming levels, and a program write pulse must be applied to the $\overline{PGM}$ pin. After the program write pulse, the programmed data may then be verified by enabling the outputs ($\overline{OE}$ = $\overline{CE}$ = V_{IL}), then comparing the written data to the read data. This device is compatible with the Intelligent Programming™ algorithm, and the Quick Pulse Programming™ algorithm. Intelligent Programming and Quick Pulse Programming are registered trademarks of Intel Corp. [9/87]

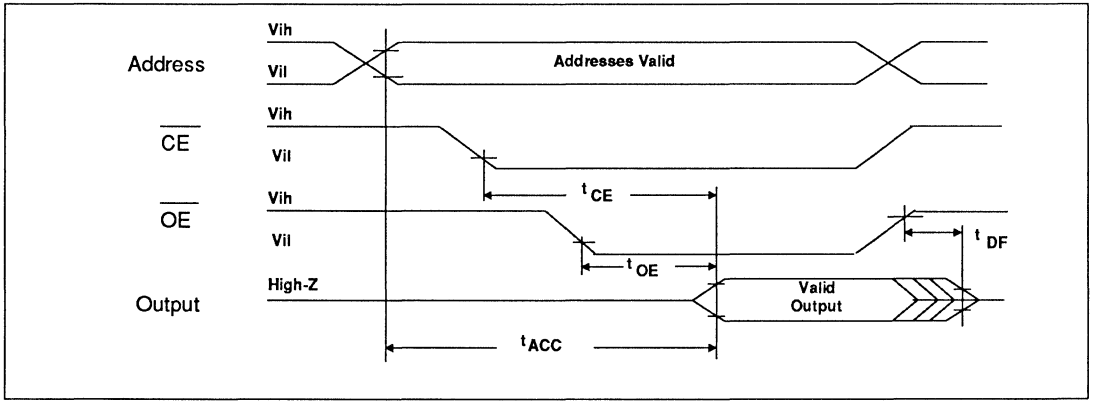
DC CHARACTERISTICS <Read Operation>
(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{LI}	Input leakage current	V_{IN} = 5.25V	-	-	10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.25V	-	-	10	µA
I_{CC1}	V_{CC} power current (standby)	$\overline{CE}$ = V_{IH}	-	-	35	mA
I_{CC2}	V_{CC} power current (operation)	$\overline{CE}$ = V_{IL}	-	-	100	mA
V_{IH}	Input voltage "H" level	-	2.0	-	V_{CC}+1	V
V_{IL}	Input voltage "L" level	-	-0.1	-	0.8	V
V_{OH}	Output voltage "H" level	I_{OH} = -400µA	2.4	-	-	V
V_{OL}	Output voltage "L" level	I_{OL} = 2.1mA	-	-	0.45	V
I_{PP}	Program power current	V_{PP} = V_{CC}	-	-	10	µA

AC CHARACTERISTICS <Read Operation>
(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	27010-12		27010-15		27010-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACC}	Address access time	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	-	120	-	150	-	200	ns
t_{CE}	$\overline{CE}$ access time	$\overline{OE}$ = V_{IL}	-	120	-	150	-	200	ns
t_{OE}	$\overline{OE}$ access time	$\overline{CE}$ = V_{IL}	-	50	-	60	-	70	ns
t_{DF}	Output disable time	$\overline{CE}$ = V_{IL}	0	40	0	50	0	55	ns

TIMING <Read Operation>



DC CHARACTERISTICS <Programming Operation>
(V_{CC} = 6.25V± 0.25V, V_{PP} = 12.75V ± 0.25V, T_A = 25°C ± 5°C)

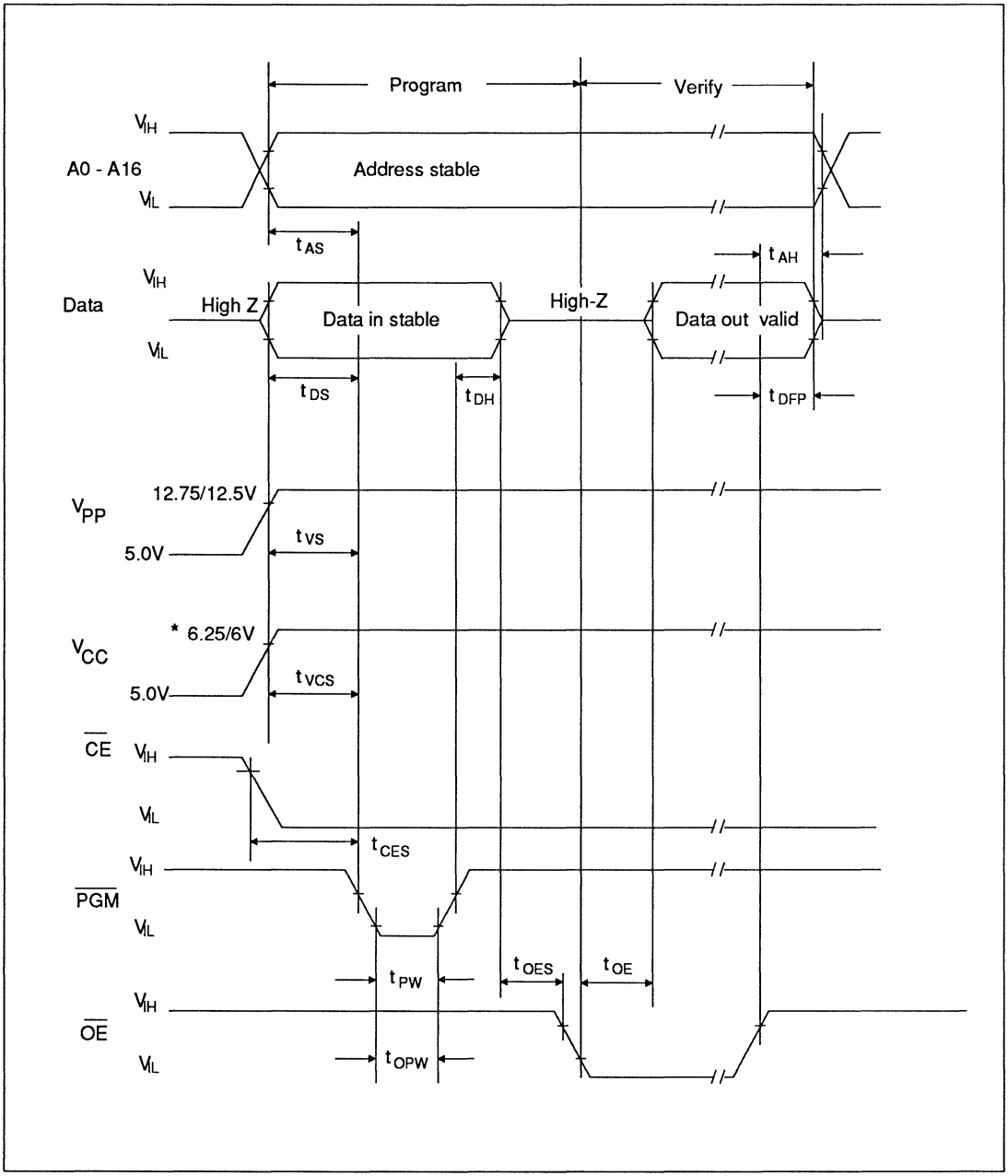
Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{LI}	Input leakage current	V_{IN} = 5.25V	-	-	10	µA
I_{PP}	V_{PP} power current	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}	-	-	50	mA
I_{CC}	V_{CC} power current	-	-	-	100	mA
V_{IH}	Input voltage "H" level	-	2.0	-	V_{CC}+1	V
V_{IL}	Input voltage "L" level	-	-0.1	-	0.8	V
V_{OH}	Output voltage "H" level	I_{OH} = -400µA	2.4	-	-	V
V_{OL}	Output voltage "L" level	I_{OL} = 2.1mA	-	-	0.45	V

AC CHARACTERISTICS <Programming Operation>
(V_{CC} = 6.25V± 0.25V, V_{PP} = 12.75V ± 0.25V, T_A = 25°C ± 5°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{AS}	Address set-up time	-	2	-	-	µs
t_{OES}	$\overline{OE}$ set-up time	-	2	-	-	µs
t_{DS}	Data set-up time	-	2	-	-	µs
t_{AH}	Address hold time	-	0	-	-	µs
t_{DH}	Data hold time	-	2	-	-	µs
t_{DFP}	Output enable to output float delay	-	0	-	130	ns
t_{VS}	V_{PP} power set-up time	-	2	-	-	µs
t_{PW}	Intelligent program pulse width	V_{CC} = 6V ±0.25	0.95	1.0	1.05	ms
	Quick-pulse program pulse width	V_{CC} = 6.25V ±0.25	95	100	105	µs
t_{OPW}	$\overline{PGM}$ overprogram pulse width	V_{CC} = 6V ±0.25	2.85	-	78.75	ms
t_{CES}	$\overline{CE}$ set-up time	-	2	-	-	µs
t_{OE}	Data valid from $\overline{OE}$	-	-	-	150	ns

These specifications may be changed without notification.

TIMING <Programming Operation>



Caution: Exceeding 14V on V_{PP} may permanently damage the device.

*** Note:** V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V for Quick Pulse Programming ™
V_{CC} = 6.00V ± 0.25V; V_{PP} = 12.50V ± 0.50V for Intelligent Programming ™

CAPACITANCE

(T_A = 25°C , F = 1MHz)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
C_{IN}	Input capacitance	V_{IN} = 0V	-	4	6	pF
C_{OUT}	Output capacitance	V_{OUT} = 0V	-	8	12	pF

NOTES

CAT27C210
1 M-BIT (64K x 16) CMOS UV EPROM

DESCRIPTION

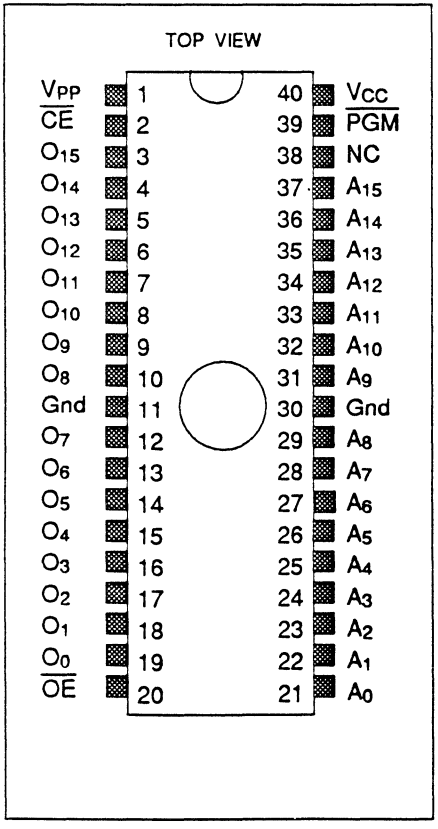
The CAT27C210 is a 1,048,576 bit high-speed UV erasable EPROM featuring low power CMOS operation, 16 three-state output buffers, and a charge-pump circuit to raise the EPROM cell's gate voltage during programming. Two control lines eliminate bus contention in microprocessor systems. The CAT27C210 is packaged in a 40 pin CERDIP (a plastic OTP) or a 44 pin PLCC (OTP).

FEATURES

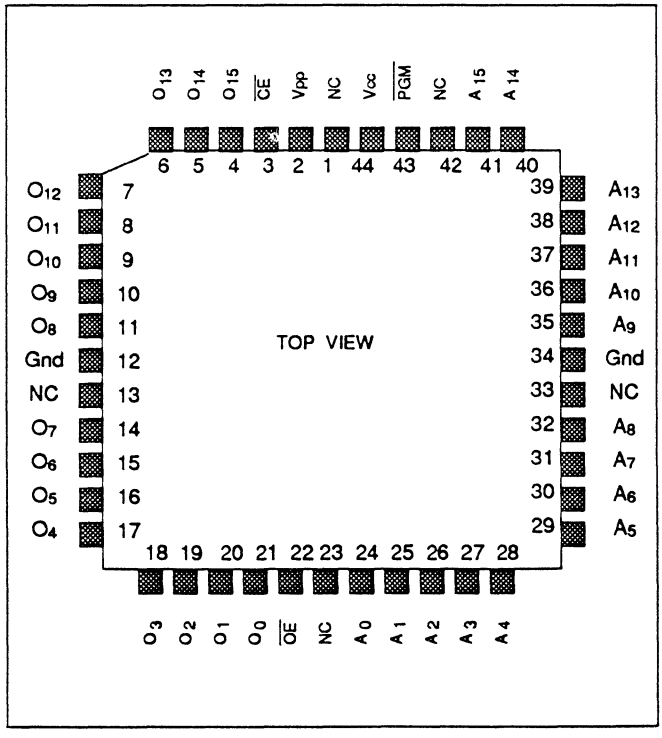
- Fast read access time: 150ns max
- Low CMOS power dissipation:
  - Active: 50mA max
  - Standby: 100µA max
- 16 three state output buffers
- ESD protection greater than 2000V
- 65,536 words x 16 bits configuration
- TTL compatible input/output
- One-Time-Programmable option
- Pin/functional equivalent to Intel 27210
- 40 pin plastic DIP (OTP), 40 pin CERDIP, or 44 pin Plastic Leaded Chip Carrier (OTP) available.
- Compatible with Quick Pulse™ programming
- Single 5V ± 10% power supply

PIN CONFIGURATIONS

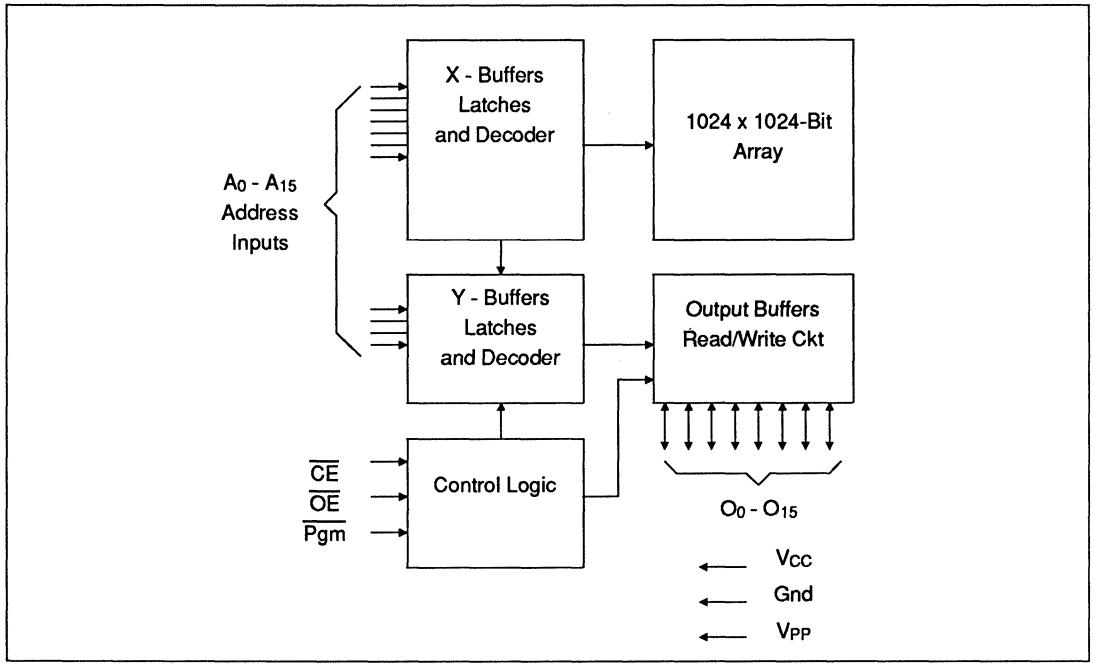
40-Pin DIP



44-Pin PLCC



BLOCK DIAGRAM



PIN NAMES

$A_0 - A_{15}$	Address inputs
$O_0 - O_{15}$	Data outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{PGM}$	Write enable
V_{CC}	Read voltage supply
V_{SS}	Ground
V_{PP}	Program voltage supply

CAPACITANCE

(T_A= 25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Limits Typ. max.	Unit
C_{OUT}	Output capacitance	V_{OUT} = 0V	10	pF
C_{IN}	Input capacitance	V_{IN} = 0V	6	pF
C_{VPP}	V_{PP} supply capacitance	V_{PP} = 0V	25	pF

Note: These parameters are periodically sampled and are not 100% tested.

FUNCTION TABLE

Mode \ Pins	V_{PP}	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A0	A9	I/O
Read	V_{CC}	V_{IL}	V_{IL}	-	-	-	DOUT
Output disable	V_{CC}	V_{IL}	V_{IH}	-	-	-	HI Z
Standby	V_{CC}	V_{IH}	-	-	-	-	HI Z
Program	V_{PP}	V_{IL}	V_{IH}	V_{IL}	-	-	D_{IN}
Program verify	V_{PP}	V_{IL}	V_{IL}	V_{IH}	-	-	D_{OUT}
Program inhibit	V_{PP}	V_{IH}	-	-	-	-	HI Z
Signature MFG	V_{CC}	V_{IL}	V_{IL}	-	V_{IL}	V_{ID}	0031H
Signature device	V_{CC}	V_{IL}	V_{IL}	-	V_{IH}	V_{ID}	0007H

The " - " means the values can be either V_{IL} or V_{IH}

NOTES:

Logic levels	V_{IH} = TTL logic 1 level. V_{IL} = TTL logic 0 level
Supply voltage	V_{PP} = programming (high V) V_{ID} = signature voltage (high V)
Read	Read mode, the content of the addressed memory word is placed on the I/O pins O_0 to O_{15}
Output disable	Device is selected (active mode), programming is disabled and O_0 to O_{15} output buffers are tri-stated (PMOS and NMOS drivers are turned off)
Standby	Device is deselected, low power dissipation.
Program	Word programming mode, logic zeros in the bit pattern driving the O_0 to to O_{15} input buffers are written into the respective memory cells of the addressed word.
Program verify	Following a programming cycle, to verify the cell contents of the memory word being programmed (not recommended as normal read operation)
Program inhibit	$\overline{CE}$ set to logic 1 level prevents programming and deselects the device.
Signature MFG	Signature mode, code of IC manufacturer output on I/O pins O_0 to O_{15}
Signature Device	Signature mode, code of IC type output on I/O pins O_0 to O_{15}

ABSOLUTE MAXIMUM RATINGS *

Temperature under bias	-10°C to +85°C
Storage temperature	-65°C to +125°C
Voltage on all input/output pins	-1.0 to +7V
Voltage on A9	-1.0 to 14.0V
D.C. output current, short-curcuit	20mA
Program supply voltage V_{PP}	-1.0 to 14.0V
Read supply voltage V_{CC}	-1.0 to +7V
Max power dissapation (T_A = 25°C)	1.0W
Max lead soldering temp (10 seconds)	260°C

(Voltage with respect to ground)

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*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION AND STANDBY MODES

Memory access for reading an address location is controlled by $\overline{CE}$ and $\overline{OE}$. Chip enable $\overline{CE}$ is used independently of all other input signals as the primary device selection. In the logic 0 state (TTL level V_{IL}), $\overline{CE}$ powers up all input and sensitive internal circuitry. In the logic 1 state (TTL level V_{IH}), $\overline{CE}$ places the device in standby mode, all DC paths to ground are shut-off and the power dissipation is reduced to a minimum. A logic 1 on the output enable $\overline{OE}$ (output enable) disables the output buffers and places the output pads in a high impedance state. Assuming that the address lines A_0 to A_{15} have been stable for a time equal to $t_{ACC} - t_{OE}$, the output data is available after a delay of t_{OE} from the falling edge of $\overline{OE}$.

SIGNATURE MODE

The signature mode allows the programmer to identify the manufacturer and the type of the part. This mode is entered as a regular READ mode by driving low the $\overline{CE}$ and $\overline{OE}$ inputs, in addition to driving the input address bit A_9 to high voltage V_{IH} level.

A logic low level (V_{IL}) on the address pin A_0 outputs on O_0 to O_{15} the binary code of the IC manufacturer.

CATALYST Code: 0000 0000 0011 0001 (0031H)

A logic high level (V_{IH}) on the address pin A_0 outputs the device type on O_0 to O_{15}

Device type: 0000 0000 0000 01110 (007H)

AC CHARACTERISTICS <READ OPERATION>

$T_A = 0^oC$ to 70^oC

Symbol	Parameter	V_{CC}±5%	27C210-15/5		27C210-17/5		27C210-20/5		27C210-25/5		Unit
		V_{CC}±10%	27C210-15		27C210-17		27C210-20		27C210-25		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACC}	Address access time		-	150	-	170	-	200	-	250	ns
t_{CE}	$\overline{CE}$ to output delay		-	150	-	170	-	200	-	250	ns
t_{OE}	$\overline{OE}$ to output delay		-	60	-	70	-	80	-	100	ns
t_{DF}	$\overline{OE}$ high to out High-Z		-	35	-	40	-	50	-	60	ns

NOTES:

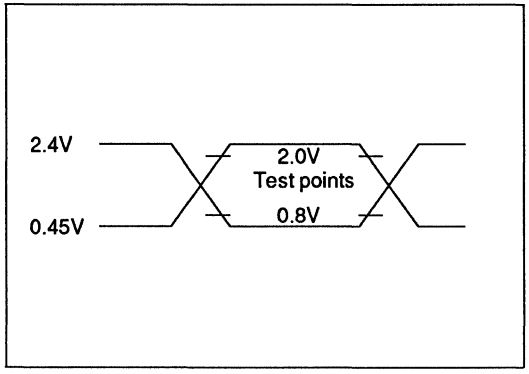
Output floating (OUT High-Z) is defined as the state where the external data line is no longer driven by the output buffer. The load condition for this measurement is shown in Figure 2. on page 3-35.

Input rise and fall times (10 to 90%) 20ns

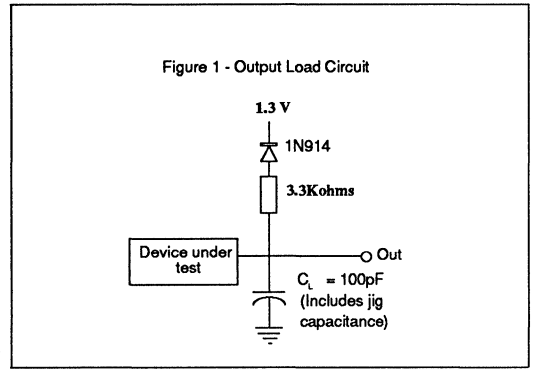
Input pulse levels . . . . . 0.45 to 2.4V

Input and output timing reference . . . . . 0.80 to 2.0V

AC TESTING IN/OUT WAVEFORM



AC TEST LOAD CIRCUIT



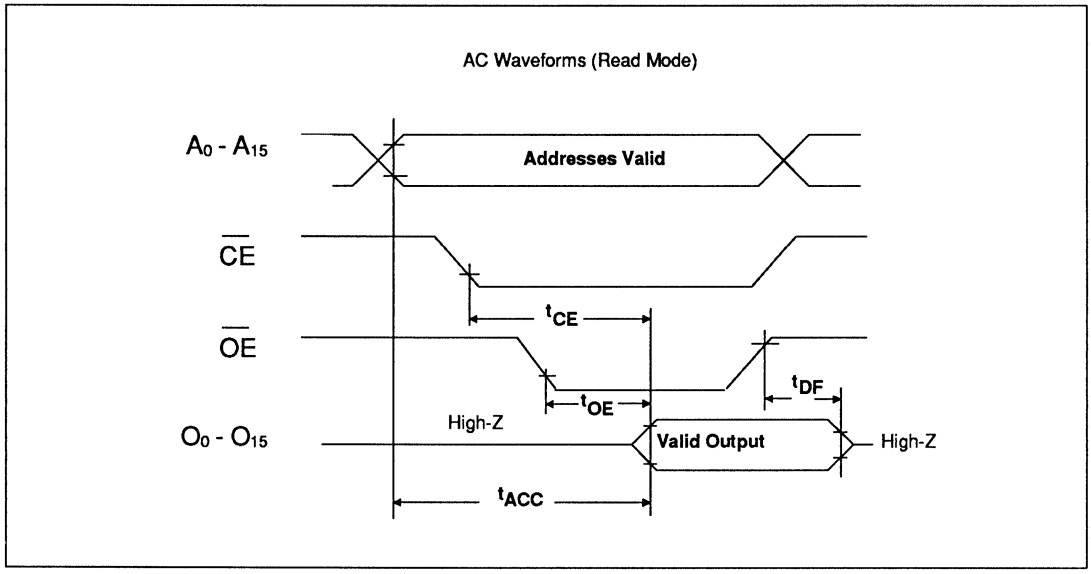
DC CHARACTERISTICS <Read and Standby Modes>

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC1}	V_{CC} active current (CMOS)	f = DC to 5MHz			50	mA
I_{CC2}	V_{CC} active current (TTL)	f = DC to 5MHz			60	mA
I_{SB1}	V_{CC} current (standby, TTL)	$\overline{CE} = V_{IH}$			1	mA
I_{SB2}	V_{CC} current (standby, CMOS)	$\overline{CE} = V_{IH}$			100	µA
I_{LI}	Input load current	V_{IN} = 5.5V			1.0	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V			1.0	µA
V_{IH}	High level input voltage TTL		2.0		V_{CC} +0.5	V
V_{IHC}	High level input voltage CMOS		V_{CC} -0.5		V_{CC} +0.5	V
V_{IL}	Low level input voltage TTL		-0.5		0.8	V
V_{ILC}	Low level input voltage CMOS		-0.5		0.3	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V
I_{PP}	V_{PP} load current (READ)	V_{PP} = 5.5V			1.0	µA

The maximum current values are with outputs O_0 to O_{15} unloaded.
V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

AC TIMING <Read Operation>



Programming Mode

As shipped, all the bits of the CAT27C210 are in the logic one state. The device is programmed by selectively writing logic zeros into the desired bit locations. To enter the programming mode, V_{CC} and V_{PP} must be adjusted to their programming levels, $\overline{CE}$ pulled to V_{IL}, and a program write pulse applied to the $\overline{PGM}$ pin. After the program write pulse, the programmed data may then be verified by enabling the outputs ($\overline{OE}$=V_{IL}, $\overline{CE}$ = V_{IL}, and $\overline{PGM}$ = V_{IH}), then comparing the written data to the read data. This device is compatible with the Intelligent™ and the Quick Pulse Programming™ algorithms. Intelligent Programming and Quick Pulse Programming are registered trademarks of Intel Corp.[9/87]

CAUTION: Exceeding 14V on the V_{PP} pin may permanently damage the device.

DC CHARACTERISTICS <Programming Mode>

(V_{CC} = +5V ±10%, T_A = 25°C ± 5°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Low voltage supply Quick Pulse program		6.0		6.5	V
V_{CC}	Low voltage supply Intelligent program		5.75		6.25	V
V_{PP}	High voltage supply Quick Pulse program		12.5		13.0	V
V_{PP}	High voltage supply Intelligent program		12.0		13.0	V
I_{CCP}	V_{CC} current, program + verify	see note			45	mA
I_{PP}	V_{PP} current, program operation				40	mA
I_{LI}	Input load current	V_{IN} = 5.5V			1.0	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V			1.0	µA
V_{IL}	Input low level TTL		-0.5		0.8	V
V_{ILC}	Input low level CMOS		-0.5		0.3	V
V_{OL}	Output low level	I_{OL} = 2.4			0.45	V
V_{IH}	Input high level TTL		2.0		V_{CC}+0.5	V
V_{IHC}	Input high level CMOS		V_{CC}-0.5		V_{CC}+0.5	V
V_{OH}	Output high level	I_{OH} = -400µA	2.4			V
V_{ID}	A_9 signature level		11.5		12.5	V

NOTES:

- The maximum current values are with outputs O_0 to O_{15} unloaded.

- V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

AC CHARACTERISTICS <Programming>

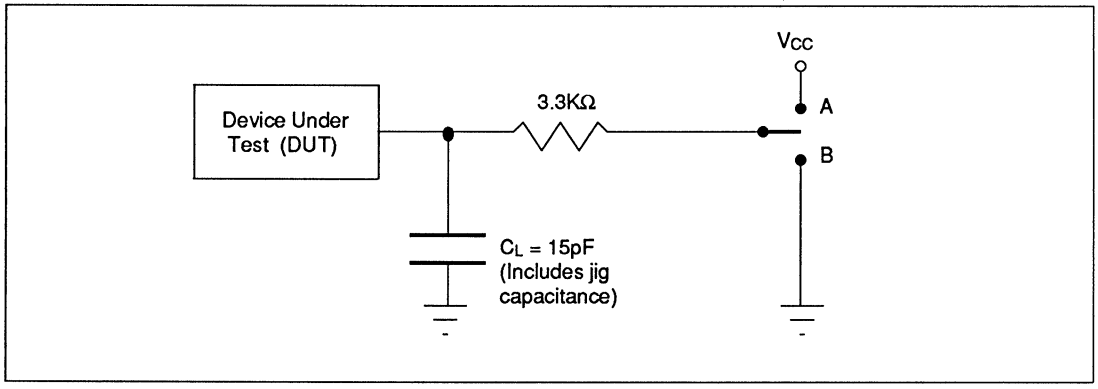
(T_A = 25°C ± 5°C)

Symbol	Parameter	Conditions	Limits Min.	Typ.	Max.	Unit
t_{AS}	Address set-up time		2.0			µs
t_{OES}	$\overline{OE}$ set-up time	Input rise and fall times: 10%-90% = 20ns Input pulse levels: 0.45 to 2.4V Input timing reference level: 0.8 to 2.0V Output timing reference	2.0			µs
t_{DS}	Data set-up time		2.0			µs
t_{AH}	Address hold time		0.0			µs
t_{DH}	Data hold time		2.0			µs
t_{CES}	$\overline{CE}$ set-up time		2.0			µs
t_{VPS}	V_{PP} set-up time		2.0			µs
t_{VCS}	V_{CC} set-up time		2.0			µs
t_{PW}	$\overline{PGM}$ pulse width, Intelligent Pgm.		0.95	1.0	1.05	ms
	$\overline{PGM}$ pulse width, Quick Pulse Pgm.		0.95	100	105	µs
t_{OPW}	$\overline{PGM}$-overprogram pulse-Intelligent Pgm		2.85	-	78.5	ms
t_{OE}	Data valid from $\overline{OE}$		-		130	ns
t_{DFP}	$\overline{OE}$ high to output High-Z		-		150	ns

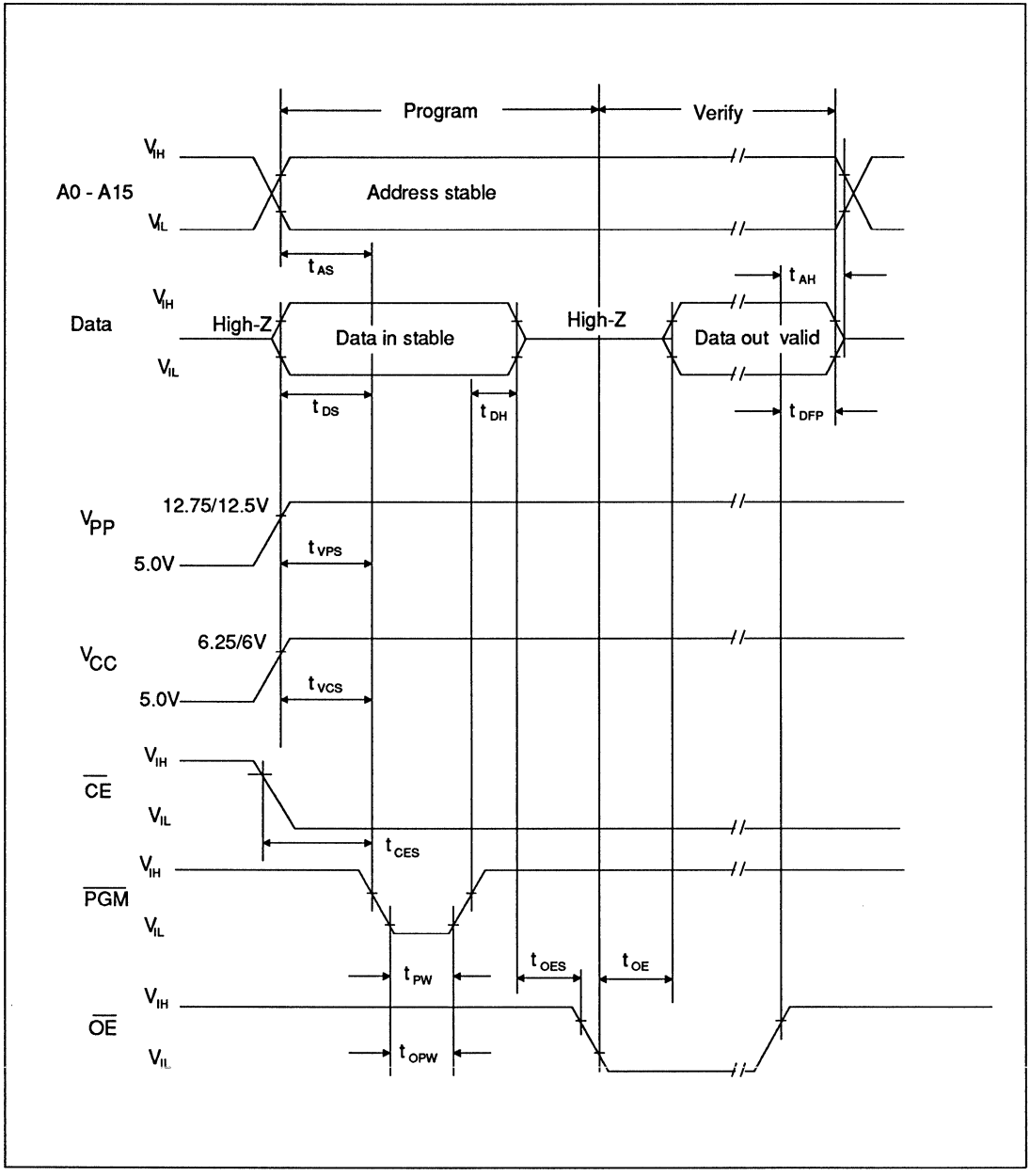
NOTE:

Output floating (OUTPUT High-Z) is defined as the state where the external data line is no longer driven by the output buffer. t_{DF} and t_{DFP} are measured with the switch in position "A" when DUT output starts at logic "0." t_{DF} and t_{DFP} are measured with the switch in position "B" when the DUT output starts at logic "1."

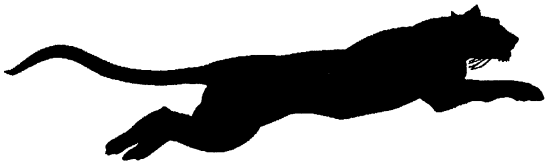
Figure 2. t_{DF} and t_{DFP} High-Z TEST LOAD CIRCUIT



AC TIMING <Programming Operation>



NOTE: When programming the device a 0.1 microfarad capacitor is required between V_{PP} and V_{SS} to suppress spurious voltage transients which can damage the part.



SECTION 3

E^2PROMS - Parallel & Serial

COMMERCIAL TEMPERATURE RANGE

HIGH ENDURANCE

INDUSTRIAL TEMPERATURE RANGE

CAT28C16A
2K x 8 BIT CMOS E^2PROM

DESCRIPTION

The CAT28C16A is a fast, low power, 5V-only CMOS E^2EPROM requiring a simple interface for in-system programming.

On-chip address and data latches, self-timed write cycle with auto-erase and V_{CC} power up/down write protection eliminate additional timing and protection hardware. Data polling is provided to allow the user to minimize write cycle time.

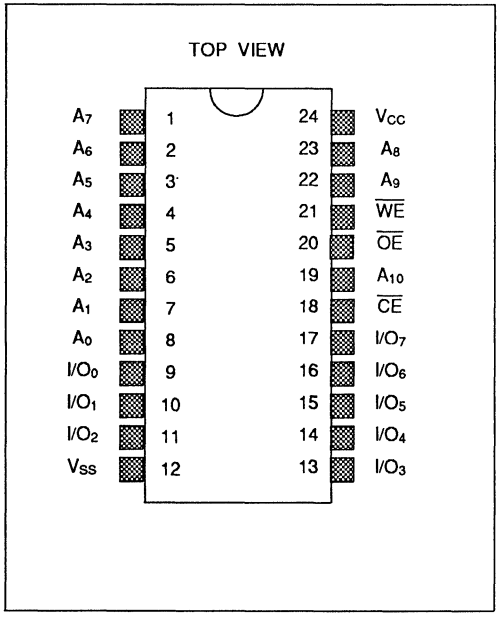
The CAT28C16A is fabricated in reliable floating gate CMOS technology. It is designed for up to 10,000 write cycles and 10 years data retention.

FEATURES

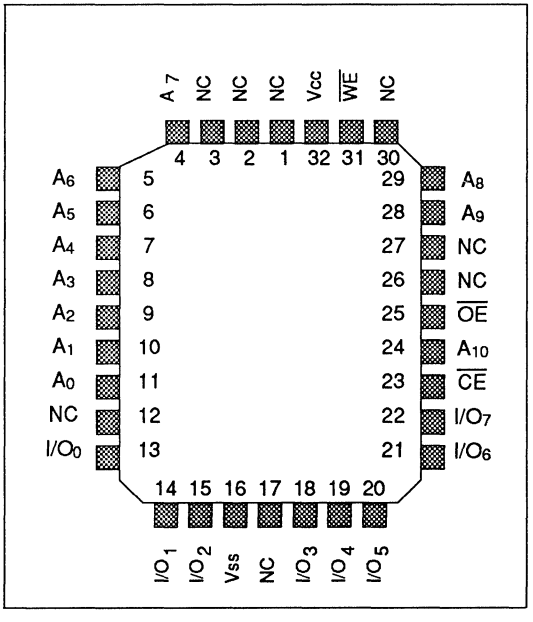
- Access time: 200ns
- Low CMOS power:
  - Active: 25mA max
  - Standby: 100µA max
- 5V-only operation
- Simple write operation:
  - On-chip address and data latches
  - Self-timed write cycle with auto-erase
  - Data polling
  - Power up/down write protection
- Fast write cycle time
  10ms max byte write
- Reliable floating gate CMOS technology
- JEDEC approved 24-pin DIP, Small Outline, and 32-pin PLCC packages available
- Power-up inadvertent write protection

PIN CONFIGURATION

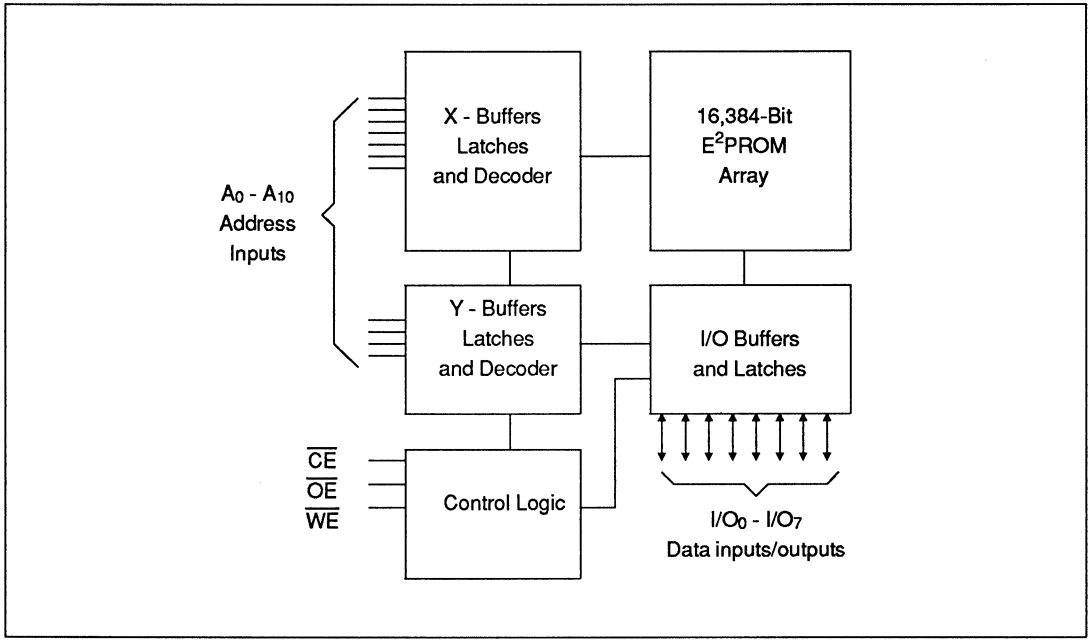
24-Pin DIP and S.O.



32-Pin PLCC



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{10}	Address inputs
I/O_0 - I/O_7	Data inputs/outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
V_{CC}	+5V
V_{SS}	Ground

CAPACITANCE

(T_A = 25°C, f = 1.0MHz, V_{CC} = 5V)

Symbol	Parameter	Conditions	Limits Typ. max.	Unit
$C_{I/O}$	Input/Output capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input capacitance	V_{IN} = 0V	6	pF

Note: These parameters are periodically sampled and are not 100% tested.

ABSOLUTE MAXIMUM RATINGS *

Temperature under bias . . . . . -40°C to +85°C
Storage temperature . . . . . -65°C to +150°C
Voltage on any input pin relative to V_{SS} . . . . . -0.5 to +7V
Voltage on any output pin relative to V_{SS} . . . . . -0.5 to V_{CC} +0.5V
D.C. output current 5mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, CAT2816A T_A = 0°C to +70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC}	V_{CC} current (operating, TTL)	$\overline{CE}$=$\overline{OE}$=V_{IL}, f=6.7MHz, all I/O's = open			35	mA
I_{CCC}	V_{CC} current (operating, CMOS)	$\overline{CE}$=$\overline{OE}$=V_{ILC}*, f=6.7MHz, all I/O's = open			25	mA
I_{SB}	V_{CC} current (standby, TTL)	$\overline{CE}$=V_{IH} All I/O's open			1	mA
I_{SBC}	V_{CC} current (standby, CMOS)	$\overline{CE}$=V_{IHC}** All I/O's open			100	µA
I_{LI}	Input leakage current	V_{IN} = GND to V_{CC}			10	µA
I_{LO}	Output leakage current	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.3		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V
V_{WI}	V_{CC} trip voltage for write protection		3.0	3.5		V

NOTE:
* V_{ILC} = -0.3V to +0.3V
** V_{IHC} = V_{CC} - 0.3V to V_{CC} + 1.0V

MODE SELECTION

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Read	L	H	L	D_{OUT}	ACTIVE
Byte write	L	⌐‾_‾¬	H	D_{IN}	ACTIVE
Standby and write inhibit	H	X	X	High-Z	STANDBY
Write inhibit	X	X	L		
Write inhibit	X	H	X		
Chip erase	L	L	12V	High-Z	ACTIVE

AC CHARACTERISTICS - TEST CONDITIONS

Parameter	Conditions
Input pulse level	0.4 to 2.4V
Input rise and fall times	10ns
Input/output timing reference level	'0' = 0.8V, '1' = 2.0V
Output load	C_L = 100pF, 1 TTL gate

AC CHARACTERISTICS <Read Cycle>

(CAT2816A T_A = 0°C to +70°C, V_{CC} = +5V ±10%)

Symbol	Parameter	28C16A-20		Units
t_{RC}	Read cycle time	200		ns
t_{CE}	$\overline{CE}$ access time		200	ns
t_{AA}	Address access time		200	ns
t_{OE}	$\overline{OE}$ access time		80	ns
t_{LZ}	$\overline{CE}$ low to active output	10		ns
t_{OLZ}	$\overline{OE}$ low to active output	10		ns
t_{HZ}	$\overline{CE}$ high to high-Z output	10	55	ns
t_{OHZ}	$\overline{OE}$ high to high-Z output	10	55	ns
t_{OH}	Output hold from address change	20		ns

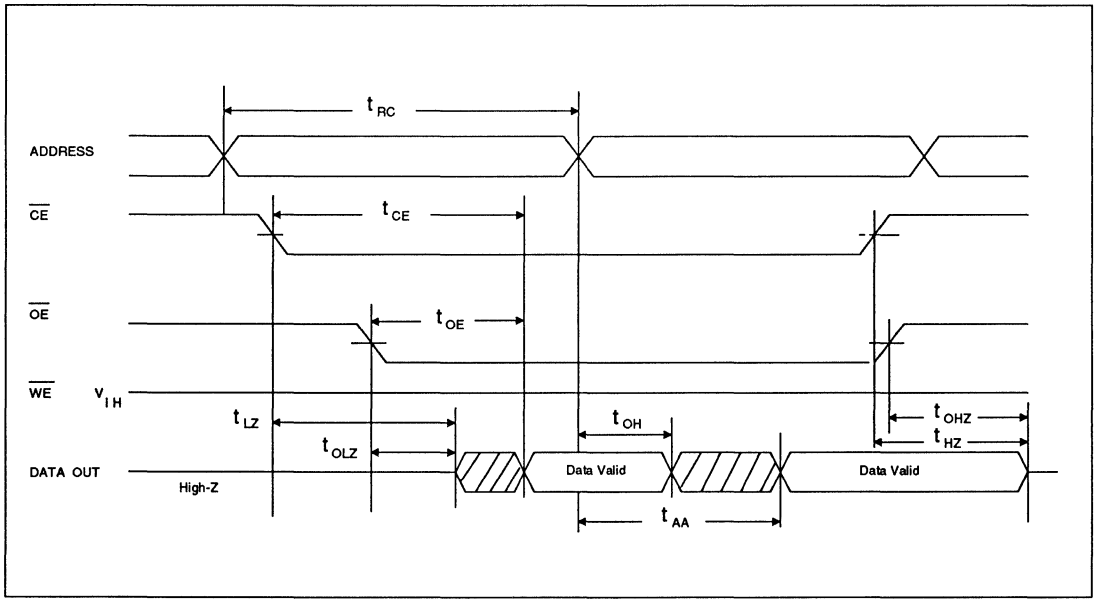
AC CHARACTERISTICS <Write Cycle>

(CAT2816A T_A = 0°C to +70°C, V_{CC} = +5V ±10%)

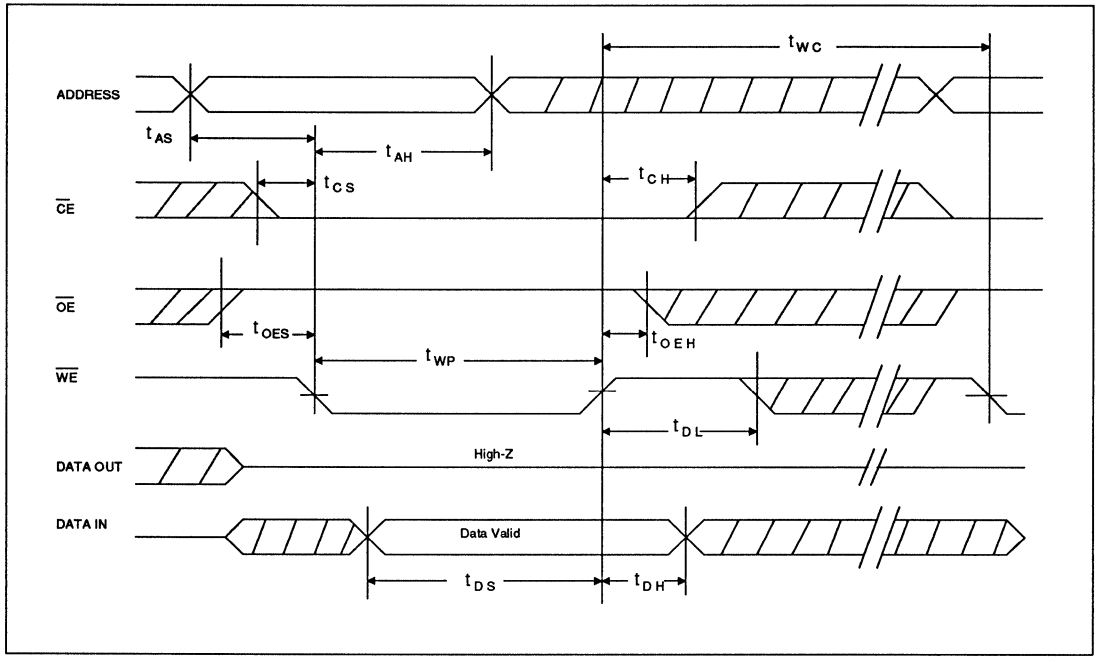
Symbol	Parameter	28C16A-20 Min.	28C16A-20 Max.	Units
t_{WC}	Write cycle time		10	ms
t_{AS}	Address setup time	10		ns
t_{AH}	Address hold time	100		ns
t_{CS}	Write setup time	0		ns
t_{CH}	Write hold time	0		ns
t_{CW} *	$\overline{CE}$ pulse time	150		ns
t_{OES}, t_{OEH}	$\overline{OE}$ setup time, $\overline{OE}$ hold time	15		ns
t_{WP} *	$\overline{WE}$ pulse width	150		ns
t_{DL}	Data latch time	50		ns
t_{DS}	Data setup time	50		ns
t_{DH}	Data hold time	10		ns
t_{INIT}	Write inhibit period after power-up	5	20	ms

NOTE: * A write pulse of less than 20ns duration will not initiate a write cycle.

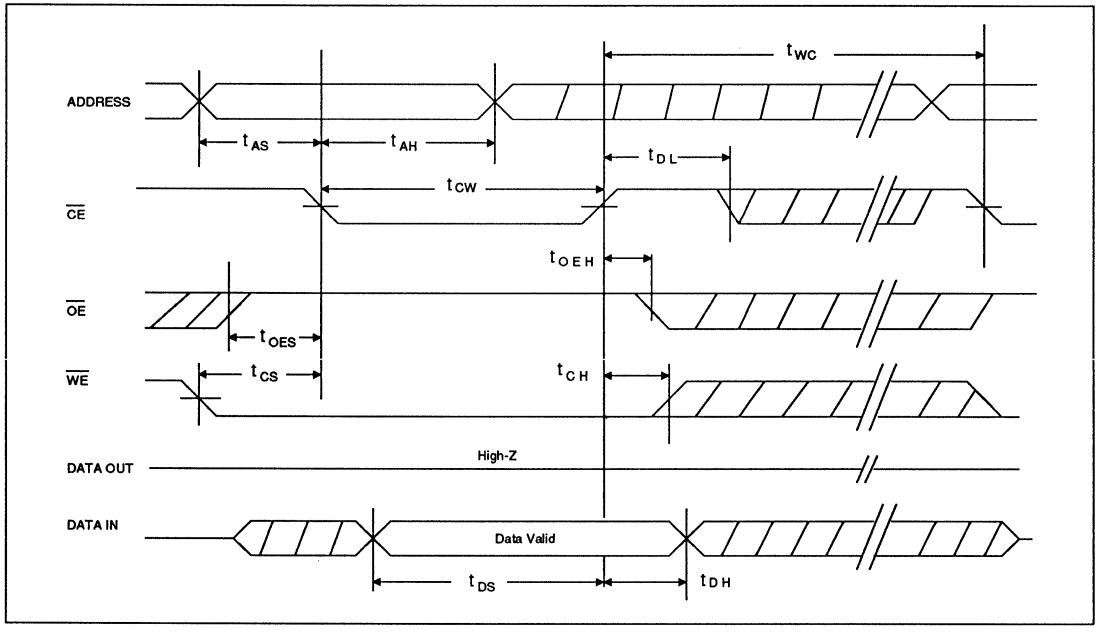
TIMING <Read Cycle>



TIMING <$\overline{WE}$ Controlled Write Cycle>



TIMING <$\overline{CE}$ Controlled Write Cycle>



PIN DESCRIPTIONS

ADDRESSES (A_0-A_{10})
The Address inputs are used to select an 8-bit memory location during read and write cycles.

CHIP ENABLE ($\overline{CE}$)
The Chip Enable input must be held LOW to enable read and write cycles. When $\overline{CE}$ is held HIGH, the device is deselected and power consumption is reduced to the standby level.

OUTPUT ENABLE ($\overline{OE}$)
The Output Enable input, in conjunction with $\overline{CE}$, determines whether the device outputs are high impedance, or output data during a read cycle.

DATA IN/DATA OUT (I/O_0-I/O_7)
Data is output to the I/O pins during a read cycle, and written into the device from the I/O pins during a write cycle.

WRITE ENABLE ($\overline{WE}$)
The Write Enable input, in conjunction with $\overline{CE}$ and $\overline{OE}$, initiates a write cycle.

DEVICE OPERATION

READ
Device data is output to the data bus when both $\overline{OE}$ and $\overline{CE}$ are LOW. The data bus is high impedance when either $\overline{CE}$ or $\overline{OE}$ go HIGH. This 2-line control architecture can be used to eliminate bus contention in a system environment.

BYTE WRITE
A write cycle is initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. Both $\overline{CE}$ and $\overline{WE}$ controlled write cycles can be executed, i.e., the address is latched on the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last, while data is latched on the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and times itself to completion.

DATA POLLING
Data polling is provided to indicate the completion of a byte write cycle. Once a byte write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O_7 (I/O_0-I/O_6 are indeterminate) until the programming cycle is complete. Upon completion of the self-timed byte write cycle all I/Os will output true data during a read cycle.

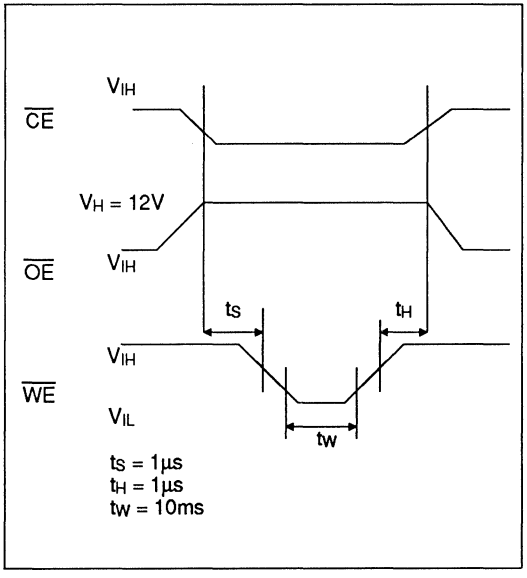
FALSE WRITE PROTECTION
(1) The CAT28C16AI has an on-chip V_{CC} sense circuit which disables the internal write circuitry whenever V_{CC} is less than 3.0V.

(2) During power-up, write operations are inhibited for 5ms to 20ms after V_{CC} reaches 3.0V. Read cycles are not affected during this initialization-period.

(3) Write cycles are inhibited if $\overline{OE}$ is LOW, or $\overline{CE}$ or $\overline{WE}$ are HIGH.

(4) A write pulse of less than 20ns duration will not initiate a write cycle.

CHIP ERASE
The entire memory can be set to 1's by setting $\overline{CE}$ LOW, $\overline{OE}$ to 12V, and pulsing $\overline{WE}$ LOW for 10ms.



CAT28C16AI - Industrial Temperature
2K x 8 BIT CMOS E^{2}PROM

DESCRIPTION

The CAT28C16AI is an industrial temperature, fast, low power, 5V-only CMOS E^{2}EPROM requiring a simple interface for in-system programming.

On-chip address and data latches, self-timed write cycle with auto-erase and V_{CC} power up/down write protection eliminate additional timing and protection hardware. Data polling is provided to allow the user to minimize write cycle time.

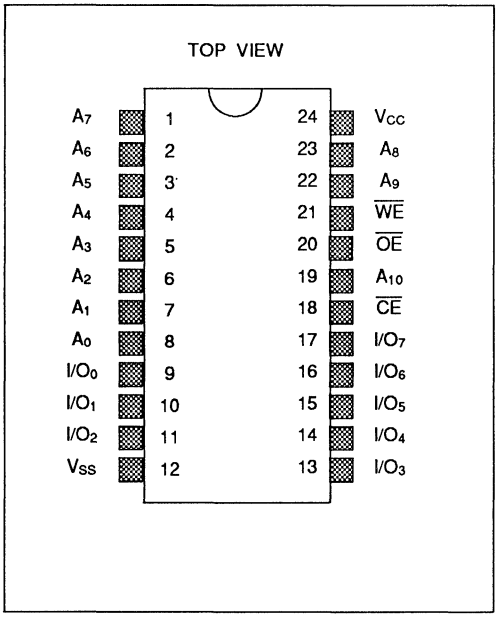
The CAT28C16AI is fabricated in reliable floating gate CMOS technology. It is designed for up to 10,000 write cycles and 10 years data retention.

FEATURES

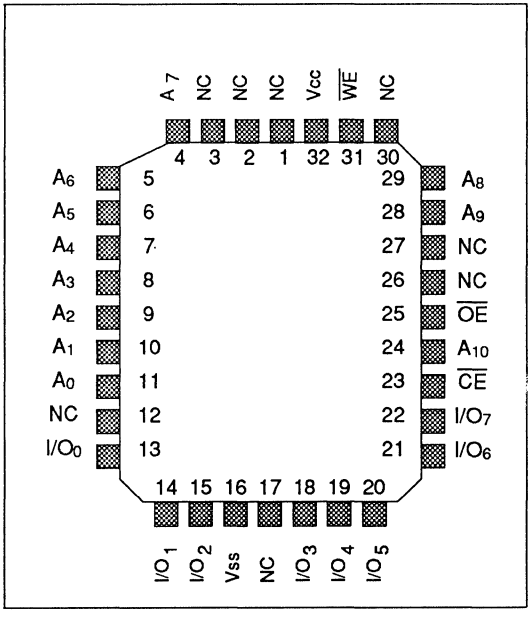
- Access time: 200ns
- Low CMOS power:
  - Active: 25mA max
  - Standby: 100µA max
- 5V-only operation
- Simple write operation:
  - On-chip address and data latches
  - Self-timed write cycle with auto-erase
  - Data polling
  - Power up/down write protection
- Fast write cycle time
  10ms max byte write
- Operating Range -40°C to 80°C
- Reliable floating gate CMOS technology
- JEDEC approved 24-pin DIP,Small Outline, and 32-pin PLCC packages available
- Power-up inadvertent write protection

PIN CONFIGURATION

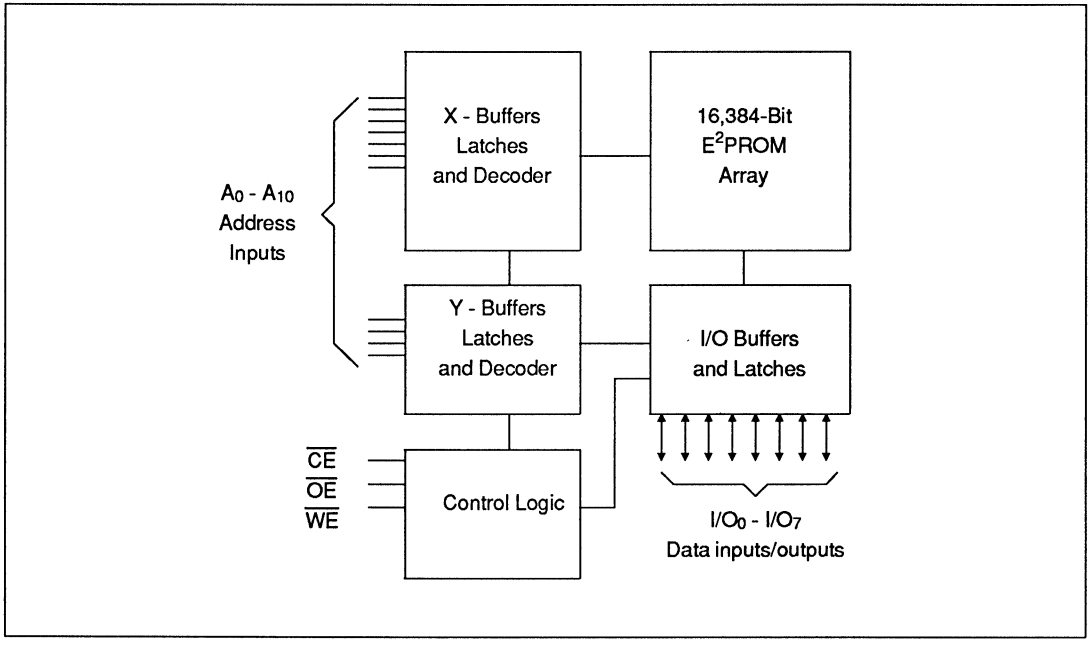
24-Pin DIP and S.O.



32-Pin PLCC



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{10}	Address inputs
I/O_0 - I/O_7	Data inputs/outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
V_{CC}	+5V
V_{SS}	Ground

CAPACITANCE

(T_A = 25°C, f = 1.0MHz, V_{CC} = 5V)

Symbol	Parameter	Conditions	Limits Typ. max.	Unit
$C_{I/O}$	Input/Output capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input capacitance	V_{IN} = 0V	6	pF

Note: These parameters are periodically sampled and are not 100% tested.

ABSOLUTE MAXIMUM RATINGS *

Temperature under bias . . . . . -40°C to +85°C
Storage temperature . . . . . -65°C to +150°C
Voltage on any input pin relative to V_{SS} . . . . . -0.5 to +7V
Voltage on any output pin relative to V_{SS} . . . . . -0.5 to V_{CC} +0.5V
D.C. output current 5mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, CAT2816AI T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC}	V_{CC} current (operating, TTL)	$\overline{CE}$=$\overline{OE}$=V_{IL}, f=6.7MHz, all I/O's = open			35	mA
I_{CCC}	V_{CC} current (operating, CMOS)	$\overline{CE}$=$\overline{OE}$=V_{ILC}*, f=6.7MHz, all I/O's = open			25	mA
I_{SB}	V_{CC} current (standby, TTL)	$\overline{CE}$=V_{IH} All I/O's open			1	mA
I_{SBC}	V_{CC} current (standby, CMOS)	$\overline{CE}$=V_{IHC}** All I/O's open			100	µA
I_{LI}	Input leakage current	V_{IN} = GND to V_{CC}			10	µA
I_{LO}	Output leakage current	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.3		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V
V_{WI}	V_{CC} trip voltage for write protection		3.0	3.5		V

NOTE:
* V_{ILC} = -0.3V to +0.3V
** V_{IHC} = V_{CC} - 0.3V to V_{CC} + 1.0V

MODE SELECTION

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Read	L	H	L	D_{OUT}	ACTIVE
Byte write	L	⌐‾⌐	H	D_{IN}	ACTIVE
Standby and write inhibit	H	X	X	High-Z	STANDBY
Write inhibit	X	X	L		
Write inhibit	X	H	X		
Chip erase	L	L	12V	High-Z	ACTIVE

AC CHARACTERISTICS - TEST CONDITIONS

Parameter	Conditions
Input pulse level	0.4 to 2.4V
Input rise and fall times	10ns
Input/output timing reference level	'0' = 0.8V, '1' = 2.0V
Output load	C_L = 100pF, 1 TTL gate

AC CHARACTERISTICS <Read Cycle>

(CAT2816AI T_A = -40°C to +85°C, V_{CC} = +5V ±10%)

Symbol	Parameter	28C16A-20		Units
t_{RC}	Read cycle time	200		ns
t_{CE}	$\overline{CE}$ access time		200	ns
t_{AA}	Address access time		200	ns
t_{OE}	$\overline{OE}$ access time		80	ns
t_{LZ}	$\overline{CE}$ low to active output	10		ns
t_{OLZ}	$\overline{OE}$ low to active output	10		ns
t_{HZ}	$\overline{CE}$ high to high-Z output	10	55	ns
t_{OHZ}	$\overline{OE}$ high to high-Z output	10	55	ns
t_{OH}	Output hold from address change	20		ns

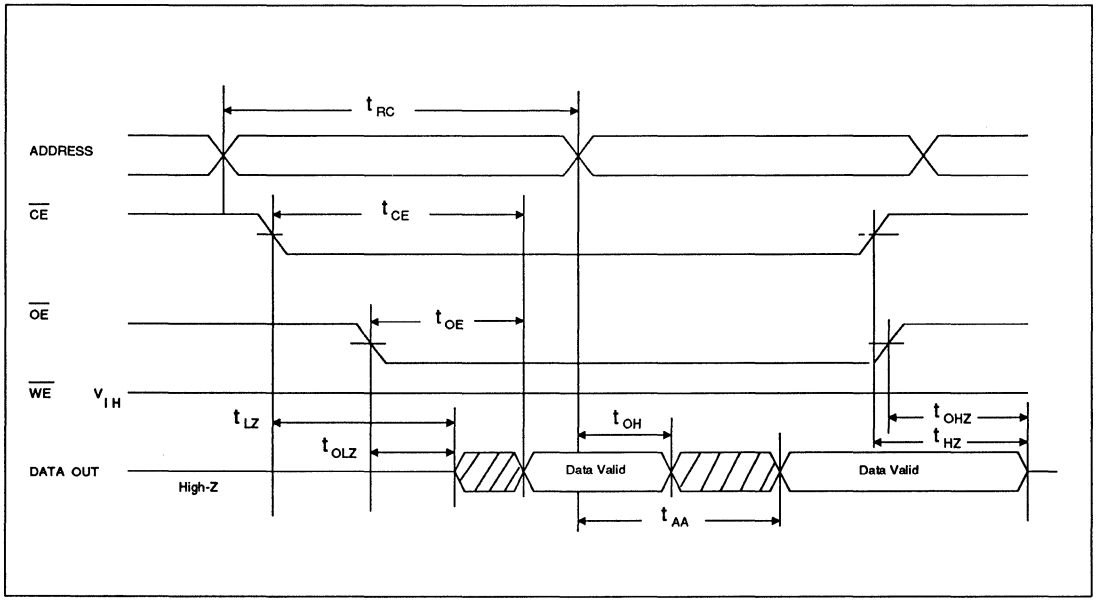
AC CHARACTERISTICS <Write Cycle>

(CAT2816AI T_A = - 40°C to +85°C, V_{CC} = +5V ±10%)

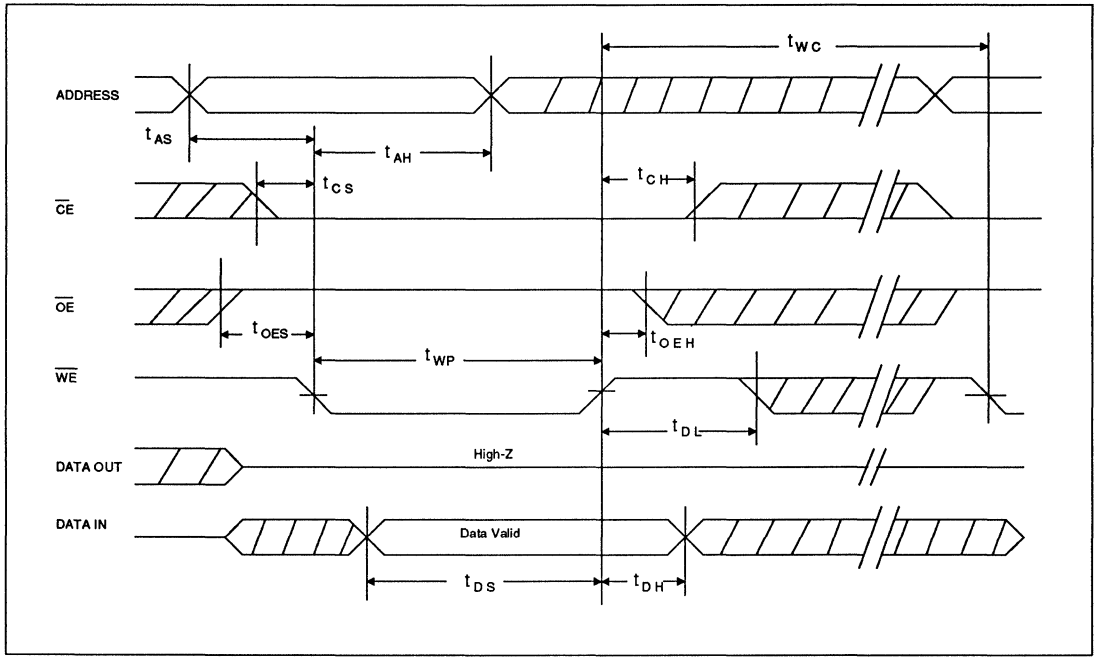
Symbol	Parameter	28C16A-20 Min.	28C16A-20 Max.	Units
t_{WC}	Write cycle time		10	ms
t_{AS}	Address setup time	10		ns
t_{AH}	Address hold time	100		ns
t_{CS}	Write setup time	0		ns
t_{CH}	Write hold time	0		ns
t_{CW} *	$\overline{CE}$ pulse time	150		ns
t_{OES}, t_{OEH}	$\overline{OE}$ setup time, $\overline{OE}$ hold time	15		ns
t_{WP} *	$\overline{WE}$ pulse width	150		ns
t_{DL}	Data latch time	50		ns
t_{DS}	Data setup time	50		ns
t_{DH}	Data hold time	10		ns
t_{INIT}	Write inhibit period after power-up	5	20	ms

NOTE: * A write pulse of less than 20ns duration will not initiate a write cycle.

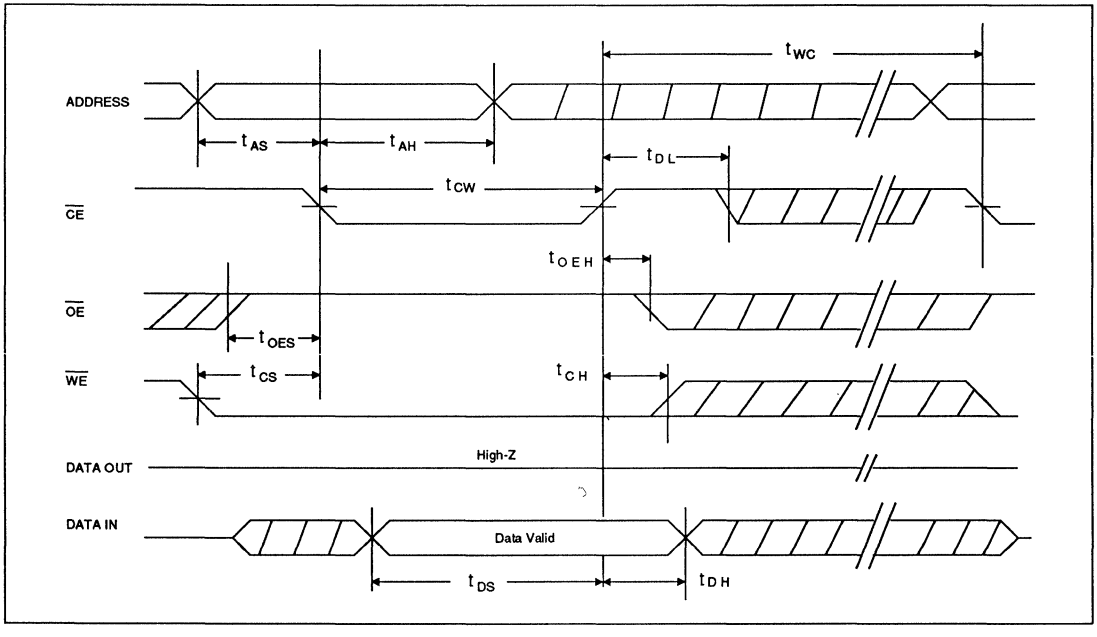
TIMING <Read Cycle>



TIMING <$\overline{WE}$ Controlled Write Cycle>



TIMING <$\overline{CE}$ Controlled Write Cycle>



PIN DESCRIPTIONS

ADDRESSES (A_0-A_{10})
The Address inputs are used to select an 8-bit memory location during read and write cycles.

CHIP ENABLE ($\overline{CE}$)
The Chip Enable input must be held LOW to enable read and write cycles. When $\overline{CE}$ is held HIGH, the device is deselected and power consumption is reduced to the standby level.

OUTPUT ENABLE ($\overline{OE}$)
The Output Enable input, in conjunction with $\overline{CE}$, determines whether the device outputs are high impedance, or output data during a read cycle.

DATA IN/DATA OUT (I/O_0-I/O_7)
Data is output to the I/O pins during a read cycle, and written into the device from the I/O pins during a write cycle.

WRITE ENABLE ($\overline{WE}$)
The Write Enable input, in conjunction with $\overline{CE}$ and $\overline{OE}$, initiates a write cycle.

DEVICE OPERATION

READ
Device data is output to the data bus when both $\overline{OE}$ and $\overline{CE}$ are LOW. The data bus is high impedance when either $\overline{CE}$ or $\overline{OE}$ go HIGH. This 2-line control architecture can be used to eliminate bus contention in a system environment.

BYTE WRITE
A write cycle is initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. Both $\overline{CE}$ and $\overline{WE}$ controlled write cycles can be executed, i.e., the address is latched on the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last, while data is latched on the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and times itself to completion.

DATA POLLING
Data polling is provided to indicate the completion of a byte write cycle. Once a byte write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O_7 (I/O_0-I/O_6 are indeterminate) until the programming cycle is complete. Upon completion of the self-timed byte write cycle all I/Os will output true data during a read cycle.

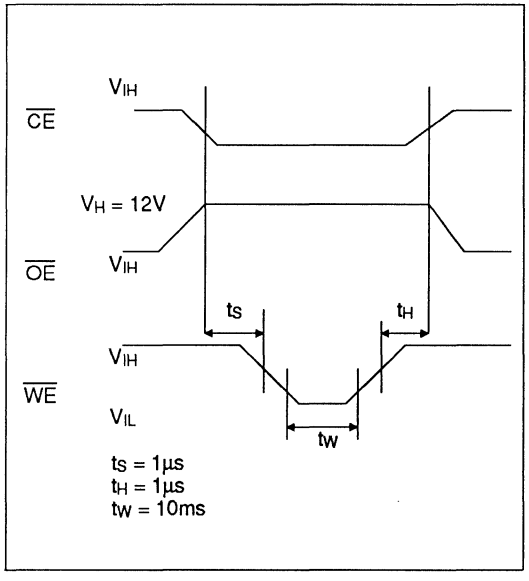
FALSE WRITE PROTECTION
(1) The CAT28C16AI has an on-chip V_{CC} sense circuit which disables the internal write circuitry whenever V_{CC} is less than 3.0V.

(2) During power-up, write operations are inhibited for 5ms to 20ms after V_{CC} reaches 3.0V. Read cycles are not affected during this initialization-period.

(3) Write cycles are inhibited if $\overline{OE}$ is LOW, or $\overline{CE}$ or $\overline{WE}$ are HIGH.

(4) A write pulse of less than 20ns duration will not initiate a write cycle.

CHIP ERASE
The entire memory can be set to 1's by setting $\overline{CE}$ LOW, $\overline{OE}$ to 12V, and pulsing $\overline{WE}$ LOW for 10ms.



CAT28C17A
2K x 8 BIT CMOS E^2PROM

DESCRIPTION

The CAT28C17A is a fast, low power, 5V-only CMOS E^2PROM requiring a simple interface for in-system programming.

On-chip address and data latches, self-timed write cycle with auto-erase and V_{CC} power up/down write protection eliminate additional timing and protection hardware. Data polling and a RDY/$\overline{BUSY}$ pin are provided to allow the user to minimize write cycle time.

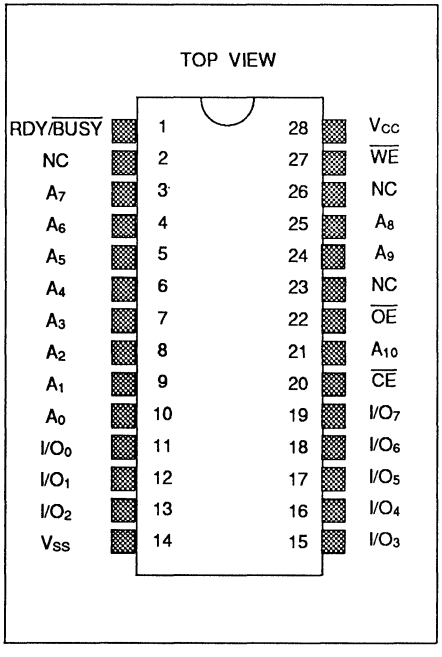
The CAT28C17A is fabricated in reliable floating gate CMOS technology. It is designed for up to10,000 write cycles and 10 years data retention.

FEATURES

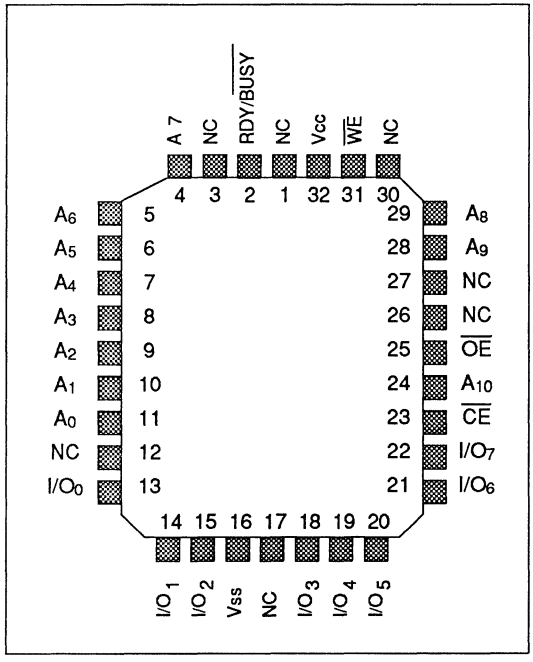
- Access time: 200ns max
- Low CMOS power:
  - Active: 25mA max
  - Standby: 100µA max
- 5V-only operation
- Simple write operation:
  - On-chip address and data latches
  - Self-timed write cycle with auto-erase
  - Data polling
- Fast write cycle time
  10ms max byte write
- Reliable floating gate CMOS technology
- JEDEC approved 28-pin DIP, Small Outline, and 32-pin PLCC packages available
- Power-up inadvertent write protection

PIN CONFIGURATION

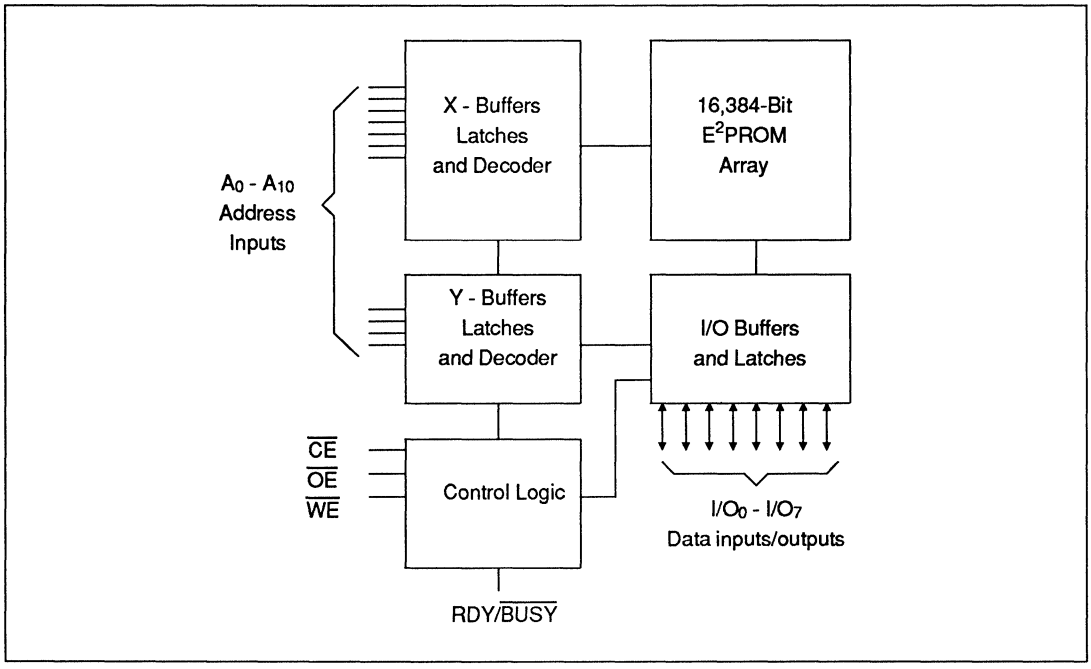
28-Pin DIP and S.O.



32-Pin PLCC



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{10}	Address inputs
I/O_0 - I/O_7	Data inputs/outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
RDY/$\overline{BUSY}$	Ready/Busy indicator
V_{CC}	+5V
V_{SS}	Ground

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V)

Symbol	Parameter	Conditions	Limits Typ. max.	Unit
$C_{I/O}$	Input/Output capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input capacitance	V_{IN} = 0V	6	pF

NOTE: These parameters are periodically sampled and are not 100% tested.

ABSOLUTE MAXIMUM RATINGS *

Temperature under bias . . . . . -40°C to +85°C
Storage temperature . . . . . -65°C to +150°C
Voltage on any input pin relative to V_{SS} . . . . . -0.5 to +7V
Voltage on any output pin relative to V_{SS} . . . . . -0.5 to V_{CC} +0.5V
D.C. output current 5mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, CAT28C17A T_A = 0°C to +70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC}	V_{CC} current (operating, TTL)	$\overline{CE}$=$\overline{OE}$=V_{IL}, f=6.7MHz, all I/O's = open			35	mA
I_{CCC}	V_{CC} current (operating, CMOS)	$\overline{CE}$=$\overline{OE}$=V_{ILC}*, f=6.7MHz, all I/O's = open			25	mA
I_{SB}	V_{CC} current (standby, TTL)	$\overline{CE}$=V_{IH} All I/O's open			1	mA
I_{SBC}	V_{CC} current (standby, CMOS)	$\overline{CE}$=V_{IHC}** All I/O's open			100	µA
I_{LI}	Input leakage current	V_{IN} = GND to V_{CC}			10	µA
I_{LO}	Output leakage current	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.3		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V
V_{WI}	V_{CC} trip voltage for write protection		3.0	3.5		V

NOTE:
* V_{ILC} = -0.3V to +0.3V
** V_{IHC} = V_{CC} - 0.3V to V_{CC} + 1.0V

MODE SELECTION

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Read	L	H	L	D_{OUT}	ACTIVE
Byte write	L	⌐‾⌐	H	D_{IN}	ACTIVE
Standby and write inhibit	H	X	X	HIGH-Z	STANDBY
Write inhibit	X	X	L		
Write inhibit	X	H	X		
Chip erase	L	L	12V	HIGH-Z	ACTIVE

AC CHARACTERISTICS - TEST CONDITIONS

Parameter	Conditions
Input pulse level	0.4 to 2.4V
Input rise and fall times	10ns
Input/output timing reference level	'0' = 0.8V, '1' = 2.0V
Output load	C_L = 100pF, 1 TTL gate

AC CHARACTERISTICS <Read Cycle>

(CAT28C17A T_A = 0°C to +70°C, V_{CC} = +5V ±10%)

Symbol	Parameter	28C17A-20 Min.	28C17A-20 Max.	Units
t_{RC}	Read cycle time	200		ns
t_{CE}	$\overline{CE}$ access time		200	ns
t_{AA}	Address access time		200	ns
t_{OE}	$\overline{OE}$ access time		80	ns
t_{LZ}	$\overline{CE}$ low to active output	10		ns
t_{OLZ}	$\overline{OE}$ low to active output	10		ns
t_{HZ}	$\overline{CE}$ high to high-Z output	10	55	ns
t_{OHZ}	$\overline{OE}$ high to high-Z output	10	55	ns
t_{OH}	Output hold from address change	20		ns

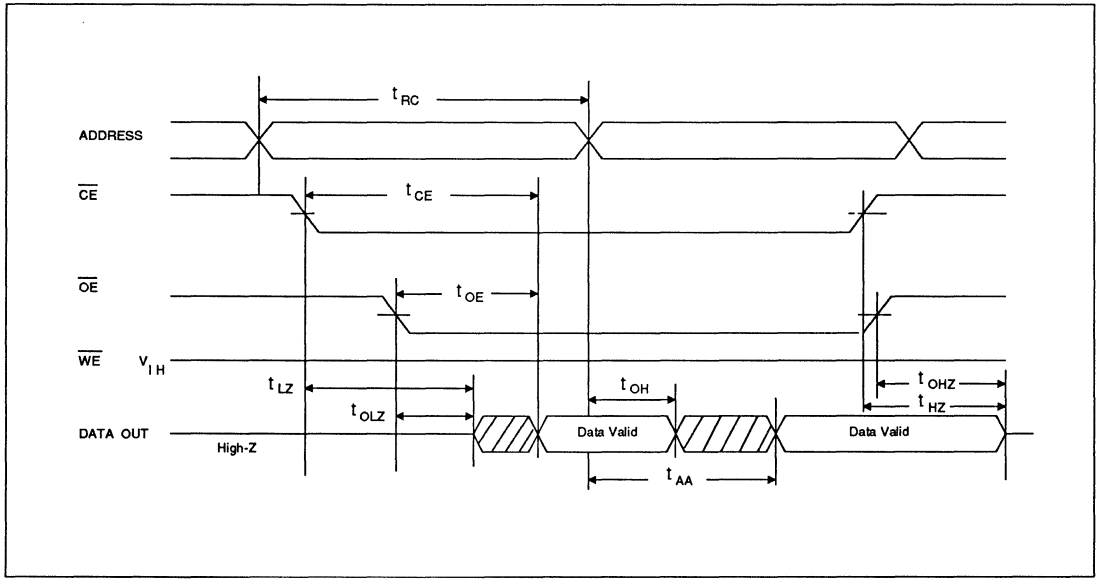
AC CHARACTERISTICS <Write Cycle>

(CAT28C17A T_A = 0°C to +70°C, V_{CC} = +5V ±10%)

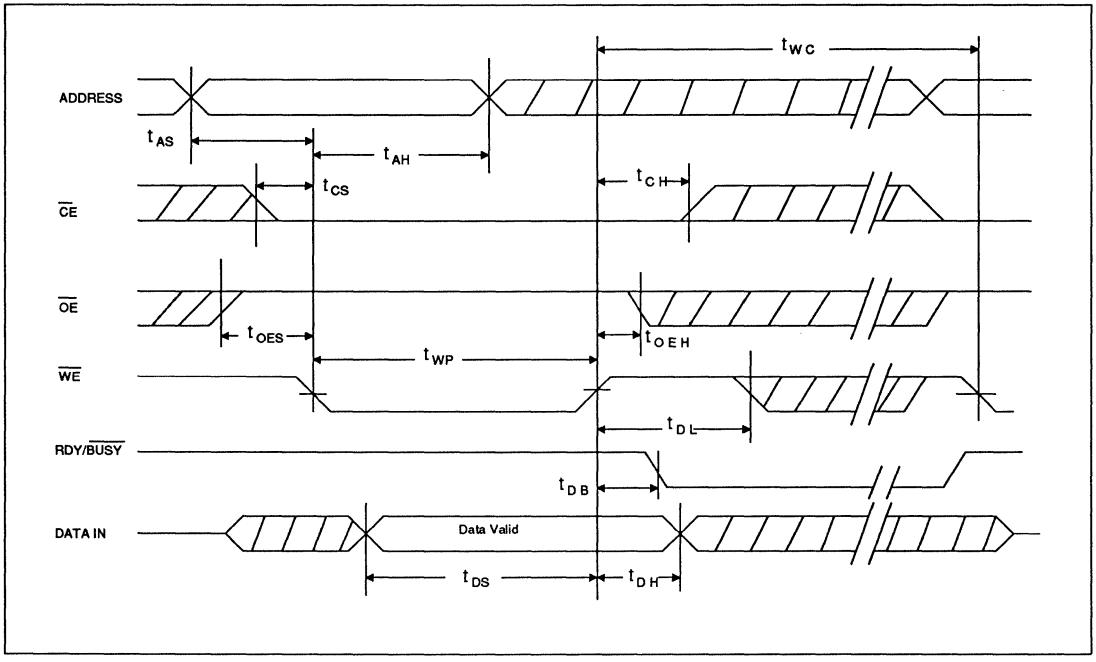
Symbol	Parameter	28C17A-20 Min	28C17A-20 Max	Units
t_{WC}	Write cycle time		10	ms
t_{AS}	Address setup time	10		ns
t_{AH}	Address hold time	100		ns
t_{CS}	Write setup time	0		ns
t_{CH}	Write hold time	0		ns
t_{CW} *	$\overline{CE}$ pulse time	150		ns
t_{OES}, t_{OEH}	$\overline{OE}$ setup time, $\overline{OE}$ hold time	15		ns
t_{WP} *	$\overline{WE}$ pulse width	150		ns
t_{DL}	Data latch time	50		ns
t_{DS}	Data setup time	50		ns
t_{DH}	Data hold time	10		ns
t_{INIT}	Write inhibit period after power-up	5	20	ms
t_{DB}	Time to device busy		80	ns

NOTE: * A write pulse of less than 20ns duration will not initiate a write cycle.

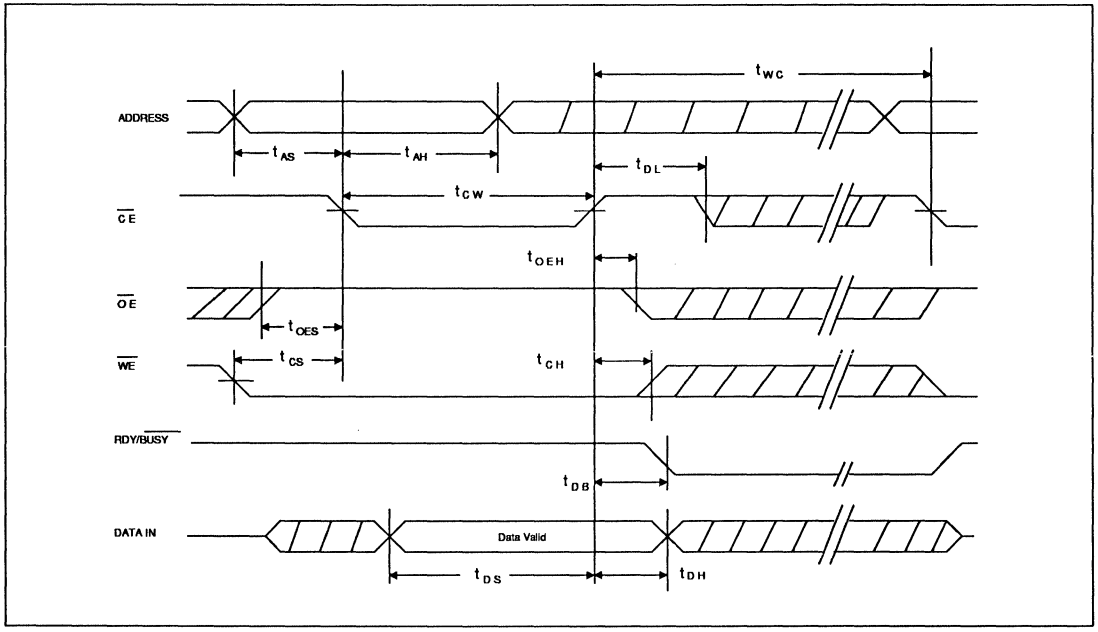
TIMING <Read Cycle>



TIMING <$\overline{WE}$ Controlled Write Cycle>



TIMING <$\overline{CE}$ Controlled Write Cycle>



PIN DESCRIPTIONS

ADDRESSES (A_0-A_{10})

The Address inputs are used to select an 8-bit memory location during read and write cycles.

CHIP ENABLE ($\overline{CE}$)

The Chip Enable input must be held LOW to enable read and write cycles. When $\overline{CE}$ is held HIGH, the device is deselected and power consumption is reduced to the standby level.

OUTPUT ENABLE ($\overline{OE}$)

The Output Enable input, in conjunction with $\overline{CE}$, determines whether the device outputs are high impedance, or output data during a read cycle.

DATA IN/DATA OUT (I/O_0-I/O_7)

Data is output to the I/O pins during a read cycle, and written into the device from the I/O pins during a write cycle.

WRITE ENABLE ($\overline{WE}$)

The Write Enable input, in conjunction with $\overline{CE}$ and $\overline{OE}$, initiates a write cycle.

READ/BUSY (RDY/$\overline{BUSY}$)

The RDY/$\overline{BUSY}$ pin is an open drain output which indicates device status during programming. This output is pulled low during the write cycle and released at the end of programming. Several devices may be OR-tied to the same RDY/$\overline{BUSY}$ line.

DEVICE OPERATION

READ

Device data is output to the data bus when both $\overline{OE}$ and $\overline{CE}$ are LOW. The data bus is high impedance when either $\overline{CE}$ or $\overline{OE}$ go HIGH. This 2-line control architecture can be used to eliminate bus contention in a system environment.

BYTE WRITE

A write cycle is initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. Both $\overline{CE}$ and $\overline{WE}$ controlled write cycles can be executed, i.e., the address is latched on the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last, while data is latched on the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and times itself to completion.

DATA POLLING

Data polling is provided to indicate the completion of a byte write cycle. Once a byte write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O_7 (I/O_0-I/O_6 are indeterminate) until the programming cycle is complete. Upon completion of the self-timed byte write cycle all I/Os will output true data during a read cycle.

FALSE WRITE PROTECTION

(I) The CAT28C17A has an on-chip VCC sense circuit which disables the internal write circuitry whenever V_{CC} is less than 3.0V.

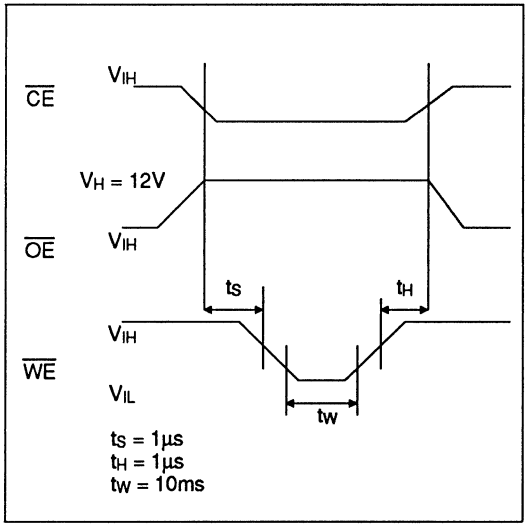
(2) During power-up, write operations are inhibited for 5ms to 20ms after VCC reaches 3.0V.Read cycles are not affected during this initialization period.

(3) Write cycles are inhibited if OE is LOW, or or WE are HIGH.

(4) A write pulse of less than 20ns duration will not initiate a write cycle.

CHIP ERASE

The entire memory can be set to 1's by setting $\overline{CE}$ LOW, $\overline{OE}$ to 12V, and pulsing $\overline{WE}$ low for 10ms.



CAT28C17AI - Industrial Temperature
2K x 8 BIT CMOS E^2PROM

DESCRIPTION

The CAT28C17AI is a fast, low power, 5V-only CMOS E^2PROM requiring a simple interface for in-system programming.

On-chip address and data latches, self-timed write cycle with auto-erase and V_{CC} power up/down write protection eliminate additional timing and protection hardware. Data polling and a RDY/$\overline{BUSY}$ pin are provided to allow the user to minimize write cycle time.

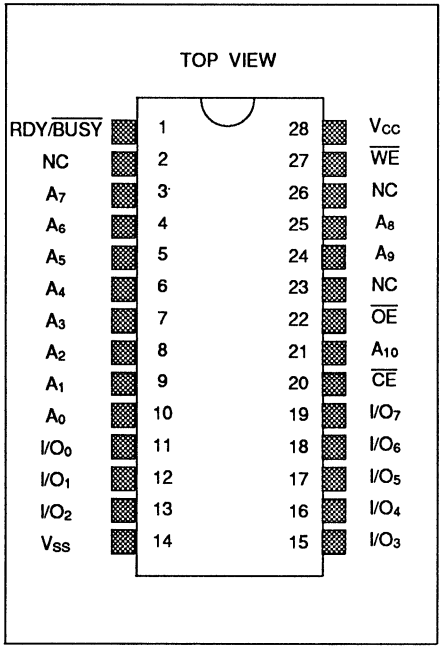
The CAT28C17AI is fabricated in reliable floating gate CMOS technology. It is designed for up to10,000 write cycles and 10 years data retention.

FEATURES

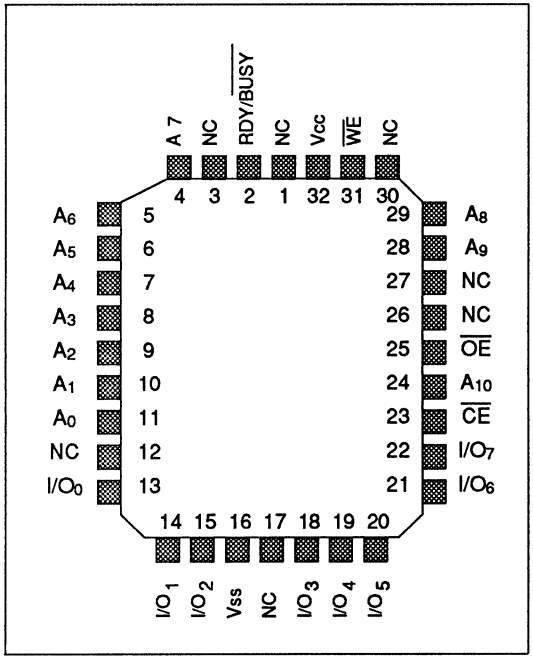
- Access time: 200ns max
- Low CMOS power:
  - Active: 25mA max
  - Standby: 100µA max
- 5V-only operation
- Simple write operation:
  - On-chip address and data latches
  - Self-timed write cycle with auto-erase
  - Data polling
- Fast write cycle time
  10ms max byte write
- Reliable floating gate CMOS technology
- JEDEC approved 28-pin DIP,Small Outline, and 32-pin PLCC packages available
- Power-up inadvertent write protection

PIN CONFIGURATION

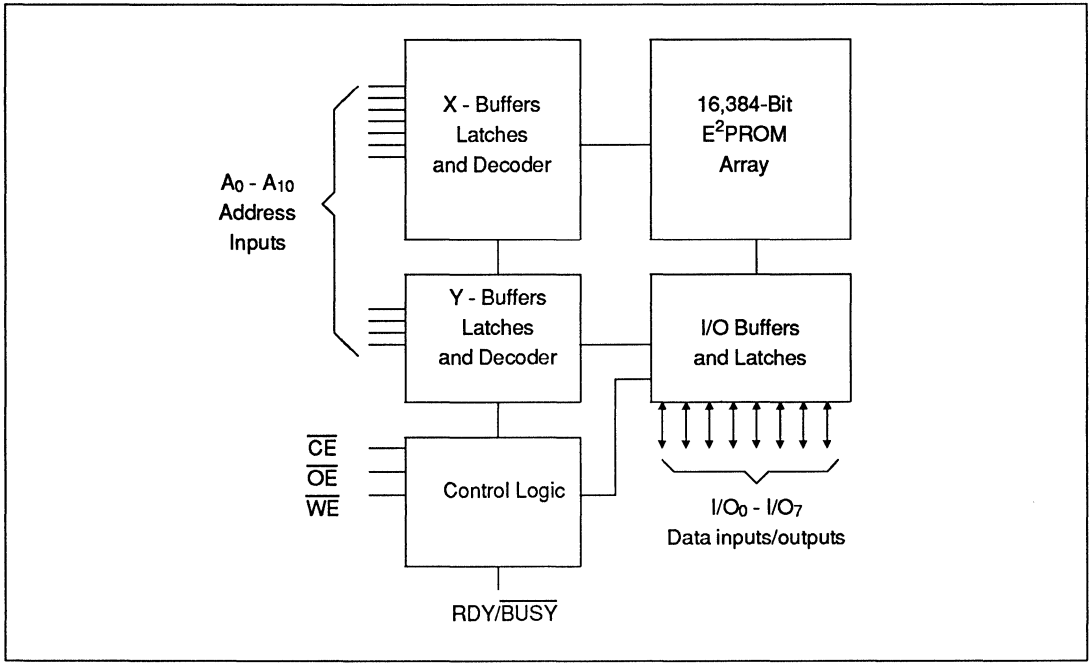
28-Pin DIP and S.O.



32-Pin PLCC



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{10}	Address inputs
I/O_0 - I/O_7	Data inputs/outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
RDY/$\overline{BUSY}$	Ready/Busy indicator
V_{CC}	+5V
V_{SS}	Ground

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V)

Symbol	Parameter	Conditions	Limits Typ. max.	Unit
$C_{I/O}$	Input/Output capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input capacitance	V_{IN} = 0V	6	pF

NOTE: These parameters are periodically sampled and are not 100% tested.

ABSOLUTE MAXIMUM RATINGS *

Temperature under bias . . . . . -40°C to +85°C
Storage temperature . . . . . -65°C to +150°C
Voltage on any input pin relative to V_{SS} . . . . . -0.5 to +7V
Voltage on any output pin relative to V_{SS} . . . . . -0.5 to V_{CC} +0.5V
D.C. output current 5mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, CAT28C17AI T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC}	V_{CC} current (operating, TTL)	$\overline{CE}$=$\overline{OE}$=V_{IL}, f=6.7MHz, all I/O's = open			35	mA
I_{CCC}	V_{CC} current (operating, CMOS)	$\overline{CE}$=$\overline{OE}$=V_{ILC}*, f=6.7MHz, all I/O's = open			25	mA
I_{SB}	V_{CC} current (standby, TTL)	$\overline{CE}$=V_{IH} All I/O's open			1	mA
I_{SBC}	V_{CC} current (standby, CMOS)	$\overline{CE}$=V_{IHC}** All I/O's open			100	µA
I_{LI}	Input leakage current	V_{IN} = GND to V_{CC}			10	µA
I_{LO}	Output leakage current	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.3		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V
V_{WI}	V_{CC} trip voltage for write protection		3.0	3.5		V

NOTE:
* V_{ILC} = -0.3V to +0.3V
** V_{IHC} = V_{CC} - 0.3V to V_{CC} + 1.0V

MODE SELECTION

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Read	L	H	L	D_{OUT}	ACTIVE
Byte write	L	⎍	H	D_{IN}	ACTIVE
Standby and write inhibit	H	X	X	HIGH-Z	STANDBY
Write inhibit	X	X	L		
Write inhibit	X	H	X		
Chip erase	L	L	12V	HIGH-Z	ACTIVE

AC CHARACTERISTICS - TEST CONDITIONS

Parameter	Conditions
Input pulse level	0.4 to 2.4V
Input rise and fall times	10ns
Input/output timing reference level	'0' = 0.8V, '1' = 2.0V
Output load	C_L = 100pF, 1 TTL gate

AC CHARACTERISTICS <Read Cycle>

(CAT28C17AI T_A = -40°C to +85°C, V_{CC} = +5V ±10%)

Symbol	Parameter	28C17A-20 Min.	28C17A-20 Max.	Units
t_{RC}	Read cycle time	200		ns
t_{CE}	$\overline{CE}$ access time		200	ns
t_{AA}	Address access time		200	ns
t_{OE}	$\overline{OE}$ access time		80	ns
t_{LZ}	$\overline{CE}$ low to active output	10		ns
t_{OLZ}	$\overline{OE}$ low to active output	10		ns
t_{HZ}	$\overline{CE}$ high to high-Z output	10	55	ns
t_{OHZ}	$\overline{OE}$ high to high-Z output	10	55	ns
t_{OH}	Output hold from address change	20		ns

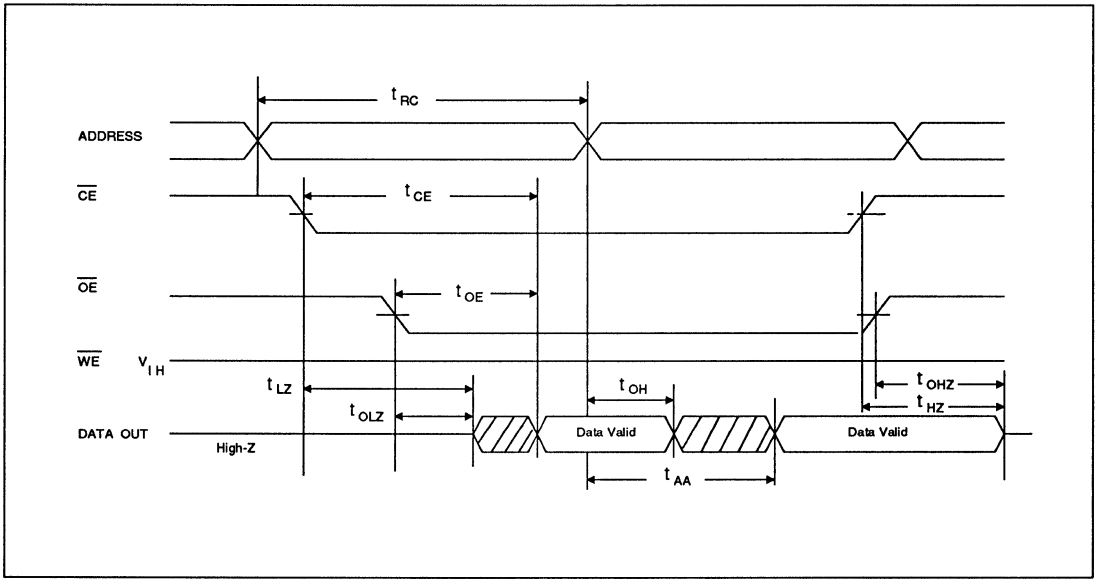
AC CHARACTERISTICS <Write Cycle>

(CAT28C17AI T_A = -40°C to +85°C, V_{CC} = +5V ±10%)

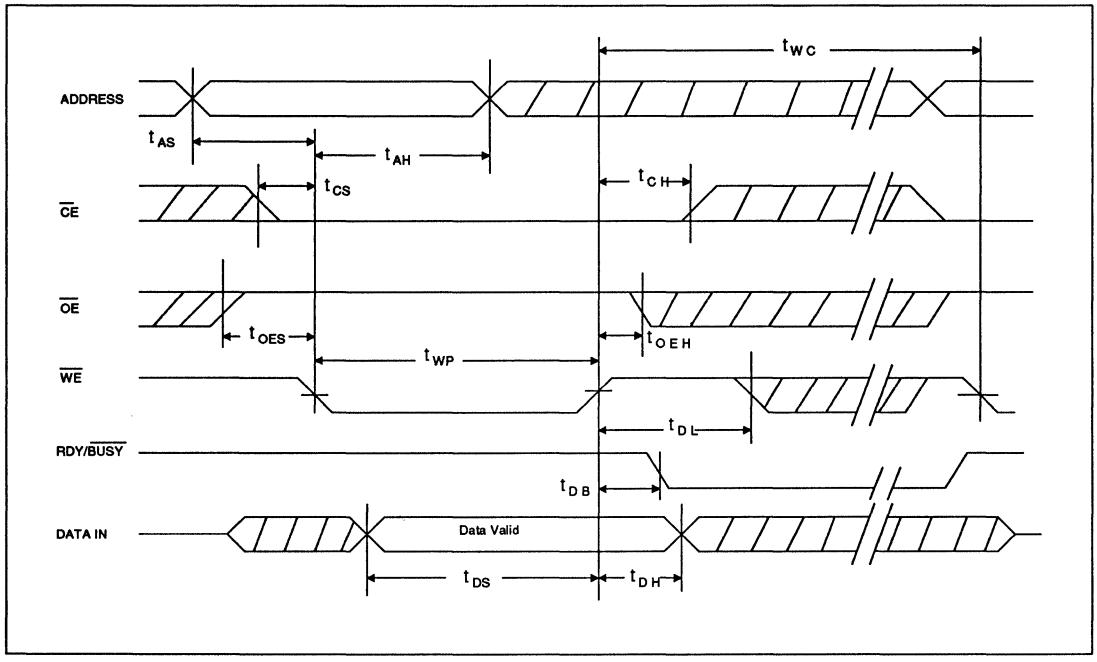
Symbol	Parameter	28C17A-20 Min	28C17A-20 Max	Units
t_{WC}	Write cycle time		10	ms
t_{AS}	Address setup time	10		ns
t_{AH}	Address hold time	100		ns
t_{CS}	Write setup time	0		ns
t_{CH}	Write hold time	0		ns
t_{CW} *	$\overline{CE}$ pulse time	150		ns
t_{OES}, t_{OEH}	$\overline{OE}$ setup time, $\overline{OE}$ hold time	15		ns
t_{WP} *	$\overline{WE}$ pulse width	150		ns
t_{DL}	Data latch time	50		ns
t_{DS}	Data setup time	50		ns
t_{DH}	Data hold time	10		ns
t_{INIT}	Write inhibit period after power-up	5	20	ms
t_{DB}	Time to device busy		80	ns

NOTE: * A write pulse of less than 20ns duration will not initiate a write cycle.

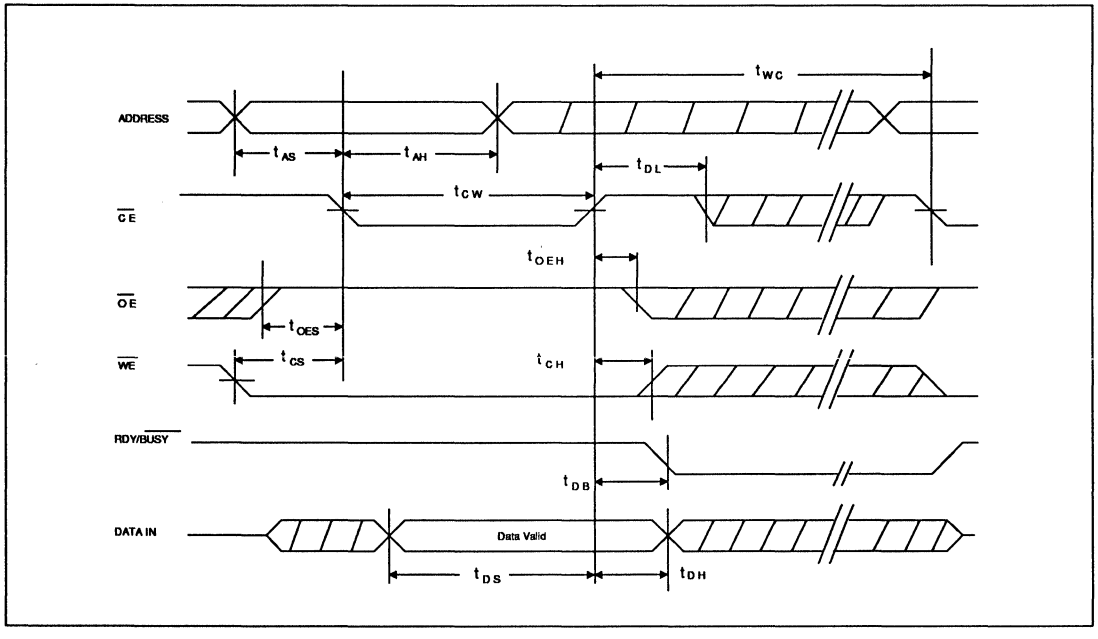
TIMING <Read Cycle>



TIMING <$\overline{WE}$ Controlled Write Cycle>



TIMING <$\overline{CE}$ Controlled Write Cycle>



PIN DESCRIPTIONS

ADDRESSES (A_0-A_{10})

The Address inputs are used to select an 8-bit memory location during read and write cycles.

CHIP ENABLE ($\overline{CE}$)

The Chip Enable input must be held LOW to enable read and write cycles. When $\overline{CE}$ is held HIGH, the device is deselected and power consumption is reduced to the standby level.

OUTPUT ENABLE ($\overline{OE}$)

The Output Enable input, in conjunction with $\overline{CE}$, determines whether the device outputs are high impedance, or output data during a read cycle.

DATA IN/DATA OUT (I/O_0-I/O_7)

Data is output to the I/O pins during a read cycle, and written into the device from the I/O pins during a write cycle.

WRITE ENABLE ($\overline{WE}$)

The Write Enable input, in conjunction with $\overline{CE}$ and $\overline{OE}$, initiates a write cycle.

READ/BUSY (RDY/$\overline{BUSY}$)

The RDY/$\overline{BUSY}$ pin is an open drain output which indicates device status during programming. This output is pulled low during the write cycle and released at the end of programming. Several devices may be OR-tied to the same RDY/$\overline{BUSY}$ line.

DEVICE OPERATION

READ

Device data is output to the data bus when both $\overline{OE}$ and $\overline{CE}$ are LOW. The data bus is high impedance when either $\overline{CE}$ or $\overline{OE}$ go HIGH. This 2-line control architecture can be used to eliminate bus contention in a system environment.

BYTE WRITE

A write cycle is initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. Both $\overline{CE}$ and $\overline{WE}$ controlled write cycles can be executed, i.e., the address is latched on the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last, while data is latched on the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and times itself to completion.

DATA POLLING

$\overline{Data}$ polling is provided to indicate the completion of a byte write cycle. Once a byte write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O_7 (I/O_0-I/O_6 are indeterminate) until the programming cycle is complete. Upon completion of the self-timed byte write cycle all I/Os will output true data during a read cycle.

FALSE WRITE PROTECTION

(I) The CAT28C17AI has an on-chip VCC sense circuit which disables the internal write circuitry whenever V_{CC} is less than 3.0V.

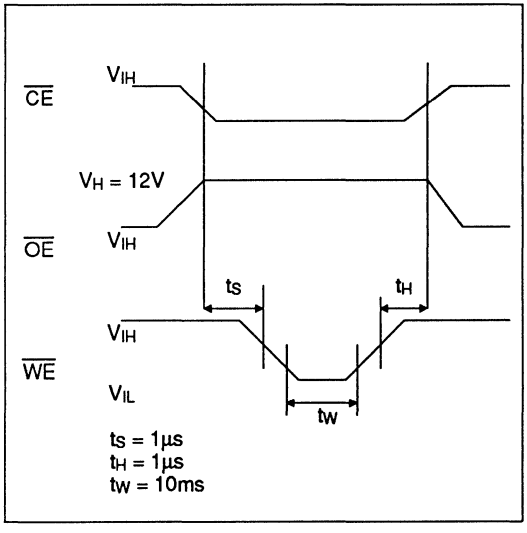
(2) During power-up, write operations are inhibited for 5ms to 20ms after VCC reaches 3.0V.Read cycles are not affected during this initialization period.

(3) Write cycles are inhibited if OE is LOW, or or WE are HIGH.

(4) A write pulse of less than 20ns duration will not initiate a write cycle.

CHIP ERASE

The entire memory can be set to 1's by setting $\overline{CE}$ LOW, $\overline{OE}$ to 12V, and pulsing $\overline{WE}$ low for 10ms.



CAT28C64A
8K x 8 BIT CMOS E^2PROM

DESCRIPTION

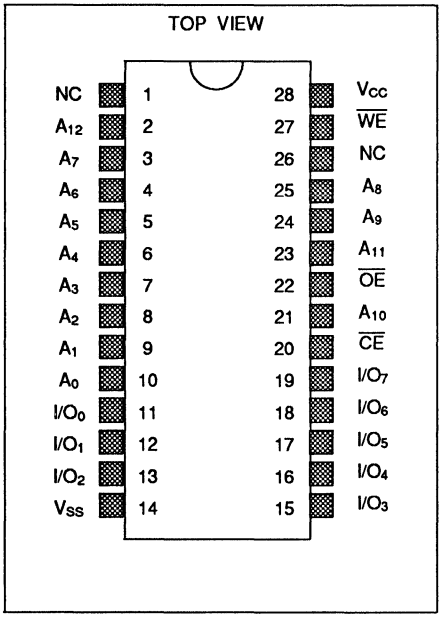
The CAT28C64A is a fast, low power, 5V-only CMOS E^2PROM requiring a simple interface for in-system programming. On-chip address and data latches, self-timed write cycle with auto-erase and V_{CC} power up/down write protection eliminate additional timing and protection hardware. Data polling allows the user to minimize write cycle time while the Page Write mode can reduce programming time. Manufactured using Catalyst's Advanced CMOS floating gate technology, the device can endure 10,000 erase/write cycles and has a data retention of 10 years. The CAT28C64A is assembled in either a 28-pin DIP, 28-pin S.O. or 32-pin PLCC package.

FEATURES

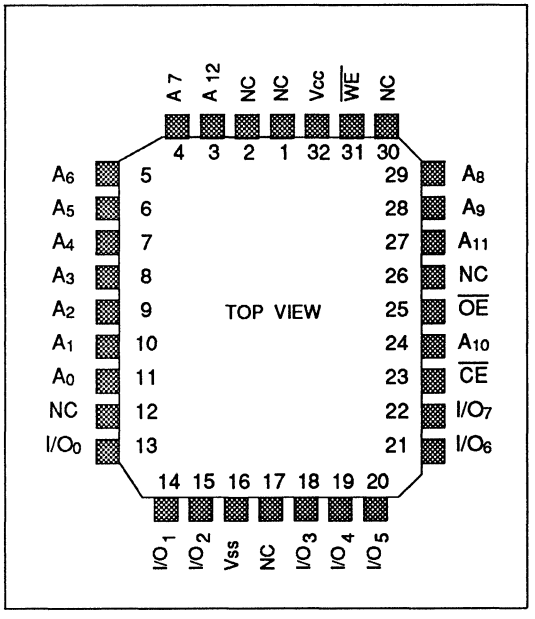
- Fast read access time: 120ns/150ns/200ns
- Low CMOS power:
  - Active 30mA max
  - Standby 100µA max
- 5V-only operation
- Simple write operation:
  - On-chip address and data latches
  - Self-timed write cycle with auto-erase
  - Data polling
- Fast nonvolatile write cycle: 10ms max
- Automatic page write: 1 to 32 bytes in 10ms
- TTL compatible I/O
- JEDEC approved DIP, Small Outline, and PLCC packages available.
- 10,000 rewrites/byte, 10 year data retention
- Power-up inadvertent write protection

PIN CONFIGURATION

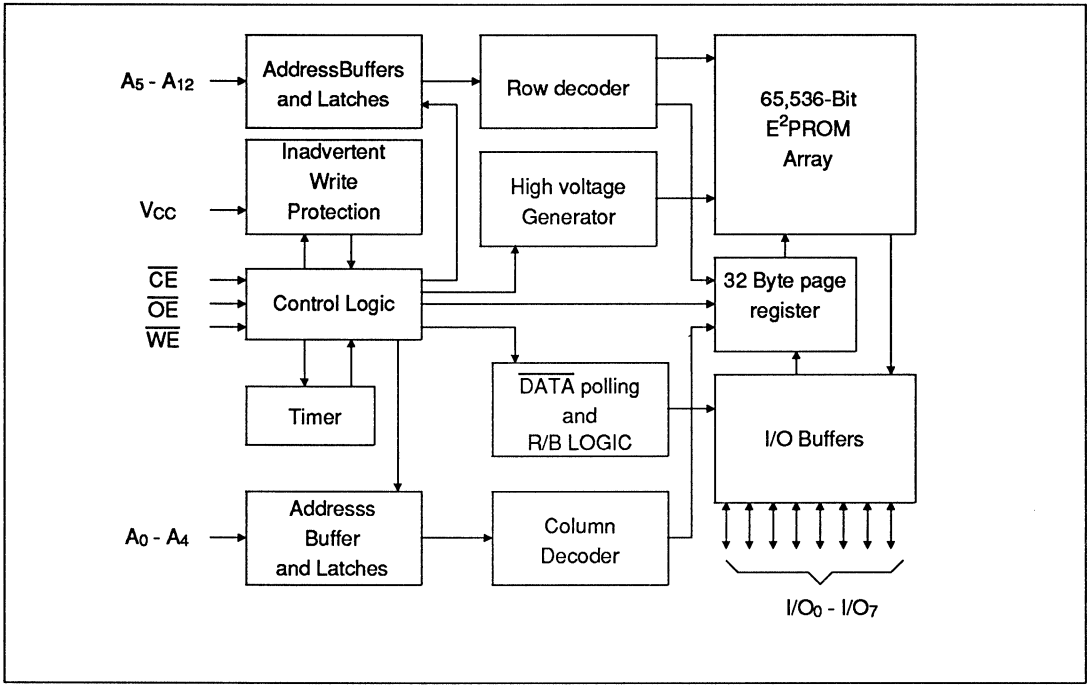
28-Pin DIP and S.O.



32-Pin PLCC



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{12}	Address inputs
I/O_0 - I/O_7	Data inputs/outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
V_{CC}	+5V
V_{SS}	Ground

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V)

Symbol	Parameter	Conditions	Limits Typ. max.	Unit
$C_{I/O}$	Input/Output capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input capacitance	V_{IN} = 0V	10	pF

NOTE: These parameters are periodically sampled and are not 100% tested.

ABSOLUTE MAXIMUM RATINGS *

Temperature under bias . . . . . -10°C to +85°C
Storage temperature . . . . . -65°C to +150°C
Voltage on any input pin relative to V_{SS} . . . . . -0.3 to V_{CC} +0.3V
Voltage on any output pin relative to V_{SS} . . . . . -0.3 to V_{CC} +0.3V
D.C. output current 5mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC}	V_{CC} current (operating, TTL)	$\overline{CE}$=$\overline{OE}$=V_{IL}, f=8.3MHz, all I/O's = open			40	mA
I_{CCC}	V_{CC} current (operating, CMOS)	$\overline{CE}$=$\overline{OE}$=V_{ILC}*, f=8.3MHz, all I/O's = open			30	mA
I_{SB}	V_{CC} current (standby, TTL)	$\overline{CE}$=V_{IH} All I/O's open			1	mA
I_{SBC}	V_{CC} current (standby, CMOS)	$\overline{CE}$=V_{IHC}** All I/O's open			100	µA
I_{LI}	Input leakage current	V_{IN} = GND to V_{CC}	-10		10	µA
I_{LO}	Output leakage current	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}	-10		10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +0.3	V
V_{IL}	Low level input voltage		-0.3		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V
V_{WI}	V_{CC} trip voltage for write protection		3.0		4.0	V

NOTE:
* V_{ILC} = -0.3V to +0.2V
** V_{IHC} = V_{CC} - 0.2V to V_{CC} + 0.3V

MODE SELECTION

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Read	L	H	L	D_{OUT}	ACTIVE
Byte write ($\overline{WE}$ controlled)	L	⎍	H	D_{IN}	ACTIVE
Byte write ($\overline{CE}$ controlled)	⎍	L	H	D_{IN}	ACTIVE
Standby, and Write inhibit	H	X	X	HIGH-Z	STANDBY
Read and Write inhibit	L	H	H	HIGH-Z	ACTIVE

AC CHARACTERISTICS - TEST CONDITIONS

Parameter	Conditions
Input pulse level	0.4 to 2.4V
Input rise and fall times	10ns
Input/output timing reference level	'0' = 0.8V, '1' = 2.0V
Output load	C_L = 100pF, 1 TTL gate

AC CHARACTERISTICS <Read Cycle>

(T_A = 0°C to +70°C, V_{CC} = +5V ±10%)

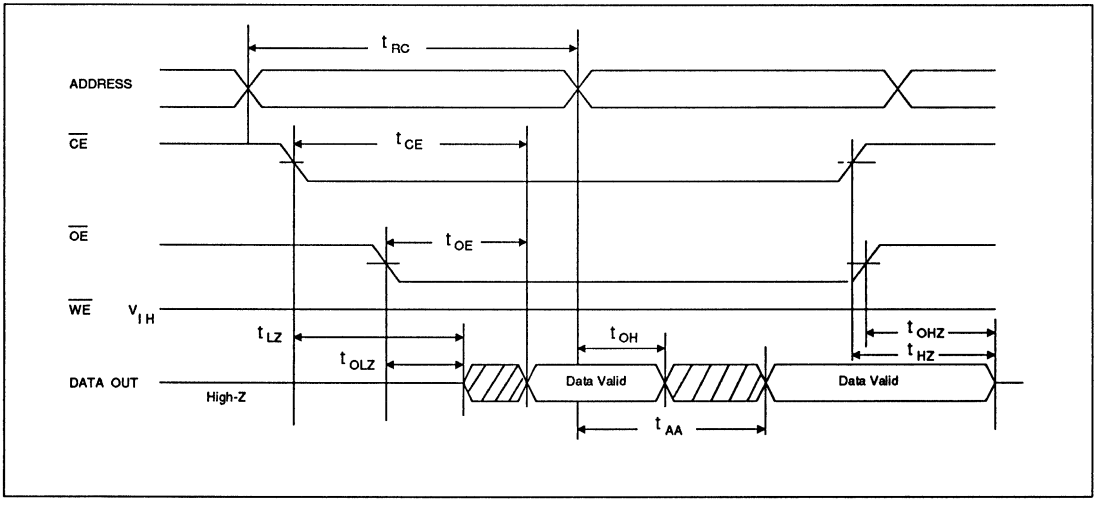
Symbol	Parameter	28C64A-12		28C64A-15		28C64A-20		Units
t_{RC}	Read cycle time	120		150		200		ns
t_{CE}	$\overline{CE}$ access time		120		150		200	ns
t_{AA}	Address access time		120		150		200	ns
t_{OE}	$\overline{OE}$ access time		60		70		90	ns
t_{LZ}	$\overline{CE}$ low to active output	10		10		10		ns
t_{OLZ}	$\overline{OE}$ low to active output	10		10		10		ns
t_{HZ}	$\overline{CE}$ high to High-Z output	10	60	10	70	10	90	ns
t_{OHZ}	$\overline{OE}$ high to High-Z output	10	60	10	70	10	90	ns
t_{OH}	Output hold from address change	20		20		20		ns

AC CHARACTERISTICS <Write Cycle>

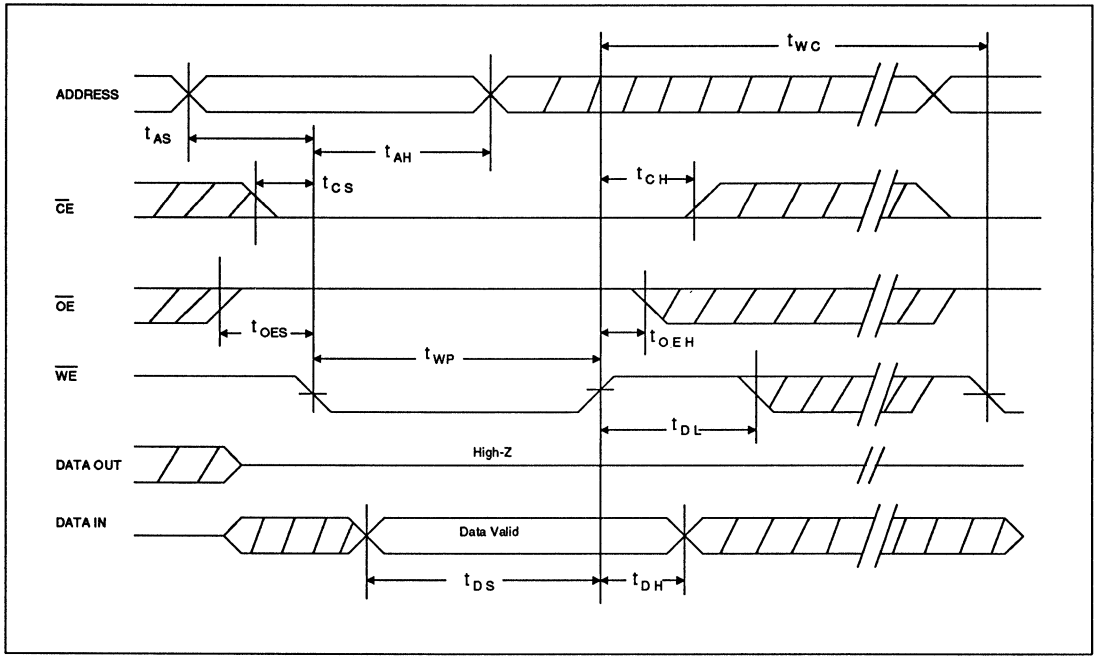
Symbol	Parameter	Limits Min	Limits Max	Units
t_{WC}	Write cycle time		10	ms
t_{AS}	Address setup time	0		ns
t_{AH}	Address hold time	100		ns
t_{CS}	Write setup time	0		ns
t_{CH}	Write hold time	0		ns
t_{CW} (1)	$\overline{CE}$ pulse time	150		ns
t_{OES}	$\overline{OE}$ setup time	10		ns
t_{OEH}	$\overline{OE}$ hold time	10		ns
t_{WP} (1)	$\overline{WE}$ pulse width	150		ns
t_{DL}	Data latch time	50		ns
t_{DS}	Data setup time	70		ns
t_{DH}	Data hold time	0		ns
t_{INIT}	Write inhibit period after power-up	5	20	ms
t_{PL} (2)	Page load time	10	100	µs

NOTES: (1) A write pulse of less than 20ns duration will not initiate a write cycle.
(2) t_{PL} is the time the internal automatic programming cycle begins.

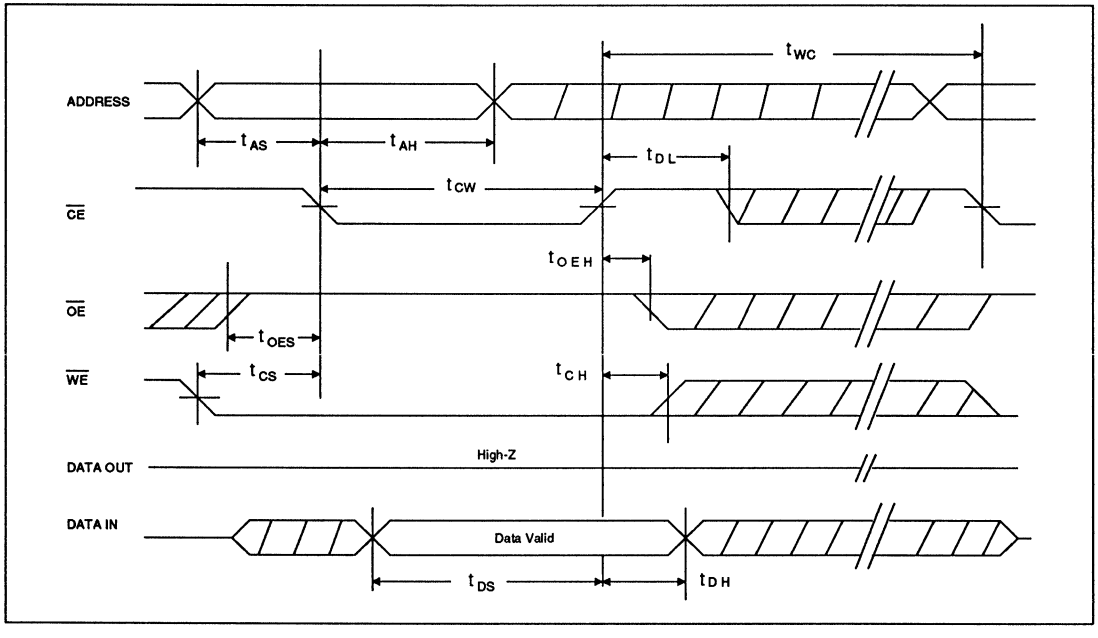
TIMING <Read Cycle>



TIMING <$\overline{WE}$ Controlled Write Cycle>



TIMING <$\overline{CE}$ Controlled Write Cycle>



PIN DESCRIPTIONS

ADDRESSES (A_0-A_{12})

The Address inputs are used to select an 8-bit memory location during read and write cycles.

CHIP ENABLE ($\overline{CE}$)

The Chip Enable input must be held LOW to enable read and write cycles. When $\overline{CE}$ is held HIGH, the device is deselected and power consumption is reduced to the standby level.

OUTPUT ENABLE ($\overline{OE}$)

The Output Enable input, in conjunction with $\overline{CE}$, determines whether the device outputs are high impedance, or output data during a read cycle.

DATA IN/DATA OUT (I/O_0-I/O_7)

Data is output to the I/O pins during a read cycle, and written into the device from the I/O pins during a write cycle.

WRITE ENABLE ($\overline{WE}$)

The Write Enable input, in conjunction with $\overline{CE}$ and $\overline{OE}$, initiates a write cycle.

DEVICE OPERATION

READ

Data stored in the CAT28C64A is transferred to the data bus when $\overline{WE}$ is held high, and both $\overline{OE}$ and $\overline{CE}$ are held low. The data bus is set in a high impedance state when either $\overline{CE}$ or $\overline{OE}$ go high.This 2-line control architecture can be used to eliminate bus contention in a system environment.

BYTE WRITE

A write cycle is initiated when both $\overline{CE}$ and $\overline{WE}$ are low, and $\overline{OE}$ is high. Write cycles can be executed using either $\overline{WE}$ or $\overline{CE}$, with the address input being latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last. Data, conversely, is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and the new data is written within 10ms.

PAGE WRITE

The page write mode of the CAT28C64A (essentially an extended BYTE WRITE mode) allows from 1 to 32 bytes of data to be programmed within a single E^2PROM write cycle. This effectively reduces the byte-write time by a factor of 32.

Following an initial WRITE operation ($\overline{WE}$ pulsed low, for t_{WP}, and then high) the page write mode can begin by issuing sequential $\overline{WE}$ pulses, which load the address and data bytes into a 32 byte temporary buffer. The page address where data is to be written, specified by bits A5 to A12, is latched on the first falling edge of $\overline{WE}$. Each byte within the page is defined by address bits A0 to A4 (which can be loaded in any order) during the first and subsequent write cycles. Each data load cycle must begin within t_{PLMIN} of the rising edge of the preceding $\overline{WE}$ pulse. There is no page write window limitation as long as $\overline{WE}$ is pulsed low within t_{PLMIN}.

Upon completion of the page write sequence, $\overline{WE}$ must stay high a minimum of t_{PLMAX} for the internal automatic program cycle to commence. This programming cycle consists of an erase cycle, which erases any data that existed in each addressed cell, and a write cycle, which writes new data back into the cell. A page write will only write data to the locations that were addressed and will not rewrite the entire page.

DATA POLLING

Data polling is provided to indicate the completion of a byte write cycle. Once a byte write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O_7 (I/O_0-I/O_6 are indeterminate) until the programming cycle is complete. Upon completion of the self-timed byte write cycle all I/Os will output true data during a read cycle.

FALSE WRITE PROTECTION

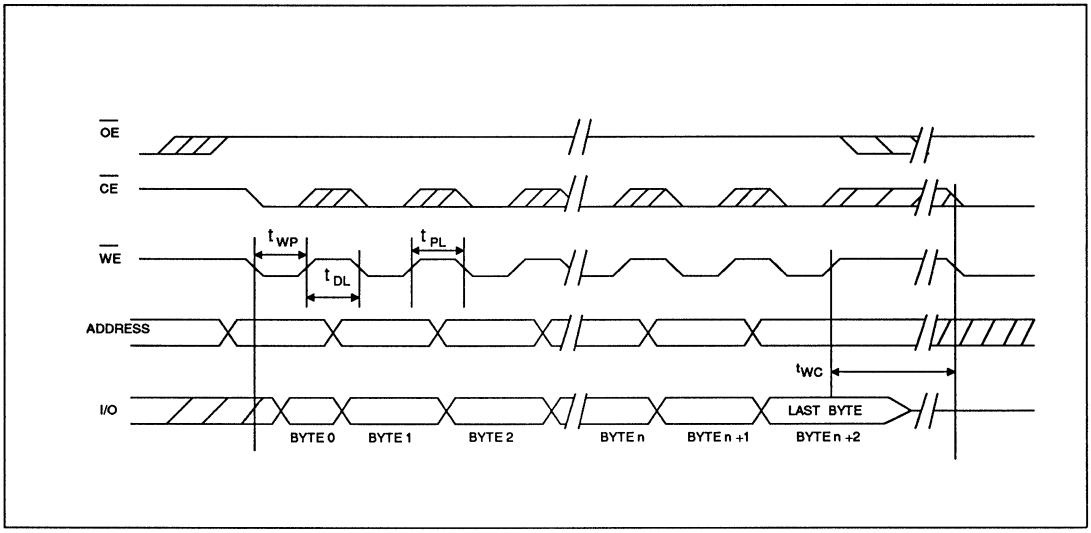
(I) The CAT28C64A has an on-chip V_{CC} sense circuit which disables the internal write circuitry whenever V_{CC} is less than 3.0V.

(2) During power-up, write operations are inhibited for 5ms to 20ms after V_{CC} reaches 3.0V. Read cycles are not affected during this initialization period.

(3) Write cycles are inhibited if $\overline{OE}$ is LOW, or $\overline{CE}$ or $\overline{WE}$ are HIGH.

(4) A write pulse of less than 20ns duration will not initiate a write cycle.

PAGE MODE WRITE CYCLE



CAT28C65A

8K x 8 BIT CMOS E^{2}PROM

Preliminary

DESCRIPTION

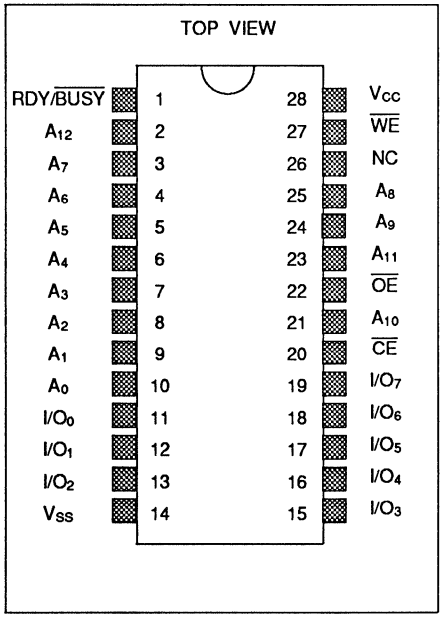
The CAT28C65A is a fast, low power, 5V-only CMOS E^{2}PROM requiring a simple interface for in-system programming. On-chip address and data latches, self-timed write cycle with auto-erase and V_{CC} power up/down write protection eliminate additional timing and protection hardware. Software and hardware data polling allows the user to minimize write cycle time while the Page Write mode can reduce programming time. Manufactured using Catalyst's Advanced CMOS E^{2}PROM floating gate technology, the device can endure 10,000 erase/write cycles and has a data retention of 10 years. The CAT28C65A is assembled in either a 28-pin DIP or S.O. or 32-pin PLCC package.

FEATURES

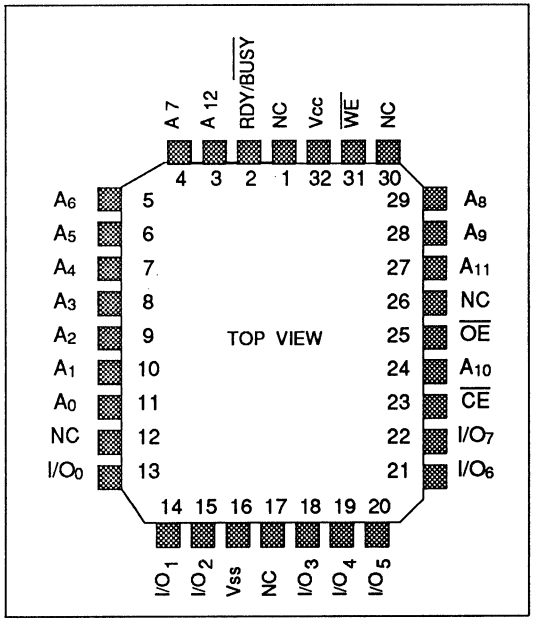
- Fast read access time: 120ns/150ns/200ns
- Low CMOS power:
  - Active: 30mA max
  - Standby: 100µA max
- 5V-only operation
- Simple write operation:
  - On-chip address and data latches
  - Self-timed write cycle with auto-erase
  - Data polling
- Fast nonvolatile write cycle: 10ms max
- Automatic page write: 1 to 32 bytes in 10ms
- TTL compatible I/O
- JEDEC approved DIP, Small Outline, and PLCC packages available
- 10,000 rewrites/byte, 10 year data retention
- RDY/$\overline{BUSY}$ status pin
- Power-up inadvertent write protection

PIN CONFIGURATION

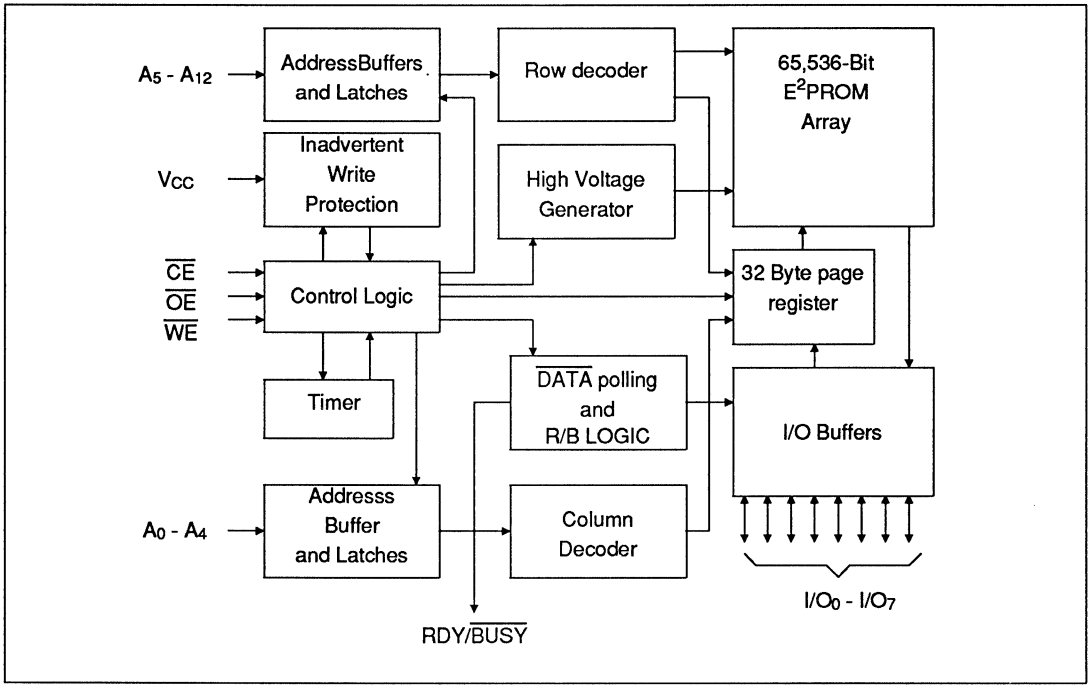
28-Pin DIP and S.O.



32-Pin PLCC



BLOCK DIAGRAM



PIN NAMES

RDY/$\overline{BUSY}$	Ready/Busy indicator
A_0 - A_{12}	Address inputs
I/O_0 - I/O_7	Data inputs/outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
V_{CC}	+5V
V_{SS}	Ground

CAPACITANCE (T_A = 25°C, f = 1.0MHz, V_{CC} = 5V)

Symbol	Parameter	Conditions	Limits Typ. max.	Unit
$C_{I/O}$	Input/Output capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input capacitance	V_{IN} = 0V	10	pF

NOTE: These parameters are periodically sampled and are not 100% tested.

ABSOLUTE MAXIMUM RATINGS *

Temperature under bias . . . . . -10°C to +85°C
Storage temperature . . . . . -65°C to +150°C
Voltage on any input pin relative to V_{SS} . . . . . -0.3 to V_{CC} +0.3V
Voltage on any output pin relative to V_{SS} . . . . . -0.3 to V_{CC} +0.3V
D.C. output current 5mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC}	V_{CC} current (operating, TTL)	$\overline{CE}$=$\overline{OE}$=V_{IL}, f=8.3MHz, all I/O's = open			40	mA
I_{CCC}	V_{CC} current (operating, CMOS)	$\overline{CE}$=$\overline{OE}$=V_{ILC}*, f=8.3MHz, all I/O's = open			30	mA
I_{SB}	V_{CC} current (standby, TTL)	$\overline{CE}$=V_{IH} All I/O's open			1	mA
I_{SBC}	V_{CC} current (standby, CMOS)	$\overline{CE}$=V_{IHC}** All I/O's open			100	µA
I_{LI}	Input leakage current	V_{IN} = GND to V_{CC}	-10		10	µA
I_{LO}	Output leakage current	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}	-10		10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +0.3	V
V_{IL}	Low level input voltage		-0.3		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V
V_{WI}	V_{CC} trip voltage for write protection		3.0		4.0	V

NOTE:
* V_{ILC} = -0.3V to +0.2V
** V_{IHC} = V_{CC} - 0.2V to V_{CC} + 0.3V

MODE SELECTION

Mode	CE	$\overline{WE}$	$\overline{OE}$	I/O	Power
Read	L	H	L	D_{OUT}	ACTIVE
Byte write ($\overline{WE}$ controlled)	L	⎍	H	D_{IN}	ACTIVE
Byte write ($\overline{CE}$ controlled)	⎍	L	H	D_{IN}	ACTIVE
Standby, and Write inhibit	H	X	X	HIGH-Z	STANDBY
Read and Write inhibit	L	H	H	HIGH-Z	ACTIVE

AC CHARACTERISTICS - TEST CONDITIONS

Parameter	Conditions
Input pulse level	0.4 to 2.4V
Input rise and fall times	10ns
Input/output timing reference level	'0' = 0.8V, '1' = 2.0V
Output load	C_L = 100pF, 1 TTL gate

AC CHARACTERISTICS <Read Cycle>

(T_A = 0°C to +70°C, V_{CC} = +5V ±10%)

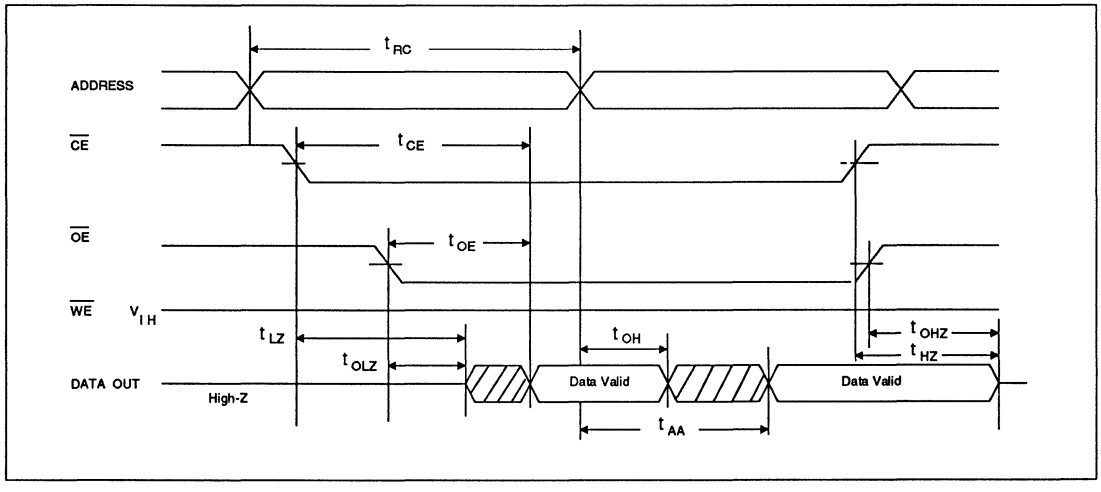
Symbol	Parameter	28C65A-12		28C65A-15		28C65A-20		Units
t_{RC}	Read cycle time	120		150		200		ns
t_{CE}	$\overline{CE}$ access time		120		150		200	ns
t_{AA}	Address access time		120		150		200	ns
t_{OE}	$\overline{OE}$ access time		60		70		90	ns
t_{LZ}	$\overline{CE}$ low to active output	10		10		10		ns
t_{OLZ}	$\overline{OE}$ low to active output	10		10		10		ns
t_{HZ}	$\overline{CE}$ high to High-Z output	10	60	10	70	10	90	ns
t_{OHZ}	$\overline{OE}$ high to High-Z output	10	60	10	70	10	90	ns
t_{OH}	Output hold from address change	20		20		20		ns

AC CHARACTERISTICS <Write Cycle> (T_A = 0° to 70°C, V_{CC} = +5V ±10%)

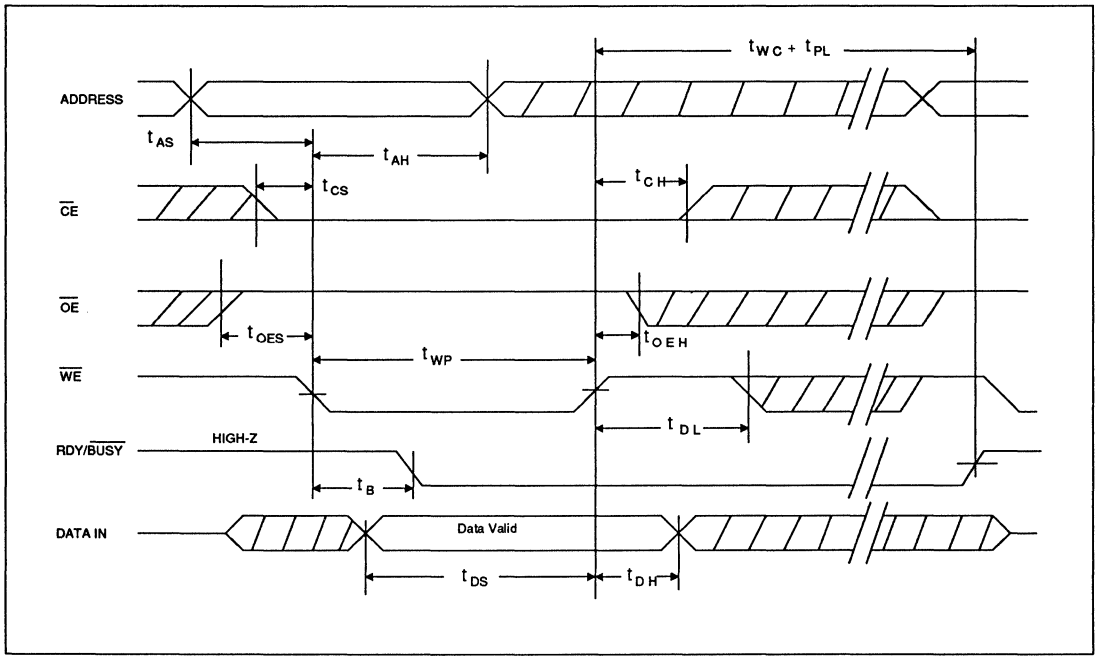
Symbol	Parameter	Limits Min.	Limits Max.	Units
t_{WC}	Write cycle time		10	ms
t_{AS}	Address setup time	0		ns
t_{AH}	Address hold time	100		ns
t_{CS}	Write setup time	0		ns
t_{CH}	Write hold time	0		ns
t_{CW} (1)	$\overline{CE}$ pulse time	150		ns
t_{OES}	$\overline{OE}$ setup time	10		ns
t_{OEH}	$\overline{OE}$ hold time	10		ns
t_{WP} (1)	$\overline{WE}$ pulse width	150		ns
t_{DL}	Data latch time	50		ns
t_B	$\overline{WE}$ low to READY/$\overline{BUSY}$ low		120	ns
t_{DS}	Data setup time	70		ns
t_{DH}	Data hold time	0		ns
t_{INIT}	Write inhibit period after power-up	5	20	ms
t_{PL} (2)	Page load time	10	100	µs

NOTES: (1) A write pulse of less than 20ns duration will not initiate a write cycle.
(2) t_{PL} is the period of the internal automatic nonvolatile programming cycle.

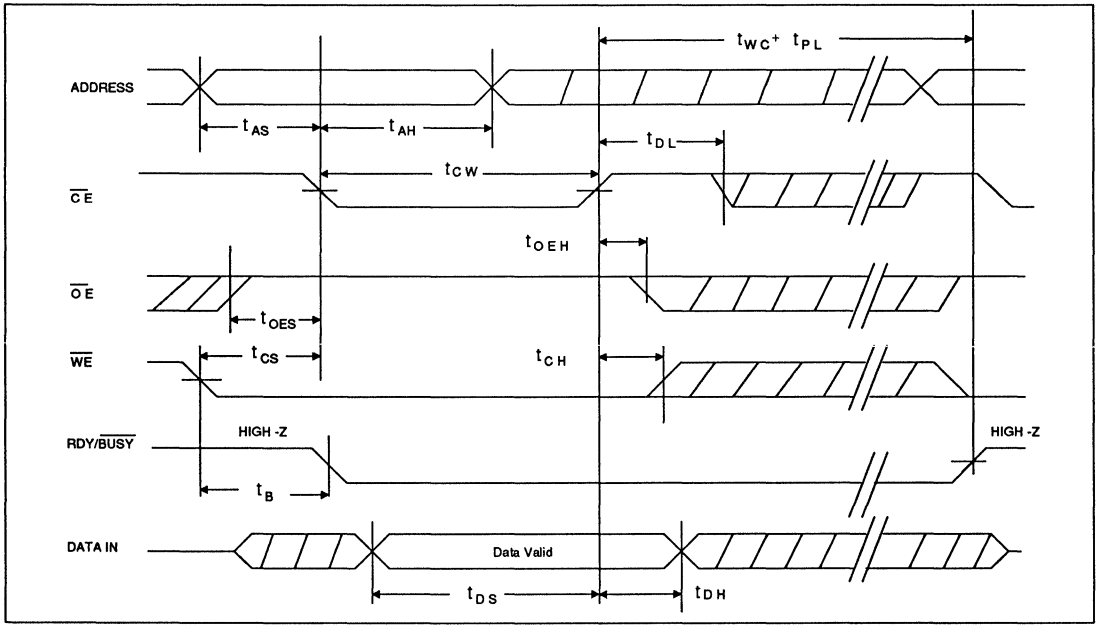
TIMING <Read Cycle>



TIMING <$\overline{WE}$ Controlled Write Cycle>



TIMING <$\overline{CE}$ Controlled Write Cycle>



PIN DESCRIPTIONS

ADDRESSES (A_0-A_{12})
The Address inputs are used to select an 8-bit memory location during read and write cycles.

CHIP ENABLE ($\overline{CE}$)
The Chip Enable input must be held LOW to enable read and write cycles. When $\overline{CE}$ is held HIGH, the device is deselected and power consumption is reduced to the standby level.

OUTPUT ENABLE ($\overline{OE}$)
The Output Enable input, in conjunction with CE, determines whether the device outputs are high impedance, or output data during a read cycle.

DATA IN/DATA OUT (I/O_0-I/O_7)
Data is output to the I/O pins during a read cycle, and written into the device from the I/O pins during a write cycle.

WRITE ENABLE ($\overline{WE}$)
The Write Enable input, in conjunction with $\overline{CE}$ and $\overline{OE}$, initiates a write cycle.

DEVICE OPERATION

READ
Data stored in the CAT28C65A is transferred to the data bus when $\overline{WE}$ is held high, and both $\overline{OE}$ and $\overline{CE}$ are held low. The data bus is in a high impedance state when either $\overline{CE}$ or $\overline{OE}$ go high. This 2-line control architecture can be used to eliminate bus contention in a system environment.

BYTE WRITE
A write cycle is initiated when both $\overline{CE}$ and $\overline{WE}$ are low, and $\overline{OE}$ is high. Write cycles can be executed using either $\overline{WE}$ or $\overline{CE}$, with the address input being latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last. Data, conversely, is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and the new data is written within 10ms.

PAGE WRITE
The page write mode of the CAT28C65A (essentially an extended BYTE WRITE mode) allows from 1 to 32 bytes of data to be programmed within a single 10ms nonvolatile write cycle. This effectively reduces the byte-write time by a factor of 32.

Following an initial WRITE operation ($\overline{WE}$ pulsed low, for t_{WP}, and then high) the page write mode can begin by issuing sequential $\overline{WE}$ pulses, which load the address and data bytes into a 32 byte temporary buffer. The page address where data is to be written, specified by bits A5 to A12, is latched on the first falling edge of $\overline{WE}$. Each byte within the page is defined by address bits A0 to A4 (which can be loaded in any order) during the first and subsequent write cycles. Each data load cycle must begin within t_{PLMIN} of the rising edge of the preceding $\overline{WE}$ pulse. There is no page write window limitation as long as $\overline{WE}$ is pulsed low within t_{PLMIN}.

Upon completion of the page write sequence, $\overline{WE}$ must stay high a minimum of t_{PLMAX} for the internal automatic program cycle to commence. This programming cycle consists of an erase cycle, which erases any data that existed in each addressed cell, and a write cycle, which writes new data back into the cell. A page write will only write data to the locations that were addressed and will not rewrite the entire page.

DATA POLLING
$\overline{Data}$ polling is provided to indicate the completion of a byte write cycle. Once a byte write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O_7 (I/O_0-I/O_6 are indeterminate) until the programming cycle is complete. Upon completion of the self-timed byte write cycle all I/Os will output true data during a read cycle.

FALSE WRITE PROTECTION
(I) The CAT28C65A has an on-chip V_{CC} sense circuit which disables the internal write circuitry whenever V_{CC} is less than 3.0V.

(2) During power-up, write operations are inhibited for 5ms to 20ms after V_{CC} reaches 3.0V. Read cycles are not affected during this initialization period.

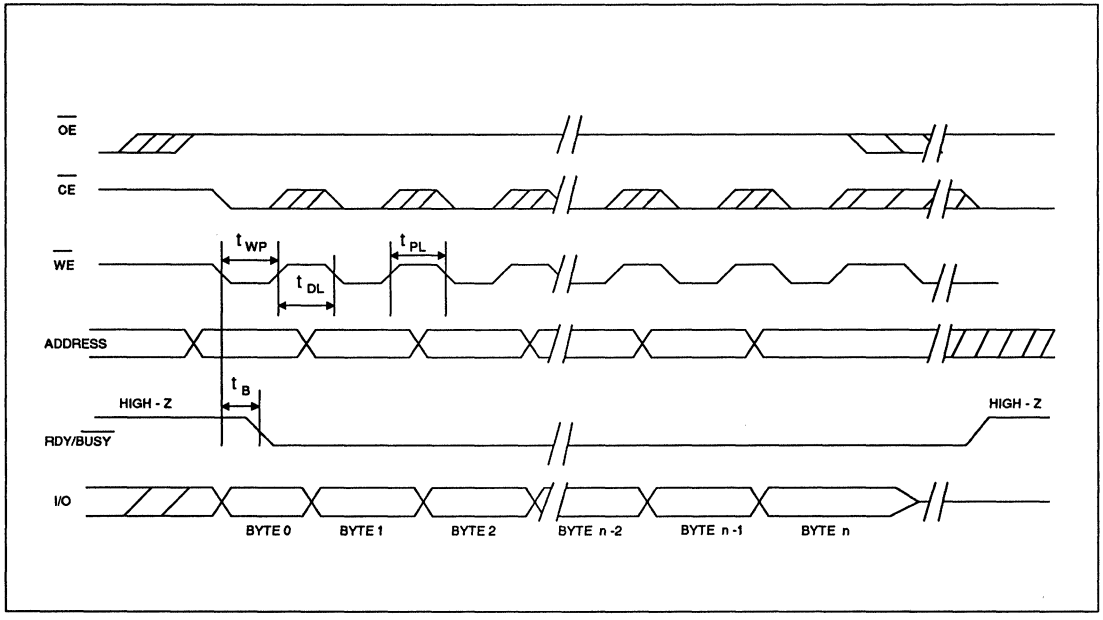
(3) Write cycles are inhibited if $\overline{OE}$ is LOW, or $\overline{CE}$ or $\overline{WE}$ are HIGH.

(4) A write pulse of less than 20ns duration will not initiate a write cycle.

READY/BUSY (RDY/$\overline{BUSY}$)

The RDY/$\overline{BUSY}$ pin is an open drain output which indicates device status during programming. It is pulled low during the write cycle and released at the end of programming. Several devices may be OR-tied to the same RDY/$\overline{BUSY}$ line.

PAGE MODE WRITE CYCLE



CAT28C256

32K x 8 BIT CMOS E^{2}PROM

Preliminary

DESCRIPTION

The CAT28C256 is a fast, low power, 5V-only CMOS E^{2}PROM requiring a simple interface for in-system programming.

On-chip address and data latches, self-timed write cycle with auto-erase and V_{CC} power up/down write protection eliminate additional timing and protection hardware. Data polling is provided to allow the user to minimize write cycle time. Page write mode reduces programming time.

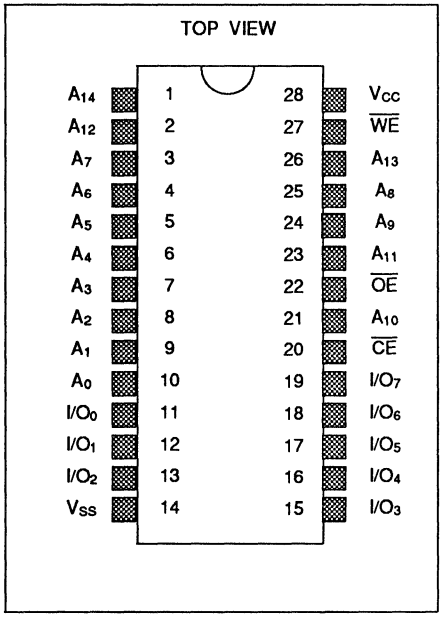
The CAT28C256 is fabricated in reliable floating gate CMOS technology. It is designed for up to10,000 write cycles and 10 years data retention.

FEATURES

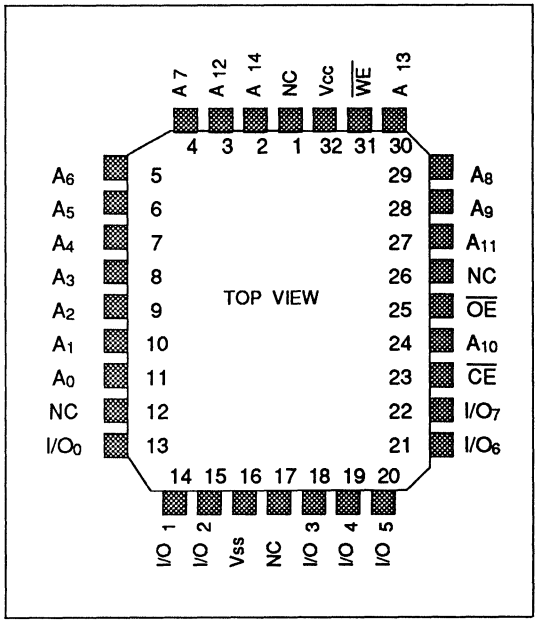
- Fast read access time: 200ns/250ns/300ns
- Low CMOS power:
  - Active: 30mA max
  - Standby: 100µA max
- 5V-only operation
- Simple write operation:
  - On-chip address and data latches
  - Self-timed write cycle with auto-erase
  - Data polling
- Fast nonvolatile write cycle: 10ms max
- Automatic page write: 1 to 64 bytes in 10ms
- TTL compatible I/O
- JEDEC approved 28-pin DIP,Small Outline, and 32-pin PLCC packages available.
- 10,000 rewrites/byte, 10 year data retention
- On-chip error correction for enhanced reliability
- Power-up inadvertent write protection

PIN CONFIGURATION

28-Pin DIP and S.O.



32-Pin PLCC



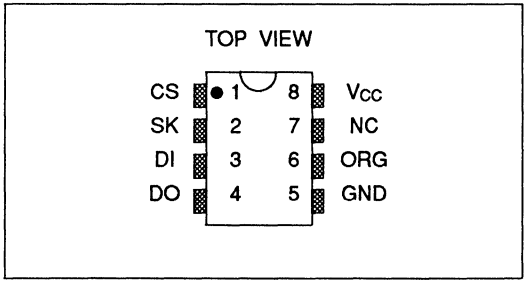
CAT33C104
4K BIT SERIAL E^2PROM

3-VOLT ONLY OPERATION

DESCRIPTION

The CAT33C104 is a 3V CMOS 4K-bit serial E^2PROM with a low current drain of 2mA (write), 0.5mA (read) in the active mode and 50µA standby. Its configuration is user selectable as either 256 registers by 16 bits or 512 registers by 8 bits and has been designed to interface serially with industry standard microcontrollers. Manufactured using Catalyst's Advanced CMOS E^2PROM floating gate technology, the device can endure 10,000 erase/write cycles and has a data retention of 10 years. The CAT33C104 is assembled in either 8-pin DIP or S.O. package.

PIN CONFIGURATION DIP AND S.O.



PIN FUNCTIONS

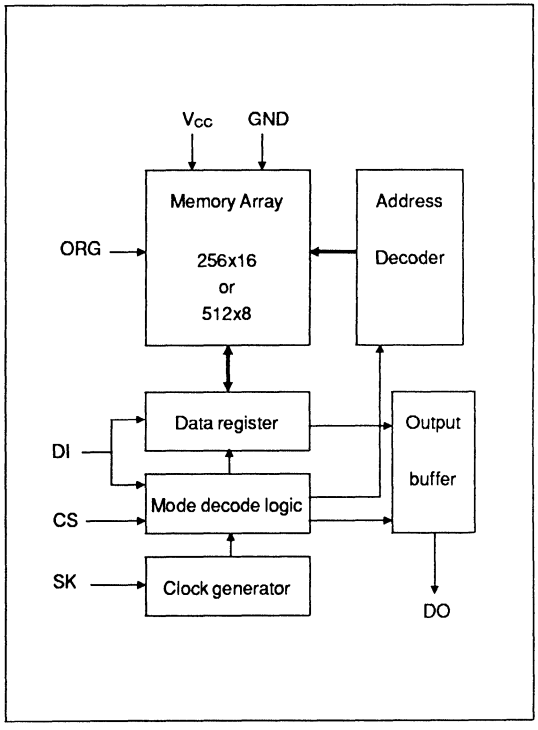
CS	Chip select
SK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+3V power supply
GND	Ground
NC	No connection
ORG	Memory organization

Note: When the **ORG** pin is connected to Vcc, the 256x16 organization is selected. When it is connected to ground, the 512x8 organization is selected. If the ORG pin is left unconnected, an internal pullup device will select the 256x16 organization.

FEATURES

- Single 3V supply (also available as a CAT35C104 single 5V supply)
- 256x16 or 512x8 user selectable serial memory
- Microwire™ compatible
- Self timed programming cycle with Autoerase
- Available in 8-pin DIP or S.O. package
- Highly reliable CMOS floating gate technology
- Operating range 0°C to 70°C [industrial temp. range available]
- 10,000 erase/write cycles
- 10 year data retention
- Power-up inadvertent write protection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature T_{stg} . . . . . -65°C to +150°C
Power supply V_{CC} . . . . . +7 V
Voltage on any input pin . . . . . -0.3 to +7V
Voltage on any output pin . . . . . -0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +3V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter		Conditions	Limits Min.	Typ.	Max.	Unit
I_{CC1}	Current consumption	Write	DI=0.0V,SK=3.0V,V_{CC}=3.0V, CS=3.0V, Output unloaded			2.0	mA
		Read				0.5	
I_{CC2}	Current consumption (standby)		V_{CC} = 3.3V, CS = 0V DI = 0V, SK = 0V			50	µA
I_{LI}	Input leakage current		V_{IN} = V_{CC}+0.1V			10	µA
I_{LO}	Output leakage current		V_{OUT} = V_{CC}, CS = 0			10	µA
V_{IH}	High level input voltage			V_{CC} -0.3		V_{CC} +1	V
V_{IL}	Low level input voltage			-0.1		0.3	V
V_{OH}	High level output voltage		I_{OH} = -10µA	V_{CC}-0.3			V
V_{OL}	Low level output voltage		I_{OL} = 10µA			0.3	V

INSTRUCTION SET

Instruction	Start Bit	Opcode	Address 512 x 8	Address 256 x 16	Data 512 x 8	Data 256 x 16	Comments
READ	1	1 0	A8 - A0	A7 - A0			Read address AN - A0
ERASE	1	1 1	A8 - A0	A7 - A0			Erase address AN - A0
WRITE	1	0 1	A8 - A0	A7 - A0	D7 - D0	D15 - D0	Write address AN - A0
EWEN	1	0 0	11XXXXXXX	11XXXXXX			Program enable
EWDS	1	0 0	00XXXXXXX	00XXXXXX			Program disable
ERAL	1	0 0	10XXXXXXX	10XXXXXX			Erase all addresses

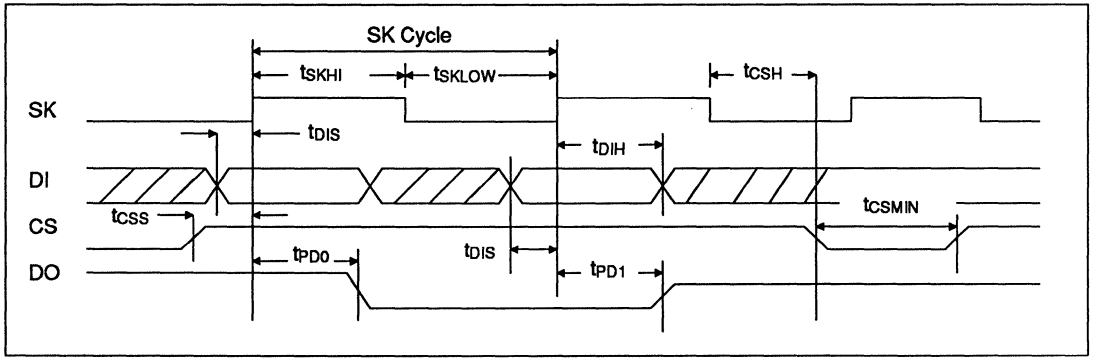
AC CHARACTERISTICS

(V_{CC} = +3V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{CSS}	CS setup time		0.2			µs
t_{CSH}	CS hold time	C_L = 100pF See Note 1. below	0			µs
t_{DIS}	DI setup time		0.4			µs
t_{DIH}	DI hold time		0.4			µs
t_{PD1}	Output delay to 1				2	µs
t_{PD0}	Output delay to 0				2	µs
t_{HZ}	Output delay to High-Z				0.4	µs
t_{EW}	Erase/Write pulse width				20	ms
t_{CSMIN}	Minimum CS low time		1			µs
t_{SKHI}	Minimum SK high time		1			µs
t_{SKLOW}	Minumun SK low time		1			µs
t_{SV}	Output delay to status valid	C_L = 100pF			1	µs
SK_{MAX}	Maximum frequency		DC		250	kHz

Note 1. All timing measurements on the CAT33C104 are defined at the point of signal crossing $V_{CC} \div 2$.

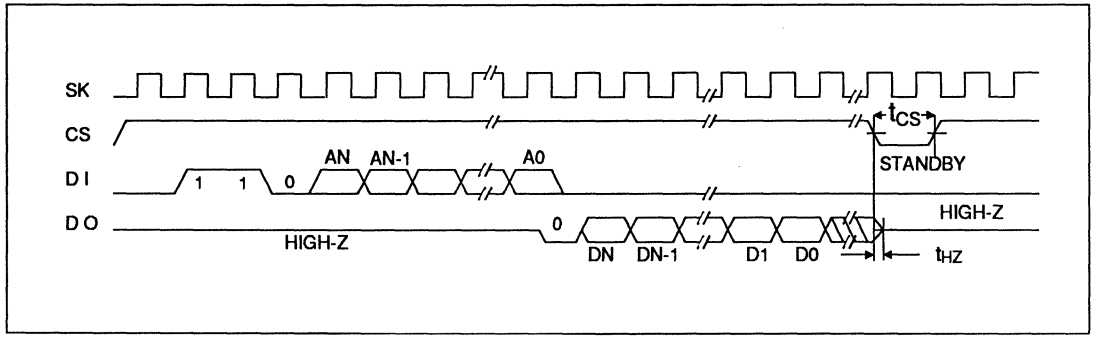
SYNCHRONOUS TIMINGS



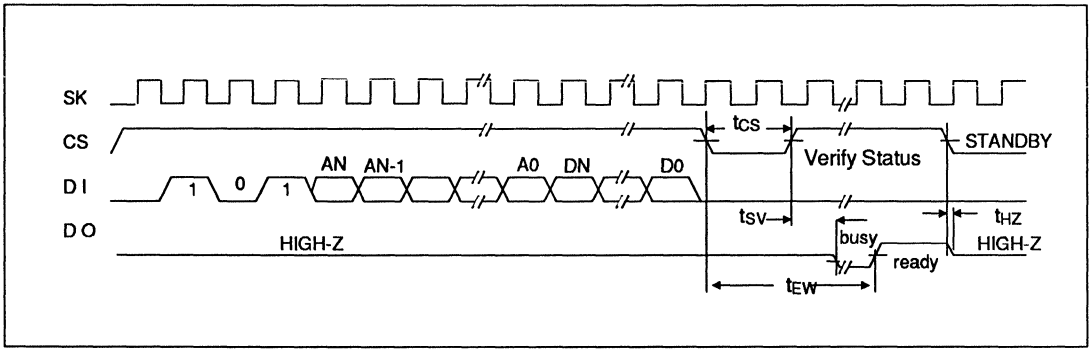
INSTRUCTION TIMING <ORGANIZATION>

Organization	A_N (or AN)	D_N (or DN)
512 x 8	A_8	D_7
256 x 16	A_7	D_{15}

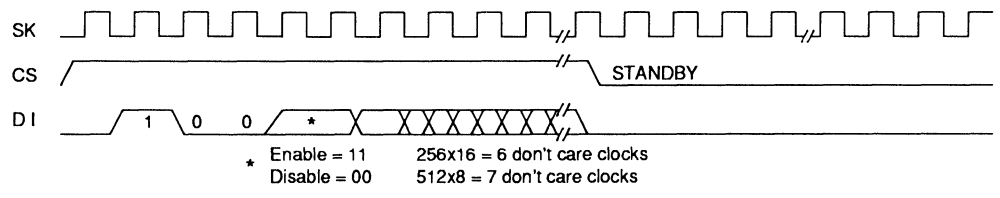
INSTRUCTION TIMING <READ>



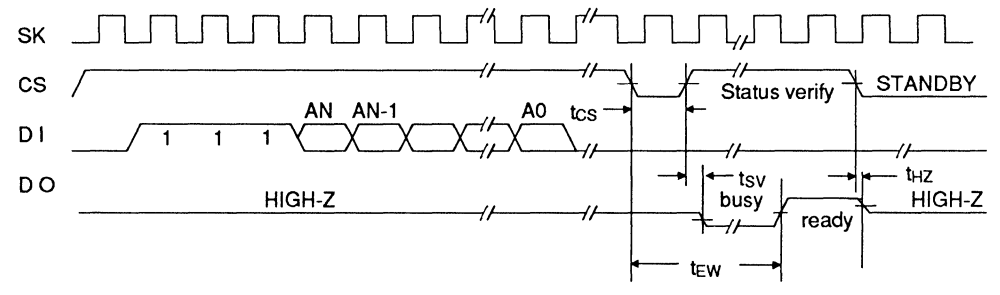
INSTRUCTION TIMING <WRITE>



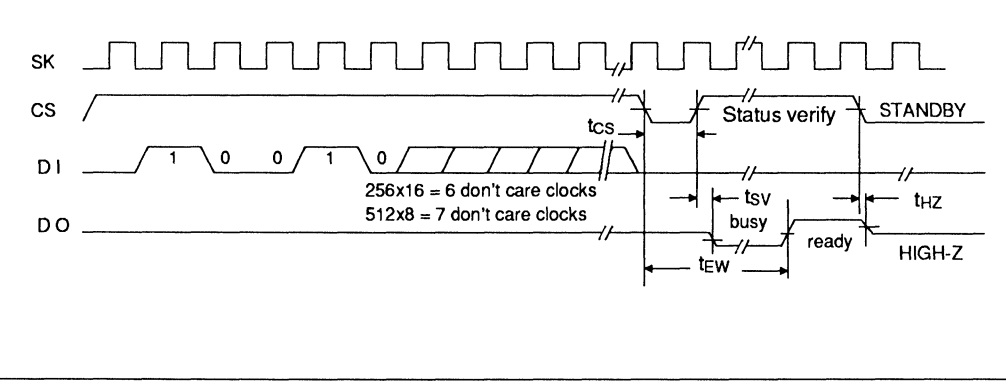
INSTRUCTION TIMING <EWEN, EWDS>



INSTRUCTION TIMING <ERASE>



INSTRUCTION TIMING <ERAL>



DEVICE OPERATION

The CAT33C104 is a 4096 bit nonvolatile memory intended for use with the COPS™ family of microcontrollers, or other standard microprocessors such as the 8048, or 8051. The CAT33C104 can be organized as either 256 registers by 16 bits, or as 512 registers by 8 bits. Six 11-bit instructions (12 bit instructions in 512 by 8 organization) control the reading, writing, and erase operations of the device. The CAT33C104 operates on a single 3V supply and will generate on-chip the high voltage required during any programming operation. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a programming operation. The ready/busy status can be determined after a programming operation by selecting the device and polling the DO pin; DO low indicates that the programming operation is not completed, while DO high indicates that the device is ready. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin. The format for all instructions sent to the CAT33C104 is a logical "1" start bit, a 2 bit (or 4 bit) op code, an 8 bit address (9 bit address when organized as 512 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 512 X 8).

READ

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT33C104 will come out of the high impedance state, and after sending an initial dummy zero bit, will begin shifting out the 16 (or 8) bits of data located at the specified address. The data bits being shifted out will toggle on the rising edge of the SK clock and are stable after the specified time delay t_{PD0} or t_{PD1}.

ERASE/WRITE ENABLE AND DISABLE

The CAT33C104 powers up in the programming disable state. Any programming after power-up or after an EWDS (programming disable) instruction must first be preceded by the EWEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT33C104 programming and erasing functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT33C104 regardless of the programming enable/disable status.

ERASE

Upon receiving an ERASE command and address, the device must be deselected for a minimum of 1μs (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT33C104 can be determined by selecting the device and polling the DO pin.

WRITE

After receiving a WRITE command, address and data, the device must be deselected for a minimum of 1μs (T_{CSMIN}). The falling edge of CS will start the self clocking erase and data store cycle of the memory register specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT33C104 can be determined by selecting the device and polling the DO pin. With the CAT33C104 it is **NOT** necessary to erase a memory register before the WRITE command.

ERASE ALL

Upon receiving an ERAL command, the device must be deselected for a minimum of 1μs (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT33C104 can be determined by selecting the device and polling the DO pin.

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CAT33C204
4K BIT SERIAL E^2PROM

3Volt OPERATION

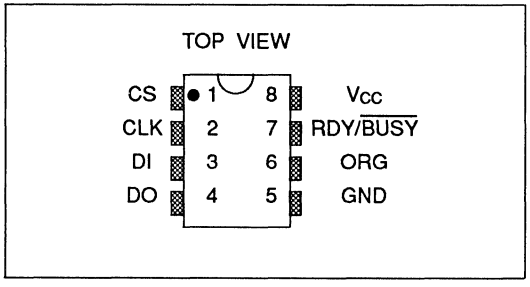
DESCRIPTION

The CAT33C204 is a 4K bit Serial E^2PROM memory device organized in 256 registers of 16 bits (ORG pin at V_{CC}) or 512 registers of 8 bits each (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT33C204 is manufactured using Catalyst's advanced CMOS E^2PROM floating gate technology. It is designed to endure 10,000 erase/write cycles and has a data retention of 10 years. It is packaged in an 8-pin DIP and Small Outline packages. It is also available in a 5V version (CAT35C204).

FEATURES

- Compatible with General Instruments ER5912
- Single 3V supply
- 256x16 or 512x8 user selectable serial memory
- 20ms programming cycle
- Self timed programming cycle with Autoerase
- Highly reliable CMOS floating gate technology
- Word and chip erasable
- Operating range 0°C to +70°C [Industrial temp. range available]
- 10,000 erase/write cycles
- 10 year data retention
- Power-up inadvertent write protection

PIN CONFIGURATION

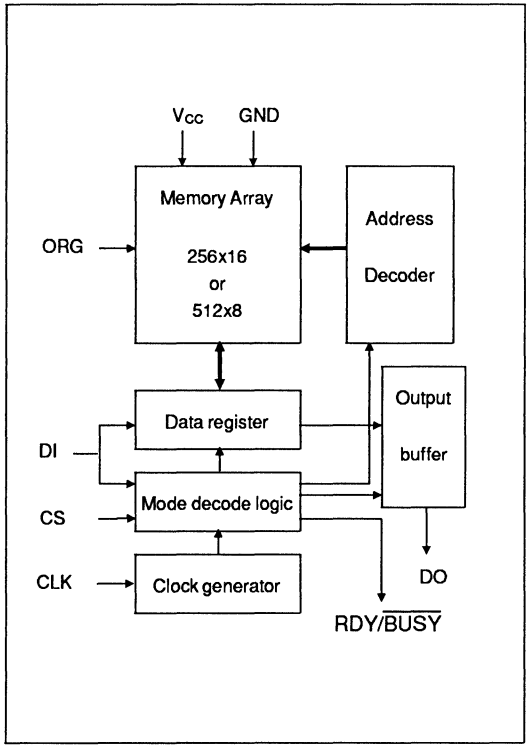


PIN FUNCTIONS

CS	Chip select
CLK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
RDY/BUSY	Status output
GND	Ground
ORG	Memory organization

Note: When the ORG pin is connected to V_{CC}, the 256x16 organization is selected. When it is connected to ground, the 512x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 256x16 organization.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature . . . . . -65°C to +150°C
Power supply (V_{CC}) . . . . . +7V
Voltage on any input pin . . . . . -0.3 to +7V
Voltage on any output pin . . . . . -0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +3V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter		Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
I_{CC1}	Current consumption	Write	Vcc=3.0V, CS=3.0V, DI=0.0V			2.0	mA
		Read	SK=3.0V, DO Unloaded			0.5	
I_{CC2}	Current consumption (stand-by)		V_{CC} = 3.3V, CS = 0V DI = 0V, SK = 0V			50	µA
I_{LI}	Input leakage current		V_{IN} = V_{CC}+0.1V			10	µA
I_{LO}	Output leakage current		V_{OUT} = V_{CC}, CS = 0			10	µA
V_{IH}	High level input voltage			V_{CC} -0.3		V_{CC} +1	V
V_{IL}	Low level input voltage			-0.1		0.3	V
V_{OH}	High level output voltage		I_{OH} = -10µA	V_{CC}-0.3			V
V_{OL}	Low level output voltage		I_{OL} = 10µA			0.3	V

INSTRUCTION SET

Instruction	Start Bit	Opcode	Address 512 x 8	Address 256 x 16	Data 512 x 8	Data 256 x 16	Comments
READ	1	1000	A8 - A0	A7 - A0			Read address AN - A0
PROGRAM	1	X100	A8 - A0	A7 - A0	D7 - D0	D15 - D0	Program address AN - A0
PEN	1	0011	000000000	00000000			Program enable
PDS	1	0000	000000000	00000000			Program disable
ERAL	1	0010	000000000	00000000			Erase all addresses
WRAL	1	0001	000000000	00000000	D7 - D0	D15 - D0	Write all addresses

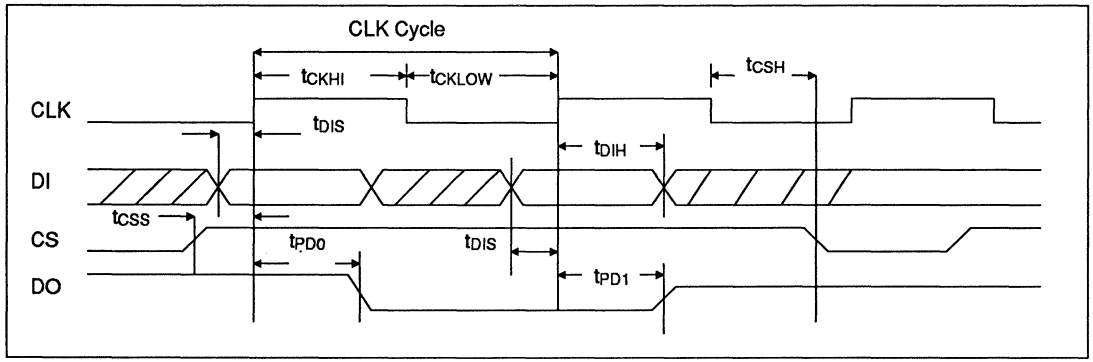
AC CHARACTERISTICS

(V_{CC} = +3V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{CSS}	CS setup time		0.2			µs
t_{CSH}	CS hold time	C_L = 100pF See Note 1. below	0			µs
t_{DIS}	DI setup time		0.4			µs
t_{DIH}	DI hold time		0.4			µs
t_{PD1}	Output delay to 1				2	µs
t_{PD0}	Output delay to 0				2	µs
t_{EW}	Erase/Write pulse width				20	ms
t_{SKHI}	Minimum SK high time		1			µs
t_{SKLOW}	Minumun SK low time		1			µs
CK_{MAX}	Maximum frequency		DC		250	KHz

Note 1. All timing measurements on the CAT33C204 are defined at the point of signal crossing V_{CC} ÷ 2.

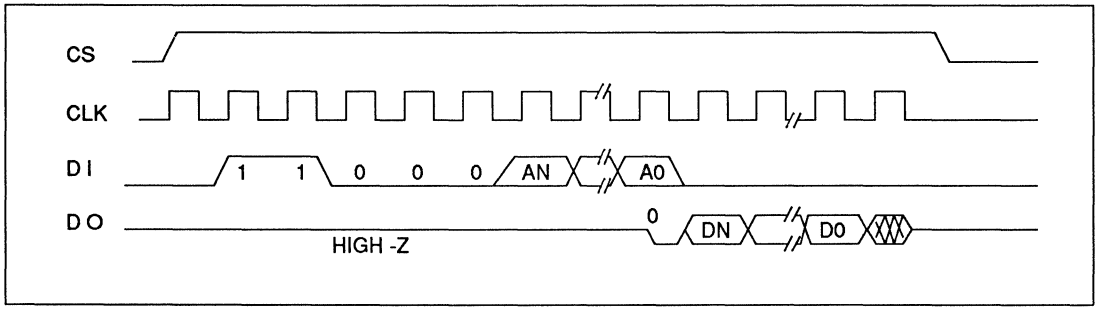
SYNCHRONOUS TIMINGS



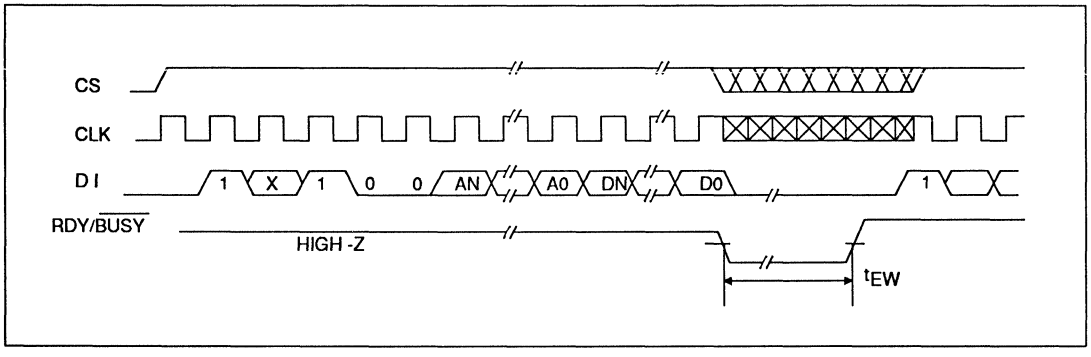
INSTRUCTION TIMING <ORGANIZATION>

Organization	A_N (or AN)	D_N (or DN)
512 x 8	A_8	D_7
256 x 16	A_7	D_{15}

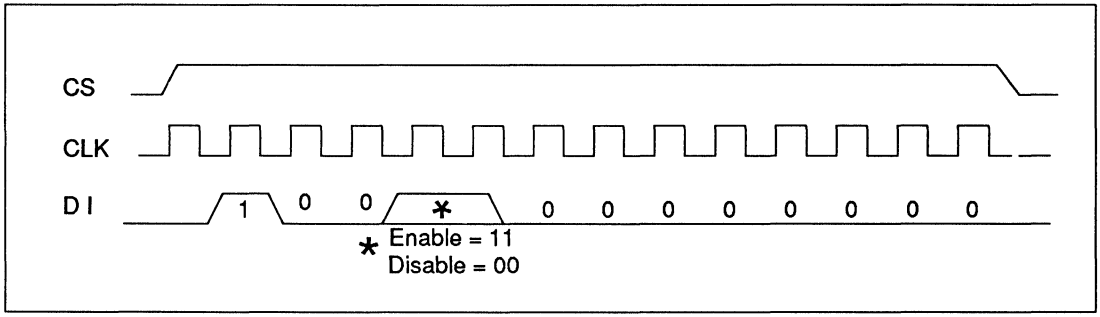
INSTRUCTION TIMING <READ>



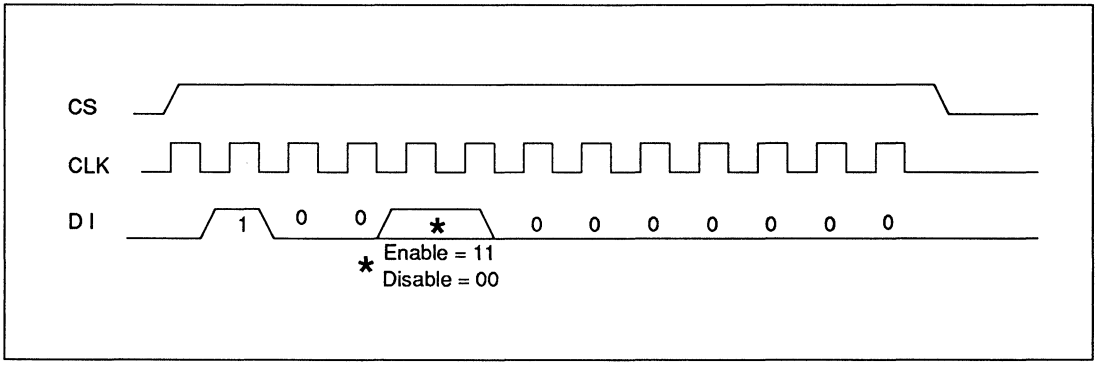
INSTRUCTION TIMING <PROGRAM>



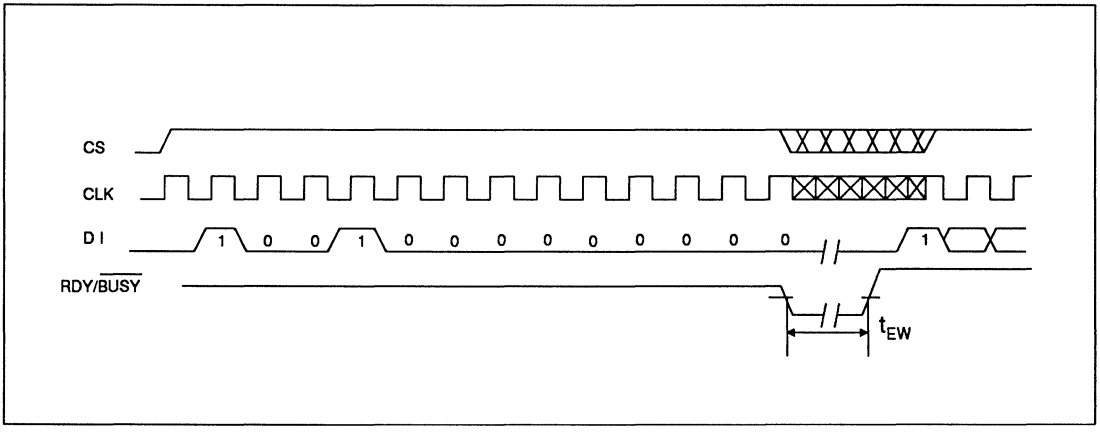
INSTRUCTION TIMING <PEN, PDS 512 x 8 organization>



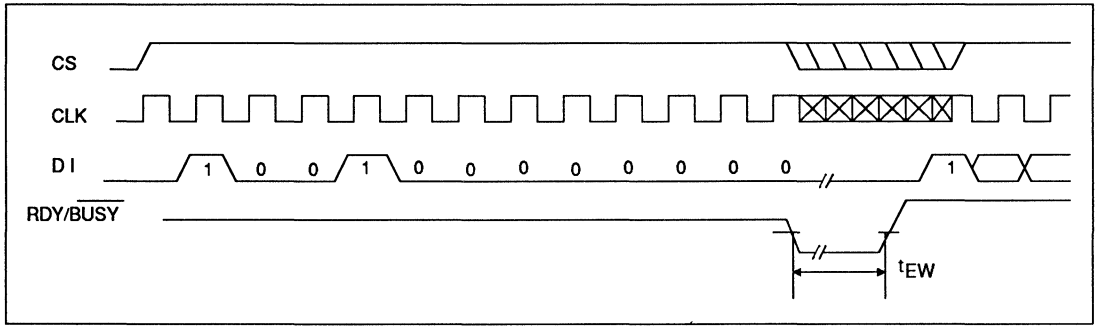
INSTRUCTION TIMING <PEN, PDS 256 x 16 organization>



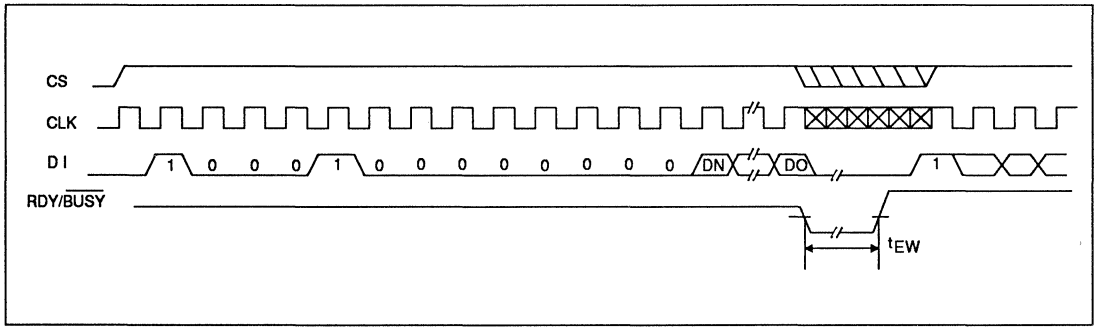
INSTRUCTION TIMING <ERAL 512 x 8 organization>



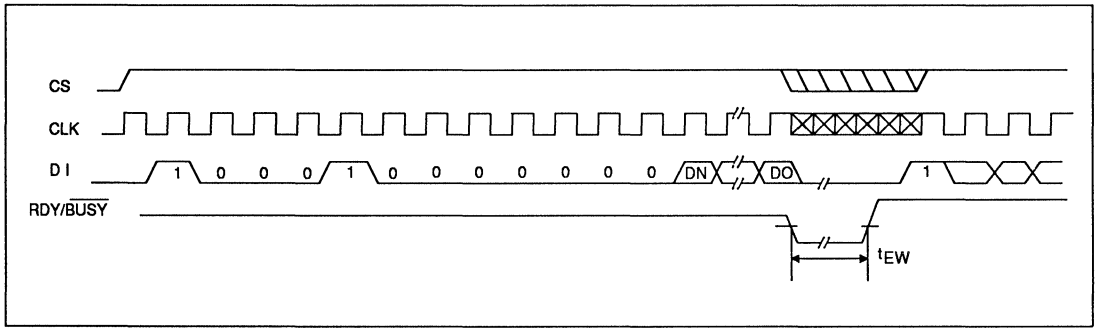
INSTRUCTION TIMING <ERAL 256 x 16 organization>



INSTRUCTION TIMING <WRAL 512 x 8 organization>



INSTRUCTION TIMING <WRAL 256 x 16 organization>



DEVICE OPERATION

The CAT33C204 is a 4096 bit nonvolatile memory intended for use with all standard controllers. The CAT33C204 can be organized as either 256 registers by 16 bits, or as 512 registers by 8 bits. Seven 11 bit instructions (12 bit instruction in 512 by 8 organization) control the reading, writing, and erase operations of the device. The CAT33C204 operates on a single 3V supply and will generate on chip the high voltage required during any programming operations. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normal in a high impedance state except when reading data from the device. The ready/busy status can be determined after a programming operation by polling the RDY/BUSY pin.

The format for all instructions sent to the

CAT33C204 is one logical "1" start bit, a 4 bit op code, an 8 bit address (9 bit address when organized as 512 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 512 X 8).

READ

Upon receiving a READ command and address (clocked into the DI pin), the DO pin of the CAT33C204 will come out of the high impedance state. After sending 1 dummy zero bit the 16 bits (or 8 bits) of data located at the address location specified in the instruction will be shifted out. The data bit being shifted out will toggle on the rising edge of the CLK and becomes stable after the specified time delay (t_{PD1} and t_{PD0}).

ERASE/WRITE ENABLE AND DISABLE

The CAT33C204 powers up in the programming disable state. Any programming after power-up or after a PDS (programming disable) instruction must first be preceded by the PEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed or the PDS instruction is sent. The PDS instruction can be used to disable all the CAT33C204's program and erase functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT33C204 regardless of the programming enable/disable status.

PROGRAM

After receiving a PROGRAM command, address, and the data, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking erase and data store cycle begins. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT33C204 can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin.

ERASE ALL

Upon receiving an ERAL command, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking erase sequence starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT33C204 can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin. Once erased, all memory bits return to logical "1" state.

CAT35C102
2K BIT SERIAL E²PROM

1 MHz OPERATION

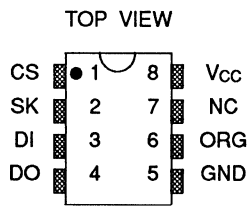
DESCRIPTION

The CAT35C102 is a 2K bit Serial E²PROM memory device organized in 128 registers of 16 bits (ORG pin at Vcc) or 256 registers of 8 bits each (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT35C102H is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 10,000 erase/write cycles and has a data retention of 10 years. It is packaged in an 8-pin DIP or S.O. package. It will be offered in a 3V version (CAT33C102).

FEATURES

- High speed 1MHz operation
- Single 5V supply
- Available in 8 pin DIP or S.O. package
- 128x16 or 256x8 user selectable serial memory
- Microwire™ compatible
- Highly reliable CMOS floating gate technology
- Self timed programming cycle with Autoerase
- Operating range 0°C to 70°C [industrial temp. range available]
- 10,000 erase/write cycles
- 10 year data retention
- Power-up inadvertent write protection

PIN CONFIGURATION

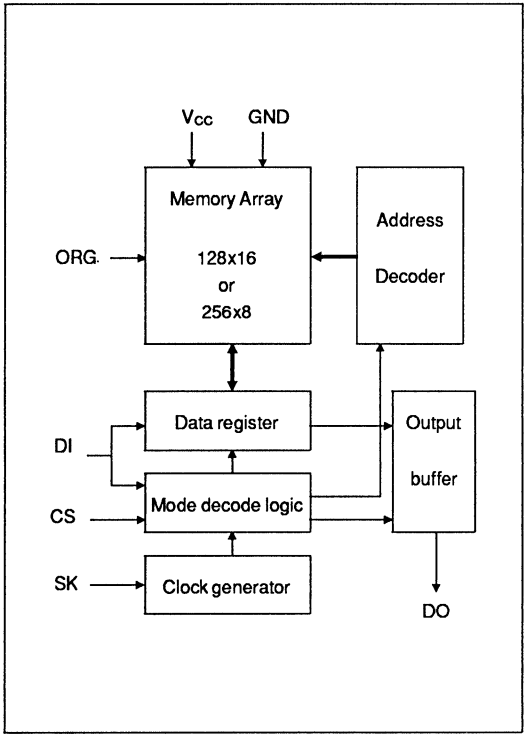


PIN FUNCTIONS

CS	Chip select
SK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
GND	Ground
NC	No connection
ORG	Memory organization

Note: When the ORG pin is connected to Vcc, the 128x16 organization is selected. When it is connected to ground, the 256x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 128x16 organization.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature . . . . . -65°C to +150°C
Power supply (V_{CC}) . . . . . +7V
Voltage on any input pin . . . . . -0.3 to +7V
Voltage on any output pin . . . . . -0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC1}	Current consumption (operating)	DI=0.0V, SK=5.0V V_{CC} =5.0V, CS = 5.0V Output unloaded			3	mA
I_{CC2}	Current consumption (standby)	V_{CC} = 5.5V, CS = 0 DI = 0, SK = 0			100	µA
I_{LI}	Input leakage current	V_{IN} = 5.5V			10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V, CS = 0			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V

INSTRUCTION SET

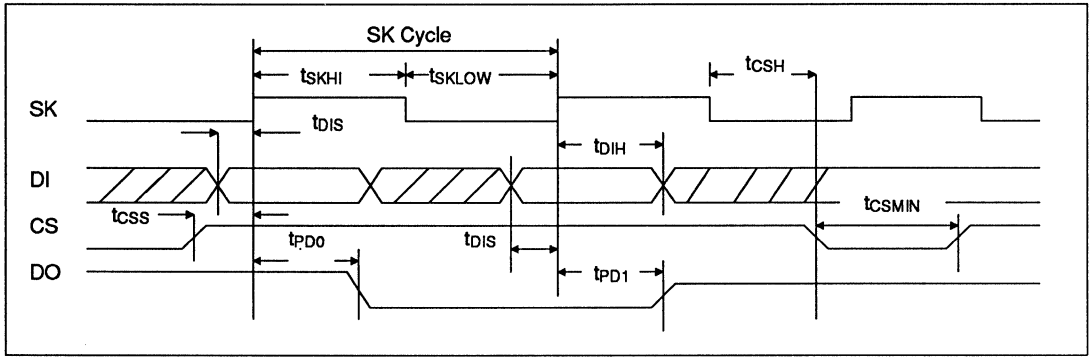
Instruction	Start Bit	Opcode	Address		Data		Comments
			256 x 8	128 x 16	256 x 8	128 x 16	
READ	1	1 0	A7 - A0	A6 - A0			Read address AN - A0
ERASE	1	1 1	A7 - A0	A6 - A0			Erase address AN - A0
WRITE	1	0 1	A7 - A0	A6 - A0	D7 - D0	D15 - D0	Write address AN - A0
EWEN	1	0 0	11XXXXXX	11XXXXX			Program enable
EWDS	1	0 0	00XXXXXX	00XXXXX			Program disable
ERAL	1	0 0	10XXXXXX	10XXXXX			Erase all addresses
WRAL	1	0 0	01XXXXXX	01XXXXX	D7 - D0	D15 - D0	Program all addresses

AC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{CSS}	CS setup time		50			ns
t_{CSH}	CS hold time	C_L = 100pF V_{OL} = 0.8V, V_{OH} = 2.0V V_{IL} = 0.45V, V_{IH} = 2.4V	0			ns
t_{DIS}	DI setup time		100			ns
t_{DIH}	DI hold time		100			ns
t_{PD1}	Output delay to 1				500	ns
t_{PD0}	Output delay to 0				500	ns
t_{HZ}	Output delay to Hi-Z				100	ns
t_{EW}	Erase/Write pulse width				10	ms
t_{CSMIN}	Minimum CS low time		250			ns
t_{SKHI}	Minimum SK high time		250			ns
t_{SKLOW}	Minimum SK low time		250			ns
t_{SV}	Output delay to status valid	C_L = 100pF			500	ns
SK_{MAX}	Maximum clock frequency		DC		1	MHz

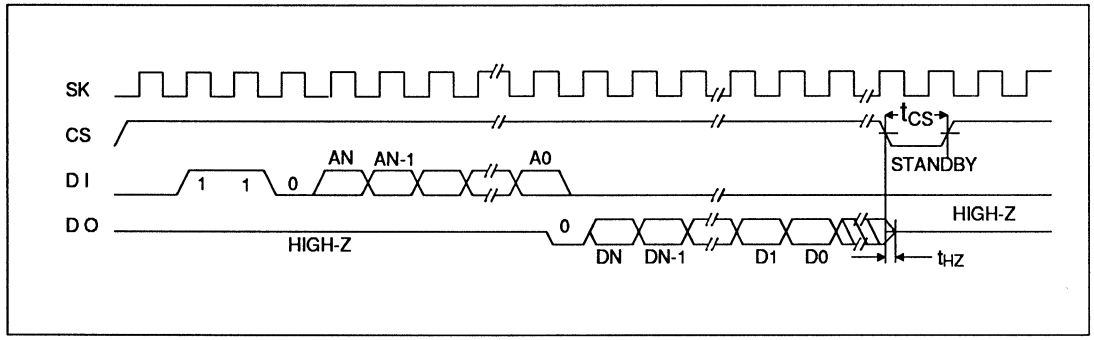
SYNCHRONOUS TIMINGS



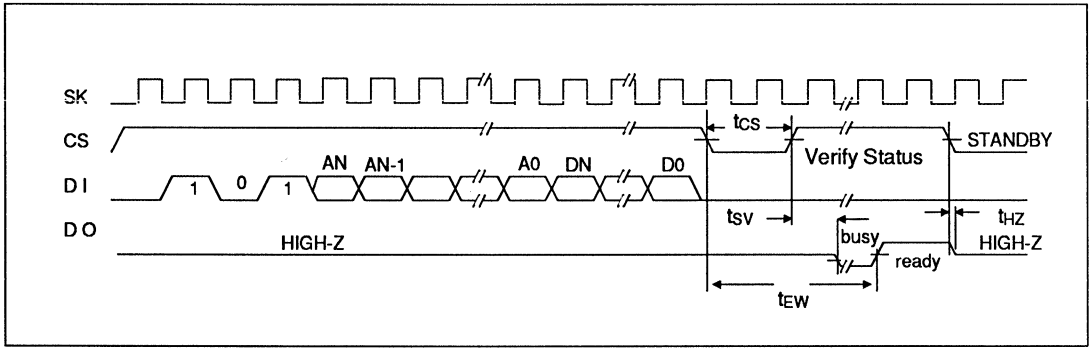
INSTRUCTION TIMING <ORGANIZATION>

Organization	A_N (or AN)	D_N (or DN)
256 x 8	A_7	D_7
128 x 16	A_6	D_{15}

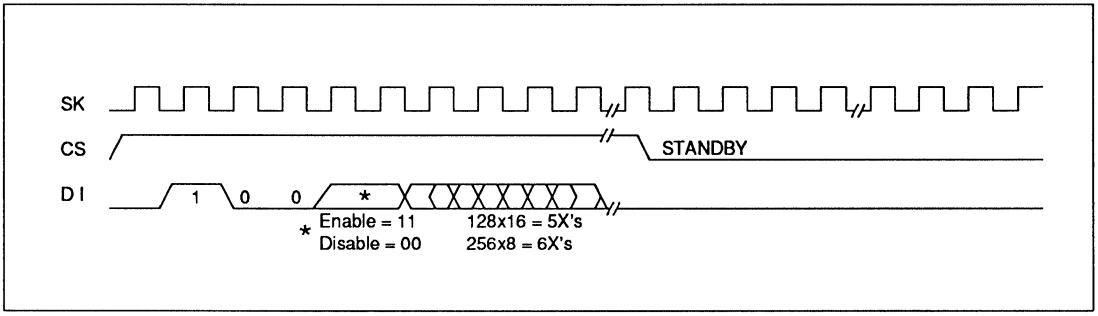
INSTRUCTION TIMING <READ>



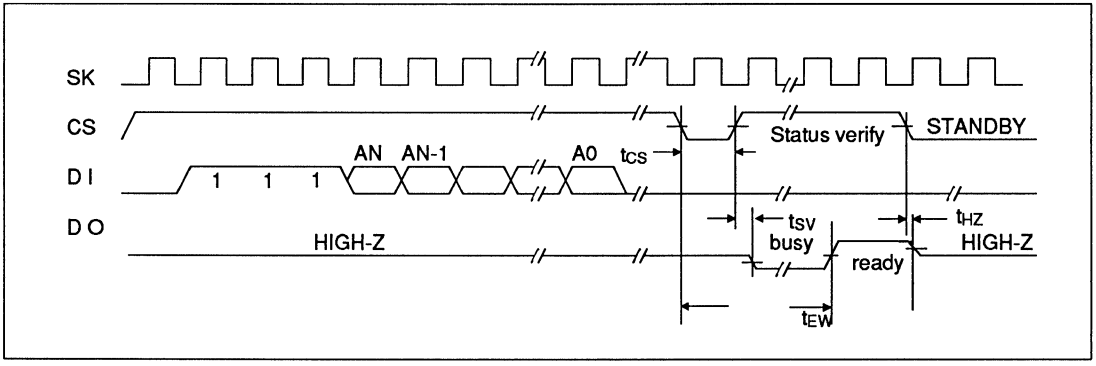
INSTRUCTION TIMING <WRITE>



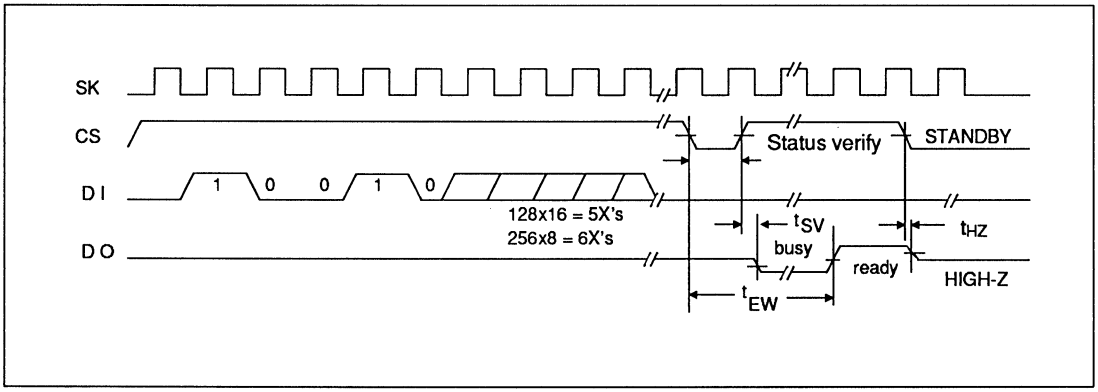
INSTRUCTION TIMING <EWEN, EWDS>



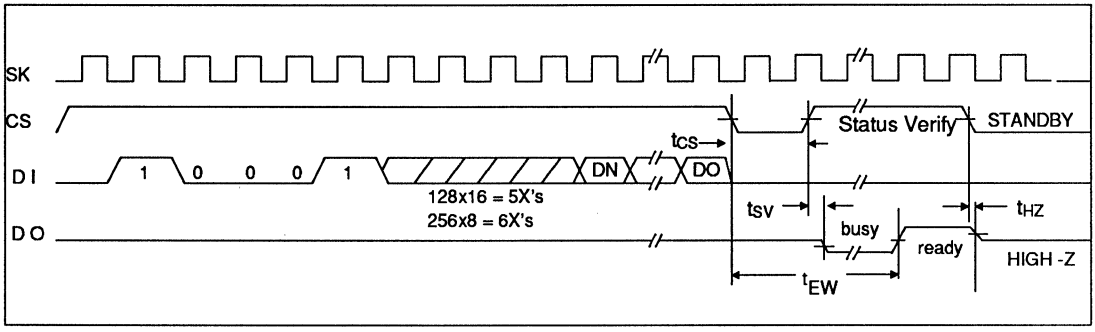
INSTRUCTION TIMING <ERASE>



INSTRUCTION TIMING <ERAL>



INSTRUCTION TIMING <WRAL>



DEVICE OPERATION

The CAT35C102 is a CMOS 2048-bit nonvolatile memory intended for use with the COPS™ family of microcontrollers, or other standard microprocessors. The CAT35C102 can be organized as either 128 registers by 16 bits, or as 256 registers by 8 bits. Seven 10-bit instructions (11 bit instructions in 256 by 8 organization) control the reading, writing and erase operations of the device. The CAT35C102 operates on a single 5V supply and will generate on chip, the high voltage required during any programming operation. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the READY/BUSY status after a programming operation. The READY/BUSY status can be determined after a programming operation by selecting the device and polling the DO pin; DO low indicates that the programming operation is not completed, while DO high indicates that the device is ready. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and and the DO pin are to be tied together to form a common DI/O pin. The format for all instructions sent to the CAT35C102 is a logical "1" start bit, a 2 bit (or 4 bit) op code, a 7 bit address (8 bit address when organized as 256 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 256 X 8).

READ

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT35C102 will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed. The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

ERASE/WRITE ENABLE AND DISABLE

The CAT35C102 powers up in the programming disable state. Any programming after power-up or after an EWDS (programming disable) instruction must first be preceded by the EWEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT35C102 programming and erasing functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT35C102 regardless of the programming enable/disable status.

ERASE

Upon receiving an ERASE command and address, the CS (chip select) must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The READY/BUSY status of the CAT35C102 can be determined by selecting the device and polling the DO pin. Once

erased, the contents of an erased location returns to a logical "1" state.

WRITE

After receiving a WRITE command, address and the data, the CS (chip select) must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C102 can be determined by selecting the device and polling the DO pin. With the CAT35C102 it is **NOT** necessary to erase a memory location before the WRITE command.

ERASE ALL

Upon receiving an ERAL command, the CS (chip select) must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C102 can be determined by selecting the device and polling the DO pin. Once erased, all memory bits return to a logical "1" state.

WRITE ALL

Upon receiving a WRAL command and data, the CS (chip select) must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C102 can be determined by selecting the device and polling the DO pin. It **IS** necessary for all memory locations to be erased before the WRAL command is executed.

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CAT35C102H - High Endurance 1 MHz 2K BIT SERIAL E^2PROM OPERATION

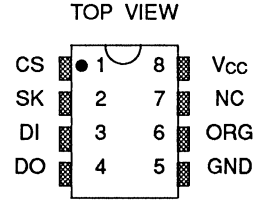
DESCRIPTION

The CAT35C102H is a high endurance 2K bit Serial E^2PROM memory device organized in 128 registers of 16 bits (ORG pin at V_{CC}) or 256 registers of 8 bits each (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT35C102H is manufactured using Catalyst's advanced CMOS E^2PROM floating gate technology. It is designed to endure 100,000 erase/write cycles and has a data retention of 100 years. It is packaged in an 8-pin DIP or S.O. package. It will be offered in a 3V version (CAT33C102H).

FEATURES

- High speed 1MHz operation
- Single 5V supply
- Available in 8 pin DIP or S.O. package
- 128x16 or 256x8 user selectable serial memory
- Mircowire™ compatible
- Highly reliable CMOS floating gate technology
- Self timed programming cycle with Autoerase
- Operating range 0°C to 70°C
- 100,000 erase/write cycles
- 100 year data retention
- Power-up inadvertent write protection

PIN CONFIGURATION

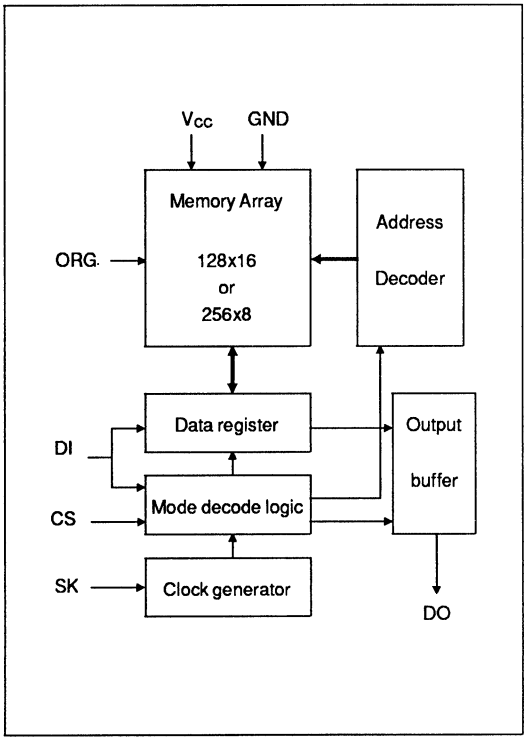


PIN FUNCTIONS

CS	Chip select
SK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
GND	Ground
NC	No connection
ORG	Memory organization

Note: When the ORG pin is connected to V_{CC}, the 128x16 organization is selected. When it is connected to ground, the 256x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 128x16 organization.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature . . . . . -65°C to +150°C
Power supply (V_{CC}) . . . . . +7V
Voltage on any input pin . . . . . -0.3 to +7V
Voltage on any output pin . . . . . -0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC1}	Current consumption (operating)	DI=0.0V, SK=5.0V V_{CC} =5.0V, CS = 5.0V Output unloaded			3	mA
I_{CC2}	Current consumption (stand-by)	V_{CC} = 5.5V, CS = 0 DI = 0, SK = 0			100	µA
I_{LI}	Input leakage current	V_{IN} = 5.5V			10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V, CS = 0			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V

INSTRUCTION SET

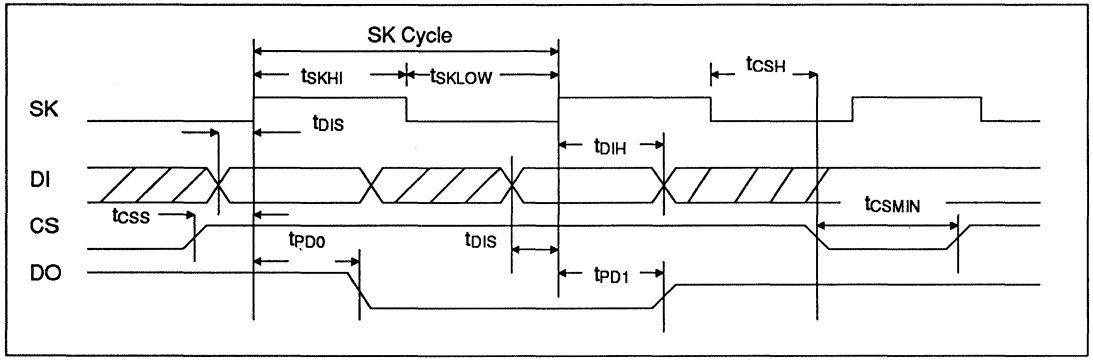
Instruction	Start Bit	Opcode	Address		Data		Comments
			256 x 8	128 x 16	256 x 8	128 x 16	
READ	1	1 0	A7 - A0	A6 - A0			Read address AN - A0
ERASE	1	1 1	A7 - A0	A6 - A0			Erase address AN - A0
WRITE	1	0 1	A7 - A0	A6 - A0	D7 - D0	D15 - D0	Write address AN - A0
EWEN	1	0 0	11XXXXXX	11XXXXX			Program enable
EWDS	1	0 0	00XXXXXX	00XXXXX			Program disable
ERAL	1	0 0	10XXXXXX	10XXXXX			Erase all addresses
WRAL	1	0 0	01XXXXXX	01XXXXX	D7 - D0	D15 - D0	Program all addresses

AC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{CSS}	CS setup time		50			ns
t_{CSH}	CS hold time	C_L = 100pF V_{OL} = 0.8V, V_{OH} = 2.0V V_{IL} = 0.45V, V_{IH} = 2.4V	0			ns
t_{DIS}	DI setup time		100			ns
t_{DIH}	DI hold time		100			ns
t_{PD1}	Output delay to 1				500	ns
t_{PD0}	Output delay to 0				500	ns
t_{HZ}	Output delay to Hi-Z				100	ns
t_{EW}	Erase/Write pulse width				10	ms
t_{CSMIN}	Minimum CS low time		250			ns
t_{SKHI}	Minimum SK high time		250			ns
t_{SKLOW}	Minimum SK low time		250			ns
t_{SV}	Output delay to status valid	C_L = 100pF			500	ns
SK_{MAX}	Maximum clock frequency		DC		1	MHz

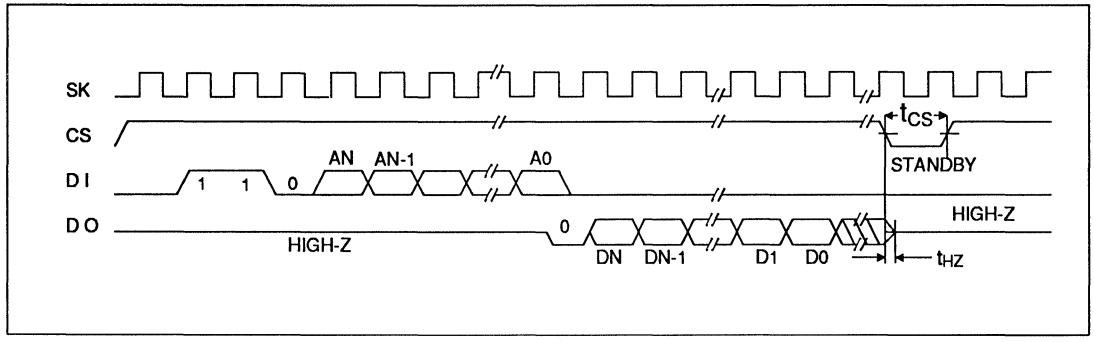
SYNCHRONOUS TIMINGS



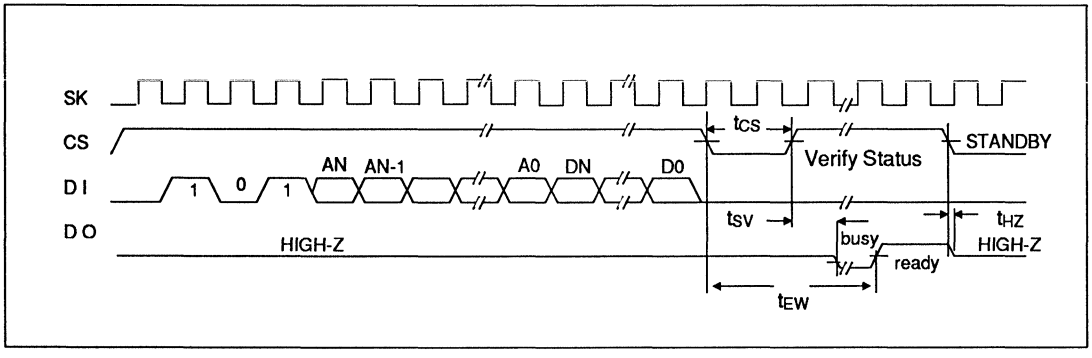
INSTRUCTION TIMING <ORGANIZATION>

Organization	A_N (or AN)	D_N (or DN)
256 x 8	A_7	D_7
128 x 16	A_6	D_{15}

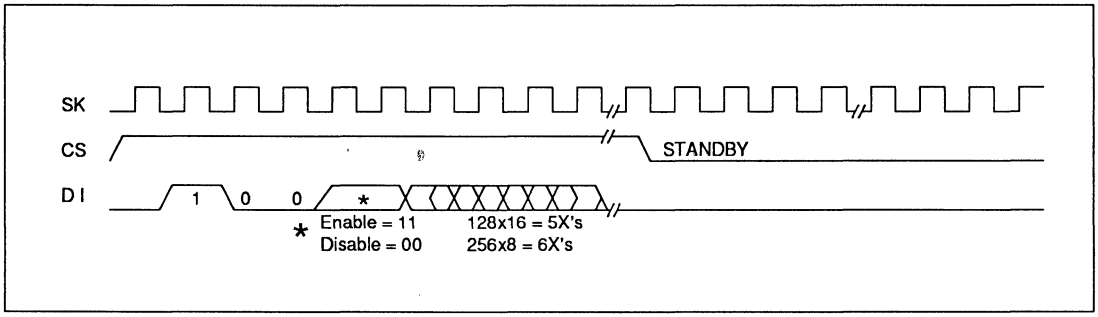
INSTRUCTION TIMING <READ>



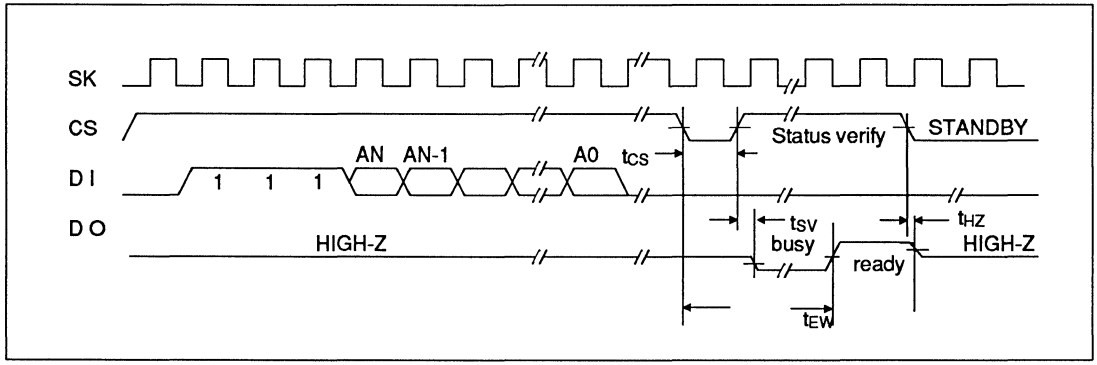
INSTRUCTION TIMING <WRITE>



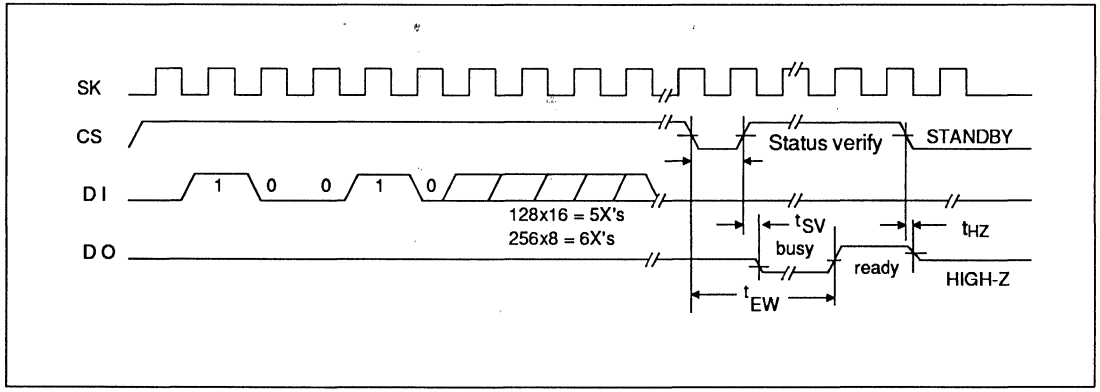
INSTRUCTION TIMING <EWEN, EWDS>



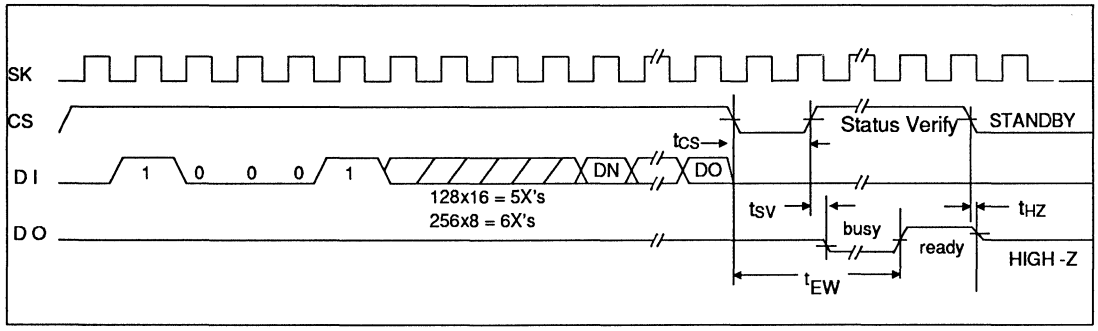
INSTRUCTION TIMING <ERASE>



INSTRUCTION TIMING <ERAL>



INSTRUCTION TIMING <WRAL>



DEVICE OPERATION

The CAT35C102H is a high endurance CMOS 2048-bit nonvolatile memory intended for use with the COPS™ family of microcontrollers, or other standard microprocessors. The CAT35C102H can be organized as either 128 registers by 16 bits, or as 256 registers by 8 bits. Seven 10-bit instructions (11 bit instructions in 256 by 8 organization) control the reading, writing and erase operations of the device. The CAT35C102H operates on a single 5V supply and will generate on chip, the high voltage required during any programming operation. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a programming operation. The ready/busy status can be determined after a programming operation by selecting the device and polling the DO pin; DO low indicates that the programming operation is not completed, while DO high indicates that the device is ready. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and and the DO pin are to be tied together to form a common DI/O pin. The format for all instructions sent to the CAT35C102H is a logical "1" start bit, a 2 bit (or 4 bit) op code, a 7 bit address (8 bit address when organized as 256 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 256 X 8).

READ

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT35C102H will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed. The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

ERASE/WRITE ENABLE AND DISABLE

The CAT35C102H powers up in the programming disable state. Any programming after power-up or after an EWDS (programming disable) instruction must first be preceded by the EWEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT35C102H programming and erasing functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT35C102H regardless of the programming enable/disable status.

ERASE

Upon receiving an ERASE command and address, the CS (chip select) must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C102H can be determined by selecting the device and polling the DO pin. Once

erased, the contents of an erased location returns to a logical "1" state.

WRITE

After receiving a WRITE command, address and the data, the CS (chip select) must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C102H can be determined by selecting the device and polling the DO pin. With the CAT35C102H it is **NOT** necessary to erase a memory location before the WRITE command.

ERASE ALL

Upon receiving an ERAL command, the CS (chip select) must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C102H can be determined by selecting the device and polling the DO pin. Once erased, all memory bits return to a logical "1" state.

WRITE ALL

Upon receiving a WRAL command and data, the CS (chip select) must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C102H can be determined by selecting the device and polling the DO pin. It **IS** necessary for all memory locations to be erased before the WRAL command is executed.

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CAT35C102I - Industrial Temperature 1MHz
2K BIT SERIAL E²PROM OPERATION

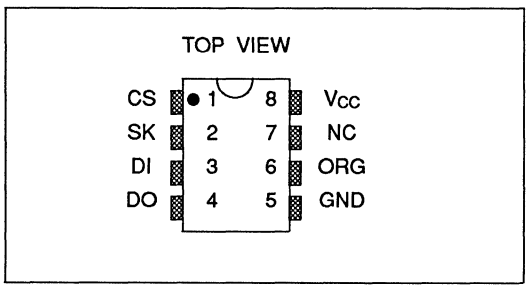
DESCRIPTION

The CAT35C102I is an industrial temperature 2K-bit Serial E²PROM memory device organized in 128 registers of 16 bits (ORG pin at V_{CC}) or 256 registers of 8 bits each (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT35C102I is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 10,000 erase/write cycles and has a data retention of 10 years. It is packaged in an 8-pin DIP or S.O. package.

FEATURES

- High speed 1MHz operation
- Single 5V supply
- Available in 8 pin DIP or S.O. package
- 128x16 or 256x8 user selectable serial memory
- Mircowire™ compatible
- Highly reliable CMOS floating gate technology
- Self timed programming cycle with Autoerase
- Operating range -40°C to +85°C
- 10,000 erase/write cycles
- 10 year data retention
- Power-up inadvertent write protection

PIN CONFIGURATION

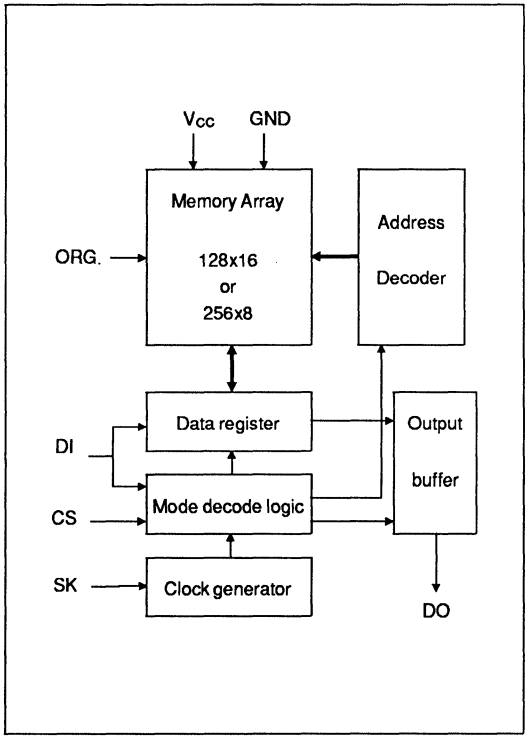


PIN FUNCTIONS

CS	Chip select
SK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
GND	Ground
NC	No connection
ORG	Memory organization

Note: When the ORG pin is connected to V_{CC}, the 128x16 organization is selected. When it is connected to ground, the 256x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 128x16 organization.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature . . . . . -65°C to +150°C
Power supply (V_{CC}) . . . . . +7V
Voltage on any input pin . . . . . -0.3 to +7V
Voltage on any output pin . . . . . -0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC1}	Current consumption (operating)	DI=0.0V, SK=5.0V V_{CC} =5.0V, CS = 5.0V Output unloaded			4	mA
I_{CC2}	Current consumption (standby)	V_{CC} = 5.5V, CS = 0 DI = 0, SK = 0			100	µA
I_{LI}	Input leakage current	V_{IN} = 5.5V			10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V, CS = 0			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V

INSTRUCTION SET

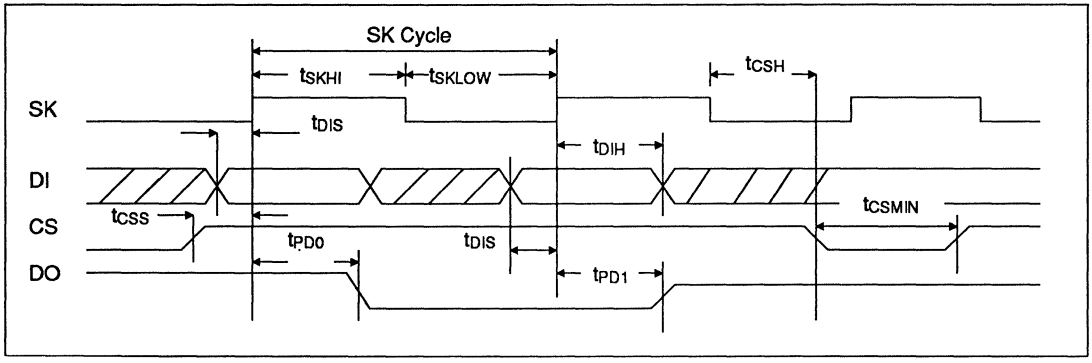
Instruction	Start Bit	Opcode	Address		Data		Comments
			256 x 8	128 x 16	256 x 8	128 x 16	
READ	1	1 0	A7 - A0	A6 - A0			Read address AN - A0
ERASE	1	1 1	A7 - A0	A6 - A0			Erase address AN - A0
WRITE	1	0 1	A7 - A0	A6 - A0	D7 - D0	D15 - D0	Write address AN - A0
EWEN	1	0 0	11XXXXXX	11XXXX			Program enable
EWDS	1	0 0	00XXXXXX	00XXXX			Program disable
ERAL	1	0 0	10XXXXXX	10XXXX			Erase all addresses
WRAL	1	0 0	01XXXXXX	01XXXX	D7 - D0	D15 - D0	Program all addresses

AC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{CSS}	CS setup time		50			ns
t_{CSH}	CS hold time	C_L = 100pF V_{OL} = 0.8V, V_{OH} = 2.0V V_{IL} = 0.45V, V_{IH} = 2.4V	0			ns
t_{DIS}	DI setup time		100			ns
t_{DIH}	DI hold time		100			ns
t_{PD1}	Output delay to 1				500	ns
t_{PD0}	Output delay to 0				500	ns
t_{HZ}	Output delay to Hi-Z				100	ns
t_{EW}	Erase/Write pulse width				10	ms
t_{CSMIN}	Minimum CS low time		250			ns
t_{SKHI}	Minimum SK high time		250			ns
t_{SKLOW}	Minimum SK low time		250			ns
t_{SV}	Output delay to status valid	C_L = 100pF			500	ns
SK_{MAX}	Maximum clock frequency		DC		1	MHz

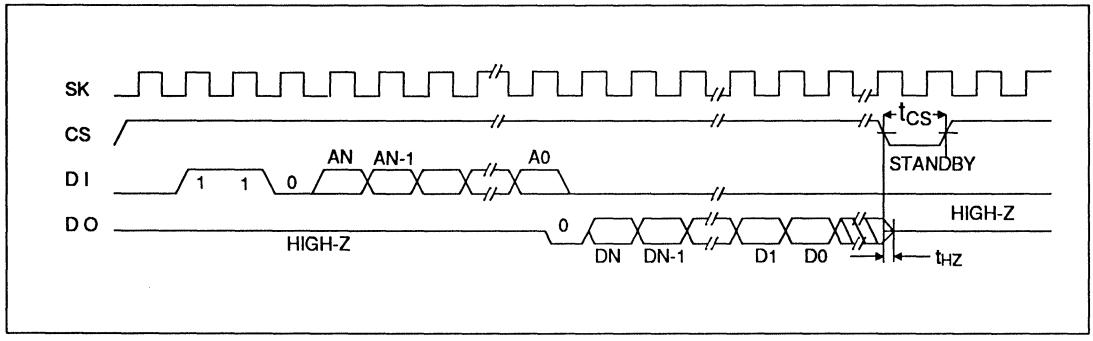
SYNCHRONOUS TIMINGS



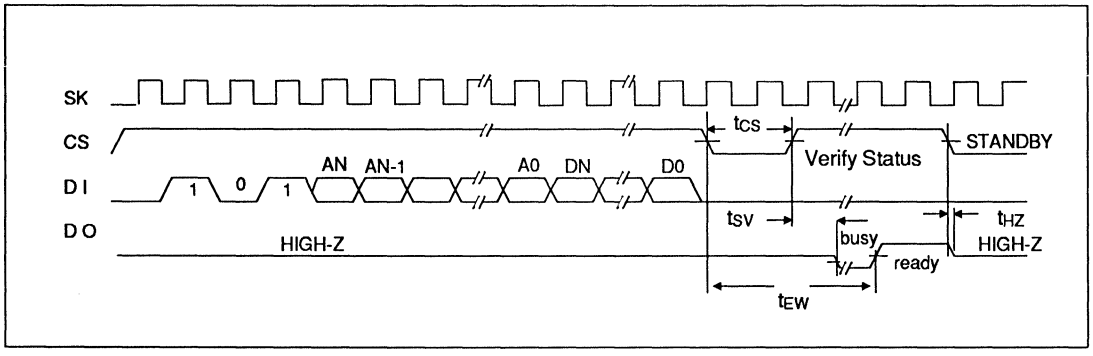
INSTRUCTION TIMING <ORGANIZATION>

Organization	A_N (or AN)	D_N (or DN)
256 x 8	A_7	D_7
128 x 16	A_6	D_{15}

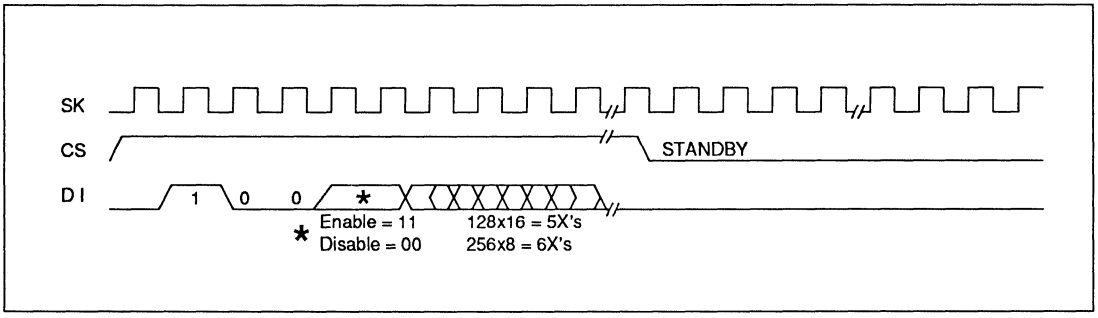
INSTRUCTION TIMING <READ>



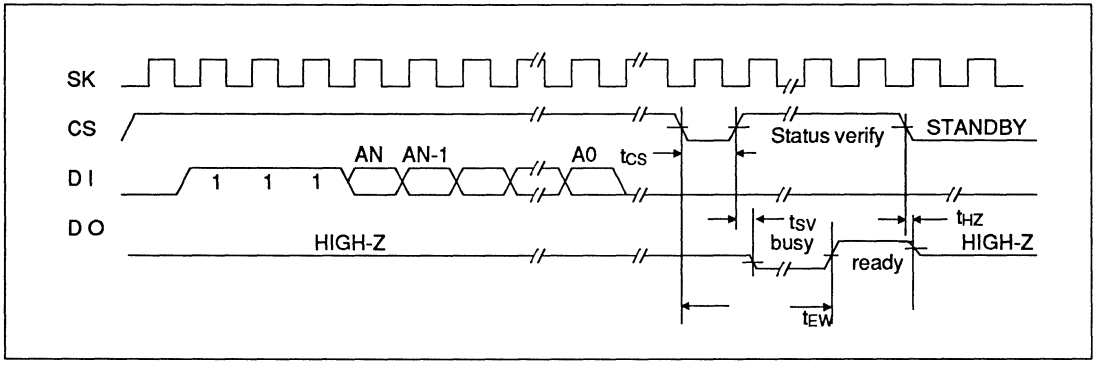
INSTRUCTION TIMING <WRITE>



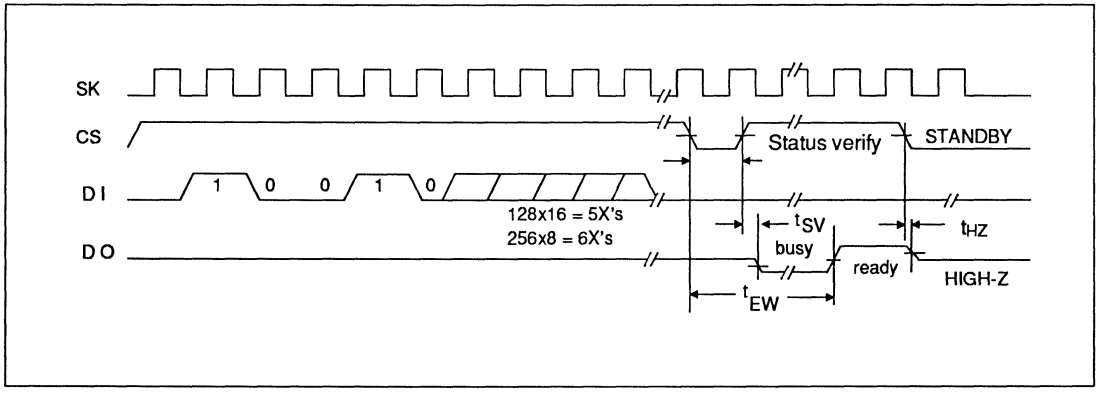
INSTRUCTION TIMING <EWEN, EWDS>



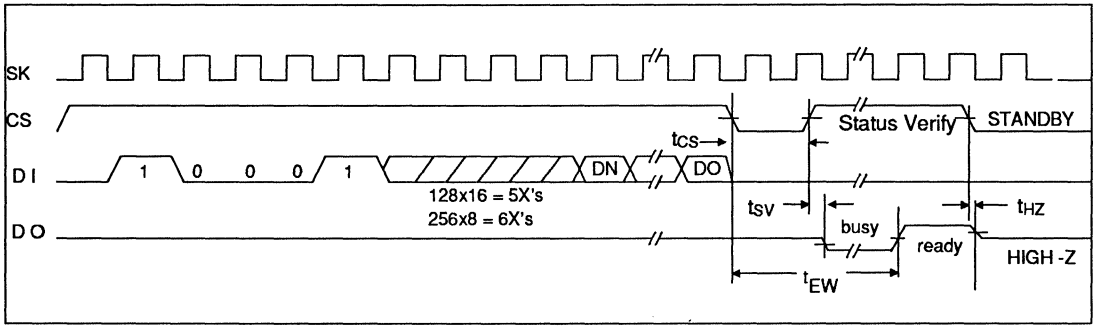
INSTRUCTION TIMING <ERASE>



INSTRUCTION TIMING <ERAL>



INSTRUCTION TIMING <WRAL>



DEVICE OPERATION

The CAT35C102I is a high endurance CMOS 2048-bit nonvolatile memory intended for use with the COPS™ family of microcontrollers, or other standard microprocessors. The CAT35C102I can be organized as either 128 registers by 16 bits, or as 256 registers by 8 bits. Seven 10-bit instructions (11 bit instructions in 256 by 8 organization) control the reading, writing and erase operations of the device. The CAT35C102I operates on a single 5V supply and will generate on chip, the high voltage required during any programming operation. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a programming operation. The ready/busy status can be determined after a programming operation by selecting the device and polling the DO pin; DO low indicates that the programming operation is not completed, while DO high indicates that the device is ready. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and and the DO pin are to be tied together to form a common DI/O pin. The format for all instructions sent to the CAT35C102I is a logical "1" start bit, a 2 bit (or 4 bit) op code, a 7 bit address (8 bit address when organized as 256 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 256 X 8).

READ

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT35C102I will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed. The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay t_{PD0} or t_{PD1}.

ERASE/WRITE ENABLE AND DISABLE

The CAT35C102I powers up in the programming disable state. Any programming after power-up or after an EWDS (programming disable) instruction must first be preceded by the EWEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT35C102I programming and erasing functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT35C102I regardless of the programming enable/disable status.

ERASE

Upon receiving an ERASE command and address, the CS (chip select) must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C102I can be determined by selecting the device and polling the DO pin. Once

erased, the contents of an erased location returns to a logical "1" state.

WRITE

After receiving a WRITE command, address and the data, the CS (chip select) must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C102I can be determined by selecting the device and polling the DO pin. With the CAT35C102I it is **NOT** necessary to erase a memory location before the WRITE command.

ERASE ALL

Upon receiving an ERAL command, the CS (chip select) must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C102I can be determined by selecting the device and polling the DO pin. Once erased, all memory bits return to a logical "1" state.

WRITE ALL

Upon receiving a WRAL command and data, the CS (chip select) must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C102I can be determined by selecting the device and polling the DO pin. It **IS** necessary for all memory locations to be erased before the WRAL command is executed.

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CAT35C104
4K BIT SERIAL E²PROM

1MHz OPERATION

DESCRIPTION

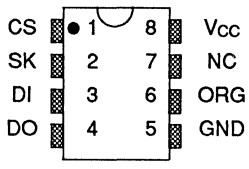
The CAT35C104 is a 4K bit serial E²PROM memory device organized in 256 registers of 16 bits (ORG pin at Vcc) or 512 registers of 8 bits each (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT35C104 is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 10,000 erase/write cycles and has a data retention of 10 years. It is packaged in an 8-pin DIP or S.O. package. This device will be offered in a G.I. compatible protocol version, the CAT35C204 and in commercial versions which will provide 3V operation (CAT33C104).

FEATURES

- Highly reliable CMOS floating gate technology
- Single 5V supply
- Available in 8 pin DIP or S.O. package
- 256x16 or 512x8 user selectable serial memory
- Microwire™ compatible
- Self timed programming cycle with Autoerase
- Operating range 0°C to +70°C [Industrial temp. range available]
- 10,000 erase/write cycles
- 10 year data retention
- Power-up inadvertent write protection

PIN CONFIGURATION

TOP VIEW

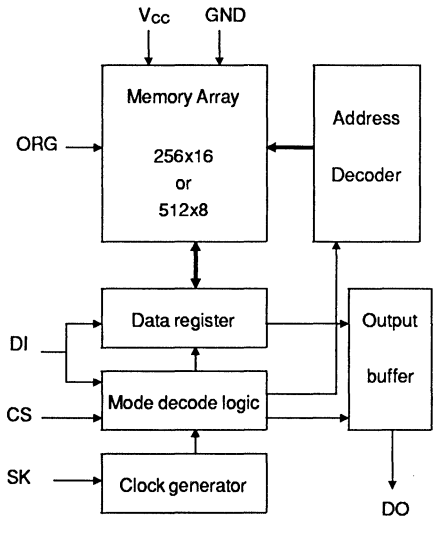


PIN FUNCTIONS

CS	Chip select
SK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
GND	Ground
NC	No connection
ORG	Memory organization

Note: When the ORG pin is connected to Vcc, the 256x16 organization is selected. When it is connected to ground, the 512x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 256x16 organization.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature . . . . . -65°C to +150°C
Power supply (V_{CC}) . . . . . +7V
Voltage on any input pin . . . . . -0.3 to +7V
Voltage on any output pin . . . . . -0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC1}	Current consumption (operating)	DI=0.0V, SK=5.0V V_{CC} =5.0V, CS =5.0V Output unloaded			3	mA
I_{CC2}	Current consumption (standby)	V_{CC} = 5.5V, CS = 0 DI = 0, SK = 0			100	µA
I_{LI}	Input leakage current	V_{IN} = 5.5V			10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V, CS = 0			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V

INSTRUCTION SET

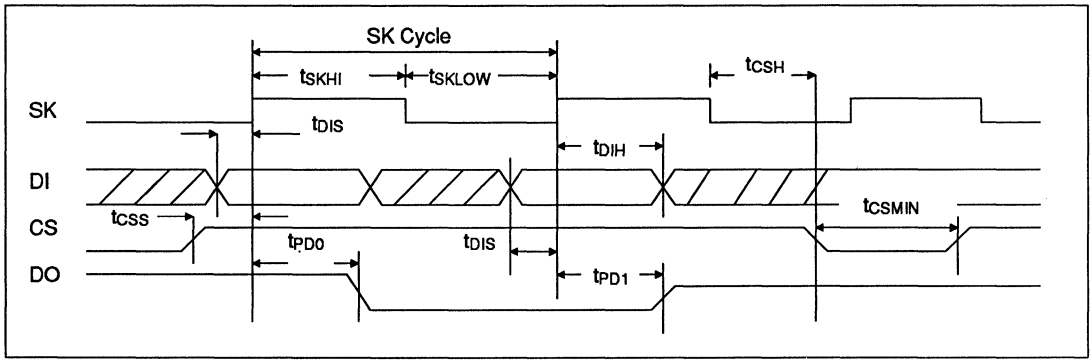
Instruction	Start Bit	Opcode	Address		Data		Comments
			512 x 8	256 x 16	512 x 8	256 x 16	
READ	1	1 0	A8 - A0	A7 - A0			Read address AN - A0
ERASE	1	1 1	A8 - A0	A7 - A0			Erase address AN - A0
WRITE	1	0 1	A8 - A0	A7 - A0	D7 - D0	D15 - D0	Write address AN - A0
EWEN	1	0 0	11XXXXXXX	11XXXXXX			Program enable
EWDS	1	0 0	00XXXXXXX	00XXXXXX			Program disable
ERAL	1	0 0	10XXXXXXX	10XXXXXX			Erase all addresses
WRAL	1	0 0	01XXXXXXX	01XXXXXX	D7 - D0	D15 - D0	Program all addresses

AC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{CSS}	CS setup time		50			ns
t_{CSH}	CS hold time	C_L = 100pF V_{OL} = 0.8V, V_{OH} = 2.0V V_{IL} = 0.45V, V_{IH} = 2.4V	0			ns
t_{DIS}	DI setup time		100			ns
t_{DIH}	DI hold time		100			ns
t_{PD1}	Output delay to 1				500	ns
t_{PD0}	Output delay to 0				500	ns
t_{HZ}	Output delay to High-Z				100	ns
t_{EW}	Erase/Write pulse width				10	ms
t_{CSMIN}	Minimum CS low time		250			ns
t_{SKHI}	Minimum SK high time		250			ns
t_{SKLOW}	Minimum SK low time		250			ns
t_{SV}	Output delay to status valid	C_L = 100pF			500	ns
SK_{MAX}	Maximum clock frequency		DC		1	MHz

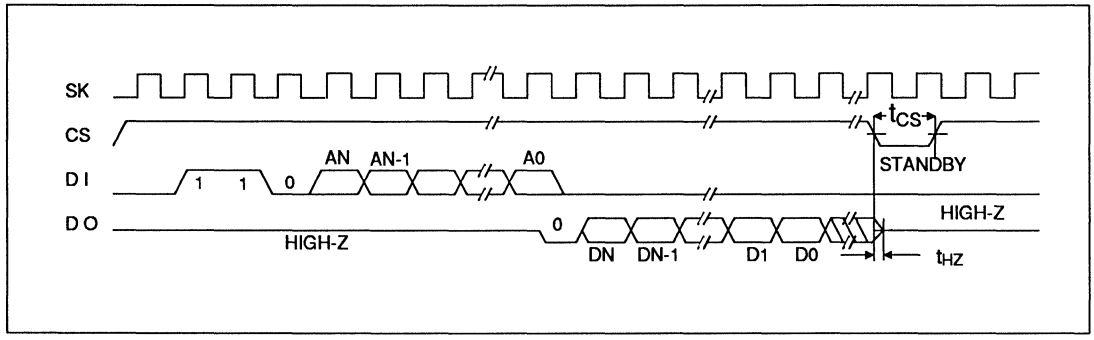
SYNCHRONOUS TIMINGS



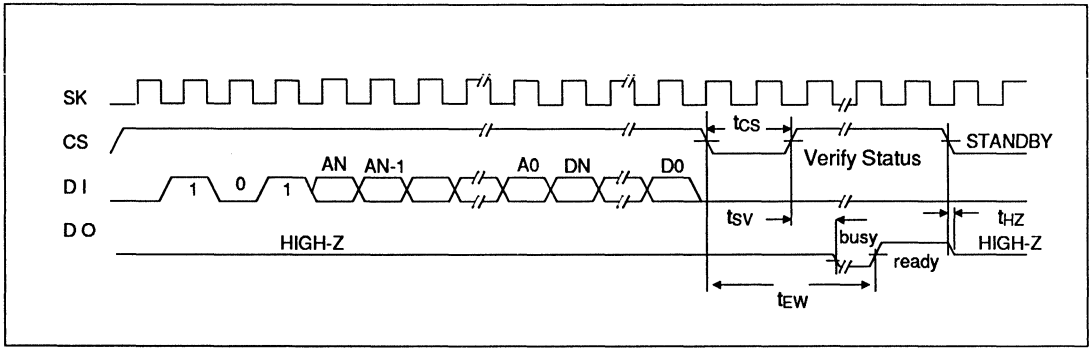
INSTRUCTION TIMING <ORGANIZATION>

Organization	A_N (or AN)	D_N (or DN)
512 x 8	A_8	D_7
256 x 16	A_7	D_{15}

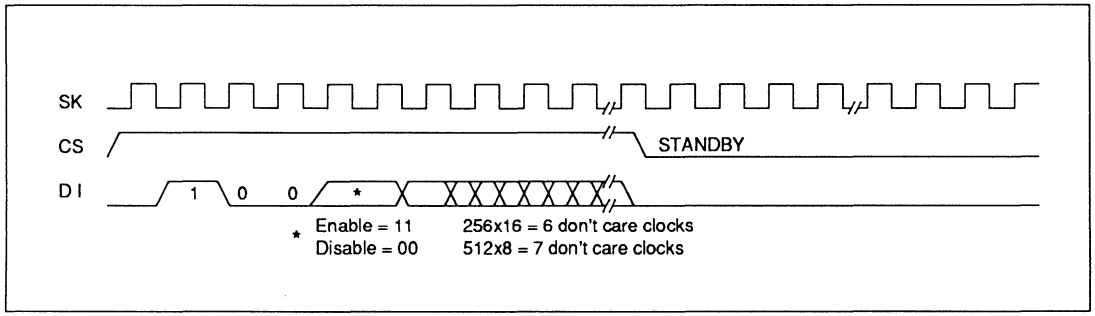
INSTRUCTION TIMING <READ>



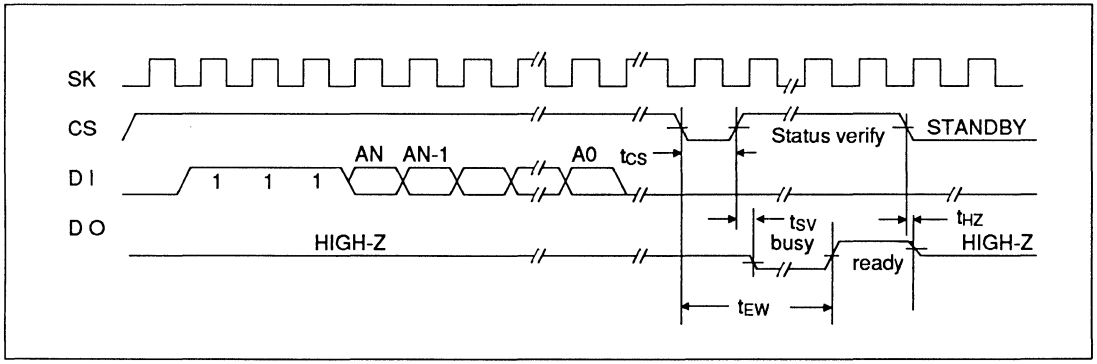
INSTRUCTION TIMING <WRITE>



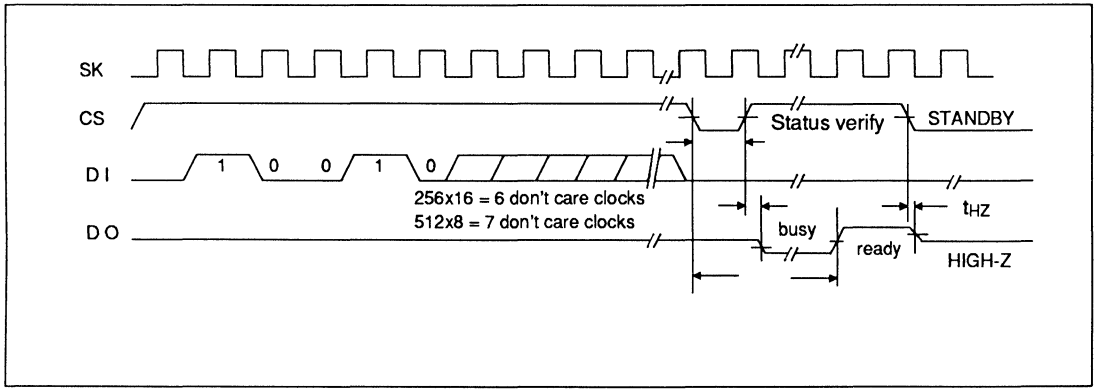
INSTRUCTION TIMING <EWEN, EWDS>



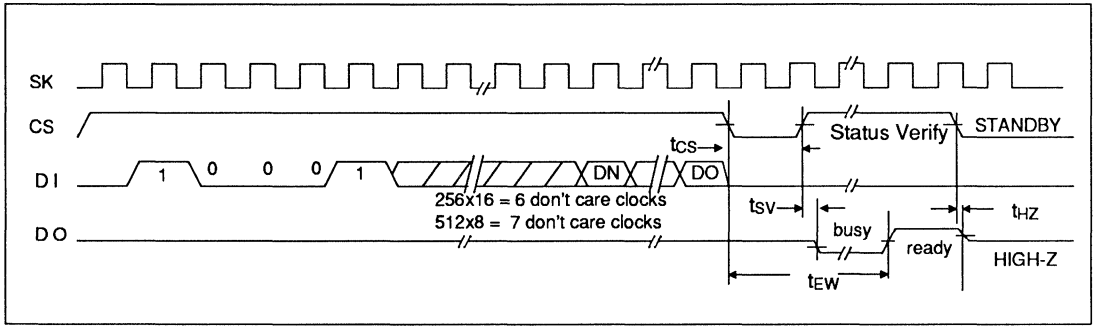
INSTRUCTION TIMING <ERASE>



INSTRUCTION TIMING <ERAL>



INSTRUCTION TIMING <WRAL>



DEVICE OPERATION

The CAT35C104 is a 4096 bit nonvolatile memory intended for use with the COPS™ family of microcontrollers, or other standard microprocessors such as the 80C48 or 80C51. The CAT35C104 can be organized as either 256 registers by 16 bits, or as 512 registers by 8 bits. Seven 11-bit instructions (12-bit instructions in 512 by 8 organization) control the reading, writing and erase operations of the device. The CAT35C104 operates on a single 5V supply and will generate on chip the high voltage required during any programming operation. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a programming operation. The ready/busy status can be determined after a programming operation by selecting the device and polling the DO pin; DO low indicates that the programming operation is not completed, while DO high indicates that the device is ready. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin. The format for all instructions sent to the CAT35C104 is a logical "1" start bit, a 2 bit (or 4 bit) op code, a 8 bit address (9 bit address when organized as 512 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 512 X 8).

At power-down, when V_{CC} falls below a threshold of approximately 3V, the data protection circuitry inhibits write mode operations and a programming disable (EWDS) is executed internally.

READ

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT35C104 will come out of the high impedance state, and after sending an initial dummy zero bit, will begin shifting out the data addressed. The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

ERASE/WRITE ENABLE AND DISABLE

The CAT35C104 powers up in the programming disable state. Any programming after power-up or after an EWDS (programming disable) instruction must first be preceded by the EWEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT35C104 programming and erasing functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT35C104 regardless of the programming enable/disable status.

ERASE

Upon receiving an ERASE command and address, the CS (chip select) must be deselected for a minimum of 1μs (T_{CSMIN}). The falling edge of CS will

start the self clocking erase cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C104 can be determined by selecting the device and polling the DO pin. Once erased, the contents of an erased location returns to logical "1" state.

WRITE

After receiving a WRITE command, address and the data, the CS (chip select) must be deselected for a minimum of 1μs (T_{CSMIN}). The falling edge of CS will start the self clocking erase and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C104 can be determined by selecting the device and polling the DO pin. With the CAT35C104 it is **NOT** necessary to erase a memory location before the WRITE command.

ERASE ALL

Upon receiving an ERAL command, the CS (chip select) must be deselected for a minimum of 1μs (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C104 can be determined by selecting the device and polling the DO pin. Once erased, all memory bits return to logical "1" state.

WRITE ALL

Upon receiving a WRAL command and data, the CS (chip select) must be deselected for a minimum of 1μs (T_{CSMIN}). The falling edge of CS will start the self clocking write cycle on all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C104 can be determined by selecting the device and polling the DO pin.

It **IS NOT** necessary for all memory locations to be erased before the WRAL command is executed.

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CAT35C104H - High Endurance 4K BIT SERIAL E^2PROM

1MHz OPERATION

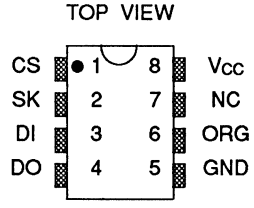
DESCRIPTION

The CAT35C104H is a high endurance 4K bit serial E^2PROM memory device organized in 256 registers of 16 bits (ORG pin at V_{CC}) or 512 registers of 8 bits each (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT35C104H is manufactured using Catalyst's advanced CMOS E^2PROM floating gate technology. It is designed to endure 100,000 erase/write cycles and has a data retention of 100 years. It is packaged in an 8-pin DIP or S.O. package. This device will be offered in a G.I. compatible protocol version, the CAT35C204H and in commercial versions which will provide 3V operation (CAT33C104H).

FEATURES

- Highly reliable CMOS floating gate technology
- Single 5V supply
- Available in 8 pin DIP or S.O. package
- 256x16 or 512x8 user selectable serial memory
- Microwire™ compatible
- Self timed programming cycle with Autoerase
- Operating range 0°C to +70°C
- 100,000 erase/write cycles
- 100 year data retention
- Power-up inadvertent write protection

PIN CONFIGURATION

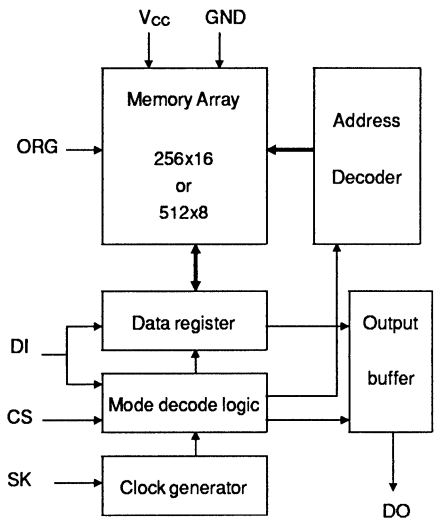


PIN FUNCTIONS

CS	Chip select
SK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
GND	Ground
NC	No connection
ORG	Memory organization

Note: When the ORG pin is connected to V_{CC}, the 256x16 organization is selected. When it is connected to ground, the 512x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 256x16 organization.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature . . . . . -65°C to +150°C
Power supply (V_{CC}) . . . . . +7V
Voltage on any input pin . . . . . -0.3 to +7V
Voltage on any output pin . . . . . -0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC1}	Current consumption (operating)	DI=0.0V, SK=5.0V V_{CC} =5.0V, CS =V_{IH} Output unloaded			3	mA
I_{CC2}	Current consumption (standby)	V_{CC} = 5.5V, CS = 0 DI = 0, SK = 0			100	µA
I_{LI}	Input leakage current	V_{IN} = 5.5V			10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V, CS = 0			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V

INSTRUCTION SET

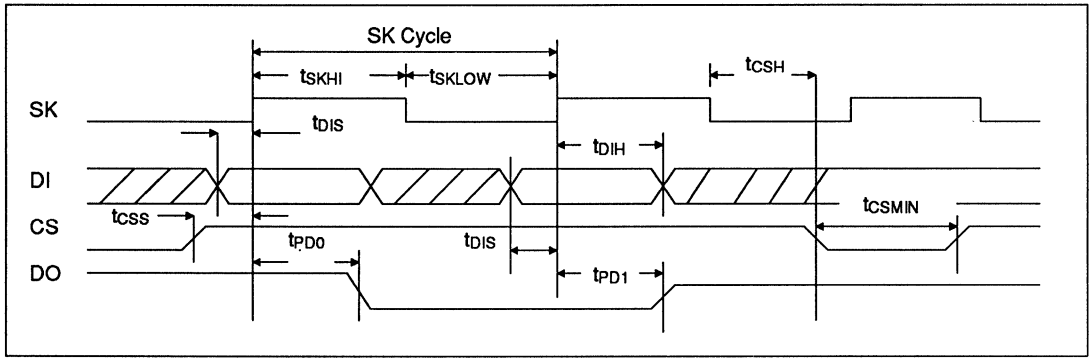
Instruction	Start Bit	Opcode	Address		Data		Comments
			512 x 8	256 x 16	512 x 8	256 x 16	
READ	1	1 0	A8 - A0	A7 - A0			Read address AN - A0
ERASE	1	1 1	A8 - A0	A7 - A0			Erase address AN - A0
WRITE	1	0 1	A8 - A0	A7 - A0	D7 - D0	D15 - D0	Write address AN - A0
EWEN	1	0 0	11XXXXXXX	11XXXXXX			Program enable
EWDS	1	0 0	00XXXXXXX	00XXXXXX			Program disable
ERAL	1	0 0	10XXXXXXX	10XXXXXX			Erase all addresses
WRAL	1	0 0	01XXXXXXX	01XXXXXX	D7 - D0	D15 - D0	Program all addresses

AC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{CSS}	CS setup time		50			ns
t_{CSH}	CS hold time	C_L = 100pF V_{OL} = 0.8V, V_{OH} = 2.0V V_{IL} = 0.45V, V_{IH} = 2.4V	0			ns
t_{DIS}	DI setup time		100			ns
t_{DIH}	DI hold time		100			ns
t_{PD1}	Output delay to 1				500	ns
t_{PD0}	Output delay to 0				500	ns
t_{HZ}	Output delay to High-Z				100	ns
t_{EW}	Erase/Write pulse width				10	ms
t_{CSMIN}	Minimum CS low time		250			ns
t_{SKHI}	Minimum SK high time		250			ns
t_{SKLOW}	Minimum SK low time		250			ns
t_{SV}	Output delay to status valid	C_L = 100pF			500	ns
SK_{MAX}	Maximum clock frequency		DC		1	MHz

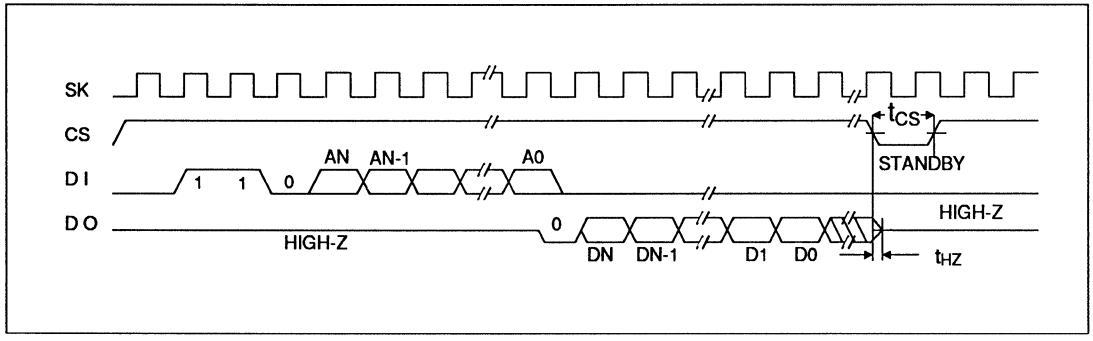
SYNCHRONOUS TIMINGS



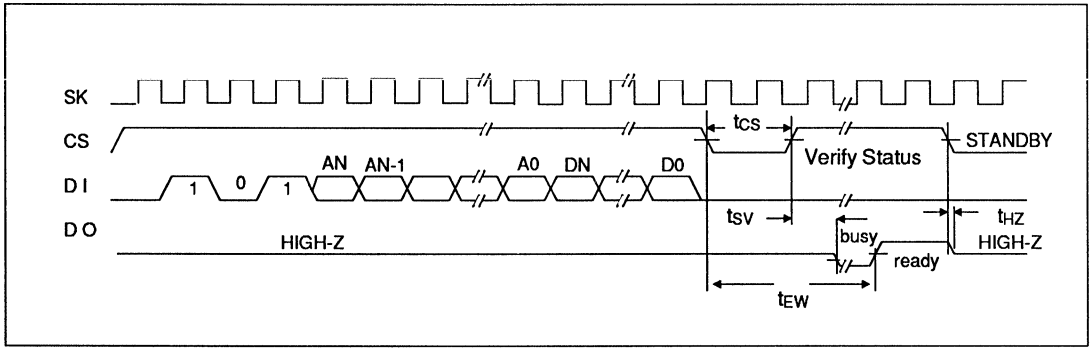
INSTRUCTION TIMING <ORGANIZATION>

Organization	A_N (or AN)	D_N (or DN)
512 x 8	A_8	D_7
256 x 16	A_7	D_{15}

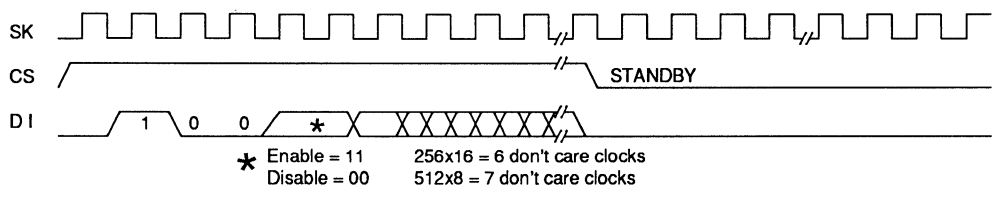
INSTRUCTION TIMING <READ>



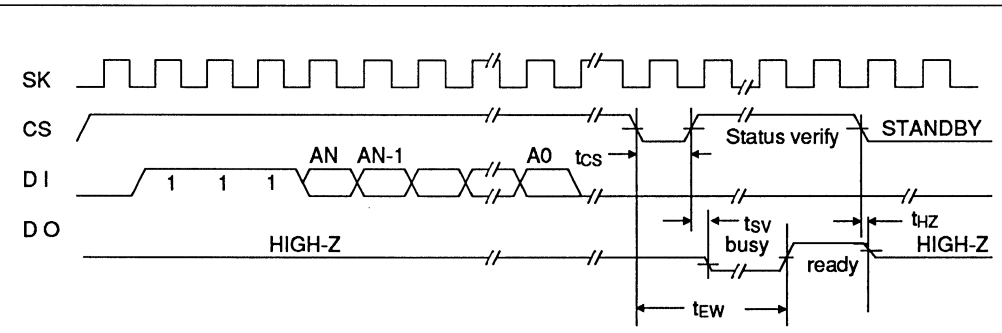
INSTRUCTION TIMING <WRITE>



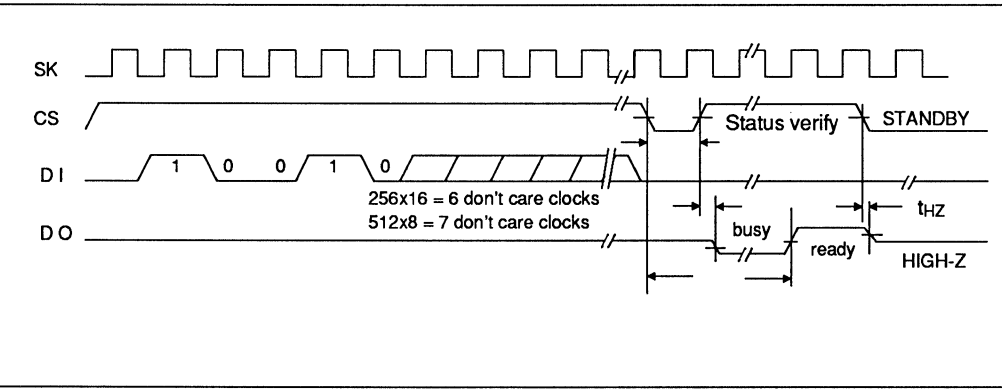
INSTRUCTION TIMING <EWEN, EWDS>



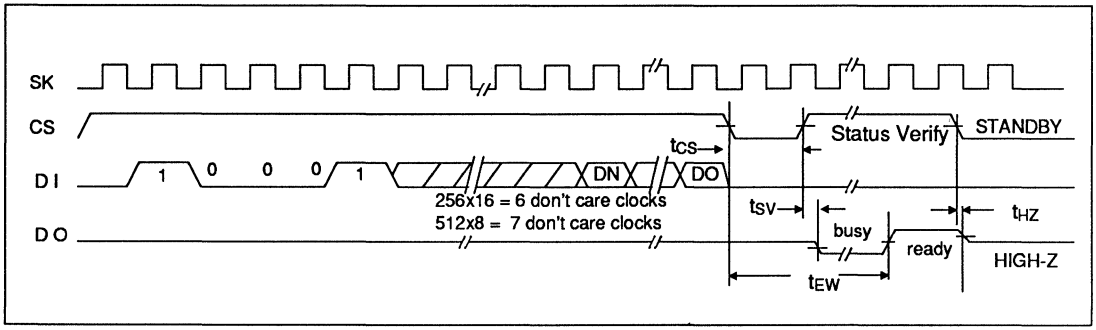
INSTRUCTION TIMING <ERASE>



INSTRUCTION TIMING <ERAL>



INSTRUCTION TIMING <WRAL>



DEVICE OPERATION

The CAT35C104H is a 4096 bit nonvolatile memory intended for use with the COPS™ family of microcontrollers, or other standard microprocessors such as the 80C48 or 80C51. The CAT35C104H can be organized as either 256 registers by 16 bits, or as 512 registers by 8 bits. Seven 11-bit instructions (12-bit instructions in 512 by 8 organization) control the reading, writing and erase operations of the device. The CAT35C104H operates on a single 5V supply and will generate on chip the high voltage required during any programming operation. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a programming operation. The ready/busy status can be determined after a programming operation by selecting the device and polling the DO pin; DO low indicates that the programming operation is not completed, while DO high indicates that the device is ready. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin. The format for all instructions sent to the CAT35C104H is a logical "1" start bit, a 2 bit (or 4 bit) op code, a 8 bit address (9 bit address when organized as 512 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 512 X 8).

At power-down, when V_{CC} falls below a threshold of approximately 3V, the data protection circuitry inhibits write mode operations and a programming disable (EWDS) is executed internally.

READ

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT35C104H will come out of the high impedance state, and after sending an initial dummy zero bit, will begin shifting out the data addressed. The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

ERASE/WRITE ENABLE AND DISABLE

The CAT35C104H powers up in the programming disable state. Any programming after power-up or after an EWDS (programming disable) instruction must first be preceded by the EWEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT35C104H programming and erasing functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT35C104H regardless of the programming enable/disable status.

ERASE

Upon receiving an ERASE command and address, the CS (chip select) must be deselected for a minimum of 1μs (T_{CSMIN}). The falling edge of CS will

start the self clocking erase cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C104H can be determined by selecting the device and polling the DO pin. Once erased, the contents of an erased location returns to logical "1" state.

WRITE

After receiving a WRITE command, address and the data, the CS (chip select) must be deselected for a minimum of 1μs (T_{CSMIN}). The falling edge of CS will start the self clocking erase and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C104H can be determined by selecting the device and polling the DO pin. With the CAT35C104H it is **NOT** necessary to erase a memory location before the WRITE command.

ERASE ALL

Upon receiving an ERAL command, the CS (chip select) must be deselected for a minimum of 1μs (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C104H can be determined by selecting the device and polling the DO pin. Once erased, all memory bits return to logical "1" state.

WRITE ALL

Upon receiving a WRAL command and data, the CS (chip select) must be deselected for a minimum of 1μs (T_{CSMIN}). The falling edge of CS will start the self clocking write cycle on all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C104H can be determined by selecting the device and polling the DO pin.

It **IS NOT** necessary for all memory locations to be erased before the WRAL command is executed.

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CAT35C104I - Industrial Temperature 1MHz 4K BIT SERIAL E^2PROM OPERATION

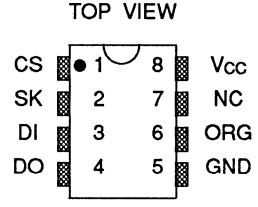
DESCRIPTION

The CAT35C104I is an industrial temperature 4K bit Serial E^2PROM memory device organized in 256 registers of 16 bits (ORG pin at V_{CC}) or 512 registers of 8 bits each (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT35C104I is manufactured using Catalyst's advanced CMOS E^2PROM floating gate technology. It is designed to endure 10,000 erase/write cycles and has a data retention of 10 years. It is packaged in an 8-pin DIP or S.O. package. This device will be offered in a G.I. compatible protocol version, the CAT35C204 and in commercial versions which will provide 3V operation (CAT33C104) and/or high-endurance (100,000 write cycle) performance.

FEATURES

- Highly reliable CMOS floating gate technology
- Single 5V supply
- Available in 8 pin DIP or S.O. package
- 256x16 or 512x8 user selectable serial memory
- Microwire™ compatible
- Self timed programming cycle with Autoerase
- Operating range -40°C to +85°C
- 10,000 erase/write cycles
- 10 year data retention
- Power-up inadvertent write protection

PIN CONFIGURATION

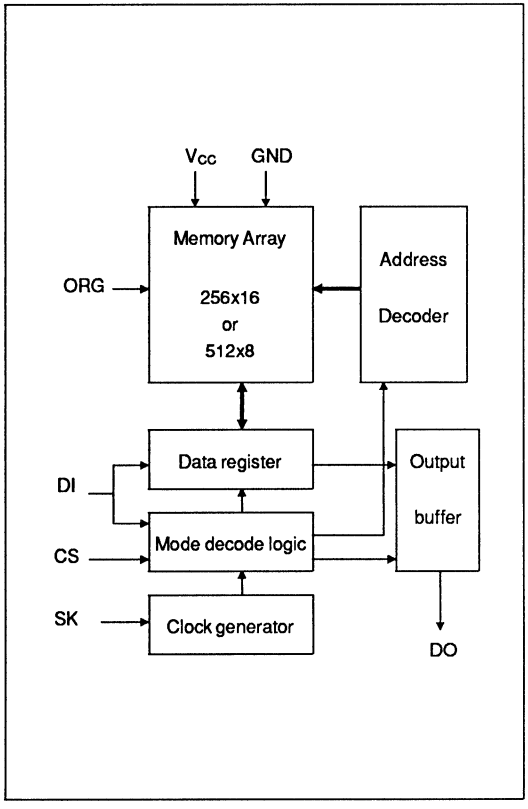


PIN FUNCTIONS

CS	Chip select
SK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
GND	Ground
NC	No connection
ORG	Memory organization

Note: When the ORG pin is connected to V_{CC}, the 256x16 organization is selected. When it is connected to ground, the 512x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 256x16 organization.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature . . . . . -65°C to +150°C
Power supply (V_{CC}) . . . . . +7V
Voltage on any input pin . . . . . -0.3 to +7V
Voltage on any output pin . . . . . -0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC1}	Current consumption (operating)	DI=0.0V, SK=5.0V V_{CC} =5.0V, CS =5.0V Output unloaded			4	mA
I_{CC2}	Current consumption (stand-by)	V_{CC} = 5.5V, CS = 0 DI = 0, SK = 0			100	µA
I_{LI}	Input leakage current	V_{IN} = 5.5V			10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V, CS = 0			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V

INSTRUCTION SET

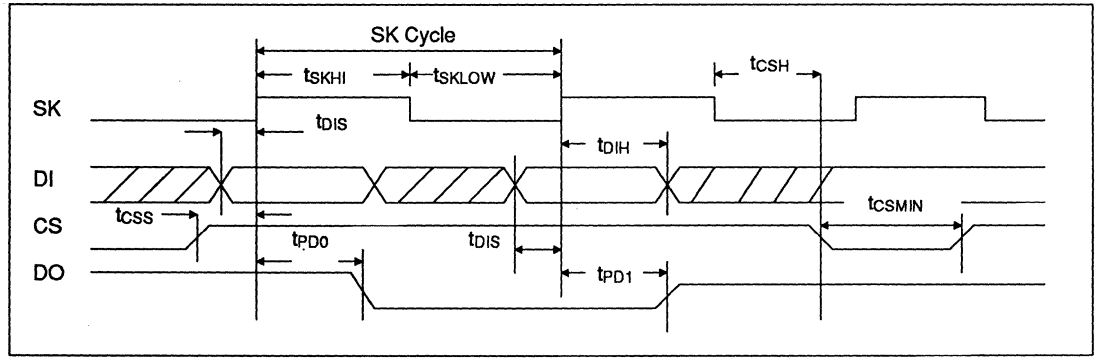
Instruction	Start Bit	Opcode	Address		Data		Comments
			512 x 8	256 x 16	512 x 8	256 x 16	
READ	1	1 0	A8 - A0	A7 - A0			Read address AN - A0
ERASE	1	1 1	A8 - A0	A7 - A0			Erase address AN - A0
WRITE	1	0 1	A8 - A0	A7 - A0	D7 - D0	D15 - D0	Write address AN - A0
EWEN	1	0 0	11XXXXXXX	11XXXXXX			Program enable
EWDS	1	0 0	00XXXXXXX	00XXXXXX			Program disable
ERAL	1	0 0	10XXXXXXX	10XXXXXX			Erase all addresses
WRAL	1	0 0	01XXXXXXX	01XXXXXX	D7 - D0	D15 - D0	Program all addresses

AC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{CSS}	CS setup time		50			ns
t_{CSH}	CS hold time	C_L = 100pF V_{OL} = 0.8V, V_{OH} = 2.0V V_{IL} = 0.45V, V_{IH} = 2.4V	0			ns
t_{DIS}	DI setup time		100			ns
t_{DIH}	DI hold time		100			ns
t_{PD1}	Output delay to 1				500	ns
t_{PD0}	Output delay to 0				500	ns
t_{HZ}	Output delay to High-Z				100	ns
t_{EW}	Erase/Write pulse width				10	ms
t_{CSMIN}	Minimum CS low time		250			ns
t_{SKHI}	Minimum SK high time		250			ns
t_{SKLOW}	Minimum SK low time		250			ns
t_{SV}	Output delay to status valid	C_L = 100pF			500	ns
SK_{MAX}	Maximum clock frequency		DC		1	MHz

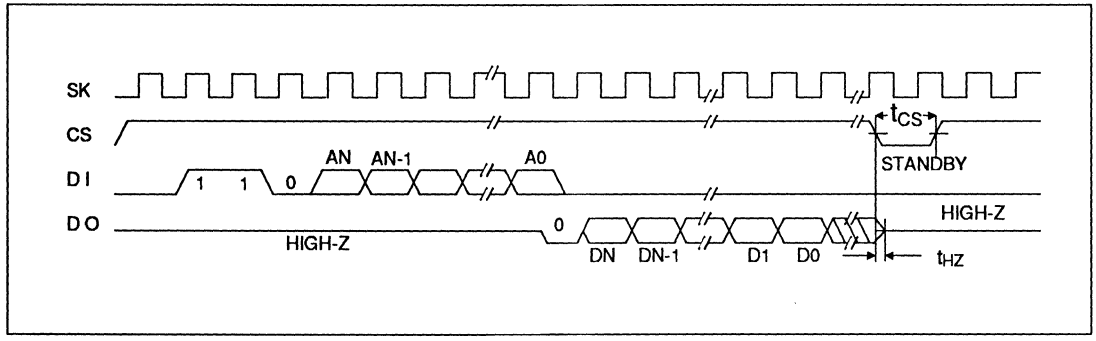
SYNCHRONOUS TIMINGS



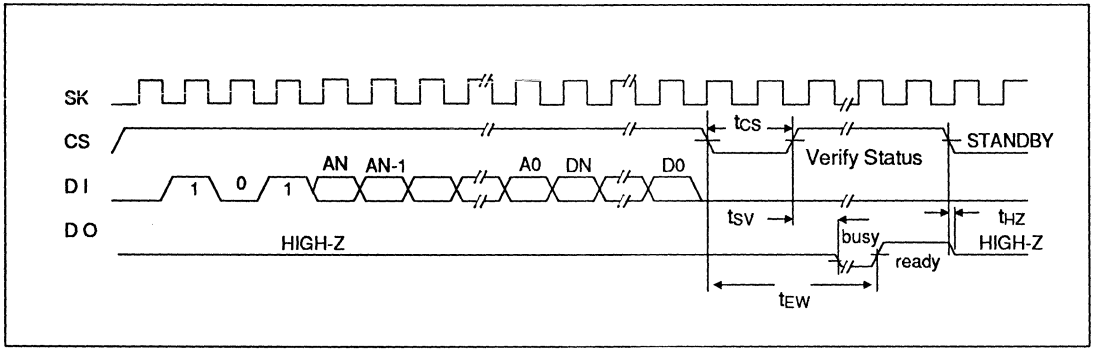
INSTRUCTION TIMING <ORGANIZATION>

Organization	A_N (or AN)	D_N (or DN)
512 x 8	A_8	D_7
256 x 16	A_7	D_{15}

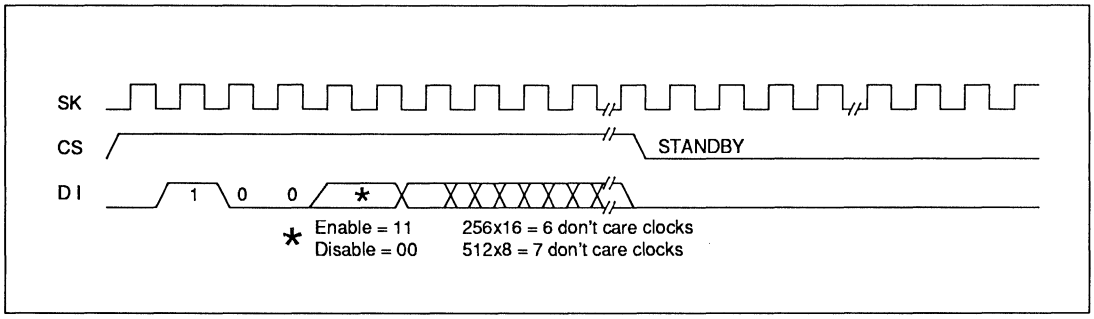
INSTRUCTION TIMING <READ>



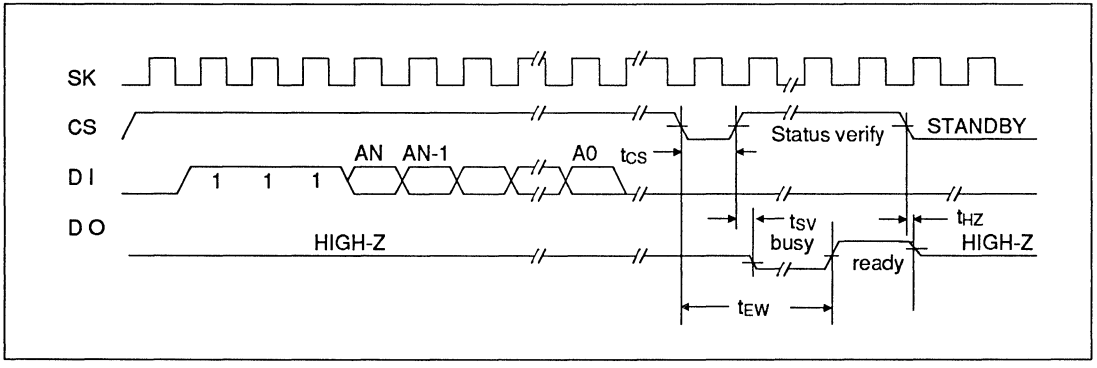
INSTRUCTION TIMING <WRITE>



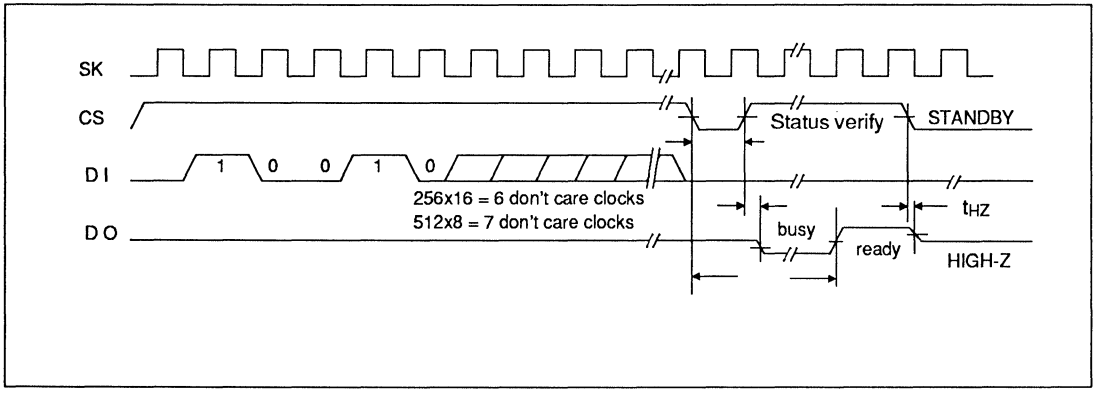
INSTRUCTION TIMING <EWEN, EWDS>



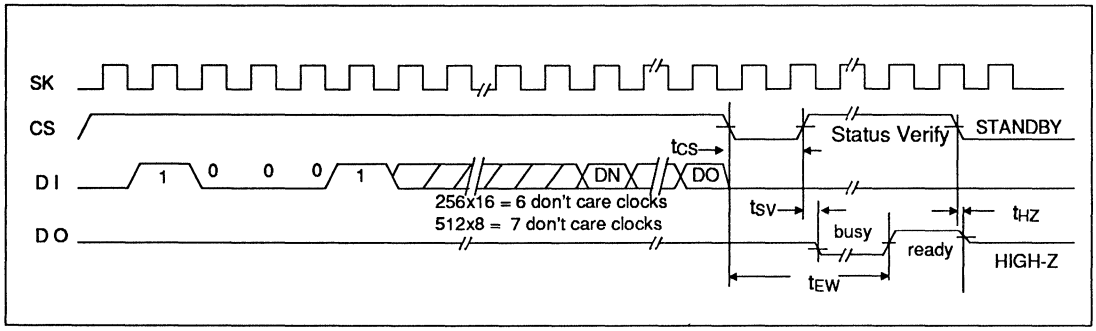
INSTRUCTION TIMING <ERASE>



INSTRUCTION TIMING <ERAL>



INSTRUCTION TIMING <WRAL>



DEVICE OPERATION

The CAT35C104I is a 4096 bit nonvolatile memory intended for use with the COPS™ family of microcontrollers as well as other standard microprocessors such as the 80C48, or 80C51. The CAT35C104I can be organized as either 256 registers by 16 bits, or as 512 registers by 8 bits. Seven 11-bit instructions (12-bit instructions in 512 by 8 organization) control the reading, writing, and erase operations of the device. The CAT35C104I operates on a single 5V supply and will generate on chip the high voltage required during any programming operation. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a programming operation. The ready/busy status can be determined after a programming operation by selecting the device and polling the DO pin; DO low indicates that the programming operation is not completed, while DO high indicates that the device is ready. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and and the DO pin are to be tied together to form a common DI/O pin. The format for all instructions sent to the CAT35C104I is a logical "1" start bit, a 2 bit (or 4 bit) op code, a 8 bit address (9 bit address when organized as 512 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 512 X 8).

At power-down, when V_{CC} falls below a threshold of approximately 3 volts, the data protection circuitry inhibits write mode operations and a programming disable (EWDS) is executed internally.

READ

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT35C104I will come out of the high impedance state, and after sending an initial dummy zero bit, will begin shifting out the data addressed. The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

ERASE/WRITE ENABLE AND DISABLE

The CAT35C104I powers up in the programming disable state. Any programming after power-up or after an EWDS (programming disable) instruction must first be preceded by the EWEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT35C104I programming and erasing functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT35C104I regardless of the programming enable/disable status.

ERASE

Upon receiving an ERASE command and address, the CS (chip select) must be deselected for a min-

imum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C104I can be determined by selecting the device and polling the DO pin. Once erased, the contents of an erased location returns to logical "1" state.

WRITE

After receiving a WRITE command, address and the data, the CS (chip select) must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C104I can be determined by selecting the device and polling the DO pin. With the CAT35C104I it is **NOT** necessary to erase a memory location before the WRITE command.

ERASE ALL

Upon receiving an ERAL command, the CS (chip select) must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C104I can be determined by selecting the device and polling the DO pin. Once erased, all memory bits return to logical "1" state.

WRITE ALL

Upon receiving a WRAL command and data, the CS (chip select) must be deselected for a minimum of 1μs (T_{CSMIN}). The falling edge of CS will start the self clocking write cycle on all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C104I can be determined by selecting the device and polling the DO pin.

It **IS NOT** necessary for all memory locations to be erased before the WRAL command is executed.

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CAT35C202
2K BIT SERIAL E^2PROM

1MHz OPERATION

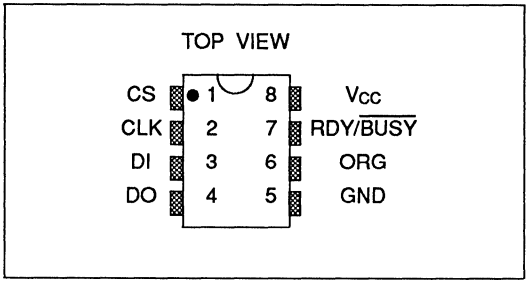
DESCRIPTION

The CAT35C202 is a CMOS 2K bit Serial E^2PROM memory device organized in 128 registers of 16 bits (ORG pin at V_{CC}) or 256 registers of 8 bits each (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT35C202 is manufactured using Catalyst's advanced CMOS E^2PROM floating gate technology. It is designed to endure 10,000 erase/write cycles and has a data retention of 10 years. Packaged in an 8-pin DIP and Small Outline packages. To be offered in a 3V version (CAT33C202).

FEATURES

- Highly reliable CMOS floating gate technology
- 10ms programming cycle
- Single 5V supply
- 128x16 or 256x8 user selectable serial memory
- Compatible with General Instruments ER5912
- Self timed programming cycle with Autoerase
- Word and chip erasable
- Operating range 0°C to 70°C [Industrial temp. range available]
- 10,000 erase/write cycles
- 10 year data retention
- Power-up inadvertent write protection

PIN CONFIGURATION

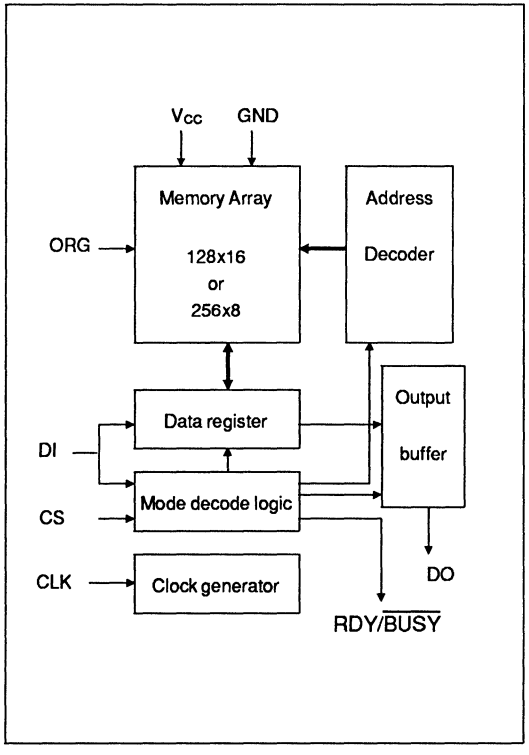


PIN FUNCTIONS

CS	Chip select
CLK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
RDY/BUSY	Status output
GND	Ground
ORG	Memory organization

Note: When the ORG pin is connected to V_{CC}, the 128x16 organization is selected. When it is connected to ground, the 256x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 128x16 organization.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature . . . . . -65°C to +150°C
Power supply (V_{CC}) . . . . . +7V
Voltage on any input pin . . . . . -0.3 to +7V
Voltage on any output pin . . . . . -0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC1}	Current consumption (operating)	DI=0.0V, SK=5.0V V_{CC} =5.0V, CS = 5.0V DO unloaded			3	mA
I_{CC2}	Current consumption (stand-by)	V_{CC} = 5.5V, CS = 0 DI = 0, SK = 0			100	µA
I_{LI}	Input leakage current	V_{IN} = 5.5V			10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V, CS = 0			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V

INSTRUCTION SET

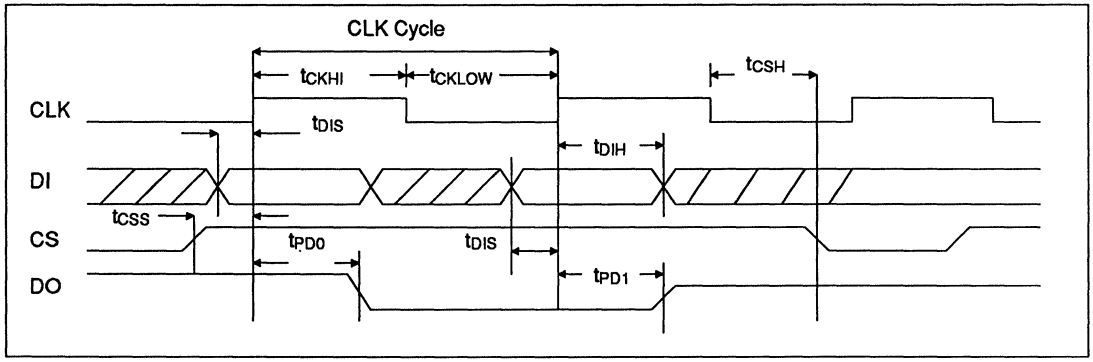
Instruction	Start Bit	Opcode	Address		Data		Comments
			256 x 8	128 x 16	256 x 8	128 x 16	
READ	1	1000	A7 - A0	A6 - A0			Read address AN - A0
PROGRAM	1	X100	A7 - A0	A6 - A0	D7 - D0	D15 - D0	Program address AN - A0
PEN	1	0011	00000000	0000000			Program enable
PDS	1	0000	00000000	0000000			Program disable
ERAL	1	0010	00000000	0000000			Erase all addresses
WRAL	1	0001	00000000	0000000	D7 - D0	D15 - D0	Write all addresses

AC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{CSS}	CS setup time		50			ns
t_{CSH}	CS hold time	C_L = 100pF V_{OL} = 0.8V, V_{OH} = 2.0V V_{IL} = 0.45V, V_{IH} = 2.4V	100			ns
t_{DIS}	DI setup time		100			ns
t_{DIH}	DI hold time		100			ns
t_{PD1}	Output delay to 1				500	ns
t_{PD0}	Output delay to 0				500	ns
t_{EW}	Erase/Write pulse width				10	ms
t_{SKHI}	Minimum SK high time		250			ns
t_{SKLOW}	Minimum SK low time		250			ns
CK_{MAX}	Maximum clock frequency		DC		1	MHz

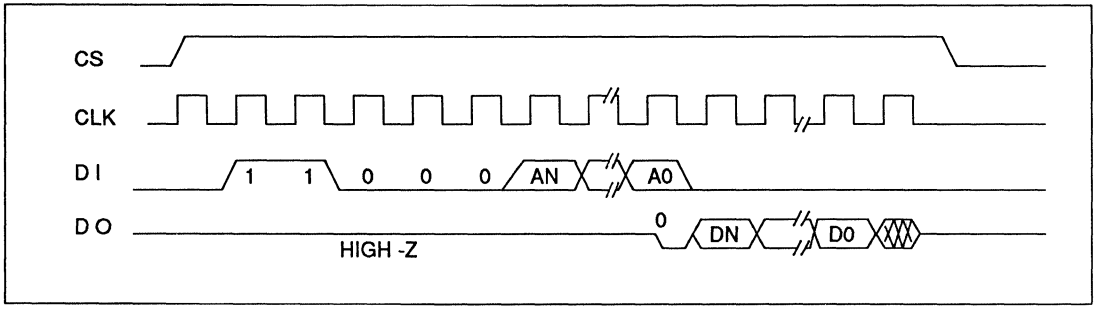
SYNCHRONOUS TIMINGS



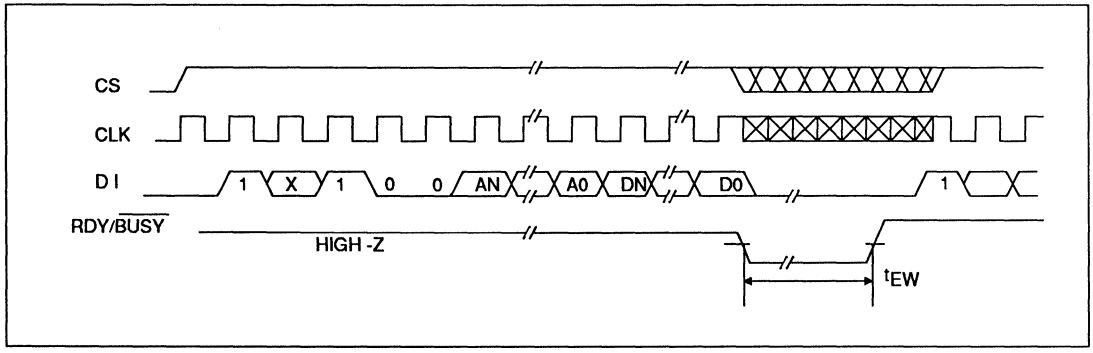
INSTRUCTION TIMING <ORGANIZATION>

Organization	A_N (or AN)	D_N (or DN)
256 x 8	A_7	D_7
128 x 16	A_6	D_{15}

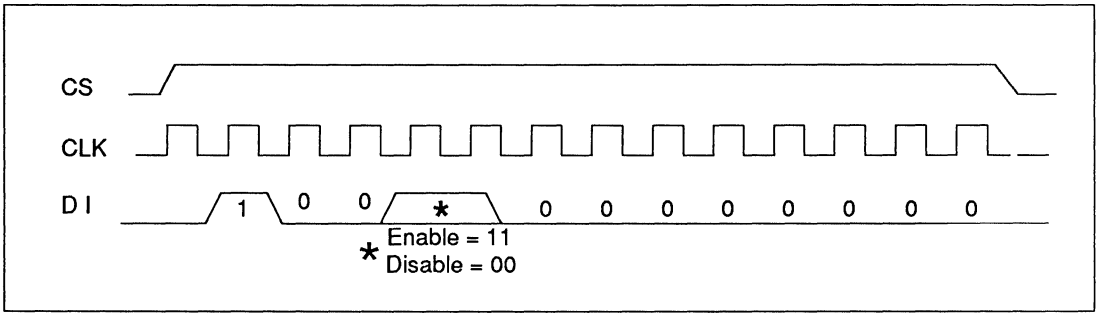
INSTRUCTION TIMING <READ>



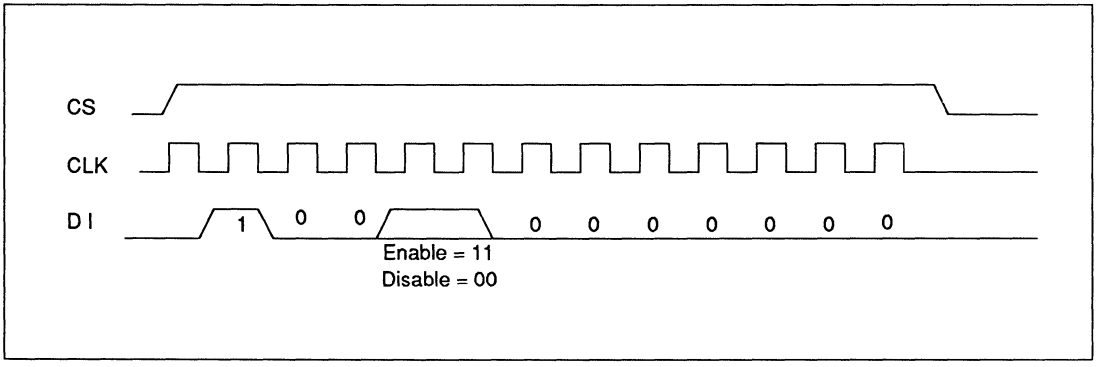
INSTRUCTION TIMING <PROGRAM>



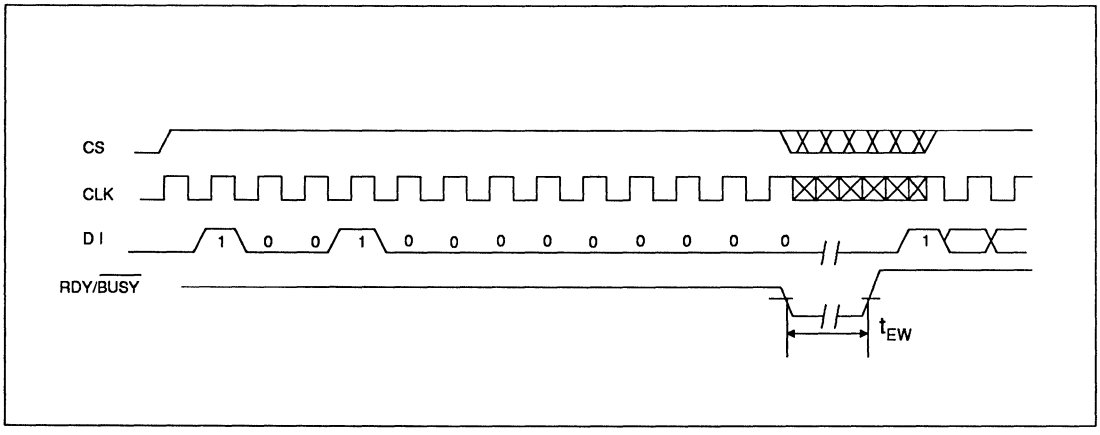
INSTRUCTION TIMING <PEN, PDS 256 x 8 organization>



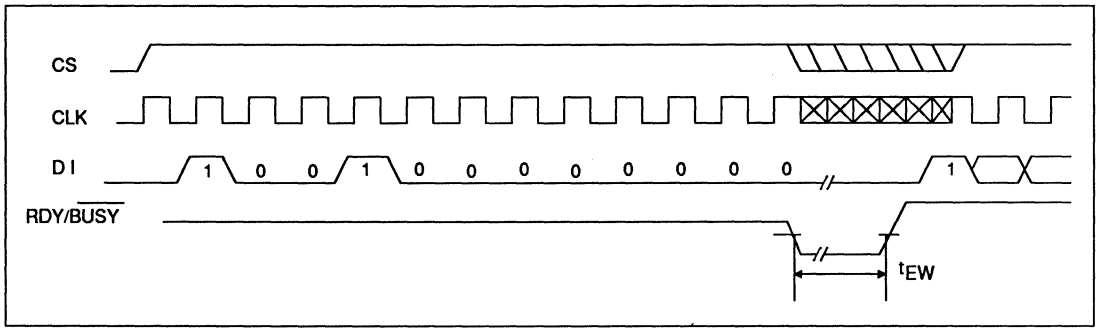
INSTRUCTION TIMING <PEN, PDS 128 x 16 organization>



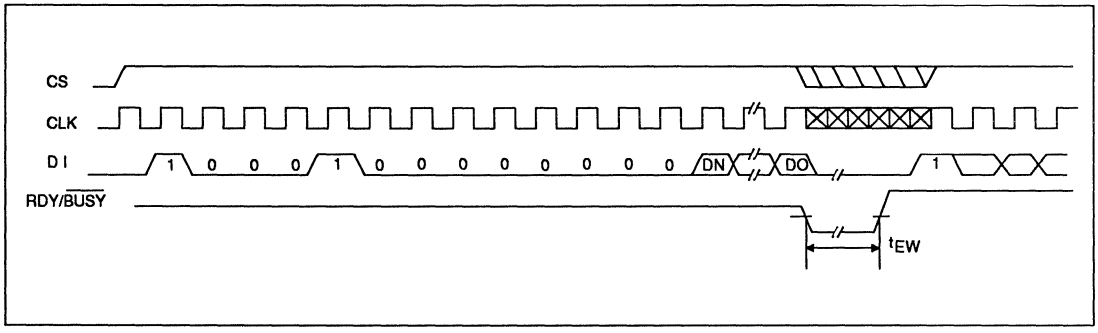
INSTRUCTION TIMING <ERAL 256 x 8 organization>



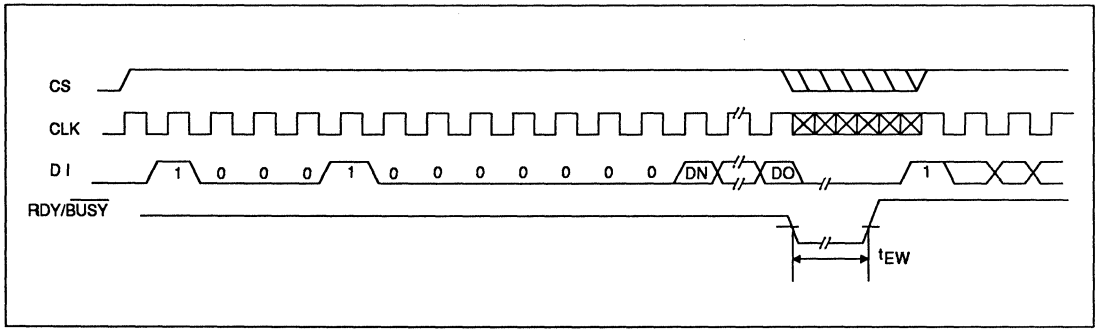
INSTRUCTION TIMING <ERAL 128 x 16 organization>



INSTRUCTION TIMING <WRAL 256 x 8 organization>



INSTRUCTION TIMING <WRAL 128 x 16 organization>



DEVICE OPERATION

The CAT35C202H is a CMOS 2048 bit nonvolatile memory intended for use with all standard controllers. The CAT35C202H can be organized as either 128 registers by 16 bits, or as 256 registers by 8 bits. Six 12 bit instructions (13 bit instruction in 256 by 8 organization) control the reading, writing, and erase operations of the device. The CAT35C202H operates on a single 5V supply and will generate on chip the high voltage required during any programming operations. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normal in a high impedance state except when reading data from the device. The ready/busy status can be determined after a programming operation by polling the RDY/BUSY pin.

The format for all instructions sent to the

CAT35C202H is one logical "1" start bit, a 4 bit op code, a 7 bit address (8 bit address when organized as 256 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 256 X 8).

READ

Upon receiving a READ command and address (clocked into the DI pin), the DO pin of the CAT35C202H will come out of the high impedance state. After sending 1 dummy zero bit the 16 bits (or 8 bits) of data located at the address location specified in the instruction will be shifted out. The data bit being shifted out will toggle on the rising edge of the CLK and becomes stable after the specified time delay (t_{PD1} and t_{PD0}).

ERASE/WRITE ENABLE AND DISABLE

The CAT35C202H powers up in the programming disable state. Any programming after power-up or after a PDS (programming disable) instruction must first be preceded by the PEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed or the PDS instruction is sent. The PDS instruction can be used to disable all the CAT35C202H's program and erase functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT35C202H regardless of the programming enable/disable status.

PROGRAM

After receiving a PROGRAM command, address, and the data, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking erase and data store cycle begins. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C202H can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin.

ERASE ALL

Upon receiving an ERAL command, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking erase sequence starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C202H can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin.

WRITE ALL

Upon receiving a WRAL command and data, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking data store cycle starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C202H can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin. It **IS** necessary for all memory locations to be erased before the WRAL command is executed.

CAT35C202H - High Endurance 2K BIT SERIAL E²PROM

1MHz OPERATION

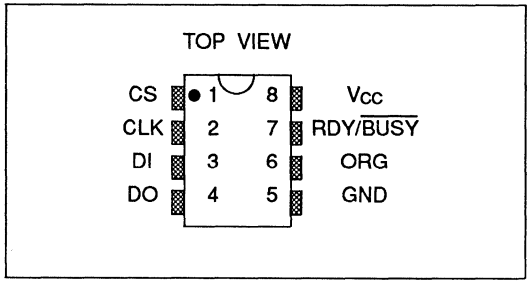
DESCRIPTION

The CAT35C202H is a high endurance CMOS 2K bit Serial E²PROM memory device organized in 128 registers of 16 bits (ORG pin at V_{CC}) or 256 registers of 8 bits each (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT35C202H is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 100,000 erase/write cycles and has a data retention of 100 years. Packaged in an 8-pin DIP and Small Outline packages. To be offered in a 3V version (CAT33C202).

FEATURES

- Highly reliable CMOS floating gate technology
- 10ms programming cycle
- Single 5V supply
- 128x16 or 256x8 user selectable serial memory
- Compatible with General Instruments ER5912
- Self timed programming cycle with Autoerase
- Word and chip erasable
- Operating range 0°C to 70°C
- 100,000 erase/write cycles
- 100 year data retention
- Power-up inadvertent write protection

PIN CONFIGURATION

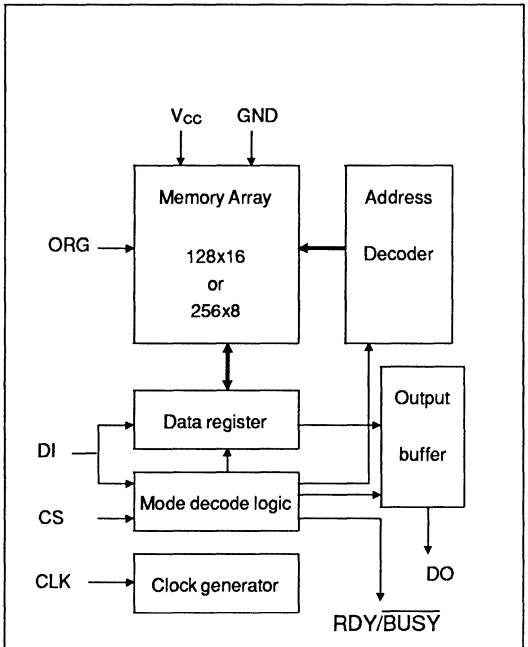


PIN FUNCTIONS

CS	Chip select
CLK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
RDY/BUSY	Status output
GND	Ground
ORG	Memory organization

Note: When the ORG pin is connected to V_{CC}, the 128x16 organization is selected. When it is connected to ground, the 256x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 128x16 organization.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature . . . . . -65°C to +150°C
Power supply (V_{CC}) . . . . . +7V
Voltage on any input pin . . . . . -0.3 to +7V
Voltage on any output pin . . . . . -0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC1}	Current consumption (operating)	DI=0.0V, SK=5.0V V_{CC} =5.0V, CS = 5.0V DO unloaded			3	mA
I_{CC2}	Current consumption (stand-by)	V_{CC} = 5.5V, CS = 0 DI = 0, SK = 0			100	µA
I_{LI}	Input leakage current	V_{IN} = 5.5V			10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V, CS = 0			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V

INSTRUCTION SET

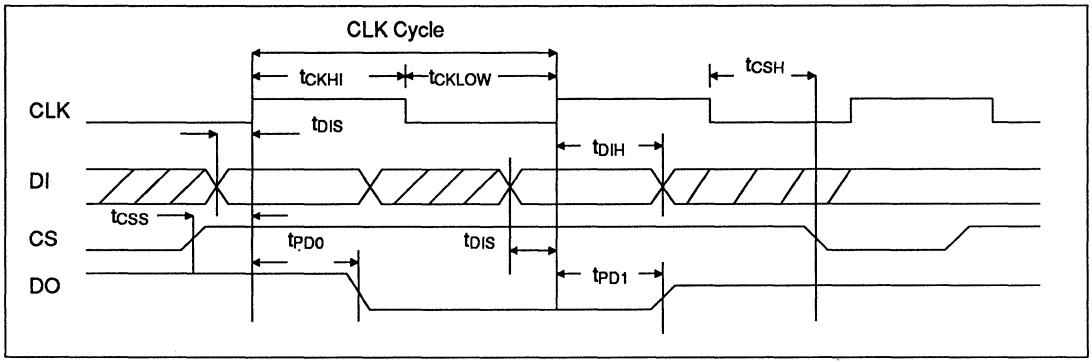
Instruction	Start Bit	Opcode	Address		Data		Comments
			256 x 8	128 x 16	256 x 8	128 x 16	
READ	1	1000	A7 - A0	A6 - A0			Read address AN - A0
PROGRAM	1	X100	A7 - A0	A6 - A0	D7 - D0	D15 - D0	Program address AN - A0
PEN	1	0011	00000000	0000000			Program enable
PDS	1	0000	00000000	0000000			Program disable
ERAL	1	0010	00000000	0000000			Erase all addresses
WRAL	1	0001	00000000	0000000	D7 - D0	D15 - D0	Write all addresses

AC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{CSS}	CS setup time		50			ns
t_{CSH}	CS hold time	C_L = 100pF V_{OL} = 0.8V, V_{OH} = 2.0V V_{IL} = 0.45V, V_{IH} = 2.4V	100			ns
t_{DIS}	DI setup time		100			ns
t_{DIH}	DI hold time		100			ns
t_{PD1}	Output delay to 1				500	ns
t_{PD0}	Output delay to 0				500	ns
t_{EW}	Erase/Write pulse width				10	ms
t_{SKHI}	Minimum SK high time		250			ns
t_{SKLOW}	Minimum SK low time		250			ns
CK_{MAX}	Maximum clock frequency		DC		1	MHz

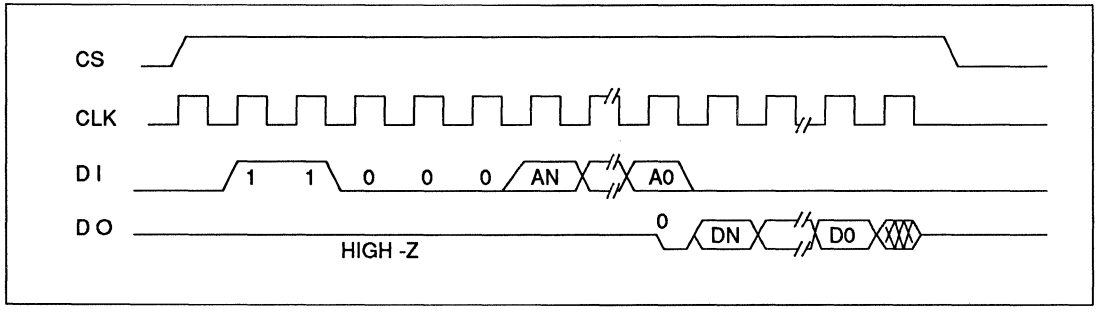
SYNCHRONOUS TIMINGS



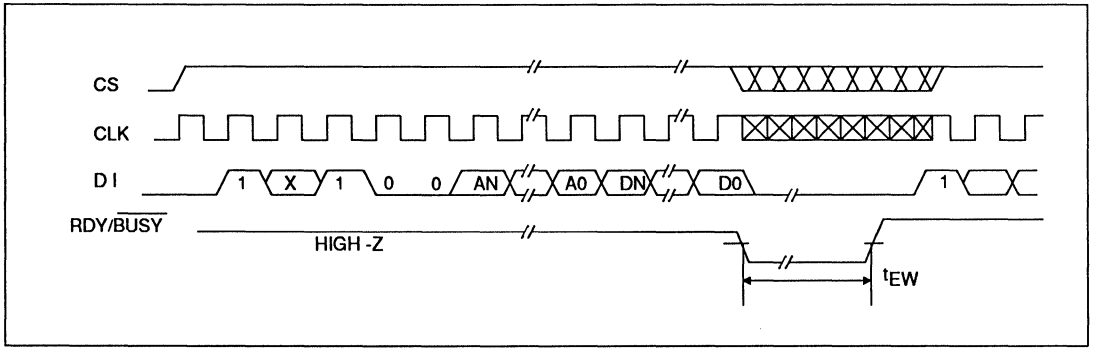
INSTRUCTION TIMING <ORGANIZATION>

Organization	A_N (or AN)	D_N (or DN)
256 x 8	A_7	D_7
128 x 16	A_6	D_{15}

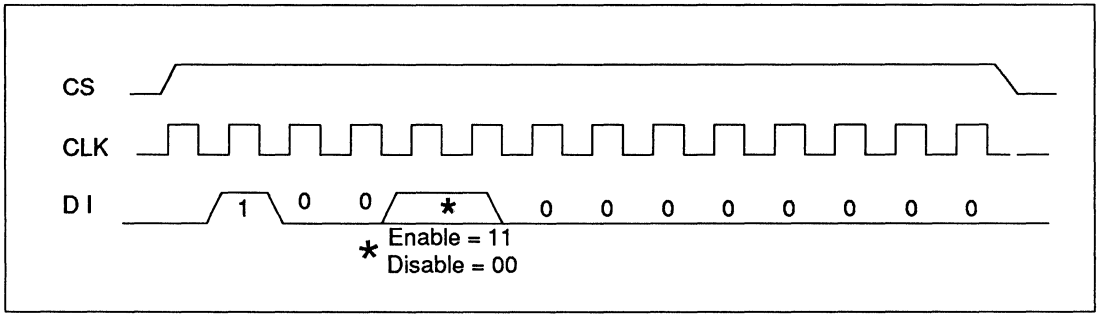
INSTRUCTION TIMING <READ>



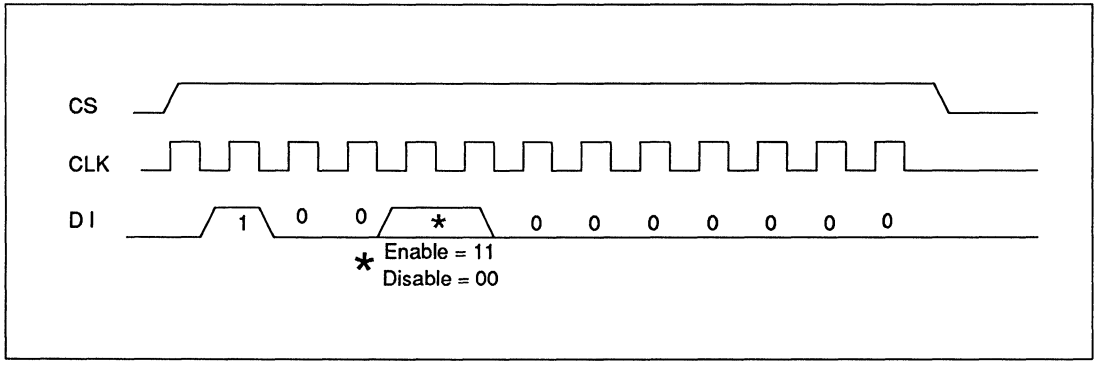
INSTRUCTION TIMING <PROGRAM>



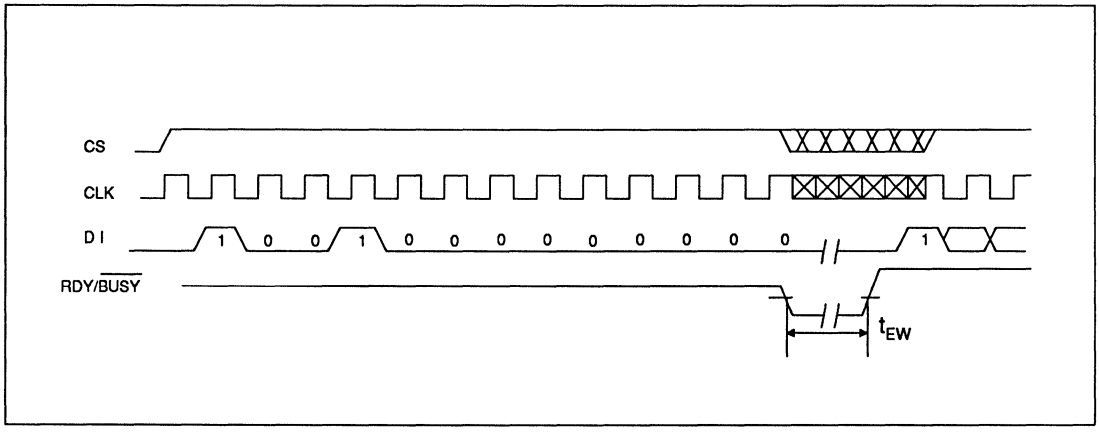
INSTRUCTION TIMING <PEN, PDS 256 x 8 organization>



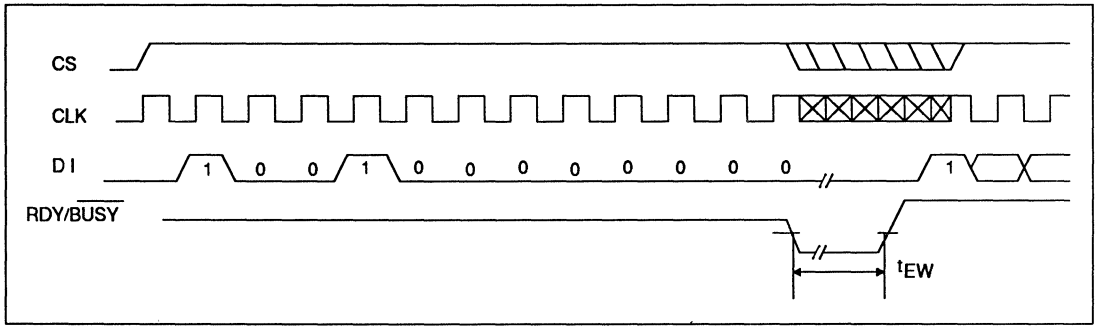
INSTRUCTION TIMING <PEN, PDS 128 x 16 organization>



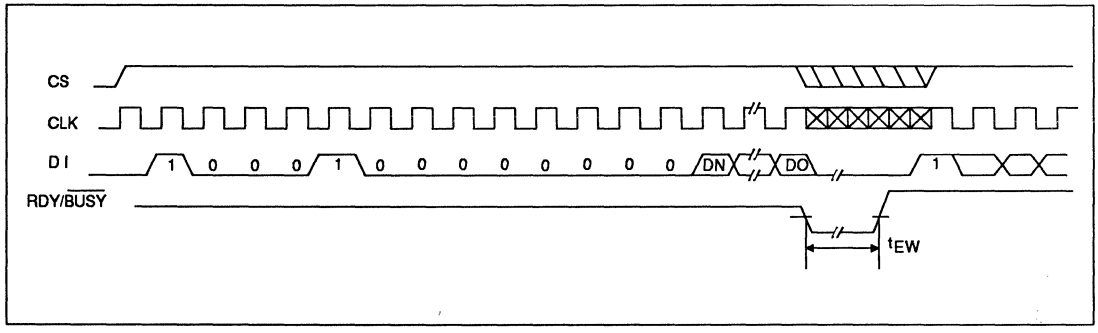
INSTRUCTION TIMING <ERAL 256 x 8 organization>



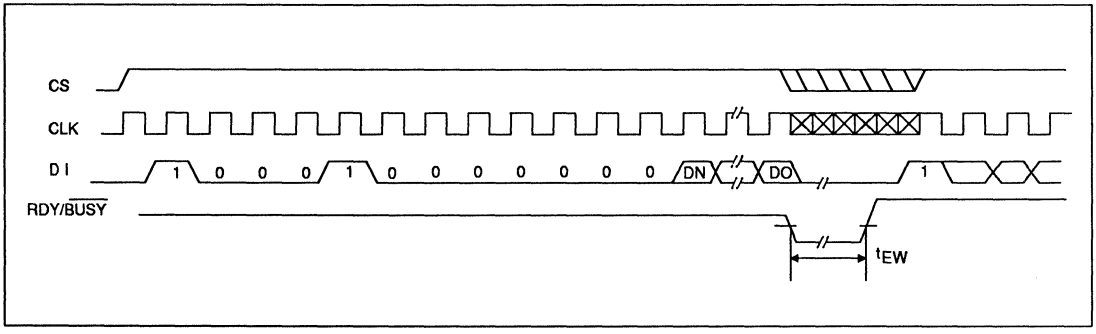
INSTRUCTION TIMING <ERAL 128 x 16 organization>



INSTRUCTION TIMING <WRAL 256 x 8 organization>



INSTRUCTION TIMING <WRAL 128 x 16 organization>



DEVICE OPERATION

The CAT35C202H is a CMOS 2048 bit nonvolatile memory intended for use with all standard controllers. The CAT35C202H can be organized as either 128 registers by 16 bits, or as 256 registers by 8 bits. Six 12 bit instructions (13 bit instruction in 256 by 8 organization) control the reading, writing, and erase operations of the device. The CAT35C202H operates on a single 5V supply and will generate on chip the high voltage required during any programming operations. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normal in a high impedance state except when reading data from the device. The ready/busy status can be determined after a programming operation by polling the RDY/BUSY pin.

The format for all instructions sent to the

CAT35C202H is one logical "1" start bit, a 4 bit op code, a 7 bit address (8 bit address when organized as 256 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 256 X 8).

READ

Upon receiving a READ command and address (clocked into the DI pin), the DO pin of the CAT35C202H will come out of the high impedance state. After sending 1 dummy zero bit the 16 bits (or 8 bits) of data located at the address location specified in the instruction will be shifted out. The data bit being shifted out will toggle on the rising edge of the CLK and becomes stable after the specified time delay (t_{PD1} and t_{PD0}).

ERASE/WRITE ENABLE AND DISABLE

The CAT35C202H powers up in the programming disable state. Any programming after power-up or after a PDS (programming disable) instruction must first be preceded by the PEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed or the PDS instruction is sent. The PDS instruction can be used to disable all the CAT35C202H's program and erase functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT35C202H regardless of the programming enable/disable status.

PROGRAM

After receiving a PROGRAM command, address, and the data, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking erase and data store cycle begins. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C202H can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin.

ERASE ALL

Upon receiving an ERAL command, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking erase sequence starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C202H can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin.

WRITE ALL

Upon receiving a WRAL command and data, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking data store cycle starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C202H can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin. It **IS** necessary for all memory locations to be erased before the WRAL command is executed.

CAT35C202I - Industrial Temperature 1MHz
2K BIT SERIAL E^2PROM OPERATION

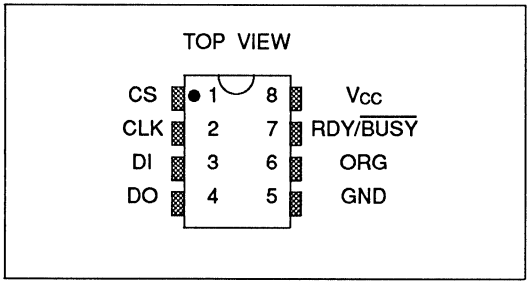
DESCRIPTION

The CAT35C202I is an industrial temperature CMOS 2K bit Serial E^2PROM memory device organized in 128 registers of 16 bits (ORG pin at V_{CC}) or 256 registers of 8 bits each (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT35C202I is manufactured using Catalyst's advanced CMOS E^2PROM floating gate technology. It is designed to endure 10,000 erase/write cycles and has a data retention of 10 years. It is packaged in an 8-pin DIP and Small Outline packages. To be offered in a 3V version (CAT33C202).

FEATURES

- Highly reliable CMOS floating gate technology
- 10ms programming cycle
- Single 5V supply
- 128x16 or 256x8 user selectable serial memory
- Compatible with General Instruments ER5912
- Self timed programming cycle with Autoerase
- Word and chip erasable
- Operating range -40°C to +85°C
- 10,000 erase/write cycles
- 10 year data retention
- Power-up inadvertent write protection

PIN CONFIGURATION

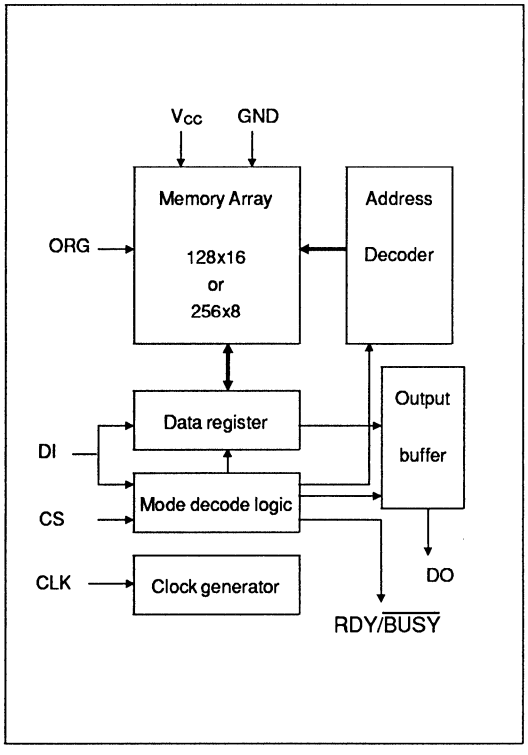


PIN FUNCTIONS

CS	Chip select
CLK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
RDY/BUSY	Status output
GND	Ground
ORG	Memory organization

Note: When the ORG pin is connected to V_{CC}, the 128x16 organization is selected. When it is connected to ground, the 256x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 128x16 organization.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature . . . . . -65°C to +150°C
Power supply (V_{CC}) . . . . . +7V
Voltage on any input pin . . . . . -0.3 to +7V
Voltage on any output pin . . . . . -0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC1}	Current consumption (operating)	DI=0.0V, SK=5.0V V_{CC} =5.0V, CS = 5.0V DO unloaded			4	mA
I_{CC2}	Current consumption (stand-by)	V_{CC} = 5.5V, CS = 0 DI = 0, SK = 0			100	µA
I_{LI}	Input leakage current	V_{IN} = 5.5V			10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V, CS = 0			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V

INSTRUCTION SET

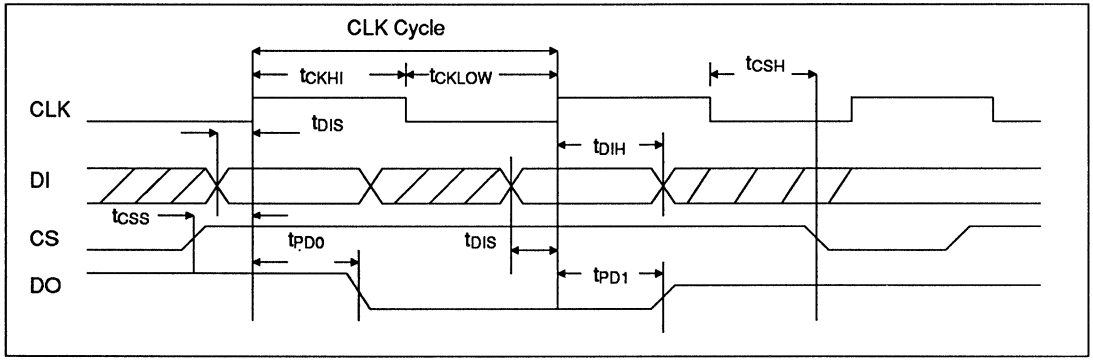
Instruction	Start Bit	Opcode	Address		Data		Comments
			256 x 8	128 x 16	256 x 8	128 x 16	
READ	1	1000	A7 - A0	A6 - A0			Read address AN - A0
PROGRAM	1	X100	A7 - A0	A6 - A0	D7 - D0	D15 - D0	Program address AN - A0
PEN	1	0011	00000000	0000000			Program enable
PDS	1	0000	00000000	0000000			Program disable
ERAL	1	0010	00000000	0000000			Erase all addresses
WRAL	1	0001	00000000	0000000	D7 - D0	D15 - D0	Write all addresses

AC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{CSS}	CS setup time		50			ns
t_{CSH}	CS hold time	C_L = 100pF V_{OL} = 0.8V, V_{OH} = 2.0V V_{IL} = 0.45V, V_{IH} = 2.4V	100			ns
t_{DIS}	DI setup time		100			ns
t_{DIH}	DI hold time		100			ns
t_{PD1}	Output delay to 1				500	ns
t_{PD0}	Output delay to 0				500	ns
t_{EW}	Erase/Write pulse width				10	ms
t_{SKHI}	Minimum SK high time		250			ns
t_{SKLOW}	Minimum SK low time		250			ns
CK_{MAX}	Maximum clock frequency		DC		1	MHz

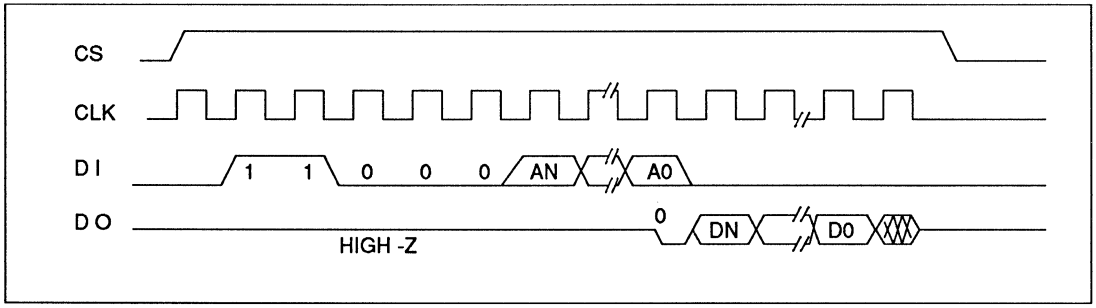
SYNCHRONOUS TIMINGS



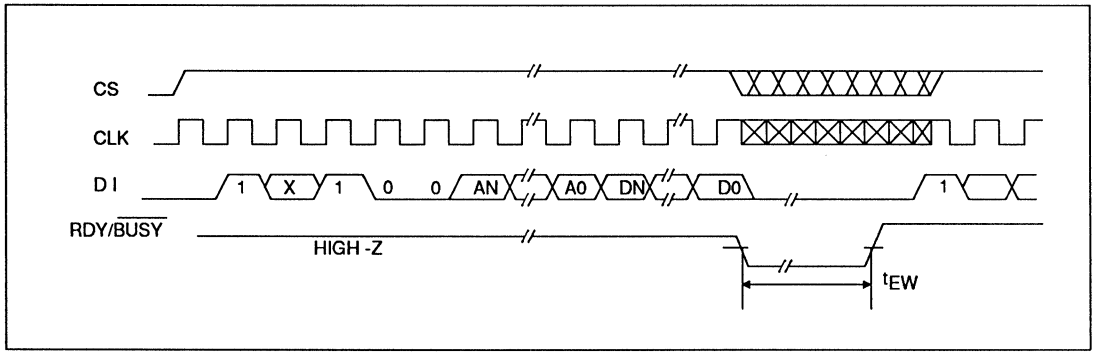
INSTRUCTION TIMING <ORGANIZATION>

Organization	A_N (or AN)	D_N (or DN)
256 x 8	A_7	D_7
128 x 16	A_6	D_{15}

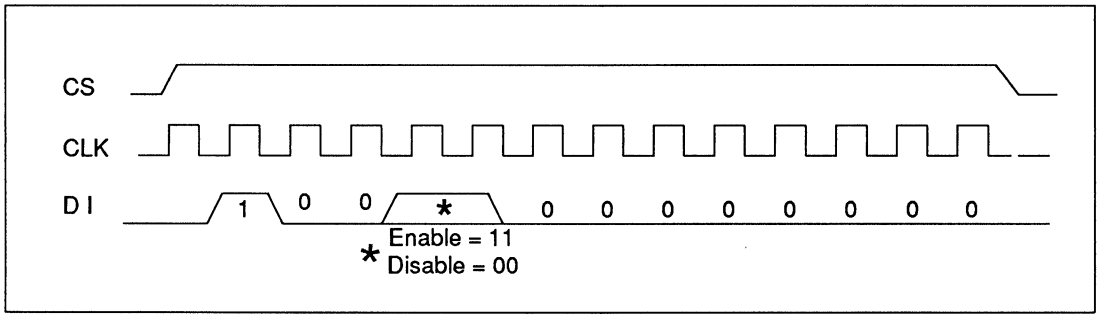
INSTRUCTION TIMING <READ>



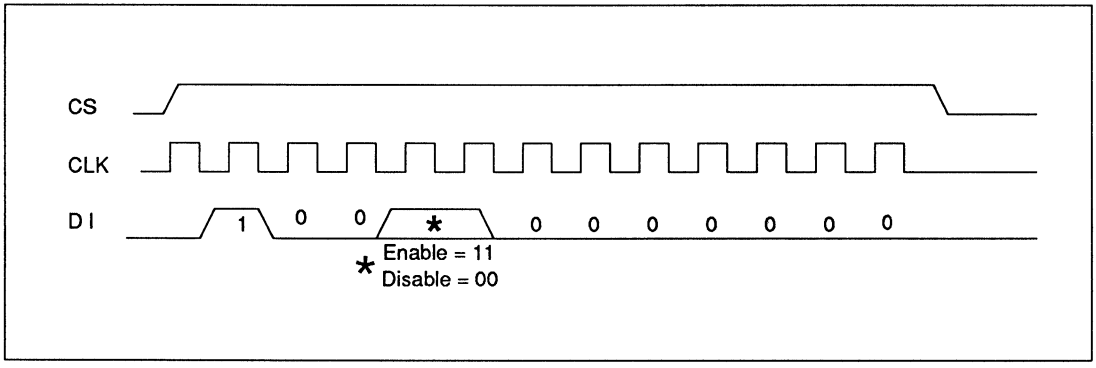
INSTRUCTION TIMING <PROGRAM>



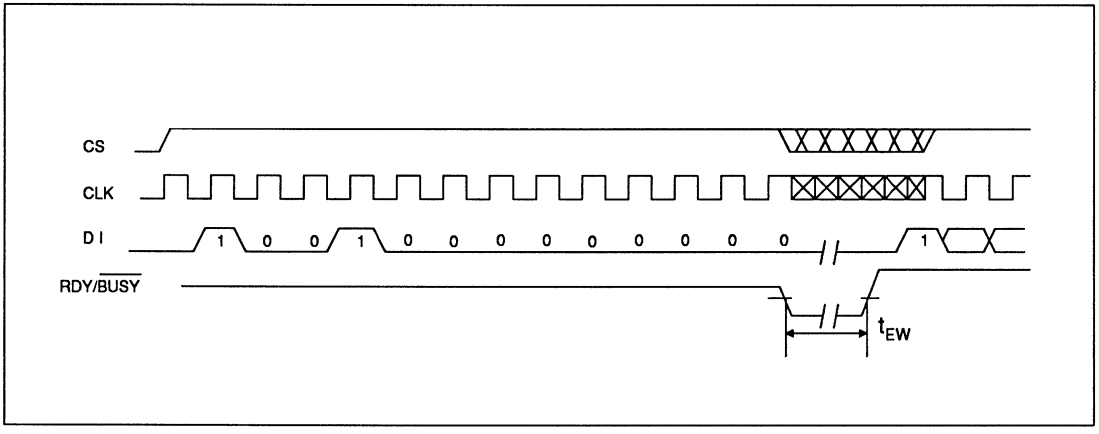
INSTRUCTION TIMING <PEN, PDS 256 x 8 organization>



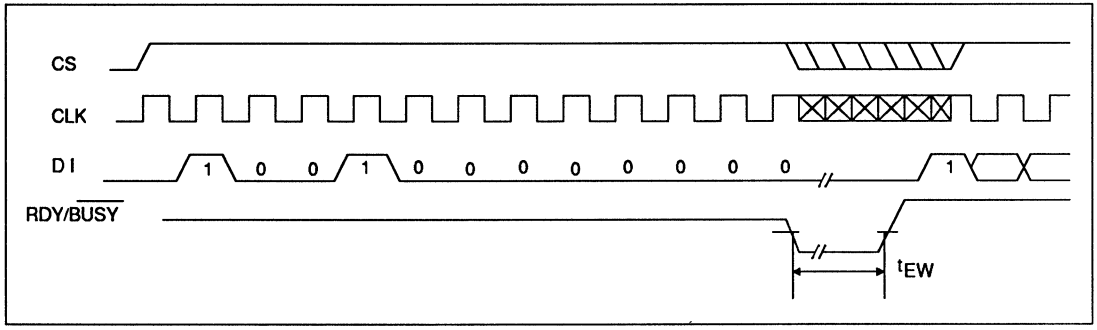
INSTRUCTION TIMING <PEN, PDS 128 x 16 organization>



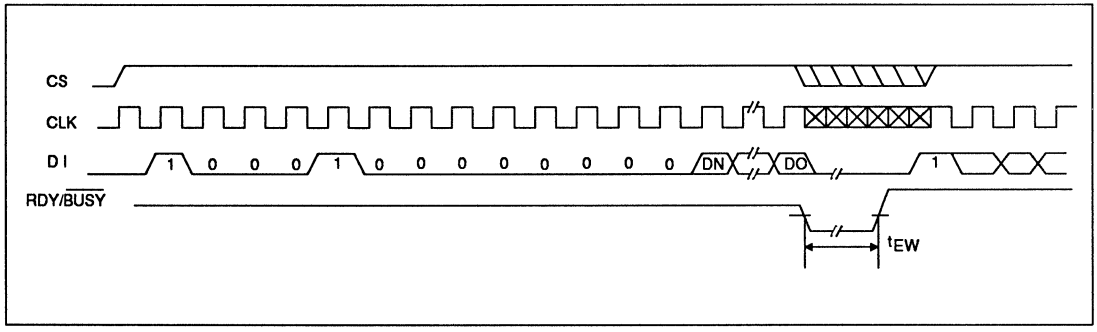
INSTRUCTION TIMING <ERAL 256 x 8 organization>



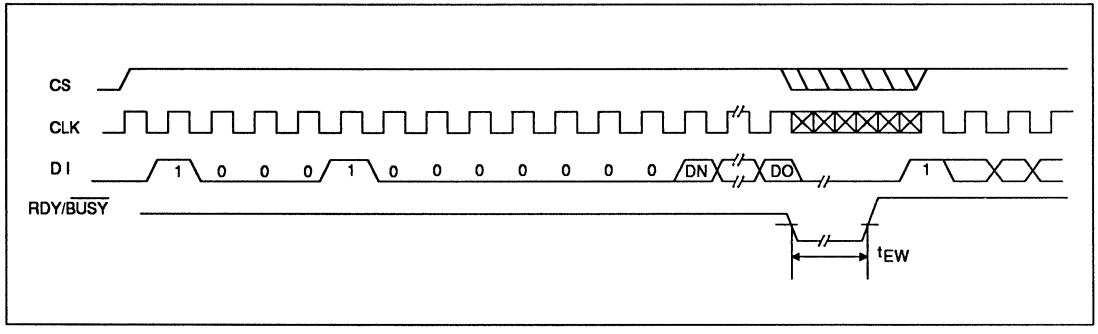
INSTRUCTION TIMING <ERAL 128 x 16 organization>



INSTRUCTION TIMING <WRAL 256 x 8 organization>



INSTRUCTION TIMING <WRAL 128 x 16 organization>



DEVICE OPERATION

The CAT35C202I is a CMOS 2048 bit nonvolatile memory intended for use with all standard controllers. The CAT35C202I can be organized as either 128 registers by 16 bits, or as 256 registers by 8 bits. Six 12 bit instructions (13 bit instruction in 256 by 8 organization) control the reading, writing, and erase operations of the device. The CAT35C202I operates on a single 5V supply and will generate on chip the high voltage required during any programming operations. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normal in a high impedance state except when reading data from the device. The ready/busy status can be determined after a programming operation by polling the RDY/BUSY pin.

The format for all instructions sent to the

CAT35C202I is one logical "1" start bit, a 4 bit op code, a 7 bit address (8 bit address when organized as 256 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 256 X 8).

READ

Upon receiving a READ command and address (clocked into the DI pin), the DO pin of the CAT35C202I will come out of the high impedance state. After sending 1 dummy zero bit the 16 bits (or 8 bits) of data located at the address location specified in the instruction will be shifted out. The data bit being shifted out will toggle on the rising edge of the CLK and becomes stable after the specified time delay (t_{PD1} and t_{PD0}).

ERASE/WRITE ENABLE AND DISABLE

The CAT35C202I powers up in the programming disable state. Any programming after power-up or after a PDS (programming disable) instruction must first be preceded by the PEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed or the PDS instruction is sent. The PDS instruction can be used to disable all the CAT35C202I's program and erase functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT35C202I regardless of the programming enable/disable status.

PROGRAM

After receiving a PROGRAM command, address, and the data, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking erase and data store cycle begins. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C202I can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin.

ERASE ALL

Upon receiving an ERAL command, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking erase sequence starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C202I can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin.

WRITE ALL

Upon receiving a WRAL command and data, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking data store cycle starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C202I can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin. It **IS** necessary for all memory locations to be erased before the WRAL command is executed.

CAT35C204
4K BIT SERIAL E²PROM

1MHz OPERATION

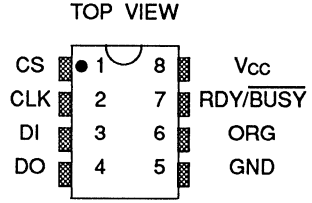
DESCRIPTION

The CAT35C204 is a 4K bit Serial E²PROM memory device organized in 256 registers of 16 bits (ORG pin at V_{CC}) or 512 registers of 8 bits each (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT35C204 is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 10,000 erase/write cycles and has a data retention of 10 years. Packaged in an 8-pin DIP and Small Outline packages. Also to be available in a 3V version (CAT33C204).

FEATURES

- Compatible with General Instruments ER5912
- Single 5V supply
- 256x16 or 512x8 user selectable serial memory
- 10ms programming cycle
- Self timed programming cycle with Autoerase
- Highly reliable CMOS floating gate technology
- Word and chip erasable
- Operating range 0°C to +70°C [Industrial temp. range available]
- 10,000 erase/write cycles
- 10 year data retention
- Power-up inadvertent write protection

PIN CONFIGURATION

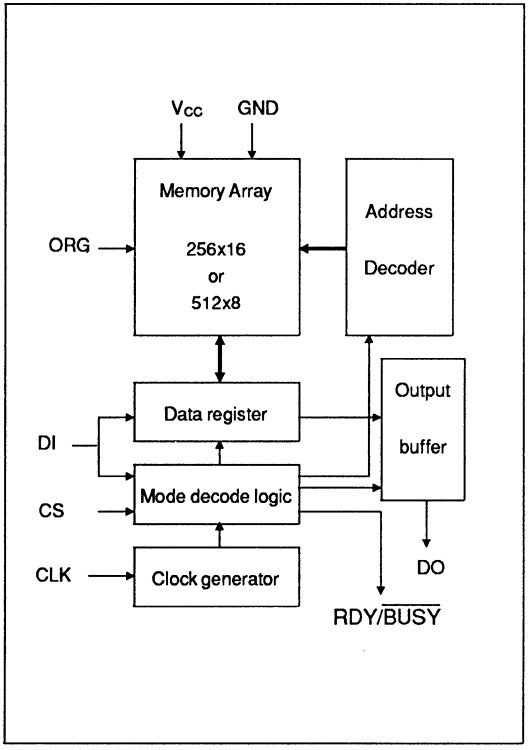


PIN FUNCTIONS

CS	Chip select
CLK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
RDY/BUSY	Status output
GND	Ground
ORG	Memory organization

Note: When the ORG pin is connected to V_{CC}, the 256x16 organization is selected. When it is connected to ground, the 512x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 256x16 organization.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature . . . . . -65°C to +150°C
Power supply (V_{CC}) . . . . . +7V
Voltage on any input pin . . . . . -0.3 to +7V
Voltage on any output pin . . . . . -0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC1}	Current consumption (operating)	DI=0.0V, SK=5.0V V_{CC} =5.0V, CS = 5.0V DO unloaded			3	mA
I_{CC2}	Current consumption (stand-by)	V_{CC} = 5.5V, CS = 0 DI = 0, SK = 0			100	µA
I_{LI}	Input leakage current	V_{IN} = 5.5V			10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V, CS = 0			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V

INSTRUCTION SET

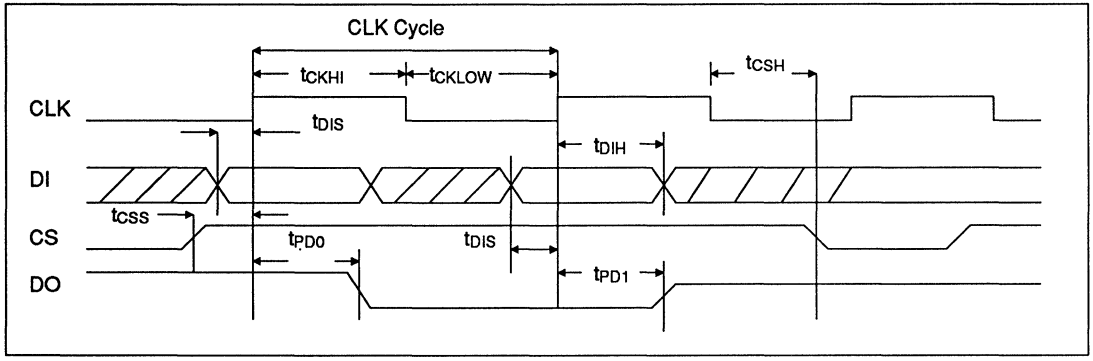
Instruction	Start Bit	Opcode	Address		Data		Comments
			512 x 8	256 x 16	512 x 8	256 x 16	
READ	1	1000	A8 - A0	A7 - A0			Read address AN - A0
PROGRAM	1	X100	A8 - A0	A7 - A0	D7 - D0	D15 - D0	Program address AN - A0
PEN	1	0011	000000000	00000000			Program enable
PDS	1	0000	000000000	00000000			Program disable
ERAL	1	0010	000000000	00000000			Erase all addresses
WRAL	1	0001	000000000	00000000	D7 - D0	D15 - D0	Write all addresses

AC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{CSS}	CS setup time		50			ns
t_{CSH}	CS hold time	C_L = 100pF V_{OL} = 0.8V, V_{OH} = 2.0V V_{IL} = 0.45V, V_{IH} = 2.4V	100			ns
t_{DIS}	DI setup time		100			ns
t_{DIH}	DI hold time		100			ns
t_{PD1}	Output delay to 1				500	ns
t_{PD0}	Output delay to 0				500	ns
t_{EW}	Erase/Write pulse width				10	ms
t_{SKHI}	Minimum SK high time		250			ns
t_{SKLOW}	Minimum SK low time		250			ns
CK_{MAX}	Maximum clock frequency		DC		1	MHz

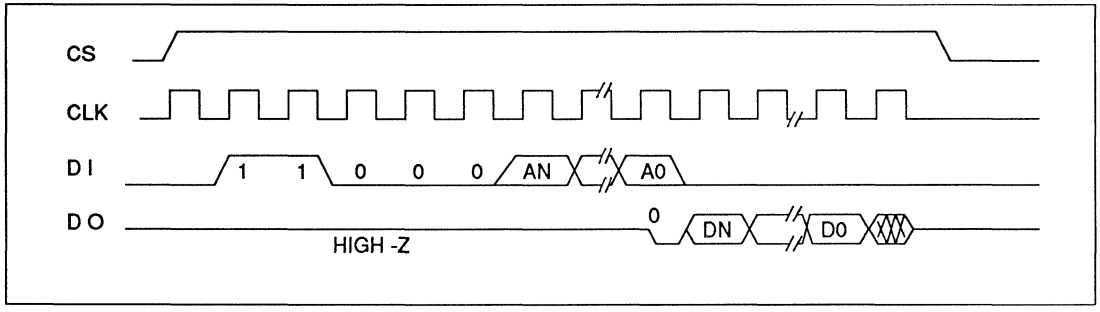
SYNCHRONOUS TIMINGS



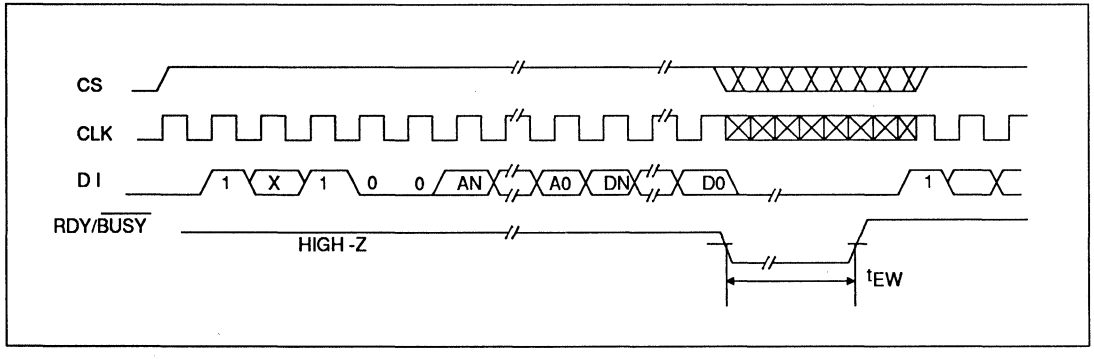
INSTRUCTION TIMING <ORGANIZATION>

Organization	A_N (or AN)	D_N (or DN)
512 x 8	A_8	D_7
256 x 16	A_7	D_{15}

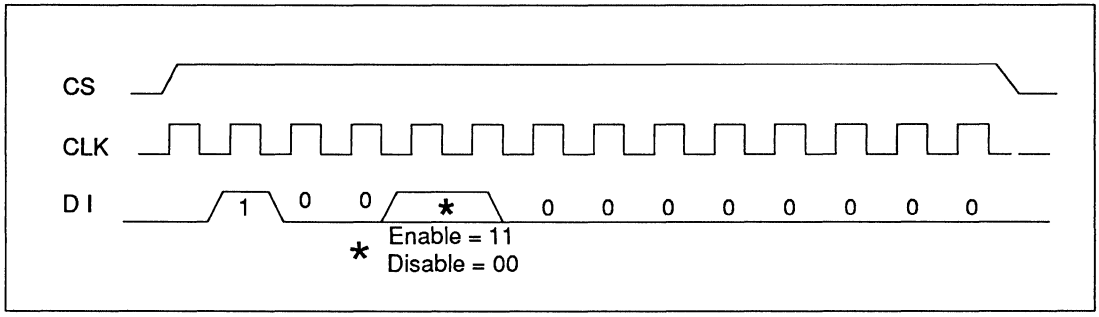
INSTRUCTION TIMING <READ>



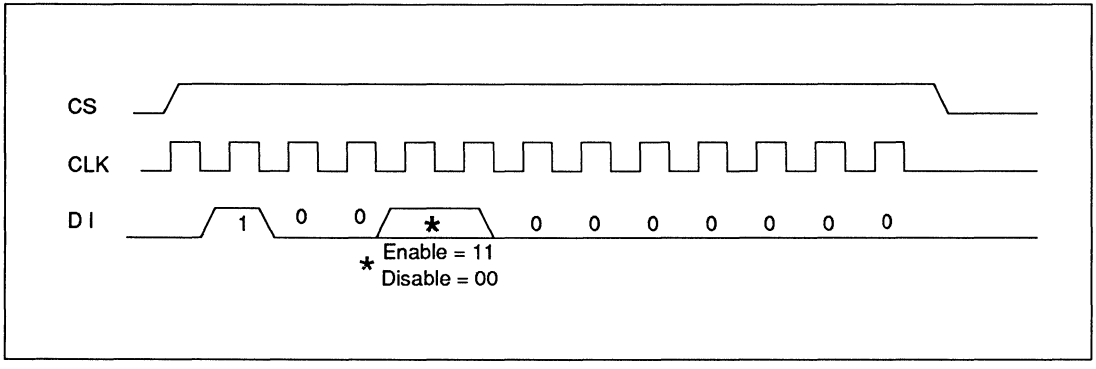
INSTRUCTION TIMING <PROGRAM>



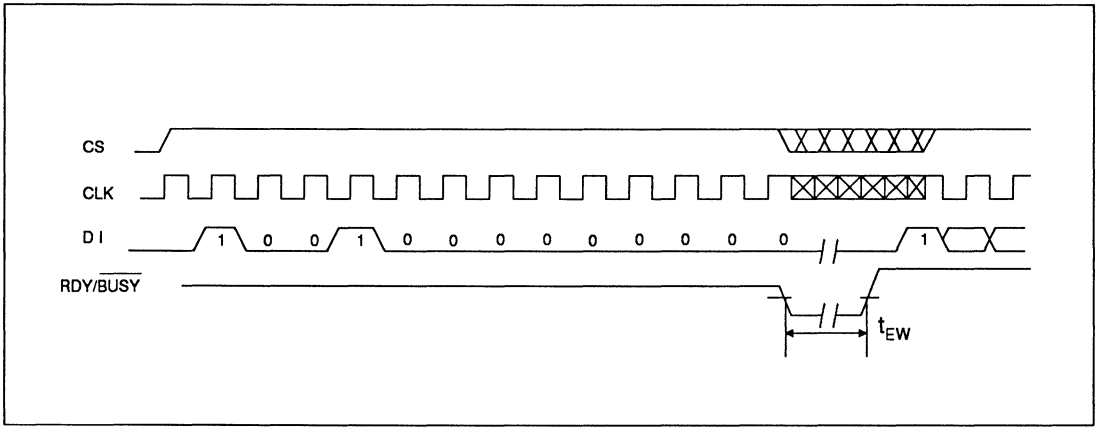
INSTRUCTION TIMING <PEN, PDS 512 x 8 organization>



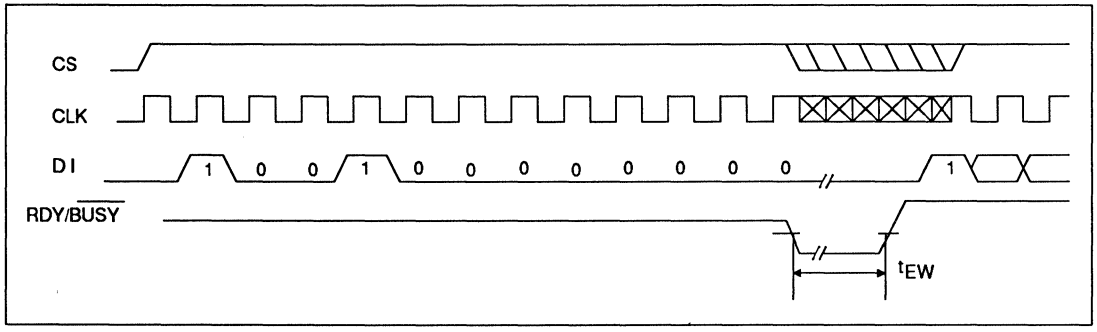
INSTRUCTION TIMING <PEN, PDS 256 x 16 organization>



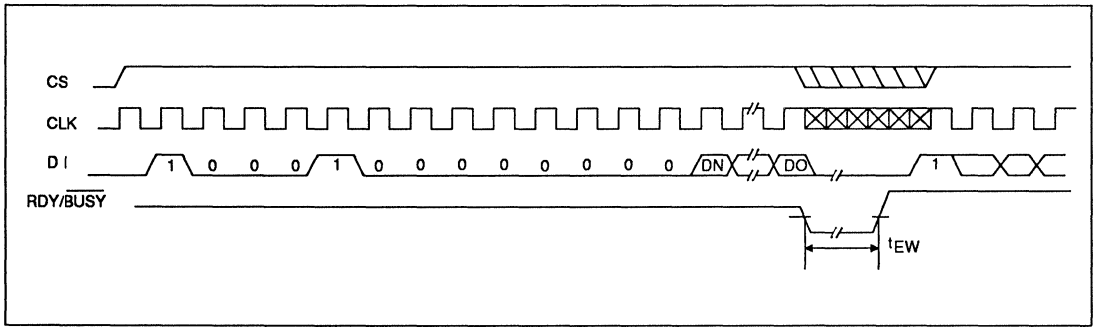
INSTRUCTION TIMING <ERAL 512 x 8 organization>



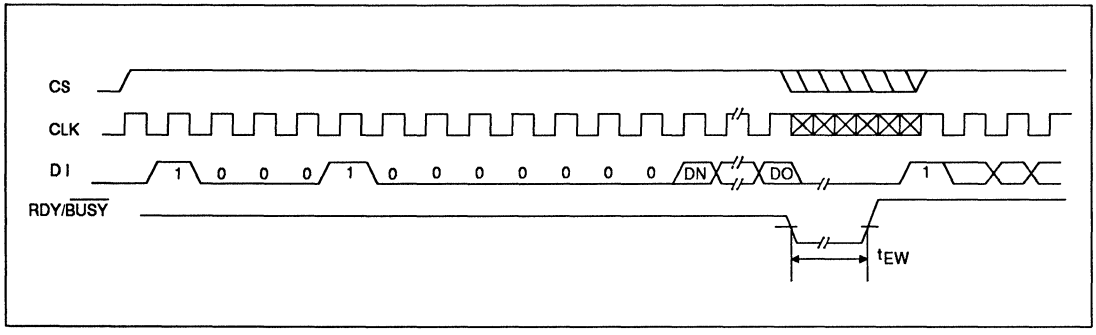
INSTRUCTION TIMING <ERAL 256 x 16 organization>



INSTRUCTION TIMING <WRAL 512 x 8 organization>



INSTRUCTION TIMING <WRAL 256 x 16 organization>



DEVICE OPERATION

The CAT35C204H is a high endurance 4096 bit nonvolatile memory intended for use with all standard controllers. The CAT35C204H can be organized as either 256 registers by 16 bits, or as 512 registers by 8 bits. Six 13 bit instructions (14 bit instruction in 512 by 8 organization) control the reading, writing, and erase operations of the device. The CAT35C204H operates on a single 5V supply and will generate on chip the high voltage required during any programming operations. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normal in a high impedance state except when reading data from the device. The ready/busy status can be determined after a programming operation by polling the RDY/$\overline{\text{BUSY}}$ pin.

The format for all instructions sent to the CAT35C204H is one logical "1" start bit, a 4 bit op code, an 8 bit address (9 bit address when organized as 512 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 512 X 8).

READ

Upon receiving a READ command and address (clocked into the DI pin), the DO pin of the CAT35C204H will come out of the high impedance state. After sending 1 dummy zero bit the 16 bits (or 8 bits) of data located at the address location specified in the instruction will be shifted out. The data bit being shifted out will toggle on the rising edge of the CLK and becomes stable after the specified time delay (t_{PD1} and t_{PD0}).

ERASE/WRITE ENABLE AND DISABLE

The CAT35C204H powers up in the programming disable state. Any programming after power-up or after a PDS (programming disable) instruction must first be preceded by the PEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed or the PDS instruction is sent. The PDS instruction can be used to disable all the CAT35C204H's program and erase functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT35C204H regardless of the programming enable/disable status.

PROGRAM

After receiving a PROGRAM command, address, and the data, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking erase and data store cycle begins. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C204H can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin.

ERASE ALL

Upon receiving an ERAL command, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking erase sequence starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C204H can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin. Once erased, all memory bits return to logical "1" state.

WRITE ALL

Upon receiving a WRAL command and data, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking data store cycle starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C204H can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin. It **IS NOT** necessary for all memory locations to be erased before the WRAL command is executed.

CAT35C204H - High Endurance 4K BIT SERIAL E^2PROM

1MHz OPERATION

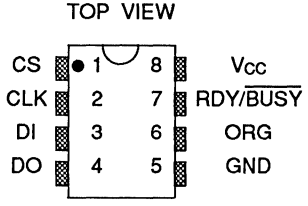
DESCRIPTION

The CAT35C204H is a high endurance 4K bit Serial E^2PROM memory device organized in 256 registers of 16 bits (ORG pin at V_{CC}) or 512 registers of 8 bits each (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT35C204H is manufactured using Catalyst's advanced CMOS E^2PROM floating gate technology. It is designed to endure 100,000 erase/write cycles and has a data retention of 100 years. Packaged in an 8-pin DIP and Small Outline packages. Also to be available in a 3V version (CAT33C204H).

FEATURES

- Compatible with General Instruments ER5912
- Single 5V supply
- 256x16 or 512x8 user selectable serial memory
- 10ms programming cycle
- Self timed programming cycle with Autoerase
- Highly reliable CMOS floating gate technology
- Word and chip erasable
- Operating range 0°C to +70°C
- 100,000 erase/write cycles
- 100 year data retention
- Power-up inadvertent write protection

PIN CONFIGURATION

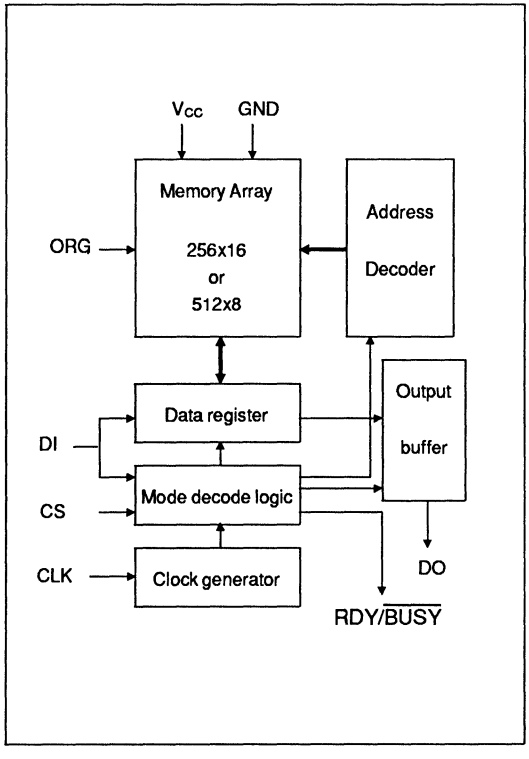


PIN FUNCTIONS

CS	Chip select
CLK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
RDY/BUSY	Status output
GND	Ground
ORG	Memory organization

Note: When the ORG pin is connected to V_{CC}, the 256x16 organization is selected. When it is connected to ground, the 512x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 256x16 organization.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature . . . . . -65°C to +150°C
Power supply (V_{CC}) . . . . . +7V
Voltage on any input pin . . . . . -0.3 to +7V
Voltage on any output pin . . . . . -0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC1}	Current consumption (operating)	DI=0.0V, SK=5.0V V_{CC} =5.0V, CS = 5.0V DO unloaded			3	mA
I_{CC2}	Current consumption (stand-by)	V_{CC} = 5.5V, CS = 0 DI = 0, SK = 0			100	µA
I_{LI}	Input leakage current	V_{IN} = 5.5V			10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V, CS = 0			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V

INSTRUCTION SET

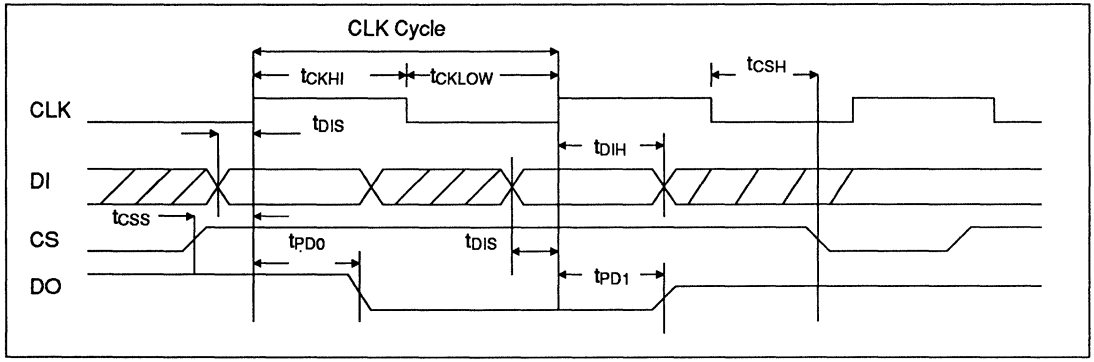
Instruction	Start Bit	Opcode	Address		Data		Comments
			512 x 8	256 x 16	512 x 8	256 x 16	
READ	1	1000	A8 - A0	A7 - A0			Read address AN - A0
PROGRAM	1	X100	A8 - A0	A7 - A0	D7 - D0	D15 - D0	Program address AN - A0
PEN	1	0011	000000000	00000000			Program enable
PDS	1	0000	000000000	00000000			Program disable
ERAL	1	0010	000000000	00000000			Erase all addresses
WRAL	1	0001	000000000	00000000	D7 - D0	D15 - D0	Write all addresses

AC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{CSS}	CS setup time		50			ns
t_{CSH}	CS hold time	C_L = 100pF V_{OL} = 0.8V, V_{OH} = 2.0V V_{IL} = 0.45V, V_{IH} = 2.4V	100			ns
t_{DIS}	DI setup time		100			ns
t_{DIH}	DI hold time		100			ns
t_{PD1}	Output delay to 1				500	ns
t_{PD0}	Output delay to 0				500	ns
t_{EW}	Erase/Write pulse width				10	ms
t_{SKHI}	Minimum SK high time		250			ns
t_{SKLOW}	Minimum SK low time		250			ns
CK_{MAX}	Maximum clock frequency		DC		1	MHz

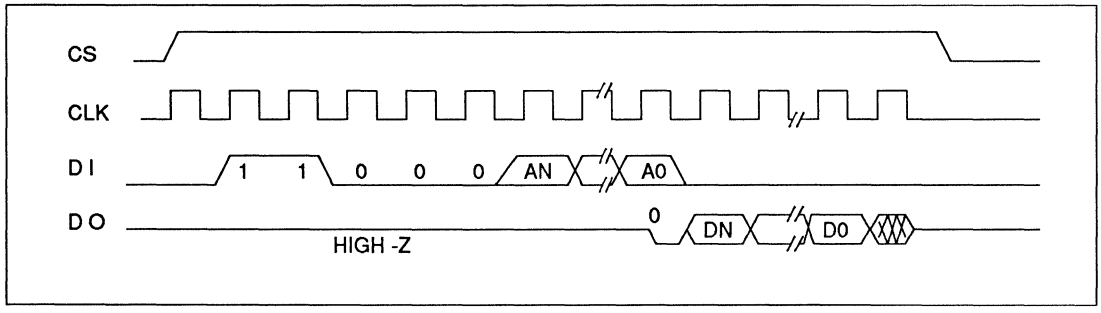
SYNCHRONOUS TIMINGS



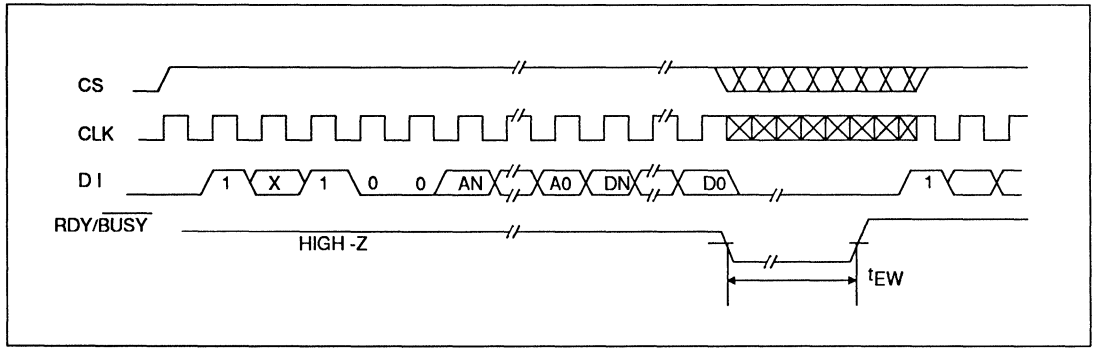
INSTRUCTION TIMING <ORGANIZATION>

Organization	A_N (or AN)	D_N (or DN)
512 x 8	A_8	D_7
256 x 16	A_7	D_{15}

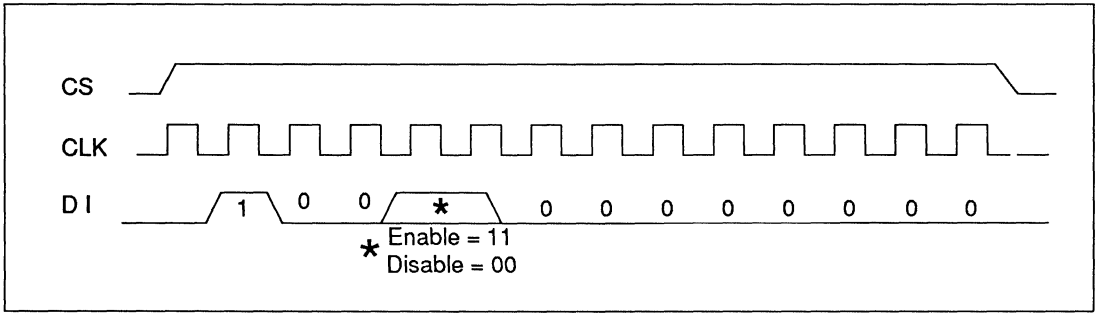
INSTRUCTION TIMING <READ>



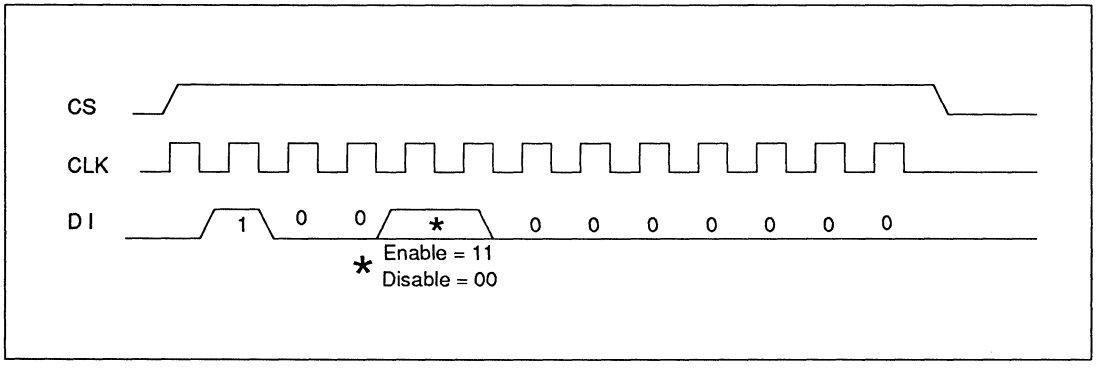
INSTRUCTION TIMING <PROGRAM>



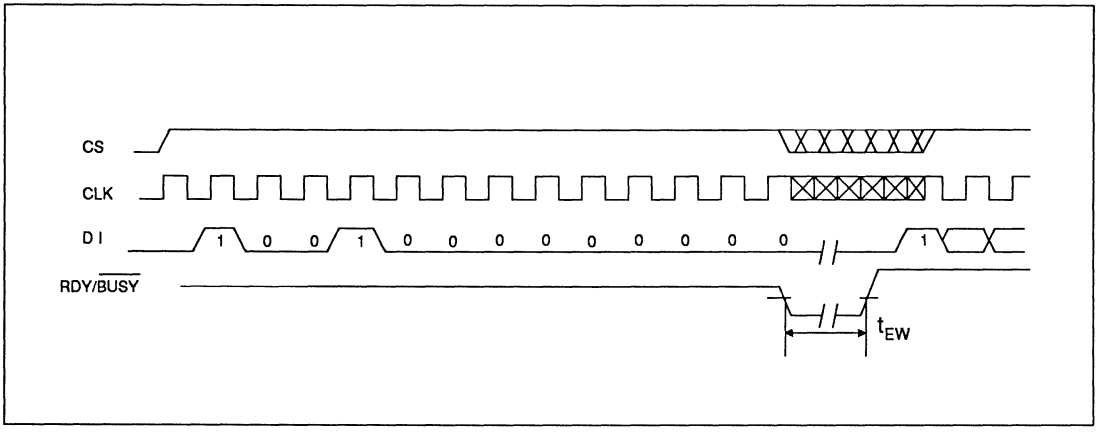
INSTRUCTION TIMING <PEN, PDS 512 x 8 organization>



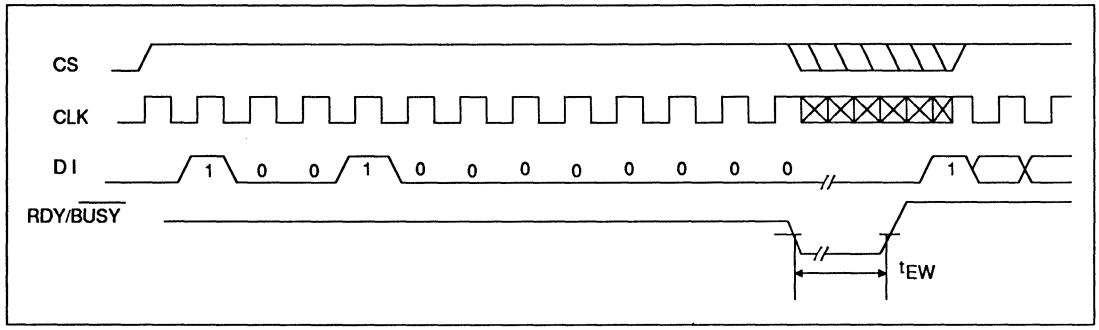
INSTRUCTION TIMING <PEN, PDS 256 x 16 organization>



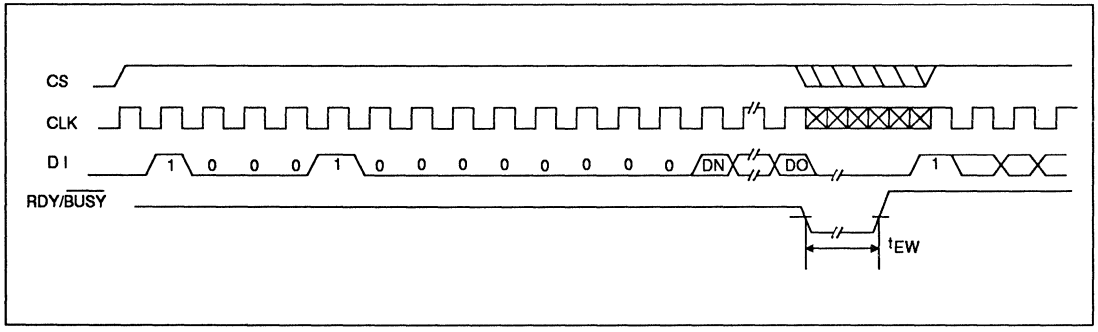
INSTRUCTION TIMING <ERAL 512 x 8 organization>



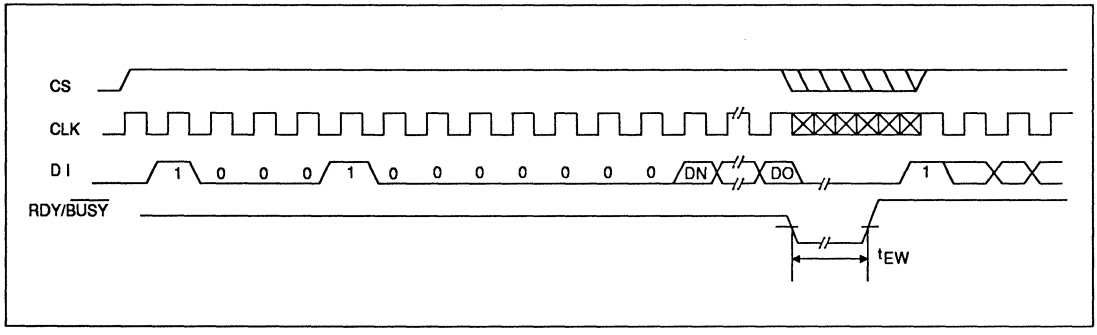
INSTRUCTION TIMING <ERAL 256 x 16 organization>



INSTRUCTION TIMING <WRAL 512 x 8 organization>



INSTRUCTION TIMING <WRAL 256 x 16 organization>



DEVICE OPERATION

The CAT35C204H is a high endurance 4096 bit nonvolatile memory intended for use with all standard controllers. The CAT35C204H can be organized as either 256 registers by 16 bits, or as 512 registers by 8 bits. Six 13 bit instructions (14 bit instruction in 512 by 8 organization) control the reading, writing, and erase operations of the device. The CAT35C204H operates on a single 5V supply and will generate on chip the high voltage required during any programming operations. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normal in a high impedance state except when reading data from the device. The ready/busy status can be determined after a programming operation by polling the RDY/$\overline{\text{BUSY}}$ pin.

The format for all instructions sent to the CAT35C204H is one logical "1" start bit, a 4 bit op code, an 8 bit address (9 bit address when organized as 512 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 512 X 8).

READ

Upon receiving a READ command and address (clocked into the DI pin), the DO pin of the CAT35C204H will come out of the high impedance state. After sending 1 dummy zero bit the 16 bits (or 8 bits) of data located at the address location specified in the instruction will be shifted out. The data bit being shifted out will toggle on the rising edge of the CLK and becomes stable after the specified time delay (t_{PD1} and t_{PD0}).

ERASE/WRITE ENABLE AND DISABLE

The CAT35C204H powers up in the programming disable state. Any programming after power-up or after a PDS (programming disable) instruction must first be preceded by the PEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed or the PDS instruction is sent. The PDS instruction can be used to disable all the CAT35C204H's program and erase functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT35C204H regardless of the programming enable/disable status.

PROGRAM

After receiving a PROGRAM command, address, and the data, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking erase and data store cycle begins. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C204H can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin.

ERASE ALL

Upon receiving an ERAL command, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking erase sequence starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C204H can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin. Once erased, all memory bits return to logical "1" state.

WRITE ALL

Upon receiving a WRAL command and data, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking data store cycle starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT35C204H can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin. It **IS NOT** necessary for all memory locations to be erased before the WRAL command is executed.

CAT59C11
1K BIT SERIAL E^2PROM

Preliminary

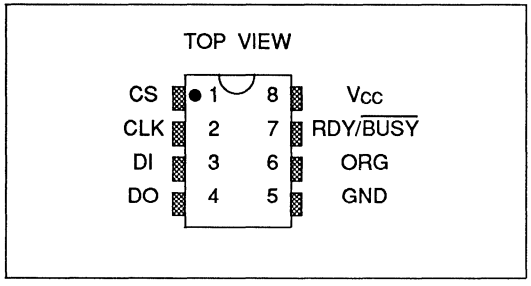
DESCRIPTION

The CAT59C11 is a 1K bit Serial E^2PROM memory device organized in 64 registers of 16 bits or 128 registers of 8 bits each. Each register can be written (or read) serially by using the DI (or DO) pin. The CAT59C11 is manufactured using Catalyst's advanced CMOS E^2PROM floating gate technology. It is designed to endure 10,000 erase/write cycles and has a data retention of 10 years. It is packaged in an 8-pin DIP and Small Outline packages. To be offered in a 3V version (CAT33C201).

FEATURES

- Highly reliable CMOS floating gate technology
- Single 5V supply
- 64x16 or 128x8 user selectable serial memory
- Compatible with General Instruments ER5911
- Self timed programming cycle with Autoerase
- Word and chip erasable
- Operating range 0°C to 70°C [industrial temp. range available]
- 100,000 erase/write cycles
- 100 year data retention
- Power-up inadvertent write protection

PIN CONFIGURATION

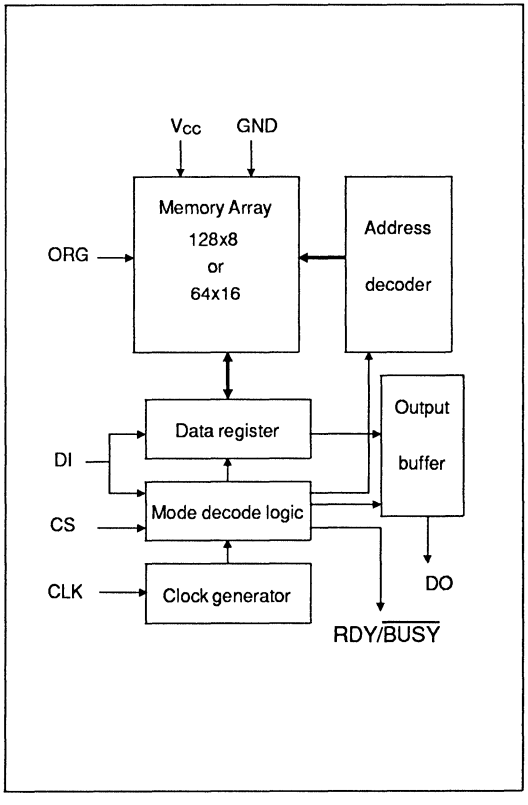


PIN FUNCTIONS

CS	Chip select
CLK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
RDY/BUSY	Status output
GND	Ground
ORG	Memory organization

Note: When the ORG pin is connected to Vcc, the 64x16 organization is selected. When it is connected to ground, the 128x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 64x16 organization.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature . . . . . -65°C to +150°C
Power supply (V_{CC}) . . . . . +7 V
Voltage on any input pin . . . . . -0.3 to +7V
Voltage on any output pin . . . . . -0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC1}	Current consumption (operating)	DI=0.0V, SK=5.5V V_{CC} =5.5V, CS = 5.5V DO unloaded			5	mA
I_{CC2}	Current consumption (stand-by)	V_{CC} = 5.5V, CS = 0 DI = 0, SK = 0			100	µA
I_{LI}	Input leakage current	V_{IN} = 5.5V			10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V, CS = 0			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V

INSTRUCTION SET

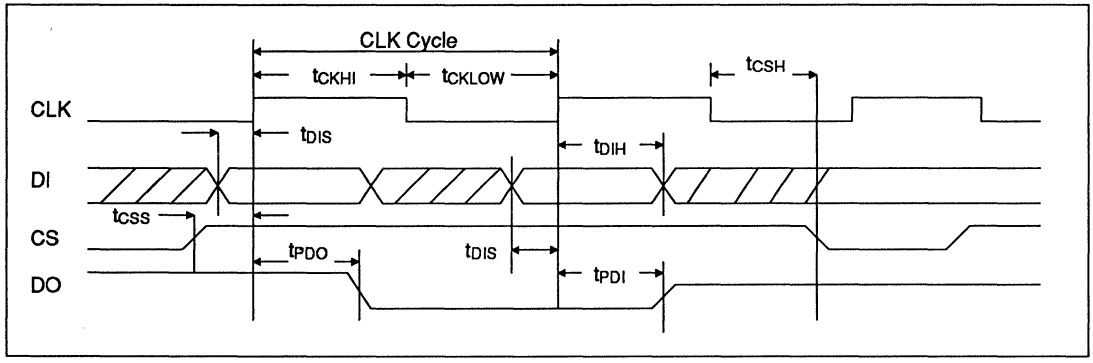
Instruction	Start Bit	Opcode	Address		Data		Comments
			128 x 8	64 x 16	128 x 8	64 x 16	
READ	1	1000	A_6 - A_0	A_5 - A_0			Read address A_N - A_0
PROGRAM	1	X100	A_6 - A_0	A_5 - A_0	D_7 - D_0	D_{15} - D_0	Program address A_N - A_0
PEN	1	0011	0000000	000000			Program enable
PDS	1	0000	0000000	000000			Program disable
ERAL	1	0010	0000000	000000			Erase all addresses
WRAL	1	0001	0000000	000000	D_7 - D_0	D_{15} - D_0	Write all addresses

AC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{CSS}	CS setup time		0.2			µs
t_{CSH}	CS hold time	C_L = 100pF V_{OL} = 0.8V, V_{OH} = 2.0V V_{IL} = 0.45V, V_{IH} = 2.4V	100			ns
t_{DIS}	DI setup time		0.4			µs
t_{DIH}	DI hold time		0.4			µs
t_{PD1}	Output delay to 1				2	µs
t_{PD0}	Output delay to 0				2	µs
t_{EW}	Erase/Write pulse width				10	ms
t_{SKHI}	Minimum SK high time		1			µs
t_{SKLOW}	Minimum SK low time		1			µs
CK_{MAX}	Maximum clock frequency		DC		250	kHz

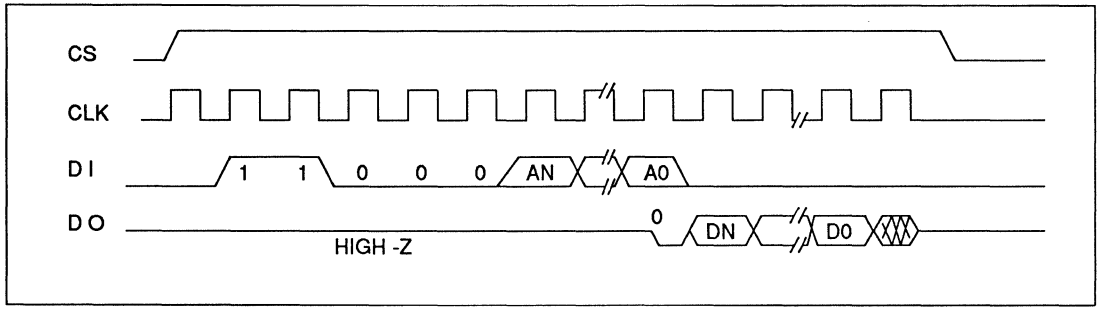
SYNCHRONOUS TIMINGS



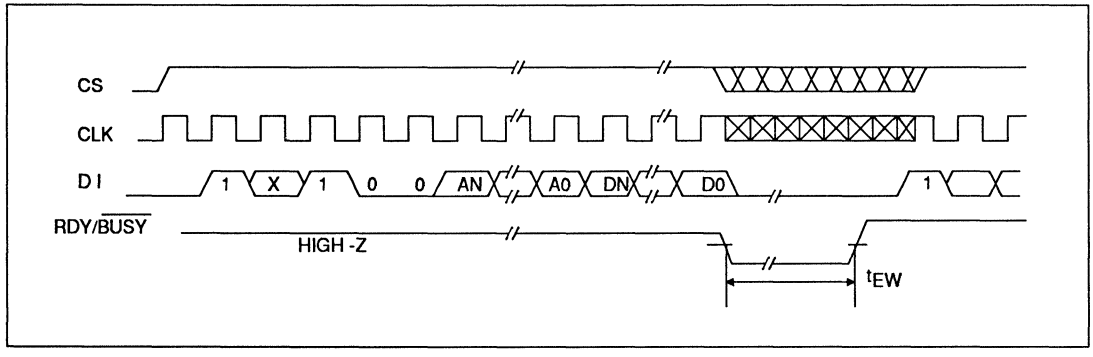
INSTRUCTION TIMING <ORGANIZATION>

Organization	A_N (or AN)	D_N (or DN)
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

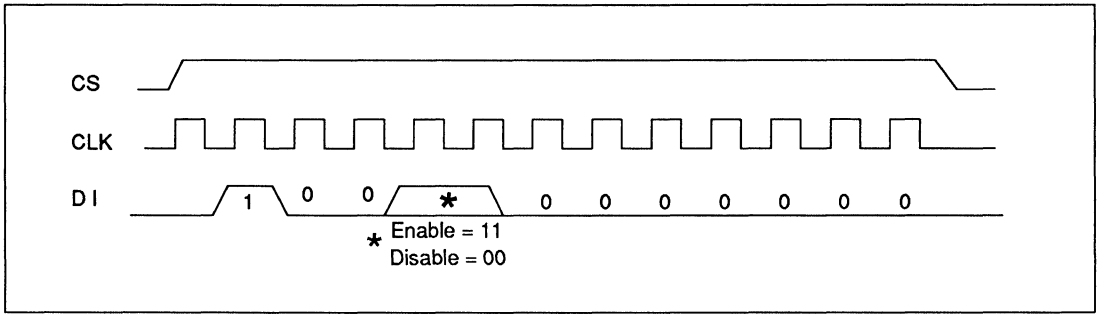
INSTRUCTION TIMING <READ>



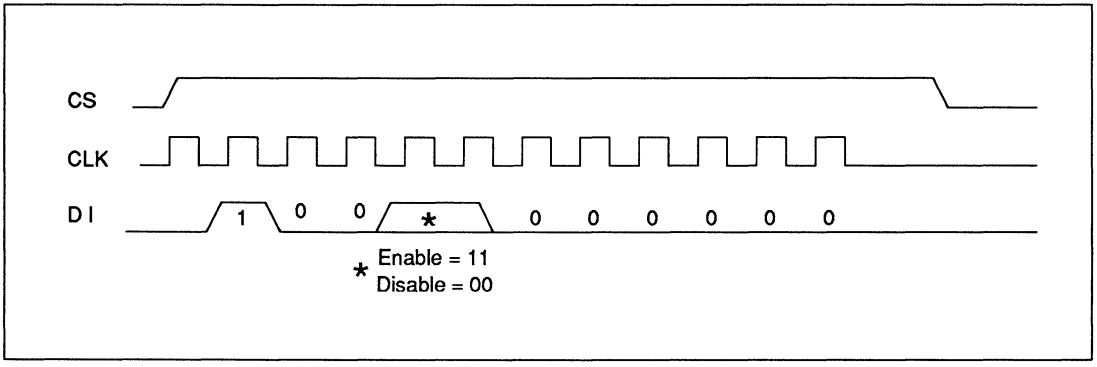
INSTRUCTION TIMING <PROGRAM>



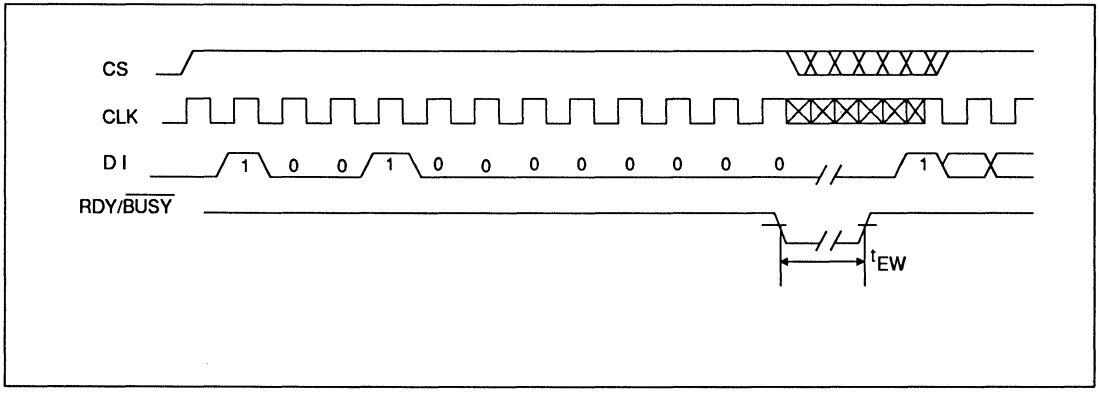
INSTRUCTION TIMING <PEN, PDS 128 x 8 organization>



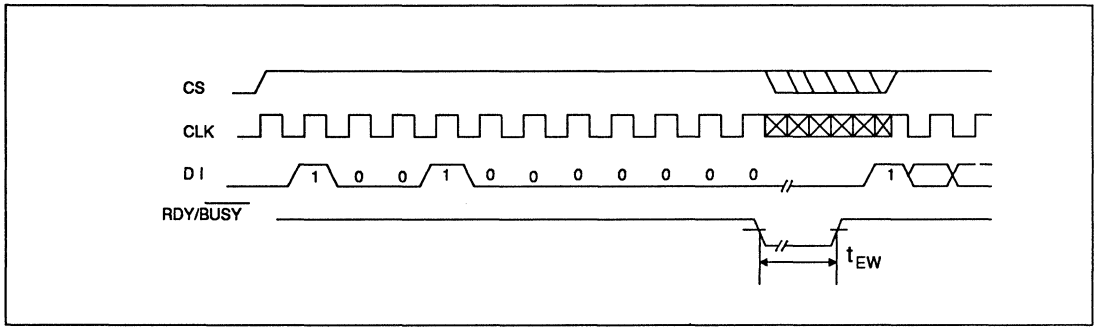
INSTRUCTION TIMING <PEN, PDS 64 x 16 organization>



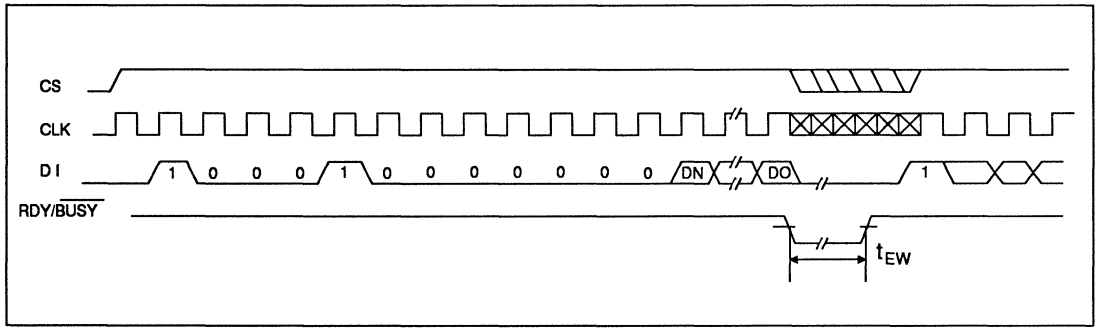
INSTRUCTION TIMING <ERAL 128 x 8 organization>



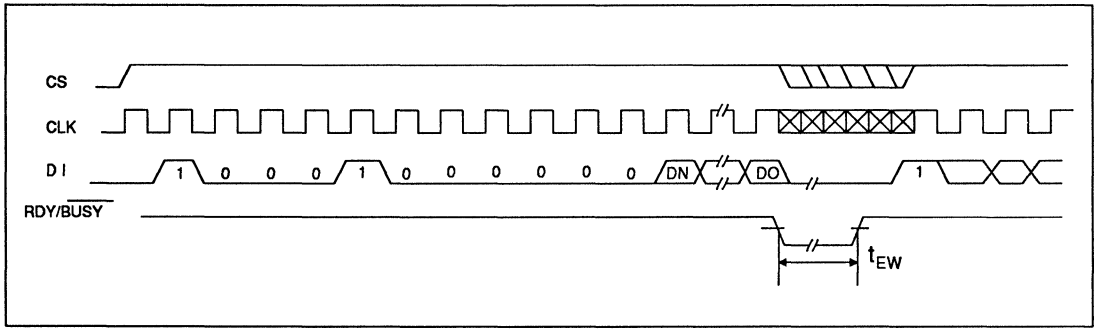
INSTRUCTION TIMING <ERAL 64 x 16 organization>



INSTRUCTION TIMING <WRAL 128 x 8 organization>



INSTRUCTION TIMING <WRAL 64 x 16 organization>



DEVICE OPERATION

The CAT59C11 is a 1024 bit nonvolatile memory intended for use with all standard controllers. The CAT59C11 can be organized as either 64 registers by 16 bits, or as 128 registers by 8 bits. Six 11 bit instructions (12 bit instruction in 128 by 8 organization) control the reading, writing, and erase operations of the device. The CAT59C11 operates on a single 5V supply and will generate on chip the high voltage required during any programming operations. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normal in a high impedance state except when reading data from the device. The ready/busy status can be determined after a programming operation by polling the RDY/BUSY pin.

The format for all instructions sent to the CAT59C11 is one logical "1" start bit, a 4 bit op code, a 6 bit address (7 bit address when organized as 128 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 128 X 8).

READ

Upon receiving a READ command and address (clocked into the DI pin), the DO pin of the CAT59C11 will come out of the high impedance state. After sending 1 dummy zero bit the 16 bits (or 8 bits) of data located at the address location specified in the instruction will be shifted out. The data bit being shifted out will toggle on the rising edge of the CLK and is stable after the specified time delay (t_{PD1} and t_{PD0}).

ERASE/WRITE ENABLE AND DISABLE

The CAT59C11 powers up in the programming disable state. Any programming after power-up or after a PDS (programming disable) instruction must first be preceded by the PEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed or the PDS instruction is sent. The PDS instruction can be used to disable all the CAT59C11's program and erase functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT59C11 regardless of the programming enable/disable status.

PROGRAM

After receiving a PROGRAM command, address, and the data, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking erase and data store cycle begins. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT59C11 can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin.

ERASE ALL

Upon receiving an ERAL command, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking erase sequence starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT59C11 can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin.

WRITE ALL

Upon receiving a WRAL command and data, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking data store cycle starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT59C11 can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin. It **IS** necessary for all memory locations to be erased before the WRAL command is executed.

CAT59C11A
1K BIT SERIAL E²PROM

Preliminary

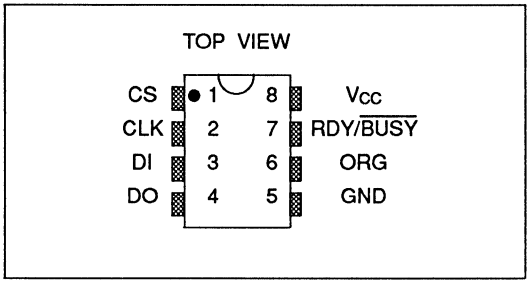
DESCRIPTION

The CAT59C11A is a 1K bit Serial E²PROM memory device organized in 64 registers of 16 bits or 128 registers of 8 bits each. Each register can be written (or read) serially by using the DI (or DO) pin. The CAT59C11A is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 10,000 erase/write cycles and has a data retention of 10 years. It is packaged in an 8-pin DIP and Small Outline packages. To be offered in a 3V version (CAT33C201).

FEATURES

- Highly reliable CMOS floating gate technology
- Single 5V supply
- 64x16 or 128x8 user selectable serial memory
- Compatible with General Instruments ER5911
- Self timed programming cycle with Autoerase
- Word and chip erasable
- Operating range 0°C to 70°C [industrial temp. range available]
- 10,000 erase/write cycles
- 10 year data retention
- Power-up inadvertent write protection

PIN CONFIGURATION

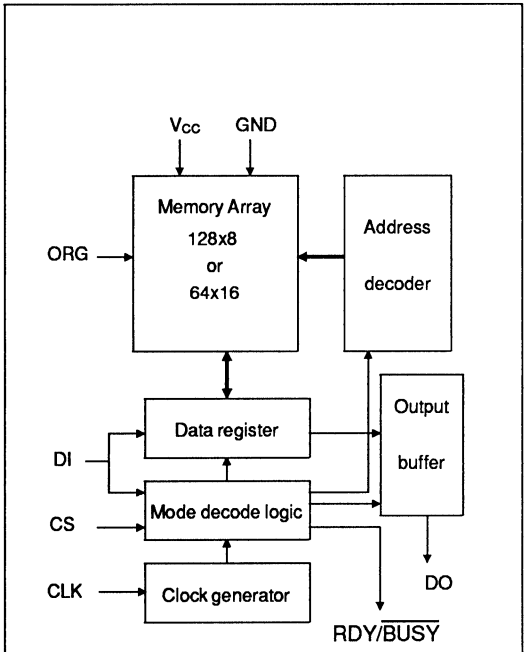


PIN FUNCTIONS

CS	Chip select
CLK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
RDY/$\overline{\text{BUSY}}$	Status output
GND	Ground
ORG	Memory organization

Note: When the ORG pin is connected to Vcc, the 64x16 organization is selected. When it is connected to ground, the 128x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 64x16 organization.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature . . . . . -65°C to +150°C
Power supply (V_{CC}) . . . . . +7 V
Voltage on any input pin . . . . . -0.3 to +7V
Voltage on any output pin . . . . . -0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC1}	Current consumption (operating)	DI=0.0V, SK=5.5V V_{CC} =5.5V, CS = 5.5V DO unloaded			3	mA
I_{CC2}	Current consumption (standby)	V_{CC} = 5.5V, CS = 0 DI = 0, SK = 0			100	µA
I_{LI}	Input leakage current	V_{IN} = 5.5V			10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V, CS = 0			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V

INSTRUCTION SET

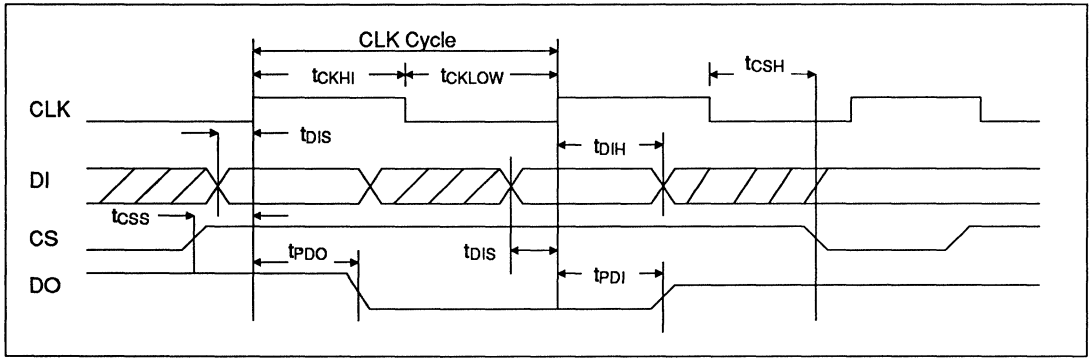
Instruction	Start Bit	Opcode	Address		Data		Comments
			128 x 8	64 x 16	128 x 8	64 x 16	
READ	1	1000	A_6 - A_0	A_5 - A_0			Read address A_N - A_0
PROGRAM	1	X100	A_6 - A_0	A_5 - A_0	D_7 - D_0	D_{15} - D_0	Program address A_N - A_0
PEN	1	0011	0000000	000000			Program enable
PDS	1	0000	0000000	000000			Program disable
ERAL	1	0010	0000000	000000			Erase all addresses
WRAL	1	0001	0000000	000000	D_7 - D_0	D_{15} - D_0	Write all addresses

AC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{CSS}	CS setup time		0.2			µs
t_{CSH}	CS hold time	C_L = 100pF V_{OL} = 0.8V, V_{OH} = 2.0V V_{IL} = 0.45V, V_{IH} = 2.4V	100			ns
t_{DIS}	DI setup time		0.4			µs
t_{DIH}	DI hold time		0.4			µs
t_{PD1}	Output delay to 1				2	µs
t_{PD0}	Output delay to 0				2	µs
t_{EW}	Erase/Write pulse width				10	ms
t_{SKHI}	Minimum SK high time		1			µs
t_{SKLOW}	Minimum SK low time		1			µs
CK_{MAX}	Maximum clock frequency		DC		250	kHz

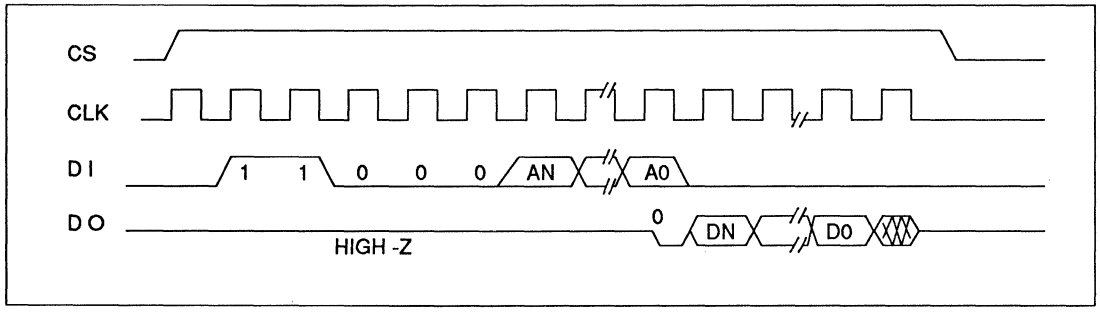
SYNCHRONOUS TIMINGS



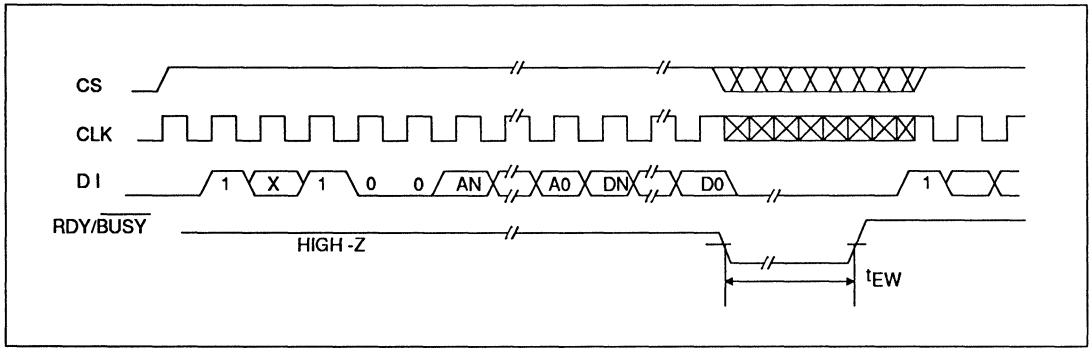
INSTRUCTION TIMING <ORGANIZATION>

Organization	A_N (or AN)	D_N (or DN)
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

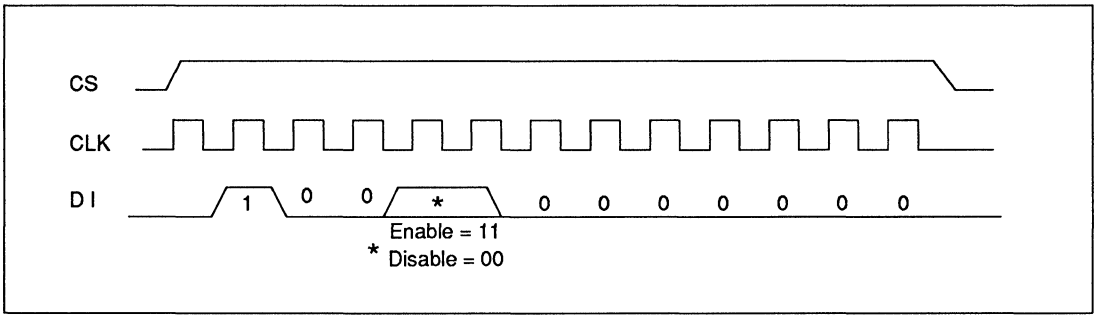
INSTRUCTION TIMING <READ>



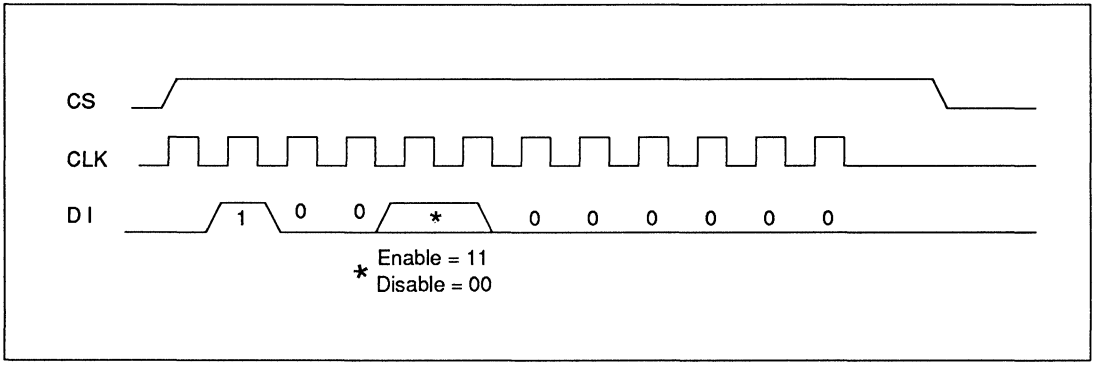
INSTRUCTION TIMING <PROGRAM>



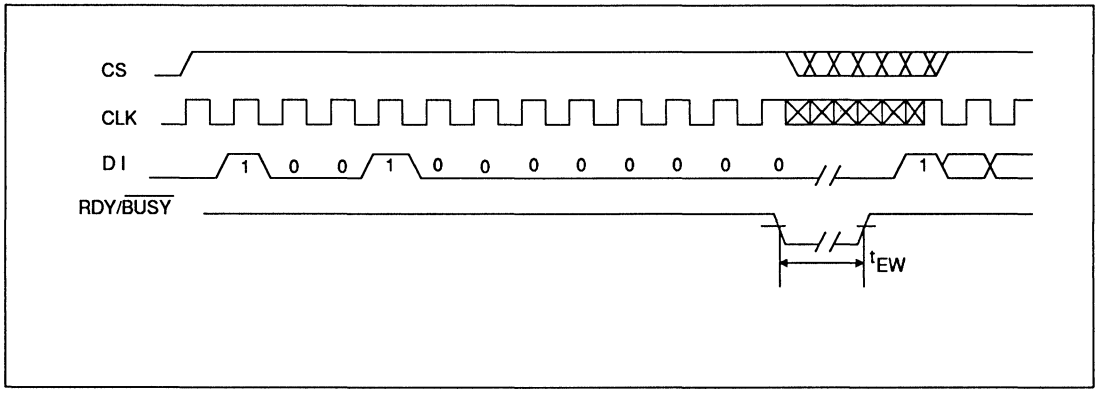
INSTRUCTION TIMING <PEN, PDS 128 x 8 organization>



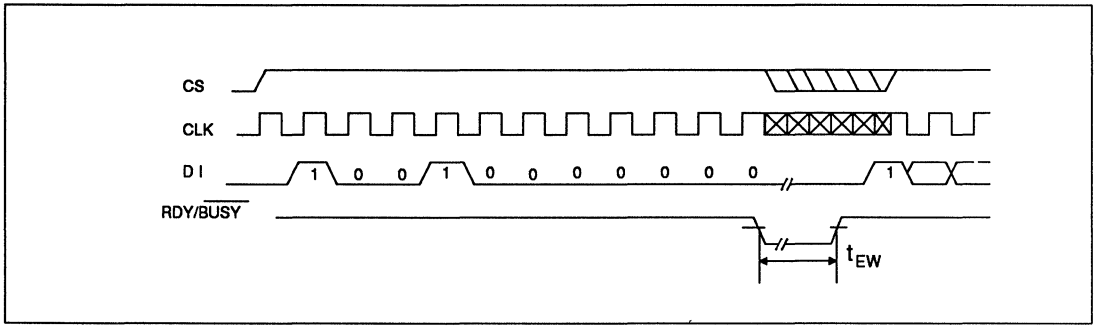
INSTRUCTION TIMING <PEN, PDS 64 x 16 organization>



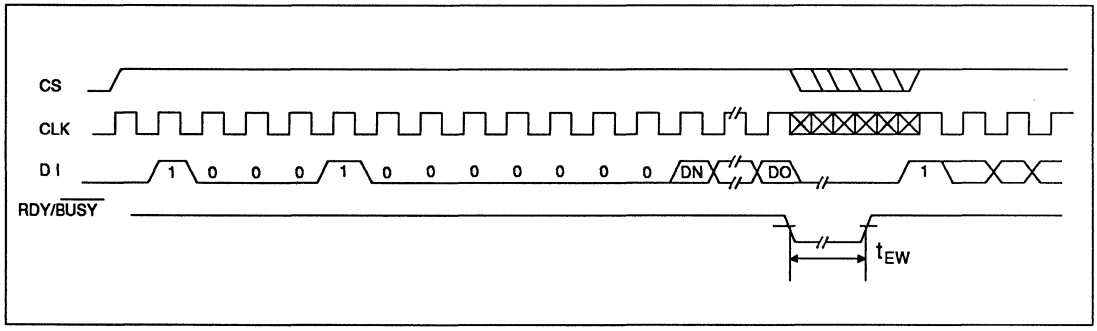
INSTRUCTION TIMING <ERAL 128 x 8 organization>



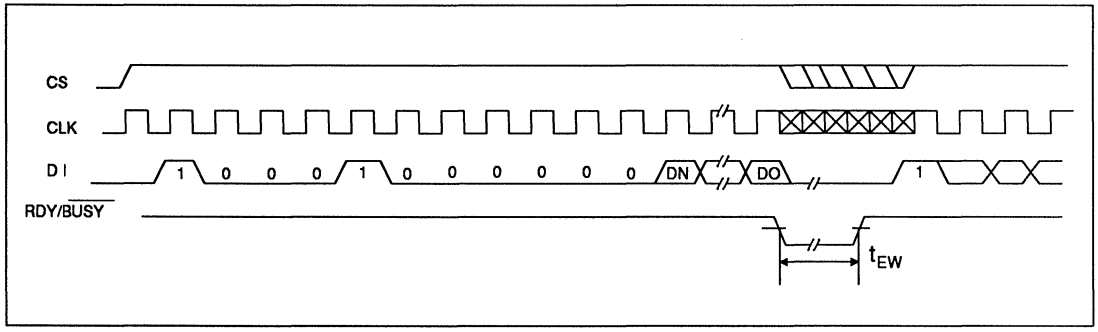
INSTRUCTION TIMING <ERAL 64 x 16 organization>



INSTRUCTION TIMING <WRAL 128 x 8 organization>



INSTRUCTION TIMING <WRAL 64 x 16 organization>



DEVICE OPERATION

The CAT59C11A is a 1024 bit nonvolatile memory intended for use with all standard controllers. The CAT59C11A can be organized as either 64 registers by 16 bits, or as 128 registers by 8 bits. Six 11 bit instructions (12 bit instruction in 128 by 8 organization) control the reading, writing, and erase operations of the device. The CAT59C11A operates on a single 5V supply and will generate on chip the high voltage required during any programming operations. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normal in a high impedance state except when reading data from the device. The ready/busy status can be determined after a programming operation by polling the RDY/BUSY pin.

The format for all instructions sent to the CAT59C11A is one logical "1" start bit, a 4 bit op code, a 6 bit address (7 bit address when organized as 128 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 128 X 8).

READ

Upon receiving a READ command and address (clocked into the DI pin), the DO pin of the CAT59C11A will come out of the high impedance state. After sending 1 dummy zero bit the 16 bits (or 8 bits) of data located at the address location specified in the instruction will be shifted out. The data bit being shifted out will toggle on the rising edge of the CLK and is stable after the specified time delay (t_{PD1} and t_{PD0}).

ERASE/WRITE ENABLE AND DISABLE

The CAT59C11A powers up in the programming disable state. Any programming after power-up or after a PDS (programming disable) instruction must first be preceded by the PEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed or the PDS instruction is sent. The PDS instruction can be used to disable all the CAT59C11A's program and erase functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT59C11A regardless of the programming enable/disable status.

PROGRAM

After receiving a PROGRAM command, address, and the data, the RDY/BUSY pin goes low and the self clocking erase and data store cycle begins. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT59C11A can be determined by polling the RDY/BUSY pin.

ERASE ALL

Upon receiving an ERAL command, the RDY/BUSY pin goes low and the self clocking erase sequence starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT59C11A can be determined by polling the RDY/BUSY pin.

WRITE ALL

Upon receiving a WRAL command and data, the RDY/BUSY pin goes low and the self clocking data store cycle starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT59C11A can be determined by polling the RDY/BUSY pin. It **IS** necessary for all memory locations to be erased before the WRAL command is executed.

CAT59C11H - High Endurance
1K BIT SERIAL E^2PROM

Preliminary

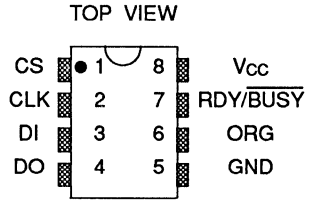
DESCRIPTION

The CAT59C11H is a high endurance 1K bit Serial E^2PROM memory device organized in 64 registers of 16 bits or 128 registers of 8 bits each. Each register can be written (or read) serially by using the DI (or DO) pin. The CAT59C11H is manufactured using Catalyst's advanced CMOS E^2PROM floating gate technology. It is designed to endure 100,000 erase/write cycles and has a data retention of 100 years. It is packaged in an 8-pin DIP and Small Outline packages. To be offered in a 3V version (CAT33C201H).

FEATURES

- Highly reliable CMOS floating gate technology
- Single 5V supply
- 64x16 or 128x8 user selectable serial memory
- Compatible with General Instruments ER5911
- Self timed programming cycle with Autoerase
- Word and chip erasable
- Operating range 0°C to 70°C
- 100,000 erase/write cycles
- 100 year data retention
- Power-up inadvertent write protection

PIN CONFIGURATION

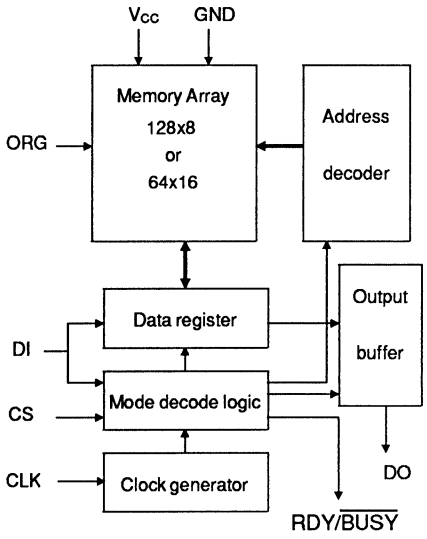


PIN FUNCTIONS

CS	Chip select
CLK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
RDY/$\overline{\text{BUSY}}$	Status output
GND	Ground
ORG	Memory organization

Note: When the ORG pin is connected to Vcc, the 64x16 organization is selected. When it is connected to ground, the 128x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 64x16 organization.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature . . . . . -65°C to +150°C
Power supply (V_{CC}) . . . . . +7V
Voltage on any input pin . . . . . -0.3 to +7V
Voltage on any output pin . . . . . -0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC1}	Current consumption (operating)	DI=0.0V, SK=5.5V V_{CC} =5.5V, CS = 5.5V DO unloaded			5	mA
I_{CC2}	Current consumption (standby)	V_{CC} = 5.5V, CS = 0 DI = 0, SK = 0			100	µA
I_{LI}	Input leakage current	V_{IN} = 5.5V			10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V, CS = 0			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V

INSTRUCTION SET

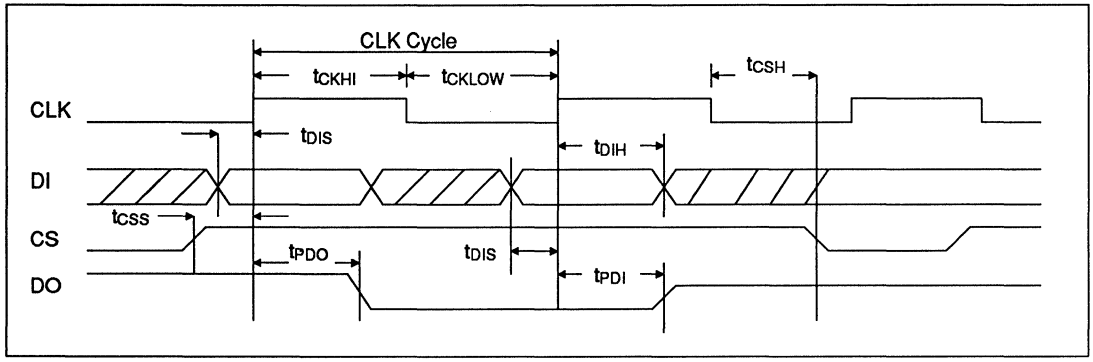
Instruction	Start Bit	Opcode	Address		Data		Comments
			128 x 8	64 x 16	128 x 8	64 x 16	
READ	1	1000	A_6 - A_0	A_5 - A_0			Read address A_N - A_0
PROGRAM	1	X100	A_6 - A_0	A_5 - A_0	D_7 - D_0	D_{15} - D_0	Program address A_N - A_0
PEN	1	0011	0000000	000000			Program enable
PDS	1	0000	0000000	000000			Program disable
ERAL	1	0010	0000000	000000			Erase all addresses
WRAL	1	0001	0000000	000000	D_7 - D_0	D_{15} - D_0	Write all addresses

AC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{CSS}	CS setup time		0.2			µs
t_{CSH}	CS hold time	C_L = 100pF V_{OL} = 0.8V, V_{OH} = 2.0V V_{IL} = 0.45V, V_{IH} = 2.4V	100			ns
t_{DIS}	DI setup time		0.4			µs
t_{DIH}	DI hold time		0.4			µs
t_{PD1}	Output delay to 1				2	µs
t_{PD0}	Output delay to 0				2	µs
t_{EW}	Erase/Write pulse width				10	ms
t_{SKHI}	Minimum SK high time		1			µs
t_{SKLOW}	Minimum SK low time		1			µs
CK_{MAX}	Maximum clock frequency		DC		250	kHz

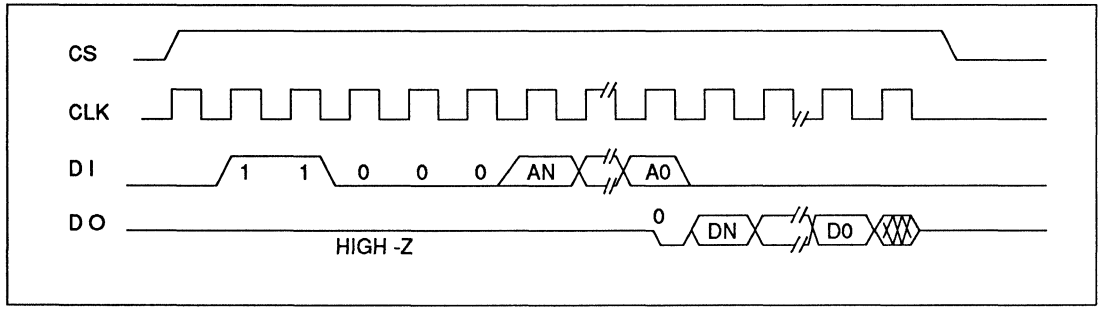
SYNCHRONOUS TIMINGS



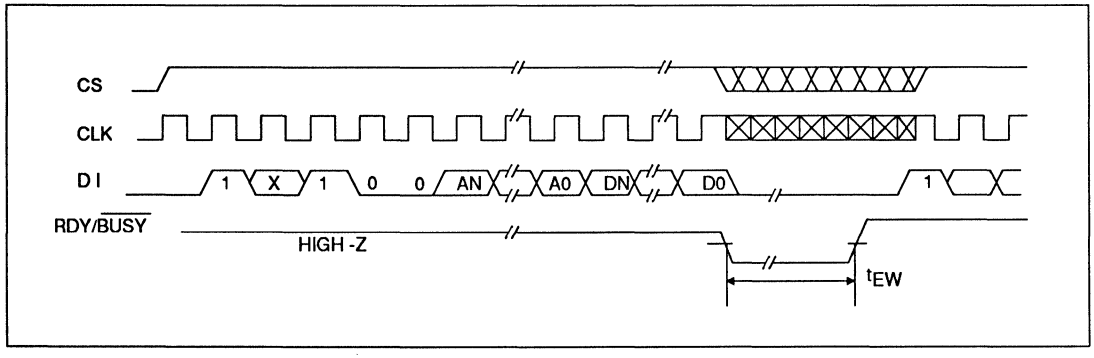
INSTRUCTION TIMING <ORGANIZATION>

Organization	A_N (or AN)	D_N (or DN)
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

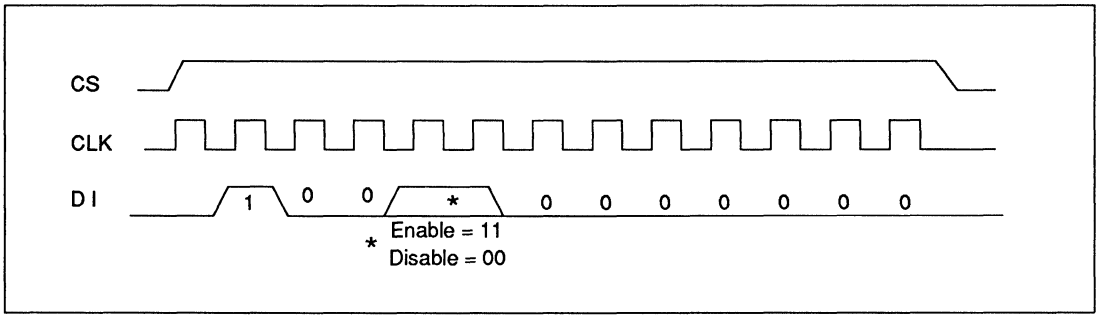
INSTRUCTION TIMING <READ>



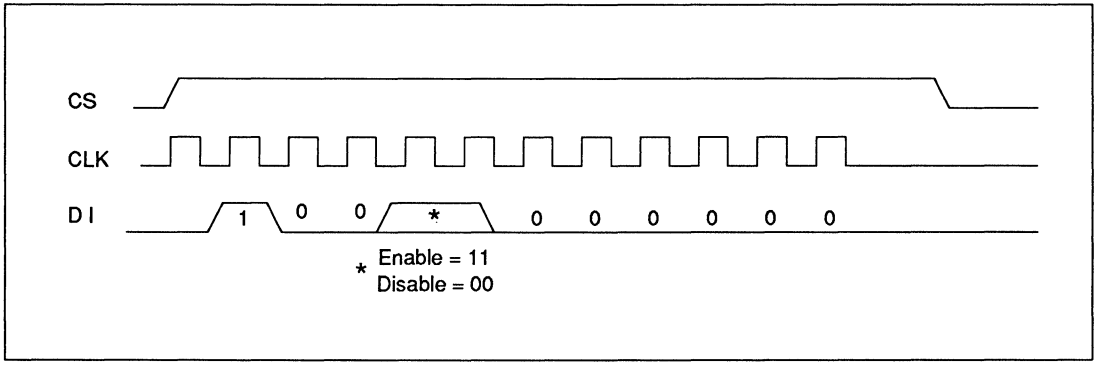
INSTRUCTION TIMING <PROGRAM>



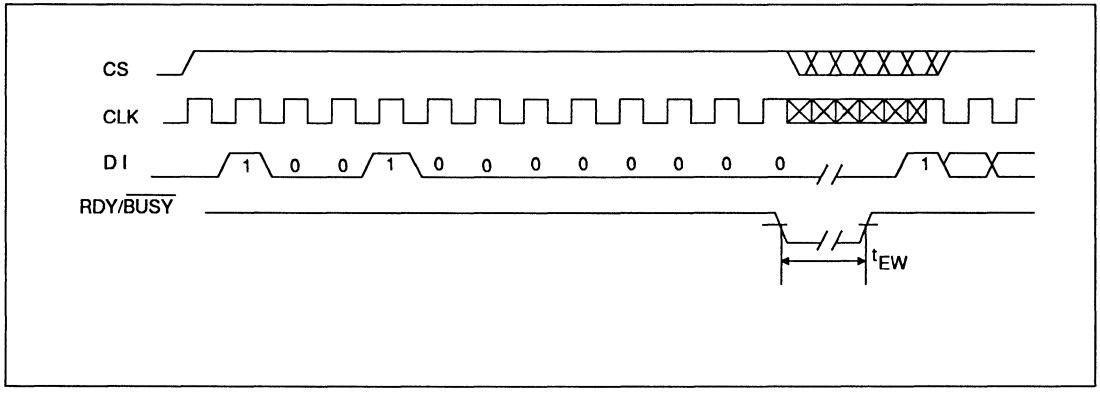
INSTRUCTION TIMING <PEN, PDS 128 x 8 organization>



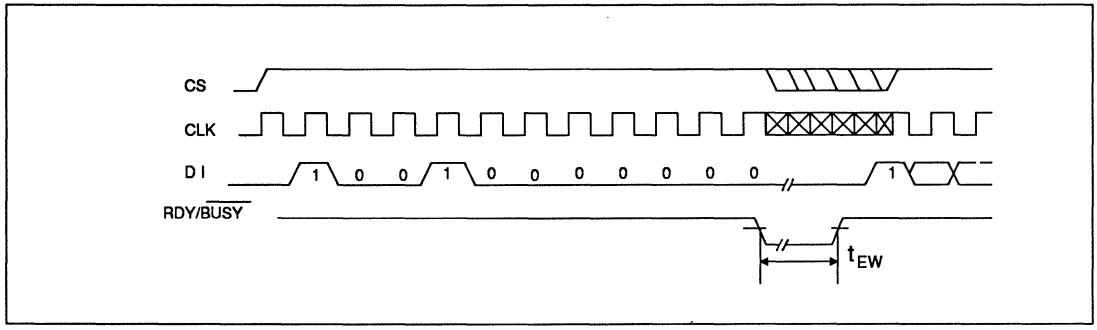
INSTRUCTION TIMING <PEN, PDS 64 x 16 organization>



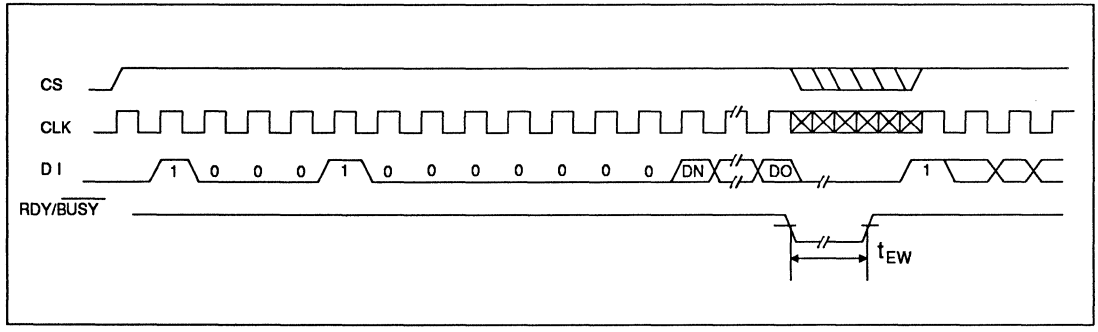
INSTRUCTION TIMING <ERAL 128 x 8 organization>



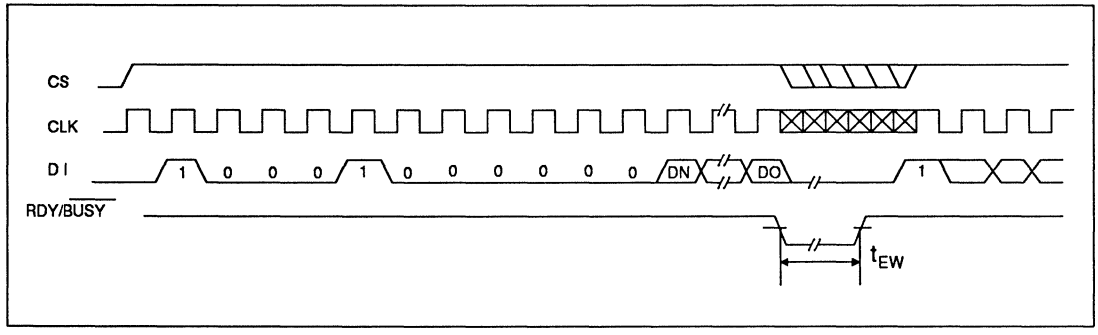
INSTRUCTION TIMING <ERAL 64 x 16 organization>



INSTRUCTION TIMING <WRAL 128 x 8 organization>



INSTRUCTION TIMING <WRAL 64 x 16 organization>



DEVICE OPERATION

The CAT59C11H is a high endurance 1024 bit non-volatile memory intended for use with all standard controllers. The CAT59C11H can be organized as either 64 registers by 16 bits, or as 128 registers by 8 bits. Six 11 bit instructions (12 bit instruction in 128 by 8 organization) control the reading, writing, and erase operations of the device. The CAT59C11H operates on a single 5 Volt supply and will generate on chip the high voltage required during any programming operations. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normal in a high impedance state except when reading data from the device. The ready/busy status can be determined after a programming operation by polling the RDY/BUSY pin.

The format for all instructions sent to the CAT59C11H is one logical "1" start bit, a 4 bit op code, a 6 bit address (7 bit address when organized as 128 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 128 X 8).

READ

Upon receiving a READ command and address (clocked into the DI pin), the DO pin of the CAT59C11H will come out of the high impedance state. After sending 1 dummy zero bit the 16 bits (or 8 bits) of data located at the address location specified in the instruction will be shifted out. The data bit being shifted out will toggle on the rising edge of the CLK and is stable after the specified time delay (t_{PD1} and t_{PD0}).

ERASE/WRITE ENABLE AND DISABLE

The CAT59C11H powers up in the programming disable state. Any programming after power-up or after a PDS (programming disable) instruction must first be preceded by the PEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed or the PDS instruction is sent. The PDS instruction can be used to disable all the CAT59C11H's program and erase functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT59C11H regardless of the programming enable/disable status.

PROGRAM

After receiving a PROGRAM command, address, and the data, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking erase and data store cycle begins. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT59C11H can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin.

ERASE ALL

Upon receiving an ERAL command, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking erase sequence starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT59C11H can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin.

WRITE ALL

Upon receiving a WRAL command and data, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking data store cycle starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT59C11H can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin. It **IS** necessary for all memory locations to be erased before the WRAL command is executed.

CAT59C11I - Industrial Temperature
1K BIT SERIAL E^{2}PROM

Preliminary

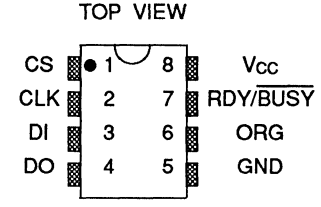
DESCRIPTION

The CAT59C11I is a 1K bit Serial E^{2}PROM memory device organized in 64 registers of 16 bits or 128 registers of 8 bits each. Each register can be written (or read) serially by using the DI (or DO) pin. The CAT59C11I is manufactured using Catalyst's advanced CMOS E^{2}PROM floating gate technology. It is designed to endure 10,000 erase/write cycles and has a data retention of 10 years. It is packaged in an 8-pin DIP and Small Outline packages. To be offered in a 3V version (CAT33C201).

FEATURES

- Highly reliable CMOS floating gate technology
- Single 5V supply
- 64x16 or 128x8 user selectable serial memory
- Compatible with General Instruments ER5911
- Self timed programming cycle with Autoerase
- Word and chip erasable
- Operating range -40°C to +85°C
- 10,000 erase/write cycles
- 10 year data retention
- Power-up inadvertent write protection

PIN CONFIGURATION

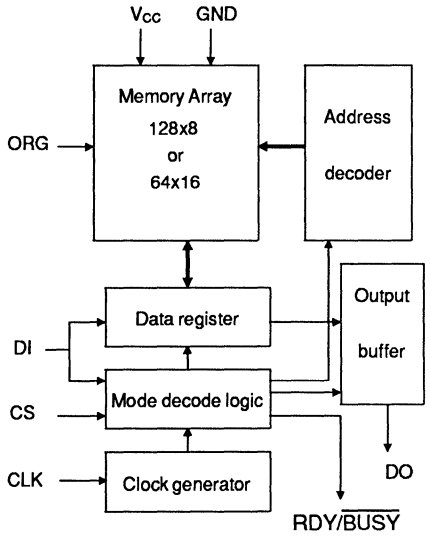


PIN FUNCTIONS

CS	Chip select
CLK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
RDY/BUSY	Status output
GND	Ground
ORG	Memory organization

Note: When the ORG pin is connected to Vcc, the 64x16 organization is selected. When it is connected to ground, the 128x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 64x16 organization.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature . . . . . -65°C to +150°C
Power supply (V_{CC}) . . . . . +7V
Voltage on any input pin . . . . . -0.3 to +7V
Voltage on any output pin . . . . . -0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC1}	Current consumption (operating)	DI=0.0V, SK=5.5V V_{CC} =5.5V, CS = 5.5V DO unloaded			5	mA
I_{CC2}	Current consumption (stand-by)	V_{CC} = 5.5V, CS = 0 DI = 0, SK = 0			100	µA
I_{LI}	Input leakage current	V_{IN} = 5.5V			10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V, CS = 0			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V

INSTRUCTION SET

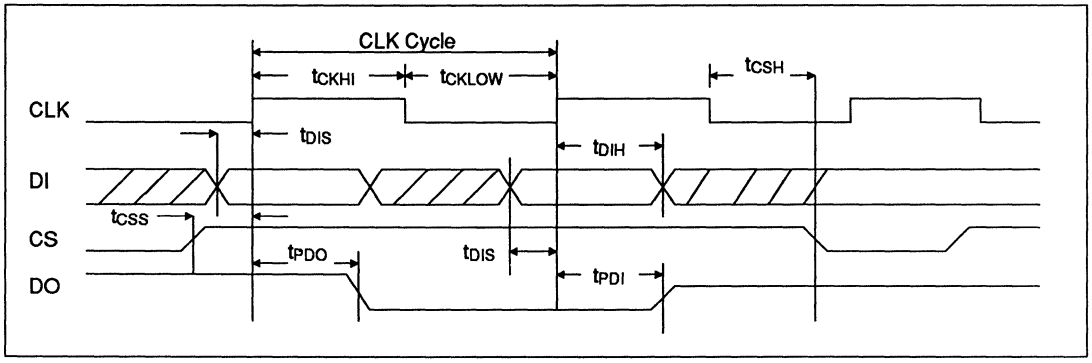
Instruction	Start Bit	Opcode	Address		Data		Comments
			128 x 8	64 x 16	128 x 8	64 x 16	
READ	1	1000	A_6 - A_0	A_5 - A_0			Read address A_N - A_0
PROGRAM	1	X100	A_6 - A_0	A_5 - A_0	D_7 - D_0	D_{15} - D_0	Program address A_N - A_0
PEN	1	0011	0000000	000000			Program enable
PDS	1	0000	0000000	000000			Program disable
ERAL	1	0010	0000000	000000			Erase all addresses
WRAL	1	0001	0000000	000000	D_7 - D_0	D_{15} - D_0	Write all addresses

AC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{CSS}	CS setup time		0.2			µs
t_{CSH}	CS hold time	C_L = 100pF V_{OL} = 0.8V, V_{OH} = 2.0V V_{IL} = 0.45V, V_{IH} = 2.4V	100			ns
t_{DIS}	DI setup time		0.4			µs
t_{DIH}	DI hold time		0.4			µs
t_{PD1}	Output delay to 1				2	µs
t_{PD0}	Output delay to 0				2	µs
t_{EW}	Erase/Write pulse width				10	ms
t_{SKHI}	Minimum SK high time		1			µs
t_{SKLOW}	Minimum SK low time		1			µs
CK_{MAX}	Maximum clock frequency		DC		250	kHz

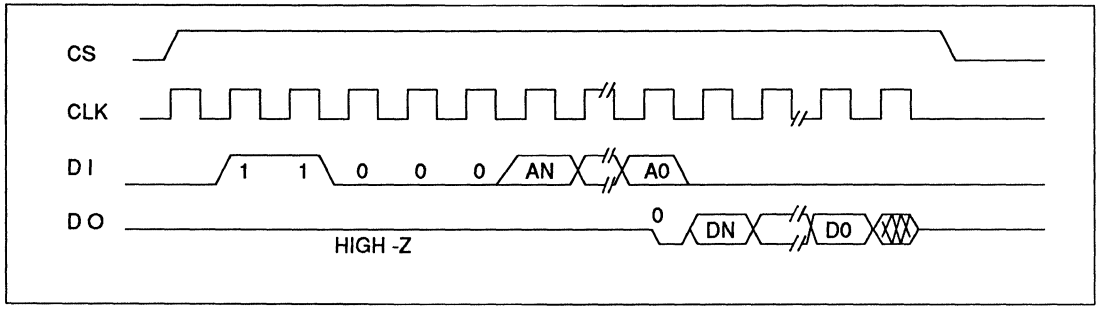
SYNCHRONOUS TIMINGS



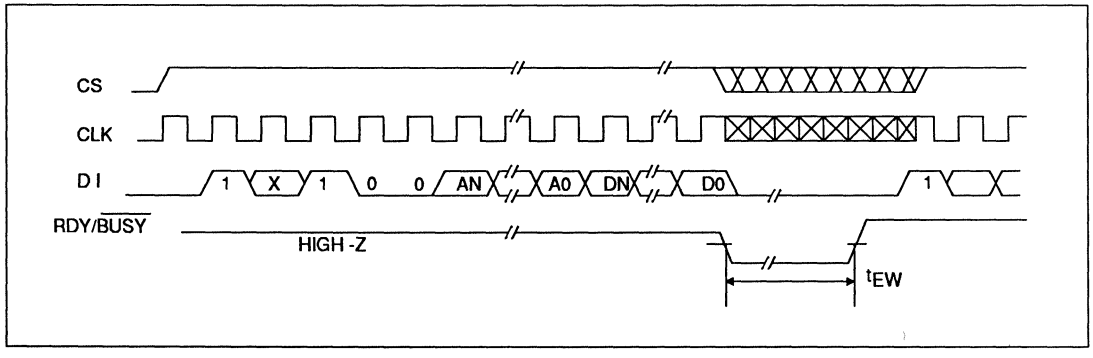
INSTRUCTION TIMING <ORGANIZATION>

Organization	A_N (or AN)	D_N (or DN)
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

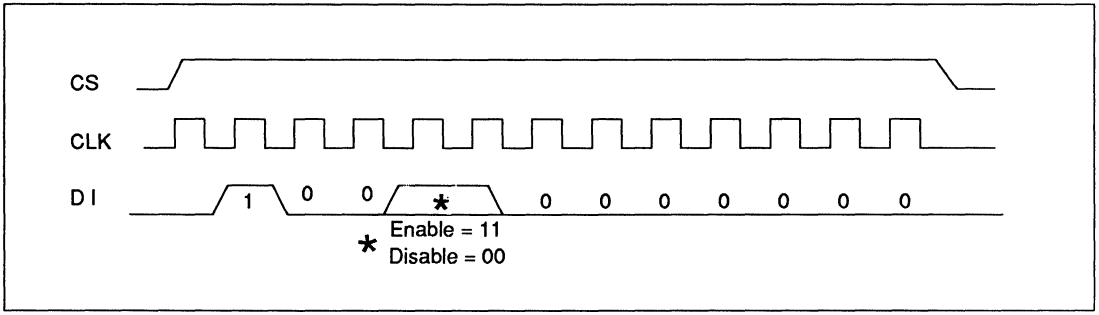
INSTRUCTION TIMING <READ>



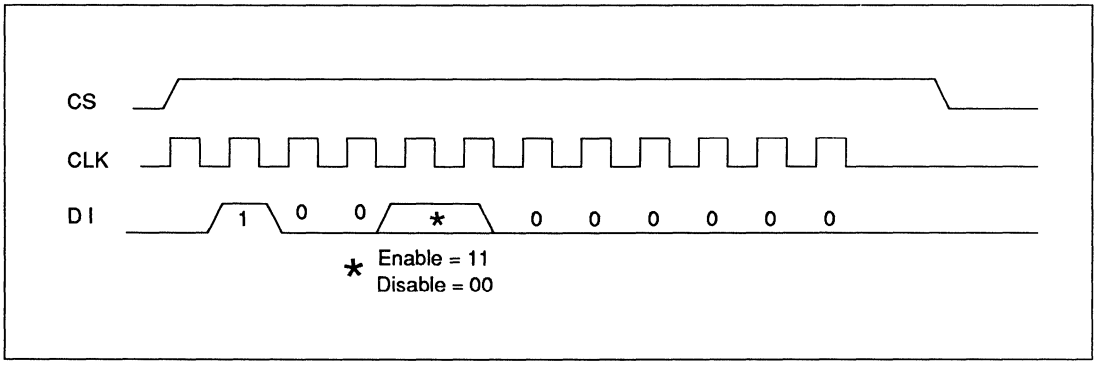
INSTRUCTION TIMING <PROGRAM>



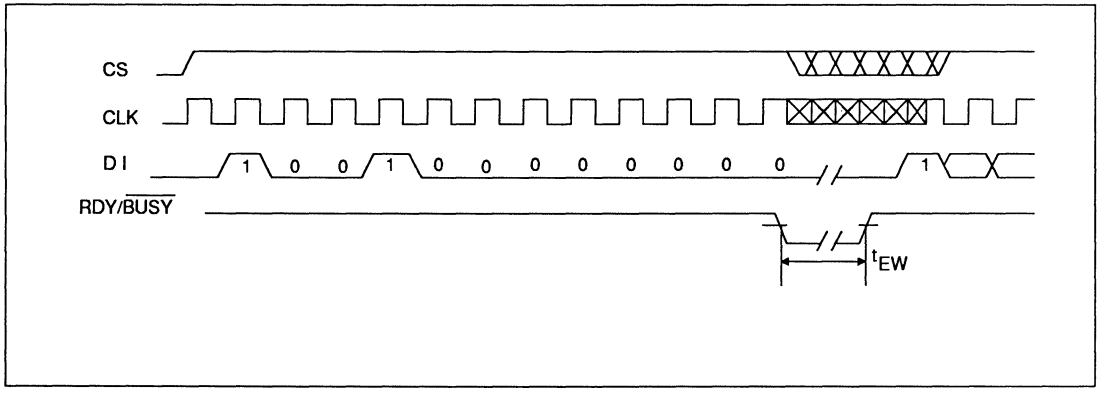
INSTRUCTION TIMING <PEN, PDS 128 x 8 organization>



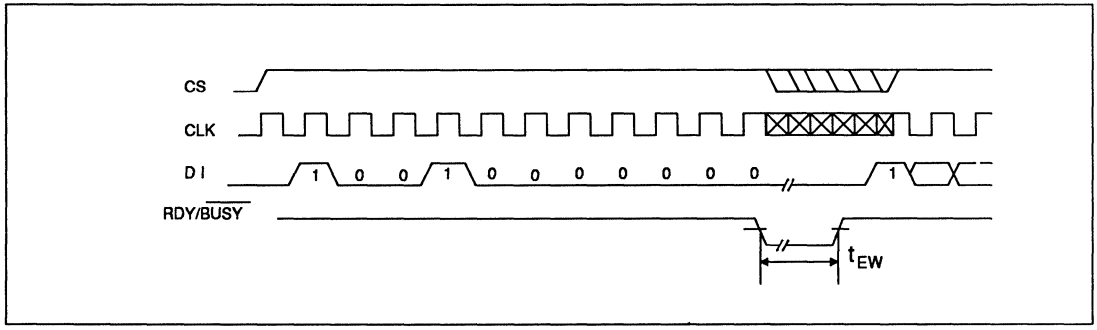
INSTRUCTION TIMING <PEN, PDS 64 x 16 organization>



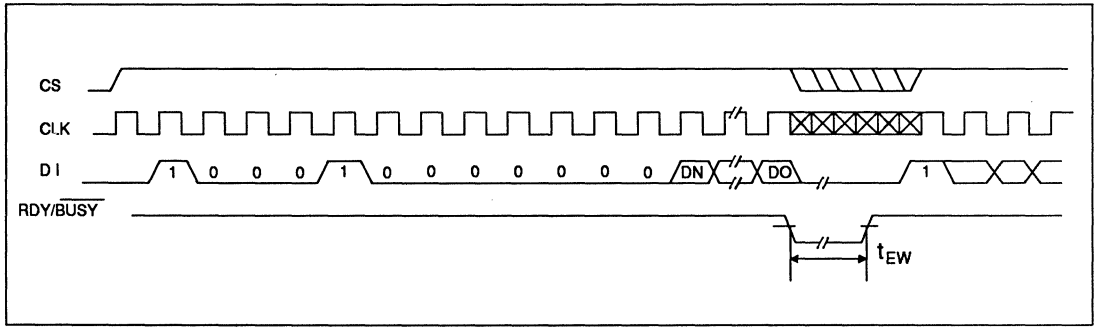
INSTRUCTION TIMING <ERAL 128 x 8 organization>



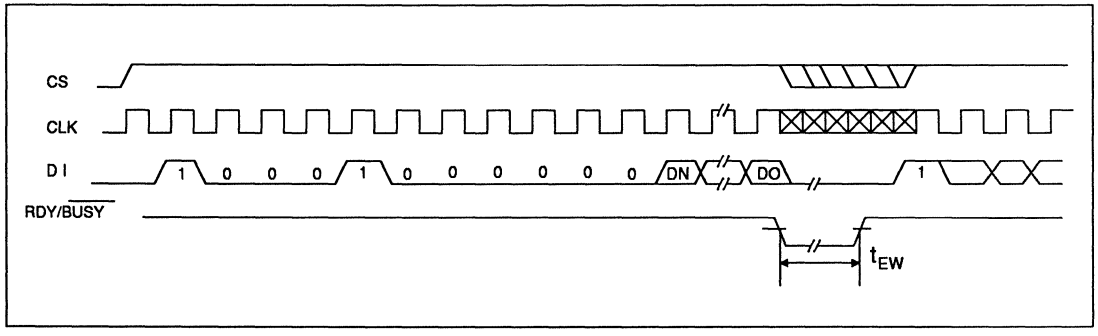
INSTRUCTION TIMING <ERAL 64 x 16 organization>



INSTRUCTION TIMING <WRAL 128 x 8 organization>



INSTRUCTION TIMING <WRAL 64 x 16 organization>



DEVICE OPERATION

The CAT59C11I is a 1024 bit nonvolatile memory intended for use with all standard controllers. The CAT59C11I can be organized as either 64 registers by 16 bits, or as 128 registers by 8 bits. Six 11 bit instructions (12 bit instruction in 128 by 8 organization) control the reading, writing, and erase operations of the device. The CAT59C11I operates on a single 5V supply and will generate on chip the high voltage required during any programming operations. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normal in a high impedance state except when reading data from the device. The ready/busy status can be determined after a programming operation by polling the RDY/$\overline{\text{BUSY}}$ pin.

The format for all instructions sent to the CAT59C11I is one logical "1" start bit, a 4 bit op code, a 6 bit address (7 bit address when organized as 128 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 128 X 8).

READ

Upon receiving a READ command and address (clocked into the DI pin), the DO pin of the CAT59C11I will come out of the high impedance state. After sending 1 dummy zero bit the 16 bits (or 8 bits) of data located at the address location specified in the instruction will be shifted out. The data bit being shifted out will toggle on the rising edge of the CLK and is stable after the specified time delay (t_{PD1} and t_{PD0}).

ERASE/WRITE ENABLE AND DISABLE

The CAT59C11I powers up in the programming disable state. Any programming after power-up or after a PDS (programming disable) instruction must first be preceded by the PEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed or the PDS instruction is sent. The PDS instruction can be used to disable all the CAT59C11I's program and erase functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT59C11I regardless of the programming enable/disable status.

PROGRAM

After receiving a PROGRAM command, address, and the data, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking erase and data store cycle begins. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT59C11I can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin.

ERASE ALL

Upon receiving an ERAL command, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking erase sequence starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT59C11I can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin.

WRITE ALL

Upon receiving a WRAL command and data, the RDY/$\overline{\text{BUSY}}$ pin goes low and the self clocking data store cycle starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT59C11I can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin. It **IS** necessary for all memory locations to be erased before the WRAL command is executed.

CAT93C46
1K-BIT SERIAL E²PROM

700KHz OPERATION

DESCRIPTION

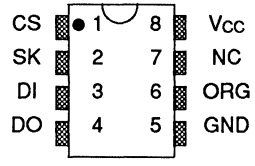
The CAT93C46 is a 1K bit Serial E²PROM memory device organized in 64 registers of 16 bits (ORG pin at Vcc) or 128 registers of 8 bits each (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT93C46 is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 10,000 erase/write cycles and has a data retention of 10 years. It is packaged in an 8 pin DIP or S.O. package. To be offered in 3V version (CAT33C101).

FEATURES

- High speed: 700 KHz clock frequency
- Single 5V supply
- 64x16 or 128x8 (user selectable) serial memory
- Compatible with National Semiconductor NMC 9346
- Self timed programming cycle with Autoerase
- Highly reliable CMOS floating gate technology
- Word and chip erasable
- 10,000 erase/write cycles
- 10 year data retention
- Power-up inadvertent write protection

PIN CONFIGURATION

TOP VIEW

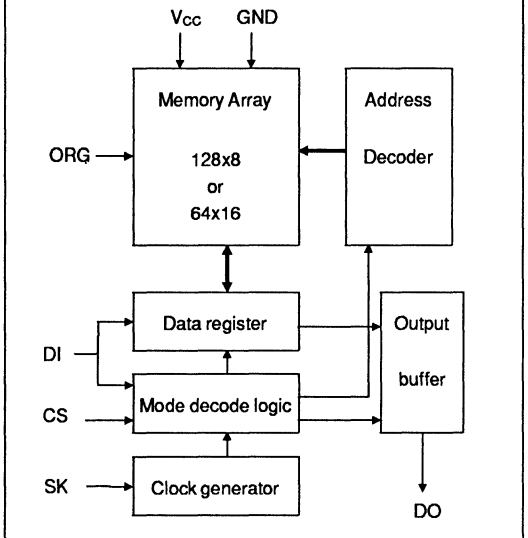


PIN FUNCTIONS

CS	Chip select
SK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
GND	Ground
NC	No connection
ORG	Memory organization

Note: When the **ORG** pin is connected to Vcc, the 64x16 organization is selected. When it is connected to ground, the 128x8 organization is selected. If the **ORG** pin is left unconnected, then an internal pullup device will select the 64x16 organization.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature	T_{stg}	-65°C to +150°C
Power supply	V_{CC}	+7 V
Voltage on any input pin		-0.3 to +7V
Voltage on any output pin		-0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, Commercial T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC1}	Current consumption (operating)	DI=0.0V, SK=5.0V V_{CC} =5.0 V, CS = 5.0V Outputs unloaded			3	mA
I_{CC2}	Current consumption (standby)	V_{CC} = 5.5V, CS = 0 DI = 0, SK = 0			100	µA
I_{LI}	Input leakage current	V_{IN} = 5.5V			10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V, CS = 0			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V

INSTRUCTION SET

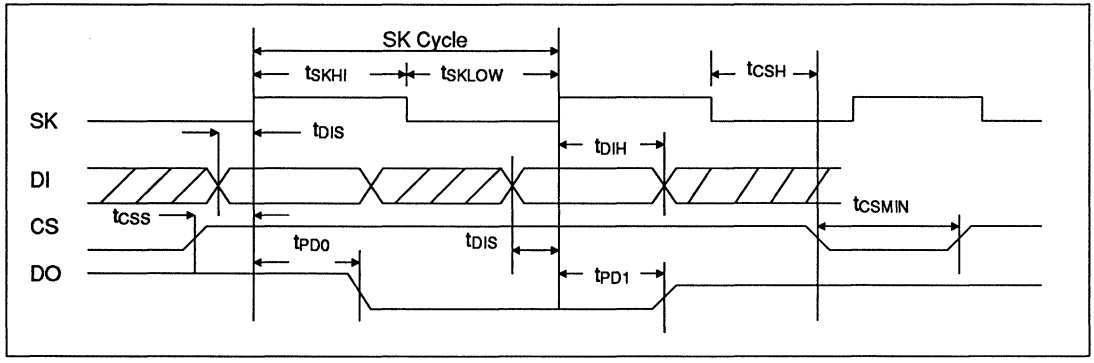
Instruction	Start Bit	Opcode	Address		Data		Comments
			128 x 8	64 x 16	128 x 8	64 x 16	
READ	1	1 0	A6 - A0	A5 - A0			Read address AN - A0
ERASE	1	1 1	A6 - A0	A5 - A0			Erase address AN - A0
WRITE	1	0 1	A6 - A0	A5 - A0	D7 - D0	D15 - D0	Write address AN - A0
EWEN	1	0 0	11XXXXX	11XXXX			Program enable
EWDS	1	0 0	00XXXXX	00XXXX			Program disable
ERAL	1	0 0	10XXXXX	10XXXX			Erase all addresses
WRAL	1	0 0	01XXXXX	01XXXX	D7 - D0	D15 - D0	Program all addresses

AC CHARACTERISTICS

(V_{CC} = +5V ±10%, Commercial T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{CSS}	CS setup time		50			ns
t_{CSH}	CS hold time	C_L = 100pF V_{OL} = 0.8V, V_{OH} = 2.0V V_{IL} = 0.45V, V_{IH} = 2.4V	0			ns
t_{DIS}	DI setup time		100			ns
t_{DIH}	DI hold time		100			ns
t_{PD1}	Output delay to 1				500	ns
t_{PD0}	Output delay to 0				500	ns
t_{HZ}	Output delay to High-Z			100		ns
t_{EW}	Erase/Write pulse width				10	ms
t_{CSMIN}	Minimum CS low time		250			ns
t_{SKHI}	Minimum SK high time		100			ns
t_{SKLOW}	Minimum SK low time		660			ns
t_{SV}	Output delay to status valid	C_L = 100pF			500	ns
SK_{MAX}	Maximum clock frequency		DC		700	kHz

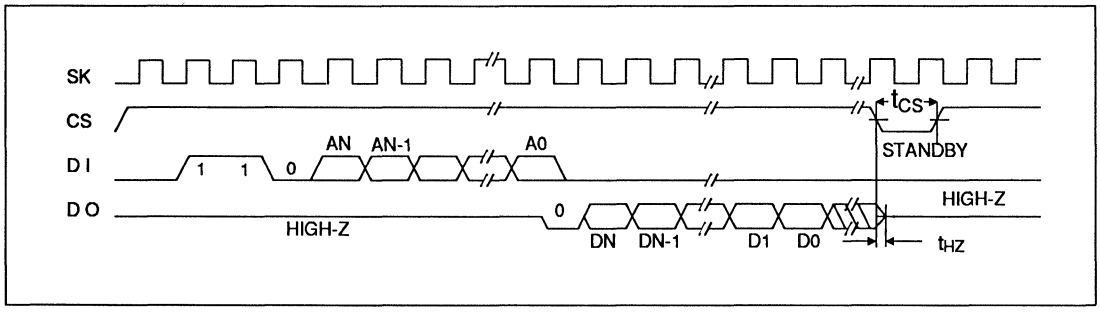
SYNCHRONOUS TIMINGS



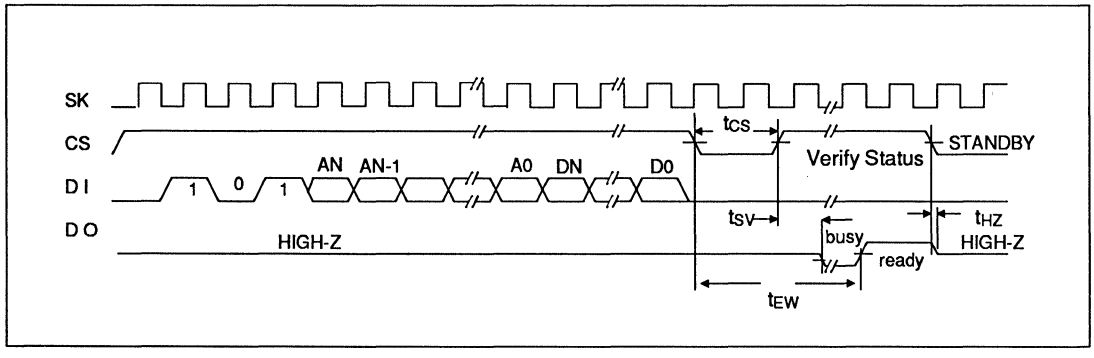
INSTRUCTION TIMING <ORGANIZATION>

Organization	A_N (or AN)	D_N (or DN)
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

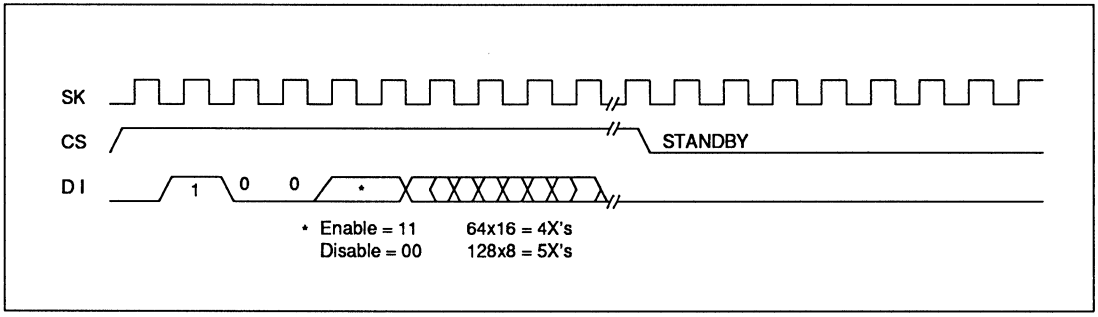
INSTRUCTION TIMING <READ>



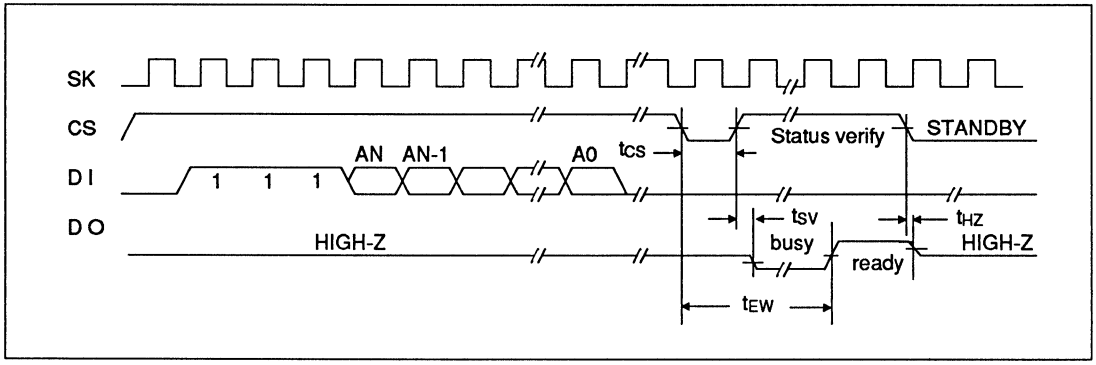
INSTRUCTION TIMING <WRITE>



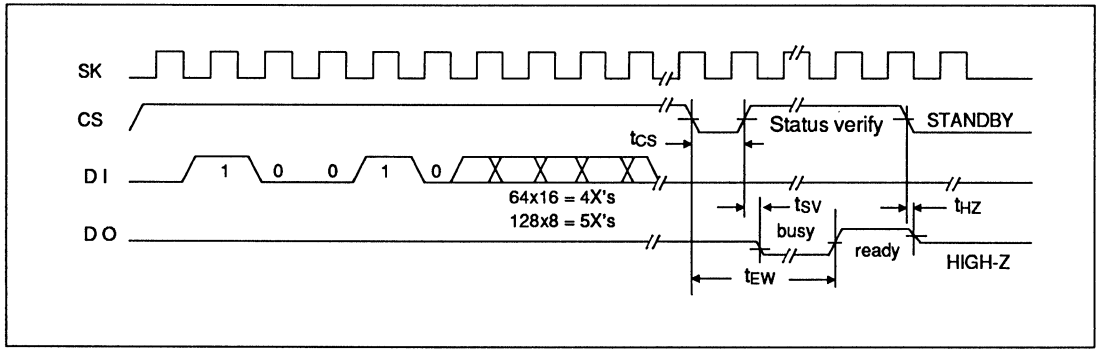
INSTRUCTION TIMING <EWEN, EWDS>



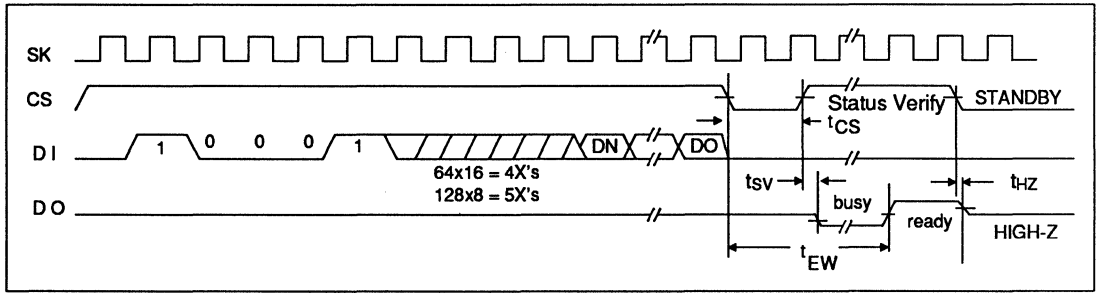
INSTRUCTION TIMING <ERASE>



INSTRUCTION TIMING <ERAL>



INSTRUCTION TIMING <WRAL>



DEVICE OPERATION

The CAT93C46 is a 1024 bit nonvolatile memory intended for use with the COPS™ family of microcontrollers, or other standard microprocessors. The CAT93C46 can be organized as either 64 registers by 16 bits, or as 128 registers by 8 bits. Seven 9 bit instructions (10 bit instruction in 128 by 8 organization) control the reading, writing and erase operations of the devices. The CAT93C46 operates on a single 5V supply and will generate on chip, the high voltage required during any programming operation. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a programming operation. The ready/busy status can be determined after a programming operation by selecting the device and polling the DO pin; DO being low indicates that the programming operation is not completed, while DO being high indicates that the device is ready. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin. The format for all instructions sent to the CAT93C46 is a logical "1" start bit, a 2 bit (or 4 bit) op code, a 6 bit address (7 bit address when organized as 128 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 128 X 8).

At power-down , when V_{CC} falls below a threshold of approximately 3.5V, the data protection circuitry inhibits all modes of operation and a programming disable (EWDS) is executed internally.

READ

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT93C46 will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed. The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

ERASE/WRITE ENABLE AND DISABLE

The CAT93C46 powers up in the programming disable state. Any programming after power-up or after an EWDS (programming disable) instruction must first be preceded by the EWEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT93C46 programming and erasing functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT93C46 regardless of the programming enable/disable status.

ERASE

Upon receiving an ERASE command and address, the CS (chip select) must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46 can be determined by

selecting the device and polling the DO pin. Once erased, the content of an erased location returns to logical "1" state.

WRITE

After receiving a WRITE command, address and the data, the CS (chip select) must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46 can be determined by selecting the device and polling the DO pin. With the CAT93C46 it is **NOT** necessary to erase a memory location before the WRITE command.

ERASE ALL

Upon receiving an ERAL command, the CS (chip select) must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46 can be determined by selecting the device and polling the DO pin. Once erased, the contents of all memory bits return to logical "1" state.

WRITE ALL

Upon receiving a WRAL command and data, the CS (chip select) must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46 can be determined by selecting the device and polling the DO pin. It **IS** necessary for all memory locations to be erased before the WRAL command is executed.

CAT93C46H - High Endurance 700KHz
1K BIT SERIAL E²PROM OPERATION

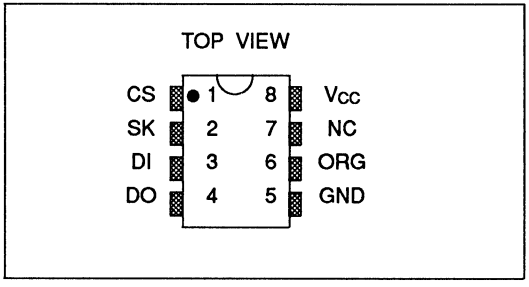
DESCRIPTION

The CAT93C46H is a High Endurance CMOS 1K-bit serial E²PROM with a low current drain of 3mA active and 100µA standby. Its configuration is user selectable as either 64 registers by 16 bits or 128 registers by 8 bits and has been designed to interface serially with industry standard microcontrollers. Manufactured using Catalyst's advanced CMOS E²PROM floating gate technology, the device can endure 100,000 erase/write cycles and has a data retention of 100 years. The CAT93C46H is assembled in either an 8-pin DIP or S.O. package, and will be available in a 3V version (CAT33C101H).

FEATURES

- High-speed 700KHz operation
- Single 5V supply
- 64x16 or 128x8 user selectable serial memory
- Compatible with National Semiconductor NMC 9346
- Self-timed programming cycle with Autoerase
- Word and chip-erasable
- Operating range 0°C to 70°C
- Highly reliable CMOS floating gate technology
- 100,000 erase/write cycles
- 100 year data retention
- Power-up inadvertent write protection

PIN CONFIGURATION DIP AND S.O.

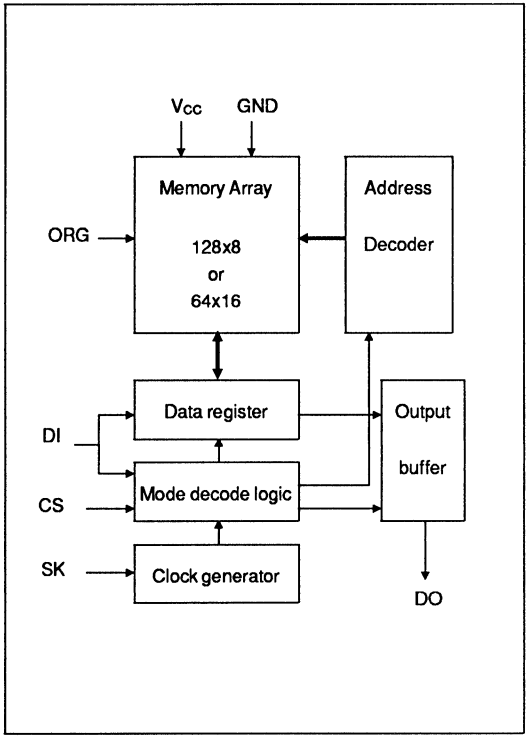


PIN FUNCTIONS

CS	Chip select
SK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
GND	Ground
NC	No connect
ORG	Memory organization

Note: When the ORG pin is connected to Vcc, the 64x16 organization is selected. When it is connected to ground, the 128x8 organization is selected. If the ORG pin is left unconnected, an internal pullup device will select the 64x16 organization.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature . . . . . -65°C to +150°C
Power supply (V_{CC}) . . . . . +7V
Voltage on any input pin . . . . . -0.3 to +7V
Voltage on any output pin . . . . . -0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC1}	Current consumption (operating)	DI=0.0V, SK=5.0V V_{CC} =5.0V, CS = 5.0V Outputs unloaded			3	mA
I_{CC2}	Current consumption (stand-by)	V_{CC} = 5.5V, CS = 0V DI = 0V, SK = 0V			100	µA
I_{LI}	Input leakage current	V_{IN} = 5.5V			10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V, CS = 0V			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V

INSTRUCTION SET

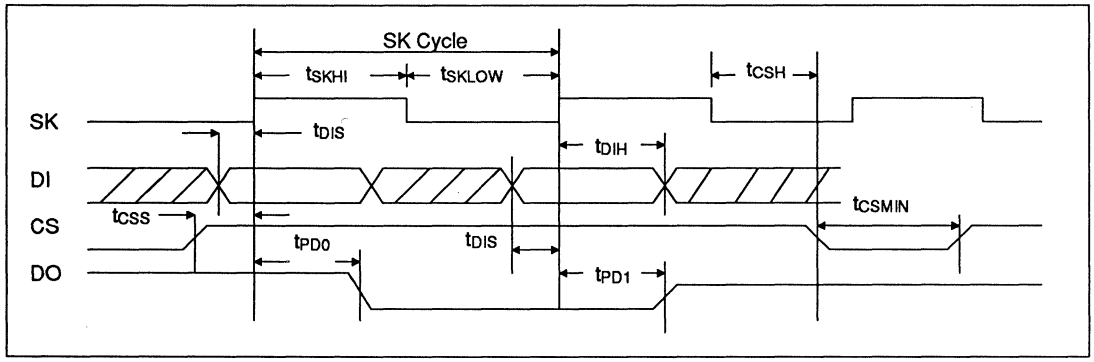
Instruction	Start Bit	Opcode	Address		Data		Comments
			128 x 8	64 x 16	128 x 8	64 x 16	
READ	1	1 0	A6 - A0	A5 - A0			Read address AN - A0
ERASE	1	1 1	A6 - A0	A5 - A0			Erase address AN - A0
WRITE	1	0 1	A6 - A0	A5 - A0	D7 - D0	D15 - D0	Write address AN - A0
EWEN	1	0 0	11XXXXX	11XXXX			Program enable
EWDS	1	0 0	00XXXXX	00XXXX			Program disable
ERAL	1	0 0	10XXXXX	10XXXX			Erase all addresses
WRAL	1	0 0	01XXXXX	01XXXX	D7 - D0	D15 - D0	Program all addresses

AC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{CSS}	CS setup time		50			ns
t_{CSH}	CS hold time	C_L = 100pF V_{OL} = 0.8V, V_{OH} = 2.0V V_{IL} = 0.45V, V_{IH} = 2.4V	0			ns
t_{DIS}	DI setup time		100			ns
t_{DIH}	DI hold time		100			ns
t_{PD1}	Output delay to 1				500	ns
t_{PD0}	Output delay to 0				500	ns
t_{HZ}	Output delay to Hi-Z			100		ns
t_{EW}	Erase/Write pulse width				10	ms
t_{CSMIN}	Minimum CS low time		250			ns
t_{SKHI}	Minimum SK high time		100			ns
t_{SKLOW}	Minimum SK low time		660			ns
t_{SV}	Output delay to status valid	C_L = 100pF			500	ns
SK_{MAX}	Maximum clock frequency		DC		700	kHz

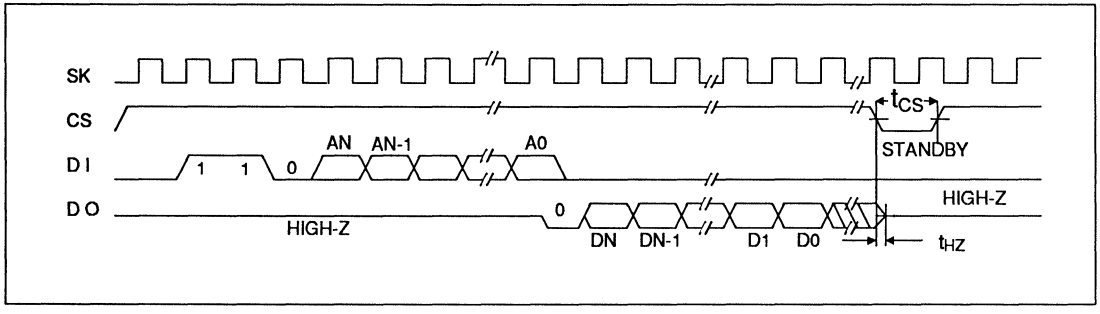
SYNCHRONOUS TIMINGS



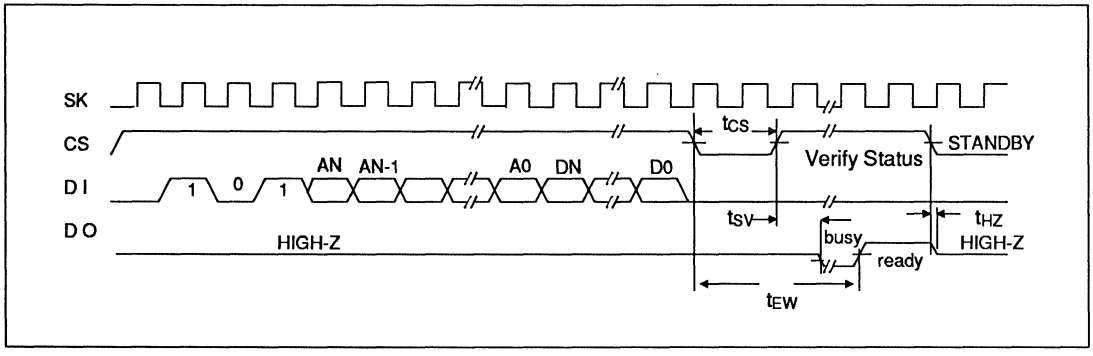
INSTRUCTION TIMING <ORGANIZATION>

Organization	A_N (or AN)	D_N (or DN)
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

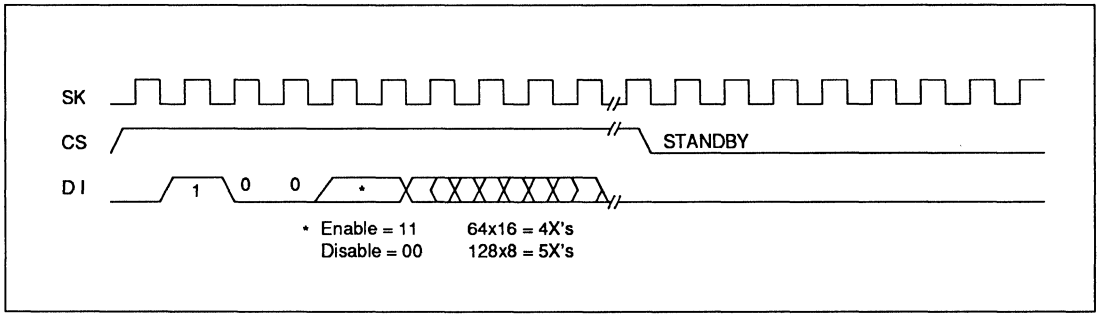
INSTRUCTION TIMING <READ>



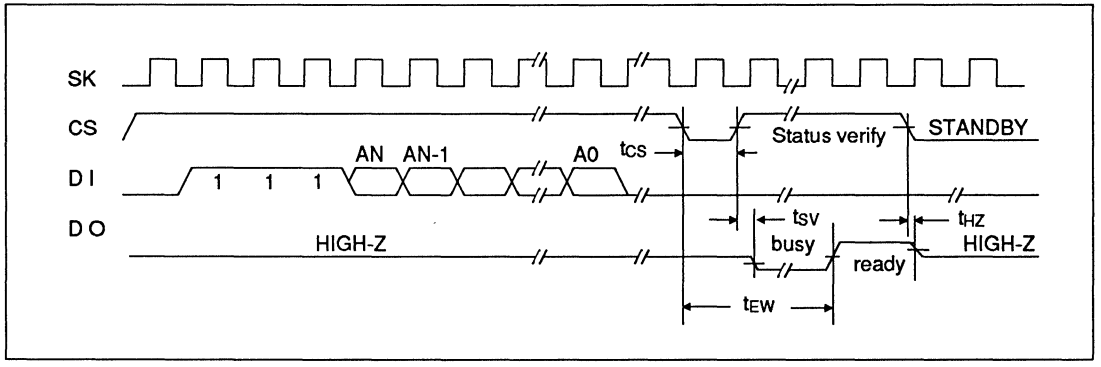
INSTRUCTION TIMING <WRITE>



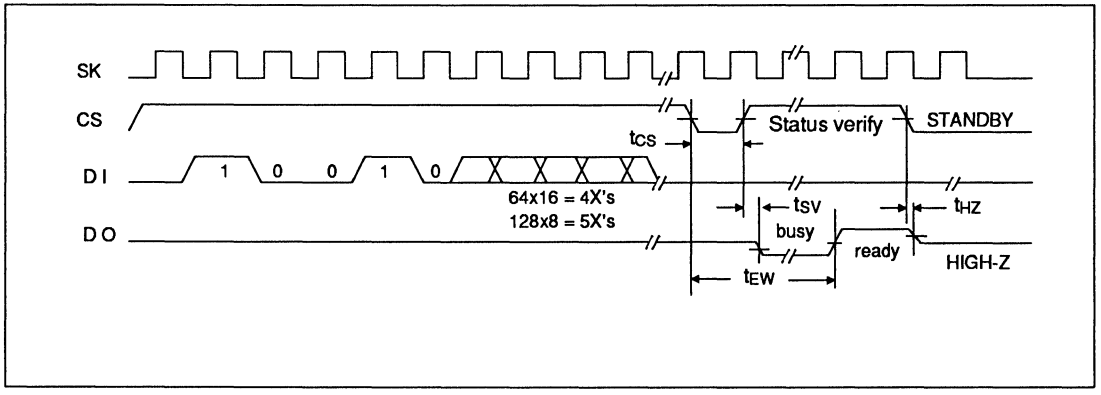
INSTRUCTION TIMING <EWEN, EWDS>



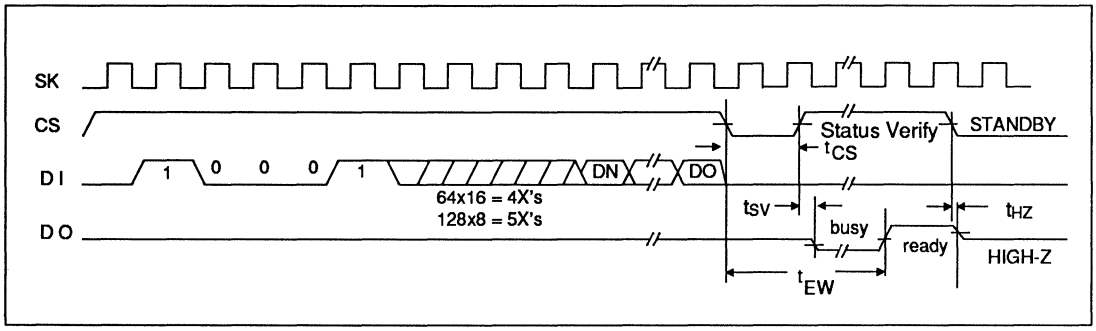
INSTRUCTION TIMING <ERASE>



INSTRUCTION TIMING <ERAL>



INSTRUCTION TIMING <WRAL>



DEVICE OPERATION

The CAT93C46H is a 1024 bit nonvolatile memory intended for use with the COPS™ family of microcontrollers and designed to operate smoothly with other standard microprocessors as well. The CAT93C46H can be organized as either 64 registers by 16 bits, or as 128 registers by 8 bits. Seven 9-bit instructions (10-bit instructions in 128 by 8 organization) control the reading, writing, and erase operations of the device. The CAT93C46H operates on a single 5V supply and will generate on-chip the high voltage required during any programming operation. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a programming operation. The ready/busy status can be determined after a programming operation by selecting the device and polling the DO pin; DO low indicates that the programming operation is not completed, while DO high indicates that the device is ready. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin. The format for all instructions sent to the CAT93C46H is a logical "1" start bit, a 2 bit (or 4 bit) op code, a 6 bit address (7 bit address when organized as 128 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 128 X 8).

READ

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT93C46H will come out of the high impedance state, and after sending an initial dummy zero bit, will begin shifting out the 16 (or 8) bits of data located at the specified address. The data bits being shifted out will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

ERASE/WRITE ENABLE AND DISABLE

The CAT93C46H powers up in the programming disable state. Any programming after power-up or after an EWDS (programming disable) instruction must first be preceded by the EWEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT93C46H programming and erasing functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT93C46H regardless of the programming enable/disable status.

ERASE

Upon receiving an ERASE command and address, the device must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of

the CAT93C46H can be determined by selecting the device and polling the DO pin. Once erased, the content of an erased location returns to logical "1" state.

WRITE

After receiving a WRITE command, address and data, the device must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase and data store cycle of the memory register specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46H can be determined by selecting the device and polling the DO pin. With the CAT93C46H it is **NOT** necessary to erase a memory register before the WRITE command.

ERASE ALL

Upon receiving an ERAL command, the device must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46H can be determined by selecting the device and polling the DO pin. Once erased, the contents of all memory bits return to logical "1" state.

WRITE ALL

Upon receiving a WRAL command and data, the device must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking write cycle to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46H can be determined by selecting the device and polling the DO pin.

It **IS** necessary for all memory locations to be erased before the WRAL command is executed.

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CAT 93C46I [Industrial Temperature]
1K-BIT SERIAL E²PROM

700KHz OPERATION

DESCRIPTION

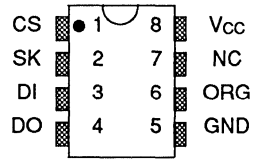
The CAT93C46I is a 1K bit Serial E²PROM memory device organized in 64 registers of 16 bits (ORG pin at Vcc) or 128 registers of 8 bits each (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT93C46I is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 10,000 erase/write cycles and has a data retention of 10 years. It is packaged in an 8 pin DIP or S.O. package. To be offered in a 3V version (CAT33C101I).

FEATURES

- High speed: 700 KHz clock frequency
- Single 5V supply
- 64x16 or 128x8 (user selectable) serial memory
- Compatible with National Semiconductor NMC 9346
- Self timed programming cycle with Autoerase
- Highly reliable CMOS floating gate technology
- Word and chip erasable
- 10,000 erase/write cycles
- 10 year data retention
- Power-up inadvertent write protection

PIN CONFIGURATION

TOP VIEW

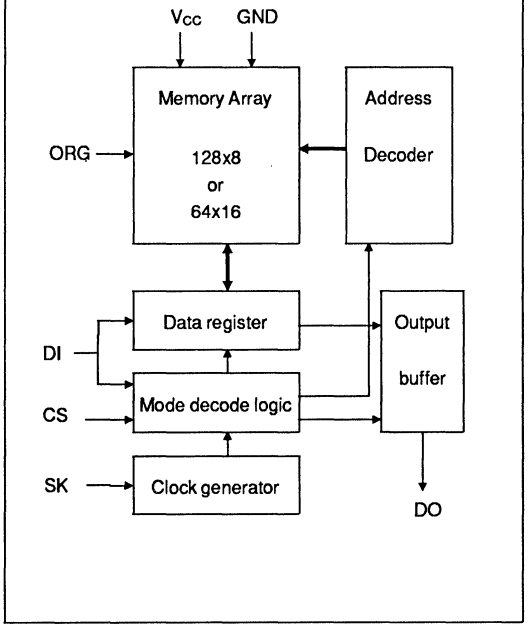


PIN FUNCTIONS

CS	Chip select
SK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
GND	Ground
NC	No connection
ORG	Memory organization

Note: When the **ORG** pin is connected to Vcc, the 64x16 organization is selected. When it is connected to ground, the 128x8 organization is selected. If the **ORG** pin is left unconnected, then an internal pullup device will select the 64x16 organization.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature	T_{stg}	-65°C to +150°C
Power supply	V_{CC}	+7 V
Voltage on any input pin		-0.3 to +7V
Voltage on any output pin		-0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, Industrial T_A = -40°C to 85°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC1}	Current consumption (operating)	DI=0.0V, SK=5.0V V_{CC} =5.0 V, CS = 5.0V Outputs unloaded			4	mA
I_{CC2}	Current consumption (standby)	V_{CC} = 5.5V, CS = 0 DI = 0, SK = 0			100	µA
I_{LI}	Input leakage current	V_{IN} = 5.5V			10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V, CS = 0			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V

INSTRUCTION SET

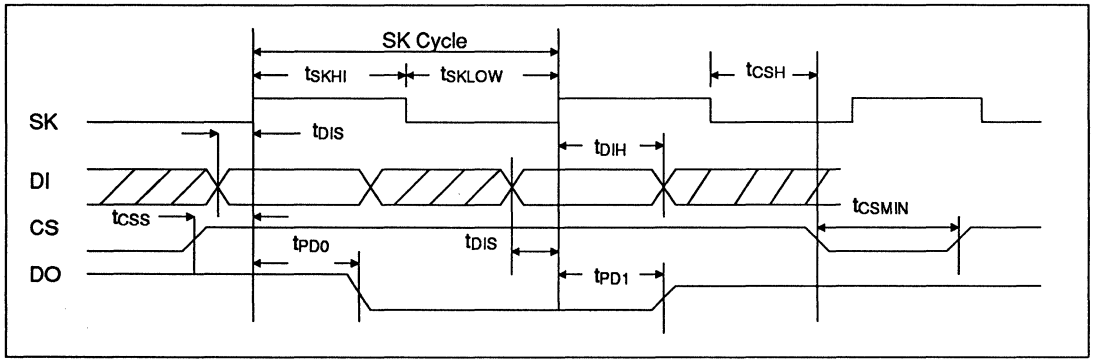
Instruction	Start Bit	Opcode	Address		Data		Comments
			128 x 8	64 x 16	128 x 8	64 x 16	
READ	1	1 0	A6 - A0	A5 - A0			Read address AN - A0
ERASE	1	1 1	A6 - A0	A5 - A0			Erase address AN - A0
WRITE	1	0 1	A6 - A0	A5 - A0	D7 - D0	D15 - D0	Write address AN - A0
EWEN	1	0 0	11XXXXX	11XXXX			Program enable
EWDS	1	0 0	00XXXXX	00XXXX			Program disable
ERAL	1	0 0	10XXXXX	10XXXX			Erase all addresses
WRAL	1	0 0	01XXXXX	01XXXX	D7 - D0	D15 - D0	Program all addresses

AC CHARACTERISTICS

(V_{CC} = +5V ±10%, Industrial T_A = -40°C to 85°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{CSS}	CS setup time		50			ns
t_{CSH}	CS hold time	C_L = 100pF V_{OL} = 0.8V, V_{OH} = 2.0V V_{IL} = 0.45V, V_{IH} = 2.4V	0			ns
t_{DIS}	DI setup time		100			ns
t_{DIH}	DI hold time		100			ns
t_{PD1}	Output delay to 1				500	ns
t_{PD0}	Output delay to 0				500	ns
t_{HZ}	Output delay to High-Z			100		ns
t_{EW}	Erase/Write pulse width				10	ms
t_{CSMIN}	Minimum CS low time		250			ns
t_{SKHI}	Minimum SK high time		100			ns
t_{SKLOW}	Minimum SK low time		660			ns
t_{SV}	Output delay to status valid	C_L = 100pF			500	ns
SK_{MAX}	Maximum clock frequency		DC		700	kHz

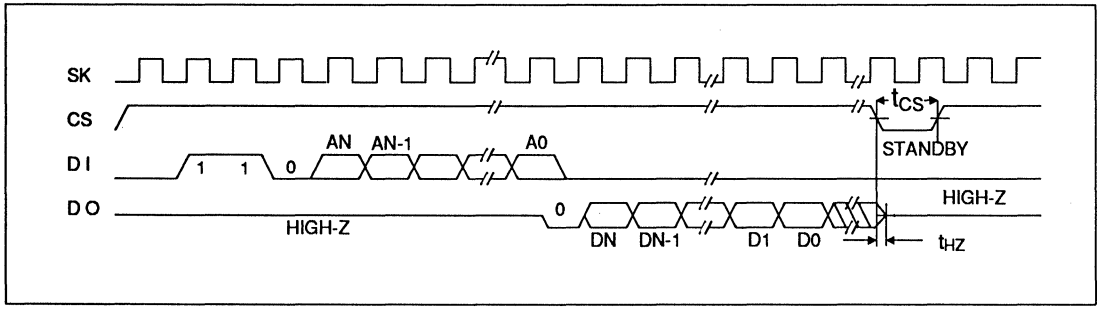
SYNCHRONOUS TIMINGS



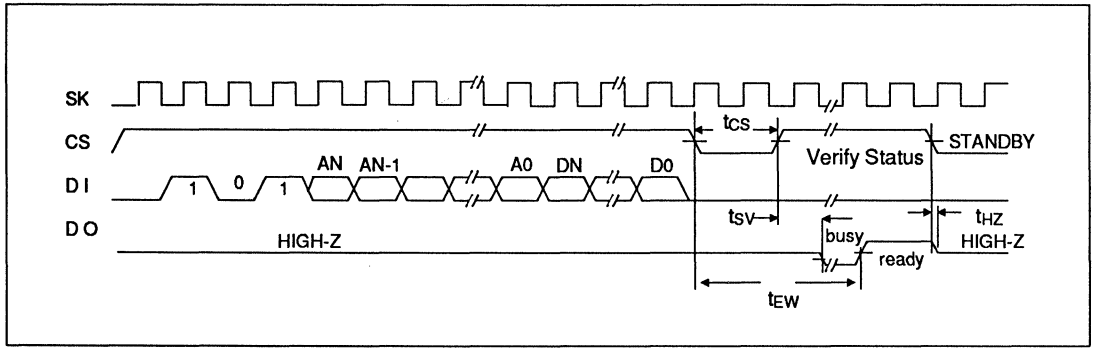
INSTRUCTION TIMING <ORGANIZATION>

Organization	A_N (or AN)	D_N (or DN)
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

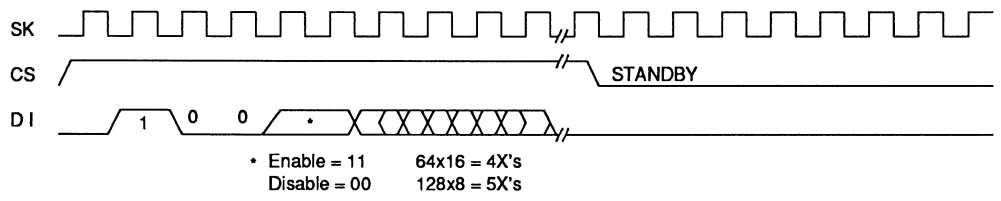
INSTRUCTION TIMING <READ>



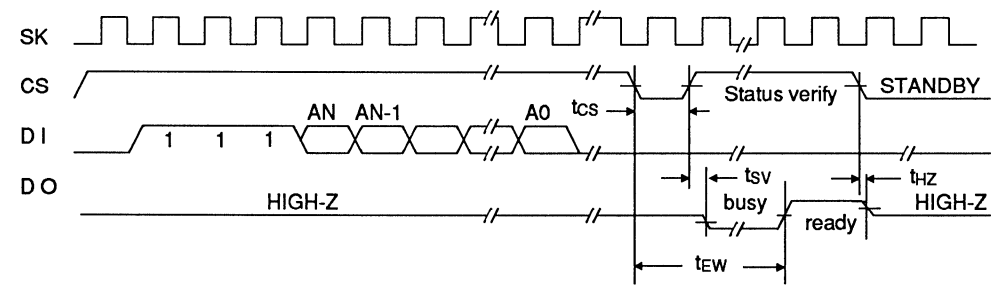
INSTRUCTION TIMING <WRITE>



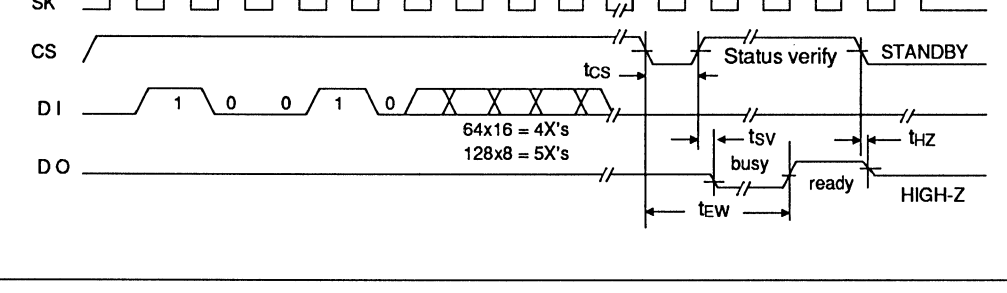
INSTRUCTION TIMING <EWEN, EWDS>



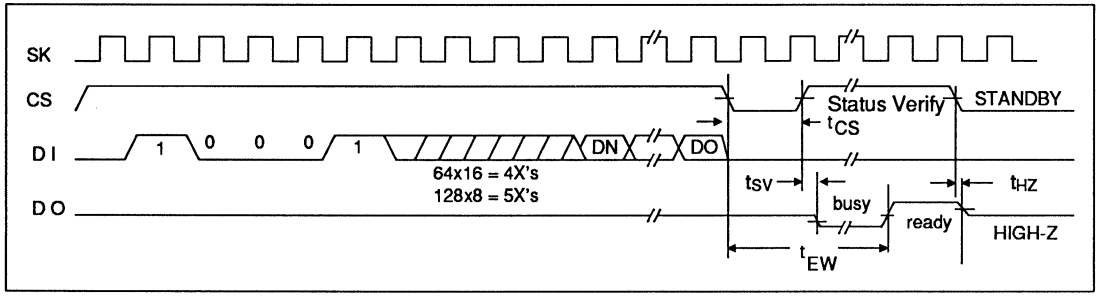
INSTRUCTION TIMING <ERASE>



INSTRUCTION TIMING <ERAL>



INSTRUCTION TIMING <WRAL>



DEVICE OPERATION

The CAT93C46I is a 1024 bit nonvolatile memory intended for use with the COPS™ family of microcontrollers, or other standard microprocessors. The CAT93C46I can be organized as either 64 registers by 16 bits, or as 128 registers by 8 bits. Seven 9 bit instructions (10 bit instruction in 128 by 8 organization) control the reading, writing and erase operations of the devices. The CAT93C46I operates on a single 5V supply and will generate on chip, the high voltage required during any programming operation. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a programming operation. The ready/busy status can be determined after a programming operation by selecting the device and polling the DO pin; DO being low indicates that the programming operation is not completed, while DO being high indicates that the device is ready. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin. The format for all instructions sent to the CAT93C46I is a logical "1" start bit, a 2 bit (or 4 bit) op code, a 6 bit address (7 bit address when organized as 128 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 128 X 8).

At power-down , when V_{CC} falls below a threshold of approximately 3.5V, the data protection circuitry inhibits all modes of operation and a programming disable (EWDS) is executed internally.

READ

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT93C46I will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed. The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

ERASE/WRITE ENABLE AND DISABLE

The CAT93C46I powers up in the programming disable state. Any programming after power-up or after an EWDS (programming disable) instruction must first be preceded by the EWEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT93C46I programming and erasing functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT93C46I regardless of the programming enable/disable status.

ERASE

Upon receiving an ERASE command and address, the CS (chip select) must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46I can be determined by

selecting the device and polling the DO pin. Once erased, the content of an erased location returns to logical "1" state.

WRITE

After receiving a WRITE command, address and the data, the CS (chip select) must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46I can be determined by selecting the device and polling the DO pin. With the CAT93C46I it is **NOT** necessary to erase a memory location before the WRITE command.

ERASE ALL

Upon receiving an ERAL command, the CS (chip select) must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46I can be determined by selecting the device and polling the DO pin. Once erased, the contents of all memory bits return to logical "1" state.

WRITE ALL

Upon receiving a WRAL command and data, the CS (chip select) must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46I can be determined by selecting the device and polling the DO pin. It **IS** necessary for all memory locations to be erased before the WRAL command is executed.

CAT93C46A
1K BIT SERIAL E²PROM

700KHz OPERATION

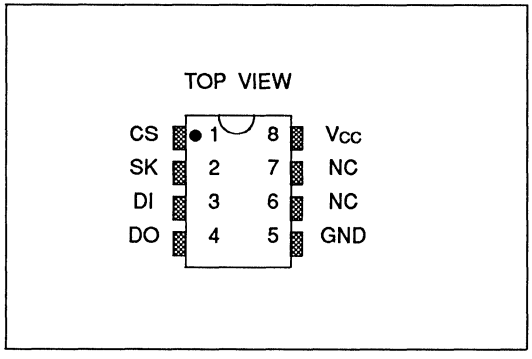
DESCRIPTION

The CAT93C46A is a CMOS 1K-bit serial E²PROM with a low current drain of 3mA active and 100µA standby. It is configured as 64 registers of 16 bits each, and has been designed to interface serially with industry standard microcontrollers. Manufactured using Catalyst's advanced CMOS E²PROM floating gate technology, the device can endure 10,000 erase/write cycles and has a data retention of 10 years. The CAT93C46A is assembled in either an 8 pin DIP or S.O. package, and will be available in a 3V version (CAT33C101A).

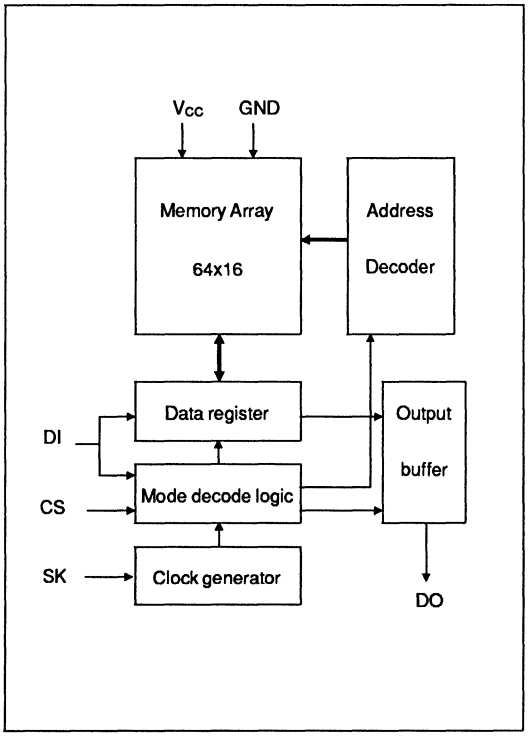
FEATURES

- High-speed 700KHz operation
- Single 5V supply
- 64x16 serial memory
- Compatible with National Semiconductor NMC 9346
- Self-timed programming cycle with Autoerase
- Word and chip-erasable
- Operating range 0°C to 70°C [industrial temperature range available]
- Highly reliable CMOS floating gate technology
- 10,000 erase/write cycles
- 10 year data retention
- Power-up inadvertent write protection

PIN CONFIGURATION DIP AND S.O.



BLOCK DIAGRAM



PIN FUNCTIONS

CS	Chip select
SK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
GND	Ground
NC	No connect

ABSOLUTE MAXIMUM RATINGS *

Storage temperature . . . . . -65°C to +150°C
Power supply (V_{CC}) . . . . . +7V
Voltage on any input pin . . . . . -0.3 to +7V
Voltage on any output pin . . . . . -0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC1}	Current consumption (operating)	DI = 0.0V, SK = 5.0V V_{CC} =5.0V, CS = 5.0V Outputs unloaded			3	mA
I_{CC2}	Current consumption (stand-by)	V_{CC} = 5.5V, CS = 0V DI = 0V, SK = 0V			100	µA
I_{LI}	Input leakage current	V_{IN} = 5.5V			10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V, CS = 0V			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V

INSTRUCTION SET

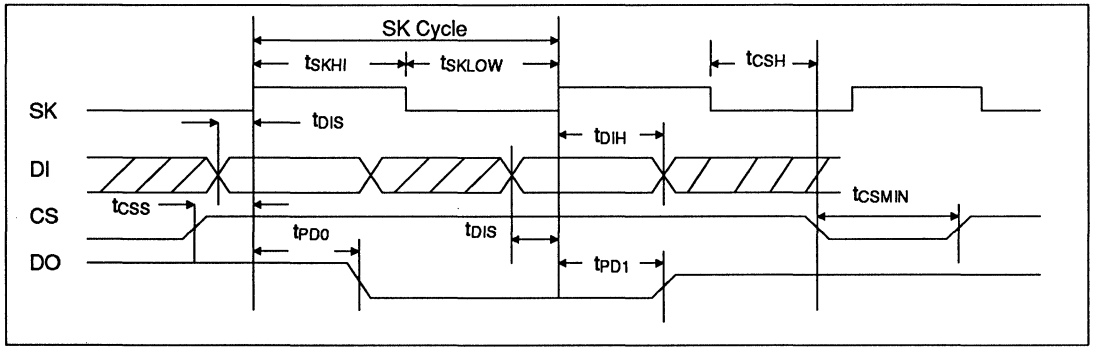
Instruction	Start Bit	Opcode	Address	Data	Comments
READ	1	1 0	A5 - A0		Read address AN - A0
ERASE	1	1 1	A5 - A0		Erase address AN - A0
WRITE	1	0 1	A5 - A0	D15 - D0	Write address AN - A0
EWEN	1	0 0	11XXXX		Program enable
EWDS	1	0 0	00XXXX		Program disable
ERAL	1	0 0	10XXXX		Erase all addresses
WRAL	1	0 0	01XXXX	D15 - D0	Program all addresses

AC CHARACTERISTICS

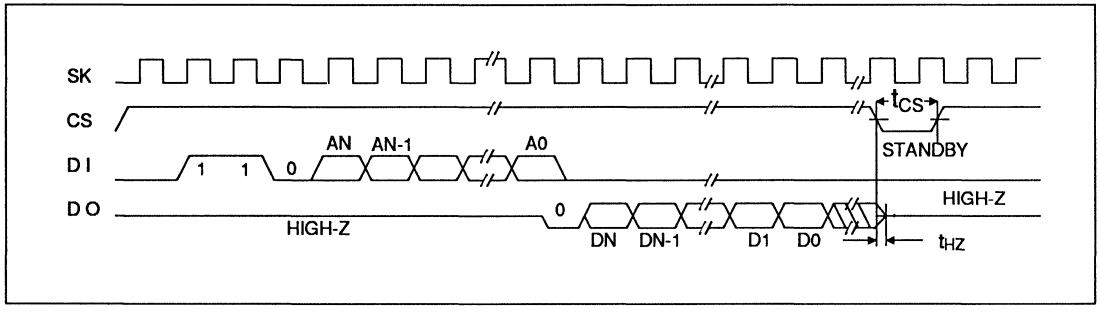
(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{CSS}	CS setup time		50			ns
t_{CSH}	CS hold time	C_L = 100pF V_{OL} = 0.8V, V_{OH} = 2.0V V_{IL} = 0.45V, V_{IH} = 2.4V	0			ns
t_{DIS}	DI setup time		100			ns
t_{DIH}	DI hold time		100			ns
t_{PD1}	Output delay to 1				500	ns
t_{PD0}	Output delay to 0				500	ns
t_{HZ}	Output delay to Hi-Z			100		ns
t_{EW}	Erase/Write pulse width				10	ms
t_{CSMIN}	Minimum CS low time		250			ns
t_{SKHI}	Minimum SK high time		100			ns
t_{SKLOW}	Minimum SK low time		660			ns
t_{SV}	Output delay to status valid	C_L = 100pF			500	ns
SK_{MAX}	Maximum clock frequency		DC		700	kHz

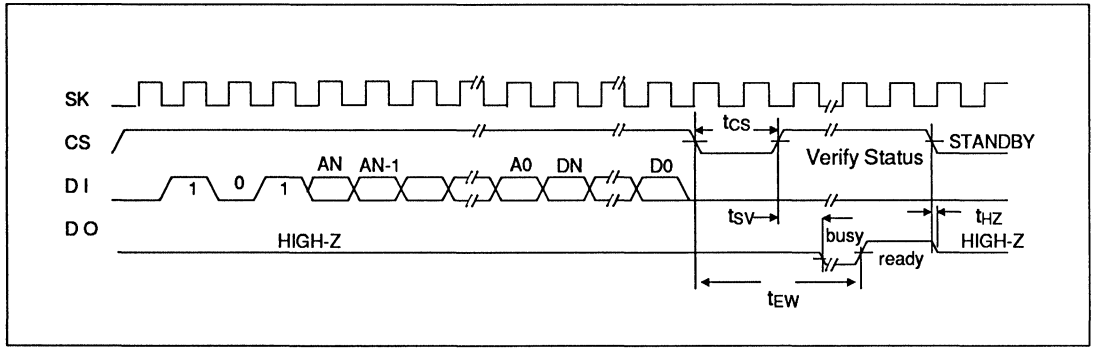
SYNCHRONOUS TIMINGS



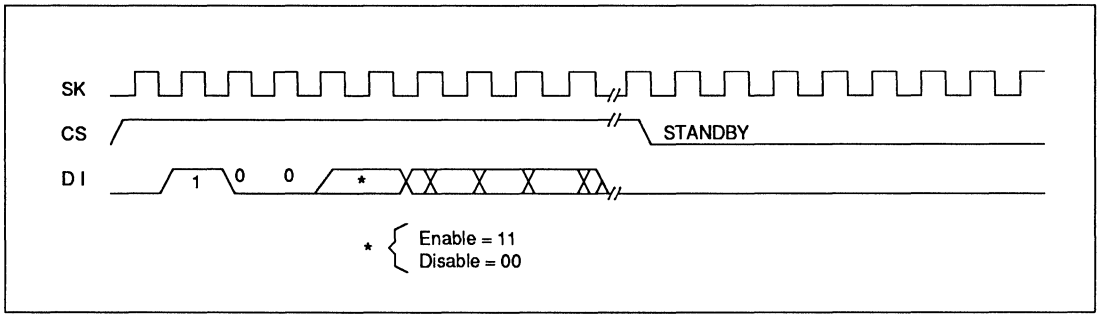
INSTRUCTION TIMING <READ>



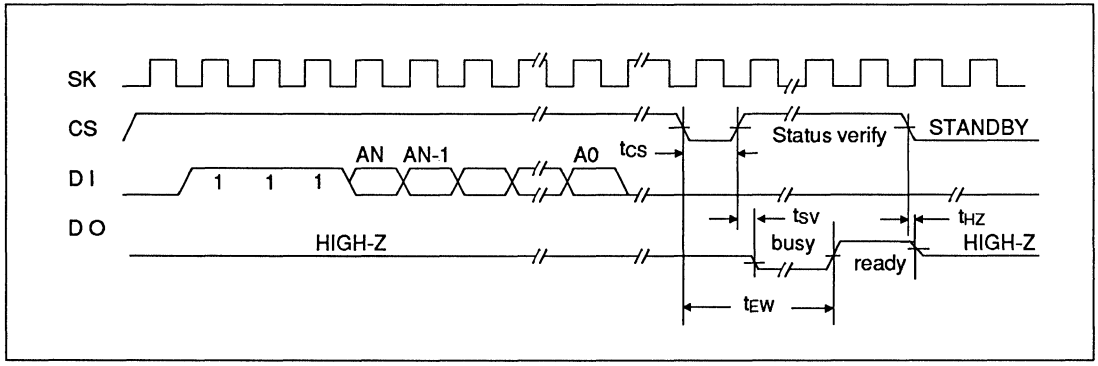
INSTRUCTION TIMING <WRITE>



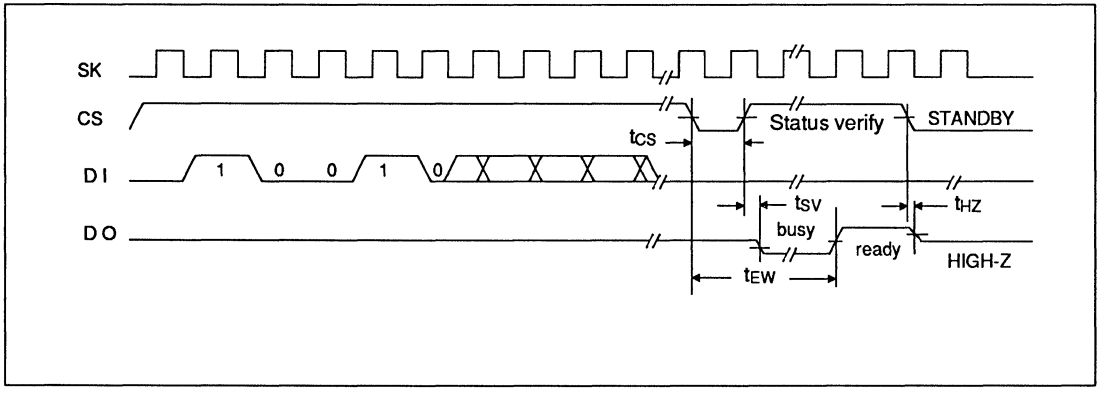
INSTRUCTION TIMING <EWEN, EWDS>



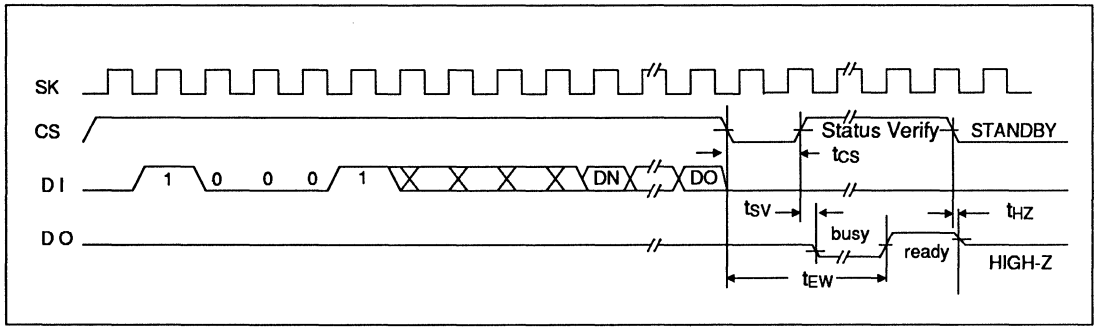
INSTRUCTION TIMING <ERASE>



INSTRUCTION TIMING <ERAL>



INSTRUCTION TIMING <WRAL>



DEVICE OPERATION

The CAT93C46A is a 1024 bit nonvolatile memory intended for use with the COPS™ family of microcontrollers and designed to operate smoothly with other standard microprocessors as well. The CAT93C46A is organized as 64 registers by 16 bits. Seven 9 bit instructions control the reading, writing and erase operations of the device. The CAT93C46A fully operates on a single 5V supply including the programming operation. Instructions, addresses and data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin remains in a high impedance state except when reading data from the device, or when checking the ready/busy status after a programming operation. The ready/busy status can be determined after a programming operation by selecting the device and polling the DO pin; DO low indicates that the programming operation is not completed, while DO high indicates that the device is ready. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin. The format for all instructions sent to the CAT93C46A is a logical "1" start bit, a 2 bit op code, a 6 bit address, and for write operations, a 16 bit data field.

READ

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT93C46A will come out of the high impedance state, and after sending an initial dummy zero bit, will begin shifting out the 16 bits of data located at the specified address. The data bits being shifted out will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

ERASE/WRITE ENABLE AND DISABLE

The CAT93C46A powers up in the programming disable state. Any programming after power-up or after an EWDS (programming disable) instruction must first be preceded by the EWEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT93C46A programming and erasing functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT93C46A regardless of the programming enable/disable status.

ERASE

Upon receiving an ERASE command and address, the device must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46A can be determined by selecting the device and polling the DO pin. Once erased, all memory locations return to a logical "1" state.

WRITE

After receiving a WRITE command, address and data, the device must be deselected for a minimum

of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase and data store cycle of the memory register specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46A can be determined by selecting the device and polling the DO pin. With the CAT93C46A it is **NOT** necessary to erase a memory register before the WRITE command.

ERASE ALL

Upon receiving an ERAL command, the device must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46A can be determined by selecting the device and polling the DO pin. Once erased, all memory locations return to logical "1" state.

WRITE ALL

Upon receiving a WRAL command and data, the device must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking write cycle to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46A can be determined by selecting the device and polling the DO pin.

It **IS** necessary for all memory locations to be erased before the WRAL command is executed.

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CAT93C46AH - High Endurance 700KHz
1K BIT SERIAL E^{2}PROM OPERATION

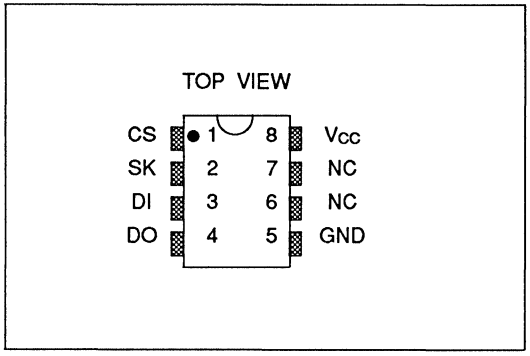
DESCRIPTION

The CAT93C46AH is an industrial temperature CMOS 1K-bit serial E^{2}PROM with a low current drain of 3mA active and 100µA standby. It is configured as 64 registers of 16 bits each, and has been designed to interface serially with industry standard microcontrollers. Manufactured using Catalyst's advanced CMOS E^{2}PROM floating gate technology, the device can endure 100,000 erase/write cycles and has a data retention of 100 years. The CAT93C46AH is assembled in either an 8 pin DIP or S.O. package, and will be available in a 3V version (CAT33C101AH).

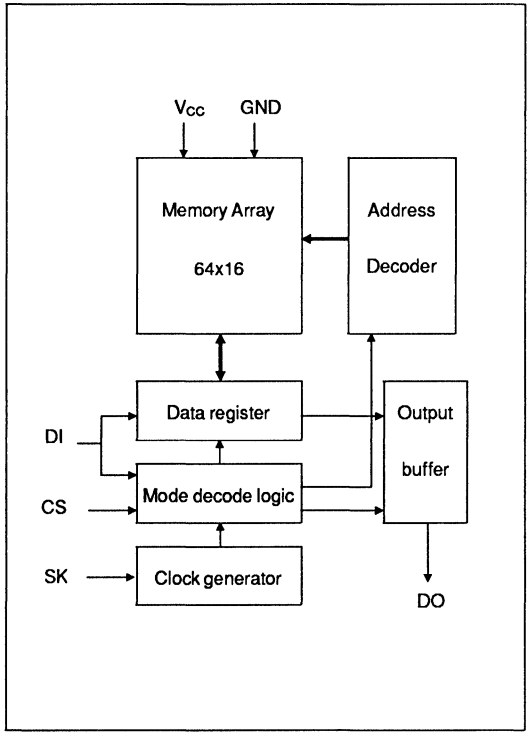
FEATURES

- High-speed 700KHz operation
- Single 5V supply
- 64x16 serial memory
- Compatible with National Semiconductor NMC 9346
- Self-timed programming cycle with Autoerase
- Word and chip-erasable
- Operating range 0°C to +70°C
- Highly reliable CMOS floating gate technology
- 100,000 erase/write cycles
- 100 year data retention
- Power-up inadvertent write protection

PIN CONFIGURATION DIP AND S.O.



BLOCK DIAGRAM



PIN FUNCTIONS

CS	Chip select
SK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
GND	Ground
NC	No connect

ABSOLUTE MAXIMUM RATINGS *

Storage temperature . . . . . -65°C to +150°C
Power supply (V_{CC}) . . . . . +7V
Voltage on any input pin . . . . . -0.3 to +7V
Voltage on any output pin . . . . . -0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC1}	Current consumption (operating)	DI = 0.0V, SK = 5.0V V_{CC} =5.0V, CS = 5.0V Outputs unloaded			3	mA
I_{CC2}	Current consumption (stand-by)	V_{CC} = 5.5V, CS = 0V DI = 0V, SK = 0V			100	µA
I_{LI}	Input leakage current	V_{IN} = 5.5V			10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V, CS = 0V			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V

INSTRUCTION SET

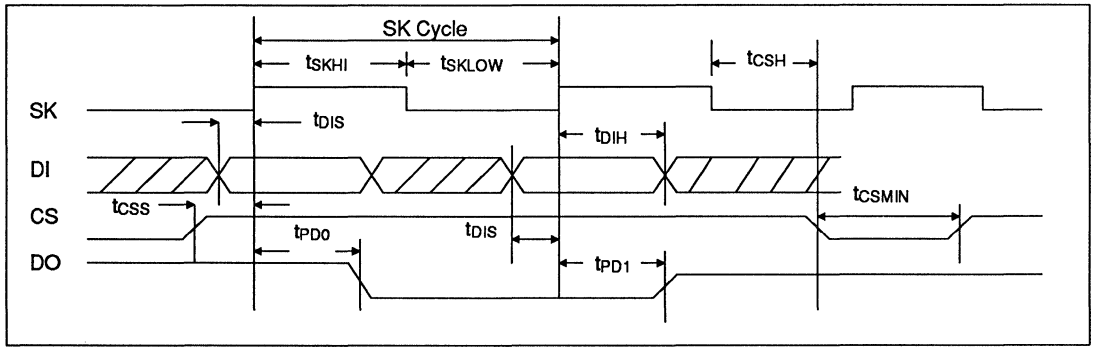
Instruction	Start Bit	Opcode	Address	Data	Comments
READ	1	1 0	A5 - A0		Read address AN - A0
ERASE	1	1 1	A5 - A0		Erase address AN - A0
WRITE	1	0 1	A5 - A0	D15 - D0	Write address AN - A0
EWEN	1	0 0	11XXXX		Program enable
EWDS	1	0 0	00XXXX		Program disable
ERAL	1	0 0	10XXXX		Erase all addresses
WRAL	1	0 0	01XXXX	D15 - D0	Program all addresses

AC CHARACTERISTICS

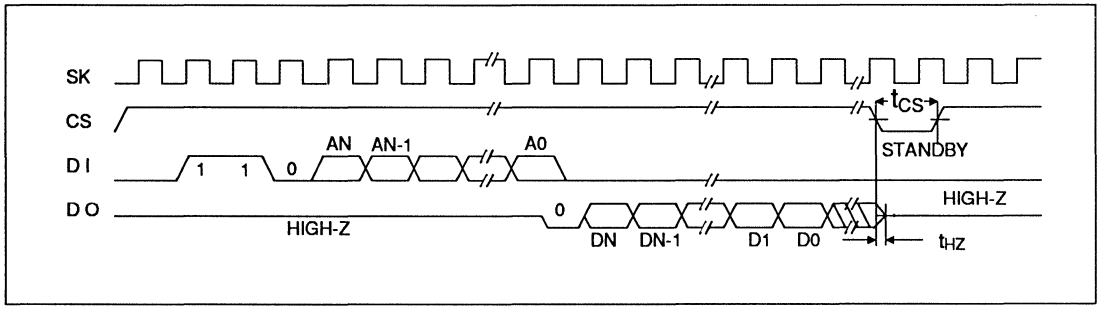
(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{CSS}	CS setup time		50			ns
t_{CSH}	CS hold time	C_L = 100pF V_{OL} = 0.8V, V_{OH} = 2.0V V_{IL} = 0.45V, V_{IH} = 2.4V	0			ns
t_{DIS}	DI setup time		100			ns
t_{DIH}	DI hold time		100			ns
t_{PD1}	Output delay to 1				500	ns
t_{PD0}	Output delay to 0				500	ns
t_{HZ}	Output delay to Hi-Z			100		ns
t_{EW}	Erase/Write pulse width				10	ms
t_{CSMIN}	Minimum CS low time		250			ns
t_{SKHI}	Minimum SK high time		100			ns
t_{SKLOW}	Minimum SK low time		660			ns
t_{SV}	Output delay to status valid	C_L = 100pF			500	ns
SK_{MAX}	Maximum clock frequency		DC		700	kHz

SYNCHRONOUS TIMINGS



INSTRUCTION TIMING <READ>



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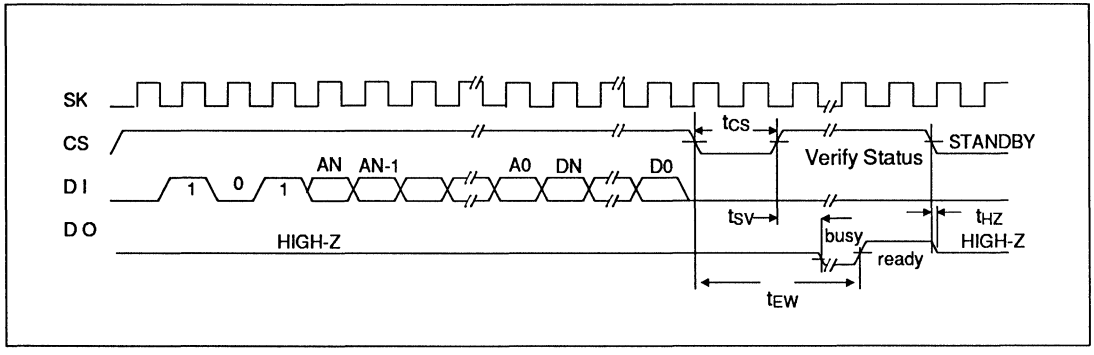
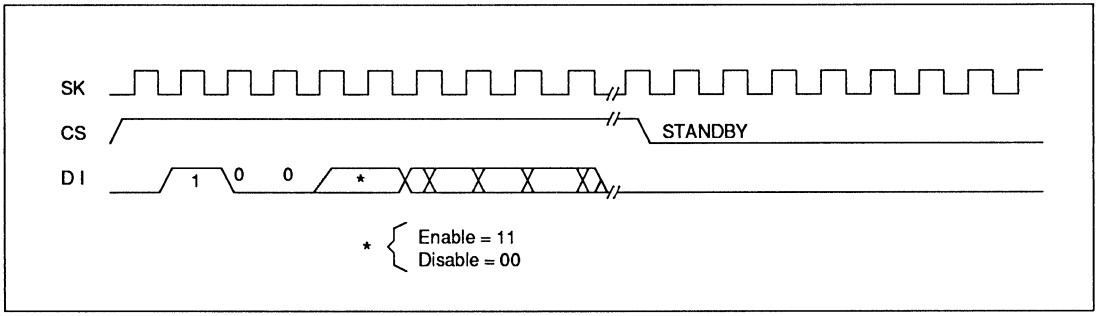
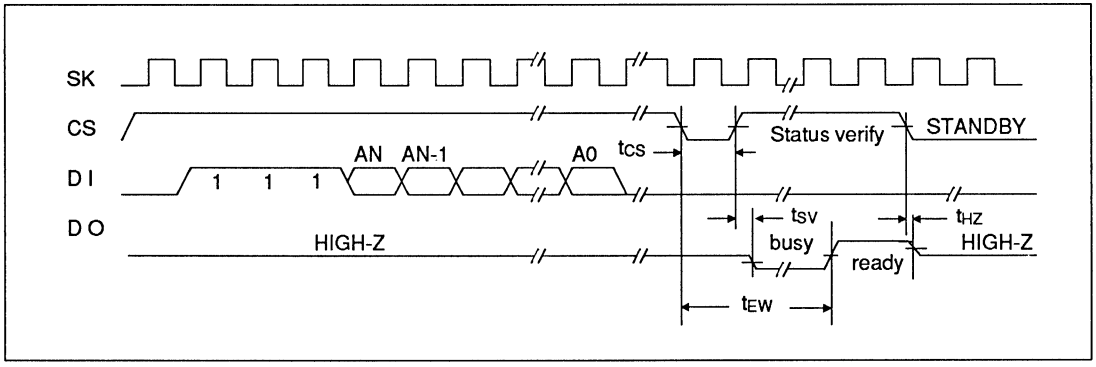


INSTRUCTION TIMING <EWEN, EWDS>



INSTRUCTION TIMING <ERASE>



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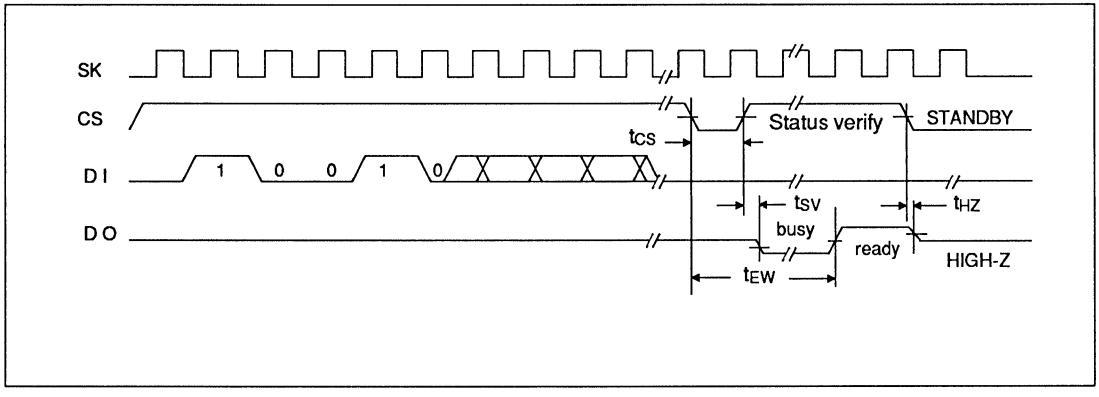

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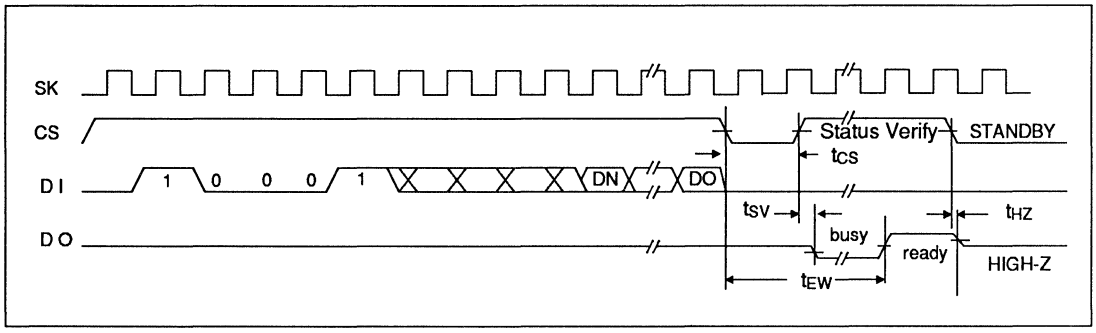

DEVICE OPERATION

The CAT93C46AH is a 1024 bit nonvolatile memory intended for use with the COPS™ family of microcontrollers and designed to operate smoothly with other standard microprocessors as well. The CAT93C46AH is organized as 64 registers by 16 bits. Seven 9 bit instructions control the reading, writing and erase operations of the device. The CAT93C46AH fully operates on a single 5V supply including the programming operation. Instructions, addresses and data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin remains in a high impedance state except when reading data from the device, or when checking the ready/busy status after a programming operation. The ready/busy status can be determined after a programming operation by selecting the device and polling the DO pin; DO low indicates that the programming operation is not completed, while DO high indicates that the device is ready. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin. The format for all instructions sent to the CAT93C46AH is a logical "1" start bit, a 2 bit op code, a 6 bit address, and for write operations, a 16 bit data field.

READ

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT93C46AH will come out of the high impedance state, and after sending an initial dummy zero bit, will begin shifting out the 16 bits of data located at the specified address. The data bits being shifted out will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

ERASE/WRITE ENABLE AND DISABLE

The CAT93C46AH powers up in the programming disable state. Any programming after power-up or after an EWDS (programming disable) instruction must first be preceded by the EWEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT93C46AH programming and erasing functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT93C46AH regardless of the programming enable/disable status.

ERASE

Upon receiving an ERASE command and address, the device must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46AH can be determined by selecting the device and polling the DO pin. Once erased, all memory locations return to a logical "1" state.

WRITE

After receiving a WRITE command, address and data, the device must be deselected for a minimum

of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase and data store cycle of the memory register specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46AH can be determined by selecting the device and polling the DO pin. With the CAT93C46AH it is **NOT** necessary to erase a memory register before the WRITE command.

ERASE ALL

Upon receiving an ERAL command, the device must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46AH can be determined by selecting the device and polling the DO pin. Once erased, all memory locations return to logical "1" state.

WRITE ALL

Upon receiving a WRAL command and data, the device must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking write cycle to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46AH can be determined by selecting the device and polling the DO pin.

It **IS** necessary for all memory locations to be erased before the WRAL command is executed.

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CAT93C46AI - Industrial Temperature 700KHz 1K BIT SERIAL E²PROM OPERATION

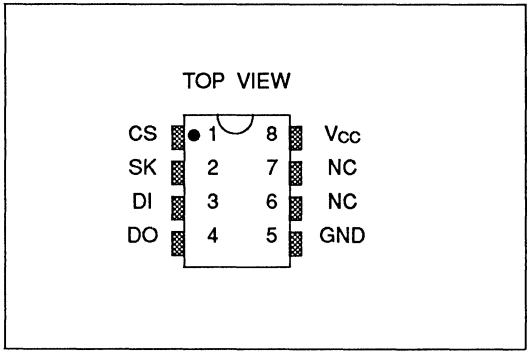
DESCRIPTION

The CAT93C46AI is an industrial temperature CMOS 1K-bit serial E²PROM with a low current drain of 3mA active and 100µA standby. It is configured as 64 registers of 16 bits each, and has been designed to interface serially with industry standard microcontrollers. Manufactured using Catalyst's advanced CMOS E²PROM floating gate technology, the device can endure 10,000 erase/write cycles and has a data retention of 10 years. The CAT93C46AI is assembled in either an 8 pin DIP or S.O. package, and will be available in a 3V version (CAT33C101AI).

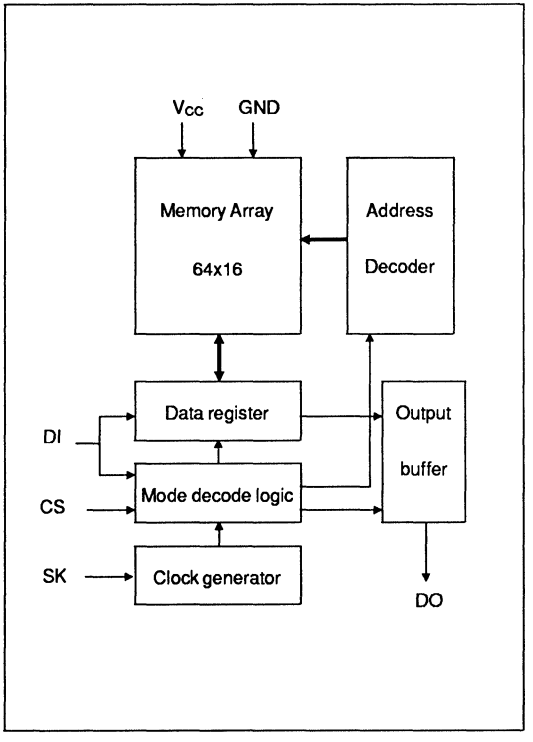
FEATURES

- High-speed 700KHz operation
- Single 5V supply
- 64x16 serial memory
- Compatible with National Semiconductor NMC 9346
- Self-timed programming cycle with Autoerase
- Word and chip-erasable
- Operating range -40°C to +85°C
- Highly reliable CMOS floating gate technology
- 10,000 erase/write cycles
- 10 year data retention
- Power-up inadvertent write protection

PIN CONFIGURATION DIP AND S.O.



BLOCK DIAGRAM



PIN FUNCTIONS

CS	Chip select
SK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
GND	Ground
NC	No connect

ABSOLUTE MAXIMUM RATINGS *

Storage temperature . . . . . -65°C to +150°C
Power supply (V_{CC}) . . . . . +7V
Voltage on any input pin . . . . . -0.3 to +7V
Voltage on any output pin . . . . . -0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC1}	Current consumption (operating)	DI = 0.0V, SK = 5.0V V_{CC} =5.0V, CS = 5.0V Outputs unloaded			4	mA
I_{CC2}	Current consumption (stand-by)	V_{CC} = 5.5V, CS = 0V DI = 0V, SK = 0V			100	µA
I_{LI}	Input leakage current	V_{IN} = 5.5V			10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V, CS = 0V			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V

INSTRUCTION SET

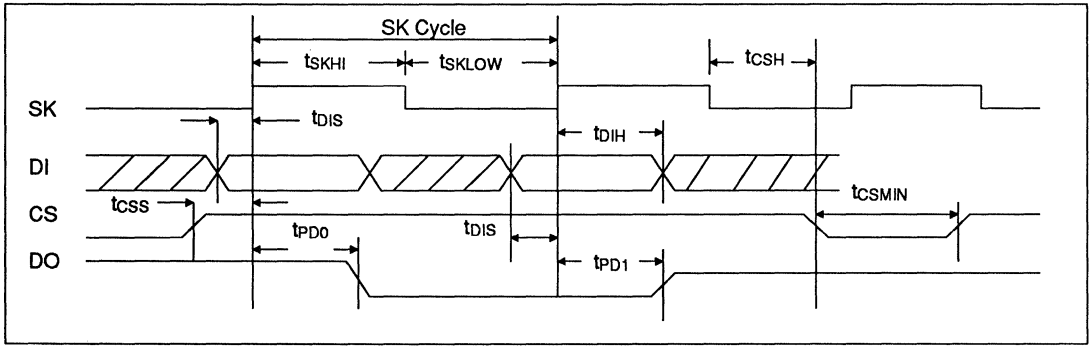
Instruction	Start Bit	Opcode	Address	Data	Comments
READ	1	1 0	A5 - A0		Read address AN - A0
ERASE	1	1 1	A5 - A0		Erase address AN - A0
WRITE	1	0 1	A5 - A0	D15 - D0	Write address AN - A0
EWEN	1	0 0	11XXXX		Program enable
EWDS	1	0 0	00XXXX		Program disable
ERAL	1	0 0	10XXXX		Erase all addresses
WRAL	1	0 0	01XXXX	D15 - D0	Program all addresses

AC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = -40°C to +85°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{CSS}	CS setup time		50			ns
t_{CSH}	CS hold time	C_L = 100pF V_{OL} = 0.8V, V_{OH} = 2.0V V_{IL} = 0.45V, V_{IH} = 2.4V	0			ns
t_{DIS}	DI setup time		100			ns
t_{DIH}	DI hold time		100			ns
t_{PD1}	Output delay to 1				500	ns
t_{PD0}	Output delay to 0				500	ns
t_{HZ}	Output delay to Hi-Z			100		ns
t_{EW}	Erase/Write pulse width				10	ms
t_{CSMIN}	Minimum CS low time		250			ns
t_{SKHI}	Minimum SK high time		100			ns
t_{SKLOW}	Minimum SK low time		660			ns
t_{SV}	Output delay to status valid	C_L = 100pF			500	ns
SK_{MAX}	Maximum clock frequency		DC		700	KHz

SYNCHRONOUS TIMINGS



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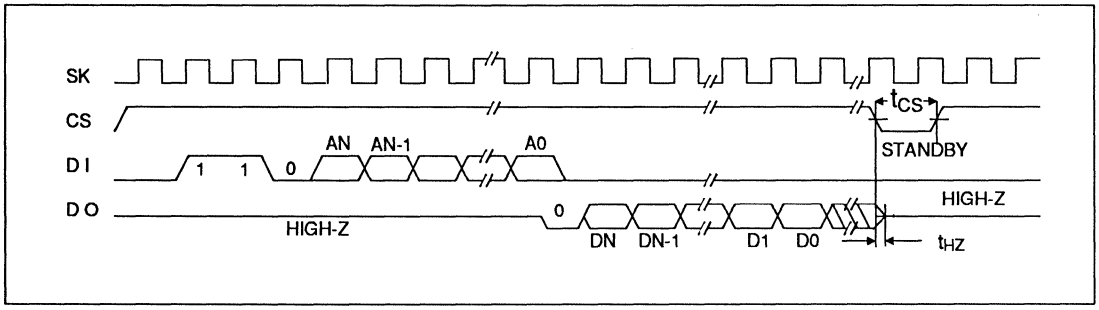

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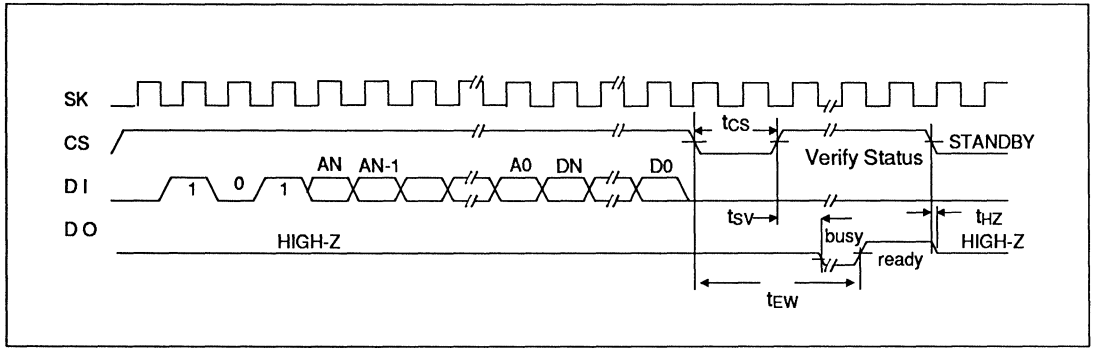

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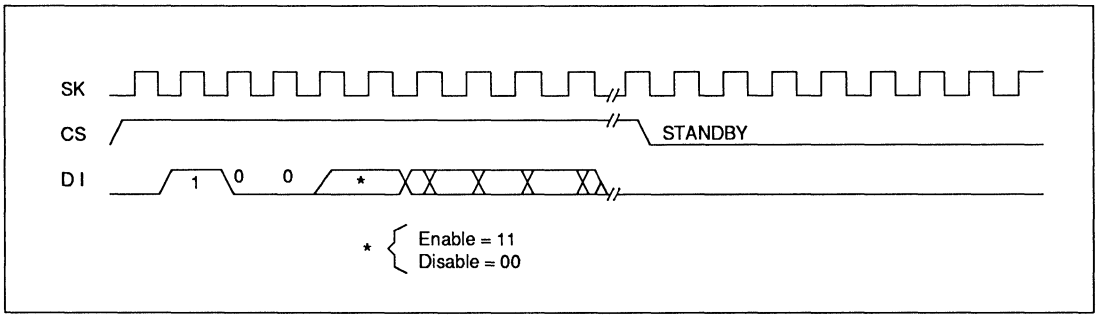

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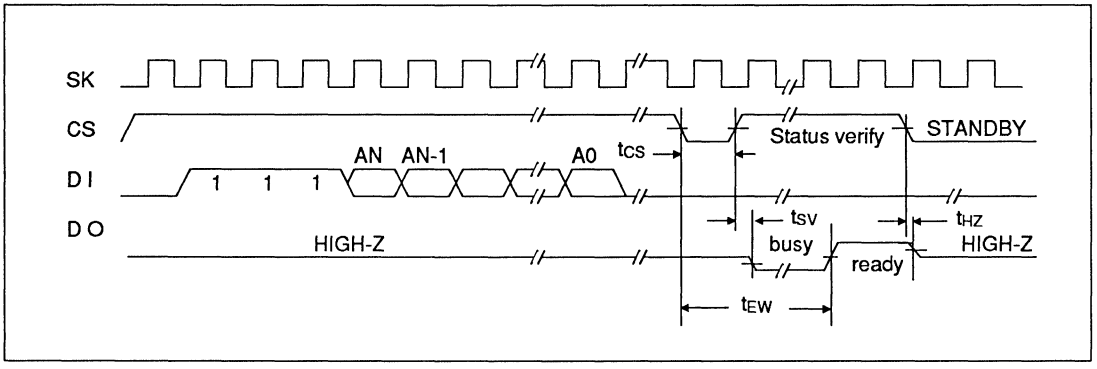

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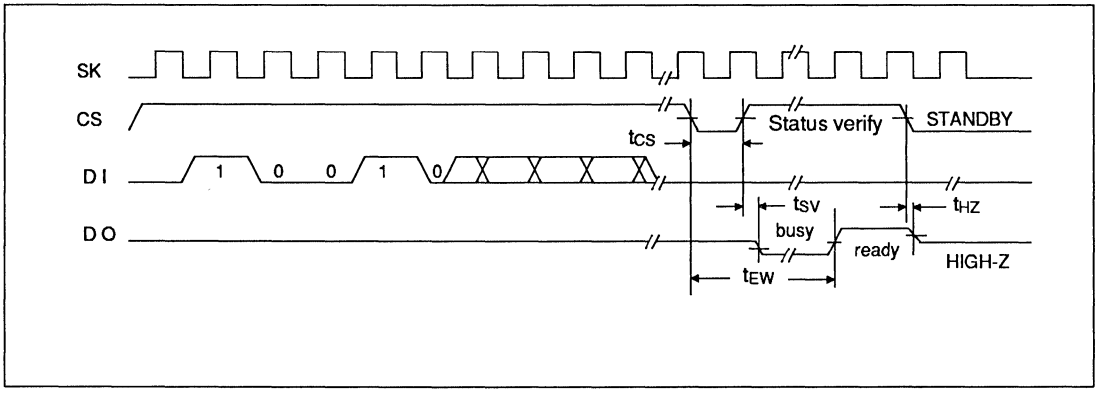
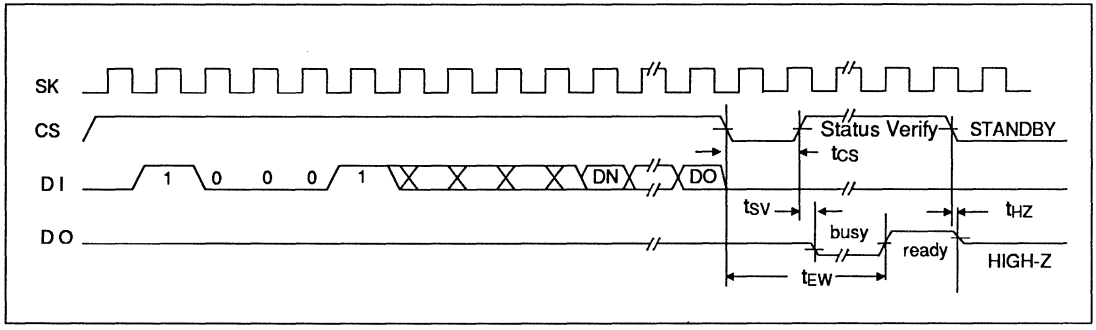


INSTRUCTION TIMING <WRAL>



DEVICE OPERATION

The CAT93C46AI is a 1024 bit nonvolatile memory intended for use with the COPS™ family of microcontrollers and designed to operate smoothly with other standard microprocessors as well. The CAT93C46AI is organized as 64 registers by 16 bits. Seven 9-bit instructions control the reading, writing and erase operations of the device. The CAT93C46AI fully operates on a single 5V supply including the programming operation. Instructions, addresses and data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin remains in a high impedance state except when reading data from the device, or when checking the ready/busy status after a programming operation. The ready/busy status can be determined after a programming operation by selecting the device and polling the DO pin; DO low indicates that the programming operation is not completed, while DO high indicates that the device is ready. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin. The format for all instructions sent to the CAT93C46AI is a logical "1" start bit, a 2 bit op code, a 6 bit address, and for write operations, a 16 bit data field.

READ

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT93C46AI will come out of the high impedance state, and after sending an initial dummy zero bit, will begin shifting out the 16 bits of data located at the specified address. The data bits being shifted out will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

ERASE/WRITE ENABLE AND DISABLE

The CAT93C46AI powers up in the programming disable state. Any programming after power-up or after an EWDS (programming disable) instruction must first be preceded by the EWEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT93C46AI programming and erasing functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT93C46AI regardless of the programming enable/disable status.

ERASE

Upon receiving an ERASE command and address, the device must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46AI can be determined by selecting the device and polling the DO pin. Once erased, all memory locations return to a logical "1" state.

WRITE

After receiving a WRITE command, address and data, the device must be deselected for a minimum

of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase and data store cycle of the memory register specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46AI can be determined by selecting the device and polling the DO pin. With the CAT93C46AI it is **NOT** necessary to erase a memory register before the WRITE command.

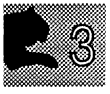
ERASE ALL

Upon receiving an ERAL command, the device must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking erase cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46AI can be determined by selecting the device and polling the DO pin. Once erased, all memory locations return to logical "1" state.

WRITE ALL

Upon receiving a WRAL command and data, the device must be deselected for a minimum of 250ns (T_{CSMIN}). The falling edge of CS will start the self clocking write cycle to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46AI can be determined by selecting the device and polling the DO pin.

It **IS** necessary for all memory locations to be erased before the WRAL command is executed.



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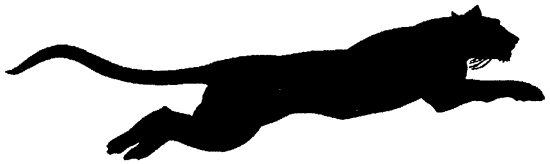


SECTION 4

E²PROMS - Secure Access

COMMERCIAL TEMPERATURE GRADE

INDUSTRIAL TEMPERATURE GRADE

CAT35C704, CAT35C704I [Industrial Temperature]

4K-bit SECURE ACCESS Serial E^2PROM

Preliminary

DESCRIPTION

The CAT35C704 is a 4K-bit Serial E^2PROM that offers a unique ***on-chip capability to safeguard stored data from unauthorized users***. Onboard E^2PROM "Access Registers" store a "password" which, once set, is used for authentication purposes prior to device operation. Two operating modes are provided: an unprotected and a password protected (secure) mode. In the unprotected mode, the CAT35C704 is a simple-to-use 4K-bit serial E^2PROM that features software memory partitioning and easy interfacing with standard microcontrollers.

In the password-protected mode, access to all or part of the device is prohibited until the correct access code has been entered. The boundary between the protected and unprotected area is user programmable. The protected area is only accessible via the correct access code, while the unprotected area allows any user READ-only access. The length of the access code is user selectable from one to eight bytes long ($\leq 1.84 \times 10^{19}$ combinations). With a 5MHz clock and 8 bytes of access code, it would take millions of years to attempt all the possible combinations.

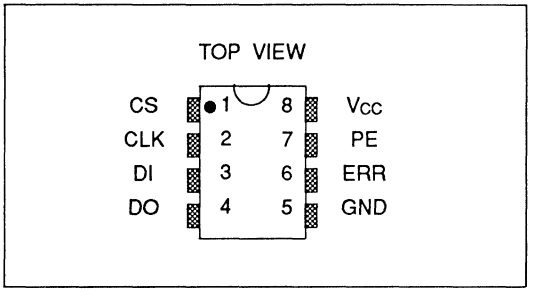
In the unprotected mode, with the use of the memory pointer, the device may be divided into read/write and read-only areas. The boundary is user programmable and can be changed without the use of an access code. This feature provides write-protection against inadvertent erasure or overwriting of data without invoking the password protection mechanism.

The CAT35C704 uses a unique ***Serial-byte*** synchronous communication protocol.

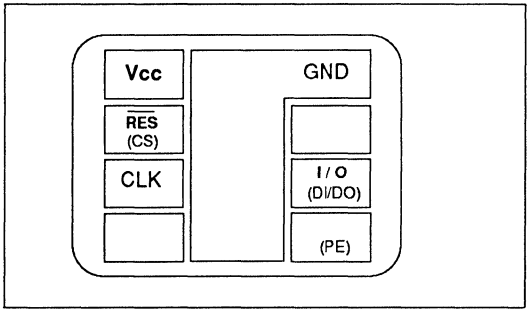
FEATURES

- Reliable 3V or 5V CMOS technology
- Password READ/WRITE - protect
- Non-password WRITE - protect
- Sequential data register READ
- User definable protected area
- Password length: 1 to 8 bytes
- Memory Array organization: x8 or x16
- High speed synchronous protocol
- Low power consumption:
  - Active: 3mA
  - Standby: 100µA
- Operating frequency: DC-5MHz
- 10 year data retention
- 10,000 write/erase cycles
- Available in 3V version

PIN OUT **DIP**



PIN OUT **CHIP-ON-BOARD (COB)**



PIN FUNCTIONS

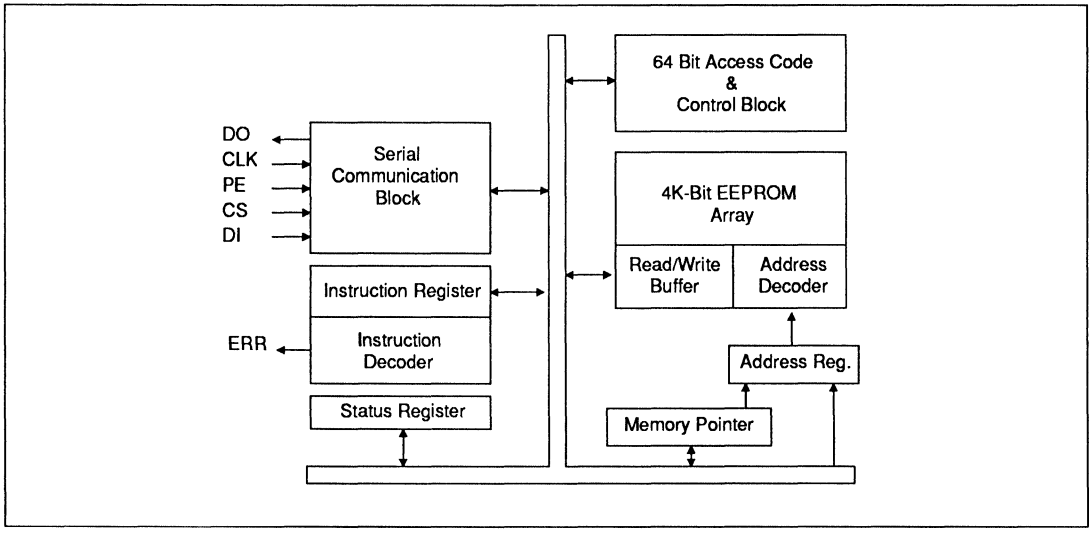
CS	Chip select	PE	Parity enable
DO *	Serial data output	ERR	Error indication pin
CLK	Clock input	Vcc	Positive power supply
DI *	Serial data input	GND	Ground

* DI,DO may be tied together to form a common I/O.

SECURE ACCESS SERIAL DEVICE FAMILY

DEVICE	OPERATING VOLTAGE	PROTOCOL	CLOCK FREQ	I/O SPEED
35C704	5V	SECS	5 MHz	5MHz
33C704	3V	SECS	5 MHz	5MHz
35C804-A	5V	UART	4.9152 MHz	9600 Baud
35C804-B	5V	UART	3.579545 MHz	9600 Baud
33C804-A	3V	UART	4.9152 MHz	9600 Baud
33C804-B	3V	UART	3.579545 MHz	9600 Baud

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature	T_{stg}	-65°C to +150°C
Power supply	V_{CC}	+7 V
Voltage on any input pin		-0.3 to +7V
Voltage on any output pin		-0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = -40°C to +85°C Industrial, 0°C to +70°C Commercial. For I_{CC} DO is unloaded.)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC}	Active Supply Current	V_{CC} =5.5V, CS = V_{CC}			3	mA
I_{SB}	Standby Supply Current	V_{CC} = 5.5V, CS = 0V DI = 0V, CLK = 0V			100	µA
V_{IL}	Input Voltage, LOW		-0.1		0.8	V
V_{IH}	Input Voltage, HIGH		2.0			V
V_{OL}	Output Voltage, LOW	I_{OL} = 2.1mA			0.4	V
V_{OH}	Output Voltage, HIGH	I_{OH} = -400µA	2.4			V
I_{LI}	Input Leakage Current	V_{IN} = 5.5V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V CS = 0V			10	µA

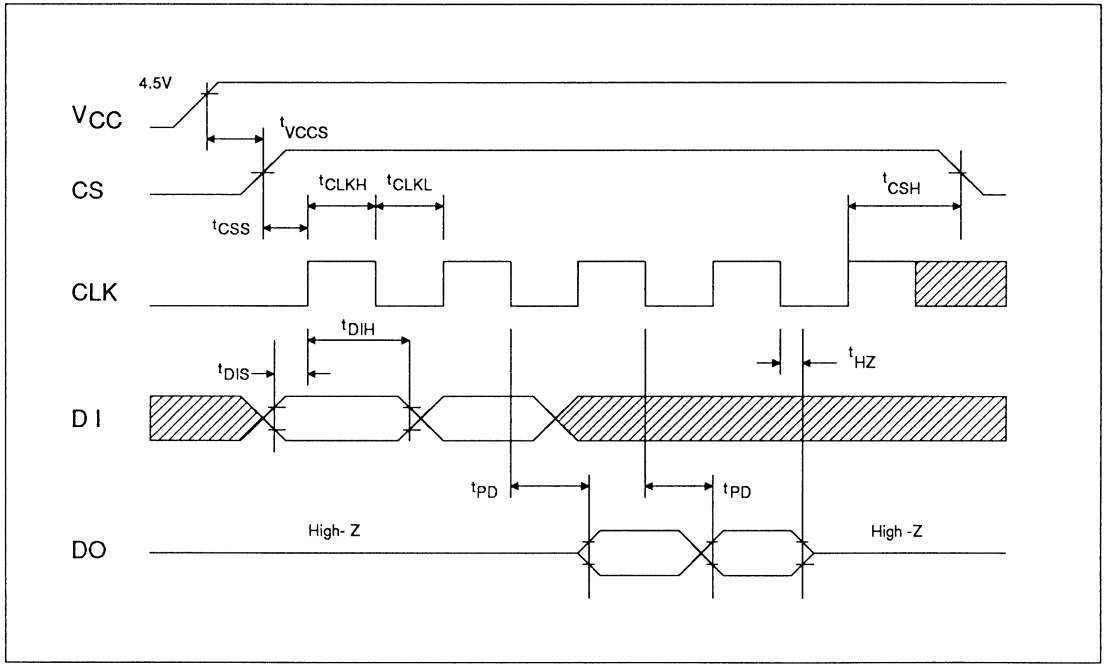
AC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = -40°C to +85°C Industrial, 0° to +70° Commercial)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{CSS}	CS setup time	C_L = 100pF V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{OH} or V_{OL}	50			ns
t_{CSH}	CS hold time		0			ns
t_{DIS}	DI setup time		50			ns
t_{DIH}	DI hold time		50			ns
t_{PD}	CLK to DO Delay				150	ns
t_{HZ} *	CLK to DO High-Z Delay				50	ns
t_{EW}	Erase/Write pulse width				10	ms
t_{CSL}	CS low pulse width		100			ns
t_{CLKH}	CLK high pulse width		100			ns
t_{CLKL}	Clock low pulse width		100			ns
t_{SV}	ERR output delay	C_L = 100pF			150	ns
t_{VCCS}	V_{CC} to CS setup time	C_L = 100pF	5			µs
f_{CLK}	Maximum clock frequency		DC		5	MHz

* t_{HZ} is measured from the falling edge of the clock to the time when the output is no longer driven.

AC TIMING



INTRODUCTION

The CAT35C704 is a 4K E^2PROM that features a password protection scheme to prevent unauthorized access to the information stored in the device. It contains an access code register which stores one to eight bytes of access code along with the length of that access code. Additionally, a memory pointer register stores the address that partitions the memory into protected and unprotected areas.

As shipped from the factory, the device is unprogrammed and unprotected. The length of the access code is equal to zero and the memory pointer register points to location zero. Every byte of the device is fully accessible without an access code. Setting a password and moving the memory pointer register to cover all or part of the memory secures the device. Once secured, the memory is divided into a read/write area and a read-only area with the entry of a valid access code. If no access code is entered, the memory is divided into a read-only area and a non-access area. Figure 1 illlustrates the partitioning of the memory arrays.

Another feature of the CAT35C704 is WRITE-protection without the use of an access code. If the memory pointer register is set to cover all or part of the memory, without setting the access code register, the device may be divided into an area which allows full access, and an area which allows READ-only access. To write into the READ-only area the user can override the memory pointer register for every WRITE instruction or he can simply move the address in the memory pointer register to uncover this area, and then WRITE into the memory. This mechanism prevents inadvertent overwriting of important data in the memory without the use of an access code. Figure 2 illustrates the partitioning of the memory areas.

To allow for convenient reading of blocks of contiguous data, the device has a READ SEQUENTIAL instruction which accepts a starting address of the block and continuously outputs data of subsequent

addresses until the end of memory, or until CHIP SELECT goes LOW.

The CAT35C704 communicates with external devices via a synchronous serial communication protocol (SECS) that has a maximum transmission rate of 5MHz. The data transmission may be a continuous stream of data or it can be packed by pulsing CHIP SELECT LOW in between each packet of information.

FIGURE 1

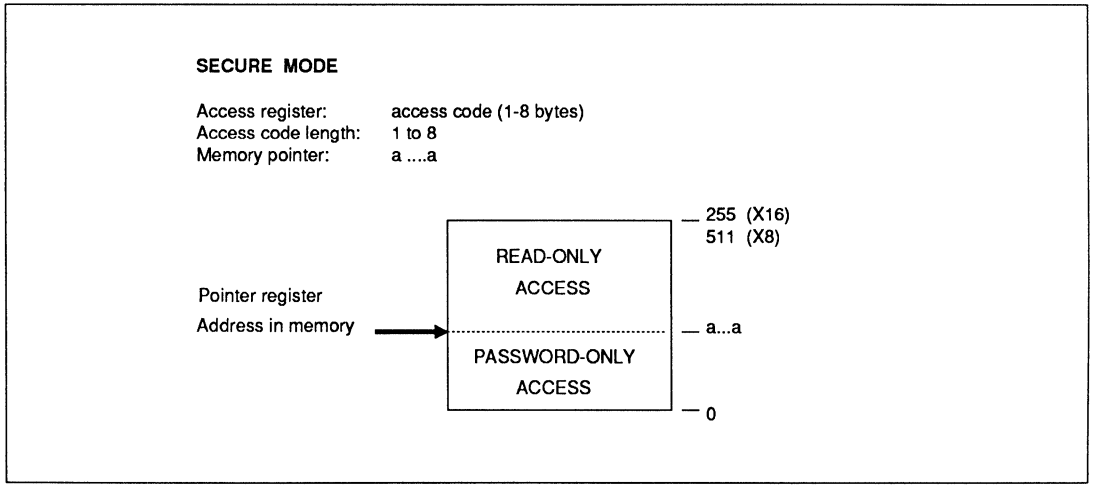
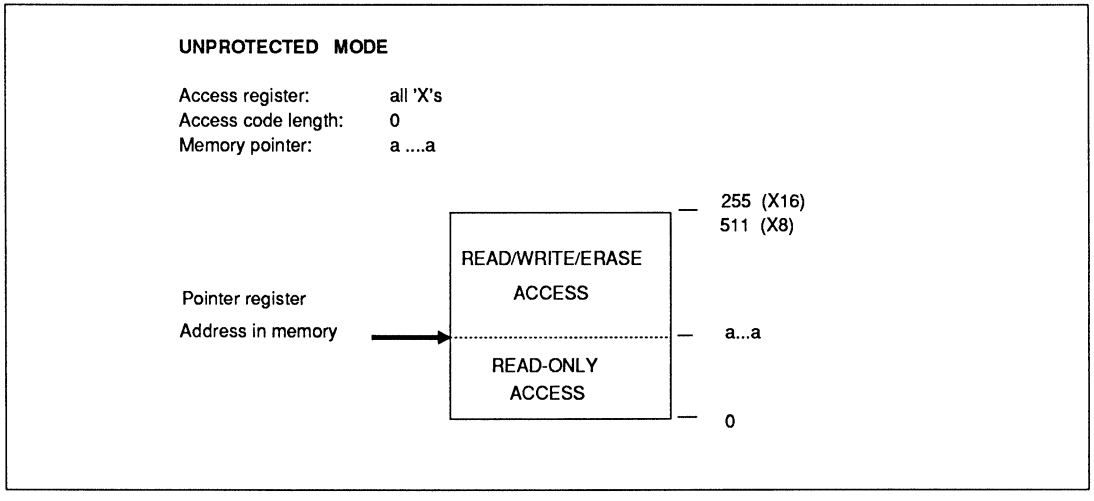


FIGURE 2



PIN DESCRIPTION

CS

Chip Select is a TTL compatible input which, when set HIGH, allows normal operation of the device. When set LOW, it resets the device, terminating all I/O communication, and puts the output in a high impedance state. CS is used to reset the device if an error condition exists or to put the device in a power-down mode to minimize power consumption. It may also be used to frame data transmission in applications where the clock and data input have to be ignored from time to time. Although CS resets the device, it does not change the write/erase or the access-enable status. These two functions, once enabled, will remain enabled until specific disabling instructions are sent or until power is removed.

CLK

The System Clock is a TTL compatible input pin that allows operation of the device over a frequency range of DC to 5MHz.

DI

The Data Input pin is TTL compatible and accepts data and instructions in a serial format. Each instruction must begin with "1" as a start bit. The device will accept as many bits as an instruction requires, including both data and address bits. With the SECS protocol, extra bits will be disregarded if they are "0's", and misinterpreted as the next instruction if they are "1's". An instruction error will cause the device to abort operation and all I/O communication will be terminated until a reset is received.

DO

The Data Output pin is a tri-state TTL compatible output. It is normally in a high impedance state unless a READ or an ENABLE BUSY instruction is executed. Following the completion of a 16-bit or 8-bit data stream, the output will return to the high impedance state. During a WRITE/ERASE cycle, if the ENABLE BUSY instruction has been previously executed, the output will stay LOW while the device is BUSY, and it will be set HIGH when the WRITE/ERASE cycle is completed. DO will stay HIGH until the completion of the next instruction's op-code and, if the next instruction is a READ, DO will output the appropriate data at the end of the instruction. If ENABLE BUSY has not been previously executed, DO will stay in a high impedance state. DO will also go to the high impedance state if an error condition is detected. If ENABLE BUSY has not been executed, to determine whether the device is in a WRITE/ERASE cycle or in an error condition, a READ STATUS instruction may be entered. When the device is in a WRITE/ERASE cycle it will output an 8-bit status word. If it does not, it is in an error condition.

PE

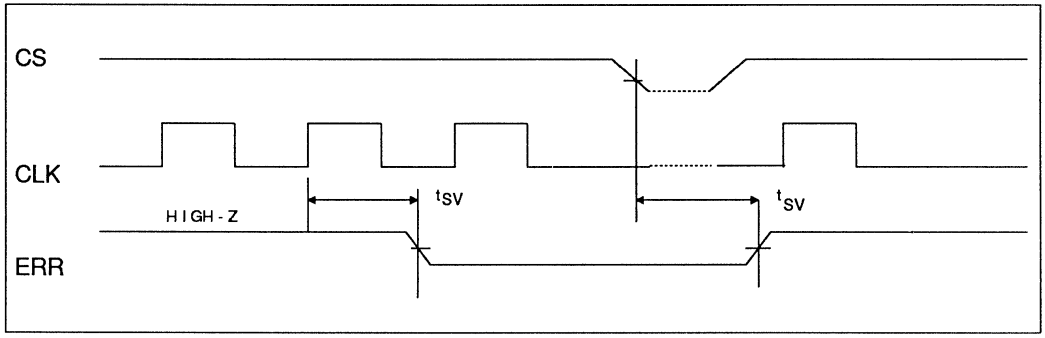
The Parity Enable pin is a TTL compatible input. If PE is set HIGH, the device will be configured to communicate using even parity, and if set LOW, it will use no parity. In this case, instructions or data that include parity bits will not be interpreted correctly.

ERR

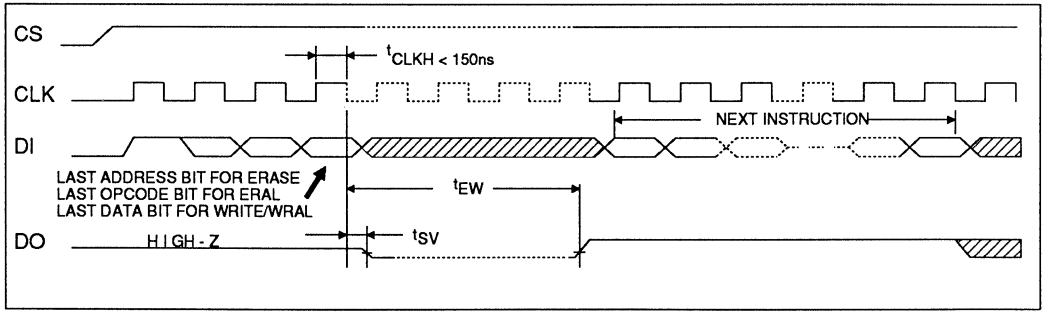
The Error indication pin is an open drain output. If either an instruction or parity error exists, the ERR pin will output a "0" until the device is reset. This can be done by pulsing CS LOW.

Note: The PE input is internally pulled down to GND (i.e. default = no parity). As with all CMOS devices, CS, CLK and DI inputs must be connected to either HIGH or LOW, and not left floating.

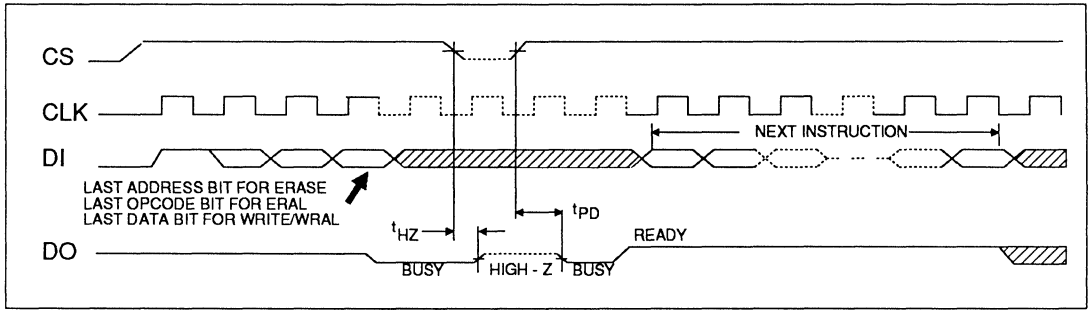
AC TIMING <ERR PIN TIMING>



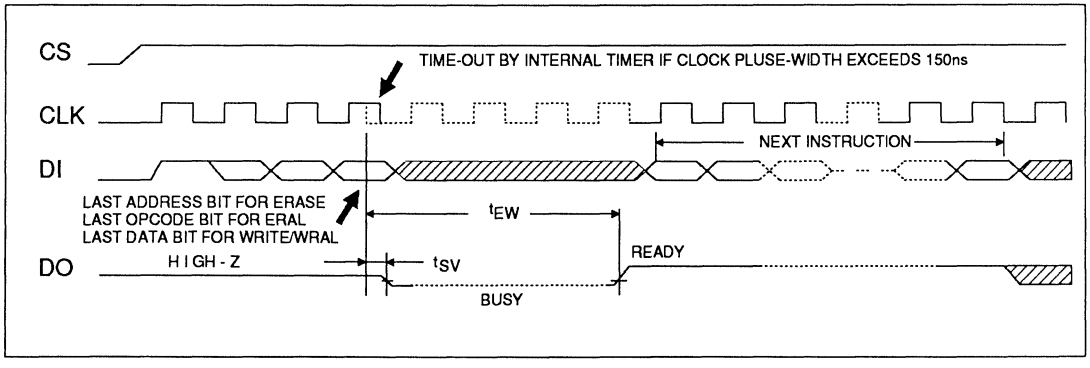
AC TIMING <t CLKH < 150 nS>



AC TIMING <CS = 0>



AC TIMING <t CLKH ≥ 150 nS>



DEVICE OPERATION

INSTRUCTIONS

The CAT35C704 instruction set includes 19 instructions.
Six instructions are related to security or write protection:

DISAC Disable Access
ENAC Enable Access
MACC Modify Access Code
OVMPR Override Memory Pointer Register
RMPR Read Memory Pointer Register
WMPR Write Memory Pointer Register

Six instructions are READ/WRITE/ERASE instructions:

ERAL Erase All
ERASE ERASE memory
READ READ memory
RSEQ Read Sequentially
WRAL Write All
WRITE WRITE memory

Seven instructions are used as control and status functions:

DISBSY Disable Busy
ENBSY Enable Busy
EWEN Erase/Write Enable
EWDS Erase/Write Disable
NOP No Operations
ORG Select Memory Organization
RSR Read Status Register

The SECS protocol supports an even parity bit if the PE pin of the device is set HIGH, otherwise there is no parity. If PE is set LOW and the incoming instruction contains a parity bit, it will be interpreted as the start bit of the next instruction. When PE is HIGH, the CAT35C704 expects a parity bit at the end of every incoming instruction. For example, the RSEQ instruction looks like this:

1100 1011 A15 ...A8 A7 ...A0 Parity-bit

Once sent, the device outputs data continuously until it reaches the end of memory. The last byte of data within this instruction contains 9 bits, with the ninth bit being the parity bit. However, if the RSEQ instruction is terminated by CS being LOW, then the output will go to high impedence without producing a parity bit.

UNPROTECTED MODE

As shipped from the factory, the CAT35C704 is in the unprotected mode. The code length is set to 0, and the memory pointer is at address 00 hex. While in this mode, any portion of the E^2PROM array can be read or written to without an access code. A portion of the memory may be protected from any write or erase operation by setting the memory pointer to the appropriate address via WMPR (Write Memory Pointer Register):

WMPR [address]

As shown previously in Figure 2, memory locations at or below the address set in the memory pointer will be write/erase protected. Thus, unintentional erasure or overwriting of data in this area will be prevented, while memory locations above the protected area still allow full access.

SECURE MODE

As shown previously in Figure 1, in the secure mode, memory locations above the address set in the memory pointer allow READ-only access. Memory locations at or below that address will require an access code before they can be accessed. The secure mode is activated with an MACC (Modify Access Code) instruction followed by a user access code which can be one to eight bytes in length.

EWEN
MACC [access code]
[access code]

The EWEN instruction enables the device to perform WRITE/ERASE operations. The access code must be entered twice for verification. If the device already has an access code, the old access code must be entered before the new access code can be accepted.

Once the secure mode is activated, access to memory locations is under software control. Access (read, write, and erase operations) to the memory locations below the address in the memory pointer must start with the ENAC (Enable Access) instructions followed by the correct access code.

ENAC [access code]
EWEN
WRITE [address][data]

The ENAC instruction, along with the access code, enables access to the protected area of the device. The EWEN instruction enables execution of the WRITE operation. This portion of the memory is otherwise inaccessible for any operation. Read-only access is allowed without the access code for memory locations above the address in the memory pointer.

The access code can be changed by the following instruction :

ENAC [old access code]
EWEN
MACC [old access code]
[access code][access code]

A two-tier protection scheme is implemented to protect data against inadvertent overwriting or erasure. To write to the memory, an EWEN (Erase/Write Enable) must first be issued. The CAT35C704 will now allow write/erase operations to be performed only on memory locations above the address set in the memory pointer. The remaining portion of the memory is still protected. To override this protection, an OVMPR (Override Memory Pointer Register -- see Memory Pointer Register) must be issued for every write/erase instruction which accesses the protected area :

ENAC [access code]
EWEN
OVMPR
WRITE [address][data]

As an alternative to the OVMPR instruction, the WMPR (Write Memory Pointer Register) instruction may be used to move the memory pointer address to uncover the area where writing is to be performed:

ENAC [access code]
EWEN
WMPR
WRITE [address][data]

As shipped from the factory, the device is in the unprotected mode. The length of the access code is user selectable from a minimum of one byte to a maximum of eight bytes (> 1.84×10^{19} combinations). Loading a zero-length access code will disable protection.

MEMORY POINTER REGISTER

The memory pointer enables the user to segment the E^2PROM array into two sections. While in the unprotected mode, the array can be segmented between read-only and full access. While in the secure mode, the memory may be segmented between read-only access and password-only access. Three instructions are dedicated to the memory pointer operations. The first one is WMPR (Write Memory Pointer Register). This instruction, followed by an address, will load (or reload) the memory pointer register with a new address. This address will be stored in the E^2PROM and can be modified only by another WMPR instruction. If the device is in the secure mode, this instruction must be preceded by the ENAC instruction and the valid access code. The second instruction is OVMPR (Override Memory Pointer Register) which allows a single write/erase to be performed to memory locations at or below the address set in the memory pointer. This instruction allows the user to modify data in a segmented array without having to move the memory pointer. Once the operation is complete, the device returns to the protected mode. The third instruction is the RMPR (Read Memory Pointer Register) which will place the current contents of the register in the serial output buffer. If the device is in the secure mode, ENAC and a valid access code are needed before the RMPR instruction can be implemented.

SECS PROTOCOL

The CAT35C704 implements the SECS communication protocol which uses an 8-bit transmission format. As shown in Figures 3-9, all instructions are 8-bits long with the first bit being the start bit and the following 7 bits being the op-code. Data can be one or two bytes long depending on the instruction and the memory array organization. By the same token each address is one or two bytes long depending on the organization of the memory array. In this protocol, the transmission of the MSB is always first and the LSB last. The CS (Chip Select) of the CAT35C704 may be used to frame the data transmission packet or it may be set HIGH for the entire duration of operation. If an error in op-code or parity (if enabled) has been detected, the ERR output will be set LOW and the CAT35C704 will stop receiving

and sending data until CS is toggled from HIGH to LOW and to HIGH again. Alternatively, an error condition may be detected by interrogating the device for a status word. If an error condition has been detected, no response will come from DO (Data Output). DO may be programmed to become tri-stated or to output a READY/BUSY status flag during write/erase cycles (see ENBSY instruction).

STATUS REGISTER

An eight bit status register is provided to allow the user to determine the status of the CAT35C704. The contents of the first three bits of the register are 101 which allows the user to quickly determine whether the device is listening or is in an error condition. The next three bits indicate the status of the device such as ready/busy, instruction error, or parity error (if either or both existed in the previous instruction.) The last two bits are reserved for future use.

ERASE ALL AND WRITE ALL

As a precaution, the ERAL and WRAL instruction has to be entered twice before it is executed. This measure is required as a redundancy check on the incoming instruction for possible transmission errors.The WRAL instruction requires sending an ERAL first (this sets a flag only) and then the WRAL instruction. The CAT35C704 will accept the following commands:

ERAL ERAL
ERAL will be executed

ERAL WRAL
WRAL will be executed

THE PARITY BIT

The SECS protocol supports an even parity bit if the PE pin of the device is set HIGH, otherwise, there is no parity. If PE is set LOW and the incoming instruction contains a parity bit, it will be interpreted as the start bit of the next instruction. When PE is HIGH, the CAT35C704 expects a parity bit at the end of every incoming instruction. For example, the RSEQ instruction will look like this :

1100 1011 A15 ..A8 A7 ...A0 Parity-bit

The device then outputs data continuously until it reaches the end of the memory. The last byte of data contains 9 bits. The ninth bit is the parity bit. However, if the RSEQ instruction is terminated by CS being LOW, then the output will go into HIGH Z without producing a parity bit.

SYSTEM ERRORS

Whenever an error occurs, be it an instruction error (unknown instruction), or parity error (perhaps caused by transmission error), the device will stop its operation. To return to normal operation, the device must be reset by pulsing CS LOW and then set back to HIGH. Resetting the device will not affect the ENAC, EWEN and ENBSY status. The error may be determined by entering the READ STATUS REGISTER (RSR) instruction. The status output is an 8-bit word with the first three bits being 101. This three bit pattern indicates that the device is out of the error condition. The fourth bit is "1" if an instruction error occurred. The fifth bit is a "1" if a parity error occurred. The sixth bit is a "1" if the device is in a WRITE/ERASE cycle. The last two bits are reserved for future use. The reason for having the "101" pattern is that if the device is in a WRITE/ERASE cycle and the ENBSY (ENABLE BUSY) instruction has not been previously executed, the device will appear to be in the error condition. If the device is in the error condition, it will not respond to any input instruction from DI. However, if the device is in a WRITE/ERASE cycle, it will respond to the RSR instruction by outputting "101 001 00". If the RSR is executed at the end of the WRITE/ERASE cycle, the output will be "101 000 00".

Figure 3 <READ TIMING>

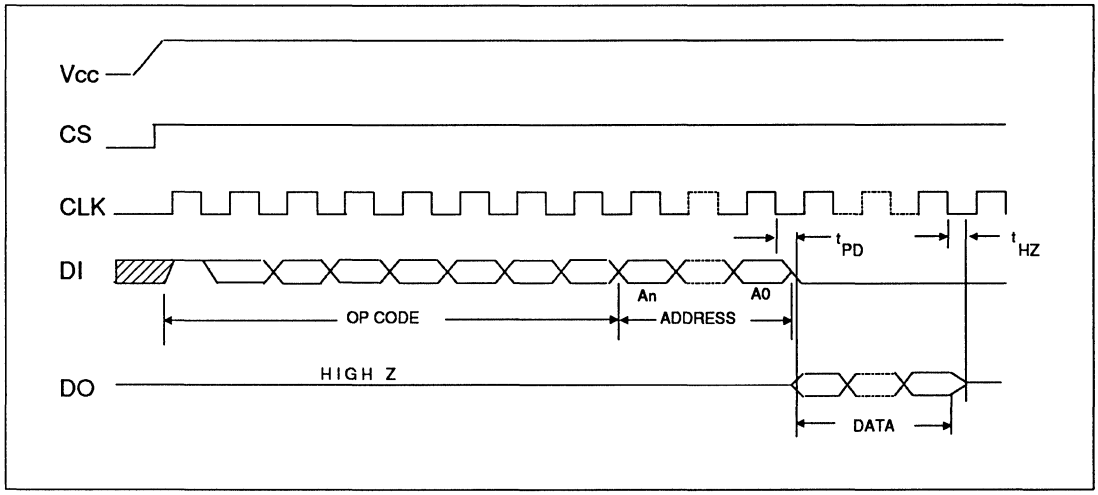


Figure 4 <WRITE TIMING>

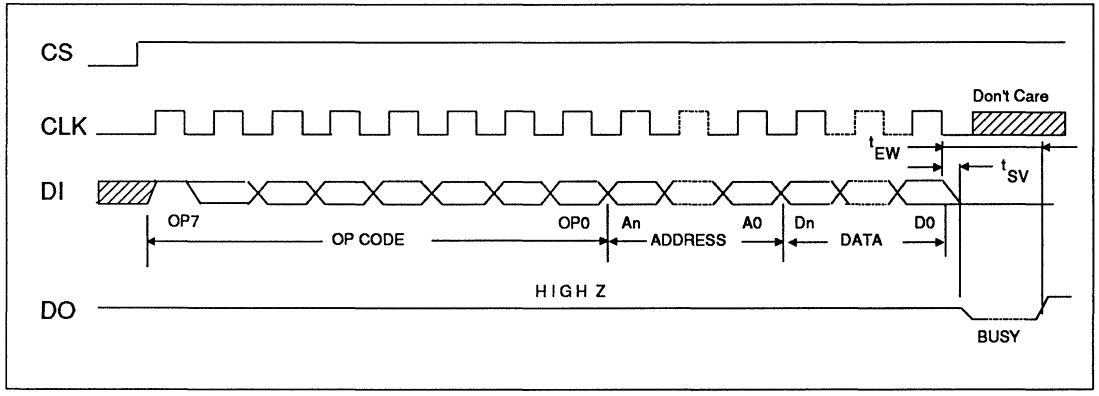


Figure 5 <EWEN/EWDS TIMING>

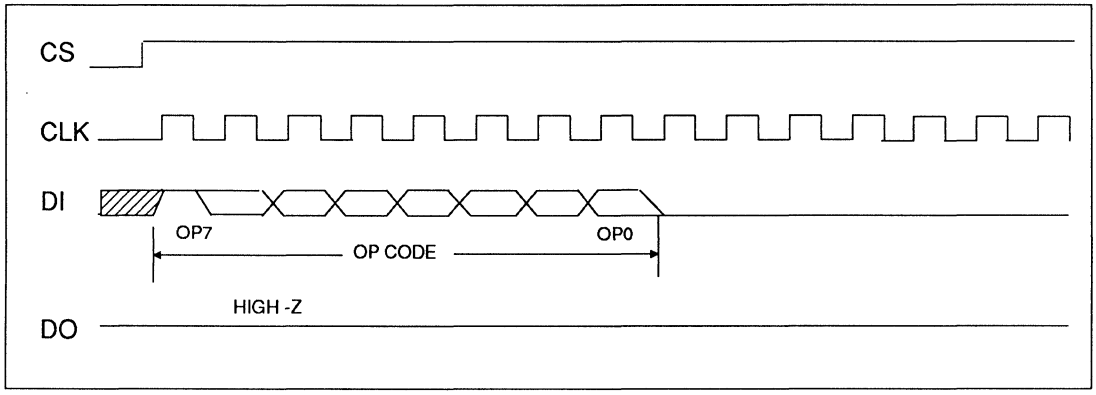


Figure 6 <ERASE TIMING>

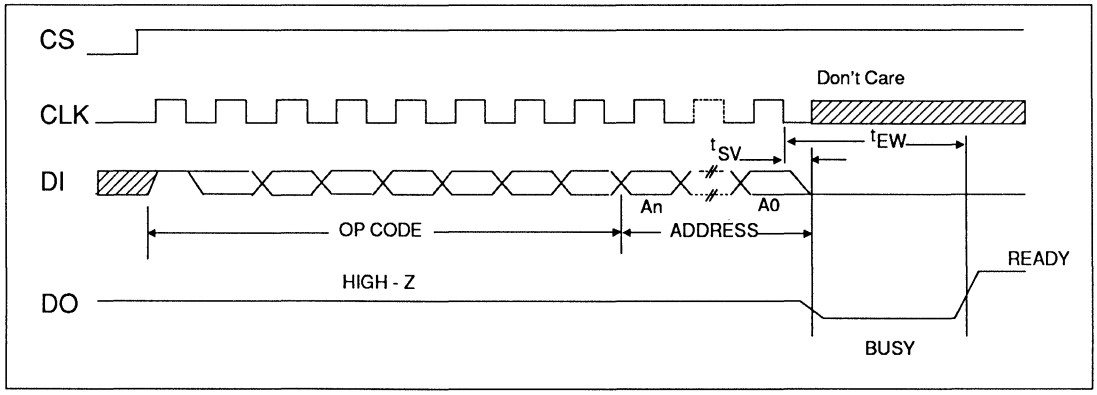


Figure 7 <ERAL TIMING>

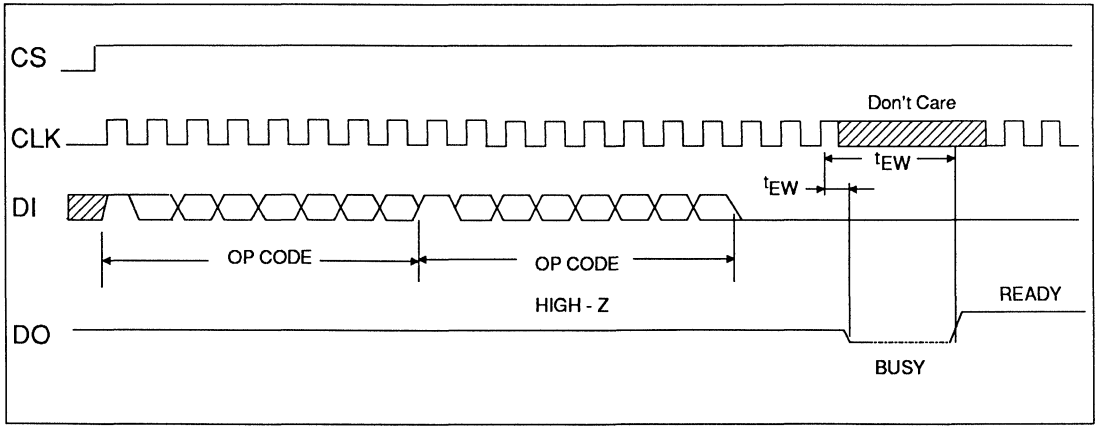


Figure 8 <WRAL TIMING>

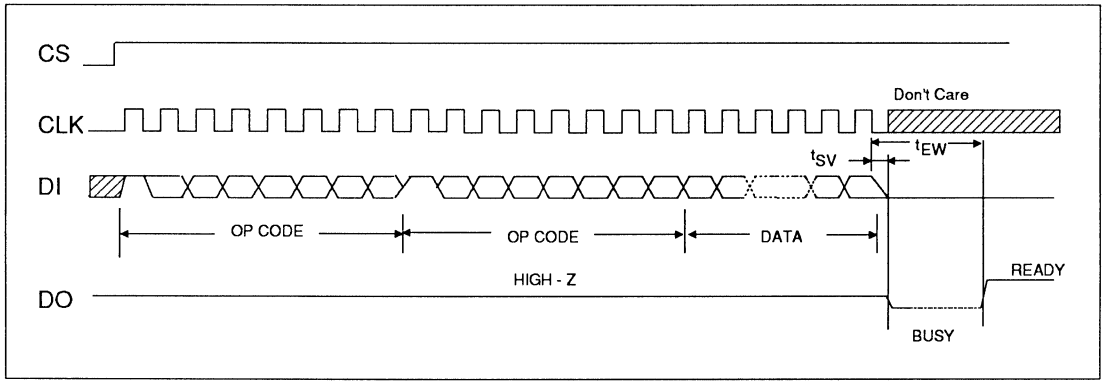
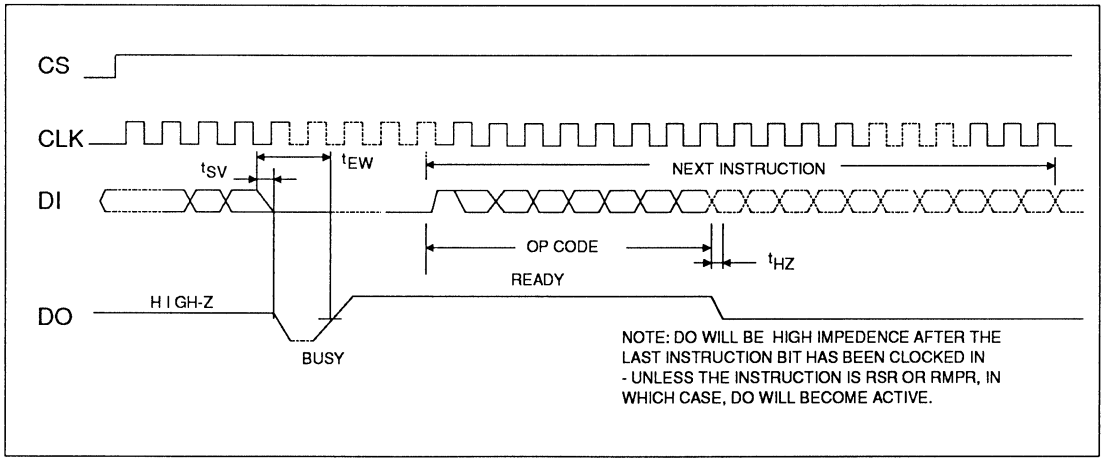


Figure 9 <WRITE TIMING>



INSTRUCTION SET

DISAC Disable Access
1000 1000

This instruction will lock the memory from all write/erase operations regardless of the contents of the memory pointer. A write can be accomplished only by first entering the ENAC instruction followed by a valid access code.

ENAC Enable Access
1100 0101
[access code]
[access code]

In the protected mode, this instruction, followed by a valid access code, unlocks the device for read/write/erase access.

WMPR Write Memory Pointer Register
1100 0100 [Addr 15-8] [Addr 7-0]
(for x8 organization)
1100 0100 [Add 7-0]
(for x16 organization)

The WMPR instruction followed by 8 or 16 bits of address (depending on the organization) will move the pointer to the newly specified address.

MACC Modify Access Code
1101 NNNN [Old access code]
[New access code] [New access code]

This instruction requires the user to enter the old access code, if one was set previously, followed by the new access code and a re-entry of the new access code for verification. Within the instruction format, the variable NNNN designates the length of the access code as the following :

NNNN = [0] No access code. Set device to unprotected mode.
NNNN = [1-8] Length of access code is 1 to 8 bytes.
NNNN = [>8] Illegal number of bytes. The CAT35C704 will ignore the rest of the transmission.

RMPR Read Memory Pointer Register
11001010

Output the content of the memory pointer register to the serial output port.

OVMPR Override Memory Pointer Register
1000 0011

Override the memory protection for the next instruction.

READ Read Memory
1100 1001[Addr 15-8][Addr 7-0]
(for x8 organization)
1100 1001[Addr 7-0]
(for x16 organization)

Output the contents of the addressed memory location to the serial port.

WRITE Write memory
1100 0001[Addr 15-8][Addr 7-0]
[Data 7-0]
1100 0001[Addr 7-0][Data 15-8]
[Data 7-0]

WRITE the 8-bit or 16-bit data to the addressed memory location. After the instruction, address, and data have been entered, the self-timed WRITE sequence will start. The addessed memory location will be erased before data is written. The DO pin may be used to output the RDY/BUSY status by having previously entered the ENBSY instruction. During the write cycle, DO will output a LOW for BUSY during the write cycle and a HIGH for READY after the cycle has been completed.

ERASE Erase Memory
1100 0000
[Addr 15 -8] [Addr 7-0]
(for x8 organization)
1100 0000
[Addr 7-0]
(for x16 organization)

Erase data in the specified memory location (set memory to "1"). After the instruction and the address have been entered, the self-timed erase sequence will start. The DO pin may be used to output the READY/BUSY status by having previously entered the ENSBY instruction. During the erase cycle, DO will output a LOW for BUSY during the write cycle

and a HIGH for ready after the cycle has been completed.

ERAL Erase All
1000 1001
1000 1001

Erase the data of all memory locations (all cells can be set to "1"). For protection against inadvertent chip erase, the ERAL instruction is required to be entered twice.

WRAL Write All
1000 1001
1100 0011 [Data 15-8] [Data 7-0]
(for x16 organization)
1000 1001
1100 0011 [Data 7-0]
(for x8 organization)

Write one or two bytes of data to all memory locations. An ERAL will be automatically performed before the WRAL is executed. For protection against inadvertent overwriting of data, the ERAL instruction is required to be entered preceding the WRAL instruction.

RSEQ Read Sequentially
1100 1011
[Addr 15-8] [Addr 7-0]
(for x8 organization)
1100 1011
[Addr 7-0] (for x16 organization)

Read memory starting from specified address, n, then n+1, etc, to the highest address or until CS goes LOW. The instruction will be terminated when CS goes LOW.

ENBSY Enable Busy
1000 0100

Enable the status indicator on DO during write/erase cycle. DO goes LOW then HIGH once the write cycle is complete. DO will go to HIGH-Z at the end of the next op code transmission.

DISBSY Disable Busy
1000 0101

Disable the status indicator on DO during write/erase cycle

EWEN Erase/Write Enable
1000 0001

Enable erase/write to be performed on non-protected portion of memory. This instruction must be entered before any write/erase instruction. Once entered, it will remain valid until power-down or an EWDS (Erase/Write Disable) is executed.

EWDS Erase/Write Disable
1000 0010
Disable all erase and write functions

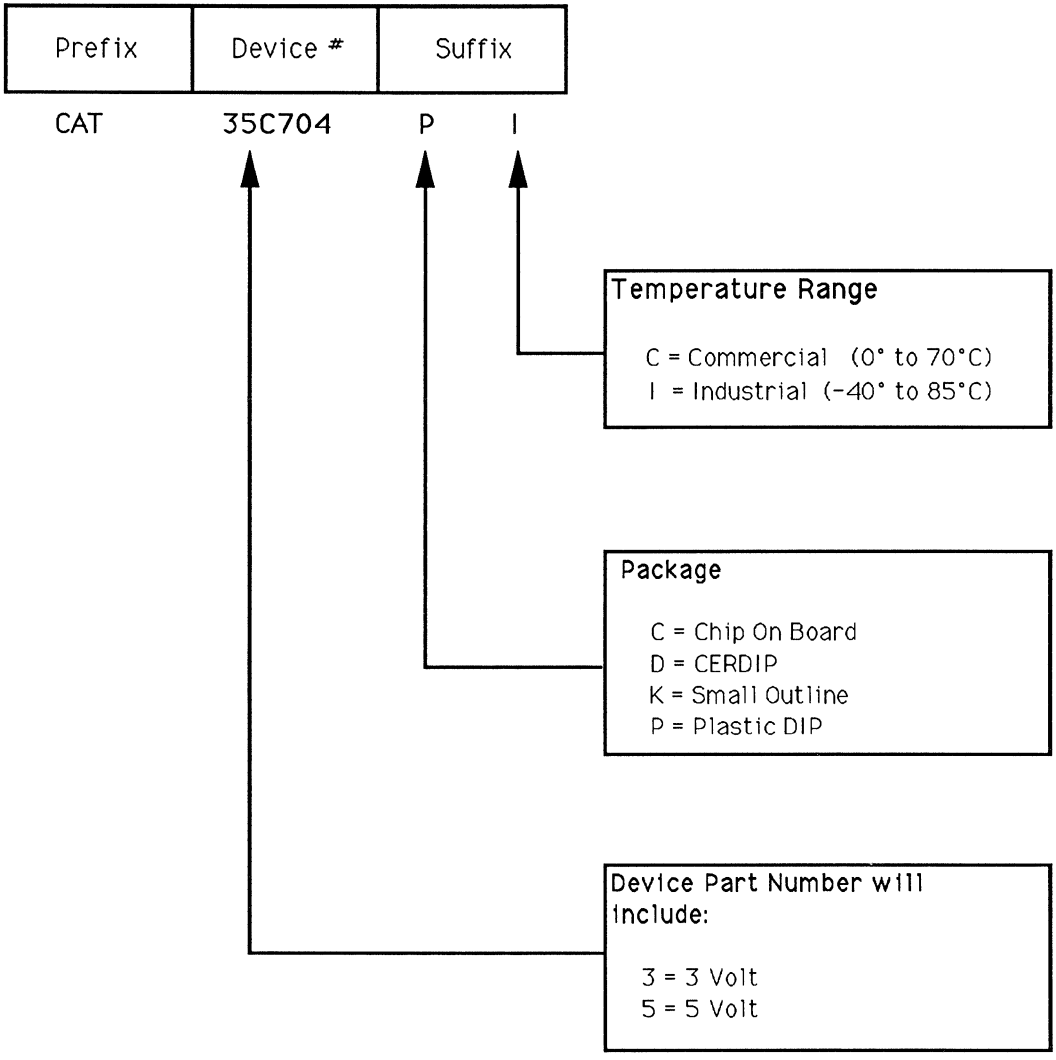
ORG Select Memory Organization
1000 011R (where R = 0 or 1)
Set memory organization
to 512x8 if R = 0.
Set memory organization
to 256x16 if R = 1.

RSR Read Status Register
1100 1000

Output the contents of the 8-bit status register. The contents of first three bits of the register is 101 which allows the user to quickly determine whether the device is listening or is in an error condition. The next three bits indicate the status such as ready/busy or, if an error existed in the previous instruction, instruction error or parity error. The last two bits are reserved for future use.

NOP No Operation
1000 0000
No Operation

ORDERING INFORMATION



CAT35C804A/B, CAT35C804AI/BI [Industrial Temperature]

4K-bit SECURE ACCESS Serial E^2PROM Preliminary

DESCRIPTION

The **CAT35C804** is a 4K-bit Serial E^2PROM that offers a unique ***on-chip capability to safeguard stored data from unauthorized users.*** Onboard E^2PROM "Access Registers" store a "password" which, once set, is used for authentication purposes prior to device operation. Two operating modes are provided: an unprotected and a password protected (secure) mode. In the unprotected mode, the **CAT35C804** is a simple-to-use 4K-bit serial E^2PROM that features software memory partitioning and easy interfacing with standard microcontrollers.

In the password-protected mode, access to all or part of the device is prohibited until the correct access code has been entered. The boundary between the protected and unprotected area is user programmable. The protected area is only accessible via the correct access code, while the unprotected area allows any user READ-only access. The length of the access code is user selectable from one to eight bytes long ($\leq 1.84 \times 10^{19}$ combinations). With a 4.9152 MHz (or 3.579545 MHz) clock and 8 bytes of access code, it would take billions of years to attempt all the possible combinations.

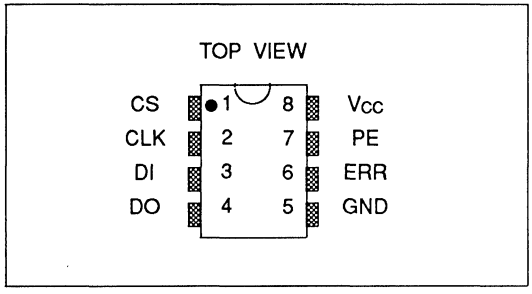
In the unprotected mode, with the use of the memory pointer, the device may be divided into read/write and read-only areas. The boundary is user programmable and can be changed without the use of an access code. This feature provides write-protection against inadvertent erasure or overwriting of data without invoking the password protection mechanism.

The CAT35C804 uses a UART- compatible asynchronous protocol.

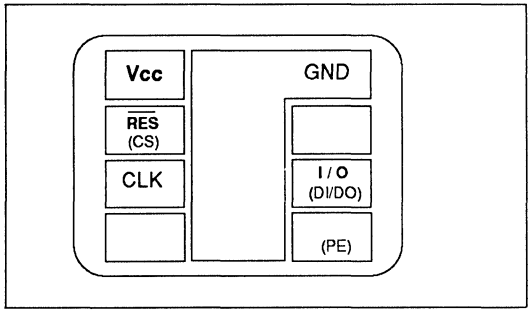
FEATURES

- Reliable 3V or 5V CMOS technology
- Password READ/WRITE - protect
- Non-password WRITE - protect
- Sequential data register READ
- User definable protected area
- Password length: 1 to 8 bytes
- Memory Array organization: x8 or x16
- UART compatible asynchronous protocol
- Low power consumption:
  - Active: 3mA
  - Standby: 100µA
- 10 year data retention
- 10,000 write/erase cycles
- Available in 3V version

PIN OUT **DIP**



PIN OUT **CHIP-ON-BOARD (COB)**



PIN FUNCTIONS

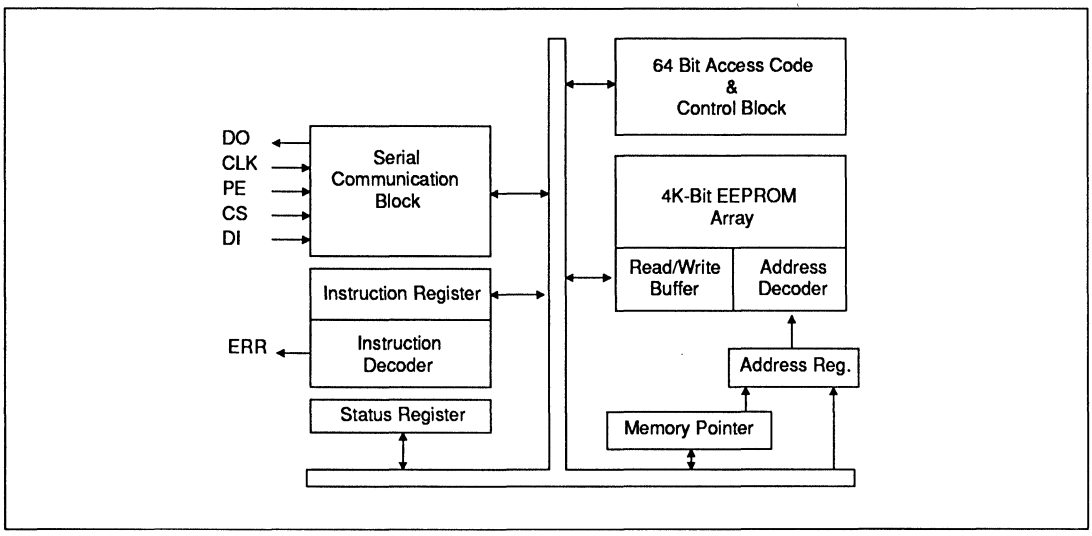
CS	Chip select	PE	Parity enable
DO *	Serial data output	ERR	Error indication pin
CLK	Clock input	Vcc	Positive power supply
DI *	Serial data input	GND	Ground

* DI,DO may be tied together to form a common I/O.

SECURE ACCESS SERIAL DEVICE FAMILY

DEVICE	OPERATING VOLTAGE	PROTOCOL	CLOCK FREQ	I/O SPEED
35C704	5V	SECS	5 MHz	5MHz
33C704	3V	SECS	5 MHz	5MHz
35C804-A	5V	UART	4.9152 MHz	9600 Baud
35C804-B	5V	UART	3.579545 MHz	9600 Baud
33C804-A	3V	UART	4.9152 MHz	9600 Baud
33C804-B	3V	UART	3.579545 MHz	9600 Baud

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature	T_{stg} . . . . . -65°C to +150°C
Power supply	V_{CC} . . . . . +7 V
Voltage on any input pin	. . . . . -0.3 to +7V
Voltage on any output pin	. . . . . -0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = -40°C to +85°C Industrial, 0°C to +70°C Commercial. For I_{CC} DO is unloaded.)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC}	Active Supply Current	V_{CC} =5.5V, CS = V_{CC}			3	mA
I_{SB}	Standby Supply Current	V_{CC} = 5.5V, CS = 0V DI = 0V, CLK = 0V			100	µA
V_{IL}	Input Voltage, LOW		-0.1		0.8	V
V_{IH}	Input Voltage, HIGH		2.0			V
V_{OL}	Output Voltage, LOW	I_{OL} = 2.1mA			0.4	V
V_{OH}	Output Voltage, HIGH	I_{OH} = -400µA	2.4			V
I_{LI}	Input Leakage Current	V_{IN} = 5.5V			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V CS = 0V			10	µA

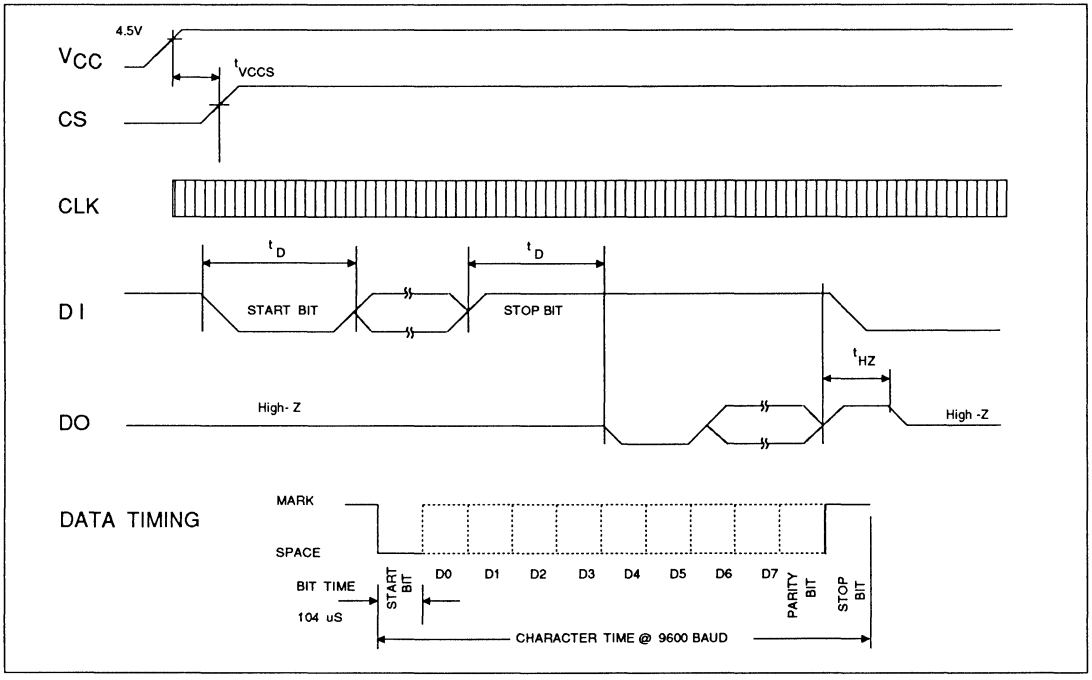
AC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = -40°C to +85°C Industrial, 0° to +70° Commercial)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{CSH}	CS hold time	C_L = 100pF V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{OH} or V_{OL}	0			ns
t_D	DATA Bit Time			104		µs
t_{PD}	CLK to DO Delay				150	ns
t_{HZ} *	CLK to DO High-Z Delay				55	µs
t_{EW}	Erase/Write pulse width				10	ms
t_{CSL}	CS low pulse width		100			ns
t_{SV}	ERR output delay	C_L = 100pF			150	ns
t_{VCCS}	V_{CC} to CS setup time	C_L = 100pF	5			µs
f_{CLK}	Maximum clock frequency		DC		5	MHz

* t_{HZ} is measured from the falling edge of the clock to the time when the output is no longer driven.

AC TIMING



INTRODUCTION

The CAT35C804 is a 4K E^2PROM that features a password protection scheme to prevent unauthorized access to the information stored in the device. It contains an access code register which stores one to eight bytes of access code along with the length of that access code. Additionally, a memory pointer register stores the address that partitions the memory into protected and unprotected areas.

As shipped from the factory, the device is unprogrammed and unprotected. The length of the access code is equal to zero and the memory pointer register points to location zero. Every byte of the device is fully accessible without an access code. Setting a password and moving the memory pointer register to cover all or part of the memory secures the device. Once secured, the memory is divided into a read/write area and a read-only area with the entry of a valid access code. If no access code is entered, the memory is divided into a read-only area and a non-access area. Figure 1 illustrates the partitioning of the memory arrays.

Another feature of the CAT35C804 is WRITE-protection without the use of an access code. If the memory pointer register is set to cover all or part of the memory, without setting the access code register, the device may be divided into an area which allows full access, and an area which allows READ-only access. To write into the READ-only area the user can override the memory pointer register for every WRITE instruction or he can simply move the address in the memory pointer register to uncover this area, and then WRITE into the memory. This mechanism prevents inadvertent overwriting of important data in the memory without the use of an access code. Figure 2 illustrates the partitioning of the memory areas.

To allow for convenient reading of blocks of contiguous data, the device has a READ SEQUENTIAL instruction which accepts a starting address of the

block and continuously outputs data of subsequent addresses until the end of memory or until CHIP SELECT goes LOW.

The CAT35C804 communicates with external devices via an asynchronous serial communication protocol. The data transmission may be a continuous stream of data or it can be packed by pulsing CHIP SELECT LOW in between each packet of information.

FIGURE 1

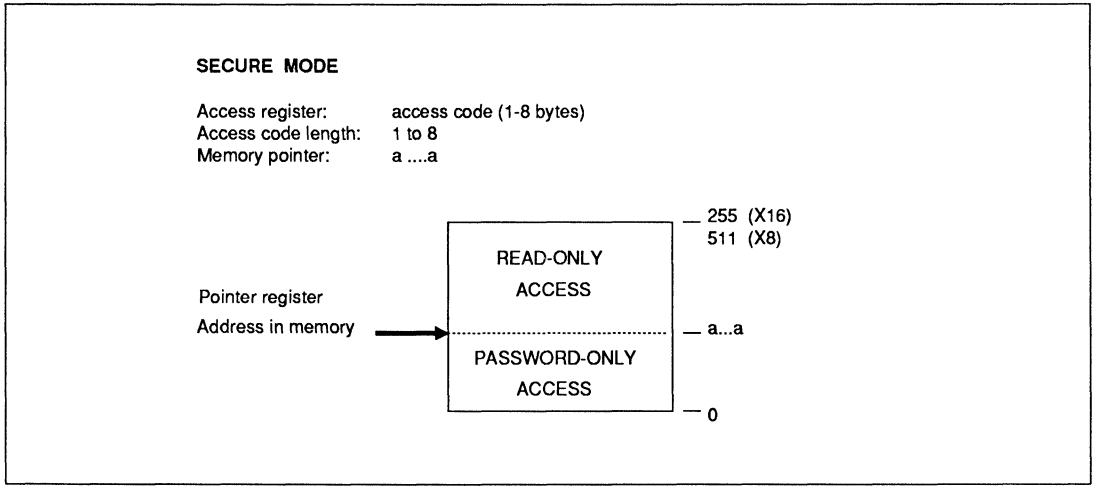
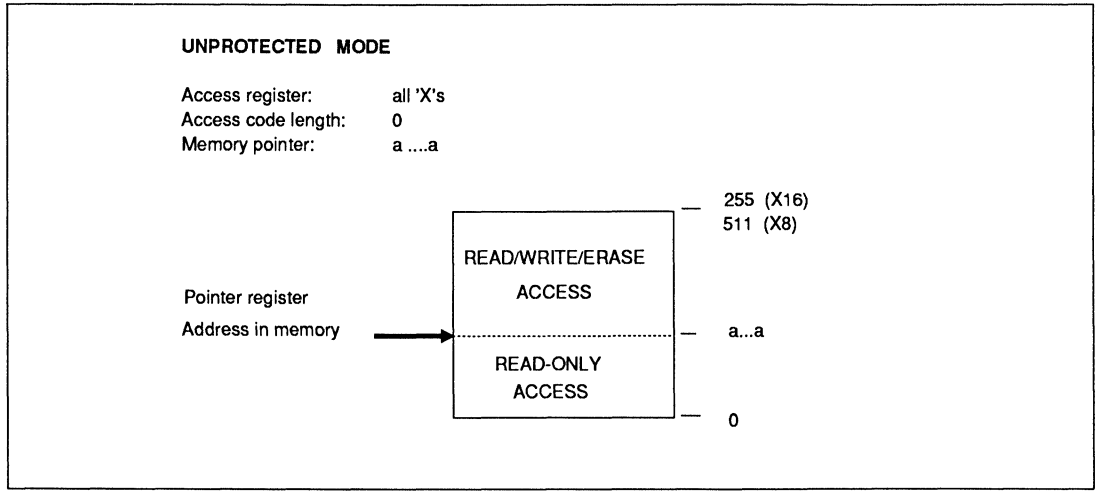


FIGURE 2



PIN DESCRIPTION

CS

Chip Select is a TTL compatible input which, when set HIGH, allows normal operation of the device. When set LOW, it resets the device, terminating all I/O communication, and puts the output in a high impedance state. CS is used to reset the device if an error condition exists or to put the device in a power-down mode to minimize power consumption. It may also be used to frame data transmission in applications where the clock and data input have to be ignored from time to time. Although CS resets the device, it does not change the write/erase or the access-enable status. These two functions, once enabled, will remain enabled until specific disabling instructions are sent or until power is removed.

CLK

The System Clock is a TTL compatible input pin that allows operation of the device at a specified frequency. The 35C804A and 35C804B are designed with an internal divider to produce a 9600 baud output for an input clock frequency of 4.9152 MHz and 3.579545 MHz respectively.

DI

The Data Input pin is TTL compatible and accepts data and instructions in a serial format. Each byte must begin with "0" as a start bit. The device will accept as many bits as an instruction requires, including both data and address bits. Extra bits will be disregarded if they are "1's" and extra "0's" will be misinterpreted as the start bit of the next instruction. An instruction error will cause the device to abort operation and all I/O communication will be terminated until a reset is received.

DO

The Data Output pin is a tri-state TTL compatible output. It is normally in a high impedance state unless a READ or an ENABLE BUSY instruction is executed. Following the completion of a 16-bit or 8-bit data stream, the output will return to the high impedance state. During a WRITE/ERASE cycle, if the ENABLE BUSY instruction has been previously executed, the output will stay LOW while the device is BUSY, and it will be set HIGH when the WRITE/ERASE cycle is completed. DO will stay HIGH until the completion of the next instruction's op-code and, if the next instruction is a READ, DO will output the appropriate data at the end of the instruction. If ENABLE BUSY has not been previously executed, DO will stay in a high impedance state. DO will also go to the high impedance state if an error condition is detected. If ENABLE BUSY has not been executed, to determine whether the device is in a WRITE/ERASE cycle or in an error condition, a READ STATUS instruction may be entered. When the device is in a WRITE/ERASE cycle it will output an 8-bit status word. If it does not, it is in an error condition.

PE

The Parity Enable pin is a TTL compatible input. If PE is set HIGH, the device will be configured to communicate using even parity, and if set LOW, it will use no parity. In this case, instructions or data that include parity bits will not be interpreted correctly.

ERR

The Error indication pin is an open drain output. If either an instruction or parity error exists, the ERR pin will output a "0" until the device is reset. This can be done by pulsing CS LOW.

Note: The PE input is internally pulled down to GND (i.e. default = no parity). As with all CMOS devices, CS, CLK and DI inputs must be connected to either HIGH or LOW, and not left floating.

DEVICE OPERATION

INSTRUCTIONS

The CAT35C804 instruction set includes 19 instructions.
Six instructions are related to security or write protection:

DISAC Disable Access
ENAC Enable Access
MACC Modify Access Code
OVMPR Override Memory Pointer Register
RMPR Read Memory Pointer Register
WMPR Write Memory Pointer Register

Six instructions are READ/WRITE/ERASE instructions:

ERAL Erase All
ERASE ERASE memory
READ READ memory
RSEQ Read Sequentially
WRAL Write All
WRITE WRITE memory

Seven instructions are used as control and status functions:

DISBSY Disable Busy
ENBSY Enable Busy
EWEN Erase/Write Enable
EWDS Erase/Write Disable
NOP No Operations
ORG Select Memory Organization
RSR Read Status Register

The UART compatible protocol supports an even parity bit if the PE pin of the device is set HIGH, otherwise there is no parity. If PE is set LOW and the incoming instruction contains a parity bit, it may be interpreted as the start bit of the next instruction. When PE is HIGH, the CAT35C804 expects a parity bit at the end of every 8 bits. For example, the RSEQ instruction looks like this:

0 1100 1011 1 1
0 A15.....A8 P 1
0 A7.....A0 P 1

Once sent, the device outputs data continuously until it reaches the end of memory. The last byte of data within this instruction contains 9 bits, with the ninth bit being the parity bit. The RSEQ instruction may be terminated by bringing CS LOW; the output will then go to high impedence.

UNPROTECTED MODE

As shipped from the factory, the CAT35C804 is in the unprotected mode. The code length is set to 0, and the memory pointer is at address 00 hex. While in this mode, any portion of the E^2PROM array can be read or written to without an access code. A portion of the memory may be protected from any write or erase operation by setting the memory pointer to the appropriate address via the WMPR (Write Memory Pointer Register):

WMPR [address]

As shown previously in Figure 2, memory locations at or below the address set in the memory pointer will be write/erase protected. Thus, unintentional erasure or overwriting of data in this area will be prevented, while memory locations above the protected area still allow full access.

SECURE MODE

As shown previously in Figure 1, in the secure mode, memory locations above the address set in the memory pointer allow READ-only access. Memory locations at or below that address will require an access code before they can be accessed. The secure mode is activated with an MACC (Modify Access Code) instruction followed by a user access code which can be one to eight bytes in length.

EWEN
MACC [access code]
[access code]

The EWEN instruction enables the device to perform WRITE/ERASE operations. The access code must be entered twice for verification. If the device already has an access code, the old access code must be entered before the new access code can be accepted.

Once the secure mode is activated, access to memory locations is under software control. Access (read, write, and erase operations) to the memory locations below the address in the memory pointer must start with the ENAC (Enable Access) instructions followed by the correct access code.

ENAC [access code]
EWEN
WRITE [address][data]

The ENAC instruction, along with the access code, enables access to the protected area of the device. The EWEN instruction enables execution of the WRITE operation. This portion of the memory is otherwise inaccessible for any operation. Read-only access is allowed without the access code for memory locations above the address in the memory pointer.

The access code can be changed by the following instruction :

ENAC [old access code]
EWEN
MACC [old access code]
[access code][access code]

A two-tier protection scheme is implemented to protect data against inadvertent overwriting or erasure. To write to the memory, an EWEN (Erase/Write Enable) must first be issued. The CAT35C804 will now allow write/erase operations to be performed only on memory locations above the address set in the memory pointer. The remaining portion of the memory is still protected. To override this protection, an OVMPR (Override Memory Pointer Register -- see Memory Pointer Register) must be issued for every write/erase instruction which accesses the protected area :

ENAC [access code]
EWEN
OVMPR
WRITE [address][data]

As an alternative to the OVMPR instruction, the WMPR (Write Memory Pointer Register) instruction may be used to move the memory pointer address to uncover the area where writing is to be performed:

ENAC [access code]
EWEN
WMPR [address]
WRITE [address][data]

As shipped from the factory, the device is in the unprotected mode. The length of the access code is user selectable from a minimum of one byte to a maximum of eight bytes ($\geq 1.84 \times 10^{19}$ combinations). Loading a zero-length access code will disable protection.

MEMORY POINTER REGISTER

The memory pointer enables the user to segment the E^2PROM array into two sections. While in the unprotected mode, the array can be segmented between read-only and full access. While in the secure mode, the memory may be segmented between read-only access and password-only access. Three instructions are dedicated to the memory pointer operations. The first one is WMPR (Write Memory Pointer Register). This instruction, followed by an address, will load (or reload) the memory pointer register with a new address. This address will be stored in the E^2PROM and can be modified only by another WMPR instruction. If the device is in the secure mode, this instruction must be preceded by the ENAC instruction and the valid access code. The second instruction is OVMPR (Override Memory Pointer Register) which allows a single write/erase to be performed to memory locations at or below the address set in the memory pointer. This instruction allows the user to modify data in a segmented array without having to move the memory pointer. Once the operation is complete, the device returns to the protected mode. The third instruction is the RMPR (Read Memory Pointer Register) which will place the current contents of the register in the serial output buffer. If the device is in the secure mode, ENAC and a valid access code are needed before the RMPR instruction can be implemented.

STATUS REGISTER

An eight bit status register is provided to allow the user to determine the status of the CAT35C804. The contents of the first three bits of the register are 101 which allows the user to quickly determine whether the device is listening or is in an error condition. The next three bits indicate the status of the device such as ready/busy, instruction error, or parity error (if either or both existed in the previous instruction). The last two bits are reserved for future use.

ERASE ALL AND WRITE ALL

As a precaution, the ERAL instruction has to be entered twice before it is executed. This measure is required as a redundancy check on the incoming in-

struction for possible transmission errors. The WRAL instruction requires sending an ERAL first (this sets a flag only) and then the WRAL instruction. The CAT35C804 will accept the following commands:

ERAL ERAL
ERAL will be executed

ERAL WRAL
WRAL will be executed

THE PARITY BIT

The UART compatible protocol supports an even parity bit if the PE pin of the device is set HIGH, otherwise, there is no parity. If PE is set LOW and the incoming instruction contains a parity bit, it will be interpreted as the start bit of the next instruction. When PE is HIGH, the CAT35C804 expects a parity bit at the end of every byte. For example, the RSEQ instruction will look like this :

0 1100 1011 1 1
0 A15.....A8 P 1
0 A7.....A7 P 1

Once sent, the device outputs data continuously until it reaches the end of the memory. The last byte of data contains 9 bits, with the ninth bit being the parity bit. The RSEQ instruction may be terminated by bringing CS low; the output will then go into high impedance.

SYSTEM ERRORS

Whenever an error occurs, be it an instruction error (unknown instruction), or parity error (perhaps caused by transmission error), the device will stop its operation. To return to normal operation, the device must be reset by pulsing CS LOW and then set back to HIGH. Resetting the device will not affect the ENAC, EWEN and ENBSY status. The error may be determined by entering the READ STATUS REGISTER (RSR) instruction. The status output is an 8-bit word with the first three bits being 101. This three bit pattern indicates that the device is out of the error condition. The fourth bit is "1" if an instruction error occurred. The fifth bit is a "1" if a parity error occurred. The sixth bit is a "1" if the device is in a WRITE/ERASE cycle. The last two bits are reserved for future use. The reason for having the "101" pattern is that if the device is in a WRITE/ERASE cycle and the ENBSY (ENABLE BUSY) instruction has not been previously executed, the device will appear to be in the error condition. If the device is in the error condition, it will not respond to any input instruction from DI. However, if the device is in a WRITE/ERASE cycle, it will respond to the RSR instruction by outputting "101 001 00". If the RSR is executed at the end of the WRITE/ERASE cycle, the output will be "101 000 00".

Figure 3 <ASYNCHRONOUS SERIAL COMMUNICATION PROTOCOL>

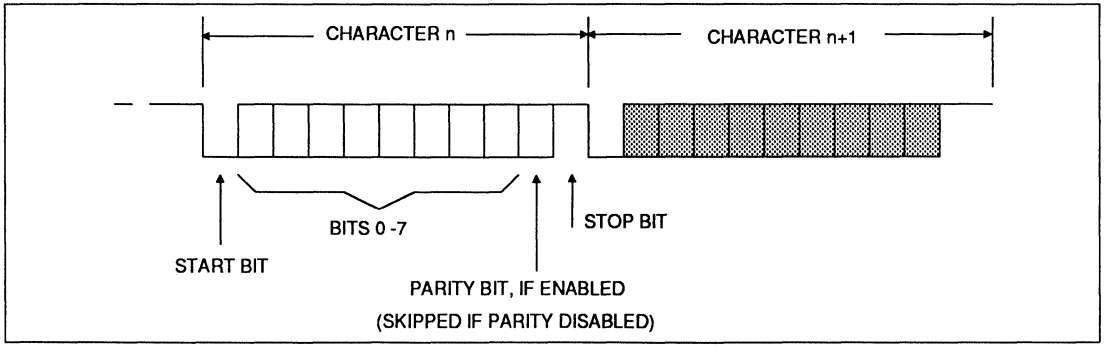


Figure 4 <READ TIMING X16 FORMAT>

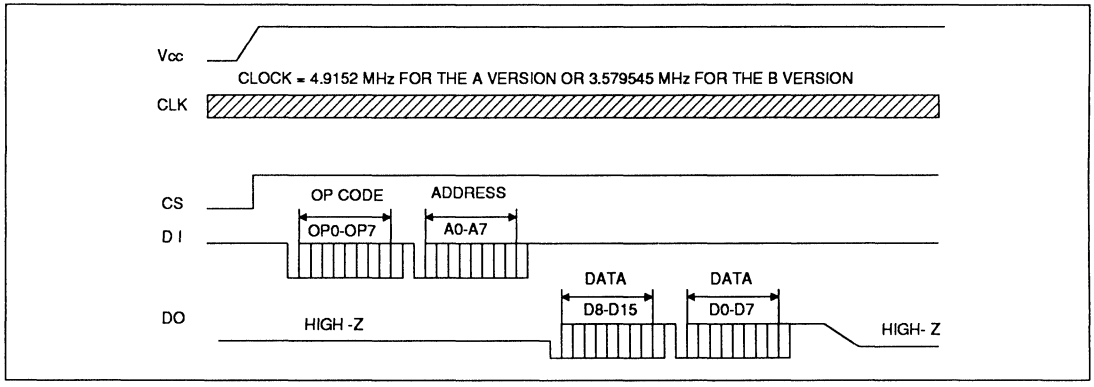
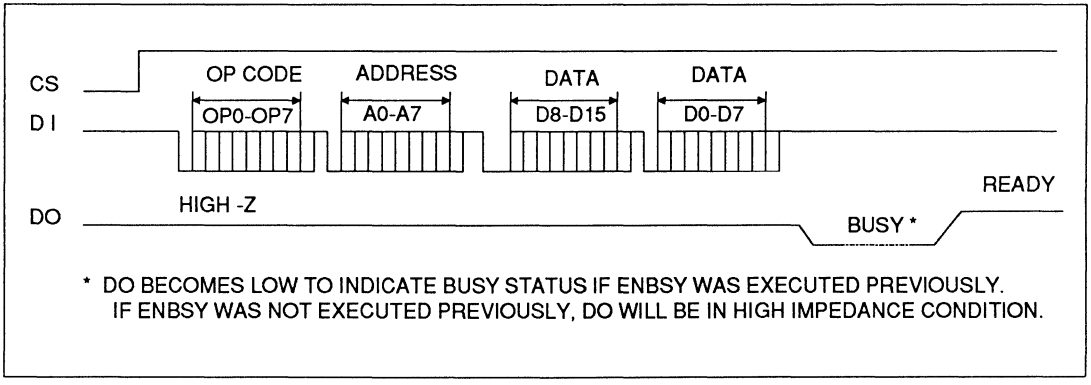


Figure 5 <WRITE TIMING X16 FORMAT>



* DO BECOMES LOW TO INDICATE BUSY STATUS IF ENBSY WAS EXECUTED PREVIOUSLY.
IF ENBSY WAS NOT EXECUTED PREVIOUSLY, DO WILL BE IN HIGH IMPEDANCE CONDITION.

Figure 6 <EWEN/EWDS TIMING x16 FORMAT>

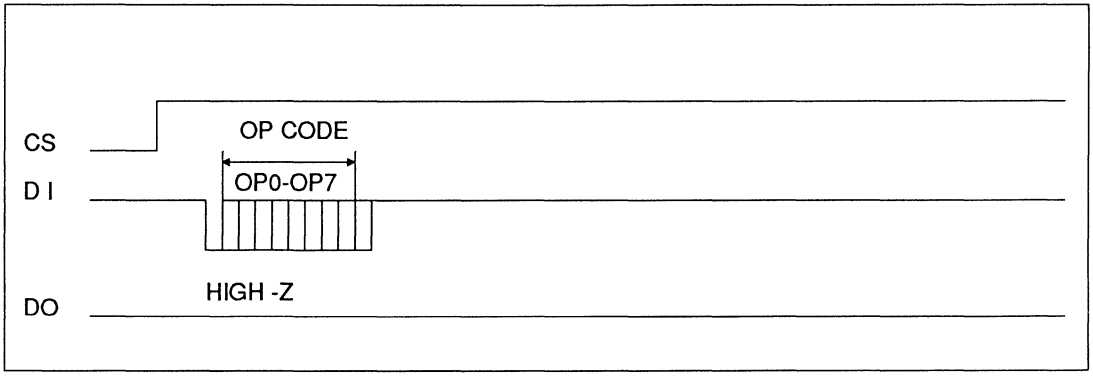


Figure 7 <ERASE TIMING x16 FORMAT>

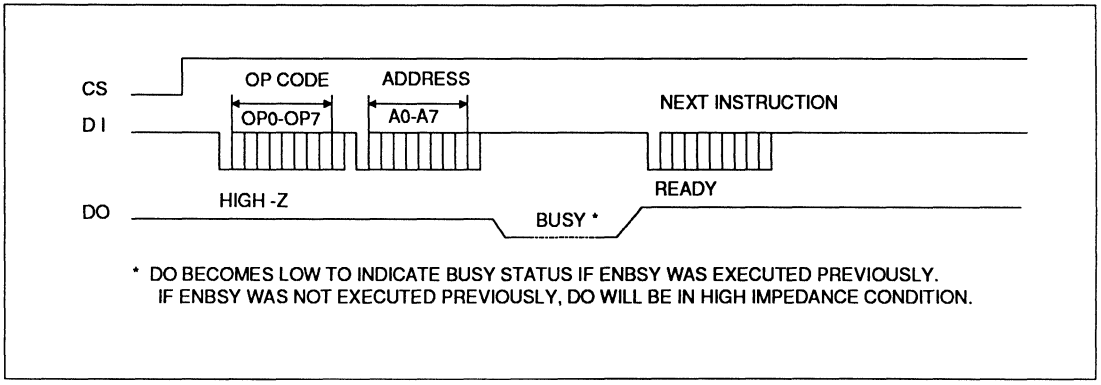


Figure 8 <ERAL TIMING x16 FORMAT>

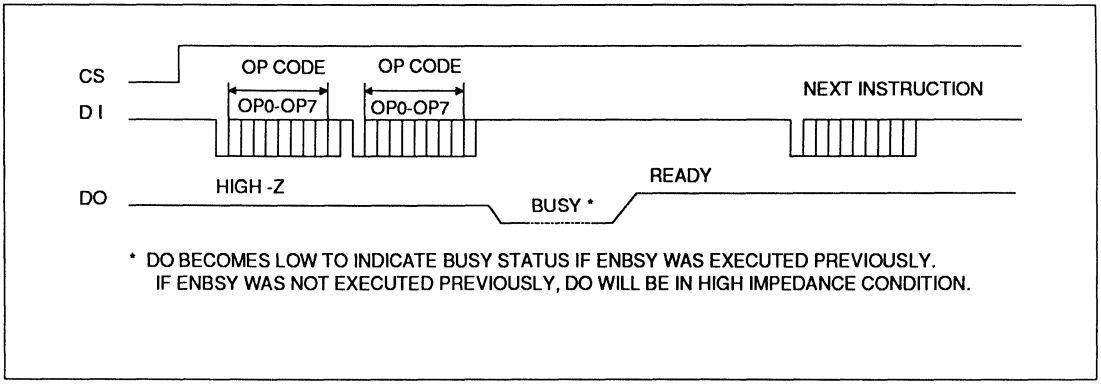


Figure 9 <WRAL TIMING x16 FORMAT>

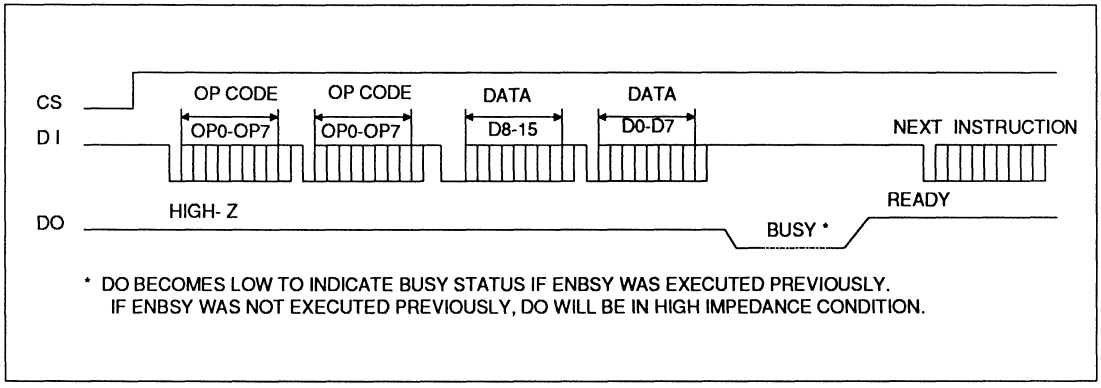


Figure 10 <READ TIMING x8 FORMAT>

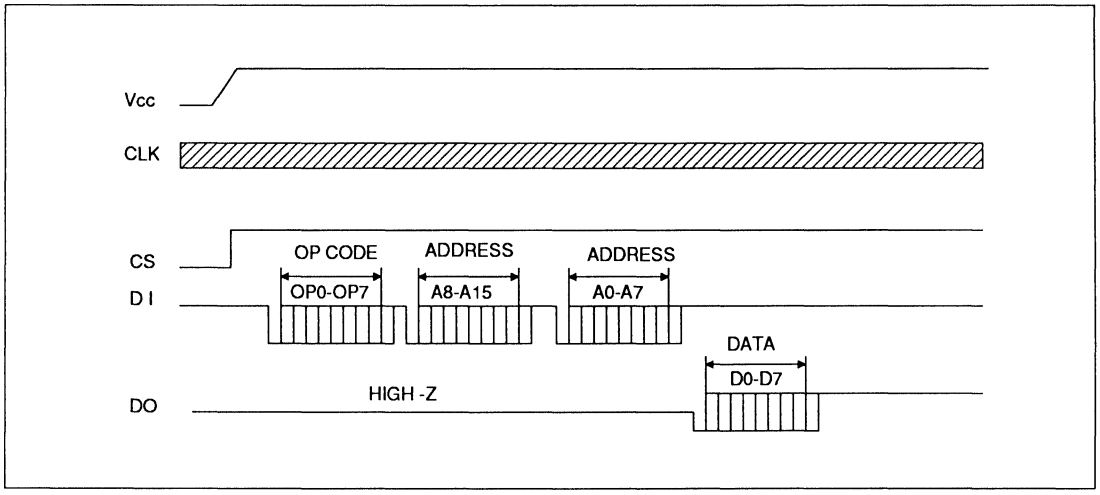
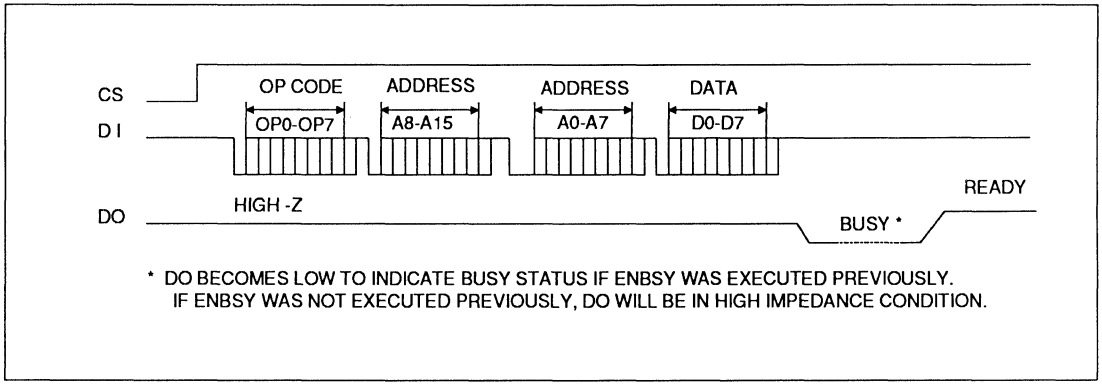


Figure 11 <WRITE TIMING x8 FORMAT>



* DO BECOMES LOW TO INDICATE BUSY STATUS IF ENBSY WAS EXECUTED PREVIOUSLY.
IF ENBSY WAS NOT EXECUTED PREVIOUSLY, DO WILL BE IN HIGH IMPEDANCE CONDITION.

Figure 12 <EWEN/EWDS TIMING x8 FORMAT>

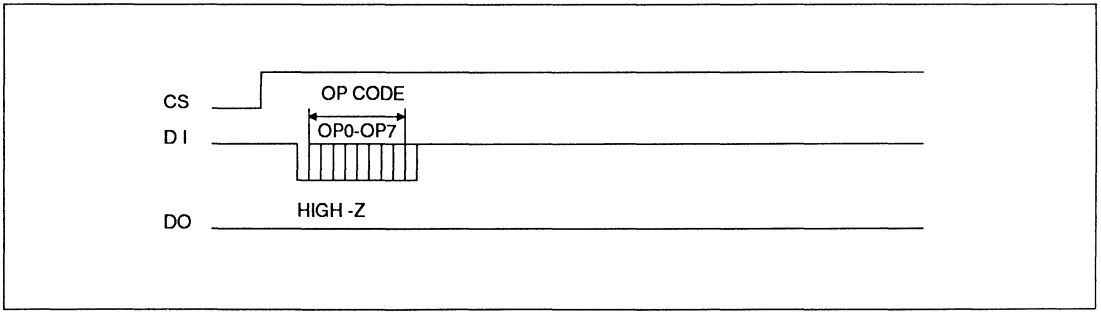


Figure 13 <ERASE TIMING x8 FORMAT>

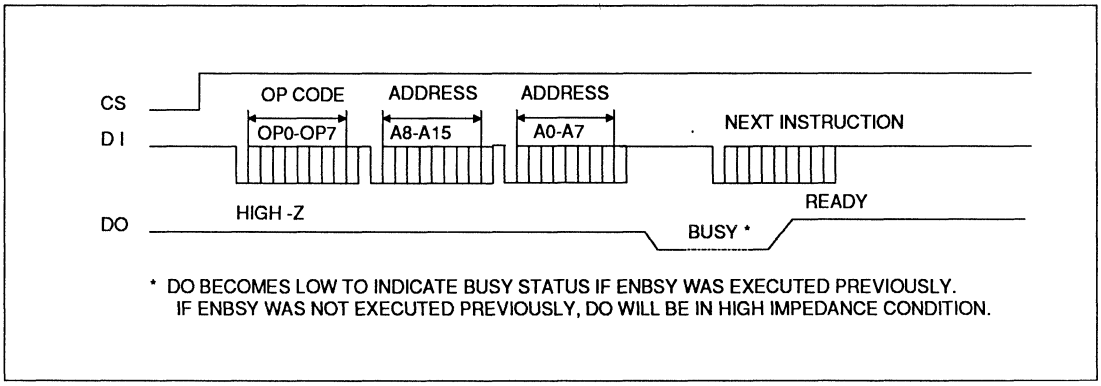


Figure 14 <ERAL TIMING x8 FORMAT>

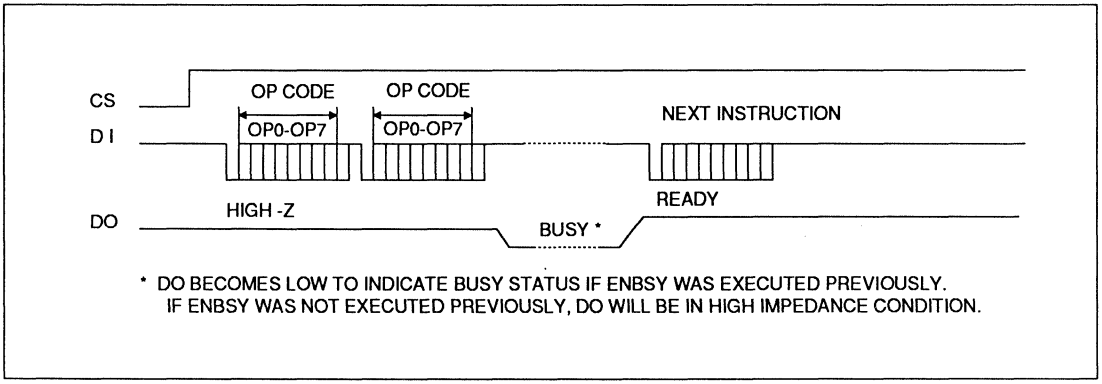
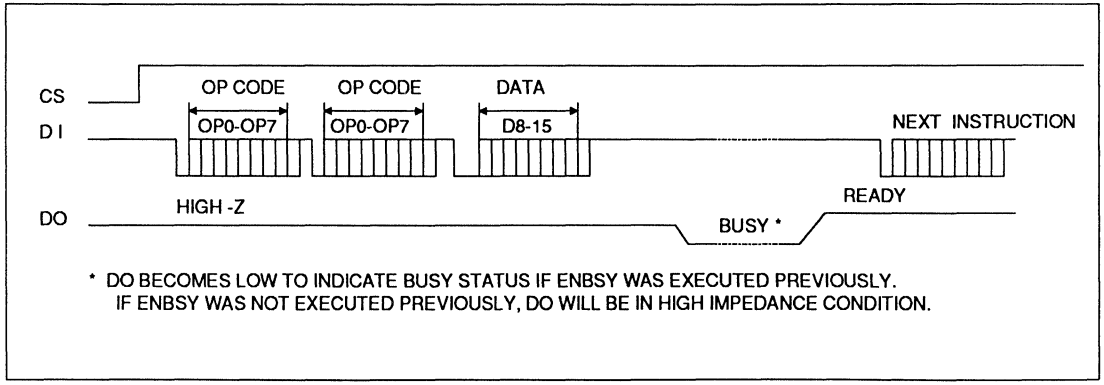


Figure 15 <WRAL TIMING x8 FORMAT>



INSTRUCTION SET

DISAC Disable Access
1000 1000

This instruction will lock the memory from all write/erase operations regardless of the contents of the memory pointer. A write can be accomplished only by first entering the ENAC instruction followed by a valid access code.

ENAC Enable Access
1100 0101
[access code]
[access code]

In the protected mode, this instruction, followed by a valid access code, unlocks the device for read/write/erase access.

WMPR Write Memory Pointer Register
1100 0100 [Addr 15-8] [Addr 7-0]
(for x8 organization)
1100 0100 [Add 7-0]
(for x16 organization)

The WMPR instruction followed by 8 or 16 bits of address (depending on the organization) will move the pointer to the newly specified address.

MACC Modify Access Code
1101 NNNN [Old access code]
[New access code] [New access code]

This instruction requires the user to enter the old access code, if one was set previously, followed by the new access code and a re-entry of the new access code for verification. Within the instruction format, the variable NNNN designates the length of the access code as the following:

NNNN = [0] No access code. Set device to unprotected mode.
NNNN = [1-8] Length of access code is 1 to 8 bytes.
NNNN = [>8] Illegal number of bytes. The CAT35C804 cease operation and requires CS to clear error condition.

RMPR Read Memory Pointer Register
11001010

Output the content of the memory pointer register to the serial output port.

OVMPR Override Memory Pointer Register
1000 0011

Override the memory protection for the next instruction.

READ Read Memory
1100 1001[Addr 15-8][Addr 7-0]
(for x8 organization)
1100 1001[Addr 7-0]
(for x16 organization)

Output the contents of the addressed memory location to the serial port. For the UART protocol start, stop, and parity bits are added to the data byte.

WRITE Write memory
1100 0001[Addr 15-8][Addr 7-0]
[Data 7-0]
1100 0001[Addr 7-0][Data 15-8]
[Data 7-0]

WRITE the 8-bit or 16-bit data to the addressed memory location. After the instruction, address, and data have been entered, the self-timed WRITE sequence will start. The addessed memory location will be erased before data is written. The DO pin may be used to output the READY/BUSY status by having previously entered the ENBSY instruction. During the write cycle, DO will output a LOW for BUSY during the write cycle and a HIGH for READY after the cycle has been completed.

ERASE Erase Memory
1100 0000
[Addr 15 -8] [Addr 7-0]
(for x8 organization)
1100 0000
[Addr 7-0]
(for x16 organization)

Erase data in the specified memory location (set memory to "1"). After the instruction and the address have been entered, the self-timed erase sequence will start. The DO pin may be used to output the READY/BUSY status by having previously entered the ENBSY instruction. During the erase cycle, DO will output a LOW for BUSY during the write cycle

and a HIGH for ready after the cycle has been completed.

ERAL Erase All
1000 1001
1000 1001

Erase the data of all memory locations (all cells can be set to "1"). For protection against inadvertent chip erase, the ERAL instruction is required to be entered twice.

WRAL Write All
1000 1001
1100 0011 [Data 15-8] [Data 7-0]
(for x16 organization)
1000 1001
1100 0011 [Data 7-0]
(for x8 organization)

Write one or two bytes of data to all memory locations. An ERAL will be automatically performed before the WRAL is executed. For protection against inadvertent overwriting of data, the ERAL instruction is required to be entered preceding the WRAL instruction.

RSEQ Read Sequentially
1100 1011
Addr 15-8 Addr 7-0
(for x8 organization)
1100 1011
Addr 7-0 (for x16 organization)

Read memory starting from specified address, n, then n+1, etc, to the highest address or until CS goes LOW. The instruction will be terminated when CS goes LOW.

ENBSY Enable Busy
1000 0100

Enable the status indicator on DO during write/erase cycle. DO goes LOW then HIGH once the write cycle is complete. DO will go to HIGH-Z at the end of the next op code instruction.

DISBSY Disable Busy
1000 0101

Disable the status indicator on DO during write/erase cycle.

EWEN Erase/Write Enable
1000 0001

Enable erase/write to be performed on non-protected portion of memory. This instruction must be entered before any write/erase instruction. Once entered, it will remain valid until power-down or an EWDS (Erase/Write Disable) is executed.

EWDS Erase/Write Disable
1000 0010
Disable all erase and write functions

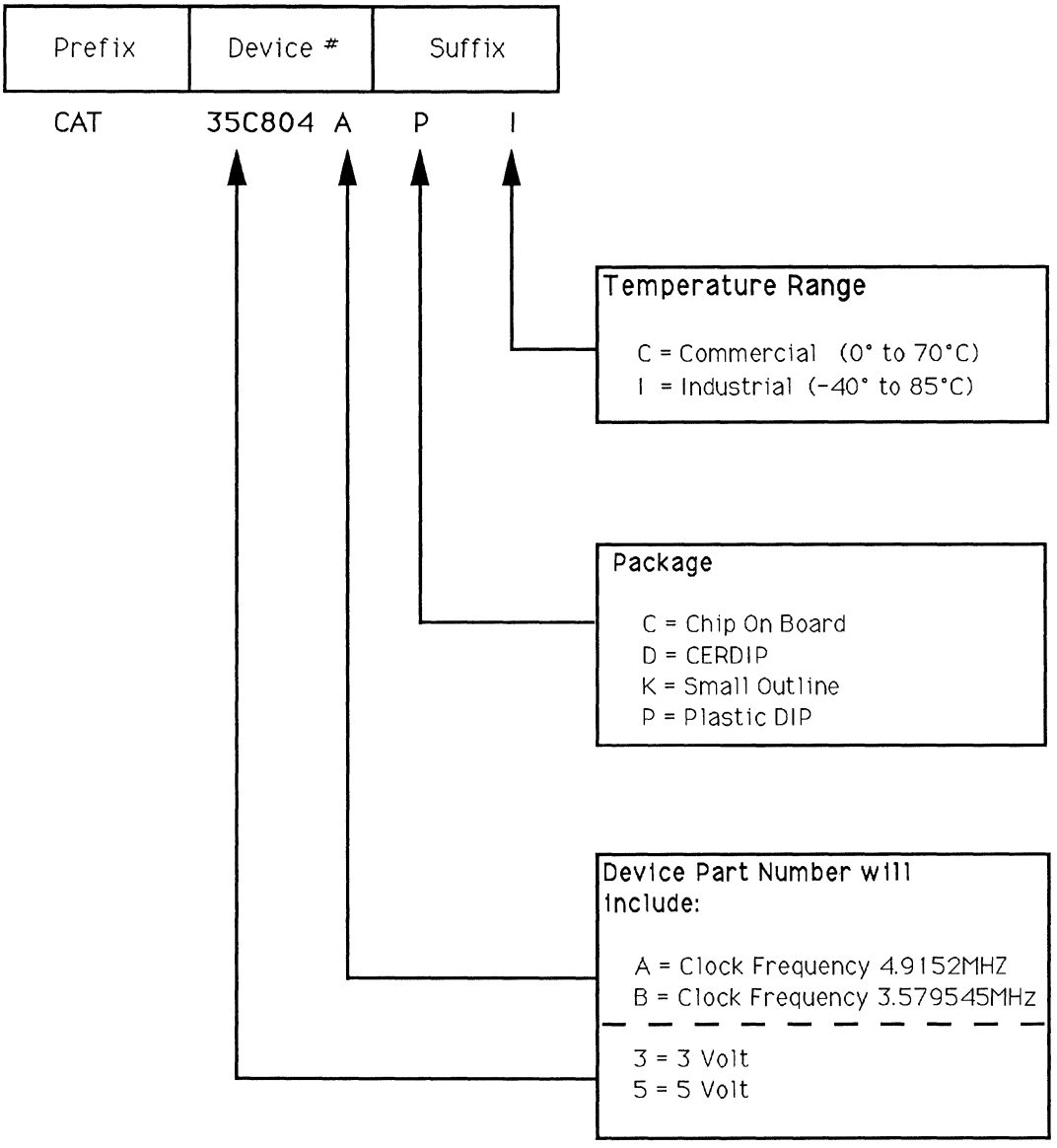
ORG Select Memory Organization
1000 011R (where R = 0 or 1)
Set memory organization
to 512x8 if R = 0.
Set memory organization
to 256x16 if R = 1.

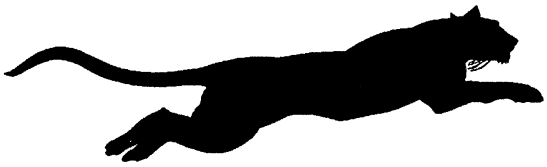
RSR Read Status Register
1100 1000

Output the contents of the 8-bit status register. The contents of first three bits of the register is 101 which allows the user to quickly determine whether the device is listening or is in an error condition. The next three bits indicate the status such as ready/busy or, if an error existed in the previous instruction, instruction error or parity error. The last two bits are reserved for future use.

NOP No Operation
1000 0000
No operation.

ORDERING INFORMATION





SECTION 5

STATIC RAMS

CAT71C256

32K x 8-BIT CMOS STATIC RAM

DESCRIPTION

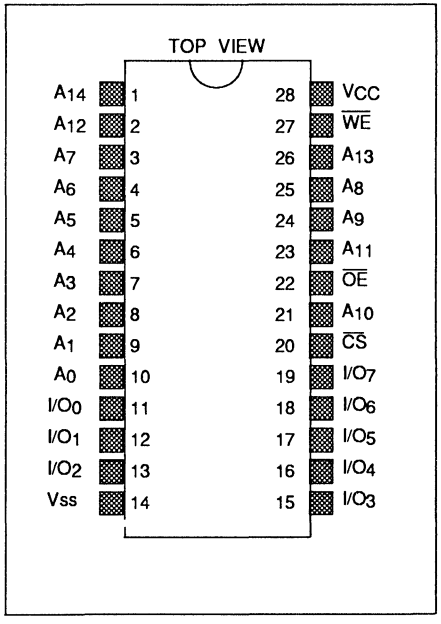
The CAT71C256 is a high performance 262,144 bit CMOS static RAM organized as a 32,768 X 8 bit array. It features 5V single power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary. The CAT71C256 is a CMOS device that requires very low power during standby (1mA). The $\overline{CS}$ and $\overline{OE}$ control signals facilitate OR-tying of the output lines, simplifying memory expansion.

FEATURES

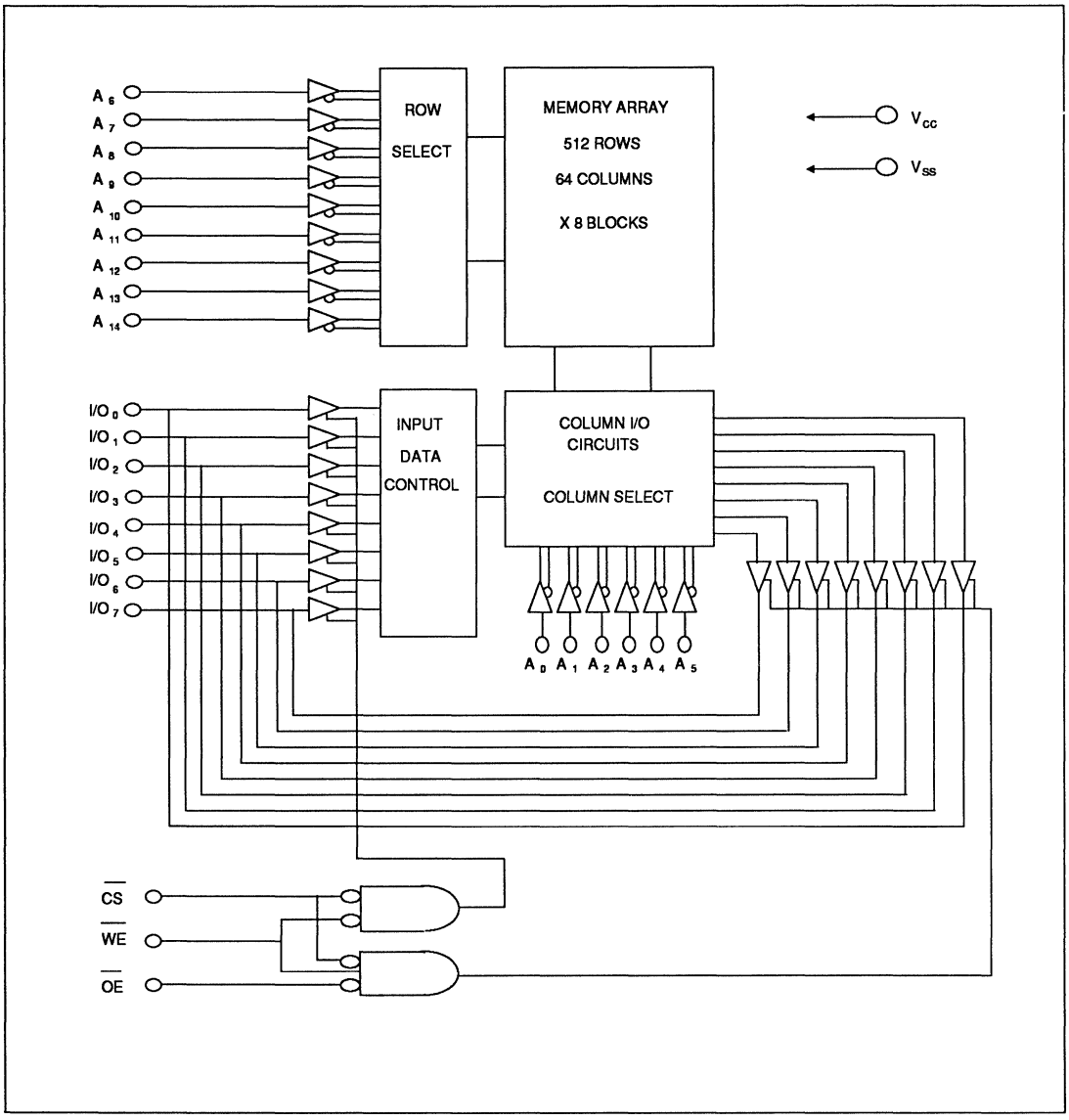
- Single 5V supply (± 10%)
- Low power consumption:
  - Active: 80mA max
  - Standby: 1mA max
- 32,768 X 8 configuration
- Static operation
- Access / Cycle time:
  - 85ns max (CAT71C256-85)
  - 100ns max (CAT71C256-10)
  - 120ns max (CAT71C256-12)
- TTL compatible INPUT/OUTPUT
- Three state outputs
- 28-pin DIP or 32-pin PLCC packages

5

PIN CONFIGURATION
28-Pin DIP



BLOCK DIAGRAM



Pin Assignment [28 and 32 pin package]

A_0 - A_{14}	:Address inputs
$\overline{I/O_0}$ - I/O_7	:Data input/output
$\overline{CS}$	:Chip select
$\overline{WE}$	:Write enable
$\overline{OE}$	:Output enable
V_{CC}, V_{SS}	:Supply voltage

MODES OF OPERATION

Mode	$\overline{CE}$	WE	$\overline{OE}$	I/O Operation
Standby	H	X	X	High-Z
Read	L	H	H	High-Z
	L	H	L	D_{OUT}
Write	L	L	X	D_{IN}

X = H or L

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Conditions	Value	Unit
V_{CC}	Supply voltage	T_A = 25°C, with respect to V_{SS}	-0.3 to 7.0	V
V_{IN}	Input voltage		-0.3 to V_{CC} +0.3	V
P_D	Power dissipation	T_A = 25°C	1.0	W
T_{STG}	Storage temperature	-	-55 to +150	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage	V_{CC} = 5V ± 10%	4.5	5	5.5	V
V_{SS}				0		V
V_{CCH}	Data retention voltage		2	5	5.5	V
V_{IH}	"H" Input voltage	5V ± 10%	2.2	-	VCC +0.3	V
V_{IL}	"L" Input voltage		-0.3	-	0.8	V
T_{OPR}	Operating temperature		0	-	+70	°C
CL	Output load		-	-	100	pF
TTL			-	-	1	-

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{LI}	Input leakage current	V_{IN} = 0 to V_{CC}	-1		1	µA
I_{LO}	Output leakage current	$\overline{CS}$ or $\overline{OE}$ = V_{IH} VI/O = 0 to V_{CC}	-1		1	µA
V_{OH}	"H" output voltage	I_{OH} = -1mA	2.4		-	V
V_{OL}	"L" output voltage	I_{OL} = 2.1mA			0.4	V
I_{CCS}	Standby supply current (CMOS)	$\overline{CS}$ ≥V_{CC} -0.2V V_{IN} =0 to V_{CC}		0.2	1	mA
I_{CCS1}	Standby supply current (TTL)	$\overline{CS}$ = V_{IH} T_{CYC} = min. cycle			3	mA
I_{CCA}	Operating supply current	Min. cycle			80	mA

AC CHARACTERISTICS - TEST CONDITIONS

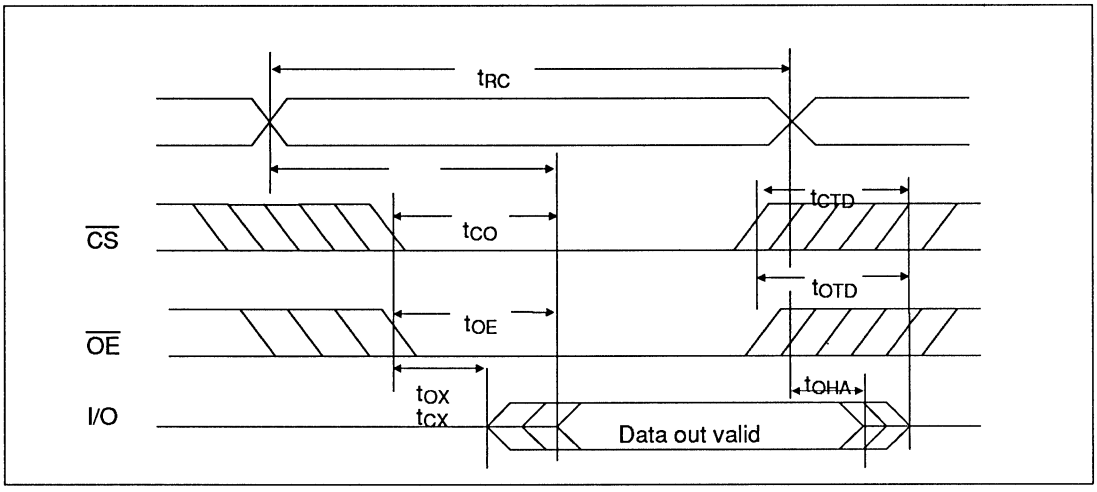
Parameter	Conditions
Input pulse level	V_{IH} = 2.4V, V_{IL} = 0.6V
Input rise and fall times	5 ns
Input/output timing reference level	1.5V
Output load	C_L = 100pF, 1 TTL gate

READ CYCLE

(V_{CC} = 5V ± 10%, T_A = 0° to 70°C)

Symbol	Parameter	71C256-85		71C256-10		71C256-12		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read cycle time	85		100		120		ns
t_{AC}	Address access time		85		100		120	ns
t_{CO}	Chip select access time		85		100		120	ns
t_{OE}	Ouput enable to output valid		45		50		60	ns
t_{CX}	Chip selection to output active	10		10		10		ns
t_{OHA}	Output hold time from address change	5		10		10		ns
t_{OTD}	Output 3-state from output disable	0	30	0	50	0	60	ns
t_{CTD}	Output 3-state from chip deselection		30		40		50	ns
t_{OX}	Output enable to output active	5		5		5		ns

READ CYCLE



NOTES:

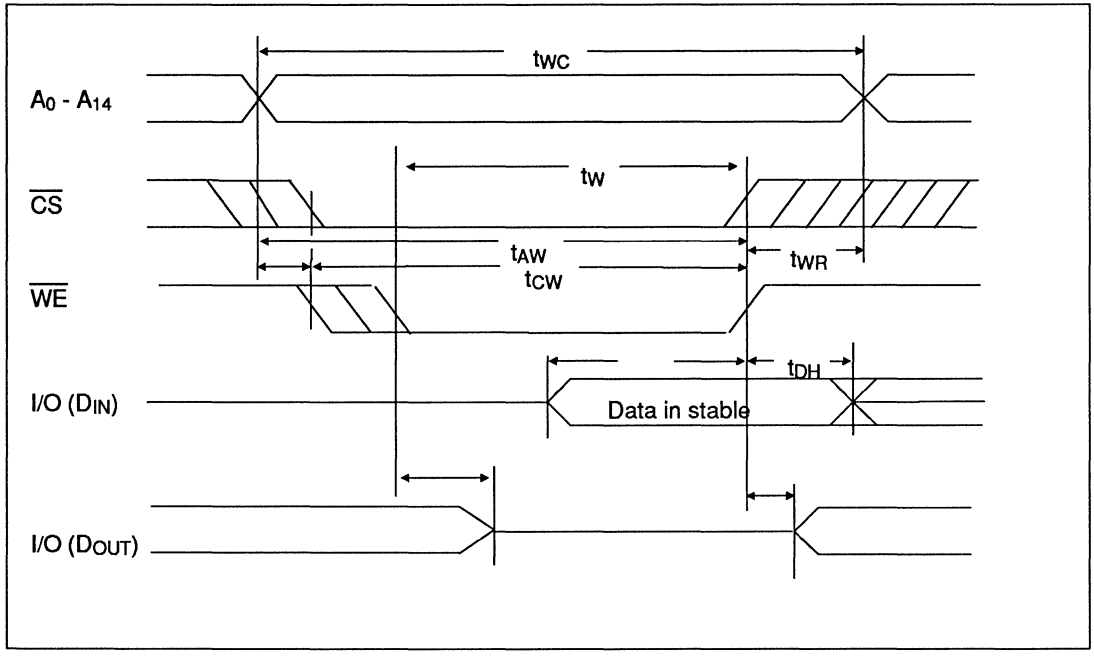
1. A READ occurs during the overlap of a low $\overline{CS}$, a low $\overline{OE}$ and a high $\overline{WE}$.
2. t_{CTD} and t_{OTD} are specified by the time when DATA OUT is floating.

WRITE CYCLE

(T_A= 0° to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	71C256-85		71C256-10		71C256-12		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write cycle time	85		100		120		ns
t_{CW}	Chip selection to End of Write	75		90		100		ns
t_{AW}	Address valid to End of Write	75		90		100		ns
t_{AS}	Address to Write set-up time	0		0		0		ns
t_W	Write time	70		75		90		ns
t_{WR}	Write recovery time	5		10		10		ns
t_{DS}	Data set-up time	40		40		50		ns
t_{DH}	Data hold from write time	0		0		0		ns
t_{OTW}	Output 3-state from write	0	30	0	50	0	60	ns
t_{WX}	Output active from End of Write	5		5		5		ns

WRITE CYCLE TIMING



NOTES:

1. Write condition: during the overlap of a low $\overline{CS}$ and a low WE.
2. $\overline{OE}$ may be both high and low in a Write cycle.
3. t_{AS} is specified from a low $\overline{CS}$ or a low $\overline{WE}$, whichever occurs last after the address is set.
4. t_W is an overlap time of a low $\overline{CS}$ and a low $\overline{WE}$.
5. t_{WR}, t_{DS} and t_{DH} are specified from a high $\overline{CS}$ or a high WE, whichever occurs first.
6. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
7. When I/O pins are in data output mode, don't force inverse input signals to those pins.

CAPACITANCE

($T_A = 25^oC$, f = 1.0MHz, V_{CC} = 5V)

Symbol	Parameter	Conditions	Limits Typ. max.	Unit
$C_{I/O}$	Input/Output capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input capacitance	V_{IN} = 0V	10	pF

Note: These parameters are periodically sampled and are not 100%

CAT71C256L - Low Power
32K x 8-BIT CMOS STATIC RAM

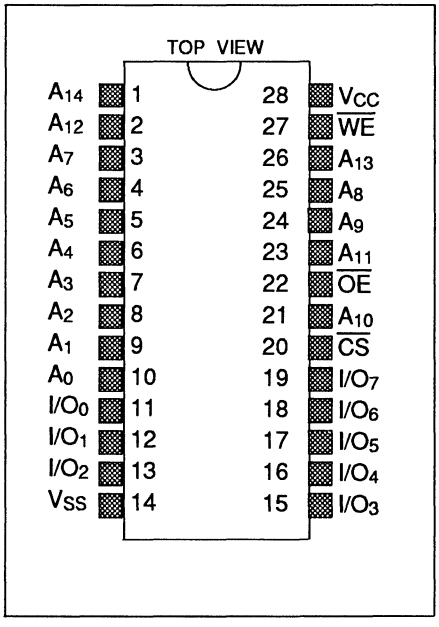
DESCRIPTION

The CAT71C256L is a low power, high performance 262,144 bit CMOS static RAM organized as a 32,768 X 8 bit array. It features 5V single power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary. The CAT71C256L is a CMOS device that requires extremely low power during standby (100µA). The $\overline{CS}$ and $\overline{OE}$ control signals facilitate OR-tying of the output lines, simplifying memory expansion.

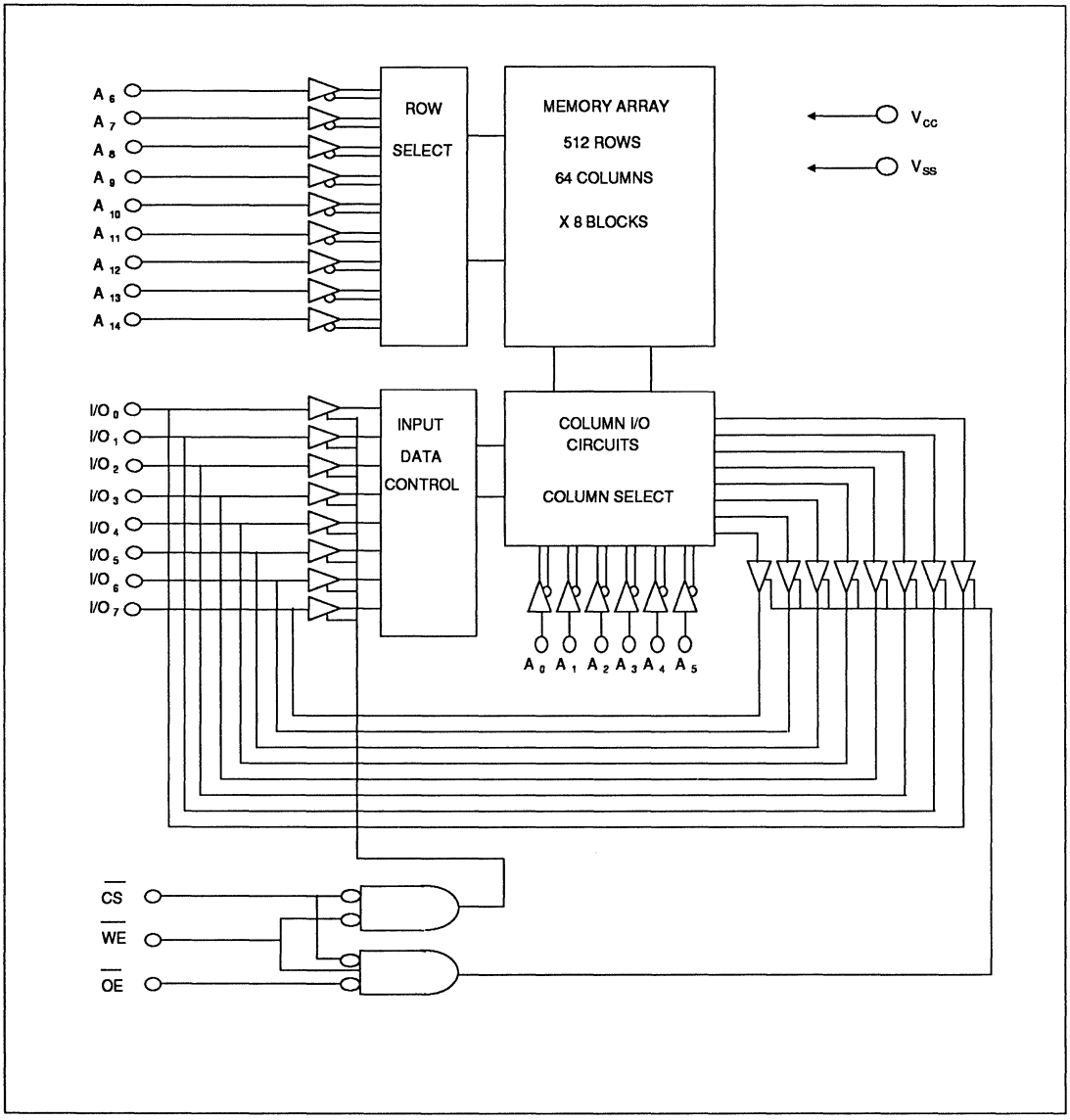
FEATURES

- Single 5V supply (±10%)
- Low power consumption:
  - Active: 80mA max
  - Standby: 100uA max
- 32,768 X 8 configuration
- Static operation
- Access / Cycle time:
  - 85ns max (CAT71C256-85)
  - 100ns max (CAT71C256-10)
  - 120ns max (CAT71C256-12)
- TTL compatible INPUT/OUTPUT
- Three state outputs
- 28-pin DIP or 32-pin PLCC packages

PIN CONFIGURATION
28-Pin DIP



BLOCK DIAGRAM



Pin Assignment [28 and 32 pin package]

A_0 - A_{14}	:Address inputs
I/O_0 - I/O_7	:Data input/output
$\overline{CS}$	:Chip select
$\overline{WE}$	:Write enable
$\overline{OE}$	:Output enable
Vcc, Vss	:Supply voltage

MODES OF OPERATION

Mode	$\overline{CS}$	WE	$\overline{OE}$	I/O Operation
Standby	H	X	X	High-Z
Read	L	H	H	High-Z
	L	H	L	D_{OUT}
Write	L	L	X	D_{IN}

X = H or L

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Conditions	Value	Unit
V_{CC}	Supply voltage	T_A = 25°C, with respect to V_{SS}	-0.3 to 7.0	V
V_{IN}	Input voltage		-0.3 to V_{CC} +0.3	V
P_D	Power dissipation	T_A = 25°C	1.0	W
T_{STG}	Storage temperature	-	-55 to +150	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage	V_{CC} = 5V ± 10%	4.5	5	5.5	V
V_{SS}				0		V
V_{CCH}	Data retention voltage		2	5	5.5	V
V_{IH}	"H" Input voltage	5V ± 10%	2.2	-	VCC +0.3	V
V_{IL}	"L" Input voltage		-0.3	-	0.8	V
T_{OPR}	Operating temperature		0	-	+70	°C
CL	Output load		-	-	100	pF
TTL			-	-	1	-

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{LI}	Input leakage current	V_{IN} = 0 to V_{CC}	-1		1	µA
I_{LO}	Output leakage current	$\overline{CS}$ or $\overline{OE}$ = V_{IH} VI/O = 0 to V_{CC}	-1		1	µA
V_{OH}	"H" output voltage	I_{OH} = -1mA	2.4		-	V
V_{OL}	"L" output voltage	I_{OL} = 2.1mA			0.4	V
I_{CCS}	Standby supply current (CMOS)	$\overline{CS}$ ≥V_{CC} -0.2V V_{IN} =0 to V_{CC}		0.2	100	µA
I_{CCS1}	Standby supply current (TTL)	$\overline{CS}$ = V_{IH} T_{CYC} = min. cycle			3	mA
I_{CCA}	Operating supply current	Min. cycle			80	mA

AC CHARACTERISTICS - TEST CONDITIONS

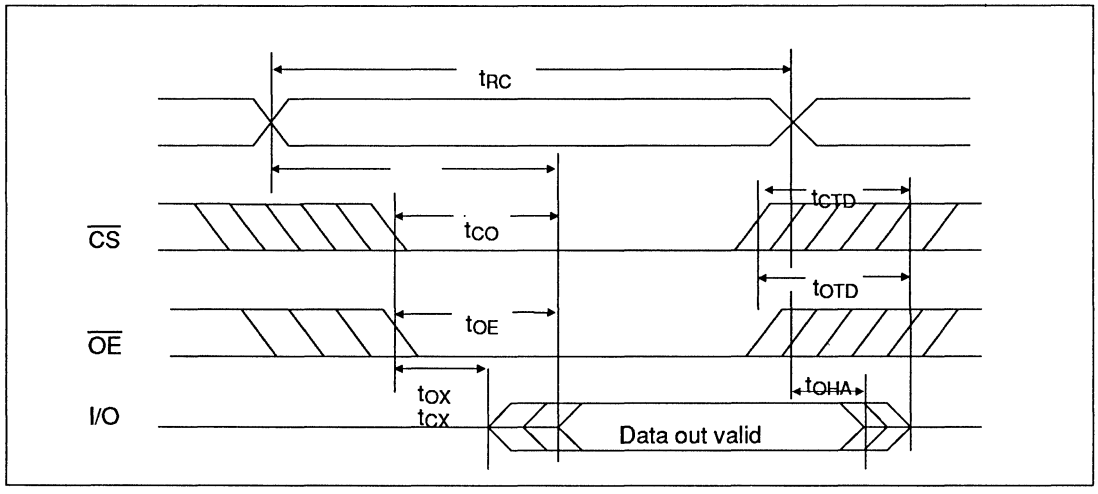
Parameter	Conditions
Input pulse level	V_{IH} = 2.4V, V_{IL} = 0.6V
Input rise and fall times	5ns
Input/output timing reference level	1.5V
Output load	C_L = 100pF, 1 TTL gate

READ CYCLE

(V_{CC} = 5V ± 10%, T_A = 0° to 70°C)

Symbol	Parameter	71C256-85		71C256-10		71C256-12		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read cycle time	85		100		120		ns
t_{AC}	Address access time		85		100		120	ns
t_{CO}	Chip select access time		85		100		120	ns
t_{OE}	Ouput enable to output valid		45		50		60	ns
t_{CX}	Chip selection to output active	10		10		10		ns
t_{OHA}	Output hold time from address change	5		10		10		ns
t_{OTD}	Output 3-state from output disable	0	30	0	50	0	60	ns
t_{CTD}	Output 3-state from chip deselection		30		40		50	ns
t_{OX}	Output enable to output active	5		5		5		ns

READ CYCLE



NOTES:

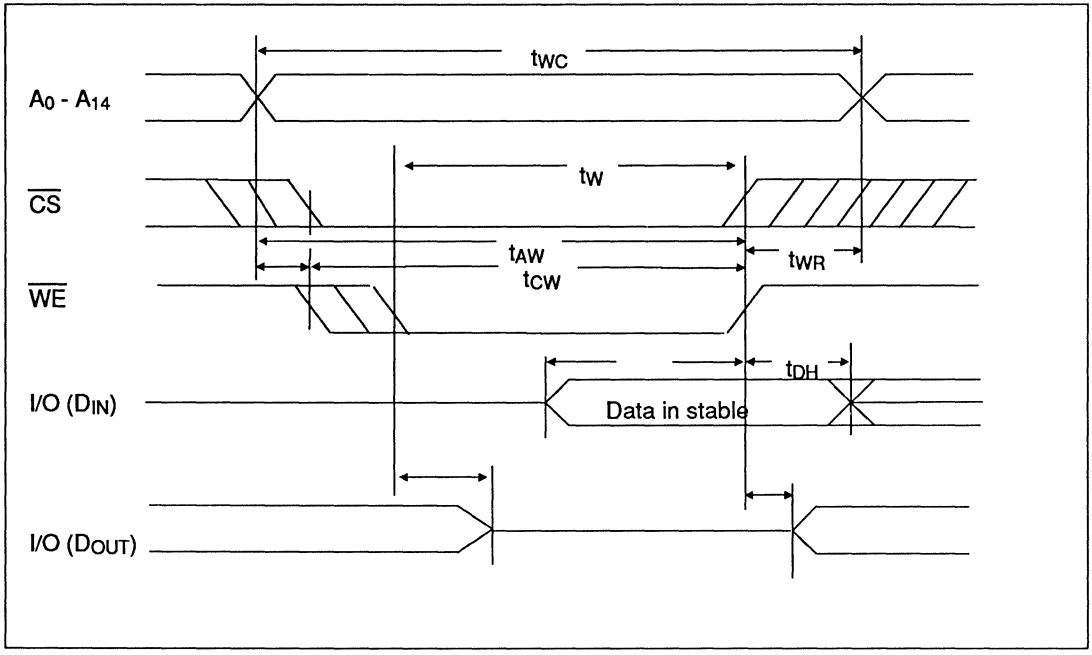
1. A READ occurs during the overlap of a low $\overline{CS}$, a low $\overline{OE}$ and a high $\overline{WE}$.
2. t_{CTD} and t_{OTD} are specified by the time when DATA OUT is floating.

WRITE CYCLE

(T_A= 0° to 70°C, V_{CC} = 5V ± 10%)

Symbol	Parameter	71C256-85		71C256-10		71C256-12		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write cycle time	85		100		120		ns
t_{CW}	Chip selection to End of Write	75		90		100		ns
t_{AW}	Address valid to End of Write	75		90		100		ns
t_{AS}	Address to Write set-up time	0		0		0		ns
t_W	Write time	70		75		90		ns
t_{WR}	Write recovery time	5		10		10		ns
t_{DS}	Data set-up time	40		40		50		ns
t_{DH}	Data hold from write time	0		0		0		ns
t_{OTW}	Output 3-state from write	0	30	0	50	0	60	ns
t_{WX}	Output active from End of Write	5		5		5		ns

WRITE CYCLE TIMING



NOTES:

1. Write condition: during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
2. $\overline{OE}$ may be both high and low in a Write cycle.
3. t_{AS} is specified from a low $\overline{CS}$ or a low $\overline{WE}$, whichever occurs last after the address is set.
4. t_W is an overlap time of a low $\overline{CS}$ and a low $\overline{WE}$.
5. t_{WR}, t_{DS} and t_{DH} are specified from a high $\overline{CS}$ or a high $\overline{WE}$, whichever occurs first.
6. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
7. When I/O pins are in data output mode, don't force inverse input signals to those pins.

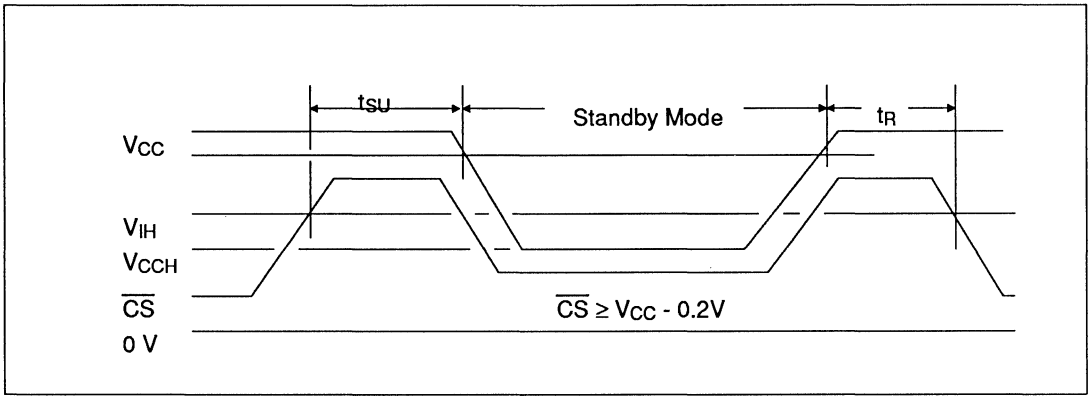
CAPACITANCE

(T_A = 25°C, f = 1.0MHz, V_{CC} = 5V)

Symbol	Parameter	Conditions	Limits Typ. max.	Unit
$C_{I/O}$	Input/Output capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN}	Input capacitance	V_{IN} = 0V	10	pF

Note: These parameters are periodically sampled and are not 100%

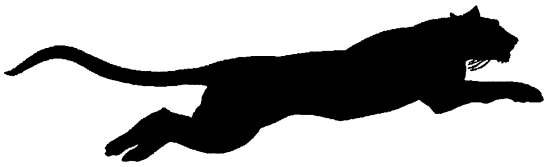
$\overline{CS}$ CONTROL



LOW V_{CC} DATA RETENTION CHARACTERISTICS

T_A = 0°C to 70°C, unless otherwise noted.

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{CCH}	V_{CC} for data retention	$\overline{CS} \geq V_{CC}$ -0.2V	2			V
I_{CCH}	Data retention current	$\overline{CS} \geq V_{CC}$ -0.2V, V_{CC} = 3V		1	50	µA
t_{SU}	$\overline{CS}$ to Data retention time		0			ns
t_R	Operation recovery time		t_{RC}			ns



SECTION 6

MICROCOMPUTERS

CAT62C580
SMART CARD MICROCOMPUTER

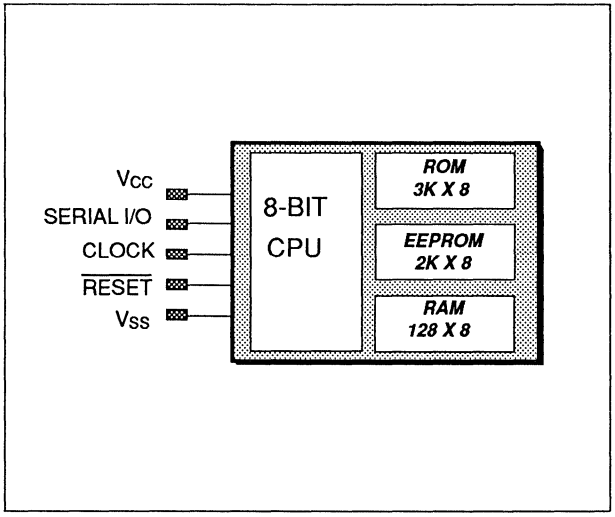
DESCRIPTION:

The CAT62C580 is a single chip 8-bit microcomputer, with a 16K-bit E^2PROM, 3K-bytes of ROM, and 128 bytes of RAM. The built-in hardware security features protect the program memory (ROM cannot be dumped). The CAT62C580's unique architecture makes it ideal for "***Portable Database***" applications, such as IC cards for banking, personal health records, and a variety of ID's including entry access, telephone debit cards, and a large number of military applications.

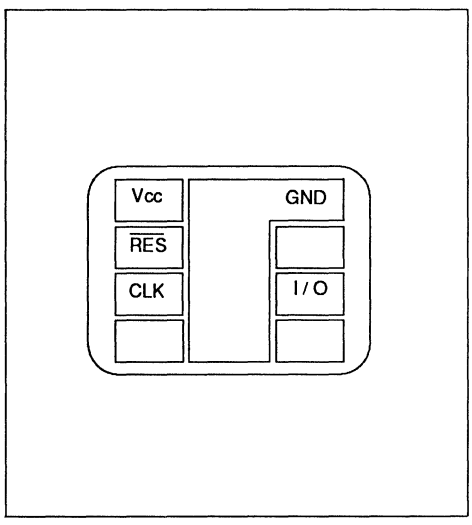
Features:

- 8-Bit CPU, RAM, E^2PROM, and ROM in a single package
- Low Power CMOS technology
- Hardware and software security
- Speed: 800ns instruction cycle at 5MHz
- Clock Frequency: D.C. to 5MHz
- Single pin, high speed serial I/O interface
- 14 internal registers
- 9 addressing modes
- 95 instructions
- 10,000 E^2PROM erase/write cycles per byte
- 10 year E^2PROM data retention

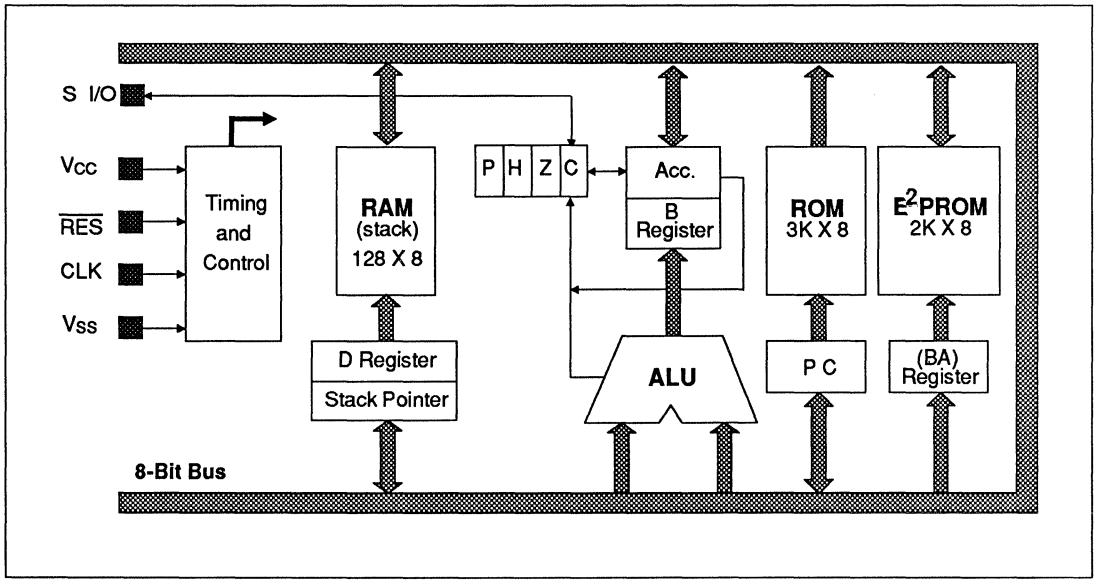
BLOCK DIAGRAM



COB MICRO MODULE



FUNCTIONAL BLOCK DIAGRAM



OPERATING CONDITIONS

Parameter	Symbol	Limits	Unit
Power Supply Voltage	V_{CC}	4.5 to 5.5	Volts
Operating Temperature Range	T_{OP}	0 to 70	^{O}C

PIN DESCRIPTION

Pin	Function	Input/Output
V_{CC}	Power supply pin, +5V ± 10%	
V_{SS}	Power supply pin, 0V	
CLOCK	CPU Clock input pin. Pulled down internally by approximately 100KΩ resistor	INPUT
$\overline{RESET}$	Resets the CPU. Pin is an active low input and is pulled down internally by approximately 100KΩ resistor	INPUT
SERIAL I/O	Serial data input/output pin or pseudo bidirectional pin. The pin is pulled up by an approximately 10KΩ resistor, and is set high at CPU reset.	INPUT/OUTPUT

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits	Unit
Supply Voltage	V_{CC}	$T_A = 25°C$	-0.5 to +7	Volts
Input Voltage	V_I	$T_A = 25°C$	-0.3 to V_{CC} +0.5	Volts
Output Voltage	V_O	$T_A = 25°C$	-0.3 to V_{CC} +0.5	Volts
Storage Temperature	T_{STG}		-40 to +125	°C

D.C. CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0° C to +70°C)

Parameter		Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Current		I_{CC}	f = 5MHz	-	4	10	mA
Low Input Voltage	CLOCK	V_{IL}	-	-0.3	-	0.5	Volts
	$\overline{RESET}$			-0.3	-	0.5	
	SERIAL I/O			-0.3	-	0.8	
High Input Voltage	CLOCK	V_{IH}	-	2.4	-	V_{CC}	Volts
	$\overline{RESET}$			4.0	-	V_{CC}	
	SERIAL I/O			2.0	-	V_{CC}	
Low Output Voltage		V_{OL}	I_{OL} MAX=1.6mA	0	-	0.4	Volts
High Output Voltage		V_{OH}	I_{OH} MAX ≥ -100µA	2.4	-	V_{CC}	Volts
Input Current (CLOCK, $\overline{RESET}$)		I_{IL1}	V_I = 0 (see note)	-	-	1	µA
		I_{IH1}	V_I = V_{CC} (see note)	-	-	20	µA
Input Current (SIO) SERIAL I/O		I_{IL2}	V_I = 0 (see note)	-	-	-1	mA
		I_{IH2}	V_I = V_{DCC} (see note)	-	-	-1	µA
Input Capacitance		C_I	f = 1MHz Ta = 25°C	-	15	-	pF
Output Capacitance		C_O		-	20	-	pF

NOTE: CLOCK and $\overline{RESET}$ are pulled down internaly, and SERIAL I/O is pulled up.

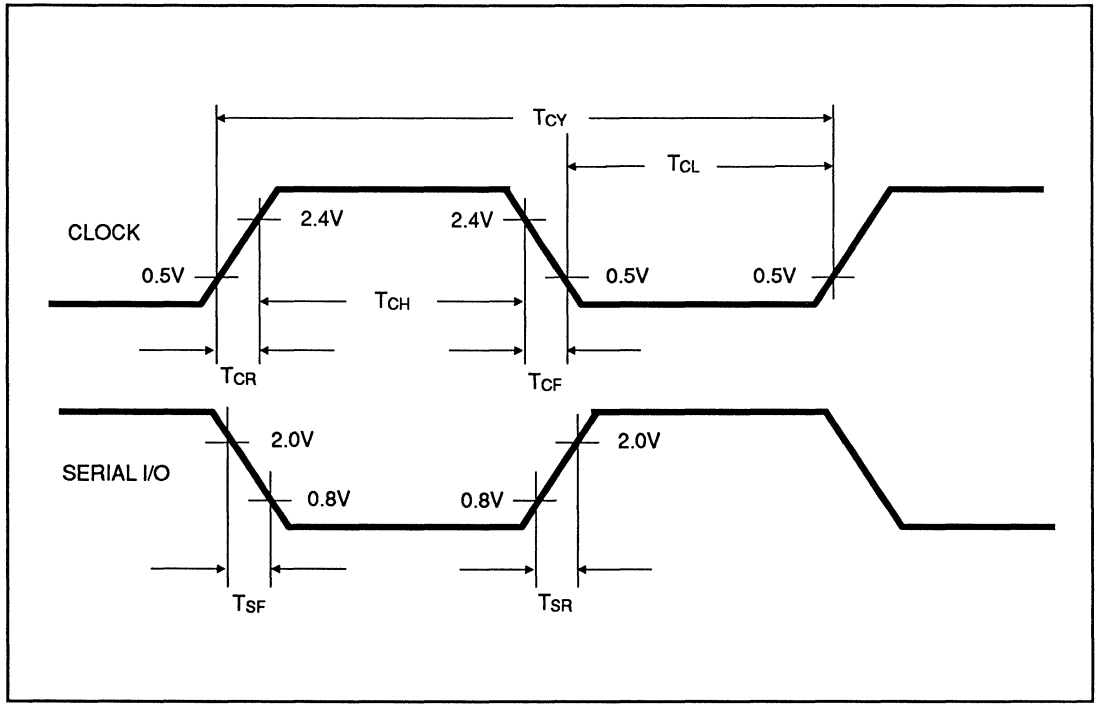
A.C. CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

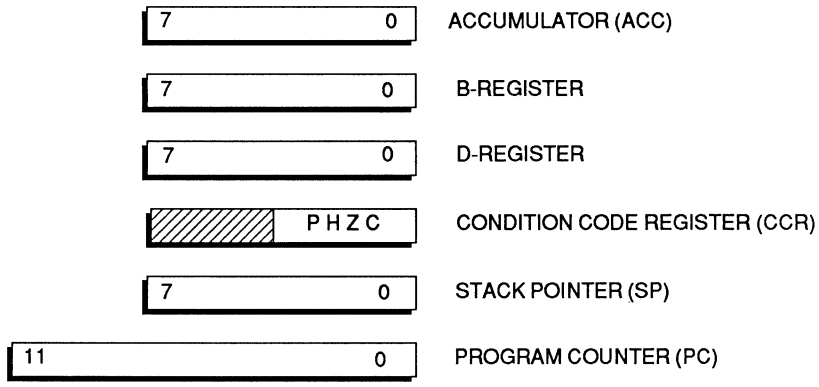
Parameter	Symbol	Min	Typ	Max	Unit
Clock Cycle Time	T_{CY}	200	-	-	ns
Clock Duty Cycle	$(T_{CH}/T_{CY})*100$	40	-	60	%
Clock Cycle Rise Time	T_{CR}	-	-	5.0	µs
Clock Cycle Fall Time	T_{CF}	-	-	5.0	µs
$\overline{\text{RESET}}$ Pulse Width	T_{RW}	8*T_{CY}	-	-	µs
Serial I/O Rise Time	T_{SR}	-	-	5.0	µs
Serial I/O Fall Time	T_{SF}	-	-	5.0	µs

NOTE: Output load capacitance = 30pF.

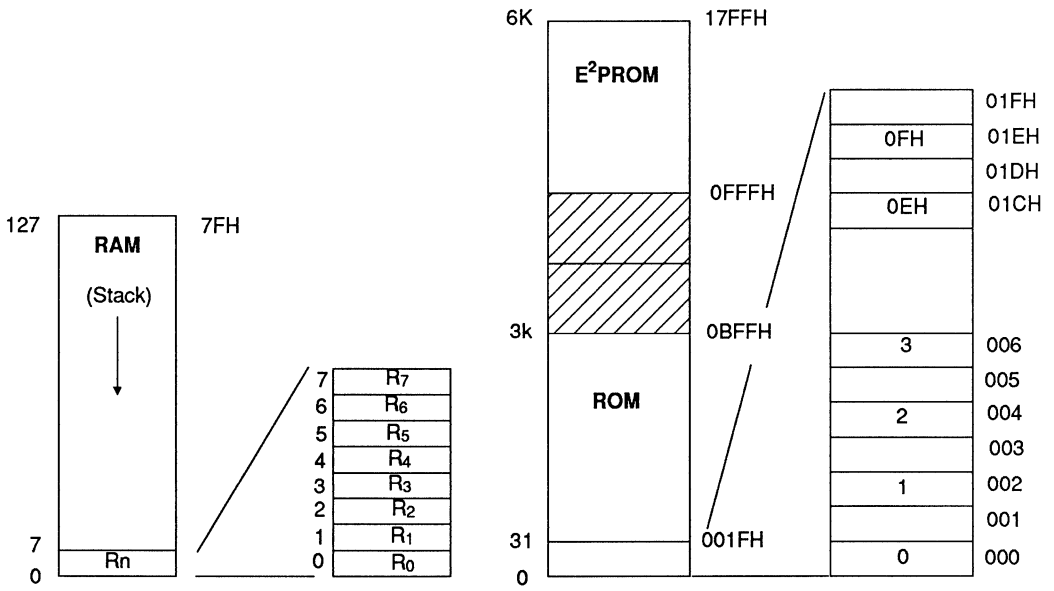
TIMING DIAGRAM



REGISTER SET



MEMORY MAP



Rn is the local register area of the RAM.

RAM map

ZP is the Zero Page addressed with the "CZP" instruction.

ROM and **E²PROM** map

INSTRUCTION SET

MNEMONIC	opr	OPERATION	BYTES	CYCLE	FLAGS			
					C	P	H	Z
MOV A, opr	B	A <-- B	1	1				*
	D	A <-- D	1	1				*
	@D	A <-- (D)	1	1				*
	@D+	A <-- (D), D <-- D+1	1	2				*
	@D-	A <-- (D), D <-- D-1	1	2				*
	N	A <-- (N)	2	2				*
	N+@D	A <-- (N + D)	2	3				*
	#N	A <-- #N	2	2				*
MOV opr, A	B	B <-- A	1	1				
	D	D <-- A	1	1				
	@D	(D) <-- (A)	1	1				
	@D+	(D) <-- A, D <-- D+1	1	2				
	@D-	(D) <-- A, D <-- D-1	1	2				
	N	(N) <--- A	2	2				
	N+@D	(N+D) <-- A	2	3				
MOV D, opr	Rn	D <-- Rn	1	2				
	#N	D <-- #N	2	2				
MOV Rn, opr	D	Rn <-- D	1	2				
	#N	Rn <-- #N	2	3				
MOV @BA, opr	@D	(BA) <--- (D)	1	4				
MOV @D, opr	@BA	(D) <--- (BA)	1	4				
MOV @D+, opr	#N	(D) <-- #N, D <-- D+1	2	2				
MOVW @D, opr	BA	(D) <-- A, (D+1) <-- B	1	3				
MOVW BA, opr	@D	A <-- (D), B <-- (D+1)	1	3				*
MOVW BA, opr	#N	A <-- $\#N_1$, B <-- $\#N_2$	3	3				*

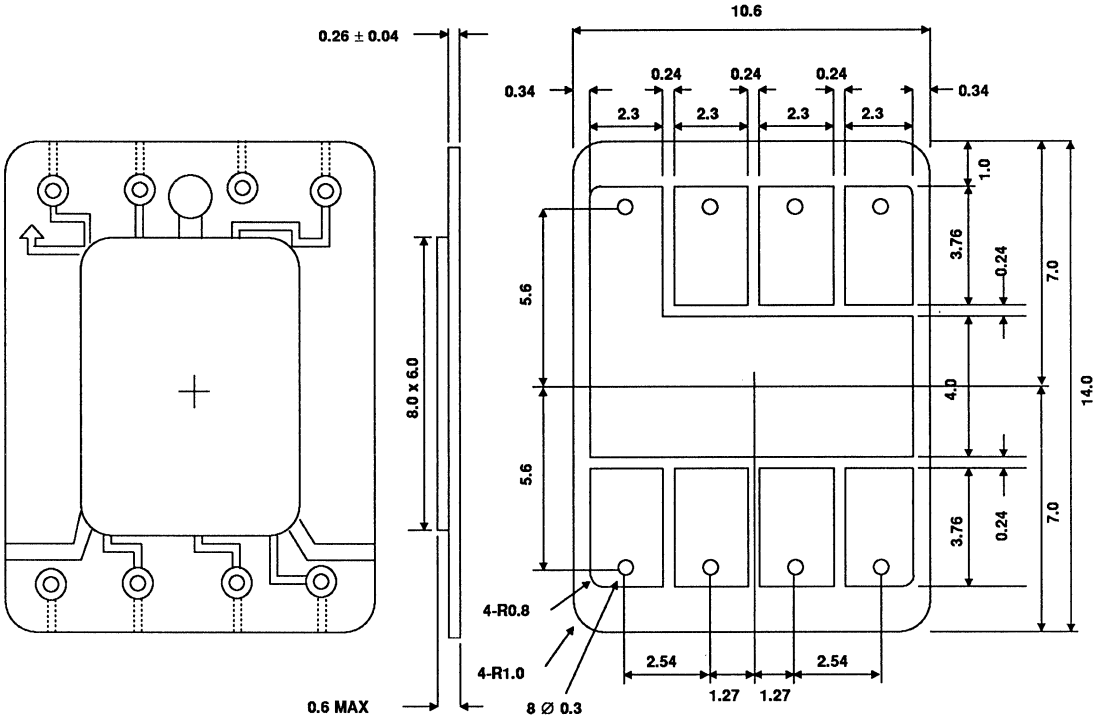
MNEMONIC	opr	OPERATION	BYTES	CYCLE	FLAGS			
					C	P	H	Z
XCH A, opr	B	A <--> B	1	2				*
	D	A <--> D	1	2				*
	@D	A <--> (D)	1	2				*
	N	A <--> (N)	2	2				*
XCH D, opr	B	D <--> B	1	2				
	SP	D <--> SP	1	2				
XCH C, opr	P	C <--> P	1	1	*	*		
ADD A, opr	@D	A <-- A + (D)	1	1	*		*	*
	N	A <-- A + (N)	2	2	*		*	*
	#N	A <-- A + #N	2	2	*		*	*
ADC A, opr	@D	A <-- A + (D) + C	1	1	*		*	*
	N	A <-- A + (N) + C	2	2	*		*	*
	#N	A <-- A + #N +C	2	2	*		*	*
DAA		Decimal Adjust	1	1	*			*
CMP A, opr	@D	A is compared with (D)	1	1	*			*
	N	A is compared with (N)	2	2	*			*
	#N	A is compared with #N	2	2	*			*
CMP @D, opr	@BA	(D) is compared with (BA)	1	4	*			*
EOR A, opr	@D	A <-- A ⊻ (D)	1	1				*
	N	A <-- A ⊻ (N)	2	2				*
	#N	A <-- A ⊻ #N	2	2				*
OR A, opr	@D	A <-- A ORed with (D)	1	1				*
	N	A <-- A ORed with (N)	2	2				*
	#N	A <-- A ORed with #N	2	2				*
AND A, opr	@D	A <-- A ANDed with (D)	1	1				*
	N	A <-- A ANDed with (N)	2	2				*
	#N	A <-- A ANDed with #N	2	2				*

MNEMONIC	opr	OPERATION	BYTES	CYCLE	FLAGS			
					C	P	H	Z
INC opr	A	A <-- A + 1	1	1				*
	D	D <-- D + 1	1	1				
	@D	(D) <-- (D) + 1	1	1				*
	N	(N) <-- (N) + 1	2	2				*
DEC opr	A	A <-- A - 1	1	1				*
	D	D <-- D - 1	1	1				
	@D	(D) <-- (D) - 1	1	1				*
	N	(N) <-- (N) - 1	2	2				*
RRC opr	A	C → A_7 to A_0	1	1	*			*
	@D	C → $(D)_7$ to $(D)_0$	1	1	*			*
	N	C → $(N)_7$ to $(N)_0$	2	2	*			*
RLC opr	A	C ← A_7 to A_0	1	1	*			*
	@D	C ← $(D)_7$ to $(D)_0$	1	1	*			*
	N	C ← $(N)_7$ to $(N)_0$	2	2	*			*
PUSH opr	PSW	(SP) <- A, (SP -1) <- CCR, SP <-- SP -2	1	3				
	D	(SP) <-- D, SP <-- SP -1	1	2				
POP opr	PSW	CCR <-(SP -1), A <-(SP -2) SP <-- SP + 2	1	3	*	*	*	
	D	D <-- SP+1, SP <-- SP+1	1	2				
JZ opr	addr	if Z=1, PC <- PC+2+addr	2	2/3				
JNZ opr	addr	if Z=0, PC <- PC+2+addr	2	2/3				
JC opr	addr	if C=1, PC <- PC+2+addr	2	2/3				
JNC opr	addr	if C=0, PC <-- PC+2+addr	2	2/3				
JB opr	baddr,addr	if (baddr)=1, PC <-- PC+3+addr	2	3/4				
JNB opr	baddr,addr	if (baddr)=0, PC <-- PC+3+addr	2	3/4				
DJNZ opr	Rn,addr	(Rn) <-- (Rn)-1, if Rn ≠ 0, PC <-- PC+2+addr (n=4 to 7)	2	3/4				
JMNE opr	#N,addr	if (D) ≠ #N, PC <-- PC + 3 + addr	3	3/4				
JDNE opr	#N,addr	if D ≠ #N, PC <-- PC + 3 + addr	3	3/4				
JMP opr	addr	PC <-- addr (0 to 4K)	2	2				

MNEMONIC	opr	OPERATION	BYTES	CYCLE	FLAGS			
					C	P	H	Z
CAL opr	addr	(SP) <-- PC+2, PC <-- addr, SP <-- SP - 2	2	4				
CZP opr	addr	(SP) <-- PC+2, PC <-- ZP, SP <-- SP - 2	1	4				
RT		PC <- (SP), SP <- SP+2	1	3				
NOP		No Operation	1	1				
CLR opr	A	A <-- 0	1	1				*
RC		C <-- 0	1	1	0			
SC		C <-- 1	1	1	1			
RB opr	baddr	(baddr) <-- 0	2	2				
SB opr	baddr	(baddr) <-- 1	2	2				
CPL opr	A	A <-- A	1	1				*
	C	C <-- C	1	1	*			
CHK opr	P	P <- C, if A=odd, C <- 1 else C <- 0	1	1	*	*		
SIN		C <-- SI/O	1	1	*			
SOUT		SI/O <-- C	1	1				
DLY opr	N	Delay N+3 Cycles	2	3 to 259				

NOTE: One instruction cycle time is equal to 4 divided by the clock frequency.

PACKAGE DIAGRAM < CHIP-ON-BOARD (COB) >



CAT62C780
SMART CARD MICROCOMPUTER

Preliminary

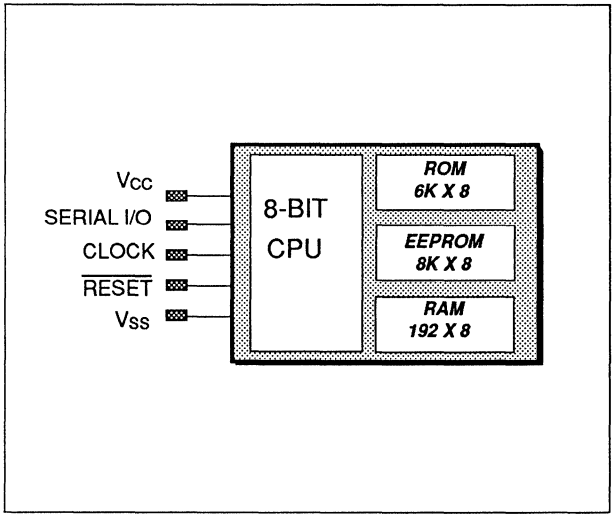
DESCRIPTION:

The CAT62C780 is an advanced single-chip 8-bit microcomputer with 64K-bits of E^2PROM, 6K-bytes of ROM, and 192-bytes of RAM. Designed specifically for IC card applications, it incorporates extensive hardware and software security to protect the program and data memories. Features include on-board hardware error correction and a 32-byte page write mode. The CAT62C780 is ideal for "*Portable Database*" applications where a significant amount of data storage is required, such as financial transactions and personal health record IC cards.

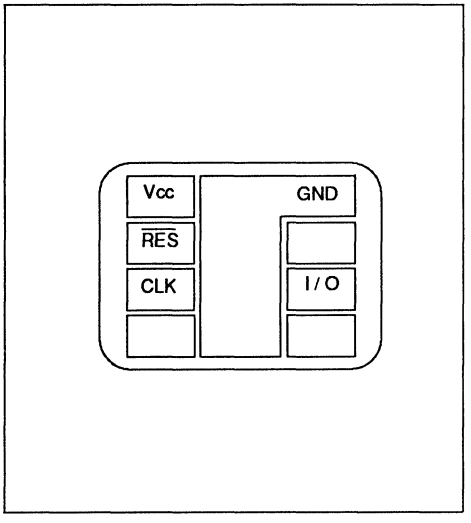
FEATURES:

- 8-Bit CPU, RAM, E^2PROM, and ROM in a single chip
- Low power CMOS technology
- Hardware and software security
- Speed: 800ns instruction cycle at 5MHz
- Clock frequency: D.C. to 5MHz
- Single pin, high speed serial I/O interface
- 22 internal registers
- 114 instructions
- 9 addressing modes
- Downward compatible with the CAT62C580
- Page-write (32-byte)
- ECC
- 10,000 E^2PROM erase/write cycles per byte
- 10 year E^2PROM data retention

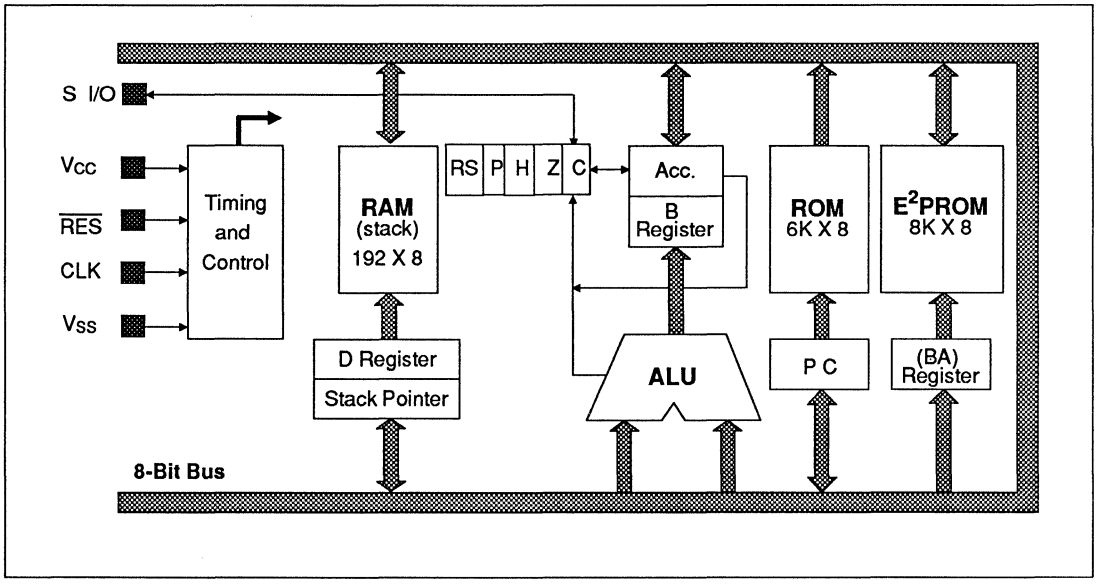
BLOCK DIAGRAM



COB MICRO MODULE



FUNCTIONAL BLOCK DIAGRAM



OPERATING CONDITIONS

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{CC}	4.5 to 5.5	Volts
Operating temperature range	T_{OP}	0 to +70	°C
Data storage temp. at E^2PROM	T_{EEH}	0 to +70	°C

PIN DESCRIPTION

Pin	Function	Input/Output
V_{CC}	Power supply pin, +5V ± 10%	
V_{SS}	Power supply pin, 0V	
CLOCK	CPU Clock input pin. Pulled down internally by approximately 1.5Meg. resistor	INPUT
$\overline{\text{RESET}}$	Resets the CPU. Pin is an active low input and is pulled down internally by approximately 1.5Meg. resistor	INPUT
SERIAL I/O	Serial data input/output pin or pseudo bidirectional pin. The pin is pulled up by an approximately 10K resistor, and is set high at CPU reset.	INPUT/OUTPUT

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits	Unit
Power supply voltage	V_{CC}	$T_A = 25°C$	-0.5 to +7	Volts
Input Voltage	V_{IN}	$T_A = 25°C$	-0.5 to V_{CC} +0.5	Volts
Output Voltage	V_{OUT}	$T_A = 25°C$	-0.5 to V_{CC} +0.5	Volts
Storage Temperature	T_{stg}		-55 to +150	°C

D.C. CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0° C to +70°C)

Parameter		Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Current		I_{CC}	f = 5 MHz	-	8.0	16	mA
Low Input Voltage	CLOCK	V_{IL}	-	-0.3	-	0.5	Volts
	$\overline{RESET}$			-0.3	-	0.6	
	SERIAL I/O			-0.3	-	0.8	
High Input Voltage	CLOCK	V_{IH}	-	2.4	-	V_{CC} +0.3	Volts
	$\overline{RESET}$			4.0	-	V_{CC} +0.3	
	SERIAL I/O			2.0	-	V_{CC} +0.3	
Low Output Voltage		V_{OL}	I_{OL} MAX=1.6mA	0	-	0.4	Volts
High Output Voltage		V_{OH}	I_{OH} MAX ≥ -100µA	2.4	-	V_{CC}	Volts
Input Current (CLOCK, $\overline{RESET}$)		I_{IL1}	V_{CC} = 5.5V, V_{IN} = 0.0V	-	-	-10	µA
		I_{IH1}	V_{CC} = 5.5V, V_{IN} = 5.5V	-	-	10	µA
Input Current (SIO) SERIAL I/O		I_{IL2}	V_{CC} = 5.5V, V_{IN} = 0.0V	-	-	-1	mA
		I_{IH2}	V_{CC} = 5.5V, V_{IN} = 5.5V	-	-	10	µA
Input Capacitance		C_I	f = 1MHz T_A = 25°C	-	10	20	pF
Output Capacitance		C_O		-	10	20	pF

NOTE: CLOCK and $\overline{RESET}$ pins are pulled down internaly, and SERIAL I/O pin is pulled up internally.

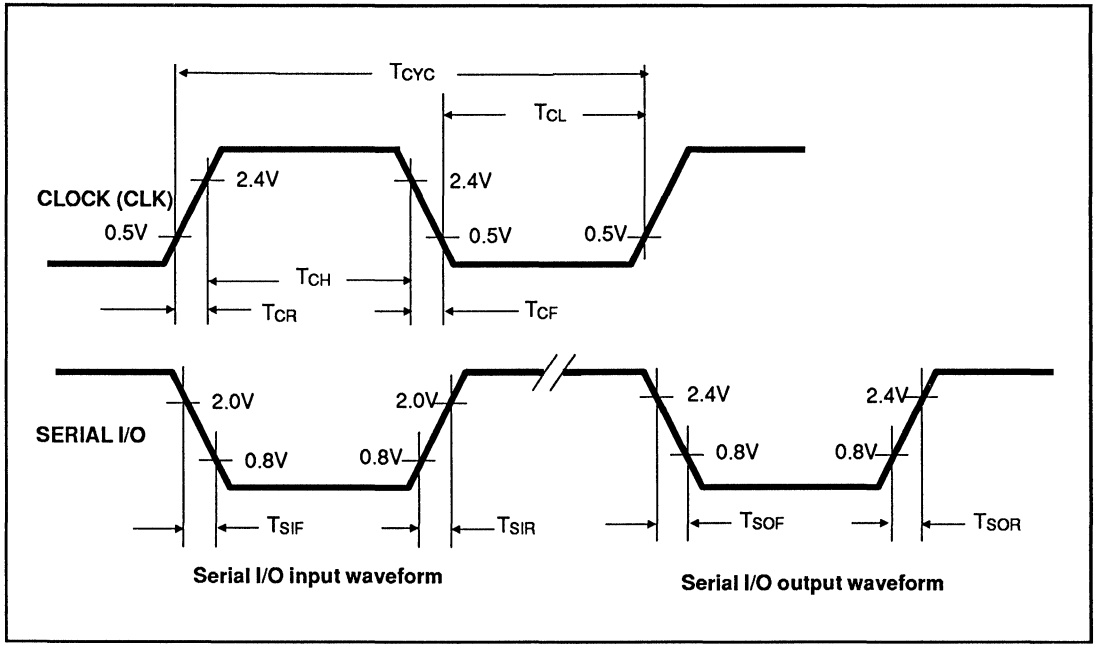
A.C. CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0°C to +70°C)

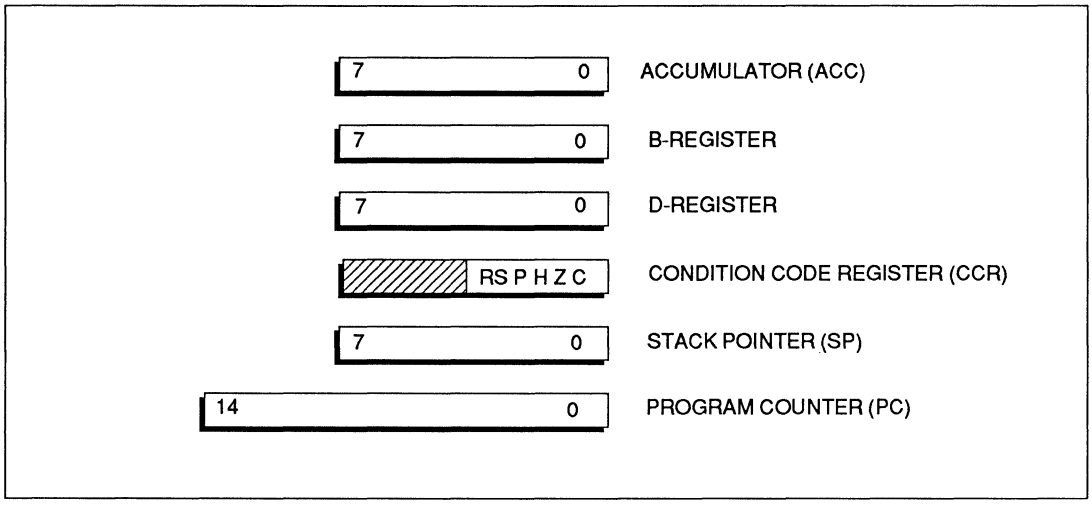
Parameter	Symbol	Min	Typ	Max	Unit
Clock cycle time	T_{CYC}	200	-	-	ns
Clock low level time	T_{CL}	0.4*T_{CYC}	-	0.6*T_{CYC}	ns
Clock high level time	T_{CH}	0.4*T_{CYC}	-	0.6*T_{CYC}	ns
Clock rise time	T_{CR}	-	-	5.0	µs
Clock fall time	T_{CF}	-	-	5.0	µs
$\overline{\text{RESET}}$ pulse width	T_{RW}	8*T_{CYC}	-	-	µs
Serial I/O rise time (input)	T_{SIR}	-	-	5.0	µs
Serial I/O fall time (input)	T_{SIF}	-	-	5.0	µs
Serial I/O rise time (output)	T_{SOR}	-	-	1.0	µs
Serial I/O fall time (output)	T_{SOF}	-	-	1.0	µs

NOTE: Output load capacitance = 30pF.

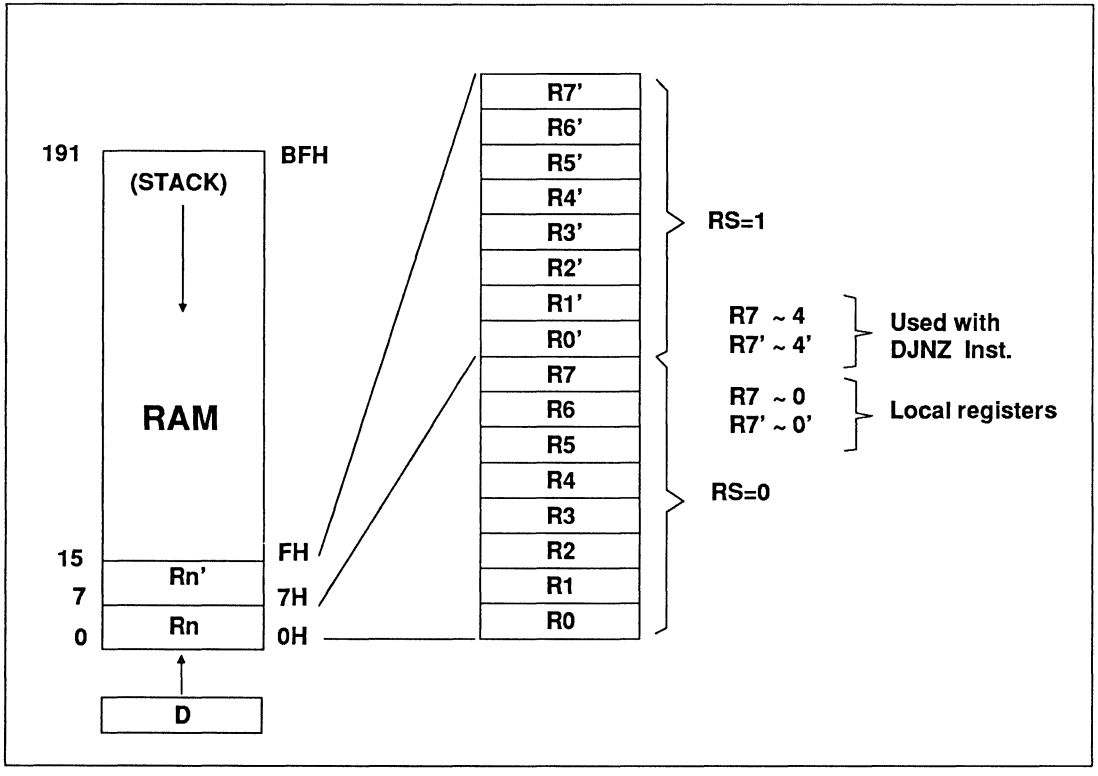
TIMING DIAGRAM



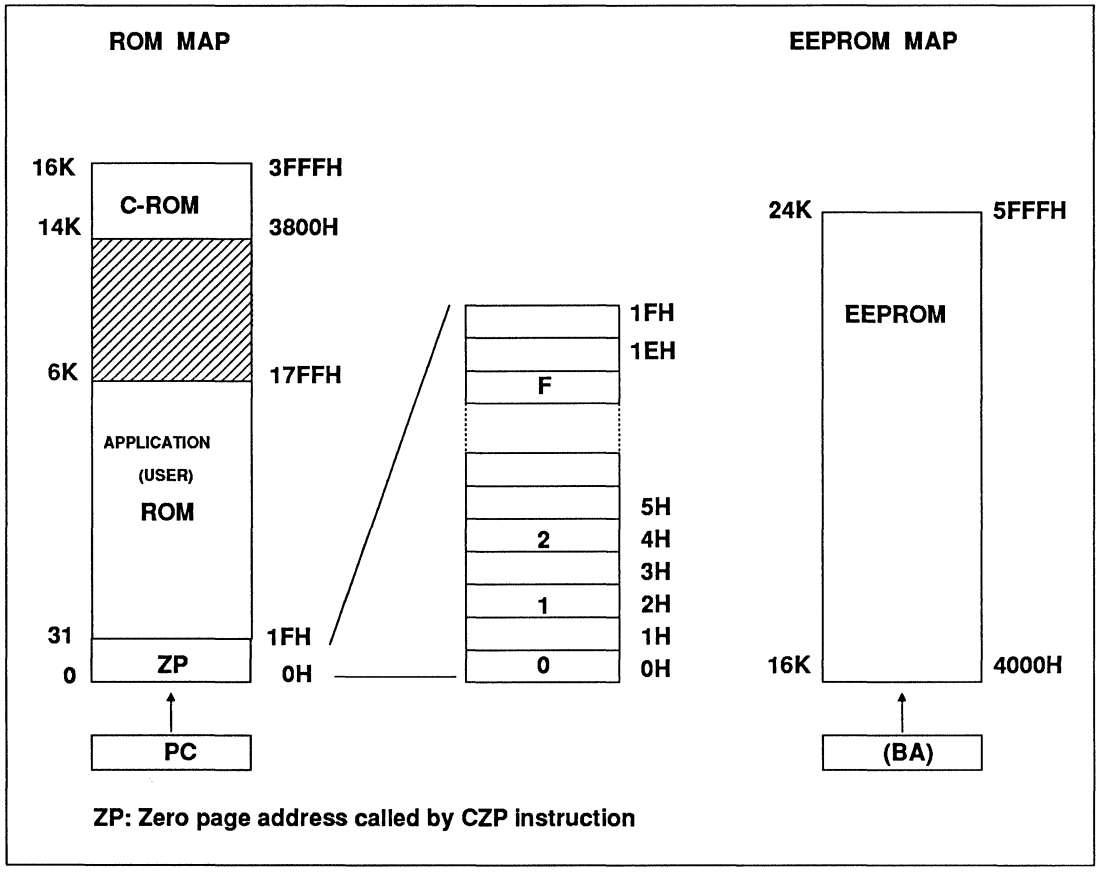
REGISTER SET



MEMORY MAP - RAM



MEMORY MAP - ROM & E^2PROM



ZP: Zero page address called by CZP instruction

E^2PROM WRITING

E^2PROM write operations are controlled by E^2PROM write subroutines installed in the built-in control ROM area. E^2PROM writing has two modes (byte-write/page-write). Byte-write and page-write subroutines are called by the EWR instruction. The E^2PROM data read is executed by the MOV@D, @BA instruction in the same manner as the CAT62C580.

BYTE-WRITE MODE

This mode writes only one byte of data, and execution is the same as setting R7 to "1" in page-write mode. The byte-write procedure is outlined next.

1. Load write (transfer) data in RAM
2. Set RAM address containing write data in D register
3. Set E^2PROM write address in BA register (4000H~5FFFH)
4. EWR XXXXH (byte-write subroutine call)

When the entry address XXXXH is called after proceeding as described above, the write (transfer) process is executed in about 10ms, and control returns to the main routine.

Note: When this subroutine is executed, 8 stack bytes are used and the data in all registers and in RAM is not destroyed.

PAGE-WRITE MODE

This mode writes one or more bytes (1~32 bytes) of data in one write cycle if the data is located in the same page. A page is composed of 32 data bytes (see Figure 1). The page-write procedure is outlined below (see Figure 2).

1. Set the page-write data in RAM
2. Set the RAM start address containing the page-write data in the D register
3. Set the number of page- write bytes in R7 (local register)
4. Set E^2PROM page write start address in BA register
5. EWR XXXXH (page-write subroutine call)

When the entry address XXXXH is called after proceeding as described above, the write (transfer) process is executed in about 10ms, and control returns to the main routine.

Note: When this subroutine is executed, 8 stack bytes are used and the data in all registers and in RAM is not destroyed.

FIGURE 1 E^2PROM PAGE ORGANIZATION

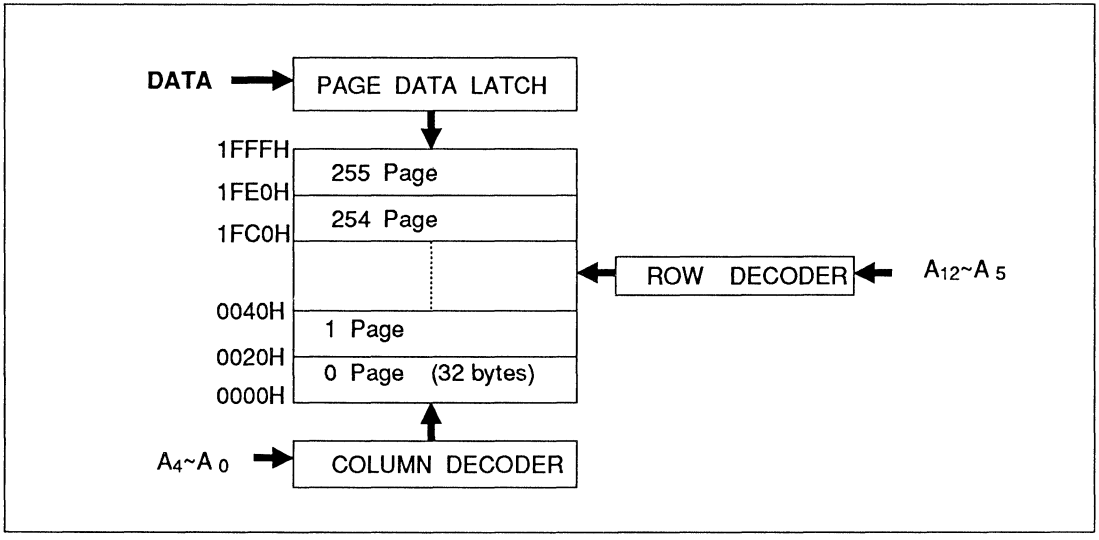
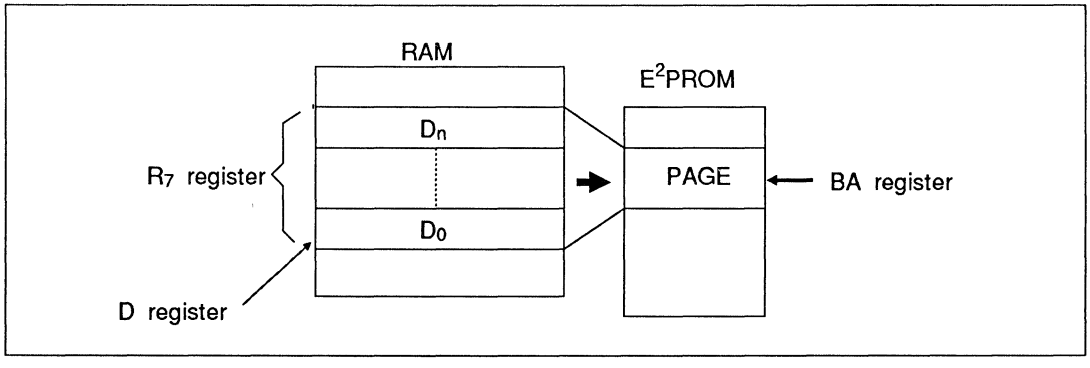


FIGURE 2 PAGE-WRITE MODE [showing data transfer to E^2PROM]



INSTRUCTION SET

MNEMONIC	opr	OPERATION	Bytes	Cycle	FLAGS					
					C	P	H	Z	RS	
MOV A, opr	B	A <-- B	1	1				*		1
	D	A <-- D	1	1				*		2
	@D	A <-- (D)	1	1				*		3
	@D+	A <-- (D), D <-- D+1	1	1				*		4
	@D-	A <-- (D), D <-- D-1	1	2				*		5
	N	A <-- (N)	2	2				*		6
	N+@D	A <-- (N + D)	2	3				*		7
	#N	A <-- #N	2	2				*		8
	Rn	A <-- Rn	1	2				*		9
MOV opr, A	B	B <-- A	1	1						10
	D	D <-- A	1	1						11
	@D	(D) <-- (A)	1	1						12
	@D+	(D) <-- A, D <-- D+1	1	1						13
	@D-	(D) <-- A, D <-- D-1	1	2						14
	N	(N) <--- A	2	2						15
	N+@D	(N+D) <-- A	2	3						16
	Rn	Rn <-- A	1	2						17
MOV D, opr	#N	D <-- #n	2	2						18
MOV @D, opr	#N	(D) <-- #N	2	2						19
MOV N, opr	#N	(N) <-- #N	3	3						20
MOV Rn, opr	#N	Rn <-- #N	2	2						21

INSTRUCTION SET

MNEMONIC	opr	OPERATION	Bytes	Cycle	FLAGS					
					C	P	H	Z	RS	
MOV @BA, opr	@D	(BA) <-- (D)	1	4						22
MOV @D, opr	@BA	(D) <-- (BA)	1	4						23
MOVW BA, opr	#N	A <-- #N, B <-- #n2	3	3				*		24
MOVW N, opr	BA	(N) <-- A, (N+1) <-- B	2	3						25
MOVW BA, opr	N	A <-- (N), B <-- (N+1)	2	3				*		26
XCH A, opr	B	A <--> B	1	1				*		27
	D	A <--> D	1	1				*		28
	@D	A <--> (D)	1	1				*		29
	N	A <--> (N)	2	2				*		30
XCH D, opr	B	D <--> B	1	2						31
	SP	D <--> SP	1	2						32
	Rn	D <--> Rn	1	2						33
XCH C, opr	P	C <--> P	1	1	*	*				34
	RS	C <--> RS	1	2	*				*	35
SWP opr	A	A7~4 <--> A3~0	1	4						36
ADD A, opr	@D	A <-- A + (D)	1	1	*		*	*		37
	N	A <-- A + (N)	2	2	*		*	*		38
	#N	A <-- A + #N	2	2	*		*	*		39
ADC A, opr	@D	A <-- A + (D) + C	1	1	*		*	*		40
	N	A <-- A + (N) + C	2	2	*		*	*		41
	#N	A <-- A + #N + C	2	2	*		*	*		42

INSTRUCTION SET

MNEMONIC	opr	OPERATION	Bytes	Cycle	FLAGS					
					C	P	H	Z	RS	
ADCW BA, opr	N	BA <-- BA + (N+1) (N) + C	2	4	*			*		43
	#N	BA <-- + #N2 • #N1 + C	3	3	*			*		44
DAA		Decimal Adjust	1	1	*			*		45
CMP A, opr	@D	A - (D)	1	1	*			*		46
	N	A - (N)	2	2	*			*		47
	#N	A - #N	2	2	*			*		48
CMP @D, opr	@BA	(D) - (BA)	1	4	*			*		49
CMPW BA, opr	N	BA - (n+1) • (n)	2	4	*			*		50
	#N	BA - #N@ • #N1	3	3	*			*		51
EOR A, opr	@D	A <-- A $\forall$ (D)	1	1				*		52
	N	A <-- A $\forall$ (D)	2	2				*		53
	#N	A <-- A $\forall$ (D)	2	2				*		54
OR A, opr	@D	A <-- A V (D)	1	1				*		55
	N	A <-- A V (N)	2	2				*		56
	#N	A <-- A V # N	2	2				*		57
AND A, opr	@D	A <-- A $\wedge$ (D)	1	1				*		58
	N	A <-- A $\wedge$ (N)	2	2				*		59
	#N	A <-- A $\wedge$ #N	2	2				*		60

INSTRUCTION SET

MNEMONIC	opr	OPERATION	Bytes	Cycle	FLAGS					
					C	P	H	Z	RS	
INC opr	A	A <-- A + 1	1	1					*	61
	D	D <-- D + 1	1	1						62
	@D	(D) <-- (D) + 1	1	1					*	63
	N	(N) <-- (N) + 1	2	2					*	64
INCW opr	BA	BA <-- BA + 1	1	2	*			*		65
DEC opr	A	A <-- A- 1	1	1				*		66
	D	D <-- D - 1	1	1						67
	@D	(D) <-- (D) -1	1	1				*		68
	N	(N) <-- (N) -1	2	2				*		69
DECW opr	BA	BA <-- BA - 1	1	2	*			*		70
CAL opr	addr	(SP)<--PC+2, PC<--addr, SP<--SP-2	2	4						71
CZP opr	addr	(SP)<--PC+1, PC<--ZP, SP<--SP-2	1	4						72
RT		PC <-- (SP), SP <-- SP + 2	1	3						73
PUSH	A	(SP) <-- A, SP <-- SP - 1	1	2						74
	D	(SP) <-- D, SP <-- SP - 1	1	2						75
	PSW	(SP)<--A, (SP-1)<--B, (SP-2)<--CCR, SP<--SP-3	1	4						76
POP opr	A	A<--(SP+1), SP<--SP+1	1	2						77
	D	D<--(SP+1), SP<--SP+1	1	2						78
	PSW	CCR<--(SP+1), B<--(SP+2), A<--(SP+3), SP<--SP+3		4	*	*	*	*	*	79

INSTRUCTION SET

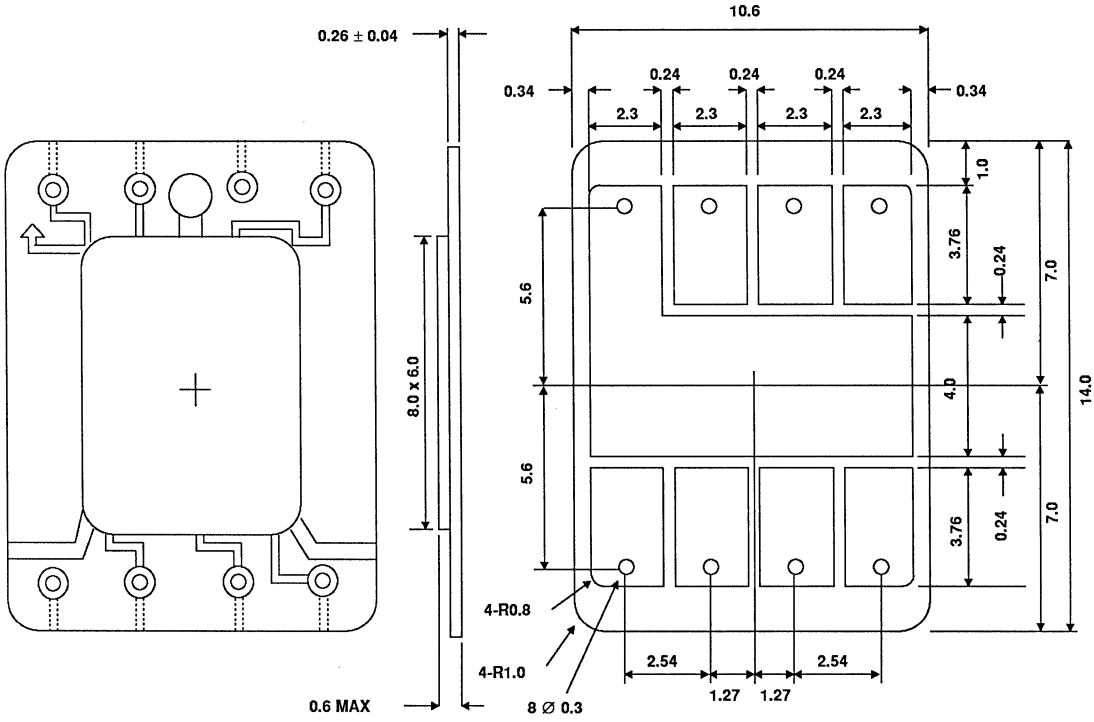
MNEMONIC	opr	OPERATION	Bytes	Cycle	FLAGS					
					C	P	H	Z	RS	
JMP opr	addr	PC <-- addr	2	2						80
JZ opr	addr	if Z = 1, PC <-- PC + 2 + addr	2	2/3						81
JNZ opr	addr	if Z ≠ 1, PC <-- PC + 2addr	2	2/3						82
JC opr	addr	if C = 1, PC <-- PC + 2 + addr	2	2/3						83
JNC opr	addr	if C ≠ 1, PC <-- PC + 2 + addr	2	2/3						84
JB opr	baddr,addr	if(baddr) = 1, PC<--PC+3+addr	3	3/4						85
JNB opr	baddr,addr	if (baddr) ≠ 1, PC<--PC+3+addr	3	3/4						86
DJNZ opr	Rn, addr	Rn<--Rn-1, if Rn≠0, PC<--PC+2+addr (n=4~7)	2	3/4						87
JMNE opr	#N, addr	if (D) ≠ #N, PC<--PC+3+addr	3	3/4						88
JDNE opr	#N, addr	if d ≠ #N, PC<--PC+3+addr	3	3/4						89
JANE opr	@D, addr	if A ≠ (D), PC <-- PC + 2 + addr	2	3/4	*			*		90
	N, addr	if A ≠ (N), PC <-- PC + 3 + addr	3	3/4	*			*		91
	#N, addr	if A ≠ #N, PC <-- PC + 3 + addr	3	3/4	*			*		92
CLR opr	A	A <-- 0	1	1				*		93
CPL opr	A	A <-- $\overline{A}$	1	1				*		94
	C	c <-- $\overline{C}$	1	1	*					95
CPLW opr	BA	BA <-- $\overline{BA}$	1	2				*		96

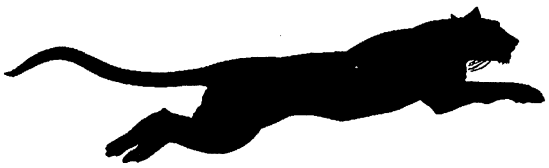
INSTRUCTION SET

MNEMONIC	opr	OPERATION	Bytes	Cycle	FLAGS					
					C	P	H	Z	RS	
RRC opr	A	C→ A 7~0 → C	1	1	*			*		97
	@D	C→ (D) 7~0 → C		1	*			*		98
	N	C→ (N) 7~0 → C	2	2	*			*		99
RCL opr	A	C← A 7~0 ← C	1	1	*			*		100
	@D	C← (D) 7~0 ← C	1	1	*			*		101
	N	C← (N) 7~0 ← C	2	2	*			*		102
SRC opr	A	O --> A 7~0 --> C	11		*			*		103
SLC opr	A	C <-- A 7~0 <-- 0	1	1	*			*		104
RC		C <-- 0	1	1	0					105
SC		C <-- 1	1	1	1					106
CHK opr	P	P <-- C, if A=odd parity C <-- 1	1	1	*	*				107
SIN		C <--SIO	1	1	*					108
SOUT		SIO <-- C	1	1						109
RB	baddr	(baddr) <-- O	2	2						110
SB	baddr	(baddr) <-- 1	2	2						111
NOP		No operation	1	1						112
DLY opr	N	Delay N+2 Cycles if N = 0, delay 258 Cycles	2	3~258						113
EWR opr *	addr	(SP)<--PC+2, PC<--addr, SP<--SP-2 addr: Entry Address	2	4						114

* Depending on the starting address, EWR is either an EEPROM byte or page-write instruction.

PACKAGE DIAGRAM < CHIP-ON-BOARD (COB) >





SECTION 7

APPLICATION NOTES

Using Catalyst's Serial E^2PROMS in Shared Input/Output Configuration

by Asim Bajwa
5/88

Catalyst Semiconductor's family of serial E^2PROMs utilizes 4 signals for the communication interface; Chip Select (CS) for device selection, Serial Clock (SK or CLK) for synchronizing serial data to and from the device, Data Input (DI) to input serial data to the device and Data Output (DO) to output serial data from the device. This interface can be reduced to 3 signals by sharing DI and DO as a common input/output signal. However, the following precautions should be taken to prevent problems due to DI/DO contention:

1) READ instruction in shared DI/DO configuration:
(applies to 93C46, 59C11, 35C102/202, 35C104/204)

DO remains in high impedance while most of the READ instruction (i.e. start bit, opcode and address) is being input and offers no contention to the DI driver on a shared DI/DO signal. However, typically 50ns after the rising edge of the serial clock shifts in the least significant bit of the address stream (A0), DO outputs the dummy '0' bit to flag the beginning of the output data stream. If A0 is a '1' and the DI driver has not been disabled by the time the '0' dummy bit becomes valid, a low impedance path between the system power supply and ground is created through the DI driver pullup and DO pulldown device (Fig. 1).

Unless this condition causes excessive noise on the system power supply (which may in turn cause noisy or spurious signals to the device), the READ instruction will continue and complete normally since A0 is already shifted into the device.

To minimize potential problems during this low impedance condition, a current limiting resistor should be placed between the DI driver and the DO pin when using the shared DI/DO signal (Fig. 2).

Alternatively, an open drain (or open collector) DI driver with pullup resistor could be used (Fig. 2).

In either case, the clocking rate should be slow enough to ensure that the resistor can charge or discharge the shared DI/DO bus capacitance before the appropriate clock edge. For example, if the resistor used is 10KΩ, and the bus capacitance is 100pF, then a safe clock rate is calculated to be:

Clock Period (T) = 2 x 3RC
= 2 x 3 x 10kΩ x 100pF
= 6μsec

Frequency (f) = 1 / T
= 167KHz

2) Programming Instructions in shared DI/DO configuration:
(93C46, 35C102 and 35C104 only)

All devices in the Catalyst serial E2PROM family feature self-timed programming cycles. A programming status signal indicates whether the self-timed programming cycle is still in progress or has been completed. A '0' status signal indicates that the device is still programming, while a '1' status signal indicates that the programming cycle has been completed and the device is ready to receive the next instruction. This feature will allow a user to minimize the programming time (t_{EW}).

The 59C11, 35C202 and 35C204 devices have a separate ready/busy signal pin (RDY/BUSY) to output the programming status signal. The DO signal stays in high impedance throughout the programming cycle and therefore will not interfere with the DI signal in a shared DI/DO configuration.

On the 93C46, 35C102 and 35C104 serial E^2PROMs, the programming status signal can be

read on the DO pin by bringing CS high after initiating a programming cycle. In a 4-signal interface, after a programming cycle is complete, the status signal is reset to high impedance by the start bit of the next instruction (Fig. 3).

In a shared DI/DO configuration, the '1' status signal on DO can be clocked into the device as a start bit and reset the status signal before it can be read. This can interfere with the DI signal for the next instruction cycle. The following steps are recommended to avoid these conditions for a 3-signal interface (Fig. 4):

1) The clock (SK) should be stopped after shifting in the programming instruction. This prevents the '1' ready status from resetting the status signal before it can be read.

2) After reading the '1' ready status, at least one clock pulse should be input to the device while the DI/DO signal is '1' in order to reset the status signal.

3) CS should then be brought low to reset the instruction logic.

The next instruction can now be executed without any contention from the DO signal.

Figure 1a. DI/DO contention timing during read cycle

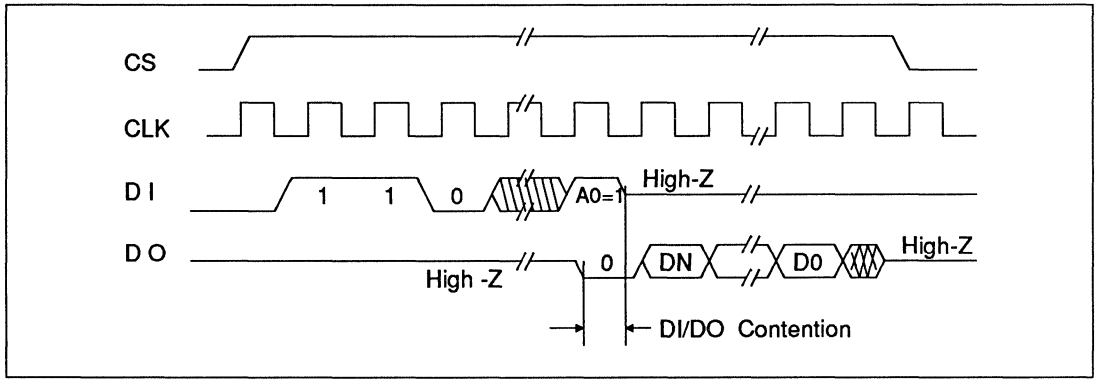


Figure 1b. Current path

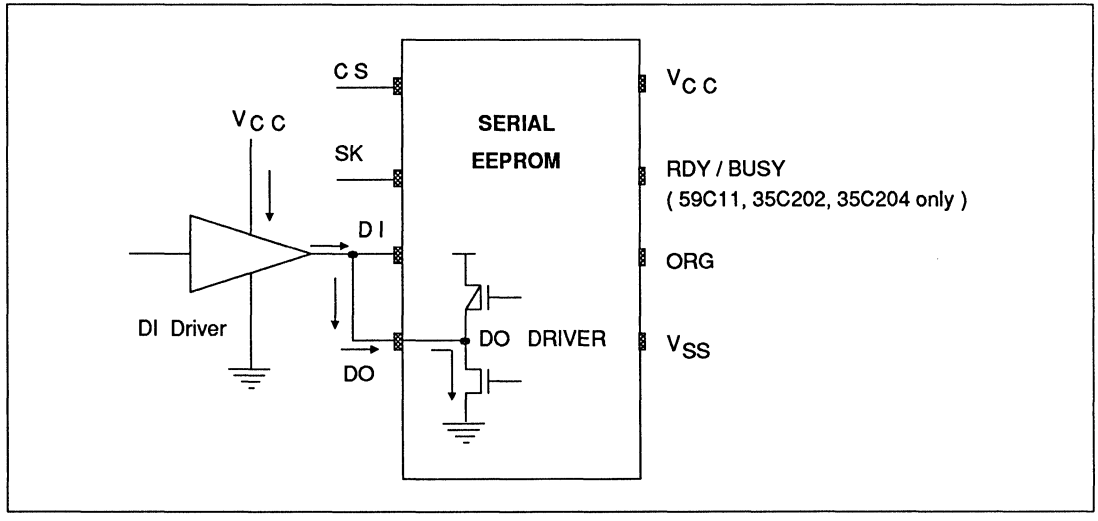


Figure 2. Possible configurations to mimimize problems due to READ contention

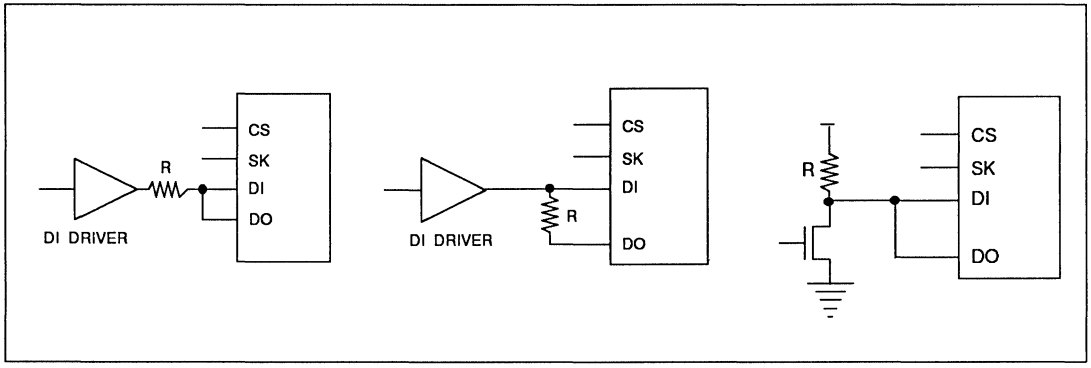


Figure 3. Programming instruction and status reset with 4-signal interface

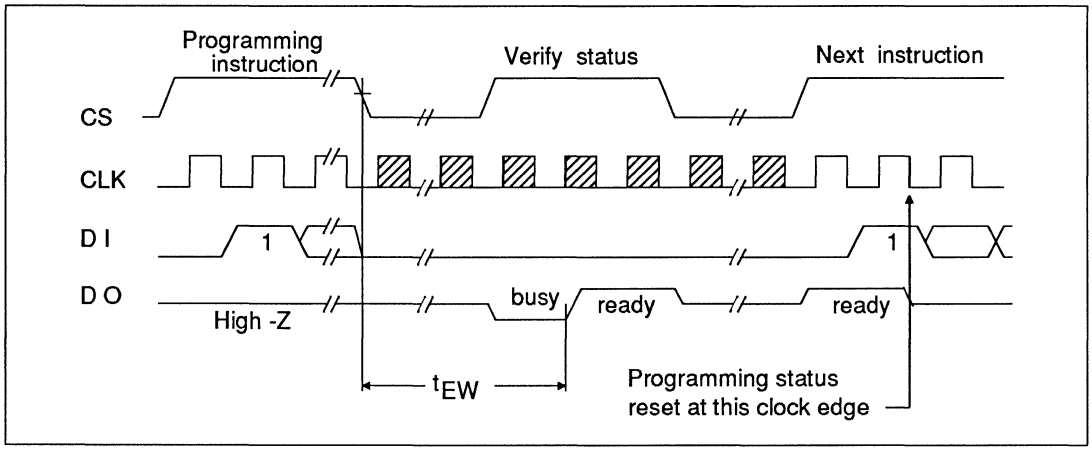
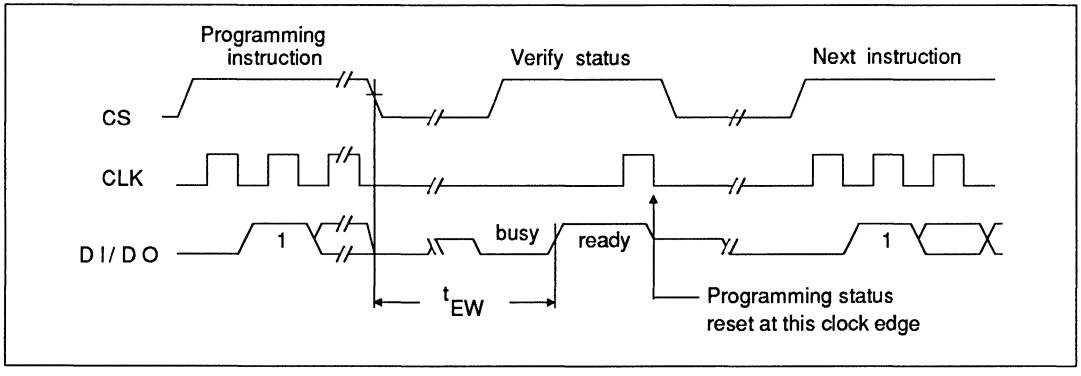


Figure 4. Programming instruction and status reset with 3-signal interface



Serial E^2PROM Programming Time Optimization

Using the CAT59C11 and CAT93C46 in 8 and 16-bit word organization

by Christophe Chevallier
3/88

Many applications with serial E^2PROMS require the storage of bytes. The best way to optimize programming speed is to program 2 bytes at a time, using the x16 organization, and then switch to the byte organization for the read operation.

In the 16-bit organization, 16 bits are programmed simultaneously. The write time is the same for 8 or 16 bits : maximum is 10ms. Writing the whole array (128 bytes) this way will save 0.64s.

To operate the E^2PROM this way, the processor controlling the data transfer should control the ORG pin (pin 6). At V_{IL} the chip is in the x8 (byte) organization, at V_{IH} the chip is in the x16 (word) organization.

Getting into programming mode
Before programming the memory, an EWEN (erase/write enable) operation should be performed. It needs to be done only once after the chip has been powered up. To protect the memory against undesirable write operations, the programming operations can be disabled by doing an EWDS (erase/write disable). It is safe to perform an EWDS if the chip is not being programmed, to avoid a false write in case of power transients. These operations (EWEN, EWDS) can be performed with the ORG pin high or low. Changing the state of the ORG pin will not change the status of the chip whether programming is enabled or disabled.

To write a 16-bit word, once the ORG and the CS pins are high, the start bit and the write opcode "01" are entered, followed by the 6-bit address (for a 1Kbit memory) and the 2 data bytes to be written. Since the device is functionally static, the SK clock can be maintained high or low long enough to give time to the processor to fetch the second data byte. The programming will start at the end of the data acquisition (59C11) or when CS goes down (93C46).

Reading at the correct address
The internal memory, in the byte organization, is divided into 2 pages of 64 bytes, the high page with A6=1 and the low page with A6=0. When writing a 16-bit word, the first 8 bits entered correspond to the high page address, the last 8 bits to the low page address (see bit maps and example). Using hexadecimal notation, the low page addresses are 0 to 3F, the high page addresses are 40 to 7F. In the 16-bit organization, only the addresses 0 to 3F are used. To get the byte address of the first byte entered, add 40 to the address used in the x16 mode. (In the example, 40 + 2E = 6E).

For example, consider the following operations:

Using x16 mode, WRITE at address 2E the data A65B. (See map 1). This will be done with ORG pin high, entering a 6-bit address.

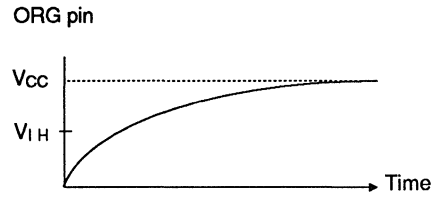
Using x8 mode (ORG pin low, entering a 7-bit address), a READ at address 2E wil output 5B, a READ at address 6E will output A6. (See map 2).

Floating the ORG pin
The ORG pin can be left floating, in this case an internal pull-up resistor will bring the pin high, selecting the 16-bit organization. When switching the ORG pin from V_{IL} to floating, care should be taken to leave enough time for the ORG pin to reach V_{IH}.

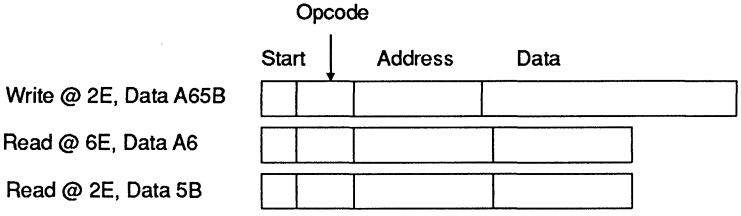
This time depends on the capacitance of the line arriving on the ORG pin. The internal pull-up is small, in order to stay within the 10µA input leakage specification. Typically, the leakage current on this pin is around 5µA at V_{IL} = 0V, and will decrease at higher input voltage.

Therefore, for a 100pF line capacitance, it will require T = C V / I = 100pF x 2V / 2.5µA (average pull-up current). T = 80µs

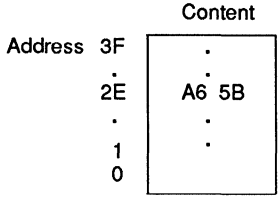
In this example, the processor should wait 100µs after releasing the ORG pin before starting a new operation. The best way to avoid this wait is to drive the ORG pin high instead of letting it float.



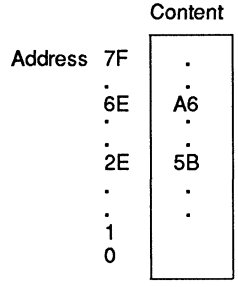
DIN / DOUT PATTERNS



LOGICAL BIT MAP 1: x 16 ORGANIZATION



LOGICAL BIT MAP 2: x 8 ORGANIZATION



CAT93C46 / CAT35C102 to 8051 Microcontroller Communication

Using the 8051's Built-in Shift Register

By Jim Troutner
5/88

The CAT93C46 and CAT35C102 are serial access E^2PROMs intended for use with many of today's standard microcontrollers and microcomputers. To operate the serial E^2PROM, first select the device by driving the CS pin to a logic one state, and shift in the instructions, address, and data into the E^2PROM's DI pin. All data is shifted in on the rising edge of the SK clock, while data being read from the device appears at the DO pin a short time delay (tpd) after the rising edge of the SK clock.

This all seems to be very straight forward and in most applications few problems will be encountered. However in some cases where it is desired to interface to microcontrollers with built in shift registers, such as the 8051, some special problems must be considered.

First, the instruction, address, and data pertaining to the memory device can range from 9 bits (for the CAT93C46 organized as 64 X 16) to as many as 12 bits (for the CAT35C104 organized as 512 X 8). In many microcontrollers, however, the built-in shift register will send and receive data only 8 bits at a time. This problem can be solved by shifting all the extra bits (required to make a multiple of 8) into the memory as zeros before the start bit is sent (all leading zeros shifted into the E^2PROM will be ignored).

Secondly, the clock line on some of these microcontrollers is initially a logic one (a clock consist of a falling edge and then a rising edge). The problem here is that the E^2PROM requires the last clock of any operation to have a falling edge before the E^2PROM is deselected. With the 8051 (or any other microcontroller that clocks in the same manner) the falling edge of the first clock is ignored, and the last clock is left in the logic one state.

The solution here would be to simply add one additional clock pulse to the SK pin before deselecting the device. Another solution (for those processors that must send 8 clocks) is to send one byte of zeros then deselect the device. Additional zeros clocked into the E^2PROM after the instruction, address, and data are shifted in will be ignored.

Additionally, communication using the processor's built in shift register will require that the DI and DO pins of the E^2PROM be wired together to form a common DI/O pin. This can be a problem. After an E^2PROM erase or write operation, the DO pin comes out of its high impedance state to indicate the E^2PROM's ready/busy status. This status must be cleared and the DO pin returned to high impedance before any additional operations can be sent to the E^2PROM. To return the DO pin to its high impedance state, deselect and then reselect the E^2PROM to start the erase or write operation. At this time, the DO pin will be driven to a logic zero state to indicate a busy status. Once accomplished, all that needs to be done is to stop the SK clock and monitor the DO pin until it indicates a ready state, then clock the status into the DI pin (DI and DO are tied). The DO will return to the high impedance state on the falling edge of the clock. If 8 clocks must be sent at a time, due to processor limitation, then when the E^2PROM status indicates it is ready, shift a byte of zeros to the E^2PROM before deselecting it. What really occurs is the processor tries to shift zeros into the E^2PROM, but the DO pin is at logic 1 and will hold the DI pin high. After the one is clocked in, the DO pin will return to high impedance and the remainder of the byte from the processor will be clocked into the E^2PROM as

zeros. Deselect the E^2PROM after returning the DO pin to the high impedance state.

An example program has been provided containing all the 8051 routines needed to exercise the CAT93C46, CAT35C102 and CAT35C104. The connection of the memory device to the 8051 is illustrated in Figure 1. In this scheme the E^2PROM's CS pin could have been connected to any available I/O line, and the ORG pin would probably be wired to Vcc or GND depending on the application. The DI pin and DO pin of the E^2PROM are wired together to form a common DI/O pin, and must be connected (through a current limiting resistor) to the RxD pin (port 3, pin 0) of the 8051. The clock of the the 8051 shift register appears at the TxD pin (port 3, pin 1).

This program utilizes the built in serial port of the 8051 set to the mode 0 configuration. This configuration defines the serial port of the 8051 as an 8 bit shift register which will receive and send data using the RxD pin as data, and the TxD pin as clock. The clock frequency of the shift register is defined as the 8051 oscillator frequency divided by 12. Therefore care must be taken not to exceed the maximum SK clock frequency of the E^2PROM by adjusting the 8051 oscillator appropriately.

The basic flow of the program is illustrated in Figure 2, and a complete assembled listing has also been provided. Subroutines in this program are used to enable the E^2PROM for a write, to erase the entire E^2PROM memory array, and to write or read a particular memory address within the E^2PROM array.

In this application the 8051 does allow programmer access to the shift register clock pin (port 3, pin 1), therefore with this processor it is not necessary to send 8 additional clocks when only one additional clock is needed.

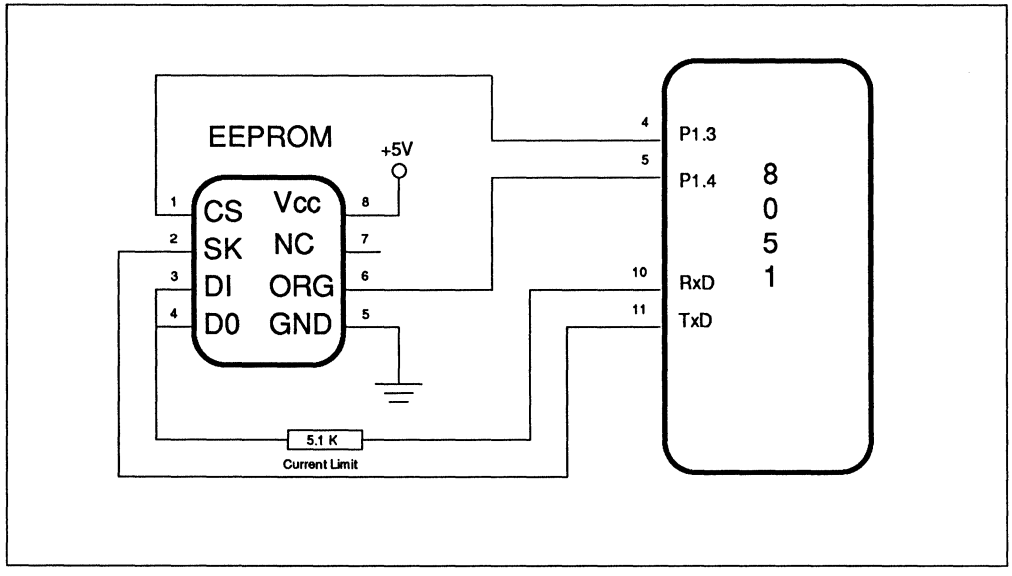


Figure 1.

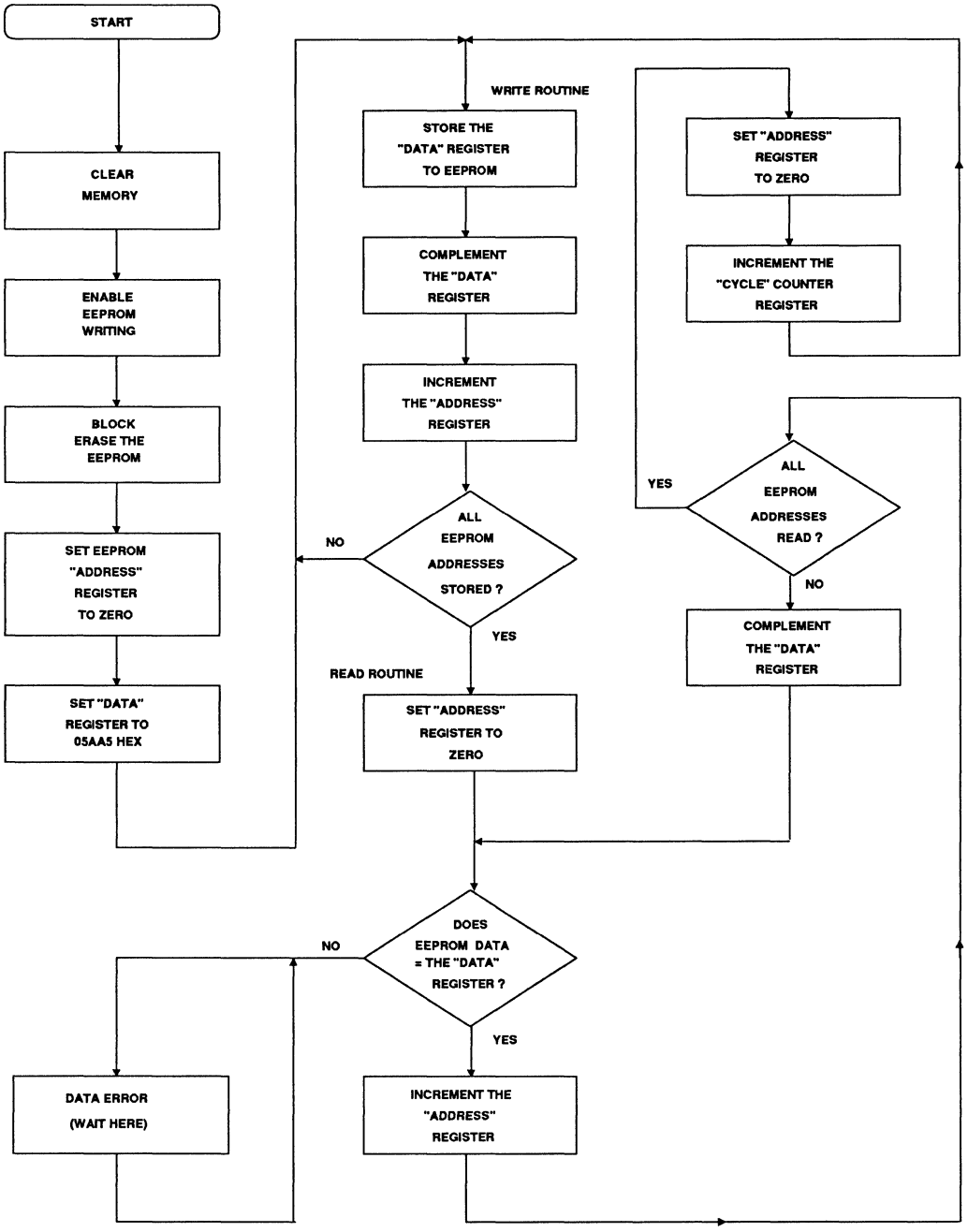

START
CLEAR MEMORY
ENABLE EEPROM WRITING
BLOCK ERASE THE EEPROM
SET EEPROM "ADDRESS" REGISTER TO ZERO
SET "DATA" REGISTER TO 05AA5 HEX
WRITE ROUTINE
STORE THE "DATA" REGISTER TO EEPROM
COMPLEMENT THE "DATA" REGISTER
INCREMENT THE "ADDRESS" REGISTER
ALL EEPROM ADDRESSES STORED ?
NO
YES
READ ROUTINE
SET "ADDRESS" REGISTER TO ZERO
SET "ADDRESS" REGISTER TO ZERO
INCREMENT THE "CYCLE" COUNTER REGISTER
ALL EEPROM ADDRESSES READ ?
YES
NO
COMPLEMENT THE "DATA" REGISTER
DOES EEPROM DATA = THE "DATA" REGISTER ?
NO
YES
DATA ERROR (WAIT HERE)
INCREMENT THE "ADDRESS" REGISTER

Figure 2.


```
< ASM51 > CROSS ASSEMBLER VER.2.5m    ASSEMBLE LIST DATE:          PAGE:   1
CAT EEPROM - 8051 I/O ROUTINES
LOC. OBJECT            LINE    STATEMENT                        C46S_16.ASM
                          1    ;
                          2            $TITLE(CAT EEPROM - 8051 I/O ROUTINES)
                          3    ;       Jim Troutner
                          4    ;       Catalyst Semiconductor
                          5    ;       Date 01/15/88
                          6
                          7    ;       This routine drives the EEPROM using the 8 bit
                          8    ;       shift register (in mode 0) of the 8051.
                          9
                         10    ;*************************************************************************
                         11    ;         8051 Port Assignments
                         12    ;*************************************************************************
                         13
                         14
    00B0                 15    DATAIO    BIT      P3.0       ;SERIAL DATA INPUT/OUTPUT PIN (RxD)
    00B1                 16    SCLK      BIT      P3.1       ;SERIAL CLOCK (TxD)
    0093                 17    EESEL     BIT      P1.3       ;EEPROM CHIP SELECT
    0094                 18    EEORG     BIT      P1.4       ;EEPROM ORGANIZATION
    00B0                 19    EESTAT    BIT      P3.0       ;EEPROM STATUS WILL APPEAR HERE
                         20
                         21    ;*************************************************************************
                         22    ;         8051 DATA MEMORY MAP
                         23    ;*************************************************************************
----                     24            DSEG 0030
                         25            ORG      030H
0030                     26    EE_ADDR:  DS       1          ;EEPROM data address.
0031                     27    INS_H:    DS       1          ;EEPROM instruction and address.
0032                     28    INS_L:    DS       1
0033                     29    DATAH:    DS       1          ;Data to be stored to, or compared
0034                     30    DATAL:    DS       1          ; to EEPROM data.
0035                     31    R_DATH:   DS       1          ;Data read from the EEPROM.
0036                     32    R_DATL:   DS       1
0040                     33            ORG      040H
0040                     34    CYCMAX:   DS       4          ;Number of write/read cycles before
0044                     35    CYCCNT:   DS       1          ; a failure.
                         36
0060                     37            ORG      060H
0060                     38    STACK:    DS       31
                         39
                         40
                         41               $EJECT
```

```
< ASM51 > CROSS ASSEMBLER VER.2.5m    ASSEMBLE LIST DATE:          PAGE:   2
CAT EEPROM - 8051 I/O ROUTINES
 LOC. OBJECT            LINE    STATEMENT                    C46S_16.ASM

                          42    ;*************************************************************************
                          43    ;        CONSTANTS
                          44    ;*************************************************************************
                          45
                          46
                          47    ; NOTE: User must enter the number of DATA bits, and  ADDRESS bits
                          48    ;        required for the EEPROM being tested. This program will
                          49    ;        automatically adjust the ORG pin of the EEPROM depending
                          50    ;        on the value entered for D_BITS.
                          51    ;
                          52    ;       This program was designed to address the CAT93C46
                          53    ;        or the CAT35C102 in an 8 bit or 16 bit data organization.
                          54    ;       It will also address the CAT35C104 in the 16 bit data
                          55    ;        organization only.
                          56    ;
                          57    ;       To modify this program to operate with a specific device
                          58    ;        such as the CAT93C46, first select the data organization
                          59    ;        mode desired (8 bits or 16 bits) by changing the D_BITS
                          60    ;        equate below. Then check the CATALYST DATA BOOK to
                          61    ;        determine the number of address bits required for that
                          62    ;        device at that data organization, and change the A_BITS
                          63    ;        below to the specified number of address bits. i.e  If
                          64    ;        A_BITS = 6, and D_BITS = 16 then the program is set up
                          65    ;        for the CAT93C46 in the 64 X 16 mode.
                          66    ;
                          67    ;      To run the program simply re-assemble it, load it the
                          68    ;      emulator, and run it.
                          69
  0006                    70    A_BITS   EQU       6              ;Number of address bits (6,7, or 8).
  0010                    71    D_BITS   EQU       16             ;Number of data bits (8, or 16).
                          72
  0004                    73    LONG     EQU       A_BITS - 2     ;Number used to adjust long
                          74                                      ; EEPROM instructions.
  0040                    75    ADDMAX   EQU   01H SHL A_BITS     ;Max EEPROM address + 1
                          76
                          77              $EJECT
```


```
< ASM51 > CROSS ASSEMBLER VER.2.5m    ASSEMBLE LIST DATE:          PAGE:   3
CAT EEPROM - 8051 I/O ROUTINES
 LOC. OBJECT            LINE     STATEMENT                    C46S_16.ASM

                          78     ;*********************************************************************
                          79     ;        EEPROM INSTRUCTIONS
                          80     ;*********************************************************************
                          81                                          ;SHORT INSTRUCTIONS
                          82                                          ; 1 START, 2 INSTRUCTION BITS
  0001                    83     READ_H   EQU       HIGH(110B SHL A_BITS)  ;READ MEMORY @ SPECIFIED ADDRESS
  0080                    84     READ_L   EQU       LOW(110B SHL A_BITS)
  0001                    85     ERASE_H  EQU       HIGH(111B SHL A_BITS)  ;ERASE CELL @ SPECIFIED ADDRESS
  00C0                    86     ERASE_L  EQU       LOW(111B SHL A_BITS)
  0001                    87     WRITE_H  EQU       HIGH(101B SHL A_BITS)  ;WRITE DATA TO SPECIFIED ADDRESS
  0040                    88     WRITE_L  EQU       LOW(101B SHL A_BITS)
                          89
                          90                                          ;LONG BIT INSTRUCTIONS
                          91                                          ; 1 START, 4 INSTRUCTION BITS
  0001                    92     EWEN_H   EQU       HIGH(10011B SHL LONG)  ;ENABLE PROGRAMING
  0030                    93     EWEN_L   EQU       LOW(10011B SHL LONG)
  0001                    94     EWDS_H   EQU       HIGH(10000B SHL LONG)  ;DISABLE PROGRAMING (DEFAULT)
  0000                    95     EWDS_L   EQU       LOW(10000B SHL LONG)
  0001                    96     ERAL_H   EQU       HIGH(10010B SHL LONG)  ;ERASE ALL ADDRESSES
  0020                    97     ERAL_L   EQU       LOW(10010B SHL LONG)
  0001                    98     WRAL_H   EQU       HIGH(10001B SHL LONG)  ;WRITE DATA TO ALL ADDRESSES
  0010                    99     WRAL_L   EQU       LOW(10001B SHL LONG)
                         100
  0001                   101     TEST_H   EQU       HIGH(06000H SHR A_BITS)
  0080                   102     TEST_L   EQU       LOW(06000H SHR A_BITS)
                         103
                         104              $EJECT
```

```
< ASM51 > CROSS ASSEMBLER VER.2.5m    ASSEMBLE LIST DATE:          PAGE:   4
CAT EEPROM - 8051 I/O ROUTINES
LOC. OBJECT            LINE    STATEMENT                      C46S_16.ASM

                        105
----                    106             CSEG 0000
                        107             ORG 0000
                        108
                        109     ;*************************************************************************
                        110     ;       PROGRAM START
                        111     ;*************************************************************************
                        112
                        113     START:
0000 02 00 30           114             JMP   PSTINT        ;Jump over Interrupt routines
                        115
0030                    116             ORG  0030H
                        117
                        118     PSTINT:                     ;Program starting point
0030 C2 93              119             CLR   EESEL         ;Deselect the EEPROM
0032 74 10              120             MOV   A,#D_BITS     ;Set the EEPROM ORG pin.
0034 B4 08 02    [0039] 121             CJNE  A,#8,ORG16
                        122     ORG8:
0037 C2 94              123             CLR   EEORG
                        124     ORG16:
0039 75 81 60           125             MOV   SP,#STACK     ;Stack = 60H -- 7FH
003C E4                 126             CLR   A             ;Clear the RAM
003D 78 7F              127             MOV   R0,#7FH
                        128     CLRLOP:
003F F6                 129             MOV   @R0,A
0040 D8 FD       [003F] 130             DJNZ  R0,CLRLOP
                        131
0042 11 93       [0093] 132             ACALL EN_EE         ;Enable the EEPROM for writing
0044 11 C9       [00C9] 133             ACALL BLKERA        ;Erase the EEPROM
                        134
0046 75 34 5A           135             MOV   DATAL,#5AH    ;Init the store data registers
0049 75 33 A5           136             MOV   DATAH,#0A5H
                        137
                        138     STORE:
004C 11 D6       [00D6] 139             ACALL EE_STR        ;Store data to the EEPROM
                        140
004E 63 34 FF           141             XRL   DATAL,#0FFH   ;Complement the data located
0051 63 33 FF           142             XRL   DATAH,#0FFH   ; in DATAL and DATAH
                        143
0054 11 83       [0083] 144             ACALL INCADD        ;Increment and test address
0056 50 F4       [004C] 145             JNC   STORE         ;Not finished store next addr.
                        146
                        147     READ:
0058 31 02       [0102] 148             ACALL EE_RD         ;Read data from the EEPROM
                        149
005A E5 36              150             MOV   A,R_DATL      ;Compare the EEPROM read data
005C B5 34 14    [0073] 151             CJNE  A,DATAL,ERROR
005F 30 94 05    [0067] 152             JNB   EEORG,DATOK   ;Data ok if in 8 bit mode.
0062 E5 35              153             MOV   A,R_DATH
0064 B5 33 0C    [0073] 154             CJNE  A,DATAH,ERROR
```

```
< ASM51 > CROSS ASSEMBLER VER.2.5m    ASSEMBLE LIST DATE:          PAGE:   5
CAT EEPROM - 8051 I/O ROUTINES
LOC. OBJECT            LINE    STATEMENT                        C46S_16.ASM

                        155     DATOK:
0067 11 83      [0083]  156             ACALL INCADD
0069 40 0A      [0075]  157             JC    INCCYC          ;Inc the cycle counter
                        158
006B 63 34 FF           159             XRL   DATAL,#0FFH     ;Complement the data located
006E 63 33 FF           160             XRL   DATAH,#0FFH     ; in DATAL and DATAH
                        161
0071 01 58      [0058]  162             AJMP  READ
                        163
                        164     ERROR:
0073 80 FE      [0073]  165             SJMP  ERROR           ;Data error,  wait here
                        166
                        167     INCCYC:
                        168                                   ;Increment the cycle counter
0075 78 44              169             MOV   R0,#CYCCNT
0077 D3                 170             SETB  C
0078 79 04              171             MOV   R1,#(CYCCNT-CYCMAX)
                        172     NXT:
007A E4                 173             CLR   A               ;Each time all the EEPROM addresses
007B 36                 174             ADDC  A,@R0           ; are written and then read correctly
007C D4                 175             DA    A               ; the register 'CYCCNT' is incremented
007D F6                 176             MOV   @R0,A           ; by one. The counter is stored in
007E 18                 177             DEC   R0              ; BCD so that it can be read directly
007F D9 F9      [007A]  178             DJNZ  R1,NXT          ; from data memory as a decimal number.
0081 01 4C      [004C]  179             AJMP STORE
                        180
                        181     ;*********************************************************************
                        182     ;         Subroutine                      " I N C A D D "
                        183     ;*********************************************************************
                        184
                        185     ; Routine will increment the address located in the EE_ADDR register
                        186     ; by one. If an overflow occurs, the address is set to 000H and
                        187     ; the routine will return with the carry bit set.
                        188
                        189     ;ENTRY:  EE_ADDR register = data address
                        190
                        191     ;EXIT:   EE_ADDR = New data address
                        192     ;        IF C = 1, then address was reset
                        193     ;           C = 0, then increment was OK
                        194     ;        Registers altered = AC, EE_ADDR, C flag.
                        195     INCADD:
0083 05 30              196             INC   EE_ADDR
0085 E5 30              197             MOV   A,EE_ADDR
0087 60 03      [008C]  198             JZ    OVRFLO
0089 B4 40 05   [0091]  199             CJNE  A,#ADDMAX,INCOK
                        200     OVRFLO:
008C 75 30 00           201             MOV   EE_ADDR,#0
008F D3                 202             SETB  C
0090 22                 203             RET
                        204     INCOK:
0091 C3                 205             CLR   C
0092 22                 206             RET
                        207
                        208     ;END SUB
```

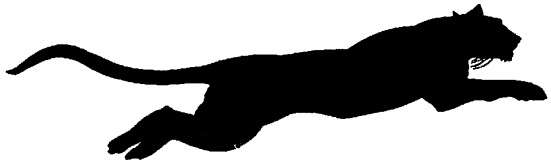
```
< ASM51 > CROSS ASSEMBLER VER.2.5m    ASSEMBLE LIST DATE:          PAGE:   6
CAT EEPROM - 8051 I/O ROUTINES
 LOC. OBJECT            LINE    STATEMENT                      C46S_16.ASM

                        209     ;*********************************************************************
                        210     ;       Subroutine                    " E N _ E E "
                        211     ;*********************************************************************
                        212
                        213     ; Routine will enable the EEPROM for data writing.
                        214
                        215     ;ENTRY:  Nothing required
                        216
                        217     ;EXIT:   Registers altered = INS_H, INS_L, and P1.3
                        218
                        219     EN_EE:
0093 75 31 01           220             MOV   INS_H,#EWEN_H      ;Store the Enable EEPROM write
0096 75 32 30           221             MOV   INS_L,#EWEN_L      ; instruction to the INS buffer.
0099 11 B7      [00B7]  222             ACALL  MIRROR            ;Swap the bits within the bytes
                        223                                      ; to shift out.
009B 11 A0      [00A0]  224             ACALL OUT16
009D 02 01 18           225             JMP   LSTCLK
                        226
                        227     ; END SUB
                        228     ;*********************************************************************
                        229     ;       Subroutine                     " O U T 1 6 " , " O U T 8 "
                        230     ;*********************************************************************
                        231
                        232     ; Routine will shift out the INS buffer to the EEPROM.
                        233
                        234     ;ENTRY:  INS_H and INS_L must contain the EEPROM instruction
                        235     ;        and address (or data to send to EEPROM).
                        236
                        237     ;EXIT:   Registers altered = P1.3
                        238
                        239     OUT16:
00A0 D2 B1              240             SETB   SCLK
00A2 D2 93              241             SETB   EESEL             ;Enable the EEPROM.
                        242     OUT16_2:
00A4 C2 99              243             CLR    TI
00A6 85 31 99           244             MOV    SBUF,INS_H        ;Shift out first 8 bits.
                        245     WFRST8:
00A9 30 99 FD   [00A9]  246             JNB    TI,WFRST8
                        247     OUT8:                            ;When entering at OUT8, the
                        248                                      ; EEPROM must already be selected.
00AC C2 99              249             CLR    TI
00AE 85 32 99           250             MOV    SBUF,INS_L        ;Shift out last 8 bits.
                        251     WLST8:
00B1 30 99 FD   [00B1]  252             JNB    TI,WLST8
00B4 C2 99              253             CLR    TI
00B6 22                 254             RET
                        255
                        256     ;END SUB
```

```
< ASM51 > CROSS ASSEMBLER VER.2.5m    ASSEMBLE LIST DATE:          PAGE:   7
CAT EEPROM - 8051 I/O ROUTINES
 LOC. OBJECT            LINE    STATEMENT                      C46S_16.ASM

                         257    ;*********************************************************************
                         258    ;        Subroutine                    " M I R R O R "
                         259    ;*********************************************************************
                         260    ; When shifting data out of the 8051, the data is shifted out LSB
                         261    ;  to MSB. When shifting data into the 8051, data is shifted in
                         262    ;  MSB to LSB.  These routines were written to represent the
                         263    ;  EEPROM Instruction, address, and data in the same manner as
                         264    ;  presented in the Catalyst data sheet, however this data must
                         265    ;  under go a bit swap (i.e. bit7  bit0, bit6  bit1, and so
                         266    ;  on) just prior to shifting it out to accommodate the LSB
                         267    ;  first output shifting of the 8051.  Since the 8051 will shift
                         268    ;  the data in MSB first, no swap is necessary when data is read
                         269    ;  from the EEPROM.
                         270
                         271    ; ENTRY:  INS_H, and INS_L = EPROM instruction plus address, or data
                         272
                         273    ; EXIT: Both INS_H and INS_L have a MSB to LSB bit swap.
                         274    ;       Registers altered = AC, INS_H, INS_L, R1, and C flag.
                         275
                         276
                         277    MIRROR:
00B7 E5 31               278             MOV   A,INS_H
00B9 79 08               279             MOV   R1,#8          ;Set up bit counter
                         280    FIN_M:
00BB 13                  281             RRC   A              ;Shift INS_H (AC) LSB into the
00BC C5 32               282             XCH   A,INS_L        ; LSB of INS_L while shifting the
00BE 33                  283             RLC   A              ; MSB of INS_L into the MSB of
00BF C5 32               284             XCH   A,INS_L        ; INS_H (AC).
00C1 D9 F8       [00BB]  285             DJNZ  R1,FIN_M       ;Check the bit counter.
00C3 13                  286             RRC   A              ;Shift last bit into INS_L
00C4 C5 32               287             XCH   A,INS_L        ;Store the swapped INS_L to INS_L.
00C6 F5 31               288             MOV   INS_H,A        ;Store the swapped INS_H to INS_H.
00C8 22                  289             RET
                         290
                         291    ; END SUB
```

```
< ASM51 > CROSS ASSEMBLER VER.2.5m    ASSEMBLE LIST DATE:          PAGE:   8
CAT EEPROM - 8051 I/O ROUTINES
 LOC. OBJECT            LINE    STATEMENT                      C46S_16.ASM

                         292    ;*********************************************************************
                         293    ;       Subroutine                    " B L K E R A "
                         294    ;*********************************************************************
                         295
                         296    ; Routine will erase the entire EEPROM memory
                         297
                         298    ;ENTRY:  Nothing required
                         299
                         300    ;EXIT:   Registers altered = INS_H, and INS_L
                         301
                         302    BLKERA:
00C9 75 31 01            303             MOV   INS_H,#ERAL_H      ;Store the Erase ALL instruction
00CC 75 32 20            304             MOV   INS_L,#ERAL_L      ; to the INS buffer.
00CF 11 B7       [00B7]  305             ACALL  MIRROR            ;Swap the bits within the bytes
                         306                                      ; to shift out.
00D1 11 A0       [00A0]  307             ACALL OUT16
00D3 02 00 EE            308             JMP   OUTRET
                         309
                         310    ;END SUB
                         311    ;*********************************************************************
                         312    ;       Subroutine                    " E E _ S T R
                         313    ;*********************************************************************
                         314
                         315    ; Routine will store the data located in DATAH and DATAL into
                         316    ;  the EEPROM at the location pointed to by EE_ADDR. In 8 bit
                         317    ;  data mode only DATAL will be stored to the EEPROM.
                         318
                         319    ; NOTE: The EEPROM must be write enabled.
                         320
                         321    ; ENTRY: EE_ADDR = address in EEPROM to store the data
                         322    ;        DATAH, and DATAL = the data to store to EEPROM
                         323
                         324    ; EXIT:  Registered altered = AC, INS_H, INS_L, and P1.3
                         325
                         326
                         327    EE_STR:
00D6 75 31 01            328             MOV   INS_H,#WRITE_H     ;Store the write instruction
00D9 74 40               329             MOV   A,#WRITE_L         ; plus address to the INS
00DB 45 30               330             ORL   A,EE_ADDR          ; register.
00DD F5 32               331             MOV   INS_L,A
00DF 11 B7       [00B7]  332             ACALL  MIRROR            ;Swap the bits within the bytes
                         333                                      ; to shift out.
00E1 11 A0       [00A0]  334             ACALL OUT16              ;Shift out the instruction.
00E3 85 33 31            335             MOV   INS_H,DATAH
00E6 85 34 32            336             MOV   INS_L,DATAL
00E9 30 94 12    [00FE]  337             JNB   EEORG,ONLY8
                         338    ALL16:
00EC 11 A4       [00A4]  339             ACALL OUT16_2            ;Shift out the DATA.
                         340    OUTRET:
00EE C2 B1               341             CLR   SCLK               ;Falling edge of last clock
00F0 C2 93               342             CLR   EESEL              ;Deselect the EEPROM.
```

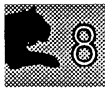
```
< ASM51 > CROSS ASSEMBLER VER.2.5m    ASSEMBLE LIST DATE:          PAGE:   9
CAT EEPROM - 8051 I/O ROUTINES
 LOC. OBJECT            LINE    STATEMENT                      C46S_16.ASM


00F2 D2 93                343            SETB  EESEL             ;Check if EEPROM is ready for
                          344    WAITRDY:                        ; the next operation.
00F4 30 B0 FD     [00F4]  345            JNB   EESTAT,WAITRDY
00F7 D2 B1                346            SETB  SCLK              ;Put DO pin of EEPROM in
00F9 C2 B1                347            CLR   SCLK              ; high Z state.
00FB C2 93                348            CLR   EESEL
00FD 22                   349            RET
                          350    ONLY8:
00FE 11 AC        [00AC]  351            ACALL OUT8
0100 80 EC        [00EE]  352            JMP   OUTRET
                          353
                          354    ;END SUB
                          355    ;*************************************************************************
                          356    ;       Subroutine                      " E E _ R D "
                          357    ;*************************************************************************
                          358
                          359    ; Routine will read the data located at the EEPROM address specified
                          360    ;  by EE_ADDR onto registers R_DATH and R_DATL. If in the 8 bit
                          361    ;  data mode, data is read into the R_DATL register.
                          362
                          363    ; ENTRY: EE_ADDR = address in EEPROM to read the data
                          364
                          365    ; EXIT:  R_DATH, and RDATL = data read from the EEPROM
                          366    ;        Registers altered = AC, INS_H, INS_L, R_DATH, R_DATL
                          367    ;                            P3.1 and P1.3
                          368
                          369
                          370    EE_RD:
0102 75 31 01             371            MOV   INS_H,#READ_H     ;Store the read instruction
0105 74 80                372            MOV   A,#READ_L         ; plus the address to the
0107 45 30                373            ORL   A,EE_ADDR         ; INS register.
0109 F5 32                374            MOV   INS_L,A
010B 11 B7        [00B7]  375            ACALL  MIRROR           ;Swap the bits within the bytes
                          376                                    ; to shift out.
010D 11 A0        [00A0]  377            ACALL OUT16             ;Send the instruction.
010F C2 B1                378            CLR   SCLK              ;Send an extra clock to clear
0111 D2 B1                379            SETB  SCLK              ; the dummy zero from the EEPROM.
0113 30 94 07     [011D]  380            JNB   EEORG,I_ONLY8
                          381    I_ALL16:
0116 31 21        [0121]  382            ACALL IN16              ;Read the data from EEPROM.
                          383    LSTCLK:
0118 C2 B1                384            CLR   SCLK              ;Falling edge of last clock
011A C2 93                385            CLR   EESEL             ;Deselect the EEPROM
011C 22                   386            RET
                          387    I_ONLY8:
011D 31 2B        [012B]  388            ACALL IN8
011F 80 F7        [0118]  389            JMP   LSTCLK
                          390    ;END SUB
```

```
< ASM51 > CROSS ASSEMBLER VER.2.5m    ASSEMBLE LIST DATE:          PAGE:  10
CAT EEPROM - 8051 I/O ROUTINES
 LOC. OBJECT            LINE    STATEMENT                    C46S_16.ASM


                        391     ;*********************************************************************
                        392     ;        Subroutine                    " I N 1 6 " , " I N 8 "
                        393     ;*********************************************************************
                        394
                        395
                        396     ; Routine will shift into the R_DATH, and R_DATL buffer
                        397     ; the data from EEPROM. If 8 bit data mode is selected, the
                        398     ; data is shifted into R_DATL.
                        399
                        400     ;ENTRY:  Nothing required
                        401
                        402     ;EXIT:   R_DATH, and RDATL = EEPROM read data.
                        403     ;        Registers altered = R_DATH, and R_DATL
                        404
                        405     IN16:
0121 C2 98              406             CLR     RI                  ;Reset the receive done flag.
0123 D2 9C              407             SETB    REN                 ;Enable serial input.
                        408     R_W1ST8:
0125 30 98 FD    [0125] 409             JNB     RI,R_W1ST8          ;Wait for the first 8 bits.
0128 85 99 35          410             MOV     R_DATH,SBUF         ;Store first byte to memory.
                        411
                        412     IN8:
012B C2 98              413             CLR     RI                  ;Reset the receive done flag.
012D D2 9C              414             SETB    REN
                        415     R_WLST8:
012F 30 98 FD    [012F] 416             JNB     RI,R_WLST8          ;Wait for last 8 bits.
0132 85 99 36          417             MOV     R_DATL,SBUF         ;Store last byte to memory.
0135 C2 9C              418             CLR     REN                 ;Disable serial input.
0137 C2 98              419             CLR     RI
0139 22                 420             RET
                        421
                        422     ;END SUB
                        423     ;*********************************************************************
                        424
                        425     END


ASSEMBLY END , ERRORS:0
LAST CODE ADDRESS:0139
```



SECTION 8

RELIABILITY & QUALITY ASSURANCE



CATALYST RELIABILITY AND QUALITY ASSURANCE

A commitment to outstanding Quality and Reliability is an integral part of the Catalyst corporate policy. This is embodied in a comprehensive quality program which is extensively documented and structured to meet the highest standards of the most discriminating customer. This program assures quality at all phases of the production process and provides for the prevention and ready detection of discrepancies and for timely and positive corrective action. The quality and reliability programs utilized at Catalyst can be divided into the following areas:

1) Design-in quality and reliability

2) Document Control

3) Incoming inspection

4) Material Traceability

5) In-Line Inspection

6) Subcontractor Control

7) Comprehensive qualification programs

8) Ongoing monitors

9) Thorough production testing

10) Continued quality and reliability improvement

11) Customer Service

By definition, quality is conformance to specification, whether process or procedures, electrical or mechanical, customer or Catalyst Semiconductor, Inc. Similarly, reliability is continued conformance to specification. Therefore, it is necessary for the Quality and Reliability group to be involved in all phases of the design and manufacturing process.

1) Designed in Quality and Reliability

The Catalyst Q/R program begins at the process design as well as circuit design level.

For example:

- Parametric margins for device operations are above and beyond those necessary to simply meet specification.

- Special attention is paid to electrostatic discharge protection (ESD). Every pin is designed to withstand 2000V minimum (Human Body model).

- Attention is also paid to layout and process sensitive problems such as CMOS latch-up. Every device must meet rigid standards and test conditions well beyond those anticipated in normal operation.

- Reliability failure rate and process parameter requirements for qualification are clearly documented for all products at or prior to product conception thereby helping to assure the highest standards of quality and reliability. These standards must be demonstrated at qualification. The involvement of quality and reliability personnel as part of the development team assures that a product manufactured under state-of-the-art technology will continue to be a useful product well into the future.

2) Document Control

The document control group maintains control over all manufacturing specifications, lot travelers, procurement specification and drawings, reticle tapes, and test programs.

They also are charged with the generation and translation of customer specification requirements into Catalyst internal travelers, specifications, and procedures.

Any and all changes to specifications are subject to approval by Engineering and Manufacturing managers.

See Fig. 1 block diagrams on document control on page 8-7.

3) Incoming Inspection

For all purchased materials the manufacturer is required to maintain a high product quality level. The manufacturer's facility must also meet the requirements of Catalyst QC and is subject to periodic audit to verify that the manufacturer is following the required quality procedures and keeping proper records. All manufacturers must be qualified before their aterials may be used in production.

Incoming inspection is performed on each lot of material, with the individual purchasing specification for that material as a standard to determine defective material. Those lots that do not meet the standard are rejected and returned to the manufacturer. The manufacturer must then analyze and report on the failures, stating what corrective action is being performed to correct the problem. Those actions are reviewed by Catalyst and, upon approval, are accepted by Catalyst for implementation by the manufacturer.

4) Material Traceability

Catalyst maintains a complete history of production lots, from incoming to outgoing inspection. Incoming material is inspected and assigned a lot number that is referenced on production travelers thereby identifying that material throughout the production process. In addition, all assembled units are marked with a lot number which provides the neccessary traceability to determine any information about the history of the component or any material used to build that component.

5) In-Line Inspection

Manufacturing facilities used to build Catalyst products are carefully monitored and audited for adequate QC and QA procedures and methods.

Among the myriad of process and quality control procedures that must be in operation the following is a sample:

- Incoming inspection of all materials such as chemicals, wafers, masks, and piece parts.
- Vendor qualification and monitoring data.
- Calibration and maintenance procedures of fab and test equipment.
- Environmental controls over temperature, relative humidity, particle content in clean air facilities, wafer resistivity and bacteria content in deionized water.
- Training procedures for operators.
- Process monitor procedures, frequency and sampling plans.
- $\bar{X}$ and R charts and evidence of corrective action response capability.

Experience has proven that such close control of operators, equipment, and environment is highly effective towards improved quality and increased yields.

Fig. 2a on page 8-8 shows typical in process QC flows utilized by Catalyst vendors to control critical process steps in wafer fab, assembly, and test.

6) Subcontractor Control

All of Catalysts subcontractor facilities and procedures must be qualified before manufacturing is allowed to begin. Every product manufactured must meet Catalyst's quality standards. In preparation for manufacturing for Catalyst, the subcontractor is instructed to use only equipment, materials, conditions, and quality control procedures which are specified or approved by Catalyst. Based on Catalyst instructions, the subcontractor develops detailed manufacturing standards which are approved or qualified by Catalyst. During manufacturing, Catalyst provides the subcontractor with technical and quality control support. The subcontractor must submit process quality control reports periodically. In addition the subcontractors facility is subject to periodic audit by Catalyst, and the products are checked regularly against Catalyst quality standards.

A summary of the relationship between Catalyst and the subcontractor is shown in Fig. 3 on page 8-10.

7) Comprehensive Qualification Programs

Catalyst's extensive Qualification Program is the backbone of the quality program. Device, process, and package qualification programs are thoroughly documented and required failure rate criteria are established as part of the development cycle. Only engineering samples are allowed to be delivered without meeting the qualification criteria. The qualification programs have their basis and are in accordance with MIL-STD-883C.

Historically, memory products have been the test vehicle for bringing new technology to the marketplace. During qualification and subsequent reliability monitor program, the memory devices are thoroughly analyzed for failure mechanisms and the process technology altered to eliminate them. After completion of this process the technology is able to be transferred to other types of devices and products, i.e., the smart card micro.

For example, the following is a list of reliability tests necessary to be performed on the qualification of a new wafer fab technology for E^2PROMs. Samples from the first 5 wafer lots must pass these tests:

1) 125° C operating life, 1000 hrs.
2) 150° C data retention storage, 1000 hrs. after 10K cycles.
3) Endurance cycle/bake @ 150° C.
4) Temp. cycle, -65 /+150° C, 1000 cycles
5) HAST, 48 hr, +5V, 94% RH, 38 PSI
6) Pressure Pot, 168 hours
7) E.S.D. (1.5K /100pf), 2000 volts all pins
8) Latch-up sensitivity, 100 mA/pin

It is from these tests that information on infant mortality, long term failure rates, and associated failure mechanisms is determined. The data from these tests are published in a reliability report and made available to our customers.

Similarly, samples of a new package technology or facility must undergo their own extensive qualification to assure the highest standards in mechanical integrity.

8) Ongoing Monitor Program

While initial qualification is a key step in product introduction, it would be meaningless if products were not monitored throughout their product life. Each quarter production lots are randomly sampled for the monitor program and submitted to many of the same comprehensive tests used for initial qualification. As in the qualification process, any device failures are carefully analyzed using bench testers, microscopes, and Scanning Electron Microscope (S.E.M.) to determine failure mechanisms and their importance to the process and the device. In this way, Catalyst reliability engineers can develop extensive data on long term problems that will quickly and accurately determine why a product may have failed and generate the necessary feedback to the applicable engineering groups.

An example of the monitor program for E^2PROM technology:

1) 125° C operating life, 1000 hrs.
2) 150° C data retention storage, 1000 hrs. after 10K cycles.
3) Endurance cycle/bake @ 150° C.
4) Temp cycles, 1000 cy, -65 /150° C.
5) H.A.S.T. test, 48 hrs., +5V, 94% R.H., 38 psi. *
6) Pressure Pot, 168 hrs. *

(* Plastic package only)

As in qualification, reliability failure rate goals are clearly documented and results are carefully scrutinized to ensure goals are met.

9) Thorough Production Testing

Every device manufactured by Catalyst must be thoroughly tested for electrical functionality prior to shipment. Test programs are validated prior to qualification to ensure the required limits, as determined in the data sheet for each product, are being met. Not only are the operating specifications carefully scrutinized, but also any and all reliability requirements must be checked. See Fig. 4.

For example, one of the most important specifications for E^2PROMs is the ability to perform 10,000 write/erase cycles and have 10 years data retention. Catalyst has taken the position that all outgoing products will meet specifications including long term reliability requirements. Therefore, 100 percent of all units are tested for reliability during the test flow. These tests are specifically designed to eliminate reliability rejects from reaching the customer as well as infant mortality type rejects.

10) Continued R/QA Improvement

In order to achieve its goal as an industry leader in reliability and quality, Catalyst is continually pushing improvements in design and process. Before any changes are implemented in a qualified technology, test chips are generated and again rigorously tested. If an improvement in process or design is to be implemented, it must again be qualified prior to shipment of any revenue parts. The same is true for any significant change in package related materials, facility, or methods.

11) Customer Service

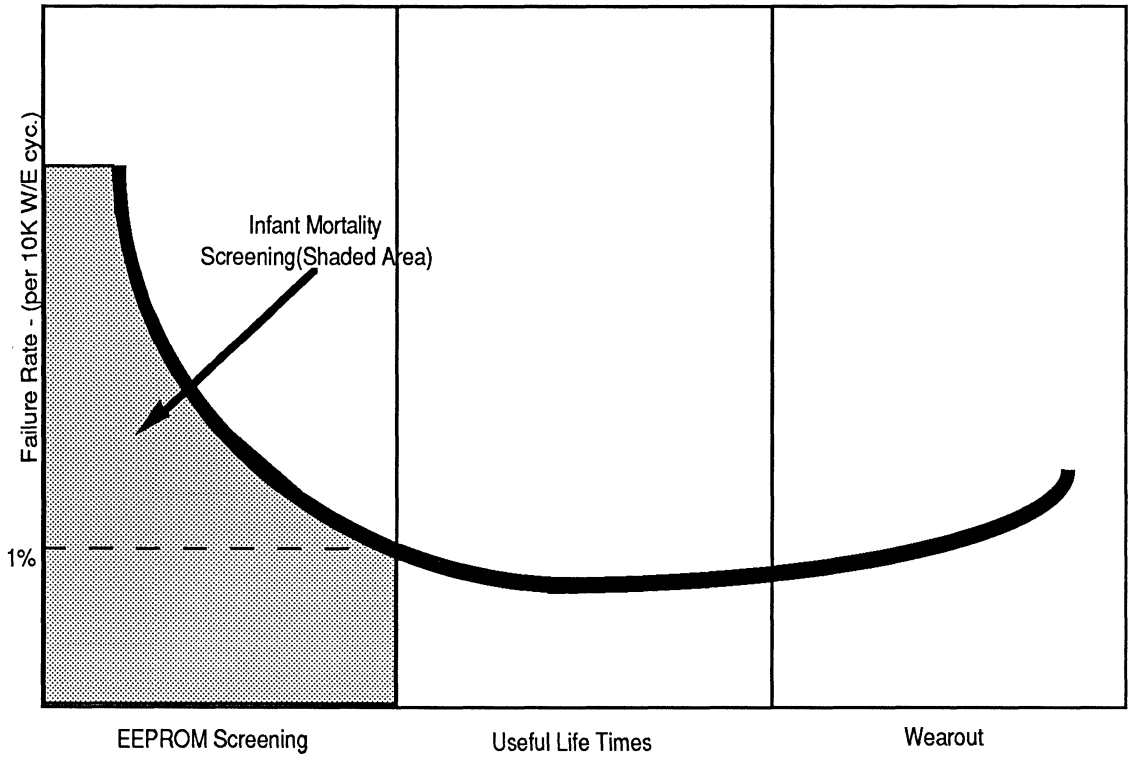
Customer feedback and problems are continually monitored and analyzed with failure analysis reports written and distributed to applicable engineering groups for immediate corrective action. Sometimes problems are related to the application, rather than the IC itself, and corrective measures can be suggested.

Customer service activities also include the collection and evaluation of quality-related feedback data from customers. It is Catalyst's intent to be continually aware of how we can improve the quality and reliability of all Catalyst products.

At Catalyst, we believe in satisfied customers.

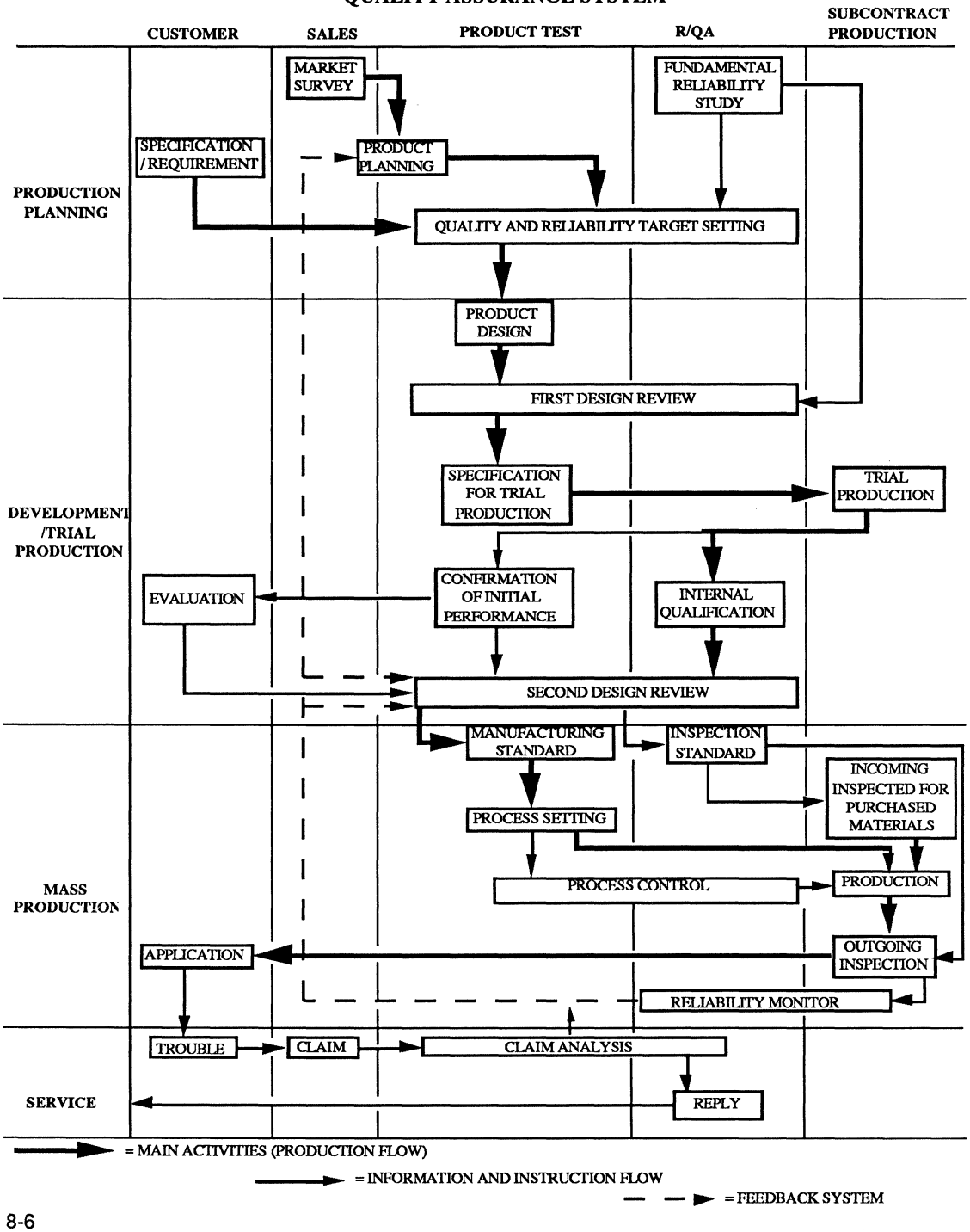
RELIABILITY LIFE CURVE

Like all system hardware -- mechanical, electrical or electronic, the reliability of EEPROM devices conforms to the well-known "bathtub" curve, which plots failure rate against time. As shown below, the three vital statistics associated with this curve are: *infant mortality, failure rate* and *useful life.*

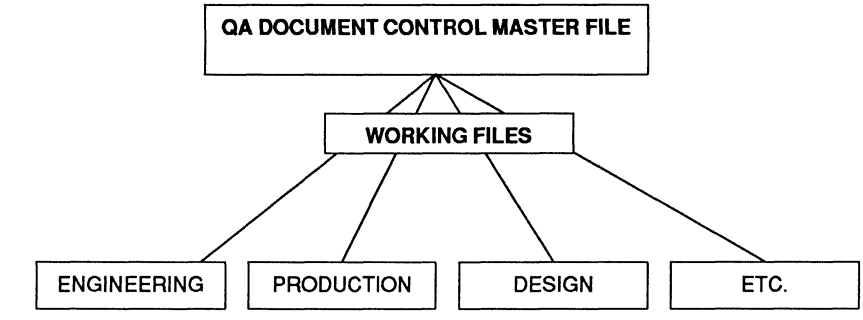


EEPROM WRITE/ERASE CYCLES

QUALITY ASSURANCE SYSTEM



CATALYST DOCUMENT CONTROL SYSTEM Fig. 1



- Specification written or data collected for engineering change of existing specification
- ECN number issued by document control.
- ECN circulated and approved by manufacturing, engineering, and R/QA managers.
- Approved ECN returned to document control.
- Document control revises master file and generates new documents to pertinent working files.

IN-PROCESS QC FLOW CHART Fig. 2A

WAFER FABRICATION (3 μm SI Gate CMOS)

FLOW	PROCESS	QC ITEM	SAMPLING METHOD
▽	STARTING MATERIAL		
○	P-WELL FORMATION	THICKNESS	1 WAFER/LOT
		RESISTIVITY	1 WAFER/LOT
○	ACTIVE AREA FORMATION	CRITICAL DIMENSION	2 WAFERS/ LOT
○	FIELD FORMATION	THICKNESS	1 WAFER/CHARGE
○	GATE FORMATION	THICKNESS	1 WAFER/CHARGE
		RESISTIVITY	1 WAFER/CHARGE
		CRITICAL DIMENSION	2 WAFERS/LOT
○	S/D FORMATION	THICKNESS	1 WAFER/10 LOTS
		RESISTIVITY	1 WAFER/ 10 LOTS
○	INTERLAYER FORMATION	THICKNESS	1 WAFER/ LOT
		P-CONCENTRATION	1 WAFER/ LOT
○	METAL FORMATION	THICKNESS	2 WAFERS/ 10 LOTS
○	FINAL PASSIVATION FORMATION	THICKNESS	2 WAFERS/ CHARGE
○	PARAMETER CHECK	DEVICE PARAMETER	3 WAFERS/ LOT
○	ELECTRICAL TEST	ELECTRICAL CHARACTERISTICS	100%

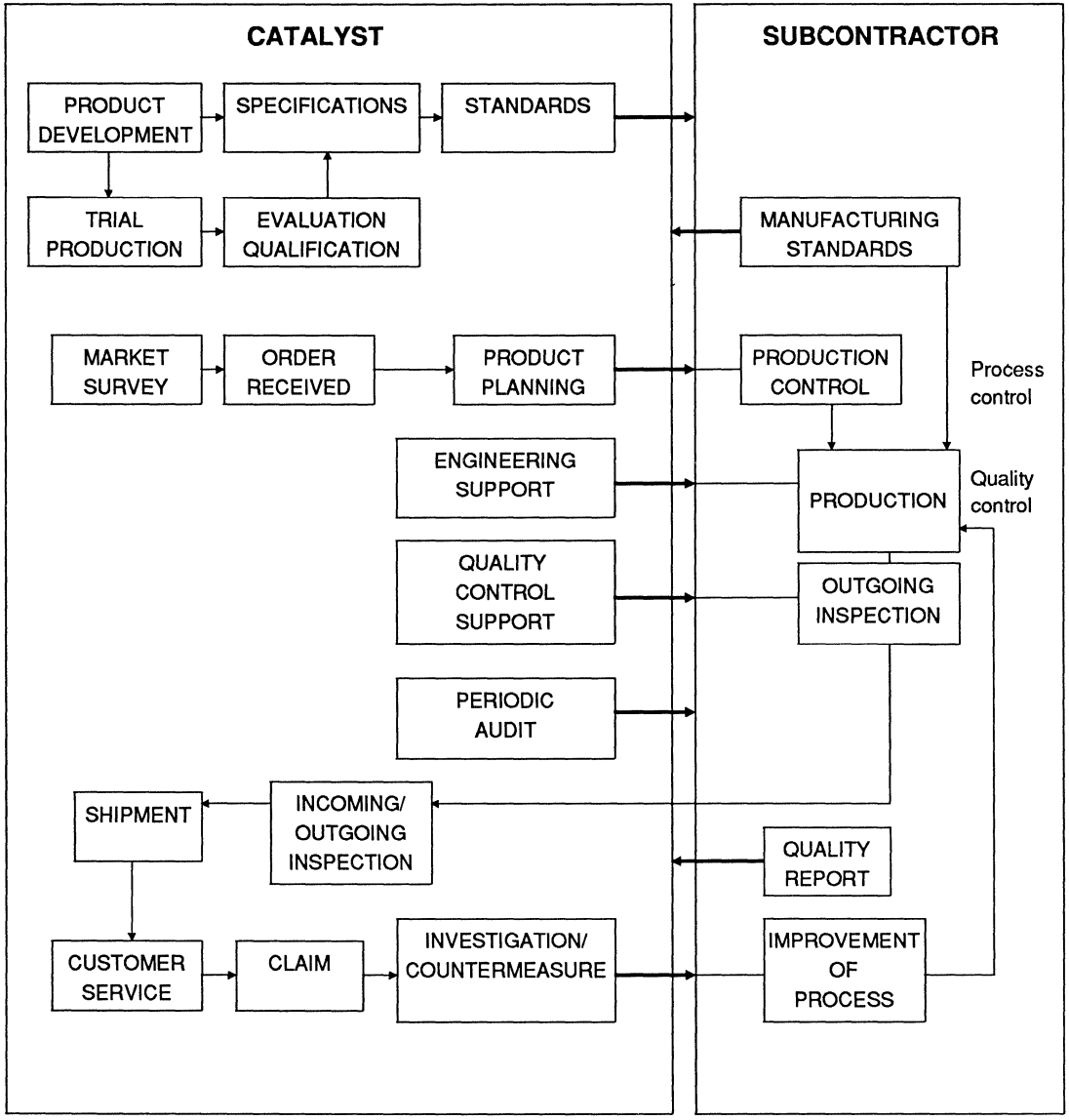
IN-PROCESS QC FLOW CHART Fig. 2B

ASSEMBLY & TESTING PROCESS (PLASTIC DIP)

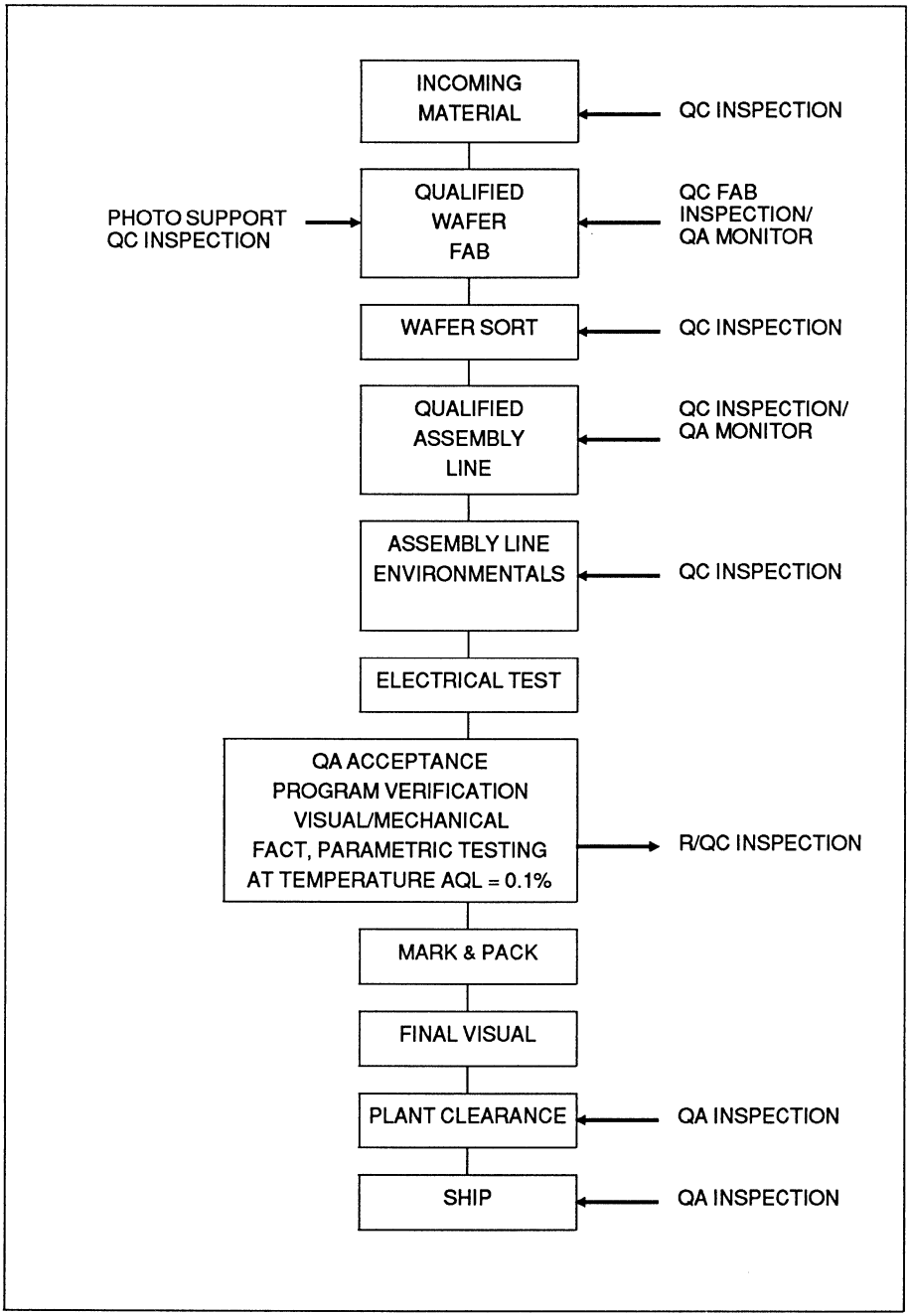
FLOW	PROCESS	QC ITEM	SAMPLING METHOD
○	SCRIBING		
○	CHIP VISUAL	VISUAL	100%
○	DIE BONDING	VISUAL	TWICE/SHIFT/MAC*
○	WIRE BONDING	BOND STRENGTH VISUAL	ONCE/SHIFT/MAC ONCE/SHIFT/MAC
○	VISUAL INSPECTION	VISUAL	100%
○	MOLDING		
○	VISUAL INSPECTION	VISUAL	100%
○	SOLDER PLATING	VISUAL	PER LOT
○	LEAD CUTTING/FORMING	VISUAL	PER LOT
○	MARKING	VISUAL	100%
○	ELECTRICAL TEST	ELECTRICAL CHARACTERISTICS	100%
◇	OUTGOING INSPECTION		
○	PACKING/SHIPPING		

* MAC means machine

SUBCONTRACTOR CONTROL SYSTEM Fig. 3



QA FLOWCHART Fig. 4



QUALITY CONTROL MONITORS - Partial List

WAFER FAB

- DI water bacteria and resistivity
- Airborne particles
- Temperature and humidity
- Oxide phosphorus content
- Metal step coverage
- Equipment calibration
- Oxide thickness
- Photolithographic critical dimensions
- Operator certification
- Process parameters measured (each lot)
- Examples: Vt measurements
  Sheet resistivity
  Oxide quality Jt., etc.

WAFER SORT

- Equipment calibration
- Temperature and humidity
- Operator certification
- Airborne particles
- Catalyst wafer sort correlation
- Group B testing on quick assembly plastic (each wafer lot)

INCOMING SORTED WAFER INSPECTION

- Visual inspection sample (LTPD = 10)
- Sort data verification
- Critical process parameters compared to purchase specification. (Catalyst has the right to accept or reject lot.)

QUALITY CONTROL MONITORS - continued

PLASTIC ASSEMBLY

- DI water bacteria and resistivity
- Temperture and humidity
- Static protected area
- Incoming materials (leadframe, gold wire, D/A and mold compound wafers)
- Visual inspection (1st, 2nd, 3rd, post mold, post mark)
- Die shear and die attach voids
- Die attach curing time and temperature
- Wire bond pull, bond cratering, ball shear
- Molding temperature
- Outgoing final visual 100%

FINAL TEST

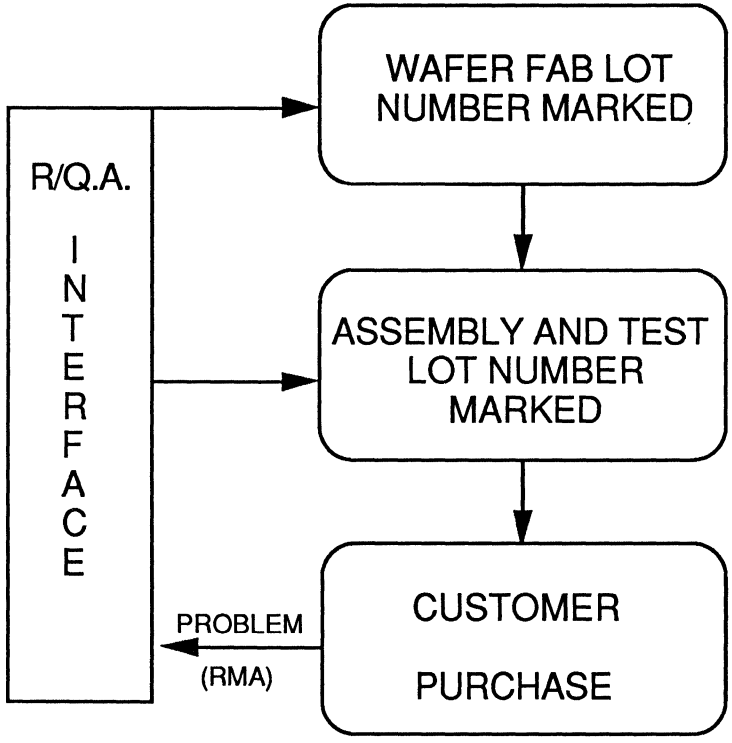
- Temperature and humidity
- Static protected area
- Operator certification
- Equipment calibration
- Catalyst test program correlation
- Effective 100% Reliability screen for all E^2PROM products

  Serial E^2PROM example: Minimum 2K W/E cycles all cells
  Bake, 150°C
  Vt check
- Outgoing Final Visual inspection 100%

ASSEMBLED DEVICES INSPECTION

- ESD protected area
- Equipment calibration
- Visual inspection
- QA electrical inspection at temperature
- Physical dimensions
- 100% documentation verification

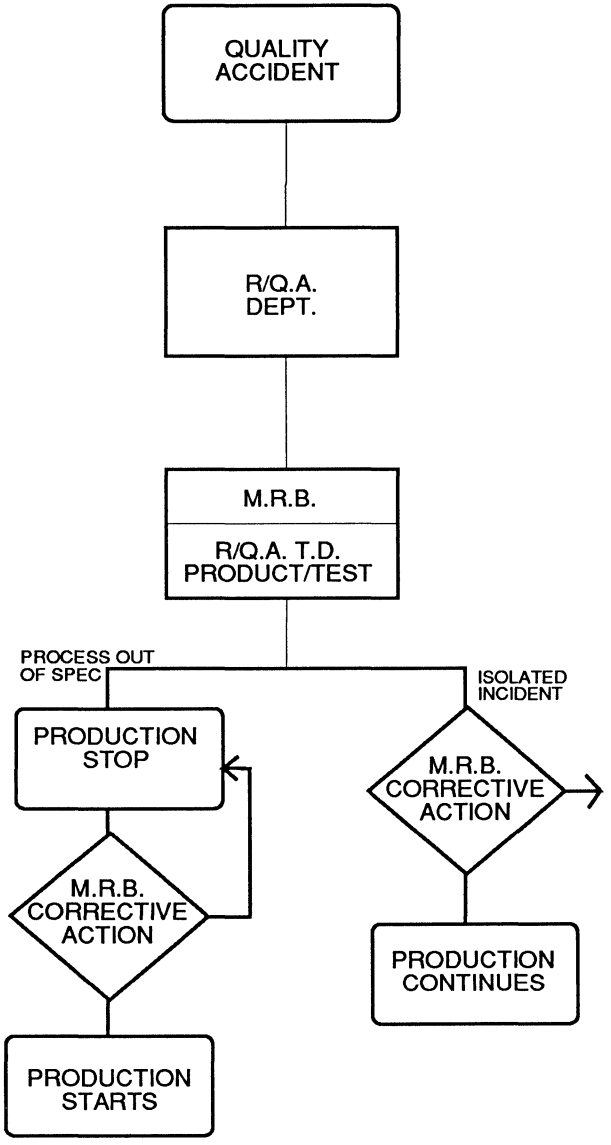
WAFER LOT TRACEABILITY



DOCUMENTATION

- FAB HISTORY, RAW MATERIAL LOT #s, INSPECTION REPORTS, ETC.
- ASSEMBLY AND TEST HISTORY, RAW MATERIAL LOT #'s, INSPECTION REPORTS, ETC.

ACCIDENT RESPONSE



KEY ACTION

- PROBLEM, ie FIELD FAILURE OR NON-CONFORMING MATERIAL
- INVESTIGATE AND DOCUMENT FAILURE ANALYSIS
- REVIEW ALL DATA, DETERMINE CORRECTIVE ACTIONS
- INFORM CUSTOMER OR VENDOR

RELIABILITY TEST DATA

Operating Life, 125°C — Reject/Sample Size

DEVICE	168 HRS	500 HRS	1000 HRS
59C11/93C46 35C102/35C202 35C104	0/1046 0/293 0/139	2/1046 0/293 0/139	0/1044 0/293 0/139

PRODUCT	DEVICE HRS	FAILURES	ACT. ENG.	60% CONF @55	CAUSE
59C11/93C46	1046000	2	0.7	38.1 FIT	FUNCTIONAL
35C102/35C202	293000	0	0.7	40.1 FIT	
35C104	139000	0	0.7	84.5 FIT	

Data Retention Post 10K 150°C Bake — Reject/Sample Size

DEVICE	168 HRS	500 HRS	1000 HRS
59C11/93C46 35C102/35C202 35C104	3/898 0/202 0/100	0/895 0/202 0/100	0/895 0/202 0/100

PRODUCT	DEVICE HRS	FAILURES	ACT. ENG.	60% CONF @55	CAUSE
59C11/93C46	898000	3	0.6	39.5 FIT	CHARGE LOSS
35C102/35C202	202000	0	0.6	38.5 FIT	
35C104	100000	0	0.6	77.8 FIT	

Endurance Cycle Bake — Reject/Sample Size

DEVICE	5K BAKE	10K BAKE	20K BAKE	50K BAKE	100K BAKE	FR(FAIL/10KCY)
59C11/93C46 35C102/35C202 35C104	0/442 0/202 0/100	0/442 0/202 0/100	0/442 0/202 0/100	0/442 0/202 0/100	2/442 CHGLOSS 0/202 1/100 CHGLOSS	.045%/10K W/E CY .000%/10K W/E CY .1%/10K W/E CY

Highly Accelerated Stress Test (HAST) Reject/Sample Size

DEVICE	24 HOURS	48 HOURS
59C11/93C46 35C102/35C202 35C104	2/290* 0/151 0/68	0/31 0/151 0/68

* Functional

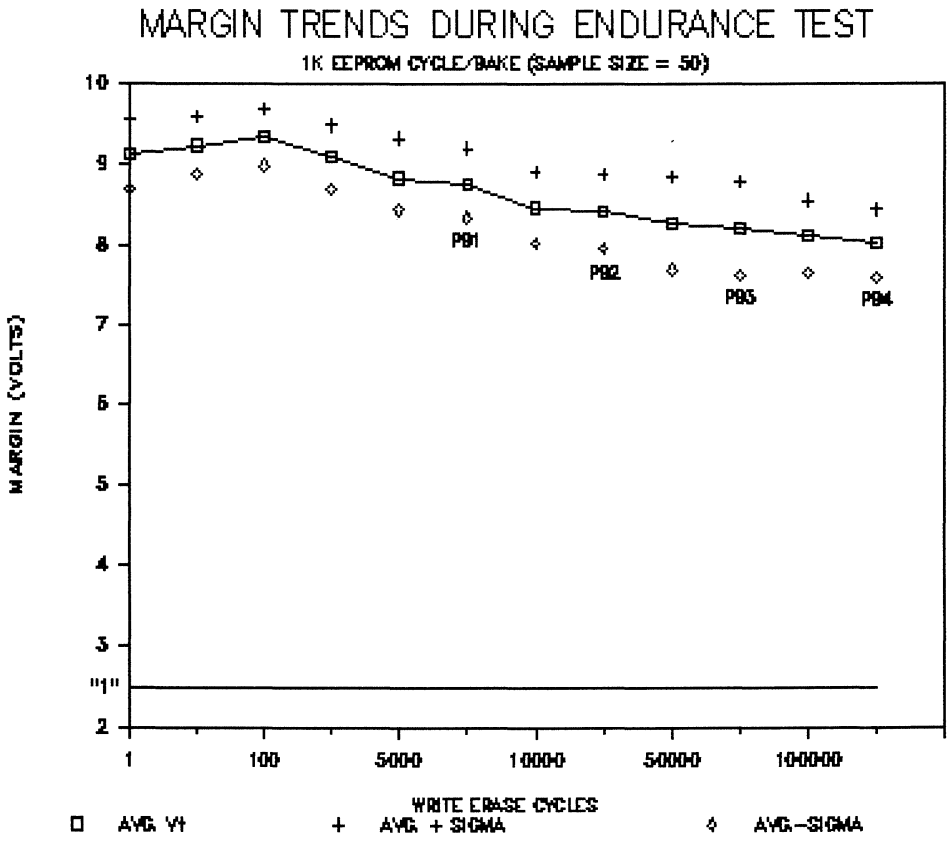
Pressure Pot (PCT), 121C, 15psi Reject/Sample Size

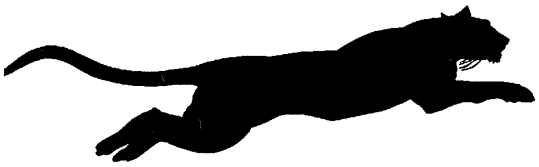
DEVICE	96 HOURS	168 HOURS	336 HOURS
59C11/93C46 35C102/35C202 35C104	0/386 1/170* 0/68	1/386* 0/169* 0/68	 0/99 0/68

*Pkg. Related

Temperature Cycles -65/150°C with 10 min. Soak Reject/Sample Size

DEVICE	150 CYC.	500 CYC.	1000 CYC.
59C11/93C46 35C102/35C202 35C104	0/226 0/169 0/68	0/226 0/169 0/68	0/226 0/169 0/68

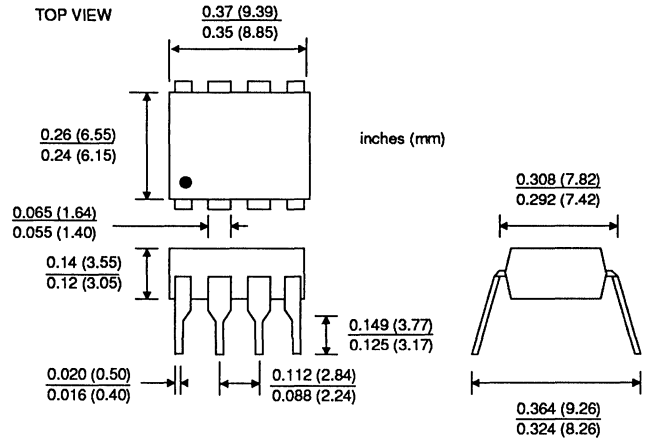

MARGIN TRENDS DURING ENDURANCE TEST
1K EEPROM CYCLE/BAKE (SAMPLE SIZE = 50)
MARGIN (VOLTS)
10
9
8
7
6
5
4
3
"1"
2
1
100
5000
10000
50000
100000
WRITE ERASE CYCLES
P91
P92
P93
P94
AVG. Vt
AVG. + SIGMA
AVG.-SIGMA



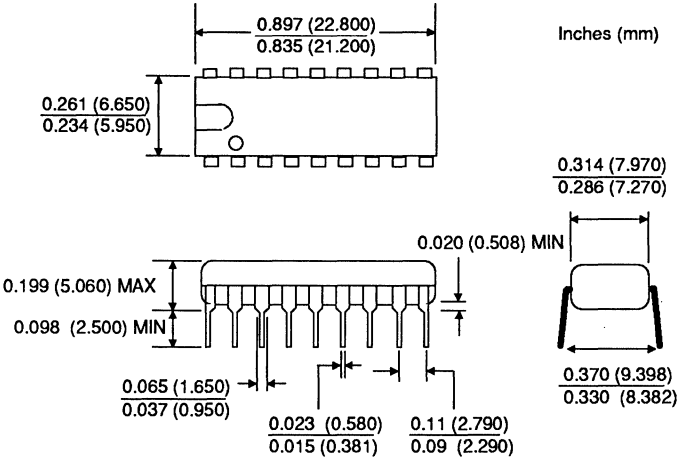
SECTION 9

PACKAGE INFORMATION

8 PIN PLASTIC DIP

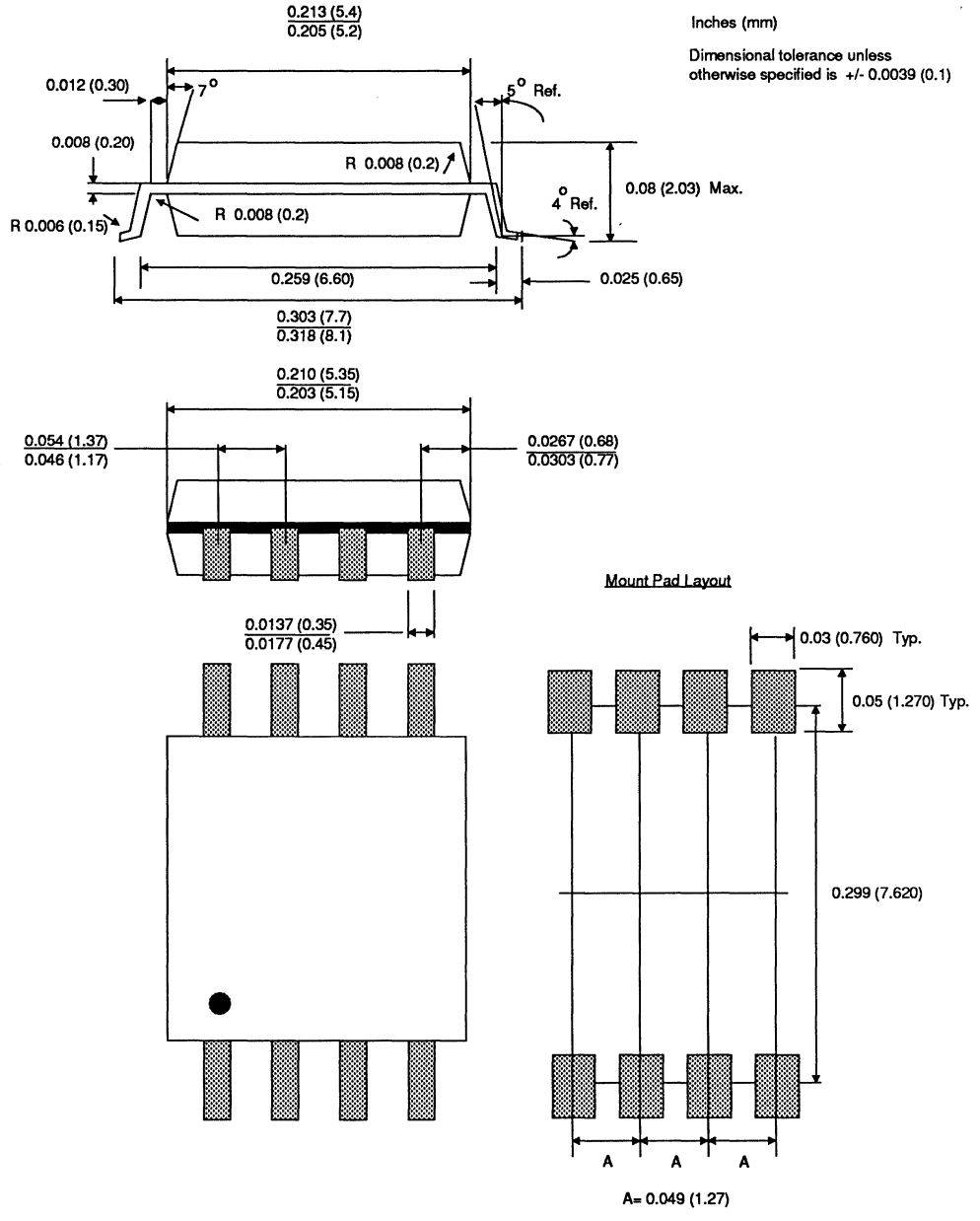


18 PIN PLASTIC DIP

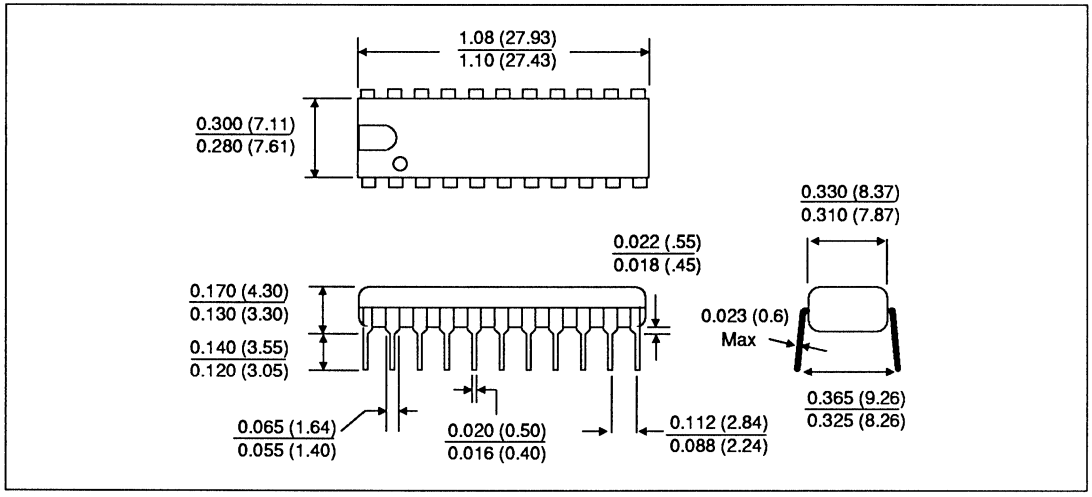


CATALYST SEMICONDUCTOR, INC.

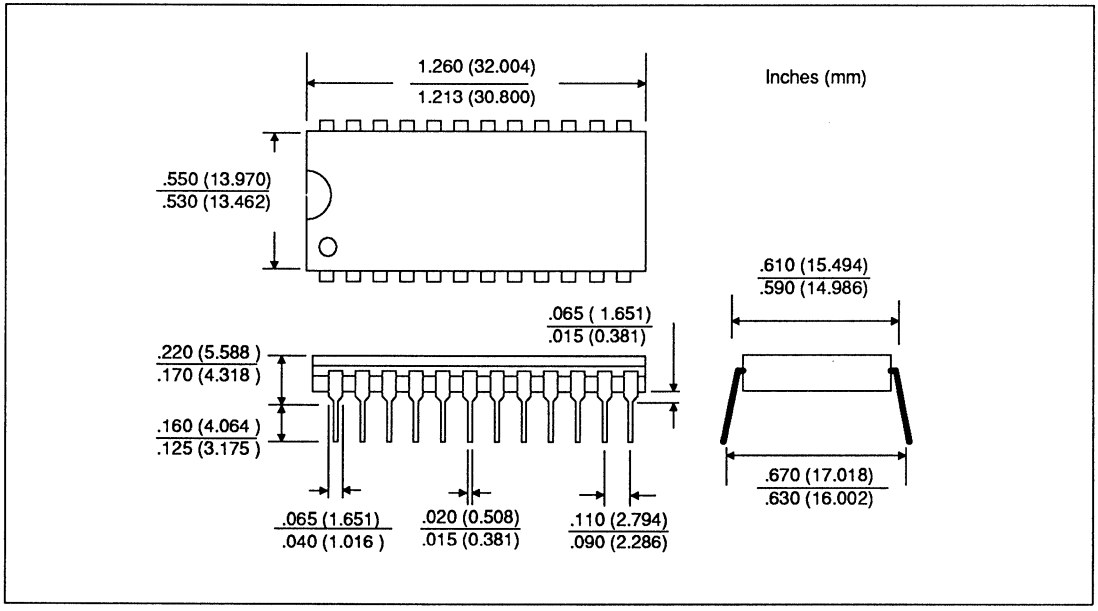
8 PIN S.O. DIP



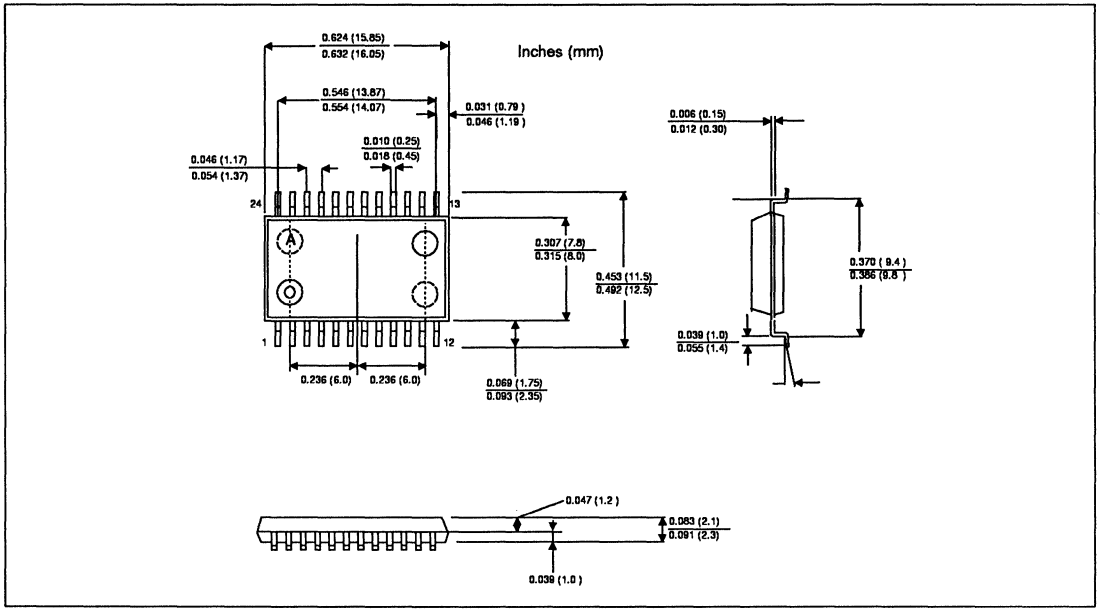
22 PIN PLASTIC DIP



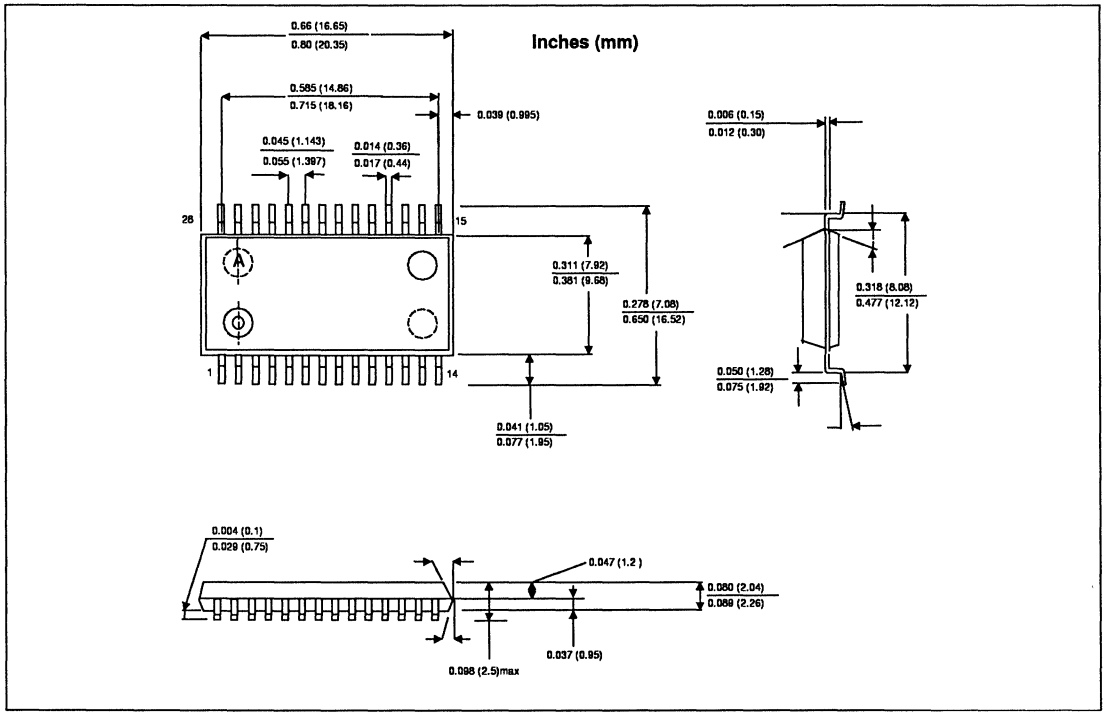
24 PIN PLASTIC DIP



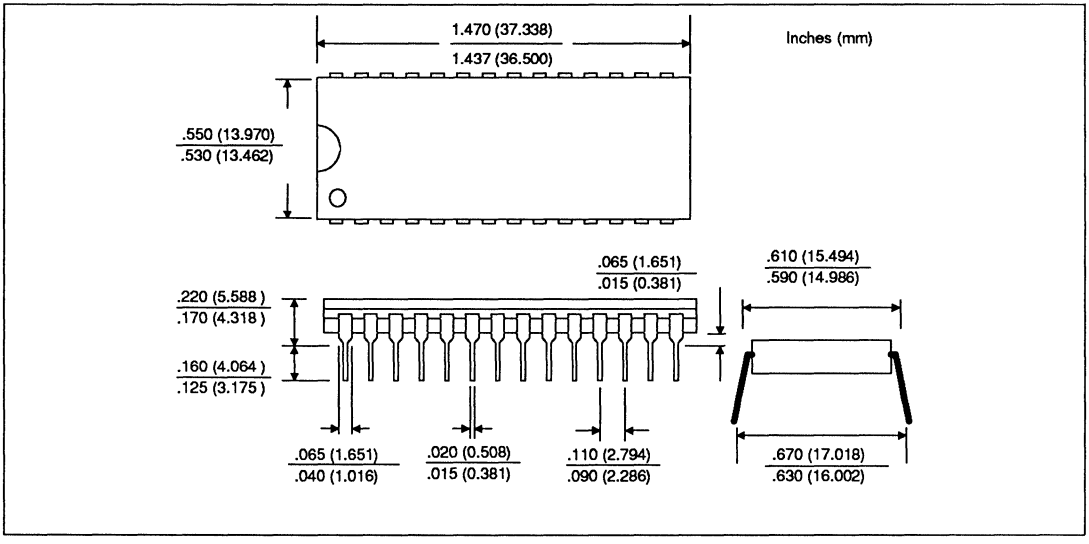
24 PIN SO



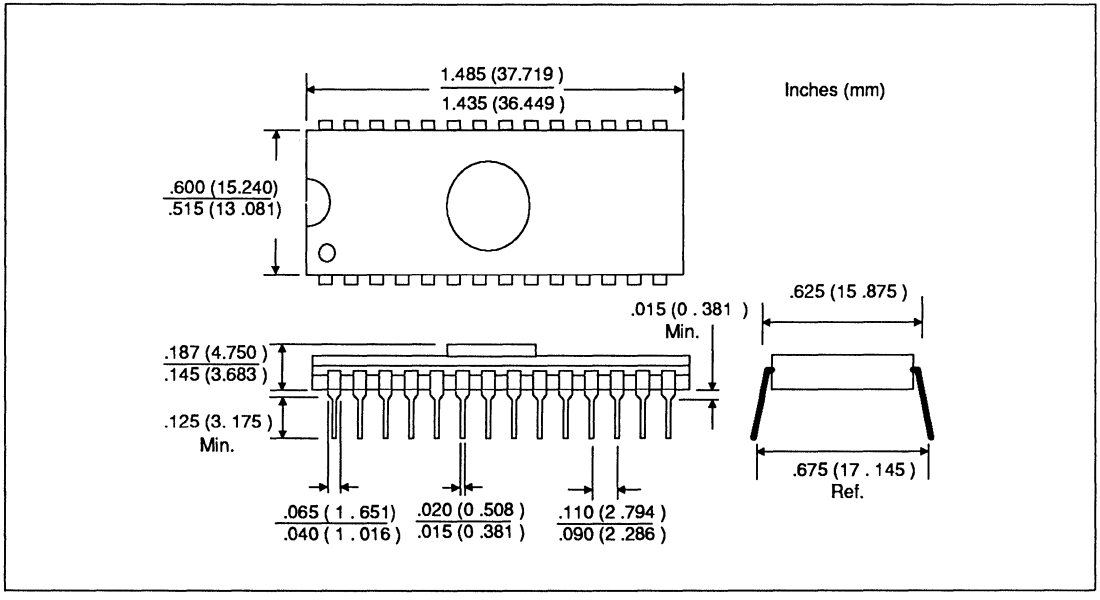
28 PIN SO



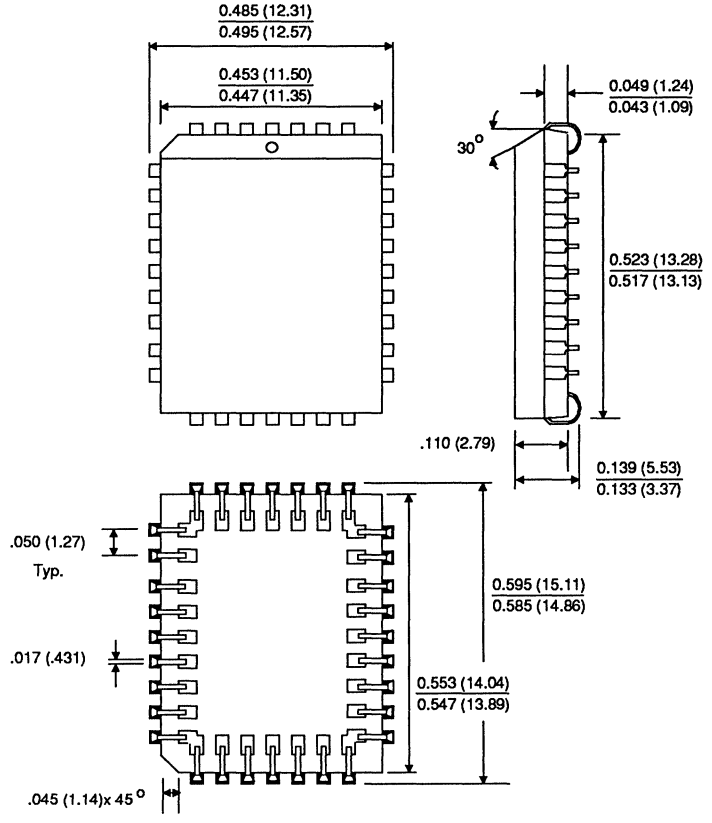
28 PIN PLASTIC DIP



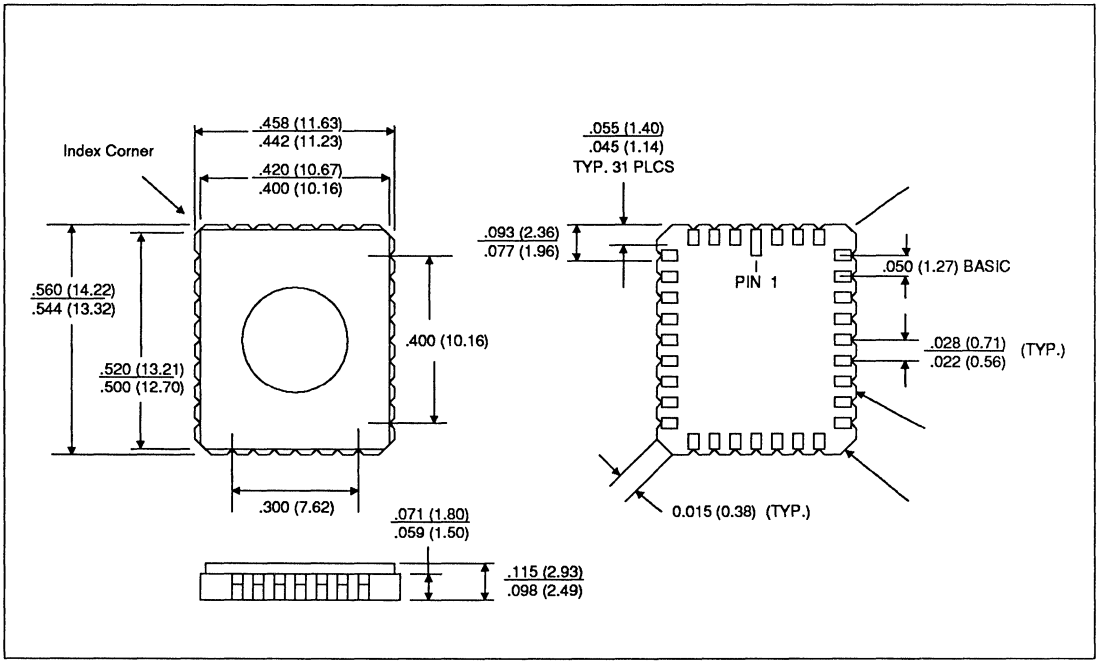
28 PIN CERDIP



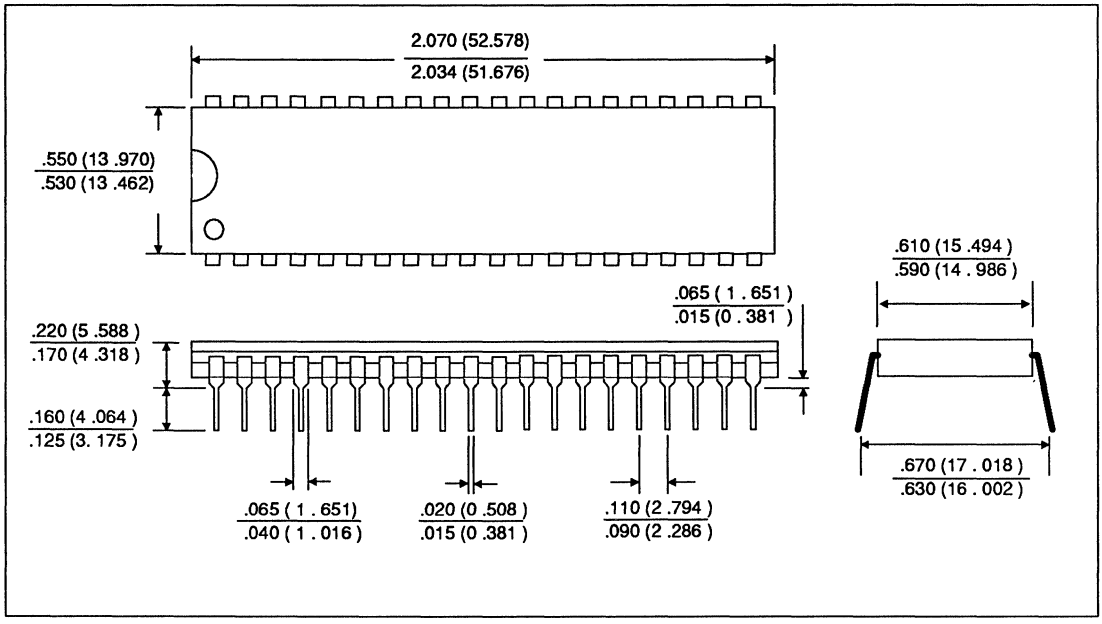
32 PIN PLCC


0.485 (12.31)
0.495 (12.57)
0.453 (11.50)
0.447 (11.35)
0.049 (1.24)
0.043 (1.09)
30°
0.523 (13.28)
0.517 (13.13)
.110 (2.79)
0.139 (5.53)
0.133 (3.37)
.050 (1.27)
Typ.
.017 (.431)
0.595 (15.11)
0.585 (14.86)
0.553 (14.04)
0.547 (13.89)
.045 (1.14)x 45°

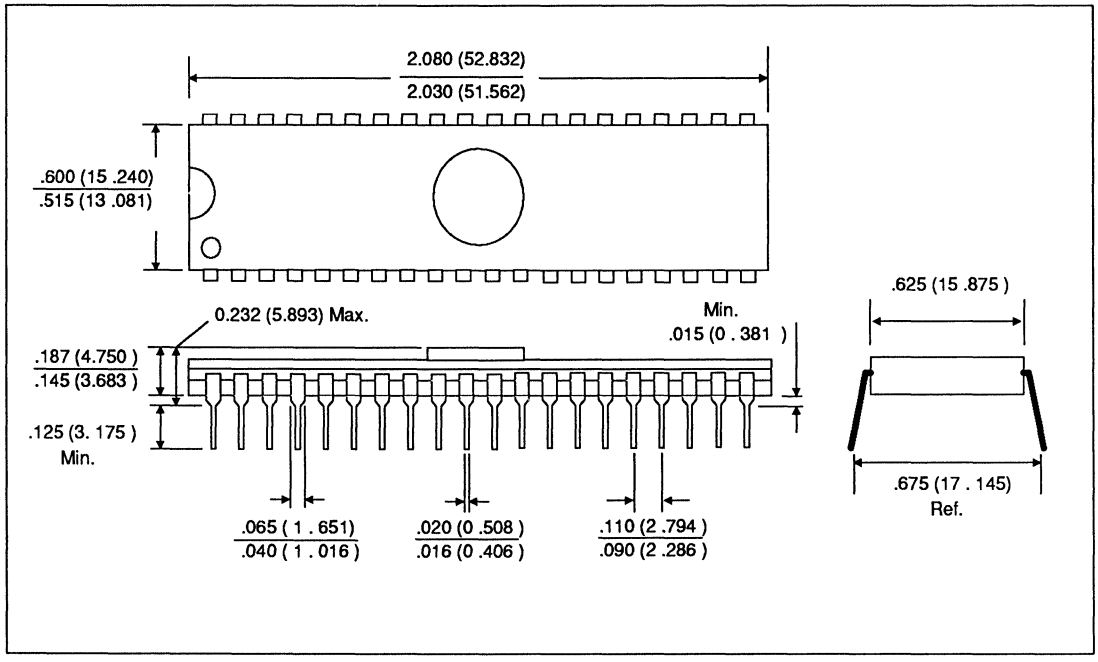
32 PIN WINDOWED CERAMIC LCC



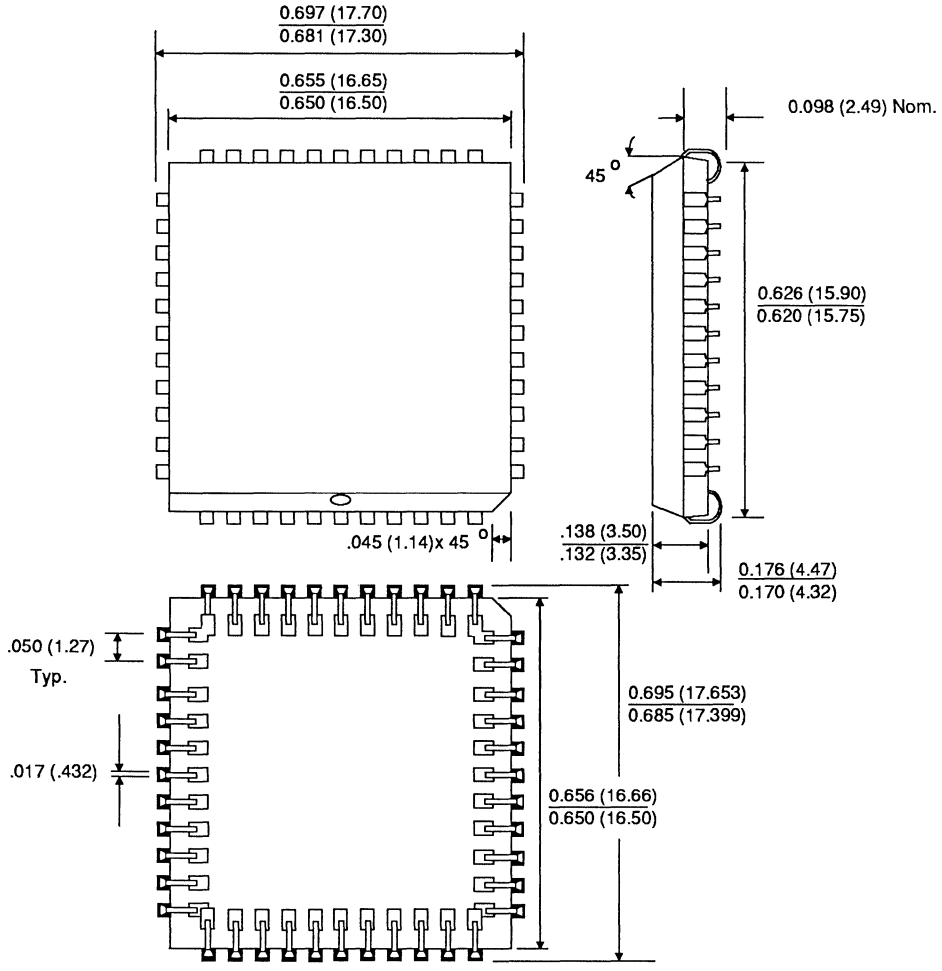
40 PIN PLASTIC DIP



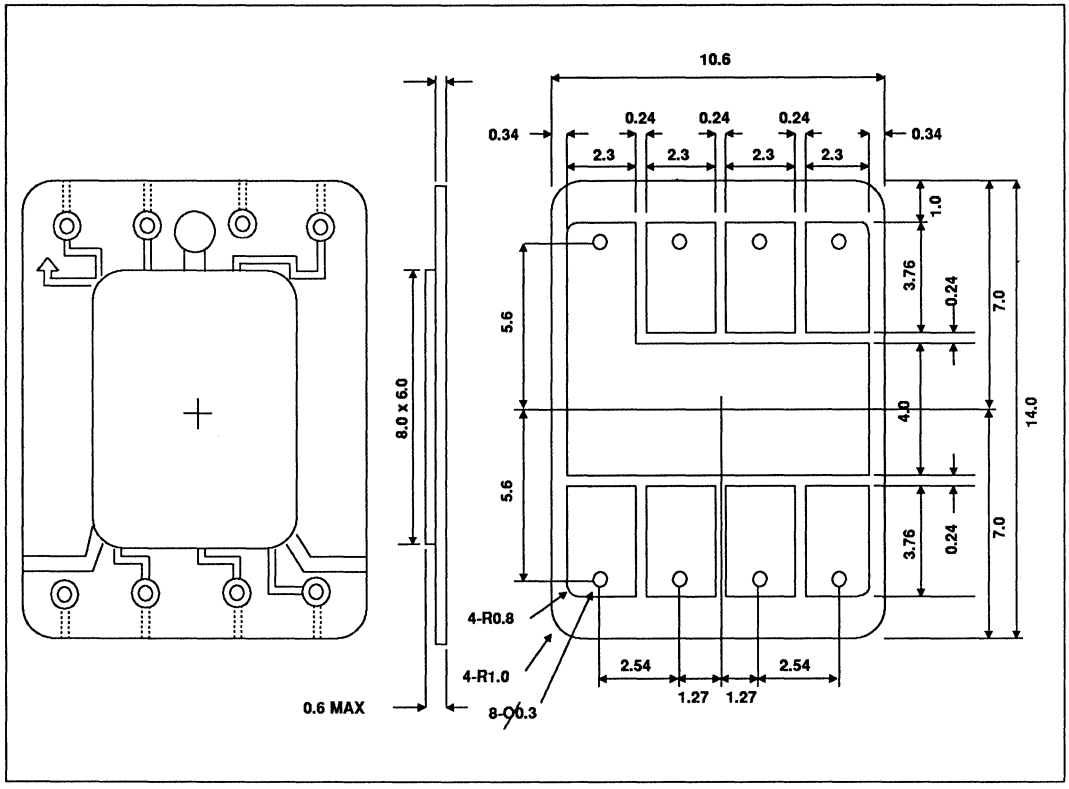
40 PIN CERDIP



44 PIN PLCC


0.697 (17.70)
0.681 (17.30)
0.655 (16.65)
0.650 (16.50)
0.098 (2.49) Nom.
45°
0.626 (15.90)
0.620 (15.75)
.045 (1.14)x 45°
.138 (3.50)
.132 (3.35)
0.176 (4.47)
0.170 (4.32)
.050 (1.27)
Typ.
.017 (.432)
0.695 (17.653)
0.685 (17.399)
0.656 (16.66)
0.650 (16.50)

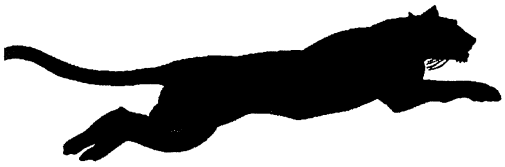
<CHIP ON BOARD>



DIE PRODUCTS

A number of CATALYST SEMICONDUCTOR's products are available for purchase in die form.

Please contact the factory or your local CATALYST SEMICONDUCTOR, INC. representative for additional information.

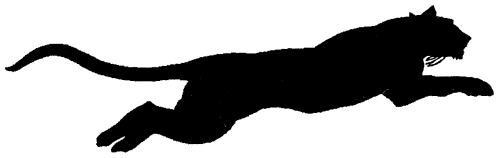


SECTION 10

CROSS REFERENCE GUIDE

CROSS REFERENCE GUIDE

CATALYST PART NUMBER AND DESCRIPTION	PART NUMBER	COMPATIBLE VENDOR	TECHNOLOGY	# PINS
CAT22C10 256 Bit (64x4) Nonvolatile CMOS Static RAM	**CAT22C10** NCR52210 X2210	 NCR XICOR	**CMOS** SNOS NMOS	**18** 18 18
CAT22C12 1024 Bit (256x4) Nonvolatile CMOS Static RAM	**CAT22C12** NCR52212 X2212	 NCR XICOR	**CMOS** SNOS NMOS	**18** 18 18
CAT24C44 256 Bit (16x16) Nonvolatile Serial CMOS Static RAM	**CAT24C44** X2444	 XICOR	**CMOS** NMOS	**8** 8

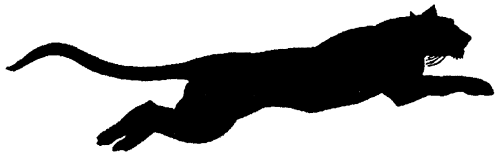


CROSS REFERENCE GUIDE

CATALYST PART NUMBER AND DESCRIPTION	PART NUMBER	COMPATIBLE VENDOR	TECHNOLOGY	# PINS
CAT27HC256	**CAT27HC256**		**CMOS**	**28**
256 Bit (32Kx8) EPROM	HN27C256HG	HITACHI	CMOS	28
	WS57C256	WSI	CMOS	28
	AT27HC256	ATMEL	CMOS	28
	AM27C256	AMD	CMOS	28
CAT27512	**CAT27512**		**NMOS**	**28**
16Kx8 EPROM V_{PP} = 12.5V	AM27512	AMD	NMOS	28
	MSM27512	OKI	NMOS	28
	M5M27512	MITSUBISHI	NMOS	28
	HN27512	HITACHI	NMOS	28
CAT27010	**CAT27010**			**32**
128Kx8 EPROM	AM27C010	AMD	CMOS	32
	27010	INTEL	HMOS	32
	NMC27C1023	NATIONAL	CMOS	32
	AT27C010	ATMEL	CMOS	32
	HN27C101G	HITACHI	CMOS	32
	PD27C1000A	NEC	CMOS	32
	MSM271000	OKI	CMOS	32
CAT2764A	**CAT2764A**		**NMOS**	**28**
8Kx8 EPROM V_{PP} = 12.5V	P2764A	INTEL	NMOS	28
	AM2764A	AMD	NMOS	28
	TMS27P64	TI	NMOS	28
	MSM2764	OKI	NMOS	28
	µPD2764	NEC	NMOS	28
	TMM2764	TOSHIBA	NMOS	28

CROSS REFERENCE GUIDE

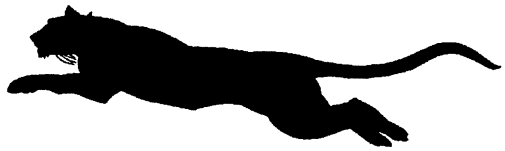
CATALYST PART NUMBER AND DESCRIPTION	PART NUMBER	COMPATIBLE VENDOR	TECHNOLOGY	# PINS
CAT27128A	**CAT27128A**		**NMOS**	**28**
16Kx8 EPROM				
V_{PP} = 12.5V	P27128A	INTEL	NMOS	28
	AM27128A	AMD	NMOS	28
	MSM27128	OKI	NMOS	28
	µPD2764	NEC	NMOS	28
CAT27C210	**CAT27C210**		**CMOS**	**40**
64Kx16				
1 Megabit EPROM	MSM27C1024	OKI	CMOS	40
	AM27C1024	AMD	CMOS	40
	27210	INTEL	HMOS	40
	M5M27102K	MITSUBISHI	MIXMOS	40
	NMC27C1024	NATIONAL	CMOS	40
	AT27HC1024	ATMEL	CMOS	40
	HN27C102AG	HITACHI	CMOS	40
	µPDC1024	NEC	CMOS	40
CAT27256	**CAT27256**		**NMOS**	**28**
32Kx8 EPROM				
V_{PP} = 12.5V	P27257	INTEL	NMOS	28
	AM27256	AMD	NMOS	28
	MSM27256	OKI	NMOS	28
	M5M27256	MITSUBISHI	NMOS	28
CAT28C16A	**CAT28C16A**		**CMOS**	**24**
2Kx8 CMOS				
E^2PROM	2816A	INTEL/SEEQ	NMOS	24
	X2816A	XICOR	NMOS	24
	28C16	ATMEL	CMOS	24
	XL2816A	EXEL	NMOS	24
	TS28C16A	THOMSON	CMOS	24
	KM2816A	SAMSUNG	NMOS	24
	NMC2816	NATIONAL	NMOS	24
	M2816	SGS	NMOS	24
	MSM2816A	OKI	NMOS	24
	R2816A	ROCKWELL	NMOS	24



CROSS REFERENCE GUIDE

CATALYST PART NUMBER AND DESCRIPTION	PART NUMBER	COMPATIBLE VENDOR	TECHNOLOGY	# PINS
CAT28C17A	**CAT28C17A**		**CMOS**	**28**
2Kx8 CMOS				
E^2PROM	2817A	INTEL/SEEQ	NMOS	28
	28C17	ATMEL	CMOS	28
	AM2817A	AMD	NMOS	28
	TS28C17A	THOMSON	CMOS	28
	KM2817A	SAMSUNG	NMOS	28
CAT28C64A	**CAT28C64A**		**CMOS**	**28**
8Kx8 CMOS				
E^2PROM	2864	INTEL	HMOS	28
	X2864A	XICOR	NMOS	28
	28C64A	ATMEL	CMOS	28
	2864A	SEEQ	NMOS	28
	AM2864A	AMD	NMOS	28
	XL2864A	EXEL	NMOS	28
	MSM286A	OKI	NMOS	28
	HN58064	HITACHI	NMOS	28
	M5M28C64AP	MITSUBISHI	NMOS	28
	KM2864A	SAMSUNG	NMOS	28
CAT28C65A	**CAT28C65A**		**CMOS**	**28**
8Kx8 CMOS				
E^2PROM	2864	ATMEL	CMOS	28
	2865A	SEEQ	CMOS	28
	KM2864A	SAMSUNG	NMOS	28

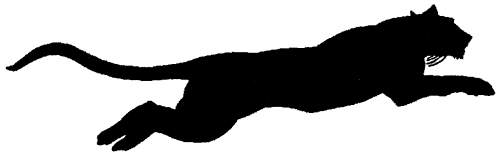
CROSS REFERENCE GUIDE



CATALYST PART NUMBER AND DESCRIPTION	PART NUMBER	COMPATIBLE VENDOR	TECHNOLOGY	# PINS
CAT35C102 (1)	**CAT35C102**		**CMOS**	**8**
2K Bit Serial				
E^2PROM	ER5912	GI (1)	SNOS	8
CAT35C202 (1)	**CAT35C202**		**CMOS**	**8**
2K Bit Serial				
E^2PROM	ER5912	GI (1)	SNOS	8
CAT59C11A	**CAT59C11A**		**CMOS**	**8**
1K Bit Serial				
E^2PROM	ER5911	GI	SNOS	8
	MSM16911	OKI (2)	CMOS	8
	TS59C11	THOMSON	CMOS	8
CAT93C46 (2)	**CAT93C46**		**CMOS**	**8**
1K Bit Serial				
E^2PROM	NMC9346/COP495	NATIONAL	NMOS	8
	93C46	ICT	CMOS	8
	HY93C46	HYUNDAI	CMOS	8
	MSM16811	OKI (2)	CMOS	8
	TS93C46	THOMSON (2)	CMOS	8
	SC22011	SIERRA	CMOS	8
	NCR59308	NCR	SNOS	8

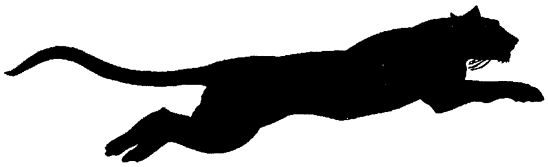
(1) User selectable organization: 64x16 or 128x8.

(2) User selectable organization: 128x16 or 256x8.



CROSS REFERENCE GUIDE

CATALYST PART NUMBER AND DESCRIPTION	PART NUMBER	COMPATIBLE VENDOR	TECHNOLOGY	# PINS
CAT93C46A	**CAT93C46A**		**CMOS**	**8**
1K Bit Serial				
E^2PROM	9346	NATIONAL	NMOS	8
	HY93C46	HYUNDAI	CMOS	8
	93C46	ICT	CMOS	8
	MSM16811RS	OKI	CMOS	8
CAT71C256	**CAT71C256**		**CMOS**	**28**
32Kx8 CMOS				
Static RAM	MSM51257RS/RJ	OKI	CMOS	28
	HM62256	HITACHI	CMOS	28
	MB84256	FUJITSU	CMOS	28
	TC53257	TOSHIBA	CMOS	28
	M5M5256	MITSUBISHI	MIXMOS	28
CAT71C256L	**CAT71C256L**		**CMOS**	**28**
32Kx8 CMOS				
Static RAM	MSM51257LRS/JS	OKI	CMOS	28
	HM61256	HITACHI	CMOS	28
	MB84256	FUJITSU	CMOS	28
	TC53257	TOSHIBA	CMOS	28
	M5M5256	MITSUBISHI	MIXMOS	28
	HY63C256/L	HYUNDAI	CMOS	28



SECTION 11

ARTICLE REPRINTS

SECURE ACCESS SERIAL E^2PROMS	Electronic Design, May 26, 1988
THE NEW FACES OF NONVOLATILE MEMORY	Electronics, July 9, 1987
SMART CARDS	Electronics, December 18, 1986

MAY 26, 1988

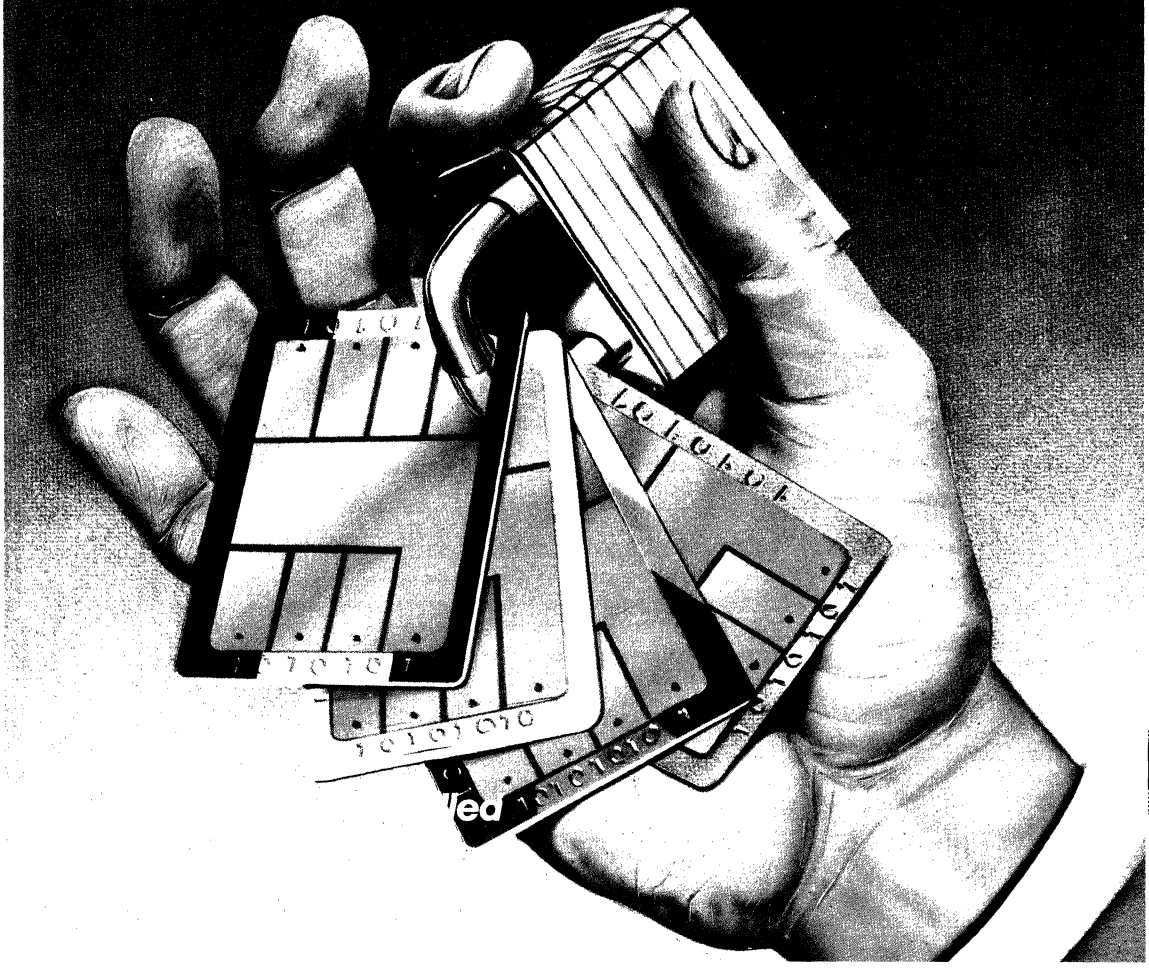
ELECTRONIC® DESIGN

A VNU BUSINESS PUBLICATION

DESIGN INNOVATION: Integrated SCSI controller transfers data at 5 Mbytes/s

ELECTRONIC DESIGN REPORT: Standardization efforts push networks toward OSI model

DESIGN APPLICATIONS: Using a digital signal processor for audio equalization



Protect your EEPROM data and gain more flexibility

Going beyond safeguarding data, intelligent EEPROMs deliver software-controllable features for a lock on security-conscious tasks.

DAVE BURSKY

Keeping data secure when it's stored in memory chips is almost impossible, especially if that data must be altered occasionally. By incorporating intelligence and security features onto an electrically erasable programmable-memory IC, Catalyst Semiconductor's intelligent EEPROM improves on previous EEPROMs and other memories that must hold critical data. Storing 4096 bits, the CAT35C704 in its special protected mode requires the entry of an access code word that can range from 8 to 64 bits (in 8-bit increments) before the data can be accessed the first time.

Where previous solutions often required two chips—an EEPROM for data storage and a microcontroller for intelligence—the 35C704 intelligent EEPROM does both tasks with one chip. It merges most functions expected of the microcontroller onto the memory chip, paring system cost and improving reliability.

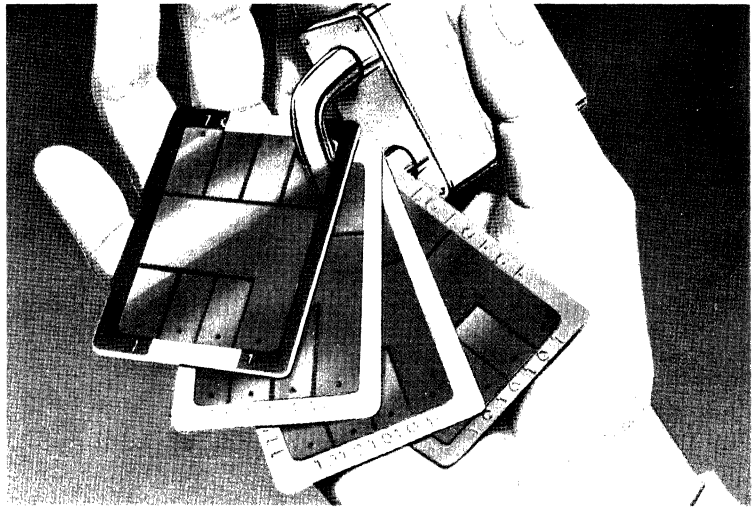
These memories suit the emerging "smart card" market, which requires nonvolatile but alterable storage, and is an ideal class of target applications, explains B. K. Marya, company president. The EEPROMs could just as well go to work in debit cards, telephone access-charge cards, security locks and access control cards, medical history cards, and even army dog tags. Industrial applications include product tracking, operating-system software protection, warranty and repair history tracking, and so forth.

The first version of the CMOS chip requires a 5-V supply, about 3 mA for operation, and roughly 100 μA during standby. By the end of the year, a version powered by just 3 V will be ready for sampling. Like most other CMOS EEPROMs, Catalyst's intelligent EEPROM makes possible 10,000 erase-write cycles and is guaranteed to retain data for 10 years.

According to Marya, the intelligent memory actually has many other features that give it even wider system appeal *(Fig. 1)*. An on-chip control processor responds to a set of 19 commands, one of which, ORG (organization), allows the designer to configure the chip to appear as either a 512 by 8 or 256 by 16 memory array. The chip is the first member of a family that will eventually offer capacities stretching from 256 bits to 16 kbits.

Under software control, the architect or programmer can determine how much memory needs protection. When the chip's write memory pointer (WMPR) instruction executes, a pointer value can be set to split the memory array into two blocks. Addresses above the pointer value are read only; addresses below and including the pointer require the security code to be accessed. Consequently, data held in the memory can be separated into two parts: Users without security clearance can access one section, while only those with "need to know" can access the other.

Because the chip was designed with low-cost applications in mind,



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it has only eight connections to the outside world. Also, the chip can be housed in inexpensive eight-pin DIPs or work with chip-on-board direct-mounting assembly schemes. Marya explains that by using so few pins, data and addresses are moved serially over the Data In and Data Out lines synchronously with the Serial Clock input. That clock input accepts frequencies ranging from dc to 5 MHz to move data on and off the chip. Also, when more intelligence is needed for the application, the I/O lines can readily connect to Intel 8051 or National COPS family microcontroller serial ports *(Fig. 2)*. To deal with various system timing situations, the EEPROM can also execute a No Operation (NOP) instruction, which essentially tells the chip to stay idle and not to execute any operations.

The simple serial port employs an 8-bit data packet—all instructions are 8 bits wide, with the first bit being the start bit and the following 7 bits representing the operation code. Data words are one or two bytes, depending on the memory organization, and words are transmitted with the most-significant bit first. With some minor differences, the serial mode is also compatible with the company's CAT93C46 serial EEPROM.

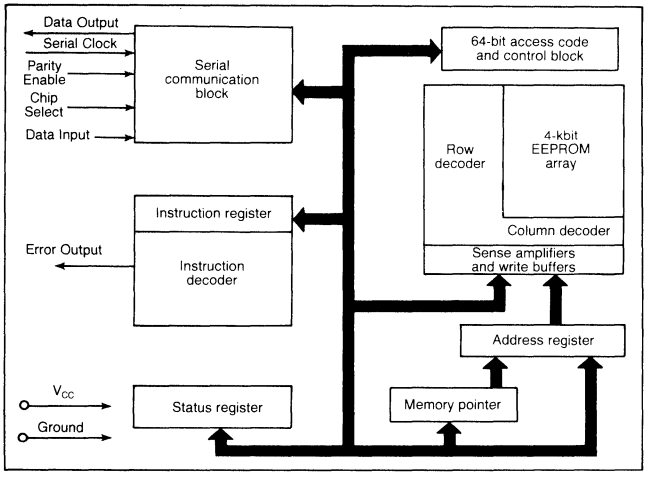
A metal-mask option converts the simple serial port into a universal asynchronous receiver-transmitter (UART) that makes possible data transfers up to 9600 baud. External oscillator frequencies of 3.579 or 4.925 MHz can be used. One or the other clock frequency must be selected before metal deposition. The UART format consists of 1 start bit, 8 data bits, 1 parity bit, and 1 stop bit. That parity bit can be enabled or disabled by setting the state of the Parity Enable (PE) pin—high for even parity, low for no or odd parity. When configured with the UART, the chip becomes the CAT35C804.

CIRCUIT STATUS

An 8-bit status register on the intelligent memory lets systems interrogate the chip and determine the circuit's status. The first three bits are preconfigured with a "101" pattern, which lets users quickly determine if the chip is listening or has an error condition. The next three bits indicate the status of the parity error (of the previous instruction), instruction error (for the previous instruction), or whether the chip is ready or busy.

The last two bits are reserved for future use. At any point the contents of the register can be read by the host system—the host simply loads the Read Status Register (RSR) command into the memory chip. The chip's Error (ERR) output pin goes high if an invalid operation code or a parity error (if enabled) is detected. When an error condition occurs, the chip will stop receiving or transmitting data until the Chip Select (CS) pin is toggled low to high. The CS pin, when held low, puts the serial port into a reset state and thus terminates all communications. Unlike the company's 93C46 serial EEPROM, the CS line need not be pulled low to initiate a programming cycle.

When received from the factory, the 35C704/804 intelligent EEPROMs are in their unprotected mode. By loading various instructions and data values, the memory organization, the length of the access code (1 to 8 bytes), the code itself, and the pointer value can be set. Data words can also be written into the main storage area. The flexible security scheme permits up to 1.84

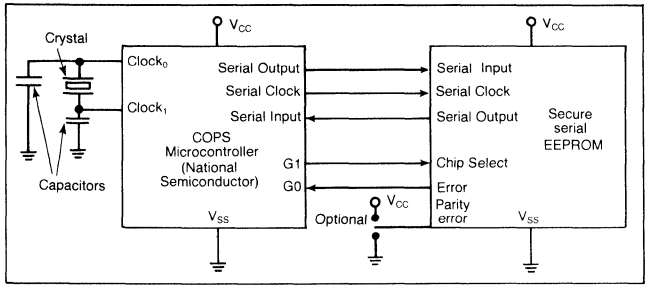


1. Besides the 4 kbits of EEPROM, the CAT35C704 intelligent memory from Catalyst Semiconductor packs a processor that manages the chip's security aspects and a serial communications port that can either be a simple serial interface or a more standard UART.

PRICE AND AVAILABILITY

With various packaging options, the CAT35C704 will be available in sample quantities in the middle of the third quarter. Initial sample prices have been set only for the eight-pin mini-DIP version, which costs about $16 in quantities of 100. The UART version (CAT35C804) will sell for less than $18. Production quantities will be ready late in the fourth quarter.

Catalyst Semiconductor Inc., 2231 Calle De Luna, Santa Clara, CA 95054; B.K. Marya, (408) 748-7700.



2. The simple serial port on the intelligent EEPROM can tie directly to microcontrollers like National Semiconductor's COPS series chips.

by 10^{19} access codes of 8 bytes each. Such a large number of codes would require 52 million years to break if the chip operates at its maximum speed of 5 MHz, Marya estimates.

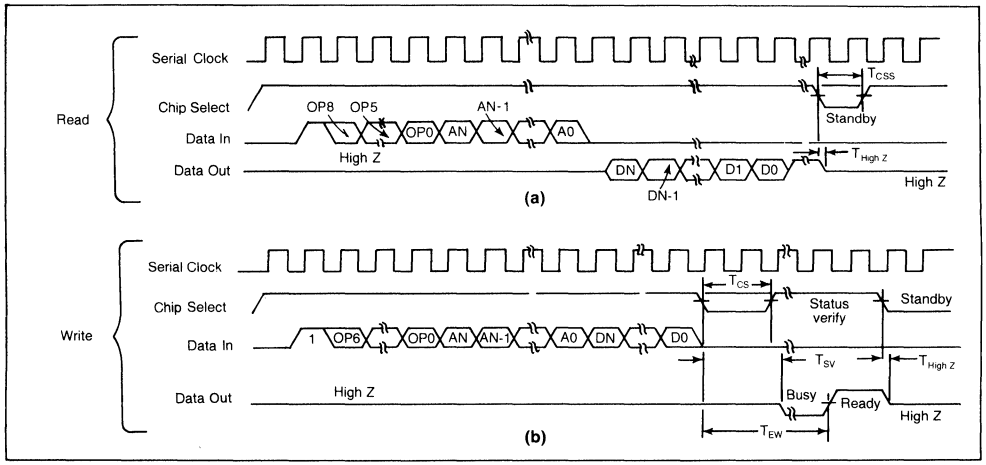
POINTER OFFERS SOME PROTECTION

When in the unprotected mode—access registers contain the hexadecimal value FFFFFFFF, and code length is set to hexadecimal 0000—any part of the EEPROM array can be read from or written to without an access code while the address pointer is at its base address (hexadecimal 00). Once the address pointer is modified through the WMPR command, any EEPROM address below the pointer is protected from any write or erase operation. This gives some degree of data protection. By changing the pointer address, the region can be "unprotected." If the host system must verify the pointer address, the Read Memory Pointer (RMPR) instruction causes the 35C704 to place the pointer address on the Serial Output line so the host can read it.

Because the circuit employs all serial transfers, read access time for a data word can be calculated from the number of bits that must be shifted in and out when the protected mode is disabled. If the chip is organized as a 512 by 8 bit memory, a 16-bit address must be shifted in (only 9 bits used, though, for now), and an 8-bit data word must be shifted out—a total of 24 clock cycles are required. With a 5-MHz maximum clock, 24 cycles translate to 4.8 μs.

A similar amount of time would be required if the chip were organized as 256 by 16—an 8-bit address is shifted in and a 16-bit data word is shifted out. Overhead operations for either configuration, such as loading the read instruction, add another eight cycles (1.6 μs) or more to the read request *(Fig. 3a)*. To read multiple data words from the memory and minimize the overhead of having to repeat the Read instruction, the Read Sequential (RSEC) command allows users to specify a starting location and then continually shift out data. This command can be terminated by bringing the Chip Select line low.

Writing data into the memory resembles the read operation—after the write instruction is loaded, the 1- or 2-byte address is loaded, followed by the 2- or 1-byte data word. After all the bytes are shifted in, though, the chip goes into a self-timed programming sequence *(Fig. 3b)*. First, the contents of the addressed location are erased, and then the new data is stored in the lo-



3. Signal timing for a read operation (a) and for a write operation (b) begin the same way. But the write operation first erases the current contents of the location and adds a self-timed programming cycle at the end to store the data in the nonvolatile cells.

cation. The entire operation takes 10 to 20 ms.

The Serial Data Out pin can be programmed to act as a status indicator pin by having the chip execute the Enable Busy (ENBSY) instruction. The pin remains low as long as the chip is in the self-timed programming mode and goes high as soon as the programming finishes. A complementary instruction, Disable Busy (DISBSY), disables the status indication feature on the Data Output line.

WIPE THE SLATE CLEAN

Selective erasing of words can take place with the Erase, and with the Erase All (ERAL) commands, users can blank the chip's contents in the same 5 to 10 ms self-timed cycle time. To prevent accidental erasure, the command must be issued twice before the chip will perform the instruction. A Write All (WRAL) command does just the opposite, allowing users to write a specified data word into all locations simultaneously. As with ERAL, the instruction must be sent twice for it to execute.

The security mode can be activated by loading the 4-bit Modify Access Code (MACC) command and following it with a 4-bit value to show how many bytes the access code will be (from 1 to 8 bytes). Following the length of the byte string are three equal-length byte strings, each containing the number of bytes specified by the 4-bit access code length. The first of those three strings is the old access code, the second the new access code, and the third, a repeat of the new access code for verification. Once activated, the memory protection is under software control.

Unless the Enable Access (ENAC) instruction followed by the same access code is sent to the chip, the memory array's protected portion (the addresses below the one and including the one that the address pointer register points to) can't be accessed. And memory contents at addresses above the pointer value can only be read but not altered. Access can also be denied by having the 35C704 execute its Disable Access (DISAC) instruction. Then, only the ENAC instruction and access code would again allow someone to access the chip's protected part.

A two-tier protection scheme prevents inadvertent writing and erasure of the memory contents. To write to the array, an Erase/Write Enable (EWEN) command must be issued. Once issued, the chip permits write operations to take place in the section of the memory array with addresses above the value held in the address pointer register. Addresses below the pointer value remain protected. The chip can also be taken out of the primed condition (the EWEN command received) through software by sending it an Erase/Write Disable (EWDS) command.

A software override of the protected area is possible, though, by the host system issuing the Override Memory Pointer (OVMPR) instruction. With that command, one instruction can override the protection and enable erase or write operations on the previously protected portion of the memory.

To safeguard data should power fail, or as part of the standard power-down operation, the on-chip data protection circuits inhibit all operating modes when the voltage drops below a preset value. The chip also internally executes an EWDS instruction to disable the erase-write mode. At power up, all modes of operation are disabled. An EWEN instruction and access code must be issued before the system tries to program the memory.□

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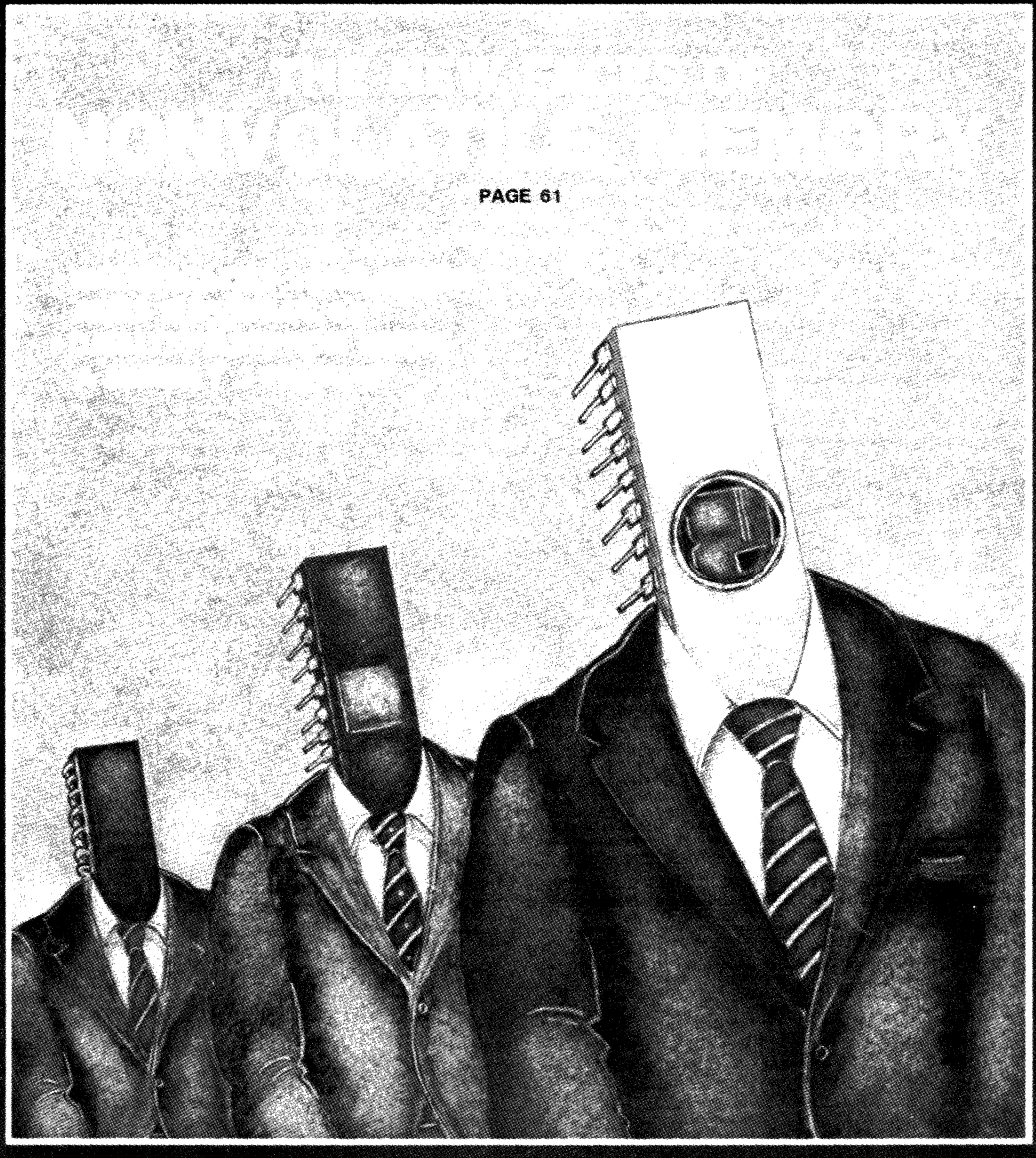


INSIDE TECHNOLOGY

THE CHANGING FACE OF NONVOLATILE MEMORIES

Faster, denser EPROMs and EEPROMs are finding new uses, displacing big ROMs and fast PROMs, for example; big chunks of them can also be added to ASICs

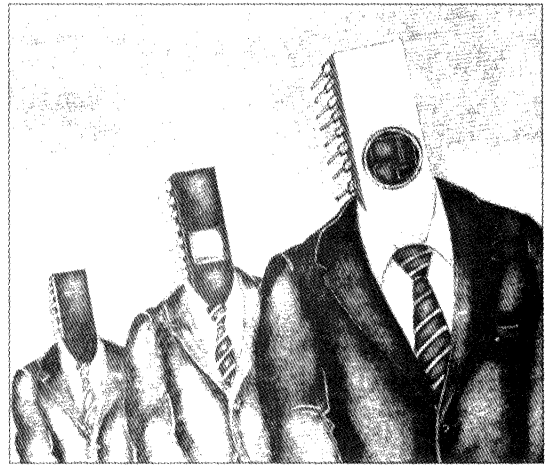
by Bernard C. Cole

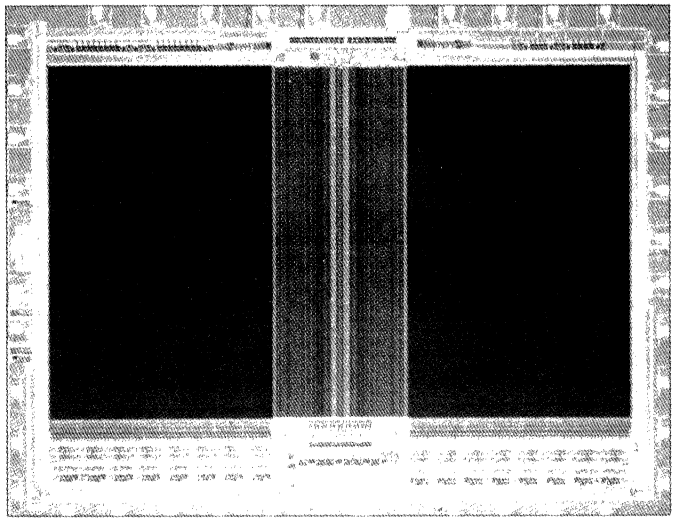
Nonvolatile memories are taking on a whole new look. As both erasable programmable read-only memories and electrically erasable PROMs get faster and denser, they are starting to displace high-density ROMs and high-speed PROMs in new applications. In current applications, nonvolatile memory will now take up significantly less board space. Higher densities also will make it easier to incorporate larger amounts of nonvolatile memory on other types of chips, opening the door to logic chips that integrate large arrays of EPROM and EEPROM.

A new generation of higher-density commodity parts is under development, while lower-density parts are being pushed to significantly faster access times. Moreover, the need for designers to choose between speed and density may disappear, as companies such as WaferScale Integration Inc. in Fremont, Calif., (see p. 65) develop parts that combine both features.

Beyond making improvements to conventional parts, a drive is under way among chip makers to develop memories tailored to specific market segments—markets where speed is paramount, or power requirements are important, for instance. An example of the latter is a 64-Kbit EEPROM that needs only 3 V, reducing backup battery requirements in lightweight portable equipment. The part was jointly developed by Catalyst Semiconductor Inc. of Santa Clara, Calif., and Oki Semiconductor Corp. of Tokyo (see p. 67). In addition, companies are looking to incorporate nonvolatile-memory technology into other non-memory chips, applying their expertise to a variety of logic circuits—including microcontrollers, digital signal processors, programmable logic, and even application-specific integrated circuits based on standard cells.

One reason for all the activity in nonvolatile-memory product development is today's healthy market. The current crop of EPROM and EEPROM products are chalking up very strong sales—so strong that cautious manufacturers are reluctant to believe the optimistic projections of future business, says Victor deDios, senior industry analyst at Dataquest Inc. of San Jose, Calif. Overall, he says, worldwide EPROM sales for 1987 can be expected to hit $1 billion, up 8% from $910 million in 1986 and up 14% from the reces-





1. FAST EPROM. A 64-K-by-16-bit EPROM developed jointly by Catalyst Semiconductor and Oki Semiconductor boasts a 150-ns access time.

sionary dip to $876 million in 1985. Next year, says deDios, with projected sales up 20% to $1.2 billion, they will again equal the sales for 1984, the industry's high point to date. Prospects are even brighter in EEPROMs. DeDios estimates that sales for 1987 will reach $231 million, up 61% from the $139 million in 1986. In 1988, he expects sales to grow by about 50% to $345 million.

And while the markets are taking off, somewhat surprisingly, Japanese makers of EPROM and EEPROM aren't keeping pace with the exploding market growth. They will slip from a market share of 15% to 20% in 1986 to less than 5% this year. To be sure, most U. S. manufacturers regard the Japanese slippage as temporary. Therefore, they're in a hurry to develop products that will put them in a strong position for both commodity parts and in high-return specialty niches when competition heats up again as the Japanese charge back into the marketplace.

For now, strong sales and the drop in Japanese competition is causing a period of price stability. And most EPROM manufacturers are using the resulting higher profits to fund more development work on CMOS processes that will take them to higher densities, higher speeds, and lower power, says deDios. The market is moving away from 64-Kbit EPROMs and toward 256-Kbit and 512-Kbit devices, says Dave Bostwick, director of strategic development for the memory group at Advanced Micro Devices Inc., Sunnyvale, Calif. Also entering the market in volume production are 1-Mbit EPROMs from AMD, Fujitsu, Hitachi, Intel, and Toshiba. One of the most recent arrivals on the 1-Mbit EPROM scene is the CAT27C210, a 64-K-by-16-bit CMOS device jointly developed by Catalyst and Oki (see fig. 1). Pin-for-pin compatible with Intel's 27210, it features 150-ns access times, an active power figure of only 150 mA, and a standby power of 500 μA.

One indicator of things to come is a 4-Mbit EPROM under development at Toshiba. Built using a 0.8-μm CMOS process, it incorporates a basic cell measuring only 9 μm^2, matching that of many single-transistor dynamic random-access memory cells. The 8-bit-wide device features a high cell current of about 10 μA, resulting in a low typical access time of 120 ns.

Access times are also being reduced in current lower-density EPROMs—from an average of 200 to 350 ns down to 150 to 200 ns, says Alan Ankerbrand, director of MOS memory marketing at National Semiconductor. And within a year, he says, speeds will edge downward even more, to about 100 to 150 ns. Dataquest's deDios agrees: "By this time next year anything under 512 Kbits in density with access times of more than 150 ns will be out of the mainstream."

In traditional full-function EEPROMs based on the Fowler-Nordheim effect, says deDios, the majority of the marketplace is moving from 64 Kbits to 256 Kbits. Most authorities agree current technology stops there, however: "Unless a radically new cell structure and architecture comes along, it will be difficult for EEPROMs to move beyond 256 Kbits," says Ian Wilson, director of product marketing at SGS Semiconductor Corp. U. S., in Phoenix, Ariz.

An alternative technology that many firms are looking at to break beyond 256 Kbits is "flash" architecture, so named because the contents of all the memory's array cells are erased simultaneously by a single field emission of electrons from the floating gate of an erase gate. Such an EEPROM combines the advantages of the ultraviolet-light-erasable PROM and floating-gate EEPROMs. It unites the high density, small size, low cost, and hot-electron-write capability of an EPROM with the easy erasability, on-board reprogrammability, high endurance, and cold-electron-tunnelling erasure of floating-gate EEPROMs.

So far, the only player in the flash EEPROM market is Seeq Technology Inc., San Jose, Calif., which introduced its first device, the 128-Kbit 48128, in August 1986. It is now following up this initial n-MOS part with two higher-density 1.5-μm CMOS parts, the 512-Kbit 48C512 and the 1-Mbit 48C1024, both with 8-bit-wide organizations. With a memory-cell size of only 20 μm^2—about one quarter the size of current EEPROM cells—these parts achieve EPROM die sizes, says

Mike Villott, vice president of marketing at Seeq, and they provide EEPROM features previously not available. Such features include on-chip address and data input latches to permit microprocessor-compatible write and erase cycles, as well as chip-erase and page-erase modes.

And whereas the 48128 required a 21-V power supply on multiple pins, the new flash EEPROMs require only a single 12-V external supply for programming and erasure. Moreover, he says, this programming voltage can be applied during read operations, which eliminates the need to switch it off when not erasing or programming. Byte write time is only 1 ms, and chip and byte erase times are no more than 5 s. Endurance—the number of times the device can be erased and written to—is 100 cycles minimum and can be screened to 1,000 cycles.

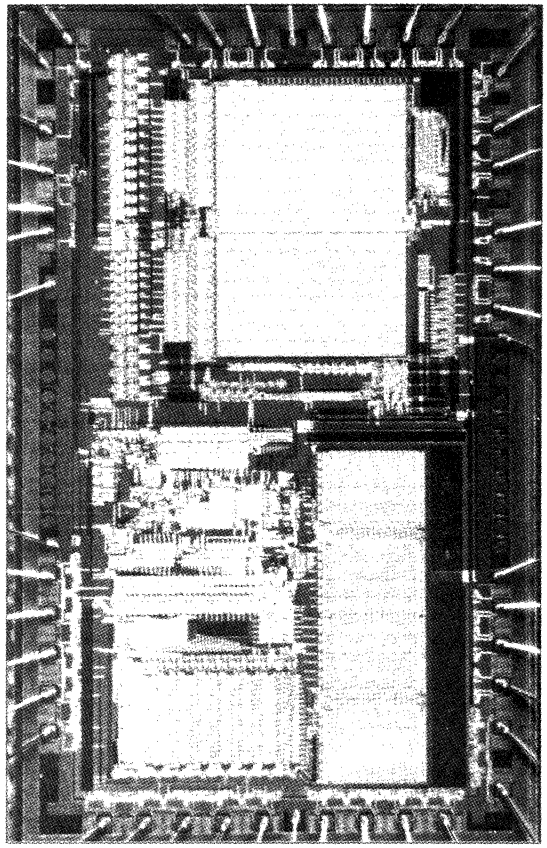
Hoping to follow Seeq into the market with a high-density flash EEPROM is Exel Microelectronics of San Jose, Calif., which is in development on a 512-Kbit device it expects to introduce early next year. Also investigating the technology as a way to achieve higher EEPROM densities are AMD, Fujitsu, Hitachi, National Semiconductor, Texas Instruments, and Toshiba.

Another recent convert appears to be Intel Corp., Santa Clara, Calif., although until recently it was enthusiastically exploring another approach to high-density EEPROMs, the thick-oxide technique pioneered by Xicor Inc. of San Jose, Calif. Intel, however, has abandoned its efforts in this area, says Don Knowlton, general manager of Intel's programmable-memory operations in Folsom, Calif., and is investigating other techniques for higher density, including the flash-EEPROM approach.

That leaves Xicor going it alone with the thick-oxide technique. The company is now in production with a 256-Kbit n-MOS device, the X28256 [*Electronics*, May 12, 1986, p. 30] and is also developing a CMOS version, the X28C256, which it expects to introduce later this year, and a 1-Mbit device tentatively scheduled for early next year.

For many manufacturers, however, the bright prospects in the mainstream EPROM and EEPROM market are essentially an opportunity to carve out new niches. The past has taught them a painful lesson: the memories may be nonvolatile, but their market is not. They want to find areas where price pressure and competition are less intense. Among the possibilities they're exploring are high-speed bipolar PROM replacements, parts tailored to specific applications such as smart cards, and other applications outside the traditional domain of EPROMs and EEPROMs.

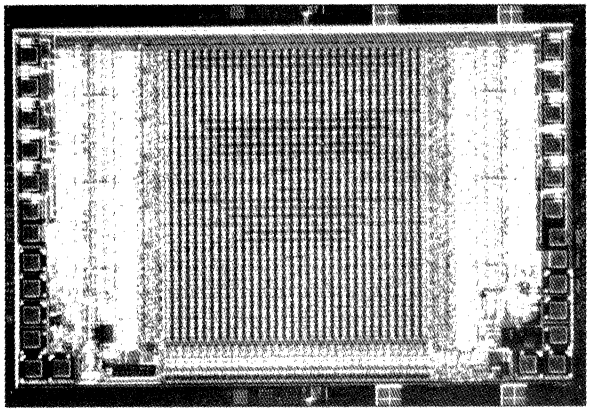
Two companies that have successfully established themselves in the bipolar PROM replacement market are Cypress Semiconductor Inc. of San Jose, Calif., and WaferScale Integration, with 16-Kbit and 64-Kbit CMOS EPROMs in the 35-to-50-ns range. Also looking to participate is Seeq, which has just introduced two byte-wide



2. REPROGRAMMABLE DSP. General Instrument has put 2.5 Kbytes of EEPROM on a digital signal processor chip.

35-ns EEPROMs, the 16-Kbit bit 36C16 and the 32-Kbit 36C32 [*Electronics*, April 30, 1987, p. 66]. Others thinking hard about entering the market include AMD, Intel, and SGS.

Another niche is being explored by Intel, which is looking at what Knowlton calls "application-oriented" EPROMs—nonvolatile memory devices with extra logic that optimizes the devices for specific applications. One of the company's first efforts in this direction was the 27916 KEPROM, or keyed-access EPROM, which combines the memory array with a pseudo-random number generator and encryption circuitry that can determine if the person accessing its contents is authorized. Taking the concept even further, the company this month introduced the first in a new series of such applications-oriented EPROMs, the 87C257 and 68C257—256-Kbit devices with on-chip latches that allow the memory's address and data pins to be tied directly to a microcontroller's multiplexed address and data



3. ERASIC. Exel's 78C800 is the first in a family of what it calls electrically reprogrammable ASICs, made with EEPROM technology.

pins. The two devices, intended for the 8051/8096 and 6800 series of microcontrollers, respectively, eliminate the need for the external logic, such as latches and inverters, that is typically required in microcontroller-based systems, says Tom Price, EPROM marketing manager.

Japanese firms seem to be carving out a niche for themselves in extremely high-density EEPROMs and EPROMs of more than 1 Mbit, for use in smart cards and memory cards. Estimated to be a billion-dollar market by the early 1990s [*Electronics,* Dec. 18, 1986, p. 55], smart cards will require high levels of built-in microcontroller intelligence, as well as memory that is both dense and nonvolatile. The only direct U. S. competitor to the Japanese in the EEPROM- and EPROM-based smart- and memory-card market is General Instrument Microelectronics, Chandler, Ariz. Besides planning to produce EPROMs and EEPROMs ranging from 256 Kbits to 1 Mbit over the next six months, the company has installed the equipment to make the smart cards themselves, as well as card readers, power supplies, and connectors. Also making efforts in this direction are Texas Instruments Inc. and Motorola Inc., but only at the chip level. The fourth contender in this arena is the team of Catalyst Semiconductor Inc. and Oki Semiconductor, which aims to produce controllers and EEPROMs.

Another strategy EPROM and EEPROM companies are following is diversification outside traditional stand-alone products. They are applying their improved nonvolatile technology to microcontrollers, DSPs, field-programmable logic, and even standard-cell ASICs.

Traditionally, small amounts of EPROM or EEPROM—usually no more than 1,024 bits—have been incorporated into microcontrollers to give users some reprogrammability. "With new advances in nonvolatile memory technology, much higher levels can be incorporated," says B. K. Marya, president of Catalyst Semiconductor. In the new generation of devices from AMD, Catalyst, Intel, SGS, and Xicor, on-chip nonvolatile memory has risen to 32 Kbits or 64 Kbits.

On-chip nonvolatile memory is also being used on DSPs. One such device is the DSP320EE12 from General Instrument, a pin-for-pin compatible version of TI's TMS320C10 DSP chip, but with 2.5 Kbytes of EEPROM added (see fig. 2). In the very near future, says Marya, it should be possible to incorporate up to 256 Kbits onto the microcontroller chip.

In programmable logic devices, two nonvolatile memory vendors—Intel and the Exel subsidiary of Exar Corp., San Jose, Calif.—have already entered the market. A third, Seeq, has just entered into a technology exchange agreement with Monolithic Memories Inc., which dominates the field-programmable array-logic market with its bipolar devices.

Just entering the market this month with a PLD product based on its EEPROM technology is Exel, with the first in a family of what it calls ERASICs, or electrically reprogrammable ASICs. Designated the 78C800 (see fig. 3), it is the first commercially available CMOS PLD offering a single-plane folded-NOR architecture, says Narayan Purohit, Exel product marketing manager. This approach makes it possible to implement multilevel logic designs and does away with the limitations of the traditional AND/OR-based designs now used. Intel's first proprietary PLD is an EPROM-based programmable bus-interface controller designated the 5CBIC. A programmable three-port transceiver with embedded programmable logic macrocells and cross-point signal routing, it allows designers to implement any of a number of different bus interfaces with a single circuit. A third company, WaferScale Integration, is working with Altera Corp. of Santa Clara, Calif., a manufacturer of EPROM-based PLDs, on a new family of user-configurable microsequencers based on its proprietary high-speed split-gate technology [*Electronics,* March 19, 1987, p. 76].

On the standard-cell side, at least two nonvolatile-memory companies—WaferScale and Exel—are in the market with cell libraries that incorporate EPROM and EEPROM cells, respectively. Similar efforts are under way at Intel and National Semiconductor, among other companies. In the Exar effort, Exel's EEPROM technology has been incorporated in standard cells ranging from a single bit to arrays of 1 Kbits. The same family of products also includes a wide range of analog megacells, including analog-to-digital and digital-to-analog converters and a variety of switched-capacitor filters. At WaferScale, engineers are upgrading an already existing EPROM-based cell library with cells that incorporate the company's newest and fastest EPROM technology. □

CATALYST'S EEPROM NEEDS A MISERLY 3 VOLTS

Five volts is no longer the magic number when engineers talk portable and battery-backed applications. Catalyst Semiconductor Inc. of Santa Clara, Calif., has just put the finishing touches on a 64-Kbit EEPROM that reads and writes with a supply voltage as low as 3 V. And this diminutive appetite comes at no substantial cost in speed. With an access time of 120 ns, the memory keeps pace with many existing 5-V devices. When operated at 5 V, its reads take a mere 60 ns. Also in its favor is the fact that it draws an active current of only 7.5 mA at 8 MHz, about a fifth that of its rivals.

Low voltage opens up a wide range of battery-backed applications, says B. K. Marya, Catalyst's founder and president—among them, hand-held computers, smart cards, pagers, beepers, and many telecommunications devices, which require long-term battery backup as well as small size.

The memory also will compete with nonvolatile static random-access memories that incorporate a 3-V lithium battery. "The advantage of battery-powered nonvolatile SRAMs is their ability to read and write data with access times of 120 ns or less," Marya points out. Moreover, "traditional high-density EEPROMs of 64 Kbits or more usually require at least a 5-V read and write voltage. And they are not only slow but also difficult to operate if reprogramming is necessary, requiring as they do at least four AA-type batteries or an expensive lithium power source." Because it can be operated and programmed with a 3-V supply, the device requires only two 1.5-V batteries in portable consumer settings and makes it possible to go with small lithium power sources in smart cards. Eventually, Marya says, as the power-supply requirements of EEPROMs continue to decline, it may be possible to substitute solar cells for batteries in a wide variety of applications.

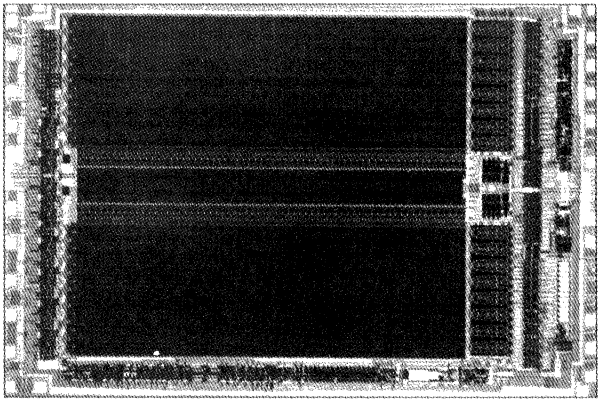
The EEPROM is the fruit of international cooperation. The cell and circuit design were contributed by Catalyst, which also created and modified the architecture. Oki Semiconductor of Tokyo furnished the process, jointly modified by the two partners, and served as the silicon foundry.

Critical to the success of the joint venture was a variety of proprietary circuit wizardry. Broadening the supply-voltage range ensured successful reads and writes despite voltage fluctuations. Bootstrapping capacitors and a clever differential sense amplifier make certain that reads are accomplished quickly in the face of low voltage and power-supply variations.

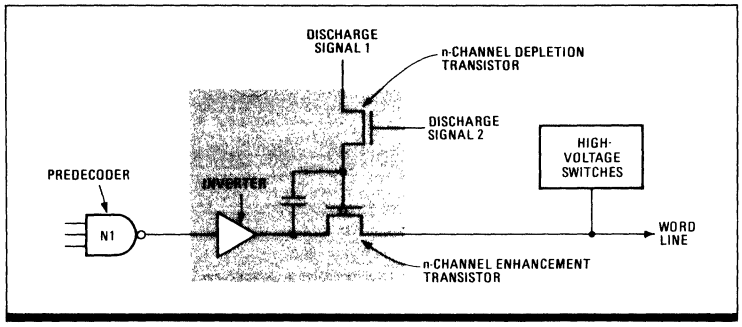
In addition, a dual-clocked, high-voltage switching circuit guarantees that switches are thrown reliably, even when the voltage fluctuates. And dynamic, rather than static, page latching keeps the memory writing even while supply voltage varies.

Measuring 4.84 by 7.06 mm and housed in a 28-pin plastic dual in-line package, the Catalyst MSM28C64A (see fig. 1) is fabricated with a slight modification of Oki's 1.5-μm n-well double-polysilicon CMOS floating-gate process. The memory incorporates five types of transistors: p-channel and n-channel enhancement-mode MOS transistors for fabricating the 3-V circuits, and enhancement, depletion, and non-ion-implanted n-type transistors for fabricating the charge-pumping circuitry that converts the 3-V supply to 18 V on-chip; in addition to these transistors, there are the floating-gate devices themselves.

The key to achieving low-voltage operation in portable applications is the ability to maintain stable reads and writes over long periods, despite the substantial variations in supply voltage associated with batteries. Relaxing the supply-voltage tolerances of the basic EEPROM cell makes that possible. With its dynamic page-mode latching scheme, the device is relatively insensitive to voltage changes and can operate even if the supply voltage varies 20% in either direction, Catalyst claims. By comparison, most competitive devices can operate only within variations of ±10 V. When operated at, for example, 5 V, the Catalyst part's supply voltage can vary from 4 to 6 V, whereas conventional EEPROMs



1. LOW VOLTAGE. Catalyst's MSM28C64A EEPROM has five types of transistors that form the charge-pump circuit needed to convert the 3-V supply to 18 V on-chip.



2. BOOTSTRAP. A decoder circuit with bootstrapping capacitor beween the two cell transistors helps keep read operations fast despite lower voltages and wider supply tolerances.

have a much narrower operating margin, from 4.5 to 5.5 V.

An additional benefit of the lower operating voltage is that power dissipation is 25% to 50% less than that of comparable devices. At 8 MHz, active power is 49.5 milliwatts and standby is only 22.5 mW. At 1 MHz, active and standby power are 15 mW and 7.5 mW, respectively.

The low operating voltage was achieved with a variety of design improvements in both the read and write circuitry. Special bootstrap decoder circuits and a differential sense amplifier made it possible to keep reads fast despite the lower voltages and wider supply tolerances. In the first instance, the key was adding bootstrapping

Catalyst uses dynamic page-mode latching, opening the door to battery operation; the usual static latching needs a highly stable supply voltage that batteries can't supply

capacitors between the two transistors in the cell and between the decoder and the output to the word line (see fig. 2). "In present designs, when the supply voltage is too low, there is insufficient voltage across the enhancement-mode read transistor to allow it to switch reliably," Marya says. "With the addition of the bootstrap capacitor, sufficient charge is accumulated to stabilize the voltage during the read operation."

To prevent latchup that might be caused by a large instantaneous discharge of current from the capacitor onto the word line, which could occur during a write, the circuit also incorporates a predecoder to step down the discharge incrementally. The differential sense amplifier also boosts the EEPROM's reliability during reads. "In other designs, when the threshold voltage of a memory cell is set to the low state during a read, a very small current flows into the bit line, on the order of about 70 to 100 μA," says Marya. "Normally, in most 5-V designs there is sufficient voltage, on the order of 0.1 to 0.2 V, to trigger the sense amplifier." In Catalyst's 3-V design, however, the voltage change is only on the order of 0.02 V. With the use of a differential sense amplifier rather than a single-ended one, this minute voltage differential is magnified about 100 times to a level sufficient to trigger operation.

To achieve low-voltage programming, Marya says, Catalyst and Oki engineers made a number of improvements to the high-voltage switches and to the page-mode latches. Usually, the high-voltage switches are controlled by a single clock, so there is only a relatively narrow range within which the switch can sense the clock edge reliably. In 5-V devices, this occurs as long as the voltage is between 4.5 and 5.5 V. Below 4.5 V, such designs fail, switching erratically. Designers from the two companies solved this, he says, by going to a fail-safe switching scheme in which a dual clock is used, allowing the switches to operate reliably over the entire range from 3 to 7 V.

In the other critical improvement to the programming circuitry, company engineers went with a dynamic page-mode latching scheme, rather than the static configuration generally used, which is highly dependent on supply voltage for correct operation. "If the supply voltage varies outside a very narrow range of a few tenths of a volt, static latching no longer works," Marya says. "With a dynamic scheme, the page-latch threshold levels vary dynamically up and down as the supply voltage varies."

As with most other high-density EEPROMs, the 16-K-by-4-bit device also incorporates two redundant rows in the event of faulty array cells. This meant that it was necessary to modify the redundant cells to operate at lower voltages. Since they are located farther out on the array, they are served by longer lines, which means more capacitance or sensing lower-voltage signals. Here, the basic changes involved modifications to the interpoly oxide to take into account the lower voltage by reducing the load capacitance. Taking advantage of the differential-sensing scheme employed in the array, a special reset circuit selects a redundant word line when a faulty bit occurs in one of the word lines. The proprietary circuit works even when the supply voltage is as low as 1 V and consumes practically no power, Marya claims. The same scheme is also employed to select or key in EEPROM-based circuit elements to trim the programming voltage and the write cycle. *–Bernard C. Cole*

For more information, circle 481 on the reader service card.

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HOW LINEAR IC DESIGNERS ARE BUILDING DENSER CHIPS/67

EXECUTIVE OUTLOOK: NO SLOWDOWN IN TECHNOLOGY/86

DECEMBER 18, 1986

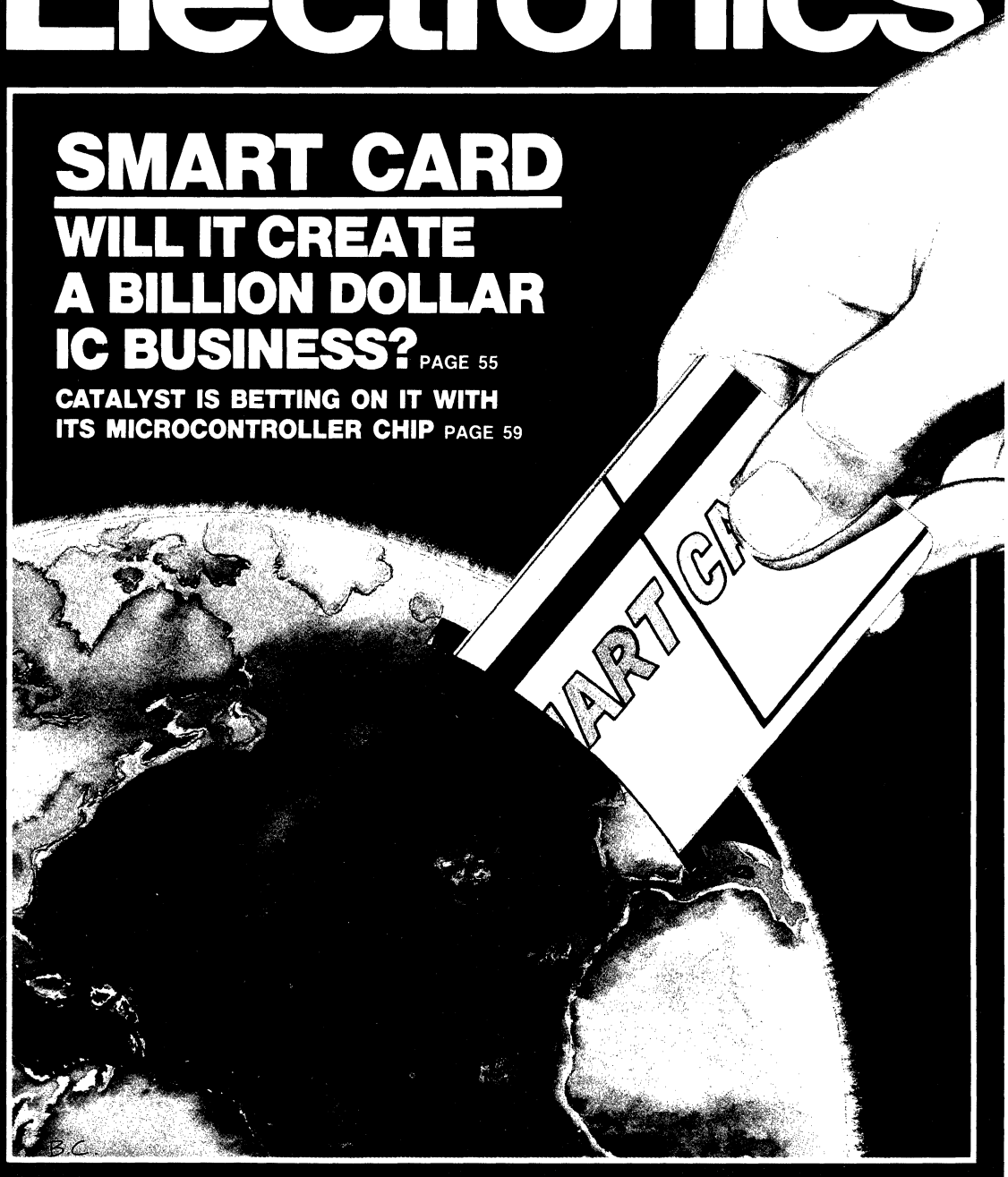
Electronics

SMART CARD

WILL IT CREATE A BILLION DOLLAR IC BUSINESS?

PAGE 55

CATALYST IS BETTING ON IT WITH ITS MICROCONTROLLER CHIP PAGE 59



DOES CATALYST HAVE THE KEY TO SMART CARDS?

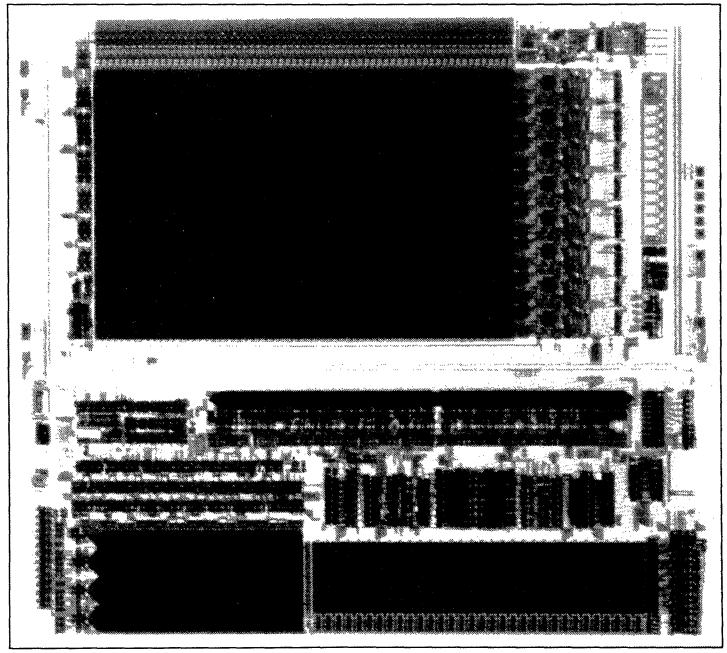
Catalyst Semiconductor thinks that its new chip, which meets ISO smart-card standards and has 2-K bytes of EEPROM, could finally open up the market

A tiny but powerful microcontroller from Catalyst Semiconductor Inc. may be the key that will unlock a worldwide billion-dollar business in smart-card chips. Measuring 4.5 by 5 mils by only 200 μm thick, the CAT61C580 chip is small enough to meet size requirements set by the International Organization for Standardization for smart-card applications, yet it packs 2-K bytes of electrically erasable, programmable read-only memory. That's at least four times the EEPROM of any other ISO-compliant smart-card chip now available using the same 2-μm CMOS design rules.

The Santa Clara, Calif., company achieved this density by stripping away the peripheral logic around the EEPROM and writing these functions into microcode. That left plenty of room for the 2-K bytes of EEPROM, and the chip is still about 30% smaller than competing devices that have only a fourth or less memory. What's more, Catalyst is working on an 8-K-byte chip, which will be made by shrinking the current 220-μm^2 EEPROM cell size to 80 μm^2 with a combination of proprietary design refinements and 1.5-μm geometries. The CAT61C580 is just being released; the 8-K-byte chip should be available next year.

Working in conjunction with joint developer Oki Electric Co., Tokyo, Catalyst designers modified an Oki microcontroller by adding a programmable logic array and 2-K bytes of EEPROM. (Fig. 1). They also managed to squeeze in 3-K bytes of ROM, 128 bytes of random-access memory, and enough electrostatic-discharge-protection circuitry to protect the chip from up to 15,000 kV, enough to protect against the static electricity generated by removing a credit card from a pocket or a billfold.

In addition, the CAT61C580 op-



1. LITTLE GIANT. Catalyst's 8-bit microcontroller is tiny enough for use in smart cards, yet it has an elephant's memory.

erates at the ISO-recommended frequency of 4.9 MHz with a high-speed instruction-cycle time of 813.8 ns, allowing it to run at the ISO's recommended 9,600 baud through a single serial input/output pin. Power dissipation of the 8-bit chip is only 20 mW.

The architecture of the chip allows asynchronous, two-way communications through a single serial I/O pin. This eliminates the need for a universal asynchronous receiver/transmitter and an interrupt, reducing the number of pins to only five—one third to one half of what's required in other approaches.

A TANTALIZING IDEA

The idea of EEPROM-based microcontrollers has long captured designers' imaginations because of the wide range of applications—not only for smart cards, but also for robotics, artificial intelligence, industrial controls, consumer products, and more. But so far, applications have been limited to a small number of niche markets for controllers, because of the small amount of EEPROM that could economically share the same chip as the microcontroller. Smart cards are one application that promises to allow EEPROM-based microcontrollers to break out of their niche; now that such a powerful chip that meets ISO smart-card standards exists, that breakout could be imminent. And with the increased memory that is promised, the chips will have a crack at the full range of potential microcontroller markets.

Catalyst president and founder B. K. Marya claims his is the only chip that meets, and in some cases exceeds, all of the ISO requirements for smart-card applications, including area, thickness, electrostatic discharge, power dissipation, and speed. Of these, the first three are the most critical, he says.

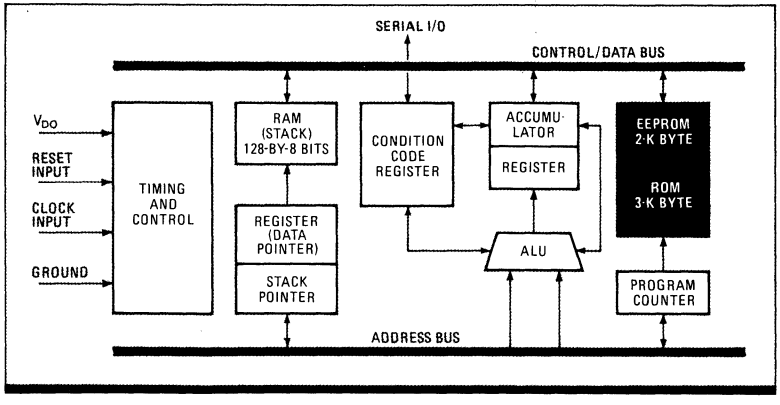
"The thickness must be no more than that of a standard credit card, 200 μm. And the area must not only be 5 by 5 mils or less, but [the chip must] be as square as possible, to prevent the possibility of breakage when the card is bent. In addition, the chip must be capable of withstanding the electrostatic discharge that builds up taking credit cards in and out of pockets and wallets." This buildup has been measured in excess of 10 kV, he says.

The 2-K-byte chip is aimed at a projected near-term market for smart cards that some estimate to be worth hundreds of millions of dollars (see p. 55). In a typical smart-card transaction, a card holder puts the card in a point-of-sale terminal. The terminal supplies the card with electric power and communicates to the card's microcontroller through pin contacts on the card's surface. The user is asked to enter a password. When the sale is rung up, the amount of the transaction is stored in the card's EEPROM, credited to the retailer's account, and debited from the card holder's credit balance, which is also stored in the card's memory. The card holder can replenish the credit balance at an automatic-banking machine.

What has held back the development of the EEPROM-based microcontroller market, Marya says, is the fact that, although stand-alone EEPROM parts of 16-K, 64-K, and 256-K densities are becoming commonplace, EEPROM-based microcontroller densities have trailed the stand-alone densities by at least four generations.

One way to achieve more on-board EEPROM is to advance the processing state of the art: scaling down the lateral dimensions from geometries between 2 and 3 μm to between 1.25 and 1.5 μm, and the vertical dimensions on the EEPROM from 150 to 250 Å down to 80 to 90 Å, which comes close to the limits at which EEPROMs operate reliably. The problem with this, says Marya, is that it requires manufacturers to push the process technology for microcontrollers beyond what is currently available even for stand-alone EEPROMs. And although such an advance is technically feasible for the high-volume applications that could use such large EEPROM/microcontroller combinations, the high cost of manufacturing such devices rules out their use. Marya says there is also the problem of reliability, which is critical for smart cards, where data integrity and security are important. So to make room for more EEPROM, Catalyst replaced the peripheral-function circuitry with microcode.

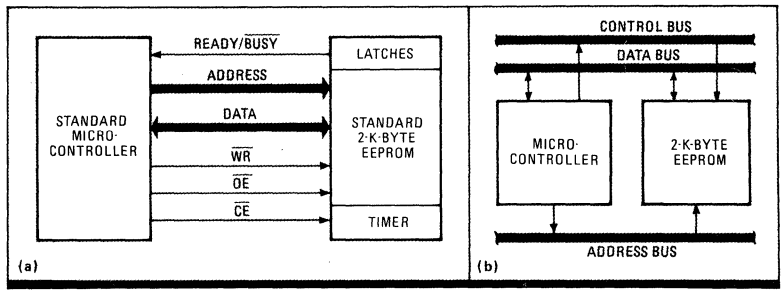
To get 2-K bytes of EEPROM into an ISO-standard smart-card chip, says Marya, "what is required is a fundamental rethinking of the architecture of EEPROM-based microcon-



2. ATTRACTIVE SWAP. By writing the latch, timer, and test logic functions into microcode, Catalyst designers were able to free up more than enough room on the chip for 2-K bytes of EEPROM.

trollers. Basically, most current implementations are 'brute-force' affairs combining the functions of an EEPROM and a microcontroller on the same chip, without any modification whatsoever."

By writing the functions of the EEPROM's peripheral logic into microcode, Catalyst has freed up real estate for more EEPROM. "Essentially, we have taken a standard EEPROM device, stripped off such peripheral circuitry as the latches, timers, and self-test logic, and incorporated these functions into the microcode of the on-board 8-bit microcontroller (Fig. 2), resulting in a 5-by-4.5-mm die size," says Marya. To achieve these breakthroughs, Catalyst designers came up with an architecture that differs from standard single-chip EEPROM/CPU implementations in five fundamental ways.



3. SIMPLIFIED BUS. By eliminating latches, timers, and test logic, the complex bus structure of a standard EEPROM-based chip (a) is replaced with a simpler three-bus arrangement (b).

First, even though it uses the same 200- to 250-μm^2 cell structure as the CPU, the 2-K-byte EEPROM takes up only half the area of the microcontroller. Second, the microcontroller's microcode has been expanded to include the latch, timing, and test functions usually associated with the operation of the EEPROM. Although this increases the area occupied by the microcode by 5%, eliminating the peripherals from the EEPROM circuitry saves 20% of the EEPROM's space.

Third, the bus architecture has been simplified. In the traditional one- and two-chip approach (Fig. 3a), at least six separate data, address, and control lines link the EEPROM and the CPU. Moreover, Marya says, the user has to provide necessary waveforms on control pins WE, OE, and CE, along with the valid data and address. The completion of programming is signaled via the RDY/BUSY pin, which has to be monitored by the microcontroller. In the CAT61C580, the interface between the CPU and the EEPROM is reduced to a three-bus structure (Fig. 3b), because the EEPROM's hard-wired latches and timer are eliminated. In addition, testing of the EEPROM is done internally, eliminating the need for test pads.

Fourth, the addressing scheme has been modified, says Marya, in that the EEPROM is above the ROM address space but, unlike the ROM, it is addressed through RAM. The addressing scheme is made efficient by eliminating page boundaries and providing both direct and indirect addressing of the RAM.

Finally, two additional registers have been added to the basic architecture: a B register to enhance the arithmetic logic unit's computation-intensive tasks, and a D register, which can be auto-incremented or -decremented to enhance the speed of the RAM's read and write operations. The 128-by-8-bit RAM provides 32 levels of nesting, and it can be used as a stack for pop and push operations.

WHAT'S IN THE MICROCODE

Most of the read, write, and erase functions are performed using two simple move commands incorporated into the CPU's microcode, MOV_1 and MOV_2. The first command transfers data from the internal RAM to the EEPROM, erasing previous data after receiving the appropriate 24-bit security code. The second command reads data out of the EEPROM locations and into the RAM. With these commands, EEPROM programming is made totally transparent to the user. "This transparency adds an additional level of security and reliability, since, unlike other implementations, the actual mechanism of writing into EEPROM is never revealed to the user," says Marya.

In addition to these special instructions, there are the 95 other housekeeping commands usually incorporated into a microcontroller: 55 one-byte instructions, 35 two-byte instructions, and 5 three-byte instructions. However, the instructions have been modified to reflect the chip's use in smart-card applications. The large number and smaller width of instructions provide more programming power to the user, and that's important in smart cards, where programming space is limited to on-board ROM, says Marya.

Security is also essential for smart-card applications, because the user stores important financial and personal information in the card's EEPROM. So Catalyst designers incorporated a set of special instructions into the microcode and a program into the on-board ROM that allows a three-level security scheme. "In a credit card application, this would make it possible not only for the primary user, say the financial institution, such as MasterCard or Visa, to have an access code, but the issuing bank and the individual card user as well—the first incorporated into the nonerasable ROM when the chip is sold to the issuing institution, and the other two inserted into the EEPROM when the card is issued to a customer," says Marya. "In any transaction, all

three codes must be matched before any information is revealed to the user or any data is changed on the card—the first two between the card and the machine automatically, and the third by the user on request."

The high voltage for erasing and programming the EEPROM cell is generated on the CAT61C580, so the chip needs only a single power supply of 5 V. Fabricated with a 2-μm EEPROM process, which combines a 2-μm CMOS logic process with a conventional high-voltage two-transistor, floating-gate tunnel-oxide EEPROM process, the chip's EEPROM is specified for 10,000 program-erase cycles and 10 years of data retention. The process uses dual oxides—a thin oxide to obtain high-speed EEPROM read capability and a thicker oxide to withstand the 21 V required for erasing and programming the cell.

In this scheme, Marya says, the user can change his code at regular intervals, as can the issuing institution via the automatic teller machine. Also, the card-reading machine can be programmed to disqualify the card after a certain number of unsuccessful attempts to enter the code. In addition, he says, further levels of security can be incorporated into the EEPROM, such as specifying several individuals who are authorized to use the card, and their credit limits.

Catalyst is evaluating a number of strategies to take advantage of planned second-generation improvements. First, implementing the 2-K-byte architecture in 1.5-μm CMOS and using the 80-μm^2 cell that is now under development will reduce the die size of 2-K-byte devices by as much as 50%, while increasing the number of dice per wafer and lowering the cost of the finished devices. Alternatively, the same process improvements will allow an increase in EEPROM array capacity from 2-K bytes to 8-K bytes without substantially increasing the present die size. Finally, Marya says, the enhancements will allow fabrication of 16-bit microcontrollers with as much as 32-K bytes of EEPROM, opening a host of application areas that require real-time response, such as artificial intelligence, robotics, and high-performance industrial and military controllers. □

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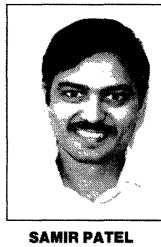
MARYA: THE MICROCONTROLLER COULD BE THE NEXT GREAT 'GIZMO'

"For years the semiconductor industry has been looking for the electronic gizmo that would approach the dollar and unit volumes that digital watches, calculators, and video games generated," says Bharat Kumar Marya—"B. K." to his friends and associates. The president and founder of Catalyst Semiconductor Inc., Santa Clara, Calif., believes that smart cards are just the tip of the iceberg in a market for nonvolatile memory-based microcontrollers that he thinks may reach $2 billion a year by the mid-1990s.

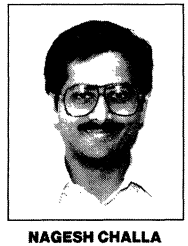
Marya, 38, thinks that many observers expect growth to come from the wrong places. "Almost everyone has turned their eyes toward personal computers and work stations, which have quickly moved from 8 to 16 to 32 bits," he says. But as explosive as that market was at its beginning, it has begun to level off in terms of growth and penetration. Moreover, he says, the largest share of the profits went to original-equipment manufacturers and system integrators, not to chip manufacturers.

"The only market that has a good chance of recreating the bonanza of dollars and unit volumes of the past is the market for smart integrated-circuit cards built around EEPROM-based, 8-bit microcontrollers," says Marya, who points out that there are some 200 million banking and credit cards in circulation. He projects that by 1990 about 25% of these cards will be integrated-circuit-based. Beyond this, he says, there are other potentially huge replacement markets, such as telephone credit cards, as well as new applications, such as health-history cards, warranty cards, security cards, military dog tags, welfare cards, and passport cards.

B. K. MARYA



SAMIR PATEL



NAGESH CHALLA

Although many of these potential IC-card applications are already being test-marketed in Europe and Japan, Marya says, the major market will ultimately be the U. S. "Ironically, virtually no U. S. semiconductor company, with the exception of some tentative efforts on the part of Motorola, is taking steps to participate in this market," he says. "U. S. companies must act fast, or we'll lose another major market."

To enter Catalyst in this market sweepstakes, Barya set up a joint development agreement with Oki Electric Co., Tokyo, 18 months ago. "We provided the basic architecture modifications, the circuit design, and the EEPROM expertise," he says. "They provided the process and fabrication capability."

Maintaining communications and schedules for the joint project required many transoceanic flights by Marya, design manager Nagesh Challa, Catalyst senior design manager Samir Patel, and Tomoaki Yoshida, an Oki section manager in Japan.

Catalyst is Marya's second startup. His first, Exel Semiconductor, an EEPROM and EPROM manufacturer, was acquired this year by Exar Inc. Marya earned a BSEE from Punjab University, India, and an MSEE from the University of New Mexico. He has since directed the design, construction, and operation of fabrication lines at several companies, including Hewlett-Packard, National Semiconductor, Synertek, and Seeq Technology.

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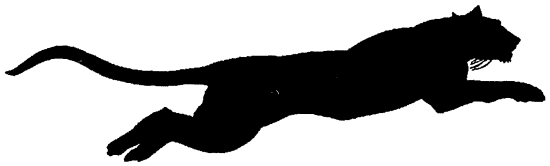

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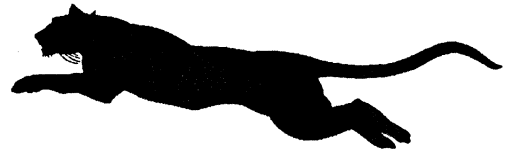

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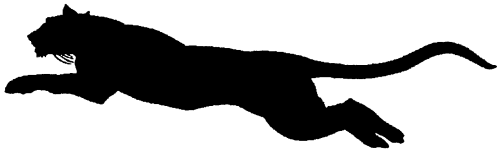

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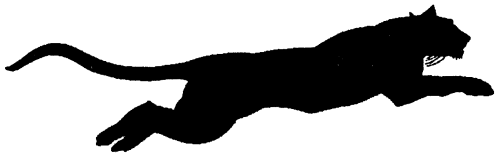

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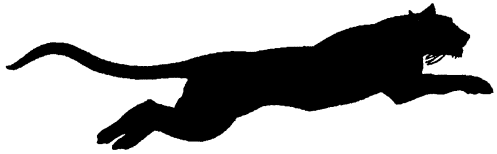

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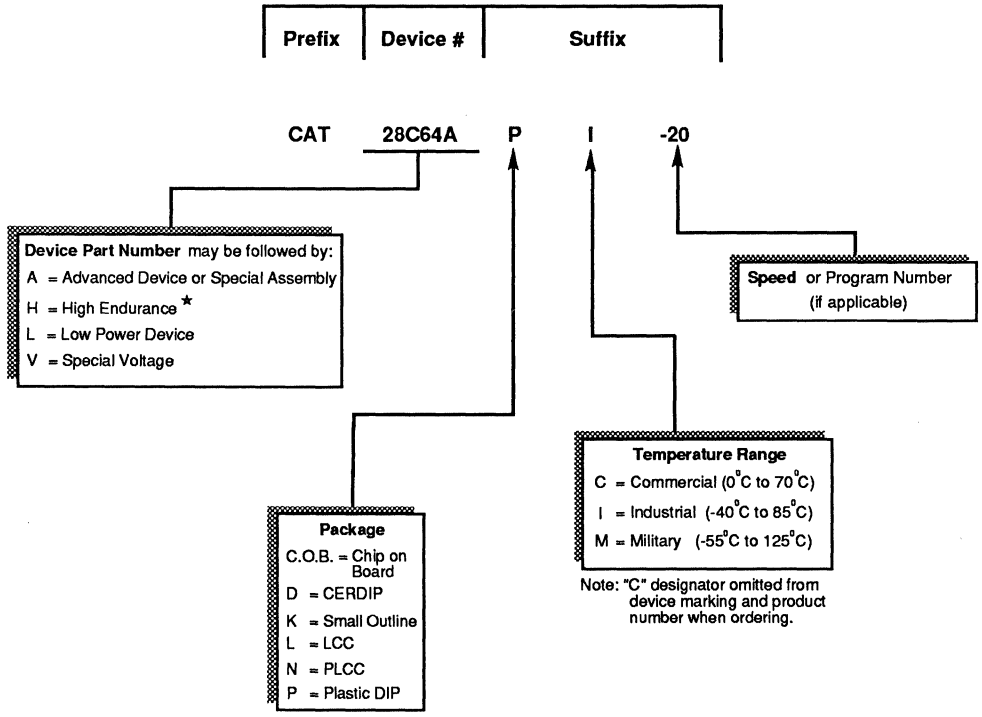

The device used in the example above is a CAT28C64API-20 (Plastic DIP, Industrial temperature, 200ns access time).

* High Endurance Device: minimum 100,000 write/erase cycles and 100 year data retention.

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