CIRRUS LOGIC

CL–CD2400/CD2401

Product Bulletin

FEATURES

- Four full-duplex multi-protocol channels (asynchronous, character synchronous and HDLC framing)
- Bit rates to 64K bit/sec on transmit and receive
- 32-bit address, 16-bit data double-buffered DMA controller for each transmitter and receiver (8 total)
- Two independent bit rate generators for transmit and receive per channel
- NRZ, NRZI and Manchester data encoding supported
- Digital PLL on each receiver
- Two independent timers per channel

Synchronous Operation Features:

- Programmable frame start/end and idle character
- Optional CRC generation and validation

HDLC Features:

- Four 8-bit or two 16-bit frame address matching
- FCS generation and validation
- CRC optionally readable
- Programmable leading pad character transmission to facilitate DPLL locking on receiving end

Four-Channel Multi-Protocol Communications Controller

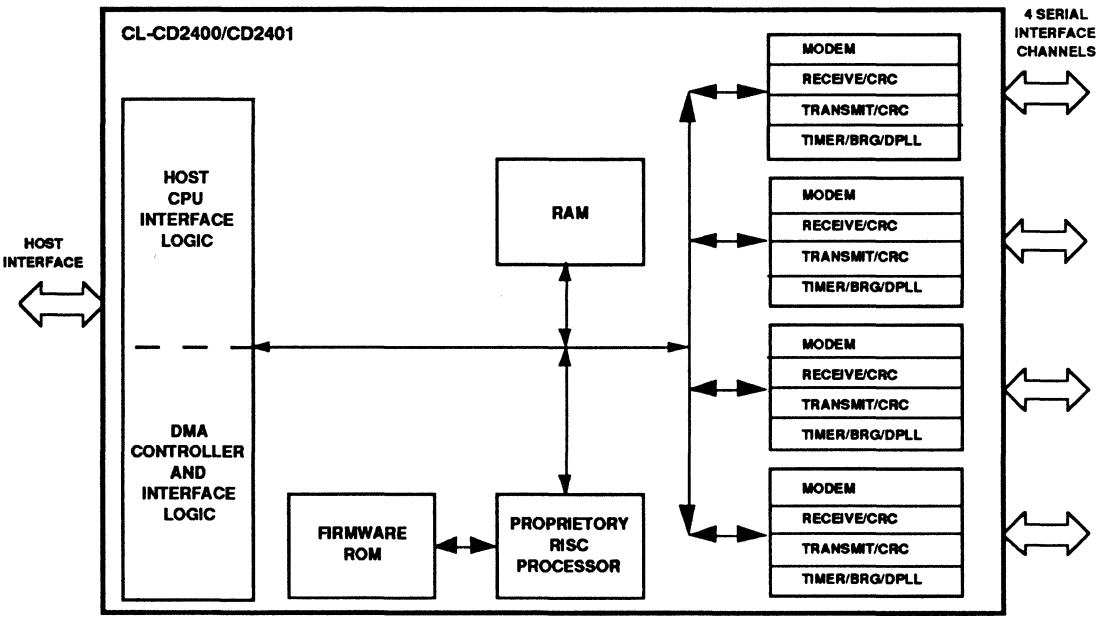
OVERVIEW

The CL-CD2400/CD2401™ is an intelligent co-processor for all types of synchronous and asynchronous communications. It is based on an on-chip, high-performance RISC processor and a flexible DMA controller with sophisticated buffer management. It has four fully independent serial channels that support all popular asynchronous, character-synchronous, and bit-synchronous protocols, at rates up to 64 kbps.

The CL-CD2401, which comes packaged in a 100-pin Plastic Quad Flat Package, provides extra modem signals for each serial channel. However, the 84-pin CL-CD2400 is functionally equivalent to the CL-CD2401.

The unique advantage of the CD2400/CD2401 is that it substantially reduces the processing burden on the host system, by off-loading these functions to its own processor. There are 16-byte FIFOs for each channel, which, combined with the DMA controller, eliminate the need for the host CPU to be involved in data transfers in real time. Additionally, the CD2400/CD2401 can monitor data being transferred and take appropriate special action when required, such as sending and responding to flow control characters.

CL-CD2400/CD2401 Functional Block Diagram



FEATURES (cont.)

HDLC Features *(cont.):*

- Programmable number of leading flags

Asynchronous Operation Features:

- User-programmable and automatic flow control modes:
  - — In-Band (software) via XON, XOFF
  - — Out-of-Band (hardware) via RTS/CTS, DTR/DSR
  - — Line break detection and generation
  - — Special characters and character range recognition and transmission
  - — Transmit delay
- Special character range detection
- 5- to 8-bit character plus optional parity
- Enhanced features for UNIX® environment
  - — Character expansion in transmit; e.g., sending <LF> will be expanded to <CR> <LF> automatically
  - — Programmable translation of receiving character with error to different pattern; e.g., Char with parity can be translated to FFh, 00h, Char in the system side

Bisync Features:

- ASCII or EBCDIC encoding
- Special character recognition for block separation and BCC processing without host intervention (Transparent Bisync)
- LCR/VCR *or* CRC modes
- BCC is optionally readable

X.21 Features:

- Detection and validation of steady state conditions (e.g., 1, off)
- Stripping of repetitive receive conditions (e.g., BEL, off)
- Synchronization of transmit data characters and control leads
- Optional stripping of SYN characters
- Automatic transmission of repeated character pattern defined by user

DMA Controller Features:

- DMA *or* interrupt selectable per channel, per direction
- Duplicate configuration register sets to reduce real-time constraints
- Append and Block Mode DMA
- Chain/unchain of long frames into multiple buffers
- 32-bit address and 8- or 16-bit data transfer
- Programmable gap in buffers following an exception of a receive character

Other Features:

- Improved interrupt schemes:
  - — Vectored interrupts to allow direct jump into proper service routines
  - — Good Data Interrupts™ eliminate need for status checks
- Easily cascadable for multiple CL-CD2400 configurations
- Transmit and receive clock rates independently set using a divisor of system clock
- 16-byte receive and transmit FIFOs
- Local and remote maintenance loopback modes
- Programmable parity (odd, even, no and forced) and number of stop bits
- Byte-endian orientation selection pin, allowing easy interface to 80 x 86- and 680 x 0-processors
- System clock of up to 20 MHz
- 5 clock/modem control signals per channel on CD2400
- 8 clock/modem control signals on CD2401
- Packaged in an 84-pin PLCC for CD2400, 100-pin PQFP for CD2401
- Advanced, low-power CMOS process technology

Application Areas:

- Unix serial I/O
- Data Concentrators/Multiplexor
- Cluster Controllers
- Bridge/Gateway
- Multi-user computer
- Terminal Server
- X.21, X.25 and SS7

PIN DESCRIPTION (cont.)

Symbol	NUM	Type	Description
Microprocessor Interface *(cont.)*			
A/D(0–15)	16	I/O, 3-state	Address/Data (0–15) — when the CD240x is not a bus master these pins provide the 16 bit data bus for reading and writing to the CD240x registers. When ADLD* is low, A/D(0–15) provide the upper address bits A(16–31) for external latching. When the CD240x is a bus master, A/D (0–15) provide a data bus for reading and writing to system memory.
ADLD*	1	O, 3-state	Address Load* — is a strobe used to externally latch the upper portion of the system address bus A(8–31). While ADLD* is low, address bits 16 through 31 are available on A/D(0–15), and address bits 8 through 15 on A(0–7).
AEN*	1	O, 3-state	Address Enable* — this output is used to output enable the external address bus drivers during CD240x DMA cycles.
DATDIR*	1	O, 3-state	Data Direction* — this output is active when either the CD240x is a bus master or the CS* pin is low. It is used to control the external data buffers; when low, the buffers should be enabled in the CD240x to system bus direction.
DATEN*	1	O, 3-state	Data Enable* — this output is active when either the CD240x is a bus master or the CS* and AS* pins are low. It is used to enable the external data bus buffers during Host register read/write operations or during DMA operations. For operations on 32-bit buses, this signal needs to be gated with A(1) to select the correct half of the data bus.
CLK	1	I	Clock — system clock.
BUSCLK	1	O	Bus Clock — is the system clock divided by 2 and is used internally to control certain bus operations.
RESET*	1	I	Reset* — asynchronously resets the CD240x, should be active for a minimum of five clock periods. When RESET* is removed the CD240x performs a software initialization of its registers.
TEST	1	I	Test — this must be kept low at all times.
BYTESWAP	1	I	This pin alters the byte ordering of data during 16-bit transfers to comply with that used in Intel® or Motorola® processors. It does not alter the bus handshake signals. A different register map is used depending on the state of this pin.
Communications Interface			
RTS*(0–3)	4	O	Request to Send* (0–3).
TXCOUT/DTR*(0–3)	4	O	Transmit Clock OUT/Data Terminal Ready* (0–3) — user-selectable via the MSVR-DTR register.
CTS* (0–3)	4	I	Clear to Send* (0–3).
TXCIN/CD*(0–3)†	4	I	Transmit Clock IN/Carrier Detect* (0–3) — when used as transmit clock, the state of the pin is still available in the MSVR register.
RXCIN/DSR*(0–3)†	4	I	Receive Clock IN/Data Set Ready* (0–3) — when used as receive clock, the state of the pin is still available in the MSVR register.
TXD(0–3)	4	O	Transmit Data (0–3) — serial data output for each channel.
RXD(0–3)	4	I	Receive Data (0–3) — serial data input for each channel.
RXCOUT(0-3) ‡	4	I	Receive clock out (0-3) — clock output of the receive data sampling clock source.

† These two signals are de-multiplexed on the CD2401.
‡ These signals are only available in the CD2401.

GENERAL DESCRIPTION

The CL-CD2400/CD2401 is a four-channel sync/async communications controller featuring full on-chip DMA for each channel in each direction. Combining the DMA and protocol controllers provides a more efficient Host CPU interface by reducing Host CPU intervention and bus occupancy for both synchronous and asynchronous modes of operation.

The throughput and performance of the CD2400/CD2401 are further improved by the following features:

- Optimized firmware sequence for on-chip protocol handling
- Simultaneous use of multiple buffers
- Ability to add data space to existing buffers during DMA
- On-chip timers to keep track of real time events
- Efficient, Fair Share™ vectored interrupts

The CD2400/CD2401 can be interrupt- or DMA-driven and contains a powerful DMA buffer management scheme. There are eight DMA channels on-chip; one for each transmitter and one for each receiver. All necessary signals for DMA handshake are included in this product. Each DMA channel contains the starting address and byte count needed for buffer control.

The user may also optionally choose to have an interrupt generated each time a buffer is completed. In other words, after a buffer has been transmitted, or after a buffer has been received, the CD2400/CD2401 generates an appropriate interrupt.

The CD2400/CD2401 uses a simple, but powerful, double buffering method. Because of this, it is readily compatible with more complex buffer control procedures, such as circular queues, buffer pools, or any other. Each transmitter and each receiver is assigned an "A" buffer and a "B" buffer. When transmitting, the host processor will alternately fill the A and B buffers, and command the CD2400/CD2401 to transmit the buffers one at a time. When receiving, the CD2400/CD2401 will fill the A and B buffers, and inform the host processor when each is ready.

An ownership bit is used for each buffer to ensure that there are no conflicts between the host and the CD2400/CD2401 as to which is currently using a particular buffer.

To improve buffer utilization efficiency, a method of buffer chaining is available, which is useful to break large packets into smaller blocks.

By using the simple DMA management of the CD2400/CD2401, the user's host processor handles transmit and receive data on a block-by-block basis; the host does not need to be concerned with character-by-character transfers, or filling and emptying the FIFOs.

Extra Interface Pins Available on Each Channel in the CL-CD2401

Package	Interface Pins									
CD2400 (84-pin PLCC)	RxD	TxD	RTS	CTS	DSR/RxCin	DTR/TxCout	—	—	—	CD/TxCin
CD2401 (100 -pin PQFP)	RxD	TxD	RTS	CTS	DSR	DTR/TxCout	***RxCin***	***RxCin***	***RxCout***	CD

PIN DESCRIPTION

Symbol	NUM	Type	Description
Microprocessor Interface			
V_{cc}	2	I	Power Supply.
GND	4	I	Ground.
CS*	1	I	Chip Select* — when low the CD240x registers may be read or written by the host.
AS*	1	I/O, 3-state	Address Strobe* — input when CD240x is the slave. This signal is output when CD240x is the bus master indicating that R/W*, A(0–7) and A(8–31)@ are valid. @ see pin ADLD* for explanation
DS*	1	I/O, 3-state	Data Strobe* — when the CD240x is not a bus master, this is an input used to strobe data into registers during write cycles and enable data onto the bus during read cycles. When the CD240x is a bus master DS* is an output used to control data transfer to and from system memory.
R/W*	1	I/O, 3-state	Read/Write* — when the CD240x is not a bus master, this pin is an input that determines if a read or write operation is required when the CS* and DS* are active. When the CD240x is a bus master R/W* is an output and indicates a read or write to system memory.
DTACK*	1	I/O, open drain	Data Transfer Acknowledge* — when the CD240x is not a bus master, this is an output and indicates to the host when a read or write to the CD240x is complete. When BR* is driven low by the CD240x, DTACK* is an input that verifies system bus is no longer in use. When the CD240x is a bus master, DTACK* is an input that indicates when system memory read and write cycles are complete.
SIZ(0–1)	2	I/O, 3-state	SIZE(0–1) — when not the active bus master these are an inputs that determine the size of the operand being read or written by the host. When the CD240x is a bus master, these are outputs determining the size of the operand being transferred to or from system memory.
IACKIN*	1	I	Interrupt Acknowledge IN* — this input qualified with DS* and A(0–7), acknowledges CD240x interrupts.
IACKOUT*	1	O	Interrupt Acknowledge OUT* — this output is driven low during interrupt acknowledge cycles for which no internal interrupt is valid.
IREQ*(1–3)	3	I/O, open-drain	Interrupt Request* (1–3) — these outputs signal that the CD240x has a valid interrupt for modem lead activity [IREQ*(1)], transmit activity [IREQ*(2)], or receive activity [IREQ*(3)].
BR*	1	O, open-drain	Bus Request* — this output is used to signal to the host processor or bus arbiter that bus mastership is required by the CD240x.
BGIN*	1	I	Bus Grant IN* — this input indicates that the bus is available after the current bus master relinquishes the bus.
BGOUT*	1	O	Bus Grant OUT* — this output is asserted when BGIN* is low and no internal bus request has been made. A daisy chain scheme of bus arbitration can be formed by connecting BGOUT* to BGIN* of the next device in the chain. If a priority scheme is preferred, bus requests must be prioritized externally and bus grant routed to the BGIN* of the appropriate device.
BGACK*	1	I/O, open-drain	Bus Grant Acknowledge* — as an input this signal is used to determine if another bus master is in control of the bus. As an output, it signals to other bus masters that this device is in control of the bus.
BERR*	1	I	Bus Error* — if this input becomes active while the CD240x is a bus master, the current bus cycle will be terminated, the bus relinquished, and an interrupt generated to indicate the error to the Host processor.
A(0–7)	8	I/O, 3-state	Address (0–7) — when the CD240x is not a bus master these pins are inputs, used to determine which registers are being accessed, or which interrupt is being acknowledged. When ADLD* is low A(0–7) output address bits 8 through 15 for external latching. When the CD240x is a bus master, A(0–7) output the least significant byte of the transfer address.

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The Company

Cirrus Logic, Inc., is a leading supplier of high-integration peripheral controller circuits for mass storage, graphics, and data communications. The company also produces state-of-the-art software and firmware to complement its product lines. Cirrus Logic technology is used in leading-edge personal computers, engineering workstations, and office automation.

The Cirrus Logic formula combines proprietary S/LA™† IC design automation with system design expertise. The S/LA design system is a proven tool for developing high-performance logic circuits in half the time of most semiconductor companies. The results are better VLSI products, on-time, that help you win in the marketplace.

Cirrus Logic's extensive quality assurance program — one of the industry's most stringent — ensures the utmost in product reliability. Talk to our systems and applications specialists; see how you can benefit from a new kind of semiconductor company — Cirrus Logic.

† U.S. Patent No. 4,293,783

SMART COMM WITH DMA CHIP HANDLES MULTIPLE PROTOCOLS

EACH OF FOUR FULL-DUPLEX CHANNELS RECEIVES AND TRANSMITS AT UP TO 64-KBAUD WITH DIFFERENT PROTOCOLS.

MILT LEONARD

System performance in data communications equipment is finding it hard to keep pace with throughput demands imposed by increased serial-data line activity and greater networking capabilities. An insufficient number of serial channels, and little or no multiple protocol-handling and direct-memory-access (DMA) capability in available peripheral chips, creates a throughput bottleneck by thrusting these added responsibilities onto the host CPU.

A second-generation intelligent peripheral chip from Cirrus Logic promises to ease such bottlenecks. It supplies four full-duplex data channels and a menu of features that offload housekeeping chores from the host CPU.

The CD2400 intelligent multiprotocol peripheral (IMP) has the basic architecture of its forerunner, the CD180, which bowed last year. But where the CD180 has eight asynchronous data channels for use in terminal servers and data concentrators, the CD2400 has four channels, each with user-selectable protocols. It also has on-chip DMA for interfacing to various data-communication equipment from different vendors.

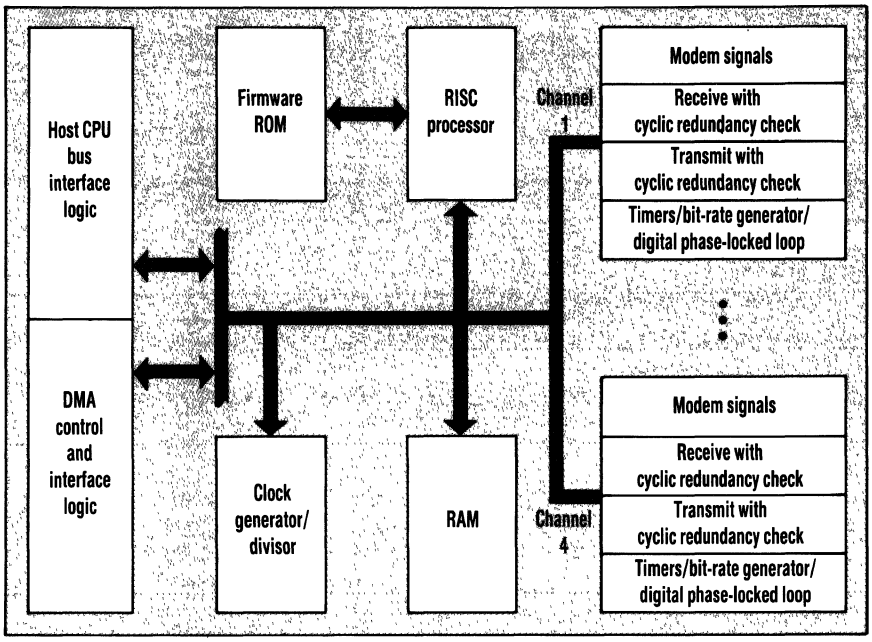
"By integrating several major control functions, the CD2400 can save significant board space," says Michael Leung, applications engineer at Cirrus Logic. "In a typical 8-channel slave serial-I/O board, for example, using two CD2400s to replace four dumb dual-channel serial controllers and two quad-channel DMA controllers reduces board area by 40 to 50%."

Four principal function blocks are integrated on the chip: a 10-MIPS reduced-instruction-set CPU with three buses, firmware ROM, RAM, and control and interface logic for the host microprocessor and DMA *(see the figure)*. On-chip protocol-handling is controlled by the firmware ROM.

The four replicated data channels, which interface to equipment external to the host, are implemented by modem I/O control logic and an I/O bit engine. Each channel has two independent timers for tracking real-time events and for reducing CPU overhead by releasing the system bus upon time-out. This feature also reduces the software design effort. Each channel also has a bit-rate generator for transmit and receive operations, a digital phase-locked loop on each receiver for extracting clock signals, and five clock and modem control lines. Transmit and receive clocks are set independently using a submultiple of the system clock, which can run at up to 20 MHz.

The CD2400 supplies four protocol options. Each channel can operate in a user-selectable synchronous, asynchronous, bisynchronous, or high-level data-link control (HDLC) mode. Asynchronous operation supplies vectored interrupts to make possible a direct jump into appropriate service routines. A proprietary feature called "good data interrupts" eliminates the need for status checks. It does so by using the on-chip CPU to monitor

MULTIPROTOCOL CONTROLLER



DRIVEN BY A RISC PROCESSOR, Cirrus Logic's CD2400 communications peripheral chip has four full-multiplexed channels, each of which can handle a different protocol. Modem control logic and bit-rate generators within each channel allow users to select the protocol and transmission rate desired.

the DMA controller and universal asynchronous receiver-transmitter (UART), to prevent unnecessary stoppage of the integrated DMA controller. Interrupts can be cascaded in applications using multiple CD2400s.

In the asynchronous mode, differences between terminal data rates are resolved by user-programmable and automatic data-flow control methods. These methods include in-band (software), out-of-band (hardware), line-break detection and generation, and special-character recognition and transmission. For example, operating with the multiplexer of a terminal server, multiple CD2400s can supply full-duplex data transfers between multiple low-speed serial lines of up to 64 kbits/s per channel, and a high-speed T1 multiplexed serial link (1.544 Mbits/s). Even higher frequencies than T1 are possible. Similar applications include use in the protocol converter of a LAN bridge or gateway, a T1 multiplexer, and a packet assembler/disassembler.

For synchronous operation, the chip offers programmable sync with frame-start/end and idle character modes, optional cyclic redundancy checking (CRC) and validation, and chaining or unchaining of long frames into multiple buffers. For communicating with equipment using the HDLC protocol, the CD2400 supplies address matching for four 8-bit or two 16-bit frames, frame-check-sequence generation and validation, and header-only (small frame) transmission and reception without DMA overhead.

For bisynchronous operation, ASCII or EBCDIC encoding is available. The chip also features special recognition for block separation and for CRC processing without host CPU intervention.

The IMP's DMA controller has a 32-bit address bus and a 16-bit multiplexed data bus. Each 16-bit data transfer takes two clock cycles (200 ns) for a 10-Mbyte/s transfer rate. DMA is supported by two 64-kbyte buffers per channel for transmit and receive operations. Header segregation eliminates DMA overhead during the reception or transmission of small HDLC frames. With handshaking, normal DMA operations can be interspersed with interrupts when special conditions or data errors occur. This isn't possible when the DMA and data-control functions are separated.

DMA efficiency is further optimized by a 16-byte-deep FIFO buffer for each channel per transmission direction. This feature reduces CPU response time during data reception and transmission, and minimizes the possibilities of FIFO buffer overruns and underruns. These capabilities enable one CD2400 to communicate with terminals having different serial-data protocols, such as a controller using the digital-data communications message protocol (DDCMP) of Digital Equipment Corp., an HDLC information-transfer controller, and an X.25 link-access protocol balanced (LAPB) controller.

Though the CD2400 has bus-timing and handshaking compatibility with Motorola microprocessors, a programmable pin is offered to select the byte-ordering convention of Motorola, Intel, and National Semiconductor processors. Control signals are also available to expand the 32-bit address for DMA.

Other IMP features are NRZ, NRZI, and Manchester data-encoding capabilities, local and remote maintenance loopback modes, a 5- to 8-bit character plus optional parity, and programmable parity and number of stop bits.

The CMOS chip is built using 2-μm design rules (1.5-μm L_{EFF}) and comes in an 84-pin plastic leaded chip carrier.□

PRICE AND AVAILABILITY

The CD2400 intelligent multiprotocol peripheral is housed in an 84-pin (J-lead) PLCC and costs $45 each in sample quantities. Production volumes are scheduled for the second quarter of 1990.

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