True Color VGA Family – CL-GD542X

Technical Reference Manual

January 1994

CL-GD542X Extended Video Modes Summary

Mode No.	VESA® No.	Colors	Display Resolution	Chars.	Refresh (Hz)
14	109	16/256K	1056 x 400	132 x 25	70
54	10A	16/256K	1056 x 350	132 x 43	70
55	109	16/256K	1056 x 350	132 x 25	70
58, 6A	102	16/256K	800 x 600	100 x 37	56, 60, 72
5C	103	256/256K	800 x 600	100 x 37	56, 60, 72
5D	104	16/256K	1024 x 768	128 x 48	87i, 60, 70, 72
5F	101	256/256K	640 x 480	80 x 30	60, 72
60	105	256/256K	1024 x 768	128 x 48	87i, 60, 70, 72
64	111	64K	640 x 480	–	60, 72
65	114	64K	800 x 600	–	56, 60
66	110	32K	640 x 480	–	60, 72
67	113	32K	800 x 600	–	56, 60
68	–	32K	1024 x 768	–	87i
6C	106	16/256K	1280 x 1024	160 x 64	87i
6D	–	256/256K	1280 x 1024	160 x 64	87i
71	112	16M	640 x 480	–	60
74	–	64K	1024 x 768	–	87i

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Revision History

Following are major changes between April1993 and January 1994 versions of this technical reference manual:

The CL-GD5429 was added to the True Color family and critical information pertaining to it provided.

Pin diagrams were added to Appendix A1.

The schematics in appendices B1, B2, and B3 were updated.

The technical information presented in B14 and D8 was updated.

Appendices B20, B21, and D9 were added.

Contents

Table of Contents

Section **Page**

Section **Page**

Section **Page**

APPENDICES

Introduction

1. INTRODUCTION

1.1 Scope of Document

This manual provides technical information for the CL-GD542X family of VGA controllers. This manual includes a description of each major component integrated into the chip, a data book, detailed information on each register, BIOS, and a number of application notes to assist hardware and software designers.

1.2 Applicable Chip Types

This manual documents chip Revision A or later.

The CL-GD542X ID Register — CR27, will read back a value indicating the chip-family member. Refer to Chapter 9, *Extension Register Descriptions*, for further information.

1.3 Intended Audience

This manual is intended for the technically sophisticated audience. It is assumed that the reader is familiar with assembly language programming on the 8088/8086, 80286/80386/80486, 80386SX, or similar microprocessor, and understands the fundamentals of video display technology.

Management personnel should find Chapter 2, *Overview*, useful.

Hardware engineers should find Chapter 3, *Data Book*, useful. It contains the pinouts and detailed pin descriptions, tables indicating how the various interfaces must be connected, and detailed DC and AC characteristics. In addition, the application notes in Appendix B should be helpful for board designs.

Software engineers should find Chapters 4-9 (register descriptions) useful for BIOS- and driver-level codes. All registers are described to the bit level. Also, the application notes in Appendices B-D should be helpful, especially those discussing the palette DAC and clock options, and programming methods.

1.4 Conventions

This section discusses conventions used throughout this document. Conventions include acronyms, abbreviations, and nomenclature usage. For a quick reference of acronyms see Table 1–2.

Bits

Bits are always listed in descending order, most-significant (highest number) to least-significant (lowest number). When discussing a bit field within a register or memory, the bit number of the most-significant bit is given on the left, followed by a colon (:) and then the bit number of the least-significant bit (e.g., bits 7:0). A field consists of a set of adjoining bits with common functionality. Registers are made up of fields of one or more bits.

Acronyms

Throughout this manual, the first usage of all acronyms has the definition following in parentheses. Table 1–2 lists acronyms common to this manual. For further definitions, refer to Appendix F1, *Glossary and Bibliography*.

Table 1–1 Acronym Quick Reference

Acronym	Definition
A.N.	Alpha Numeric
BIOS	Basic Input Output System
BPP	Bits Per Pixel
CGA	Color Graphics Adapter
CMOS	Complementary Metal-Oxide Semiconductor
EEPROM	Electrically Erasable/Programmable Read-Only Memory
EISA	Extended Industry Standard Architecture
FIFO	First-In/First-Out
I/O	Input/Output
LUT	LookUp Table
MSB	Most-Significant Bit
RAS	Row Address Strobe
R/W	Read/Write
TTL	Transistor-Transistor Logic
VGA	Video Graphics Array
VRAM	Video (Dynamic) Random Access Memory

Acronym	Definition
A.P.A.	All Points Addressable
BitBLT	Bit Boundary Block Transfer
CAS	Column Address Strobe
CLUT	Color Lookup Table
DRAM	Dynamic Random Access Memory
EGA	Enhanced Graphics Adapter
EPROM	Electrically Programmable Read-Only Memory
HSYNC/VSYNC	Horizontal/Vertical Synchronization
LSB	Least-Significant Bit
MD	Memory Data
RAM	Random Access Memory
RGB	Red, Green, Blue
SR logic	Set/Reset logic
VESA	Video Electronics Standards Association
VLUT	Video Lookup Table

Abbreviations

The unit 'K byte' designates 1024 bytes. The unit 'Mbyte' designates 1,048,576 bytes (1024 squared). The unit 'Gbytes' designates 1,000 megabytes. The unit 'Hz' designates hertz. The unit 'kHz' designates 1,000 hertz. The unit 'MHz' designates 1,000 kilohertz. The unit

'ns' designates nanosecond. The unit 'µs' designates microsecond (1,000 nanoseconds). The unit 'ms' designates millisecond (1,000 microseconds). The unit 'mA' designates milliampere. The use of 'tbd' in tables indicates values that are 'to be determined'. N/A designates 'not available'.

Numeric Naming

Hexadecimal numbers are represented with all letters in upper case and a lower-case 'h' is appended to them (e.g., '14h', '3A7h', and 'C000h' are hexadecimal numbers). Numbers not indicated by an 'h' are decimal. Octal numbers are not used in this manual.

Reserved

When a system memory or I/O address is referred to as 'Reserved', it means that writing to that address is not permitted. Reserved bits *must* be written as '0' to maintain upward compatibility.

Read-Only

The word 'Read-only' is used to indicate registers and bits that can be read, but not written to.

Logic States

In this manual, logic states are indicated in all capitals (e.g., Reset HIGH).

Overview

2. OVERVIEW

The True Color VGA family of VGA controllers supports high-resolution graphics and text display modes for a variety of color CRT monitors using industry-standard 15-pin analog video and VESA interfaces.

The CL-GD542X chips are hardware- and software-compatible with the IBM® VGA, and provide improved performance and additional functionality.

Highly integrated, these chips include a programmable dual-frequency synthesizer and palette DAC. A complete 512K motherboard solution can be implemented with a single DRAM.

The CL-GD542X implements all control and data registers in the standard VGA controller. It also implements all data manipulation capabilities and data paths in the standard VGA adapter.

2.1 Features

The following is a list of the major features of the CL-GD542X family of VGA controllers:

Table 2–1. CL-GD542X Family Features

Features	GD5420	GD5422	GD5424	GD5426	GD5428	GD5429
Performance						
VESA® VL-Bus and Direct '386 or '486 CPU Interface			✓	✓	✓	✓
BitBLT engine				✓	Enhanced	Memory-mapped I/O
Zero-wait-state operation	✓	✓	✓	✓	✓	✓
Maximum display memory	1 Mbyte	1 Mbyte	1 Mbyte	2 Mbytes	2 Mbytes	2 Mbytes
Display memory interface	16-bit	32-bit	32-bit	32-bit	32-bit	32-bit
Hardware cursor (in pixels)	up to 32 x 32	up to 64 x 64	up to 64 x 64	up to 64 x 64	up to 64 x 64	up to 64 x 64
Maximum Dot Clock frequency	75 MHz	80 MHz	80 MHz	80 MHz	80 MHz	86 MHz
Maximum MCLK frequency	50 MHz	50 MHz	50 MHz	50 MHz	50 MHz	60 MHz
High integration						
Integrated palette DAC and dual-frequency synthesizer	✓	✓	✓	✓	✓	✓
Motherboard VGA solution with only two ICs	✓	✓	✓	✓	✓	✓
Built-in port for VESA® passthrough feature connector	✓	✓	✓	✓	✓	✓

Table 2–1. CL-GD542X Family Features *(cont.)*

Features	GD5420	GD5422	GD5424	GD5426	GD5428	GD5429
Built-in ISA (up to 12.5 MHz), Microchannel® bus support	✓	✓	✓	✓	✓	✓
Flexibility						
Support for x4-, x8-, and x16-bit-wide memory DRAMs	✓	✓	✓	✓	✓	✓
8- or 16-bit host bus I/O and memory interface	✓	✓	✓	✓	✓	✓
8-bit gray and 3-3-2 RGB DAC modes					✓	✓
General						
100% hardware- and BIOS-compatible with IBM® VGA display standards	✓	✓	✓	✓	✓	✓
'Green PC' compliant	✓	✓	✓	✓	✓	✓
132-column text mode support	✓	✓	✓	✓	✓	✓
46E8 or 3C3 sleep mechanism		✓	✓	✓	✓	✓
Video Overlay and 'Color Key' support		✓	✓	✓	✓	✓
VESA® VAFC Base Support (for Video Overlay)						✓
Clocking support for CL-PX2080 MediaDAC™					✓	✓
Low-power CMOS, 160-pin package	✓	✓	✓	✓	✓	✓
Screen resolution and colors						
640 x 480	up to 256	up to 16M	up to 16M	up to 16M	up to 16M	up to 16M
800 x 600	up to 256	up to 64K	up to 64K	up to 64K	up to 64K	up to 64K
1024 x 768 (interlaced)	up to 256	up to 256	up to 256	up to 256	up to 64K	up to 64K
1024 x 768 (non-interlaced)	up to 256	up to 256	up to 256	up to 256	up to 256	up to 256
1280 x 1024 (interlaced)		up to 16	up to 16	up to 256	up to 256	up to 256

Table 2–2. Summary of Screen Resolutions

Resolutions	CL-GD5420	CL-GD5422	CL-GD5424	CL-GD5426/'28/'29
640 x 480 x 256 color, 8 bits/pixel	✓	✓	✓	✓
640 x 480 x 32K color, 16 bits/pixel		✓	✓	✓
640 x 480 x 64K color, 16 bits/pixel		✓	✓	✓
640 x 480 x 16M color, 24 bits/pixel		✓	✓	✓
800 x 600 x 16 color, 4 bit planes	✓	✓	✓	✓
800 x 600 x 256 color, 8 bits/pixel	✓	✓	✓	✓
800 x 600 x 32K color, 16 bits/pixel		✓	✓	✓
800 x 600 x 64K color, 16 bits/pixel		✓	✓	✓
1024 x 768 x 16 color, 4 bit planes (interlaced and non-interlaced)	✓	✓	✓	✓
1024 x 768 x 256 color, 8 bits/pixel (interlaced and non-interlaced)	✓	✓	✓	✓
1024 x 768 x 32K color, 16 bits/pixel (interlaced)				✓
1024 x 768 x 64K color, 16 bits/pixel (interlaced)				✓
1280 x 1024 x 16 color, 4 bit planes (interlaced)		✓	✓	✓
1280 x 1024 x 256 color, 8 bits/pixel (interlaced)				✓

2.2 Chip Architecture

The CL-GD542X includes all the hardware required to implement CPU updates to display memory, Screen Refresh, and DRAM Refresh. It interfaces directly with the host system or the local bus, the display memory, and the monitor. The host interface can be either 8-or 16-bits-wide for memory and I/O. The CL-GD542X requires no glue logic for address decoding and control logic handshaking.

The four major activities supported by the CL-GD542X are:

- **Host access to CL-GD542X registers**
- **Host access to display memory**
- **Display access to display memory (screen refresh)**
- **Display Memory Refresh**

2.2.1 Host Access to CL-GD542X Registers

The host (typically an ISA, Microchannel®, or '386 and '486 local bus) can access CL-GD542X registers by setting up 16- or 24-bit addresses and generating I/O control signals to read or write 8- or 16-bit data. Other activities, such as DRAM refresh, screen refresh, and delayed CPU writes to display memory can take place concurrently with accesses to registers.

The registers are listed in Chapter 3, *Data Book*, and described in Chapters 4 - 9. These registers include all the standard VGA registers, and are host-readable to allow BIOS and driver software to determine the state of the graphics adapter.

2.2.2 Host Access to Display Memory

The CL-GD542X handles the host access to display memory. The host effects memory accesses in the VGA address range to transfer data to or from one or more of the four display memory Planes. All of the required video handshake interface signals are internally generated by the CL-GD542X with no requirement for external logic decoding.

The CL-GD542X takes 24-bit addresses from the host, and transforms them according to the selected addressing mode and address space mappings, finally issuing multiplexed addresses to the planes via the MA[9:0] Address bus. RAS*, CAS*, OE*, and WE*[3:0] provide timing and control to the display memories. When interfacing to DRAMs that have dual-CAS* signals, the CAS* pin becomes WE*, and the WE*[3:0] pins become CAS*[3:0].

A Write Buffer is logically located at the CPU interface to isolate the CPU from the display memory. The CPU Write accesses to display memory take place immediately until the Write Buffer is full. The address and data are written into the cache, and the actual write into display memory occurs later. If the Write Buffer is full, wait states will be inserted until there is space.

2.2.3 Display Access to Display Memory

The CL-GD542X also contains an intelligent Address Sequencer that allocates display memory cycles not only to the host, but also to the display CRT Controller for screen refresh.

A FIFO logically between the Memory Sequencer and the Attribute Controller decouples the memory speed from the display speed, allowing the execution of Fast-page-mode accesses for screen refresh. This minimizes the memory bandwidth required.

The display is blanked during horizontal and vertical retrace intervals, freeing additional memory bandwidth for host access. The CL-GD542X improves on the performance of the IBM VGA implementation, especially for lower-resolution displays.

2.2.4 Display Memory Refresh

The CL-GD542X handles the refresh of the dynamic RAMs used for the display memory. During each horizontal blanking period, a selectable number of CAS*-before-RAS* refresh cycles are executed.

2.3 Major Components

The CL-GD542X incorporates all the major subsections of the IBM VGA/EGA into a single integrated circuit:

- **Sequencer**
- **CRT Controller**
- **Graphics Controller**
- **Attribute Controller**
- **Programmable Dual-Frequency Synthesizer**
- **Palette DAC**

In describing the CL-GD542X family of VGA controllers, it is useful to retain the identity of the original major subsections found in the IBM EGA and VGA controllers. The architectures of these major subsections are described on the following pages.

2.3.1 Sequencer

The Sequencer controls access to the display memory. It ensures that the necessary screen refresh and dynamic memory refresh cycles are executed, and that the remaining memory cycles are made available for CPU and BLT read/write operations.

The Sequencer consists of a memory arbitrator and a memory controller. It accepts requests from memory address counters associated with the CRTC, and address transformation logic associated with the Graphics Controller. It uses the Video FIFO to deliver data to the Attribute Controller, and the Write Buffer to transfer data to the Graphics Controller.

The Memory Sequencer Registers are described in Chapter 5.

The memory controller is driven by a memory clock (MCLK) optimized for the speed of the DRAM used, independent of the video clock. It generates the signals and addresses necessary for accessing the display memory. The memory arbitrator is also driven by the memory clock. It implements a policy that selects requests from either the CPU or the CRT on a dynamic priority.

2.3.2 CRT Controller

The CRT Controller generates the horizontal and vertical synchronization signals for the CRT display. It includes various registers that allow flexible configuration options. These options include user-configurable horizontal and vertical timing and polarity, cursor position, horizontal scanlines, and other display-related characteristics. The CRT Controller registers are described in Chapter 6.

The CRT Controller is equivalent to the IBM CRTC as implemented in the IBM VGA hardware. The CRT Controller also provides split screen capability and smooth scrolling. A simplified block diagram of the CRT Controller is shown in Figure 2–1.

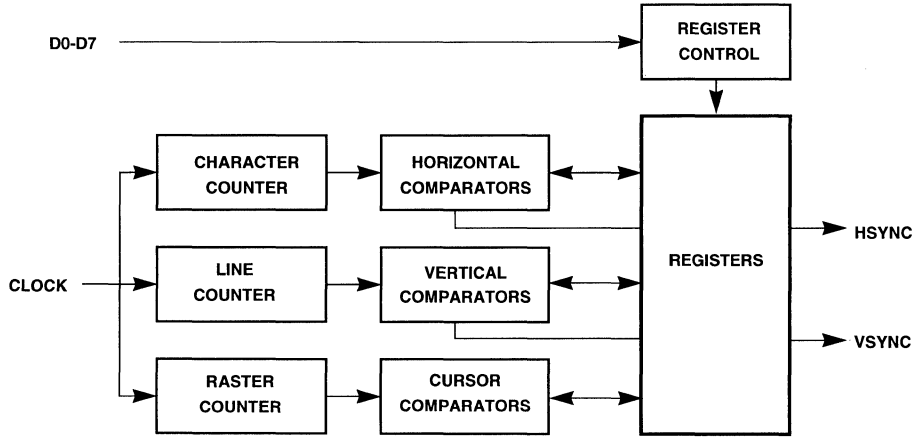

Figure 2–1. CRT Controller Functional Block Diagram

2.3.3 Graphics Controller

The Graphics Controller operates in either text or graphics modes and has the following major functions:

- **Provides the host CPU a read/write access path to display memory**
- **Controls all four memory planes**
- **Allows data to be manipulated prior to being written to display RAM**
- **Formats data for use in various backward compatibility modes**
- **Provides color comparators for use in color painting modes**
- **Reads/writes 32-bit words through the 32-bit display memory interface**
- **Combines display RAM data and attribute data for output to the Pixel bus**

The Graphics Controller directs data from the display memory to the Attribute Controller and to the CPU. Figures 2–2 and 2–3 illustrate typical write and read operations, respectively.

For a write operation, the data from the CPU bus are combined with the data from the Set/Reset Logic, depending on the Write mode. In addition, the data may be combined with the contents of the read latches, and some bits or planes may be masked (prevented from being changed). See the descriptions of the Graphics Controller registers in Chapter 7 for more information.

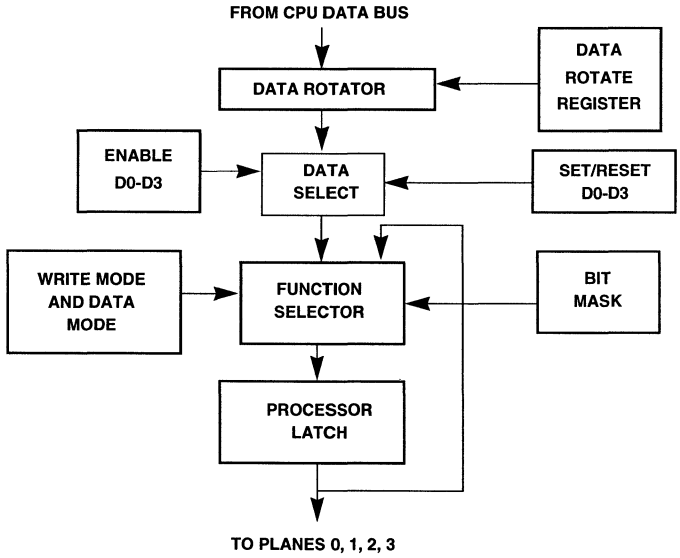

Figure 2–2. Graphics Controller Write Operation

The Graphics Controller is also involved when the CPU is reading data from display memory. Depending on the Read mode, the data returned may be the actual contents of the display memory, or it may reflect the outcome of comparisons with the color value in one of the Graphics Controller registers. See the descriptions of the Graphics Controller registers in Chapter 7 for more information.

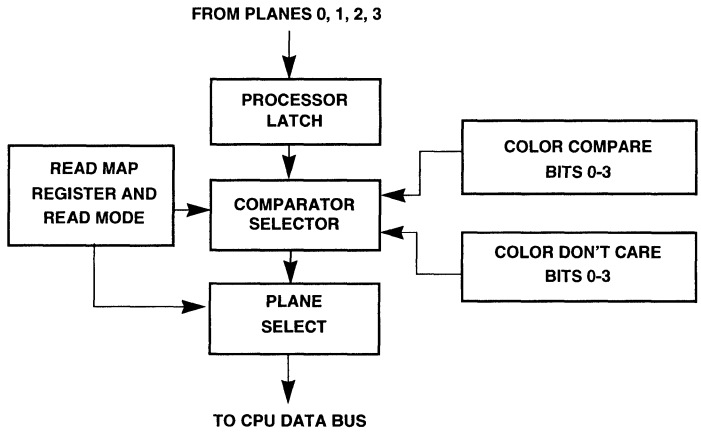

Figure 2–3. Graphics Controller Read Operation

2.3.4 Attribute Controller

The Attribute Controller controls blinking and underline operations in alphanumeric modes. It also provides the horizontal pixel panning capability in both alphanumeric and graphics modes. The Attribute Controller registers are described in Chapter 8. Figure 2–4 depicts the functional block diagram of the Attribute Controller.

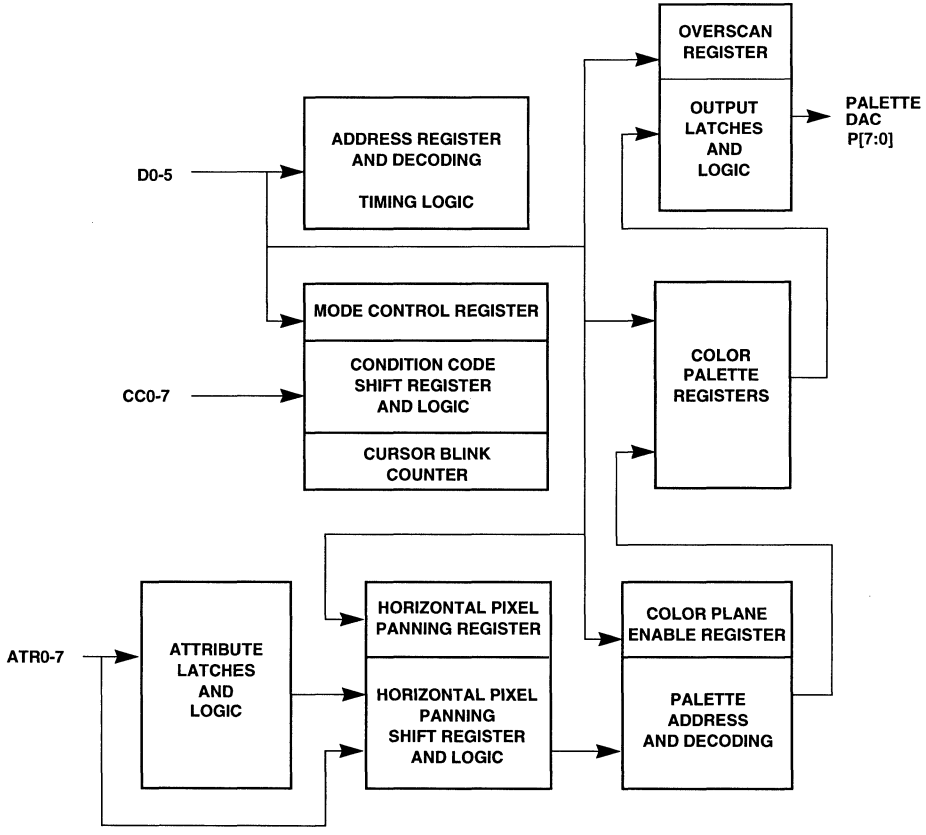

Figure 2–4. Attribute Controller Functional Block Diagram

2.3.5 Dual-Frequency Synthesizer

The CL-GD542X includes an integrated dual-frequency synthesizer that can be programmed to generate the VCLK for many standard screen formats, and the MCLK used by the Sequencer. The synthesizer requires a single-reference frequency of 14.31818 MHz that can be supplied by the on-chip oscillator, or can be injected from an external source.

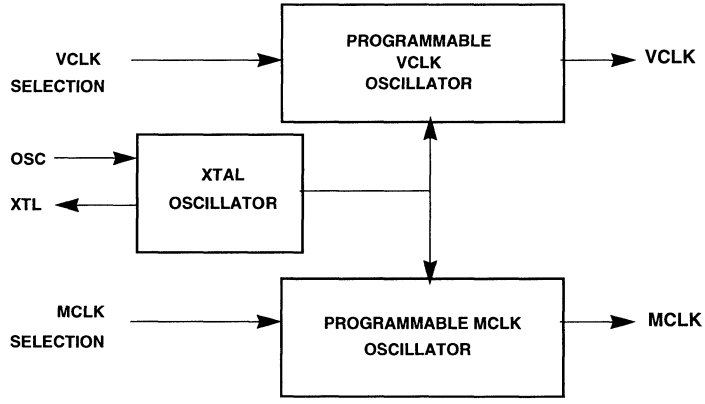

Figure 2–5. Programmable Dual-Frequency Synthesizer Functional Diagram

2.3.6 Palette DAC

The CL-GD542X includes an integrated palette DAC that can interface directly to the monitor connector via appropriate RFI filters. The palette DAC can be programmed for 256 simultaneous colors from a palette of 256K, or it can be programmed for Direct-color mode. In Direct-color mode, two or three contiguous bytes from the display memory are combined for each pixel. This allows 32K, 64K, or 16.8 million simultaneous colors on the screen. Figure 2–6 is a functional block diagram of the palette DAC.

The pixel bus, DCLK, and BLANK* can be driven into the CL-GD542X. This allows it to operate in the VESA-standard VGA Pass-through Connector mode. Fifteen- or sixteen-bit data can also be inserted from an external source through the P[7:0] pins. In addition to the VESA standard, the EVIDEO input is capable of switching at the pixel rate. The 24-bit data cannot be driven through this connector.

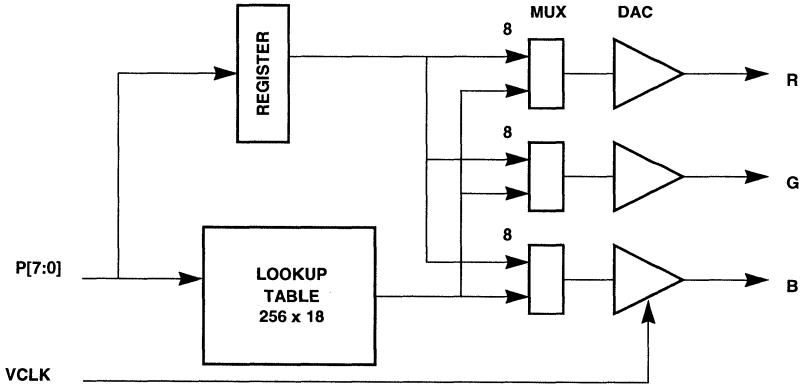

Figure 2–6. 256-Color Direct-Color Palette DAC

2.4 Hardware/Software Compatibility

The CL-GD542X includes all registers and data paths required for VGA controllers. Enhancements include 1024 x 768, 8-bit Pixel mode, an internal color palette, eight simultaneously loadable text fonts, Write mode 3, and readable registers.

Extended-resolution display modes are made possible by the high video clock rates and high display memory bandwidth.

Extended text and graphics resolutions beyond the 640 x 350 IBM EGA and 640 x 480 VGA standards are also supported by the Cirrus Logic BIOS on both fixed-frequency, PS/2™-compatible monitors as well as multiple-frequency monitors such as the NEC® MultiSync™. These include 132-column and 60-line text modes, 640 x 480 and 800 x 600 32,768 and 65,536-color graphics modes, 800 x 600 16-color VESA mode, and 640 x 480 16.8-million True Color mode. The extended-resolution capabilities of the CL-GD542X are listed in the Chapter 3, *Data Book*, along with the listing of the standard screen formats.

2.5 Video Subsystem Architecture

The following diagram shows the main components needed to implement a functional VGA subsystem using the CL-GD542X. The interfaces that must be implemented are the host CPU interface, the BIOS interface (for adapter board implementation only), the display memory interface, and the CRT interface.

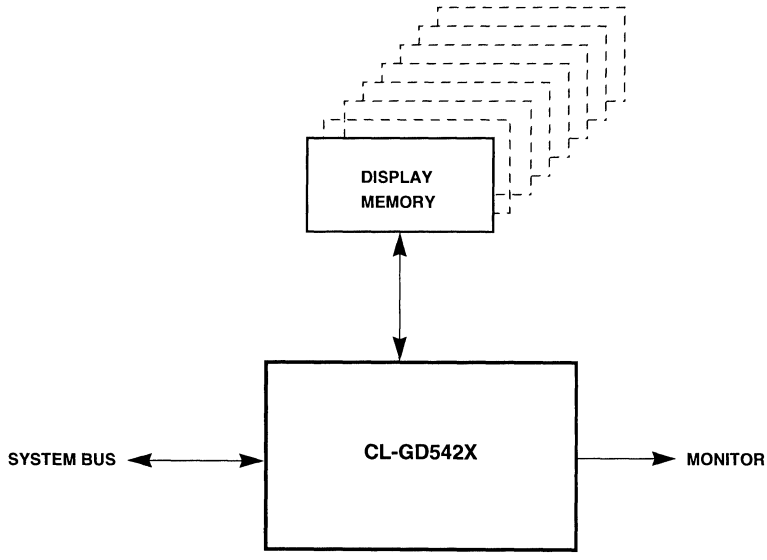

Figure 2–7. Video Subsystem Architecture

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Data Book

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CIRRUS LOGIC®

True Color VGA Family

Preliminary Data Book

FEATURES

- **32-bit GUI acceleration**
  - — Bit block transfer (BitBLT) engine
  - — Color expansion for 8- or 16-bit pixels
- **16/32-bit CPU interface**
  - — VESA® VL-Bus™ (up to 50 MHz)
  - — ISA bus (12.5 MHz)
  - — MicroChannel® bus
  - — Zero-wait-state write cycles
- **Resolutions up to 1280 x 1024**
  - — 1024 x 768 x 256 colors non-interlaced
  - — 800 x 600 x 64K colors non-interlaced
  - — 640 x 480 x 16M colors non-interlaced
  - — 1280 x 1024 x 256 colors interlaced
  - — 1024 x 768 x 64K colors interlaced
- **Programmable dual-clock synthesizer**
  - — Pixel clock programmable up to 86 MHz
  - — Memory clock programmable up to 60 MHz
- **Integrated 24-bit true-color RAMDAC**
- **'Green PC' power-saving features**
  - — VESA® Display Power Management Signal (DPMS)
  - — Internal DAC with programmable power-down mode
  - — Static monitor sync signals
- **Support for multimedia applications**
  - — 3-3-2 RGB DAC modes for video playback (CL-GD5428/'29)
  - — Support of VESA® VAFC Baseline for video overlay (CL-GD5429)
- **100% hardware- and BIOS-compatible with IBM® VGA display standards**

True Color VGA Family

CL-GD5429	– Memory-Mapped I/O VGA GUI Accelerator with Local Bus
CL-GD5428	– Enhanced VGA GUI Accelerator with Local Bus
CL-GD5426	– VGA GUI Accelerator with Local Bus
CL-GD5424	– Local Bus True Color VGA
CL-GD5422	– True Color VGA
CL-GD5420	– Super VGA

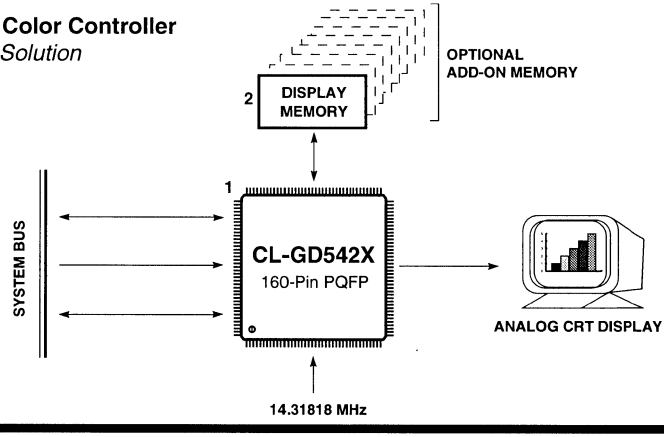
OVERVIEW

The CL-GD542X family of true-color VGA controllers offers an extensive range of industry-leading features and functionality for IBM®-compatible personal computers.

Ideally suited to highly integrated systems, CL-GD542X chips require no external support other than display memory and a 14.31818-MHz frequency reference. CL-GD542X chips are 100% hardware- and BIOS-compatible with IBM VGA standards, and connect directly to an ISA, MicroChannel®, or local bus, allowing a minimum adapter solution.

Operating at dot clock rates programmable up to 86 MHz, CL-GD542X chips support standard and VESA® high-resolution and extended modes. The internal palette DAC may be configured as an industry-standard RAMDAC to provide a palette of 256K colors, or true-color displays of 32K, 64K, and 16.8 million colors. *(cont.)*

Single-Chip True Color Controller
Two-Device VGA Solution



OVERVIEW (cont.)

The internal dual-frequency synthesizer requires a single crystal or reference for all supported screen resolutions, as well as all standard display memory speeds and formats. The CL-GD542X chips implement all control and data registers according to current VGA standards. They also implement all standard data path and manipulation functions, providing complete hardware compatibility.

In addition, the CL-GD542X chips support extended registers and capabilities to provide functional and performance enhancements beyond standard VGA.

CL-GD542X chips support ISA, MicroChannel, or 32-bit VL-Bus interfaces in all operations, including I/O and memory operations in planar modes. The write cycles to memory are optimized with zero-wait-state capability. Sixteen/thirty-two-bit local bus interfacing can be achieved for '386SX, '386DX, and '486 microprocessors as well as VESA VL-Bus. The CL-GD5426/'28/'29 also offer BitBLT operation for GUI acceleration.

The CL-GD542X family also includes many power-saving ('Green PC') features, including an internal DAC with programmable power-down mode, sync signals that can be individually disabled (static levels), and internal clocks programmable to low frequencies for nearly static operation.

Software Support

CL-GD542X VGA Software Drivers

Cirrus Logic provides a comprehensive range of software drivers to enhance the resolution and performance of many software packages.

Software Drivers	Resolution Supported[1]	Number of Colors
Microsoft® Windows v3.X	640 x 480, 800 x 600, 1024 x 768 640 x 480, 800 x 600, 1024 x 768 640 x 480	16 and 256 colors 65,536 colors 16.8 million colors
Microsoft® Windows NT v3.1	640 x 480, 800 x 600, 1024 x 768, 1280 x 1024	16 and 256 colors
OS/2® v2.0, v2.1	640 x 480, 800 x 600, 1024 x 768	16 and 256 colors[2]
AutoCAD® v11, v12	640 x 480, 800 x 600, 1024 x 768, 1280 x 1024 640 x 480, 800 x 600, 1024 x 768 640 x 480	16 and 256 colors 65,536 colors 16.8 million colors
Autoshade® v2.0 3D Studio® v1, v2	640 x 480, 800 x 600, 1024 x 768, 1280 x 1024 640 x 480, 800 x 600, 1024 x 768 640 x 480	256 colors 65,536 colors 16.8 million colors
GEM® v3.X Ventura Publisher™ v2, v3	800 x 600, 1024 x 768	16 colors
Lotus® 1-2-3™ v2.X Lotus® Symphony™ v2	132 x 25, 132 x 43 (text) 800 x 600	16 colors
Lotus® 1-2-3™ v3.3	800 x 600, 1024 x 768	16 colors
WordPerfect® v5.1	132 x 25, 132 x 43 (text) 800 x 600, 1024 x 768	16 colors
WordPerfect® v6.0	640 x 480, 800 x 600, 1024 x 768	16 and 256 colors
WordStar™ v5.5 – 7.0	800 x 600, 1024 x 768	16 colors
Microsoft® Word v5.X	132 x 25, 132 x 43 (text) 800 x 600, 1024 x 768	16 colors
MicroStation®	640 x 480, 800 x 600, 1024 x 768	16 and 256 colors

NOTES:

1) Not all monitors support all resolutions; 640 x 480 drivers will run on PS/2-type monitors. Extended resolutions are dependant upon monitor type and VGA system implementation.
2) OS/2 v2.0 requires a v2.0 Corrective Service Pack for 256 colors.

CL-GD542X Family Features

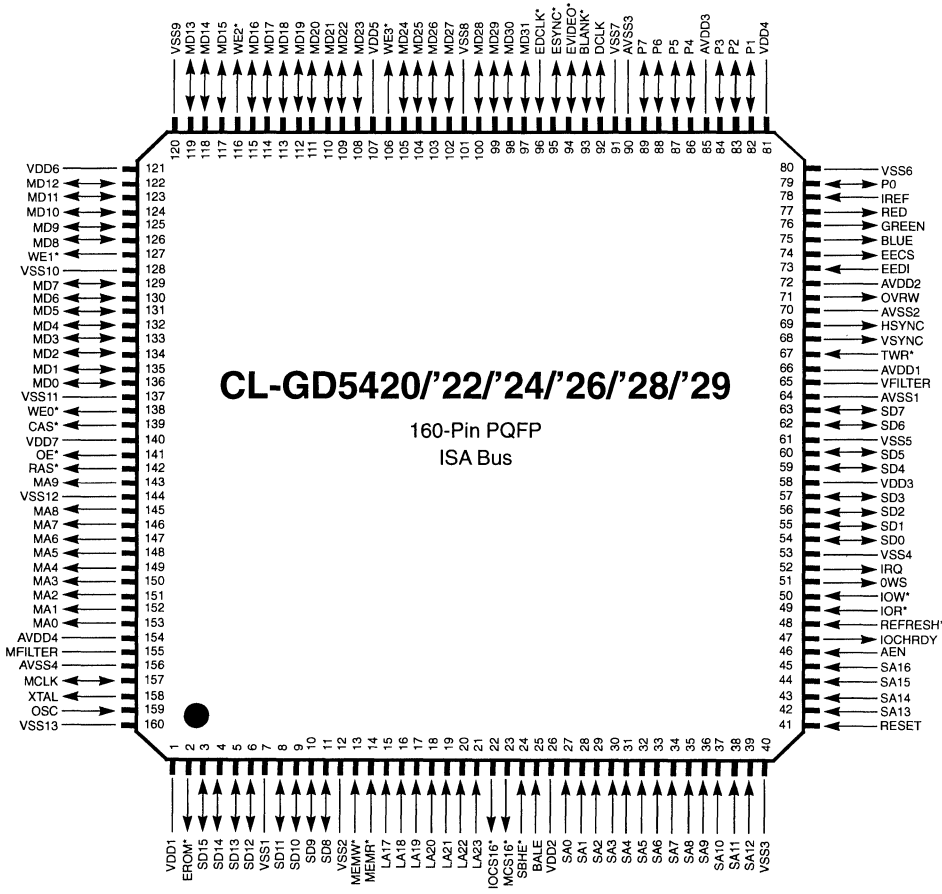
Features	CL-GD5420	CL-GD5422	CL-GD5424	CL-GD5426	CL-GD5428	CL-GD5429
Performance						
VESA® VL-Bus™ and direct '386 or '486 CPU interface			✓	✓	✓	✓
BitBLT engine				✓	Enhanced	Memory-mapped I/O
Zero-wait-state operation	✓	✓	✓	✓	✓	✓
Maximum display memory	1 Mbyte	1 Mbyte	1 Mbyte	2 Mbytes	2 Mbytes	2 Mbytes
Display memory interface	16-bit	32-bit	32-bit	32-bit	32-bit	32-bit
Hardware cursor (in pixels)	up to 32 x 32	up to 64 x 64	up to 64 x 64	up to 64 x 64	up to 64 x 64	up to 64 x 64
Maximum dot clock frequency	75 MHz	80 MHz	80 MHz	80 MHz	80 MHz	86 MHz
High Integration						
Integrated palette DAC and dual-frequency synthesizer	✓	✓	✓	✓	✓	✓
Motherboard VGA solution with only two ICs	✓	✓	✓	✓	✓	✓
Built-in port for VESA® passthrough feature connector	✓	✓	✓	✓	✓	✓
Built-in ISA (up to 12.5 MHz), MicroChannel® bus support	✓	✓	✓	✓	✓	✓
Flexibility						
Support for x4-, x8-, and x16-bit-wide memory	✓	✓	✓	✓	✓	✓
8- or 16-bit host bus I/O and memory interface	✓	✓	✓	✓	✓	✓
8-bit gray and 3-3-2 RGB DAC modes					✓	✓
General						
100% hardware- and BIOS-compatible with IBM® VGA display standards	✓	✓	✓	✓	✓	✓
'Green PC'-compliant	✓	✓	✓	✓	✓	✓
132-column text mode support	✓	✓	✓	✓	✓	✓
46E8 or 3C3 sleep mechanism		✓	✓	✓	✓	✓
Video overlay and color key support		✓	✓	✓	✓	✓
VESA® VAFC Baseline support (for video overlay)						✓
Support for CL-PX2080 MediaDAC™					✓	✓
Low-power CMOS, 160-pin PQFP package	✓	✓	✓	✓	✓	✓
Screen Resolution and Colors						
640 x 480	up to 256	up to 16.5M	up to 16.5M	up to 16.5M	up to 16.5M	up to 16.5M
800 x 600	up to 256	up to 64K	up to 64K	up to 64K	up to 64K	up to 64K
1024 x 768 (interlaced)	up to 256	up to 256	up to 256	up to 256	up to 64K	up to 64K
1024 x 768 (non-interlaced)	up to 256	up to 256	up to 256	up to 256	up to 256	up to 256
1280 x 1024 (interlaced)		up to 16	up to 16	up to 256	up to 256	up to 256

Table of Contents

1. PIN INFORMATION

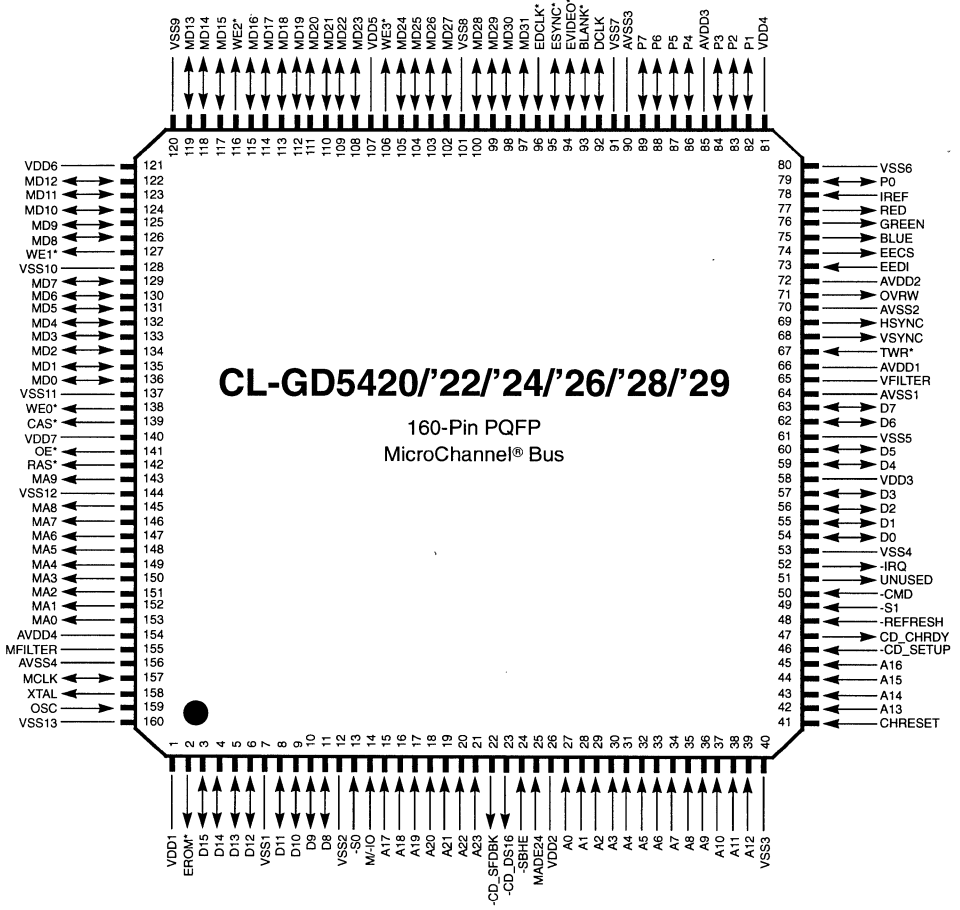
The CL-GD542X family of VGA controllers is available in a 160-pin quad flat pack device configuration, shown below.

1.1 Pin Diagram (ISA Bus)



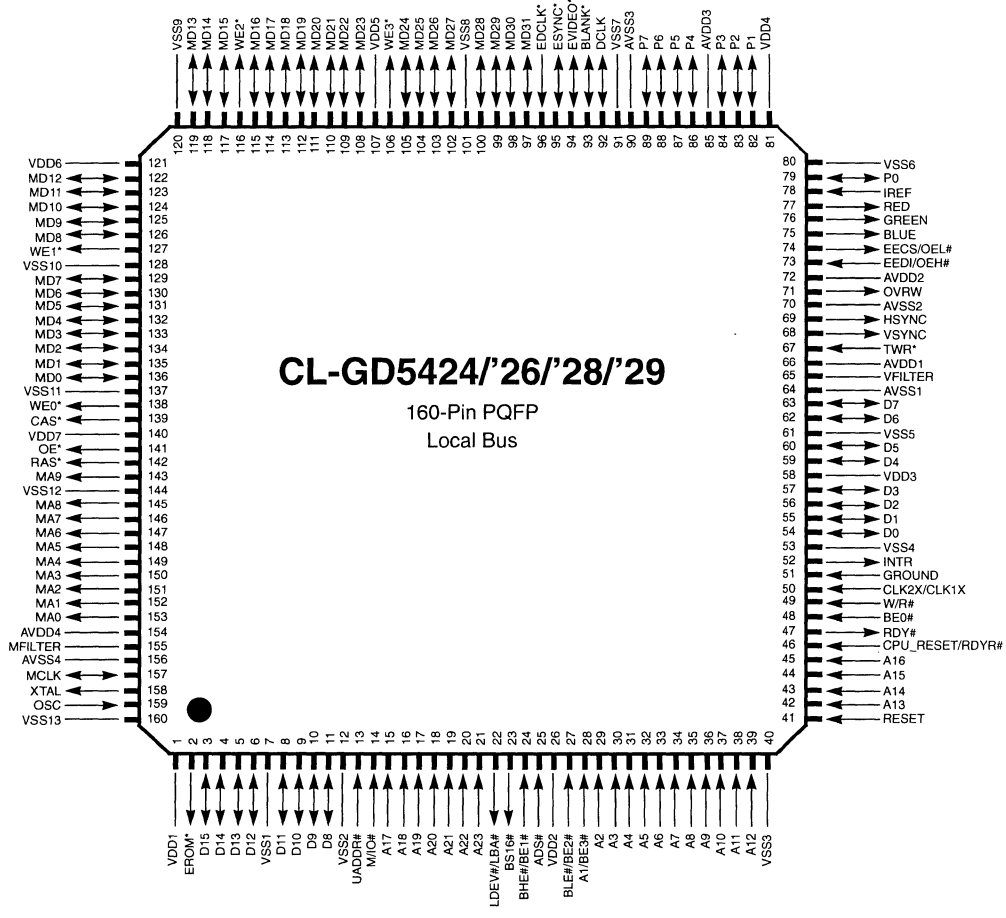
NOTE: WE1*, WE0*, MD[15:0], and OVRW are reserved on CL-GD5420.

1.2 Pin Diagram (MicroChannel® Bus)



NOTE: WE1*, WE0*, MD[15:0], and OVRW are reserved on CL-GD5420.

1.3 Pin Diagram (Local Bus)



1.4 Pin Summary

Table 1–1. Host Interface — ISA/MicroChannel®

Pin Number	Pin Type	Pull-up[a]	I_{OH}[b] (mA)	I_{OL}(mA)	Load (pF)	ISA	MicroChannel®
21	In	•				LA23	A23
20	In	•				LA22	A22
19	In	•				LA21	A21
18	In	•				LA20	A20
17	In	•				LA19	A19
16	In	•				LA18	A18
15	In	•				LA17	A17
45	In					SA16	A16
44	In					SA15	A15
43	In					SA14	A14
42	In					SA13	A13
39	In					SA12	A12
38	In					SA11	A11
37	In					SA10	A10
36	In					SA9	A9
35	In					SA8	A8
34	In					SA7	A7
33	In					SA6	A6
32	In					SA5	A5
31	In					SA4	A4
30	In					SA3	A3
29	In					SA2	A2
28	In					SA1	A1
27	In					SA0	A0
3	I/O	•	-3	12	240	SD15	D15
4	I/O	•	-3	12	240	SD14	D14
5	I/O	•	-3	12	240	SD13	D13
6	I/O	•	-3	12	240	SD12	D12
8	I/O	•	-3	12	240	SD11	D11
9	I/O	•	-3	12	240	SD10	D10
10	I/O	•	-3	12	240	SD9	D9
11	I/O	•	-3	12	240	SD8	D8
63	I/O		-3	12	240	SD7	D7
62	I/O		-3	12	240	SD6	D6
60	I/O		-3	12	240	SD5	D5
59	I/O		-3	12	240	SD4	D4
57	I/O		-3	12	240	SD3	D3
56	I/O		-3	12	240	SD2	D2
55	I/O		-3	12	240	SD1	D1
54	I/O		-3	12	240	SD0	D0
24	In	•				SBHE*	-SBHE

Table 1–1. Host Interface — ISA/MicroChannel® *(cont.)*

Pin Number	Pin Type	Pull-up[a]	I_{OH}[b] (mA)	I_{OL}(mA)	Load (pF)	ISA	MicroChannel®
25	In					BALE	MADE24
46	In					AEN	-CD_SETUP
49	In					IOR*	-S1
50	In					IOW*	-CMD
14	In					MEMR*	M/-IO
13	In					MEMW*	-S0
41	In	•				RESET	CHRESET
48	In					REFRESH*	-REFRESH
47	Out		-3	20	200	IOCHRDY	CD_CHRDY
22	Out		-3	20	200	IOCS16*	-CD_SFDBK
23	Out		-3	20	200	MCS16*	-CD_DS16
51	Out		(OC)	20	200	0WS	(unused)
52	Out		-3	20	200	IRQ	-IRQ

[a] • indicates the presence of a 250KΩ, ± 50 % pull-up resistor.

[b] Data pads nominally rated at -3 mA I_{OH} will sink -15 mA at V_{OH} = 2.0V.

Table 1–2. Host Interface — Local Bus (CL-GD5424/'26/'28/'29 only)

Pin Number	Pin Type	Pull-up[a]	I_{OH}[b] (mA)	I_{OL} (mA)	Load (pF)	'386SX	'386DX	'486	VESA® VL-Bus™
21	In	•				A23	A23	A23	A23
20	In	•				A22	A22	A22	A22
19	In	•				A21	A21	A21	A21
18	In	•				A20	A20	A20	A20
17	In	•				A19	A19	A19	A19
16	In	•				A18	A18	A18	A18
15	In	•				A17	A17	A17	A17
45	In					A16	A16	A16	A16
44	In					A15	A15	A15	A15
43	In					A14	A14	A14	A14
42	In					A13	A13	A13	A13
39	In					A12	A12	A12	A12
38	In					A11	A11	A11	A11
37	In					A10	A10	A10	A10
36	In					A9	A9	A9	A9
35	In					A8	A8	A8	A8
34	In					A7	A7	A7	A7
33	In					A6	A6	A6	A6
32	In					A5	A5	A5	A5
31	In					A4	A4	A4	A4
30	In					A3	A3	A3	A3

Table 1–2. Host Interface — Local Bus (CL-GD5424/'26/'28/'29 only) *(cont.)*

Pin Number	Pin Type	Pull-up[a]	I_{OH}[b] (mA)	I_{OL} (mA)	Load (pF)	'386SX	'386DX	'486	VESA® VL-Bus™
29	In					A2	A2	A2	A2
28	In					A1	BE3#	BE3#	BE3#
27	In					BLE#	BE2#	BE2#	BE2#
3	I/O	•	-3	12	240	D15	D15	D15	D15
4	I/O	•	-3	12	240	D14	D14	D14	D14
5	I/O	•	-3	12	240	D13	D13	D13	D13
6	I/O	•	-3	12	240	D12	D12	D12	D12
8	I/O	•	-3	12	240	D11	D11	D11	D11
9	I/O	•	-3	12	240	D10	D10	D10	D10
10	I/O	•	-3	12	240	D9	D9	D9	D9
11	I/O	•	-3	12	240	D8	D8	D8	D8
63	I/O		-3	12	240	D7	D7	D7	D7
62	I/O		-3	12	240	D6	D6	D6	D6
60	I/O		-3	12	240	D5	D5	D5	D5
59	I/O		-3	12	240	D4	D4	D4	D4
57	I/O		-3	12	240	D3	D3	D3	D3
56	I/O		-3	12	240	D2	D2	D2	D2
55	I/O		-3	12	240	D1	D1	D1	D1
54	I/O		-3	12	240	D0	D0	D0	D0
24	In	•				BHE#	BE1#	BE1#	BE1#
25	In					ADS#	ADS#	ADS#	LADS#
46	In					CPU-Reset	CPU-Reset	CPU-Reset	RDYRTN#
49	In					W/R#	W/R#	W/R#	W/R#
50	In					CLK2X	CLK2X	CLK1X	LCLK
14	In					M/IO#	M/IO#	M/IO#	M/IO#
13	In					(unused)	UADDR#	UADDR#	UADDR#
41	In	•				RESET	RESET	RESET	RESET
48	In					(unused)	BE0#	BE0#	BE0#
47	Out		-3	20	200	READY#	READY#	RDY#	RDY#
22	Out		-3	20	200	LBA#	LBA#	LBA#	LDEV#
23	Out		-3	20	200	(unused)	BS16#	BS16#	LDS16#
51	In		(OC)	20	200	GROUND	GROUND	GROUND	GROUND
52	Out		-3	20	200	INTR	INTR	INTR	INTR

[a] • indicates the presence of a 250KΩ, ± 50 % pull-up resistor.

[b] Data pads nominally rated at -3 mA I_{OH} will sink -15 mA at V_{OH} = 2.0V.

Table 1–3. Synthesizer Interface

Pin Number	Pin Type	Pull-up	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Name
159	In					OSC
158	Analog Out					XTAL
155	Analog					MFILTER
65	Analog					VFILTER
157	I/O		-12	12	20	MCLK

Table 1–4. Video Interface

Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Name
68	TS Out		-12	-12	50	VSYNC
69	TS Out		-12	-12	50	HSYNC
93	I/O		-12	12	50	BLANK*
89	I/O		-12	12	50	P7
88	I/O		-12	12	50	P6
87	I/O		-12	12	50	P5
86	I/O		-12	12	50	P4
84	I/O		-12	12	50	P3
83	I/O		-12	12	50	P2
82	I/O		-12	12	50	P1
79	I/O		-12	12	50	P0
92	I/O		-12	12	50	DCLK
95	I/O	•				ESYNC*
94	I/O	•				EVIDEO*
96	In	•				EDCLK*
77	Analog Out					RED
76	Analog Out					GREEN
75	Analog Out					BLUE
78	Analog In					IREF

[a] • indicates the presence of a 250KΩ, ± 50% pull-up resistor.

Table 1–5. Display Memory Interface

Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Name
142	Out		-8	12	50	RAS*
139	Out		-12	12	50	CAS*[b]
141	Out		-12	12	50	OE*[c]
106	Out		-12	12	50	WE3*[d]
116	Out		-12	12	50	WE2*
127	Out		-12	12	50	WE1*[e]
138	Out		-12	12	50	WE0*[e]
143	Out		-12	12	50	MA9
145	Out		-12	12	50	MA8
146	Out		-12	12	50	MA7
147	Out		-12	12	50	MA6
148	Out		-12	12	50	MA5
149	Out		-12	12	50	MA4
150	Out		-12	12	50	MA3
151	Out		-12	12	50	MA2
152	Out		-12	12	50	MA1
153	Out		-12	12	50	MA0
97	I/O	•	-12	12	50	MD31
98	I/O	•	-12	12	50	MD30
99	I/O	•	-12	12	50	MD29
100	I/O	•	-12	12	50	MD28
102	I/O	•	-12	12	50	MD27
103	I/O	•	-12	12	50	MD26
104	I/O	•	-12	12	50	MD25
105	I/O	•	-12	12	50	MD24
108	I/O	•	-12	12	50	MD23
109	I/O	•	-12	12	50	MD22
110	I/O	•	-12	12	50	MD21
111	I/O	•	-12	12	50	MD20
112	I/O	•	-12	12	50	MD19
113	I/O	•	-12	12	50	MD18
114	I/O	•	-12	12	50	MD17
115	I/O	•	-12	12	50	MD16
117	I/O	•	-12	12	50	MD15[e]
118	I/O	•	-12	12	50	MD14[e]
119	I/O	•	-12	12	50	MD13[e]
122	I/O	•	-12	12	50	MD12[e]
123	I/O	•	-12	12	50	MD11[e]
124	I/O	•	-12	12	50	MD10[e]
125	I/O	•	-12	12	50	MD9[e]
126	I/O	•	-12	12	50	MD8[e]

Table 1–5. Display Memory Interface *(cont.)*

Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Name
129	I/O	•	-12	12	50	MD7[e]
130	I/O	•	-12	12	50	MD6[e]
131	I/O	•	-12	12	50	MD5[e]
132	I/O	•	-12	12	50	MD4[e]
133	I/O	•	-12	12	50	MD3[e]
134	I/O	•	-12	12	50	MD2[e]
135	I/O	•	-12	12	50	MD1[e]
136	I/O	•	-12	12	50	MD0[e]

[a] • indicates the presence of a 250KΩ, ± 50 % pull-up resistor.

[b] CAS* is redefined as WE* for multiple-CAS* 256K x 16 DRAMs for CL-GD5422/'24/'26/'28/'29.

[c] OE* is redefined as RAS1* for 2-Mbyte display memory configurations for CL-GD5426/'28/'29 only.

[d] WE*[3:0] are redefined as CAS*[3:0] for multiple-CAS* 256K x 16 DRAMs for CL-GD5422/'24/'26/'28/'29.

[e] WE1*, WE0, MD[15:0] are reserved on CL-GD5420.

Table 1–6. Miscellaneous Pins

Pin Number	Pin Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Name
74	Out		-12	12	35	EECS[b]
73	In					EEDI[c]
2	Out		-12	12	35	EROM*
71	Out		-12	12	35	OVRW[d]
67	In					TWR*

[a] • indicates the presence of a 250KΩ, ± 50 % pull-up resistor.

[b] EECS is redefined as OEL# when the CL-GD5424/'26/'28/'29 (only) is configured for '486, VESA VL-Bus, or local bus operation.

[c] EEDI is redefined as OEH# when the CL-GD5424/'26/'28/'29 (only) is configured for '486, VESA VL-Bus, or local bus operation.

[d] OVRW is reserved on CL-GD5420.

Table 1–7. Power and Ground

Pin Number	Pin Type	Pull-up	I_{OH}	I_{OL}	Load (pF)	Name	Note
140	Power					VDD7	Digital
121	Power					VDD6	Digital
107	Power					VDD5	Digital
81	Power					VDD4	Digital
58	Power					VDD3	Digital
26	Power					VDD2	Digital
1	Power					VDD1	Digital
160	Ground					VSS13	Digital
144	Ground					VSS12	Digital
137	Ground					VSS11	Digital
128	Ground					VSS10	Digital
120	Ground					VSS9	Digital
101	Ground					VSS8	Digital
91	Ground					VSS7	Digital
80	Ground					VSS6	Digital
61	Ground					VSS5	Digital
53	Ground					VSS4	Digital
40	Ground					VSS3	Digital
12	Ground					VSS2	Digital
7	Ground					VSS1	Digital
66	Power					AVDD1	VCLK
64	Ground					AVSS1	VCLK
154	Power					AVDD4	MCLK
156	Ground					AVSS4	MCLK
85	Power					AVDD3	DAC
72	Power					AVDD2	DAC
90	Ground					AVSS3	DAC
70	Ground					AVSS2	DAC

2. DETAILED PIN DESCRIPTIONS

The following abbreviations are used for pin types in the following sections: (I) indicates input; (O) indicates output; (TS) indicates three-state; (OC) indicates open collector.

2.1 Host Interface — ISA Bus Mode

Name	Type	Description
LA[23:17]	I	**ADDRESS [23:17]:** These inputs, in conjunction with SA[16:0], are used to select the resource to be accessed during memory operations. These address bits are latched with the falling edge of BALE.
SA[16:0]	I	**ADDRESS [16:0]:** These inputs, in conjunction with LA[23:17], are used to select the resource to be accessed during any memory or I/O operation. These address bits must remain valid throughout the cycle.
SD[15:8]	TS	**SYSTEM DATA [15:8]:** These bi-directional pins are used to transfer data during 16-bit memory or I/O operations. These pins may be connected directly to the corresponding ISA Bus pins. These pads have pull-up resistors to guarantee a valid input level when not connected.
SD[7:0]	TS	**SYSTEM DATA [7:0]:** These bi-directional pins are used to transfer data during any memory or I/O operation. These pins may be connected directly to the corresponding ISA Bus pins.
SBHE*	I	**SYSTEM BYTE HIGH ENABLE:** This input is used in conjunction with A[0] to determine the width and alignment of a data transfer. SBHE* and A[0] are decoded as shown in the following Table 2–1:
BALE	I	**BUS ADDRESS LATCH ENABLE:** This active-HIGH input is used to latch LA[23:17] on the HIGH-to-LOW transition.
AEN	I	**ADDRESS ENABLE:** If this input is high, it indicates that the current cycle is a DMA cycle. In this case, the CL-GD542X will not respond to I/O cycles. There is no effect on memory cycles.

Table 2–1. SBHE/A0 Decoding

SBHE*	A0	Function
0	0	16-bit Transfer
0	1	Upper-byte Transfer
1	0	Lower-byte Transfer
1	1	Lower-byte Transfer *(on odd address)*

2.1 Host Interface — ISA Bus Mode *(cont.)*

Name	Type	Description
IOR*	I	**I/O READ:** This active-LOW input is used to indicate that an I/O read is occurring. If the address on SA[15:0] is within the range of the CL-GD542X, it will respond by placing the contents of the appropriate register on the System Data bus.
IOW*	I	**I/O WRITE:** This active-LOW input is used to indicate that an I/O write is occurring. If the address on SA[15:0] is within the range of the CL-GD542X, it will respond by transferring the contents of the System Data bus into the appropriate register. The transfer will occur on the trailing (rising) edge of this signal. A list of I/O addresses to which the CL-GD542X will respond appears in Section 5. When a 16-bit I/O write is done, the address specified is typically the Index register for one of the VGA groups. The index should appear on SD[7:0] and the data should appear on SD[15:8].
MEMR*	I	**MEMORY READ:** This active-LOW input is used to indicate that a memory read is occurring. If linear addressing is being used, this pin must be connected to ISA Signal MEMR*. If linear addressing is not being used, this pin must be connected to ISA Signal SMEMR*. The CL-GD542X decodes A[23:15] to determine if a display memory read is occurring. If so, data is placed on the System Data pins according to the read mode and the contents of display memory. The CL-GD542X decodes A[23:15] to determine if a BIOS read is occurring. If so, the CL-GD542X makes EROM* active for the duration of MEMR*.
MEMW*	I	**MEMORY WRITE:** This active-LOW input is used to indicate that a memory write is occurring. If linear addressing is being used, this pin must be connected to ISA Signal MEMW*. If linear addressing is not being used, this pin must be connected to ISA Signal SMEMW*. The CL-GD542X decodes A[23:15] to determine if a display memory write is occurring. If so, data is written into display memory according to the write mode and the data on SD[15:0]. The data are latched in the CL-GD542X on the rising edge of this signal, and are actually transferred to display memory later.
RESET	I	**RESET:** This active-HIGH signal is used to initialize the CL-GD542X to a known state. The trailing (falling) edge of this input loads the Configuration register CF[14:0] with the data on MD[30:16], determined by internal pull-up resistors and optional external pull-down resistors.
REFRESH*	I	**REFRESH*:** This active-LOW signal indicates that a DRAM refresh is occurring. The CL-GD542X ignores memory read operations occurring when REFRESH* is active since it controls the refresh of display memory.

2.1 Host Interface — ISA Bus Mode *(cont.)*

Name	Type	Description
IOCHRDY	TS	**I/O CHANNEL READY:** This output, when driven LOW, indicates that additional wait states are to be inserted into the current display memory read or write cycle. This output is never driven LOW during I/O cycles or BIOS reads. During a display memory read cycle, this signal is always driven LOW as soon as MEMR* goes active. When the data are ready to be placed on the System Data bus, this signal is driven HIGH. It remains high until MEMR* goes inactive; it then goes high impedance. During a display memory write cycle, this signal is driven HIGH as soon as MEMW* goes active if there is space in the Write Buffer. If there is no space in the Write Buffer, this signal is driven LOW as soon as MEMW* goes active and remains LOW until there is space. Once there is space in the Write Buffer, this signal is driven HIGH. It will remain high until MEMW* goes inactive; it then goes high impedance.
IOCS16*	OC	**I/O CHIP SELECT 16*:** This open-collector output is driven LOW to indicate that the CL-GD542X can execute an I/O operation at the address currently on the bus in 16-bit mode. This signal is generated from a decode of A[15:0] and AEN. Table 2–2 indicates the range of addresses for which the CL-GD542X will generate IOCS16*:

Table 2–2. IOCS16* Addresses

Address	Function
3C4, 3C5	Sequencer
3CE, 3CF	Graphics Controller
3B4/3D4, 3B5/3D5	CRT Controller
3BA/3DA	Input Status register 1

2.1 Host Interface — ISA Bus Mode *(cont.)*

Name	Type	Description
MCS16*	OC	**MEMORY CHIP SELECT 16*:** This open-collector output is driven LOW to indicate that the CL-GD542X can execute a memory operation at the address currently on the bus in 16-bit mode. Table 2–3 summarizes the conditions under which MCS16* is made active.

Table 2–3. MSC16* Addresses

Resource	Address Bits	Address Range	Qualifier
Display memory	A[23:17]	A000:0-BFFF:F	SR8[6] = 1 (No other VGA card)
Display memory	A[23:17]	1 Mbyte	SR7[7:4] $\neq$ 0 Linear Addressing
BIOS	A[23:15]	C000:0-C7FF:F	CF[6] = 0 (16-bit BIOS)

NOTE: The SA bits are generated late enough to typically make them unusable for generating MCS16*. The CL-GD542X uses a fast path from SA[16:15] to MCS16*.

0WS* OC **ZERO WAIT STATE*:** This open-collector output is driven LOW to indicate that the current cycle can be completed without any additional wait states. The circumstances under which 0WS* will be made active are summarized in the following Table 2–4:

Table 2–4. Zero Wait State* Cycles

Cycle Type	Qualifier
Display Memory Write	Write Buffer not full
BIOS Read	CF[1] = 0 (not on CL-GD5429)

IRQ TS **INTERRUPT REQUEST:** This active-HIGH output indicates the CL-GD542X has reached the end of an active field. Specifically, the transition occurs at the beginning of the bottom border. This pin is typically unused in PC/AT add-in cards, but may be connected to IRQ2/IRQ9 via a jumper block. See register CR11 for a description of the controls for this pin.

2.2 Host Interface — MicroChannel® Bus Mode

Name	Type	Description
A[23:0]	I	**ADDRESS [23:0]:** These inputs are used to select the resource to be accessed during memory or I/O operation. These address bits are latched with the falling edge of -CMD. A[23:17] have internal pull-ups, whereas A[16:0] do not.
D[15:0]	TS	**DATA [15:0]:** These bi-directional pins are used to transfer data during memory or I/O operation. These pins may be connected directly to the corresponding MicroChannel bus pins.
-SBHE	I	**-SYSTEM BYTE HIGH ENABLE:** This input is used in conjunction with A[0] to determine the width and alignment of a data transfer. This signal is latched with -CMD low. This pad has a pull-up resistor SBHE and A[0] are decoded as shown in Table 2–5:
MADE24	I	**MEMORY ADDRESS ENABLE 24:** This active-HIGH input is latched the falling edge of -CMD. It indicates that the address is in the lower 16 Mbytes of address space. It must be HIGH for the CL-GD542X to participate in a memory cycle.
-CD_SETUP	I	**CARD SETUP:** When this active-LOW input is active, the CL-GD542X is placed in Setup mode. In Setup mode, the CL-GD542X will respond only to POS102 accesses. It will not respond to any other I/O accesses or to display memory accesses. It will respond to BIOS reads. This signal is latched with the falling edge of -CMD.

Table 2–5. -SBHE/A0 Decoding

-SBHE	A0	Function
0	0	16-bit Transfer
0	1	Upper-byte Transfer
1	0	Lower-byte Transfer
1	1	Lower-byte Transfer *(on odd address)*

2.2 Host Interface — MicroChannel® Bus Mode *(cont.)*

Name	Type	Description
-S1	I	**-STATUS 1:** This signal, in conjunction with -S0 and M/-IO, is used to determine the cycle type that occurs. The encoding is shown in the following Table 2–6:
-CMD	I	**-COMMAND:** The falling edge of this input is used to latch the address bus, MADE24, -SBHE, -REFRESH, M/-IO, -CD_SETUP, -S0, and -S1. It is also used to time the actual data transfer. During I/O or memory-read cycles, the CL-GD542X drives valid data onto the bus prior to the trailing edge of this signal. During write cycles, the CL-GD542X expects valid data while this input is active and latches the data at the trailing edge.
M/-IO	I	**MEMORY/-IO:** This signal, in conjunction with -S0 and -S1, is decoded to determine the cycle type. See the description of -S1.
-S0	I	**-STATUS 0:** This signal, in conjunction with -S1 and M/-IO is decoded to determine the cycle type. See the description of -S1.
RESET	I	**RESET:** This active-HIGH signal is used to initialize the CL-GD542X to a known state. The trailing (falling) edge of this input loads the Configuration register CF[14:0] with the data on MD[30:16], determined by internal pull-up resistors and optional external pull-down resistors.

Table 2–6. MicroChannel® Cycle Type Encoding

M/-IO	-S0	-S1	Cycle
0	0	0	Reserved
0	0	1	I/O Write
0	1	0	I/O Read
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Memory Write
1	1	0	Memory Read
1	1	1	Reserved

2.2 Host Interface — MicroChannel® Bus Mode *(cont.)*

Name	Type	Description
-REFRESH	I	**-REFRESH:** This active-LOW signal indicates that a DRAM refresh is occurring. This signal is latched with -CMD low. The CL-GD542X ignores memory-read operations occurring when REFRESH is active since it controls the refresh of display memory.
CD_CHRDY	O	**CARD CHANNEL READY:** This output is driven LOW to request that additional wait states be inserted into the current display memory read or write cycle. This output is never driven LOW during I/O cycles or BIOS reads. During a display memory read cycle, this signal is always driven LOW as soon as -S1 goes LOW. When the data are ready to be placed on the System Data bus, this signal is driven HIGH. During a display memory write cycle, this signal is driven HIGH as soon as -S0 goes LOW if there is space in the Write Buffer. If there is no space in the Write Buffer, this signal is driven LOW as soon as -S0 goes LOW and remains LOW until there is space. Once there is space in the Write Buffer, this signal is driven HIGH.
-CD_SFDBK	OC	**-CARD SELECTED FEEDBACK:** This open-collector output is driven LOW to indicate that the CL-GD542X can respond to the addresses currently on the bus. This signal is generated from a decode of -REFRESH, MADE24, A[23:0], and M/-IO. This signal is made active for the Address Range C000:0-C7FF:F only if CF[6] = 0 (indicating a 16-bit BIOS). If CF[6] = 1, this signal will not be made active for Address Range C000:0-C7FF:F. Also, this signal will not be made active for Addresses 102 or 103 if M/-IO is LOW, which indicates I/O.
-CD_DS16	OC	**-CARD SIZE 16:** This open-collector output is driven LOW to indicate that the CL-GD542X can execute a memory or I/O operation at the address currently on the bus in 16-bit mode. This output is generated from a decode of A[23:0], MADE24, -REFRESH, and M/-IO. Table 2–7 summarizes the conditions under which -CD_DS16 is made active.

Table 2–7. -CD-DS16 Addresses

Resource	Address Bits	Address Range
Display memory	A[23:15]	A000:0-BFFF:F
Display memory	A[23:15]	1 Mbyte
BIOS (CF[6] = 0 only)	A[23:11]	C000:0-C7FF:F
I/O	A[15:1]	3C4, 3C5 3CE, 3CF 3B/D4, 3B/D5 3B/DA

2.2 Host Interface — MicroChannel® Bus Mode *(cont.)*

Name	Type	Description
-IRQ	OC	**-INTERRUPT REQUEST:** This open-collector output indicates the CL-GD542X has reached the end of an active field. Specifically, the transition occurs at the beginning of the bottom border. This pin is typically connected to IRQ9 via a jumper block. See register CR11 for a description of the controls for this pin. This pin is never driven HIGH.

2.3 Host Interface — Local Bus (CL-GD5424/'26/'28/'29 only)

A number of bus interface pins are redefined according to the local bus type to which the CL-GD5424/'26/'28/'29 is connected. These are listed in Table 2–8, which is ordered by CL-GD5424/'26/'28/'29 pin number.

Table 2–8. Redefined Host Interface Pins

Pin	'386SX	'386DX	'486	VESA® VL-Bus™
13	(unused)	UADDR#	UADDR#	UADDR#
23	(unused)	BS16#	BS16#	LBS16#
24	BHE#	BE1#	BE1#	BE1#
27	BLE#	BE2#	BE2#	BE2#
28	A1	BE3#	BE3#	BE3#
46	CPU-RESET	CPU-RESET	GND	RDYRTN#
47	READY#	READY#	BRDY#	BRDY#
48	(unused)	BE0#	BE0#	BE0#
50	CLK2X	CLK2X	CLK1X	LCLK
51	GROUND	GROUND	GROUND	GROUND
73	(unused)	(unused)	OEH#	OEH#
74	(unused)	(unused)	OEL#	OEL#

Name	Type	Description
A[23:2]	I	**ADDRESS [23:2]:** These inputs are used to select the resource to be accessed during memory or I/O operations. A[23:17] have internal pull-ups; A[16:2] do not. A[3:2] are burst address bits for the '486.
D[15:0]	TS	**DATA [15:0]:** These bi-directional pins are used to transfer data during any memory or I/O operation. These pins are directly connected to D[15:0] of the '386SX or '386DX bus. These pins are connected via four bi-directional data transceivers to the 32 data pins of the '486 or VESA VL-Bus. The transceivers are controlled with OEH#, OEL#, and W/R#. These pads have pull-up resistors.

2.3 Host Interface — Local Bus (CL-GD5424/'26/'28/'29 only) *(cont.)*

Name	Type	Description
BE[3:0]#	I	**BYTE ENABLE [3:0]#:** These active-LOW inputs are connected directly to the '386DX/'486 or VESA VL byte enable outputs. In the case of the '386SX, BE0# is unused and may be left un-connected. BE1#, 2, and 3 are redefined as BHE#, BLE#, and A1, respectively. They must be connected directly to the corresponding '386 outputs.
ADS#	I	**ADDRESS STROBE:** This active-LOW input indicates that a new cycle has begun. It must be connected directly to the ADS# pin on the CPU. For VESA VL-Bus, this pin is connected to LADS#.
CPU-RESET	I	**CPU RESET:** When this active-HIGH input is active, the CL-GD542X is forced into an initial condition. It is used to synchronize the CL-GD542X to CLK1X or CLK2X. This pin must be connected to the RESET pin of the CPU in a '386 system. It must be connected to Ground in a '486 system. It must be connected to RDYRTN# in a VESA VL-Bus system.
W/R#	I	**WRITE/READ:** This input indicates whether a write or read operation is to occur. It must be connected directly to the W/R# pin on the CPU. If W/R# is HIGH, a write will occur. If it is LOW, a read will occur.
CLK2X	I	**CLOCK 2X:** This is the timing reference for the CL-GD542X when connected to a '386SX or '386DX local bus. This is redefined as CLK1X for the '486 local bus. In either case, it must be connected directly to the corresponding CPU pin. For VESA VL-Bus, this pin is connected to LCLK.
M/IO#	I	**MEMORY/IO#:** This input indicates whether a memory or I/O operation is to occur. It must be connected directly to the M/IO# pin on the CPU. If M/IO# is HIGH, a memory operation will occur. If it is LOW, an I/O operation will occur.
UADDR#	I	**UPPER ADDRESS:** This active-LOW input is a decode of the upper-CPU Address bits A[32:24]. This input is unused in the case of a '386SX local bus and may be left unconnected. Refer to appendices in the *CL-GD542X Technical Reference Manual* for information on the generation of this signal.
RESET	I	**RESET:** This active-HIGH input initializes the CL-GD542X to a known state. The trailing (falling) edge of this input loads the Configuration register CF[14:0] with the data on MD[30:16], determined by internal pull-up resistors and optional external pull-down resistors.

2.3 Host Interface — Local Bus (CL-GD5424/'26/'28/'29 only) *(cont.)*

Name	Type	Description
RDY#	TS	**RDY #:** This active-low signal is used as an output to terminate a CL-GD542X bus cycle.
LBA#	TS	**LOCAL BUS ACKNOWLEDGE #:** This open-collector output is driven LOW to indicate that the CL-GD542X will respond to the current cycle. This signal is generated from a decode of A[23:2], UADDR, and M/IO#. This output will be active before the middle of the first T2 after an active ADS#. For VESA VL-Bus, this pin is connected to LDEV#.
BS16#	OC	**BUS SIZE 16 #:** This active-LOW output is driven by the CL-GD542X to indicate that the current cycle addresses a 16-bit resource. The '386DX/'486 will convert the cycle to an appropriate number of 16-bit transfers. This pin is not used for a '386SX local bus and may be left unconnected. For VESA VL-Bus, this pin is connected to LBS16#.
INTR	TS	**INTERRUPT REQUEST:** This active-HIGH output indicates the CL-GD542X has reached the end of an active field. Specifically, the transition occurs at the beginning of the bottom border. See register CR11 for a description of the controls for this pin.
OEH#	O	**OUTPUT ENABLE HIGH#:** This active-LOW output controls the output enables for the data transceivers that connect the CL-GD542X SD[15:0] pins to the '486 or VESA VL-Bus D[31:16] pins.
OEL#	O	**OUTPUT ENABLE LOW#:** This active-LOW output controls the output enables for the data transceivers that connect the CL-GD542X SD[15:0] pins to the '486 or VESA VL-Bus D[15:0] pins.

2.4 Dual-Frequency Synthesizer Interface

Name	Type	Description
OSC	I	**OSCILLATOR INPUT:** This TTL input pin supplies the reference frequency for the dual-frequency synthesizer. It requires an input frequency of 14.31818 ± 0.01% MHz with a duty cycle of 50 ± 10%. This input can be supplied from the appropriate pin on the ISA or MicroChannel bus, or from an oscillator, or with a series-resonant crystal connected between this pin and the XTAL pin.
XTAL	O	**CRYSTAL:** This output pin allows the use of a crystal to supply the reference frequency for the synthesizer. A series-resonant crystal may be connected between this pin and the OSC pin. If this pin is not used for a crystal connection, it must be left un-connected.
MFILTER	O	**MEMORY CLOCK FILTER:** This pin must be connected to a PI RC filter returned to AVSS4. The values of the two capacitors and the resistor are shown in Appendix B17 in the *CL-GD542X Technical Reference Manual.* The filter components, especially the input capacitor and the resistor, must be placed as closely as possible to this pin.
VFILTER	O	**VIDEO CLOCK FILTER:** This pin must be connected to a PI RC filter returned to AVSS1 or AVDD1, depending on processing. The values of the two capacitors and the resistor are shown in Appendix B17 in the *CL-GD542X Technical Reference Manual.* The filter components, especially the input capacitor and the resistor, must be placed as closely as possible to this pin.
MCLK	I/O	**MEMORY CLOCK:** This pin is normally an output and may be used to monitor the internal MCLK. Typically, it would not be connected. If CF[4] is a zero, MCLK will be an input and the internal MCLK oscillator will be disabled. This configuration is intended for testing only.

2.5 Video Interface

Name	Type	Description
VSYNC	TS	**VERTICAL SYNC:** This output supplies the vertical synchronization pulse to the monitor. The polarity of this output is programmable. This pin is put into high impedance when ESYNC* is LOW. This pin may be connected directly to the corresponding pin on the feature connector.
HSYNC	TS	**HORIZONTAL SYNC:** This output supplies the horizontal synchronization pulse to the monitor. The polarity of this output is programmable. This pin is put into high impedance when ESYNC* is LOW. This pin may be connected directly to the corresponding pin on the feature connector.
BLANK*	I/O	**BLANK*:** This is a bi-directional pin. If ESYNC* is HIGH, BLANK* is an output. As an output, it supplies a blanking signal to the feature connector. If ESYNC* is LOW, BLANK* is an input. As an active-LOW input, it forces the RED, GREEN, and BLUE outputs to zero current. This pin may be connected directly to the corresponding pin on the feature connector.
P[7:0]	I/O	**PIXEL BUS [7:0]:** These are bi-directional pins. If EVIDEO* is HIGH, these pins are outputs and reflect the address into the palette DAC. If EVIDEO* is LOW, these pins are inputs and can be used to drive pixel values into the palette DAC. These pins may be connected directly to the corresponding pins on the feature connector.
DCLK	I/O	**VIDEO DOT CLOCK:** This is a bi-directional pin. If EDCLK* is HIGH, this is an output and may be used to externally latch the data on the Pixel Bus. If EDCLK* is LOW, this is an input and may be used to clock data on the Pixel Bus into the CL-GD542X. This pin may be connected directly to the corresponding pin on the feature connector.
ESYNC*	I/O	**ENABLE SYNC AND BLANK:** This input is used to control the buffers on HSYNC, VSYNC, and BLANK*. If ESYNC* is HIGH, the controlled pins are outputs. If ESYNC* is LOW, BLANK* is an input. HSYNC and VSYNC are not driven by the CL-GD542X, and must be driven externally to valid input levels. This pin may be connected directly to the corresponding pin on the feature connector.
EVIDEO*	I/O	**ENABLE VIDEO:** This input controls the buffers on P[7:0]. If EVIDEO* is HIGH, P[7:0] are outputs. If EVIDEO* is LOW, P[7:0] are inputs. This pin may be connected directly to the corresponding pin on the feature connector. This pin is not limited to static operation; it can switch at the DCLK rate.
EDCLK*	I	**ENABLE DOT CLOCK:** This input is used to control the buffer on DCLK. If EDCLK* is HIGH, DCLK is an output. If EDCLK* is LOW, DCLK is an input. This pin may be connected directly to the corresponding pin on the feature connector.

2.5 Video Interface *(cont.)*

Name	Type	Description
RED	O	**RED VIDEO:** This analog output supplies current corresponding to the red value of the pixel being displayed. Each of the three DACs consists of 255 summed current sources. For each pixel, either the 6-bit value from the look-up table or a 5-, 6-, or 8-bit true-color value is applied to each DAC input to determine the number of current sources to be summed. Full-scale current on the RED, GREEN, and BLUE outputs is related to IREF as follows: $If = (63/30) \times IREF$ To maintain IBM VGA compatibility, each DAC output is typically terminated to monitor ground with a 150-Ω 2-percent resistor. This resistor, in parallel with the 75-Ω resistor in the monitor, will yield a 50-Ω impedance to ground. For a full-scale voltage of 700 mV, full-scale current output should be 14 mA.
GREEN	O	**GREEN VIDEO:** This analog output supplies current corresponding to the green value of the pixel being displayed. See the description of RED for information regarding the termination of this pin.
BLUE	O	**BLUE VIDEO:** This analog output supplies current corresponding to the blue value of the pixel being displayed. See the description of RED for information regarding the termination of this pin.
IREF	I	**DAC CURRENT REFERENCE:** The current drawn from AVDD through this pin determines the full-scale output of each DAC. This pin should be connected to a constant current source. A recommended circuit is provided in appendices of the *CL-GD542X Technical Reference Manual.*

2.6 Display Memory Interface

Name	Type	Description
RAS*	O	**ROW ADDRESS STROBE *:** This active-LOW output is used to latch the row address from MA[9:0] into the DRAMs. This pin must be connected to the RAS* pins of all the DRAMs in the display memory array. These pads, and those for the other DRAM controls, are matched for one to four loads. If eight DRAMs are used, damping resistors may be required to control edge rates and undershoot on these and other control pins.
CAS*	O	**COLUMN ADDRESS STROBE *:** This active-LOW output is used to latch the Column Address from MA[9:0] into the DRAMs. This pin must be connected to the CAS* pins of all the DRAMs in the display memory array. **NOTE:** If CF[12] = 0 (dual-CAS* DRAMs), this pin becomes WE*.
OE*	O	**OUTPUT ENABLE *:** This active-LOW output is used to control the output enables of the DRAMs. For 256K x 4 DRAMs and 256K x 16 DRAMs with Dual-write Enables, this pin must be connected to the OE* pins of all the DRAMs in the display memory array. For 256K x 16 DRAMs with dual-CAS*, this pin is a no-connect. For the CL-GD5426/'28/'29 with 2 Mbytes of display memory, this pin becomes RAS1*. See the DRAM Configuration Tables, Section 4.
WE[3:0]*	O	**WRITE ENABLE [3:0]*:** These active-LOW outputs are used to control the Write Enable inputs of the DRAMs. These pins must be connected to the WE* pins of the DRAMs as indicated in the DRAM Configuration Tables, Section 4. **NOTE:** If CF[12]=0 (dual-CAS DRAMs) these pins become CAS[3:0]*. These pins may be connected to the CAS* pins of the DRAMs. WE[1:0] are reserved on the CL-GD5420 (Revision 'A').
MA[9]	O	**MEMORY ADDRESS [9]:** This pin controls one address input of the DRAMs. See the DRAM Configuration Tables, Section 4.
MA[8:0]	O	**MEMORY ADDRESS [8:0]:** These pins control the address inputs of the DRAMs. These pins must be connected to the address pins of the DRAMs. See the DRAM Configuration Tables, Section 4.
MD[31:0]	TS	**MEMORY DATA [31:0]:** These pins are used to transfer data between the CL-GD542X and the display memory. These pins must be connected to the data pins of the DRAMs. See the DRAM Configuration Tables, Section 4. These pins are forced into High Impedance when RESET is active; this allows the configuration pull-down resistors to override the weak pull-ups and be loaded into the Configuration register (CF). MD[15:0] are reserved on the CL-GD5420 (Revision 'A').

2.7 Miscellaneous Pins

Name	Type	Description
EECS	O	**EEPROM CHIP SELECT:** This pin is used to control the Chip Select of the optional configuration EEPROM, and should be connected directly to that pin (ISA and Microchannel only). **NOTE:** This pin is redefined as OEL* for the '486 or VESA VL-Bus (CL-GD5424/'26/'28/'29 only).
EEDI	I	**EEPROM DATA IN:** This pin is used to read the data from the optional configuration EEPROM, and should be connected directly to the Data Out pin (ISA and Microchannel only). **NOTE:** This pin is redefined as OEH* for the '486 or VESA VL-Bus (CL-GD5424/'26/'28/'29 only).
EROM*	O	**ENABLE ROM BUFFERS*:** This active-LOW output is used to control the Output Enable pins of up to two 8-bit bus drivers. These buffers are used to connect the data pins of the BIOS EPROMs to the System Data Bus. This output is forced HIGH when RESET is active. This output goes active only for memory read cycles to the Address Range C000:0 through C7FF:F. It is gated with MEMR* in ISA mode, and is gated with -CMD in MicroChannel mode. It is un-latched address decode in Local Bus modes.
OVRW	O	**OVERLAY WINDOW:** This signal is active-LOW. It is intended to be used in applications involving video overlays. For additional connectivity information, see Appendix B14 in the *CL-GD542X Technical Reference Manual.* OVRW is reserved on the CL-GD5420.
TWR*	I	**TEST LATCH LOAD ENABLE*:** This pin is intended for factory testing and must be pulled-up for normal operation. It can be used in board-level testing to disable most of the CL-GD542X output pins. For additional information, see Appendix B14 in the *CL-GD542X Technical Reference Manual.*

2.8 Power Pins

Name	Type	Description
VDD[7:1]	Power	**PLUS FIVE (LOGIC):** These seven pins are used to supply +5 volts to the core logic of the CL-GD542X. Each pin must be connected to the VCC rail as described in Appendices B1 - B3. Each pin must be bypassed with a 0.1-µF capacitor with proper high-frequency characteristics, as closely to the pin as possible. If a multi-layer board is used, each VDD pin must be connected to the power plane as described in Appendices B1 - B3.
VSS[13:1]	Ground	**GROUND (LOGIC):** These 13 pins are used to supply ground reference to the core logic of the CL-GD542X. Each pin must be connected directly to the GND rail. If a multi-layer board is used, each VSS pin must be connected to the ground plane.
AVDD[1]	Power	**PLUS FIVE (VCLK):** This pin is used to supply +5 volts to the video clock synthesizer of the CL-GD542X. This pin must be connected to the VCC rail via a 33-Ω resistor and bypassed to AVSS4 with a 10-µF capacitor.
AVSS[1]	Ground	**GROUND (VCLK):** This pin is used to supply ground reference to the video clock synthesizer of the CL-GD542X. This pin must be connected to the GND rail.
AVDD[4]	Power	**PLUS FIVE (MCLK):** This pin is used to supply +5 volts to the memory clock synthesizer of the CL-GD542X. This pin must be connected to the VCC rail via a 33-Ω resistor and bypassed to AVSS4 with a 10-µF capacitor.
AVSS[4]	Ground	**GROUND (MCLK):** This pin is used to supply ground reference to the video clock synthesizer of the CL-GD542X. This pin must be connected to the GND rail.
AVDD[3:2]	Power	**PLUS FIVE (DAC):** These two pins are used to supply +5 volts to the palette DAC of the CL-GD542X. Each pin must be connected directly to the VCC rail. Each pin must be bypassed as closely to the pin as possible with a 0.1-µF capacitor with proper high-frequency characteristics. If a multi-layer board is used, each VDD pin must be connected to the power plane.
AVSS[3:2]	Ground	**GROUND (DAC):** These two pins are used to supply ground reference to the palette DAC of the CL-GD542X. Each pin must be connected to the GND rail. For various adapter board and motherboard solutions, see appendices in the *CL-GD542X Technical Reference Manual.*

3. FUNCTIONAL DESCRIPTION

3.1 General

The CL-GD542X family of VGA controllers offers a complete VGA-standards-compatible solution. All of the hardware necessary for CPU updates to memory, screen refresh and DRAM refresh is included in the CL-GD542X. A complete VGA motherboard solution can be implemented with one 256K x 16 DRAM with any CL-GD542X chip.

The chip block diagram on the following page shows CL-GD542X connection to the host, display memory, and monitor. Each member of the CL-GD542X family of VGA controllers is pin-to-pin compatible on the system bus.

3.2 Functional Blocks

The following functional blocks have been integrated into the CL-GD542X:

CPU Interface

The CL-GD542X connects directly to the ISA bus, E-ISA bus, MicroChannel bus, or '386 and '486 bus (CL-GD5424/'26/'28/'29 only). No glue logic is required. The CL-GD542X internally decodes a 16- or 24-bit address and responds to the applicable control lines. It executes both I/O accesses and memory accesses as either an 8- or 16-bit device.

CPU Write Buffer

The CPU Write Buffer contains a queue of CPU write accesses to display memory that have not been executed because of memory arbitration. Maintaining a queue allows the CL-GD542X to release the CPU as soon as it has recorded the address and data, and to execute the operation when display memory is available, increasing CPU performance.

Graphics Controller

The Graphics Controller is located between the CPU interface and the Memory Sequencer. It performs text manipulation, data rotation, color mapping, and miscellaneous operations.

BitBLT

This is a unique GUI acceleration feature in the CL-GD5426/'28/'29. The BitBLT function moves data with ROPs (Raster Operations). This operation occurs in Packed-pixel modes with 8-, 16-, or 24-bit-per-pixel transfers. Color Expansion can be used to translate monochrome images to 8- or 16-bit color. The source or destination of a BitBLT operation can be system memory.

Memory Arbitrator

The Memory Arbitrator allocates bandwidth to the four functions that compete for the limited bandwidth of display memory. These are CPU access, screen refresh, DRAM refresh, and BitBLT. DRAM refresh is handled invisibly by allocating a selectable number of CAS*-before-RAS* refresh cycles at the beginning of each scanline. Screen refresh and CPU/BitBLT access are allocated cycles according to the FIFO-control parameters, with priority given to screen refresh.

Memory Sequencer

The Memory Sequencer generates timing for display memory. This includes RAS*, CAS* and multiplexed-address timing, as well as WE* and OE* timing. The Sequencer generates CAS*-before-RAS* refresh cycles, Random Read and Random Early Write cycles, and Fast-page mode Read and Early Write cycles. The Memory Sequencer generates multiple-CAS* or -WE* Signals according to the memory type used.

CRT Controller

The CRT Controller generates the HSYNC and VSYNC Signals required for the monitor, as well as BLANK* signals required by the palette DAC.

Video FIFO

The Video FIFO allows the Memory Sequencer to execute the display memory accesses needed for screen refresh at maximum memory speed rather than at the screen refresh rate. This makes it possible to collect the accesses for screen refresh near the beginning of the scanline, and to execute them in Fast-page mode rather than Random Read mode.

Attribute Controller

The Attribute Controller formats the display for the screen. Display color selection, text blinking and underlining are performed by the Attribute Controller. Alternate font selection occurs in the Attribute Controller.

Palette DAC

The palette DAC block contains the color palette and three 8-bit digital-to-analog converters. The color palette, with 256 18-bit entries, converts a color code that specifies the color of a pixel into three 6-bit values, one each for red, green, and blue.

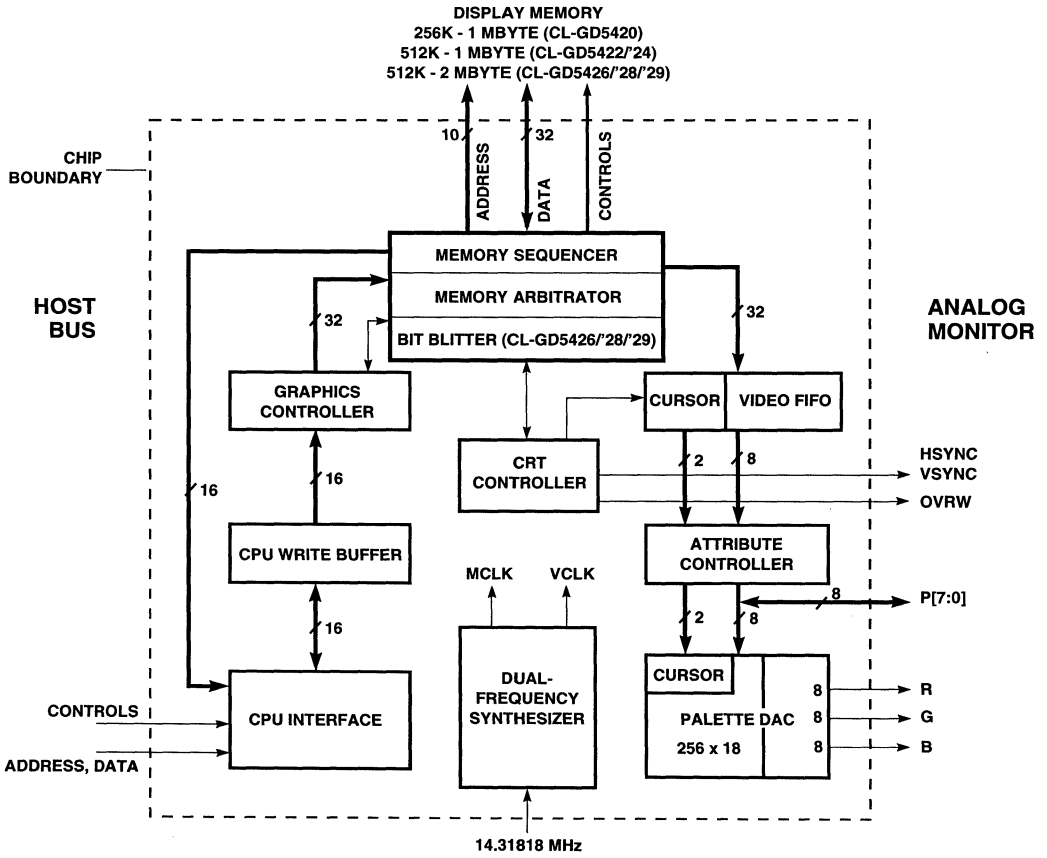


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Figure 3–1. CL-GD542X Chip Block Diagram

Alternatively, the CL-GD542X (excluding the CL-GD5420) can be configured for 15-, 16-, or 24-bit pixels. This allows 32K, 65K, or 16 million simultaneous colors to be displayed on the screen. The 24 bits are allocated as 8-8-8 for the 16 million colors, 5-6-5 for the 64K Color mode, or 5 to each (red, green, and blue) DAC for the 32K Color mode.

Dual-Frequency Synthesizer

The dual-frequency synthesizer generates the Memory Sequencer Clock and the Video Display Clock from a single reference frequency. The frequency of each clock is programmable. The reference frequency can be generated with an internal crystal-controlled oscillator. Alternatively, it can be supplied from an external TTL source.

VESA® Connector/VGA Passthrough Connector

The CL-GD542X is designed to connect directly to a VESA connector. It supports the three enable/disable inputs, and the Pixel bus can drive the connector directly. Through this connector, the overlay feature could be used in multimedia applications. This allows for internal DAC utilization in 16-bit-per-pixel mode. The CL-GD5429 supports the VESA Advanced Feature Connector (VAFC) Baseline for Video Overlay.

3.3 Functional Operation

The four major operations handled by the CL-GD542X are discussed below.

CPU Access to Registers

The host can be any processor controlling an ISA, E-ISA, MicroChannel, or '386 and '486 local bus. It accesses CL-GD542X registers by setting up 16- or 24-bit addresses and making controls such as IORD* or IOWR* active. The CL-GD542X can respond either as an 8- or 16-bit peripheral, depending on how the chip has been designed into the system.

DRAM and screen refresh occur concurrently with, and independently of, register access (unless the host is changing display parameters or has suppressed refresh). Registers are described in detail in the *CL-GD542X Technical Reference Manual.*

CPU Access to Display Memory

All host accesses to display memory are handled by the CL-GD542X. The host first sets up certain parameters, such as color and write masks, then generates a memory access in the range to which the CL-GD542X is programmed to respond.

Display Memory Refresh

The CL-GD542X automatically generates a selectable number of CAS*-before-RAS* refresh cycles during each horizontal timing period.

Screen Refresh

The CRT monitor requires a near-constant rewriting since its only memory is the phosphor persistence. This persistence is typically only a few milliseconds. The CL-GD542X fetches information from the display memory for each scanline as quickly as possible, using Fast-page mode cycles to fill the Video FIFO. This allows the maximum possible time for the host to access the display memory.

3.4 Performance

The CL-GD542X is designed with the following performance-enhancing features:

- Accelerated Microsoft Windows with BitBLT (CL-GD5426/'28/'29 only)
- 16-bit CPU interface to I/O registers for faster host access
- 16-bit CPU interface to display memory for faster host access in all modes, including Planar mode
- 32-bit display memory data bus for faster access to display memory (CL-GD5422/'24/'26/'28/'29)
- DRAM Fast-page mode operations for faster access to display memory
- Zero-wait-state performance and a CPU write buffer allows faster CPU access for writes to display
- Video FIFO to minimize memory contention
- 32 x 32 and 64 x 64 hardware cursor to improve Microsoft Windows performance
- Increased throughput with '386 and '486 local bus interface (CL-GD5424/'26/'28/'29)

3.5 Compatibility

The CL-GD542X includes all registers and data paths required for VGA controllers.

The CL-GD542X supports extensions to VGA, including 1024 x 768 x 256 interlaced and non-interlaced, and 1280 x 1024 x 256 interlaced modes. Additionally, various 132-column text modes are supported.

3.6 Board Testability

The CL-GD542X chip is testable, even when installed on a PC board. By using Pinscan Testing, any IC signal pins not connected to the board or shorted to a neighboring pin or trace, will be detected. The Signature Generator allows the entire system, including the display memory, to be tested at speed.

4. CL-GD542X CONFIGURATION TABLES

4.1 Video Modes

Table 4–1. IBM® Standard VGA Video Modes

Mode No.	VESA® No.	No. of Colors	Char. x Row	Char. Cell	Screen Format	Display Mode	Pixel Freq. MHz	Horiz. Freq. kHz	Vert. Freq. Hz
0,1	0,1	16/256K	40 x 25	9 x 16	360 x 400	Text	14	31.5	70
2, 3	2, 3	16/256K	80 x 25	9 x 16	720 x 400	Text	28	31.5	70
4, 5	4, 5	4/256K	40 x 25	8 x 8	320 x 200	Graphics	12.5	31.5	70
6	6	2/256K	80 x 25	8 x 8	640 x 200	Graphics	25	31.5	70
7	7	Monochrome	80 x 25	9 x 16	720 x 400	Text	28	31.5	70
D	D	16/256K	40 x 25	8 x 8	320 x 200	Graphics	12.5	31.5	70
E	E	16/256K	80 x 25	8 x 14	640 x 200	Graphics	25	31.5	70
F	F	Monochrome	80 x 25	8 x 14	640 x 350	Graphics	25	31.5	70
10	10	16/256K	80 x 25	8 x 14	640 x 350	Graphics	25	31.5	70
11	11	2/256K	80 x 30	8 x 16	640 x 480	Graphics	25	31.5	60
12	12	16/256K	30 x 30	8 x 16	640 x 480	Graphics	25	31.5	60
12+	12+	16/256K	30 x 30	8 x 16	640 x 480	Graphics	31.5	37.9	72
13	13	256/256K	40 x 25	8 x 8	320 x 200	Graphics	12.5	31.5	70

Table 4–2. Cirrus Logic Extended Video Modes

Mode No.	VESA® No.	No. of Colors	Char. x Row	Char. Cell	Screen Format	Display Mode	Pixel Freq. MHz	Horiz. Freq. kHz	Vert. Freq. Hz
14	–	16/256K	132 x 25	8 x 16	1056 x 400	Text	41.5	31.5	70
54	10A	16/256K	132 x 43	8 x 8	1056 x 350	Text	41.5	31.5	70
55	109	16/256K	132 x 25	8 x 14	1056 x 350	Text	41.5	31.5	70
58,6A	102	16/256K	100 x 37	8 x 16	800 x 600	Graphics	36	35.2	56
58,6A	102	16/256K	100 x 37	8 x 16	800 x 600	Graphics	40	37.8	60
58,6A	102	16/256K	100 x 37	8 x 16	800 x 600	Graphics	50	48.1	72
5C	103	256/256K	100 x 37	8 x 16	800 x 600	Graphics	36	35.2	56
5C	103	256/256K	100 x 37	8 x 16	800 x 600	Graphics	40	37.9	60
5C	103	256/256K	100 x 37	8 x 16	800 x 600	Graphics	50	48.1	72
5D†	104	16/256K	128 x 48	8 x 16	1024 x 768	Graphics	44.9	35.5	87†

Table 4–2. Cirrus Logic Extended Video Modes *(cont.)*

Mode No.	VESA® No.	No. of Colors	Char. x Row	Char. Cell	Screen Format	Display Mode	Pixel Freq. MHz	Horiz. Freq. kHz	Vert. Freq. Hz
5D	104	16/256K	128 x 48	8 x 16	1024 x 768	Graphics	65	48.3	60
5D	104	16/256K	128 x 48	8 x 16	1024 x 768	Graphics	75	56	70
5D	104	16/256K	128 x 48	8 x 16	1024 x 768	Graphics	77	58	72
5F	101	256/256K	80 x 30	8 x 16	640 x 480	Graphics	25	31.5	60
5F	101	256/256K	80 x 30	8 x 16	640 x 480	Graphics	31.5	37.9	72
60†	105	256/256K	128 x 48	8 x 16	1024 x 768	Graphics	44.9	35.5	87†
60	105	256/256K	128 x 48	8 x 16	1024 x 768	Graphics	65	48.3	60
60	105	256/256K	128 x 48	8 x 16	1024 x 768	Graphics	75	56	70
60	105	256/256K	128 x 48	8 x 16	1024 x 768	Graphics	77	58	72
64	111	64K	–	–	640 x 480	Graphics	25	31.5	60
64	111	64K	–	–	640 x 480	Graphics	31.5	37.9	72
65	114	64K	–	–	800 x 600	Graphics	36	35.2	56
65	114	64K	–	–	800 x 600	Graphics	40	37.8	60
66	110	32K‡	–	–	640 x 480	Graphics	25	31.5	60
66	110	32K‡	–	–	640 x 480	Graphics	31.5	37.9	72
67	113	32K‡	–	–	800 x 600	Graphics	36	31.5	56
6C†	106	16/256K	160 x 64	8 x 16	1280 x 1024	Graphics	75	48	87†
6D†	–	256/256K	160 x 64	8 x 16	1280 x 1024	Graphics	75	48	87†
71	112	16M	80 x 30	8 x 16	640 x 480	Graphics	25	31.5	60
74†	–	64K	–	–	1024 x 768	Graphics	44.9	35.5	87†

NOTES:

1) Some modes are not supported by all CL-GD542X controllers. Refer to the CL-GD542X Data Book and Software Release Kit for the list of video modes supported by the CL-GD542X BIOS.
2) Not all monitors support all modes. The fastest vertical refresh rate for the monitor type selected will be used automatically.
3) '‡' indicates 32K Direct-Color/256-color Mixed mode.
4) '†' indicates Interlaced mode.

4.2 Configuration Register, CF1

When RESET (system power-on reset) goes active, the CL-GD542X samples the levels on several of the Display Memory Data MD[x] pins. These levels are latched into a write-only configuration register (CF1). The data bits in this register are not accessible to the host CPU. The levels on the Memory Data bus are by default a logic '1' during power-on reset due to internal 250K-Ω pull-up resistors. A logic '0' is achieved by installing an external 6.8K-Ω pull-down resistor on the memory data line corresponding to the appropriate bit in the Configuration register. The following table identifies the Configuration register bits and the particular VGA function enabled by the latched level on the Memory Data bus during power-on reset.

Table 4–3. Configuration Register Bits

CF Bits	Level	Description	Memory Data Bit	Pin Number
15	0 1	Source VCLK on MCLK pin (CL-GD5429) Source MCLK on MCLK pin (CL-GD5429)	MD31	97
14, 7, 5	000 001 010 011 100 101 110 111	Reserved '386DX local bus (CL-GD5424/'26/'28/'29) '386SX local bus (CL-GD5424/'26/'28/'29) '486SX/DX local bus (CL-GD5424/'26/'28) VESA® VL-Bus™ > 33 MHz (CL-GD5429) MicroChannel® bus VESA® VL-Bus™ (CL-GD5424/'26/'28/'29) ISA bus	MD30, 23, 21	98, 108, 110
13	0 1	Asymmetric DRAM Symmetric DRAM	MD29	99
12	0 1	CAS3:0, single-WE* (except CL-GD5420) WE3:0, single-CAS*	MD28	100
11	0 1	7-MCLK RAS* cycle 6-MCLK RAS* cycle	MD27	102
10,9	00 01 10 11	50.11363-MHz MCLK 44.74431-MHz MCLK 41.16477-MHz MCLK 37.58523-MHz MCLK	MD26, 25	103, 104
8	0 1	64K ROM BIOS @ C0000-CFFFF 32K ROM BIOS @ C0000-C7FFF	MD24	105
6	0 1	16-bit BIOS ROM (MCS16* generated for 64K or 32K) 8-bit BIOS ROM (CL-GD5424 does not generate MCS16*)	MD22	109
4	0 1	External MCLK (pin 157 is an input) (Test) Internal MCLK (pin 157 is an output)	MD20	111
3	0 1	Port 3C3h is Video System Sleep register Port 46E8h is Video System Sleep register	MD19	112
2		8514 DAC Addressing(CL-GD5424/'26/'28) 2070 Local Bus Address (CL-GD5429)	MD18	113
1	0 1 0 1	Zero wait enabled (except CL-GD5429) Zero wait disabled (except CL-GD5429) Enable 2070 Address Decode (CL-GD5429) DIsable 2070 Address Decode (CL-GD5429)	MD17	114
0		DAC power-down	MD16	115

4.3 Host Interface Signals

With the pin connections listed below, the CL-GD542X will interface directly to an ISA, MicroChannel, or local bus.

Table 4–4. Bus Connections

CL-GD542X Pin	ISA Bus	MicroChannel® Bus	'386SX	'386DX	'486	VESA® VL-Bus™
[45..42], [39..29]	SA[16:2]	A[16:2]	A[16:2]	A[16:2]	A[16:2]	A[16:2]
28	SA1	A1	A1	BE3#	BE3#	BE3#
27	SA0	A0	BLE#	BE2#	BE2#	BE2#
[21..15]	LA[23:17]	A[23:17]	A[23:17]	A[23:17]	A[23:17]	A[23:17]
[11..8], [6..3]	SD[15:8]	D[15:8]	D[15:8]	D[15:8]	D[15:8]†	D[15:8]†
[63..62], [60..59], [57..54]	SD[7:0]	D[7:0]	D[7:0]	D[7:0]	D[7:0]†	D[7:0]†
24	SBHE*	-SBHE	BHE#	BE1#	BE1#	BE1#
25	BALE	MADE24	ADS#	ADS#	ADS#	ADS#
46	AEN	-CD_SETUP	CPU-Reset	CPU-Reset	Ground	RDYRTN#
49	IOR*	-S1	W/R#	W/R#	W/R#	W/R#
50	IOW*	-CMD	CLK2X	CLK2X	CLK1X	CLK1X
14	MEMR*	M/-IO	M/IO#	M/IO#	M/IO#	M/IO#
13	MEMW*	-S0	(unused)	UADDR#	UADDR#	UADDR#
41	RESET	CHRESET	RESET	RESET	RESET	RESET
48	REFRESH	-REFRESH	(unused)	BE0#	BE0#	BE0#
23	MCS16*	-CD_DS16	(unused)	BS16#	BS16#	BS16#
51	0WS*	(unused)	GROUND	GROUND	GROUND	GROUND
52	IRQ	-IRQ	INTR	INTR	INTR	INTR
47	IOCHRDY	CD_CHRDY	READY#	READY#	RDY#	RDY#
22	IOCS16*	-CD_SFDBK	LBA#	LBA#	LBA#	LBA#
159	OSC	OSC	OSC	OSC	OSC	OSC
2	EROM*	EROM*	EROM*	EROM*	EROM*	EROM*

NOTES:

1) For ISA bus applications, note that SA[19..17] are not found on the CL-GD542X; this means that an adapter board will only function in a 16-bit slot.
2) The OSC and EROM* pins are common in all configurations.
3) The OSC pin is an input for 14.31818 MHz.
4) † Data lines D[15:0] connect to external data steering transceiver.

5. VGA REGISTER PORT MAP

Table 5–1. VGA Register Port Map

Address	Port
94	POS 102 Access Control (3C3 sleep)
102	POS102 register
3B4	CRT Controller Index (R/W — monochrome)
3B5	CRT Controller Data (R/W — monochrome)
3BA	Feature Control (W), Input Status register 1 (R) (monochrome)
3C0	Attribute Controller Index/Data (Write)
3C1	Attribute Controller Index/Data (Read)
3C2	Miscellaneous Output (W), Input Status register 0 (R)
3C3	MotherBoard Sleep
3C4	Sequencer Index (R/W)
3C5	Sequencer Data (R/W)
3C6	Video DAC Pixel Mask (R/W), Hidden DAC register (R/W)
3C7	Pixel Address Read mode (W), DAC State (R)
3C8	Pixel Mask Write mode (R/W)
3C9	Pixel Data (R/W)
3CA	Feature Control Readback (R)
3CC	Miscellaneous Output Readback (R)
3CE	Graphics Controller Index (R/W)
3CF	Graphics Controller Data (R/W)
3D4	CRT Controller Index (R/W — color)
3D5	CRT Controller Data (R/W — color)
3DA	Feature Control (W), Input Status register 1 (R) (color)
46E8	Adapter Sleep

6. CL-GD542X REGISTERS

External/General Registers

Abbreviation	Register Name	Index	Port
102 Access	POS 102 Access Control	–	94
POS102	POS102	–	102
VSSM	Motherboard Sleep *(CL-GD5424/'26/'28 only)*	–	3C3
VSSM	Adapter Sleep	–	46E8
MISC	Miscellaneous Output	–	3C2 (Write)
MISC	Miscellaneous Output	–	3CC (Read)
FC	Feature Control	–	3?A (Write)
FC	Feature Control	–	3CA (Read)
FEAT	Input Status Register 0	–	3C2
STAT	Input Status Register 1	–	3?A
3C6	Pixel Mask	–	3C6
3C7	Pixel Address Read Mode	–	3C7 (Write)
3C7	DAC State	–	3C7 (Read)
3C8	Pixel Address Write Mode	–	3C8
3C9	Pixel Data	–	3C9

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

VGA Sequencer Registers

Abbreviation	Register Name	Index	Port
SRX	Sequencer Index	–	3C4
SR0	Reset	0	3C5
SR1	Clocking Mode	1	3C5
SR2	Plane Mask	2	3C5
SR3	Character Map Select	3	3C5
SR4	Memory Mode	4	3C5

CRT Controller Registers

Abbreviation	Register Name	Index	Port
CRX	CRTC Index	–	3?4
CR0	Horizontal Total	0	3?5
CR1	Horizontal Display End	1	3?5
CR2	Horizontal Blanking Start	2	3?5
CR3	Horizontal Blanking End	3	3?5
CR4	Horizontal Sync Start	4	3?5
CR5	Horizontal Sync End	5	3?5
CR6	Vertical Total	6	3?5
CR7	Overflow	7	3?5
CR8	Screen A Preset Row Scan	8	3?5
CR9	Character Cell Height	9	3?5

6. CL-GD542X REGISTERS *(cont.)*

CRT Controller Registers (cont.)

Abbreviation	Register Name	Index	Port
CRA	Text Cursor Start	A	3?5
CRB	Text Cursor End	B	3?5
CRC	Screen Start Address High	C	3?5
CRD	Screen Start Address Low	D	3?5
CRE	Text Cursor Location High	E	3?5
CRF	Text Cursor Location Low	F	3?5
CR10	Vertical Sync Start	10	3?5
CR11	Vertical Sync End	11	3?5
CR12	Vertical Display End	12	3?5
CR13	Offset	13	3?5
CR14	Underline Row Scan	14	3?5
CR15	Vertical Blanking Start	15	3?5
CR16	Vertical Blanking End	16	3?5
CR17	Mode Control	17	3?5
CR18	Line Compare	18	3?5
CR22	Graphics Data Latches Readback	22	3?5
CR24	Attribute Controller Toggle Readback	24	3?5
CR26	Attribute Controller Index Readback	26	3?5

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

VGA Graphics Controller Registers

Abbreviation	Register Name	Index	Port
GRX	Graphics Controller Index	–	3CE
GR0	Set/Reset	0	3CF
GR1	Set/Reset Enable	1	3CF
GR2	Color Compare	2	3CF
GR3	Data Rotate	3	3CF
GR4	Read Map Select	4	3CF
GR5	Mode	5	3CF
GR6	Miscellaneous	6	3CF
GR7	Color Don't Care	7	3CF
GR8	Bit Mask	8	3CF

6. CL-GD542X REGISTERS *(cont.)*

VGA Attribute Controller Registers

Abbreviation	Register Name	Index	Port
ARX	Attribute Controller Index	–	3C0/3C1
AR0-ARF	Attribute Controller Palette	0:F	3C0/3C1
AR10	Attribute Controller Mode	10	3C0/3C1
AR11	Overscan (Border) Color	11	3C0/3C1
AR12	Color Plane Enable	12	3C0/3C1
AR13	Pixel Panning	13	3C0/3C1
AR14	Color Select	14	3C0/3C1

Extension Registers

Abbreviation	Register Name	Index	Port
SR2	Enable Writing Pixel Extension	2	3C5
SR6	Unlock ALL Extensions	6	3C5
SR7	Extended Sequencer Mode	7	3C5
SR8	EEPROM Control	8	3C5
SR9	Scratch-Pad 0	9	3C5
SRA	Scratch-Pad 1	A	3C5
SRB	VCLK0 Numerator	B	3C5
SRC	VCLK1 Numerator	C	3C5
SRD	VCLK2 Numerator	D	3C5
SRE	VCLK3 Numerator	E	3C5
SRF	DRAM Control	F	3C5
SR10	Graphics Cursor Y Position	10	3C5
SR11	Graphics Cursor X Position	11	3C5
SR12	Graphics Cursor Attributes	12	3C5
SR13	Graphics Cursor Pattern Address Offset	13	3C5
SR14	Scratch-Pad 2 *(CL-GD5426/'28 only)*	14	3C5
SR15	Scratch-Pad 3 *(CL-GD5426/'28 only)*	15	3C5
SR16	Performance Tuning *(CL-GD5424/'26/'28 /'29 only)*	16	3C5
SR17	Configuration Readback and Extended Control *(CL-GD5428/'29 only)*	17	3C5
SR18	Signature Generator Control *(except CL-GD5420)*	18	3C5
SR19	Signature Generator Result Low Byte *(except CL-GD5420)*	19	3C5
SR1A	Signature Generator Result High Byte *(except CL-GD5420)*	1A	3C5
SR1B	VCLK0 Denominator and Post-Scalar Value	1B	3C5
SR1C	VCLK1 Denominator and Post-Scalar Value	1C	3C5
SR1D	VCLK2 Denominator and Post-Scalar Value	1D	3C5
SR1E	VCLK3 Denominator and Post-Scalar Value	1E	3C5
SR1F	BIOS ROM Write Enable and MCLK Select	1F	3C5

6. CL-GD542X REGISTERS *(cont.)*

Extension Registers (cont.)

Abbreviation	Register Name	Index	Port
GR0	Write Mode 5 Background Extension	0	3CF
GR1	Write Mode 4, 5 Foreground Extension	1	3CF
GR9	Offset Register 0	9	3CF
GRA	Offset Register 1	A	3CF
GRB	Graphics Controller Mode Extensions	B	3CF
GRC	Color Key *(CL-GD5424/'26/'28/'29 only)*	C	3CF
GRD	Color Key Mask *(CL-GD5424/'26/'28/'29 only)*	D	3CF
GRE	Miscellaneous Control *(CL-GD5428/'29 only)*	E	3CF
GR10	16-bit Pixel BG Color High Byte *(except CL-GD5420)*	10	3CF
GR11	16-bit Pixel FG Color High Byte *(except CL-GD5420)*	11	3CF
CR19	Interlace End	19	3?5
CR1A	Interlace Control	1A	3?5
CR1B	Extended Display Controls	1B	3?5
CR1D	Overlay Mode Controls	1D	3?5
CR25	Part Status	25	3?5
CR27	ID	27	3?5
HDR	Hidden DAC *(except CL-GD5420)*	–	3C6

CL-GD5426/'28/'29 BitBLT Registers

Abbreviation	Register Name	Index	Port
GR20	BLT Width Low	20	3CF
GR21	BLT Width High	21	3CF
GR22	BLT Height Low	22	3CF
GR23	BLT Height High	23	3CF
GR24	BLT Destination Pitch Low	24	3CF
GR25	BLT Destination Pitch High	25	3CF
GR26	BLT Source Pitch Low	26	3CF
GR27	BLT Source Pitch High	27	3CF
GR28	BLT Destination Start Low	28	3CF
GR29	BLT Destination Start Mid	29	3CF
GR2A	BLT Destination Start High	2A	3CF
GR2C	BLT Source Start Low	2C	3CF
GR2D	BLT Source Start Mid	2D	3CF
GR2E	BLT Source Start High	2E	3CF
GR30	BLT Mode	30	3CF
GR31	BLT Start/Status	31	3CF
GR32	BLT Raster Operation	32	3CF
GR34	Transparent Color Select Low *(except CL-GD5429)*	34	3CF
GR35	Transparent Color Select High *(except CL-GD5429)*	35	3CF
GR38	Transparent Color Mask Low *(except CL-GD5429)*	38	3CF
GR39	Transparent Color Mask High *(except CL-GD5429)*	39	3CF

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

7. ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Ratings

Ambient temperature under bias ..... 0° to 70° C

Storage temperature ..... -65° to 150° C

Voltage on any pin ..... V_{SS} -0.5V to V_{CC} + 0.5V

Operating power dissipation ..... 1.5 Watts

Power supply voltage ..... 7 Volts

Injection current (latch-up testing) ..... 100 mA

NOTE: Stresses above those listed may cause permanent damage to system components. These are stress ratings only. Functional operation at these or any conditions above those indicated in the operational ratings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

7.2 DC Specifications (Digital)

(V_{CC} = 5V ± 5%, T_A = 0° to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Test Conditions	Note
V_{CC}	Power Supply Voltage	4.75	5.25	Volts	Normal Operation	
V_{IL}	Input Low Voltage	0	0.8	Volts		
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	Volts		
V_{OL}	Output Low Voltage		0.5	Volts	I_{OL} = 4 mA	1
V_{OH}	Output High Voltage	2.4		Volts	I_{OH} = 400 µA	2
I_{CC}	Supply Current				V_{CC} Nominal	3
I_{IH}	Input High Current		10	µA	$V_{IL} = V_{DD}$	
I_{IL}	Input Low Current	-10		µA	V_{DD} = 5.25, V_{IL} =0	
I_{IHP}	Input High Current (Pullup)	-10	10	µA	$V_{IL} = V_{DD}$	
I_{ILP}	Input Low Current (Pullup)	-45	-12	µA	V_{DD} = 5.25, V_{IL} =0	
I_{OZ}	Input Leakage	-10	10	µA	$0 < V_{IN} < V_{CC}$	
C_{IN}	Input Capacitance		10	pF		4
C_{OUT}	Output Capacitance		10	pF		4

NOTES:

1) I_{OL} is specified for a standard buffer. See the Pin Summary for further information.

2) I_{OH} is specified for a standard buffer. See the Pin Summary for further information.

3) I_{CC} is measured with VCLK and MCLK as indicated in the table below:

Part Number	VCLK	MCLK	I_{CC}
CL-GD5420	75 MHz	50 MHz	250
CL-GD5422	80 MHz	50 MHz	260
CL-GD5424	80 MHz	50 MHz	260
CL-GD5426/'28	80 MHz	50 MHz	260
CL-GD5429	86 MHz	60 MHz	tbd

4) This is not 100% tested, but is periodically sampled.

7.3 DC Specifications (Palette DAC)

(V_{CC} = 5V ± 5%, T_A = 0° to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Test Conditions	Note
A_{VDD}	DAC Supply Voltage	4.75	5.25	Volts	Normal Operation	
I_{REF}	DAC Reference Current	-3	-10	mA		1

NOTE: See the Detailed Pin Description for information regarding nominal I_{REF}.

7.4 DC Specifications (Frequency Synthesizer)

(V_{CC} = 5V ± 5%, T_A = 0° to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Test Conditions	Note
A_{VDD}	Synthesizer Supply Voltage	4.75	5.25	Volts		

7.5 DAC Characteristics

(V_{CC} = 5V ± 5%, T_A = 0° to 70° C, unless otherwise specified)

Symbol	Parameter	MAX	Units	Test Conditions	Note
R	Resolution	8	Bits		
IO	Output Current	30	mA	VO < 1V	
TR	Analog Output Rise/Fall Time	8	ns		2, 3, 4
TS	Analog Output Settling Time	15	ns		2, 3, 5
TSK	Analog Output Skew	tbd	ns		2, 3, 6
DT	DAC-to-DAC Correlation	2.5	%		6, 7
GI	Glitch Impulse Typical	tbd	pV-Sec		2, 3, 6
IL	Integral Linearity	1.5	LSB		
DL	Differential Linearity	1.5	LSB		

NOTES:

1) TD is measured from the 50% point of VCLK to 50% point of full-scale transition.
2) Load is 50 Ω and 30 pF per analog output.
3) IREF = -6.67 mA.
4) TR is measured from 10% to 90% full-scale.
5) TS is measured from 50% of full-scale transition to output remaining within 2% of final value.
6) Outputs loaded identically.
7) About the mid-point of the distribution of the three DACs measured at full-scale output.

7.6 List of Waveforms

Table 7–1. I/O Write Timing (ISA Bus)[a]

Symbol	Parameter	MIN	MAX	Units
t_1	Address, SBHE* Setup to IOW* Active	5	–	ns
t_2	IOW* Pulse Width	40	–	ns
t_3	Data Setup to IOW* Inactive	5	–	ns
t_4	Data Hold from IOW* Inactive	10	–	ns
t_5	Address, SBHE* Hold from IOW* Inactive	5	–	ns
t_6	IOW* Inactive to Any Command Active	80	–	ns

[a]AEN must be Inactive.

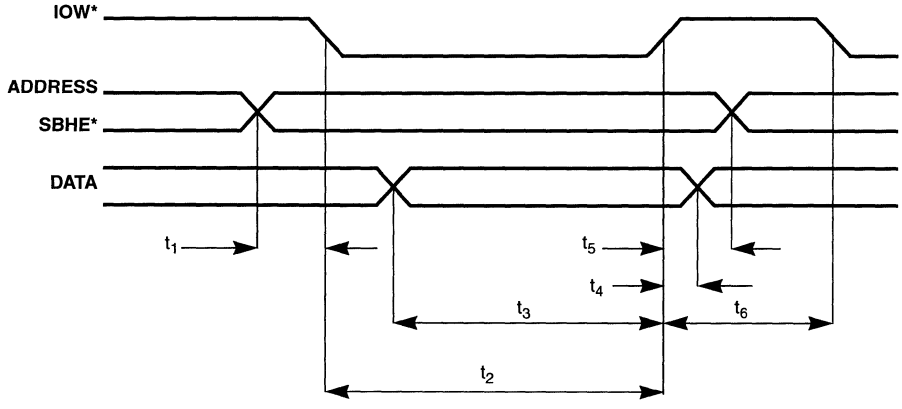


Figure 7–1. I/O Write Timing (ISA Bus)

Table 7–2. I/O Read Timing (ISA Bus)[a]

Symbol	Parameter	MIN	MAX	Units
t_1	Address, SBHE* Setup to IOR* Active	5	–	ns
t_2	IOR* Active to Low Impedance Delay	0	–	ns
t_3	Data delay from IOR* Active (IOR* Access Time)	–	60	ns
t_4	IOR* Pulse Width	70	–	ns
t_5	Data Hold from IOR* Inactive	0	20	ns
t_6	Address, SBHE* Hold from IOR* Inactive	0	–	ns
t_7	IOR* Inactive to High Impedance Delay	0	20	ns

[a]AEN must be Inactive.

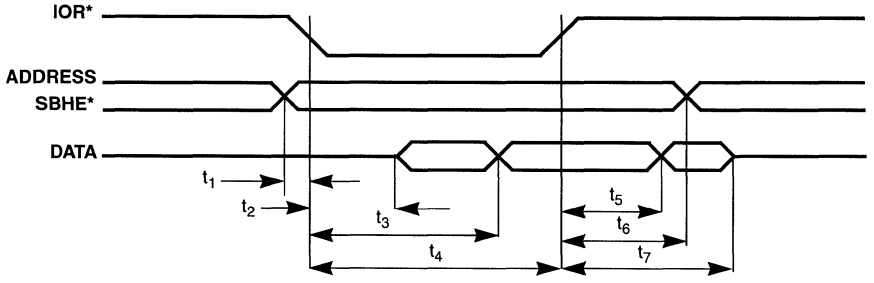


Figure 7–2. I/O Read Timing (ISA Bus)

Table 7–3. Memory Write Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	Address, SBHE* to SMEMW* Active Setup	5	–	ns
t_2	SMEMW* Pulse Width	3	–	t[a]
t_3	Data Valid from SMEMW* Active	–	3	t
t_4	Data Hold from SMEMW* Inactive	10	–	ns
t_5	Address, SBHE* Hold from SMEMW* Inactive	0	–	ns
t_6	SMEMW* Inactive to next SMEMW*	3	–	t

[a] t = MCLK Period.

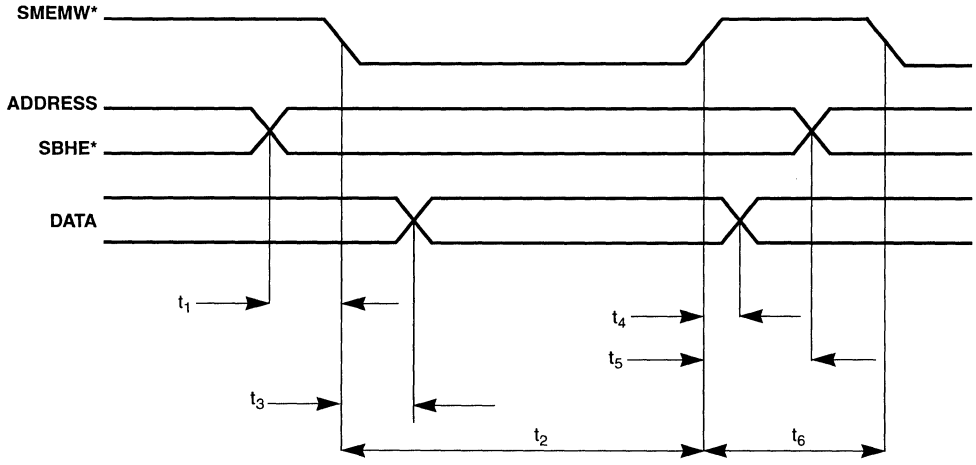


Figure 7–3. Memory Write Timing (ISA Bus)

Table 7–4. Memory Read Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	Address, SBHE* to SMEMR* Active	5	–	ns
t_2	SMEMR* Active to Low Impedance Delay	0	–	ns
t_3	Data Delay from IOCHRDY Active	–	15	ns
t_4	SMEMR* Pulse Width	–	[a]	ns
t_5	Data Hold from SMEMR* Inactive	0	20	ns
t_6	Address, SBHE* Hold from SMEMR* Inactive	0	–	ns
t_7	SMEMR* Inactive to High Impedance Delay	–	20	ns

[a] SMEMR* active-pulse width is determined by IOCHRDY.

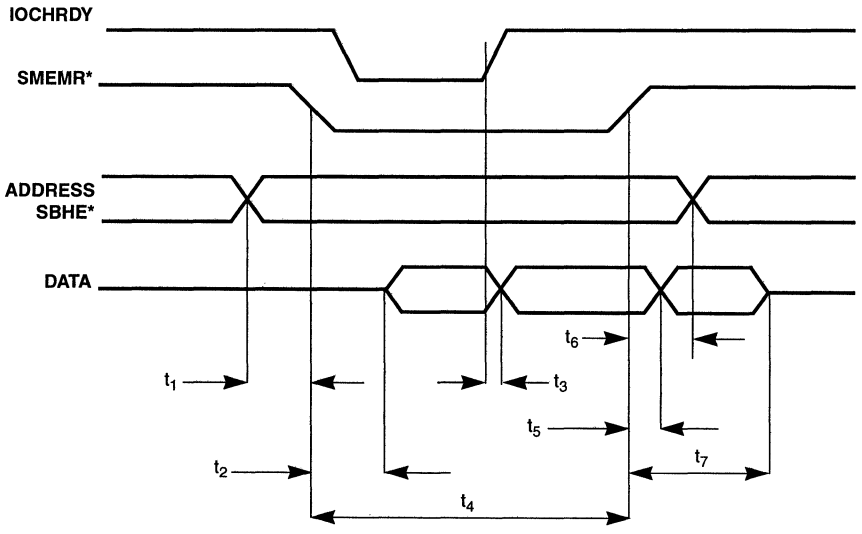


Figure 7–4. Memory Read Timing (ISA Bus)

Table 7–5. MCS16* Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Units
t_{1a}	MCS16* Active Delay from LA[23:17] Valid	–	20	ns
t_{1b}	MCS16* Active Delay from SA[16:15] Valid	–	14	ns
t_2	MCS16* Inactive Delay from Address Invalid	–	25	ns

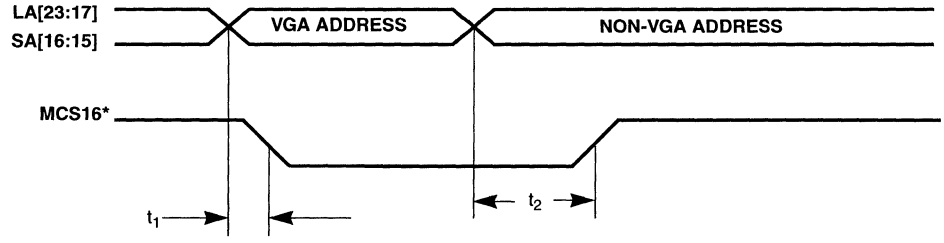


Figure 7–5. MCS16* Timing (ISA Bus)

Table 7–6. IOCS16* Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	IOCS16* Active Delay from Address	–	25	ns
t_2	IOCS16* Inactive Delay from Address	–	30	ns

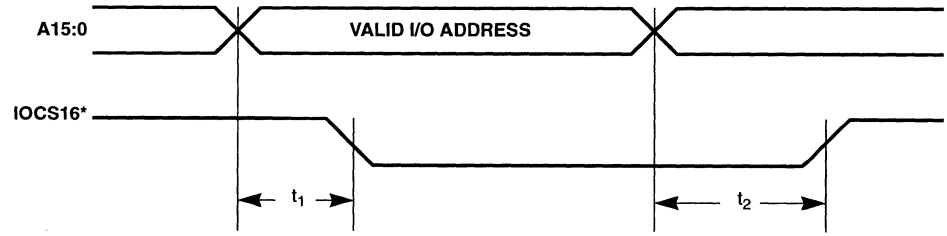


Figure 7–6. IOCS16* Timing (ISA Bus)

Table 7–7. BALE Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	LA23:17 Setup to BALE Negative Transition	20	–	ns
t_2	SBHE* Setup to BALE Negative Transition	20	–	ns
t_3	LA23:17 Hold from BALE Negative Transition	20	–	ns
t_4	SBHE* Hold from BALE Negative Transition	20	–	ns
t_5	BALE Pulse Width	20	–	ns

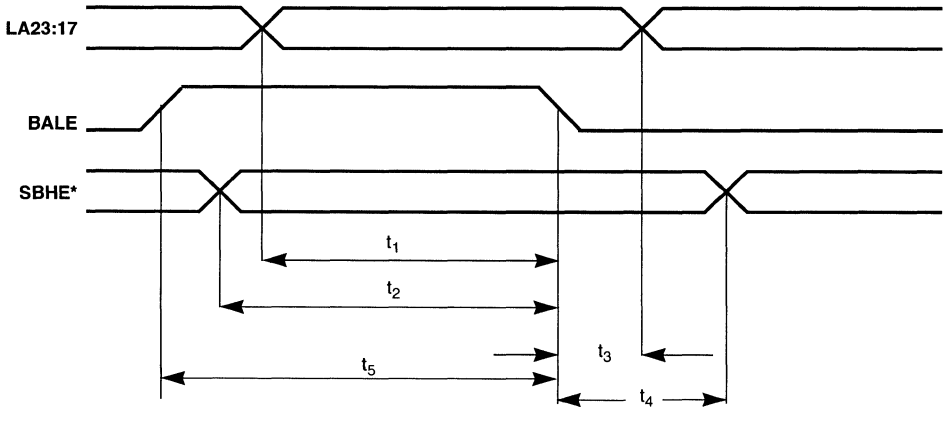


Figure 7–7. BALE Timing (ISA Bus)

Table 7–8. IOCHRDY for Memory Access Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	SMEMR* or SMEMW* Active to IOCHRDY Inactive LOW	–	28	ns
t_2	IOCHRDY Inactive Low Pulse Width	10	[a]	ns

[a] Video mode dependant.

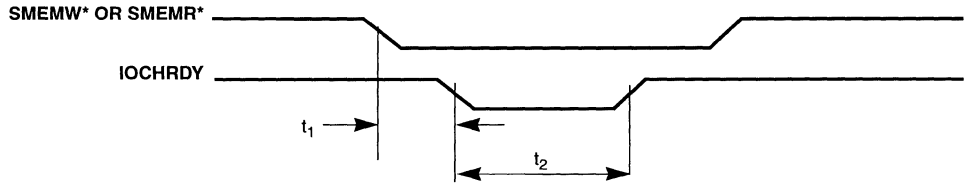


Figure 7–8. IOCHRDY for Memory Access Timing (ISA Bus)

Table 7–9. 0WS* Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Units
t_{1a}	0WS* Active Delay from SMEMR* (BIOS Access)	–	22	ns
t_{1b}	0WS* Active Delay from SMEMW* (Display Memory Write)	–	18	ns
t_{2a}	0WS* High Impedance Delay from SMEMR*	–	18	ns
t_{2b}	0WS* High Impedance Delay from SMEMW*	–	19	ns

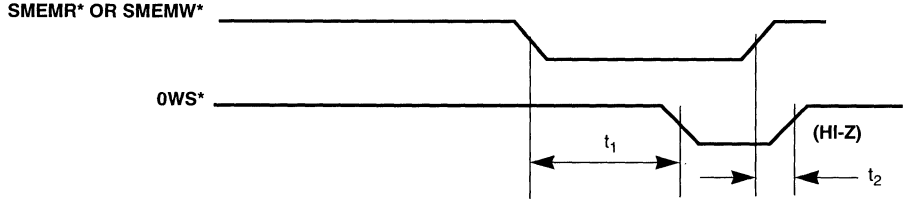


Figure 7–9. 0WS* Timing (ISA Bus)

Table 7–10. Refresh Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	REFRESH* Active Setup to SMEMR* Active	20	–	ns
t_2	REFRESH* Active Hold from SMEMR* Active	0	–	ns

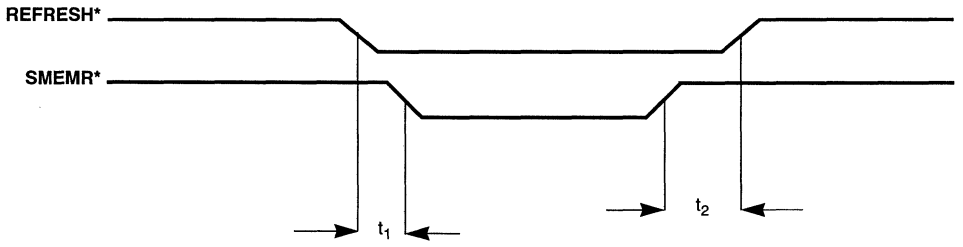


Figure 7–10. Refresh Timing (ISA Bus)

Table 7–11. EROM* Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	EROM* Active Delay from SMEMR* Active	–	30	ns
t_2	EROM* Inactive Delay from SMEMR* Inactive	–	20	ns

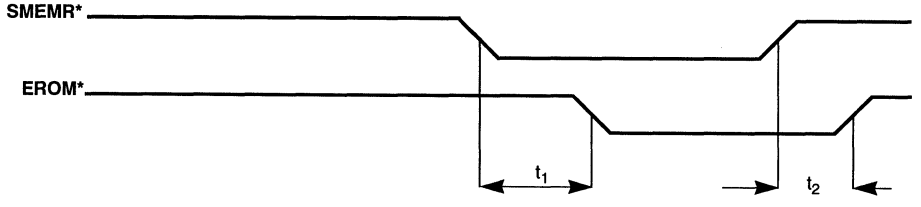


Figure 7–11. EROM* Timing (ISA Bus)

Table 7–12. AEN Timing (ISA Bus)[a]

Symbol	Parameter	MIN	MAX	Units
t_1	AEN Setup to IOR* or IOW* Active	5	–	ns
t_2	AEN Hold from IOR* or IOW* Inactive	5	–	ns

[a] AEN High, as shown below, will cause the CL-GD542X to **ignore** the I/O Cycle.

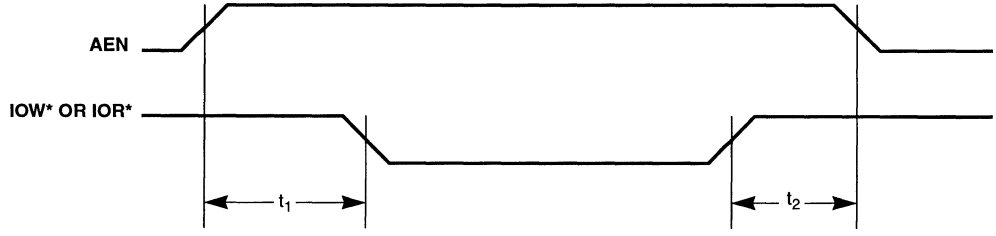


Figure 7–12. AEN Timing (ISA Bus)

Table 7–13. Write Timing (MicroChannel® Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	Data to -CMD Active Setup	-15	–	ns
t_{2a}	-CMD Active Pulse Width (Default Cycle)	90	–	ns
t_{2b}	-CMD Active Pulse Width (Synchronous Extended Cycle)	190	–	ns
t_{2c}	-CMD Active Pulse Width (Asynchronous Extended Cycle)	a	a	ns
t_3	Data Hold from -CMD Inactive	0	–	ns
t_4	CD_CHRDY Active to -CMD Inactive Delay	0	–	ns

[a]The maximum t_{2c} depends on Display Memory activity.

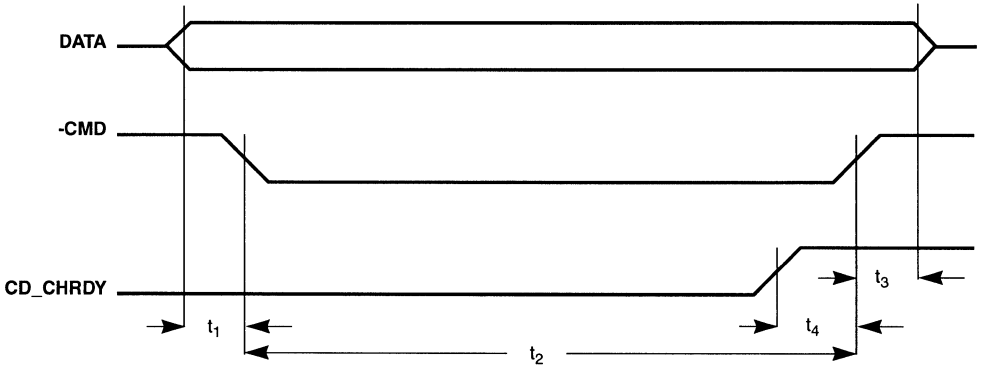


Figure 7–13. Write Timing (MicroChannel® Bus)

Table 7–14. Read Timing (MicroChannel® Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	-CMD Active to Data Valid Delay (Default Cycle) (I/O Read)	–	45	ns
t_2	CD_CHRDY Active to Data Valid Delay (Memory Read Cycle)	–	45	ns
t_3	Read Data Hold from -CMD Inactive	0	–	ns
t_4	Read Data High Impedance from -CMD Inactive	–	30	ns

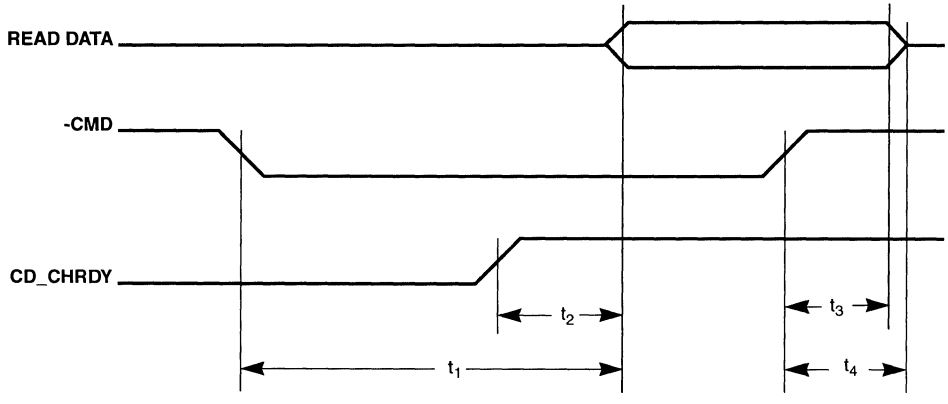


Figure 7–14. Read Timing (MicroChannel® Bus)

Table 7–15. -CD_DS16 Timing (MicroChannel® Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	-CD_DS16 Active from Address, M/-IO, MADE24 Valid	0	50	ns

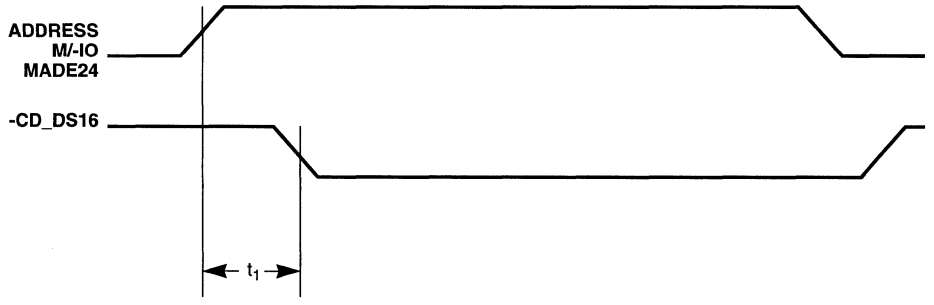


Figure 7–15. -CD_DS16 Timing (MicroChannel® Bus)

Table 7–16. -CMD Timing (MicroChannel® Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	Address Valid Setup to -CMD Active	80	–	ns
t_2	Status Active Setup to -CMD Active	50	–	ns
t_3	-SBHE Valid Setup to -CMD Active	35	–	ns
t_4	-CMD Pulse Width	90	–	ns
t_5	Address, -SBHE Hold from -CMD Active	25	–	ns
t_6	Status Hold from -CMD Active	25	–	ns

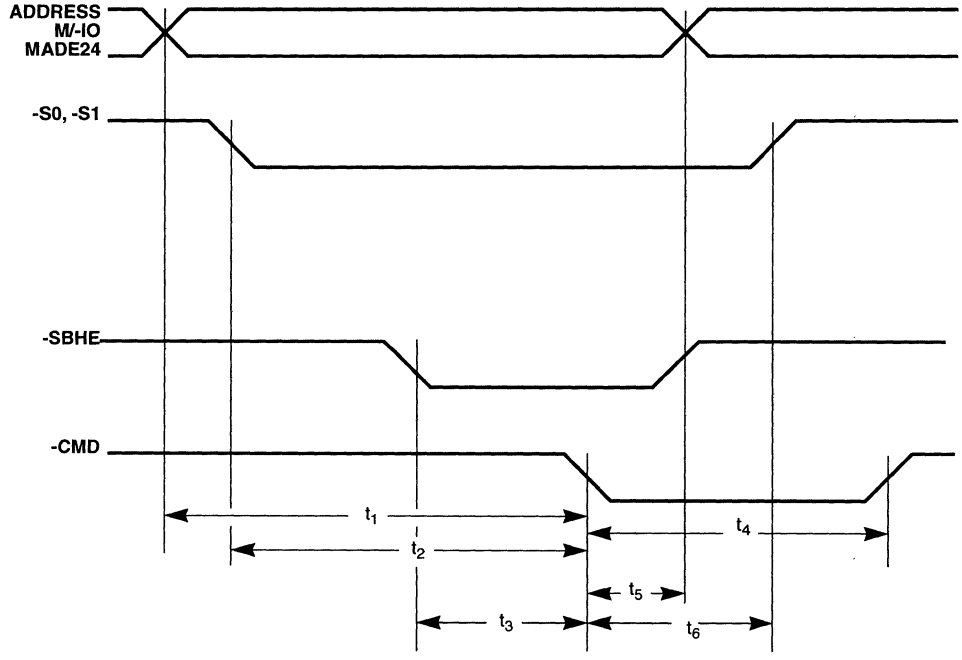


Figure 7–16. -CMD Timing (MicroChannel® Bus)

Table 7–17. CD_CHRDY Timing (MicroChannel® Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	CD_CHRDY Inactive (LOW) from Address Valid	–	50	ns
t_2	CD_CHRDY Inactive (LOW) from Status Active	–	25	ns
t_3	CD_CHRDY Inactive (LOW) Pulse Width	–	3.5	ms

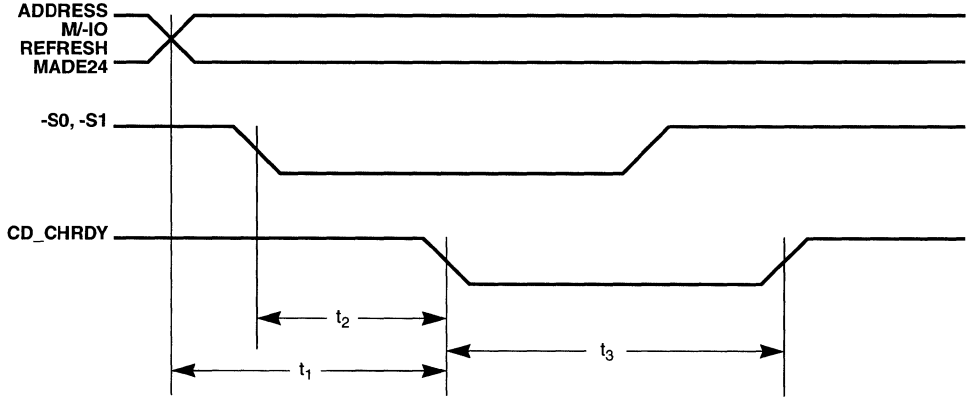


Figure 7–17. CD_CHRDY Timing (MicroChannel® Bus)

Table 7–18. -Refresh Timing (MicroChannel® Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	-REFRESH Setup to Status Active	5	–	ns
t_2	-REFRESH Setup to -CMD Active	40	–	ns
t_3	-REFRESH Hold from -CMD Active	25	–	ns

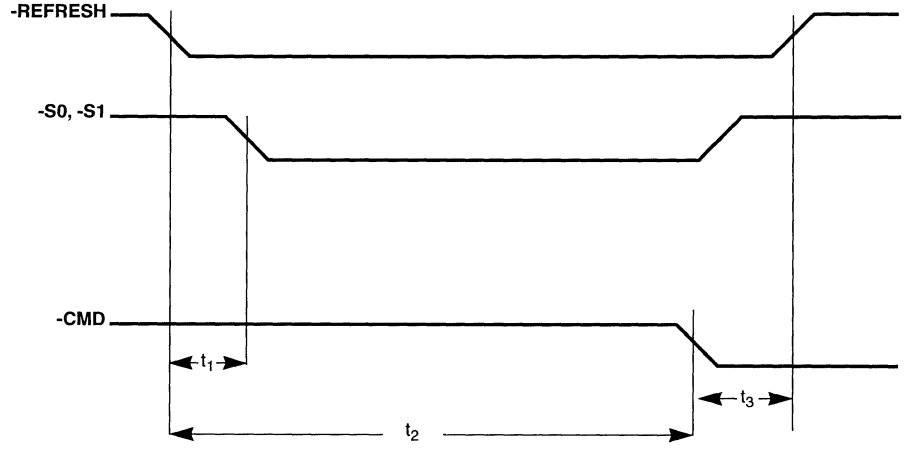


Figure 7–18. -Refresh Timing (MicroChannel® Bus)

Table 7–19. -EROM Timing (MicroChannel® Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	-CMD Active to -EROM Active	–	30	ns
t_2	-CMD Inactive to -EROM Inactive	0	30	ns

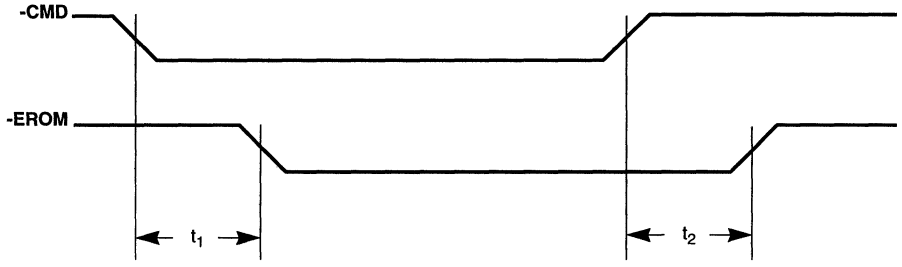


Figure 7–19. -EROM Timing (MicroChannel® Bus)

Table 7–20. -CD_SFDBK Timing (MicroChannel® Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	Address, M/-IO, MADE24 Valid to -CD_SFDBK Active Delay	–	55	ns
t_2	Address, M/-IO, MADE24 Invalid to -CD_SFDBK Inactive Delay	0	–	ns

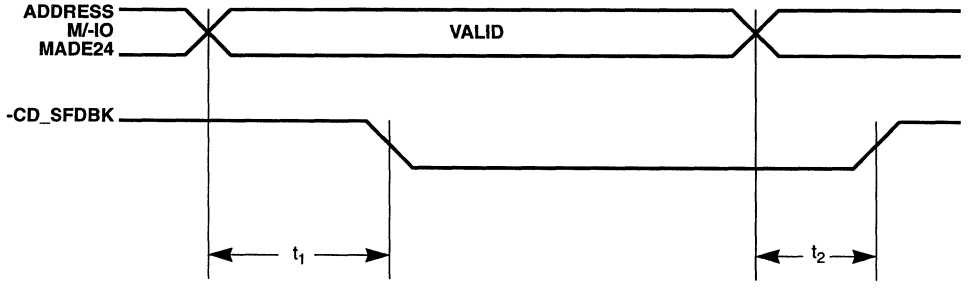


Figure 7–20. -CD_SFDBK Timing (MicroChannel® Bus)

Table 7–21. -CD_SETUP Timing (MicroChannel® Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	-CD_SETUP Active Setup to -CMD Active	10	–	ns
t_2	-CD_SETUP Delay to CD_CHRDY Inactive	–	95	ns
t_3	-CMD Active to -CD_SETUP Inactive Hold	25	–	ns

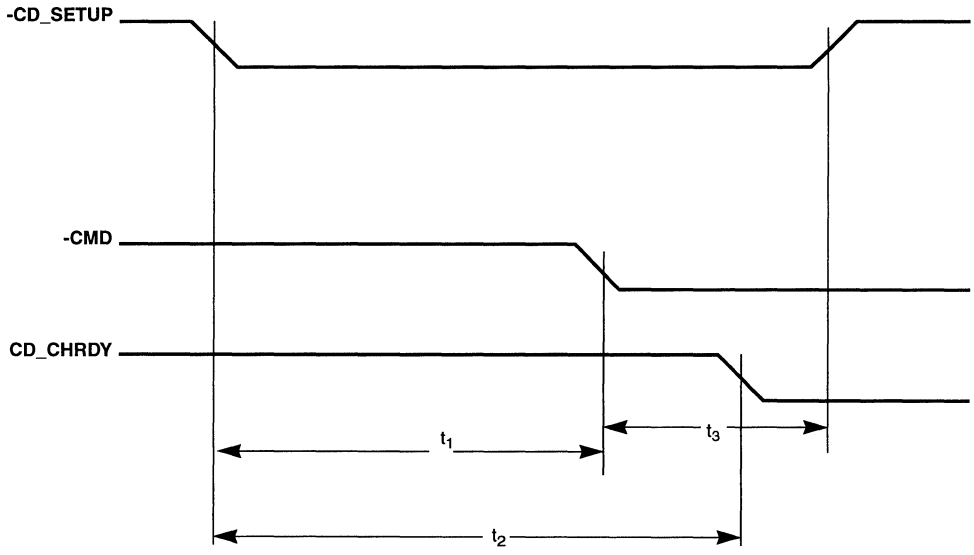


Figure 7–21. -CD_SETUP Timing (MicroChannel® Bus)

Table 7–22. CLK1X, CLK2X Timing (Local Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	Rise Time (CLK1X) '486 (V_{IL} - V_{IH})	–	4	ns
t_2	Fall Time (CLK1X) '486 (V_{IH} - V_{IL})	–	4	ns
t_3	High Period (CLK1X) '486 (V_{IH} - V_{IH})	40	60	% t_5
t_4	Low Period (CLK1X) '486 (V_{IL} - V_{IL})	40	60	% t_5
t_5	Period (CLK1X) '486	25	–	ns
t_5	Period (CLK1X) '486 (CL-GD5429)	20	–	ns
t_1	Rise Time (CLK2X) '386 (V_{IL} - V_{IH})	–	4	ns
t_2	Fall Time (CLK2X) '386 (V_{IH} - V_{IL})	–	4	ns
t_3	High Period (CLK2X) '386 (V_{IH} - V_{IH})	40	60	% t_5
t_4	Low Period (CLK2X) '386 (V_{IL} - V_{IL})	40	60	% t_5
t_5	Period (CLK2X) '386	12.5	–	ns

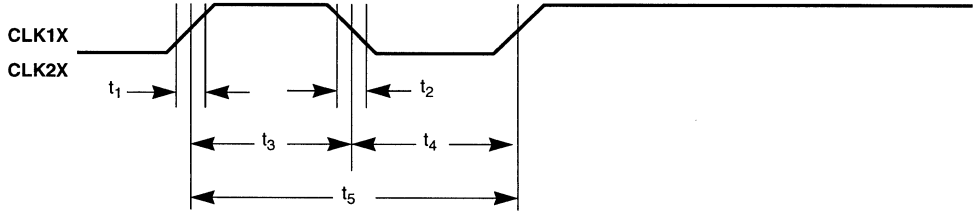


Figure 7–22. CLK1X, CLK2X Timing (Local Bus)

Table 7–23. Reset Timing (Local Bus)[a]

Symbol	Parameter	MIN	MAX	Units
t_1	CPU_Reset Hold time from CLK2X	10	–	ns
t_2	CPU_Reset Setup time to CLK2X	2	–	ns

[a] Applies to '386 only. For '486, pin 46 must be tied to Ground. For VESA VL-Bus, pin 46 must be tied to RDYRTN#.

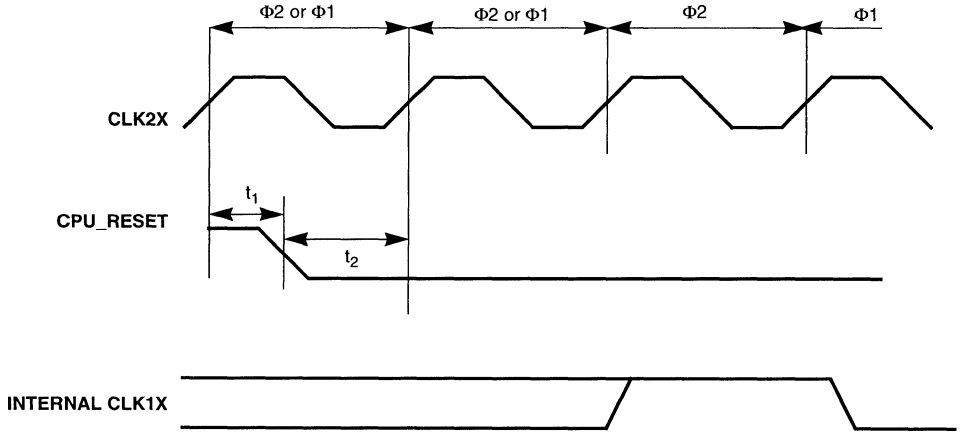


Figure 7–23. Reset Timing (Local Bus)

Table 7–24. ADS#, LBA#, BS16# Timing (Local Bus)

Symbol	Parameter	MIN	MAX	MIN 5429	MAX 5429	Units
t_1	Address, Status, ADS# Setup to CLK1X	8	–	4	–	ns
t_2	LBA#/LDEV# Active Delay from Address, Status	–	15	–	15	ns
t_3	BS16# Active Delay CLK1X	–	15	–	3	ns
t_4	LBA# Inactive Delay from Address, Status	–	18	–	18	ns

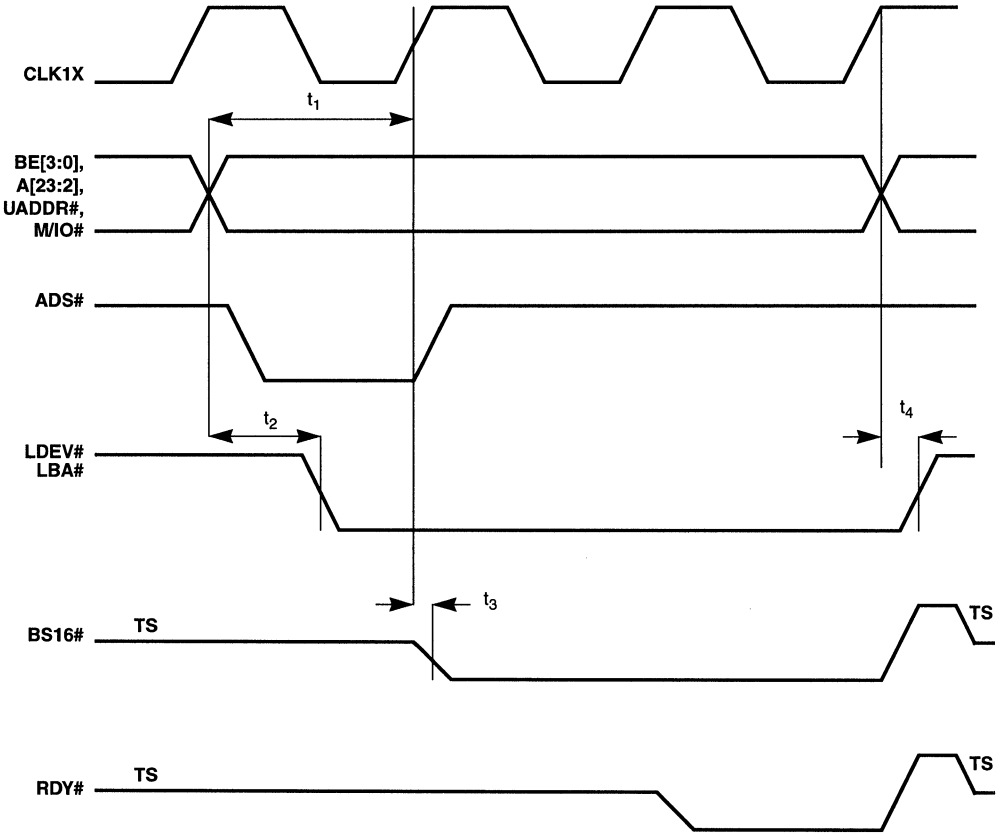


Figure 7–24. ADS#, LBA#, BS16# Timing (Local Bus)

Table 7–25. RDY# Delay (Local Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	RDY# Active Delay from CLK1X	3	13	ns
t_2	RDY# Inactive Delay from CLK1X	–	23	ns
t_3	RDY# High before HI-Z	–	1/2	CLK1X

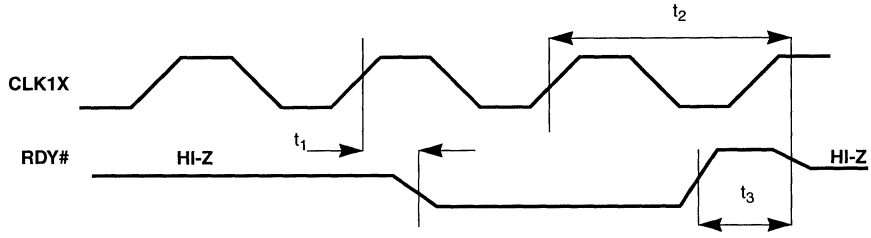


Figure 7–25. RDY# Delay (Local Bus)

Table 7–26. Read Data Timing (Local Bus)

Symbol	Parameter	MIN	MAX	MIN '5429	MAX '5429	Units
t_1	Read Data Setup to RDY# Active	0	–	0	–	ns
t_2	Read Data Hold from RDY# Inactive	12	–	12	–	ns
t_3	RDYRTN# Setup to CLK1X	8	–	5	–	ns
t_4	RDYRTN# Hold from CLK1X	5	–	2	–	ns

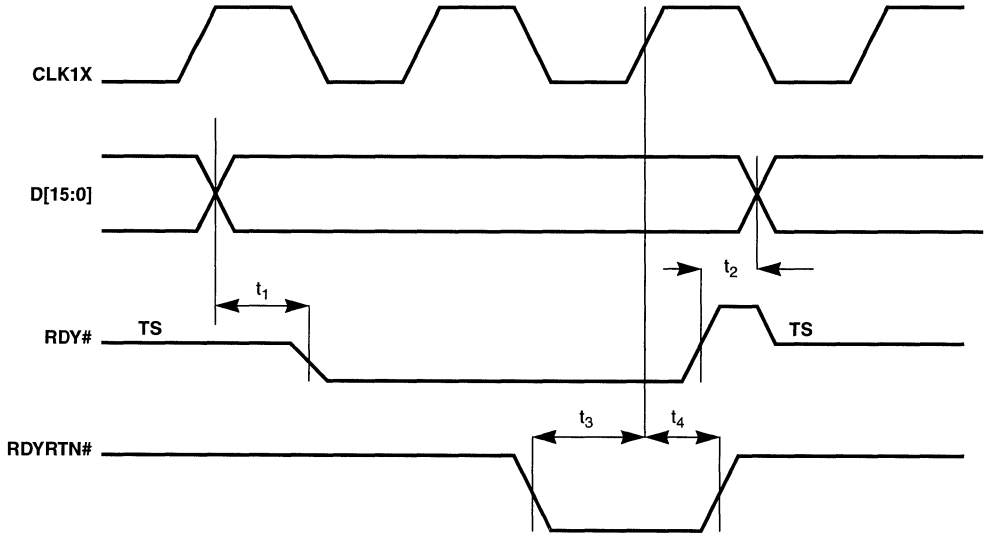
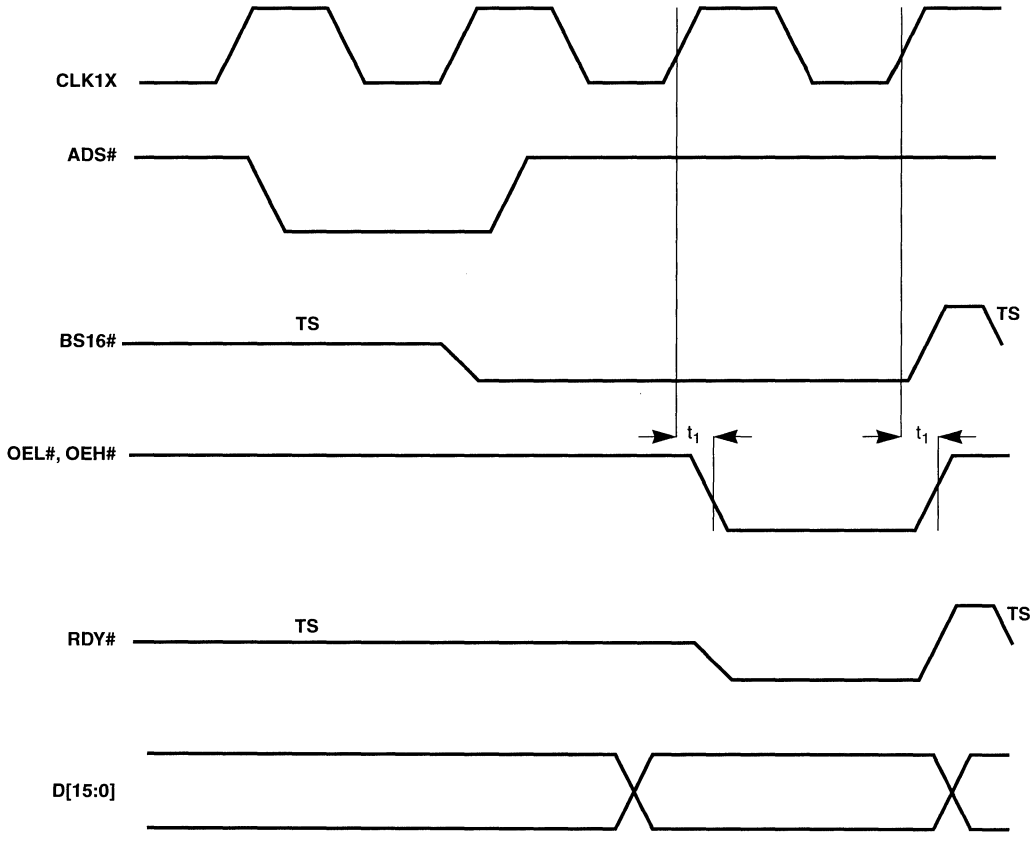


Figure 7–26. Read Data Timing (Local Bus)

Table 7–27. Buffer Control Timing: Read Cycle (Local Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	OEL#, OEH# Delay	0	14	ns

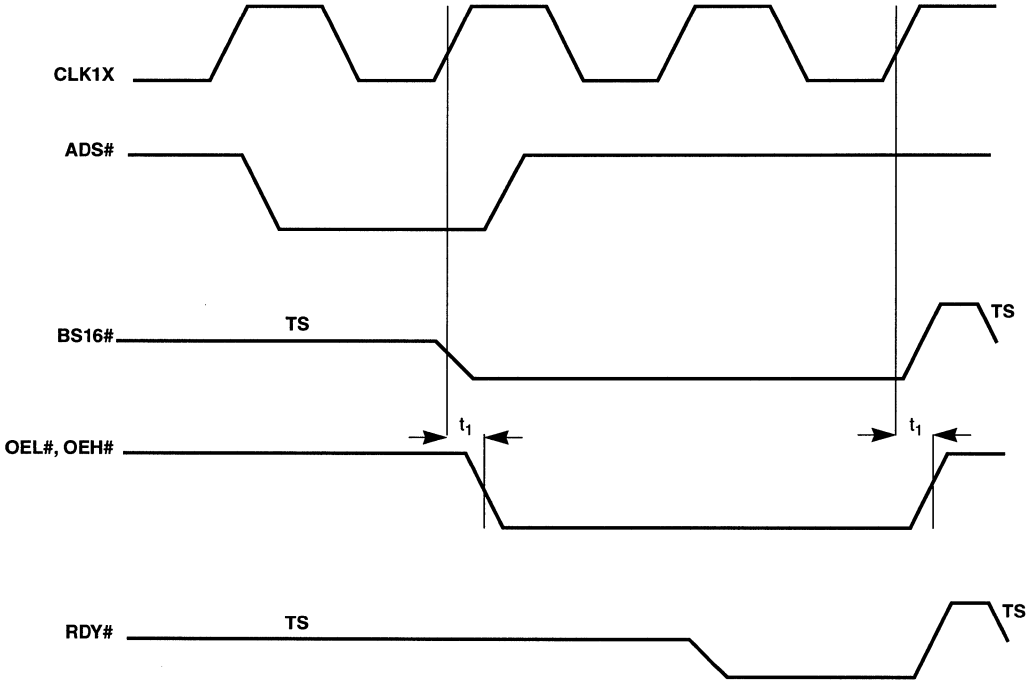


NOTE: Both OEL# and OEH# are active for read cycles.

Figure 7–27. Buffer Control Timing: Read Cycle (Local Bus)

Table 7–28. Buffer Control Timing: Write Cycle (Local Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	OEL#, OEH# Delay	0	14	ns



NOTE: Only one of OEL# and OEH# is active for write cycles.

Figure 7–28. Buffer Control Timing: Write Cycle (Local Bus)

Table 7–29. Read/Write Timing (Display Memory Bus) (t = MCLK)

Symbol	Parameter	MIN	MAX
t_1	t_{ASR}: Address Setup to RAS* Active	1.5t - 2 ns	–
t_2	t_{ASC}: Address Setup to CAS* Active	1t - 1 ns	–
t_3	t_{RCD}: RAS* Active to CAS* Active Delay (Standard RAS)	2.5t - 2 ns	–
t_3	t_{RCD}: RAS* Active to CAS* Active Delay (Extended RAS)	3t - 2 ns	–
t_4	t_{RAH}: Row Address Hold from RAS* Active	1.5t	–
t_5	t_{CAH}: Column Address Hold from CAS* Active	1t	–
t_7	WE* Inactive to OE* Active	1.5t - 2 ns	–
t_8	t_{RAC}: Data Valid from RAS* Active (Standard RAS)	–	4t - 1 ns
t_8	t_{RAC}: Data Valid from RAS* Active (Extended RAS)	–	4.5t - 1 ns
t_9	t_{CAC}: Data Valid from CAS* Active	–	1t + 3 ns
t_{10}	t_{AA}: Data Valid from Column Address Valid	–	2t
t_{12}	t_{RP}: RAS* Precharge (RAS* Pulse Width High) (Standard RAS)	2.5t - 2 ns	–
t_{12}	t_{RP}: RAS* Precharge (RAS* Pulse Width High) (Extended RAS)	3t	–
t_{13}	t_{RC}: Random Cycle (Standard RAS)	6t	–
t_{13}	t_{RC}: Random Cycle (Extended RAS)	7t	–
t_{14}	t_{RCH}: Read Command Hold from CAS* High	0.5t - 5 ns	–
t_{17}	t_{CP}: CAS* Precharge (CAS* Pulse Width High)	1t - 6 ns	1t - 3 ns
t_{18}	t_{CWL}: WE* Active Setup to CAS* Active	1t + 2 ns	–
t_{19}	t_{WCH}: WE* Active Hold from CAS* Active	1.5t	–
t_{20}	t_{WP}: WE* Active Pulse Width	2.5t - 2 ns	–
t_{21}	t_{DS}: Write Data Setup to CAS* Active	1t - 2 ns	1t + 2 ns
t_{22}	t_{DH}: Write Data Hold from CAS* Active	1t + 1 ns	–
t_{23}	t_T: Transition Time	2 ns	5 ns
t_{25}	t_{RAS}: RAS* Pulse Width Low (Standard RAS)	3.5t	–
t_{25}	t_{RAS}: RAS* Pulse Width Low (Extended RAS)	4t - 2 ns	–
t_{26}	t_{CAS}: CAS* Pulse Width Low	1t + 3 ns	1t + 6 ns
t_{27}	Read Data Setup to CAS* High	0 ns	–
t_{28}	Read Data Hold from CAS* High	10 ns	–
t_{29}	t_{PC}: Page Mode Cycle Time	2t	–

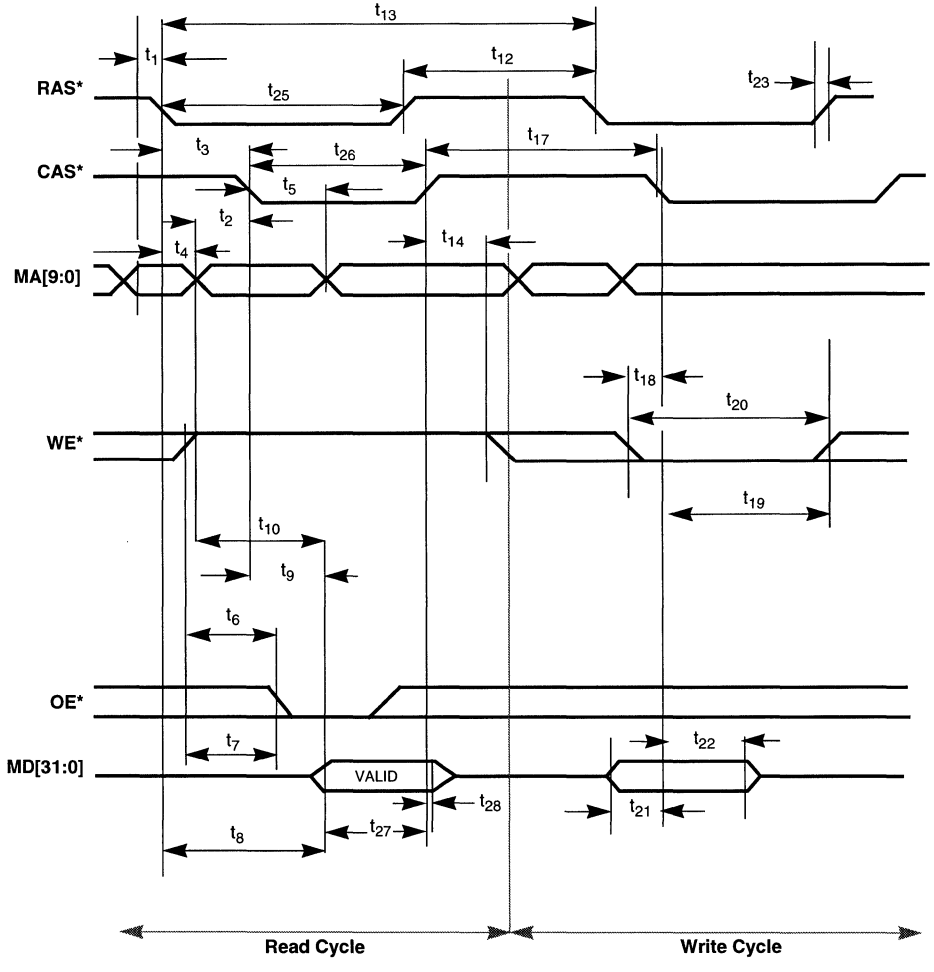


Figure 7–29. Read/Write Timing (Display Memory Bus) (t = MCLK)

Table 7–30. CAS*-before-RAS* Refresh Timing (Display Memory Bus)[a]

Symbol	Parameter	MIN	MAX
t_1	tCSR: CAS* Active Setup to RAS* Active1	1t	–
t_2	tRAS: RAS* Low Pulse Width	4t	–
t_3	tRP: RAS* High Pulse Width	3t	–

[a] There will be either three or five RAS* pulses while CAS* remains low.

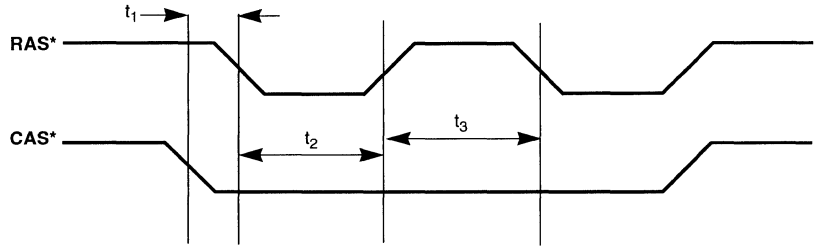


Figure 7–30. CAS*-before-RAS* Refresh Timing (Display Memory Bus)

Table 7–31. P-Bus as Inputs (8-bit Mode) (External DCLK)

Symbol	Parameter	MIN	MAX	Units
t_1	P[7:0], BLANK* Setup to DCLK	-1	–	ns
t_2	P[7:0], BLANK* Hold from DCLK	7	–	ns

NOTE: This is VESA Static Overlay mode.

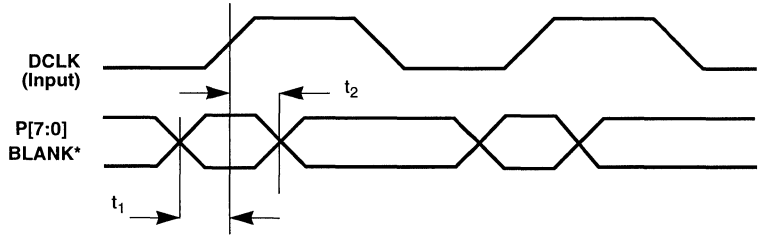


Figure 7–31. P-Bus as Inputs (8-bit Mode) External DCLK)

Table 7–32. Feature Bus Timing (Outputs) (Internal DCLK) (8-Bit Mode)

Symbol	Parameter	MIN	MAX	Units
t_1	DCLK to BLANK* Delay	-1	1	ns
t_2	DCLK to HSYNC, VSYNC Delay	1	3	ns
t_3	DCLK to P[7:0] Delay	-2	0	ns
t_4	DCLK to OVRW Delay	-1	1	ns

NOTE: This is VAFC Baseline Output.

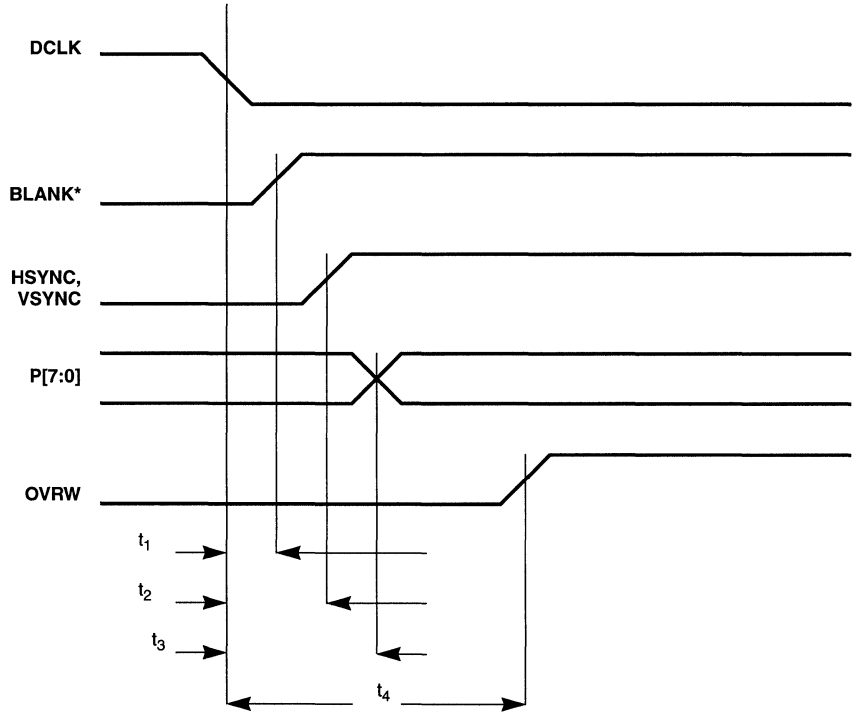


Figure 7–32. Feature Bus Timing (Outputs) (Internal DCLK) (8-Bit Mode)

Table 7–33. P-Bus as Outputs (16-bit Mode) (Internal DCLK) (CL-GD5428/'29 Only)

Symbol	Parameter	MIN	MAX	Units
t_1	DCLK (Rising Edge) to P[7:0] Delay	-2	0	ns
t_2	DCLK (Falling Edge) to P[7:0] Delay	-1	1	ns

NOTE: SR7[2:1] programmed to '0,1' and GRE[0] programmed to '1'.

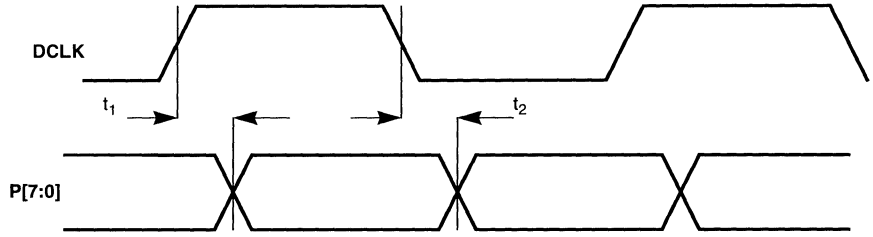


Figure 7–33. P-Bus as Outputs (16-bit Mode) (Internal DCLK) (CL-GD5428/'29 Only)

Table 7–34. P-Bus as Inputs (16-bit Mode) (External DCLK) (VAFC)

Symbol	Parameter	MIN CL-GD5428	MIN CL-GD5429	Units
t_1	P[7:0] Setup to DCLK (Rising Edge) (External DCLK)	-5	2	ns
t_2	P[7:0] Hold from DCLK (Rising Edge) (External DCLK)	6	2	ns
t_3	P[7:0] Setup to DCLK (Falling Edge) (External DCLK)	-3	2	ns
t_4	P[7:0] Hold from DCLK (Rising Edge) (External DCLK)	6	2	ns

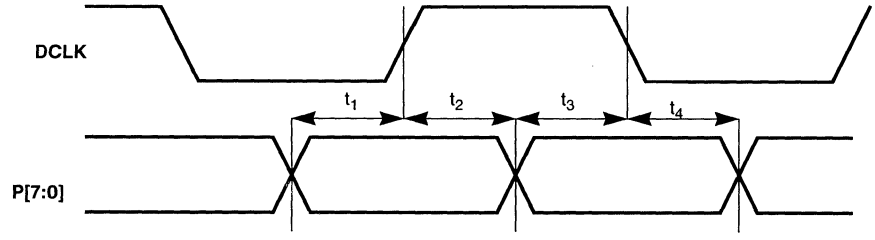


Figure 7–34. P-Bus as Inputs (16-bit Mode) (External DCLK) (VAFC)

Table 7–35. DCLK As Input

Symbol	Parameter	MIN	MAX	Units
t_1	Rise Time (DCLK)	–	3	ns
t_2	Fall Time (DCLK)	–	3	ns
t_3	High Period (DCLK)	40	60	% of t_5
t_4	Low Period (DCLK)	40	60	% of t_5
t_5	Period (DCLK)	17	–	ns

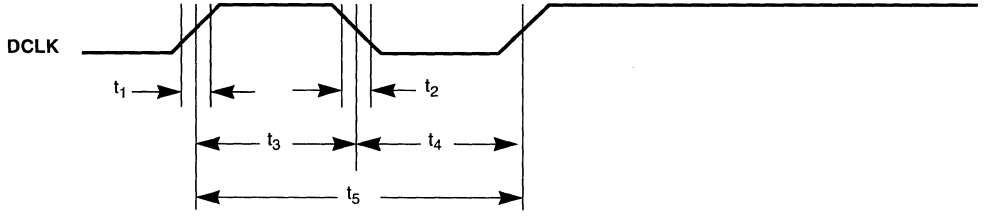


Figure 7–35. DCLK As Input

Table 7–36. Reset Timing

Symbol	Parameter	MIN	MAX	Units
t_1	Reset Pulse Width	12	–	MCLK
t_2	MD[31:16] Setup to Reset falling edge	2	–	ns
t_3	MD[31:16] Hold from Reset falling edge	25	–	ns
t_4	Reset Low to first IOW*	12	–	MCLK

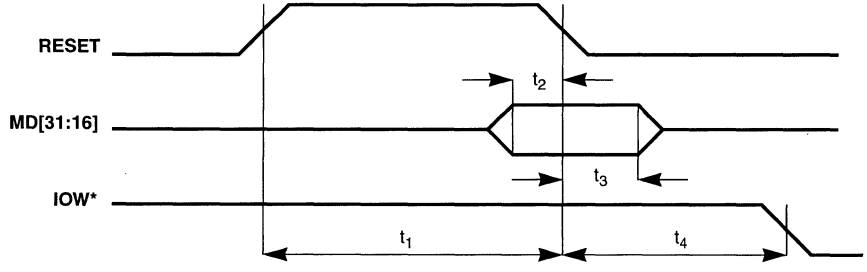
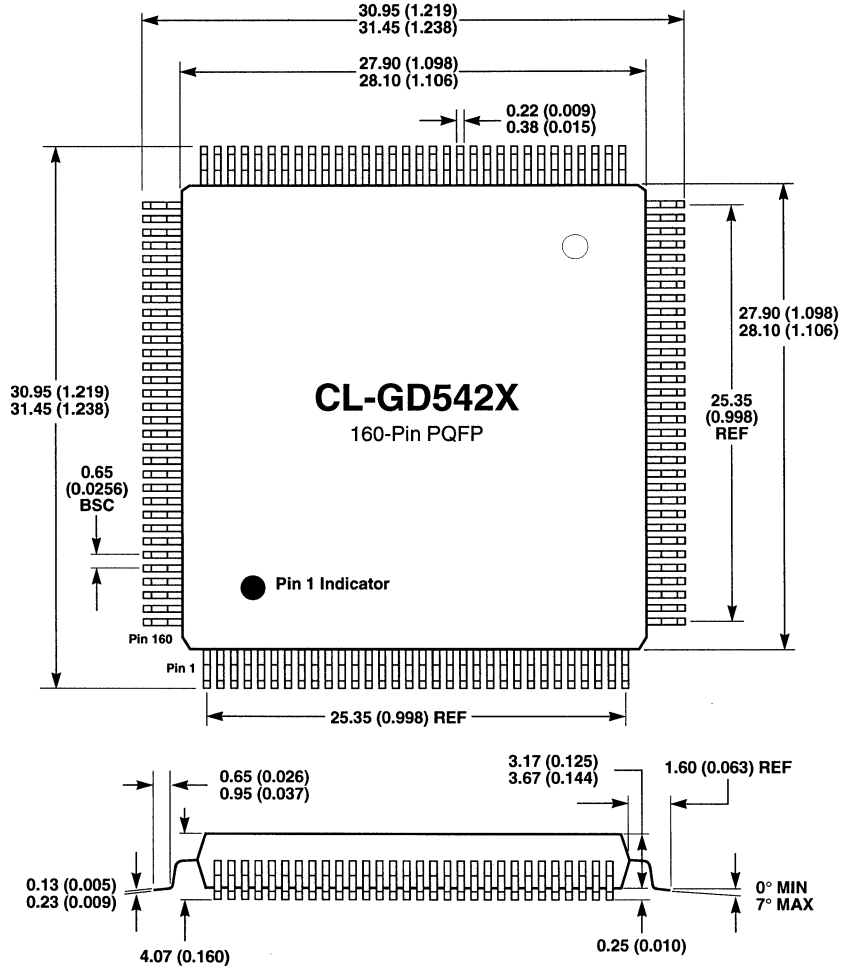


Figure 7–36. Reset Timing

8. PACKAGE DIMENSIONS

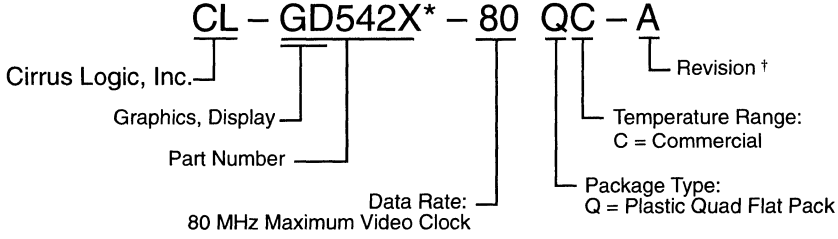


NOTES:

1) Dimensions are in millimeters (inches).
2) Drawing above does not reflect exact package pin count.
3) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.

9. ORDERING INFORMATION

9.1 CL-GD542X Package Marking Numbering Guide



† Contact Cirrus Logic, Inc. for up-to-date information on revisions.
* '2X' represents CL-GD5420/'22/'24/'26/'28/'29 respectively.

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345429-005

External and General Registers

4. EXTERNAL AND GENERAL REGISTERS

The External and General registers in the CL-GD542X are summarized in Table 4–1.

Table 4–1. External and General Registers Quick Reference

Abbreviation	Register Name	Index	Port	Page
102 Access	POS 102 Access Control	–	94	4 - 3
POS102	POS102	–	102	4 - 4
VSSM	Motherboard Sleep (CL-GD5424/'26/'28 only)	–	3C3	4 - 5
VSSM	Adapter Sleep	–	46E8	4 - 7
MISC	Miscellaneous Output	–	3C2 (write)	4 - 8
MISC	Miscellaneous Output	–	3CC (read)	4 - 8
FC	Feature Control	–	3?A (write)	4 - 10
FC	Feature Control	–	3CA (read)	4 - 10
FEAT	Input Status Register 0	–	3C2	4 - 11
STAT	Input Status Register 1	–	3?A	4 - 12
3C6	Pixel Mask	–	3C6	4 - 13
3C7	Pixel Address (Read mode)	–	3C7 (write)	4 - 14
3C7	DAC State	–	3C7 (read)	4 - 15
3C8	Pixel Address (Write mode)	–	3C8	4 - 16
3C9	Pixel Data	–	3C9	4 - 17

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

4.1 POS 94: 102 Access Control Register (Write only)

I/O Port Address: 94

Index: –

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	POS 102 Access	1
4	Reserved	
3	Reserved	
2	Reserved	
1	Reserved	
0	Reserved	

This register contains the enable bit for POS102. This register is accessible only if the CL-GD542X is configured for 3C3 sleep and for ISA or local bus. The register is not readable. When the CL-GD542X is configured for local bus, it will respond to writes to the register by latching the data, but will not generate LBA# or LRDY#.

Bit	Description
7:6	**Reserved**
5	**POS102 Access:** This bit controls access to POS102 if the CL-GD542X is configured for 3C3 sleep and is configured for ISA bus or local bus. If this bit is programmed to a '0', POS102 is accessible; if it is programmed to a '1', POS102 is not accessible. In addition, if this bit is programmed to a '0', the Video Subsystem Enable in 3C3 is overridden, and the CL-GD542X will remain in Sleep mode.
4:0	**Reserved**

4.2 POS102: POS102 Register

I/O Port Address: 102

Index: –

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	Reserved	
0	Video Subsystem Enable	0

This register contains a Video Subsystem Enable bit. This register is accessible if the CL-GD542X is configured for a Microchannel host and if -CD_SETUP was active when -ADL went active.

Bus Configuration	Sleep Address	Register Accessibility
ISA, local	46E8	46E8 [4] = 1
Local	3C3	3C3[4] = 1
Microchannel	Any	-CD_SETUP pin LOW

Bit	Description
7:1	**Reserved**
0	**Video Subsystem Enable:** If this bit is programmed to a '1', the CL-GD542X is enabled and operates normally if the VSE bit in 46E8 or 3C3 is also a '1'. If this bit is programmed to a '0', the CL-GD5420/'22 is disabled. It will not respond to any accesses except setup accesses to I/O Address 102. If this bit is programmed to a '0', the CL-GD5424/'26/'28 is disabled. It will not respond to any accesses except setup accesses to I/O Address 102 or 3C3.

4.3 VSSM: MicroChannel Sleep Address Register (CL-GD5424/'26/'28/'29 only)

I/O Port Address: 3C3

Index: –

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	Reserved	
0	Video Subsystem Enable	0

This is the Sleep Address for the MicroChannel VGA.

Bit	Description
7:1	**Reserved**
0	**Video Subsystem Enable:** If the CL-GD5424/'26/'28/'29 is not configured for MicroChannel, this bit cannot be accessed. If the CL-GD5424/'26/'28 is configured for MicroChannel, this bit has the following meaning: If this bit is programmed to a '1', the CL-GD5424/'26/'28/'29 is enabled and operates normally. If this bit is programmed to a '0', the CL-GD5424/'26/'28 is disabled; it will not respond to any I/O accesses except those addressed to 3C3. This bit will not respond to any accesses to display memory, but will respond normally to BIOS accesses. The video enable is unaffected.

4.4 VSSM: Motherboard Sleep Address Register (CL-GD5424/'26/'28/'29 only)

I/O Port Address: 3C3

Index: –

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Setup	0
3	Video Subsystem Enable	0
2	Reserved	
1	Reserved	
0	Reserved	

This is the Sleep Address for a motherboard VGA. This register can be accessed only if the CL-GD5424/'26/'28/'29 is configured for 3C3 Sleep Address. The CL-GD5424/'26/'28/'29 is configured for 3C3 Sleep Address, if CF[3] is a '0', and it is configured for local bus.

Bit	Description
7:5	**Reserved**
4	**Setup:** If this bit is programmed to a '1', the CL-GD542X is in Setup mode. In Setup mode, the resister at I/O Address 102 is accessible, and the register at 3C3 is accessible. The chip will respond normally to accesses to BIOS, but will not respond to accesses to display memory. If this bit is programmed to a '0', the chip is not in Setup mode and operates normally.
3	**Video Subsystem Enable:** If the CL-GD542X is not configured for 3C3 Sleep Address, this bit cannot be accessed. If the CL-GD542X is configured for 3C3 Sleep Address, this bit has the following meaning: If this bit is programmed to a '1', the CL-GD542X is enabled and operates normally. If this bit is programmed to a '0', the CL-GD542X is disabled; it will not respond to any I/O accesses except those addressed to 3C3 and 102. It will not respond to any accesses to display memory, but will respond normally to BIOS accesses. The video enable is unaffected.
2:0	**Reserved**

4.5 VSSM: Adapter Sleep Address Register (Write only)

I/O Port Address: 46E8

Index: –

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Setup	0
3	Video Subsystem Enable	0
2	Reserved	
1	Reserved	
0	Reserved	

This is the Sleep Address for an adapter VGA. This register can be accessed only if the CL-GD542X is configured for 46E8 Sleep Address. The CL-GD5420/'22 are always configured for 46E8 Sleep Address. The CL-GD5424/'26/'28/'29 are configured for 46E8 Sleep Address if CF[3] = 1. This register is write only.

Bit	Description
7:5	**Reserved**
4	**Setup:** If this bit is programmed to a '1', the CL-GD542X is in Setup mode. In Setup mode, the resister at I/O Address 102 is accessible, and the register at 46E8 is accessible. The chip will respond normally to accesses to BIOS, but will not respond to accesses to display memory. If this bit is programmed to a '0', the chip is not in Setup mode and operates normally.
3	**Video Subsystem Enable:** If the CL-GD542X is not configured for 46E8 Sleep Address, this bit cannot be accessed. If the CL-GD542X is configured for 46E8 Sleep Address, this bit has the following meaning: If this bit is programmed to a '1', the CL-GD542X is enabled and operates normally. If this bit is programmed to a '0', the CL-GD542X is disabled; it will not respond to any I/O accesses except those addressed to 46E8 and 102. It will not respond to any accesses to display memory, but will respond normally to BIOS accesses. The video enable is unaffected.
2:0	**Reserved**

4.6 MISC: Miscellaneous Output Register

I/O Port Address: 3C2 (write) 3CC (read)

Index: –

Bit	Description
7	Vertical Sync Polarity
6	Horizontal Sync Polarity
5	Page Select
4	Reserved
3	Clock Select [1]
2	Clock Select [0]
1	Enable Display Memory
0	CRTC I/O Address

This is one of the standard VGA registers with an assortment of bits that have nothing in common.

Bit **Description**

7 **Vertical Sync Polarity:** If this bit is programmed to a '0', the Vertical Sync will be a normally LOW signal, going HIGH to indicate the beginning of sync time. If this bit is programmed to a '1', the Vertical Sync will be a normally HIGH signal, going LOW to indicate the beginning of sync time.

6 **Horizontal Sync Polarity:** If this bit is programmed to a '0', the Horizontal Sync will be a normally LOW signal, going HIGH to indicate the beginning of sync time. If this bit is programmed to a '1', the Vertical Sync will be a normally HIGH signal, going LOW to indicate the beginning of sync time.

For some monitors, the polarity of Vertical and Horizontal Sync indicate the number of scanlines per frame. The following table summarizes this:

MISC[7]	MISC[6]	Vertical Size	Vertical Total
0 (+)	0 (+)	Reserved	Reserved
0 (+)	1 (-)	400	414
1 (-)	0 (+)	350	362
1 (-)	1 (-)	480	496

4.6 MISC: Miscellaneous Output Register *(cont.)*

Bit **Description**

5 **Page Select:** This bit affects the meaning of the LSB of display memory address when in Even/Odd modes (SR4[2]=1). If this bit is programmed to a '0', only odd memory locations are selected. If this bit is programmed to a '1', only even memory locations are selected.

NOTE: This bit is effective in modes 6, D, E, 11, and 12. This bit is ignored if Chain (GR6[1]) or Chain4 (SR4[3]) are enabled.

4 **Reserved**

3:2 **Clock Select:** This two-bit field is used to choose among the four VCLK frequencies, as shown in the following table:

EDCLK	MISC[3]	MISC[2]	VCLK Source	Default Frequency
1	0	0	VCLK0	25.180 MHz
1	0	1	VCLK1	28.325 MHz
1	1	0	VCLK2	41.165 MHz
1	1	1	VCLK3	36.082 MHz
0	1	X	DCLK pin (DAC and CRTC Counters)	
0	0	X	DCLK pin (DAC only)	

NOTE: Refer to Appendix B8 for programming additional VCLK frequencies.

1 **Enable Display Memory:** If this bit is programmed to a '0', the CL-GD542X will not respond to any accesses to display memory. If this bit is programmed to a '1', the CL-GD542X will respond normally to accesses to display memory.

0 **CRTC I/O Address:** This bit selects I/O addresses for either Monochrome or Color mode. The affected addresses are summarized in the table below:

MISC[0]	ISR/FC	CRTC Index	CRTC Data	Mode
0	3BA	3B4	3B5	Monochrome
1	3DA	3D4	3D5	Color

4.7 FC: Feature Control Register

I/O Port Address: 3?A (Write) 3CA (Read)

Index: –

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	VSYNC Control	0
2	Reserved	
1	Reserved	
0	Reserved	

This is one of the original IBM PC registers. Nearly all the bits are no longer used.

Bit	Description
7:4	**Reserved**
3	**VSYNC Control:** If this bit is programmed to a '1', VSYNC is logically OR'ed with Display Enable (an internal signal) prior to going to the VSYNC pin. If this bit is programmed to a '0', VSYNC is unchanged.
2:0	**Reserved**

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

4.8 FEAT: Input Status Register 0

I/O Port Address: 3C2

Index: –

Bit	Description
7	Interrupt Pending
6	Reserved
5	Reserved
4	DAC Sensing
3	Reserved
2	Reserved
1	Reserved
0	Reserved

The bits in this read-only register are nearly all undefined.

Bit	Description
7	**Interrupt Pending:** If this bit is a '1', an interrupt request is pending. If this bit is a '0', no interrupt is pending. See the description of CR11 for more information regarding the CL-GD542X interrupt system.
5	**Reserved**
4	**DAC Sensing:** This bit is used for DAC Sensing.
3:0	**Reserved**

4.9 STAT: Input Status Register 1

I/O Port Address: 3?A

Index: –

Bit	Description
7	Reserved
6	Reserved
5	Diagnostic [1]
4	Diagnostic [0]
3	Vertical Retrace
2	Reserved
1	Reserved
0	Display Enable

This read-only register contains some status bits.

Bit **Description**

7:6 **Reserved**

5:4 **Diagnostic [1:0]:** These bits follow two of eight outputs of the Attribute Controller. The selection is made according to AR12[5:4] (Color Plane Enable register) as indicated in the following table:

AR12[5]	AR12[4]	STAT[5]	STAT[4]
0	0	P[2] Red	P[0] Blue
0	1	P[5] Secondary Blue	P[4] Green
1	0	P[3] Secondary Red	P[1} Secondary Green
1	1	P[7]	P[6]

For the CL-GD5424/'26/'28/'29 only, these bits can reflect the Input Data on P[7:0]. This occurs only if P[7:0] are inputs as set by CR1A[3:2]. Refer to Application Note B14, *Video Overlay and DAC Mode Switching.*

3 **Vertical Retrace**: A '1' indicates that vertical retrace is in progress.

2:1 **Reserved**

0 **Display Enable:** If this bit is read as a '0', video is being serialized and displayed. If this bit is read as a '1', vertical or horizontal blanking is active.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

4.10 Pixel Mask Register

I/O Port Address: 3C6

Index: –

Bit	Description
7	Pixel Mask [7]
6	Pixel Mask [6]
5	Pixel Mask [5]
4	Pixel Mask [4]
3	Pixel Mask [3]
2	Pixel Mask [2]
1	Pixel Mask [1]
0	Pixel Mask [0]

The bits in this read register form the Pixel Mask for the palette DAC. This is typically programmed to all ones by the Cirrus Logic BIOS. The same address is used to access the Hidden DAC register which is described in Chapter 9, *Extension Registers*.

Bit	Description
7:0	**Pixel Mask [7:0]:** This field is the Pixel Mask for the palette DAC. If a bit in this field is programmed to a '0', the corresponding bit in the pixel data will be ignored in looking up an entry in the LUT.

4.11 Pixel Address Register (Read Mode) (Write only)

I/O Port Address: 3C7

Index: –

Bit	Description
7	Pixel Address (Read Mode) [7]
6	Pixel Address (Read Mode) [6]
5	Pixel Address (Read Mode) [5]
4	Pixel Address (Read Mode) [4]
3	Pixel Address (Read Mode) [3]
2	Pixel Address (Read Mode) [2]
1	Pixel Address (Read Mode) [1]
0	Pixel Address (Read Mode) [0]

The bits in this write-only register form the Pixel Address (Read mode) for the palette DAC. This is used to specify the entry in the LUT to be read.

Bit	Description
7:0	**Pixel Address (Read Mode) [7:0]:** This field is the Pixel Address (Read mode) for the Video LUT. This address is incremented at the conclusion of every third read of the Pixel Data register.

4.12 DAC State Register (Read only)

I/O Port Address: 3C7

Index: –

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Reserved
1	DAC State [1]
0	DAC State [0]

The bits in this read-only register indicate whether a read or write to the LUT occurred last.

Bit	Description
7:2	**Reserved**
1:0	**DAC State [1:0]:** This field indicates whether the Pixel Address Read register or the Pixel Address Write register was accessed last. The two bits will always be the same. If they are '0,0', a write operation is in progress. If they are '1,1', a read operation is in progress.

4.13 Pixel Address Register (Write Mode)

I/O Port Address: 3C8

Index: –

Bit	Description
7	Pixel Address (Write Mode) [7]
6	Pixel Address (Write Mode) [6]
5	Pixel Address (Write Mode) [5]
4	Pixel Address (Write Mode) [4]
3	Pixel Address (Write Mode) [3]
2	Pixel Address (Write Mode) [2]
1	Pixel Address (Write Mode) [1]
0	Pixel Address (Write Mode) [0]

The bits in this registers form the Pixel Address (Write mode) for the palette DAC. This is used to specify the entry in the LUT that is to be written.

Bit	Description
7:0	**Pixel Address (Write Mode) [7:0]:** This field is the Pixel Address (Write mode) for the Video LUT. This address is incremented at the conclusion of every third write to the Pixel Data register.

4.14 Pixel Data Register

I/O Port Address: 3C9

Index: –

Bit	Description
7	Pixel Data [7]
6	Pixel Data [6]
5	Pixel Data [5]
4	Pixel Data [4]
3	Pixel Data [3]
2	Pixel Data [2]
1	Pixel Data [1]
0	Pixel Data [0]

This is the Pixel Data for the palette DAC.

Bit	Description
7:0	**Pixel Data [7:0]**: This field is the Pixel Data for the palette DAC. This is a read/write register. Prior to writing to this register, 3C8 is written with the first or only pixel address. Then three values, corresponding to the Red, Green, and Blue values for the pixel are written to this address. Following the third write, the values are actually transferred to the LUT and the Pixel Address is incremented in case new values for the next pixel address are to be written. Prior to reading from this register, 3C7 is written with the first or only pixel address. Then three values, corresponding to the Red, Green, and Blue values for the pixel may be read from this address. Following the third read, the Pixel Address is incremented in case the value for the next pixel address are to be read.

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VGA Sequencer Registers

5. VGA SEQUENCER REGISTERS

The CL-GD542X VGA Sequencer registers are summarized in the following table. Please note that there are Extension registers that are accessed using the VGA Sequencer Ports.

Table 5–1. VGA Sequencer Registers Quick Reference

Abbreviation	Register Name	Index	Port	Page
SRX	Sequencer Index	–	3C4	5 - 3
SR0	Reset	0	3C5	5 - 4
SR1	Clocking Mode	1	3C5	5 - 5
SR2	Plane Mask	2	3C5	5 - 7
SR3	Character Map Select	3	3C5	5 - 8
SR4	Memory Mode	4	3C5	5 - 10

5.1 SRX: Sequencer Index Register

I/O Port Address: 3C4

Index: –

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Sequencer Index [4]
3	Sequencer Index [3]
2	Sequencer Index [2]
1	Sequencer Index [1]
0	Sequencer Index [0]

This register is used to specify the register in the sequencer block to be accessed by the next I/O Read or Write to Address 3C5. Indices greater than five point to registers that are defined in Chapter 9, *Extension Registers*.

Bit	Description
7:5	**Reserved**
4:0	**Sequencer Index [4:0]:** This field selects the register to be accessed with the next I/O Read or I/O Write to 3C5.

5.2 SR0: Reset Register

I/O Port Address: 3C5

Index: 0

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	Synchronous Reset	1
0	Asynchronous Reset	1

This register is used to reset the Sequencer. These bits are for compatibility only and need never be used in the CL-GD542X.

Bit	Description
7:2	**Reserved**
1	**Synchronous Reset:** If this bit is programmed to a '0', the sequencer will be cleared and halted. This disables screen refresh and display memory refresh. If this bit is programmed to a '1', the sequencer will operate normally, if SR0[0] is a '1'.
0	**Asynchronous Reset:** If this bit is programmed to a '0', the sequencer will be cleared and halted. In addition, SR3 will be cleared. If this bit is programmed to a '1', the sequencer will operate normally, if SR0[1] is a '1'.

5.3 SR1: Clocking Mode Register

I/O Port Address: 3C5

Index: 1

Bit	Description
7	Reserved
6	Reserved
5	Full Bandwidth
4	Shift and Load 32
3	Dot Clock ÷ 2
2	Shift and Load 16
1	Reserved
0	8/9 Dot Clock

This register is used to control some miscellaneous functions in the Sequencer.

Bit	Description
7:6	**Reserved**
5	**Full Bandwidth:** If this bit is programmed to a '1', screen refresh will stop. This allows the CPU to use nearly 100% of the display memory bandwidth. HSYNC and VSYNC will continue normally and display memory refresh will continue. BLANK* will go active and stay active (the DAC outputs will be zero). If this bit is programmed to a '0', the CL-GD542X will operate normally.
4	**Shift and Load 32:** This bit, in conjunction with bit 2 of this register, control the Display Data Shifters in the Graphics Controller according to the following table:
3	**Dot Clock ÷ 2:** If this bit is programmed to a '1', the VCLK is divided by two to generate DCLK. This is used for low-resolution Video modes such as 0, 1, 4, 5, and D. If this bit is programmed to a '0', the Master Clock is not divided by two.

SR1[4]	SR1[2]	Data Shifters Loaded
0	0	Every Character Clock
0	1	Every 2nd Character Clock
1	x	Every 4th Character Clock

5.3 SR1: Clocking Mode Register *(cont.)*

Bit	Description
2	**Shift and Load 16:** See the description of bit 4 of this register.
1	**Reserved**
0	**8/9 Dot Clock:** If this bit is programmed to a '1', DCLK is divided by eight to generate character clock. If this bit is programmed to a '0', DCLK is divided by nine to generate character clock. This is used for 720 x 350 and 720 x 400 resolution Text modes.

5.4 SR2: Plane Mask Register

I/O Port Address: 3C5

Index: 2

Bit	Description
7	Enable Writing Pixel 7
6	Enable Writing Pixel 6
5	Enable Writing Pixel 5
4	Enable Writing Pixel 4
3	Map 3 Enable/Enable Writing Pixel 3
2	Map 2 Enable/Enable Writing Pixel 2
1	Map 1 Enable/Enable Writing Pixel 1
0	Map 0 Enable/Enable Writing Pixel 0

This register is used to enable or disable writing to the four planes of display memory. If Extended Write modes 4 or 5 are selected, or if Write mode 1 is selected and GRB[1] = 1, this register is redefined as controlling the writing of up to eight pixels.

Bit	Description
7:4	**Reserved:** These four bits are reserved if Extended Write modes 4 and 5 are disabled. This would be the case for VGA compatibility modes.
3:0	**Map Enable [3:0]:** These four bits are used to individually control whether bit planes 3:0 will be written with Write modes 0 through 3.
7:0	**Enable Writing Pixel [7:0]:** These eight bits are used to individually control whether pixels 7:0 will be written if Extended Write modes 4 or 5 are selected, or if Write mode 1 is selected and GRB[2] = 1. Programming a '1' enables the corresponding pixel.

5.5 SR3: Character Map Select Register

I/O Port Address: 3C5

Index: 3

Bit	Description
7	Reserved
6	Reserved
5	Secondary Map Select [0]
4	Primary Map Select [0]
3	Secondary Map Select [2]
2	Secondary Map Select [1]
1	Primary Map Select [2]
0	Primary Map Select [1]

This register is used to specify the primary and secondary character sets (fonts). This is applicable to Text modes only.

Bit **Description**

7:6 **Reserved**

5, 3:2 **Secondary Map Select:** These three bits select the Secondary Character Map according to the following table:

SR3[5]	SR3[3]	SR3[2]	Map	Offset
0	0	0	0	0K
0	0	1	1	16K
0	1	0	2	32K
0	1	1	3	48K
1	0	0	4	8K
1	0	1	5	24K
1	1	0	6	40K
1	1	1	7	56K

5.5 SR3: Character Map Select Register *(cont.)*

Bit **Description**

4, 1:0 **Primary Map Select:** These three bits select the Primary Character Map according to the following table:

SR3[4]	SR3[1]	SR3[0]	Map	Offset
0	0	0	0	0K
0	0	1	1	16K
0	1	0	2	32K
0	1	1	3	48K
1	0	0	4	8K
1	0	1	5	24K
1	1	0	6	40K
1	1	1	7	56K

NOTES:

1) In Text Video modes, the ASCII text character is stored in Plane 0, the attribute is stored in Plane 1, and the font is stored in Plane 2.
2) Bit 3 of the Attribute byte normally controls the intensity of the foreground color. This bit may be redefined to be a switch between character sets, allowing 512 displayable characters. This switch is enabled whenever there is a difference between the values of the Primary Map Select and Secondary Map Select, and SR4[1] is a '1'.
3) The format of the Plane 2 Font Address bits 15:0 is:
   F2 F1 F0 C7 C6 C5 C4 C3 C2 C1 C0 R4 R3 R2 R1 R0,
   where F[2:0] is the Character Map Select, C[7:0] is the ASCII character, and R[4:0] is the Character Row (scanline in the character cell).

5.6 SR4: Memory Mode Register

I/O Port Address: 3C5

Index: 4

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Chain-4
2	Odd/Even
1	Extended Memory
0	Reserved

This register is used to control some miscellaneous functions in the Sequencer.

Bit	Description
7:4	**Reserved**
3	**Chain-4:** If this bit is programmed to a '1', A0 provides Plane Select bit 0, and A1 provides Plane Select bit 1. This has an effect similar to Odd/Even mode except that both A1 and A0 are used. This bit takes priority over SR4[2] (Odd/Even) and GR5[4]. There is not a separate bit in the Graphics Controller to select Chain4 as is the case with the Odd/Even bit. The Graphics Controller Read Map register (GR4) is ignored when this bit is a '1'.
2	**Odd/Even:** If this bit is programmed to a '0', the sequencer will be put into Odd/Even mode. Even CPU addresses will access Planes 0 and 2; odd CPU addresses will access Planes 1 and 3. This bit must be programmed to a '0' for text modes. The value of this bit must track GR5[4] (Odd/Even). The values will be opposite.
1	**Extended Memory:** If this bit is programmed to a '0', the effective memory size will be 64K, regardless of the memory actually installed. EGA modes require this to be the case. If this bit is programmed to a '1', the effective memory size will be equal to the actual memory installed.
0	**Reserved**

CRT Controller Registers

6. CRT CONTROLLER REGISTERS

The CL-GD542X VGA CRT Controller registers are summarized in the following table. Please note that there are Extension registers that are accessed using the VGA CRT Controller Ports.

While reading this chapter, refer to Figure 6–1 (page 6–5) and Table 6–2 (page 6–6) for a summary of CRTC registers.

Table 6–1. CRT Controller Registers Quick Reference

Abbreviation	Register Name	Index	Port	Page
CRX	CRTC Index	–	3?4	6 - 3
CR0	Horizontal Total	0	3?5	6 - 4
CR1	Horizontal Display End	1	3?5	6 - 7
CR2	Horizontal Blanking Start	2	3?5	6 - 8
CR3	Horizontal Blanking End	3	3?5	6 - 9
CR4	Horizontal Sync Start	4	3?5	6 - 11
CR5	Horizontal Sync End	5	3?5	6 - 12
CR6	Vertical Total	6	3?5	6 - 14
CR7	Overflow	7	3?5	6 - 15
CR8	Screen A Preset Row Scan	8	3?5	6 - 16
CR9	Character Cell Height	9	3?5	6 - 17
CRA	Text Cursor Start	A	3?5	6 - 18
CRB	Text Cursor End	B	3?5	6 - 19
CRC	Screen Start Address High	C	3?5	6 - 20
CRD	Screen Start Address Low	D	3?5	6 - 21
CRE	Text Cursor Location High	E	3?5	6 - 22
CRF	Text Cursor Location Low	F	3?5	6 - 23
CR10	Vertical Sync Start	10	3?5	6 - 24
CR11	Vertical Sync End	11	3?5	6 - 25
CR12	Vertical Display End	12	3?5	6 - 26
CR13	Offset	13	3?5	6 - 27
CR14	Underline Row Scanline	14	3?5	6 - 28
CR15	Vertical Blanking Start	15	3?5	6 - 29
CR16	Vertical Blanking End	16	3?5	6 - 30
CR17	Mode Control	17	3?5	6 - 31
CR18	Line Compare	18	3?5	6 - 33
CR22	Graphics Data Latches Readback	22	3?5	6 - 34
CR24	Attribute Controller Toggle Readback	24	3?5	6 - 35
CR26	Attribute Controller Index Readback	26	3?5	6 - 36

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.1 CRX: CRTC Index Register

I/O Port Address: 3?4

Index: –

Bit	Description
7	Reserved
6	Reserved
5	CRTC Index [5]
4	CRTC Index [4]
3	CRTC Index [3]
2	CRTC Index [2]
1	CRTC Index [1]
0	CRTC Index [0]

This register is used to specify the register in the CRTC Controller block to be accessed by the next I/O Read or I/O Write to Address 3?5. The registers at indices 19, 1A, 1B, 25, and 27 are described in Chapter 9, *Extension Registers*.

Bit	Description
7:6	**Reserved**
5:0	**CRTC Index [5:0]:** This value points to register to be accessed in the next I/O Read or I/O Write to address 3?5. Note that registers above 18 were actually never documented by IBM.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.2 CR0: Horizontal Total Register

I/O Port Address: 3?5

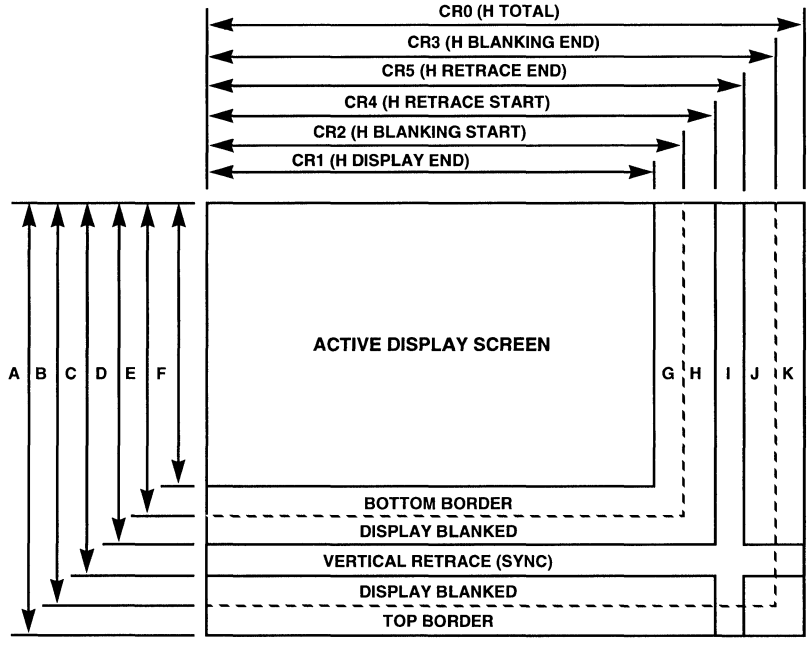
Index: 0

Bit	Description
7	Horizontal Total [7]
6	Horizontal Total [6]
5	Horizontal Total [5]
4	Horizontal Total [4]
3	Horizontal Total [3]
2	Horizontal Total [2]
1	Horizontal Total [1]
0	Horizontal Total [0]

This register is used to specify the total number of character clocks per horizontal period.

Bit	Description
7:0	**Horizontal Total:** This eight-bit field specifies the total number of character clocks per horizontal period. The Character Clock (derived from the VCLK according to the character width) is counted in the Character Counter. The value of the Character Counter is compared with the value in this register to provide the basic horizontal timing. All horizontal and vertical timing is eventually derived from the register. The value in the register is 'Total number of character times minus five'. Figure 6–1 indicates the way the horizontal and vertical timing is defined. The horizontal timing is calculated in terms of character clock periods and the vertical timing is calculated in terms of horizontal periods. Table 6–2 indicates how the various timing registers are extended.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.



A - CR6 (V TOTAL)
B - CR16 (V BLANKING END)
C - CR11 (V RETRACE END)
D - CR10 (V RETRACE START)
E - CR15 (V BLANKING START)
F - CR12 (V DISPLAY END)
G - RIGHT BORDER
H - DISPLAY BLANKED
I - HORIZONTAL RETRACE (SYNC)
J - DISPLAY BLANKED
K - LEFT BORDER

Figure 6–1. CRTC Timing Registers

The Extension And Overflow bits are organized by parameter and bit position in Table 6–2.

Table 6–2. Summary of CRTC Timing Registers[a]

Parameter/Bit	9	8	7	6	5	4:0
H Total			CR0[7]	CR0[6]	CR0[5]	CR0[4:0]
H Display End			CR1[7]	CR1[6]	CR1[5]	CR1[4:0]
H Blank Start			CR2[7]	CR2[6]	CR2[5]	CR2[4:0]
H Blank End			**CR1A[5]**	**CR1A[4]**	CR5[7]	CR3[4:0]
H Sync Start			CR4[7]	CR4[6]	CR4[5]	CR4[4:0]
H Sync End						CR5[4:0]
V Total	CR7[5]	CR7[0]	CR6[7]	CR6[6]	CR6[5]	CR6[4:0]
V Sync Start	CR7[7]	CR7[2]	CR10[7]	CR10[6]	CR10[5]	CR10[4:0]
V Sync End						CR11[3:0]
V Display End	CR7[6]	CR7[1]	CR12[7]	CR12[6]	CR12[5]	CR12[4:0]
V Blank Start	CR9[5]	CR7[3]	CR15[7]	CR15[6]	CR15[5]	CR15[4:0]
V Blank End	**CR1A[7]**	**CR1A[6]**	CR16[7]	CR16[6]	CR16[5]	CR16[4:0]
Line Compare	CR9[6]	CR7[4]	CR18[7]	CR18[6]	CR18[5]	CR18[4:0]
Offset		**CR1B[4]**	CR13[7]	CR13[6]	CR13[5]	CR13[4:0]

a. Bits shown in **bold** text are extensions.

6.3 CR1: Horizontal Display End Register

I/O Port Address: 3?5

Index: 1

Bit	Description
7	Horizontal Display End [7]
6	Horizontal Display End [6]
5	Horizontal Display End [5]
4	Horizontal Display End [4]
3	Horizontal Display End [3]
2	Horizontal Display End [2]
1	Horizontal Display End [1]
0	Horizontal Display End [0]

This register is used to specify the number of character clocks during horizontal display time.

Bit	Description
7:0	**Horizontal Display End [7:0]:** This register specifies the number of character clocks during horizontal display time. For text modes, this is the number of characters; for graphics modes, this is the number of pixels per scanlines divided by the number of pixels per character clock. The value in the register is the number of character clocks minus one. Refer to Figure 6–1 and Table 6–2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.4 CR2: Horizontal Blanking Start Register

I/O Port Address: 3?5

Index: 2

Bit	Description
7	Horizontal Blanking Start [7]
6	Horizontal Blanking Start [6]
5	Horizontal Blanking Start [5]
4	Horizontal Blanking Start [4]
3	Horizontal Blanking Start [3]
2	Horizontal Blanking Start [2]
1	Horizontal Blanking Start [1]
0	Horizontal Blanking Start [0]

This register is used to specify the Character Count where Horizontal Blanking starts.

Bit	Description
7:0	**Horizontal Blanking Start [7:0]:** The contents of this register specify the Character Count at which Horizontal Blanking starts. For text modes, this is the number of characters; for graphics modes, this is the number of pixels per scanline divided by the number of pixels per character clock. The value programmed into CR2 must always be larger than the value programmed into CR1. Refer to Figure 6–1 and Table 6–2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.5 CR3: Horizontal Blanking End Register

I/O Port Address: 3?5

Index: 3

Bit	Description
7	Compatible Read
6	Display Enable Skew [1]
5	Display Skew [0]
4	Horizontal Blanking End [4]
3	Horizontal Blanking End [3]
2	Horizontal Blanking End [2]
1	Horizontal Blanking End [1]
0	Horizontal Blanking End [0]

This register is used to determine the width of the Horizontal Blanking Period. In addition, this register controls Display Enable Skew and access to CR10 and CR11.

Bit	Description
7	**Compatible Read:** If this bit is programmed to a '0', registers CR10 and CR11 are write-only registers. If this bit is programmed to a '1', registers CR10 and CR11 are read/write registers.
6:5	**Display Enable Skew [1:0]:** This two-bit field is used to specify the number of Character Clocks that display enable is to be delayed from Horizontal Total. This is necessary to compensate for the accesses of the Character Code and Attribute byte, the accesses of the font, etc. The following table indicates the coding of CR3[6:5]:

CR3[6]	CR3[5]	Skew	Note
0	0	0	
0	1	1	Typical setting
1	0	2	
1	1	3	

NOTE: If the skew is programmed too low, the left most character will be repeated. If the skew is programmed too high, one or more characters will disappear at the left of each character row.

6.5 CR3: Horizontal Blanking End Register *(cont.)*

Bit	Description
4:0	**Horizontal Blanking End [4:0]:** This field determines the width of the Horizontal Blanking Period. This field is extended with CR5[7]. The least-significant five or six bits of the Character Counter are compared with the contents of this field. When a match occurs, the Horizontal Blanking Period is ended. Note that the Horizontal Blanking Period is limited to 63 character-clock times. The value to be programmed into this register may be calculated by subtracting the desired blanking period from the value programmed into CR2 (Horizontal Blanking Start). The Blanking period must never be programmed to extend past the Horizontal Total. If CR1B[5] or CR1B[7] is programmed to a '1', this field is extended with Extension register CR1A[5:4]. Refer to Figure 6–1 and Table 6–2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.6 CR4: Horizontal Sync Start Register

I/O Port Address: 3?5

Index: 4

Bit	Description
7	Horizontal Sync Start [7]
6	Horizontal Sync Start [6]
5	Horizontal Sync Start [5]
4	Horizontal Sync Start [4]
3	Horizontal Sync Start [3]
2	Horizontal Sync Start [2]
1	Horizontal Sync Start [1]
0	Horizontal Sync Start [0]

This register specifies the time at which Horizontal Sync becomes active.

Bit	Description
7:0	**Horizontal Sync Start [7:0]:** This field specifies the Character Count at which HSYNC (Horizontal Sync) becomes active. Adjusting the value in this field moves the display horizontally on the screen. The Horizontal Sync Start **must** be programmed to a value equal to or greater than Horizontal Display End. The time from Horizontal Sync Start to Horizontal Total **must** be equal to or greater than four character times. Refer to Figure 6–1 and Table 6–2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.7 CR5: Horizontal Sync End Register

I/O Port Address: 3?5

Index: 5

Bit	Description
7	Horizontal Blanking End [5]
6	Horizontal Sync Delay [1]
5	Horizontal Sync Delay [0]
4	Horizontal Sync End [4]
3	Horizontal Sync End [3]
2	Horizontal Sync End [2]
1	Horizontal Sync End [1]
0	Horizontal Sync End [0]

This register specifies the position at which the Horizontal Sync pulse ends, effectively specifying the width of the pulse. In addition, this register contains an overflow bit and a skew field.

Bit	Description
7	**Horizontal Blanking End [5]:** This bit extends the Horizontal Blanking End value by one bit. Refer to register CR3 for an explanation of the Horizontal Blanking End Value.
6:5	**Horizontal Sync Delay [1:0]:** This two-bit field is used to delay the external Horizontal Sync pulse from the position implied in CR4. This is necessary in some modes to allow internal timing signals triggered from Horizontal Sync Start to begin prior to Display Enable. The following table summarizes the HSYNC delay:

CR[6]	CR5[5]	Skew In Character Clocks
0	0	0
0	1	1
1	0	2
1	1	3

6.7 CR5: Horizontal Sync End Register *(cont.)*

Bit	Description
4:0	**Horizontal Sync End [4:0]:** This field determines the width of the Horizontal Sync pulse. The least-significant five bits of the Character Counter are compared with the contents of this field. When a match occurs, the Horizontal Sync pulse is ended. Note the Horizontal Sync pulse is limited to 31 character-clock times. The value to be programmed into this register may be calculated by subtracting the desired Sync width from the value programmed into CR4 (Horizontal Sync Start). The Sync pulse must never be programmed to extend past the Horizontal Total. In addition, HSYNC should always end during the Horizontal Blanking period. Refer to Figure 6–1 and Table 6–2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.8 CR6: Vertical Total Register

I/O Port Address: 3?5

Index: 6

Bit	Description
7	Vertical Total [7]
6	Vertical Total [6]
5	Vertical Total [5]
4	Vertical Total [4]
3	Vertical Total [3]
2	Vertical Total [2]
1	Vertical Total [1]
0	Vertical Total [0]

This register specifies the total number of scanlines per frame.

Bit	Description
7:0	**Vertical Total [7:0]:** This field is the low-order eight bits of a ten-bit field that defines the total number of scanlines per frame. This field is extended with CR5[7] and CR5[0]. The value programmed into the Vertical Total field is the total number of scanlines minus two. Refer to Figure 6–1 and Table 6–2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.9 CR7: Overflow Register

I/O Port Address: 3?5

Index: 7

Bit	Description
7	Vertical Sync Start [9]
6	Vertical Display End [9]
5	Vertical Total [9]
4	Line Compare [8]
3	Vertical Blanking Start [8]
2	Vertical Sync Start [8]
1	Vertical Display End [8]
0	Vertical Total [8]

This register contains bits that extend various vertical count fields. Refer to Figure 6–1 and Table 6–2 for a summary of CRTC Timing registers.

Bit	Description
7	**Vertical Retrace Start [9]:** This bit extends the Vertical Retrace Start (CR10) field to ten bits.
6	**Vertical Display End [9]:** This bit extends the Vertical Display End (CR12) field to ten bits.
5	**Vertical Total [9]:** This bit extends the Vertical Total (CR6) field to ten bits.
4	**Line Compare [8]:** This bit extends the Line Compare (CR18) field to nine bits.
3	**Vertical Blanking Start [8]:** This bit extends the Vertical Blanking Start (CR15) field to nine bits.
2	**Vertical Retrace Start [8]:** This bit extends the Vertical Retrace Start (CR10) field to nine bits.
1	**Vertical Display End [8]:** This bit extends the Vertical Display End (CR12) field to nine bits.
0	**Vertical Total [8]:** This bit extends the Vertical Total (CR6) field to nine bits.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.10 CR8: Screen A Preset Row Scan Register

I/O Port Address: 3?5

Index: 8

Bit	Description
7	Reserved
6	Byte Pan [1]
5	Byte Pan [0]
4	Screen A Preset Row Scan [4]
3	Screen A Preset Row Scan [3]
2	Screen A Preset Row Scan [2]
1	Screen A Preset Row Scan [1]
0	Screen A Preset Row Scan [0]

This register specifies the row scanline at which Screen A begins, allowing scrolling on a scanline basis (soft scroll). In addition, this register specifies the Byte Pan (coarse panning).

Bit **Description**

7 **Reserved**

6:5 **Byte Pan [1:0]:** This two-bit field controls coarse panning. It can specify a pan of up to 24 pixels with a resolution of eight pixels. AR13 provides for panning on a pixel basis. The values programmed into CR8[6:5] are interpreted as indicated in the following table:

CR8[6]	CR8[5]	Bytes	Pixels
0	0	0	0
0	1	1	8
1	0	2	16
1	1	3	24

4:0 **Screen A Preset Row Scan [4:0]:** This field specifies the scanline at which the first character row will begin. This provides scrolling on a scanline basis (soft scrolling). The contents of this field should be changed only during Vertical Retrace time.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.11 CR9: Character Cell Height Register

I/O Port Address: 3?5

Index: 9

Bit	Description
7	CRTC Scan Double
6	Line Compare [9]
5	Vertical Blank Start [9]
4	Character Cell Height [4]
3	Character Cell Height [3]
2	Character Cell Height [2]
1	Character Cell Height [1]
0	Character Cell Height [0]

This register specifies the number of scanlines in the character cell. In addition, it contains two vertical overflow bits and one control bit.

Bit	Description
7	**CRTC Scan Double:** If this bit is programmed to a '1', every scanline is displayed twice in succession. The Scanline Counter-based addressing (Character Height, Cursor Start and End, and Underline location) double. This bit is typically used to display 200-line modes at 400 scanlines. This function is not available in interlaced video modes.
6	**Line Compare [9]:** This bit extends the Line Compare field (CR18) to ten bits.
5	**Vertical Blank Start [9]:** This bit extends the Vertical Blank Start field (CR15) to ten bits.
4:0	**Character Cell Height [4:0]:** This field specifies the vertical size of the character cell in terms of scanlines. The value programmed into this field is the actual size minus 1. Refer to Figure 6–1 and Table 6–2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.12 CRA: Text Cursor Start Register

I/O Port Address: 3?5

Index: A

Bit	Description
7	Reserved
6	Reserved
5	Disable Text Cursor
4	Text Cursor Start [4]
3	Text Cursor Start [3]
2	Text Cursor Start [2]
1	Text Cursor Start [1]
0	Text Cursor Start [0]

This register specifies the scanline at which the text cursor is to begin. In addition, this register contains a bit that will disable the text cursor.

Bit	Description
7:6	**Reserved**
5	**Disable Text Cursor:** If this bit is programmed to a '1', the text cursor will be disabled (that is, it will be removed). If this bit is programmed to a '0', the text cursor will function normally.
4:0	**Text Cursor Start [4:0]:** This field specifies the scanline within the Character Cell at which the text cursor is to start. If the Text Cursor Start value is greater than the Text Cursor End value, there will be no text cursor displayed. If the Text Cursor Start value is equal to the Text Cursor End value, the text cursor will occupy a single scanline.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.13 CRB: Text Cursor End Register

I/O Port Address: 3?5

Index: B

Bit	Description
7	Reserved
6	Text Cursor Skew [1]
5	Text Cursor Skew [0]
4	Text Cursor End [4]
3	Text Cursor End [4]
2	Text Cursor End [4]
1	Text Cursor End [4]
0	Text Cursor End [4]

This register specifies the scanline within the Character Cell at which the Text Cursor is to end. It also contains a field that allows the Text Cursor to be skewed from the location specified in CRE and CRF.

Bit	Description
7	**Reserved**
6:5	**Text Cursor Skew [1:0]:** This two-bit field specifies a delay, in Character Clocks, from the Text Cursor Location specified in CRE and CRF to the actual cursor.
4:0	**Text Cursor End [4:0]:** This field specifies the scanline within the Character at which the Text Cursor is to end. A value greater than the Character Cell Height will yield an effective ending value equal to the Cell Height.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.14 CRC: Screen Start Address High Register

I/O Port Address: 3?5

Index: C

Bit	Description
7	Screen Start A Address [15]
6	Screen Start A Address [14]
5	Screen Start A Address [13]
4	Screen Start A Address [12]
3	Screen Start A Address [11]
2	Screen Start A Address [10]
1	Screen Start A Address [9]
0	Screen Start A Address [8]

This register, and CRD, specify the location in display memory at which the data to be displayed on the screen begins.

Bit	Description
7:0	**Screen Start A Address [15:8]:** The Screen Start A field specifies the location in display memory at which the screen begins. This register contains bits 15:8 of this value; bits 7:0 are in register CRD; bits 17:16 are in CR1B. Refer to Figure 6–1 and Table 6–2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.15 CRD: Screen Start Address Low Register

I/O Port Address: 3?5

Index: D

Bit	Description
7	Screen Start A Address [7]
6	Screen Start A Address [6]
5	Screen Start A Address [5]
4	Screen Start A Address [4]
3	Screen Start A Address [3]
2	Screen Start A Address [2]
1	Screen Start A Address [1]
0	Screen Start A Address [0]

This register, and CRC, specify the location in display memory at which the data to be displayed on the screen begins.

Bit	Description
7:0	**Screen Start A Address [7:0]:** The Screen Start A field specifies the location in display memory at which the screen begins. This register contains bits 7:0 of this value; bits 15:8 are in register CRC; bits 18:16 are in CR1B. Refer to Figure 6–1 and Table 6–2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.16 CRE: Text Cursor Location High Register

I/O Port Address: 3?5

Index: E

Bit	Description
7	Text Cursor Location [15]
6	Text Cursor Location [14]
5	Text Cursor Location [13]
4	Text Cursor Location [12]
3	Text Cursor Location [11]
2	Text Cursor Location [10]
1	Text Cursor Location [9]
0	Text Cursor Location [8]

This register, with CRF, specifies the location in display memory at which the Text Cursor is to be displayed.

Bit	Description
7:0	**Text Cursor Location [15:8]:** The Text Cursor Location is a 16-bit field that specifies the location in display memory at which the Text Cursor is to be displayed. This register contains bits 15:8 of this field; CRF contains bits 7:0. **NOTE:** The value contained in this field is an address in display memory, not an offset from the beginning of the screen. If the value of Screen A Start is changed without a compensating change in the Text Cursor Location field, the Text Cursor will move on the screen. Refer to Figure 6–1 and Table 6–2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.17 CRF: Text Cursor Location Low Register

I/O Port Address: 3?5

Index: F

Bit	Description
7	Text Cursor Location [7]
6	Text Cursor Location [6]
5	Text Cursor Location [5]
4	Text Cursor Location [4]
3	Text Cursor Location [3]
2	Text Cursor Location [2]
1	Text Cursor Location [1]
0	Text Cursor Location [0]

This register, with CRE, specifies the location in display memory at which the Text Cursor is to be displayed.

Bit	Description
7:0	**Text Cursor Location [7:0]:** The Text Cursor Location is a 16-bit field that specifies the location in display memory at which the Text Cursor is to be displayed. This register contains bits 7:0 of this field. Refer to Figure 6–1 and Table 6–2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.18 CR10: Vertical Sync Start Register

I/O Port Address: 3?5

Index: 10

Bit	Description
7	Vertical Sync Start [7]
6	Vertical Sync Start [6]
5	Vertical Sync Start [5]
4	Vertical Sync Start [4]
3	Vertical Sync Start [3]
2	Vertical Sync Start [2]
1	Vertical Sync Start [1]
0	Vertical Sync Start [0]

The Vertical Sync Start field specifies the scanline at which the Vertical Sync pulse will become active. This register contains the low-order eight bits of that field.

Bit	Description
7:0	**Vertical Sync Start [7:0]:** The Vertical Sync field specifies the scanline at which the Vertical Sync pulse will become active. This register contains bits 7:0 of that field. This register is extended by bits in CR7. Refer to Figure 6–1 and Table 6–2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.19 CR11: Vertical Sync End Register

I/O Port Address: 3?5

Index: 11

Bit	Description
7	Write Protect CR7-CR0
6	Refresh Cycle Control
5	Disable Vertical Interrupt
4	Clear Vertical Interrupt
3	Vertical Sync End [3]
2	Vertical Sync End [2]
1	Vertical Sync End [1]
0	Vertical Sync End [0]

This register specifies the scanline at which the Vertical Sync pulse is to become inactive, thereby effectively specifying the Vertical Sync pulse width. In addition, this register contains controls for the interrupt and two miscellaneous control bits.

Bit	Description
7	**Write Protect CR7-CR0:** If this bit is programmed to a '1', registers CR0..CR7 cannot be written. Writes addressed to those registers will simply be ignored. CR7[4] (Line Compare Extension) can always be written. If this bit is programmed to a '0', registers CR0..CR7 can be written normally.
6	**Refresh Cycle Control:** If this bit is programmed to a '1', five refresh cycles will be executed per scanline. If this bit is programmed to a '0', three refresh cycles will be executed per scanline.
5	**Disable Vertical Interrupt:** If this bit is programmed to a '1', the vertical interrupt will be disabled. In this case, the Interrupt pin can never go active. If this bit is programmed to a '0', the vertical interrupt will be enabled and will function normally.
4	**Clear Vertical Interrupt:** If this bit is programmed to a '0', the Interrupt Pending bit (FEAT[7]) will be cleared to a '0' and the interrupt pin will be forced inactive. Programming this bit to a '1' has no effect.
3:0	**Vertical Sync End [3:0]:** This field determines the width of the Vertical Sync pulse. The least-significant four bits of the Scanline Counter are compared with the contents of this field. When a match occurs, the Vertical Sync pulse is ended. Note the Vertical Sync pulse is limited to 15 scanlines. The value to be programmed into this register may be calculated by subtracting the desired Sync width from the value programmed into the Vertical Sync Start field. The Sync pulse must never be programmed to extend past the Vertical Total. Refer to Figure 6–1 and Table 6–2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.20 CR12: Vertical Display End Register

I/O Port Address: 3?5

Index: 12

Bit	Description
7	Vertical Display End [7]
6	Vertical Display End [6]
5	Vertical Display End [5]
4	Vertical Display End [4]
3	Vertical Display End [3]
2	Vertical Display End [2]
1	Vertical Display End [1]
0	Vertical Display End [0]

The Vertical Display End field is used to specify the scanline at which the display is to end.

Bit	Description
7:0	**Vertical Display End [7:0]:** The Vertical Display End field is used to specify the scanline at which the display is to end. This register contains the least-significant eight bits of this field. Refer to Figure 6–1 and Table 6–2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.21 CR13: Offset Register

I/O Port Address: 3?5

Index: 13

Bit	Description
7	Offset [7]
6	Offset [6]
5	Offset [5]
4	Offset [4]
3	Offset [3]
2	Offset [2]
1	Offset [1]
0	Offset [0]

This register specifies the distance in display memory between the beginnings of adjacent character rows or scanlines. This is sometimes referred to as display 'pitch'.

Bit	Description
7:0	**Offset [7:0]:** This register specifies the distance in display memory between the beginnings of adjacent character rows or scanlines. This field is extended to nine bits with CR1B[4]. At the beginning of each scanline (except the first), the address from which to beginning fetching data is calculated by adding the contents of this register to the beginning address of the previous scanline or character row. The offset will be left-shifted one or two bit positions depending on CR17[6].

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.22 CR14: Underline Row Scanline Register

I/O Port Address: 3?5

Index: 14

Bit	Description
7	Reserved
6	DoubleWord Mode
5	Count by Four
4	Underline scanline [4]
3	Underline scanline [3]
2	Underline scanline [2]
1	Underline scanline [1]
0	Underline scanline [0]

This register is used to specify the underline scanline.

Bit	Description
7	**Reserved**
6	**DoubleWord Mode:** When this bit is programmed to a '1', double-word addresses are forced. The CRTC Memory Address Counter is rotated left two bit positions, so that display memory Address bits 1 and 0 are sourced from CRTC Address Counter bits 13 and 12, respectively. When this bit is programmed to a '0', CR17[6] controls whether the chip uses byte or word addresses.
5	**Count by Four:** This bit must be programmed to a '1' when DoubleWord mode is enabled to clock the Memory Address Counter with Character Clock divided by four. This bit must be programmed to a '0' when DoubleWord mode is not enabled
4:0	**Underline Scanline [4:0]:** This field specifies the scanline within the Character Cell where the underline will occur.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.23 CR15: Vertical Blank Start Register

I/O Port Address: 3?5

Index: 15

Bit	Description
7	Vertical Blank Start [7]
6	Vertical Blank Start [6]
5	Vertical Blank Start [5]
4	Vertical Blank Start [4]
3	Vertical Blank Start [3]
2	Vertical Blank Start [2]
1	Vertical Blank Start [1]
0	Vertical Blank Start [0]

This register specifies the scanline at which blank is to become active.

Bit	Description
7:0	**Vertical Blank Start [7:0]:** The Vertical Blank Start field specifies the scanline on which Vertical Blank is to begin. The low-order eight bits of that field are in this register. Refer to Figure 6–1 and Table 6–2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.24 CR16: Vertical Blank End Register

I/O Port Address: 3?5

Index: 16

Bit	Description
7	Vertical Blank End [7]
6	Vertical Blank End [6]
5	Vertical Blank End [5]
4	Vertical Blank End [4]
3	Vertical Blank End [3]
2	Vertical Blank End [2]
1	Vertical Blank End [1]
0	Vertical Blank End [0]

The Vertical Blank End field specifies the scanline at which Vertical Blank is to end.

Bit	Description
7:0	**Vertical Blank End [7:0]:** The Vertical Blank End field specifies the scanline at which Vertical Blank is to end. This register contains the low-order eight bits of that field. If CR1B[5] is programmed to a '0', this register contains the entire field. The contents of the Vertical Blank End field are compared to the Scanline Counter to determine when to terminate Vertical Blank. This limits the duration of Vertical Blank to 255 scanlines if CR1B[5] is programmed to a '0'. Refer to Figure 6–1 and Table 6–2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.25 CR17: Mode Control Register

I/O Port Address: 3?5

Index: 17

Bit	Description
7	Timing Enable
6	Byte/Word Mode
5	Address Wrap
4	Reserved
3	Count by Two
2	Multiply Vertical Registers by Two
1	Select Row Scan Counter
0	Compatibility Mode (CGA) Support

This register contains a number of miscellaneous control bits.

Bit	Description
7	**Timing Enable:** If this bit is programmed to a '1', the CRTC Timing Logic is enabled and functions normally. If this bit is programmed to a '0', the CRTC Timing Logic is disabled.
6	**Byte/Word Mode:** If this bit is programmed to a '1', the contents of the CRTC Address Counter are sent to the display memory without being rotated. If this bit is programmed to a '0', the contents of the CRTC Address Counter are rotated left one bit position before being sent to the display memory.
5	**Address Wrap:** If CR17[6] is programmed to '1', this bit is ignored. If CR17[6] is programmed to a '0' and this bit is programmed to a '1', then the left rotation described above involves 16 bits of the CRTC Address Counter. If CR17[6] is programmed to a '0' and this bit is programmed to a '0', then the left rotation described above involves 14 bits of the CRTC Address Counter.
4	**Reserved**
3	**Count by Two:** If this bit is programmed to a '1', then the CL-GD542X will clock the Memory Address Counter with Character Clock divided by two. If this bit is programmed to a '0', then the CL-GD542X will clock the Memory Address Counter with Character Clock.
2	**Multiply Vertical Registers by Two:** If this bit is programmed to a '1', the Scanline Counter is clocked with Horizontal Sync divided by two. This allows the number of scanlines to be doubled to 2048. Observe that all the periods will be even multiples of two scanlines. If this bit is programmed to a '0', the Scanline Counter is clocked with Horizontal Sync.

6.25 CR17: Mode Control Register *(cont.)*

Bit	Description
1	**Select Row Scan Counter:** If this bit is programmed to a '0', Row Scan Counter [1] is substituted for CRTC Address Counter [14]. This provides for Hercules™ compatibility. If this bit is programmed to a '1', the substitution described above does not occur.
0	**Compatibility Mode (CGA) Support:** If this bit is programmed to a '0', Row Scan Counter [0] is substituted for CRTC Address Counter [14]. This provides for CGA compatibility. If this bit is programmed to a '1', the substitution described above does not occur.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.26 CR18: Line Compare Register

I/O Port Address: 3?5

Index: 18

Bit	Description
7	Line Compare [7]
6	Line Compare [6]
5	Line Compare [5]
4	Line Compare [4]
3	Line Compare [3]
2	Line Compare [2]
1	Line Compare [1]
0	Line Compare [0]

The Line Compare field is used to specify where Screen A terminates and Screen B begins.

Bit	Description
7:0	**Line Compare [7:0]:** The Line Compare field is used to specify where Screen A terminates and Screen B begins. This register contains the eight least-significant bits of this field. The Line Compare field may be used to implement a vertically split screen. The top portion of the screen is called Screen A and may begin anywhere in display memory. Screen A can be panned and scrolled on a pixel basis. The bottom portion of the screen is called Screen B. Screen B always begins at location '0' in display memory and cannot be panned or scrolled. Refer to Figure 6–1 and Table 6–2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.27 CR22: Graphics Data Latches Readback Register

I/O Port Address: 3?5

Index: 22

Bit	Description
7	Graphics Data Latch n Readback [7]
6	Graphics Data Latch n Readback [6]
5	Graphics Data Latch n Readback [5]
4	Graphics Data Latch n Readback [4]
3	Graphics Data Latch n Readback [3]
2	Graphics Data Latch n Readback [2]
1	Graphics Data Latch n Readback [1]
0	Graphics Data Latch n Readback [0]

This register address is used to read the four Graphics Controller Data Latches.

Bit	Description
7:0	**Graphics Data Latch n Readback [7:0]:** This read-only register may be used to read back one of the four Graphics Controller Data Latches. The latch is selected with GR4[1:0]. These latches are loaded whenever display memory is read by the CPU.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.28 CR24: Attribute Controller Toggle Readback Register

I/O Port Address: 3?5

Index: 24

Bit	Description
7	Attribute Controller Toggle
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Reserved
1	Reserved
0	Reserved

This read-only register provides access to the Attribute Controller Toggle.

Bit	Description
7	**Attribute Controller Toggle:** If this bit is a '1', the Attribute Controller will read or write a data value on the next access. If this bit is a '0', the Attribute Controller will read or write an index value on the next access.
6:0	**Reserved**

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.29 CR26: Attribute Controller Index Readback Register

I/O Port Address: 3?5

Index: 26

Bit	Description
7	Reserved
6	Reserved
5	Video Enable
4	Attribute Controller Index [4]
3	Attribute Controller Index [3]
2	Attribute Controller Index [2]
1	Attribute Controller Index [1]
0	Attribute Controller Index [0]

This read-only register provides access to the current Attribute Controller Index.

Bit	Description
7:6	**Reserved**
5	**Video Enable:** This bit follows the Video Enable bit in the Attribute Controller Index register.
4:0	**Attribute Controller Index [4:0]:** This field follows the index in the Attribute Controller Index register.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

VGA Graphics Controller Registers

7. VGA GRAPHICS CONTROLLER REGISTERS

The CL-GD542X VGA Graphics Controller registers are summarized in the following table. Please note that there are Extension registers that are accessed using the VGA Graphics Controller Port.

Table 7-1. VGA Graphics Controller Registers Quick Reference

Abbreviation	Register Name	Index	Port	Page
GRX	Graphics Controller Index	–	3CE	7 - 3
GR0	Set/Reset	0	3CF	7 - 4
GR1	Set/Reset Enable	1	3CF	7 - 5
GR2	Color Compare	2	3CF	7 - 6
GR3	Data Rotate	3	3CF	7 - 7
GR4	Read Map Select	4	3CF	7 - 8
GR5	Mode	5	3CF	7 - 9
GR6	Miscellaneous	6	3CF	7 - 12
GR7	Color Don't Care	7	3CF	7 - 13
GR8	Bit Mask	8	3CF	7 - 14

7.1 GRX: Graphics Controller Index Register

I/O Port Address: 3CE

Index: –

Bit	Description
7	Reserved
6	Reserved
5	Graphics Controller Index [5]
4	Graphics Controller Index [4]
3	Graphics Controller Index [3]
2	Graphics Controller Index [2]
1	Graphics Controller Index [1]
0	Graphics Controller Index [0]

This register is used to specify the register in the VGA Graphics Controller group or the Extension register that will be accessed by the next I/O read or I/O write to 3CF.

Bit	Description
7:6	**Reserved**
5:0	**Graphics Controller Index [5:0]:** This field specifies the register in the VGA Graphics Controller group or the Extension register that will be accessed by the next I/O read or I/O write to 3CF. Registers indexes above 1F are valid for the CL-GD5426/'28/'29 only.

7.2 GR0: Set/Reset Register

I/O Port Address: 3CF

Index: 0

Bit	Description
7	Reserved/ Write Mode 5 Background [7]
6	Reserved/ Write Mode 5 Background [6]
5	Reserved/ Write Mode 5 Background [5]
4	Reserved/ Write Mode 5 Background [4]
3	Set/Reset Plane 3/Write Mode 5 Background [3]
2	Set/Reset Plane 2/Write Mode 5 Background [2]
1	Set/Reset Plane 1/Write Mode 5 Background [1]
0	Set/Reset Plane 0/Write Mode 5 Background [0]

This register specifies the values to be written into the respective display memory planes when the processor executes a Write mode 0 or 3 operation. If Extended Write mode 5 is selected, this register specifies the background color.

Bit	Description
7:4	**Reserved:** If Extended Write mode 5 is not selected, these bits are reserved. If GRB[2]=0, writes to these bits will be ignored and reads from these bits will return zeroes. If GRB[2]=1, these bits will be read/write but the contents will not be used.
3:0	**Set/Reset Plane [3:0]:** If Extended Write mode 5 is not selected, these bits will control the values written into the respective display memory planes for Write mode 0 and 3. Refer to the description of GR5 for an overview of the Write modes.
7:0	**Write Mode 5 Background [7:0]:** If Extended Write mode 5 is selected, these bits specify the background color. Refer to the description of GR5 for an overview of the Write modes.

7.3 GR1: Set/Reset Enable Register

I/O Port Address: 3CF

Index: 1

Bit	Description
7	Reserved/ Write Mode 4, 5 Foreground [7]
6	Reserved/ Write Mode 4, 5 Foreground [6]
5	Reserved/ Write Mode 4, 5 Foreground [5]
4	Reserved/ Write Mode 4, 5 Foreground [4]
3	Enable SR Plane 3/ Write Mode 4, 5 Foreground [3]
2	Enable SR Plane 2/ Write Mode 4, 5 Foreground [2]
1	Enable SR Plane 1/ Write Mode 4, 5 Foreground [1]
0	Enable SR Plane 0/ Write Mode 4, 5 Foreground [0]

This register is used with GR0 to determine the values to be written into the respective display memory planes when Write mode 0 is selected. If Extended Write modes 4 or 5 are selected, this register defines the foreground color.

Bit	Description
7:4	**Reserved:** If Extended Write modes 4 or 5 are not selected, these bits are reserved. If GRB[2]=0, writes to these bits will be ignored and reads from these bits will return zeroes. If GRB[2]=1, these bits will be read/write but the contents will not be used.
3:0	**Enable SR Plane [3:0]:** These bits are used with GR0 to determine the values written into the display memory planes when Write mode 0 is selected. If a bit in this field is programmed to a '1', the corresponding value in GR0 will be written into the corresponding display memory plane. If a bit in this field is programmed to a '0', the corresponding value from the CPU data bus will be written into the corresponding display memory plane. Refer to the description of GR5 for an overview of the Write modes. For the CL-GD5429 only, if SR7[0] is programmed to a '1', the value from the CPU bus will be written, regardless of the contents of this field.
7:0	**Write Mode 4, 5 Foreground [7:0]:** If Extended Write mode 4 or 5 is selected, these bits specify the foreground color. Refer to the description of GR5 for an overview of the Write modes.

7.4 GR2: Color Compare Register

I/O Port Address: 3CF

Index: 2

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Color Compare Plane [3]
2	Color Compare Plane [2]
1	Color Compare Plane [1]
0	Color Compare Plane [0]

This register specifies the color compare value for Read mode 1.

Bit	Description
7:4	**Reserved**
3:0	**Color Compare Plane [3:0]:** These four bits are compared with each of eight bits from the corresponding display memory planes under the mask in GR7 when a Read mode 1 takes place. Refer to the description of GR5 for an overview of the Read modes.

7.5 GR3: Data Rotate Register

I/O Port Address: 3CF

Index: 3

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Function Select [1]
3	Function Select [0]
2	Rotate Count [2]
1	Rotate Count [1]
0	Rotate Count [0]

This register contains two fields that are used with Write modes 0 and 3.

Bit **Description**

7:5 **Reserved**

4:3 **Function Select [1:0]:** This field control the operation that takes place between the data in the latches and the data from the CPU or SR logic. The result of this operation is written into display memory. This field is used for Write mode 0 only. The operations are summarized in the following table:

GR3[4]	GR3[3]	Operation
0	0	None: The data in the latches are ignored.
0	1	Logical 'AND'
1	0	Logical 'OR'
1	1	Logical 'XOR"

2:0 **Rotate Count [2:0]:** This field allows data from the CPU bus to be rotated up to seven bit positions prior to being altered by the SR logic. Refer to the description of GR5 for an overview of the Write modes.

7.6 GR4: Read Map Select Register

I/O Port Address: 3CF

Index: 4

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Reserved
1	Plane Select [1]
0	Plane Select [0]

This register is used to specify the display memory plane for Read mode 0.

Bit	Description
7:2	**Reserved**
1:0	**Plane Select [1:0]:** This field specifies the display memory plane for Read mode 0. The values are shown in the following table:

GR4[1]	GR4[0]	Plane Selected
0	0	0
0	1	1
1	0	2
1	1	3

7.7 GR5: Mode Register

I/O Port Address: 3CF

Index: 5

Bit	Description
7	Reserved
6	256-color Mode
5	Shift Register Mode
4	Odd/Even
3	Read Mode
2	Reserved/Write Mode [2]
1	Write Mode [1]
0	Write Mode [0]

This register specifies the Write mode and Read mode. In addition, it controls the configuration of the Data Shift registers.

Bit	Description
7	**Reserved**
6	**256-color Mode:** If this bit is programmed to a '1', the Video Shift registers will be configured for 256-color Video modes. GR5[5] is ignored. If this bit is programmed to a '0', the Video Shift registers will be configured for 16-, 4-, or 2-color modes.
5	**Shift Register Mode:** If this bit is programmed to a '1', the Video Shift registers will be configured for CGA compatibility. This is used for Video modes 4 and 5. If this bit is programmed to a '0', the Video Shift registers will be configured for EGA compatibility.
4	**Odd/Even:** If this bit is programmed to a '1', the Graphics Controller will be configured for Odd/Even Addressing mode. This bit should always be programmed to the opposite value as SR4[2].

7.7 GR5: Mode Register *(cont.)*

Bit	Description
3	**Read Mode:** This bit specifies whether the chip is in Read mode 0 or Read mode 1. **Read Mode 0:** If this bit is programmed to a '0', the CPU will read data directly from display memory. Each read will return eight adjacent bits of the display memory plane specified in GR4[1:0]. The color-match logic is not used in Read mode 0. Note that an I/O read of CR22 will force a Read mode 0 operation. **Read Mode 1:** If this bit is programmed to a '1', the CPU will read the results of the color compare logic. Read mode 1 allows eight adjacent pixels (16-color modes) to be compared to a specified color value in a single operation. Each of the eight bits returned to the processor indicates the result of a compare between the four bits of the Color Compare GR2[3:0]) and the bits from the four display memory planes. If the four bits of the Color Compare match the four bits from the display memory planes, a '1' will be returned for the corresponding bit position. If any bits in the Color Don't Care (GR7[3:0]) are zeroes, the corresponding plane comparison will be forced to match.
2:0	**Write Mode [2:0]:** These three bits specify the Write mode or Extended Write mode. If GRB[2] is programmed to a '0', bit 2 will be forced to a '0'. Only Write modes 0 through 3 will be available. **Write Mode 0:** Each of the four display memory planes is written with the CPU data rotated by the number of counts in GR3[2:0]. If a bit in GR1[3:0] is programmed to a '1', the corresponding plane is written with the contents of the corresponding bit in GR0[3:0]. The contents of the data latches may be combined with the data from the SR logic under control of GR3[4:3]. Bit planes are enabled with SR2[3:0]. Bit positions are enabled with GR8. **Write Mode 1:** Each of the four display memory planes is written with the data in the Data Latches. The Data Latches had been loaded from display memory with a previous read. GR8 is ignored in Write mode 1. **Write Mode 2:** Display memory planes 3:0 are written with value of Data bits 3:0, respectively. The four bits are replicated eight times each to write up to eight adjacent pixels. Bit planes are enabled with SR2[3:0]. Bit positions are enabled with GR8. The Data Rotator, SR logic and Function Select fields are ignored in Write mode 2.

7.7 GR5: Mode Register *(cont.)*

Bit	Description
2:0 *(cont.)*	**Write Mode 3:** The data for each display memory plane comes from the corresponding bit of GR0[3:0]. The bit-position-enable field is formed with the logical AND of GR8 and the rotated CPU data. The SR and Function Select fields are ignored in Write mode 3. **Extended Write Mode 4:** The contents of GR1[7:0] are written into to up to eight adjacent pixels. The CPU data is used to control whether pixels are written. If a bit in the CPU is a '1', the corresponding pixel is written. If a bit in the CPU data is a '0', the corresponding pixel is not changed. This mode is intended for 256-color text expansion where the background is to be preserved. In the CL-GD5422/'24/'26/'28/'29, it can also be used for 64K-color text expansion. **Extended Write Mode 5:** The contents of either GR1[7:0] or GR0[7:0] are written into each of eight adjacent pixels. The choice between GR1 and GR0 is made for each of the eight pixels according the value of the corresponding bit of the CPU data. This is summarized in the following table. This mode is intended for 256-color text expansion where both the foreground and background are to be written. In the CL-GD5422/'24/'26/'28/'29, it can also be used for 64K-color text expansion.

CPU Data	GR0/GR1	Note
0	GR0	Background
1	GR1	Foreground

7.8 GR6: Miscellaneous Register

I/O Port Address: 3CF

Index: 6

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Memory Map [1]
2	Memory Map [0]
1	Chain Odd Maps to Even
0	Graphics Mode

This register contains miscellaneous control bits.

Bit **Description**

7:4 **Reserved**

3:2 **Memory Map [1:0]:** This field specifies the beginning address and size of the display memory in the Host Address Space. This is summarized in the following table:

GR6[3]	GR6[2]	Memory Map	Beginning Address	Length	Mode(s)
0	0	0	A000:0	128K	Extended
0	1	1	A000:0	64K	EGA/VGA
1	0	2	B000:0	32K	Hercules
1	1	3	B800:0	32K	CGA

1 **Chain Odd Maps to Even:** When this bit is programmed to a '1', CPU Address bit 0 is replaced with a higher-order address bit. This causes even host addresses to access Planes 0 and 2, and odd host addresses to access Planes 1 and 3. This mode is useful for MDA emulation.

0 **Graphics Mode:** If this bit is programmed to a '1', the CL-GD542X will function in Graphics (A.P.A.) modes. If it is programmed to a '0', the chip will function in Text (A.N.) modes.

7.9 GR7: Color Don't Care Register

I/O Port Address: 3CF

Index: 7

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Color Don't Care Plane [3]
2	Color Don't Care Plane [2]
1	Color Don't Care Plane [1]
0	Color Don't Care Plane [0]

This register is used with GR2 for Read mode 1 accesses.

Bit	Description
7:4	**Reserved**
3:0	**Color Don't Care Plane [3:0]:** These four bits are used to control whether the four planes will be involved in color compares. If a bit is programmed to a '1', the corresponding plane will be involved; if a bit is programmed to a '0', the corresponding plane will not be involved. Refer to the description of GR5 for an overview of the Read modes.

7.10 GR8: Bit Mask Register

I/O Port Address: 3CF

Index: 8

Bit	Description
7	Write Enable [7]
6	Write Enable [6]
5	Write Enable [5]
4	Write Enable [4]
3	Write Enable [3]
2	Write Enable [2]
1	Write Enable [1]
0	Write Enable [0]

This register is used to control writing to display memory on a bit basis in Write modes 0, 2, and 3.

Bit	Description
7:0	**Write Enable [7:0]:** Each bit in this register controls whether the corresponding bit in display memory is written in Write modes 0, 2, and 3. If a bit is programmed to a '1', the corresponding bit in display memory. If a bit is programmed to a '0', the corresponding bit in display memory will not be written. This write protection is orthogonal to that provided by SR2.

Attribute Controller Registers

8. ATTRIBUTE CONTROLLER REGISTERS

The CL-GD542X Attribute Controller registers are summarized in the following table:

Table 8–1. Attribute Controller Registers Quick Reference

Abbreviation	Register Name	Index	Port	Page
ARX	Attribute Controller Index	–	3C0/3C1	8 - 3
AR0-ARF	Attribute Controller Palette	0:F	3C0/3C1	8 - 4
AR10	Attribute Controller mode	10	3C0/3C1	8 - 5
AR11	Overscan (Border) Color	11	3C0/3C1	8 - 7
AR12	Color Plane Enable	12	3C0/3C1	8 - 8
AR13	Pixel Panning	13	3C0/3C1	8 - 9
AR14	Color Select	14	3C0/3C1	8 - 10

8.1 ARX: Attribute Controller Index Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: (n/a)

Bit	Description
7	Reserved
6	Reserved
5	Video Enable
4	Attribute Controller Index [4]
3	Attribute Controller Index [3]
2	Attribute Controller Index [2]
1	Attribute Controller Index [1]
0	Attribute Controller Index [0]

This register is used to specify the register in the Attribute Controller block that is accessed with the next I/O read or I/O write to 3C1 or 3C0, respectively. Observe that the same port addresses are used for the index and data for the Attribute Controller block, unlike the other blocks for which the Index and Data registers are at different addresses. Alternate writes toggle between index and data. It is possible to read the toggle at CR24, and the index value at CR26.

Bit	Description
7:6	**Reserved**
5	**Video Enable:** When this bit is programmed to a '0', the screen displays the color indicated by the Overscan register (AR11). When this bit is programmed to a '1', normal video is displayed.
4:0	**Attribute Controller Index [4:0]:** This field is the index into the Data registers in the Attribute Controller block.

8.2 AR0-ARF: Attribute Controller Palette Registers

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 0:F

Bit	Description
7	Reserved
6	Reserved
5	Secondary Red
4	Secondary Green/Intensity
3	Secondary Blue/ Mono
2	Red
1	Green
0	Blue

In 16-color Text and Graphics modes, these digital palette entries are chosen by the four bits of pixel data, and point to Video RAM entries. The Video RAM entries are normally programmed so that the DAC Outputs reflect these values. That is, the Video RAM is programmed to simulate standard EGA colors.

Bit	Description
7:6	**Reserved**
5:0	**Palette Entries**

8.3 AR10: Attribute Controller Mode Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 10

Bit	Description
7	AR14 Video Source Enable
6	Pixel Double Clock Select
5	Pixel Panning Compatibility
4	Reserved
3	Blink Enable
2	Line Graphics Enable
1	Display Type
0	Graphics Mode

This register contains some miscellaneous control bits for the Attribute Controller.

Bit	Description
7	**AR14 Video Source Enable:** If this bit is programmed to a '1', AR14[1:0] are used as the source for the Lookup Table Address bits [5:4]. This allows the rapid selection of four 16-color palettes. If an 8-, 16-, or 24-bit Pixel mode is chosen, this bit is ignored. If this bit is programmed to a '0', the Palette registers AR0-F[5:4] are used as the source for the Lookup Table Address bits [5:4].
6	**Pixel Double Clock Select:** If this bit is programmed to a '1', pixels are clocked on every other clock cycle and AR0-F is bypassed. This is used with mode 13. The Sequencer Logic operates at twice the Pixel Rate. If this bit is programmed to a '0', pixels are clocked on every cycle.
5	**Pixel Panning Compatibility:** If this bit is programmed to a '1', a Line Compare match in the CRTC will force the output of the Pixel Panning register to a '0' until the next VSYNC occurs. This allows the panning of Screen A without Screen B. If this bit is programmed to a '0', the two parts of a split screen will pan together.
4	**Reserved**
3	**Blink Enable:** If this bit is programmed to a '1', character blinking is enabled at the Vertical Refresh Frequency divided by 32. If this bit is programmed to a '0', character blinking is disabled.
2	**Line Graphics Enable:** If this bit is programmed to a '1', the ninth bit of a nine-bit-wide character cell will be made the same as the eighth bit for character codes in the range C0 through DF. If this bit is programmed to a '0', the ninth bit of nine-bit-wide character cell will be the same as the background.

8.3 AR10: Attribute Controller Mode Register *(cont.)*

Bit **Description**

1 **Display Type:** This bit is useful only if the CL-GD542X is in Alphanumeric modes. If this bit is programmed to a '1', the contents of the Attribute byte are treated as MDA-compatible attributes. The following table shows examples of monochrome attributes:

Blink Bit 7	Background Bit [6:4]	Intensity Bit 3	Foreground Bit [2:0]	Hex Code	Attribute
0	0	0	7	07	Normal
0	0	1	7	0F	Intense
0	0	0	1	01	Underline
0	0	1	1	09	Underline Intense
0	7	0	0	70	Reverse
1	7	0	0	F0	Blinking Reverse

If this bit is programmed to a '0', the contents of the Attribute byte are treated as color attributes.

0 **Graphics Mode:** If this bit is programmed to a '1', the Attribute Controller will function in A.P.A. (Graphics) mode. If this bit is programmed to a '0', the Attribute Controller will function in A.N. (Alphanumeric) modes.

8.4 AR11: Overscan (Border) Color Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 11

Bit	Description
7	Reserved
6	Reserved
5	Secondary Red
4	Secondary Green
3	Secondary Blue
2	Red
1	Green
0	Blue

This register points to the entry in the LUT that defines the border color. Typically, the LUT entries are programmed so that the color defined above is the color that actually results. The border is defined as that portion of the raster between blanking and active video, on all four sides. Refer to Figure 6–1 at register CR0.

Bit	Description
7:6	**Reserved**
5:0	**Border Color [5:0]:** Either four or six of these bits are used to select the LUT entry for the Border Color in CGA and EGA modes.

8.5 AR12: Color Plane Enable Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 12

Bit	Description
7	Reserved
6	Reserved
5	Video Status Mux [1]
4	Video Status Mux [0]
3	Enable Plane [3]
2	Enable Plane [2]
1	Enable Plane [1]
0	Enable Plane [0]

This register contains a field that enables the four planes into the Attribute Controller Palette registers. It also contains a field that chooses the inputs for Diagnostic bits in STAT[5:4].

Bit **Description**

7:6 **Reserved**

5:4 **Video Status Mux [1:0]:** This field chooses the inputs for the Diagnostic bits in STAT[5:4] as indicated in the following table:

AR12[5]	AR12[4]	STAT[5]	STAT[4]
0	0	P[2]: Red	P[0]: Blue
0	1	P[3]: Secondary Blue	P[1]: Green
1	0	P[5]: Secondary Red	P[4]: Secondary Green
1	1	P[7]	P[6]

3:0 **Enable Color Plane [3:0]:** If any bit in this field is programmed to a '1', the data from the corresponding display memory plane is enabled in the choice of the Attribute Controller Palette register. If any bit in this field is programmed to a '0', the data from the corresponding display memory plane is forced to a '0' in the choice of the Attribute Controller Palette register.

8.6 AR13: Pixel Panning Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 13

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Pixel Panning [3]
2	Pixel Panning [2]
1	Pixel Panning [1]
0	Pixel Panning [0]

This register specifies the number of pixels the display data will be shifted to the left. This field functions both in the Graphics (A.N.) and Alphanumeric (A.P.A.) modes.

Bit	Description
7:4	**Reserved**
3:0	**Pixel Panning [3:0]:** This field specifies the number of pixels the display data will be shifted to the left. This field is interpreted as indicated in the following table:

AR13[3:0]	9-Bit Characters	8-Bit Characters	Mode 13
0	1 bit left	(none)	(none)
1	2 bits left	1 bit left	–
2	3 bits left	2 bits left	1 bit left
3	4 bits left	3 bits left	–
4	5 bits left	4 bits left	2 bits left
5	6 bits left	5 bits left	–
6	7 bits left	6 bits left	3 bits left
7	8 bits left	7 bits left	–
8-F	no shift	1 bit right	–

8.7 AR14: Color Select Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 14

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Color Bit C [7]
2	Color Bit C [6]
1	Color Bit C [5]
0	Color Bit C [4]

This register contains two fields that are involved in the selection of addresses into the LUT.

Bit	Description
7:4	**Reserved**
3:2	**Color Bit C [7:6]:** These two bits are concatenated with the six bits from the Attribute Controller Palette register to form the address into the LUT and to drive P[7:6]. These bit are ignored in 8-, 16-, and 24-bit Pixel modes.
1:0	**Color Bits C [4:5]:** If AR10[7] is programmed to a '1', these two bits replace the corresponding two bits from the Attribute Controller Palette register to form the address into the LUT and to drive P[7:6]. If AR10[7] is programmed to a '0', these two bits are ignored. These bits are ignored in 8-, 16-, and 24-bit Pixel modes.

Extension Registers

9. EXTENSION REGISTERS

The CL-GD542X Extension registers are summarized in Table 9–1.

Table 9–1. Extension Registers Quick Reference

Abbreviation	Register Name	Index	Port	Page
SR2	Enable Writing Pixel Extension[a]	2	3C5	5 - 7
SR6	Unlock ALL Extensions *(except CL-GD5429)*	6	3C5	9 - 5
SR7	Extended Sequencer Mode	7	3C5	9 - 6
SR8	EEPROM Control	8	3C5	9 - 8
SR9	Scratch-Pad 0	9	3C5	9 - 10
SRA	Scratch-Pad 1	A	3C5	9 - 10
SRB	VCLK0 Numerator	B	3C5	9 - 11
SRC	VCLK1 Numerator	C	3C5	9 - 11
SRD	VCLK2 Numerator	D	3C5	9 - 11
SRE	VCLK3 Numerator	E	3C5	9 - 11
SRF	DRAM Control	F	3C5	9 - 12
SR10	Graphics Cursor Y Position	10	3C5	9 - 14
SR11	Graphics Cursor X Position	11	3C5	9 - 15
SR12	Graphics Cursor Attributes	12	3C5	9 - 16
SR13	Graphics Cursor Pattern Address Offset	13	3C5	9 - 17
SR14	Scratch-Pad 2 *(CL-GD5426/'28/'29 only)*	14	3C5	9 - 18
SR15	Scratch-Pad 3 *(CL-GD5426/'28/'29 only)*	15	3C5	9 - 18
SR16	Performance Tuning *(CL-GD5424/'26/'28/'29 only)*	16	3C5	9 - 19
SR17	Configuration Readback and Extended Control *(CL-GD5428 only)*	17	3C5	9 - 21
SR18	Signature Generator Control *(except CL-GD5420)*	18	3C5	9 - 22
SR19	Signature Generator Result Low Byte *(except CL-GD5420)*	19	3C5	9 - 24
SR1A	Signature Generator Result High Byte *(except CL-GD5420)*	1A	3C5	9 - 25
SR1B	VCLK0 Denominator and Post-Scalar Value	1B	3C5	9 - 26
SR1C	VCLK1 Denominator and Post-Scalar Value	1C	3C5	9 - 26
SR1D	VCLK2 Denominator and Post-Scalar Value	1D	3C5	9 - 26
SR1E	VCLK3 Denominator and Post-Scalar Value	1E	3C5	9 - 26

Table 9–1. Extension Registers Quick Reference *(cont.)*

Abbreviation	Register Name	Index	Port	Page
SR1F	BIOS ROM Write Enable and MCLK Select	1F	3C5	9 - 27
GR0	Write Mode 5 Background Extension[b]	0	3CF	7 - 4
GR1	Write Mode 4, 5 Foreground Extension[‡]	1	3CF	7 - 5
GR9	Offset Register 0	9	3CF	9 - 29
GRA	Offset Register 1	A	3CF	9 - 31
GRB	Graphics Controller Mode Extensions	B	3CF	9 - 32
GRC	Color Key *(CL-GD5424/'26/'28/'29 only)*	C	3CF	9 - 34
GRD	Color Key Mask *(CL-GD5424/'26/'28/'29 only)*	D	3CF	9 - 35
GRE	Miscellaneous Control *(CL-GD5428/'29 only)*	E	3CF	9 - 36
GR10	16-bit Pixel Background Color High Byte *(except CL-GD5420)*	10	3CF	9 - 37
GR11	16-bit Pixel Foreground Color High Byte *(except CL-GD5420)*	11	3CF	9 - 38
GR20	BLT Width Low *(CL-GD5426/'28/'29 only)*	20	3CF	9 - 39
GR21	BLT Width High *(CL-GD5426/'28/'29 only)*	21	3CF	9 - 40
GR22	BLT Height Low *(CL-GD5426/'28/'29 only)*	22	3CF	9 - 41
GR23	BLT Height High *(CL-GD5426/'28/'29 only)*	23	3CF	9 - 42
GR24	BLT Destination Pitch Low *(CL-GD5426/'28/'29 only)*	24	3CF	9 - 43
GR25	BLT Destination Pitch High *(CL-GD5426/'28/'29 only)*	25	3CF	9 - 44
GR26	BLT Source Pitch Low *(CL-GD5426/'28/'29 only)*	26	3CF	9 - 45
GR27	BLT Source Pitch High *(CL-GD5426/'28/'29 only)*	27	3CF	9 - 46
GR28	BLT Destination Start Low *(CL-GD5426/'28/'29 only)*	28	3CF	9 - 47
GR29	BLT Destination Start Mid *(CL-GD5426/'28/'29 only)*	29	3CF	9 - 48
GR2A	BLT Destination Start High *(CL-GD5426/'28/'29 only)*	2A	3CF	9 - 49
GR2C	BLT Source Start Low *(CL-GD5426/'28/'29 only)*	2C	3CF	9 - 50
GR2D	BLT Source Start Mid *(CL-GD5426/'28/'29 only)*	2D	3CF	9 - 51
GR2E	BLT Source Start High *(CL-GD5426/'28/'29 only)*	2E	3CF	9 - 52
GR2F	BLT Write Mask Destination *(CL-GD5429 only)*	2F	3CF	9 - 53
GR30	BLT Mode *(CL-GD5426/'28/'29 only)*	30	3CF	9 - 54

Table 9–1. Extension Registers Quick Reference *(cont.)*

Abbreviation	Register Name	Index	Port	Page
GR31	BLT Start/Status *(CL-GD5426/'28/'29 only)*	31	3CF	9 - 57
GR32	BLT Raster Operation *(CL-GD5426/'28/'29 only)*	32	3CF	9 - 58
GR34	Transparent Color Select Low *(CL-GD5426/'28 only)*	34	3CF	9 - 60
GR35	Transparent Color Select High *(CL-GD5426/'28 only)*	35	3CF	9 - 61
GR38	Transparent Color Mask Low *(CL-GD5426/'28 only)*	38	3CF	9 - 62
GR39	Transparent Color Mask High *(CL-GD5426/'28 only)*	39	3CF	9 - 63
CR19	Interlace End	19	3?5	9 - 64
CR1A	Interlace Control	1A	3?5	9 - 65
CR1B	Extended Display Controls	1B	3?5	9 - 67
CR1D	Overlay Mode Controls *(CL-GD5429 only)*	1C	3?5	9 - 69
CR25	Part Status	25	3?5	9 - 70
CR27	ID	27	3?5	9 - 71
HDR	Hidden DAC	–	3C6	9 - 72

a. Refer to Chapter 5 (Section 5.4) for the description of this register.
b. Refer to Chapter 7 (Sections 7.2 and 7.3) for the description of these registers.

9.1 SR6: Unlock ALL Extensions Register (Except CL-GD5429)

I/O Port Address: 3C5

Index: 6

Bit	Description	Reset State
7	Don't Care	0
6	Don't Care	0
5	Don't Care	0
4	Unlock	0
3	Don't Care	1
2	Unlock	1
1	Unlock	1
0	Unlock	1

This register is used to enable or disable access to the Extension registers.

Bit	Description
7:0	**Extensions Register Access Value:** If this field is loaded with xxx1x010, it will be read as 00010010, and the Extension registers will be enabled for read and write access. If this field is loaded with any other value, it will be read as 00001111, and the Extension registers will be disabled for read and write access. This register is not implemented on the CL-GD5429. The extension registers on the CL-GD5429 are always unlocked.

9.2 SR7: Extended Sequencer Mode Register

I/O Port Address: 3C5

Index: 7

Bit	Description	Reset State
7	Memory Segment 3 (except CL-GD5420)	0
6	Memory Segment 2 (except CL-GD5420)	0
5	Memory Segment 1 (except CL-GD5420)	0
4	Memory Segment 0 (except CL-GD5420)	0
3	Reserved	
2	Select CRTC Character Clock Divider [1]	(except CL-GD5420)
1	Select CRTC Character Clock Divider [0]	(except CL-GD5420)
0	Select High-Resolution 256-Color (8-bit/pixel)	

This register has several purposes; these are described in the following bit descriptions:

Bit	Description
7:4	**Memory Segment Select (Reserved on CL-GD5420):** If this field is programmed to 0000, the CL-GD542X will be configured as a standard VGA, responding to accesses at Axxx:x or Bxxx:x. or both. Refer to the description of GR6[3:2]. If this field is programmed to any value other than 0000, the CL-GD542X will be configured for 1-Mbyte linear addressing. It will respond to any memory access for which Address bits 23:20 match the Memory Segment Select field. If GRB[5] is programmed to a '1', the CL-GD5426/'28/'29 only will respond to a 2-Mbyte address range. The 1-Mbyte Address Range will have a one-to-one mapping to the 1 Mbyte of installed display memory only if there is a full 1 Mbyte of memory installed, and the chip is configured for extended 256-color Chain-4 addressing. If the chip is configured for unchained, x8 or x16 addressing, or if less than 1 Mbyte of display memory is installed, it will respond to the entire 1-Mbyte range, but address wrapping will take place. If GRB[5] is programmed to a '1', the CL-GD5426/'28/'29 will respond to a 2-Mbyte address range. In this case, SR7[4] is a don't care; the address range must be aligned on a 2 Mbyte boundary. Programming SR7[7:4] to any odd value will result in the next lower Mbyte being used, which is almost certainly not what the programmer had in mind.
3	**Reserved**

9.2 SR7: Extended Sequencer Mode Register *(cont.)*

Bit **Description**

2:1 **Select CRTC Character Clock Divider [1:0] (Except CL-GD5420):** This field selects the CRTC Character Clock Divider mode, as indicated in the following table:

SR7[2]	SR7[1]	Mode
0	0	Normal Operation
0	1	Clock ÷ 2 for 16 bit/pixel data
1	0	Clock ÷ 3 for 24 bit/pixel data
1	1	16 bit/pixel data at pixel rate *(CL-GD5426/'28/'29 only)*

Clock ÷ 2 for 16-Bit/Pixel Data: If this mode is selected, the DAC and Video Shift register is clocked at the VCLK (Data Byte) Rate, and the CRTC is clocked with a character clock of 8 pixels (16 VCLKs). This allows the CRTC timing value for 640 x 480 and 800 x 600 with 16-bit pixels to be programmed in units of an 8-pixel character clock. CR13 (Offset register) will be set to A0h for 640 x 480 mode and C8h for 800 x 600 mode. This mode is available only if the CL-GD542X is configured for a 32-bit DRAM Interface. The hardware cursor x-position may be set in pixel units. The cursor will only be supported with the internal DAC and not through the feature connector. The Cursor Data Invert function will operate on the actual 15-, 16-, or 18-bit RGB data presented to the DAC.

Clock ÷ 3 for 24-Bit/Pixel Data: If this mode is selected, the DAC and Video Shift register is clocked at the VCLK (Data Byte) Rate, and the CRTC is clocked with a character clock of 8 pixels (24 VCLKs). This allows the CRTC timing value for 640 x 480 with 24-bit pixels to be programmed in units of an 8-pixel character clock. CRTC13 (Offset register) will be set to F0h. This mode is available only if the CL-GD542X is configured for a 32-bit DRAM Interface. The Hardware Cursor is not supported in this configuration.

16-Bit/Pixel Data at Pixel Rate: If this mode is selected, the Sequencer will provide 16-bit data to the palette DAC at the displayed Pixel Rate. This allows 5-5-5 or 5-6-5 Color modes to the selected with a 1x VCLK. The data at P[7:0] will be only the low-byte of the Pixel Data. The high-byte is not available externally. This mode provides for 1024 x 768, 5-5-5 or 5-6-5 color with VCLK equal to the Pixel Rate. This is available on the CL-GD5426/'28/'29 only.

0 **Select High Resolution 256-color Mode:** If this bit is programmed to a '1', the Video Shift registers are configured so that one character clock is equal to eight pixels. In addition, true packed-pixel memory addressing is enabled. This is used with all extended resolution packed-pixel modes.
For the CL-GD5429 only, this disables the Set/Reset logic. Write mode 0 writes will write the CPU data regardless of GR1[3:0].

NOTE: In true packed-pixel addressing, consecutive pixels are stored at consecutive addresses. This is in contrast with Chain-4 addressing in which consecutive pixels are stored at every fourth address in display memory.

9.3 SR8: EEPROM Control Register

I/O Port Address: 3C5

Index: 8

Bit	Description
7	EEPROM Input Data
6	Disable MCS16* for Display Memory
5	Latch ESYNC and EVIDEO*
4	Enable EEPROM Data and SK
3	DI to EEPROM
2	SK to EEPROM
1	Enable EEPROM Data In
0	CS Out to EEPROM

This register controls the optional configuration EEPROM. In addition, SR8[6] is used to control MCS16*. The EEPROM contains configuration data such as monitor timing options. Typically, the EEPROM will be a 1K-bit serial EEPROM compatible with the NM93C46N. This option is not available when the CL-GD5424/'26/'28/'29 is configured for the '486 local bus or VESA VL-Bus because pins 73 and 74 are redefined.

Bit	Description
7	**EEPROM Input Data:** This read-only bit reflects the state of the EEDI pin (pin 73) if SR8[1] is a '1'. If SR8[1] is a '0', this bit will always be read as a '0'.
6	**Disable MCS16* for Display Memory:** If this bit is programmed to a '1', accesses to display memory will not cause MCS16* to be made active. This prevents interference in the case where two video cards are installed. This bit is meaningful only when the CL-GD542X is installed on an ISA bus adapter. For all other configurations, it must be programmed to a '0'. In addition, this bit must be programmed to a '0' when programming BitBLTs using system memory for either the source or the destination.
5	**Latch ESYNC and EVIDEO*:** When this bit is programmed to a '0', the ESYNC and EVIDEO* pins are inputs and control the HSYNC, VSYNC, BLANK*, and P[7:0] drivers in the normal manner. When this bit is programmed to a '1', the input levels on ESYNC and EVIDEO* are latched internally and these latched levels control the HSYNC, VSYNC, BLANK*, and P[7:0] drivers. This frees the ESYNC and EVIDEO* pins to control the EEPROM. This bit should be programmed to a '1' prior to setting SR8[4] and it should be programmed to a '0' after clearing SR8[4:0].
4	**Enable EEPROM Data and SK:** When this bit is programmed to a '1', ESYNC and EVIDEO* become outputs and reflect the values in SR8[2] and SR8[3], respectively. When this bit is programmed to a '0', ESYNC and EVIDEO* are inputs.

9.3 SR8: EEPROM Control Register *(cont.)*

Bit	Description
3	**Data to EEPROM:** When SR8[4] is programmed to a '1', the level on EVIDEO* will reflect the value of this bit. This bit is used to control DI of the EEPROM.
2	**SK to EEPROM:** When SR8[4] is programmed to a '1', the level on ESYNC will reflect the value of this bit. This bit is used to control SK of the EEPROM.
1	**Enable EEPROM Data In:** When this bit is programmed to a '1', the level on EEDI will be reflected on SR8[7].
0	**CS out to EEPROM:** The level on EECS (pin 74) will reflect the value of this bit.

9.4 SR9, SRA: Scratch Pad 0, 1 Registers

I/O Port Address: 3C5

Index: 9, A

Bit	Description	Reset State
7	R/W Data [7]	0
6	R/W Data [6]	0
5	R/W Data [5]	0
4	R/W Data [4]	0
3	R/W Data [3]	0
2	R/W Data [2]	0
1	R/W Data [1]	0
0	R/W Data [0]	0

These two registers are reserved for the exclusive use of the CL-GD542X BIOS, and must never be written by any application program. They are listed here only for completeness. The bit assignments are shown in section 1.3 of Appendix E1, *VGA BIOS Specification*.

Bit	Description
7:0	**R/W Data[7:0]:** These bits are reserved for the Cirrus Logic BIOS.

9.5 SRB, SRC, SRD, SRE: VCLK0, 1, 2, 3 Numerator Registers

I/O Port Address: 3C5

Index: B, C, D, E

Bit	Description
7	Reserved
6	VCLK Numerator [6]
5	VCLK Numerator [5]
4	VCLK Numerator [4]
3	VCLK Numerator [3]
2	VCLK Numerator [2]
1	VCLK Numerator [1]
0	VCLK Numerator [0]

These registers, in conjunction with SR1B-SR1E, are used to set the frequency of video clocks. Refer to Appendix B8 for complete programming information for the synthesizers.

Bit **Description**

7 **Reserved**

6:0 **VCLK Numerator [6:0]:** The following table shows the values these registers are loaded with at RESET:

Clock	Freq. (MHz)	N	D	P	Numerator	Denominator/ Prescaler
VCLK0	25.180	102	29	1	66h	3Bh
VCLK1	28.325	91	23	1	5Bh	2Fh
VCLK2	41.165	69	24	0	45h	30h
VCLK3	36.082	126	25	1	7Eh	33h

9.6 SRF: DRAM Control Register

I/O Port Address: 3C5

Index: F

Bit	Description	Reset State
7	DRAM Bank Select (CL-GD5426/'28/'29 only)	–
6	Disable CRT FIFO Fast-Page detection Mode	0
5	CRT FIFO Depth Control (Except CL-GD5420)	0
4	DRAM Data Bus Width [1] (Except CL-GD5420)	0
3	DRAM Data Bus Width [0]	0
2	RAS Timing: MD[27] (Read-only)	CF[11]
1	MCLK Select [1] (Read-only)	CF[10]
0	MCLK Select [0] (Read-only)	CF[9]

This register is used to control the display memory.

Bit	Description
7	**DRAM Bank Select (CL-GD5426/'28/'29 only):** If this bit is programmed to a '1', the CL-GD5426/'28/'29 will be configured for four 256K x 16 DRAMs. OE* (pin 141 is redefined as RAS1*). Refer to Appendix B7. This mode is possible with the CL-GD5426/'28/'29 only. If this bit is programmed to a '0', the CL-GD5426/'28/'29 will be configured for four 512K x 8 DRAMs.
6	**Disable CRT FIFO Fast-Page Mode:** When this bit is programmed to a '1', writes to display memory will take place as random cycles. This bit must be programmed to a '1' when loading font data for page-mode font access and when performing multiple color-expand writes in 16-bit pixel modes. This will avoid CRT FIFO under-runs. This is required for CL-GD5422 and CL-GD5424 only. When this bit is programmed to a '0', consecutive writes to display memory will be executed as Fast-page mode writes whenever possible. The RESET value of this bit is a '0'.
5	**CRT FIFO Depth Control (Except CL-GD5420):** When this bit is programmed to a '0', the CRT FIFO depth will be set to eight levels (32 bits/level). This is the default. This will typically be used for standard video modes and extended 16-color modes. When this bit is programmed to a '1', the CRT FIFO depth will be set to 16 levels (64 bytes). This setting should never be used for any text mode. This will typically be used for any 16-bit or 24-bit pixel modes and extended 8-bit pixel modes. For the CL-GD5429 only, programming this bit to a '1' sets the CRT FIFO depth to 20.

9.6 SRF: DRAM Control Register *(cont.)*

Bit **Description**

4:3 **DRAM Data Bus Width:** This two-bit field is used to specify the display memory Data bus width according to the following table:

SRF[4]	SRF[3]	Data Bus Width	Total Memory
0	0	8 bit (CL-GD5420 only)	256K
0	1	16 bit	512K (1 Mbyte for CL-GD5420 using 512K x 8 DRAMs)
1	0	32 bit (Unavailable in CL-GD5420)	1 Mbyte (2 Mbyte for CL-GD5426/'28/'29)
1	1	Reserved	

These bits have one level of buffering. At the end of each horizontal scanline refresh interval (that is, when Horizontal Blanking begins), these bits are transferred to the timing logic. This avoids changing the timing logic in the middle of a scanline.

2 **RAS Timing MD[27]:** This read-only bit indicates the RAS timing as selected in CF[11]. This is summarized in the following table:

SRF[2] CF[11]	Pull-down on MD[27]	RAS High	RAS Low	Note
0	Yes	3 MCLK	4 MCLK	Extended RAS
1	No	2.5 MCLK	3.5 MCLK	Standard RAS

1:0 **MCLK Select (Read only):** This two-bit read-only field indicates the default MCLK frequency as selected in CF[10:9]. This is summarized in the following table:

SRF[1] CF[10]	SRF[0] CF[9]	Pull-down on MD[26]	Pull-down on MD[25]	Frequency (MHz)
0	0	Yes	Yes	50.11363
0	1	Yes	No	44.74431
1	0	No	Yes	41.16477
1	1	No	No	37.58523

9.7 SR10: Graphics Cursor X Position Register

I/O Port Address: 3C5

Index: 10, 30, 50, 70, 90, B0, D0, F0

Bit	Description	Reset State
7	Cursor X [10]	0
6	Cursor X [9]	0
5	Cursor X [8]	0
4	Cursor X [7]	0
3	Cursor X [6]	0
2	Cursor X [5]	0
1	Cursor X [4]	0
0	Cursor X [3]	0

This register, and bits 7:5 of the index used to access it, are used to define the horizontal (X) pixel offset of the Graphics Cursor. Refer to Appendix D3 for more information regarding the Graphics Cursor.

The data forms the upper-eight bits of the 11-bit position; bits 7:5 of the index form the lower-three bits of the 11-bit position. This allows the entire 11-bit cursor offset to be written in a single 16-bit I/O write. The offset must be placed in AX[15-5], AX[4:0] must be 10000, and DX must be 03C4. If 10, 30, 50...F0 is written to 3C4 without writing to 3C5 (a byte write), then a read of 3C4 will return the previously stored three bits of the cursor position.

Bit	Description
7:0	**Cursor X [10:3]:** This 8-bit field forms the upper-eight bits of the 11-bit horizontal offset of the Graphics Cursor. The index used to access this register forms the low-order-three bits of the 11-bit offset.

9.8 SR11: Graphics Cursor Y Position Register

I/O Port Address: 3C5

Index: 11, 31, 51, 71, 91, B1, D1, F1

Bit	Description	Reset State
7	Cursor Y [10]	0
6	Cursor Y [9]	0
5	Cursor Y [8]	0
4	Cursor Y [7]	0
3	Cursor Y [6]	0
2	Cursor Y [5]	0
1	Cursor Y [4]	0
0	Cursor Y [3]	0

This register, and bits 7:5 of the index used to access it, are used to define the vertical (Y) scanline offset of the Graphics Cursor. Refer to Appendix D3 for more information regarding the Graphics Cursor.

The data forms the upper-eight bits of the 11-bit position; bits 7:5 of the index form the lower-three bits of the 11-bit position. This allows the entire 11-bit cursor offset to be written in a single 16-bit I/O write. The offset must be placed in AX[15-5], AX[4:0] must be 10001, and DX must be 03C4. If 11, 31, 51...F1 is written to 3C4 without writing to 3C5 (a byte write), then a read of 3C4 will return the previously stored three bits of the cursor position.

For the CL-GD5424/'26/'28, the hardware cursor cannot be used if CR17[2] is programmed to a '1' (Multiply Vertical registers by two). The CL-GD5429 does not have this restriction.

Bit	Description
7:0	**Cursor Y[10:3]:** This 8-bit field forms the upper-eight bits of the 11-bit horizontal offset of the Graphics Cursor. The index used to access this register forms the low-order-three bits of the 11-bit offset.

9.9 SR12: Graphics Cursor Attributes Register

I/O Port Address: 3C5

Index: 12

Bit	Description
7	Overscan Color Protect (CL-GD5424/'26/'28/'29 only)
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Cursor Size Select (Reserved in CL-GD5420)
1	Allow Access to DAC Extended Colors
0	Graphics Cursor Enable

This register is used to enable or disable the Graphics Cursor, as well as set the size and the palette DAC LUT entries used to define the colors. Refer to Appendix D3 for a complete programming guide for the Graphics Cursor.

Bit	Description
7	**Overscan Color Protect (CL-GD5424/'26/'28/'29 only):** If this bit is programmed to a '1', the border color will be DAC LUT entry 258. Note that entry 258 can be accessed only if SR12[1] is programmed to a '1'. If this bit is programmed to a '0', the border color is normal; that is, the contents of the palette pointed to by AR11. AR11 normally contains a '0', and palette entry '0' normally contains values corresponding to black.
6:3	**Reserved**
2	**Cursor Size Select (Reserved in CL-GD5420):** If this bit is programmed to a '0', the Graphics Cursor will be 32 x 32 pixels. If it is programmed to a '1', the Graphics Cursor will be 64 x 64 pixels. It must always be programmed to a '0' for the CL-GD5420.
1	**Allow Access to DAC Extended Colors:** If this bit is programmed to a '1', DAC lookup table entries 256 and 257 are accessible as locations x0h and xFh. Entry 256 will be used as the cursor background and entry 257 will be used as the cursor foreground. This provides for a cursor that is completely independent of the display data colors. Entry 258 is accessible as location x2h, and provides a selected overscan color. If this bit is programmed to a '0', the DAC LUT will be VGA-compatible.
0	**Graphics Cursor Enable:** If this bit is programmed to a '1', the Graphics Cursor will be enabled and will appear on the screen. If it is programmed to a '0', the Graphics Cursor will be disabled and will not appear on the screen.

9.10 SR13: Graphics Cursor Pattern Address Offset Register

I/O Port Address: 3C5

Index: 13

Bit	Description
7	Reserved
6	Reserved
5	Cursor Select [5]
4	Cursor Select [4]
3	Cursor Select [3]
2	Cursor Select [2]
1	Cursor Select [1]
0	Cursor Select [0]

This register is used to select one of 64-cursor patterns (32 x 32 cursor) or one of 16-cursor patterns (64 x 64 cursor). Refer to Appendix D3 for a complete programming guide for the Graphics Cursor.

Bit	Description
7:6	**Reserved**
5:0	**Cursor Select (32 x 32 Cursor):** This six-bit field is used to select one of 64 possible cursor patterns stored at the top (highest addressed 16K bytes) of display memory. This definition of these six bits is valid only if SR12[2] is programmed to a '0'.
5:2	**Cursor Select (64 x 64 Cursor) (Except CL-GD5420):** This 4-bit field is used to select one of 16 possible cursor patterns stored at the top (highest addressed 16K bytes) of display memory. This definition of these four bits is valid only if SR12[2] is programmed to a '1'. SR13[1:0] are ignored in this case.

9.11 SR14, SR15: Scratch Pad 2, 3 Registers (CL-GD5426/'28/'29 only)

I/O Port Address: 3C5

Index:14, 15

Bit	Description	Reset State
7	R/W Data [7]	0
6	R/W Data [6]	0
5	R/W Data [5]	0
4	R/W Data [4]	0
3	R/W Data [3]	0
2	R/W Data [2]	0
1	R/W Data [1]	0
0	R/W Data [0]	0

These two registers are reserved for the exclusive use of the CL-GD542X BIOS and must never be written by any application program. They are listed here only for completeness.

Bit	Description
7:0	**R/W Data[7:0]:** These bits are reserved for the Cirrus Logic BIOS.

9.12 SR16: Performance Tuning Register (CL-GD5424/'26/'28/'29 only)

I/O Port Address: 3C5

Index:16

Bit	Description	Reset State
7	RDY Delay for I/O [1]	1
6	RDY Delay for I/O [0]	1
5	RDY Delay for Memory Write [1]	1
4	RDY Delay for Memory Write [0]	1
3	FIFO Demand Threshold [3]	0
2	FIFO Demand Threshold [2]	0
1	FIFO Demand Threshold [1]	0
0	FIFO Demand Threshold [0]	0

This register is used to control the delay from ADS# to RDY#, and to control the threshold at which the CRT FIFO will be refilled. This register is defined only for the CL-GD5424, CL-GD5426, and CL-GD5428. This register must never be written by an application program. It is listed here for completeness only.

Bit **Description**

7:6 **RDY Delay for I/O [1:0]:** This field is used to control the delay from ADS# to RDY# for I/O cycles. This field applies only when the CL-GD5424/'26/'28/'29 is configured for local bus. The following table summarizes the values:

SR16[7]	SR16[6]	CPU1X Clock Delay	Note
0	0	1	
0	1	1	
1	0	2	
1	1	2	Default

9.12 SR16: Performance Tuning Register (CL-GD5424/'26/'28/'29 only) *(cont.)*

Bit **Description**

5:4 **RDY Delay for Memory Write [1]:** This field is used to control the delay from ADS# to RDY# for memory write cycles. This field applies only when the CL-GD5424/'26/'28/'29 is configured for local bus. The following table summarizes the values:

SR16[5]	SR16[4]	CPU1X Clock Delay CL-GD5424/'26/'28	CL-GD5429	Note
0	0	2	1	
0	1	3	2	
1	0	4	3	
1	1	5	4	Default

The value programmed into this field must satisfy the following inequality:
ClockDelay x CPU Clock Period > 3 x MCLK Period + 2 ns.

3:0 **FIFO Demand Threshold [3:0]:** The value written to this field will select the level at which the Sequencer will begin cycles to refill the CRT FIFO (and thereby hold off CPU cycles or pre-empt fast page mode BLT cycles). For each Video mode and MCLK frequency, there will be an optimum value that will most efficiently use the DRAM. These values are automatically programmed by the Cirrus Logic, Inc. BIOS.

9.13 SR17: Configuration Readback and Extended Control Register (Except CL-GD5420)

I/O Port Address: 3C5

Index:17

Bit	Description	Reset State
7	Reserved	
6	Memory-mapped I/O Address (CL-GD5429 only)	
5	System Bus Select [2]: MD30 (Read-only)	CF[14]
4	System Bus Select [1]: MD23 (Read-only)	CF[7]
3	System Bus Select [0]: MD21 (Read-only)	CF[5]
2	Enable Memory-mapped I/O (CL-GD5429 only)	
1	Power-down Palette Memory (CL-GD5429 only)	
0	Shadow DAC Writes on Local Bus	1

This register contains a read-only field that allows the BIOS to determine the bus type. In addition, bit 0 can be used to control DAC shadowing.

Bit	Description
7	**Reserved**
6	**Memory-mapped I/O Address (CL-GD5429 only):** If Memory-mapped I/O is not enabled, or if linear addressing is not enabled, this bit is ignored. If linear addressing and Memory-mapped I/O are both enabled, this bit has the following meaning. If this bit is programmed to a '0', the address space for Memory-mapped I/O will be 256 bytes beginning at B800:0. If this bit is programmed to a '1', the address space for Memory-mapped I/O will be the last 256 bytes of the 2 Mbyte of linear address space.
5:3	**System Bus Select [2:0] (Read-only):** This read-only field will reflect Configuration bits CF[14, 7, 5], the System Bus Select bits. See Appendix B9 for the definition of these bits. This field is intended for use by the Cirrus Logic BIOS.
2	**Enable Memory-mapped I/O (CL-GD5429 only):** If this bit is programmed to a '0', Memory-mapped I/O is not enabled. If this bit is programmed to a '1', the BLT registers (GR0, GR1, GR10-11, and GR20-32) will be addressed as a 256 byte block of memory. This allows much faster access. See Appendix B20, *Memory-mapped I/O*, for more information.
1	**Power-down Palette Memory (CL-GD5429 only):** If this bit is programmed to a '0', the DAC Palette Memory (SRAM) is clocked and functions normally. If this bit is programmed to a '1', the DAC Palette Memory is not clocked. This reduces power in the chip.
0	**Shadow DAC Writes on Local Bus:** If this bit is programmed to a '0', writes to the internal DAC will return LBA# and RDY# normally. If this bit is programmed to a '1', writes to the DAC addresses will accept data, but will not return LBA# or RDY#, causing the write to be passed on to an external DAC on the ISA bus. The reset state of this bit is a '1'. Reads to the DAC addresses will always operate normally.

9.14 SR18: Signature Generator Control Register (Except CL-GD5420)

I/O Port Address: 3C5

Index:18

Bit	Description
7	Disable MCLK Driver (CL-GD5424/'26/'28/'29 only)
6	Disable DCLK/Pixel Bus Drivers (CL-GD5424/'26/'28/'29 only)
5	Enable Data Generator (CL-GD5428/'29 only)
4	Pixel Bus Select [2]
3	Pixel Bus Select [1]
2	Pixel Bus Select [0]
1	Reset Signature Generator
0	Signal Generator Enable/Status

This register is used to control and monitor the status of the Signature Generator. The CL-GD542X Signature Generator is used for board-level testing of the video sub-system. Refer to Appendix B11 for a complete description of the Signature Generator.

Bit	Description
7	**Disable MCLK Driver (CL-GD5424/'26/'28/'29 only):** If this bit is programmed to a '1', the MCLK driver is disabled. This is intended for testing. If this bit is programmed to a '0', the MCLK driver operates normally.
6	**Disable DCLK/Pixel Bus Drivers (CL-GD5424/'26/'28/'29 only):** If this bit is programmed to a '1', the DCLK and Pixel bus drivers are disabled. This is intended for testing. If this bit is programmed to a '0', the DCLK and Pixel bus drivers operate normally.
5	**Enable Data Generator (CL-GD5428/'29 only):** If this bit is programmed to a '1', pseudo-random data will be placed on the Memory Data bus. This is used in conjunction with the Signature Generator for factory testing only.

9.14 SR18: Signature Generator Control Register (Except CL-GD5420) *(cont.)*

Bit **Description**

4:2 **Pixel Bus Select [2:0]:** This field is used to select the bit of the Pixel bus that will be used as the input for the Signature Generator according to the following table:

SR18[4]	SR18[3]	SR18[2]	P-Bus Bit
0	0	0	P[0]
0	0	1	P[1]
0	1	0	P[2]
0	1	1	P[3]
1	0	0	P[4]
1	0	1	P[5]
1	1	0	P[6]
1	1	1	P[7]

1 **Reset Signature Generator:** When this bit is programmed to a '1', the Signature Generator is reset to an initial, defined, condition. When it is programmed to a '0', the Signature Generator is allowed to run under the control of SR18[0].

0 **Signature Generator Enable/Status:** When this bit is programmed to a '1', the Signature Generator will begin operation on the next VSYNC. It will accumulate a signature from the Pixel Bus bit chosen by SR18[4:2] for one video frame and will then stop, forcing this bit to a '0'. The program can determine when the signature is complete by monitoring this bit.

9.15 SR19: Signature Generator Result Low Byte Register (Except CL-GD5420)

I/O Port Address: 3C5

Index: 19

Bit	Description	Reset State
7	Signature Generator Result [7]	0
6	Signature Generator Result [6]	0
5	Signature Generator Result [5]	0
4	Signature Generator Result [4]	0
3	Signature Generator Result [3]	0
2	Signature Generator Result [2]	0
1	Signature Generator Result [1]	0
0	Signature Generator Result [0]	0

This register is used to read the low-order byte of the Signature Generator result. The CL-GD542X Signature Generator is used for board-level testing of the video sub-system. Refer to Appendix B11 for a complete description of the Signature Generator.

Bit	Description
7:0	**Signature Generator Result [7:0]**

9.16 SR1A: Signature Generator Result High Byte Register (Except CL-GD5420)

I/O Port Address: 3C5

Index: 1A

Bit	Description	Reset State
7	Signature Generator Result [15]	0
6	Signature Generator Result [14]	0
5	Signature Generator Result [13]	0
4	Signature Generator Result [12]	0
3	Signature Generator Result [11]	0
2	Signature Generator Result [10]	0
1	Signature Generator Result [9]	0
0	Signature Generator Result [8]	0

This register is used to read the high-order byte of the Signature Generator result. The CL-GD542X Signature Generator is used for board-level testing of the video sub-system. Refer to Appendix B11 for a complete description of the Signature Generator.

Bit	Description
7:0	**Signature Generator Result [15:8]**

9.17 SR1B, SR1C, SR1D, SR1E: VCLK Denominator and Post Scalar Value Registers

I/O Port Address: 3C5

Index: 1B, 1C, 1D, 1E

Bit	Description
7	Reserved
6	Reserved
5	VCLK Denominator [4]
4	VCLK Denominator [3]
3	VCLK Denominator [2]
2	VCLK Denominator [1]
1	VCLK Denominator [0]
0	VCLK Post Scalar (÷2)

This register, in conjunction with SRB, is used to determine the frequency of video clock 0 (VCLK0). Refer to Appendix B8 for complete programming information for the synthesizers. The reset values for these four registers are shown in the table in the VCLK Numerator.

Bit	Description
7:6	**Reserved**
5:1	**VCLK Denominator [4:0]**
0	**VCLK Post Scalar (÷2)**

9.18 SR1F: BIOS ROM Write Enable and MCLK Select Register (CL-GD5424/'26/'28/'29 only)

I/O Port Address: 3C5

Index: 1F

Bit	Description	Reset State
7	Enable BIOS Write	0
6	Use MCLK as VCLK (CL-GD5428/'29 only)	
5	MCLK Frequency [5]	0
4	MCLK Frequency [4]	(Refer to MCLK Table below)
3	MCLK Frequency [3]	"
2	MCLK Frequency [2]	"
1	MCLK Frequency [1]	"
0	MCLK Frequency [0]	"

This register is defined only for the CL-GD5424/'26/'28/'29. It allows the MCLK frequency to be programmed. In addition, bit 7 is used to allow writing to the BIOS FLASH ROM. This register should never be programmed by an applications program; it is listed for completeness only.

Bit	Description
7	**Enable BIOS Write:** If this bit is programmed to a '1', host writes to memory addresses in the range C000:0 through C7FF:F will make EROM* active. This allows the reprogramming of the BIOS if it is stored in FLASH ROM. This function is not currently supported by the Cirrus Logic BIOS.
6	**Use MCLK as VCLK (CL-GD5428/'29 only):** If this bit is programmed to a '0', the VCLK Synthesizer will operate normally. If this bit is programmed to a '1', VCLK is derived from MCLK as follows:

SR1F[6]	SR1E[0]	VLCK Source
0	x	VCLK (Normal Operation)
1	0	VCLK = MCLK
1	1	VCLK = MCLK/2

9.18 SR1F: BIOS ROM Write Enable and MCLK Select Register (CL-GD5424/'26/'28/'29 only) *(cont.)*

Bit **Description**

5:0 **MCLK Frequency [5:0]:** This field directly programs the MCLK frequency as indicated in the following equation:

MCLK = Reference ÷ 8 x SR1F[5:0]

= 1.79 x SR1F[5:0], assuming a reference frequency of 14.3 MHz.

This field may be programmed with any value from 4 to 28 (decimal). The CL-GD5429 may be programmed to any value to 33 (decimal). Refer to Appendix B7 for information regarding the DRAM specification requirements for various MCLK frequencies. The following table shows examples assuming a reference frequency of 14.31818 MHz:

SR1F[5:0] (Decimal)	SR1F[5:0] (Hex)	MCLK Frequency	Corresponding CF[10:9]
21	15	37.585 MHz	11
23	17	41.165 MHz	10
25	19	44.744 MHz	01
28	1C	50.114 MHz	00
32	20	57.273 MHz	-
34	22	60.852 MHz	-

NOTE: The appearance of any frequency above 50 MHz in this table is not to be taken as a guarantee that any particular Cirrus Logic product will operate at that frequency or that DRAMs are available which will support that frequency.

9.19 GR9: Offset Register 0

I/O Port Address: 3CF

Index:9

Bit	Description	Reset State
7	Offset 0 [7]	0
6	Offset 0 [6]	0
5	Offset 0 [5]	0
4	Offset 0 [4]	0
3	Offset 0 [3]	0
2	Offset 0 [2]	0
1	Offset 0 [1]	0
0	Offset 0 [0]	0

This register is used to provide access to up to 1 Mbyte of display memory with 4K bytes granularity or 2 Mbytes of display memory with 16K bytes granularity. The contents of this register are added to A[19:12] when Extension register GRB[0] is programmed to '0', and when GRB[0] is programmed to '1' and SA15=0. For the CL-GD5426/'28 only, if GRB[5] is programmed to a '1', bits 6:0 of this register are added to A[20:14] to provide access to up to 2 Mbytes of display memory with 16K bytes granularity.

The Display Memory Address, prior to being modified by address wrap controls is called XMA. It is the sum of XA and an Offset register. XA is the address on the bus with bits 16 and 15 possibly forced to a '0' as indicated in the following table:

Configuration	XA[16]	XA[15]	XA[14:0]
128K Memory: GR6[3:2]=0,0	SA[16]	SA[15]	SA[14:0]
64K Memory: GR6[3:2]=0,1 **AND** Offset 1 Disabled: GRB[0]=0	0	SA[15]	SA[14:0]
64K Memory: GR6[3:2]=0,1 **OR** Offset 1 Enabled: GRB[0]=1	0	0	SA[14:0]

The XA address is summed with the contents of an Offset register with one of three relative alignments according to the configuration. These are indicated in the three diagrams that follow:

1 Mbyte Memory, 4K Granularity, VGA Mapping:

0	0	0	XA[16]	XA[15]	SA[14]	SA[13]	SA[12]
+OFF[7]	OFF[6]	OFF[5]	OFF[4[	OFF[3]	OFF[2]	OFF[1]	OFF[0]
XMA[19]	XMA[18]	XMA[17]	XMA[16]	XMA[15]	XMA[14]	XMA[13]	XMA[12]

9.19 GR9: Offset Register 0 *(cont.)*

2 Mbyte Memory, 16K Granularity, VGA Mapping:

0	0	0	0	XA[16]	XA[15]	SA[14]	SA[13]	SA[12]
+OFF[6]	OFF[5]	OFF[4]	OFF[3]	OFF[2]	OFF[1]	OFF[0]	0	0
XMA[20]	XMA[19]	XMA[18]	XMA[17]	XMA[16]	XMA[15]	XMA[14]	XMA[13]	XMA[12]

1 or 2 Mbyte Memory, 16K Granularity, Linear Addressing:

LA[20]	LA[19]	LA[18]	LA[17]	SA[16]	SA[15]	SA[14]	SA[13]	SA[12]
+OFF[6]	OFF[5]	OFF[4]	OFF[3]	OFF[2]	OFF[1]	OFF[0]	0	0
XMA[20]	XMA[19]	XMA[18]	XMA[17]	XMA[16]	XMA[15]	XMA[14]	XMA[13]	XMA[12]

Refer to Appendix D1 for programming notes regarding extended addressing.

Bit	Description
7:0	**Offset 0 [7:0]:** This value is added to A[19:12] to provide the address into display memory. This Offset register is selected when GRB[0] is programmed to a '0' or when GRB[0] is a '1' and SA15=0.

9.20 GRA: Offset Register 1

I/O Port Address: 3CF

Index: A

Bit	Description	Reset State
7	Offset 1 [7]	0
6	Offset 1 [6]	0
5	Offset 1 [5]	0
4	Offset 1 [4]	0
3	Offset 1 [3]	0
2	Offset 1 [2]	0
1	Offset 1 [1]	0
0	Offset 1 [0]	0

This register is used to provide access to up to 1 Mbyte of display memory with 4K bytes granularity. The contents of this register are added to A[19:12] when Extension register GRB[0] is programmed to '1' and SA15=1. For the CL-GD5426/'28/'29 only, if GRB[5] is programmed to a '1', bits 6:0 of this register are added to A[20:14] to provide access to up to 2 Mbytes of display memory with 16K bytes granularity.

Bit	Description
7:0	**Offset 1 [7:0]:** This value is added to A[19:12] to provide the address into display memory. This Offset register is selected when GRB[0] is programmed to a '1' and SA15=1. If GRB[0] is programmed to a '0', this register is unused.

9.21 GRB: Graphics Controller Mode Extensions Register

I/O Port Address: 3CF

Index: B

Bit	Description
7	Reserved
6	Reserved
5	Offset Granularity (CL-GD5426/'28/'29 only)
4	Enable Enhanced Writes for 16-bit pixels
3	Enable Eight Byte Data Latches
2	Enable Extended Write Modes
1	Enable BY8 Addressing
0	Enable Offset Register 1

This register is used to enable or disable extended write modes. These extended modes provide enhanced performance.

Bit	Description
7:6	**Reserved**
5	**Offset Granularity (CL-GD5426/'28/'29 only):** This bit is defined for the CL-GD5426/'28/'29 only. If this bit is programmed to a '1', the Offset registers are redefined as containing bits [6:0] which are added to Address bits [20:14] to provide access to 2 Mbytes of display memory with 16K bytes granularity. SR7[4] (low-order bit of 1-Mbyte address page) becomes a don't care.
4	**Enable Enhanced Writes for 16-bit pixels:** When this bit and GRB[2] are both programmed to ones, the CL-GD542X will execute enhanced Write mode 4 and 5 writes. In particular, • **BY16 Addressing Enabled:** The system address is shifted by four relative to true packed-pixel addressing so that each system byte address points to a different 8 pixel (16 byte) block in display memory. • **16 Byte Transfer Enabled:** Up to 16 bytes (8 pixels) can be written into display memory for each CPU byte transfer. • **GR10 and GR11 Enabled:** GR10 and GR11 are enabled as foreground and background color extensions. • **SR2 Doubling Enabled:** Each bit of SR2 is used as a pixel write mask for two bytes (one pixel).
3	**Enable Eight Byte Data Latches:** If this bit is programmed to a '1', the display memory latches are eight bytes wide rather than the normal four.

9.21 GRB: Graphics Controller Mode Extensions Register *(cont.)*

Bit	Description
2	**Enable Extended Write Modes:** If this bit is programmed to a '1', the CL-GD542X will execute extended mode write. In particular: • **8 Byte Transfer Enabled:** Up to 8 bytes (8 pixels) can be written into display memory for each CPU byte transferred. If GRB[4] is programmed to a '1'; up to 16 bytes can be written for color expansion. • **GR5[2] Enabled:** Extended Write modes 4 and 5 can be enabled. • **GR0 Extended:** register GR0 is extended from 4 bits to 8 bits. • **GR1 Extended:** register GR1 is extended from 4 bits to 8 bits. • **SR2 Extended:** register SR2 is extended from 4 bits to 8 bits. • **GRB[4] Enabled:** GRB[2] must be programmed to a '1' to enable GRB[4].
1	**Enable BY8 Addressing:** The system address is shifted by 3 relative to true packed-pixel addressing so that each system byte address points to a different 8-pixel (8-byte) block in display memory. This bit is a don't care if GRB[4] is programmed to a '1'.
0	**Enable Offset Register 1:** If this bit is programmed to a '1', then SA15 will be used to choose between Offset register 0 and 1. If this bit is programmed to a '0', then Offset register 0 will always be chosen regardless of the value of SA15. This bit must always be programmed to a '0' for 1 Mbyte of linear addressing.

9.22 GRC: Color Key Compare Register (CL-GD5424/'26/'28/'29 only)

I/O Port Address: 3CF

Index: C

Bit	Description	Reset State
7	Color Key Compare [7]	1
6	Color Key Compare [6]	1
5	Color Key Compare [5]	1
4	Color Key Compare [4]	1
3	Color Key Compare [3]	1
2	Color Key Compare [2]	1
1	Color Key Compare [1]	1
0	Color Key Compare [0]	1

This register contains an 8-bit value that is compared to the video data. A match, when Mode Switching 10 or 11 is chosen, will cause the pixel to be replaced with data from the feature connector. Refer to Appendix B14.

Bit	Description
7:0	**Color Key Compare [7:0]:** This value is the color key used with Mode Switching 10 and 11. Refer to Appendix B14.

9.23 GRD: Color Key Compare Mask Register (CL-GD5424/'26/'28/'29 only)

I/O Port Address: 3CF

Index: D

Bit	Description	Reset State
7	Color Key Compare Mask [7]	0
6	Color Key Compare Mask [6]	0
5	Color Key Compare Mask [5]	0
4	Color Key Compare Mask [4]	0
3	Color Key Compare Mask [3]	0
2	Color Key Compare Mask [2]	0
1	Color Key Compare Mask [1]	0
0	Color Key Compare Mask [0]	0

This register contains an 8-bit mask under which the color key compare is made. A '1' will cause to corresponding bit to *not* participate in the compare. Refer to Appendix B14.

Bit	Description
7:0	**Color Key Compare Mask [7:0]:** This value is the mask under which the color key compare is made. Refer to Appendix B14.

9.24 GRE: Miscellaneous Control Register (CL-GD5428/'29 only)

I/O Port Address: 3CF

Index: E

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Static Clock (CL-GD5429 only)
2	Static VSYNC (CL-GD5429 only)
1	Static HSYNC (CL-GD5429 only)
0	DCLK Output (÷2)

This register contains bits relating to power management.

Bit	Description
7:4	**Reserved**
3	**Static Clock (CL-GD5429 only):** If this bit is programmed to a '1', the CL-GD5429 will be placed in Static Clock mode. VCLK and MCLK are gated off, so that the chip does not dissipate any dynamic power. The RAMDAC is powered down. DRAM refresh continues. **NOTE:** When the chip is in Static Clock mode, memory accesses are not possible. The only host access that is allowed is an I/O cycle to remove the chip from Static Clock mode.
2	**Static VSYNC (CL-GD5429 only):** If this bit is programmed to a '1', the VSYNC output will be static. The level will be as programmed in MISC[7]. In addition, the RAMDAC will be powered down. If this bit is programmed to a '0', the VSYNC pin will function as programmed by the CRTC registers. See Appendix B21, *Power Management*, for detailed information regarding 'Green Computing'.
1	**Static HSYNC (CL-GD5429 only):** If this bit is programmed to a '1', the HSYNC output will be static. The level will be as programmed in MISC[6]. In addition, the RAMDAC will be powered down. If this bit is programmed to a '0', the HSYNC pin will function as programmed by the CRTC registers. See Appendix B21, *Power Management*, for detailed information regarding 'Green Computing'.
0	**DCLK Output (÷2):** If this bit is programmed to a '0', the CL-GD542X operates normally. If this bit is programmed to a '1', the CL-GD5428 will simulate external DAC Clocking mode 1. The rising edge of DCLK may be used to clock the low byte of 16-bit data; the falling edge of DCLK may be used to clock the high byte of 16-bit data.

9.25 GR10: 16-bit Pixel Background Color High Byte Register

I/O Port Address: 3CF

Index: 10

Bit	Description
7	Background Color [15]
6	Background Color [14]
5	Background Color [13]
4	Background Color [12]
3	Background Color [11]
2	Background Color [10]
1	Background Color [9]
0	Background Color [8]

This register contains the high-order 8 bits of the extended background color for Extended Write mode 5 and Color Expanded BitBLT operations.

Bit	Description
7:0	**Background Color [15:8]:** These are the high-order 8 bits of the background color for Write mode 5.

9.26 GR11: 16-bit Pixel Foreground Color High Byte Register

I/O Port Address: 3CF

Index: 11

Bit	Description
7	Foreground Color [15]
6	Foreground Color [14]
5	Foreground Color [13]
4	Foreground Color [12]
3	Foreground Color [11]
2	Foreground Color [10]
1	Foreground Color [9]
0	Foreground Color [8]

This register contains the high-order 8 bits of the extended foreground color for Extended Write modes 5 and 4 and Color Expanded BitBLT operations.

Bit	Description
7:0	**Foreground Color [15:8]:** These are the high-order 8 bits of the foreground color for Extended Write modes 5 and 4.

9.27 GR20: BLT Width Low Register (CL-GD5426/'28/'29 only)

I/O Port Address: 3CF

Index: 20

Bit	Description
7	BLT Width [7]
6	BLT Width [6]
5	BLT Width [5]
4	BLT Width [4]
3	BLT Width [3]
2	BLT Width [2]
1	BLT Width [1]
0	BLT Width [0]

This register contains the low-order 8 bits of the 11-bit value specifying the width-1, in bytes, of the areas involved in a BitBLT. Refer to Appendix D8, *BitBLT Engine**.

Bit	Description
7:0	**BLT Width [7:0]:** This field is the low-order 8 bits of the BLT Width. Refer to Appendix D8.

* For Sections 9.27 through 9.48 refer to Appendix D8, *BitBLT Engine*, for additional detailed information.

9.28 GR21: BLT Width High Register (CL-GD5426/'28/'29 only)

I/O Port Address: 3CF

Index: 21

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	BLT Width [10]
1	BLT Width [9]
0	BLT Width [8]

This register contains the high-order 3 bits of the 11-bit value specifying the width-1, in bytes, of the areas involved in a BitBLT.

Bit	Description
7:3	**Reserved**
2:0	**BLT Width [10:8]:** This field is the high-order 3 bits of the BLT Width.

9.29 GR22: BLT Height Low Register (CL-GD5426/'28/'29 only)

I/O Port Address: 3CF

Index: 22

Bit	Description
7	BLT Height [7]
6	BLT Height [6]
5	BLT Height [5]
4	BLT Height [4]
3	BLT Height [3]
2	BLT Height [2]
1	BLT Height [1]
0	BLT Height [0]

This register contains the low-order 8 bits of the 10-bit value specifying the height-1, in scanlines, of the areas involved in a BitBLT.

Bit	Description
7:0	**BLT Height [7:0]:** This field is the low-order 8 bits of the BLT height.

9.30 GR23: BLT Height High Register (CL-GD5426/'28/'29 only)

I/O Port Address: 3CF

Index: 23

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Reserved
1	BLT Height [9]
0	BLT Height [8]

This register contains the high-order 2 bits of the 10-bit value specifying the Height-1, in scanlines, of the areas involved in a BitBLT.

Bit	Description
7:2	**Reserved**
1:0	**BLT Height [9:8]:** This field is the high-order 2 bits of the BLT Height.

9.31 GR24: BLT Destination Pitch Low Register (CL-GD5426/'28/'29 only)

I/O Port Address: 3CF

Index: 24

Bit	Description
7	BLT Destination Pitch [7]
6	BLT Destination Pitch [6]
5	BLT Destination Pitch [5]
4	BLT Destination Pitch [4]
3	BLT Destination Pitch [3]
2	BLT Destination Pitch [2]
1	BLT Destination Pitch [1]
0	BLT Destination Pitch [0]

This register contains the low-order 8 bits of the 12-bit (13-bit for CL-GD5429 only) value specifying the destination pitch (that is, the scanline-to-scanline byte address offset) of the areas involved in a BitBLT.

Bit	Description
7:0	**BLT Destination Pitch [7:0]:** This field is the low-order 8 bits of the BLT destination pitch.

9.32 GR25: BLT Destination Pitch High Register (CL-GD5426/'28/'29 only)

I/O Port Address: 3CF

Index: 25

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	BLT Destination Pitch [12] (CL-GD5429 only)
3	BLT Destination Pitch [11]
2	BLT Destination Pitch [10]
1	BLT Destination Pitch [9]
0	BLT Destination Pitch [8]

This register contains the high-order 4 bits (5 bits for CL-GD5429) of the 12-bit (13-bit for CL-GD5429) value specifying the Destination Pitch (that is, the scanline-to-scanline byte address offset) of the areas involved in a BitBLT.

Bit	Description
7:5	**Reserved**
4	**BLT Destination Pitch [12] (CL-GD5429 only):** This is the high-order bit of the BLT Destination Pitch for the CL-GD5429 only.
3:0	**BLT Destination Pitch [11:8]:** This field is the high-order 4 bits of the BLT Destination Pitch. Bit 4 is also used for the CL-GD5429 only.

9.33 GR26: BLT Source Pitch Low Register (CL-GD5426/'28/'29 only)

I/O Port Address: 3CF

Index: 26

Bit	Description
7	BLT Source Pitch [7]
6	BLT Source Pitch [6]
5	BLT Source Pitch [5]
4	BLT Source Pitch [4]
3	BLT Source Pitch [3]
2	BLT Source Pitch [2]
1	BLT Source Pitch [1]
0	BLT Source Pitch [0]

This register contains the low-order 8 bits of the 12-bit (13-bit for CL-GD5429 only) value specifying the source pitch (that is, the scanline-to-scanline byte address offset) of the areas involved in a BitBLT.

Bit	Description
7:0	**BLT Source Pitch [7:0]:** This field is the low-order 8 bits of the BLT source pitch.

9.34 GR27: BLT Source Pitch High Register (CL-GD5426/'28/'29 only)

I/O Port Address: 3CF

Index: 27

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	BLT Source Pitch [12] (CL-GD5429 only)
3	BLT Source Pitch [11]
2	BLT Source Pitch [10]
1	BLT Source Pitch [9]
0	BLT Source Pitch [8]

This register contains the high-order 4 (5 for CL-GD5429 only) bits of the 12-bit (13 for CL-GD5429 only) value specifying the source pitch (that is, the scanline-to-scanline byte address offset) of the areas involved in a BitBLT.

Bit	Description
7:5	**Reserved**
4	**BLT Source Pitch [12] (CL-GD5429 only):** This is the high-order bit of the BLT source pitch for the CL-GD5429 only.
3:0	**BLT Source Pitch [11:8]:** This field is the high-order 4 bits of the BLT source pitch. Bit 4 is also used for the CL-GD5429 only.

9.35 GR28: BLT Destination Start Low Register (CL-GD5426/'28/'29 only)

I/O Port Address: 3CF

Index: 28

Bit	Description
7	BLT Destination Start [7]
6	BLT Destination Start [6]
5	BLT Destination Start [5]
4	BLT Destination Start [4]
3	BLT Destination Start [3]
2	BLT Destination Start [2]
1	BLT Destination Start [1]
0	BLT Destination Start [0]

This register contains the low-order 8 bits of the 21-bit value specifying the byte address of the beginning destination pixel for a BitBLT.

Bit	Description
7:0	**BLT Destination Start [7:0]:** This field is the low-order 8 bits of the BLT Destination Start.

9.36 GR29: BLT Destination Start Mid Register (CL-GD5426/'28/'29 only)

I/O Port Address: 3CF

Index: 29

Bit	Description
7	BLT Destination Start [15]
6	BLT Destination Start [14]
5	BLT Destination Start [13]
4	BLT Destination Start [12]
3	BLT Destination Start [11]
2	BLT Destination Start [10]
1	BLT Destination Start [9]
0	BLT Destination Start [8]

This register contains the middle 8 bits of the 21-bit value specifying the byte address of the beginning destination pixel for a BitBLT.

Bit	Description
7:0	**BLT Destination Start [15:8]:** This field is the middle 8 bits of the BLT Destination Start.

9.37 GR2A: BLT Destination Start High Register (CL-GD5426/'28/'29 only)

I/O Port Address: 3CF

Index: 2A

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	BLT Destination Start [20]
3	BLT Destination Start [19]
2	BLT Destination Start [18]
1	BLT Destination Start [17]
0	BLT Destination Start [16]

This register contains the high-order 5 bits of the 21-bit value specifying the byte address of the beginning destination pixel for a BitBLT.

Bit	Description
7:5	**Reserved**
4:0	**BLT Destination Start [20:16]:** This field is the high-order 5 bits of th BLT Destination Start.

9.38 GR2C: BLT Source Start Low Register (CL-GD5426/'28/'29 only)

I/O Port Address: 3CF

Index: 2C

Bit	Description
7	BLT Source Start [7]
6	BLT Source Start [6]
5	BLT Source Start [5]
4	BLT Source Start [4]
3	BLT Source Start [3]
2	BLT Source Start [2]
1	BLT Source Start [1]
0	BLT Source Start [0]

This register contains the low-order 8 bits of the 21-bit value specifying the byte address of the beginning source pixel for a BitBLT.

Bit	Description
7:0	**BLT Source Start [7:0]:** This field is the low-order 8 bits of the BLT Source Start.

9.39 GR2D: BLT Source Start Mid Register (CL-GD5426/'28/'29 only)

I/O Port Address: 3CF

Index: 2D

Bit	Description
7	BLT Source Start [15]
6	BLT Source Start [14]
5	BLT Source Start [13]
4	BLT Source Start [12]
3	BLT Source Start [11]
2	BLT Source Start [10]
1	BLT Source Start [9]
0	BLT Source Start [8]

This register contains the middle 8 bits of the 21-bit value specifying the byte address of the beginning source pixel for a BitBLT.

Bit	Description
7:0	**BLT Source Start [15:8]:** This field is the middle 8 bits of the BLT Source Start.

9.40 GR2E: BLT Source Start High Register (CL-GD5426/'28/'29 only)

I/O Port Address: 3CF

Index: 2E

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	BLT Source Start [20]
3	BLT Source Start [19]
2	BLT Source Start [18]
1	BLT Source Start [17]
0	BLT Source Start [16]

This register contains the high-order 5 bits of the 21-bit value specifying the byte address of the beginning source pixel for a BitBLT.

Bit	Description
7:5	**Reserved**
4:0	**BLT Source Start [20:16]:** This field is the high-order 5 bits of the BLT Source Start.

9.41 GR2F: BLT Write Mask Destination Register (CL-GD5429 only)

I/O Port Address: 3CF

Index: 2E

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Write Mask [2]
1	Write Mask [1]
0	Write Mask [0]

This register contains a write mask used for clipping on the left edge of color-expanded Bit-BLTS.

Bit	Description
7:3	**Reserved**
2:0	**BLT Source Start [20:16]:** If this field is written to any value other than '0', then n pixels will not be written on the left edge of each scanline for a color-expanded BLT.

9.42 GR30: BLT Mode Register (CL-GD5426/'28/'29 only)

I/O Port Address: 3CF

Index: 30

Bit	Description
7	Enable Color Expand
6	Enable 8 x 8 Pattern Copy
5	Reserved
4	Color Expand/Transparency Width
3	Enable Transparency Compare
2	BLT Source Display/System Memory
1	BLT Destination Display/System Memory
0	BLT Direction

This register contains the bits that specify the details, but not the ROP, of the BLT.

Bit	Description
7	**Enable Color Expand:** If this bit is programmed to a '1', the ROP source will be the expanded result from the bit-mapped source. The destination must be screen memory and the direction must be 'increment'. The Color registers at GR0, GR1, GR10, and GR11 are used for the bit-map color expand BLT operations. All Raster OPs are available. When the source data is expanded, the MSB of the first source byte will become the first pixel in the screen destination. For color-expanded BLTs (system or display memory source), each logical line must be filled out to an even byte with 'dummy' bits if it is not an even multiple of eight pixels (that is, the source bytes must be completely used). These extra bits will be ignored under the control of the BLT width setting. When the source of color-expand data is display memory, the source starting address must be on a 4-byte boundary, and the addressing will always be linear (the source pitch will be ignored). Refer to Appendix D7 for information regarding Color Expansion. If this bit is programmed to a '0', the ROP source will be the pixel data read from the source. For the CL-GD5429 only: The 8 byte monochrome pattern for a color expanded BLT must begin on an 8-byte boundary. The low-order three bits of the source start address will determine which byte of the pattern is used for the first scanline of the destination. That is, the low-order three bits of the source address function as a vertical offset for the pattern.

9.41 GR2F: BLT Write Mask Destination Register (CL-GD5429 only)

I/O Port Address: 3CF

Index: 2E

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Write Mask [2]
1	Write Mask [1]
0	Write Mask [0]

This register contains a write mask used for clipping on the left edge of color-expanded Bit-BLTS.

Bit	Description
7:3	**Reserved**
2:0	**BLT Source Start [20:16]:** If this field is written to any value other than '0', then n pixels will not be written on the left edge of each scanline for a color-expanded BLT.

9.42 GR30: BLT Mode Register (CL-GD5426/'28/'29 only)

I/O Port Address: 3CF

Index: 30

Bit	Description
7	Enable Color Expand
6	Enable 8 x 8 Pattern Copy
5	Reserved
4	Color Expand/Transparency Width
3	Enable Transparency Compare
2	BLT Source Display/System Memory
1	BLT Destination Display/System Memory
0	BLT Direction

This register contains the bits that specify the details, but not the ROP, of the BLT.

Bit	Description
7	**Enable Color Expand:** If this bit is programmed to a '1', the ROP source will be the expanded result from the bit-mapped source. The destination must be screen memory and the direction must be 'increment'. The Color registers at GR0, GR1, GR10, and GR11 are used for the bit-map color expand BLT operations. All Raster OPs are available. When the source data is expanded, the MSB of the first source byte will become the first pixel in the screen destination. For color-expanded BLTs (system or display memory source), each logical line must be filled out to an even byte with 'dummy' bits if it is not an even multiple of eight pixels (that is, the source bytes must be completely used). These extra bits will be ignored under the control of the BLT width setting. When the source of color-expand data is display memory, the source starting address must be on a 4-byte boundary, and the addressing will always be linear (the source pitch will be ignored). Refer to Appendix D7 for information regarding Color Expansion. If this bit is programmed to a '0', the ROP source will be the pixel data read from the source. For the CL-GD5429 only: The 8 byte monochrome pattern for a color expanded BLT must begin on an 8-byte boundary. The low-order three bits of the source start address will determine which byte of the pattern is used for the first scanline of the destination. That is, the low-order three bits of the source address function as a vertical offset for the pattern.

9.42 GR30: BLT Mode Register (CL-GD5426/'28/'29 only) *(cont.)*

Bit **Description**

6 **Enable 8 x 8 Pattern Copy:** If this bit is programmed to a '1', the source pattern will be copied repeatedly to the destination rectangular area. The pattern source must be aligned on a four-byte boundary, except for color expansion when the source must be aligned on an eight-byte boundary. The source will be linear addressed data in one of three arrangements as shown in the following table:

Operating Mode	Arrangement
Color Expansion Enabled	8 bytes of Monochrome bitmap for the 8 x 8 pattern
8-bit Pixels	64 bytes of color data for 64 pixels
16-bit Pixels	128 bytes of color data for 64 pixels

5 **Reserved**

4 **Color Expand/Transparency Width:** If this bit is programmed to a '1', and color expansion is enabled, the bit-mapped source will be expanded to 16 bits/pixel. If this bit is programmed to a '0', and color expansion is enabled, the bit-mapped source will be expanded to 8 bits/pixel.

If this bit is programmed to a '1' and GR30[3] is programmed to a '1', the transparency compare will be done on 16-bit pixels (CL-GD5426/'28 only). If this bit is programmed to a '0' and GR30[3] is programmed to a '1', the transparency compare will be done on 8-bit pixels.

3 **Enable Transparency Compare:** For the CL-GD5426/'28 only, if this bit is programmed to a '1', then the result of the ROP is compared to the Transparent Color register for each pixel. If the compare is a match, then the data are *not* written to the destination. The transparency feature must be used, and the transparent color set to the background color, if the color expand BLT is to be used with an opaque foreground and a transparent background (similar to Extended Write mode 4).

If this bit is programmed to a '0', the data are written to the destination without regard to the Transparent Color register.

For the CL-GD5429 only: This bit is used for Color Expand with Transparency. If this bit is programmed to a '1', then zeroes in the monochrome image being expanded will result in the corresponding pixel not being written. This is the equivalent of Extend Write mode 4. Only the foreground is written. If this bit is programmed to a '0', then zeroes in the monochrome image being expanded will result in the background color being written into the corresponding pixel.

9.42 GR30: BLT Mode Register (CL-GD5426/'28/'29 only) *(cont.)*

Bit	Description
2	**BLT Source Display/System Memory:** If this bit is programmed to a '1', the BLT source will be system memory rather than display memory. The CPU will perform the system bus transfers; the CL-GD5426/'28/'29 will ignore the address provided with such transfers. The CPU is required to transfer data in increments of four bytes. If the total number of bytes moved for a BLT is not a multiple of four, the CPU must write 'extra' bytes. System memory-to-system memory BLTs are not allowed. If this bit is programmed to a '0', the BLT source will be display memory. **NOTE:** When system-to-screen BitBLTs are being executed, 16- or 32-bit host transfers must be used. When system-to-screen BitBLTs involving color expansion are being executed, the BLT Source Start registers must be programmed to a '0'.
1	**BLT Destination Display/System Memory:** If this bit is programmed to a '1', the BLT destination will be system memory rather than Display Memory. The CPU will perform the system bus transfers; the CL-GD5426/'28/'29 will ignore the address provided with such transfers. The CPU is required to transfer data in increments of four bytes. If the total number of bytes moved for a BLT is not a multiple of four, the CPU must read 'extra' bytes. System memory-to-system memory BLTs are not allowed. If this bit is programmed to a '0', the BLT destination will be display memory. **NOTE:** When system-to-screen BitBLTs are being executed, 16- or 32-bit host transfers must be used.
0	**BLT Direction:** If this bit is programmed to a '1', the source and destination addresses will be decremented. The BLT will proceed from higher addresses to lower addresses. In this case, the starting address will be the highest addressed byte in each area. If this bit is programmed to a '0', the source and destination addresses will be incremented. The BLT will proceed from lower addresses to higher addresses.

9.43 GR31: BLT Start/Status Register (CL-GD5426/'28/'29 only)

I/O Port Address: 3CF

Index: 31

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	BLT Progress Status (Read-only)
2	BLT Reset
1	BLT Start/Suspend
0	BLT Status (Read-only)

This register contains the bit that actually begins a BLT, and a bit that indicates whether the BLT has completed.

Bit	Description
7:4	**Reserved**
3	**BLT Progress Status (Read-only):** This bit will be set to a '1' at the start of a BLT and will be reset to a '0' when the entire operation completes. If the BLT is *suspended* (refer to GR31[1]), this bit will remain a '1'. If the BLT is *reset* (refer to GR3[2]), this bit will be reset to a '0'.
2	**BLT Reset:** If this bit is programmed to a '1', the entire BLT engine will be immediately reset and any operation in progress will be terminated. The operation cannot be restarted.
1	**BLT Start/Suspend:** When this bit is programmed to a '1', the BLT will begin with the next available display memory cycle. This bit will be cleared to a '0' when the BLT is completed. If this bit is programmed to a '0', the BLT will be suspended at the end of the current scanline. GR31[0] must be monitored to determine when the BLT actually stops. If the BLT is suspended by programming this bit to a '0', then the BLT Height registers will reflect the line count for the last completed transfer. A suspended BLT may be resumed by merely programing this bit to a '1'.
0	**BLT Status (Read-only):** If this bit is a '1', the BLT is in progress. If this bit is a '0', then the BLT is complete.

9.44 GR32: BLT Raster Operation Register (ROP) (CL-GD5426/'28/'29 only)

I/O Port Address: 3CF

Index: 32

Bit	Description
7	f [7]
6	f [6]
5	f [5]
4	f [4]
3	f [3]
2	f [2]
1	f [1]
0	f [0]

This register selects a two-operand ROP.

Bit	Description
7:0	**f [7:0]:** This eight bit value selects a two-operand Raster Operation, as indicated in the table below. This table is ordered by Microsoft ROP.

Z RPN	Z	ROP (hex)	Microsoft® Name	Microsoft ROP
0	0	00	BLACKNESS	00000042
DPon	~P.~D	90	-	000500A9
DPna	~P.D	50	-	000A0329
Pn	~P	D0	-	000F0001
DSon	~S.~D	90	NOTSRCERASE	001100A6
DSna	~S.D	50	–	00220326
Sn	~S	D0	NOTSRCCOPY	00330008
SDna	S.~D	09	SRCERASE	00440328
PDna	P.~D	09	-	00500325
Dn	~D	0B	DSTINVERT	00550009
DPx	P~=D	59	PATINVERT	005A0049
DPan	~P+~D	DA	-	005F00E9
DSx	S~=D	59	SRCINVERT	00660046
DSan	~S+~D	DA	–	007700E6
DSa	S.D	05	SRCAND	008800C6

9.44 GR32: BLT Raster Operation Register (ROP) (CL-GD5426/'28/'29 only) *(cont.*

Bit **Description**

7:0 *(cont.)*

Z RPN	Z	ROP (hex)	Microsoft® Name	Microsoft ROP
DSxn	S=D	95	-	00990066
DPa	P.D	05		00A000C9
PDxn	P=D	95	-	00A50065
D	D	06	–	00AA0029
DPno	~P+D	D6	-	00AF0229
DSno	~S+D	D6	MERGEPAINT	00BB0226
S	S	0D	SRCCOPY	00CC0020
SDno	S+~D	AD	–	00DD0228
DSo	S+D	6D	SRCPAINT	00EE0086
P	P	0D	PATCOPY	00F00021
PDno	P+~D	AD	-	00F50225
DPo	P+D	6D	-	00FA0089
1	1	0E	WHITENESS	00FF0062

NOTE: In the first two columns, **D** denotes destination, **S** denotes source, and **P** denotes pattern.
The first column is reverse Polish notation. The operators are: **a** denotes and, **o** denotes or, **x** denotes exclusive or, and **n** denotes not. As an example, the second entry would be interpreted: Destination, (enter), Pattern, oR, nOT.
The second column is provided as a service for those who prefer to avoid RPN. The operators are: ~ denotes not, . denotes and, and + denotes or. As an example, the second entry would be interpreted: NOT pattern AND NOT destination. (Demorgan's theorem says these two interpretations are equivalent).

9.45 GR34: BLT Transparent Color Low Register (CL-GD5426/'28 only)

I/O Port Address: 3CF

Index: 34

Bit	Description
7	BLT Transparent Color [7]
6	BLT Transparent Color [6]
5	BLT Transparent Color [5]
4	BLT Transparent Color [4]
3	BLT Transparent Color [3]
2	BLT Transparent Color [2]
1	BLT Transparent Color [1]
0	BLT Transparent Color [0]

This register contains the low-order 8 bits of the 16-bit transparent color. If GR30[3] is programmed to a '1', this value will be compared with the ROP result. If it is equal, the ROP result is not written to the Destination.

Bit	Description
7:0	**BLT Transparent Color [7:0]:** This field is the low-order 8 bits of the BLT Transparent Color.

9.46 GR35: BLT Transparent Color High Register (CL-GD5426/'28 only)

I/O Port Address: 3CF

Index: 35

Bit	Description
7	BLT Transparent Color [15]
6	BLT Transparent Color [14]
5	BLT Transparent Color [13]
4	BLT Transparent Color [12]
3	BLT Transparent Color [11]
2	BLT Transparent Color [10]
1	BLT Transparent Color [9]
0	BLT Transparent Color [8]

This register contains the high-order 8 bits of the 16-bit transparent color. If GR30[3] is programmed to a '1', this value will be compared with the ROP result. If it is equal, the ROP result is not written to the Destination. For 8-bit color modes, GR35 must be set equal to GR34.

Bit	Description
7:0	**BLT Transparent Color [15:8]:** This field is the high-order 8 bits of the BLT Transparent Color.

9.47 GR38: BLT Transparent Color Mask Low Register (CL-GD5426/'28 only)

I/O Port Address: 3CF

Index: 38

Bit	Description
7	BLT Transparent Color Mask [7]
6	BLT Transparent Color Mask [6]
5	BLT Transparent Color Mask [5]
4	BLT Transparent Color Mask [4]
3	BLT Transparent Color Mask [3]
2	BLT Transparent Color Mask [2]
1	BLT Transparent Color Mask [1]
0	BLT Transparent Color Mask [0]

This register contains the low-order 8 bits of the 16-bit Transparent Color Mask. If GR30[3] is programmed to a '1', the transparent color will be compared with the ROP result under this mask. If it is equal, the ROP result is not written to the Destination.

Bit	Description
7:0	**BLT Transparent Color Mask [7:0]:** This field is the low-order 8 bits of the BLT Transparent Color Mask. A '1' in any bit location makes the corresponding compare a don't care.

9.48 GR39: BLT Transparent Color Mask High Register (CL-GD5426/'28 only)

I/O Port Address: 3CF

Index: 39

Bit	Description
7	BLT Transparent Color Mask [15]
6	BLT Transparent Color Mask [14]
5	BLT Transparent Color Mask [13]
4	BLT Transparent Color Mask [12]
3	BLT Transparent Color Mask [11]
2	BLT Transparent Color Mask [10]
1	BLT Transparent Color Mask [9]
0	BLT Transparent Color Mask [8]

This register contains the high-order 8 bits of the 16-bit Transparent Color Mask. If GR30[3] is programmed to a '1', the transparent color will be compared with the ROP result under this mask. If it is equal, the ROP result is not written to the Destination. For 8-bit color modes, GR39 must be equal to GR38.

Bit	Description
7:0	**BLT Transparent Color Mask [15:8]:** This field is the high-order 8 bits of the BLT Transparent Color Mask. A '1' in any bit location makes the corresponding compare a don't care.

9.49 CR19: Interlace End Register

I/O Port Address: 3?5

Index: 19

Bit	Description
7	Interlace End [7]
6	Interlace End [6]
5	Interlace End [5]
4	Interlace End [4]
3	Interlace End [3]
2	Interlace End [2]
1	Interlace End [1]
0	Interlace End [0]

This register is used to contain the ending horizontal character count for the Odd Field VSYNC.

Bit	Description
7:0	**Interlace End:** This value is the number of characters in the last scanline of the Odd Field in Interlaced timing. This can be adjusted to center the scanlines in the Odd Field half way between scanlines in the Even Field. This register is typically programmed to approximately half the Horizontal Total.

9.50 CR1A: Miscellaneous Control Register

I/O Port Address: 3?5

Index: 1A

Bit	Description
7	Vertical Blank End Overflow [9]
6	Vertical Blank End Overflow [8]
5	Horizontal Blank End Overflow [7]
4	Horizontal Blank End Overflow [6]
3	Overlay/DAC Mode Switching Control [1]
2	Overlay/DAC Mode Switching Control [0]
1	Enable Double Buffered Display Start Address
0	Enable Interlaced

This register contains timing overflow bits as well as some Miscellaneous Control bits.

Bit **Description**

7:6 **Vertical Blank End Overflow:** This two-bit field is used to extend the Vertical Blank End value to 10 bits. Refer to the description of CR0 for a table containing all the timing value bits. These bits are enabled only if CR1B[5] is programmed to a '1' or if CR1B[7] is programmed to a '1' for the CL-GD5424/'26/'28/'29 only.

5:4 **Horizontal Blank End Overflow:** This two-bit field is used to extend the Horizontal Blanking End value to 8 bits. Refer to the description of CR0 for a table containing all the timing value bits. These bits are enabled only if CR1B[5] is programmed to a '1' or if CR1B[7] is programmed to a '1' for the CL-GD5424/'26/'28/'29 only.

3:2 **Overlay/DAC Mode Switching Control [1:0]:** This field is used to select Overlay and DAC Mode Switching. The values are summarized in the following table. Refer to Appendix B14 for further information.

CR1A[3]	CR1A[2]	Mode	Note
0	0	Normal Operation	
0	1	Mode Switching and Overlay with EVIDEO* (or OVRW*)	OVRW* for CL-GD5429 only
1	0	Mode Switching and Overlay for OVRW* and Color Key	CL-GD5424/'26/'28/'29 only
1	1	Mode Switching and Overlay with Color Key only	

9.50 CR1A: Miscellaneous Control Register *(cont.)*

Bit	Description
1	**Enable Double Buffered Display Start Address:** If this bit is programmed to a '1', the Display Start Address will be updated on the VSYNC following a write to Start Address Low. This provides control of display frame switching without the need to explicitly monitor VSYNC.
0	**Enable Interlaced**: If this bit is programmed to a '1', interlaced timing is enabled. By interlaced timing, it means interlaced sync in Text mode, and interlaced sync and video data in graphics mode. In addition, IRQ requests are generated only at the end of odd fields; that is at the end of a frame. For interlaced sync and data in graphics mode, the CRTC Scan Double (CR9[7]) must be programmed to a '0'. Graphics modes 4 and 6 must always be non-interlaced.

9.51 CR1B: Extended Display Controls Register

I/O Port Address: 3?5

Index: 1B

Bit	Description
7	Enable Blank End Extensions (CL-GD5424/'26/'28/'29 only)
6	Enable Text Mode Fast-Page
5	Blanking Control
4	Offset Register Overflow 8
3	Extended Display Start Address Bit 18 (CL-GD5426/'28/'29 only)
2	Extended Display Start Address Bit 17
1	Enable Extended Address Wrap
0	Extended Display Start Address Bit 16

This register contains a number of miscellaneous bits that control extended display functions.

Bit	Description
7	**Enable Blank End Extensions (CL-GD5424/'26/'28/'29 only):** If this bit is programmed to a '0', the Vertical and Horizontal Blank End Extension bits in CR1A are disabled if CR1B[5] is also a '0'. If this bit is programmed to a '1', the Vertical and Horizontal Blank End Extension bits in CR1A are enabled, regardless of the programming of CR1B[5].
6	**Enable Text Mode Fast-Page**: If this bit is programmed to a '0', all font fetch cycles take place as random read cycles. This bit must be programmed to a '0' for standard VGA dual-font operation. If this bit is programmed to a '1', fast-page Mode cycles will be used to fetch font data. This allows for text modes with a VCLK greater than 30 MHz, as is required for 132-column modes.
5	**Blanking Control:** If this bit is programmed to a '0', the DAC blanking will be controlled by the blanking signal generated by the CRTC. In this case, the border can be used (Refer to AR11). If this bit is programmed to a '1', the DAC blanking will be controlled by Display Enable. The DAC will be blanked during the time when the border is normally displayed. In addition, the OVRW pin (pin 71) will be an output and will follow the blanking signal generated by the CRTC. This signal may be directed to the feature connector or may be used to control an external overlay circuit. Finally, programming this bit to a '1' enables the Vertical and Horizontal Blank End Extension bits in CR1A. Refer to Appendix B14.

9.51 CR1B: Extended Display Controls Register *(cont.)*

Bit	Description
4	**Offset Register Overflow 8:** This bit extends the CRTC Offset register (CR13) by one bit. Refer to the description of CR0 in Table 6–1 for a summary of CRTC Timing register.
3	**Extended Display Start Address Bit 18 (CL-GD5426/'28/'29 only):** This is bit 17 of the Display Start Address. Refer to the description of CR1 in Table 6–1 for a summary of CRTC Timing register.
2	**Extended Display Start Address Bit 17:** This is bit 17 of the Display Start Address. Refer to the description of CR1 in Table 6–1 for a summary of CRTC Timing register.
1	**Enable Extended Address Wrap:** If this bit is programmed to a '0', the display memory address wraps at 64K maps (256K total memory). This provides VGA compatibility. If this bit is programmed to a '1', the display memory address wraps at the total available memory size. In particular, this bit provides the following functions: If this bit is programmed to a '1', and Chain-4 addressing is selected (SR4[3]=1), then DRAM addresses A0 and A1 are supplied from addresses XMA[16] and XMA[17]. XMA[18:12] addresses are the sum of XA[16:12] and either Offset register 0 or 1. If this bit is programmed to a '1' and CRTC Double Word addressing is selected (CR14[6]=1), then DRAM addresses A0 and A1 are supplied from CRTC addresses CR[14] and CR[15]. This provides four displayable pages in Video mode 13h. Character Counter addresses CA[16] and CA[18] provide up to 256K bytes in each bit plane, or 1 Mbyte of packed-pixel memory. If this bit is programmed to a '0', the CRTC Character Address Counter is 16-bits-wide, providing VGA compatibility. If this bit is programmed to a '1', the Counter is 18-bits-wide (19-bits-wide in CL-GD5426/'28/'29 only).
0	**Extended Display Start Address Bit 16:** This is bit 16 of the Extended Display Start Address. Refer to the description of CR0 in Table 6–1 for a summary of CRTC Timing register.

9.52 CR1D:Overlay Mode Register (CL-GD5429 only)

I/O Port Address: 3?5

Index: 1D

Bit	Description
7	Reserved
6	Overlay Timing Signal Source
5	Reserved
4	Reserved
3	Reserved
2	DAC Mode Switching Control [1]
1	DAC Mode Switching Control [0]
0	Reserved

This register contains a number of bits that control extended overlay modes.

Bit **Description**

7 **Reserved**

6 **Overlay Timing Signal Source:** If this bit is programmed to a '0', the EVIDEO* input is used as the timing signal for Overlay modes 01 and 10. This is the default.

If this bit is programmed to a '1', the internally generated signal OVRW* is used as the timing signal for Overlay modes 01 and 10. This avoids the requirement to connect OVRW* to EVIDEO*.

5:3 **Reserved**

2:1 **DAC Mode Switching Control [1:0]:** This field controls DAC Mode Switching. This control only the DAC Mode Switching; the selection of pixel data is still done as programmed into CR1A[3:2].

CR1D[2:1]	DAC Mode Switching
00	Switch True selected Extended DAC mode
01	Switch False selected Extended DAC mode
1X	Extended DAC mode Disabled

0 **Reserved**

9.53 CR25: Part Status Register

I/O Port Address: 3?5

Index: 25

Bit	Description
7	PSR [7]
6	PSR [6]
5	PSR [5]
4	PSR [4]
3	PSR [3]
2	PSR [2]
1	PSR [1]
0	PSR [0]

This read-only register is used for factory testing and internal tracking only.

Bit	Description
7:0	**Part Status Value**

9.54 CR27: ID Register

I/O Port Address: 3?5

Index: 27

Bit	Description
7	Device ID [5]
6	Device ID [4]
5	Device ID [3]
4	Device ID [2]
3	Device ID [1]
2	Device ID [0]
1	Reserved
0	Reserved

This read-only register will return a value that uniquely identifies the chip.

Bit **Description**

7:2 **Device ID:** This six-bit field contains a unique value that identifies the device according to the following table:

Product	CR27[7:2]
CL-GD5420	100010
CL-GD5422	100011
CL-GD5424	100101
CL-GD5426	100100
CL-GD5428	100110
CL-GD5429	100111

1:0 **Reserved**

9.55 HDR: Hidden DAC Register (Except CL-GD5420)

I/O Port Address: 3C6

Index: –

Bit	Description	Reset State
7	Enable 5-5-5 Mode	0
6	Enable All Extended Modes	0
5	Clocking Mode	0
4	32K Color Control	0
3	Extended Mode Select [3] (CL-GD5428 only)	0
2	Extended Mode Select [2]	0
1	Extended Mode Select [1]	0
0	Extended Mode Select [0]	0

This register is used to enable extended color modes, including 15-bit/pixel, 16-bit/pixel, and 24-bit/pixel modes. This register is cleared to all zeroes at RESET, putting the CL-GD542X in VGA-compatibility mode.

This register is accessed by reading the Pixel Mask register at 03C6h four times in succession; the next write or read at 03C6h will access the Hidden DAC register. When the HIdden DAC register is written, the internal counter is reset and the four dummy reads must be executed again. For the CL-GD5422/'24/'26/'28/'29, a read from the Hidden DAC register resets the counter and the four dummy reads must be executed again. For the CL-GD5428 only, reads from 3C6 do not lock the Hidden DAC register.

Bit	Description
7	**Enable 5-5-5 Mode:** If this bit is programmed to a '0', the extended color modes are disabled and the palette DAC is VGA-compatible. If this bit is programmed to a '1', extended color modes are enabled, as chosen by bit 6 and bits 2:0 of this register.
6	**Enable ALL Extended Modes:** If this bit is programmed to a '0' and bit 7 is programmed to a '1', the palette DAC will be in 5-5-5 Sierra™ mode, regardless of the value programmed into bits 3:0. If this bit is programmed to a '1' and bit 7 is programmed to a '1', the palette DAC mode will be chosen by the value programmed into bits 3:0 of this register.
5	**Clocking Mode:** If this bit is programmed to a '0', Clocking mode 1 will be chosen. In Clocking mode 1, 16-bit/pixel modes will use both edges of DCLK to latch data. The rising edge of DCLK will latch the low byte and the falling edge of DCLK will latch the high byte. If this bit is programmed to a '1', Clocking mode 2 will be chosen. In Clocking mode 2, 16-bit/pixel modes will use only the rising edge of DCLK to latch data. The DCLK must be supplied at twice the pixel rate. The least-significant byte is latched on the first rising edge and the most-significant byte is latched on the second rising edge. **NOTE:** All modes other than 16-bit/pixel use only the rising DCLK edge regardless of this bit. This bit should be programmed to a '0' only for externally supplied DCLK and data.

9.55 HDR: Hidden DAC Register (Except CL-GD5420) *(cont.)*

Bit **Description**

5 *(cont.)* **Clocking Mode:** For the CL-GD5429 only: This bit controls the clocking of input data as follows. If this bit is programmed to a '0', both edges of DCLK will be used. The rising edge will latch the low byte and the falling edge will latch the high byte.

If this bit is programmed to a '1', the CL-GD5429 is configured for VESA VAFC 2X mode. Each rising edge will clock in one byte. Every two bytes is assembled into a single 16-bit pixel which is displayed twice (two clock periods).

4 **32K Color Control:** If this bit is programmed to a '0', 5-5-5 operation will take place normally. If this bit is programmed to a '1', Pixel Data bit 15 will be used to choose between palette operation and 5-5-5 color. This allows 5-5-5 data to overlay 256-color images on a pixel-by-pixel basis. If Pixel Data bit 15 is a '1', then bits 7:0 choose a palette entry and bits 14:8 are ignored. If Pixel Data bit 15 is a '0', then 5-5-5 operation is chosen.

3:0 **Extended Mode Select [3:0]:** If bits 7 and 6 are both programmed to ones, then this four-bit field selects the extended color mode according to the following table:

Bit 7	Bit 6	Bit 3	Bit 2	Bit 1	Bit 0	Function
0	x	x	x	x	x	VGA compatibility
1	0	x	x	x	x	5-5-5 Sierra™
1	1	0	0	0	0	5-5-5 Sierra™
1	1	0	0	0	1	5-6-5 XGA™
1	1	0	0	1	x	Reserved
1	1	0	1	0	0	Reserved
1	1	0	1	0	1	8-8-8 16-million color
1	1	0	1	1	x	DAC power-down CL-GD5428/'29 only
1	1	1	0	0	0	8-bit grayscale CL-GD5428/'29 only
1	1	1	0	0	1	3-3-2 8-bit RGB CL-GD5428/'29 only
1	1	1	0	1	x	Reserved
1	1	1	1	x	x	Reserved

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VGA BIOS

10. VGA BIOS

10.1 BIOS Overview

The CL-GD542X VGA BIOS is a high-performance firmware product optimized to take full advantage of the CL-GD542X True Color VGA controller. The CL-GD542X BIOS is based on proven BIOS technology, and is fully compatible with the IBM VGA BIOS interrupt 10h interface. The BIOS is designed to provide a well-defined interface between MS-DOS, application software, and special OEM utility programs. In addition, it provides an extended set of functions to support the CL-GD542X VGA controller.

10.1.1 Main BIOS Features

The CL-GD542X VGA BIOS supports the following key features:

- 100% IBM VGA-compatible BIOS
- Support for high-resolution, extended 256-colors, Direct-Color™ and True Color Video Modes
- High-performance operation
- Modular, proven design
- Adapter or system board implementation (C000/E000 segments)
- Can be integrated with system BIOS
- Supports switch-less configuration
- Can be customized without source code
- VESA-compatible modes and interface

10.1.2 Extended Video Mode Support

The CL-GD542X VGA BIOS provides full support for all extended high-resolution video modes via interrupt 10h function calls. In addition, the CL-GD542X VGA BIOS supports a variety of extended functions, such as VGA display configuration and extended VGA inquiry. For a detailed description of these functions, refer to the CL-GD542X VGA BIOS External Software Specification document (Appendix E1).

10.1.3 Direct-Color Operation

The CL-GD542X BIOS supports Direct-color and True Color Video Modes. The CL-GD542X simultaneously displays 32K or 64K colors at resolutions of up to 800 x 600 and 16M colors at up to 640 x 480. This 15/16/24-bits per pixel Video Mode is TARGA- and XGA-Mode-compatible.

10.1.4 High Performance

The BIOS is optimized to provide maximum performance in adapter or motherboard implementations. The 16-bit system bus and Display Memory Interface of the CL-GD542X and its internal FIFOs are fully used by the BIOS. In addition, time critical routines — such as TTY output and scroll — are designed to provide maximum throughput in both text and graphics modes.

10.1.5 System Integration

The CL-GD542X VGA BIOS can easily be integrated for an adapter or motherboard design. The BIOS — 32K bytes in size — is provided for both the C000 and E000 address segments. To save space on the system board, the CL-GD542X VGA BIOS can be incorporated into the system BIOS ROM at either C000 or E000 addresses.

The BIOS does not require DIP switches or external hardware to be properly configured. A well-defined interface to the CL-GD542X BIOS configuration is available for system BIOS or OEM setup routines.

10.1.6 Customization

The default CL-GD542X BIOS is designed to be implemented without modification in almost all environments. However, the CL-GD542X BIOS can also be easily customized for a specific system environment. Modifications can also be accomplished with the Cirrus Logic OEM System Integration (OEMSI) utility program; such modifications do not require the CL-GD542X VGA BIOS source code. Hundreds of BIOS parameters and features can be modified, including:

- Sign-on message
- Display type configuration
- Video Mode parameter tables
- Font tables

10.1.7 Compatibility

The CL-GD542X BIOS is 100-percent compatible with the IBM VGA BIOS and supports BIOS-level compatibility for adapter card or integrated VGA on the system board. In addition, the CL-GD542X BIOS complies fully with the video modes and specifications issued by the Video Electronics Standards Association (VESA).

10.2 CL-GD542X VGA BIOS Initialization and Power-Up Diagnostics

The CL-GD542X VGA BIOS is shipped in two formats — a segment-C000-based VGA BIOS configured for VGA adapter cards that will be plugged into PC systems, and segment-E000-based VGA BIOS configured for integrated VGA video subsystems on the motherboard. The following sequence of steps is performed by the VGA BIOS at power-up initialization:

For Segment-C000-Adapter-Based VGA BIOS:

1. Checks if VGA BIOS Vector Interrupt 10h is already initialized.
2. If so, calls the INT 10h Function to disable the existing VGA card to sleep.
3. Disables the VGA adapter by writing a value of 16h to I/O Port 46E8H.
4. Programs I/O Port 102h with data 01h to enable video subsystem.
5. Writes a value of 0eh to 46E8H to enable I/O and memory addressing.
6. Writes I/O Port 4AE8H to disable 8514/A.
7. Disables VGA video (by programming Sequencer Clocking Mode Register, [Bit 5] = 1).
8. Initializes Video Vectors INT 10h and INT 42h.

9. Enables extensions by writing GR0A (I/O Port 3CE, Index = 0aH) with data 0ECH.
10. Initializes CL-GD542X Extension Registers.
11. Checks for co-resident MDA video adapter; if MDA is present, initializes co-resident bits and sets up MDA adapter.
12. Checks for CGA; if present, initializes co-resident bits, sets VGA to monochrome, and enables CGA.
13. Tests Video Memory.
14. Initializes Text Mode 3.
15. Displays sign-on message.
16. If any POST error flags are set, prints error messages.

For Segment-E000-Motherboard-Based VGA BIOS (CL-GD5424 or higher):

1. Enables VGA Setup Mode by writing VGA Video Sleep Enable Register (VSE I/O Port 46E8H with value of 16H).
2. Programs POS 2 Register (I/O Port 102H with data 01H) to enable video subsystem.
3. Writes a value of 0H to 46E8H to disable existing VGA adapter I/O and memory addressing.
4. Enables motherboard VGA by programming VSE Register 3C3H with data value 1.
5. Writes I/O Port 4AE8H to disable 8514/A.
6. Disables VGA video (by programming Sequencer Clocking Mode Register, [Bit 5] = 1).
7. Initializes Video Vectors INT 10H and INT 42H.
8. Enables extensions by writing GR0A (I/O Port 3CE, Index = 0AH) with data 0ECH.
9. Initializes CL-GD542X Extension Registers.
10. Checks for co-resident MDA video adapter; if MDA is present, initializes co-resident bits and sets up MDA adapter.
11. Checks for CGA, if present, initializes co-resident bits, and sets VGA to monochrome and enables CGA.
12. Tests Video Memory.
13. Initializes Text Mode 3.
14. Displays sign-on message.
15. If any POST error flags are set, prints error messages.
16. Checks to see if a VGA adapter is also present in the system; if so, disables motherboard VGA controller.

10.3 Video BIOS Interrupt Vectors

The interrupt vectors that must be initialized by DOS (including the planar and video BIOSes) are listed in Table 10–4 later in this chapter. Of these, the vectors (at locations 0:0040, 0000:007C, 0000:0108, 0000:010C) corresponding to vectors 10, 1F, 42, 43 are handled by the video BIOS.

10H — Video Services (Vector Location = 0000:0040H)

The CL-GD542X BIOS functions are accessed using interrupt 10H. Application programs place a function code in AH, and, if required, in other registers calling parameters and then execute an INT 10H instruction. When the BIOS gains control, the appropriate code is executed to perform the function; parameter values may be left in processor registers to be returned to the calling program upon exit from the interrupt routine.

The functions supported by the CL-GD542X BIOS allow the calling program to set the current mode, manipulate the cursor, place characters and individual pixels on the display, scroll the screen, load character fonts and color palette values, and read the light pen position. These functions are described in following sections.

1DH — 6845 Initialization (Vector Location = 0000:0074H)

This vector points to the initialization routines that set up the 6845.

1FH — CGA Character Set (Vector Location = 0000:007CH)

This pointer is used for the table of the upper 128 characters in CGA Modes 4, 5, and 6. The INT 43H Vector is used for the lower 128 characters for these modes.

42H — Old Video Services Pointer (Vector Location = 0000:0108H)

This location used to be the INT 10H vector for planar BIOS video services. When the EGA/VGA is installed, BIOS routines reload this address with a pointer to the planar INT 10H video service routine entry point.

43H — Graphics Character Table (Vector Location = 0000:010CH)

BIOS routines use this vector to point to a table of bitmaps that are used when graphics characters are displayed. This table is used for the lower 128 characters in Video Modes 4, 5, and 6. This table is also used for 256 characters in all additional graphics modes (IBM standard as well as Cirrus Logic extensions).

The Interrupt 10H calls constitute the bulk of the services provided by the video BIOS and will be later described in detail. They are listed along with the function and subfunction that define the particular service required. Note that some INT 10H services were introduced with the VGA and are not available on the earlier EGA. The services have been divided up into functional groupings.

10.3.1 Interrupt 10H: BIOS Video Service Routines Contents

Function	Sub-Function	Description	Adapter
00H		Set Video Mode	EGA,VGA
01H		Set Cursor Type	EGA,VGA
02H		Set Cursor Position	EGA,VGA
03H		Get Cursor Position	EGA,VGA
04H		Get Light Pen Position	EGA,VGA
05H		Select Active Display Page	EGA,VGA
06H		Window Scroll-Up	EGA,VGA
07H		Window Scroll-Down	EGA,VGA
08H		Read Character/Attribute at Cursor Position	EGA,VGA
09H		Write Character/Attribute at Cursor Position	EGA,VGA
0AH		Write Character at Cursor Position	EGA,VGA
0BH	00H	Set Background/Border Color	EGA,VGA
	01H	Select the Palette Set	EGA,VGA
0CH		Write Dot (Pixel)	EGA,VGA
0DH		Read Dot (Pixel)	EGA,VGA
0EH		Write Teletype Character to Active Page	EGA,VGA
0FH		Get Video Mode	EGA,VGA
10H		Palette Manipulations	EGA,VGA
	00H	Set Individual Palette Register (Internal Palette Register)	
	01H	Set OverScan (Border) Register	
	02H	Set All Palette Registers and OverScan Register	
	03H	Intensity/Blinking	
	04H-06H	Reserved	
	07H	Read Individual Palette Register (Internal Palette Register)	
	08H	Read OverScan (Border) Register	
	09H	Read All Palette Registers and OverScan Register	
	0AH-0FH	Reserved	
	10H	Set Individual Color Register (RAMDAC/External Palette Register)	
	11H	Reserved	
	12H	Set Block of Color Registers	
	13H	Select Color Page (Not Valid in Mode 13H)	
	14H	Reserved	
	15H	Read Individual Color Register (RAMDAC/External Palette Register)	
	16H	Reserved	
	17H	Read Block of Color Registers	
	18H-19H	Reserved	

10.3.1 Interrupt 10H: BIOS Video Service Routines Contents *(cont.)*

Function	Sub-Function	Description	Adapter
	1AH	Read Current State of Color Page	
	1BH	Sum Color Values To Gray Shades	
11H		CHARACTER GENERATOR	EGA,VGA
	00H	Load User Text Font	
	01H	Load 8 x 14 ROM Text Font	
	02H	Load 8 x 8 ROM Text Font	
	03H	Select Block Specifier	
	04H	Load 8 x 16 ROM Text Font	VGA
	10H	Load User Text Font and Reprogram Controller	
	11H	Load 8 x 14 ROM Text Font and Reprogram Controller	
	12H	Load 8 x 8 ROM Text Font and Reprogram Controller	
	14H	Load 8 x 16 ROM Text Font and Reprogram Controller	VGA
	20H	Set Pointer of User's Graphics Font Table to Interrupt 1FH	
	21H	Set Pointer of User's Graphics Font Table to Interrupt 43H	
	22H	Set Pointer of 8 x 14 ROM Graphics Font Table to Interrupt 43H	
	23H	Set Pointer of 8 x 8 ROM Graphics Font Table to Interrupt 43H	
	24H	Set Pointer of 8 x 16 ROM Graphics Font Table to Interrupt 43H	VGA
	30H	Get Font Information	
12H		Alternate Select	EGA,VGA
	10H	Get Configuration Information	
	20H	Select Alternate PrintScreen Routine	
	30H	Select Scanlines (Alphanumeric Mode)	
	31H	Enable/Disable Default Palette Loading	
	32H	Enable/Disable Video	
	33H	Enable/Disable Grayscale Summing	
	34H	Enable/Disable Cursor Emulation	
	35H	Switch Active Display	
	36H	Enable/Disable Screen Refresh	
	13H	Write String in Teletype	EGA,VGA
	1AH	Get/Set Display Combination Code	VGA
1BH		Get Functionality/State Information	VGA
1CH		Save/Restore Video State	VGA
	1DH - FFH	Reserved	

10.4 Description Of Functions

10.4.1 Function: 00H • Set Video Mode

[Entry]

AH = 00H
AL = Video Mode (see below)

[Return]

NONE

[Note]

1. Video Mode Table for standard VGA:

Mode	Resolution	Type	Colors	Pages
00H/01H	40 x 25 (360 x 400)	Text	16	8
02H/03H	80 x 25 (640 x 400)	Text	16	8
04H/05H	320 x 200 (40 x 25)	Graphics	4	1
06H	640 x 200) (80 x 25)	Graphics	2	1
07H	80 x 25 (720 x 400)	Text	Monochrome	8
08H - 0CH	Reserved			
0DH	320 x 200 (40 x 25)	Graphics	16	8
0EH	640 x 200 (80 x 25)	Graphics	16	4
0FH	640 x 350 (80 x 25)	Graphics	Monochrome	2
10H	640 x 350 (80 x 25)	Graphics	16	2
11H	640 x 480 (80 x 25)	Graphics	2	1
12H	640 x 480 (80 x 25)	Graphics	16	1
13H	320 x 200 (40 x 25)	Graphics	256	1

2. If Bit 7 of AL is set, the display buffer will not be cleared. Otherwise, the display buffer will be cleared during mode setting (EGA, VGA only) (Clear Screen).
3. No hardware cursor in graphics modes.
4. Default Mode during POST: Mode 3H = Color Monitor, Mode 07H = Monochrome Monitor.
5. There is no difference between Modes 00H and 01H, 02H and 03H, or 05H and 06H on EGA/VGA. They are only different on CGA, which supports composite video displays.
6. The default settings of each Video Mode can be overridden by several subfunctions in Function 12H or by supply user's video service table whose address is stored in BIOS data area (0040:A8H).
7. See Application Note E1 for extended modes.

10.4.2 Function: 01H • Set Cursor Type

[Entry]

AH = 01H
CH = Start scanline of cursor (0 base)
CL = End scanline of cursor (0 base)

[Return]

NONE

[Notes]

1. This function is available in text modes only. The values of cursor type are stored at [40:60].
2. The definition of value in Register CH:

Bit	Definition
7-6	Reserved = 0
5	1 = No cursor display 0 = Normal blinking cursor
4-0	Start scanline (0 base)

3. The definition of value in Register CL:

Bit	Definition
7	Reserved = 0
6-5	Number of character skew
4-0	End scanline (0 base)

   * On EGA, the value in this register should be one greater than the real bottom of the cursor.

4. Default setting:

Font Size	Start	End
8 x 8	6	7
8 x 14	11	12
8 x 16	13	14

5. To allow cursor displaying as the values set in the function call, turn off cursor emulation. The Cursor Emulation Flag is located in Bit 0 of [40:87]. It can be turned on/off by Subfunction 34H of Function 12H call.

10.4.3 Function: 02H • Set Cursor Position

[Entry]

AH = 02H
BH = Display page (0 base)
DH = Row number of cursor location start (0 base)
DL = Column number of cursor location end (0 base)

[Return]

NONE

[Notes]

1. This function is available for both text and graphics modes.
2. If Register DL is specified over the width of screen displayable area, it will cause the cursor to wrap to the next row. If Register DH is specified over the height of screen displayable area, it causes the cursor to disappear.
3. Default setting for each mode: Cursor Location at 0000H.
4. BIOS maintains one cursor location for each page and supports up to eight pages. These values are recorded at [40:50], and occupy eight words (one word for each location).

10.4.4 Function: 03H • Get Cursor Position

[Entry]

AH = 03H
BH = Display page (0 base)

[Return]

CH = Start scanline of cursor (0 base)
CL = End scanline of cursor (0 base)
DH = Row number of cursor start location (0 base)
DL = Column number of cursor end location (0 base)

[Note]

1. Cursor type is same for all pages. The cursor location of each page is maintained separately.

10.4.5 Function: 04H • Get Light Pen Position*

[Entry]
AH = 04H

[Return]

AH = 00H	Light Pen inactive
or	
AH = 01H	Light Pen active and returns following values
BX = Pixel column	(X coordinate in graphics modes (0 base))
CX = Pixel row	(Y coordinate in graphics modes above Mode 06H (0 base))
CH = Pixel row	(Y coordinate in Graphics Modes 04H - 06H (0 base))
DH = Character row	(Y coordinate in text modes (0 base))
DL = Character column	(X coordinate in text modes (0 base))

[Notes]
1. The color of background and foreground will affect the sensitivity of light pen.
2. High-resolution device affects the accuracy of light pen.

* ***Not supported***

10.4.6 Function: 05H • Select Active Display Page

[Entry]
AH = 05H
AL = Display page (0 base)

[Return]
None

[Notes]
1. The contents of each page will not be altered by changing to other pages.
2. Please refer to mode table of Function 00H.

10.4.7 Function: 06H • Window Scroll Up

[Entry]

AH = 06H
AL = Number of rows to be scrolled up (0 = scroll up and clear entire window)
BH = Attribute to be used in inserting blank lines
CH = Y coordinate of top left corner of window (0 base)
CL = X coordinate of top left corner of window (0 base)
DH = Y coordinate of bottom right corner of window (0 base)
DL = X coordinate of bottom right corner of window (0 base)

[Return]

None

[Notes]

1. This function will clear the entire window when it encounters the number of rows of window equal to the value in Register AL or AL = 0.
2. The image, outside the window, will not be changed. The cursor will not be updated.
3. A new blank line with attribute value specified in BH is inserted from the bottom of window whenever an old line at the top of window is scrolled out of window.
4. This function is available for both text and graphics modes.

10.4.8 Function: 07H • Window Scroll Down

[Entry]

AH = 07H
AL = Number of rows to be scrolled down (0 = scroll down and clear entire window)
BH = Attribute to be used in inserting blank lines
CH = Y coordinate of top left corner of window (0 base)
CL = X coordinate of top left corner of window (0 base)
DH = Y coordinate of bottom right corner of window (0 base)
DL = X coordinate of bottom right corner of window (0 base)

[Return]

None

[Notes]

1. This function will clear entire window when it encounters the number of rows of window equal to the value in Register AL or AL = 0.
2. The image, outside the window, will not be changed. The cursor will not be updated.
3. A new blank line with attribute value specified in BH is inserted from the top of window whenever an old line at the bottom of window is scrolled out of window.
4. This function is available for both text and graphics modes.

10.4.9 Function: 08H • Read Character/Attribute at Cursor Position

[Entry]
AH = 08H
BH = Display page (0 base)

[Return]
AH = Attribute (Valid on text modes)
AL = ASCII character code

[Notes]
1. This function is able to read data from other valid inactive pages in multiple page modes at any time.
2. The cursor is not updated after reading a character from the screen, and has to be moved explicitly.
3. No control characters are recognized such as LF, CR, BACKSPACE, and BELL.
4. In Graphics Modes 04H - 06H of CGA adapter, the first half of character font (Code 00H - 7FH) is maintained in system ROM only. To support the second half of character font (Code 80H - FFH), the Interrupt Vector 1FH, at 0000:007CH, has to be initialized to point to the second half of character font.
5. Graphics modes return the Character Code only. Three characters, 00H/20H/FFH, cannot be distinguished, and the function always reads them back as Character Code 00H.
6. The character codes will be read back as Character Code 00H when they are written with a color that is same as the background color in graphics modes.

10.4.10 Function: 09H • Write Character/Attribute at Cursor Position

[Entry]
AH = 09H
AL = ASCII character code
BH = Display page (0 base)
or
BL = Attribute (text modes)
Display color (graphics modes)
CX = Repeat character count

[Return]
None

[Notes]
1. This function is able to write data to other valid inactive pages in multiple page modes at any time.
2. The cursor is not updated after writing a character to the screen, and has to be moved explicitly.
3. No control characters are recognized such as LF, CR, BACKSPACE, and BELL.
4. Graphics Modes 04H - 06H of CGA adapter, the first half of character font (Code 00H -

7FH) is maintained in system ROM only. To support the second half of character font (Code 80H - FFH), the Interrupt Vector 1FH, at 0000:007CH, has to be initialized to point to the second half of character font.

5. In graphics modes, the color (attribute) is treated as pixel color to generate an ASCII character pattern. And the color value will be masked according to the number of colors in the video modes.
6. The character codes will be displayed as blank when they are written with the color that is the same as the background color in graphics modes.
7. The characters written to the screen, specified in CX, should not extend to the next row in graphics modes. Otherwise, invalid results would be generated.
8. If Bit 7 of Register BL is set, the function will take the color value X'OR with the value in display memory. (Valid in all graphics modes except Mode 13H). This feature can be used in fast character/dot erasing.

10.4.11 Function: 0AH • Write Character at Cursor Position

[Entry]

AH = 0AH
AL = ASCII character code
BH = Display page (0 base)

or

BL = Foreground color (graphics modes only)
CX = Repeat character count

[Return]

None

[Notes]

1. This function is able to write data to other valid inactive pages in multiple page modes at any time.
2. The cursor is not updated after writing a character to screen and has to be moved explicitly.
3. No control characters are recognized such as LF, CR, BACKSPACE, and BELL.
4. Graphics Modes 04H - 06H of CGA adapter, the first half of character font (Code 00H - 7FH) is maintained in system ROM only. To support the second half of character font (Code 80H - FFH), the Interrupt Vector 1FH, at 0000:007CH, has to be initialized to point to the second font.
5. In graphics modes, the color (attribute) is treated as pixel color to generate ASCII character pattern. And the color value will be masked according to the number of colors in the video modes.
6. The character codes will be displayed as blank when they are written with the color same as background color in graphics modes.
7. The characters written to screen, specified in CX, should not extend to next row in graphics modes. Otherwise, invalid results would be generated.
8. If Bit 7 of Register BL is set, the function will take the color value X'OR with the value in display memory (valid in all graphics modes except Mode 13H). This feature can be used in fast character/dot erasing.

10.4.12 Function: 0BH

Function: 0BH • Subfunction: 00H — Set Background/Border Color

[Entry]

AH = 0BH
BH = 00H
BL = Color Value (0 - 31: Low-Intensity Colors = 0 - 15, High-Intensity Colors = 16 - 31)
– Border Color for text modes (Modes 00H - 03H)
– Color for 640 x 200 Graphics Mode (Mode 06H)

[Return]

None

[Note]

1. There are several functions in Function 10H that allow extensive display colors control for both text and graphics modes.

Function: 0BH • Subfunction: 01H — Select Palette Set

[Entry]

AH = 0BH
BH = 01H (Valid on Modes 04H and 05H 320 x 200 only)
BL = 0 - palette set: Background, Green, Red, Brown
1 – palette set: Background, Cyan, Magenta, White

[Return]

None

[Note]

1. For the CGA adapter, the palette set is defined as follows:

Mode	BL	Palette Set
04H	00H	Background, Green, Red, Yellow
	01H	Background, Cyan, Violet, White
05H	00/01H	Background, Cyan, Red, White

10.4.13 Function: 0CH • Write Dot (Pixel)

[Entry]
AH = 0CH
AL = Color value for pixel (Bit 7 is X'OR flag)
BH = Display page (0 base)
CX = X coordinate, column number (0 base)
DX = Y coordinate, row number (0 base)

[Return]
None

[Notes]
1. For coordinates' range, please refer to the resolution field of mode table in Function 00H.
2. Bit 7 of Register AL set will cause the requesting color value X'OR with memory color value.

10.4.14 Function: 0DH • Read Dot (Pixel)

[Entry]
AH = 0DH
BH = Display page (0 base)
CX = X coordinate, column number (0 base)
DX = Y coordinate, row number (0 base)

[Return]
AL = Dot (Pixel) color

[Note]
1. For coordinates' range, please refer to the resolution field of mode table in Function 00H.

10.4.15 Function: 0EH • Write Character to Active RAM in Teletype Mode

[Entry]
AH = 0EH
AL = ASCII character
BL = Foreground color in graphics modes

[Return]
None

[Notes]
1. Control characters such as LF, CR, Backspace, and BELL are recognized. (ASCII Codes: LF = 0AH, CR = 0DH, Backspace = 08H, BELL = 07H).
2. Line wrapping and screen scrolling are supported.
3. Cursor is moved to next position after writing a character to screen.

4. PC BIOS Version 10/19/81 or earlier; the Register BH has to be set to a 0.
5. The color value in Register BL will do X'OR with the content of display memory if Bit 7 of the register is set in graphics modes.
6. In text modes, the attribute of a character written to a new line is taken from the attribute of the last character in previous line. In such a case, control the attribute for a character, use Function 09H with blank character/attribute first before the function issued.

10.4.16 Function: 0FH • Get Video State

[Entry]
AH = 0FH

[Return]
AH = Number of displayable columns (1 base)
AL = Current video mode
BH = Current active page (0 base)

10.4.17 Function: 10H

Function 10H • Subfunction: 00H — Set Individual Palette Register (Internal Palette Register)

[Entry]
AH = 10H
AL = 00H (Subfunction)
BH = Color value
BL = Palette Register (0 - 0FH)

[Return]
None

[Notes]
1. Color value in the Internal Palette Register serves as a pointer that points to one of external registers (RAMDAC).
2. The color would not be changed by this function on Mode 13H.

Function: 10H • Subfunction: 01H — Set Overscan (Border) Register

[Entry]

AH = 10H
AL = 01H (Subfunction)
BH = Color value (00H - FFH)

[Return]

None

[Note]

1. Border color is driven by one of 256 external registers.

Function: 10H • Subfunction: 02H — Set All Palette Registers and OverScan Register

[Entry]

AH = 10H
AL = 02H (Subfunction)
ES: DX = Point to a 17-byte buffer

[Return]

None

[Notes]

1. The first 16 bytes in the buffer are used to store the values for 16 Internal Palette Registers. The last byte is the value for Overscan Register.
2. The display color would not be affected except Overscan Register on Mode 13H.

Function: 10H • Subfunction: 03H — Toggle Intensify/Blinking Bit

[Entry]

AH = 10H
AL = 03H (Subfunction)
BL = 00H - Intensify
01H - Blinking

[Return]

None

[Notes]

1. Bit 7 of Attribute Byte is interpreted according to the setting state by this function, which can provide 16 background colors (in intensify state) of 16-color text modes.
2. This function also supports Monochrome Modes (07H, 0FH).

Function: 10H • Subfunction: 4-6H — Reserved

Function: 10H • Subfunction: 07H — Read Individual Palette Register (Internal Palette Register)

[Entry]

AH = 10H
AL = 07H (Subfunction)
BL = Palette Register (0 - 0FH)

[Return]

BH = Color value

[Note]

1. Color Value in Internal Palette Register is served as a pointer that points to one of external registers (RAMDAC).

Function: 10H • Subfunction: 08H — Read Overscan (Border) Register

[Entry]

AH = 10H
AL = 08H (Subfunction)

[Return]

BH = Color value

[Note]

1. Border color is from 00H to FFH.

Function: 10H • Subfunction: 09H — Read All Palette Registers and OverScan Register

[Entry]

AH = 10H
AL = 09H (Subfunction)
ES: DX = Point to a 17-byte buffer
(The first 16 bytes for returning values from 16 palette registers respectively and the last byte for Overscan Register).

[Return]

ES: DX = Point to the same buffer provided from the entry of function call.

Function: 10H • Subfunction: 0A-0FH — Reserved

Function: 10H • Subfunction: 10H — Set Individual Color Register (RAMDAC/External Palette Registers)

[Entry]

AH = 10H
AL = 10H (Subfunction)
BX = Color Register (00H - FFH)
DH = Red color
CH = Green color
CL = Blue color

[Return]

None

[Notes]

1. Currently, each color is only 6-bit significant. Three colors, RGB, are worked as a group and are formed into a 18-bit datum stored in the Color Register.
2. The maximum displayable colors are 256 out of 256K colors (two exponential 18).
3. In standard VGA, Mode 13H uses all 256 Color Registers to display colors.
4. BIOS will load default values into Color Registers whenever Function 00H (set Video Mode) is called. This is true only when the disable flag of default palette loading is not set (refer to Subfunction 31H of Function 12H).
5. With gray-summing flag set, BIOS will weight three color values and sum-to-grayshade value; and then it will use the value for all three colors.

Function: 10H • Subfunction: 11H — Reserved

Function: 10H • Subfunction: 12H — Set Block of Color Registers

[Entry]

AH = 10H
AL = 12H (Subfunction)
BX = Start Color Register (00H - FFH)
CX = Number of color registers to set
ES: DX = Point to table of color values (each table entry is in RGB format)

[Return]

None

[Notes]

1. Currently, each color is only 6-bit significant. Three colors, RGB, are worked as a group and are formed into a 18-bit datum stored in the Color Register.
2. The maximum displayable colors are 256 out of 256K colors (2 exponential 18).
3. In standard VGA, Mode 13H uses all 256 Color Registers to display colors.

4. BIOS will load default values into Color Registers whenever Function 00H (set Video Mode) is called. This is true only when the disable flag of default palette loading is not set (refer to Subfunction 31H of Function 12H).
5. With gray-summing flag set, BIOS will weight three color elements (RGB) of Color Register; and sum them to grayshade value, which is based on the formula (30% Red + 59% Green + 11% Blue). The grayshade value will be written back to three elements (RGB) of Color Register.

Function: 10H • Subfunction: 13H — Select Color Page (Not valid on Mode 13H)

[Entry]

AH = 10H
AL = 13H (Subfunction)
BL = 00H (select paging mode)
01H (select color page)
When BL = 00H -
BH = 00H (select 4 pages of 64-color Register page)
01H (select 16 pages of 16-color Register page)
When BL = 01H -
BH = Color page number (0 base)

[Return]

None

[Notes]

1. All video modes except 256-color modes are supported by the function.
2. This function treats 256-color Registers as sets of 16- or 64-color Registers. It can be used to display different colors quickly by switching among color sets (pages).
3. Default setting is Page 0 of 64-color Page Mode after Video Mode set. Normally, Function 00H (set Video Mode) will load the default colors of the first 64-color Registers (Page 00H) for all standard VGA modes except Mode 13H (248 registers loading).

Function: 10H • Subfunction: 14H — Reserved

Function: 10H • Subfunction: 15H — Read Individual Color Register (RAMDAC/External Palette Registers)

[Entry]

AH = 10H
AL = 15H (Subfunction)
BX = Color Register (00H - FFH)

[Return]

DH = Red color
CH = Green color
CL = Blue color

[Notes]

1. Currently, each color is only 6-bit significant. Three colors, RGB, are worked as a group and they are formed into a 18-bit datum stored in the Color Register.
2. The maximum displayable colors are 256 out of 256K colors (2 exponential 18).
3. In standard VGA, Mode 13H uses all 256-color Registers to display colors.
4. With gray-summing flag set, the only value returned from all three color elements of Color Register is the grayshade value.

Function: 10H • Subfunction: 16H — Reserved

Function: 10H • Subfunction: 17H — Read Block of Color Registers

[Entry]

AH = 10H
AL = 17H (Subfunction)
BX = Start Color Register (00H - FFH)
CX = Number of Color Registers to read
ES: DX = Point to user provided buffer for returned color values

[Return]

ES: DX = Point to same buffer from function call entry (buffer is treated as a color table and each entry of the table consists of three bytes in RGB format).

[Notes]

1. Currently, each color is a 6-bit value. All three colors form a 18-bit datum.
2. The maximum displayable colors are 256 out of 256K colors (two exponential 18).
3. In standard VGA, Mode 13H uses all 256-color Registers to display colors.
4. BIOS will load default values into Color Registers whenever Function 00H (set Video Mode) is called. This is true only when the disable flag of default palette loading is not set (please refer to Subfunction 31H of Function 12H).
5. With gray-summing flag set, the only value returned for all three colors is grayshade value.

Function: 10H • Subfunction: 18-19H — Reserved

Function: 10H • Subfunction: 1AH — Read Current State of Color Page (Not valid on Mode 13H)

[Entry]

AH = 10H
AL = 1AH (Subfunction)

[Return]

BH = Current page (Value depends on Paging Mode, 00H is default)
BL = Current Paging Mode
(00H = 4 pages of 64-Color Registers (default), 01H = 16 pages of 16-color Registers)

[Notes]

1. All video modes except 256-color modes are supported by the function.
2. This function treats 256-color Registers as sets of 16- or 64-color Registers. It can be used to display different colors quickly by switching among color sets (pages).
3. Default setting is page 00H of 6-color page mode after Video Mode set.

Function: 10H • Subfunction: 1BH — Sum Color Values to Grayshades

[Entry]

AH = 10H
AL = 1BH (Subfunction)
BX = Start Color Register (00H - FFH)
CX = Number of Color Registers to sum

[Return]

None

[Note]

1. This function will sum the Color Registers desired into grayshade values regardless the gray-summing flag.

10.4.18 Function: 11H

Function: 11H • Subfunction: 00H — Load User Text Font

[Entry]

AH = 11H
AL = 00H (Subfunction)
BH = Number of bytes per character
BL = Block to load (00H - 07H)
CX = Number of characters to store
DX = ASCII character ID of the first character in the font table (ES: BP)
ES: BP = Point to user-provided font table

[Return]

None

[Notes]

1. This function is only available for text modes. The value in Register BH represents the height of each character. It can be specified a maximum of 32 bytes per character in standard VGA specification.

2. In VGA, the character font is loaded into RAM Map 2 (0 base), which can contain up to eight fonts at any time, and is available for the Character Generator only. Consequently, the block value specified in Register BL is ranged from 00H (Default) to 07H.
3. Two character fonts out of eight can be used at any time. This provides 512 simultaneously displayable characters instead of 256 characters. The way to display two different fonts at one time can be accomplished by the following:
   a) Load fonts into desired blocks.
   b) Subfunction 03H (Select Block Specifier) of Function 11H is called to select two different font blocks out of eight font blocks; one for primary font, the other for secondary font.
   c) The Bit 3 of Attribute Byte is served as the Font Block Selector and foreground intensity for the character.
      Bit 3 = 0 — Primary font selected and normal display (eight foreground colors)
      if Subfunction 00H of Function 10H is called with BX = 0712H.
      Bit 3 = 1 — Secondary font selected and normal display (eight foreground colors)
      else
      Bit 3 = 1 — Secondary font selected and intensity display (16 foreground colors).
4. Default setting by BIOS loads a font into Block 0, which is used for both primary font and secondary font (256 displayable characters).
5. The font loading by Subfunction 00H requires caution since the controller is not reprogrammed; abnormal character display may occur. For example:
   If a font table is loaded to override the font in a block, a double image may result (especially when the loaded font size is smaller than the one previously displayed).

Function: 11H • Subfunction: 01H — Load 8 x 14 ROM Font

[Entry]

AH = 11H
AL = 01H (Subfunction)
BL = Block to load (00H - 07H)

[Return]

None

[Notes]

1. This function is only available for text modes.
2. The height of character is 14 bytes, but the height of display cell is same as default setting.
3. In VGA, the character font is loaded into RAM Map 2 (0 base), which can contain up to eight fonts at any time, and is available for the Character Generator only. Consequently, the block value specified in Register BL is ranged from 00H (Default) to 07H.
4. Two character fonts out of eight can be used at any time. This provides 512 simultaneously displayable characters instead of 256 characters. The way to display two different fonts at one time can be accomplished by the following:
   a) Load fonts into desired blocks.
   b) Subfunction 03H (Select Block Specifier) of Function 11H is called to select two different font blocks out of eight font blocks; one for primary font, the other for secondary font.

c) The Bit 3 of Attribute Byte is served as the Font Block Selector and foreground intensity for the character.

Bit 3 = 0 — Primary font selected and normal display (eight foreground colors).

if Subfunction 00H of Function 10H is called with BX = 0712H

Bit 3 = 1 — Secondary font selected and normal display (eight foreground colors)

else

Bit 3 = 1 — Secondary font selected and intensity display (16 foreground colors).

5. Default setting by BIOS loads a font into Block 0, which is used for both primary font and secondary font (256 displayable character).
6. The font loading by Subfunction 00H requires caution since the controller is not reprogrammed; abnormal character display may occur. For example:

   If a font table is loaded to override the font in a block, a double image may result (especially when the loaded font size is smaller than the one previously displayed).

Function: 11H • Subfunction: 02H — Load 8 x 8 ROM Font

[Entry]

AH = 11H
AL = 08H (Subfunction)
BL = Block to load (00H - 07H)

[Return]

None

[Notes]

1. This function is only available for text modes.
2. The height of character is eight bytes, but the height of display cell is same as default setting.
3. In VGA, the character font is loaded into RAM Map 2 (0 base), which can contain up to eight fonts at any time, and is available only for the Character Generator. Consequently, the block value specified in Register BL is ranged from 00H (Default) to 07H.
4. Two character fonts out of eight can be used at any time. This provides 512 simultaneously displayable characters instead of 256 characters. The way to display two different fonts at one time can be accomplished by the following:
   a) Load fonts into desired blocks.
   b) Subfunction 03H (Select Block Specifier) of Function 11H is called to select two different font blocks out of eight font blocks; one for primary font, the other for secondary font.
   c) The Bit 3 of Attribute Byte is served as the Font Block Selector and foreground intensity for the character.

      Bit 3 = 0 — Primary font selected and normal display (eight foreground colors).

      if Subfunction 00H of Function 10H is called with BX = 0712H

      Bit 3 = 1 — Secondary font selected and normal display (eight foreground colors)

      else

      Bit 3 = 1 — Secondary font selected and intensity display (16 foreground colors).
5. Default setting by BIOS loads a font into Block 0, which is used for both primary font and secondary font (256 displayable characters).

6. The font loading by Subfunction 00H requires caution since the controller is not reprogrammed; abnormal character display may occur. For example:

   If a font table is loaded to override the font in a block, a double image may result (especially when the loaded font size is smaller than the one previously displayed).

Function: 11H • Subfunction: 03H — Select Block Specifier

[Entry]

AH = 11H
AL = 03H (Subfunction)
BL = Selection of character generator blocks

[Return]

None

[Notes]

1. The definition of the value in Register BL as follows:

Bits	Font Blocks
4, 1, 0	Primary Font Block (00H - 07H)
5, 3, 2	Secondary Font Block (00H - 07H)

2. For EGA-compatible operation, Bits 0-1 is used for primary font, and Bits 2-3 for secondary font.
3. To retain eight consistent colors during 512-character display, the Subfunction 00H of Function 10H has to be called first with the following setting:

   AX = 1000H, BX = 0712H

Function: 11H • Subfunction: 04H — Load 8 x 16 ROM Font

[Entry]

AH = 11H
AL = 04H (Subfunction)
BL = Block to load (00H - 07H)

[Return]

None

[Notes]

1. This function is only available for text modes.
2. The height of character is 16 bytes, but the height of the display cell is the same as default setting.
3. In VGA, the character font is loaded into RAM Map 2 (0 base), which can contain up to eight fonts, and is available for the Character Generator only. Consequently, the block value specified in Register BL is ranged from 00H (Default) to 07H.
4. Two character fonts out of eight can be used at any time (512 simultaneously displayable characters, not 256 characters). The way to display two different fonts at one time can be accomplished by the following:

a) Load fonts into desired blocks.
b) Subfunction 03H (Select Block Specifier) of Function 11H is called to select two different font blocks out of eight font blocks; one for primary font, the other for secondary font.
c) The Bit 3 of Attribute Byte is served as the Font Block Selector and foreground intensity for the character.
   Bit 3 = 0 — Primary font selected and normal display (eight foreground colors).
   if Subfunction 00H of Function 10H is called with BX = 0712H
   Bit 3 = 1 — Secondary font selected and normal display (eight foreground colors)
   else
   Bit 3 = 1 — Secondary font selected and intensity display (16 foreground colors).

5. Default setting by BIOS loads a font into Block 0, which is used for both primary font and secondary font (256 displayable characters).
6. The font loading by Subfunction 00H requires caution since the controller is not reprogrammed; abnormal character display may occur. For example:
   If a font table is loaded to override the font in a block, a double image may result (especially when the loaded font size is smaller than the one previously displayed).

Function: 11H • Subfunction: 10H — Load User Text Font and Reprogram Controller

[Entry]
AH = 11H
AL = 10H (Subfunction)
BH = Number of bytes per character
BL = Block to load (00H - 07H)
CX = Number of characters to store
DX = ASCII character ID of the first character in the font table (ES: BP)
ES: BP = Point to user-provided font table

[Return]
None

[Notes]
1. This function is only available for text modes.
2. The value in Register BH represents the height of each character. It can be specified a maximum of 32 bytes per character in standard VGA specification.
3. In VGA, the character font is loaded into RAM Map 2 (0 base), which can contain up to eight fonts at any time, and is available for the Character Generator only. Consequently, the block value specified in Register BL is ranged from 00H (Default) to 07H.
4. Two character fonts out of eight can be at any time. This means 512 simultaneously displayable characters instead of 256 characters. The way to display two different fonts at one time can be accomplished by the following:
   a) Load fonts into desired blocks.
   b) Subfunction 03H (Select Block Specifier) of Function 11H is called to select two different font blocks out of eight font blocks; one for primary font, the other for secondary font.

c) The Bit 3 of Attribute Byte is served as the Font Block Selector and foreground intensity for the character.
Bit 3 = 0 — Primary font selected and normal display (eight foreground colors).
if Subfunction 00H of Function 10H is called with BX = 0712H
Bit 3 = 1 — Secondary font selected and normal display (eight foreground colors)
else
Bit 3 = 1 — Secondary font selected and intensity display (16 foreground colors).

5. Default setting by BIOS loads a font into Block 0, which is used for both primary font and secondary font (256 displayable characters).
6. Subfunction 10H is almost identical to Subfunction 00H except the following differences:
   a) Page 00H has to be active.
   b) Character Height (Bytes per character) will be recalculated.
   c) Number of rows (0 base) are recalculated as:
   (scanlines per screen/Character Height) minus 1.
   d) The length of display buffer will be recalculated as (Total number of rows x Total number of columns) x 2 (1 base).
   e) The CRTC Registers are reprogrammed as follows:

Index	Register Name	Change
09H	Maximum scanlines	Character Height minus 1
0AH	Cursor Start	Character Height minus 2
0BH	Cursor End	Character Height minus 1
12H	Vertical Display Enable End For 350 or 400 scanline Modes (Rows per screen x Character Height) minus 1 For 200 scanline Modes (Rows per screen x Character Height) x 2) minus 1	
14H	Underline Location	Character Height minus 1 (Mode 07H only)

   f) It has to be called immediately after Function 00H call (set Video Mode). Otherwise, the result will be unpredictable.

Function: 11H • Subfunction: 11H — Load 8 x 14 ROM Font and Reprogram Controller

[Entry]
AH = 11H
AL = 11H (Subfunction)
BL = Block to load (00H - 08H)

[Return]
None

[Notes]
1. This function is only available for text modes.

2. The character and display cells are both 14 bytes high (scanlines).
3. In VGA, the character font is loaded into RAM Map 2 (0 base), which can contain up to eight fonts at any time and is available for the Character Generator only. Consequently, the block value specified in Register BL is ranged from 00H (Default) to 07H.
4. Two character fonts out of eight can be used at any time. This means 512 simultaneously displayable characters instead of 256 characters. The way to display two different fonts at one time can be accomplished by the following:
   a) Load fonts into desired blocks.
   b) Subfunction 03H (Select Block Specifier) of Function 11H is called to select two different font blocks out of eight font blocks; one for primary font, the other for secondary font.
   c) The Bit 3 of Attribute Byte is served as the Font Block Selector and foreground intensity for the character.

      Bit 3 = 0 — Primary font selected and normal display (eight foreground colors).

      if Subfunction 00H of Function 10H is called with BX = 0712H

      Bit 3 = 1 — Secondary font selected and normal display (eight foreground colors)

      else

      Bit 3 = 1 — Secondary font selected and intensity display (16 foreground colors).
5. Default setting by BIOS loads a font into Block 0, which is used for both primary font and secondary font (256 displayable characters).
6. Subfunction 11H is almost identical to Subfunction 01H except the following differences:
   a) Page 00H has to be active.
   b) Character Height = 14.
   c) Number of rows (0 base) are recalculated as:
      (Scanlines per screen/Character Height) minus 1.
   d) The length of display buffer will be recalculated as:
      (Total number of rows x Total number of columns) x 2 (1 base)
   e) The CRTC Registers are reprogrammed as follows:

Index	**Register Name**	**Change**
09H	Maximum Scanlines	13 (0DH)
0AH	Cursor Start	12 (0CH)
0BH	Cursor End	13 (0DH)
12H	Vertical Display Enable End	(Rows per screen x 14) minus 1
14H	Underline Location (Mode 07H only)	13 (0DH)

   f) It has to be called immediately after Function 00H call (set Video Mode). Otherwise, the result will be unpredictable.

Function: 11H • Subfunction: 12H — Load 8 x 8 ROM Font and Reprogram Controller

[Entry]

AH = 11H
AL = 12H (Subfunction)
BL = Block to load (00H - 07H)

[Return]

None

[Notes]

1. This function is only available for text modes.
2. The height of character and display cell are all eight bytes (scanlines).
3. In VGA, the character font is loaded into RAM Map 2 (0 base), which can contain up to eight fonts at any time and is available for the Character Generator only. Consequently, the block value specified in Register BL is ranged from 00H (Default) to 07H.
4. Two character fonts out of eight can be used at any time. This means 512 simultaneously displayable characters instead of 256 characters. The way to display two different fonts at one time can be accomplished by the following:
   a) Load fonts into desired blocks.
   b) Subfunction 03H (Select Block Specifier) of Function 11H is called to select two different font blocks out of eight font blocks; one for primary font, the other for secondary font.
   c) The Bit 3 of Attribute Byte is served as the Font Block Selector and foreground intensity for the character.
      Bit 3 = 0 — Primary font selected and normal display (eight foreground colors).
      if Subfunction 00H of Function 10H is called with BX = 0712H
      Bit 3 = 1 — Secondary font selected and normal display (eight foreground colors)
      else
      Bit 3 = 1 — Secondary font selected and intensity display (16 foreground colors).
5. Default setting by BIOS loads a font into Block 0, which is used for both primary font and secondary font (256 displayable characters).
6. Subfunction 12H is almost identical to Subfunction 02H except the following differences:
   a) Page 00H has to be active.
   b) Character Height = 8.
   c) Number of rows (0 base) are recalculated as
      (Scanlines per screen/Character Height) minus 1.
   d) The length of display buffer will be recalculated as:
      (Total number of rows x Total number of columns) x 2 (1 base).
   e) The CRTC Registers are reprogrammed as follows:

Index	Register Name	Change
09H	Maximum Scanlines	7 (07H)
0AH	Cursor Start	6 (06H)
0BH	Cursor End	7 (07H)
12H	Vertical Display Enable End	(Rows per screen x 8) minus 1
14H	Underline Location (Mode 07H only)	7 (07H)

   f) It has to be called immediately after Function 00H call (set Video Mode). Otherwise, the result will be unpredictable.

Function: 11H • Subfunction: 14H — Load 8 x 16 ROM Font and Reprogram Controller

[Entry]

AH = 11H
AL = 14H (Subfunction)
BL = Block to load (00H - 07H)

[Return]

None

[Notes]

1. This function is only available for text modes.
2. The height of character and display cell are all 16 bytes (scanlines).
3. In VGA, the character font is loaded into RAM Map 2 (0 base), which can contain up to eight fonts at any time and is available for the Character Generator only. Consequently, the block value specified in Register BL is ranged from 00H (Default) to 07H.
4. Two character fonts out of eight can be used at any time. This means 512 simultaneously displayable characters instead of 256 characters. The way to display two different fonts at one time can be accomplished by the following:
   a) Load fonts into desired blocks.
   b) Subfunction 03H (Select Block Specifier) of Function 11H is called to select two different font blocks out of eight font blocks; one for primary font, the other for secondary font.
   c) The Bit 3 of Attribute Byte is served as the Font Block Selector and foreground intensity for the character. Bit 3 = 0 – Primary font selected and normal display (eight foreground colors). If Subfunction 00H of Function 10H is called with BX = 0712H
      Bit 3 = 1 — Secondary font selected and normal display (eight foreground colors)
      else
      Bit 3 = 1 — Secondary font selected and intensity display (16 foreground colors).
5. Default setting by BIOS loads a font into Block 0, which is used for both primary font and secondary font (256 displayable characters).
6. Subfunction 14H is almost identical to Subfunction 04H except the following differences:
   a) Page 00H has to be active.
   b) Character Height = 16.
   c) Number of Rows (0 base) are recalculated as:
      (Scanlines per screen/Character Height) minus 1.
   d) The length of display buffer will be recalculated as (Total number of rows x Total number of columns) x 2 (1 base).
   e) The CRTC Registers are reprogrammed as follows:

Index	Register Name	Change
09H	Maximum Scanlines	15 (0FH)
0AH	Cursor Start	14 (0EH)
0BH	Cursor End	15 (0FH)
12H	Vertical Display Enable End	(Rows per screen x16) minus 1
14H	Underline Location	15 (0FH) (Mode 07H only)

   f) It has to be called immediately after Function 00H call (set Video Mode). Otherwise, the result will be unpredictable.

Function: 11H • Subfunction: 20H — Set Pointer of User's Graphics Font Table to Interrupt 1FH

[Entry]

AH = 11H
AL = 20H (Subfunction)
ES: BP = Point to user's graphics font table

[Return]

None

[Notes]

1. The value in this Interrupt Vector serves as a pointer that points to Graphics Font for character codes (80H - FFH) in Modes 04H, 05H, and 06H.
2. In CGA adapter, the planar BIOS only provides 128 character codes (00H - 7FH). The user can supply the other half of character codes (80H - FFH), or use GRAFTABL in DOS to load this half.
3. This function has to be called immediately after setting Video Mode.

Function: 11H • Subfunction: 21H — Set Pointer of User's Graphics Font Table to Interrupt 43H

[Entry]

AH = 11H
AL = 21H (Subfunction)
BL = Character rows specifier
    00H = Value in Register DL (the number of displayable rows specified by user)
    01H = 14 (0EH) character rows
    02H = 25 (19H) character rows
    03H = 43 (2BH) character rows
CX = Bytes per character
DL = Number of character rows (if Register BL = 00H)
ES: BP = Point to user's graphics font table

[Return]

None

[Note]

1. The value in this Interrupt Vector serves as a pointer that points to Graphics Font for character codes (00H - 7FH) in Modes 04H, 05H, and 06H. The vector also handles Graphics Font for character codes (00H - FFH) in all other graphics modes.
2. This function should only be called immediately after setting Video Mode.
3. The portion of character rows above displayable rows will not be displayed unless it is scrolled up.
4. The overlapping screen may occur on video modes that use all display memory addresses such as Mode 13H.

Function: 11H • Subfunction: 22H — Set Pointer of ROM 8 x14 Graphics Font Table to Interrupt 43H

[Entry]

AH = 11H
AL = 22H (Subfunction)
BL = The specifier of character rows on screen
- 00H = Value in Register DL (the number of displayable rows specified by user)
- 01H = 14 (0EH) character rows
- 02H = 25 (19H) character rows
- 03H = 43 (2BH) character rows

DL = Number of character rows to display (if Register BL = 00H)

[Return]

None

[Notes]

1. The value in this Interrupt Vector serves as a pointer that points to Graphics Font for character codes (00H - 7FH) in Modes 04H, 05H, and 06H. The vector also handles Graphics Font for character codes (00H - FFH) in all other graphics modes.
2. This function should only be called immediately after setting Video Mode.
3. The portion of character rows above displayable rows will not be displayed unless it is scrolled up.
4. The overlapping screen may occur on video modes that use all display memory addresses such as Mode 13H.

Function: 11H • Subfunction: 23H — Set Pointer of ROM 8 x 8 Graphics Font Table to Interrupt 43H

[Entry]

AH = 11H
AL = 23H (Subfunction)
BL = Specifier of character rows on screen
- 00H = Value in Register DL (the number of displayable rows specified by user)
- 01H = 14 (0EH) character rows
- 02H = 25 (19H) character rows
- 03H = 43 (2BH) character rows

DL = Number of character rows to display (if Register BL = 00H)

[Return]

None

[Notes]

1. The value in this Interrupt Vector serves as a pointer that points to Graphics Font for character codes (00H - 7FH) in Modes 04H, 05H, and 06H. The vector also handles Graphics Font for character codes (00H - FFH) in all other graphics modes.
2. This function should only be called immediately after setting Video Mode.

3. The portion of character rows above displayable rows will not be displayed unless it is scrolled up.
4. The overlapping screen may occur on video modes that use all display memory addresses such as Mode 13H.

Function: 11H • Subfunction: 24H — Set Pointer of ROM 8 x 16 Graphics Font Table to Interrupt 43H

[Entry]

AH = 11H
AL = 24H (Subfunction)
BL = Specifier of character rows on screen
    00H = Value in Register DL (the number of displayable rows specified by user)
    01H = 14 (0EH) character rows
    02H = 25 (19H) character rows
    03H = 43 (2BH) character rows
DL = Number of character rows to display (if Register BL = 00H)

[Return]

None

[Notes]

1. The value in this Interrupt Vector serves as a pointer that points to Graphics Font for character codes (00H - 7FH) in Modes 04H, 05H, and 06H. The vector also handles Graphics Font for character codes (00H - FFH) in all other graphics modes.
2. This function should only be called immediately after setting Video Mode.
3. The portion of character rows above displayable rows will not be displayed unless it is scrolled up.
4. The overlapping screen may occur on video modes that use all display memory addresses such as Mode 13H.

Function: 11H • Subfunction: 30H — Get Pointer Information of Fonts

[Entry]

AH = 11H
AL = 30H (Subfunction)
BH = Pointer information of fonts
- 00H - Current Font Pointer stored in Interrupt Vector 1FH
- 01H - Current Font Pointer stored in Interrupt Vector 43H
- 02H - Font Pointer of ROM 8 x 14 Font Table
- 03H - Font Pointer of ROM 8 x 8 Font Table (Character Codes 00H - 7FH)
- 04H - Font Pointer of ROM 8 x 8 Font Table (Character Codes 80H - FFH)
- 05H - Font Pointer of ROM 9 x 14 Alternate Font Table
- 06H - Font Pointer of ROM 8 x 16 Font Table
- 07H - Font Pointer of ROM 9 x 16 Alternate Font Table

[Return]

CX = Current character height (Bytes per Character)
DL = Number of rows of current video mode (0 base)
ES: BP = Pointer information of desired font

10.4.19 Function: 12H

Function: 12H • Subfunction: 10H — Get Current Video Configuration

[Entry]

AH = 12H
BL = 10H (Subfunction)

[Return]

BH = 00H - Color Mode (3Dx)
01H - Monochrome Mode (3Bx)
BL = Video Memory Size
00H = 64K bytes
01H = 128K bytes
02H = 192K bytes
03H = 256K bytes

CH = Feature Bits	Feature Control Output Bit Setting	Input Status Register 0 - (3C2H)
0	0	Bit 5
1	0	Bit 6
2	1	Bit 5
3	1	Bit 6
4 - 7	Reserved	

CL = Switch Settings	Description
Bit 0	Configuration Switch-1
Bit 1	Configuration Switch-2
Bit 2	Configuration Switch-3
Bit 3	Configuration Switch-4
Bit 4 - Bit 7	Reserved

Function: 12H • Subfunction: 20H — Alternate PrintScreen Handler

[Entry]

AH = 12H
BL = 20H (Subfunction)

[Return]

None

[Note]

1. This function call will replace original PrintScreen Interrupt Handler (Interrupt 05H) to support the modes whose displayable rows on screen are over 25 rows.

Function: 12H • Subfunction: 30H — Select Scanlines for Text Modes

[Entry]

AH = 12H
BL = 30H (Subfunction)
AL = Specifier of scanlines
00H = 200 scanlines
01H = 350 scanlines
02H = 400 scanlines

[Return]

AL = 12H (function supported)

[Notes]

1. The selected scanlines will take effect on next mode setting.
2. Mode 07H is only supported 350/400 scanlines. Modes 00H - 03H are supported by three scanlines.
3. The modes, 200 scanlines, are double scanned.

Function: 12H • Subfunction: 31H — Enable/Disable Default Palette Loading

[Entry]

AH = 12H
BL = 31H (Subfunction)
AL = 00H - Enable default palette loading
01H - Disable default palette loading

[Return]

AL = 12H (function supported)

[Notes]

1. This function will take effect on next mode setting.
2. All Internal/External Palette Registers will be affected.

Function: 12H • Subfunction: 32H — Enable/Disable Video

[Entry]
AH = 12H
BL = 32H (Subfunction)
AL = 00H - Enable Video
01H - Disable Video

[Return]
AL = 12H (function supported)

[Note]
1. Video subsystem will not respond to any I/O or Video Memory Addressing.

Function: 12H • Subfunction: 33H — Enable/Disable Summing-to-Grayshades

[Entry]
AH = 12H
BL = 33H (Subfunction)
AL = 00H - Enable summing-to-grayshades
01H - Disable summing-to-grayshades

[Return]
AL = 12H (function supported)

[Note]
1. This function will take effect on a subsequent mode setting or internal/external palettes setting.

Function: 12H • Subfunction: 34H — Enable/Disable Cursor Emulation

[Entry]
AH = 12H
BL = 34H (Subfunction)
AL = 00H - Enable cursor emulation
01H - Disable cursor emulation

[Return]
AL = 12H (function supported)

[Notes]
1. This function will take effect on a subsequent mode setting or Function 01H call (set cursor type).
2. Bit 0 of Address [40:87] Emulation Flag is affected.

Function: 12H • Subfunction: 35H — Switch Video Display

[Entry]

AH = 12H
BL = 35H (Subfunction)
AL = 00H - Initial video adapter turned off
(ES:DX must point to a 128-byte buffer for switching state save area)
01H - System board video turned on
02H - Active video turned off (ES:DX must point to a buffer for switching state save area)
03H - Inactive video turned on (ES:DX must point to a buffer which saves switching state previously)
ES:DX = Buffer for switching state (valid when AL = 00H, 02H, or 03H)

[Return]

AL = 12H (function supported)

[Notes]

1. There are several requirements have to be met before using this function. Requirements:
   a) Two video subsystems coexisting: system board video and video adapter.
   b) The usage of video resources has conflicted between two video systems.
   c) Video adapter is primary video, system board is secondary video.
   d) This function has to be supported by system board video and video adapter.

2. If the first time switching from video adapter to system board video:
   Call the function with Register AL = 00H
   Call the function with Register AL = 01H
   else
   Call the function with Register AL = 02H
   Call the function with Register AL = 03H

Function: 12H • Subfunction: 36H — Enable/Disable Screen Display

[Entry]

AH = 12H
BL = 36H (Subfunction)
AL = 00H - Enable screen display
01H - Disable screen display

[Return]

AL = 12H (function supported)

[Note]

1. This function can be used for fast video memory updating without losing synchronization.

10.4.20 Function: 13H • Write Teletype String

[Entry]

AH = 13H

AL = Write function specifier

- 00H - Write character string without updating cursor (BL = Attribute)
- 01H - Write character string with updating cursor (BL = Attribute)
- 02H - Write character/attribute string without updating cursor
- 03H - Write character/attribute string with updating cursor

BH = Display page (0 base)

BL = Attribute (valid when AL = 00H or 01H)

CX = String length

DH = Start Y coordinate of string displayed on screen

DL = Start X coordinate of string displayed on screen

ES: BP = Start address of string (in Segment: Offset Format)

[Return]

None

[Notes]

1. Control Characters: LF, CR, Backspace, and BELL are recognized. (ASCII Codes: LF = 0AH, CR = 0DH, Backspace = 08H, BELL = 07H).
2. String can be written to any pages regardless of active state.
3. Line wrapping and screen scrolling are supported. Screen scrolling is only supported on active page.
4. The color value in Register BL will do X'OR with the content of display memory, if Bit 7 of the register is set in graphics modes.

10.4.21 Function: 1AH

Function: 1AH • Subfunction: 00H — Get Display Combination Code (DCC)

[Entry]

AH = 1AH
AL = 00H (Subfunction)

[Return]

If function supported:
AL = 1AH
BH = Alternate display code
BL = Active display code

[Notes]

1. The index of current DCC entry in DCC table is stored in address [40:8A].
2. Display Combination Code Definition:

Code	Definition
00H	No Display
01H	Monochrome Display Adapter (MDA)
02H	Color Display Adapter (CGA)
03H	Reserved
04H	EGA with Color Monitor (EGA)
05H	EGA with Monochrome Monitor (MEGA)
06H	Professional Graphics Adapter with Color Display (PGA)
07H	Video Graphics Array with Analog Monochrome Monitor (MVGA)
08H	Video Graphics Array with Analog Color Monitor (VGA)

Function: 1AH • Subfunction: 01H — Set Display Combination Code (DCC)

[Entry]

AH = 1AH
AL = 01H (Subfunction)
BH = Alternate display code
BL = Active display code

[Return]

If function supported:
AL = 1AH

[Note]

1. Display Combination Code Definition:

Code	Definition
00H	No Display
01H	Monochrome Display Adapter (MDA)
02H	Color Display Adapter (CGA)
03H	Reserved
04H	EGA with Color Monitor (EGA)
05H	EGA with Monochrome Monitor (MEGA)
06H	Professional Graphics Adapter with Color Display (PGA)
07H	Video Graphics Array with Analog Monochrome Monitor (MVGA)
08H	Video Graphics Array with Analog Color Monitor (VGA)

2. User is responsible for providing correct DCC. There is no physical checking device.

10.4.22 Function: 1BH

Function: 1BH • Collection of Video Information

[Entry]

AH = 1BH
BX = 00H
ES: DI = Pointer points to 128-byte buffer

[Return]

If function supported
AL = 1BH

[Notes]

1. Video information in 128-byte buffer:

Offset	Size	Definition
00H	2 Words	Pointer points to collection of static functionality information
04H	Byte	Current Video Mode
05H	Word	Number of columns (1 base)
07H	Word	Refresh Buffer Length (unit: byte)
09H	Word	The starting address of Refresh Buffer (Offset value relates to start of video memory; default = 0000H)
0BH	8 Words	Cursor Position for each page (maximum eight pages supported)
1BH	Word	Current Cursor Type (High Byte = start scanline, Low Byte = end scanline)
1DH	Byte	Active Video Page
1EH	Word	Base Port Address of CRT Controller (CRTC) (Monochrome = 3BxH, Color = 3DxH)
20H	Byte	Current setting of 3B8H or 3D8H (Mode Control Register)
21H	Byte	Current setting of 3B9H or 3D9H
22H	Byte	Number of rows (1 base)
23H	Word	Character height (1 base; unit: scanline)
25H	Byte	Active Display Code
26H	Byte	Alternate Display Code
27H	Word	Number of displayable colors (1 base; monochrome = 0000H)
29H	Byte	Number of Pages (1 base)
2AH	Byte	Specifier of vertical resolution 00H = 200 scanlines 01H = 350 scanlines 02H = 400 scanlines 03H = 480 scanlines 04H - FFH = Reserved
2BH	Byte	Primary Font Block (00H - 07H)
2CH	Byte	Secondary Font Block (00H - 07H)
2DH	Byte	Flags of Video State: **Bit** **Definition** 7-6 Reserved 0 = Background intensity 1 = Blinking (Default) 4 0 = Cursor Emulation Disable 1 = Cursor Emulation Enable 3 0 = Default Palette Loading Enable 1 = Default Palette Loading Disable 2 0 = Color Monitor Attached 1 = Monochrome Monitor Attached 1 0 = Summing-to-grayshades Disable 1 = Summing-to-grayshades Enable 0 1 = All Modes are active on all displays
2E - 30H	Reserved	
31H	Byte	Specifier of total video RAM 00H = 64K bytes

		01H = 128K bytes 02H = 192K bytes 03H = 256K bytes 04H - FFH = Reserved
32H	Byte	Save pointer state information: Bit Definition 7-6 Reserved 5 1 = Extension of Display Combination Code Active 4 1 = Palette Override Active 3 1 = Graphics Font Override Active 2 1 = Alpha Font Override Active 1 1 = Dynamic Save Area Active 0 1 = 512-character Set Active
33 - 3FH	Reserved	

2. Collection of static functionality information:

Offset	**Size**	**Definition**
00H	Byte	Available video modes if bit set: **Bit Video Mode** 0 00H 1 01H 2 02H 3 03H 4 04H 5 05H 6 06H 7 07H
01H	Byte	Available video modes if bit set: **Bit Video Mode** 0 08H 1 09H 2 0AH 3 0BH 4 0CH 5 0DH 6 0EH 7 0FH
00H	Byte	Available video modes if bit set: **Bit Video Mode** 0 10H 1 11H 2 12H 3 13H 4 - 7 Reserved
03 - 06H	Reserved	
07H	Byte	Number of scanlines available in text modes: (Subfunction 30H, Function 12H)

		Bit	**Scanlines (if Bit = 1)**
		0	200
		1	350
		2	400
		3 - 7	Reserved
08H	Byte	Number of active character blocks available in text modes	
09H	Byte	Maximum number of character blocks available in text modes	
0AH	Byte	Supported functions (No. 1):	
		Bit	**Function (if Bit = 1)**
		0	All Modes on All Displays
		1	Summing to grayshades
		2	Character fonts Loading
		3	Default Palette Loading
		4	Cursor Emulation
		5	EGA Palettes (Internal Palettes)
		6	Color Palettes (External Palettes/RAMDAC)
		7	Color Paging
0BH	Byte	Supported functions (No. 2):	
		Bit	**Function (if Bit = 1)**
		0	Reserved
		1	Save/Restore Video State
		2	Background Intensity/Blinking Control
		3	Set Display Combination Code
		4 - 7	Reserved
0C - 0DH	Reserved		
0EH	Save Pointer Functions:		
		Bit	**Function (if Bit = 1)**
		0	512-character Set
		1	Dynamic Save Area
		2	Alpha Font Override
		3	Graphics Font Override
		4	Palette Override
		5	Extension of Display Combination Code
		6 - 7	Reserved
0FH	Reserved		

10.4.23 Function: 1CH

Function: 1CH • Subfunction: 00H — Get Buffer Size for Video State

[Entry]

AH = 1AH
AL = 00H (Subfunction)
CX = Requested Video State:

Bit	Video State
0	Hardware State
1	BIOS Data Area
2	Color Registers (External Palettes/RAMDAC)
3 - 15	Reserved

[Return]

If function supported
AL = 1CH
BX = Blocks/Buffer (Unit: 64 Byte/Block)

[Note]

1. This function will report the sufficient size of buffer to save video state. To guarantee Subfunction 01H and 02H performed successfully, this subfunction should be called first.

Function: 1CH • Subfunction: 01H — Saving Video State

[Entry]

AH = 1AH
AL = 01H (Subfunction)
CX = Requested Video States:

Bit	Video States
0	Hardware State
1	BIOS Data Area
2	Color Registers (External Palettes/RAMDAC)
3 - 15	Reserved

ES: BX = Pointer points to buffer (Segment: Offset format)

[Return]

If function supported:
AL = 1CH
ES: BX = State information saved in user-supplied buffer

Function: 1CH • Subfunction: 02H — Restore Video State

[Entry]

AH = 1AH

AL = 02H (Subfunction)

CX = Requested Video States:

Bit	Video States
0	Hardware State
1	BIOS Data Area
2	Color Registers (External Palettes/RAMDAC)
3 - 15	Reserved

ES: BX = Pointer points to previous saved buffer (Segment: Offset format)

[Return]

If function supported:

AL = 1CH

10.5 VGA Sleep Mode And Display Switching

The IBM VGA standard supports a Sleep Mode feature to enable/disable CPU addressing of the VGA subsystem video memory and I/O ports. For integrated VGA subsystems on the motherboard, the video subsystem is enabled or disabled by programming a Video Subsystem Enable Register at I/O Port 3C3H. On VGA adapter cards, a control register at I/O Port 46E8H is used. These two separate schemes of enabling/disabling addressing allows two VGAs (driving separate display monitors) to coexist in a system and have the capability to switch active video from one display to another. The IBM standard VGA BIOS supports a set of function calls to select Sleep Mode and display switching features.

The CL-GD542X VGA controller, depending on the application, can be programmed to respond at either 3C3H or 46E8H I/O Port for enabling/disabling CPU addressing. This allows for full IBM VGA compatibility, whether the design is an integrated motherboard VGA or an adapter card solution.

See Section 10.2 for the power-on initialization sequence.

10.6 Address Maps

The tables on the following pages provide background information regarding the usage of system memory, port address space, and interrupt vectors by DOS and its I/O routines (Planar and Peripheral BIOSes). The areas of interest to video subsystem users and designers are highlighted in bold text.

Table 10–1. MS DOS Memory Map After Loading

FE0000 - FFFFFF	128K bytes to 'shadow' system ROM BIOS
100000 - FDFFFF	15 Mbytes of extended memory in protected mode only
FFFF:000F (I Mbyte)	**Planar BIOS**
F000:0000	**Expansion BIOS (motherboard video BIOS)**
E000:0000	Voice Communication BIOS/LIM EMS page map area
D000:8000	Network BIOS/LIM EMS page map area
D000:0000	LIM EMS page map area
C000:C000	Hard disk BIOS
C000:8000	**EGA/VGA adapter BIOS**
C000:0000	EGA display RAM
B000:C000	CGA display RAM (or HGC mode graphics RAM)
B000:8000	HGC display RAM
B000:4000	MDA/HGC display RAM
B000:0000	**EGA/VGA display RAM**
A000:0000	**Top of system RAM** COMMAND.COM (transient portion), free RAM, COMMAND.COM (resident portion), installable device drivers, file control blocks, disk buffers, DOS tables, DOS kernel (MSDOS.SYS), resident DOS device drivers (IO.SYS)
0000:0600	ROM BIOS data area
0000:0400	Interrupt vectors
0000:0000	

Table 10–2. BIOS Data Area Assignments

0040:0000 WORD		COM1 Port base address
0040:0002 WORD		COM2 Port base address
0040:0004 WORD		COM3 Port base address
0040:0006 WORD		COM4 Port base address
0040:0008 WORD		Printer 1 port base address
0040:000A WORD		Printer 2 port base address
0040:000C WORD		Printer 3 port base address
0040:000E WORD		Printer 4 port base address
0040:0010 WORD	**EQUIPMENT_FLAG**	

Bit	**Definition**
D15, D14	No. or printer adapters
D13,D12	reserved
D11,D10,D9	No. of RS232-C
D8	reserved
D7,D6	No. of diskette drives
D5,D4	Identify the current primary display device:

D5	**D4**	**Adapter**
0	0	EGA (or none)
0	1	CGA 40 x 25
1	0	CGA 80 x 25
1	1	MDA

D3,D2	reserved	
D1	math coprocessor	
D0	IPL diskette	
0040:0012 BYTE		reserved
0040:0013 WORD	USABLE_RAM	Usable memory size in kilobytes
0040:0015 BYTE		reserved
0040:0016 BYTE		reserved
0040:0017 WORD	KBD_CNTRL	stores status of special keys
0040:0019 BYTE	ALT_KBD	alternate keypad entry
0040:001A WORD	KBD_BUF_HD	Points to head of keyboard buffer
0040:001C WORD	KBD_BUF_TL	Points to tail of keyboard buffer
0040:001E 16 WDS	KBD_BUFFER	Circular keyboard buffer
0040:003E BYTE		Diskette drive re-calibrate status
0040:003F BYTE		Diskette drive motor status
0040:0040 BYTE		Diskette drive motor off counter
0040:0041 BYTE		Last diskette driver operation status
0040:0042 7 BYTES		Diskette driver controller status
0040:0049 BYTE	**VIDEO_MODE**	**Current BIOS Video Mode**
0040:004A WORD	**COLUMNS**	**Number of text columns**
0040:004C WORD	**PAGE_LENGTH**	**Length of each page in bytes**
0040:004E WORD	**START_ADDR**	**Start Address Register value for page**
0040:0050 8 WDS	**CURSOR_POS**	**Cursor positions for all eight pages The high byte of each word contains the character row, the low byte the column**

0040:0060 WORD	**CURSOR_TYPE**	**Start and ending lines for text cursor. High byte has start line.**
0040:0062 BYTE	**ACTIVE_PAGE**	**Currently displayed page number**
0040:0063 WORD	**ADDR_CRTC**	**I/O Port address of 6845/CRTC address register (3B4 monochrome; 3D4 color)**
0040:0065 BYTE	**CRT_MODE_SET**	**Current value for Mode Control register (3B8 MDA; 3D8 CGA). The EGA and VGA values emulate the MDA/CGA values**
0040:0066 BYTE	**CRT_PALETTE**	**Current value for the CGA color select register (3D9); emulated by EGA/VGA**
0040:0067 DWORD		pointer to MCA PS/2 reset code
0040:006B BYTE		reserved
0040:006C DWORD		Timer counter
0040:0070 BYTE		Timer overflow
0040:0071 BYTE		Break key state
0040:0072 WORD		RESET flag
0040:0074 BYTE		Last hard disk drive operation status
0040:0075 BYTE		No. of hard disk drives attached
0040:0076 BYTE		PC XT hard disk drive control
0040:0077 BYTE		PC XT hard disk drive controller port
0040:0078 BYTE		Printer 1 Time-out value
0040:0079 BYTE		Printer 2 Time-out value
0040:007A BYTE		Printer 3 Time-out value
0040:007B BYTE		Printer 4 Time-out value
0040:007C BYTE		COM1 Time-out value
0040:007D BYTE		COM2 Time-out value
0040:007E BYTE		COM3 Time-out value
0040:007F BYTE		COM4 Time-out value
0040:0080 WORD		Keyboard Buffer Start Offset pointer
0040:0082 WORD		Keyboard Buffer End Offset pointer
0040:0084 BYTE	**ROWS**	**Number of text rows minus 1**
0040:0085 WORD	**CHAR_HEIGHT**	**Bytes per character**
0040:0087 BYTE	**INFO_1**	

Bit	Description
D7	equals Bit D7 from AL register on most recent mode select. (A one indicates display memory was not cleared by mode select).
D6, D5	Display memory size (00=64K, 01=128K, 10=192K, 11=256K)
D4	reserved
D3	A zero indicates EGA is the primary display
D2	A one will force the BIOS to wait for Vertical Retrace before memory write.
D1	A one indicates that EGA is in Monochrome Mode.
D0	A zero means that CGA cursor emulation is enabled. The cursor shape will be modified if enhanced text is used.

0040:0088 BYTE **INFO_3**

D4-D7 Feature Control Bits (from Feature Control Register)

	D0-D3	EGA Configuration Switch settings
0040:0089 BYTE	**FLAGS**	**Miscellaneous flags**
	D7	Alphanumeric Scanlines (with Bit 4): **Bit 7 Bit 4** 0 0 350-line Mode 0 1 400-line Mode 1 0 200-line Mode 1 1 (reserved)
	D6	1 – display switching is enabled 0 – display switching is disabled
	D5	(reserved)
	D4	(see Bit 7)
	D3	1 – default palette loading is disabled 0 – default palette loading is enabled
	D2	1 – using monochrome monitor 0 – using color monitor
	D1	1 – grayscale summing is enabled 0 – grayscale summing is disabled
	D0	1 – VGA active 0 – VGA not active

0040:008A BYTE	reserved
0040:008B BYTE	media control
0040:008C BYTE	Hard disk drive controller status
0040:008D BYTE	Hard disk drive error status
0040:008E BYTE	Hard disk drive interrupt control
0040:008F BYTE	reserved
0040:0090 BYTE	Drive 0 Media state
0040:0091 BYTE	Drive 1 Media state
0040:0092 BYTE	reserved
0040:0093 BYTE	reserved
0040:0094 BYTE	Drive 0 Current cylinder
0040:0095 BYTE	Drive 1 Current cylinder
0040:0096 BYTE	Keyboard Mode State and Type flags
0040:0097 BYTE	Keyboard LED Flags
0040:0098 WORD	Address offset to User Wait Complete flag
0040:009A WORD	Segment address to User Wait Complete flag
0040:009C WORD	User wait count – Low word (µsecs)
0040:009E WORD	User wait count – High word (µsecs)
0040:00A0 BYTE	Wait active flag
0040:00A1 BYTE	reserved
0040:00A2 BYTE	reserved
0040:00A3 BYTE	reserved
0040:00A4 BYTE	reserved
0040:00A5 BYTE	reserved
0040:00A6 BYTE	reserved
0040:00A7 BYTE	reserved

0040:00A8 DWORD SAVE_PTR Pointer to BIOS Save Pointer Table

NOTE: The next 84 bytes from 0040:00A1 to 0040:00FF are reserved.

Table 10–3. I/O Port Assignment for PC XT and AT Computers

Port Usage for PC XT	I/O Address	Port Usage for AT
DMA Controller	000 - 0IF	DMA Controller, Note 1
Interrupt Controller	020 - 03F	Interrupt Controller, Note 1
Timer	040 - 04F	Coprocessor access, Timer
	050 - 05F	Timer
PPI (system configuration)	060 - 063	
	060 - 06F	Keyboard
Reserved	070 - 07F	Real-time Clock
DMA Page Register	080 - 09F	DMA Page Register
NMI Mask Register	0A0 - 0AF	
	0A0 - 0BF	Interrupt Controller, Note 2
Reserved	0B0 - 0FF	
	0C0 - 0DF	DMA Controller, Note 2
	0F0 - 0FF	Math coprocessor
Unusable	100 - 13F	Reserved
Unusable	140 - 14F	Token Ring Adapter, Note 2
Unusable	150 - 15F	Advanced Color Graphics Display
Unusable	160 - 16F	Advanced Mono Graphics Display
Unusable	170 - 177	Fixed-disk Adapter, Note 2
Unusable	1C0 - 1CF	Token Ring Adapter, Note 1
Unusable	1E8 - 1EF	Streaming Tape Drive Adapter
Unusable	IF0 - IF7	Fixed-Disk Adapter, Note 1
Unusable	1F8 - 1FF	Reserved
Game I/O	200 - 20F	Game I/O
Expansion Unit	210 - 217	
Multifunction Card, Note 1	218 - 21F	Multifunction Card, Note 1
Reserved	220 - 24F	
	278 - 27F	Parallel Port 2
Clock Calendar, Note 1	2C0 - 2CF	Clock Calendar, Note 1
	2D0 - 2DF	3278/79 Emulation Adapter, Clock/calender, Note 1
Serial Port 4, Note 1	2E0 - 2E7	
Serial Port 3 or 4, Note 1	2E8 - 2EF	
Reserved	2F0 - 2F7	Interrupt Sharing
Serial Port 2	2F8 - 2FF	Serial Port 2
Prototype Card	300 - 31F	Prototype Card
Fixed Disk	320 - 32F	
	360 - 36F	PC Network
Parallel Port 1	378 - 37F	Parallel Port 1
SDLC	380 - 38F	SDLC, Bisync 2
Bisync	3A0 - 3AF	Bisync 1
MDA and printer adapter	**3B0 - 3BF**	**MDA, EGA/VGA and printer adapter**
EGA/VGA Adapter	**3C0 - 3CF**	**EGA/VGA**
CGA	**3D0 - 3DF**	**CGA, EGA/VGA**
Reserved	3E0 - 3E7	
Serial Port 3, Note 1	3E8 - 3EF	

Table 10–3. I/O Port Assignment for PC XT and AT Computers *(cont.)*

Port Usage for PC XT	I/O Address	Port Usage for AT
Diskette Controller	3F0 - 3F7	Diskette Controller
Serial Port 1	3F8 - 3FF	Serial Port 1
	400 - 43F	Reserved
	440 - 44F	Coprocessor Access
	450 - 50F	Reserved
	510 - 52F	Multi-protocol Adapter
	550 - 557	Coprocessor to main CPU communication
	6F0 - 6F7	Interrupt sharing
	910 - 92F	Multi-protocol Adapter
	D10 - D2F	Extended Monochrome Graphics Display
	E90 - E9F	PSLA
	1230-124F	1st Address range: multi-port async
	2230-224F	2nd Address range: multi-port async
	3230-324F	3rd Address range: multi-port async
	4230-424F	4th Address range: multi-port async
	46E8	**VGA add-in Adapter Sleep Enable**

NOTE: Use of port for this function is common, but not standard.

Table 10–4. Interrupt Vector Assignments

VECTOR TABLE ENTRY	INT NO.	NAME	
0000:0000	0	Divide by zero	
0000:0004	1	Single step	
0000:0008	2	Non-maskable	
0000:000C	3	Break-point	
0000:0010	4	Overflow	
0000:0014	5	Print screen	
0000:0018	6	(Reserved)	
0000:001D	7	(Reserved)	
0000:0020	8	Time	H/W IRQ0
0000:0024	9	Keyboard	H/W IRQ1
0000:0028	A	Network	H/W IRQ2
0000:002C	B	Comm. Port 2	H/W IRQ3
0000:0030	C	Comm. Port 1	H/W IRQ4
0000:0034	D	Hard disk	H/W IRQ5
0000:0038	E	Diskette	H/W IRQ6
0000:003C	F	Printer	H/W IRQ7
0000:0040	**10**	**EGA/VGA BIOS Video Services**	
0000:0044	11	Equipment check	
0000:0048	12	Determine memory size	
0000:004C	13	Diskette/disk	
0000:0050	14	Communications	
0000:0054	15	Cassette (***see*** Notes)	
0000:0058	16	Keyboard	
0000:005C	17	Printer	
0000:0060	18	Resident BASIC	
0000:0064	19	Bootstrap	
0000:0068	1A	Time of day	
0000:006C	1B	Keyboard break	
0000:0070	1C	Timer tick	
0000:0074	**1D**	**Video initialization**	
0000:0078	1E	Diskette parameters	
0000:007C	**1F**	**Optional Pointer to Upper 128 CGA 8 x 8 characters**	

Table 10–4. Interrupt Vector Assignments *(cont.)*

THE FOLLOWING INTERRUPTS ARE RESERVED FOR USE BY DOS:

VECTOR TABLE ENTRY	INT NO.	NAME
0000:0080	20	Program Terminate
0000:0084	21	Function Request
0000:0088	22	Terminate Process Exit Address
0000:008C	23	Control-C Handler Address
0000:0090	24	Critical Error Handler Address
0000:0094	25	Absolute Disk Read
0000:0098	26	Absolute Disk Write
0000:009C	27	Terminate But Stay Resident
0000:00AA-00B8	28-2E	RESERVED
0000:00BC	2F	Print Spool Control
0000:00C0-00FC	30-3F	RESERVED
0000:0108	**42**	**Old BIOS Video Services**
0000:010C	**43**	**Pointer to CGA 8 x 8 Char Set**

NOTES:

1) The INT 15 interrupt service handler has an additional responsibility in systems with an E000 segment video BIOS; besides cassette service, it will handle video subsystem services.
2) The complete list of interrupt numbers goes to FFH; each vector is a double word so the pointer for INT xH is stored at absolute location 4xH.

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Appendix A1

Connector Pinouts

CONNECTOR PINOUTS

Table A1–8. VGA DB15

Pin Number	Function
1	Analog RED
2	Analog GREEN
3	Analog BLUE
4	Monitor ID 2
5	No Connection
6	Analog RED Return
7	Analog GREEN Return
8	Analog BLUE Return
9	No Connection
10	Digital Ground
11	Monitor ID 0
12	Monitor ID 1
13	HSYNC
14	VSYNC
15	Monitor ID 3

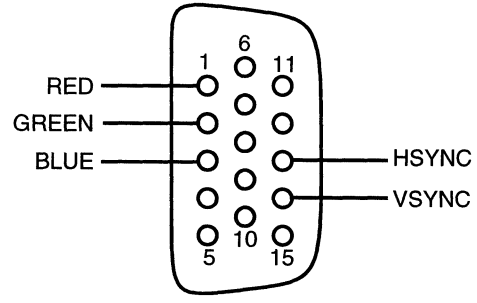
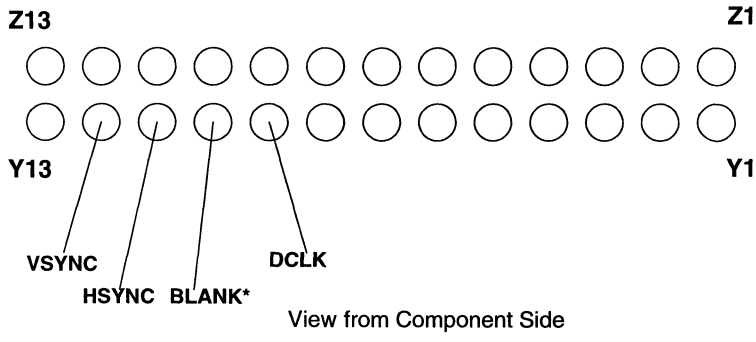


Table A1–9. VESA® Passthrough Connector

Number	Z	Y
1	Ground	P[0]
2	Ground	P[1]
3	Ground	P[2]
4	EVIDEO*	P[3]
5	ESYNC*	P[4]
6	EDCLK*	P[5]
7	+5V (Note)	P[6]
8	Ground	P[7]
9	Ground	DCLK
10	Ground	BLANK*
11	Ground	HSYNC
12	MCLK (Note)	VSYNC
13	OVRW* (Note)	Ground

NOTE: These pins are assigned by Cirrus Logic for VAFC Support.



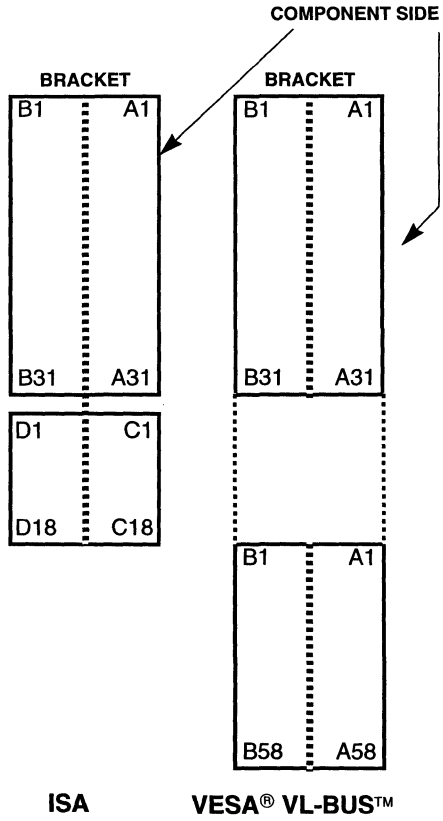
View from Component Side

Table A1–10. ISA Bus

Pin	Component Side A	Solder Side B	Component Side C	Solder Side D
1	IOCHCHK*	Ground	SBHE*	MCS16*
2	SD7	RESET	LA23	IOCS16*
3	SD6	+5V	LA22	IRQ10
4	SD5	IRQ9	LA21	IRQ11
5	SD4	-5V	LA20	IRQ12
6	SD3	DRQ2	LA19	IRQ15
7	SD2	-12V	LA18	IRQ14
8	SD1	0WS*	LA17	DACK0*
9	SD0	+12V	MEMR*	DRQ0
10	IOCHRDY	Ground	MEMW*	DACK5*
11	AEN	SMEMW*	SD8	DRQ5*
12	SA19	SMEMR*	SD9	DACK6*
13	SA18	IOW*	SD10	DRQ6
14	SA17	IOR*	SD11	DACK7*
15	SA16	DACK3*	SD12	DRQ7
16	SA15	DRQ3	SD13	+5V
17	SA14	DACK1*	SD14	MASTER*
18	SA13	DRQ1	SD15	Ground
19	SA12	REFRESH*		
20	SA11	CLK		
21	SA10	IRQ7		
22	SA9	IRQ6		
23	SA8	IRQ5		
24	SA7	IRQ4		
25	SA6	IRQ3		
26	SA5	DACK2*		
27	SA4	T/C		
28	SA3	BALE		
29	SA2	+5V		
30	SA1	OSC		
31	SA0	Ground		

Table A1–11. VESA® VL-Bus (CL-GD5424/'26/'28/'29 only)

Pin	Solder Side 'B'	Component Side 'A'	Pin	Solder Side 'B'	Component Side 'A'
1	DAT00	DAT01	30	ADR17	ADR16
2	DAT02	DAT03	31	ADR15	ADR14
3	DAT04	GND	32	V_{CC}	ADR12
4	DAT06	DAT05	33	ADR13	ADR10
5	DAT08	DAT07	34	ADR11	ADR08
6	GND	DAT09	35	ADR09	GND
7	DAT10	DAT11	36	ADR07	ADR06
8	DAT12	DAT13	37	ADR05	ADR04
9	V_{CC}	DAT15	38	GND	WBACK# (not used)
10	DAT14	GND	39	ADR03	BE0#
11	DAT16	DAT17	40	ADR02	V_{CC}
12	DAT18	V_{CC}	41	n/c	BE1#
13	DAT20	DAT19	42	RESET# (not used)	BE2#
14	GND	DAT21	43	D/C# (not used)	GND
15	DAT22	DAT23	44	M/IO#	BE3#
16	DAT24	DAT25	45	W/R#	ADS#
17	DAT26	GND	46	Key	Key
18	DAT28	DAT27	47	Key	Key
19	DAT30	DAT29	48	RDYRTN#	LRDY#
20	V_{CC}	DAT31	49	GND	LDEV<X>#
21	ADR31	ADR30	50	IRQ9 (not used)	LREQ<X># (not used)
22	GND	ADR28	51	BRDY# (not used)	GND
23	ADR29	ADR26	52	BLAST# (not used)	LGNT<X>#
24	ADR27	GND	53	ID0 (not used)	V_{CC}
25	ADR25	ADR24	54	ID1 (not used)	ID2 (not used)
26	ADR23	ADR22	55	GND	ID3 (not used)
27	ADR21	V_{CC}	56	LCLK	ID4 (not used)
28	ADR19	ADR20	57	V_{CC}	LKEN# (not used)
29	GND	ADR18	58	LBS16#	LEADS# (not used)



Appendix B1

16-Bit ISA Adapter Board
Application Note

16-BIT ISA ADAPTER BOARD

1. INTRODUCTION

This application note discusses the logic design and layout of an ISA adapter for the CL-GD542X family of VGA controllers; please refer to Chapter 3 , *Data Book* for a list of controller features. Since the CL-GD542X family shares a common pinout, the only schematic differences are in the Video Memory interface. The CL-GD5420 is limited to a maximum of 512K bytes of DRAM, the CL-GD5422 and CL-GD5424 are limited to 1 Mbyte, and the CL-GD5426/'28/'29 can support up to 2 Mbytes. This application note covers the ISA bus interface, BIOS, display memory, Monitor/Video DAC interface, Integrated Clock, and hardware features.

A sample system schematic and bill of materials are included at the end of this appendix. The schematic capture program used for generating the sample adapter schematic is ORCAD™ SDT 4.10. The schematic and layout (Gerber Output) files are included with the manufacturing package, or these files can be downloaded from the Cirrus Logic Bulletin Board Service, (510) 440-9080 (refer to Appendix D9 for more information about the BBS). The manufacturing package consists of all the documentation, software, firmware, working files, and sample components necessary for evaluating the CL-GD542X in an adapter implementation.

2. ISA BUS INTERFACE

An adapter board based on this schematic will not function in an 8-bit ISA connector; the schematic shown is for an implementation of the CL-GD542X for a 16-bit-only ISA bus Interface. The adapter board is limited to a 16-bit ISA interface because SA17, SA18, and SA19 (from the 8-bit connector) are not used and are replaced by LA17, LA18, and LA19 (from the 16-bit connector).

The Bus Interface signals do not require additional buffering, as the CL-GD542X will directly drive the ISA bus. The active-high RESET DRV signal from the ISA bus needs to be conditioned by an R/C network (R2 and C19) to filter out any possible noise or glitches. Jumper JP1 is for PC/AT 0WS (zero-wait-state) operation. Placing a shunt on this jumper allows the CL-GD542X to signal the system processor that the present bus cycle can be completed without inserting additional ISA bus wait states. The reference 14.31818-MHz signal required by the integrated frequency synthesizer is obtained from the unbuffered ISA bus OSC input.

3. BIOS

The BIOS EPROM support logic consists of either one or two sets of EPROM and octal bidirectional buffers. One set (U2 and U3) is required for an 8-bit-only BIOS. The complete complement of U2, U3, U5, and U6, as well as R15 (pull-down resistor on MD22), is required for a 16-bit BIOS. The BIOS is linear, that is, both EPROMs contain identical data and are inter changeable. Configuration resistor R16 (pull-down resistor on MD17) is required if the adapter board is to operate with zero-wait-state access to the BIOS EPROMs. The EPROMs must have a less than 200-ns access time, but 150 ns is best for reliable zero-wait-state operation.

4. DISPLAY MEMORY

The display memory, as shown in the schematics for the CL-GD542X, can be configured for either 512K bytes or 1 Mbyte of 256K x 4 memory (the schematics show both SOJ and DIP package pinouts). The CL-GD5420 display memory (on the board), is limited to 512K bytes; it *cannot* be expanded to 1 Mbyte if 256K x 4 DRAMs are used. The schematics must be redrawn to support different DRAM configurations, such as symmetric or asymmetric, SOJ or DIP, and 256K x 4, 512K x 8, or 256K x 16. Refer to Appendix B7 for an overview of all the possible memory types and their connection to the CL-GD542X.

The allowable DRAM types with the optimum t_{RAC} time for a specific Memory Clock (MCLK) can also be determined from Appendix B7, which describes the DRAM timings expected from each Memory Clock selection. The Memory Clock frequency is selected by R17 and R18, as shown in the DRAM timing options found in the schematic. Resistor R23 is used for choosing high-performance or normal MCLK RAS cycles. Refer to Appendix B9 for an explanation of the various possible configuration settings.

5. MONITOR/VIDEO DAC INTERFACE

The integrated Video DAC requires an external current-reference source (IREF) consisting of Q1 (2N3904), D5 (TL431), and the associated R/C components shown on the schematic. This is an inexpensive IREF circuit that does not require a negative-voltage source. This circuit can easily be replaced with any one of various current-reference circuits based on an LM337, LM334, LP2951, or LM317, as long as the nominal IREF current drawn through the IREF pin is 6.7 mA. The IREF current determines the full-scale output voltage of the Video DAC, and therefore the brightness of the displayed image.

The included schematic shows optional diodes D1, D2, D3, and D4 that can provide Electrostatic Discharge (ESD) protection and prevent latch-up in the CL-GD542X. Latch-up can occur due to high-energy discharges from monitor arc-over or from 'hot-switching' AC-coupled monitors. These diodes can be left out of the circuit without affecting the normal operation of the adapter board.

The analog Red, Green, and Blue (RGB) lines going from the CL-GD542X to the Monitor Interface Connector (P1) have standard PI-filter circuits to reduce EMI and noise for FCC Class B compliance. The analog outputs are capable of directly driving a singly-terminated 75-ohm load to a peak-white amplitude of 0.7V. The 150-Ω pull-down resistors on the RGB lines correspond to an effective DAC output loading of 50 ohms. Each RGB analog output should have a source-load resistor located as close as possible to the CL-GD542X to minimize reflections.

6. INTEGRATED CLOCK

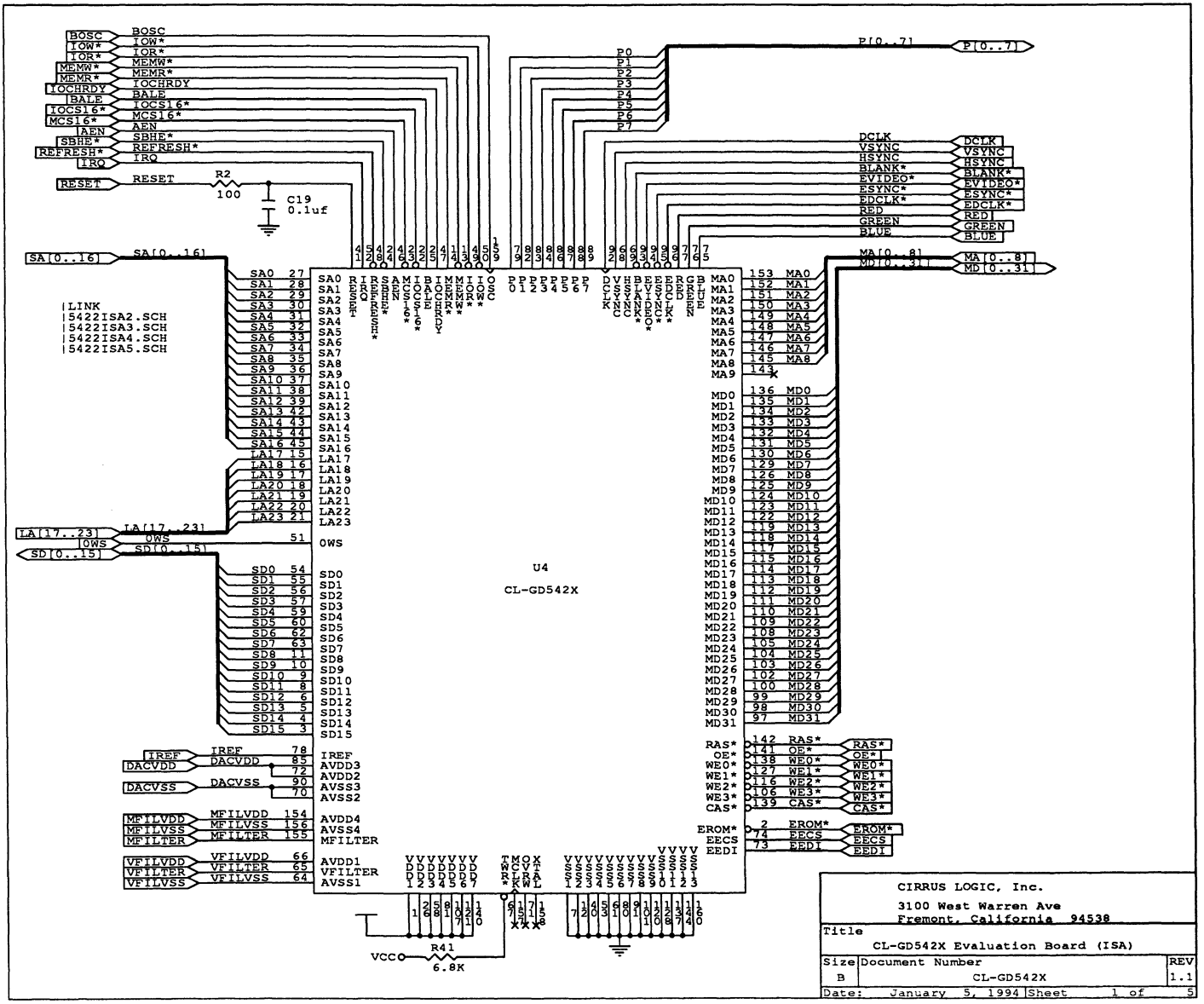
The integrated dual-clock synthesizer uses the 14.31818-MHz clock from the ISA bus as a reference for generating the VCLKs (Video Clock) and MCLKs (Memory Clock). This reference clock can be replaced by a 14.31818-MHz series-resonant crystal by disconnecting the trace to ISA bus pin B30, and connecting the crystal across pins 158 and 159 of the CL-GD542X (pin 158 is a no-connect).

The internal dual-clock synthesizer requires two external loop-filter circuits, one for the VCLK, and the other for MCLK. The Memory Clock filter consists of R19, C29, and CC25. The VCLK filter consists of R13, C13, and C17 for N-WELL devices and R13, C38, and C39 for P-WELL devices. Refer to Appendix B17 for a description of N-WELL versus P-WELL device considerations.

7. HARDWARE FEATURES

The schematic shows that the adapter board can be configured to support an external EEPROM (U1) for storing monitor timing options. Choosing not to install an EEPROM (U1) will not affect the operation of the adapter board, but it will require the execution of a configuration program from within the AUTOEXEC.BAT file. If the EEPROM is not installed, R3 and R4 are not required; however, the traces from J1 pins 10 and 8 must be connected to CL-GD542X pins 94 and 95, respectively, if the VESA Connector is to be used.

Adding J1 will provide a VESA-compliant VGA passthrough connector for transferring pixel data to or from the internal Video DAC. The 13-pin-by-2-row connector is a less costly alternative than the IBM version, which requires a routing of the printed circuit board. If the connector is not installed, R3 and R4 are not required. Choosing not to install the connector will not affect the operation of the adapter board.



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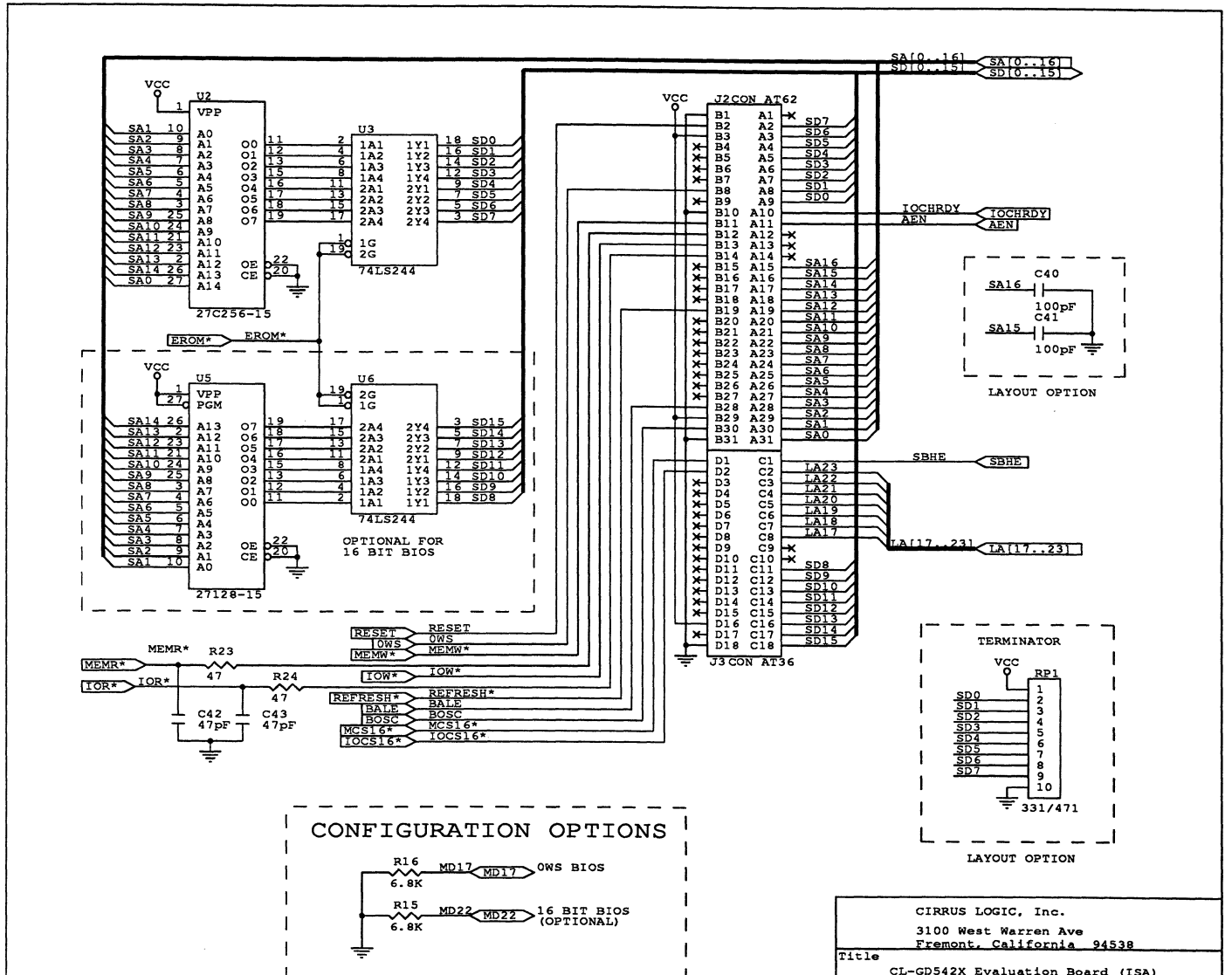
CL-GD542X Evaluation Board (ISA)		
Size: B	Document Number: CL-GD542X	REV: 1.1
Date: January 5, 1994	Sheet 1 of 5	



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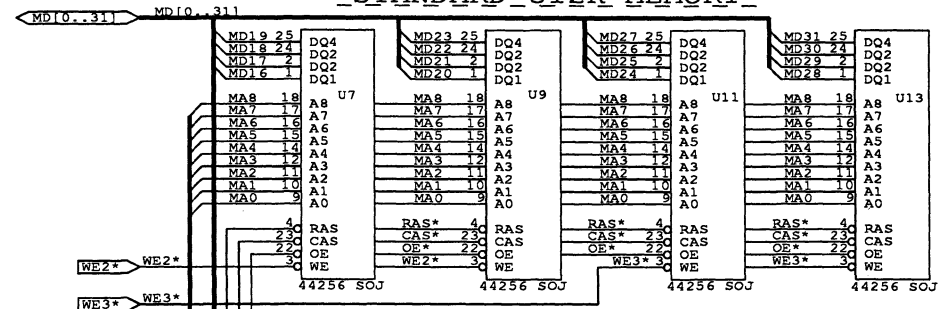
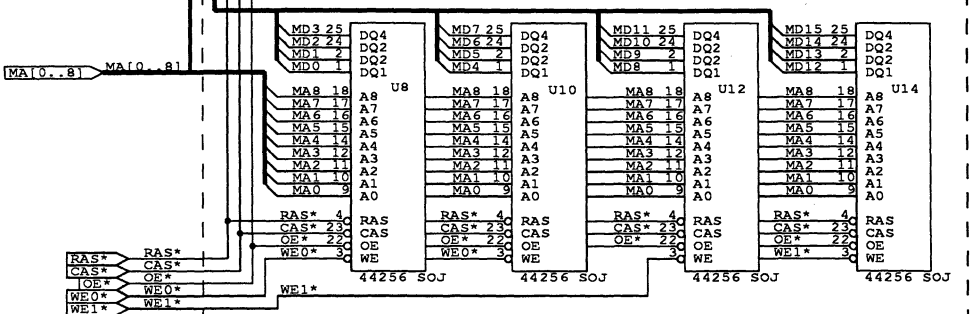
Size	Document Number	REV
B	ISA BUS & BIOS	1.1
Date: January 5, 1994	Sheet 2 of 5	

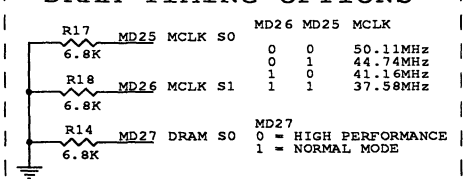
_STANDARD_512K MEMORY_



1 MEG DRAM OPTION



DRAM TIMING OPTIONS



NOTE: DRAM SPEED DEPENDS ON THE DRAM TIMING OPTIONS
REFER TO APP NOTE B7:MEMORY CONSIDERATIONS

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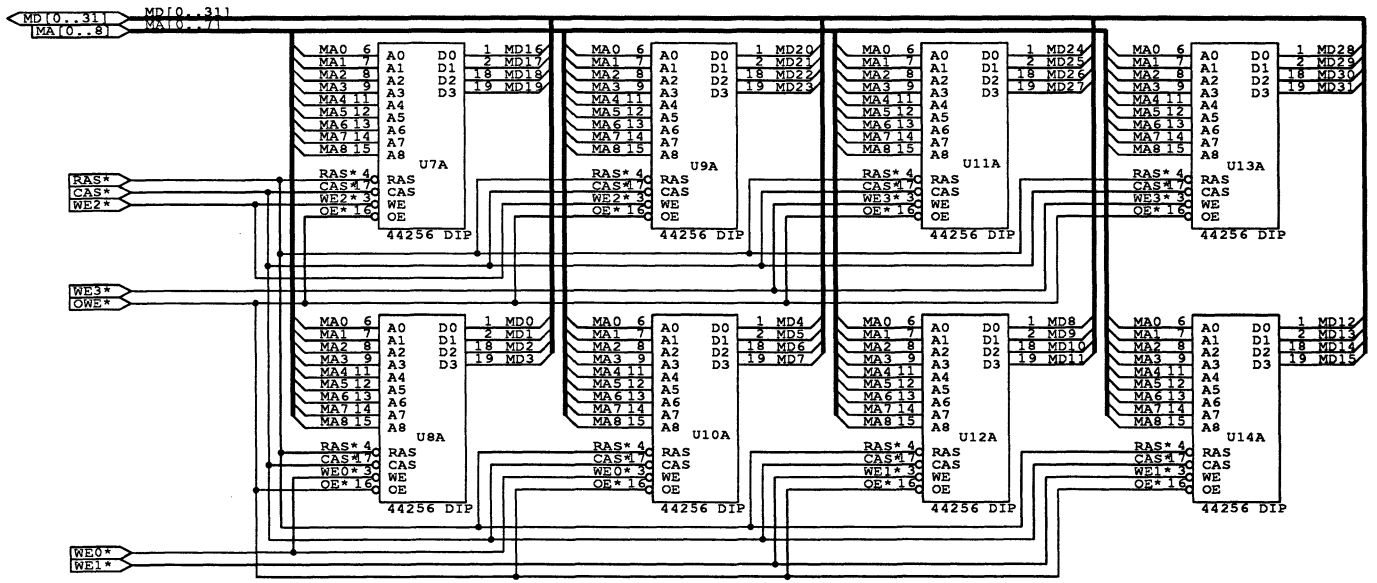
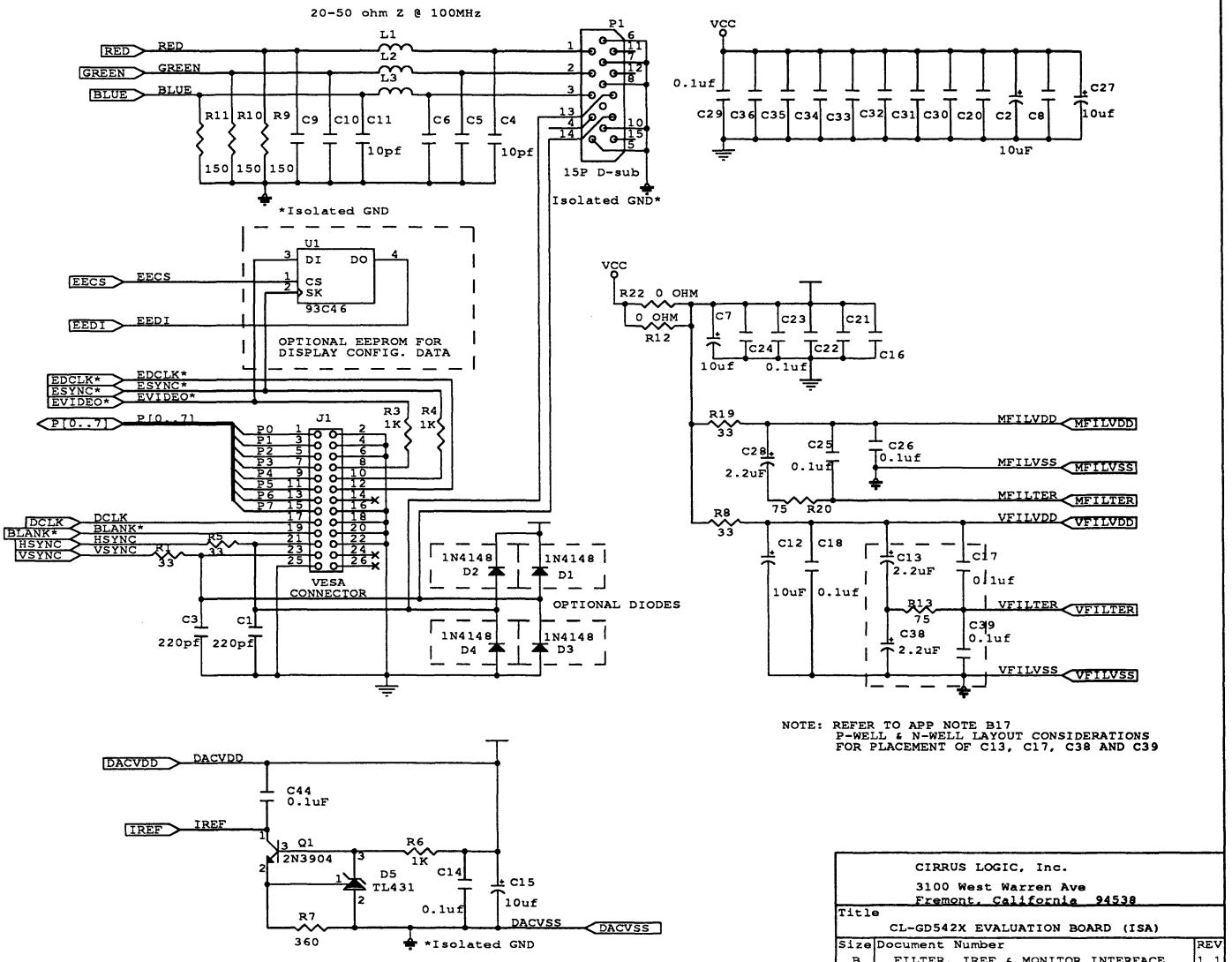
Title		
CL-GD542X Evaluation Board (ISA)		
Size: B	Document Number: TOTAL 1Mb Memory	REV: 1.1
Date: January 5, 1994	Sheet 3 of 5	

ALTERNATIVE 1MB DRAM MEMORY (DIP PACKAGE)

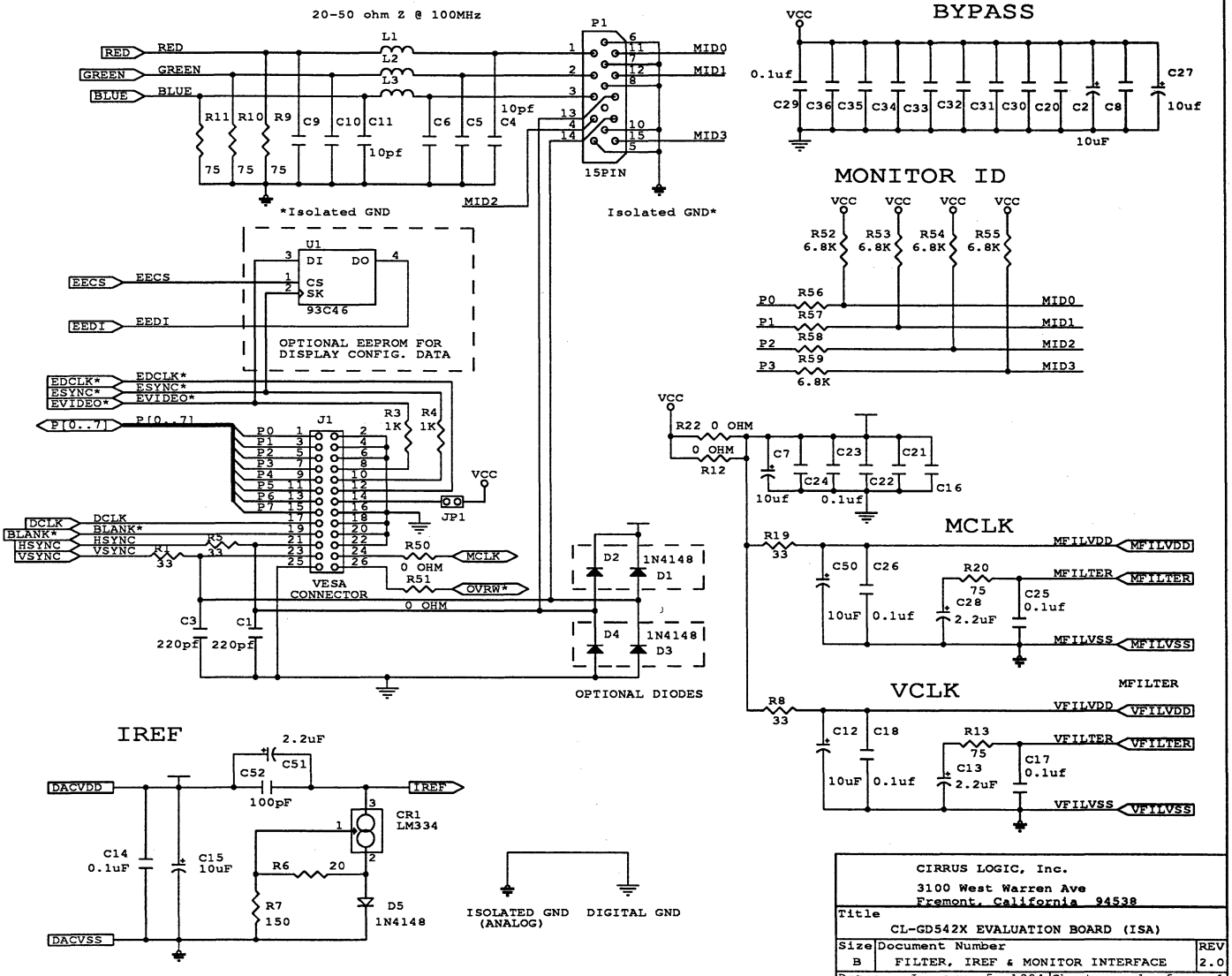


CIRRUS LOGIC, Inc. 3100 West Warren Ave Fremont, California 94538		
Title: CL-GD542X Evaluation Board (ISA)		
Size: B	Document Number: ALTERNATIVE DIP DRAM MEMORY	REV: 1.1
Date: January 5, 1994	Sheet 4 of 5	



CIRRUS LOGIC, Inc. 3100 West Warren Ave Fremont, California 94538		
Title: CL-GD542X EVALUATION BOARD (ISA)		
Size: B	Document Number: FILTER, IREF & MONITOR INTERFACE	REV: 1.1
Date: January 5, 1994	Sheet 5 of 5	

NOTE: FOR NEW DESIGN, REPLACE PAGE 5 WITH THIS PAGE.



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Title	CL-GD542X EVALUATION BOARD (ISA)	
Size B	Document Number FILTER, IREF & MONITOR INTERFACE	REV 2.0
Date: January 5, 1994	Sheet 1 of 1	

Note : Use this BOM only if the page 5 (rev 1.1) is replaced by the new page 5(rev 2.0).

CL-GD542x Evaluation Board — Revised: Jan 5, 1994
SOJ/DIP DRAMs — Revision: 1.0
Bill Of Materials — Page 1

Item	Qty	Reference	Part
1	2	C1,C3	220pf, 50V Ceramic CAP
2	24	C2,C8,C14,C16,C18,C19, C20,C21,C22,C23,C24,C25, C26,C30,C31,C32,C33,C34, C35,C36,C29,C17,C44,C52	0.1uf, 35V, 20%, Ceramic CAP
3	6	C4,C5,C6,C9,C10,C11	10pf, 50V Ceramic CAP
4	3	C13,C28,C51	2.2uF, 16V, 20% Tantalum CAP
5	5	C7,C12,C15,C27,C50	10uf, 16V, 20%, Tantalum CAP
6	2	C40,C41	100pf, 50V Ceramic CAP
7	2	C42,C43	47pf, 50V Ceramic CAP
8	4	R1,R5,R8,R19	33 Ohm Resistor, 1/4W, 5%
9	4	R2,R3,R4	1K Ohm Resistor, 1/4W, 5%
10	1	R6	20 Ohm Resistor, 1/4W, 1%
11	1	R7	150 Ohm Resistor, 1/4W, 5%
12	2	R22,R12	0 Ohm Resistor
12A*	2	R50,R51	0 Ohm Resistor
13	5	R20,R13,R9,R10,R11	75 Ohm Resistor, 1/4W, 5%
14	5	R14,R15,R16,R17,R18	6.8K Ohm Resistor, 1/4W, 5%
14A*	8	R52,R53,R54,R55,R56 R57,R58,R59	6.8K Ohm Resistor, 1/4W, 5%
15	2	R23,R24	47 Ohm Resistor, 1/4W, 5%
16	1	RP1##	SIP 10, Data Terminator (see note)
17*	4	D1,D2,D3,D4	1N4148, 10ma Switching DIODE
18	1	CR1	LM334, Current Source, TO-92
19	1	D5	1N4148, 10ma Switching DIODE
20*	1	U1	NM93C46N, Configuration EEPROM
21	2	U3,U6	74LS244, Bus Transceiver
22	1	U4	CL-GD542x, Cirrus VGA Controller
23*	2	U2,U5	27256-15, BIOS ROM
24	8	U7,U8,U9,U10, U11,U12,U13,U14	44256-70, 256Kx4 DRAM, SOJ (USE DIP OR SOJ)
25	8**	U7A,U8A,U9A,U10A, U11A,U12A,U13A,U14A	44256-70, 256Kx4 DRAM, DIP (USE DIP OR SOJ)
26	3	L1,L2,L3	Ferrite bead, 20-50 ohms Z @ 100MHz
27	1	P1	15P D-SUB, PC Mount
28	1	JP1	1x2 PIN, 0.1" Space, Twin Jumper
29	1	J1	13x2 PIN HEADER
30	1	Mounting Bracket	GLOBE MFG., Type G172 or Equiv.
31	2**	Socket	28 Pin Socket for BIOS
32	1	Printed Circuit Board	CL-GD542x PCB

NOTE: * = Optional Components
** = Only one Optional
= Thevinen-equivalent terminators with 330 ohms pullups to VCC and 470 ohm pulldowns to ground (GND).
PIN 1 = VCC, PIN 10 = GND, PIN [2..9] = SD[0..7]

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Appendix B2

MicroChannel Board
Application Note

MICROCHANNEL BOARD[1]

1. INTRODUCTION

This application note discusses a possible logic design of an MicroChannel adapter for the CL-GD542X. Since the CL-GD542X family shares a common pinout, the only schematic differences are in the Video Memory interface. The CL-GD5422 is limited to 1 Mbyte; the CL-GD5426/'28/'29 can support up to 2 Mbytes. The discussion covers the MicroChannel bus interface, BIOS, display memory, the Monitor/Video DAC Interface, Integrated Clock, and hardware features.

A sample system schematic and bill of materials are included at the end of this appendix. A sample adapter schematic and layout (Gerber Output) files are included with the manufacturing package, or these files can be downloaded from the Cirrus Logic Bulletin Board System, (510) 440-9080 (refer to Appendix D9 for more information about the BBS). The schematic-capture program used for generating the sample adapter schematic is ORCAD™ SDT 4.10. The manufacturing package consists of all the documentation, software, firmware, working files, and sample components necessary for evaluating the CL-GD542X in an adapter implementation.

2. MICROCHANNEL® BUS INTERFACE

The Bus Interface signals do not require additional buffering; the CL-GD542X will directly drive the MicroChannel bus. The active-high CHRESET signal from the MicroChannel bus needs to be conditioned by an R/C network (R2 and C19) to filter out any possible noise or glitches. The reference 14.31818-MHz signal required by the integrated frequency synthesizer is obtained from the unbuffered MicroChannel bus OSC Input.

The MicroChannel schematic has an external PAL22V10 (U17), which has the address decodes for read-only POS registers 100h and 101h. Register 100h reads back an 80h and register 101h reads back 63h when CDSETUP is active at boot-up. In MicroChannel mode, the CL-GD542X chips only respond to Sleep Address 3C3h, whether in an adapter or motherboard configuration. This can be a problem in adapter applications; a full implementation may require extra external logic to compensate for the missing adapter-board Sleep Address 46E8h.

A pull-down Configuration resistor, R24, is required to configure the CL-GD542X for MicroChannel operation.

3. BIOS

The BIOS EPROM support logic consists of either one or two sets of EPROMs, an octal bidirectional buffer, and two octal latches. The address latches (U15 and U16) capture the least-significant 16-bit address from the bus (on the MicroChannel bus, the address is not

1. This appendix applies only to CL-GD5426/'28 at the time of this publication.

required to remain stable throughout the cycle). The latches are transparent as long as CMD* is high, and latch the address while CMD* is low. The latched address is only for the EPROM since the CL-GD542X latches the address with CMD*.

One set of EPROMs and buffers (U2 and U3) is required for an 8-bit-only BIOS. The complete set of U2, U3, U5, and U6, as well as R14 (pull-down resistor on MD22) is required for a 16-bit BIOS. The BIOS is linear, that is, it will not split with odd and even bytes. Configuration resistor R15 (pull-down resistor on MD17) is required if the adapter board is to operate with zero-wait-state access to the BIOS EPROMs. The EPROMs must have a less than 200-ns access time (150 ns is recommended) for reliable, zero-wait-state operation.

4. DISPLAY MEMORY

The display memory, as shown in the schematic for the CL-GD542X, can be configured for either 512K bytes or 1 Mbyte of 256K x 4 memory (the schematics show both SOJ and DIP package pinouts). The display memory size for the CL-GD5420 is limited to 512K bytes; it *can only* be expanded to 1 Mbyte using 512K x 8 DRAMs. The schematics must be redrawn to support different DRAM configurations, such as symmetric or asymmetric, SOJ or DIP, and 256K x 4, 512K x 8, or 256K x 16. Refer to the DRAM Configuration Table in Appendix B7 for an overview of all the possible memory types and their connection to the CL-GD542X.

The allowable DRAM types with the optimum t_{RAC} time for a specific MCLK (Memory Clock) can also be determined from Appendix B7, which also documents the DRAM timings expected from each MCLK selection. The MCLK frequency is selected by R16 and R17, as shown in the DRAM timing options found in the schematic. Resistor R23 is used for choosing high-performance or normal MCLK RAS cycles. Refer to Appendix B9 for an explanation of the various configuration settings possible.

5. MONITOR/VIDEO DAC INTERFACE

The integrated Video DAC requires an external current-reference source (IREF) consisting of Q1, D5, and the associated R/C components shown on the schematic. This is an inexpensive IREF circuit that does not require a negative-voltage source. This circuit can easily be replaced with any one of various current-reference circuits based on an LM337, LM334, LP2951, or LM317, as long as the nominal IREF current drawn through the IREF pin is 6.7 mA. The IREF current determines the full-scale output voltage of the Video DAC, and therefore determines the brightness of the displayed image.

The schematic shows optional diodes D1, D2, D3, and D4 that can provide ESD (Electrostatic Discharge) protection and prevent latch-up in the CL-GD542X. Latch-up can occur due to high-energy discharges from monitor arc-over or from 'hot-switching' AC-coupled monitors. These diodes can be left out of the circuit without affecting the normal operation of the adapter board.

The analog Red, Green, and Blue (RGB) lines going from the CL-GD542X to the monitor interface connector (P1) have standard PI-filter circuits to reduce EMI and noise for FCC Class B compliance. The analog outputs are capable of directly driving a singly-terminated 75-Ω load to a peak-white amplitude of 0.7V. The 150-Ω pull-down resistors on the RGB lines correspond to an effective DAC output loading of 50 ohms. Each RGB analog output should have a source-load resistor located as close as possible to the CL-GD542X to minimize reflections.

6. INTEGRATED CLOCK

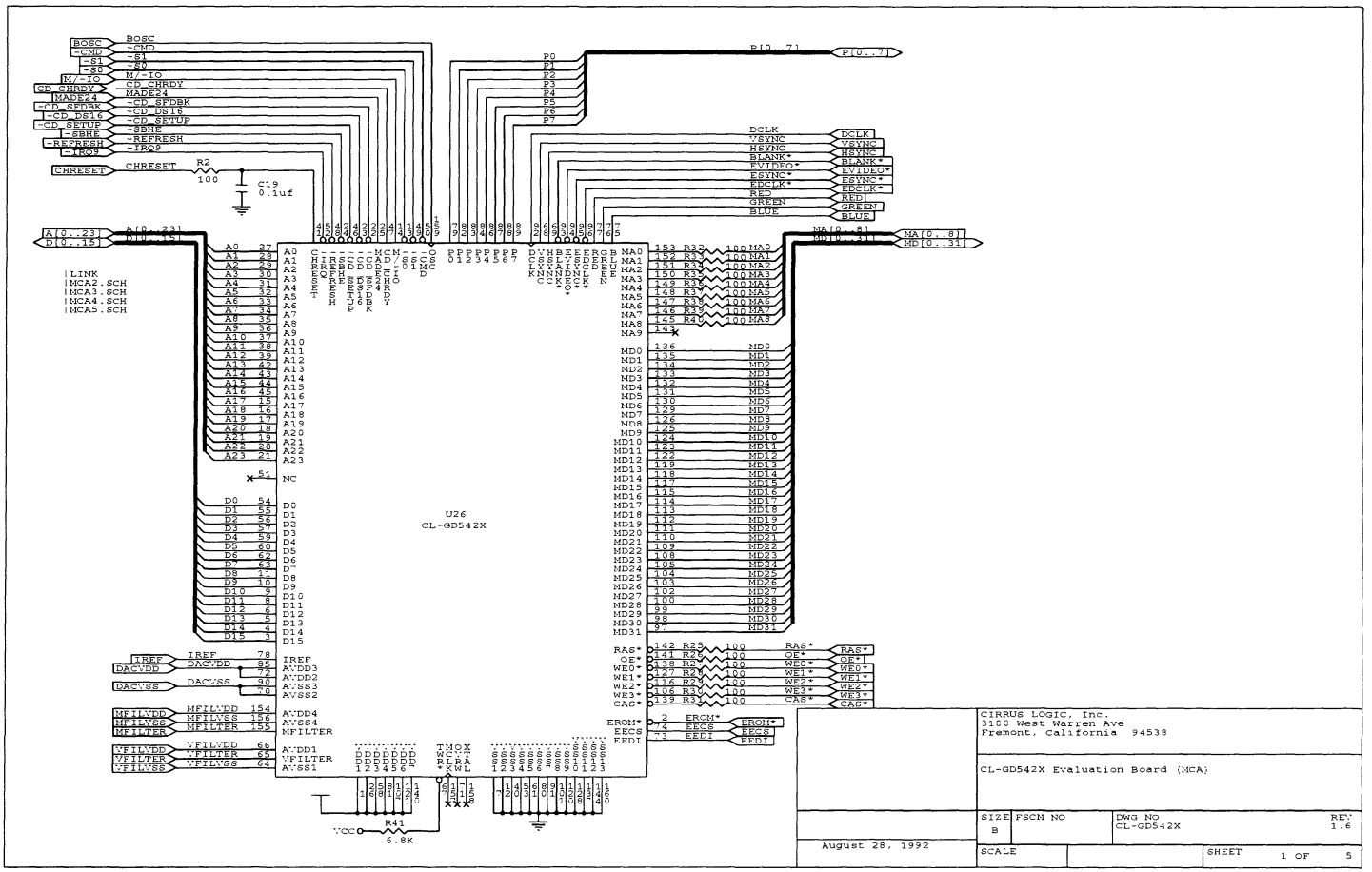
The integrated dual-clock synthesizer uses the 14.31818-MHz clock from the MicroChannel bus as a reference for generating the VCLKs (Video Clock) and MCLKs. This reference clock can be replaced by a 14.31818-MHz series-resonant crystal by disconnecting the trace to MicroChannel bus pin, B4, and connecting the crystal across pins 158 and 159 of the CL-GD542X (pin 158 is a no-connect).

The internal dual-clock synthesizer requires two external loop-filter circuits, one for the VCLK, and the other for the MCLK. The MCLK filter consists of R19, C29, and C25. The VCLK filter consists of R13, C13, and C17. Both of these filters require a separate, isolated ground.

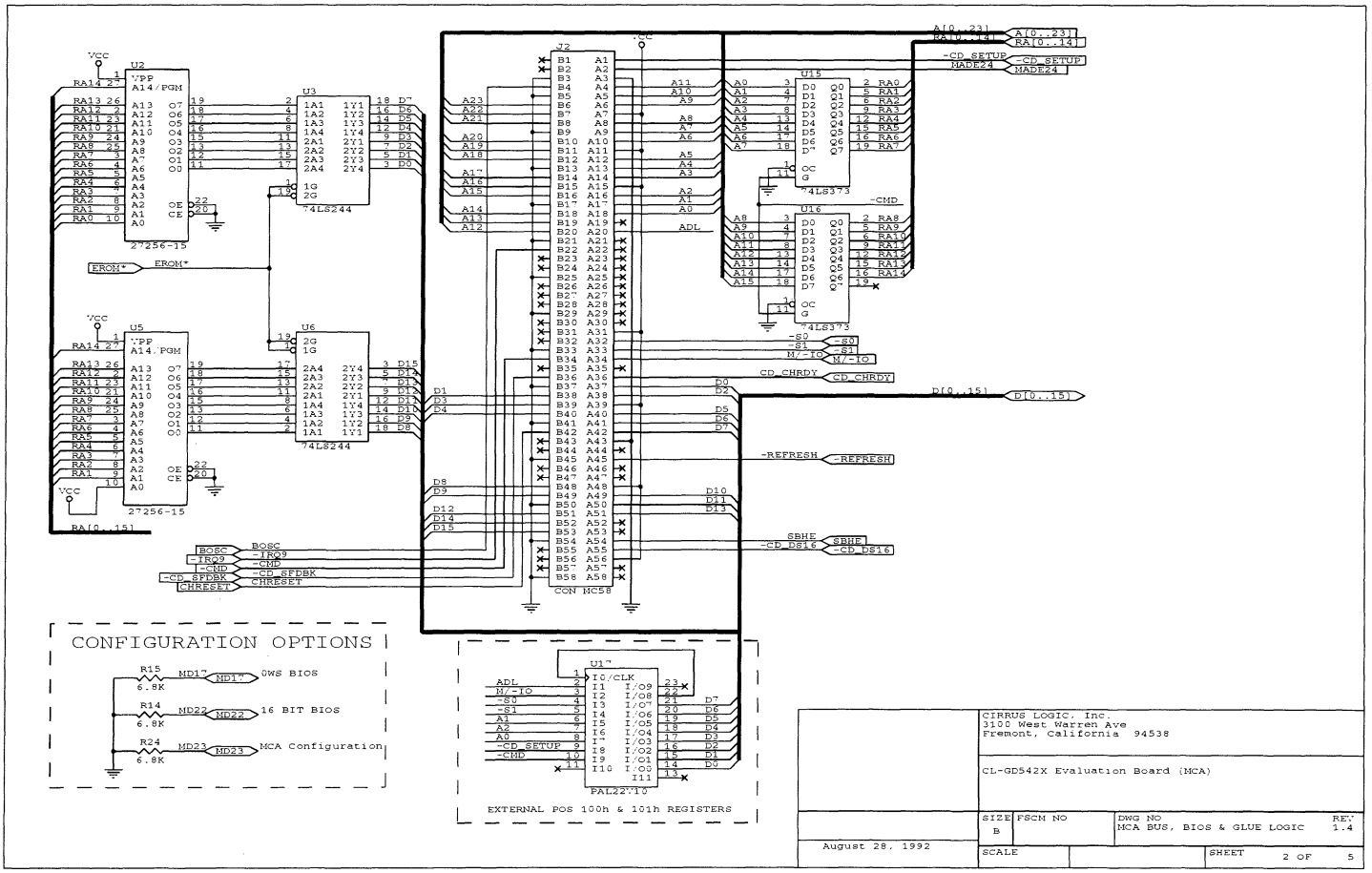
7. HARDWARE FEATURES

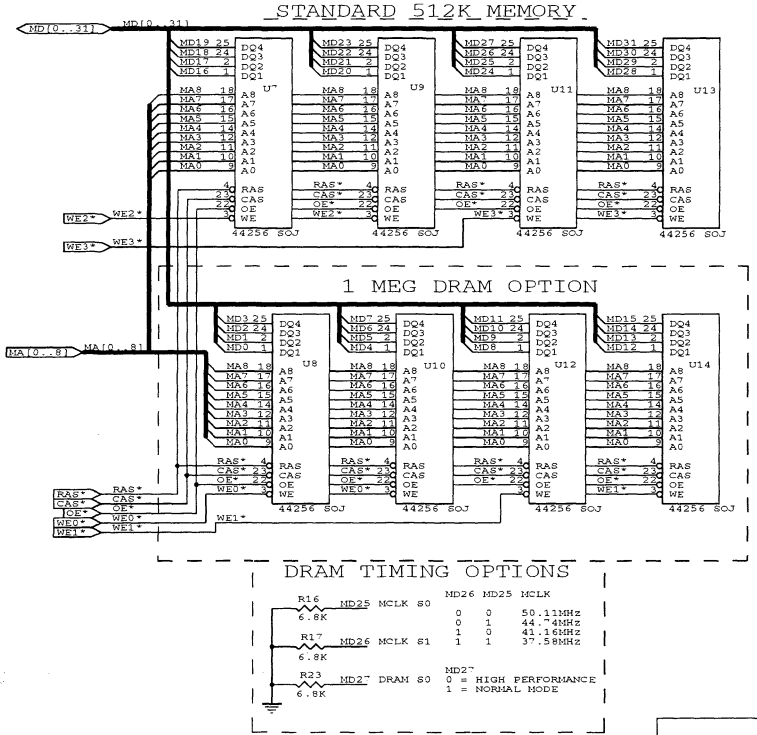
The sample schematic included in this appendix shows that the adapter board can be configured to support an external EEPROM (U1) for storing monitor timing options. Choosing not to install an EEPROM (U1) will not affect the operation of the adapter board, but will require the execution of a configuration program from within the AUTOEXEC.BAT file. If the EEPROM is not installed, R3 and R4 are not required . However, if the VESA connector is to be used, the traces from J1 pins 10 and 8 must be connected to CL-GD542X pins 94 and 95, respectively.

Adding J1 will provide a VESA-compliant VGA passthrough connector for transferring pixel data to or from the internal Video DAC. The 13-pin-by-2-row connector is a less costly alternative to the IBM version, which requires a routing of the printed circuit board. If the connector is not installed, R3 and R4 are not required. Choosing not to install the connector will not affect the operation of the adapter board.



	CIRRUS LOGIC, Inc. 3100 West Warren Ave Fremont, California 94538		
	CL-GD542X Evaluation Board (MCA)		
	SIZE B	FSCM NO	DWG NO CL-GD542X REV 1.6
August 28, 1992	SCALE		SHEET 1 OF 5


CONFIGURATION OPTIONS
R15 6.8K MD17 MD17* 0WS BIOS
R14 6.8K MD22 MD22 16 BIT BIOS
R24 6.8K MD23 MD23 MCA Configuration
EXTERNAL POS 100h & 101h REGISTERS
CON MC58
PAL22V10
74LS244
74LS373
27256-15
EPROM*
CIRRUS LOGIC, Inc.
3100 West Warren Ave
Fremont, California 94538
CL-GD542X Evaluation Board (MCA)
August 28, 1992
SIZE B
FSCM NO
DWG NO MCA BUS, BIOS & GLUE LOGIC
REV 1.4
SCALE
SHEET 2 OF 5



DRAM TIMING OPTIONS

R16 6.8K — MD25 MCLK S0
R17 6.8K — MD26 MCLK S1
R23 6.8K — MD27 DRAM S0

MD26	MD25	MCLK
0	0	50.11MHz
0	1	44.74MHz
1	0	41.16MHz
1	1	37.58MHz

MD27
0 = HIGH PERFORMANCE
1 = NORMAL MODE

NOTE: DRAM SPEED DEPENDS ON THE DRAM TIMING OPTIONS
REFER TO APP NOTE B":MEMORY CONSIDERATIONS

CIRRUS LOGIC, Inc.
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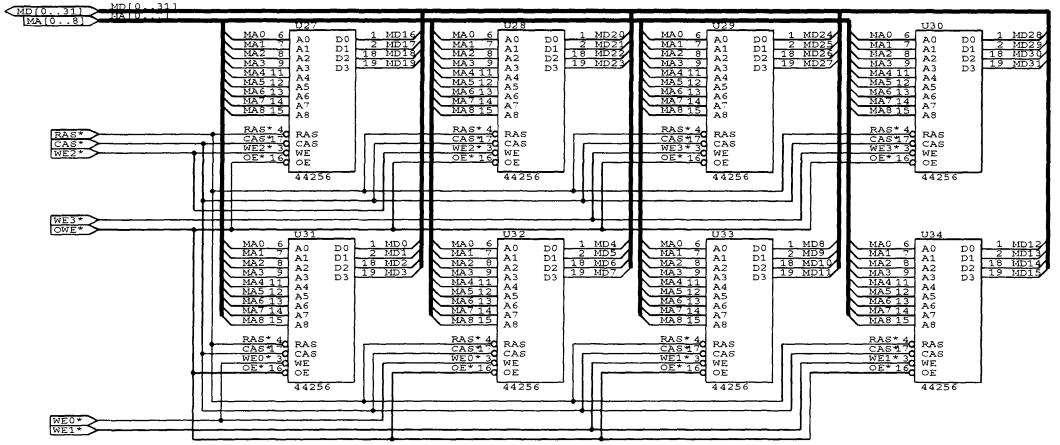
Fremont, California 94538

CL-GD542X Evaluation Board (MCA)

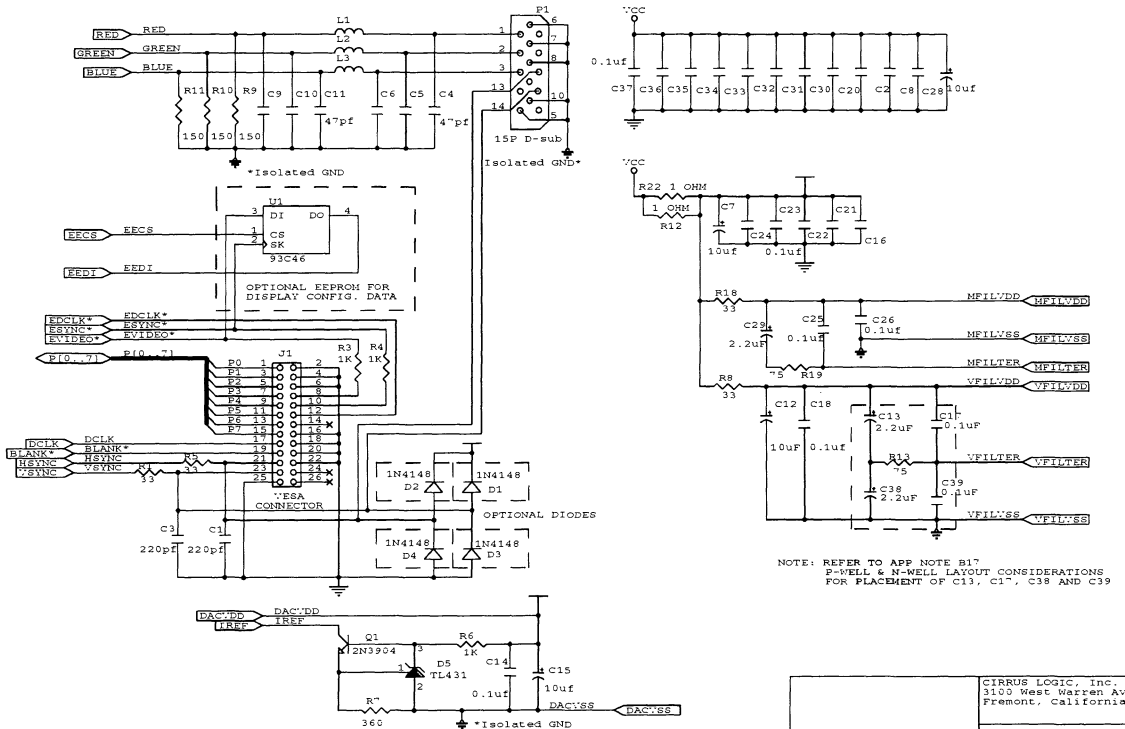
SIZE	FSCM NO	DWG NO	REV
B		TOTAL 1Mb Memory	1.4

August 28, 1992 | SCALE | SHEET 3 OF 5

ALTERNATIVE 1MB DRAM MEMORY (DIP PACKAGE)



	CIRRUS LOGIC, Inc. 3100 West Warren Ave Fremont, California 94538			
	CL-GD542X Evaluation Board (MCA)			
	SIZE B	FSCN NO	DWG NO ALTERNATIVE DIP DRAM MEMORY	REV 1.4
August 28, 1992	SCALE		SHEET 4 OF 5	



NOTE: REFER TO APP NOTE B17
P-WELL & N-WELL LAYOUT CONSIDERATIONS
FOR PLACEMENT OF C13, C17, C38 AND C39

CIRRUS LOGIC, Inc.
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Fremont, California 94538

CL-GD542X EVALUATION BOARD (MCA)

SIZE B | FSCM NO | DWG NO FILTER, IREF & MONITOR INTERFACES | REV

September 18, 1992 | SCALE | SHEET 5 OF 5

Item	Quantity	Reference	Part
1	2	C3,C1	220pf
2	23	C2,C8,C14,C16,C17,C18, C19,C20,C21,C22,C23,C24, C25,C26,C30,C31,C32,C33, C34,C35,C36,C37,C39	0.1uf
3	6	C4,C5,C6,C9,C10,C11	47pf
4	4	C7,C12,C15,C28	10uf
5	3	C13,C29,C38	2.2uF
6	4	D1,D2,D3,D4	1N4148
7	1	D5	TL431
8	3	ISO1,ISO2,ISO4	VIDISO
9	1	ISO5	MFILISO
10	1	ISO6	VFILISO
11	1	J1	13x2 PIN HEADER
12	1	J2	CON MC58
13	3	L1,L2,L3	Ferrite bead
14	1	P1	15P D-sub
15	1	Q1	2N3904
16	4	R1,R5,R8,R18	33
17	17	R2,R25,R26,R27,R28,R29, R30,R31,R32,R33,R34,R35, R36,R37,R38,R39,R40	100
18	3	R3,R4,R6	1K
19	1	R7	360
20	3	R9,R10,R11	150
21	2	R22,R12	1 OHM
22	2	R19,R13	75
23	7	R14,R15,R16,R17,R23,R24, R41	6.8K
24	1	U1	93C46
25	2	U2,U5	27256-15
26	2	U3,U6	74LS244
27	8	U7,U8,U9,U10,U11,U12,U13, U14	44256 SOJ
28	2	U15,U16	74LS373
29	1	U17	PAL22V10
30	1	U26	CL-GD542X
31	8	U27,U28,U29,U30,U31,U32, U33,U34	44256

Appendix B3

'486 VESA Local Bus

Application Note

'486 VESA® LOCAL BUS

1. INTRODUCTION

This application note discusses the logic design and layout of a complete VGA solution for a VESA VL-Bus '486 local bus adapter based on the CL-GD5424, CL-GD5426, and the CL-GD5428. The CL-GD5424/'26/'28/'29 share a common pinout; however, schematic differences will be found in the Video Memory and host CPU Bus interface. The CL-GD5424 is limited to a maximum of 1 Mbyte of DRAM, and the CL-GD5426/'28/'29 support a maximum of 2 Mbytes. The discussion covers the VL-Bus interface, BIOS, display memory, the Monitor/Video DAC interface, Integrated Clock, and hardware features.

A sample system schematic and bill of materials are included at the end of this appendix. The schematic and layout (Gerber Output) files are included with the manufacturing package, or these files can be downloaded from the Cirrus Logic Bulletin Board Service, (510) 440-9080 (refer to Appendix D9 for more information on the Cirrus Logic BBS). The schematic-capture program used for generating the sample adapter schematic is ORCAD SDT 4.10. The manufacturing package consists of all the documentation, software, firmware, working files, and sample components necessary for evaluating the CL-GD5424/'26/'28/'29 in a local bus adapter implementation.

2. '486 LOCAL BUS INTERFACE

The CL-GD5424/'26/'28/'29 is designed to interface directly with '386SX/DX and '486SX/DX CPUs with a minimal of glue logic. Configuration Resistor R24 (pull-down resistor on MD21) is required if the CL-GD5424/'26/'28/'29 is to operate in VESA Local Bus mode. The CL-GD5424/'26/'28/'29 connects directly to the CPU address, data and control lines, except for glue logic required for generating control signals missing from the local bus connector and word-steering logic for 32-bit systems. Two possible local bus configurations are discussed in the following sections: Motherboard and VL-Bus adapter.

2.1 Motherboard '486 Local Bus Interface

In a motherboard implementation, the CL-GD5424/'26/'28/'29 interfaces directly to the CPU. In 32-bit systems, no complicated word-steering logic is required if the BS16# line from the CL-GD5424/'26/'28/'29 is connected directly to the CPU. BS16# will cause the CPU to run multiple bus cycles to complete a data transaction with the CL-GD5424/'26/'28/'29. Four sets of octal transceivers — U16, U17, U18, and U19 — are used for interfacing the 32-bit CPU with the 16-bit CL-GD5424/'26/'28/'29. In a '486 design, the EEPROM Control pins become Word-steering Control signals (OEL# and OEH#) for the octal transceivers.

2.2 VESA® VL-Bus '486 Local Bus Interface

The VESA VL-Bus specification is the more stable of the possible local bus adapter card implementations. It is rapidly becoming a standard bus interface, and provides all of the local bus control signals required by the CL-GD5424/'26/'28/'29 except for UADDR#. This signal is a simple decode of ADR24 and ADR25, indicating that the current address is in the valid Video Memory (lower 64-Mbyte address range). The VL-Bus provides a 1x clock that connects directly to the CL-GD5424/'26/'28/'29 CLK1X pin. For a '486 implementation, the RDYRTN# and RESET pins on the CL-GD5424/'26/'28/'29 connect directly to the VL-Bus RDYRTN# pin.

The active-high RESET DRV signal needs to be conditioned by an R/C network (R2 and C19) to filter out any possible noise or glitches, and is connected to the RESET pin. Holding this signal high will disable CL-GD5424/'26/'28/'29.

The 14.31818-MHz reference signal required by the integrated Frequency Synthesizer is obtained from either the unbuffered local bus OSC input or an optional 14.3-MHz crystal. An optional high-pass filter (C42/R42) can be used to filter a noisy reference input.

3. BIOS

For a motherboard implementation, it is assumed that the BIOS is E000:0 (i.e., it is linked into the main system BIOS). For adapter card applications, the BIOS EPROM support logic consists of one EPROM (U20) and one octal bi-directional buffer (U21). In adapter Local Bus configuration, the BIOS EPROM interfaces directly to the ISA Bus Address, Data Bus, and SMEMRD signal. The CL-GD5424/'26/'28/'29 generates the appropriate EPROM Enable (EROM#) signal, which must be qualified with SMEMRD# (U22).

4. DISPLAY MEMORY

The display memory, as shown in the included schematics for the CL-GD5424/'26/'28/'29, can be configured for 1 or 2 Mbytes of memory (the schematics show two 256K x 16 SOJ packages for the first 1 Mbyte of memory used by either CL-GD5424, CL-GD5426, or CL-GD5428; the other 256K x 4 DIP package DRAMs are the optional 1-Mbyte upgrade option for the CL-GD5426/'28/'29). The schematics must be redrawn to support different DRAM configurations, such as symmetric or asymmetric, SOJ or DIP, and 256K x 4, 512K x 8, or 256K x 16. Refer to the DRAM configuration table in Appendix B7 for an overview of all the possible memory types and their connection to the CL-GD5424/'26/'28/'29.

The allowable DRAM types with the optimum t_{RAC} time for a specific Memory Clock (MCLK) can also be determined from Appendix B7. The application note describes the DRAM timings expected from each Memory Clock selection. The Memory Clock frequency is selected by R16 and R17, as shown in the DRAM timing options found in the schematic. Resistor R23 is used for choosing high-performance or normal MCLK RAS cycles. Refer to Appendix B9 for an explanation of the various configuration settings possible.

5. MONITOR/VIDEO DAC INTERFACE

The integrated Video DAC requires an external current-reference source (IREF) consisting of Q1, D5, and the associated R/C components shown on the schematic. This is an inexpensive IREF circuit that does not require a negative-voltage source. This circuit can easily be replaced with any one of various current-reference circuits based on an LM337, LM334, LP2951, or LM317, as long as the nominal IREF current drawn through the IREF pin is 6.7 mA. The IREF current determines the full-scale output voltage of the Video DAC, and therefore determines the brightness of the displayed image.

The analog Red, Green, and Blue (RGB) lines going from the CL-GD5424/'26/'28/'29 to the monitor interface connector (P1) have standard PI-filter circuits to reduce EMI and noise for FCC Class B compliance. The analog outputs are capable of directly driving a singly-terminated 75-Ω load to a peak-white amplitude of 0.7V. The 150-Ω pull-down resistors on the RGB lines correspond to an effective DAC output loading of 50 ohms. Each RGB analog output should have a source-load resistor located as close as possible to the CL-GD5424/'26/'28/'29 to minimize reflections.

6. INTEGRATED CLOCK

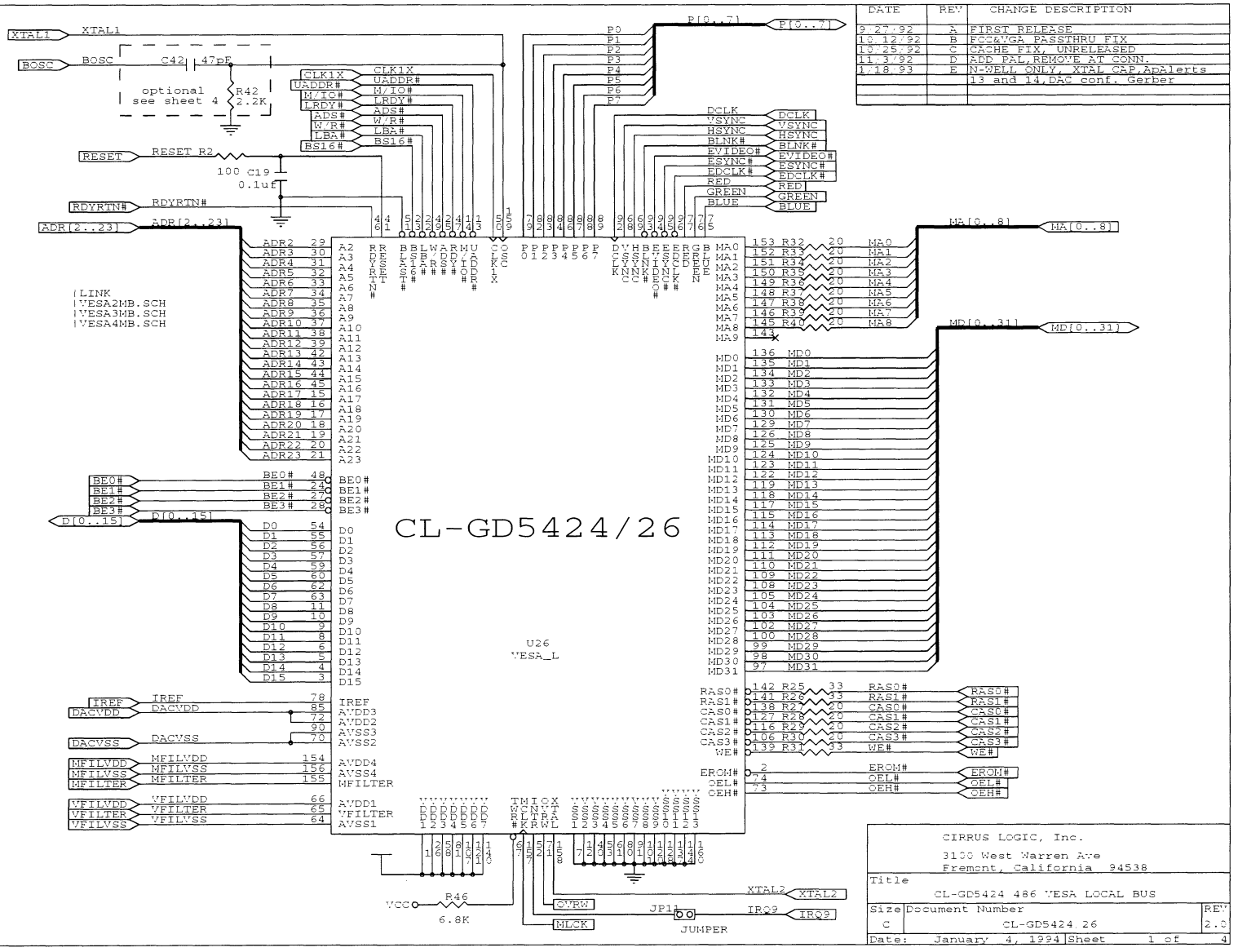
The integrated dual-clock synthesizer uses the 14.31818-MHz clock from the local bus as a reference for generating the Video and Memory Clocks. This reference clock can be replaced by a 14.31818-MHz series-resonant crystal by disconnecting the trace to the local bus and connecting the crystal across pins 158 and 159 of the CL-GD5424/'26/'28/'29.

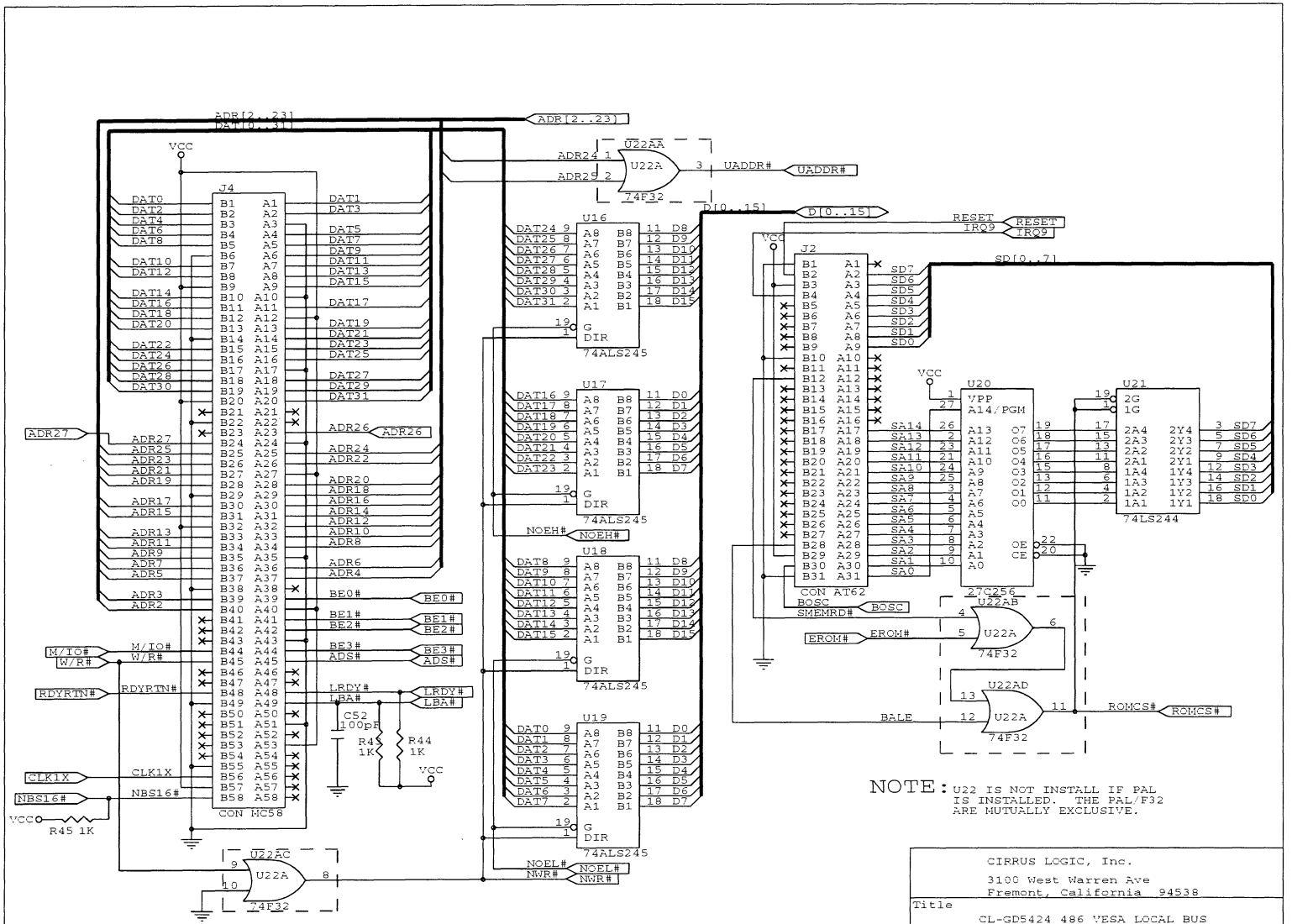
The internal dual-clock synthesizer requires two external loop-filter circuits, one for the Video Clock and the other for the Memory Clock. The Memory Clock filter consists of R19, C29, and C25. The Video Clock filter consists of R13, C13, and C17. The VFILTER circuit has capacitor components C38, C39, C13, and C17. Refer to Appendix B17 for a description of capacitors to use. For example, C38 and C39 are installed for N-WELL devices and C13 and C17 are installed for P-WELL devices. Careful board layout will guarantee optimal operation. Refer to Appendix B12 for more information regarding P-WELL and N-WELL configurations.

7. HARDWARE FEATURES

The '486 local bus schematic shows that an external EEPROM for storing monitor timing options is not supported because its control signals are used for word steering. The external EEPROM is supported in '386SX/DX local bus systems. Choosing not to install an EEPROM will not affect the operation of the adapter board, but it will require the execution of a configuration program from within the AUTOEXEC.BAT file.

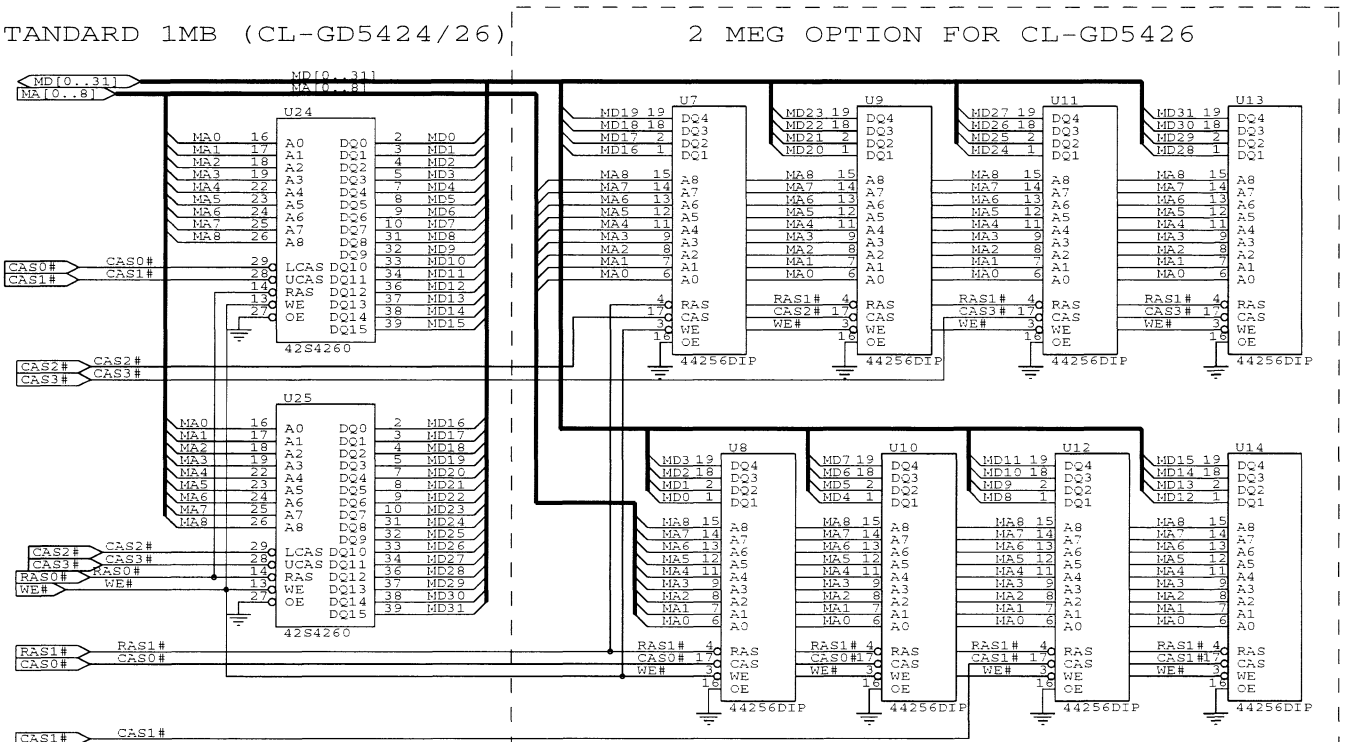
Adding J1 will provide a VESA-compliant VGA passthrough connector for transferring pixel data to or from the internal Palette DAC. The 13-pin-by-2-row connector is a less costly alternative than the IBM version, which requires a routing of the printed circuit board. Choosing not to install the connector will not affect the operation of the adapter board.


CL-GD5424/26
U26
VESA_L
DATE	REV	CHANGE DESCRIPTION
9.27.92	A	FIRST RELEASE
10.12.92	B	FCC&WGA PASSTHRU FIX
10.25.92	C	CACHE FIX, UNRELEASED
11.3.92	D	ADD PAL,REMOVE AT CONN.
1.18.93	E	N-WELL ONLY, XTAL CAP,APAlerts 13 and 14,DAC conf. Gerber
CIRRUS LOGIC, Inc.
3100 West Warren Ave
Fremont, California 94538
Title
CL-GD5424 486 VESA LOCAL BUS
Size C
Document Number CL-GD5424.26
REV 2.0
Date: January 4, 1994
Sheet 1 of 4



NOTE: U22 IS NOT INSTALL IF PAL IS INSTALLED. THE PAL/F32 ARE MUTUALLY EXCLUSIVE.

CIRRUS LOGIC, Inc. 3100 West Warren Ave Fremont, California 94538		
Title: CL-GD5424 486 VESA LOCAL BUS		
Size: C	Document Number: BUS INTERFACE	REV: 2.0
Date: January 19, 1993	Sheet 2 of 4	



DRAM TIMING OPTIONS

	MD26	MD25	MCLK
R16 6.8K MD25 MCLK S0	0	0	50.11MHz
	0	1	44.74MHz
R17 6.8K MD26 MCLK S1	1	0	41.16MHz
	1	1	37.58MHz

R23 6.8K MD27 MCLK SPEED — MD27: 0 = MCLK > 50Mhz; 1 = MCLK <= 50Mhz

R41 6.8K MD28 Multiple CAS

NOTE: DRAM SPEED DEPENDS ON THE DRAM TIMING OPTIONS
REFER TO APP NOTE B7:MEMORY CONSIDERATIONS

LOCAL BUS CONFIG.

R24 6.8K MD21 VESA VL Bus Config.

DAC SHADOW/DISABLE

R21 6.8K JP2 MD16 DAC SHADOW ENABLE

DAC Shadow
Note: Shadow only for 5426 rev AC
Internal DAC disable for 5424 rev AE

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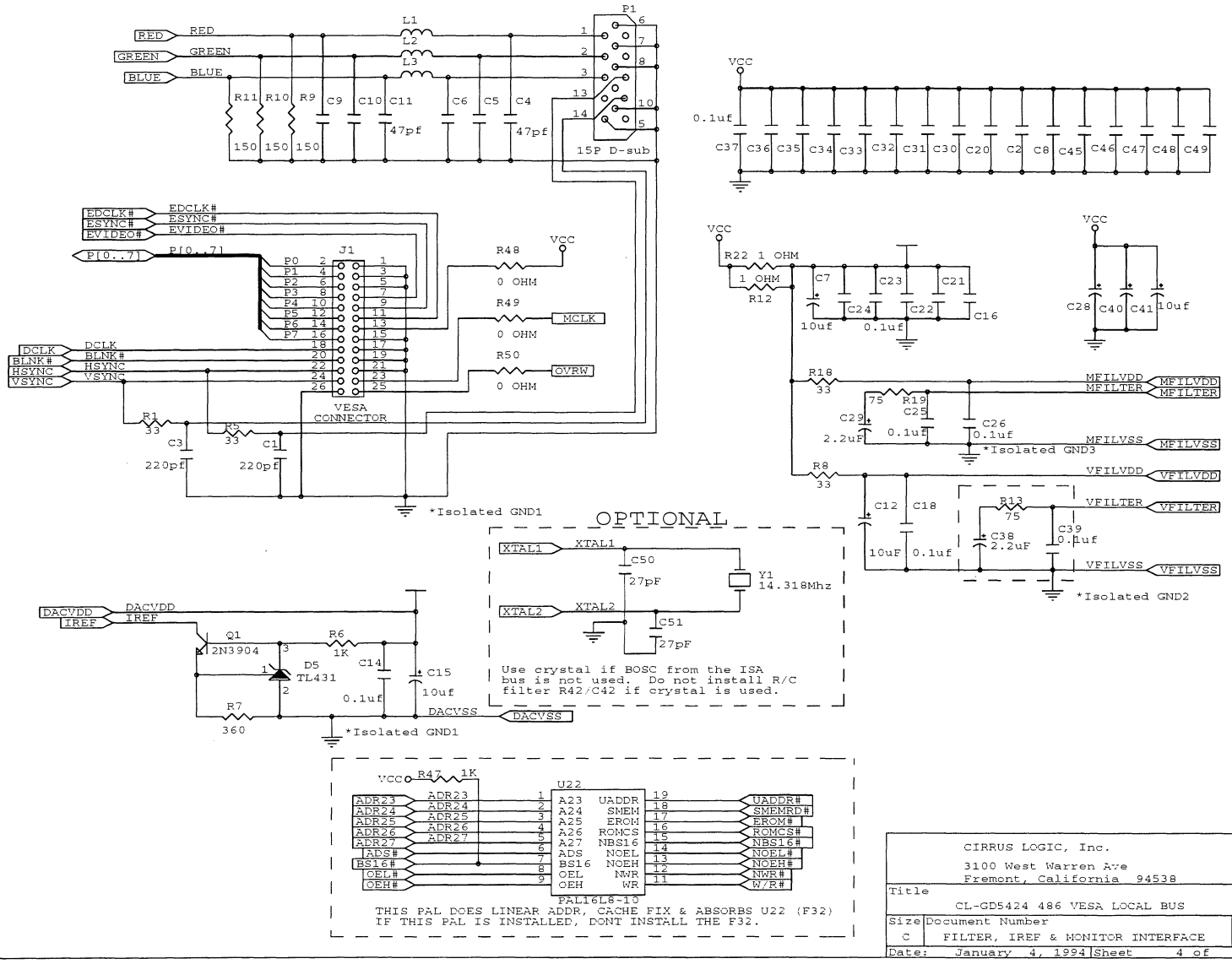
Fremont, California 94538

Title: CL-GD5424 486 VESA LOCAL BUS

Size	Document Number	REV
C	TOTAL 2Mb Memory	1.5
Date: January 19, 1993	Sheet 3 of 4	



CIRRUS LOGIC, Inc.
3100 West Warren Ave
Fremont, California 94538

Title	CL-GD5424 486 VESA LOCAL BUS	
Size: C	Document Number: FILTER, IREF & MONITOR INTERFACE	REV: 1.8
Date: January 4, 1994	Sheet 4 of 4	

Item	Quantity	Reference	Part
1	2	C1,C3	220PF
2	27	C2,C8,C14,C16,C18,C19, C20,C21,C22,C23,C24,C25, C26,C30,C31,C32,C33,C34, C35,C36,C37,C39,C45,C46, C47,C48,C49	0.1UF
3	7	C4,C5,C6,C9,C10,C11,C42	47PF
4	6	C7,C12,C15,C28,C40,C41	10UF
5	2	C29,C38	2.2UF
6	2	C50,C51	27PF
7	1	C52	100PF
8	1	D5	TL431
9	1	JP2	DAC SHADOW
10	1	JP11	JUMPER
11	1	J1	13X2 PIN HEADER
12	1	J2	CON AT62
13	1	J4	CON MC58
14	3	L1,L2,L3	FERRITE BEAD
15	1	P1	15P D-SUB
16	1	Q1	2N3904
17	7	R1,R5,R8,R18,R25,R26,R31	33
18	1	R2	100
19	5	R6,R43,R44,R45,R47	1K
20	1	R7	360
21	3	R9,R10,R11	150
22	2	R12,R22	1 OHM
23	2	R13,R19	75
24	7	R16,R17,R21,R23,R24,R41, R46	6.8K
25	13	R27,R28,R29,R30,R32,R33, R34,R35,R36,R37,R38,R39, R40	20
26	1	R42	2.2K
27	3	R48,R49,R50	0 OHM
28	8	U7,U8,U9,U10,U11,U12,U13, U14	44256DIP
29	4	U16,U17,U18,U19	74ALS245
30	1	U20	27C256
31	1	U21	74LS244
32	1	U22	PAL16L8-10
33	1	U22A	74F32
34	2	U24,U25	42S4260
35	1	U26	VESA_L
36	1	Y1	14.318MHZ

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Appendix B4

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Appendix B5

CL-GD5420-75QC-B VGA Controller

Application Note

CL-GD5420-75QC-B VGA CONTROLLER

1. OVERVIEW

The CL-GD5420-75QC-B video controller is a highly cost-effective 1-Mbyte VGA controller. Incorporating a built-in True Color palette DAC, dual-programmable Clock Synthesizer, and system bus and feature connector interface support, the CL-GD5420-75QC-B requires only DRAMs to complete a video system. Optimized DRAM timing, 32-bit memory interface, and an advanced Write Buffer provides high-performance memory access. A hardware Graphics Cursor improves the performance and appearance of graphical user interfaces such as Microsoft Windows. The CL-GD5420-75QC-B is pin-to-pin compatible with the CL-GD542X product family.

2. FEATURES

- Full IBM VGA-compatibility in a 160-pin plastic quad flat pack (PQFP) package.
- Built-in True Color palette DAC. The video outputs connect directly to analog displays.
- Built-in monitor-type detection circuit.
- Programmable internal memory clock.
- Programmable internal video clocks at up to 75 MHz.
- Connects directly to the MicroChannel or PC/XT/AT system bus.
- Supports 16-bit data for I/O and BIOS ROM.
- Supports 32-bit display memory.
- Supports 1-Mbyte display memory.
- Choice of two flexible DRAM timings.
- Write cycles to display memory are optimized by combining a Memory Write Buffer and zero-wait-state (AT Bus) request capability.
- Internal asynchronous display data FIFO allows the system optimum access to memory.
- Supports EEPROM for (switchless) configuration data.
- 132-column A.N. (Alphanumeric mode) on all monitors.
- 256-color Graphics mode at 1024 x 768 at 44 Hz interlace (70-ns DRAMs).
- Pinscan on the pads and signature analysis.
- Graphics Cursor; 32 x 32 pixel, Windows-compatible.

DRAM Support *(Refer to Appendix B7 for more information)*

Two, 256K x 4; 256K bytes
Four, 256K x 4; 512K bytes
Eight, 256K x 4; 1 Mbyte
One, 512K x 8; 512K bytes
Two, 512K x 8; 1 Mbyte
One, 256K x 16; 512K bytes (two WE-type: asymmetric or symmetric)
Two, 256K x 16; 1 Mbyte (two WE-type: symmetric only)

Standard RAS Timing

RAS high: 2.5 MCLK MIN
RAS low: 3.5 MCLK MIN
CAS cycle: 2 MCLK
Use MCLK = 37.5 for 80 ns, 41 or 45 MHz for 70 ns

Extended RAS Timing

RAS high: 3 MCLK MIN
RAS low: 4 MCLK MIN
CAS cycle: 2 MCLK
Use MCLK = 45 MHz for 80 ns, 50 MHz for 70 ns

MCLK Options:

Power-on default values are:

CF(10)	CF(9)	MCLK value
0	0	50.11363 MHz
0	1	44.74431 MHz
1	0	41.16477 MHz
1	1	37.58523 MHz

To program the MCLK, use the extended Sequencer register (SR:1F). Refer to Appendix B8.

2.1 Video Clock Support

All four VCLK values are programmable, the power-on default values are:

VCLK0 = 25.1802 MHz (Standard VGA graphics)
VCLK1 = 28.3251 MHz (Standard VGA text)
VCLK2 = 41.1648 MHz (132-column text, PS/2 monitors)
VCLK3 = 36.0818 MHz (800 x 600, 56 Hz)

Other available frequencies (VCLK3):

31.193 (640 x 480, 72 Hz), 50.113 (800 x 600, 72 Hz)
39.992 (800 x 600, 60 Hz), 64.982 (1024 x 768, 60-Hz non-interlaced)
44.907 (1024 x 768, interlaced), 75.169 (1024 x 768, 70-Hz non-interlaced)

NOTE: Only those frequencies listed above will be guaranteed by testing. All other intermediate frequencies will not be tested.

The following register bits have been added to CL-GD5420-75QC-B to support the above listed features:

1. SRF[4] is no longer reserved. It is used to set 32-bit data path (1-Mbyte memory).
2. SR12[7] — Overscan Color Protect. This bit is not available in CL-GD5420.
3. SR1F[5:0] — Used for the MCLK frequency. The CL-GD5420 does not have programmable memory clock.
4. The Hidden DAC register is located at 3C6.

Refer to Chapters 4 - 9 for details on above-mentioned registers.

Appendix B6

True Color Modes
Application Note

TRUE COLOR MODES

1. INTRODUCTION

Each video controller in the CL-GD542X family has a built-in palette DAC. The CL-GD5420 has an industry-standard palette DAC that provides 256 simultaneous colors out of a palette of 256K on the display screen. The CL-GD5422/'24/'26/'28 have a True Color Multi-mode palette DAC that supports the following modes — useful in multimedia applications:

- 8 bit-per-pixel (VGA-standard 256-color Palette mode)
- 15 bit-per-pixel (32K color, 5-5-5 TARGA™ mode)
- 16 bit-per-pixel (64K color, 5-6-5 XGA™ mode)
- 24 bit-per-pixel (16.8-million color, True Color mode)
- Mix mode: 32K (5-5-5 mode) colors and 256 colors (standard VGA mode)

CL-GD5428/'29 support 8-bit RGB (3-3-2) and 8-bit grayscale.

2. PROGRAMMING FOR A TRUE COLOR MULTI-MODE PALETTE DAC

The Hidden DAC register (I/O Port 3C6H) is used to enable Extended Color modes. At reset, this register is loaded with 00H, and the palette DAC is programmed in a compatible mode. In this mode, the palette DAC is functionally equivalent to the industry-standard Brooktree® BT476 RAMDAC™. By writing code to the Hidden DAC register, the palette DAC can be programmed in one of the modes mentioned above.

The following method is used to write to the Hidden DAC register:

Step 1: Read from the Pixel Mask register (3C6H) four times in succession. No other read/writes should be directed to that address.

Step 2: After the fourth read, the Pixel Mask register will point to the Hidden DAC register. At this point, the Hidden DAC register can be programmed by writing a code to it at Port 3C6H. Any other read from/write to any address other than the Pixel Mask register will reset an internal counter to a '0' and must be preceded by Step 1 again.

Table B6–1. Extended Mode Select

MSB 7	6	5	4	3	2	1	LSB 0	Hex	Function
1	1	1/0	0	0	0	0	0	E0/C0	5-5-5 mode with 32K colors
1	1	1/0	1	0	0	0	0	F0/D0	5-5-5 and 256-color Mix mode
1	1	X	0	0	0	0	1	E1/C0	5-6-5 mode with 64K colors
1	1	X	0	0	1	0	1	E5/C0	8-8-8 mode with 16.8-million colors
1	1	X	0	0	1	1	X	C6	DAC power-down *(CL-GD5429 only)*

Table B6–1. Extended Mode Select *(cont.)*

MSB 7	6	5	4	3	2	1	LSB 0	Hex	Function
1	1	X	0	1	0	0	0	C8	8-bit Gray Scale *(CL-GD5428/'29 only)*
1	1	X	0	1	0	0	1	C9	3-3-2 mode *(CL-GD5428/'29 only)*

NOTE: See the Hidden DAC register (Section 9.51) description.
bit 5: Clocking mode 1 = 0
Clocking mode 2 = 1
Use Clocking mode 1 *only* when using a video overlay feature.

2.1 5-5-5 Mode with 32K Colors

This mode supports the industry-standard 5-5-5 RGB mode with 32,768 colors. Each pixel is represented by 15 bits containing five bits of Red, Green, and Blue color information. The input sequence for each pixel is low byte first, followed by high byte by using the Clocking mode 1 or 2. The first low byte will be taken on the first rising edge of clock occurring after BLANK* has gone inactive (high). All subsequent bytes are clocked in on the rising edge of clock. The CLUT is ignored in this mode.

Table B6–2. Pixel Data Format in 5-5-5 Mode

MSB HIGH BYTE								LOW BYTE							LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	4	3	2	1	0	4	3	2	1	0	4	3	2	1	0
X	RED					GREEN					BLUE				

2.2 Mix Mode

If bit 4 of the Hidden DAC register is set to a '1', the pixel data bit 15 will be used to select between 5-5-5 RGB mode and use of the standard palette DAC on a pixel-by-pixel basis.

Table B6–3. Pixel Data Format in Mix Mode

MSB HIGH BYTE								LOW BYTE							LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	4	3	2	1	0	4	3	2	1	0	4	3	2	1	0
555	RED					GREEN					BLUE				

Table B6–4. PLT: Palette Lookup Table

MSB HIGH BYTE								LOW BYTE							LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	X	X	X	X	X	X	X	7	6	5	4	3	2	1	0
PLT	IGNORED							Palette DAC LUT INPUT							

2.3 5-6-5 Mode with 64K Colors

This mode supports the XGA™ 5-6-5 RGB mode with 65,536 colors. Each pixel is represented by 16 bits containing 5 bits of Red, 6 bits of Green, and 5 bits of Blue color information. The input sequence for each pixel is low byte first, followed by high byte by using the Clocking mode 1 or 2. The first low byte will be taken on the first rising edge of clock occurring when BLANK* has gone inactive (high). All subsequent bytes are clocked in on the rising edge of clock. The CLUT is ignored in this mode.

Table B6–5. Pixel Data Format in 5-6-5 Mode with 64K Colors

MSB HIGH BYTE								LOW BYTE							LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
4	3	2	1	0	5	4	3	2	1	0	4	3	2	1	0
RED					GREEN						BLUE				

2.4 8-8-8 Mode with 16.8 Million Colors

This mode supports the industry-standard 8-8-8 RGB mode with 16,777,216 colors. Each pixel is represented by 24 bits containing 1 byte each of Red, Green, and Blue color information. The input sequence for each pixel is low byte (Blue) first, followed by middle (Green) byte, followed by high (Red) byte by using the Clocking mode 1 or 2. The first low byte will be taken on the first rising edge of clock occurring when BLANK* has gone inactive (high). All subsequent bytes are clocked in on the rising edge of clock. The palette LUT is ignored in this mode.

Table B6–6. Pixel Data Format in 8-8-8 Mode with 16.8M Colors

MSB HIGH BYTE								MIDDLE BYTE								LOW BYTE							LSB
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
RED								GREEN								BLUE							

2.5 3-3-2 Mode with 256 Colors (CL-GD5428/'29 Only)

This mode supports the industry standard 3-3-2 RGB mode with 256 colors. Each pixel is represented by 8 bits containing 3 bits of Red color, 3 bits of Green color, and 2 bits of Blue color. The palette LUT is ignored in this mode.

Table B6–7. Pixel Data Format in 3-3-2 Mode with 256 Colors

MSB EACH BYTE							
7	6	5	4	3	2	1	0
RED			GREEN			BLUE	

2.6 8-bit Grayscale Mode (CL-GD5428/'29 Only)

This mode supports the industry standard of 8 bit grayscale with 256 shades of gray. Each pixel is represented by 8 bits. The palette LUT is ignored in the mode.

Table B6–8. Pixel Data Format in 8-bit Gray Scale

MSB EACH BYTE							
7	6	5	4	3	2	1	0
GRAYSCALE							

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Appendix B7

Memory Configurations
Application Note

MEMORY CONFIGURATIONS

1. INTRODUCTION

The CL-GD542X supports many display memory configurations, from 256K bytes to 2 Mbytes, using DRAMs that are organized by:

- 256K x 4
- 512K x 8
- 256K x 16 — dual-WE* or dual-CAS*

For 256K x 4 DRAM configuration, the total display memory can be expanded from 256K bytes to 512/1024K bytes by adding devices without changing any jumpers. For 256K x 16 DRAM configuration, the total display memory can be expanded from 512K bytes to 2 Mbytes. For 512K x 8 DRAMs, the total display memory can be expanded from 1 to 2 Mbytes. Note that a few signals change functions according to the device organization that is used.

For optimum performance, multiple-CAS* configurations should be chosen over multiple-WE* configurations.

Table B7–1. CL-GD542X Memory Configurations

Memory Configuration	CL-GD5420	CL-GD5422	CL-GD5424	CL-GD5426/'28/'29
256K byte: Two, 256K x 4	X			
512K byte: Four, 256K x 4	X	X	X	X
512K byte: One, 256K x 16	X[a]	X	X	X
1 Mbyte: Two, 256K x 16	X[b]	X	X	X
1 Mbyte: Two, 512K x 8	X			
1 Mbyte: Eight, 256K x 4	X[c]	X	X	X
2 Mbyte[d]: Four, 512K x 8				X
2 Mbyte[d]: Four, 256K x 16				X
2 Mbyte[d]: Two, 256K x 16 and eight, 256K x 4				X

a. The CL-GD5420 can support one 256K x 16 (512K bytes) only with a dual-WE* DRAM.
b. CL-GD5420 Revision 'B' only with dual-WE* symmetric DRAMs.
c. CL-GD5420 Revision 'B' only.
d. For 2 Mbyte modes, see the description of SRF[7].

The following tables indicate, for each case, how each device must be connected.

Table B7–2. *256K x 4 DRAMs*: 256K byte Display Memory (CL-GD5420 only)

Memory Device	One	Two
OE*	OE*	OE*
WE*	WE3*	WE3*
RAS*	RAS*	RAS*
CAS*	CAS*	CAS*
ADDR	MA[8:0]	MA[8:0]
DATA	MD[27:24]	MD[31:28]
PLANE	0, 1, 2, 3	0, 1, 2, 3

Table B7–3. *256K x 4 DRAMs*: 512K byte Display Memory

Memory Device	One	Two	Three	Four
OE*	OE*	OE*	OE*	OE*
WE*	WE3*	WE3*	WE2*	WE2*
RAS*	RAS*	RAS*	RAS*	RAS*
CAS*	CAS*	CAS*	CAS*	CAS*
ADDR	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]
DATA	MD[27:24]	MD[31:28]	MD[19:16]	MD[23:20]
PLANE	1, 3		0, 2	

Table B7–4. *512K x 8 DRAMs*: 1-Mbyte Display Memory (CL-GD5420 only)

Memory Device	One	Two
OE*	OE*	OE*
WE*	WE2*	WE3*
RAS*	RAS*	RAS*
CAS*	CAS*	CAS*
ADDR	MA[9:0]	MA[9:0]
DATA	MD[23:16]	MD[31:24]
PLANE	0, 2	1, 3

Table B7–5. *256K x 4 DRAMs*: 1-Mbyte Display Memory, Multiple WE*

Memory Device	One	Two	Three	Four	Five	Six	Seven	Eight
OE*	OE*	OE*	OE*	OE*	OE*	OE*	OE*	OE*
WE*	WE2*	WE2*	WE3*	WE3*	WE0*	WE0*	WE1*	WE1*
RAS*	RAS*	RAS*	RAS*	RAS*	RAS*	RAS*	RAS*	RAS*
CAS*	CAS*	CAS*	CAS*	CAS*	CAS*	CAS*	CAS*	CAS*
ADDR	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]
DATA	MD[19:16]	MD[23:20]	MD[27:24]	MD[31:28]	MD[3:0]	MD[7:4]	MD[11:8]	MD[15:12]
PLANE	2		3		0		1	

Table B7–6. *256K x 4 DRAMs*: 1-Mbyte Display Memory, Multiple CAS*

Memory Device	One	Two	Three	Four	Five	Six	Seven	Eight
OE*	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND	GROUND
WE*	CAS*	CAS*	CAS*	CAS*	CAS*	CAS*	CAS*	CAS*
RAS*	RAS*	RAS*	RAS*	RAS*	RAS*	RAS*	RAS*	RAS*
CAS*	WE2*	WE2*	WE3*	WE3*	WE0*	WE0*	WE1*	WE1*
ADDR	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]
DATA	MD[19:16]	MD[23:20]	MD[27:24]	MD[31:28]	MD[3:0]	MD[7:4]	MD[11:8]	MD[15:12]
PLANE	2		3		0		1	

Table B7–7. *256K x 16 DRAMs*: 512K byte Display Memory — Two-WE* Type

Memory Device	One (symmetric)	One (asymmetric)
LWE*	WE2*	WE2*
UWE*	WE3*	WE3*
OE*	OE*	OE*
RAS*	RAS*	RAS*
CAS*	CAS*	CAS*
ADDR[0]	MA[0]	MA[8]
ADDR[7:1]	MA[7:1]	MA[7:1]
ADDR[8]	MA[8]	MA[0]
ADDR[9]	not valid	MA[9]
DATA	MD[31:16]	MD[31:16]
PLANE	0, 1, 2, 3	0, 1, 2, 3

Table B7–8. *256K x 16 DRAMs*: 512K byte Display Memory — Two-CAS Type

Memory Device	One (symmetric)	One (asymmetric)
LCAS*	WE2*[a]	WE2*[a]
UCAS*	WE3*[b]	WE3*[b]
OE*	GND	GND
RAS*	RAS*	RAS*
WE*	CAS*[c]	CAS*[c]
ADDR[0]	MA[0]	MA[8]
ADDR[7:1]	MA[7:1]	MA[7:1]
ADDR[8]	MA[8]	MA[0]
ADDR[9]	not valid	MA[9]
DATA	MD[31:16]	MD[31:16]
PLANE	0, 1, 2, 3	0, 1, 2, 3

a. WE2* pin becomes CAS2* for dual-CAS 256K x 16 DRAM.
b. WE3* pin becomes CAS3* for dual-CAS 256K x 16 DRAM.
c. CAS* pin becomes WE* signal for dual-CAS 256K x 16 DRAM.

Table B7–9. *256K x 16 DRAMs*: 1-Mbyte Display Memory — Two-WE* Type

Memory Device	One (symmetric)	Two (symmetric)	One (asymmetric)	Two (asymmetric)
LWE*	WE2*	WE0*	WE2*	WE0*
UWE*	WE3*	WE1*	WE3*	WE1*
OE*	OE*	OE*	OE*	OE*
RAS*	RAS*	RAS*	RAS*	RAS*
CAS*	CAS*	CAS*	CAS*	CAS*
ADDR[0]	MA[0]	MA[0]	MA[8]	MA[8]
ADDR[7:1]	MA[7:1]	MA[7:1]	MA[7:1]	MA[7:1]
ADDR[8]	MA[8]	MA[8]	MA[0]	MA[0]
ADDR[9]	not valid	not valid	MA[9]	MA[9]
DATA	MD[31:16]	MD[15:0]	MD[31:16]	MD[15:0]
PLANE	2, 3	0, 1	2, 3	0, 1

Table B7–10. *256K x 16 DRAMs*: 1-Mbyte Display Memory — Two-CAS Type

Memory Device	One (symmetric)	Two (symmetric)	One (asymmetric)	Two (asymmetric)
LCAS*	WE2* [b]	WE0* [a]	WE2* [b]	WE0* [a]
UCAS*	WE3* [d]	WE1* [c]	WE3* [d]	WE1* [c]
OE*	GND	GND	GND	GND
RAS*	RAS*	RAS*	RAS*	RAS*
WE*	CAS* [e]	CAS* [e]	CAS* [e]	CAS* [e]
ADDR[0]	MA[0]	MA[0]	MA[8]	MA[8]
ADDR[7:1]	MA[7:1]	MA[7:1]	MA[7:1]	MA[7:1]
ADDR[8]	MA[8]	MA[8]	MA[0]	MA[0]
ADDR[9]	not valid	not valid	MA[9]	MA[9]
DATA	MD[31:16]	MD[15:0]	MD[31:16]	MD[15:0]
PLANE	2, 3	0, 1	2, 3	0, 1

a. WE0* pin becomes CAS0* for dual-CAS 256K x 16 DRAM.
b. WE2* pin becomes CAS2* for dual-CAS 256K x 16 DRAM.
c. WE1* pin becomes CAS1* for dual-CAS 256K x 16 DRAM.
d. WE3* pin becomes CAS3* for dual-CAS 256K x 16 DRAM.
e. CAS* pin becomes WE* signal for dual-CAS 256K x 16 DRAM.

Table B7–11. *256K x 16 DRAMs*: 2-Mbyte Display Memory — Two-WE* Type (symmetric)

Memory Device	One (symmetric)	Two (symmetric)	Three (symmetric)	Four (symmetric)
LWE*	WE2*	WE0*	WE2*	WE0*
UWE*	WE3*	WE1*	WE3*	WE1*
OE*	OE*	OE*	OE*	OE*
RAS*	RAS*	RAS*	MA[9][a]	MA[9][a]
CAS*	CAS*	CAS*	CAS*	CAS*
ADDR[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]
DATA	MD[31:16]	MD[15:0]	MD[31:16]	MD[15:0]
PLANE	2, 3	0, 1	2, 3	0, 1

a. MA[9] pin becomes RAS1* for dual-WE* 256K x 16 DRAM (symmetric).

Table B7–12. *256K x 16 DRAMs*: 2-Mbyte Display Memory — Two-CAS* Type (symmetric)

Memory Device	One (symmetric)	Two (symmetric)	Three (symmetric)	Four (symmetric)
LCAS*	WE2*[b]	WE0*[a]	WE2*[b]	WE0*[a]
UCAS*	WE3*[d]	WE1*[c]	WE3*[d]	WE1*[c]
OE*	GND	GND	GND	GND
RAS*	RAS*	RAS*	OE*[e]	OE*[e]
WE*	CAS*[f]	CAS*[f]	CAS*[f]	CAS*[f]
ADDR[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]
DATA	MD[31:16]	MD[15:0]	MD[31:16]	MD[15:0]
PLANE	2, 3	0, 1	2, 3	0, 1

a. WE0* pin becomes CAS0* for dual-CAS 256K x 16 DRAM.
b. WE2* pin becomes CAS2* for dual-CAS 256K x 16 DRAM.
c. WE1* pin becomes CAS1* for dual-CAS 256K x 16 DRAM.
d. WE3* pin becomes CAS3* for dual-CAS 256K x 16 DRAM.
e. OE* pin becomes RAS1* signal for dual-CAS 256K x 16 DRAM.
f. CAS* pin becomes WE* signal for dual-CAS 256K x 16 DRAM.

Table B7–13. *256K x 16/256K x 4 DRAMs*: 2-Mbyte Display Memory — Two-CAS* Type (symmetric)

Devices	1 256 x 16	2 256 x 16	3 256 x 4	4 256 x 4	5 256 x 4	6 256 x 4	7 256 x 4	8 256 x 4	9 256 x 4	10 256 x 4
LCAS	WE0* [a]	WE2* [c]	–	–	–	–	–	–	–	–
VCAS	WE1* [b]	WE3* [d]	–	–	–	–	–	–	–	–
CAS	–	–	WE0*[a]	WE0*[a]	WE1* [b]	WE1* [b]	WE2* [c]	WE2* [c]	WE3* [d]	WE3* [d]
OE	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
RAS	RAS*	RAS*	OE* [e]	OE* [e]	OE* [e]	OE* [e]	OE* [e]	OE* [e]	OE* [e]	OE* [e]
WE	CAS*[f]	CAS* [f]	CAS* [f]	CAS* [f]	CAS* [f]	CAS* [f]	CAS* [f]	CAS* [f]	CAS* [f]	CAS* [f]
ADDR	8:0	8:0	8:0	8:0	8:0	8:0	8:0	8:0	8:0	8:0
DATA	15:0	31:16	3:0	7:4	11:8	15:12	16:14	23:20	27:24	31:28

a. WE0* pin becomes CAS0* for dual-CAS 256K x 16 DRAM.
b. WE1* pin becomes CAS1* for dual-CAS 256K x 16 DRAM.
c. WE2* pin becomes CAS2* for dual-CAS 256K x 16 DRAM.
d. WE3* pin becomes CAS3* for dual-CAS 256K x 16 DRAM.
e. OE* pin becomes RAS1* signal for dual-CAS 256K x 16 DRAM.
f. CAS* pin becomes WE* signal for dual-CAS 256K x 16 DRAM.

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Appendix B8

Clock Options

Application Note

CLOCK OPTIONS

1. INTRODUCTION

This application note discusses clock options available to CL-GD542X-based system designs.

2. MCLK — MEMORY CLOCK SELECTION

The Clock Synthesizer generates all the clocks needed for the memory timing (RAS*, CAS*, etc.) using an external reference clock, typically 14.31818 MHz. The Clock Synthesizer is a built-in feature of the CL-GD542X family.

The CL-GD5420 and the CL-GD5422 have four fixed memory clocks. At reset, data present on the Memory Data lines (MD26 and MD25) are loaded into the Configuration register, which is not accessible to software. Data can be presented via internal pull-up or external pull-down resistors. Typical values for an external pull-down resistor is 6.8 KΩ, and 250 KΩ for an internal pull-up resistor. A pull-down resistor will cause the corresponding Configuration bit to be a '0' and a '1' for pull-up resistor. Use the following table to select proper MCLK depending upon the type of DRAM used.

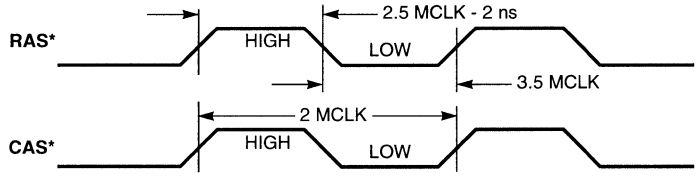
NOTE: A '0' corresponds to an external pull-down resistor (6.8 KΩ); a '1' corresponds to an internal pull-up resistor.

MD26	MD25	MCLK (MHz)
0	0	50.11363
0	1	44.74431
1	0	41.16477
1	1	37.58523

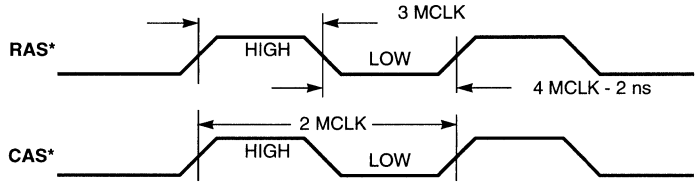
The CL-GD542X family supports two types of DRAM timing: standard and extended RAS* timing. A standard timing is used for generic DRAMs. Selection of DRAM timing can be made by setting the Configuration Register bit 12 (MD27). A pull-down resistor will cause the corresponding Configuration bit to be a '0' and a '1' for pull-up resistor; see the following table:

MD27	DRAM Timing Selection
0	Extended RAS* (7-MCLK RAS* cycle)
1	Standard RAS* (6-MCLK RAS* cycle)

Refer to Appendix B19, *DRAM Timing Calculations*, for determining which DRAMs can be used at a given MCLK frequency. In standard DRAM timing, the CAS* and RAS* cycle have the following parameters:



Refer to Appendix B19 (DRAM Timing Calculations) for determining which DRAMs can be used at a given MCLK frequency. In the extended DRAM timing, the CAS* and RAS* Cycles have the following parameters:



3. PROGRAMMABLE MCLK

The CL-GD5424/'26/'28/'29 have a programmable memory clock for higher performance. An extended Sequencer register (SR1F) is used for MCLK programming. The Sequencer registers are located at 3C4 (Index) and 3C5 (Data registers). The MCLK selected at RESET by MD25 and MD26 will be valid (see above description) until it gets overwritten by software.

The following values for the MCLK are set on RESET:

MCLK (MHz)	SR1F[5:0] (Hex)	SR1F[5:0] (Dec.)
37.585	15	21
41.165	17	23
44.744	19	25
50.114	1C	28

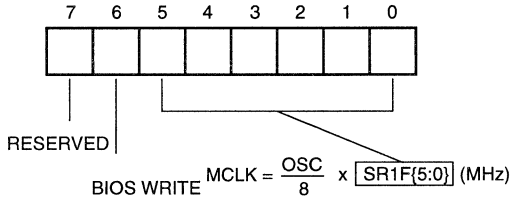
SR (3C4) Index 1F: Bits D5:0 are used to program a MCLK frequency.

NOTE: It is *extremely* important not to change this register after the BIOS sets it for a proper MCLK value.

The following formula is used to calculate the MCLK frequency:

I/O Address: 3C4 Index
3C5 Data Registers

Index: 1F



Valid range for SR1F[5:0] is from: $4 < SR:1F[5:0] < 28_d$.
OSC = 14.31818 MHz ± 0.01% with a duty cycle of 50 ± 10%.

For the CL-GD5429 only, the maximum value for SR1F[5:0] is 33 (decimal).

4. VCLK — VIDEO CLOCK PROGRAMMING

This clock is used to derive the Video Dot Clock (DCLK), VS (Vertical Sync), and HS (Horizontal Sync) timing for various SVGA modes. Video Clock (VCLKX) are generated internally using an external reference clock, typically 14.31818 MHz. There are four video clocks supported in the CL-GD542X family. All four VCLK values are programmable with following power-on default values:

- **VCLK0 = 25.1802 MHz (Standard VGA graphics)**
- **VCLK1 = 28.3251 MHz (Standard VGA text)**
- **VCLK2 = 41.1648 MHz (132-column text)**
- **VCLK3 = 36.082 MHz (Used for 800 x 600 Graphics Mode)**

For the CL-GD5420, the maximum VCLKX is up to 75 MHz. For CL-GD5422/'24/'26/'28, the maximum VCLKX is up to 80 MHz. For the CL-GD5429, the maximum VCLKX is 86 MHz. The maximum VCLK for a given MCLK frequency depends upon the following factors:

- Memory Data bus width: 8, 16, or 32 bits (for text modes, the 32-bit DRAM data width is the same performance as 16-bit data)
- **Display Mode**

  Standard VGA Text (dual font).

  Page Mode Text (single font, but higher VCLK possible, used for 132-column).

  All standard VGA Graphics modes: 2-, 4-, 16-color and 320 x 200 x 256-color modes.

  Super VGA 256-color modes.

16-bit-per-pixel modes (32K and 64K color).
24-bit-per-pixel modes (16.8 million colors).
Hardware limit of VCLK.

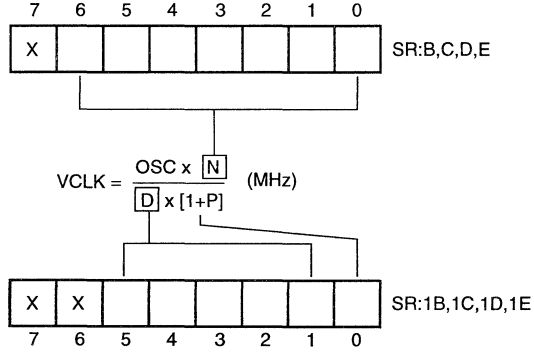
- For text modes, the DRAM-timing parameter of standard/high performance is important
- For text modes, the font width of 8 or 9 dots also determines the maximum VCLK
- The display FIFO depth also affects text mode maximum VCLKs

Eight extended Sequencer registers are used to program VCLKX. These registers are accessible only if all the Extended registers are unlocked (the Extended Registers are not lockable on the CL-GD5429). A Sequencer register (SR:6) must be loaded with 12h to unlock all CL-GD542X Extended registers. The following extended Sequencer registers are used to program the VCLKX:

Sequencer I/O Address = 3C4

SR:B = VCLK0 numerator value
SR:1B = VCLK0 denominator and post-scalar value
SR:C = VCLK1 numerator value
SR:1C = VCLK1 denominator and post-scalar value
SR:D = VCLK2 numerator value
SR:1D = VCLK2 denominator and post-scalar value
SR:E = VCLK3 numerator value
SR:1E = VCLK3 denominator and post-scalar value

The 7-bit Numerator (N), 5-bit Denominator (D), and 1-bit Post (P) for each Video Clock (VCLKX) determines its frequency according to the following formula:



The registers are read/write and preset with the following data by RESET: *i = B, C, D, E*

CLOCK	VCLK (MHz)	N	D	P (SR1i(0)	SRi (6:0)	SR1i (5:0)
VCLK0	25.225	74	21	1	$4A_h$	$2B_h$
VCLK1	28.325	91	23	1	$5B_h$	$2F_h$
VCLK2	41.165	69	24	0	45_h	30_h
VCLK3	36.082	126	25	1	$7E_h$	33_h

Other tested frequencies:

	31.499	66	15	1	42_h	$1F_h$
	39.992	81	29	0	51_h	$3A_h$
	44.907	85	29	0	55_h	36_h
	49.866	101	29	0	65_h	$3A_h$
	64.982	118	26	0	76_h	34_h
	72.163	126	25	0	$7E_h$	32_h
	74.999	110	21	0	$6E_h$	$2A_h$
	80.013	95	17	0	$5F_h$	22_h

4.1 Video Dot Clock (VCLKX) Selection

The Video Dot Clock is selected by a combination of Configuration Register bit CF(5), Miscellaneous Output register (I/O Port 3C2) bits 2:3, and Input EDCLK (pin 96). The Configuration register (CF14:0) cannot be accessed by software, and it is used to select the MCLK source. Bit 5 of this register can be set by an external pull-down resistor (6.8 KW) on MD20. If no pull-down resistor is installed on MD20, bit 5 of Configuration register will be set to a '1' by an internal pull-up resistor (250 KW).

Bit 5 (MD20) of Configuration register: MCLK (pin 157) source
0 = External, MCLK is configured as an input for test purposes.
1 = Internal, MCLK is configured to output the internally generated MCLK.

Following table is used to select VCLKX:

EDCLK (pin 96)	3C2: 3	3C2: 2	Dot Clock selected
1	0	0	VCLK0
1	0	1	VCLK1
1	1	0	VCLK2
1	1	1	VCLK3
0	1	X	DCLK Input to DAC and CRTC
0	0	X	DCLK to DAC only

4.2 Using MCLK as VCLK (CL-GD5428/'29 Only)

If the two synthesizers are programmed to frequencies which are very close, or are nearly harmonically related, there is a possibility that they will interfere with each other. This can result in a jitter on the screen. The solution to this problem is to simply shut down the VCLK synthesizer and use the MCLK synthesizer for both frequencies. This is controlled with SR1F[6] and SR1E[6] as indicated in the following table.

SR1F[6]	SR1E[6]	VCLK Source
0	x	VCLK (Normal Operation)
1	0	VCLK=MCLK
1	1	VCLK=MCLK/2

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Appendix B9

Configuration Notes

Application Note

CONFIGURATION NOTES

1. INTRODUCTION

This application note documents the Configuration register (CF15:0) of the CL-GD542X. An overview is provided that shows all the bits for each family member. Then the Configuration register is described individually for the CL-GD5420, the CL-GD5422, and CL-GD5424/'26/'28/'29.

CONFIGURATION REGISTER (CF15:0)

This 16-bit register configures the CL-GD542X into various modes of operation. Software *cannot* access this register. Data present on the Memory Data bus MD[31:16] is loaded into this register by power-on RESET. Data on the MD bus can be presented via internal pull-up or external pull-down resistors. Typical values for an external pull-down resistor is 6.8 KΩ, and 250 KΩ for an internal pull-up resistor. A pull-down resistor will cause the corresponding Configuration bit to be a '0' and a '1' for pull-up resistor. If no pull-down resistors are installed on the MD bus, this register is loaded with data FFFF at power-on RESET.

NOTE: A '0' corresponds to an external pull-down resistor (6.8 KΩ); a '1' corresponds to an internal pull-up resistor.

2. CONFIGURATION OVERVIEW

The following table may be used as an overview to the configuration register for all family members. It can be seen that considerable commonality exists.

Table B9–1. Configuration Overview

CF-	MD-	CL-GD5420	CL-GD5422	CL-GD5424/'26/'28	CL-GD5429
15	31	SR7[7]	Reserved	Reserved	MCLK Output pin source
14	30	SR7[6]	Reserved	Host bus configuration select [2]	
13	29	SR7[5]	Select asymmetric RAS*/CAS* addressing		
12	28	SR7[4]	Select multiple CAS* DRAM interface		
11	27	Select Extended RAS* timing			
10	26	Default MCLK select (CF10 and CF9)			
9	25				
8	24	Select 64K ROM BIOS			
7	23	Select MicroChannel host interface		Host bus configuration select [1]	
6	22	Select 16-bit ROM BIOS width (Enable MCS16*)			
5	21	Reserved		Host bus configuration select [0]	

Table B9–1. Configuration Overview *(cont.)*

CF-	MD-	CL-GD5420	CL-GD5422	CL-GD5424/'26/'28	CL-GD5429
4	20	Select MCLK pin to be input (Factory Testing only)			
3	19	46E9 Sleep	Reserved	VGA Sleep address select	
2	18	Reserved	Reserved	8514 DAC Address	PX2070 Address
1	17	Enable zero-wait-state BIOS			PX2070 Enable
0	16	Reserved	Reserved	DAC power-down	

3. CONFIGURATION NOTES FOR CL-GD5420

Table B9–2. CF15:0 for the CL-GD5420

Configuration Register															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MD 31	MD 30	MD 29	MD 28	MD 27	MD 26	MD 25	MD 24	MD 23	MD 22	MD 21	MD 20	MD 19	MD 18	MD 17	MD 16

CF15 : Latched input for optional configuration switch; readable at SR7, bit 7.
CF14 : Latched input for optional configuration switch; readable at SR7, bit 6.
CF13 : Latched input for optional configuration switch; readable at SR7, bit 5.
CF12 : Latched input for optional configuration switch; readable at SR7, bit 4.

CF11 : DRAM Timing Select
0 : Extended RAS (RAS high = 3 MCLK, RAS low = 4 MCLK)
1 : Standard RAS (RAS high = 2.5 MCLK, RAS low = 3.5 MCLK)

CF10 : MCLK Frequency Select bit 1 (MSB)
CF9 : MCLK Frequency Select bit 0 (LSB)

CF10	CF9	MCLK (MHz)
0	0	50.11363
0	1	44.74431
1	0	41.16477
1	1	37.58523

CF8 : ROM BIOS size select
0 : 64K at C0000 to CFFFF
1 : 32K at C0000 to C7FFF

CF7 : System (host) bus interface selection
0 : MicroChannel interface
1 : ISA (PC/XT/AT) bus interface

CF6 : VGA BIOS ROM select
0 : 16-bit BIOS ROM
1 : 8-bit BIOS ROM

CF5 : Reserved

CF4 : Memory Clock (MCLK) source select
0 : External supply, MCLK pin is configured as an input
1: Internally generated, MCLK pin is configured as an output

CF3 : Select VGA Enable Register Address (AT bus interface only)
0 : VGA Enable register is mapped into 46E9
1 : VGA Enable register is mapped into 46E8

(This bit changes the I/O Port Address of the VGA Enable register normally mapped into Port 46E8 for use in motherboard implementations of the CL-GD5420. This bit allows disabling the CL-GD5420 through Port 46E9 instead. Therefore, any VGA video adapters enabled by Port 46E8 will not conflict with the CL-GD5420. The BIOS must be configured for this option. This bit has no effect in a MicroChannel bus configuration because the VGA Enable register is 3C3h).

CF2 : Reserved

CF1 : Enable BIOS ROM zero-wait-state
0 : Enable Output ZWS* to be driven active accessing the BIOS ROM
1 : Output ZWS* remains high impedance when accessing the BIOS ROM

CF0 : Reserved

4. CONFIGURATION NOTES FOR CL-GD5422

Table B9–3. CF15:0 for the CL-GD5422

Configuration Register															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MD 31	MD 30	MD 29	MD 28	MD 27	MD 26	MD 25	MD 24	MD 23	MD 22	MD 21	MD 20	MD 19	MD 18	MD 17	MD 16

CF15: Reserved

CF14 :Reserved

CF13 : Select asymmetric RAS/CAS* addressing
0 : CAS* Address uses MA7:0, RAS* address uses MA[9:0]
1 : RAS* and CAS* Addresses are output on MA[8:0]

CF12 : Select multiple-CAS* or multiple-WE* DRAM Interface
0 : Multiple CAS* — CAS*[3:0] used with one WE*
1 : Multiple WE* — WE*[3:0] used with one CAS**

CF11 : DRAM Timing Select
0 : Extended RAS* (RAS* high = 3 MCLK, RAS* low = 4 MCLK)
1 : Standard RAS* (RAS* high = 2.5 MCLK , RAS* low = 3.5 MCLK)

CF10 : MCLK Frequency Select bit 1 (MSB)
CF9 : MCLK Frequency Select bit 0 (LSB)

CF10	CF9	MCLK (MHz)
0	0	50.11363
0	1	44.74431
1	0	41.16477
1	1	37.58523

CF8 : ROM BIOS size select
0 : 64K at C0000 to CFFFF
1 : 32K at C0000 to C7FFF

CF7 : System (host) bus Interface selection
0 : MicroChannel interface
1 : ISA (PC/XT/AT) bus interface

CF6 : VGA BIOS ROM select
0 : 16-bit BIOS ROM

MCS16* for BIOS ROM is decoded from C0000-C7FFF or C0000-CFFFF, depending on CF8 (Configuration bit 8).

1 : 8-bit BIOS ROM (MCS16* will not be decoded)

CF5 : Reserved

CF4 : Memory Clock (MCLK) source select
0 : External supply, the MCLK pin is configured as an input
1 : Internally generated, the MCLK pin is configured as an output

CF3 : Reserved

CF2 : Reserved

CF1 : Enable BIOS ROM zero-wait-state
0 : Enable output ZWS* to be driven active accessing the BIOS ROM
1 : Output ZWS* remains high impedance when accessing the BIOS ROM

CF0 : Reserved

5. CONFIGURATION NOTES FOR CL-GD5424/'26/'28

Table B9–4. CF15:0 for the CL-GD5424/'26/'28

Configuration Register															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MD 31	MD 30	MD 29	MD 28	MD 27	MD 26	MD 25	MD 24	MD 23	MD 22	MD 21	MD 20	MD 19	MD 18	MD 17	MD 16

CF14 : Bus Type Select [2]

CF13 : Select asymmetric RAS*/CAS* addressing
0 : CAS* Address uses MA7:0, RAS* address uses MA[9:0]
1 : RAS* and CAS* Addresses are output on MA[8:0]

CF12 : Select multiple-CAS* or multiple-WE* DRAM Interface
0 : Multiple CAS* — CAS*[3:0] used with one WE*
1 : Multiple WE* — WE*[3:0] used with one CAS*

Special case for the CL-GD5426/'28

CF13	CF12	Note
0	0	OE* pin becomes RAS1* for 2-Mbyte memory option

CF11 : DRAM Timing Select
0 : Extended RAS* (RAS* high = 3 MCLK, RAS* low = 4 MCLK)
1 : Standard RAS* (RAS* high = 2.5 MCLK, RAS* low = 3.5 MCLK)

CF10 : MCLK Frequency Select bit 1 (MSB)
CF9 : MCLK Frequency Select bit 0 (LSB)

CF10	CF9	MCLK (MHz)
0	0	50.11363
0	1	44.74431
1	0	41.16477
1	1	37.58523

CF8 : ROM BIOS Size Select
0 : 64K at C0000 to CFFFF
1 : 32K at C0000 to C7FFF

CF7: Bus-type Select[1] (see CF5 for details)

CF6 : VGA BIOS ROM Select
0 : 16-bit BIOS ROM

MCS16* for BIOS ROM is decoded from C0000-C7FFF or C0000-CFFFF, depending on CF8 (Configuration bit 8).

1 : 8-bit BIOS ROM (MCS16* will not be decoded)

CF5 : Bus-type Select [0]

Table B9–5. Bus Selection

Bus Interface	CF14	CF7	CF5
Reserved	0	0	0
'386DX local bus	0	0	1
'386SX local bus	0	1	0
'486SX/DX local bus	0	1	1
Reserved	1	0	0
VESA® VL-Bus™	1	1	0
MicroChannel® bus	1	0	1
ISA bus	1	1	1

NOTE: When configured for the VESA VL-Bus, the CPU RESET signal becomes the RDYRTN# signal.

CF4 : Memory Clock (MCLK) Source Select
0 : External supply, MCLK pin is configured as an input
1 : Internally generated, MCLK pin is configured as an output

CF3 (MD19):
MicroChannel: If a pull-down is installed on MD19, the CL-GD5426/'28 will be configured for 46E8 sleep. Bit 3 of 46E8 is the VGA Enable bit. If no pull-down is installed on MD19, the CL-GD5426/'28 will be configured for 3C3 sleep. Bit 0 of 3C3 is the VGA Enable bit.
All other Buses: If a pull-down is installed on MD19, the CL-GD5426/'28 will be configured for 3C3 sleep. Bit 0 of 3C3 is the VGA Enable bit. If no pull-down is installed on MD19, the CL-GD5426/'28 will be configured for 46E8 sleep. Bit 3 of 46E8 is the VGA Enable bit; bit 4 of 46E8 enables access to POS102.

POS102 Access:
MicroChannel: If the CL-GD5426/'28 is configured for the MicroChannel bus, CD-SETUP controls access to POS102.
All other Buses: If the CL-GD5426/'28 is configured for 46E8 sleep, 46E8[4] controls access to POS102. If the CL-GD5426/'28 is configured for 3C3 sleep, 94[5] controls access to POS102.

CF2 (MD18):
If a pull-down is installed on MD18, the internal DAC will respond to the 8514 DAC Address 2EA-2ED in addition to the standard VGA DAC addresses. If no pull-down is installed on MD18, the internal DAC will respond to the standard VGA DAC addresses only.

CF1 : Enable BIOS ROM zero-wait select
0 : Enable output ZERO* to be driven active accessing the BIOS ROM
1 : Output ZERO* remains high impedance when accessing the BIOS ROM

CF0 (MD16):
If a pull-down is installed on MD16, the DAC will be powered-down. There will be no response to I/O accesses at 3C6-3C9 except DAC writes will be shadowed and reads from 3C7 will be executed normally. The EROM output will be active for DAC I/O accesses at 3C6-3C9 except reads to 3C7. The EROM output will be active for memory reads at C000. If no pull-down is installed on MD16, the DAC will function in the standard manner.

6. CONFIGURATION NOTES FOR CL-GD5429

Table B9–6. CF15:0 for the CL-GD5429

Configuration Register															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MD 31	MD 30	MD 29	MD 28	MD 27	MD 26	MD 25	MD 24	MD 23	MD 22	MD 21	MD 20	MD 19	MD 18	MD 17	MD 16

CF15 : Select MCLK pin output source (see also CF4)
0 : The MCLK pin will source the internal VCLK VCO signal.
1 : The MCLK pin will source the internal MCLK VCO signal.

CF14 : Bus Select Type[2]. See CF5.

CF13 : Select asymmetric RAS*/CAS* addressing
0 : CAS* Address uses MA7:0, RAS* address uses MA[9:0]
1 : RAS* and CAS* Addresses are output on MA[8:0]

CF12 : Select multiple-CAS* or multiple-WE* DRAM Interface
0 : Multiple CAS* — CAS*[3:0] used with one WE*
1 : Multiple WE* — WE*[3:0] used with one CAS*

Special case for the CL-GD5429:

CF13	CF12	Note
0	0	OE* pin becomes RAS1* for 2-Mbyte memory option

CF11 : DRAM Timing Select
0 : Extended RAS* (RAS* high = 3 MCLK, RAS* low = 4 MCLK)
1 : Standard RAS* (RAS* high = 2.5 MCLK, RAS* low = 3.5 MCLK)

CF10 : MCLK Frequency Select bit 1 (MSB)
CF9 : MCLK Frequency Select bit 0 (LSB)

CF10	CF9	MCLK (MHz)
0	0	50.11363
0	1	44.74431
1	0	41.16477
1	1	37.58523

CF8 : ROM BIOS Size Select
0 : 64K at C0000 to CFFFF
1 : 32K at C0000 to C7FFF

CF7: Bus-type Select[1]: See CF5

CF6 : VGA BIOS ROM Select
0 : 16-bit BIOS ROM

MCS16* for BIOS ROM is decoded from C0000-C7FFF or C0000-CFFFF, depending on CF8 (Configuration bit 8).

1 : 8-bit BIOS ROM (MCS16* will not be decoded)

CF5 : Bus-type Select

Table B9–7. Bus Selection

Bus Interface	CF14	CF7	CF5
Reserved	0	0	0
'386DX local bus	0	0	1
'386SX local bus	0	1	0
Reserved	0	1	1
VESA® VL-Bus™ (> 33 MHz)	1	0	0
VESA® VL-Bus™ (<= 33 MHz)	1	1	0
MicroChannel® bus	1	0	1
ISA bus	1	1	1

CF4 : Memory Clock (MCLK) Source Select
0 : External supply, MCLK pin is configured as an input. Factory Testing only
1 : Internally generated, MCLK pin is configured as an output

CF3 (MD19):
0 : If a pull-down is installed on MD19, the CL-GD5429 will be configured for 3C3 sleep. Bit 0 of 3C3 is the VGA Enable bit.
1 : If no pull-down is installed on MD19, the CL-GD5429 will be configured for 46E8 sleep. Bit 3 of 46E8 is the VGA Enable bit; bit 4 of 46E8 enables access to POS102.

POS102 Access:

If the CL-GD5428 is configured for 46E8 sleep, 46E8[4] controls access to POS102. If the CL-GD5428 is configured for 3C3 sleep, 94[5] controls access to POS102.

CF2 (MD18):2070 Address when CF1 = 0.

0 : Select 2070 Address of 0290h to 029Bh.

1 : Select 2070 Address of 27C0h to 27CBh.

CF1 : Enable VESA VL LDEV# decode for 2070.

0: Enable 2070 Address decode for range selected by CF2. Generates LDEV# but no LRDY#.

1: Disable 2070 Address decode. CF2 is a don't care.

CF0 (MD16):

0 : The DAC will be powered-down. There will be no response to I/O accesses at 3C6-3C9 except DAC writes will be shadowed and reads from 3C7 will be executed normally. The EROM output will be active for DAC I/O accesses at 3C6-3C9 except reads to 3C7. The EROM output will be active for memory reads at C000.

1 : The DAC will function in the standard manner.

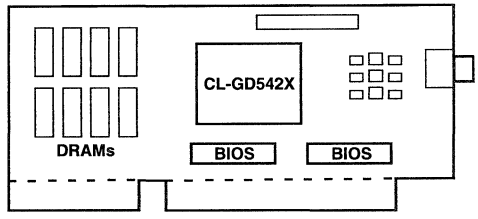
Appendix B10

PC Board Layout Considerations
Application Note

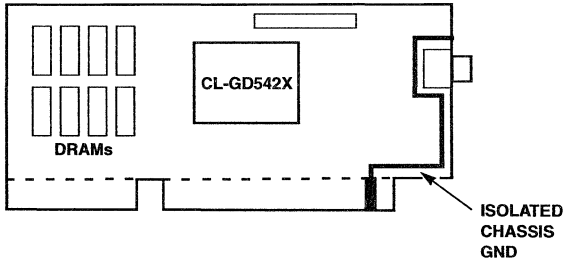
PC BOARD LAYOUT CONSIDERATIONS

1. LAYOUT CONSIDERATIONS

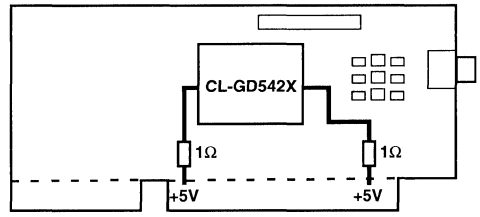
For dependable performance, it is very important to have a proper board layout. General placement of the components on an ISA board should match the following figure.



The layout should be optimized for the lowest noise on the VDD and VSS and provide good decoupling. A well-designed power distribution network is critical to reduce digital switching noise. For the two-layer design, ***solid wide*** traces are recommended on the power and ground lines. The width of the power traces should be at least 0.050 inches. The chassis ground plane should be isolated from the digital ground as indicated in the diagram below. Only the video connector mounting holes should be connected to the chassis ground plane. On the multi-layer boards, VSS (GND) pins should be directly connected to the ground plane.



The CL-GD542X family has built-in latch-up protection circuitry, but to add ***additional*** latch-up protection, power to the CL-GD542X should be provided through two 1Ω 1/4-Watt resistors. These resistors should be placed in parallel to +5V, with the power pins AVDDx and VDDx of CL-GD542X along with the decoupling capacitors shown in the following figure.



All the appropriate interface traces should be as short as possible, especially OSC (pin 159) and RESET (pin 41). All decoupling capacitors should be located close to the device with short leads to reduce lead inductance (refer to Appendix B1).

2. CLOCK SYNTHESIZER

The Clock Synthesizer is a built-in feature of the CL-GD542X product line. All needed frequencies are derived from a reference clock, typically 14.318 MHz. AVDD1 and AVDD4 to the Clock Synthesizer requires a low-noise power supply. The filter components for the MFILTER and VFILTER should be placed close to the pins to reduce power-supply noise, which can cause clock jitter. Refer to the Appendix B1 for the detailed values of the filter components.

3. HOST BUS INTERFACE

A digital ground plane (thick trace) should be used to isolate RESET and I/OCHRDY from high-speed system data lines to minimize cross-talk. Also, provide a RC-filter to the RESET Signal to reduce noise. A short trace length for the Address/Data bus will minimize noise and cross-talk.

4. VIDEO OUTPUT

The RGB, HSYNC, and VSYNC Output pins should be located close to the Video Connectors to minimize noise pickup. Place a PI-shape filter, consisting of two 47-pF capacitors and a ferrite bead, between the RGB line and the Video Connector (15-pin D-SUB). Refer to the schematics in Appendix B1 for additional details.

5. LAYOUTS AVAILABLE

Complete manufacturing kits, consisting of schematics, BOMs, and Gerber files are available to OEMs on the Cirrus Logic, Inc. Bulletin Board System (refer to Appendix D9 for more information on the BBS). These are for both ISA and VESA VL boards. Contact your sales office for further information.

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Appendix B11

Signature Generator
Application Note

SIGNATURE GENERATOR

1. INTRODUCTION

To automatically test the CL-GD542X video-output logic at full speed, Signature Generator (SG) logic has been added to the IC. With the addition of this feature, it is possible to capture a unique 16-bit signature for any given mode setup and video memory data. An error in the Video Memory interface, control logic, or pixel data manipulation will produce a different signature which can be compared to a known good signature value obtained from the same image. This allows the test technician to quickly and accurately test a video screen without having to visually inspect the screen for errors. This method is used extensively in the Manufacturing Test.

To run the SG, bits must be written in extended Sequencer register SR18 to initialize and arm the SG. A Status bit will reflect that the SG is running; when the Status bit changes state to 'not running', the signature may be read from extended Sequencer registers SR19 and SR1A.

Note that the signature is a function of the displayed pixels, not the display data. If the display screen includes blinking attributes or a blinking cursor, then the signature will be different for those frames when the pixel is blinked off as compared to those when the pixel is blinked on.

The SG register definitions are as follows:

SR18: Signature Generator Control

D7:5	Reserved
D4:2	Pixel Data Select. These three bits select one of the eight Pixel Data Bits to use as SG Input. 111 = P(7), 110 = P(6)... 000 = P(0)
D1	Reset Signature Generator 1 = Reset the Signature Generator 0 = Allow the Signature Generator to operate
D0	Signature Generator Enable/Status 1 = Start Generating Signature on next VSYNC (write) 0 = Signature Generator finished running; signature data ready (read)

NOTE: This bit must be set to start the SG and is automatically cleared when the SG is done.

SR19: Signature Generator Result — low byte

D7:0 Low byte of the 16-bit result from one video frame of signature data

SR1A: Signature Generator Result — high byte

D7:0 High byte of the 16-bit result from one video frame of signature data

The following code example in 'C' describes the method a programmer would take to capture eight signatures for any given screen. It is assumed that the screen is already being displayed, and no blinking attributes (in Text mode) are being displayed:

```
signature_capture ()  /*Capture eight signatures for any given
mode*/
  {
unsigned int result,i,SR19,SR1A;
unsigned int SIG [8];
union REGS in;

  in.x.ax = 0x0100;   /* shut of the cursor, if in text mode */
  in.x.cx = 0x2000;
  int86x (0x10,&in,&out,&seg);
  outp (0x3c4,6);     /* unlock extended registers */
  outp (0x3c5,0x12); /* (not required for CL-GD5429) */
  for (i = 0;i <= 7; i++) {  /* cycle through all pixel data bits */
   outp (0x3c4,0x18);      /* arm the SG and set for pixel data bit */
    outp (0x3c5, (2 | (i<<2)));      /* reset */
    outp (0x3c5, (i << 2));          / *select the data bit*/
    outp (0x3c4,0x18);
    outp (0x3c5, (1 | (i << 2)));    / *and start the SG */
    result = inp (0x3c5);            /* pre-read SG status */
   while ((result & 0x01) != 0) {  /*wait until signature is done */
      outp (0x3c4,0x18);
      result = inp (0x3c5);          /* read the status*/
    }
    outp (0x3c4,0x19);  /* get low signature byte */
    SR19 = inp (0x3c5);
    outp (0x3c4,0x1A);  /* get high signature byte */
    SR1A = inp (0x3c5);
    SIG [i] = (SR1A << 8) + SR19;
  }                                  /*end of for */
  }
```

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Appendix B12

PCB Layout Considerations For Motherboards
Application Note

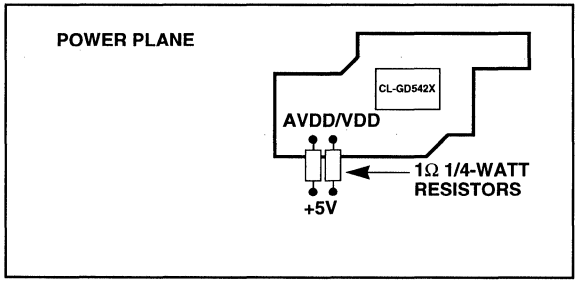
PCB LAYOUT CONSIDERATIONS FOR MOTHERBOARDS

1.0 LAYOUT CONSIDERATIONS (FOR FOUR LAYERS)

For dependable performance, it is important to have a proper layout. Refer to Appendix B10 for detailed description for two-layer PCB layout considerations and component placement. Follow the same guidelines as described in Appendix B10 except for the Power and Ground Planes.

2.0 POWER PLANE

The CL-GD542X family has built-in latch-up protection circuitry, but to add ***additional*** latch-up protection, power to the CL-GD542X should be provided through two 1Ω, 1/4-watt resistors. These resistors should be placed in parallel with each other, but in series with VCC (+5V) to VDDx and AVDD2-3. Power to AVDD1 and AVDD4 is provided through RC networks. Refer to Appendix B1 for ISA adapter board schematics. A block diagram for the Power Plane is shown below:

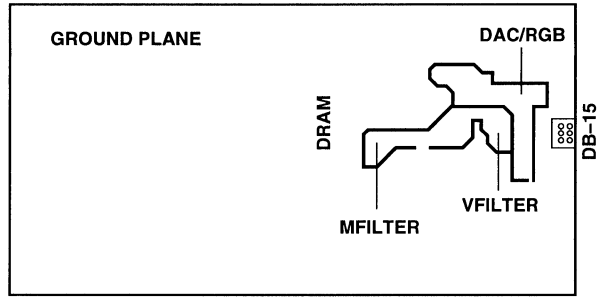


NOTE: The solid line cuts the main Power Plane and creates a separate power segment for the CL-GD542X. The main Power Plane can be used to supply the power for the DRAMs, Buffers, and EPROMs (if any).

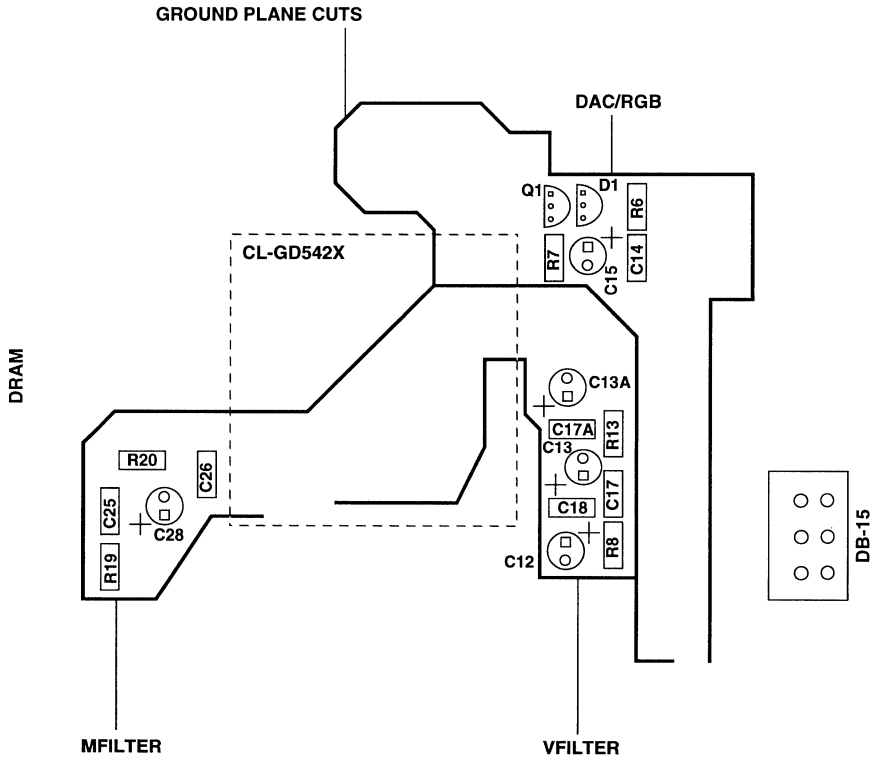
3.0 GROUND PLANE

Since the CL-GD542X has a built-in True Color Multi-mode palette DAC and Clock Synthesizer, it is important that these analog components have noise-free power and ground. Special attention must be paid to the VFILTER, MFILTER, and IREF pins, and the associated passive components for those pins. The VFILTER pin is used to generate the Video Clock for all graphics and text modes. The MFILTER pin is used for the memory (DRAM) timing. The IREF pin provides the constant current to the True Color palette DAC, which provides the analog output on the RBG lines. The chassis and the RGB signal should also be isolated from the main ground.

Use the following diagram as a reference for Ground Plane layout.



The figure below shows the detailed placement of the passive components for the MFILTER, VFILTER, and IREF Circuitry (refer to Appendix B1 for ISA adapter board schematics and for the reference names of the components).



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Appendix B13

Pinscan Testing

Application Note

PINSCAN TESTING

1. INTRODUCTION

Pinscan testing is a technique for verifying if an IC has been properly soldered to a circuit board. Any IC signal pin that is not connected to the board, or that is shorted to any neighboring pin or trace, can be detected using automated testing. The advantage of pinscan testing is that the test patterns to verify full-board connectivity are much simpler than would otherwise be possible. The pins are connected sequentially around the IC in a single chain, so that the value on each output pin depends only on the values applied to other pins, rather than the internal state of the VGA processor. In addition, the pinscan logic is strictly combinatorial, so no clock pulses are required.

The first pin in the chain is an input pin; the last pin is an output pin. Each input signal is exclusive-OR'ed (XOR'ed) with the scan data from its lower-numbered neighboring input or output pin. The result of this XOR is passed to its higher-numbered neighbor. Each output pin will be driven with the value passed from its lower-numbered neighbor; that value is inverted and passed to its higher-numbered neighbor.

In Pinscan mode, the test program begins by driving all the input pins to a '0', and verifying that the output pins match the values shown in the table that follows. On subsequent cycles, the program drives each input pin, one at a time, to a '1' and verifies that all the 'down-stream' outputs match the values shown. In each case, the output is inverted from the value for the all-zeroes case.

If the value applied to an input pin changes and the 'down-stream' output pins do not change, then that input is shorted or not soldered. If any single output is wrong, then it is either shorted or not soldered.

Entering Pinscan Mode

The CL-GD542X is placed into Pinscan mode by making RESET HIGH for at least 20 ns while TWR* is LOW.

Exiting Pinscan Mode

The CL-GD542x is removed from Pinscan mode by making RESET HIGH with TWR* HIGH.

Pinscan Order

In the following table, the pin names are for ISA bus. Both versions of the CL-GD5420 are slightly different from the newer members of the family. These differences are covered in the notes.

Table B13–1. Pinscan Order

Pin Name	Pin Number	Direction	All Inputs = 0	1 Input = 1	CL-GD5420 -65QC (P-well) Note	CL-GD5420 -75QC (N-well) Note
SD[15]	3	In				
SD[14]	4	In				
SD[13]	5	In				
SD[12]	6	In				
SD[11]	8	In				
SD[10]	9	In				
SD[9]	10	In				
SD[8]	11	In				
MEMW*	13	In				
MEMR*	14	In				
LA[17]	15	In				
LA[18]	16	In				
LA[19]	17	In				
LA[20]	18	In				
LA[21]	19	In				
LA[22]	20	In				
LA[23]	21	In				
IOCS16*	22	Out	1	0		
MCS16*	23	Out	0	1		
SBHE*	24	In				
BALE	25	In				
SA[0]	27	In				
SA[1]	28	In				
SA[2]	29	In				
SA[3]	30	In				
SA[4]	31	In				
SA[5]	32	In				
SA[6]	33	In				

Table B13–1. Pinscan Order *(cont.)*

Pin Name	Pin Number	Direction	All Inputs = 0	1 Input = 1	CL-GD5420 -65QC (P-well) Note	CL-GD5420 -75QC (N-well) Note
SA[7]	34	In				
SA[8]	35	In				
SA[9]	36	In				
SA[10]	37	In				
SA[11]	38	In				
SA[12]	39	In				
RESET	41	In				
SA[13]	42	In				
SA[14]	43	In				
SA[15]	44	In				
SA[16]	45	In				
AEN	46	In				
IOCHRDY	47	Out	0	1		
REFRESH*	48	In				
IOR*	49	In				
IOW*	50	In				
0WS*	51	Out	Hi-Z	0		
IRQ	52	Out	0	1		
SD[0]	54	In				
SD[1]	55	In				
SD[2]	56	In				
SD[3]	57	In				
SD[4]	59	In				
SD[5]	60	In				
SD[6]	62	In				
SD[7]	63	In				
TWR*	67	In				
VSYNC	68	Out	1	0		

Table B13–1. Pinscan Order *(cont.)*

Pin Name	Pin Number	Direction	All Inputs = 0	1 Input = 1	CL-GD5420 -65QC (P-well) Note	CL-GD5420 -75QC (N-well) Note
HSYNC	69	Out	0	1		
OVRW*	71	Out	1	0	n/c	n/c
EEDI	73	In				
EECS	74	Out	0	1	1 for all inputs =0, 0 for 1 input = 1	
P[0]	79	In				
P[1]	82	In				
P[2]	83	In				
P[3]	84	In				
P[4]	86	In				
P[5]	87	In				
P[6]	88	In				
P[7]	89	In				
DCLK	92	In				
BLANK*	93	In				
EVIDEO*	94	In				
ESYNC*	95	In				
EDCLK*	96	In				
MD[31]	97	In				
MD[30]	98	In				
MD[29]	99	In				
MD[28]	100	In				
MD[27]	102	In				
MD[26]	103	In				
MD[25]	104	In				
MD[24]	105	In				
WE3*	106	In	0	1	Output: See Note 1	
MD[23]	108	In				
MD[22]	109	In				

Table B13–1. Pinscan Order *(cont.)*

Pin Name	Pin Number	Direction	All Inputs = 0	1 Input = 1	CL-GD5420 -65QC (P-well) Note	CL-GD5420 -75QC (N-well) Note
MD[21]	110	In				
MD[20]	111	In				
MD[19]	112	In				
MD[18]	113	In				
MD[17]	114	In				
MD[16]	115	In				
WE2*	116	In	1	0	Output: See Note 2	
MD[15]	117	In				n/c
MD[14]	118	In				n/c
MD[13]	119	In				n/c
MD[12]	122	In				n/c
MD[11]	123	In				n/c
MD[10]	124	In				n/c
MD[9]	125	In				n/c
MD[8]	126	In				n/c
WE1*	127	In	0	1	Output: Note 3	n/c
MD[7]	129	In				n/c
MD[6]	130	In				n/c
MD[5]	131	In				n/c
MD[4]	132	In				n/c
MD[3]	133	In				n/c
MD[2]	134	In				n/c
MD[1]	135	In				n/c
MD[0]	136	In				n/c
WE0*	138	In	1	0	Output: Note 4	n/c
CAS*	139	In				
OE*	141	Out	0	1	Note 5	
RAS	142	Out	1	0	Note 5	

Table B13–1. Pinscan Order *(cont.)*

Pin Name	Pin Number	Direction	All Inputs = 0	1 Input = 1	CL-GD5420 -65QC (P-well) Note	CL-GD5420 -75QC (N-well) Note
MA[9]	143	Out	0	1	Note 5	
MA[8]	145	Out	1	0	Note 5	
MA[7]	146	Out	0	1	Note 5	
MA[6]	147	Out	1	0	Note 5	
MA[5]	148	Out	0	1	Note 5	
MA[4]	149	Out	1	0	Note 5	
MA[3]	150	Out	0	1	Note 5	
MA[2]	151	Out	1	0	Note 5	
MA[1]	152	Out	0	1	Note 5	
MA[0]	153	Out	1	0	Note 5	
MCLK	157	In				
EROM*	2	Out	0	1	Note 5	

Notes:

1. Pin 106 is an input on all chips except both versions of the CL-GD5420. On the '20, it is an output with the sense indicated in the table.
2. Pin 116 is an input on all chips except both versions of the CL-GD5420. On the '20, it is an output with the sense indicated in the table.
3. Pin 127 is an input on all chips except both versions of the CL-GD5420. On the '20-65QC, it is a no-connect. On the '20-75QC, it is an output with the sense indicated in the table.
4. Pin 138 is an input on all chips except both versions of the CL-GD5420. On the '20-65QC, it is a no-connect. On the '20-75QC, it is an output with the sense indicated in the table.
5. The CL-GD5420-65QC, all outputs from pin 141 through pin 2 have opposite sense as the rest of the family. That is, the sense for the '20-65QC is *opposite* as indicated in the table.

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Appendix B14

Video Overlay and DAC Mode Switching Application Note

VIDEO OVERLAY AND DAC MODE SWITCHING

1. INTRODUCTION

This appendix describes the Video Overlay and DAC Mode Switching functions available on the CL-GD542X family. The following table indicates the capabilities of each family member.

Table B14–1. Video Overlay Functions

Capability	GD5420	GD5422	GD5424	GD5426/'28	GD5429
VESA passthrough	Yes	Yes	Yes	Yes	Yes
Switch with EVIDEO*	No	Yes	Yes	Yes	Yes
On-chip Window timing generator	No	Yes	Yes	Yes	Yes
Switch with Color Key	No	Yes	Yes	Yes	Yes
Switch with OVRW* and Color Key	No	No	Yes	Yes	No
Switch with EVIDEO* and Color Key	No	No	No	No	Yes
VAFC Output Baseline	Yes	Yes	Yes	Yes	Yes
VAFC Input Baseline	No	No	No	No	Yes

2. OVERVIEW

Video Overlay refers to dynamically changing the video source between data from the VGA display memory and data from an external source. The overlay can take place on a pixel basis. Refer to Figure B14–1.

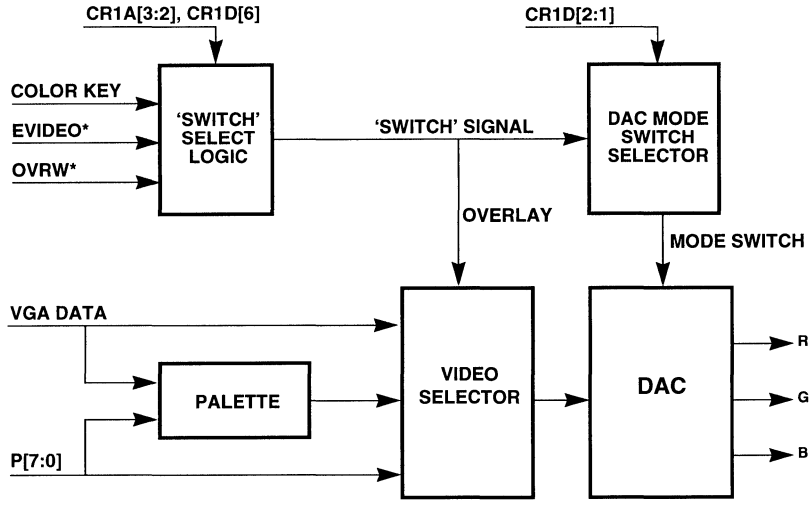

Figure B14–1. Mode Switching

The pixels that are to be overlayed can be chosen with the EVIDEO* pin or the internally generated OVRW* signal (for the CL-GD5429 only). This selection method is called *timing*. The pixels to be overlaid can be chosen with the Color Key Compare logic. This selection method is called *key*, The selection method is determined by CR1A[3:2] and CR1D[6].

The following table enumerates the six cases that are covered in detail later in this appendix.

Table B14–2. SWITCH Chosen With

CR1A[3]	CR1A[2]	CR1D[6]	Source of Switch	EVIDEO*
0	0	X	VGA-compatible Operation: Switch disabled	Input
0	1	0	EVIDEO* pin	Input
0	1	1	OVRW* signal CL-GD5429 only	Input
1	0	0	EVIDEO* pin AND'ed with Color Key Compare CL-GD5429 only	Input
1	0	1	OVRW* signal AND'ed with Color Key Compare Except CL-GD5429	Output
1	1	X	Color Key Compare	Output

DAC Mode Switching refers to dynamically changing the DAC mode between standard VGA 8-bit-per-pixel through the palette, and another mode (such as 8- or 16-bit RGB). DAC Mode Switching can take place on a pixel basis.

In every case where DAC Mode Switching is used, one mode will be the standard VGA 8-bits mode through the LUT. The second mode will be the one programmed into the Hidden DAC register.

The CL-GD542X can be programmed so that DAC Mode Switching occurs when 'Switch' is active, or when 'Switch' is not active, or not at all, as shown Table B14–3.

Table B14–3. Relationship Between Switch and DAC Mode Switching

CR1D[2:1]	DAC Mode Switching
00	Choose Extended DAC mode on Switch true
01	Choose Extended DAC mode on Switch false
1x	Mode switching disabled

The various cases of extended DAC mode programming and DAC Mode Switching selections are all more or less orthogonal, leading to many combination. Table B14–4 lists various useful combinations. Observe that these combinations are independent of the actual source of the Switch Signal (that is, how the window is defined).

Table B14–4. Switch and DAC Mode Switching Combinations

BackGround	Window	CR1D[2:1]	CR1D[0]	HDR	Note
Internal LUT	External 8-bit RBG	00	0	0xC9	
Internal LUT	External grayscale	00	0	0xC8	
Internal LUT	External 15-bit RGB	00	0	0xC0	
Internal LUT	External 16-bit RGB	00	0	0xC1	VAFC Baseline
Internal LUT	External LUT	1x	0	0x00	
Internal 8-bit RGB	External LUT	01	0	0xC9	
Internal 8-bit RGB	External 8-bit RGB	1x	0	0xC9	
Internal 15-bit RGB	External 8-bit LUT	01	0	0xC0	
Internal 16-bit RGB	External 8-bit LUT	01	0	0xC1	

NOTE: Internal refers to data taken from the display memory. External refers to data taken from the Pixel bus (P[7:0]). 'LUT' refers to 8-bit data used to choose a color from the lookup table.

3. SWITCH WITH EVIDEO*

Switch with EVIDEO* is selected when the CR1A[3,2] field is programmed to '0,1'. For the CL-GD5429 only, CR1D[6] must be programmed to '0'. The P-bus is switched to inputs. The external Video Generator must always drive the bus to guarantee valid CMOS logic levels, even when the inputs are being ignored.

There is no requirement for pixels to be overlayed to be contiguous (adjacent), either horizontally or vertically. The extended DAC mode programmed into the HDR will be chosen either when EVIDEO* is active, or when EVIDEO* is not active, or not at all. This depends on the programming of CR1D[2:1]. The block diagram in Figure B14–2. indicates how a system might be configured to use this mode.

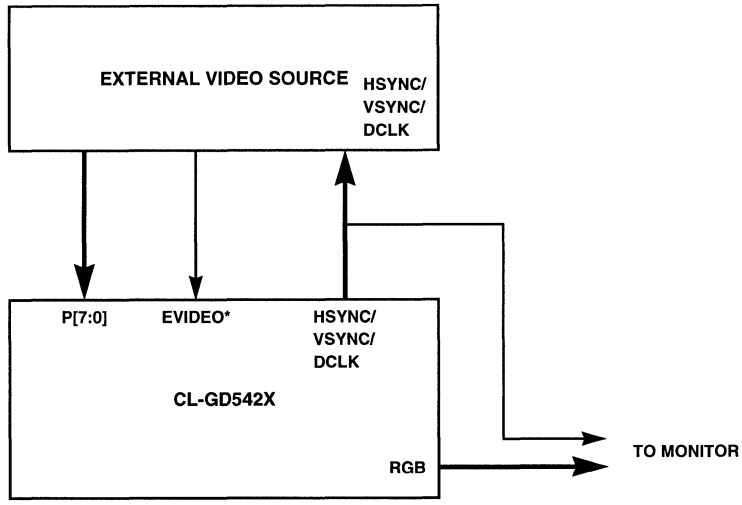

Figure B14–2. System Configuration with EVIDEO*

The external video source has the responsibility for determining which portion of the screen is going to be overlayed with its video. For every pixel that is to be overlayed, it must drive EVIDEO* active, and it must provide either 8- or 16-bit video at the P-bus.

The system designer must guarantee that the External Video Source and the CL-GD542X are in synchrony (otherwise the overlayed video will appear at random places on the screen). This is why the sync and DCLK signals are made available from the CL-GD542X to the External Video Source.

EVIDEO* has a setup and hold time requirement with respect to DCLK to guarantee that the desired pixel will be overlayed and that adjacent pixels will not be overlayed. Observe that DCLK is an output and EVIDEO* is an input. This is not a typical definition of set up and hold times.

If 8-bit data is being clocked into the P-bus, there is a data setup and hold requirement to the positive-going edge of DCLK. If 16-bit data is being clocked into the P-bus, there is a data setup and hold requirement to both edges of DCLK (the DAC is in Clocking mode 1). The rising edge of DCLK will clock the least-significant byte of the pixel; the falling edge will clock the most-significant byte.

4. SWITCH WITH COLOR KEY

Switch with Color Key is enabled when the CR1A[3:2] field is programmed to '1,1'. In this mode, the choice of pixels to be overlayed is controlled strictly by the contents of display memory. If a VGA pixel byte compares with the contents of the Color Key register, Switch will be enabled. EVIDEO* is a normally LOW output in this mode; it will go HIGH one VCLK period before any pixel is replaced. If horizontally contiguous pixels are to be replaced, EVIDEO* will remain high appropriately.

The matching of the pixel with the Color Key is done under a mask. GRC contains the Color Key; GRD contains the mask. The key is compared with the pixel from display memory only for those bits for which the mask is a '0'. If the values 0xFC through 0xFF are to be used for the key, register GRC can be loaded with any value in the range 0xFC though 0xFF, and GRD would be loaded with the value 0x03.

In cases where the CL-GD542X is programmed for other than 8-bits-per-pixel, the high-order byte of the pixel will be compared; the other(s) will be ignored. This is shown in Table B14–5.

Table B14–5. Color Key Bytes

Mode	Byte Compared
8 bits-per-pixel	Every byte
16 bits-per-pixel	High byte

There is no requirement that the pixels to be overlayed are contiguous (adjacent), either horizontally or vertically. The Extended DAC mode programmed into the HDR will be chosen either when the color key matches, when the color key does not match, or not at all. This depends on the programming of CR1D[2:1]. The block diagram in Figure B14–3 indicates how a system might be configured to use this mode.

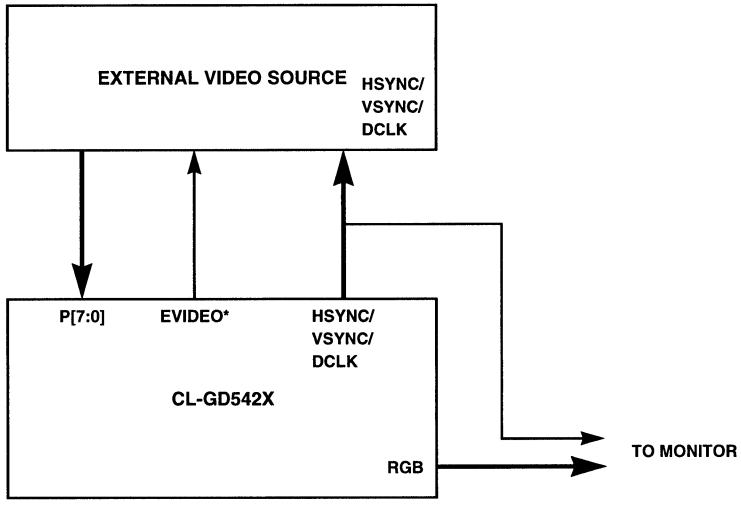

Figure B14–3. System Configuration with Color Key

The external video source can determine which pixels are to be overlayed by monitoring the EVIDEO* output of the CL-GD542X. For every pixel that is to be overlayed, it must provide either 8- or 16-bit video at the P-bus.

If 8-bit data is being clocked into the P-bus, there is a data setup and hold requirement to the positive-going edge of DCLK. If 16-bit data is being clocked into the P-bus, there is a data setup and hold requirement to both edges of DCLK (the DAC is in Clocking Mode 1). The rising edge of DCLK will clock the least-significant byte of the pixel; the falling edge will clock the most-significant byte.

5. SWITCH WITH COLOR KEY ANDed with EVIDEO* (CL-GD5429)

Switch with Color Key ANDed with EVIDEO* when the CR1A[3:2] field is programmed to '1,0'. CR1D[6] must be programmed to a '0'. The Switch signal is the logical 'AND' of the Color Key Comparison and EVIDEO* being low. EVIDEO* is an input in this mode. This mode in available only on the CL-GD5429.

The extended DAC mode programmed into the HDR will be chosen either when the condi-

tion is true, or when the condition is not true, or not at all. This depends on the programming of CR1D[2:1].

This mode is intended to restrict the Color Key effect to a specified area.

This mode can also be used to mechanize a dynamic window with horizontal resolution finer than an eight-pixel character clock. The coarse horizontal timing would be generated with the on-chip Window Timing Generator as described above, and the fine (pixel resolution) would be controlled by changing either the contents of display memory or the Color Key Mask.

6. ON-CHIP WINDOW TIMING GENERATOR

The CL-GD542X contains logic to generate a single rectangular window. If this mode is enabled, the window timing comes out on OVRW*, which may be fed back into EVIDEO*; the chip specifies its own window. For the CL-GD5429 only, the internal signal is directly available as the Switch signal. For the CL-GD5424/'26/'28, OVRW* can be ANDed with Color Key to provide the switch signal.

This mode is chosen by programming CR1B[5] to a '1'. When this is done, the blanking term to the palette DAC comes from Display Enable, and there is no border. This frees the Blank Generator Logic, which is used as a window generator. The following timing diagram shows how the Blank Start and Blank End registers specify either the horizontal or vertical component of the window; the other is similar. The Horizontal Blank End field is extended to eight bits and the Vertical Blank End is extended to 10 bits.

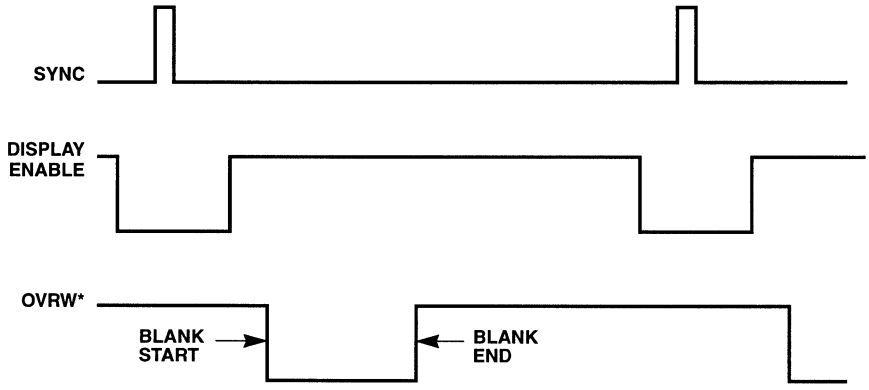

Figure B14–4. Blank End And Blank Start Timing

When the vertical timing and the horizontal timing generated coincide, OVRW* will be driven LOW, and this indicates the window. OVRW* may be connected directly to EVIDEO* if Switch on Color Key only is never going to be chosen. If Switch on Color Key only will be chosen, OVRW* must be driven into EVIDEO* with an external three-state buffer to avoid a potential bus collision. This is avoided on the CL-GD5429 by making the term available internally.

This method of generating timing has four restrictions that require consideration. First, since the blank timing generation logic is used for window generation, there can be no border. This is inconsequential since the VESA timing specifications do not include a border. Second, since the Horizontal Counters operate on an eight-pixel character clock, the resolution of the horizontal component of the window is eight pixels. This can be overcome at least in part by using EVIDEO* ANDed with Color Key, as discussed previously. Third, there can only be a single window and it must be rectangular. Finally, the first or third (or subsequent) scanline or group of eight pixels can be chosen as a window boundary, but not the second scanline or group of eight pixels.

When programming horizontal and vertical blanking, nine registers must be programmed to set the four blank parameters. Five of these registers contain bits related to other functions.

Table B14–6. Programming of Horizontal and Vertical Blanking

Register	Bits	Parameter	Other Bits
CR2	7:0	Horizontal Blank Start [7:0]	–
CR3	4:0	Horizontal Blank End [4:0]	7:5
CR5	7	Horizontal Blank End [5]	6:0
CR7	3	Vertical Blank Start [8]	7:4, 2:0
CR9	5	Vertical Blank Start [9]	7:6, 4:0
CR15	[7:0]	Vertical Blank Start [7:0]	–
CR16	[7:0]	Vertical Blank End [7:0]	–
CR1A	[7:6]	Vertical Blank End [9:8]	3:0
CR1A	[5:4]	Horizontal Blank End [7:6]	–

7. SWITCH WITH OVRW* (CL-GD5429 Only)

Switch with OVRW* is selected when the CR1A[3,2] field is programmed to '0,1' and CR1D[6] must be programmed to '1'. This mode is available on the CL-GD5429 only. The P-Bus is switched to inputs. The external Video Generator must always drive the bus to guarantee valid CMOS logic levels, even when the inputs are being ignored.

The Extended DAC mode programmed into the HDR will be chosen either when OVRW* is active, or when OVRW* is not active, or not at all. This depends on the programming of CR1D[2:1]. The block diagram in Figure B14–5 indicates how a system might be configured to use this mode.

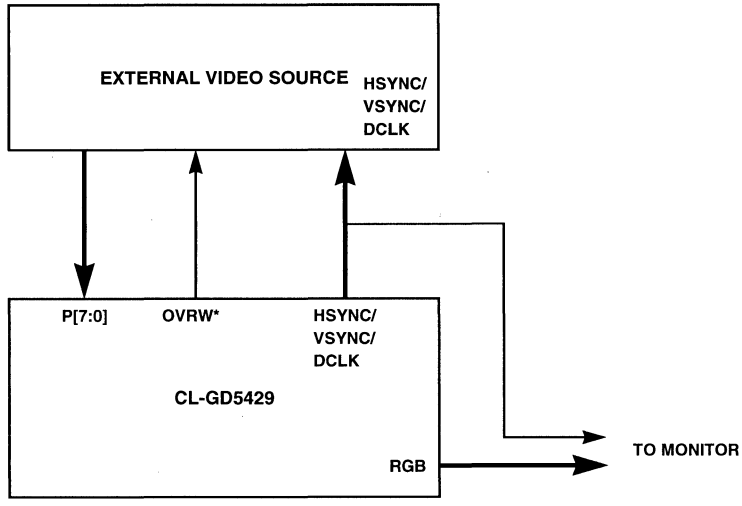

Figure B14–5. System Configuration with OVRW* (CL-GD5429 Only)

The external video source must monitor OVRW* to determine which portion of the screen is going to be overlayed with its video. For every pixel that is to be overlayed, it must provide either 8- or 16-bit video at the P-bus.

If 8-bit data is being clocked into the P-bus, there is a data setup and hold requirement to the positive-going edge of DCLK. If 16-bit data is being clocked into the P-bus, there is a data setup and hold requirement to both edges of DCLK (the DAC is in Clocking mode 1). The rising edge of DCLK will clock the least-significant byte of the pixel; the falling edge will clock the most-significant byte.

8. VESA ADVANCED FEATURE CONNECTOR (VAFC)

All members of the CL-GD542X family support VAFC baseline output; the CL-GD5429 also supports VAFC baseline input. At the time of this writing, hardware and software to implement baseline input is in development. An application note will be available when development is complete. For board support of these functions, ensure that the extra pins on the feature connector are wired via jumpers or zero-Ω resistors, as indicated in Table B14–7.

Table B14–7. Connections to VESA Feature Connector for VAFC Compatibility

Pin	Jumper to:	Note
Z7	VCC	Power for VAFC/VESA bridge
Z12	MCLK	Will be VCLK VCO
Z13	OVRW*	Internally generated window timing

9. USING THE INTERNAL CLOCK WITH DCLK AS INPUT

The overlay modes described in this Appendix are intended to be used in a configuration where the video clock is provided by the external video source. If the clock were to be provided by the CL-GD542X, then the result is a situation of clocking data into a device where the device itself is providing the clock.

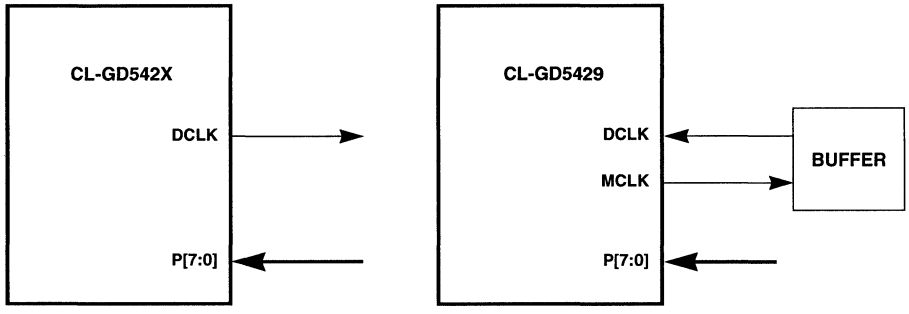

Figure B14–6. DCLK as an Input

This presents an almost impossible situation when it comes to characterizing the setup and hold times involved. Since the characterization equipment operates synchronously, it was never intended to deal with internally generated, asynchronous clocks. The result is, with respect to the internal DCLK, setup and hold times are not specified.

As a configuration option, the CL-GD5429 VCLK VCO can be sourced onto the MCLK pin. This is selected when a pull-down resistor is installed on MD29. Supplying an external buffer will drive MCLK into DCLK making both DCLK and the Pixel bus inputs, making it possible to specify setup and hold times.

10. STATIC OVERLAY

The CL-GD542X supports the standard VESA passthrough function, during which the EVIDEO* pin is statically driven LOW and video is driven into the P-bus. The entire frame is overlayed, and the contents of display memory are ignored. EDCLK* is typically driven LOW so that DCLK as well as the video are supplied externally.

Appendix B15

EEPROM Interface and Programming Application Note

EEPROM INTERFACE AND PROGRAMMING

1. INTRODUCTION

This application note covers the interface and programming details of the optional EEPROM (Electrically Erasable Programmable Read-Only Memory), and provides an overview of Extension register SR8. The timing restrictions imposed by the EEPROM device are covered along with examples of writing and reading the EEPROM.

The EEPROM is used by the Cirrus Logic BIOS to contain system configuration information, such as monitor type and refresh rate. The BIOS uses the first eight bytes of the EEPROM; it would be possible to use the rest for other applications.

The programming examples are for the XL93C46 1024-bit device.

The EEPROM option is available only if the CL-GD542x is configured for ISA bus.

2. EXTENSION REGISTER SR8

The EEPROM interface is controlled through the Extension register SR8 (refer to Chapter 9 for details on this register). The bits are summarized in Table B15–1

Table B15–1. Extension Register SR8 Bit Summary

Bit	Function
7	EEPROM Input Data
6	Disable MCS16* for display memory (**NOTE**: This bit *must* be preserved.)
5	Latch ESYNC/EVIDEO* Input state
4	Enable ESYNC/EVIDEO* as outputs for EEPROM Data and Serial Data Clock (SK)
3	Serial Data Input (DI) to EEPROM if bit 4 = 1
2	SK to EEPROM if bit 4 = 1
1	Enable EEPROM Data In
0	Chip Select (CS) to EEPROM

3. TIMING CONSIDERATIONS

Serial EEPROMs are inherently slow devices. Software written to control EEPROMs must include timing delays so that signal transitions do not take place too quickly. A data sheet for the particular device should be consulted; the parameters listed in Table B15–2 are typical.

Table B1–2. Typical Timing Parameters

Parameter	MIN	MAX	Units
DI setup to SK positive transition	1	–	µs
DI hold from SK positive transition	1	–	µs
SK High-pulse Width	2		µs
SK Low-pulse Width	2		µs
DO delay from SK positive transition	2		µs

The times specified in the table above are minimums. Longer delays will not damage the device. The EEPROM write operation requires 10 µs after the last bit has been transferred; no other operation is allowed until this time has elapsed.

The XL95C46 EEPROMs are organized as 64 sixteen-bit locations (each with a 6-bit address). Any data transfer, read, or write must transfer all 16 bits for correct operation.

3.1 Write Example

1. Set the CL-GD542X for EEPROM Control:
   a. Unlock the Extended registers (SR6=12h).
   b. Determine the state of SR8[6] and save it for all subsequent writes.
   c. Latch ESYNC and EVIDEO* Inputs (SR8[5]=1).
   d. Enable EEPROM Interface (SR8[4]=1, SR8[1]=1). For all writes to SR8 from now until Step 5, bits 5, 4, and 1 must be uniformly, and bit 6 must *always* be as determined in Step 1b.

2. Enable the EEPROM for writes:
   a. Set the EEPROM Chip Select high (SR8[0]=1).
   b. Send the Write Enable Command (0100 1100000) to the EEPROM:
      – write data bit into SR8[3]
      – set SK high (SR8[2]=1)
      – set SK low (SR8[2]=0)
      – get the next data bit and repeat the sequence until all 11 bits are sent.
   c. Set the EEPROM Chip Select low (SR8[0]=0).

3. Write 16 bits of data to the EEPROM location desired:
   a. Set the EEPROM Chip Select high (SR8[0]=1).
   b. Send the Write Register Command (0101 A5..A0 D15..D0) to the EEPROM:
      – write data bit into SR8[3]
      – set SK high (SR8[2]=1)
      – set SK low (SR8[2]=0)
      – the bit sequence is 0101 A5..A0 D15..D0
      where A5..A0 is the 6-bit address and D15..D0 is the data.
   c. Set the EEPROM Chip Select low (SR8[0]=0).

4. Repeat Step 3, if required.

5. Disable the EEPROM:
   a. Set the EEPROM Chip Select high (SR8[0]=1).
   b. Send the Disable Programming Command (0100 0000000) to the EEPROM
      – write data bit into SR8[3]
      – set SK high (SR8[2]=1)
      – set SK low (SR8[2]=0)
      – get the next data bit and repeat the sequence until all 11 bits are sent.
   c. Set the EEPROM Chip Select low (SR8[0]=0).

6. Remove the CL-GD542X from EEPROM Control:
   a. Disable the EEPROM Interface (SR8[4]=0, SR8[1]=0).
   b. Un-latch ESYNC and EVIDEO* (SR8[5]=0).
   c. Lock the Extended registers (SR6=0).

3.2 Read Example

1. Set the CL-GD542X for EEPROM Control:
   a. Unlock the Extended registers (SR6=12h).
   b. Determine the state of SR8[6] and save it for all subsequent writes.
   c. Latch ESYNC and EVIDEO* Inputs (SR8[5]=1).
   d. Enable EEPROM Interface (SR8[4]=1, SR8[1]=1). For all writes to SR8 from now until Step 5, bits 5, 4, and 1 must be uniformly, and Bit 6 must *always* be as determined in Step 1b.

2. Read the EEPROM:
   a. Set the EEPROM Chip Select high (SR8[0]=1).
   b. Send the READ Command (010 A5..A0) to the EEPROM:
      – write data bit into SR8[3]
      – set SK high (SR8[2]=1)
      – set SK low (SR8[2]=0)
      – get the next data bit and repeat the sequence until all 10 bits are sent.
   c. Read EEPROM Data D15..D0.
      – set SK high (SR8[2]=1)
      – set SK low (SR8[2]=0)
      – read the data bit at SR8[7]: first bit is D15
      – continue until all 16 bits are read.
   d. Set the EEPROM Chip Select low (SR8[0]=0).

3. Repeat Step 2, if required.

4. Remove the CL-GD542X from EEPROM Control:
   a. Disable the EEPROM Interface (SR8[4]=0, SR8[1]=0).
   b. Un-latch ESYNC and EVIDEO* (SR8[5]=0).
   c. Lock the Extended registers (SR6=0).

Appendix B16

Family Compatibility and Upgrading Application Note

FAMILY COMPATIBILITY AND UPGRADING

1. INTRODUCTION

This application note shows the relationship among members of the True Color VGA family and also provides some insight into planning the end-user product for upgrading.

The CL-GD542X family of VGA controllers consists of six members. In order of increasing capability and cost, the True Color family members are: CL-GD5420, CL-GD5422, CL-GD5424, CL-GD5426, CL-GD5428, and CL-GD5429.

By upgrade path, it is meant that a higher-numbered (more capable) family member can be soldered onto the same board that previously supported a lower-numbered family member. Clearly, if more memory is to be used than was possible with the less capable family member, there must be space for an upgrade on the board.

In some cases it makes sense to upgrade without increasing the memory capability. For example, an upgrade from a CL-GD5420 to a CL-GD5422 will take advantage of the board-level tests made possible by the Signature Generator feature.

Table B16–1 provides an overview of the *differences* in the family members, and is *not* a capability chart for the family.

Table B16–1. CL-GD542X Family Differences

Item	GD5420	GD5422	GD5424	GD5426/'28	GD5429
Host Bus					
Bus Connections	ISA, Micro-Channel	ISA, Micro-Channel	ISA, Micro-Channel, '386/'486 Local	ISA, Micro-Channel, '386/'486 Local	ISA, Micro-Channel, '386/'486 Local
Linear Addressing	–	✓	✓	✓	✓
Display Memory					
Maximum Memory	1024K	1024K	1024K	2048K	2048K
Colors @ 640 x 480	256	16M	16M	16M	16M
Colors @ 800 x 600	256	64K	64K	64K	64K
Colors @1024 x 768	256[a]	256	256	64K (Interlaced)	64K (Interlaced)
Colors @ 1280 x 1024	–	16 (Interlaced)	16 (Interlaced)	256 (Interlaced)	256 (Interlaced)
Video Overlay					
Video Overlay with 'Color Key'	–	✓	✓	✓	✓
Color Key Mask	–	–	✓	✓	✓

Table B16–1. CL-GD542X Family Differences *(cont.)*

Item	GD5420	GD5422	GD5424	GD5426/'28	GD5429
Video Overlay *(cont.)*					
VAFC Baseline Compliance	–	–	–	–	✓
GENLOCK Support	–	–	–	–	✓
Performance Enhancement					
Graphics Cursor	32 x 32	32 x 32, 64 x 64	32 x 32, 64 x 64	32 x 32, 64 x 64	32 x 32, 64 x 64
Local Bus	–	–	✓	✓	✓
BitBLT Engine	–	–	–	✓	✓
Performance Tuning	–	–	✓	✓	✓
Miscellaneous					
True Color DAC	–	✓	✓	✓	✓
Signature Generator	–	✓	✓	✓	✓
Programmable MCLK	–[b]	–[b]	✓	✓	✓
Maximum Pixel Rate	75 MHz	80 MHz	80 MHz	80 MHz	86 MHz

a. If the CL-GD5420 is configured for 1024K bytes of display memory, it can support 1024 x 768 x 256 colors in Interlaced mode only.
b. CL-GD5420-75QC-B and CL-GD5422-80QC-C have programmable MCLK.

2. DRAM UPGRADES

The following table indicates the amount of DRAM of each DRAM type that can be supported by each family member. For each DRAM type, a common layout can be used. If the chip supports only a limited number of DRAMs, the other DRAM positions will be left un-populated.

Table B16–2. DRAM Upgrade

DRAM Configuration	GD5420	GD5422	GD5424	GD5426/'28	GD5429
256K x 4	2, 4, or 8	4 or 8	4 or 8	4 or 8	4 or 8
512K x 8	2	-	-	4	4
256K x 16 Symmetric Dual WE*	1	1 or 2	1 or 2	1, 2, or 4	1, 2, or 4
256K x 16 Symmetric Dual CAS*	–	1 or 2	1 or 2	1 or 2	1 or 2

Table B16–2. DRAM Upgrade

DRAM Configuration	GD5420	GD5422	GD5424	GD5426/'28	GD5429
256K x 16 Asymmetric Dual WE*	1	1 or 2	1 or 2	1, 2, or 4	1, 2, or 4

3. SOFTWARE CONSIDERATIONS

A common BIOS is provided for CL-GD5422/'24/'26/'28/'29. To take advantage of the BitBLT engine, there are different drivers for the CL-GD5426/'28/'29. The CL-GD5420 shares the BIOS and drivers with the CL-GD5402.

4. LOCAL BUS CONSIDERATIONS

For a local bus application, only the CL-GD5424/'26/'28/'29 should be considered. However, to take advantage of the BitBLT engine in an ISA or MicroChannel bus application, it is possible to upgrade from the CL-GD5422 to a CL-GD5426/'28/'29.

Appendix B17

P-WELL/N-WELL Layout Considerations

Application Note

P-WELL/N-WELL LAYOUT CONSIDERATIONS

1. INTRODUCTION

This application note discusses video-clock filter components and layout changes for the CL-GD542X family of VGA controllers. The current video-clock filter is designed for a silicon process known as the 'P-WELL' substrate. The changes recommended in this application note are for CL-GD542X controllers that have been manufactured with either the 'P-WELL' or 'N-WELL' process. The CL-GD5420 and CL-GD5402 VGA controllers manufactured using the P-WELL can still be obtained, though the N-WELL is preferred for future designs. A board layout can be designed to accommodate either the N-WELL or P-WELL process. CL-GD5424/'26/'28/'29 will only ever be supplied in N-WELL material. Boards intended for these devices should make provisions for N-WELL only.

2. P-WELL VERSUS N-WELL PROCESS

The P-WELL process has been used for manufacturing all CL-GD5402, CL-GD5420, and CL-GD5422 devices. However, the need for faster operation and low-power consumption requires that all future CL-GD542X and CL-GD5402 devices be manufactured using the N-WELL process. Internal to the device, the P-WELL process uses the silicon substrate as the conductor for VDD. In contrast, the N-WELL process uses the substrate as the conductor for VSS. The internal VCO relies on a variable-voltage difference between it and the substrate to generate the desired video clock frequency. Using the N-WELL process gives a finer control of this difference when using higher frequencies.

2.1 Identifying P-WELL and N-WELL Devices

The following table indicates which devices are P-WELL and N-WELL.

Table B17–3. P-WELL, N-WELL Product

Device Order Number	Processing	Note
CL-GD5401-42QC-B	P-WELL	
CL-GD5402-65QC-B	P-WELL	Product obsolete Not recommended for new designs
CL-GD5402-75QC-C	N-WELL	Product obsolete Not recommended for new designs
CL-GD5420-65QC-A	P-WELL	Product obsolete Not recommended for new designs
CL-GD5420-75QC-B	N-WELL	Product obsolete Not recommended for new designs
CL-GD5420-75QC-C	N-WELL	

Table B17–3. P-WELL, N-WELL Product

Device Order Number	Processing	Note
CL-GD5422-75QC-A	P-WELL	
CL-GD5422-80QC-C	N-WELL	Product obsolete Not recommended for new designs
CL-GD5422-80QC-D	N-WELL	
CL-GD5424	N-WELL	All
CL-GD5426	N-WELL	All
CL-GD5428	N-WELL	All
CL-GD5429	N-WELL	All

3. RECOMMENDED CHANGES

For optimal operation, circuit designs using CL-GD542X and CL-GD5402 devices based on N-WELL process must provide a well-filtered VDD source and a means of selecting either VDD or VSS for the video-clock filter.

3.1 VDD Filter Change

Higher video clock frequencies require a well-filtered VDD source. This can be accomplished by changing the value of the 33-Ω resistor, 10-µF and 0.1-µF capacitors, or any other method that will provide a well-filtered VDD. Modifying the VDD filter to use ferrite beads is not recommended. The circuit also shows a VFILTER network comprising of a 75-Ω resistor, and C13 and C17 capacitors. For improved high-frequency noise rejection, the value of the C13 capacitor can be varied from 2.2 µF to 1.0 µF, and the value of the C17 capacitor from 0.1 µF to 0.03 µF. Reommended values are 2.2 µF and 0.1 µF.

3.2 Layout Change

The VFILTER design layout should accommodate either an N-WELL or P-WELL device. The design layout below shows how the VFILTER circuit is configured for this dual purpose. If an N-WELL device is used, capacitors C38 (C13A in some designs) and C39 (C17A in some designs) are installed instead of C13 and C17. For a P-WELL device, install capacitors C13 and C17. Note that the 75-Ω resistor and the VFILTER, AVSS1, and AVDD1 connections are common to either device type.

NOTE: For an N-WELL connection, the polarity of C38 (C13A) is *opposite* that of C13 for a P-WELL connection.

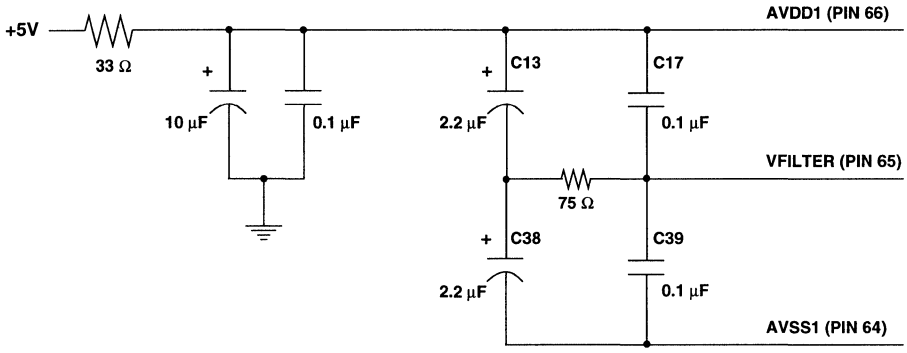

Figure B17–1. VFILTER Design Layout

Appendix B18

Manufacturing Test
Application Note

MANUFACTURING TEST

1. MANUFACTURING TEST PROGRAM

1.1 Specifications and Operating Instructions

The Manufacturing Test Program (MFGTST.EXE) provides the ability to visually and programmatically verify correct operation of the CL-GD542X family. Primary features include write/read/compare tests of all video register groups, write/read/compare tests of all video RAM, display patterns for visual verification of all primary video modes, as well as a complete set of miscellaneous video tests designed to verify proper operation of the video chip. All RAM and register tests are self-checking to the extent that values will be read and compared to expected values. When a difference is detected, an error message will be generated. All display patterns (except for signature testing) must be visually inspected to verify proper operation.

The program also detects chip type and automatically configures itself to run all valid tests for the video chip installed in the system. For example, if a CL-GD5422 is installed in the system, the program automatically sets internal menus and external command-line options to run CL-GD5422-specific tests. In all cases where a particular test is chip-specific, the program senses and records it.

The operating mode of the test program may be selected from display-menu options, or may be specified with command-line parameters. This overview details the user interface and operation of the test program.

1.2 Using the MFGTST Menu-Driven Interface

At the DOS prompt type:

```
MFGTST /m  [Enter]
```

When the '/m' option is selected, the user is in Menu mode (after the initial Cirrus Logic logo screen). From these menus, the user may select from a variety of register, display, or miscellaneous video tests. To select a test, the up, down, left, or right arrow keys are used to change the currently highlighted selection. Optionally, a "point and shoot" interface may be used if a mouse driver has been loaded. When the desired selection is highlighted, press the Enter key to execute the test. The ESC key always terminates a test, as well as the program when at the main menu. The following section lists and discusses tests available while in Menu mode.

1.2.1 Register Tests

- Memory tests, for current Video RAM installed in the video system
- Input Status Register 1 test (Sync bits)
- Sequencer register tests
- CRTC register tests
- Graphics Controller register tests

- Attribute Controller register tests
- Miscellaneous Output register test
- Feature Control register test
- DAC State register test
- PEL Mask register test
- DAC Palette register tests
- Extended register tests
- DAC Comprehensive Test

All registers that are both writable and readable are tested by writing bit patterns to the register and then reading the same register. The result of the read operation is compared with the expected result. If a difference is detected, an error message is generated. If reserved bits are defined for a register, they are not included in the write pattern (i.e., they are excluded from the compare). An extra test insures that if ones are written to any reserved bits, they remain set to zeros in the read value.

The test patterns used for the write operation are derived from the loop count. Write values range from 0 to 255 (all possible bit patterns). When an error occurs, the loop does not abort. The error bits are recorded, and the register test continues. When all bit patterns have been written, the bit errors are analyzed. Information regarding bits that appear to be stuck high or stuck low are included in the error message that is generated.

If multiple compare errors occur on a single register, a count of bad registers is incremented by one, even though the total number of compare errors is greater than one. For example, if a register has one bit stuck low (0), the bad register is incremented (to 1), and the total number of compare errors will be 128. These statistics will be displayed in a summary, if the Verbose mode (option '/v') was specified at the command line at program execution.

In addition to write/read/compare tests, Write Protection register tests are also performed. If Write Protect registers can be modified while locked, an error will be generated. Finally, the display enabled, and Vertical Retrace bits in the Input Status Register 1 are verified to ensure that they toggle between active video and retrace states.

First Mbyte Video Memory Test performs a write/read/compare loop on the first Mbyte of display memory. Before the memory test begins, the video chip is configured for a Packed-pixel mode. Using Write mode 2, all planes are written with a pre-selected test pattern (color). This value is loaded into the Color Compare register. Using Read mode 1, the entire memory address space is read (and compared) against the write value. If all pixels do not compare successfully, an error will be generated. When an error has been detected, RAM locations above the error location are not checked, that is, an error is only generated for the first faulty location. The RAM test verifies 16 different test patterns written to the video memory.

Video Memory Test 2 uses Write mode 0 in an appropriate Video mode, where the test patterns are written to and read back from video RAM directly. If the write value is different when read back, an error will be generated.

When running the test from the command line, all tests listed above are run as a complete set. Individual register tests may only be selected while in Menu mode.

1.3 Display and Miscellaneous Tests

- 80-column Text mode 3 test pattern
- 80-column Text mode 3 test (8 pages)
- 80 column Text mode 7 test pattern
- 40 column Text mode 1 test pattern
- 320 x 200 Graphics mode 4 test pattern
- 640 x 200 Graphics mode 6 test pattern
- 640 x 350 Graphics mode 10h test pattern
- 640 x 480 Graphics mode 12h test pattern
- 640 x 480 Graphics mode 11h test pattern
- 320 x 200 Graphics mode 13h test pattern
- VGA graphics standard 256-color palette test pattern
- Extended Video mode patterns (See Tables 4-1 and 4-2 in chapter 3, Data Book. Note that not all video modes are available on all chip/memory configuration combinations.)
- Rotate DAC test pattern
- 512-character set test
- Pan and scroll test
- Split-screen test
- 360 x 480 x 256 non-standard VGA mode test pattern
- Summing-to-Grayscale test
- 12-rows x 80-columns Text mode test
- Text mode scanline test (200, 350, or 400 scanlines)
- Reset DAC, display static screens
- Hardware Graphics Cursor tests
- Write mode Tests
- x8 and x16 Addressing Tests, Latches
- Signature Generator tests
- Signature Generator output
- BitBLT Tests
- Non-standard mode 71h @ 65 MHz through 95 MHz DLCK

1.4 Miscellaneous Test Descriptions

1. **Rotate DAC Test Pattern:** In this test, the DAC is reset to a color spectrum and then slowly rotated from right to left. The spectrum is rotated on the register-level only. For example, the color in register 1 is loaded into register 0, and the color in register 0 is loaded into register 255, and so on. Once the pattern is first drawn to memory, no other writes to memory are made. The test is run in mode 13h (320 x 200 x 256 colors). If colors seem to remain stationary (not rotated) or migrate in an unusual manner, this may indicate a chip-level problem.
2. **512-Character Test:** In this test, both a 9 x 16 character set (left side) and 8 x 8 character set (right side) are displayed simultaneously in mode 3. This is accomplished by loading two 256-character sets into Memory Plane 2. Sequencer register 3 is then set to select character sets 0 and 1. This enables Character Attribute bit 3 to select between the first or second set when writing characters to the display.
3. **Pan and Scroll Test:** By setting and continually updating several CRTC registers, it is possible on a standard VGA to achieve a smooth pan and scroll of the display. The logical width of the display in this case must be larger than the display screen itself to permit horizontal scrolling. The text 'PANNING AND SCROLLING TEST,' with normal VGA operation, should pan and scroll from the lower right-hand corner of the screen to the upper left-hand corner of the screen and stop.
4. **Split-screen Test:** In this test, the display is split into two pieces, upper and lower. The upper portion of the screen remains stationary, while the lower portion is slowly scrolled up over the upper, and then scrolled down, out of sight. A split screen on a standard VGA can be achieved by adjusting the Line Compare and Start Address CRTC registers.
5. **360 x 480 x 256 Non-standard VGA Mode Test Pattern:** It is possible on standard VGA hardware to create a graphics mode that is 360 x 480 x 256 colors (using only the standard VGA 28-MHz dot clock). This mode is currently supported in many major software packages. This display pattern verifies correct operation of this non-standard VGA mode.
6. **Summing-to-Grayscale Test:** Grayscale summing (summing color values to their grayscale equivalents, 256 colors to 64 shades of gray) is verified in this test. The pattern is the same one displayed in the 256-color palette test, only in this case, the colors are summed to grayscale.
7. **12 x 80 Text Mode Test:** It is possible in mode 3, to display a 'stretched' 8 x 16 character (pseudo 8 x 32) by performing the following:
   a) Set character font to 200 scanlines.
   b) Set mode 3, to allow 200-scanline option to take effect.
   c) Set an 8 x 16 character font on.
   This test verifies this hidden standard VGA feature.
8. **Select Scanlines Test:** This test displays mode 3 in 200, 350, and 400 scanlines.
9. **Reset DAC, Display Static Screens:** The DAC is reset to a color spectrum in the first screen as well as an RGB gradient in the second screen. Both screens are displayed in VGA mode 13h (320 x 200 x 256 color).
10. **Hardware Graphics Cursor Tests:** The Hardware Cursor is used in 16-color planar and 256-color Packed-pixel modes to provide a pointer for graphical user interfaces. A Hardware Cursor (mouse pointer) will improve performance because the screen data will

not have to be rewritten when the cursor is moved; it will improve the appearance of the screen by providing a smoothly moving cursor. The cursor is a 32 x 32 or 64 x 64 (CL-GD5422/'24/'26/'28/'29 only) pixel array of two planes. The following tests are performed on both the 32 x 32 and 64 x 64 Hardware Cursor:

a) **Pattern Address Tests:** The 32 x 32 cursor has space for 64 possible patterns that can be loaded into video memory and made available to any graphical application, while the 64 x 64 cursor has a possible space for 16 patterns. This test loads the maximum possible number of patterns into memory, and displays each pattern on the screen.

b) **Cursor Attribute Tests:** It is possible (with the Hardware Cursor) to set foreground and background colors for the cursor that are independent of the colors stored in the standard palette DAC. This test verifies the correct operation of Hardware-cursor Colors 0 and 1.

c) **Cursor Attribute Tests (inverted):** This test verifies the correct operation of the Hardware Cursor when programmed for Inverted mode.

d) **Cursor X/Y Position Test:** To ensure proper positioning of the graphics cursor on the screen, the Hardware Cursor in this test is moved across the screen from the top right-hand corner to the bottom left-hand corner. All Hardware Cursor tests are performed while in VGA mode 12h.

11. **Write Mode Tests:** Write mode 1 as well as Extended Write modes 4 and 5 are tested in BY8 and BY16 addressing, fill, scroll, and color expansion tests. Tests are also performed on the 4-byte and 8-byte-wide latches. The following tests are available:

a) Write mode 1, standard addressing and latches (mode 5FH) with scroll.

b) Write mode 1, BY8 addressing, 8-byte-wide data latches (mode 5FH) with scroll.

c) Write mode 4, BY8 addressing (mode 5FH) Fill Test.

d) Write mode 4, BY8 addressing (mode 5FH) Mask Tests (2 screens).

e) Write mode 5, BY8 addressing (mode 5FH) Mask Tests (5 screens).

f) Write mode 4, Text Write Test, BY8 addressing (mode 5FH).

g) Write mode 5, Text Write Test, BY8 addressing (mode 5FH).

h) Write mode 4 Fill, Write mode 1 Scroll, with 8-byte-wide latches (mode 5FH).

i) Write mode 4 Monochrome Bitmap Conversion Test (mode 5FH).

j) Write mode 0, with Raster Op's (GR3), 4 screens in mode 13H.

k) Write mode 0, Data Rotator Test (GR3), 8 screens.

l) Write mode 1, 8-byte wide data latches (mode 64H) with scroll.

m) Write mode 4, BY16 addressing (mode 64H) Fill Test.

n) Write mode 4, BY16 addressing (mode 64H) Mask Tests (2 screens).

o) Write mode 5, BY16 addressing (mode 64H) Mask Tests (5 screens).

p) Write mode 4, Text Write Test, BY16 addressing (mode 64H).

q) Write mode 5, Text Write Test, BY16 addressing (mode 64H).

r) Write mode 4 Fill, Write mode 1 Scroll, with 8-byte-wide latches (mode 64H).

s) Write mode 4 Monochrome Bitmap Conversion Test (mode 64H).

NOTE: At the time of this publication, plans are underway to add other Write mode tests, which will include tests for the other CL-GD545X family-specific features.

12. **Signature Generator Tests** (Not for the CL-GD5420)**:** To automatically test CL-GD542X video-output logic at full speed, Signature Generator (SG) logic was added to the IC. The SG uses a 16-bit CCITT-standard Cyclic Redundancy Check (CRC) algorithm, commonly used in data communications to ensure the integrity of large blocks of data. The SG operates on the Pixel Data P[7:0] over the active display time of a video frame. In the case of interlaced modes, the SG operates over one full video-refresh cycle of an odd and an even frame. The data from one bit at a time of the Pixel Data bus is used by the SG to produce a unique signature for any given mode setup or video memory data. By storing known good values, the Manufacturing Test samples signatures from a set of display patterns, and compares the known signatures to the newly sampled signatures. If both match, then the screen is said to be correct. If a mismatch occurs, then a problem may exist in the VGA hardware or firmware. This allows the user to automatically test screen data without having to visually inspect a screen for error (which can be complicated, especially in High-color and True Color modes). The CCITT CRC is designed to run on a serial bit stream. The SG has a 3-bit control field to select which bit of the Pixel Data bus to run through the CRC on each frame. Checking the entire Pixel Data bus requires that a signature be taken for each Pixel Data Bus bits, or eight signatures per screen. Running one signature per Pixel Data Bus bit helps pinpoint the cause of a failure, since seven of the SG runs may be good and only one fail; isolating the problem to a subset of the IC pins and/or memory is achievable.

    Using most of the manually viewed screens as input, signatures are captured and compared for possible errors. In operations where speed of testing is of the essence as well as eliminating human error, signature testing takes the place of the visual inspection of display screens; in most cases, it would be the most desirable and accurate way to test a Video mode.
13. **Signature Generator Output** *(Except the CL-GD5420)*: This option displays the eight signatures captured for each screen tested. This information can be used to determine where a possible problem may exist within the IC.

14. **BitBLT tests:** The following BitBLT tests are available that test all the basic BitBLT functions of the CL-GD545X family.
    a) Screen-to-screen, mode 5FH
    b) Screen-to-screen with Overlap, mode 5FH
    c) Large BitBlt, mode 5FH
    d) Large BitBlt, mode 64H
    e) Large BitBlt, mode 71H
    f) Full-screen BitBlt, mode 5FH
    g) Screen-to-off-screen-to-screen
    h) System-to-screen (9 x 4 boxes)
    i) System-to-screen (160 x 120 boxes)
    j) Pattern Copy, 8-bits (mode 5FH)
    k) Pattern Copy, 16-bits (mode 64H)
    l) Screen-to-system (160 x 120 box)
    m) Pattern Copy with Color Expand, 8-bit
    n) Pattern Copy with Color Expand, 16-bit

NOTE: At the time of this publication, plans are underway to add other CL-GD545X-family-specific BitBLT tests. These tests will be added in future updates to the Manufacturing Test and its documentation.

15. **Non-standard Mode 71H @ 65 MHz through 95 MHz:** This test allows the user to reset mode 71H from its default dot clock setting of 75 MHz to non-standard values in the range given above. The MHz values are selected by using the left and right arrow keys while the test pattern is visible on screen. When a new value is selected, the dot clock is reprogrammed and the resulting screen is adjusted.

1.5 Running MFGTST from the Command Line

Running the Manufacturing Test with no parameters simply runs all standard tests. The following options are available from the command line:

/h	Displays a help screen while in DOS (/? also accepted); a brief, one screen list of valid command line options are shown. No tests are run.
/m	Runs the program in Menu mode, as described above.
/x	Runs all self-checking tests only (register tests); this option does not display test patterns or miscellaneous tests.
/n	Runs all display pattern tests only; this option does not run self-checking register and video RAM tests
/d<n>	Maximum time each test pattern is displayed. the default is to wait indefinitely until a key is pressed. If <n> is not specified, default <n> is 1 second. The maximum delay is 9.
/v	Generates detailed messages on test status. Additional test information in Verbose mode is displayed for self-checking tests. Successful completion messages are generated in addition to any error messages.
/q	Do not display messages to standard output (con:); no test messages will be output to the display in Quiet mode.
/e<n>	Number of errors permitted before program aborts; the maximum number of bad register/RAM locations that will be tolerated before the program terminates (default is 1). The actual number of compare errors (on a single register/RAM location) may be higher than this number.
/w	Pause after error message (until any key pressed).
/r<n>	Number of test passes; default <n> = 1;
/c<n>	Send message output to com<n>, default <n> = 1; <n> specifies the port to be used, and may range from 1 to 4.
/p<n>	Send message output to lpt<n>, default <n> = 1; LPT1, LPT2, or LPT3 may be selected with <n> set to 1, 2, or 3.
f <path name>	Send message output to disk file, <path name> name of file, default =<path name> \video.rpt. This is in addition to the screen output, unless the /q option has been specified. The file name may be a fully qualified (path) file name. If <path name> is not specified, the default file ~video.rpt is used. This parameter must be the last item on the command line, when several options are grouped together (e.g., /vsf err.rpt).

/+	Runs extended miscellaneous tests along with standard tests; this is a lengthy test set and should only be used when the most complete comprehensive test suite is desired.
/s	Runs signature testing on selected video screens (except the CL-GD5420)
/u	User-defined test scripts option: Syntax: C:>mfgtst /u<path scriptfilename> This option runs the Manufacturing Test from the command line with a user-defined script file, instead of using the default tests and test order. If this option is not used, the normal default tests and order will be used during command line run. When the script option is active, the following command line options are suppressed: '/s', '/n', and '/x'. A sample script file is available (SCRIPT.MFG) which has all the current test options available in the form of string input to the program. Only one test string may occupy a line in the script file. The script file may have any name, and may be used as many times as needed. Tests may also be in any order. While this option is active, Verbose mode ('/v') is always turned on.

NOTE: Strings in the script file must be written exactly as those shown in the sample script file. If the strings are altered, MFGTST.EXE will not recognize the test and will pass it over and go on to the next test command in the script file.

1.6 Command Line Examples

1) MFGTST /sv	This execution invokes the Self-checking register and RAM tests only. No test patterns or miscellaneous tests are displayed. Verbose mode displays messages to the display screen indicating successful test completion.
2) MFGTST /s /v	Same as example 1.
3) MFGTST -sv	Same as example 1.
4) MFGTST /nd	The display patterns are run with a maximum delay of 1 second between each screen, or until a key is pressed. No self-checking tests are run.
5) MFGTST /f error.rpt	Message output is sent to file error.rpt in addition to the display.
6) MFGTST /d 3	ILLEGAL parameter, this must be specified as /d3, as well as any other command-line parameter that has <n> as a sub-parameter.

1.7 Manufacturing Test Updates

The Manufacturing Test is constantly updated. As more and more products are added to the Cirrus Logic family of graphics controllers, more tests are added to the Manufacturing Test Software to support new functions and features of our current and future products. Contact Cirrus Logic, Inc., for up-to-date Manufacturing Test Software and documentation.

OEMs can download the latest Manufacturing Test from the Cirrus Logic Bulletin Board Service at (510) 440-9080.

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Appendix B19

DRAM Timing Calculations Application Note

DRAM TIMING CALCULATIONS

1. INTRODUCTION

This application note discusses DRAM timing for the CL-GD542X family. Included is a table (Table B19–1) that calculates the available times for various MCLK frequencies. Standard RAS* timing and extended RAS* timing are both covered. Next, Table B19–4 shows the same parameters from data sheets of various DRAMs. Finally, an example shows how the data from the two tables can be combined.

2. MCLK FREQUENCIES

Table B19–1 evaluates the parameters in Table 7–29 of the CL-GD542X Data Book (Chapter 3) for various values of SR1F[4:0]. For each value of SR1F[4:0], the frequency and period of MCLK is calculated. Then each parameter in Table 7–29 is evaluated. The resulting numbers are the DRAM requirement for that MCLK frequency. Table B19–1 also shows MCLK values above 50 MHz, for reference only. Only the CL-GD5429 is specified for an MCLK above 50 MHz. The columns corresponding to frequencies that can be selected without programming SR1F are in **bold**.

NOTE: The numbers is this table are the results of calculations. You should measure the signals at the DRAMs in your environment with your layout, damping resistors, and capacitive loading.

Table B19–1. MCLK Frequencies

	SR1F[4:0] (hex):	15	16	17	18	19	1A	1B	1C	1D	1E	1F	20	21
	Frequency (MHz):	**37.6**	39.4	**41.2**	43.0	**44.7**	46.5	48.3	**50.1**	51.9	53.7	55.5	57.3	59.1
	Period (ns):	**26.6**	25.4	**24.3**	23.3	**22.3**	21.5	20.7	**20.0**	19.3	18.6	18.0	17.5	16.9
	Period/Two:	**13.3**	12.7	**12.1**	11.6	**11.2**	10.7	10.3	**10.0**	9.6	9.3	9.0	8.7	8.5
t_1	t_{ASR}: Address setup to RAS*	**37.9**	36.1	**34.4**	32.9	**31.5**	30.2	29.0	**27.9**	26.9	25.9	25.0	24.2	23.4
t_2	t_{ASC}: Address setup to CAS*	**25.6**	24.4	**23.3**	22.3	**21.3**	20.5	19.7	**19.0**	18.3	17.6	17.0	16.5	15.9
t_3	t_{RCD}: RAS* to CAS* (Standard RAS*)	**64.5**	61.5	**58.7**	56.2	**53.9**	51.7	49.7	**47.9**	46.2	44.6	43.1	41.7	40.3
t_3	t_{RCD}: RAS* to CAS* (Extended RAS*)	**77.8**	74.2	**70.9**	67.8	**65.0**	62.5	60.1	**57.9**	55.8	53.9	52.1	50.4	48.8
t_4	t_{RAH}: Row Address Hold	**39.9**	38.1	**36.4**	34.9	**33.5**	32.2	31.0	**29.9**	28.9	27.9	27.0	26.2	25.4
t_5	t_{CAH}: Column Address Hold	**26.6**	25.4	**24.3**	23.3	**22.3**	21.5	20.7	**20.0**	19.3	18.6	18.0	17.5	16.9
t_7	WE* Inactive to OE* Active	**37.9**	36.1	**34.4**	32.9	**31.5**	30.2	29.0	**27.9**	26.9	25.9	25.0	24.2	23.4

Table B19–1. MCLK Frequencies *(cont.)*

	SR1F[4:0] (hex):	15	16	17	18	19	1A	1B	1C	1D	1E	1F	20	21
t_8	t_{RAC}: RAS* Access (Standard RAS*)	**105.4**	100.6	**96.2**	92.1	**88.4**	85.0	81.8	**78.8**	76.1	73.5	71.1	68.8	66.7
t_8	t_{RAC}: RAS* Access (Extended RAS*)	**118.7**	113.3	**108.3**	103.8	**99.6**	95.7	92.1	**88.8**	85.7	82.8	80.1	77.6	75.2
t_9	t_{CAC}: CAS* Access (MAX)	**29.6**	28.4	**27.3**	26.3	**25.3**	24.5	23.7	**23.0**	22.3	21.6	21.0	20.5	19.9
t_{10}	t_{AA}: Column Address Access (MAX)	**53.2**	50.8	**48.6**	46.6	**44.7**	43.0	41.4	**39.9**	38.5	37.2	36.0	34.9	33.9
t_{12}	t_{RP}: RAS* Precharge (Standard RAS*)	**64.5**	61.5	**58.7**	56.2	**53.9**	51.7	49.7	**47.9**	46.2	44.6	43.1	41.7	40.3
t_{12}	t_{RP}: RAS* Precharge (Extended RAS*)	**79.8**	76.2	**72.9**	69.8	**67.0**	64.5	62.1	**59.9**	57.8	55.9	54.1	52.4	50.8
t_{13}	t_{RC}: Random Cycle (Standard RAS*)	**159.6**	152.4	**145.8**	139.7	**134.1**	128.9	124.2	**119.7**	115.6	111.7	108.1	104.8	101.6
t_{13}	t_{RC}: Random Cycle (Extended RAS*)	**186.2**	177.8	**170.0**	163.0	**156.4**	150.4	144.9	**139.7**	134.9	130.4	126.2	122.2	118.5
t_{14}	t_{RCH}: Read Command Hold	**8.3**	7.7	**7.1**	6.6	**6.2**	5.7	5.3	**5.0**	4.6	4.3	4.0	3.7	3.2
t_{17}	t_{CP}: CAS* Precharge	**20.6**	19.4	**18.3**	17.3	**16.3**	15.5	14.7	**14.0**	13.3	12.6	12.0	11.5	10.9
t_{18}	t_{CWL}: WE Active to CAS*	**28.6**	27.4	**26.3**	25.3	**24.3**	23.5	22.7	**22**	21.3	20.6	20.0	19.5	18.9
t_{19}	t_{WCH}: WE Active Hold	**39.9**	38.1	**36.4**	34.9	**33.5**	32.2	31.0	**29.9**	28.9	27.9	27.0	26.2	25.4
t_{20}	t_{WP}: WE Pulse Width	**64.5**	61.5	**58.7**	56.2	**53.9**	51.7	49.7	**47.9**	46.2	44.6	43.1	41.7	40.3
t_{21}	t_{DS}: Data Setup to CAS*	**24.6**	23.4	**22.3**	21.3	**20.3**	19.5	18.7	**18.0**	17.3	16.6	16.0	15.5	14.9
t_{22}	t_{DH}: Data Hold from CAS*	**27.6**	26.4	**25.3**	24.3	**23.3**	22.5	21.7	**21.0**	20.3	19.6	19.0	18.5	17.9
t_{23}	t_T: Transition Time	**2.0**	2.0	**2.0**	2.0	**2.0**	2.0	2.0	**2.0**	2.0	2.0	2.0	2.0	2.0
t_{25}	t_{RAS}: (Standard RAS*)	**93.1**	88.9	**85.0**	81.5	**78.2**	75.2	72.4	**69.8**	67.4	65.2	63.1	61.1	59.3
t_{25}	t_{RAS}: (Extended RAS*)	**104.4**	99.6	**95.2**	91.1	**87.4**	84.0	80.8	**77.8**	75.1	72.5	70.1	67.8	65.7
t_{26}	t_{CAS}: CAS*	**29.6**	28.4	**27.3**	26.3	**25.3**	24.5	23.7	**23.0**	22.3	21.6	21.0	20.5	19.9
t_{27}	Read Data to CAS* High	**0.0**	0.0	**0.0**	0.0	**0.0**	0.0	0.0	**0.0**	0.0	0.0	0.0	0.0	0.0
t_{28}	Read Data from CAS* High	**10.0**	10.0	**10.0**	10.0	**10.0**	10.0	10.0	**10.0**	10.0	10.0	10.0	10.0	10.0
t_{29}	t_{PC}: Page-mode Cycle	**53.2**	50.8	**48.6**	46.6	**44.7**	43.0	41.4	**39.9**	38.5	37.2	36.0	34.9	33.9

3. STANDARD RAS* VS. EXTENDED RAS*

In Table B19–1, there are five pairs of parameters that are calculated twice — once for six-MCLK random cycles and once for seven-MCLK random cycles. RAS* timing is controlled by CF[12]. A summary is listed in Table B19–2.

Table B19–2. CF[12] – RAS* Timing

CF[12]	MD27	New Name	Old Name	t_{RC}
1	No pull-down	Standard RAS* timing	Default	6-MCLK
0	Pull-down	Extended RAS* timing	High performance	7-MCLK

If a pull-down is installed, 1/2 MCLK cycle is added to the RAS* precharge period (t_{RP}) and 1/2 MCLK cycle is added to the delay between RAS* and CAS* (t_{RCD}). This allows the system designer to take full advantage of DRAM with faster relative CAS* times. The MCLK can be increased, decreasing the CAS* times (t_{CAC}, t_{PC}) while maintaining relatively long RAS* times.

There are five parameters in Table 7–29 of the CL-GD542X Data Book (see Chapter 3) that are redefined depending on which RAS* timing is selected, enumerated in Table B19–3 below.

Table B19–3. New Timing Definitions

Symbols	Parameter	Standard	Extended
t_3	t_{RCD}: RAS* to CAS*	2.5t - 2 ns	3t - 2 ns
t_8	t_{RAC}: Data from RAS*	4t - 1 ns	4.5t - 1 ns
t_{12}	t_{RP}: RAS* Precharge	2.5t - 2 ns	3t
t_{13}	t_{RC}: Random Cycle	6t	7t
t_{25}	t_{RAS}: RAS* Pulse Width	3.5t	4t - 2 ns

There is a decrease in performance when switching from standard RAS* timing to extended RAS* timing without an accompanying increase in MCLK. If the memory is lightly loaded (as would be the case of a CL-GD5422 in an ISA bus environment), the decrease is less than 5%. If the memory is very heavily loaded (as would be the case of a CL-GD5426/'28/'29 in a VESA VL-Bus environment), the decrease can approach 20%. It is best to run the target application in the intended configuration and obtain system-specific numbers before deciding.

4. 70-NS DRAMS

Table B19–4 contains data sheet values for a number of DRAMs with 70-ns Row Access Time (t_{RAC}). Using this table, it can be determined that most of the values do not vary from vendor to vendor. The obvious exception is Page-mode Cycle Time (t_{PC}). The fastest data sheet value is for the brand 'M' 256K x 4; the slowest data sheet value is for the brand 'H' 256K x 4.

Table B19–4. 70-ns DRAMs

	Vendor:	Brand H	Brand M	Brand S	Brand H
	Part Number: Configuration: Speed:	HM514256A 256K x 4 70	MT4C4256 256K x 4 70	KM44C256B 256K x 4 70	HM514260 256K x 16 70
t_1	t_{ASR}: Address setup to RAS*	0	0	0	0
t_2	t_{ASC}: Address setup to CAS*	0	0	0	0
t_3	t_{RCD}: RAS* to CAS* (Standard RAS*)	20	20	20	20
t_3	t_{RCD}: RAS* to CAS* (Extended RAS*)	20	20	20	20
t_4	t_{RAH}: Row Address Hold	10	10	10	10
t_5	t_{CAH}: Column Address Hold	15	15	15	15
t_7	WE* Inactive to OE* Active	–	–	–	–
t_8	t_{RAC}: RAS* Access (Standard RAS*)	70	70	70	70
t_8	t_{RAC}: RAS* Access (Extended RAS*)	70	70	70	70
t_9	t_{CAC}: CAS* Access (MAX)	20	20	20	20
t_{10}	t_{AA}: Column Address Access (MAX)	35	35	35	35
t_{12}	t_{RP}: RAS* Precharge (Standard RAS*)	50	50	50	50
t_{12}	t_{RP}: RAS* Precharge (Extended RAS*)	50	50	50	50
t_{13}	t_{RC}: Random Cycle (Standard RAS*)	130	130	130	130
t_{13}	t_{RC}: Random Cycle (Extended RAS*)	130	130	130	130
t_{14}	t_{RCH}: Read Command Hold	0	0	0	0
t_{17}	t_{CP}: CAS* Precharge	10	10	10	10
t_{18}	t_{CWL}: WE Active to CAS*	20	20	20	20
t_{19}	t_{WCH}: WE Active Hold	15	15	15	15
t_{20}	t_{WP}: WE Pulse Width	10	15	15	10
t_{21}	t_{DS}: Data Setup to CAS*	0	0	0	0

Table B19–4. 70-ns DRAMs *(cont.)*

	Vendor:	Brand H	Brand M	Brand S	Brand H
	Part Number: Configuration: Speed:	HM514256A 256K x 4 70	MT4C4256 256K x 4 70	KM44C256B 256K x 4 70	HM514260 256K x 16 70
t_{22}	t_{DH}: Data Hold from CAS*	15	15	15	15
t_{23}	t_T: Transition Time	3	3	3	3
t_{25}	t_{RAS}: (Standard RAS*)	70	70	70	70
t_{25}	t_{RAS}: (Extended RAS*)	70	70	70	70
t_{26}	t_{CAS}: CAS*	20	20	20	20
t_{27}	Read Data to CAS* High	–	–	–	–
t_{28}	Read Data from CAS* High	0	0	0	0
t_{29}	t_{PC}: Page-mode Cycle	50	40	45	45

5. A COMBINED EXAMPLE

Comparing the times available (Table B19–1) with the times required (Table B19–4), the times available should be equal to or greater than the times required. As an example, Table B19–5 includes the Brand 'S' numbers with those of Table B19–1 so that the numbers can be easily compared. With an MCLK frequency of 43.0 MHz, no parameters are violated. In every case, for standard RAS* or extended RAS*, more time is available than is required.

Table B19–5. Brand 'S' DRAMs

	SR1F (Hex):	15	16	17	18	19	Brand S	1A
	Frequency (MHz): Period (ns): Period/Two:	**37.6** **26.6** **13.3**	39.4 25.4 12.7	**41.2** **24.3** **12.1**	43.0 23.3 11.6	**44.7** **22.3** **11.2**	KM44C256B 256K x 4 70	46.5 21.5 10.7
t_1	t_{ASR}: Address setup to RAS*	**37.9**	36.1	**34.4**	32.9	**31.5**	0	30.2
t_2	t_{ASC}: Address setup to CAS*	**25.6**	24.4	**23.3**	22.3	**21.3**	0	20.5
t_3	t_{RCD}: RAS* to CAS* (Standard RAS*)	**64.5**	61.5	**58.7**	56.2	**53.9**	20	51.7
t_3	t_{RCD}: RAS* to CAS* (Extended RAS*)	**77.8**	74.2	**70.9**	67.8	**65.0**	20	62.5
t_4	t_{RAH}: Row Address Hold	**39.9**	38.1	**36.4**	34.9	**33.5**	10	32.2
t_5	t_{CAH}: Column Address Hold	**26.6**	25.4	**24.3**	23.3	**22.3**	15	21.5
t_7	WE* Inactive to OE* Active	**37.9**	36.1	**34.4**	32.9	**31.5**	–	30.2
t_8	t_{RAC}: RAS* Access (Standard RAS*)	**105.4**	100.6	**96.2**	92.1	**88.4**	70	85.0

Table B19–5. Brand 'S' DRAMs *(cont.)*

	SR1F (Hex):	15	16	17	18	19	Brand S	1A
	Frequency (MHz): Period (ns): Period/Two:	**37.6** **26.6** **13.3**	39.4 25.4 12.7	**41.2** **24.3** **12.1**	43.0 23.3 11.6	**44.7** **22.3** **11.2**	KM44C256B 256K x 4 70	46.5 21.5 10.7
t_8	t_{RAC}: RAS* Access (Extended RAS*)	**118.7**	113.3	**108.3**	103.8	**99.6**	70	95.7
t_9	t_{CAC}: CAS* Access (MAX)	**29.6**	28.4	**27.3**	26.3	**25.3**	20	24.5
t_{10}	t_{AA}: Column Address Access (MAX)	**53.2**	50.8	**48.6**	46.6	**44.7**	35	43.0
t_{12}	t_{RP}: RAS* Precharge (Standard RAS*)	**71.5**	68.5	**65.7**	63.2	**60.9**	50	58.7
t_{12}	t_{RP}: RAS* Precharge (Extended RAS*)	**79.8**	76.2	**72.9**	69.8	**67.0**	50	64.5
t_{13}	t_{RC}: Random Cycle (Standard RAS*)	**159.6**	152.4	**145.8**	139.7	**134.1**	130	128.9
t_{13}	t_{RC}: Random Cycle (Extended RAS*)	**186.2**	177.8	**170.0**	163.0	**156.4**	130	150.4
t_{14}	t_{RCH}: Read Command Hold	**8.3**	7.7	**7.1**	6.6	**6.2**	0	5.7
t_{17}	t_{CP}: CAS* Precharge	**20.6**	19.4	**18.3**	17.3	**16.3**	10	15.5
t_{18}	t_{CWL}: WE Active to CAS*	**28.6**	27.4	**26.3**	25.3	**24.3**	20	23.5
t_{19}	t_{WCH}: WE Active Hold	**39.9**	38.1	**36.4**	34.9	**33.5**	15	32.2
t_{20}	t_{WP}: WE Pulse Width	**64.5**	61.5	**58.7**	56.2	**53.9**	15	51.7
t_{21}	t_{DS}: Data Setup to CAS*	**24.6**	23.4	**22.3**	21.3	**20.3**	0	19.5
t_{22}	t_{DH}: Data Hold from CAS*	**27.6**	26.4	**25.3**	24.3	**23.3**	15	22.5
t_{23}	t_T: Transition Time	**2.0**	2.0	**2.0**	2.0	**2.0**	3	2.0
t_{25}	t_{RAS}: (Standard RAS*)	**93.1**	88.9	**85.0**	81.5	**78.2**	70	75.2
t_{25}	t_{RAS}: (Extended RAS*)	**104.4**	99.6	**95.2**	91.1	**87.4**	70	84.0
t_{26}	t_{CAS}: CAS*	**29.6**	28.4	**27.3**	26.3	**25.3**	20	24.5
t_{27}	Read Data to CAS* High	**0.0**	0.0	**0.0**	0.0	**0.0**	–	0.0
t_{28}	Read Data from CAS* High	**10.0**	10.0	**10.0**	10.0	**10.0**	0	10.0
t_{29}	t_{PC}: Page-mode Cycle	**53.2**	50.8	**48.6**	46.6	**44.7**	45	43.0

With an MCLK frequency of 44.7 MHz, a single parameter would be violated. The importance of this violation must be examined on a case-by-case basis. The parameter violations are summarized in Table B19–6.

Table B19–6. Parameter Violation Summary

Symbol	Parameter	Required	Available	Difference
t_{29}	t_{PC}: Page-mode cycle	45 MHz	44.7 MHz	0.7%

Appendix B20

Memory-Mapped I/O

MEMORY-MAPPED I/O

1. INTRODUCTION

The CL-GD5429 (only) allows application programs to access the BLT-control registers as memory locations. This can be up to four times faster than using I/O accesses, particularly when multiple registers must be changed at once. The register address is implied in the address rather than being transferred as part of the data (the Index field). This doubles the data transfer rate at once. Since DWORD transfers are allowed, the data transfer rate is doubled again.

Memory-mapped I/O is enabled when SR17[2] is programmed to a '1'. GR6[3:2] must be programmed to '0,1'. This means that if the CL-GD5429 is not programmed for Linear Addressing, the window into display memory is 64K (A000:0 to AFFF:F).

If SR17[6] is programmed to a '0', a block of 256 bytes of memory address space is reserved beginning at B800:0. If SR17[6] is programmed to a '1', *and* linear addressing is enabled, a block of 256 bytes of memory address space is reserved at the end of the 2-Mbyte linear address space. In this case, the block appears at the end of the 2-Mbyte space regardless of the amount of DRAM actually installed.

Memory-mapped I/O can be done using BYTE, WORD, or DWORD cycles. Memory-mapped Read cycles are valid only for the BLT Status register (GR31). When the CL-GD5429 is configured for local bus, reads to other addresses will return LDEV# and LRDY# but the data will be indeterminate. Memory-mapped I/O can be freely intermixed with ordinary I/O.

Table B20–1 indicates the registers that are accessible using memory-mapped I/O. Alternate doublewords are shaded to make it more easy to determine which registers are grouped together by virtue of being in a common doubleword.

Table B20–1. Memory-mapped I/O Registers

Offset (Hex)	Register	Description
00	GR0	Background Color Low byte
01	GR10	Background Color High byte
02	–	Reserved
03	–	Reserved
04	GR1	Foreground Color Low byte
05	GR11	Foreground Color High byte
06	–	Reserved
07	–	Reserved
08	GR20	BLT Width Low
09	GR21	BLT Width High
0A	GR22	BLT Height Low
0B	GR23	BLT Height High
0C	GR24	BLT Destination Pitch Low
0D	GR25	BLT Destination Pitch High
0E	GR26	BLT Source Pitch Low
0F	GR27	BLT Source Pitch High
10	GR28	BLT Destination Address Low
11	GR29	BLT Destination Address Mid
12	GR2A	BLT Destination Address High
13	GR2B	Reserved
14	GR2C	BLT Source Address Low
15	GR2D	BLT Source Address Mid
16	GR2E	BLT Source Address High
17	GR2F	BLT Destination Write Mask
18	GR30	BLT mode
19	–	Reserved
1A	GR32	BLT Raster OP
1B-3F	–	Reserved
40	GR31	BLT Start/Status (R/W)
41-FF	–	Reserved

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Appendix B21

Power Management

POWER MANAGEMENT

1. INTRODUCTION

The CL-GD542X family of graphics controllers feature comprehensive PC-power management functions that support compliance with the United States Environmental Protection Agency's Energy Star Computer Program, a voluntary program that promotes energy-efficient technology for desktop computers. Compliance with the Energy Star program will be a qualification for federal government purchases of computers, monitors, and printers.

The purpose of this appendix is to describe the methods used in the CL-GD542X family to comply with Energy Star.

Some of the methods described in this appendix involve programming registers in the CL-GD542X. If the application program does reprogram registers, it *must* first save the register contents so that it can subsequently restore them. In addition, it may be necessary to unlock the extended registers.

2. DISPLAY POWER MANAGEMENT SIGNALING (DPMS)

The greatest power savings can be obtained is by putting the monitor into a low-power mode. This requires, of course, that the monitor respond to DPMS (Display Power Management Signaling).

The VESA (Video Electronics Standards Association) DPMS proposal defines four levels of display power, as shown in the following table.

Table B21–2. VESA® DPMS Proposal States

Name	Definition	HSYNC	VSYNC	Note
ON	Full operation	Active	Active	
Stand-by	Optional state of minimal power reduction	Inactive	Active	Supported by CL-GD5429 only
Suspend	Significant reduction of power consumption	Active	Inactive	
Off	Lowest level of power consumption	Inactive	Inactive	

The CL-GD542X family is compliant with the VESA Display Power Management BIOS Extensions, VBE/PM. These calls are described in the sections that follow.

2.1 Report VBE/PM Capabilities

Input:

AH = 4fh		VESA Extension
AL = 10h		VBE/PM Services
BL = 00h		Report VBE/PM Capabilities
ES:DI		Null pointer, must be 0000:0000h
		Reserved for future use

Output:

AX =		Status
BH =		Power saving state signals supported by the controller (Note 1)
		1 = supported, 0 = not supported
	Bit 0	STAND BY
	Bit 1	SUSPEND
	Bit 2	OFF
	Bit 3	REDUCED ON (intended for flat panel displays)

NOTES

1) The attached display may not support all the power states that can be signaled by the controller. It is the responsibility of the power-management program to determine the power-saving states that are offered by the controller. If the controller has means of determining which power-saving state is implemented in the attached display device, that function reports the power-saving states supported by both the controller and the display.

The CL-GD5422/'24/'26/'28 support SUSPEND and OFF. In addition, the CL-GD5429 supports STAND BY.

2.2 Set Display Power State

Input:

AH = 4fh		VESA Extension
AL = 10h		VBE/PM Services
BL = 01h		Set Display Power State
BH =		Requested Power state
	00h	ON
	01h	STAND BY
	02h	SUSPEND
	04h	OFF
	08h	REDUCED ON (intended for flat panel displays)

Output:

AX =	Status: If the requested state is not available, this function will return AX = 14h to indicate that the function is supported but the call failed. The BH register and Display Power State shall be left unchanged in this case.
BH =	Unchanged

2.3 Get Display Power State

Input: AH = 4fh VESA Extension
AL = 10h VBE/PM Services
BL = 02h Get Display Power State

Output: AX = Status: If this function is not supported by the controller hardware, AL=01 should be returned in the status.

BH = Power state currently requested by the controller
- 00h ON
- 01h STAND BY
- 02h SUSPEND
- 04h OFF
- 08h REDUCED ON (intended for flat panel displays)

3. POWER MANAGEMENT HARDWARE BITS (CL-GD5429 Only)

The CL-GD5429 has three bits in Extension register GRE that are intended for power management. These are shown in the diagram below. Note that other bits in this register may perform other functions. See Chapter 9 for a complete description of register GRE.

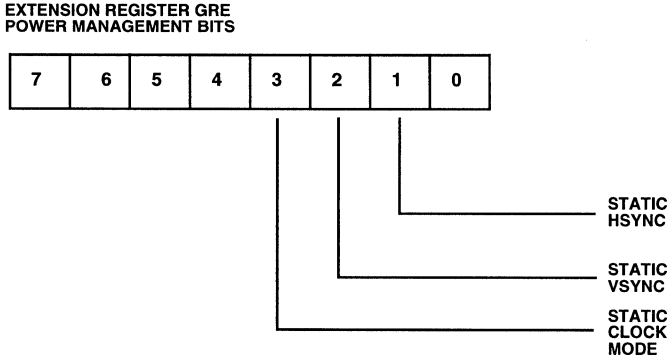

Figure B21–1. Register GRE Power Management Bits

When GRE[3] is programmed to a '1', the CL-GD5429 is switched to Static Clock mode. This does the following:

- Screen refresh is turned off
- VCLK is turned off
- MCLK is turned off. This action, along with turning off VCLK, results in zero dynamic power.
- DRAM refresh continues
- DAC is powered-down

When GRE[2] is programmed to a '1', the VSYNC output will be static. The level will be as programmed in MISC[7]. In addition, the DAC will be powered-down.

When GRE[1] is programmed to a '1', the HSYNC output will be static. This bit, in conjunction with GRE[2], provides for direct programming of the DPMS states described above. The level will be as programmed in MISC[6]. In addition, the DAC will be powered-down.

4. POWER MANAGEMENT HARDWARE BITS (CL-GD5422/'24/'26/'28)

4.1 DAC Power-Down

The DAC can be put into a power-down state by programming the Hidden DAC register to C7h. The CL-GD5429 also supports this.

4.2 Video Clock/Display Memory Refresh

The video clock can be reduced to as low as 3.46 MHz and the DRAM refresh can be reduced to 5 cycles every 4.6 μs, without losing the contents of display memory. This reduces the power in the display memory array and also reduces the power in the controller chip. The following steps are involved:

1. Divide DCLK by two and select 8 pixels-per-character
   - Program SR1 to 29h.

2. Select VCLK0
   - Program MISC[3:2] to 00h.

3. Set VCLK0 to 3.48 MHz
   - Program SR0B to 0fh.
   - Program SR1B to 3fh.

4. Unlock Horizontal Timing and select 5 refresh cycles-per-scanline
   - Program CR11 to 40h.

5. Set Horizontal Total to 14 character clocks
   - Program CR0 to 09h.

6. Set other horizontal parameters to be consistent with HTOTAL of 16
   - Program CR1 to 02h.
   - Program CR4 to 03h.
   - Program CR5 to 02h.

4.3 Memory Clock

MCLK can be reduced to as low as 7.14 MHz. This reduces the power in the chip. Program SR1F to 04h.

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Appendix C1

Software Support
Application Note

SOFTWARE SUPPORT

1. INTRODUCTION

The True Color VGA family of controllers is provided with the CL-GD542X VGA BIOS and an extensive set of utilities and software drivers. The following sections briefly describe some of the utilities and software drivers available.

To get an up-to-date list of utilities and software drivers supported, refer to the CL-GD542X True Color VGA BIOS or CL-GD542X Software Drivers Kit. The latest drivers are available on the Cirrus Logic Bulletin Board Service at (510) 440-9080 (refer to Appendix D9 for more information on the Cirrus Logic BBS).

1.1 CL-GD542X VGA SOFTWARE UTILITES

This section describes the software utilities provided with the CL-GD542X VGA Controllers, and explains the function and usage of each.

1.1.1 CLMODE — A CL-GD542X Video Mode Configuration Utility

The CL-GD542X VGA Controllers support many more video modes than the original IBM VGA. Some of these extended modes are 132-column Text modes, 800 x 600, 1024 x 768, and 1280 x 1024 x 16/256-color Graphics modes, 800 x 600 Direct-Color, and 640 x 480 True Color modes. To take advantage of these features, a compatible monitor must be installed, and the proper monitor parameters need to be selected.

The CLMODE utility provides a number of graphics configuration options, all of which are selectable from a menu or by direct keyboard input at the DOS command line. The menu options include:

- Monitor-type selection based on monitor's vertical and horizontal sync frequencies.
- Selection and setting of CL-GD542X VGA BIOS Standard and Extended Video modes.
- Extended Video Mode preview to verify high-resolution modes supported by the video subsystem.
- Selection and setting of video refresh rates for each individual video mode resolution (i.e., 640 x 480, 800 x 600, 1024 x 768, and 1280 x 1024) to match video refresh rates supported by a monitor.

1.1.2 VGA.EXE — RAMBIOS Utility

This VGA.EXE utility is an executable version of the VGA BIOS EPROM code that can be loaded into DOS memory. The VGA.EXE utility allows the VGA BIOS to be executed out of 16- or 32-bit system memory, instead of an 8-bit or 16-bit bus ROM. This permits most operations that use the VGA BIOS to run much faster.

The most noticeable performance boost is in text modes where VGA BIOS character-write and text-scrolling functions are used. Common benchmark programs that can be used to demonstrate this increase in performance are PC Bench™ from Ziff-Davis Publishing Company®, and QA Plus™ from Diagsoft®.

However, most Graphical User Interface (GUI) applications do not use the BIOS heavily, so actual performance increases vary between applications, and in some cases may not be significant.

Many of the newest '386 and '486 PCs automatically cache (copy into system memory) the VGA BIOS upon booting the machine. This is sometimes called 'Shadow RAM'. In this case, the BIOS is already executing out of 16- or 32-bit memory, and the VGA.EXE utility is not necessary.

The VGA.EXE utility can be executed from the command line or inserted in the AUTOEXEC.BAT. The utility will then automatically install itself in system memory at the correct address, shortly after power-on or a warm-boot.

The RAMBIOS utility only works with MS-DOS or PC-DOS, and does not work with OS/2™, Unix®, or Xenix®.

1.1.3 OEM System Integration (OEMSI) Utility

The OEMSI (OEM System Integration) utility enables the Cirrus Logic VGA BIOS to be customized to system requirements. Since the OEMSI operates upon the binary (executable) image of the BIOS, source code is no longer necessary for customization. Several different derivative BIOSes can easily be generated from the same core, which reduces maintenance problems and simplifies software-generation control. If OEMSI is used, the RAM BIOS should not be shipped since its use would override the changes.

A wide range of parameters, default values, and tables can easily be modified or replaced using the OEMSI program. The following components of the Cirrus Logic VGA BIOS can be modified with the OEMSI program:

Sign-on message. In addition to the Cirrus Logic copyright notices displayed when the system boots up, custom copyright messages may be inserted. The positioning of the cursor, after the copyright messages have been displayed, can also be changed.

Display-type configuration. The standard mechanism can be chosen, in which the display type is determined by reading software-configuration switches, or by a software interrupt 15H call.

Hardware Configuration Registers. The CL-GD542X VGA BIOS hardware configuration table includes register values that are programmed at POST. This allows customizing of register values that program Video Dot Clocks, Memory Clocks, and other programmable settings.

Video Mode parameter tables. These tables contain the complete set of register values for each Standard and Extended Video mode. Values for both the Standard VGA registers and Cirrus Logic Extension registers are contained in the tables.

Font tables. All fonts used by the Cirrus Logic VGA BIOS can be modified or completely replaced by using the OEMSI utility. A flexible scheme is implemented, whereby font tables can be exported from the binary image of the BIOS or imported to it.

1.1.4 SETRES Utility

The SETRES utility is a Windows application that can be used to conveniently set the resolution and number of colors of the display. It is intended primarily for end users who will be changing the resolution fairly often.

1.2 CL-GD542X VGA Software Drivers

A number of text and graphics device drivers are available to enhance the operation of VGA graphics applications.

1.2.1 Driver Applicability

The VGA graphics portion of a system needs no software drivers to run applications in Standard-resolution mode. The following drivers are provided as a service to the user for improved resolution and performance to many software packages.

Cirrus Logic recognizes that quality device drivers are an important feature of any video subsystem; therefore, our list of available device drivers is continuously expanding. Please refer to the CL-GD542X Software Drivers Kit for the latest list of available device drivers.

Table C1–1. Cirrus Logic Text and Graphics Drivers

Software Drivers	Resolution Supported*	No. of Colors
Microsoft® Windows 3.x	640 x 480, 800 x 600, 1024 x 768, 1280 x 1024 640 x 480, 800 x 600,1024 x 768, 1280 x 1024 640 x 480, 800 x 600, 1024 x 768 640 x 480	16 colors 256 colors 65,536 colors 16.8 million colors
Microsoft Windows NT V1.X	640 x 480, 800 x 600, 1024 x 768	16 and 256 colors
OS/2 V2.0, V2.1	800 x 600, 1024, x 768 640 x 480, 800 x 600, 1024, x 768	16 colors 256 colors
AutoCAD® V11, V12 Autoshade® V2.0 w/ Renderman, 3D Studio V1,V2	640 x 480, 800 x 600, 1024 x 768, 1280 x 1024 640 x 480, 800 x 600,1024 x 768, 1280 x 1024 640 x 480, 800 x 600, 1024 x 768 640 x 480	16 colors 256 colors 65,536 colors 16.8 million colors
GEM™ V3.x	800 x 600, 1024 x 768	16 colors
Ventura Publisher® V2, V3	800 x 600, 1024 x 768	16 colors
Lotus 1-2-3® V2.x,	132 x 25, 132 x 43 (text) 800 x 600	16 colors 16 colors
Lotus 1-2-3® V3.x	132 x 25, 132 x 43 (text) 800 x 600, 1024 x 768	16 colors 16 colors
Microsoft® Word® V5.x	132 x 25, 132 x 43 (text) 800 x 600, 1024 x 768	16 colors 16 colors
WordPerfect® V5.0	800 x 600	16 colors
WordPerfect® V5.1	132 x 25, 132 x 43 (text) 800 x 600, 1024 x 768	16 colors 16 colors
WordStar® V5.5 -V7.0	800 x 600, 1024 x 768	16 colors

***NOTE:** Not all monitor types support all resolutions. 640 x 480 drivers will run on PS/2-type monitors. Extended resolutions are dependent on monitor type and VGA system implementation.

Appendix D1

Extended Video Modes Programming Application Note

Table of Contents

EXTENDED VIDEO MODES PROGRAMMING

1. INTRODUCTION

The CL-GD542X family of VGA controllers is capable of supporting a wide range of Super VGA high-resolution video graphics modes. The CL-GD542X supports graphics modes of up to:

- 1280 x 1024 x 16 colors
- 1280 x 1024 x 256 colors
- 800 x 600 x 32K and 64K colors
- 640 x 480 x 16.8 million colors

The Extended VGA Video modes are described in terms of video memory organization, extended display memory addressing, and mapping schemes as supported by the CL-GD542X VGA controllers.

This application note also includes software programming examples demonstrating how to implement some of these features.

2. SUPER VGA DISPLAY MODES

The following table shows the Extended Video Graphics modes supported by the CL-GD542X:

Table D1–3. Extended Modes

Mode Number*	Resolution	Colors	Bits/Pixel	Memory Organization	Memory Required
58h, 6Ah	800 x 600	16	4	Planar	256K
5Ch	800 x 600	256	8	Packed	512K
5Dh	1024 x 768	16	4	Planar	512K
5Fh	640 x 480	256	8	Packed	512K
60h	1024 x 768	256	8	Packed	1024K
62h	640 x 480	32,768	15	RGB[a] (5-5-5)	1024K
63h	800 x 600	32,768	15	RGB[a] (5-5-5)	1024K
64h	640 x 480	65,536	16	RGB[b] (5-6-5) Packed	1024K
65h	800 x 600	65,536	16	RGB[b] (5-6-5) Packed	1024K
66h	640 x 480	32,768	15/8	Mixed[c] RGB(5-5-5)/ 256-colors Packed	1024K
67h	800 x 600	32,768	15/8	Mixed[c] RGB(5-5-5)/ 256-colors Packed	1024K
6Ch	1280 x 1024	16	4	Planar	1024K
6Dh	1280 x 1024	256	8	Packed	2048K
6Fh	320 x 200	65,536	16	RGB[b] (5-6-5) Packed	512K
70h	320 x 200	16.8 million	24	RGB[d] (8-8-8) Packed	512K
71h	640 x 480	16.8 million	24	RGB[d] (8-8-8) Packed	1024K
74h	1024 x 768	65, 536	16	RGB[b] (5-6-5) Packed	2048K

NOTES:

* Not all video modes are available on all CL-GD542X controllers. Refer to CL-GD542X Data Sheet and Software Release Kit for the list of video modes supported by the CL-GD542X BIOS.

a) The 32,768-color Video modes are RGB (5-5-5) Packed-pixel modes compatible with industry standard.

b) The 65,536 Direct-Color Video modes are RGB (5-6-5) Packed-pixel modes compatible with industry standard.

c) The Mixed format allows 32,768-color Video modes RGB (5-5-5) and 256-colors (8-bits/pixel) packed format to be combined.

d) The 640 x 480 x 16.8 million True Color Video mode with 1024K display memory is RGB (8-8-8) Packed-pixel modes compatible with 24-bit/pixel TARGA™ Truevision format.

3. 16-COLOR PLANAR MODE MEMORY ORGANIZATION

The Planar Video Memory denotes that a pixel is represented by bits of information dispersed across a set of planes. The 16-color mode requires four bits per pixel, which means four display planes have the pixel represented by one bit per plane. The display memory is organized as bytes, and there are eight pixels per byte. The memory planes are overlaid in the CPU memory address space so that each plane occupies the same CPU address. The CPU can access any of these planes independently for read/write operations by programming the appropriate select registers.

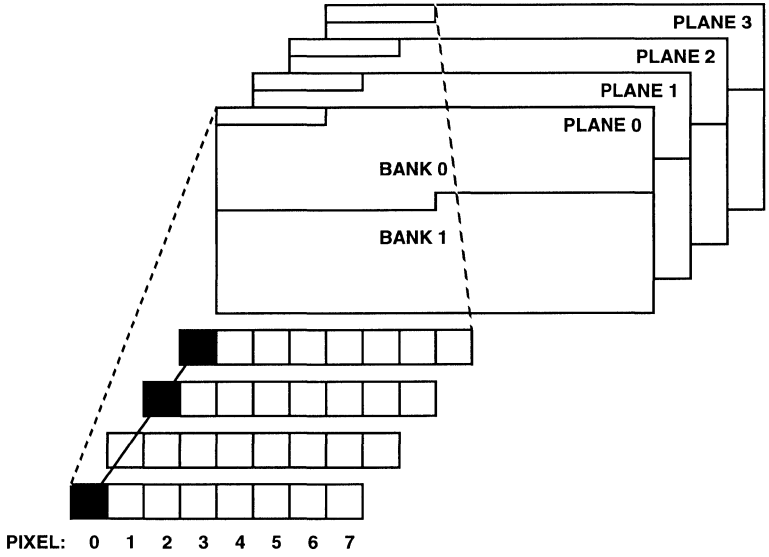

Figure D1–1. 16-Color Planar Modes

Figure D1–1 shows the video memory organized in four display planes for 16-color Planar mode. The color information for each pixel is stored in corresponding bits across four planes. The figure also depicts how Bank 0 and Bank 1 are aligned across each plane.

The standard IBM VGA supports 256K bytes of video memory. In 16-color Planar mode, the video memory is divided into four planes with 64K bytes per plane. The 64K bytes segment of each plane is mapped normally from A0000 to AFFFF, and the CPU can easily address each of the video memory planes. The problem arises for a video mode that requires more than 64K bytes of addressable video memory per plane. For example the 1024 x 768, 16-color Planar mode requires 98,304 bytes of display memory per plane, and a way to remap different segments of display memory into the CPU-limited address range. The display memory address remapping scheme is discussed in a later section.

4. 256-COLOR PACKED PIXEL MODES

The 256-color modes use eight bits (or one byte) per pixel; the term 'packed' means all information about each pixel is packed in one plane. The CL-GD542X memory controller handles all the address generation; to the CPU the display memory appears as if it were linear 64K bytes of addressable display memory. For high-resolution modes that require addressing beyond the 64K byte segment of video memory, the CL-GD542X has display memory remapping schemes to 'page-in' the display memory segments.

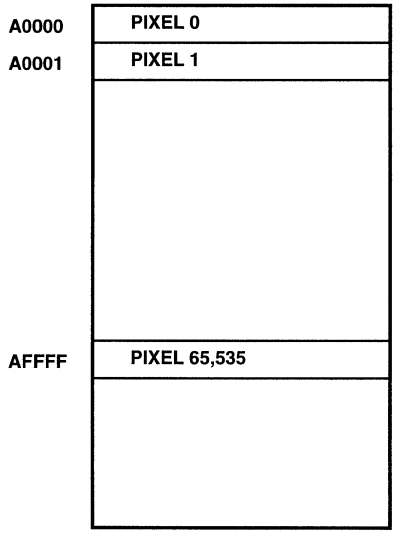

Figure D1–2. 256-Color Packed-Pixel Mode

Figure D1–2 shows how eight bits per pixel (Packed-pixel mode) bytes are stored in terms of physical plane organization. The memory controller makes this organization completely transparent; therefore to the CPU the byte addressing is sequential. For example, at Segment A000, Pixel 0 resides at offset 0, Pixel 1 at offset 1, and Pixel 65535 at offset 65535. To address display memory beyond 64K segment boundary, the CL-GD542X supports a display memory paging scheme that allows up to 1 Mbyte of display memory to be paged into the CPU address range.

5. DIRECT-COLOR (32,768 OR 65,536 COLORS), PACKED-PIXEL MODES

The CL-GD542X VGA controllers support a Direct-color mode that is capable of displaying 32,768 or 65,536 colors simultaneously at screen resolutions of up to 800 x 600. The CL-GD542X uses its internal palette DAC to support this TARGA- or IBM XGA-compatible mode, where 15 or 16 bits per pixel of color information is used to display 32,768 or 65,536 colors. The VGA-standard palette DAC LUT is limited to 256 addresses. This scheme bypasses the LUT, and passes 15 or 16 bits of RGB (RED, GREEN, and BLUE) color information directly to the DAC to generate the high-range colors. The CL-GD542X Direct-color mode displays close to true-color images on standard VGA analog monitors for desktop and multimedia applications.

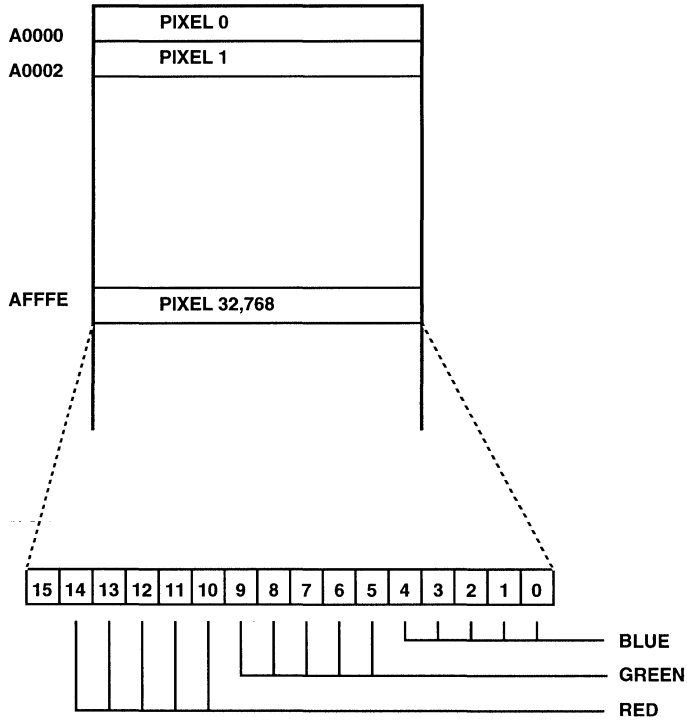

Figure D1–3. 32,768 Color (15-Bit) Packed-Pixel Mode

Figure D1–3 shows the 15-bit (32,768 colors) Direct-color, Packed-pixel mode organization. The RGB color information is stored in 5-5-5 format, and the MSB (bit 15) is ignored. Two bytes per pixel are used for storing the color information. The CPU addressing is completely sequential. The 5-5-5 format represents most-significant bits of RED, GREEN, and BLUE of the 24-bit DAC output.

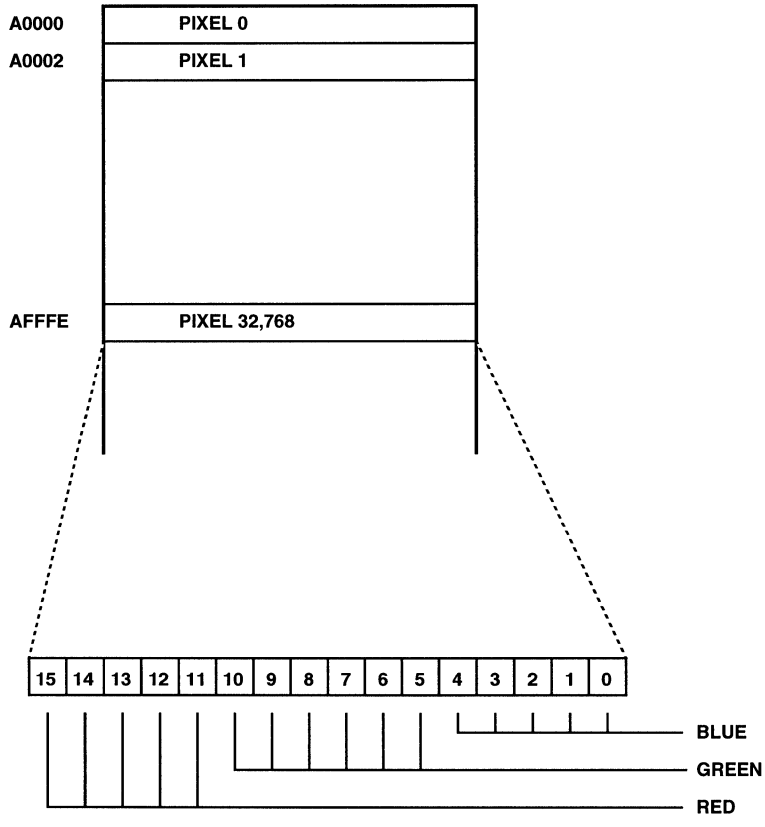

Figure D1–4. 65,536 Color (16-Bit) Packed-Pixel Mode

Figure D1–4 shows the 16-bit (65,536 colors) Direct-color, Packed-pixel mode organization. The RGB color information is stored in a 5-6-5 format comprising 5-bits of RED, 6-bits of GREEN, and 5-bits of BLUE. The color information (per pixel) is read from display memory, and used by the internal palette DAC in Direct-color mode to display 65,536 colors simultaneously.

6. MIXED 32,768 COLORS (RGB 5-5-5) and 256-COLOR (8-BITS/ PIXEL) PACKED-PIXEL MODES

The CL-GD542X VGA controllers palette DAC supports a Mixed-color mode that is capable of combining RGB 5-5-5 format and packed 8-bit per pixel format. The CL-GD542X internal palette DAC is set to mixed mode format by programming the Hidden DAC register 3C6h. In mixed mode operation, Pixel Data bit 15 is used to choose between palette operation and RGB 5-5-5 color. This allows 5-5-5 data to overlay 256-color images on a pixel-by-pixel basis. If bit 15, the most-significant bit (MSB) of the 16-bit pixel data is a '0', then bits 14:0 are treated as 5-5-5 RGB data. If the most-significant bit (MSB) is set to a '1' then bits 7:0 choose a palette entry in the palette DAC LUT and bits 14:8 are ignored.

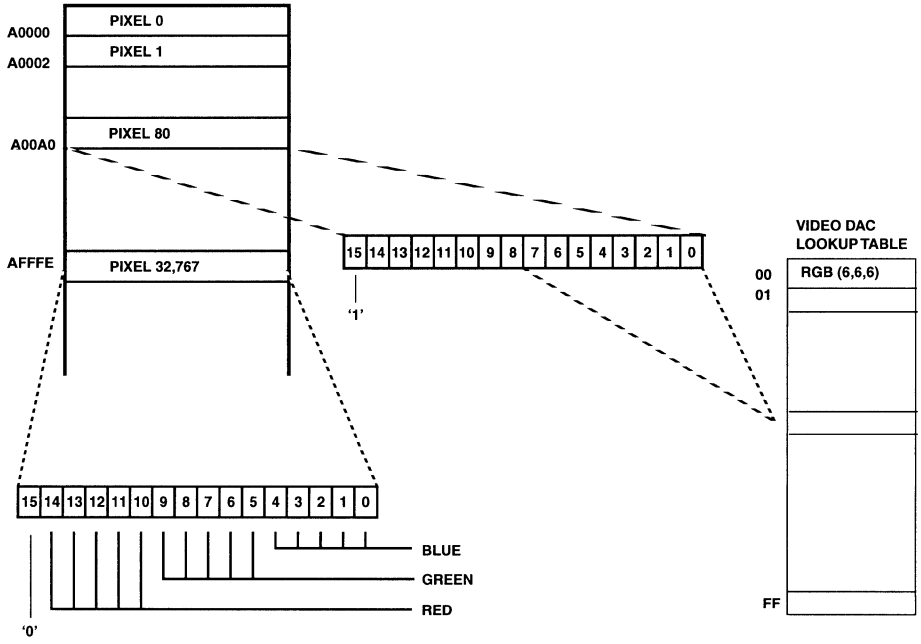

Figure D1–5. Mixed-32,768-Color (15-Bit) Packed-Pixel Data Format

Figure D1–5 shows the Mixed-color, RGB 5-5-5 packed-pixel data format. Two bytes per pixel are used for storing the color information. The MSB (bit 15) of pixel data is '0', so bits 14-0 are treated as RGB 5-5-5 format. If the MSB (bit 15) is a '1' then bits 7-0 are used as index to lookup color information from the palette DAC LUT. The CPU addressing is completely sequential.

7. TRUE COLOR 24-BIT (16.8 MILLION COLORS), PACKED-PIXEL MODES

The CL-GD542X VGA controller supports a True Color mode that is capable of displaying 16-million colors simultaneously at screen resolutions of up to 640 x 480. The CL-GD542X uses its internal palette DAC to support this TARGA-compatible mode, where 24 bits per pixel of color information is used to display 16-million colors. The VGA-standard palette DAC LUT is limited to 256 addresses. This scheme bypasses the LUT, and passes 24 bits of RGB (RED, GREEN, and BLUE) color information directly to the DAC to generate the high-range of colors. The CL-GD542X True Color mode offers professional-quality color images to be displayed on standard VGA analog monitors for desktop and multimedia applications.

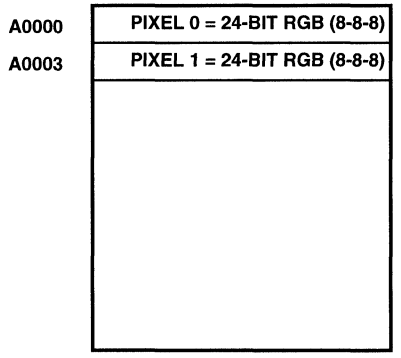

Figure D1–6. 24-bit True Color Packed-Pixel Mode

Figure D1–6 shows how True Color 24-bits per pixel (RGB 8-8-8) video mode data bytes are stored in terms of physical plane organization. The memory controller makes this organization completely transparent, hence to the CPU the byte addressing is sequential. For example, at Segment A000, Pixel 0 RGB color information is stored in three sequential bytes: Blue color information resides at offset 0, Green color information resides at offset 1, and Red color information resides at offset 2. Pixel 1 RGB information is at offset 3. To address display memory beyond 64K segment boundary, the CL-GD542X supports a display memory paging scheme that allows up to 1 Mbyte of display memory to be paged into the CPU address range.

8. EXTENDED VIDEO MEMORY ADDRESSING TECHNIQUES

The CL-GD542X is capable of addressing up to 1 Mbyte of display memory. In the DOS environment, there is 128K bytes of memory space at A0000 - BFFFF reserved for display memory. If the VGA has to share this memory with MDA, Hercules, or CGA, it is left with the single 64K byte segment from A0000 to AFFFF.

The CL-GD542X supports single-paging and dual-paging display memory addressing schemes that allow mapping of two 32K byte segments, or one 64K byte segment of display memory into CPU address space.

The CL-GD542X also supports a linear address mapping scheme that allows the display memory to be mapped to a continuous 1-Mbyte region above the standard 1-Mbyte DOS address space. This allows application programs to access the full 1 Mbyte of display memory instead of being constrained to a 64K bytes window. To take advantage of this linear-addressing feature, drivers need to be written to ensure compatibility with the operating systems.

8.1 Single-Page Addressing

The single-page addressing scheme allows a 64K byte segment of display memory to be mapped to the A0000 - AFFFF of CPU address range. The segment of display memory that is mapped into the CPU address range is selected by programming the Extension register GR9: Offset register 0 (I/O Port Address 3CF, Index = 0 x 09).

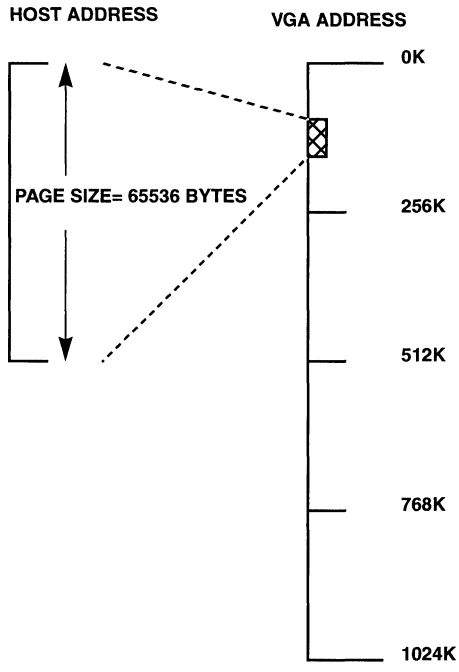

Figure D1–7. Single-Page Mapping Scheme

8.2 Dual-Page Addressing

The dual-page addressing scheme allows two segments of display memory to be mapped into the CPU address range. The two segments are mapped into address range A0000 - A7FFF and A8000 - AFFFF. The two segments of display memory mapped into the CPU address range is determined by the Offset Register 0 and Offset Register 1. The dual-page address mapping is used for read-modify-write operation on large blocks of data. The two separate display memory segments can be accessed by the CPU for read and write operations. This allows block transfer of data via repeat move string DMA instructions.

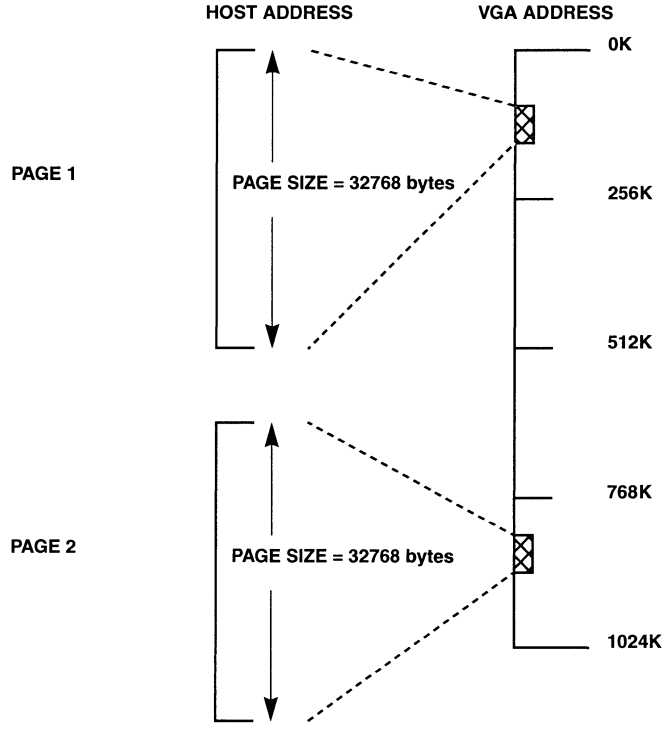

Figure D1–8. Dual-Page Mapping Scheme

The start address of a page is determined by the 8-bit value programmed in the corresponding Offset register.

For 1-Mbyte VGA mapping, the 8-bit Offset register value is added to the 16 bits of CPU address, to generate the 20-bit Display Memory Address.

For a page size of 64K bytes, Figure D1–9 shows the Offset register and the CPU Address bits that are added to generate the Display Memory Address. Note that the corresponding four bits that are overlapping allow the Start Page Address to begin at any 4K boundary of display memory.

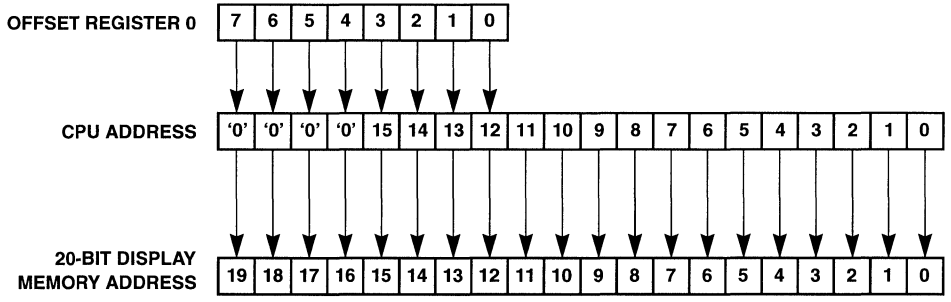

Figure D1–9. 64K Page Mode Remapping Adder Alignment for 1-Mbyte Memory

For 2-Mbytes VGA mapping, the 8-bit Offset register value is added to the bits of CPU address, to generate the 21-bit Display Memory Address.

For a page size of 64K bytes, Figure D1–10 shows the Offset register and the CPU Address bits that are added to generate the 2-Mbyte Display Memory Address. Note that the corresponding two bits that are overlapping allow the Start Page Address to begin at any 16K boundary of display memory.

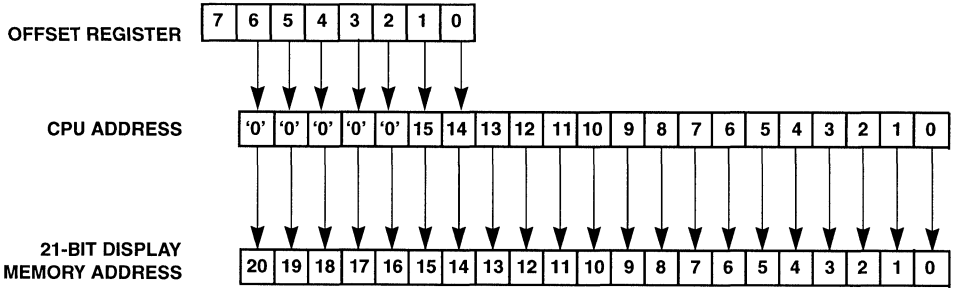

Figure D1–10. 64K Page Mode Remapping Adder Alignment for 2-Mbyte Memory (CL-GD5426/'28 Only)

For Dual-Page Mapping, the start address of pages can be at any 4K boundary of display memory. The two pages that are mapped into CPU address range can be any two separate or overlapping segments of display memory.

For a page size of 32K bytes, Figure D1–11 shows how the Base Address Remapping and CPU Address bits are added to find the resulting Display Memory Address. Note that the CPU Address bit 15 is used to select whether Offset Register 0 or Offset Register 1 will be used to calculate resulting value of Display Memory Address.

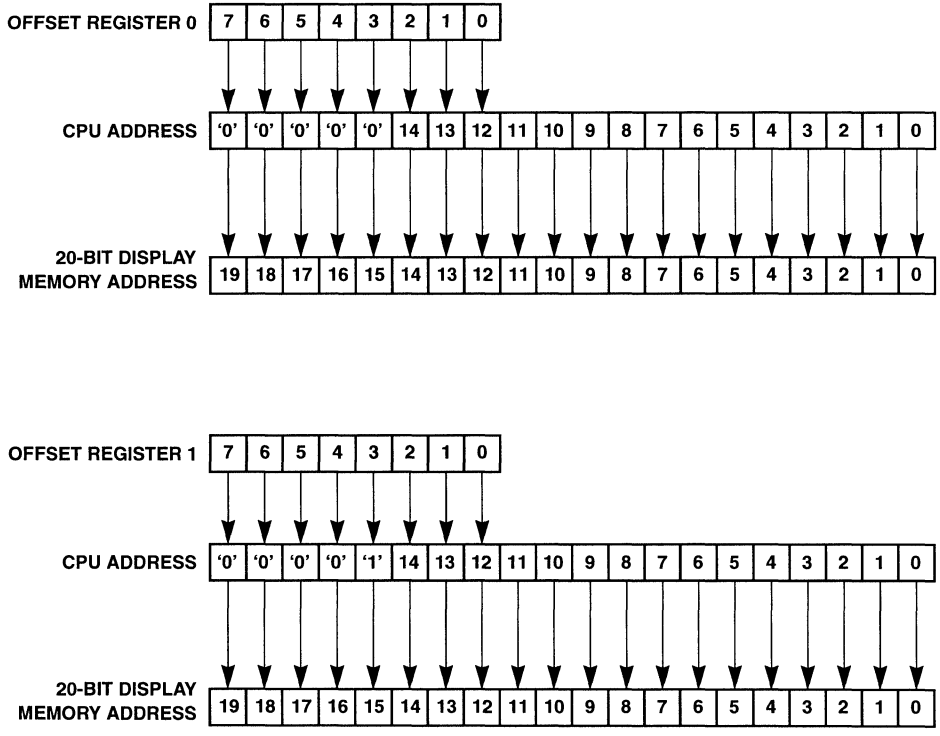

Figure D1–11. 32K Page Mode Remapping Adder Alignment For 1-Mbyte Display Memory

Note that in Figure D1-11, bit 15 of the CPU address selects whether Offset 0 or Offset 1 will be used for the Display Memory Addressing.

The following table lists the CL-GD542X Extension registers that control the CPU Base Address and display memory mapping functions:

Table D1–4. CL-GD542X Extension Registers

Function	Register Name	Port	Index	Bit	Value
Single-Page	GRB: Graphics Controller Mode Extensions	3CF	0B	0	0
Dual-Page	GRB: Graphics Controller Mode Extensions	3CF	0B	0	1
Offset register granularity 4K or16K	GRB: Graphics Controller Mode Extensions	3CF	0B	5	0 or 1
Linear Addressing	SR7: Graphics Controller Mode Extensions	3C4	07	7:4	15..0
Offset Register 0	GR9: Offset register 0	3CF	09	7:0	255..0
Offset Register 1	GRA: Offset register 1	3CF	0A	7:0	255..0

Figure D1–12 and D1–13 below show the Extension registers that control the Extended Memory-mapping functions. The following figures show the register bits as listed in the Table D1–2 above.

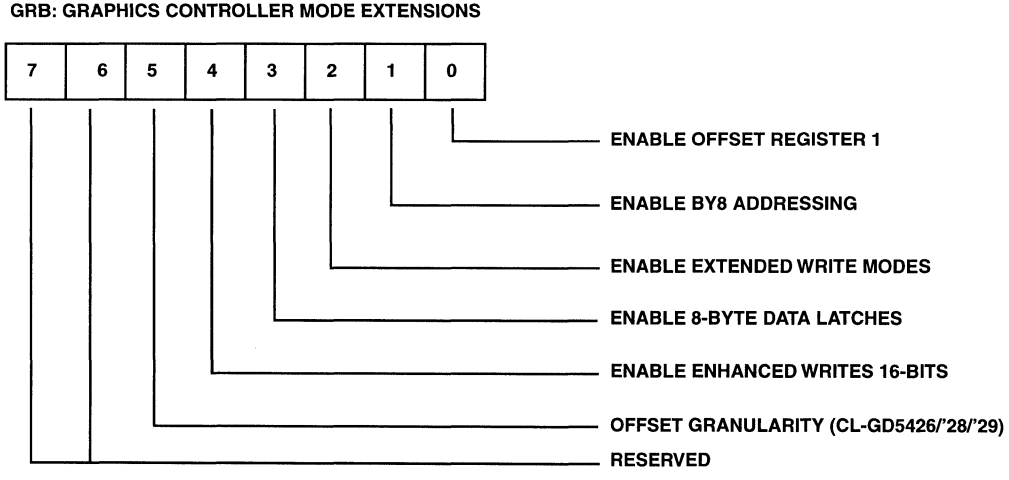

Figure D1–12. Extension Register GRB

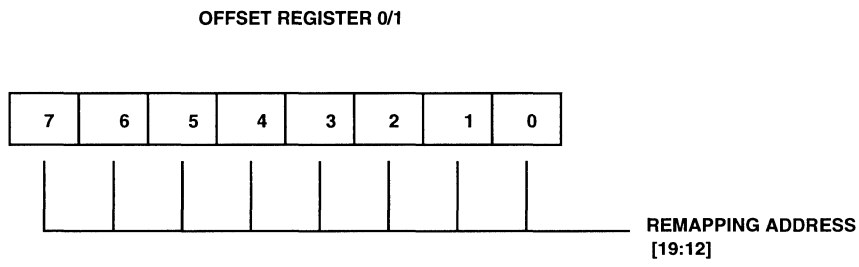

Figure D1–13. Extension Register GR9/GRA

9. VGA PROGRAMMING EXAMPLES

This section provides the software programming examples with source code listing and discussion on the following topics:

- Identifying CL-GD542X VGA Controllers
- Setting up CL-GD542X Extended Video modes via INT 10h Function Call
- Enabling/disabling Extension register Access
- Selecting Single-Page Mapping
- Selecting Dual-Page Mapping
- Loading Single-Page Bank with a new start address
- Loading Dual-Page Banks with new start addresses

9.1 Identifying the CL-GD542X VGA Controllers

The CL-GD542X VGA Controllers can be identified by calling the Extended VGA BIOS inquiry function via INT 10H. If a VGA BIOS is not available, then a controller can by identified by programming the Unlock All Extension register (SR6) and reading the Chip ID register (CR27). The following code show the steps to enable/disable CL-GD542X Extended register access:

```
Enable Extension Register Macro:
;    Function:
;    Enabling Extensions
;     Calling Protocol:
;    enable_extensions

     enable_extensions macro
     mov   dx,03c4h              ; select Extended Register SR6 i/o port
     mov   al,06h                ; Unlock All Extension register index
     mov   ah,12h                ; load with xxx1x010 to enable extension
     out   dx,ax                 ; write index and data
     endm

Disable Extension Register Macro:

     ; Function:
     ;     Disabling Extensions

     ; Calling Protocol:
     ;     disable_extensions

     disable_extensions macro
     mov   dx,03c4h              ; select Extended Register SR6 i/o port
     mov   al,06h                ; Unlock All Extension register index
     mov   ah,00h                ; load with 00 to disable extension
     out   dx,ax                 ; write index and data
     endm
```

NOTE: SR6 is not implemented on the CL-GD5429. This means that the extension registers are always enabled. The two code segments listed above have no effect on the CL-GD5429.

9.2 Determining if VGA Controller is a CL-GD542X

The CL-GD542X Chip ID register (CR 27) is used to identify the CL-GD542X family of controllers. The following sample code shows how to program the Extension registers to read the Chip ID and determine the chip type:

```
;Function: Identify Cirrus Logic CL-GD542X VGA controller
;Input Parameters:;none
;Output Parameters:
;     AL =00    ID FAILED
;     AL =11    CL-GD5402
```



```
;       AL =12    CL-GD5420
;       AL =13    CL-GD5422
;       AL =14    CL-GD5424
;       AL =15    CL-GD5426
;       AL =16    CL-GD5420r1
;       AL =17    CL-GD5402r1
;       AL =18    CL-GD5428
        AL =19    CL-GD5429
; Calling Protocol:
; VGAchip = Id_GD542x()*/

_Id_GD542x proc far
        mov     dx,3c4h     ; load Unlock All Extensions I/O port
        mov     al,06       ; load SR6 register index
        out     dx,al       ; write index and data register
        inc     dx          ;
        in      al,dx       ; read data register
        mov     ah,00h      ;
        cmp     al,12h      ; check SR6 read back value
        jne     chk29       ; see if this is a 5429 (no SR6)
        mov     dx,3d4h     ; load chip Id CR27 I/O port return
        mov     al,27h      ; select CR27 index
        out     dx,al       ;
        inc     dx          ;
        in      al,dx       ; read chip id
        mov     ah,11h      ;
        cmp     al,89h      ; check for CL-GD5402
        jb      exit        ;
        mov     ah,17h      ; check for CL-GD5402r1
        je      exit        ;
        mov     ah,12h
        cmp     al,8ah      ; check for CL-GD5420
        je      exit        ;
        mov     ah,16h
        cmp     al,8bh      ; check for CL-GD5420r1
        je      exit
        shr     al,1
        shr     al,1
        mov     ah,13h      ;
        cmp     al,23h      ; check if GD5422
        je      exit        ;
        mov     ah,14h      ;
        cmp     al,25h      ; check if GD5424
        je      exit        ;
        mov     ah,15h      ;
        cmp     al,24h      ; check if GD5426
        je      exit        ;
        mov     ah,16h      ;
        cmp     al,26h      ; check if GD5428
        je      exit        ;
        mov     ah,16h      ;
        cmp     al,26h      ; check if GD5428
        je      exit        ;
```

```
      mov     ah,00h      ; failed id
exit: mov     al,ah       ; return in AL the chip id value
      xor     ah,ah       ; zero AH
      ret
chk29:mov     dx,3d4h     ;we will read out
      mov     al,27h      ;the chip ID register
      out     dx,al       ;point to chip ID register
      inc     dl          ;data register
      in      al,dx       ;read chip ID
      shr     al,1        ;shift to discard
      shr     al,1        ; revision level bits
      mov     ah,18h      ;in case it is
      cmp     al,27h      ;CL-GD5429 ID
      je      exit        ;yes it was
      xor     ah,ah       ;no it wasn't
      jmp     exit
_Id_GD542x endp
```

9.3 Initializing CL-GD542X Super VGA Mode Via INT 10h Call

The following listing is used to initialize the desired video mode by calling the Cirrus Logic VGA BIOS Set Mode Function:

```
;Set Video Mode
;set up Extended Video mode supported by CL-GD542X VGA BIOS
;
;Calling Protocol
; al = desired CL-GD542X video mode number
;Return
; al = current video mode
;
Set_Video_Mode proc near
      mov ah,0 ; VGA BIOS setmode function 0
      int 10H  ; call VGA BIOS interrupt 10 Hex, al= mode number
      mov ah,0Fh; VGA BIOS get current video mode number
      int 10h  ;
      ret      ; return current video mode number in al
Set_Video_Mode endp
```


9.4 Programming Single-Page Mapping

The following listing shows the Extension registers that need to be programmed to set up CL-GD542X Single-Page Mapping:

```
; Single Page Mapping
; Setup Single-Page Mapping

; Calling Protocol
;     Set_Single_Page

Set_Single_Page proc near
;setup CPU Base Address Control Register for single page, 64k page size
      mov      dx,03ceh     ; select GRB extension register i/o port
      mov      al,0bh       ; select GRB register index
      out      dx,al        ; write index register
      inc      dx           ; inc dx to read data port
      in       al,dx        ; read data
      and      al,0feh      ; apply mask to set GRB[0] = 0
      out      dx,al        ; write i/o port with new data
      ret
Set_Single_Pageendp
```

9.5 Programming Dual-Page Mapping

The following listing shows the Extension registers that need to be programmed to set up CL-GD542X Dual-Page Mapping:

```
; Dual Page Mapping
;     Setup Dual-Page Mapping
;
; Calling Protocol
;     Set_Dual_Page

Set_Dual_Page proc far

; setup Graphics Controller Mode Extensions Register for dual page size
      mov      dx,03ceh     ; select extension register i/o port
      mov      al,0bh       ; select CPU Base Address Register index
      out      dx,al        ; write index register
      inc      dx           ; inc dx to read data port
      in       al,dx        ; read data
      or       al,01h       ; data = enable 32k pagesize, dual page
      out      dx,al        ; write i/o port with new data
      ret
Set_Dual_Page  endp
```

9.6 Programming the Address Remapping Registers

The CPU Base Address Mapping registers represent the eight most-significant bits of the 1 Mbyte address range that can be mapped into the limited CPU address range of A0000 - BFFFF. If the page size is selected to be 64K bytes, then the display memory is mapped into CPU address range A0000 - AFFFF. The 64K byte segment that is remapped into CPU address range can start at any 4K address boundary of display memory. This means that with 1 Mbyte of display memory, the Remapping registers can select any one of the possible 256 start address locations.

The following examples shows how to select the desired page for Single-Page Mapping with 64K page size, and Dual-Page Mapping with 32K page size.

9.7 Programming Single-Page Remapping with a 64K Segment Address

The following listing shows how the Extension Offset Register 0 needs to be programmed to map a desired page (64K bytes) of display memory into CPU address at Segment A000.

```
;Function:
;Load the Single Page Offset Register 0 with the new start address
;of a 64K byte segment
; Input:
; bl = 0..255
; page number for start address of desired 64k byte segment
;
; Calling Protocol:
; Select_Single_Page

Select_Single_Page macro
      mov       dx,3CEh      ; load GR09 extension register i/o port
      mov       al,09h       ; load Offset Register 0 index
      mov       ah,bl        ; get page number
      out       dx,ax        ; program selected page
Select_Single_Page endm
```

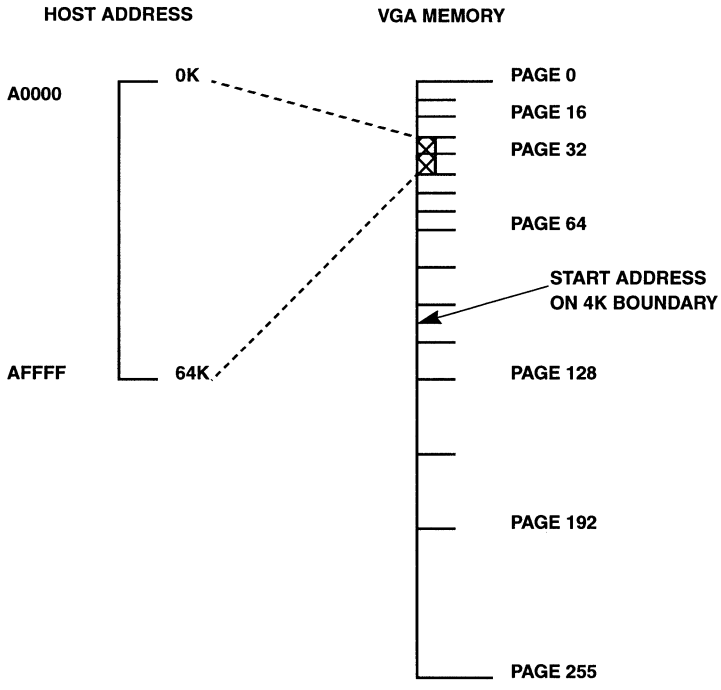

Figure D1–14. Single 64K Byte Page Mapping Scheme

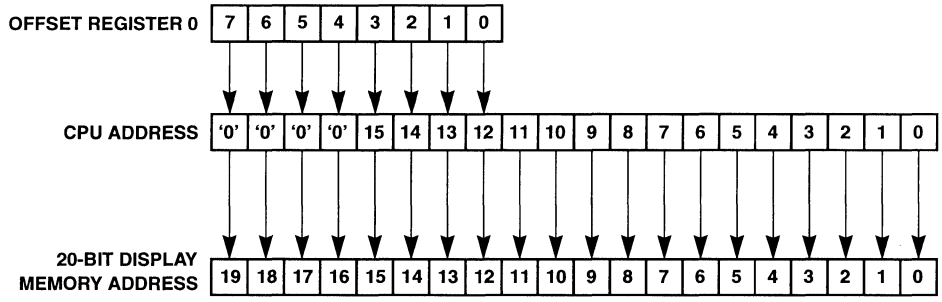

Figure D1–15. 64K Page Mode Remapping Adder Alignment For 1-Mbyte Display Memory

Figure D1–14 shows how the eight bits of the Offset register 0, is added with 20 bits of CPU address to generate a 20-bit Display Memory Address.

9.8 Programming Dual-Page Remapping Address with a 32K Segment Bank Address

The following listing shows the Extension registers that need to be programmed to set up Dual-Page Remapping Address with a 32K Segment Bank Address:

```
;Function:
;Load the Dual Page Remapping Registers with the new star address
;at 32K byte segments

; Input:
;bl = 0..255 page number for segment mapped to A0000 - A7FFF
;bh = 0..255 page number for segment mapped to A8000 - AFFFF

; Calling Protocol:
;Select_Dual_Pages

Select_Dual_Pages macro
mov   dx,3CEh  ; load extension register i/o port
mov   al,09h   ; load CPU Base Addr. Mapping Register A index
mov   ah,bl    ; get page number for A0000-A7FFF mapping
out   dx,ax    ; program selected page
mov   al,0ah   ; load CPU Base Addr. Mapping Register A index
mov   ah,bh    ; get page number for A8000-AFFFF mapping
out   dx,ax    ; program selected page
Select_Dual_Pages endm
```


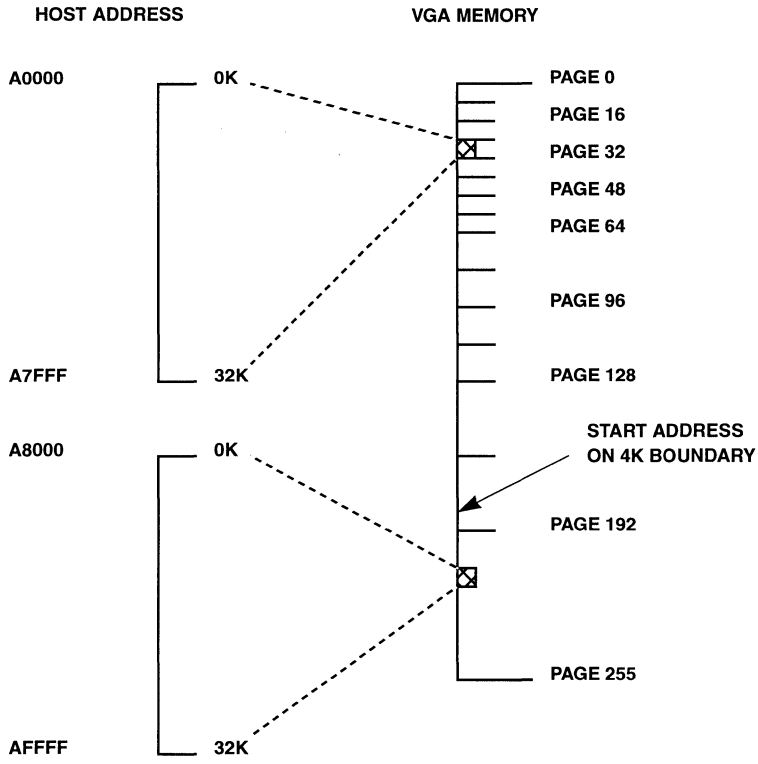

Figure D1–16. Dual-Page (32K Byte) Mapping Scheme

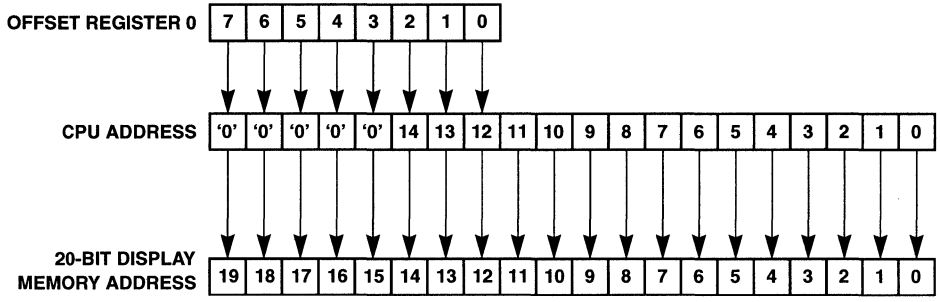

Figure D1–17. 32K Page Mode Remapping Adder Alignment For 1-Mbyte Display Memory

Figure D1-17 shows how the eight bits of the Offset register 0 or Offset register 1 (based on CPU address bit 15) is used along with 16-bit CPU address to generate a 20-bit Display Memory Address.

Appendix D2

Linear Addressing
Application Note

LINEAR ADDRESSING

1. INTRODUCTION

The CL-GD542X family of VGA controllers can be configured to access display memory in a linear or a segmented fashion. The Linear Addressing mode forces all display memory to be continuous.

In extended DOS or OS/2 applications, it is possible to place the VGA memory into high memory where there is space to place one (or two) Mbytes of display memory into a contiguous address space. This allows the application programs to ignore the Offset register programming.

2. LINEAR ADDRESS ADVANTAGES

The Linear Addressing of display memory offers two advantages. Firstly, it ensures faster programs; secondly, it ensures contiguous high-speed operation from a hardware perspective.

The software advantage requires an extended operating system and access to the memory through the 80286, 80386, or 80486 processors. The 32-bit instructions can be used to access the 1 Mbyte memory without Segment registers.

The hardware advantage is primarily aimed at video frame grabbers/overlay devices where the hardware has a continuous stream of data coming in to the True Color VGA controller display memory.

3. LINEAR ADDRESS MAPPING

The Extended Sequencer Modes register SR7 bits 7:4 determine the 1-Mbyte system memory segment of the 16-Mbyte address space that can be selected for CL-GD542X display memory mapping.

If these bits are all zeroes, then the CL-GD542X is configured as a standard VGA mapped to the 64K segments of 0A000h and/or 0B000h as selected by the VGA Register bits GR6[3:2].

If these bits are non-zeroes, then the CL-GD542X is set for linear addressing in the 1 Mbyte of system address selected. With the linear address selected, the standard VGA address GR6[3:2] and 3C2[5] have no effect on video memory mapping.

With 1 Mbyte of display memory installed and extended 256-color Chain-4 addressing selected, the 1 Mbyte of linear system address will have a one-to-one mapping to display memory addressing.

If the CL-GD542X is set for unchained, BY8 or BY16 addressing, each bit plane will be seen as a 256K linear map that is duplicated four times in the selected 1 Mbyte of system address space.

If less than 1 Mbyte of display memory is installed, the CL-GD542X will still respond to the entire 1 Mbyte of system address space, but display memory 'Address Wrapping' will occur.

4. SUMMARY

The CL-GD542X Linear Addressing option allows applications running under extended operating systems to take advantage of the linear display memory access and offer faster performance.

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Appendix D3

Hardware Cursor
Application Note

HARDWARE CURSOR

1. INTRODUCTION

The CL-GD542X family of VGA controllers is capable of supporting a 32 x 32 or 64 x 64 Hardware Cursor (mouse pointer) in 16-color planar, 256-color, and 32K and 64K Packed-pixel Graphics Modes.

The Hardware Cursor replaces the software mouse pointer commonly used by GUI (Graphics User Interface) applications. The Hardware Cursor eliminates the need for application software to save and restore the screen data as the mouse cursor position changes.

The application software needs to initialize the Hardware Cursor once, and from that point only needs to update the cursor (x, y) position to move the cursor on the screen. The Hardware Cursor offers a smooth-moving mouse pointer with improved performance as compared to a software cursor.

Multiple Hardware Cursor patterns can be loaded into the upper display memory area, allowing application programs to select one of the patterns as the active-cursor pattern.

2. HARDWARE CURSOR OPERATION

The Hardware Cursor is a pixel array of two planes: Cursor Plane 0 and Cursor Plane 1. Table D3–1 shows how the corresponding bits of the two planes determine the displayed state of each cursor pixel.

Table D3–1. Hardware Cursor Planes

Cursor Plane 0	Cursor Plane 1	Hardware Cursor Pixel Display State
0	0	Transparent
0	1	Inverted VGA Display Data
1	0	Cursor Color 0
1	1	Cursor Color 1

The Cursor Color 0 and 1 is supplied by the internal palette DAC two extra LUT (lookup table) locations at Index 00h and 0Fh. This allows for Hardware Cursor colors to be independent of the palette DAC Table Index 00h through FFh.

The CL-GD542X Extension SR12: Graphics Cursor Attributes register can be programmed to:

- Select the cursor size
- Enable access to the palette DAC cursor colors
- Enable/disable the cursor

The Hardware Cursor data is located in the upper 16K of display memory (or upper 4K of each logical memory plane). Based on the cursor size selected, 32 x 32 or 64 x 64, the number of cursor patterns that can be loaded in display memory at one time is either 64 or 16. The Graphics Cursor Pattern Address Offset register allows the application to select one of the cursor patterns loaded in display memory to be selected as the active-graphics cursor.

The Hardware Cursor position is controlled by programming the Graphics Cursor X position and Graphics Cursor Y position. The 11-bit Cursor X location and Cursor Y location values are programmed by initiating a 16-bit I/O write, where bits 7:5 of the Index register are the least-significant bits of the 11-bit value.

The following table shows the CL-GD542X Extension register bits for programming the Hardware Cursor:

Table D3–2. CL-GD542X Extension Register Bits

Function Description	Extension Register	I/O Port Address	Register Bits	Value
Graphics Cursor Enable	SR12	3C5h	0	1
Access Graphics palette DAC colors	SR12	3C5h	1	1
32 x 32 Graphics Cursor size	SR12	3C5h	2	0
64 x 64 Graphics Cursor size	SR12	3C5h	2	1
Graphics Cursor Pattern Offset	SR13	3C5h	5:0	63..0
Graphics Cursor X position	SR10, 30, 50, 70, 90, B0, D0, F0	3C4h/3C5h	7:5/7:0	2047..0
Graphics Cursor Y position	SR11, 31, 51, 71, 91, B1, D1, F1	3C4h/3C5h	7:5/7:0	2047..0

3. 32 x 32 HARDWARE CURSOR

For a 32 x 32 cursor size, each cursor pattern requires 256 bytes (128 bytes per plane x 2 cursor planes). This allows for 64-cursor patterns to be loaded into Hardware Cursor data area at the top of display memory. The active-graphics-cursor pattern is selected by programming the Graphics Cursor Pattern Address register (SR12) bits 5:0.

The Hardware Cursor pattern data from Cursor Plane 0 and Cursor Plane 1 is loaded into display memory in the following order. The 256 bytes are stored across the four logical Display Memory Planes — 64 bytes per plane. The first 32 bytes of each memory plane are from Cursor Plane 0 and last 32 bytes are from Cursor Plane 1.

4. 64 x 64 HARDWARE CURSOR

The 64 x 64 cursor size is only available with 32-bit-wide display memory.

For a 64 x 64 cursor size, each cursor pattern requires 1024 bytes (512 bytes per plane x 2 cursor planes). This allows for 16-cursor patterns to be loaded into Hardware Cursor data area at the top of display memory. The active-graphics-cursor pattern is selected by programming the Graphics Cursor Pattern Address register (SR12) bits 5:2.

The 64 x 64 Hardware Cursor pattern data from Cursor Plane 0 and Cursor Plane 1 is loaded into display memory one cursor scanline at a time; 8 bytes written across the four logical display planes (2 bytes per plane). One cursor scanline is loaded from Cursor Plane 0 followed by one cursor scanline from Cursor Plane 1. This is done until all 64 scanlines from the Cursor Plane 0 and Cursor Plane 1 are loaded into display memory.

5. SUMMARY

The CL-GD542X programmable 32 x 32 or 64 x 64 size Hardware Cursor eliminates the application program's overhead of maintaining a software mouse pointer. The Hardware Cursor offers a smooth and fast-moving mouse pointer interface.

Appendix D4

Interlaced Mode
Application Note

INTERLACED MODE

1. INTRODUCTION

In the CL-GD542X family of VGA controllers, the CRT registers can be programmed to operate Text or Graphics Video modes on interlaced or non-interlaced monitors.

The following sections describe the Interlaced mode display operation as well as Interlaced modes supported by CL-GD542X VGA controllers.

2. INTERLACED MODE DISPLAY OPERATION

Video displays are either interlaced or non-interlaced. In an interlaced display, alternate scanlines are updated every frame, and in a non-interlaced display, every scanline is updated every frame.

Interlaced mode is used when the VGA controller or monitor hardware cannot keep up with the data required by the video system. The greater the resolution of the video system, the faster the hardware must be to keep pace with the data rates.

The interlaced hardware needs to only be half as fast as the non-interlaced hardware. The disadvantage of the interlaced display is that the eye can begin to detect the alternating frequencies on the screen, especially when used under the fluorescent light, which operates at 60 Hz.

3. 1024 x 768 INTERLACED MODE

The standard VGA Video modes are non-interlaced modes. However, Super VGA modes, such as 1024 x 768 resolution, require a data clock rate of 65 MHz for non-interlaced operation. The display monitor also need to support the 65-MHz Dot Clock and support 48.3-kHz horizontal scan rate to run at 60-Hz vertical refresh rate.

The other alternative is to run the 1024 x 768 Interlaced Video mode, which requires a dot clock of 44.9 MHz and a monitor that supports 35.5-kHz horizontal scan rate.

For interlaced mode, the CL-GD542X CR Vertical Timing register values are typically programmed based on vertical resolution divided by two.

The CL-GD542X Extension register CR1A, Miscellaneous Control bit 0 is set to a '1' to select Interlaced mode operation. Also CR19, Interlace End bits [7:0] need to be programmed to center the scanlines in the odd field half way between scanlines in the even field.

Appendix D5

132-Column Text Mode
Application Note

132-COLUMN TEXT MODE

1. INTRODUCTION

The CL-GD542X family of controllers is capable of supporting 132-column Alphanumeric Text modes. The CL-GD542X VGA BIOS supports the extended 132-column Text modes listed in Table D5–1.

Table D5–1. CL-GD542X Extended 132-Column Text Modes

Mode Number	Resolution	Colors	Timing Options
14h (XGA)	132 x 25 Text	16 colors	70 Hz
53h	132 x 60 Text	16 colors	60 Hz
54h	132 x 43 Text	16 colors	70 Hz

The CL-GD542X VGA BIOS supports all standard interrupt 10h function calls to support 132-column text mode operation. As in standard VGA 80-column text modes, the application program can call the VGA BIOS 'Set Mode' function call to initialize the 132-column mode. From this point the application program can either call the VGA BIOS to manipulate text or write character/attribute data directly to display memory.

The following section describes the CL-GD542X extended 132-column Text mode operation.

2. 132-COLUMN TEXT MODE OPERATION

The CL-GD542X has hardware enhancements to support the extended 132-column-wide text modes. The 132-column Extended Video Mode is selected by setting CR1B, Miscellaneous Control register bit 6. The following is a description of the steps executed by the BIOS to set 132-column mode of operation:

- The Video Dot Clock is set to 41.164 MHz to support 31.5-MHz Horizontal Sync rate.
- The Sequencer is programmed to select eight-dot character clock.
- The memory organization for character font tables is different for 132-column modes. With the 132-column Mode selected, CR1B[6] = 1. The font tables that are normally loaded in Plane 2 are automatically remapped into Plane 2 and Plane 3 of the physical DRAM pages. The CL-GD542X re-maps character generator dot patterns of all lower 128-character codes into Plane 2, and all the upper 128-character codes into Plane 3. One half of each 64K byte of physical plane is used, providing a total of eight Character Maps (8K byte each) to be loaded into Memory Plane 2 and 3.
- Due to the Plane 2 and 3 remapping, the 132-column mode does not support displaying two different character maps on the screen at the same time. (This is normally done in standard VGA 80-column text modes by selecting Character Attribute bit 3 of the selected character).

3. 132-COLUMN CRT CONTROLLER PROGRAMMING

The following horizontal CRT Controller register values are recommended for 132-column Text modes.

Table D5–2. 132-Column Text Mode CRT Horizontal Parameters 3?4/3?5

CRT Register	CRT Register Description	Index	Value
CR0	Horizontal Total	0	9Fh
CR1	Horizontal Display Enable End	1	83h
CR2	Start Horizontal Blanking	2	84h
CR3	End Horizontal Blanking	3	82h
CR4	Start Horizontal Retrace	4	8Ah
CR5	End Horizontal Retrace	5	9Eh
CR13	Offset	13	42h

NOTE: ? = 'B' for Monochrome and 'D' for Color mode.

The above table values correspond to 132-column Text mode for 31.5-kHz horizontal scan rate using a 41.164-MHz dot clock.

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Appendix D6

Color Expansion and Extended Write Modes

COLOR EXPANSION AND EXTENDED WRITE MODES

1. INTRODUCTION

The CL-GD542X family supports color expansion for faster CPU write performance. This is implemented via two Extended Write modes and the BitBLT engine. These Extended Write modes operate on eight pixels at a time, in 8- or 16-bits-per-pixel Graphics modes with packed-pixel addressing. Extended Write modes can be used for faster text write, pattern fill, and block-move operations in Graphics modes. in addition, the BitBLT engine supports color expansion for 8- and 16-bit-per-pixel modes.

The following sections cover Extended Write modes from a programming point of view. The basic advantage of color expansion is explained and the registers involved described. Finally, the capabilities of the BitBLT engine are covered.

2. COLOR EXPANSION — HOW PERFORMANCE IS ENHANCED

In many configurations the CPU cannot send data across the host interface as quickly as it can be written into display memory. This results in a level of performance less than is possible, particularly in configurations involving a 32- or 64-bit display memory bus.

Consider an ISA bus machine with a 32-bit display memory bus using Video mode 5F (640 x 480 x 256 colors). With an MCLK of 50 MHz, the total display memory bandwidth is about 100 Mbytes/second. With a refresh rate of 72 Hz, 31.5 Mbytes/second of that bandwidth will be used to refresh the screen (neglecting retrace time), leaving nearly 70 Mbytes/second available for the CPU to update the screen. An ISA bus has a theoretical bandwidth of no more than 8-12 Mbytes/second, leaving as much as 60 Mbytes/second unused.

The standard VGA includes some write modes to help with the situation discussed above. These modes involve replicating CPU data for more than one bit plane and writing directly from the display memory interface latches. The latter allows the movement of data within the display memory without crossing the host bus.

The CL-GD542X family takes these performance-enhancing measures to their logical conclusion in the following way. It is often the case that only one or two colors need to be written into display memory at any time (consider filling the screen with a pattern or writing text with a single background and a single foreground color). If the actual foreground and background colors are stored in the chip itself, then a single bit is all that must be sent across the Host Bus for each pixel. This leverages the host-interface bandwidth by a factor of 8 or 16, making it possible to use nearly all the available display memory bandwidth. This is called *Color Expansion*, and it is implemented with Extended Write modes 4 and 5.

3. COLOR EXPANSION WITHOUT THE BITBLT ENGINE

The controls that enable the Extended Write modes are in GRB[4:1], as indicated in Figure D6-1. These bits are described in detail in Chapter 9, Extension registers. Briefly, bits 3:1

are programmed to '1's for 8-bit-per-pixel modes, and bits 4:2 are programmed to '1's for 16-bit-per-pixel modes.

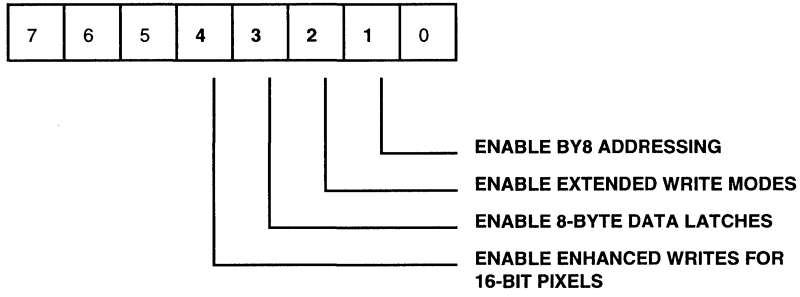

Figure D6–1. Color Expansion Controls

Enable BY8 Addressing shifts the address bits between the host and display memory three bits. This means that each **bit** within the host address space will correspond to a pixel in display memory. The pattern to be expanded is an ordered string of bits, each bit corresponding to a pixel. It can be transferred across the bus with a move string instruction and each bit will be expanded into a complete 8- or 16-bit pixel.

Enable Extended Write Modes can be considered a master enable; it must be programmed to a '1' to turn any of this procedure on.

Enable 8-byte Data Latches allows the use of eight, rather than the standard four data latches at the display memory interface.

Enable Enhanced Write for 16-bit Pixels must be programmed to a '1' to use color expansion in 16-bit-per-pixel Video modes. When this bit is programmed to a '1', each bit across the host bus still corresponds to a pixel, now a 16-bit pixel. Observe that 24-bit-per-pixel color expansion is not supported.

4. EXTENDED WRITE MODE 4

Extended Write mode 4 is enabled when the GR5[2:0] field is programmed to '100', and the Extended Write modes are enabled as described above. In Extended Write mode 4, the foreground color will be written into each pixel for which the corresponding bit on the host bus is a '1'. The foreground color will be contained in GR1 and GR11 (for 8-bit pixels GR11 is ignored).

Pixels corresponding to CPU bus bits that are a '0', will not be written in Extended Write mode 4. Extended Write mode 4 is intended for writing text into display memory for which the background is not to be modified.

5. EXTENDED WRITE MODE 5

Extended Write mode 5 is enabled when the GR5[2:0] field is programmed to '101', and the Extended Write modes are enabled as described above. In Extended Write mode 5, the foreground color will be written into each pixel for which the corresponding bit on the host bus is a '1'. The foreground color is contained in registers GR1 and GR11 (for 8-bit pixels GR11 is ignored). The background color will be written into each pixel for which the corresponding bit on the host bus is a '0'. The foreground color is contained in registers GR0 and GR10 (for 8-bit pixels GR10 is ignored).

Extended Write mode 5 will support 8- and 16-bits-per-pixel.

6. COLOR EXPANSION USING BITBLT ENGINE

This appendix reviews the information regarding Color Expansion. The data can be expanded into 8- or 16-bits-per-pixel. Refer to Appendix D8 for detailed information on the BitBLT engine.

The data to be expanded is always a single bit-per-pixel. The data can represent text or icons. In this case it would typically, but not necessarily, be transferred across the host interface. That is, Color Expansion would typically be a system-to-screen BitBLT operation.

The data could also be a pattern that is to be repeatedly expanded and written into display memory. In this case, the source data must be in display memory (pattern copies are supported only for screen-to-screen BitBLTs).

The Foreground Color registers are GR1 and GR1; Background Color registers are GR0 and GR10. Tables D6-1 and D6-2 indicate how the registers are allocated to the various colors.

Table D6–1. Background Color Registers

Format	GR0	GR10
8 bits/pixel	Single byte	Don't care
16 bits/pixel	Low byte	High byte

Table D6–2. Foreground Color Registers

Format	GR1	GR11
8 bits/pixel	Single byte	Don't care
16 bits/pixel	Low byte	High byte

Appendix D7

Reserved

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Appendix D8

BitBLT Engine

Application Note

BITBLT ENGINE

1. INTRODUCTION

Written from a software programmer's standpoint, this appendix describes the CL-GD542X BitBLT engine. The CL-GD5426, CL-GD5428, and CL-GD5429 all include a BitBLT engine. To help establish a common nomenclature, relevant terms are defined. Also included is an example of basic operation. Various methods of modifying the source data before writing it into the destination region are covered, these are: ROPs (Raster Operations), Color Expansion, and Pattern Fill. Practical considerations covered are: BLT Direction, using system memory for either the source or destination, and how to start, suspend, and resume a BLT. This document concludes with a complete summary of BLT registers, a discussion of Memory-mapped I/O, and some practical examples.

2. DEFINITIONS

This section includes a definition of terms.

Source Area: The source area of a BitBLT is the area from which the data are copied. The source area may be in display or system memory; it may be a monochrome image which will be expanded into color; it may be a single 8 pixel x 8 pixel image that will be replicated to fill a larger area. The source area is never written except in special cases where it and the destination area overlap in display memory.

Destination Area: The destination area of a BitBLT is the area into which the data are written. The destination area may be in display or system memory.

Width: The Width of a BitBLT refers to the number of bytes (not pixels) of destination that are processed before adding the Pitch values to the Address values. If the destination area is actually or potentially on the screen (that is, if it is a rasterized area that will be displayed), the Width is the number of bytes (not necessarily pixels) in each scanline. If the destination area is off-screen (or in system memory) and the source is a rasterized area (and there is no pattern copy or color expansion), the Width is the number of bytes per scanline of source. If neither the destination or source is a rasterized area, Width is simply the number of bytes that are processed before the Pitch values are added to the Address values, and has no special meaning. Width is specified in the register pair GR20/GR21. The number actually written into this register pair is one less than the actual desired width. This is an 11-bit value, allowing a maximum width of 2048 bytes.

Height: The Height of a BitBLT refers to the number of times the Pitch values are added to the Address values. If the destination area, source area, or both are actually or potentially on the screen (if either is a rasterized area that will be displayed), the Height is the number of scanlines in that area. If not, Height is simply the number of times the Pitch values are added to the Address values and has no special meaning. In this case, Width and Height are simply two numbers that are multiplied together to define the number of bytes in the destination. Height is specified in the register pair GR22/GR23. The number actually written into

the register pair is one less than the actual desired height. This is a 10-bit value, allowing a maximum height of 1024 scanlines. The contents of the registers containing the Height are not modified during the operation.

Width and Height are shown for a displayable area in Figure D8-1.

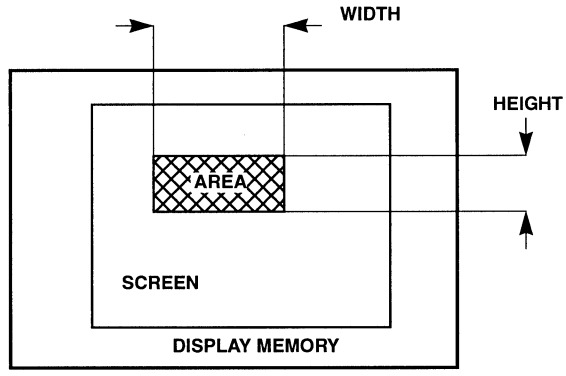

Figure D8–1. Width and Height

Pitch: The destination Pitch and source Pitch are the values that are added to the respective addresses after each *width* bytes of destination have been processed. Destination and source Pitch are specified separately. When an area is a rasterized image, the respective pitch will be the number of bytes between vertically adjacent pixels. This is the number of bytes between the (first) pixels of scanline n and scanline n+1; the number that is added to the address to get from one scanline to the next. When an area is off-screen display memory, it will often be stored so that scanlines are in contiguous locations. This minimizes fragmentation. In this case, the respective Pitch would be set equal to the Width (+1). When an area is in system memory, the respective Pitch is unused and is a 'don't care'. When executing BLTs with pattern copy or color expansion, the source area is taken to be linear and the source Pitch is a 'don't care'. The source Pitch is specified in register pair GR26/GR27. The destination Pitch is specified in register pair GR24/GR25. For the CL-GD5426/'28, these register pairs are both 12-bit values, allowing a Pitch of 4095 bytes. For the CL-GD5429, these register pairs are both 13-bit values, allowing a Pitch of 8191 bytes. Figure D8-2 shows Pitch for the case of a rasterized image.

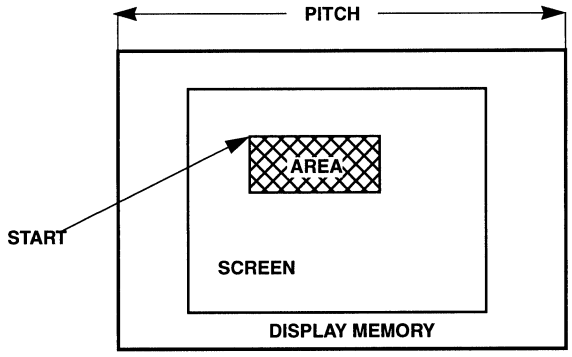

Figure D8–2. Pitch and Start

Start: Refers to the address of the first byte of a destination or source area. This is a byte offset from the beginning of display memory. The start address of the destination area is specified in register triplet GR28/GR29/GD2A. The start address of the source area is specified in register triplet GR2C/GR2D/GR2E. Each start address is a 21-bit value, allowing up to 2 Mbytes of display memory. The start address is shown in Figure D8-2.

3. AN EXAMPLE: DISPLAY MEMORY TO DISPLAY MEMORY

Table D8-1 shows how the BLT registers would have to be programmed for a very simple BLT operation. This will copy a 128-byte x 64-scanline area in display memory. The CL-GD542X is assumed to be programmed in Video Mode 65 (800 x 600, 16-bits per pixel). Therefore, each 128-byte scanline actually represents 64 pixels. The source begins at location 0, and the destination begins at location 160200 (100 scanlines from the top of the screen, 100 pixels from the left edge).

Table D8–1. Source Copy BLT

Register(s)	Contents (Decimal)	Field	How Calculated
GR0/GR10	Don't care	Background color	Only for Color Expansion
GR1/GR11	Don't care	Foreground color	Only for Color Expansion
GR20/GR21	127	Width	(64 x 2) -1
GR22/GR23	63	Height	64 - 1
GR24/GR25	1600	Destination Pitch	800 x 2
GR26/GR27	1600	Source Pitch	800 x 2

Table D8–1. Source Copy BLT *(cont.)*

Register(s)	Contents (Decimal)	Field	How Calculated
GR28/GR29/GR2A	160200	Destination Start	(100 x 1600) + (100 x 2)
GR2C/GR2D/GR2E	0	Source Start	Beginning of display memory
GR2F	don't care	Write Mask	Only for Color Expansion
GR30	0	Mode	Vanilla BLT
GR32	0Dh	Raster Op	SRC COPY
GR33	0	Mode Extension	Unused
GR31	2	Start	Set bit 1

This BLT will be executed as indicated in the following fragment of pseudo-code:

```
sourceAdrs = sourceStartAdrs;
destAdrs = destStartAdrs;
for (i = 0; i < Height; i++)              /*for each scan line*/
    {
    workingSourceAdrs = sourceAdrs
    workingDestAdrs = destAdrs
    for (j =0; j < Width; j++)            /*for each byte*/
         {
         Process one byte of Destination;
         workingDestAdrs++;               /*to next byte*/
         workingSourceAdrs++;
         }
    sourceAdrs = sourceAdrs + sourcePitch; /*next scan line*/
    destAdrs = destAdrs + destPitch;
    }
```

The BLT engine processes *width* bytes of destination, incrementing temporary source and destination addresses after each byte (actually, multiple bytes are processed in parallel). At the end of each *width* bytes, the respective pitch values are added to the addresses as they were at the beginning of the scanline, moving on to the next scanline. This continues for *height* iterations.

All BLTs are processed in this general manner. There are some variations. For color expansion, the SourceAdrs will be incremented as a bit address rather than a byte address. For pattern copies, the SourceAdrs is incremented modulo some number so that it is used over and over. If the decrement bit is set, the addresses will be decremented rather incremented.

4. ROPS (RASTER OPERATIONS)

In addition to merely moving bytes from the source area to the destination area, the CL-GD542X BitBLT engine can combine the source or pattern bytes with the destination bytes using various logical operations. Further, the source or destination or both can be ignored.

There are exactly 16 ways in which two bits can be logically combined; these are enumerated in Table D8-2. The same value for GR32 is used regardless of whether the operation uses Source or Pattern. The same information is given in non-reverse notion in the description of register GR32 in Chapter 9.

The CL-GD542X BitBLT engine directly implements all 16 ways of logically combining two operands. Combinations of three operands can be synthesized from these in the unusual cases where this is necessary.

Table D8–2. Raster Operations

Source Operation	Microsoft® Name/ Raster Operation	Pattern Operation	Microsoft® Name/ Raster Operation	GR32 (Hex)
0	BLACKNESS 00000042	0	BLACKNESS 00000042	00
DSon	NOTSRCERASE 001100A6	DPon	– 000500A9	90
DSna	– 00220326	DPna	– 000A0329	50
Sn	NOTSRCCOPY 00330008	Pn	– 000F0001	D0
SDna	SRCERASE 00440328	PDna	– 00500325	09
Dn	DSTINVERT 00550009	Dn	DSTINVERT 00550009	0B
DSx	SRCINVERT 00660046	DPx	PATINVERT 005A0049	59
DSan	– 007700E6	DPan	– 005F00E9	DA
DSa	SRCAND 008800C6	DPa	– 00A000C9	05
DSxn	– 00990066	PDxn	– 00A50065	95
D	– 00AA0029	D	– 00AA0029	06
DSno	MERGEPAINT 00BB0226	DPno	– 00AF0229	D6

Table D8–2. Raster Operations *(cont.)*

Source Operation	Microsoft® Name/ Raster Operation	Pattern Operation	Microsoft® Name/ Raster Operation	GR32 (Hex)
S	SRCCOPY 00CC0020	P	PATCOPY 00F00021	0D
SDno	– 00DD0228	PDno	– 00F50225	AD
DSo	SRCPAINT 00EE0086	DPo	– 00FA0089	6D
1	WHITENESS 00FF0062	1	WHITENESS 00FF0062	0E

5. COLOR EXPANSION

If GR30[7] is programmed to a '1', the source input to the ROP will not be actual data from the source area, but will be *color expanded* data. The source area is a monochrome image. Since the source image is a single bit-per-pixel, substantial performance benefits can be gotten, especially if the source is being expanded to 16-bits. Color Expansion can be used anytime a single foreground color or a single foreground color and a single background color are to appear in the destination. The CL-GD542x supports color expansion for 8- and 16-bit-per-pixel modes. The source can be either an 8 x 8 pattern (display memory only) or it can be monochrome data from either display memory or system memory. When the source is in display memory, it must be on a four-byte boundary. When the source is an 8 x 8 pattern, it must be on an eight-byte boundary.

Ones in the source area will result in the foreground color being written into the corresponding byte(s) of the destination area. Zeroes in the source area will result in either the background color being written into the corresponding byte(s) of the destination area, or no alteration to the destination area (transparency). The destination must be Screen Memory and the direction must be increment. Any ROP may be used, although SRCCOPY is most common when using color expansion.

The most-significant-bit of the first source byte will be expanded into the ROP source data for the first pixel of the destination. Depending on the contents of GR30[4], it will be expanded to 1 or 2 bytes. The following tables indicate the registers that contain the expansion colors.

Table D8–3. Color Expansion ('1' in source)

GR30[4]	Width	GR1	GR11
0	8-bit	Color	Don't care
1	16-bit	Low byte	High byte

Table D8–4. Color Expansion ('0' in source)

GR30[4]	Width	GR0	GR10
0	8-bit	Color	Don't care
1	16-bit	Low byte	High byte

The next bit of source data is processed for the next 1or 2 bytes of destination, and so on, until *width* bytes of destination have been processed. Unused source bits will be discarded to the end of the current byte. The destination address is modified by the destination pitch. The source pitch is ignored since the source is taken to be a linear string of bytes. The next byte of source will be the first eight pixels for the next scanline.

6. COLOR EXPANSION WITH TRANSPARENCY (CL-GD5426/'28)

For the CL-GD5426/'28, if GR30[3] is programmed to a '1', Transparency Compare is enabled. The results of the ROP will be compared to the contents of the Transparent Color register (GR34/35) for each pixel. If they compare in all bit positions for which the Transparent Compare Mask register (GR38/39) are '0', the results will *not* be written to display memory. In 8-bit pixel modes (GR30[4] = '0'), registers GR34 and GR35 *must* be programmed identically, as must GR38 and GR39.

The transparency feature must be used, and the transparent color set to the background color if color expansion is to be used with an opaque foreground and a transparent background (analog of Extended Write mode 4). The Foreground Color registers are used as indicated in Table D8–5.

Table D8–5. Color Expansion with Transparency ('1' in Source)

GR30[4]	Width	GR1	GR11
0	8-bit	Color	Don't care
1	16-bit	Low byte	High byte

7. COLOR EXPANSION WITH TRANSPARENCY (CL-GD5429)

For the CL-GD5429, if GR30[3] is programmed to a '1', the pixels corresponding to '0's in the source area are not written. This is the analog of Extended Write mode 4. This is used for a Transparent Write. If GR30[2] is programmed to a '0', the pixels corresponding to '0's in the source area are written with the contents of the background color register(s). This is the analog of Extended Write mode 5.

For the CL-GD5429, the Background Color registers are ignored when transparency is enabled. The Foreground Color registers are used as indicated in TableD8–6.

Table D8–6. Color Expansion with Transparency ('1' in Source)

GR30[4]	Width	GR1	GR11
0	8-bit	Color	Don't care
1	16-bit	Low byte	High byte

8. COLOR EXPANSION with LEFT EDGE CLIPPING (CL-GD5429 Only)

For the CL-GD5429 only, if registers GR2F[2:0] are programmed to any value other than zero, the first *n* pixels of each scanline of the destination will not be written. The destination address must be on an eight pixel boundary. This is typically used in conjunction with pattern fills with color expansion.

9. PATTERN FILLS

In some cases it is necessary to fill an area with a repeating pattern. The CL-GD542X BitBLT engine has provisions for pattern replication with or without color expansion. The pattern size is 8 pixels x 8 pixels, chosen for compatibility with Microsoft Windows.

If GR30[6] is programmed to a '1', the source is taken to be an array of 8 pixels x 8 pixels. It will be repeatedly copied to the destination area with, color expansion if necessary. For any scanline, the same eight pixels of source data are used repeatedly. The source pitch will be ignored. The number of bytes in the source pattern is a function of the operating mode, as indicated in Table D8-5.

Table D8–7. Source for Pattern Fills

Operating Mode	Arrangement	Starting Address Boundary
Color Expansion	8 bytes of monochrome data for 64 pixels	8 bytes
8-bit pixels	64 bytes of color data for 64 pixels	64 bytes
16-bit pixels	128 bytes of color data for 64 pixels	128 bytes
32-bit pixels	256 bytes of color data for 64 pixels	256 bytes

10. PATTERN VERTICAL PRESET (CL-GD5429 Only)

The CL-GD5429 supports pattern vertical preset for pattern fill with Color Expansion. The low-order 3 bits of the Source Start Address (GR2C[2:0]) selects the eight pixels to be used for the first (or only) scanline. This is possible because the pattern must be in an eight-byte boundary. This makes it possible to force vertical alignment of the pattern. The vertical alignment is useful for the filled rectangles and polygons described below.

11. PATTERNED POLYGON FILLS (CL-GD5429 Only)

The CL-GD5429 has special provisions for patterned polygon fills. The polygon to be filled is decomposed into a series of single scanlines, each of which are filled with a single BitBLT. The first such operation will read all eight bytes of monochrome pattern. Thereafter, so long

as no writes to the Source Start Address registers or to the BLT Mode register occur, subsequent operations will use the previously loaded source data (skipping the read cycle). In addition, the Y offset initially set by the three low-order bits of the Source Start Address (GR2C[2:0]) will be incremented modulo eight at the end of each operation. This results in each scan line starting one byte further into the pattern than the scanline immediately above. The polygon may be filled with a series of single scanline fills that change only the Destination Start Address, left-edge pixel clipping, and width. The operation should proceed from top to bottom (if it goes from bottom to top, the pattern will be vertically flipped).

12. BLT DIRECTION

If the source and destination areas overlay in display memory, one must be certain that the operation progresses so that the source area is not overwritten prior to being used. Consider Figure D8-3. If the operation were to begin with the upper left corner of the source and destination, the contents of the overlapped area would be overwritten before being used.

If register GR30[0] is programmed to a '1', the direction in which the operation progresses will be reversed. The bytes will be processed right-to-left and bottom-to-top. In Figure D8-3 this guarantees that bytes of the source are used prior to being changed. Observe that the start addresses in this case are the highest in the areas, not the lowest.

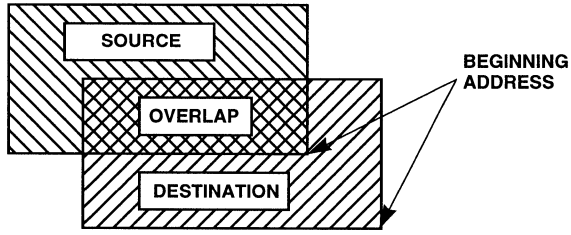

Figure D8–3. Overlapping BLT

13. SYSTEM MEMORY

The source area or the destination area, but not both, of a BitBLT can be system memory. What this really means from the point of view of the CL-GD542X is that the source or destination is the system bus. If either the source or destination of a BLT is system memory, SR8[6] *must* be programmed to '0'.

If GR30[2] is programmed to a '1', the BLT source will be system memory. The CPU must perform the bus transfers; the CL-GD542X is never a bus master. The address provided by the CPU with such transfers is ignored (except it must be in the range being decoded as display memory). The CPU *must* execute DWORD transfers (even though these would be broken into pairs of WORD transfers for ISA bus).

For system-to-screen BitBLTs, up to three bytes of the last transfer for each scanline will be ignored (depending on width). The next scanline will begin with the next DWORD transfer.

If GR30[1] is programmed to a '1', the BLT destination will be system memory. The CPU will perform the bus transfers; the CL-GD542X is never a bus master. The address provided by the CPU for such transfers is ignored (except it must be in the range being decoded as display memory). The CPU *must* execute DWORD transfers (even though these would be broken into pairs of WORD transfers for ISA bus). The CL-GD542X will pad each scanline with up to three indeterminate bytes (depending on width). BLTs involving color expansion or pattern copy cannot use this mode.

14. START/SUSPEND/RESET CONTROLS

Once the parameters have been loaded into the registers the BitBLT can be started. It is possible to suspend and then resume a BitBLT. It is also possible to unconditionally reset the BitBLT engine. These functions are controlled by bits in GR31.

Register GR31[1] is programmed to a '1' to start a BLT. So long as the BLT is in progress, GR31[0] will be a '1'. When the BLT has completed, GR31[0] will be a '0'. Monitoring GR31[0] is the most straight-forward way to synchronize with the BitBLT engine. While the BLT is in progress, the CL-GD542X display memory and BLT registers (except GR31) must not be accessed for read or write.

It is possible to suspend a BLT by programming register GR31[1] to '0'. Register GR31[0] must be monitored to determine when the BLT has actually been suspended and it is safe to access display memory. When register GR31[0] is a zero, then the BLT has been successfully suspended or has been completed.

When a BLT has been suspended, the CPU may access display memory only for write operations. If the program reads display memory during a suspended BLT, working registers will be overwritten and the first few bytes of the BLT, when it is resumed, will use invalid data.

The CPU can determine whether a suspended BLT was actually suspended, or went to completion coincidentally with the suspension, by reading GR31[3]. If it is a '1', the BLT was suspended and must be resumed. If it is a '0', the BLT was actually completed and need not be resumed. The BLT is resumed by programming GR31[1] to a '1'. BLTs can be suspended and resumed multiple times.

The current operation can be unconditionally stopped, and the entire BitBLT engine reset by programming GR31[2] to a '1'. GR31[3] and GR31[0] will be forced to '0' and the operation will stop after the next write. This may result in partial pixels being written.

NOTE: A BLT operation that is reset *cannot* be resumed.

15. COMPLETE BLT REGISTER LIST

Table D8-6 lists every register associated with the BitBLT engine.

Table D8–8. BLT Register List

Register	Memory-Mapped I/O Offset (Hex)	How Used	Size (Bits)	Modified?	Note
GR0	00	Background Color byte 0	8	No	–
GR1	04	Foreground Color byte 0	8	No	–
GR10	01	Background Color byte 1	8	No	–
GR11	05	Foreground Color byte 1	8	No	–
GR20	08	Width byte 0	8	–	–
GR21	09	Width byte 1	3	–	–
GR22	0A	Height byte 0	8	No	–
GR23	0B	Height byte 1	2	No	–
GR24	0C	Destination Pitch byte 0	8	No	–
GR25	0D	Destination Pitch byte 1	4	No	5 bits on CL-GD5429
GR26	0E	Source Pitch byte 0	8	No	–
GR27	0F	Source Pitch byte 1	4	No	5 bits on CL-GD5429
GR28	10	Destination Start byte 0	8	Yes	–
GR29	11	Destination Start byte 1	8	Yes	–
GR2A	12	Destination Start byte 2	5	Yes	–
GR2B	13	Reserved			–
GR2C	14	Source Start byte 0	8	Yes	–
GR2D	15	Source Start byte 1	8	Yes	–
GR2E	16	Source Start byte 2	5	Yes	–
GR2F	17	Destination Write Mask	3	No	CL-GD5429 only
GR30	18	BLT mode	8	No	–
GR31	40	Start/Status	4	–	–
GR32	1A	ROP	8	No	–
GR33	1B	BLT reserved	–	–	–
SR2	–	Plane Mask register	8	No	–

16. MEMORY-MAPPED I/O (CL-GD5429 only)

All the registers listed above, except SR2, can be written as memory locations. This is called Memory-mapped I/O. This makes it possible to load the registers more quickly because they can be written four-per-access. This capability is unique to the CL-GD5429.

Memory-mapped I/O is enabled when SR17[2] is programmed to a '1'. The registers are mapped beginning at address B800:0. The CL-GD5430 can be programmed to place the Memory-mapped I/O area at the last 256 bytes of the linear address space. GR6[3:2] must be programmed to 01. When Memory-mapped I/O is enabled, only GR31 is accessible as an I/O location. Appendix B20, *Memory-mapped I/O*, contains a list of registers ordered by offset.

17. MISCELLANEA

BLT Registers Modified: A few of the registers associated with a BLT are modified while the BLT is occurring. Therefore, they must be re-written prior to the next BLT even if the initial values are to be the same. An exception is the Height registers (GR22/GR23). A working copy of this field is made when the BLT begins so that the field itself is not changed. This is useful for repeatedly drawing horizontal lines and for patterned polygon fills.

18. EXAMPLES

Text Expansion Example: Using color expansion, a text string is copied from system memory. The monochrome image of the string is arranged in system memory by scanline. The destination area is 150 pixels x 25 scanlines, 8-bits-per-pixel. The destination pitch is 1024 pixels. The registers must be loaded as indicated in Table D8–9. If the background pixels are not to be written, GR30[3] would be set to a '1'.

Table D8–9. Text Expansion BLT

Register(s)	Contents (Decimal)	Field	How Calculated
GR0/GR10	xx	Background Color	As desired
GR1/GR11	xx	Foreground Color	As desired
GR20/GR21	149	Width	150 - 1
GR22/GR23	24	Height	25 - 1
GR24/GR25	1024	Destination Pitch	-
GR26/GR27	n/a	Source Pitch	(System memory)
GR28/GR29/GR2A	xxxxx	Destination Start	-
GR2C/GR2D/GR2E	n/a	Source Start	(System memory)
GR2F	0	Write Mask	No Clipping

Table D8–9. Text Expansion BLT *(cont.)*

Register(s)	Contents (Decimal)	Field	How Calculated
GR30	84h	Mode	Color Expansion, System Memory Source
GR32	0Dh	Raster Op	SRC COPY
GR33	0	Mode Extension	Unused
GR31	2	Start	Set bit 1

After the registers are loaded the source bitmap must be transferred. The first DWORD write will transfer the image for pixels 0-31. The second write will transfer the image for pixels 32-63. The third will transfer 64-95, and the fourth will transfer 96-127. The fifth DWORD transfer is special. The data for this transfer is shown in Figure D8-4.

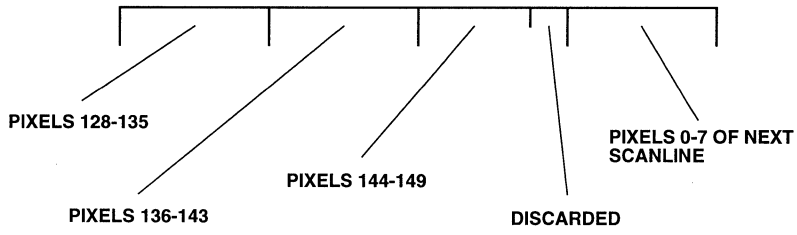

Figure D8–4. Color Expand Transfer

A total of 119 DWORD transfers will be required; the last one byte of the last transfer will be discarded.

Appendix D9

Cirrus Logic Bulletin Board Service

CIRRUS LOGIC BBS

1. INTRODUCTION

This appendix discusses the Cirrus Logic BBS (Bulletin Board Service) which is intended primarily for one-way communication from Cirrus Logic to its OEMs and end users. The latest drivers are available to Cirrus Logic OEMs and end users, but only Cirrus Logic OEMs can obtain the latest BIOS images over the BBS.

Cirrus Logic maintains strict access control to this bulletin board to minimize the possibility of distribution of pirated or virus-ridden software. Only Cirrus Logic employees have upload access to publicly downloadable file areas. An end user or OEM can upload files, but not to a publicly downloadable area.

The software running on this board is Wildcat!™ IM, written by Mustang Software®, Inc. Cirrus Logic operates eight remote nodes and one local node to the BBS.

2. TELEPHONE NUMBER AND COMMUNICATION PARAMETERS

The telephone number of the Cirrus Logic BBS is (510) 440-9080. The communication parameters are:

- 8 data bits
- no parity
- 1 stop bit

The Cirrus Logic BBS line supports up to a 14,400 baud rate. However, baud connections of 300 and 1200 bps are allowed, as long those connections do not prohibit access and cause complaints to be registered.

3. FIRST-TIME LOG ON

Upon connection with the bulletin board, the name and password fields have default entries for a guest account. If merely downloading drivers, demonstration programs, or utilities, use the default entry. This avoids filling out the questionnaire and purging the user database, yet allows access to most files.

If schematic diagrams or BIOS files are required, or if planning to upload files, log on with your name (or company name). The system will prompt a password entry and require that the questionnaire be completed. When completed, the name and password chosen is added to the user database and access is the same as a guest log on.

4. UPGRADED ACCESS

If requiring access to BIOS image or schematic diagram files, or if exchanging files with Cirrus Logic personnel on a regular basis, an upgrade of your account is necessary. Account upgrades are handled through your contact at Cirrus Logic (usually through a sales office).

Setting up an upgrade account requires one working day from the time of request. Three to five working days are required for the request to be processed after being received at Cirrus Logic in Fremont, California.

5. ORGANIZATION OF THE BOARD

The Cirrus Logic BBS is organized into 'Product' areas and a 'General Public Messages' area. The Product areas, as of October 1993, are listed in Table D9–1.

Table D9–1. Product Areas

Area	Name	Note
1	General Public Messages	Non-specific programs, README, etc.
2	510/520	
3	5320	
4	5410	
5	5401/'02/'20	Software-wise, 5420 is related to 5401/'02
6	5422/'24/'26/'28/'29	
7	5434	Alpine
8	Northstar	Not yet open
9	Spare Desktop	Not yet open
10	610/620	
11	62XX	
12	634X	
13	641X	
14	642X	
15	6440	
16	Spare Laptop	Not yet open
17	Pixel Products	
18	Modems	
19	6710/6720	

The General Public Messages area contains non-specific programs such as PKWare and ID_CHIP. This area also contains README files that describe the contents and layout of the board. The upload areas also reside in the General Public Messages area. The upload areas are readable only by Cirrus Logic employees.

The other product areas are connected to five file areas each. These file areas are listed in Table D9–2.

Table D9–2. File Areas within Product Areas

File Area	Note	Download Access
Drivers	Driver disks	All
Demonstrations	BLT demo, slide viewers, etc.	All
Utilities	e.g., CLMODE	All
BIOS	BIOS images, MFGTST	Integrator, OEM
Schematics	ORCAD schematic diagrams	OEM

Appendix E1

VGA BIOS

External Function Specification

VGA BIOS EXTERNAL FUNCTION SPECIFICATION

1. INTRODUCTION

This document provides a specification for the external software interface of the Cirrus Logic VGA BIOS (Basic Input/Output System).

The Cirrus Logic VGA BIOS is fully compatible with the standard IBM® VGA BIOS and the Interrupt 10h video service functions. This document does not describe the standard Interrupt 10h functions. These functions are described in detail in various other public documents (see the list of literature in Appendix F1).

All interface extensions to the standard VGA BIOS are fully described in this document.

1.1 Main Features

The Cirrus Logic BIOS is a high-performance firmware product designed to take maximum advantage of the Cirrus Logic VGA controller, especially in the areas of display quality, power management and video performance. The following are some of the major features of the product:

- 100% IBM® VGA-compatible BIOS
- High performance operation
- Modular, proven design
- Adapter or system board implementation (or C000/E000 segments)
- Can be integrated with system BIOS
- Supports switchless configuration
- Can be customized without source code
- VESA®-compatible modes
- VESA®-compatible INT 10h interface

1.2 Implementation Type

The Cirrus Logic VGA controller and BIOS can be implemented as an adapter board or placed directly on the motherboard. The following two sections describe specific information relating to implementation type.

1.2.1 Adapter Implementation

When the video subsystem is implemented as an optional video adapter, the video BIOS will reside at segment C000h for a length of 32K bytes.

The video subsystem is initialized in the standard method. The BIOS will begin with 55h, AAh, and a length indicator. The indicated length will check-sum to a '0', modulo 256. The planar BIOS will make a far call to C000:3 to initialize the video subsystem at power-up.

1.2.2 Planar Implementation

When the video subsystem is implemented as an integral part of the system, the BIOS will reside at segment E000h. The planar BIOS must make a far call to E000:3 to initialize the video subsystem at power-up. This initialization must occur, and must occur prior to initializing any adapter video BIOS. Initialization of optional video adapter ROM BIOS at C000h will be done in the standard manner.

For the video subsystem to co-exist with adapter video subsystems, control must be transferred to the video BIOS at E000h from the F000:F065 entry point. The motherboard BIOS must place a far jump to E000:1B at F000:F065. The E000h video BIOS will handle all requirements of CGA and MGA adapters, and coexist with compatible VGA adapters.

For the video subsystem to operate in some environments, a direct BIOS entry is provided to call some BIOS functions without using the interrupt vector table or BIOS data areas in low memory. At offset E000:0019 or C000:0019 is a data word that contains the offset of the VGA BIOS entry point. This word points to the instruction immediately following the CLI clear interrupt instruction. The BIOS preserves the state of the interrupt flag internally, so if interrupts are disabled upon entry through this point, they will remain disabled throughout execution of the BIOS. Note that only certain BIOS functions, such as save/restore state should be used unless the interrupt table and BIOS data area are correctly initialized.

1.3 Configuration

1.3.1 INT 15 Support

The system BIOS should implement INT 15h AX=448EH. This is a signal that the video BIOS is ready to accept INT 10 option calls. When this interrupt is received, the system BIOS should perform any option selection required via INT 10h Function 12h, as described in this document. Note that the video BIOS invokes this INT 15 call prior to the initial mode set and displaying the sign-on message.

1.3.2 Scratch Register Definitions

For motherboard implementation without the EEPROM, an INT 15 call is made by the CLMODE Utility to pass configuration changes to the motherboard BIOS to be saved in the CMOS memory.

Input:	AX=	448Fh
	DL=	SRA
	DH=	SR9

The INT 15 routine service should clear the Carry bit to indicate that the call is supported. The use of these registers is explained below.

SR09:	7:6	1024 x 768 Frequency
	5:4	800 x 600 Frequency
	3:2	Maximum Resolution
	1:0	Unused (for OEM use)
SR0A:	7	Reserved
	6	High refresh (640 x 480 Frequency)
	5	Reserved
	4:3	Memory Size (00=256, 01=512, 10=1 Mbyte, 11=2 Mbyte)
	2:1	Reserved
	0	16/8-bit memory (1=16 bit, 0=8 bit)

2. VIDEO MODES

The Cirrus Logic VGA BIOS supports all standard VGA modes. These standard VGA modes are listed in the following table.

Table E1–1. Standard VGA Modes

Mode No.	VESA® Mode No.	No. of Colors	Char. x Row	Char. Cell	Pixels	Display Mode	Horiz. Freq.	Vert. Freq.
00/01	–	16/256	40 x 25	8 x 8	320 x 200	Text	31.5	70
00*/01*	–	16/256	40 x 25	8 x 14	320 x 350	Text	31.5	70
00+/01+	–	16/256	40 x 25	9 x 16	360 x 400	Text	31.5	70
02/03	–	16/256	80 x 25	8 x 8	640 x 200	Text	31.5	70
02*/03*	–	16/256	80 x 25	8 x 14	640 x 350	Text	31.5	70
02+/03+	–	16/256	80 x 25	9 x 16	720 x 400	Text	31.5	70
04/05	–	4/256	40 x 25	8 x 8	320 x 200	Graphics	31.5	70
6	–	2/256	80 x 25	8 x 8	640 x 200	Graphics	31.5	70
07*	–	Monochrome	80 x 25	9 x 14	720 x 350	Text	31.5	70
07+	–	Monochrome	80 x 25	9 x 16	720 x 400	Text	31.5	70
0D	–	16/256	40 x 25	8 x 8	320 x 200	Graphics	31.5	70
0E	–	16/256	80 x 25	8 x 8	640 x 200	Graphics	31.5	70
0F	–	Monochrome	80 x 25	8 x 14	640 x 350	Graphics	31.5	70
10	–	16/256	80 x 25	8 x 14	640 x 350	Graphics	31.5	70
11	–	2/256	80 x 30	8 x 16	640 x 480	Graphics	31.5	60
12	–	16/256	80 x 30	8 x 16	640 x 480	Graphics	31.5	60
13	–	256/256	40 x 25	8 x 8	320 x 200	Graphics	31.5	70

The CL-GD540X and CL-GD542X VGA BIOS supports standard VESA® and Extended Modes. These modes are listed in Table E1–2.

Table E1–2. Cirrus Logic Extended Video Modes

Mode No.	VESA® No.	No. of Colors	Char. x Row	Char. Cell	Screen Format	Display Mode	Pixel Freq. MHz	Horiz. Freq. kHz	Vert. Freq. Hz
14	–	16/256K	132 x 25	8 x 16	1056 x 400	Text	41.5	31.5	70
54	10A	16/256K	132 x 43	8 x 8	1056 x 350	Text	41.5	31.5	70
55	109	16/256K	132 x 25	8 x 14	1056 x 350	Text	41.5	31.5	70
58, 6A	102	16/256K	100 x 37	8 x 16	800 x 600	Graphics	36	35.2	56
58, 6A	102	16/256K	100 x 37	8 x 16	800 x 600	Graphics	40	37.8	60
58, 6A	102	16/256K	100 x 37	8 x 16	800 x 600	Graphics	50	48.1	72
5C	103	256/256K	100 x 37	8 x 16	800 x 600	Graphics	36	35.2	56
5C	103	256/256K	100 x 37	8 x 16	800 x 600	Graphics	40	37.9	60
5C	103	256/256K	100 x 37	8 x 16	800 x 600	Graphics	50	48.1	72
5D†	104	16/256K	128 x 48	8 x 16	1024 x 768	Graphics	44.9	35.5	87†
5D	104	16/256K	128 x 48	8 x 16	1024 x 768	Graphics	65	48.3	60
5D	104	16/256K	128 x 48	8 x 16	1024 x 768	Graphics	75	56	70
5D	104	16/256K	128 x 48	8 x 16	1024 x 768	Graphics	77	58	72
5F	101	256/256K	80 x 30	8 x 16	640 x 480	Graphics	25	31.5	60
5F	101	256/256K	80 x 30	8 x 16	640 x 480	Graphics	31.5	37.9	72
60†	105	256/256K	128 x 48	8 x 16	1024 x 768	Graphics	44.9	35.5	87†
60	105	256/256K	128 x 48	8 x 16	1024 x 768	Graphics	65	48.3	60
60	105	256/256K	128 x 48	8 x 16	1024 x 768	Graphics	75	56	70
60	105	256/256K	128 x 48	8 x 16	1024 x 768	Graphics	77	58	72
64	111	64K	–	–	640 x 480	Graphics	25	31.5	60
64	111	64K	–	–	640 x 480	Graphics	31.5	37.9	72
65	114	64K	–	–	800 x 600	Graphics	36	35.2	56
65	114	64K	–	–	800 x 600	Graphics	40	37.8	60
66	110	32K‡	–	–	640 x 480	Graphics	25	31.5	60
66	110	32K‡	–	–	640 x 480	Graphics	31.5	37.9	72
67	113	32K‡	–	–	800 x 600	Graphics	36	31.5	56

Table E1–2. Cirrus Logic Extended Video Modes *(cont.)*

Mode No.	VESA® No.	No. of Colors	Char. x Row	Char. Cell	Screen Format	Display Mode	Pixel Freq. MHz	Horiz. Freq. kHz	Vert. Freq. Hz
68†	–	32K‡	–	–	1024 x 768	Graphics	44.9	35.5	87†
6C†	106	16/256K	160 x 64	8 x 16	1280 x 1024	Graphics	75	48	87†
6D†	–	256/256K	160 x 64	8 x 16	1280 x 1024	Graphics	75	48	87†
71	112	16M	80 x 30	8 x 16	640 x 480	Graphics	25	31.5	60
74†	–	64K	–	–	1024 x 768	Graphics	44.9	35.5	87†

NOTES:

1) Some modes are not supported by all CL-GD542X controllers. Refer to the CL-GD542X Data Book and Software Release Kit for the list of Video modes supported by the CL-GD542X BIOS.
2) Some modes are not supported by all monitors. The fastest vertical refresh rate for the monitor type selected will be automatically used.
3) '‡' character stands for 32K Direct-Color/256-color Mixed mode.
4) '†' character stands for Interlaced mode.

3. INTERRUPT 10H INTERFACE EXTENSIONS

The Cirrus Logic BIOS supports all standard VGA BIOS Interrupt 10h video service functions. In addition, the BIOS provides extensive support for various features of the Cirrus Logic VGA controller. These functions are available as extended functions under Interrupt 10h.

The standard VGA BIOS Interrupt 10h video service functions are not described in this document.

All extended function calls will preserve the CPU registers, except those used to pass information from the BIOS.

3.1 Function Summary

Table E1–3 provides an overview of the extended functions provided by the Cirrus Logic BIOS.

Table E1–3. Extended Function Summary

AH Register	BL Register	Function
12h	80h	Inquire VGA type
12h	81h	Inquire BIOS version number
12h	82h	Inquire design revision code
12h	85h	Return installed memory
12h	93h	Force 8 bit
12h	9Ah	Inquire user options
12h	A0h	Query Video mode availability
12h	A1h	Read monitor type and ID
12h	A2h	Set monitor type (horizontal)
12h	A3h	Set VGA refresh
12h	A4h	Set monitor type (vertical)

3.2 Inquiry Functions

The inquiry functions are supported for all versions of the video BIOS. These functions allow applications software to determine and use other functions described in the user options.

3.2.1 Inquire VGA Type

This function provides a mechanism for software to determine the type of Cirrus Logic VGA controller, silicon revision number and its corresponding hardware capabilities. BIOS versions that do not support this family of function will preserve the input value in AL register.

Input:
AH= 12h
BL= 80h

Output:
AX= Controller type
0= No extended alternate select support
1= Reserved
2= CL-GD510/520
3= CL-GD610/620
4= CL-GD5320
5= CL-GD6410
6= CL-GD5410
7= CL-GD6420
8= CL-GD6412
10h= CL-GD5401
11h= CL-GD5402
12h= CL-GD5420
13h= CL-GD5422
14h= CL-GD5424
15h= CL-GD5426
16h= CL-GD5420r1
17h= CL-GD5402rl
18h= CL-GD5428
19h= CL-GD5429
20h= CL-GD6205/15/25
30h= CL-GD5432
31h= CL-GD5434

BL= Silicon revision number
0-7Fh= Silicon revision
80h= Silicon revision number not available

3.2.2 Inquire BIOS Version Number

This function provides a mechanism for software to determine the BIOS version number.

Input:
AH= 12h
BL= 81h

Output:
AH= Major BIOS version number
AL= Minor BIOS version number

Example: If BIOS version is 1.02, then AH is 01 and AL is 02.

3.2.3 Inquire Cirrus Logic Design Revision Code

This function provides a mechanism for software to determine the revision of Cirrus Logic silicon.

Input: AH= 12h
BL= 82h

Output: AL= Chip revision

3.2.4 Return Installed Memory

The function returns the amount of video memory present in 64K units.

Input: AH= 12h
BL= 85h

Output: AL= Amount of video memory present in 64K units.

3.3 Miscellaneous Functions

The functions in this section are miscellaneous chipset functionality.

3.3.1 Force 8-Bit Operation

This function forces 16-bit operation in an environment where 16-bit operation is possible. Takes effect immediately.

Input: AH= 12h
BL= 93h

AL= 0 Run as 16-bit device
AL= 1 Force 8-bit operation

Output: Nothing

3.4 Additional Functions

The functions in this section support various features of the Cirrus Logic VGA controller.

3.4.1 Inquire User Options

This function returns the current status of user options.

Input:
AH= 12h
BL= 9Ah

Output:
AX= Contains the following options
- Bits 1:0= Reserved
- Bits 4:2= Monitor Type (Horizontal)
- Bits 6:5 Vertical montype maximum resolution
- Bits 9:7= Reserved
- Bit 10= Force 8-bit operation (0=16-bit, 1=8-bit)
- Bits 13:11= Reserved
- Bit 14= Vertical montype 640 x 480 frequency (VGA refresh)
- Bit 15= Reserved

BX= Reserved
CX= Contains the following options
- Bits 3:0= Reserved
- Bits 5:4= Vertical montype 1280 x 1024 frequency
- Bits 10:6= Reserved
- Bits 12:11= Vertical montype 800 x 600 frequency
- Bits 15:13= Vertical montype 1024 x 768 frequency

DX= Reserved

3.5 Global Functions

3.5.1 Query Video Mode Availability

Input:
AH= 12h
AL= Video mode number (0-7fh)
BL= A0h

Output:
AH= Bit 0
- 0= Video mode not supported
- 1= Video mode supported

DS:SI: Pointer to standard video parameters, or FFFF:FFFF if standard parameters undefined for this mode
ES:DI: Pointer to supplemental video parameters, or FFFF:FFFF if supplemental parameters undefined for this mode

BX= Offset to BIOS sub-routine that will fix up the parameters pointed to by DS:SI. This routine requires ES:DI points to the proper supplemental video parameters.

3.5.2 Read Monitor ID/Type

This function reads the Monitor ID and senses the type of monitor attached.

Input:
AH = 12h
BL = A1h Read monitor ID and type from 15-pin connector

Output:
BH = Monitor ID
09h = IBM 8604/8507 or equivalent
0Ah = IBM 8514 or equivalent
0Bh = IBM 8515 or equivalent
0Dh = IBM 8503 or equivalent
0Eh = IBM 8512/8513 or equivalent
0Fh = No monitor
00..08, 0C = reserved

BL = Monitor gender
00 = Color display
01 = Grayscale display
02 = No display

3.5.3 Set Monitor Type (Horizontal)

This function sets the monitor type in terms of horizontal timings. The monitor type information is used by the BIOS to select the optimal display timings for extended modes. The current monitor type can be read back using Function 9A.

Input:
AH = 12h
BL = A2h Set monitor type

AL = Monitor type to set
0 = VGA (31.5 kHz)
1 = 8514-compatible (31.5kHz and 35.5 kHz(i))
2 = Super VGA (31.5 kHz - 35.1 kHz)
3 = Extended Super VGA (31.5 kHz - 35.5 kHz)
4 = Multi-freq. (31.5 kHz - 37.8 kHz)
5 = Extended multi-freq. (31.5 kHz - 48.0 kHz)
6 = Super multi-freq. (31.5 kHz - 56.0 kHz)
7 = Extended super multi-freq. (31.5 kHz - 64.0 kHz)

Output: Nothing

3.5.4 Set Refresh Type

This function toggles the VGA refresh rate between normal vertical refresh and high vertical refresh for flicker reduction. The current refresh can be read back using Function 9A.

Input:
AH = 12h
BL = A3h Set High/Low VGA refresh
AL = Enable/disable
1 = Enable high refresh
0 = Use normal VGA refresh

Output: Nothing

3.5.5 Set Monitor Type (Vertical)

This function sets the monitor type in terms of vertical timings. The monitor type information is used by the BIOS to determine which frequency to use when selecting an extended mode. It also is used to define what mode resolutions are available. The vertical monitor type can be read back using Function 9A. Calls to Function 0A2h (Set Monitor Type - Horizontal) and Function 0A3h (Set Refresh Type) will be converted into vertical equivalents, thus affecting the state of the maximums allowed.

Input:
AH = 012h
BL = 0A4h
AL[3:0] = Maximum Vertical Resolution
000h = 480 scanlines
001h = 600 scanlines
002h = 768 scanlines
003h = 1024 scanlines
004h - 00Fh = Reserved
AL[7:4] = 640 x 480 Frequency
000h = 60 Hz
001h = 72 Hz
002h - 00Fh = Reserved
BH[3:0] = 800 x 600 Frequency
000h = 56 Hz
001h = 60 Hz
002h = 72 Hz
003h - 00Fh = Reserved
BH[7:4] = 1024 x 768 Frequency
000h = 87i Hz
001h = 60 Hz
002h = 70 Hz
003h = 72 Hz
004h = 76 Hz
005h - 00Fh = Reserved
CH[7:4] = 1280 x 1024 Frequency
000h = 87i Hz
001h = 60 Hz
002h = 70 Hz
003h - 00Fh = Reserved
CL = Reserved
DX = Reserved

4. VESA® SUPER VGA STANDARD

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Purpose: To standardize a common software interface to Super VGA video adapters to provide simplified software application access to advanced VGA products.

Summary: The standard provides a set of functions that an application program can use to:

a) Obtain information about the capabilities and characteristics of a specific Super VGA implementation.
b) Control the operation of such hardware in terms of video mode initialization and video memory access. The functions are provided as an extension to the VGA BIOS video services, accessed through INT 10h.

4.1 Goals and Objectives

The purpose of the VESA VGA BIOS Extension is to provide a common software interface for developers to design applications that work on widely disparate architectures. Being a common software interface to Super VGA graphics products, the primary objective is to enable application and system software to adapt to and exploit the wide range of features available in these VGA extensions.

The VESA BIOS Extension attempts to address the following two main issues:

a) Return information about the video environment to the application
b) Assist the application in initializing and programming the hardware.

4.1.1 Video Environment Information

The VESA BIOS Extension provides several functions to return information about the video environment. These functions return system-level information as well as video-mode-specific details. Function 00h returns general system-level information, including an OEM identification string. The function also returns a pointer to the supported video modes. Function 01h may be used by the application to obtain information about each supported video mode. Function 03h returns the current video mode.

4.1.2 Programming Support

The VESA BIOS Extension provides several functions to interface to the different Super VGA hardware implementations. The most important of these is Function 02h, Set Super VGA Video mode. This function isolates the application from the tedious and complicated task of setting up a video mode. Function 05h provides an interface to the underlying memory-mapping hardware. Function 04h enables an application to save and restore a Super VGA state without determining specifics of the particular implementation.

4.1.3 Compatibility

The primary design objective of the VESA BIOS Extension is to preserve maximum compatibility to the standard VGA environment. In no way should the BIOS extensions compromise compatibility or performance. Another related concern is to minimize the changes necessary to an existing VGA BIOS. RAM- as well as ROM-based implementations of the BIOS extension should be possible.

4.2 Standard VGA BIOS

A primary design goal with the VESA BIOS Extension is to minimize the effects on the standard VGA BIOS. Standard VGA BIOS functions should need to be modified as little as possible. This is important since ROM- as well as RAM-based versions of the extension may be implemented.

Two standard VGA BIOS functions are affected by the VESA extension. These are Function 00h (Set Video mode) and Function 0Fh (Read current video state). VESA-aware applications will not set the video mode using VGA BIOS Function 00h. Nor will such applications use VGA BIOS Function 0Fh. VESA BIOS Functions 02h (Set Super VGA mode) and 03h (Get Super VGA mode) will be used instead.

VESA-unaware applications (such as old Pop-up programs and other TSRs, or the CLS command of MS-DOS), might use VGA BIOS Function 0Fh to get the present video mode. Later it may call VGA BIOS Function 00h to restore/re-initialize the old video mode.

To make such applications run properly, VESA recommends that whatever value returned by VGA BIOS Function 0Fh (it is the OEM's responsibility to define this number), it can be used to re-initialize the video mode through VGA BIOS Function 00h. Thus, the BIOS should record the last Super VGA mode in effect.

It is recommended, but not mandatory, to support output functions (such as TTY-output, scroll, set pixel, etc.) in Super VGA modes. If the BIOS extension doesn't support such output functions, Bit D2 (Output functions supported) of the ModeAttributes field (returned by VESA BIOS Function 01h) should be cleared.

4.3 Super VGA Mode Numbers

Standard VGA mode numbers are 7-bits-wide and presently ranges from 00h to 13h. OEMs have defined extended video modes in the range 14h to 7Fh. Values in the range 80h to FFh cannot be used, since VGA BIOS Function 00h (Set Video mode) interprets bit 7 as a flag to clear/not clear video memory.

Due to the limitations of 7-bit mode numbers, VESA Video mode numbers are 15-bits-wide. To initialize a Super VGA mode, its number is passed in the BX register to VESA BIOS Function 02h (Set Super VGA mode).

The format of VESA mode numbers is as follows:

D0-D8=	Mode number If D8 = 0, this is not a VESA-defined mode If D8 = 1, this is a VESA-defined mode
D9-D14=	Reserved by VESA for future expansion (= 0)
D15=	Reserved (= 0)

4.4 Extended VGA BIOS

Several new BIOS calls have been defined to support Super VGA Modes. For maximum compatibility with the standard VGA BIOS, these calls are grouped under one function number. This number is passed in the AH Register to the INT 10h handler.

The designated Super VGA extended function number is 4Fh. This function number is presently unused in most, if not all, VGA BIOS implementations. A standard VGA BIOS performs no action when function call 4F is made. Super VGA Standard VS911022 defines subfunctions 00H through 08H. Subfunction numbers 09H through 0FFH are reserved for future use.

4.4.1 Status Information

Every function returns status information in the AX register. The format of the status word is as follows:

AL =	4Fh:	Function is supported
AL ! =	4Fh:	Function is not supported
AH =	00h:	Function call successful
AH =	01h:	Function call failed

Software should treat a non-zero value in the AH register as a general failure condition. In later versions of the VESA BIOS Extension new error codes might be defined.

4.4.2 Function 00h — Return Super VGA information

The purpose of this function is to provide information to the calling program about the general capabilities of the Super VGA environment. The function fills an information block structure at the address specified by the caller. The information block size is 256 bytes.

Input: AH= 4Fh Super VGA support
AL= 00h Return Super VGA information
ES:DI= Pointer to buffer

Output: AX= Status
All other registers are preserved.

The information block has the following structure:

```
VgaInfoBlock struc
    VESASignature   db      'VESA'          ; 4 signature bytes
    VESAVersion     dw      ?               ; VESA version number
    OEMStringPtr    dd      ?               ; Pointer to OEM string
    Capabilities    db      4 dup (?)       ; capabilities of the video environment
    VideoModePtr    dd      ?               ; pointer to supported Super VGA Modes
    TotalMemory     dw      ?               ; Number of 64kb memory blocks on board
    Reserved        db      236 dup (?)     ; Remainder of VgaInfoBlock
VgaInfoBlock ends
```

The VESASignature field contains the characters 'VESA' if this is a valid block.

The VESAVersion is a binary field that specifies what level of the VESA standard the Super VGA BIOS conforms to. The higher byte specifies the major version number. The lower byte specifies the minor version number. The current VESA version number is 1.2. Applications written to use the features of a specific version of the VESA BIOS Extension are guaranteed to work in later versions. The VESA BIOS Extension will be fully upwards compatible.

The OEMStringPtr is a far pointer to a null-terminated OEM-defined string. The string may used to identify the video chip, video board, memory configuration, etc., to hardware-specific display drivers. There are no restrictions on the format of the string.

The Capabilities field describes what general features are supported in the video environment. The bits are defined as follows:

D0= DAC is switchable
0 = DAC is fixed width, with 6-bits per primary color
1 = DAC width is switchable
D1-31 = Reserved

The VideoModePtr points to a list of supported Super VGA (VESA-defined as well as OEM-specific) Mode numbers. Each mode number occupies one word (16 bits). The list of mode numbers is terminated by a -1 (0FFFFh). Please refer to Section 4.3 for a description of VESA mode numbers. The pointer could point into either ROM or RAM, depending on the specific implementation. Either the list would be a static string stored in ROM, or the list would be generated at run-time in the information block (see above) in RAM. It is the applications responsibility to verify the current availability of any mode returned by this Function through the Return Super VGA mode information (Function 1) call. Some of the returned modes may not be available due to the video boards current memory and monitor configuration.

The TotalMemory field indicates the amount of memory installed on the VGA board. Its value represents the number of 64K bytes blocks of memory currently installed.

4.4.3 Function 01h — Return Super VGA Mode Information

This function returns information about a specific Super VGA Video mode that was returned by Function 0. The function fills a mode information block structure at the address specified by the caller. The mode information block size is maximum 256 bytes.

Some information provided by this function is implicitly defined by the VESA mode number. However, some Super VGA implementations might support other video modes than those defined by VESA. To provide access to these modes, this function also returns various other information about the mode.

Input:	AH=	4Fh	Super VGA support
	AL=	01h	Return Super VGA Mode information
	CX=		Super VGA Video Mode number
	ES:DI=		Pointer to 256 byte buffer
Output:	AX=		Status
	All other registers are preserved.		

The mode information block has the following structure:

```
ModeInfoBlock   struc
; mandatory information

    ModeAttributes      dw      ?       ; mode attributes
    WinAAttributes      db      ?       ; window A attributes
```



```
        WinBAttributes      db      ?       ; window B attributes
        WinGranularity      dw      ?       ; window granularity
        WinSize             dw      ?       ; window size
        WinASegment         dw      ?       ; window A start segment
        WinBSegment         dw      ?       ; window B start segment
        WinFuncPtr          dd      ?       ; pointer to window function
        BytesPerScanLine    dw      ?       ; bytes per scanline extended information

        XResolution         dw      ?       ; horizontal resolution
        YResolution         dw      ?       ; vertical resolution
        XCharSize           db      ?       ; character cell width
        YCharSize           db      ?       ; character cell height
        NumberOfPlanes      db      ?       ; number of memory planes
        BitsPerPixel        db      ?       ; bits per pixel
        NumberOfBanks       db      ?       ; number of banks
        MemoryModel         db      ?       ; memory model type
        BankSize            db      ?       ; bank size in kb
        NumberOfImagePages  db      ?       ; Number of Images
        Reserved            db      1       ; reserved for page function

        RedMaskSize         db      ?       ;size of direct color red mask in  bits
        RedFieldPosition    db      ?       ;bit position of lsb of red mask
        GreenMaskSize       db      ?       ;size of direct color green mask in bits
        GreenFieldPosition  db      ?       ;bit position of lsb of green mask
        BlueMaskSize        db      ?       ;size of direct color blue mask in bits
        BlueFieldPosition   db      ?       ;bit position of lsb of blue mask
        RsvdMaskSize        db      ?       ;size of direct color reserved mask in bits
        RsvdFieldPosition   db      ?       ;bit position of lsb of reserved mask
        DirectColorModeInfo db      ?       ;Direct Color Mode attributes

        Reserved            db      216 dup (?)  ; remainder of ModeInfoBlock
ModeInfoBlock   ends
```

The ModeAttributes field describes certain important characteristics of the video mode. Bit D0 specifies whether this mode can be initialized in the present video configuration. This bit can be used to block access to a video mode if it requires a certain monitor type, and that this monitor is presently not connected. Bit D1 specifies whether extended mode information is available. This information is required in VESA BIOS Extension version 1.2 and later. Bit D2 indicates whether the BIOS have support for output functions such as TTY output, scroll, pixel output etc. in this mode (it is recommended, but not mandatory, that the BIOS have support for all output functions).

The field is defined as follows:

D0= Mode supported in hardware
- 0= Mode not supported in hardware
- 1= Mode supported in hardware

D1= Extended information available
- 0= Extended Mode information not available
- 1= Extended Mode information available

D2= Output functions supported by BIOS
- 0= Output functions not supported by BIOS
- 1= Output functions supported by BIOS

D3= Monochrome/Color Mode (see note below)
- 0= Monochrome Mode

1= Color Mode
D4= Mode type
0= Text Mode
1= Graphics Mode
D5-D15= Reserved

NOTE: Monochrome modes have their CRTC address at 3B4h. Color modes have their CRTC address at 3D4h. Monochrome modes have attributes in which only bit 3 (video) and bit 4 (intensity) of the attribute controller output are significant. Therefore, monochrome text modes have attributes of off, video, high intensity, blink, etc. monochrome graphics modes are two-plane graphics modes and have attributes of off, video, high intensity, and blink. Extended two-color modes that have their CRTC address at 3D4h, are color modes with one bit per pixel and one plane. The standard VGA modes, 06h and 11h would be classified as color modes, while the standard VGA modes 07h and 0fh would be classified as monochrome modes.

The BytesPerScanline field specifies how many bytes each logical scanline consists of. The logical scanline could be equal to or larger than the displayed scanline.

The WinAAttributes and WinBAttributes describe the characteristics of the CPU windowing scheme such as whether the windows exist and are read/writeable, as follows:

D0= Window supported
0= Window is not supported
1= Window is supported
D1= Window readable
0= Window is not readable
1= Window is readable
D2= Window writable
0= Window is not writeable
1= Window is writeable
D3-D7= Reserved

If neither window is supported (bit D0 = 0), then an application can assume that window paging is not supported, and that the display memory buffer resides at the CPU address appropriate for the MemoryModel of the mode.

The WinGranularity specifies the smallest boundary, in kilobytes, on which the window can be placed in the video memory. If WinGranularity equals a '0' then CPU display memory windowing is not supported.

The WinSize specifies the size of the window in kilobytes.

The WinASegment and WinBSegment address specify the segment addresses where the windows are located in the CPU address space.

The WinFuncAddr specifies the address of the CPU video memory windowing function. The windowing function can be invoked either through VESA BIOS Function 05h, or by calling the function directly. A direct call will provide faster access to the Hardware Paging registers than using INT 10h, and is intended to be used by high-performance applications. If WinFuncPtr is NULL (0000:0000) then CPU display memory windowing is not supported.

The XResolution and YResolution specify the width and height of the video mode. In graphics modes, this resolution is in units of pixels. In text modes this resolution is in units of characters. Note that text mode resolutions, in units of pixels, can be obtained by multiplying XResolution and YResolution by the cell width and height, if the extended information is present.

The XCharSize and YCharSize specify the size of the character cell in pixels.

The NumberOfPlanes field specifies the number of memory planes available to software in that mode. For standard 16-color VGA graphics, this would be set to a four. For standard Packed-pixel modes, the field would be set to a '1'.

The BitsPerPixel field specifies the total number of bits that define the color of one pixel. For example, a standard VGA Four-plane 16-color Graphics mode would have a four in this field and a packed-pixel 256-color Graphics Mode would specify a eight in this field. The number of bits per pixel per plane can normally be derived by dividing the BitsPerPixel field by the NumberOfPlanes field.

The MemoryModel field specifies the general type of memory organization used in this mode. The following models have been defined:

00h=	Text Mode
01h=	CGA graphics
02h=	Hercules graphics
03h=	Four-plane planar
04h=	Packed pixel
05h=	Non-chain4, 256 color
06h=	Direct Color
07h=	YUV
08h-0fh=	Reserved, to be defined by VESA
10h-ffh=	To be defined by OEM

In Version 1.1 and earlier of the VESA Super VGA BIOS Extension, Direct Color 1:5:5:5, 8:8:8, and 8:8:8:8 are defined as Packed-pixel model with 16, 24, and 32 bits per pixel, respectively. In Version 1.2 and later of the VESA Super VGA BIOS Extension, it is recommended that Direct-color modes use the Direct-color MemoryModel and use the MaskSize and FieldPosition fields of the ModeInfoBlock to describe the pixel format. BitsPerPixel is always defined to be the total size of the pixel, in bits.

The NumberOfBanks is the number of banks in which the scanlines are grouped. The remainder from dividing the scanline number by the number of banks is the bank that contains the scanline and the quotient is the scanline number within the bank. For example, CGA graphics modes have two banks and Hercules® Graphics mode has four banks. For modes that don't have scanline banks (such as VGA modes 0Dh-13h), this field should be set to a '1'.

The BankSize field specifies the size of a bank (group of scanlines) in units of 1K byte. For CGA and Hercules graphics modes this is a eight, as each bank is 8192 bytes in length. For modes that don't have scanline banks (such as VGA modes 0Dh-13h), this field should be set to a '0'.

The NumberOfImagePages field specifies the number of additional complete display images that will fit into the VGA memory, at one time, in this mode. The application may load more than one image into the VGA memory if this field is a non-zero, and flip the display between the images.

The Reserved field has been defined to support a future VESA BIOS extension feature and will always be set to a '1' in this version.

The RedMaskSize, GreenMaskSize, BlueMaskSize, and RsvdMaskSize fields define the size, in bits, of the red, green, and blue components of a Direct-color Pixel. A bit mask can be constructed from the MaskSize fields using simple shift arithmetic. Example MaskSize values for Direct-color 5:6:5 mode would be 5, 6, 5, and 0, for the red, green, blue, and reserved fields, respectively. The MaskSize fields should be set to a '0' in modes using a MemoryModel that does not have pixels with component fields.

The RedFieldPosition, GreenFieldPosition, BlueFieldPosition, and RsvdFieldPosition fields define the bit position within the Direct-color Pixel or YUV pixel of the least-significant bit of the respective color component. A color value can be aligned with its pixel field by shifting the value left by the FieldPosition. Example FieldPosition values for Direct-color 5:6:5 mode would be 11, 5, 0, and 0, for the red, green, blue, and reserved fields, respectively. The FieldPosition fields should be set to a '0' in modes using a MemoryModel that does not have pixels with component fields.

The DirectColorModeInfo field describes important characteristics of Direct-color Modes. Bit D0 specifies whether the color ramp of the DAC is fixed or programmable. If the color ramp is fixed, then it cannot be changed. If the color ramp is programmable, it is assumed that the red, green, and blue lookup tables can be loaded using a standard VGA DAC Color registers BIOS Call (AX=1012h). Bit D1 specifies whether the Rsvd field of the Direct-color pixel can be used by the application or is reserved, and thus unusable.

D0= Color ramp is fixed/programmable
- 0= Color ramp is fixed
- 1= Color ramp is programmable

D1= Rsvd field is usable/reserved
- 0= Rsvd field is reserved
- 1= Rsvd field is usable by the application

The MapFuncAddr specifies the address of the mapping function. The mapping function can be invoked either through VESA BIOS Function 06h, or by calling the function directly. A direct call will provide a faster memory mapping than using INT 10h, and is intended to be used by high-performance applications.

NOTE: Version 1.1 and later VESA BIOS extensions will zero-out all unused fields in the Mode Information Block, always returning exactly 256 bytes. This facilitates upward compatibility with future versions of the standard, as any newly-added fields will be designed such that values of zero will indicate nominal defaults or non-implementation of optional features. (For example, a field containing a bit-mask of extended capabilities would reflect the absence of all such capabilities.) Applications that wish to be backwards-compatible to Version 1.0 VESA BIOS extensions should pre-initialize the 256-byte buffer before calling Return Super VGA mode Information.

4.4.4 Function 02h — Set Super VGA Video Mode

This function initializes a video mode. The BX register contains the video mode number. The format of VESA mode numbers is described in Section 2. If the mode cannot be set, the BIOS should leave the video environment unchanged and return a failure error code.

Input:
AH= 4Fh Super VGA support
AL= 02h Set Super VGA Video Mode
BX= Video mode
D0-D14= Video mode number
D15= Clear memory flag
0= Clear video memory
1= Don't clear video memory

Output:
AX= Status
All other registers are preserved.

4.4.5 Function 03h — Return Current Video Mode

This function returns the current video mode in BX register. The format of VESA Video mode numbers is described in Section 2 of this document.

Input:
AH= 4Fh Super VGA support
AL= 03h Return current video mode

Output:
AX= Status
BX= Current video mode number
All other registers are preserved.

NOTE: In a standard VGA BIOS, Function 0Fh (Read current video state) returns the current video mode in the AL register. In D7 of AL register, it also returns the status of the Memory Clear bit (D7 of 40:87). This bit is set if the mode was set without clearing memory. In this Super VGA Function, the Memory Clear bit will not be returned in BX register since the purpose of the function is to return the video mode only. If an application must obtain the Memory Clear bit, it should call VGA BIOS Function Fh.

4.4.6 Function 04h — Save/Restore Super VGA Video State

These functions provide a mechanism to save and restore the Super VGA video state. The functions are a superset of the three subfunctions under standard VGA BIOS Function 1Ch (Save/restore video state). The complete Super VGA video state (except video memory) should be saveable/restorable by setting the requested states mask (in the CX register) to 000Fh.

Input:
AH= 4Fh Super VGA support
AL= 04h Save/Restore Super VGA video state
DL= 00h Return save/restore state buffer size
CX= Requested states
D0= Save/restore video hardware state
D1= Save/restore video BIOS data state
D2= Save/restore video DAC state
D3= Save/restore Super VGA state

Output: AX= Status
BX= Number of 64-byte blocks to hold the state buffer
All other registers are preserved.

Input:

AX=	4Fh	Super VGA support
AL=	04h	Save/Restore Super VGA video state
DL=	01h	Save Super VGA video state
CX=		Requested states (see above)
ES:BX=		Pointer to buffer

Output: AX= Status
All other registers are preserved.

Input:

AH=	4Fh	Super VGA support
AL=	04h	Save/Restore Super VGA video state
DL=	02h	Restore Super VGA video state
CX=		Requested states (see above)
ES:BX=		Pointer to buffer

Output: AX= Status
All other registers are preserved.

4.4.7 Function 05h — CPU Video Memory Window Control

This function sets or gets the position of the specified window in the video memory. The function allows direct access to the Hardware Paging registers. To use this function properly, the software should use VESA BIOS Function 01h (Return Super VGA mode information) to determine the size, location, and granularity of the windows.

Input:

AH=	4Fh	Super VGA support
AL=	05h	Super VGA video memory window control
BH=	00h	Select super VGA video memory window
BL=		Window number
	0=	Window A
	1=	Window B
DX=		Window position in video memory (in window granularity units)

Output: AX= Status
See note below.

Input:

AH=	4Fh	Super VGA support
AL=	05h	Super VGA video memory window control
BH=	01h	Return super VGA video memory window
BL=		Window number
	0=	Window A
	1=	Window B

Output:

AX=	Status
DX=	Window position in video memory (in window granularity units)

See note below.

NOTE: This function is also directly accessible through a far call from the application. The address of the BIOS function may be obtained by using VESA BIOS Function 01h, return Super VGA mode information. A field in the ModeInfoBlock contains the address of this function. Note that this function may be different among video modes in a particular BIOS implementation so the function pointer should be obtained after each set mode.

In the far call version, no status information is returned to the application. Also, in the far call version, the AX and DX registers will be destroyed. Therefore if AX and/or DX register must be preserved, the application must do so prior to making the far call.

The application must load the input arguments in BH, BL, and DX registers (for Set Window), but does not need to load either AH or AL register to use the far call version of this function.

4.4.8 Function 06h — Set/Get Logical Scanline Length

This function sets or gets the length of a logical scanline. This function allows an application to set up a logical video memory buffer that is wider than the displayed area. Function 07h then allows the application to set the starting position that is to be displayed.

Input:	AH =	4fh	Super VGA Support
	AL =	06h	Logical Scanline Length
	BL =	00h	Select Scanline Length
	CX =		Desired Width in Pixels
Output:	AX =		Status
	BX =		Bytes Per Scanline
	CX =		Actual Pixels Per Scanline
	DX =		Maximum Number of Scanlines
Input:	AH =	4fh	Super VGA Support
	AL =	06h	Logical Scanline Length
	BL =	01h	Return Scanline Length
Output:	AX =		Status
	BX =		Bytes Per Scanline
	CX =		Actual Pixels Per Scanline
	DX =		Maximum Number of Scanlines

NOTE: The desired width in pixels may not be achievable because of VGA hardware considerations. The next larger value will be selected that will accommodate the desired number of pixels, and the actual number of pixels will be returned in CX register. BX register returns a value that, when added to a pointer into video memory, will point to the next scanline. For example, in a mode 13h this would be 320, but in mode 12h this would be 80. DX register returns the number of logical scanlines based upon the new scanline length and the total memory installed and usable in this display mode. This function is also valid in text modes. In text modes, the application should determine the current character cell width through VESA Function 1 (or VGA BIOS Function 1BH), multiply that times the desired number of characters per line, and pass that value in the CX register.

4.4.9 Function 07h — Set/Get Display Start

This function selects the pixel to be displayed in the upper-left corner of the display from the logical page. This function can be used to pan and scroll around logical screens that are larger than the displayed screen. This function can also be used to rapidly switch between two different displayed screens for double-buffered animation effects.

Input:	AH =	4fh	Super VGA Support
	AL =	07h	Display Start Control
	BH =	00h	Reserved and must be a '0'
	BL =	00h	

	CX =		First Displayed Pixel In Scanline
	DX =		First Displayed Scanline
Output:	AX =	Status	
Input:	AH =	4fh	Super VGA Support
	AL =	07h	Display Start Control
	BL =	01h	Return Display Start
Output:	AX =		Status
	BH =		00h Reserved and will be a '0'
	CX =		First Displayed Pixel In Scanline
	DX =		First Displayed Scanline

NOTE: This function is also valid in text modes. In text modes, the application should find out the current character cell width through VESA Function 1 (or VGA BIOS Function 1BH), multiply that times the desired starting character column, and pass that value in the CX register. It should also multiply the current character cell height times the desired starting character row, and pass that value in the DX register.

4.4.10 Function 08h — Set/Get DAC Palette Control

This function queries and selects the operating mode of the DAC palette. Some DACs are configurable to provide 6 bits, 8 bits, or more of color definition per red, green, and blue primary color. The DAC palette width is assumed to be reset to standard VGA 6 bits per primary during a standard or VESA Set Super VGA mode (AX=4F02h) call.

Input:	AH=	4fh	Super VGA Support
	AL=	08h	Set/Get DAC Palette Control
	BL =	00h	Set DAC Palette Width
	BH=		Desired number of bits of color per primary (Standard VGA = 6)
Output:	AX=		Status
	BH=		Current number of bits of color per primary (Standard VGA = 6)
Input:	AH=	4fh	Super VGA Support
	AL=	08h	Set/Get DAC Palette Control
	BL =	01h	Get DAC Palette Width
Output:	AX=		Status
	BH=		Current number of bits of color per primary (Standard VGA = 6)

An application can determine if DAC switching is available by querying bit D0 of the Capabilities field of the VgaInfoBlock structure returned by VESA Return Super VGA Information (AX=4F00h). The application can then attempt to set the DAC palette width to the desired value. If the Super VGA is not capable of selecting the requested palette width, then the next lower value that the Super VGA is capable of selecting. The resulting palette width is returned.

4.4.11 Function 10h — Display Power Management Extensions

This function queries, selects, and returns the Power Management capabilities and states of the controller. An application can determine which states are available using the Query Function; it can select a state, and it can determine which state has been previously selected.

Input:
AH= 4fh Super VGA Support
AL= 10f VBE/PM Services
BL= 00h Report VBE/PM Capabilities
ES:DI= Null pointer, must be 0000:0000 in version 1.0

Output:
AX= Status
BH= Power saving state signals support by the controller:
1 = supported, 0 = not supported
bit 0 STAND BY
bit 1 SUSPEND
bit 2 OFF
bit 3 REDUCED ON (not supported by DPMS 1.0)
bit 4-7 reserved
BL= VBE/PM Version number
bits 7:4 Major Version number
bits 3:0 Minor Version number

Input:
AH= 4fh Super VGA Support
AL= 10h VBE/PM Services
BL= 01h Set Display Power State
BH= Requested Power State
00h ON
01h STAND BY
02h SUSPEND
04h OFF
08h REDUCED ON (not supported by DPMS 1.0)

Output:
AX= Status
BH= Unchanged

Input:
AH= 4fh Super VGA Support
AL= 10h VBE/PM Services
BL= 02h Get Display Power State

Output:
AX= Status
BH= Display Power State
00h ON
01h STAND BY
02h SUSPEND
04h OFF
08h REDUCED ON (not supported by DPMS 1.0)
bits 7:4 are reserved and
should be ignored to ensure upward compatability.

5. EXTENDED MODES IN RAM

5.1 Extensions to the Save Area Table

The Cirrus Logic BIOS (standard versions) supports VGA-compatible modes along with a set of extended modes. OEMs may add new modes to the system, or redefine existing modes that are in the VGA ROM by manipulating the BIOS Save Area Table pointed to by 0040:00A8. This table is located in ROM after the system is booted. Any changes must be made in a RAM copy. The Cirrus Logic BIOS has extended the definition of this table with 'negative' offsets that point to Cirrus Logic-BIOS-defined parameters. The compatible table, along with the defined extensions are listed in Table E1–4.

Table E1–4. Set Area Table and Extensions

Offset	Type	Description
-14h	DWORD	Ptr to next negative offset table in linked list
-10h	WORD	Set to 04h if offset -14h is valid ptr, set to 00h if this link is the last in RAM. To block all ROM-based modes, set this field to 04h, and offset -14 to 0:0
-0Eh	WORD	Size of supplemental table
-0Ch	DWORD	Ptr to extended mode supplemental parameters
-08h	DWORD	Ptr to extended mode standard parameters
-04h	WORD	Number of extended video modes
-02h	WORD	'RV' identifier
00h	DWORD	Pointer to standard mode standard parameters
04h	DWORD	Dynamic saver area pointer (palette save area)
08h	DWORD	Alpha mode auxiliary character generator ptr
0Ch	DWORD	Graphics mode auxiliary character generator ptr
10h	DWORD	Secondary save pointer
14h	DWORD	Reserved and set to a zero
18h	DWORD	Reserved and set to a zero

5.2 BIOS Processing

The Cirrus Logic BIOS will determine what mode to select by processing a linked list of extended mode supplemental parameters tables, while evaluating several factors such as memory size, monitor type, memory clock, and the chipset that it is running on. Traveling from the top down, the BIOS will service a mode set request once all factors have been satisfied. A mode that has multiple horizontal frequencies must be sequentially ordered from the highest frequency at the top to the lowest on the bottom. This ensures that the BIOS will always set the correct mode for the given monitor type.

Modes can be added to the BIOS by manipulating the structure described above. The BIOS will always search for the RAM-defined links first to satisfy a mode set request. If it cannot find a mode based on the current configuration of the video subsystem, the ROM tables will then be scanned.

If new modes are to be added to the BIOS by defining them in RAM, a TSR need only modify the negative offsets described above (i.e., higher refreshes of previously defined modes, or entirely new mode numbers). If modes are to be redefined, special care must be taken. If a TSR modifies a particular frequency of a mode that has higher frequencies already defined in ROM, all frequencies must be redefined in RAM.

5.3 Extended Mode Supplemental Parameters

Table E1–5 describes what the BIOS expects in the supplemental structure discussed above.

Table E1–5. Supplemental Parameters

Offset	Size	Description
00	Byte	Video mode number
01	Word	VESA video mode number
03	Word	Horizontal resolution
05	Word	Vertical resolution
07	Byte	Bits per color
08	Byte	Character width
09	Byte	Character height
0A	Byte	VESA memory model (defined in VESA Function 1)
0B	Byte	VESA mode attributes (defined in VESA Function 1)
0C	Byte	Reserved (00)
0D	Byte	Reserved (00)
0E	Byte	What chipsets mode is allowed on (bit location based on return value in AL of alternate Function 80h)
0F	Byte	Memory required, in 64K blocks
10	Byte	Bit mask of supported monitors (montype)
11	Byte	SR07, Extd Sequ Ctrl
12	Byte	SR0F, DRAM Ctrl
13	Byte	SR0E, VCLK3 numerator
14	Byte	SR1E, VCLK3 denominator
15	Byte	GR0B, Grfx Extensions

Table E1–5. Supplemental Parameters *(cont.)*

Offset	Size	Description
16	Byte	CR19, Interlace end
17	Byte	CR1A, Misc Ctrl
18	Byte	CR1B, Display Ctrl
19	Byte	DACEXT, Hidden DAC register

Appendix F1

Glossary

Glossary

Add-in Card, Adapter Card: A circuit board that plugs into a computer motherboard and connects it to some external device, such as a video monitor or storage subsystem.

A.N.: An acronym for Alpha Numeric. Only those patterns defined in the font tables can be displayed. Information can usually be displayed more quickly than is the case with APA images because fewer bits need to be manipulated by the software.

A.P.A.: An acronym for All Points Addressable. Each pixel on the screen is individually programmable. Any pattern (subject to the resolution of the system) can be displayed. This typically requires that one to two orders of magnitude more information be manipulated than is the case with an A.N. system.

Analog Interface: An interface between a video controller and a video display in which pixel colors are determined by the voltage levels on three output lines (RGB). A theoretically unlimited number of colors can be supported by this method (the maximum number anyone talks about is 16,777,216). The voltage level on any line varies between zero volts (for black) to about 700 millivolts (for maximum brightness). The lines are typically terminated in 75 ohms at the monitor end and 150 ohms at the graphics controller end. In the IBM world, the analog interface is usually mechanized with a 15-pin, 3-row connector.

Analog Monitor: A video monitor that uses an analog interface. In IBM terms, commonly known as a PS/2 monitor, or a VGA monitor when used in conjunction with a VGA controller. Most modern analog monitors have a switch allowing them to be used as a digital monitor.

Analog: A signal that can assume intermediate levels between on and off. Contrast with **Digital**.

ASCII: American Standard Code for Information Interchange. This is a 7-bit code used to encode alphanumeric information. In the IBM-compatible world, this is expanded to eight bits to encode a total of 256 alphanumeric and control characters.

AUTOEXEC.BAT: A file used to direct a series of activities that occur during system boot-up.

Auto-Monitor Detect: A feature of Cirrus Logic VGA controllers and BIOS that senses the type of monitor that is connected. This uses a scheme that involves the use of comparators to sense the terminations present on the RGB lines.

BIOS-Level Compatibility: With regard to a VGA subsystem, this means that the BIOS supplied is in compliance with the IBM VGA standard. This is the minimum level of compatibility necessary to accommodate the majority of standard applications.

BIOS: An acronym for Basic Input Output System. In IBM-compatible personal computers, this is a set of ROM-based firmware routines that control the resources of the system and make them available to application programs in an orderly manner. These routines provide basic input/output services for the operating system and for applications programs that use interrupts to call them. Also called ROM BIOS.

Bit: Binary Digit. A single piece of information, on or off, 0 or 1, high or low, closed or open, up or down, in or out, alive or dead, black or white.

BitBLT: An acronym for Bit Boundary Block Transfer. A type of graphics drawing routine that moves a rectangle of data from one area of display memory to another. The data specifically need not have any particular alignment. Graphics controllers frequently include varying degrees of hardware to help speed BitBLT operations. The original destination is one of the source operands.

Bitmap: A rectangular array of locations, each of which is associated with a location (pixel) on a monitor. The contents of each location determines the color of the pixel. Often times there are more locations in the bitmap than on the screen, allowing images to be maintained for later presentation.

Block Diagram: A diagram in which blocks are used to represent components or subsystems of a system. Usually the blocks are connected with lines indicating data or control flow.

Byte: A group of eight bits addressed as a unit. Can take any of 256 (2^8) values.

CAS: Column Address Strobe. One of the DRAM control signals.

CGA, Color Graphics Adapter: This was the first color adapter available for the IBM personal computer. It has lower resolution, both spatial and color. While CGA is generally considered obsolete, the VGA standard includes the video modes originally designed for CGA.

Character Cell Matrix: In Text Mode, the area of display used to display one character. On VGA, character cells are either 8, 9, 12, or 16 pixels wide and usually are either 8, 14, or 16 pixels high.

Character Clock: This clock is generated by dividing the VCLK. The Monitor Timing Signals (HSYNC, VSYNC) are derived by dividing the character clock.

Color Key: The CL-GD5422, CL-GD5424, CL-GD5426, CL-GD5428, and CL-GD5429 have the capability of overlaying the computer-generated video, on a pixel-by-pixel basis, with external video. One method of determining whether to overlay a pixel involves comparing it with a specific color.

Color Lookup Table (CLUT): Translates color information from the display memory into color information for the CRT display. It may be found in a Video DAC.

Color Modes: Uses two, four, eight, or sixteen bits per pixel. The following table summarizes the number of colors and the standards for which the colors were first available.

Table F1–1. Color Modes

Bits per Pixel	Number of Colors	Standards
2	4	CGA/EGA
4	16	CGA/EGA/VGA
8	256	VGA
15	32,368	TARGA™
16	65,536	VGA/XGA™
24	16,777,216	Cirrus Logic True Color

Color Planes: In planar modes, the display memory is separated into four independent planes of memory, with each plane dedicated to controlling one color component (Red, Green, Blue, and Intensify). Each pixel of the display occupies one bit position in each plane. In character modes and packed pixel modes, the data is organized differently.

CONFIG.SYS: A file that provides the system with information regarding application requirements. This information may include peripherals that are connected and require special drivers (such as a mouse). Other information that might be specified is the number of files that may be open simultaneously, or the number of disk drives that may be accessed.

CMOS: Complementary Metal Oxide Semiconductor. A digital logic family that is characterized by high density, low-to-medium power, and medium-to-high speeds. All modern VGA controllers are fabricated using CMOS.

CRT, Cathode Ray Tube: An electron beam is generated, accelerated, and made to strike a phosphor coating on the inside of an evacuated glass enclosure. The phosphor glows as a result of the energy imparted by the beam. By precisely controlling the position and intensity of the electron beam, meaningful patterns are made to appear in the phosphor and are visible through the glass.

DCLK: The package pin on which the pixel clock is present. See also VCLK.

Digital Interface: A type of interface used between video controller and video display in which display color is controlled by digital color control lines switching on and off. The number of colors that can be supported depends on the number of signal lines in the interface, and is generally either 8, 16, or 64. Most digital interfaces are TTL (Transistor-Transistor Logic)-compatible. CGA, MDA, and EGA use digital interfaces. In the IBM world, the digital interface is usually mechanized with a 9-pin connector.

Digital Monitor (TTL): A monitor that receives its input in the form of a digital code. Typical digital monitors can display 8, 16, or 64 colors.

Digital: A method of representing data whereby the individual components are either fully on or fully off.

Digitize: To convert an analog image or signal to a corresponding series of numbers.

Display Memory: The area in the computer memory where the information used to update the screen is kept. In the IBM-compatible world, the range of addresses for this data is A000:0 through BFFF:F.

Display Modes: In the IBM-compatible world, a number of standard display modes have been defined. The standard modes for MDA, CGA, EGA, and VGA are enumerated in the table below.

Table F1–2. Display Modes

Mode(s)	Colors	Alphanumeric Resolution	Pixel Resolution	A.N./ A.P.A
0,1	16	40 x 25	360 x 400	A.N.
2,3	16	80 x 25	720 x 400	A.N.
4,5	4	40 x25	320 x 200	A.P.A.
6	2	80 x 25	640 x 200	A.P.A.
7	Mono.	80 x 25	720 x 400	A.N.
D	16	40 x 25	320 x 200	A.P.A.
E	16	80 x 25	640 x 200	A.P.A.
F	Mono.	80 x 25	640 x 250	A.P.A.
10	16	80 x 25	640 x 350	A.P.A.
11	2	80 x 30	640 x 480	A.P.A.
12	16	80 x 30	640 x 480	A.P.A.
13	256	40 x 25	320 x 200	A.P.A.

Dithering: To intersperse a pattern of one color (for example, blue) with a pattern of another color (for example, red) to give the subjective effect of a color somewhere between the two colors (blue and red together make magenta). This technique is effective over large surfaces but fails if the area is too small. This technique creates more colors at the expense of resolution.

DIP: Dual Inline Package. A method of packaging semiconductor chips that was essentially ubiquitous until the 1980s. It is being replaced with plastic quad flatpack and pin grid arrays for devices with high pin counts and small outline packages for devices with low or medium pin counts.

DRAM: Dynamic Random Access Memory. A memory technology that is characterized by extremely high density, low power, and low cost. It must be more or less continuously refreshed to avoid loss of data.

Driver: A software module that interfaces a particular display device to an application program to allow operation at higher resolutions than standard VGA.

EEPROM, Electronically Erasable Programmable Read-only Memory: A memory storage device that can be written repeatedly with no special erasure fixture. EEPROMs do not lose their contents when they are powered down. The Cirrus Logic, Inc. BIOS can use EEPROMs to record information regarding the connected monitor.

EGA: Enhanced Graphics Adapter. This was the second color adapter available for IBM-compatible computers. While EGA is generally considered obsolete, the VGA standard includes the modes originally designed for EGA.

Emulation: Simulation of unavailable hardware by available hardware and software. Emulations improve the usefulness of a product by making it compatible with other products. EGA is capable of emulating MDA and sometimes CGA and Hercules. VGA is capable of emulating EGA, CGA, and MDA.

EPROM: Electrically Programmable Read-only Memory: A memory storage device that can be written once (per erasure cycle) and read many times. In the VGA world, it is used for holding the BIOS.

Fast-Page Mode: A read or write mode of DRAMs that is characterized by a decrease in cycle time of about 2-3 and a corresponding increase in performance. The data accessed in Fast-Page Mode cycles must be adjacent in memory.

Feature Connector: An expansion connector on the VGA that can be used to accept or drive video signals to or from the VGA. This is used in applications involving video overlay.

FIFO: First In First Out. A memory that can temporarily hold data so that the sending device can send data faster than the receiving device can accept it. The sending and receiving devices typically operate asynchronously.

Fixed-Frequency Monitor: A monitor that can accept a fixed-horizontal frequency, usually 31.5 kHz. Such monitors can accommodate different vertical resolutions by operating at different vertical frequencies, usually either 60 or 70 Hz.

Frequency Synthesizer: An electronic circuit that can generate a number of frequencies from a fixed-reference frequency. Some frequency synthesizers can generate only a relatively small number of frequencies; others can generate hundreds of different frequencies.

Glue Logic: Additional logic devices (typically SSI) required to interconnect the major components of a system.

Graphics Controller: On EGA and VGA, a section of circuitry that can provide hardware assist for graphics drawing algorithms by performing logical functions on data written to display memory.

Graphics Mode: (Also A.P.A.) A display mode in which all pixels on the display screen can be controlled independently to draw graphics objects (as opposed to Text mode, in which only a pre-defined set of characters can be displayed).

HERC, Hercules® Graphics Adapter (HGC): The third display format standardized for the PC family of computers, following the MDA and CGA. It provides standard 80-character-by-25-row alphanumeric display, and 720 horizontal by 348 vertical pixels in Monochrome Graphics mode. It was designed as a replacement for MDA, and provided monochrome A.P.A.

Hex Code, Hexadecimal: A numbering system using base 16. The allowable digits are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, and F. A base 16 numbering system is useful because conversion to and from base 2 is trivial. Numbers written in base 16 are typically denoted by a prepended '0x' or an appended 'h'.

Interlaced: An graphics system in which the even scanlines are refreshed in one vertical cycle (field), and the odd scanlines are refreshed in another vertical cycle. The advantage is that the video bandwidth is roughly half that required for a non-interlaced system of the same resolution. This results in less costly hardware. The disadvantage of an interlaced system is flicker, especially when displaying objects that are only a few scanline high.

ISA: Industry Standard Architecture. In reference to IBM-compatible computers, it is the definition of the standard bus.

Mapping: Mapping refers to the definition of memory for storing data used by a particular Video Mode. The range of addresses reserved for video information in IBM-compatible systems is from A000:0 to BFFF:F.

MCGA, Multicolor Graphics Array: A graphics adapter designed for the PS/2 series of personal computers, with similar function to the CGA and downwardly compatible to the CGA at the BIOS, control register, and display memory levels. Like the VGA, the MCGA drives either an analog monochrome or analog RGB monitor.

MDA, Monochrome Display Adapter: The original display adapter marketed by IBM for personal computers. MDA has no bit-mapped graphics capability.

MicroChannel Bus: The IBM-designed replacement for ISA bus. This bus is found in all but the lowest-end PS/2 models.

Monitor: Another term for a CRT Display.

Monochrome Modes: Uses one bit per pixel. 'Two-color' modes are similar to monochrome modes because they can display two colors; the two colors do not need to be black and white, sometimes they are amber or green with black.

Motherboard: The large printed circuit board in a personal computer into which the adapter boards plug. It contains the CPU and core memory. It may also contain the video controller or a number of other peripherals.

Multiple-FIFO Architecture: A video controller architecture that is characterized by having multiple (two) FIFOs or Write Buffers. There is typically one FIFO or Write Buffer at the CPU interface and one FIFO in the screen refresh stream.

Multifrequency Monitor: A monitor that will accommodate a variety of horizontal and vertical synchronization frequencies. This type of monitor accepts inputs from many different video display adapters, and is typically capable of either analog or digital input.

Nibble: A group of four bits, typically contiguous. Can take any of 16 (2^4) values.

Non-interlaced: A video system in which every pixel is refreshed during every vertical scan. A non-interlaced system is normally more expensive than an interlaced system of the same resolution, but is usually said to have a more pleasing appearance.

Overlay: The superimposition of video (typically live) onto computer generated graphics.

Overscan: That portion on all four sides of the raster between active video and blanking.

Packed Pixel: Color information for a pixel packed into one word of memory data. For a system with few colors, this packed pixel may require only a part of one word of memory; for very elaborate systems, a packed pixel might be several words long. See **Planar**.

Palette: The range of colors available on the screen, not necessarily simultaneously. For VGA, this is either 16 simultaneous colors out of 262,144 or 256 simultaneous colors out of 262,144. For CL-GD542X, the palette is extended to 32,768, 65,536, or 16,777,216 simultaneous color on the screen.

Palette DAC: The triple eight-bit DAC with its associated lookup table.

PGA, Professional Graphics Adapter: The next step up from the EGA in resolution, speed, depth, performance, and cost. The graphics resolution is 640 by 480 with 256 simultaneous colors. It has an on-board processor to provide high-level graphics functions, such as two- and three-dimensional graphics, windowing, clipping, viewing transformations, modeling transformations without relying on the host PC processor.

Pixel: An acronym for picture element, and is also called a pel. A pixel is the smallest addressable graphic on a display screen. In RGB systems, the color of a pixel is defined by some Red intensity, some Green intensity, and some Blue intensity.

Planar: In video terms, the pixel color information is stored in four bits across four memory planes. This allows a maximum of 16 colors (2^4). See **Packed Pixel**.

RAM, Random Access Memory: This term has come to mean any semiconductor memory whose write access time is approximately the same as its read access time. This is typically taken to include SRAMs (Static RAMs) and DRAMs (Dynamic RAMs). This definition specifically eliminates memories that cannot be altered at all and memories that require a special fixture for erasing (such as EPROMs).

RAM BIOS: The BIOS can be copied from relatively slow ROM into relatively fast RAM. When this is done, it will execute faster, enhancing performance of the subsystem being controlled.

RAS: Row Address Strobe. A DRAM control signal.

Refresh (Display or Screen Refresh): An image drawn on a CRT display will remain visible only for a few milliseconds (the persistence of the screen phosphor), unless it is redrawn continuously. This process is called display refresh or screen refresh. Different displays use different refresh rates, but display refresh is normally required between 50 and 70 times a second to avoid any visible screen flickering. Sixty times a second is a common refresh rate. In general, a higher refresh rate results in more stable appearing display.

Register-Level Compatibility: If a peripheral is compatible at the register level with another peripheral, it means that every bit in every register has precisely the same meaning. This implies that application programs can circumvent the BIOS and directly program registers in a peripheral device without functionality problems. The CL-GD542X is register-level-compatible with the IBM VGA standard.

Registers: In a VGA controller, these are the storage elements that contain data relating to the mode or configuration of the device, as opposed to the Display Memory that contains the image. Traditionally, the registers are divided into six groups: General, Sequencer, CRT Controller, Graphics Controllers, Attribute, and Expansion. The VGA registers are accessed by a number of addressing schemes, each involving an index or address register and a data register.

Resolution, Color: The number of simultaneous colors is determined by the number of bits associated with each pixel in the display memory. The more colors, the more bits. If n bits per pixel are used, 2^n color combinations can be generated. EGA uses from one to four bits per pixel, permitting up to 16 (2^4) colors to be displayed on the screen at the same time. The VGA has an added mode that supports eight bits per pixel, or 256 (2^8) simultaneous colors. The CL-GD542X has additional modes that support up to 24 bits per pixel or 16,777,216 (2^{24}) simultaneous colors.

Resolution, Spatial: The number of pixels in an area or on the screen. Resolution is typically specified as pixels per scanline and scanlines per frame. Higher resolution images require more processing and greater storage requirements per image. In addition, monitor cost increases with resolution, particularly above about one million pixels. Different applications require different resolutions.

RGB: Used with color displays, an interface that uses three color signals (Red, Green, and Blue), as opposed to an interface used with a monochrome display that requires only a single signal. Both digital and analog RGB interfaces exist.

ROM, Read-only Memory: A type of memory that is characterized by not being alterable (but see EPROM). ROMs are typically used to contain low-level programs that do not change, such as BIOS.

Simultaneous Colors: The number of colors in a display system that can be displayed on the screen at one time. This number is limited by the circuitry of the display adapter, and is usually much smaller than the number of colors the display device can actually support. The number of simultaneous colors a display adapter will support is normally determined by the number of color planes, or bits per pixel, that it uses. For example, a device with four bits per pixel will support 16 simultaneous colors.

Sleep Mode: A VGA controller can be put to 'sleep' by writing a value to a particular bit of a particular register. The register is normally at address 3C3 or 46E8 in the IBM-compatible world. When a VGA controller is asleep, it will respond to no further commands except a command to wake up or a BIOS read. This allows two VGA controllers to share common addresses, so long as their sleep addresses and BIOS addresses are not the same.

Software: A computing system is normally spoken of as having two major components: hardware and software. Software is that portion that instructs the hardware in the step-by-step procedure necessary to perform a particular task.

Super VGA: Graphics adapters that extend the capabilities of the features provided by the original IBM VGA. The first Super VGA provided a 640 x 480 x 256-Color Mode.

Surface Mount Technology (SMT): A method of mounting devices (such as integrated circuits, resistors, capacitors, and others) on printed circuit boards that is characterized by not requiring mounting holes. Rather, the devices are soldered to pads on the printed wires board. Surface-mount devices are typically smaller than the equivalent through-hole device.

TTL, Transistor-Transistor Logic: A collection of logic families developed beginning in the 1960s. TTL is gradually being replaced with CMOS for all, but the fastest or most cost-sensitive applications.

True Color: 24-bit-per-pixel color providing photo-realistic image quality.

VCLK: The internal signal operating at the pixel rate.

Vertical Retrace: The time interval immediately following the completion of a complete frame (or field for an interlaced display). The electron beam returns to the top of the display screen in preparation for the next frame or field during this period.

VESA, Video Electronics Standards Association: A consortium of CRT monitor vendors, graphics chip vendors, and graphics software vendors that set hardware and software standards for PC-compatible graphics monitors and software interfaces.

VGA, Video Graphics Array: The VGA standard was introduced by IBM in 1987. In the IBM definition, the maximum spatial resolution is 640 x 480 (Modes 11 and 12), and the maximum color resolution is 256 colors (Mode 13). This has been enhanced or extended by third party chip vendors to up to 1280 x 1024 and up to 16,777,216 colors.

VLSI, Very Large Scale Integration: The technology of manufacturing integrated circuits (chips) with thousands of transistors on a single device. The personal computer was made possible because of VLSI technology.

VRAM, Video (Dynamic) Random Access Memory: Memory chips with two ports, one used for random accesses and the other capable of serial accesses. Once the serial port has been initialized (with a transfer cycle) it can operate independently of the random port. This frees the random port for CPU accesses. The result of adding the serial port is a significantly reduced amount of interference from screen refresh. VRAMs cost more per bit than DRAMs.

Wait State: When a system processor is reading or writing a memory or peripheral device that cannot respond fast enough, one or more time intervals (typically on the order of hundreds of nanoseconds each) are inserted during which the processor does nothing but wait for the slower device. While this has a detrimental effect on system throughput, it is unavoidable. The number of wait states can be reduced using techniques such as CPU-bus caches or write FIFOs.

Word: The amount of memory that a given computer can access in a single cycle. In the IBM-compatible world, this is either 16 or 32 bits.

Write Buffer: A term used in the CL-GD542X literature to denote the buffer that is logically positioned between the CPU interface and the display memory.

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Index

Index

C

D

E

G

H

R

S

T

W–Z

Notes

Notes

Notes

Notes

Notes

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2	STX	DC2	"	2	B	R	b	r
3	ETX	DC3	#	3	C	S	c	s
4	EOT	DC4	$	4	D	T	d	t
5	ENQ	NAK	%	5	E	U	e	u
6	ACK	SYN	&	6	F	V	f	v
7	BEL	ETB	`	7	G	W	g	w
8	BS	CAN	(	8	H	X	h	x
9	HT	EM	)	9	I	Y	i	y
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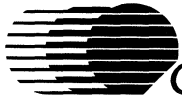

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