CRYSTAL
SEMICONDUCTOR CORPORATION

DATA BOOK

Crystal Semiconductor was founded to bring the benefits of leadership, high quality, analog VLSI solutions to our customers.

Crystal Semiconductor Corporation

Data Book

LIFE SUPPORT AND NUCLEAR POLICY

CRYSTAL SEMICONDUCTOR PRODUCTS ARE NOT AUTHORIZED FOR AND SHOULD NOT BE USED WITHIN LIFE SUPPORT SYSTEMS OR NUCLEAR FACILITY APPLICATIONS WITHOUT THE SPECIFIC WRITTEN CONSENT OF CRYSTAL SEMICONDUCTOR.

Life Support Systems are equipment intended to support or sustain life and whose failure to perform when properly used in accordance with instructions provided can be reasonably expected to result in personal injury or death. Users contemplating applications of Crystal Semiconductor products in Life Support Systems are requested to contact Crystal Semiconductor factory headquarters to establish suitable terms and conditions for these applications. Crystal Semiconductor's warranty is limited to replacement of defective components and does not cover injury to persons or property or other consequential damages.

Examples of devices considered to be life support devices are neonatal oxygen analyzers, nerve stimulators (whether used for anesthesia, pain relief, or other purposes), autotransfusion devices, blood pumps, defibrillators, arrhythmia detectors and alarms, pacemakers, hemodialysis systems, peritoneal dialysis systems, neonatal ventilator incubators, ventilators for both adults and infants, anesthesia ventilators, and infusion pumps, as well as other devices designated as "critical" by the FDA. The above are examples only and are not intended to be conclusive or exclusive of any other life support device.

Examples of nuclear facility applications are applications in (a) a nuclear reactor, or (b) any device designed or used in connection with the handling, processing, packaging, preparation, utilization, fabricating, alloying, storing, or disposal of fissionable material or waste products thereof.

• Notes •

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COMPANY INFORMATION

Crystal's proprietary SMART Analog™ design technique, incorporating analog and digital circuitry in monolithic CMOS devices, represents a powerful new technology in the semiconductor industry. This innovative approach to design eliminates many of the sources of inconsistent performance in traditional analog circuitry.

Maximum system performance is built-in from initial research on end-user requirements through product definition. Product quality and reliability is designed into the device architecture and is further assured through rigorous standards for fabrication, assembly and testing. Crystal's part numbering scheme is as follows:

CSLXXXX - TPNNH/R

DEVICE REVISION: DOES NOT APPEAR HERE ON PACKAGE MARK.
REVISION IS COVERED IN DATE CODE STAMP.
USED ONLY FOR ORDERING/TRACKING.

SPECIAL HANDLING ,ALPHA CHARACTER ONLY

ELECTRICAL OR SPEED SPECIFICATION. (OPTIONAL) UP TO 2 NUMERIC DIGITS. NO ALPHA CHARACTERS. SEE DATA SHEET

PACKAGE CODE -REQUIRED ,ALPHA CHARACTER ONLY,NO NUMERICS

P = PLASTIC DIP	S = 0.3" SOIC
C = CERAMIC SIDEBRAZE	W = 0.6" SOIC
D = CERDIP	E= CERAMIC LCC
L = PLASTIC LEADED CHIP CARRIER,J LEAD	
U= UNPACKAGED DIE	

TEMPERATURE SPECIFICATION - REQUIRED,ALPHA CHARACTER ONLY
SIGNAL CONDITIONING/COMMUNICATION:
BLANK = 0°C to 70°C
I = - 40°C to 85°C
M = - 55°C to 125°C

TEMPERATURE/ACCURACY - REQUIRED,ALPHA CHARACTER ONLY
DATA ACQUISITION:

TEMPERATURE	ACCURACY		
	GOOD	BETTER	BEST
0°C to 70°C	J	K	L
-40°C to 85°C	A	B	C
-55°C to 125 °C	S	T	U

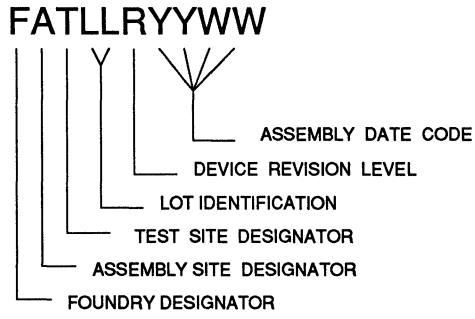
FOUR ALPHANUMERIC DIGITS COMPRISE REMAINDER OF BASIC PART NUMBER

CRYSTAL PRODUCT LINE (PROPRIETARY PARTS; SECOND-SOURCE PARTS HAVE EXCEPTIONS):
3 = DATA ACQ. SUPPORT CIRCUITS
5 = A/D CONVERTERS
6 = TELECOMMUNICATIONS
7 = SIGNAL CONDITIONING
8 = DATACOMMUNICATIONS

CRYSTAL SEMICONDUCTOR
"CS" = ALL CRYSTAL PRODUCTS;EXCEPT FOR
"CSZ" = S - TO - Z A/D CONVERTERS

REV2

In addition to the part number, all Crystal parts have a second line of marking, which can be decoded as follows:



LOT CODE IDENTIFIER - TWO DIGIT ALPHA CHARACTER. IDENTIFIER SEQUENCE WILL BEGIN WITH AA,AB,AC, ETC. EACH LOT WILL RECEIVE A UNIQUE IDENTIFIER REGARDLESS OF DEVICE OR START DATE. SEQUENCE BEGINS AGAIN WITH AA WHEN ZZ HAS BEEN UTILIZED.

COMPANY BACKGROUND

Crystal Semiconductor Corporation was founded in 1984 with the goal of supplying the industry with high-performance, mixed analog/digital CMOS circuits.

To meet its objectives, Crystal recruited a staff of renowned CMOS analog design engineers, a scarce resource in the industry, and teamed them with designers trained in system architecture development.

By coupling this design staff with highly qualified application and test engineers and seasoned management, Crystal has achieved several industry firsts. Systems designers now benefit from the performance and cost savings of Crystal breakthroughs such as self-calibrating ADCs, a universal filter, monolithic T1 interfaces and the industry's first implementations of "delta sigma" oversampling A-to-D converters.

Headquartered in Austin, Texas, Crystal sells its products worldwide through a network of manufacturer's representatives. Crystal's entire marketing and sales organization is committed to providing quality products and reliable, rapid service.

QUALITY AND RELIABILITY INFORMATION

Crystal Semiconductor is committed at every level of the company to the highest possible standards of quality and reliability in its products. This committment is evident in all phases of operations: initial product definition, design, fabrication, assembly, test, qualification and customer service. Product quality and reliability is an active concern of each Crystal employee.

In Product Definition

To ensure maximum system performance, Crystal works with users to identify and quantify the parameters, including quality and reliability issues, that best serve customer needs. Quality and reliability become part of the design goals, along with electrical performance and cost.

In Design

Conservative 3-micron CMOS design rules are the basis for all current Crystal products. In addition, extensive use is made of proven standard cells to drastically reduce the possibility of design errors.

Each pin in every SMART Analog product is designed to meet ESD levels of at least 2500V when tested per MIL STD 883C, Method 3015. Each pin is also designed to withstand more than 200mA of DC latch current.

Crystal SMART Analog design architectures provide quality and reliability comparable to leading digital devices and memories. This is far superior to traditional analog ICs and hybrids. On-chip digital error correction provides stable performance over time and temperature by taking advantage of digital controls that are insensitive to parametric analog problems such as leakages and shifts in threshold voltage. Using Crystal devices, designers have fewer error sources to consider. The result is a less complicated, more reliable system.

In Fabrication and Assembly

Crystal ensures reliable delivery of quality parts by accessing established foundries in multiple locations (Japan, Canada and California today). Each fabrication facility is qualified by Crystal. Assembly is performed both domestically and offshore under carefully documented and well-controlled conditions.

Wafer fabrication and assembly processes undergo in-line quality inspections. Wafers are inspected optically to guidelines based on MIL STD 883C, Method 2010. Each die is electrically tested using proprietary test circuits that verify key parameters. Following assembly, packages are subjected to a variety of mechanical inspections to verify integrity and insure high quality. (For example, x-ray inspection to 3.0 percent LTPD is one of the standard production tests.)

In Test

In a break from traditional analog components, Crystal's SMART Analog products include basic test capabilities designed into each chip. Crystal's in-process quality assurance program uses this designed-in testability to monitor and track the performance and quality of these complex circuits. Finished packaged components are tested 100 percent electrically, over temperature where critical parameters are involved. With these extensive quality programs, Crystal guarantees outgoing electrical quality levels on all data sheet specifications to a 0.065 percent AQL level over the full specified temperature range.

Throughout the assembly and test phases, traceability to the original wafer lot is carefully maintained.

In Product Qualification

Before any Crystal product is released to production and shipped in volume, it must undergo a thorough qualification program. Crystal has separate qualification criteria to address both long-term reliability and infant mortality so that the sources of failure are identified and eliminated. Crystal uses military specifications as the guidelines for reliability tests, methods and procedures. (See Table 1.)

To ensure reliability of the design and processes, full qualification requires that three non-consecutive lots are used during the qualification program. Fabrication and assembly facilities are audited quarterly and periodically requalified. Any design or process changes restart the qualification procedure.

These steps guarantee that Crystal products maintain the high standards of reliability designed-in from the start.

TABLE 1 - QUALIFICATION TESTS

TEST/CONDITION	MIL STD 883C METHOD	INFANT MORTALITY TESTS		LONG-TERM RELIABILITY TESTS		
		DURATION	PASS/FAIL CRITERION	DURATION	PASS/FAIL CRITERION	CRYSTAL GOAL
OPERATING LIFE +125 C, Dynamic Bias +/-5.5V Supplies NOTE 3	1015 COND D	168 HRS	0.7%	1000 HRS	700 FITS (70 C/60% UPPER CONFIDENCE LEVEL)	100 FITS (70 c/ 60% UCL)
TEMPERATURE HUMIDITY BIAS NOTE 1 +85 C/85% RH Static Bias	N/A	168 HRS	1.0 %	1000 HRS	3.0 %	1.0 %
TEMPERATURE CYCLING -65 C to +150 C Then Gross Leak Test	1010.5 COND C	100 CYCLES	1.0 %	1000 CYCLES	3.0 %	1.0 %
THERMAL SHOCK -55 C to +125 C Then Gross Leak Test	1011.4 COND B	100 CYCLES	1.0 %	500 CYCLES	3.0 %	1.0 %
STORAGE LIFE +150 C, No Bias	1008 COND C	168 HRS	1.0 %	1000 HRS	3.0 %	1.0%
AUTOCLAVE NOTE 1 & 2 +121 C/100% RH 2 Atmosphere, No Bias	N/A	48 HRS	1.0 %	144 HRS	3.0 %	1.0 %
CENTRIFUGE 30 Kg/y1 Axis	2001.2	--	--	--	5.0 %	1.0 %
ELECTROSTATIC DISCHARGE	3015.1	--	2500V	5 UNITS, ALL PINS	0 FAIL	4000V
LATCH UP DC Current	N/A	--	100 mA	5 UNITS, ALL PINS	0 FAIL	200mA
MARKING PERMANENCY NOTE 2	N/A	--	--	--	--	3.0 %
SOLDERABILITY	2003.3	--	--	--	--	1.0 %

NOTE 1 - This test applies only to plastic devices, which are non-hermetic.
NOTE 2 - This test is optional if the assembly site has been previously qualified.
NOTE 3 - 1 FIT (Failure In Time) = 1 Failure per Billion device hours.
NOTE 4 - UCL = Upper Confidence Level.
NOTE 5 - Temperature Humidity Bias, Temperature Cycling, Thermal Shock, Storage Life, and Autoclave Pass Criteria and goals are based upon a statistical 90% Upper Confidence Level.
NOTE 6 - Qualification Material is sourced from three non-consecutive manufacturing lots.

In Customer Service

Compliance with purchasing requirements is ensured through the use of Crystal's computerized system "Compass"(Crystal On-line Marketing Production and Sales System). This processing system ensures that all orders are entered correctly, scheduled properly, produced according to schedule, and shipped with zero discrepancies.

All systems and procedures at Crystal Semiconductor are aimed at continously improving the quality and reliability of our products and services to meet the needs of our customers.

Crystal's philosophy on quality is to anticipate problems and develop systems and controls to alleviate possible problems. It is a well stated fact by Juran and Deming, two of the nation's foremost experts on quality, that 85% of all quality problems are system related and 15% are worker related. Therefore, Crystal devotes its major quality efforts toward preventing system related quality problems.

Crystal has a very aggressive audit program in place. Monthly internal audits are performed to insure compliance to the extensive documentation of instructions and criteria for testing and inspection. Semiannual vendor audits are performed on the assembly and fabrication foundries. Vendor audits insure the adequacy and compliance of specifications, product flow, training, process controls and cleanliness. All internal and external audits have provisions for ratings and a system for corrective action requirements. These frequent audits by assembly, fabrication and quality engineers maximize system quality compliance.

As an added measure of continued high quality from assembly and fabrication foundries, thorough incoming inspections are performed. Wafer level optical inspection is based upon guidelines of MIL STD 883C, METHOD 2010. Test die are electrically tested to verify compliance to key process parameters based upon design rules specifications. These electrical parameters include threshold voltages, breakdown voltages, material resistance, and contact resistance. Assembly packaging inspection includes external visual, marking permanency, solderability, x-ray, hermeticity, die shear, wirepull and internal visual.

Preventive measures are very much in force in the final test area. Equipment calibration and preventive maintenance procedures are strictly adhered to. Handling procedures for Electrostatic Discharge are in place throughout the test areas. Non-conforming material is segregated until corrective action is agreed upon. There are controlled procedures for releasing new test programs and new test equipment to the production environment. In summary, Crystal Semiconductor is committed to meet the quality requirements of its customers.

MILITARY AND DIE SALES INFORMATION

The SMART Analog™ technology of Crystal Semiconductor offers unique advantages for high performance analog-to-digital conversion in military applications and as die to be incorporated into hybrid microcircuit devices.

SMART Analog ADC architectures achieve their accuracy through the inclusion of digital logic on-chip to ensure performance specifications. Self-calibrating ADCs, one family of circuits, incorporate a digital microcontroller to correct for linearity as well as gain and offset errors. Delta-sigma oversampling ADCs, another family, sample the signal substantially faster than the system sampling rate and then digitally filter average many actual samples to obtain a highly accurate output at the system rate.

Both self-calibration and oversampling architectures therefore achieve three benefits that are crucial to military and hybrid programs:

- Analog performance of the device is governed by digital functionality which is easily tested during the die manufacturing process at waferprobe. SMART Analog devices all include digital self-test modes to further enhance this thorough testability.

- Analog performance is immune to the factors which cause traditional ADCs to drift. The digital logic implements a closed loop feedback system which continually compensates for drift mechanisms while the part is operational. SMART Analog devices therefore retain the full rated accuracy over time and over temperature.

- CMOS processing used in Crystal ADCs is an industry-proven process which results in very low power consumption and highly reliable, easy to manufacture products.

MILITARY STANDARD PROCESSING

Crystal Semiconductor is committed to supplying product to the military marketplace as a major long-term focus of our business.

All devices are designed to meet the extended temperature ranges required for military applications. The wafer fabrication and device assembly facilities used for Crystal standard production were selected for their proven capability to provide product processed to military requirements.

At the time of this publication, wafer fab, packaging, and test facility have all passed Crystal military audit. Qualification lots are in process. Our CAGE FSCM/MILSCAP number is 0A384.

This advance planning will enable Crystal Semiconductor to offer MIL STD 883C Class B compliant production on most Data Acquisition circuits during 1988. Consult Crystal for the exact availability dates of any specific product.

DIE SALES

Systems have been established at Crystal to fully support sale of integrated circuits at the die level.

All die manufacturing activities maintain configuration control and traceability to the original wafer lot. Passivation thicknesses are controlled to meet military requirements and die storage is maintained in accordance with MIL STD 883, method 2010. Scribed and broken individual die are 100% inspected to the requirements of MIL STD 883, method 2010, test condition B. Shipment of die to Crystal customers is accomplished in waffle packs which each contain die from only one wafer lot.

INTRODUCTION

Crystal offers a range of T1/CCITT line interface ICs which provide a programmable pulse shaping line-driver, a timing and data recovery circuit, a jitter attenuator and diagnostic features all in single VLSI analog CMOS devices.

The CS6158, CS61534 and CS61574 are an upwards pin compatible family of T1/CCITT line interfaces designed as front ends to PCM framing transceivers. Basic functionality is provided in the CS6158. Increased functionality including microprocessor bus control interfaces and two jitter attenuation options are provided by the CS61534 and CS61574. The CS61544 is designed for stand alone T1 applications where PCM framing transceivers are not required (such as high speed modems and multiplexors). The CS6152 is designed as a cost-effective front end to digital, gate-array based, clock recovery circuits, providing exactly those analog driver and receiver interface functions that must be implemented external to the ASIC device.

USER'S GUIDE

	Compatible Family of Line Interface ICs for use with Framing Tranceivers				Line Interface IC for Stand Alone Use
Device:	CS6158	CS6152	CS61534	CS61574	CS61544
Data Rates:					
1.544 MHz	♥	♥	♥	♥	♥
2.048 MHz	♥	♥	♥	♥	
Transmitter:					
DSX-1 Driver	♥	♥	♥	♥	♥
G.703 Driver	♥	♥	♥	♥	
Driver Monitor		♥	♥	♥	♥
Jitter Attenuator			♥		♥
Receiver:					
Narrow Band Clock Recovery			♥		♥
Wide Band Clock Recovery	♥			♥	
Wander Attenuator				♥	
AMI to TTL Buffer		♥			
µP Bus Control Option			♥	♥	
AMI/B8ZS Encode/Decode					♥
Loopbacks	♥		♥	♥	♥
Package	22/28 pin DIP	24 pin DIP	28 pin DIP	28 pin DIP	28 pin DIP

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Semiconductor Corporation

CS61534

PCM Line Interface

Features

- Provides Analog PCM Line Interface for T1 and 2.048 MHz Applications
- Programmable Pulse-Shaping Line Driver
- Performs Data and Timing Recovery
- Transparent to AMI Polarity
- Diagnostic and Performance Monitoring Features
- Selectable Hardware or Host Processor Modes
- Jitter Attenuator
- 3 Micron CMOS for High Reliability

General Description

The CS61534 combines the analog transmit and receive line interface functions for a PCM system interface in one 28 pin device. The PCM line interface operates from a single 5 Volt supply, is transparent to the PCM framing format, and can work with ABAM and other cable types.

Crystal's SMART ANALOG™ circuitry shapes the transmit pulse internally, providing the appropriate pulse shape at the DSX-1 cross-connect for line lengths ranging from 0 to 655 feet in T1 applications. Maximum range is greater than 450 meters. The transmitter uses an elastic store to remove jitter from the outgoing data prior to transmission.

Applications

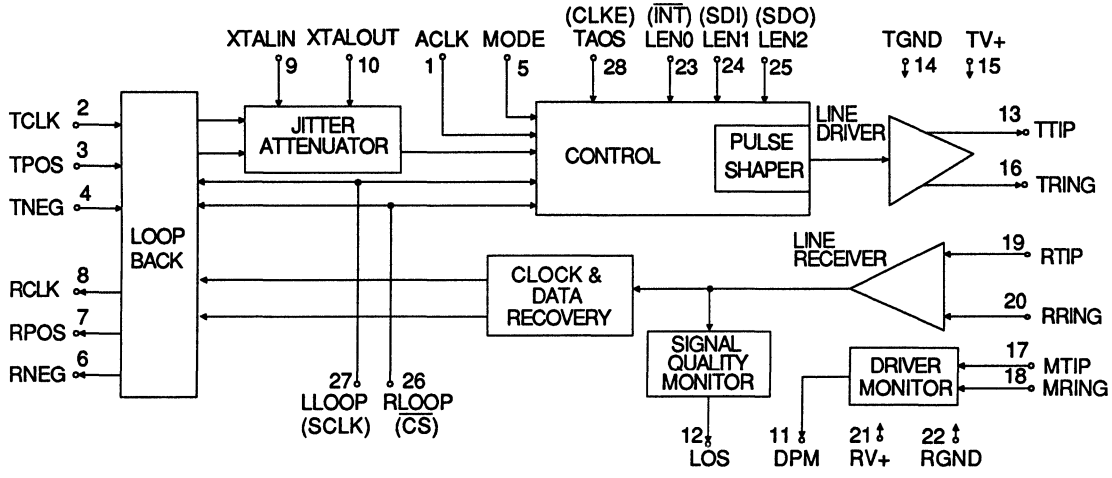
- Interfacing Network Equipment to a DSX-1 Cross Connect.
- Interfacing Customer Premises Equipment such as PABXs, T1 Multiplexers, Data PBXs and LAN Gateways to a Channel Service Unit or T1 modem.

ORDERING INFORMATION

CS61534-IP - 28 Pin Plastic DIP (T1 only)
CS61534-IP1- 28 Pin Plastic DIP (T1 & CEPT)
CS61534-IL - 28 J-lead PLCC (T1 only)
CS61534-IL1 - 28 J-lead PLCC (T1 & CEPT)

2

Block Diagram



Crystal Semiconductor Corporation
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(512)445-7222 TWX:910-874-1352

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply (referenced to GND)	RV+, TV+	-	6.0	V
Input Voltage, Any Pin (Note 1)	V_{in}	RGND-0.3	RV+ + 0.3	V
Input Current, Any Pin (Note 2)	I_{in}	-	10	mA
Ambient Operating Temperature	T_A	-40	85	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes: 1. Excluding RTIP, RRING.
2. Transient currents of up to 100 mA will not cause SCR latch-up.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply (Note 3)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature	T_A	-40	25	85	°C
Total Power Dissipation (Note 4) 100% ones density & max. line length @ 5.25V	P_D	-	-	760	mW

Notes: 3. TV+ must not exceed RV+ by more than 0.3V.
4. Power dissipation while driving 25 Ω load over operating temperature range. Includes CS61534 and load.

ANALOG SPECIFICATIONS (T_A = - 40 ° to 85 ° C, V+ = 5.0V ± 5%, GND = 0V)

Parameters	Min	Typ	Max	Units
Receiver Sensitivity Below DSX-1	-10	-	-	dB
Jitter Attenuation Curve Corner Frequency T1 (Note 5)	-	-	50	Hz
Jitter Attenuation Curve Corner Frequency CEPT (Note 6)	-	40	-	Hz
Input Jitter Tolerance - Transmitter	7.0	-	-	Unit Intervals
Transmitter Output Load (Note 7)	-	25	-	ohms
Loss of Signal Threshold	-	0.5	-	V

Notes: 5. Crystal pull range: ± 200 ppm. Five unit intervals of input jitter.
6. Crystal pull range: ± 66 ppm. 1.5 unit intervals of input jitter.
7. Transmitter is a low impedance voltage source. Transmitter performance is typical with a 25Ω load for T1 applications, which is determined by the 2:1 turns ratio of transformer and 100 Ω line impedance.

DIGITAL CHARACTERISTICS (T_A = - 40 ° to 85 ° C, V+ = 5.0V ± 5%, GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (Notes 8, 9) PINS 1-5, 23-28	V_{IH}	2.0	-	-	V
Low-Level Input Voltage (Notes 8, 9) PINS 1-5, 23-28	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Notes 8, 9) I_{OUT}=-40 uA PINS 6-8, 11, 12, 23, 25	V_{OH}	2.4	-	-	V
Low-Level Output Voltage (Notes 8, 9) I_{OUT}= 1.6 mA PINS 6-8, 11, 12, 23, 25	V_{OL}	-	-	0.4	V
Input Leakage Current		-	-	±10	uA
High Impedance Leakage Current PIN 25 (Note 8)		-	-	±10	uA

Notes: 8. Functionality of pins 23 and 25 depends on the mode. See Host/Hardware mode description.
9. Output drivers will output CMOS logic levels into a CMOS load.

T1 SWITCHING CHARACTERISTICS (T_A = - 40 ° to 85 ° C, V+ = 5.0V ± 5%, GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter	Symbol	Min	Typ	Max	Units
Crystal Frequency (Note 10)	f_c	-	6.176000	-	MHz
TCLK Frequency	f_{in}	-	1.544	-	MHz
ACLK Frequency (Note 11)	f_{out}	-	1.544	-	MHz
RCLK Pulse Width	t_{pwh}	-	324	-	ns
(Note 12)	t_{pwl}	-	324	-	ns
Duty Cycle (Note 13)		-	50	-	%
Rise Time, All Digital Outputs (Note 14)	t_r	-	-	100	ns
Fall Time, All Digital Outputs (Note 14)	t_f	-	-	100	ns
TPOS/TNEG to TCLK Falling Setup Time	t_{su}	0	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time	t_h	50	-	-	ns
RPOS/RNEG to RCLK Rising Setup Time	t_{su}	-	274	-	ns
RCLK Rising to RPOS/RNEG Hold Time	t_h	-	274	-	ns
Reset Pulse Duration		0.2	-	2000	us

Notes: 10. Crystal must meet specifications described in *Applications* section of this data sheet.
11. ACLK provided by an external source.
12. The sum of the pulse widths must always meet the frequency specifications.
13. Duty cycle is (t_{pwh} / (t_{pwh} + t_{pwl})) * 100%.
14. At max load of 1.6 mA and 50 pF.

CCITT SWITCHING CHARACTERISTICS (T_A = - 40 ° to 85 ° C, V+ = 5.0V ± 5%, GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 15)	f_c	-	8.192000	-	MHz
TCLK Frequency		f_{in}	-	2.048	-	MHz
ACLK Frequency	(Note 16)	f_{out}	-	2.048	-	MHz
RCLK Pulse Width		t_{pwh}	-	244	-	ns
	(Note 17)	t_{pwl}	-	244	-	ns
Duty Cycle	(Note 18)		-	50	-	%
Rise Time, All Digital Outputs	(Note 19)	t_r	-	-	100	ns
Fall Time, All Digital Outputs	(Note 19)	t_f	-	-	100	ns
TPOS/TNEG to TCLK Falling Setup Time		t_{su}	0	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time		t_h	50	-	-	ns
RPOS/RNEG to RCLK Rising Setup Time		t_{su}	-	194	-	ns
RCLK Rising to RPOS/RNEG Hold Time		t_h	-	194	-	ns
Reset Pulse Duration			0.2	-	2000	us

Notes: 15. Crystal must meet specifications described in *Applications* section of this data sheet.
16. ACLK provided by an external source.
17. The sum of the pulse widths must always meet the frequency specifications.
18. Duty cycle is (t_{pwh} / (t_{pwh} + t_{pwl})) * 100%.
19. At max load of 1.6 mA and 50 pF.

SWITCHING CHARACTERISTICS - HOST MODE (T_A = - 40 ° to 85 ° C, V+ = 5.0V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter	Symbol	Min	Typ.	Max	Units
SDI to SCLK Setup Time	t_{dc}	50	-	-	ns
SCLK to SDI Hold Time	t_{cdh}	50	-	-	ns
SCLK Low Time	t_{cl}	250	-	-	ns
SCLK High Time	t_{ch}	250	-	-	ns
SCLK Rise and Fall Time	t_r , t_f	-	-	50	ns
$\overline{CS}$ to SCLK Setup Time	t_{cc}	50	-	-	ns
SCLK to $\overline{CS}$ Hold Time	t_{cch}	50	-	-	ns
$\overline{CS}$ Inactive Time	t_{cwh}	250	-	-	ns
SCLK to SDO Valid (Note 20)	t_{cdv}	-	-	200	ns
$\overline{CS}$ to SDO High Z	t_{cdz}	-	100	-	ns

Note: 20. Output load capacitance = 50 pF.

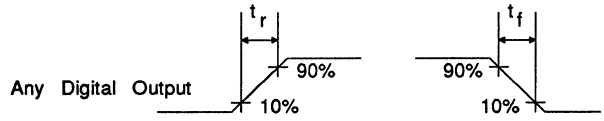


Figure 1. - Signal Rise and Fall Characteristics

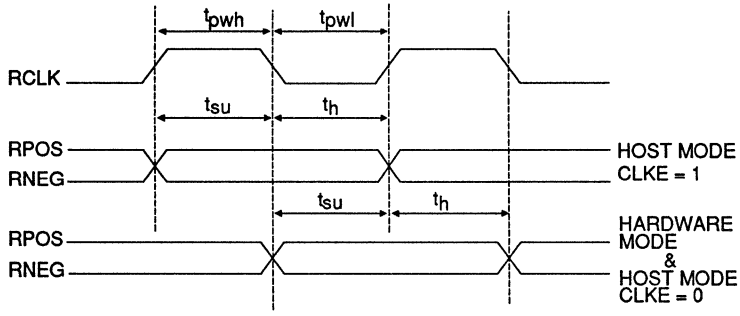


Figure 2. - Recovered Clock and Data Switching Characteristics

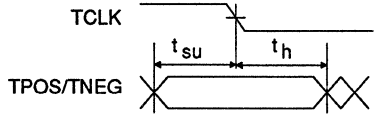


Figure 3. - Transmit Clock and Data Switching Characteristics

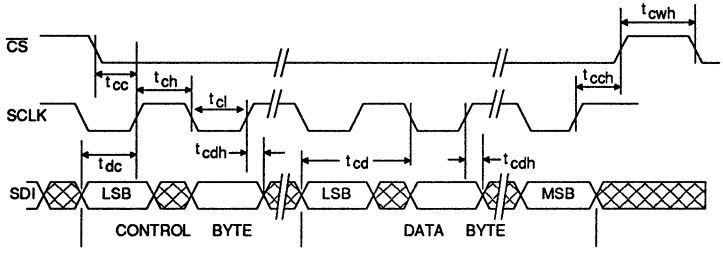


Figure 4. - Serial Port Write Timing Diagram

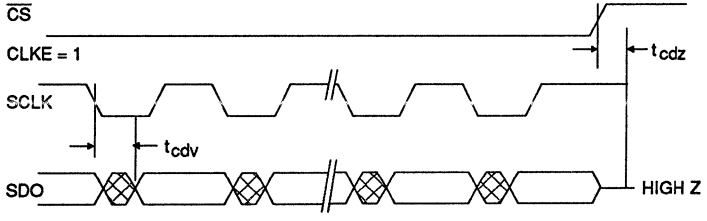


Figure 5. - Serial Port Read Timing Diagram

THEORY OF OPERATION

Transmitter

The transmitter takes binary (unipolar) data from a PCM transceiver and produces alternate bipolar pulses of appropriate shape. The transmit clock and transmit data (TCLK, TPOS & TNEG) are supplied synchronously. Data is sampled on the falling edge of the input clock.

The CCITT pulse shape and T1 pulse shapes for line lengths from 0 to 655 feet (as measured from the CS61534 to the DSX-1 cross connect) are selectable. Pulse shaping and signal level are determined by "line length select" inputs and require no external circuitry. Pulse shaping is accomplished with a slew rate controlled fast digital to analog converter. Alternate mark inversion operation is implemented by driving the line in a true differential manner. In order to achieve the necessary line voltages, which exceed the 5 volt supply, a two-to-one, step-up transformer is required. The line driver is a low-impedance voltage source designed to drive a 25 Ω equivalent load.

To place the device in a low power dissipation mode (i.e., to disable the drive), the TPOS and TNEG should be held low while TCLK continues to be input. When any transmit control pin (TAOS, LEN0-2, LLOOP, or RLOOP) is toggled, the transmitter stabilizes within 16 bit periods.

Transmit Line Length Selection

For T1 applications, the line length selection supports both a three partition arrangement for ICOT and MAT cable, and a five partition arrangement for ABAM and PIC cable as shown in Table 1. For each line length selected, the CS61534 modifies the output pulse to meet the requirements of Technical Advisory 34 and TR-TSY-000009. The exact pulse shape achieved at the DSX-1 can be effected by details of the board layout, transformer selection, and other factors. Once board layout is completed, it is recommended that the line length settings be evaluated. It is possible that an alternative interpretation of the LEN2/1/0 distance ranges is more appropriate. A typical output pulse is shown in Figure 6.

LEN2	LEN1	LEN0	LINE LENGTH SELECTED (FEET)	CABLE TYPE
0	1	1	0-220	MAT and ICOT
0	0	1	220-440	
0	1	0	440-655	
0	1	1	0-133	ABAM and PIC
1	0	0	133-266	
1	0	1	266-399	
1	1	0	399-533	
1	1	1	533-655	
0	0	0	G.703	2.048 MHz CCITT

Table 1 - Line Length Selection

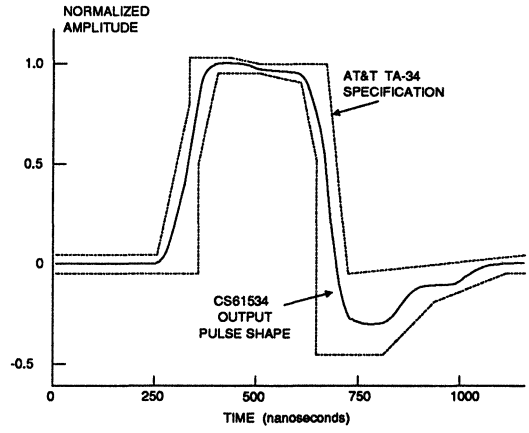


Figure 6 - Typical Pulse Shape at DSX-1 Cross Connect

The remaining line length selection is for CCITT options. Transformer and resistor values depend on whether the coax or shielded cable is used, as

	For coaxial cable, 75 ohm load and transformer specified in Table A2.	For shielded twisted pair, 120 ohm load and transformer specified in Table A2.
Nominal peak voltage of a mark (pulse)	2.37 V	3 V
Peak voltage of a space (no pulse)	0 ± 0.237 V	0 ± 0.3 V
Nominal pulse width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the centerof the pulse interval	0.95 to 1.05	
Ratio of the widths of positive and negative pulses at the nominal halfamplitude	0.95 to 1.05	

Table 2 - CCITT G.703 Pulse Specifications

shown in the *Applications* section at the back of this data sheet. The CCITT pulse shape meets the template shown in Figure 7, assuming the conditions shown in Table 2 are met.

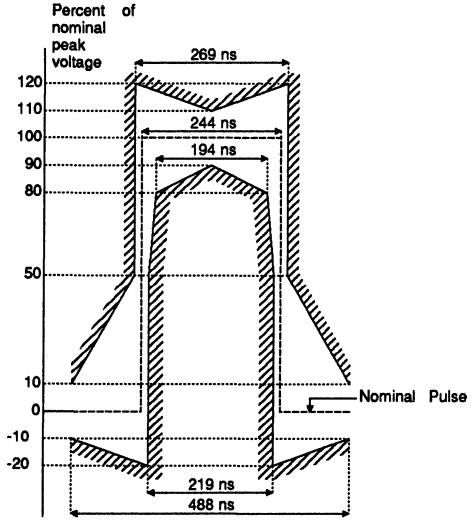


Figure 7 - Mask of the Pulse at the 2048 kbps Interface

Transmit Jitter Attenuator

The CS61534 will tolerate and attenuate at least seven unit intervals of jitter (peak-to-peak) from a signal. Figure 8 shows a family of curves which show the jitter attenuation achieved by the CS61534 at T1 data rates. Each curve shows the jitter attenuation for a signal with constant jitter amplitude over a range of jitter frequencies. The

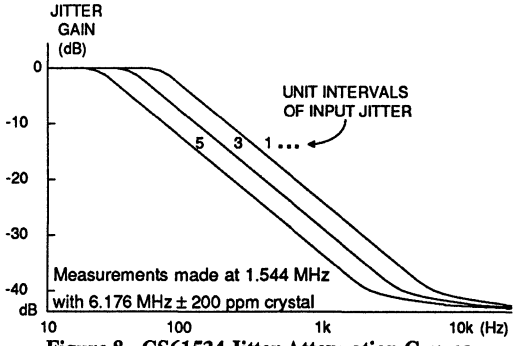


Figure 8 - CS61534 Jitter Attenuation Curves

more jitter a signal has, the more the jitter is attenuated. The jitter attenuator on the transmitter side meets the jitter attenuation and input tolerance specifications of AT&T Publication 43802, as shown in Figures 9 and 10. CCITT jitter attenuation performance is discussed in the *Applications* section (page 17).

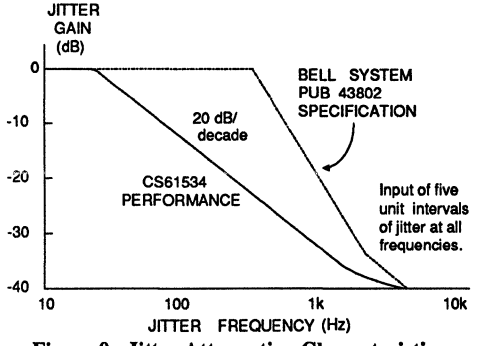


Figure 9 - Jitter Attenuation Characteristics

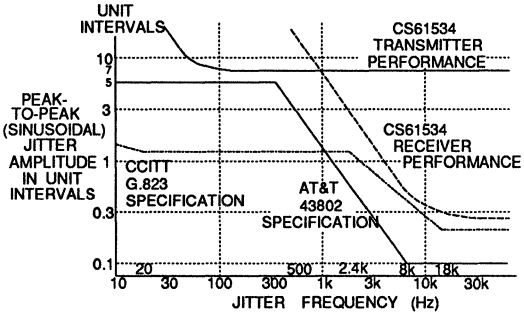


Figure 10 - Input Jitter Tolerance

Jitter attenuation is accomplished by means of a 16-bit FIFO and a variable oscillator. The frequency of the variable oscillator is controlled by logic in the CS61534 to be the same as the average input clock signal, TCLK. TCLK controls the write pointer of the FIFO. Data present on TPOS/TNEG is written into the memory location selected by the write pointer. The read pointer of the FIFO, and the transmit frequency of the device, are determined by the crystal oscillator. Internal logic tracks the relative positions of the FIFO's pointers, and adjusts the oscillator's load capacitance, which controls its frequency to maintain the FIFO in a half full condition (read and write pointers kept 8-bits apart). Slow changes in input signal frequency are tracked, while high frequency variations in the TCLK signal are absorbed by the FIFO.

The external reference crystal used by the jitter attenuator should have a nominal frequency of 6.176 MHz, (8.192 MHz for CCITT rates), and have a pull range, in the oscillator circuit, that is sufficient to meet the frequency tolerance requirements specified for the system. Furthermore, the frequency tolerance must be met over all operating temperatures. The jitter attenuator can be disabled by driving XTALIN with a clock which is *exactly* four times the TCLK frequency. Disabling the jitter attenuator also disables remote loopback.

Transmit All Ones Select

The transmitter provides for all ones insertion at the frequency of the alternate clock input, ACLK. The transmit clock can be used as the alternate clock by connecting pins 1 and 2 together. Transmit all ones is selected when TAOS goes high, and causes continuous ones to be transmitted on the line (TTIP and TRING) using the alternate clock, ACLK. In this mode, the TPOS, TNEG and TCLK inputs are ignored. If Remote Loopback is in effect, any TAOS request will be ignored.

Receiver

The receiver extracts data and clock from an AMI (Alternate Mark Inversion) coded signal and outputs clock and synchronized data. The receiver is sensitive to signals over the entire range of DSX-1/CCITT cable lengths and requires no equalization. The signal is received on both ends of a center-tapped, center-grounded transformer. The transformer is center tapped on the CS61534 side. The clock and data recovery circuit meets or exceeds the jitter tolerance specifications of Publication 43802 and CCITT G. 823, (see Figure 10).

The two leads of the transformer (RTIP and RRING) have opposite polarity allowing the receiver to treat RTIP and RRING as unipolar signals. Comparators are used to detect pulses on RTIP and RRING. The comparator thresholds are dynamically established by peak detectors.

Clock recovery is achieved through a frequency and phase lock loop (FPLL). Upon power up and reset of the CS61534, and prior to the start of clock acquisition, the FPLL has its center frequency trained. A current controlled oscillator (ICO) is trained relative to the crystal oscillator frequency reference. The current is adjusted until it is just sufficient to change a fixed capacitor to a fixed reference voltage in a half period of the reference clock. This current is then held

constant. The FPLL is controlled, small signal, by the output of the phase detector and loop filter, which takes the form of a current. This is added to the fixed current to modulate the ICO about the center frequency and close the loop. This training limits the lock range of the FPLL to ± 6% of the trained frequency (1.544 MHz for T1 or 2.048 MHz for CCITT), guaranteeing that the FPLL is immune to false lock. The FPLL is insensitive to variations in temperature and slight variations in power supply voltage, but fairly large changes in power supply voltage will change the control current in the FPLL, reducing its effectiveness.

In the hardware mode, data at RPOS and RNEG is stable and may be sampled on the rising edge of the recovered clock. In the host mode, CLKE determines the clock polarity for which output data is stable and valid as shown in Table 3.

MODE (pin 5)	CLKE (pin 28)	DATA	CLOCK	Clock Edge for Valid Data
LOW	X	RPOS RNEG	RCLK RCLK	Rising Rising
HIGH	LOW	RPOS RNEG SDO	RCLK RCLK SCLK	Rising Rising Falling
HIGH	HIGH	RPOS RNEG SDO	RCLK RCLK SCLK	Falling Falling Rising

X= Don't care

Table 3 - Data Output / Clock Relationship

Loss of Signal

The receiver reports loss of the received signal on the Loss of Signal pin, LOS. The threshold for loss of signal is 0.5 volts. A loss of signal will be indicated within 200 bit periods if an active signal falls below the threshold. In the event that the input signal drops to zero volts, the loss of signal will be indicated within 32 bit periods. When a loss of signal is detected, RPOS and RNEG are not valid, but the receiver will continue to try to recover data. LOS will return to a low state when a valid signal returns to RTIP and RRING. RCLK is always output but may drift up to 6% from the nominal frequency. Note that in the host mode, LOS is simultaneously available from pin 12 and the register.

Local Loopback

The local loopback mode bypasses the receive circuit and routes the digital transmit clock and data to the receive clock and data pins. A local loopback occurs in response to LLOOP going high. The transmit data and clock signals (TPOS, TNEG and TCLK) are sent out on the line through TTIP and TRING unless transmit all ones, TAOS, is selected, in which case AMI-coded continuous ones are transmitted on the line at the rate determined by ACLK.

Remote Loopback

In remote loopback, the recovered clock and data input on RTIP and RRING are sent through the elastic store to remove jitter, and back out on the line via TTIP and TRING. Selecting remote loopback overrides any TAOS request (see Table 4). The recovered incoming signals are also sent to RCLK, RPOS and RNEG. A remote loopback occurs in response to RLOOP going high. Simultaneous selection of local and remote loopback modes is not valid (see Reset). Bipolar violations are passed unchanged through the CS61534 during remote loopback.

RLOOP Input Signal	TAOS Input Signal	Source of Data for TTIP & TRING	Source of Clock for TTIP & TRING
0	0	TPOS & TNEG	TCLK
0	1	all 1s	ACLK
1	X	RTIP & RRING	RTIP & RRING

Notes:
1. X = Don't care. The identified All Ones Select input is ignored when the indicated loopback is in effect.
2. Logic 1 indicates that Loopback or All Ones option is selected.

Table 4 - Interaction of RLOOP and TAOS

Driver Performance Monitor

To aid in early detection and easy isolation of nonfunctioning links, the CS61534 is able to monitor transmit drive performance and report when the driver is no longer operational. This feature can be used to monitor either the device's performance or the performance of a neighboring CS61534. The driver performance monitor indicator is normally at a low (zero) logic level, and goes to high level upon detecting driver failure.

The driver performance monitor consists of a receiver that monitors the transmitted signal on input pins, MTIP and MRING. If no signal is present on MTIP and MRING for 32 clock cycles, the DPM pin goes high.

Whenever more than one CS61534 reside on the same circuit board, the effectiveness of the driver performance monitor can be maximized by having each CS61534 monitor performance of a neighboring CS61534 device, rather than having it monitor its own performance. Note that in the host mode, DPM is available from both the register and pin 11.

Reset

The CS61534 initiates internal reset procedures either upon power up or in response to a reset request. After initial power up, the device will delay for 10 ms after the oscillator starts to allow the power supply and the oscillator to stabilize before initiating the training procedure for the FPLL. Training the FPLL takes at most 43 ms, but typically requires less than half that amount of time. If the power supply has not reached stable operating voltage within 10 ms, the device should be reset after the power supply has stabilized. These conditions should also be adhered to if temporary loss of power supply occurs.

In the Hardware Mode, a reset request is made by simultaneously setting both RLOOP and LLOOP high for a period not to exceed 2 ms. Reset will be completed within 53 ms after the falling edge of the reset request (falling edge of RLOOP and LLOOP).

In the Host Mode, a reset is initiated by simultaneously writing RLOOP and LLOOP to the register. The device will first clear its data registers then initiate the FPLL training procedure which will be complete within 53 ms.

During the reset procedure, the loss of signal indicator, LOS, is high. Once the reset procedures are completed, the loss of signal indicator goes low signifying that normal operation of the device has begun.

Mode of Operation

The CS61534 can be operated in two modes, the hardware mode and the host mode. In the hardware mode, discrete pins are used to interface the device's control functions and status information. In the host mode, the CS61534 is connected to a host processor and a serial data bus is used for input and output of control and status information. There are six dual function pins whose functionality is determined by the mode pin, MODE. Table 5 shows the pin definitions.

PIN #	MODE	
	HARDWARE	HOST
PIN 23	LEN0	$\overline{INT}$
PIN 24	LEN1	SDI
PIN 25	LEN2	SDO
PIN 26	RLOOP	$\overline{CS}$
PIN 27	LLOOP	SCLK
PIN 28	TAOS	CLKE

Table 5 - Pin Definitions

Serial Interface

In the host mode, pins 23 through 28 serve as a microprocessor/microcontroller interface. One on-board register can be written to the SDI pin or

read from the SDO pin at the clock rate determined by SCLK. Through this register, a host controller can be used to control operational characteristics and monitor device status. The serial port read/write timing is independent of the system transmit and receive timing.

Data transfers are initiated by taking the chip select input, $\overline{CS}$, low ($\overline{CS}$ must initially be high). Address and input data bits are clocked in on the rising edge of SCLK. The clock edge on which output data is stable and valid is determined by CLKE as shown in Table 3. Data transfers are terminated by setting $\overline{CS}$ high. $\overline{CS}$ may go high no sooner than 50 ns after the falling edge of the 16th SCLK cycle, and must go high before the rising edge of the 24th SCLK cycle.

Figure 11 shows the timing relationships for data transfers when CLKE = 1. When CLKE = 0, data output from the serial port, SDO, is valid on the falling edge of SCLK. Data bit D7 is held until the rising edge of the 17th clock cycle.

An address/command byte, shown in Table 6, precedes a data register. The first bit of the address/command byte determines whether a read or a write is requested. The next six bits contain the address. The CS61534 responds to address 16 (0010000). The last bit is ignored.

LSB, first bit	0	R/$\overline{W}$	Read/Write Select; 0 = write, 1 = read
	1	ADD0	LSB of address. Must be 0
	2	ADD1	Must be 0
	3	ADD2	Must be 0
	4	ADD3	Must be 0
	5	ADD4	Must be 1
	6	-	Reserved - Must be 0
MSB, last bit	7	X	Don't Care

Table 6 - Address/Command Byte

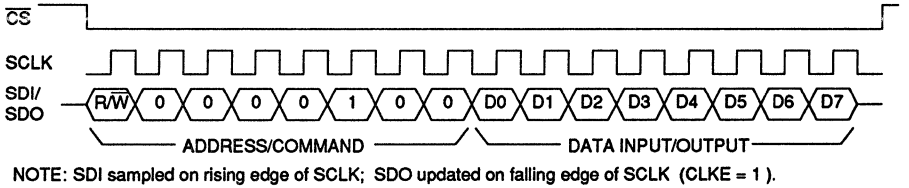
The data register, shown in Table 7, can be read/written by the serial port. Data is input/-output on the eight clock cycles immediately following the address/command byte. Bits 0 and 1 are read only. During a write to the register, the CS61534 ignores the first two bits of the data byte. SDO goes to a high-impedance state when not in use. SDO and SDI may be tied together in applications where the host processor has a bidirectional I/O port.

LSB: first bit in or out	0	LOS	Loss Of Signal
	1	DPM	Driver Performance Monitor
	2	LEN0	Bit 0 - Line Length Select
	3	LEN1	Bit 1 - Line Length Select
	4	LEN2	Bit 2 - Line Length Select
	5	RLOOP	Remote Loopback
	6	LLOOP	Local Loopback
MSB: last bit in or out	7	TAOS	Transmit All Ones Select

Table 7 - Data Register

Power Supply

The device operates from a single 5 volt supply. Separate pins for transmit and receive supplies provide internal isolation. However these pins may be connected externally with no impact on device performance, provided the power supply pins are decoupled to their respective grounds. The transmit power supply should be decoupled from ground with a 68 µF capacitor and a mylar or ceramic 1.0 µF capacitor. A 0.1 µF mylar or ceramic capacitor should be used on the receive power supply. These capacitors should be located physically close to the device. TV+ must not exceed RV+ by more than 0.3V.

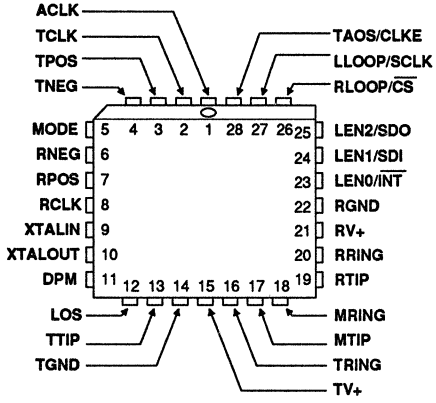


NOTE: SDI sampled on rising edge of SCLK; SDO updated on falling edge of SCLK (CLKE = 1).

Figure 11 - Input / Output Timing

PIN DESCRIPTIONS

ALTERNATE EXTERNAL CLOCK	ACLK	1	28	TAOS/CLKE	TRANSMIT ALL ONES / CLOCK EDGE
TRANSMIT CLOCK	TCLK	2	27	LLOOP/SCLK	LOCAL LOOPBACK / SERIAL CLOCK
TRANSMIT POSITIVE PULSE	TPOS	3	26	RLOOP/$\overline{CS}$	REMOTE LOOPBACK / CHIP SELECT
TRANSMIT NEGATIVE PULSE	TNEG	4	25	LEN2/SDO	LINE / SERIAL DATA OUT
MODE SELECTION	MODE	5	24	LEN1/SDI	LENGTH / SERIAL DATA OUT
RECEIVED NEGATIVE PULSE	RNEG	6	23	LEN0/$\overline{INT}$	SELECT / ALARM INTERUPT
RECEIVED POSITIVE PULSE	RPOS	7	22	RGND	RECEIVE GROUND
RECOVERED CLOCK	RCLK	8	21	RV+	RECEIVE V+ (+5VDC)
CRYSTAL CONNECTION	XTALIN	9	20	RRING	RECEIVE RING
CRYSTAL CONNECTION	XTALOUT	10	19	RTIP	RECEIVE TIP
DRIVER PERFORMANCE MONITOR	DPM	11	18	MRING	MONITORED RING
LOSS OF SIGNAL	LOS	12	17	MTIP	MONITORED TIP
TRANSMIT TIP	TTIP	13	16	TRING	TRANSMIT RING
TRANSMIT GROUND	TGND	14	15	TV+	TRANSMIT V+ (+5VDC)



Power Supplies

TV+ - Positive Power Supply, Transmit Drivers, Pin 15.

Positive power supply for the transmit drivers; typically +5 volts. TV+ must not exceed RV+ by more than 0.3V.

TGND - Ground, Transmit Drivers, Pin 14.

Power supply ground for the transmit drivers; typically 0 volts.

RV+ - Positive Power Supply, Pin 21.

Positive power supply for the device, except transmit drivers; typically +5 volts.

RGND - Ground, Pin 22.

Power supply ground for the device, except transmit drivers; typically 0 volts.

Oscillator

XTALIN, XTALOUT - Crystal Connections, Pins 9 and 10.

A 6.176 MHz (8.192 MHz for CCITT applications) crystal should be connected across these pins. If desired, an externally generated 6.176 MHz (8.192 MHz for CCITT) clock signal may be input to XTALIN, pin 9; XTALOUT, pin 10, should be left floating. Overdriving the oscillator with an external source disables the jitter attenuator. This externally generated clock must be *exactly* four times the frequency of the TCLK signal.

Control

MODE - Mode Select, Pin 5.

Setting MODE to logic 1 puts the CS61534 in the host mode. In the host mode, a serial control port is used to control the CS61534 and determine its status. Setting MODE to logic 0 puts the CS61534 in the hardware mode, where configuration and status are controlled by discrete pins. MODE defines the status of pins 23 through 28.

Hardware Mode

TAOS - Transmit All Ones Select, Pin 28.

Setting TAOS to a logic 1 causes continuous ones to be transmitted at the frequency determined by ACLK.

LLOOP - Local Loopback, Pin 27.

Setting LLOOP to a logic 1 routes the transmit clock and data to the receive clock and data pins, bypassing the receive circuit. TCLK and TPOS/TNEG are still transmitted unless overridden by a TAOS request.

RLOOP - Remote Loopback, Pin 26.

Setting RLOOP to a logic 1 causes the recovered clock and data to be sent through the jitter attenuator and through the driver back to the line. The recovered signal is also sent to RCLK and RPOS/RNEG. Any TAOS request is ignored. If the oscillator is being driven with a 4x clock, the remote loopback function is not possible.

Simultaneously taking RLOOP and LLOOP high for less than 2 ms initiates a device reset.

LEN0, LEN1, LEN2 - Line Length Selection, Pins 23, 24 and 25.

Determines the shape and amplitude of the transmitted pulse to accommodate several cable types and lengths. See Table 1 for information on line length selection.

Host Mode

$\overline{\text{INT}}$ - Receive Alarm Interrupt, Pin 23.

Goes low when received signal is lost (LOS is high), or the transmitter driver has failed (DPM is high), to flag the host processor. $\overline{\text{INT}}$ will stay low until the fault condition goes away. $\overline{\text{INT}}$ is an open drain output and should be tied to the positive supply through a resistor.

SDI - Serial Data Input, Pin 24.

Data for the on-chip registers and is sampled on the rising edge of SCLK.

SDO - Serial Data Output, Pin 25.

Status and control information from the on-chip registers. If CLKE is high SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to or $\overline{CS}$ is high.

CLKE - Clock Edge, Pin 28.

Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. Conversely, setting CLKE to logic 0 causes RPOS and RNEG to be valid on the rising edge of RCLK, and SDO to be valid on the falling edge of SCLK.

SCLK - Serial Clock, Pin 27.

Clock used to read or write the serial port registers.

$\overline{CS}$ - Chip Select, Pin 26.

Pin must transition from high to low to read or write the serial ports.

Inputs

ACLK - Alternate External Clock, Pin 1.

This input should be tied to TCLK or some other externally generated 1.544 (or 2.048) MHz clock. The frequency of ACLK determines the rate at which TAOS is output.

TCLK, TPOS, TNEG - Transmit Clock, Transmit Positive Data, Transmit Negative Data - Pins 2, 3 and 4.

Inputs for clock and data to be transmitted. Signal jitter is attenuated and the signal is driven on to the line through TTIP and TRING. TPOS and TNEG are sampled on the falling edge of TCLK. A TPOS input causes a positive pulse to be transmitted, while a TNEG input causes a negative pulse to be transmitted.

RTIP, RRING - Receive Tip, Receive Ring, Pins 19 and 20.

The AMI receive signal is input to these pins. A center-tapped, center-grounded, 2:1, step-up transformer is required on these inputs, as shown in Figure A1. Data and clock are recovered and output on RPOS/RNEG and RCLK.

MTIP, MRING - Monitored Tip, Monitored Ring, Pins 17 and 18.

These pins are normally connected to TTIP and TRING and monitor the output of a CS61534. If the monitors are not used, tying MTIP low and MRING high through a resistor will reduce power consumption slightly. If the $\overline{INT}$ pin in the host mode is used, and the monitor is not used, input a clock signal to one of the monitor pins and tie the other monitor pin to approximately the clock's mid-voltage level. This clock frequency can range from 100 kHz to the TCLK frequency.

Status

LOS - Loss of Signal, Pin 12.

LOS goes to a logic 1 when the received signal falls below a 0.5 volt threshold, or after 32 clock cycles with out a detected one. LOS returns to logic 0 when signal returns.

DPM - Driver Performance Monitor, Pin 11.

If no signal is present on MTIP and MRING for 32 clock cycles, DPM goes to a logic 1 until the first detected signal.

Outputs

RCLK, RPOS, RNEG - Recovered Clock, Receive Positive Data, Receive Negative Data - Pins 8, 7 and 6.

Data and clock are recovered from the RTIP and RRING inputs are output at these pins. A signal on RPOS corresponds to a positive pulse received on RTIP and RRING, while a signal on RNEG corresponds to the receipt of a negative pulse. RPOS and RNEG are NRZ. In the hardware mode, RPOS and RNEG are stable and valid on the rising edge of RCLK. In the host mode, CLKE determines the clock edge for which RPOS and RNEG are stable and valid. See Table 3.

TTIP, TRING - Transmit Tip, Transmit Ring, Pins 13 and 16.

The AMI signal is driven to the line through these pins. This output is designed to drive a 25 Ω load. A 2:1 step-up transformer is required as shown in Figure A1. When driving 75 Ω coax cable, two 2.2 Ω resistors should be added as shown in Figure A2. The transmitter will drive twisted-shielded pair cable, terminated with 120 Ω, without additional components.

APPLICATIONS

Line Interface

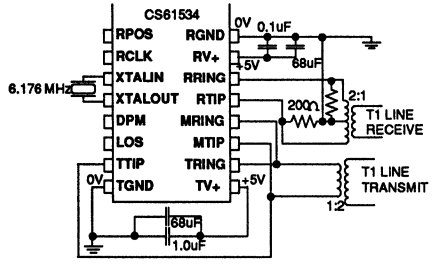


Figure A1. - Typical Configuration Showing Line Interface

Figure A1 shows the typical configuration for interfacing the CS61534 to a T1 line through transmit and receive transformers. The receiver transformer is center tapped and center grounded with 200 Ω resistors between the center tap and each leg on the CS61534 side. These resistors provide the 100 Ω termination for the T1 line. When terminating twisted-shielded pair cable, 240 Ω resistors will provide the required 120 Ω load.

Figure A2 shows the configuration needed for transmitting data at 2.048 MHz onto a 75 Ω coax cable. The 2.2 Ω resistors serve two functions.

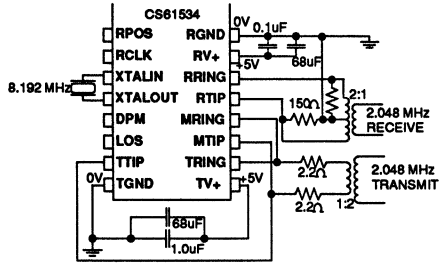


Figure A2. - Configuration for Transmitting onto 75 Ω Coax

First, they provide the appropriate 25 Ω load to TTIP and TRING. Second, the resistors attenuate the signal slightly to meet the CCITT pulse amplitude requirements. Note that these 2.2 Ω resistors should not be used when interfacing to CCITT 120 Ω cable. For the receiver, the terminating resistors should be 150 Ω to provide the necessary 75 Ω termination to the line.

Decoupling and filtering of the power supplies is crucial for proper operation of the analog sections in the transmit and receive paths. If the same power and ground buses supply both the transmitter and receiver supply inputs, the 68 µF capacitor shown on the transmit supply can be eliminated. The decoupling capacitors shown in Figures A1 and A2 should be high grade capacitors, (i.e., 68 µF - tantalum or better; 1.0 and 0.1 µF - mylar or ceramic), and should be located as close as possible to the power supply pins of the chip. Wire wrap bread-boarding of the CS61534 is not recommended because lead resistance and wrap inductance serve to defeat the function of the decoupling capacitors.

Selecting an Oscillator Crystal

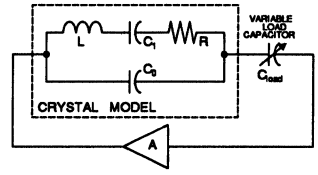


Figure A3. - Equivalent Circuit of Oscillator

Figure A3 shows an equivalent representation of the oscillator circuit. The variable load capacitor is internal to the CS61534. The value of this capacitor is controlled by logic internal to the CS61534. Based on this model, equations 1 and 2 have been developed to help calculate the required crystal parameters necessary to meet system requirements.

CS61534. Based on this model, equations 1 and 2 have been developed to help calculate the required crystal parameters necessary to meet system requirements.

Two important parameters in this model are the upper and lower bounds of C_{load} (the variable load capacitor) and the value of C_O. C_O can be used to control the series resonant frequency of the crystal. The minimum value of C_{load} sets the maximum parallel resonant frequency. Together, C_O and C_{load} can be used to set the pull range of the oscillator and its maximum and minimum frequencies.

Determining Required Pull Range

Four factors contribute to the required pull range of the crystal:

1) The frequency range required for the application,
2) The frequency drift of the crystal over the operating temperature range,
3) The variability in load capacitance from IC to IC,
4) The accuracy to which the crystal can be manufactured.

All of these factors have been measured or can be controlled.

Frequency Tolerance / C_L in pf	T1 6.176000 MHz ±130 ppm or less	CEPT 8.192000 MHz ±50 ppm or less
$C_{low\ freq}$ min 34.0	6175197 - Δtd	8191590 - Δtd
$C_{high\ freq}$ max 11.7	6176803 + Δtd	8192410 + Δtd
MAXIMUM ALLOWABLE PULL RANGE	390 ppm	230 ppm

Δ_{td} = crystal temperature drift from -40 to +85 deg. C.

Table A1. - T1 and CEPT Requirement

For a given crystal geometry, the series resonant frequency of the crystal is inversely proportional to C_O. The relationship of the crystal's series resonant frequency to its parallel resonant frequency in the oscillator circuit determines the pull range of the oscillator. The further away the series resonant frequency is from the parallel resonant frequency (which is set by the load condition in the oscillator circuit) the greater the pull range of the crystal. That is: a smaller C_O (greater series resonant frequency) results in less pull range, while the larger the C_O (lower series resonant frequency), the greater the pull range.

The series resonant frequency of the crystal is calculated by Equation 1.

$$f_S = f_N - \frac{\Delta f}{2(C_L-C_H)}(C_L+C_H+2C_O) \qquad [C's\ in\ pF] \quad (1)$$

f_S = series resonant frequency of crystal

f_N = 4 * Nominal Signal Frequency
- should be 6.176000 MHz for North America (T1)
- should be 8.192000MHz for Europe (CCITT)

Δf = required pull range of crystal in Hz (Δppm*f_N)

C_L = load capacitance for low frequency oscillation (average is ~38.0 pF)

C_H = load capacitance for high frequency oscillation (average is ~10.5 pF)

The parallel resonant frequency is calculated by Equation 2.

$$f_{load} = f_S\left(\frac{C_1+C_{load}+C_O}{C_{load}+C_O}\right)^{1/2} \quad (2)$$

Table A1 shows the crystal frequency as a function of load capacitance. The deviation in frequency from the nominal is shown in ppm. Temperature drift has been accounted for as shown. *The accuracy to which C_O can be controlled, and the accuracy to which a crystal can be trained or calibrated should be factored in to guarantee that the required frequency range will be met.*

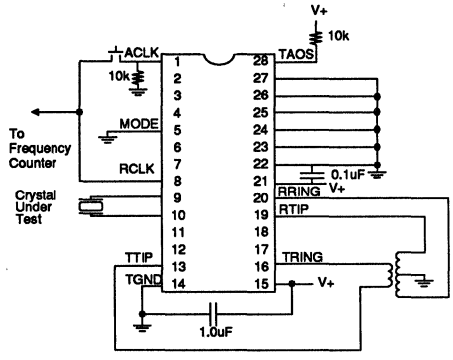


Figure A4. - Crystal Pull Range Test

The setup shown in Figure A4 can be used to test crystals. When no ACLK signal is applied to the device, the oscillator will tend to pull to one extreme of its pull range. Momentarily pressing the push button moves the relative positions of the FIFO pointers and if the write pointer stops (when the push button opens) in the right relationship to the read pointer, the oscillator will pull to the other end of its range. It may take a few tries.

Transformers

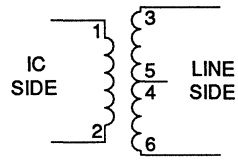
Transformers listed in Table A2 have been found to be suitable for use with the CS61534.

Manufacturer	Part #
Pulse Engineering	5764
Pulse Engineering	FAL 1.0
Pulse Engineering	FAL 4.1
Schott Corp.	67112060
Bell Fuse	0553-5006-IC
Nova Magnetics	6500-07-011
Midcom	671-5832

Note: The Pulse Eng. 1682x is still acceptable, but the other Pulse Engineering transformers are preferred.

Table A2. - Suitable Transformers

Figure A5 shows the connections for some of the recommended transformers for the transmitter.



Bell Fuse 0553-5006-IC
Schott Corp. 67112060
Pulse Engineering 5764 & FAL 1.0

Figure A5.- Some Recommended Transmitter/Transformer Connections

Key transmit transformer specifications are:

Turns ratio: 1:2 (or 1:1:1) ± 5%,
Primary inductance: 600 µH min measured at 10kHz and 0.005 VRMS.
Leakage inductance: 1.3 µH max with secondary shorted.
Interwinding capacitance: 23 pF max, primary to secondary

To save on power consumption under normal operating conditions, the output drivers are powered down during the transmission of a space (zero) on to the line. Approximately one quarter cycle prior to transmitting a mark (one), the drivers are enabled. The transformer, interacting with the driver, can cause a slight voltage difference (<200 mV) between the driven zero and the non-driven zero. We recommend that this effect be eliminated by inserting a ≥0.2uF non-polarized capacitor in series with the primary of the transmit transformer. Consult the factory for more information.

Receive Side Jitter Attenuation

In some applications it is desirable to attenuate jitter from the received signal. A CS61600 PCM jitter attenuator can be used to remove at least seven unit intervals of jitter from the recovered clock and data as shown in Figure A6. In the host mode, the inverter is not needed if CLKE is high.

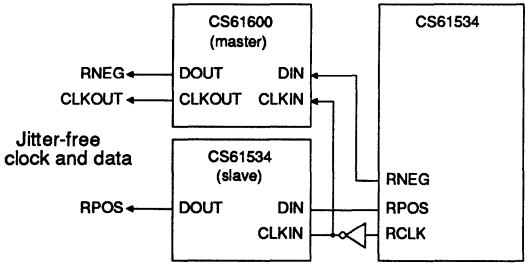


Figure A6 - Receive Jitter Attenuation

Applicable Systems

Figure A7 shows a T1 span from a customer premises location through a TELCO DSX-1 cross connect. As shown in Figure A7, the CS61534 is applicable in customer premises systems that interconnect to a channel service unit (CSU), and in network equipment that connects to a DSX-1 cross connect.

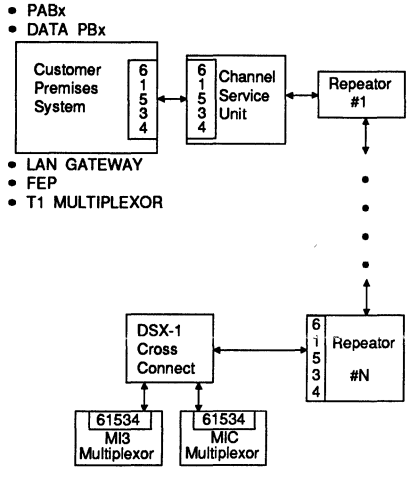


Figure A7. - Application of CS61534

Interfacing The CS61534 With T1 Digital Transceivers

This section gives general guidance on how to interface the CS61534 with digital T1 framing and signaling transceivers such as the R8070, and DS2180. Design attention must be given to insure that the devices are properly interfaced. To interface with the R8070, connect the devices as shown in Figure A8. The CS61534 is shown in the hardware mode.

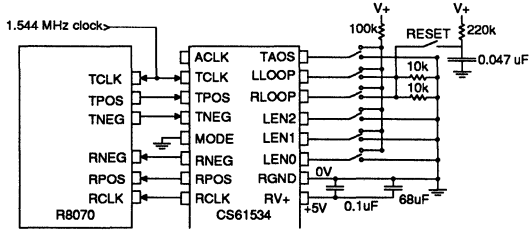


Figure A8. - Interfacing the CS61534 with and R8070

To interface with the DS2180, connect the devices as shown in Figure A9. In this case, the CS61534 and DS2180 are in host mode controlled by a microprocessor serial interface. If the CS61534 is used in hardware mode, then the CS61534 RCLK output must be inverted before being input to the DS2180.

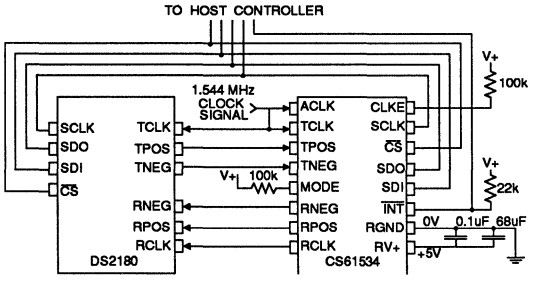


Figure A9. - Interfacing the CS61534 with a DS2180

CS61574 Compatibility

See the application note: "*CS61534 Design Guidelines to Insure Compatibilty with CS61574*".

Semiconductor Corporation

CS61544

T1 Line Interface

Features

- Provides Analog T1 Line Interface
- Fully Compatible with T.A. #34, Publication 43802 & TR-TSY-000009
- Programmable Pulse-Shaping Line Driver
- Performs Data and Timing Recovery
- Implements ISDN Primary Rate and DMI Interface
- Diagnostic and Performance Monitoring Features
- Selectable B8ZS Encode/Decode
- Jitter Attenuator
- 3 Micron CMOS for High Reliability

General Description

The CS61544 combines the analog transmit and receive line interface functions for a T1 system interface in one 28 pin device. The T1 line interface operates from a single 5V supply, is transparent to the T1 framing format, and can work with ABAM and other cable types. Crystal's SMART ANALOG™ circuitry shapes the transmit pulse internally, providing the appropriate pulse shape at the DSX-1 cross-connect for line lengths ranging from 0 to 655 feet. Maximum range is greater than 1500 feet. The transmitter uses an elastic store to remove jitter from the outgoing data prior to transmission.

Applications

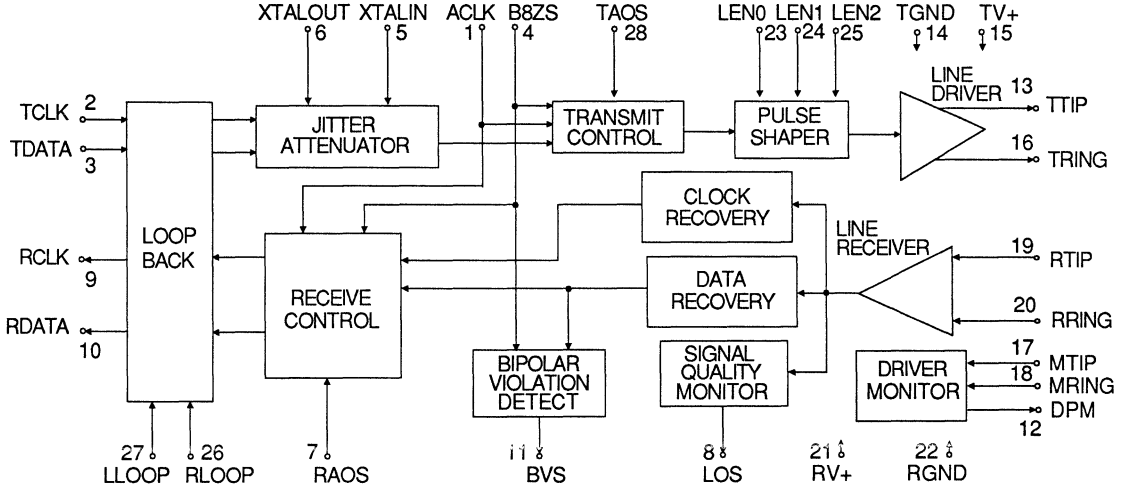
- Interfacing Network Equipment such as Multiplexors, Channel Banks and Switching Systems to a DSX-1 Cross Connect
- Interfacing Customer Premises Equipment such as PABXs, T1 Multiplexors, Data PBXs and LAN Gateways to a Channel Service Unit, or T1 modem.

ORDERING INFORMATION

CS61544-IP - 28 Pin Plastic DIP
CS61544-ID - 28 Pin Cerdip
CS61544-IL - 28 Pin PLCC (j-leads)

2

Block Diagram



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, Texas 78760
(512)445-7222 TWX:910-874-1352

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply (referenced to GND)	RV+, TV+	-	6.0	V
Input Voltage, Any Pin (note 1)	V_{in}	RGND-0.3	RV+ + 0.3	V
Input Current, Any Pin (note 1 & 2)	I_{in}	-	10	mA
Ambient Operating Temperature	T_A	-40	85	°C
Storage Temperature	T_{stg}	-65	150	°C

Notes: 1. Excluding RTIP and RRING.
2. Transient currents of up to 100 mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply (note 3)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature	T_A	-40	25	85	°C
Total Power Dissipation (note 4) 100% ones density & max. line length @ 5.25 V	P_D	-	-	760	mW

Notes: 3. TV+ must not exceed RV+ by more than 0.3V.
4. Power dissipation while driving 25Ω load, over operating temperature range. Includes CS61544 and load.

DIGITAL CHARACTERISTICS (T_A = -40 °C to 85 °C; V+ = 5.0V ± 5%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage PINS 1-5, 7, 23 - 28	V_{IH}	2.0	-	-	V
Low-Level Input Voltage PINS 1-5, 7, 23 - 28	V_{IL}	-	-	0.8	V
High-Level Output Voltage (note 5) I_{OUT}=-40 uA PINS 6, 8 - 12	V_{OH}	2.4	-	-	V
Low-Level Output Voltage (note 5) I_{OUT}= 1.6 mA PINS 6, 8 - 12	V_{OL}	-	-	0.4	V
Input Leakage Current		-	-	±10	uA

Note: 5. Output drivers will output CMOS logic levels into a CMOS load.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (T_A = -40°C to +85°C; V+ = 5.0V ±5%; GND = 0V)

Parameters	Min	Typ	Max	Units
AMI Output Pulse Amplitudes Measured at the DSX	2.4	3.0	3.6	V_{0-p}
Load Presented to Transmitter Output (note 6)	-	25	-	ohms
Input Jitter Tolerance-Transmitter	7.0	-	-	Unit Intervals
Jitter Attenuation Curve Corner Frequency (note 7)	-	50	-	Hz
Loss of Signal Threshold	-	0.5	-	V
Receiver Sensitivity Below DSX-1 (2.4V)	-10	-	-	dB

Notes: 6. On the CS61544 side of the 2:1 transformer, line is 100Ω.
7. Crystal pull range: ± 200 ppm. Five unit intervals of input jitter. Slope above corner frequency is -20dB/decade. See Figure 5.

SWITCHING CHARACTERISTICS (T_A = -40°C to +85°C; V+ = 5.0V ±5%; GND = 0V; Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter	Symbol	Min	Typ	Max	Units
Crystal Frequency (note 8)	f_c	-	6.176000	-	MHz
TCLK Frequency	f_{in}	-	1.544	-	MHz
ACLK Frequency (note 9)	f_{out}	-	1.544	-	MHz
RCLK Pulse Width	t_{pwh}	-	324	-	ns
(note 10)	t_{pwl}	-	324	-	ns
Duty Cycle (note 11)		-	50	-	%
Rise Time, All Digital Outputs (note 12)	t_r	-	-	100	ns
Fall Time, All Digital Outputs (note 12)	t_f	-	-	100	ns
TDATA to TCLK Falling Setup Time	t_{su}	25	-	-	ns
TCLK Falling to TDATA Hold Time	t_h	25	-	-	ns
RDATA to RCLK Rising Setup Time	t_{su}	-	274	-	ns
RCLK Rising to RDATA Hold Time	t_h	-	274	-	ns
Reset Pulse Duration		0.2	-	2000	us

Notes: 8. Crystal must meet specifications described in Applications section of this data sheet.
9. ACLK provided by an external source or TCLK.
10. The sum of the pulse widths must always meet the frequency specifications.
11. Duty cycle is $(t_{pwh} / (t_{pwh}+t_{pwl}))*100\%$.
12. At maximum load of 1.6mA and 50pF.

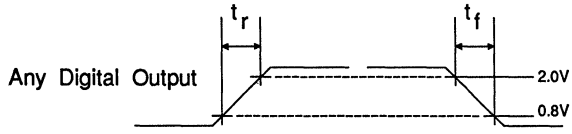


Figure 1 - Signal Rise and Fall Characteristics

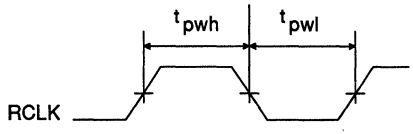


Figure 2 - Clock Signal Quality

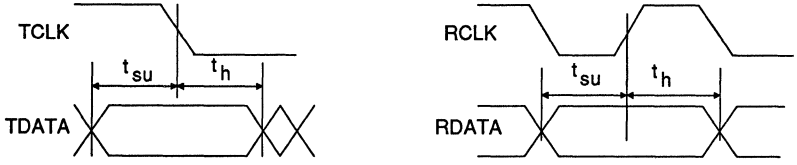


Figure 3 - Switching Characteristics

Note that when externally looping RCLK back into TCLK, RCLK must be inverted.

THEORY OF OPERATION

Transmitter

The transmitter takes binary (unipolar) data from a T1 terminal and produces alternate bipolar pulses of appropriate shape. The transmit clock and transmit data (TCLK, TDATA) are supplied synchronously. Data is sampled on the falling edge of the input clock.

Line lengths from 0 to 655 feet (as measured from the CS61544 to the DSX-1 cross connect) are selectable. Pulse shaping and signal level are determined by "line length select" inputs and require no external circuitry. Pulse shaping is accomplished with a slew rate controlled fast digital to analog converter. Alternate mark inversion operation is implemented by driving the line in a true differential manner. In order to achieve the necessary line voltages, which exceed the 5 volt supply, a two-to-one, step-up transformer is required. The line driver drives a 25Ω equivalent load.

To place the device in a low power dissipation mode (i.e., to disable the drive), the B8ZS and TDATA should be held low while TCLK continues to be input. When any transmit control pin (TAOS, LEN0, LEN1, LEN2, LLOOP, or RLOOP) is toggled, the transmitter stabilizes within 16 bit periods.

B8ZS coding can be inserted into the data stream using the B8ZS select feature. This feature replaces every string of eight consecutive zeros with a pulse train containing bipolar violations. The violations can then be decoded at the receive end and the original data recovered.

Transmit Line Length Selection

Line length selection can be controlled by an intelligent controller or hard-wired with a switch which is set at the time of installation. The line length selection supports both a three-partition arrangement for ICOT and MAT cable, and a five-partition arrangement for ABAM and PIC cable as shown in Table 1. For each line length selected, the CS61544 modifies the output pulse to meet the requirements of Technical Advisory 34 and TR-TSY-000009. A typical output pulse is shown in Figure 4.

2

Table 1 - Line Length Selection

LEN2	LEN1	LEN0	LINE LENGTH SELECTED (FEET)	CABLE TYPE
0	0	0	0-220	MAT and ICOT
0	0	1	220-440	
0	1	0	440-655	
0	1	1	0-133	ABAM and PIC
1	0	0	133-266	
1	0	1	266-399	
1	1	0	399-533	
1	1	1	533-655	

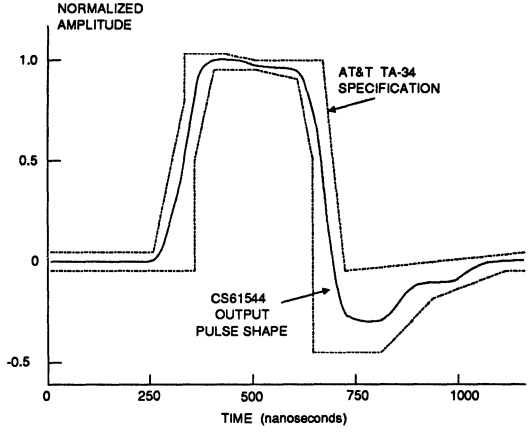


Figure 4 - Typical Pulse Shape at DSX-1 Cross Connect

Transmit Jitter Attenuator

The 61544 will tolerate and attenuate at least seven unit intervals of jitter (peak-to-peak) from a T1 signal. Figure 5 shows a family of curves which show the jitter attenuation achieved by the 61544. Each curve shows the jitter attenuation for a signal with constant jitter amplitude over a range of jitter frequencies. The more jitter a signal has, the more the jitter is attenuated. The jitter attenuator on the transmitter side meets the jitter attenuation and input tolerance specifications of AT&T Publication 43802, as shown in Figures 6 and 7.

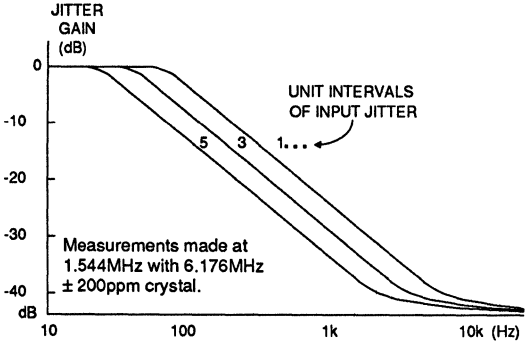


Figure 5 - CS61544 Jitter Attenuation Curves

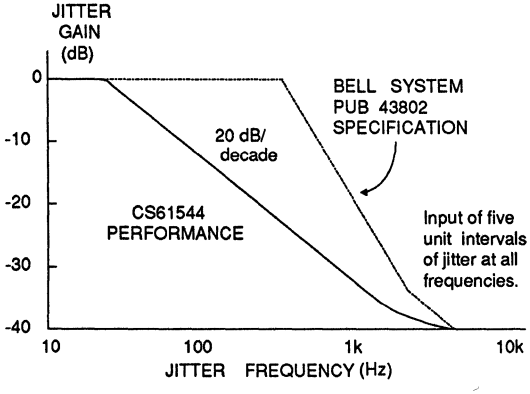


Figure 6 - Jitter Attenuation Characteristics

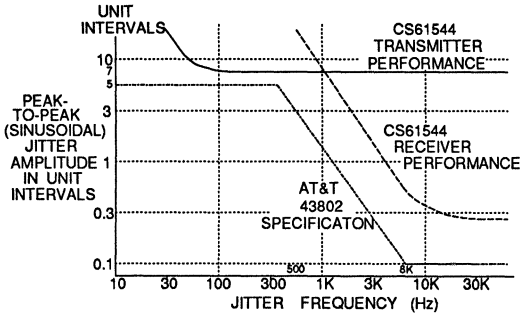


Figure 7 - Input Jitter Tolerance of Transmitter and Receiver

Jitter attenuation is accomplished by means of a 16 bit FIFO and a variable oscillator. The frequency of the variable oscillator is controlled by logic in the CS61544 to be the same as the average input clock signal, TCLK. TCLK controlls the write pointer of the FIFO. Data present on TDATA is written into the memory location selected by the write pointer. The read pointer of the FIFO, and the transmit frequency of the device, are determined by the crystal oscillator. Internal logic tracks the relative positions of the FIFO's pointers, and adjusts the oscillator's load capacitance to maintain the FIFO in a half full condition (read and write pointers kept 8 bits apart). Slow changes in input signal frequency are tracked, while high frequency variations in the TCLK signal are absorbed by the FIFO.

The external reference crystal used by the jitter attenuator should have a nominal frequency of 6.176 MHz, and have a pull range, in the oscillator circuit, that is sufficient to meet the frequency tolerance requirements specified for the system. Furthermore, the frequency tolerance must be met over all operating temperatures. The jitter attenuator can be disabled by driving XTALIN with a clock which is exactly four times the TCLK frequency.

Transmit All Ones Select

The transmitter provides for all ones insertion at the frequency of the alternate clock input, ACLK. (The transmit clock can be used as the alternate clock by connecting pins 1 and 2 together). Transmit all ones is selected when TAOS goes high, and causes continuous ones to be transmitted on the line (TTIP and TRING) using the alternate clock. The TDATA and TCLK inputs are ignored. If Remote Loopback is in effect, any TAOS request will be ignored.

Receiver

The receiver extracts data and clock from an AMI (Alternate Mark Inversion) coded signal and outputs clock and synchronized data. The receiver is sensitive to signals over the entire range of cable lengths and requires no equalization or ALBO (Automatic Line Build Out) circuits. The signal is received on both ends of a center-tapped, center-grounded transformer. The transformer is center tapped on the CS61544 side. Data on RDATA is stable and may be sampled on the rising edge of the recovered clock, RCLK. The clock and data recovery circuit meets or exceeds the jitter tolerance specifications of Publication 43802.

The two leads of the receiver transformer have opposite polarity and drive the receiver inputs RTIP and RRING differentially. Comparators detect pulses on RTIP and RRING. The comparator thresholds are dynamically established by peak detectors.

Clock recovery is achieved through a frequency and phase lock loop (FPLL). Upon power up and reset of the CS61544, and prior to the start of clock acquisition, the FPLL has its center frequency trained. A current controlled oscillator (ICO) is trained relative to the crystal oscillator frequency reference. The current is adjusted until it is just sufficient to change a fixed capacitor to a fixed reference voltage in a half period of the reference clock. This current is then held constant. The FPLL is controlled, small signal, by the output of the phase detector and loop filter, which takes the form of a current. This is added to the fixed current to modulate the ICO about the center frequency and close the loop. This training limits the lock range of the FPLL to ± 6% of the trained frequency (1.544 MHz), guaranteeing that the FPLL is immune to false lock. The FPLL is insensitive to variations in temperature and slight variations in power supply voltage, but fairly large changes in power supply voltage will change the control current in the FPLL, reducing its effectiveness.

The received signal is monitored to detect bipolar violations. If a bipolar violation is detected, a positive strobe (BVS) is output with a width of one half the clock period.

The receiver has the capability to decode signals which have been transmitted with B8ZS bipolar violations. This feature is enabled when B8ZS (pin 4) goes high. Recovered data is processed by B8ZS decode (if enabled) and sent to the output. The bipolar violation detection algorithm is also modified to not detect the B8ZS encoded violation as an error.

Loss of Signal

The receiver reports loss of the received signal on the Loss of Signal pin, LOS. The threshold for loss of signal is 0.5 volts. A loss of signal will be indicated within 200 bit periods if an active signal falls below the threshold. In the event that the input signal drops to zero volts, the loss of signal will be indicated within 32 bit periods. When a loss of signal is detected, RDATA is not valid, but the receiver will continue to try to recover data. LOS will return to a low state when a valid signal returns to RTIP and RRING. RCLK is always output, but may drift up to ± 6% from 1.544 MHz.

Receive All Ones Select

Receive all ones is selected when RAOS goes high. If receive all ones is selected when the local loopback is not in effect, continuous ones are sent to RDATA using the alternate clock, ACLK, for timing. The alternate clock, ACLK, is sent to RCLK. (The transmit clock, TCLK, can be used as the alternate clock by connecting pins 1 and 2 together.) If it is desirable to have all ones automatically replace recovered data (at RDATA) upon loss of signal, then RAOS and LOS should be tied together (pins 7 and 8).

Local Loopback

The local loopback mode bypasses the receive circuit and routes the digital transmit clock and data to the receive clock and data pins. A local loopback occurs in response to LLOOP going high. Any RAOS request is overridden (see Table 2). The transmit clock and data signals, TCLK and TDATA are sent out on the line through TTIP and TRING unless transmit all ones, TAOS, is selected, in which case continuous ones are transmitted on the line at the rate determined by ACLK.

Table 2 - Interaction of LLOOP and RAOS

LLOOP Input Signal	RAOS Input Signal	Source of Data for RDATA	Source of Clock for RCLOCK
0	0	RTIP & RRING	RTIP & RRING
0	1	all 1s	ACLK
1	X	TDATA	TCLK

Remote Loopback

In remote loopback, the recovered clock and data input on RTIP and RRING are sent through the elastic store to remove jitter, and back out on the line via TTIP and TRING. Selecting remote loopback overrides any TAOS request (see Table 3). The recovered incoming signals are also sent to RCLK and RDATA unless receive all ones (RAOS) is selected, in which case continuous ones and an alternate clock are sent to RCLK and RDATA. Remote loopback occurs in response to RLOOP going high. Simultaneous selection of local and remote loopback modes is not valid (see *Reset*).

Table 3 - Interaction of RLOOP and TAOS

RLOOP Input Signal	TAOS Input Signal	Source of Data for TTIP & TRING	Source of Clock for TTIP & TRING
0	0	TDATA	TCLK
0	1	all 1s	ACLK
1	X	RTIP & RRING	RTIP & RRING

Notes:
1. X - Don't care. The identified All Ones Select input is ignored when the indicated loopback is in effect.
2. Logic 1 indicated that Loopback or All Ones option is selected.

Driver Performance Monitor

To aid in early detection and easy isolation of nonfunctioning T1 links, the CS61544 is able to monitor transmit drive performance and report when the driver is no longer operational. This feature can be used to monitor either the device's performance or the performance of a neighboring CS61544. The driver performance monitor indicator is normally at a low (zero) logic level, and goes to high level upon detecting driver failure.

The driver performance monitor consists of a receiver that monitors the transmitted signal on input pins, MTIP and MRING. If no signal is present on MTIP and MRING for 32 clock cycles, the DPM pin goes high.

Whenever more than one CS61544 reside on the same circuit board, the effectiveness of the driver

performance monitor can be maximized by having each CS61544 monitor performance of a neighboring CS61544 device, rather than having it monitor its own performance.

Reset

The CS61544 initiates internal reset procedures either upon power up or in response to a reset request. After initial power up, the device will delay for 10 ms after the oscillator starts to allow the power supply and the oscillator to stablize before initiating the training proceedure for the FPLL. Training the FPLL takes at most 43 ms, but typically requires less than half that ammount of time. If the power supply has not reached stable operating voltage within 10 ms, the device should be reset after the power supply has stablized. These conditions should also be adhered to if temporary loss of power supply occurs.

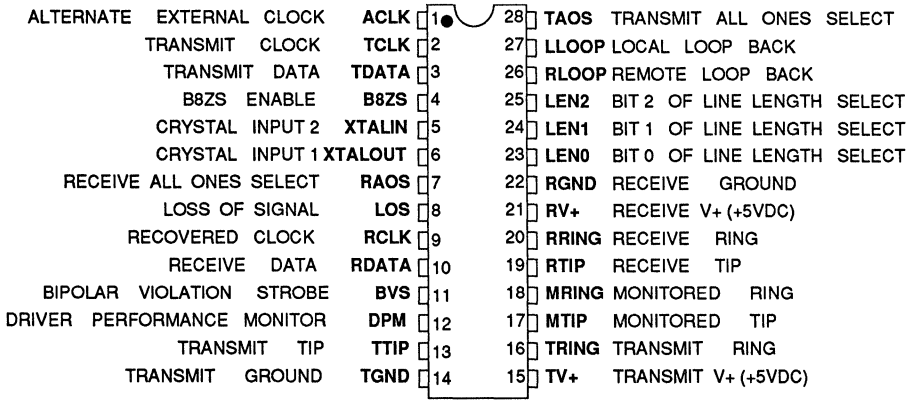
A reset request is made by simultaneously setting both RLOOP and LLOOP high for a period not to exceed 2 ms. Reset will be completed within 53 ms after the falling edge of the reset request (falling edge of RLOOP and LLOOP).

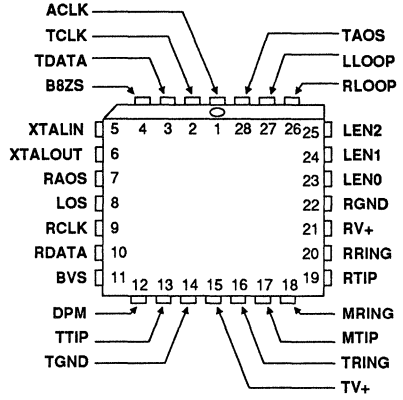
During the reset procedure, the loss of signal indicator is high. Once the reset procedures are completed, the loss of signal indicator goes low, signifying that normal operation of the device has begun.

Power Supply

The device operates from a single 5 volt supply. Separate pins for transmit and receive supplies provide internal isolation. However these pins may be connected externally with no impact on device performance, provided the power supply pins are decoupled to their respective grounds. The receive power supply should be decoupled from ground with a 68 µF tantalum, (or better), capacitor, and a mylar or ceramic 0.1 µF capacitor. A 1.0 µF mylar or ceramic capacitor should be used on the transmit power supply. These capacitors should be located physically close to the device. TV+ must not exceed RV+ by more than 0.3V.

PIN DESCRIPTIONS





Power Supplies

TV+ - Positive Power Supply, Transmit Drivers, Pin 15.

Positive power supply for the transmit drivers; typically +5 volts. TV+ must not exceed RV+ by more than 0.3V.

TGND - Ground, Transmit Drivers, Pin 14.

Power supply ground for the transmit drivers; typically 0 volts.

RV+ - Positive Power Supply, Pin 21.

Positive power supply for the device, except transmit drivers; typically +5 volts.

RGND - Ground, Pin 22.

Power supply ground for the device, except transmit drivers; typically 0 volts.

Oscillator

XTALIN, XTALOUT - Crystal Inputs, Pins 5 and 6.

A 6.176 MHz crystal should be connected across these pins. An externally generated 6.176 MHz clock signal may be put into the XTALIN pin, disabling the jitter attenuator. This clock must be *exactly* four times the frequency at TCLK. See the applications section for more information on crystals.

Control

B8ZS - B8ZS Encoding Enable, Pin 4.

Setting B8ZS to a logic 1 enables B8ZS encoding of the transmit data and B8ZS decoding of the receive data.

RAOS - Receive All Ones Select, Pin 7.

Setting RAOS to a logic 1 causes continuous ones to be sent to RDATA at the frequency determined by ACLK.

TAOS - Transmit All Ones Select, Pin 28.

Setting TAOS to a logic 1 causes continuous ones to be transmitted at the frequency determined by ACLK.

LLOOP - Local Loopback, Pin 27.

Setting LLOOP to a logic 1 routes the transmit clock and data to the receive clock and data pins, bypassing the receive circuit. Any RAOS request is ignored. TCLK and TDATA are still transmitted unless overridden by a TAOS request.

RLOOP - Remote Loopback, Pin 26.

Setting RLOOP to a logic 1 causes the recovered clock and data to be sent through the jitter attenuator and through the driver back to the line. The recovered signal is also sent to RCLK and RDATA unless overridden by a RAOS request. Any TAOS request is ignored. If the oscillator is being driven with a 4X clock, the remote loopback function is not possible.

Simultaneously taking RLOOP and LLOOP high for less than 2 ms initiates a device reset.

LEN0, LEN1, LEN2 - Line Length Selection, Pins 23, 24 and 25.

Determines the shape and amplitude of the transmitted pulse to accomodate several cable types and lengths. See Table 1 for information on line length selection.

Inputs

ACLK - Alternate External Clock, Pin 1.

This input should be tied to TCLK or some other externally generated 1.544 MHz clock. The frequency of ACLK determines the rate at which TAOS and RAOS are output.

TCLK, TDATA - Transmit Clock, Transmit Data, Pins 2 and 3.

Inputs for clock and data to be transmitted. Signal jitter is attenuated and the signal is driven on to the line through TTIP and TRING. TDATA is sampled on the falling edge of TCLK.

RTIP, RRING - Receive Tip, Receive Ring, Pins 19 and 20.

The receive AMI signal is input to these pins. A center-tapped, center-grounded, 2:1, step-up transformer is required on these inputs, as shown in Figure A3. Data and clock are recovered and output on RDATA and RCLK.

MTIP, MRING - Monitored Tip, Monitored Ring, Pins 17 and 18.

These pins are normally connected to TTIP and TRING and monitor the output of a CS61544. If the monitors are not used, tying MTIP low and MRING high through a resistor will reduce power consumption slightly.

Outputs

RCLK, RDATA - Recovered Clock, Receive Data, Pins 9 and 10.

Data and clock are recovered from the RTIP and RRING inputs and output at these pins. RDATA is valid on the rising edge of RCLK.

TTIP, TRING - Transmit Tip, Transmit Ring, Pins 13 and 16.

The AMI, T1 signal is driven to the line through these pins. This output is designed to drive a 25Ω load. A 2:1 step-up transformer is required to drive the line as shown in Figure A1.

Status

LOS - Loss of Signal, Pin 8.

LOS goes to a logic 1 when the received signal falls below a 0.5 volt threshold, or after 32 clock cycles with out a detected one. LOS returns to logic 0 when the signal returns.

BVS - Bipolar Violation Strobe, Pin 11.

BVS goes to a logic 1 when a bipolar violation is detected in the received signal. The strobe is approximatly 324 ns wide and aligned with the rising edge of RCLK. The strobe will occur concurrently with the RDATA output for which the violation was detected. The bipolar violation detection algorithm is modified when B8ZS is selected to accept B8ZS encoded data.

DPM - Driver Performance Monitor, Pin 12.

If no signal is present on MTIP and MRING for 32 clock cycles, DPM goes to a logic 1 until the first detected signal.

APPLICATIONS

Selecting an Oscillator Crystal

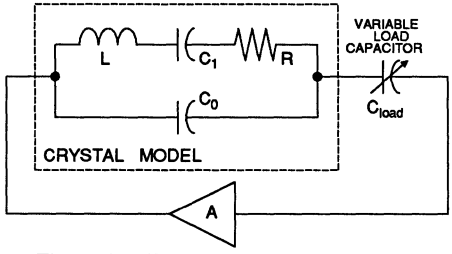


Figure A1 - Equivalent Circuit Oscillator

Figure A1 shows an equivalent representation of the oscillator circuit. The variable load capacitor is internal to the CS61544. The value of this capacitor is controlled by logic internal to the CS61544. Based on this model, equations 1 and 2 have been developed to help calculate the required crystal parameters necessary to meet system requirements.

Three important parameters in this model are the upper and lower bounds of C_{load} (the variable load capacitor) and the values of C_0 and C_1. C_0 can be used to control the series resonant frequency of the crystal. With respect to the parallel resonant frequency for a given load, the minimum value of C_{load} sets the maximum parallel resonant frequency. Together, C_0 C_1 and C_{load} can be used to set the pull range of the oscillator and its maximum and minimum frequencies.

Determining Required Pull Range

Four factors contribute to the required pull range of the crystal:

1) The frequency range required for the application,
2) The frequency drift of the crystal over the operating temperature range,
3) The variability in load capacitance from IC to IC,
4) The accuracy to which the crystal can be manufactured.

All of these factors have been measured or can be controlled to some extent.

For a given crystal geometry, the series resonant frequency of the crystal is inversely proportional to C_0, and directly proportional to C_1. The relationship of the crystal's series resonant frequency to its parallel resonant frequency in the oscillator circuit determines the pull range of the oscillator. The further away the series resonant frequency is from the parallel resonant frequency (which is set by the load condition in the oscillator circuit) the greater the pull range of the crystal. That is: a larger C_1 (smaller C_0 and greater series resonant frequency) results in less pull range, while the smaller the C_1 (larger C_0, and lower series resonant frequency), the larger the pull range.

The series resonant frequency of the crystal is2 calculated by Equation 1.

$$f_S = f_N - \frac{\Delta f}{2(C_L - C_H)}(C_L + C_H + 2C_0) \qquad (C\text{'s in pF}) \qquad (1)$$

f_S = series resonant frequency of crystal
f_N = 4 * Nominal Signal Frequency
- should be 6.176000 MHz for North America (T1)
Δf = required pull range of crystal in Hz (Δppm*f_N)
C_L = load capacitance for low frequency oscillation
(average is ~38.0 pF)
C_H = load capacitance for high frequency oscillation
(average is ~10.5 pF)

The parallel resonant frequency is calculated by Equation 2.

$$f_{load} = f_S \left(\frac{C_1 + C_{load} + C_0}{C_{load} + C_0} \right)^{1/2} \qquad (2)$$

Table A1 shows the crystal frequency as a function of load capacitance. The deviation in frequency from the nominal is shown in ppm.

Frequency Tolerance / C_L in pf	T1 6.176000 MHz ±130 ppm or less
$C_{low\ freq}$ min 34.0	6175197 - Δ_{td}
$C_{high\ freq}$ max 11.7	6176803 + Δ_{td}
MAXIMUM ALLOWABLE PULL RANGE	390 ppm

Δ_{td} = crystal temperature drift from -40 to +85 deg. C.

Table A1 - T1 Crystal Frequency

Temperature drift has been accounted for as shown. *The accuracy to which C_O can be controlled, and the accuracy to which a crystal can be trained or calibrated should be factored in to guarantee that the required frequency range will be met.*

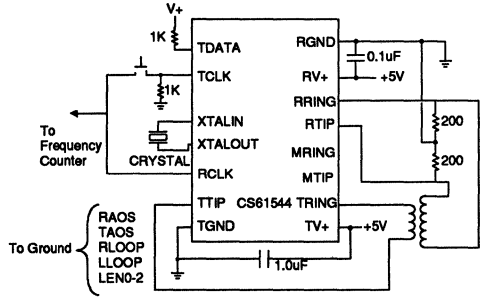


Figure A2 - Crystal Pull Range Test

The setup shown in Figure A2 can be used to test crystals. When no TCLK signal is applied to the device, the oscillator will tend to pull to one extreme of its pull range. Momentarily pressing the push button moves the relative positions of the FIFO pointers and if the write pointer stops (when the push button opens) in the right relationship to the read pointer, the oscillator will pull to the other end of its range. It may take a few tries.

General Applications

Figure A3 shows the typical configuration for the CS61544, including transmit and receive transformers. The receiver transformer is center tapped and center grounded with 200Ω resistors between the center tap and each leg on the CS61544 side. These resistors provide the 100Ω termination for the T1 line. Line Length Select pins are shown in a manual switching configuration. These inputs can be controlled by logic circuitry if desired.

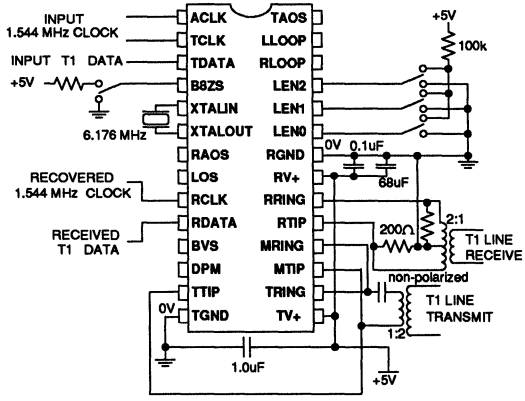


Figure A3 - Typical Configuration Showing Line Interface

Decoupling

Decoupling and filtering of the power supplies is crucial for proper operation of the analog sections in the transmit and receive paths. If different power and ground busses supply the transmitter and receiver supply inputs, a 68 µF capacitor should be added to the transmit supply. The decoupling capacitors shown in Figure A3 should be high grade capacitors, (i.e., 68 µF - tantalum or better; 1.0 and 0.1 µF - mylar or ceramic), and should be located as close as pos-

sible to the power supply pins of the chip. Wire wrap bread-boarding of the CS61544 is not recommended because lead resistance and wrap inductance serve to defeat the function of the decoupling capacitors.

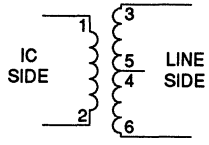
Transformers

Manufacturer	Part #
Pulse Engineering	5764
Pulse Engineering	FAL 1.0
Pulse Engineering	FAL 4.1
Schott Corp.	67112060
Bell Fuse	0553-5006-IC
Nova Magnetics	6500-07-011
Midcom	671-5832

Note: The Pulse Eng. 1682x is still acceptable, but the other Pulse Engineering transformers are preferred.

Table A2 - Suitable Transformers

Transformers listed in Table A2 have been found to be suitable for use with the CS61544. Figure A4 shows the connections for some of the transformers mentioned in the Table A2. The transformers should be placed physically close to the CS61544.



Bell Fuse 0553-5006-IC
Schott Corp. 67112060
Pulse Engineering 5764 & FAL 1.0

Figure A4 - Transmitter Transformer Configuration

To save on power consumption under normal operating conditions, the output drivers are powered down during the transmission of a space (zero) on to the line. Approximately one quarter cycle prior to transmitting a mark (one), the drivers are enabled. The transformer, interacting with the driver, can cause a slight voltage difference (<200 mV) between the driven zero and the non-driven zero. We recommend that this effect be eliminated by inserting a ≥0.2 uF non-polarized capacitor in series with the primary of the transformer. Contact the factory for more information.

Receive Side Jitter Attenuation

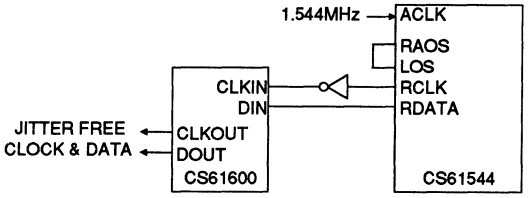


Figure A5 - Receiver Jitter Attenuation

In some applications it is desirable to attenuate jitter from the received signal. A CS61600 PCM jitter attenuator can be used to remove at least seven unit intervals of jitter from the recovered clock and data as shown in Figure A5.

Maintaining Recovered Clock

Figure A5 also shows how the recovered clock, RCLK, can be maintained within desired specifications in the event that the received AMI signal is lost. This design requires a locally generated 1.544 MHz clock whose frequency is within the required system specifications. This clock is input to the ACLK input of the CS61544. The loss of signal output, LOS, is connected to the receive all ones select input, RAOS.

If the AMI signal is lost, the LOS signal goes high, taking RAOS high, directing the CS61544 to output all ones at RDATA at the frequency determined by ACLK (i.e. RCLK = ACLK). The CS61600 will buffer any instantaneous phase or frequency change at the RCLK and RDATA

retaining clock integrity. This type of circuit is necessary since the frequency/phase lock loop in the CS61544 will drift about 6% when the AMI signal is lost.

If the receiver input returns, LOS goes low, deselecting RAOS, and returning the circuit to its normal operating status. It is important to note that LOS will go low as soon as a valid pulse is detected, which is before the receiver has locked onto the incoming signal. It is advisable to delay the transition from RAOS to the receiver output for a few milliseconds after LOS indicates receipt of signal.

Applicable Systems

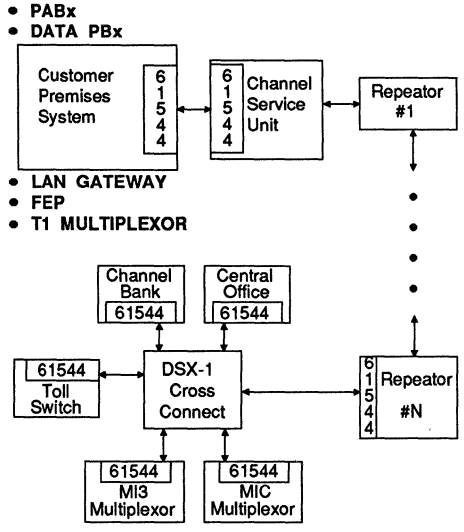


Figure A6 - Applicable Types of Connection

Figure A6 shows a T1 span from a customer premises location through a TELCO DSX-1 cross connect. As shown in Figure A6, the CS61544 is applicable in customer premises systems that interconnect to a channel service unit (CSU), and is applicable in network equipment that connects to a DSX-1 cross connect.

Interfacing The CS61544 With T1 Digital Transceivers

This section gives general guidance on how to interface the CS61544 with digital T1 framing and signaling transceivers such as the R8050, R8060, R8070, and DS2180. Design attention must be given to insuring that the devices are properly interfaced. For example, it may be necessary in invert clock signals to insure the accurate sampling of data. Connections required for interfacing Rockwell's R8050 and R8060 are shown in Figure A7.

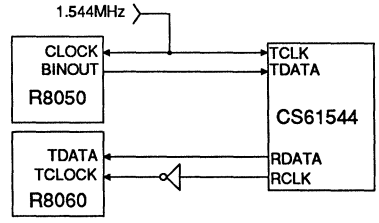


Figure A7 - Interfacing CS61544 with R8050 and R8060

To interface with the R8070, connect the devices as shown in Figure A8. When RPOS is strapped to RNEG, B8ZS encoding/decoding and bipolar violation detection processing is deactivated in the R8070. These functions are performed by the CS61544.

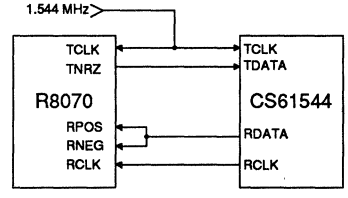


Figure A8 - Interfacing CS61544 with R8070

To interface with the DS2180, connect the devices as shown in Figure A9. When RPOS is tied to RNEG, B8ZS encoding/decoding and bipolar violation detection functions are performed by the CS61544.

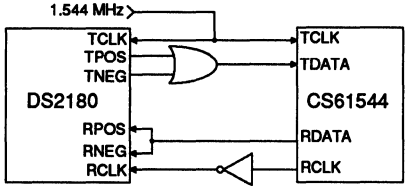


Figure A9 - Interfacing CS61544 with DS2180

Test and Evaluation of the CS61544

When connecting the receive clock and data, RCLK and RDATA, to the transmit clock and data, TCLK and TDATA, of the CS16544, be sure to invert the clock signal.

Transmitter or Receiver Function Only

If the CS61544 is used for transmit only, tie RTIP and RRING high through a resistor, ground RAOS, RLOOP, and LLOOP, and float the outputs. To configure the device for receive only, float TTIP, TRING, TV+ and TGND, ground TAOS, TCLK, TDATA, RLOOP, LLOOP and LEN0/1/2 .

• Notes •

Semiconductor Corporation

CS61574

PCM Line Interface

Features

- Provides Analog PCM Line Interface for T1 and 2.048 MHz Applications
- Provides Line Driver, and Data and Clock Recovery Functions
- Jitter Attenuation starting at 6 Hz with >300 UIs of tolerance in attenuator
- Jitter Tolerance of Receiver: 0.4 UIs to 100 kHz
- Microprocessor Controllable
- Compatible with CSUs and DACSs
- CS61534 Compatibility Mode
- Diagnostic Features

General Description

The CS61574 combines the analog transmit and receive line interface functions for a T1/CEPT interface in a 28 pin device. The line interface operates from a single 5 volt supply and is transparent to the framing format. Crystal's SMART ANALOG™ circuitry shapes the transmit pulse internally, providing the appropriate pulse shape for CSUs or for connecting to PCM crossconnects for line lengths ranging from 0 to 655 feet. Maximum range is greater than 1500 feet. The receiver uses an elastic store to remove jitter from the incoming data.

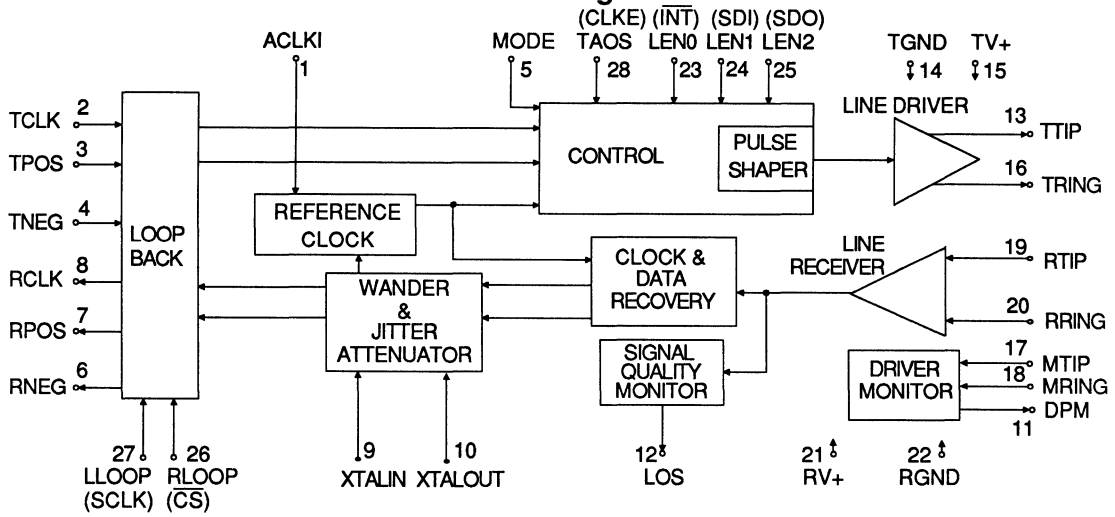
Applications

- Interfacing Network Equipment such as DACS and Channel Banks to a DSX-1 Cross Connect
- Interfacing Customer Premises Equipment to a CSU
- Building Channel Service Units

ORDERING INFORMATION

CS61574-IP - 28 Pin Plastic DIP; T1 only
CS61574-IP1 - 28 Pin Plastic DIP; T1 & CEPT
CS61574-IL - 28 Pin PLCC (j-leads);T1 only
CS61574-IL1 - 28 Pin PLCC (j-leads);T1 & CEPT

Block Diagram



Preliminary Product Information | *This document contains data for a new product. Crystal Semiconductor reserves the right to modify this product without notice.*

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, Texas 7876(
(512)445-7222 TWX:910-874-135(

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply (referenced to GND)	RV+, TV+	-	6.0	V
Input Voltage, Any Pin (Note 1)	V_{in}	RGND-0.3	RV+ + 0.3	V
Input Current, Any Pin (Note 2)	I_{in}	-10	10	mA
Ambient Operating Temperature	T_A	-40	85	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operations at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes: 1. Excluding RTIP, RRING, which must stay within -6V to RV + 0.3V.
2. Transient currents of up to 100 mA will not cause SCR latch-up. Also TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply (Note 3)	RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature	T_A	-40	25	85	°C
Total Power Dissipation (Note 4) 100% ones density & max. line length @ 5.25V	P_D	-	620	-	mW

Notes: 3. TV+ must not exceed RV+ by more than 0.3V.
4. Power dissipation while driving 25 Ω load over operating temperature range. Includes CS61574 and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.

DIGITAL CHARACTERISTICS (T_A = - 40 ° to 85 ° C, V+ = 5.0V ± 5%, GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (Notes 5, 6) PINS 1-5, 10, 23-28	V_{IH}	2.0	-	-	V
Low-Level Input Voltage (Notes 5, 6) PINS 1-5, 10, 23-28	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Notes 5, 6) I_{OUT}=-40 uA PINS 6-8, 11, 12, 23, 25	V_{OH}	2.4	-	-	V
Low-Level Output Voltage (Notes 5, 6) I_{OUT}= 1.6 mA PINS 6-8, 11, 12, 23, 25	V_{OL}	-	-	0.4	V
Input Leakage Current		-10	-	+10	uA
Three-State Leakage Current PIN 25 (Note 5)		-10	-	+10	uA

Notes: 5. Functionality of pins 23 and 25 depends on the mode. See Host/Hardware mode description.
6. Output drivers will output CMOS logic levels into a CMOS load.

ANALOG SPECIFICATIONS (T_A = - 40 ° to 85 ° C, V+ = 5.0V ± 5%, GND = 0V)

Parameter		Min	Typ	Max	Units
TRANSMITTER					
AMI Output Pulse Amplitudes (Measured at the DSX; Normalization factor for Figure 6)		2.4	3.0	3.6	V
Load Presented To Transmitter Output		-	25	-	Ohms
Jitter Added by the Transmitter (Note 7)	10Hz - 8kHz	-	0.01	-	UI
	8kHz - 40kHz	-	0.025	-	UI
	10Hz - 40kHz	-	0.025	-	UI
	Broad Band	-	0.05	-	UI
RECEIVER					
Sensitivity Below DSX (0dB = 2.4V)		10	-	-	dB
Loss of Signal Threshold		-	0.3	-	V
Data Decision Threshold		-	65	-	% of peak
Allowable Consecutive Zeros before LOS		160	175	190	
Input Jitter Tolerance	10kHz - 100kHz (Note 8)	0.4	-	-	UI
JITTER ATTENUATOR					
Jitter Attenuation Curve Corner Frequency (Note 9)		-	6	-	Hz

Notes: 7. Input signal to TCLK is jitter free.
8. See Figure 9.
9. Circuit attenuates jitter at 20 dB/decade above the corner frequency. See Figure 10.

2

T1 SWITCHING CHARACTERISTICS (T_A = - 40 ° to 85 ° C, V+ = 5.0V ± 5%, GND = 0V;
Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 10)	f_c	-	6.176000	-	MHz
TCLK Frequency		f_{in}	-	1.544	-	MHz
ACLKI Frequency	(Note 11)	f_{out}	-	1.544	-	MHz
RCLK Pulse Width		t_{pwh}	-	324	-	ns
	(Note 12)	t_{pwl}	-	324	-	ns
RCLK Duty Cycle	(Note 13)		-	50	-	%
Rise Time, All Digital Outputs	(Note 14)	t_r	-	-	100	ns
Fall Time, All Digital Outputs	(Note 14)	t_f	-	-	100	ns
TPOS/TNEG to TCLK Falling Setup Time		t_{su}	25	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time		t_h	25	-	-	ns
RPOS/RNEG to RCLK Rising Setup Time		t_{su}	-	274	-	ns
RCLK Rising to RPOS/RNEG Hold Time		t_h	-	274	-	ns

CCITT SWITCHING CHARACTERISTICS (T_A = - 40 ° to 85 ° C, V+ = 5.0V ± 5%, GND = 0V;
Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 10)	f_c	-	8.192000	-	MHz
TCLK Frequency		f_{in}	-	2.048	-	MHz
ACLKI Frequency	(Note 11)	f_{out}	-	2.048	-	MHz
RCLK Pulse Width		t_{pwh}	-	244	-	ns
	(Note 12)	t_{pwl}	-	244	-	ns
RCLK Duty Cycle	(Note 13)		-	50	-	%
Rise Time, All Digital Outputs	(Note 14)	t_r	-	-	100	ns
Fall Time, All Digital Outputs	(Note 14)	t_f	-	-	100	ns
TPOS/TNEG to TCLK Falling Setup Time		t_{su}	25	-	-	ns
TCLK Falling to TPOS/TNEG Hold Time		t_h	25	-	-	ns
RPOS/RNEG to RCLK Rising Setup Time		t_{su}	-	194	-	ns
RCLK Rising to RPOS/RNEG Hold Time		t_h	-	194	-	ns

Notes: 10. Crystal must meet specifications described in *Applications* section of this data sheet.
11. ACLK provided by an external source or TCLK.
12. The sum of the pulse widths must always meet the frequency specifications.
13. Duty cycle is (t_{pwh} / (t_{pwh} + t_{pwl})) * 100%.
14. At max load of 1.6 mA and 50 pF.

SWITCHING CHARACTERISTICS - HOST MODE (T_A = - 40 ° to 85 ° C, V+ = 5.0V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = RV+)

Parameter	Symbol	Min	Typ.	Max	Units
SDI to SCLK Setup Time	t_{dc}	50	-	-	ns
SCLK to SDI Hold Time	t_{cdh}	50	-	-	ns
SCLK Low Time	t_{cl}	250	-	-	ns
SCLK High Time	t_{ch}	250	-	-	ns
SCLK Rise and Fall Time	t_r , t_f	-	-	50	ns
$\overline{CS}$ to SCLK Setup Time	t_{cc}	50	-	-	ns
SCLK to $\overline{CS}$ Hold Time	t_{cch}	50	-	-	ns
$\overline{CS}$ Inactive Time	t_{cwh}	250	-	-	ns
SCLK to SDO Valid (Note 15)	t_{cdv}	-	-	200	ns
$\overline{CS}$ to SDO High Z	t_{cdz}	-	100	-	ns

Note: 15. Output load capacitance = 50 pF.

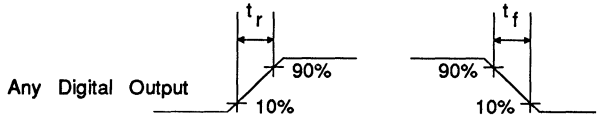


Figure 1. - Signal Rise and Fall Characteristics

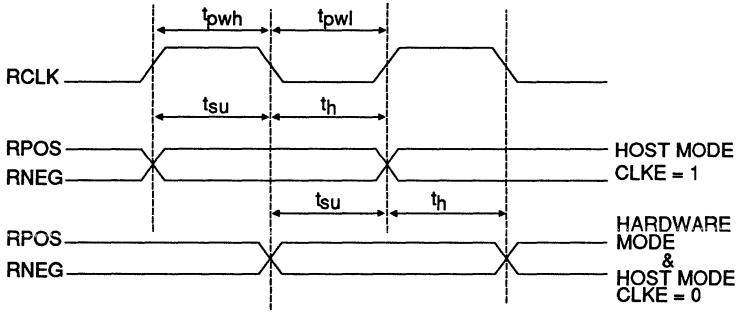


Figure 2. - Recovered Clock and Data Switching Characteristics

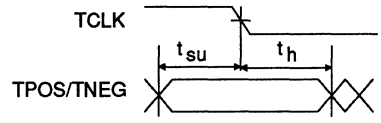


Figure 3. - Transmit Clock and Data Switching Characteristics

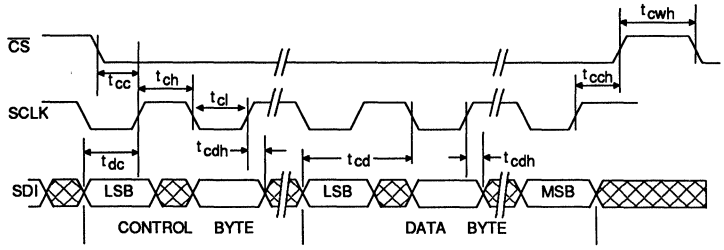


Figure 4. - Serial Port Write Timing Diagram

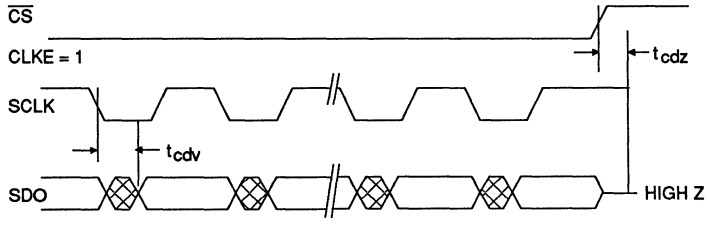


Figure 5. - Serial Port Read Timing Diagram

THEORY OF OPERATION

Transmitter

The transmitter takes binary (dual unipolar) data from a T1 terminal and produces alternate bipolar pulses of appropriate shape. The transmit clock and transmit data (TCLK, TPOS & TNEG) are supplied synchronously. Data is sampled on the falling edge of the input clock.

Either T1 or CCITT G.703 pulse shapes may be selected. For T1 application, line lengths from 0 to 655 feet (as measured from the CS61574 to the DSX-1 cross connect) are selectable. Pulse shaping and signal level are determined by "line length select" inputs and require no external circuitry. Pulse shaping is accomplished with a slew rate controlled fast digital to analog converter. Alternate mark inversion operation is implemented by driving the line in a true differential manner. In order to achieve the necessary line voltages, which exceed the 5 volt supply, a two-to-one, step-up transformer is required. The line driver is designed to drive a 25 Ω equivalent load.

To place the device in a low power dissipation mode (i.e., to disable the drive), the TPOS and TNEG should be held low while TCLK continues to be input. When any transmit control pin (TAOS, LEN0-2 or LLOOP) is toggled, the transmitter stabilizes within 22-bit periods. The transmitter will take longer to stabilize when RLOOP is selected because the timing circuitry must adjust to the new frequency.

Transmit Line Length Selection

The transmitter has a 13-phase delay line which divides each TCLK cycle into 13 phases. These phases are then used to trigger different portions of the output wave form. For T1 applications, the line length selection offers a five partition arrangement for ABAM and PIC cable as shown in Table 1. For each line length selected, the CS61574 modifies the output pulse to meet the requirements of Compatibility Bulletin 119. When using cable other than ABAM or equivalent, it is recommended that the optimal LEN0, 1, & 2 settings be determined by experimentation using the same type of cable to be used in the application. A typical output pulse is shown in Figure 6.

LEN2	LEN1	LEN0	LINE LENGTH SELECTED (FEET)	APPLICATION
0	1	1	0-133	DSX-1 ABAM and PIC
1	0	0	133-266	
1	0	1	266-399	
1	1	0	399-533	
1	1	1	533-655	
0	0	1	Reserved	
0	0	0	G.703	2.048 MHz CCITT
0	1	0	Part 68, Option A	CSU
0	1	1	TICI.2	

Table 1 - Line Length Selection

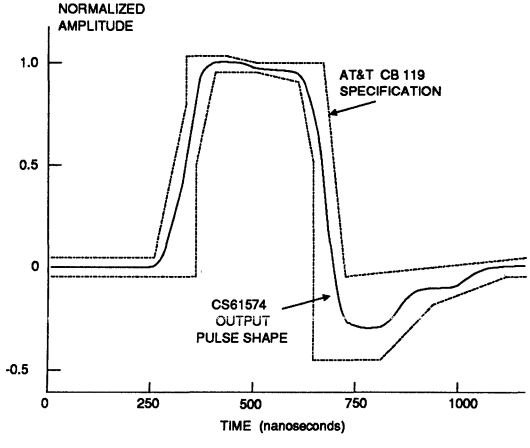


Figure 6 - Typical Pulse Shape at DSX-1 Cross Connect

	For coaxial cable, 75 ohm load and transformer specified in Table A2.	For shielded twisted pair, 120 ohm load and transformer specified in Table A2.
Nominal peak voltage of a mark (pulse)	2.37 V	3 V
Peak voltage of a space (no pulse)	0 ± 0.237 V	0 ± 0.3 V
Nominal pulse width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the center of the pulse interval	0.95 to 1.05	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05	

Table 2 - CCITT G.703 Pulse Specifications

The CCITT G.703 pulse shape is also supported. Transformer and resistor values depend on whether the coax or shielded cable is used, as shown in the *Applications* section at the back of this data sheet. The CCITT pulse shape meets the template shown in Figure 7, assuming the conditions shown in Table 2 are met. The T1 CSU pulse shapes meet FCC Part 68 for 0dB line build out and future ECSA T1C1.2 pulse shapes as shown in Table 1 .

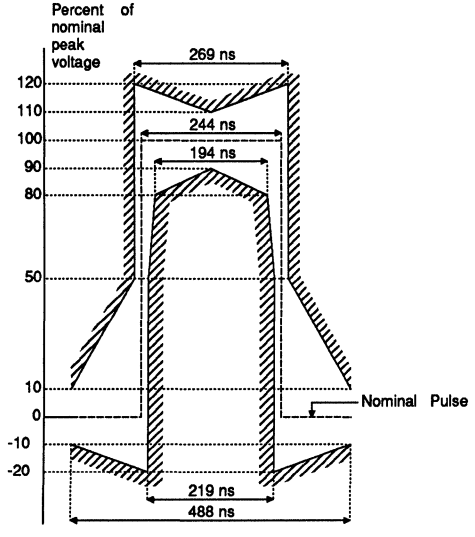


Figure 7 - Mask of the Pulse at the 2048 kbps Interface

Transmit All Ones Select

The transmitter provides for all ones insertion at the frequency of TCLK. Transmit all ones is selected when TAOS goes high, and causes continuous ones to be transmitted on the line (TTIP and TRING). In this mode, the TPOS and TNEG inputs are ignored. If Remote Loopback is in effect, any TAOS request will be ignored.

Receiver

The receiver extracts data and clock from an AMI (Alternate Mark Inversion) coded signal and outputs clock and synchronized data. The receiver is sensitive to signals over the entire range of cable lengths and requires no equalization or ALBO (Automatic Line Build Out) circuits. The signal is received on both ends of a center-tapped, center-grounded transformer. The transformer is center tapped on the CS61574 side. The clock and data recovery circuit meets or exceeds the jitter tolerance specifications of Publications 43802, 43801, 62411, TR-TSY-000170, and CCITT REC. G.823.

A block diagram of the receiver is shown in Figure 8. The two leads of the transformer (RTIP and RRING) have opposite polarity allowing the receiver to treat RTIP and RRING as unipolar

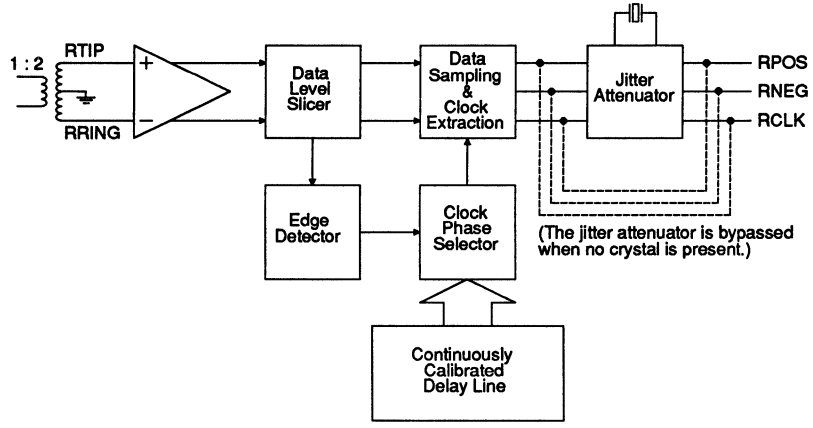


Figure 8. - Receiver Block Diagram

signals. Comparators are used to detect pulses on RTIP and RRING. The comparator thresholds are dynamically established by peak detectors to be at least 65% of peak level.

The leading edge of an incoming data pulse triggers the clock phase selector. The phase selector chooses one of the 13 available phases which the delay line produces for each bit period. The output from the phase selector feeds the clock and data recovery circuits which generate the recovered clock and sample the incoming signal at appropriate intervals to recover the data.

Data sampling will continue at the periods selected by the phase selector until an incoming pulse phase deviates enough to cause a new phase to be selected for data sampling. The phases of the delay line are selected and updated to allow as much as 0.4 UI of jitter from 10 kHz to 100 kHz, without error. The jitter tolerance of the receiver is shown in Figure 9. Additionally, this method of clock and data recovery is tolerant

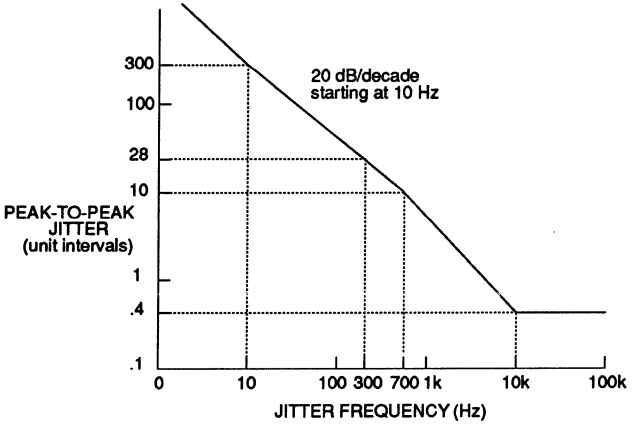


Figure 9. - Input Jitter Tolerance of Receiver
(Clock Recovery Circuit and Jitter Attenuator)

of long strings of consecutive zeros. The data sampler will continuously sample data based on its last input until a new pulse arrives to update the clock phase selector.

The delay line is continuously calibrated relative to a reference clock, which is provided by either ACLKI or the crystal oscillator if ACLKI is grounded. In operation, the delay loop is continuously calibrated by the reference clock to ensure timing accuracy during operation, even if temperature or power supply voltage fluctuate. The delay line produces 13 phases for each cycle of the reference clock. In effect, the 13 phases are analogous to a 20 MHz clock when the reference clock is 1.544 MHz. This implementation utilizes the benefits of a 20 MHz clock for clock recovery without actually having the clock present to impede analog circuit performance.

In the hardware mode, data at RPOS and RNEG is stable and may be sampled on the rising edge of the recovered clock. In the host mode, CLKE determines the clock polarity for which output data is stable and valid as shown in Table 3.

MODE (pin 5)	CLKE (pin 28)	DATA	CLOCK	Clock Edge for Valid Data
LOW	X	RPOS	RCLK	Rising
		RNEG	RCLK	Rising
HIGH	LOW	RPOS	RCLK	Rising
		RNEG	RCLK	Rising
		SDO	SCLK	Falling
HIGH	HIGH	RPOS	RCLK	Falling
		RNEG	RCLK	Falling
		SDO	SCLK	Rising

X= Don't care

Table 3 - Data Output / Clock Relationship

Loss of Signal

The CS61574 will indicate loss of signal upon receiving 175 consecutive zeros. A digital counter counts received zeros, based on RCLK cycles. The zero input level is determined either when zeros are received, or when the received signal amplitude degrades below a $0.3V_{peak}$ threshold. LOS returns to logic zero when the received signal returns to 12.5% ones density (based on 4 ones out of 32 bit periods). Received data is output on RPOS/RNEG regardless of LOS status.

The receiver reports loss of signal by setting the Loss of Signal pin, LOS, high. If the serial interface is used, the LOS bit will be set and an interrupt will be issued on $\overline{INT}$. LOS will go low (and flag the $\overline{INT}$ pin again if the serial I/O is used) when a valid signal is detected. Note that in the host mode, LOS is simultaneously available from both the register and pin 12. Table 4 shows the status of RCLK upon LOS.

Crystal present?	ACLKI present?	LOS	Source of RCLK
No	Yes	Yes	ACLKI
Yes	No	Yes	Centered Crystal
Yes	Yes	Yes	ACLKI via the Jitter Attenuator

Table 4. - RCLK Status at LOS

Note that if a crystal is used, the jitter attenuator will buffer any instantaneous changes in phase or frequency between the last recovered clock and the reference clock (which is provided by either the crystal or ACLKI). This means that RCLK will smoothly transition to the new frequency.

Wander and Jitter Attenuator

The jitter attenuator is designed to reduce wander and jitter in the recovered clock signal. It consists of a 32 bit FIFO, a crystal oscillator, a set of capacitors and control logic. The jitter attenuator meets or exceeds the jitter attenuation requirements of Publications 43802, 62411, and REC. G.742. A typical jitter attenuation curve is

shown in Figure 10. The jitter attenuator can be disabled and its FIFO bypassed by grounding XTALOUT, pin 10, and tying XTALIN, pin 9, to the supply through a resistor.

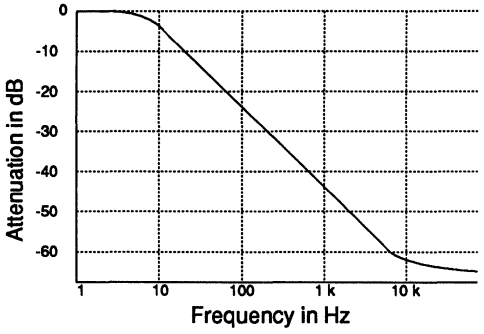


Figure 10. - Typical Jitter Attenuation Curve

The jitter attenuator works in the following manner. The recovered clock and data are input to the FIFO with the recovered clock controlling the FIFO's write pointer. The crystal oscillator controls the FIFO's read pointer which reads data out of the FIFO and presents it at RPOS and RNEG. The update rate of the read pointer is analogous to RCLK. By changing the load capacitance that the CS61574 presents to the crystal, the oscillation frequency is adjusted to the average frequency of the recovered signal. Logic determines the phase relationship between the read and write pointers and decides how to adjust the load capacitance of the crystal. Thus the jitter attenuator behaves as a first-order phase lock loop. Signal jitter is absorbed in the FIFO.

The FIFO in the jitter attenuator is designed to neither overflow nor underflow. If the jitter amplitude becomes very large, the read and write pointers may get very close together. Should they attempt to cross, either an earlier or a later clock phase will be selected from oscillator and used to drive the read pointer thereby preventing the pointers from crossing (i.e. the oscillator's divide by four circuit adjusts by performing a divide by 3 1/2 or divide by 4 1/2 to prevent the overflow or underflow). During this activity, RCLK will effectively be locked, to the recovered clock, but data will never be lost. The jitter attenuator is designed so it will tolerate at least 28 unit intervals before the overflow or underflow mechanism takes effect.

Local Loopback

The local loopback mode takes clock and data presented on TCLK, TPOS, and TNEG, sends it through the jitter attenuator and outputs it at RCLK, RPOS and RNEG. If the jitter attenuator is disabled, it is bypassed. Inputs to the transmitter are still transmitted on the line, unless TAOS has been selected in which case, AMI-coded continuous ones are transmitted to the line at the rate determined by TCLK. Receiver inputs are ignored when local loopback is in effect. Local loopback is selected by taking LLOOP, pin 27, high or LLOOP may be commanded via the serial interface.

Remote Loopback

In remote loopback, the recovered clock and data input on RTIP and RRING are sent through the jitter attenuator to remove jitter, and back out on the line via TTIP and TRING. Selecting remote loopback overrides any TAOS request (see Table 5). The recovered incoming signals are also sent

RLOOP Input Signal	TAOS Input Signal	Source of Data for TTIP & TRING	Source of Clock for TTIP & TRING
0	0	TDATA	TCLK
0	1	all 1s	TCLK
1	X	RTIP & RRING	RTIP & RRING(RCLK)

Notes:
1. X = Don't care. The identified All Ones Select input is ignored when the indicated loopback is in effect.
2. Logic 1 indicates that Loopback or All Ones option is selected.

Table 5. - Interaction of RLOOP and TAOS

to RCLK, RPOS and RNEG. A remote loopback occurs in response to RLOOP going high. Simultaneous selection of local and remote loopback modes is not valid (see Reset).

Driver Performance Monitor

To aid in early detection and easy isolation of nonfunctioning links, the CS61574 is able to monitor transmit drive performance and report when the driver is no longer operational. This feature can be used to monitor either the device's performance or the performance of a neighboring driver. The driver performance monitor indicator is normally at a low (zero) logic level, and goes to high level upon detecting driver failure.

The driver performance monitor consists of a receiver that monitors the transmitted signal on input pins, MTIP and MRING. If no signal is present on MTIP and MRING for 63 clock cycles, the DPM pin goes high.

Whenever more than one CS61574 reside on the same circuit board, the effectiveness of the driver performance monitor can be maximized by having each CS61574 monitor performance of a neighboring CS61574 device, rather than having it monitor its own performance. Note that in the host mode, DPM is available from both the register and pin 11.

Power On Reset / Reset

Upon power-up, the CS61574 is held in a static state until the supply crosses a threshold of approximately three volts. When this threshold is crossed, the device will delay for about 10 ms to allow the power supply to reach operating voltage. After this delay, calibration of the delay lines used in the transmit and receive sections commences. The delay lines can only be calibrated if a reference clock is present. The reference clock for the receiver is provided by ACLKI, or the crystal oscillator is used if ACLKI is grounded. The reference clock for the transmitter is provided by TCLK. The initial calibration should take less than 20 ms.

In operation, the delay lines are continuously calibrated, making the performance of the device independent of power supply or temperature variations. The continuous calibration function forgoes any requirement to reset a CS61574 when in operation. However, a reset function is available in both the Hardware and Host modes.

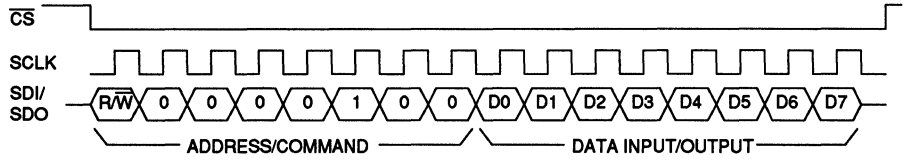
In the Hardware mode, a reset request is made by simultaneously setting both RLOOP and LLOOP high for at least 200 ns. Reset will initiate on the falling edge of the reset request (falling edge of RLOOP and LLOOP). In the Host Mode, a reset is initiated by simultaneously writing RLOOP and LLOOP to the register. In either mode, a reset will set all registers to 0 and force the oscillator to its center frequency before initiating calibration.

Mode of Operation

	MODE	
PIN #	HARDWARE	HOST
PIN 23	LEN0	$\overline{\text{INT}}$
PIN 24	LEN1	SDI
PIN 25	LEN2	SDO
PIN 26	RLOOP	$\overline{\text{CS}}$
PIN 27	LLOOP	SCLK
PIN 28	TAOS	CLKE

Table 6. - Pin Definitions

The CS61574 can be operated in two modes, the hardware mode and the host mode. In the hardware mode, discrete pins are used to interface the device's control functions and status information. In the host mode, the CS61574 is connected to a host processor and a serial data bus is used for input and output of control and



NOTE: SDI sampled on rising edge of SCLK; SDO updated on falling edge of SCLK (CLKE = 1).

Figure 11. - Input / Output Timing

status information. There are six dual function pins whose functionality is determined by the mode pin, MODE. Table 6 shows the pin definitions.

Serial Interface

In the host mode, pins 23 through 28 serve as a microprocessor/microcontroller interface. One on-board register can be written to the SDI pin or read from the SDO pin at the clock rate determined by SCLK. Through this register, a host controller can be used to control operational characteristics and monitor device status. The serial port read/write timing is independent of the system transmit and receive timing.

Data transfers are initiated by taking the chip select input, $\overline{CS}$, low ($\overline{CS}$ must initially be high). Address and input data bits are clocked in on the rising edge of SCLK. The clock edge on which output data is stable and valid is determined by CLKE as shown in Table 3. Data transfers are terminated by setting $\overline{CS}$ high. $\overline{CS}$ may go high no sooner than 50 ns after the falling edge of the SCLK cycle corresponding to the last write bit. For a serial data read, $\overline{CS}$ may go high any time to terminate the output.

Figure 11 shows the timing relationships for data transfers when CLKE = 1. When CLKE = 0, data output from the serial port, SDO, is valid on the falling edge of SCLK. Data bit D7 is held until the rising edge of the 17th clock cycle for CLKE = 1; data is held until the falling edge of the 17th clock cycle for CLKE = 0.

An address/command byte, shown in Table 7, precedes a data register. The first bit of the address/command byte determines whether a read or a write is requested. The next six bits contain the address. The CS61574 responds to address 16 (0010000). The last bit is ignored.

LSB, first bit	0	R/$\overline{W}$	Read/Write Select; 0 = write, 1 = read
	1	ADD0	LSB of address. Must be 0
	2	ADD1	Must be 0
	3	ADD2	Must be 0
	4	ADD3	Must be 0
	5	ADD4	Must be 1
	6	-	Reserved - Must be 0
MSB, last bit	7	X	Don't Care

Table 7. - Address/Command Byte

The data register, shown in Table 8, can be written to the serial port. Data is input on the eight clock cycles immediately following the address/command byte. Bits 0 and 1 are used to clear an interrupt issued from the $\overline{INT}$ pin, which occurs in response to a loss of signal or a problem with the output driver.

LSB: first bit in	0	clr LOS	Clear Loss Of Signal
	1	clr DPM	Clear Driver Performance Monitor
	2	LEN0	Bit 0 - Line Length Select
	3	LEN1	Bit 1 - Line Length Select
	4	LEN2	Bit 2 - Line Length Select
	5	RLOOP	Remote Loopback
	6	LLOOP	Local Loopback
MSB: last bit in	7	TAOS	Transmit All Ones Select

NOTE: Setting bits 5,6 & 7 to 101 or 111 puts the CS61574 into a factory test mode.

Table 8. - Input Data Register

LSB: first bit in	0	LOS	Loss Of Signal
	1	DPM	Driver Performance Monitor
	2	LEN0	Bit 0 - Line Length Select
	3	LEN1	Bit 1 - Line Length Select
	4	LEN2	Bit 2 - Line Length Select

Table 9. - Output Data Bits 0 - 4

Output data from the serial interface is presented as shown in Tables 9 and 10. Bits 2, 3 and 4 can be read to verify line length selection. Bits 5, 6 and 7 must be decoded. Codes 101, 110 and 111 (Bits 5, 6 and 7) indicate intermitent losses of signal and/or driver problems.

SDO goes to a high impedance state when not in use. SDO and SDI may be tied together in applications where the host processor has a bidirectional I/O port.

Bits 5	6	7	Status
0	0	0	Reset has occurred or no program input.
0	0	1	TAOS in effect.
0	1	0	LLOOP in effect.
0	1	1	TAOS/LLOOP in effect.
1	0	0	RLOOP in effect.
1	0	1	DPM changed state since last "clear DPM" occurred.
1	1	0	LOS has changed state since last "clear LOS" occurred.
1	1	1	LOS & DPM have changed state since last "clear LOS" and "clear DPM".

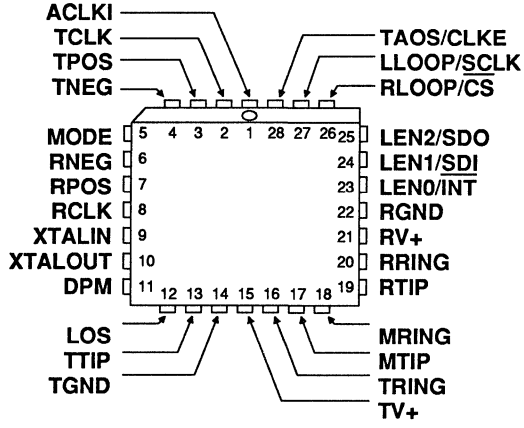
Table 10. Coding for Serial Output bits 5,6,7

Power Supply

The device operates from a single 5 volt supply. Separate pins for transmit and receive supplies provide internal isolation. However these pins may be connected externally with no impact on device performance, provided the power supply pins are decoupled to their respective grounds. If the same power bus is used, the receive power supply should be decoupled from ground with a 68 µF tantalum capacitor and a mylar or ceramic 0.1 µF capacitor. A 1.0 µF mylar or ceramic capacitor should be used on the transmit power supply. These capacitors should be located physically close to the device. If seperate power busses are used for TV+/TGND and RV+/RGND, an additional 68 µF capacitor should be used on the transmit supply. TV+ must not exceed RV+ by more than 0.3V.

PIN DESCRIPTIONS

ALTERNATE EXTERNAL CLOCK	ACLKI	1	28	TAOS/CLKE	TRANSMIT ALL ONES SELECT
TRANSMIT CLOCK	TCLK	2	27	LLOOP/SCLK	LOCAL LOOP BACK
TRANSMIT POSITIVE PULSE	TPOS	3	26	RLOOP/CS	REMOTE LOOP BACK
TRANSMIT NEGATIVE PULSE	TNEG	4	25	LEN2/SDO	BIT 2 OF LINE LENGTH SELECT
MODE SELECTION	MODE	5	24	LEN1/SDI	BIT 1 OF LINE LENGTH SELECT
RECEIVED NEGATIVE PULSE	RNEG	6	23	LEN0/INT	BIT 0 OF LINE LENGTH SELECT
RECEIVED POSITIVE PULSE	RPOS	7	22	RGND	RECEIVE GROUND
RECOVERED CLOCK	RCLK	8	21	RV+	RECEIVE V+ (+5VDC)
CRYSTAL CONNECTION	XTALIN	9	20	RRING	RECEIVE RING
CRYSTAL CONNECTION	XTALOUT	10	19	RTIP	RECEIVE TIP
DRIVER PERFORMANCE MONITOR	DPM	11	18	MRING	MONITORED RING
LOSS OF SIGNAL	LOS	12	17	MTIP	MONITORED TIP
TRANSMIT TIP	TTIP	13	16	TRING	TRANSMIT RING
TRANSMIT GROUND	TGND	14	15	TV+	TRANSMIT V+ (+5VDC)



Power Supplies

TV+ - Positive Power Supply, Transmit Drivers, Pin 15.
Positive power supply for the transmit drivers; typically +5 volts. TV+ must not exceed RV+ by more than 0.3V.

TGND - Ground, Transmit Drivers, Pin 14.
Power supply ground for the transmit drivers; typically 0 volts.

RV+ - Positive Power Supply, Pin 21.
Positive power supply for the device, except transmit drivers; typically +5 volts.

RGND - Ground, Pin 22.
Power supply ground for the device, except transmit drivers; typically 0 volts.

Oscillator

XTALIN, XTALOUT - Crystal Connections, Pins 9 and 10.

A 6.176 MHz (8.192 MHz for CCITT applications) crystal should be connected across these pins. The jitter attenuator may be disabled by tying XTALIN, Pin 9 to the power supply through a resistor, and grounding XTALOUT, Pin 10. Overdriving the oscillator with an external clock is not supported.

Control

MODE - Mode Select, Pin 5.

Setting MODE to logic 1 puts the CS61574 in the host mode. In the host mode, a serial control port is used to control the CS61574 and determine its status. Setting MODE to logic 0 puts the CS61574 in the hardware mode, where configuration and status are controlled by discrete pins. MODE defines the status of pins 23 through 28.

Hardware Mode

TAOS - Transmit All Ones Select, Pin 28.

Setting TAOS to a logic 1 causes continuous ones to be transmitted at the frequency determined by TCLK.In the host mode, simultaneous selection of RLOOP & TAOS enables a factory test mode.

LLOOP - Local Loopback, Pin 27.

Setting LLOOP to a logic 1 routes the transmit clock and data through the jitter attenuator to the receive clock and data pins. TCLK and TPOS/TNEG are still transmitted unless overridden by a TAOS request. Inputs on RTIP and RRING are ignored.

RLOOP - Remote Loopback, Pin 26.

Setting RLOOP to a logic 1 causes the recovered clock and data to be sent through the jitter attenuator (if active) and through the driver back to the line. The recovered signal is also sent to RCLK and RPOS/RNEG. Any TAOS request is ignored in the hardware mode. In the host mode, simultaneous selection of RLOOP & TAOS enables a factory test mode.

Simultaneously taking RLOOP and LLOOP high for at least 200 ns initiates a device reset.

LEN0, LEN1, LEN2 - Line Length Selection, Pins 23, 24 and 25.

Determines the shape and amplitude of the transmitted pulse to accommodate several cable types and lengths. See Table 1 for information on line length selection.

Host Mode

$\overline{\text{INT}}$ - Receive Alarm Interrupt, Pin 23.

Goes low when LOS or DPM change state to flag the host processor. $\overline{\text{INT}}$ is cleared by reading the serial data output. $\overline{\text{INT}}$ is an open drain output and should be tied to the positive supply through a resistor.

SDI - Serial Data Input, Pin 24.
Data for the on-chip registers and is sampled on the rising edge of SCLK.

SDO - Serial Data Output, Pin 25.
Status and control information from the on-chip registers. If CLKE is high SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to or $\overline{CS}$ is high.

CLKE - Clock Edge, Pin 28.
Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. Conversely, setting CLKE to logic 0 causes RPOS and RNEG to be valid on the rising edge of RCLK, and SDO to be valid on the falling edge of SCLK.

SCLK - Serial Clock, Pin 27.
Clock used to read or write the serial port registers.

$\overline{CS}$ - Chip Select, Pin 26.
Pin must transition from high to low to read or write the serial ports.

Inputs

ACLKI - Alternate External Clock Input, Pin 1.
Either a 1.544 MHz (or 2.048 MHz for CCITT) clock must be input to ACLKI, or this pin must be tied to ground. If ACLKI is grounded, an appropriate crystal must be attached to XTLOUT and XTLIN, pins 9 and 10. If ACLKI is driven by a clock, this clock is used to calibrate the delay lines. ACLKI is driven to the RCLK output upon loss of signal. If the jitter attenuator is active, ACLKI is input to the jitter attenuator upon loss of signal.

TCLK, TPOS, TNEG - Transmit Clock, Transmit Positive Data, Transmit Negative Data - Pins 2, 3 and 4.
Inputs for clock and data to be transmitted. The signal is driven on to the line through TTIP and TRING. TPOS and TNEG are sampled on the falling edge of TCLK. A TPOS input causes a positive pulse to be transmitted, while a TNEG input causes a negative pulse to be transmitted.

RTIP, RRING - Receive Tip, Receive Ring, Pins 19 and 20.
The AMI receive signal is input to these pins. A center-tapped, center-grounded, 2:1, step-up transformer is required on these inputs, as shown in Figure A1 in the *Applications* section. Data and clock are recovered and output on RPOS/RNEG and RCLK.

MTIP, MRING - Monitored Tip, Monitored Ring, Pins 17 and 18.
These pins are normally connected to TTIP and TRING and monitor the output of a CS61574. If the monitors are not used, tying MTIP low and MRING high through a resistor will reduce power consumption slightly. If the $\overline{INT}$ pin in the host mode is used, and the monitor is not used, input a clock signal to one of the monitor pins and tie the other monitor pin to ap-

proximately the clock's mid-voltage level. This clock frequency can range from 100 kHz to the TCLK frequency.

Status

LOS - Loss of Signal, Pin 12.

LOS goes to a logic 1 when 175 consecutive zeros have been detected. LOS returns to logic 0 when a 12.5% ones density signal returns (determined by receipt of 4 ones within 32 bit periods). When in the loss of signal state, received ones are still output at RPOS/RNEG.

DPM - Driver Performance Monitor, Pin 11.

If no signal is present on MTIP and MRING for 63 clock cycles, DPM goes to a logic 1 until the first detected signal.

Outputs

RCLK, RPOS, RNEG - Recovered Clock, Receive Positive Data, Receive Negative Data - Pins 8, 7 and 6.

Data and clock are recovered from the RTIP and RRING inputs and are output at these pins. A signal on RPOS corresponds to a positive pulse received on RTIP and RRING, while a signal on RNEG corresponds to the receipt of a negative pulse. RPOS and RNEG are NRZ. In the hardware mode, RPOS and RNEG are stable and valid on the rising edge of RCLK. In the host mode, CLKE determines the clock edge for which RPOS and RNEG are stable and valid. See Table 3.

TTIP, TRING - Transmit Tip, Transmit Ring, Pins 13 and 16.

The AMI signal is driven to the line through these pins. This output is designed to drive a 25 Ω load. A 2:1 step-up transformer is required as shown in Figure A1. When driving 75 Ω coax cable, two 2.2 Ω resistors should be added as shown in Figure A2. The transmitter will drive twisted-shielded pair cable, terminated with 120 Ω, without additional components.

APPLICATIONS

Line Interface

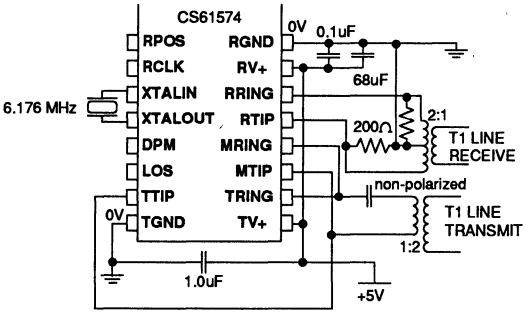


Figure A1. - Typical Configuration Showing Line Interface

Figure A1 shows the typical configuration for interfacing the CS61574 to a T1 line through transmit and receive transformers. The receiver transformer is center tapped and center grounded with 200 Ω resistors between the center tap and each leg on the CS61574 side. These resistors provide the 100 Ω termination for the T1 line. When terminating twisted-shielded pair cable, 240 Ω resistors will provide the required 120 Ω load.

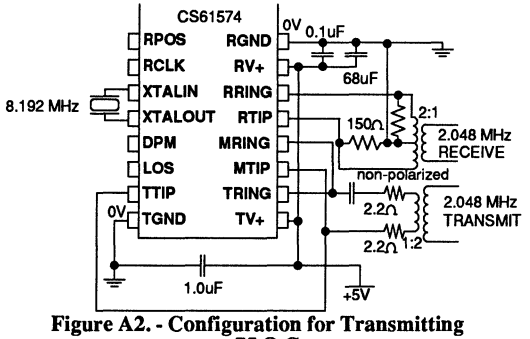


Figure A2. - Configuration for Transmitting onto 75 Ω Coax

Figure A2 shows the configuration needed for transmitting data at 2.048 MHz onto a 75 Ω coax cable. The 2.2 Ω resistors serve two functions. First, they provide the appropriate 25 Ω load to TTIP and TRING. Second, the resistors attenuate the signal slightly to meet the CCITT pulse amplitude requirements. Note that these 2.2 Ω resistors should not be used when interfacing to CCITT 120 Ω cable. For the receiver, the terminating resistors should be 150 Ω to provide the necessary 75 Ω termination to the line.

Decoupling

Decoupling and filtering of the power supplies is crucial for proper operation of the analog sections in the transmit and receive paths. If different power and ground buses supply the transmitter and receiver supply inputs, a 68 µF capacitor should be added to the transmit supply. The decoupling capacitors shown in Figures A1 and A2 should be high grade capacitors, (i.e., 68 µF - tantalum or better; 1.0 and 0.1 µF - mylar or ceramic), and should be located as close as possible to the power supply pins of the chip. Wire wrap bread-boarding of the CS61574 is not recommended because lead resistance and wrap inductance serve to defeat the function of the decoupling capacitors.

Selecting an Oscillator Crystal

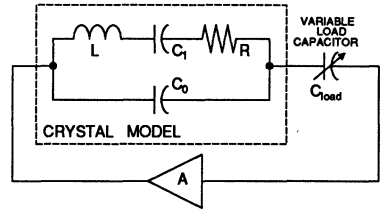


Figure A3. - Equivalent Circuit of Oscillator

Figure A3 shows an equivalent representation of the oscillator circuit. The variable load capacitor is internal to the CS61574. The value of this capacitor is controlled by logic internal to the CS61574. Based on this model, equations 1 and 2 have been developed to help calculate the required crystal parameters necessary to meet system requirements.

Two important parameters in this model are the upper and lower bounds of C_{load} (the variable

load capacitor) and the value of C_O. C_O can be used to control the series resonant frequency of the crystal. The minimum value of C_{load} sets the maximum parallel resonant frequency. Together, C_O and C_{load} can be used to set the pull range of the oscillator and its maximum and minimum frequencies.

Determining Required Pull Range

Four factors contribute to the required pull range of the crystal:

1) The frequency range required for the application,
2) The frequency drift of the crystal over the operating temperature range,
3) The variability in load capacitance from IC to IC,
4) The accuracy to which the crystal can be manufactured.

All of these factors have been measured or can be controlled.

For a given crystal geometry, the series resonant frequency of the crystal is inversely proportional to C_O. The relationship of the crystal's series resonant frequency to its parallel resonant frequency in the oscillator circuit determines the pull range of the oscillator. The further away the series resonant frequency is from the parallel resonant frequency (which is set by the load condition in the oscillator circuit) the greater the pull range of the crystal. That is: a smaller C_O (greater series resonant frequency) results in less pull range, while the larger the C_O (lower series resonant frequency), the greater the pull range.

The series resonant frequency of the crystal is calculated by Equation 1.

$$f_S = f_N - \frac{\Delta f}{2(C_L - C_H)}(C_L + C_H + 2C_O) \quad (C\text{'s in pF}) \quad (1)$$

The parallel resonant frequency is calculated by Equation 2.

$$f_{load} = f_S \left(\frac{C_1 + C_{load} + C_O}{C_{load} + C_O} \right)^{1/2} \quad (2)$$

f_S = series resonant frequency of crystal
f_N = 4 * Nominal Signal Frequency
- should be 6.176000 MHz for North America (T1)
- should be 8.192000MHz for Europe (CCITT)

Δf = required pull range of crystal in Hz (Δppm*f_N)
C_L = load capacitance for low frequency oscillation (average is ~38.0 pF)
C_H = load capacitance for high frequency oscillation (average is ~10.5 pF)

Table A1 shows the crystal frequency as a function of load capacitance. The deviation in frequency from the nominal is shown in ppm. Temperature drift has been accounted for as shown. *The accuracy to which C_O can be controlled, and the accuracy to which a crystal can be trained or calibrated should be factored in to guarantee that the required frequency range will be met.*

	T1	CEPT
Frequency Tolerance / C_L in pf	6.176000 MHz ±130 ppm or less	8.192000 MHz ±50 ppm or less
$C_{low\ freq}$ min 34.0	6175197 - Δtd	8191590 - Δtd
$C_{high\ freq}$ max 11.7	6176803 + Δtd	8192410 + Δtd
MAXIMUM ALLOWABLE PULL RANGE	390 ppm	230 ppm

Δ_{td} = crystal temperature drift from -40 to +85 deg. C.

Table A1. - T1 and CEPT Requirement

Transformers

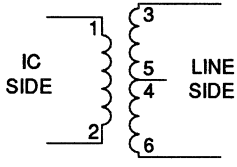
Manufacturer	Part #
Pulse Engineering	5764
Pulse Engineering	FAL 1.0
Pulse Engineering	FAL 4.1
Schott Corp.	67112060
Bell Fuse	0553-5006-IC
Nova Magnetics	6500-07-011
Midcom	671-5832

Note: The Pulse Eng. 1682x is still acceptable, but the other Pulse Engineering transformers are preferred.

Table A2. - Suitable Transformers

Transformers listed in Table A2 have been found to be suitable for use with the CS61574. Figure A4 shows the connections for some of the recommended transformers for the transmitter. Key transmit transformer specifications are:

Turns ratio: 1:2 (or 1:1:1) ± 5%,
Primary inductance: 600 µH min measured at 10kHz and 0.005 VRMS.
Leakage inductance: 1.3 µH max with secondary shorted.
Interwinding capacitance: 23 pF max, primary to secondary.



Bell Fuse 0553-5006-IC
Schott Corp. 67112060
Pulse Engineering 5764 & FAL 1.0

Figure A4.- Some Recommended Transmitter Transformer Configurations

To save on power consumption under normal operating conditions, the output drivers are powered down during the transmission of a space (zero) on to the line. Approximately one quarter cycle prior to transmitting a mark (one), the drivers are enabled. The transformer interacting with the driver can cause a slight voltage difference (<200 mV) between the driven zero and the non-driven zero. We recommend that this effect be eliminated by inserting a ≥0.2 uF non-polarized capacitor in series with the primary of the transformer. Contact the factory for more information.

Transmit Side Jitter Attenuation

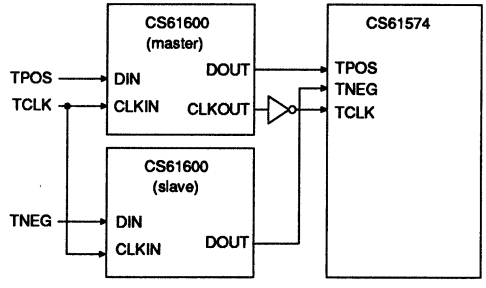


Figure A5. - Transmit Clock and Data Jitter Attenuation

In some applications it is desirable to attenuate jitter from the signal to be transmitted. A CS61600 PCM jitter attenuator can be used to remove at least seven unit intervals of jitter from the transmit clock and data as shown in Figure A5.

Interfacing The CS61574 With T1 Digital Transceivers

This section gives general guidance on how to interface the CS61574 with digital T1 framing and signaling transceivers such as the R8070, and DS2180. Design attention must be given to insure that the devices are properly interfaced. To interface with the R8070, connect the devices as shown in Figure A6. The CS61574 is shown in the hardware mode.

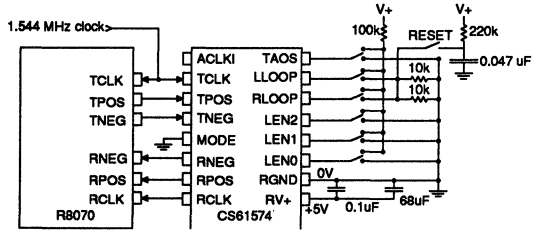


Figure A6. - Interfacing the CS61574 with and R8070

To interface with the DS2180, connect the devices as shown in Figure A7. In this case, the CS61574 and DS2180 are in host mode controlled by a microprocessor serial interface. If the CS61574 is used in hardware mode, then the CS61574 RCLK output must be inverted before being input to the DS2180.

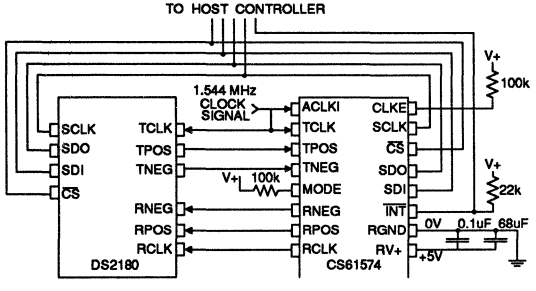


Figure A7. - Interfacing the CS61574 with a DS2180

CS61534 Compatibility

See the Application Note "*CS61534 Design Guidelines to Insure Compatibility with CS61574*".

Semiconductor Corporation

CS6152

PCM Analog Interface

Features

- Provides Analog PCM Line Interface for T1 and 2.048 MHz Applications
- Compliments Digital Gatearray Clock-Recovery Circuits
- Programmable Pulse-Shaping Line Driver
- Provides Receiver AMI-to-TTL Buffer
- Low Power Consumption
- Upwards compatible from CS61534
- Driver Performance Monitor
- Minimal External Components

General Description

The CS6152 combines the analog transmit and receive line interface functions for a PCM system interface in one device. The PCM line interface operates from a 5 Volt supply, is transparent to the PCM framing format, and can work with ABAM and other cable types. Crystal's SMART ANALOG™ circuitry shapes the transmit pulse internally, providing the appropriate pulse shape at the DSX-1 cross-connect for line lengths ranging from 0 to 655 feet in T1 applications. The device provides the ideal front-end to digital gate array based clock recovery circuits.

2

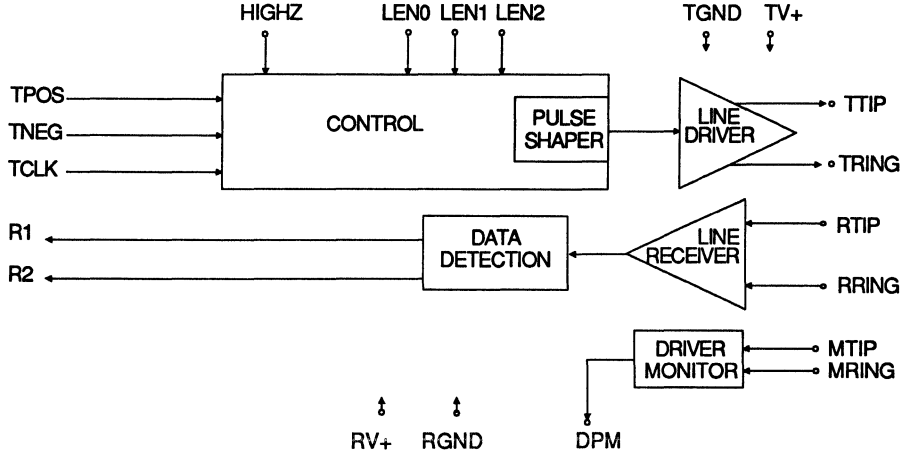
Applications

- Interfacing Network Equipment such as Multiplexers, Channel Banks and Switching Systems to a DSX-1 Cross Connect.
- Interfacing Customer Premises Equipment such as PABXs, T1 Multiplexers, Data PBXs and LAN Gateways to a Channel Service Unit or T1 modem.

ORDERING INFORMATION

CS6152-IP - 24 Pin Plastic, 300 mil DIP
CS6152-IL - 28 Pin J-lead PLCC

Block Diagram



Product Preview

This document contains data for a new product. Crystal Semiconductor reserves the right to modify or discontinue this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, Texas 78760
(512)445-7222 TWX:910-874-1352

• Notes •

Semiconductor Corporation

CS6158

PCM Line Interface

Features

- Provides Analog PCM Line Interface for T1 and 2.048 MHz Applications
- CS61534/CS61574 Compatibility Mode
- Fully monolithic PLL (internal loop filter)
- Provides Line Driver, and Data and Clock Recovery Functions
- Internal generation of transmitted pulse width and pulse shape
- Minimum external components (no external crystal required)

General Description

The CS6158 combines the analog transmit and receive line interface functions for a T1 interface in a 22 pin or 28 pin device. The line interface operates from a single 5 Volt supply and is transparent to the framing format. Crystal's SMART ANALOG™ circuitry shapes the transmit pulse internally, providing the appropriate pulse shape for line lengths ranging from 0 to 655 feet from a DSX-1 cross-connect. An upwards migration path is provided from the 28-pin CS6158 to the higher function CS61534 and CS61574.

Applications

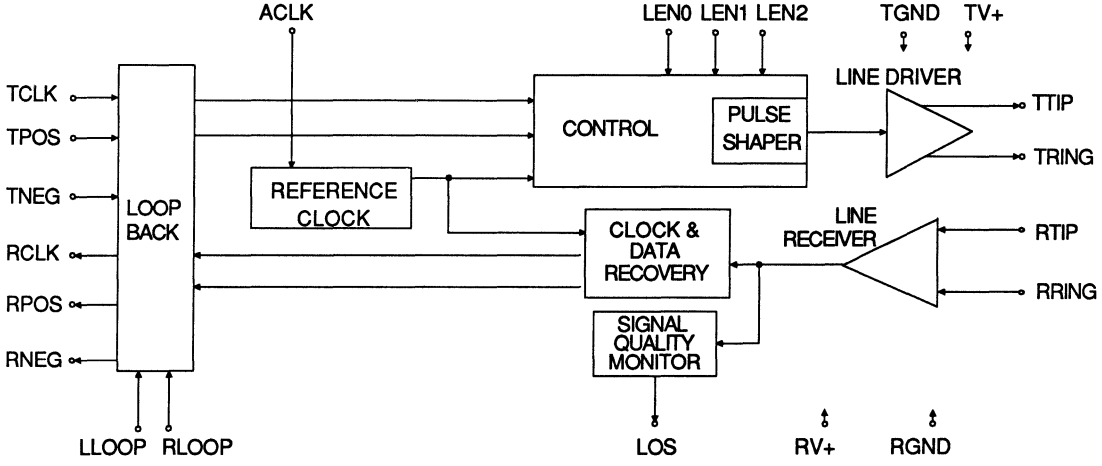
- Interfacing Network Equipment to a DSX-1 Cross Connect
- Interfacing Customer Premises Equipment to a CSU
- Building Channel Service Units

ORDERING INFORMATION

CS6158-IP - 28 Pin Plastic DIP
CS6158-IP2 - 22 Pin Plastic DIP
CS6158-IL - 28 Pin PLCC

2

Block Diagram



Product Preview

This document contains data for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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• Notes •

INTRODUCTION

Crystal offers two jitter attenuator circuits. The CS61600 PCM jitter attenuator uses a 16-bit FIFO and a variable oscillator to provide up to 40 dB of jitter reduction in a 1.544 to 2.048 MHz data stream. Also offered is the CS80600, a general purpose high speed (4.5 to 8.5 MHz) jitter attenuator. This part may be used in conjunction with the TMS380 device family to double the number of stations connected to an IEEE 802.5 token ring local area network. The CS80600 slows the accumulation of data-dependent jitter, allowing more stations and repeaters to be inserted on the ring without overflowing the elastic buffer of the active system monitor. The input to the CS80600 is clock and data which have been recovered by the TMS38051/52. Jitter is removed by the CS80600 using an 8-Manchester symbol FIFO and a variable oscillator. The dejittered clock and data are then input to the TMS38020.

USER'S GUIDE

Device:	CS61600	CS80600
Data Rates	1.544 MHz or 2.048 MHz	4.5-8.5 MHz
Size of FIFO	16	8
Package	14 pin DIP	14 pin DIP

CONTENTS

Semiconductor Corporation

CS61600

PCM Jitter Attenuator

Features

- Unique Clock-Tracking Circuitry Filters 50 Hz or Higher Frequency Jitter for T1 Applications and 40 Hz for CEPT
- Minimal External Components Required
- 14 Pin DIP
- Single 5 Volt Supply
- 3 Micron CMOS for High Reliability and Low Power Dissipation: 50 mW Typical at 25°C

General Description

The CS61600 from Crystal Semiconductor accepts T1 (1.544 Mb/s) or CCITT standard (2.048 Mb/s) data and clock inputs, and tolerates at least 7 (and up to 14) unit intervals, peak-to-peak, of jitter. Before outputting data and clock, jitter is attenuated using an internal clock-tracking variable oscillator and a 16 bit FIFO elastic store.

The jitter attenuation function can be determined by appropriate specification of the external crystal.

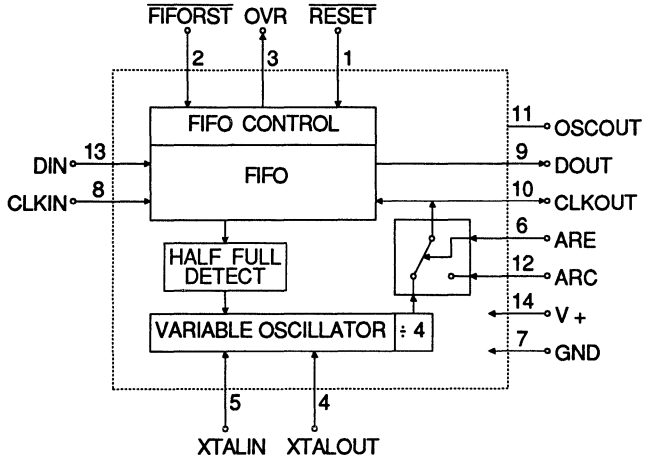
The CS61600 is transparent to data format, and is intended for application in carrier systems, switching systems, Local Area Network gateways and multiplexers.

ORDERING INFORMATION

CS61600-IP - 14 Pin Plastic DIP; T1 only
CS61600-IP1 - 14 Pin Plastic DIP; T1 & CCITT

3

Block Diagram



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, Texas 78760
(512)445-7222 TWX:910-874-1352

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply	V+ - GND	- 0.3	7.0	V
Input Voltage	V_{in}	GND - 0.3	V+ + 0.3	V
Input Current, Any Pin (Note 1)	I_{in}	-	10	mA
Ambient Operating Temperature	T_A	- 40	85	°C
Storage Temperature	T_{stg}	- 65	150	°C

Note: 1. Transient currents of up to 100 mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply	V+ -GND	4.5	5.0	5.5	V
Ambient Operating Temperature	T_A	- 40	25	85	°C

DIGITAL CHARACTERISTICS (T_A = -40°C to 85°C; V+ = 5V ± 10%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 2 & 3)	V_{OH}	2.4	-	-	V
Low-Level Output Voltage (Note 2 & 4)	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	± 10.0	uA

Notes: 2. Outputs will drive CMOS logic levels into a CMOS load.
3. I_{out} = -40 µA
4. I_{out} = 1.6 mA

Specifications subject to change without notice.

ANALOG CHARACTERISTICS (T_A = -40°C to 85°C; V+ = 5V ± 10%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
Power Dissipation	P_D	-	50	85	mW
Input Jitter Tolerance		7	-	14*	Unit Intervals

* Depends on accuracy of crystal with respect to CLKIN frequency. See *Applications* section.

3

SWITCHING CHARACTERISTICS (T_A = -40°C to 85°C; V+ = 5V ± 10%; GND = 0V)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	T1	f_c	-	6.176000	-	MHz
	CCITT (Note 5)		-	8.192000	-	
CLKIN Frequency	T1	f_{in}	-	1.544	-	MHz
	CCITT (Note 6)		-	2.048	-	
CLKOUT Frequency	T1	f_{out}	-	1.544	-	MHz
	CCITT (Note 6)		-	2.048	-	
Clock Pulse Width	T1	t_{pwh}	-	324	-	ns
		t_{pwl}	-	324	-	
	CCITT	t_{pwh}	-	244	-	ns
	(Note 7)	t_{pwl}	-	244	-	
Acceptable CLKIN range	(Note 8)		-	±130	-	ppm
Duty Cycle	(Note 9)		-	50	-	%
Rise Time, All Digital Outputs	(Note 10)	t_r	-	36	100	ns
Fall Time, All Digital Outputs	(Note 10)	t_f	-	17	100	ns
DIN to CLKIN Falling Setup Time		t_{su}	30	-	-	ns
CLKIN Falling to DIN Hold Time		t_h	50	-	-	ns
CLKOUT Falling To DOUT Propagation Delay		t_{phl}	-	-	200	ns

Note:
5. Crystal should have sufficient pull range when in the oscillator circuit, to meet the system's frequency tolerance requirement over the operating temperature range. See *Applications* section for more information on crystals.
6. Although CLKIN and CLKOUT will vary in instantaneous frequency (jitter) over time, CLKOUT will have the same average frequency as CLKIN.
7. The sum of the pulse widths must always meet the frequency specifications.
8. Crystal must have at least ± 130ppm pull range over operating temperature range.
9. Duty cycle is (t_{PWH} / (t_{PWH} + t_{PWL})) x 100%.
10. At C_L = 50pF.

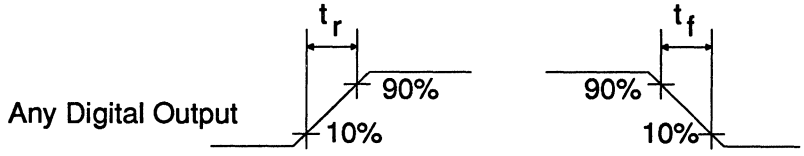


Figure 1. Signal Rise and Fall Characteristics

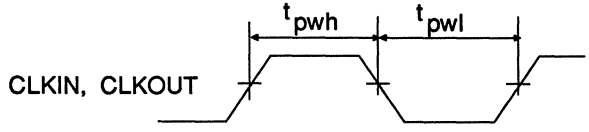


Figure 2. Clock Signal Quality

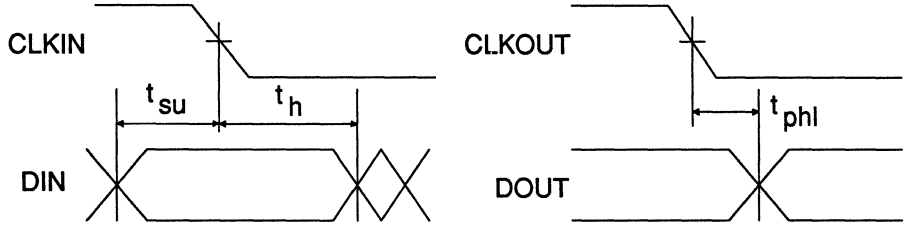


Figure 3. Switching Characteristics

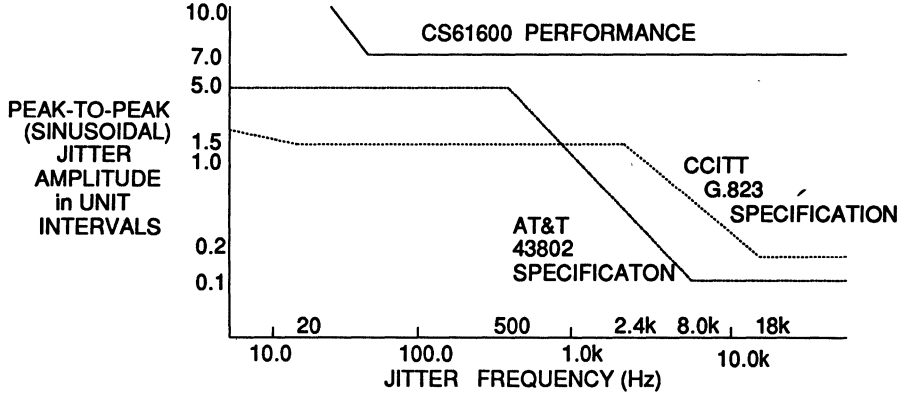


Figure 4. Input Jitter Tolerance

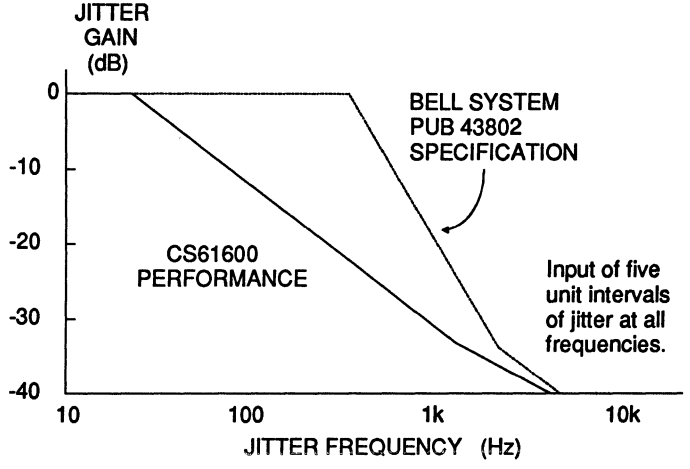


Figure 5. Jitter Attenuation Characteristic

CIRCUIT DESCRIPTION

Jitter Attenuation

The CS61600 will tolerate and attenuate at least seven unit intervals of jitter from clock and data signals of 1.544 MHz and 2.048 MHz. An external clock divide circuit can be added for jitter attenuation for lower frequency signals. Jitter attenuation is accomplished by means of a FIFO and a variable oscillator. The frequency of the oscillator is controlled by logic in the CS61600 to be the same as the average of the input clock signal, CLKIN. Signal jitter is absorbed in the FIFO.

The FIFO's write pointer is controlled by the CLKIN signal. Data present on DIN is written into the memory location selected by the write pointer. The CLKOUT signal corresponds to the FIFO's read pointer and is controlled by the crystal oscillator. Internal logic determines the relationship of the read pointer and the write pointer, and adjusts the speed of the oscillator. For example, if the CLKIN signal is at a higher frequency than the CLKOUT signal, the write pointer will start to catch up with the read pointer. When this situation is detected, the capacitive loading the device presents to the crystal is reduced, resulting in an increase in oscillator frequency and read pointer (CLKOUT) frequency. The oscillator frequency is periodically updated and adjusted to maintain the FIFO at half full. High frequency variations in the phase of the CLKIN signal (jitter) are absorbed in the FIFO.

There are some advantages to this method of jitter attenuation. The device can tolerate large amplitude jitter at high frequencies. The device can track slow changes of the input clock frequency (wander) and tolerate input frequencies ranging over a specified frequency tolerance.

A by product of this method of jitter attenuation is that the greater the input jitter, the greater the jitter attenuation, and the lower the frequency at which the device starts to attenuate jitter. Conversely, low amplitude jitter receives little attenuation. This performance characteristic is shown graphically in Figure 6.

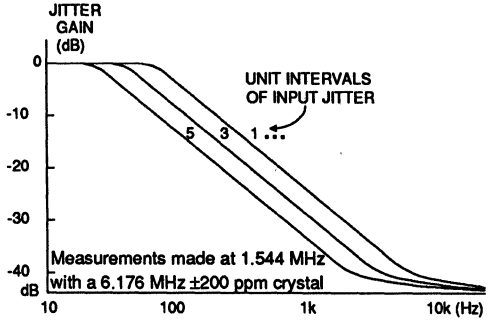


Figure 6. Jitter Attenuation Characteristics

CCITT Jitter Attenuation

The CS61600 can be used in CCITT applications. If rigid crystal specifications are met, the attenuation performance of the CS61600 will meet the requirements of REC. G. 742 as shown in Figure 7. The crystal, when placed in the oscillator circuit in parallel with a 25 pF, 2%, NPO capacitor, must have a frequency pull range of at least ± 50 ppm, and at most ± 66 ppm. The crystal must also be insensitive to changes in temperature to ensure that the system frequency tolerances are always met over the system's operating temperature range.

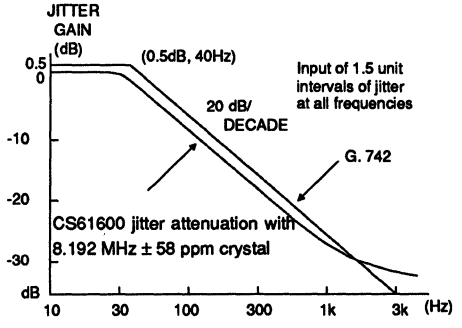


Figure 7. - CCITT Jitter Attenuation Characteristics

Crystal Semiconductor is presently working with crystal manufacturers to establish a crystal that will meet these requirements. Contact the factory or your local sales representative for more information.

Using the CS61600 in a Slave Configuration

It is possible to use an externally generated clock signal to clock data out of the CS61600. When an external clock is used, a crystal is not necessary. The external clock is input to the Alternate Read Clock input, ARC (pin 12). Holding the Alternate Read Enable pin, ARE (pin 6), high directs the CS61600 to clock data out of the FIFO at the rate determined by ARC. Unless the clock signal on ARC is at exactly the same average frequency as the clock signal on CLKIN, the CS61600 will be prone to underflow or overflow, and data will be lost. See the *Applications* section of this data sheet for more information on the use of an alternate clock.

Oscillator and Crystal

The CS61600 requires an external 6.176000 MHz (8.192000 MHz for CCITT) crystal be connected to pins XTALOUT (pin 5) and XTALIN (pin 4). The oscillator circuit divides the crystal frequency by four, and switches various capacitive loads to provide a clock that swings in five steps from at least 1.544MHz - 130 ppm to at least 1.544 MHz + 130 ppm (2.048 MHz - 50 ppm to 2.048 MHz + 50 ppm for CCITT). The crystal oscillator must be able to reach these signal frequency tolerances over the system's operating temperature range. The oscillator adjusts to and holds the average frequency of the signal input to CLKIN.

Some applications specify a narrower frequency tolerance. In these cases, it is possible to improve jitter attenuation performance by specifying a crystal with less pull range. A narrow pull range crystal has the effect of shifting the curves shown in Figure 6 to the left. Care must be taken to ensure that the crystal/oscillator will reach the signal's frequency extremes over the operating temperature range of the system. More information on specifying and testing crystals is provided in the *Applications* section at the back of this data sheet.

FIFO Overflow/Underflow

Because the oscillator clock, which is used to empty the FIFO, has a wider frequency range than the standard T1 input signal, the FIFO should never underflow or overflow. However, if underflow or overflow occurs, the buffer overflow/underflow flag, OVR (pin 3), goes high. A $\overline{\text{RESET}}$ (pin 1) resets the overflow flag. If an overflow occurs, the 16 bits of data in the FIFO are lost. An underflow condition causes the next 16 bits read from the FIFO to be invalid. In either case, the CS61600 will immediately attempt to relock on to the clock signal. Holding $\overline{\text{RESET}}$ low disables the overflow flag, OVR.

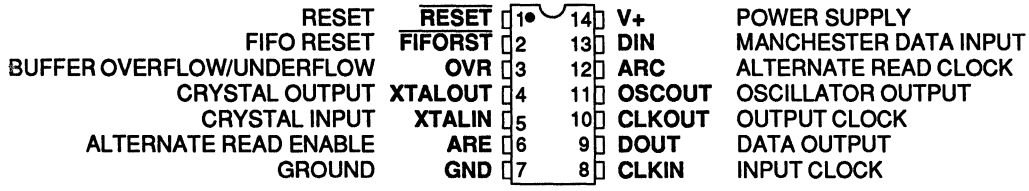
FIFO Reset

Taking the $\overline{\text{FIFORST}}$ pin low causes most of the subcircuits of the CS61600 to go into a reset state. These circuits will remain in a reset condition until $\overline{\text{FIFORST}}$ is returned to a logic 1 state. This function will set the FIFO write and read pointers to the first and eighth locations respectively. The oscillator will continue to run and CLKOUT will be held low.

Power-Up Reset

Upon power up, the CS61600 goes through an initialization procedure which requires approximately 3 ms. During this initialization procedure, OVR is held high. After initialization is complete, OVR goes low. When the clock signal is input to CLKIN, the CS61600 will immediately try to lock onto the clock signal on CLKIN. At this point, the FIFO may overflow, and the $\overline{\text{RESET}}$ pin should be toggled to clear the overflow/underflow flag, OVR.

PIN DESCRIPTIONS



Power Supplies

V+ - Positive Power Supply, PIN 14.
Typically +5V volts.

GND - Ground, PIN 7.
Ground reference.

Oscillator

XTALIN, XTALOUT - Crystal Input 1, 2; PINS 5, 4.
6.176 MHz or 8.192 MHz crystal inputs. A 200 kohm resistor should be connected across these pins. There is no need for external capacitors. The crystal should be connected to XTALIN and XTALOUT with minimal length traces on the pc board.

Control

$\overline{\text{RESET}}$ - Reset, PIN 1.
When $\overline{\text{RESET}}$ is taken low, the OVR signal is reset.

$\overline{\text{FIFORST}}$ - FIFO Reset, PIN 2.
Taking $\overline{\text{FIFORST}}$ low resets the read and write pointers of the FIFO. Resetting the pointers will cause some data loss. When $\overline{\text{FIFORST}}$ is low, the OSCOUT output is disabled.

ARE - Alternate Read Enable, PIN 6.
For normal operation, ARE is held at logic 0. In this configuration the oscillator controls the read pointer of the FIFO. When ARE is at logic 1, the read pointer of the FIFO will be controlled by the clock signal on pin 12, ARC.

Inputs

CLKIN - Clock Input, PIN 8.
Clock for the data input. This clock contains the jitter to be removed.

DIN - Data Input, PIN 13.

Input data is sampled on the falling edge of CLKIN.

ARC - Alternate Read Clock, PIN 12.

When ARE, Pin 6, is at logic 1, a clock signal on ARC will control the FIFO's read pointer. CLKOUT, pin 10, will be at the same frequency and phase as ARC. Setting ARE to logic 0 results in the device using its oscillator to generate CLKOUT.

Outputs

OVR - Buffer Overflow/Underflow, PIN 3.

Goes high if the FIFO overflows or underflows, and is cleared by $\overline{\text{RESET}}$.

DOUT - Data Output, PIN 9.

Output data with jitter attenuated. DOUT is stable and valid on the rising edge of CLKOUT.

CLKOUT - Output Clock, PIN 10.

Jitter reduced clock output corresponding to the data on DOUT.

OSCOUT - Oscillator Output, Pin 11.

Output of on-chip oscillator, divided by four. This pin should be left floating for normal operation.

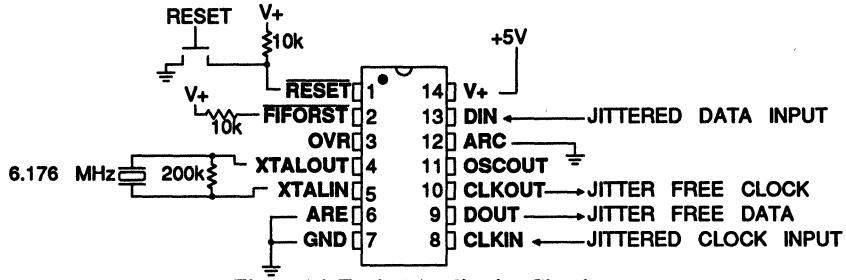


Figure A1. Typical Application Circuit

APPLICATIONS

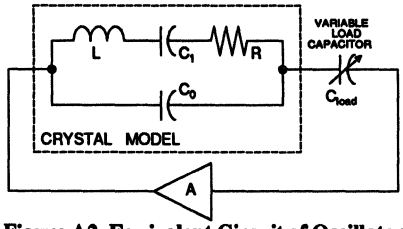


Figure A2. Equivalent Circuit of Oscillator

Selecting an Oscillator Crystal

Figure A2 shows an equivalent representation of the oscillator circuit. The variable load capacitor is internal to the CS61600. The value of this capacitor is controlled by logic internal to the CS61600. Based on this model, Equations 1 and 2 have been developed to help calculate the required crystal parameters necessary to meet system requirements.

Two important parameters in this model are the upper and lower bounds of C_{load} (the variable load capacitor) and the value of C_o. C_o can be used to control the series resonant frequency of the crystal. The minimum value of C_{load} sets the maximum parallel resonant frequency. Together, C_o and C_{load} can be used to set the pull range of the oscillator and its maximum and minimum frequencies.

Determining Required Pull Range

Four factors contribute to the required pull range of the crystal:

1) The frequency range required for the application,

2) The frequency drift of the crystal over the operating temperature range,

3) The variability in load capacitance from IC to IC,

4) The accuracy to which the crystal can be manufactured.

All of these factors have been measured or can be controlled.

For a given crystal geometry, the series resonant frequency of the crystal is inversely proportional to C_o. The relationship of the crystal's series resonant frequency to its parallel resonant frequency in the oscillator circuit determines the pull range of the oscillator. The further away the series resonant frequency is from the parallel resonant frequency (which is set by the load condition in the oscillator circuit) the greater the pull range of the crystal. That is: a smaller C_o (greater series resonant frequency) results in less pull

range, while the larger the C_O (lower series resonant frequency), the larger the pull range.

The series resonant frequency of the crystal is calculated by Equation 1.

$$f_S = f_N - \frac{\Delta f}{2(C_L - C_H)} \quad (C_L + C_H + 2C_O)$$

Equation 1.

f_S = series resonant frequency of crystal
f_N = 4 x Nominal Signal Frequency
- should be 6.176000 MHz for North America (T1)
- should be 8.192000 MHz for Europe (CEPT)

Δf = required pull range of crystal in Hz (Δ ppm x f_N)
C_L = load capacitance for low frequency oscillation (average is ~38.0 pF)
C_H = load capacitance for high frequency oscillation (average is ~11.0 pF)

The parallel resonant frequency is calculated by Equation 2.

$$f_{load} = f_S \left(\frac{C_1 + C_{load} + C_0}{C_{load} + C_0} \right) 1/2$$

Equation 2.

Table A1 shows the crystal frequency as a function of load capacitance. The deviation in frequency from the nominal is shown in ppm. Temperature drift has been accounted for as shown. *The accuracy to which C_O can be controlled, and the accuracy to which a crystal can be trained or calibrated should be factored in to guarantee that the required frequency range will be met.*

	T1	CEPT
Frequency Tolerance / C_L in pf	6.176000 MHz ±130 ppm or less	8.192000 MHz ±50 ppm or less
$C_{low\ freq}$ min 34.0	6175197 - Δtd	8191590 - Δtd
$C_{high\ freq}$ max 11.7	6176803 + Δtd	8192410 + Δtd
MAXIMUM ALLOWABLE PULL RANGE	390 ppm	230 ppm

Δ_{td} = crystal temperature drift from -40 to +85 deg. C.

Table A1. T1 and CEPT Requirements

The 8.192 MHz crystal specified in Table A1 meets CCITT data rates and frequency tolerance requirements and will attenuate jitter. However, this crystal will not meet CCITT Rec. G. 742 jitter attenuation specifications.

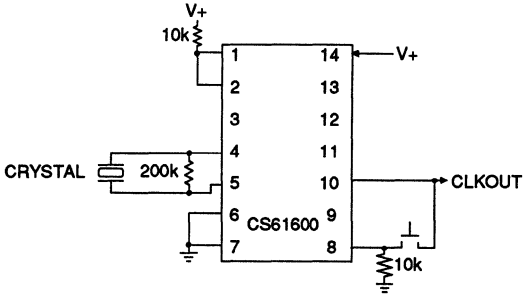


Figure A3. Crystal Pull Range Test

The setup shown in Figure A3 can be used to test crystals. When no CLKIN signal is applied to the device, the oscillator will tend to pull to one extreme of its pull range. Momentarily pressing the push button moves the relative positions of the FIFO pointers and if the write pointer stops (when the push button opens) in the right relationship to the read pointer, the oscillator will pull to the other end of its range. It may take a few tries.

General Applications

The CS61600 will tolerate and attenuate at least seven unit intervals of jitter over the specified range of input clock and oscillator frequencies. If the oscillator crystal is chosen so that the center frequency of its pull range is close to the input frequency, CLKIN, the CS61600 will tolerate

more jitter; up to 14 unit intervals will be tolerated under optimal conditions.

Consider the case where the average clock frequency at CLKIN approaches the slow end of the range, 1.544 MHz - 130 ppm. In this case, the oscillator will be near the bottom of its pull range, restricting its ability to achieve frequencies well below the CLKIN frequency. The result is that the read pointer of the FIFO will begin to catch up to the write pointer. If enough jitter is introduced, the read pointer will overtake the write pointer resulting in an error (i.e. the device will try to read out data before it is written in). A similar situation occurs when the CLKIN signal approaches the fast end of its range, 1.544 MHz + 130 ppm.

Taking care in selecting the proper crystal can result in improved jitter tolerance without degrading the performance of the CS61600. If the center frequency of the oscillator is precisely four times the CLKIN frequency, and the crystal has at least the specified pull range, the CS61600 will tolerate 14 unit intervals of jitter. In this case, the read and write pointers of the FIFO will maintain optimal separation when the signal is jitter free, allowing the device to tolerate maximum jitter input.

Master/Slave Configuration

Some T1 applications require separate representations of the positive and negative going pulses for an AMI signal. Two CS61600s can be used to remove jitter from a set of signals consisting of POS, NEG and CLK. Figure A4 shows the master/slave configuration.

This configuration requires one crystal (on the master). The CLKOUT signal from the master controls the FIFO read pointer of the slave CS61600. Setting ARE, pin 6, of the slave to logic 1 directs the device to use the clock input to ARC, pin 12, to control the FIFO read pointer. For this configuration to function properly, the positions of the FIFO the read and write pointers in both devices must correspond. The FIFO pointer reset, $\overline{\text{FIFORST}}$, of both devices must be tied together. After the power supplies have stabilized, and the clock has been input at CLKIN, $\overline{\text{FIFORST}}$ should be momentarily pulled low to reset the pointers of both devices. The overflow flags should then be reset by momentarily pulling $\overline{\text{RESET}}$, pin 1, low.

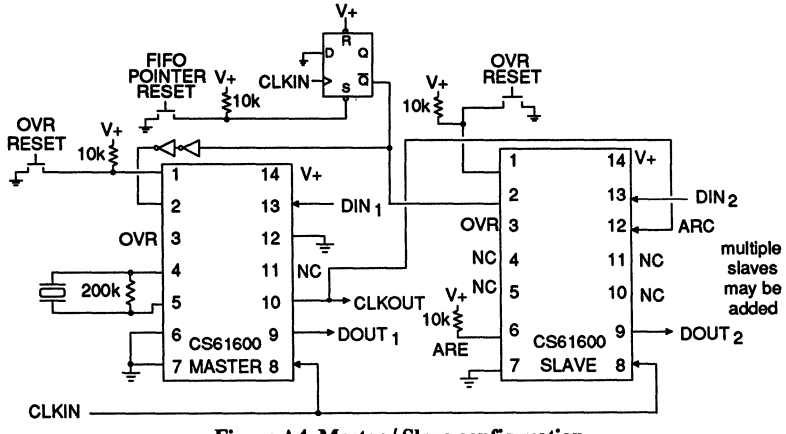


Figure A4. Master / Slave configuration

Additional slaves may be added. The ARC input may be derived from either the CLKOUT pin on the master, or the CLKOUT pin on a preceding slave. When using the master's CLKOUT pin, the fan out must be considered. Attaching several inputs to the CLKOUT pin increases the load that the output must drive. The added capacitance will reduce the switching speed of the output driver. Similarly, a configuration which uses the CLKOUT signal of each CS61600 to drive the subsequent CS61600 will induce some propagation delay. These potential timing problems should be considered when cascading CS61600s.

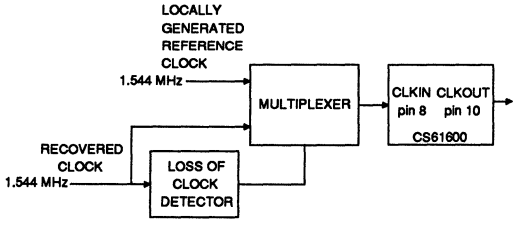


Figure A5. Maintaining Clock Integrity

Maintaining Clock

Many applications require that the clock signal from CLKOUT be maintained within some specified range of frequencies when the clock signal on CLKIN (often generated from a recovered T1 signal clock) goes away. Figure A5 shows one method for maintaining the CLKOUT signal. The reference clock is a locally generated clock whose frequency lies within the tolerance of the applicable specifications which govern the system's design. When the CLKIN signal goes away, the multiplexor should switch in the reference clock. Since this clock goes through the jitter attenuator, phase and frequency integrity at CLKOUT is maintained.

Jitter Attenuation at Different Clock Rates

The CS61600 can be used to attenuate jitter at frequencies below 2.048 MHz. For signal frequencies above about 900 kHz, selection of the appropriate crystal will suffice. For jitter attenuation of lower frequency signals, an external divider is required. Figure A6 shows how the CS61600 can be configured for low frequency jitter attenuation.

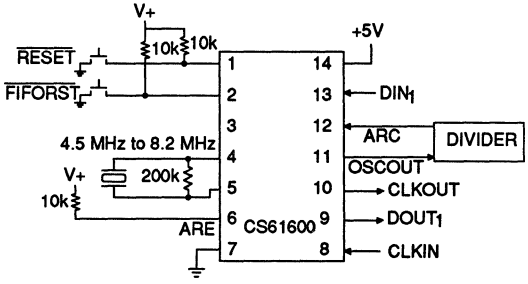


Figure A6. Low Clock Frequency Jitter Attenuation

Frequency tolerance of the input signal is still based on the pull range of the crystal in ppm. For example, a 64 kbps jitter attenuator which uses an external divide by 32, and a 8.192 MHz crystal with ± 200 ppm pull range will have ± 200 ppm tolerance at 64 kbps or ± 12.8 Hz.

3

• Notes •

Semiconductor Corporation

CS80600

High Speed Jitter Attenuator

Features

- Accepts Input Clock with Frequency of 4.5 MHz to 8.5 MHz
- Unique Clock-Tracking Circuitry
- Tolerates and Attenuates At Least 3 Unit Intervals of Jitter
- Minimal External Components Required
- 14 Pin DIP
- Single 5 Volt Supply
- 3 Micron CMOS For High Reliability And Low Power Dissipation: 50 mW Typical At 25°C

General Description

The CS80600 from Crystal Semiconductor accepts 4.5 to 8.5 MHz clock and data inputs, and removes up to plus or minus three data bits of jitter before outputting the data and clock. Jitter is removed using an internal clock tracking circuit and an 8-bit FIFO elastic store.

Applications

Token Ring: The CS80600 can be used to eliminate the accumulation of data-pattern dependent jitter which is the primary factor limiting the size of token rings. The CS80600 is intended for application in station adaptor cards, in active wiring concentrators and in repeaters.

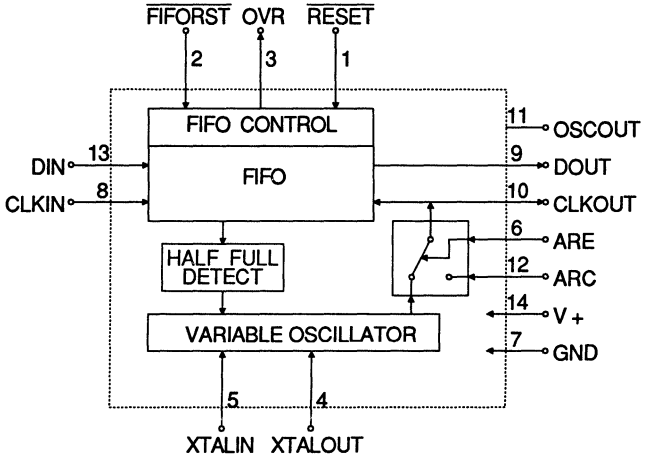
PCM: TIC, T2 & CEPT2 and second order multiplexors.

ORDERING INFORMATION

CS80600-P - 14 Pin Plastic DIP

3

Block Diagram



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, Texas 78760
(512)445-7222 TWX:910-874-1352

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply	V+ - GND	-	7.0	V
Input Voltage	V_{in}	GND - 0.3	V+ + 0.3	V
Input Current, Any Pin (Note 1)	I_{in}	-	100	mA
Ambient Operating Temperature	T_A	- 40	85	°C
Storage Temperature	T_{stg}	- 65	125	°C

Note: 1. Device can tolerate transients of up to 100mA without latching up.

WARNING: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply	V+	4.5	5.0	5.5	V
Ambient Operating Temperature	T_A	-40	25	85	°C
Power Dissipation	P_D	20	50	85	mW
Input Jitter Tolerance	-	3	-	7	Unit Intervals

DIGITAL CHARACTERISTICS (T_A = 0°C to 70°C; V+ = 5V ± 10%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 2 & 3)	V_{OH}	2.4	-	-	V
Low-Level Output Voltage (Note 2 & 4)	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	±10.0	uA

Notes: 2. Outputs will drive CMOS logic levels into a CMOS load.
3. I_{out} = -40 µA
4. I_{out} = 1.6 mA

Specifications subject to change without notice.

SWITCHING CHARACTERISTICS (T_A = 0°C to 70°C; V+ = 5V ± 10%; GND = 0V)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency	(Note 5)	f_c	4.500	-	8.500	MHz
CLKIN Frequency	(Note 6)	f_{in}	-	f_c	-	MHz
CLKOUT Frequency	(Note 6)	f_{out}	-	f_c	-	MHz
Clock Pulse Width		t_{pwl}	-	$1/(2f_c)$	-	ns
	(Note 7)	t_{pwl}	-	$1/(2f_c)$	-	ns
Duty Cycle	(Note 8)	-	-	50	-	%
Rise Time, All Digital Outputs	(Note 9)	t_r	-	36	-	ns
Fall Time, All Digital Outputs	(Note 9)	t_f	-	17	-	ns
DIN to CLKIN Falling Setup Time		t_{su}	30	-	-	ns
CLKIN Falling to DIN Hold Time		t_h	50	-	-	ns
CLKOUT Rising To DOUT Propagation Delay		t_{phl}	-	-	60	ns
$\overline{\text{RESET}}$ Pulse Width		-	100	-	-	ns
$\overline{\text{FIFORST}}$ Pulse Width		-	100	-	-	ns

Note:
5. Crystal must meet specifications described in *Applications* Section of this data sheet.
6. Although CLKIN and CLKOUT will vary in instantaneous frequency (jitter), over time CLKOUT will have the same average frequency as CLKIN.
7. The sum of the pulse widths must always meet the frequency specifications.
8. Duty cycle is (t_{PWH} / (t_{PWH} + t_{PWL})) x 100%.
9. At maximum load of 1.6mA and 50pF.

3

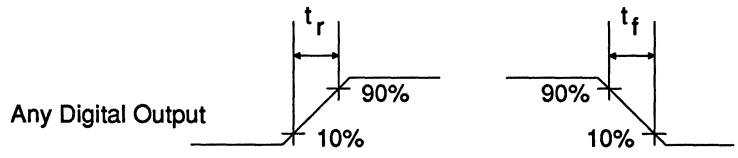


Figure 1. Signal Rise and Fall Characteristics

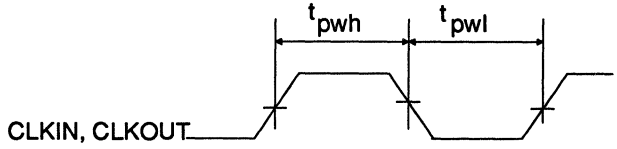


Figure 2. Clock Signal Quality

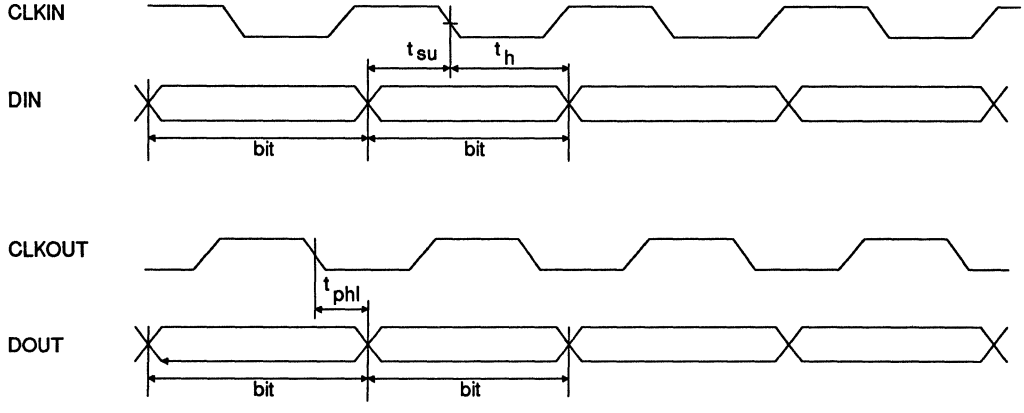


Figure 3. Switching Characteristics

CIRCUIT DESCRIPTION

Jitter Attenuation

The CS80600 will tolerate and attenuate at least three unit intervals of jitter from a 4.5MHz to 8.5MHz data and clock signal. An external clock divide circuit can be added for jitter attenuation for lower frequency signals. Jitter attenuation is accomplished by means of a FIFO and a variable oscillator. The frequency of the oscillator is controlled by logic in the CS80600 to be the same as the average of the input clock signal, CLKIN. Signal jitter is absorbed in the FIFO.

The FIFO's write pointer is controlled by the CLKIN signal. Data present on DIN is written into the memory location selected by the write pointer. The CLKOUT signal corresponds to the FIFO's read pointer and is controlled by the crystal oscillator. Internal logic determines the relationship of the read pointer and the write pointer, and adjusts the speed of the oscillator. For example, if the CLKIN signal is at a higher frequency than the CLKOUT signal, the write pointer will start to catch up with the read pointer. When this situation is detected, the capacitive loading the device presents to the crystal is reduced, resulting in an increase in oscillator frequency and read pointer (CLKOUT) frequency. The oscillator frequency is periodically updated and adjusted to maintain the FIFO at half full. High frequency variations in the phase of the CLKIN signal (jitter) are absorbed in the FIFO.

There are some advantages to this method of jitter attenuation. The device can tolerate large amplitude jitter at high frequencies. The device can track slow changes of the input clock frequency (wander) and tolerate input frequencies ranging over a specified frequency tolerance.

A by product of this method of jitter attenuation is that the greater the input jitter, the greater the jitter attenuation, and the lower the frequency at which the device starts to attenuate jitter. Conversely, low amplitude jitter recieves little attenuation. This performance characteristic is shown graphically in Figure 4.

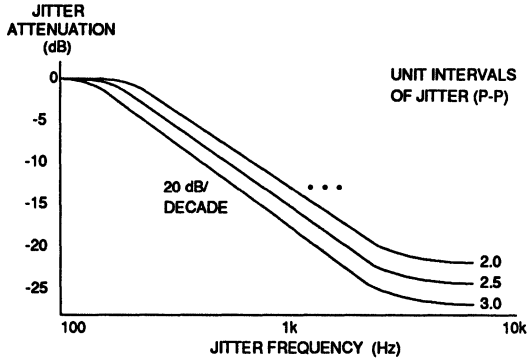


Figure 4 - Jitter Attenuation Characteristics for 8MHz Nominal Frequency

Clock Operation

The CS80600 requires an external crystal. Exacting crystal specifications must be met to ensure proper operation of the curcuit. Information on specifying crystals for the CS80600 is provided in the *Applications* section which appends this data sheet.

It is possible to use an externally generated clock signal to clock data out of the CS80600. The external clock is input to the Alternate Read Clock input, (ARC, pin 12). Holding the Alternate Read Enable pin high (ARE, pin 6), directs the CS80600 to clock data out of the FIFO at the rate determined by ARC. Unless the clock signal on ARC is at exactly the same average frequency as the clock signal on CLKIN, the CS80600 will be prone to underflow or overflow and data will be lost.

FIFO Overflow/Underflow

If underflow or overflow occurs, the buffer overflow/underflow flag, OVR (pin 3), goes high. A $\overline{\text{RESET}}$ (pin 1) resets the overflow flag. If an overflow occurs, the eight bits of data in the FIFO are lost. An underflow condition causes the next eight bits read from the FIFO to be invalid. In either case, the CS80600 will immediately attempt to relock on to the clock signal. Holding $\overline{\text{RESET}}$ low disables the OVR flag.

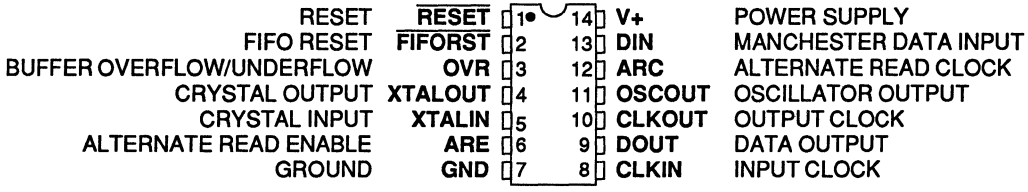
FIFO Reset

Taking the $\overline{\text{FIFORST}}$ pin low causes most of the subcircuits of the CS80600 to go into a reset state. These circuits will remain in a reset condition until $\overline{\text{FIFORST}}$ is returned to a logic 1 state. This function will set the FIFO write and read pointers to the first and fourth locations respectively. The oscillator will continue to run and CLKOUT will continue to be output.

Power-Up Reset

Upon power up, the CS80600 goes through an initialization procedure which requires approximately 3 ms. During power-up reset, the overflow pin, OVR, is held high. When initialization is complete, the OVR pin goes low and the CS80600 is ready to lock on to an input clock signal on CLKIN.

PIN DESCRIPTIONS



Power Supplies

V+ - Positive Power Supply, PIN 14.
Typically +5V volts.

GND - Ground, PIN 7.
Ground reference.

Oscillator

XTALOUT; XTALIN - Crystal Output; Crystal Input; PINS 4, 5.
A 20 kΩ resistor should be connected across these pins parallel with the crystal. There is no need for external capacitors. The crystal should be connected to XTALIN and XTALOUT with minimal length traces on the pc board.

Control

$\overline{\text{RESET}}$ - Reset, PIN 1.
When $\overline{\text{RESET}}$ is taken low, the OVR signal is reset.

$\overline{\text{FIFORST}}$ - FIFO Reset, PIN 2.
Taking $\overline{\text{FIFORST}}$ low resets the read and write pointers of the FIFO. Resetting the pointers will cause some data loss.

ARE - Alternate Read Enable, PIN 6.
For normal operation, ARE is held at logic 0. In this configuration the oscillator controls the read pointer of the FIFO. When ARE is at logic 1, the read pointer of the FIFO will be controlled by the clock signal on pin 12, ARC.

Inputs

CLKIN - Clock Input, PIN 8.
Clock for the data input. This clock contains the jitter to be removed.

DIN - Data Input, PIN 13.

Data input is sampled on the falling edge of CLKIN.

ARC - Alternate Read Clock, PIN 12.

When ARE, Pin 6, is at logic 1, a clock signal on ARC will control the FIFO's read pointer. CLKOUT, pin 10, will be at the same frequency and phase as ARC. Setting ARE to logic 0 results in the device using its oscillator to generate CLKOUT.

Outputs

OVR - Buffer Overflow/Underflow, PIN 3.

Goes high if the FIFO overflows or underflows, and is cleared by $\overline{\text{RESET}}$.

DOUT - Data Output, PIN 9.

Data output with jitter removed. DOUT is stable and valid on the rising edge of CLKOUT.

CLKOUT - Output Clock, PIN 10.

Jitter free clock output corresponding to the data on DOUT.

OSCOUT - Oscillator Output, Pin 11.

Output of the crystal oscillator.

APPLICATIONS

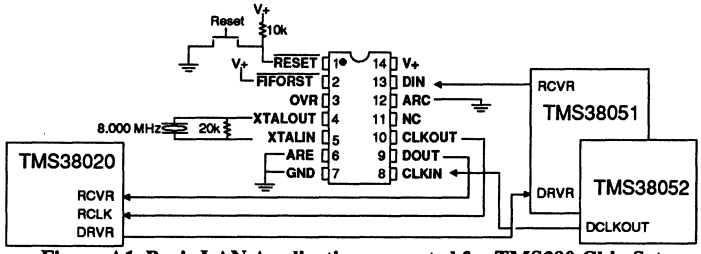


Figure A1. Basic LAN Application suggested for TMS380 Chip Set

3

Token Ring Operation

The CS80600 can be used, as shown in Figure A1 with the TMS380 Token Ring adaptor chip-set in station adaptors, active wiring concentrators and/or repeaters to attenuate jitter that accumulates in a ring. Figure A1 has the effect of masking frequency deviations from the TMS38020 and preventing the "Hardware Error Process" from triggering. In this case, error recovery occurs as the result of higher level procedures.

Figure A2 allows the "Hardware Error Process" to occur. When the CS80600 overflows or underflows, a MUX is used to pass the out-of-frequency clock data around the CS80600 for a fixed number of bits. After those number of bits are passed, the CS80600 is switched back into the circuit. This allows the TMS38020 to observe a wide frequency variation.

Figure A3 shows how the CS80600 can be used to generate a FRAQ signal, thereby allowing the TMS38051/52 PLL to be controlled in a repeater without the use of the TMS38020.

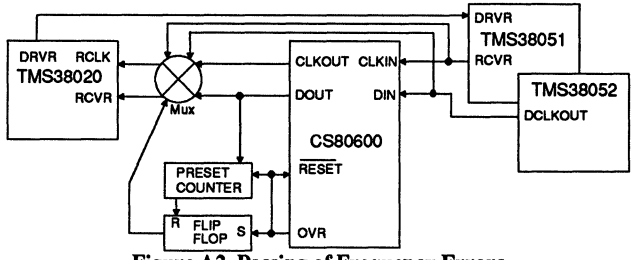


Figure A2. Passing of Frequency Errors

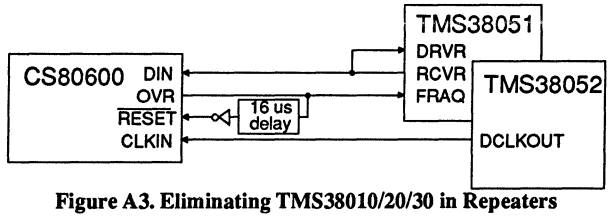


Figure A3. Eliminating TMS38010/20/30 in Repeaters

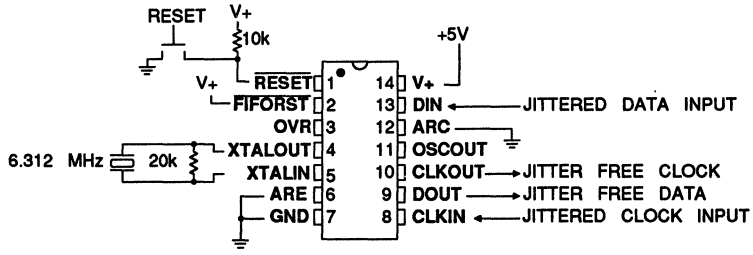


Figure A4. Typical Jitter Attenuation Curcuit

T2 Operation

The CS80600 may be connected as shown in Figure A4 for jitter attenuation in T2 applications.

Selecting an Oscillator Crystal

Figure A5 shows an equivalent representation of the oscillator circuit. The variable load capacitor is internal to the CS80600. The value of this capacitor is controlled by logic internal to the CS80600. Based on this model, equations 1 and 2 have been developed to help calculate the required crystal parameters necessary to meet system requirements.

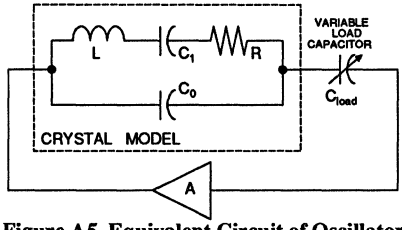


Figure A5. Equivalent Circuit of Oscillator

Two important parameters in this model are the upper and lower bounds of C_{load} (the variable load capacitor) and the value of C_o. C_o can be used to control the series resonant frequency of the crystal. The minimum value of C_{load} sets the maximum parallel resonant frequency. Together, C_o and C_{load} can be used to set the pull range of the oscillator and its maximum and minimum frequencies.

Determining Required Pull Range

Four factors contribute to the required pull range of the crystal:

1) The frequency range required for the application.
2) The frequency drift of the crystal over the operating temperature range.
3) The variability in load capacitance from IC to IC.
4) The accuracy to which the crystal can be manufactured.

All of these factors have been measured or can be controlled.

For a given crystal geometry, the series resonant frequency of the crystal is inversely proportional to C_o. The relationship of the crystal's series resonant frequency to its parallel resonant frequency in the oscillator circuit determines the pull range of the oscillator. The further away the series resonant frequency is from the parallel resonant frequency (which is set by the load condition in the oscillator circuit) the greater the pull range of the crystal. That is: a smaller C_o (greater series resonant frequency) results in less pull range, while the larger the C_o (lower series resonant frequency), the larger the pull range.

The series resonant frequency of the crystal is calculated by Equation 1.

$$f_S = f_N - \frac{\Delta f}{2(C_L-C_H)}(C_L+C_H+2C_0) \quad (C\text{'s in pF}) \quad (1)$$

f_S = series resonant frequency of crystal
f_N = 4 x Nominal Signal Frequency
- should be 8.000000 MHz for LAN
- should be 6.312000 MHz for T2
- should be 8.448000 MHz for CEPT2

Δf = required pull range of crystal in Hz (Δppm x f_N)
C_L = load capacitance for low frequency oscillation (average is ~44.0 pF)
C_H = load capacitance for high frequency oscillation (average is ~9.5 pF)

The parallel resonant frequency is calculated by Equation 2.

$$f_{load} = f_S \left(\frac{C_1+C_{load}+C_0}{C_{load}+C_0}\right)^{1/2} \quad (2)$$

Table A1 shows the crystal frequency as a function of load capacitance. The deviation in frequency from the nominal is shown in ppm. Temperature drift has been accounted for as shown. *The accuracy to which C_0 can be controlled, and the accuracy to which a crystal can be trained or calibrated should be factored in to guarantee that the required frequency range will be met.*

The setup shown in Figure A6 can be used to test crystals. When no CLKIN signal is applied to the device, the oscillator will tend to pull to one extreme of its pull range. Momentarily pressing the push button moves the relative positions of the FIFO pointers and if the write pointer stops (when the push button opens) in the right relationship to the read pointer, the oscillator will pull to the other end of its range. It may take a few tries.

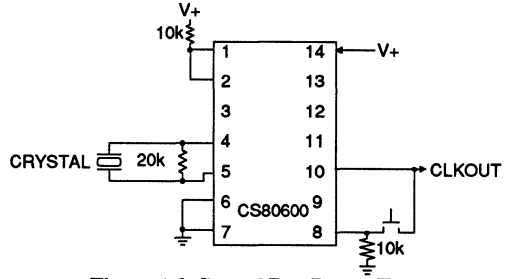


Figure A6. Crystal Pull Range Test

General Applications

The CS80600 will tolerate and attenuate at least three unit intervals of jitter over the specified range of input clock and oscillator frequencies. If the oscillator crystal is chosen so that the center frequency of its pull range is close to the input frequency, CLKIN, the CS80600 will tolerate more jitter; up to seven unit intervals will be tolerated under optimal conditions.

NOMINAL INPUT SIGNAL FREQUENCY
8.000000 MHz

C_L in pf	FREQUENCY TOLERANCE OF INPUT SIGNAL ±100 ppm		
$C_{low\ freq}$ min 41.0	-170 ppm 7998640	$C_{high\ freq}$ max 10.7	+170 ppm 8001360
ASSUMING ±50 ppm TEMPERATURE DRIFT FROM 0°- 70° C			
MAXIMUM ALLOWABLE PULL RANGE: 400 ppm			

CRYSTAL FREQUENCY FOR CORRESPONDING LOAD CAPACITANCE

Table A1. LAN Crystal Requirements

Consider the case where the average clock frequency at CLKIN approaches the slow end of the range, 8.000 MHz - 100 ppm. In this case, the oscillator will be near the bottom of its pull range, restricting its ability to achieve frequencies well below the CLKIN frequency. The result is that the read pointer of the FIFO will begin to catch up to the write pointer. If enough jitter is introduced, the read pointer will overtake the write pointer resulting in an error (i.e. the device will try to read out data before it is written in). A similar situation occurs when the CLKIN signal approaches the fast end of its range, 8.000 MHz + 100 ppm. In either case, the CS80600 will tolerate at least 3 unit intervals of jitter.

Taking care in selecting the proper crystal can result in improved jitter tolerance without degrading the performance of the CS80600. If the center frequency of the oscillator is precisely four times the CLKIN frequency, and the crystal has at least the specified pull range, the CS80600 will tolerate 7 unit intervals of jitter. In this case, the read and write pointers of the FIFO will maintain optimal separation when the signal is jitter free, allowing the device to tolerate maximum jitter input.

Master/Slave Configuration

Some applications require separate representations of the positive and negative going pulses for an AMI signal. Two CS80600s can be used to remove jitter from a set of signals consisting of POS, NEG and CLK. Figure A7 shows the master/slave configuration.

This configuration requires one crystal (on the master). The CLKOUT signal from the master controls the FIFO read pointer of the slave CS80600. Setting ARE, pin 6, of the slave to logic 1 directs the device to use the clock input to ARC, pin 12, to control the FIFO read pointer. For this configuration to function properly, the positions of the FIFO the read and write pointers in both devices must correspond. The FIFO pointer reset, $\overline{\text{FIFORST}}$, of both devices must be tied together. After the power supplies have stabilized, and the clock has been input at CLKIN, $\overline{\text{FIFORST}}$ should be momentarily pulled low to reset the pointers of both devices. The overflow flags should then be reset by momentarily pulling $\overline{\text{RESET}}$, pin 1, low.

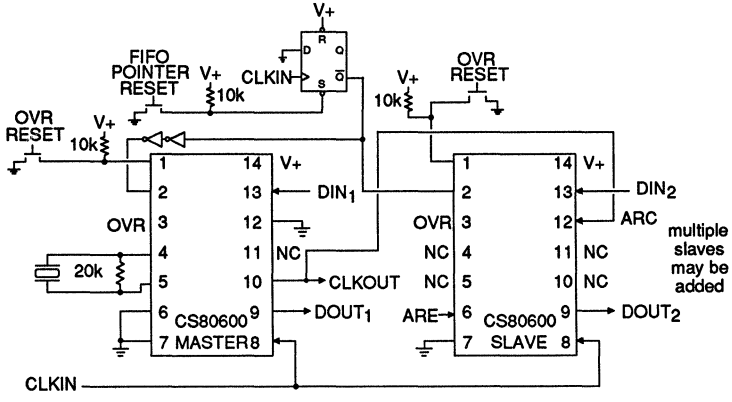


Figure A7. Master/Slave Configuration

Additional slaves may be added. The ARC input may be derived from either the CLKOUT pin on the master, or the CLKOUT pin on a preceding slave. When using the master's CLKOUT pin, the fan out must be considered. Attaching several inputs to the CLKOUT pin increases the load that the output must drive. The added capacitance will reduce the switching speed of the output driver. Similarly, a configuration which uses the CLKOUT signal of each CS80600 to drive the subsequent CS80600 will induce some propagation delay. These potential timing problems should be considered when cascading CS80600s.

Creating Phase Coherent Clocks From Two Clock/Data Streams

The master/slave configuration can be used to align two independent clock/data streams as long as the clocks of both signals are at exactly the same average frequency. The schematic shown in Figure A7 is used to implement this application, but CLKIN signals are independent, not tied together. This application will attenuate jitter as long as the jitter input to either device plus the difference in unit intervals between the clock signals does not exceed seven unit intervals. Note that more jitter can be tolerated if the guidelines described at the beginning of this section are followed.

Maintaining Clock

Many applications require that the clock signal from CLKOUT be maintained within some specified range of frequencies when the clock signal on CLKIN (often generated from a recovered T2 or CEPT2 signal clock) goes away. Figure A8 shows one method for maintaining the CLKOUT signal. The reference clock is a locally generated clock whose frequency lies within the tolerance of the applicable specifications which govern the system's design. When the CLKIN signal goes away, the multiplexor should switch in the reference clock. Since this clock goes through the jitter attenuator, phase and frequency integrity at CLKOUT is maintained.

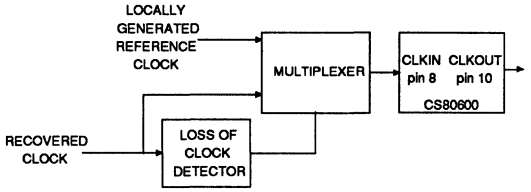


Figure A8. Maintaining Clock Integrity

Jitter Attenuation at Different Clock Rates

The CS80600 can be used to attenuate jitter at frequencies below 4.5 MHz. For signal frequencies above about 4.5 MHz, selection of the appropriate crystal will suffice. For jitter attenuation of lower frequency signals, an external divider is required. Figure A9 shows how the CS80600 can be configured for low frequency jitter attenuation.

Frequency tolerance of the input signal is still based on the pull range of the crystal in ppm. For example, a 64 kbps jitter attenuator which uses an external divide by 32, and a 8.192 MHz crystal with ± 200 ppm pull range will have ± 200 ppm tolerance at 64 kbps or ± 12.8 Hz.

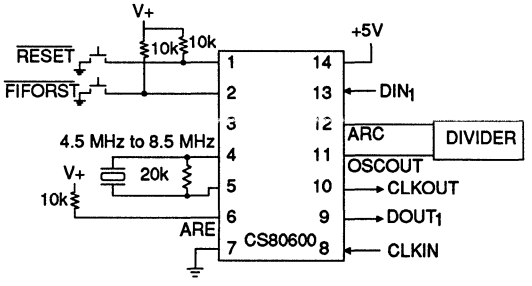


Figure A9. Low Frequency Jitter Attenuation

• Notes •

INTRODUCTION

Crystal's industry-standard DTMF receivers, CS8870, CS202, CS203 and CS204, are available at aggressive pricing while exhibiting performance which exceeds that of competitive devices. The Crystal CS20X family requires half the power of industry alternatives, provides 22 dB more dial-tone rejection and has better latch-up immunity than products available from other vendors. The receivers incorporate filters to guarantee the best possible signal-to-noise ratio. This allows highly accurate decoding of telephone tones into digital outputs.

USER'S GUIDE

Device:	CS202/3 DTMF Receiver	CS204 DTMF Receiver	CS8870 DTMF Receiver
Package Size (# pins)	18	14	18
Signal Sensitivity	-32 dBm	-32 dBm	-29 dBm
Dial Tone Tolerance	22 dB	22 dB	22 dB
Acceptable Twist	10 dB	10 dB	10 dB
Typical Power Consumption	4.5 mA	4.5 mA	6 mA
Tone Pairs Detected	12 or 16	16	16
Output Format	Hex/Binary	Hex	Hex
Package	18 pin DIP	14 pin DIP	18 pin DIP

CONTENTS

Semiconductor Corporation

CS202/3

DTMF Receiver

Features

- Full Receiver Implementation
- Central Office Quality
- Detects 12 or 16 DTMF Tone Pairs
- Uses Inexpensive 3.579 MHz Colorburst Crystal
- Hex or Binary 2-of-8 Output
- Synchronous or Handshake Controlled Output
- Built-in Filter for Dial Tone Rejection
- 18 Pin Package
- Single 5 Volt ±10% Power Supply
- Early detect output (CS203)
- Pin Compatible with SSI 202/SSI 203

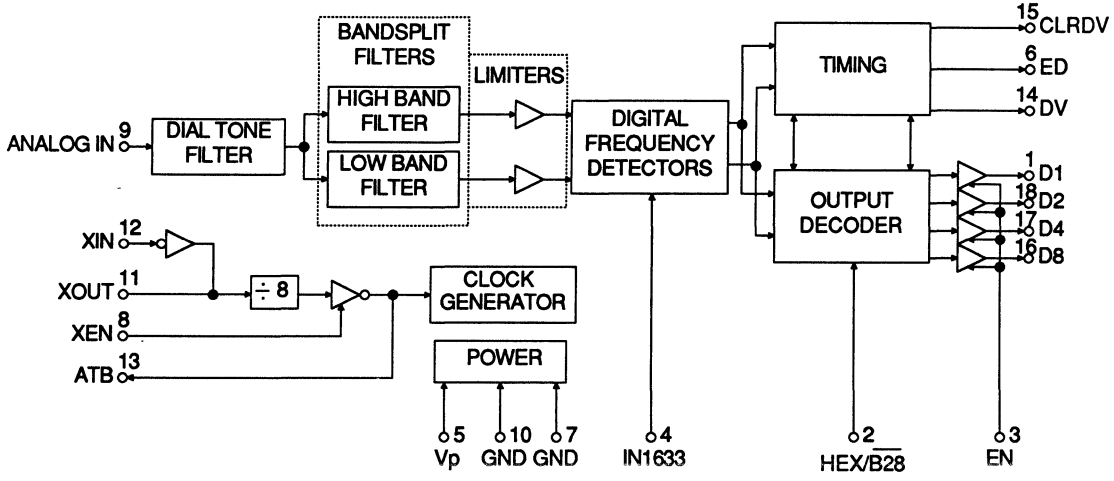
General Description

The CS202 and CS203 are fully integrated DTMF (Dual Tone Multifrequency) receivers that decode the tone pairs used in standard tone dialing schemes. All of the functions needed for decoding the tone pairs are implemented using Crystal's double-poly CMOS process for low power and high performance.

ORDERING INFORMATION
CS202-IP 18 Pin Plastic DIP
CS203-IP 18 Pin Plastic DIP
All standard 300 mil DIPS

4

Block Diagram



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, Texas 78760
(512)445-7222 TWX:910-874-1352

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply	Vp - GND	-	7.0	V
Input Voltage, Any Pin Except Analog in	V_{in}	- 0.5	Vp + 0.5	V
Input Voltage, Analog In	V_{in}	Vp - 10	Vp + 0.5	V
Input Current, Any Pin (Note 1)	I_{in}	-	±10.0	mA
Ambient Operating Temperature	T_A	- 40	85	°C
Storage Temperature	T_{stg}	- 65	150	°C

WARNING: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Note: 1. Transient currents of up to 100 mA will not cause SCR latch-up.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply	V_p	4.5	5.0	5.5	V
Crystal Frequency	F_C	3.5759	3.5795	3.5831	MHz
Ambient Operating Temperature	T_A	0	25	70	°C

DIGITAL CHARACTERISTICS (T_A = 0°C to 70°C; V_p = 5V ± 10%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	0.7Vp	-	Vp	Volts
Low-Level Input Voltage	V_{IL}	0	-	0.3Vp	Volts
High-Level Output Voltage 200 uA Load (Note 2)	V_{OH}	Vp - 0.5	-	Vp	Volts
Low-Level Output Voltage 400 uA Load (Note 2)	V_{OL}	0	-	0.5	Volts

Note: 2. Does not include XOUT.

Specifications subject to change without notice.

ANALOG CHARACTERISTICS (T_A = 0°C to 70°C; V_p = 5V ± 10%)

Parameter	Symbol	Min	Typ	Max	Units
Supply Current (Note 3)	I_p	-	6.0	12	mA
Frequency Detect Bandwidth	BW	± (1.5+2Hz)	±2.3	±3.5	% of f_o
Detection Amplitude (Note 4)	-	- 32	-	- 2	dBm
Twist (Note 5)	-	-	±10	-	dB
60 Hz Tolerance	-	-	0.8	-	V_{rms}
Dial Tone Tolerance (Note 6, 10)	-	-	22	-	dB
Talk Off (Note 7)	-	-	2	-	hits
Power Supply Noise (Note 8)	-	-	10	-	mV_{p-p}
Noise Tolerance (Note 7, 10)	-	-	- 12	-	dB
Input Impedance at ANALOG IN (Note 9)	Z_{in}	100//15	-	-	kohm// pF

Notes:
3. T_A = 25°C
4. Each tone. dBm = decibels above or below a reference power of 1mW into a 600Ω load.
5. Twist = high tone/low tone.
6. Precise dial tone frequencies of 350Hz ± 2% and 440Hz ± 2%.
7. MITEL tape #CM 7290
8. Bandwidth limited (3kHz) Gaussian noise.
9. V_{in} = (V_p - 10V) to V_p
10. Referenced to lower amplitude tone

4

SWITCHING CHARACTERISTICS (T_A = 0°C to 70°C; V_p = 5V ± 10%)

Parameter		Symbol	Min	Typ	Max	Units
Tone Time:	for detect	t_{on}	40	-	-	ms
	for reject	t_{on}	-	-	20	ms
Pause Time:	for detect	t_{off}	40	-	-	ms
	for reject	t_{off}	-	-	20	ms
Detect Time		t_d	25	-	46	ms
Release Time		t_r	25	-	50	ms
Data Setup Time		t_{su}	7	-	-	us
Data Hold Time		t_h	7	9	10	us
DV Clear Time		t_{cl}	-	160	250	ns
CLRDV Pulse Width		t_{pw}	200	-	-	ns
ED Detect Time		t_{ed}	5	-	22	ms
ED Release Time		t_{er}	0.5	-	18	ms
Output Enable Time (Note 11) C_L = 50 pF, R_L = 1 kohm		t_{en}	-	200	300	ns
Output Disable Time (Note 11) C_L = 35 pF, R_L = 500 ohms		t_{dis}	-	150	200	ns
Output Rise Time (Note 11) C_L = 50 pF		t_{rise}	-	200	300	ns
Output Fall Time (Note 11) C_L = 50 pF		t_{fall}	-	160	250	ns

Note: 11. R_L and C_L are parallel impedances.

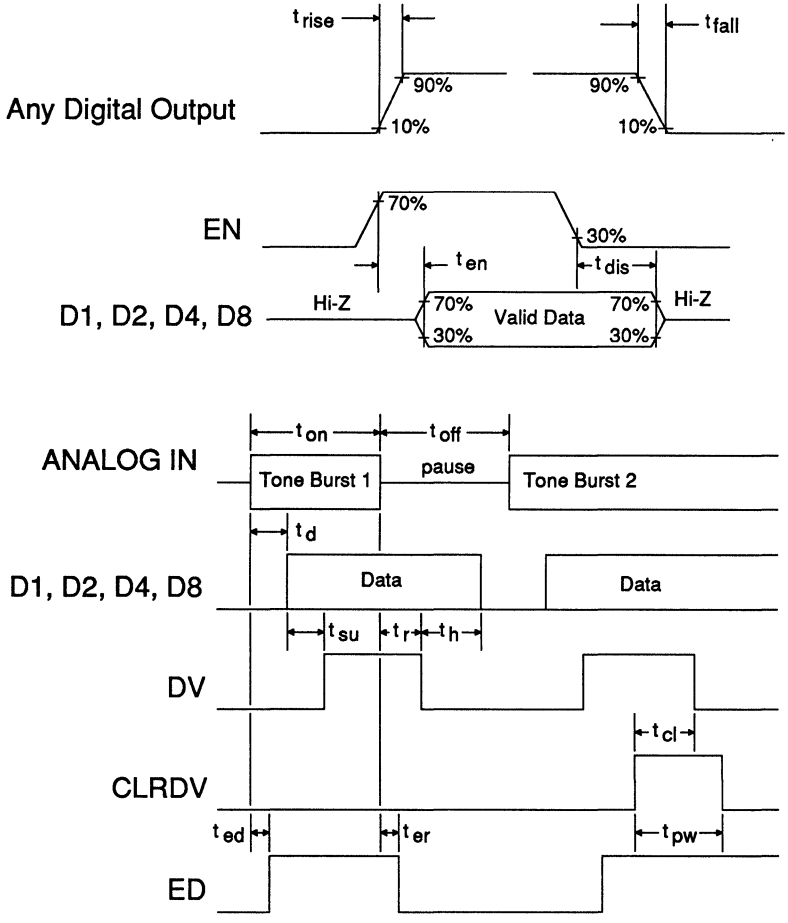


Figure 1 - Timing Diagram

GENERAL DESCRIPTION

The CS202 and CS203 are complete Dual Tone Multifrequency (DTMF) Receivers designed to detect 12 or 16 digits in either a 2-of-7 or 2-of-8 tone selection scheme. These devices provide all of the necessary filtering and require only an external 3.5795 MHz colorburst crystal and a resistor to provide a reference clock. Both devices are designed using a high-density, low-power CMOS technology, and provide the best performance at the lowest cost.

The CS202 and CS203 have filtering on board to guarantee the best signal-to-noise performance possible. The DTMF signal is passed through a dial tone reject filter to reduce dial tone interference, and is then separated into low and high groups using two bandsplit filters. The output of each bandsplit filter contains frequency components from only one DTMF tone group.

Table 1 - DTMF Dialing Matrix

Low-Band	High-Band			
	Column 1 1209 Hz	Column 2 1336 Hz	Column 3 1477 Hz	Column 4 1633 Hz
Row 1 697 Hz	1	2	3	A
Row 2 770 Hz	4	5	6	B
Row 3 852 Hz	7	8	9	C
Row 4 941 Hz	*	0	#	D

For a valid DTMF signal to be detected, each group must simultaneously contain only one valid DTMF tone. Detection of the two tones is accomplished with a digital algorithm. The sinusoidal filter output waveforms pass through a pair of hard limiters. The decoder takes the resultant square waves and measures their periods. This period measurement varies with jitter created by any extraneous signals within the signal passed to the limiter. The period measurement is averaged over a number of cycles and compared to a range of period measurements representing the three or four expected tones. If both bands have a valid tone decoded, the ED signal (CS203 only) will go high.

After two valid tones have been recognized by the decoder, the tones are subjected to a detect timing cycle. The two tones must remain valid for 20 to 40 ms for DV to go high, indicating that a valid digit has been decoded. This prevents voices or other in-band noise from creating a false trigger.

After a valid digit is indicated, the timing circuit will then enable a timing chain that detects drop-outs. If a signal drop of less than 20 ms duration occurs, it will be ignored. This timing prevents false triggering due to keybounce or other signal interruptions. Any drop-out in excess of 40 ms is considered a valid release; the receiver is reset (DV goes low), and all decoded outputs are cleared for the next decode.

Interfacing to the CS202 and CS203

The CS202 and CS203 have analog, data and control interfaces. The analog interface determines how an analog voice channel is connected. The data interface controls the method of extracting output data. The control interface determines what signals are detected and how they are presented to the data interface.

The analog interface consists of only one signal: ANALOG IN. The ANALOG IN signal can be either DC-coupled or AC-coupled using a 0.01µF capacitor. Care must be taken not to exceed the voltage requirements of the pin. It is also desirable to add a simple RC lowpass filter to bandlimit the input to the voice band (100 Hz to 3.4 kHz) so that high frequency noise near the 55.9 kHz internal sampling frequency is not aliased into the voice band by the internal switched-capacitor filters.

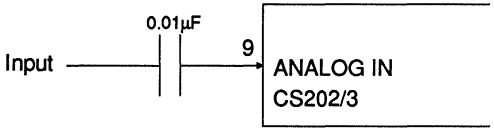


Figure 2 - AC - Coupled Input

The data interface is structured as either a strobed (synchronous) or handshake output. In the strobe mode, CLRDV is held low and DV is used as a data clock to strobe valid information from the data pins (D1, D2, D4, D8). The handshake mode is useful in an edge-triggered environment. The DV pin is used to generate an interrupt which forces the system to read information from the data pins. The interrupt (DV), is then cleared by taking CLRDV high momentarily. When there is a need to interface the receivers to a bus, the CS202 and CS203 can be three-state controlled by the EN pin. The EN pin must be held high to take the devices out of the high impedance state and into a data output mode. Conversely, taking EN low will force the devices into high impedance states and prevent bus conflicts.

Table 2 - Digital Encoding of DTMF Signal

Digit	Hexadecimal				Binary 2-of-8			
	D8	D4	D2	D1	D8	D4	D2	D1
1	0	0	0	1	0	0	0	0
2	0	0	1	0	0	0	0	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	0	0
5	0	1	0	1	0	1	0	1
6	0	1	1	0	0	1	1	0
7	0	1	1	1	1	0	0	0
8	1	0	0	0	1	0	0	1
9	1	0	0	1	1	0	1	0
0	1	0	1	0	1	1	0	1
*	1	0	1	1	1	1	0	0
#	1	1	0	0	1	1	1	0
A	1	1	0	1	0	0	1	1
B	1	1	1	0	0	1	1	1
C	1	1	1	1	1	0	1	1
D	0	0	0	0	1	1	1	1

The control interface is represented by the HEX/$\overline{B28}$ pin and the IN1633 pin. Both of these pins control the output data. The HEX/$\overline{B28}$ pin will place the output in a hex format when tied high, and will put it into a binary coded 2-of-8 output format when held low. The IN1633 pin is used to select either the 12 digit or the 16 digit format. When this pin is high, the devices will consider any tone pairs con-taining the 1633Hz signal (digits A, B, C and D) as invalid signals. When this pin is low, all tones are decoded.

Clock Generation

The CS202 and CS203 provide two separate means of clock generation, internal and external. With internal clock generation, a 3.5795 MHz crystal is tied between XIN and XOUT, a 1MΩ resistor is tied in parallel with the crystal to guarantee oscillation, and the XEN signal is tied high enabling the crystal oscillator. In this mode, the ATB pin is a 447.443 kHz clock output which can be used to drive up to 10 other CS202 and CS203 devices that are in the external clock mode.

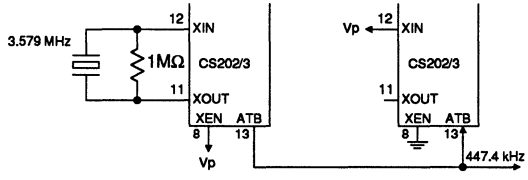
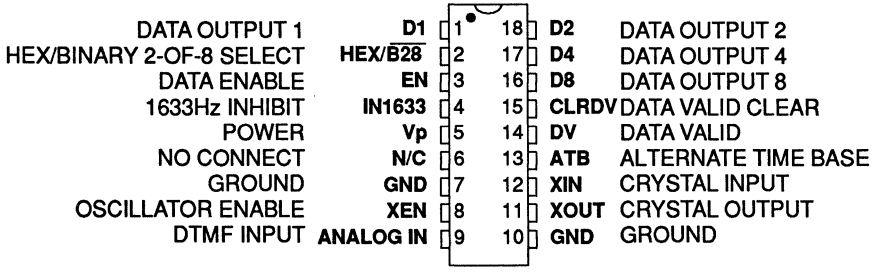


Figure 3 - Clock Options

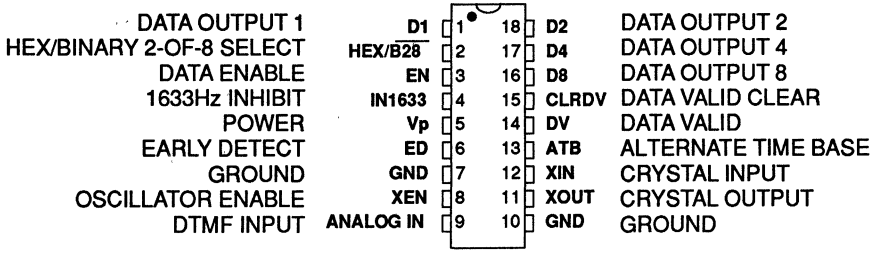
The external clock mode is obtained by tying XIN high and XEN low. In this mode, the internal oscillator output is placed in a high impedance state, and ATB is used to input a 447.443 kHz clock.

Power Supply

The CS202 and CS203 operate on a 5V ± 10% power supply. As with any circuit that combines analog and digital signals, good power supply decoupling is recommended. For best performance, a 0.1µF non-polarized (mylar, ceramic, etc.) capacitor should be tied between Vp and GND. Additional low frequency protection can be achieved with a 10µF electrolytic capacitor connected in parallel with the 0.1µF capacitor. The decoupling capacitors should be situated as close to the device as possible.



CS202



CS203

PIN DESCRIPTIONS

Power Supplies

Vp - Positive Power Supply, PIN 5.
Nominally, +5 volts.

GND - Ground, PINS 7 and 10.
Negative power supply pins. Normally connected to system ground (0 volts). Pin 10 must be connected to ground. Pins 7 and 10 are connected together internally so that an external connection of pin 7 to ground is optional. If pins 7 and 10 are both connected to ground, they should be tied to the same ground trace on the PCB.

Oscillator

XIN - Crystal Input, PIN 12.
Input pin for the crystal oscillator. One lead of the crystal and its bias resistor are tied to this pin.

XOUT - Crystal Output, PIN 11.
Crystal oscillator output pin. One lead of the bias resistor and crystal are tied to this pin.

XEN - Oscillator Enable, PIN 8.
Setting XEN to logic 1 puts the device in the internal clock mode. The on chip oscillator is used as the clock and the ATB pin is configured to output 447.443 kHz ($f_{OSC}/8$). Setting XEN to logic 0 puts the device in the external clock mode. In the external clock mode, a clock signal input to the ATB pin is used to clock the device; the internal oscillator is not used.

ATB - Alternate Time Base, PIN 13.
In the internal clock mode (XEN = 1), ATB will output a 447.443 kHz clock ($f_{OSC}/8$). In the external clock mode (XEN = 0), a 447.443 kHz clock should be input to the ATB pin.

Inputs

ANALOG IN - DTMF Input, PIN 9.
Signal channel input. The DTMF tones to be decoded are input into this pin.

IN1633 - 1633 Hz Inhibit, PIN 4.

Setting IN1633 to logic 1 causes the device to not decode tone pairs which contain 1633 Hz tones. If IN1633 is set to logic 0, the device will decode all 16 DTMF tone pairs.

HEX/$\overline{\text{B28}}$ - Hex/$\overline{\text{B28}}$, Binary 2-of-8 Select, PIN 2.

Setting HEX/$\overline{\text{B28}}$ to logic 1 causes the code corresponding to the decoded DTMF signal to be output in a Hexadecimal format. Data will be output in a Binary 2 of 8 format if HEX/$\overline{\text{B28}}$ is set to logic 0.

EN - Data Enable, PIN 3.

Holding EN at logic 1 enables the data outputs. Setting EN to logic 0 causes the data outputs to go to a high impedance state.

CLRDV - Data Valid Clear, PIN 15.

Setting CLRDV to a logic 1 clears a data valid indication on DV.

Outputs

D1; D2; D4; D8 - Data Outputs, PINS 1; 18; 17; 16.

A code corresponding to a decoded DTMF signal is output on these pins. This output can be in hexadecimal (HEX/$\overline{\text{B28}}$ = 1) or binary 2 of 8 (HEX/$\overline{\text{B28}}$ = 0).

DV - Data Valid, PIN 14.

DV goes to logic 1 when the code corresponding a valid tone pair is present on the data outputs.

ED - Early Detect (CS203 Only), PIN 6.

Indicates data detection prior to processing through the timing circuitry. It is subject to false triggering and drop-outs but can be used to determine if signals are reaching the decoder.

Miscellaneous

N/C - No Connect (CS202 Only), PIN 6.

Not internally bonded.

Semiconductor Corporation

CS204

DTMF Receiver

Features

- Full Receiver Implementation
- Central Office Quality
- Detects All 16 DTMF Tone Pairs
- Uses Inexpensive 3.579 MHz Colorburst Crystal
- Hex Output
- Built-in Filter for Dial Tone Rejection
- 14 Pin Package
- Single 5 Volt ±10% Power Supply
- Low Power CMOS Technology
- Pin Compatible with SSI 204

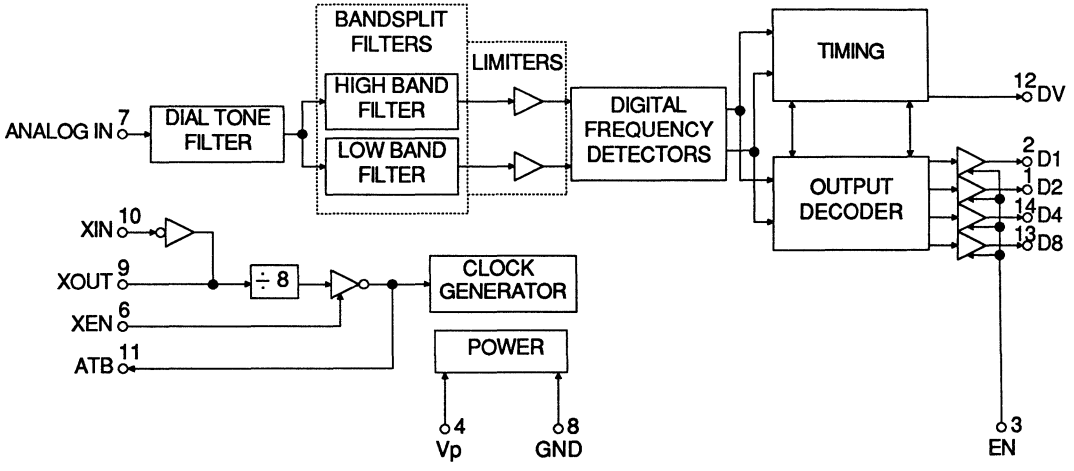
General Description

The CS204 is a fully integrated DTMF (Dual Tone Multifrequency) receiver that decodes the tone pairs used in standard tone dialing schemes. All of the functions needed for decoding the tone pairs are implemented using Crystal's double-poly CMOS process for low power and high performance.

ORDERING INFORMATION
CS204-P 14 Pin Plastic DIP
Standard 300 mil DIPs

4

Block Diagram



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, Texas 78760
(512)445-7222 TWX:910-874-1352

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply	Vp - GND	-	7.0	V
Input Voltage, Any Pin Except Analog in	V_{in}	- 0.5	Vp + 0.5	V
Input Voltage, Analog In	V_{in}	Vp - 10	Vp + 0.5	V
Input Current, Any Pin (Note 1)	I_{in}	-	±10.0	mA
Ambient Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{stg}	- 65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Note: 1. Transient currents of up to 100mA will not cause latch-up.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply	V_p	4.5	5.0	5.5	V
Crystal Frequency	F_C	3.5759	3.5795	3.5831	MHz
Ambient Operating Temperature	T_A	0	25	70	°C

DIGITAL CHARACTERISTICS (T_A = 0°C to 70°C; V_p = 5V ± 10%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	0.7Vp	-	Vp	Volts
Low-Level Input Voltage	V_{IL}	0	-	0.3Vp	Volts
High-Level Output Voltage 200 uA load (Note 2)	V_{OH}	Vp - 0.5	-	Vp	Volts
Low-Level Output Voltage 400 uA load (Note 2)	V_{OL}	0	-	0.5	Volts

Note: 2. Does not include XOUT.

Specifications subject to change without notice.

ANALOG CHARACTERISTICS (T_A = 0°C to 70°C; V_p = 5V ± 10%)

Parameter	Symbol	Min	Typ	Max	Units
Supply Current	I_p	-	6.0	12	mA
Frequency Detect Bandwidth	BW	± (1.5+ 2Hz)	±2.3	±3.5	% of f_b
Detection Amplitude (note 3)	-	- 32	-	- 2	dBm
Twist (note 4)	-	-	±10	-	dB
60 Hz Tolerance	-	-	0.8	-	V_{rms}
Dial Tone Tolerance (note 5, 9)	-	-	22	-	dB
Talk Off (note 6)	-	-	2	-	hits
Power Supply Noise (note 7)	-	-	10	-	mV_{p-p}
Noise Tolerance (note 6, 9)	-	-	- 12	-	dB
Input Impedance at ANALOG IN (note 8)	Z_{in}	100//15	-	-	kohm// pF

Notes: 3. Each tone. dBm = decibels above or below a reference power of 1mW into a 600Ω load.
4. Twist = high tone/low tone.
5. Precise dial tone frequencies of 350Hz ± 2% and 440Hz ± 2%.
6. MITEL tape #CM 7290
7. Bandwidth limited (3kHz) Gaussian noise.
8. V_{in} = (V_p - 10V) to V_p
9. Referenced to lower amplitude tone

4

SWITCHING CHARACTERISTICS (T_A = 0°C to 70°C; V_p = 5V ± 10%)

Parameter	Symbol	Min	Typ	Max	Units
Tone Time:					
for detect	t_{on}	40	-	-	ms
for reject	t_{on}	-	-	20	ms
Pause Time:					
for detect	t_{off}	40	-	-	ms
for reject	t_{off}	-	-	20	ms
Detect Time	t_d	25	-	46	ms
Release Time	t_r	25	-	50	ms
Data Setup Time	t_{su}	7	-	-	us
Data Hold Time	t_h	7	9	10	us
Output Enable Time (note 10) C_L = 50 pF, R_L = 1 kohm	t_{en}	-	200	300	ns
Output Disable Time (note 10) C_L = 35 pF, R_L = 500 Ohms	t_{dis}	-	150	200	ns
Output Rise Time (note 10) C_L = 50 pF	t_{rise}	-	200	300	ns
Output Fall Time (note 10) C_L = 50 pF	t_{fall}	-	160	250	ns

Note: 10. R_L and C_L are parallel impedances.

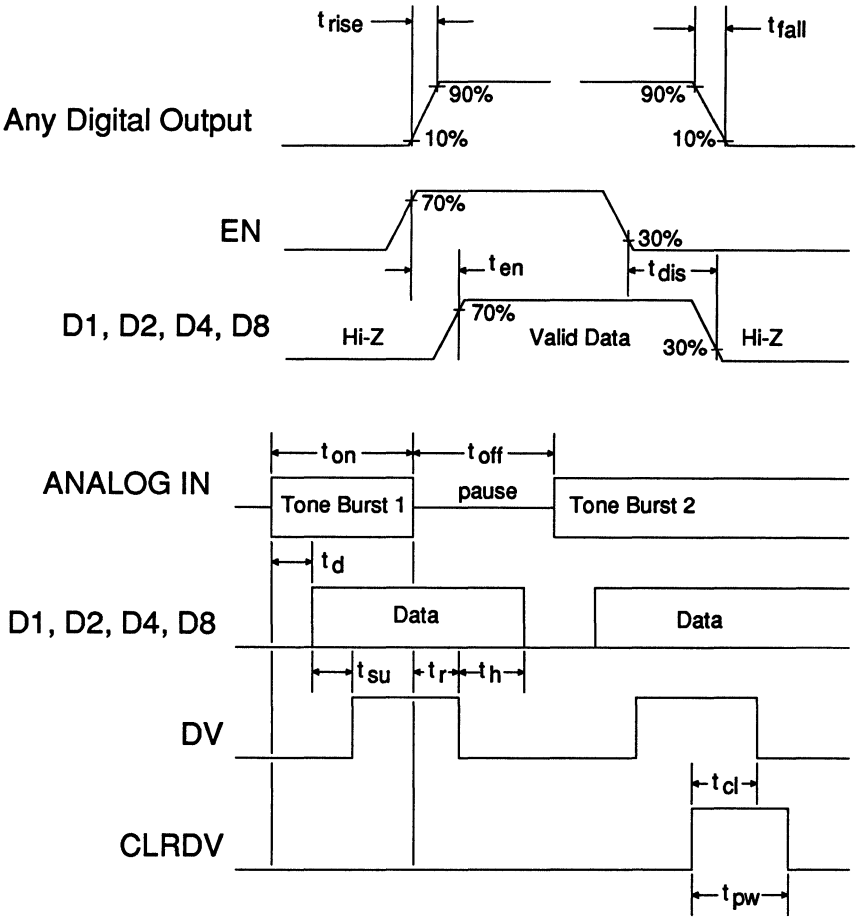


Figure 1 - Timing Diagram

GENERAL DESCRIPTION

The CS204 is a complete Dual Tone Multifrequency (DTMF) Receiver designed to detect 16 digits in a 2-of-8 tone selection scheme. This part provides all of the necessary filtering and requires only an external 3.5795 MHz colorburst crystal and a resistor to provide a reference clock. This device is designed using a high-density, low-power CMOS technology and provides the best performance at the lowest cost.

The CS204 has filtering on board to guarantee the best signal-to-noise performance possible. The DTMF signal is passed through a dial tone reject filter to reduce dial tone interference, and is then separated into low and high groups using two bandsplit filters. The output of each bandsplit filter contains frequency components from only one DTMF tone group.

Table 1 - DTMF Dialing Matrix

Low-Band	High-Band			
	Column 1 1209 Hz	Column 2 1336 Hz	Column 3 1477 Hz	Column 4 1633 Hz
Row 1 697 Hz	1	2	3	A
Row 2 770 Hz	4	5	6	B
Row 3 852 Hz	7	8	9	C
Row 4 941 Hz	*	0	#	D

For a valid DTMF signal to be detected, each group must simultaneously contain only one valid DTMF tone. Detection of the two tones is accomplished with a digital algorithm. The sinusoidal filter output waveforms pass through a pair of hard limiters. The decoder takes the resultant square waves and measures the period. This period measurement varies with jitter created by any extraneous signals within the signal passed to the limiter. The period measurement is averaged over a number of cycles and compared to a range of period measurements representing the four expected tones. After two valid tones have been recognized by the decoder, the tones are subjected to a detect timing cycle. The two tones must remain valid for 20 to 40 ms for DV to go high, indicating that a valid digit has been decoded. This prevents voices or other in-band noise from creating a false trigger.

After a valid digit is indicated, the timing circuit will then enable a timing chain that detects drop-outs. If a signal drop of less than 20 ms occurs, it will be ignored. This timing prevents false triggering due to key bounce or other signal interruptions. Any drop-out in excess of 40 ms is considered a valid release; the receiver is reset (DV goes low), and all decoded outputs are cleared for the next decode.

Interfacing to the CS204

The CS204 has analog and data interfaces. The analog interface determines how an analog voice channel is connected. The data interface is used to extract information from the receiver.

The analog interface consists of only one signal: ANALOG IN. The ANALOG IN signal can be either DC-coupled or AC coupled using a 0.01µF capacitor. Care must be taken to not exceed the voltage requirements of the pin. On-chip capacitor coupling guarantees that the signal is properly referenced internally. It is also desirable to add a simple RC lowpass filter to bandlimit the input to the voice band (100 Hz to 3.4 kHz) so that high frequency noise near the 55.9 kHz internal sampling frequency is not aliased into the voice band by the internal switched-capacitor filters.

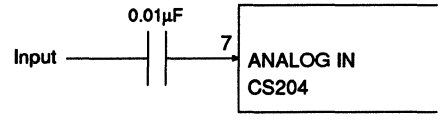


Figure 2 - AC-Coupled Input

The data interface is structured as a synchronous output. Data is extracted from the receiver by using the DV pin as either an output strobe or by scanning and externally detecting the positive-going edge of DV. Data is considered valid only when DV is high.

Clock Generation

The CS204 provides two separate means of clock generation, internal and external. With internal clock generation, a 3.5795 MHz crystal is tied between XIN and XOUT, a 1MΩ resistor is tied in parallel with the crystal to guarantee oscillation, and the XEN signal is tied high enabling the crystal oscillator. In this mode, the ATB pin is a 447.443 kHz clock output which can be used to drive up to 10 other CS202, CS203 or CS204 devices that are in the external clock mode. The external clock mode is obtained by tying XIN high and XEN low. In this mode, the internal oscillator output is placed in a high impedance state, and ATB is used to input a 447.443 kHz clock.

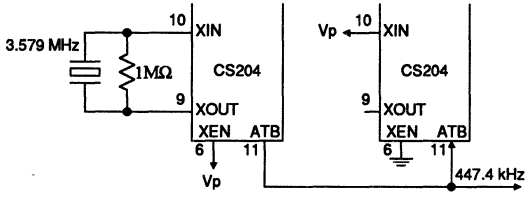


Figure 3 - Clock Options

Power Supply

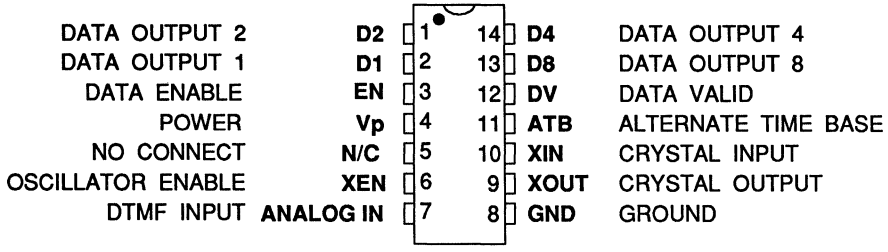
The CS204 operates from a 5 volts ± 10% power supply. As with any circuit that combines analog and digital signals, good power supply decoupling is recommended. For best performance, a 0.1µF non-polarized (mylar, ceramic, etc.) capacitor should be tied between Vp and GND. Additional low frequency protection can be achieved with a 10µF electrolytic capacitor connected in parallel with the 0.1µF capacitor.

Table 2 - Output Codes

Digit	Hexadecimal			
	D4	D3	D2	D1
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	1	0	1	0
*	1	0	1	1
#	1	1	0	0
A	1	1	0	1
B	1	1	1	0
C	1	1	1	1

4

PIN DESCRIPTIONS



Power Supplies

Vp - Positive Power Supply, PIN 4.
Nominally +5 volts.

GND - Ground, PIN 8.
Most negative power supply pin. Normally connected to system ground (0 volts).

Oscillator

XIN - Crystal Input, PIN 10.
Input pin for the crystal oscillator. One lead of the crystal and its bias resistor are tied to this pin.

XOUT - Crystal Output, PIN 9.
Crystal oscillator output pin. One lead of the bias resistor and crystal are tied to this pin.

XEN - Oscillator Enable, PIN 6.
Setting XEN to logic 1 puts the device in the internal clock mode. The on chip oscillator is used as the clock and the ATB pin is configured to output 447.443 kHz ($f_{OSC}/8$). Setting XEN to logic 0 puts the device in the external clock mode. In the external clock mode, a signal input to the ATB pin is used to clock the device; the internal oscillator is not used.

ATB - Alternate Time Base, PIN 11.
In the internal clock mode (XEN=1), ATB will output a 447.443 kHz clock ($f_{OSC}/8$). In the external clock mode (XEN=0), a 447.433 kHz clock should be input to the ATB pin.

Inputs

ANALOG IN - DTMF Input, PIN 7.
Signal channel input. The DTMF tones to be decoded are input into this pin.

EN - Data Enable, PIN 3.

Holding EN at logic 1 enables the data outputs. Setting EN to logic 0 causes the data outputs to go to a high impedance state.

Outputs

D1; D2; D4; D8 - Data Outputs, PINS 2; 1; 14; 13.

A code corresponding to a decoded DTMF signal is output on these pins in a hexadecimal format.

DV - Data Valid, PIN 12.

DV goes to logic 1 when the code corresponding to a valid tone pair is present on the data outputs.

Miscellaneous

N/C - No Connect, PIN 5.

Not internally bonded.

• Notes •

Semiconductor Corporation

CS8870

DTMF Receiver

Features

- Full Receiver Implementation
- Central Office Quality
- Adjustable Receive Sensitivity
- Adjustable Detection and Release Time
- Single Supply Operation
- Low Power Consumption
- 18 Pin Package
- Pin Compatible with MT8870

General Description

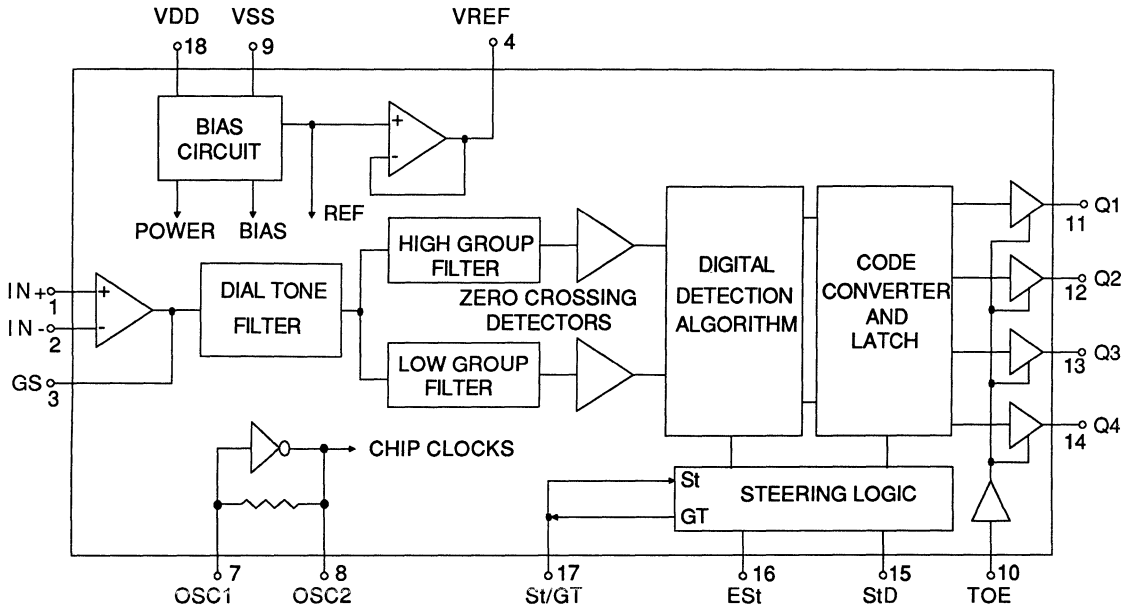
The CS8870 is a fully integrated Dual Tone Multi-frequency (DTMF) receiver for decoding tone pairs generated by a tone dialing telephone. The decoded signal is output as a four bit binary code. All of the functions needed to decode the 16 DTMF tone pairs are integrated in the CS8870 using CRYSTAL'S CMOS double-poly process, taking advantage of the low power and high performance offered by this technology.

ORDERING INFORMATION

CS8870-IP 18 Pin Plastic DIP

4

Block Diagram



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, Texas 78760
(512)445-7222 TWX:910-874-1352

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply	V_{DD}-V_{SS}	-	6.0	Volts
Input Voltage	V_{in}	V_{SS}-0.3	V_{DD}+0.3	Volts
Input Current, Any Pin *	I_{in}	-	10	mA
Power Dissipation **	P_D	-	1000	mW
Ambient Operating Temperature	T_A	-40	85	°C
Storage Temperature	T_{stg}	-65	150	°C

*Transient currents of up to 100mA will not cause latch-up.
**Derate above 75°C at 16 mW/°C; all leads soldered to board.

WARNING: Operating this device at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply	V_{DD} -V_{SS}	4.75	5.0	5.25	Volts
Ambient Operating Temperature	T_A	0	25	70	°C
Crystal Frequency	f_C	3.5759	3.5795	3.5831	MHz

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (T_A = 25°C; V_{DD} = 5V; V_{SS} = 0V; f_C = 3.579545MHz)

Parameter	Symbol	Min	Typ *	Max	Units
Supply Current	I_{DD}	-	6.0	10.0	mA
Power Consumption		-	30	45	mW
Input Impedance, pins 1 & 2 (note 12)	R_{IN}	-	10	-	Mohms
Steering Threshold Voltage	V_{TSt}	2.2	-	2.5	V
Signal Levels for Valid Input (each tone of composite signal) (notes 1, 2, 3, 5, 6, 9)		- 29 27.5	- -	+1 883	dBm mVrms
Twist (notes 2,3,6,9,13)		-	±10	-	dB
Frequency Detect Bandwidth (notes 2,3,5,9)		±1.5% ±2Hz	-	±3.5%	
Third Tone Tolerance (notes 2,3,4,5,9,10)		-	- 16	-	dB
Noise Tolerance (notes 2,3,4,5,7,9,10)		-	- 12	-	dB
Dial Tone Tolerance (notes 2,3,4,5,8,9,10)		-	+ 22	-	dB
Clock Output (OSC 2, pin 8) Capacitive Load		-	-	30	pF
V_{REF} Output Voltage No Load	V_{REF}	2.4	-	2.8	V
V_{REF} Output Resistance	R_{OR}	-	10	-	kohms

Parameters measured using test circuit shown in Figure 4.
*Typical figures for design only; not guaranteed and not subject to production testing.

Notes:
1. dBm referenced to power of 1mW into 600Ω load.
2. Digit sequence consists of all 16 DTMF tones.
3. Tone duration of 40ms, tone pause of 40ms.
4. Nominal DTMF frequencies are used.
5. Both tones of the composite signal have equal amplitudes.
6. Tone pair is deviated by ± 1.5% ± 2Hz
7. Bandwidth limited to 3kHz Gaussian noise.
8. Precise dial tone frequencies of 350Hz ± 2% and 440Hz ± 2%.
9. For error rate of better than 1 in 10,000.
10. Referenced to lowest frequency component of DTMF signal.
11. Referenced to minimum valid accept level.
12. Input frequency of 1kHz.
13. Twist = high tone/low tone.

4

ANALOG CHARACTERISTICS Gain Setting Amplifier

(T_A = 25°C; V_{DD} = 5V; V_{SS} = 0V; voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ*	Max	Units
Input Leakage Current (note 14)	I_{IN}	-	100	-	nA
Input Resistance	R_{IN}	-	10	-	Mohms
Input Offset Voltage	V_{OS}	-	25	-	mV
Common Mode Rejection (note 15)	CMRR	-	60	-	dB
Power Supply Rejection (note 16)	PSRR	-	60	-	dB
DC Open Loop Voltage Gain	A_{VOL}	-	65	-	dB
Open Loop Unity Gain Bandwidth	f_C	-	1.5	-	MHz
Output Voltage Swing (note 17)	V_O	-	4.5	-	Vp-p
Tolerable Capacitive Load, GS pin	C_L	-	100	-	pF
Tolerable Resistive Load, GS pin	R_L	-	50	-	kohms
Common Mode Range (note 18)	V_{CM}	-	3.0	-	Vp-p

*Typical figures for design only; not guaranteed and not subject to production testing.

Notes: 14. $V_{SS} \le V_{IN} \le V_{DD}$
15. $-3.0V \le V_{IN} \le +3.0V$
16. At 1kHz
17. $R_L \ge 100k\Omega$ to V_{SS}
18. Unloaded

SWITCHING CHARACTERISTICS (T_A = 25°C; V_{DD} = 5V; V_{SS} = 0V; f_C = 3.579545MHz)

Parameter	Symbol	Min	Typ*	Max	Units
Tone Present Detection Time	t_{DP}	5	11	14	ms
Tone Absent Detection Time	t_{DA}	0.5	4	8.5	ms
Tone Duration Accept+	t_{REC}	-	-	40	ms
Tone Duration Reject+	$\overline{t_{REC}}$	20	-	-	ms
Interdigit Pause Accept+	t_{ID}	-	-	40	ms
Interdigit Pause Reject+	t_{DO}	20	-	-	ms
Propagation Delay (St to Q) (note 19)	t_{PQ}	-	8	11	us
Propagation Delay (St to StD) (note 19)	t_{PStD}	-	12	-	us
Output Data Set Up (Q to StD) (note 19)	t_{QStD}	-	3.4	-	us
Propagation Delay (TOE to Q) (note 20) ENABLE	t_{PTE}	-	50	-	ns
DISABLE	t_{PTD}	-	300	-	ns
Clock Input Rise Time	t_{LHCL}	-	-	110	ns
Clock Input Fall Time	t_{HLCL}	-	-	110	ns
Clock Input Duty Cycle	DC_{CL}	40	50	60	%

Parameters measured using test curcuit shown in Figure 4.
*Typical figures for design only; not guaranteed and not subject to production testing.
+User adjustable; see *General Description* on page 30.

Notes: 19. TOE = V_{DD}
20. R_L = 10kΩ, C_L = 50pF

4

DIGITAL CHARACTERISTICS (T_A = 25°C; V_{DD} = 5V; V_{SS} = 0V; voltages referenced to V_{SS})

Parameter		Symbol	Min	Typ*	Max	Units
Digital Inputs	"0" level	V_{IL}	-	-	1.5	V
	"1" level	V_{IH}	3.5	-	-	
Digital Outputs (note 21)	"0" level	V_{OL}	-	-	0.03	V
	"1" level	V_{OH}	4.97	-	-	
Output Low (Sink) Current (note 22)		I_{OL}	1	2.5	-	mA
Output High (Source) Current (note 23)		I_{OH}	0.4	0.8	-	mA
Input Leakage Current (note 24)		I_{IH}, I_{IL}	-	0.1	-	uA
Pull Up Source Current (note 25)		I_{SO}	-	7.5	15	uA

*Typical figures for design only; not guaranteed and not subject to production testing.

Notes: 21. No Load
22. V_{OUT} = 0.4V
23. V_{OUT} = 4.6V
24. V_{IN} = V_{SS} or V_{DD}
25. TOE(pin 10) = 0V

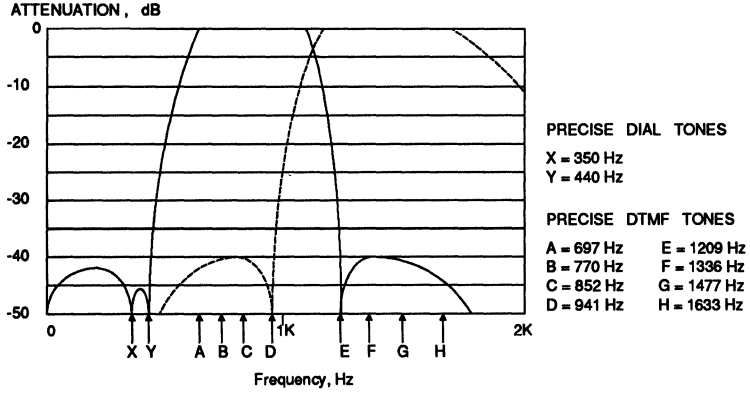
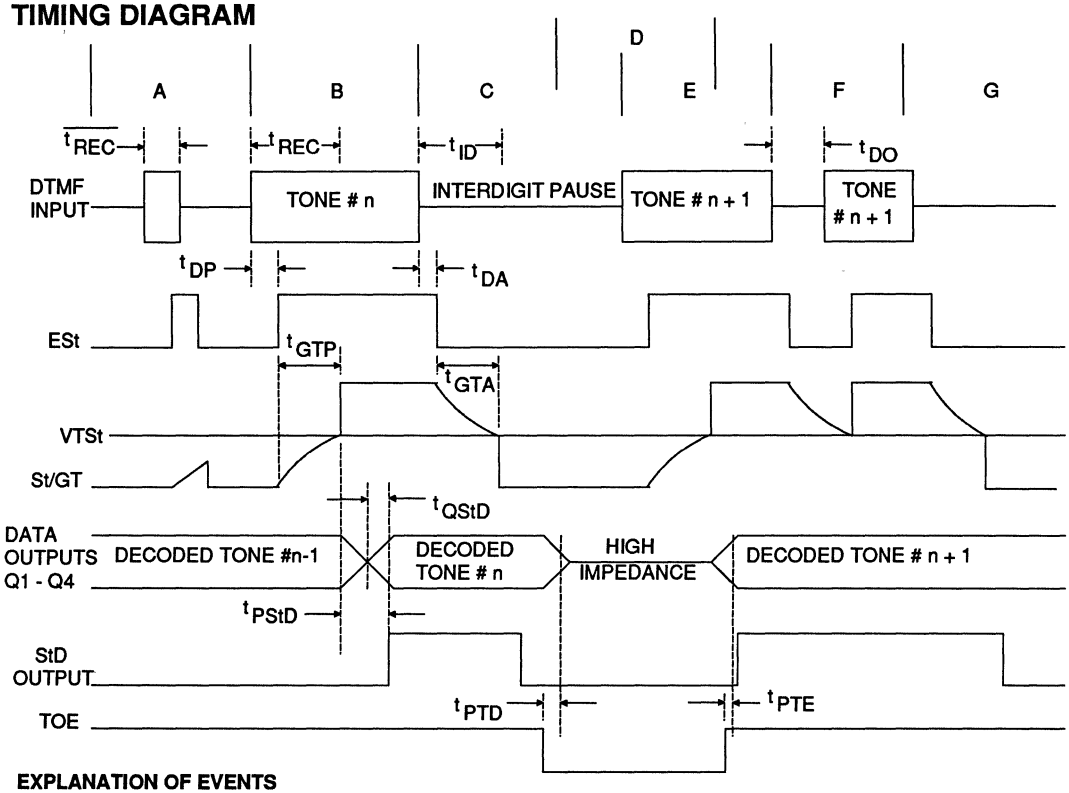


Figure 1 - Filter Characteristics

TIMING DIAGRAM



EXPLANATION OF EVENTS

A. Short tone burst is detected, but duration is invalid.
B. Tone # n is detected, and duration is valid. Decoded to outputs.
C. End of tone # n detected and duration is valid. Outputs remain latched until next valid tone.
D. Three state outputs are disabled (high impedance).
E. Tone # n + 1 is detected and validated. Decoded to outputs.
F. Three state outputs are enabled. Momentary dropout of tone # n + 1 does not register at outputs.
G. End of tone # n + 1 detected and validated. Outputs remain latched until next valid tone.

DEFINITION OF SYMBOLS

ESt - EARLY STEERING OUTPUT - Indicates detection of valid DTMF signal.
St/GT - STEERING INPUT/GUARD TIME OUTPUT - Drives external timing circuit.
Q1-Q4 - DATA OUTPUTS - Gives code corresponding to decoded tone pair.
StD - DELAYED STEERING OUTPUT - Indicates that valid signals have been present (or absent) for the required time.
TOE - TONE OUTPUT ENABLE (Input) - Holding TOE low causes Q1-Q4 to go to high impedance state.

$t_{\overline{REC}}$ - DTMF signal duration too short to be detected as valid.
t_{REC} - Minimium signal duration required for valid recognition.
t_{ID} - Minimum acceptable time between valid signals.
t_{DO} - Maximum allowable dropout of DTMF signal.
t_{PTD} - Propagation Delay, Disable
t_{PTE} - Propagation Delay, Enable
t_{DP} - Time to detect presence of valid signal.
t_{DA} - Time to detect absence of valid signal.
t_{GTP} - Tone Present Guard Time
t_{GTA} - Tone Absent Guard Time.
t_{QStD} - Output Data Setup (Q to StD)
t_{PStD} - Propagation Delay (St to StD)

GENERAL DESCRIPTION

The CS8870 is a complete Dual Tone Multifrequency (DTMF) receiver designed to detect all 16 tone pairs and output a corresponding four bit binary code. This device provides all necessary filtering and requires a minimum of external components. Low power CMOS technology provides the highest performance for the lowest cost.

Filter Section

The CS8870's on chip filtering provides excellent signal-to-noise performance. The DTMF signal is separated into high and low groups using two six pole, bandpass switched capacitor filters. The bandpass filters are elliptical designs with notches placed at 350 Hz and 440 Hz for exceptional dial tone rejection. The output of each bandpass filter contains frequency components from only one DTMF tone group. The filter outputs are smoothed and then limited by high gain comparators, which have hysteresis to reduce sensitivity to unwanted low level signals, jitter, and noise. The comparators' outputs swing from rail to rail at the frequencies of the incoming tones.

Decoder Section

The decoder uses a digital detection algorithm to determine the frequencies of the two tones. The decoder measures the period of the square wave output of the comparators. The period measurement is averaged over a number of cycles and compared to a range of period measurements representing the four possible tones in either band. This averaging prevents DTMF simulation by extraneous signals such as voice, while allowing small frequency deviations in the signal. The averaging algorithm has been optimized to provide excellent immunity to "talk-off" and tolerance to the presence of interfering frequencies (third tones) and noise. When both bands simultaneously decode a valid tone, the Early Steering (ESt) output goes high. Should the DTMF signal be lost, the ESt pin will go low.

Steering Circuit

The receiver verifies that the duration of a valid signal is sufficient before registering a decoded tone pair. Tone detection timing is controlled by an external resistor and capacitor (see Figure 2). After a valid tone is present for t_{DP} (Tone Present Detection Time), ESt goes high, and the capacitor discharges through resistor R. The voltage on the St/GT pin changes as a function of the RC time constant, providing the DTMF signal remains valid. When the capacitor voltage (and the voltage on St/GT) reaches the Steering Threshold Voltage, V_{TSt}, the GT output drives the capacitor voltage to VDD. At this point, the four bit code corresponding to the DTMF signal is latched to the outputs. GT remains high as long as ESt remains high. After the output latches settle, the Delayed Steering Output, StD, goes high, indicating that a valid tone pair has been registered. The code is made available at outputs Q1 - Q4 by pulling the three state control input, TOE, to a logic high.

The steering circuit works in reverse to sense the interdigit pause between signals. When the DTMF signal is removed, the capacitor charges. When the Steering Threshold Voltage is reached, GT is pulled to V_{SS}. This circuit also

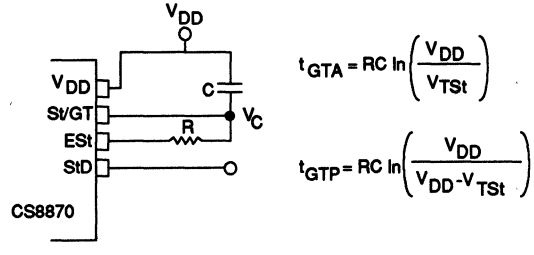


Figure 2 - Basic Steering Circuit

enables the receiver to tolerate signal dropouts too short to be considered a valid pause.

Guard Time Adjustment

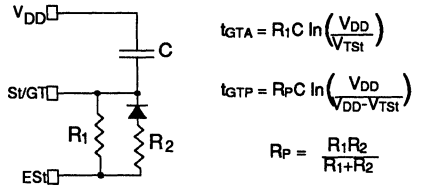
The external timing circuitry shown in Figures 2 and 3, enables the user to adjust the timing to meet specific needs. The following formulas, along with the formulas given in Figure 2, are used to determine the resistor and capacitor values.

$$t_{REC} = t_{DP} + t_{GTP}$$
$$t_{ID} = t_{DA} + t_{GTA}$$

t_{REC} is the minimum signal duration accepted by the receiver. t_{DP} is the Tone Present Detection Time (the time a valid tone must be present before ESt goes high). t_{ID} is the Interdigit Pause Time. t_{DA} is the Tone Absent Detection Time. Values for t_{DP} and t_{DA} are given in the Switching Characteristics Table. Using the configuration shown in Figure 2, and the recommended capacitor value of 0.1µF, a t_{REC} of 40ms is achieved by using a 300kΩ resistor.

Different circuit configurations may be used to independently select Tone Present Guard Time, t_{GTP}, and Tone Absent Guard Time, t_{GTA}, durations. Using the equations and circuits shown in Figure 3, the designer can meet system specifications which place limits on accept and reject times for tone and pause durations, and tailor system parameters such as "talk-off" and noise immunity. For example, increasing recognition time improves talk-off performance (speech immunity) since it reduces the probability that tones simulated by speech remain valid long enough to register.

a) Decreasing Tone Present Guard Time, t_{GTP} ($t_{GTP} < t_{GTA}$)



b) Decreasing Tone Absent Guard Time, t_{GTA} ($t_{GTP} > t_{GTA}$)

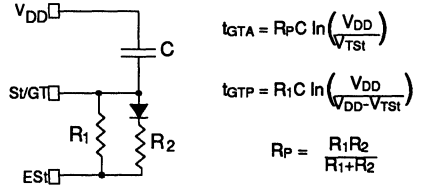


Figure 3 - Steering Circuits for Guard Time Adjustment

Input Configuration

Input signals to the CS8870 pass through an on-chip operational amplifier. A voltage reference, VREF, is provided to bias the input near mid-supply. Figure 4 shows a single ended input configuration with the inputs biased at VREF, and for unity gain. A differential input configuration is shown in Figure 5. The feedback resistor, R5, connected to the op-amp output, GS, can be used to control the gain.

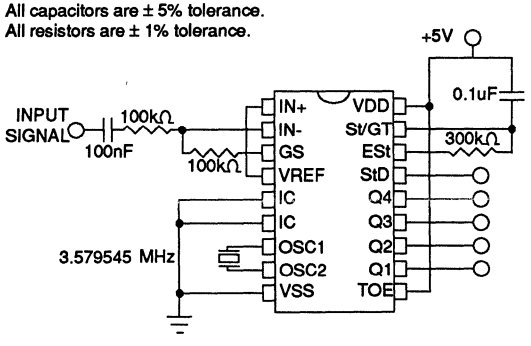
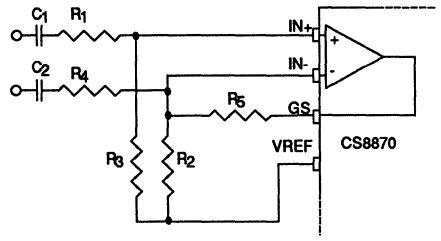


Figure 4 - Single Ended Input Configuration



$C_1 = C_2 = 0.01\mu F$
$R_1 = R_4 = R_5 = 100k\Omega$
$R_2 = 60k\Omega$
$R_3 = 37.5k\Omega$

$$R_3 = \frac{R_2 R_5}{R_2 + R_5}$$

$$\text{Voltage Gain (Av diff)} = \frac{R_5}{R_1}$$

$$\text{Input Impedance } (Z_{IN} \text{ diff}) = 2\sqrt{R_1 + \left(\frac{1}{\omega C}\right)^2}$$

Figure 5 - Differential Input Configuration

F_{LOW}	F_{HIGH}	KEY	TOE	Q4	Q3	Q2	Q1
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	0	1	1	1
852	1336	8	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1336	0	H	1	0	1	0
941	1209	*	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	0	1
770	1633	B	H	1	1	1	0
852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
-	-	ANY	L	Z	Z	Z	Z

L - LOGIC LOW H - LOGIC HIGH
Z - HIGH IMPEDANCE

Table 1 - Functional Decoding

Crystal Oscillator

An external 3.579545 MHz (TV colorburst) crystal must be connected across pins OSC1 and OSC2 to complete the internal clock circuit. Up to ten CS8870s may be driven by one crystal by connecting the oscillator output, OSC2, with the oscillator input, OSC1, of another device through a 30pf capacitor. Refer to Figure 6.

Logic high on TOE enables the data output pins to output code for the last valid DTMF signal received. Q1 is the LSB. These outputs go to a high impedance state when TOE is low. See the Functional Decode table, Table 1.

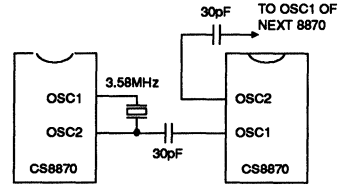


Figure 6 - Oscillator Interconnection

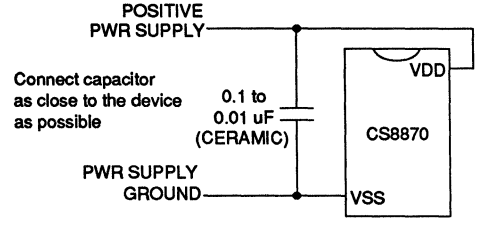
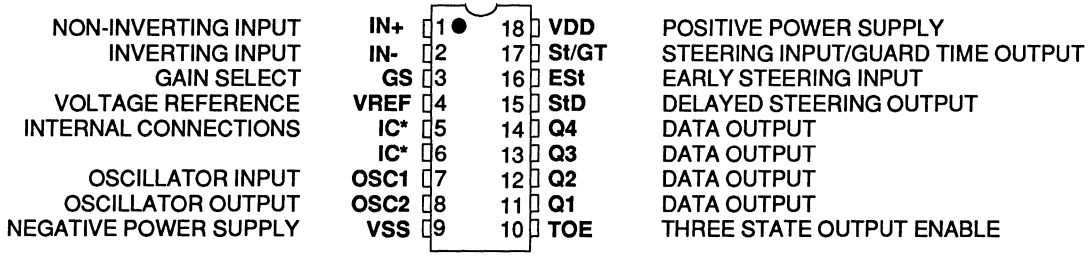


Figure 7. Power Supply Decoupling

PIN DESCRIPTIONS



*Connect to V_{SS}

Power Supplies

VDD - Positive Power Supply Input, PIN 18.
Normally connected to +5 volts. A 0.01µF to 0.1µF ceramic capacitor should be connected as close to the device as possible across V_{DD} and V_{SS}. (See Figure 7).

VSS - Negative Power Supply Input, PIN 9.
Normally connected to 0 volts.

Oscillator

OSC1; OSC2 - Oscillator Input, PIN 7; Oscillator Output, PIN 8.
A 3.579545 MHz crystal connected across these pins completes the internal clock circuit.

Inputs

St/GT - Steering Input/Guard Time Output, PIN 17.
When the voltage on this pin rises past the Steering Threshold Voltage, V_{TSt}, the device registers the detected tone pair, updates the output latch, and drives this pin to a logic high. When the voltage on this pin falls below V_{TSt}, this pin goes to a logic low, freeing the device to accept a new tone pair. The Guard Time Output's function is to reset the external steering time constant. The state of GT is a function of ESt and St.

IN+ - Non-Inverting Input, PIN 1.
Non-inverting input to the front end operational amplifier.

IN- - Inverting Input, PIN 2.
Inverting input to the front end operational amplifier.

TOE - Three State Output Enable, PIN 10.

Logic high on this pin enables outputs Q1 - Q4. Internal pull up.

Outputs

GS - Gain Select, PIN 3.

Connected to the output of the front end operational amplifier. Gain applied to the input can be controlled by a feedback resistor at this pin.

VREF - Voltage Reference, PIN 4.

Voltage on this pin is nominally 2.5 VDC independent of power supply, and may be used to bias inputs at mid supply.

Q1, Q2, Q3, Q4 - Data Outputs, PINS 11, 12, 13, 14.

Logic high on TOE enables pins to output code for last valid DTMF signal received. Q1 is the LSB. These outputs go to a high impedance state when TOE is low. See Functional Decode Table.

StD - Delayed Steering Output, PIN 15.

Outputs a logic high when voltage on St/GT exceeds V_{TSt} and the output latch has been updated with code from the received tone pair. StD goes to a logic low when voltage on St/GT falls below V_{TSt}.

ESt - Early Steering Output, PIN 16.

Goes to a logic high whenever the detection algorithm detects a valid tone pair. Any loss of a valid DTMF signal causes the output to go to a logic low

IC, IC - Internal Connection, PINS 5, 6.

Both pins must be tied to V_{SS}.

INTRODUCTION

Crystal's optical interface devices dramatically cut the cost of implementing low-to-meduim speed optical links. The CS8123/4 Optimodems use just one optical cable to implement full duplex host-to-terminal, ISDN and TEMPEST links, slashing the cost of optical components in half. The CS8125/6 support T1 links at a fraction of the cost of optical hybrids. All of Crystal's optical interface devices include clock recovery, line code encoder/decoders, diagnostic fetaures and adjustable transmit power levels.

USER'S GUIDE

Device:	CS8123 Optimodem	CS8124 Optimodem	CS8125 T1 Transmitter	CS8126 T1 Receiver
Maximum Data Rate				
Synchronous	-	256 kbps	1.544 MHz	1.544 MHz
Asynchronous	38.4 kHz	38.4 kHz	-	-
Maximum Range	2 km	2 km	7 km	7 km
Number of Cables for Full Duplex Link	1	1	2	2
Package	16 pin DIP	24 pin 0.3" DIP	16 pin DIP	16 pin DIP

CONTENTS

Semiconductor Corporation

CS8123/4

OPTIMODEM™

Features

- Time Compression Multiplexing for full-duplex communication over a single optical fiber.
- Synchronous operation from 2.4 kbps to 256 kbps.
- Asynchronous operation from DC to 38.4 kbps.
- 10^{-9} BER up to 2 km.
- System diagnostic capabilities.
- Four optional secondary control channels provide independent end-to-end transmission links.
- Independent transmit and receive clocks.
- Self-calibrating noise-bandwidth limiting.

General Description

The CS8123 and CS8124 from Crystal Semiconductor Corporation are SMART Analog™ full-duplex modem devices that receive and transmit serial binary data over a single fiber-optic cable. Both devices provide the filtering, encoding, decoding and data buffering to implement a "ping-pong" communication channel.

The 16-pin CS8123 device supports asynchronous communication control lines $\overline{RTS}$ & $\overline{CTS}$. The 24-pin CS8124 device supports asynchronous and synchronous communications with control lines $\overline{CTS}$, $\overline{RTS}$, $\overline{DTR}$ & $\overline{DSR}$. These lines can be used for RS-232C compatible modem control, or end-to-end transmission channels.

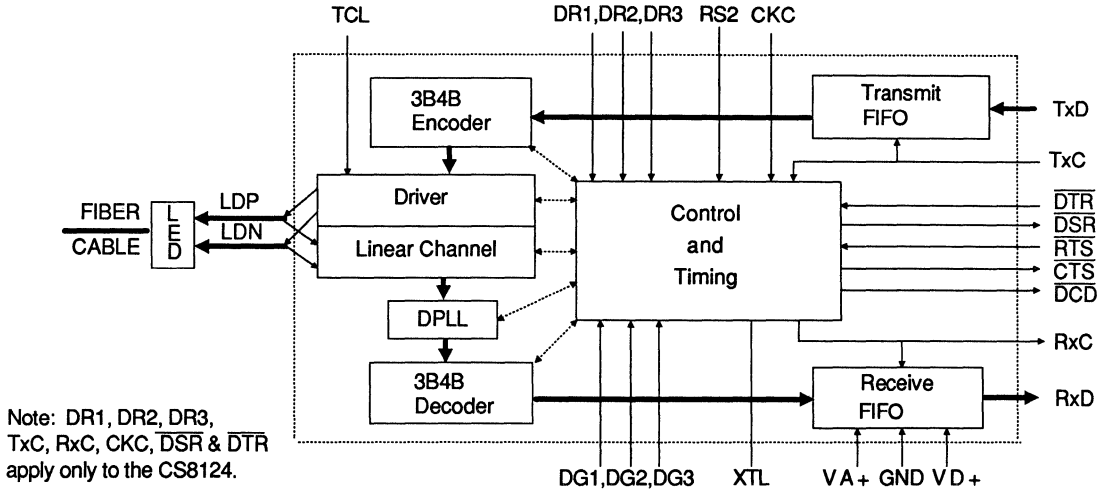
SMART Analog and OPTIMODEM are trademarks of Crystal Semiconductor Corporation.

ORDERING INFORMATION

CS8123-IP - 16 Pin Plastic DIP
CS8124-IP - 24 Pin Plastic DIP (Skinny 0.3" wide)

5

Block Diagram



Note: DR1, DR2, DR3, TxC, RxC, CKC, $\overline{DSR}$ & $\overline{DTR}$ apply only to the CS8124.

Preliminary Product Information | *This document contains data for a new product. Crystal Semiconductor reserves the right to modify this product without notice.*

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply	V+ - GND	- 0.3	6.0	V
Input Voltage	V_{in}	GND - 0.3	V+ + 0.3	V
Input Current (Note 1) (Any pin except LDP, LDN, VA+, VD+ & GND)	I_{in}	-	10	mA
Ambient Operating Temperature	T_A	- 40	85	°C
Storage Temperature	T_{stg}	- 65	150	°C
Power Dissipation	P_D	-	500	mW

WARNING: Operating this device at or beyond these limits may result in permanent damage to the device. Normal operation of the part is not guaranteed at or beyond these extremes.

Note: 1. Transient currents of up to 100 mA will not cause SCR latch-up.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply	V+	4.75	5.0	5.25	V
Ambient Operating Temperature	T_A	-40	25	85	°C
LED Drive Current (Note 2)	I_{LDC}	8.5	100	115	mA

Note: 2. LED drive current can be reduced by connecting an external resistor to the Transmit Current Level, TCL, pin. Minimum drive current is achieved by grounding TCL pin.

DIGITAL CHARACTERISTICS (T_A = -40 °C to 85 °C; V+ = 5V ± 5%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (Note 3)	V_{IH}	2.0	-	-	V
Low-Level Input Voltage Pins (Note 3)	V_{IL}	-	-	0.8	V
High-Level Output Voltage I_{OUT} = -40 uA (Notes 4,5)	V_{OH}	2.4	-	-	V
Low-Level Output Voltage I_{OUT} = 1.6 mA (Notes 4,5)	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	± 10.0	-	uA
Three-State Leakage Currents	I_{oz}	-	-	± 10	uA

Notes: 3. Input pins are: DR 1/2/3, DG 1/2/3, RS2, CKC, $\overline{DTR}$, $\overline{RTS}$, TxD, TxC.
4. Output pins are: $\overline{DSR}$, $\overline{CTS}$, $\overline{DCD}$, RxD, RxC, TxC.
5. Output drivers will output CMOS logic levels into a CMOS load.

OPERATING CHARACTERISTICS (T_A = -40 °C to 85 °C; V+ = 5V ± 5%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
Power Dissipation, normal operation (Note 6)	P_{DNO}	100	250	300	mW
Power Dissipation, continuous transmission (Note 6)	P_{DCT}	150	375	450	mW
Power Dissipation, continuous reception (Note 6)	P_{DCR}	100	125	150	mW
Power Dissipation, IC only, normal operation	P_D	100	200	250	mW

Note: 6. Total power dissipated by IC and LED, LED as specified in Table A2.

SWITCHING CHARACTERISTICS (T_A = -40 °C to 85 °C; V+ = 5V ± 5%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
Crystal Frequency	f_C	-	9.216	12.4	MHz
TxC & RxC Frequency: Synchronous Transmit or Receive Only	f_{ckc} f_{ckc}	2.4 -	- $f_C/8$	256 -	kHz kHz
RxD & TxD Data Rate: Synchronous Asynchronous		2.4 dc	- -	256 38.4	kHz kHz
RxC & TxC Duty Cycle (Note 7, 8)		-	50	-	%
Rise Time, All Digital Outputs (Note 9)	t_r	-	-	100	ns
Fall Time, All Digital Outputs (Note 9)	t_f	-	-	100	ns
TxD to TxC Rising Setup Time (Note 8)	t_{su}	25	-	-	ns
TxC Falling to TxD Hold Time (Note 8)	t_h	25	-	-	ns
RxD to RxC Rising Setup Time (Note 8)	t_{su}	-	$\frac{1}{2 f_{ckc}}$-100	-	ns
RxC Rising to RxD Hold Time (Note 8)	t_h	-	$\frac{1}{2 f_{ckc}}$-100	-	ns
Frequency Deviation at TxC Input from Selected Rate (Note 8, 10)		-	-	500	ppm

Notes: 7. Duty cycle is ($t_{pwh}/(t_{pwh} + t_{pwl})$) * 100%.
8. CS8124 in synchronous operation (not all DR1/2/3 low).
9. At maximum load of 1.6 mA and 50 pF.
10. In Synchronous mode, data rate selected by DR1/2/3.
In Transmit only mode, selected rate is $f_C/8$.
Crystal frequency must be within ± 50 ppm of specified frequency.

5

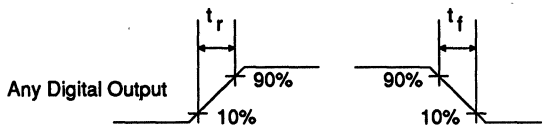


Figure 1 - Digital Output Rise and Fall Characteristics

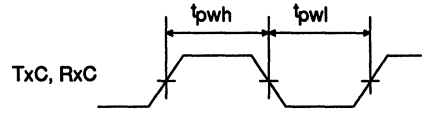


Figure 2 - Clock Signal Timing

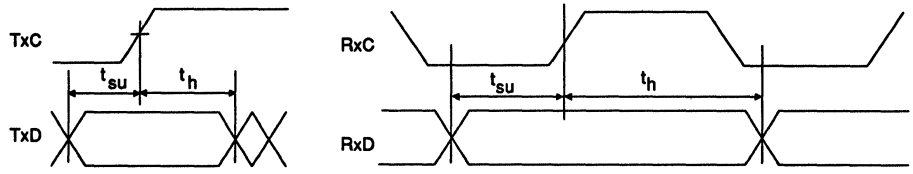


Figure 3 - Switching Characteristics

CIRCUIT DESCRIPTION

The CS8123/4 OPTIMODEMs receive and transmit serial binary data over a single fiber-optic cable. The modems provide the filtering, encoding, decoding and data buffering to implement a Time Compression Multiplexed "ping-pong" channel. Both modems support full-duplex asynchronous operation up to 38.4 kbps. The CS8124 also supports full-duplex synchronous communication at 2.4, 9.6, 19.2, 64, 144, 192 and 256 kbps.

The $\overline{RTS}$, $\overline{CTS}$, $\overline{DSR}$ and $\overline{DTR}$ pins can be selectively used in one of two modes: as end-to-end communication channels, or as conventional modem control lines used in handshakes with the OPTIMODEMs (DCE). The desired mode is selected through the RS2 pin. Both modems provide extensive diagnostic and maintenance capabilities.

Efficient 3B4B line encoding is employed to ensure accurate transmission of data regardless of ones density. The 3B4B line code technique generates a four-bit binary code which corresponds to three binary input bits. This DC balanced code provides sufficient ones density to satisfy the requirements of the receiver's phase-lock loop while optimizing transmission bandwidth and reducing noise. At the receive end, the four-bit code is converted back to the original three bits before being output on RxD.

The CS8123/4 minimizes the number of external components required, using just one LED to both send and receive data on a single fiber. The CS8123/4 can support cables up to 2000 meters as discussed in the section on LED requirements in the *Applications* section which appends this data sheet. Total transmission delay through two OPTIMODEMs and 2 km of cable will be a maximum of 100 µs.

Transmit Section

In the asynchronous mode, the TxC clock is not used and the CS8123/4 accepts data asynchronously on the TxD input pin. The TxD input is oversampled by at least 7.5 times, to create a 288 kbps data stream which is stored in the Transmit FIFO.

In the synchronous mode, the CS8124 accepts data on the TxD input pin using the TxC clock. This data is then stored as a succession of digital words in the Transmit FIFO. The Clock Control (CKC) input is used to select either an internally generated TxC clock or an externally provided TxC clock.

Clocks

The CS8123 operates asynchronously. The CS8124 may be operated in either the synchronous or asynchronous mode. The CS8124 provides three clock options. The OPTIMODEM's frequency reference is provided by connecting a crystal between the XTL pin and ground. Alternatively, the XTL pin may be overdriven by an external clock.

1) Asynchronous operation: DR1/2/3 = low. RxC and TxC pins of CS8124 are held in a high impedance state.

2) Synchronous with externally provided transmit clock: Not all DR1/2/3 = low; CKC = high. An externally generated clock must be input to the TxC pin at the rate selected by DR1/2/3.

3) Synchronous with internally provided transmit clock: Not all of DR1/2/3 = low; CKC = low. The CS8124 generates the transmit clock and outputs it at the TxC pin.

In the synchronous mode, the two TxC clocks at either end of the link are allowed to deviate from each other by several hundred ppm. Also,

an externally provided TxC clock can deviate from the rate selected on DR/1/2/3 by several hundred ppm. TxC clocks can be simultaneously externally provided at both ends of the link.

Receive Section

The LED detects the data burst from the far-end modem. A digital phase-lock loop performs the timing recovery to maintain synchronization between the master and slave OPTIMODEMs. The recovered signal is decoded and then stored in the Receive FIFO.

In the asynchronous mode, the recovered data is output on RxD. In the synchronous mode, bit stuffing is used to synchronize the transmit and receive data rates. The data has any stuffed bits removed during its transfer to the Receive FIFO. The Receive FIFO provides the output to the RxD pin using the RxC clock.

Digital Carrier Detect

A logical zero on the Digital Carrier Detect, ($\overline{DCD}$), output indicates that ping-pong synchronization has occurred between the near-end and far-end modems and that data transmission can occur.

Diagnostic Features

The CS8123/4 provides several capabilities to facilitate fault isolation and system performance verification. These diagnostic features are selected using the DG1, DG2, and DG3 pins. Table 1 shows the various diagnostic modes and the corresponding setting for DG1/2/3.

Forced-Slave Modes

An innovative diagnostic capability allows the user to change the synchronization algorithm. In normal operation, both OPTIMODEMs in a link start the synchronization process as peers. As synchronization start-up proceeds, either one can assume the role of "master" or "slave". This allows the user to configure the diagnostic mode pins of both OPTIMODEMs on the same link in an identical manner. Using the diagnostic input pins it is possible to force the near-end OPTIMODEM to assume the slave mode, eliminating any synchronization start-up ambiguity, and guaranteeing a minimum

DG1	DG2	DG3	Diagnostic Mode
0	0	0	Normal Full-Duplex Operation
0	0	1	Local Loopback
0	1	0	Remote Loopback
0	1	1	Remote Loopback with Forced-Slave Mode
1	0	0	Reset
1	0	1	Continuous Receive
1	1	0	Continuous Transmit
1	1	1	Full-Duplex Operation with Forced-Slave Mode

Table 1. - Diagnostic Mode Selection

start up time. However, the user must now insure that only one of the two OPTIMODEMs is in this mode.

Loopbacks

Two loopback modes are provided on the CS8123/4: local and remote loopbacks. Loopbacks are supported in both asynchronous or synchronous modes, with either internal or external TxC clock. In local loopback mode, the transmit data and clock (if applicable) inputs are looped back internal to the near-end CS8123/4 and output on the receive data and clock outputs. This allows the near-end user to verify performance up to, but not including, the near-end LED and LED interface circuit. Data is still transmitted to the far-end OPTIMODEM. Inputs to the near-end receiver from the LED are ignored and $\overline{DCD}$ is high. Local loopback takes precedence over remote loopback.

When remote loopback is selected on the near-end CS8123/4, the near-end OPTIMODEM directs the far-end OPTIMODEM to loop back its received data. This allows the user to verify performance of the complete near-end CS8123/4, the fiber, the LEDs and most of the far-end CS8123/4. The far-end OPTIMODEM also outputs received data and clock (when applicable) at RxD and RxC. When remote loopback is selected and synchronization is achieved, $\overline{DCD}$ goes low on the near-end OPTIMODEM. When remote loopback is in effect, the far-end OPTIMODEM ignores inputs on TxC and TxD and brings $\overline{DCD}$ high.

Continuous Transmit and Receive Modes

To further aid in system diagnostics, the CS8123/4 has two special operating modes: continuous transmit and continuous receive. In continuous transmit mode, the near-end CS8123/4 sends the encoded version of the data input on TxD. TxD must be clocked into the part at a rate of one-eighth the crystal frequency. As in normal operation, TxC can be either an input or an output. The 3B4B coding is still employed so the actual transmission rate is one-sixth the crystal frequency. If TxC is externally generated, its frequency can differ from the nominal frequency by several hundred ppm.

When continuous transmit is selected, the receiver is inoperative, no ping-pongs take place and $\overline{DCD}$ stays high. Measurements can then be made at the output of the near-end LED and at the far-end output of the fiber cable to isolate LED and/or cable failures.

In continuous receive mode, the receiver continually receives data and outputs the data and clock on the receive outputs, RxD and RxC. This allows performance of the LED as a receiver to be verified. $\overline{DCD}$ is held low in the continuous receive mode once synchronization is achieved. The transmitter is inactive in this mode.

Transmit Current Adjustment

The transmit current level is typically 100 mA when TCL is left unconnected. The current level may be adjusted by tying the TCL pin to ground through a resistor as shown in Figure 4. Tying TCL directly to ground selects the minimum drive current of 10 mA. The output drive current corresponding to a given resistor can be calculated using the following Equation:

$$I_{drive} = 100 \left(\frac{111 + R_{TCL}}{1111 + R_{TCL}} \right) mA$$

Equation 1.

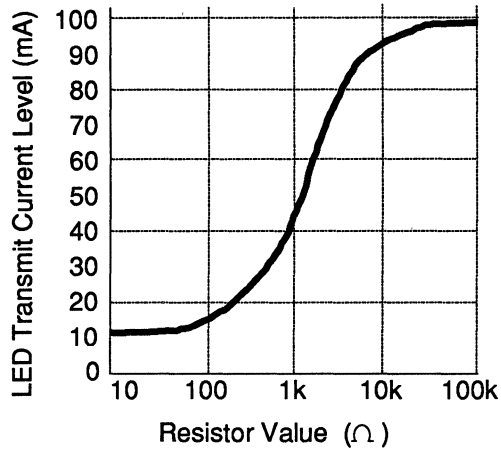
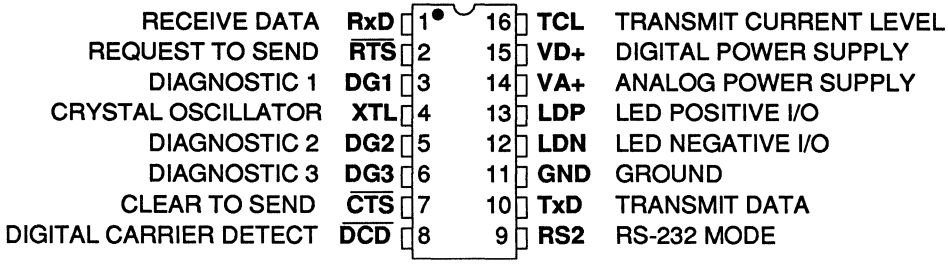
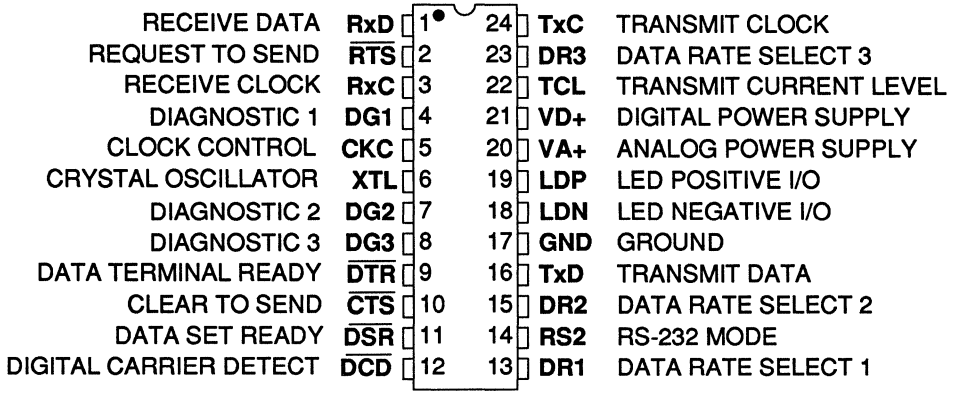


Figure 4 - Resistor to Set the Transmit Current Level



CS8123



CS8124

PIN DESCRIPTIONS

Power Supplies

VA+ - Analog Power Supply, PIN 20 on CS8124; PIN 14 on CS8123.
Typically +5 volts.

VD+ - Digital Power Supply, PIN 21 on CS8124; PIN 15 on CS8123.
Typically +5 volts.

GND - Ground, PIN 17 on CS8124; PIN 11 on CS8123.
Ground reference.

Oscillator

XTL - Crystal Oscillator, PIN 6 on CS8124; PIN 4 on CS8123.
Crystal or external clock input. There is no need for the crystal to use external capacitors or biasing resistors. The crystal, if used, should have one pin connected to XTL with minimal length trace on the printed circuit board; the other pin of the crystal should be tied to ground. Standard operation requires a 9.216 MHz (± 50 ppm) crystal or clock. Other frequencies may be used to adjust the OPTIMODEM throughput and data rates up to a maximum of 12.3 MHz.

Inputs

TxD - Transmit Data, PIN 16 on CS8124; PIN 10 on CS8123.
Data to be transmitted. In the asynchronous mode, the rate of the data can be from DC to 38.4 kbps. In the synchronous mode, data is clocked into the CS8124 on the rising edge of TxC.

TxC - Transmit Clock (CS8124 Only), PIN 24.
When CKC is low, TxC will output a clock at the rate selected by DR1/DR2/DR3. When CKC is high, TxC accepts input clock from an external source. TxC goes into a high impedance state when asynchronous operation is selected. For synchronous operation TxD is sampled on the rising edge of TxC.

CKC - Clock Control (CS8124 Only), PIN 5.
Defines the source of the clock signal on TxC for synchronous operation. A high on CKC indicates that external clock is being input on TxC. A low on CKC indicates the the CS8124 is sending out TxC at one of the rates selected on the DR1/DR2/DR3 data rate selection inputs. If CKC is left unconnected (floating), CKC pulls low, selecting the internal clock.

DR1; DR2; DR3 - Data Rate 1; 2; 3 (CS8124 Only), PINS 13, 15, 23.

Select a data rate for the TxC and RxC pins as shown in Table 2. If these pins are left unconnected (floating), the CS8124 defaults to asynchronous operation.

DR1	DR2	DR3	Data Rate (kbps) with 9.216 MHz crystal
0	0	0	Async : dc to 38.4
0	0	1	2.4
0	1	0	9.6
0	1	1	19.2
1	0	0	64
1	0	1	144
1	1	0	192
1	1	1	256

Note that a 56 kbps link can be implemented by using a 8.064MHz crystal and the 64 kbps data rate selection.

Table 2 - Data Rate Selection

DG1; DG2; DG3 - Diagnostic 1; 2; 3, PINS 4, 7, 8 on CS8124; PINS 3, 5, 6 on CS8123.

Select a diagnostic mode as shown in Table 1 in the *Circuit Description* section. If these pins are left unconnected, (floating), the OPTIMODEM assumes the mode for Normal Operation.

RS2 - RS-232C Control Mode Select, PIN 14 on CS8124; PIN 9 on CS8123.

Selects whether the $\overline{\text{CTS}}$, $\overline{\text{RTS}}$, $\overline{\text{DSR}}$ and $\overline{\text{DTR}}$ are used in an end-to-end mode, or modem control handshake mode. When RS2 is low, the end-to-end mode is in effect as shown in Figure 5. If RS2 is left unconnected, (floating), the end-to-end mode is in effect.

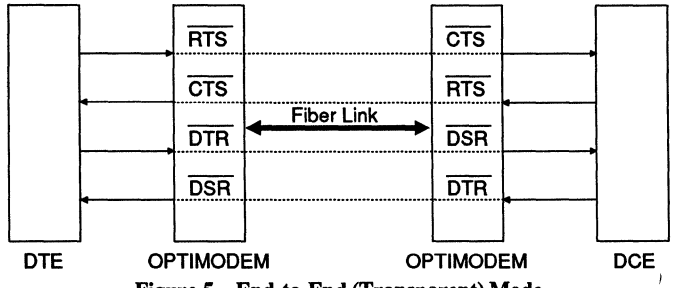


Figure 5. - End-to-End (Transparent) Mode

When RS2 is high, the modem control mode, as shown in Table 3, is in effect:

OPTIMODEM (DCE)	DTE
1. Modem powers up, then asserts $\overline{DSR}$.	1. DTE initializes, then asserts $\overline{DTR}$.
2. Recognizes $\overline{DTR}$ and begins ping-pong synchronization.	2. Recognizes $\overline{DSR}$ and waits for $\overline{DCD}$.
3. When Synchronization is achieved, asserts $\overline{DCD}$.*	3. Recognizes $\overline{DCD}$, then asserts $\overline{RTS}$.
4. Recognizes $\overline{RTS}$, then asserts $\overline{CTS}$.**	4. Recognizes $\overline{CTS}$, then starts communication with far end.

* If synchronization is lost, modem takes $\overline{DCD}$ and $\overline{CTS}$ high.
** If $\overline{RTS}$ goes high, modem takes $\overline{CTS}$ high.

Table 3. - Modem Control Mode

$\overline{DTR}$ - Data Terminal Ready (CS8124 Only), PIN 9.

In the end-to-end mode, data input on $\overline{DTR}$ is transmitted over the link and presented at the far end as the $\overline{DSR}$ output. In the modem control mode, a logical low indicates that the DTE is powered up and initialized.

$\overline{RTS}$ - Request To Send , PIN 2 on CS8124 and CS8123.

In the end-to-end mode, the $\overline{RTS}$ input is transmitted over the link and presented at the far end as the $\overline{CTS}$ output. In the modem control mode, a logical low indicates that the DTE is ready to communicate to the far end.

TCL - Transmit Current Level, PIN 22 on CS8124; PIN 16 on CS8123.

Defines the current driven into LDP/LDN. When left unconnected, the current level is typically 100mA. When tied to ground, output current level is at a minimum of about 10 mA. Current can be set at an intermediate level, (as shown in Figure 4 in the *Circuit Description* section), by tying this pin to ground through a resistor.

Outputs

$\overline{DCD}$ - Digital Carrier Detect, PIN 12 on CS8124; PIN 8 on CS8123.

A low level indicates that synchronization has occurred between the far-end and near-end modems, and that end-to-end transmissions can occur on the $\overline{DTR}$/$\overline{DSR}$, $\overline{CTS}$/$\overline{RTS}$ and TxD/RxD channels. $\overline{DCD}$ is high on the OPTIMODEM for which local loopback has been selected, and during a remote loopback selected by the far-end terminal. $\overline{DCD}$ is low when continuous receive is selected or when a remote loopback selected by the near-end modem and synchronization is achieved. $\overline{DCD}$ is high when continuous transmit has been selected.

$\overline{\text{CTS}}$ - Clear To Send, PIN 10 on CS8124; PIN 7 on CS8123.

In the end-to-end mode, CTS shows the state of the far-end $\overline{\text{RTS}}$ input. Each $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ pair can be used as a half duplex, 1.2 kbps data channel. The channel is always asynchronous for both the CS8123 and the CS8124, being oversampled at a rate of approximately 12 kHz.

In the modem control mode (RS2 = high), a logical low indicates that the DTE can begin transmission over the TxD and RxD pins.

$\overline{\text{DSR}}$ - Data Set Ready (CS8124 Only), PIN 11.

In the end-to-end mode, $\overline{\text{DSR}}$ outputs the data input on the far end $\overline{\text{DTR}}$ pin. Each $\overline{\text{DSR}}$/$\overline{\text{DTR}}$ pair can be used as a half duplex, 1.2 kbps data channel. The channel is always asynchronous for both the CS8123 and the CS8124, being oversampled at a rate of approximately 12 kHz.

In the modem control mode (RS2 = high), a logical low indicates that the OPTIMODEM is powered up.

RxD - Received Data, PIN 1 on CS8124 and CS8123.

The data can be read asynchronously (in that mode) or is valid on the rising edge of RxC (in the synchronous mode).

RxC - Received Clock (CS8124 only), PIN 3.

In the synchronous mode, RxD is valid and stable on the rising edge of RxC. RxC goes into a high impedance state when asynchronous operation is selected.

Inputs/Outputs

LDP; LDN - LED Positive I/O; LED Negative I/O, PIN 19 & 18 on CS8124; PINS 13 & 12 on CS8123.

These bidirectional pins connect directly to the LED, and alternately drive and receive from the LED. LDP connects to the LED anode and LDN connects to the LED cathode. It is absolutely critical that LED be connected to LDP and LDN with the shortest possible traces on the printed circuit board.

APPLICATION NOTES

The OPTIMODEMs at opposite ends of the link must be within 50 °C of each other to insure operation of the link. This requirement results from the fact the LED emission spectrum shifts with temperature, as does the responsivity peak. To insure sufficient overlap of emission and responsivity bands the two ends must be within 50 °C of each other.

LED Requirements

Table A1 shows the distance ranges that should be realized with LEDs from various vendors, on a variety of fiber optic cable types. Some specifications for the various cable types are given in Table A3. These calculations are based upon data gathered during a characterization activity performed by Crystal Semiconductor.

The target LED specifications are given in Table A2, and some suggested LEDs are listed below table A1.

Power Supply Decoupling

V+A, V+D and GND should be decoupled using the circuit shown in Figure A1. The 68 µF capacitor is required to filter the power supply, and prevent power supply ripple. Ripple can occur at the power supply pins of the device as a result of the different current demands when the OPTIMODEM is transmitting or receiving.

Cable Type	DISTANCE	
	Cable ends at the same temperature	Cable ends different by 50 deg. C.
200 PCS	2000	1000
100/140 um	2000	1000
85/125 um	1400	700
62.5/125 um	1000	500
50/125 um	100	50
1000 um Plastic	12	6

Table A1 - Cable Lengths Supported (meters)

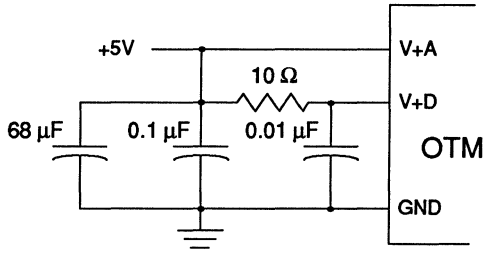


Figure A1 - Power Supply Decoupling

The requirement for the 68 µF capacitor can be reduced if a solid, well filtered power supply is used and good power and ground planes are utilized on the circuit board. The greater the resistance of the power and ground traces on the PC board, the greater the need for a large power supply filter capacitor, placed in close proximity to the OPTIMODEM.

Because of the sensitivity of the analog circuitry to power supply noise, evaluation of the OPTIMODEM using wire-wrapped boards is not recommended.

Vendor	Part Number
Honeywell	HFE4000-904
Hewlett Packard	HFBR1405

Approved LED Vendors

RECOMMENDED LED SPECIFICATIONS (T_A = 25°C, V+ = 5V ± 5%, GND = 0V)

Parameter	Symbol	Min	Max	Units	Conditions
Forward Voltage	V_F	1.4	2.2	V	I_F = 100mA
Breakdown Voltage	V_{BR}	-1.8	-	V	I_R = 100uA
Series Resistance	r_S	-	10	Ohms	dc
Diode Capacitance (Note A1)	C_T	-	150	pF	Vr = 0V f = 1 MHz
Fiber Coupled Power	P_{OC}	40	-	uW	I_F = 50mA 100 um Graded NA = 0.29
P_{oc} Temperature Coefficent (Note A2)	$\Delta P_{oc}/\Delta T$	-0.025	-	dB/°C	
Response Time	t_r, t_f	-	10	ns	10 -90% I_F=100mA No Pre-Bias
Responsivity	R_o	0.025	-	A/W	V_R = 0V
R_o Temperature Coeff. (Notes A2 & A3)	$\Delta R_o/\Delta T$	-0.3	-	mA/ W-°C	V_R = 0V
Leakage Current	I_D	-	1.0	uA	V_R = 0V

Table A2. - LED Specifications

Notes: A1. $\sigma \leq 25\%$.
A2. Industrial Temperature Range (-40°C to 85°C).
A3. Includes Spectral Variance.

Type	Numerical Aperture	Attenuation (dB per km)
200 um PCS	0.40	6.0
100/140 um	0.29	6.0
85/125 um	0.26	5.5
62.5/125 um	0.28	5.0
50/125 um	0.20	4.0
1000 um Plastic	0.50	1000

Table A3 - Cable Specifications

Semiconductor Corporation

CS8125/6

Optical Transmitter/Receiver

Features

- Supports Links at 1.544 MHz up to 7 km
- Receiver Sensitivity: 30 nA to 30 uA , -42 dBm (assuming R=0.5 nA/nW)
- Selectable Transmit Power Levels, 60 mA and 12 mA
- Optical Dynamic Range of 30 dB
- Monolithic Clock Recovery
- 3B4B Line Encoding/Decoding

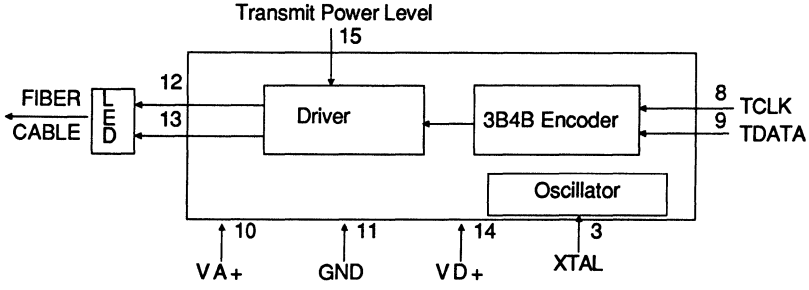
General Description

The CS8125 and CS8126 from Crystal Semiconductor Corporation are SMART Analog™ interface devices that receive and transmit serial binary data at T1 rates over two fiber-optic cables. Together, they provide filtering, modulation, demodulation, line encoding/decoding, & clock recovery.

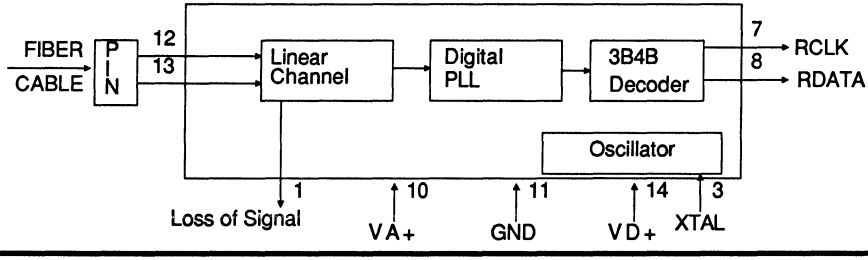
ORDERING INFORMATION
CS8125 - 16 Pin Plastic DIP
CS8126 - 16 Pin Plastic DIP

5

CS8125 Transmitter



CS8126 Receiver



Product Preview

This document contains data for a new product . Crystal Semiconductor reserves the right to modify this product without notice.

SEP '87
DS33PP1

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, Texas 78760
(512)445-7222 TWX:910-874-1352

• Notes •

INTRODUCTION

Crystal offers a line of monolithic self-calibrating A/D converters which can recalibrate at any time or temperature, thus ensuring accuracy throughout their operating lives. The CS5012, CS5014 and CS5016 converters range from 12 to 16 bits of resolution and are ideal for instrumentation and control applications. They include on-chip interfaces to 8 to16-bit microprocessors. All converters feature integral track-and-hold functions that convert ac signals without loss of accuracy. On-chip self-calibration ensures that linearity, offset and full-scale errors remain within 1/2 LSB with no missing codes. Calibration can be initiated upon hardware or software command. The converters can also be placed in transparent background calibration modes.

Crystal's industry standard CS7820 8-bit sampling A/D is an extremely cost-effective solution to many general purpose conversion requirements. The inherent track-and-hold input is matched with a 1.36 µs maximum conversion time and easy interfacing to microprocessors. A pin-for-pin replacement for competitive parts, the CS7820 has aggressive pricing and deliveries, complemented by Crystal's unsurpassed quality and reliability standards.

USER'S GUIDE

Device:	CS5016	CS5014	CS5012	CS7820
Resolution (Bits)	16	14	12	8
Conversion Technique	Succ. Approx.	Succ. Approx.	Succ. Approx.	2-Stage Flash
Conversion Time, Max (µSEC)	16	14	7	1.36
Linearity Error, Max	+/- 0.0015%	+/- 0.003%	+/- 0.012%	+/- 0.5 LSB
No Missing Codes, Min (Bits)	16	14	12	8
Power Dissipation (mW)	120	120	120	40
On-Chip Sample/Hold	♥	♥	♥	♥
Temperature Ranges	Com, Ind, Mil	Com, Ind, Mil	Com, Ind, Mil	Com, Ind, Mil
Package	40-Pin DIP	40-Pin DIP	40-Pin DIP	20-Pin DIP

CONTENTS

Semiconductor Corporation

CS5012

12-Bit, 7us Self-Calibrating A/D Converter

Features

- Monolithic CMOS A/D Converter
  - Microprocessor Compatible
  - Parallel and Serial Output
  - Inherent Track/Hold Input
- True 12-Bit Precision
  - Linearity Error: ± 1/4 LSB
  - Total Unadjusted Error: ± 1/4 LSB
  - No Missing Codes
- 7.2 Microsecond Conversion Time
  - Throughput Rates up to 100kHz
- Self Calibration Maintains Accuracy Over Time and Temperature
- Low Power Dissipation: 120mW
- Pin Compatible with CS5014/CS5016

General Description

The CS5012 is a 12-bit monolithic CMOS analog to digital converter with 7.2 microsecond conversion time. Unique self-calibration circuitry, which can be under intelligent control, insures maximum nonlinearity of 1/2 LSB and no missing codes. Offset and full scale errors are kept within 1/2 LSB, eliminating the need for manual calibration of any kind. Unipolar and bipolar input ranges are digitally selectable.

The CS5012 consists of a DAC, conversion and calibration microcontroller, oscillator, comparator, microprocessor compatible 3-State I/O, and calibration circuitry. The input track-and-hold, inherent to the device's sampling architecture, acquires the analog input signal after each conversion within 2.8us to 0.01%, allowing throughput rates up to 100kHz.

The CS5012 is pin compatible with the CS5014 and CS5016 A/D converters allowing system upgrading and downgrading without hardware alterations.

ORDERING INFORMATION: Page 29

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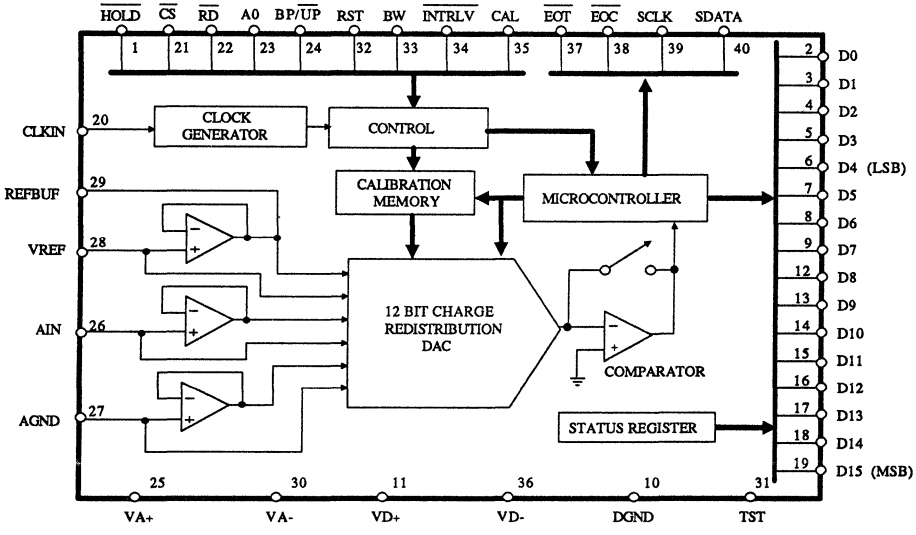


Crystal Semiconductor Corporation
P.O. Box 17847, Austin, Texas 78760
(512)445-7222 TWX:910-874-1352

ANALOG CHARACTERISTICS

(T_A = 25°C; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 2.5V to 4.5V;
f_{clk} = 6.8MHz for -7, 4MHz for -12, 2MHz for -24; Analog Source Impedance = 200Ω unless otherwise specified.)

Parameter *		CS5012-K min	CS5012-K typ	CS5012-K max	CS5012-B min	CS5012-B typ	CS5012-B max	CS5012-T min	CS5012-T typ	CS5012-T max	Units
Specified Temperature Range			0 to +70			-40 to +85			-55 to +125		°C
Accuracy											
Linearity Error	Note 1		± 1/4	± 1/2		± 1/4	± 1/2		± 1/4	± 1/2	LSB
T_{min} to T_{max}	Note 2		± 1/8			± 1/4			± 1/4		ΔLSB
Differential Linearity	Note 1		± 1/4	± 1/2		± 1/4	± 1/2		± 1/4	± 1/2	LSB
T_{min} to T_{max}	Note 2		± 1/32			± 1/32			± 1/32		ΔLSB
Full Scale Error	Note 1		± 1/4	± 1/2		± 1/4	± 1/2		± 1/4	± 1/2	LSB
T_{min} to T_{max}	Note 2		± 1/16			± 1/16			± 1/8		ΔLSB
Unipolar Offset	Note 1		± 1/4	± 1/2		± 1/4	± 1/2		± 1/4	± 1/2	LSB
T_{min} to T_{max}	Note 2		± 1/16			± 1/16			± 1/8		ΔLSB
Bipolar Offset	Note 1		± 1/4	± 1/2		± 1/4	± 1/2		± 1/4	± 1/2	LSB
T_{min} to T_{max}	Note 2		± 1/16			± 1/8			± 1/8		ΔLSB
Bipolar Negative Full-Scale Error											
	Note 1		± 1/4	± 1/2		± 1/4	± 1/2		± 1/4	± 1/2	LSB
T_{min} to T_{max}	Note 2		± 1/16			± 1/4			± 1/4		ΔLSB
Total Unadjusted Error	Note 1		± 1/4			± 1/4			± 1/4		LSB
T_{min} to T_{max}	Note 2		± 1/4			± 1/4			± 1/4		ΔLSB
Noise	Unipolar Mode		45			45			45		uV_{rms}
(Note 3)	Bipolar Mode		90			90			90		uV_{rms}
Analog Input											
Aperture Time			25			25			25		ns
Aperture Jitter			100			100			100		ps
Aperture Time Matching	(Note 4)		TBD			TBD			TBD		ns
Full Power Bandwidth	(Note 5)		32			32			32		kHz
Input (Note 6)	Unipolar Mode		275	375		275	375		275	375	pF
Capacitance	Bipolar Mode		165	220		165	220		165	220	pF

Notes:
1. Applies after calibration at any temperature within the specified temperature range.
2. Total drift over specified temperature range since calibration at power-up at 25°C.
3. Wideband noise aliased into the baseband. Referred to the input.
4. Part to part.
5. V_{in} = 9V p-p. Refer to *Analog Input* section on page 17 for discussion of input slew rate.
6. Applies only in track mode. When converting or calibrating, input capacitance will not exceed 15pF.

* Refer to *Error Definitions* on page 28.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (continued)

Parameter		CS5012-K min	typ	max	CS5012-B min	typ	max	CS5012-T min	typ	max	Units
Conversion & Throughput											
Conversion Time	– 7			7.2			7.2			-	us
	–12			12.25			12.25			12.25	us
(Notes 7,8)	–24			24.5			24.5			24.5	us
Acquisition Time	– 7		2.5	2.8		2.5	2.8		-	-	us
	–12		3.0	3.75		3.0	3.75		3.0	3.75	us
(Note 8)	–24		4.5	5.25		4.5	5.25		4.5	5.25	us
Throughput	– 7	100			100			-			kHz
	–12	62.5			62.5			62.5			kHz
(Note 8)	–24	33.6			33.6			33.6			kHz
Power Supplies											
DC Power Supply Currents	(Note 9)										
I_{A+}			9	19		9	19		9	19	mA
I_{A-}			-9	-19		-9	-19		-9	-19	mA
I_{D+}			3	6		3	6		3	6	mA
I_{D-}			-3	-6		-3	-6		-3	-6	mA
Power Dissipation	(Note 9)		120	250		120	250		120	250	mW
Power Supply Rejection	(Note 10)										
Positive Supplies			84			84			84		dB
Negative Supplies			84			84			84		dB

Notes:
7. Measured from falling transition on $\overline{HOLD}$ to falling transition on $\overline{EOC}$.
8. Conversion, acquisition, and throughput times depend on the master clock, sampling, and calibration conditions. The numbers shown assume sampling and conversion is synchronized with the CS5012's conversion clock, interleave calibrate is disabled, and operation is from the full-rated external clock. A detailed discussion of conversion timing appears on page 11.
9. All outputs unloaded. All inputs CMOS levels.
10. With 300mV p-p, 1kHz ripple applied to each analog supply separately in bipolar mode. Rejection improves by 6dB in the unipolar mode to 90dB. A plot of typical power supply rejection versus frequency appears on page 21.

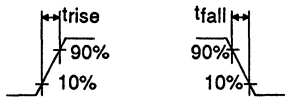
6

SWITCHING CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 50pF)

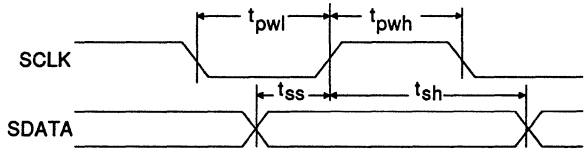
Parameter	Symbol	Min	Typ	Max	Units
Master Clock Frequency:					
Internally Generated: - 7	f_{CLK}	2.4	-	-	MHz
- 12		2.4	-	-	
- 24		1.0	-	-	
Externally Supplied: - 7		-	-	6.8	
- 12		-	-	4	
- 24		-	-	2	
Master Clock Duty Cycle	-	30	-	70	%
Rise Times: Any Digital Input	t_{rise}	-	-	1.0	us
Any Digital Output		-	20	-	ns
Fall Times: Any Digital Input	t_{fall}	-	-	1.0	us
Any Digital Output		-	20	-	ns
$\overline{HOLD}$ Pulse Width	t_{hpw}	$1/f_{CLK} + 50$	-	t_c	ns
Conversion Time	t_c	(Note 11)	-	(Note 11)	us
Data Delay Time	t_{dd}	-	40	100	ns
$\overline{EOC}$ Pulse Width (Note 12)	t_{epw}	$4/f_{CLK} - 20$	-	-	ns
Set Up Times: CAL, $\overline{INTRLV}$ to $\overline{CS}$ Low	t_{cs}	20	10	-	ns
A0 to $\overline{CS}$ and $\overline{RD}$ Low	t_{as}	20	10	-	
Hold Times:					
$\overline{CS}$ or $\overline{RD}$ High to A0 Invalid	t_{ah}	50	30	-	ns
$\overline{CS}$ High to CAL, $\overline{INTRLV}$ Invalid	t_{ch}	50	30	-	
Access Times: $\overline{CS}$ Low to Data Valid					
-K, B	t_{ca}	-	90	120	ns
-T		-	115	150	
$\overline{RD}$ Low to Data Valid					
-K, B	t_{ra}	-	90	120	ns
-T		-	115	150	
Output Float Delay: -K, B	t_{fd}	-	50	110	ns
$\overline{CS}$ or $\overline{RD}$ High to Output Hi-Z -T			50	140	
Serial Clock Pulse Width Low	t_{pwl}	-	$2/f_{CLK}$	-	ns
Pulse Width High	t_{pwh}	-	$2/f_{CLK}$	-	
Set Up Times: SDATA to SCLK Rising	t_{ss}	$2/f_{CLK} - 100$	$2/f_{CLK}$	-	ns
Hold Times: SCLK Rising to SDATA	t_{sh}	$2/f_{CLK} - 100$	$2/f_{CLK}$	-	ns

Notes: 11. See Table 1 and master clock frequencies above.

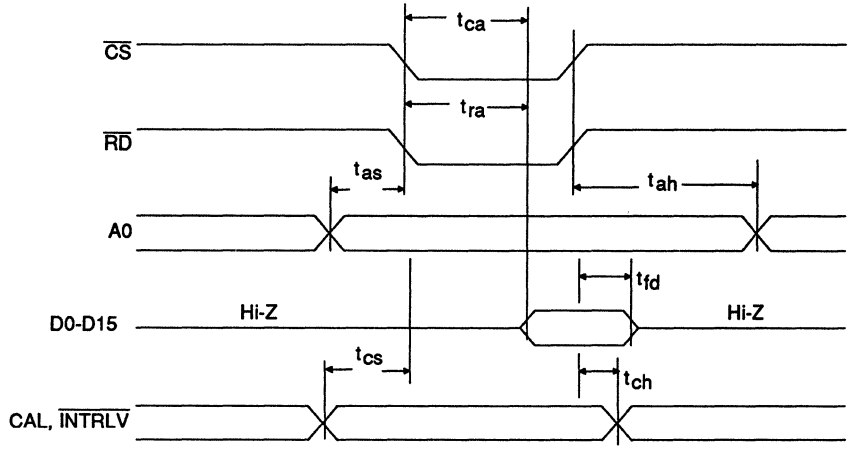
12. $\overline{EOC}$ remains low 4 master clock cycles if $\overline{CS}$ and $\overline{RD}$ are held low. Otherwise, it returns high within 4 master clock cycles from the start of a data read operation or a conversion cycle.



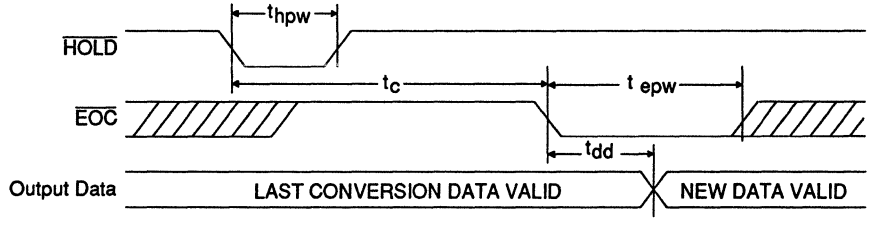
Rise and Fall Times



Serial Output Timing



Read and Calibration Control Timing



Conversion Timing

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%)

All measurements below are performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 13)	V_{OH}	VD+ - 1.0V	-	-	V
Low-Level Output Voltage Iout=1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	10	uA
3-State Leakage Current	I_{OZ}	-	-	±10	uA
Digital Output Pin Capacitance	C_{out}	-	9	-	pF

Note: 13. I_{out} = -100µA. This specification guarantees TTL compatability (VOH = 2.4V @ I_{out} = -40µA).

RECOMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see note 14.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.5	5.0	VA+	V
	Negative Digital	VD-	−4.5	−5.0	−5.5	V
	Positive Analog	VA+	4.5	5.0	5.5	V
	Negative Analog	VA-	−4.5	−5.0	−5.5	V
Analog Reference Voltage		VREF	2.0	-	VA+ - 0.5	V
Analog Input Voltage: (Note 15)	Unipolar	V_{AIN}	AGND	-	VREF	V
	Bipolar	V_{AIN}	-VREF	-	VREF	V

Notes: 14. All voltages with respect to ground.

15. The CS5012 can accept input voltages up to the analog supplies (VA+ and VA-). It will output all 1's for inputs above VREF and all 0's for inputs below AGND in unipolar mode and -VREF in bipolar mode.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to ground)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	−0.3	VA+ + 0.3	V
	Negative Digital	VD-	0.3	−6.0	V
	Positive Analog	VA+	−0.3	6.0	V
	Negative Analog	VA-	0.3	−6.0	V
Input Current, Any Pin Except Supplies (Note 16)		I_{in}	-	±10	mA
Analog Input Voltage (AIN and VREF pins)		V_{INA}	VA- - 0.3	VA+ + 0.3	V
Digital Input Voltage		V_{IND}	-0.3	VA+ + 0.3	V
Ambient Operating Temperature		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

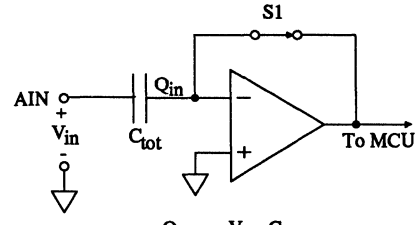
Note: 16. Transient currents of up to 100mA will not cause SCR latch up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guarateed at these extremes.

THEORY OF OPERATION

The CS5012 utilizes the most popular method of executing high-speed, high-resolution A/D conversion: successive approximation. As with all other iterative comparison methods, the analog input is successively compared to the output of a D/A converter controlled by the conversion algorithm. Successive approximation begins by comparing the analog input to the DAC output which is set to half-scale (MSB on, all other bits off). If the input is found to be below half-scale, the MSB is reset to zero and the input is compared to one-quarter scale (next MSB on, all others off). If the input were above half-scale, the MSB would remain high and the next comparison would be at three-quarters of full scale. This procedure continues until all bits have been exercised.

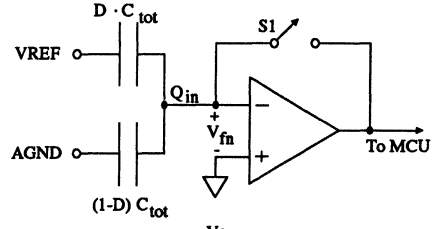
The CS5012 implements the successive-approximation algorithm using a unique charge-redistribution architecture. Instead of the traditional resistor network, the DAC is an array of binary-weighted capacitors. All capacitors in the array share a common node at the comparator's input. Their other terminals are capable of being connected to AIN, AGND, or VREF (Figure 1). When the device is not calibrating or converting, all capacitors are tied to AIN forming C_{tot}. Switch S1 is closed and the charge on the array, Q_{in}, tracks the input signal V_{in} (Figure 2a).



$$-Q_{in} = V_{in}\ C_{tot}$$

Figure 2a. Tracking Mode

When the conversion command is issued, switch S1 opens as shown in Figure 2b. This traps charge Q_{in} on the comparator side of the capacitor array and creates a floating node at the comparator's input. The conversion algorithm operates on this fixed charge, and the signal at the analog input pin is ignored. In effect, the entire DAC capacitor array serves as analog memory during conversion much like a hold capacitor in a sample/hold amplifier.



$$D = \frac{V_{in}}{VREF} \text{ for } V_{fn} = 0V$$

Figure 2b. Convert Mode

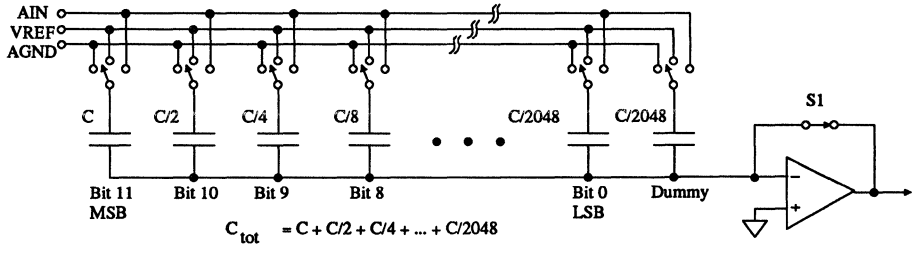


Figure 1. Charge Redistribution DAC

The conversion consists of manipulating the free plates of the capacitor array to VREF and AGND to form a capacitive divider. Since the charge at the floating node remains fixed, the voltage at that point depends on the proportion of capacitance tied to VREF versus AGND. The successive-approximation algorithm is used to find the proportion of capacitance, termed D in Figure 2b, which when connected to the reference will drive the voltage at the floating node (V_{fn}) to zero. That binary fraction of capacitance represents the converter's digital output.

The CS5012's charge redistribution architecture easily supports bipolar input ranges. If half the capacitor array (the MSB capacitor) is tied to VREF rather than AIN in the track mode, the input range is doubled and is offset half-scale. The magnitude of the reference voltage thus defines both positive and negative full-scale (-VREF to +VREF), and the digital code is an offset binary representation of the input.

Calibration

The ability of the CS5012 to convert accurately to 12-bits clearly depends on the accuracy of its comparator and DAC. The CS5012 utilizes an "auto-zeroing" scheme to null errors introduced by the comparator. All offsets are stored on the capacitor array while in the track mode and are effectively subtracted from the input signal when a conversion is initiated. Auto-zeroing enhances power supply rejection at frequencies well below the conversion rate.

To achieve 12-bit accuracy from the DAC, the CS5012 uses a novel self-calibration scheme. Each bit capacitor shown in Figure 1 actually consists of several capacitors which can be manipulated to adjust the overall bit weight. During calibration, an on-chip microcontroller adjusts the sub-arrays to precisely ratio the bits. Each bit is adjusted to just balance the sum of all less significant bits plus one dummy LSB (for example, 16C = 8C + 4C + 2C + C + C). Calibration resolution for the array is a small fraction of an LSB resulting in nearly ideal differential and integral linearity.

DIGITAL CIRCUIT CONNECTIONS

The CS5012 can be applied in a wide variety of master clock, sampling, and calibration conditions which directly affect the device's conversion time and throughput. The device also features on-chip 3-state output buffers and a complete interface for connecting to 8-bit and 16-bit digital systems. Output data is also available in serial format.

Master Clock

The CS5012 operates from a master clock which can be externally supplied or internally generated. The internal oscillator is activated by externally tying the CLKIN input low. Alternatively, the CS5012 can be synchronized to the external system by driving the CLKIN pin with a TTL or CMOS clock signal.

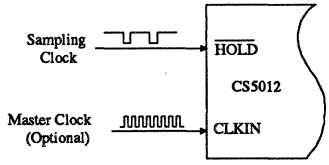


Figure 3a. Asynchronous Sampling

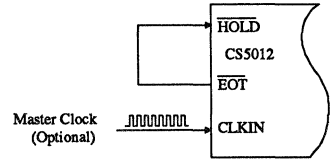


Figure 3b. Synchronous Sampling

All calibration, conversion, and throughput times directly scale to master clock frequency. Thus, throughput can be precisely controlled and/or maximized using an external master clock. In contrast, the CS5012's internal oscillator will vary from unit-to-unit and over temperature. Its tolerance gives rise to minimum and maximum conversion times and throughput rates. The -7 version of the CS5012 is specified for accurate operation with an external clock up to 6.8MHz; its internal clock frequency is specified at a minimum of 2.4MHz. The -12 version is specified for accurate operation with an external clock up to 4MHz; its internal clock frequency is specified at a minimum of 2.4MHz. The -24 version can handle external clocks up to 2MHz; its internal clock can range as low as 1.0MHz (see *Switching Characteristics*, page 6). Each version can typically convert with clocks as low as 10kHz at room temperature.

Initiating Conversions

A falling transition on the $\overline{\text{HOLD}}$ pin places the input in the hold mode and initiates a conversion cycle. The $\overline{\text{HOLD}}$ input is latched internally by the master clock, so it can return high anytime after one master clock cycle plus 50ns. Upon completion of the conversion cycle, the CS5012 automatically returns to the track mode. In contrast to systems with separate track-and-holds and A/D converters, a sampling clock can simply be connected to the $\overline{\text{HOLD}}$ input (Figure 3a). The duty cycle of this clock is not critical. It need only remain low at least one master clock cycle plus 50ns, but no longer than the minimum conversion time or an additional conversion cycle will be initiated with inadequate time for acquisition.

Microprocessor-Controlled Operation

Sampling and conversion can be placed under microprocessor control (Figure 4) by simply gating the device's decoded address with the write strobe for the $\overline{\text{HOLD}}$ input. Thus, a write cycle to the CS5012's base address will initiate a conversion (the data word is irrelevant). However, the write cycle must be to the odd address (A0 high) to avoid initiating a software controlled reset (see *Reset*, page 13).

The calibration control inputs, CAL, and $\overline{\text{INTRLV}}$ are also internally latched by $\overline{\text{CS}}$, so they must be in the appropriate state whenever the chip is selected during a read or write cycle. Address lines A1 and A2 are shown connected to CAL and $\overline{\text{INTRLV}}$ in Figure 4 placing calibration under microprocessor control as well. Thus, any read or write cycle to the CS5012's base address will initiate or terminate calibration.

Conversion Time/Throughput

Upon completing a conversion cycle and returning to the track mode, the CS5012 requires time to acquire the analog input signal before another conversion can be initiated. The acquisition time

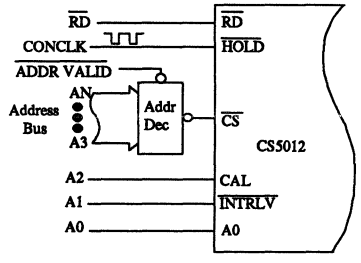


Figure 4a. Conversions Asynchronous to Master Clock

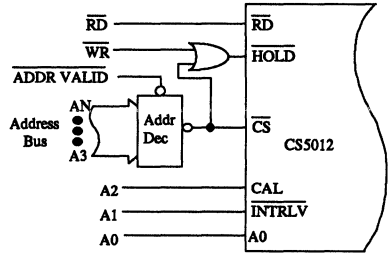


Figure 4b. Conversions under Microprocessor Control

is specified as six master clock cycles plus 2.25µs (1.32µs for the -7 version only). This adds to the conversion time to define the converter's maximum throughput. The conversion time of the CS5012, in turn, depends on the sampling, calibration, and master clock conditions.

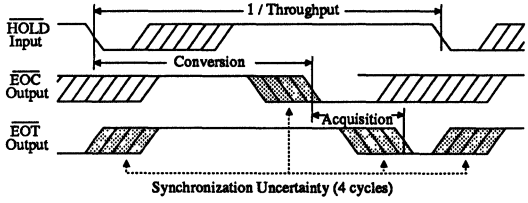


Figure 5a. Asynchronous Sampling (External Clock)

Asynchronous Sampling

The CS5012 internally operates from a clock which is delayed and divided down from the master clock ($f_{CLK}/4$). If sampling is not synchronized to this internal clock, the conversion cycle may not begin until up to four clock cycles after $\overline{HOLD}$ goes low *even though the charge is trapped immediately*. In this asynchronous mode (Figure 3a), the four clock cycles add to the minimum 49 clock cycles to define the maximum conversion time (see Figure 5a and Table 1).

Synchronous Sampling

To achieve maximum throughput, sampling can be synchronized with the internal conversion clock by connecting the End-of-Track ($\overline{EOT}$) output to $\overline{HOLD}$ (Figure 3b). The $\overline{EOT}$ output falls 15 master clock cycles after $\overline{EOC}$ indicating the analog input has been acquired to the CS5012's specified accuracy. The $\overline{EOT}$ output is synchronized to the internal conversion clock, so the four clock cycle synchronization uncertainty is removed yielding throughput at 1/64th of the master clock frequency (see Figure 5b and Table 1).

Also, the CS5012's internal RC oscillator exhibits significant jitter (typically ± 0.05% of its period), which is high compared to crystal oscillators. If the CS5012 is configured for synchronous sampling while operating from its internal oscillator, this jitter will directly affect sampling purity.

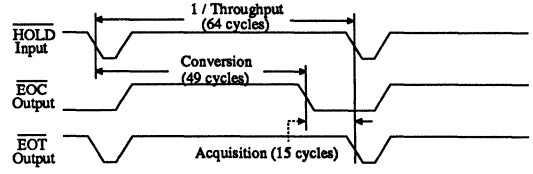


Figure 5b. Synchronous (Loopback) Mode

The $\overline{EOT}$ output is an accurate indicator of the CS5012's acquisition requirement when operating at the -7 version's full rated speed (with a 6.8MHz master clock). However, $\overline{EOT}$ will allow the CS5012 more acquisition time than necessary when operating with a clock less than 6.8MHz. The $\overline{EOT}$ output always falls 15 master clock cycles after $\overline{EOC}$. When operating the -24

	Conversion Time		Throughput Time	
Sampling Mode	min	max	min	max
Synchronous (Loopback)	49T	49T	64T	64T
Asynchronous	49T	53T + 235ns	N/A	59T + 2.25µs (+1.32µs for -7 version only)

(T ≡ one master clock cycle)

Table 1. Conversion and Throughput Times

with a master clock of 2MHz or less, higher throughput can be achieved than in the loopback configuration by using an external counter. The counter should be reset by the falling edge of $\overline{EOC}$ and count the appropriate number of clock cycles after each conversion. When the total time is greater than six clock cycles plus 2.25µs the counter can trigger a new conversion at $\overline{HOLD}$. For example, when using a 2MHz clock, 2.25µs takes between four and five clock cycles. When six cycles are added to this it is seen that the counter should trigger a new conversion at the eleventh clock cycle.

Reset

Upon power up, the CS5012 must be reset to guarantee a consistent starting condition and initially calibrate the device. Due to the CS5012's low power dissipation and low temperature drift, no warm-up time is required before reset to accommodate any self-heating effects. However, the voltage reference input should have stabilized to within 5% of its final value before RST falls to guarantee an accurate calibration. Later, the CS5012 may be reset at any time to initiate a single full calibration. Reset overrides all other functions. If reset, the CS5012 will clear and initiate a new calibration cycle mid-conversion or mid-calibration.

Resets can be initiated in hardware or software. The simplest method of resetting the CS5012 involves strobing the RST pin high. When RST is brought high all internal logic clears. When it returns low a full calibration begins which takes 1,443,840 master clock cycles (approximately 360ms with a 4MHz clock) to complete. A simple power-on reset circuit can be built using a resistor and capacitor, and a Schmidt-trigger inverter to prevent oscillation (see Figure 6). The CS5012 can also be reset in software when under microprocessor control. The CS5012 will reset whenever $\overline{CS}$, A0, and $\overline{HOLD}$ are taken low simultaneously. See the *Microprocessor Interface* section on page 14 to eliminate the possibility of inadvertent software reset. The $\overline{EOC}$ output remains high throughout the reset operation and will fall upon its completion. It can thus be used to generate an interrupt indicating the CS5012 is ready for operation. Six master clock cycles plus 2.25µs (1.32µs for the -7 version only) must be allowed after $\overline{EOC}$ falls to allow for acquisition. Under microprocessor-independent operation with 3-states permanently enabled ($\overline{CS}$, $\overline{RD}$ low; A0 high) the $\overline{EOC}$ output will not fall at the completion of the reset operation.

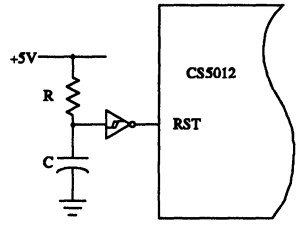


Figure 6. Power-On Reset Circuitry

Initiating Calibration

All modes of calibration can be controlled in hardware or software. Accuracy can thereby be insured at any time or temperature throughout operating life. After initial calibration at power-up, the CS5012's charge-redistribution design yields better temperature drift and more graceful aging than resistor-based technologies, so calibration is actually required less often than with traditional devices.

The first mode of calibration, reset, results in a single full calibration cycle. The second type of calibration, termed "burst" cal, is useful when the ADC sees some downtime but not enough to perform a full reset calibration. Burst cal can be terminated mid-calibration; it picks up where it left off previously, so calibrations can be done in piecemeal fashion. Burst cal is initiated by bringing the CAL input high with $\overline{CS}$ low. The CAL input is level-triggered and latches on the rising

6

edge of $\overline{CS}$, so a write cycle can be used to control calibration in software. Burst cal will continue to loop through calibration cycles until terminated. Once CAL returns low, at least 26 master clock cycles plus 2.25µs (1.32µs for the -7 version) must be allowed before a conversion is initiated to ensure the CS5012 has completed its calibration experiment and has acquired the analog input. The $\overline{EOC}$ output indicates the completion of the final calibration experiment. (See note on page 29.)

The CS5012 features a background calibration mode called "interleave." Interleave appends a single calibration experiment to each conversion cycle and thus requires no dead time for calibration. The CS5012 gathers data between conversions and will adjust its transfer function once it completes the entire sequence of experiments (one calibration cycle per 72,192 conversions). Initiated by bringing both the $\overline{INTRLV}$ input and $\overline{CS}$ low (or hard-wiring $\overline{INTRLV}$ low), interleave extends the CS5012's effective conversion time by 20 master clock cycles (5µs @ 4MHz). Other than reduced throughput, interleave is totally transparent to the user.

Burst calibrations initiated at CAL pick up where interleave left off, so calibration cycles can be hastened by "bursting" a number of experiments whenever the CS5012 sees free time. Interleave is subordinate to burst calibrations, so $\overline{INTRLV}$ could still be externally tied low.

Microprocessor Interface

The CS5012 features an intelligent microprocessor interface which offers detailed status information and allows software control of the self-calibration functions. Output data is available in either 8-bit or 16-bit formats for easy interfacing to industry-standard microprocessors.

Strobing both $\overline{CS}$ and $\overline{RD}$ low enables the CS5012's 3-state output buffers with either output data or status information depending on the status of A0. An address bit can be connected to A0 as shown in Figure 4b thereby memory mapping the status register and output data. Conversion status can be polled in software by reading the status register ($\overline{CS}$ and $\overline{RD}$ strobed low with A0 low), and masking status bits S0-S5 and S7 (by logically AND'ing the status word with 01000000) to determine the value of S6. Similarly, the software routine can determine calibration status using other status bits (see Table 2). *Care must be taken not to read the status register (A0 low) while $\overline{HOLD}$ is low, or a software reset will result* (see *Reset*, page 13).

Alternatively, the End-of-Convert ($\overline{EOC}$) output can be used to generate an interrupt or drive a DMA controller to dump the output directly into memory after each conversion. The $\overline{EOC}$ pin

PIN	STATUS BIT	STATUS	DEFINITION
D0	S0	$\overline{END\ OF\ CONVERSION}$	Falls upon completion of a conversion, and returns high on the first subsequent read.
D1	S1	RESERVED	Reserved for factory use.
D2	S2	LOW BYTE/$\overline{HIGH\ BYTE}$	When data is to be read in an 8-bit format (BW=0), indicates which byte will appear at the output next.
D3	S3	$\overline{END\ OF\ TRACK}$	When low, indicates the input has been acquired to the devices specified accuracy.
D4	S4	RESERVED	Reserved for factory use.
D5	S5	TRACKING	High when the device is tracking the intput.
D6	S6	CONVERTING	High when the device is converting the held input.
D7	S7	CALIBRATING	High when the device is calibrating.

Table 2. Status Bit Definitions

falls as each conversion cycle is completed and data is valid at the output. It returns high within four master clock cycles of the first subsequent data read operation or after the start of a new conversion cycle.

To interface with a 16-bit data bus, the BW input to the CS5012 should be held high and all 12 data bits read in parallel on pins D15-D4. With an 8-bit bus, the converter's 12-bit result must be read in two portions. In this instance, BW should be held low and the 8 MSB's obtained on the first read cycle following a conversion. The second read cycle will yield the 4 LSB's with four trailing zeroes. Both bytes appear on pins D0-D7. The upper/lower bytes of the same data will continue to toggle on subsequent reads until the next conversion finishes. Status bit S2 indicates which byte will appear on the next data read operation.

The CS5012 internally buffers its output data, so data can be read while the device is tracking or converting the next sample. Therefore, retrieving the converter's digital output requires no reduction in ADC throughput. Enabling the 3-state outputs while the CS5012 is converting will not introduce conversion errors. When TTL loads are utilized the potential for crosstalk between digital and analog sections of the system is increased. This crosstalk is due to high digital supply and signal currents arising from the TTL drive current required of each digital output. Connecting CMOS logic to the digital outputs is recommended. Suitable logic families include 4000B, 74HC, 74AC, 74ACT, and 74HCT.

The two calibration control inputs, CAL and $\overline{\text{INTRLV}}$, are level-triggered and latched on the rising edge of $\overline{\text{CS}}$. Calibration can be placed under software control by connecting address lines to the CAL and $\overline{\text{INTRLV}}$ inputs as shown in Figure 4a. Any read or write cycle to the CS5012's base address will thereby initiate or terminate calibration.

Microprocessor Independent Operation

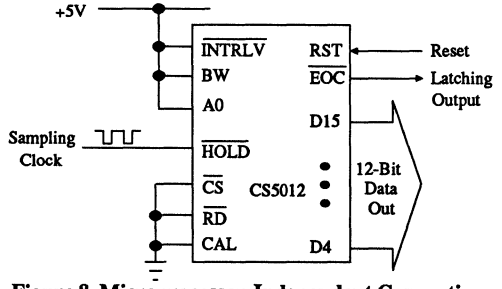


Figure 8. Microprocessor-Independent Connections

The CS5012 can be operated in a stand-alone mode independent of intelligent control. In this mode, $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are hard-wired low permanently enabling the 3-state output buffers. A free-running condition is established when BW is tied high, CAL is tied low, and $\overline{\text{HOLD}}$ is continually strobed low or tied to $\overline{\text{EOT}}$. The CS5012's $\overline{\text{EOC}}$ output can be used to externally latch the output data if desired. With $\overline{\text{CS}}$ and $\overline{\text{RD}}$ hard-wired low, $\overline{\text{EOC}}$ will strobe low for four master clock cycles after each conversion. Data will be unstable up to 100ns after $\overline{\text{EOC}}$ falls, so it should be latched on the rising edge of $\overline{\text{EOC}}$.

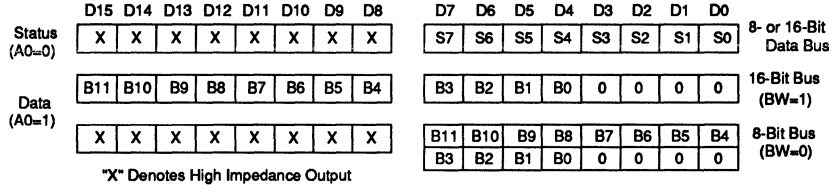


Figure 7. Data Format

Serial Output

All successive-approximation A/D converters derive their digital output serially starting with the MSB. The CS5012 presents each bit to the SDATA pin four master clock cycles after it is derived and can be latched using the serial clock output, SCLK. Just subsequent to each bit decision SCLK will fall and return high once the bit information on SDATA has stabilized. Thus, the rising edge of the SCLK output should be used to clock the data from the CS5012 (See Figure 9).

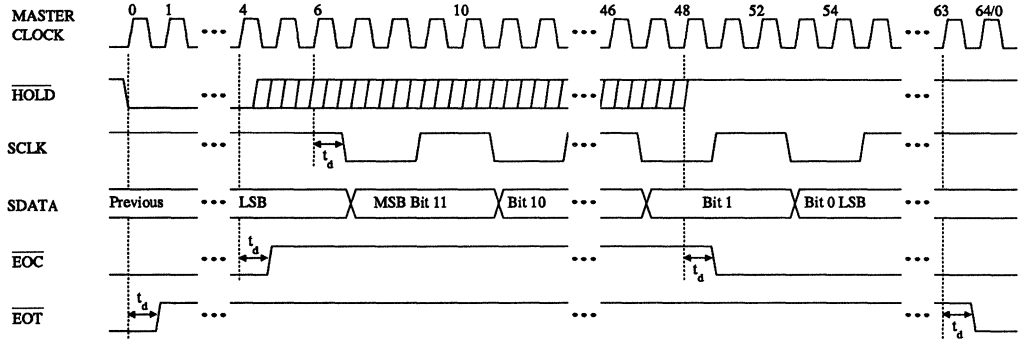
ANALOG CIRCUIT CONNECTIONS

Most popular successive-approximation A/D converters generate dynamic loads at their analog connections. The CS5012 internally buffers all analog inputs (AIN, VREF, and AGND) to ease the demands placed on external circuitry. However, accurate system operation still requires careful attention to details at the design stage regarding source impedances as well as grounding and decoupling schemes.

Reference Considerations

An application note titled "*Voltage References for the CS501X/CSZ511X Series of A/D Converters*" is available for the CS5012. In addition to working through a reference circuit design example, it offers seven built-and-tested reference circuits.

During conversion, each capacitor of the calibrated capacitor array is switched between VREF and AGND in a manner determined by the successive-approximation algorithm. The charging and discharging of the array results in a current load at the reference. The CS5012 includes an internal buffer amplifier to minimize the external reference circuit's drive requirement and preserve the reference's integrity. Whenever the array is switched during conversion, the buffer is used to pre-charge the array thereby providing the bulk of the necessary charge. The appropriate array capacitors are then switched to the unbuffered VREF pin to avoid any errors due to offsets and/or noise in the buffer.



notes: 1. t_d can vary from 135ns - 235ns over military temperature range and over ± 10% supply variation.
2. For asynchronous mode, transitions of SCLK, SDATA, $\overline{EOC}$, $\overline{EOT}$ can shift by up to 4 clocks; e.g. the first high to low transition of SLCK may be on clock #6 to #9. The timing relationship between SLCK, SDATA, $\overline{EOC}$, and $\overline{EOT}$ is fixed.

Figure 9. Serial Output Timing

The external reference circuitry need only provide the residual charge required to fully charge the array after pre-charging from the buffer. This creates an ac current load as the CS5012 sequences through conversions. The reference circuitry must have a low enough output impedance to drive the requisite current without changing its output voltage significantly. As the analog input signal varies, the switching sequence of the internal capacitor array changes. The current load on the external reference circuitry thus varies in response with the analog input. Therefore, the external reference must not exhibit significant peaking in its output impedance characteristic at signal frequencies or their harmonics.

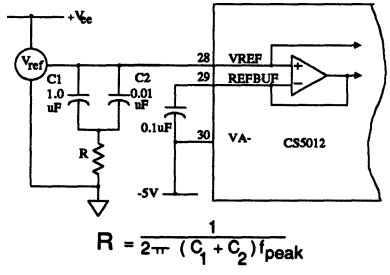


Figure 10. Reference Connections

A large capacitor connected between VREF and AGND can provide sufficiently low output impedance at the high end of the frequency spectrum, while almost all precision references exhibit extremely low output impedance at dc. The presence of large capacitors on the output of some voltage references, however, may cause peaking in the output impedance at intermediate frequencies. Care should be exercised to ensure that significant peaking does not exist or that some form of compensation is provided to eliminate the effect.

The magnitude of the current load on the external reference circuitry will scale to the master clock frequency. With a 4MHz clock, the reference must supply a maximum load current of 10µA peak-to-peak (1µA typical). An output impedance of 15Ω will therefore yield a maximum error of 150µV. With a 2.5V reference and LSB size of 0.6mV, this would insure better than 1/4 LSB accuracy. A 1µF capacitor exhibits an impedance of less than 15Ω at frequencies greater than 10kHz. A high-quality tantalum capacitor in parallel with a smaller ceramic capacitor is recommended.

Peaking in the reference's output impedance can occur because of capacitive loading at its output. Any peaking that might occur can be reduced by placing a small resistor in series with the capacitors (Figure 10). The equation in Figure 10 can be used to help calculate the optimum value of R for a particular reference. The term "f_{peak}" is the frequency of the peak in the output impedance of the reference before the resistor is added.

The CS5012 can operate with a wide range of reference voltages, but signal-to-noise performance is maximized by using as wide a signal range as possible. The recommended reference voltage is between 2.5 and 4.5 volts. The CS5012 can actually accept reference voltages up to the positive analog supply. However, the buffer's offset may increase as the reference voltage approaches VA+ thereby increasing external drive requirements at VREF. A 4.5V reference is the maximum reference voltage recommended. This allows 0.5V headroom for the internal reference buffer. Also, the buffer enlists the aid of an external 0.1µF ceramic capacitor which must be tied between its output, REFBUF, and the negative analog supply, VA-. For more information on references, consult "Application Note: *Voltage References for the CS501X/CSZ511X Series of A/D Converters*".

Analog Input Connection

The analog input terminal functions similarly to the VREF input after each conversion when

switching into the track mode. During the first six master clock cycles in the track mode, the buffered version of the analog input is used for pre-charging the capacitor array. An additional period is required for fine-charging directly from AIN to obtain the specified accuracy. Figure 11 exemplifies this operation. During pre-charge the charge on the capacitor array first settles to the buffered version of the analog input. This voltage is offset from the actual input voltage. During fine-charge, the charge then settles to the accurate unbuffered version.

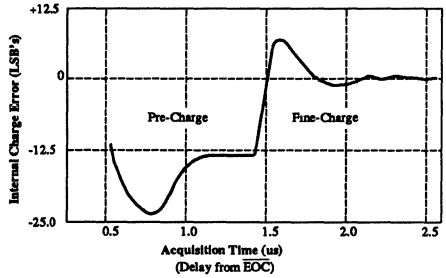


Figure 11. Internal Acquisition Time

The acquisition time of the CS5012 depends on the master clock frequency. This is due to a fixed pre-charge period. For instance, operating the -12 version with an external 4MHz master clock results in a 3.75µs acquisition time: 1.5µs for pre-charging (6 clock cycles) and 2.25µs for fine-charging. Fine-charge settling is specified as a maximum of 2.25µs for an analog source impedance of less than 200Ω. (On the -7 version it is specified as 1.32µs.) In addition, the comparator requires a source impedance of less than 400Ω around 2MHz for stability, which is met by practically all bipolar op amps. Large dc source impedances can be accommodated by adding capacitance from AIN to ground (typically 200pF) to decrease source impedance at high frequencies. However, high dc source resistances will increase the input's RC time constant and extend the necessary acquisition time.

The CS5012 can track full power signals up to 32kHz in the track mode. During the first six clock cycles following a conversion (pre-charge), the CS5012 is capable of slewing at 5V/µs in unipolar mode. In bipolar mode, only half the capacitor array is connected to the analog input so the CS5012 can slew at 10V/µs. After the first six master clock cycles, it will slew at 0.25V/µs in the unipolar mode and 0.5V/µs in bipolar mode. Acquisition of fast slewing signals (step functions) can be hastened if the step occurs during or immediately following the conversion cycle. For instance, channel selection in multiplexed applications should occur while the CS5012 is converting (see Figure 12). Multiplexer settling is thereby

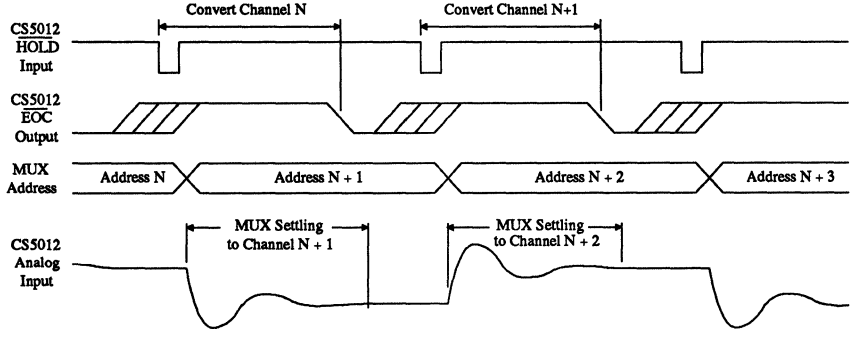


Figure 12.Pipelined MUX Input Channels

removed from the overall throughput equation, and the CS5012 can convert at full speed.

Analog Input Range/Coding Format

The reference voltage directly defines the input voltage range in both the unipolar and bipolar configurations. In the unipolar configuration (BP/$\overline{UP}$ low), the first code transition occurs 0.5 LSB above AGND, and the final code transition occurs 1.5 LSB's below VREF. Coding is in straight binary format. In the bipolar configuration (BP/$\overline{UP}$ high), the first code transition occurs 0.5 LSB above -VREF and the last transition occurs 1.5 LSB's below +VREF. Coding is in an offset-binary format. Positive full scale gives a digital output of 111111111111, and negative full scale gives a digital output of 000000000000.

Grounding and Power Supply Decoupling

The CS5012 uses the analog ground connection, AGND, only as a reference voltage. No dc power currents flow through the AGND connection, and it is completely independent of DGND. However, any noise riding on the AGND input relative to the system's analog ground will induce conversion errors. Therefore, both the analog input and reference voltage should be referred to the AGND pin, which should be used as the entire system's analog ground.

The digital and analog supplies are isolated within the CS5012 and are pinned out separately to minimize coupling between the analog and digital sections of the chip. All four supplies should be decoupled to their respective grounds using 0.1µF ceramic capacitors. If significant low-frequency noise is present on the supplies, 1µF tantalum capacitors are recommended in parallel with the 0.1µF capacitors.

The positive digital power supply of the CS5012 must never exceed the positive analog supply by more than a diode drop or the CS5012 could experience permanent damage. If the two supplies are derived from separate sources, care must be taken that the analog supply comes up first at power-up. The system connection diagram on page 23 shows a decoupling scheme which allows the CS5012 to be powered from a single set of ±5V rails. The positive digital supply is derived from the analog supply through a 10Ω resistor to avoid the analog supply dropping below the digital supply. If this scheme is utilized, care must be taken to insure that any digital load currents (which flow through the 10Ω resistors) do not cause the magnitude of digital supplies to drop below the analog supplies by more than 0.5 volts. Digital supplies must always remain above the minimum specification.

As with any high-precision A/D converter, the CS5012 requires careful attention to grounding and layout arrangements. However, no unique layout issues must be addressed to properly apply the CS5012. The CDB5012 evaluation board is available for the CS5012, which avoids the need to design, build, and debug a high-precision PC board to initially characterize the part. The board comes with a socketed CS5012, and can be quickly reconfigured to simulate any combination of sampling, calibration, master clock, and analog input range conditions.

6

CS5012 PERFORMANCE

Differential Nonlinearity

The most prevalent source of nonlinearity in high resolution converters is bit weight errors. These errors arise from the deviation of bits from their ideal binary-weighted ratios, and lead to nonideal widths for each code. If DNL errors are large, and code widths shrink to zero, it is possible for one or more codes to be entirely missing. The CS5012 calibrates all bits in the capacitor array to a small fraction of an LSB resulting in nearly ideal DNL. A histogram plot of typical DNL can be seen in Figure 13.

A histogram test is a statistical method of deriving an A/D converter's differential nonlinearity. A ramp is input to the A/D and a large number of samples are taken to insure a high confidence level in the test's result. The number of occurrences for each code is monitored and stored. A perfect A/D converter would have all codes of equal size and therefore equal numbers of occurrences. In the histogram test a code with the average number of occurrences will be considered ideal (DNL = 0). A code with more or less occurrences than average will appear as a DNL of greater or less than zero LSB. A missing code has zero occurrences, and will appear as a DNL of -1 LSB.

Integral Nonlinearity

Integral nonlinearity is defined as the deviation of the transfer function from an ideal straight line through zero and full scale. Even if differential linearity errors are small, they may combine to produce a gross INL error at some point in the transfer function. A unique calibration algorithm, a lack of superposition of errors due to a capacitor based DAC, and low capacitor voltage coefficient keep INL errors below ±1/2 LSB.

Clock Feedthrough

Maintaining the integrity of analog signals in the presence of digital switching noise is a difficult problem. The CS5012 can be synchronized to the digital system using the CLKIN input to avoid conversion errors due to asynchronous interference. However, digital interference will still affect sampling purity due to coupling between the CS5012's analog input and master clock.

The effect of clock feedthrough depends on the sampling conditions. If the sampling signal at the $\overline{\text{HOLD}}$ input is synchronized to the master clock, clock feedthrough will appear as a dc offset at the CS5012's output. The offset could theoretically reach the peak coupling magnitude (Figure 14), but the probability of this occurring is small since the peaks are spikes of short duration.

Master Clock		Analog Input	Clock Feedthrough	
Int/Ext	Freq	Source Impedance	RMS	Peak-to-Peak
Internal	2MHz	50 Ω	15uV	70uV
External	2MHz	50 Ω	25uV	110uV
External	4MHz	50 Ω	40uV	150uV
External	4MHz	25 Ω	25uV	110uV
External	4MHz	200 Ω	80uV	325uV

Figure 14. Examples of Measured Clock Feedthrough

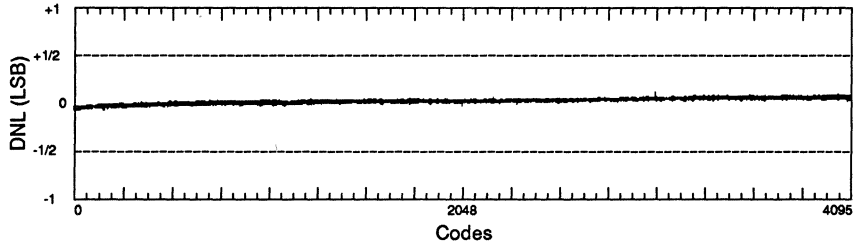


Figure 13. CS5012 Differential Nonlinearity Plot

If sampling is performed asynchronously with the master clock, clock feedthrough will appear as an ac error at the CS5012's output. With a fixed sampling rate, a tone will appear as the clock frequency aliases into the baseband. The tone frequency can be calculated using the equation below and could be selectively filtered in software using DSP techniques.

$$f_{tone} = (Nf_s - f_{clk})$$

where $N = f_{clk}/f_s$ rounded to the nearest integer

The magnitude of clock feedthrough depends on the master clock conditions and the source impedance applied to the analog input. When operating with the CS5012's internally generated clock, the CLKIN input is grounded and the dominant source of coupling is through the device's substrate. As shown in Figure 14, a typical CS5012 operating with its internal oscillator at 2MHz and 50Ω of analog input source impedance wil exhibit only 15μV rms of clock feedthrough. However, if a 2MHz external clock is applied to CLKIN under the same conditions, feedthrough increases to 25μV rms. Feedthrough also increases with clock frequency; a 4MHz clock yields 40μV rms.

Clock feedthrough can be reduced by limiting the source impedance applied at the analog input. As shown in Figure 14, reducing source impedance from 50Ω to 25Ω yields a 15μV rms reduction in feedthrough. Therefore, when operating the CS5012 with high-frequency external master clocks, it is important to minimize source impedance applied to the CS5012's input.

Also, the overall effect of clock feedthrough can be minimized by maximizing the input range and LSB size. The reference voltage applied to VREF can be maximized, and the CS5012 can be operated in bipolar mode which inherently doubles the LSB size over the unipolar mode.

Power Supply Rejection

The CS5012's power supply rejection performance is enhanced by the on-chip self-calibration and an "auto-zero" process. Drifts in power supply voltages at frequencies less than the calibration rate have negligible effect on the CS5012's accuracy. This, of course, is because the CS5012 adjusts its offset to within a small fraction of an LSB during calibration.

Above the calibration frequency the excellent power supply rejection of the internal amplifiers is augmented by an auto-zero process. Any offsets are stored on the capacitor array and are effectively subtracted once conversion is initiated. Figure 15 shows power supply rejection of the CS5012 in the bipolar mode with the analog input grounded and a 300mV p-p ripple applied to each supply. Power supply rejection improves by 6dB in the unipolar mode.

Notches of increased rejection arise from the auto-zeroing at the conversion rate. The frequencies at which these notches occur also depend on the value of the captured analog input. The line shows worst-case rejection for all combinations of conversion rates and input conditions in the bipolar mode. Again, power supply rejection is 6dB better in the unipolar mode.

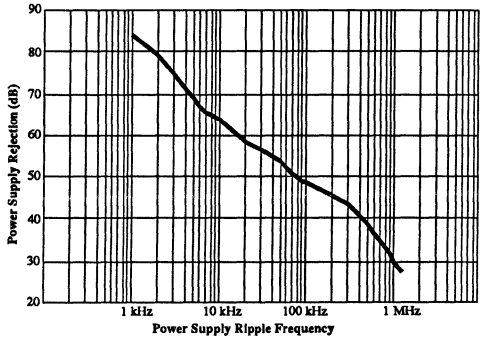


Figure 15. Power Supply Rejection

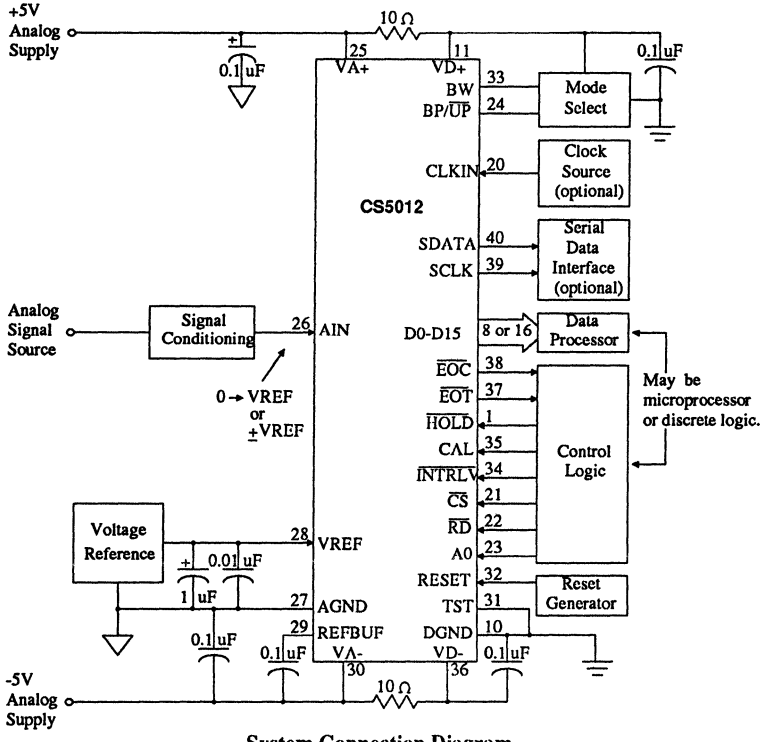
Aperture Jitter

Track-and-hold amplifiers commonly exhibit two types of aperture jitter. The first, more appropriately termed "aperture window", is an input voltage dependent variation in the aperture delay. Its signal-dependency causes distortion at high frequencies. The CS5012's proprietary architecture avoids applying the input voltage across a sampling switch, thus avoiding any "aperture window" effects. The second type of aperture jitter, due to component noise, assumes a random nature. With only 100ps peak-to-peak aperture jitter, the CS5012 can process full-scale signals up to 1/2 the throughput frequency without any errors due to aperture jitter.

$\overline{HOLD}$	$\overline{CS}$	CAL	$\overline{INTRLV}$	$\overline{RD}$	A0	RST	Function
↓	X	X	X	X	*	0	Hold and Start Convert
X	0	1	X	X	*	0	Initiate Burst Calibration
1	0	0	X	X	*	0	Stop Burst Cal and Begin Track
X	0	X	0	X	*	0	Initiate Interleave Calibration
X	0	X	1	X	*	0	Terminate Interleave Cal
X	0	X	X	0	1	0	Read Output Data
1	0	X	X	0	0	0	Read Status Register
X	1	X	X	X	*	X	High Impedance Data Bus
X	X	X	X	1	*	X	High Impedance Data Bus
X	X	X	X	X	X	1	Reset
0	0	X	X	X	0	X	Reset

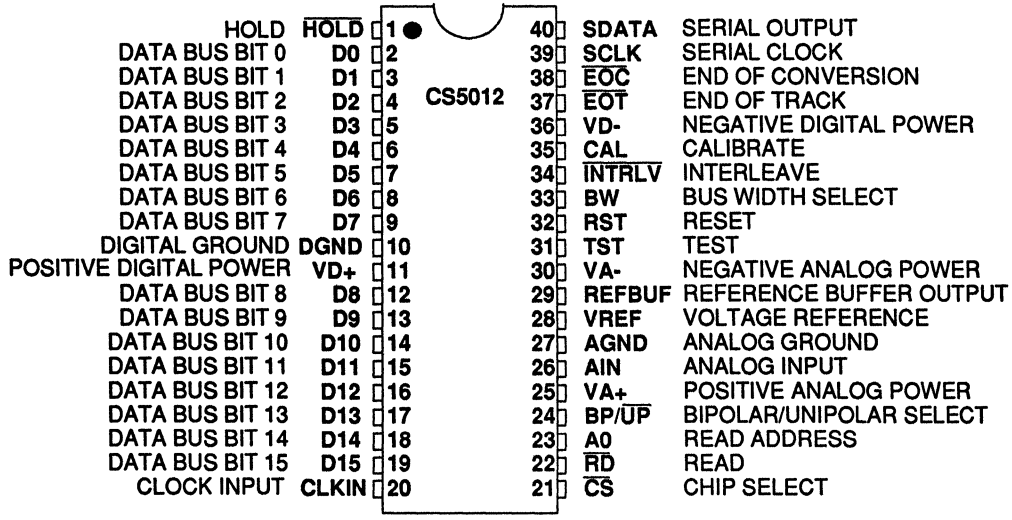
* The status of A0 is not critical to the operation specified. However, A0 should not be low with $\overline{CS}$ and $\overline{HOLD}$ low, or a software reset will result.

CS5012 Truth Table



System Connection Diagram

PIN DESCRIPTIONS



Power Supply Connections

VD+ - Positive Digital Power, PIN 11.
Positive digital power supply. Nominally +5 volts.

VD- - Negative Digital Power, PIN 36.
Negative digital power supply. Nominally -5 volts.

DGND - Digital Ground, PIN 10.
Digital ground reference.

VA+ - Positive Analog Power, PIN 25.
Positive analog power supply. Nominally +5 volts.

VA- - Negative Analog Power, PIN 30.
Negative analog power supply. Nominally -5 volts.

AGND - Analog Ground, PIN 27.
Analog ground reference.

Oscillator

CLKIN - Clock Input, PIN 20.

All conversions and calibrations are timed from a master clock which can either be supplied by driving this pin with an external clock signal, or can be internally generated by tying this pin to DGND.

Digital Inputs

$\overline{\text{HOLD}}$ - Hold, PIN 1.

A falling transition on this pin sets the CS5012 to the hold state and initiates a conversion. This input must remain low at least one master clock cycle plus 50ns.

$\overline{\text{CS}}$ - Chip Select, PIN 21.

When high, the data bus outputs are held in a high impedance state and the input to CAL and $\overline{\text{INTRLV}}$ are ignored. A falling transition initiates or terminates burst or interleave calibration (depending on the status of CAL and $\overline{\text{INTRLV}}$) and a rising transition latches both the CAL and $\overline{\text{INTRLV}}$ inputs. If $\overline{\text{RD}}$ is low, the data bus is driven as indicated by BW and A0.

$\overline{\text{RD}}$ - Read, PIN 22.

When $\overline{\text{RD}}$ and $\overline{\text{CS}}$ are both low, data is driven onto the data bus. If either signal is high, the data bus outputs are held in a high impedance state. The data driven onto the bus is determined by BW and A0.

A0 - Read Address, PIN 23.

Determines whether data or status information is placed onto the data bus. When high during the read operation, converted data is placed onto the data bus; when low, the status register is driven onto the bus.

BP/$\overline{\text{UP}}$ - Bipolar/Unipolar Input Select, PIN 24.

When high, the device is configured with a bipolar transfer function ranging from -VREF to +VREF. Encoding is in an offset binary format, with the mid-scale code 100...0000 centered at AGND. When low, the device is configured for a unipolar transfer function from AGND to VREF. Unipolar encoding is in straight binary format.

RST - Reset, PIN 32.

When taken high, all internal digital logic is reset. Upon being taken low, a full calibration sequence is initiated.

BW - Bus Width Select, PIN 33.

When hard-wired high, all 12 data bits are driven onto the bus simultaneously during a data read cycle. When low, the bus is in a byte wide format. On the first read following a conversion, the eight MSB's are driven onto D7-D0. A second read cycle places the four LSB's with four trailing zeroes on D7-D0. Subsequent reads will toggle the higher/lower order byte. Regardless of BW's status, a read cycle with A0 low yields the status information on D7-D0.

$\overline{\text{INTRLV}}$ - Interleave, PIN 34.

When latched low using $\overline{\text{CS}}$, the device goes into interleave calibration mode. A full calibration will complete every 79,192 conversions. The effective conversion time extends by 20 clock cycles.

CAL - Calibrate, PIN 35. (See note on page 29.)

When latched high using $\overline{\text{CS}}$, burst calibration results. The device cannot perform conversions during the calibration period which will terminate only once CAL is latched low again. Calibration picks up where the previous calibration left off, and calibration cycles complete every 1,443,840 master clock cycles. If the device is converting when a calibration is signaled, it will wait until that conversion completes before beginning.

Analog Inputs

AIN - Analog Input, PIN 26.

Input range in unipolar mode is zero volts to VREF. Input range in bipolar mode is -VREF to +VREF. The output impedance of buffer driving this input should be less than or equal to 200Ω.

VREF - Voltage Reference, PIN 28.

The analog reference voltage which sets the analog input range. It represents positive full scale for both bipolar and unipolar operation, and its magnitude sets negative full scale in bipolar mode. The allowable range for VREF is 2.5V to 4.5V.

Digital Outputs

D0 through D15 - Data Bus Outputs, PINS 2 thru 9, 12 thru 19.

3-state output pins. Enabled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$, they offer the converter's 12-bit output in a format consistent with the state of BW if A0 is high. If A0 is low, bits D0-D7 offer status register.

$\overline{\text{EOT}}$ - End Of Track, PIN 37.

If low, indicates that enough time has elapsed since the last conversion for the device to acquire the analog input signal (3.75µs for 4MHz external clock).

$\overline{EOC}$ - End Of Conversion, PIN 38.

This output indicates the end of a conversion or calibration cycle. It is high during a conversion and will fall to a low state upon completion of the conversion cycle indicating valid data is available at the output. Returns high on the first subsequent read or the start of a new conversion cycle.

SDATA - Serial Output, PIN 40.

Presents each output data bit after it is determined by the successive approximation algorithm. Valid on the rising edge of SCLK, data appears MSB first, LSB last, and each bit remains valid until the next bit appears.

SCLK - Serial Clock Output, PIN 39.

Used to clock converted output data serially from the CS5012. Serial data is stable on the rising edge of SCLK.

Analog Outputs

REFBUF - Reference Buffer Output, PIN 29.

Reference buffer output. A 0.1µF ceramic capacitor must be tied between this pin and VA-.

6

Miscellaneous

TST - Test, PIN 31.

Allows access to the CS5012's test functions which are reserved for factory use. Must be tied to DGND.

ERROR DEFINITIONS

Linearity Error - The deviation of a code from a straight line passing through the endpoints of the transfer function after zero- and full-scale errors have been externally calibrated. "Zero-scale" is a point 1/2 LSB below the first code transition and "full-scale" is a point 1/2 LSB beyond the code transition to all ones. The deviation is measured from the middle of each particular code. Units in LSB's.

Differential Linearity - The deviation of a code's width from the ideal width. Units in LSB's.

Full Scale Error - The deviation of the last code transition from the ideal (VREF-3/2 LSB's) after all offsets have been accounted for. Units in LSB's.

Unipolar Offset - The deviation of the first code transition from the ideal (1/2 LSB above AGND) when in unipolar mode (BP/$\overline{UP}$ low). Units in LSB's.

Bipolar Offset - The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below AGND) when in bipolar mode (BP/$\overline{UP}$ high). Units in LSB's.

Bipolar Negative Full-scale Error - The deviation of the first code transition from the ideal when in bipolar mode (BP/$\overline{UP}$ high). The ideal is defined as lying on a straight line which passes through the final and mid-scale code transitions. Units in LSB's.

Total Unadjusted Error - The worst-case combination of offset error, full-scale error, and linearity error. Units in LSB's.

Aperture Time - The time required after the hold command for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

Aperture Jitter - The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

Note: Temperatures specified define ambient conditions in free-air during test and do not refer to the junction temperature of the device.

Ordering Guide

Model	Conversion Time	Temp. Range	Package
CS5012-KP24	24.50 µs	0 to +70 °C	40-Pin Plastic DIP
CS5012-KP12	12.25 µs	0 to +70 °C	40-Pin Plastic DIP
CS5012-KP7	7.20 µs	0 to +70 °C	40-Pin Plastic DIP
CS5012-BC24	24.50 µs	-40 to +85 °C	40-Pin Ceramic Side-Brazed DIP
CS5012-BC12	12.25 µs	-40 to +85 °C	40-Pin Ceramic Side-Brazed DIP
CS5012-BC7	7.20 µs	-40 to +85 °C	40-Pin Ceramic Side-Brazed DIP
CS5012-TC24	24.50 µs	-55 to +125 °C	40-Pin Ceramic Side-Brazed DIP
CS5012-TC12	12.25 µs	-55 to +125 °C	40-Pin Ceramic Side-Brazed DIP

ADDENDUM

Burst Calibration

Burst calibration mode allows control of partial calibration cycles. Due to an unforeseen condition inside the part, asynchronous termination of calibration (CAL brought low) may result in a sub-optimal calibration result. It is recommended that burst calibration is not used, until the silicon is revised to prevent this effect.

The reset and interleave mode work perfectly, and should be used instead of burst mode. The CS5012's very low drift over temperature means that, under most circumstances, calibration need only be performed at power-up, using reset (See *Analog Characteristics* table on the second page of this data sheet).

If you wish to use burst calibration, then please contact the factory for advice and new part availability information.

• Notes •

Semiconductor Corporation

CS5014

14-Bit, 14us Self-Calibrating A/D Converter

Features

- Monolithic CMOS A/D Converter
  - Microprocessor Compatible
  - Parallel and Serial Output
  - Inherent Track/Hold Input
- True 14-Bit Precision
  - Linearity Error: ± 1/4 LSB
  - Total Unadjusted Error: ± 1 LSB
  - No Missing Codes
- 14.25 Microsecond Conversion Time
  - Throughput Rates up to 56kHz
- Self Calibration Maintains Accuracy Over Time and Temperature
- Low Power Dissipation: 120mW
- Pin Compatible with CS5012/CS5016

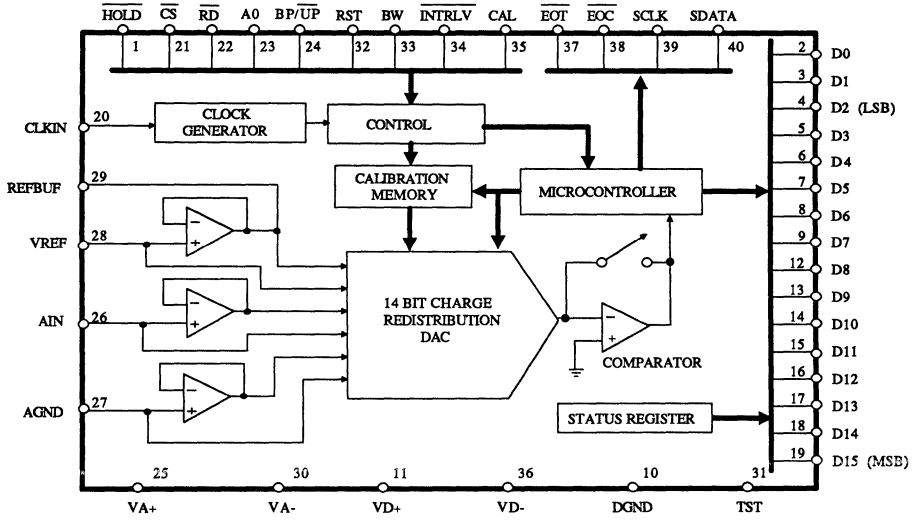
General Description

The CS5014 is a 14-bit monolithic CMOS analog to digital converter with 14.25 microsecond conversion time. Unique self-calibration circuitry, which can be under intelligent control, insures maximum nonlinearity of 1/2 LSB and no missing codes. Offset and full scale errors are kept within 1/2 LSB, eliminating the need for manual calibration of any kind. Unipolar and bipolar input ranges are digitally selectable.

The CS5014 consists of a DAC, conversion and calibration microcontroller, oscillator, comparator, microprocessor compatible 3-State I/O, and calibration circuitry. The input track-and-hold, inherent to the device's sampling architecture, acquires the analog input signal after each conversion within 3.75us to 0.003%, allowing throughput rates up to 56kHz.

The CS5014 is pin compatible with the CS5012 and CS5016 A/D converters allowing system upgrading and downgrading without hardware alterations.

ORDERING INFORMATION: Page 57



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, Texas 78760
(512)445-7222 TWX:910-874-1352

ANALOG CHARACTERISTICS (T_A = 25°C; VA+,VD+ = 5V; VA-,VD- = -5V; VREF = 4.5V; f_{clk} = 4MHz for -14, 2MHz for -28; Analog Source Impedance = 200 Ω unless otherwise specified)

Parameter *	CS5014-K min	CS5014-K typ	CS5014-K max	CS5014-B min	CS5014-B typ	CS5014-B max	CS5014-T min	CS5014-T typ	CS5014-T max	Units
Specified Temperature Range		0 to +70			-40 to +85			-55 to +125		°C
Accuracy										
Linearity Error										
T_{min} to T_{max} (Note 1)		±1/4	±1/2		±1/4	±1/2		±1/4	±1/2	LSB
Differential Linearity										
T_{min} to T_{max} (Notes 1,2)		±1/4	±1/2		±1/4	±1/2		±1/4	±1/2	LSB
Full Scale Error (Note 1)		±1/2	±1		±1/2	±1		±1/2	±1	LSB
T_{min} to T_{max} (Note 3)		±1/4			±1/4			±1/2		ΔLSB
Unipolar Offset (Note 1)		±1/4	±3/4		±1/4	±3/4		±1/4	±3/4	LSB
T_{min} to T_{max} (Note 3)		±1/4			±1/4			±1/2		ΔLSB
Bipolar Offset (Note 1)		±1/4	±3/4		±1/2	±3/4		±1/2	±3/4	LSB
T_{min} to T_{max} (Note 3)		±1/4			±1/2			±1/2		ΔLSB
Bipolar Negative Full-Scale Error (Note 1)		±1/2	±1		±1/2	±1		±1/2	±1	LSB
T_{min} to T_{max} (Note 3)		±1/4			±1/4			±1/2		ΔLSB
Total Unadjusted Error (Note 1)		±1			±1			±1		LSB
T_{min} to T_{max} (Note 3)		±1/2			±1			±1		ΔLSB
Noise (Note 4) Unipolar Mode		45			45			45		uV_{rms}
Bipolar Mode		90			90			90		uV_{rms}
Analog Input										
Aperture Time		25			25			25		ns
Aperture Jitter		100			100			100		ps
Aperture Time Matching (Note 5)		TBD			TBD			TBD		ns
Full Power Bandwidth (Note 6)		28			28			28		kHz
Input Capacitance (Note 7) Unipolar Mode		275	375		275	375		275	375	pF
Bipolar Mode		165	220		165	220		165	220	pF

Notes:
1. Applies after calibration at any temperature witnin the specified temperature range.
2. No missing codes guaranteed.
3. Total drift over specified temperature range since calibration at power-up at 25°C.
4. Wideband noise aliased into baseband. Referred to input.
5. Part to part.
6. Vin = 9V p-p. Refer to *Analog Input* Section on page 45 for discussion of input slew rate.
7. Applies only in track mode. When converting or calibrating, input capacitance will not exceed 15 pF.

* Refer to *Error Definitions* on page 56.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (continued)

Parameter		CS5014-K min	CS5014-K typ	CS5014-K max	CS5014-B min	CS5014-B typ	CS5014-B max	CS5014-T min	CS5014-T typ	CS5014-T max	Units
Conversion & Throughput											
Conversion Time	−14			14.25			14.25			14.25	us
(Notes 8,9)	−28			28.5			28.5			28.5	us
Acquisition Time	−14		3.0	3.75		3.0	3.75		3.0	3.75	us
(Note 9)	−28		4.5	5.25		4.5	5.25		4.5	5.25	us
Throughput	−14	55.6			55.6			55.6			kHz
(Note 9)	−28	29.6			29.6			29.6			kHz
Power Supplies											
DC Power Supply Currents (Note 10)											
I_{A+}			9	19		9	19		9	19	mA
I_{A-}			−9	−19		−9	−19		−9	19	mA
I_{D+}			3	6		3	6		3	6	mA
I_{D-}			−3	−6		−3	−6		−3	−6	mA
Power Dissipation	(Note 10)		120	250		120	250		120	250	mW
Power Supply Rejection	(Note 11)										
Positive Supplies			84			84			84		dB
Negative Supplies			84			84			84		dB

Notes:
8. Measured from falling transition on $\overline{\text{HOLD}}$ to falling transition on $\overline{\text{EOC}}$.
9. Conversion, acquisition, and throughput times depend on the master clock, sampling and calibration conditions. The numbers shown assume sampling and conversion is synchronized with the CS5014's conversion clock, interleave calibrate is disabled, and operation is from the full-rated external clock. A detailed discussion of conversion timing appears on page 39.
10. All outputs unloaded. All inputs CMOS levels.
11. With 300m p-p, 1kHz ripple applied to each analog supply separately in the bipolar mode. Rejection improves by 6dB in the unipolar mode to 90dB. A plot of typical power supply rejection versus frequency appears on page 49.

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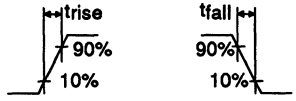
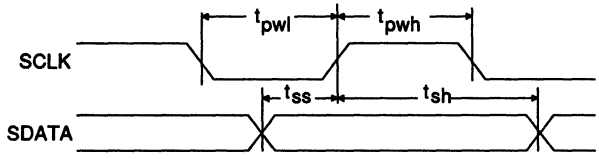
SWITCHING CHARACTERISTICS ($T_A = T_{min}$ to T_{max} ; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ±10%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50pF)

Parameter	Symbol	Min	Typ	Max	Units
Master Clock Frequency:					
Internally Generated: -14	f_{CLK}	2	-	-	MHz
-28		1	-	-	
Externally Supplied: -14		-	-	4	
-28		-	-	2	
Master Clock Duty Cycle	-	30	-	70	%
Rise Times: Any Digital Input	t_{rise}	-	-	1.0	us
Any Digital Output		-	20	-	ns
Fall Times: Any Digital Input	t_{fall}	-	-	1.0	us
Any Digital Output		-	20	-	ns
$\overline{HOLD}$ Pulse Width	t_{hpw}	$1/f_{CLK} + 50$	-	t_c	ns
Conversion Time	t_c	(Note 12)	-	(Note 12)	us
Data Delay Time	t_{dd}	-	40	100	ns
$\overline{EOC}$ Pulse Width (Note 13)	t_{epw}	$4/f_{CLK} - 20$	-	-	ns
Set Up Times: CAL, $\overline{INTRLV}$ to $\overline{CS}$ Low	t_{cs}	20	10	-	ns
A0 to $\overline{CS}$ and $\overline{RD}$ Low	t_{as}	20	10	-	
Hold Times:					
$\overline{CS}$ or $\overline{RD}$ High to A0 Invalid	t_{ah}	50	30	-	ns
$\overline{CS}$ High to CAL, $\overline{INTRLV}$ Invalid	t_{ch}	50	30	-	
Access Times: $\overline{CS}$ Low to Data Valid					
-K, B	t_{ca}	-	90	120	ns
-T		-	115	150	
$\overline{RD}$ Low to Data Valid					
-K, B	t_{ra}	-	90	120	ns
-T		-	115	150	
Output Float Delay: -K, B	t_{fd}	-	50	110	ns
$\overline{CS}$ or $\overline{RD}$ High to Output Hi-Z -T			50	140	
Serial Clock Pulse Width Low	t_{pwl}	-	$2/f_{CLK}$	-	ns
Pulse Width High	t_{pwh}	-	$2/f_{CLK}$	-	
Set Up Times: SDATA to SCLK Rising	t_{ss}	$2/f_{CLK} - 100$	$2/f_{CLK}$	-	ns
Hold Times: SCLK Rising to SDATA	t_{sh}	$2/f_{CLK} - 100$	$2/f_{CLK}$	-	ns

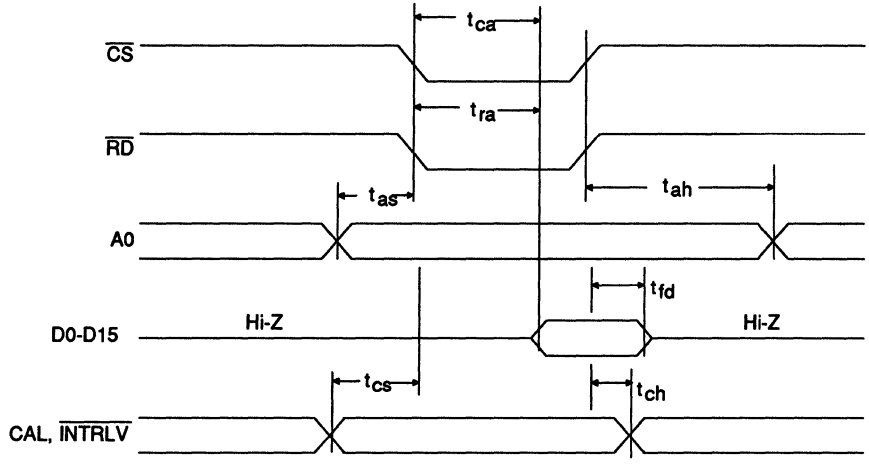
Notes: 12. See Table 1 and master clock frequencies above.
13. $\overline{EOC}$ remains low 4 master clock cycles if $\overline{CS}$ and $\overline{RD}$ are held low. Otherwise, it returns high within four master clock cycles from the start of a data read operation or a conversion cycle.



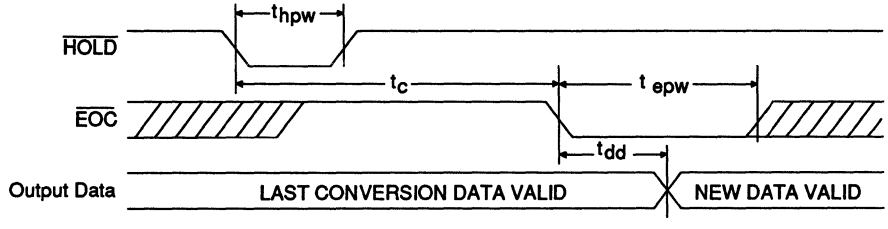
Rise and Fall Times



Serial Output Timing



Read and Calibration Control Timing



Conversion Timing

6

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max} ; VA+, VD+ = 5V ±10%; VA-, VD- = -5V ±10%)

All measurements below are performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 14)	V_{OH}	VD+ - 1.0V	-	-	V
Low-Level Output Voltage Iout=1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	10	uA
3-State Leakage Current	I_{OZ}	-	-	±10	uA
Digital Output Pin Capacitance	C_{out}	-	9	-	pF

Notes: 14. I_{out} = -100µA. This specification guarantees TTL compatibility (VOH=2.4V @ I_{out}=-40µA).

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see Note 15.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.5	5.0	VA+	V
	Negative Digital	VD-	−4.5	−5.0	−5.5	V
	Positive Analog	VA+	4.5	5.0	5.5	V
	Negative Analog	VA-	−4.5	−5.0	−5.5	V
Analog Reference Voltage		VREF	2.5	4.5	VA+ - 0.5	V
Analog Input Voltage:	Unipolar	V_{AIN}	AGND	-	VREF	V
(Note 16)	Bipolar	V_{AIN}	-VREF	-	VREF	V

Notes: 15. All voltages with respect to ground.

16. The CS5014 can accept input voltages up to the analog supplies (VA+ and VA-). It will output all 1's for inputs above VREF and all 0's for inputs below AGND in unipolar mode and -VREF in bipolar mode.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to ground)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	−0.3	VA+ + 0.3	V
	Negative Digital	VD-	0.3	−6.0	V
	Positive Analog	VA+	−0.3	6.0	V
	Negative Analog	VA-	0.3	−6.0	V
Input Current, Any Pin Except Supplies (Note 17)		I_{in}	-	±10	mA
Analog Input Voltage (AIN and VREF pins)		V_{INA}	VA- - 0.3	VA+ + 0.3	V
Digital Input Voltage		V_{IND}	-0.3	VA+ + 0.3	V
Ambient Operating Temperature		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

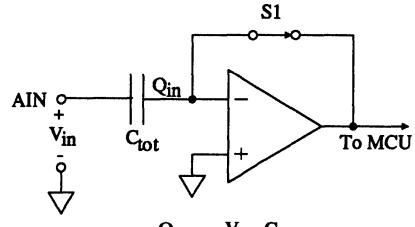
Note: 17. Transient currents of up to 100mA will not cause SCR latch-up.

Warning: Operation at or beyond these limits may result in permanent damages to the device. Normal operation is not guaranteed at these extremes.

THEORY OF OPERATION

The CS5014 utilizes the most popular method of executing high-speed, high-resolution A/D conversion: successive approximation. As with all other iterative comparison methods, the analog input is successively compared to the output of a D/A converter controlled by the conversion algorithm. Successive approximation begins by comparing the analog input to the DAC output which is set to half-scale (MSB on, all other bits off). If the input is found to be below half-scale, the MSB is reset to zero and the input is compared to one-quarter scale (next MSB on, all others off). If the input were above half-scale, the MSB would remain high and the next comparison would be at three-quarters of full scale. This procedure continues until all bits have been exercised.

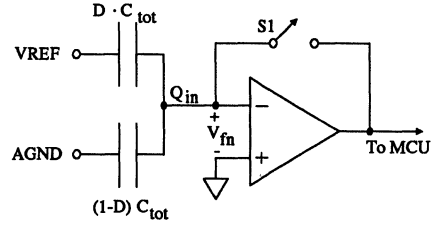
The CS5014 implements the successive-approximation algorithm using a unique charge-redistribution architecture. Instead of the traditional resistor network, the DAC is an array of binary-weighted capacitors. All capacitors in the array share a common node at the comparator's input. Their other terminals are capable of being connected to AIN, AGND, or VREF (Figure 1). When the device is not calibrating or converting, all capacitors are tied to AIN forming C_{tot}. Switch S1 is closed and the charge on the array, Q_{in}, tracks the input signal V_{in} (Figure 2a).



$$-Q_{in} = V_{in}\ C_{tot}$$

Figure 2a. Tracking Mode

When the conversion command is issued, switch S1 opens as shown in Figure 2b. This traps charge Q_{in} on the comparator side of the capacitor array and creates a floating node at the comparator's input. The conversion algorithm operates on this fixed charge, and the signal at the analog input pin is ignored. In effect, the entire DAC capacitor array serves as analog memory during conversion much like a hold capacitor in a sample/hold amplifier.



$$D = \frac{V_{in}}{VREF} \text{ for } V_{fn} = 0V$$

Figure 2b. Convert Mode

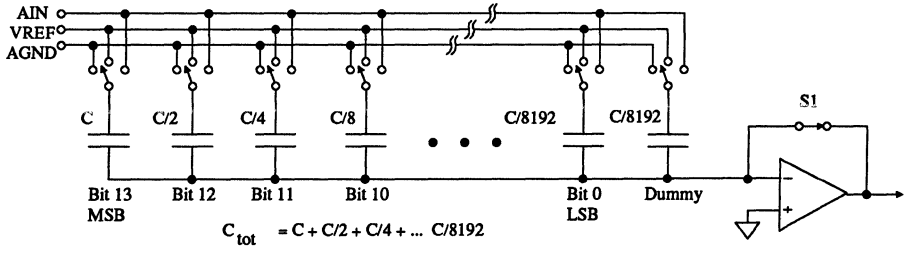


Figure 1. Charge Redistribution DAC

The conversion consists of manipulating the free plates of the capacitor array to VREF and AGND to form a capacitive divider. Since the charge at the floating node remains fixed, the voltage at that point depends on the proportion of capacitance tied to VREF versus AGND. The successive-approximation algorithm is used to find the proportion of capacitance, termed D in Figure 2b, which when connected to the reference will drive the voltage at the floating node (V_{fn}) to zero. That binary fraction of capacitance represents the converter's digital output.

The CS5014's charge redistribution architecture easily supports bipolar input ranges. If half the capacitor array (the MSB capacitor) is tied to VREF rather than AIN in the track mode, the input range is doubled and is offset half-scale. The magnitude of the reference voltage thus defines both positive and negative full-scale (-VREF to +VREF), and the digital code is an offset binary representation of the input.

Calibration

The ability of the CS5014 to convert accurately to 14-bits clearly depends on the accuracy of its comparator and DAC. The CS5014 utilizes an "auto-zeroing" scheme to null errors introduced by the comparator. All offsets are stored on the capacitor array while in the track mode and are effectively subtracted from the input signal when a conversion is initiated. Auto-zeroing enhances power supply rejection at frequencies well below the conversion rate.

To achieve 14-bit accuracy from the DAC, the CS5014 uses a novel self-calibration scheme. Each bit capacitor shown in Figure 1 actually consists of several capacitors which can be manipulated to adjust the overall bit weight. During calibration, an on-chip microcontroller adjusts the sub-arrays to precisely ratio the bits. Each bit is adjusted to just balance the sum of all less significant bits plus one dummy LSB (for example, 16C = 8C + 4C + 2C + C + C). Calibration resolution for the array is a small fraction of an LSB resulting in nearly ideal differential and integral linearity.

DIGITAL CIRCUIT CONNECTIONS

The CS5014 can be applied in a wide variety of master clock, sampling, and calibration conditions which directly affect the device's conversion time and throughput. The device also features on-chip 3-state output buffers and a complete interface for connecting to 8-bit and 16-bit digital systems. Output data is also available in serial format.

Master Clock

The CS5014 operates from a master clock which can be externally supplied or internally generated. The internal oscillator is activated by externally tying the CLKIN input low. Alternatively, the CS5014 can be synchronized to the external system by driving the CLKIN pin with a TTL or CMOS clock signal.

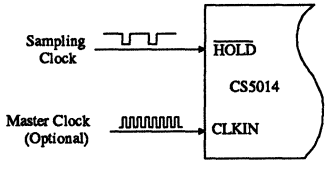


Figure 3a. Asynchronous Sampling

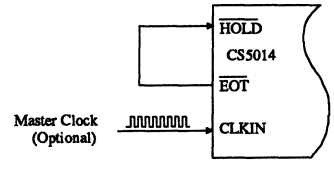


Figure 3b. Synchronous Sampling

All calibration, conversion, and throughput times directly scale to master clock frequency. Thus, throughput can be precisely controlled and/or maximized using an external master clock. In contrast, the CS5014's internal oscillator will vary from unit-to-unit and over temperature. Its tolerance gives rise to minimum and maximum conversion times and throughput rates. The -14 version of the CS5014 is specified for accurate operation with an external clock up to 4MHz; its internal clock frequency is specified at a minimum of 2MHz. The -28 version can handle external clocks up to 2MHz; its internal clock can range as low as 1MHz (see *Switching Characteristics*, page 34). Both versions can typically convert with clocks as low as 10kHz at room temperature.

Initiating Conversions

A falling transition on the $\overline{\text{HOLD}}$ pin places the input in the hold mode and initiates a conversion cycle. The $\overline{\text{HOLD}}$ input is latched internally by the master clock, so it can return high anytime after one master clock cycle plus 50ns. Upon completion of the conversion cycle, the CS5014 automatically returns to the track mode. In contrast to systems with separate track-and-holds and A/D converters, a sampling clock can simply be connected to the $\overline{\text{HOLD}}$ input (Figure 3a). The duty cycle of this clock is not critical. It need only remain low at least one master clock cycle plus 50ns, but no longer than the minimum conversion time or an additional conversion cycle will be initiated with inadequate time for acquisition.

Microprocessor-Controlled Operation

Sampling and conversion can be placed under microprocessor control (Figure 4) by simply gating the device's decoded address with the write strobe for the $\overline{\text{HOLD}}$ input. Thus, a write cycle to the CS5014's base address will initiate a conversion (the data word is irrelevant). However, the write cycle must be to the odd address (A0 high) to avoid initiating a software controlled reset (see *Reset*, page 41).

The calibration control inputs, CAL, and $\overline{\text{INTRLV}}$ are also internally latched by $\overline{\text{CS}}$, so they must be in the appropriate state whenever the chip is selected during a read or write cycle. Address lines A1 and A2 are shown connected to CAL and $\overline{\text{INTRLV}}$ in Figure 4 placing calibration under microprocessor control as well. Thus, any read or write cycle to the CS5014's base address will initiate or terminate calibration.

Conversion Time/Throughput

Upon completing a conversion cycle and returning to the track mode, the CS5014 requires time to acquire the analog input signal before another conversion can be initiated. The acquisition time is specified as six master clock cycles plus 2.25µs. This adds to the conversion time to define the converter's maximum throughput. The conversion time of the CS5014, in turn, depends on the sampling, calibration, and master clock conditions.

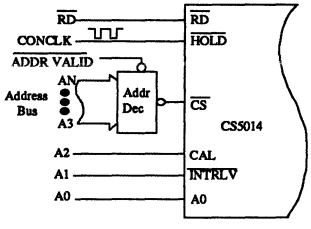


Figure 4a. Conversions Asynchronous to Master Clock

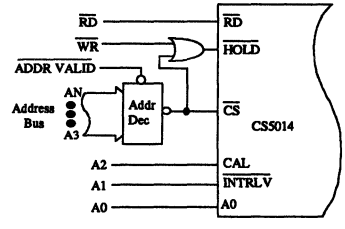


Figure 4b. Conversions under Microprocessor Control

Asynchronous Sampling

The CS5014 internally operates from a clock which is delayed and divided down from the master clock ($f_{CLK}/4$). If sampling is not synchronized to this internal clock, the conversion cycle may not begin until up to four clock cycles after $\overline{HOLD}$ goes low *even though the charge is trapped immediately.* In this asynchronous mode (Figure 3a), the four clock cycles add to the minimum 57 clock cycles to define the maximum conversion time (see Figure 5a and Table 1).

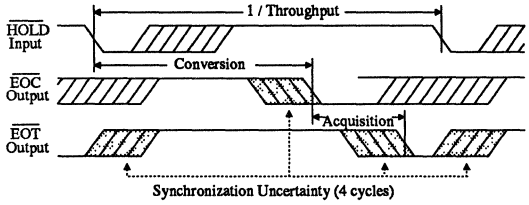


Figure 5a. Asynchronous Sampling (External Clock)

Synchronous Sampling

To achieve maximum throughput, sampling can be synchronized with the internal conversion clock by connecting the End-of-Track ($\overline{EOT}$) output to $\overline{HOLD}$ (Figure 3b). The $\overline{EOT}$ output falls 15 master clock cycles after $\overline{EOC}$ indicating the analog input has been acquired to the CS5014's specified accuracy. The $\overline{EOT}$ output is synchronized to the internal conversion clock, so the four clock cycle synchronization uncertainty is removed yielding throughput at 1/72nd of the master clock frequency (see Figure 5b and Table 1).

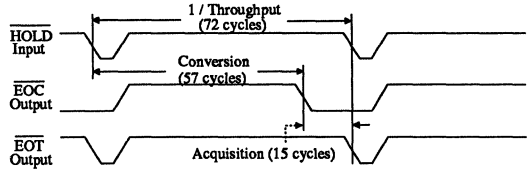


Figure 5b. Synchronous (Loopback) Mode

Also, the CS5014's internal RC oscillator exhibits significant jitter (typically ±0.05% of its period), which is high compared to crystal oscillators. If the CS5014 is configured for synchronous sampling while operating from its internal oscillator, this jitter will directly affect sampling purity.

The $\overline{EOT}$ output is an accurate indicator of the CS5014's acquisition requirement when operating at the -14 version's full rated speed (3.75µs with a 4MHz master clock). However, $\overline{EOT}$ will allow the CS5014 more acquisition time than necessary when operating with a clock less than 4MHz. The $\overline{EOT}$ output always falls 15 master clock cycles after $\overline{EOC}$. The CS5014 only needs 3.75µs (six cycles @4MHz plus 2.25µs). When operating the -28 with a master clock of 2MHz or less, higher throughput can be achieved than in the loopback configuration by using an external counter. The counter should be reset by the falling edge of $\overline{EOC}$ and count the appropriate number of clock cycles after each conversion. When the total time is greater than six clock

	Conversion Time		Throughput Time	
Sampling Mode	min	max	min	max
Synchronous (Loopback)	57T	57T	72T	72T
Asynchronous	57T	61T + 235ns	N/A	67T + 2.25µs

(T ≡ one master clock cycle)

Table 1. Conversion and Throughput Times

cycles plus 2.25µs the counter can trigger a new conversion at $\overline{HOLD}$. For example, when using a 2MHz clock, 2.25µs takes between four and five clock cycles. When six cycles are added to this it is seen that the counter should trigger a new conversion at the eleventh clock cycle.

Reset

Upon power up, the CS5014 must be reset to guarantee a consistent starting condition and initially calibrate the device. Due to the CS5014's low power dissipation and low temperature drift, virtually no warm-up time is required before reset to accommodate any self-heating effects. However, the voltage reference input should have stabilized to within 1% of its final value before RST falls to guarantee an accurate calibration. Later, the CS5014 may be reset at any time to initiate a single full calibration. Reset overrides all other functions. If reset, the CS5014 will clear and initiate a new calibration cycle mid-conversion or mid-calibration.

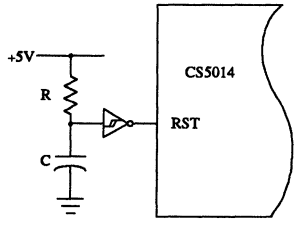


Figure 6. Power-On Reset Circuitry

Resets can be initiated in hardware or software. The simplest method of resetting the CS5014 involves strobing the RST pin high. When RST is brought high all internal logic clears. When it returns low a full calibration begins which takes 1,443,840 master clock cycles (approximately 360ms with a 4MHz clock) to complete. A simple power-on reset circuit can be built using a resistor and capacitor, and a Schmidt-trigger inverter to prevent oscillation (see Figure 6). The CS5014 can also be reset in software when under microprocessor control. The CS5014 will reset whenever $\overline{CS}$, A0, and $\overline{HOLD}$ are taken low simultaneously. See the *Microprocessor Interface* section on page 42 to eliminate the possibility of inadvertent software reset. The $\overline{EOC}$ output remains high throughout the reset operation and will fall upon its completion. It can thus be used to generate an interrupt indicating the CS5014 is ready for operation. Six master clock cycles plus 2.25µs must be allowed after $\overline{EOC}$ falls to allow for acquisition. Under microprocessor-independent operation with 3-states permanently enabled ($\overline{CS}$, $\overline{RD}$ low; A0 high) the $\overline{EOC}$ output will not fall at the completion of the reset operation.

Initiating Calibration

All modes of calibration can be controlled in hardware or software. Accuracy can thereby be insured at any time or temperature throughout operating life. After initial calibration at power-up, the CS5014's charge-redistribution design yields better temperature drift and more graceful aging than resistor-based technologies, so calibration is actually required less often than with traditional devices.

The first mode of calibration, reset, results in a single full calibration cycle. The second type of calibration, termed "burst" cal, is useful when the ADC sees some downtime but not enough to perform a full reset calibration. Burst cal can be terminated mid-calibration; it picks up where it left off previously, so calibrations can be done in piecemeal fashion. Burst cal is initiated by bringing the CAL input high with $\overline{CS}$ low. The CAL input is level-triggered and latches on the rising edge of $\overline{CS}$, so a write cycle can be used to control calibration in software. Burst cal will continue to loop through calibration cycles until terminated. Once CAL returns low, at least 26 master clock cycles plus 2.25µs (8.75µs @ 4MHz clock) must be allowed before a conversion is initiated to ensure the CS5014 has completed its calibration experiment and has

acquired the analog input. The $\overline{EOC}$ output indicates the completion of the final calibration experiment. (See note on page 57.)

The CS5014 features a background calibration mode called "interleave." Interleave appends a single calibration experiment to each conversion cycle and thus requires no dead time for calibration. The CS5014 gathers data between conversions and will adjust its transfer function once it completes the entire sequence of experiments (one calibration cycle per 72,192 conversions). Initiated by bringing both the $\overline{INTRLV}$ input and $\overline{CS}$ low (or hard-wiring $\overline{INTRLV}$ low), interleave extends the CS5014's effective conversion time by 20 master clock cycles (5µs @ 4MHz). Other than reduced throughput, interleave is totally transparent to the user.

Burst calibrations initiated at CAL pick up where interleave left off, so calibration cycles can be hastened by "bursting" a number of experiments whenever the CS5014 sees free time. Interleave is subordinate to burst calibrations, so $\overline{INTRLV}$ could still be externally tied low.

Microprocessor Interface

The CS5014 features an intelligent microprocessor interface which offers detailed status information and allows software control of the self-calibration functions. Output data is available in either 8-bit or 16-bit formats for easy interfacing to industry-standard microprocessors.

Strobing both $\overline{CS}$ and $\overline{RD}$ low enables the CS5014's 3-state output buffers with either output data or status information depending on the status of A0. An address bit can be connected to A0 as shown in Figure 4b thereby memory mapping the status register and output data. Conversion status can be polled in software by reading the status register ($\overline{CS}$ and $\overline{RD}$ strobed low with A0 low), and masking status bits S0-S5 and S7 (by logically AND'ing the status word with 01000000) to determine the value of S6. Similarly, the software routine can determine calibration status using other status bits (see Table 2). *Care must be taken not to read the status register (A0 low) while $\overline{HOLD}$ is low, or a software reset will result* (see *Reset*, page 41).

Alternatively, the End-of-Convert ($\overline{EOC}$) output can be used to generate an interrupt or drive a DMA controller to dump the output directly into memory after each conversion. The $\overline{EOC}$ pin falls as each conversion cycle is completed and data is valid at the output. It returns high within four master clock cycles of the first subsequent data read operation or after the start of a new conversion cycle.

PIN	STATUS BIT	STATUS	DEFINITION
D0	S0	$\overline{END\ OF\ CONVERSION}$	Falls upon completion of a conversion, and returns high on the first subsequent read.
D1	S1	RESERVED	Reserved for factory use.
D2	S2	LOW BYTE/$\overline{HIGH\ BYTE}$	When data is to be read in an 8-bit format (BW=0), indicates which byte will appear at the output next.
D3	S3	$\overline{END\ OF\ TRACK}$	When low, indicates the input has been acquired to the devices specified accuracy.
D4	S4	RESERVED	Reserved for factory use.
D5	S5	TRACKING	High when the device is tracking the intput.
D6	S6	CONVERTING	High when the device is converting the held input.
D7	S7	CALIBRATING	High when the device is calibrating.

Table 2. Status Bit Definitions

To interface with a 16-bit data bus, the BW input to the CS5014 should be held high and all 14 data bits read in parallel on pins D15-D2. With an 8-bit bus, the converter's 14-bit result must be read in two portions. In this instance, BW should be held low and the 8 MSB's obtained on the first read cycle following a conversion. The second read cycle will yield the 6 LSB's with two trailing zeroes. Both bytes appear on pins D0-D7. The upper/lower bytes of the same data will continue to toggle on subsequent reads until the next conversion finishes. Status bit S2 indicates which byte will appear on the next data read operation.

The CS5014 internally buffers its output data, so data can be read while the device is tracking or converting the next sample. Therefore, retrieving the converter's digital output requires no reduction in ADC throughput. Enabling the 3-state outputs while the CS5014 is converting will not introduce conversion errors. When TTL loads are utilized the potential for crosstalk between digital and analog sections of the system is increased. This crosstalk is due to high digital supply and signal currents arising from the TTL drive current required of each digital output. Connecting CMOS logic to the digital outputs is recommended. Suitable logic families include 4000B, 74HC, 74AC, 74ACT, and 74HCT.

The two calibration control inputs, CAL and $\overline{\text{INTRLV}}$, are level-triggered and latched on the rising edge of $\overline{\text{CS}}$. Calibration can be placed under software control by connecting address lines to the CAL and $\overline{\text{INTRLV}}$ inputs as shown in Figure 4a. Any read or write cycle to the CS5014's base address will thereby initiate or terminate calibration.

Microprocessor Independent Operation

The CS5014 can be operated in a stand-alone mode independent of intelligent control. In this mode, $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are hard-wired low permanently enabling the 3-state output buffers. A free-running condition is established when BW is tied high, CAL is tied low, and $\overline{\text{HOLD}}$ is continually strobed low or tied to $\overline{\text{EOT}}$. The CS5014's $\overline{\text{EOC}}$ output can be used to externally latch the output data if desired. With $\overline{\text{CS}}$ and $\overline{\text{RD}}$ hard-wired low, $\overline{\text{EOC}}$ will strobe low for four master clock cycles after each conversion. Data will be unstable up to 100ns after $\overline{\text{EOC}}$ falls, so it should be latched on the rising edge of $\overline{\text{EOC}}$.

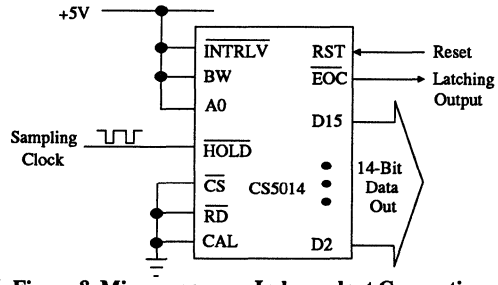


Figure 8. Microprocessor-Independent Connections

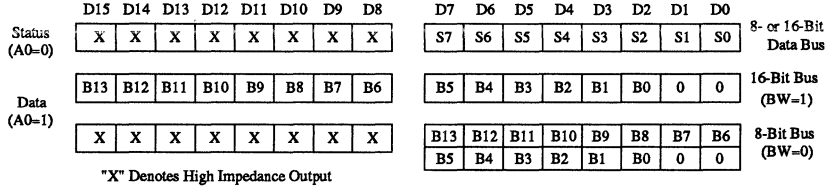


Figure 7. Data Format

Serial Output

All successive-approximation A/D converters derive their digital output serially starting with the MSB. The CS5014 presents each bit to the SDATA pin four master clock cycles after it is derived and can be latched using the serial clock output, SCLK. Just subsequent to each bit decision SCLK will fall and return high once the bit information on SDATA has stabilized. Thus, the rising edge of the SCLK output should be used to clock the data from the CS5014 (See Figure 9).

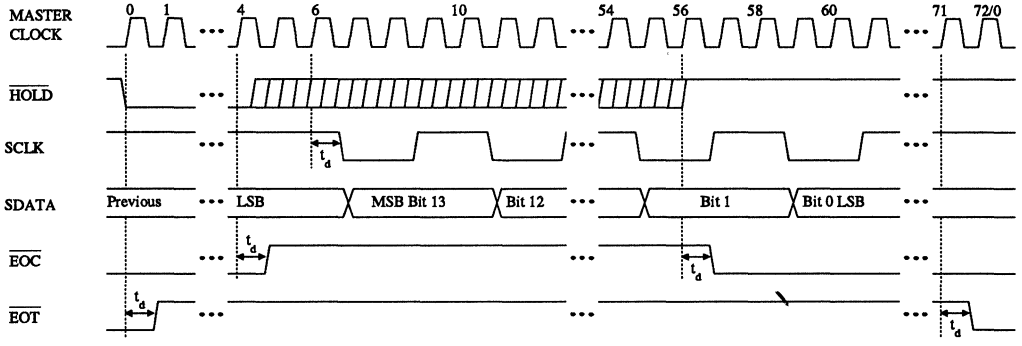
ANALOG CIRCUIT CONNECTIONS

Most popular successive-approximation A/D converters generate dynamic loads at their analog connections. The CS5014 internally buffers all analog inputs (AIN, VREF, and AGND) to ease the demands placed on external circuitry. However, accurate system operation still requires careful attention to details at the design stage regarding source impedances as well as grounding and decoupling schemes.

Reference Considerations

An application note titled "*Voltage References for the CS501X/CSZ511X Series of A/D Converters*" is available for the CS5014. In addition to working through a reference circuit design example, it offers seven built-and-tested reference circuits.

During conversion, each capacitor of the calibrated capacitor array is switched between VREF and AGND in a manner determined by the successive-approximation algorithm. The charging and discharging of the array results in a current load at the reference. The CS5014 includes an internal buffer amplifier to minimize the external reference circuit's drive requirement and preserve the reference's integrity. Whenever the array is switched during conversion, the buffer is used to pre-charge the array thereby providing the bulk of the necessary charge. The appropriate array capacitors are then switched to the unbuffered VREF pin to avoid any errors due to offsets and/or noise in the buffer.



notes: 1. t_d can vary from 135ns - 235ns over military temperature range and over ± 10% supply variation.
2. For asynchronous mode, transitions of SCLK, SDATA, $\overline{EOC}$, $\overline{EOT}$ can shift by up to 4 clocks; e.g. the first high to low transition of SLCK may be on clock #6 to #9. The timing relationship between SLCK, SDATA, $\overline{EOC}$, and $\overline{EOT}$ is fixed.

Figure 9. Serial Output Timing

The external reference circuitry need only provide the residual charge required to fully charge the array after pre-charging from the buffer. This creates an ac current load as the CS5014 sequences through conversions. The reference circuitry must have a low enough output impedance to drive the requisite current without changing its output voltage significantly. As the analog input signal varies, the switching sequence of the internal capacitor array changes. The current load on the external reference circuitry thus varies in response with the analog input. Therefore, the external reference must not exhibit significant peaking in its output impedance characteristic at signal frequencies or their harmonics.

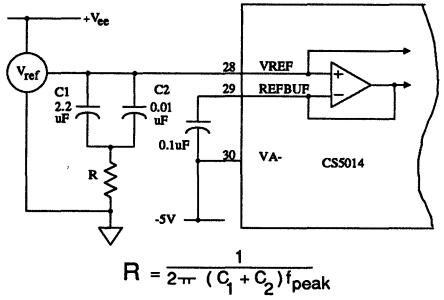


Figure 10. Reference Connections

A large capacitor connected between VREF and AGND can provide sufficiently low output impedance at the high end of the frequency spectrum, while almost all precision references exhibit extremely low output impedance at dc. The presence of large capacitors on the output of some voltage references, however, may cause peaking in the output impedance at intermediate frequencies. Care should be exercised to ensure that significant peaking does not exist or that some form of compensation is provided to eliminate the effect.

The magnitude of the current load on the external reference circuitry will scale to the master clock frequency. At full speed (4MHz clock), the reference must supply a maximum load current of 10µA peak-to-peak (1µA typical). An output impedance of 4Ω will therefore yield a maximum error of 40µV. With a 4.5V reference and LSB size of 275µV, this would insure better than 1/4 LSB accuracy. A 2.2µF capacitor exhibits an impedance of less than 4Ω at frequencies greater than 5kHz. A high-quality tantalum capacitor in parallel with a smaller ceramic capacitor is recommended.

Peaking in the reference's output impedance can occur because of capacitive loading at its output. Any peaking that might occur can be reduced by placing a small resistor in series with the capacitors (Figure 10). The equation in Figure 10 can be used to help calculate the optimum value of R for a particular reference. The term "f_{peak}" is the frequency of the peak in the output impedance of the reference before the resistor is added.

The CS5014 can operate with a wide range of reference voltages, but signal-to-noise performance is maximized by using as wide a signal range as possible. The recommended reference voltage is 4.5 volts. The CS5014 can actually accept reference voltages up to the positive analog supply. However, the buffer's offset may increase as the reference voltage approaches VA+ thereby increasing external drive requirements at VREF. A 4.5V reference is the maximum reference voltage recommended. This allows 0.5V headroom for the internal reference buffer. Also, the buffer enlists the aid of an external 0.1µF ceramic capacitor which must be tied between its output, REFBUF, and the negative analog supply, VA-. For more information on references, consult "Application Note: *Voltage References for the CS501X/CSZ511X Series of A/D Converters*".

Analog Input Connection

The analog input terminal functions similarly to the VREF input after each conversion when

switching into the track mode. During the first six master clock cycles in the track mode, the buffered version of the analog input is used for pre-charging the capacitor array. An additional period is required for fine-charging directly from AIN to obtain the specified accuracy. Figure 11 exemplifies this operation. During pre-charge the charge on the capacitor array first settles to the buffered version of the analog input. This voltage is offset from the actual input voltage. During fine-charge, the charge then settles to the accurate unbuffered version.

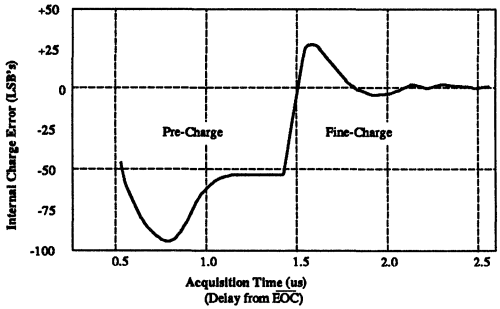


Figure 11. Internal Acquisition Time

The acquisition time of the CS5014 depends on the master clock frequency. This is due to a fixed pre-charge period. For instance, operating the -14 version with an external 4MHz master clock results in a 3.75µs acquisition time: 1.5µs for pre-charging (6 clock cycles) and 2.25µs for fine-charging. Fine-charge settling is specified as a maximum of 2.25µs for an analog source impedance of less than 200Ω. In addition, the comparator requires a source impedance of less than 400Ω around 2MHz for stability, which is met by practically all bipolar op amps. Large dc source impedances can be accommodated by adding capacitance from AIN to ground (typically 200pF) to decrease source impedance at high frequencies. However, high dc source resistances will increase the input's RC time constant and extend the necessary acquisition time.

The CS5014 can track full power signals up to 28kHz in the track mode. During the first six clock cycles following a conversion (pre-charge), the CS5014 is capable of slewing at 5V/µs in unipolar mode. In bipolar mode, only half the capacitor array is connected to the analog input so the CS5014 can slew at 10V/µs. After the first six master clock cycles, it will slew at 0.25V/µs in the unipolar mode and 0.5V/µs in bipolar mode. Acquisition of fast slewing signals (step functions) can be hastened if the step occurs during or immediately following the conversion cycle. For instance, channel selection in multiplexed applications should occur while the CS5014 is converting (see Figure 12). Multiplexer settling is thereby

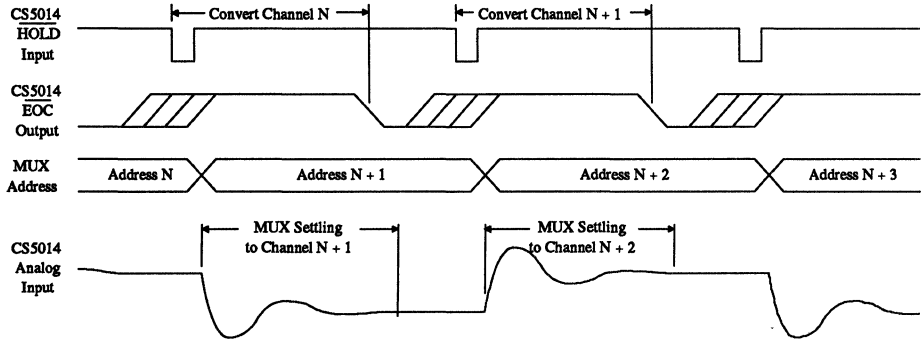


Figure 12. Pipelined MUX Input Channels

removed from the overall throughput equation, and the CS5014 can convert at full speed.

Analog Input Range/Coding Format

The reference voltage directly defines the input voltage range in both the unipolar and bipolar configurations. In the unipolar configuration (BP/$\overline{UP}$ low), the first code transition occurs 1/2 LSB above AGND, and the final code transition occurs 3/2 LSB's below VREF. Coding is in straight binary format. In the bipolar configuration (BP/$\overline{UP}$ high), the first code transition occurs 1/2 LSB above -VREF and the last transition occurs 3/2 LSB's below +VREF. Coding is in an offset-binary format. Positive full scale gives a digital output of 1111111111111, and negative full scale gives a digital output of 0000000000000.

Grounding and Power Supply Decoupling

The CS5014 uses the analog ground connection, AGND, only as a reference voltage. No dc power currents flow through the AGND connection, and it is completely independent of DGND. However, any noise riding on the AGND input relative to the system's analog ground will induce conversion errors. Therefore, both the analog input and reference voltage should be referred to the AGND pin, which should be used as the entire system's analog ground.

The digital and analog supplies are isolated within the CS5014 and are pinned out separately to minimize coupling between the analog and digital sections of the chip. All four supplies should be decoupled to their respective grounds using 0.1µF ceramic capacitors. If significant low-frequency noise is present on the supplies, 1uF tantalum capacitors are recommended in parallel with the 0.1µF capacitors.

The positive digital power supply of the CS5014 must never exceed the positive analog supply by more than a diode drop or the CS5014 could experience permanent damage. If the two supplies are derived from separate sources, care must be taken that the analog supply comes up first at power-up. The system connection diagram on page 51 shows a decoupling scheme which allows the CS5014 to be powered from a single set of ± 5V rails. The positive digital supply is derived from the analog supply through a 10Ω resistor to avoid the analog supply dropping below the digital supply. If this scheme is utilized, care must be taken to insure that any digital load currents (which flow through the 10Ω resistors) do not cause the magnitude of digital supplies to drop below the analog supplies by more than 0.5 volts. Digital supplies must always remain above the minimum specification.

As with any high-precision A/D converter, the CS5014 requires careful attention to grounding and layout arrangements. However, no unique layout issues must be addressed to properly apply the CS5014. The CDB5014 evaluation board is available for the CS5014, which avoids the need to design, build, and debug a high-precision PC board to initially characterize the part. The board comes with a socketed CS5014, and can be quickly reconfigured to simulate any combination of sampling, calibration, master clock, and analog input range conditions.

CS5014 PERFORMANCE

Differential Nonlinearity

The most prevalent source of nonlinearity in high resolution converters is bit weight errors. These errors arise from the deviation of bits from their ideal binary-weighted ratios, and lead to nonideal widths for each code. If DNL errors are large, and code widths shrink to zero, it is possible for one or more codes to be entirely missing. The CS5014 calibrates all bits in the capacitor array to a small fraction of an LSB resulting in nearly ideal DNL. A histogram plot of typical DNL can be seen in Figure 13.

A histogram test is a statistical method of deriving an A/D converter's differential nonlinearity. A ramp is input to the A/D and a large number of samples are taken to insure a high confidence level in the test's result. The number of occurrences for each code is monitored and stored. A perfect A/D converter would have all codes of equal size and therefore equal numbers of occurrences. In the histogram test a code with the average number of occurrences will be considered ideal (DNL = 0). A code with more or less occurrences than average will appear as a DNL of greater or less than zero LSB. A missing code has zero occurrences, and will appear as a DNL of -1 LSB.

Integral Nonlinearity

Integral nonlinearity is defined as the deviation of the transfer function from an ideal straight line through zero and full scale. Even if differential linearity errors are small, they may combine to produce a gross INL error at some point in the transfer function. A unique calibration algorithm, a lack of superposition of errors due to a capacitor based DAC, and low capacitor voltage coefficient keep INL errors below ± 1/2 LSB.

Clock Feedthrough

Maintaining the integrity of analog signals in the presence of digital switching noise is a difficult problem. The CS5014 can be synchronized to the digital system using the CLKIN input to avoid conversion errors due to asynchronous interference. However, digital interference will still affect sampling purity due to coupling between the CS5014's analog input and master clock.

The effect of clock feedthrough depends on the sampling conditions. If the sampling signal at the $\overline{\text{HOLD}}$ input is synchronized to the master clock, clock feedthrough will appear as a dc offset at the CS5014's output. The offset could theoretically reach the peak coupling magnitude (Figure 14), but the probability of this occurring is small since the peaks are spikes of short duration.

Master Clock		Analog Input	Clock Feedthrough	
Int/Ext	Freq	Source Impedance	RMS	Peak-to-Peak
Internal	2MHz	50 Ω	15uV	70uV
External	2MHz	50 Ω	25uV	110uV
External	4MHz	50 Ω	40uV	150uV
External	4MHz	25 Ω	25uV	110uV
External	4MHz	200 Ω	80uV	325uV

Figure 14. Examples of Measured Clock Feedthrough

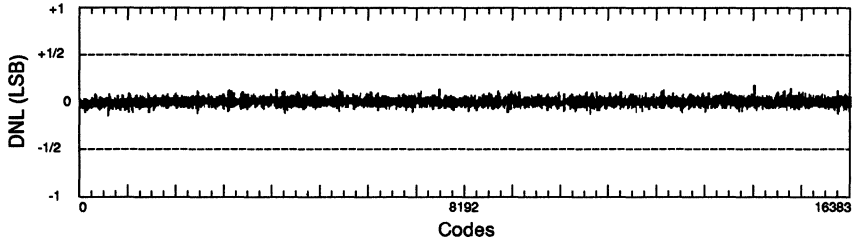


Figure 13. CS5014 Differential Nonlinearity Plot

If sampling is performed asynchronously with the master clock, clock feedthrough will appear as an ac error at the CS5014's output. With a fixed sampling rate, a tone will appear as the clock frequency aliases into the baseband. The tone frequency can be calculated using the equation below and could be selectively filtered in software using DSP techniques.

$$f_{tone} = (Nf_s - f_{clk})$$

where $N = f_{clk}/f_s$ rounded to the nearest integer

The magnitude of clock feedthrough depends on the master clock conditions and the source impedance applied to the analog input. When operating with the CS5014's internally generated clock, the CLKIN input is grounded and the dominant source of coupling is through the device's substrate. As shown in Figure 14, a typical CS5014 operating with its internal oscillator at 2MHz and 50Ω of analog input source impedance wil exhibit only 15μV rms of clock feedthrough. However, if a 2MHz external clock is applied to CLKIN under the same conditions, feedthrough increases to 25μV rms. Feedthrough also increases with clock frequency; a 4MHz clock yields 40μV rms.

Clock feedthrough can be reduced by limiting the source impedance applied at the analog input. As shown in Figure 14, reducing source impedance from 50Ω to 25Ω yields a 15μV rms reduction in feedthrough. Therefore, when operating the CS5014 with high-frequency external master clocks, it is important to minimize source impedance applied to the CS5014's input.

Also, the overall effect of clock feedthrough can be minimized by maximizing the input range and LSB size. The reference voltage applied to VREF can be maximized, and the CS5014 can be operated in bipolar mode which inherently doubles the LSB size over the unipolar mode.

Power Supply Rejection

The CS5014's power supply rejection performance is enhanced by the on-chip self-calibration and an "auto-zero" process. Drifts in power supply voltages at frequencies less than the calibration rate have negligible effect on the CS5014's accuracy. This, of course, is because the CS5014 adjusts its offset to within a small fraction of an LSB during calibration.

Above the calibration frequency the excellent power supply rejection of the internal amplifiers is augmented by an auto-zero process. Any offsets are stored on the capacitor array and are effectively subtracted once conversion is initiated. Figure 15 shows power supply rejection of the CS5014 in the bipolar mode with the analog input grounded and a 300mV p-p ripple applied to each supply. Power supply rejection improves by 6dB in the unipolar mode.

Notches of increased rejection arise from the auto-zeroing at the conversion rate. The frequencies at which these notches occur also depend on the value of the captured analog input. The line shows worst-case rejection for all combinations of conversion rates and input conditions in the bipolar mode. Again, power supply rejection is 6dB better in the unipolar mode.

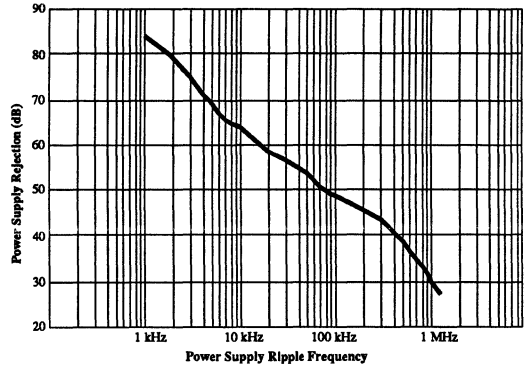


Figure 15. Power Supply Rejection

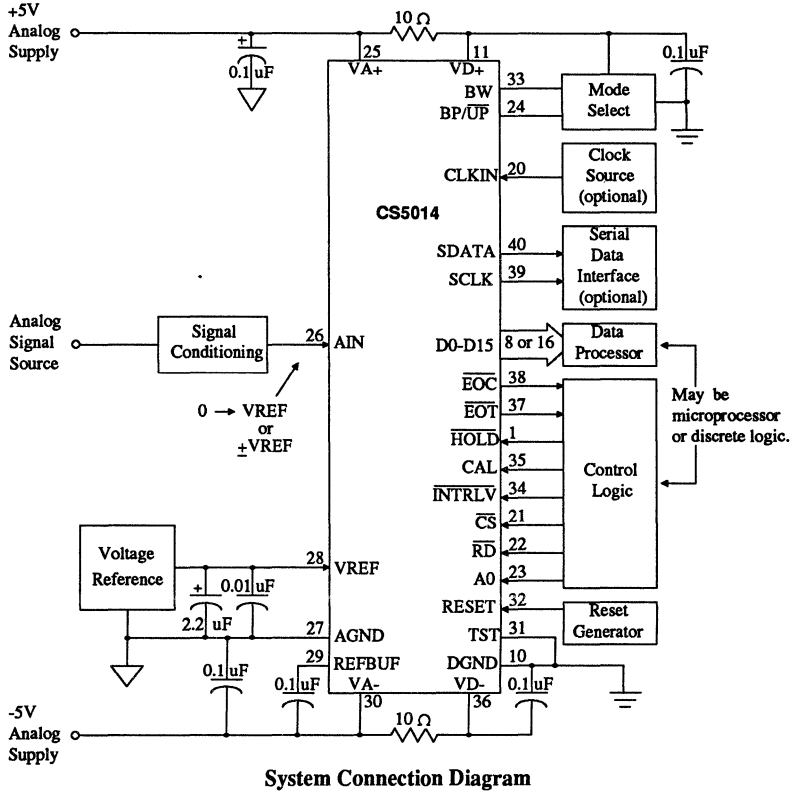
Aperture Jitter

Track-and-hold amplifiers commonly exhibit two types of aperture jitter. The first, more appropriately termed "aperture window", is an input voltage dependent variation in the aperture delay. Its signal-dependency causes distortion at high frequencies. The CS5014's proprietary architecture avoids applying the input voltage across a sampling switch, thus avoiding any "aperture window" effects. The second type of aperture jitter, due to component noise, assumes a random nature. With only 100ps peak-to-peak aperture jitter, the CS5014 can process full-scale signals up to 1/2 the throughput frequency without any errors due to aperture jitter.

$\overline{HOLD}$	$\overline{CS}$	CAL	$\overline{INTRLV}$	$\overline{RD}$	A0	RST	Function
↓	X	X	X	X	*	0	Hold and Start Convert
X	0	1	X	X	*	0	Initiate Burst Calibration
1	0	0	X	X	*	0	Stop Burst Cal and Begin Track
X	0	X	0	X	*	0	Initiate Interleave Calibration
X	0	X	1	X	*	0	Terminate Interleave Cal
X	0	X	X	0	1	0	Read Output Data
1	0	X	X	0	0	0	Read Status Register
X	1	X	X	X	*	X	High Impedance Data Bus
X	X	X	X	1	*	X	High Impedance Data Bus
X	X	X	X	X	X	1	Reset
0	0	X	X	X	0	X	Reset

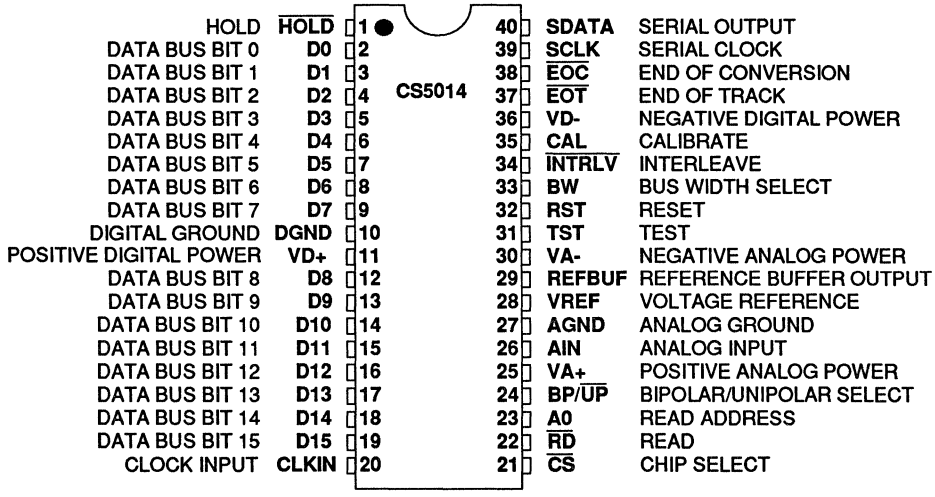
* The status of A0 is not critical to the operation specified. However, A0 should not be low with $\overline{CS}$ and $\overline{HOLD}$ low, or a software reset will result.

CS5014 Truth Table



System Connection Diagram

PIN DESCRIPTIONS



Power Supply Connections

VD+ - Positive Digital Power, PIN 11.
Positive digital power supply. Nominally +5 volts.

VD- - Negative Digital Power, PIN 36.
Negative digital power supply. Nominally -5 volts.

DGND - Digital Ground, PIN 10.
Digital ground reference.

VA+ - Positive Analog Power, PIN 25.
Positive analog power supply. Nominally +5 volts.

VA- - Negative Analog Power, PIN 30.
Negative analog power supply. Nominally -5 volts.

AGND - Analog Ground, PIN 27.
Analog ground reference.

Oscillator

CLKIN - Clock Input, PIN 20.

All conversions and calibrations are timed from a master clock which can either be supplied by driving this pin with an external clock signal, or can be internally generated by tying this pin to DGND.

Digital Inputs

$\overline{\text{HOLD}}$ - Hold, PIN 1.

A falling transition on this pin sets the CS5014 to the hold state and initiates a conversion. This input must remain low at least one master clock cycle plus 50ns.

$\overline{\text{CS}}$ - Chip Select, PIN 21.

When high, the data bus outputs are held in a high impedance state and the input to CAL and $\overline{\text{INTRLV}}$ are ignored. A falling transition initiates or terminates burst or interleave calibration (depending on the status of CAL and $\overline{\text{INTRLV}}$) and a rising transition latches both the CAL and $\overline{\text{INTRLV}}$ inputs. If $\overline{\text{RD}}$ is low, the data bus is driven as indicated by BW and A0.

$\overline{\text{RD}}$ - Read, PIN 22.

When $\overline{\text{RD}}$ and $\overline{\text{CS}}$ are both low, data is driven onto the data bus. If either signal is high, the data bus outputs are held in a high impedance state. The data driven onto the bus is determined by BW and A0.

6

A0 - Read Address, PIN 23.

Determines whether data or status information is placed onto the data bus. When high during the read operation, converted data is placed onto the data bus; when low, the status register is driven onto the bus.

BP/$\overline{\text{UP}}$ - Bipolar/Unipolar Input Select, PIN 24.

When high, the device is configured with a bipolar transfer function ranging from -VREF to +VREF. Encoding is in an offset binary format, with the mid-scale code 100...0000 centered at AGND. When low, the device is configured for a unipolar transfer function from AGND to VREF. Unipolar encoding is in straight binary format.

RST - Reset, PIN 32.

When taken high, all internal digital logic is reset. Upon being taken low, a full calibration sequence is initiated.

BW - Bus Width Select, PIN 33.

When hard-wired high, all 14 data bits are driven onto the bus simultaneously during a data read cycle. When low, the bus is in a byte wide format. On the first read following a conversion, the eight MSB's are driven onto D7-D0. A second read cycle places the six LSB's with two trailing zeros on D7-D0. Subsequent reads will toggle the higher/lower order byte. Regardless of BW's status, a read cycle with A0 low yields the status information on D7-D0.

$\overline{\text{INTRLV}}$ - Interleave, PIN 34.

When latched low using $\overline{\text{CS}}$, the device goes into interleave calibration mode. A full calibration will complete every 79,192 conversions. The effective conversion time extends by 20 clock cycles.

CAL - Calibrate, PIN 35. (See note on page 57.)

When latched high using $\overline{\text{CS}}$, burst calibration results. The device cannot perform conversions during the calibration period which will terminate only once CAL is latched low again. Calibration picks up where the previous calibration left off, and calibration cycles complete every 1,443,840 master clock cycles. If the device is converting when a calibration is signaled, it will wait until that conversion completes before beginning.

Analog Inputs

AIN - Analog Input, PIN 26.

Input range in the unipolar mode is zero volts to VREF. Input range in bipolar mode is -VREF to +VREF. The output impedence of buffer driving this input should be less than or equal to 200Ω.

VREF - Voltage Reference, PIN 28.

The analog reference voltage which sets the analog input range. It represents positive full scale for both bipolar and unipolar operation, and its magnitude sets negative full scale in bipolar mode.

Digital Outputs

D0 through D15 - Data Bus Outputs, PINS 2 thru 9, 12 thru 19.

3-state output pins. Enabled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$, they offer the converter's 16-bit output in a format consistent with the state of BW if A0 is high. If A0 is low, bits D0-D7 offer status register.

$\overline{\text{EOT}}$ - End Of Track, PIN 37.

If low, indicates that enough time has elapsed since the last conversion for the device to acquire the analog input signal (3.75µs for 4MHz external clock).

$\overline{\text{EOC}}$ - End Of Conversion, PIN 38.

This output indicates the end of a conversion or calibration cycle. It is high during a conversion and will fall to a low state upon completion of the conversion cycle indicating valid data is available at the output. Returns high on the first subsequent read or the start of a new conversion cycle.

SDATA - Serial Output, PIN 40.

Presents each output data bit after it is determined by the successive approximation algorithm. Valid on the rising edge of SCLK, data appears MSB first, LSB last, and each bit remains valid until the next bit appears.

SCLK - Serial Clock Output, PIN 39.

Used to clock converted output data serially from the CS5014. Serial data is stable on the rising edge of SCLK.

Analog Outputs

REFBUF - Reference Buffer Output, PIN 29.

Reference buffer output. A 0.1µF ceramic capacitor must be tied between this pin and VA-.

Miscellaneous

TST - Test, PIN 31.

Allows access to the CS5014's test functions which are reserved for factory use. Must be tied to DGND.

ERROR DEFINITIONS

Linearity Error - The deviation of a code from a straight line passing through the endpoints of the transfer function after zero- and full-scale errors have been accounted for. "Zero-scale" is a point 1/2 LSB below the first code transition and "full-scale" is a point 1/2 LSB beyond the code transition to all ones. The deviation is measured from the middle of each particular code. Units in LSB's.

Differential Linearity - The deviation of a code's width from the ideal width. Units in LSB's.

Full Scale Error - The deviation of the last code transition from the ideal (VREF-3/2 LSB's). Units in LSB's.

Unipolar Offset - The deviation of the first code transition from the ideal (1/2 LSB above AGND) when in unipolar mode (BP/UP low). Units in LSB's.

Bipolar Offset - The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below AGND) when in bipolar mode (BP/$\overline{UP}$ high). Units in LSB's.

Bipolar Negative Full-Scale Error - The deviation of the first code transition from the ideal when in bipolar mode (BP/$\overline{UP}$ high). The Ideal is defined as lying on a straight line which passes through the final and mid-scale code transitions. Units in LSB's.

Total Unadjusted Error - The worst-case combination of offset error, full-scale error, and linearity error. Units in LSB's.

Aperture Time - The time required after the hold command for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

Aperture Jitter - The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

Note: Temperatures specified define ambient conditions in free-air during test and do not refer to the junction temperature of the device.

Ordering Guide

Model	Conversion Time	Temp. Range	Package
CS5014-KP28	28.50 µs	0 to +70 °C	40-Pin Plastic DIP
CS5014-KP14	14.25 µs	0 to +70 °C	40-Pin Plastic DIP
CS5014-BC28	28.50 µs	-40 to +85 °C	40-Pin Ceramic Side-Brazed DIP
CS5014-BC14	14.25 µs	-40 to +85 °C	40-Pin Ceramic Side-Brazed DIP
CS5014-TC14	14.25 µs	-55 to +125 °C	40-Pin Ceramic Side-Brazed DIP

ADDENDUM

Burst Calibration

Burst calibration mode allows control of partial calibration cycles. Due to an unforeseen condition inside the part, asynchronous termination of calibration (CAL brought low) may result in a sub-optimal calibration result. It is recommended that burst calibration is not used, until the silicon is revised to prevent this effect.

The reset and interleave mode work perfectly, and should be used instead of burst mode. The CS5014's very low drift over temperature means that, under most circumstances, calibration need only be performed at power-up, using reset (See *Analog Characteristics* table on the second page of this data sheet).

If you wish to use burst calibration, then please contact the factory for advice and new part availability information.

• Notes •

Semiconductor Corporation

CS5016

16-Bit, 16us Self-Calibrating A/D Converter

Features

- Monolithic CMOS A/D Converter
  - Microprocessor Compatible
  - Parallel and Serial Output
  - Inherent Track/Hold Input
- True 16-Bit Precision
  - Linearity Error: 0.001% FS
  - No Missing Codes
- 16.25 Microsecond Conversion Time
  - Throughput Rates up to 50kHz
- Self Calibration Maintains Accuracy Over Time and Temperature
- Low Power Dissipation: 120mW
- Pin Compatible with CS5012/CS5014

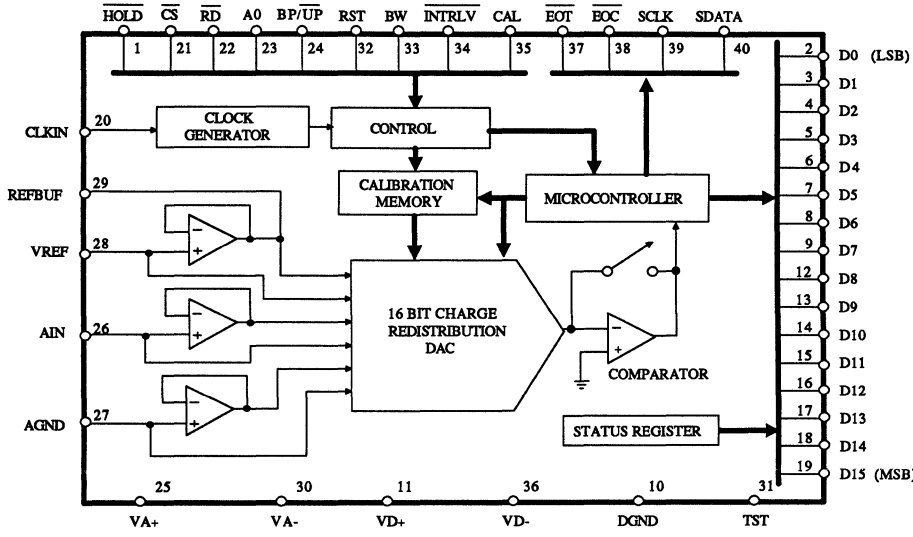
General Description

The CS5016 is a 16-bit monolithic CMOS analog to digital converter with 16.25 microsecond conversion time. Unique self-calibration circuitry, which can be under intelligent control, insures maximum nonlinearity of 0.001% FS and no missing codes. Offset and full scale errors are kept within 1 LSB, eliminating the need for manual calibration of any kind. Unipolar and bipolar input ranges are digitally selectable.

The CS5016 consists of a DAC, conversion and calibration microcontroller, oscillator, comparator, microprocessor compatible 3-State I/O, and calibration circuitry. The input track-and-hold, inherent to the device's sampling architecture, acquires the analog input signal after each conversion within 3.75us allowing throughput rates up to 50kHz.

The CS5016 is pin compatible with the CS5012 and CS5014 A/D converters allowing system upgrading and downgrading without hardware alterations.

ORDERING INFORMATION: Page 85



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, Texas 78760
(512)445-7222 TWX:910-874-1352

ANALOG CHARACTERISTICS (T_A = 25°C; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 4.5V; f_{clk} = 4MHz for -16, 2MHz for -32; Analog Source Impedance = 200Ω; Synchronous Sampling.)

Parameter *		CS5016 -J,K min	CS5016 -J,K typ	CS5016 -J,K max	CS5016 -A,B min	CS5016 -A,B typ	CS5016 -A,B max	CS5016 -S,T min	CS5016 -S,T typ	CS5016 -S,T max	Units
Specified Temperature Range			0 to +70			-40 to +85			-55 to +125		°C
Accuracy											
Linearity Error	(Note 1)										
T_{min} to T_{max}	-J, A, S		0.002	0.003		0.002	0.003		0.002	0.003	% FS
T_{min} to T_{max}	-K, B, T		0.001	0.0015		0.001	0.0015		0.001	0.0015	% FS
Differential Linearity	(Note 2)	16			16			16			Bits
Full Scale Error	(Note 1)		±2	±3		±2	±3		±2	±3	LSB
T_{min} to T_{max}	(Note 3)		±1			±1			±2		ΔLSB
Unipolar Offset	(Note 1)		±1	±3/2		±1	±3		±1	±3	LSB
T_{min} to T_{max}	(Note 3)		±1			±1			±2		ΔLSB
Bipolar Offset	(Note 1)		±1	±3/2		±1	±2		±1	±2	LSB
T_{min} to T_{max}	(Note 3)		±1			±2			±2		ΔLSB
Bipolar Negative Full-Scale Error	(Note 1)		±2	±3		±2	±3		±2	±3	LSB
T_{min} to T_{max}	(Note 3)		±1			±2			±2		ΔLSB
Noise (Note 4)	Unipolar Mode		35			35			35		uV_{rms}
	Bipolar Mode		70			70			70		uV_{rms}
Analog Input											
Aperture Time			25			25			25		ns
Aperture Jitter			100			100			100		ps
Aperture Time Matching	(Note 5)		TBD			TBD			TBD		ns
Full Power Bandwidth	(Note 6)		25			25			25		kHz
Input Capacitance (Note 7)	Unipolar Mode		275	375		275	375		275	375	pF
	Bipolar Mode		165	220		165	220		165	220	pF

Notes:
1. Applies after calibration at any temperature within the specified temperature range.
2. Minimum resolution for which no missing codes is guaranteed.
3. Total drift over specified temperature range since calibration at power-up at 25°C.
4. Wideband noise aliased into the baseband. Referred to the input.
5. Part to part.
6. V_{in} = 9V p-p. Refer to *Analog Input* section on page 73 for discussion of input slew rate.
7. Applies only in track mode. When converting or calibrating, input capacitance will not exceed 15pF.

* Refer to *Error Definitions* on page 84.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (continued)

Parameter	CS5016-J,K min	typ	max	CS5016-A,B min	typ	max	CS5016-S,T min	typ	max	Units
Conversion & Throughput										
Conversion Time –16			16.25			16.25			16.25	us
(Notes 8,9) –32			32.5			32.5			32.5	us
Acquisition Time –16		3.0	3.75		3.0	3.75		3.0	3.75	us
(Note 9) –32		4.5	5.25		4.5	5.25		4.5	5.25	us
Throughput –16	50.0			50.0			50.0			kHz
(Note 9) –32	26.5			26.5			26.5			kHz
Power Supplies										
DC Power Supply Currents (Note 10)										
I_{A+}		9	19		9	19		9	19	mA
I_{A-}		–9	–19		–9	–19		–9	19	mA
I_{D+}		3	6		3	6		3	6	mA
I_{D-}		–3	–6		–3	–6		–3	–6	mA
Power Dissipation (Note 10)		120	250		120	250		120	250	mW
Power Supply Rejection (Note 11)										
Positive Supplies		84			84			84		dB
Negative Supplies		84			84			84		dB

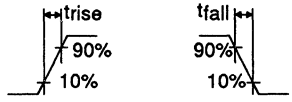
Notes:
8. Measured from falling transition on $\overline{HOLD}$ to falling transition on $\overline{EOC}$.
9. Conversion, acquisition, and throughput times depend on the master clock, sampling, and calibration conditions. The numbers shown assume sampling and conversion is synchronized with the CS5016's conversion clock, interleave calibrate is disabled, and operation is from the full-rated, external clock. A detailed discussion of conversion timing appears on page 68.
10. All outputs unloaded. All inputs CMOS levels.
11. With 300mV p-p, 1kHz ripple applied to each analog supply separately in bipolar mode. Rejection improves by 6dB in the unipolar mode to 90dB. A plot of typical power supply rejection versus frequency appears on page 78.

6

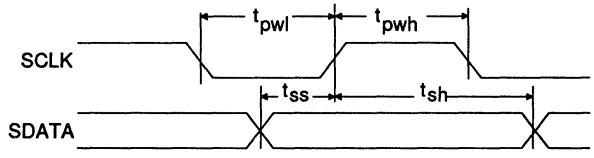
SWITCHING CHARACTERISTICS (T_A = T_{min} to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 50pF)

Parameter	Symbol	Min	Typ	Max	Units
Master Clock Frequency:					
Internally Generated: -16	f_{CLK}	2	-	-	MHz
-32		1	-	-	
Externally Supplied: -16		-	-	4	
-32		-	-	2	
Master Clock Duty Cycle	-	30	-	70	%
Rise Times: Any Digital Input	t_{rise}	-	-	1.0	us
Any Digital Output		-	20	-	ns
Fall Times: Any Digital Input	t_{fall}	-	-	1.0	us
Any Digital Output		-	20	-	ns
$\overline{HOLD}$ Pulse Width	t_{hpw}	$1/f_{CLK}$ + 50	-	t_c	ns
Conversion Time	t_c	(Note 12)	-	(Note 12)	us
Data Delay Time	t_{dd}	-	40	100	ns
$\overline{EOC}$ Pulse Width (Note 13)	t_{epw}	$4/f_{CLK}$ - 20	-	-	ns
Set Up Times: CAL, $\overline{INTRLV}$ to $\overline{CS}$ Low	t_{cs}	20	10	-	ns
A0 to $\overline{CS}$ and $\overline{RD}$ Low	t_{as}	20	10	-	
Hold Times:					
$\overline{CS}$ or $\overline{RD}$ High to A0 Invalid	t_{ah}	50	30	-	ns
$\overline{CS}$ High to CAL, $\overline{INTRLV}$ Invalid	t_{ch}	50	30	-	
Access Times: $\overline{CS}$ Low to Data Valid					
-J,K,A,B	t_{ca}	-	90	120	ns
-S,T		-	115	150	
$\overline{RD}$ Low to Data Valid					
-J,K,A,B	t_{ra}	-	90	120	ns
-S,T		-	115	150	
Output Float Delay: -J,K,A,B	t_{fd}	-	50	110	ns
$\overline{CS}$ or $\overline{RD}$ High to Output Hi-Z -S,T			50	140	
Serial Clock Pulse Width Low	t_{pwl}	-	$2/f_{CLK}$	-	ns
Pulse Width High	t_{pwh}	-	$2/f_{CLK}$	-	
Set Up Times: SDATA to SCLK Rising	t_{ss}	$2/f_{CLK}$ - 100	$2/f_{CLK}$	-	ns
Hold Times: SCLK Rising to SDATA	t_{sh}	$2/f_{CLK}$ - 100	$2/f_{CLK}$	-	ns

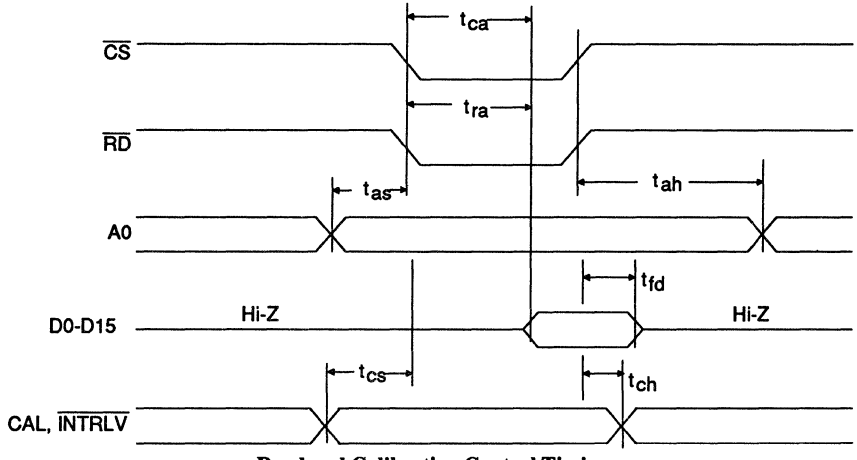
Notes: 12. See Table 1 and master clock frequencies above.
13. $\overline{EOC}$ remains low 4 master clock cycles if $\overline{CS}$ and $\overline{RD}$ are held low. Otherwise, it returns high within 4 master clock cycles from the start of a data read operation or a conversion cycle.



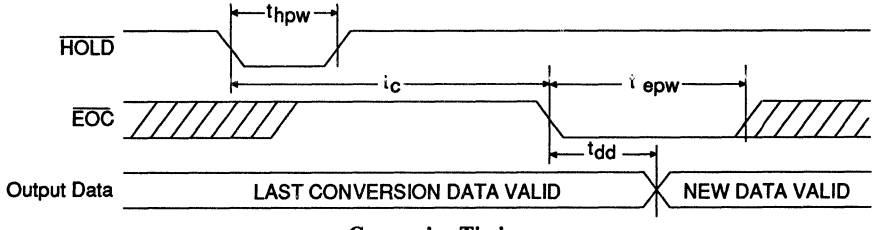
Rise and Fall Times



Serial Output Timing



Read and Calibration Control Timing



Conversion Timing

6

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%)

All measurements below are performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 14)	V_{OH}	VD+ - 1.0V	-	-	V
Low-Level Output Voltage Iout=1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	10	uA
3-State Leakage Current	I_{OZ}	-	-	±10	uA
Digital Output Pin Capacitance	C_{out}	-	9	-	pF

Note: 14. I_{out} = -100µA. This specification guarantees TTL compatability (VOH = 2.4V @ I_{out} = -40µA).

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see note 15.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.5	5.0	VA+	V
	Negative Digital	VD-	−4.5	−5.0	−5.5	V
	Positive Analog	VA+	4.5	5.0	5.5	V
	Negative Analog	VA-	−4.5	−5.0	−5.5	V
Analog Reference Voltage		VREF	2.5	4.5	VA+ - 0.5	V
Analog Input Voltage:	Unipolar	V_{AIN}	AGND	-	VREF	V
(Note 16)	Bipolar	V_{AIN}	-VREF	-	VREF	V

Notes: 15. All voltages with respect to ground.

16. The CS5016 can accept input voltages up to the analog supplies (VA+ and VA-). It will output all 1's for inputs above VREF and all 0's for inputs below AGND in unipolar mode and -VREF in bipolar mode.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	−0.3	VA+ + 0.3	V
	Negative Digital	VD-	0.3	−6.0	V
	Positive Analog	VA+	−0.3	6.0	V
	Negative Analog	VA-	0.3	−6.0	V
Input Current, Any Pin Except Supplies (Note 17)		I_{in}	-	±10	mA
Analog Input Voltage (AIN and VREF pins)		V_{INA}	VA- - 0.3	VA+ + 0.3	V
Digital Input Voltage		V_{IND}	-0.3	VA+ + 0.3	V
Ambient Operating Temperature		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

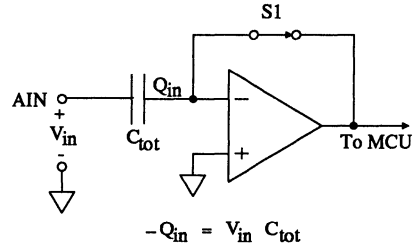
Note: 17. Transient currents of up to 100mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guarateed at these extremes.

THEORY OF OPERATION

The CS5016 utilizes the most popular method of executing high-speed, high-resolution A/D conversion: successive approximation. As with all other iterative comparison methods, the analog input is successively compared to the output of a D/A converter controlled by the conversion algorithm. Successive approximation begins by comparing the analog input to the DAC output which is set to half-scale (MSB on, all other bits off). If the input is found to be below half-scale, the MSB is reset to zero and the input is compared to one-quarter scale (next MSB on, all others off). If the input were above half-scale, the MSB would remain high and the next comparison would be at three-quarters of full scale. This procedure continues until all bits have been exercised.

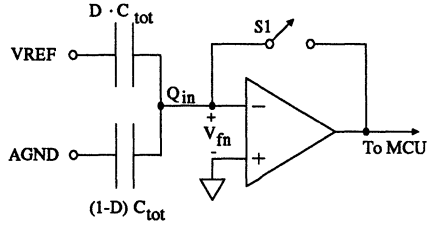
The CS5016 implements the successive-approximation algorithm using a unique charge redistribution architecture. Instead of the traditional resistor network, the DAC is an array of binary-weighted capacitors. All capacitors in the array share a common node at the comparator's input. Their other terminals are capable of being connected to AIN, AGND, or VREF (Figure 1). When the device is not calibrating or converting, all capacitors are tied to AIN forming C_{tot}. Switch S1 is closed and the charge on the array, Q_{in}, tracks the input signal V_{in} (Figure 2a).



$-Q_{in} = V_{in}\ C_{tot}$

Figure 2a. Tracking Mode

When the conversion command is issued, switch S1 opens as shown in Figure 2b. This traps charge Q_{in} on the comparator side of the capacitor array and creates a floating node at the comparator's input. The conversion algorithm operates on this fixed charge, and the signal at the analog input pin is ignored. In effect, the entire DAC capacitor array serves as analog memory during conversion much like a hold capacitor in a sample/hold amplifier.



$$D = \frac{V_{in}}{VREF} \text{ for } V_{fn} = 0V$$

Figure 2b. Convert Mode

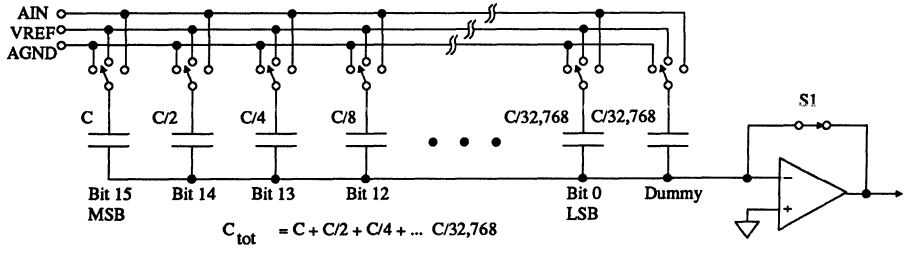


Figure 1. Charge Redistribution DAC

The conversion consists of manipulating the free plates of the capacitor array to VREF and AGND to form a capacitive divider. Since the charge at the floating node remains fixed, the voltage at that point depends on the proportion of capacitance tied to VREF versus AGND. The successive-approximation algorithm is used to find the proportion of capacitance, termed D in Figure 2b, which when connected to the reference will drive the voltage at the floating node (V_{fn}) to zero. That binary fraction of capacitance represents the converter's digital output.

The CS5016's charge redistribution architecture easily supports bipolar input ranges. If half the capacitor array (the MSB capacitor) is tied to VREF rather than AIN in the track mode, the input range is doubled and is offset half-scale. The magnitude of the reference voltage thus defines both positive and negative full-scale (-VREF to +VREF), and the digital code is an offset binary representation of the input.

Calibration

The ability of the CS5016 to convert accurately to 16-bits clearly depends on the accuracy of its comparator and DAC. The CS5016 utilizes an "auto-zeroing" scheme to null errors introduced by the comparator. All offsets are stored on the capacitor array while in the track mode and are effectively subtracted from the input signal when a conversion is initiated. Auto-zeroing enhances power supply rejection at frequencies well below the conversion rate.

To achieve 16-bit accuracy from the DAC, the CS5016 uses a novel self-calibration scheme. Each bit capacitor shown in Figure 1 actually consists of several capacitors which can be manipulated to adjust the overall bit weight. An on-chip microcontroller adjusts the subarrays to precisely ratio the bits. Each bit is adjusted to just balance the sum of all less significant bits plus one dummy LSB (for example, 16C = 8C + 4C + 2C + C + C). During calibration, the CS5016 implements statistical noise reduction to calibrate accurately to ± 1/4 LSB. It performs multiple experiments per calibration decision to reduce the effective noise bandwidth and the probability of making an incorrect decision. The resulting probability of obtaining a 1/4 LSB error is less than one in a thousand, with a negligible chance of obtaining a calibration error of 1/2 LSB.

DIGITAL CIRCUIT CONNECTIONS

The CS5016 can be applied in a wide variety of master clock, sampling, and calibration conditions which directly affect the device's conversion time and throughput. The device also features on-chip 3-state output buffers and a complete interface for connecting to 8-bit and 16-bit digital systems. Output data is also available in serial format.

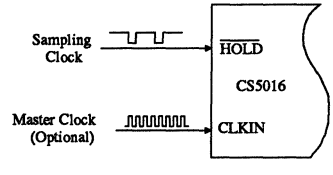


Figure 3a. Asynchronous Sampling

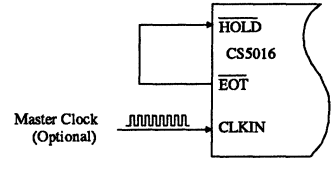


Figure 3b. Synchronous Sampling

Master Clock

The CS5016 operates from a master clock which can be externally supplied or internally generated. The internal oscillator is activated by externally tying the CLKIN input low. Alternatively, the CS5016 can be synchronized to the external system by driving the CLKIN pin with a TTL or CMOS clock signal.

All calibration, conversion, and throughput times directly scale to master clock frequency. Thus, throughput can be precisely controlled and/or maximized using an external master clock. In contrast, the CS5016's internal oscillator will vary from unit-to-unit and over temperature. Its tolerance gives rise to minimum and maximum conversion times and throughput rates. The -16 version of the CS5016 is specified for accurate operation with an external clock up to 4MHz; its internal clock frequency is specified at a minimum of 2MHz. The -32 version can handle external clocks up to 2MHz; its internal clock can range as low as 1MHz (see *Switching Characteristics*, page 62). Both versions can typically convert with clocks as low as 10kHz at room temperature.

Initiating Conversions

A falling transition on the $\overline{\text{HOLD}}$ pin places the input in the hold mode and initiates a conversion cycle. The $\overline{\text{HOLD}}$ input is latched internally by the master clock, so it can return high anytime after one master clock cycle plus 50ns. Upon completion of the conversion cycle, the CS5016 automatically returns to the track mode. In contrast to systems with separate track-and-holds and A/D converters, a sampling clock can simply be connected to the $\overline{\text{HOLD}}$ input (Figure 3a). The duty cycle of this clock is not critical. It need only remain low at least one master clock cycle plus 50ns, but no longer than the minimum conversion time or an additional conversion cycle will be initiated with inadequate time for acquisition.

Microprocessor-Controlled Operation

Sampling and conversion can be placed under microprocessor control (Figure 4) by simply gating the device's decoded address with the write strobe for the $\overline{\text{HOLD}}$ input. Thus, a write cycle to the CS5016's base address will initiate a conversion (the data word is irrelevant). However, the write cycle must be to the odd address (A0 high) to avoid initiating a software controlled reset (see *Reset*, page 69).

The calibration control inputs, CAL, and $\overline{\text{INTRLV}}$ are also internally latched by $\overline{\text{CS}}$, so they must be in the appropriate state whenever the chip is selected during a read or write cycle. Address lines A1 and A2 are shown connected to CAL and $\overline{\text{INTRLV}}$ in Figure 4 placing calibration under microprocessor control as well. Thus, any read or write cycle to the CS5016's base address will initiate or terminate calibration.

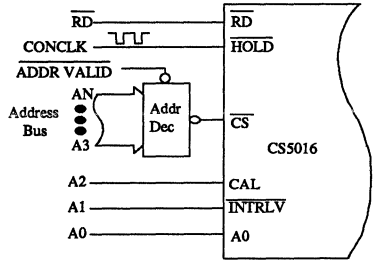


Figure 4a. Conversions Asynchronous to Master Clock

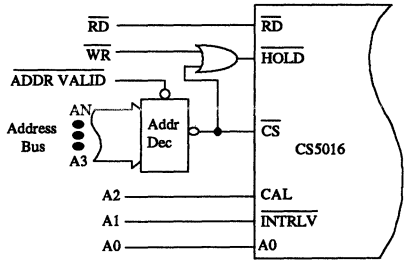


Figure 4b. Conversions under Microprocessor Control

Conversion Time/Throughput

Upon completing a conversion cycle and returning to the track mode, the CS5016 requires time to acquire the analog input signal before another conversion can be initiated. The acquisition time is specified as six master clock cycles plus 2.25µs. This adds to the conversion time to define the converter's maximum throughput. The conversion time of the CS5016, in turn, depends on the sampling, calibration, and master clock conditions.

Asynchronous Sampling

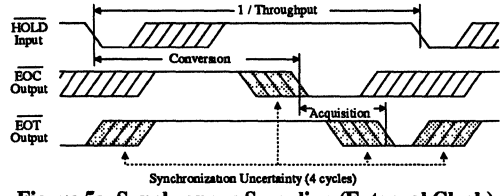


Figure 5a. Synchronous Sampling (External Clock)

The CS5016 internally operates from a clock which is delayed and divided down from the master clock ($f_{CLK}/4$). If sampling is not synchronized to this internal clock, the conversion cycle may not begin until up to four clock cycles after $\overline{HOLD}$ goes low *even though the charge is trapped immediately.* In this asynchronous mode (Figure 3a), the four clock cycles add to the minimum 65 clock cycles to define the maximum conversion time (see Figure 5a and Table 1).

Synchronous Sampling

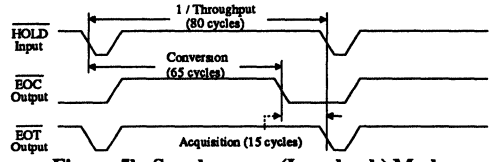


Figure 5b. Synchronous (Loopback) Mode

To achieve maximum throughput, sampling can be synchronized with the internal conversion clock by connecting the End-of-Track ($\overline{EOT}$) output to $\overline{HOLD}$ (Figure 3b). The $\overline{EOT}$ output falls 15 master clock cycles after $\overline{EOC}$ indicating the analog input has been acquired to the CS5016's specified accuracy. The $\overline{EOT}$ output is synchronized to the internal conversion clock, so the four clock cycle synchronization uncertainty is removed yielding throughput at 1/80th of the master clock frequency (see Figure 5b and Table 1).

Also, the CS5016's internal RC oscillator exhibits significant jitter (typically ± 0.05% of its period), which is high compared to crystal oscillators. If the CS5016 is configured for synchronous sampling while operating from its internal oscillator, this jitter will directly affect sampling purity.

The $\overline{EOT}$ output is an accurate indicator of the CS5016's acquisition requirement when operating at the -16 version's full rated speed (3.75µs with a 4MHz master clock). However, $\overline{EOT}$ will allow the CS5016 more acquisition time than

	Conversion Time		Throughput Time	
Sampling Mode	min	max	min	max
Synchronous (Loopback)	65T	65T	80T	80T
Asynchronous	65T	69T + 235ns	N/A	75T + 2.25µs

(T ≡ one master clock cycle)

Table 1. Conversion and Throughput Times

necessary when operating with a clock less than 4MHz. The $\overline{EOT}$ output always falls 15 master clock cycles after $\overline{EOC}$. The CS5016 only needs 3.75µs (six cycles @4MHz plus 2.25µs). When operating the -32 with a master clock of 2MHz or less, higher throughput can be achieved than in the loopback configuration by using an external counter. The counter should be reset by the falling edge of $\overline{EOC}$ and count the appropriate number of clock cycles after each conversion. When the total time is greater than six clock cycles plus 2.25µs the counter can trigger a new conversion at $\overline{HOLD}$. For example, when using a 2MHz clock, 2.25µs takes between four and five clock cycles. When six cycles are added to this it is seen that the counter should trigger a new conversion at the eleventh clock cycle.

Reset

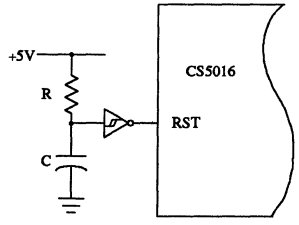


Figure 6. Power-On Reset Circuitry

Upon power up, the CS5016 must be reset to guarantee a consistent starting condition and initially calibrate the device. Due to the CS5016's low power dissipation and low temperature drift, no warm-up time is required before reset to accommodate any self-heating effects. However, the voltage reference input should have stabilized to within 0.25% of its final value before RST falls to guarantee an accurate calibration. Later, the CS5016 may be reset at any time to initiate a single full calibration. Reset overrides all other functions. If reset, the CS5016 will clear and initiate a new calibration cycle mid-conversion or mid-calibration.

Resets can be initiated in hardware or software. The simplest method of resetting the CS5016 involves strobing the RST pin high. When RST is brought high all internal logic clears. When it returns low a full calibration begins which takes 1,443,840 master clock cycles (approximately 360ms with a 4MHz clock) to complete. A simple power-on reset circuit can be built using a resistor and capacitor, and a Schmidt-trigger inverter to prevent oscillation (see Figure 6). The CS5016 can also be reset in software when under microprocessor control. The CS5016 will reset whenever $\overline{CS}$, A0, and $\overline{HOLD}$ are taken low simultaneously. See the *Microprocessor Interface* section on page 70 to eliminate the possibility of inadvertent software reset. The $\overline{EOC}$ output remains high throughout the reset operation and will fall upon its completion. It can thus be used to generate an interrupt indicating the CS5016 is ready for operation. Six master clock cycles plus 2.25µs must be allowed after $\overline{EOC}$ falls to allow for acquisition. Under microprocessor-independent operation with 3-states permanently enabled ($\overline{CS}$, $\overline{RD}$ low; A0 high) the $\overline{EOC}$ output will not fall at the completion of the reset operation.

Initiating Calibration

All modes of calibration can be controlled in hardware or software. Accuracy can thereby be insured at any time or temperature throughout operating life. After initial calibration at power-up, the CS5016's charge-redistribution design yields better temperature drift and more graceful aging than resistor-based technologies, so calibration is actually required less often than with traditional devices.

The first mode of calibration, reset, results in a single full calibration cycle. The second type of calibration, termed "burst" cal, is useful when the ADC sees some downtime but not enough to perform a full reset calibration. Burst cal can be terminated mid-calibration; it picks up where it left off previously, so calibrations can be done in

piecemeal fashion. Burst cal is initiated by bringing the CAL input high with $\overline{CS}$ low. The CAL input is level-triggered and latches on the rising edge of $\overline{CS}$, so a write cycle can be used to control calibration in software. Burst cal will continue to loop through calibration cycles until terminated. Once CAL returns low, at least 26 master clock cycles plus 2.25µs (8.75µs @ 4MHz clock) must be allowed before a conversion is initiated to ensure the CS5016 has completed its calibration experiment and has acquired the analog input. The $\overline{EOC}$ output indicates the completion of the final calibration experiment. (See note on page 85.)

The CS5016 features a background calibration mode called "interleave." Interleave appends a single calibration experiment to each conversion cycle and thus requires no dead time for calibration. The CS5016 gathers data between conversions and will adjust its transfer function once it completes the entire sequence of experiments (one calibration cycle per 72,192 conversions). Initiated by bringing both the $\overline{INTRLV}$ input and $\overline{CS}$ low (or hard-wiring $\overline{INTRLV}$ low), interleave extends the CS5016's effective conversion time by 20 master clock cycles (5µs @ 4MHz). Other than reduced throughput, interleave is totally transparent to the user.

Burst calibrations initiated at CAL pick up where interleave left off, so calibration cycles can be hastened by "bursting" a number of experiments whenever the CS5016 sees free time. Interleave is subordinate to burst calibrations, so $\overline{INTRLV}$ could still be externally tied low.

Microprocessor Interface

The CS5016 features an intelligent microprocessor interface which offers detailed status information and allows software control of the self-calibration functions. Output data is available in either 8-bit or 16-bit formats for easy interfacing to industry-standard microprocessors.

Strobing both $\overline{CS}$ and $\overline{RD}$ low enables the CS5016's 3-state output buffers with either output data or status information depending on the status of A0. An address bit can be connected to A0 as shown in Figure 4b thereby memory mapping the status register and output data. Conversion status can be polled in software by reading the status register ($\overline{CS}$ and $\overline{RD}$ strobed low with A0 low), and masking status bits S0-S5 and S7 (by logically AND'ing the status word with 01000000) to determine the value of S6. Similarly, the software routine can determine calibration status using other status bits (see Table 2). *Care must be taken not to read the status register (A0 low) while $\overline{HOLD}$ is low, or a software reset will result* (see *Reset*, page 69).

PIN	STATUS BIT	STATUS	DEFINITION
D0	S0	$\overline{END\ OF\ CONVERSION}$	Falls upon completion of a conversion, and returns high on the first subsequent read.
D1	S1	RESERVED	Reserved for factory use.
D2	S2	LOW BYTE/$\overline{HIGH\ BYTE}$	When data is to be read in an 8-bit format (BW=0), indicates which byte will appear at the output next.
D3	S3	$\overline{END\ OF\ TRACK}$	When low, indicates the input has been acquired to the devices specified accuracy.
D4	S4	RESERVED	Reserved for factory use.
D5	S5	TRACKING	High when the device is tracking the intput.
D6	S6	CONVERTING	High when the device is converting the held input.
D7	S7	CALIBRATING	High when the device is calibrating.

Table 2. Status Bit Definitions

Alternatively, the End-of-Convert ($\overline{EOC}$) output can be used to generate an interrupt or drive a DMA controller to dump the output directly into memory after each conversion. The $\overline{EOC}$ pin falls as each conversion cycle is completed and data is valid at the output. It returns high within four master clock cycles of the first subsequent data read operation or after the start of a new conversion cycle.

To interface with 16-bit a data bus, the BW input to the CS5016 should be held high and all 16 data bits read in parallel on pins D15-D0. With an 8-bit bus, the converter's 16-bit result must be read in two portions. In this instance, BW should be held low and the 8 MSB's obtained on the first read cycle following a conversion. The second read cycle will yield the 8 LSB's. Both bytes appear on pins D0-D7. The upper/lower bytes of the same data will continue to toggle on subsequent reads until the next conversion finishes. Status bit S2 indicates which byte will appear on the next data read operation.

The CS5016 internally buffers its output data, so data can be read while the device is tracking or converting the next sample. Therefore, retrieving the converter's digital output requires no reduction in ADC throughput. Enabling the 3-state outputs while the CS5016 is converting will not introduce conversion errors. When TTL loads are utilized the potential for crosstalk between digital and analog sections of the system is increased. This crosstalk is due to high digital supply and signal currents arising from the TTL drive current required of each digital output. Connecting CMOS logic to the digital outputs is recommended. Suitable logic families include 4000B, 74HC, 74AC, 74ACT, and 74HCT.

The two calibration control inputs, CAL and $\overline{INTRLV}$, are level-triggered and latched on the rising edge of $\overline{CS}$. Calibration can be placed under software control by connecting address lines to the CAL and $\overline{INTRLV}$ inputs as shown in Figure 4a. Any read or write cycle to the CS5016's base address will thereby initiate or terminate calibration.

Microprocessor Independent Operation

The CS5016 can be operated in a stand-alone mode independent of intelligent control. In this mode, $\overline{CS}$ and $\overline{RD}$ are hard-wired low permanently enabling the 3-state output buffers. A free-running condition is established when BW is tied high, CAL is tied low, and $\overline{HOLD}$ is continually strobed low or tied to $\overline{EOT}$. The CS5016's $\overline{EOC}$ output can be used to externally latch the output data if desired. With $\overline{CS}$ and $\overline{RD}$ hard-wired low, $\overline{EOC}$ will strobe low for four

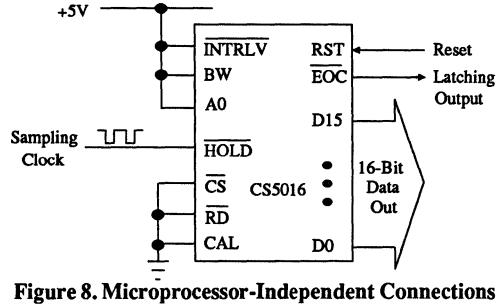


Figure 8. Microprocessor-Independent Connections

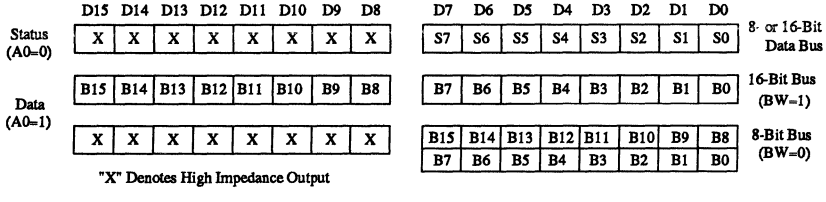


Figure 7. Data Format

master clock cycles after each conversion. Data will be unstable up to 100ns after $\overline{EOC}$ falls, so it should be latched on the rising edge of $\overline{EOC}$.

Serial Output

All successive-approximation A/D converters derive their digital output serially starting with the MSB. The CS5016 presents each bit to the SDATA pin four master clock cycles after it is derived and can be latched using the serial clock output, SCLK. Just subsequent to each bit decision SCLK will fall and return high once the bit information on SDATA has stabilized. Thus, the rising edge of the SCLK output should be used to clock the data from the CS5016 (See Figure 9).

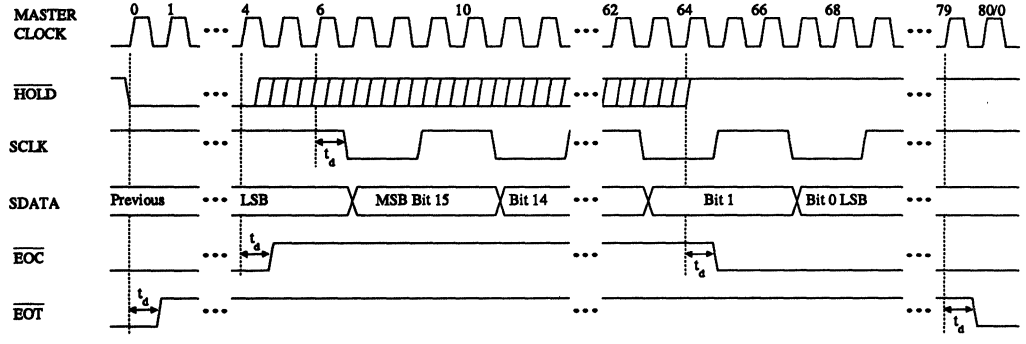
ANALOG CIRCUIT CONNECTIONS

Most popular successive-approximation A/D converters generate dynamic loads at their analog connections. The CS5016 internally buffers all analog inputs (AIN, VREF, and AGND) to ease the demands placed on external circuitry. However, accurate system operation still requires careful attention to details at the design stage regarding source impedances as well as grounding and decoupling schemes.

Reference Considerations

An application note titled "*Voltage References for the CS501X/CSZ511X Series of A/D Converters*" is available for the CS5016. In addition to working through a reference circuit design example, it offers seven built-and-tested reference circuits.

During conversion, each capacitor of the calibrated capacitor array is switched between VREF and AGND in a manner determined by the successive-approximation algorithm. The charging and discharging of the array results in a current load at the reference. The CS5016 includes an internal buffer amplifier to minimize the external reference circuit's drive requirement and preserve the reference's integrity. Whenever the array is switched during conversion, the buffer is used to pre-charge the array thereby providing the bulk of the necessary charge. The appropriate array capacitors are then switched to the unbuffered VREF pin to avoid any errors due to offsets and/or noise in the buffer.



Notes: 1. t_d can vary from 135ns to 235ns over military temperature range and over ± 10% supply variation.
2. For asynchronous mode, transitions of SLCK, SDATA, $\overline{EOC}$, $\overline{EOT}$ can shift by up to 4 clocks; e.g. the first high to low transition of SCLK may be on clock #6 to #9. The timing relationship between SLCK, SDATA, $\overline{EOC}$, and $\overline{EOT}$ is fixed.

Figure 9. Serial Output Timing

The external reference circuitry need only provide the residual charge required to fully charge the array after pre-charging from the buffer. This creates an ac current load as the CS5016 sequences through conversions. The reference circuitry must have a low enough output impedance to drive the requisite current without changing its output voltage significantly. As the analog input signal varies, the switching sequence of the internal capacitor array changes. The current load on the external reference circuitry thus varies in response with the analog input. Therefore, the external reference must not exhibit significant peaking in its output impedance characteristic at signal frequencies or their harmonics.

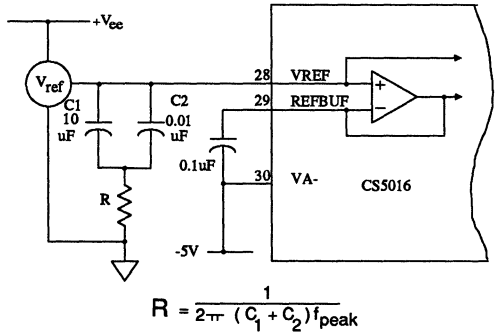


Figure 10. Reference Connections

A large capacitor connected between VREF and AGND can provide sufficiently low output impedance at the high end of the frequency spectrum, while almost all precision references exhibit extremely low output impedance at dc. The presence of large capacitors on the output of some voltage references, however, may cause peaking in the output impedance at intermediate frequencies. Care should be exercised to ensure that significant peaking does not exist or that some form of compensation is provided to eliminate the effect.

The magnitude of the current load on the external reference circuitry will scale to the master clock frequency. At full speed (4MHz clock), the reference must supply a maximum load current of 10µA peak-to-peak (1µA typical). An output impedance of 2Ω will therefore yield a maximum error of 20µV. With a 4.5V reference and LSB size of 69µV, this would insure approximately 1/4 LSB accuracy. A 10µF capacitor exhibits an impedance of less than 2Ω at frequencies greater than 16kHz. A high-quality tantalum capacitor in parallel with a smaller ceramic capacitor is recommended.

Peaking in the reference's output impedance can occur because of capacitive loading at its output. Any peaking that might occur can be reduced by placing a small resistor in series with the capacitors (Figure 10). The equation in Figure 10 can be used to help calculate the optimum value of R for a particular reference. The term "f_{peak}" is the frequency of the peak in the output impedance of the reference before the resistor is added.

The CS5016 can operate with a wide range of reference voltages, but signal-to-noise performance is maximized by using as wide a signal range as possible. The recommended reference voltage is 4.5 volts. The CS5016 can actually accept reference voltages up to the positive analog supply. However, the buffer's offset may increase as the reference voltage approaches VA+ thereby increasing external drive requirements at VREF. A 4.5V reference is the maximum reference voltage recommended. This allows 0.5V headroom for the internal reference buffer. Also, the buffer enlists the aid of an external 0.1µF ceramic capacitor which must be tied between its output, REFBUF, and the negative analog supply, VA-. For more information on references, consult "Application Note: *Voltage References for the CS501X/CSZ511X Series of A/D Converters*".

Analog Input Connection

The analog input terminal functions similarly to the VREF input after each conversion when

switching into the track mode. During the first six master clock cycles in the track mode, the buffered version of the analog input is used for pre-charging the capacitor array. An additional period is required for fine-charging directly from AIN to obtain the specified accuracy. Figure 11 exemplifies this operation. During pre-charge the charge on the capacitor array first settles to the buffered version of the analog input. This voltage is offset from the actual input voltage. During fine-charge, the charge then settles to the accurate unbuffered version.

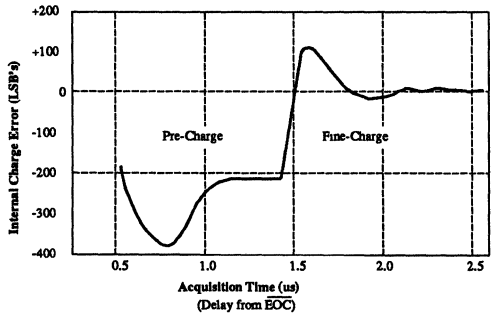


Figure 11. Internal Acquisition Time

The acquisition time of the CS5016 depends on the master clock frequency. This is due to a fixed pre-charge period. For instance, operating the -16 version with an external 4MHz master clock results in a 3.75µs acquisition time: 1.5µs for pre-charging (6 clock cycles) and 2.25µs for fine-charging. Fine-charge settling is specified as a maximum of 2.25µs for an analog source impedance of less than 200Ω. In addition, the comparator requires a source impedance of less than 400Ω around 2MHz for stability, which is met by practically all bipolar op amps. Large dc source impedances can be accommodated by adding capacitance from AIN to ground (typically 200pF) to decrease source impedance at high frequencies. However, high dc source resistances will increase the input's RC time constant and extend the necessary acquisition time.

The CS5016 can track full power signals up to 25kHz in the track mode. During the first six clock cycles following a conversion (pre-charge), the CS5016 is capable of slewing at 5V/µs in unipolar mode. In bipolar mode, only half the capacitor array is connected to the analog input so the CS5016 can slew at 10V/µs. After the first six master clock cycles, it will slew at 0.25V/µs in the unipolar mode and 0.5V/µs in bipolar mode. Acquisition of fast slewing signals (step functions) can be hastened if the step occurs during or immediately following the conversion cycle. For instance, channel selection in multiplexed applications should occur while the CS5016 is converting (see Figure 12). Multiplexer settling is thereby

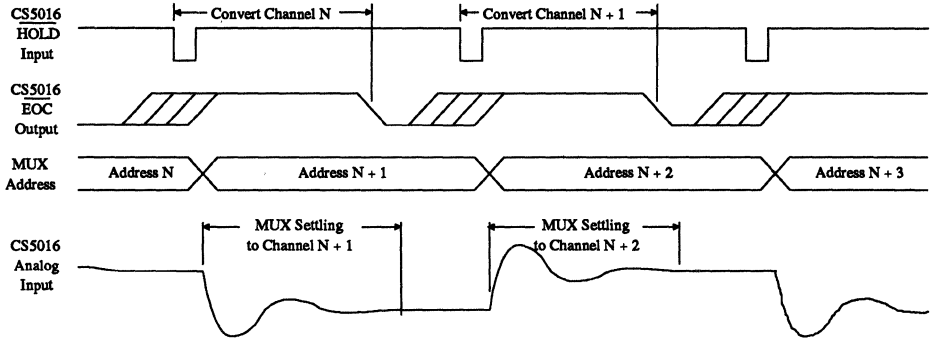


Figure 12. Pipelined MUX Input Channels

removed from the overall throughput equation, and the CS5016 can convert at full speed.

Analog Input Range/Coding Format

The reference voltage directly defines the input voltage range in both the unipolar and bipolar configurations. In the unipolar configuration (BP/$\overline{UP}$ low), the first code transition occurs 0.5 LSB above AGND, and the final code transition occurs 1.5 LSB's below VREF. Coding is in straight binary format. In the bipolar configuration (BP/$\overline{UP}$ high), the first code transition occurs 0.5 LSB above -VREF and the last transition occurs 1.5 LSB's below +VREF. Coding is in an offset-binary format. Positive full scale gives a digital output of 1111111111111111, and negative full scale gives a digital output of 0000000000000000.

Grounding and Power Supply Decoupling

The CS5016 uses the analog ground connection, AGND, only as a reference voltage. No dc power currents flow through the AGND connection, and it is completely independent of DGND. However, any noise riding on the AGND input relative to the system's analog ground will induce conversion errors. Therefore, both the analog input and reference voltage should be referred to the AGND pin, which should be used as the entire system's analog ground.

The digital and analog supplies are isolated within the CS5016 and are pinned out separately to minimize coupling between the analog and digital sections of the chip. All four supplies should be decoupled to their respective grounds using 0.1µF ceramic capacitors. If significant low-frequency noise is present on the supplies, 1µF tantalum capacitors are recommended in parallel with the 0.1µF capacitors.

The positive digital power supply of the CS5016 must never exceed the positive analog supply by more than a diode drop or the CS5016 could experience permanent damage. If the two supplies are derived from separate sources, care must be taken that the analog supply comes up first at power-up. The system connection diagram on page 79 shows a decoupling scheme which allows the CS5016 to be powered from a single set of ± 5V rails. The positive digital supply is derived from the analog supply through a 10Ω resistor to avoid the analog supply dropping below the digital supply. If this scheme is utilized, care must be taken to insure that any digital load currents (which flow through the 10Ω resistors) do not cause the magnitude of digital supplies to drop below the analog supplies by more than 0.5 volts. Digital supplies must always remain above the minimum specification.

As with any high-precision A/D converter, the CS5016 requires careful attention to grounding and layout arrangements. However, no unique layout issues must be addressed to properly apply the CS5016. The CDB5016 evaluation board is available for the CS5016, which avoids the need to design, build, and debug a high-precision PC board to initially characterize the part. The board comes with a socketed CS5016, and can be quickly reconfigured to simulate any combination of sampling, calibration, master clock, and analog input range conditions.

6

CS5016 PERFORMANCE

Differential Nonlinearity

The most prevalent source of nonlinearity in high resolution converters is bit weight errors. These errors arise from the deviation of bits from their ideal binary-weighted ratios, and lead to nonideal widths for each code. If DNL errors are large, and code widths shrink to zero, it is possible for one or more codes to be entirely missing. The CS5016 calibrates all bits in the capacitor array to ± 1/4 LSB resulting in nearly ideal DNL. A histogram plot of typical DNL can be seen in Figure 13.

A histogram test is a statistical method of deriving an A/D converter's differential nonlinearity. A ramp is input to the A/D and a large number of samples are taken to insure a high confidence level in the test's result. The number of occurrences for each code is monitored and stored. A perfect A/D converter would have all codes of equal size and therefore equal numbers of occurrences. In the histogram test a code with the average number of occurrences will be considered ideal (DNL = 0). A code with more or less occurrences than average will appear as a DNL of greater or less than zero LSB. A missing code has zero occurrences, and will appear as a DNL of -1 LSB.

Integral Nonlinearity

Integral nonlinearity is defined as the deviation of the transfer function from an ideal straight line through zero and full scale. Even if differential linearity errors are small, they may combine to produce a gross INL error at some point in the transfer function. A unique calibration algorithm, a lack of superposition of errors due to a capacitor based DAC, and low capacitor voltage coefficient keep INL errors below 0.0015% of full scale.

Noise

An A/D converter's noise can be described like that of any other analog component. However, the converter's output is in digital form so any filtering of its noise must be performed in the digital domain. Digitized samples of analog inputs are often considered individual, static snap-shots in time with no uncertainty or noise. In reality, the result of each conversion depends on the analog input level and the instantaneous value of noise sources in the ADC. If sequential samples from the ADC are treated as a "waveform", simple filtering can be implemented in software to improve noise performance with minimal processing overhead.

All analog circuitry in the CS5016 is wideband in order to achieve fast conversions and high throughput. Wideband noise in the CS5016 integrates to 35μV rms in unipolar mode (70μV rms in bipolar mode). This is approximately 1/2 LSB rms with a 4.5V reference in both modes. Figure 14 shows a histogram plot of output code occurrences obtained from 5000 samples taken from a CS5016 in the bipolar mode. Hexadecimal code 80CD was arbitrarily selected and the analog input was set close to code center. With a noiseless converter, code 80CD would always appear. The histogram plot of the CS5016 has a "bell" shape with all codes other than 80CD due to internal noise.

In a sampled data system all information about the analog input applied to the sample/hold appears in the baseband from dc to one-half the sampling rate. This includes high-frequency components which alias into the baseband. Low-pass (anti-alias) filters are therefore used to remove frequency components in the input signal which are above one-half the sample rate.

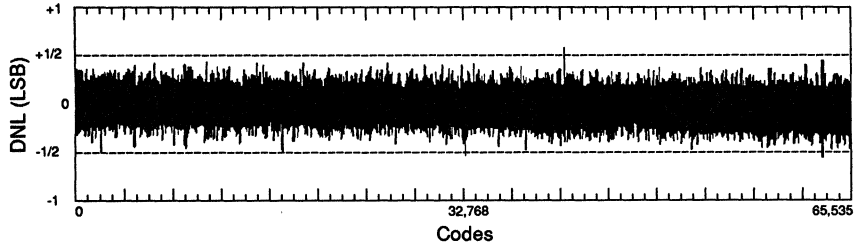


Figure 13. CS5016 Differential Nonlinearity Plot

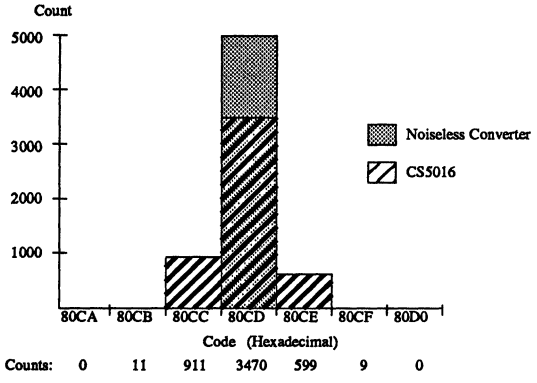


Figure 14. Histogram Plot of 5000 Conversion Inputs

However, all wideband noise introduced by the CS5016 still aliases into the baseband. This "white" noise is evenly spread from dc to one-half the sampling rate and integrates to 35μV rms in unipolar mode.

Noise in the digital domain can be reduced by sampling at higher than the desired word rate and averaging multiple samples for each word. Oversampling spreads the CS5016's noise over a wider band (for lower noise density), and averaging applies a low-pass response which filters noise above the desired signal bandwidth. In general, the CS5016's noise performance can be maximized in any application by always sampling at the maximum specified rate of 50kHz (for lowest noise density) and digitally filtering to the desired signal bandwidth.

More sophisticated bandlimiting filters other than averaging can be implemented in software for better roll-off and noise improvement. One example of an FIR (Finite Impulse Response) filter is effectively a rolling, weighted average of sequential samples. Such filters can be implemented with very little processing overhead, or alternatively, dedicated DSP chips can be used to implement all system filtering. Digital filters offer the benefits of ideal accuracy and stable, repeatable response independent of time and environmental conditions.

Clock Feedthrough

Maintaining the integrity of analog signals in the presence of digital switching noise is a difficult problem. The CS5016 can be synchronized to the digital system using the CLKIN input to avoid conversion errors due to asynchronous interference. However, digital interference will still affect sampling purity due to coupling between the CS5016's analog input and master clock.

The effect of clock feedthrough depends on the sampling conditions. If the sampling signal at the $\overline{\text{HOLD}}$ input is synchronized to the master clock, clock feedthrough will appear as a dc offset at the CS5016's output. The offset could theoretically reach the peak coupling magnitude (Figure 15), but the probability of this occurring is small since the peaks are spikes of short duration.

Master Clock		Analog Input	Clock Feedthrough	
Int/Ext	Freq	Source Impedance	RMS	Peak-to-Peak
Internal	2MHz	50 Ω	15uV	70uV
External	2MHz	50 Ω	25uV	110uV
External	4MHz	50 Ω	40uV	150uV
External	4MHz	25 Ω	25uV	110uV
External	4MHz	200 Ω	80uV	325uV

Figure 15. Examples of Measured Clock Feedthrough

If sampling is performed asynchronously with the master clock, clock feedthrough will appear as an ac error at the CS5016's output. With a fixed sampling rate, a tone will appear as the clock frequency aliases into the baseband. The tone frequency can be calculated using the equation below and could be selectively filtered in software using DSP techniques.

$$f_{tone} = (N f_s - f_{clk})$$

where $N = f_{clk}/f_s$ rounded to the nearest integer

The magnitude of clock feedthrough depends on the master clock conditions and the source impedance applied to the analog input. When

operating with the CS5016's internally generated clock, the CLKIN input is grounded and the dominant source of coupling is through the device's substrate. As shown in Figure 15, a typical CS5016 operating with its internal oscillator at 2MHz and 50Ω of analog input source impedance will exhibit only 15μV rms of clock feedthrough. However, if a 2MHz external clock is applied to CLKIN under the same conditions, feedthrough increases to 25μV rms. Feedthrough also increases with clock frequency; a 4MHz clock yields 40μV rms.

Clock feedthrough can be reduced by limiting the source impedance applied at the analog input. As shown in Figure 15, reducing source impedance from 50Ω to 25Ω yields a 15μV rms reduction in feedthrough. Therefore, when operating the CS5016 with high-frequency external master clocks, it is important to minimize source impedance applied to the CS5016's input.

Also, the overall effect of clock feedthrough can be minimized by maximizing the input range and LSB size. The reference voltage applied to VREF can be maximized, and the CS5016 can be operated in bipolar mode which inherently doubles the LSB size over the unipolar mode.

Power Supply Rejection

The CS5016's power supply rejection performance is enhanced by the on-chip self-calibration and an "auto-zero" process. Drifts in power supply voltages at frequencies less than the calibration rate have negligible effect on the CS5016's accuracy. This, of course, is because the CS5016 adjusts its offset to within a small fraction of an LSB during calibration. Above the calibration frequency the excellent power supply rejection of the internal amplifiers is augmented by an auto-zero process. Any offsets are stored on the capacitor array and are effectively subtracted once conversion is initiated. Figure 16 shows power supply rejection of the CS5016 in the bipolar mode with the analog input grounded and a 300mV p-p ripple applied to each supply. Power supply rejection improves by 6dB in the unipolar mode.

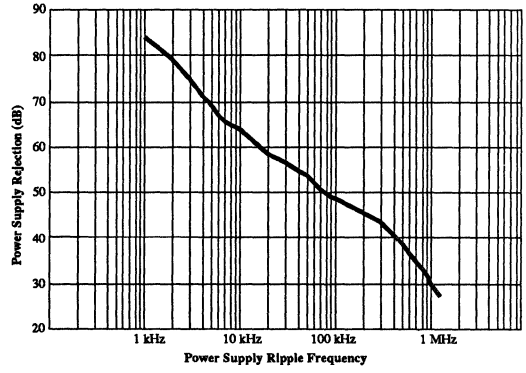


Figure 16. Power Supply Rejection

Notches of increased rejection arise from the auto-zeroing at the conversion rate. The frequencies at which these notches occur also depend on the value of the captured analog input. The line shows worst-case rejection for all combinations of conversion rates and input conditions in the bipolar mode. Again, power supply rejection is 6dB better in the unipolar mode.

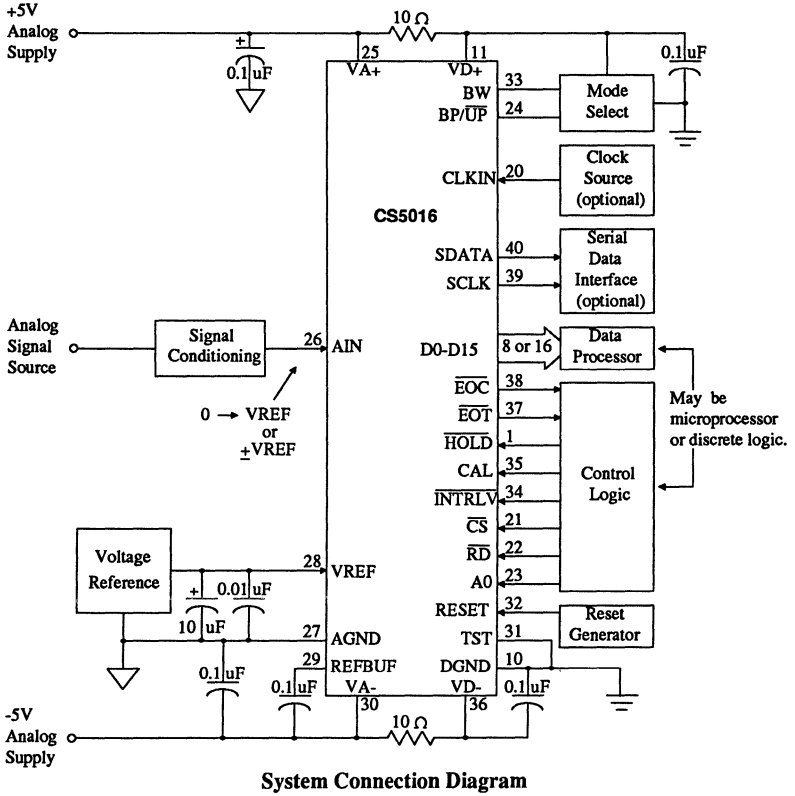
Aperture Jitter

Track-and-hold amplifiers commonly exhibit two types of aperture jitter. The first, more appropriately termed "aperture window", is an input voltage dependent variation in the aperture delay. Its signal-dependency causes distortion at high frequencies. The CS5016's proprietary architecture avoids applying the input voltage across a sampling switch, thus avoiding any "aperture window" effects. The second type of aperture jitter, due to component noise, assumes a random nature. With only 100ps peak-to-peak aperture jitter, the CS5016 can process full-scale signals up to 1/2 the throughput frequency without any errors due to aperture jitter.

$\overline{HOLD}$	$\overline{CS}$	CAL	$\overline{INTRLV}$	$\overline{RD}$	A0	RST	Function
↓	X	X	X	X	*	0	Hold and Start Convert
X	0	1	X	X	*	0	Initiate Burst Calibration
1	0	0	X	X	*	0	Stop Burst Cal and Begin Track
X	0	X	0	X	*	0	Initiate Interleave Calibration
X	0	X	1	X	*	0	Terminate Interleave Cal
X	0	X	X	0	1	0	Read Output Data
1	0	X	X	0	0	0	Read Status Register
X	1	X	X	X	*	X	High Impedance Data Bus
X	X	X	X	1	*	X	High Impedance Data Bus
X	X	X	X	X	X	1	Reset
0	0	X	X	X	0	X	Reset

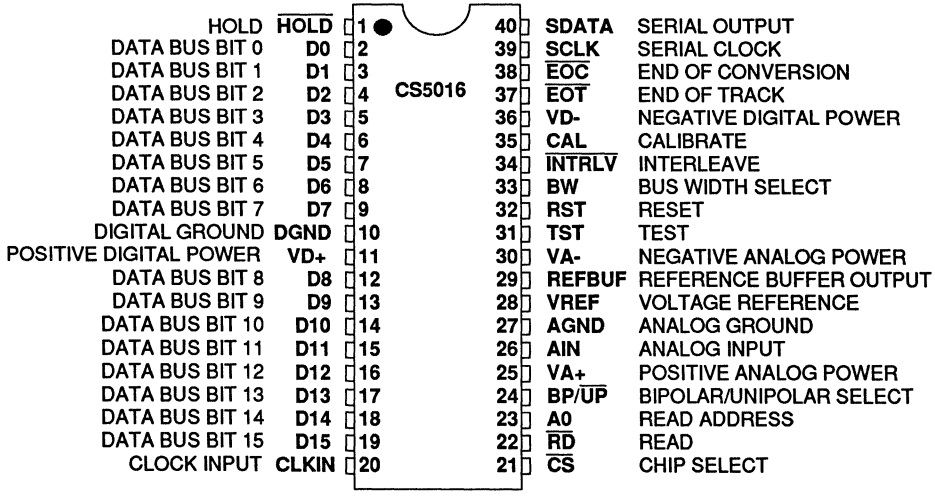
* The status of A0 is not critical to the operation specified. However, A0 should not be low with $\overline{CS}$ and $\overline{HOLD}$ low, or a software reset will result.

CS5016 Truth Table



System Connection Diagram

PIN DESCRIPTIONS



Power Supply Connections

VD+ - Positive Digital Power, PIN 11.
Positive digital power supply. Nominally +5 volts.

VD- - Negative Digital Power, PIN 36.
Negative digital power supply. Nominally -5 volts.

DGND - Digital Ground, PIN 10.
Digital ground reference.

VA+ - Positive Analog Power, PIN 25.
Positive analog power supply. Nominally +5 volts.

VA- - Negative Analog Power, PIN 30.
Negative analog power supply. Nominally -5 volts.

AGND - Analog Ground, PIN 27.
Analog ground reference.

Oscillator

CLKIN - Clock Input, PIN 20.

All conversions and calibrations are timed from a master clock which can either be supplied by driving this pin with an external clock signal, or can be internally generated by tying this pin to DGND.

Digital Inputs

$\overline{\text{HOLD}}$ - Hold, PIN 1.

A falling transition on this pin sets the CS5016 to the hold state and initiates a conversion. This input must remain low at least one master clock cycle plus 50ns.

$\overline{\text{CS}}$ - Chip Select, PIN 21.

When high, the data bus outputs are held in a high impedance state and the input to CAL and $\overline{\text{INTRLV}}$ are ignored. A falling transition initiates or terminates burst or interleave calibration (depending on the status of CAL and $\overline{\text{INTRLV}}$) and a rising transition latches both the CAL and $\overline{\text{INTRLV}}$ inputs. If $\overline{\text{RD}}$ is low, the data bus is driven as indicated by BW and A0.

$\overline{\text{RD}}$ - Read, PIN 22.

When $\overline{\text{RD}}$ and $\overline{\text{CS}}$ are both low, data is driven onto the data bus. If either signal is high, the data bus outputs are held in a high impedance state. The data driven onto the bus is determined by BW and A0.

A0 - Read Address, PIN 23.

Determines whether data or status information is placed onto the data bus. When high during the read operation, converted data is placed onto the data bus; when low, the status register is driven onto the bus.

BP/$\overline{\text{UP}}$ - Bipolar/Unipolar Input Select, PIN 24.

When high, the device is configured with a bipolar transfer function ranging from -VREF to +VREF. Encoding is in an offset binary format, with the mid-scale code 100...0000 centered at AGND. When low, the device is configured for a unipolar transfer function from AGND to VREF. Unipolar encoding is in straight binary format.

RST - Reset, PIN 32.

When taken high, all internal digital logic is reset. Upon being taken low, a full calibration sequence is initiated.

BW - Bus Width Select, PIN 33.

When hard-wired high, all 16 data bits are driven onto the bus simultaneously during a data read cycle. When low, the bus is in a byte wide format. On the first read following a conversion, the eight MSB's are driven onto D7-D0. A second read cycle places the eight LSB's on D7-D0. Subsequent reads will toggle the higher/lower order byte. Regardless of BW's status, a read cycle with A0 low yields the status information on D7-D0.

$\overline{\text{INTRLV}}$ - Interleave, PIN 34.

When latched low using $\overline{\text{CS}}$, the device goes into interleave calibration mode. A full calibration will complete every 79,192 conversions. The effective conversion time extends by 20 clock cycles.

CAL - Calibrate, PIN 35. (See note on page 85.)

When latched high using $\overline{\text{CS}}$, burst calibration results. The device cannot perform conversions during the calibration period which will terminate only once CAL is latched low again. Calibration picks up where the previous calibration left off, and calibration cycles complete every 1,443,840 master clock cycles. If the device is converting when a calibration is signaled, it will wait until that conversion completes before beginning.

Analog Inputs

AIN - Analog Input, PIN 26.

Input range in the unipolar mode is zero volts to VREF. Input range in bipolar mode is -VREF to +VREF. The output impedence of buffer driving this input should be less than or equal to 200Ω.

VREF - Voltage Reference, PIN 28.

The analog reference voltage which sets the analog input range. It represents positive full scale for both bipolar and unipolar operation, and its magnitude sets negative full scale in bipolar mode.

Digital Outputs

D0 through D15 - Data Bus Outputs, PINS 2 thru 9, 12 thru 19.

3-state output pins. Enabled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$, they offer the converter's 16-bit output in a format consistent with the state of BW if A0 is high. If A0 is low, bits D0-D7 offer status register.

$\overline{\text{EOT}}$ - End Of Track, PIN 37.

If low, indicates that enough time has elapsed since the last conversion for the device to acquire the analog input signal (3.75µs for 4MHz external clock).

$\overline{EOC}$ - End Of Conversion, PIN 38.

This output indicates the end of a conversion or calibration cycle. It is high during a conversion and will fall to a low state upon completion of the conversion cycle indicating valid data is available at the output. Returns high on the first subsequent read or the start of a new conversion cycle.

SDATA - Serial Output, PIN 40.

Presents each output data bit after it is determined by the successive approximation algorithm. Valid on the rising edge of SCLK, data appears MSB first, LSB last, and each bit remains valid until the next bit appears.

SCLK - Serial Clock Output, PIN 39.

Used to clock converted output data serially from the CS5016. Serial data is stable on the rising edge of SCLK.

Analog Outputs

REFBUF - Reference Buffer Output, PIN 29.

Reference buffer output. A 0.1µF ceramic capacitor must be tied between this pin and VA-.

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Miscellaneous

TST - Test, PIN 31.

Allows access to the CS5016's test functions which are reserved for factory use. Must be tied to DGND.

ERROR DEFINITIONS

Linearity Error - The deviation of a code from a straight line passing through the endpoints of the transfer function after zero- and full-scale errors have been accounted for. "Zero-scale" is a point 1/2 LSB below the first code transition and "full-scale" is a point 1/2 LSB beyond the code transition to all ones. The deviation is measured from the middle of each particular code. Units in LSB's.

Differential Linearity - The deviation of a code's width from the ideal width. Units in LSB's.

Full Scale Error - The deviation of the last code transition from the ideal (VREF-3/2 LSB's). Units in LSB's.

Unipolar Offset - The deviation of the first code transition from the ideal (1/2 LSB above AGND) when in unipolar mode (BP/UP low). Units in LSB's.

Bipolar Offset - The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below AGND) when in bipolar mode (BP/$\overline{UP}$ high). Units in LSB's.

Bipolar Negative Full-Scale Error - The deviation of the first code transition from the ideal when in bipolar mode (BP/$\overline{UP}$ high). The ideal is defined as lying on a straight line which passes through the final and mid-scale code transitions. Units in LSB's.

Aperture Time - The time required after the hold command for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

Aperture Jitter - The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

Note: Temperatures specified define ambient conditions in free-air during test and do not refer to the junction temperature of the device.

Ordering Guide

Model	Linearity	Conversion Time	Temp. Range	Package
CS5016-JC32	.0030%	32.50 µs	0 to 70 °C	40-Pin Ceramic Side-Brazed DIP
CS5016-JC16	.0030%	16.25 µs	0 to 70 °C	40-Pin Ceramic Side-Brazed DIP
CS5016-KC32	.0015%	32.50 µs	0 to 70 °C	40-Pin Ceramic Side-Brazed DIP
CS5016-KC16	.0015%	16.25 µs	0 to 70 °C	40-Pin Ceramic Side-Brazed DIP
CS5016-AC32	.0030%	32.50 µs	-40 to +85 °C	40-Pin Ceramic Side-Brazed DIP
CS5016-AC16	.0030%	16.25 µs	-40 to +85 °C	40-Pin Ceramic Side-Brazed DIP
CS5016-BC32	.0015%	32.50 µs	-40 to +85 °C	40-Pin Ceramic Side-Brazed DIP
CS5016-BC16	.0015%	16.25 µs	-40 to +85 °C	40-Pin Ceramic Side-Brazed DIP
CS5016-SC16	.0030%	16.25 µs	-55 to +125 °C	40-Pin Ceramic Side-Brazed DIP
CS5016-TC16	.0015%	16.25 µs	-55 to +125 °C	40-Pin Ceramic Side-Brazed DIP

ADDENDUM

Burst Calibration

Burst calibration mode allows control of partial calibration cycles. Due to an unforeseen condition inside the part, asynchronous termination of calibration (CAL brought low) may result in a sub-optimal calibration result. It is recommended that burst calibration is not used, until the silicon is revised to prevent this effect.

The reset and interleave mode work perfectly, and should be used instead of burst mode. The CS5016's very low drift over temperature means that, under most circumstances, calibration need only be performed at power-up, using reset (See *Analog Characteristics* table on the second page of this data sheet).

If you wish to use burst calibration, then please contact the factory for advice and new part availability information.

• Notes •

Semiconductor Corporation

CS7820

High Speed 8-Bit A-to-D with Track and Hold

Features

- Completely Self-Contained
  - On-Chip Track and Hold
  - Microprocessor Interface
  - Internal Clock
  - Overrange Flag
- Fast Conversions: 1.36us max
- True 8-Bit Accuracy over Temperature
  - No Trims Required
  - No Missing Codes
- Low Power Dissipation: 100mW max
- Replaces ADC0820 and AD7820
- Single +5V Supply
- Improved Latch-up Resistance

General Description

The CS7820 is a low-cost, easy to use, microprocessor compatible 8-bit analog-to-digital converter with on-chip track-and-hold function. Use of CMOS and half-flash techniques allow both high throughput rates (1.36us max conversion time) and low power requirements (100mW max over the full Mil temperature range.)

The input to the CS7820 is tracked and held by on-chip sampling circuitry, eliminating the need for an external track-and-hold amplifier for input signals slewing at less than 100mV/us.

The CS7820 is designed to appear as a memory location or I/O port to a microprocessor without additional external interfacing logic. All of the data outputs use latched, three-state output buffers, allowing direct connection to a data bus or input port on a microprocessor system.

The CS7820 is pin compatible with the ADC0820 and AD7820.

ORDERING INFORMATION: Page 88

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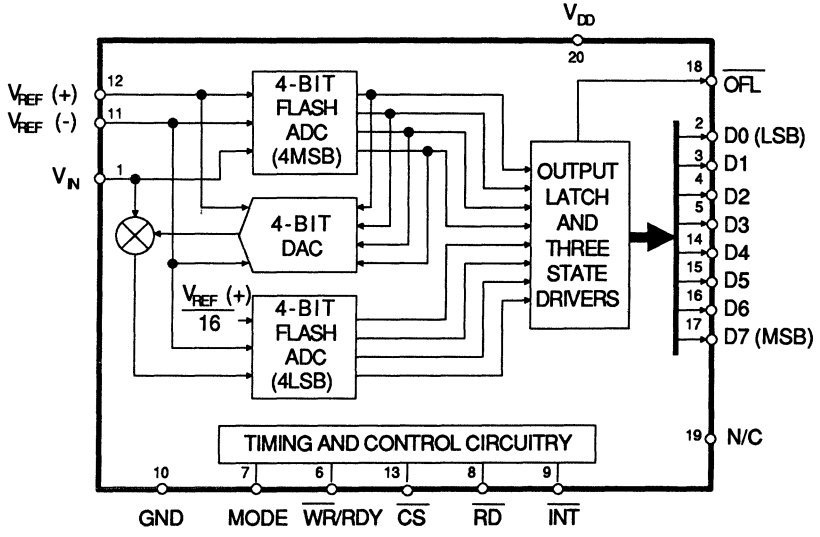


Crystal Semiconductor Corporation
P.O. Box 17847, Austin, Texas 78760
(512)445-7222 TWX:910-874-1352

ANALOG CHARACTERISTICS

(V_{DD} = +5V; $V_{REF}(+)$ = +5V; $V_{REF}(-)$ = GND = 0V; RD-Mode; T_A = T_{MIN} to T_{MAX} unless otherwise stated.)

Parameter	CS7820-K,L min	CS7820-K,L typ	CS7820-K,L max	CS7820-B,C min	CS7820-B,C typ	CS7820-B,C max	CS7820-T,U min	CS7820-T,U typ	CS7820-T,U max	Units
Specified Temperature Range	0	to	+70	-40	to	+85	-55	to	+125	°C
Accuracy										
Resolution	8			8			8			Bits
Total Unadjusted Error -K/B/T			±1			±1			±1	LSB
(Note 1) -L/C/U			±1/2			±1/2			±1/2	LSB
No Missing Code Resolution	8			8			8			Bits
Reference Input										
Input Resistance	1.0		4.0	1.0		4.0	1.0		4.0	kΩ
$V_{REF}(+)$ Input Voltage Range	V_{REF} (-)		V_{DD}	V_{REF} (-)		V_{DD}	V_{REF} (-)		V_{DD}	V
$V_{REF}(-)$ Input Voltage Range	GND		V_{REF} (+)	GND		V_{REF} (+)	GND		V_{REF} (+)	V
Analog Input										
Voltage Range	GND-0.1		V_{DD}+0.1	GND-0.1		V_{DD}+0.1	GND-0.1		V_{DD}+0.1	V
Leakage Current (V_{IN} = 0V to 5V)			±3			±3			±3	uA
Capacitance (Note 2)		45			45			45		pF
Slew Rate, Tracking (Note 2)		0.2	0.1		0.2	0.1		0.2	0.1	V/us
Power Supply										
Supply Range for Specified Operation	4.75		5.25	4.75		5.25	4.75		5.25	V
Supply Current ($\overline{CS}$=$\overline{RD}$=0V)			15			20			20	mA
Power Dissipation		40			40			40		mW
Power Supply Sensitivity V_{DD}=5V±5%		±1/16	±1/4		±1/16	±1/4		±1/16	±1/4	LSB

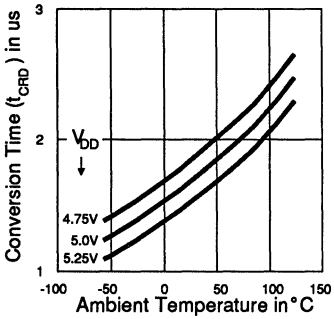
Notes: 1. Total unadjusted Error includes offset, full-scale and linearity errors.
2. Sample tested at 25°C to assure compliance.

Ordering Guide

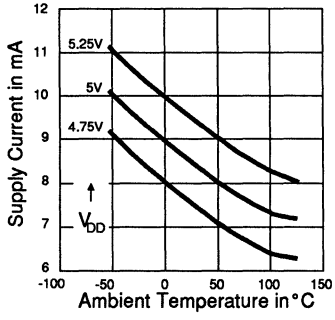
Model	Error	Temp Range	Package
CS7820-KP	± 1 LSB	0 to 70°C	20-Pin Plastic DIP
CS7820-LP	± 1/2 LSB	0 to 70°C	20-Pin Plastic DIP
CS7820-BD	± 1 LSB	-40 to 85°C	20-Pin CerDIP
CS7820-CD	± 1/2 LSB	-40 to 85°C	20-Pin CerDIP
CS7820-TD	± 1 LSB	-55 to 125°C	20-Pin CerDIP
CS7820-UD	± 1/2 LSB	-55 to 125°C	20-Pin CerDIP

Specifications are subject to change without notice.

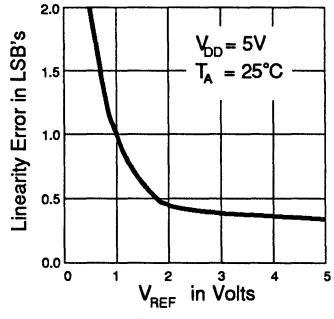
Typical Performance Characteristics



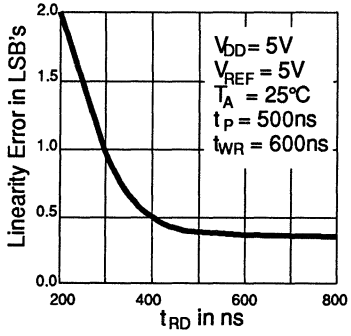
Conversion Time (RD Mode) vs. Temperature



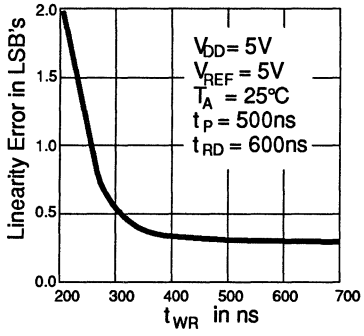
Power Supply Current vs. Temperature (not including reference ladder)



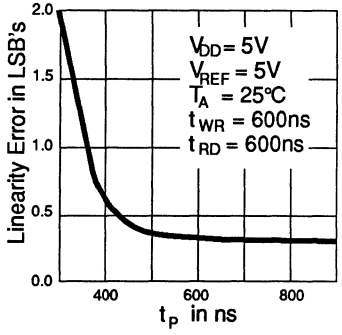
Accuracy vs. V_{REF} ($V_{REF} = V_{REF}(+) - V_{REF}(-)$ and 1LSB = $V_{REF}/256$)



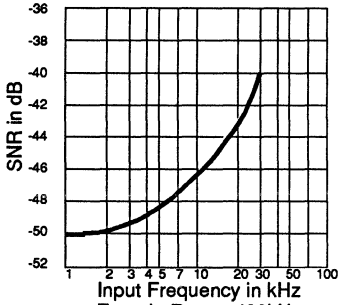
Accuracy vs. t_{RD}



Accuracy vs. t_{WR}

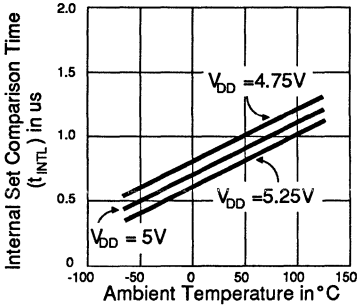


Accuracy vs. t_P

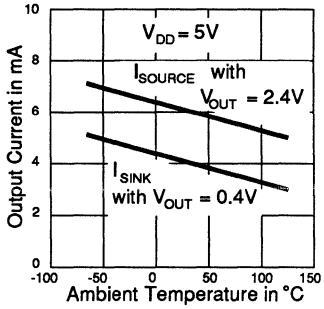


Encode Rate = 400kHz
Input Signal = 5V p-p
Measurement Bandwidth = 80kHz

Signal-Noise Ratio vs. Input Frequency



Internal Time Delay (t_{INTL}) vs. Temperature



Output Current vs. Temperature

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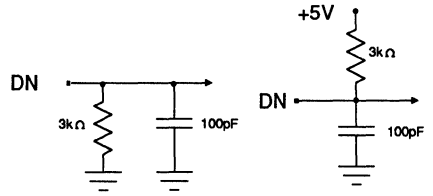
SWITCHING CHARACTERISTICS (V_{DD} = 5V; $V_{REF}(+)$ = 5V; $V_{REF}(-)$ = GND = 0V. (Note 6))

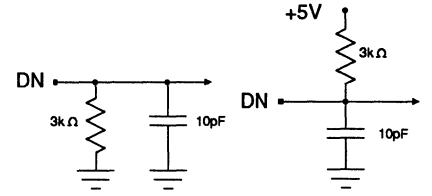
Parameter		Symbol	CS7820-K,L Min	CS7820-K,L Typ	CS7820-K,L Max	CS7820-B,C Min	CS7820-B,C Typ	CS7820-B,C Max	CS7820-T,U Min	CS7820-T,U Typ	CS7820-T,U Max	Units
$\overline{CS}$ to $\overline{RD}$/$\overline{WR}$ Setup Time	T_A = 25°C	t_{CSS}	0			0			0			ns
	$T_A = T_{MIN}$ to T_{MAX}		0			0			0			ns
$\overline{CS}$ to $\overline{RD}$/$\overline{WR}$ Hold Time	T_A = 25°C	t_{CSH}	0			0			0			ns
	$T_A = T_{MIN}$ to T_{MAX}		0			0			0			ns
$\overline{CS}$ to $\overline{RDY}$ Delay with	T_A = 25°C	t_{RDY}			70			70			70	ns
a 2kΩ Pull-Up	$T_A = T_{MIN}$ to T_{MAX}	(Note 3)			90			90			100	ns
Conversion Time,	T_A = 25°C	t_{CRD}			1.6			1.6			1.6	us
RD Mode	$T_A = T_{MIN}$ to T_{MAX}				2.0			2.0			2.5	us
Data Access Time,	T_A = 25°C	t_{ACCO}			t_{CRD}+35			t_{CRD}+35			t_{CRD}+35	ns
RD Mode	$T_A = T_{MIN}$ to T_{MAX}	(Note 4)			t_{CRD}+35			t_{CRD}+45			t_{CRD}+60	ns
$\overline{RD}$ to $\overline{INT}$ Delay,	T_A = 25°C	t_{INTH}		125	175		125	175		125	175	ns
RD Mode	$T_A = T_{MIN}$ to T_{MAX}	(Note 3)			225			225			225	ns
Data Hold Time	T_A = 25°C	t_{DH}			60			60			60	ns
	$T_A = T_{MIN}$ to T_{MAX}	(Note 5)			80			80			100	ns
Delay Time between	T_A = 25°C	t_P	500			500			500			ns
Conversions	$T_A = T_{MIN}$ to T_{MAX}		600			600			600			ns
Write Pulse Width	T_A = 25°C	t_{WR}	0.6		50	0.6		50	0.6		50	us
	$T_A = T_{MIN}$ to T_{MAX}		0.6		50	0.6		50	0.6		50	us
Conversion Time,	T_A = 25°C	t_{CWR-RD}			1360			1360			1360	ns
WR/RD Mode	$T_A = T_{MIN}$ to T_{MAX}				1525			1525			1550	ns
Delay Time between $\overline{WR}$	T_A = 25°C	t_{RD}	600			600			600			ns
and $\overline{RD}$ Pulses	$T_A = T_{MIN}$ to T_{MAX}		700			700			700			ns
Data Access Time, WR-RD	T_A = 25°C	t_{ACC1}			160			160			160	ns
Mode (Fig. 6)	$T_A = T_{MIN}$ to T_{MAX}	(Note 4)			225			225			250	ns
$\overline{RD}$ to $\overline{INT}$ Delay	T_A = 25°C	t_{RI}			140			140			140	ns
	$T_A = T_{MIN}$ to T_{MAX}				200			200			225	ns
$\overline{WR}$ to $\overline{INT}$ Delay	T_A = 25°C	t_{INTL}		700	1000		700	1000		700	1000	ns
	$T_A = T_{MIN}$ to T_{MAX}	(Note 3)			1400			1400			1700	ns
Data Access Time, WR-RD	T_A = 25°C	t_{ACC2}			70			70			70	ns
Mode (Fig. 5)	$T_A = T_{MIN}$ to T_{MAX}	(Note 4)			90			90			110	ns
$\overline{WR}$ to $\overline{INT}$ Delay, Stand-	T_A = 25°C	t_{IHWR}			100			100			100	ns
Alone Operation	$T_A = T_{MIN}$ to T_{MAX}	(Note 3)			130			130			150	ns
Data Access Time	T_A = 25°C	t_{ID}			50			50			50	ns
after $\overline{INT}$, Stand-	$T_A = T_{MIN}$ to T_{MAX}				65			65			75	ns
Alone Operation												

Notes: 3. CL = 50pF.
4. Measured with the load shown in Fig. 1, and defined as the time for an output to cross 0.8V or 2.4V.
5. Measured with the load shown in Fig. 2, and defined as the time required for the data lines (D0 - D7) to change 0.5V.
6. Sample tested to ensure compliance.



a. High-Z to V_{OH} b. High-Z to V_{OL}

Figure 1. Load Circuits for Data Access Time Test



a. V_{OH} to High-Z b. V_{OL} to High-Z

Figure 2. Load Circuits for Data Hold Time Test

DIGITAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; $V_{DD} = 5V \pm 5\%$; $V_{REF}(+) = 5V$; $V_{REF}(-) = GND = 0V$; All measurements below are performed under static conditions.)

Parameter	Symbol	Min	Typ	Max	Units
Logic Inputs (CS, WR, RD)					
High-Level Input Voltage	V_{IH}	2.4			V
Low-Level Input Voltage	V_{IL}			0.8	V
High-Level Input Current (CS, RD)	I_{IH}			1	uA
High-Level Input Current (WR)	I_{IH}			3	uA
Low-Level Input Current	I_{IL}			-1	uA
Input Capacitance (Note 7)			5	8	pF
Logic Inputs (MODE)					
High-Level Input Voltage	V_{IH}	3.5			V
Low-Level Input Voltage	V_{IL}			1.5	V
High-Level Input Current	I_{IH}			200	uA
Low-Level Input Current	I_{IL}			-1	uA
Input Capacitance (Note 7)			5	8	pF
Logic Outputs (D0-D7, OFL, INT)					
High-Level Output Voltage (@ -360uA)	V_{OH}	4.0			V
Low-Level Output Voltage (@ 1.6mA)	V_{OL}			0.4	V
Output Current (Leakage on D0-D7)	I_{out}			±3	uA
Output Capacitance (Note 7)			5	8	pF

Note: 7. Sample tested at 25°C to ensure compliance.

ABSOLUTE MAXIMUM RATINGS (GND = 0V; All voltages with respect to ground.)

Parameter	Symbol	Min	Max	Units
Power Supply Voltage	V_{DD}	−0.3	10.0	V
Input Current, Any Pin Except Supply	I_{in}	-	±10	mA
Voltage, Any Pin Except Supply	V_{in}	-0.3	V_{DD} + 0.3	V
Ambient Operating Temperature	T_A	-55	125	°C
Storage Temperature	T_{STG}	-65	150	°C
Power Dissipation (Any Package) to 75 °C Derate above 75 °C			500 6	mW mW/ °C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

6

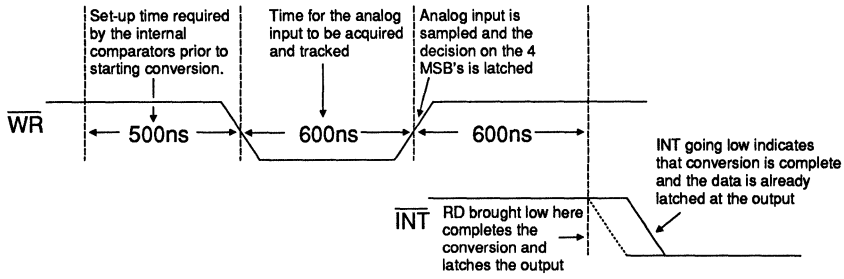


Figure 3. Basic Operation (WR-RD Mode)

GENERAL DESCRIPTION

The CS7820 generates an accurate 8-bit digital output representation of the analog input signal by making use of two 4-bit flash converters, and implementing a two-step conversion architecture. This approach achieves both high speed conversions and 8-bit accuracy without external user trims. The CS7820 also has an inherent track-and-hold input stage, which eliminates the need for an external track-and-hold in most applications.

The two-step flash architecture first converts the 4 MSB's (most significant bits.) These 4-bits of data drive an on-board DAC, whose output is subtracted from the analog input. The remainder is then fed into the second flash converter to generate the 4 LSB's (least significant bits.) The digital side of the CS7820 is designed for ease of operation and flexibility in use with microprocessors or in stand-alone operation.

BASIC OPERATION

The basic operating timing for the CS7820 in the WR-RD Mode is shown in Figure 3. A conversion is initiated by a falling edge on $\overline{WR}$, which causes the input stage to start acquiring and tracking the analog input. The MSB flash converter comparators track the input as long as $\overline{WR}$ stays low, with a minimum of 600 ns required to acquire the input signal. When $\overline{WR}$ returns high, the 4 bits of the MSB flash converter output are latched into the output buffers, and the LSB flash converter begins. $\overline{INT}$ goes low about 700 ns later, indicating that the 4 LSB's of data are latched into the output buffer, and that the full conversion has been completed. The output data word is then accessed by bringing $\overline{RD}$ low.

To control the conversion time externally, $\overline{RD}$ can be brought low as soon as 600 ns after $\overline{WR}$ goes high. This latches the 4 LSB's and outputs the data word on D0-D7. A minimum setup time of 500 ns is required after $\overline{INT}$ goes low before initiating another conversion (by $\overline{WR}$ going low.)

DIGITAL INTERFACE

The input level at the MODE pin determines the basic interface mode of the CS7820. A Logic Low input puts the converter in the RD mode,

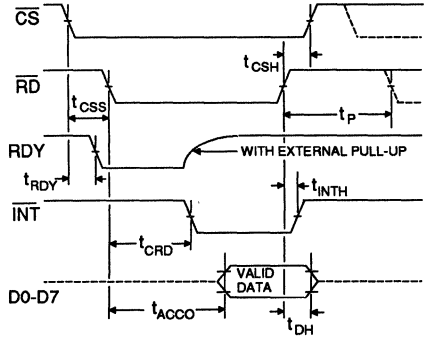


Figure 4. RD Mode

while a Logic High input puts the converter in the WR-RD mode.

RD Mode

The RD mode allows the user to control conversion and data access with the $\overline{RD}$ input (see Figure 4.) A conversion is initiated by bringing $\overline{RD}$ low, and it is kept low until output data appears. This mode is useful for microprocessors that can be put into a WAIT state, since the processor can use a single READ instruction to initiate conversion, wait, and read the output data.

In RD mode, pin 6 ($\overline{WR}$/RDY) provides a status output, RDY, which can be used to drive the WAIT or READY input of a microprocessor. There is no internal pull-up on RDY (it is an open drain output). RDY goes low after the falling edge of $\overline{CS}$ and then goes high impedance at the end of a conversion. An $\overline{INT}$ output pin is also available, which goes low at the end of a conversion and returns high on the rising edge of either $\overline{RD}$ or $\overline{CS}$.

WR-RD Mode

The WR-RD mode provides the fastest conversion time by allowing the user full control over the various stages in the conversion process. In this mode, pin 6 ($\overline{WR}$/RDY) is used as a WRITE input to the converter. With $\overline{CS}$ low, a falling edge on $\overline{WR}$ initiates a conversion. Various options are available for reading the output data.

Using internal delay. In this mode, the $\overline{INT}$ output is used to signal the processor to read the data (Figure 5.) $\overline{INT}$ goes low about 700 ns after the rising edge of $\overline{WR}$, indicating that the conversion has been completed and the data word is available in the output latch. To access D0-D7, $\overline{RD}$ is brought low with $\overline{CS}$ low. The rising edge of either $\overline{RD}$ or $\overline{CS}$ resets $\overline{INT}$.

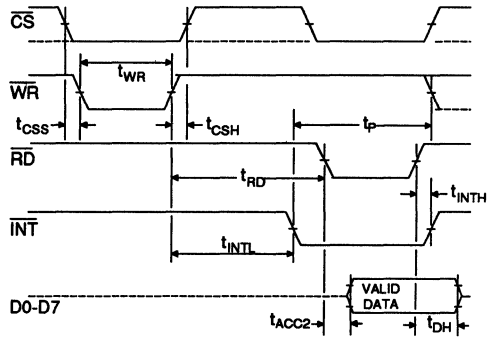


Figure 5. WR-RD Mode ($t_{RD} > t_{INTL}$)

Using external RD timing. In this mode, the $\overline{RD}$ input can be used to externally minimize conversion time (Figure 6.) This mode is useful in applications with critical timing, since the internal delay on $\overline{INT}$ can vary with supplies and temperature. (See the typical performance curves.) Bringing $\overline{RD}$ low before $\overline{INT}$ goes low completes the conversion and enables the output latch. This can be done as soon as 600 ns after the rising edge of $\overline{WR}$.

Pipelined operation. By tying $\overline{WR}$ and $\overline{RD}$ together, the CS7820 can be pipelined. With $\overline{CS}$ low, bringing $\overline{WR}$ and $\overline{RD}$ low together both initiates a new conversion and enables the output latch so that the user can read the results of the previous conversion.

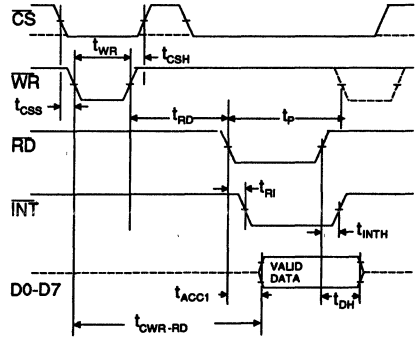


Figure 6. WR-RD Mode ($t_{RD} < t_{INTL}$)

Stand-Alone operation. The CS7820 can also be used in stand-alone operation, by tying $\overline{CS}$ and $\overline{RD}$ to ground. A conversion is initiated by bringing $\overline{WR}$ low, and the output data will be valid approximately 700 ns after the rising edge of $\overline{WR}$. (Figure 7.)

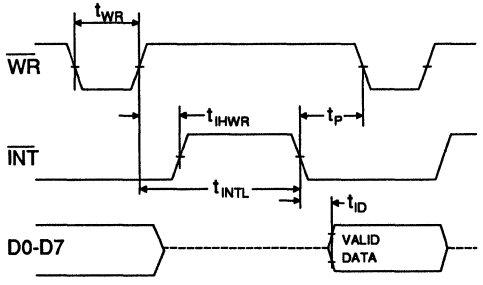


Figure 7. WR-RD Mode
Stand-Alone Operation ($\overline{CS}$ = $\overline{RD}$ = 0V)

ANALOG OPERATING INFORMATION

Reference and Input

The two reference inputs to the CS7820 define the zero to fullscale range of the converter. These are fully differential inputs. The negative reference input defines the analog input level that will generate an output data word of all zeroes, while the positive reference input defines the analog input level that will generate an output data word of all ones.

The analog input can span the range of the reference input range. Thus the sensitivity of the converter can be increased by reducing the span of the reference inputs (and making the size of each LSB smaller). Use of the reference structure also allows the analog input span to be offset from zero, as shown in Figure 12.

Although the analog input is not differential, the reference flexibility facilitates use in most measurement applications. The input and reference architecture also facilitates ratiometric applications.

Inherent Track-and-Hold

The equivalent input circuit for the CS7820 is shown in Figure 8a. The inherent sampling structure means that a wide variety of high speed input signals can be measured without requiring an external track-and-hold. Typically, input signals with slew rates below 200 mV/µs can be converted with full 8-bit accuracy. Faster input signals will start to degrade accuracy, because of input time constants and charge injection through the comparator input switches, but the degradation will occur less quickly than on traditional successive approximation converters.

The CS7820 tracks the analog input signal while $\overline{WR}$ is low, and holds the input signal approximately 100 ns after the rising edge of $\overline{WR}$. This is effectively the aperture delay of the inherent track-and-hold.

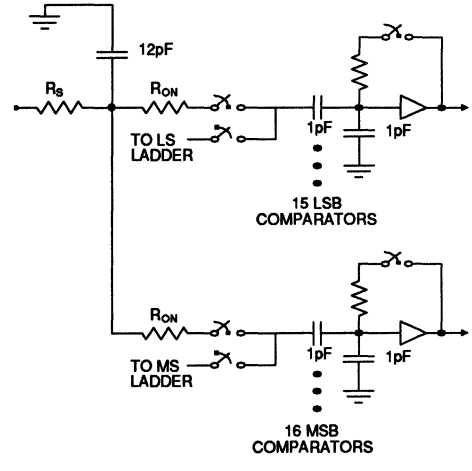


Figure 8a. CS7820 Equivalent Input Circuit

Input Current

The sampling input of the CS7820 provides a varying load for the input signal depending on the stage of the conversion cycle. (Refer again to Figure 8a.) When conversion starts ($\overline{WR}$ is brought low) the analog input is connected to the MSB and LSB flash converter inputs, effectively seeing thirty-one 1 pF capacitors. These capacitors need to be charged during the acquisition phase ($\overline{WR}$ held low) through the resistance of the internal analog switches, which range from about 2 kΩ to 5 kΩ. Stray capacitance adds about 12 pF to the input load. For large source resistances, Figure 8b approximates the load RC network. As the source impedance increases, the capacitors take longer to charge.

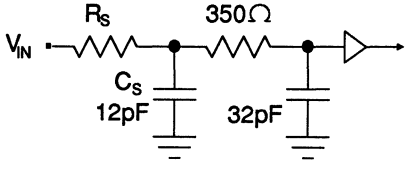


Figure 8b. CS7820 RC Network Model

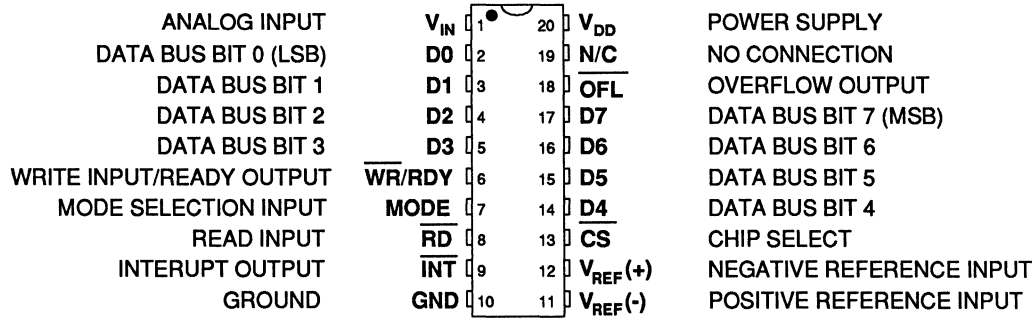
Input resistances up to 1 kΩ can be used without settling problems with the typical 45 pF input capacitance. For larger source resistances, the width of the $\overline{WR}$ pulse needs to be increased. This means that the RD mode may be inappropriate for applications with higher source resistances, since the acquisition time is internally set. Alternatively, an input buffer could be used to drive the analog input of the CS7820.

Input Filtering

Because the sampling input structure has a minimum 600 ns charging time while $\overline{WR}$ is held low, transients on the analog input will not normally degrade the converter's performance. It is therefore not necessary to filter the input to the CS7820 in most applications.

6

PIN DESCRIPTIONS



Analog and Reference Inputs

V_{IN} - Analog Input, Pin 1

V_{REF}(-) - Negative Reference Input, Pin 11

Lower limit of the reference span. Sets the voltage level for an output code of all zeroes.

V_{REF}(+) - Positive Reference Input, Pin 12

Upper limit of the reference span. Sets the voltage level for an output code of all ones.

Digital Inputs and Outputs

D0 through D7 - Data Bus Outputs, Pins 2 thru 5 and 14 thru 17

Tri-state output pins. D0 (the LSB) is on Pin 2, ascending to D7 (the MSB) on pin 17.

$\overline{WR}$/RDY - Write Input/ Ready Output, Pin 6

Depending on the mode of operation, acts as either an input pin to initiate conversions (WR-RD mode) or as an output status pin to indicate that the conversion is complete and the output data is ready (RD mode).

MODE - Mode Selection Input, Pin 7

Determines whether the device operates in the WR-RD mode or the RD mode. It has an internal pull-down circuit with a 50µA current source, so the default operating condition is the RD mode.

$\overline{RD}$ - Read Input, Pin 8

$\overline{RD}$ must be low to access data.

$\overline{INT}$ - Interrupt Output, Pin 9

$\overline{INT}$ going low indicates the conversion is complete.

$\overline{CS}$ - Chip Select Input, Pin 13

$\overline{CS}$ must be low for the device to accept $\overline{RD}$ or $\overline{WR}$ inputs.

$\overline{OFL}$ - Overflow Output, Pin 18

If the analog input is greater than $V_{REF}(+)$ -1/2 LSB, $\overline{OFL}$ will be high at the end of the conversion. This can be used to cascade devices for increased resolution. This output pin is not tri-state.

Power Supply and Ground

GND - Ground, Pin 10

V_{DD} - Power Supply, Pin 20

APPLICATIONS INFORMATION

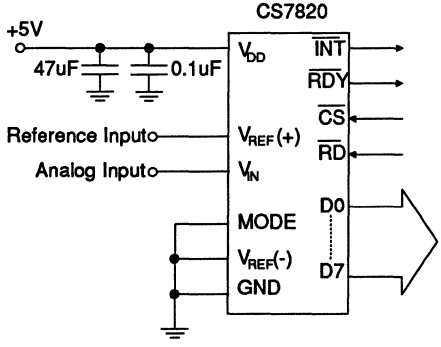


Figure 9. RD Mode, 8-Bit Resolution

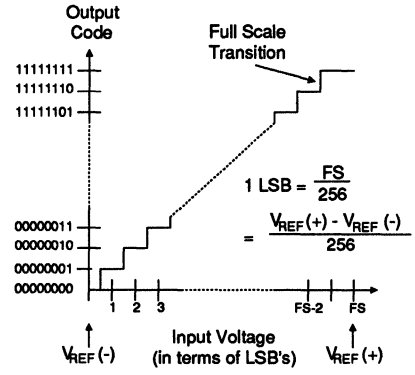


Figure 10. CS7820 Transfer Function

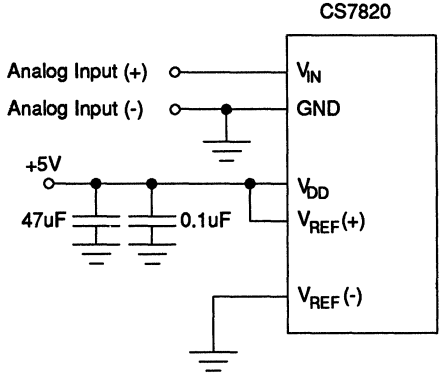


Figure 11. Using the Supply as Reference

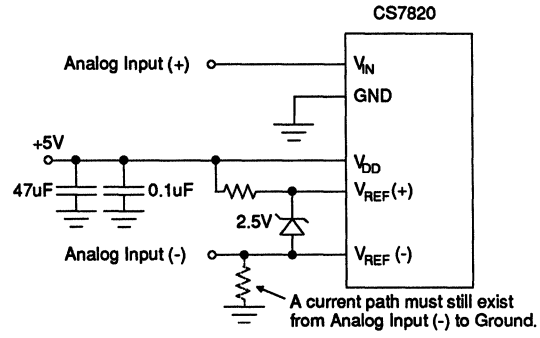


Figure 12. Input Not Referenced to Ground

INTRODUCTION

The design and production of signal processing systems is made dramatically easier using Crystal's line of S-to-Z™ converters. Specified for DSP applications, these specialized 12- to 16-Bit A/D converters perform the sampling function to bridge the continuous-time s-domain and sampled-time z-domain. FFT production test techniques guarantee the dynamic frequency response of each device at full rated clock speed. With throughput rates from 20 kHz to 1 MHz they are ideal for single or multichannel voiceband, audioband and higher frequency applications.

USER'S GUIDE

Device:	CSZ5316/7	CSZ5116	CSZ5114	CSZ5112	CSZ5412
Resolution (Bits)	16	16	14	12	12
Conversion Technique	Delta-Sigma	Succ. Approx.	Succ. Approx.	Succ. Approx.	2-Step Flash
Throughput (kHz)	20	50	56	100	1000
THD %	0.007	0.001	0.003	0.008	0.02
S/(N + D) (dB)	80	92	83	73	70
Power Dissipation (mW)	220	120	120	120	750
On-Chip Sample/Hold	♥	♥	♥	♥	♥
On-Chip Ref	♥				
On-Chip Anti-Alias Filtering	♥				
Temperature Ranges	Com, Ind, Mil	Com, Ind, Mil	Com, Ind, Mil	Com, Ind, Mil	Com, Ind, Mil
Package	18-Pin DIP	40-Pin DIP	40-Pin DIP	40-Pin DIP	40-Pin DIP

CONTENTS

Semiconductor Corporation

CSZ5112

12-Bit, 100kHz Sampling A/D Converter

Features

- Monolithic CMOS A/D Converter
  - Inherent Sampling Architecture
  - 3-State Output Buffers
  - Microprocessor Interface
- Sampling Rates up to 100kHz
- Low Harmonic Distortion
  - Total Harmonic Distortion: 0.008%
  - Peak Harmonic or Noise: −87dB
- Low Power Dissipation: 120mW
- Pin Compatible with CSZ5114/CSZ5116

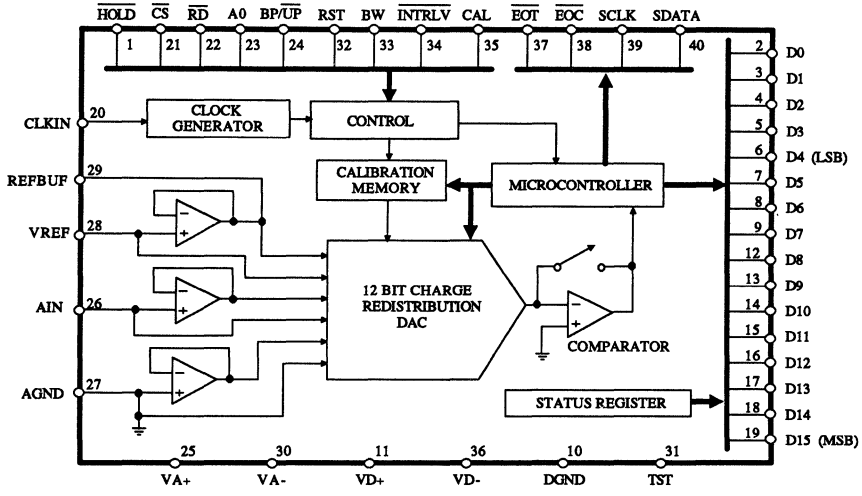
General Description

The CSZ5112 CMOS analog-to-digital converter is an ideal front end for single- or multi-channel digital signal processing systems. It needs no external sample/hold amplifier at its input to convert ac signals - the sampling function is inherent to its charge redistribution design.

Using a standard successive-approximation algorithm, the CSZ5112 sequences through a 12-bit conversion in 7.2 microseconds. With 2.8 microseconds needed between conversions for acquisition, the CSZ5112 can support throughput rates up to 100kHz. It is therefore ideal for processing audioband signals.

The CSZ5112 features an on-chip self-calibration scheme which calibrates its bit weights to true 12-bit accuracy. This insures low distortion and maintains good signal-to-noise performance with low-level signals.

ORDERING INFORMATION: Page 30



S-to-Z ™ Converter

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, Texas 78760
(512)445-7222 TWX:910-874-1352

7

ANALOG CHARACTERISTICS

(T_A = 25°C; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 2.5V to 4.5V; Full-Scale Input Sinewave, 1KHz; f_{clk} = 6.8MHz for -7, 4MHz for -12, 2MHz for -24; f_s = 100kHz for -7, 63kHz for -12, 34kHz for -24; Bipolar Mode ; Analog Source Impedance = 200Ω unless otherwise specified)

Parameter*	CSZ5112-K min	CSZ5112-K typ	CSZ5112-K max	CSZ5112-B min	CSZ5112-B typ	CSZ5112-B max	CSZ5112-T min	CSZ5112-T typ	CSZ5112-T max	Units
Specified Temperature Range		0 to 70			-40 to +85			-55 to +125		°C
Dynamic Performance										
Peak Harmonic or Spurious Noise										
1kHz Input 25°C	84	87		84	87		84	87		dB
(Note 1) T_{min} to T_{max}	84	87		84	87		84	87		dB
12kHz Input	80	83		80	83		80	83		dB
Total Harmonic Distortion		0.008			0.008			0.008		%
Signal-to-Noise Ratio										
0dB Input T_{min} to T_{max}	72	73		72	73		72	73		dB
-60dB Input		13			13			13		dB
dc Accuracy										
Differential Linearity (Note 2)	12			12			12			Bits
Full Scale Error T_{min} to T_{max}		± 1/4			± 1/4			± 1/4		LSB
Unipolar Offset T_{min} to T_{max}		± 1/4			± 1/4			± 1/4		LSB
Bipolar Offset T_{min} to T_{max}		± 1/4			± 1/4			± 1/4		LSB
Bipolar Zero Error T_{min} to T_{max}		± 1/4			± 1/4			± 1/4		LSB
Analog Input										
Aperture Time		25			25			25		ns
Aperture Jitter		100			100			100		ps
Full Power Bandwidth (Note 3)		32			32			32		kHz
Input Capacitance Unipolar Mode		275	375		275	375		275	375	pF
(Note 4) Bipolar Mode		165	220		165	220		165	220	pF

Notes:
1. All T_{min} to T_{max} specifications apply after calibration at the temperature of interest.
2. Minimum resolution for which no missing codes is guaranteed.
3. Refer to the *Analog Input* section on page 17 for a discussion of input slew capabilities.
4. Applies only in the track mode. When converting or calibrating, input capacitance will not exceed 15pF.

*Refer to *Error Definitions* on page 29.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter		CSZ5112-K min	typ	max	CSZ5112-B min	typ	max	CSZ5112-T min	typ	max	Units
Conversion & Throughput											
Conversion Time	– 7			7.2			7.2			-	us
	–12			12.25			12.25			12.25	us
(Notes 5,6)	–24			24.5			24.5			24.5	us
Acquisition Time	– 7		2.5	2.80		2.5	2.80		-	-	us
	–12		3.0	3.75		3.0	3.75		3.0	3.75	us
(Note 6)	–24		4.5	5.25		4.5	5.25		4.5	5.25	us
Throughput	– 7	100			100			-			kHz
	–12	62.5			62.5			62.5			kHz
(Note 6)	–24	33.6			33.6			33.6			kHz
Power Supplies											
Power Supply Currents (Note 7)											
I_{A+}			9	19		9	19		9	19	mA
I_{A-}			–9	–19		–9	–19		–9	–19	mA
I_{D+}			3	6		3	6		3	6	mA
I_{D-}			–3	–6		–3	–6		–3	–6	mA
Power Dissipation	(Note 7)		120	250		120	250		120	250	mW
Power Supply Rejection (Note 8)											
Positive Supplies			84			84			84		dB
Negative Supplies			84			84			84		dB

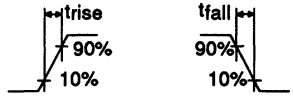
Notes:
5. Measured from falling transition on $\overline{\text{HOLD}}$ to falling transition on $\overline{\text{EOC}}$.
6. Conversion, acquisition, and throughput times depend on the master clock, sampling, and calibration conditions. The numbers shown assume sampling and conversion is synchronized with the CSZ5112's internal conversion clock, interleave calibrate is disabled, and operation is from the full-rated external master clock. A detailed discussion of conversion timing appears on page 11.
7. All outputs unloaded. All inputs CMOS levels.
8. With 300mV p-p, 1kHz ripple applied to each supply separately in the bipolar mode. Rejection improves by 6dB in the unipolar mode to 90dB. A plot of typical power supply rejection appears on page 23.

7

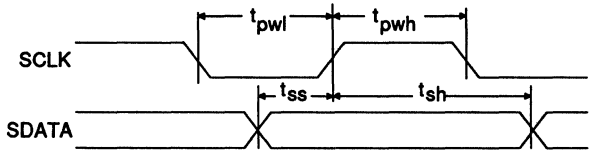
SWITCHING CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 50pF)

Parameter	Symbol	Min	Typ	Max	Units
Master Clock Frequency:					
Internally Generated: -7	f_{CLK}	2	-	-	MHz
Internally Generated: -12		2	-	-	
Internally Generated: -24		1	-	-	
Externally Supplied: -7		-	-	6.8	
Externally Supplied: -12		-	-	4	
Externally Supplied: -24		-	-	2	
Master Clock Duty Cycle	-	30	-	70	%
Rise Times: Any Digital Input	t_{rise}	-	-	1.0	us
Any Digital Output		-	20	-	ns
Fall Times: Any Digital Input	t_{fall}	-	-	1.0	us
Any Digital Output		-	20	-	ns
$\overline{HOLD}$ Pulse Width	t_{hpw}	$1/f_{CLK} + 50$	-	t_c	ns
Conversion Time	t_c	(Note 9)	-	(Note 9)	us
Data Delay Time	t_{dd}	-	40	100	ns
$\overline{EOC}$ Pulse Width (Note 10)	t_{epw}	$4/f_{CLK} - 20$	-	-	ns
Set Up Times: CAL, $\overline{INTRLV}$ to $\overline{CS}$ Low	t_{cs}	20	10	-	ns
A0 to $\overline{CS}$ and $\overline{RD}$ Low	t_{as}	20	10	-	
Hold Times:					
$\overline{CS}$ or $\overline{RD}$ High to A0 Invalid	t_{ah}	50	30	-	ns
$\overline{CS}$ High to CAL, $\overline{INTRLV}$ Invalid	t_{ch}	50	30	-	
Access Times: $\overline{CS}$ Low to Data Valid -K, B	t_{ca}	-	90	120	ns
Access Times: $\overline{CS}$ Low to Data Valid -T		-	115	150	
$\overline{RD}$ Low to Data Valid -K, B	t_{ra}	-	90	120	ns
$\overline{RD}$ Low to Data Valid -T		-	115	150	
Output Float Delay: -K, B	t_{fd}	-	50	110	ns
$\overline{CS}$ or $\overline{RD}$ High to Output Hi-Z -T		-	50	140	
Serial Clock Pulse Width Low	t_{pwl}	-	$2/f_{CLK}$	-	ns
Serial Clock Pulse Width High	t_{pwh}	-	$2/f_{CLK}$	-	
Set Up Times: SDATA to SCLK Rising	t_{ss}	$2/f_{CLK} - 100$	$2/f_{CLK}$	-	ns
Hold Times: SCLK Rising to SDATA	t_{sh}	$2/f_{CLK} - 100$	$2/f_{CLK}$	-	ns

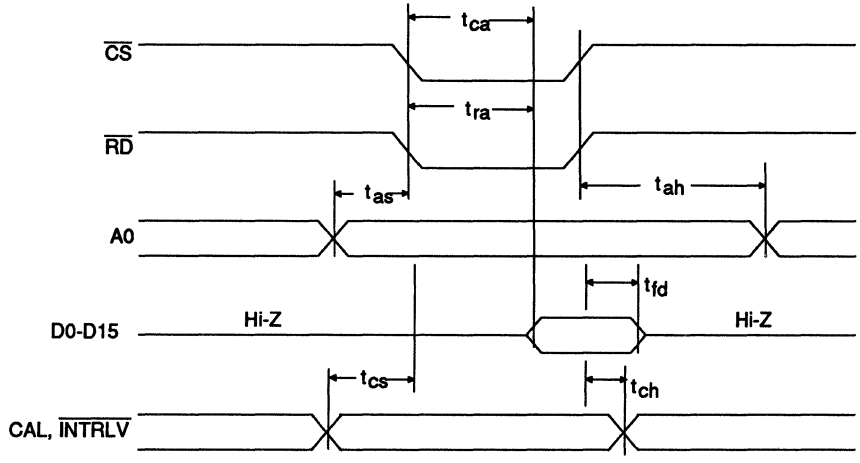
Notes: 9. See Table 1 and master clock frequencies above.
10. $\overline{EOC}$ remains low 4 master clock cycles if $\overline{CS}$ and $\overline{RD}$ are held low. Otherwise, It returns high within four master clock cycles from the start of a data read operation or a conversion cycle.



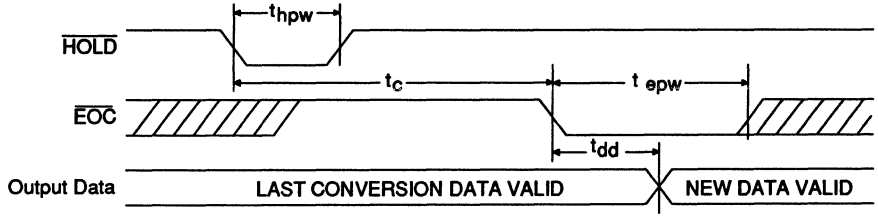
Rise and Fall Times



Serial Output Timing



Read and Calibration Control Timing



Conversion Timing

7

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%)

All measurements below are performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 11)	V_{OH}	VD+ - 1.0V	-	-	V
Low-Level Output Voltage Iout=1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	10	uA
3-State Leakage Current	I_{OZ}	-	-	±10	uA
Digital Output Pin Capacitance	C_{out}	-	9	-	pF

Note: 11. I_{out} = -100µA. This specification guarantees TTL compatibility (VOH=2.4V @ I_{out} = -40µA).

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see Note 12.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.5	5.0	VA+	V
	Negative Digital	VD-	−4.5	−5.0	−5.5	V
	Positive Analog	VA+	4.5	5.0	5.5	V
	Negative Analog	VA-	−4.5	−5.0	−5.5	V
Analog Reference Voltage		VREF	2.0	2.5	VA+-0.5	V
Analog Input Voltage:	Unipolar	V_{AIN}	AGND	-	VREF	V
(Note 13)	Bipolar	V_{AIN}	-(VREF)	-	VREF	V

Notes: 12. All voltages with respect to ground.

13. The CSZ5112 can accept input voltages up to the analog supplies (VA+ and VA-). It will output all 1's for inputs above VREF and all 0's for inputs below AGND in unipolar mode and -VREF in bipolar mode.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	−0.3	VA+ + 0.3	V
	Negative Digital	VD-	0.3	−6.0	V
	Positive Analog	VA+	−0.3	6.0	V
	Negative Analog	VA-	0.3	−6.0	V
Input Current, Any Pin Except Supplies (Note 14)		I_{in}	-	±10	mA
Analog Input Voltage (AIN and VREF pins)		V_{INA}	VA- - 0.3	VA+ + 0.3	V
Digital Input Voltage		V_{IND}	-0.3	VA+ + 0.3	V
Ambient Operating Temperature		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

Note: 14. Transient currents of up to 100mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

THEORY OF OPERATION

The CSZ5112 utilizes the most popular method of executing high-speed, high-resolution A/D conversion: successive approximation. As with all other iterative comparison methods, the analog input is successively compared to the output of a D/A converter controlled by the conversion algorithm. Successive approximation begins by comparing the input to the DAC output set to half-scale (MSB on, all other bits off). If the input is found to be below half-scale, the MSB is reset to zero and the input is compared to one-quarter scale (next-MSB on, all others off). If the input were above half-scale, the MSB would remain high and the next comparison would be at three-quarters of fullscale. This procedure continues until all bits have been exercised.

The CSZ5112 implements the successive approximation algorithm using a unique charge-redistribution architecture. Instead of the traditional resistor network, the DAC is an array of binary-weighted capacitors. All legs of the array share a common node at the comparator's input, with their other terminals capable of being connected to AIN, AGND, or VREF (Figure 1). When the device is not calibrating or converting, all bits are tied to AIN forming C_{tot}. Switch S1 is closed and the charge on the array, Q_{in}, tracks the input signal V_{in} (Figure 2a).

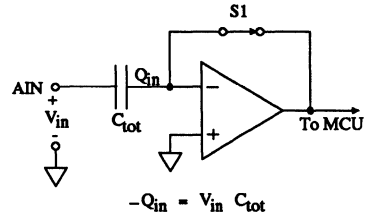


Figure 2a. Tracking Mode

When the conversion command is issued, switch S1 opens as shown in Figure 2b. This traps charge Q_{in} on the comparator side of the capacitor array and creates a floating node at the comparator's input. The conversion algorithm operates on this fixed charge, and the signal at the analog input pin is ignored. In effect, the entire DAC capacitor array serves as analog memory during conversion much like a hold capacitor in a sample/hold amplifier.

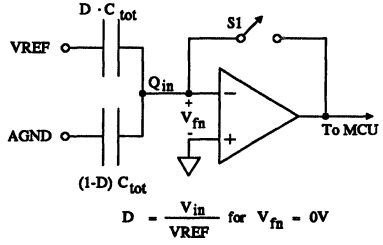


Figure 2b. Convert Mode

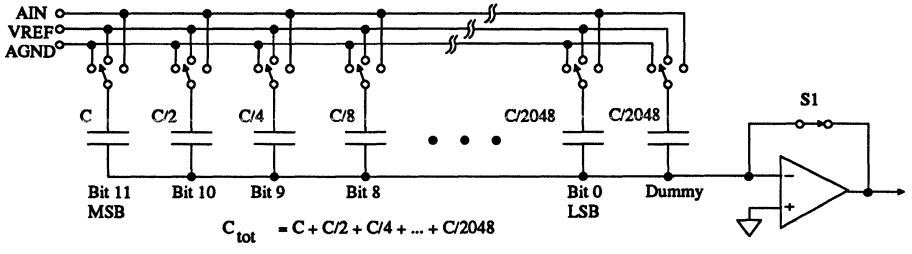


Figure 1. Charge Redistribution DAC

The conversion consists of manipulating the free plates of the capacitor array to VREF and AGND to form a capacitive divider. Since the charge at the floating node remains fixed, the voltage at that point depends on the proportion of capacitance tied to VREF versus AGND. The successive-approximation algorithm is used to find the proportion of capacitance, termed D in Figure 2b, which will drive the voltage at the floating node to zero. That binary fraction of capacitance represents the converter's digital output.

The CSZ5112's charge redistribution architecture easily supports bipolar input ranges. If half the capacitor array (the MSB capacitor) is tied to VREF rather than AIN in the track mode, the input range doubles and offsets half-scale. The magnitude of the reference voltage thus defines both positive and negative full-scale (-VREF to +VREF), and the digital code is an offset binary representation of the input.

Calibration

The ability of the CSZ5112 to convert accurately to 12-bits clearly depends on the accuracy of its comparator and DAC. The CSZ5112 utilizes an "auto-zeroing" scheme to null errors introduced by the comparator. All offsets are stored on the capacitor array while in the track mode and are effectively subtracted from the input signal when a conversion is initiated. Auto-zeroing enhances power supply rejection at frequencies below the conversion rate.

To achieve 12-bit accuracy from the DAC, the CSZ5112 uses a novel self-calibration scheme. Each bit capacitor shown in Figure 1 actually consists of several capacitors which can be manipulated to adjust the overall bit weight. During calibration, an on-chip microcontroller manipulates the sub-arrays to precisely ratio the bits. Each bit is adjusted to just balance the sum of all less significant bits plus one dummy LSB (for example, 16C = 8C + 4C + 2C + C + C). Calibration resolution for each bit is a small fraction of an LSB, resulting in a nearly ideal transfer function.

DIGITAL CIRCUIT CONNECTIONS

The CSZ5112 can be applied in a wide variety of master clock, sampling, and calibration conditions which directly affect the device's conversion time and throughput. The device also features on-chip 3-state output buffers and a complete interface for connecting to 8- and 16-bit digital systems. Output data is also available in serial format.

Master Clock

The CSZ5112 operates from a master clock which can be externally supplied or internally generated. The internal oscillator is activated by holding the CLKIN input low. Alternatively, the CSZ5112 can be synchronized to the external system by driving the CLKIN pin with a TTL or CMOS clock signal.

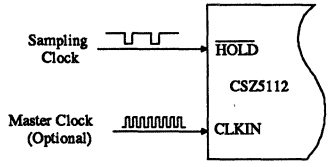


Figure 3a. Asynchronous Sampling

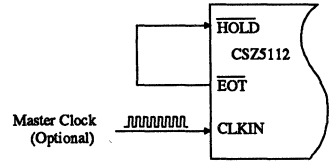


Figure 3b. Synchronous Sampling

All calibration, conversion, and throughput times directly scale to master clock frequency. Thus, throughput can be precisely controlled and/or maximized using an external master clock. In contrast, the CSZ5112's internal oscillator will vary from unit-to-unit and over temperature. Its tolerance gives rise to minimum and maximum conversion times and throughput rates. The -7 version of the CSZ5112 is specified for accurate operation with an external clock up to 6.8MHz; its internal clock frequency is specified at a minimum of 2MHz. The -12 version is specified for accurate operation with an external clock up to 4MHz; its internal clock frequency is specified at a minimum of 2MHz. The -24 version can handle external clocks up to 2MHz, and its internal clock can range as low as 1MHz (see *Switching Characteristics*, page 6).

Sampling/Initiating Conversions

A falling transition on the $\overline{\text{HOLD}}$ pin places the input in the hold mode and initiates a conversion cycle. The $\overline{\text{HOLD}}$ input is latched internally by the master clock, so it can return high anytime after one master clock cycle plus 50ns. Upon completion of the conversion cycle, the CSZ5112 automatically returns to the track mode. In contrast to systems with separate track-and-holds and A/D converters, a sampling clock can simply be connected to the $\overline{\text{HOLD}}$ input (Figure 3a). The duty cycle of this clock is not critical. It need only remain low at least one master clock cycle plus 50ns, but no longer than the minimum conversion time or an additional conversion cycle will be initiated with inadequate time for acquisition.

Conversion Time/Throughput

Upon completing a conversion cycle and returning to the track mode, the CSZ5112 requires time to acquire the analog input signal before another conversion can be initiated. The acquisition time is specified as six master clock cycles plus 2.25µs (1.32µs for the -7 version). This adds to the conversion time to define the converter's maximum throughput. The conversion time of the CSZ5112, in turn, depends on the sampling, calibration, and master clock conditions.

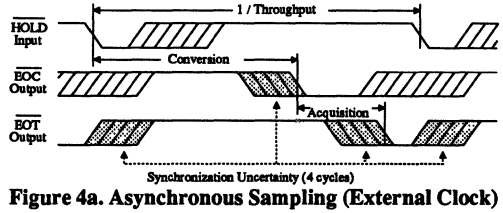


Figure 4a. Asynchronous Sampling (External Clock)

Asynchronous Sampling

The CSZ5112 internally operates from a clock which is delayed and divided down from the master clock ($f_{CLK}/4$). If sampling is not synchronized to this internal clock, the conversion cycle may not begin until up to four clock cycles after $\overline{\text{HOLD}}$ goes low *even though the charge is trapped immediately*. In this asynchronous mode (Figure 3a), the four clock cycles add to the minimum 49 clock cycles to define the maximum conversion time (see Figure 4a and Table 1).

	Conversion Time		Throughput Time	
Sampling Mode	min	max	min	max
Synchronous (Loopback)	49T	49T	64T	64T
Asynchronous	49T	53T + 235ns	N/A	59T + 2.25µs (+1.32µs for -7 version)

(T ≡ one master clock cycle)

Table 1. Conversion and Throughput Times

Synchronous Sampling

To achieve maximum throughput, sampling can be synchronized with the internal conversion clock by connecting the End-of-Track ($\overline{EOT}$) output back to $\overline{HOLD}$ (Figure 3b). The $\overline{EOT}$ output falls 15 master clock cycles after $\overline{EOC}$ indicating the analog input has been acquired to the CSZ5112's specified accuracy. The $\overline{EOT}$ output is synchronized to the internal conversion clock, so the four clock cycle synchronization uncertainty is removed yielding throughput at 1/64th of the master clock frequency (see Figure 4b and Table 1).

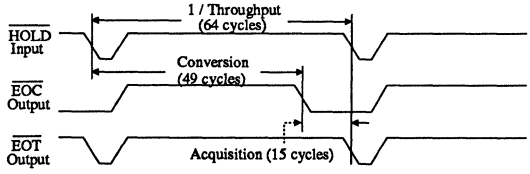


Figure 4b. Synchronous (Loopback) Mode

Also, the CSZ5112's internal RC oscillator exhibits significant jitter (typically ± 0.05% of its period), which is high compared to crystal oscillators. If the CSZ5112 is configured for synchronous sampling while operating from its internal clock, this jitter will affect sampling purity.

The $\overline{EOT}$ output is an accurate indicator of the CSZ5112's acquisition requirement when operating at the -7 version's full rated speed (with a 6.8MHz master clock). However, $\overline{EOT}$ will allow the CSZ5112 more acquisition time than necessary when operating with a clock less than the maximum specified. The $\overline{EOT}$ output always falls 15 master clock cycles after $\overline{EOC}$, when in reality, the CSZ5112 only needs six cycles plus 2.25µs (1.32µs for the -7 version). When operating the -24 with a master clock of 2MHz or less, higher throughput can be achieved than in the loopback configuration by using an external counter. The counter should be reset by the falling edge of $\overline{EOC}$ and count the clock cycles after each conversion. When the total time is greater than six clock cycles plus 2.25µs, the counter can trigger a new conversion at $\overline{HOLD}$. For example, when using a 2MHz clock, 2.25µs takes between four and five clock cycles. When six cycles are added to this it is seen that the counter should trigger a new conversion at the eleventh clock cycle.

Reset

Upon power up, the CSZ5112 must be reset to guarantee a consistent starting condition and to initially calibrate the device. Due to the CSZ5112's low power dissipation and low temperature drift, no warm-up time is required before reset to accomodate any self-heating effects. However, the voltage reference must stabilize to within ± 5% of its final value before reset. Later, the CSZ5112 may be reset at any time to initiate calibration. Reset overrides all other functions. If reset, the CSZ5112 will clear and initiate a new calibration cycle mid-conversion or mid-calibration.

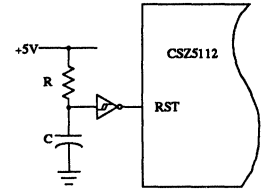


Figure 5. Power-On Reset Circuitry

Resets can be initiated in hardware or software. The simplest method of resetting the CSZ5112 involves strobing the RST pin high. When RST is brought high all internal logic clears. When it returns low a full calibration begins which takes 1,443,840 master clock cycles to complete (approximately 360ms with a 4MHz master clock). A simple power-on reset circuit can be

built using a resistor and capacitor, and a Schmidt-trigger inverter to prevent oscillation (see Figure 5). The CSZ5112 can also be reset in software when under microprocessor control. The CSZ5112 will reset whenever $\overline{CS}$, A0, and $\overline{HOLD}$ are low simultaneously. The $\overline{EOC}$ output remains high throughout the reset operation and will fall upon its completion. It can thus be used to generate an interrupt indicating the CSZ5112 is ready for operation. Six clock cycles plus 2.25µs (1.32µs for the -7 version) must be allowed after $\overline{EOC}$ falls for acquisition. Under microprocessor-independent operation with 3-states permanently enabled ($\overline{CS}$, $\overline{RD}$ low; A0 high) the $\overline{EOC}$ output will not fall at the completion of the reset operation.

Initiating Calibration

All modes of calibration can be controlled in hardware or software. Accuracy can thereby be insured at any time or temperature throughout operating life. After initial calibration at power-up, the CSZ5112's charge-redistribution design yields better temperature drift and more graceful aging than resistor-based technologies, so calibration is actually required less often than with traditional devices.

The first mode of calibration, reset, results in a single full calibration cycle. The second type of calibration, termed "burst" cal, is useful when the ADC sees some downtime but not enough to perform a full reset calibration. Burst cal can be terminated mid-calibration; it picks up where it left off previously, so calibrations can be done in piecemeal fashion. Burst is initiated by bringing the CAL input high with $\overline{CS}$ low. The CAL input is level-triggered and latches on the rising edge of $\overline{CS}$, so a write cycle can be used to control calibration in software. Burst will continue to loop through calibration cycles until terminated. Once CAL returns low, at least 26 master clock cycles plus 2.25µs (1.32µs for the -7 version) must be allowed before a conversion is initiated to ensure the CSZ5112 has completed its calibration experiment and has acquired the analog input. The $\overline{EOC}$ output indicates the completion of the final calibration experiment. (See note on page 30.)

The CSZ5112 features a background calibration mode called "interleave." Interleave appends a single calibration experiment to each conversion cycle and thus requires no dead time for calibration. The CSZ5112 gathers data between conversions and will adjust its transfer function once it completes the entire sequence of experiments (one calibration cycle per 72,192 conversions). Initiated by bringing both the $\overline{INTRLV}$ input and $\overline{CS}$ low (or hard-wiring $\overline{INTRLV}$ low), interleave extends the CSZ5112's effective conversion time by 20 master clock cycles. Other than reduced throughput, interleave is totally transparent to the user.

Burst calibrations initiated at CAL pick up where interleave left off, so calibration cycles can be hastened by "bursting" a number of experiments whenever the CSZ5112 sees free time. Interleave is subordinate to burst calibrations, so $\overline{INTRLV}$ could still be held low.

Microprocessor Interface

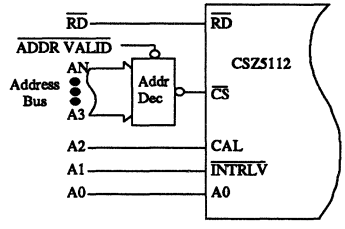


Figure 6. Address/Control Bus Connections

The CSZ5112 features an intelligent microprocessor interface which offers detailed status information and allows software control of the self-calibration functions. Output data is available in either 8- or 16-bit formats for easy interfacing to industry-standard microprocessors.

PIN	STATUS BIT	STATUS	DEFINITION
D0	S0	$\overline{\text{END OF CONVERSION}}$	Falls upon completion of a conversion, and returns high on the first subsequent read.
D1	S1	RESERVED	Reserved for factory use.
D2	S2	LOW BYTE/$\overline{\text{HIGH BYTE}}$	When data is to be read in an 8-bit format (BW=0), indicates which byte will appear at the output next.
D3	S3	$\overline{\text{END OF TRACK}}$	When low, indicates the input has been acquired to the devices specified accuracy.
D4	S4	RESERVED	Reserved for factory use.
D5	S5	TRACKING	High when the device is tracking the intput.
D6	S6	CONVERTING	High when the device is converting the held input.
D7	S7	CALIBRATING	High when the device is calibrating.

Table 2. Status Bit Definitions

Strobing both $\overline{CS}$ and $\overline{RD}$ low enables the CSZ5112's 3-state output buffers with either output data or status information depending on the status of A0. An address bit can be connected to A0 as shown in Figure 6 thereby memory mapping the status register and output data. Conversion status can be polled in software by reading the status register ($\overline{CS}$ and $\overline{RD}$ strobed low with A0 low), and masking status bits S0-S5 and S7 (by logically AND'ing the status word with 01000000) to determine the value of S6. Similarly, the software routine can determine calibration status using other status bits (see Table 2). *Care must be taken not to read the status register (A0 low) while $\overline{HOLD}$ is low, or a software reset will result* (see *Reset*, page 12).

Alternatively, the End-of-Convert ($\overline{EOC}$) output can be used to generate an interrupt or drive a DMA controller to dump the output directly into memory after each conversion. The $\overline{EOC}$ pin falls as each conversion cycle is completed and data is valid at the output. It returns high within four master clock cycles of the first subsequent data read operation or after the start of a new conversion cycle. To interface with 16-bit data busses, the BW input to the CSZ5112 should be held high and all 12 data bits read in parallel on pins D15-D4. With 8-bit buses, the converter's 12-bit result must be read in two portions. In this instance, BW should be held low and the 8 MSB's obtained on the first read cycle following a conversion. The second read cycle will yield the 4 LSB's with four trailing zeroes. Both bytes appear on pins D0-D7. The upper/lower bytes of the same data will continue to toggle on subsequent reads until the next conversion finishes. Status bit S2 indicates which byte will appear on the next data read operation.

The CSZ5112 internally buffers its output data, so data can be read while the device is tracking or converting the next sample. Retrieving the converter's digital output therefore requires no

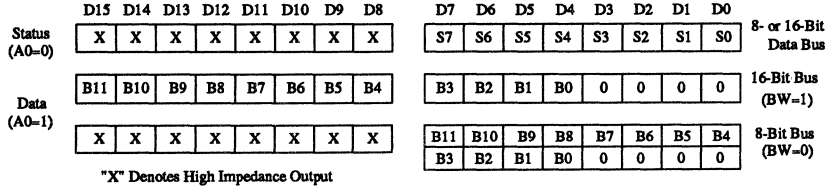


Figure 7. Data Format

reduction in ADC throughput. Enabling the 3-state outputs while the CSZ5112 is converting will not introduce conversion errors. However, using TTL loads will increase the potential for crosstalk between the analog and digital portions of the chip. This crosstalk is due to the high digital supply and signal currents arising from the TTL drive current required of each digital output. Connecting CMOS logic to the CSZ5112's digital outputs is recommended. Suitable logic families include 4000B, 74HC, 74AC, 74ACT, and 74HCT.

The two calibration control inputs, CAL and $\overline{\text{INTRLV}}$, are level-triggered and latched on the rising edge of $\overline{\text{CS}}$. Calibration can be placed under software control by connecting address lines to the CAL and $\overline{\text{INTRLV}}$ inputs as shown in Figure 6. Any read or write cycle to the CSZ5112's base address will thereby initiate or terminate calibration.

Microprocessor Independent Operation

The CSZ5112 can be operated in a stand-alone mode independent of intelligent control. In this mode, $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are hard-wired low permanently enabling the 3-state output buffers. A free-running condition is established when BW is tied high, CAL is tied low, and $\overline{\text{HOLD}}$ is continually strobed low or tied to $\overline{\text{EOT}}$. The CSZ5112's $\overline{\text{EOC}}$ output can be used to externally latch the output data if desired. With $\overline{\text{CS}}$ and $\overline{\text{RD}}$ hard-wired low, $\overline{\text{EOC}}$ will strobe low for four

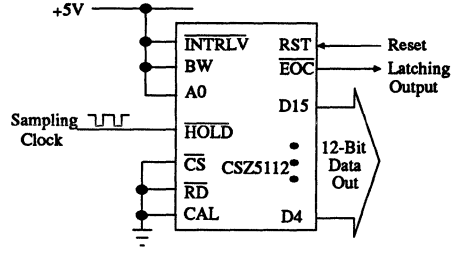


Figure 8. Microprocessor-Independent Connections

master clock cycles after each conversion. Data will be unstable up to 100ns after $\overline{\text{EOC}}$ falls, so it should be latched on the rising edge of $\overline{\text{EOC}}$.

Serial Output

All successive-approximation A/D converters derive their digital output serially starting with the MSB. The CSZ5112 presents each bit to the SDATA pin four master clock cycles after it is derived and can be latched using the serial clock output, SCLK. Just subsequent to each bit decision SCLK will fall and return high once the bit information on SDATA has stabilized. Thus, the rising edge of the SCLK output should be used to clock the data from the CSZ5112 (See Figure 9).

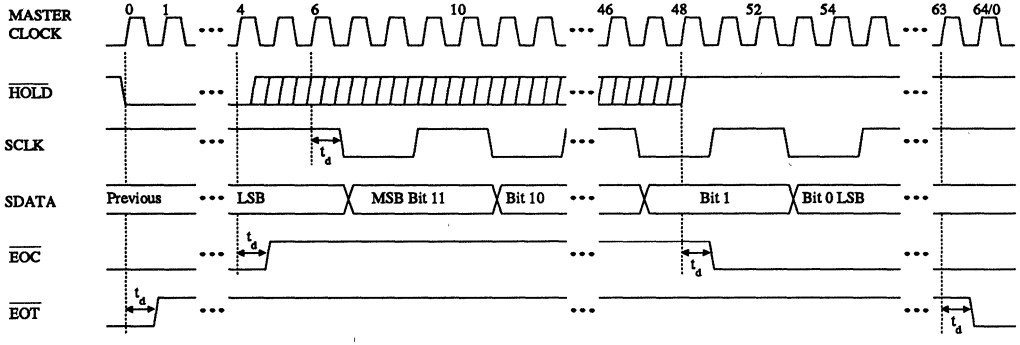
ANALOG CIRCUIT CONNECTIONS

Most popular successive-approximation A/D converters generate dynamic loads at their analog connections. The CSZ5112 internally buffers all analog inputs (AIN, VREF, and AGND) to ease the demands placed on external circuitry. However, accurate system operation still requires careful attention to details at the design stage regarding source impedances as well as grounding and decoupling schemes.

Reference Considerations

An application note titled "*Voltage References for the CS501X/CSZ511X Series of A/D Converters*" is available for the CSZ5112. In addition to working through a reference circuit design example, it offers seven built-and-tested reference circuits.

During conversion, the members of the calibrated capacitor array are switched between VREF and AGND in a manner determined by the successive-approximation algorithm. The charging and discharging of the array results in a current load at the reference. The CSZ5112



notes: 1. t_d can vary from 135ns - 235ns over military temerature range and over ± 10% supply variation.
2. For asynchronous mode, transitions of SCLK, SDATA, $\overline{EOC}$, $\overline{EOT}$ can shift by up to 4 clocks; e.g. the first high to low transition of SCLK may be on clock #6 to #9. The timing relationship between SCLK, SDATA, $\overline{EOC}$, and $\overline{EOT}$ is fixed.

Figure 9. Serial Output Timing

includes an internal buffer amplifier to minimize the external reference circuit's drive requirement and preserve the reference's integrity. Whenever the array is switched during conversion, the buffer is used to pre-charge the array thereby providing the bulk of the necessary charge. The appropriate array capacitors are then switched to the unbuffered VREF pin to avoid any errors due to offsets and/or noise in the buffer.

The external reference circuitry need only provide the residual charge required to fully charge the array after pre-charging from the buffer. This creates an ac current load as the CSZ5112 sequences through conversions. The reference circuitry must have a low enough output impedance to drive the requisite current without changing its output voltage significantly.

As the analog input signal varies, the switching sequence of the internal capacitor array changes. The current load on the external reference circuitry thus varies in response with the analog input. Therefore, the external reference must not exhibit significant peaking in its output impedance characteristic at signal frequencies or their harmonics.

A large capacitor connected between VREF and AGND can provide sufficiently low output impedance at the high end of the frequency spectrum, while almost all precision references exhibit extremely low output impedance at dc. The presence of large capacitors on the output of some voltage references, however, may cause peaking in the output impedance at intermediate frequencies. Care should be exercised to ensure that significant peaking does not exist or that some form of compensation is provided to eliminate the effect.

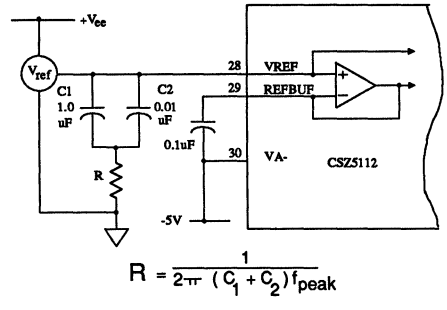


Figure 10. Reference Connections

The magnitude of the current load on the external reference circuitry will scale to the master clock frequency. At full speed (4MHz clock), the reference must supply a maximum load current of 10µA peak-to-peak (1µA typical). An output impedance of 15Ω will therefore yield a maximum error of 150µV. With a 2.5V reference and LSB size of 0.6mV, this would insure better than 1/4 LSB accuracy. A 1µF capacitor exhibits an impedance of less than 15Ω at frequencies greater than 10kHz. A high-quality tantalum capacitor in parallel with a smaller ceramic capacitor is recommended.

Peaking in the reference's output impedance can occur due to capacitive loading at its output. Any peaking can be reduced by placing a small resistor in series with the capacitors (Figure 10). The equation in Figure 10 can be used to help calculate the optimum value of R for a particular reference. The term "f_{peak}" is the frequency of the peak in the output impedance of the reference before the resistor is added.

The CSZ5112 can operate with a wide range of reference voltages, but signal-to-noise performance is maximized by using as wide a signal range as possible. The recommended reference voltage is between 2.5 and 4.5 volts. The CSZ5112 can actually accept reference voltages up to the positive analog supply. However, the buffer's offset may increase as the reference voltage approaches VA+ thereby increasing external drive requirements at VREF. Thus, a 4.5V reference is the maximum voltage recommended. Also, the buffer enlists the aid of an external 0.1µF ceramic capacitor which must be tied between its output, REFBUF, and the negative analog supply, VA-. For more information on references, consult "Application Note: *Voltage References for the CS501X/ CSZ511X Series of A/D Converters*".

Analog Input Connection

The analog input terminal functions similarly to the VREF input after each conversion when switching into the track mode. During the first six master clock cycles in the track mode, the buffered version of the analog input is used for pre-charging the capacitor array. An additional period is required for fine-charging directly from AIN to obtain the specified accuracy. Figure 11 exemplifies this operation. During pre-charge the charge on the capacitor array first settles to the buffered version of the analog input. This voltage is offset from the actual input voltage. During fine-charge, the charge then settles to the accurate unbuffered version.

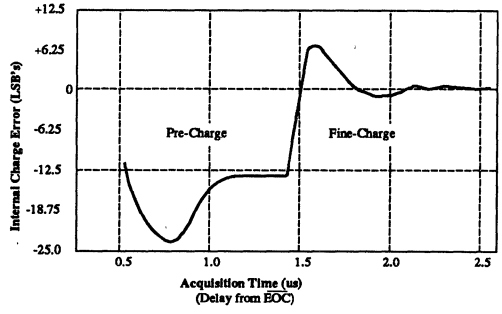


Figure 11. Internal Acquisition Time

The acquisition time of the CSZ5112 depends on the master clock frequency due to the fixed pre-charge period. For instance, operating the -12 version with an external 4MHz master clock results in a 3.75µs acquisition time: 1.5µs for pre-charging (6 clock cycles) and 2.25µs for fine-charging. Fine-charge settling is specified as a maximum of 2.25µs for an analog source impedance of less than 200Ω. (On the -7 version it is specified as 1.32µs.)

In addition, the comparator requires a source impedance of less than 400Ω around 2MHz for stability, which is met by practically all bipolar

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op amps. Large dc source impedances can be accommodated by adding capacitance from AIN to ground (typically 200pF) to decrease source impedance at high frequencies. However, high dc source resistances will increase the input's RC time constant and extend the necessary acquisition time.

The CSZ5112 can track full power signals up to 32kHz in the track mode. During the first six clock cycles following a conversion (pre-charge), the CSZ5112 is capable of slewing at 5V/µs in unipolar mode. In bipolar mode, only half the capacitor array is connected to the analog input so the CSZ5112 can slew at 10V/µs. After the first six master clock cycles, it will slew at 0.25V/µs in the unipolar mode and 0.5V/µs in bipolar mode. Acquisition of fast slewing signals (step functions) can be hastened if the step occurs during or immediately following the conversion cycle. For instance, channel selection in multiplexed applications should occur while the CSZ5112 is converting (see Figure 12). Multiplexer settling is thereby removed from the overall throughput equation, and the CSZ5112 can convert at full speed.

Analog Input Range/Coding Format

The reference voltage directly defines the input voltage range in both the unipolar and bipolar configurations. In the unipolar configuration (BP/$\overline{UP}$ low), the first code transition occurs 0.5 LSB above AGND, and the final code transition occurs 1.5 LSB's below VREF. Coding is in straight binary format. In the bipolar configuration (BP/$\overline{UP}$ high), the first code transition occurs 0.5 LSB above -VREF and the last transition occurs 1.5 LSB's below +VREF. Coding is in an offset-binary format. Positive full scale gives a digital output of 1111111111111111, and negative full scale gives a digital output of 0000000000000000.

Grounding and Power Supply Decoupling

The CSZ5112 uses the analog ground connection, AGND, only as a reference voltage. No dc power currents flow through the AGND connection, and it is completely independent of DGND. However, any noise riding on the AGND input relative to the system's analog ground will induce conversion errors. Therefore, both the analog input and reference voltage should be referred to the AGND pin, which should be used as the entire system's analog ground.

The digital and analog supplies are isolated within the CSZ5112 and are pinned out separately to minimize coupling between the analog and digital sections of the chip. All four supplies should be decoupled to their respective grounds using 0.1µF ceramic capacitors. If sig-

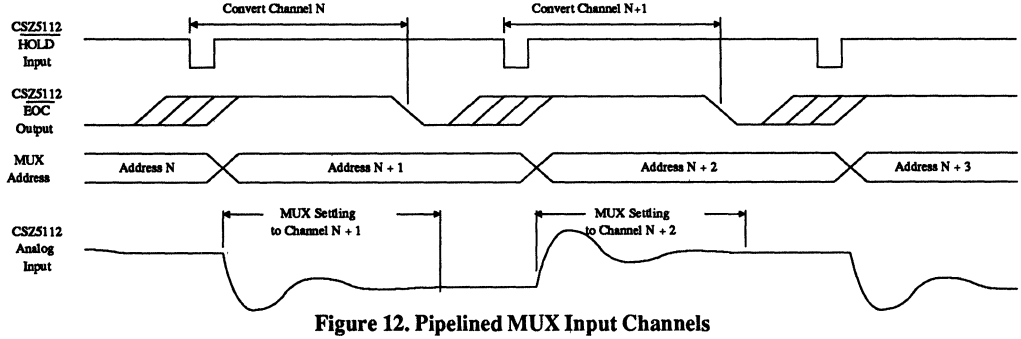

Figure 12. Pipelined MUX Input Channels

nificant low-frequency noise is present on the supplies, 1µF tantalum capacitors are recommended in parallel with the 0.1µF capacitors.

The positive digital power supply of the CSZ5112 must never exceed the positive analog supply by more than a diode drop or the CSZ5112 could experience permanent damage. If the two supplies are derived from separate sources, care must be taken that the analog supply comes up first at power-up. The system connection diagram on page 24 shows a decoupling scheme which allows the CSZ5112 to be powered from a single set of ± 5V rails. The positive digital supply is derived from the analog supply through a 10Ω resistor (rather than vice versa) to avoid the analog supply dropping below the digital supply. If this scheme is utilized, care must be taken to insure that any digital load currents (which flow through the 10Ω resistors) do not cause the digital supplies to drop below their minimum specification of ± 4.5V.

As with any high-precision A/D converter, the CSZ5112 requires careful attention to grounding and layout arrangements. However, no unique layout issues must be addressed to properly apply the CSZ5112. The CDB5112 evaluation board is available for the CSZ5112, which avoids the need to design, build, and debug a high-precision PC board to initially characterize the part. The board comes with a socketed CSZ5112, and can be quickly reconfigured to simulate any combination of sampling, calibration, master clock, and analog input range conditions.

CSZ5112 PERFORMANCE

The CSZ5112 offers 100% tested dynamic performance. Due to the broad range of operating conditions and performance requirements in signal processing applications, the following section is included to illustrate the CSZ5112's error sources and their effect on a signal's spectral content.

FFT Tests and Windowing

In the factory, the CSZ5112 is tested using Fast Fourier Transform (FFT) techniques to analyze the converter's dynamic performance. A pure sinewave is applied to the CSZ5112, and a "time record" of 1024 samples is captured and processed. The FFT algorithm analyzes the spectral content of the digital waveform and distributes its energy among 512 "frequency bins". Assuming an ideal sinewave, distribution of energy in bins outside of the fundamental and dc can only be due to quantization effects and errors in the CSZ5112.

If sampling is not synchronized to the input sinewave, it is highly unlikely that the time record will contain an integer number of periods of the input signal. However, the FFT assumes that the signal is periodic, and will calculate the spectrum of a signal that appears to have large discontinuities, thereby yielding a severely distorted spectrum. To avoid this problem, the time record is multiplied by a window function prior to performing the FFT. The window function smoothly forces the endpoints of the

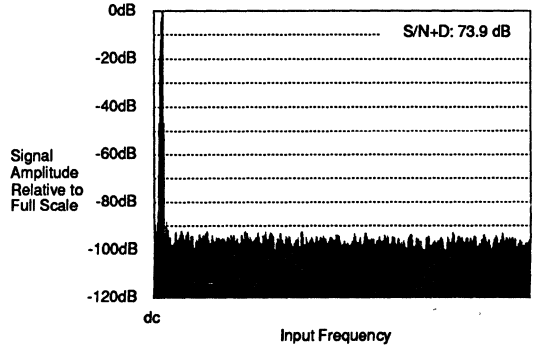

Figure 13. FFT Plot of Ideal 12-bit Signal

time record to zero, thereby removing the discontinuities. The effect of the window in the frequency-domain is to convolute the spectrum of the window with that of the actual input.

The quality of the window used for harmonic analysis is typically judged by its highest side-lobe level. The Blackman-Harris window used for testing the CSZ5112 has a maximum side-lobe level of -92dB. Figure 13 shows an FFT computed from an ideal 12-bit sinewave multiplied by a Blackman-Harris window. Artifacts of windowing are discarded from the signal-to-noise calculation using the assumption that all noise sources are white. All FFT plots in this data sheet were derived by averaging the FFT results from ten time records. This filters the spectral variability that can arise from capturing finite time records without disturbing the total energy outside the fundamental. All harmonics which exist above the noise floor are therefore more clearly visible in the plots. For more information on FFT's and windowing refer to:

F.J.HARRIS, "On the use of windows for harmonic analysis with the Discrete Fourier Transform", Proc.IEEE, Vol.66, No.1, Jan 1978, pp.51-83.

Nonlinearity

Analog-to-digital converters have traditionally been specified using dc specifications such as Integral and Differential Nonlinearity at worst-case points on the transfer curve. These specifications are not particularly useful in signal processing applications since they offer little information on the overall shape of converter's transfer curve, and therefore do not directly correlate to the converter's effect on a signal's spectral content.

Integral Nonlinearity (INL; also termed Relative Accuracy or just Nonlinearity) is defined as the deviation of the transfer function from an ideal straight line. Bows and waves in the transfer curve generate harmonic distortion. However, the most prevalent source of nonlinearity in high-resolution converters is bit-weight errors; that is, the deviation of bits from their ideal binary-weighted ratios. At dc, bit-weight errors most visibly affect the converter's Differential Nonlinearity, or the deviation of codes from their ideal widths. Due to the limitations of factory trim techniques, the worst-case condition of bit-weight errors has traditionally also defined the point of maximum INL.

Bit-weight errors have a drastic effect on a converter's ac performance. They can be analyzed as step functions superimposed on the input signal. Since bits (and their errors) switch in and out throughout the transfer curve, their effect is signal dependent. That is, harmonic and intermodulation distortion, as well as noise, can vary with different input conditions. Designing a system around characterization data is risky since transfer curves can differ drastically unit-to-unit and lot-to-lot.

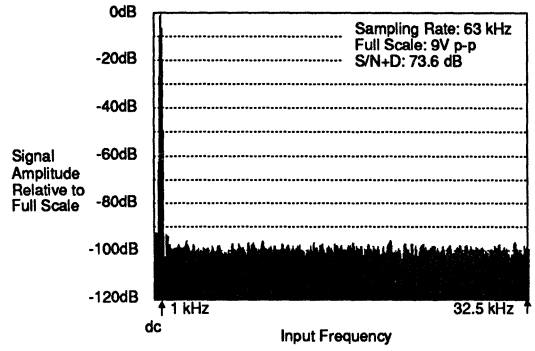

Figure 14. FFT Plot with 1kHz, Full-Scale Input

The CSZ5112 achieves repeatable signal-to-noise and harmonic distortion performance using an on-chip self-calibration scheme. The CSZ5112 calibrates its bit weights to a small

fraction of an LSB at 12-bits yielding peak distortion below the noise floor (see Figure 14). Unlike traditional ADC's, the linearity of the CSZ5112 is not limited by bit-weight errors; its performance is therefore extremely repeatable and independent of input signal conditions.

Sampling Distortion

The ultimate limitation on the CSZ5112's linearity (and distortion) arises from nonideal sampling of the analog input voltage. The calibrated capacitor array used during conversions is also used to track and hold the analog input signal. The conversion is not performed on the analog input voltage per se, but is actually performed on the charge trapped on the capacitor array at the moment the $\overline{HOLD}$ command is given. The charge on the array is ideally related to the analog input voltage by $Q_{in} = -V_{in} \times C_{tot}$ as shown in Figure 2. Any deviation from this ideal relationship will result in conversion errors even if the conversion process proceeds flawlessly.

At dc, the DAC capacitor array's voltage coefficient dictates the converter's linearity. This variation in capacitance with respect to applied signal voltage yields a nonlinear relationship between charge Q_{in} and the analog input voltage

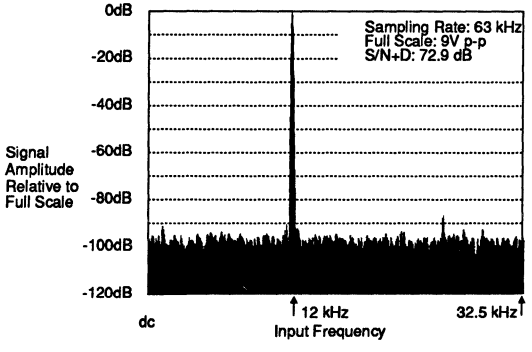

Figure 15. FFT Plot of 12kHz, Full-Scale Input

V_{in} and places a bow or wave in the transfer function. This is the dominant source of distortion at low input frequencies.

The ideal relationship between Q_{in} and V_{in} can also be distorted at high signal frequencies due to nonlinearities in the internal MOS switches. Dynamic signals cause ac current to flow through the switches connecting the capacitor array to the analog input pin in the track mode. Nonlinear on-resistance in the switches causes a nonlinear voltage drop. This effect worsens with increased signal frequency since the magnitude of the steady state current increases. It assumes a linear relationship with input frequency and is illustrated in Figure 15 (the second harmonic at 24kHz).

This distortion is strictly an ac sampling phenomenon. If significant energy exists at high frequencies, the effect can be eliminated using an external track-and-hold amplifier to create an effective dc input. Delaying the $\overline{HOLD}$ signal to the CSZ5112 slightly from the sampling signal to the track-and-hold amplifier will allow the array's charge current to decay, thereby eliminating any voltage drop across the switches. Since the CSZ5112 has a second sampling function on-chip, the external track-and-hold can return to the track mode once the converter's $\overline{HOLD}$ input falls. It need only acquire the analog input by the time the entire conversion cycle finishes.

Quantization Noise

The error due to quantization of the analog input ultimately dictates the accuracy of any A/D converter. The continuous analog input must be represented by one of a finite number of digital codes, so the best accuracy to which an analog input can be known from its digital code is ± 1/2 LSB. Under circumstances commonly encountered in signal processing applications, this quantization error can be treated as a random variable. The magnitude of the error is limited to

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± 1/2 LSB, but any value within this range has equal probability of occurrence. Such a probability distribution leads to an error "signal" with an rms value of 1 LSB/$\sqrt{12}$. Using an rms signal value of FS/$\sqrt{8}$ (amplitude = FS/2), this relates to an ideal 12-bit signal-to-noise ratio of 74dB (6.02*N* + 1.76dB, where *N* is the number of bits).

Equally important is the spectral content of this error signal. It can be shown to be approximately white, with its energy spread uniformly over the band from dc to one-half the sampling rate. Advantage of this characteristic can be made by judicious use of filtering. If the signal is bandlimited, much of the quantization error can be filtered out, and improved system performance can be attained. As illustrated in Figures 14 and 15, the CSZ5112's on-chip self-calibration provides very accurate bit weights which yield nearly ideal 12-bit performance.

Clock Feedthrough

Maintaining the integrity of analog signals in the presence of digital switching noise is a difficult problem. The CSZ5112 can be synchronized to the digital system using the CLKIN input to avoid conversion errors due to asynchronous interference. However, digital interference will still affect sampling purity due to coupling between the CSZ5112's analog input and master clock.

Master Clock		Analog Input	Clock Feedthrough	
Int/Ext	Freq	Source Impedance	RMS	Peak-to-Peak
Internal	2MHz	50 Ω	15uV	70uV
External	2MHz	50 Ω	25uV	110uV
External	4MHz	50 Ω	40uV	150uV
External	4MHz	25 Ω	25uV	110uV
External	4MHz	200Ω	80uV	325uV

Figure 16. Examples of Measured Clock Feedthrough

The effect of clock feedthrough depends on the sampling conditions. If the sampling signal at the $\overline{HOLD}$ input is synchronized to the master clock, clock feedthrough will appear as a dc offset at the CSZ5112's output. The offset could theoretically reach the peak coupling magnitude (Figure 16), but the probability of this occurring is small since the peaks are spikes of short duration.

$$f_{tone} = (Nf_s - f_{clk})$$

where $N = f_{clk}/f_s$ rounded to the nearest integer

If sampling is performed asynchronously with the master clock, clock feedthrough will appear as an ac error at the CSZ5112's output. With a fixed sampling rate, a tone will appear as the clock frequency aliases into the baseband. The tone frequency can be calculated using the equation below and could be selectively filtered in software using DSP techniques.

The magnitude of clock feedthrough depends on the master clock conditions and the source impedance applied to the analog input. When operating with the CSZ5112's internally-generated clock, the CLKIN input is grounded and the dominant source of coupling is through the device's substrate. As shown in Figure 16, a typical CSZ5112 operating with its internal oscillator at 2MHz and 50Ω of analog input source impedance will exhibit only 15μV rms of clock feedthrough (-116dB with a 9V p-p full scale). However, if a 2MHz external clock is applied to CLKIN under the same conditions, feedthrough increases to 25uV rms (-111dB). Feedthrough also increases with clock frequency; a 4MHz clock yields 40μV rms (-107dB).

Clock feedthrough can be reduced by limiting the source impedance applied at the analog input. As shown in Figure 16, reducing source impedance from 50Ω to 25Ω yields a 15μV rms

reduction in feedthrough. Therefore, when operating the CSZ5112 with high-frequency external master clocks, it is important to minimize source impedance applied to the CSZ5112's input.

Also, the overall effect of clock feedthrough can be minimized by maximizing the input range and LSB size. The reference voltage applied to VREF can be maximized, and the CSZ5112 can be operated in bipolar mode which inherently doubles the LSB size over the unipolar mode.

Aperture Jitter

Track-and-hold amplifiers commonly exhibit two types of aperture jitter. The first, more appropriately termed "aperture window", is an input voltage dependent variation in the aperture delay. Its signal-dependancy causes distortion at high frequencies. The CSZ5112's proprietary architecture avoids applying the input voltage across a sampling switch, thus avoiding any "aperture window" effects. The second type of aperture jitter assumes a random nature and appears in an FFT as a spreading in the fundamental. With only 100ps peak-to-peak aperture jitter, the CSZ5112 can process full-scale signals well above the Nyquist rate with 12-bit accuracy.

Power Supply Rejection

The CSZ5112's power supply rejection performance is enhanced by the on-chip self-calibration and an "auto-zero" process. Drifts in power supply voltages at frequencies less than the calibration rate have negligible effect on the CSZ5112's accuracy. This, of course, is because the CSZ5112 adjusts its offset to within a small fraction of an LSB during calibration.

Above the calibration frequency the excellent power supply rejection of the internal amplifiers is augmented by an auto-zero process. Any offsets are stored on the capacitor array and are effectively subtracted once conversion is initiated. Figure 17 shows power supply rejection of the CSZ5112 in the bipolar mode with the analog input grounded and a 300mV p-p ripple applied to each analog supply. Power supply rejection improves by 6dB in the unipolar mode.

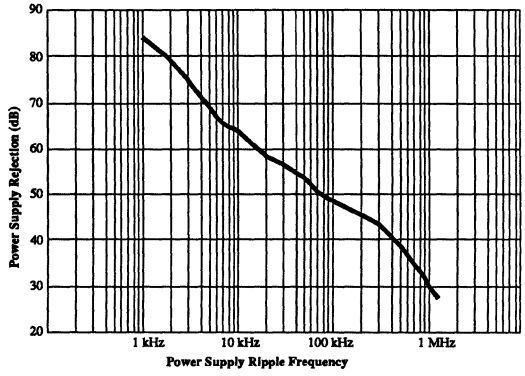


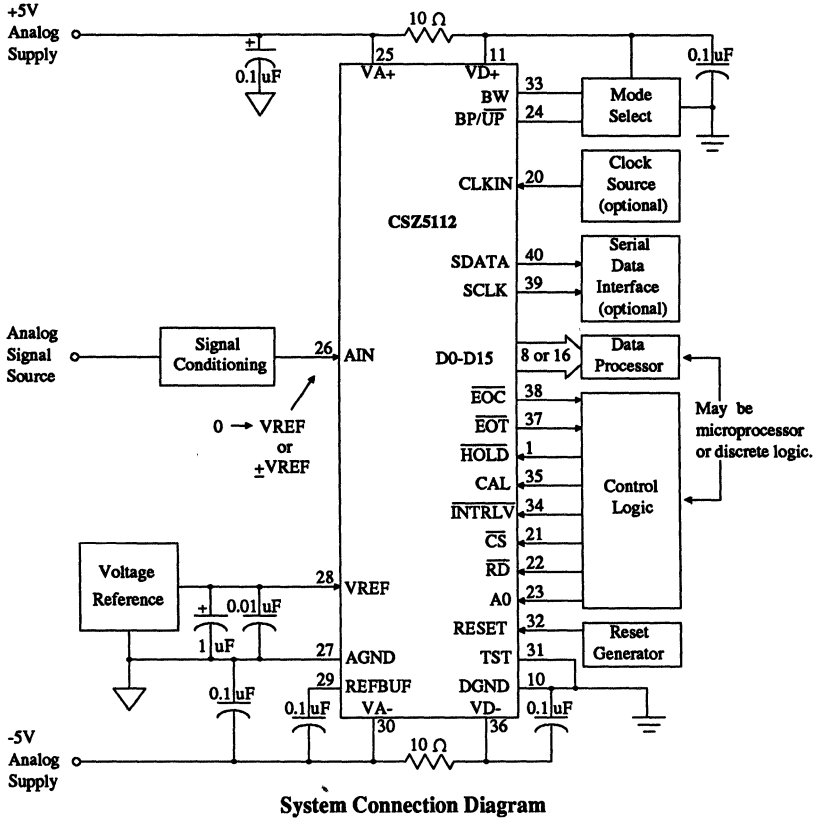
Figure 17. Power Supply Rejection

Notches of increased rejection arise from the auto-zeroing at the conversion rate. The frequencies at which these notches occur also depend on the value of the captured analog input. The line shows worst-case rejection for all combinations of conversion rates and input conditions in the bipolar mode. Again, power supply rejection is 6dB better in the unipolar mode.

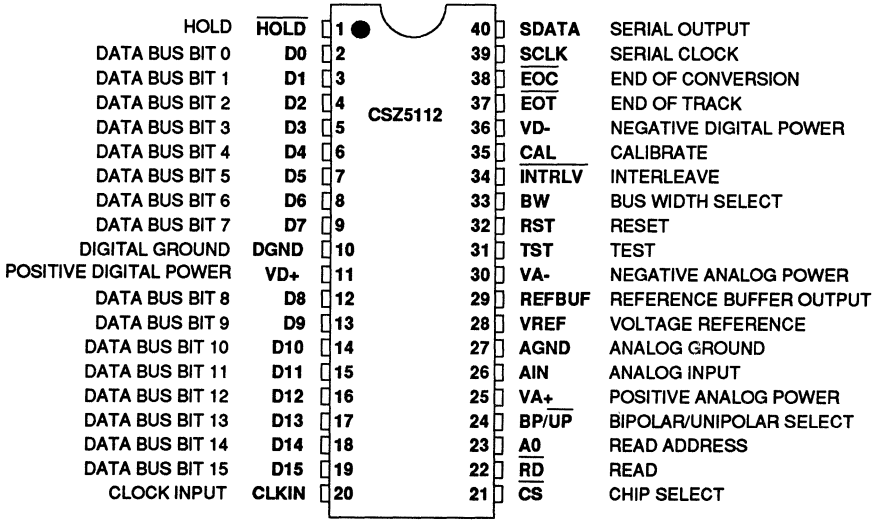
$\overline{HOLD}$	$\overline{CS}$	CAL	$\overline{INTRLV}$	$\overline{RD}$	A0	RST	Function
↓	X	X	X	X	*	0	Hold and Start Convert
X	0	1	X	X	*	0	Initiate Burst Calibration
1	0	0	X	X	*	0	Stop Burst Cal and Begin Track
X	0	X	0	X	*	0	Initiate Interleave Calibration
X	0	X	1	X	*	0	Terminate Interleave Cal
X	0	X	X	0	1	0	Read Output Data
1	0	X	X	0	0	0	Read Status Register
X	1	X	X	X	*	X	High Impedance Data Bus
X	X	X	X	1	*	X	High Impedance Data Bus
X	X	X	X	X	X	1	Reset
0	0	X	X	X	0	X	Reset

* The status of A0 is not critical to the operation specified. However, A0 should not be low with $\overline{CS}$ and $\overline{HOLD}$ low, or a software reset will result.

CSZ5112 Truth Table



System Connection Diagram



PIN DESCRIPTIONS

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Power Supply Connections

VD+ - Positive Digital Power, PIN 11.
Positive digital power supply. Nominally +5 volts.

VD- - Negative Digital Power, PIN 36.
Negative digital power supply. Nominally -5 volts.

DGND - Digital Ground, PIN 10.
Digital ground reference.

VA+ - Positive Analog Power, PIN 25.
Positive analog power supply. Nominally +5 volts.

VA- - Negative Analog Power, PIN 30.
Negative analog power supply. Nominally -5 volts.

AGND - Analog Ground, PIN 27.
Analog ground reference.

Oscillator

CLKIN - Clock Input, PIN 20.

All conversions and calibrations are timed from a master clock which can either be supplied by driving this pin with an external clock signal, or can be internally generated by tying this pin to DGND.

Digital Inputs

$\overline{\text{HOLD}}$ - Hold, PIN 1.

A falling transition on this pin sets the CSZ5112 to the hold state and initiates a conversion. This input must remain low at least one master clock cycle plus 50ns.

$\overline{\text{CS}}$ - Chip Select, PIN 21.

When high, the data bus outputs are held in a high impedance state and the inputs to CAL and $\overline{\text{INTRLV}}$ are ignored. A falling transition initiates or terminates burst or interleave calibration (depending on the status of CAL and $\overline{\text{INTRLV}}$) and a rising transition latches both the CAL and $\overline{\text{INTRLV}}$ inputs. If $\overline{\text{RD}}$ is low, the data bus is driven as indicated by BW and A0.

$\overline{\text{RD}}$ - Read, PIN 22.

When $\overline{\text{RD}}$ and $\overline{\text{CS}}$ are both low, data is driven onto the data bus. If either signal is high, the data bus outputs are held in a high impedance state. The data driven onto the bus is determined by BW and A0.

A0 - Read Address, PIN 23.

Determines whether data or status information is placed onto the data bus. When high during the read operation, converted data is placed onto the data bus; when low, the status register is driven onto the bus.

BP/$\overline{\text{UP}}$ - Bipolar/Unipolar Input Select, PIN 24.

When high, the device is configured with a bipolar transfer function ranging from -VREF to +VREF. Encoding is in an offset binary format, with the mid-scale code 100...0000 centered at AGND. When low, the device is configured for a unipolar transfer function from AGND to VREF. Unipolar coding is in straight binary format.

RST - Reset, PIN 32.

When taken high, all internal digital logic is reset. Upon returning low, a full calibration sequence is initiated.

BW - Bus Width Select, PIN 33.

When high, all 12 data bits are driven onto the bus simultaneously during a data read cycle. When low, the bus is in a byte wide format. On the first read following a conversion, the eight MSB's are driven onto D7-D0. A second read cycle places the four LSB's with four trailing zeroes on D7-D0. Subsequent reads will toggle the higher/lower order bytes of the same data until the next conversion completes. Regardless of BW's status, a read cycle with A0 low yields the status information on D7-D0.

$\overline{\text{INTRLV}}$ - Interleave, PIN 34.

When latched low using $\overline{CS}$, the device goes into interleave calibration mode. A full calibration will complete every 72,192 conversions. The effective conversion time extends by 20 clock cycles.

CAL - Calibrate, PIN 35. (See note on page 30.)

When latched high using $\overline{CS}$, burst calibration results. The device cannot perform conversions during the calibration period which will terminate only once CAL is latched low again. Calibration picks up where the previous calibration left off, and calibration cycles complete every 1,443,840 master clock cycles. If the device is converting when a calibration is signaled, it will wait until that conversion completes before beginning calibration.

Analog Inputs

AIN - Analog Input, PIN 26.

Input range in unipolar mode is zero volts to VREF. Input range in bipolar mode is -VREF to +VREF. The output impedance of buffer driving this input should be less than or equal to 200Ω.

VREF - Voltage Reference, PIN 28.

The analog reference voltage which sets the analog input range. It represents positive full scale for both bipolar and unipolar operation, and its magnitude sets negative full scale in bipolar mode.

Digital Outputs

D0 through D15 - Data Bus Outputs, PINS 2 thru 9, 12 thru 19.

3-state output pins. Enabled by $\overline{CS}$ and $\overline{RD}$, they offer the converter's 12-bit output in a format consistent with the state of BW if A0 is high. If A0 is low, bits D0-D7 offer the status register.

$\overline{\text{EOT}}$ - End Of Track, PIN 37.

If low, indicates that enough time has elapsed since the last conversion for the device to acquire the analog input signal (3.75μs for 4MHz external clock).

$\overline{EOC}$ - End Of Conversion, PIN 38.

This output indicates the end of a conversion or reset calibration cycle. It is high during a conversion and will fall to a low state upon completion of the conversion cycle indicating valid data is available at the output. Returns high on the first subsequent read or the start of a new conversion cycle.

SDATA - Serial Output, PIN 40.

Presents each output data bit after it is determined by the successive approximation algorithm. Valid on the rising edge of SCLK, data appears MSB first, LSB last, and each bit remains valid until the next bit appears.

SCLK - Serial Clock Output, PIN 39.

Used to clock converted output data serially from the CSZ5112. Serial data is stable on the rising edge of SCLK.

Analog Outputs

REFBUF - Reference Buffer Output, PIN 29.

Reference buffer output. A 0.1µF ceramic capacitor must be tied between this pin and VA-.

Miscellaneous

TST - Test, PIN 31.

Allows access to the CSZ5112's test functions which are reserved for factory use. Must be tied to DGND.

ERROR DEFINITIONS

Peak Harmonic or Spurious Noise (More accurately, Signal to Peak Harmonic or Spurious Noise) - The ratio of the rms value of the signal to the rms value of the next largest spectral component below the Nyquist rate (excepting dc). This component is often an aliased harmonic when the signal frequency is a significant proportion of the sampling rate. Expressed in decibels.

Total Harmonic Distortion - The ratio of the rms sum of all harmonics to the rms value of the signal. Units in percent.

Signal-to-Noise Ratio - Ratio of the rms value of the signal to the rms sum of all other spectral components below the Nyquist rate (excepting dc), including distortion components. Expressed in decibels.

Full Scale Error - The deviation of the last code transition from the ideal (VREF-3/2 LSB's) after all offsets have been externally compensated. Units in LSB's.

Unipolar Offset - The deviation of the first code transition from the ideal (1/2 LSB above AGND) when in unipolar mode (BP/$\overline{UP}$ low). Units in LSB's.

Bipolar Offset - The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below AGND) when in bipolar mode (BP/$\overline{UP}$ high). Units in LSB's.

Bipolar Zero - The deviation of the first code transition from the ideal (1/2 LSB above -VREF) when in bipolar mode (BP/$\overline{UP}$ high). Units in LSB's.

7

Aperture Time - The time required after the hold command for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

Aperture Jitter - The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

Note: Temperatures specified define ambient conditions in free-air during test and do not refer to the junction temperature of the device.

Ordering Guide

Model	Throughput	Temp Range	Package
CSZ5112-KP24	34 kHz	0 to 70 °C	40-Pin Plastic DIP
CSZ5112-KP12	63 kHz	0 to 70 °C	40-Pin Plastic DIP
CSZ5112-KP7	100 kHz	0 to 70 °C	40-Pin Plastic DIP
CSZ5112-BC24	34 kHz	-40 to +85 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5112-BC12	63 kHz	-40 to +85 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5112-BC7	100 kHz	-40 to +85 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5112-TC24	34 kHz	-55 to +125 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5112-TC12	63 kHz	-55 to +125 °C	40-Pin Ceramic Side-Brazed DIP

ADDENDUM

Burst Calibration

Burst calibration mode allows control of partial calibration cycles. Due to an unforeseen condition inside the part, asynchronous termination of calibration (CAL brought low) may result in a sub-optimal calibration result. It is recommended that burst calibration is not used, until the silicon is revised to prevent this effect.

The reset and interleave mode work perfectly, and should be used instead of burst mode. The CSZ5112's very low drift over temperature means that, under most circumstances, calibration need only be performed at power-up, using reset.

If you wish to use burst calibration, then please contact the factory for advice and new part availability information.

Semiconductor Corporation

CSZ5114

14-Bit, 56kHz Sampling A/D Converter

Features

- Monolithic CMOS A/D Converter
  - Inherent Sampling Architecture
  - 3-State Output Buffers
  - Microprocessor Interface
- Sampling Rates up to 56kHz
- Ultra-Low Distortion
  - Total Harmonic Distortion: 0.003%
  - Peak Harmonic or Noise: −98dB
- Low Power Dissipation: 120mW
- Pin Compatible with CSZ5112/CSZ5116

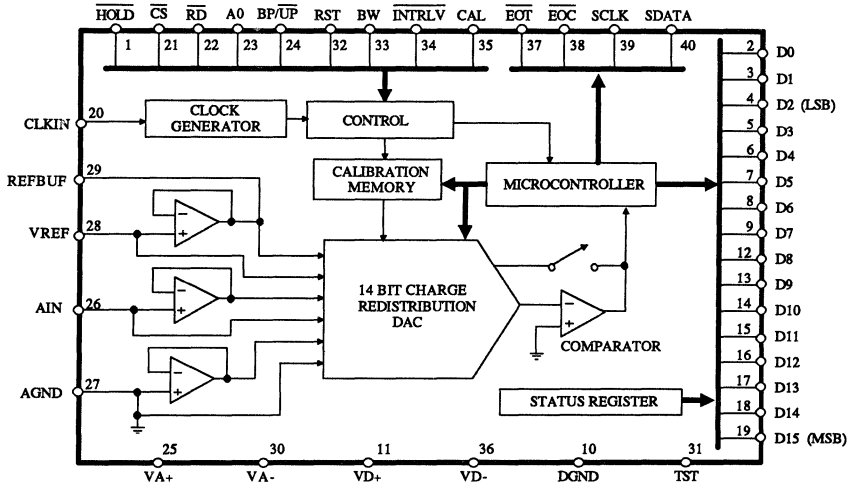
General Description

The CSZ5114 CMOS analog-to-digital converter is an ideal front end for single- or multi-channel digital signal processing systems. It needs no external sample/hold amplifier at its input to convert ac signals - the sampling function is inherent to its charge redistribution design.

Using a standard successive-approximation algorithm, the CSZ5114 sequences through a 14-bit conversion in 14.25 microseconds. With 3.75 microseconds needed between conversions for acquisition, the CSZ5114 can support throughput rates up to 56kHz. It is therefore ideal for processing audioband signals.

The CSZ5114 features an on-chip self-calibration scheme which calibrates its bit weights to true 14-bit accuracy. This insures low distortion and maintains good signal-to-noise performance with low-level signals.

ORDERING INFORMATION: Page 59



S-to-Z™ Converter

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, Texas 78760
(512)445-7222 TWX:910-874-1352

ANALOG CHARACTERISTICS

(T_A = 25°C; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 4.5V;
Full-Scale Input Sinewave, 1kHz; f_{clk} = 4MHz for -14, 2MHz for -28; f_s = 56kHz for -14, 30kHz for -28;
Bipolar Mode ; Analog Source Impedance = 200Ω unless otherwise specified)

Parameter*	CSZ5114-K min	CSZ5114-K typ	CSZ5114-K max	CSZ5114-B min	CSZ5114-B typ	CSZ5114-B max	CSZ5114-T min	CSZ5114-T typ	CSZ5114-T max	Units
Specified Temperature Range		0 to 70			-40 to +85			-55 to +125		°C
Dynamic Performance										
Peak Harmonic or Spurious Noise										
1kHz Input T_{min} to T_{max}	94	98		94	98		94	98		dB
12kHz Input (Note 1)	84	87		84	87		84	87		dB
Total Harmonic Distortion		0.003			0.003			0.003		%
Signal-to-Noise Ratio										
0dB Input T_{min} to T_{max}	82	84		82	84		82	84		dB
-60dB Input (Note 2)		23			23			23		dB
dc Accuracy										
Differential Linearity (Note 3)	14			14			14			Bits
Full Scale Error T_{min} to T_{max}		± 1/2			± 1/2			± 1/2		LSB
Unipolar Offset T_{min} to T_{max}		± 1/4			± 1/4			± 1/4		LSB
Bipolar Offset T_{min} to T_{max}		± 1/4			± 1/2			± 1/2		LSB
Bipolar Zero Error T_{min} to T_{max}		± 1/2			± 1/2			± 1/2		LSB
Analog Input										
Aperture Time		25			25			25		ns
Aperture Jitter		100			100			100		ps
Full Power Bandwidth (Note 4)		28			28			28		kHz
Input Capacitance Unipolar Mode		275	375		275	375		275	375	pF
(Note 5) Bipolar Mode		165	220		165	220		165	220	pF

Notes:
1. All T_{min} to T_{max} specifications apply after calibration at the temperature of interest.
2. A detailed plot of S/(N+D) vs. input amplitude appears on page 49.
3. Minimum Resolution for which no missing codes is guaranteed.
4. Refer to the *Analog Input* section on page 45 for a discussion of input slew capabilities.
5. Applies only in the track mode. When converting or calibrating, input capacitance will not exceed 10pF.

*Refer to *Error Definitions* on page 58.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter	CSZ5114-K min	typ	max	CSZ5114-B min	typ	max	CSZ5114-T min	typ	max	Units
Conversion & Throughput										
Conversion Time −14			14.25			14.25			14.25	us
(Notes 6, 7) −28			28.5			28.5			28.5	us
Acquisition Time −14		3.0	3.75		3.0	3.75		3.0	3.75	us
(Note 7) −28		4.5	5.25		4.5	5.25		4.5	5.25	us
Throughput −14	55.6			55.6			55.6			kHz
(Note 7) −28	29.6			29.6			29.6			kHz
Power Supplies										
Power Supply Currents (Note 8)										
I_{A+}		9	19		9	19		9	19	mA
I_{A-}		- 9	- 19		- 9	- 19		- 9	- 19	mA
I_{D+}		3	6		3	6		3	6	mA
I_{D-}		- 3	- 6		- 3	- 6		- 3	- 6	mA
Power Dissipation (Note 8)		120	250		120	250		120	250	mW
Power Supply Rejection (Note 9)										
Positive Supplies		84			84			84		dB
Negative Supplies		84			84			84		dB

Notes:
6. Measured from falling transition on $\overline{HOLD}$ to falling transition on $\overline{EOC}$.
7. Conversion, acquisition, and throughput times depend on the master clock, sampling, and calibration conditions. The numbers shown assume sampling and conversion is synchronized with the CSZ5114's internal conversion clock, interleave calibrate is disabled, and operation is from the full-rated external master clock. A detailed discussion of conversion timing appears on page 39.
8. All outputs unloaded. All inputs CMOS levels.
9. With 300mV p-p, 1kHz ripple applied to each supply separately in the bipolar mode. Rejection improves by 6dB in the unipolar mode to 90dB. A plot of typical power supply rejection appears on page 52.

7

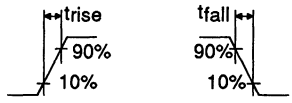
SWITCHING CHARACTERISTICS

($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; Logic 0 = 0V; Logic 1 = VD+; C_L = 50pF)

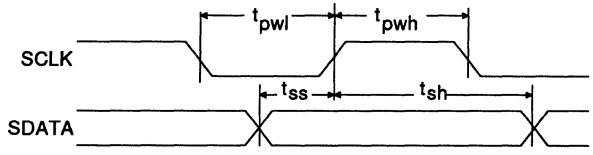
Parameter	Symbol	Min	Typ	Max	Units
Master Clock Frequency:					
Internally Generated: -14	f_{CLK}	2	-	-	MHz
-28		1	-	-	
Externally Supplied: -14		-	-	4	
-28		-	-	2	
Master Clock Duty Cycle	-	30	-	70	%
Rise Times: Any Digital Input	t_{rise}	-	-	1.0	us
Any Digital Output		-	20	-	ns
Fall Times: Any Digital Input	t_{fall}	-	-	1.0	us
Any Digital Output		-	20	-	ns
$\overline{HOLD}$ Pulse Width	t_{hpw}	$1/f_{CLK} + 50$	-	t_c	ns
Conversion Time	t_c	(Note 10)	-	(Note 10)	us
Data Delay Time	t_{dd}	-	40	100	ns
$\overline{EOC}$ Pulse Width (Note 11)	t_{epw}	$4/f_{CLK} - 20$	-	-	ns
Set Up Times: CAL, $\overline{INTRLV}$ to $\overline{CS}$ Low	t_{cs}	20	10	-	ns
A0 to $\overline{CS}$ and $\overline{RD}$ Low	t_{as}	20	10	-	
Hold Times:					
$\overline{CS}$ or $\overline{RD}$ High to A0 Invalid	t_{ah}	50	30	-	ns
$\overline{CS}$ High to CAL, $\overline{INTRLV}$ Invalid	t_{ch}	50	30	-	
Access Times: $\overline{CS}$ Low to Data Valid					
-K, B	t_{ca}	-	90	120	ns
-T		-	115	150	
$\overline{RD}$ Low to Data Valid					
-K, B	t_{ra}	-	90	120	ns
-T		-	115	150	
Output Float Delay: $\overline{CS}$ or $\overline{RD}$ High to Output Hi-Z	t_{fd}	-	50	70	ns
Serial Clock Pulse Width Low	t_{pwl}	-	$2/f_{CLK}$	-	ns
Pulse Width High	t_{pwh}	-	$2/f_{CLK}$	-	
Set Up Times: SDATA to SCLK Rising	t_{ss}	$2/f_{CLK} - 100$	$2/f_{CLK}$	-	ns
Hold Times: SCLK Rising to SDATA	t_{sh}	$2/f_{CLK} - 100$	$2/f_{CLK}$	-	ns

Notes: 10. See Table 1 and master clock frequencies above.

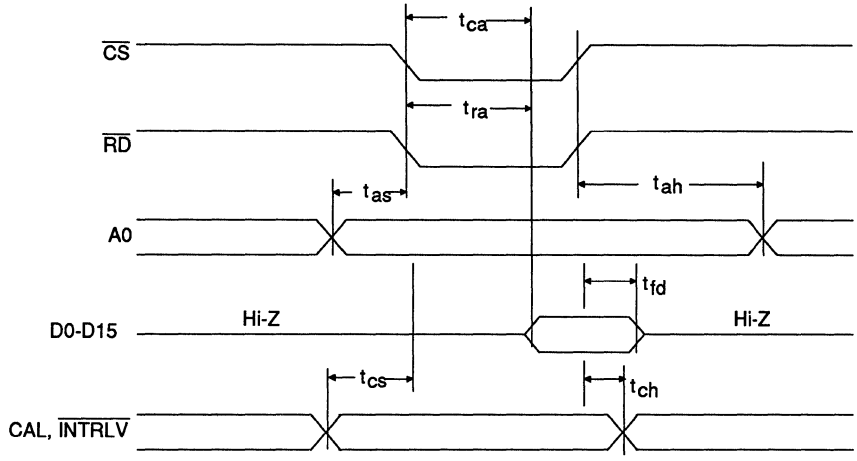
11. $\overline{EOC}$ remains low 4 master clock cycles if $\overline{CS}$ and $\overline{RD}$ are held low. Otherwise, It returns high within four master clock cycles from the start of a data read operation or a conversion cycle.



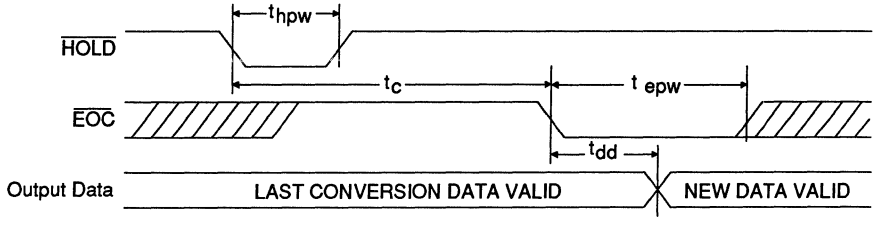
Rise and Fall Times



Serial Output Timing



Read and Calibration Control Timing



Conversion Timing

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 12)	V_{OH}	VD+ - 1.0V	-	-	V
Low-Level Output Voltage I_{out} = 1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	10	uA
3-State Leakage Current	I_{OZ}	-	-	±10	uA
Digital Output Pin Capacitance	C_{out}	-	9	-	pF

Note: 12. I_{out} = -100mA. This specification guarantees TTL compatibility (V_{OH} = 2.4V @ I_{out} = -40µA).

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see Note 13.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.5	5.0	5.5	V
	Negative Digital	VD-	−4.5	−5.0	−5.5	V
	Positive Analog	VA+	4.5	5.0	5.5	V
	Negative Analog	VA-	−4.5	−5.0	−5.5	V
Analog Reference Voltage		VREF	2.5	4.5	VA+ - 0.5	V
Analog Input Voltage:	Unipolar	V_{AIN}	AGND	-	VREF	V
(Note 14)	Bipolar	V_{AIN}	-(VREF)	-	VREF	V

Notes: 13. All voltages with respect to ground.

14. The CSZ5114 can accept input voltages up to the analog supplies (VA+ and VA-). It will produce an output of all 1's for inputs above VREF and all 0's for inputs below AGND in unipolar mode and -VREF in bipolar mode.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	−0.3	VA+ + 0.3	V
	Negative Digital	VD-	0.3	−6.0	V
	Positive Analog	VA+	−0.3	6.0	V
	Negative Analog	VA-	0.3	−6.0	V
Input Current, Any Pin Except Supplies (Note 15)		I_{in}	-	±10	mA
Analog Input Voltage (AIN and VREF pins)		V_{INA}	VA- - 0.3	VA+ + 0.3	V
Digital Input Voltage		V_{IND}	-0.3	VD+ + 0.3	V
Ambient Operating Temperature		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

Note: 15. Transient currents of up to 100mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

THEORY OF OPERATION

The CSZ5114 utilizes the most popular method of executing high-speed, high-resolution A/D conversion: successive approximation. As with all other iterative comparison methods, the analog input is successively compared to the output of a D/A converter controlled by the conversion algorithm. Successive approximation begins by comparing the input to the DAC output set to half-scale (MSB on, all other bits off). If the input is found to be below half-scale, the MSB is reset to zero and the input is compared to one-quarter scale (next-MSB on, all others off). If the input were above half-scale, the MSB would remain high and the next comparison would be at three-quarters of full scale. This procedure continues until all bits have been exercised.

The CSZ5114 implements the successive approximation algorithm using a unique charge-redistribution architecture. Instead of the traditional resistor network, the DAC is an array of binary-weighted capacitors. All legs of the array share a common node at the comparator's input, with their other terminals capable of being connected to AIN, AGND, or VREF (Figure 1). When the device is not calibrating or converting, all bits are tied to AIN forming C_{tot}. Switch S1 is closed and the charge on the array, Q_{in}, tracks the input signal V_{in} (Figure 2a).

When the conversion command is issued, switch S1 opens as shown in Figure 2b. This traps

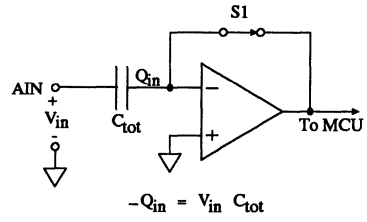


Figure 2a. Tracking Mode

charge Q_{in} on the comparator side of the capacitor array and creates a floating node at the comparator's input. The conversion algorithm operates on this fixed charge, and the signal at the analog input pin is ignored. In effect, the entire DAC capacitor array serves as analog memory during conversion much like a hold capacitor in a sample/hold amplifier.

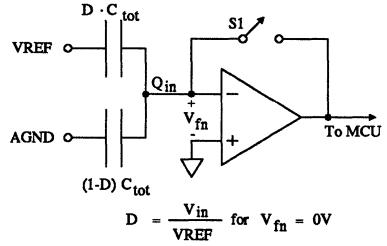


Figure 2b. Convert Mode

The conversion consists of manipulating the free plates of the capacitor array to VREF and AGND to form a capacitive divider. Since the charge at the floating node remains fixed, the voltage at that point depends on the proportion of capacitance tied to VREF versus AGND. The

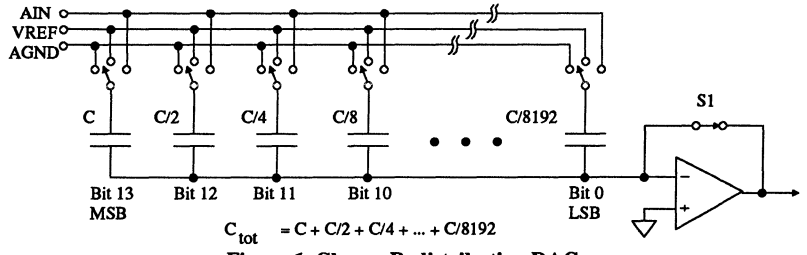


Figure 1. Charge Redistribution DAC

successive-approximation algorithm is used to find the proportion of capacitance, termed D in Figure 2b, which will drive the voltage at the floating node to zero. That binary fraction of capacitance represents the converter's digital output.

The CSZ5114's charge redistribution architecture easily supports bipolar input ranges. If half the capacitor array (the MSB capacitor) is tied to VREF rather than AIN in the track mode, the input range doubles and offsets half-scale. The magnitude of the reference voltage thus defines both positive and negative full-scale (-VREF to +VREF), and the digital code is an offset binary representation of the input.

Calibration

The ability of the CSZ5114 to convert accurately to 14-bits clearly depends on the accuracy of its comparator and DAC. The CSZ5114 utilizes an "auto-zeroing" scheme to null errors introduced by the comparator. All offsets are stored on the capacitor array while in the track mode and are effectively subtracted from the input signal when a conversion is initiated. Auto-zeroing enhances power supply rejection at frequencies below the conversion rate.

To achieve 14-bit accuracy from the DAC, the CSZ5114 uses a novel self-calibration scheme. Each bit capacitor shown in Figure 1 actually consists of several capacitors which can be manipulated to adjust the overall bit weight. During calibration, an on-chip microcontroller manipulates the sub-arrays to precisely ratio the bits. Each bit is adjusted to just balance the sum of all less significant bits plus one dummy LSB (for example, 16C = 8C + 4C + 2C + C + C). Calibration resolution for each bit is one-sixteenth of an LSB, resulting in a nearly ideal transfer function.

DIGITAL CIRCUIT CONNECTIONS

The CSZ5114 can be applied in a wide variety of master clock, sampling, and calibration conditions which directly affect the device's conversion time and throughput. The device also features on-chip 3-state output buffers and a complete interface for connecting to 8- and 16-bit digital systems. Output data is also available in serial format.

Master Clock

The CSZ5114 operates from a master clock which can be externally supplied or internally generated. The internal oscillator is activated by holding the CLKIN input low. Alternatively, the CSZ5114 can be synchronized to the external system by driving the CLKIN pin with a TTL or CMOS clock signal.

All calibration, conversion, and throughput times directly scale to master clock frequency. Thus, throughput can be precisely controlled and/or maximized using an external master clock. In contrast, the CSZ5114's internal oscillator will vary from unit-to-unit and over temperature. Its tolerance gives rise to minimum and maximum

a. Asynchronous Sampling

b. Synchronous Sampling

Figure 3. Sampling Connections

conversion times and throughput rates. The -14 version of the CSZ5114 is specified for accurate operation with an external clock up to 4MHz; its internal clock frequency is specified at a minimum of 2MHz. The -28 version can handle external clocks up to 2MHz; its internal clock can range as low as 1MHz (see *Switching Characteristics*, page 34).

Sampling/Initiating Conversions

A falling transition on the $\overline{\text{HOLD}}$ pin places the input in the hold mode and initiates a conversion cycle. The $\overline{\text{HOLD}}$ input is latched internally by the master clock, so it can return high anytime after one master clock cycle plus 50ns. Upon completion of the conversion cycle, the CSZ5114 automatically returns to the track mode. In contrast to systems with separate track-and-holds and A/D converters, a sampling clock can simply be connected to the $\overline{\text{HOLD}}$ input (Figure 3a). The duty cycle of this clock is not critical. It need only remain low at least one master clock cycle plus 50ns, but no longer than the minimum conversion time or an additional conversion cycle will be initiated with inadequate time for acquisition.

Conversion Time/Throughput

Upon completing a conversion cycle and returning to the track mode, the CSZ5114 requires time to acquire the analog input signal before another conversion can be initiated. The acquisition time is specified as six master clock cycles plus 2.25µs. This adds to the conversion time to define the converter's maximum throughput. The conversion time of the CSZ5114, in turn, depends on the sampling, calibration, and master clock conditions.

Asynchronous Sampling

The CSZ5114 internally operates from a clock which is delayed and divided down from the master clock ($f_{CLK}/4$). If sampling is not synchronized to this internal clock, the conversion cycle may not begin until up to four clock cycles after $\overline{\text{HOLD}}$ goes low even though the charge is trapped immediately. In this asynchronous mode (Figure 3a), the four clock cycles add to the minimum 57 clock cycles to define the maximum conversion time (see Figure 4a and Table 1).

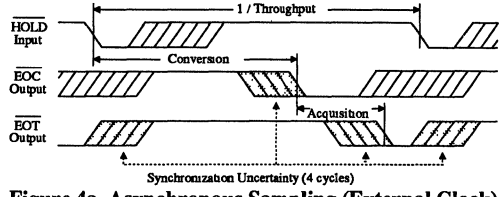


Figure 4a. Asynchronous Sampling (External Clock)

Synchronous Sampling

To achieve maximum throughput, sampling can be synchronized with the internal conversion clock by connecting the End-of-Track ($\overline{\text{EOT}}$) output to $\overline{\text{HOLD}}$ (Figure 3b). The $\overline{\text{EOT}}$ output falls 15 master clock cycles after $\overline{\text{EOC}}$ indicating the analog input has been acquired to the

	Conversion Time		Throughput Time	
Sampling Mode	min	max	min	max
Synchronous (Loopback)	57T	57T	72T	72T
Asynchronous	57T	61T + 235ns	N/A	67T + 2.25µs

(T ≡ one master clock cycle)

Table 1. Conversion and Throughput Times

CSZ5114's specified accuracy. The $\overline{EOT}$ output is synchronized to the internal conversion clock, so the four clock cycle synchronization uncertainty is removed yielding throughput at 1/80th of the master clock frequency (see Figure 4b and Table 1). To achieve maximum throughput in the loopback mode, the master clock high time must not exceed 100ns.

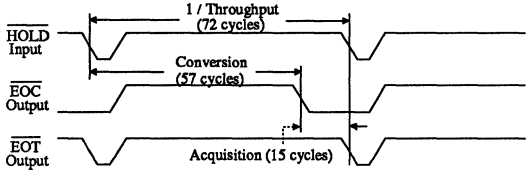


Figure 4b. Synchronous (Loopback) Mode

Also, the CSZ5114's internal RC oscillator exhibits significant jitter (typically ± 0.05% of its period), which is high compared to crystal oscillators. If the CSZ5114 is configured for synchronous sampling while operating from its internal oscillator, this jitter will directly affect sampling purity.

The $\overline{EOT}$ output is an accurate indicator of the CSZ5114's acquisition requirement when operating at the -14 version's full rated speed (3.75µs with a 4MHz master clock). However, $\overline{EOT}$ will allow the CSZ5114 more acquisition time than necessary when operating with a clock less than 4MHz. The $\overline{EOT}$ output always falls 15 master clock cycles after $\overline{EOC}$. The CSZ5114 only needs 3.75µs (six cycles @4MHz plus 2.25µs). When operating the -28 with a master clock of 2MHz or less, higher throughput can be achieved than in the loopback configuration by using an external counter. The counter should be reset by the falling edge of EOC and count the appropriate number of clock cycles after each conversion. When the total time is greater than six clock cycles plus 2.25µs the counter can trigger a new conversion at $\overline{HOLD}$. For example, when using a 2MHz clock, 2.25µs takes between four and five clock cycles. When six cycles are added to this it is seen that the counter should trigger a new conversion at the eleventh clock cycle.

Reset

Upon power up, the CSZ5114 must be reset to guarantee a consistent starting condition and initially calibrate the device. Due to the CSZ5114's low power dissipation and low temperature drift, no warm-up time is required before reset to accommodate any self-heating effects. However, the voltage reference input should have stabilized to within 0.25% of its final value before RST falls to guarantee an accurate calibration. Later, the CSZ5114 may be reset at any time to initiate a single full calibration. Reset overrides all other functions. If reset, the CSZ5114 will clear and initiate a new calibration cycle mid-conversion or mid-calibration.

Resets can be initiated in hardware or software. The simplest method of resetting the CSZ5114 involves strobing the RST pin high. When RST is brought high all internal logic clears. When it returns low a full calibration begins which takes 1,443,840 master clock cycles (approximately 360ms with a 4MHz clock) to complete. A simple power-on reset circuit can be built using a resistor and capacitor, and a Schmidt-trigger inverter to prevent oscillation (see Figure 5). The CSZ5114 can also be reset in software when under microprocessor control. The CSZ5114 will reset whenever $\overline{CS}$, A0, and $\overline{HOLD}$ are taken low simultaneously. See the *Microprocessor*

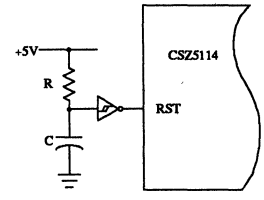


Figure 5. Power-On Reset Circuitry

Interface section to eliminate the possibility of inadvertent software reset. The $\overline{EOC}$ output remains high throughout the reset operation and will fall upon its completion. It can thus be used to generate an interrupt indicating the CSZ5114 is ready for operation. Six master clock cycles plus 2.25µs must be allowed after $\overline{EOC}$ falls to allow for acquisition. Under microprocessor-independent operation with 3-states permanently enabled ($\overline{CS}$, $\overline{RD}$ low; A0 high) the $\overline{EOC}$ output will not fall at the completion of the reset operation.

Initiating Calibration

All modes of calibration can be controlled in hardware or software. Accuracy can thereby be insured at any time or temperature throughout operating life. After initial calibration at power-up, the CSZ5114's charge-redistribution design yields better temperature drift and more graceful aging than resistor-based technologies, so calibration is actually required less often than with traditional devices.

The first mode of calibration, reset, results in a single full calibration cycle. The second type of calibration, termed "burst" cal, is useful when the ADC sees some downtime but not enough to perform a full reset calibration. Burst cal can be terminated mid-calibration; it picks up where it left off previously, so calibrations can be done in piecemeal fashion. Burst cal is initiated by bringing the CAL input high with $\overline{CS}$ low. The CAL input is level-triggered and latches on the rising edge of $\overline{CS}$, so a write cycle can be used to control calibration in software. Burst cal will continue to loop through calibration cycles until terminated. Once CAL returns low, at least 26 master clock cycles plus 2.25µs (8.75µs @ 4MHz clock) must be allowed before a conversion is initiated to ensure the CSZ5114 has completed its calibration experiment and has acquired the analog input. The $\overline{EOC}$ output indicates the completion of the final calibration experiment. (See note on page 59.)

The CSZ5114 features a background calibration mode called "interleave." Interleave appends a single calibration experiment to each conversion cycle and thus requires no dead time for calibration. The CSZ5114 gathers data between conversions and will adjust its transfer function once it completes the entire sequence of experiments (one calibration cycle per 72,192 conversions). Initiated by bringing both the $\overline{INTRLV}$ input and $\overline{CS}$ low (or hard-wiring $\overline{INTRLV}$ low), interleave extends the CSZ5114's effective conversion time by 20 master clock cycles. Other than reduced throughput, interleave is totally transparent to the user.

Burst calibrations initiated at CAL pick up where interleave left off, so calibration cycles can be hastened by "bursting" a number of experiments whenever the CSZ5114 sees free time. Interleave is subordinate to burst calibrations, so $\overline{INTRLV}$ could still be hard-wired low.

Microprocessor Interface

The CSZ5114 features an intelligent microprocessor interface which offers detailed status information and allows software control of the self-calibration functions. Output data is available in either 8- or 16-bit formats for easy interfacing to industry-standard microprocessors.

Strobing both $\overline{CS}$ and $\overline{RD}$ low enables the CSZ5114's 3-state output buffers with either output data or status information depending on the status of A0. An address bit can be connected

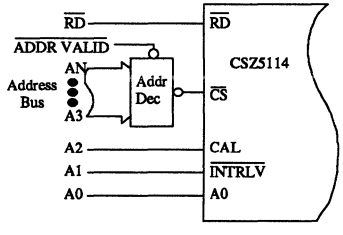


Figure 6. Address/Control Bus Connections

PIN	STATUS BIT	STATUS	DEFINITION
D0	S0	$\overline{\text{END OF CONVERSION}}$	Falls upon completion of a conversion, and returns high on the first subsequent read.
D1	S1	RESERVED	Reserved for factory use.
D2	S2	LOW BYTE/$\overline{\text{HIGH BYTE}}$	When data is to be read in an 8-bit format (BW=0), indicates which byte will appear at the output next.
D3	S3	$\overline{\text{END OF TRACK}}$	When low, indicates the input has been acquired to the devices specified accuracy.
D4	S4	RESERVED	Reserved for factory use.
D5	S5	TRACKING	High when the device is tracking the intput.
D6	S6	CONVERTING	High when the device is converting the held input.
D7	S7	CALIBRATING	High when the device is calibrating.

Table 2. Status Bit Definitions

to A0 as shown in Figure 6 thereby memory mapping the status register and output data. Conversion status can be polled in software by reading the status register ($\overline{CS}$ and $\overline{RD}$ strobed low with A0 low), and masking status bits S0-S5 and S7 (by logically AND'ing the status word with 01000000) to determine the value of S6. Similarly, the software routine can determine calibration status using other status bits (see Table 2). *Care must be taken not to read the status register (A0 low) while $\overline{HOLD}$ is low, or a software reset will result* (see *Reset*, page 40).

Alternatively, the End-of-Convert ($\overline{EOC}$) output can be used to generate an interrupt or drive a DMA controller to dump the output directly into memory after each conversion. The $\overline{EOC}$ pin falls as each conversion cycle is completed and data is valid at the output. It returns high within four master clock cycles of the first subsequent data read operation or after the start of a new conversion cycle.

To interface with a 16-bit data bus, the BW input to the CSZ5114 should be held high and all 14 data bits read in parallel on pins D15-D2. With an 8-bit bus, the converter's 14-bit result must be read in two portions. In this instance, BW should be held low and the 8 MSB's obtained on the first read cycle following a conversion. The second read cycle will yield the 6 LSB's with two trailing zeroes. Both bytes appear on pins D0-D7. The upper/lower bytes of the same data will continue to toggle on subsequent reads until the next conversion finishes. Status bit S4 indicates which byte will appear on the next data read operation.

The CSZ5114 internally buffers its output data, so data can be read while the device is tracking or converting the next sample. Therefore, retrieving the converter's digital output requires no reduction in ADC throughput. Enabling the 3-state outputs while the CSZ5114 is converting will not introduce conversion errors. When TTL

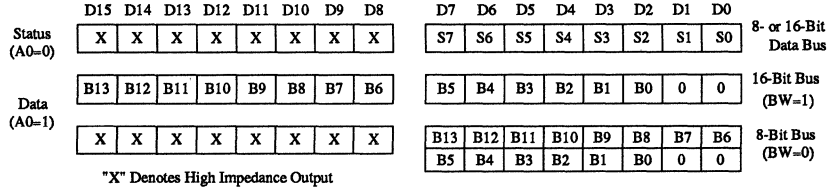


Figure 7. Data Format

loads are utilized the potential for crosstalk between digital and analog sections of the system is increased. This crosstalk is due to high digital supply and signal currents arising from the TTL drive current required of each digital output. Connecting CMOS logic to the digital outputs is recommended. Suitable logic families include 4000B, 74HC, 74AC, 74ACT, and 74HCT.

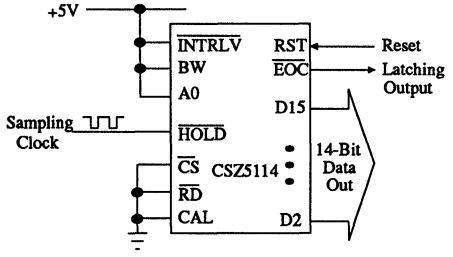


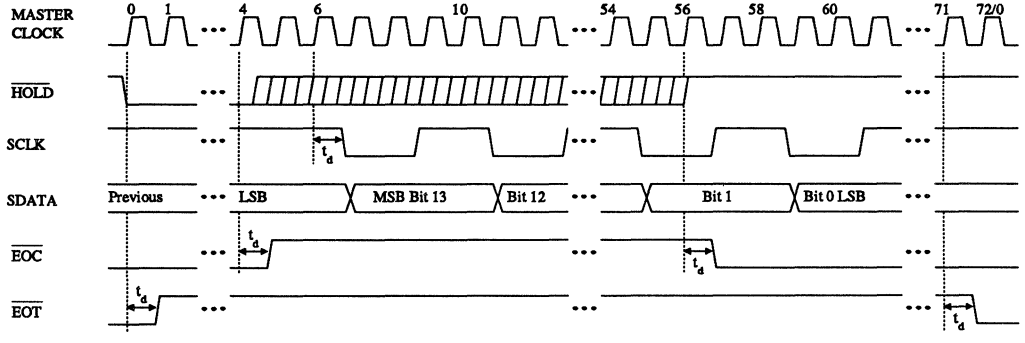
Figure 8. Microprocessor-Independent Connections

Microprocessor Independent Operation

The CSZ5114 can be operated in a stand-alone mode independent of intelligent control. In this mode, $\overline{CS}$ and $\overline{RD}$ are hard-wired low permanently enabling the 3-state output buffers. A free-running condition is established when BW is tied high, CAL is tied low, and $\overline{HOLD}$ is continually strobed low or tied to $\overline{EOT}$. The CSZ5114's $\overline{EOC}$ output can be used to externally latch the output data if desired. With $\overline{CS}$ and $\overline{RD}$ hard-wired low, $\overline{EOC}$ will strobe low for four master clock cycles after each conversion. Data will be unstable up to 100ns after $\overline{EOC}$ falls, so it should be latched on the rising edge of $\overline{EOC}$.

Serial Output

All successive-approximation A/D converters derive their digital output serially starting with the MSB. The CSZ5114 presents each bit to the SDATA pin four master clock cycles after it is derived and can be latched using the serial clock output, SCLK. Just subsequent to each bit decision SCLK will fall and return high once the bit information on SDATA has stabilized. Thus, the rising edge of the SCLK output should be used to clock the data from the CSZ5114 (See Figure 9).



notes: 1. t_d can vary from 135ns - 235ns over military temerature range and over ± 10% supply variation.
2. For asynchronous mode, transitions of SCLK, SDATA, $\overline{EOC}$, $\overline{EOT}$ can shift by up to 4 clocks; e.g. the first high to low transition of SCLK may be on clock #6 to #9. The timing relationship between SCLK, SDATA, $\overline{EOC}$, and $\overline{EOT}$ is fixed.

Figure 9. Serial Output Timing

ANALOG CIRCUIT CONNECTIONS

Most popular successive-approximation A/D converters generate dynamic loads at their analog connections. The CSZ5114 internally buffers all analog inputs (AIN, VREF, and AGND) to ease the demands placed on external circuitry. However, accurate system operation still requires careful attention to details at the design stage regarding source impedances as well as grounding and decoupling schemes.

Reference Considerations

An application note titled "*Voltage References for the CS501X/CSZ511X Series of A/D Converters*" is available for the CSZ5114. In addition to working through a reference circuit design example, it offers seven built-and-tested reference circuits.

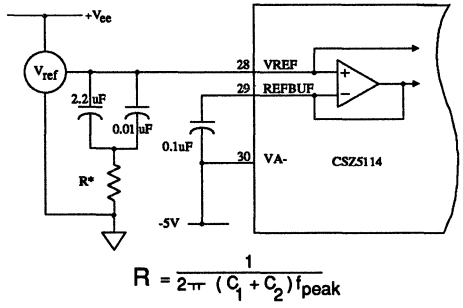


Figure 10. Reference Connections

During conversion, the members of the calibrated capacitor array are switched between VREF and AGND in a manner determined by the successive-approximation algorithm. The charging and discharging of the array results in a current load at the reference. The CSZ5114 includes an internal buffer amplifier to minimize the external reference circuit's drive requirement and preserve the reference's integrity. Whenever the array is switched during conversion, the buffer is used to pre-charge the array thereby providing the bulk of the necessary charge. The appropriate array capacitors are then switched to the unbuffered VREF pin to avoid any errors due to offsets and/or noise in the buffer.

The external reference circuitry need only provide the residual charge required to fully charge the array after pre-charging from the buffer. This creates an ac current load as the CSZ5114 sequences through conversions. The reference circuitry must have a low enough output impedance to drive the requisite current without changing its output voltage significantly.

As the analog input signal varies, the switching sequence of the internal capacitor array changes. The current load on the external reference circuitry thus varies in response with the analog input. Therefore, the external reference must not exhibit significant peaking in its output impedance characteristic at signal frequencies or their harmonics.

A large capacitor connected between VREF and AGND can provide sufficiently low output impedance at the high end of the frequency spectrum, while almost all precision references exhibit extremely low output impedance at dc. The presence of large capacitors on the output of some voltage references, however, may cause peaking in the output impedance at intermediate frequencies. Care should be exercised to ensure that significant peaking does not exist or that some form of compensation is provided to eliminate the effect.

The magnitude of the current load on the external reference circuitry will scale to the master clock frequency. At full speed (4MHz clock), the reference must supply a maximum load current of 10µA peak-to-peak (1µA typical). An output impedance of 4Ω will therefore yield a maximum error of 40µV. With a 4.5V reference and LSB size of 276µV, this would insure better than 1/4 LSB accuracy. A 2.2 µF capacitor exhibits an impedance of less than 4Ω at

frequencies greater than 5kHz, and voltage references with dc output impedances less than an ohm are readily available. A high-quality tantalum capacitor in parallel with a smaller ceramic capacitor is recommended.

Peaking in the reference's output impedance can occur because of capacitive loading at its output. Any peaking that might occur can be reduced by placing a small resistor in series with the capacitors (Figure 10). The equation in Figure 10 can be used to help calculate the optimum value of R for a particular reference. The term "f_{peak}" is the frequency of the peak in the output impedance of the reference before the resistor is added.

The CSZ5114 can operate with a wide range of reference voltages, but signal-to-noise performance is maximized by using as wide a signal range as possible. The recommended reference voltage is 4.5 volts. The CSZ5114 can actually accept reference voltages up to the positive analog supply. However, the buffer's offset may increase as the reference voltage approaches VA+ thereby increasing external drive requirements at VREF. A 4.5V reference is the maximum reference voltage recommended. This allows 0.5V headroom for the internal reference buffer. Also, the buffer enlists the aid of an external 0.1µF ceramic capacitor which must be tied between its output, REFBUF, and the negative analog supply, VA-. For more information on references, consult "Application Note: *Voltage References for the CS501X-CSZ511X Series of A/D Converters*".

Analog Input Connection

The analog input terminal functions similarly to the VREF input after each conversion when switching into the track mode. During the first six master clock cycles in the track mode, the buffered version of the analog input is used for pre-charging the capacitor array. An additional period is required for fine-charging directly from AIN to obtain the specified accuracy. Figure 11 exemplifies this operation. During pre-charge the charge on the capacitor array first settles to the buffered version of the analog input. This voltage is offset from the actual input voltage. During fine-charge, the charge then settles to the accurate unbuffered version.

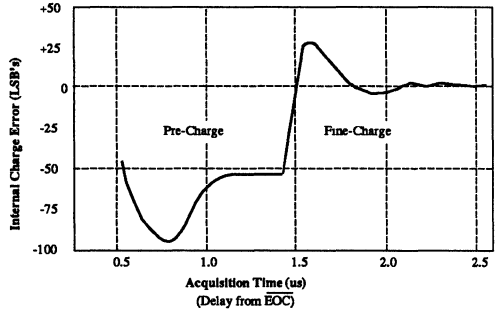


Figure 11. Internal Acquisition Time

The acquisition time of the CSZ5114 depends on the master clock frequency. This is due to a fixed pre-charge period. For instance, operating the -14 version with an external 4MHz master clock results in a 3.75µs acquisition time: 1.5µs for pre-charging (6 clock cycles) and 2.25µs for fine-charging. Fine-charge settling is specified as a maximum of 2.25µs for an analog source impedance of less than 200Ω.

In addition, the comparator requires a source impedance of less than 400Ω around 2MHz for stability, which is met by practically all bipolar op amps. Large dc source impedances can be accommodated by adding capacitance from AIN to ground (typically 200pF) to decrease source impedance at high frequencies. However, high dc source resistances will increase the input's RC time constant and extend the necessary acquisition time.

The CSZ5114 can track full power signals up to 28kHz in the track mode. During the first six

clock cycles following a conversion, the CSZ5114 is capable of slewing at 5V/µs in unipolar mode. In bipolar mode, only half the capacitor array is connected to the analog input so the CSZ5114 can slew at 10V/µs. After the first six master clock cycles, it will slew at 0.25V/µs in the unipolar mode and 0.5V/µs in bipolar mode. Acquisition of fast slewing signals (step functions) can be hastened if the step occurs during or immediately following the conversion cycle. For instance, channel selection in multiplexed applications should occur while the CSZ5114 is converting (see Figure 12). Multiplexer settling is thereby removed from the overall throughput equation, and the CSZ5114 can convert at full speed.

Analog Input Range/Coding Format

The reference voltage directly defines the input voltage range in both the unipolar and bipolar configurations. In the unipolar configuration (BP/$\overline{UP}$ low), the first code transition occurs 0.5 LSB above AGND, and the final code transition occurs 1.5 LSB's below VREF. Coding is in straight binary format. In the bipolar configuration (BP/$\overline{UP}$ high), the first code transition occurs 0.5 LSB above -VREF and the last transition occurs 1.5 LSB's below +VREF. Coding is in an offset-binary format. Positive full scale gives a digital output of 11111111111111, and negative full scale gives a digital output of 00000000000000.

Grounding and Power Supply Decoupling

The CSZ5114 uses the analog ground connection, AGND, only as a reference voltage. No dc power currents flow through the AGND connection, and it is completely independent of DGND. However, any noise riding on the AGND input relative to the system's analog ground will induce conversion errors. Therefore, both the analog input and reference voltage should be referred to the AGND pin, which should be used as the entire system's analog ground. The digital and analog supplies are isolated within the CSZ5114 and are pinned out separately to minimize coupling between the analog and digital sections of the chip. All four supplies should be decoupled to their respective grounds using 0.1µF ceramic capacitors. If significant low-frequency noise is present on the supplies, 1µF tantalum capacitors are recommended in parallel with the 0.1µF capacitors.

The positive digital power supply of the CSZ5114 must never exceed the positive analog supply by more than a diode drop or the CSZ5114 could experience permanent damage. If the two

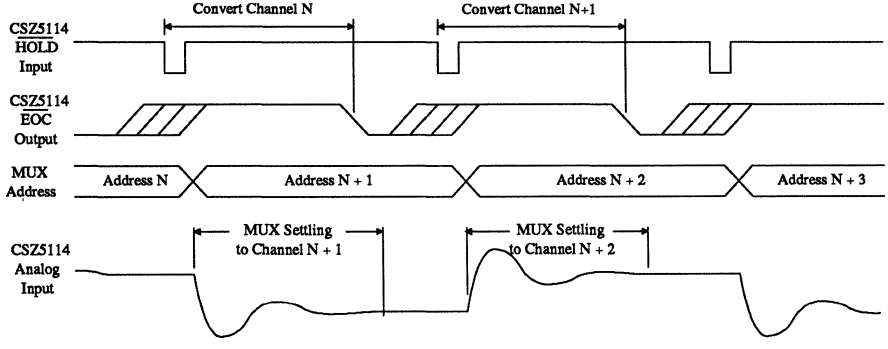


Figure 12. Pipelined MUX Input Channels

supplies are derived from separate sources, care must be taken that the analog supply comes up first at power-up. The system connection diagram on page 53 shows a decoupling scheme which allows the CSZ5114 to be powered from a single set of ± 5V rails. The positive digital supply is derived from the analog supply through a 10Ω resistor to avoid the analog supply dropping below the digital supply. If this scheme is utilized, care must be taken to insure that any digital load currents (which flow through the 10Ω resistors) do not cause the magnitude of digital supplies to drop below the analog supplies by more than 0.5 volts. Digital supplies must always remain above the minimum specification.

As with any high-precision A/D converter, the CSZ5114 requires careful attention to grounding and layout arrangements. However, no unique layout issues must be addressed to properly apply the CSZ5114. The CDB5114 evaluation board is available for the CSZ5114, which avoids the need to design, build, and debug a high-precision PC board to initially characterize the part. The board comes with a socketed CSZ5114, and can be quickly reconfigured to simulate any combination of sampling, calibration, master clock, and analog input range conditions.

CSZ5114 PERFORMANCE

The CSZ5114 offers 100% tested dynamic performance. Due to the broad range of operating conditions and performance requirements in signal processing applications, the following section is included to illustrate the CSZ5114's error sources and their effect on a signal's spectral content.

FFT Tests and Windowing

In the factory, the CSZ5114 is tested using Fast Fourier Transform (FFT) techniques to analyze the converter's dynamic performance. A pure sinewave is applied to the CSZ5114, and a "time record" of 1024 samples is captured and processed. The FFT algorithm analyzes the spectral content of the digital waveform and distributes its energy among 512 "frequency bins." Assuming an ideal sinewave, distribution of energy in bins outside of the fundamental and dc can only be due to quantization effects and errors in the CSZ5114.

If sampling is not synchronized to the input sinewave, it is highly unlikely that the time record will contain an integer number of periods of the input signal. However, the FFT assumes that the signal is periodic, and will calculate the spectrum of a signal that appears to have large discontinuities, thereby yielding a severely distorted spectrum. To avoid this problem, the time record is multiplied by a window function prior to performing the FFT. The window function smoothly forces the endpoints of the time record to zero, thereby removing the discontinuities. The effect of the window in the frequency-domain is to convolute the spectrum of the window with that of the actual input.

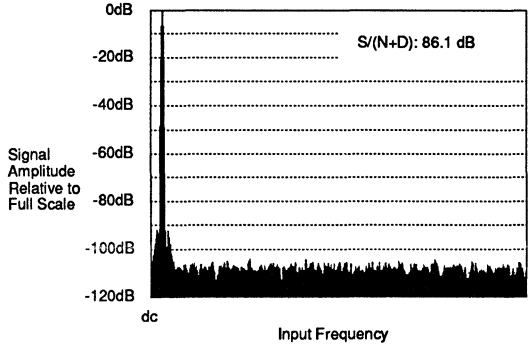


Figure 13. FFT Plot of Ideal 14-bit Signal

The quality of the window used for harmonic analysis is typically judged by its highest side-lobe level. The Blackman-Harris window used for testing the CSZ5114 has a maximum side-lobe level of -92dB. Figure 13 shows an FFT computed from an ideal 14-bit sinewave multiplied by a Blackman-Harris window. Artifacts of windowing are discarded from the signal-to-noise calculation using the assumption that all noise sources are white. All FFT plots in this data sheet were derived by averaging the FFT results from ten time records. This filters the spectral variability that can arise from capturing finite time records without disturbing the total energy outside the fundamental. All harmonics and the -92dB side-lobes from the Blackman-Harris window are therefore clearly visible in the plots. For more information on FFT's and windowing refer to: F.J. HARRIS, "On the use of windows for harmonic analysis with the Discrete Fourier Transform", Proc. IEEE, Vol. 66, No. 1, Jan 1978, pp.51-83.

Nonlinearity

Analog-to-digital converters have traditionally been specified using dc specifications such as Integral and Differential Nonlinearity at worst-case points on the transfer curve. These specifications are not particularly useful in signal processing applications since they offer little information on the overall shape of converter's transfer curve, and therefore do not directly correlate to the converter's effect on a signal's spectral content.

Integral Nonlinearity (INL; also termed Relative Accuracy or just Nonlinearity) is defined as the deviation of the transfer function from an ideal straight line. Bows and waves in the transfer curve generate harmonic distortion. However, the most prevalent source of nonlinearity in high-resolution converters is bit-weight errors; that is, the deviation of bits from their ideal binary-weighted ratios. At dc, bit-weight errors most visibly affect the converter's Differential Nonlinearity, or the deviation of codes from their ideal widths. Due to the limitations of factory trim techniques, the worst-case condition of bit-weight errors has traditionally also defined the point of maximum INL.

Bit-weight errors have a drastic effect on a converter's ac performance. They can be analyzed as step functions superimposed on the input signal. Since bits (and their errors) switch in and out throughout the transfer curve, their effect is signal dependent. That is, harmonic and intermodulation distortion, as well as noise, can vary with different input conditions. Designing a system around characterization data is risky since transfer curves can differ drastically unit-to-unit and lot-to-lot.

The CSZ5114 achieves repeatable signal-to-noise and harmonic distortion performance using an on-chip self-calibration scheme. The CSZ5114 calibrates its bit weights to ± 1/16 LSB at 14-bits (± 0.0004% FS) yielding peak distortion as low as -100dB (see Figure 14). Unlike traditional ADC's, the linearity of the CSZ5114 is not limited by bit-weight errors; its performance is therefore extremely repeatable and independent of input signal conditions.

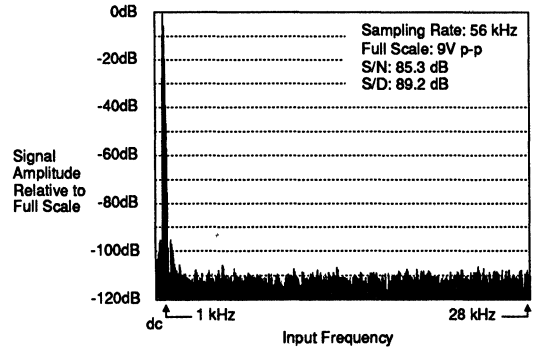


Figure 14. FFT Plot with 1kHz Full-Scale Input

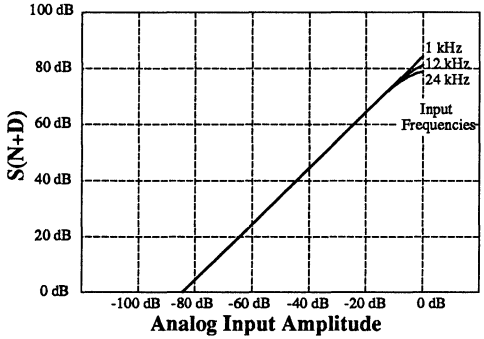


Figure 15. S/(N+D) vs. Input Amplitude (9V p-p Full-Scale Input)

Sampling Distortion

The ultimate limitation on the CSZ5114's linearity (and distortion) arises from nonideal sampling of the analog input voltage. The calibrated capacitor array used during conversions is also used to track and hold the analog input signal. The conversion is not performed on the analog input voltage per se, but is actually performed on the charge trapped on the capacitor array at the moment the $\overline{HOLD}$ command is given. The charge on the array is ideally related to the analog input voltage by $Q_{in} = -V_{in} \times C_{tot}$ as shown in Figure 2. Any deviation from this ideal relationship will result in conversion errors even if the conversion process proceeds flawlessly.

At dc, the DAC capacitor array's voltage coefficient dictates the converter's linearity. This variation in capacitance with respect to applied signal voltage yields a nonlinear relationship between charge Q_{in} and the analog input voltage V_{in} and places a bow or wave in the transfer function. This is the dominant source of distortion at low input frequencies (Figure 14).

The ideal relationship between Q_{in} and V_{in} can also be distorted at high signal frequencies due to nonlinearities in the internal MOS switches. Dynamic signals cause ac current to flow through the switches connecting the capacitor array to the analog input pin in the track mode. Nonlinear on-resistance in the switches causes a nonlinear voltage drop. This effect worsens with increased signal frequency as shown in Figure 15 since the magnitude of the steady state current increases. First noticeable at 1kHz, this distortion assumes a linear relationship with input frequency. With signals 20dB or more below full-scale, it no longer dominates the converter's overall S/(N+D) performance (Figure 16).

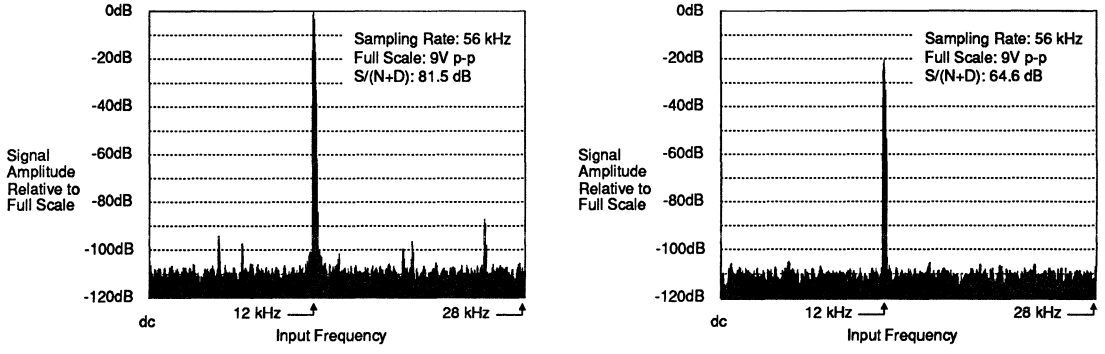


Figure 16. FFT Plots of 12kHz Signals at Full-Scale and 20dB Below Full-Scale

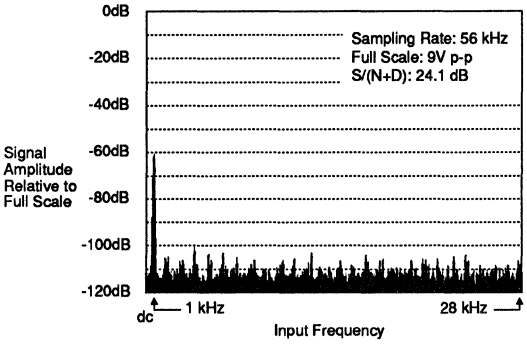


Figure 17. FFT plot of 1kHz Signal 60dB Below Full Scale

This distortion is strictly an ac sampling phenomenon. If significant energy exists at high frequencies, the effect can be eliminated using an external track-and-hold amplifier to create an effective dc input. Delaying the $\overline{\text{HOLD}}$ signal to the CSZ5114 slightly from the sampling signal to the trackand-hold amplifier will allow the array's charge current to decay, thereby eliminating any voltage drop across the switches. Since the CSZ5114 has a second sampling function on-chip, the external track-and-hold can return to the track mode once the converter's HOLD input falls. It need only acquire the analog input by the time the entire conversion cycle finishes.

Quantization Noise

The error due to quantization of the analog input ultimately dictates the accuracy of any A/D converter. The continuous analog input must be represented by one of a finite number of digital codes, so the best accuracy to which an analog input can be known from its digital code is ± 1/2 LSB. Under circumstances commonly encountered in signal processing applications, this quantization error can be treated as a random variable. The magnitude of the error is limited to ± 1/2 LSB, but any value within this range has equal probability of occurrence. Such a probability distribution leads to an error "signal" with an rms value of 1 LSB/$\sqrt{12}$. Using an rms signal value of FS/$\sqrt{8}$ (amplitude = FS/2), this relates to an ideal 14-bit signal-to-noise ratio of 86dB.

Equally important is the spectral content of this error signal. It can be shown to be approximately white, with its energy spread uniformly over the band from dc to one-half the sampling rate. Advantage of this characteristic can be made by judicious use of filtering. If the signal is bandlimited, much of the quantization error can be filtered out using DSP techniques, and improved system performance can be attained.

As illustrated in Figures 15 and 17, the CSZ5114's on-chip self-calibration provides very accurate bit weights which yield no degradation in quantization noise with low-level input signals.

Clock Feedthrough

Maintaining the integrity of analog signals in the presence of digital switching noise is a difficult problem. The CSZ5114 can be synchronized to the digital system using the CLKIN input to avoid conversion errors due to asynchronous interference. However, digital interference will still affect sampling purity due to coupling between the CSZ5114's analog input and master clock.

The effect of clock feedthrough depends on the sampling conditions. If the sampling signal at the $\overline{\text{HOLD}}$ input is synchronized to the master clock, clock feedthrough will appear as a dc offset at the CSZ5114's output. The offset could theoretically reach the peak coupling magnitude (Figure 18), but the probability of this occurring is small since the peaks are spikes of short duration.

If sampling is performed asynchronously with the master clock, clock feedthrough will appear as an ac error at the CSZ5114's output. With a fixed sampling rate, a tone will appear as the clock frequency aliases into the baseband. The tone frequency can be calculated using the equation below and could be selectively filtered in software using DSP techniques.

$$f_{tone} = (Nf_s - f_{clk})$$

where $N = f_{clk}/f_s$ rounded to the nearest integer

The magnitude of clock feedthrough depends on the master clock conditions and the source impedance applied to the analog input. When operating with the CSZ5114's internally generated clock, the CLKIN input is grounded and the dominant source of coupling is through the device's substrate. As shown in Figure 18, a typical CSZ5114 operating with its internal oscillator at 2MHz and 50Ω of analog input source impedance will exhibit only 15μV rms (-116dB with a 9V p-p full-scale) of clock feedthrough. However, if a 2MHz external clock is applied to CLKIN under the same conditions, feedthrough increases to 25μV rms (-111dB). Feedthrough also increases with clock frequency; a 4MHz clock yields 40μV rms (-107dB).

Master Clock		Analog Input	Clock Feedthrough	
Int/Ext	Freq	Source Impedance	RMS	Peak-to-Peak
Internal	2MHz	50Ω	15uV	70uV
External	2MHz	50Ω	25uV	110uV
External	4MHz	50Ω	40uV	150uV
External	4MHz	25Ω	25uV	110uV
External	4MHz	200Ω	80uV	325uV

Figure 18. Examples of Measured Clock Feedthrough

Clock feedthrough can be reduced by limiting the source impedance applied at the analog input. As shown in Figure 18, reducing source impedance from 50Ω to 25Ω yields a 15μV rms reduction in feedthrough. Therefore, when operating the CSZ5114 with high-frequency external master clocks, it is important to minimize source impedance applied to the CSZ5114's input.

Also, the overall effect of clock feedthrough can be minimized by maximizing the input range and LSB size. The reference voltage applied to VREF can be maximized, and the CSZ5114 can be operated in bipolar mode which inherently doubles the LSB size over the unipolar mode.

Aperture Jitter

Track-and-hold amplifiers commonly exhibit two types of aperture jitter. The first, more appropriately termed "aperture window", is an input voltage dependent variation in the aperture delay. Its signal-dependancy causes distortion at high frequencies. The CSZ5114's proprietary architecture avoids applying the input voltage across a sampling switch, thus avoiding any "aperture window" effects. The second type of aperture jitter assumes a random nature and appears in an FFT as a spreading in the fundamental. With only 100ps peak-to-peak aperture jitter, the CSZ5114 can process full-scale signals up to 96kHz with 14-bit accuracy.

Power Supply Rejection

The CSZ5114's power supply rejection performance is enhanced by the on-chip self-calibration and an "auto-zero" process. Drifts in power supply voltages at frequencies less than the calibration rate have negligible effect on the CSZ5114's accuracy. This, of course, is because the CSZ5114 adjusts its offset to within a small fraction of an LSB during calibration. Above the calibration frequency the excellent power supply rejection of the internal amplifiers is augmented by an auto-zero process. Any offsets are stored on the capacitor array and are effectively subtracted once conversion is initiated. Figure 19 shows power supply rejection of the CSZ5114 in

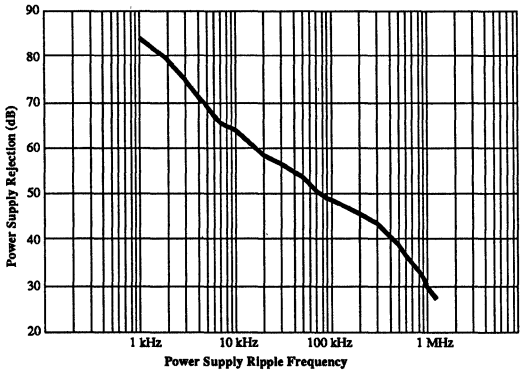


Figure 19. Power Supply Rejection

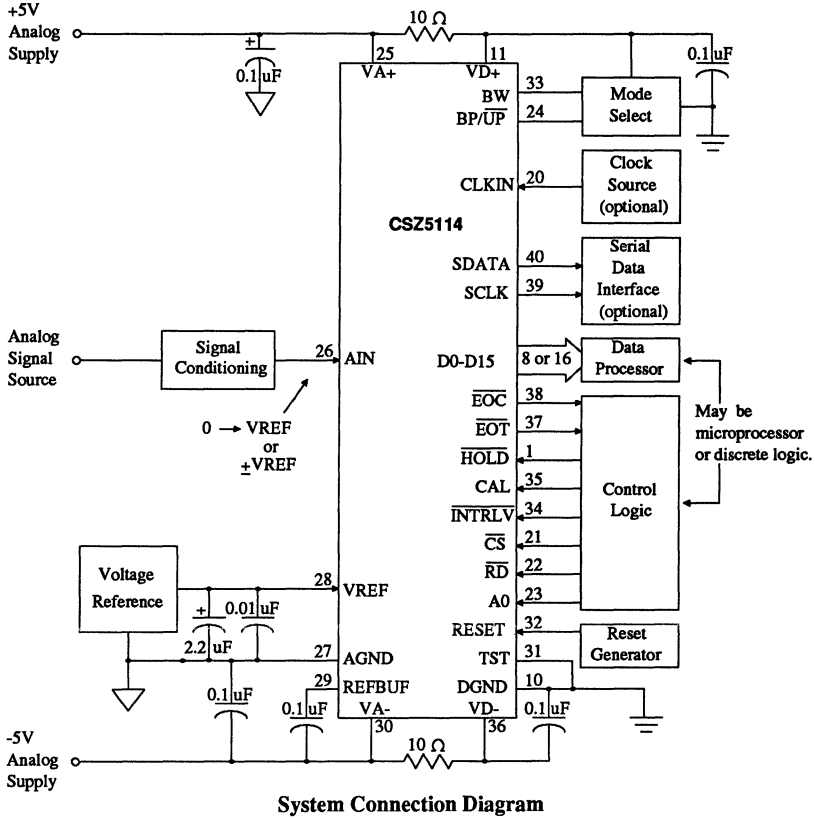
the bipolar mode with the analog input grounded and a 300mV p-p ripple applied to each supply. Power supply rejection improves by 6dB in the unipolar mode.

Notches of increased rejection arise from the auto-zeroing at the conversion rate. The frequencies at which these notches occur also depend on the value of the captured analog input. The line shows worst-case rejection for all combinations of conversion rates and input conditions in the bipolar mode. Again, power supply rejection is 6dB better in the unipolar mode.

$\overline{HOLD}$	$\overline{CS}$	CAL	$\overline{INTRLV}$	$\overline{RD}$	A0	RST	Function
↓	X	X	X	X	*	0	Hold and Start Convert
X	0	1	X	X	*	0	Initiate Burst Calibration
1	0	0	X	X	*	0	Stop Burst Cal and Begin Track
X	0	X	0	X	*	0	Initiate Interleave Calibration
X	0	X	1	X	*	0	Terminate Interleave Cal
X	0	X	X	0	1	0	Read Output Data
1	0	X	X	0	0	0	Read Status Register
X	1	X	X	X	*	X	High Impedance Data Bus
X	X	X	X	1	*	X	High Impedance Data Bus
X	X	X	X	X	X	1	Reset
0	0	X	X	X	0	X	Reset

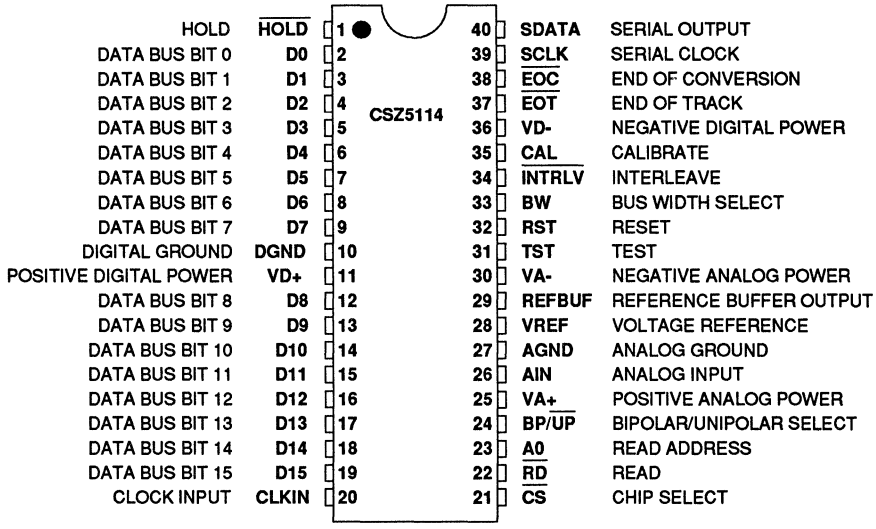
* The status of A0 is not critical to the operation specified. However, A0 should not be low with $\overline{CS}$ and $\overline{HOLD}$ low, or a software reset will result.

CSZ5114 Truth Table



System Connection Diagram

PIN DESCRIPTIONS



Power Supply Connections

VD+ - Positive Digital Power, PIN 11.
Positive digital power supply. Nominally +5 volts.

VD- - Negative Digital Power, PIN 36.
Negative digital power supply. Nominally -5 volts.

DGND - Digital Ground, PIN 10.
Digital ground reference.

VA+ - Positive Analog Power, PIN 25.
Positive analog power supply. Nominally +5 volts.

VA- - Negative Analog Power, PIN 30.
Negative analog power supply. Nominally -5 volts.

AGND - Analog Ground, PIN 27.
Analog ground reference.

Oscillator

CLKIN - Clock Input, PIN 20.

All conversions and calibrations are timed from a master clock which can either be supplied by driving this pin with an external clock signal, or can be internally generated by tying this pin to DGND.

Digital Inputs

$\overline{\text{HOLD}}$ - Hold, PIN 1.

A falling transition on this pin sets the CSZ5114 to the hold state and initiates a conversion. This input must remain low at least one master clock cycle plus 50ns.

$\overline{\text{CS}}$ - Chip Select, PIN 21.

When high, the data bus outputs are held in a high impedance state and the inputs to CAL and $\overline{\text{INTRLV}}$ are ignored. A falling transition initiates or terminates burst or interleave calibration (depending on the status of CAL and $\overline{\text{INTRLV}}$) and a rising transition latches both the CAL and $\overline{\text{INTRLV}}$ inputs. If $\overline{\text{RD}}$ is low, the data bus is driven as indicated by BW and A0.

$\overline{\text{RD}}$ - Read, PIN 22.

When $\overline{\text{RD}}$ and $\overline{\text{CS}}$ are both low, data is driven onto the data bus. If either signal is high, the data bus outputs are held in a high impedance state. The data driven onto the bus is determined by BW and A0.

A0 - Read Address, PIN 23.

Determines whether data or status information is placed onto the data bus. When high during the read operation, converted data is placed onto the data bus; when low, the status register is driven onto the bus.

BP/$\overline{\text{UP}}$ - Bipolar/Unipolar Input Select, PIN 24.

When high, the device is configured with a bipolar transfer function ranging from -VREF to +VREF. Encoding is in an offset binary format, with the mid-scale code 100...0000 centered at AGND. When low, the device is configured for a unipolar transfer function from AGND to VREF.

RST - Reset, PIN 32.

When taken high, all internal digital logic is reset. Upon returing low, a full calibration sequence is initiated.

BW - Bus Width Select, PIN 33.

When high, all 14 data bits are driven onto the bus simultaneously during a data read cycle. When low, the bus is in a byte wide format. On the first read following a conversion, the eight MSB's are driven onto D7-D0. A second read cycle places the six LSB's with two trailing zeroes on D7-D0. Subsequent reads will toggle the higher/lower order bytes of the same data until the next conversion completes. Regardless of BW's status, a read cycle with A0 low yields the status information on D7-D0.

$\overline{\text{INTRLV}}$ - Interleave, PIN 34.

When latched low using CS, the device goes into interleave calibration mode. A full calibration will complete every 72,192 conversions. The effective conversion time extends by 20 clock cycles.

CAL - Calibrate, PIN 35. (See note on page 59.)

When latched high using $\overline{\text{CS}}$, burst calibration results. The device cannot perform conversions during the calibration period which will terminate only once CAL is latched low again. Calibration picks up where the previous calibration left off, and calibration cycles complete every 1,443,840 master clock cycles. If the device is converting when a calibration is signaled, it will wait until that conversion completes before beginning calibration.

Analog Inputs

AIN - Analog Input, PIN 26.

Input range in the unipolar mode is zero volts to VREF. Input range in bipolar mode is -VREF to +VREF. The output impedance of buffer driving this input should be less than or equal to 200Ω.

VREF - Voltage Reference, PIN 28.

The analog reference voltage which sets the analog input range. It represents positive full scale for both bipolar and unipolar operation, and its magnitude sets negative full scale in bipolar mode.

Digital Outputs

D0 through D15 - Data Bus Outputs, PINS 2 thru 9, 12 thru 19.

Tri-state output pins. Enabled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$, they offer the converter's 14-bit output in a format consistent with the state of BW if A0 is high. If A0 is low, bits D0-D7 offer the status register.

$\overline{\text{EOT}}$ - End Of Track, PIN 37.

If low, indicates that enough time has elapsed since the last conversion for the device to acquire the analog input signal (3.75μs for 4MHz external clock).

$\overline{EOC}$ - End Of Conversion, PIN 38.

This output indicates the end of a conversion or reset calibration cycle. It is high during a conversion and will fall to a low state upon completion of the conversion cycle indicating valid data is available at the output. Returns high on the first subsequent read or the start of a new conversion cycle.

SDATA - Serial Output, PIN 40.

Presents each output data bit after it is determined by the successive approximation algorithm. Valid on the rising edge of SCLK, data appears MSB first, LSB last, and each bit remains valid until the next bit appears.

SCLK - Serial Clock Output, PIN 39.

Used to clock converted output data serially from the CSZ5114. Serial data is stable on the rising edge of SCLK.

Analog Outputs

REFBUF -Reference Buffer Output, PIN 29.

Reference buffer output. A 0.1µF ceramic capacitor must be tied between this pin and VA-.

Miscellaneous

TST - Test, PIN 31.

Allows access to the CSZ5114's test functions which are reserved for factory use. Must be tied to DGND.

ERROR DEFINITIONS

Peak Harmonic or Spurious Noise (More accurately, Signal to Peak Harmoninc or Spurious Noise) - The ratio of the rms value of the signal to the rms value of the next largest spectral component below the Nyquist rate (excepting dc). This component is often an aliased harmonic when the signal frequency is a significant proportion of the sampling rate. Expressed in decibels.

Total Harmonic Distortion - The ratio of the rms sum of all harmonics to the rms value of the signal. Units in percent.

Signal-to-Noise Ratio - Ratio of the rms value of the signal to the rms sum of all other spectral components below the Nyquist rate (excepting dc), including distortion components. Expressed in decibels.

Full Scale Error - The deviation of the last code transition from the ideal (VREF-3/2 LSB's) after all offsets have been externally compensated. Units in LSB's.

Unipolar Offset - The deviation of the first code transition from the ideal (1/2 LSB above AGND) when in unipolar mode (BP/$\overline{UP}$ low). Units in LSB's.

Bipolar Offset - The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below AGND) when in bipolar mode (BP/$\overline{UP}$ high). Units in LSB's.

Bipolar Zero - The deviation of the first code transition from the ideal (1/2 LSB above -VREF) when in bipolar mode (BP/$\overline{UP}$ high). Units in LSB's.

Aperture Time - The time required after the hold command for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

Aperture Jitter - The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

Note: Temperatures specified define ambient conditions in free-air during test and do not refer to the junction temperature of the device.

Ordering Guide

Model	Throughput	Temp Range	Package
CSZ5114-KP28	30 kHz	0 to 70 °C	40-Pin Plastic Dip
CSZ5114-KP14	56 kHz	0 to 70 °C	40-Pin Plastic Dip
CSZ5114-BC28	30 kHz	-40 to +85 °C	40-Pin Ceramic Side-Brazed Dip
CSZ5114-BC14	56 kHz	-40 to +85 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5114-TC14	56 kHz	-55 to +125 °C	40-Pin Ceramic Side-Brazed DIP

ADDENDUM

Burst Calibration

Burst calibration mode allows control of partial calibration cycles. Due to an unforeseen condition inside the part, asynchronous termination of calibration (CAL brought low) may result in a sub-optimal calibration result. It is recommended that burst calibration is not used, until the silicon is revised to prevent this effect.

The reset and interleave mode work perfectly, and should be used instead of burst mode. The CSZ5114's very low drift over temperature means that, under most circumstances, calibration need only be performed at power-up, using reset.

If you wish to use burst calibration, then please contact the factory for advice and new part availability information.

• Notes •

Semiconductor Corporation

CSZ5116

16-Bit, 50kHz Sampling A/D Converter

Features

- Monolithic CMOS A/D Converter
  - Inherent Sampling Architecture
  - 3-State Output Buffers
  - Microprocessor Interface
- Sampling Rates up to 50kHz
- Ultra-Low Distortion
  - Total Harmonic Distortion: 0.001%
  - Peak Harmonic or Noise: −104dB
- Low Power Dissipation: 120mW
- Pin Compatible with CSZ5112/CSZ5114

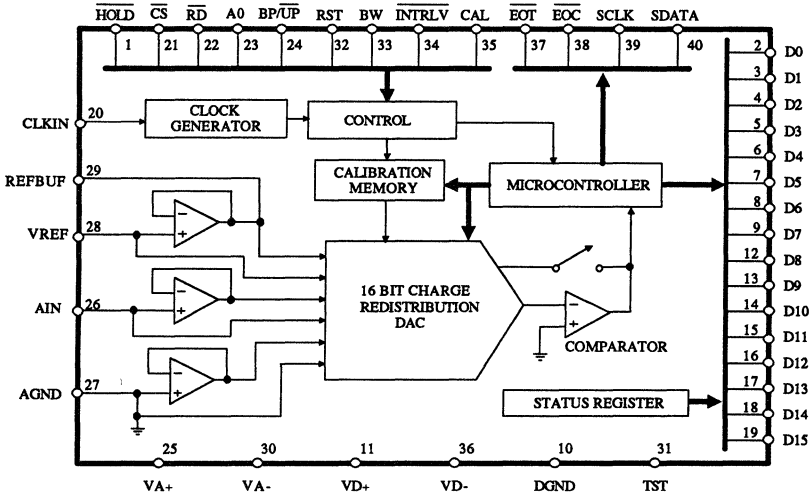
General Description

The CSZ5116 CMOS analog-to-digital converter is an ideal front-end for single- or multi-channel digital signal processing systems. It needs no external sample/hold amplifier at its input to convert ac signals - the sampling function is inherent to its charge redistribution design.

Using a standard successive-approximation algorithm, the CSZ5116 sequences through a 16-bit conversion in 16.25 microseconds. With 3.75 microseconds needed between conversions for acquisition, the CSZ5116 can support throughput rates up to 50kHz. It is therefore ideal for processing audioband signals.

The CSZ5116 features an on-chip self-calibration scheme which calibrates its bit weights to true 16-bit accuracy. This insures low distortion and maintains good signal-to-noise performance with low-level signals.

ORDERING INFORMATION: Page 89



S-to-Z™ Converter

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, Texas 78760
(512)445-7222 TWX:910-874-1352

ANALOG CHARACTERISTICS

(T_A = 25°C; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 4.5V;
Full-Scale Input Sinewave, 1kHz; f_{clk} = 4MHz for -16, 2MHz for -32; f_s = 50kHz for -16, 25kHz for -32;
Bipolar Mode ; Analog Source Impedance = 200Ω unless otherwise specified)

Parameter*		CSZ5116-J,K,L min	typ	max	CSZ5116-A,B,C min	typ	max	CSZ5116-S,T,U min	typ	max	Units
Specified Temperature Range			0 to 70			-40 to 85			-55 to 125		°C
Dynamic Performance											
Peak Harmonic or Spurious Noise											
	-J,A,S	92	94		92	94		92	94		dB
1kHz Input	-K,B,T	96	100		96	100		96	100		dB
T_{min} to T_{max}	-L,C,U	100	104		100	104		100	104		dB
(Note 1)	-J,A,S	82	84		82	84		82	84		dB
12kHz Input	-K,B,T	85	88		85	88		85	88		dB
	-L,C,U	85	91		85	91		85	91		dB
Total Harmonic Distortion											
	-J,A,S		0.004			0.004			0.004		%
	-K,B,T		0.002			0.002			0.002		%
	-L,C,U		0.001			0.001			0.001		%
Signal-to-Noise Ratio											
	-J,A,S	84	87		84	87		84	87		dB
0dB Input	-K,B,T	87	90		87	90		87	90		dB
T_{min} to T_{max}	-L,C,U	90	92		90	92		90	92		dB
	-J,A,S		27			27			27		dB
-60dB Input	-K,B,T		30			30			30		dB
(Note 2)	-L,C,U		32			32			32		dB
dc Accuracy											
Differential Linearity	(Note 3)	16			16			16			Bits
Full Scale Error	T_{min} to T_{max}		±2			±2			±2		LSB
Unipolar Offset	T_{min} to T_{max}		±1			±1			±1		LSB
Bipolar Offset	T_{min} to T_{max}		±1			±1			±1		LSB
Bipolar Zero Error	T_{min} to T_{max}		±2			±2			±2		LSB

Notes: 1. All T_{min} to T_{max} specifications apply after calibration at the temperature of interest.
2. A detailed plot of S/(N+D) vs. input amplitude appears on page 79.
3. Minimum resolution for which no missing codes is guaranteed.

*Refer to *Error Definitions* on page 88.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter	CSZ5116-J,K,L min	typ	max	CSZ5116-A,B,C min	typ	max	CSZ5116-S,T,U min	typ	max	Units
Analog Input										
Aperture Time		25			25			25		ns
Aperture Jitter		100			100			100		ps
Full Power Bandwidth (Note 4)		25			25			25		kHz
Input Capacitance Unipolar Mode		275	375		275	375		275	375	pF
(Note 5) Bipolar Mode		165	220		165	220		165	220	pF
Conversion & Throughput										
Conversion Time –16			16.25			16.25			16.25	us
(Notes 6, 7) –32			32.5			32.5			32.5	us
Acquisition Time –16		3.0	3.75		3.0	3.75		3.0	3.75	us
(Note 7) –32		4.5	5.25		4.5	5.25		4.5	5.25	us
Throughput –16	50			50			50			kHz
(Note 7) –32	26.5			26.5			26.5			kHz
Power Supplies										
Power Supply Currents (Note8)										
I_{A+}		9	19		9	19		9	19	mA
I_{A-}		–9	–19		–9	–19		–9	–19	mA
I_{D+}		3	6		3	6		3	6	mA
I_{D-}		–3	–6		–3	–6		–3	–6	mA
Power Dissipation (Note 8)		120	250		120	250		120	250	mW
Power Supply Rejection (Note 9)										
Positive Supplies		84			84			84		dB
Negative Supplies		84			84			84		dB

Notes:
4. Refer to the *Analog Input* section on page 75 for a discussion of input slew capabilities.
5. Applies only in the track mode. When converting or calibrating, input capacitance will not exceed 15pF.
6. Measured from falling transition on $\overline{HOLD}$ to falling transition on $\overline{EOC}$.
7. Conversion, acquisition, and throughput times depend on the master clock, sampling, and calibration conditions. The numbers shown assume sampling and conversion is synchronized with the CSZ5116's conversion clock, interleave calibrate is disabled, and operation is from the full-rated external clock. A detailed discussion of conversion timing appears on page 69.
8. All outputs unloaded. All inputs CMOS levels.
9. With 300mV p-p, 1kHz ripple applied to each supply separately in the bipolar mode. Rejection improves by 6dB in the unipolar mode to 90dB. A plot of typical power supply rejection appears on page 82.

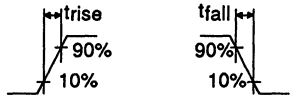
7

SWITCHING CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 50pF)

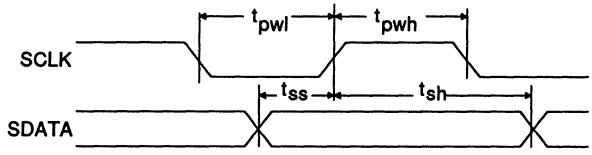
Parameter	Symbol	Min	Typ	Max	Units
Master Clock Frequency:					
Internally Generated: -16	f_{CLK}	2	-	-	MHz
-32		1	-	-	
Externally Supplied: -16		-	-	4	
-32		-	-	2	
Master Clock Duty Cycle	-	30	-	70	%
Rise Times: Any Digital Input	t_{rise}	-	-	1.0	us
Any Digital Output		-	20	-	ns
Fall Times: Any Digital Input	t_{fall}	-	-	1.0	us
Any Digital Output		-	20	-	ns
$\overline{HOLD}$ Pulse Width	t_{hpw}	$1/f_{CLK} + 50$	-	t_c	ns
Conversion Time	t_c	(Note 10)	-	(Note 10)	us
Data Delay Time	t_{dd}	-	40	100	ns
$\overline{EOC}$ Pulse Width (Note 11)	t_{epw}	$4/f_{CLK} - 20$	-	-	ns
Set Up Times: CAL, $\overline{INTRLV}$ to $\overline{CS}$ Low	t_{cs}	20	10	-	ns
A0 to $\overline{CS}$ and $\overline{RD}$ Low	t_{as}	20	10	-	
Hold Times:					
$\overline{CS}$ or $\overline{RD}$ High to A0 Invalid	t_{ah}	50	30	-	ns
$\overline{CS}$ High to CAL, $\overline{INTRLV}$ Invalid	t_{ch}	50	30	-	
Access Times: $\overline{CS}$ Low to Data Valid					
-J, K, L, A, B, C	t_{ca}	-	90	120	ns
-S, T, U		-	115	150	
$\overline{RD}$ Low to Data Valid					
-J, K, L, A, B, C	t_{ra}	-	90	120	ns
-S, T, U		-	115	150	
Output Float Delay: -J, K, L, A, B, C	t_{fd}	-	50	110	ns
$\overline{CS}$ or $\overline{RD}$ High to Output Hi-Z -S, T, U			50	140	
Serial Clock Pulse Width Low	t_{pwl}	-	$2/f_{CLK}$	-	ns
Pulse Width High	t_{pwh}	-	$2/f_{CLK}$	-	
Set Up Times: SDATA to SCLK Rising	t_{ss}	$2/f_{CLK} - 100$	$2/f_{CLK}$	-	ns
Hold Times: SCLK Rising to SDATA	t_{sh}	$2/f_{CLK} - 100$	$2/f_{CLK}$	-	ns

Notes: 10. See Table 1 and master clock frequencies above.

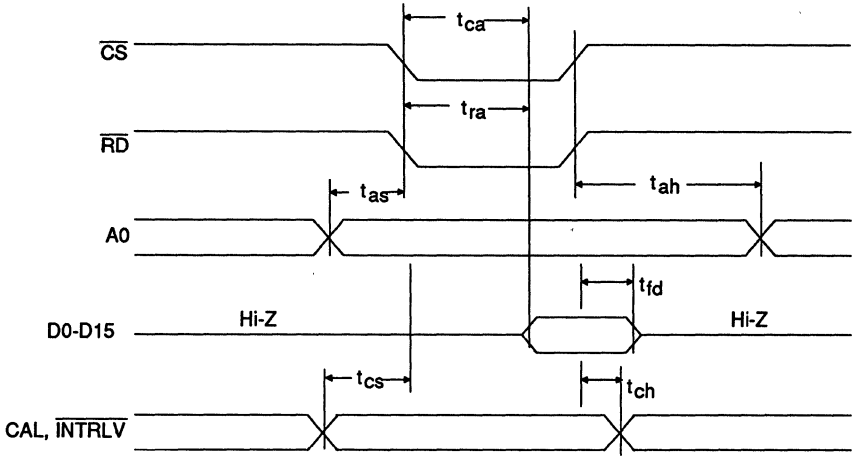
11. $\overline{EOC}$ remains low 4 master clock cycles if $\overline{CS}$ and $\overline{RD}$ are held low. Otherwise, It returns high within four master clock cycles from the start of a data read operation or a conversion cycle.



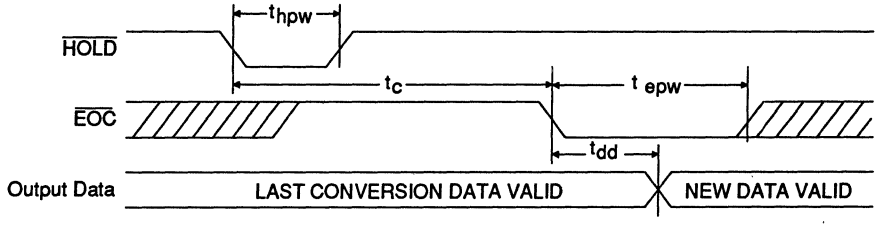
Rise and Fall Times



Serial Output Timing



Read and Calibration Control Timing



Conversion Timing

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 12)	V_{OH}	VD+ - 1.0V	-	-	V
Low-Level Output Voltage Iout=1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	10	uA
3-State Leakage Current	I_{OZ}	-	-	±10	uA
Digital Output Pin Capacitance	C_{out}	-	9	-	pF

Note: 12. I_{OUT} = -100µA. This specification guarantees TTL compatibility (VOH = 2.4V @ Iout = -40µA).

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see Note 13.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.5	5.0	VA+	V
	Negative Digital	VD-	−4.5	−5.0	−5.5	V
	Positive Analog	VA+	4.5	5.0	5.5	V
	Negative Analog	VA-	−4.5	−5.0	−5.5	V
Analog Reference Voltage		VREF	2.5	4.5	VA+ - 0.5	V
Analog Input Voltage: (Note 14)	Unipolar	V_{AIN}	AGND	-	VREF	V
	Bipolar	V_{AIN}	-VREF	-	VREF	V

Notes: 13. All voltages with respect to ground.
14. The CSZ5116 can accept input voltages up to the analog supplies (VA+ and VA-). It will produce an output of all 1's for inputs above VREF and all 0's for inputs below AGND in unipolar mode and -VREF in bipolar mode.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to ground)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	−0.3	VA+ + 0.3	V
	Negative Digital	VD-	0.3	−6.0	V
	Positive Analog	VA+	−0.3	6.0	V
	Negative Analog	VA-	0.3	−6.0	V
Input Current, Any Pin Except Supplies (Note 15)		I_{in}	-	±10	mA
Analog Input Voltage (AIN and VREF pins)		V_{INA}	VA- - 0.3	VA+ + 0.3	V
Digital Input Voltage		V_{IND}	−0.3	VD+ + 0.3	V
Ambient Operating Temperature		T_A	−55	125	°C
Storage Temperature		T_{stg}	−65	150	°C

Note: 15. Transient currents of up to 100mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

THEORY OF OPERATION

The CSZ5116 utilizes the most popular method of executing high-speed, high-resolution A/D conversion: successive approximation. As with all other iterative comparison methods, the analog input is successively compared to the output of a D/A converter controlled by the conversion algorithm. Successive approximation begins by comparing the input to the DAC output set to half-scale (MSB on, all other bits off). If the input is found to be below half-scale, the MSB is reset to zero and the input is compared to one-quarter scale (next-MSB on, all others off). If the input were above half-scale, the MSB would remain high and the next comparison would be at three-quarters of full scale. This procedure continues until all bits have been exercised.

The CSZ5116 implements the successive-approximation algorithm using a unique charge-redistribution architecture. Instead of the traditional resistor network, the DAC is an array of binary-weighted capacitors. All legs of the array share a common node at the comparator's input, with their other terminals capable of being connected to AIN, AGND, or VREF (Figure 1). When the device is not calibrating or converting, all bits are tied to AIN forming C_{tot}. Switch S1 is closed and the charge on the array, Q_{in}, tracks the input signal V_{in} (Figure 2a).

When the conversion command is issued, switch S1 opens as shown in Figure 2b. This traps charge Q_{in} on the comparator side of the capacitor array and creates a floating node at the comparator's input. The conversion algorithm operates on this fixed charge, and the signal at the analog input pin is ignored. In effect, the entire DAC capacitor array serves as analog memory during conversion much like a hold capacitor in a sample/hold amplifier.

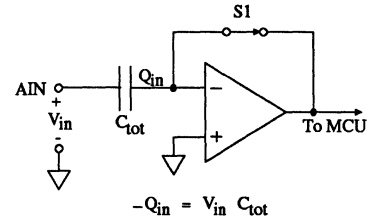


Figure 2a. Tracking Mode

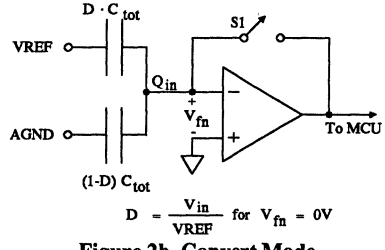


Figure 2b. Convert Mode

The conversion consists of manipulating the free plates of the capacitor array to VREF and AGND to form a capacitive divider. Since the charge at the floating node remains fixed, the voltage at that point depends on the proportion of

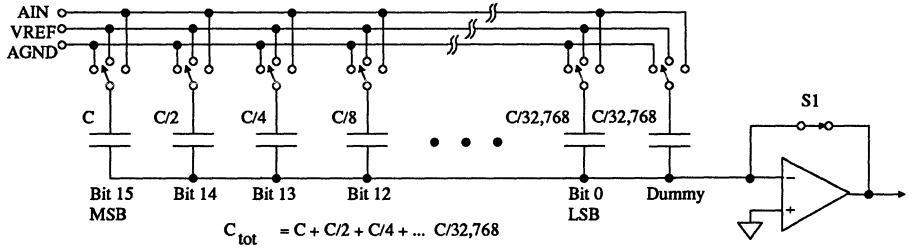


Figure 1. Charge Redistribution DAC

capacitance tied to VREF versus AGND. The successive-approximation algorithm is used to find the proportion of capacitance, termed D in Figure 2b, which will drive the voltage at the floating node to zero. That binary fraction of capacitance represents the converter's digital output.

The CSZ5116's charge redistribution architecture easily supports bipolar input ranges. If half the capacitor array (the MSB capacitor) is tied to VREF rather than AIN in the track mode, the input range doubles and offsets half-scale. The magnitude of the reference voltage thus defines both positive and negative full-scale (-VREF to +VREF), and the digital code is an offset binary representation of the input.

Calibration

The ability of the CSZ5116 to convert accurately to 16-bits clearly depends on the accuracy of its comparator and DAC. The CSZ5116 utilizes an "auto-zeroing" scheme to null errors introduced by the comparator. All offsets are stored on the capacitor array while in the track mode and are effectively subtracted from the input signal when a conversion is initiated. Auto-zeroing enhances power supply rejection at frequencies below the conversion rate.

To achieve 16-bit accuracy from the DAC, the CSZ5116 uses a novel self-calibration scheme. Each bit capacitor shown in Figure 1 actually consists of several capacitors which can be manipulated to adjust the overall bit weight. During calibration, an on-chip microcontroller manipulates the sub-arrays to precisely ratio the bits. Each bit is adjusted to just balance the sum of all less significant bits plus one dummy LSB (for example, 16C = 8C + 4C + 2C + C + C). During calibration, the CSZ5116 implements statistical noise reduction to calibrate accurately to ± 1/4 LSB. It performs multiple experiments per calibration decision to reduce the effective noise bandwidth and the probability of making an incorrect decision. The resulting probability of obtaining a 1/4 LSB error is less than one in a thousand, with a negligible chance of obtaining a calibration error of 1/2 LSB.

DIGITAL CIRCUIT CONNECTIONS

The CSZ5116 can be applied in a wide variety of master clock, sampling, and calibration conditions which directly affect the device's conversion time and throughput. The device also features on-chip 3-state output buffers and a complete interface for connecting to 8- and 16-bit digital systems. Output data is also available in serial format.

Master Clock

The CSZ5116 operates from a master clock which can be externally supplied or internally generated. The internal oscillator is activated by hard-wiring the CLKIN input low. Alternatively, the CSZ5116 can be synchronized to the external system by driving the CLKIN pin with a TTL or CMOS clock signal.

a. Asynchronous Sampling

b. Synchronous Sampling

Figure 3. Sampling Connections

All calibration, conversion, and throughput times directly scale to master clock frequency. Thus, throughput can be precisely controlled and/or maximized using an external master clock. In contrast, the CSZ5116's internal oscillator will vary from unit-to-unit and over temperature. Its tolerance gives rise to minimum and maximum conversion times and throughput rates. The -16 version of the CSZ5116 is specified for accurate operation with an external clock up to 4MHz; its internal clock frequency is specified at a minimum of 2.0MHz. The -32 version can handle external clocks up to 2MHz; its internal clock can range as low as 1.0MHz (see *Switching Characteristics*, page 64).

Sampling/Initiating Conversions

A falling transition on the $\overline{\text{HOLD}}$ pin places the input in the hold mode and initiates a conversion cycle. The $\overline{\text{HOLD}}$ input is latched internally by the master clock, so it can return high anytime after one master clock cycle plus 50ns. Upon completion of the conversion cycle, the CSZ5116 automatically returns to the track mode. In contrast to systems with separate track-and-holds and A/D converters, a sampling clock can simply be connected to the $\overline{\text{HOLD}}$ input (Figure 3a). The duty cycle of this clock is not critical. It need only remain low at least one master clock cycle plus 50ns, but no longer than the minimum conversion time or an additional conversion cycle will be initiated with inadequate time for acquisition.

Conversion Time/Throughput

Upon completing a conversion cycle and returning to the track mode, the CSZ5116 requires time to acquire the analog input signal before another conversion can be initiated. The acquisition time is specified as six master clock cycles plus 2.25µs. This adds to the conversion time to define the converter's maximum throughput. The conversion time of the CSZ5116, in turn, depends on the sampling, calibration, and master clock conditions.

Asynchronous Sampling

The CSZ5116 internally operates from a clock which is delayed and divided down from the master clock ($f_{CLK}/4$). If sampling is not synchronized to this internal clock, the conversion cycle may not begin until up to four clock cycles after $\overline{\text{HOLD}}$ goes low even though the charge is trapped immediately. In this asynchronous mode (Figure 3a), the four clock cycles add to the minimum 65 clock cycles to define the maximum conversion time (see Figure 4a and Table 1).

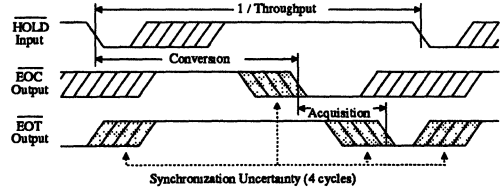


Figure 4a. Asynchronous Sampling (External Clock)

	Conversion Time		Throughput Time	
Sampling Mode	min	max	min	max
Synchronous (Loopback)	65T	65T	80T	80T
Asynchronous	65T	69T + 235ns	N/A	75T + 2.25µs

(T ≡ one master clock cycle)

Table 1. Conversion and Throughput Times

Synchronous Sampling

To achieve maximum throughput, sampling can be synchronized with the internal conversion clock by connecting the End-of-Track ($\overline{EOT}$) output to $\overline{HOLD}$ (Figure 3b). The $\overline{EOT}$ output falls 15 master clock cycles after $\overline{EOC}$ indicating the analog input has been acquired to the CSZ5116's specified accuracy. The $\overline{EOT}$ output is synchronized to the internal conversion clock, so the four clock cycle synchronization uncertainty is removed yielding throughput at 1/80th of the master clock frequency (see Figure 4b and Table 1).

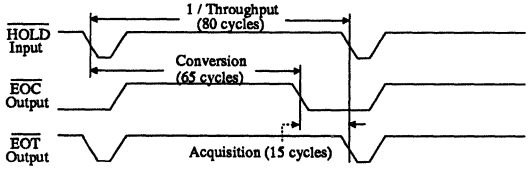


Figure 4b. Synchronous (Loopback) Mode

Also, the CSZ5116's internal RC oscillator exhibits significant jitter (typically ± 0.05% of its period), which is high compared to crystal oscillators. If the CSZ5116 is configured for synchronous sampling while operating from its internal oscillator, this jitter will directly affect sampling purity.

The $\overline{EOT}$ output is an accurate indicator of the CSZ5116's acquisition requirement when operating at the -16 version's full rated speed (3.75µs with a 4MHz master clock). However, $\overline{EOT}$ will allow the CSZ5116 more acquisition time than necessary when operating with a clock less than 4MHz. The $\overline{EOT}$ output always falls 15 master clock cycles after $\overline{EOC}$. The CSZ5116 only needs 3.75µs (six cycles @4MHz plus 2.25µs). When operating the -32 with a master clock of 2MHz or less, higher throughput can be achieved than in the loopback configuration by using an external counter. The counter should be reset by the falling edge of $\overline{EOC}$ and count the appropriate number of clock cycles after each conversion. When the total time is greater than six clock cycles plus 2.25µs the counter can trigger a new conversion at $\overline{HOLD}$. For example, when using a 2MHz clock, 2.25µs takes between four and five clock cycles. When six cycles are added to this it is seen that the counter should trigger a new conversion at the eleventh clock cycle.

Reset

Upon power up, the CSZ5116 must be reset to guarantee a consistent starting condition and initially calibrate the device. Due to the CSZ5116's low power dissipation and low temperature drift, no warm-up time is required before reset to accommodate any self-heating effects. However, the voltage reference input should have stabilized to within 0.25% of its final value before RST falls to guarantee an accurate calibration. Later, the CSZ5116 may be reset at any time to initiate a single full calibration. Reset overrides all other functions. If reset, the CSZ5116 will clear and initiate a new calibration cycle mid-conversion or mid-calibration.

Resets can be initiated in hardware or software. The simplest method of resetting the CSZ5116 involves strobing the RST pin high. When RST is brought high all internal logic clears. When it returns low a full calibration begins which takes 1,443,840 master clock cycles (approximately

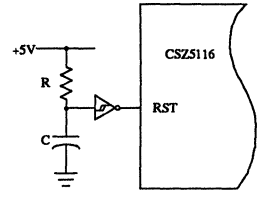


Figure 5. Power-On Reset Circuitry

360ms with a 4MHz clock) to complete. A simple power-on reset circuit can be built using a resistor and capacitor, and a Schmidt-trigger inverter to prevent oscillation (see Figure 5). The CSZ5116 can also be reset in software when under microprocessor control. The CSZ5116 will reset whenever $\overline{CS}$, A0, and $\overline{HOLD}$ are taken low simultaneously. See the *Microprocessor Interface* section to eliminate the possibility of inadvertent software reset. The $\overline{EOC}$ output remains high throughout the reset operation and will fall upon its completion. It can thus be used to generate an interrupt indicating the CSZ5116 is ready for operation. Six master clock cycles plus 2.25µs must be allowed after $\overline{EOC}$ falls to allow for acquisition. Under microprocessor-independent operation with 3-states permanently enabled ($\overline{CS}$, $\overline{RD}$ low; AO high) the $\overline{EOC}$ output will not fall at the completion of the reset operation.

Initiating Calibration

All modes of calibration can be controlled in hardware or software. Accuracy can thereby be insured at any time or temperature throughout operating life. After initial calibration at power-up, the CSZ5116's charge-redistribution design yields better temperature drift and more graceful aging than resistor-based technologies, so calibration is actually required less often than with traditional devices.

The first mode of calibration, reset, results in a single full calibration cycle. The second type of calibration, termed "burst" cal, is useful when the ADC sees some downtime but not enough to perform a full reset calibration. Burst cal can be terminated mid-calibration; it picks up where it left off previously, so calibrations can be done in piecemeal fashion. Burst cal is initiated by bringing the CAL input high with $\overline{CS}$ low. The CAL input is level-triggered and latches on the rising edge of $\overline{CS}$, so a write cycle can be used to control calibration in software. Burst cal will continue to loop through calibration cycles until terminated. Once CAL returns low, at least 26 master clock cycles plus 2.25µs (8.75µs @ 4MHz clock) must be allowed before a conversion is initiated to ensure the CSZ5116 has completed its calibration experiment and has acquired the analog input. The $\overline{EOC}$ output indicates the completion of the final calibration experiment. (See note on page 89.)

The CSZ5116 features a background calibration mode called "interleave." Interleave appends a single calibration experiment to each conversion cycle and thus requires no dead time for calibration. The CSZ5116 gathers data between conversions and will adjust its transfer function once it completes the entire sequence of experiments (one calibration cycle per 72,192 conversions). Initiated by bringing both the $\overline{INTRLV}$ input and $\overline{CS}$ low (or hard-wiring $\overline{INTRLV}$ low), interleave extends the CSZ5116's effective conversion time by 20 master clock cycles. Other than reduced throughput, interleave is totally transparent to the user.

Burst calibrations initiated at CAL pick up where interleave left off, so calibration cycles can be hastened by "bursting" a number of experiments whenever the CSZ5116 sees free time. Interleave is subordinate to burst calibrations, so $\overline{INTRLV}$ could still be hard-wired low.

Microprocessor Interface

The CSZ5116 features an intelligent microprocessor interface which offers detailed status

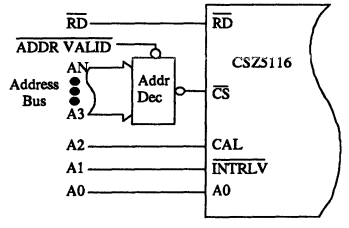


Figure 6. Address/Control Bus Connections

PIN	STATUS BIT	STATUS	DEFINITION
D0	S0	$\overline{\text{END OF CONVERSION}}$	Falls upon completion of a conversion, and returns high on the first subsequent read.
D1	S1	RESERVED	Reserved for factory use.
D2	S2	LOW BYTE/$\overline{\text{HIGH BYTE}}$	When data is to be read in an 8-bit format (BW=0), indicates which byte will appear at the output next.
D3	S3	$\overline{\text{END OF TRACK}}$	When low, indicates the input has been acquired to the devices specified accuracy.
D4	S4	RESERVED	Reserved for factory use.
D5	S5	TRACKING	High when the device is tracking the intput.
D6	S6	CONVERTING	High when the device is converting the held input.
D7	S7	CALIBRATING	High when the device is calibrating.

Table 2. Status Bit Definitions

information and allows software control of the self-calibration functions. Output data is available in either 8- or 16-bit formats for easy interfacing to industry-standard microprocessors.

Strobing both $\overline{CS}$ and $\overline{RD}$ low enables the CSZ5116's 3-state output buffers with either output data or status information depending on the status of A0. An address bit can be connected to A0 as shown in Figure 6 thereby memory mapping the status register and output data. Conversion status can be polled in software by reading the status register ($\overline{CS}$ and $\overline{RD}$ strobed low with A0 low), and masking status bits S0-S5 and S7 (by logically AND'ing the status word with 01000000) to determine the value of S6. Similarly, the software routine can determine calibration status using other status bits (see Table 2). *Care must be taken not to read the status register (A0 low) while $\overline{HOLD}$ is low, or a software reset will result* (see *Reset*, page 70).

Alternatively, the End-of-Convert ($\overline{EOC}$) output can be used to generate an interrupt or drive a DMA controller to dump the output directly into memory after each conversion. The $\overline{EOC}$ pin falls as each conversion cycle is completed and data is valid at the output. It returns high within four master clock cycles of the first subsequent data read operation or after the start of a new conversion cycle. To interface with 16-bit data busses, the BW input to the CSZ5116 should be held high and all 16 data bits read in parallel. With 8-bit buses, the converter's 16-bit result must be read in two 8-bit bytes. In this instance, BW should be held low and the MSB's obtained on the first read cycle following a conversion and the LSB's on the second. Both bytes appear on pins D0-D7. The upper/lower bytes of the same data will continue to toggle on subsequent reads until the next conversion finishes. Status bit S4 indicates which byte will appear on the next data read operation.

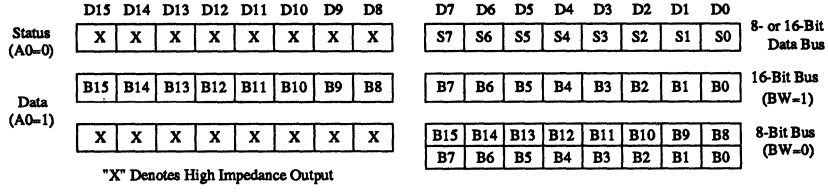


Figure 7. Data Format

The CSZ5116 internally buffers its output data, so data can be read while the device is tracking or converting the next sample. Therefore, retrieving the converter's digital output requires no reduction in ADC throughput. Enabling the 3-state outputs while the CSZ5116 is converting will not introduce conversion errors. When TTL loads are utilized the potential for crosstalk between digital and analog sections of the system is increased. This crosstalk is due to high digital supply and signal currents arising from the TTL drive current required of each digital output. Connecting CMOS logic to the digital outputs is recommended. Suitable logic families include 4000B, 74HC, 74AC, 74ACT, and 74HCT.

The two calibration control inputs, CAL and $\overline{\text{INTRLV}}$, are level-triggered and latched on the rising edge of $\overline{\text{CS}}$. Calibration can be placed under software control by connecting address lines to the CAL and $\overline{\text{INTRLV}}$ inputs as shown in Figure 6. Any read or write cycle to the CSZ5116's base address will thereby initiate or terminate calibration.

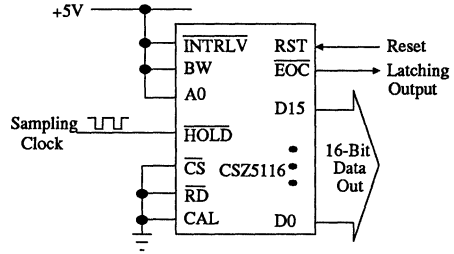
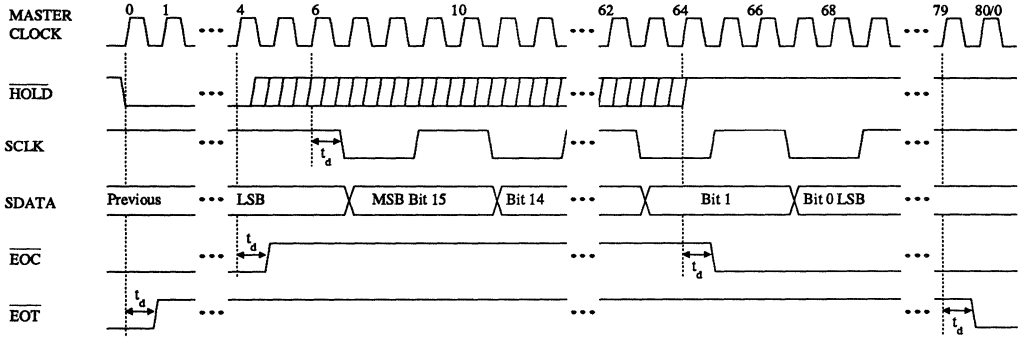


Figure 8. Microprocessor-Independent Connections

Microprocessor Independent Operation

The CSZ5116 can be operated in a stand-alone mode independent of intelligent control. In this mode, $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are hard-wired low permanently enabling the 3-state output buffers. A free-running condition is established when BW is tied high, CAL is tied low, and $\overline{\text{HOLD}}$ is continually strobed low or tied to $\overline{\text{EOT}}$. The CSZ5116's $\overline{\text{EOC}}$ output can be used to externally latch the output data if desired. With $\overline{\text{CS}}$ and $\overline{\text{RD}}$ hard-wired low, $\overline{\text{EOC}}$ will strobe low for four master clock cycles after each conversion. Data will be unstable up to 100ns after $\overline{\text{EOC}}$ falls, so it should be latched on the rising edge of $\overline{\text{EOC}}$.



notes: 1. t_d can vary from 135ns - 235ns over military temerature range and over ± 10% supply variation.
2. For asynchronous mode, transitions of SCLK, SDATA, $\overline{\text{EOC}}$, $\overline{\text{EOT}}$ can shift by up to 4 clocks; e.g. the first high to low transition of SCLK may be on clock #6 to #9. The timing relationship between SCLK, SDATA, $\overline{\text{EOC}}$, and $\overline{\text{EOT}}$ is fixed.

Figure 9. Serial Output Timing

Serial Output

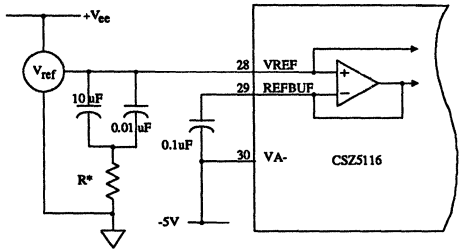
All successive-approximation A/D converters derive their digital output serially starting with the MSB. The CSZ5116 presents each bit to the SDATA pin four master clock cycles after it is derived and can be latched using the serial clock output, SCLK. Just subsequent to each bit decision SCLK will fall and return high once the bit information on SDATA has stabilized. Thus, the rising edge of the SCLK output should be used to clock the data from the CSZ5116 (See Figure 9).

ANALOG CIRCUIT CONNECTIONS

Most popular successive-approximation A/D converters generate dynamic loads at their analog connections. The CSZ5116 internally buffers all analog inputs (AIN, VREF, and AGND) to ease the demands placed on external circuitry. However, accurate system operation still requires careful attention to details at the design stage regarding source impedances as well as grounding and decoupling schemes.

Reference Considerations

An application note titled "*Voltage references for the CS501X/CSZ511X Series of A/D Converters*" is available for the CSZ5116. In addition to working through a reference circuit design example, it offers seven built-and-tested reference circuits.



$$R = \frac{1}{2\pi (C_1 + C_2) f_{peak}}$$

Figure 10. Reference Connections

During conversion, the members of the calibrated capacitor array are switched between VREF and AGND in a manner determined by the successive-approximation algorithm. The charging and discharging of the array results in a current load at the reference. The CSZ5116 includes an internal buffer amplifier to minimize the external reference circuit's drive requirement and preserve the reference's integrity. Whenever the array is switched during conversion, the buffer is used to pre-charge the array thereby providing the bulk of the necessary charge. The appropriate array capacitors are then switched to the unbuffered VREF pin to avoid any errors due to offsets and/or noise in the buffer.

The external reference circuitry need only provide the residual charge required to fully charge the array after pre-charging from the buffer. This creates an ac current load as the CSZ5116 sequences through conversions. The reference circuitry must have a low enough output impedance to drive the requisite current without changing its output voltage significantly.

As the analog input signal varies, the switching sequence of the internal capacitor array changes. The current load on the external reference circuitry thus varies in response with the analog input. Therefore, the external reference must not exhibit significant peaking in its output impedance characteristic at signal frequencies or their harmonics.

A large capacitor connected between VREF and AGND can provide sufficiently low output impedance at the high end of the frequency spectrum, while almost all precision references exhibit extremely low output impedance at dc. The presence of large capacitors on the output of some voltage references, however, may cause peaking in the output impedance at intermediate frequencies. Care should be exercised to ensure that significant peaking does not exist or that some form of compensation is provided to eliminate the effect.

The magnitude of the current load on the external reference circuitry will scale to the master clock frequency. At full speed (4MHz clock), the reference must supply a maximum load current of 10µA peak-to-peak (1µA typical). An output impedance of 2Ω will therefore yield a maximum error of 20µV. With a 4.5V reference and LSB size of 69µV this would insure approximately 1/4 LSB accuracy. A 10µF capacitor exhibits an impedance of less than 2Ω at frequencies greater than 16kHz, and voltage references with dc output impedances less than one 2Ω are readily available. A high-quality tantalum capacitor in parallel with a smaller ceramic capacitor is recommended.

Peaking in the reference's output impedance can occur because of capacitive loading at its output. Any peaking that might occur can be reduced by placing a small resistor in series with the capacitors (Figure 10). The equation in Figure 10 can be used to help calculate the optimum value of R for a particular reference. The term "f_{peak}" is the frequency of the peak in the output impedance of the reference before the resistor is added.

The CSZ5116 can operate with a wide range of reference voltages, but signal-to-noise performance is maximized by using as wide a signal range as possible. The recommended reference voltage is 4.5 volts. The CSZ5116 can actually accept reference voltages up to the positive analog supply. However, the buffer's offset may increase as the reference voltage approaches VA+ thereby increasing external drive requirements at VREF. A 4.5V reference is the maximum reference voltage recommended. This allows 0.5V headroom for the internal reference buffer. Also, the buffer enlists the aid of an external 0.1µF ceramic capacitor which must be tied between its output, REFBUF, and the negative analog supply, VA-. For more information on references, consult "Application Note: *Voltage References for the CS501X CSZ511X Series of A/D Converters*".

Analog Input Connection

The analog input terminal functions similarly to the VREF input after each conversion when switching into the track mode. During the first six master clock cycles in the track mode, the buffered version of the analog input is used for pre-charging the capacitor array. An additional period is required for fine-charging directly from AIN to obtain the specified accuracy. Figure 11 exemplifies this operation. During pre-charge the charge on the capacitor array first settles to the buffered version of the analog input. This voltage is offset from the actual input voltage. During fine-charge, the charge then settles to the accurate unbuffered version.

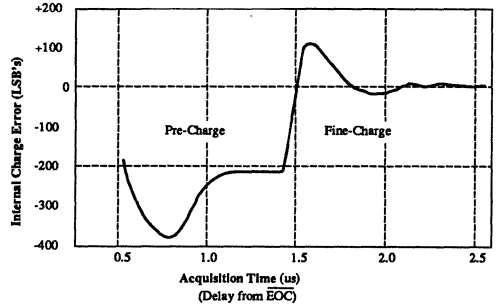


Figure 11. Internal Acquisition Time

The acquisition time of the CSZ5116 depends on the master clock frequency. This is due to a fixed pre-charge period. For instance, operating the -16 version with an external 4MHz master clock results in a 3.75µs acquisition time: 1.5µs for pre-charging (6 clock cycles) and 2.25µs for fine-charging. Fine-charge settling is specified as a maximum of 2.25µs for an analog source impedance of less than 200Ω.

In addition, the comparator requires a source impedance of less than 400Ω around 2MHz for stability, which is met by practically all bipolar op amps. Large dc source impedances can be accommodated by adding capacitance from AIN

to ground (typically 200pF) to decrease source impedance at high frequencies. However, high dc source resistances will increase the input's RC time constant and extend the necessary acquisition time.

The CSZ5116 can track full power signals up to 25kHz in the track mode. During the first six clock cycles following a conversion, the CSZ5116 is capable of slewing at 5V/µs in unipolar mode. In bipolar mode, only half the capacitor array is connected to the analog input so the CSZ5116 can slew at 10V/µs. After the first six master clock cycles, it will slew at 0.25V/µs in the unipolar mode and 0.5V/µs in bipolar mode. Acquisition of fast slewing signals (step functions) can be hastened if the step occurs during or immediately following the conversion cycle. For instance, channel selection in multiplexed applications should occur while the CSZ5116 is converting (see Figure 12). Multiplexer settling is thereby removed from the overall throughput equation, and the CSZ5116 can convert at full speed.

Analog Input Range/Coding Format

The reference voltage directly defines the input voltage range in both the unipolar and bipolar configurations. In the unipolar configuration (BP/$\overline{UP}$ low), the first code transition occurs 0.5 LSB above AGND, and the final code transition occurs 1.5 LSB's below VREF. Coding is in straight binary format. In the bipolar configuration (BP/$\overline{UP}$ high), the first code transition occurs 0.5 LSB above -VREF and the last transition occurs 1.5 LSB's below +VREF. Coding is in an offset-binary format. Positive full scale gives a digital output of 1111111111111111, and negative full scale gives a digital output of 0000000000000000.

Grounding and Power Supply Decoupling

The CSZ5116 uses the analog ground connection, AGND, only as a reference voltage. No dc power currents flow through the AGND connection, and it is completely independent of DGND. However, any noise riding on the AGND input relative to the system's analog ground will induce conversion errors. Therefore, both the analog input and reference voltage should be referred to the AGND pin, which should be used as the entire system's analog ground. The digital and analog supplies are isolated within the CSZ5116 and are pinned out separately to minimize coupling between the analog and digital sections of the chip. All four supplies should be decoupled to their respective grounds using 0.1µF ceramic capacitors. If significant lowfrequency noise is present on the supplies, 1µF tantalum capacitors are recommended in parallel with the 0.1µF capacitors.

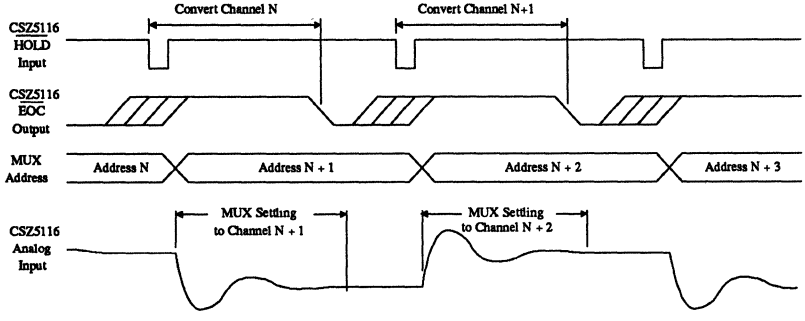


Figure 12. Pipelined MUX Input Channels

The positive digital power supply of the CSZ5116 must never exceed the positive analog supply by more than a diode drop or the CSZ5116 could experience permanent damage. If the two supplies are derived from separate sources, care must be taken that the analog supply comes up first at power-up. The system connection diagram on page 83 shows a decoupling scheme which allows the CSZ5116 to be powered from a single set of ± 5V rails. The positive digital supply is derived from the analog supply through a 10Ω resistor to avoid the analog supply dropping below the digital supply. If this scheme is utilized, care must be taken to insure that any digital load currents (which flow through the 10Ω resistors) do not cause the magnitude of digital supplies to drop below the analog supplies by more than 0.5 volts. Digital supplies must always remain above the minimum specification.

As with any high-precision A/D converter, the CSZ5116 requires careful attention to grounding and layout arrangements. However, no unique layout issues must be addressed to properly apply the CSZ5116. The CDB5116 evaluation board is available for the CSZ5116, which avoids the need to design, build, and debug a high-precision PC board to initially characterize the part. The board comes with a socketed CSZ5116, and can be quickly reconfigured to simulate any combination of sampling, calibration, master clock, and analog input range conditions.

CSZ5116 PERFORMANCE

The CSZ5116 offers 100% tested dynamic performance. Due to the broad range of operating conditions and performance requirements in signal processing applications, the following section is included to illustrate the CSZ5116's error sources and their effect on a signal's spectral content.

FFT Tests and Windowing

In the factory, the CSZ5116 is tested using Fast Fourier Transform (FFT) techniques to analyze the converter's dynamic performance. A pure sinewave is applied to the CSZ5116, and a "time record" of 1024 samples is captured and processed. The FFT algorithm analyzes the spectral content of the digital waveform and distributes its energy among 512 "frequency bins." Assuming an ideal sinewave, distribution of energy in bins outside of the fundamental and dc can only be due to quantization effects and errors in the CSZ5116.

If sampling is not synchronized to the input sinewave, it is highly unlikely that the time record will contain an integer number of periods of the input signal. However, the FFT assumes that the signal is periodic, and will calculate the spectrum of a signal that appears to have large discontinuities, thereby yielding a severely distorted spectrum. To avoid this problem, the time record is multiplied by a window function prior to performing the FFT. The window function smoothly forces the endpoints of the time record to zero, thereby removing the discontinuities. The effect of the window in the frequency-domain is to convolute the spectrum of the window with that of the actual input.

The quality of the window used for harmonic analysis is typically judged by its highest side-lobe level. The Blackman-Harris window used for testing the CSZ5116 has a maximum side-lobe level of -92dB. Figure 13 shows an FFT computed from an ideal 16-bit sinewave multiplied by a Blackman-Harris window. Artifacts of windowing are discarded from the signal-to-noise calculation using the assumption that quantization noise is white. All FFT plots in this data sheet were derived by averaging the FFT results from ten time records. This filters the spectral variability that can arise from capturing finite time records without disturbing the total energy outside the fundamental. All harmonics

and the -92dB side-lobes from the Blackman-Harris window are therefore clearly visible in the plots. For more information on FFT's and windowing refer to: F.J. HARRIS, "On the use of windows for harmonic analysis with the Discrete Fourier Transform", Proc. IEEE, Vol. 66, No. 1, Jan 1978, pp.51-83.

Nonlinearity

Analog-to-digital converters have traditionally been specified using dc specifications such as Integral and Differential Nonlinearity at worst-case points on the transfer curve. These specifications are not particularly useful in signal processing applications since they offer little information on the overall shape of converter's transfer curve, and therefore do not directly correlate to the converter's effect on a signal's spectral content.

Integral Nonlinearity (INL; also termed Relative Accuracy or just Nonlinearity) is defined as the deviation of the transfer function from an ideal straight line. Bows and waves in the transfer curve generate harmonic distortion. However, the most prevalent source of nonlinearity in high-resolution converters is bit-weight errors; that is, the deviation of bits from their ideal binary-weighted ratios. At dc, bit-weight errors most visibly affect the converter's Differential Nonlinearity, or the deviation of codes from their ideal widths. Due to the limitations of factory trim techniques, the worst-case condition of bit-weight errors has traditionally also defined the point of maximum INL.

Bit-weight errors have a drastic effect on a converter's ac performance. They can be analyzed as step functions superimposed on the input signal. Since bits (and their errors) switch in and out throughout the transfer curve, their effect is signal dependent. That is, harmonic and intermodulation distortion, as well as noise, can vary with different input conditions. Designing a system around characterization data is risky since transfer curves can differ drastically unit-to-unit and lot-to-lot.

The CSZ5116 achieves repeatable signal-to-noise and harmonic distortion performance using an on-chip self-calibration scheme. The CSZ5116 calibrates its bit weights to ± 1/4 LSB at 16-bits (± 0.0004% FS) yielding peak distortion as low as -105dB (see Figure 14). Unlike traditional ADC's, the linearity of the CSZ5116 is not limited by bit-weight errors; its performance is therefore extremely repeatable and independent of input signal conditions.

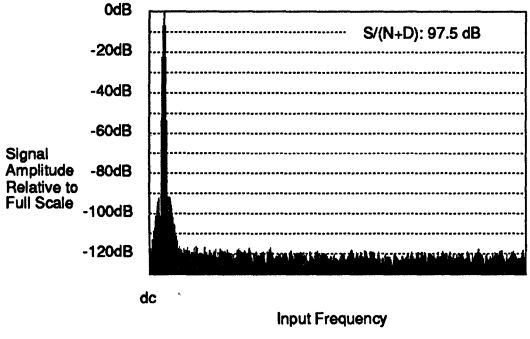


Figure 13. FFT Plot of Ideal 16-bit Signal

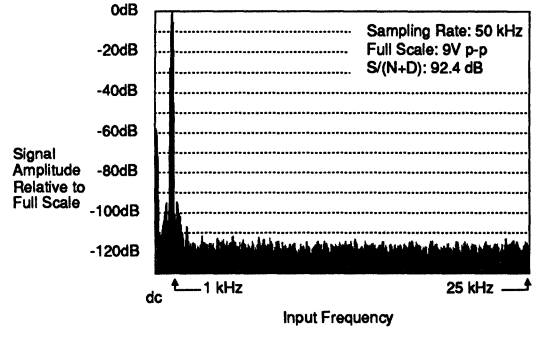


Figure 14. FFT Plot with 1kHz Full-Scale Input

Sampling Distortion

The ultimate limitation on the CSZ5116's linearity (and distortion) arises from nonideal sampling of the analog input voltage. The calibrated capacitor array used during conversions is also used to track and hold the analog input signal. The conversion is not performed on the analog input voltage per se, but is actually performed on the charge trapped on the capacitor array at the moment the $\overline{HOLD}$ command is given. The charge on the array is ideally related to the analog input voltage by $Q_{in} = -V_{in} \times C_{tot}$ as shown in Figure 2. Any deviation from this ideal relationship will result in conversion errors even if the conversion process proceeds flawlessly.

At dc, the DAC capacitor array's voltage coefficient dictates the converter's linearity. This variation in capacitance with respect to applied signal voltage yields a nonlinear relationship between charge Q_{in} and the analog input voltage V_{in} and places a bow or wave in the transfer function. This is the dominant source of distortion at low input frequencies (Figure 14).

The ideal relationship between Q_{in} and V_{in} can also be distorted at high signal frequencies due to nonlinearities in the internal MOS switches. Dynamic signals cause ac current to flow through the switches connecting the capacitor array to the analog input pin in the track mode. Nonlinear on-resistance in the switches causes a nonlinear voltage drop. This effect worsens with increased signal frequency as shown in Figure 15 since the magnitude of the steady state current increases. First noticeable at 1kHz, this distortion assumes a linear relationship with input frequency. With signals 20dB or more below full-scale, it no longer dominates the converter's overall S/(N+D) performance (Figure 16).

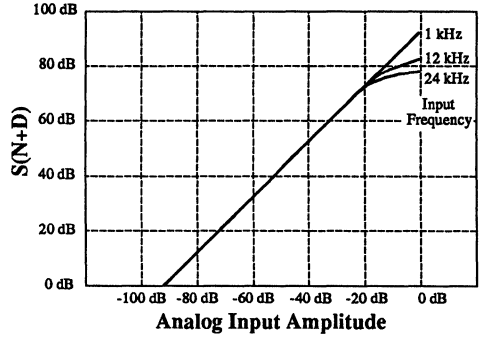
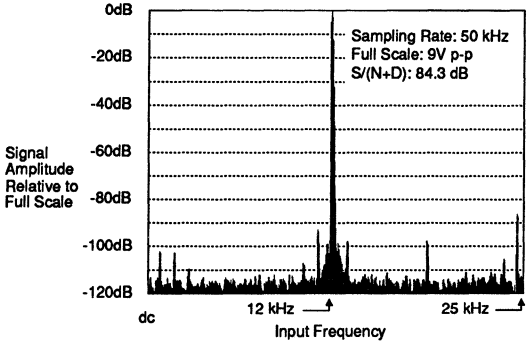


Figure 15. S/(N+D) vs. Input Amplitude (9V p-p Full-Scale Input)



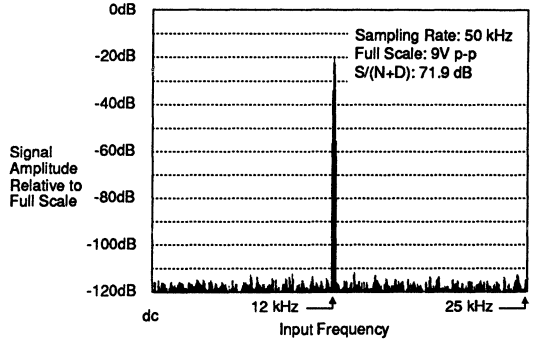


Figure 16. FFT Plots of 12kHz Signals at Full-Scale and 20dB Below Full-Scale

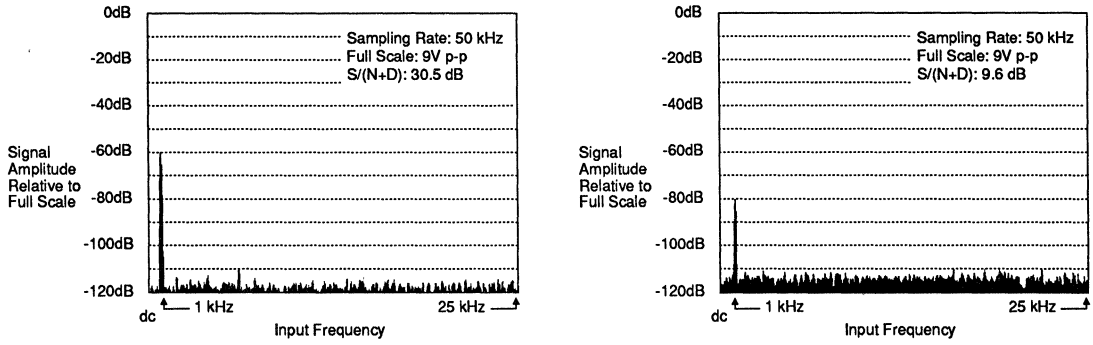


Figure 17. FFT plots of 1kHz Signals 60dB and 80dB Below Full Scale

This distortion is strictly an ac sampling phenomenon. If significant energy exists at high frequencies, the effect can be eliminated using an external track-and-hold amplifier to allow the array's charge current to decay, thereby eliminating any voltage drop accross the switches. Since the CSZ5116 has a second sampling function on-chip, the external track-and-hold can return to the track mode once the converter's $\overline{\text{HOLD}}$ input falls. It need only acquire the analog input by the time the entire conversion cycle finishes.

Quantization Noise

The error due to quantization of the analog input ultimately dictates the accuracy of any A/D converter. The continuous analog input must be represented by one of a finite number of digital codes, so the best accuracy to which an analog input can be known from its digital code is ± 1/2 LSB. Under circumstances commonly encountered in signal processing applications, this quantization error can be treated as a random variable. The magnitude of the error is limited to ± 1/2 LSB, but any value within this range has equal probability of occurance. Such a probability distribution leads to an error "signal" with an rms value of 1 LSB/$\sqrt{12}$. Using an rms signal value of FS/$\sqrt{8}$ (amplitude = FS/2), this relates to an ideal 16-bit signal-to-noise ratio of 98.1dB.

Equally important is the spectral content of this error signal. It can be shown to be approximately white, with its energy spread uniformly over the band from dc to one-half the sampling rate. Advantage of this characteristic can be made by judicious use of filtering. If the signal is bandlimited, much of the quantization error can be filtered out, and improved system performance can be attained.

As illustrated in Figures 15 and 17, the CSZ5116's on-chip self-calibration provides very accurate bit weights which yield no degradation in quantization noise with low-level input signals. In fact, quantization noise remains below the noise floor in the CSZ5116 which dictates the converter's signal-to-noise performance.

Clock Feedthrough

Maintaining the integrity of analog signals in the presence of digital switching noise is a difficult problem. The CSZ5116 can be synchronized to the digital system using the CLKIN input to avoid conversion errors due to asynchronous interference. However, digital interference will still affect sampling purity due to coupling between the CSZ5116's analog input and master clock.

The effect of clock feedthrough depends on the sampling conditions. If the sampling signal at the $\overline{HOLD}$ input is synchronized to the master clock, clock feedthrough will appear as a dc offset at the CSZ5116's output. The offset could theoretically reach the peak coupling magnitude (Figure 18), but the probability of this occurring is small since the peaks are spikes of short duration.

Master Clock		Analog Input	Clock Feedthrough	
Int/Ext	Freq	Source Impedance	RMS	Peak-to-Peak
Internal	2MHz	50 Ω	15uV	70uV
External	2MHz	50 Ω	25uV	110uV
External	4MHz	50 Ω	40uV	150uV
External	4MHz	25 Ω	25uV	110uV
External	4MHz	200Ω	80uV	325uV

Figure 18. Examples of Measured Clock Feedthrough

If sampling is performed asynchronously with the master clock, clock feedthrough will appear as an ac error at the CSZ5116's output. With a fixed sampling rate, a tone will appear as the clock frequency aliases into the baseband. The tone frequency can be calculated using the equation below and could be selectively filtered in software using DSP techniques.

$$f_{tone} = (Nf_s - f_{clk})$$

where $N = f_{clk}/f_s$ rounded to the nearest integer

The magnitude of clock feedthrough depends on the master clock conditions and the source impedance applied to the analog input. When operating with the CSZ5116's internally generated clock, the CLKIN input is grounded and the dominant source of coupling is through the device's substrate. As shown in Figure 18, a typical CSZ5116 operating with its internal oscillator at 2MHz and 50Ω of analog input source impedance will exhibit only 15μV rms of clock feedthrough (-116dB with a 9V p-p full scale). However, if a 2MHz external clock is applied to CLKIN under the same conditions, feedthrough increases to 25μV rms(-111dB). Feedthrough also increases with clock frequency; a 4MHz clock yields 40μV rms (-107dB). Clock feedthrough can be reduced by limiting the source impedance applied at the analog input. As shown in Figure 18, reducing source impedance from 50Ω to 25Ω yields a 15μV rms reduction in feedthrough. Therefore, when operating the CSZ5116 with high-frequency external master clocks, it is important to minimize source impedance applied to the CSZ5116's input.

Also, the overall effect of clock feedthrough can be minimized by maximizing the input range and LSB size. The reference voltage applied to VREF can be maximized, and the CSZ5116 can be operated in bipolar mode which inherently doubles the LSB size over the unipolar mode.

Aperture Jitter

Track-and-hold amplifiers commonly exhibit two types of aperture jitter. The first, more appropriately termed "aperture window", is an input voltage dependent variation in the aperture delay. Its signal-dependancy causes distortion at high frequencies. The CSZ5116's proprietary architecture avoids applying the input voltage across a sampling switch, thus avoiding any "aperture window" effects. The second type of aperture jitter assumes a random nature and appears in an FFT as a spreading in the fundamental. With only 100ps peak-to-peak aperture jitter, the CSZ5116 can process full-scale signals up to 24kHz with 16-bit accuracy.

Power Supply Rejection

The CSZ5116's power supply rejection performance is enhanced by the on-chip self-calibration and an "auto-zero" process. Drifts in power supply voltages at frequencies less than the calibration rate have negligible effect on the CSZ5116's accuracy. This, of course, is because

the CSZ5116 adjusts its offset to within a small fraction of an LSB during calibration. Above the calibration frequency the excellent power supply rejection of the internal amplifiers is augmented by an auto-zero process. Any offsets are stored on the capacitor array and are effectively subtracted once conversion is initiated. Figure 19 shows power supply rejection of the CSZ5116 in the bipolar mode with the analog input grounded and a 300mV p-p ripple applied to each supply. Power supply rejection improves by 6dB in the unipolar mode.

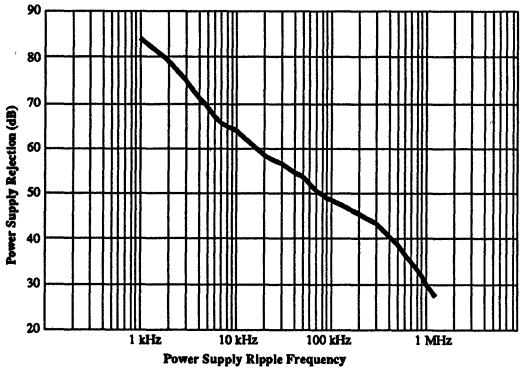


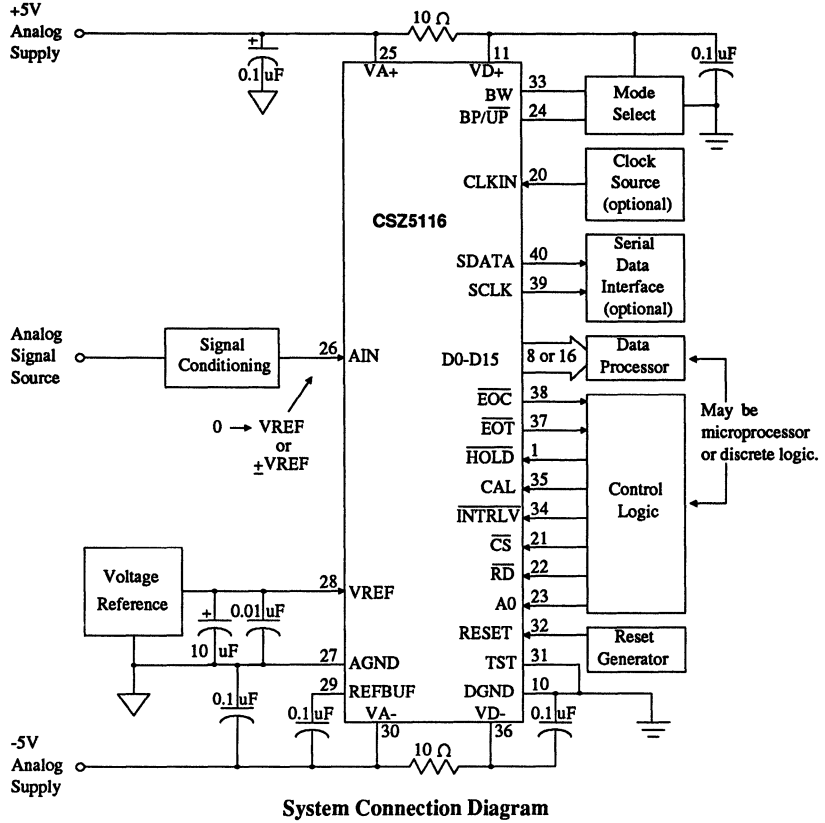
Figure 19. Power Supply Rejection

Notches of increased rejection arise from the auto-zeroing at the conversion rate. The frequencies at which these notches occur also depend on the value of the captured analog input. The line shows worst-case rejection for all combinations of conversion rates and input conditions in the bipolar mode. Again, power supply rejection is 6dB better in the unipolar mode.

$\overline{HOLD}$	$\overline{CS}$	CAL	$\overline{INTRLV}$	$\overline{RD}$	A0	RST	Function
↓	X	X	X	X	*	0	Hold and Start Convert
X	0	1	X	X	*	0	Initiate Burst Calibration
1	0	0	X	X	*	0	Stop Burst Cal and Begin Track
X	0	X	0	X	*	0	Initiate Interleave Calibration
X	0	X	1	X	*	0	Terminate Interleave Cal
X	0	X	X	0	1	0	Read Output Data
1	0	X	X	0	0	0	Read Status Register
X	1	X	X	X	*	X	High Impedance Data Bus
X	X	X	X	1	*	X	High Impedance Data Bus
X	X	X	X	X	X	1	Reset
0	0	X	X	X	0	X	Reset

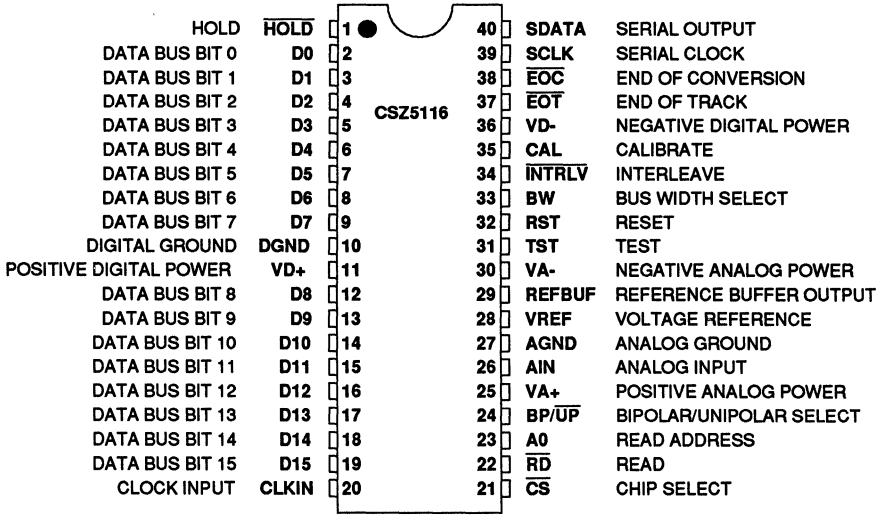
* The status of A0 is not critical to the operation specified. However, A0 should not be low with $\overline{CS}$ and $\overline{HOLD}$ low, or a software reset will result.

CSZ5116 Truth Table



System Connection Diagram

PIN DESCRIPTIONS



Power Supply Connections

VD+ - Positive Digital Power, PIN 11.
Positive digital power supply. Nominally +5 volts.

VD- - Negative Digital Power, PIN 36.
Negative digital power supply. Nominally -5 volts.

DGND - Digital Ground, PIN 10.
Digital ground reference.

VA+ - Positive Analog Power, PIN 25.
Positive analog power supply. Nominally +5 volts.

VA- - Negative Analog Power, PIN 30.
Negative analog power supply. Nominally -5 volts.

AGND - Analog Ground, PIN 27.
Analog ground reference.

Oscillator

CLKIN - Clock Input, PIN 20.
All conversions and calibrations are timed from a master clock which can either be supplied by driving this pin with an external clock signal, or can be internally generated by tying this pin to DGND.

Digital Inputs

$\overline{\text{HOLD}}$ - Hold, PIN 1.
A falling transition on this pin sets the CSZ5116 to the hold state and initiates a conversion. This input must remain low at least one master clock cycle plus 50ns.

$\overline{\text{CS}}$ - Chip Select, PIN 21.
When high, the data bus outputs are held in a high impedance state and the inputs to CAL and $\overline{\text{INTRLV}}$ are ignored. A falling transition initiates or terminates burst or interleave calibration (depending on the status of CAL and $\overline{\text{INTRLV}}$) and a rising transition latches both the CAL and $\overline{\text{INTRLV}}$ inputs. If $\overline{\text{RD}}$ is low, the data bus is driven as indicated by BW and A0.

$\overline{\text{RD}}$ - Read, PIN 22.
When $\overline{\text{RD}}$ and $\overline{\text{CS}}$ are both low, data is driven onto the data bus. If either signal is high, the data bus outputs are held in a high impedance state. The data driven onto the bus is determined by BW and A0.

A0 - Read Address, PIN 23.
Determines whether data or status information is placed onto the data bus. When high during the read operation, converted data is placed onto the data bus; when low, the status register is driven onto the bus.

BP/$\overline{\text{UP}}$ - Bipolar/Unipolar Input Select, PIN 24.
When high, the device is configured with a bipolar transfer function ranging from -VREF to +VREF. Encoding is in an offset binary format, with the mid-scale code 100...0000 centered at AGND. When low, the device is configured for a unipolar transfer function from AGND to VREF.

RST - Reset, PIN 32.

When taken high, all internal digital logic is reset. Upon returing low, a full calibration sequence is initiated.

BW - Bus Width Select, PIN 33.

When high, all 16 data bits are driven onto the bus simultaneously during a data read cycle. When low, the bus is in a byte wide format. On the first read following a conversion, the eight MSB's are driven onto D7-D0. A second read cycle places the eight LSB's on D7-D0. Subsequent reads will toggle the higher/lower order bytes of the same data until the next conversion completes. Regardless of BW's status, a read cycle with A0 low yields the status information on D7-D0.

$\overline{\text{INTRLV}}$ - Interleave, PIN 34.

When latched low using $\overline{\text{CS}}$, the device goes into interleave calibration mode. A full calibration will complete every 72,192 conversions. The effective conversion time extends by 20 clock cycles.

CAL - Calibrate, PIN 35. (See note on page 89.)

When latched high using $\overline{\text{CS}}$, burst calibration results. The device cannot perform conversions during the calibration period which will terminate only once CAL is latched low again. Calibration picks up where the previous calibration left off, and calibration cycles complete every 1,443,840 master clock cycles. If the device is converting when a calibration is signaled, it will wait until that conversion completes before beginning calibration.

Analog Inputs

AIN - Analog Input, PIN 26.

Input range in the unipolar mode is zero volts to VREF. Input range in the bipolar mode is -VREF to +VREF. The output impedance of buffer driving this input should be less than or equal to 200Ω.

VREF - Voltage Reference, PIN 28.

The analog reference voltage which sets the analog input range. It represents positive full scale for both bipolar and unipolar operation, and its magnitude sets negative full scale in bipolar mode.

Digital Outputs

D0 through D15 - Data Bus Outputs, PINS 2 thru 9, 12 thru 19.

Tri-state output pins. Enabled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$, they offer the converter's 16-bit output in a format consistent with the state of BW if A0 is high. If A0 is low, bits D0-D7 offer the status register.

$\overline{EOT}$ - End Of Track, PIN 37.

If low, indicates that enough time has elapsed since the last conversion for the device to acquire the analog input signal (3.75µs for 4MHz external clock).

$\overline{EOC}$ - End Of Conversion, PIN 38.

This output indicates the end of a conversion or reset calibration cycle. It is high during a conversion and will fall to a low state upon completion of the conversion cycle indicating valid data is available at the output. Returns high on the first subsequent read or the start of a new conversion cycle.

SDATA - Serial Output, PIN 40.

Presents each output data bit after it is determined by the successive approximation algorithm. Valid on the rising edge of SCLK, data appears MSB first, LSB last, and each bit remains valid until the next bit appears.

SCLK - Serial Clock Output, PIN 39.

Used to clock converted output data serially from the CSZ5116. Serial data is stable on the rising edge of SCLK.

Analog Outputs

REFBUF - Reference Buffer Output, PIN 29.

Reference buffer output. A 0.1µF ceramic capacitor must be tied between this pin and VA-.

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Miscellaneous

TST - Test, PIN 31.

Allows access to the CSZ5116's test functions which are reserved for factory use. Must be tied to DGND.

ERROR DEFINITIONS

Peak Harmonic or Spurious Noise (More accurately, Signal to Peak Harmonic or Spurious Noise) - The ratio of the rms value of the signal to the rms value of the next largest spectral component below the Nyquist rate (excepting dc). This component is often an aliased harmonic when the signal frequency is a significant proportion of the sampling rate. Expressed in decibels.

Total Harmonic Distortion - The ratio of the rms sum of all harmonics to the rms value of the signal. Units in percent.

Signal-to-Noise Ratio - The ratio of the rms value of the signal to the rms sum of all other spectral components below the Nyquist rate (excepting dc), including distortion components. Expressed in decibels.

Full Scale Error - The deviation of the last code transition from the ideal (VREF-3/2 LSB's) after all offsets have been externally compensated. Units in LSB's.

Unipolar Offset - The deviation of the first code transition from the ideal (1/2 LSB above AGND) when in unipolar mode (BP/$\overline{UP}$ low). Units in LSB's.

Bipolar Offset - The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below AGND) when in bipolar mode (BP/$\overline{UP}$ high). Units in LSB's.

Bipolar Zero Error - The deviation of the first code transition from the ideal (1/2 LSB above -VREF) when in bipolar mode (BP/$\overline{UP}$ high). Units in LSB's.

Aperture Time - The time required after the hold command for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

Aperture Jitter - The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

Note: Temperatures specified define ambient conditions in free-air during test and do not refer to the junction temperature of the device.

Ordering Guide

Model	Signal to Noise Ratio	Throughput	Temp. Range	Package
CSZ5116-JC32	87 dB	26.5 kHz	0 to 70 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5116-JC16	87 dB	50 kHz	0 to 70 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5116-KC32	90 dB	26.5 kHz	0 to 70 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5116-KC16	90 dB	50 kHz	0 to 70 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5116-LC32	92 dB	26.5 kHz	0 to 70 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5116-LC16	92 dB	50 kHz	0 to 70 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5116-AC32	87 dB	26.5 kHz	-40 to +85 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5116-AC16	87 dB	50 kHz	-40 to +85 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5116-BC32	90 dB	26.5 kHz	-40 to +85 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5116-BC16	90 dB	50 kHz	-40 to +85 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5116-CC32	92 dB	26.5 kHz	-40 to +85 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5116-CC16	92 dB	50 kHz	-40 to +85 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5116-SC16	87 dB	50 kHz	-55 to +125 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5116-TC16	90 dB	50 kHz	-55 to +125 °C	40-Pin Ceramic Side-Brazed DIP
CSZ5116-UC16	92 dB	50 kHz	-55 to +125 °C	40-Pin Ceramic Side-Brazed DIP

ADDENDUM

Burst Calibration

Burst calibration mode allows control of partial calibration cycles. Due to an unforeseen condition inside the part, asynchronous termination of calibration (CAL brought low) may result in a sub-optimal calibration result. It is recommended that burst calibration is not used, until the silicon is revised to prevent this effect.

The reset and interleave mode work perfectly, and should be used instead of burst mode. The CSZ5116's very low drift over temperature means that, under most circumstances, calibration need only be performed at power-up, using reset.

If you wish to use burst calibration, then please contact the factory for advice and new part availability information.

• Notes •

Semiconductor Corporation

CSZ5316

16-Bit, 20 kHz Oversampling A/D Converter

Features

- 16 Bit Resolution / 84 dB Dynamic Range
- Full Scale Signal to Total Harmonic Distortion - 80 dB typ.
- Output Rate - 20 kHz max.
- Internal Track and Hold Amplifier
- On-chip Voltage Reference
- Linear Phase Digital Filter
- DSP Compatible Codec-Like Serial Interface
- Low Power Dissipation: 220 mW typ.

General Description

The CSZ5316 analog to digital converter is a unique, very high resolution A/D converter with excellent AC characteristics for voice-band signal processing applications such as high performance modems and voice recognition systems.

Delta-sigma modulation, a technique which utilizes oversampling followed by a digital decimation process, provides a digital output of 84 dB dynamic range, and 80 dB signal to distortion, for input signals with bandwidths from 0 to 10 kHz.

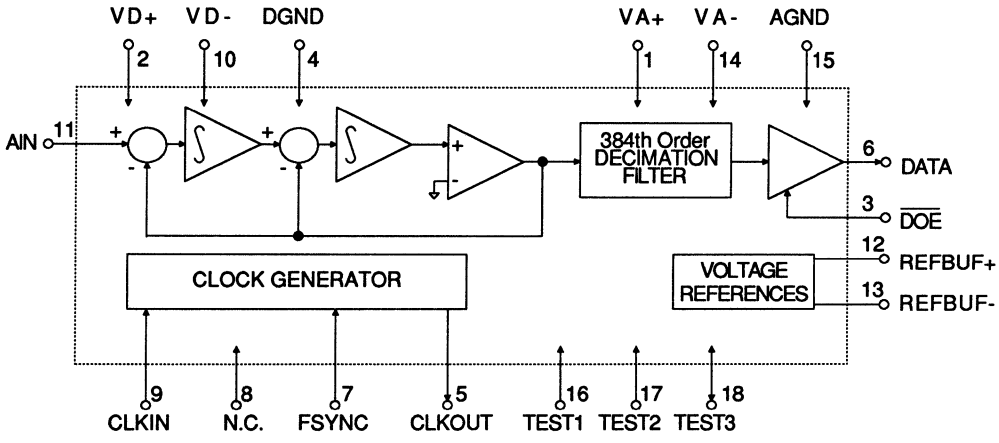
Crystal's 3 micron CMOS process ensures high reliability and power dissipation of less than 250 mW.

Note: This device was formerly designated the CS5316.

ORDERING INFORMATION

CSZ5316-P 18 pin Plastic, 0°C - 70°C.
CSZ5316-ID 18 pin Cerdip, -40°C - 85°C.

Block Diagram



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Crystal Semiconductor Corporation
P.O. Box 17847, Austin, Texas 78760
(512)445-7222 TWX:910-874-1352

ABSOLUTE MAXIMUM RATINGS (DGND, AGND = 0V)

Parameter	Symbol	Min	Max	Units
DC Supply				
Positive Analog	VA+	-	6.0	V
Negative Analog	VA-	-	- 6.0	V
Positive Digital	VD+	-	6.0	V
Negative Digital (Note 1)	VD-	-	- 6.0	V
Input Voltage	V_{in}			
Any Digital Input		DGND - 0.3	VD+ + 0.3	V
AIN		VA- - 0.3	VA+ + 0.3	V
Input Current, Any pin except power supplies (Note 2)	I_{in}	-	10	mA
Ambient Operating Temperature	T_A	-55	125	^{0}C
Storage Temperature	T_{stg}	-65	150	^{0}C

Notes: 1. VD+ must never exceed VA+ by more than +0.3V.
2. The CSZ5316 will tolerate a transient input current of up to 100mA without latching up.

WARNING: Operating this device at or beyond these limits may result in permanent damage to the device. Normal operation of the part is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (DGND, AGND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
DC Supply					
Positive Analog	VA+	4.5	5.0	5.5	V
Negative Analog	VA-	- 4.5	- 5.0	-5.5	V
Positive Digital	VD+	4.5	5.0	5.5	V
Negative Digital	VD-	- 4.5	- 5.0	-5.5	V
Ambient Operating Temp. (Note 3)	T_A	T_{MIN}	25	T_{MAX}	^{0}C
CLKIN Frequency	f_c	0.01	-	5.12	MHz

Note: 3. See *Ordering information* on page 91.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Note 4)

($T_A = T_{MIN}$-T_{MAX}; VA+ = 5V ± 10%; VA- = -5V ± 10%; AGND = 0V; CLKIN = 4.9152MHz)

Parameter	Symbol	Min	Typ	Max	Units
Input Signal Bandwidth	BW	0	-	9.6	kHz
Input Voltage Range	V_{in}	-2.75	-	+2.75	V_{p-p}
Dynamic Range (1kHz Input) (Note 5)	DR	78	84	-	dB
Signal-to-Distortion (1kHz) (Note 6)	SDR	72	80	-	dB
Power Dissipation	P_D	-	220	250	mW
AC Input Impedance (1kHz)	Z_{in}	-	30	-	kohms
Absolute Group Delay (Note 7)	D_G	78.125	-	-	us
Power Supply Rejection (1kHz)	PSR				
VA+		-	35	-	dB
VA-		-	55	-	dB
VD+		-	60	-	dB
VD- (Note 8)		-	55	-	dB

Notes:
4. Analog characteristics are measured at 4.9152MHz CLKIN, corresponding to an output rate of 19.2kHz. The device is guaranteed to function up to 5.12MHz CLKIN, corresponding to 20kHz output, and will typically function, with some degradation in performance, to beyond 6MHz CLKIN (see graph of typical dynamic range vs. frequency on page 98).
5. Full scale signal to noise plus distortion measured with input 20dB below full scale (RMS measurements).
6. Full scale signal to harmonic distortion measured with input at full scale (RMS measurements).
7. Group delay is constant with respect to analog input frequency, and is determined by the formula D_G = 384/CLKIN.
8. Power supply rejection increases above 4kHz due to the effect of the on-chip FIR filter.

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DIGITAL CHARACTERISTICS ($T_A = T_{MIN}$-T_{MAX}; VD+ = 5V ± 10%; VD- = -5V ± 10%; DGND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage All Except CLKIN (Note 9)	V_{IH}	2.0	-	-	V
High-Level Input Voltage CLKIN (Note 9)	V_{IH}	3.5	-	-	V
Low-Level Input Voltage All Except CLKIN (Note 9)	V_{IL}	-	-	0.8	V
Low-Level Input Voltage CLKIN (Note 9)	V_{IL}	-	-	1.5	V
High-Level Output Voltage (Note 10)	V_{OH}	VD+ -1.0V	-	-	V
Low-Level Output Voltage I_{out} = 1.6 mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{LKG}	-	-	10	uA
Tri-State Leakage Current	I_{OZ}	-	-	10	uA

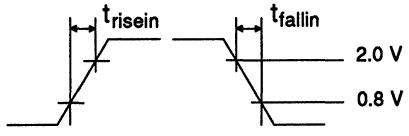
Notes:
9. Input current = 0.5µA.
10. I_{out} = -100µA. This specification guarantees TTL compatibility. (V_{OH} = 2.4V @ I_{out} = -40µA)

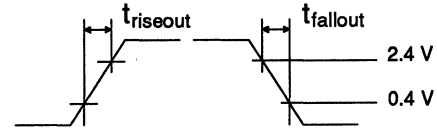
SWITCHING CHARACTERISTICS

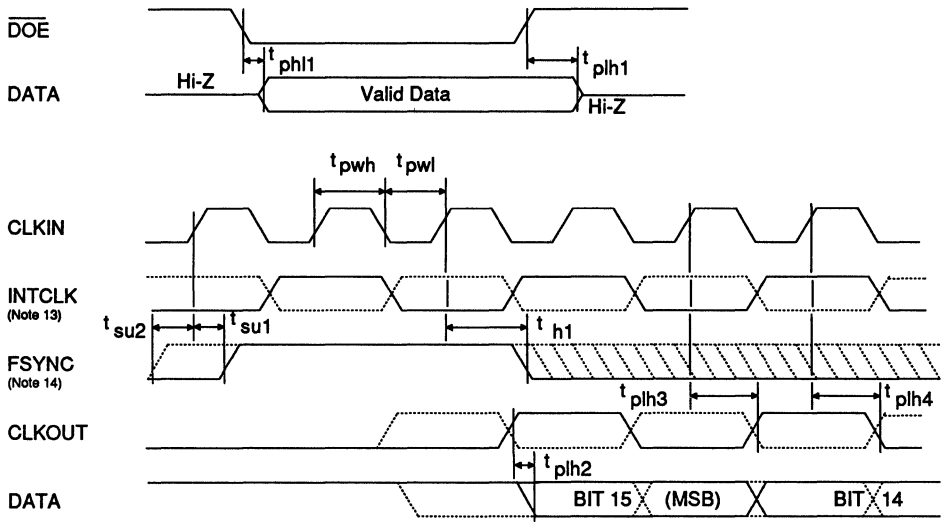
($T_A = T_{MIN}$-T_{MAX}; C_L = 50pF; VD+ = 5V ± 10%; VD- = -5V ± 10%; DGND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
Output Rise Time (Note 11)	$t_{riseout}$	-	15	20	ns
Output Fall Time (Note 11)	$t_{fallout}$	-	15	20	ns
Input Rise Time	t_{risein}	-	20	1000	ns
Input Fall Time	t_{fallin}	-	20	1000	ns
CLKIN Frequency(256 t_{sync}) (Note 4)	f_{clk}	-	-	5.12	MHz
FSYNC Period(256/f_{clk})	t_{sync}	50	-	-	us
Setup Times					
CLKIN Rising to FSYNC Rising	t_{su1}	-	-	35	ns
FSYNC Rising to CLKIN Rising	t_{su2}	-	-	50	ns
Hold Times					
CLKIN Rising to FSYNC Falling	t_{h1}	0	-	-	ns
CLKIN Pulse Width (Note 12)	t_{pwh}	40	-	-	ns
	t_{pwl}	40	-	-	ns
Propagation Delays					
DOE Falling to Data Valid	t_{phl1}	-	30	-	ns
DOE Rising to Hi-Z	t_{plh1}	-	30	-	ns
CLKOUT Rising to Data Valid	t_{plh2}	-	-	75	ns
CLKIN Rising to CLKOUT Rising	t_{plh3}	-	-	200	ns
CLKIN Rising to CLKOUT Falling	t_{plh4}	-	-	200	ns

Note: 11. 50pF load (includes probe and jig capacitance)
12. $t_{pwh} + t_{pwl} = 1/f_{clk}$







Notes: 13. INTCLK is an internal free-running clock derived by dividing CLKIN by 2. Its phase is not known by the user and may follow either the solid or the dotted line. When the phase is the same as the dotted line, CLKOUT and DATA will also behave as shown by the dotted lines.

14. FSYNC is recognized on the falling edge of INTCLK. To guarantee FSYNC is recognized, it should be generated on the rising edge of CLKIN and must settle within 35ns. It should then remain active two CLKIN cycles as shown in the above diagram.

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SYSTEM DESIGN WITH THE CSZ5316

Overview

The CSZ5316 functions as a complete data conversion subsystem for a voice-band signal processing system. The voltage reference, sample & hold, and much of the anti-aliasing filter required for most applications are all implemented on chip. The chip has low power dissipation at about 220 mW typical, and has excellent power supply rejection, making it less sensitive to board layout and power supply characteristics than other A/D converters of comparable specifications. A general system connection diagram is shown in Figure 1.

Power Supplies

Although the CSZ5316 requires less attention to grounding and layout arrangements than other 16-bit A/D converters, care should still be taken. Independent analog and digital power supply pins are intended to isolate digital noise from the analog circuitry. The analog supplies, VA+ (pin 1) and VA- (pin 14), should be decoupled with respect to analog ground, AGND (pin 15). The digital supplies, VD+ (pin 2) and VD- (pin 10) should be decoupled with respect to digital ground, DGND (pin 4). Decoupling should be accomplished with 0.1 µF ceramic capacitors under all circumstances. If significant low frequency noise is present in the supplies,

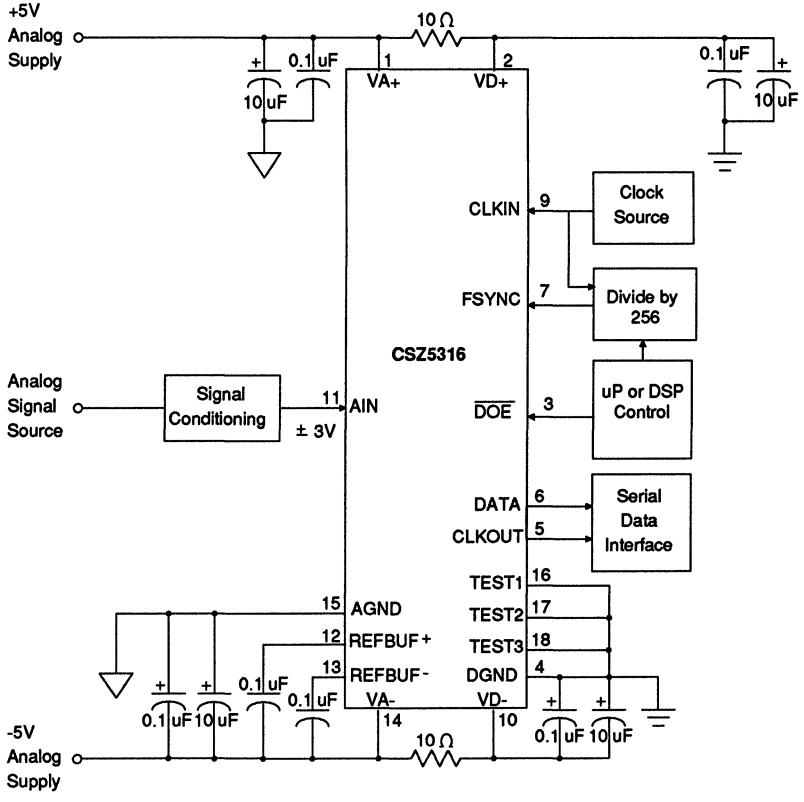


Figure 1. System Connection Diagram

10 µF tantalum capacitors are recommended in parallel with the 0.1 µF capacitors.

The positive digital power supply of the CSZ5316 must never exceed the positive analog supply by more than a diode drop or the chip could be permanently damaged. If the two supplies are derived separately, the analog supply must come up first at power-up. Figure 1 shows a decoupling scheme which allows the CSZ5316 to be powered from a single set of ± 5V rails. The positive digital supply is derived from the analog supply through a 10 Ω resistor to prevent the analog supply from dropping below the digital supply.

Digital Design Considerations

Clocking

Two clocks should be supplied to the CSZ5316, the 5.12 MHz (max) 50% duty cycle master clock, input to CLKIN, and the frame synchronization clock, input to FSYNC (pin 7). The frame synchronization clock rate is the master clock rate divided by 256. The FSYNC input must be clocked synchronously with the master clock and should be derived from the master clock. An asynchronous FSYNC pulse will reset the digital filter and conversion errors will result.

The output rate may be set as needed by adjusting the master clock. If the output rate of the CSZ5316 must be varied to phase lock to some arbitrary signal, the period of the master clock may safely be varied to accomplish this as long as it is always kept greater than 150 ns. As the CLKIN period is reduced below 200 ns, signal to noise plus distortion performance will degrade smoothly to a typical level of about 70 dB at a constant 6.66 MHz CLKIN (150 ns periods).

The master clock is divided by two on-chip to generate an internal clock (INTCLK) used for sampling and digital timing. The timing diagram on page 95 shows the relationship of this internal clock, INTCLK, with CLKIN and FSYNC. FSYNC is sampled on the falling edge of INTCLK and must be stable at that time. Since the phase of INTCLK is not known to the user, FSYNC should be generated on CLKIN rising edges, settle within 35 ns, and be at least two CLKIN periods in length. The internal logic will only react to FSYNC transitions from low to high, so the maximum length of the pulse is governed by the requirement that FSYNC be low for one INTCLK falling edge before it returns high signalling a new frame.

Data Output Characteristics & Coding Format

As shown in figure 2, the CSZ5316 outputs a sixteen bit data word in a serial burst at the INTCLK rate (the master clock rate divided by two). The data is output on DATA (pin 6) on the first rising edge of INTCLK after FSYNC has been recognized as going high. The data is then output on 16 consecutive INTCLK rising edges. CLKOUT (pin 5) is a gated version of INTCLK that is active while data is being output. Data will be stable on the falling edge of CLKOUT.

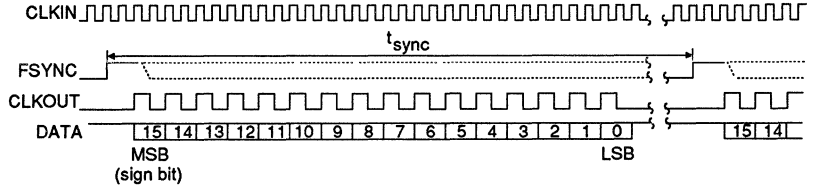


Figure 2. Data Output

After sixteen CLKOUT pulses, DATA will go high, and CLKOUT will go low, until the next FSYNC rising edge.

Data read from the CSZ5316 is a two's complement digital representation of the analog input. The most significant bit (MSB), which is the sign bit, is output first in the serial data stream. Bits are output in descending order to the least significant bit (LSB).

A tri-state option, data output enable, $\overline{DOE}$ (pin 3), is available for bus oriented applications. However, it is asynchronous with respect to the rest of the CSZ5316. If $\overline{DOE}$ goes high during a data burst, DATA goes to a high impedance state. Any data output while $\overline{DOE}$ is high is lost.

Analog Design Considerations

DC Characteristics

The CSZ5316 is intended for signal acquisition, or AC applications. Its absolute offset and gain characteristics are not specified and will vary with temperature. If the CSZ5316 is used in an application where DC measurement is important, a system level calibration scheme to adjust for gain and offset errors is recommended.

The Analog Input Range

The input range of the CSZ5316 is ± 2.75 volts. Internal voltage references set the analog input full-scale to the ± 2.75V limit. Note that differences in ground potential between the analog input common and AGND will appear as a signal added at the input of the device.

Dynamic Range

Processing the output of the CSZ5316 with a digital lowpass filter serves to increase the dynamic range of the unfiltered portion of the input bandwidth by eliminating the noise energy contributed by the filtered portion of the original input bandwidth. The unfiltered portion of the original input bandwidth can then be described with fewer output samples, according to the Nyquist criterion. For example, if the input bandwidth is cut in half with the digital lowpass filter, the unfiltered portion can now be described by dropping every other output sample, a process known as decimation.

Input Bandwidth			Dynamic Range	
Min	Max	Units	Typical	Units
0	5	kHz	88	dB
0	2.5	kHz	90	dB

Table 1. Dynamic Range with Additional Digital Filtering

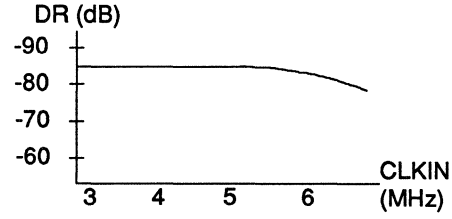


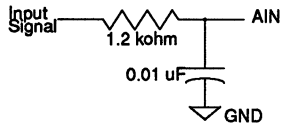
Figure 3. Typical Dynamic Range vs. CLKIN Frequency at 1 kHz Input

Antialiasing Considerations

The two sources of potential aliasing in the CSZ5316 are the initial sampling of the analog input and the digital decimation process.

Initial Sampling

The analog input, AIN, is sampled at the INTCLK rate (1/2 CLKIN) by an on-chip track and hold amplifier. Input frequencies above 1/2 INTCLK (the Nyquist frequency) will alias, or wrap, around 1/2 INTCLK such that input



Note: Distortion due to this filter will be coded as distortion by the CSZ5316. Therefore a low distortion high frequency capacitor such as NPO-ceramic is recommended.

Figure 4. Antialiasing Filter

frequencies in the region of INTCLK will appear as noise in the band of interest. If signals in this region are expected, a simple single-pole low-pass antialiasing filter can be used as shown in Figure 4. This filter ensures that any noise generated by aliasing around 1/2 INTCLK (at 1.28 MHz) is attenuated by at least 40 dB. Use of other CLKIN rates may require that the cutoff frequency of the filter shown be adjusted.

Decimation

The output of the first stage of the CSZ5316, the delta-sigma modulator, is fed into an on-chip low-pass digital filter which has the frequency response defined in Figure 5. The output of the filter is then decimated such that the sampling rate is reduced from the INTCLK rate to F = INTCLK/128. This means that the output of the digital filter is effectively resampled at rate F, which has aliasing implications. Signals at multiples of F will alias into the baseband (wrap around multiples of F/2) after being attenuated according to the filter response defined in Figure 5. For example, if F = 20 kHz (INTCLK = 2.56 MHz), an input tone at 28 kHz will be attenuated by 39.9 dB and will appear at 8 kHz in the output spectrum.

Antialiasing to compensate for the effect of sample rate reduction, or decimation, in the CSZ5316 will depend upon the input bandwidth desired.

0 -F/4 Input Bandwidth

If the band of interest is from 0 to F/4, an off-chip low-pass filter and decimation step to reduce the output rate to F/2 and reject the band greater than F/4 is recommended. This increases the dynamic range of the CSZ5316 and eases the antialiasing task. Signals from 3F/4 to F will alias into the 0 to F/4 band but will be attenuated

$$20 \log \left| \left(\frac{\sin (N \pi f T)}{N \sin (\pi f T)} \right)^3 \right| = \text{Magnitude (dB)}$$

Where $T = 1/f_s = 2/f_{clk}$
N=128
f_s = input sampling frequency
f = input frequency
$F = f_s/128$ =output data rate

EXAMPLES:
for f_s = 2.56 MHz
at f = 5 kHz Magnitude is -2.74 dB
at f = 10 kHz Magnitude is -11.8 dB

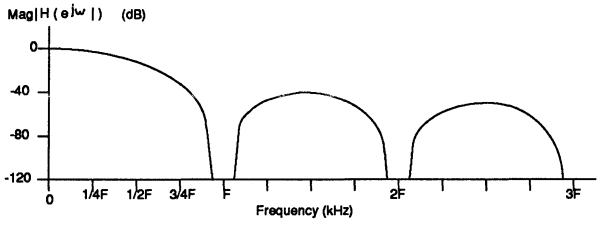


Figure 5. Low-Pass Filter Response

at least 31.4 dB by the on-chip filter. Aliased signals can be attenuated further by an analog antialiasing filter preceding the CSZ5316.

The F/2 data rate, needed to describe the 0 to F/4 input band, can also be obtained by simply dropping every other output of the CSZ5316. If this is done, input signals will now alias around multiples of F/4 (including the band from F/4 to F/2 which is minimally attenuated by the on-chip filter), and a more complex analog antialiasing filter is required. The analog filter's response will still be added to the response of the on-chip FIR filter however, so the analog filter's complexity will be slightly less than that required for a traditional A/D converter.

0 -F/2 Input Bandwidth

If the band from F/4 to F/2 is also of interest, an analog antialiasing filter must be used. The filter complexity required will be similar to the case where output samples are dropped to obtain the F/2 output rate described above. Also, the attenuation of input signals in this band by the on-chip digital filter must be taken into account (see Figure 5).

See Application Note "*Antialiasing Considerations for the CSZ5316*" for a more detailed discussion.

CSZ5316 PERFORMANCE

The CSZ5316 features 100% tested dynamic performance. The following section is included to illustrate the test method used for the CSZ5316, the CSZ5316's error sources, and their effect on a signal's spectral content.

FFT Tests and Windowing

The CSZ5316 is tested using Fast Fourier Transform (FFT) techniques to analyze the converter's dynamic performance. A pure sine wave is applied to the CSZ5316 and a "time record" of 1024 samples is captured and processed. The FFT algorithm analyzes the spectral content of the digital waveform and distributes its energy among 512 "frequency bins". Assuming an ideal sinewave, distribution of energy in bins outside of the fundamental and DC can only be due to quantization effects and errors in the CSZ5316.

If sampling is not synchronized to the input sinewave it is highly unlikely that the time record will contain an exact integer number of periods of the input signal. However, the FFT assumes that the signal is periodic, and will calculate the spectrum of a signal that appears to have large discontinuities, thereby yielding a severely distorted spectrum. To avoid this problem, the time record is multiplied by a

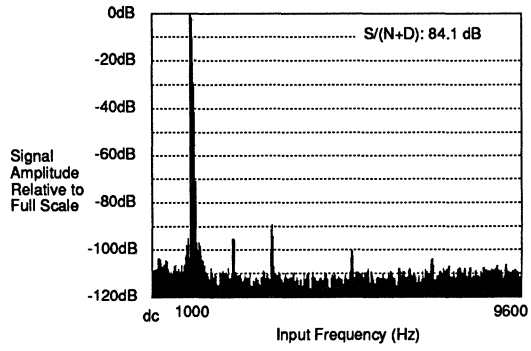


Figure 6. CSZ5316 Dynamic Performance

window function prior to performing the FFT. The window function smoothly forces the endpoints of the time record to zero, removing the discontinuities. The effect of the "window" in the frequency domain is to convolute the spectrum of the window with that of the actual input.

The quality of the window used for harmonic analysis is typically judged by its highest side-lobe level. The Blackman-Harris window used to test the CSZ5316 has a maximum side-lobe level of -92 dB.

Figure 6 shows an FFT plot of a typical CSZ5316 with a 1 KHz sinewave input generated by an "ultra-pure" sine wave generator and the output multiplied by a Blackman-Harris window. Artifacts of windowing are discarded from the signal-to-noise calculation using the assumption that quantization noise is white. All FFT plots in this data sheet were derived by averaging the FFT results from ten time records. This filters the spectral variability that can arise from capturing finite time records, without disturbing the total energy outside the fundamental. All harmonics and the -92 dB side-lobes from the Blackman-Harris window are therefore clearly visible in the plots.

Full - scale - signal - to - noise - plus - distortion [S/(N+D)] is calculated as the ratio of the RMS power of the fundamental to the sum of the RMS power of the FFT's other frequency bins, which include both noise and distortion. Full-scale-signal-to-noise is calculated in the same way but excludes frequency bins where harmonics are expected. In this case, signal-to-noise-plus-distortion is shown to be better than 84 dB for an input frequency range of 0 to 9.6 kHz (fs/2).

The graph in Figure 7 is also derived from measurements taken of a CSZ5316 and shows the linear relationship between input signal level and signal-to-noise-plus-distortion. The dotted line beginning at a signal level of about -40 dB indicates the range of performance variation that can be expected from CSZ5316's at low input signal levels. Any input signal greater than -40 dB, regardless of frequency, will keep the S/(N+D) performance relative to the signal of interest on the solid line. However, if no input signal greater than -40 dB is present, the performance of a CSZ5316 may vary to the limit indicated by the dotted line.

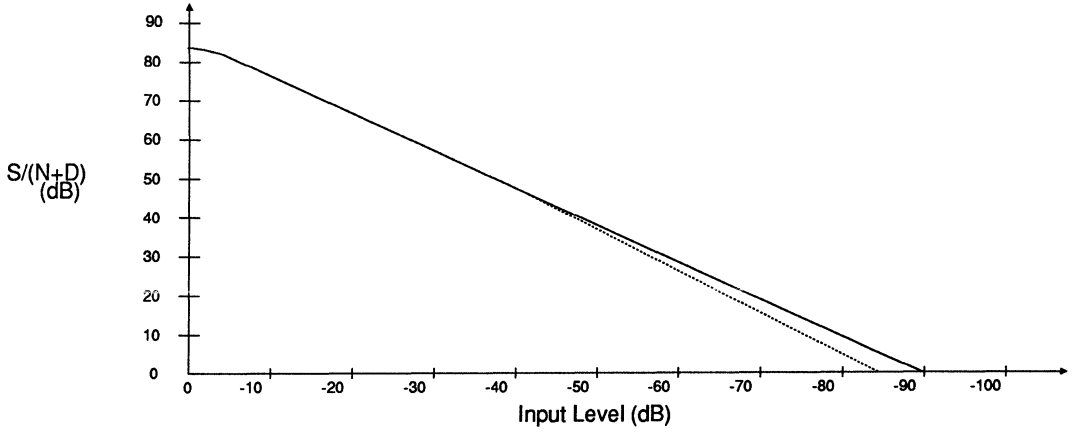


Figure 7. Typical Signal to Noise plus Distortion vs. Input Signal Level

Error Sources in the CSZ5316

Noise

The noise floor of an ideal 16 bit A/D converter is -98.08 dB, determined by the formula 6.02N+1.76, where N is the number of bits of the converter's resolution. This noise, called quantization noise, is a consequence of errors generated by digitizing any continuous time signal. Each A/D conversion approximates an analog value with a digital value, and the difference between the analog input and the digital approximation is the quantization error. Quantization noise is typically assumed to be white, spread evenly between DC and the input sampling frequency.

If the integrated noise of an A/D converter is any higher than -98.08 dB, other noise sources are present in the device. In the case of the CSZ5316 (typical noise floor -84 dB for 0-F/2 bandwidth and -90 dB for 0-F/4) the additional noise comes mainly from "1/f" noise sources, and aliasing of quantization noise.

"1/f" noise is so named because the noise energy is roughly inversely proportional to the noise frequency. 1/f noise is caused by "surface effects" on the chip and it varies with the semiconductor process.

Aliasing of quantization noise from higher frequency bands occurs due to the effect of the decimation filter (as described in *Antialiasing Considerations*). Aliasing of quantization noise accounts for much of the additional noise of the CSZ5316. In contrast, the contribution of thermal noise to the noise floor of the CSZ5316 is negligible due to the effect of the same on-chip decimation filter.

Distortion

The primary cause of harmonic distortion in the CSZ5316 is a phenomenon called charge injection. Charge injection is a consequence of non-ideal switches being used to switch charge between capacitors on the chip, and is a non-linear function of the voltage involved, in this case, the analog input voltage. Charge injection results in some minor linearity errors in the CSZ5316, which translates into harmonic distortion in the frequency domain.

Harmonic distortion characteristics of the CSZ5316 are excellent at 80 dB full scale signal to THD (typical), as are intermodulation distortion characteristics, shown in Figure 8. Intermodulation distortion results from the modulation of two or more input frequencies by a non-linear transfer function.

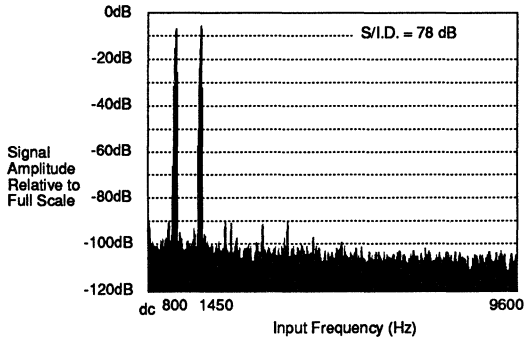
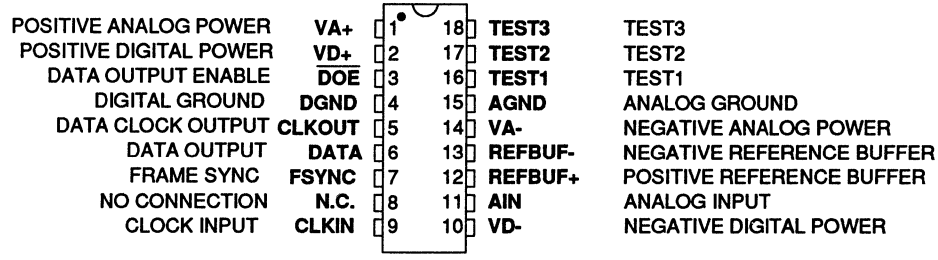


Figure 8. Intermodulation Distortion

PIN DESCRIPTIONS



Power Supplies

VD+ - Positive Digital Power, PIN 2.
Positive digital supply voltage. 5 volts typical.

VD- - Negative Digital Power, PIN 10.
Negative digital supply voltage. -5 volts typical.

DGND - Digital Ground, PIN 4.
Digital ground reference. 0 volts typical.

VA+ - Positive Analog Power, PIN 1.
Positive analog supply voltage. 5 volts typical.

VA- - Negative Analog Power, PIN 14.
Negative analog supply voltage. -5 volts typical.

AGND - Analog Ground, PIN 15.
Analog ground reference. 0 volts typical.

Oscillator

CLKIN - Clock Input, PIN 9.
Master clock input. CMOS compatible input, for a 5.12 MHz (maximum) clock generated externally.

N.C. - No Connection, PIN 8.
This pin is not bonded to the chip and must be left floating.

Inputs

AIN - Analog Input, PIN 11.
Analog input for the signal to be converted.

FSYNC - Frame Sync, Pin 7.
Frame synchronization pulse input. A pulse with frequency CLKIN/256 is applied to this pin to start data output and synchronize internal circuitry.

$\overline{\text{DOE}}$ - Data Output Enable, PIN 3.
Three-state control for DATA. When low, DATA is active and when high, DATA is in a high impedance state.

TEST1; TEST2; TEST3 - Test Inputs, PINS 16; 17; 18.
For factory use. Tied to digital ground during operation.

Outputs

DATA - Data Output, PIN 6.
Serial data output pin. Converted data is clocked out on this pin by CLKOUT.

CLKOUT - Data Output Clock, PIN 5.
Data output clock. See the section on Data Output Characteristics (p. 97) for a complete explanation.

REFBUF+ - Positive Voltage Reference Noise Buffer, PIN 12.
Pin used to attenuate noise on the internal positive voltage reference. Should be connected to the analog ground through a 0.1 µF ceramic capacitor.

REFBUF- - Negative Voltage Reference Noise Buffer, PIN 13.
Pin used to attenuate noise on the internal negative voltage reference. Should be connected to the analog ground through a 0.1 µF ceramic capacitor.

APPENDIX

THEORY OF OPERATION

The CSZ5316 is an "oversampling" A/D converter making use of a "delta-sigma" modulation loop followed by a finite impulse response (FIR) digital filter. Oversampling refers to the fact that the analog input is sampled at a rate far greater than twice the highest frequency of interest as required by the Nyquist theorem. The A/D conversion actually takes place in the modulation loop while the filter is used both to convert the modulation loop output to a DSP compatible format and to filter frequencies higher than the band of interest.

The fundamental principle behind delta-sigma conversion is that of a rough single bit A/D converter embedded in an analog negative feedback loop with high open loop gain.

The Voltage-Follower Analogy

A comparison can be made with the simple voltage-follower op amp circuit shown in Figure A1. Output stage noise sources are represented by e_n. At low frequencies, e_n has little effect on the analog output. The two differential amplifier input devices dominate the noise. The linearity of the amplifier is excellent as long as the open loop gain is high.

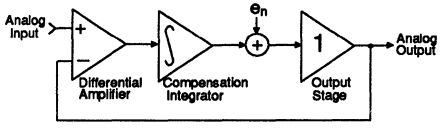


Figure A1. Op amp Voltage-Follower

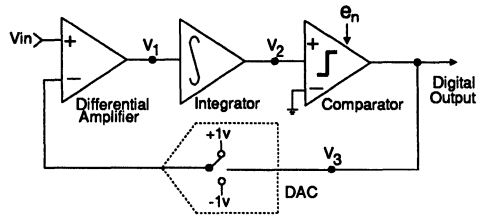


Figure A2. Delta-Sigma Modulation Loop

In the case of the delta-sigma modulation loop shown in Figure A2, the ADC-DAC combination creates a unity gain signal path much like the op amp output stage of Figure A1. Here, e_n is dominated by the random errors of quantization, or quantization noise.

The high performance of the CSZ5316 can be understood by analogy to the voltage-follower circuit. First, the quantization noise of the comparator is white, spread uniformly in frequency between DC and the high sampling rate. Second, at low frequencies, the gain from e_n to the digital output is very low. As a result, because of the high frequency oversampling process, when the modulator output is processed by a digital lowpass filter, a high resolution, low noise representation of the low frequency input signal is obtained. This lowpass filter function, as well as decimation of the high speed (input sampling rate) output to a rate 256 times lower, is accomplished by the 384th order FIR filter on the CSZ5316.

Because the ADC on the CSZ5316 is a comparator and the DAC has only two output levels, plus and minus full scale, both blocks are inherently linear. Overall modulator linearity is limited only by imperfections in the sample & hold and analog gain stage, or integrator.

7

Modulation-Loop Walk Through

The delta-sigma A/D converter can be understood more intuitively by demonstration. A simple first order delta-sigma modulation loop is shown in figure A2. Full scale input is ± 1V and nodes are labeled V_1, V_2, and V_3 representing the outputs of the differential amplifier, the switched-capacitor integrator, and the comparator respectively. The output of the comparator, node V_3, is the output of the loop (input to the digital decimation filter) and will be converted into plus or minus full scale (+1 or -1) by the DAC. At the differential amplifier, the 1 or -1 is subtracted from the analog input voltage and the result, the voltage at node V_1, is input to the switched-capacitor integrator. The switched-capacitor integrator acts as an analog accumulator; ie. the input voltage, at node V_1, is added to the voltage on node V_2 and the sum of the two becomes the new voltage on node V_2. Node V_2 is then compared to ground and generates a 1 on node V_3 if greater than ground and a -1 if less. This completes the loop. Each operation occurs once during each clock cycle.

An example is shown in Table A. If all of the nodes are initially set to 0 and the analog input voltage is set to .6V, the state of each node for 8 clock cycles is shown in the table. Since the voltages on each node in clock cycle 2 and clock cycle 7 are identical, the period defined by clock cycles 2 through 6 will repeat if the analog input remains unchanged. Therefore, the average value of node V_3 for that period, .6, reflects the average value of any large number of node V_3 values. In other words, the average value of a number of the single bit modulation loop outputs is a numerical representation of the value of the analog input.

As pointed out in the initial discussion, this process is only valid for low frequency inputs. For a given sampling frequency, the accuracy achievable degrades as the input frequency increases. In the case of the CSZ5316, a 384th order FIR digital filter is used both to decimate (reduce the sampling rate of) the output of the modulation loop to sixteen bit words at 20 kHz max output rate and to filter out higher frequency components of the input.

This example is a simplification of the actual process taking place in the CSZ5316. The simple averaging step shown does not extract any information from the sequence of the pattern, while the weighted averaging process actually used on the chip extracts that information, resulting in a

Clock Period	V_1 Diff. Amp. Out	V_2 Integrator Out	V_3 Comparator/DAC Out	Period Average
0	0	0	0	
1	.6	.6	1	
2	-.4	.2	1	
3	-.4	-.2	-1	
4	1.6	1.4	1 Period	.6
5	-.4	1.0	1	
6	-.4	.6	1	
7	-.4	.2	1	
8	-.4	-.2	-1	

Table A.

sharper frequency response for the FIR filter. Also, the CSZ5316 actually makes use of a second order delta-sigma modulation loop, rather than a first order loop. This serves to increase the gain in the loop and, in turn, increases the dynamic range of the device. In fact, for a given input frequency band, a second order delta-sigma modulation loop will realize a 15 dB improvement in dynamic range every time the sampling rate is doubled, while a first order loop realizes only a 9 dB improvement. A first order version of the CSZ5316 could achieve only ~72 dB of dynamic range compared to ~90 dB for the CSZ5316, for the nominal 0-5 kHz input range.

The CSZ5316's maximum output rate of 20 kHz, twice the 10 kHz Nyquist rate of the nominal input bandwidth (0-5 kHz), was implemented to give the user the option of doubling the input bandwidth (0-10 kHz) keeping in mind the attenuation effects of the digital filter in the 5-10 kHz region. Several system design options are available, depending upon input bandwidth requirements, as described in this data sheet in the section on antialiasing considerations.

• Notes •

Semiconductor Corporation

CSZ5317

16-Bit, 20kHz Oversampling A/D Converter

Features

- Complete Voiceband DSP Front-End
  - 16-Bit A/D Converter
  - Internal Track/Hold Amplifier
  - On-chip Voltage Reference
  - Linear-Phase Digital Filter
- On-Chip PLL for Simplified Output Phase Locking in Modem Applications
- 84dB Dynamic Range
- 80dB Total Harmonic Distortion
- Output Word Rates up to 20kHz
- DSP-Compatible Serial Interface
- Low Power Dissipation: 280mW

General Description

The CSZ5317 is an ideal analog front-end for voiceband signal processing applications such as high-performance modems, passive sonar, and voice recognition systems. It includes a 16-bit A/D converter with internal track/hold amplifier, a voltage reference, and a linear-phase digital filter.

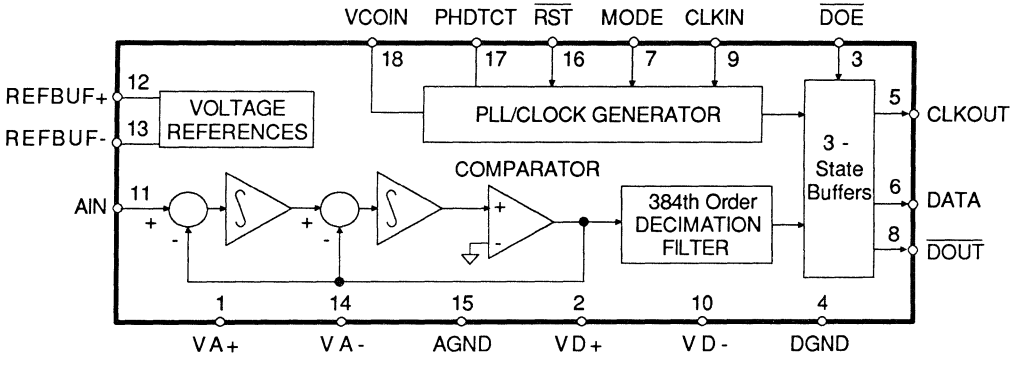
An on-chip phase-lock loop (PLL) circuit simplifies the CSZ5317's use in applications where the output word rate must be locked to an external sampling signal.

The CSZ5317 uses delta-sigma modulation to achieve 16-bit output word rates up to 20kHz. The delta-sigma technique utilizes oversampling followed by a digital filtering and decimation process. The combination of oversampling and digital filtering greatly eases anti-alias requirements. Thus, the CSZ5317 offers 84dB dynamic range and 80dB THD for signal bandwidths up to 10kHz at a fraction of the cost of hybrid and discrete solutions.

The CSZ5317's advanced CMOS construction provides low power consumption of 280mW and the inherent reliability of monolithic devices.

7

Block Diagram



Product Preview

This document contains data for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

SEP '87
DS27PP.1

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, Texas 78760
(512)445-7222 TWX:910-874-1352

• Notes •

Semiconductor Corporation

CSZ5412

12-Bit, 1MHz Self-Calibrating A/D Converter

Features

- Monolithic CMOS Sampling ADC
  On-Chip Track and Hold Amplifier
  Microprocessor Interface
- Throughput Rates up to 1MHz
- True 12-Bit Accuracy over Temperature
  Maximum Nonlinearity: 1/2 LSB
  No Missing Codes to 12 Bits
- Total Harmonic Distortion: 0.02%
- Dynamic Range: 72dB
- Self-Calibration Maintains Accuracy over Time and Temperature
- Low Power Dissipation: 700mW

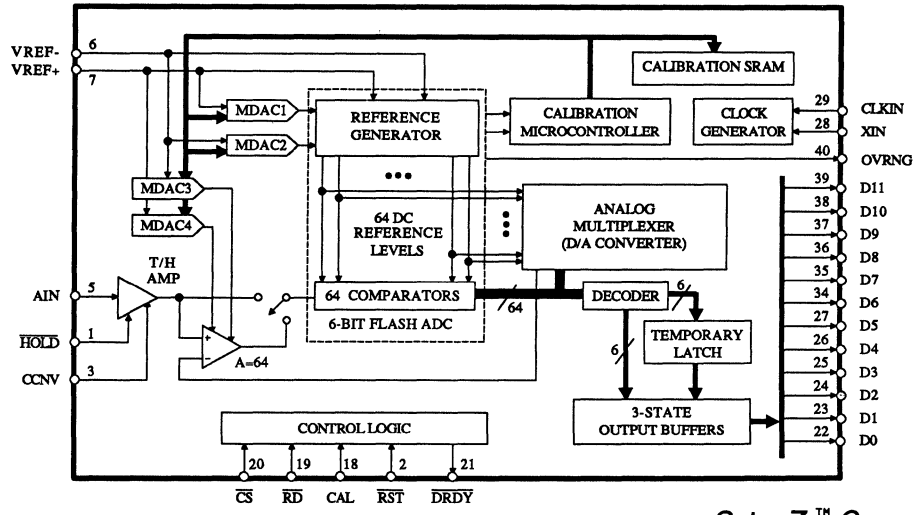
General Description

The CSZ5412 CMOS analog to digital converter provides a true 12-bit representation of an analog input signal at sampling rates up to 1MHz. To achieve high throughput, the CSZ5412 uses pipelined acquisition and settling times as well as overlapped conversion cycles.

Unique self-calibration circuitry, which can be accessed in hardware or software, insures 12-bit accuracy over time and temperature and eliminates the need for manual calibration of any kind. Also, a background calibration process constantly adjusts the converter's linearity, thereby insuring superior harmonic distortion and signal-to-noise performance throughout operating life.

The CSZ5412's advanced CMOS construction provides low power consumption of 700mW and the inherent reliability of monolithic devices.

ORDERING INFORMATION: Page 128



S-to-Z ™ Converter

7

Preliminary Product Information | *This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.*

OCT '87
DS2PP2

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, Texas 78760
(512)445-7222 TWX:910-874-1352

ANALOG CHARACTERISTICS (T_A = 25°C (Note 1); All VA+ pins, VD+ = 5V; All VA- pins, VD- = -5V; VREF+ = +1.5V; VREF- = -1.5V; f_{CLK} = 8MHz for -1, 4MHz for -2; 100 kHz Full Scale Input Sinewave; Continuous Convert Mode unless otherwise specified).

Parameter*			CSZ5412-J,K min	CSZ5412-J,K typ	CSZ5412-J,K max	CSZ5412-A,B min	CSZ5412-A,B typ	CSZ5412-A,B max	CSZ5412-S,T min	CSZ5412-S,T typ	CSZ5412-S,T max	Units
Resolution			12			12			12			Bits
Specified Temperature Range			0 to 70			-40 to +85			-55 to +125			°C
Dynamic Performance												
Peak Harmonic or Spurious Noise												
100kHz Input	25°C	-J,A,S	74	76		74	76		74	76		dB
		-K,B,T	77	79		77	79		77	79		
	T_{min} to T_{max} (Note 1)	-J,A,S	TBD	75		TBD	75		TBD	75		
		-K,B,T	TBD	75		TBD	75		TBD	75		
490kHz Input		-J,A,S		75			75			75		
		-K,B,T		75			75			75		
Total Harmonic Distortion		-J,A,S		0.02			0.02			0.02		%
		-K,B,T		0.02			0.02			0.02		
Signal-to-(Noise plus Distortion)												
0dB Input (Full Scale)	25°C	-J,A,S	65	67		65	67		65	67		dB
		-K,B,T	68	70		68	70		68	70		
	T_{min} to T_{max} (Note 1)	-J,A,S	TBD	67		TBD	67		TBD	67		
		-K,B,T	TBD	70		TBD	70		TBD	70		
-40dB Input		-J,A,S		32			32			32		
		-K,B,T		32			32			32		
dc Accuracy												
Linearity Error												
	-J,A,S	T_{min} to T_{max}		±3/4	±1		±3/4	±1		TBD	TBD	LSB
(Note 1)	-K,B,T	T_{min} to T_{max}		±3/8	±1/2		±3/8	±1/2		TBD	TBD	
Differential Linearity												
	-J,A,S	T_{min} to T_{max}				No Missing Codes Guaranteed						
(Note 1)	-K,B,T	T_{min} to T_{max}			±0.9			±0.9			TBD	LSB
Full Scale Error		T_{min} to T_{max}		±1/2			±1/2			±3/4		LSB
Offset Error (Note 2)		T_{min} to T_{max}		±1/2			±1/2			±3/4		LSB

Notes: 1. All T_{min} to T_{max} specifications apply after calibration at the temperature of interest. Temperatures specified define ambient conditions in free-air during test and do not refer to the junction temperature of the device.
2. Worst case conditions: unipolar (VREF- = 0V) or bipolar (VREF- = -1.5V) input range.

* Refer to *Definitions* on page 127.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter	CSZ5412-J,K min	typ	max	CSZ5412-A,B min	typ	max	CSZ5412-S,T min	typ	max	Units
Analog Input										
Aperture Time		35			35			35		ns
Aperture Jitter		50			50			50		ps, rms
Input Bandwidth										
Small Signal, -3dB (Note 3)		4			4			4		MHz
Full Power, -3dB		3			3			3		MHz
Overvoltage Recovery Time (Note 4)		1			1			1		us
Analog Input Impedance at dc		10			10			10		Mohms
Input Capacitance VREF- pin		50			50			50		pF
AIN, VREF+ pins		10			10			10		pF
Conversion & Throughput										
Conversion Time −1	1.25		1.375	1.25		1.375	1.25		1.375	us
(Notes 5, 6) −2	2.5		2.75	2.5		2.75	2.5		2.75	us
Throughput Rate −1	1			1			1			MHz
(Note 6) −2	0.5			0.5			0.5			MHz
Acquisition Time (Note 7)		300			300			300		ns
Power Supplies										
Power Supply Current (Note 8)										
I_{A+}		65	TBD		65	TBD		65	TBD	mA
I_{A-}		−65	TBD		−65	TBD		−65	TBD	mA
I_{D+}		5	TBD		5	TBD		5	TBD	mA
I_{D-}		−5	TBD		−5	TBD		−5	TBD	mA
Power Dissipation (Note 8)		700	TBD		700	TBD		700	TBD	mW
Power Supply Rejection										
Positive Supplies		TBD			TBD			TBD		dB
Negative Supplies		TBD			TBD			TBD		dB

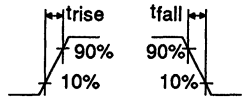
Notes:
3. Input 40 dB below full scale.
4. Temporary overrange input conditions of less than 0.5V beyond the references will not affect subsequent conversions. If the sampled analog input exceeds either reference voltage by greater than 0.5V, the CSZ5412 may require 4288 master clock cycles to recover to 12-bit accuracy.
5. Measured from falling transition on $\overline{\text{HOLD}}$ to falling transition on $\overline{\text{DRDY}}$.
6. Applies for conversions triggered externally. In Continuous Convert mode throughput proceeds at one-eighth the master clock frequency with a fixed 10 clock cycle conversion time.
7. The internal track-and-hold returns to the track mode on the fourth master clock cycle after the start of a conversion cycle. It is guaranteed to acquire a full-scale step to 12-bit accuracy while operating at full throughput.
8. All outputs unloaded. All inputs CMOS levels.

SWITCHING CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; All VA+ pins, VD+ = 5V ± 5%; All VA- pins, VD- = -5V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF).

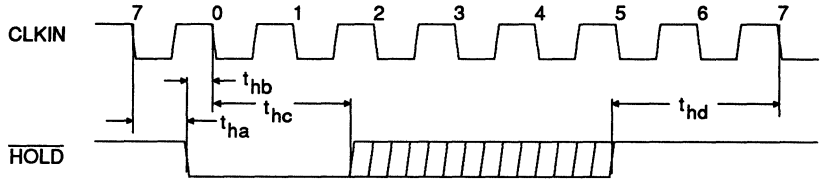
Parameter	Symbol	Min	Typ	Max	Units
Master Clock Frequency: -1	f_{CLK}	TBD	-	8	MHz
-2		TBD	-	4	MHz
Master Clock Duty Cycle	-	40	-	60	%
Rise Times: Any Digital Input (Note 9)	t_{rise}	-	-	1.0	us
Any Digital Output		-	20	-	ns
Fall Times: Any Digital Input (Note 9)	t_{fall}	-	-	1.0	us
Any Digital Output		-	20	-	ns
Hold/Master Clock Phase Relationship					
State 7 to $\overline{HOLD}$ Low	t_{ha}	50	-	-	ns
$\overline{HOLD}$ Low to State 0	t_{hb}	30	-	-	ns
State 0 to $\overline{HOLD}$ High	t_{hc}	50	-	-	ns
$\overline{HOLD}$ High to State 7	t_{hd}	30	-	-	ns
Conversion Time (Note 10)	t_c	10	-	11	MCC*
$\overline{DRDY}$ Pulse Width	t_{dpw}	-	3	-	MCC*
Data Delay Time	t_{dd}	-	40	TBD	ns
Access Times: $\overline{CS}$ Low to Data Valid	t_{csa}	-	90	TBD	ns
(Note 11) $\overline{RD}$ Low to Data Valid	t_{rda}	-	90	TBD	ns
Output Float Delay: $\overline{CS}$ or $\overline{RD}$ High to Output Hi-Z	t_{fd}	-	50	TBD	ns
Set Up Times: CAL to $\overline{CS}$ Low	t_{cs}	TBD	10	-	ns
Hold Times: $\overline{CS}$ High to CAL Invalid	t_{ch}	TBD	20	-	ns
Cal Pulse Width: CAL and $\overline{CS}$ Low	t_{csh}	2	-	4096	MCC*
$\overline{RST}$ Pulse Width	t_{rpw}	2	-	4096	MCC*

Notes: 9. Any digital input except $\overline{HOLD}$ and CLKIN, which should be driven with signals which have rise and fall times of at least 25 ns.
10. Conversion time in the Continuous Convert mode is a fixed 10 clock cycles.
11. Data goes valid when both $\overline{CS}$ and $\overline{RD}$ are low simultaneously. Each access time assumes the other control input is already low or falls concurrently.

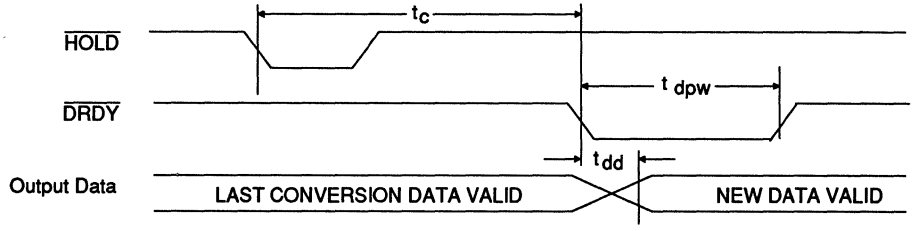
* MCC = Master Clock Cycles



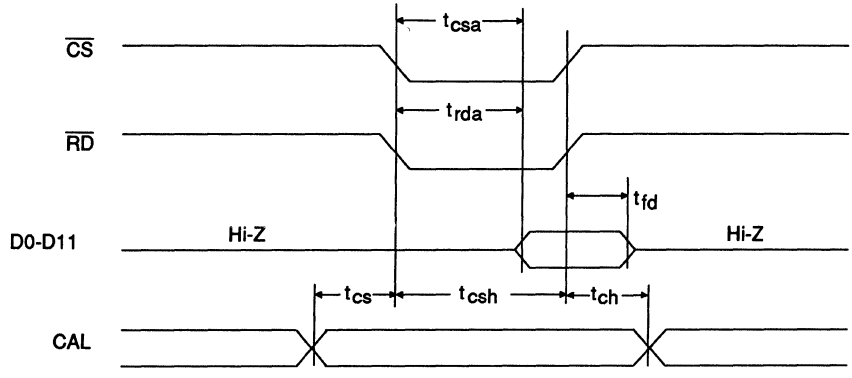
Rise and Fall Times



Hold/Master Clock Phase Relationship



Conversion Timing



Read and Calibration Control Timing

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; All VA+ pins, VD+ = 5V ± 5%; All VA- pins, VD- = -5V ± 5%) All measurements below are performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (Note 12)	V_{IH}	2.0	-	-	V
Low-Level Input Voltage (Note 12)	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 13)	V_{OH}	VD+ - 1.0V	-	-	V
Low-Level Output Voltage Iout = 1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-10	-	+10	uA
3-State Leakage Current	I_{OZ}	-10	-	+10	uA
Digital Output Pin Capacitance	C_{out}	-	9	-	pF

Note: 12. All pins except $\overline{HOLD}$ and CLKIN which accept only CMOS-compatible inputs (V_{IL} = 0.5V and V_{IH} = VD+ - 0.5V).
13. I_{out} = -100µA. This specification guarantees TTL compatibility (V_{OH} = 2.4V @ I_{out} = -40µA).

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see note 14).

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies: Positive Digital	VD+	4.75	5.0	VA2+, VA5+	V
Negative Digital	VD-	−4.75	−5.0	−5.25	V
Positive Analog	VA1+ - VA5+	4.75	5.0	5.25	V
Negative Analog	VA1- - VA3-	−4.75	−5.0	−5.25	V
Analog Input Voltage	V_{AIN}	VREF-	-	VREF+	V
Analog Reference Voltages					
Unipolar Input Range	VREF+	2.0	-	3.0	V
	VREF-	-	AGND	-	V
Bipolar Input Range	VREF+	1.0	-	1.5	V
	VREF-	−1.0	-	−1.5	V

Notes: 14. All voltages with respect to ground.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to ground).

Parameter	Symbol	Min	Max	Units
DC Power Supplies: Positive Digital	VD+	−0.3	VA2+,VA5+ + 0.3	V
Negative Digital	VD-	0.3	−6.0	V
Positive Analog (Note 15)	VA1+ - VA5+	−0.3	6.0	V
Negative Analog	VA1- - VA3-	0.3	−6.0	V
Input Current, Any Pin Except Supplies (Note 16)	I_{in}	-	+10	mA
Analog Input Voltage (AIN and VREF pins)	V_{INA}	VA1- - VA3- - 0.3	VA2+,VA5+ + 0.3	V
Digital Input Voltage	V_{IND}	−0.3	VA2+,VA5+ + 0.3	V
Ambient Operating Temperature	T_A	−55	125	°C
Storage Temperature	T_{stg}	−65	150	°C

Notes: 15. VA1+, VA3+, VA4+ must never exceed VA2+ and VA5+ by more than 0.3V.
16. Transient currents of up to 100mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

THEORY OF OPERATION

To achieve high speed and high accuracy, the CSZ5412 implements a standard 2-step flash A/D conversion using a self-calibrating architecture. Throughput is further maximized using pipelined acquisition and settling times as well as overlapped conversion cycles.

2-Step Flash A/D Conversion

The fastest method of performing A/D conversion is the brute-force single-step flash approach, for which an N-bit conversion involves comparing the analog input to 2^N-1 graduated voltage levels. The outputs from the 2^N-1 comparators are then processed and encoded into the proper binary format. The major limitation to this technique is that the number (and accuracy requirements) of comparators doubles with each additional bit of resolution. Thus, single-step flash converters are impractical today at greater than 8 or 10 bits of resolution.

The 2-step technique that the CSZ5412 uses employs slightly more complex sub-circuit blocks to achieve high resolution and results in negligible speed degradation. As shown in Figure 1, the CSZ5412 consists of a track-and-hold amplifier (T/H_1), a 6-bit flash ADC, a 6-bit DAC, and a differential amplifier. When the convert command is issued, T/H_1 holds the analog input signal and the flash ADC converts the six MSB's (most-significant-bits) of the output word. The MSB's, once decoded, are latched. The flash converter's output is also loaded into the DAC. The DAC's output therefore represents the analog input less the quantization error of the first 6-bit flash conversion. This signal is then subtracted from the original analog input to yield the quantization error, which is then multiplied by 64 (2^6) and again applied to the flash ADC to yield the six LSB's (least-significant-bits). In effect, the first 6-bit flash forms the transfer function into 64 segments which are then filled in with 64 codes each by the second 6-bit flash. This yields a total of 4096 codes (64x64) for 12-bit resolution.

Calibration

The CSZ5412 uses several calibration techniques to insure 12-bit accuracy over time and temperature. A unique reference generating circuit provides the 64 graduated reference levels for the flash ADC and DAC. Critical to the CSZ5412's overall linearity, these references are continually adjusted to 12-bit accuracy during device operation. This background adjustment process is completely transparent to the user and results in less than ±1/2 LSB nonlinearity. Also, all comparators in the flash ADC are auto-zeroed to avoid differential linearity errors at the 64 segment boundaries due to noise and/or offsets in the comparators.

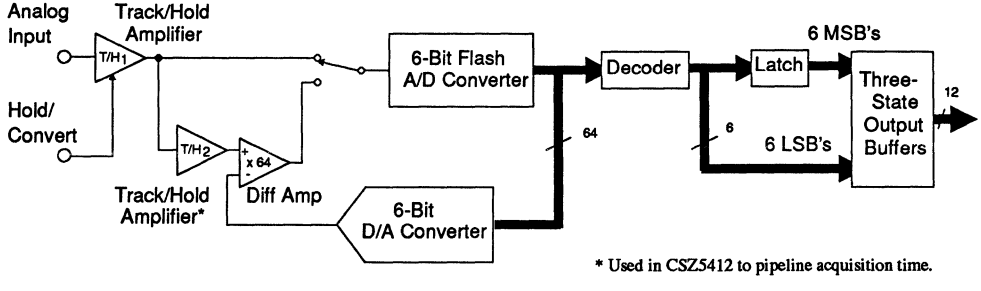


Figure 1. Block Diagram of 2-Step Flash A/D Converter

The CSZ5412 also uses digital correction schemes. An on-chip microcontroller manipulates dedicated MDAC's to set the gain and offset of the 6-bit flash ADC; this insures less than ±1/2 LSB overall full-scale and offset errors in the CSZ5412. Gain and offset are similarly calibrated in the differential amplifier to avoid linearity errors at the 64 segment boundaries.

Upon power-up, the CSZ5412 is reset in hardware or software to initially calibrate the device. Calibration can be similarly initiated at any later time throughout operating life to insure 12-bit accuracy independent of environmental conditions.

Pipelined Timing

To achieve throughput rates up to 1MHz, the CSZ5412 pipelines settling times in both the sampling and conversion processes. The CSZ5412 can actually begin a conversion cycle while still operating on the previous sample. As shown in Figure 2, the *Hold and Convert* command for Sample N+1 can be issued before data from Sample N is valid at the output. By definition, the throughput time of the CSZ5412 is shorter than the conversion time due to the overlapped conversion cycles. Compared to a non-pipelined 1MHz ADC, the CSZ5412 provides the same 1MHz throughput, only the output data is delayed slightly in time (1.25µs delay through the ADC rather than 1µs).

The CSZ5412 also uses a second track-and-hold amplifier (termed *T/H2* in Figure 3) to pipeline the converter's acquisition time. As shown in Figure 3, *T/H2* holds the output from *T/H1* valid for the second flash conversion, *Flash 2*. This allows *T/H1* to release and acquire the analog input signal during the second flash conversion, allowing another *Hold & Convert* command to be issued even before the completion of *Flash 2*.

DIGITAL CIRCUIT CONNECTIONS

In addition to master clock and sampling connections which set the converter's timing, the CSZ5412 offers an *Overrange* output, 3-state output buffers, and flexible control interface. The CSZ5412 can therefore connect directly to a microprocessor's data and control busses or can be operated in a stand-alone mode.

Master Clock

The CSZ5412 operates from a master clock reference which must be supplied in the form of either a crystal or external clock. A crystal can be tied across the CLKIN and XIN pins, or alternatively, the CSZ5412 can be synchronized to the external system by driving CLKIN with a CMOS-compatible clock (XIN left floating). The master clock should never be shut off for longer than one second while the CSZ5412 is powered-up or the converter's dynamic logic could potentially draw excessive current. Clock

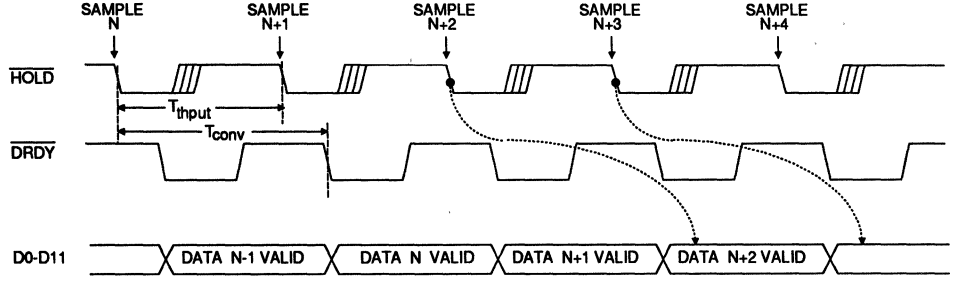


Figure 2. Pipelined Conversion Cycles

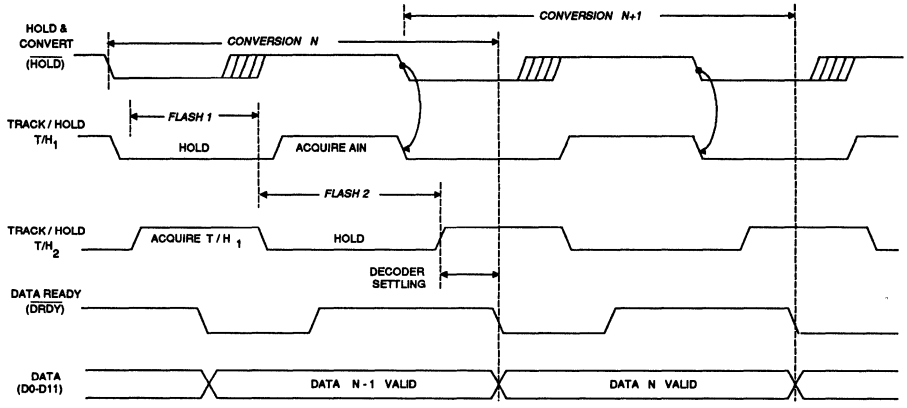


Figure 3. Pipelined Acquisition and Settling Times.

cycles can be selectively skipped at any time, but the clock's average frequency should never drop below the device's minimum specification (see Switching Characteristics, page 114).

Sampling/Initiating Conversions

There are two methods of controlling the CSZ5412's sampling/conversion timing. First, the CSZ5412 has a $\overline{\text{HOLD}}$ input which, on a falling edge, places the input track-and-hold amplifier in the hold state and initiates a conversion cycle. The CSZ5412 also features a *Continuous Convert* mode (CCNV and $\overline{\text{HOLD}}$ high) in which hold commands are internally generated every eight master clock cycles. The sampling/throughput rate is therefore controlled by adjusting the master clock frequency and there is no need to generate a sampling clock.

Lower sampling rates can be created in the *Continuous Convert* mode by running the CSZ5412 at full throughput and decimating the output, selectively reading only a fraction of the available samples. Variable sampling rates can be implemented in this manner using a programmable divider on the $\overline{\text{DRDY}}$ output. When operating in the *Continuous Convert* mode, attention should be paid to jitter on the master clock, since jitter will directly affect sampling purity.

If the phase of sampling must be precisely controlled, the $\overline{\text{HOLD}}$ input must be used since the hold signal is internally-generated in the *Continuous Convert* mode. A falling edge on $\overline{\text{HOLD}}$ places the internal track-and-hold amplifier in the hold state and signals a conversion cycle to begin on the next rising edge of the master clock. The $\overline{\text{HOLD}}$ input was designed for minimum aperture jitter and therefore requires CMOS-compatible logic levels (not TTL-compatible).

Due to the CSZ5412's background calibration timing, $\overline{\text{HOLD}}$ commands must be synchronized to the master clock and can only occur at intervals of 8 master clock cycles. The first $\overline{\text{HOLD}}$ command after a reset or calibration cycle defines state 0 in the CSZ5412's timing circuitry (see Figure 4). The sampling signal applied to $\overline{\text{HOLD}}$ must adhere to frequencies of $f_{clk}/8N$ such that subsequent $\overline{\text{HOLD}}$ commands will always fall between state 7 and state 0. If the sampling clock changes phase and a $\overline{\text{HOLD}}$ command occurs before state 7 or after state 0 the CSZ5412 may be thrown out of calibration, and 4288 clock cycles must be allowed for the converter to complete a full background adjustment cycle. Likewise, conversion data should be considered invalid for 4288 clock cycles following the first $\overline{\text{HOLD}}$ command after reset or calibration to insure specified accuracy.

7

Most often the sampling signal applied to $\overline{HOLD}$ can be derived from the master clock. In these cases, the master clock is divided by 8, 16, 24, 32, etc. If sampling must be locked to some external clock source, a phase-locked loop can be used to generate a master clock signal for CLKIN from the sampling signal. In this instance jitter on the $\overline{HOLD}$ input will directly affect sampling purity; however, the CSZ5412 will tolerate significant jitter on the master clock without loss of accuracy (assuming the $\overline{HOLD}$/CLKIN phase specifications outlined on page 114 are met).

Conversion Time/Throughput

In the *Continuous Convert* mode, throughput will proceed at one-eighth the master clock frequency and the delay through the CSZ5412 will be ten master clock cycles. When hold commands are generated externally at the $\overline{HOLD}$ pin, the analog input is held immediately as the $\overline{HOLD}$ input falls and the conversion cycle begins on the next rising edge of the master clock. The CSZ5412's conversion time will range from 10 to 11 clock cycles depending on the phase relationship of the $\overline{HOLD}$ signal to the master clock (see Figure 4). Throughput can still proceed at $f_{clk}/8$ independent of the conversion time. The pipelined overlap between conversion cycles will range from to 2 to 3 clock cycles.

Reset

Upon power-up, the CSZ5412 must be reset to guarantee a consistent starting condition and initially calibrate the device. A falling edge on the $\overline{RST}$ pin clears all internal logic and a rising edge initiates a calibration cycle which takes 203,578 master clock cycles to complete. The $\overline{RST}$ input must remain low for at least 2 master clock cycles but no longer than one second or the internal dynamic logic could draw excessive current. The $\overline{RST}$ input is internally latched, so a simple power-up reset circuit can be constructed by tying a capacitor from $\overline{RST}$ to DGND and a resistor from $\overline{RST}$ to VD+.

Due to the CSZ5412's modest power dissipation and low temperature drift, no warm-up time is needed before reset to accommodate any self-heating effects. However, the voltage references (VREF+ and VREF-) should have stabilized to within their specified accuracies. The CSZ5412 can be reset later at any time during operation to initiate calibration. Reset overrides all other functions. If reset, the CSZ5412 will clear and initiate a new calibration cycle mid-conversion or mid-calibration.

Overrange

The CSZ5412 will flag an overrange input at the OVRNG pin whenever *the sampled analog input* exceeds either the positive or negative reference voltage. If the sampled input exceeds VREF+, OVRNG will go high as DRDY falls, and all ones will be loaded into the output buffers. Similarly, if the analog input is below VREF-, OVRNG will go high as all zeroes are loaded into the output buffers. An overrange condition will not impede device operation and OVRNG

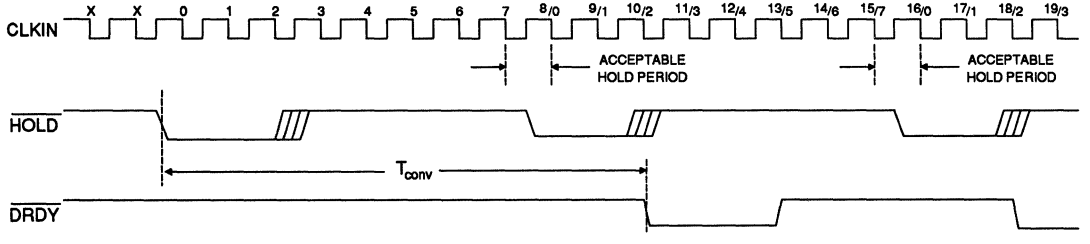


Figure 4. Hold / Conversion Timing.

will return low within 2144 to 4288 master clock cycles or at the end of a reset or calibration cycle if one is initiated. If the *sampled analog input* ever exceeds either reference by greater than 0.5V, the CSZ5412 may lose calibration. The OVRNG output can therefore be used as an interrupt indicating accuracy may have been compromised and up to 4288 clock cycles must be allowed for the CSZ5412 to recover.

The OVRNG output remains high throughout a reset/calibration sequence and will return low after its completion. It can therefore be used to generate an interrupt indicating the CSZ5412 has completed calibration and is ready for operation.

Microprocessor Controlled Operation

The CSZ5412 features 3-state output buffers and a control interface which allow the device to connect directly to a microprocessor's data and control busses. Strobing both $\overline{CS}$ and $\overline{RD}$ low enables the CSZ5412's 3-state output buffers with the converter's 12-bit output word. As shown in Figure 5, a decoded address is normally applied to $\overline{CS}$, and the $\overline{RD}$ input is derived from read and strobe signals from the microprocessor's control bus. The Data Ready ($\overline{DRDY}$) output can be used to generate an interrupt or drive a DMA controller to dump the CSZ5412's output directly into memory after each conversion. The $\overline{DRDY}$ output falls as new data is being loaded into the output buffers and returns high after three master clock cycles.

The CSZ5412 internally buffers its output data, so data can be read while the device is tracking or converting the next sample. Therefore, retrieving the converter's digital output requires no reduction in ADC throughput. The CSZ5412 should be synchronized to the digital system via CLKIN to avoid potential errors due to enabling the 3-state output buffers while the part is converting. Using TTL loads also increases the potential for crosstalk between the digital and analog portions of the system. This crosstalk is due to high digital supply and signal currents arising from the TTL drive current required of each digital output. Connecting CMOS logic to the CSZ5412's digital outputs is recommended. Suitable logic families include 4000B, 74HC, 74AC, 74ACT, and 74HCT.

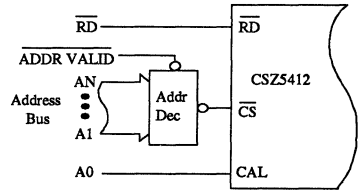


Figure 5. Microprocessor Controlled Operation.

$\overline{CS}$	$\overline{RD}$	CCNV	$\overline{HOLD}$	CAL	$\overline{RST}$	Function
0	0	X	X	0	1	Read Output Data
*	1	X	X	*	1	High Impedance Data Bus
1	X	X	X	X	1	High Impedance Data Bus
*	X	1	1	*	1	Continuous Convert Mode
*	X	0	⅂	*	1	Hold and Start Convert
X	X	X	X	X	0	Reset
0	X	X	X	1	X	Reset

*** Not critical to the operation specified. However, $\overline{CS}$ should not be low with CAL high or a software reset will result.**

Table 1. CSZ5412 Truth Table.

Initiating Calibration

In addition to the hardware reset, the CSZ5412 features a software calibration capability. Whenever CAL goes high with $\overline{CS}$ low, a calibration cycle will be initiated which is equivalent to the reset function described on page 120. As shown in Figure 5, line A0 from the address bus can be connected to the CAL input when operating under microprocessor control. A read cycle from the CSZ5412's base address with A0 low will therefore retrieve output data while a read or write cycle with A0 high will initiate calibration. The CAL input is level sensitive, and like $\overline{RST}$, CAL overrides all other functions. Software-initiated calibrations can thus be used in lieu of a hardware reset at power-up.

Stand-Alone Operation

The CSZ5412 can be operated in a stand-alone mode independent of intelligent control. In this mode, $\overline{CS}$ and $\overline{RD}$ are hard-wired low, permanently enabling the 3-state output buffers. A free-running condition is established when CAL is tied low, and $\overline{HOLD}$ is continually strobed low or CCNV is held high. The CSZ5412's $\overline{DRDY}$ output can be used to externally latch the output data if desired. The $\overline{DRDY}$ output will strobe low for three master clock cycles after each conversion. Data will typically be unstable for 40ns after $\overline{DRDY}$ falls, so it should be latched on the rising edge of $\overline{DRDY}$. This results in a total delay of 13 master clock cycles through the CSZ5412.

ANALOG CIRCUIT CONNECTIONS

Like most 2-step flash A/D converters with internal track-and-hold amplifiers, the CSZ5412 offers a trivial load at its analog input compared to successive-approximation and single-step flash A/D converters. The reference connections similarly present high impedance loads. However, accurate system operation still requires careful attention to details at the design stage regarding source impedances as well as grounding and decoupling schemes.

Analog Input and Reference Connections

The CSZ5412's analog input range is defined by the voltages applied to the VREF- and VREF+ pins. The analog input (AIN) is referenced only to these reference voltages and is completely independent of the analog ground pins. The first code transition ideally occurs 1 LSB above VREF- and the last transition occurs 1 LSB below VREF+. The CSZ5412 can operate with input ranges as low as 2.0V p-p, but signal-to-noise performance is maximized by using the full specified range of 3V p-p. Unipolar input ranges are achieved by tying VREF- to the system's analog ground and applying the reference voltage to VREF+. Bipolar input ranges are achieved by applying positive and negative voltages of equal magnitude to VREF+ and VREF- respectively. In this configuration, coding is in offset-binary format.

The CSZ5412's analog input (AIN) pin looks directly into the noninverting terminal of the track-and-hold amplifier resulting in over 10MΩ input impedance and less than 10pF input capacitance. The VREF+ connection also presents a static load of 10MΩ and 10pF, and VREF- presents a static load of 10MΩ and 50pF. These static capacitive loads of 10pF and 50pF dominate the analog input and reference input impedance characteristics at high frequencies. The VREF+ and VREF- connections also have minor dynamic loads which require the reference inputs to be decoupled with 0.01μF (ceramic) capacitors.

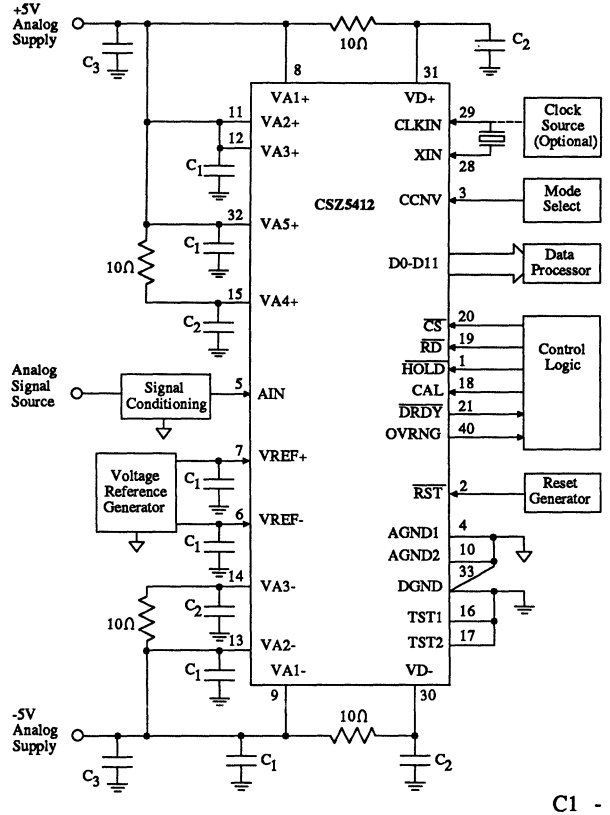
The voltage applied to the analog input (AIN) pin should not exceed either reference voltage by more than 0.5V. If such a signal is sampled by the internal track/hold amplifier, the CSZ5412 could be thrown out of calibration. Output data could then be invalid for the subsequent 4288

master clock cycles until the CSZ5412 completes a background adjustment cycle.

Grounding and Power Supply Decoupling

The CSZ5412 uses the analog ground connections, AGND1 and AGND2, only as stable, low impedance sources. No dc power currents flow through these connections, and they are completely independent of AIN and DGND. Still, AGND1 and AGND2 should be tied to the system's analog ground. The CSZ5412's analog input is referenced only to VREF+ and VREF-. Therefore, the analog input and reference voltages should be referred to the same ground potential (not necessarily AGND) which should be used as the entire system's analog ground. The optimal grounding configuration for the CSZ5412 utilizes one ground plane under the CSZ5412. Peripheral analog and digital circuitry should be partitioned on the circuit board and separate ground planes may or may not be used.

The digital and analog supplies are isolated within the CSZ5412 and are pinned out separately to minimize coupling between the analog and digital sections of the chip. The analog supplies also have multiple connections which minimize lead inductances and power separate portions of the converter's analog circuitry. The decoupling



C1 - 0.01µF ceramic
C2 - 0.01µF / / 0.1µF ceramic
C3 - 0.1µF ceramic

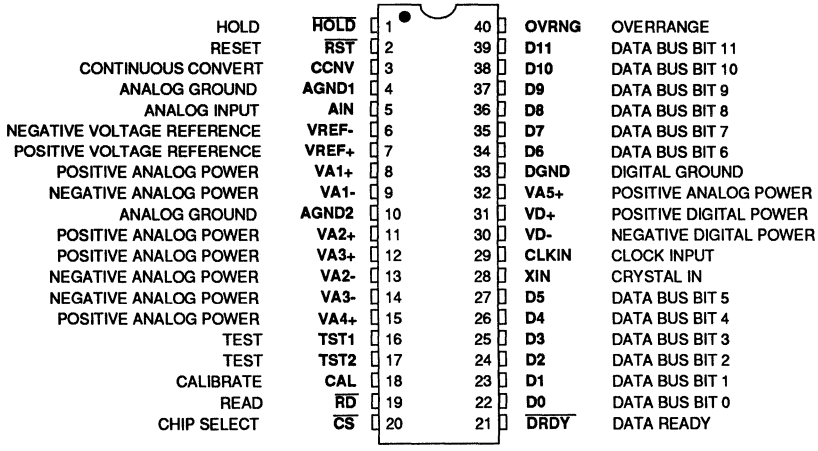
*VA2+ and VA5+ must be externally connected.

Figure 6. System Connection Diagram.

scheme shown in the *System Connection Diagram* in Figure 6 provides optimal decoupling between the CSZ5412's digital circuitry and the various analog sections of the chip. Ceramic capacitors are acceptable for all decoupling, and they should be placed as close to the supply pins as possible. If significant low-frequency noise is present on the supplies, 10µF tantalum capacitors are recommended in parallel with 0.1µF ceramic capacitors on the ±5V rails.

The positive digital power supply (VD+) should never exceed the positive analog supplies (VA2+ or VA5+) or the CSZ5412 could experience permanent damage. If the two supplies are derived from separate sources, care should be taken that the analog supply comes up first at power-up. The *System Connection Diagram* in Figure 6 shows a decoupling scheme which allows the CSZ5412 to be powered from a single set of ±5V rails. The positive digital supply is derived from the analog supplies though a 10Ω resistor to avoid the analog supply dropping below the digital supply. If this scheme is used, care must be taken to insure that any digital load currents (which flow through the 10Ω resistors) do not cause the magnitude of the digital supplies to drop below their minimum specification of 4.75V.

As with any high-speed, high-precision A/D converter, the CSZ5412 requires careful attention to grounding and layout arrangements. The CDB5412 evaluation board is available for the CSZ5412, which eliminates the need to design, build, and debug a high-precision PC board to initially characterize the part. The board comes with a socketed CSZ5412 and can be quickly reconfigured to simulate any combination of sampling, calibration, and master clock conditions.



PIN DESCRIPTIONS

Power Supply Connections

VD+ - Positive Digital Power, PIN 31.
Positive digital supply voltage. Nominally +5 volts.

VD- - Negative Digital Power, PIN 30.
Negative digital supply voltage. Nominally -5 volts.

DGND - Digital Ground, PIN 33.
Digital ground reference.

VA+ - Positive Analog Power, PINS 8, 11, 12, 15, 32.
Positive analog supply voltage. Nominally +5 volts.

VA- - Negative Analog Power, PINS 9, 13, 14.
Negative analog supply voltage. Nominally -5 volts.

AGND - Analog Ground, PIN 4, 10.
Analog ground reference.

Oscillator

CLKIN; XIN - Clock In, PIN 29; Crystal In, PIN 28.
Used to generate the internal master clock. A crystal can be tied across the two pins or an external CMOS-compatible clock can be driven into CLKIN if XIN is left floating.

Digital Inputs

$\overline{\text{HOLD}}$ - Hold Input, PIN 1.
A negative transition on $\overline{\text{HOLD}}$ puts the track-and-hold amplifier into the hold state and initiates the conversion sequence. Conversions must be synchronized with the master clock at $f_{CLK}/8N$ where N = 1,2,3. The $\overline{\text{HOLD}}$ input is CMOS-compatible.

CCNV - Continuous Convert, PIN 3.
When held high with the $\overline{\text{HOLD}}$ input high, throughput will proceed at $1/8^{th}$ the master clock frequency.

$\overline{\text{CS}}$ - Chip Select, PIN 20.
Activates the $\overline{\text{RD}}$ and CAL inputs. When $\overline{\text{CS}}$ is high, these inputs have no effect and the data bus (D0 through D11) is held in a high impedance state.

$\overline{\text{RD}}$ - Read, PIN 19.
When held low with $\overline{\text{CS}}$ also low, enables D0-D11.

$\overline{\text{RST}}$ - Reset, PIN 2.

When taken low, all internal logic is reset to its cleared or default state. When brought high again, a full calibration results. The CSZ5412 will not operate while $\overline{\text{RST}}$ is low nor during the resulting full calibration cycle.

CAL - Calibrate, PIN 18.

Same as $\overline{\text{RST}}$ only enabled by $\overline{\text{CS}}$.

Analog Inputs

VREF+ - Positive Voltage Reference, PIN 7.

Represents positive full scale voltage. Typically +1.5V with respect to AGND (bipolar system) or +3V with respect to AGND and VREF- (unipolar system).

VREF- - Negative Voltage Reference, PIN 6.

Represents negative full scale voltage. Typically -1.5V with respect to AGND (bipolar system) or tied to AGND (unipolar system).

AIN - Analog Input, PIN 5.

Analog input to the track-and-hold amplifier.

Digital Outputs

OVRNG - Overrange, PIN 40.

Goes high if the sampled analog input voltage exceeds VREF+ or VREF-. It does not impede device operation and returns low within 2144 to 4288 master clock cycles. OVRNG also goes high during reset and calibration cycles and can therefore be used to indicate end of calibration.

$\overline{\text{DRDY}}$ - Data Ready, PIN 21.

Falls when new data is becoming available at the outputs. Returns high three master clock cycles later.

Digital Input/Outputs

D0 through D11 - Data Bus, PINS 22 thru 27, 34 thru 39.

Three-state data bus.

Miscellaneous Pins

TST1 - Test, PIN 16.

Reserved for factory use. Must be tied to DGND for proper device operation.

TST2 - Test, PIN 17.

Reserved for factory use. Must be tied to DGND for proper device operation.

DEFINITIONS

Peak Harmonic or Spurious Noise (More accurately, Signal to Peak Harmonic or Spurious Noise) - The ratio of the rms value of the signal to the rms value of the next largest spectral component below the Nyquist rate (excepting dc). This component is often an aliased harmonic when the signal frequency is a significant proportion of the sampling rate. Expressed in decibels.

Total Harmonic Distortion - Ratio of the rms sum of all harmonics to the rms value of of the signal. Units in percent.

Signal-to-(Noise plus Distortion) - Ratio of the rms value of the signal to the rms sum of all other spectral components below the Nyquist rate (excepting dc). Expressed in decibels.

Linearity Error - The deviation of a code from a straight line passing through the endpoints of the transfer function after zero- and full-scale errors have been accounted for. "Zero-scale" is a point 1/2 LSB below the first code transition, and "full-scale" is a point 1/2 LSB beyond the code transition to all ones. The deviation is measured from the middle of each particular code. Units in LSB's.

Differential Nonlinearity - The deviation of a code's width from the ideal width. Units in LSB's.

Full Scale Error - The deviation of the last code transition from the ideal (VREF+ - 1 LSB). Units in LSB's.

Offset Error - The deviation of the first code transition from the ideal (VREF- + 1 LSB). Units in LSB's.

Aperture Time - The time required after the hold command is issued for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

Aperture Jitter - The range of variation in the aperture time. Effectively a "sampling window" which ultimately dictates the maximum input slew rate acceptable for a given accuracy. Units in picoseconds.

Ordering Guide

Model	Throughput	Signal to (Noise plus Distortion)	Linearity Error	Temp Range	Package
CSZ5412-JC2	500kHz	65 dB	±1 LSB	0 to 70°C	40-Pin Ceramic SB DIP
CSZ5412-KC2	500kHz	68 dB	±1/2 LSB	0 to 70°C	40-Pin Ceramic SB DIP
CSZ5412-JC1	1MHz	65 dB	±1 LSB	0 to 70°C	40-Pin Ceramic SB DIP
CSZ5412-KC1	1MHz	68 dB	±1/2 LSB	0 to 70°C	40-Pin Ceramic SB DIP
CSZ5412-AC2	500kHz	65 dB	±1 LSB	-40 to +85°C	40-Pin Ceramic SB DIP
CSZ5412-BC2	500kHz	68 dB	±1/2 LSB	-40 to +85°C	40-Pin Ceramic SB DIP
CSZ5412-AC1	1MHz	65 dB	±1 LSB	-40 to +85°C	40-Pin Ceramic SB DIP
CSZ5412-BC1	1MHz	68 dB	±1/2 LSB	-40 to +85°C	40-Pin Ceramic SB DIP
CSZ5412-SC1	1MHz	65 dB	TBD	-55 to +125° C	40-Pin Ceramic SB DIP
CSZ5412-TC1	1MHz	68 dB	TBD	-55 to +125° C	40-Pin Ceramic SB DIP

INTRODUCTION

As the industry's first monlithic 4-channel track-and-hold amplifier, the CS31412 frees-up board space and reduces system costs normally associated with sampling and multiplexing analog signals for conversion. The CS31412 takes a snapshot of four single-ended or two differential signals and stores the analog values in on-chip hold capacitors. An on-chip digital correction scheme calibrates all dc and dynamic errors, including hold pedestals, to less than 700 μV. Channel selection and calibration can be placed under software control using the microprocessor interface. Since the CS31412 can calibrate at any time or temperature, it ensures accuracy throughout its operating life.

The CS31412's fast 1 μs acquisition time and 12-bit accuracy make it ideal for processing high-frequency signals. In applications where fast sampling is not critical, the CS31412's 0.007 μV/ μs droop in the hold mode allows slower conversion of the channels without loss of accuracy. The CS31412 dissipates only 250 mW of power.

A complete single-channel track-and-hold, the CS3112, is also available. On-chip hold capacitors and calibration logic simplify use, and keep all dc and dynamic errors, including pedestal error, below 700 μV. This accuracy is ensured over time and temperature by easy user control of the calibration circuitry.

USER'S GUIDE

Device:	CS31412	CS3112
# of Track & Holds	4	1
Acquisition Time	1 μs	1 μs
Power Consumption	250 mW	130 mW
Package	18-Pin DIP	14-Pin DIP

CONTENTS

Semiconductor Corporation

CS31412

4 Channel Simultaneous Track and Hold

Features

- Completely Self-Contained
  - Four Track-and-Hold Amplifiers
  - On-Chip Hold Capacitors
  - Output Multiplexer
  - Two Output Buffer Amplifiers
  - Microprocessor Interface
- 800ns Acquisition Time to 0.01%
- Aperture Jitter : 100ps
- True 12-Bit Accuracy over Temperature
  - Total Offset Including Hold Pedestal: ± 700uV Max
- Low Droop Rate: 0.001uV/us
- Auto-Calibration Insures Accuracy Over Time and Temperature
- Low Power Dissipation: 250mW

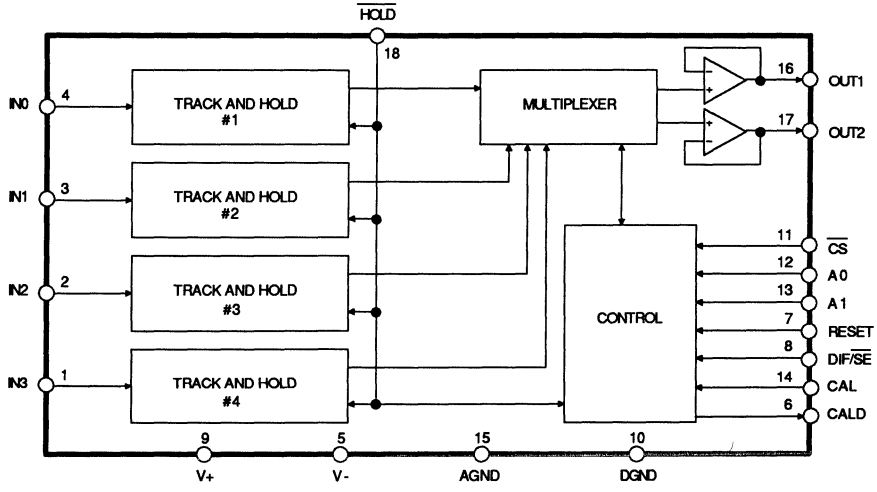
General Description

The CS31412 is a four-channel track and hold capable of processing four single-ended or two differential inputs with 12-bit accuracy. It consists of four track-and-hold amplifiers, an analog multiplexer, two output buffers, and a microprocessor interface.

Controlled by a single $\overline{\text{HOLD}}$ input, the four track-and-hold amplifiers can simultaneously hold their outputs with only 100ps of aperture jitter and later acquire their inputs within 800ns to 0.01%. On-chip hold capacitors limit droop to 0. 001uV/us, and first order leakage compensation minimizes droop over temperature. Unique auto-calibration circuitry limits all internal dynamic and dc errors to less than 700uV, guaranteeing 12-bit accuracy over time and temperature.

The CS31412 can be configured, controlled, and monitored through its microprocessor interface, or can be operated independently of intelligent control.

ORDERING INFORMATION: Page 7



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Crystal Semiconductor Corporation
P.O. Box 17847, Austin, Texas 78760
(512)445-7222 TWX:910-874-1352

ANALOG CHARACTERISTICS

(T_A = 25°C, V+ = +5.0V, V- = -5.0V, R_L = 10kΩ, C_L = 50pF, unless otherwise specified)

Parameter*	CS31412-J,K min	CS31412-J,K typ	CS31412-J,K max	CS31412-A,B min	CS31412-A,B typ	CS31412-A,B max	CS31412-S,T min	CS31412-S,T typ	CS31412-S,T max	Units
Specified Temperature Range		0 to +70			-40 to +85			-55 to +125		°C
Accuracy										
Total Offset (Note 1) 25°C			± 0.7			± 0.7			± 0.7	mV
T_{min}			± 0.7			± 2			± 3	mV
T_{max}			± 0.7			± 0.7			± 0.7	mV
Offset Drift (Note 2) T_{min} to T_{max}		± 0.020			± 0.025			± 0.030		mV/°C
Tracking Offset			± 20			± 20			± 20	mV
Nonlinearity (Note 3) 25°C			± 0.5			± 0.5			± 0.5	mV
T_{min} to T_{max}		± 0.5			± 0.5			± 0.5		mV
Gain Error (Note 3) 25°C		± 0.01			± 0.01			± 0.01		% FS
T_{min} to T_{max}		± 0.01			± 0.01			± 0.01		% FS
Dynamic Characteristics										
Acquisition Time										
(6V step to 0.01%) -J,A,S		1.8	2.5		1.8	2.5		1.8	2.5	us
-K,B,T		0.8	1.0		0.8	1.0		0.8	1.0	us
(6V step to 0.1%) -J,A,S		1.2			1.2			1.2		us
-K,B,T		0.6			0.6			0.6		us
Track to Hold Settling to 0.01%		0.5	0.8		0.5	0.8		0.5	0.8	us
Mux Output Settling Time										
(6V step to 0.01%) -J,A,S		1.8	2.5		1.8	2.5		1.8	2.5	us
-K,B,T		1.3	1.5		1.3	1.5		1.3	1.5	us
(6V step to 0.1%) -J,A,S		1.5			1.5			1.5		us
-K,B,T		1.0			1.0			1.0		us
Aperture Time		20			20			20		ns
Aperture Time Matching (Note 4)		2			2			2		ns
Aperture Jitter		100			100			100		ps
Interchannel Aperture Offset		100			100			100		ps
Droop Rate 25°C		± 0.001	± 0.1		± 0.001	± 0.1		± 0.001	± 0.1	uV/us
T_{min} to T_{max}			± 0.6			± 1.0			± 5.0	uV/us

Notes:
1. Applies after calibration at any temperature within the specified temperature range.
2. Applies over specified temperature range without recalibration since calibration at 25°C.
3. Applies over the input voltage range of -3V to +3V.
4. Part to part.

* Refer to *Error Definitions* on page 14.

ANALOG CHARACTERISTICS (Continued)

Parameter*	CS31412-J,K min	typ	max	CS31412-A,B min	typ	max	CS31412-S,T min	typ	max	Units
Analog Input										
Large Signal Bandwidth (6V p-p Input)		2			2			2		MHz
Small Signal Gain Bandwidth (60mV p-p Input)		2.5			2.5			2.5		MHz
Interchannel Isolation (Note 5)		90			90			90		dB
Input Impedance (dc)		100			100			100		MΩ
Input Capacitance		4			4			4		pF
Input Bias Current		100			100			100		pA
Analog Output										
Noise										
Track Mode (Note 6)		50			50			50		uV_{rms}
Hold Mode (Note 7)		33			33			33		uV_{rms}
Output Impedance at dc (Hold Mode) (Note 8)		0.1			0.1			0.1		Ω
Power Supplies										
Power Supply Currents										
Positive		25	45		25	45		25	45	mA
Negative		−25	−45		−25	−45		25	−45	mA
Power Supply Rejection Ratio										
Positive (Note 9)		75			75			75		dB
Negative (Note 10)		60			60			60		dB

Notes:
5. With a 100kHz input signal.
6. Total noise from dc to 1MHz.
7. Total noise from dc to 1MHz.
8. Applies over the input voltage range of -3V to +3V.
9. With 300mV p-p, 1kHz ripple applied to V+.
10. With 300mV p-p, 1kHz ripple applied to V-.

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Specifications are subjec to change without notice.

SWITCHING CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; V+ = 5V±10%; V- = -5V±10%)

Parameter	Symbol	Min	Typ	Max	Units
A0, A1, RESET, DIF/$\overline{SE}$, CAL to $\overline{CS}$ Setup Time	t_{su}	20	5	-	ns
$\overline{CS}$ to A0, A1, RESET, DIF/$\overline{SE}$, CAL Hold Time	t_h	5	1	-	ns
$\overline{CS}$ Pulse Width	t_{pw}	100	50	-	ns
$\overline{CS}$ Low and CAL High to CALD High	t_{cal}	-	3.5	10	ms

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; V+ = 5V±10%; V- = -5V±10%)

All measurements below are performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	1.7	-	V
Low-Level Input Voltage	V_{IL}	-	1.6	0.8	V
High-Level Output Voltage (Note 11)	V_{OH}	V+ -1.0V	-	-	V
Low-Level Output Voltage Iout=1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	10	uA

Note: 11. I_{out}=-100µA. This specification guarantees TTL compatability (VOH = 2.4V @ I_{out} = -40µA).

RECOMMENDED OPERATION CONDITIONS (AGND, DGND = 0V, see note 12).

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies: Positive	V+	4.5	5.0	5.5	V
Negative	V-	–4.5	–5.0	–5.5	V
Analog Input Voltage:	V_{IN}	–3.0	-	3.0	V

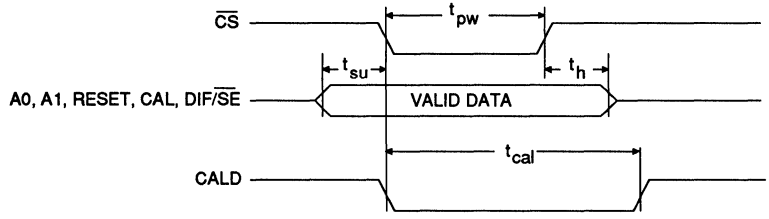
Note: 12. All voltages with respect to ground.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, All voltages with respect to ground)

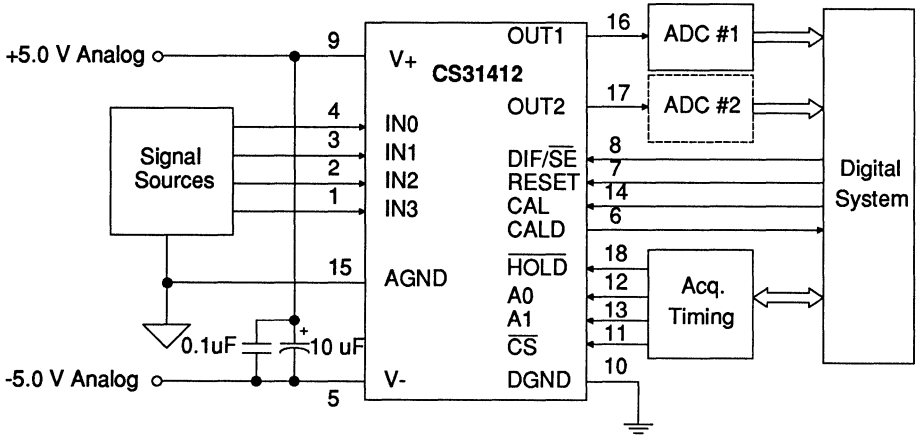
Parameter	Symbol	Min	Max	Units
DC Power Supplies: Positive	V+	− 0.3	6.0	V
Negative	V-	0.3	− 6.0	V
Input Current, Any Pin Except Supplies (Note 13)	I_{in}	-	±10	mA
Analog Input Voltage	V_{INA}	V- - 0.3	V+ + 0.3	V
Digital Input Voltage	V_{IND}	- 0.3	VA+ + 0.3	V
Ambient Operating Temperature	T_A	- 55	125	°C
Storage Temperature	T_{stg}	- 65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Note: 13. Transient currents of up to 100mA will not cause SCR latch-up.



Timing Diagram



System Connection Diagram

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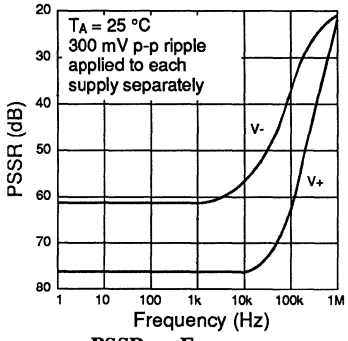
ORDERING GUIDE

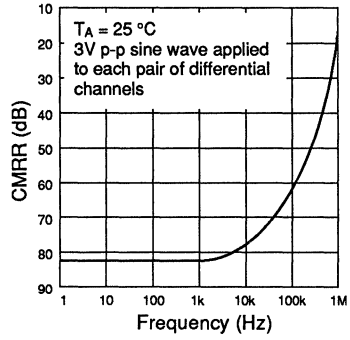
MODEL	ACQUISITION TIME	TEMP. RANGE	PACKAGE
CS31412-JD	2.5µs	0 TO 70°C	18-Pin Cerdip
CS31412-KD	1.0µs	0 TO 70°C	18-Pin Cerdip
CS31412-AD	2.5µs	-40 TO +85°C	18-Pin Cerdip
CS31412-BD	1.0µs	-40 TO +85°C	18-Pin Cerdip
CS31412-SD	2.5µs	-55 TO +125°C	18-Pin Cerdip
CS31412-TD	1.0µs	-55 TO +125°C	18-Pin Cerdip

TYPICAL PERFORMANCE CHARACTERISTICS

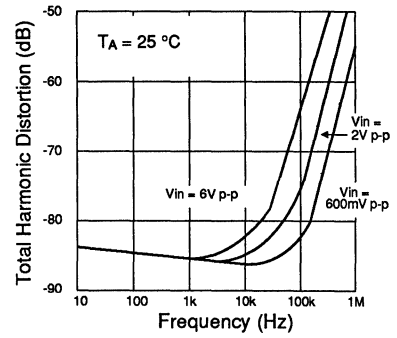
(V+ = +5.0V, V- = -5.0V)



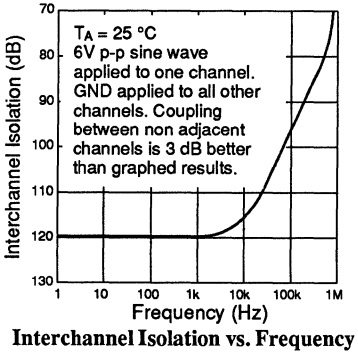
PSSR vs. Frequency



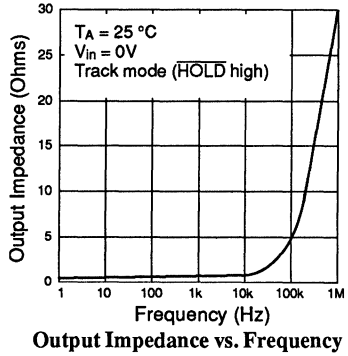
Differential Mode CMRR vs. Frequency



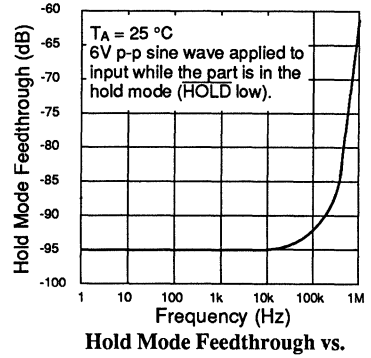
Distortion vs. Frequency



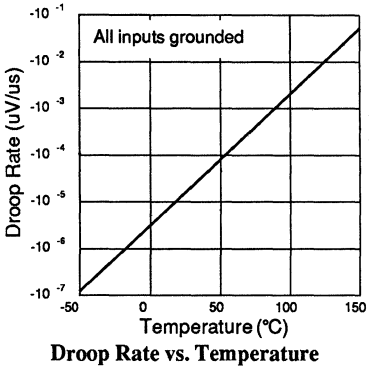
Interchannel Isolation vs. Frequency



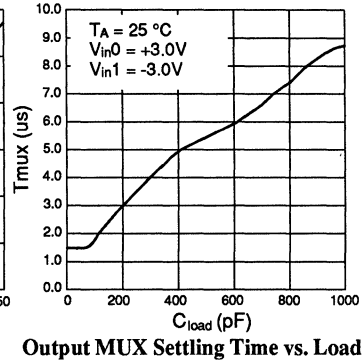
Output Impedance vs. Frequency



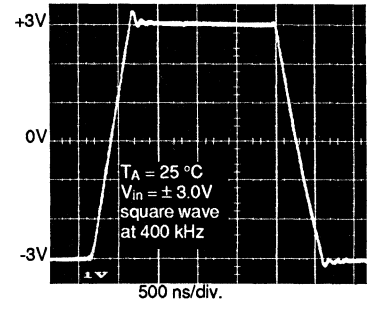
Hold Mode Feedthrough vs. Frequency



Droop Rate vs. Temperature



Output MUX Settling Time vs. Load Capacitance



Full Scale Acquisition

General Description

The CS31412 consists of four track-and-hold amplifiers with on-chip hold capacitors, an analog multiplexer, and two output buffers. The CS31412 requires no external components or manual trims of any kind to achieve true 12-bit performance, and thus eliminates the task of error budgeting several components with complex (and often hidden) error sources.

The CS31412 can handle either four single-ended or two differential analog signals. The device is controlled through its on-board microprocessor interface, or it can be operated independently of intelligent control. Unique auto-calibration circuitry nulls any dynamic or dc error introduced between the analog input pin and the buffer's output for each channel. The CS31412 thereby guarantees true 12-bit accuracy over time and temperature.

Analog Multiplexer

The analog multiplexer takes the outputs of the four track-and-hold amplifiers and passes the selected outputs to the OUT1 and OUT2 pins. When DIF/$\overline{SE}$ is low, the multiplexer is configured as a four-to-one multiplexer and each amplifier is treated as a single-ended analog input referenced to AGND. When DIF/$\overline{SE}$ is high, the multiplexer is configured as dual two-to-one multiplexers and the track-and-hold amplifiers are treated as two groups of two amplifiers which allows the CS31412 to process differential signals. This option can also be used to increase system throughput by using the CS31412 with two A/D converters (see System Throughput). Table 1 shows the multiplexer and buffer amplifier configurations as determined by the DIF/$\overline{SE}$ pin and the address pins, A0 and A1. In the differential mode, the A0 input should be tied low to avoid floating the output buffer amplifiers. In addition, the buffer amplifier at OUT2 in the single-ended mode does not float; its output remains within 50mV of AGND and must remain unconnected.

DIF/$\overline{SE}$	A1	A0	OUT1	OUT2
0	0	0	IN0	0V*
0	0	1	IN1	0V*
0	1	0	IN2	0V*
0	1	1	IN3	0V*
1	0	0	IN0	IN1
1	0	1	N/A**	N/A**
1	1	0	IN2	IN3
1	1	1	N/A**	N/A**

* AGND ± 50mV
** Floating Output: A0 should be tied low in differential mode

Table 1. Truth Table of MUX Configurations

Calibration

The CS31412 features on-chip digital intelligence and measurement circuitry capable of calibrating all four input channels. For each channel, the device internally deselects the input signal and switches a known reference voltage (AGND) to the input of the track-and-hold amplifier. In the calibration mode, the CS31412 uses an internal microcontroller and special nulling circuitry to reduce all errors at the OUT1 and OUT2 pins to less than ±700µV. Thus, all internal errors including dc offsets and dynamic errors due to charge injection (hold pedestal) are trimmed to 12-bit accuracy (732µV is 1/2 LSB at 12 bits with a ±3V input signal). The output of the CS31412 is only calibrated during the hold mode ($\overline{HOLD}$ low). During tracking, each channel may have up to ± 20mV of offset.

At power-up, the CS31412 automatically sets A0, A1, and DIF/$\overline{SE}$ low. The user then must initiate a calibration to initially calibrate the device. This is achieved by bringing the CAL input high and $\overline{CS}$ low simultaneously. Calibration can be similarly initiated during operation at any time thus insuring accuracy under any conditions. During the calibration cycle (which takes about 3.5ms to complete) the CALD pin remains low. During this period, any load on OUT1 and

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OUT2 must remain constant; otherwise, errors could be introduced which might affect accuracy. Another calibration cannot take place until CAL has been latched low by $\overline{CS}$ and then taken back high. If a new calibration is initiated before the current calibration is finished, the CS31412 will complete the current calibration before initiating the new one.

The DIF/$\overline{SE}$ input to the CS31412 must be in the correct state when initiating a calibration since the offsets of the analog output buffers are also calibrated. If the part is switched between the single ended and differential modes during operation, a new calibration must be initiated to guarantee that the Total Offset specification is met.

Digital Interface

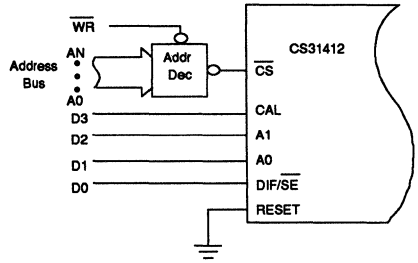
The CS31412 includes a digital interface designed for maximum flexibility. The digital inputs, A0, A1, CAL, and DIF/$\overline{SE}$, are internally gated with $\overline{CS}$. The input latches for the A0 and A1 inputs are level sensitive and latch on the rising edge of $\overline{CS}$. Any state changes on these pins while $\overline{CS}$ is low appear at the output(s). In a microprocessor-controlled application, the $\overline{CS}$ control input is usually derived from a decoded address as well as write and strobe signals off of the control bus (Figure 1a). Channel selection and calibration initiation thereby involve writing to the CS31412's address using data bits to control A0, A1, CAL, and DIF/$\overline{SE}$. For microprocessor-independent operation in single-ended mode, $\overline{CS}$ is tied low and the digital inputs are controlled by externally-latched signals (Figure 1b).

When using the differential mode in a microprocessor-independent configuration, $\overline{CS}$ cannot be tied low since DIF/$\overline{SE}$ is latched on the rising edge of $\overline{CS}$. A one-shot can be used to pulse $\overline{CS}$ on power-up. In applications with dedicated inputs, DIF/$\overline{SE}$ can be hardwired high or low.

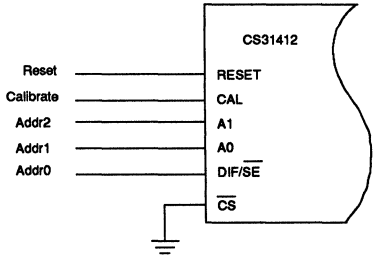
The CS31412's CALD output can be used to generate an interrupt indicating the CS31412 has completed calibration. Alternatively, calibration status can be polled in software by connecting CALD to the data bus via a three-state buffer.

Reset

The CS31412 includes a reset function which guarantees a predictable state (A0, A1, CAL and DIF/$\overline{SE}$ all low) after power up. The CS31412 is reset when the RESET pin high and $\overline{CS}$ is low simultaneously. Since this function can be emulated in software by writing all 0's to the CS31412 when under microprocessor control, it



a. MPU-Controlled Operation



b. MPU-Independent Operation

Figure 1. - CS31412 Control Connections

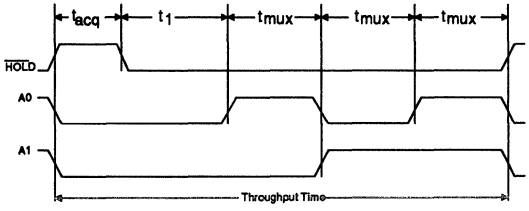
is mainly useful when operating independently of intelligent control (Figure 1b).

System Throughput

Throughput of the CS31412 varies depending on the number of input signals used, and the grade of the part. System timing diagrams which enable the the throughput of the CS31412 to be calculated are shown in Figure 2. Table 2 is a listing of throughput times for the various part grades and number of input channels used. These times assume that no time is required for A/D conversion. When the part is used in the differential mode, throughput time will be equal to the two channel throughput time.

Since one of the four channels must be connected to the output buffer, the Track-to-Hold settling time (t_{tth}) is included in the first channel's settling time (t_1). The address inputs A0, and A1 must be switched before the part is put in the hold mode ($\overline{HOLD}$ low) so that the first channel's output is valid at time (t_1). After the first output is settled, the addresses can be used to mux each of the other three channels to the output.

When interfacing the CS31412 with an A/D converter which includes an integrated sample/hold, such as Crystal's CS501X series, additional reduction in throughput time can be obtained by



t_{acq}: Acquisition Time
t_{tth}: Track to Hold Settling Time
t_{mux}: Mux Output Settling Time
t_1: First Channel Settling Time
$t_1 = \sqrt{t_{tth}^2 + t_{mux}^2}$

Figure 2. Four Channel Timing

Grade	Single Channel	Two Channels	Three Channels	Four Channels
-J, A, S	4.10us	6.58us	9.09us	11.6us
-K, B, T	2.70us	4.20us	5.71us	7.19us

Table 2. Throughput Time

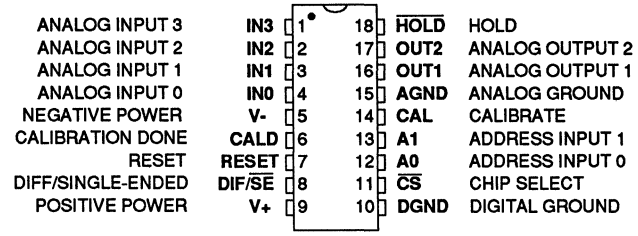
pipelining settling times. As soon as the A/D has captured the output of the CS31412, $\overline{HOLD}$ can be brought high and the CS31412 can acquire the new input signals and settle the first muxed channel while the A/D is converting. Likewise, output mux settling for all other other channels can be pipelined during conversion removing all of the CS31412's timing from the throughput equation. System throughput can therefore proceed at the ADC's maximum throughput. Using the CS31412 in the differential mode with two ADCs will reduce throughput time further because two channels can be converted simultaneously (see System Connection Diagram, page 7).

Power Supplies

The CS31412 uses the analog ground voltage (AGND) only as a reference voltage. No dc power currents flow through the AGND connection, and it is completely independent of DGND. However, any noise riding on AGND relative to the system's analog ground plane will result in offset errors. Therefore, the analog inputs should be referenced to the AGND pin which should be used as the entire system's analog ground. Decoupling should be performed between the V+ pin and the V- pin using 0.1uF ceramic cap. If significant low frequency noise is present on the supplies, a 10µF tantalum capacitor is recommended in parallel with the 0.1uF capacitor. *The decoupling capacitors should be placed as close to the CS31412's power supply pins as possible.*

8

PIN DESCRIPTIONS



Power Supplies

V+ - Positive Power, PIN 9
Most positive supply voltage. Nominally +5 volts.

V- - Negative Power, PIN 5
Most negative supply voltage. Nominally -5 volts.

DGND - Digital Ground, PIN 10
Digital ground reference.

AGND - Analog Ground, PIN 15
Analog ground reference.

Analog Inputs

IN0; IN1; IN2; IN3 - Analog Inputs 0;1;2;3, PINS 4,3,2,1
Analog inputs to the four track and hold amplifiers.

Digital Inputs

$\overline{CS}$ - Chip Select, PIN 11
Enables the RESET, DIF/$\overline{SE}$, A0, A1, and CAL digital inputs.

RESET - Reset, PIN 7
Sets A0, A1, DIF/$\overline{SE}$ and CAL low when held high and $\overline{CS}$ is strobed low.

DIF/$\overline{SE}$ - Differential/Single-Ended Select, PIN 8

Configures the output multiplexer in either a single-ended or differential mode. It is latched on the rising edge of $\overline{CS}$, but usually tied high or low. If set low, the four analog inputs are routed through OUT1. If set high, IN0 and IN1 are paired as one differential signal and IN2 and IN3 are paired as a second.

A0; A1 - Address Input 0; Address Input 1, PINS 12, 13

Select which amplifier or amplifier pair is output on the OUT1 and OUT2 pins. A0 should be held low when DIF/$\overline{SE}$ is high to avoid floating the outputs.

CAL - Calibrate, PIN 14

When taken high with $\overline{CS}$ low, initiates a full internal calibration.

$\overline{HOLD}$ - Hold, PIN 18

A falling transition on this pin signals all four amplifiers to hold their inputs simultaneously. When brought high, the amplifiers acquire, and then track the input signal.

Analog Outputs

OUT1; OUT2 - Analog Output 1; Analog Output 2, PINS 16, 17

The buffered outputs from the multiplexer; OUT1 is always active and OUT2 is active only in the differential mode (DIF/$\overline{SE}$ high).

Digital Outputs

CALD - Calibration Done, PIN 6

Indicates calibration status. After reset, if CALD is high the device has finished calibration. Returns low upon reset or the initiation of calibration.

ERROR DEFINITIONS

Total Offset - The difference between the analog voltage applied to the analog input (A0, A1, A2, or A3) and the signal that appears at the appropriate output pin (OUT1 or OUT2) after the hold command has been issued and all transients have settled. Applies only in the hold mode, not while tracking the analog inputs. Includes all internal offsets, including those due to charge injection (hold pedestals). Units in millivolts.

Nonlinearity - The deviation from a straight line on the plot of output vs input. Nonlinearity is specified as the change in *Total Offset* over the signal range of -3V to +3V. Units in millivolts.

Gain Error - Calculated as the difference between the *Total Offsets* resulting from -3V and +3V dc input signals relative to a 6V input range. Units in percent of full scale.

Acquisition Time - The time required after the negation of the hold command ($\overline{HOLD}$ high) for the track-and-hold amplifiers to reach their final values to within a specified error band (±0.01% or ± 0.1%) . Measured internally at the inputs to the multiplexer, it determines the minimum time allowed before reassertion of the hold command. Indicates nothing about the outputs as measured at OUT1 or OUT2. Units in microseconds.

Track-to-Hold Settling - The time required after the hold command is given for each track and hold to reach its final value to within a specified error band (±0.01%). Includes switch delay (aperture) time but not multiplexer and output buffer settling. Units in microseconds.

MUX Output Settling - The time required after reconfiguring the multiplexer for the outputs at OUT1 and OUT2 to reach their final value to within a specified error band (±0.01% or ±0.1%). Measured from the falling edge of $\overline{CS}$ with A0 and A1 valid. Units in microseconds.

Aperture Time - The time required after the hold command for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

Aperture Jitter - The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

Interchannel Aperture Offset - The range of variation in aperture time between the four track-and-hold amplifiers for a given hold command. A measure of simultaneity. Units in picoseconds.

Droop Rate - The change in the output voltage over time while in the hold mode. Units in microvolts per microsecond.

Large Signal Bandwidth - The frequency at which the output amplitude while tracking a full scale 6V p-p sine wave is 3dB below the input amplitude. Units in megahertz.

Small Signal Gain Bandwidth - The frequency at which the output amplitude while tracking a 60mV p-p sine wave is 3dB below the input amplitude. Units in megahertz.

Interchannel Isolation - A measure of crosstalk between input channels while in the track mode. Units in decibels.

• Notes •

Semiconductor Corporation

CS3112

High Speed Precision Track and Hold

Features

- Completely Self-Contained
  On-Chip Hold Capacitor
  Microprocessor Interface
- Fast Acquisition: 1us max to 0.01%
- Low Aperture Jitter: 100ps
- True 12-Bit Accuracy over Temperature
  Total Offset, Including
  Hold Pedestal: ±700uV max
- Low Droop Rate: 0.001uV/us
- Self-Calibration Insures Accuracy Over Time and Temperature
- Low Power Dissipation: 200mW max

General Description

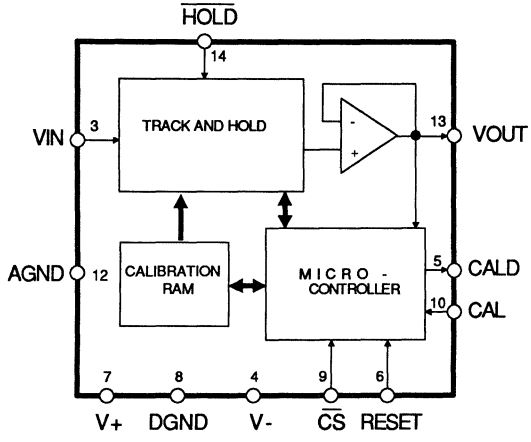
The CS3112 is a high speed track and hold with full 12-bit accuracy. It is completely self-contained, including hold capacitor, output buffer and calibration circuitry.

Aperture jitter of 100ps and maximum acquisition time of 1us to 0.01% provide excellent dynamic performance. On-chip hold capacitors limit droop to 0.001uV/us, and first order leakage compensation minimizes droop over the full operating temperature range.

Unique calibration circuitry limits all internal dynamic and dc errors to less than 700uV, guaranteeing 12-bit accuracy over time and temperature. Advanced CMOS fabrication insures low power consumption and increased reliability.

The CS3112 can be controlled and monitored through its microprocessor interface, or can operate independently.

ORDERING INFORMATION: Page 26



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, Texas 78760
(512)445-7222 TWX:910-874-1352

ANALOG CHARACTERISTICS

(T_A = 25°C, V+ = +5.0V, V- = -5.0V, R_L = 10KΩ, C_L = 50pF, unless otherwise specified)

Parameter*	CS3112-J,K min	CS3112-J,K typ	CS3112-J,K max	CS3112-A,B min	CS3112-A,B typ	CS3112-A,B max	CS3112-S,T min	CS3112-S,T typ	CS3112-S,T max	Units
Specified Temperature Range		0 to +70			-40 to +85			-55 to +125		°C
Accuracy										
Total Offset (Note 1) 25°C to T_{max}			± 0.7			± 0.7			± 0.7	mV
25°C to T_{min}			± 0.7			± 0.7			± 1.0	mV
Offset Drift (Note 2) T_{min} to T_{max}		±0.020			±0.025			±0.030		mV/°C
Tracking Offset			±20			±20			±20	mV
Nonlinearity 25°C		±0.4	±0.5		±0.4	±0.5		±0.4	±0.5	mV
(Note 3) T_{min} to T_{max}		±0.4			±0.4			±0.4		mV
Gain Error T_{min} to T_{max}		±0.01			±0.01			±0.01		% FS
Dynamic Characteristics										
Acquisition Time -J,A,S		1.5	2.0		1.5	2.0		1.5	2.0	us
(6V step to 0.01%) -K,B,T		0.9	1.0		0.9	1.0		0.9	1.0	us
Acquisition Time -J,A,S		1.0			1.0			1.0		us
(6V step to 0.1%) -K,B,T		0.5			0.5			0.5		us
Track to Hold Settling to 0.01%		0.5	0.8		0.5	0.8		0.5	0.8	us
Aperture Time		20			20			20		ns
Aperture Time Matching (Note 4)		2			2			2		ns
Aperture Jitter		100			100			100		ps
Droop Rate 25°C		±0.001	±0.1		±0.001	±0.1		±0.001	±0.1	uV/us
T_{min} to T_{max}			±0.6			±1.0			±5.0	uV/us
Analog Input										
Large Signal Bandwidth (6V p-p Input)		2.0			2.0			2.0		MHz
Small Signal Gain Bandwidth (60mV p-p Input)		2.5			2.5			2.5		MHz
Input Impedance (dc)		100			100			100		MΩ
Input Capacitance		5			5			5		pF
Input Bias Current		100			100			100		pA
Analog Output										
Noise (Note 5) Track Mode		50			50			50		uV_{rms}
Hold Mode		33			33			33		uV_{rms}
Power Supplies										
Supply Currents Positive		13	20		13	20		13	20	mA
Negative		−13	−20		−13	−20		−13	−20	mA

*Refer to Error Definitions on page 25.

Specifications are subject to change without notice.

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see note 5).

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies: Positive	V+	4.5	5.0	5.5	V
Negative	V-	- 4.5	−5.0	−5.5	V
Analog Input Voltage:	V_{IN}	- 3.0	-	3.0	V

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; V+ = 5V±10%; V- = -5V±10%)

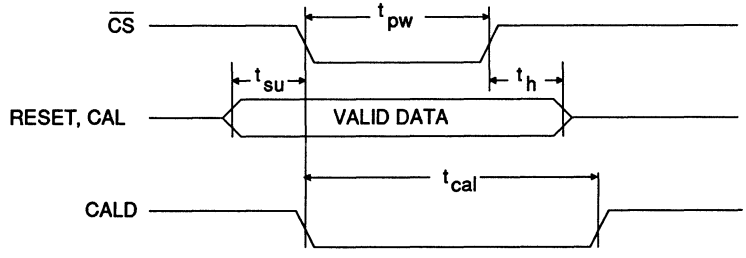
All measurements below are performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	1.7	-	V
Low-Level Input Voltage	V_{IL}	-	1.6	0.8	V
High-Level Output Voltage (Note 6)	V_{OH}	V+ - 1.0V	-	-	V
Low-Level Output Voltage, Iout=1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	10	uA

SWITCHING CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; V+ = 5V±10%; V- = -5V±10%)

Parameter	Symbol	Min	Typ	Max	Units
RESET, CAL to $\overline{CS}$ Setup Time	t_{su}	20	10	-	ns
$\overline{CS}$ to RESET, CAL Hold Time	t_h	5	1	-	ns
$\overline{CS}$ Pulse Width	t_{pw}	100	50	-	ns
$\overline{CS}$ Low and CAL High to CALD High	t_{cal}	-	4	10	ms

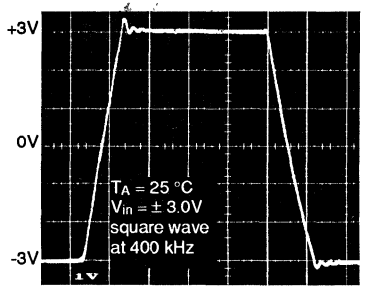
Notes:
1. Applies after calibration at any temperature within the specified temperature range.
2. Applies over specified temperature range without recalibration since calibration at 25°C.
3. Applies over the input voltage range of -3V to +3V.
4. Part to part.
5. Total noise from dc to 1MHz.
6. All voltages with respect to ground.
7. I_{out} = -100µA. This specification guarantees TTL compatability (VOH = +2.4V @ I_{out} = -40µA).



CS3112 Timing Diagram

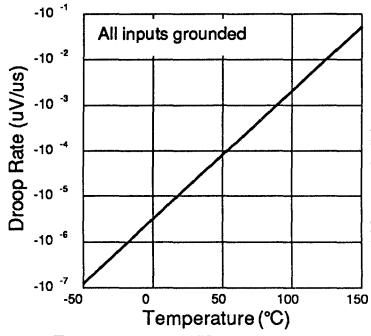
TYPICAL PERFORMANCE CHARACTERISTICS

(V+ = +5.0V, V- = -5.0V)

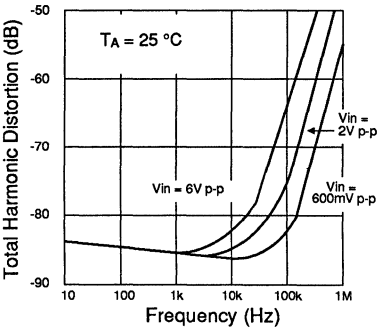


500 ns/div.

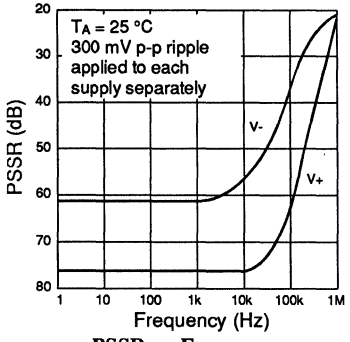
Full Scale Acquisition



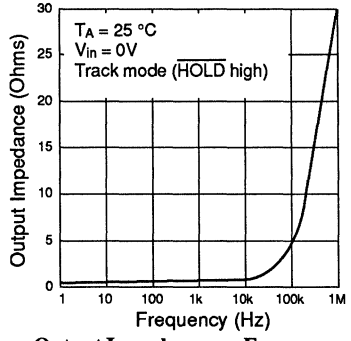
Droop Rate vs. Temperature



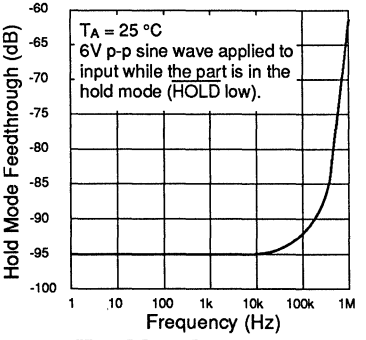
Distortion vs. Frequency



PSSR vs. Frequency



Output Impedance vs. Frequency



Hold Mode Feedthrough vs. Frequency

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, All voltages with respect to ground).

Parameter	Symbol	Min	Max	Units
DC Power Supplies: Positive	V+	−0.3	6.0	V
Negative	V-	0.3	−6.0	V
Input Current, Any Pin Except Supplies (Note 8)	I_{IN}	-	±10	mA
Analog Input Voltage	V_{INA}	V- - 0.3	V+ + 0.3	V
Digital Input Voltage	V_{IND}	-0.3	V+ + 0.3	V
Ambient Operating Temperature	T_A	-55	125	°C
Storage Temperature	T_{STG}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Note: 8. Transient currents of up to 100mA will not cause SCR latch-up.

General Description

The CS3112 consists of a complete track-and-hold amplifier with on-chip hold capacitor, an output buffer, and calibration circuitry. Use of an on-chip buffer isolates the track-and-hold amplifier from load conditions for optimal performance, and the calibration circuitry nulls out error sources. The CS3112 requires no external components or manual trims of any kind to achieve true 12-bit performance.

The CS3112 can be controlled through its on-board microprocessor interface, or can be operated independently. Unique auto-calibration circuitry nulls any dynamic or dc error introduced between the analog input pin and the buffer's output. The CS3112 thereby guarantees true 12-bit accuracy over time and temperature.

Calibration

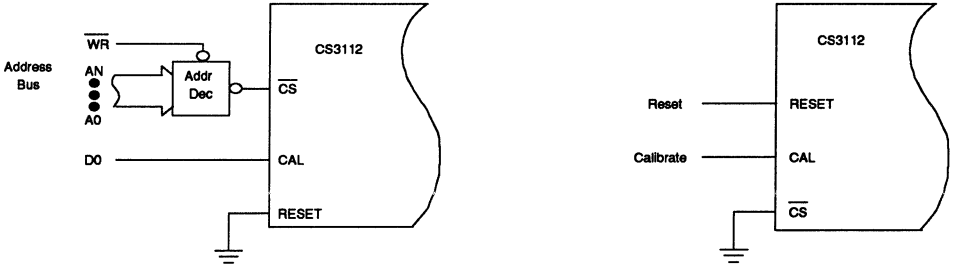
The CS3112 features on-chip measurement circuitry and digital intelligence capable of calibrating to full 12-bit accuracy. In the calibration mode, an internal microcontroller and special nulling circuitry reduce all errors at the VOUT pin to less than ±700µV. The controller disconnects the input signal and switches a known reference voltage (AGND) to the input of the track-and-hold amplifier. This voltage is captured on the internal hold capacitor, and a DAC is adjusted to remove any error. Thus, all internal errors, including dc offset and dynamic errors due to charge injection (hold pedestal), are trimmed to 12-bit accuracy (732µV is 1/2 LSB at 12 bits with a ±3V input signal). During tracking, there may be up to ±20mV of offset.

At power-up, the user must calibrate the device. Calibration is achieved by bringing the CAL input high with $\overline{CS}$ low. (In the stand-alone mode, $\overline{CS}$ is grounded, so only the CAL pin needs to be pulsed.) Calibration can be similarly initiated during operation at any time, thus insuring accuracy under any conditions.

During the calibration cycle (which takes about 4ms to complete) the CALD pin remains low. During this period, any load on VOUT must remain constant; otherwise, errors could be introduced which might affect accuracy. Another calibration cannot take place until CAL has first been latched low by $\overline{CS}$ and then latched high again. If a new calibration is initiated before the current calibration is finished, the CS3112 will complete the current calibration before initiating the new one.

Digital Interface

The CS3112 includes a digital interface designed for maximum flexibility. In a microprocessor-controlled application, the $\overline{CS}$ control input is



a. MPU-Controlled Operation

b. Independent Operation

Figure 1. CS3112 Control Connections

usually derived from a decoded address as well as write and strobe signals from the control bus (see Figure 1a). Calibration initiation thereby involves writing to the CS3112's address using a data bit to control CAL. For microprocessor-independent operation, $\overline{CS}$ is tied low and the digital inputs are controlled by externally-latched signals (see Figure 1b).

The CS3112's CALD output can be used to generate an interrupt indicating that calibration has been completed. Alternatively, calibration status can be polled in software by connecting CALD to the data bus via a three-state buffer.

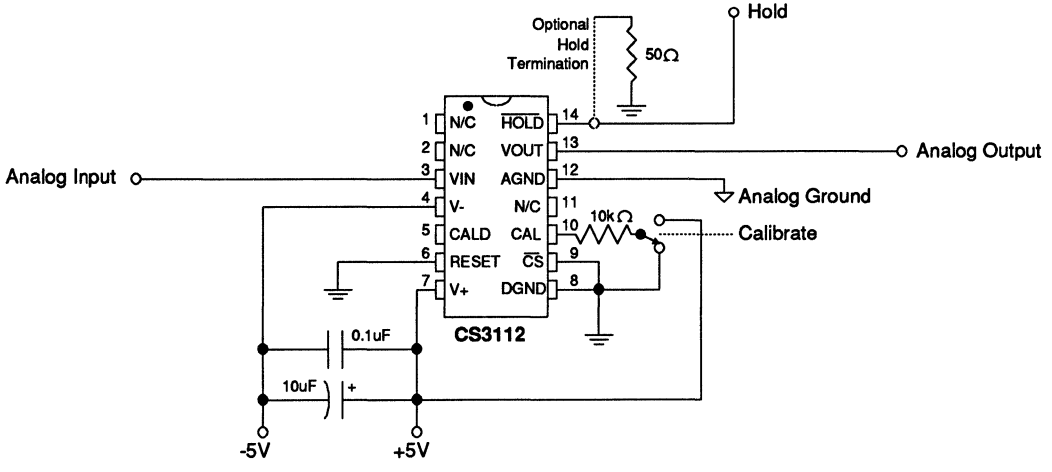
Reset

The CS3112 includes a reset function which guarantees a predictable state (CAL low) after power-up. The CS3112 is reset when the RESET pin is high and $\overline{CS}$ is low simultaneously. Since this function can be emulated in software by writing a 0 to the CS3112 when under microprocessor control, it is mainly useful when operating independently (Figure 1b). It is not necessary to reset before calibration, but a reset command at power-up will insure that the CS3112 does not come up calibrating.

Power Supplies

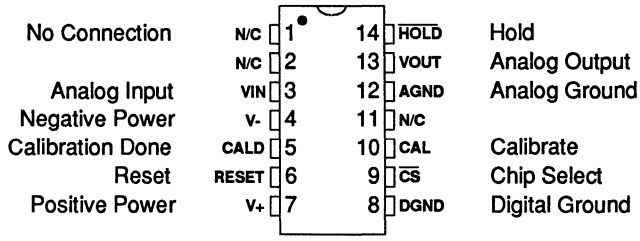
The CS3112 uses the analog ground voltage (AGND) only as a reference voltage. No signal or dc power currents flow through the AGND connection, and it is completely independent of DGND. Both the analog input and output are referenced to to the AGND pin internally, and this pin needs to be at the same potential as the entire system's analog ground plane to minimize offset errors induced by noise between the AGND pin and the system analog ground.

Decoupling should be performed between the V+ pin and the V- pin using a 0.1µF ceramic cap. If significant low frequency noise is present on the supplies, a 10µF tantalum capacitor is recommended in parallel with the 0.1µF capacitor. *The decoupling capacitors should be placed as close to the CS3112's power supply pins as possible.*



Simple Test Connections - Independent Operation

PIN DESCRIPTIONS



Analog Input and Output

VIN - Analog Input, PIN 3
Analog input to the track-and-hold amplifier.

VOUT - Analog Output , PIN 13
Buffered output from the track-and-hold.

Power Supplies

V+ - Positive Power, PIN 7
Most positive supply voltage. Nominally +5 volts.

V- - Negative Power, PIN 4
Most negative supply voltage. Nominally -5 volts.

DGND - Digital Ground, PIN 8
Digital ground.

AGND - Analog Ground, PIN 12
Analog ground reference.

8

Digital Inputs and Outputs

$\overline{\text{HOLD}}$ - Hold, PIN 14

A falling transition on this pin switches the track-and-hold amplifier to the hold mode. When brought high, the track-and-hold is switched to the track mode, and acquires and then tracks the input signal.

CAL - Calibrate, PIN 10

When taken high with $\overline{\text{CS}}$ low, initiates a full internal calibration.

CALD - Calibration Done, PIN 5

Indicates calibration status. After reset, if CALD is high the device has finished calibration. Returns low upon reset or the initiation of calibration.

$\overline{\text{CS}}$ - Chip Select, PIN 9

Enables the RESET and CAL digital inputs.

RESET - Reset, PIN 6

Sets CAL low internally when held high and $\overline{\text{CS}}$ is strobed low.

ERROR DEFINITIONS

Total Offset - The difference between the analog input voltage and the voltage at the output pin after the hold command has been issued and all transients have settled. Applies only in the hold mode, not while tracking the analog inputs. Includes all internal offsets, including those due to charge injection (hold pedestals). Units in millivolts.

Nonlinearity - The deviation from a straight line on the plot of output vs input. Nonlinearity is specified as the change in *Total Offset* over the signal range of -3V to +3V. Units in millivolts.

Gain Error - Calculated as the difference between the errors resulting from a -3V and a +3V dc input signal, relative to a 6V input range. Units in percent of full scale.

Acquisition Time - The time required after the negation of the hold command ($\overline{\text{HOLD}}$ high) for the track-and-hold amplifier to reach its final value to within a specified error band (±0.01% or ±0.1%). This determines the minimum time allowed before reassertion of the hold command. Units in microseconds.

Track-to-Hold Settling - The time required after the hold command is given for the output buffer amplifier to reach its final value to within a specified error band (±0.01%). Includes switch delay (aperture) time. Units in microseconds.

Aperture Time - The delay after the hold command for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

Aperture Jitter - The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

Droop Rate - The change in the output voltage over time while in the hold mode. Units in microvolts per microsecond.

Large Signal Bandwidth - The frequency at which the output amplitude is 3dB below the input amplitude while tracking a full scale 6V p-p sine wave. Units in megahertz.

Small Signal Gain Bandwidth - The frequency at which the output amplitude is 3dB below the input amplitude while tracking a 60mV p-p sine wave. Units in megahertz.

Ordering Guide

Model	Acquisition Time	Temperature Range	Package
CS3112-JD	2.0µs	0 to +70°C	14-Pin Cerdip
CS3112-KD	1.0µs	0 to +70°C	14-Pin Cerdip
CS3112-AD	2.0µs	-40 to +85°C	14-Pin Cerdip
CS3112-BD	1.0µs	-40 to +85°C	14-Pin Cerdip
CS3112-SD	2.0µs	-55 to +125°C	14-Pin Cerdip
CS3112-TD	1.0µs	-55 to +125°C	14-Pin Cerdip

INTRODUCTION

Ideal for adaptive filtering applications, a family of digitally programmable switched capacitor filters provides the user with complete software control over the filter response.

Virtually any audioband filter response of eighth order or below is obtained by writing digital configuration coefficients to on-chip registers through a standard microprocessor interface. The chip can also load itself by reading coefficients directly from memory. Accuracy of a filter response is typically within 1 percent of the calculated value (for corner frequencies) and dynamic range is a minimum of 72 dB. Bandwidth varies depending upon the transfer function implemented, but can extend from 0 to 50 kHz. Anti-aliasing, smoothing and input gain control are supported with on-chip uncommited operational amplifiers.

The user is provided instant feedback on filter performance in his system by the Crystal-ICE filter development system. The PC-based design tool includes filter synthesis software and an in-circuit hardware emulator.

USER'S GUIDE

Device:	CS7008	CS7004
Frequency Range	5Hz to 20kHz	5Hz to 20kHz
Dynamic Range	72 dB	72 dB
Maximum Filter Order	8th	4th
Power Dissipation	180 mW	100 mW
Package	28 pin DIP	28 pin DIP

CONTENTS

Semiconductor Corporation

CS7008

Digitally Configurable Universal Filter

Features

- Digitally Programmable to Obtain Even-Order Audio-Band Filters of Eighth Order or Below
- Dynamically Configurable for Adaptive Filtering Applications
- Microprocessor Compatible Digital Interface
- Two User Configurable Op Amps for Antialiasing and Smoothing
- Supported by CRYSTAL-ICE Filter Development System
- Low Power CMOS

General Description

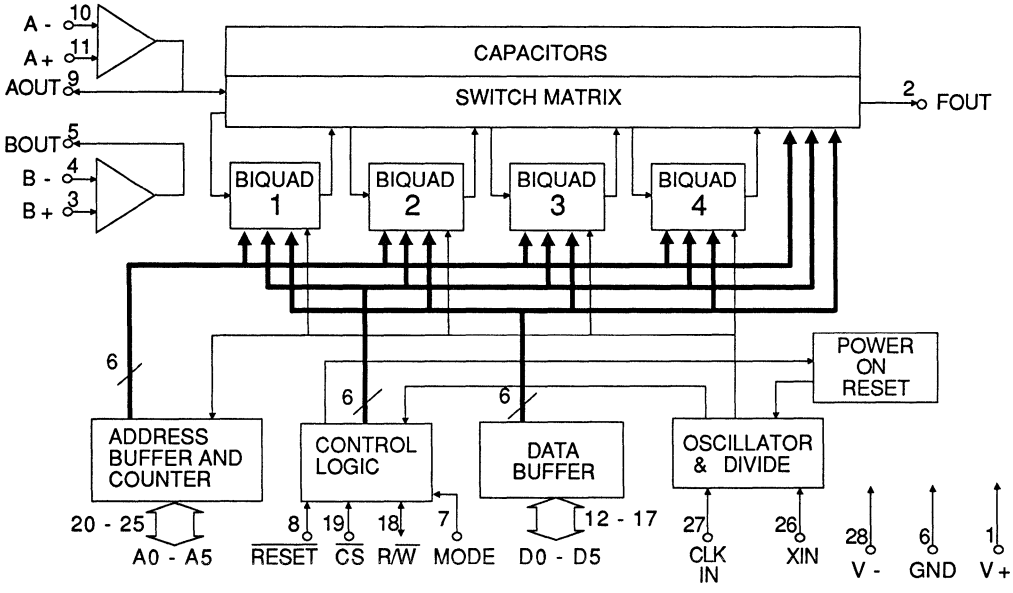
The CS7008 is fabricated in CMOS using Crystal's SMART Analog™ design techniques. It is a digitally configurable switched capacitor filter capable of providing the system designer with virtually any precisely defined, audio-band, even-order filter response of eighth order or below. An efficient microprocessor interface permits in-system reconfiguration of the filter response and cost-effective system design. Access to two operational amplifiers is also provided for use as antialiasing and smoothing filters if desired.

System design is supported by the CRYSTAL-ICE Filter Development System. The development system consists of hardware and software for use with an IBM PC and provides in-circuit emulation of the CS7008.

ORDERING INFORMATION

CS7008-P - 28 Pin Plastic,	0°C to 70°C
CS7008-ID - 28 Pin CerDIP,	-40°C to +85°C
CS7008-MD-28 Pin CerDIP,	-55°C to +125°C

Block Diagram



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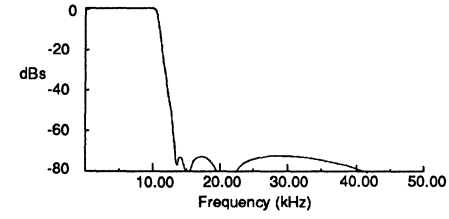
Preliminary Product Information | *This document contains data for a new product. Crystal Semiconductor reserves the right to modify this product without notice.*

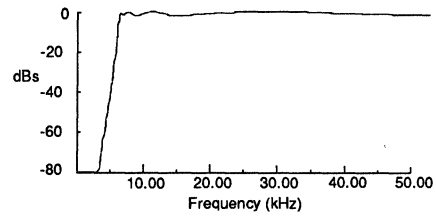
Crystal Semiconductor Corporation
P.O. Box 17847, Austin, Texas 78760
(512)445-7222 TWX:910-874-1352

TYPICAL FREQUENCY RESPONSE

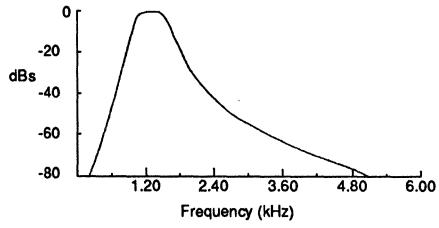
The CS7008 is completely software programmable for type, order and response curve of the desired filter. Here are some examples:



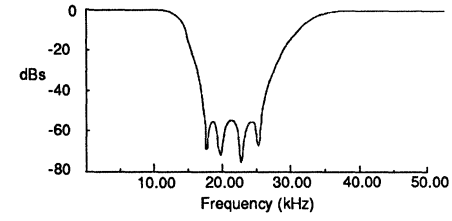
Elliptic Low-Pass



Chebyshev I High-Pass



Butterworth Bandpass



Chebyshev II Band-Stop

GENERAL INFORMATION ON FILTER CHARACTERISTICS

Due to the universal nature of the CS7008, most filter specifications are transfer function dependent to some degree. It is recommended that the user characterize the device for the transfer function or functions to be implemented. Since the matching of filter characteristics from device to device is excellent, filter characteristics specific to a transfer function will apply to all CS7008's within the limits indicated in the section on typical device performance. Stability of filter characteristics over temperature is also excellent, so performance specific to a particular transfer function will vary little over the full temperature range specified.

ANALOG CHARACTERISTICS-FILTER (T_A = 25° C, V+ = 5.0V, V- = -5.0V, GND = 0V)

Transfer Function Dependent Specifications..

Parameter		Symbol	Min	Typ	Max	Units
Dynamic Range	(Note 1)		72			dB
Output Noise	(Note 1)				480	uV rms
Signal to THD AIN = 6.75 kHz, Vi= ±2.75 V_{peak}	(Note 1)		50	55		dB
Device to Device Phase Matching	(Note 1)			±3		Degrees
Device to Device Gain Matching	(Note 1)			±1		dB
DC Output Offset	(Note 1)	V_{oo}		TBD		
Power Supply Rejection Ratio	(Note 1)			TBD		dB
Filter Cutoff Frequency (E damping)			1.0	20,000	TBD	Hz
Filter Cutoff Frequency (F damping)			1.0	25,000	TBD	Hz
Input Voltage Range		V_I	- 3.0		3.0	V_{peak}
Output Voltage Swing THD = -50 dB		V_o	- 2.75		2.75	V_{peak}

Note: 1. All specifications in this section apply to the CS7008 configured with an 8th order Chebyshev II band-pass transfer function (-1 dB cutoff frequencies of 6.4 kHz and 13 kHz, f osc = 1.038 MHz and fs = 173 kHz, E damping). Measurement bandwidth: 10 Hz to 30 kHz. See appendix for detailed capacitor values.

Typical Performance Characteristics:

The final production revision of the CS7008 is in the process of being characterized as this data goes to press. Characterization is being done for both 8th order transfer functions and for a single biquad. Contact the Factory for the latest information.

ANALOG CHARACTERISTICS - AUXILIARY AMPLIFIERS

(T_A = 25° C, V+ = 5.0V, V- = -5.0V, GND = 0V)

Parameter		Symbol	Min	Typ	Max	Units
DC Open Loop Gain	(Note 2)	A_{VOL}	-	78	-	dB
Gain Bandwidth Product	(Note 2)	G_{BW}	-	1.0	-	MHz
Input Offset Voltage		V_{IO}	-	25	-	mV
Output Swing	(Note 2)	$V_{O(P-P)}$	- 3.5	-	3.5	V_{peak}
Output Short Circuit Current		I_{OS}	-	0.5	-	mA
Common Mode Range	(Note 2)	V_{CM}	- 3.5	-	3.5	V_{peak}
Common Mode Rejection Ratio	(Note 3)	CMRR	-	60	-	dB
Slew Rate	(Note 4)	SR	-	2.0	-	V/us

Notes: 2. R_L = 1 MΩ.
3. fo = 60 Hz.
4. R_L = 1 MΩ, C_L = 20 pF.

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ANALOG CHARACTERISTICS-FILTER (T_A = 25° C, V+ = 5.0V, V- = -5.0V, GND = 0V)

Specifications independent of filter order and transfer function.

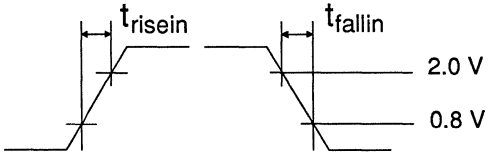
Parameter	Symbol	Min	Typ	Max	Units
Power Consumption			180		mW
Clock Feedthrough			40		mV_{p-p}

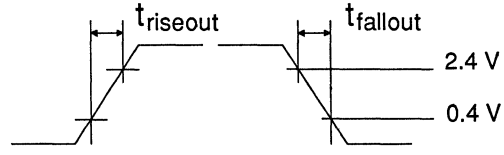
SWITCHING CHARACTERISTICS

(T_A = 25° C, V+ = 5.0V, V- = -5.0V, GND = 0V)

Parameter		Symbol	Min	Typ	Max	Units
Output Rise Time	(Note 5)	$t_{riseout}$	-	15	20	ns
Output Fall Time	(Note 5)	$t_{fallout}$	-	15	20	ns
Input Rise Time		t_{risein}	-	20	1000	ns
Input Fall Time		t_{fallin}	-	20	1000	ns

Note: 5. 50 pF load (includes probe and jig capacitance).



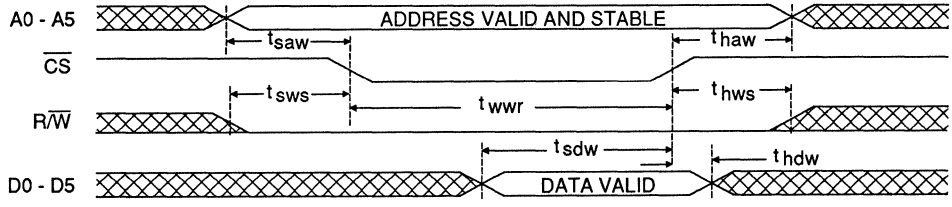


SWITCHING CHARACTERISTICS Writing to the CS7008

.(T_A = 25° C, V+ = 5.0V, V- = -5.0V, GND = 0V).

Parameter		Symbol	Min	Typ	Max	Units
Address-Write Set-Up Time		t_{saw}	100	-	-	ns
Address-Write Hold Time		t_{haw}	0	-	-	ns
Write Pulse-Width Low		t_{wwr}	200	-	-	ns
Data-Write Set-Up Time	(Note 6)	t_{sdw}	200	-	-	ns
Data-Write Hold Time		t_{hdw}	0	-	-	ns
Write-Chip Select Set-Up Time		t_{sws}	0	-	-	ns
Write-Chip Select Hold Time		t_{hws}	0	-	-	ns

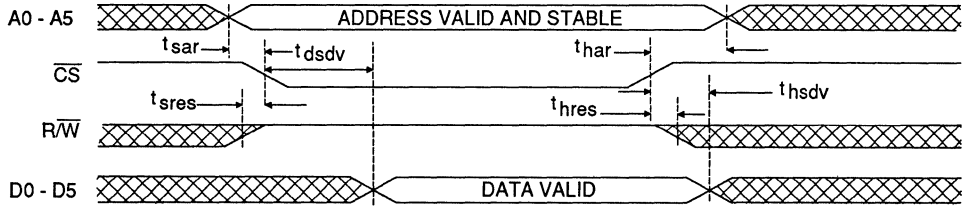
Note: 6. Minimum time required for data to be valid while write pulse is low.



SWITCHING CHARACTERISTICS Reading from the CS7008

.(T_A = 25° C, V+ = 5.0V, V- = -5.0V, GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
Address-Read Set-Up Time	t_{sar}	0	-	-	ns
Address-Read Hold Time	t_{har}	0	-	-	ns
Read Enable to Read Stable Hold Time	t_{sres}	0	-	-	ns
Read Enable to Read Stable Hold Time	t_{hres}	0	-	-	ns
Read Strobe to Data Valid Delay	t_{dsdv}	350	-	-	ns
Read Strobe Data Valid Hold Time	t_{hsdv}	0	-	-	ns

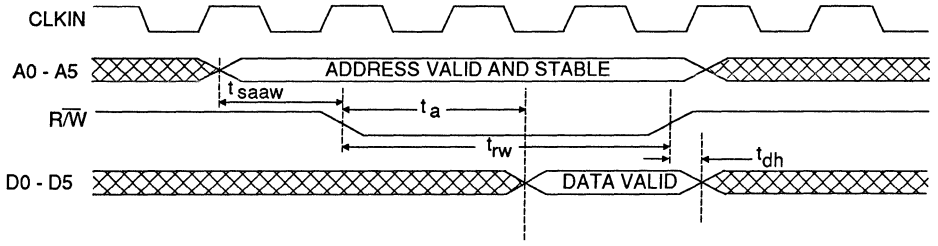


SWITCHING CHARACTERISTICS Reading from external ROM

(T_A = 25° C, V + = 5.0V, V- = -5.0V, GND = 0V, fOSC = 1.5 MHz, CLKDIV = 1)

Parameter		Symbol	Min	Typ	Max	Units
Auto-Address to Write Set-Up	(Note 7)	t_{saaw}	667	-	-	ns
R/W Pulse Width	(Note 8)	t_{rw}	-	1667	-	ns
Data Valid After R/W Goes High		t_{dh}	0	-	-	ns
ROM Access Time	(Note 9)	t_a	-	-	1133	ns

Notes: 7. Time equal to 1 clock cycle.
8. Time equal to 2.5 clock cycles.
9. Maximum allowable ROM output delay (Time equal to 1 clk cycle + (1 clk cycle - 200 ns)).



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CLOCK SPECIFICATIONS (T_A = 25° C, V+ = 5.0V, V- = -5.0V, GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
Oscillator Frequency Range	f_{OSC}		TBD	4.0	MHz
Oscillator Duty Cycle		40		60	%
Sampling Frequency Range	f_S			250	kHz

DIGITAL CHARACTERISTICS (T_A = 25° C, V+ = 5.0V, V- = -5.0V, GND = 0V).

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	Except Pin 7	V_{IH}	2.0	-	-	V
	Pin 7 only		70% V+	-	-	V
Low-Level Input Voltage	Except Pin 7	V_{IL}		-	0.8	V
	Pin 7 only		-	-	30% V+	V
High-Level Output Voltage	(Note 10)	V_{OH}	2.4	-	-	V
Low-Level Output Voltage	(Note 10)	V_{OL}	-	-	0.4	V
Input Leakage Current			-	-	10	uA
Three-State Leakage Current			- 10	-	10	uA

Note: 10. Digital outputs will output CMOS logic levels into a CMOS load.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Units
Positive Supply		V+	4.75	5.0	5.25	Volts
Negative Supply		V-	- 4.75	- 5.0	- 5.25	Volts
Ambient Operating Temperature	-P -ID -MD	T_A	0 -40 -55	-	70 +85 +125	^oC

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
DC Supplies	Positive	V+	- 0.3	+6.0	Volts
	Negative	V -	+ 0.3	-6.0	
Input Voltage		V_{in}	V - - 0.3	V+ + 0.3	Volts
Input Current, Any Pin	(Note 11)	I_{in}	-	10	mA
Power Dissipation		P_D	-	500	mW
Ambient Operating Temperature	-P	T_A	0	70	°C
	-ID		-40	+85	
	-MD		-55	+125	
Storage Temperature		T_{stg}	- 65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation of the part is not guaranteed at these extremes.

Note: 11. Transient currents of up to 100mA will not cause SCR latch up.

9

THEORY OF OPERATION

The CS7008 is a programmable universal filter consisting of four separate biquadratic filter sections, any one of which is independently programmable to obtain high-pass, low-pass, band-pass, band-reject, notch, high-pass notch, low-pass notch, or all-pass filter functions. Almost any audio band, even order (eighth order or below) filter can be obtained. The biquad filter sections can be cascaded using 1, 2, 3, or 4 sections to achieve 2nd, 4th, 6th, or 8th order filters. The CS7008 filter configurations can be dynamically controlled by a microprocessor or, in the self-program mode, a fixed set of filter coefficients can be read by the CS7008 from an external ROM.

Filter design is supported by the CRYSTAL-ICE (In Circuit Emulator) Filter Development System. The CRYSTAL-ICE package includes software that generates the coefficients for the CS7008. The user specifies the filter parameters in terms of transition frequencies and their respective magnitudes. The system provides an interface through which coefficients can be down-loaded to an in-circuit CS7008. CRYSTAL-ICE supports development of low-pass, high-pass, band-pass, and band-stop filters. Butterworth, Chebyshev I and II, and elliptic (Cauer) filter responses are attainable.

Configuration Information

The CS7008 must be loaded with valid data before the filter will function. The data consists of a clock divide code, (cdc), capacitor coefficients, a configuration code for each biquad required, (conf), and a biquad arrangement code, (barr). Information on each of these parameters is provided in subsequent sections. The Address Map shows how the data must be arranged for loading into the CS7008.

Clock

As with any sampled data system, the maximum signal frequency that can be effectively sampled, processed, and reconstructed is the Nyquist frequency, fS/2. As filter cutoff frequencies approach the Nyquist frequency, several things happen:

a) Sin(x)/x distortion increases and requires compensation,

b) Antialiasing and reconstruction filter complexity increases,

c) CS7008 coefficients are larger and coefficient truncation effects are minimized.

To minimize the unfavorable effects of sin(x)/x distortion, and reduce antialiasing and reconstruction filter complexity, the sampling frequency, fS, should be at least 10 times higher than the signal's highest frequency of interest. Crystal recommends an oversampling ratio of 20 to 30. Such oversampling ratios usually provide acceptable capacitor values, negate sin(x)/x distortion, and reduce antialiasing filter complexity.

When an acceptable fS for a particular application has been determined, the required oscillator frequency, fOSC, can be derived from Equation 1.

$$fosc = fs \times 6 \times CLKDIV$$

Equation 1.

The maximum sampling frequency for the CS7008 is 250 kHz. CLKDIV corresponds to the clock divide code, (cdc), which is loaded into the memory of the CS7008 and sets an internal clock divide. If the oscillator frequency exceeds 1.5 MHz, CLKDIV must be set so fS does not exceed 250 kHz. Permissible CLKDIVs are; 1, 2, 4, 8, 16, 32, 64, and 128. The clock divide code is loaded at address 30 (1E hex). See

Table 2 for more information. Note that for a given filter configuration, a change in fS will result in a proportional change in the filter's pass band frequencies, but the filter Q will remain the same.

Signal Input and Output

To achieve optimum performance, the largest input signal amplitudes should be adjusted to approach the device's maximum input level. Larger input signals take advantage of the dynamic range of the device, thereby maximizing the signal to noise ratio. An antialiasing filter may be required at the input. The input op amp (op amp A) can be used to perform this low-pass filtering function.

The output signal is a 100% duty cycle PAM (staircase) signal, constructed at the sampling frequency, fS. The uncommitted op amp (op amp B) can be configured as a smoothing filter for the output signal.

Data Input/Output

The CS7008 contains six address lines, A0-A5, and six data lines, D0 -D5. Since the data bus is six bits, all references to a "byte" refer to a six bit byte. Some of the bytes needed to configure the CS7008 do not use all six bits. In these cases the unused bits are the most significant bits and are considered "don't cares" (x) when written. When reading from the CS7008, unused bits should be masked off. The CS7008 can be loaded by a microprocessor or from external ROM by an automatic "self-programming" routine contained in the CS7008. The MODE pin determines whether the CS7008 is in the microprocessor mode (MODE = GND) or the self-programming mode (MODE = V+). In the self-programming mode, the CS7008 sequentially addresses an external ROM where filter coefficients are stored. The R/$\overline{W}$ pin is used to enable the ROM's outputs and an internally generated strobe clocks the data into the CS7008's registers.

In the microprocessor mode, a microprocessor controls memory access. When R/$\overline{W}$ is at logic 0, data is clocked into the memory of the CS7008 on the negative transition of $\overline{CS}$ and is latched on the positive transition of $\overline{CS}$.

Data may also be read from the memory of the CS7008. This is accomplished by holding the read/write control pin, R/$\overline{W}$, at logic 1 and setting the chip select pin, $\overline{CS}$, to logic 0 as a strobe. Refer to the Timing Diagrams of Figures 1, 2 and 3 for details.

Biquads

Each biquad consists of two capacitor arrays which are connected to two op amps through a series of switches, as shown by the block

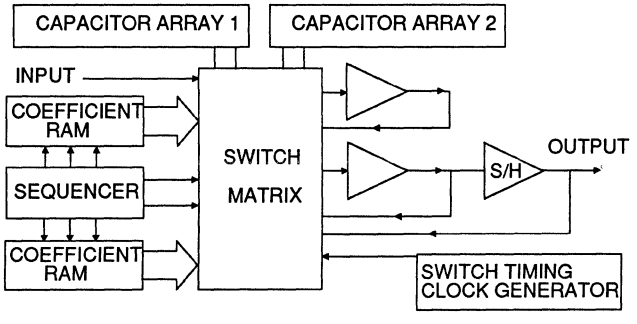

Figure 5. - Block Diagram of a Single Biquad

diagram in Figure 5. The capacitor coefficients determine the configuration of the capacitor array's switch matrix. As a signal is switched through a biquad, the desired value of capacitance is selected by the appropriate configuration of the switch matrix. After a charge has been switched through the selected capacitor, the capacitor array is grounded, discharging the array to prepare it for the next switch configuration.

Each biquad section is capable of implementing z-domain biquadratic transfer functions of the form:

$$H(z) = \frac{\gamma + \varepsilon z^{-1} + \delta z^{-2}}{1 + \alpha z^{-1} + \beta z^{-2}}$$

Equation 2.

The circuit representing the general active-SC biquad used in the CS7008 is shown in Figure 6. The z-domain transfer function for this circuit is:

$$\frac{V_{out}}{V_{in}} = \frac{Az^{-1}(G-Hz^{-1}) + D(1-z^{-1})(I-Jz^{-1})}{Az^{-1}(C+E-Ez^{-1}) + D(1-z^{-1})(F+B-Bz^{-1})}$$

Equation 3.

Note that Equation 3 is equivalent to Equation 2.

Equation 3 is solved to obtain the coefficients A through J. For optimal dynamic range, the signal level of both biquad op amps is important. Equation 4 gives the transfer function from the input to the output of the first op amp.

$$\frac{V'}{V_{in}} = \frac{(I-Jz^{-1})(C+E-Ez^{-1}) - (G-Hz^{-1})(F+B-Bz^{-1})}{Az^{-1}(C+E-Ez^{-1}) + D(1-z^{-1})(F+B-Bz^{-1})}$$

Equation 4.

The dynamic range of both biquad op amps should be maximized by modifying capacitors A and D so that the maximum voltage swing is achieved through the biquad (i.e., both op amps swing 5.5 V p-p, max).

Capacitor groups (C, D, E, G, H) and (A, B, F, I, J) can be independently scaled without affecting the transfer function. The capacitors are programmed to 11 bit resolution allowing equivalent capacitor values to range from 0 to 2047. In the CS7008, capacitors B and D are fixed at equivalent values of 1024; therefore, the

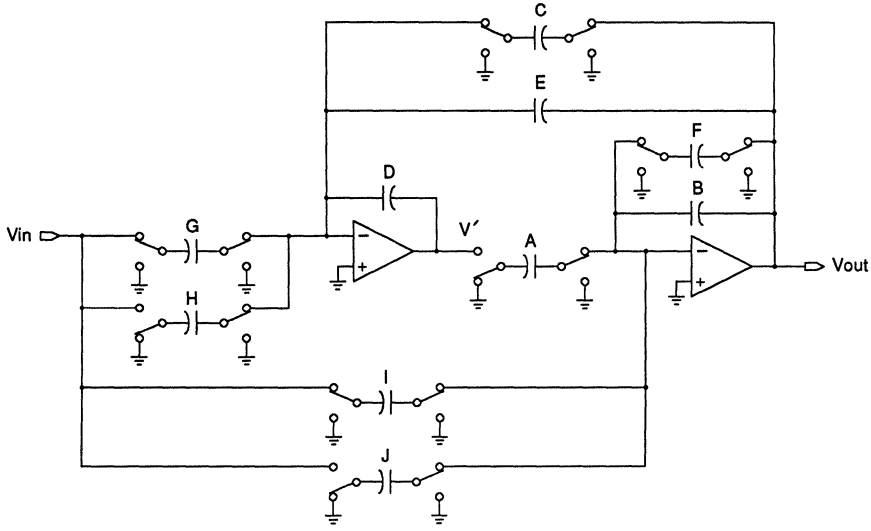

Figure 6. - General Active Switched Capacitor Biquad Filter

two capacitor groups listed above must be normalized so that B and D are 1024.

If any of the equivalent capacitor values of the first group, (C, D, E, G, H), exceed the maximum value of 2047 when normalized, A and D can be scaled to achieve the transfer function. This dynamic range scaling causes V' to increase with respect to V. In this case, the input signal to the filter must be limited proportionately to prevent clipping at the output of the first op amp.

Figure 7 is an excerpt of Figure 6 showing the programmable capacitor A, in detail. All programmable capacitors are of this form. The following illustrates how to program a capacitor. In Figure 7, the numbers above the individual capacitors that make up A are the unit capacitor values (1024, 512, 256, etc.). The numbers below the capacitors are the individual bit positions (b10 = most significant bit, b0 = least significant bit). Figure 7 shows the switches programmed for a binary value of 10010001101 which, when adding the unit capacitor values, gives capacitor A the equivalent value of 1165 (= 1024 + 128 + 8 + 4 + 1). The equivalent value for a capacitor is the binary value, converted to decimal.

The 11 bit capacitor coefficients must be split into two bytes to load the CS7008. To load this capacitor, A, into biquad 1, the lower five bits, 01101 (decimal 13), would be loaded at address location 0 and the upper six bits, 100100 (decimal 36), would be loaded at address location 1. The Address Map lists all the address locations for all the capacitors in each biquad.

Possible configurations of the biquads in the CS7008 allow either E or F damping, and J or H input capacitors. Each biquad has a configuration byte, "conf", that determines how the memory locations E/F, CE/C, and J/H are to be used.

One biquad configuration requires additional consideration. If E damping is selected for a particular biquad, the value of the E capacitor must be added to the C capacitor for the biquad to function properly. For this case, the C capacitor is referred to as "CE", and is loaded into the memory location for CE/C (=CE). The value of the E capacitor must still be loaded into

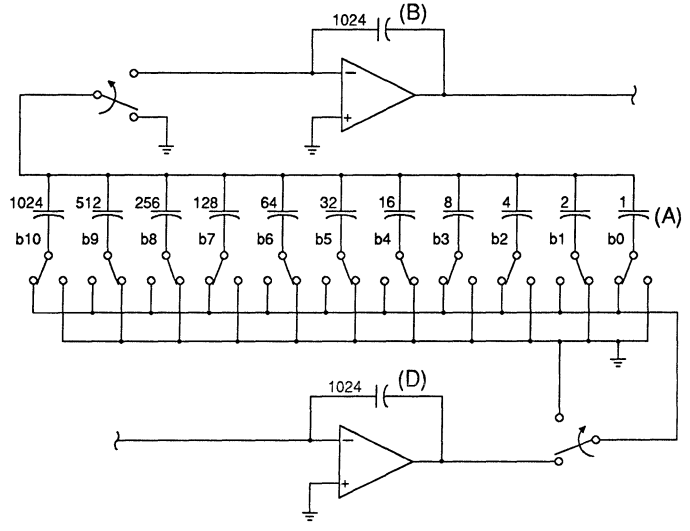

Figure 7. - Equivalent Capacitor Arrangement

the E/F (=E) memory location. No special consideration is necessary for F damping, i.e., the values of C and F are loaded into locations for CE/C (=C) and E/F (=F) respectively. See Table 1 for more information on biquad configuration. For more information regarding the transfer function in Equation 3, consult the text, "Modern Filter Design" by M. S. Ghausi and K. R. Laker, published by Prentice-Hall.

Cascading Biquads (Biquad Arrangement Code)

The biquad sections can be cascaded allowing the user to define 2nd, 4th, 6th, or 8th order filters. Permissible biquad configurations are shown in Figure 4. The biquad arrangement code, barr, is an 11 bit word which determines which biquad sections are connected between the analog input and the analog output, FOUT. The arrangement code is divided into two bytes located at address 62, barr (low byte), and 63, barr (high byte). Valid barr codes are given in Table 3.

When developing higher order filters (fourth order and above), certain implementations require biquad section(s) with gains exceeding unity, even though the overall filter response does not have any gain. Excessive gain in one section could saturate the amplifiers, distorting the signal. In all cases, care must be taken in arranging biquad coefficient groups so signals do not clip. An example of this is a high Q, low-pass filter cascaded with a low Q, low-pass filter which has a lower cutoff frequency. In this situation, the biquad coefficient groups must be arranged so that the high gain of the high Q section(s) is preceded by the low Q, lower cutoff section(s) which attenuates the signal at those frequencies where gain is a problem in subsequent biquads. For filters of 6th order and below, the additional biquad(s) can be used in cascade for sin(x)/x compensation or phase linearization.

Op Amps

Two op amps are provided on the CS7008. The output of op amp A is connected to the biquad filter input. This op amp must be used for signal input and can be configured for antialiasing and input gain. Op amp B is uncommitted and can be applied as the user wishes.

Power Supplies

Typical power supplies are V+ = +5 volts, V- = -5 volts and GND = 0 volts. Since the device's analog and digital grounds share the same pin, this pin should be isolated from all other digital grounds whenever possible, to prevent noise from interfering with the analog circuitry. Always decouple the V- and V+ power supply pins to the analog ground (GND) with 0.1 µF ceramic capacitors. These capacitors should be situated as close to the device as possible.

High-Frequency Applications

Filter performance is specified for frequencies up to 20 kHz.

However, the CS7008 is capable of handling transfer functions for frequencies well in excess of 20 kHz.

ADDRESS MAP

ADDRESS binary	hex	dec	Biquad #	Capacitor or Code	byte	# of bits	Comments
000000	00	00	1	A	Low	5	
000001	01	01	1	A	High	6	
000010	02	02	1	E/F *	Low	5	
000011	03	03	1	E/F *	High	6	
000100	04	04	1	CE/C *	Low	5	CE - E Damping
000101	05	05	1	CE/C *	High	6	C-F Damping
000110	06	06	1	conf *		2	Configuration Byte
000111	07	07	. . . . .				Not Used
001000	08	08	1	J/H *	Low	5	
001001	09	09	1	J/H *	High	6	
001010	0A	10	1	I	Low	5	
001011	0B	11	1	I	High	6	
001100	0C	12	1	G	Low	5	
001101	0D	13	1	G	High	6	
001110	0E	14	. . . . .				Not Used
001111	0F	15	. . . . .				Not Used
010000	10	16	2	A	Low	5	
010001	11	17	2	A	High	6	
010010	12	18	2	E/F *	Low	5	
010011	13	19	2	E/F *	High	6	
010100	14	20	2	CE/C *	Low	5	CE - E Damping
010101	15	21	2	CE/C *	High	6	C-F Damping
010110	16	22	2	conf *		2	Configuration Byte
010111	17	23	. . . . .				Not Used
011000	18	24	2	J/H *	Low	5	
011001	19	25	2	J/H *	High	6	
011010	1A	26	2	I	Low	5	
011011	1B	27	2	I	High	6	
011100	1C	28	2	G	Low	5	
011101	1D	29	2	G	High	6	
011110	1E	30		cdc †		3	Clock Divide Code
011111	1F	31	. . . . .				Not Used

* Configuration byte determines which capacitor to use. See Table 1.

† See Table 2.

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ADDRESS MAP, CONT.

ADDRESS binary	hex.	dec.	Biquad #	Capacitor or Code	byte	# of bits	Comments
100000	20	32	3	A	Low	5	
100001	21	33	3	A	High	6	
100010	22	34	3	E/F *	Low	5	
100011	23	35	3	E/F *	High	6	
100100	24	36	3	CE/C *	Low	5	CE - E Damping
100101	25	37	3	CE/C *	High	6	C- F Damping
100110	26	38	3	conf *		2	Configuration Byte
100111	27	39	. . . . .				Not Used
101000	28	40	3	J/H *	Low	5	
101001	29	41	3	J/H *	High	6	
101010	2A	42	3	I	Low	5	
101011	2B	43	3	I	High	6	
101100	2C	44	3	G	Low	5	
101101	2D	45	3	G	High	6	
101110	2E	46	. . . . .				Not Used
101111	2F	47	. . . . .				Not Used
110000	30	48	4	A	Low	5	
110001	31	49	4	A	High	6	
110010	32	50	4	E/F *	Low	5	
110011	33	51	4	E/F *	High	6	
110100	34	52	4	CE/C *	Low	5	CE - E Damping
110101	35	53	4	CE/C *	High	6	C- F Damping
110110	36	54	4	conf *	Low	2	Configuration Byte
110111	37	55	. . . . .				Not Used
111000	38	56	4	J/H *	Low	5	
111001	39	57	4	J/H *	High	6	
111010	3A	58	4	I	Low	5	
111011	3B	59	4	I	High	6	
111100	3C	60	4	G	Low	5	
111101	3D	61	4	G	High	6	
111110	3E	62		barr †	Low	6	Biquad Arrangement
111111	3F	63		barr †	High	5	Biquad Arrangement

* See Table 1.

† See Table 3.

TABLE 1. - BIQUAD CONFIGURATION CODES: conf

D1	D0	J / H	E / F	CE / C	Comments
0	0	J	E	CE	J input cap. with E damping. CE = C + E *
0	1	J	F	C	J input cap. with F damping.
1	0	H	E	CE	H input cap. with E damping. CE = C + E *
1	1	H	F	C	H input cap. with F damping.

* See "Biquads" section for more information on CE/C.

TABLE 2. - CLOCK DIVIDE CODES: cdc

D2	D1	D0	cdc	CLKDIV
0	0	0	0	1
0	0	1	1	2
0	1	0	2	4
0	1	1	3	8
1	0	0	4	16
1	0	1	5	32
1	1	0	6	64
1	1	1	7	128

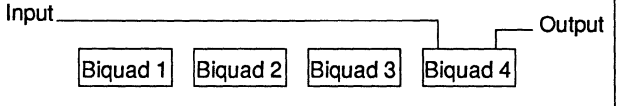
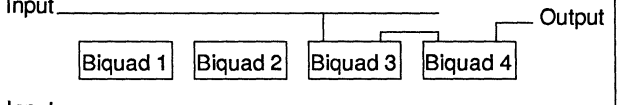
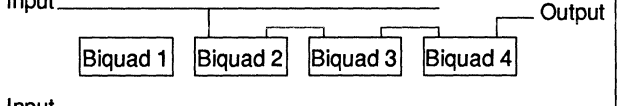
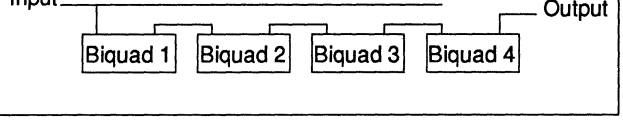
Note: CLKDIV = 2^{cdc}

Oscillator Frequency = f_{OSC}

Sample Frequency = f_S

$$f_S = \frac{f_{OSC}}{6 \times CLKDIV}$$

TABLE 3. - BIQUAD ARRANGEMENT CODES: barr

barr (low byte) Address 3E binary	hex.	dec.	barr (high byte) Address 3F binary	hex.	dec.	Configuration
000000	00	00	011000	18	24	
000000	00	00	010101	15	21	
101000	28	40	010100	14	20	
100101	25	37	010100	14	20	

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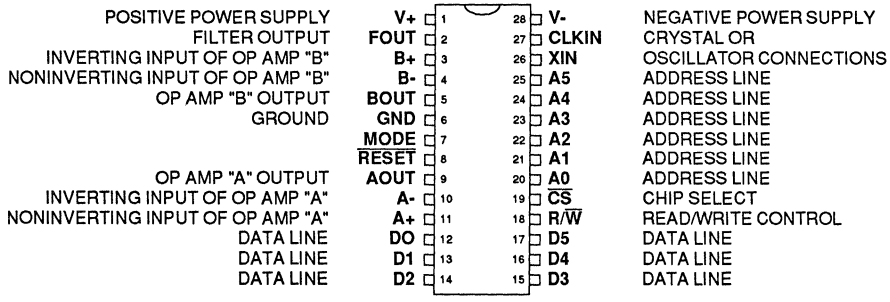
PIN DESCRIPTIONS



Power Supplies

V+ - Positive Power Supply, Pin 1

Most positive supply, typically +5 volts.

V– - Negative Power Supply, Pin 28

Most Negative Supply, typically -5 volts.

GND - Ground, Pin 6

Both analog and digital grounds are connected to this pin, which is typically held at 0 volts. This pin should be isolated from other digital grounds whenever possible to reduce noise in the analog circuits of the CS7008.

Oscillator

XIN, CLKIN - Oscillator Inputs, Pins 26 and 27.

A crystal connected across these pins sets the frequency of the internal oscillator. An externally generated clock may be connected to CLKIN, pin 27, which is TTL compatible.

Op Amps

A– - Inverting Input of Op Amp A, Pin 10.

Inverting input of an op amp whose output is connected to the biquad filter input. This op amp is used to buffer signals to the CS7008 for filtering.

A+ - Noninverting Input of Op Amp A, Pin 11.

Noninverting input of an op amp whose output is connected to the biquad filter input. This op amp is used to buffer signals to the CS7008 for filtering.

AOUT - Output of Op Amp A, Pin 9.
This pin is also connected to the input of the biquad filter.

B– - Inverting Input of Op Amp B, Pin 4.
Inverting input of the uncommitted op amp.

B+ - Noninverting Input of Op Amp B, Pin 3.
Noninverting input of the uncommitted op amp.

BOUT - Output of Op Amp B, Pin 5.
Output of the uncommitted op amp.

Inputs

MODE - Pin 7.
Setting the mode pin to V+ places the CS7008 in the self-programming mode. In the self-programming mode, the CS7008 executes an internal routine to read data from an external ROM upon power up or reset. Setting the mode pin to GND configures the CS7008 to be controlled by a microprocessor.

$\overline{\text{RESET}}$ - Pin 8.
For normal operation, the $\overline{\text{RESET}}$ should be held at V+. Setting the $\overline{\text{RESET}}$ to GND will halt operation. If MODE = V+, the self-programming routine will be initiated when $\overline{\text{RESET}}$ returns to V+. If MODE = GND, normal operation will resume when $\overline{\text{RESET}}$ returns to V+.

R/$\overline{\text{W}}$ - Read/Write Control, Pin 18.
A TTL compatible input/output used for memory access to the CS7008. When the CS7008 is in the microprocessor interface mode (MODE = GND), R/$\overline{\text{W}}$ serves as a write enable. When R/$\overline{\text{W}}$ is at a logic 0, data is clocked into the CS7008's memory on the negative transition of $\overline{\text{CS}}$, and is latched on the positive transition of $\overline{\text{CS}}$.

In the self-program mode (MODE = V+), R/$\overline{\text{W}}$ is used to enable the ROM's outputs and clock data into the CS7008's registers. Data can be read from the memory of the CS7008 by holding R/$\overline{\text{W}}$ at logic 1, and taking chip select, $\overline{\text{CS}}$, to logic 0.

$\overline{\text{CS}}$ - Chip Select, Pin 19.
A TTL compatible input used for memory access. In the microprocessor interface mode (MODE = GND), $\overline{\text{CS}}$ goes low providing a strobe to clock data into the CS7008's data registers, provided R/$\overline{\text{W}}$ is at logic 0. Data is latched on the positive transition of $\overline{\text{CS}}$. The data bus is in a high-impedance state while $\overline{\text{CS}}$ is held high.

In the self-programming mode (MODE = V+), $\overline{\text{CS}}$ serves no function and should be tied to V+ with a 100 kΩ resistor. The necessary strobes are internally generated by the CS7008.

D0-D5 - Data Inputs, Pins 12 -17.

The data bus uses six pins, and is TTL compatible. It is bidirectional, allowing data to be transferred to and from memory. Pullup resistors must be used on the data pins if they are not continually driven (bus in high-impedance state). 20 kΩ resistors are adequate.

A0-A5 - Address Inputs, Pins 20 -25.

Six pins are used for the address bus, providing 64 addresses. This bus is bidirectional, allowing data to be written to the memory address specified on these pins when the CS7008 is in the microprocessor interface mode (MODE = GND). Pullup resistors must be used on the address pins if they are not continually driven (bus in high-impedance state). 20 kΩ resistors are adequate. In the self-programming mode, addresses are output to the external ROM.

Output

FOUT - Biquad Filter Output, Pin 2.

The filtered signal is reconstructed as a staircase waveform (100% duty cycle PAM), at the sampling frequency, fS, and output at this pin.

APPENDIX

Since the CS7008 is a universal filter, it is impossible to specify the CS7008's performance for every possible transfer function. Therefore, a typical filter was selected for the *Analog Characteristics - Filter* table to show the performance of the CS7008. The selected filter specification is as follows:

Chebyshev II band-pass filter
-1 dB cutoff frequencies of 6.4 kHz and 13 kHz
Sample frequency (fs) of 173 kHz
Oscillator frequency (fosc) of 1.038 MHz
Measurement Bandwidth of 10 Hz to 30 kHz

Capacitor Values

Biquad 1	Biquad 2	Biquad 3	Biquad 4
A = 336	A = 312	A = 492	A = 235
E = 927	E = 673	E = 248	E = 252
CE = 1392	CE = 882	CE = 725	CE = 470
J = 317	J = 983	J = 90	J = 660
I = 317	I = 983	I = 90	I = 660
G = 442	G = 80	G = 254	G = 18
conf = 0	conf = 0	conf = 0	conf = 0

• Notes •

Semiconductor Corporation

CS7004

Digitally Configurable Universal Filter

Features

- Digitally Programmable to Obtain 2nd or 4th Order Audio-Band Filters
- Dynamically Configurable for Adaptive Filtering Applications
- Microprocessor Compatible Digital Interface
- Two User Configurable Op Amps for Antialiasing and Smoothing
- Supported by CRYSTAL-ICE Filter Development System
- Low Power CMOS
- 28 Pin DIP
- Pin Compatible with CS7008

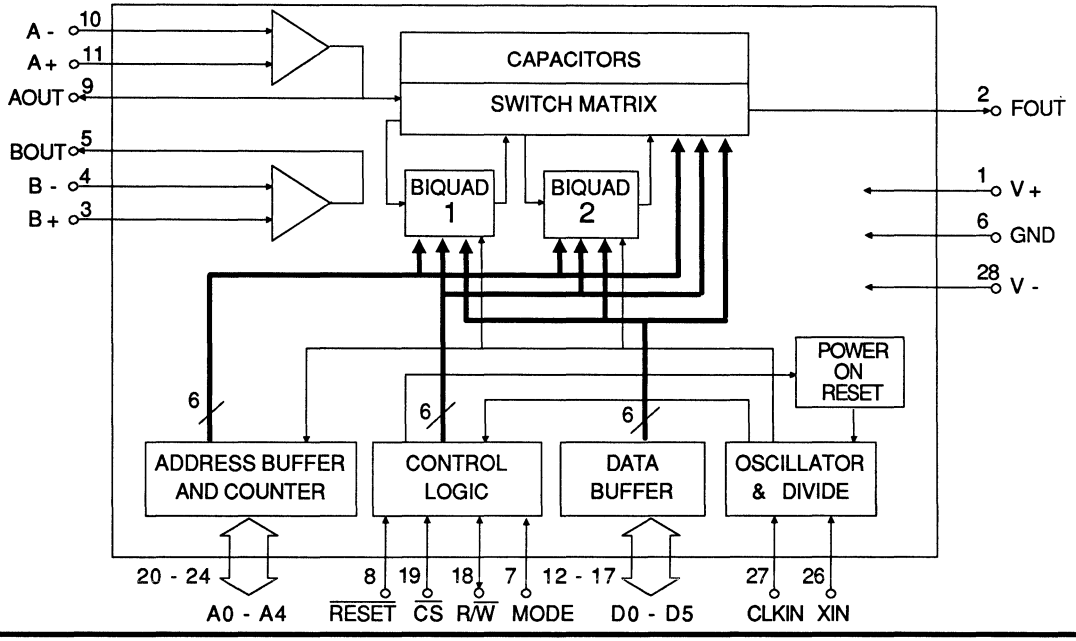
General Description

The CS7004 is fabricated in CMOS using Crystal Semiconductor's SMART ANALOG ™ design techniques. It is a digitally configurable switched capacitor filter capable of providing the system designer with virtually any precisely defined, audio-band, 2nd or 4th order filter response. An efficient microprocessor interface permits in-system reconfiguration of the filter response, and allows more cost-effective system design. Access to two operational amplifiers is also provided for use as antialiasing and smoothing filters if desired. System design is supported by the CRYSTAL-ICE Filter Development System. The development system consists of hardware and software for use with an IBM PC and provides in-circuit emulation of the CS7004 or CS7008.

ORDERING INFORMATION

CS7004-P - 28 Pin Plastic DIP	0°C - 70 °C
CS7004-ID - 28 Pin CerDIP	-40 °C - 85 °C

Block Diagram



Product Preview

This document contains data for a product under development. Crystal Semiconductor reserves the right to modify this product without notice.

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SEP '87
DS21PP1

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• Notes •

Semiconductor Corporation

CDS7000

CRYSTAL-ICE Filter Development System

Hardware Requirements:

- IBM PC or compatible with a minimum 256k of memory.
- IBM high-resolution monochrome monitor or compatible
- Hercules monochrome graphics card or compatible
- 8087 math coprocessor

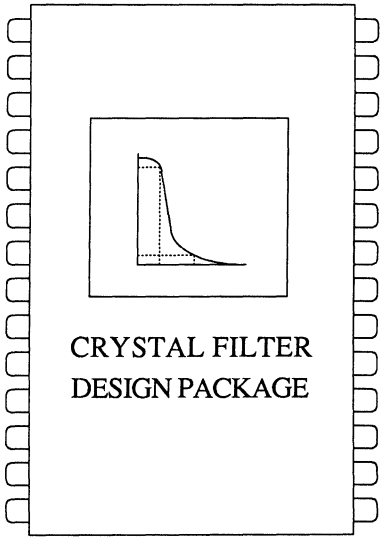
Software Requirements:

- PC-DOS or MS-DOS 2.1 or higher

General Description

The IBM PC based CDS7000, "Crystal-ICE" Filter Development System, consists of hardware and software which support filter development using the CS7008 Universal Filter. Crystal-ICE provides the designer with a quick and easy path from a initial understanding of a system's filtering requirements to a cost-effective hardware implementation of the needed filter . The menu-driven software supports filter synthesis from system specifications, direct entry of transfer functions, and filter modification at either the transfer function level or the circuit level. The in-circuit emulator (ICE) permits immediate feedback on the designed filter's performance in a system.

The CS7008 Universal Filter is fabricated in CMOS using Crystal's SMART ANALOG™ design techniques. It is a digitially configurable switched capacitor filter capable of providing virtually any audio-band, even-order filter response of eighth order or below.



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Chapters 1 & 4 From the Crystal-Ice User's Manual

SEP '87
DS3UM1

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SECTION 1. - INTRODUCTION

The CRYSTAL-ICE Filter Development System from Crystal Semiconductor is a design tool which supports the CS7008 Universal Filter. The system features an In-Circuit Emulator or "ICE Probe", which will perform a specified filtering function in a circuit board designed to use the CS7008. The arduous mathematical effort required to design a filter is eliminated by using CRYSTAL-ICE. Filter transfer functions and the coefficients required to configure the CS7008 are generated by the filter development software provided with the system. Filter coefficients developed by the program are easily downloaded to the ICE Probe, which is plugged into the user's system, where performance is evaluated. CRYSTAL-ICE makes it possible to design, test, and refine filters with unprecedented ease.

The CRYSTAL-ICE Filter Development System is shown in Figure 1-1. It consists of an ICE Probe, an interface system called the "ICE Box", interconnect cables, and the filter synthesis software which was developed by Crystal Semiconductor in conjunction with the University of New Mexico. The ICE Probe contains a CS7008 and plugs directly into a 28 pin socket in the user's system. The analog pins of the CS7008 in the probe interface with the circuit board, while the address bus, data bus and control lines interface with the ICE Box. The ICE Box controls the interface between an IBM PC and the ICE Probe. The ICE Box accepts RS-232-C formatted data output from the COM port of the PC, converts it to the appropriate parallel format, and loads the CS7008 contained in the ICE Probe.

Filters are developed using CRYSTAL-ICE by responding to menus generated by the filter development software. The program will support design of low-pass, high-pass, bandpass, and band-stop filters. Each of these filter types can be implemented as Butterworth, Chebyshev I, Chebyshev II, or elliptic (Cauer) filter responses. The program generates even order filters up to eighth order, corresponding to the capabilities of the CS7008.

To design a filter, the user simply inputs the desired filter's channel objectives as prompted by the program, thereby defining a "Filter Template". The program calculates the z-domain biquadratic transfer functions for the selected filter implementation. The response of the filter developed by the program can be evaluated graphically by directing the program to display plots of decibels vs. frequency, magnitude vs. frequency, phase vs. frequency and pole-zero locations.

CRYSTAL-ICE can also display the z-domain biquadratic transfer functions. It is possible to modify these transfer functions, or enter new transfer functions, without using the filter synthesis portion of CRYSTAL-ICE. The transfer functions are used to calculate the normalized

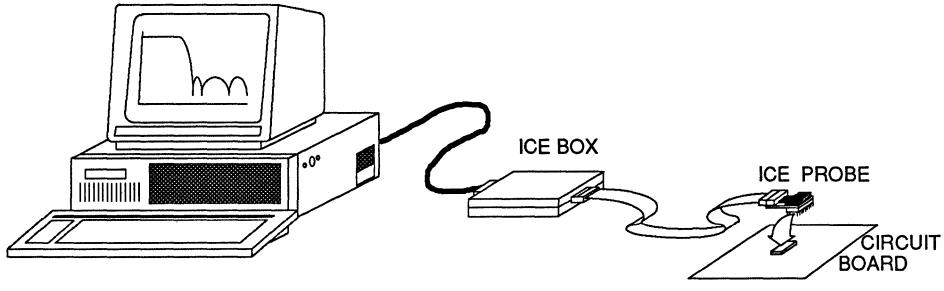


Figure 1-1. - Crystal-ICE Filter Development System

capacitor values which configure the CS7008. It is also possible to input and/or modify these capacitor values. The program will generate the CS7008 coefficients as well as the transfer function(s) that correspond to the capacitor values.

Once a desired filter response is obtained, all variables associated with that filter can be saved onto disk for later retrieval.

The CS7008 has two modes of operation. One mode allows a microprocessor to load the CS7008 coefficients, controlling its operation. In the second mode, the CS7008 reads coefficients directly from a user-defined memory upon power-up or reset. To support this mode, the CRYSTAL-ICE software can download coefficients directly to an EPROM Programmer via one of the COM ports on the PC.

The CRYSTAL-ICE software runs on an IBM PC or compatible, with a Hercules monochrome graphics card, an 8087 math coprocessor, an MS-DOS or PC-DOS operating system (version 2.1 or above), and a high-resolution monochrome monitor.

The ICE Box requires a +5 volt supply. The ICE Probe requires +5 and -5 volt supplies and a clock source which must be provided by the user's circuit board. This circuit board must also provide the analog interface for the CS7008. To assist the user in developing such a circuit board, an unpopulated CS7008 printed circuit board (PCB) is included with the ICE system. Appendix C contains the information needed to build the PCB to the necessary specifications. All other hardware and software required to implement a filter are provided with the ICE system.

1.1 In-Circuit Emulation and Interactive Design

The ICE Probe, which contains a CS7008, plugs into a 28 pin socket on a circuit board designed to accept the CS7008. The circuit board should include the analog interface for the CS7008, which consists of an antialiasing filter, a smoothing filter, an oscillator crystal or clock source, the signal inputs and outputs and the power supplies required by the CS7008. Directing the CRYSTAL-ICE program to load the CS7008 causes the coefficients generated by the program to be transferred to the CS7008 in the ICE Probe. Signals can then be applied to the circuit's inputs, and the performance of the filter in the circuit can be evaluated. Modifications to the filter response can be accomplished in minutes, and the results observed instantaneously. This iterative process can continue until the optimum filter response is achieved.

The In-Circuit Emulator gives the designer the opportunity to evaluate all aspects of circuit performance before "freezing" a design. The ability to evaluate the circuit is not limited to electrical performance. For example, the circuit board can be subjected to a variety of environmental conditions. If necessary, the filter response can be modified to account for any system level variations that may occur.

CRYSTAL-ICE can also be used to develop coefficients for adaptive filter applications, since many different filters can easily be designed for a given system. Any filter supported by CRYSTAL-ICE can be generated in a matter of minutes.

Once the performance of a filter is satisfactory, the filter coefficients generated by CRYSTAL-ICE can be loaded into a (EP)ROM used to configure the CS7008 in its "self-program" mode, or stored in memory to be loaded into the CS7008 by a microprocessor.

The versatility of the CS7008 makes this development system very powerful. Literally millions of filters can be implemented using the CS7008 and the CRYSTAL-ICE system.

SECTION 4. - FILTER DEVELOPMENT

The CRYSTAL-ICE Filter Development software allows the user to design a filter by specifying a filter performance template. There are four kinds of filters supported by CRYSTAL-ICE: low-pass, high-pass, band-pass, and band-stop. CRYSTAL-ICE offers four possible implementations of these filters: Butterworth, Chebyshev I, Chebyshev II, and elliptic (Cauer). A synopsis of the features of these different filter implementations is given in the Filter Implementations section of Appendix A.

4.1 Using CRYSTAL-ICE to Design a Filter

Using CRYSTAL-ICE, a filter is designed by moving through a series of menus which allow the user to first specify a filter and then examine plots of the filter's theoretical performance. The main menus are arranged in the sequence shown in Figure 4-1. From each menu, select the desired item by typing the corresponding number and striking the Return key. The Back Space key can be used to delete an entry before striking the Return key. The ESCape key can be used in any menu, except the Filter Type menu, to regress one menu in the sequence. When in the Filter Template Menu or Filter Response Plots, the Tab key is used to move through the menu.

The Filter Type menu is the only menu from which the program can be terminated (to DOS). All other menus (except DOS Files and EPROM Programmer menus) allow you to return directly to the Filter Type menu to start a new filter design or terminate the program.

4.1.1 Printing Screens

There are two types of screens in the filter development software: text and graphics. The Filter Template and Filter Response Plots are graphics screens while all other screens are text. The "Print Screen" command shown on the filter response plots will cause a screen dump to occur. The software configures the PC to print graphics screens. If a print of a text screen is desired, the shift PrtSc key must be pressed and immediately followed by the ESCape key. If a graphics print has already started, pressing the ESCape key will stop the print.

4.2 Filter Type Menu

The first menu displayed by the program is the Filter Type menu, shown in Figure 4-2. To select the desired filter type, enter the corresponding number and hit the Return key. Notice that this menu provides direct access to the CS7008 Details menu. This allows those who have independently developed solutions for the biquad

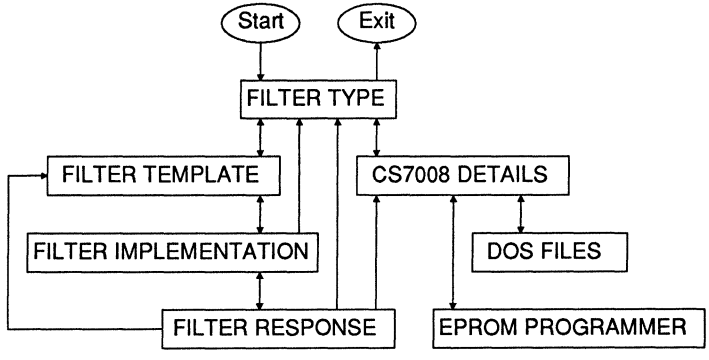


Figure 4-1. - Menu Arrangement

FILTER TYPE

1 - Low Pass
2 - High Pass
3 - Band Pass
4 - Band Stop
5 - CS7008 Details Menu
6 - Exit Program

Enter Selection:

Figure 4-2. - Filter Type Menu

equations or derived capacitor values to bypass the filter synthesis portion of the program. The use of the CS7008 Details menu for entering or changing filter parameters is described in greater detail in Section 6. When entering the CS7008 Details menu from the Filter Type menu, no calculations occur. If pre-calculated capacitor coefficients are desired, the CS7008 Details menu should be entered from the Filter Response menu.

4.3 Filter Template Menu

Once a filter type is selected, a diagram representing the filter type is displayed on the screen along with a list of parameters used to describe the filter's response. This is referred to as the Filter Template. The Filter Template for the low-pass filter, with all of the input options, is shown in Figure 4-3. The Tab key or Return key is used to enter new values or to move through the display if values already exist.

The first parameter entered is the scaling factor. The scaling factor determines whether frequencies used by the program will be input and displayed in hertz (select "H") or kilohertz (select "K"). When initially entered, the program will default to kilohertz if the Return or Tab key is struck. Once the scaling factor is entered, the remaining parameters required to specify a filter are displayed.

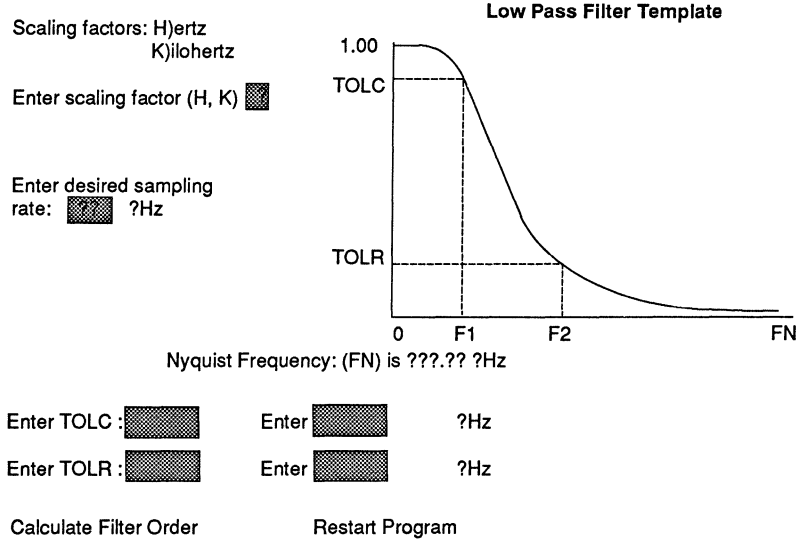


Figure 4-3. - Low Pass Filter Template

The next entry is the sampling rate. The sampling rate is determined by the oscillator or clock frequency input to the CS7008 and the clock divide code as given in Equation 1.

$$fosc = fs \times 6 \times CLKDIV$$

Equation 1.

When a sampling rate is entered, the program responds by displaying the Nyquist frequency. The Nyquist frequency equals one half of the sampling frequency (fS), and is the highest frequency which can be filtered at the specified sampling rate. It is advisable to select a sampling frequency well in excess of the highest frequency of interest in the signal to be filtered. See Appendix A for more detailed information.

The filter's pass band and rejection band parameters are entered by specifying the cutoff and rejection amplitude tolerances, TOLC and TOLR, and their corresponding frequencies. TOLC and TOLR are entered in values normalized to one (i.e., these values must be less than 1, and greater than 0). If you prefer to think in decibels, the tolerances are easily converted from magnitude to decibels by using Equation 2.

$$TOL_{dB} = 20 \log_{10} TOL_{MAG.}$$

Equation 2.

The tolerances can be entered with resolutions to five digits to the right of the decimal point. Corner frequencies can be entered to accuracies of six significant digits. The maximum frequency entered must be less than the Nyquist frequency (fS/2). If an inappropriate value is entered, the program will not accept the entry and will prompt you to enter a new value. The backspace key can be used while entering parameters to delete characters to the cursor's left.

Once all of the parameters have been entered, it is possible to modify any entry by using the Tab key to move through the display. The Tab key is also used to select the menu commands at the bottom of the display. The highlighted command is entered by striking the Return key. When a satisfactory set of parameters describing the filter template have been entered, select the "Calculate Filter Order" command. The program will determine the order required for each filter implementation, and display the Filter Implementation menu. An example is shown in Figure 4-4.

4.4 Filter Implementation Menu

```
                    FILTER IMPLEMENTATION
-------------------------------------------------------------
1 - Butterworth    EXCEEDS EIGHTH ORDER
2 - Chebyshev I        Order : 8
3 - Chebyshev II       Order : 8
4 - Elliptic           Order : 6
5 - Return to Filter Template
6 - Restart Program
Enter Selection:
```

Figure 4-4. - Filter Implementation Menu

If the filter order required for a particular implementation exceeds eight, the program will display "EXCEEDS EIGHTH ORDER" next to that filter implementation. If necessary, return to the Filter Template and change the parameters to reduce the filter order.

Selecting one of the filter implementations directs the program to calculate a z-domain transfer function for each biquad required. The program uses the transfer function to generate the plots offered on the Filter Response menu, which is shown in Figure 4-5.

4.5 Filter Response Menu

```
FILTER RESPONSE
---------------------------------------------
1 - Magnitude Plot
2 - Decibel Plot
3 - Phase Plot
4 - Pole-Zero Plot
5 - CS7008 Details Menu
6 - Return to Filter Template
7 - Return to Filter Implementation Menu
8 - Restart Program

Enter Selection:
```

Figure 4-5. - Filter Response Menu

From the Filter Response menu it is possible to return to the Filter Implementation menu to select a different implementation, or to go back to the Filter Template to change the filter's parameters. Each time the parameters are changed, the filter order and transfer functions are recalculated.

When viewing a plot, the Tab key is used to highlight the different menu items at the bottom of the screen such as "Modify Frequency Window" or "Print Screen". When the Return key is pressed, the highlighted menu item is entered. The graphs are plotted from 0 Hz to the Nyquist frequency (with the exception of the pole-zero plot). For filters with oversampling ratios which approach 20 (as recommended), the interesting portions of the plots occupy only a small portion of the whole plot. "Modify Frequency Window" allows expansion of any portion of the plot by reducing the range of frequencies plotted along the frequency axis. The beginning and ending frequencies for the plot, FLow and FHigh, can be specified, and those frequencies will be retained until a different filter template is specified.

Once the filter developed by the synthesis portion of the program is satisfactory, the next step is to calculate the actual capacitor values needed to configure the CS7008 and evaluate the in-circuit filter performance. To calculate the filter coefficients for the CS7008, select "CS7008 Details Menu" from the Filter Response menu. The program calculates the capacitor values and other information needed to configure the CS7008 from the transfer functions previously generated. Errors can occur when calculating capacitor values from ideal transfer functions. Some errors occur because the capacitor values required are larger than the permissible range of the CS7008 or the Q of the transfer function is excessively large. Appendix B, Section 3, describes these errors in detail. The above calculations will not occur when entering the CS7008 Details Menu from the Filter Type Menu.

4.6 CS7008 Details Menu

The CS7008 Details menu, shown in Figure 4-6, provides the capability to display and change both the coefficients of the filter transfer functions and the normalized capacitor values. The digital words used to configure the CS7008 can also be displayed. To load the digital words into the CS7008 on the ICE Probe, select "Load CS7008". This command directs the program to transfer its data to the ICE Box, which in turn loads the CS7008 in the ICE Probe. When downloading to the ICE Box, the ICE Probe must be powered or the following message will occur:

No Probe voltage sensed. Cannot download.
Press any key to continue

If this occurs, power up the ICE Probe and reselect "Load CS7008" from the CS7008 Details menu. Downloading should now work properly.

Item 3 on the CS7008 Details menu, View CS7008 Coefficients, displays the digital words (and corresponding addresses) for the capacitor

values shown in the Biquad Values menu. Data in the CS7008 Coefficients menu is formatted for the CS7008 as specified in the data sheet (Appendix D).

CS7008 DETAILS

1 - View H(z)
2 - View Biquad Values
3 - View CS7008 Coefficients
4 - Load CS7008
5 - EPROM Programmer
6 - DOS Files
7 - Restart Program

Enter Selection:

Figure 4-6. - CS7008 Details Menu

Select item 5 to download the filter data to an EPROM programmer. Item 6 allows the user to save or recall filter data from disk. Items 5 and 6 are explained in detail in Section 4.7 and 4.8 respectively.

With the exception of entering the clock divide code to be loaded into the CS7008, items 1 and 2 on the CS7008 Details menu are intended for individuals who are knowledgeable regarding switched capacitor biquad filters. The capabilities offered through items 1 and 2 are discussed in Section 6.

4.6.1 Changing the Clock Divide Code

The clock divide code is loaded into the memory of the CS7008, and determines the internal oscillator divide within the device. The clock divide code is initialized to a default value of one when the program is executed. It may be necessary to change the clock divide code depending on the particular application. For more information see the section on Oscillator, Sampling Frequency and Clock Divide in Appendix A.

To change the clock divide code, select "View Biquad Values". The Biquad Values menu displays the normalized biquad capacitor values for the specified filter. Select item 6 to change the clock divide. The program prompts you to enter the desired clock divide code. The clock divide codes that will be accepted by the CS7008 are 1, 2, 4, 8, 16, 32, 64, or 128. After the new clock divide code is entered, return to the CS7008 Details menu. Once changed, the clock divide code will remain at the selected value until a new value is entered by the user. Unless you intend to change the filter's transfer functions, be careful not to change any other parameter from this menu.

4.6.2 Suboptimal Dynamic Range Scaling

The transfer functions generated by the filter synthesis routines may require capacitors with normalized unit values exceeding 2047. In some cases it is possible to scale unit capacitor values and still achieve the desired filter. This capacitor scaling causes the gain through the affected biquad to increase. The maximum input signal to the filter must decrease to compensate for the gain. This process reduces the CS7008's dynamic range, which is why it is referred to as suboptimal dynamic range scaling.

Not all capacitors can be scaled. When possible, the filter development program will automatically scale capacitors, up to the point where the input is reduced to 5% of the maximum input voltage swing for the CS7008. When dynamic range scaling of capacitors in a biquad occurs, a warning is issued as shown in Figure 4-7. This warning directs the user to limit the dynamic range of the input signal by a specified amount.

**** Input Voltage Range reduced to 85% of maximum value. ****
Press any key to continue

Figure 4-7. - Input Voltage Reduction Warning

If more than one biquad requires dynamic range scaling, additional warnings will be issued. The input signal's voltage range should be limited to the smallest of the percentages displayed. The smallest percentage will be displayed at the top of the Biquad Values menu.

4.7 EPROM Programmer Menu

The CS7008 has two modes of operation. One mode will allow a microprocessor to load CS7008 coefficients, and thereby control its operation. In the other, a self-programming mode, the CS7008 will read coefficients from memory upon power-up or reset. To facilitate the use of this mode, the CRYSTAL-ICE Filter Development software supports downloading to an EPROM programmer via one of the COM ports on the PC. The EPROM programmer must support RS-232-C communications and either Intel Hex or Motorola S-Record data formats.

```
Format: Intel Hex                    Port: COM2
 BAUD: 1200   Data Bits: 7   Parity: Even   Stop Bits: 2

Start Address: 0          (0x0)

        :10000000000000000000000000000000000000000000F0
        :1000100006110611180301000B010B0118030100062
        :10002000140A040A1C040100110511051C04000037
        :100030001F05150E021500000B070B070D062814EF
        :0000001FF

                              EPROM PROGRAMMER
                              ----------------------------------
                              1 - Load Programmer
                              2 - Change Start Address
                              3 - Change Port Parameters
                              4 - Return to CS7008 Details Menu

Enter Selection:
```

Figure 4-8. - EPROM Programmer Menu

The user must supply the cable to interface the PC and EPROM programmer. Section 3.3 lists the specifications for this interface cable.

The EPROM Programmer menu is accessed from the CS7008 Details menu and is shown in Figure 4-8. The default port parameters are listed on the top two lines of the screen. The filter coefficients are loaded into 64 successive locations with the start address being the first of the 64 locations. The lines between the start address and the menu contain the actual records to be downloaded.

4.7.1 Loading the EPROM Programmer

If item one, Load Programmer, is selected, the software will attempt to send the data through the COM port (listed at the top of the screen) to the programmer. If the attempt is unsuccessful, one of the following messages will appear:

COMx not responding (DSR inactive)
Press any key to continue

or:

COMx not responding (Time Out)
Press any key to continue

where x in COMx designates the port used. If either of these messages appear, verify that the EPROM programmer is powered, connected to that particular COM port, and waiting for data to be downloaded. See Appendix B, Section 4 for more information on these two errors.

If the EPROM programmer signals an error while downloading, verify that the port parameters displayed at the top of the screen are the same as the EPROM programmer's parameters.

4.7.2 Changing the Start Address

Item two from the menu, Change Start Address, allows the filter coefficients to be loaded into any set of adjacent addresses in the EPROM. Once "Change Start Address" is selected, a new address must be entered in decimal notation. The Tab key may be used to increment one filter length (64 bytes). Pressing the Return key enters the address and updates the records to reflect the new address.

4.7.3 Changing Port Parameters

Using menu item three, Change Port Parameters, almost any aspect of the port can be modified to suit the EPROM programmer used. Any modified parameter will remain in effect until the program is exited. When "Change Port Parameters" is selected, the bottom line of the screen will change as shown in Figure 4-9, and an enlarged cursor will blink to the right of the first parameter. The Tab key will change the value to the left of the cursor.

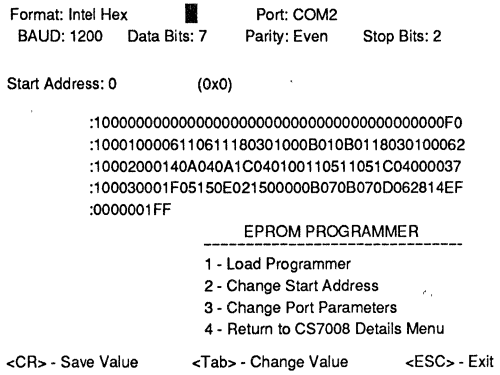


Figure 4-9. - Changing Port Parameters

Use the Tab key to "roll" through the available values until the appropriate one is displayed. Pressing the Return key (CR) will save the value and move the cursor on to the next parameter. The ESCape key will immediately cause an exit back to the initial EPROM Programmer menu. The parameter selected when the ESCape key is pressed will not retain a changed value (the Return key must be used first).

If the modified COM port parameter is the same as that of the ICE Box, then the cable for the EPROM programmer must replace the ICE Box cable on the PC. Before leaving the EPROM Programmer menu, the ICE Box must be reconnected to the COM port. In this instance, the following message will appear as a reminder:

ICE Box must be reconnected to COMx
Press any key to exit

where x in COMx indicates the port number. Below is a list of the port parameters with all their possible values:

Format: Intel Hex
Motorola S-Record

Port:
COM1
COM2
COM3*
COM4*

*IBM BIOS only supports two COM ports. If COM3 or COM4 exist, they must be BIOS compatible.

Baud:
150
300
600
1200
4800
9600

Data Bits:
7
8

Parity:
None
Even
Odd

Stop Bits:
1
2

4.8 DOS Files Menu

Once a desired filter is obtained, all the variables associated with that filter can be saved onto disk for later retrieval. The DOS Files menu is shown in Figure 4-10 and is accessed from the CS7008 Details menu. The top line on this screen displays the present working directory. The next line displays the most recent file read from or saved to disk. The file name will disappear if a new filter is calculated using the synthesis portion of the program. If no extension is given when reading from or saving to disk, a ".UF" is assumed.

Directory - C:\FILTER
File Name -

DOS FILES

1 - Read File
2 - Save File
3 - Change Directory
4 - Return to CS7008 Details Menu

Enter Selection:

Figure 4-10. - DOS Files Menu

4.8.1 Reading Files

When reading a file from disk, the program will prompt the user for a filename. Filenames must adhere to DOS standards. DOS device names may not be used for filenames. Consult the DOS manual for filename specifications. Errors can occur because of the following:

invalid disk specifier
invalid path specifier
invalid filename
file not found
invalid format in file

All errors are discussed in detail in Appendix B, Subsections 5 and 6.

4.8.2 Saving Files

When saving a file to disk, the program will prompt the user for a filename. In choosing the filename, the user must follow the same conventions as when reading files from disk. Errors can occur because of the following:

invalid disk specifier
invalid path specifier
invalid filename

Errors are discussed in detail in Appendix B, Subsections 5 and 6. If the file specified already exists, the program will ask for verification before replacing it.

4.8.3 Changing Directories

Changing the present working directory will allow a more orderly file structure since different filter projects may be kept in different directories. When changing directories, the new directory must already exist. New directories should be created using DOS prior to executing the CRYSTAL-ICE software. Changing directories will also allow changing disk drives. If no directory is given when changing drives, the current

directory for that particular drive is used. DOS remembers the current directory for each drive. The following errors can occur when changing directories:

invalid disk drive specifier
invalid path specifier

All errors are explained in detail in Appendix B, Subsections 5 and 6.

4.9 Menu Paths

Figures 4-11 thru 4-15 depict the possible paths from each of the main menus in the filter development program. These figures are intended to serve as a handy reference for understanding the menu structure used in the CRYSTAL-ICE filter development software.

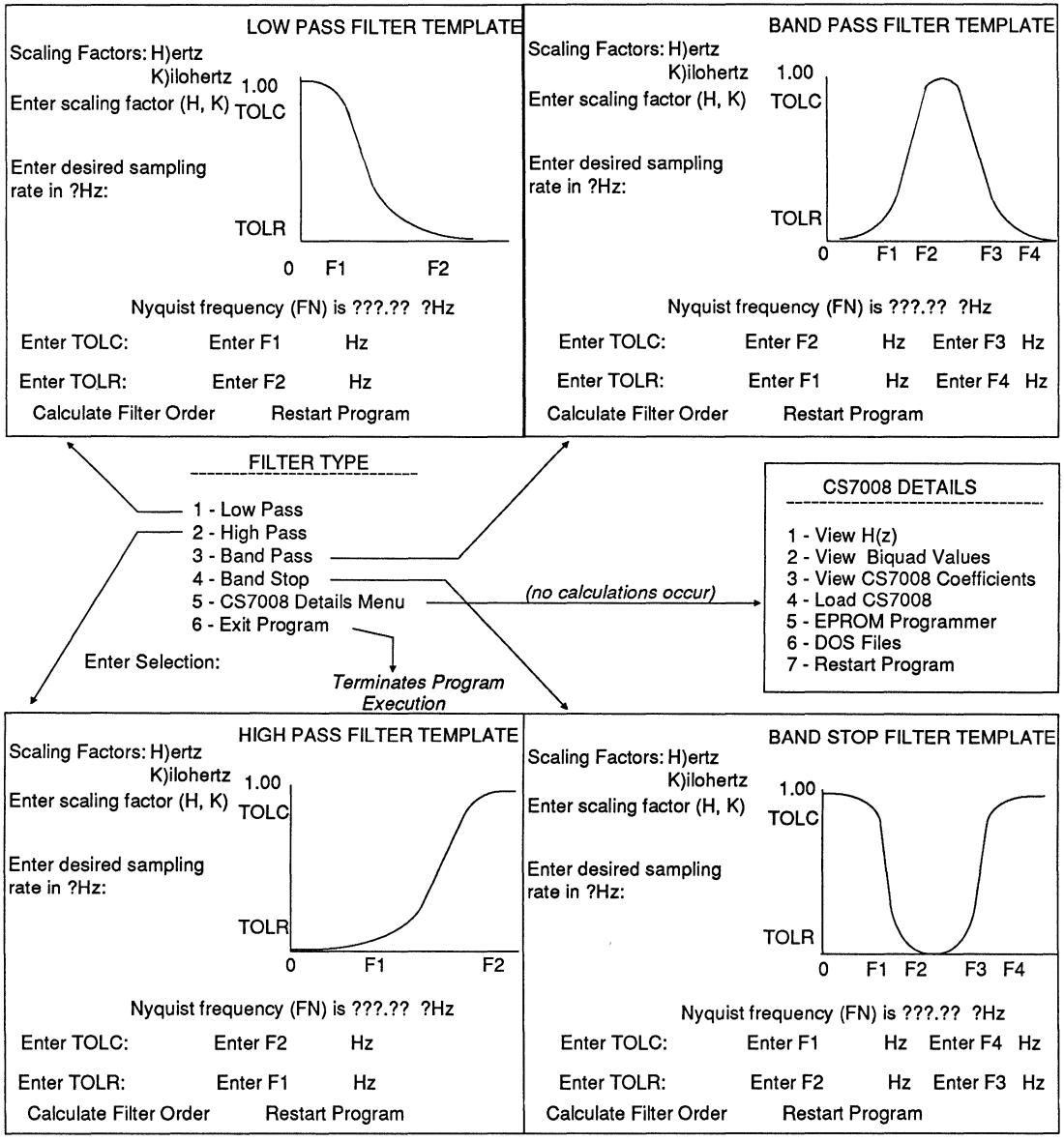


Figure 4-11. - Filter Type Menu Paths

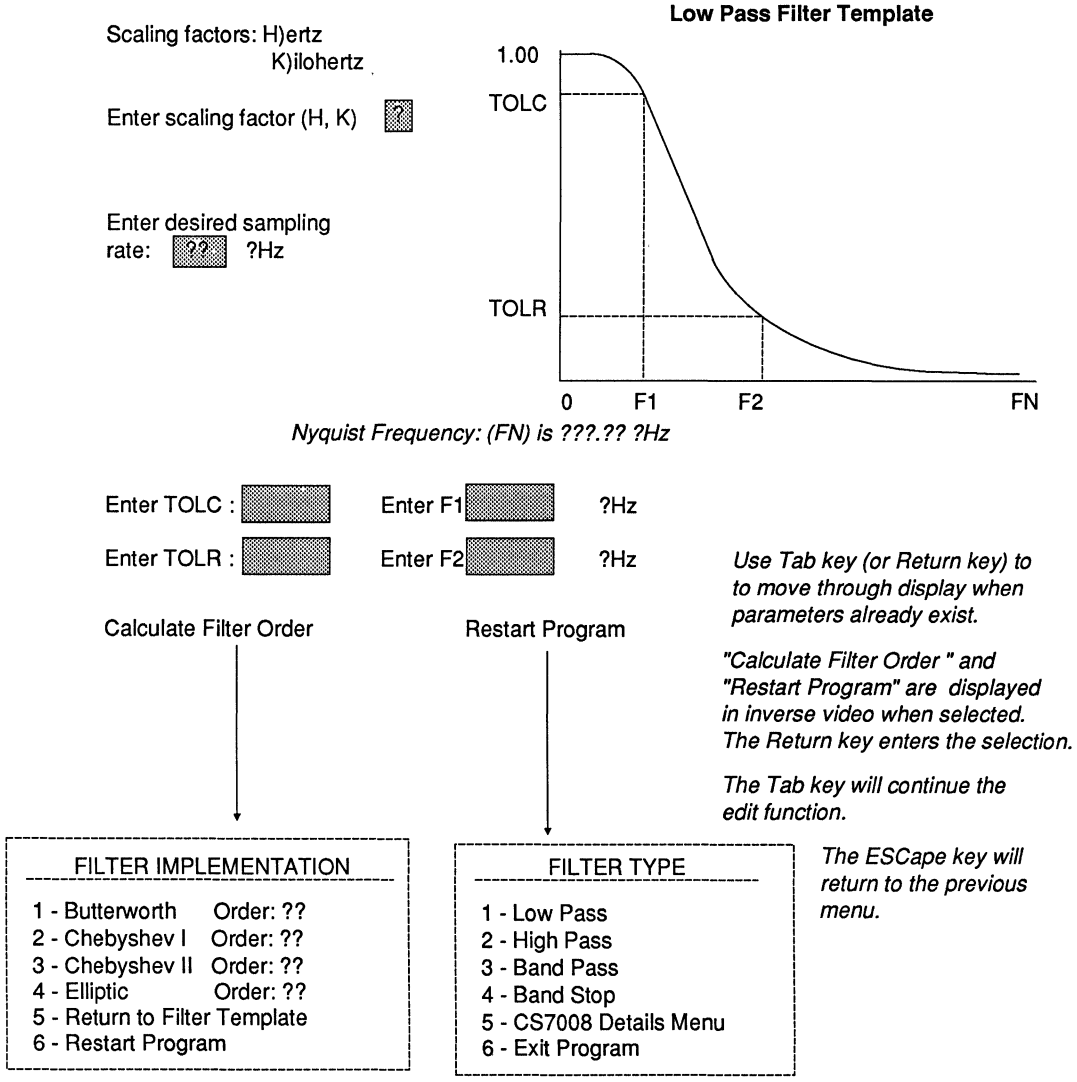


Figure 4-12. - Filter Template Paths

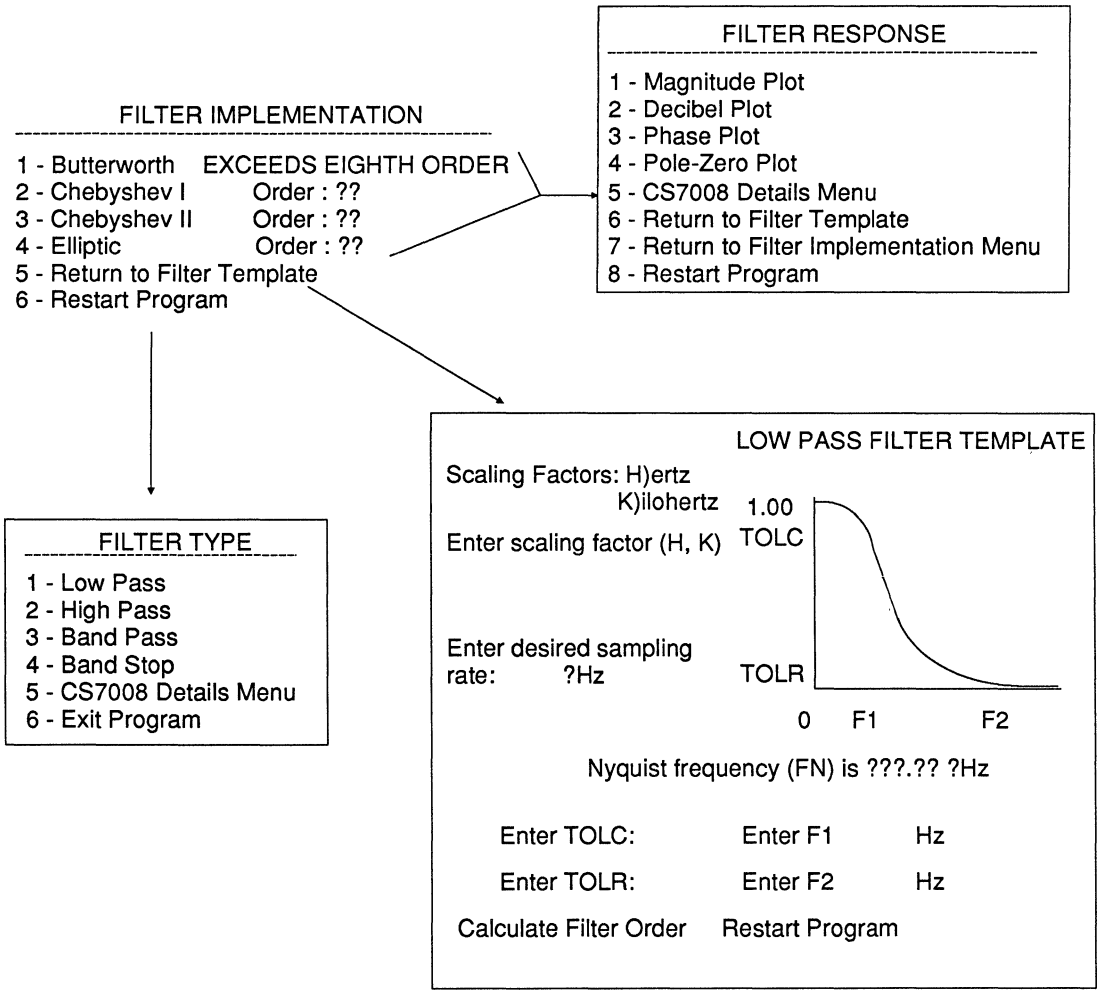


Figure 4-13. - Filter Implementation Menu Paths

9

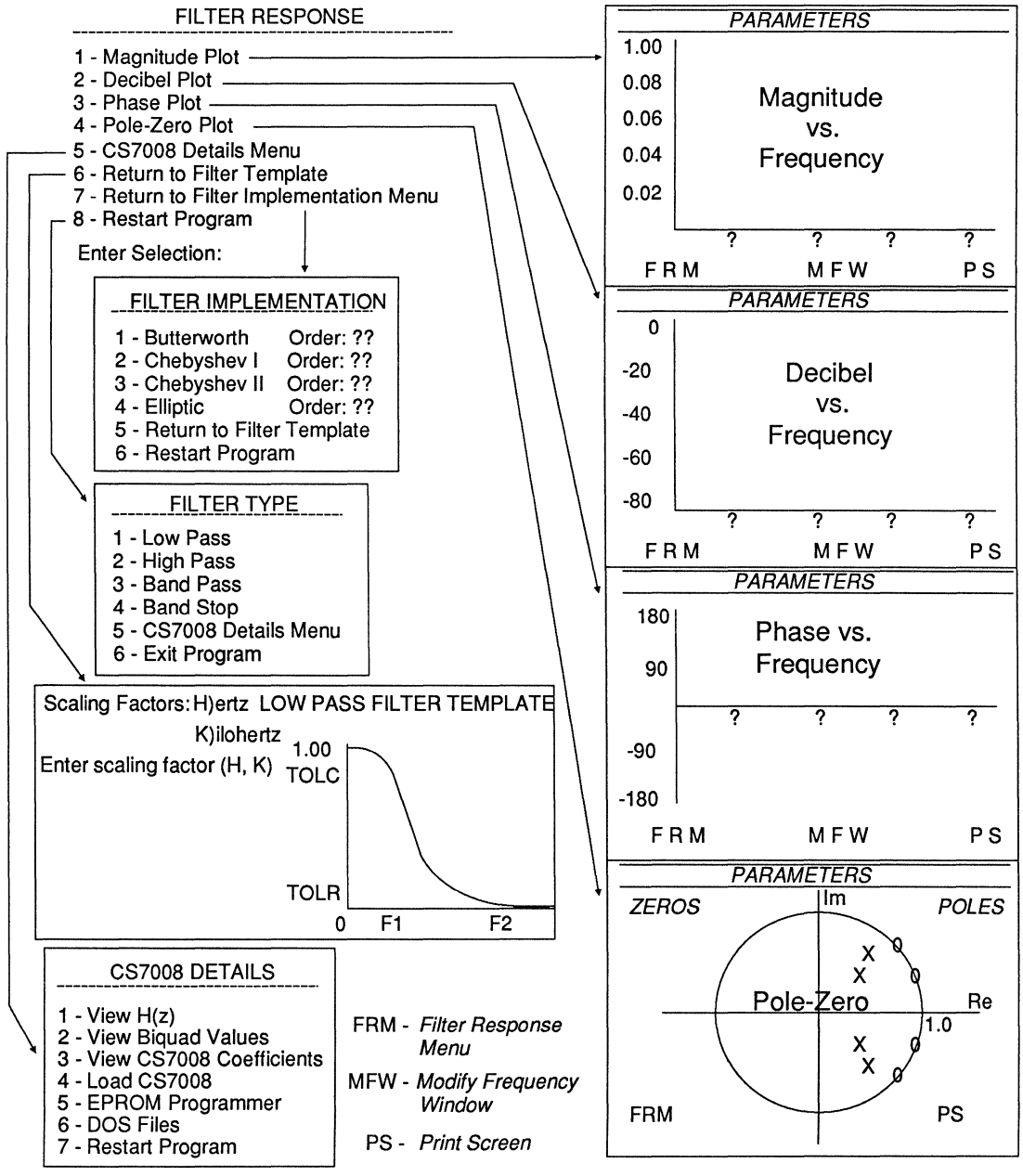


Figure 4-14. - Filter Response Menu Paths

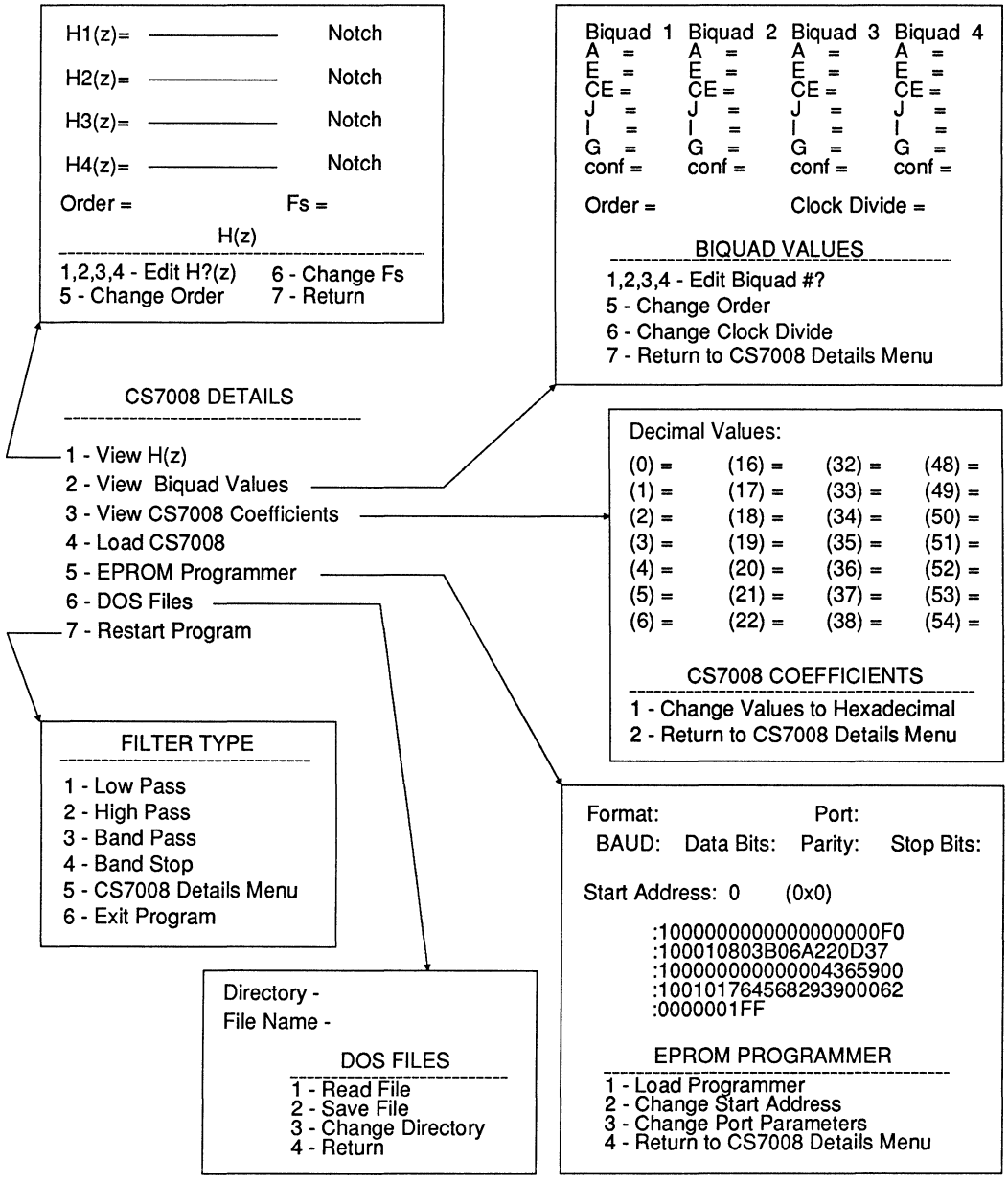


Figure 4-15. - CS7008 Details Menu

• Notes •

INTRODUCTION

High-quality evaluation boards are available to allow rapid evaluation of Crystal products, often freeing the customer from the task of initial breadboarding. The layout and grounding schemes may be used as quidelines for the customer's own system design. Isolation of system problems can be aided by comparison with the evaluation board operation.

USER'S GUIDE

Device:	Crystal Part Included	Basic Function
CDB31412	CS31412-KD	Quad Sample/Hold
CDB5012	CS5012-KP12	12-Bit, 12 µs, A-to-D
CDB5014	CS5014-KP14	14-Bit, 14 µs, A-to-D
CDB5016	CS5016-JC16	16-Bit, 16 µs, A-to-D
CDB5112	CSZ5112-KP12	73 dB, 63 kHz, A-to-D
CDB5114	CSZ5114-KP14	83 dB, 55 kHz, A-to-D
CDB5116	CSZ5116-JC16	92 dB, 50 kHz, A-to-D
CDB5316	CSZ5316-P	84 dB Voice-Band, A-to-D
CDB5412	CSZ5412	12-Bit, 1 MHz, A-to-D
CDB61534	CS61534-IP1	T1/CEPT Line Interface
CDB61544	CS61544-IP	T1 Line Interface
CDB7008	CS7008-C	Switched Cap Filter

CONTENTS

Semiconductor Corporation

CDB31412

CS31412 Evaluation Board

Features

- Industry Standard Header Connector
- BNC Connectors for Analog I/O's
- DIP-Switch Selectable:
  Differential & Single-Ended Modes
  Analog Mux Configuration
- Push Button Reset and Calibration
- User Configurable Ground Planes

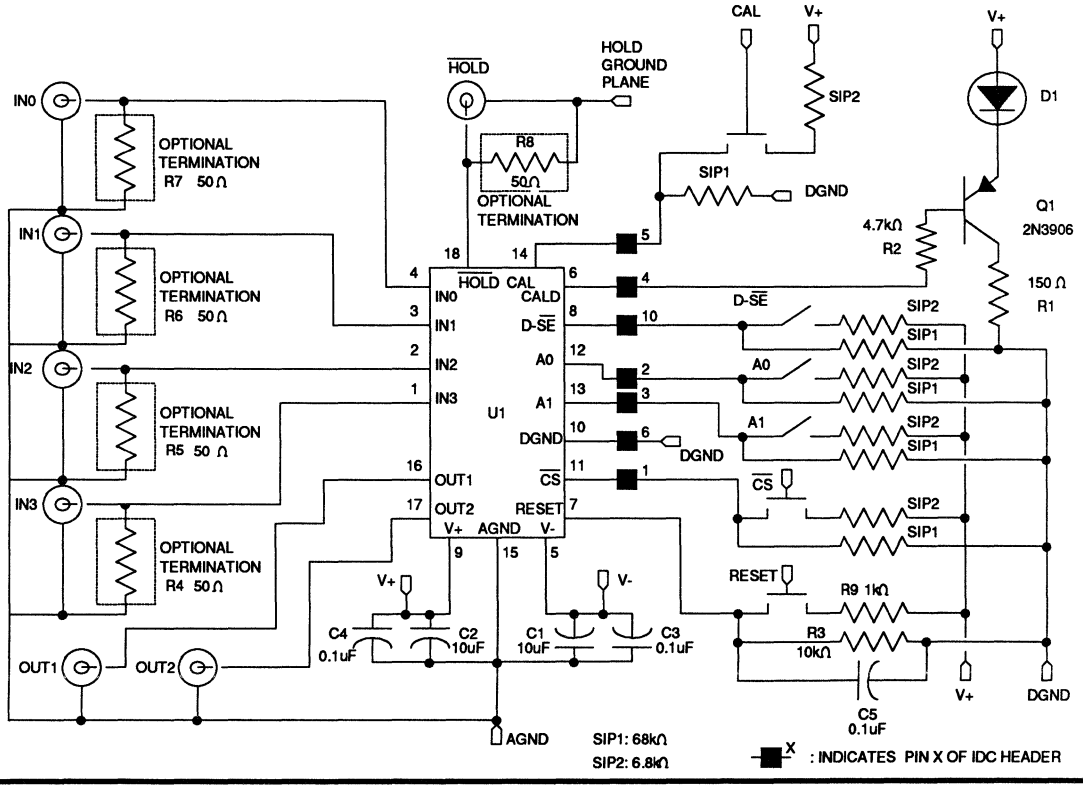
General Description

The CDB31412 Evaluation Board is designed to allow the user to quickly evaluate the function and performance of the CS31412 Simultaneous Track-and-Hold.

All analog inputs and outputs can be interfaced to the board with coaxial BNC connectors. Optional termination resistors can also be added.

A 10 pin IDC header is provided for microprocessor control.

ORDERING INFORMATION
CDB31412



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, Texas 78760
(512)445-7222 TWX: 910-874-1352

Analog Input and Output Connections

The four analog inputs to the CS31412 are connected to the CDB31412 via the BNC coaxial connectors labeled IN0, IN1, IN2, IN3. These inputs have locations reserved for termination resistors if they are needed. The analog outputs from the CS31412 are available at the BNC coaxial connectors labeled OUT1, and OUT2.

DIP-Switch Configuration

The input mode is controlled by the D-$\overline{SE}$ switch of DIP-switch SW4. If it is off, the part is in single-ended mode (4-to-1 mux). If it is on, the part is in the differential mode (dual 2-to-1 mux). After changing the differential mode switch position, the $\overline{CS}$ pushbutton must be depressed to internally latch the part. The CS31412 must be calibrated after switching between single-ended and differential modes.

The A1 and A0 switches of DIP-switch SW4 control the CS31412's output control mux. The chart below summarizes the DIP-switch configurations.

Reset and Calibration

The CS31412 will usually reset itself upon power-up. Since this function is not guaranteed, the chip must be reset upon power-up in system operation. The part can be reset on the CDB31412 board by momentarily depressing pushbutton SW3. After resetting the part, the LED will be on indicating that the part needs to be calibrated. To initiate a calibration, depress pushbutton SW1. After approximately 3.5 milliseconds, the LED will turn off indicating that the part has been calibrated. The CS31412 is now ready for operation.

Microprocessor Interface

The CAL, $\overline{CS}$, A0, A1, and D-$\overline{SE}$ inputs and the CALD output are available at the 10 pin IDC header. The five inputs are pulled low through 68 kΩ resistors placing the CS31412 in a microprocessor independent mode. These inputs may be pulled high by the DIP-switches and pushbutton or by driving the 10-pin IDC header. When using the header to externally drive these inputs, the three DIP-switches controlling A0, A1, and D-$\overline{SE}$ must be in the off position so that no loading will occur. All remaining pins of the IDC header are tied to DGND and cannot be driven.

D-$\overline{SE}$	A1	A0	OUT1	OUT2
off	off	off	IN0	0.0V
off	off	on	IN1	0.0V
off	on	off	IN2	0.0V
off	on	on	IN3	0.0V
on	off	off	IN0	IN1
on	on	off	IN2	IN3

Figure 1. Dip-Switch Configuration

Decoupling

The CDB31412's decoupling scheme was designed to insure accurate evaluation of the CS31412's performance independent of the quality of the power supplies. Each supply is decoupled at the part with a 10 µF electrolytic capacitor to filter low-frequency noise and a 0.1 µF ceramic capacitor to handle higher frequencies. Depending on the quality of the system's power supplies, the decoupling scheme could be relaxed in actual use.

Ground Planes

The CDB31412 has three separate ground planes which may be interconnected by the user to simulate actual system conditions. When shipped from the factory, the analog ground plane, the digital ground plane, and the hold ground plane are separate. Jumpers J1, J2, J3, and J4 are used to interconnect these ground planes. Separate ground planes are the suggested configuration for best performance of the part. For more information on grounding, Application Note: "Suggested Grounding and Supply Arrangements for the CS31412" is recommended.

COMPONENT LIST

150 Ω resistor	R1
4.7 kΩ resistor	R2
10 kΩ resistor	R3
1 kΩ resistor	R9
68.0 kΩ sip resistor	SIP1
6.8 kΩ sip resistor	SIP2
0.1 µF capacitor	C3, C4, C5
10 µF capacitor	C1, C2
CS31412 Track/Hold	U1
2N3906 transistor	Q1
LED	D1
3 pos. SPST DIP switch	SW4
SPST pushbutton	SW1, SW2, SW3
10 pin header	P12
PC-mount BNC	P5, P6, P7, P8, P9, P10, P11
red banana jack	P1
black banana jack	P3, P4
green banana jack	P2
1" 4-40 spacer	POST1, POST2, POST3, POST4
3/8" 4-40 screw	SC1, SC2, SC3, SC4

• Notes •

Semiconductor Corporation

CDB501X

Evaluation Board for CS501X & CSZ511X ADC's

Features

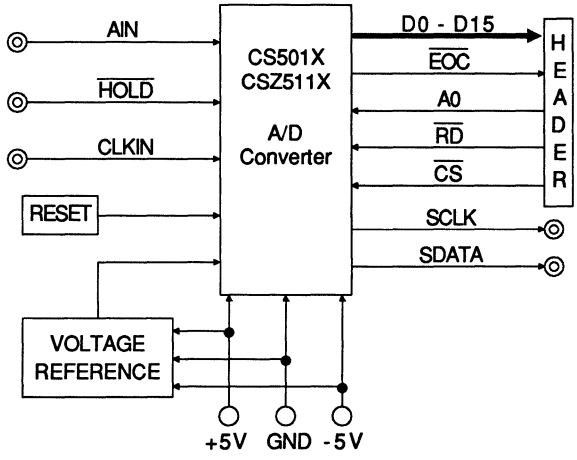
- PC/uP-Compatible Header Connection
  - 16-Bit Parallel Data
  - End-of-Conversion Output
  - $\overline{CS}$, $\overline{RD}$, and A0 Control Inputs
- DIP-Switch Selectable:
  - Unipolar/Bipolar Input Range
  - Burst & Interleave Calibration Modes
  - Continuous Conversion
- Adjustable Voltage Reference
- Serial Data and Clock BNC Connections
- Operation from Internally-Generated or Externally-Supplied Master Clock

General Description

The CDB501X is an evaluation board that eases the laboratory characterization of any of the CS501X or CSZ511X A/D converters. The board can be easily reconfigured to simulate any combination of sampling, master clock, calibration, and input range conditions.

The converter's parallel output data and several control inputs and outputs are available at a 40 pin strip header allowing easy interfacing to PC's or microprocessor busses. Output data is also available in serial form at SCLK and SDATA coaxial BNC connectors.

Evaluation can also be performed over a wide range of input spans using the on-board reference circuitry. Furthermore, the CDB501X features DIP-switch selectable unipolar/bipolar input ranges and two calibration modes: burst and interleave cal. Calibration can be initiated at any time on the CDB501X by momentarily depressing a reset pushbutton.



CS501X=CS5012, CS5014, or CS5016
CSZ511X=CSZ5112, CSZ5114, or CSZ5116

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Analog Input

The analog input to the A/D converter is supplied through the BNC coaxial connector labeled AIN. Analog input polarity is controlled by the first position switch on the DIP-switch, SW-1. If it is on, the input is unipolar ranging from GND to VREF. If the switch is off, the input range is bipolar with the magnitude of the reference voltage defining both zero- and full-scale (±VREF).

The A/D converter's internal analog input buffer requires a source impedance of less than 400 Ω at 1MHz for stability. Acquisition and throughput are specified assuming a dc source impedance of less than 200 Ω. Infinitely large dc source impedances can be accomodated by adding capacitance (typically 200pF) from the analog input to ground. However, high dc source resistances degrade acquisition time and consequently throughput.

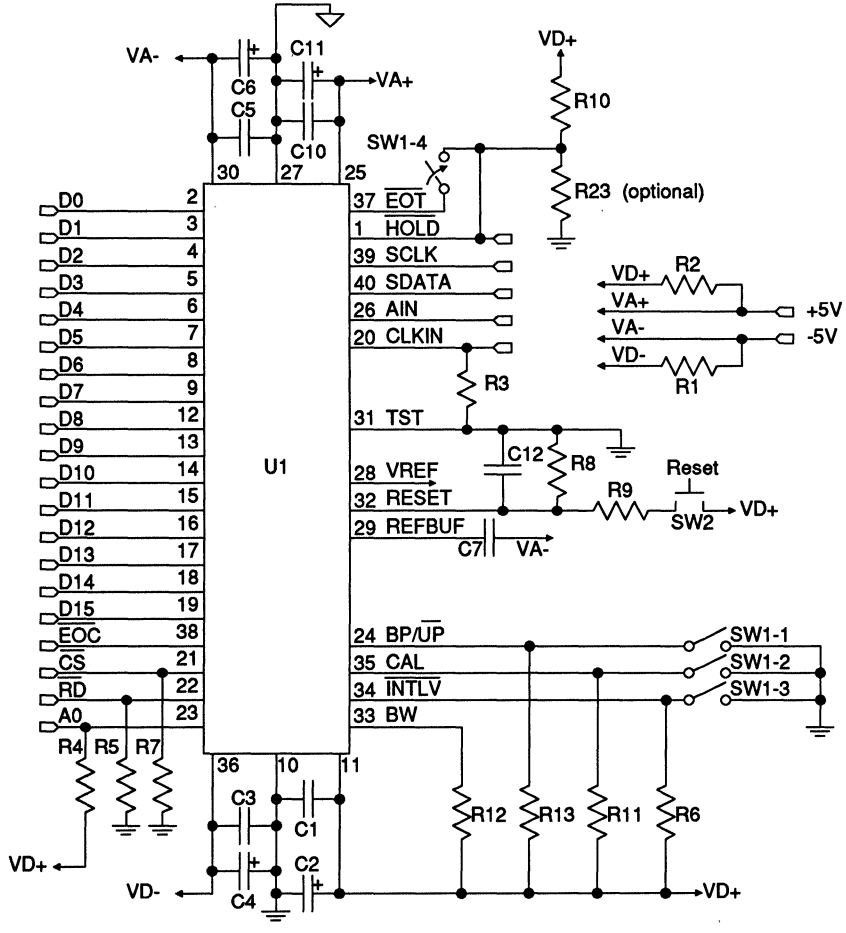


Figure 1. CDB501X Schematic
(Reference Circuitry Appears in Figure 3)

	OFF	ON
Position 1	Bipolar	Unipolar
Position 2	Burst Cal	Normal Operation
Position 3	Normal	Interleaved Cal
Position 4	Normal	Continuous Conversion

Figure 2. DIP-Switch Definitions

Initiating Conversions

A negative transition on the converter's $\overline{\text{HOLD}}$ pin places the device's analog input into the hold mode and initiates a conversion cycle. On the CDB501X, this input can be generated by one of two means. First, it can be supplied through the BNC coaxial connector appropriately labeled $\overline{\text{HOLD}}$. Alternatively, switch position 4 of the DIP-switch can be placed in the on position, thus looping the converter's $\overline{\text{EOT}}$ output back to $\overline{\text{HOLD}}$. This results in continuous conversions at a fraction of the master clock frequency (see "synchronous operation" in the converter's data sheet).

The A/D converter's $\overline{\text{EOT}}$ output is an indicator of its acquisition status; it falls when the analog input has been acquired to the specified accuracy. If an external sampling clock is applied to the $\overline{\text{HOLD}}$ BNC connector, care must similarly be taken to obey the converter's acquisition and maximum sampling rate requirements. A more detailed discussion of acquisition and throughput can be found in the converter's data sheet.

The CDB501X is shipped from the factory without the $\overline{\text{HOLD}}$ BNC input terminated for operation with an external sampling clock. However, location R23 is reserved for the insertion of a 51 Ω resistor to eliminate reflections of the incoming clock signal.

Voltage Reference Circuitry

The CDB501X features an adjustable voltage reference which allows characterization over a wide range of reference voltages. The circuitry consists of a 2.5V voltage reference (1403) and an adjustable gain block with a discrete output stage (Figure 3). The output stage minimizes the output's headroom requirements allowing the reference voltage to come within 300mV of the positive supply.

The coarse and fine trim potentiometers are factory calibrated to a reference voltage of 4.5V (a table of output code values for a reference voltage of 4.5V appears in the CS501X data sheets, but not in the CSZ511X data sheets). When calibrating the reference, the voltage should be measured directly at the VREF input (pin 28) or at the ungrounded lead of decoupling capacitor C9.

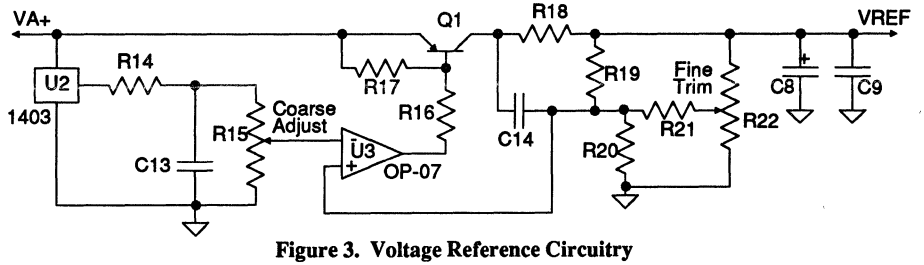


Figure 3. Voltage Reference Circuitry

Reset/Self-Calibration Modes

The A/D converter will usually reset itself upon power-up. Since this function is not guaranteed, the converter must be reset upon power-up in system operation. The converter can be reset on the CDB501X board by momentarily depressing pushbutton SW-2 thus initiating a full calibration cycle; 1,443,840 master clock cycles later the converter is ready for normal operation.

The converters also feature two other modes of calibration: burst and interleave. Burst calibration can be initiated by moving switch position 2 on the DIP-switch to the off position. In this mode (CAL high), the A/D converter continually loops through calibration cycles until CAL returns low. Interleave can be initiated by setting switch position 3 to the on position. In the interleave mode ($\overline{\text{INTRLV}}$ low), the converter appends one small portion of a calibration cycle (20 master clock cycles) to each conversion cycle. Thus, a full calibration cycle completes every 72,192 conversion cycles.

A more detailed discussion of the converters' calibration modes and capabilities can be found in their data sheets.

Parallel Output Data/Microprocessor Interface

The converter's outputs D0-D15, its $\overline{\text{CS}}$, $\overline{\text{RD}}$, and A0 inputs, and its $\overline{\text{EOC}}$ output are available at the 40 pin header. The $\overline{\text{CS}}$ and $\overline{\text{RD}}$ inputs are pulled low through 10 kΩ resistors placing the converter in a microprocessor-independent mode. Control input A0 is pulled up, insuring the converter's output word, rather than the status register, appears at the header.

The converter's 3-state output buffers and microprocessor interface can be exercised by driving the $\overline{\text{CS}}$ and/or $\overline{\text{RD}}$ inputs at the header. Similarly, the converter's 8-bit status register can be obtained on D0-D7 by driving A0 low.

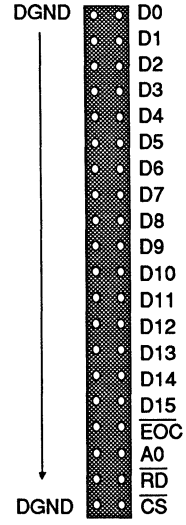


Figure 4. Header Pin Definitions

The converter's $\overline{\text{EOC}}$ and data outputs are not buffered on the CDB501X. Therefore, careful attention should be paid to the load presented by any cabling, especially if the 3-state output buffers are to be exercised at speed. Twisted ribbon cable is typically specified at 10pF/ft, so several feet can generally be accomodated.

Serial Output Data

Serial output data is available at the two BNC connections SCLK and SDATA. Data appears MSB first, LSB last, and is valid on the rising edge of SCLK.

Master Clock

The A/D converter operates from a master clock which can either be internally-generated or externally-supplied. For operation with an external clock, the BNC connector labeled CLKIN should be driven with a TTL clock signal. The CDB501X is shipped from the factory with the CLKIN input terminated by a 51 Ω resistor to eliminate line reflections of the incoming clock.

If the CLKIN BNC input is left floating, this resistor pulls the converter's clock input down to ground, thus activating its internal oscillator.

Decoupling

The CDB501X's decoupling scheme was designed to insure accurate evaluation of the converter's performance independent of the quality of the power supplies. Each supply is decoupled at the converter with a 10µF electrolytic capacitor to filter lowfrequency noise and a 0.1µF ceramic capacitor to handle higher frequencies. The auto-zeroing action of the converter's comparator provides extremely good power supply rejection at low frequencies. Depending on the quality of the system's power supplies, the decoupling scheme could be relaxed in actual use.

COMPONENT LIST

10 Ω resistor	R1, R2
51 Ω resistor	R3
4.7 Ω resistor	R18
1 kΩ resistor	R9, R14
560 Ω resistor	R17
10 kΩ resistor	R4, R5, R6, R7, R8, R10, R11, R12, R13
2.43 kΩ resistor	R19, R20
3.3 kΩ resistor	R16
240 kΩ resistor	R21
50 kΩ potentiometer	R15
50 kΩ potentiometer	R22
0.068 µF capacitor	C14
0.1 µF capacitor	C1, C3, C5, C7, C9, C10, C12
10 µF capacitor	C2, C4, C6, C8, C11, C13
CS501X/511X A/D converter	U1
1403 2.5V reference	U2
OP07 op amp	U3
2N2907A transistor	Q1
4 pos. SPST DIP switch	SW1
N.O. SPST pushbutton	SW2
20 pin header	CON1
bulkhead BNC	CON2, CON3, CON4, CON5, CON6
red banana jack	CON7
black banana jack	CON8
green banana jack	CON9
1" 4-40 spacer	POST1, POST2, POST3, POST4, POST5, POST6
3/8" 4-40 screw	SC1, SC2, SC3, SC4, SC5, SC6

• Notes •

Semiconductor Corporation

CDB5316

CSZ5316 Evaluation Board

Features

- Easy To Use Digital Interface
  Parallel 16 Bits With Clock
  Serial Output With Clock
- On-Board Clock Generation
  19.2 KHz Output Rate
- Industry Standard Header Connector
  IDC Connector used to access
  Parallel Data, Serial Data, and
  Clock

General Description

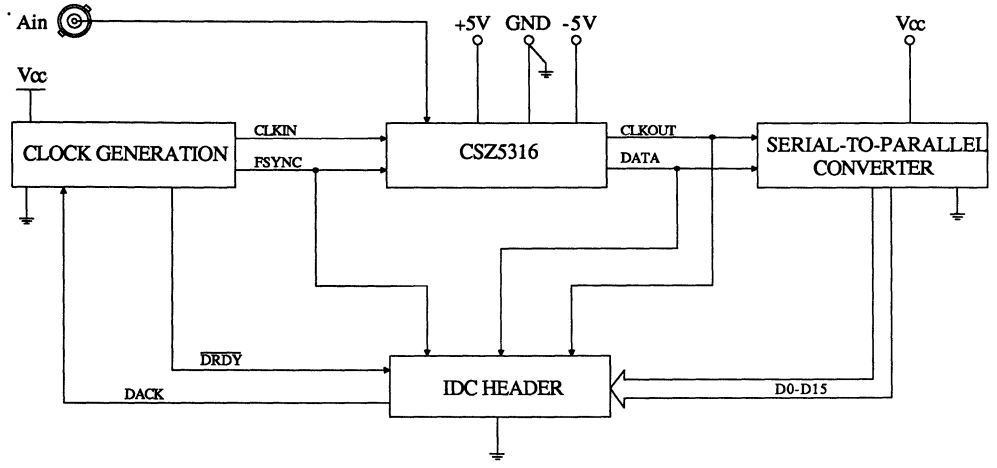
The CDB5316 Evaluation Board is designed to allow the user to quickly evaluate the performance of the CSZ5316 Delta-Sigma Analog-to-Digital Converter. All that is required to use this board is an external power supply, a signal source and an ability to read either serial or parallel 16 bit data words.

Note: The CSZ5316 was formerly designated as the CS5316

ORDERING INFORMATION

CDB5316

Block Diagram



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GENERAL DESCRIPTION

The CDB5316 Evaluation Board is a stand-alone environment for easy lab evaluation of the CSZ5316 Delta-Sigma Analog-to-Digital Converter. Included on the board is the clock generation circuitry needed to drive the CSZ5316 and a serial-to-parallel converter which allows the user to access the data in either a parallel or serial mode. When supplied with the necessary +5 volts and -5 volts power supplies and an analog signal source, the CDB5316 will provide converted data at the 40 pin header.

Suggested Evaluation Method

An efficient evaluation of the CSZ5316 using the CDB5316 may be accomplished as described below.

Equipment needed consists of the following:

- The CDB5316 Evaluation Board
- A power supply capable of supplying +5V and
- 5V
- A spectrally pure sine wave generator such as the KrohnHite Model 4400A "Ultra-Low Distortion Oscillator"
- A PC equipped with a digital data acquisition board such as the Metrabyte Model PIO12 "24 Bit Parallel Digital I/O Interface"
- A software routine to collect the data and perform a Fast Fourier Transform (FFT)

The set-up is straightforward. Use the sine-wave generator to supply the analog signal to the CDB5316. Converted data will then appear at the header on the CDB5316. The header should be connected to the digital data acquisition board in the PC through an IDC 40 pin connector and cable. The software routine should collect the data from the CDB5316 and run a standard 1024 point Fast Fourier Transform (FFT). Such an analysis results in a plot similar to Figure 1 using a 1kHz input signal and a Blackman-Harris window for the FFT.

The signal to noise and signal to total harmonic distortion characteristics of the CSZ5316 may be easily measured in this way. The signal to total harmonic distortion value for a particular input is the ratio of the RMS value of the input signal and the sum of the RMS values of the harmonics shown in the diagram. The dynamic range of the CSZ5316 can be measured by reducing the input amplitude so that distortion products become negligible. This allows an accurate measurement of the noise floor.

More complex analysis such as intermodulation distortion measurements can be accomplished with the addition of more wave form generators.

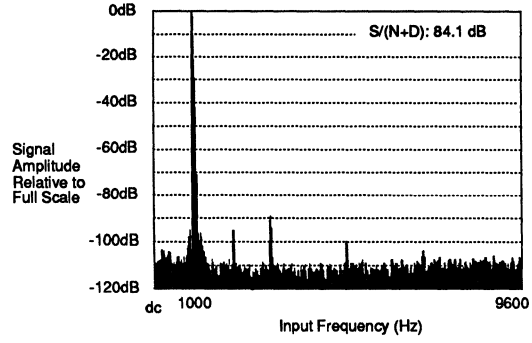


Figure 1. - FFT Plot Example

Power Supplies

The power supply connections are fairly straight forward. A tracking split supply should be used to generate +5 volts and -5 volts. These should be connected to their respective inputs. A good quality low ripple, low noise supply will give the best performance. The +5 volt supply can also be used for VCC and should be connected between the VCC board jack and the power supply, as opposed to connecting the VCC jack straight to the +5V jack. The +5V jack is the positive power source for the CSZ5316 IC whereas the VCC jack supplies power to all the digital IC's. Care should be taken that noise is not coupled between VCC and +5V; however, supply noise is

generally not a problem with the CSZ5316 since the on-chip decimation filter will remove any interference outside of its passband (9.6kHz).

CIRCUIT DESCRIPTION

Clock Generation

The time base for the CDB5316 is a 4.9152 MHz crystal oscillator as shown in Figure 1. A clock source may be input at the CLKIN BNC connector to override the crystal oscillator. The clock is divided by 256 through two four bit binary ripple counters and re-aligned by a D Flip-Flop. The result is the necessary master clock (4.9152 MHz, CLKIN) and the frame synchronization signal (19.2 kHz, FSYNC). If an external clock source is used, FSYNC will be the clock source divided by 256. Figure 2 depicts the clock generation circuitry.

Two optional handshaking signals are shown with the clock generation circuitry. These signals are Data Ready ($\overline{\text{DRDY}}$) and Data Acknowledge (DACK). $\overline{\text{DRDY}}$ makes a transition low with the falling edge of FSYNC indicating that parallel data is available. $\overline{\text{DRDY}}$ is reset high when DACK returns to a high state. The Parallel Data Timing diagram, Figure 6, illustrates the operation of $\overline{\text{DRDY}}$ and DACK with the arrows indicating control of each edge of $\overline{\text{DRDY}}$. If DACK is not driven, it will be held high by a pull-up driving $\overline{\text{DRDY}}$ continuously high. These signals are designed for parallel I/O cards that

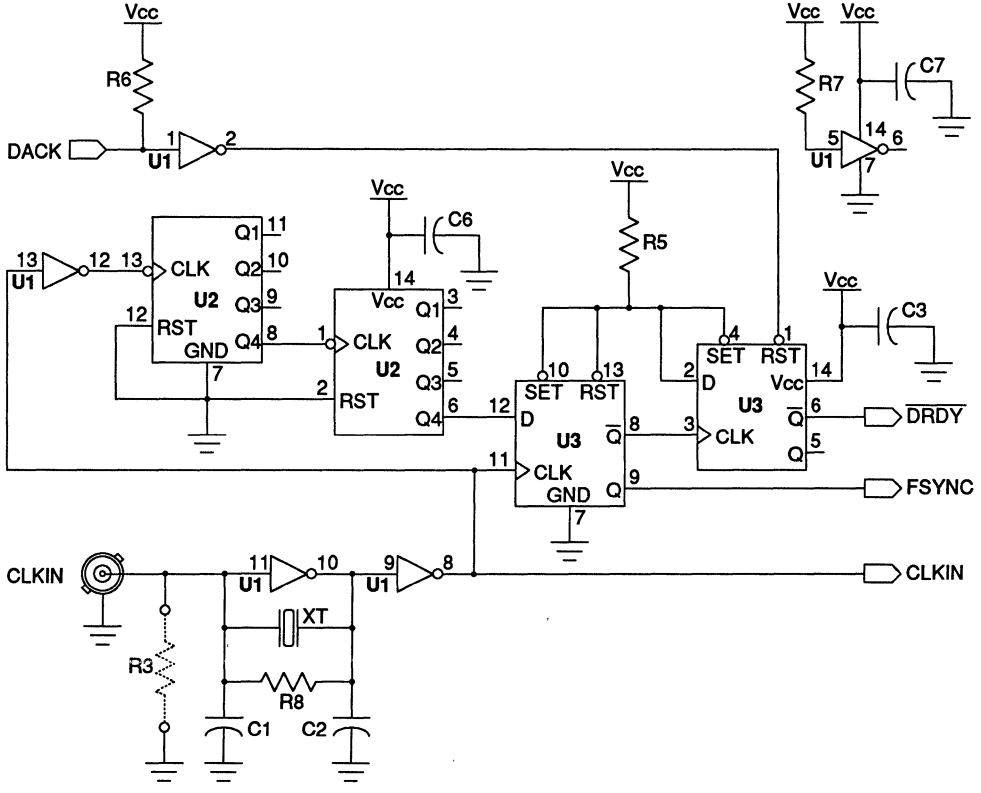


Figure 2. - Clock Generation Circuitry

support this type of handshaking such as the MetraByte PIO12 Interface Card designed for use in an IBM PC.

Analog-To-Digital Conversion

The analog-to-digital conversion is handled by the CSZ5316 which is shown in Figure 3 as U6. The signal level at AIN should not exceed the values indicated in the CSZ5316 Data Sheet. Antialiasing requirements are a function of AIN's bandwidth and out-of-band energy. A full discussion can be found in Application Note "Antialiasing Considerations for the CSZ5316". Once the data is converted, it will be output to both the serial-to-parallel converter and the IDC header. The data is output from the CSZ5316 as a 16-bit burst of serial information with a data rate of 2.4576 MHz (clock source divided by 2) and a burst rate of 19.2 kHz (FSYNC rate). The burst starts after the rising edge of FSYNC. Figure 4 illustrates serial data timing but for more detailed timing information see the CSZ5316 data sheet.

Serial-To-Parallel Conversion

The serial-to-parallel conversion is handled by a pair of 8-bit serial-to-parallel converters that are chained to handle the full 16-bit data word as shown in Figure 6. The serial data from the CSZ5316 is clocked into the converters with

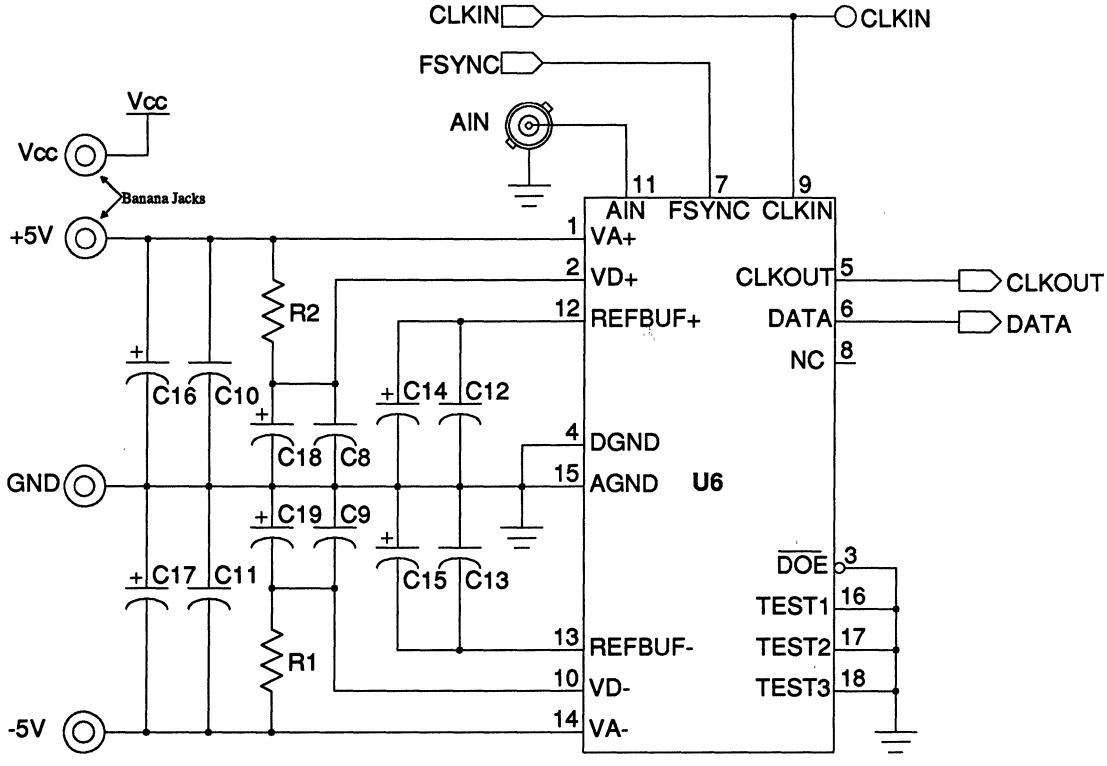
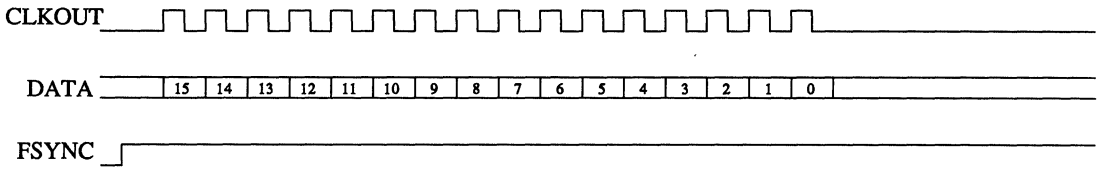


Figure 3. - Analog-to-Digital Converter



Note: For a complete description of serial timing see the CSZ5316 Data Sheet

Figure 4. - Serial Data Timing

CLKOUT. The output is always available so, as the data is being clocked in, the information at the parallel interface will be changing. This data will change in a period that starts following the rising edge of FSYNC and lasts for about 6.5 microseconds. The data is always stable when FSYNC is low and for this reason data should only be considered valid when FSYNC is low. Figure 5 illustrates when parallel data is valid and the operation of the handshaking signals. $\overline{\text{DRDY}}$ is output from the CDB5316 indicating parallel data is valid and DACK is used to reset $\overline{\text{DRDY}}$ acknowledging that data has been received. FSYNC may be used instead of $\overline{\text{DRDY}}$ if no acknowledgement signal is used.

Both serial and parallel outputs are available through the 40 pin header which can be used with a standard IDC connector that has two rows of 20 pins spaced 0.100" apart.

Components

Table 1 below lists the major components on the CDB5316 Evaluation Board. All integrated circuits that are attached to the IDC header are socketed as a precaution. Since the IC's used are CMOS, standard CMOS precautions should be observed when handling the Evaluation Board. Figure 7, A bird's eye view of the CDB5316 Board, will help in locating component positions.

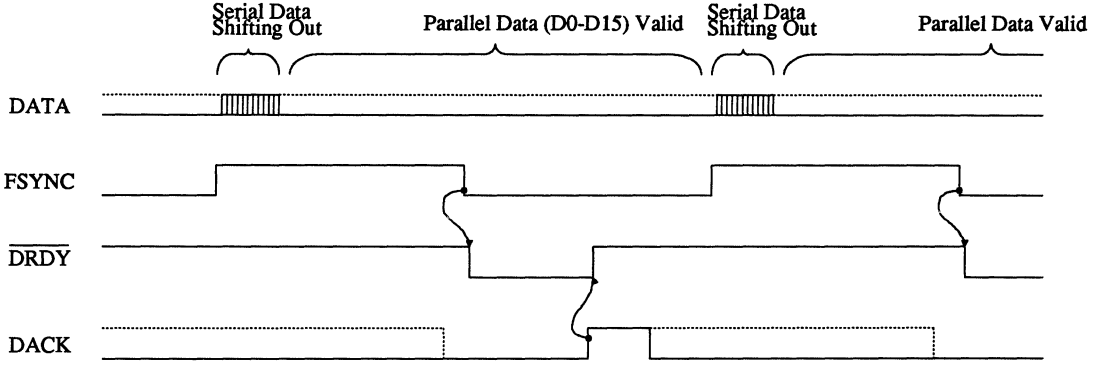


Figure 5. - Parallel Data Timing

Mnemonic	Part Description	Comments
U1	74HCU04 - Octal Buffer	
U2	74HCT393 - Ripple Counter	
U3	74HCT74 - Dual D Flip-Flop	
U4, U5	74HCT299 - Shift Register	
U6	CSZ5316 - Delta-Sigma ADC	
C1, C2	22 pF Capacitors	Crystal Loading
C3-C13	0.1 uF Capacitors	High Frequency Decoupling
C14-C19	10 uF Capacitors	Low Frequency Decoupling
R1, R2	10 ohm Resistors	Power Supply Decoupling
R3	51 ohm Resistor	Impedance Matching - optional, not supplied
R4-R7	22 kohm Resistors	Pull-ups
R8	10 Mohm Resistor	Crystal Loading
XT	4.9152 MHz Crystal	

Table 1. - Parts List

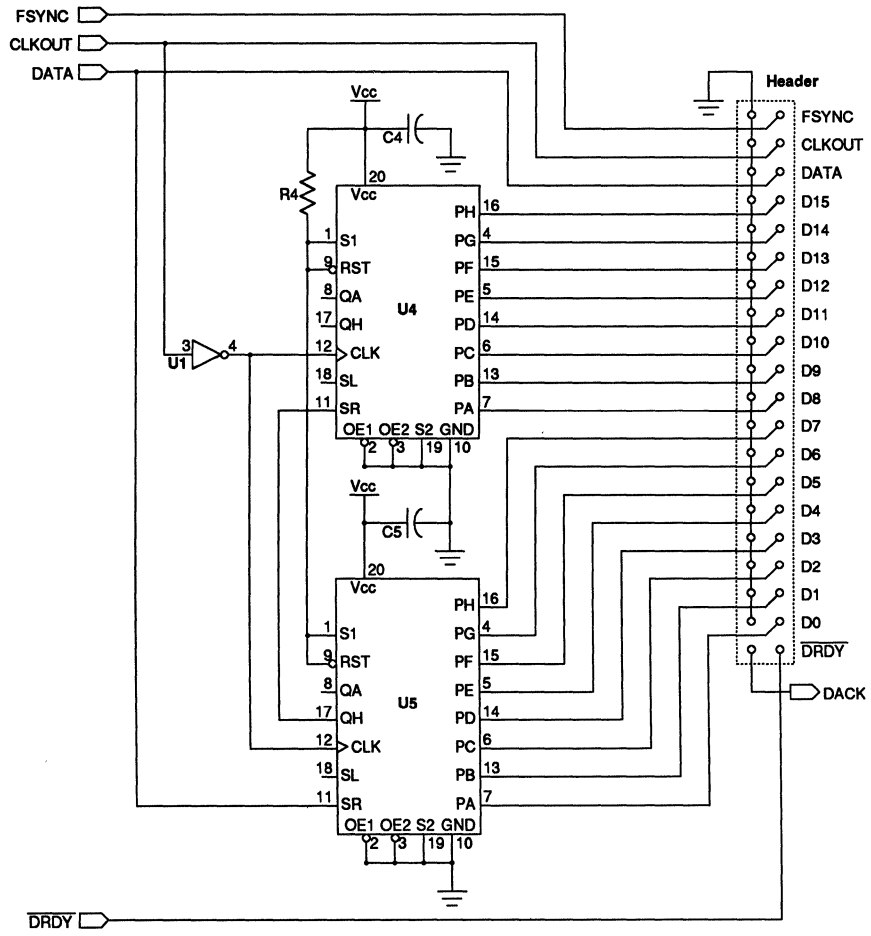


Figure 6. - Serial-to-Parallel Converter

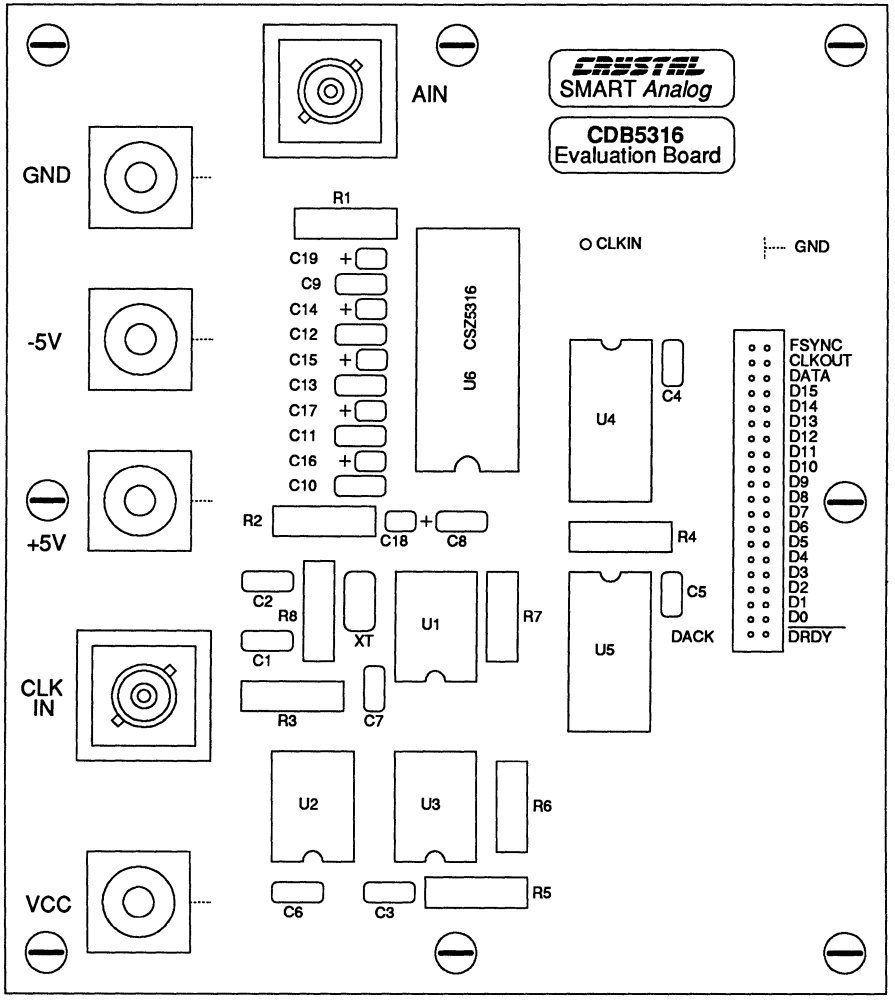


Figure 7. - Bird's Eye View

• Notes •

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CDB5412

CSZ5412 Evaluation Board

Features

- Throughput Rates up to 1 MHz
- PC/uP-Compatable Header Connection
- Buffered 12-Bit Data
- Jumper Selectable:
  - Unipolar/Bipolar Input Range
  - Continuous Convertion
- Adjustable Voltage Reference
- Operation from On-Board Crystal or Externally-Supplied Master Clock

General Description

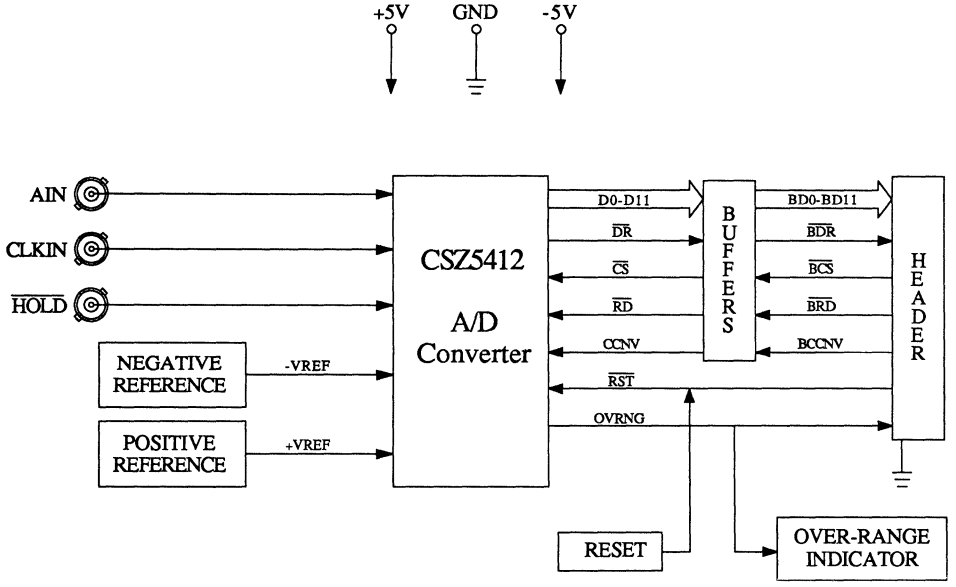
The CBD5412 is a completed, tested evaluation board for the CSZ5412 12-bit high-speed analog-to-digital converter. It includes a socketed CSZ5412, and all of the components necessary to quickly and thoroughly verify converter performance under a wide variety of operating conditions.

On board circuitry includes voltage references and clock circuitry, plus data buffers, so that the user need only suppy power, and an input signal to exercise the CSZ5412.

ORDERING INFORMATION

CDB5412

Block Diagram



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• Notes •

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CDB61534

PCM Line Interface Demonstration Board

Features

- Socketed CS61534
- Complete Line Interface Function
- Slide Switch Control of Digital Inputs
- Reset Circuit
- Mode Selection Circuit

General Description

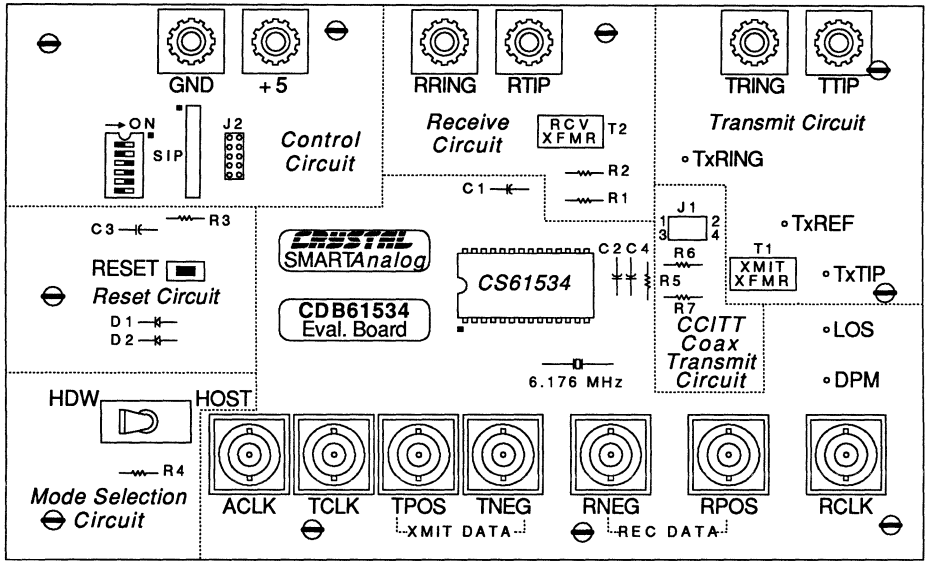
The board comes with a socketed CS61534 IC plus all the discretes required so that the CS61534's performance can be verified in the lab without having to first build a breadboard.

The board has four banana connectors for connecting two 100-to-120 ohm twisted pair cables to the line transformers present on the board. Two other banana connectors allow for easy connection of an external five volt power supply. Power supply decoupling capacitors are resident on the board. BNC connectors allow easy access to the Received Clock and Data, the Transmit Clock and Data, and the Alternate Clock. Testing terminals provide access to the Serial Control Interface, DPM, MTIP, MRING, TTIP, TRING, LOS and center tap of the transmit transformer.

Additional components provided on the board are a crystal, a reset circuit and a DIP switch for controlling the input pins: LEN0, LEN1, LEN2, TAOS, RLOOP and LLOOP.

ORDERING INFORMATION
CDB61534

BOARD LAYOUT



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CIRCUIT DESCRIPTION

The CDB61534 PCM Line Interface Demonstration Board is an evaluation tool for the CS61534. The board allows the CS61534 to be evaluated with no further breadboarding required. The CDB61534 comes with two crystals: a 6.176 MHz crystal installed for T1 operation and a 8.192 MHz crystal which can be installed for CCITT operation. Alternatively, a clock of four times the TCLK frequency can be input to XTALIN, disabling the jitter attenuator (4xCLOCK must have the same phase as TCLK).

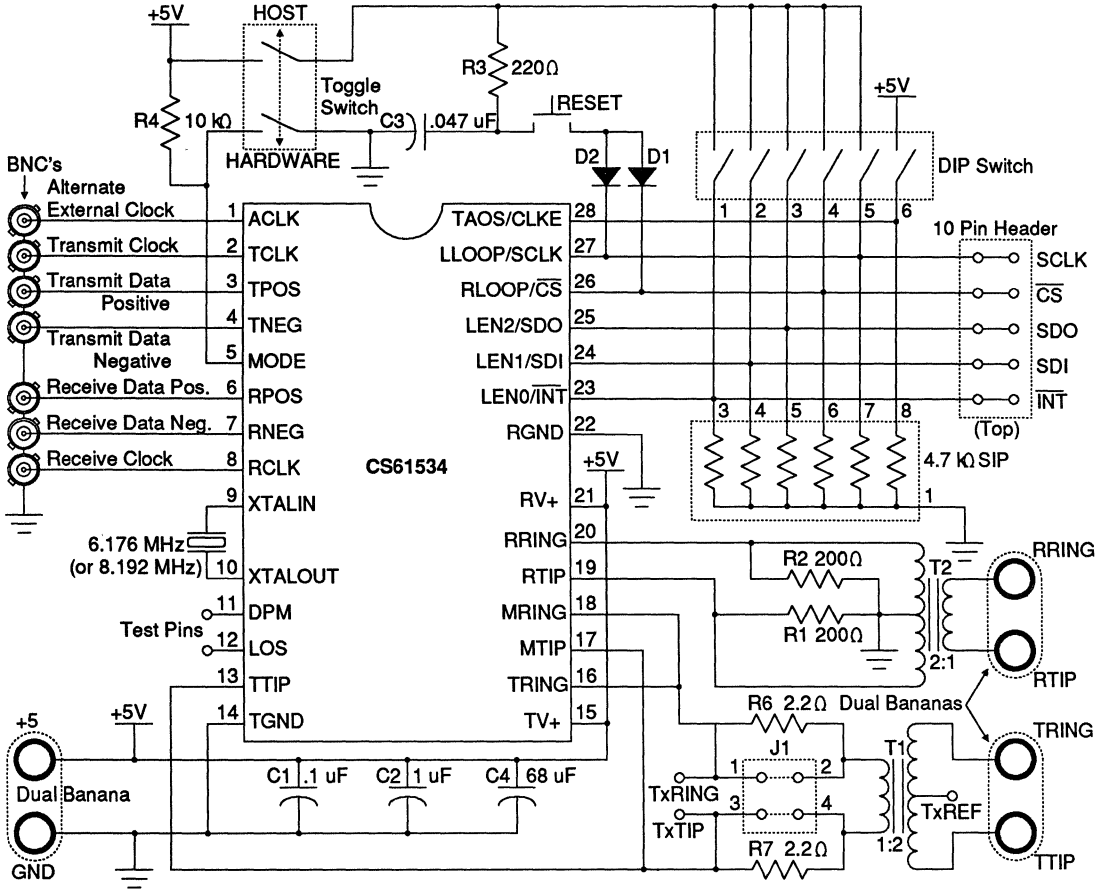

Figure 1. CDB61534 Schematic

Transmit Circuit

The transmit circuit consists of a 1:2 step-up transformer (T1) and banana connectors (TTIP and TRING) for terminating a twisted pair. This circuit is activated by connecting pin 1 to pin 2, and pin 3 to pin 4 on pin header J1.

Additional circuitry is provided to support interfacing to a CCITT coax line (75Ω load, and 2.37V pulse height). This circuit uses two 2.2Ω resistors (R6 and R7) to control pulse amplitude, and is activated by removing the jumpers from pin header J1.

TxTIP and TxRING can be used to directly access pins 13 and 16 of the CS61534. TxREF allows access to the center tap (line side) of the transmit transformer.

Receive Circuit

The receive circuit consists of a center-tapped transformer (T2) and banana connectors (RTIP and RRING) for connecting the receive twisted pair. Resistors R1 and R2 provide a proper termination load for twisted pair applications, and should be replaced by 150Ω resistors for 75Ω CCITT coax cable applications.

Power Supply

The power supply circuit consists of two banana connectors (GND and +5) for connecting to ground and plus five volts. A 0.1µF decoupling capacitor (C1) is supplied for the receive power pins. 1.0µF and 68µF capacitors (C2 and C4) are supplied for the transmit power supply.

Mode Selection Circuit

The Mode Selection circuit controls pin 5 of the CS61534, and selects between host mode and hardware mode. The circuit consists of a toggle switch and a 10kΩ resistor (R4).

RESET Circuit

The RESET circuit consists of a switch, two diodes (D1, D2), a capacitor (C3) and a resistor (R3). When in the hardware mode and the switch is pushed, the RLOOP and LLOOP pins are momentarily pulled high. RESET is invoked in the host mode by writing a command over SDI.

Control Circuit -Hardware Mode Operation

The control circuit consists of a set of 6 DIP slide switches which control pins 23 through 28 of the CS61534 as shown in Table 1. Turning a switch on provides a 5 Volt signal to the corresponding pin.

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Switch	CS61534 Pin Affected	Switch Position	
		On (right, toward center of board)	Off (left, toward edge of board)
1	LEN0 (23)	Logic High	Logic Low
2	LEN1 (24)		
3	LEN2 (25)		
4	RLOOP (26)	Loopback selected	Loopback not selected
5	LLOOP (27)		
6	TAOS (28)	Transmit all 1's to the line	Normal transmission

Table 1. Switch Position Interpretation

Control Circuit -Host Mode Operation

The serial bus pins of the CS61534 are accessed by connecting to the 10 pin header. Each pin on one side of the header is connected to the adjacent pin on the other side. The DIP slide switch is still used to control CLKE (pin 28). Placing the CLKE slide in the on position (right, toward the edge of the board), gives RCLK and SCLK polarity compatible with the DS2180. When CLKE is in the off position (left, toward the center of the board), RCLK has the same polarity as in the hardware mode (R8070 compatibility). All of the other DIP switches are disabled in the host mode.

WATCH OUT! Do not switch the board to the hardware mode when it is connected to your serial interface. If any of the dip switches are on, the power supply will be connected to your serial interface, potentially damaging its output circuits.

EVALUATION HINTS

1. A 100Ω load should be connected to the TTIP and TRING banana connectors when evaluating the transmitted signal.

2. When externally implementing a loopback by connecting RPOS/RNEG to TPOS/TNEG and RCLK to TCLK, be sure to insert an inverter between RCLK and TCLK (i.e., when in the hardware mode, or when in the host mode and CLKE is low).

3. If an excessive amount of ringing is experenced at TTIP/ TRING due to the transmit transformer, try inserting a 100Ω resistor at the R5 location.

Semiconductor Corporation

CDB61544

PCM Line Interface Demonstration Board

Features

- Socketed CS61544
- Complete Line Interface Function
- Slide Switch Control of Digital Inputs
- Reset Circuit

General Description

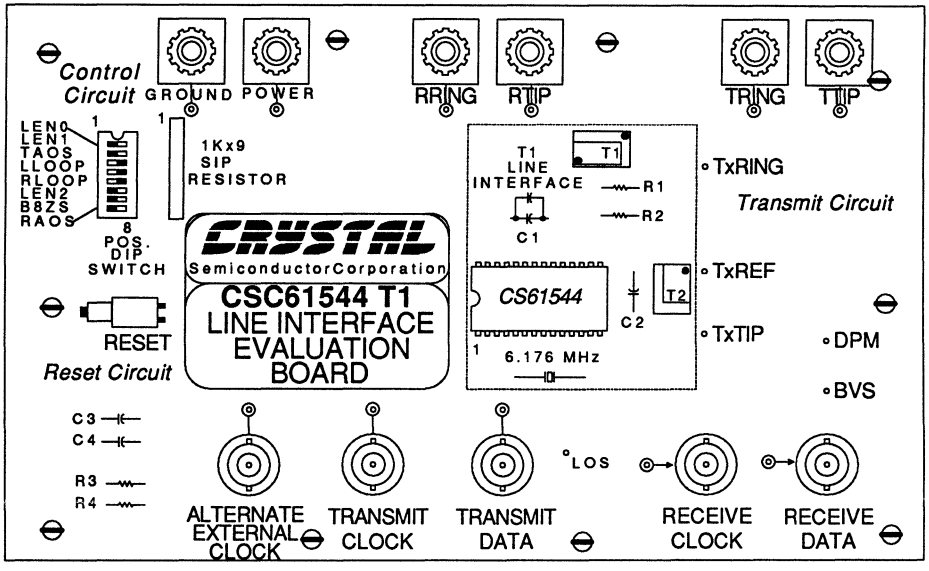
The board comes with a socketed CS61544 IC plus all the discretes required so that the CS61544's performance can be verified in the lab without having to first build a breadboard.

The board has four banana connectors for connecting two 100 ohm twisted pair cables to the line transformers present on the board. Two other banana connectors allow for easy connection of an external five volt power supply. Power supply decoupling capacitors are resident on the board. BNC connectors allow easy access to the Received Clock and Data, the Transmit Clock and Data, and the Alternate Clock. Testing terminals provide access to DPM, MTIP, MRING, TTIP, TRING, LOS and center tap of the transmit transformer.

Additional components provided on the board are a crystal, a reset circuit and a DIP switch for controlling the input pins: LEN0, LEN1, LEN2, TAOS, RLOOP, LLOOP, B8ZS AND RAOS.

ORDERING INFORMATION
CDB61544

BOARD LAYOUT



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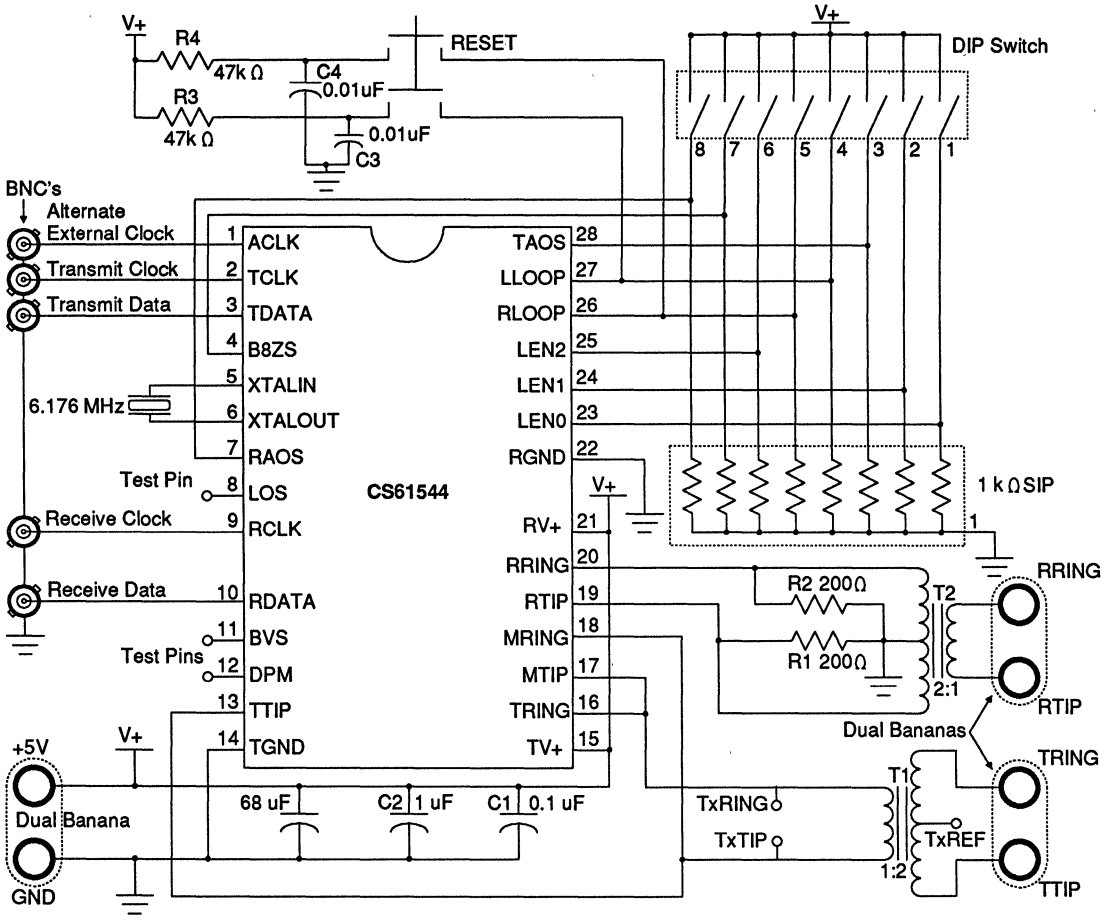
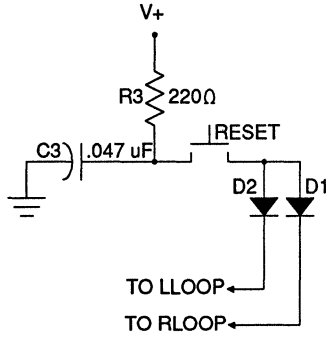
Crystal Semiconductor Corporation
P.O. Box 17847, Austin, Texas 78760
(512)445-7222 TWX:910-874-1352





NEW AND IMPROVED RESET CIRCUIT

(NOT PROVIDED, BUT RECOMMENDED FOR SIMILAR DESIGNS)

Semiconductor Corporation

CDB7008

CS7008 Evaluation Board

Features

- Up to 64 Different Filters On-Board
- Optional Input Antialiasing Filter
- Optional Output Smoothing Filter
- Operation from On-Board Crystal or Externally-Supplied Clock
- Supports CRYSTAL-ICE Filter Development System

General Description

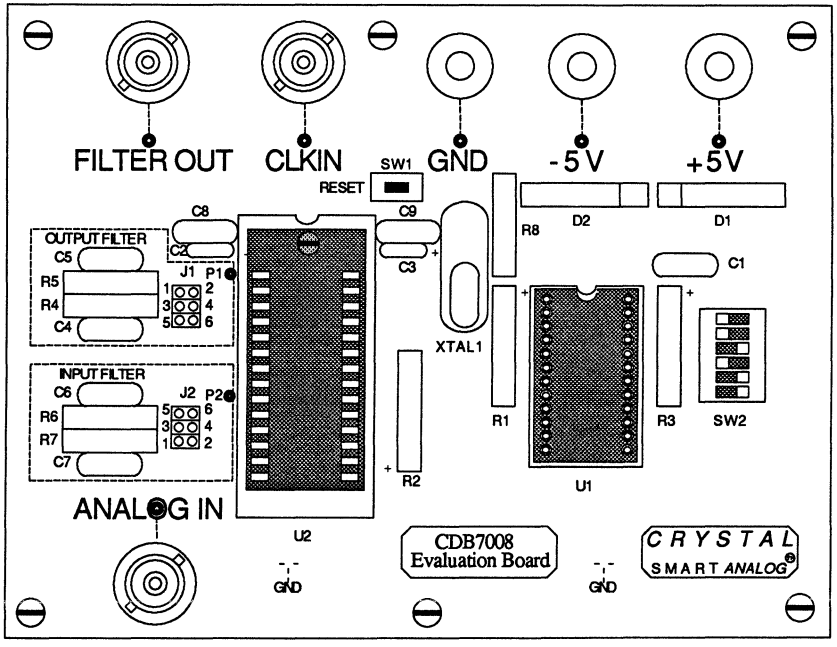
The CDB7008 allows the user to quickly verify the performance of the CS7008 Universal Filter under a wide variety of operating conditions. The on-board EPROM contains a large variety of filters that are DIP switch selectable and loaded into the CS7008 when RESET is pressed.

Jumpers on the input and output filters can be configured to provide antialiasing and smoothing, or the filters can be bypassed altogether.

ORDERING INFORMATION

CDB7008

Board Layout



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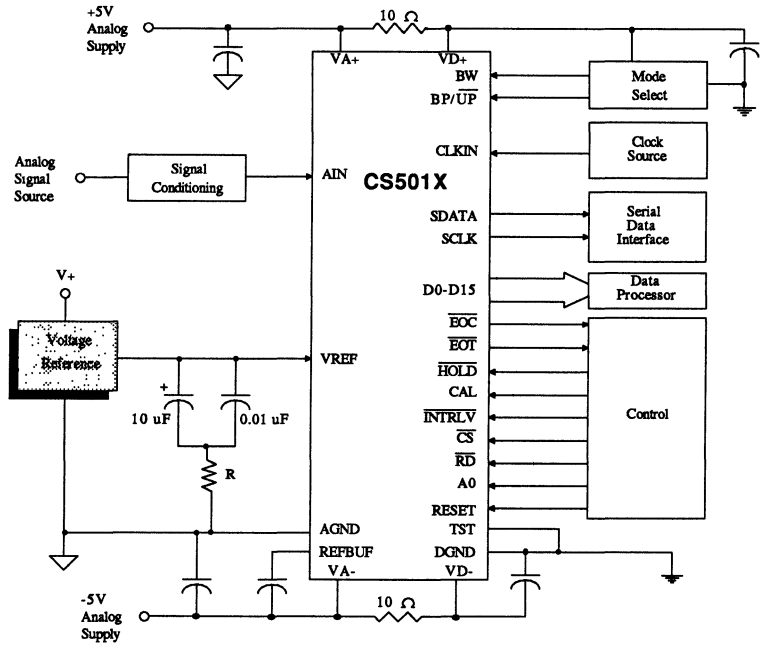
• Notes •

CONTENTS

Application Note

Voltage References for the CS501X / CSZ511X Series of A/D Converters

by
Bruce Del Signore



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INTRODUCTION

This application note discusses voltage references for use with Crystal Semiconductor's CS501X series of A/D converters and CSZ511X series of S-to-Z converters™. Reference design considerations, a design example and suggested reference circuits are explained in detail.

Voltage references provide accurate voltages for use in data acquisition systems in order to establish a basis for conversion. In a data acquisition system, the value of the reference sets the gain of the A/D stage since the digital output corresponds to the ratio of the analog input signal to the reference voltage.

In static applications, information is contained in the signal amplitude, therefore the absolute value of the reference voltage is important. In many signal processing applications, information is contained in the frequency and phase of the signal. Here, absolute value is not as important as the stability of the reference voltage during conversion.

Zener-diode Reference

There are two major varieties of voltage references. The first is the zener-diode based reference which uses a reverse-biased zener diode operated in its breakdown region. Most zeners breakdown at voltages of about 6.0V which limits the minimum supply voltage necessary for operation. When the diode is supplied with a constant current, it has a constant voltage drop. Zener references use a zener diode and an integrated feedback amplifier which provides constant current, gain, and buffering for the zener diode.

Zener diodes exhibit two types of breakdown. The first is zener breakdown which has a negative temperature coefficient and is dominant at low current levels. The second, avalanche breakdown, occurs at higher current levels and has a positive temperature coefficient. At some specific current level, these two effects cancel each other and the temperature coefficient of the zener breakdown voltage is zero. As the ambient temperature changes, one of the breakdown mechanisms becomes dominant and the the reverse-biased diode voltage will exhibit a temperature coefficient.

Bandgap Reference

The second major type of reference is the bandgap reference. This reference uses the base-emitter voltage (V_{be}) of a bipolar transistor as a basis for operation. The V_{be} has a negative temperature coefficient (-2mV/°C). This negative temperature coefficient is balanced by a voltage with a positive temperature coefficient of the same magnitude. This voltage is usually obtained by using the difference of two V_{be}'s of transistors operating at different current densities. When both voltages are scaled and summed together, the result is a voltage which is less sensitive to temperature. The headroom required for bias and support circuitry is only a few volts over the output voltage.

Reference Specifications

Voltage references have six important specifications. These are absolute accuracy, temperature coefficient, long-term reference drift, power supply sensitivity, output impedance, and output noise.

Absolute or untrimmed accuracy is the difference between the actual output voltage and the ideal output voltage. It is specified in millivolts.

Temperature coefficient describes the drift in the output voltage with temperature. Since this drift is nonlinear, curve fitting is often used for all temperatures between those actually tested. Voltage references are available with temperature coefficients as low as 1 ppm/°C. Inexpensive

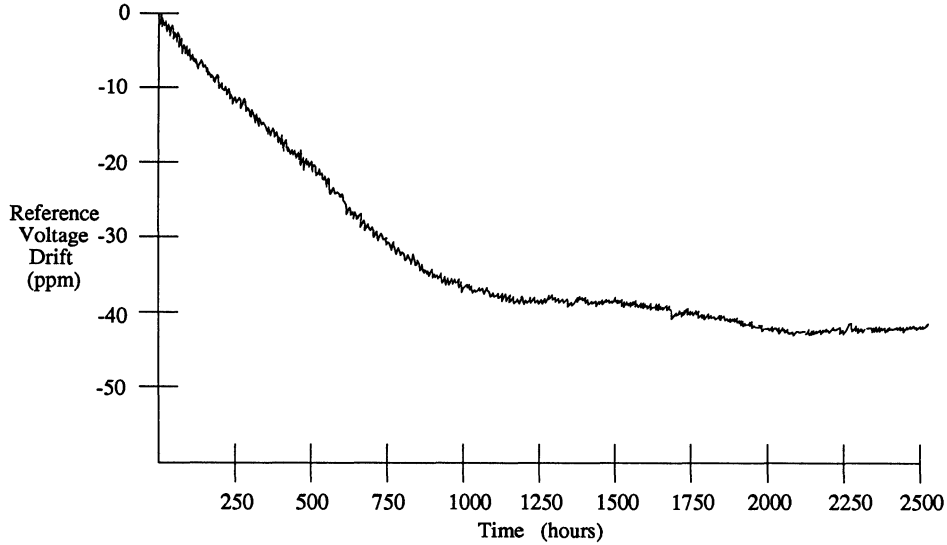


Figure 1. - Long Term Stability of a Typical Zener Reference

references are available with 10 to 50 ppm/°C drift which is comparable to on-chip references of bipolar A/D converters. Temperature coefficient is specified in ppm/°C.

Long term stability is the drift in the reference voltage over time. Most references show minor deviations in voltage due to 1/f noise in circuit components. These deviations are usually small and are superimposed on a larger drift characteristic which is due to device aging. An example of this is seen in Figure 1. Long term drift is specified in ppm/1000 hrs.

Power supply sensitivity (line regulation) is the change in output voltage due to a change in power supply. Most references have good power supply rejection at dc, but ac power supply rejection is also important when power supplies are subject to high frequency coupling or noise spikes. PSRR (Power Supply Rejection Ratio) is the ratio of the change in power supply to the change in output voltage. It is specified in dB.

Output impedance is important because of the dynamic loads generated by the CS501X successive-approximation A/D converters. When the reference is sourcing or sinking current, its output voltage will change due to non-zero output impedance. This impedance must be low enough at all frequencies of interest so the deviation in reference voltage when sourcing current is negligible. Output impedance is specified in ohms.

Output noise can lead to comparison errors in the A/D converter, and subsequently conversion errors. For the CS501X converters, reference noise is more evident with full scale inputs. It is specified in μV peak-to-peak.

Design Considerations

When interfacing voltage references to the CS501X series of A/D converters, their specifications should be robust enough so that the reference does not become a source of conversion error. During conversion, each capacitor of the calibrated capacitor array in the CS501X is switched between VREF and AGND in a manner determined by the successive-approximation algorithm. The charging and

discharging of the array results in a current load at the reference. The CS501X A/D converters include an internal buffer amplifier to minimize the external reference circuit's drive requirement and preserve the reference's integrity. Whenever the array is switched during conversion, the buffer is used to pre-charge the array thereby providing the bulk of the necessary charge. This buffer enlists the aid of an external 0.1µF ceramic capacitor which must be tied between its output, REFBUF, and the negative analog supply, VA-. The appropriate array capacitors are then switched to the unbuffered VREF pin to avoid any errors due to offsets and/or noise in the buffer. The external reference circuitry need only provide the residual charge required to fully charge the array after pre-charging from the internal buffer. This creates an ac current load as the CS501X sequences through conversions.

The reference circuitry must have a low enough output impedance to provide the requisite current without changing its output voltage significantly. As the analog input signal varies, the switching sequence of the internal capacitor array changes. The current load on the external reference circuitry thus varies in response with the analog input. Also with CS501X converters, bits are converted at a 1MHz rate with a full speed (4MHz) clock. The reference must settle within one microsecond so that it will be accurate before the next bit is converted. Signal amplitude dependent loading and conversion settling time require the output impedance of the reference to remain low from dc to at least 1MHz in order to ensure good converter performance.

The CS501X series of converters can operate with a wide range of reference voltages, but signal-to-noise performance is maximized by using as wide a signal range as possible. All CS501X converters can actually accept reference voltages up to the positive analog supply. However, the internal buffer's offset may increase as the reference voltage approaches VA+. This increases external drive requirements at VREF. Allowing 250mV headroom for the internal reference buffer is recommended. If the supplies are regulated specifically for the converter, 5.0 volt references may be used if the supply voltages for the CS501X are kept between ± 5.25 and ± 5.5 volts.

The magnitude of the current load presented to the external reference circuitry by the CS501X converters will vary with the master clock frequency. At full speed (4MHz clock), the CS501X A/D converters require maximum load currents of 10µA peak-to-peak (1µA peak-to-peak typical). The voltage reference must supply this current and maintain adequate voltage regulation. The load currents scale proportionately with the master clock frequency. Slower clocks can be used to relax maximum output impedance specification of the reference.

When driving multiple A/D converters from the same reference circuit, load currents will scale proportionally to the number of converters. Distribute the required decoupling components such that each ADC is locally decoupled.

Part # / f_{clk}	4MHz	2MHz	1MHz	500kHz
CS5012/CSZ5112 (Vref=4.5V)	27	54	108	216
CS5012/CSZ5112 (Vref=2.5V)	15	30	60	120
CS5014/CSZ5114 (Vref=4.5V)	7	14	28	56
CS5016/CSZ5116 (Vref=4.5V)	2	4	8	16

All units in ohms

Table 1. - Maximum Output Impedance for ≈ 1/4 LSB Reference Deviation

A reference with a maximum output impedance of 2 Ω will yield a maximum error of 20μV. This reference could drive a CS5016 (LSB=69μV with a 4.5V reference) and maintain approximately 1/4 LSB deviation during conversion. Similarly for the CS5014 (LSB=276μV with a 4.5V reference), and CS5012 (LSB=613μV with a 2.5V reference), maximum impedances of 7 and 15 Ω respectively will maintain adequate regulation. Table 1 defines maximum reference impedances allowed for each of the Crystal A/D's operating at different master clock frequencies in order to keep reference deviation approximately equal to 1/4 LSB.

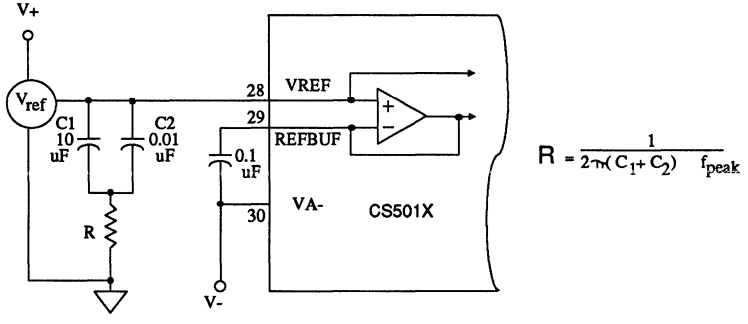
All precision references exhibit extremely low output impedance at dc. However, as frequency increases the impedance also increases. A large capacitor connected between VREF and AGND can provide sufficiently low output impedance at the high end of the frequency spectrum where the reference impedance is too high.

For example, the impedance of an ideal 10μF capacitor drops below 1 Ω at frequencies greater than 16kHz. However, actual capacitors behave differently due to their physical structure. Tantalum-foil electrolytic capacitors begin to appear inductive at frequencies around 100kHz and as a result their impedance begins to rise at frequencies above this. Aluminum electrolytic capacitors appear inductive at frequencies around 10kHz. Ceramic-disk capacitors behave much closer to ideal and begin to appear inductive at frequencies around 5MHz, but 10μF ceramic-disk capacitors are quite rare. Therefore, a high-quality tantalum capacitor (10μF) in parallel with a smaller (0.1μF) ceramic capacitor is recommended. This combination yields low impedance up to frequencies around 50MHz.

Peaking

The presence of large capacitors on the output of some voltage references may cause peaking in the output impedance at intermediate frequencies. Care should be exercised to ensure that significant peaking does not exist or that some form of compensation is provided to reduce it.

Most commercially available references use an integrated op-amp to buffer the actual reference generator. External capacitive loading will degrade performance of this op-amp. This degradation can be analyzed using classical analysis techniques. The open loop gain of an ideal op-amp is primarily determined by the internal compensation capacitor which generates a left-half-plane-pole (LHPP) at a very low frequency. The effect of this pole is to reduce the open loop gain by 20dB per decade and to add a -90 degree phase shift to the open loop transfer characteristic. Adding a capacitive load to the output of the op-amp generates another LHPP at a frequency inversely proportional to the



$$R = \frac{1}{2\pi(C_1+C_2)\ f_{peak}}$$

Figure 2. - Reference Connections

capacitor's value. An additional 20dB per decade reduction in gain and -90 degree phase shift result from the second LHPP.

The unity gain bandwidth of an op-amp (f_0), is the frequency at which the open loop gain goes to unity. If the total phase shift reaches -180 degrees before f_0 is reached the op-amp will become unstable. The closed loop frequency response peaks at f_0. As the total open loop phase shift at f_0 approaches -180 degrees, the closed loop peak at f_0 approaches infinity. The point of critical damping is the point where the peaking is precisely zero. Any phase shift less than this results in no peaking, and phase shift greater than this results in increased peaking.

Any peaking that might occur can be reduced by placing a small resistor in series with the capacitors (Figure 2). This resistor adds a left-half-plane-zero (LHPZ) to the open loop characteristic of the op-amp. This zero increases the gain by 20dB per decade, and adds a +90 degree phase shift. The resulting reduction in total phase shift at f_0 reduces peaking in the closed loop characteristic. The equation in Figure 2 can be used to help calculate the optimum value of R for a particular reference.

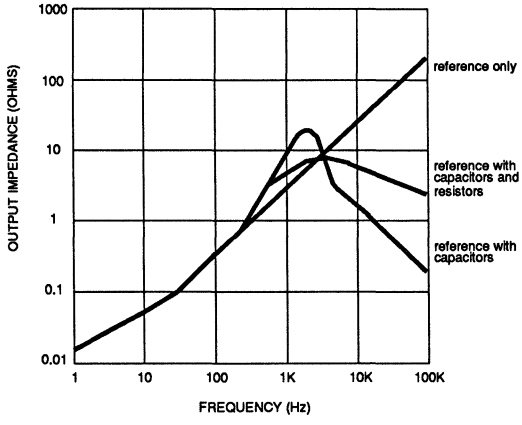


Figure 3. - Output Impedance Curves for LT1019-5

The term "f_{peak}" is the frequency of the peak in the output impedance of the reference before the resistor is added.

Design Example

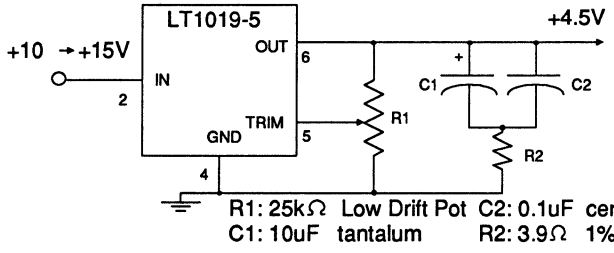
Figure 3 shows the output impedance characteristic of an LT1019-5 reference trimmed to 4.5V. The three curves represent impedances of the stand-alone reference, the reference with a 10µF tantalum and a 0.1µF ceramic capacitor added in parallel to the output, and the reference with the capacitors and a 2.2 Ω resistor in series with them (See Figure 2). Without loading, the reference impedance rises above 100 Ω at 50kHz. Adding the capacitors, peaking can be seen, but the maximum impedance is about 13 Ω at 4kHz. As shown in Table 1, 13 Ω is sufficient for use with the 12-bit converters and for the 14 and 16-bit converters with slow master clocks. With the addition of the 2.2 Ω resistor, the peak is reduced to 6 Ω and the impedance approaches 2.2 Ω at high frequencies.

Suggested Voltage Reference Circuits

Seven references were characterized for use with the CS501X family of successive-approximation A/D converters and the CSZ511X family of S-to-Z converters™. Important reference specifications such as output impedance and drift were measured for all references using standard test techniques. In addition, a Fast-Fourier Transform (FFT) test was performed to characterize the total dynamic performance of each reference circuit while driving a CSZ5116 converter. The same CSZ5116 was used for all tests yielding results which allow the comparison between different references. A summary of performance can be seen in the table on page 13. During the FFT test, a pure sine wave is applied to the CSZ5116 and a "time record" of 1024 samples is captured and processed. The FFT algorithm analyzes the spectral content of the waveform and distributes its energy among 512 "frequency bins". Distribution of energy in bins

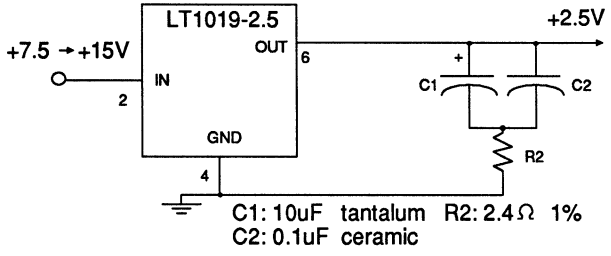
outside of the fundamental and dc can be attributed to errors in the A/D converter's performance, the reference, or the input sine wave.

The result of the FFT test is the ratio of input signal amplitude to the combination of harmonic distortion and total integrated noise. It is referred to as S/(N+D) in all of the performance charts in Figures 4 to 10. This ratio is expressed in dB. If input sine wave distortion and the actual A/D converter's distortion and noise are assumed to be negligible, the S/(N+D) is due to the reference only. In reality, this assumption can not be made. In the case of the Great Reference (See Figure 10), performance matches or exceeds the capability of the test setup. S/(N+D) ratios of 72 and 82 dB are sufficient for the 12-bit and 14-bit converters. For the 16-bit converters, 88 to 94 dB is necessary.



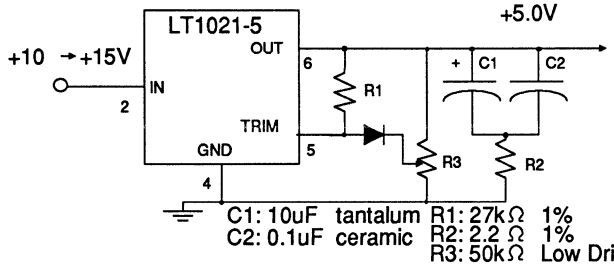
Reference Type	Bandgap
Untrimmed Accuracy	2.5mV
Max Impedance	6.5Ω @3.2kHz
Total Output Drift	5ppm/ °C
PSRR (50Hz to 500Hz)	90dB
Long Term Stability	-
Output Noise (dc to 1MHz)	250uV p-p
S / (N + D) (100Hz)	89dB
S / (N + D) (1kHz)	89dB

Figure 4. - LT1019-5 Reference Trimmable to 4.5V



Reference Type	Bandgap
Untrimmed Accuracy	1.25mV
Max Impedance	4.0Ω @5.8kHz
Total Output Drift	5ppm/ °C
PSRR (50Hz to 500Hz)	90dB
Long Term Stability	-
Output Noise (dc to 1MHz)	100uV p-p
S / (N + D) (100Hz)	87dB
S / (N + D) (1kHz)	86dB

Figure 5. - LT1019-2.5 Reference



Reference Type	Zener
Untrimmed Accuracy	2.5mV
Max Impedance	3.8Ω @5.0kHz
Total Output Drift	3ppm/ °C
PSRR (50Hz to 500Hz)	86dB
Long Term Stability	15ppm/1000hr
Output Noise	60uV p-p
S / (N + D) (100Hz)	90dB
S / (N + D) (1kHz)	90dB

Figure 6. - LT1021 Reference

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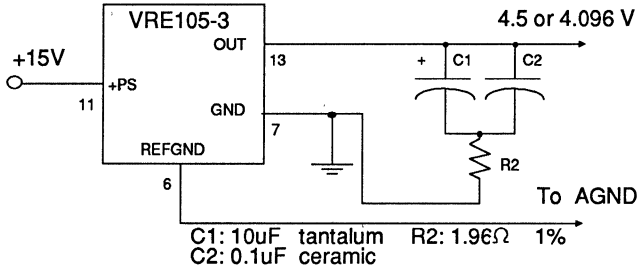


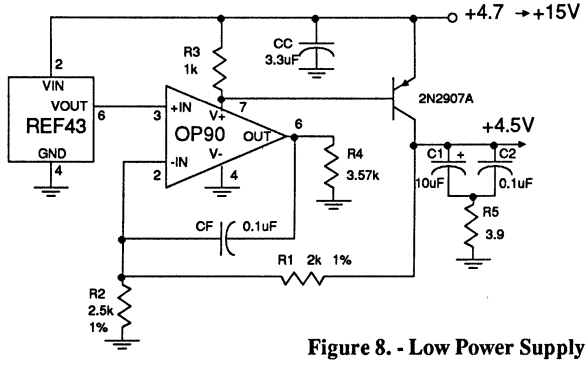
Reference Type	Zener
Untrimmed Accuracy	500uV
Max Impedance	2.5Ω@20kHz
Total Output Drift	0.5ppm/°C
PSRR (50Hz to 500Hz)	100dB
Long Term Stability	6ppm/1000hr
Total Output Noise	80uV p-p
S/(N+D) (100Hz)	90dB
S/(N+D) (1kHz)	90dB

Figure 7. - VRE105-3 Reference

FFT tests were performed at 100Hz and 1kHz. The 100Hz test checks the output impedance of the reference chip itself which dominates at low frequencies. At intermediate frequencies in the kHz range, highest output impedance was seen in all references. This was tested using the 1kHz FFT test. Since the reference capacitors dominate the impedance at high frequencies, high frequency FFT tests were not necessary. Although not tested, the best reference is likely to yield the best DNL performance when using a CS501X part. The least complicated reference circuit is the stand-alone reference chip with a passive compensation network. Its temperature drift and noise performance is equal to the reference chip itself since the compensation network does not change the dc output voltage. Keeping the output impedance low from dc to 1MHz is not trivial however, since there is no additional active circuitry added to perform this task. Four references were tested in the stand-alone configuration. Figures 4, 5, 6, and 7 illustrate schematics and measured specifications for these references. All references are monolithic with the exception of the VRE105-3 reference which is a hybrid. The calculated value of R2 in each of the references above will change slightly between units. Since the actual variation is small, picking the closest 1% tolerance resistor to the calculated value should give similar performance for all references of a particular manufacturer's model.

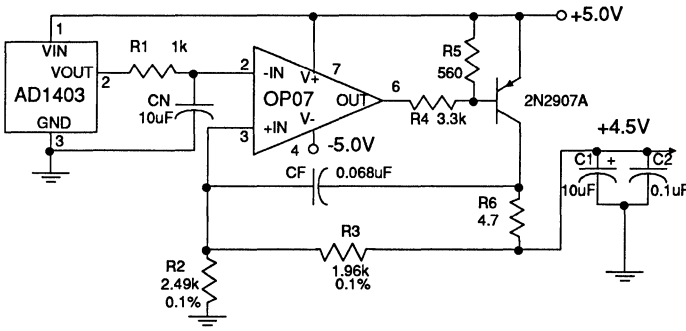
Other stand-alone voltage references with similar specifications include the AD584, REF02, REF03, REF10, and REF43. When designing with these references, the equation shown in Figure 2 should be used to calculate the appropriate value of R2 for each type of reference.

For applications which use ± 5.0 volt supplies, the reference in Figure 8 can be used. This reference circuit, designed by PMI, takes advantage of their new low power op-amp in a novel feedback configuration to achieve a 4.5



Reference Type	Zener
Untrimmed Accuracy	1.5mV
Max Impedance	4.4Ω @ 1kHz
Total Output Drift	8.0ppm/°C
PSRR (50Hz to 100Hz)	60dB
Long Term Stability	-
Output Noise (dc to 1MHz)	400uV p-p
S/(N+D) (100Hz)	88dB
S/(N+D) (1kHz)	88dB

Figure 8. - Low Power Supply Reference



Reference Type	Zener
Untrimmed Accuracy	50mV
Max Impedance	6.9Ω @ 2kHz
Total Output Drift	25ppm/°C
PSRR (50Hz to 100Hz)	80dB
Long Term Stability	-
Output Noise (dc to 1MHz)	30uV p-p
S / (N + D) (100Hz)	90dB
S / (N + D) (1kHz)	90dB

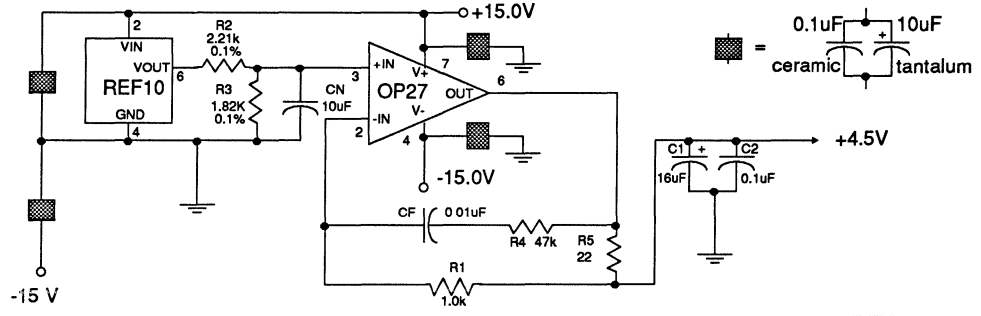
Figure 9. - Low Headroom Reference

volt reference which operates from 4.7 to 15 volt supplies.

Since only a few microamps of quiescent current flows in the op-amp, it can be assumed that the only current flowing in R3 is the same as that flowing in R4. It can be shown that V6 = 3.57(Vin-V7). For an output of 4.5 volts, and a supply of 4.7 volts, the op-amp has a supply of approximately 4.0 volts and an output voltage of 2.14 volts. This output voltage is well within the maximum specification of the OP-90 op-amp. Other references can be substituted for the REF43 if different drift or noise specifications are required.

The reference shown in Figure 9 is a low noise reference with less than 30μV peak-to-peak of noise from dc to 1MHz. It uses a discrete output stage allowing Vref to come within 300mV of the positive supply. The filtering network R1,CN reduces the bandwidth of the reference and therefore reduces the total output noise. The OP-07 is a low noise op-amp which buffers the filtered reference. This op-amp contributes very little noise to the entire reference circuitry.

The temperature coefficient of this reference is primarily due to to the matching of the gain resistors R2 and R3, so low temperature drift resistors should be used. Long term drift is dominated by the AD1403's drift. Other 2.5 volt



Reference Type	Zener
Untrimmed Accuracy	25mV
Max Impedance	0.5Ω @ 3kHz
Total Output Drift	9ppm/°C

PSRR (50Hz to 100Hz)	95dB
Long Term Stability	50ppm/1000hr
Output Noise (dc to 1MHz)	5uV p-p
S / (N + D) (100Hz)	92dB
S / (N + D) (1kHz)	92dB

Figure 10. - Great Reference

references can be used to improve this specification. The output voltage can be changed by adjusting R2 and R3 according to the following equation: Vref = Vout*((R2+R3)/R2). Resistors with 0.1% tolerance for R2 and R3 limit the reference's untrimmed accuracy only. Resistors with 1% or 5% tolerance can be used if untrimmed accuracy less than 50mV is not necessary. The supplies of the OP-07 should be bypassed with 0.1µF capacitors to ground.

The reference in Figure 10 exhibits very good noise, output impedance, and long term drift performance. It can be used in appications which have ± 15 volt supplies available. The reference has noise less than 10µV peak-to-peak from dc to 1MHz. The filtering network R2, R3, and CN filters noise components greater than 10Hz from the output of the REF10 reference. The OP-27 is a very low noise op-amp with excellent input offset drift over time and temperature.

The temperature coefficient of this reference is primarily due to to the matching of the voltage divider R2 and R3. Matched, low temperature drift resistors should be used when absolute accuracy is required. Temperature drift of the reference chip plus input offset drift of the op-amp is about 9ppm/°C. Other 10 volt references can be used in place of the REF10.

The reference voltage can be changed by adjusting R2 and R3 according to the following equation. Vref = Vout*(R3/(R2+R3)).

This circuit has no protection against accidentally applying ± 15V to the VREF pin. This could occur if the OP27 fails.

Miscellaneous Applications Information

Thermal temperature gradients due to power dissipation on the voltage reference die can create output voltage shifts. Keeping the entire chip on an isothermal plane is helpful. Reference load conditions should be kept very close to those specified, or degraded temperature performance will result. Some references specify a thermal regulation in ppm/mW. This can be used to calculate voltage drift for a specific power dissipation due to loading.

Overall die temperature change can cause thermally induced output voltage variations which can exceed electrical effects. Shifts in power dissipation on the board level are the major contributor to this error. In critical applications, using a heat-sink is recommended to keep the reference temperature deviations small.

Thermocouple effects between package leads can also cause excessive output voltage drift and noise. Differences between materials in IC leads and PC-board traces can cause thermoelectric currents to flow. Ambient air turbulence around the leads causes mismatches in the temperature between the package leads. The resulting thermoelectric voltage contributes to noise. Using dual in-line packages (DIPs) is recommended over using TO-5 type packages. The copper or Alloy 42 lead frames on DIPs are much less sensitive to thermocouple effects than the Kovar leads of the TO-5 packages. Using an enclosure such as a polysulfone shield which blocks the air flow over the reference package will also reduce the problem by reducing air movement around the package leads.

In reference circuits which have external gain setting resistors, tracking of the temperature coefficients of these resistors is vital. Wirewound resistors made of Evenohm or Mangamin have the lowest temperature coefficients. Ceramic film resistors such as Vishay are also good. Matching in resistor temperature coefficients as good as 0.4 ppm/°C can be achieved. Arranging these resistors in close proximity to one another also helps matching. SIP or DIP resistors by Beckman exhibit the best matching since all resistors are processed on the same substrate.

Part #	Manufacturer	Telephone Number
VRE105-3	Thaler Corporation	(602) 742-5572
LT1019-5 LT1019-2.5 LT1021-5	Linear Technology	(408) 942-0810
OP07 OP90 REF02 REF03 REF43	Precision Monolithics Inc.	(408) 727-9222
OP27 REF10	Burr-Brown	(602) 746-1111
AD584 AD1403	Analog Devices	(617) 329-4700

List of Manufacturers

Reference	Type	Untrimmed Accuracy	Maximum Impedance	Output Drift	PSRR (50Hz to 100Hz)
LT1019-5	Bandgap	2.5mV	6.5Ω @ 3.2kHz	5ppm/°C	90dB
LT1019-2.5	Bandgap	1.25mV	4.0Ω @ 5.8kHz	5ppm/°C	90dB
LT1021-5	Zener	2.5mV	3.8Ω @ 5.0kHz	3ppm/°C	86dB
VRE105-3	Zener	500uV	2.5Ω @ 20kHz	0.5ppm/°C	100dB
Low Supply	Zener	1.5mV	4.4Ω @ 1kHz	8ppm/°C	60dB
Low Headroom	Zener	50mV	6.9Ω @ 2kHz	25ppm/°C	80dB
Great	Zener	25mV	0.5Ω @ 3kHz	9ppm/°C	95dB

Reference	Long Term Stability *	Output Noise (dc to 1MHz)	S/(N+D) (100Hz)	S/(N+D) (1kHz)
LT1019-5	-	250uV p-p	89dB	89dB
LT1019-2.5	-	100uV p-p	87dB	86dB
LT1021-5	15ppm/1000hr	60uV p-p	90dB	90dB
VRE105-3	6ppm/1000hr	80uV p-p	90dB	90dB
Low Supply	-	400uV p-p	88dB	88dB
Low Headroom	-	30uV p-p	90dB	90dB
Great	50ppm/1000hr	10uV p-p	92dB	92dB

Performance Comparison Table

* Taken from reference data sheets. All other parameters were measured.

• Notes •

Semiconductor Corporation

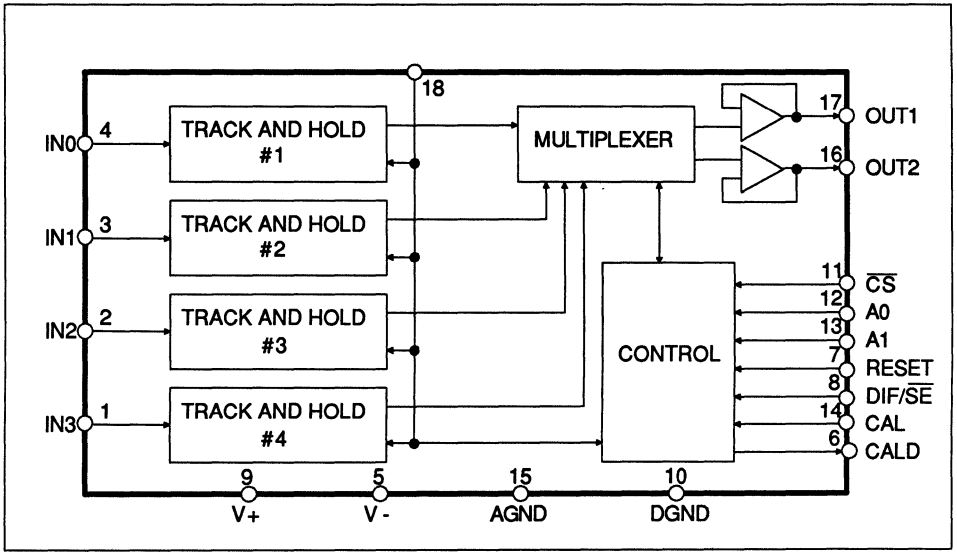
CS31412

Application Note

Suggested Grounding and Supply Arrangements for the CS31412

by

Steven Harris



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APPLICATION NOTE

CS31412 Quad Track and Hold Amplifier Recommended Grounding and Supply Arrangements

The CS31412 connections fall into 6 classes: analog inputs, analog outputs, non time-critical digital inputs, digital outputs, power supplies, and the hold signal. The fundamental guideline to follow is to think carefully about the currents flowing due to the above 6 classes of signals, and keep them separate.

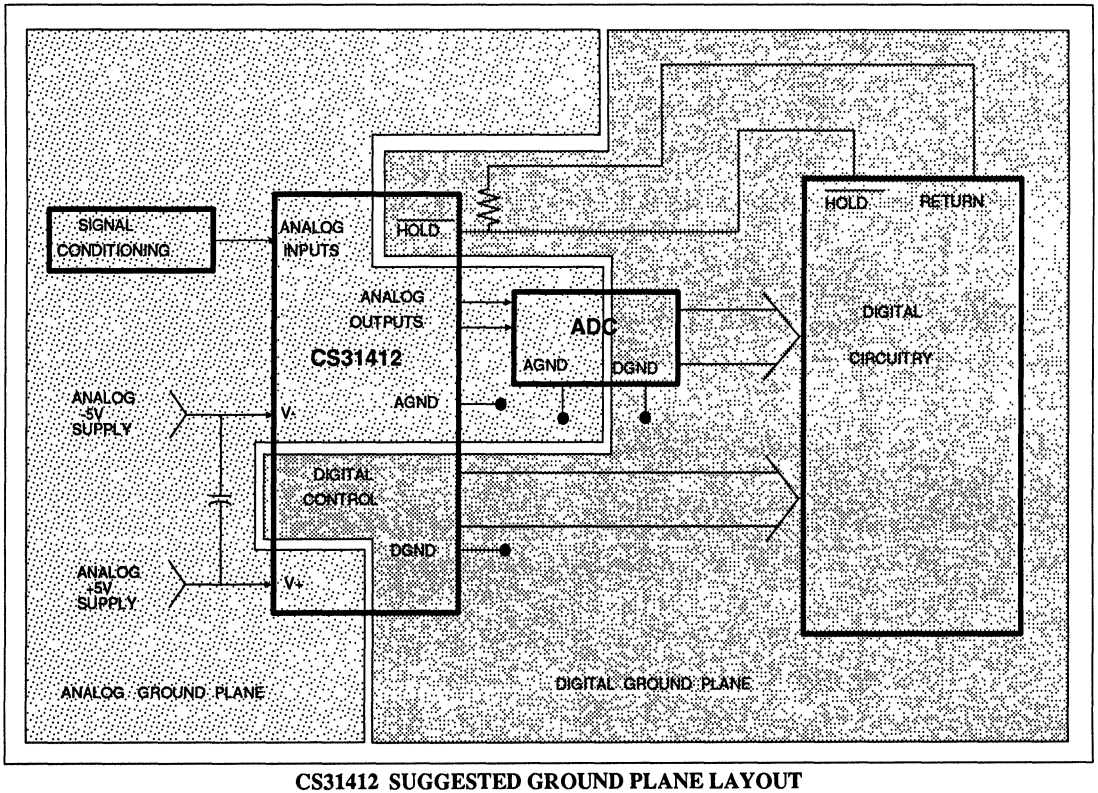
A good layout scheme will:

a) Keep digital signal noise from the analog output.

b) Obtain the best possible accuracy.
c) Minimize the aperture jitter.
d) Minimize power supply noise affecting the output.

The following guidelines will help to achieve these goals:

1) Have separate analog and digital grounds. Only join these grounds together at one place, typically either at the power supply or at the ADC.
2) Decouple the part with a 10µF/0.1µF capacitor combination connected between V+ and V-, as near to the part pins as possible
3) Group all of the non time-critical digital signal traces together and keep them separated from the analog signals. Also use digital ground traces to



CS31412 SUGGESTED GROUND PLANE LAYOUT

isolate this group of traces from the other signals.
4) The high input impedance of the part on the analog input pins results in a very small input current. Nevertheless, if termination resistors are used, the return currents for each resistor should be kept separate to avoid introducing crosstalk
5) Connect the loads to the analog outputs such that the return currents do not flow in any input related ground leads.
6) Typically the hold signal will be terminated to ground near to the CS31412. This gives a clean edge and also minimizes the absolute amplitude of the hold signal. Both the hold signal and its return current trace should be brought back to the pins of the part generating the signal.

The figure shows a possible ground plane layout, concentrating on the area around the CS31412.

Notes:

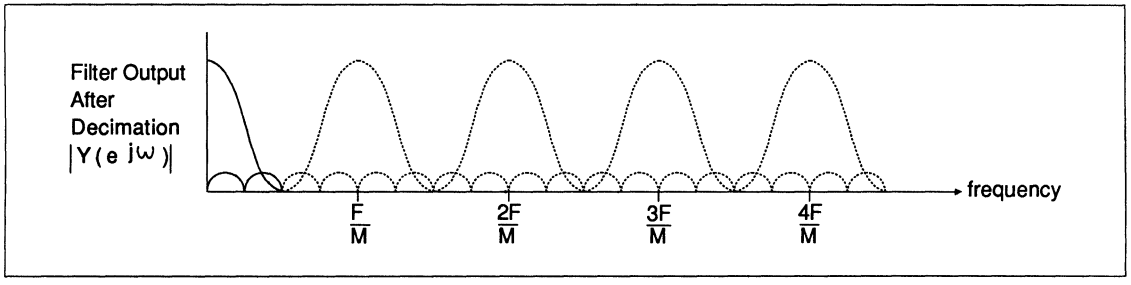
1) The CS31412 is grossly out of scale. It is enlarged to highlight the grounding around the sample hold.

2) The Analog and Digital ground planes should be joined together at the ADC or at the power supplies.

• Notes •

Antialiasing Considerations for the CSZ5316

by
Nav Sooch



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APPLICATION NOTE

ANTIALIASING CONSIDERATIONS FOR THE CSZ5316

Introduction:

Delta-Sigma A/D converters perform a rough A/D conversion at a high rate and digitally filter the output to obtain an accurate low frequency conversion. Since the input is initially sampled at a high rate and followed by a digital filter, the majority of antialias filtering is performed by the digital filter. However, aliasing problems due to decimation still remain. These aliasing issues can be addressed by analog and/or digital filters. In general, the antialias filtering requirements of the CSZ5316 are simpler than those of conventional A/D converters. This application note describes the aliasing properties of the CSZ5316 and provides examples of filtering options.

Note: Antialiasing requirements are a function of the desired signal bandwidth and out-of-band energy. For simplicity, a clock rate of 4.096 MHz has been chosen for this note. If the actual clock rate is different, all the frequency values in this

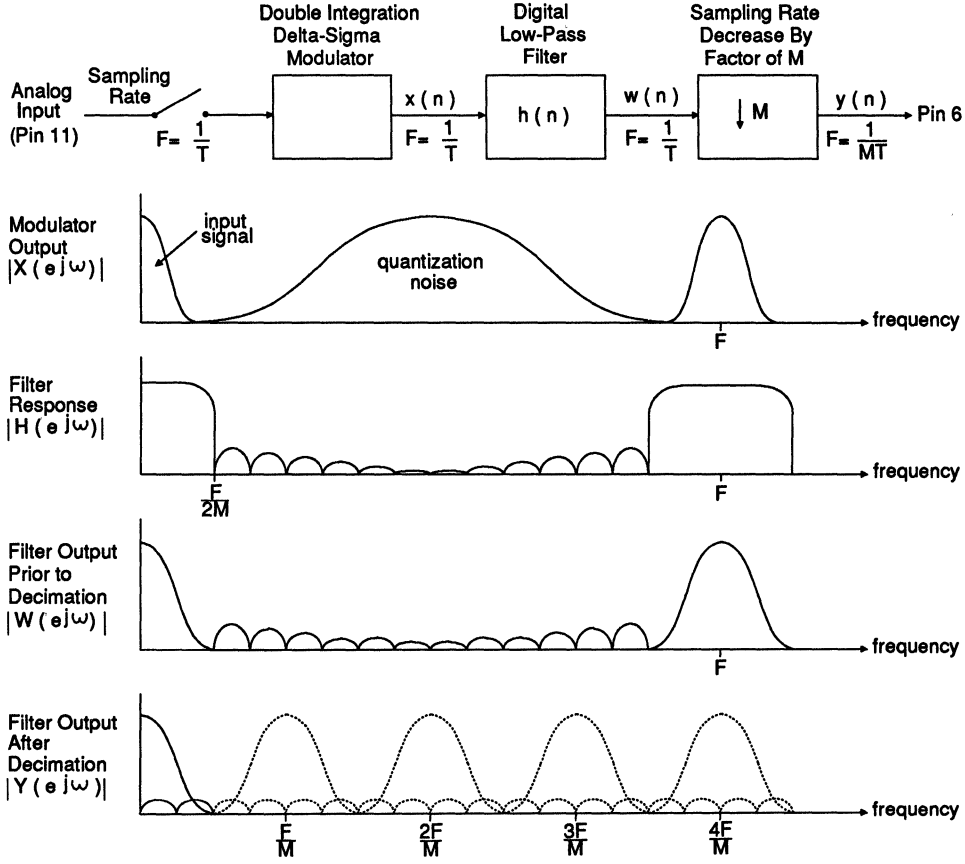


Figure 1. - Block Diagram and Typical Spectra for Sampling Rate Reduction by a Factor of M

note should be scaled by (actual clock rate)/(4.096 MHz).

Initial Sampling:

The initial sampling of the analog input is done at 2.048 MHz. There is no internal filtering of frequencies at (2.048)n MHz + 8 kHz (where n = 1,2,3...). If signals in this band exist, an analog filter must attenuate them. Typically, a single-pole RC filter will suffice (see CSZ5316 data sheet).

Decimation:

The process of digitally converting the sampling rate of a signal from a given rate F to a lower rate F' is called decimation. The decimation process is shown graphically in the frequency domain in Figure 1. The delta-sigma modulator output, x(n), sampled at frequency F is fed into a low-pass filter with response h(n). The output of this filter is decimated by a factor M to a new sampling rate of F' = F/M.

The analog modulator on the CSZ5316 is followed by a digital filter that has the following frequency response:

$$\text{Mag}\,|H(e^{j\omega})| = \left|\frac{\sin(N\pi f/fs)}{N\sin(\pi f/fs)}\right|^3 \quad (1)$$

$$\text{where } N = 128 \text{ and } fs = \frac{CLKIN}{2}$$

The digital filter's frequency response is plotted in Figure 2. The output rate of this digital filter is internally decimated to 16 kHz. Decimating to 16 kHz implies that he output of the filter is effectively resampled at 16 kHz. Therefore, signals at multiples of 16 kHz will alias into the baseband after being attenuated according to the filter response defined in Equation 1. For example, an input tone at 28 kHz will be attenuated by 53.4 dB and will appear at 4 kHz in the output spectrum (2 (16 kHz) - 28 KHz = 4 kHz).

Table 1 shows the antialiasing rejection at a few key frequencies.

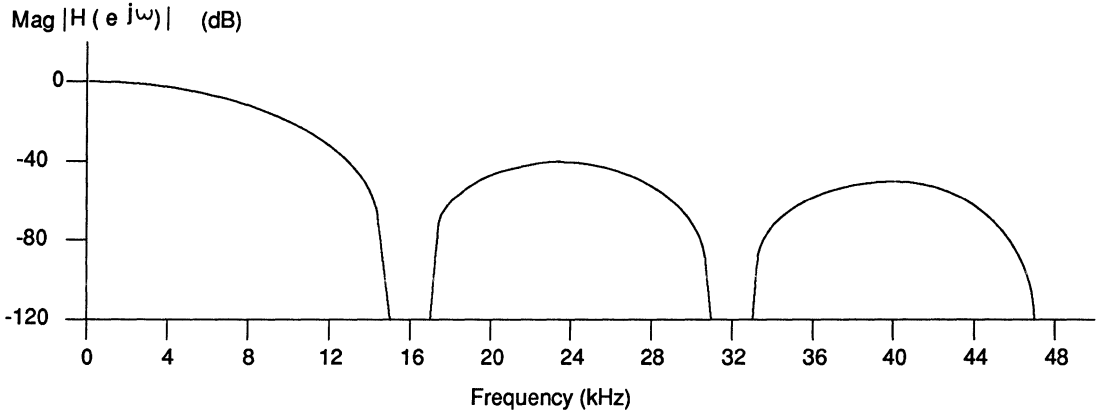


Figure 2. - Low-Pass Filter Response

Input Frequency (kHz)	Output Frequency (kHz)	Attenuation (dB)
10	6	19.6
12	4	31.4
14	2	51.4
18	2	57.9
20	4	44.7
24	8	40.4
28	4	53.4
34	2	74.5

Table 1. - Antialiasing Rejection at Key Frequencies

Note that the worst case rejection into the 0-4 kHz band is 31.4 dB for input signals at 12 kHz. Also note that very little rejection is provided for signals that alias into the 4-8 kHz band.

ANTIALIASING STRATEGIES

One of the following three cases and associated antialiasing strategies should apply to any CSZ5316 application:

Case 1 -No Out of Band Energy

4 kHz Bandwidth:

If there is no incoming energy past 4 kHz, the digital output can be decimated to 8 kHz by simply dropping every other output sample. Incoming signals past 4 kHz can always be filtered by an analog filter prior to A/D conversion. Since the digital output is not filtered prior ro decimation, the dynamic range will be 84 dB (see Data Sheet).

8 kHz Bandwidth:

When signals from 0 to 8 kHz are of interest, the incoming signals must be band-limited to 8 kHz. Since the CSZ5316 output rate is already at the Nyquist rate of 16 kHz, no further decimation is necessary. The dynamic range will be 84 dB.

Case 2 -Limited Out of Band Energy

Assume that the input signal has the following spectrum:

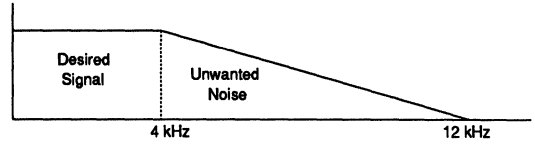


Figure 3. - Limited Out of Band Energy

Two filtering methods are possible to prevent aliasing:

Analog Filter on Input

An analog filter can be used to remove the energy in the 4-12 kHz band prior to A/D conversion. The digital output of the CSZ5316 can be decimated to 8 kHz. If decimation is done without digital filtering, the dynamic range will be 84 dB (see Data Sheet).

Digital Filter on Output

Unwanted noise from 8 to 12 kHz will alias into the 4-8 kHz band after internal decimation in the CSZ5316. A digital filter can be used at the output of the CSZ5316 to remove energy in the 4-8 kHz band. The output of this external digital filter can be decimated to 8 kHz. In this case, the dynamic range will be 90 dB (see Data Sheet).

Case 3 -Lots of Out of Band Energy

Assume that the input signal has the following spectrum:

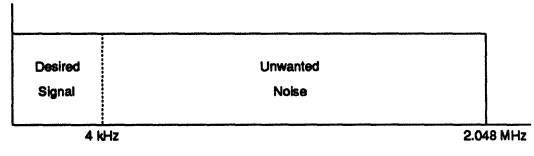


Figure 4. - Lots of Out of Band Energy

The following filtering possibilities exist:

Analog Filter

An analog filter can be used to remove energy past 4 kHz. The digital output of the CSZ5316 can be decimated (drop every other sample) to 8 kHz. If decimation is done without a post digital filter, then the dynamic range will be 84 dB (see Data Sheet).

Analog and Digital filters

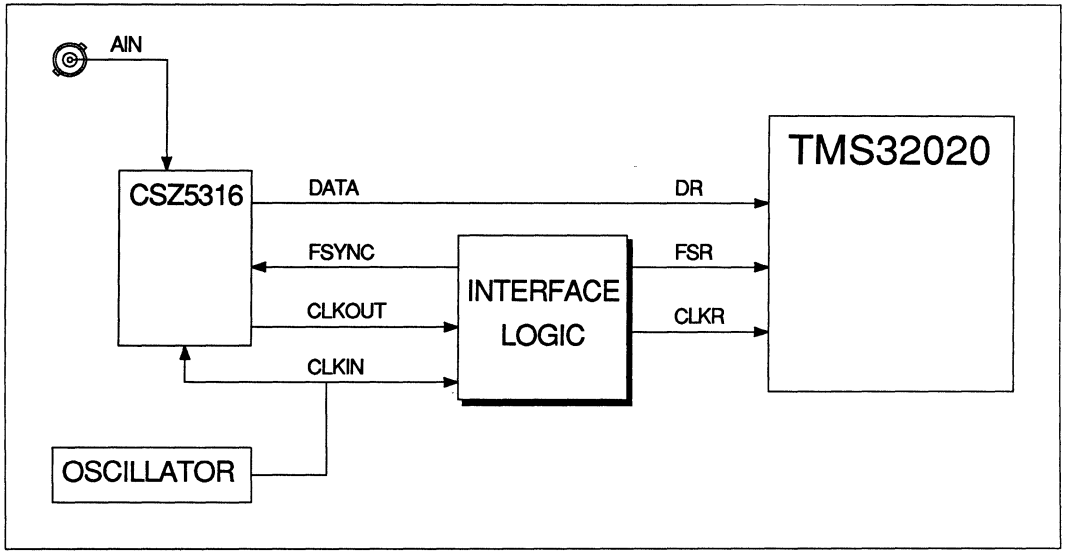
A combination of analog and digital filters can be used. The digital filter can remove signals that alias into the 4-8 kHz band. As seen from Table 1, the frequencies that alias into the 4-8 kHz band are 8-12 kHz, 20-28 kHz, 36-44 kHz, and so on. The internal decimation filter on the CSZ5316 provides a minimum rejection of 31.4 dB for components in the 12-20 kHz and 28-36 kHz bands. Note that the requirements on this analog filter are significantly relaxed compared to the filter in the analog alone option (i.e. the transition band for this analog filter is much wider). Since a digital filter is used to remove energy in the 4-8 kHz band, the dynamic range will be 90 dB (see Data Sheet).

• Notes •

Application Note

TMS32020-to-CSZ5316 Interface

by
Clif Sanchez



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INTRODUCTION

The CSZ5316 Delta-Sigma Analog to Digital converter is a high resolution A/D converter with excellent AC characteristics for voice-band signal processing applications. This application note describes one way to interface the CSZ5316 to the TMS32020 Digital Signal Processor.

Functional Description

The need for this interface logic is two-fold.

First, the TMS32020 samples FSR on the falling edge of CLKR and must sample FSR high at least once. Therefore, CLKOUT cannot be directly used for CLKR because CLKOUT only occurs when data is output, which is one cycle too late. Part of the interface logic creates a synchronous clock, CLKR, which is in phase with CLKOUT.

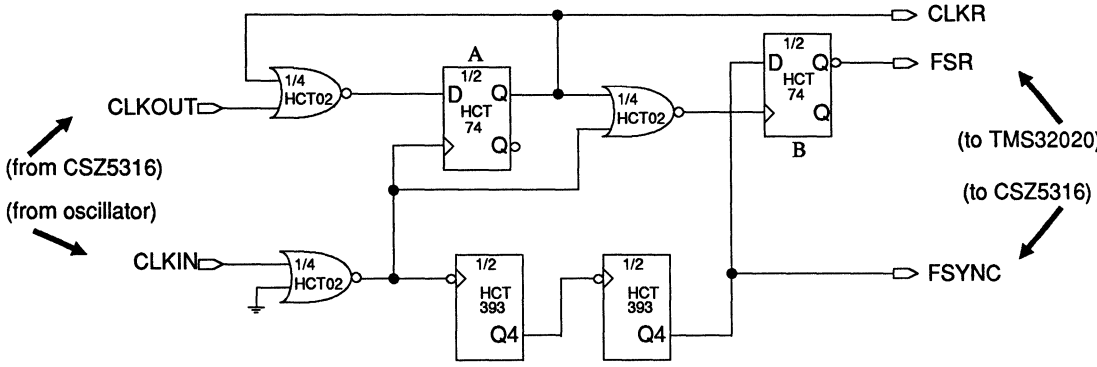
Second, the CSZ5316 uses a modulo-2 counter internally. This counter is half the frequency of CLKIN and generates DATA and CLKOUT. Since the phase of the internal clock is indeterminant, a random FSYNC could occur during either phase of the internal clock. The TMS32020 requires FSR ($\overline{\text{FSYNC}}$) to transition in the low half-cycle of CLKR (derived from CLKOUT). Therefore, part of the interface logic synchronizes FSYNC to CLKR low.

Circuit Description

The oscillator block shown on page 25 must output a clock in accordance with the specifications for CLKIN in the CSZ5316 Data Sheet.

The interface logic block consists of three IC's and generates the control signals needed by the CSZ5316 and the TMS32020 serial interface. The IC's depicted in the diagram are "74HCT" CMOS which are quieter than "74LS" logic and are TTL compatible, but the latter will also work.

The schematic diagram shown below is the entire interface for the CSZ5316-to-TMS32020 interface. The circuit takes the master clock, CLKIN, and inverts it using one of the NOR gates. This is fed into the binary counters (HCT393) to produce a clock frequency of CLKIN divided by 256.



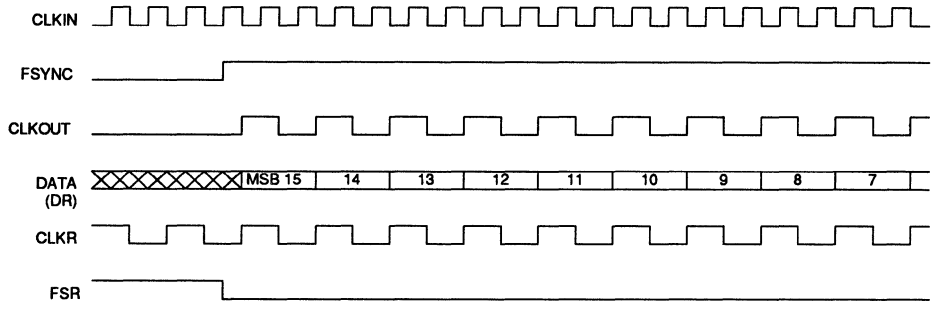
CSZ5316-to-TMS32020 Interface

The D flip-flop (HCT74) labeled "A" generates a continuous clock, and the NOR gate on the input forces the synchronous clock to the same phase as CLKOUT. Once the synchronous clock, CLKR, is in phase with CLKOUT it will stay that way.

The D flip-flop labeled "B" synchronizes the output of the binary counters to the rising edge of CLKIN (the falling edge of $\overline{\text{CLKIN}}$) but the NOR gate might delay that operation one CLKIN cycle if CLKR isn't low. This synchronizes FSYNC and FSR to CLKR low.

Timing

The diagram below illustrates the timing generated by the interface logic. On startup, two extra FSYNC cycles are needed to produce valid data.



Note: Circuit guarantees: 1. FSR falls in the center of CLKR low
2. Data starts on the next rising edge of CLKR

CSZ5316 to TMS32020 Interface Timing

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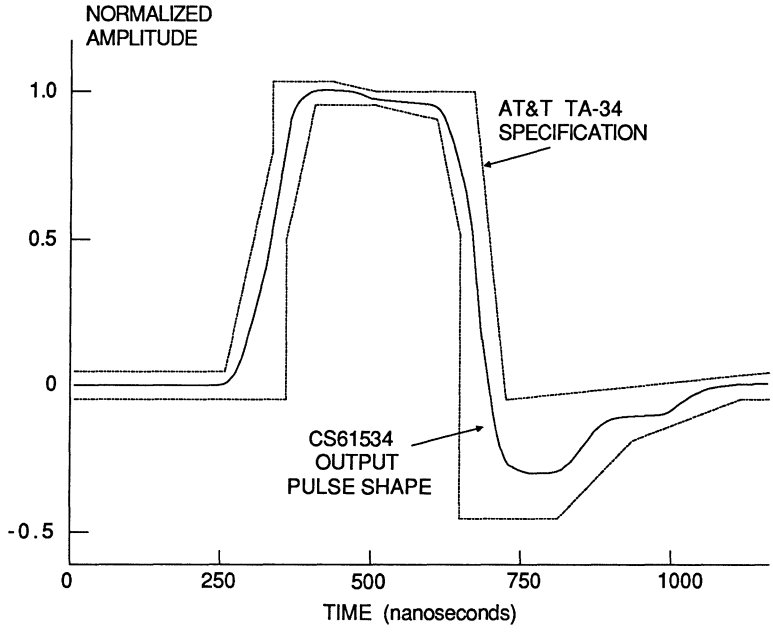
• Notes •

Application Note

CS61534 Design Guidelines to Insure Compatibility with the CS61574

by Bob Bridge and Roger Taylor



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CS61534 DESIGN GUIDELINES TO INSURE COMPATABILITY WITH CS61574

The following guidelines should be considered during board design for the CS61534 to facilitate changing to the 61574 when it becomes available.

1. LINE LENGTHS:

In the CS61574, line lengths, LEN2/1/0 = 001 and LEN2/1/0 = 010 will be changed to provide additional ABAM pulseshapes. The simplest migration path results when those settings are not used in the CS61534.

2. HOST MODE:

The CS61574 host mode has more functionality than the CS61534 host mode, but they are compatible, provided the codes 101, 110, and 111 for bits 5, 6, and 7 are not used. These codes will have specific functions in the CS61574.

In the CS61534, the $\overline{INT}$ pin stays low as long as a fault condition exists (e.g., LOS, DPM), and can not be cleared over the serial interface. In the CS61574, $\overline{INT}$ goes low whenever DPM or LOS changes state, and can be cleared using the serial interface.

To select RLOOP on the CS61534, it is recommended that code 100 be used, rather than 101 (which can be used since RLOOP overrides TAOS).

3. EXTERNAL CRYSTAL / ALTERNATE CLOCK:

To maintain board compatibility from the CS61534 to the CS61574, an external crystal should be used and the ACKLI input should either be tied to an external clock or tied to ground. Overdriving a crystal input of the CS61574 with a four-times clock is not supported.

4. LOSS OF SIGNAL TEST:

The CS61534 determines loss of signal as either 32 zeroes in a row, or decay of the peak signal (low amplitude signal for about 200 bit periods). The CS61574 uses just the "decay" test.

5. JITTER ATTENUATION:

Note that the jitter attenuator in the CS61534 is moved to the recieve path on the CS61574 and is a more powerful circuit.

6. RECOVERED CLOCK UPON LOSS OF SIGNAL:

Upon LOS, the CS61574 RCLK frequency will assume the center frequency of the external crystal (or ACKLI if present). This is in contrast to the CS61534 where RCLK could drift 6% upon LOS.

CONTENTS

RELIABILITY INFORMATION

Concept of Reliability

In general terms, the reliability of a semiconductor device is defined as the measure of the functional stability of the device with respect to time. Expressed in more quantitive sense, it is the probability that the device will operate with a specified performance over a specified period of time under a given set of conditions.

Reliability characteristics are usually stated in reverse terms as the loss of ability to function, or failure rate. The reliability performance of a device can be best summarized by the reliability life or "bathtub" curve (Fig. 1). The reliability performance is characterized by three phases: infant mortality, useful life or random failure period, and wearout. Infant mortality failures can be reduced by proper manufacturing controls and screening techniques. The useful life period is typically a long period of time where only occasional random failures occur. During this time the failure rate is usually very low. The final period, wearout, is that in which the device fails due to continuous phenomena that existed at the time of manufacture. Using proper design guidelines and device application, this period is shifted well beyond the lifetime required by the user.

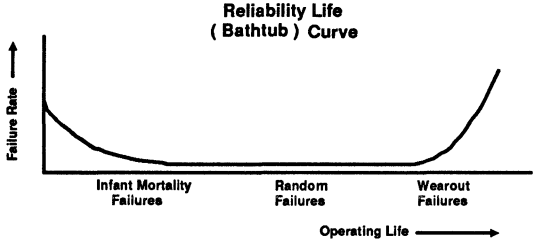

Figure 1

Failure Rate Calculations

Failures during typical reliability stressing generally are in the infant mortality and random failure sections of the "bathtub" curve. These failures can be stated in their accelerated stress condition term or they can be derated to actual operating conditions by commonly accepted mathematical models.

Environmental stresses, such as autoclave, temperature cycling, thermal shock, storage life and 85 °C/85% R.H., usually have their failure rate expressed in accelerated condition terms, due to the lack of widely recognized derating models. These are usually expressed as % failure/stress time. An example of this would be a temperature cycling failure rate expressed as % / 1000 cycles. These failure rates should have a confidence level associated with the data given. For environmental stresses, Crystal publishes data with a 90% confidence level. To calculate this failure rate with confidence levels, the following calculations are made:

$$f_c = f_a + Z \left\{ \sqrt{\frac{f_a (1 - f_a)}{n}} \right\} \qquad \text{EQ. \#1}$$

Where: f_c = failure rate with confidence level
f_a = actual observed failure rate
n = number of sample stressed
Z = value of the standard normal probability distribution associated with the desired confidence level

This calculation is based on binomial probability statistics. As can be seen in the equation, the sample size is a key contributor in determining the difference in the actual failure rate and that

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of the failure rate with the desired confidence level.

Operating life usually is reported in the derated form. Failure rates for other temperatures are calculated using a computed acceleration factor. The thermal acceleration factor (AF) is related to the thermal activation energy (EA) by the Arrhenius relationship:

$$AF\ (T1 \rightarrow T2) = e^{\frac{-EA\left(\frac{1}{T1} - \frac{1}{T2}\right)}{K}} \qquad \text{EQ.\#2}$$

Where:
- AF = acceleration factor
- EA = thermal activation energy (eV)
- k = Boltzman's constant (8.63 E -5 eV / K)
- T1 = test junction temperature (K)
- T2 = desired junction temperature (K)

It should be noted that junction temperature should be used in determining acceleration factors. This temperature can be obtained from Eq. #3.

$$TJ = TA + O_{JA} * PD \qquad \text{EQ. \#3}$$

Where:
- TJ = junction temperature (C)
- TA = ambient temperature (C)
- O_{JA} = package thermal dissipation (C / watt)
- PD = device power dissipation (watts)

Three items play an important part in determining the final acceleration factor and must be considered when comparing derated failure rates. They are : 1) activation energy used, 2) derated from actual junction temperature vs. ambient temperature and 3) derated operating temperature.

TABLE 2
ACCELERATED FACTORS FOR DIFFERENT ACTIVATION ENERGII
125 °C --> 70 °C

E. A.	ACCELERATION FACTOR
1.0	106.0
.9	66.7
.8	41.7
.7	26.3
.6	16.4
.5	10.3
.4	6.5
.3	4.1

Table 2 compares acceleration factors for different activation energies. As you can see using a 1.0 eV activation energy versus a .7 eV activation energy results in a factor of four increase in the acceleration factor. Crystal takes the conservative approach, using an activation energy of .7 eV. Table 3 compares acceleration factors for different operating temperatures. This shows how derating to a lower temperature or using ambient temperature can greatly affect the acceleration factor of Arrhenius equation. Using ambient temperatures instead of junction temperature can affect acceleration factors by a multiple of about three on a high power device.

TABLE 3
ACCELERATION FACTORS FOR DIFFERENT TEMPERATURES
E. A. = .7 eV

TEMPERATURE CHANGE	ACCELERATION FACTOR
125 --> 70°C	26.3
125 --> 55°C	77.5
125 --> 25°C	933.0
204 --> 149°C	9.2 (Note 1)

Note 1: This equivalent to an ambient temperature change from 125 -->70 °C on a 40 pin ceramic device with a power dissipation of 1 Watt

There are many probability models used in reliability analysis. The Weibull distribution is often used for product life prediction because it can describe increasing and decreasing failure rates. Also the Weibull distribution has both a shape parameter (B) and a scaling parameter (a). This is very useful in accurately describing the shape and scaling of the "bathtub" tub.

$$h(t) = \frac{B}{a} t^{(B-1)} \qquad \text{EQ. \#4}$$

The Weibull cumulative distribution function for population failing by time t is:

$$F(t) = 1 - e^{(\frac{t}{a})^B} = 1 - R(t) \qquad \text{EQ. \#5}$$

Where:
- t = time
- a = alpha - the Weibull scale parameter
- B = beta - the Weibull shape parameter
- F(t) = the failure distribution function
- R(t) = the reliability function
- h(t) = the instantaneous failure rate

The function F(t) and R(t) are shown in Fig. 2.

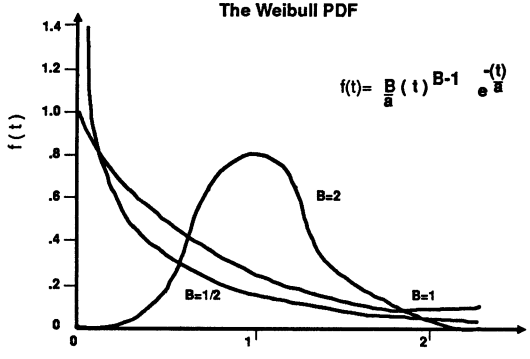

Figure 2

Mathematically these functions are described :

$$F(t) = \int_0^t f(t)\,dt \qquad \text{EQ. \#6}$$

$$R(t) = \int_t^{\infty} f(t)\,dt \qquad \text{EQ. \#7}$$

where f(t) = failure rate probability distribution function

Integration of the Weibull hazard function, factoring for conversion to failure rate in fits (failure per billion device hours) and factoring for Arrhenius acceleration factors will result in the following failure rate equation:

$$F.R. = \frac{10^9}{t2 - t1} \left\{ \frac{(\frac{t2}{AF})^B - (\frac{t1}{AF})^B}{a} \right\} \qquad \text{EQ.\#8}$$

t 2 = time 2
t 1 = time1
F.R. = Failure Rate in Fits

To correctly solve for the failure rate we must have a value for the shape parameter (B) and the scale parameter (a). To do this we twice take the natural logarithm of Eq. #5 above and obtain:

$$\frac{\ln \ln}{1 - F(t)} = B \ln(t) - \ln(a) \qquad \text{EQ. \#9}$$

This equation takes the slope intercept form

$y = Bx + I$

where $y = \ln \ln (1 / 1 - F(t))$

$x = \ln t$
B = slope of the line
$I = \ln a$ = y -intercept.

Using linear regression techniques or Weibull plotting paper, we can obtain the shape parameter (B) and the scale parameter (a) by:

B = Slope
$a = e^{-1}$

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For B = 1, the Weibull distribution is the exponential distribution. In practice very few products have B = 1. Most semiconductor devices have a beta of less than 1 indicating the steep slope of the "bathtub" slope. A beta of greater than 1 indicates that the failure rate increases with age. Fig. 2 gives shape of the Weibull distribution for different B values.

A confidence level must also be placed on this data. This is done by placing a confidence level on the scaling parameter(a) using chi-square statistics. The equation below gives the formula for obtaining this transformation:

$$a(\%C.L.) = a\{2r / x^2(C; 2r + 2)\}^{\frac{1}{B}}$$

EQ. # 10

r = number of rejects in sample

$x^2(C; 2r + 2)$ = the c percentile of the chi-square distribution with (2r + 2) degree of freedom.

These chi-squared percentile are tabulated in most statistics books. On operating life stresses, Crystal uses a 60% confidence level in reporting the failure rate. These failure rates are derated to 70 °C, 55 °C and 25 °C.

In summary, Crystal semiconductor uses conservative models that are accepted throughout the semiconductor industry to determine the reliability failure rates of their devices.

Accelerated Operating Life Stress

Accelerated operating life stressing is performed to accelerate failure mechanisms, which are thermally activated, through the application of extreme temperature and dynamic biasing conditions. The typical temperature and voltage conditions used in the stress are 125 °C with a bias level at the maximum data sheet specifications. Some devices may be stressed at an even higher voltage level, to further stress the oxides of the device. All devices used in life stressing are sampled directly from the production flow with no special processing or pre-screening. Stressing is performed per mil STD 883, method 1015 and condition D (dynamic signals) . These dynamic conditions simulate as much as possible actual operating conditions in an application.

Both infant mortality operating life stress (168 HRS) and long term operating life (typically 1000 HRS) are reported. Infant mortality life simulates approximately 6-8 months in the field at 70 °C and is reported as % / 168 HRS. Long term life simulates the total failure rate in the field and is expressed in FITs. (failures in time) 1 FIT = 1 failure per billion device hours. Derating of long term operating life is done using Arrhenius thermal equations along with Weibull statistics. A 60% upper confidence limit (UCL) and .7 electron Volts (eV) activation energy are used in this calculation.

85 °C/85% R.H.

85 °C/ 85% RH is an enviromental stress performed at a temperature of 85 °C and a relative humidity of 85%. The test is designed to measure the moisture resistance of plastic encapsulated devices. A nominal voltage static bias is applied, with minimum bias consumption, to the device, to create the electrolytic corrosion acceleration of the metallization. Failures are expressed in % / time with 168, 500 and 1000 hour results reported.

Autoclave

Autoclave is also an enviromental stress which measures the moisture resistance of plastic encapsulated devices. Conditions for this test are a temperature of 121 °C and 100% relative humidity and 2 atmosphere of pressure (15 PSIG), with no bias applied to the circuit. Corrosion of the die is the expected failure

mechanism. Stressing is usually performed for 144 hours. Failures are expressed in % / time with 48, 96 and 144 hour results reported.

Temperature Cycling

Temperature cycling typically accelerates the effects of thermal expansion mismatch among the different components within a specific package and circuit. The stress is performed per MIL STD 883, method 1010 and condition C. (-65 °C to +150 °C). Stressing is done in an air enviroment. A cycle consists of ten minutes at -65 °C, five minutes transfer time, and ten minutes at +150 °C. Stressing is typically performed for 1000 cycles. Failures are expressed in % / cycles, with 100, 500 and 1000 cycle results reported.

Thermal Shock

The objective of thermal shock is basically the same as that of temperature cycling to exercise the difference in thermal expansion coefficients in the integrated circuit system. Thermal Shock provides additional stress as the device is exposed to a rapid change in temperature, due to a maximum transfer time of ten seconds, as well as the increased thermal conductivity of a liquid environment. This test is performed per MIL STD 883, Method 1011, Condition B (-55 °C to +125 °C). Devices are placed in a fluorocarbon bath cooled to -55 °C for five minutes, then transferred to an adjacent bath filled with fluorocarbon at 125 °C for five minutes. This is equal to one cycle of thermal shock. Stressing is performed for 500 cycles. Failures are expressed in % / cycles, with results reported at 100, 200 and 500 cycles.

High Temperature Storage Life

Storage life is an environmental stress where temperature is the only stress. Stressing is performed per MIL STD 883, Method 1008, Condition C. (150 °C) Stressing is performed to 1000 hours. Failures are expressed in % / hours, with results reported at 100, 500 and 1000 hours.

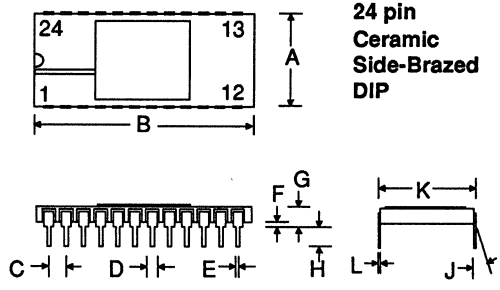
Electrostatic Discharge Testing

Electrostatic discharge testing is performed to determine the handling sensitivity of a semiconductor device. This test is performed per MIL STD 883, Method 3015 which simulates the resistance (1500 Ω) and capacitance (150 picofarads) of the human body.

CMOS Latchup Testing

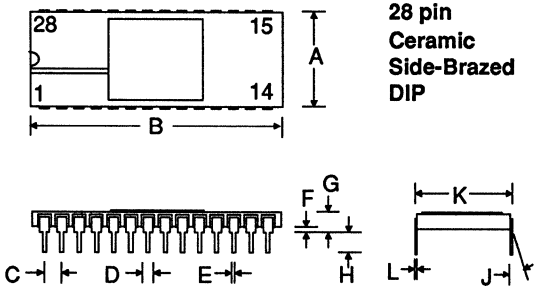
CMOS latchup testing is performed to ascertain the sensitivity of a devivce input to sustain a SCR latchup due to a DC current. The pin being tested has a DC current forced to it with the device power supplies at nominal voltage and inputs at ground state. Susceptibility of each input is tested with both a negative and positive current forced to it.

MECHANICAL DATA



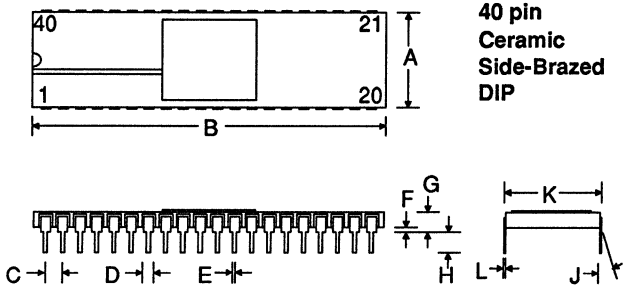
24 pin Ceramic Side-Brazed DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.73	15.34	0.580	0.604
B	27.64	33.53	1.088	1.320
C	2.54 BSC		0.100 BSC	
D	0.76	1.40	0.030	0.055
E	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.67	4.32	0.105	0.170
H	2.54	4.57	0.100	0.180
J	-	10°	-	10°
K	14.99	15.49	0.590	0.610
L	0.20	0.30	0.008	0.012



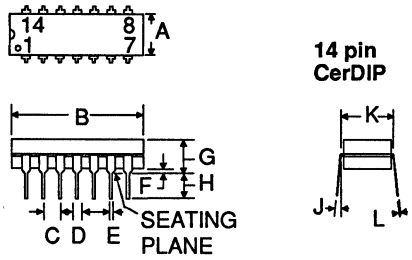
28 pin Ceramic Side-Brazed DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.73	15.34	0.580	0.604
B	35.20	35.92	1.386	1.414
C	2.54 BSC		0.100 BSC	
D	0.76	1.40	0.030	0.055
E	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.79	4.32	0.110	0.170
H	2.54	4.57	0.100	0.180
J	-	10°	-	10°
K	14.99	15.49	0.590	0.610
L	0.20	0.30	0.008	0.012



40 pin Ceramic Side-Brazed DIP

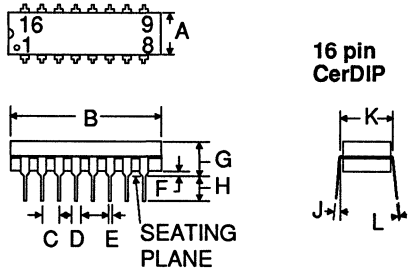
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.63	15.49	0.576	0.610
B	50.29	51.31	1.980	2.020
C	2.54 BSC		0.100 BSC	
D	0.76	1.52	0.030	0.060
E	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.79	4.32	0.110	0.170
H	2.54	4.57	0.100	0.180
J	-	10°	-	10°
K	14.99	15.65	0.590	0.616
L	0.20	0.30	0.008	0.012



14 pin CerDIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	7.49	0.240	0.295
B	19.05	19.94	0.750	0.785
C	2.54 BSC		0.100 BSC	
D	1.40	1.78	0.055	0.070
E	0.38	0.53	0.015	0.021
F	0.51	1.02	0.020	0.040
G	3.81	5.08	0.150	0.200
H	2.92	4.32	0.115	0.170
J	-	15°	-	15°
K	7.62 BSC		0.300 BSC	
L	0.20	0.30	0.008	0.012

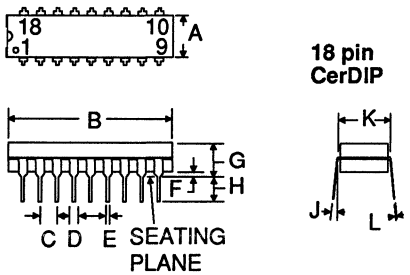
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION K TO CENTER OF LEADS WHEN FORMED PARALLEL.



16 pin CerDIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	7.49	0.240	0.295
B	19.05	19.94	0.750	0.785
C	2.54 BSC		0.100 BSC	
D	1.40	1.78	0.055	0.070
E	0.38	0.53	0.015	0.021
F	0.51	1.02	0.020	0.040
G	3.81	5.08	0.150	0.200
H	2.92	4.32	0.115	0.170
J	-	15°	-	15°
K	7.62 BSC		0.300 BSC	
L	0.20	0.30	0.008	0.012

NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION K TO CENTER OF LEADS WHEN FORMED PARALLEL.



18 pin CerDIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	7.49	0.240	0.295
B	22.35	23.11	0.880	0.910
C	2.54 BSC		0.100 BSC	
D	1.40	1.78	0.055	0.070
E	0.38	0.53	0.015	0.021
F	0.51	1.02	0.020	0.040
G	3.81	5.08	0.150	0.200
H	2.92	4.32	0.115	0.170
J	0°	15°	0°	15°
K	7.62 BSC		0.300 BSC	
L	0.20	0.30	0.008	0.012

NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION K TO CENTER OF LEADS WHEN FORMED PARALLEL.

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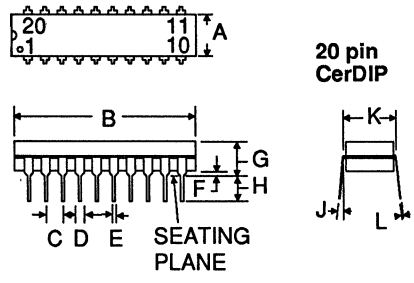
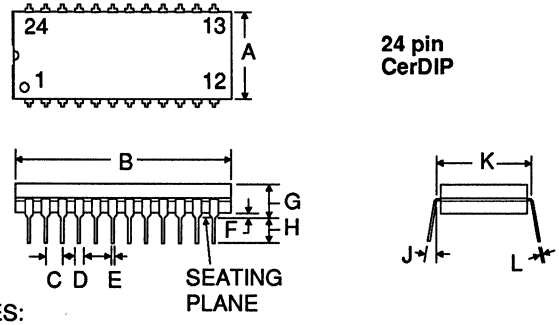


20 pin
CerDIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.60	7.49	0.260	0.295
B	23.88	25.15	0.940	0.990
C	2.54 BSC		0.100 BSC	
D	1.40	1.65	0.055	0.065
E	0.38	0.56	0.015	0.022
F	0.25	1.02	0.010	0.040
G	3.81	5.08	0.150	0.200
H	2.92	4.06	0.115	0.160
J	0°	15°	0°	15°
K	7.62 BSC		0.300 BSC	
L	0.20	0.30	0.008	0.012

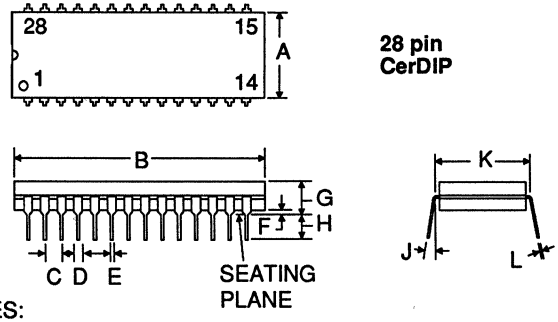
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION K TO CENTER OF LEADS WHEN FORMED PARALLEL.



24 pin
CerDIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.70	15.49	0.500	0.610
B	31.24	32.77	1.230	1.290
C	2.54 BSC		0.100 BSC	
D	1.27	1.52	0.050	0.060
E	0.41	0.51	0.016	0.020
F	0.51	1.27	0.020	0.050
G	4.06	5.59	0.160	0.220
H	2.92	4.06	0.115	0.160
J	0°	15°	0°	15°
K	15.24 BSC		0.600 BSC	
L	0.20	0.30	0.008	0.012

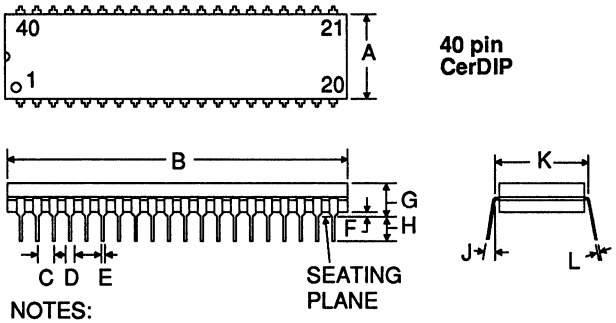
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION K TO CENTER OF LEADS WHEN FORMED PARALLEL.



28 pin
CerDIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.70	15.37	0.500	0.605
B	36.45	37.85	1.435	1.490
C	2.54 BSC		0.100 BSC	
D	1.27	1.65	0.050	0.065
E	0.38	0.56	0.015	0.022
F	0.51	1.27	0.020	0.050
G	4.06	5.84	0.160	0.230
H	2.92	4.06	0.115	0.160
J	5°	15°	5°	15°
K	15.24 BSC		0.600 BSC	
L	0.20	0.30	0.008	0.012

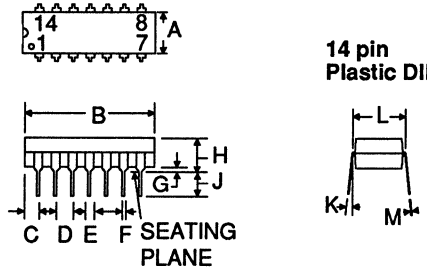
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION K TO CENTER OF LEADS WHEN FORMED PARALLEL.



40 pin CerDIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.70	15.37	0.500	0.605
B	50.29	52.57	1.980	2.070
C	2.54 BSC		0.100 BSC	
D	1.27	1.65	0.050	0.065
E	0.38	0.56	0.015	0.022
F	0.51	1.27	0.020	0.050
G	4.06	5.84	0.160	0.230
H	2.92	4.06	0.115	0.160
J	5°	15°	5°	15°
K	15.24 BSC		0.600 BSC	
L	0.20	0.30	0.008	0.012

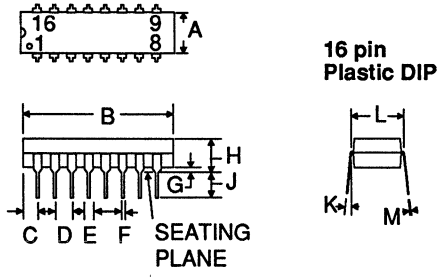
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION K TO CENTER OF LEADS WHEN FORMED PARALLEL.



14 pin Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	18.54	19.56	0.730	0.770
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.78	0.040	0.070
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.81	5.08	0.150	0.200
J	2.92	3.43	0.115	0.135
K	0°	10°	0°	10°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



16 pin Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	18.80	19.30	0.740	0.760
C	1.32	2.89	0.015	0.035
D	2.54 BSC		0.100 BSC	
E	1.02	1.78	0.040	0.070
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.81	5.08	0.150	0.200
J	2.92	3.43	0.115	0.135
K	0°	10°	0°	10°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.

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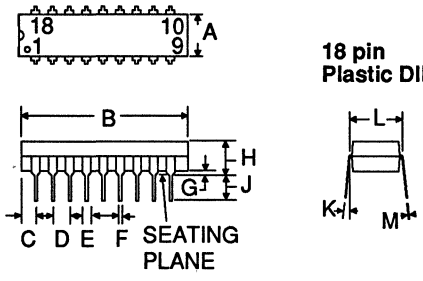
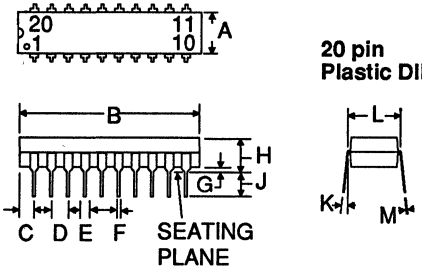


18 pin
Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	22.22	23.24	0.875	0.915
C	1.02	1.52	0.040	0.060
D	2.54 BSC		0.100 BSC	
E	1.27	1.78	0.050	0.070
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.56	4.57	0.140	0.180
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

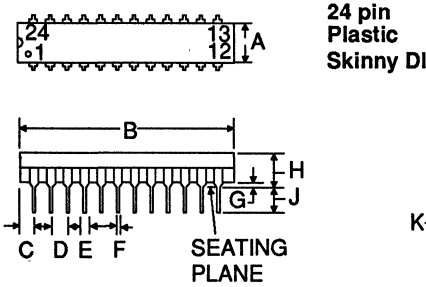
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



20 pin
Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	25.65	26.42	1.010	1.040
C	1.27	1.78	0.050	0.070
D	2.54 BSC		0.100 BSC	
E	1.27	1.78	0.050	0.070
F	0.38	0.56	0.015	0.022
G	0.51	1.02	0.020	0.040
H	3.94	4.57	0.155	0.180
J	2.79	3.56	0.110	0.140
K	0°	15°	0°	15°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

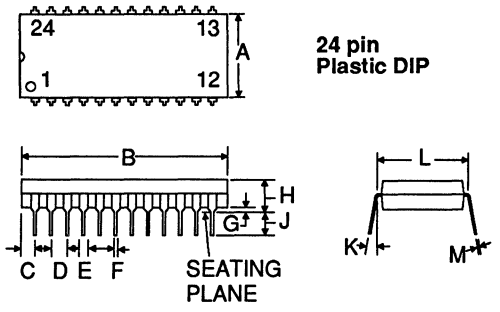
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



24 pin
Plastic
Skinny DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	31.37	32.13	1.235	1.265
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	4.57	0.155	0.180
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	7.62 BSC		0.300 BSC	
M	0.20	0.38	0.008	0.015

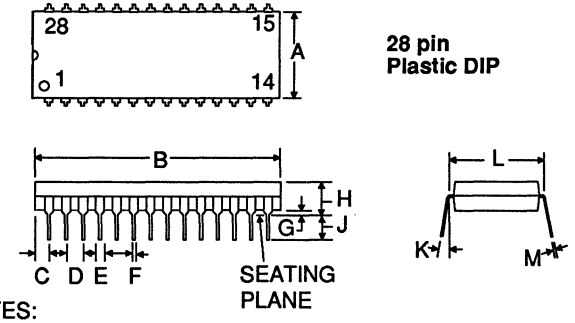
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



24 pin
Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	13.72	14.22	0.540	0.560
B	31.37	32.13	1.235	1.265
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	5.08	0.155	0.200
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	15.24 BSC		0.600 BSC	
M	0.20	0.38	0.008	0.015

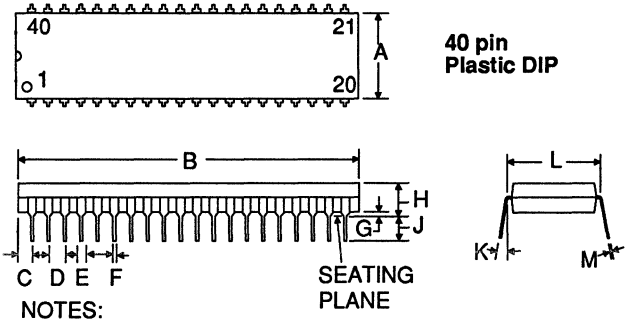
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



28 pin
Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	13.72	14.22	0.540	0.560
B	36.45	37.21	1.435	1.465
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	5.08	0.155	0.200
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	15.24 BSC		0.600 BSC	
M	0.20	0.38	0.008	0.015

NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



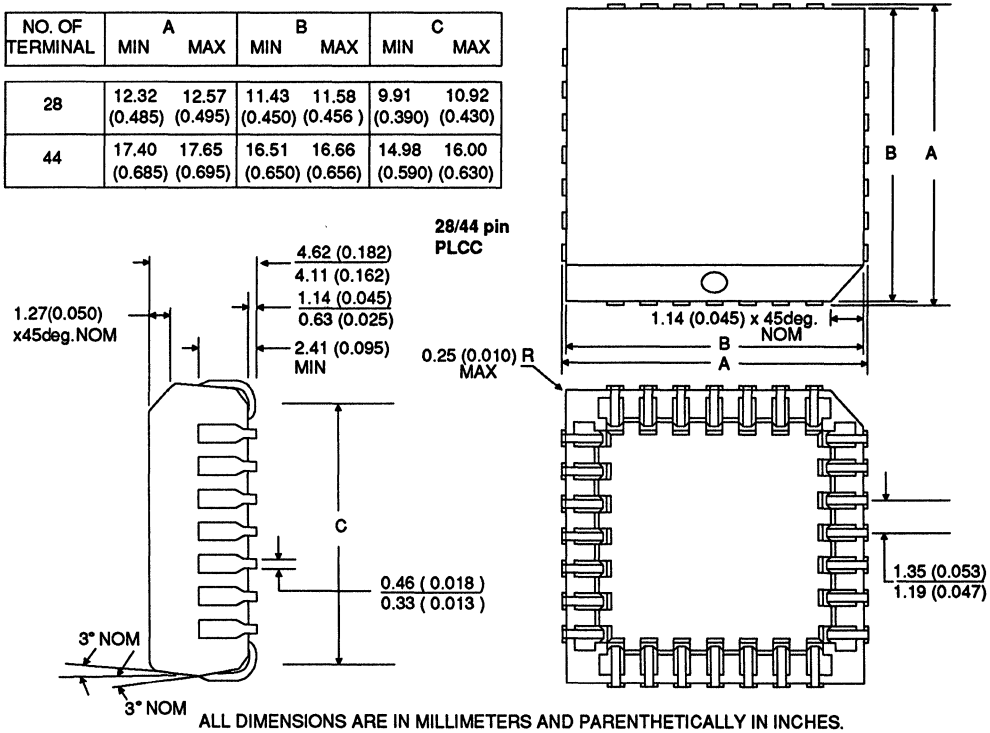
40 pin
Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	13.72	14.22	0.540	0.560
B	51.69	52.45	2.035	2.065
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	5.08	0.155	0.200
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	15.24 BSC		0.600 BSC	
M	0.20	0.38	0.008	0.015

NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.

12

NO. OF TERMINAL	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
28	12.32 (0.485)	12.57 (0.495)	11.43 (0.450)	11.58 (0.456)	9.91 (0.390)	10.92 (0.430)
44	17.40 (0.685)	17.65 (0.695)	16.51 (0.650)	16.66 (0.656)	14.98 (0.590)	16.00 (0.630)



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

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DEFINITION OF PRELIMINARY PART TYPES

Before a part is in full production, Crystal will supply preliminary parts. There are two varieties:

I.Engineering Sample (ES)

Engineering sample "ES" is a product which has not been completely characterized or where qualification has not reached the first lot 500 hours read point. ES product will be assembled per manufacturing specs at qualified assembly sites. All units will be tested to a published data sheet and applicable errata sheet (if needed). Any ES units which are tested only at room temperature will receive a supplemental brand "25°". As soon as automated temperature testing is available for this device, all subsequent ES units will be 100% temperature tested.

The following premium - temperature product grades will always be 100% tested at temperature:

TELECOMMUNICATIONS - "M" grade
DATA ACQUISITION - "A", "B", "C", "S", "T", and "U" grades

II. Engineering Prototype (EP)

Engineering Prototype is an engineering prototype of a device which works sufficiently for beta site purposes.

DEFINITION OF DATA SHEET TYPES

Each product developed by Crystal will be supported by technical literature where the data sheets progress through the following levels of refinement:

I. Product Preview

This is a 1-to-4 page document which describes the main features and specifications for a product that is under development. Some specifications such as exact pin-outs may not be finalized at time of publication. The purpose of this document is to provide customers with advance product planning information.

II. Preliminary Product Information

This is the first document completely describing a new product. It contains an overview, specifications, timing diagrams, theory of operation, pin-out diagram, applications information, ordering guide and mechanical information. The numbers in this data sheet are based on prototype silicon performance and on worst-case simulation models. The specifications represent the designer's best estimate for the "real" numbers. Min and max values are included where possible. The purpose of this document is to provide system designers with technical information sufficiently detailed to guarantee that they can safely begin active development.

III. Final Data Sheet

This is an updated version of the preliminary data sheet reflecting actual production performance of the final product. Updates include tighter specifications, more min and max values, and any application information that has arisen during the early life of the part. The purpose of this document is to communicate the confirmed performance of products which have passed qualification, been fully characterized, and are in production.

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