CS5394

117 dB, 48 kHz Audio A/D Converter

Features

- 24-Bit Resolution
- Complete CMOS Stereo A/D System
  - Delta-Sigma A/D Converters
  - Digital Anti-Alias Filtering
  - S/H Circuitry and Voltage Reference
- Adjustable System Sampling Rates
  - including 32 kHz, 44.1 kHz and 48 kHz
- 117dB Dynamic Range (A-Weighted)
- Low Noise and Distortion
  - >103 dB THD + N
- Differential Analog Circuitry
- Internal 64x Oversampling
- Linear Phase Digital Anti-Alias Filtering
  - with >117 dB Stopband Attenuation
- Single +5 V Power Supply
- Power Down Mode

Description

The CS5394 is a complete analog-to-digital converter for stereo digital audio systems. It performs sampling, analog-to-digital conversion and anti-alias filtering, generating 24-bit values for both left and right inputs in serial form. The output sample rate can be up to 50 kHz per channel.

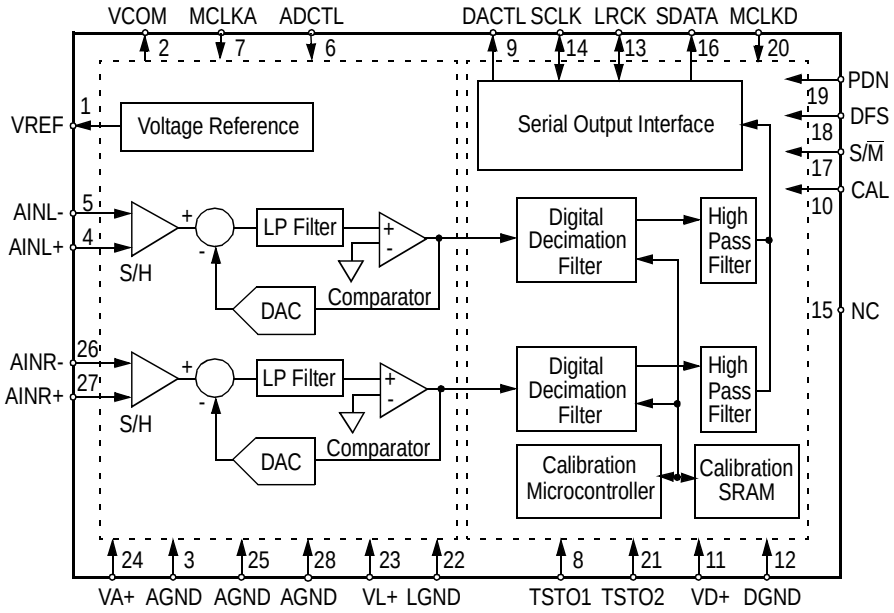
The CS5394 uses 7th-order, delta-sigma modulation with 64x oversampling followed by digital filtering and decimation, which removes the need for an external anti-alias filter. The ADC uses a differential architecture which provides excellent noise rejection.

The CS5394 has a linear phase filter with passband of dc to 22.1 kHz, 0.005 dB passband ripple and >117 dB stopband rejection.

The CS5394 is targeted for the highest performance professional audio systems requiring wide dynamic range, negligible distortion and low noise.

ORDERING INFORMATION

CS5394-KS -10° to 70° C 28-pin SOIC



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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ANALOG CHARACTERISTICS (T_A = 25° C; VA+, VL+,VD+ = 5 V; Full-scale Input Sinewave, 997 Hz; Fs = 48 kHz; SCLK = 3.072 MHz; Analog connections as shown in Figure 1; Measurement Bandwidth is 20 Hz to 20 kHz unless otherwise specified; Logic 0 = 0V, Logic 1 = VD+.

Parameter		Symbol	Min	Typ	Max	Units
Resolution		-	24	-	-	Bits
Dynamic Performance						
Dynamic Range		-	TBD	114	-	dB
	(A-weighted)		TBD	117	-	dB
Total Harmonic Distortion + Noise	-1.0 dB (Note 1)	THD+N	TBD	103	-	dB
	-20 dB (Note 1)		TBD	94	-	dB
	-60 dB (Note 1)		TBD	54	-	dB
Total Harmonic Distortion	-1.0 dB (Note 1)	THD	TBD	0.0007	-	%
Interchannel Phase Deviation		-	-	0.01	-	°
Interchannel Isolation		-	-	118	-	dB
dc Accuracy						
Interchannel Gain Mismatch		-	-	0.05	-	dB
Gain Error		-	-		5	%
Gain Drift		-	-	100	-	ppm/°C
Bipolar Offset Error	with High Pass filter (Note 2)	-	-	512	-	LSB
Analog Input						
Full-scale Differential Input Voltage	(Note 3)	V_{IN}	3.8	4.0	4.2	V_{pp}
Input Impedance		Z_{IN}	-	4.5	-	kΩ
Common-Mode Rejection Ratio	1 kHz	CMRR	-	82	-	dB
Power Supplies						
Power Supply Current	(VA+)+(VL+)	I_A+	-	140	TBD	mA
(Normal Operation)	VD+	I_D+	-	40	TBD	mA
Power Supply Current	(VA+)+(VL+)	I_A+	-	100	-	µA
(Power-Down Mode)	VD+	I_D+	-	100	-	µA
Power Consumption			-	900	TBD	mW
	(Power-Down)		-	1.0	-	mW
Power Supply Rejection Ratio	(1 kHz)	PSRR	-	60	-	dB

Notes: 1. Referenced to typical full-scale differential input voltage (4.0 Vpp).
2. Digital offset is added following high pass filter to avoid the idle channel noise degradation that can result from the transition between 0 and -1 in a two's complement system.
3. Specified for a fully differential input ±{(AINR+)-(AINR-)}. The ADC accepts input volta analog supplies (VA+ and AGND). Full-scale outputs will be produced for differential inputs beyond V_{IN}.

* Refer to *Parameter Definitions* at the end of this data sheet.

Specifications are subject to change without notice.

DIGITAL FILTER CHARACTERISTICS

(T_A = 25 °C; VA+, VL+ ,VD+ = 5V ± 5%; Fs = 48 kHz)

Parameter			Symbol	Min	Typ	Max	Units
Passband	(-0.01 dB)	(Note 4)		0	-	22.1	kHz
Passband Ripple				-	-	±0.005	dB
Stopband		(Note 4)		26.6	-	3050	kHz
Stopband Attenuation		(Note 5)		117	-	-	dB
Group Delay (Fs = Output Sample Rate)			t_{gd}	-	34/Fs	-	µs
Group Delay Variation vs Frequency			Δt_{gd}	-	-	0.0	µs
High Pass Filter Characteristics							
Frequency Response:	-3 dB -0.036dB	(Note 4)		- -	1.8 20	- -	Hz Hz
Phase Deviation	@ 20 Hz	(Note 4)		-	5.3	-	Degree
Passband Ripple				-	-	0	dB

Notes: 4. Filter characteristic scales with sample rate.

5. The analog modulator samples the input at 3.072 MHz for Fs equal to 48 kHz. There is no rejection of input signals which are (n x 3.072 MHz) ±22.1 kHz, where n = 0,1,2,3...

DIGITAL CHARACTERISTICS

(T_A = 25 °C; VA+, VL+ ,VD+ = 5V ± 5%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.4	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage at I_O = -20 µA	V_{OH}	(VD+) - 1.0	-	-	V
Low-Level Output Voltage at I_O = 20 µA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	±10	mA

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, All voltages with respect to ground.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Analog	VA+	-0.3	-	+6.0	V
	Positive Logic	VL+	-0.3	-	+6.0	V
	Positive Digital	VD+	-0.3	-	+6.0	V
	|VA+ - VD+|		-	-	0.4	V
	|VA+ - VL+|		-	-	0.4	V
	|VD+ - VL+|		-	-	0.4	V
Input Current	(Note 6)	I_{in}	-	-	±10	mA
Analog Input Voltage	(Note 7)	V_{INA}	-0.7	-	(VA+)+0.7	V
Digital Input Voltage	(Note 7)	V_{IND}	-0.7	-	(VD+)+0.7	V
Ambient Operating Temperature (Power Applied)		T_A	-55	-	+125	°C
Storage Temperature		T_{stg}	-65	-	+150	°C

Notes: 6. Any pin except supplies. Transient currents of up to +/-100 mA on the analog input pins will not cause SCR latch-up.

7. The maximum over/under voltage is limited by the input current.

WARNING: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AGND, DGND = 0V, all voltages with respect to ground.)

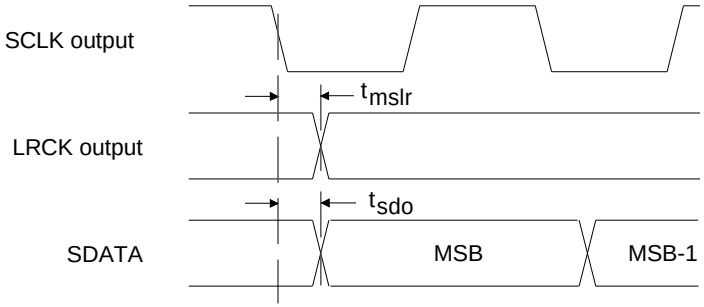
Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.75	5.0	5.25	V
	Positive Logic	VL+	4.75	5.0	5.25	V
	Positive Analog	VA+	4.75	5.0	5.25	V
	|VA+ - VD+|		-	-	0.4	V

SWITCHING CHARACTERISTICS

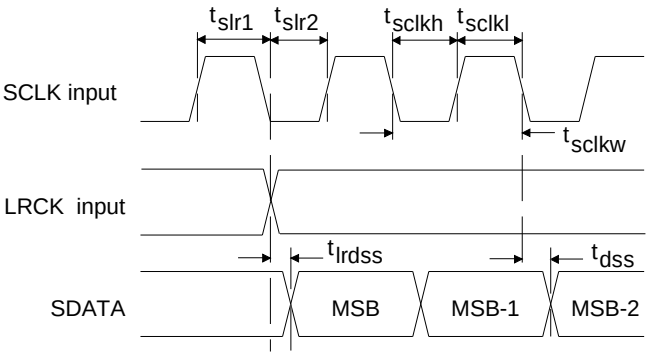
(T_A = 25 °C; VA+ = 5V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = VA+ = VD+; C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Units
Output Sample Rate	F_s	2	-	50	kHz
MCLK Period	t_{clkw}	78	-	1950	ns
MCLK Low	t_{clkl}	26	-	-	ns
MCLK High	t_{clkh}	26	-	-	ns
MASTER MODE					
SCLK falling to LRCK	t_{mslr}	- 20	-	+ 20	ns
SCLK falling to SDATA valid	t_{sdo}	-	-	20	ns
SCLK Duty cycle		-	50	-	%
SLAVE MODE					
LRCK Period	1/ F_s	20	-	500	µs
LRCK duty cycle		-	50	-	%
SCLK Period	t_{sclkw}	(Note 8)	-	-	ns
SCLK Pulse Width Low	t_{sclkl}	(Note 9)	-	-	ns
SCLK Pulse Width High	t_{sclkh}	60	-	-	ns
SCLK falling to SDATA valid	t_{dss}	-	-	(Note 10)	ns
LRCK edge to MSB valid	t_{lrdss}	-	-	(Note 10)	ns
SCLK rising to LRCK edge delay	t_{slr1}	(Note 10)	-	-	ns
LRCK edge to rising SCLK setup time	t_{slr2}	(Note 10)	-	-	ns

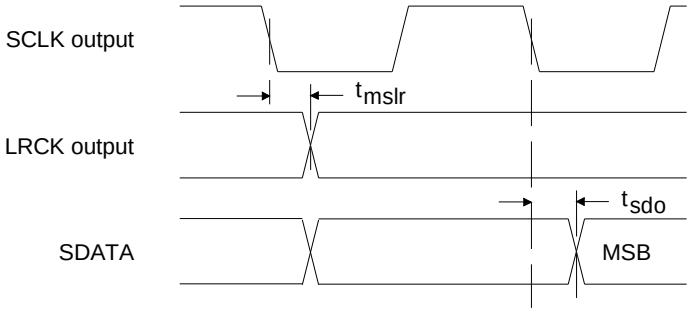
Notes: 8. $\frac{1}{64\ F_s}$ 9. $\frac{1}{128\ F_s}$ 10. $\frac{1}{256\ F_s}$ +20 ns



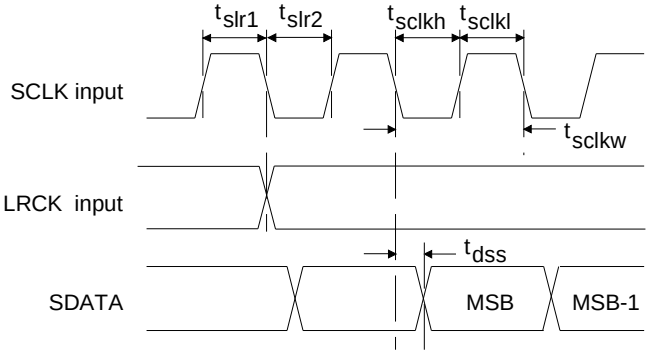
SCLK to SDATA & LRCK - MASTER mode
Serial Data Format, DFS low



SCLK to LRCK & SDATA - SLAVE mode
Serial Data Format, DFS low



SCLK to SDATA & LRCK - MASTER mode
Serial Data Format, DFS high
I^2S compatible



SCLK to LRCK & SDATA - SLAVE mode
Serial Data Format, DFS high
I^2S compatible

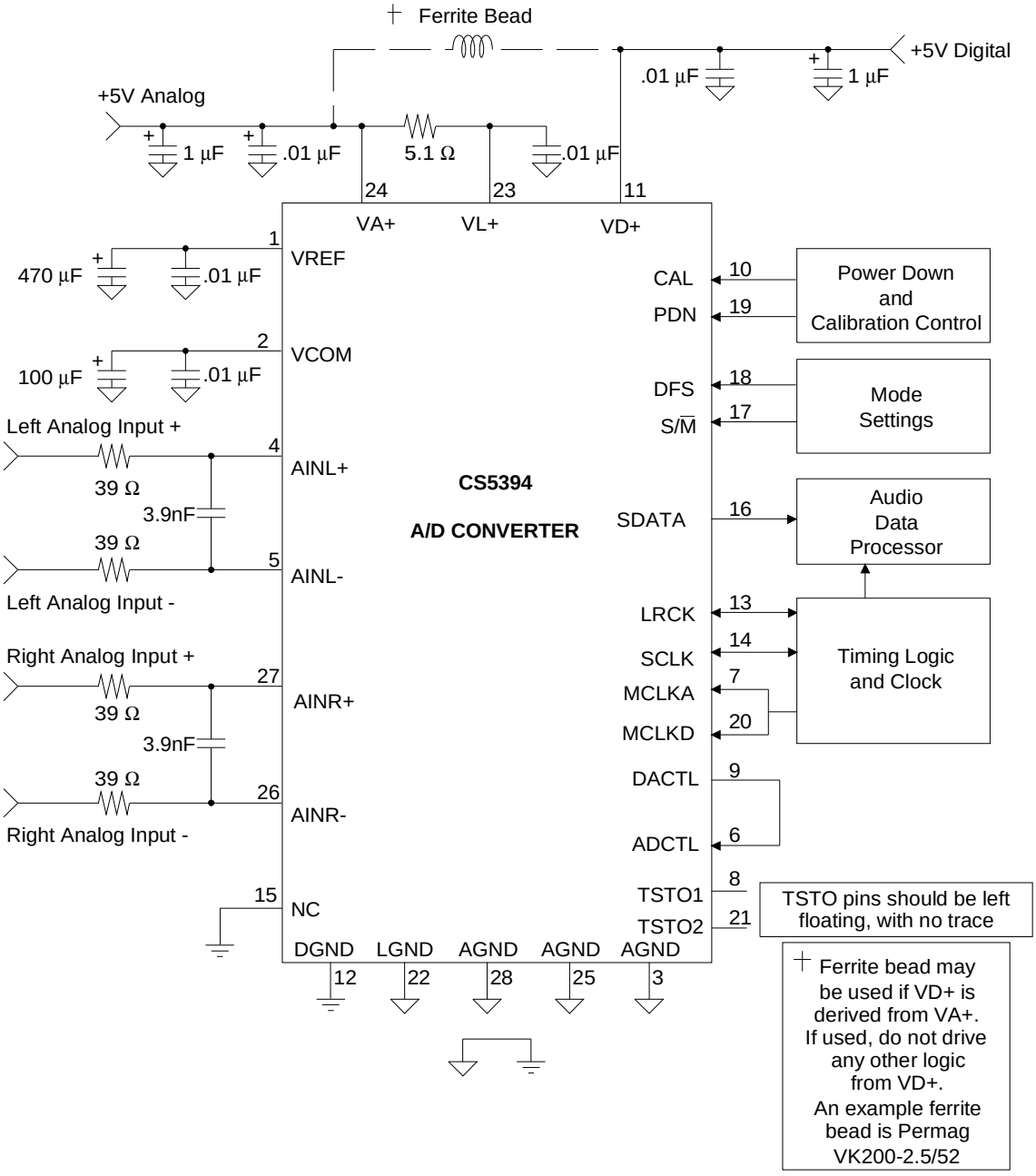


Figure 1. Typical Connection Diagram

GENERAL DESCRIPTION

The CS5394 is a 24-bit, stereo A/D converter designed for stereo digital audio applications. The device uses a patented, 7th-order tri-level delta-sigma modulator to sample the analog input signals at 64 times the output sample rate (Fs) of the device. Sample rates of up to 50 kHz are supported. The analog input channels are simultaneously sampled by separate delta-sigma modulators. The resulting serial bit streams are digitally filtered, yielding pairs of 24-bit values. This technique yields nearly ideal conversion performance independent of input frequency and amplitude. The converter does not require difficult-to-design or expensive anti-alias filters and it does not require external sample-and-hold amplifiers or voltage references.

An on-chip voltage reference provides for a differential input signal range of 4.0 Vpp. The device also contains a high pass filter, implemented digitally after the decimation filter, to completely eliminate any internal offsets in the converter or any offsets present at the input circuitry to the device. Output data is available in serial form, coded as 2's complement 24-bit numbers. The typical power consumption of 900 mW can be reduced by use of the power-down mode.

For more information on delta-sigma modulation techniques see the references at the end of this data sheet.

SYSTEM DESIGN

Very few external components are required to support the ADC. Normal power supply decoupling components, voltage reference bypass capacitors and a single resistor and capacitor on each input for anti-aliasing are all that's required, as shown in Figure 1.

Master Clock

The master clock is the clock source for the delta-sigma modulator (MCLKA) and digital filters (MCLKD). The required MCLKA/D frequencies are determined by the desired Fs and must be 256× Fs. The CS5394 operates at a 48 kHz sample rate when using a 12.288 MHz master clock. Table 1 shows some common master clock frequencies.

LRCK (kHz)	MCLKA/D (MHz)	SCLK (MHz)
32	8.192	2.048
44.1	11.2896	2.822
48	12.288	3.072

Table 1. Common Clock Frequencies

SERIAL DATA INTERFACE

The CS5394 supports two serial data formats, including I^2S, which are selected via the digital format select pin, DFS. The digital input format determines the relationship between the serial data, left/right clock and serial clock. Figures 2 and 3 detail the interface formats. The serial data interface is accomplished via the serial data output, SDATA, serial data clock, SCLK, and the left/right clock, LRCK. The serial nature of the output data results in the left and right data words being read at different times. However, the samples within an LRCK cycle represent simultaneously sampled analog inputs.

Serial Data

The serial data block consists of 24 bits of audio data presented in 2's-complement format with the MSB-first. The data is clocked from SDATA by the serial clock and the channel is determined by the Left/Right clock.

Serial Clock

The serial clock shifts the digitized audio data from the internal data registers via the SDATA pin. SCLK is an output in Master Mode where internal dividers will divide the master clock by 4 to generate a serial clock which is 64× Fs. In Slave Mode, SCLK is an input with a serial clock typically between 48× and 128× Fs. It

is recommended that SCLK be equal to 64× Fs, though other frequencies are possible, to avoid potential interference effects which may degrade system performance.

Left / Right Clock

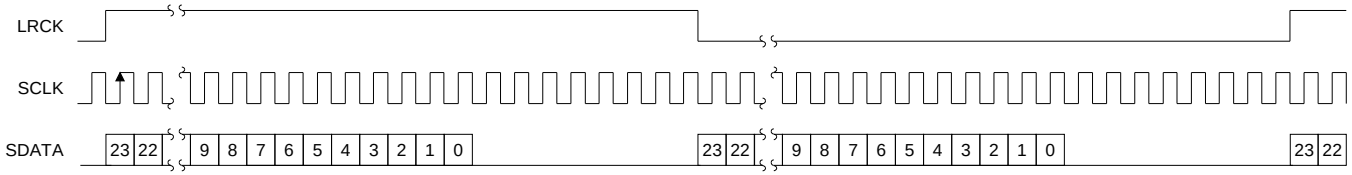
The Left/Right clock, LRCK, determines which channel, left or right, is to be output on SDATA. In Master Mode, LRCK is an output whose frequency is equal to Fs. In Slave Mode, LRCK is an input whose frequency must be equal to Fs and synchronous to MCLKA/D.

Master Mode

In Master mode, SCLK and LRCK are outputs which are internally derived from the master clock. Internal dividers will divide MCLKA/D by 4 to generate a SCLK which is 64× Fs and by 256 to generate a LRCK which is equal to Fs. The CS5394 is placed in the Master mode with the slave/master pin, S/$\overline{M}$, low.

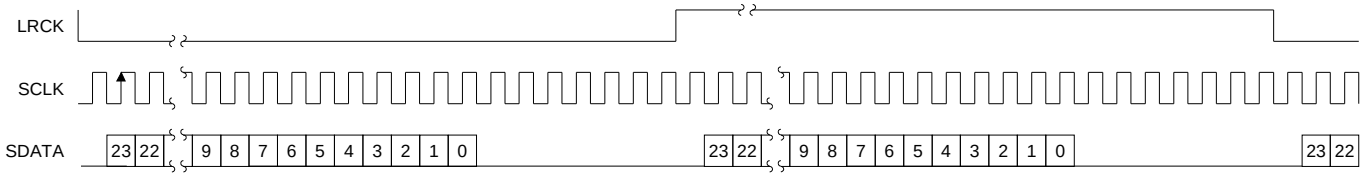
Slave Mode

LRCK and SCLK become inputs in slave mode. LRCK must be externally derived from MCLKA/D and be equal to Fs. It is recommended that SCLK be equal to 64×. Other frequencies between 48× and 128× Fs are possible but may degrade system performance due to interference effects. The master clock frequency must be 256× Fs. The CS5394 is placed in the Slave mode with the slave/master pin, S/$\overline{M}$, high.



MASTER	SLAVE
24-Bit Left Justified Data Data Valid on Rising Edge of 64x SCLK MCLK equal to 256x F_S	24-Bit Left Justified Data Data Valid on Rising Edge of SCLK MCLK equal to 256x F_S

Figure 2. Serial Data Format, DFS low.



MASTER	SLAVE
I^2S 24-Bit Data Data Valid on Rising Edge of 64x SCLK MCLK equal to 256x F_S	I^2S 24-Bit Data Data Valid on Rising Edge of SCLK MCLK equal to 256x F_S

Figure 3 Serial Data Format, DFS High (I^2S compatible).

Analog Connections

Figure 1 shows the analog input connections. The analog inputs are presented differentially to the modulators via the AINR+/- and AINL+/- pins. Each analog input will accept a maximum of 2.0 Vpp. The + and - input signals are 180° out of phase resulting in a differential input voltage of 4.0 Vpp. Figure 4 shows the input signal levels for full scale. Input signals can be AC or DC coupled. The VCOM output is available to filter the internal common mode and is not intended to be used as a external reference for DC coupling.

The CS5394 samples the analog inputs at 64× Fs, 3.072 MHz for a 48 kHz sample-rate. The digital filter rejects all noise above 26.6 kHz except for frequencies at 3.072 MHz ± 22.1 kHz (and multiples of 3.072 MHz). Most audio signals do not have significant energy at 3.072 MHz. Nevertheless, a 39 Ω resistor in series with each analog input and a 3.9 nF capacitor across the inputs will attenuate any noise energy at 3.072 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient must be avoided since these will degrade signal linearity. NPO and COG capacitors are acceptable. If active circuitry precedes the ADC, it is recommended that the above RC filter is placed between the active circuitry and the AINR and AINL pins. The above example frequencies scale linearly with sample rate.

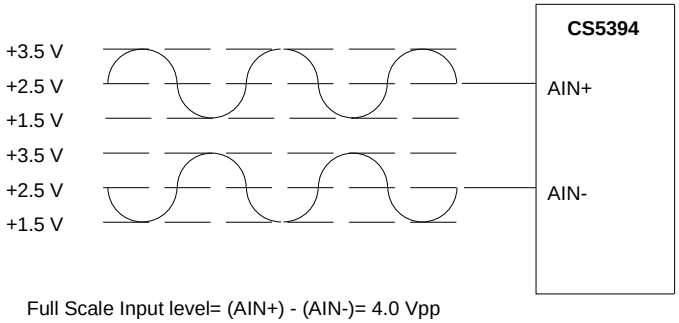


Figure 4. Full Scale Input Voltage

The on-chip voltage reference is available at VREF for the purpose of decoupling only. The circuit traces attached to this pin must be minimal in length and no load current may be taken from VREF. The recommended decoupling scheme, Figure 1, is a 470 µF electrolytic capacitor and a 0.01 µF ceramic capacitor connected from VREF to AGND. The decoupling capacitors, particularly the 0.01 µF, must be positioned to minimize the electrical path from VREF and pin 3, AGND, on the printed circuit board.

High Pass Filter

The CS5394 includes a high pass filter after the decimator to remove the indeterminate DC offsets introduced by the analog buffer stage and the CS5394 analog modulator. A 512 LSB offset is added, following the digital high pass filter, to avoid potential noise coupling that can result from the digital transient currents induced with the transition between 0 and -1 in a two's complement system. Therefore, there is is a fixed offset of 512 LSB's.

The characteristics of this first-order high pass filter are outlined below for Fs equal to 48 kHz. The filter response scales linearly with sample rate.

Frequency response:	-3 dB @ 2.0 Hz
	-0.036 dB @ 20 Hz
Phase deviation:	5.3 degrees @ 20 Hz
Passband ripple:	None

Power-up and Calibration

The delta-sigma modulators settle in a matter of microseconds after the analog section is powered, either through the application of power or by exiting the power-down mode. However, the voltage reference will take much longer to reach a final value due to the presence of external capacitance on the VREF pin. A time delay of approximately 10 ms/µF is required after applying power to the device or after exiting a power down state. The typical connection diagram of Figure 1 requires a 5 second delay.

A calibration of the tri-level delta-sigma modulator should always be initiated following power-up and after allowing sufficient time for the voltage on the external VREF capacitor to settle. This is required to minimize noise and distortion. Calibration is activated on a rising edge applied to the CAL pin and requires 2050 LRCK cycles. It is also advised that the CS5394 be calibrated after the device has reached thermal equilibrium to maximize performance.

Grounding and Power Supply Decoupling

As with any high resolution converter, the ADC requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows the recommended power arrangements, with VA+ and VL+ connected to a clean +5 V supply. VD+, which powers the digital filter, may be run from the system +5V logic supply, provided that it is not excessively noisy (< ± 50 mV pk-to-pk). Alternatively, VD+ may be powered from VA+ via a ferrite bead. In this case, no additional devices should be powered from VD+. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the ADC as possible, with the low value ceramic capacitor being the nearest.

The printed circuit board layout should have separate analog and digital regions and ground planes, with the ADC straddling the boundary. All signals, especially clocks, should be kept away from the VREF pin in order to avoid unwanted coupling into the modulators. The VREF decoupling capacitors, particularly the 0.01 µF, must be positioned to minimize the electrical path from VREF and pin 3, AGND. The CDB5394 evaluation board demonstrates the optimum layout and power supply arrangements, as well as allowing fast evaluation of the ADC.

To minimize digital noise, connect the ADC digital outputs only to CMOS inputs.

Additional printed circuit board design and circuit design hints are included in the application note, "Layout and Design Rules for Data Converters" and the Audio Engineering Society paper "How to Achieve Optimum Performance from Delta-Sigma A/D & D/A Converters".

PERFORMANCE

Digital Filter

Figures 5-8 show the performance of the digital filter included in the ADC. All plots are normalized to Fs. Assuming a sample rate of 48 kHz, the 0.5 frequency point on the plot refers to 24 kHz. The filter frequency response scales precisely with Fs.

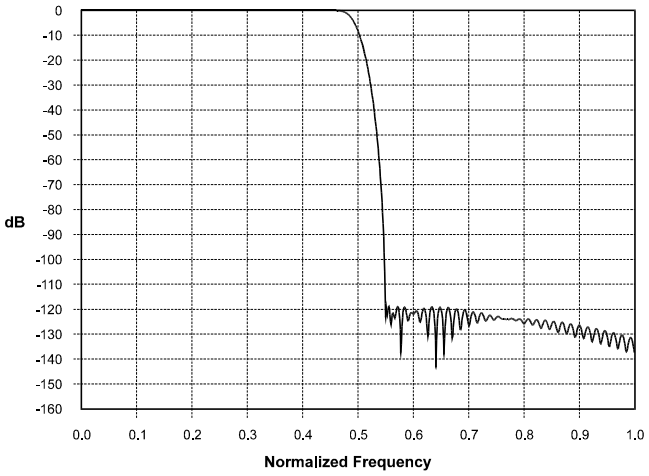


Figure 5. CS5394 Stopband Attenuation

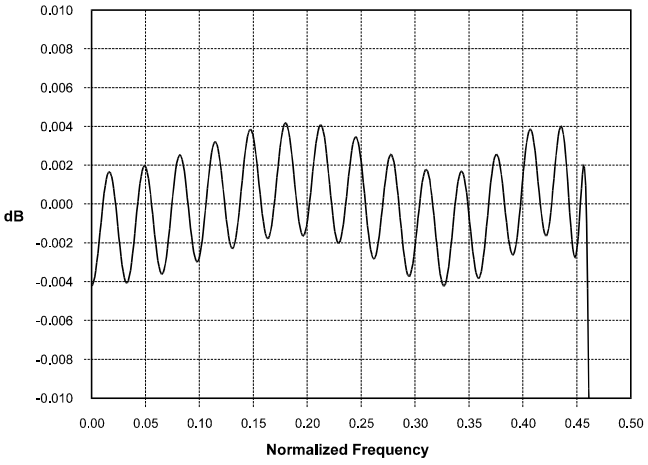


Figure 6. CS5394 Passband Ripple

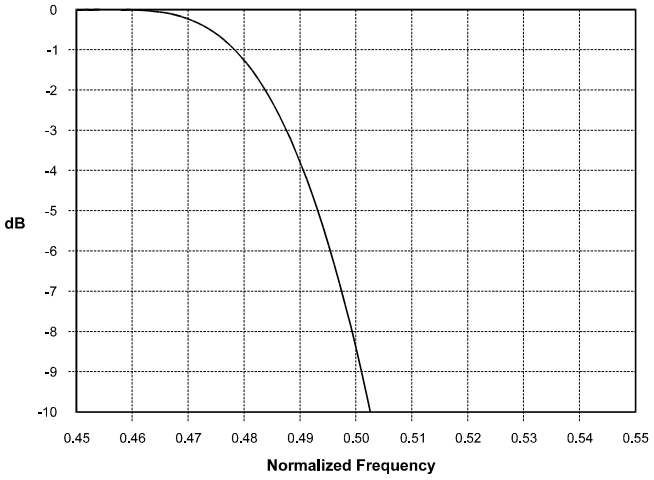


Figure 7. CS5394 Transition Band

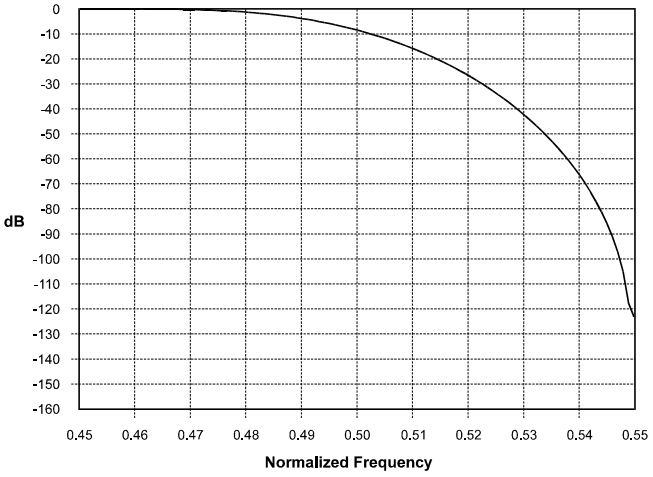
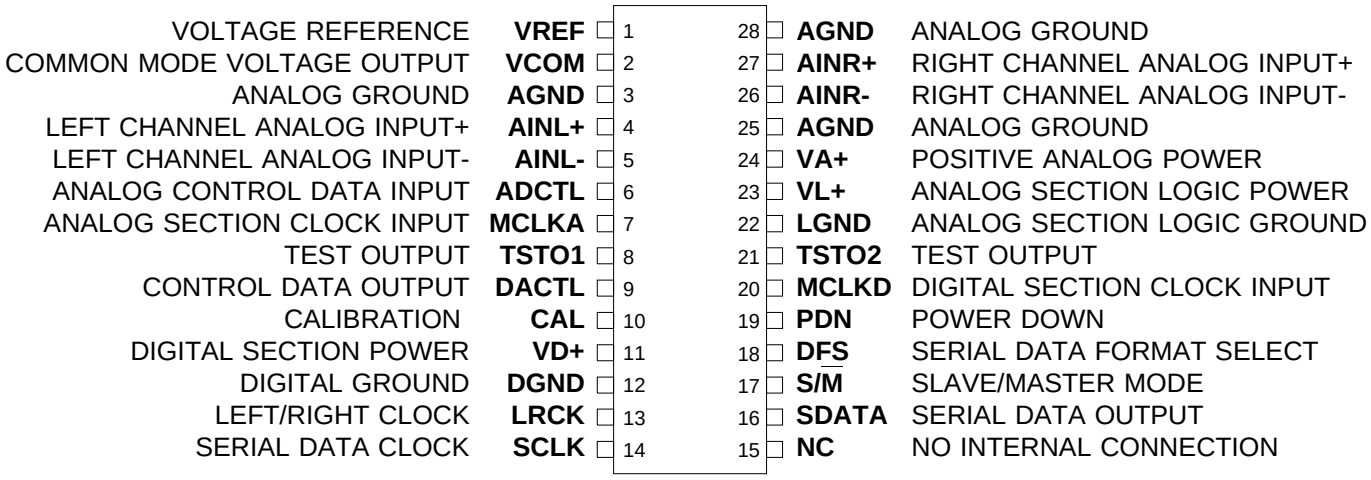


Figure 8. CS5394 Transition Band

PIN DESCRIPTIONS



Power Supply Connections

VA+ - Positive Analog Power, Pin 24.
Positive analog supply. Nominally +5 volts.

VL+ - Positive Logic Power, Pin 23.
Positive logic supply for the analog section. Nominally +5 volts.

AGND - Analog Ground, Pins 3, 25 and 28.
Analog ground reference.

LGND - Logic Ground, Pin 22.
Ground reference for the logic portions of the analog section.

VD+ - Positive Digital Power, Pin 11.
Positive supply for the digital section. Nominally +5 volts.

DGND - Digital Ground, Pin 12.
Digital ground reference for the digital section.

Analog Inputs

AINR-, AINR+ - Differential Right Channel Analog Inputs, Pins 26 and 27.
Analog input connections for the right channel differential inputs. Nominally 4.0 Vpp differential for full-scale digital output.

AINL-, AINL+ - Differential Left Channel Analog Inputs, Pins 4 and 5.
Analog input connections for the left channel differential inputs. Nominally 4.0 Vpp differential for full-scale digital output.

Analog Outputs

VCOM - Common Mode Voltage Output, Pin 2.

Nominally +2.5 volts. Requires a 100 µF electrolytic capacitor in parallel with 0.01 µF ceramic capacitor for decoupling to AGND. It is not recommended that this output be used to bias the analog input buffer circuits.

VREF - Voltage Reference Output, Pin 1.

Nominally +4 volts. Requires a 470 µF electrolytic capacitor in parallel with 0.01 µF ceramic capacitor for decoupling to AGND.

Digital Inputs

ADCTL - Analog Control Input, Pin 6.

Must be connected to DACTL. This signal enables communication between the analog and digital circuits.

DFS - Digital Format Select, Pin 18.

The relationship between LRCK, SCLK and SDATA is controlled by the DFS pin. When high, the serial output data format is I^2S compatible. The serial data format is left-justified when low.

CAL - Calibration, Pin 10.

Activates the calibration of the tri-level delta-sigma modulator on the rising edge of the CAL input.

MCLKA - Analog Section Input Clock, Pin 7.

This clock is internally divided and controls the delta-sigma modulators. An MCLKA frequency of 12.288 MHz sets a modulator sampling rate of 3.072 MHz and a output sample rate of 48 kHz. MCLKA must be connected to MCLKD.

MCLKD - Digital Section Input Clock, Pin 20.

MCLKD clocks the digital filter and must be connected to MCLKA. The required MCLKD frequency is determined by the desired sample rate. A MCLKD of 12.288 MHz corresponds to Fs equal to 48 kHz. MCLKA must be connected to MCLKD.

PDN - Power Down, Pin 19.

When high, the device enters power down. Upon returning low, the device enters normal operation.

S/$\overline{\text{M}}$ - Slave or Master Mode, Pin 17.

When high, the device is configured for Slave mode where LRCK and SCLK are inputs. The device is configured for Master mode where LRCK and SCLK are outputs when S/$\overline{\text{M}}$ is low.

Digital Outputs

DACTL- Digital to Analog Control Output, PIN 9.

Must be connected to ADCTL. This signal enables communication between the digital and analog circuits.

SDATA - Digital Audio Data Output, Pin 16.

The 24-bit audio data is presented MSB first, in 2's complement format.

Digital Inputs or Outputs

LRCK - Left/Right Clock, Pin 13.

LRCK determines which channel, left or right, is to be output on SDATA. The relationship between LRCK, SCLK and SDATA is controlled by the Digital Format Select (DFS) pin. Although the outputs for each channel are transmitted at different times, Left/Right pairs represent simultaneously sampled analog inputs. In master mode, LRCK is an output whose frequency is equal to Fs. In Slave Mode, LRCK is an input whose frequency must be equal to Fs.

SCLK - Serial Data Clock, Pin 14.

Clocks the individual bits of the serial data from SDATA. The relationship between LRCK, SCLK and SDATA is controlled by the Digital Format Select (DFS) pin. In master mode, SCLK is an output clock at 64× Fs. In slave mode, SCLK is an input which requires a continuously supplied clock at any frequency from 48× to 128× Fs (64× is recommended).

Miscellaneous

TSTO1, TSTO2 - Test Outputs, Pins 8 and 21.

These pins are intended for factory test outputs. They must not be connected to any external component or any length of circuit trace.

NC - No Connection, Pin 15

This pin is not connected internally and should be connected to DGND to minimize noise coupling.

PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified band width made with a -60 dBFs signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified band width (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFs as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

REFERENCES

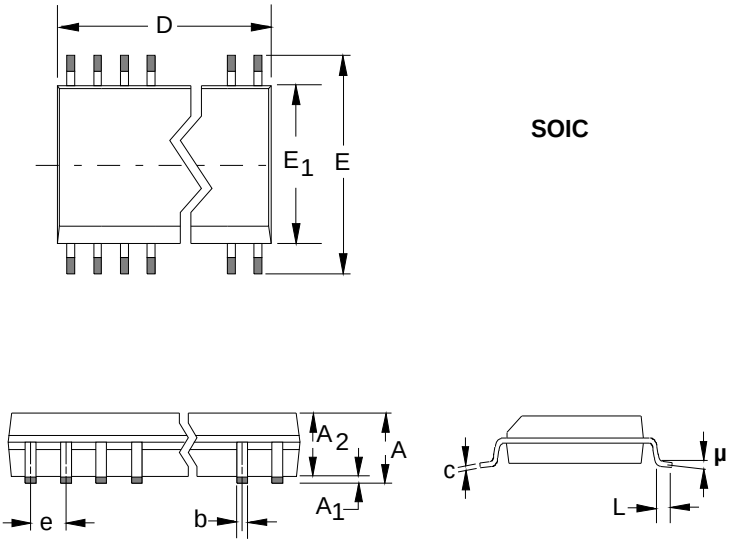
1) "A Fifth-Order Delta-Sigma Modulator with 110 dB Audio Dynamic Range" by I. Fujimori, K. Hamashita and E.J. Swanson. Paper presented at the 93rd Convention of the Audio Engineering Society, October 1992.

2) "A Stereo 16-bit Delta-Sigma A/D Converter for Digital Audio" by D.R. Welland, B.P. Del Signore, E.J. Swanson, T. Tanaka, K. Hamashita, S. Hara, K. Takasuka. Paper presented at the 85th Convention of the Audio Engineering Society, November 1988.

3) " The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters, and on Oversampling Delta Sigma ADC's" by Steven Harris. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

4) " An 18-Bit Dual-Channel Oversampling Delta-Sigma A/D Converter, with 19-Bit Mono Application Example" by Clif Sanchez. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

5) " How to Achieve Optimum Performance from Delta-Sigma A/D and D/A Converters" by Steven Harris. Presented at the 93rd Convention of the Audio Engineering Society, October 1992.



SOIC

pins	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
16	9.91	10.16	10.41	0.390	0.400	0.410
20	12.45	12.70	12.95	0.490	0.500	0.510
24	14.99	15.24	15.50	0.590	0.600	0.610
28	17.53	17.78	18.03	0.690	0.700	0.710

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.41	2.54	2.67	0.095	0.100	0.105
A_1	0.127	-	0.300	0.005	-	0.012
A_2	2.29	2.41	2.54	0.090	0.095	0.100
b	0.33	0.46	0.51	0.013	0.018	0.020
c	0.203	0.280	0.381	0.008	0.011	0.015
D	see table above					
E	10.11	10.41	10.67	0.398	0.410	0.420
E_1	7.42	7.49	7.57	0.292	0.295	0.298
e	1.14	1.27	1.40	0.040	0.050	0.055
L	0.41	-	0.89	0.016	-	0.035
µ	0°	-	8°	0°	-	8°

A DIVISION OF CIRRUS LOGIC

CDB5394
CDB5396/7

Evaluation Board for CS5394 and CS5396/7

Features

- Demonstrates recommended layout and grounding arrangements
- CS8404A generates AES/EBU and/or IEC 958 compatible digital audio
- Buffered serial output interface
- Digital and analog patch areas
- On-board or externally supplied system timing

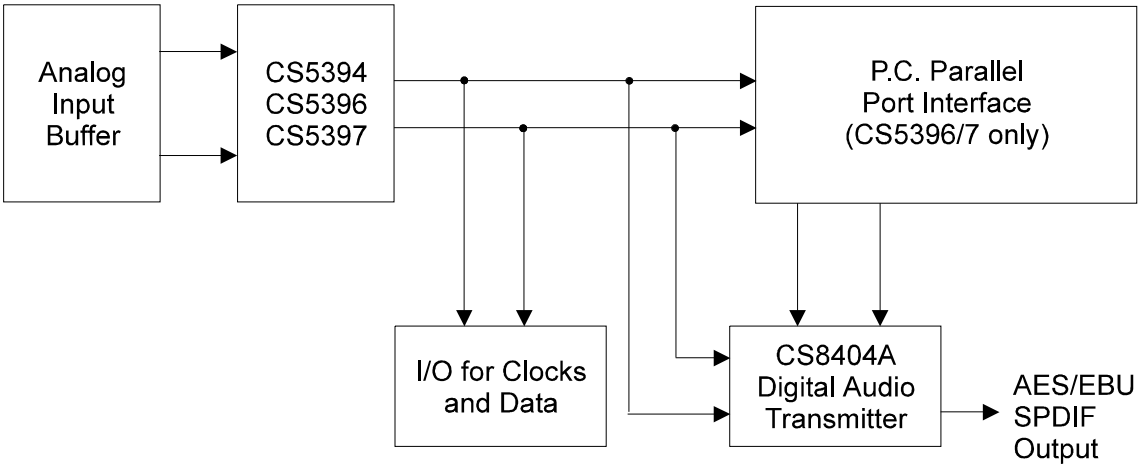
General Description

The CDB5394, CDB5396 and CDB5397 evaluation boards are an excellent means for quickly evaluating the CS5394, CS5396 and CS5397 24-bit, stereo A/D converters. Evaluation requires a digital signal processor, a low distortion analog signal source and a power supply. Analog inputs are provided via XLR connectors for both channels.

Also included is a CS8404A digital audio interface transmitter which generates AES/EBU, S/PDIF, and EIAJ-340 compatible audio data. The digital audio data is available via RCA phono and optical connectors.

The evaluation board may also be configured to accept external timing signals for operation in a user application during system development.

ORDERING INFORMATION:
CDB5394, CDB5396, CDB5397



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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OVERVIEW

CDB5394/96/97 System

The CDB5394/96/97 evaluation boards are an excellent means of quickly evaluating the CS5394, CS5396 or CS5397. The CS8404A digital audio interface transmitter provides an easy interface to digital audio signal processors, including the majority of digital audio test equipment. The evaluation board has been designed to accept an analog input and provide optical and coaxial digital outputs. The evaluation board also allows the user to access clocks and data through a 10-pin header for system development.

The CDB5394/96/97 schematic has been partitioned into 7 schematics shown in Figures 2 through 8. Each partitioned schematic is represented in the system diagram shown in Figure 1. Notice that the system diagram also includes the connections between the partitioned schematics.

Power Supply Circuitry and Grounding

Power is supplied to the evaluation board by six binding posts as shown in Figure 8. +5VA provides 5 Volt power to the converter, VCOM buffer and the crystal oscillator. The +/-12V binding posts provide power to the analog input buffer. +5VD supplies 5 Volt power to the digital section of the board. Z1-Z4 are transient suppression diodes which also provide protection from incorrectly connected power supply leads.

Configuration for Stand-Alone or Control Port Mode

Refer to Tables 2-4 for the jumper settings required to configure the evaluation board.

Power-Down and Calibration - Stand alone Mode

The CS5394 and CS5396/97 in Stand-Alone mode are placed into the power-down mode simply by depressing the PDN switch (S1). Power-down is released when the PDN switch is released. A calibration sequence should be manually initiated by depressing the CAL switch (S2) following power-down.

Power-Down and Calibration - Control Port Mode for CDB5396/97 Only

Power-down and calibration are available only through the control port. The calibration and power-down buttons on the evaluation board are ignored when configured in the Control Port mode.

Supplied Control Port Commands for CDB5396/97

The evaluation board includes a set of DOS files which allow communication through a PC parallel port to the evaluation board.

The supplied commands include:

cal64x.bat - Performs a calibration and initialization sequence and sets the CS5396/97 into the 64X oversampling mode.

cal128x.bat - Performs a calibration and initialization sequence and sets the CS5396/97 into the 128X oversampling mode.

rdi2c.exe <Map>- This routine returns the value located in the register pointed to by <map>. The <map> value is in hex and the value returned is in hex.

wri2c.exe <map> <data> - This routine writes the value of <data> into the register pointed to by <map>. Both values are in hex.

rst.exe - Sends a reset command to the device.

mode128x.bat - Sets the device into the 128X oversampling mode. The cal128x.bat command includes this sequence.

mode64x.bat - Sets the device into the 64X oversampling mode. The cal64x.bat command includes this sequence.

gnd.bat - Disconnects the analog modulators from the input pins and attaches the modulator inputs to the internal common mode voltage.

ungnd.bat - Disconnects the analog modulators from the internal common mode voltage and attaches the modulator inputs to the input pins.

General Comments on the Parallel Port

The evaluation board will be partially powered through the PC cable when the supplies to the evaluation board are off. This will affect the RC timing circuit which places the CS5396/97 into the Control Port mode. It is required that the evaluation board go through the power-up sequence without the cable to the PC connected.

Input Buffer

The differential input circuit shown in Figure 4 is well-suited for the CS5394/96/7 in professional applications. The circuit will accept a differential or single-ended signal of either polarity and provide a differential signal with the proper DC offset to the CS5394 or CS5396/97. The circuit also incorporates 6 dB of attenuation to scale down professional input levels to the input voltage range of the CS5394/96/97. A nominal input level of 13 Volts rms to the evaluation board will achieve a full scale digital output from the CS5394/96/97. The common mode rejection of the system is limited by the passive component matching of the input buffer circuit. The analog input connector is a standard female XLR with Pin 2 positive, Pin 3 return, and Pin 1 shield.

R1, R5, R16 and C65 form an RC network which provides anti-alias filtering and the optimum source impedance for the CS5394/96/97 right channel inputs. R2, R3, R15 and C66 duplicate this function for the left channel. Notice that this circuit also provides approximately 13.25 dB attenuation to lower the noise contributed from the analog input buffer.

The CS5394/96/97 are able to withstand input currents of 100 mA maximum, as stated in the CS5394 and CS5396/7 data sheets. The OPA627 op-amp is not able to deliver 100 mA, so input protection diodes are not required. However, protection diodes are recommended if there is a possibility that overrange signals could be applied at the ADC inputs which exceed 100 mA. Refer to the Crystal application note, "AN10: A/D Converter Input Protection Techniques."

CS5394 and CS5396/7 A/D Converters

The CS5394/96/97 A/D converters are shown in Figure 2. A description of these devices are included in the CS5394 and CS5396/7 datasheets.

CS8404A Digital Audio Interface

Figure 4 shows the circuitry for the CS8404A digital audio interface transmitter. The CS8404A can implement AES/EBU, S/PDIF, and EIAJ-340 interface standards. The Digital Interface Format for the transmitter must be set to match the format chosen for the CS5394 or CS5396/7 as defined in Tables 2-4. SW2 provides 8 DIP switches to select various modes and bits for the CS8404A; switch definitions and the default settings for SW2 are listed in Tables 5-6. Digital outputs are provided on an RCA connector via an isolation transformer and on an optical transmitter. For more detailed information on the CS8404A and the digital audio standards, see the CS8403A/CS8404A data sheet.

I/O Port for Clocks and Data

A serial output interface is provided on I/O Port_1, as shown in Figure 6. When I/O Port is set to the MASTER position, MCLK, SCLK, LRCK and SDATA are outputs from I/O Port. When I/O Port is in the SLAVE position, MCLK and SDATA are outputs, while SCLK and LRCK become inputs. Hence, in SLAVE mode, the SCLK and LRCK signals must be externally derived from MCLK to run the ADC. All signals are buffered in order to isolate the converter from external circuitry. Note that the

CS5394/96/97 must also be properly configured for Slave or Master mode.

CS8404A Format Configuration

The CS5394/96/97 supports two Digital Interface Formats for both master and slave configurations. Format 0 has valid data on the rising edge of SCLK and the CS8404A has no corresponding mode. However, inverting SCLK so that data is valid on the falling edge of SCLK will make Format 0 of the CS5394/96/97 match Format 1 of the CS8404A. Jumpers are available to configure the CS8404A to Format 1 and perform inversion of SCLK. See Tables 4-6.

Digital Interface Format 1 is the I2S compatible mode and matches Format 4 of the transmitter. Refer to Tables 4-6 for jumper positions.

CS8404A MCLK Generation

The crystal oscillator (U5) is either 256x for the 64x oversampling mode or 512x for the 128x oversampling mode. However, the CS8404A requires a master clock frequency of 128x Fs. Therefore, the MCLK must be divided by either 2 or 4 depending on the mode of operation. Refer to Tables 4-6 for the proper jumper selection.

Grounding and Power Supply Decoupling

The CS5394/96/97 require careful attention to power supply and grounding arrangements to optimize performance. The CS5394/96/97 is positioned over the analog ground plane.

This layout technique is used to minimize digital noise and to insure proper power supply matching/sequencing. The decoupling capacitors are located as close to the ADC as possible. Extensive use of ground plane fill on both the analog and digital sections of the evaluation board yield large reductions in radiated noise effects.

The evaluation board uses separate analog and digital ground planes which are joined at the converter. This arrangement isolates the analog circuitry from the digital logic.

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+5VA	input	+5 Volts for analog section
+5VD	input	+5 Volts for digital section
±12V	input	±12 Volts for analog input
AGND	input	Analog ground connection from power source
DGND	input	Digital ground connection from power source
AINL	input	Left channel differential/single ended analog input
AINR	input	Right channel differential/single ended analog input
LRCK, SCLK	input/output	I/O for serial and left/right clocks
MCLK	output	Master clock output
SDATA	output	Serial data output
coaxial output	output	CS8404A digital output via transformer
optical output	output	CS8404A digital output via optical transmitter

Table 1: System Connections

Jumper	Purpose	Position	Function Selected
HDR1	Sets the proper pull-up for the parallel port	**High** Low	Selects a 2k pull-up for I2C compliance Invalid selection for uC mode
HDR7	Sets the proper pull-up for the parallel port	**High** Low	Selects a 2k pull-up for I2C compliance Invalid selection for uC mode
HDR8	Sets the proper pull-up for the parallel port	**High** Low	Selects a 2k pull-up for I2C compliance Invalid selection for Control Port mode
HDR10	Selects Stand-Alone or Control Port mode	**High** Low	Selects Control Port Mode Invalid selection for Control Port Mode
HDR11	Selects I2C or SPI mode for CS5396/97 control port	**High** Low	Selects I2C mode Selects SPI Mode
SDATA	Selection of data source for output from the SPDIF and I/O port	**1** 2	Selects SDATA1 Selects SDATA2
I/O Port	I/O port Slave or Master selection	Slave **Master**	LRCK and SDATA are inputs to the port. LRCK and SDATA are outputs from the port
8404A Mode 1 Mode 2 Mode 3	Sets CS8404A data format selection for CS5396/97 compatibility. All jumpers must be set to either I2S or LJ and be compatible with the CS5396/97 data format.	**I2S** LJ	I2S data format selected Left Justified data format selected
CS8404A	MCLK divide for CS8404 and CS5396/97 compatibility	**128 x** 64 x	Divide MCLK by 4 for 128x oversampling mode Divide MCLK by 2 for 64x oversampling mode
CS5396/97	Supports a future function of the CS5396/97	High **Low**	Invalid selection Should be set LOW

Bold indicates default settings

Table 2: CDB5396 and CDB5397 Control Port Mode jumper Setting

Jumper	Purpose	Position	Function Selected
HDR1	Secondary effect on power-down implementation	High **Low**	Invalid selection for Stand-alone Mode Must be set low for operation
HDR7	CS5396/97 digital data format selection	**High** Low	Selects I2S data format Selects Left justified data format
HDR8	CS5396/97 Master or Slave mode selection	High **Low**	Selects Slave Mode Selects Master Mode
HDR10	Selects Stand-alone or Control Port mode	High **Low**	Selects Control Port Mode Selects Stand-alone Mode
HDR11	Selects polarity of power-down	**High** Low	Must be set High Invalid selection, CDB will not function
SDATA	Selection of Data source for output from the SPDIF and I/O port	**1** 2	Selects SDATA1 Selects SDATA2
I/O Port	I/O port Slave or Master selection	Slave **Master**	LRCK and SDATA are inputs to the port LRCK and SDATA are outputs from the port
8404A Mode 1 Mode 2 Mode 3	Sets CS8404A data format selection for CS5396/97 compatibility. All jumpers must be set to either I2S or LJ and be compatible with the CS5396/97 data format (HDR7)	**I2S** LJ	I2S data format selected Left Justified data format selected
CS8404A	MCLK divide for CS8404 and CS5396/97 compatibility	128 x **64 x**	Divide MCLK by 4 for 128x oversampling mode Divide MCLK by 2 for 64x oversampling mode
CS5396/97	Supports a future function of the CS5396/97	High **Low**	Invalid selection Should be set LOW

Table 3: CDB5396 and CDB5397 Stand-Alone Mode Jumper Settings

Jumper	Purpose	Position	Function Selected
HDR1	Secondary effect on power-down implementation	High **Low**	Invalid selection for Stand-alone Mode Must be set low for operation
HDR7	CS5394 digital data format selection	**High** Low	Selects I2S data format Selects Left justified data format
HDR8	CS5394 Master or Slave mode selection	High **Low**	Selects Slave Mode Selects Master Mode
HDR10	Selects Stand-alone or Control Port mode	High **Low**	Invalid selection for CS5394 Selects Stand-alone Mode
HDR11	Selects polarity of power-down	**High** Low	Must be set High Invalid selection, CDB will not function
SDATA	Selection of Data source for output from the SPDIF and I/O port	**1** 2	Selects SDATA1 Invalid selection for CS5394
I/O Port	I/O port Slave or Master selection	Slave **Master**	LRCK and SDATA are inputs to the port LRCK and SDATA are outputs from the port
8404A Mode 1 Mode 2 Mode 3	Sets CS8404A data format selection for CS5394 compatibility. All jumpers must be set to either I2S or LJ and be compatible with the CS5394 data format (HDR7)	**I2S** LJ	I2S data format selected Left Justified data format selected
CS8404A	MCLK divide for CS8404 and CS5394 compatibility	128 x **64 x**	Invalid selection for CS5394 Divide MCLK by 2 for 64x oversampling mode
CS5396/97	Supports a future function of the CS5396/97	High **Low**	Invalid selection Should be set LOW

Bold indicates default settings

Table 4: CDB5394 Jumper Settings

Switch#	0=Closed, 1=Open	Comment
6	$\overline{PRO=0}$	Consumer Mode (C0=0)
	FC1, FC0	C24,C25,C26,C27 - Sample Frequency
8, 5	0 0 *0 1 1 0 1 1	0000 - 44.1 kHz 0100 - 48 kHz 1100 - 32 kHz 0000 - 44.1 kHz, CD Mode
7	$\overline{C3}$	C3,C4,C5 - Emphasis (1 of 3 bits)
	*1 0	000 - None 100 - 50/15 µs
4	$\overline{C2}$	C2 - Copy/Copyright
	*1 0	0 - Copy Inhibited/Copyright Asserted 1 - Copy Permitted/Copyright Not Asserted
3	$\overline{C15}$	C15 - Generation Status
	*1 0	0 - Definition is based on category code 1 - See CS8402A Data Sheet, App. A
	$\overline{C8}$, $\overline{C9}$	C8-C14 - Category Code (2 of 7 bits)
1, 2	1 1 1 0 0 1 *0 0	0000000 - General 0100000 - PCM encoder/decoder 1000000 - Compact Disk - CD 1100000 - Digital Audio Tape - DAT

Table 5: CS8404A Switch Definitions - Consumer Mode

Switch#	0=Closed, 1=Open	Comment
6	$\overline{PRO=1}$	Professional Mode (C0=1)
8	CRE	Local Sample Address Counter & Reliability Flags
	0 1	Disabled Internally Generated
7, 4	$\overline{C6}$, $\overline{C7}$	C6,C7 - Sample Frequency
	1 1 1 0 0 1 0 0	00 - Not Indicated - Default to 48 kHz 01 - 48 kHz 10 - 44.1 kHz 11 - 32 kHz
5	$\overline{C1}$	C1 - Audio
	1 0	0 - Normal Audio 1 - Non-Audio
3	$\overline{C9}$	C8,C9,C10,C11 - Channel Mode (1 of 4 bits)
	1 0	0000 - Not indicated - Default to 2-channel 0100 - Stereophonic
1, 2	EM1, EM0	C2,C3,C4 - Emphasis (2 of 3 bits)
	1 1 1 0 0 1 0 0	000 - Not Indicated - Default to none 100 - No Emphasis 110 - 50/15 µs 111 - CCITT J.17

Table 6: CS8404A Switch Definitions - Professional Mode

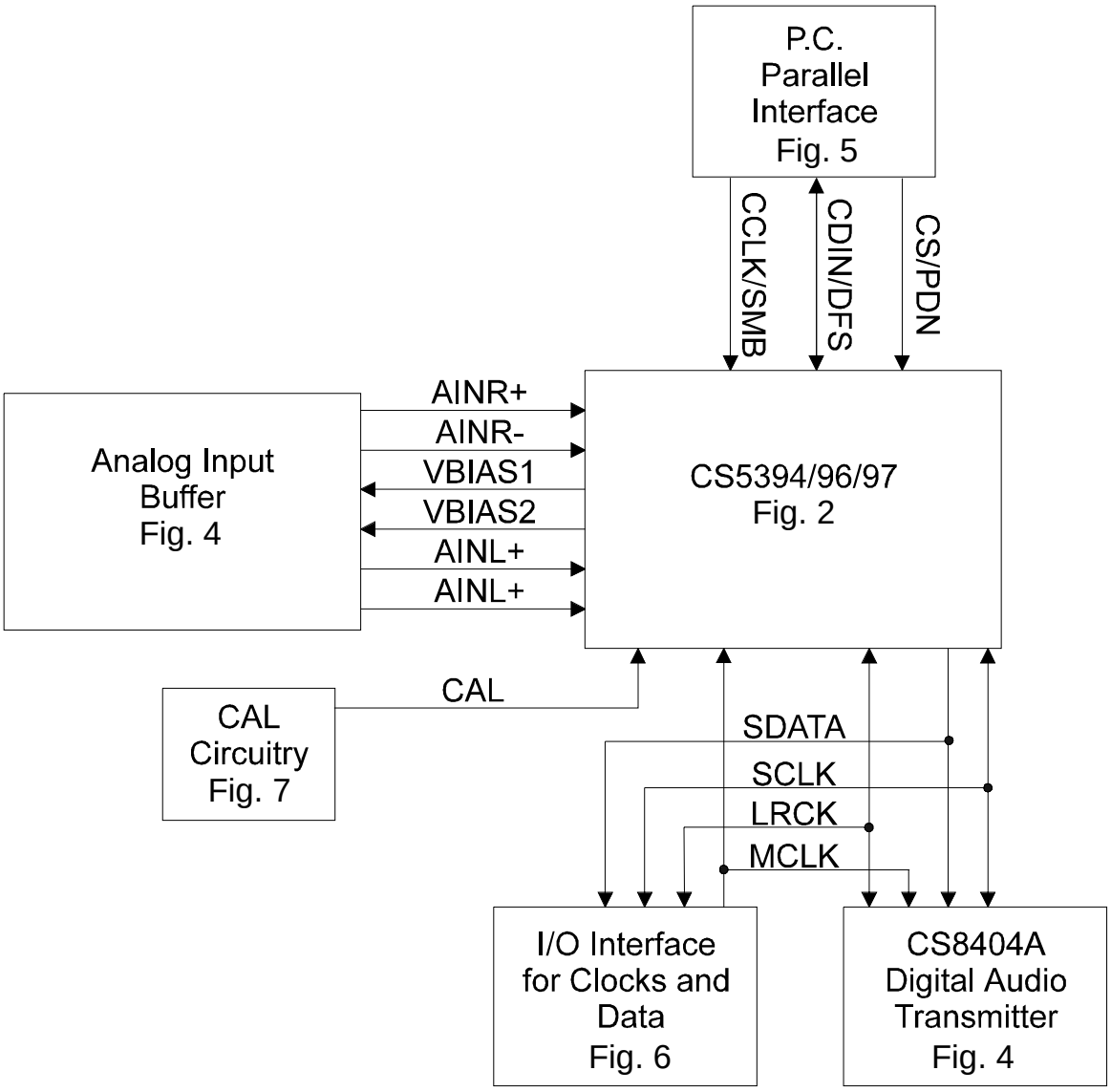


Figure 1. System Block Diagram and Signal Flow

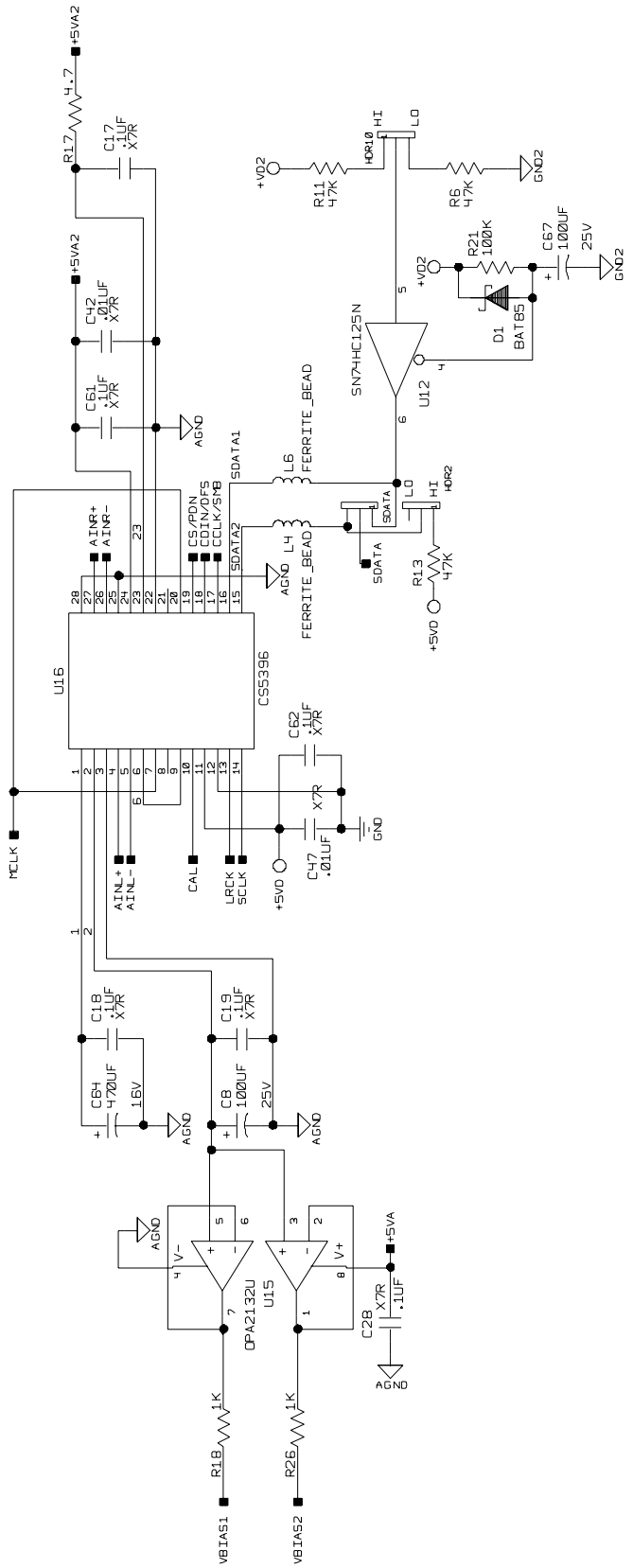


Figure 2. CS5394 and CS5396/7 Connections

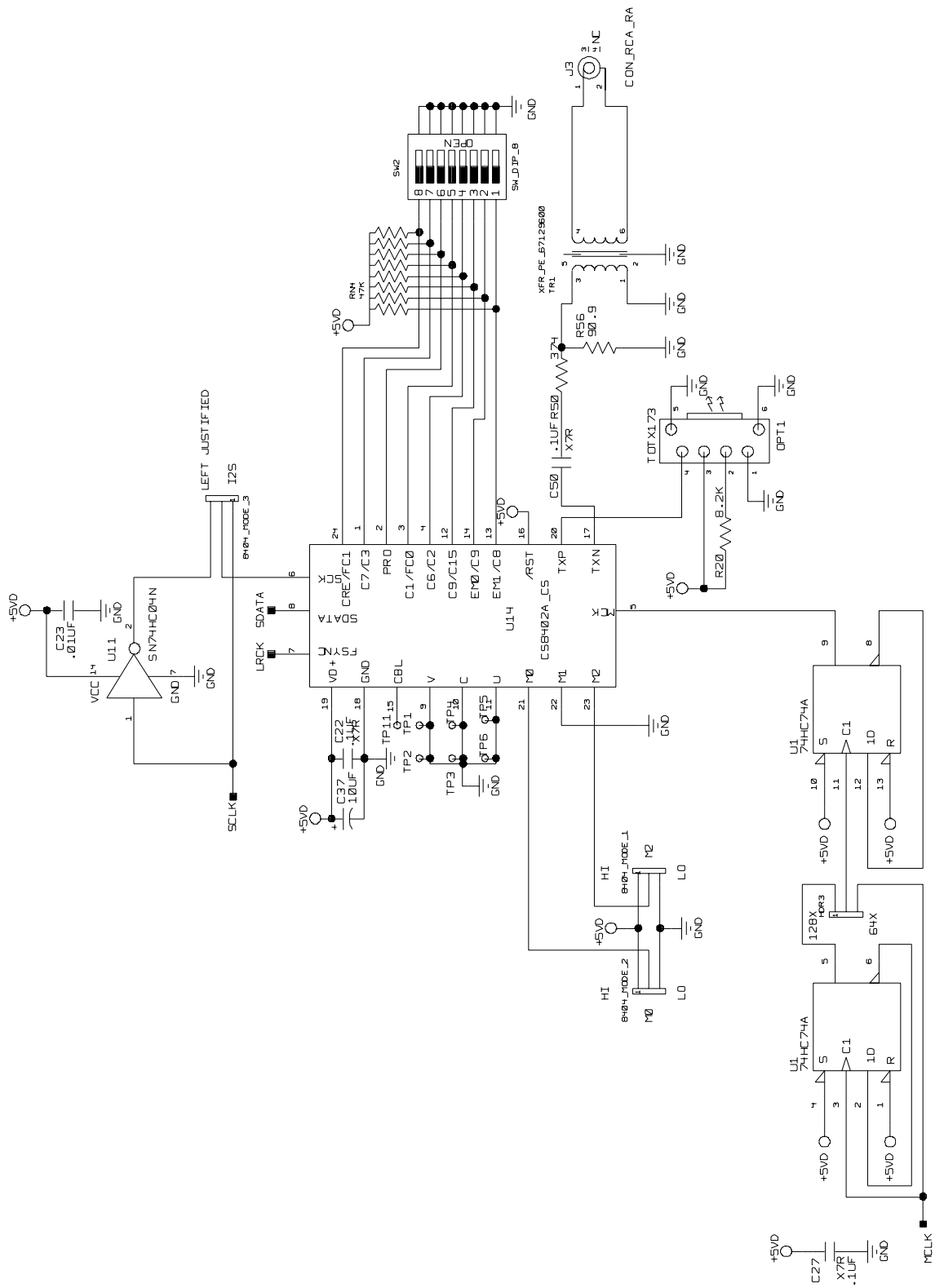


Figure 3. CS8404A Digital Audio Transmitter and Connections

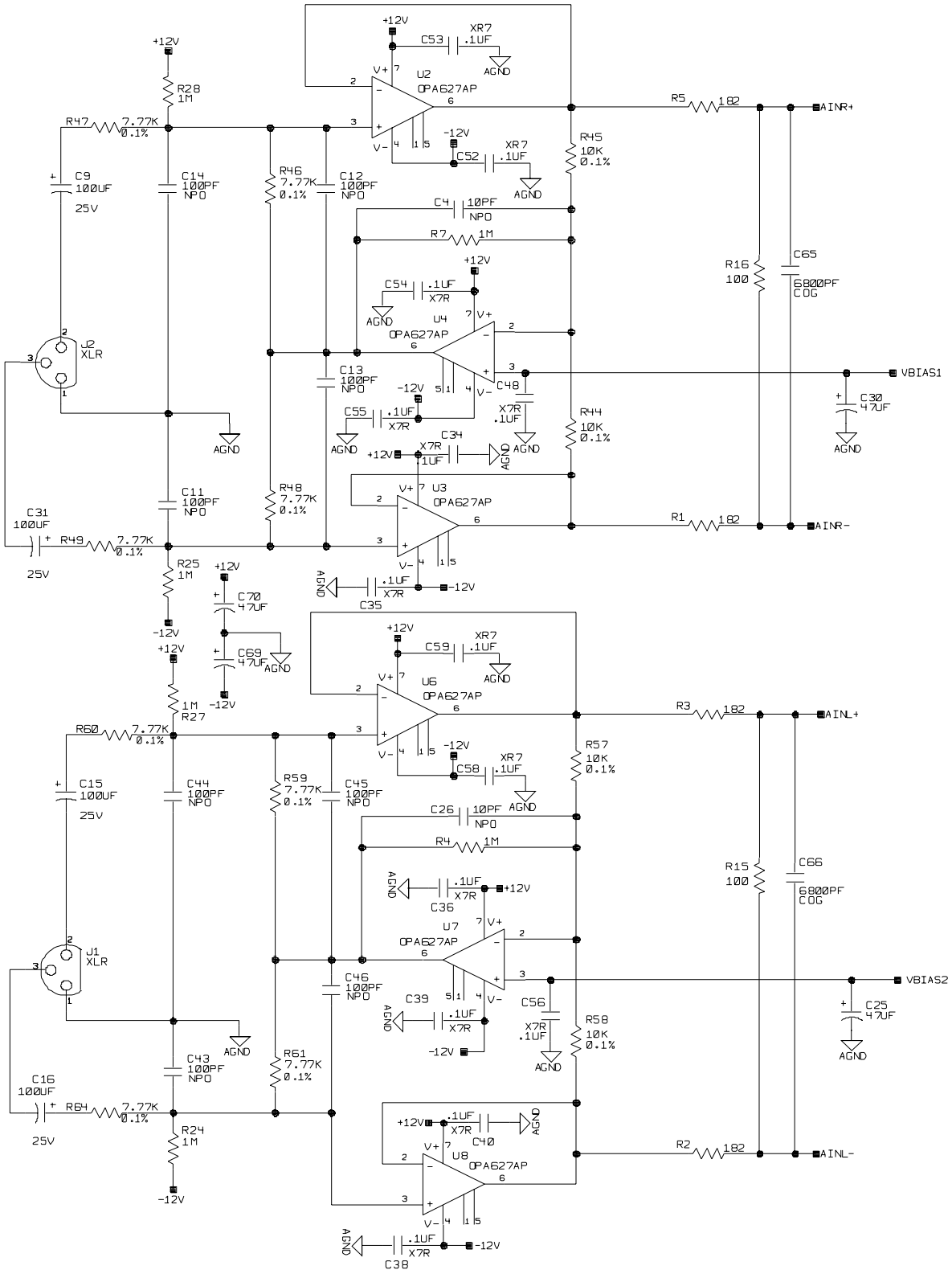


Figure 4. Analog Input Buffer

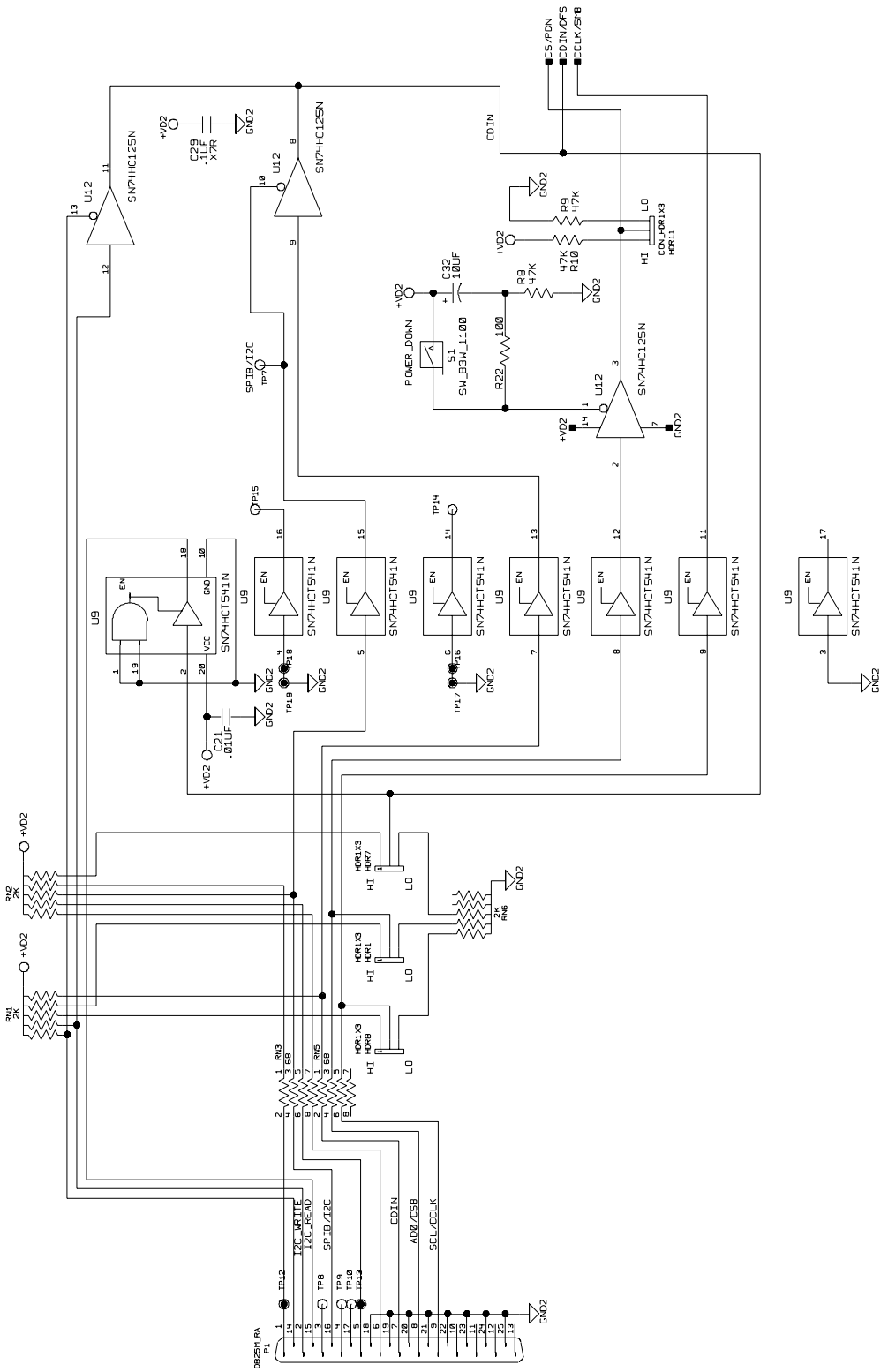


Figure 5. P.C. Parallel Interface

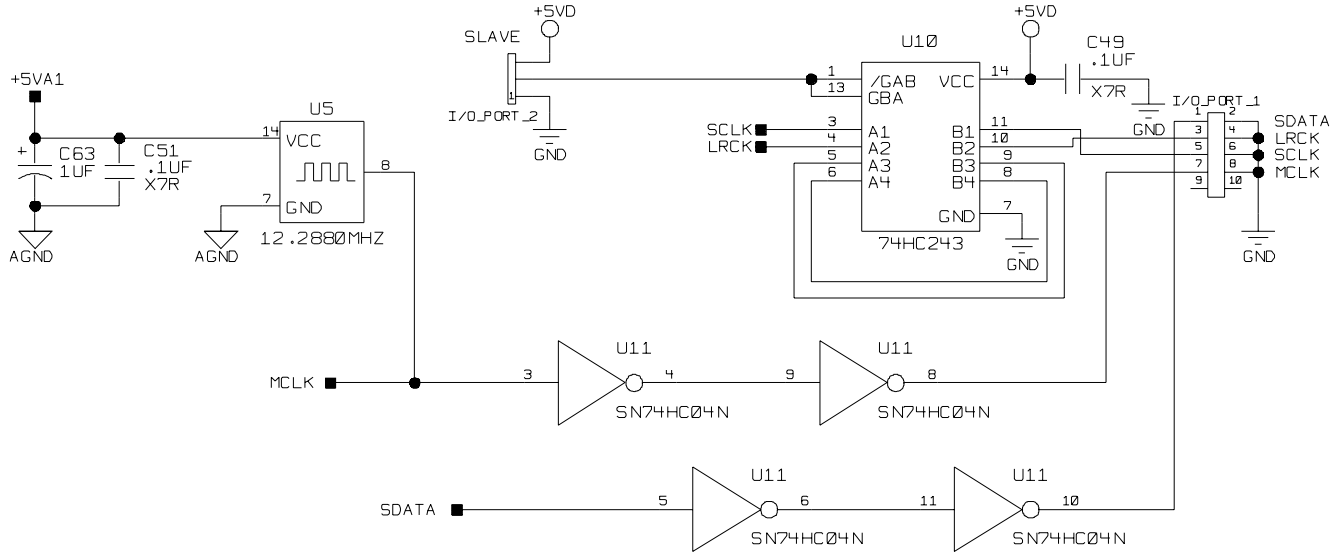


Figure 6. I/O Interface for Clocks & Data

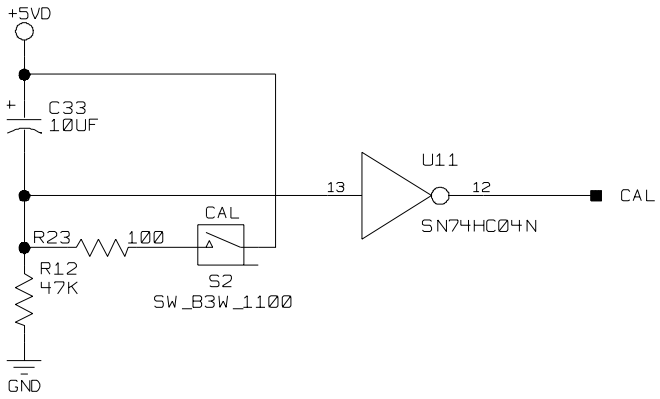


Figure 7. CAL Circuitry

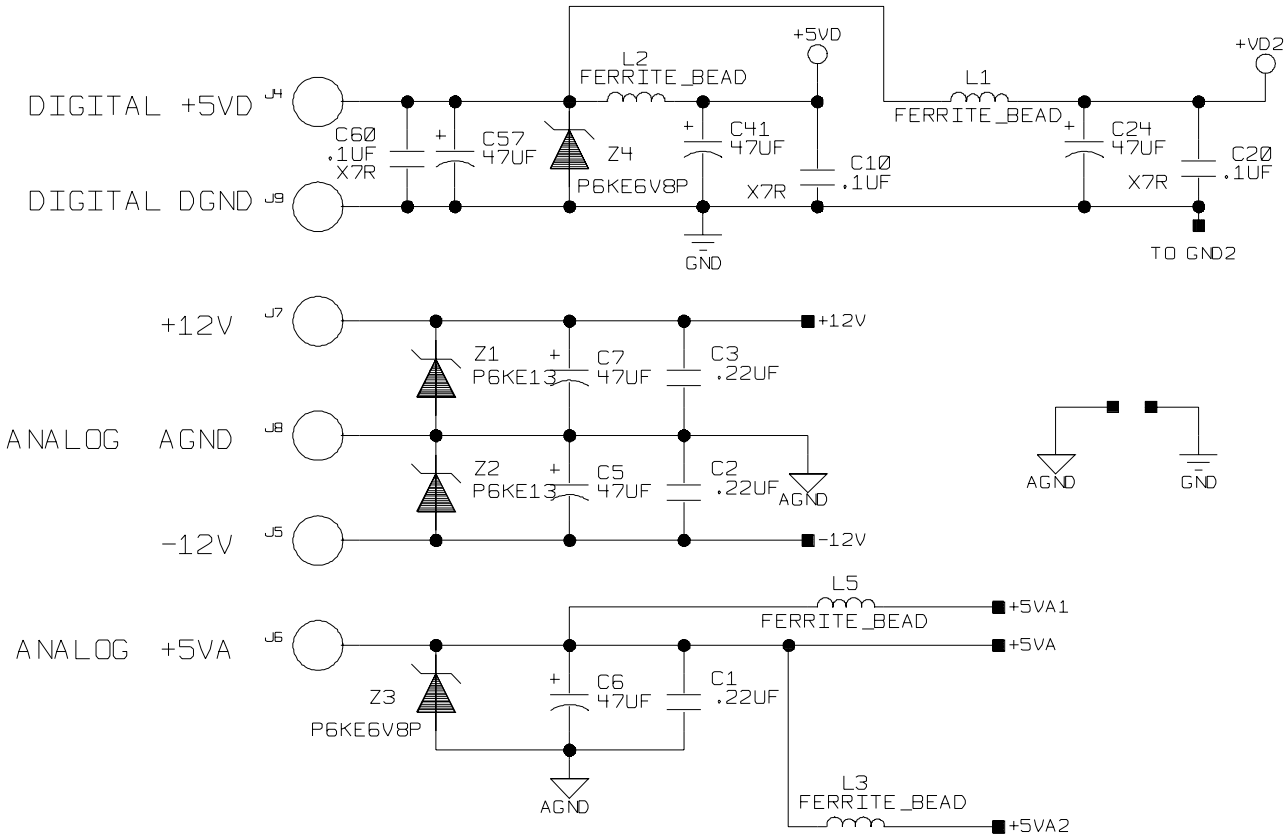


Figure 8. Power Supply & Reset Circuitry

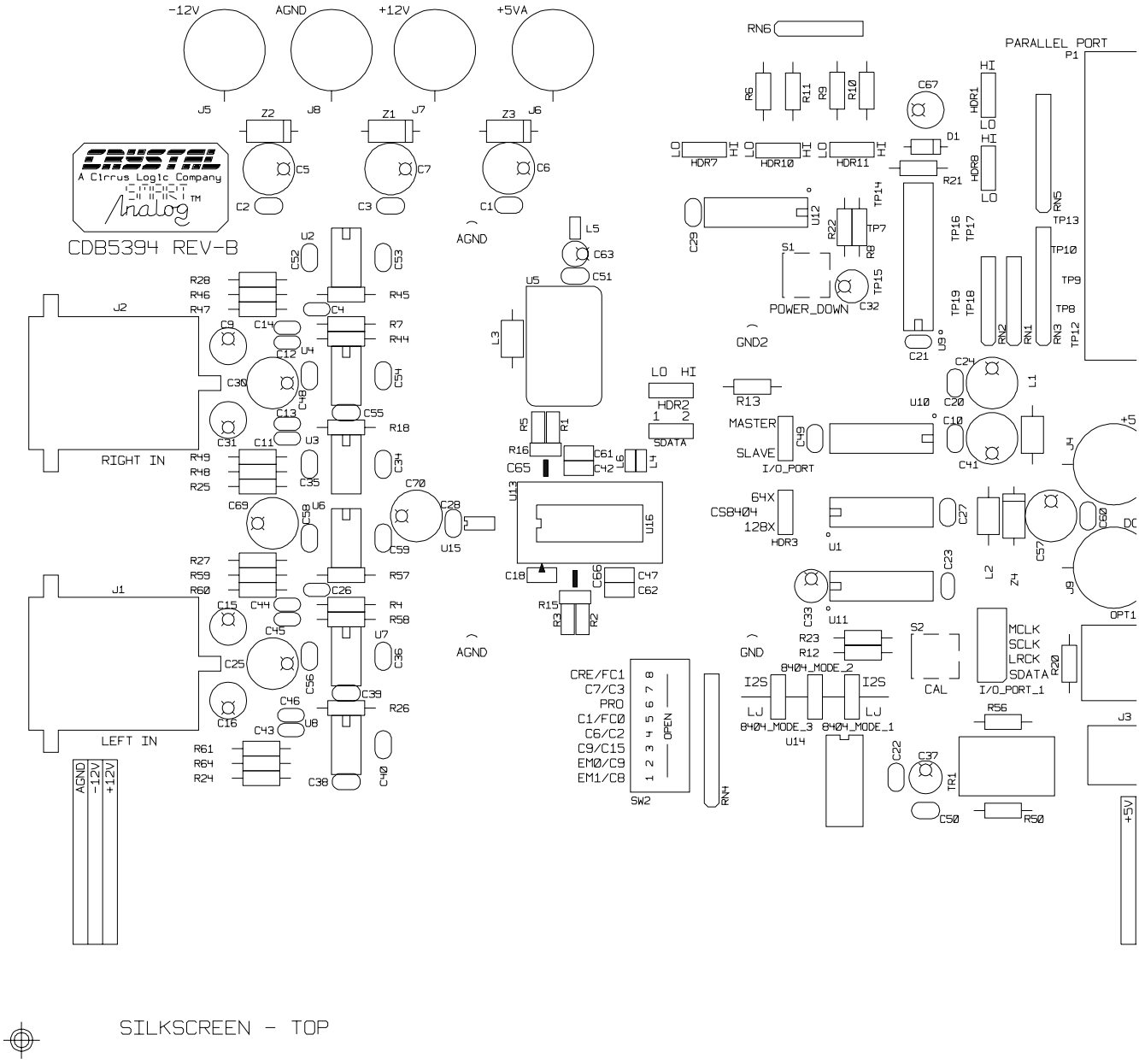
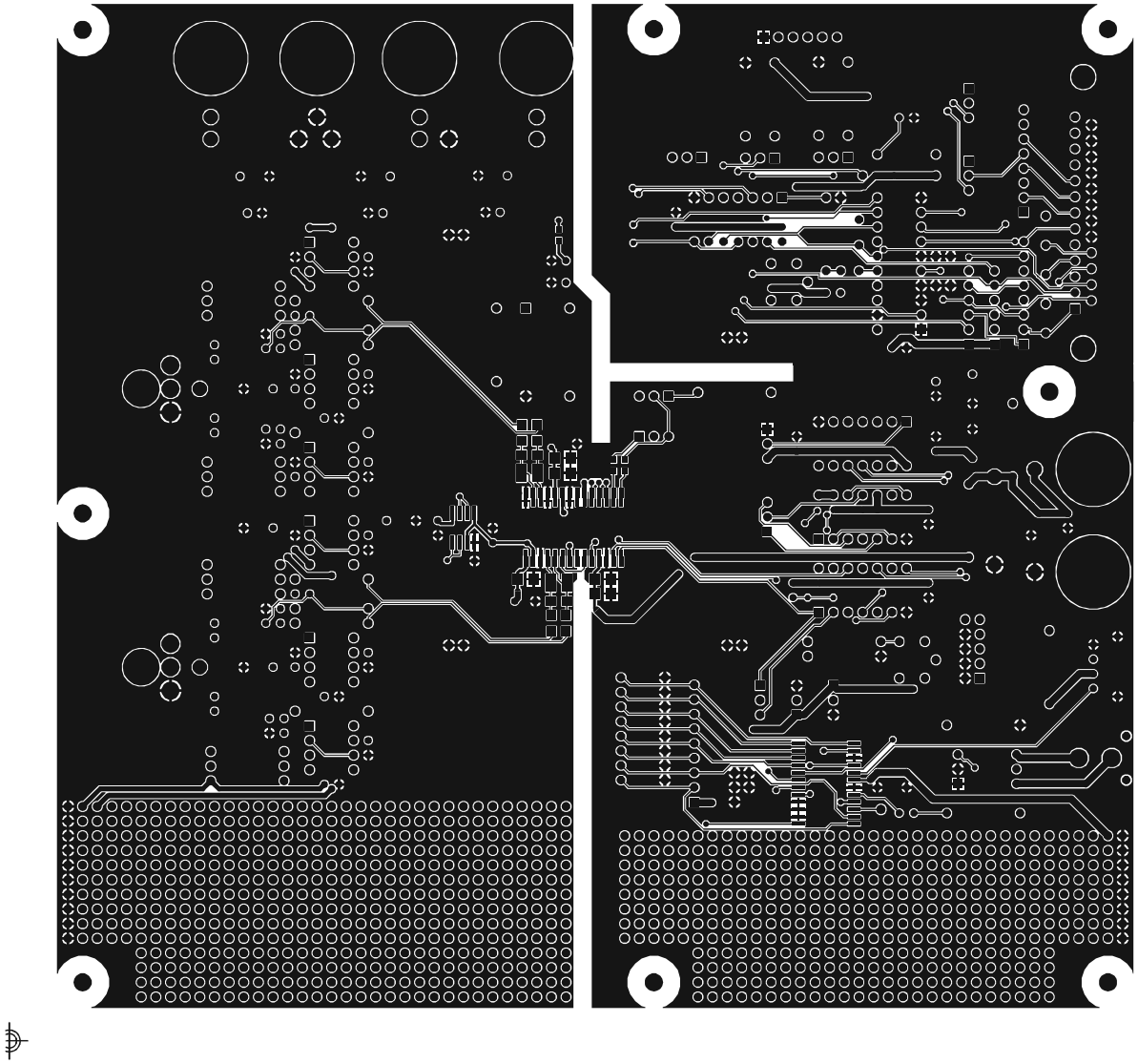


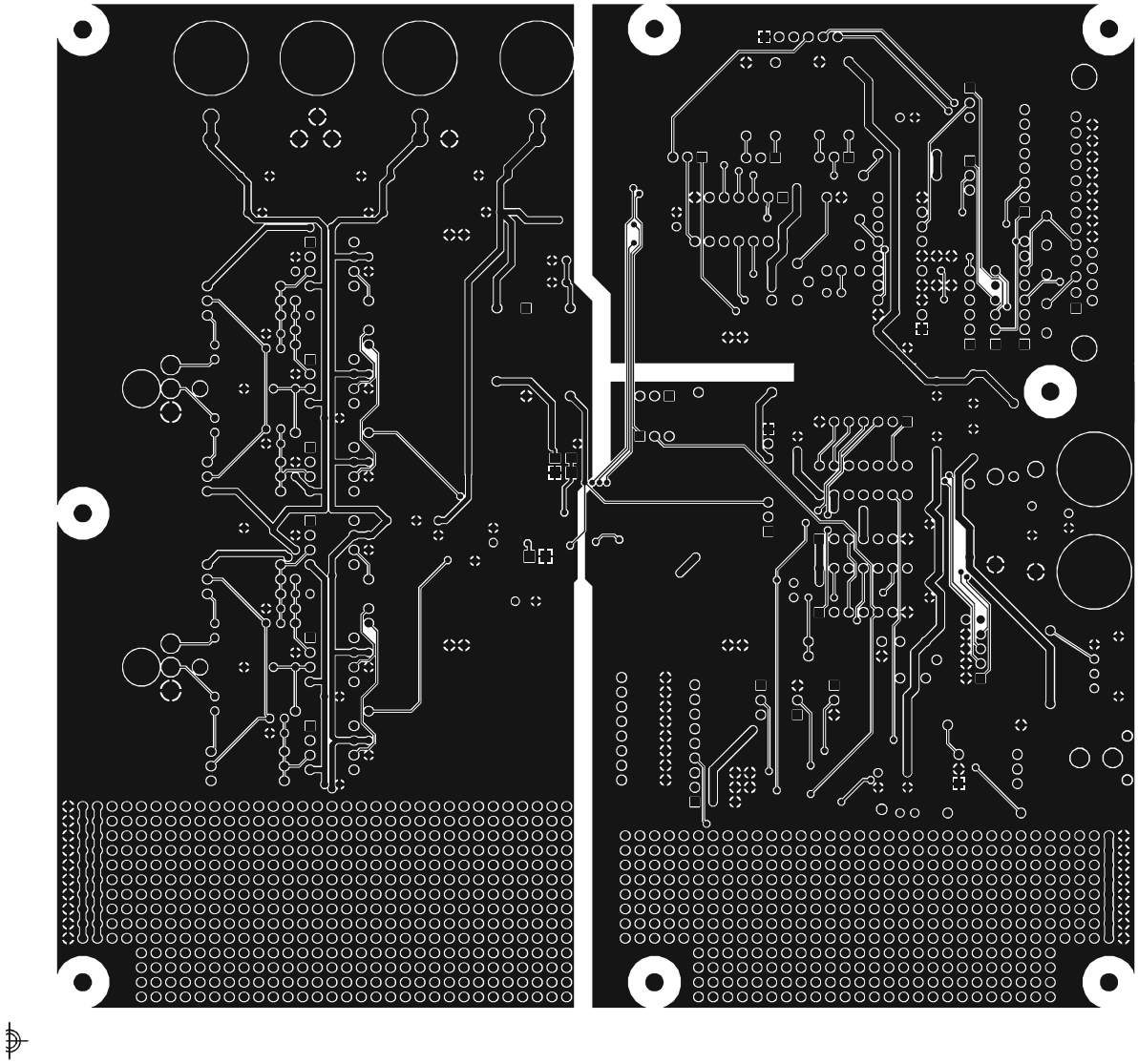
Figure 9. CDB5394 and CDB5396/7 Component Silkscreen Side (top)

Figure 10. CDB5394 and CDB5396/7 Component Silkscreen Side (bottom)



TOP SIDE

Figure 11. CDB5394 and CDB5396/7 Component Copper Side (top)



BOTTOM SIDE

Figure 12. CDB5394 and CDB5396/7 Component Copper Side (bottom)

• Notes •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