A NEW D-C TRANSISTOR DIFFERENTIAL AMPLIFIER

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The stable amplification of low-level signals of less than 1 millivolt magnitude has usually been done with a carrier-type feedback amplifier employing a complex modulation-demodulation system incorporating a short-lived and bulky mechanical chopper. The much simpler all-transistor d-c differential amplifier, however, has not been suitable due to drifts in gain and operating point during aging and temperature variations. This paper relates to improvements in both aging and temperature variations as a result of improved device characteristics obtained with the double-diffused planar silicon transistors having a passivated surface[1] and a compound transistor circuit. It shall be shown that this circuit offers very good incremental gain stability, with single-ended as well as differential output capabilities.

ESTABLISHMENT OF THE D-C OPERATING POINT

Okada[2] has shown for the conventional differential stage, Figure 1, that the output function is given by:

$$E_{2o} - E_{1o} = \frac{\left[\alpha_1 R_{L1} + \alpha_2 R_{L2}\right]\left[\left(E_{1i} - E_{2i}\right) + \left(V_{BE2} - V_{BE1}\right)\right]}{\Delta}$$

$$+ \frac{\left[\alpha_1 R_{L1} + \alpha_2 R_{L2}\right]\left[\left(R_{b2} I_{CO1} - R_{b2} I_{CO2}\right) + \frac{V_{EE}}{R_{ee}}\left(\frac{R_{b1}}{\beta_1} - \frac{R_{b2}}{\beta_2} + R_{E1} - R_{E2}\right)\right]}{\Delta}$$

$$+ \left[I_{CO1} R_{L1} - I_{CO2} R_{L2}\right] \qquad (1)$$

where $\Delta = R_{e1} + R_{e2} + \frac{R_{b1}}{\beta_1} + \frac{R_{b2}}{\beta_2} + \frac{R_{b1} R_{b2}}{\beta_1 \beta_2 R_E}$

and where it is assumed that α is constant, $R_L \ll r_c$, and the device extrinsic resistances are included in R_{e1}, R_{e2}, R_{b1}, and R_{b2}.

To obtain the initial balance, that is when $E_{2o} - E_{1o}$ and $E_{1i} - E_{2i}$ are both zero, the remainder of Equation (1) must sum to zero. The term relating to V_{EE} may be made small if R_{ee} is sufficiently large which is readily accomplished by employing the impedance gain of a transistor operated as a current source. Then, for ideally matched transistors with respect to V_{BE}, and I_{CO}, the conditions of balance are fulfilled. Since such selection of units is not feasible on a production basis, the common alternative is to vary the relative magnitudes of R_{e1} and R_{e2} at the expense of unequal emitter currents.

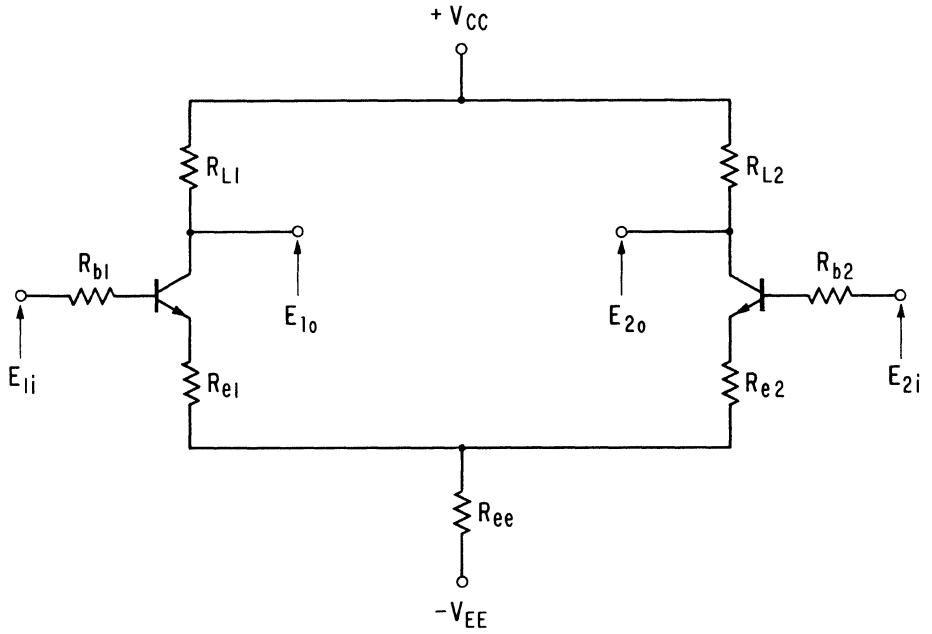


Fig. 1 The generalized transistor differential stage.

The first order factors responsible for drift of the operating point are well known; specifically, the thermal effects on the transistor's emitter-base voltage, current gain, and I_{CBO}. For the planar-passivated transistors mentioned previously, the magnitudes and distribution of I_{CBO} (as shown by Figure 2a) are such that their effects may be neglected to temperatures as high as 100°C to 125°C for source impedances of 10^3 ohms to 10^4 ohms. Variations of β however, are not so well ordered, thus placing an upper limit on R_{b1} and R_{b2}. This may be alleviated to a certain extent by maintaining a minimum collector current commensurate with the output loading. The most difficult obstacle to overcome is the matching of the emitter to base voltage (V_{BE}) characteristic and its temperature coefficient which are both functions of: emitter current, h_{FE}, the doping densities of the emitter and base at the junction, and the relative magnitudes of diffusion and space-charge region recombination-generation currents[3, 4]. It has been found, however, that the uniformity of characteristics inherent in the planar-diffused junction devices with passivated surfaces lends to selection methods for optimum temperature matching. A typical group distribution is shown in Figure 2b.

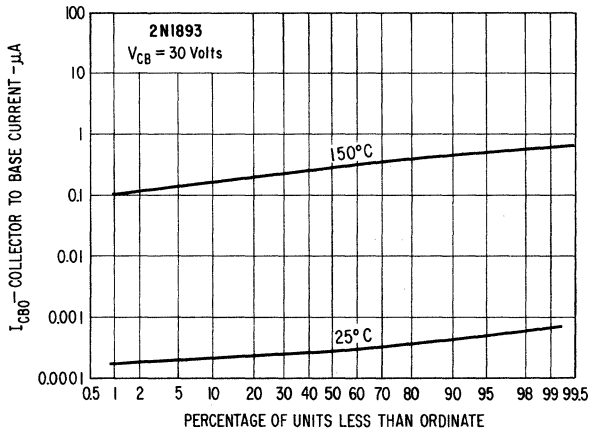


Fig. 2 (a) A typical distribution of I_{CBO} as a function of temperature, for the planar transistor.

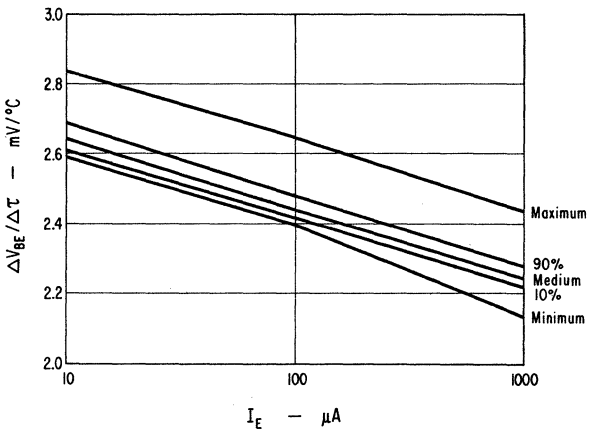


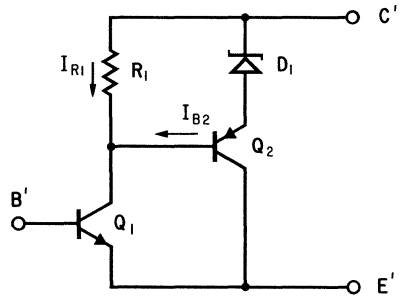
Fig. 2 (b) A typical distribution of Base-Emitter voltage temperature coefficient.

The PNP/NPN compound block circuit shown in Figure 3 takes maximum advantage of the improved characteristics of planar-diffused junction transistors and further reduces the effects of β variations. The complementary configuration is used to minimize the number of components and simplify biasing. D_1 is a breakdown diode having a positive temperature coefficient slightly greater in magnitude than that of the emitter-base voltage of Q_2. A temperature rise has the effect of increasing the current through R_1 while I_{b2} decreases. By proper selection of D_1 and R_1, I_{C1} may be maintained constant over the operating temperature range, which is a necessary condition for minimizing drift. If R_1 is chosen such that I_{C1} is less than I_{C2} by an order of magnitude, the input current is proportionately decreased. The current gain of the three-terminal transistor equivalent of this circuit, is given by:

$$h_{FE} = \beta_1 \left[1 + \beta_2 \left(\frac{I_{B2}}{I_{B2} + I_{R1}} \right) \right] \tag{2}$$

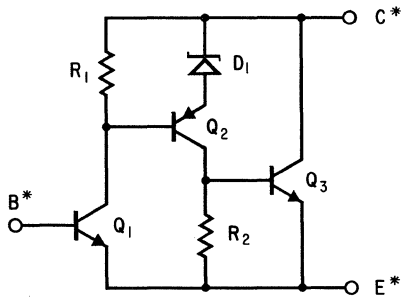
The reduced input current permits operation from higher source impedances than for the single transistor stage, while maintaining the desired constant operating bias condition.

An extension of the PNP/NPN compound block having higher gain is shown in Figure 4. I_{C1} is maintained constant in the same way, but may be reduced considerably since I_{B2} is now smaller. No attempt is made to maintain I_{C2} constant, as the differential changes in Q_2 operating point are of little consequence. While the latter circuit results in very small base currents, the limiting factor for the source impedance is again determined by I_{CBO} temperature considerations.



$$\beta' = \beta_1 \left[1 + \beta_2 \left(\frac{I_{b2}}{I_{b2} + I_{R1}} \right) \right]$$

Fig. 3 The PNP/NPN compound block.



$$\beta^* \simeq \beta_1 \beta_3 \left[1 + \beta_2 \left(\frac{I_{b2}}{I_{b2} + I_{R1}} \right) \right]$$

Fig. 4 An extension of the compound block, having higher gain.

Previously, only the electrical aspects of the amplifier have been considered. If in packaging an assembly where the input transistor pairs are thermally separated such that temperature differentials could readily exist, the following effects will be present. Since the V_{BE} temperature coefficients are from 2 mV/°C to 3 mV/°C in magnitude, than a ΔT of 0.01°C represents an apparent signal input of 20μV to 30 μV. To overcome this very serious obstacle, units have been fabricated using two selected devices in a single TO-5 package, which under worse conditions gives small gradients having short duration. A further consideration suggested by J. J. Sparkes concerns the device dissipation and thermal resistance. Low frequency signals create temperature variations at the collector junction and the resulting emitter-base temperature cycles being determined by the thermal resistance. This phenomenon is minimized by operating at low collector currents and voltages.

Specific examples of these amplifiers are the circuits shown in Figures 5 and 6 using the two-transistor and three-transistor blocks, respectively, which have been designed for optimum d-c performance. Matched input transistors provide equivalent input drifts in the range of 3 μV/°C to 5 μV/°C which have been attained over the range of -70°C to +125°C. Eight hour stability for the two-transistor block is approximately $\pm$ 12 μV with a 330 ohm source impedance and $\pm$ 16 μV for a 2500 ohm input and the three transistor block drifts are about one-half of these. The circuit is insensitive to power supply variations. No selection is required with respect to V_{BE} of the PNP units. Operation is improved, however, if the current gains are somewhat matched.

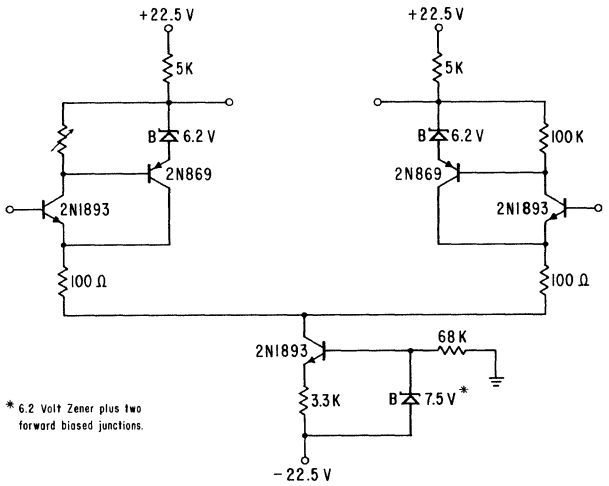


Fig. 5 The improved differential amplifier using the two-transistor block.

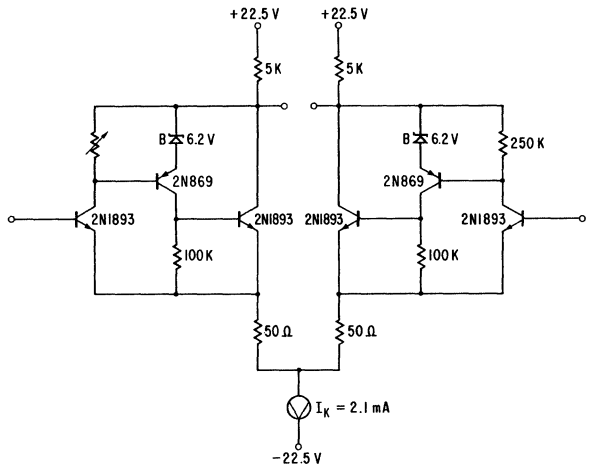


Fig. 6 The improved differential amplifier using the three-transistor block.

THE AMPLIFIER SMALL-SIGNAL CHARACTERISTICS

In addition to d-c stability criteria for the amplifiers discussed, the designer must consider the incremental or small-signal behavior. The purpose is to make the circuit voltage gain insensitive to device parameter variation. The amplifier performance is analyzed here on the basis of the single-ended equivalent stage. Employing the conventional h-parameter notation, the voltage gain is given by:

$$A_v = \frac{R_L}{\left(\frac{h_i}{h_f} + R_e\right) + R_L\left(\frac{\Delta h}{h_f} + h_o R_e\right)} \quad \text{(common emitter h-parameters)} \tag{3}$$

Since for an ideal transistor the voltage gain is determined by the ratio R_L/R_e, an inspection of the denominator of Equation (3) indicates that R_e should be large to satisfy $R_e \gg h_i/h_f$, but R_e should be small such that $R_L R_e h_o \ll R_e$. It is shown (Appendix 1) that an optimum R_e may be chosen to most closely approximate the limit case voltage gain and minimize the effects of transistor parameters as well. This optimum R_e is given by:

$$R_e \text{ (opt.)} = \left(\frac{h_i}{h_o h_f g}\right)^{1/2} \tag{4}$$

The input resistance is also of interest since this determines the loading placed upon the source. This is related by:

$$R_{in} = \frac{h_i + h_f R_e + \Delta^h R_L}{1 + h_o R_L} \tag{5}$$

To facilitate predicting the performance of the two- and three-transistor blocks, advantage is taken of their three terminal equivalence to obtain the h' parameters and h* parameters of the two- and three-transistor compounds respectively (See Appendix II). Using Equations (3) and (5), the curves of Figures 7 and 8 were calculated. The effect of feedback in the two-and three-transistor stages is immediately evident in both optimum gain and input resistance performance.

The resistance values of Figures 5 and 6 were selected for optimum gain performance for the devices selected. Measured characteristics were in excellent agreement with predicted values for both amplifiers.

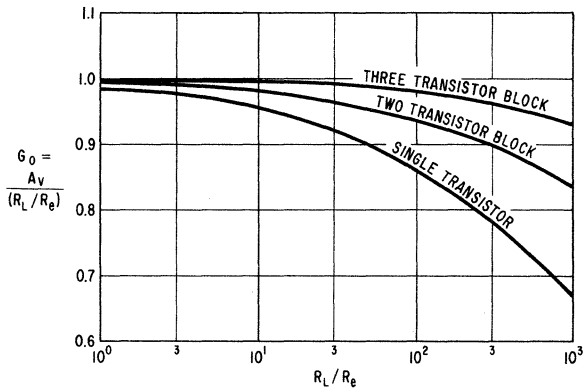


Fig. 7 The ratio of actual voltage gain to limit case, R_L/R_e, as a function of R_L/R_e with R_e optimized.

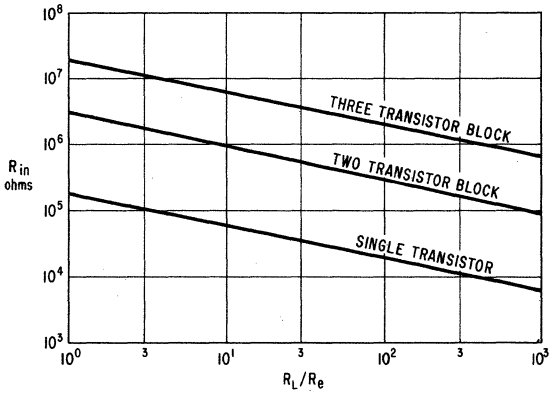


Fig. 8 Input resistance as a function of R_L/R_e with R_e optimized.

TRANSISTOR CHARACTERISTICS FOR AN OPTIMIZED D-C AMPLIFIER

From Equation (1), it is immediately apparent that I_{CO} must be small, the base-emitter voltages must be well matched (essential to realize equal input-transistor collector currents), and the transistors must have similar current gains. One necessary condition in realizing these requirements is that surface effects be kept small. The passivated surface units achieve this quite well. The planar diffused junction transistor has an excellent uniformity with respect to emitter and base sensitive characteristics making feasible a production type matching selection.

In addition, the device must have a minimal Early effect. This is best realized by a very highly doped base and lightly doped collector ideally with an abrupt junction such that collector-base space charge variations occur primarily in the collector. As a further consequence of this, high β units are not desirable since they are typically accompanied by narrow base widths and increased Early effect sensitivity.

CONCLUSION

The amplifier described compares favorably with many commercially available chopper types with respect to temperature drift and gain stability. The circuit is extremely simple and easily packaged as shown by Figure 9.

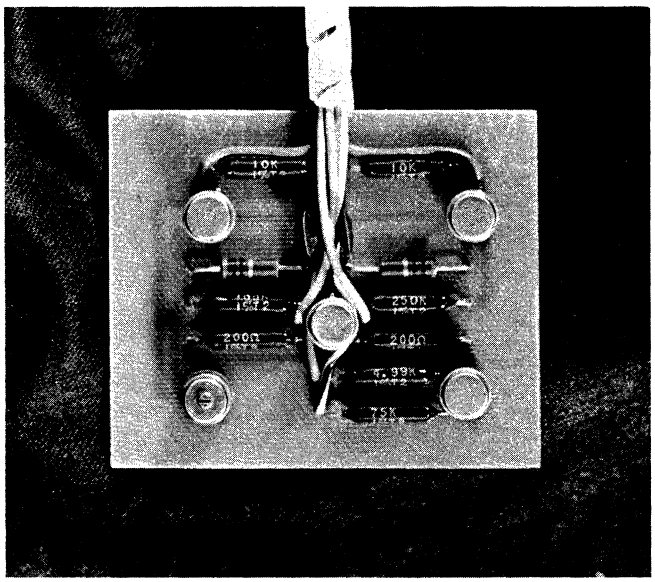


Fig. 9 Printed circuit board version of amplifier shown in figure 5.

While optimum gain behavior has been stressed, it is possible to effect compromises such as increased input impedance with an increased transistor dependence. The maximum bandwidth is of the order of 10^4 cps to 10^5 cps, but by rolling off at lower frequencies, equivalent input noise may be reduced considerably.

The writer gratefully acknowledges the many helpful discussions with Drs. V. H. Grinich and C. T. Sah and the patience and care of Messrs. R. Robson and E. Oliver in fabricating the devices and circuits used.

APPENDIX I

For the common-emitter stage with emitter series resistance, and $R_e h_o \ll 1$, the voltage gain is given by:

$$A_v = \frac{R_L}{\left(\frac{h_i}{h_f} + R_e\right) + R_L\left(\frac{\Delta h}{h_f} + h_o R_e\right)} \tag{A1}$$

Defining the ratio, $R_L/R_e = g$, Equation (A1) becomes:

$$A_v = \frac{gR_e}{R_e^2 g h_o + R_e\left(g\frac{\Delta h}{hf} + 1\right) + \frac{h_i}{h_f}} \tag{A2}$$

Equation (A2) will attain a maximum for a certain R_e determined by:

$$\frac{d(A_v)}{dR_e} = \frac{\left[R_e^2 g h_o + R_e\left(g\frac{\Delta h}{h_f} + 1\right) + \frac{h_i}{h_f}\right]g - gR_e\left(2R_e g h_o + g\frac{\Delta h}{hf} + 1\right)}{\left[R_e^2 g h_o + R_e\left(g\frac{\Delta h}{h_f} + 1\right) + \frac{h_i}{h_f}\right]^2} = 0 \tag{A3}$$

Solving Equation (A3) for R_e,

$$R_e = \left(\frac{h_i}{h_o h_f g}\right)^{1/2} \tag{A4}$$

(for the optimum R_e)

APPENDIX II

The three terminal n-transistor block may be characterized by an equivalent set of h' parameters. Consider the circuit of Figure 3, having the block diagram shown in Figure 10a. To simplify the diagram, R_1 and the dynamic impedance of D_1 are included in the h parameters of Q_2 such that

$$h'_{i2} = \frac{R_1\left(h_{i2} + h_{f2}R_{D1}\right)}{R_1 + h_{i2} + h_{f2}R_{D1}} \tag{A5}$$

$$\text{and } h'_{f2} = h_{f2}\left(\frac{R_1}{R_1 + h'_{i2}}\right) \tag{A6}$$

The signal flow graph corresponding to Figure 10a is shown in Figure 10b. From the flow graph, the following relationships are obtained by inspection:

$$h'_i = \frac{h_{i1}\left(1 + h_{o1}h'_{i2}\right) - h_{f1}h_{r1}h'_{i2}}{1 + h_{o1}h'_{i2}}$$

$$h'_f = \frac{-h_{f1}h'_{f2}}{1 + h_{o1}h'_{i2}}$$

$$h'_r = \frac{h_{r1}h_{r2}}{1 + h_{o1}h'_{i2}}$$

$$h'_o = \frac{h_{o2}\left(1 + h_{o1}h'_{i2}\right) - h'_{f2}h_{r2}h_{o1}}{1 + h_{o1}h'_{i2}}$$

Since from the d-c operating bias conditions $I_{C1} \approx 0.1 \cdot I_{C2}$, then it follows that $h_{o1} < h_{o2}$, and as a consequence $h_{o1}h'_{i2} \ll 1$. Further, since $h_{i1} > h_{i2}$, $h_{f1}h_{r1} \ll 1$, and $h_{f2}h_{r2} \ll 1$, then the h' notations may be simplified to:

$$h'_i = h_{i1} \tag{A7}$$

$$h'_f = -h_{f1}h'_{f2} \tag{A8}$$

$$h'_r = h_{r1}h_{r2} \tag{A9}$$

$$h'_o = h_{o2} \tag{A10}$$

It must be noted that all h_{jk} parameters used are for the common-emitter configuration.

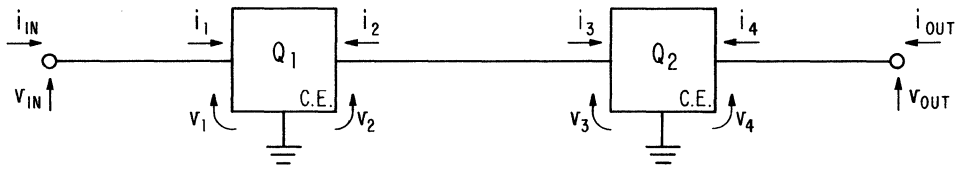


Fig. 10 (a) The block diagram of the two-transistor circuit of figure 3.

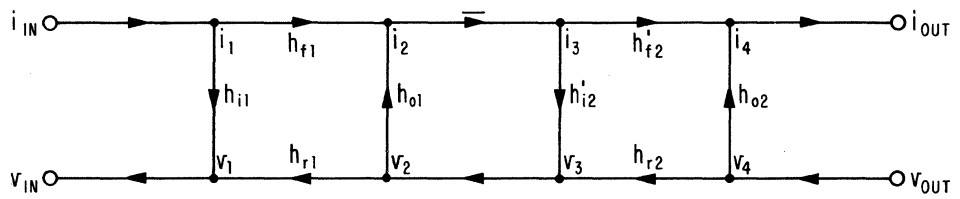


Fig. 10 (b) The associated signal-flow-graph.

The circuit of Figure 4 is analyzed in a similar manner, (See Figure 11). The complete expressions for the h* parameters are found to be:

$$h^*_i = \frac{h_{i1}(D) - h^*_{i2}\left[h_{f1}h_{r1}\left(1 + h_{o2}h^*_{i3}\right)\right] - h^*_{i3}\left[h_{f1}h_{r1}\left(1 + h^*_{f2}\right)\left(1 - h_{r2}\right)\right]}{D}$$

$$h^*_f = \frac{-h_{f1}\left[h^*_{f2}\left(1 + h^*_{f3}\right) - h_{o2}h^*_{i3}\right]}{D}$$

$$h^*_r = \frac{h_{r1}\left[h_{r2}\left(1 - h_{r3}\right) + h_{o2}h^*_{i3}\right]}{D}$$

$$h^*_o = \frac{h_{o3}(D) + h_{o2}\left[\left(1+h^*_{f3}\right)\left(1-h_{r3}\right)\right] - h_{o1}\left[h^*_{f2}h_{r2}\left(1+h^*_{f3}\right)\left(1-h_{r3}\right) + h^*_{f3}h_{r3}\left(1+h^*_{f2}\right)\left(1-h_{r2}\right)\right]}{D}$$

where $D = 1 + h_{o1}\left[h^*_{i2}\left(1 + h_{o2}h^*_{i3}\right) + h_{i3}\left(1 + h^*_{f2}\right)\left(1 - h_{r2}\right)\right] + h_{o2}h_{i3}$

and h^*_{i2} and h^*_{f2} are determined by the relationships given in Equations (A5) and (A6) respectively. Further, h^*_{i3} and h^*_{f3} are modified to include R_2. Using similar assumptions concerning relative magnitudes as for the two-transistor case, the h* parameters may then be reduced to:

$$h^*_i = h_{i1} \tag{A11}$$

$$h^*_f = -h_{f1}\left[h^*_{f2}\left(1 + h^*_{f3}\right)\right] \tag{A12}$$

$$h^*_r = h_{r1} \tag{A13}$$

$$h^*_o = h_{o3} \tag{A14}$$

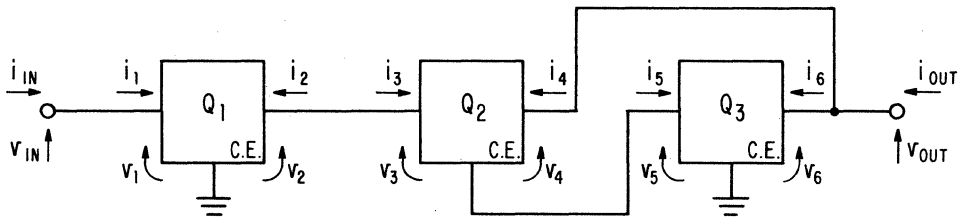


Fig. 11 (a) The block diagram of the three-transistor circuit.

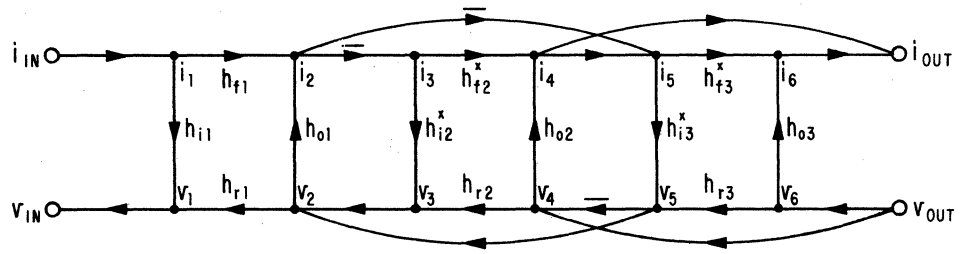


Fig. 11 (b) The signal-flow-graph.

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