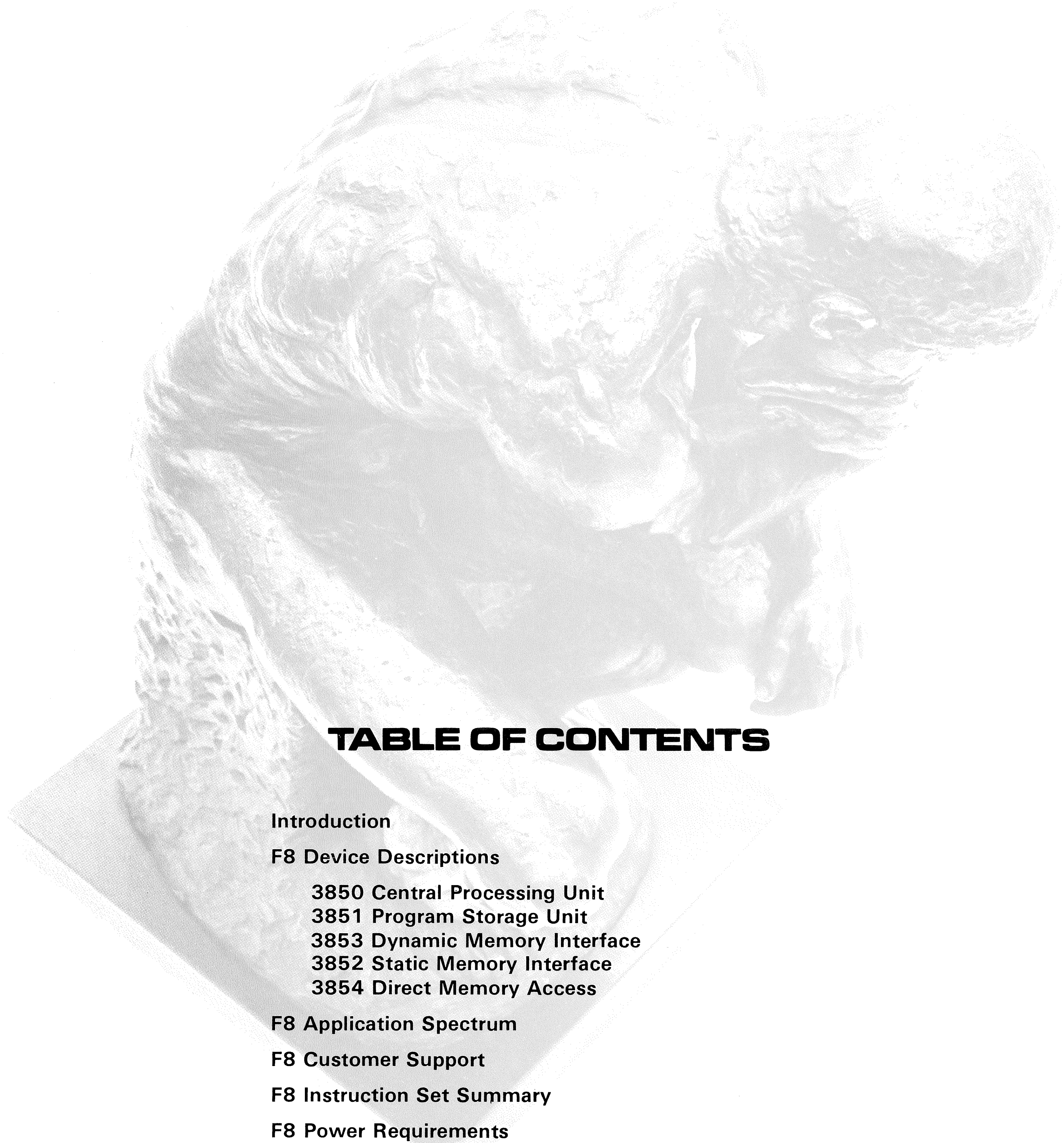
FAIRCHILD SEMICONDUCTOR

F8 MICROPROCESSOR



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THINK F8 UNIVERSAL STANDARD MICROPROCESSOR

VERSATILE . . EFFICIENT . . COST EFFECTIVE

The ultimate goal, from F8 design concept through development and production, was to produce the most versatile, efficient, cost-effective microprocessor system available today. To accomplish this, five stringent parameters, based on user experience with other systems, were set forth as guidelines for the F8.

- Minimum Parts Count
- Cost Effectiveness
- Simple Peripheral Interfaces
- Easy Expansion through Modular Architecture
- Simplified Programming and Debugging

HOW WERE F8 GOALS MET ?

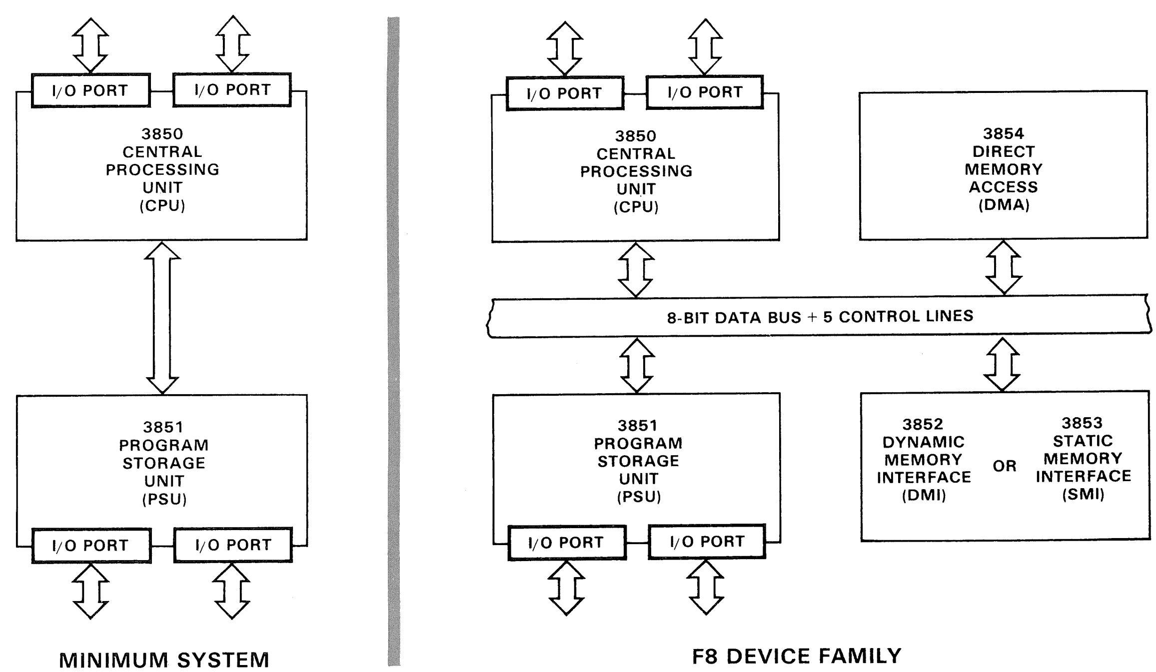
By . . . *unique system partitioning* the system functions have been divided among the various circuits of the F8 family to provide sophisticated modularity. As a result, it is now possible to build a minimum microprocessor system with only two devices. To this system PSU, RAM and I/O devices can be added to form medium size or memory intensive systems with a minimum use of external parts. And, finally, for solving complex problems, the F8 devices can be connected as subsystems into a synergistic system of independent microprocessors.

By . . . *incorporating the I/O structure on the chips* so that the majority (95%) of the peripheral devices can be directly controlled without the need for special circuits. The trick is to accommodate the characteristics of a given peripheral device in the software. The I/O hardware structure includes a programmable timer, an efficient interrupt system and bidirectional I/O ports.

By . . . providing *carefully thought out software* for generating and debugging microprograms and a choice of three hardware modules for speeding up prototype development.

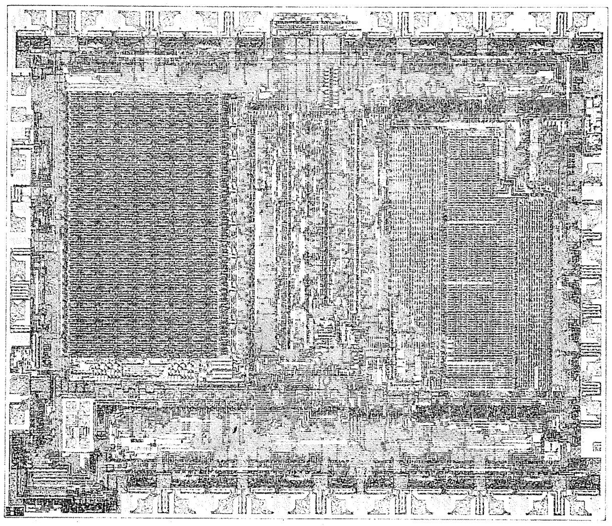
WHAT IS THE RESULT ?

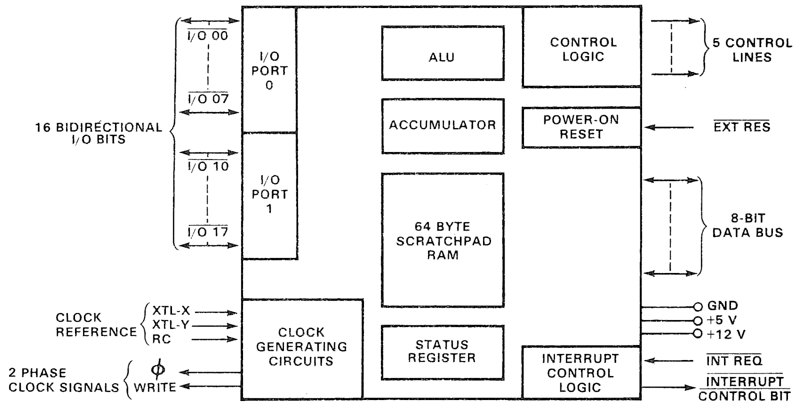
. . . *a complete family of LSI circuits* that can be used as building blocks to construct versatile, efficient, cost effective systems from the most simple to the highly complex.



3850 CENTRAL PROCESSING UNIT

Fairchild's F8 Central Processing Unit (CPU) contains all of the functions of an ordinary central processor and adds some time and money saving features uniquely its own. For instance, the 64 bytes of scratchpad RAM memory already included on the F8 CPU eliminate the need for external RAM circuits in many applications. Clock and power-on-reset circuitry, normally requiring additional integrated circuit packages, are included on-chip. Fairchild's CPU also contains 16 bits of fully bidirectional input and output lines internally latched (for storing output data) and capable of driving a standard TTL load.



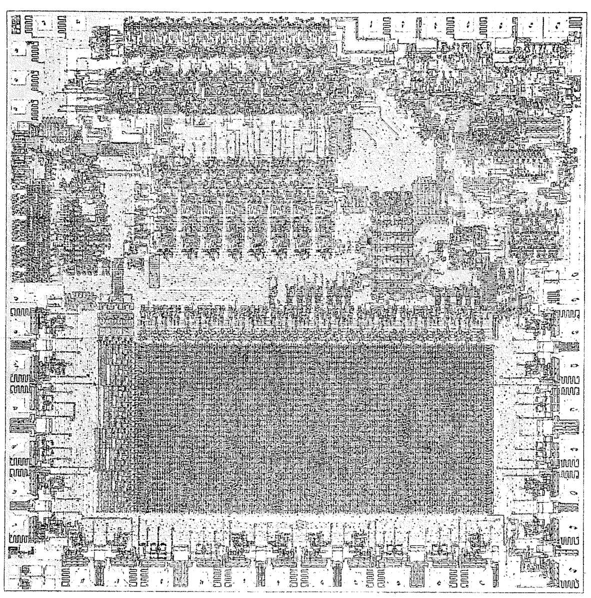


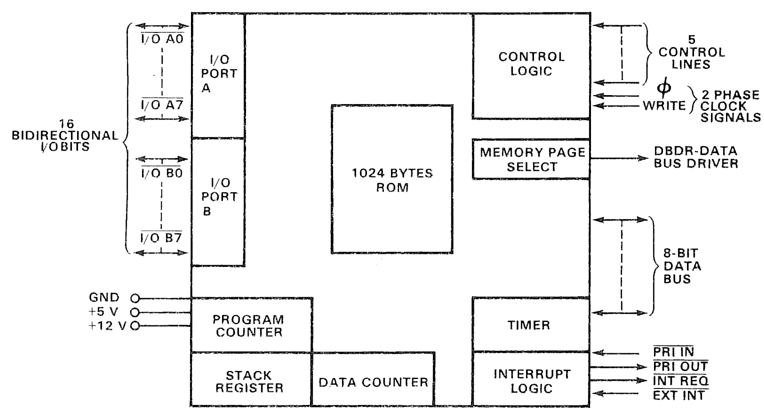
3850
CPU BLOCK DIAGRAM

3851 PROGRAM STORAGE UNIT

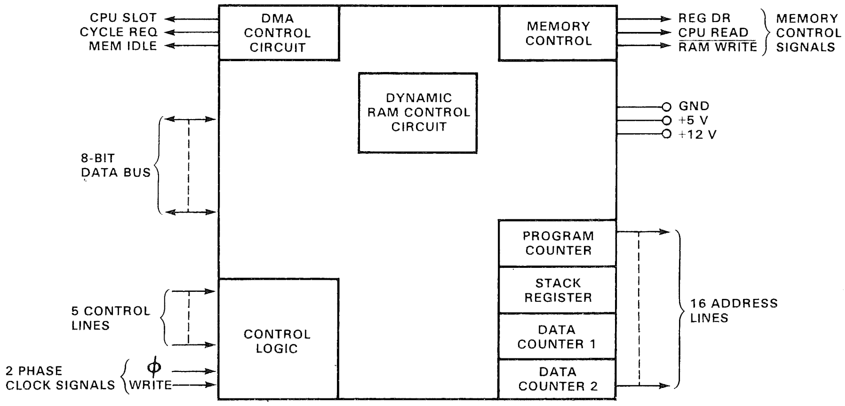
It is important to note that Fairchild's Program Storage Unit (PSU) is not just a conventional Read Only Memory. In addition to containing 1024 bytes of mask programmable ROM for program and constant storage, the F8 PSU includes the addressing logic for memory referencing, a Program Counter, an Indirect Address Register (the Data Counter) and a Stack Register. A complete vectored interrupt level, including an external interrupt line to alert the central processor, is provided. All of the logic necessary to request, acknowledge and reset the interrupt is on the F8 PSU. The 8-bit Programmable Timer is especially useful for generating real time delays. The PSU has an additional 16 bits of TTL compatible, bidirectional, fully latched I/O lines.

Systems requiring more program storage may be expanded by adding more PSU circuits. For example, one F8 CPU and three F8 PSUs will produce a microprocessor system complete with 64 bytes of RAM, 3072 bytes of ROM, 64 I/O bits, three interrupt levels, and three programmable timers. This complete system will require only four IC packages.

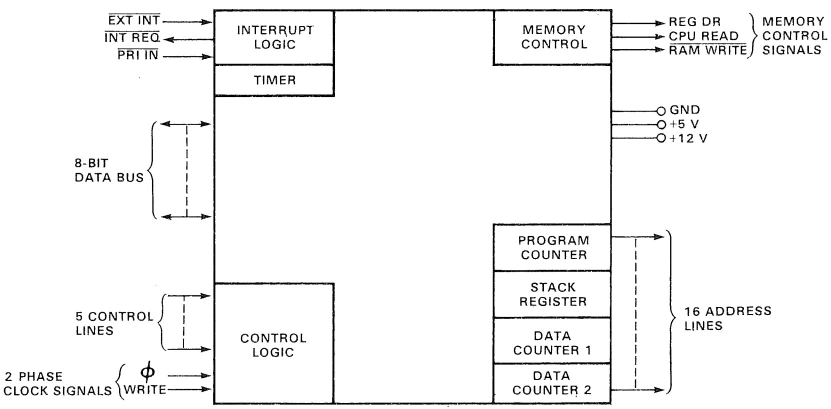




3851
PSU BLOCK DIAGRAM



3852
DMI BLOCK DIAGRAM

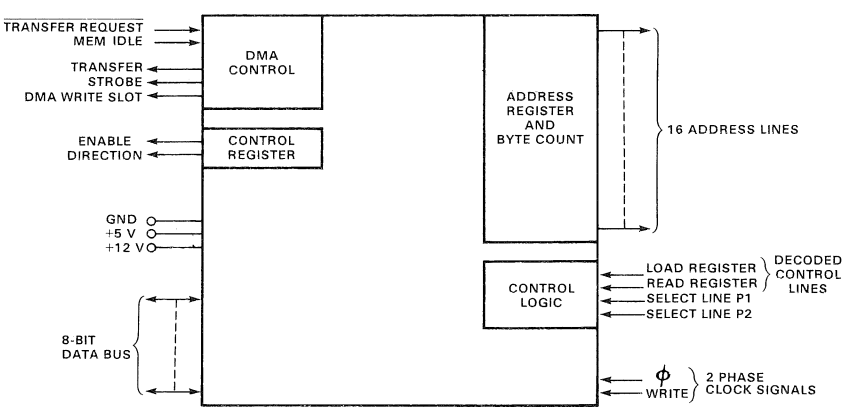


3853
SMI BLOCK DIAGRAM

3852/3853 MEMORY INTERFACE

For applications requiring more than the 64 byte RAM located on the CPU, two memory interface circuits are included in the F8 set. Each device generates the 16 address lines and the signals necessary to interface with up to 65K bytes of RAM, PROM or ROM memory. Either device may be used in conjunction with standard static semiconductor memory devices.

The Static Memory Interface (SMI) contains a full level of interrupt capability and a programmable timer. The Dynamic Memory Interface (DMI) contains all of the logic necessary to refresh MOS dynamic memories without degrading the system throughput time. The F8 DMI can also interface with static memories when desired.



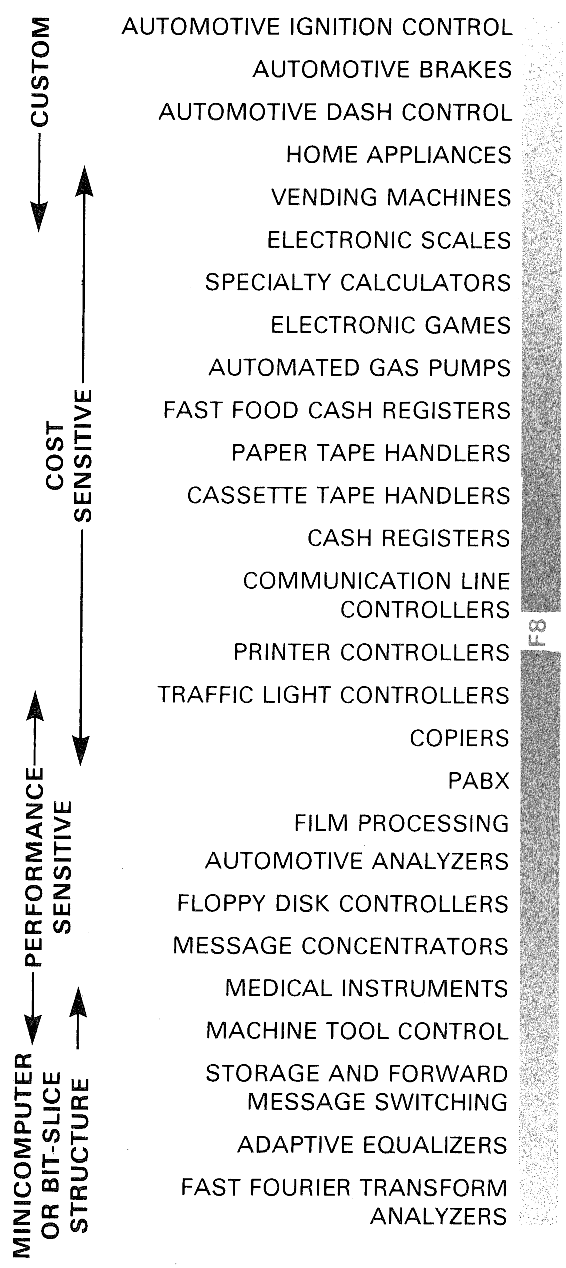
3854
DMA BLOCK DIAGRAM

3854 DIRECT MEMORY ACCESS

Fairchild's Direct Memory Access (DMA) device sets up a high speed data path to link F8 memory with peripheral electronics. The F8 DMA circuit, when working in conjunction with the F8 DMI, does not require overhead electronics to keep track of memory addresses, bytes transferred and handshaking signals. The data transfer is initiated by the CPU under program control. Once started, the DMA transfer will continue without CPU intervention. The CPU can sense the enable line of the DMA to determine the completion of a transfer. The entire DMA transfer will take place without halting the central processor.

F8 MICROPROCESSOR APPLICATION SPECTRUM

Because of its unique system partitioning, the F8 device set can be applied across a wide range of applications. The minimum two-circuit system is the basis for a modular architecture that can handle increasingly complex problems. A system of medium complexity can be designed by adding more F8 PSUs. The use of an F8 memory interface device allows up to 65K bytes of standard memories to be incorporated into the F8 system. For highly complex applications, independent F8 subsystems can be connected into a multiprocessing system in which each subsystem can operate independently yet can be controlled by one CPU that is the coordinator.



A TWO-CIRCUIT SYSTEM

The two-circuit F8 microprocessor is suitable for small data terminals, controllers, and specialty calculators. The keyboard is connected directly to the F8 I/O ports without special interfaces. Switch-bounce protection, rollover, and key encoding are all under software control. Software also decodes signals for LED readouts.

As an appliance controller, for example, the two-circuit system can perform all input-output sensing, actuating, timing, and computation operations. A system like the combination washing-machine-and-dryer controller in *Figure 1* requires more than 250 components when other microprocessor device sets are used, but with the F8 devices uses only 55 components, including 28 LEDs and the power semiconductor devices and relays used to control the motors. A set of custom circuits would also require about 50 parts, but initial engineering expense is heavy and severe penalties are incurred if changes are required. With the F8 system changes can be made by merely changing the program.

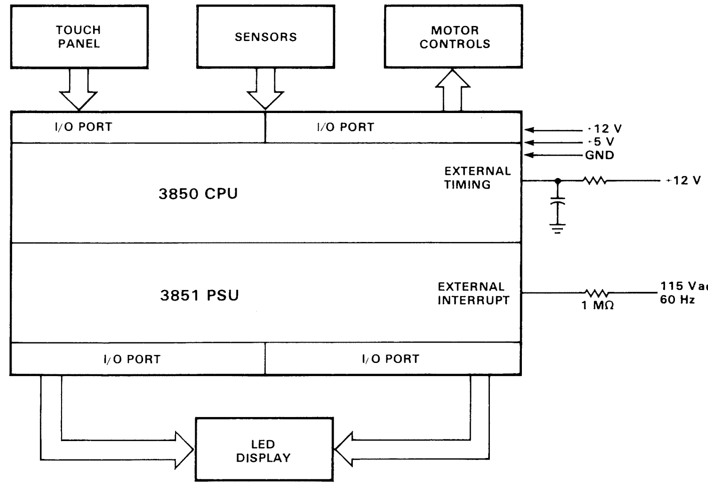


Fig. 1. Two-Circuit System

A MORE COMPLEX SYSTEM

The versatility of the F8 system is indicated by the traffic-light-controls system in *Figure 2*. The use of one CPU and two PSU circuits provides the designer with two timers, two interrupts, an onboard clock, onboard power-on reset, onboard switch decoding, and 48 bidirectional I/O bits. This system could be tied to vehicle detectors in the road, to monitor traffic for left-turn lanes as well as through-traffic flow in four directions. It would also react to interrupts from the pedestrian control buttons at each corner. There also is sufficient I/O capability to permit communication with and control of neighboring intersections and to allow the system to be operated manually or tested for proper operation.

Five F8 features are of particular interest for this type of application. One of the interrupts can eliminate the need for such external circuits as a comparator to compare a count of the cars with a predetermined value to cause the light to change. (The CPU can handle the simple arithmetic of counting cars.) This interrupt also eliminates the need for continuous polling of traffic count by the microcomputer. The second interrupt would be ideal for permitting pedestrian control to override the automatic system. The internal clock, with an external cyrstal, can also control light routines.

The two timers permit simultaneous counting of delay for vehicle signals and flashing warning lights for pedestrians. The onboard power-on reset acts in case of power failure to start the system automatically when power is renewed. The bidirectional I/Os have built-in latches that eliminate the need for external latches for the job of "holding" commands for lights as well as the momentary commands provided by timers and sensors.

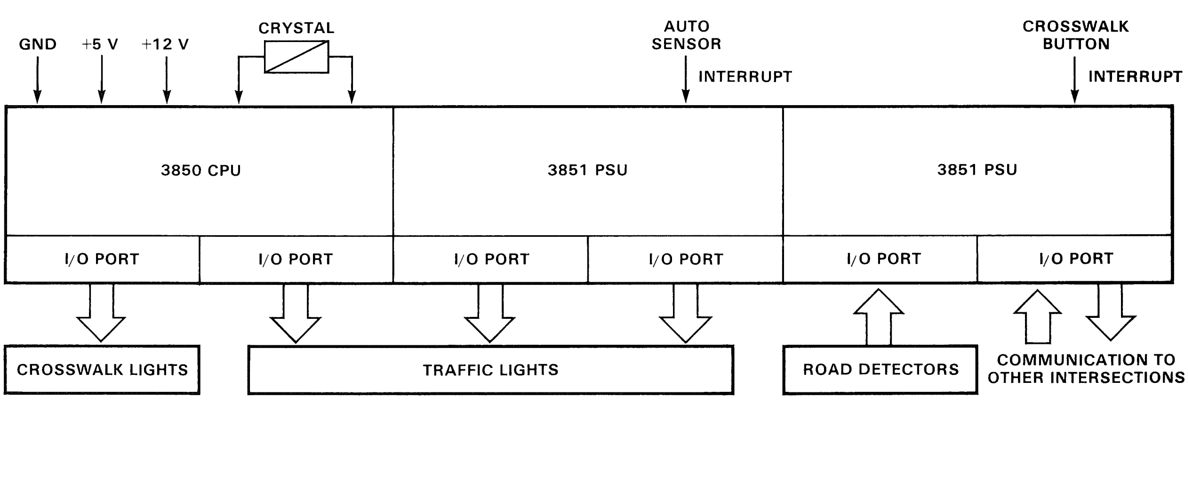


Fig. 2. Medium Complexity System

A MEMORY INTENSIVE SYSTEM

A typical application is a printing credit-verification terminal *(Figure 3)*. Such a system requires high performance and yet must be low in cost if it is to reach a large market. Only four different F8 devices are required to handle a keyboard input, visual display, card reader, and printer as well as provide a modem interface and memory interface for external RAM storage. This printing credit-verification system might be compared to a "bare mini-computer" in terms of utility, however, a detailed engineering evaluation would show that it costs less, has fewer parts and a more flexible I/O structure.

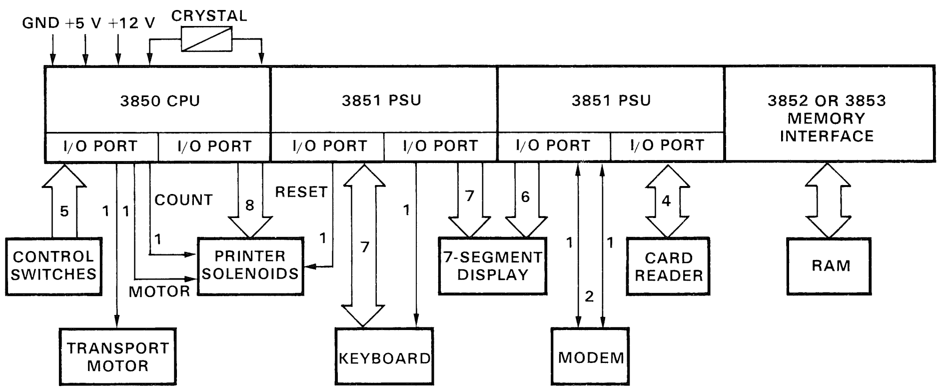


Fig. 3. Memory Intensive System

MULTI-MICROPROCESSOR SYSTEM

Figure 4 shows a specific application of the multi-processing concept as applied to a keyboard-to-floppy-disk system. Possibly this is the most cost-effective way of implementing this system, conservatively costing less than 50% of a conventional implementation. This system involves concurrent operation of three floppy disks, magnetic tape, CRT, keyboard, printer, and modem. While the low-speed devices (the keyboard, printer, and modem) can be adequately handled by the programmed I/O structure, the high-speed devices (disks, magnetic tape, and CRT) require separate F8 CPUs and PSUs.

This scheme provides simplicity of control, modularity, and freedom to expand. In this case, the units operating concurrently are: one magnetic-tape unit (25 μs/byte); three floppy-disk units (32 μs/byte each); and a CRT unit (71 μs/byte). This combination requires an aggregate bandwidth of 0.1478 byte/μs. This is well within the F8's upper bandwidth limit of 0.5 byte/μs.

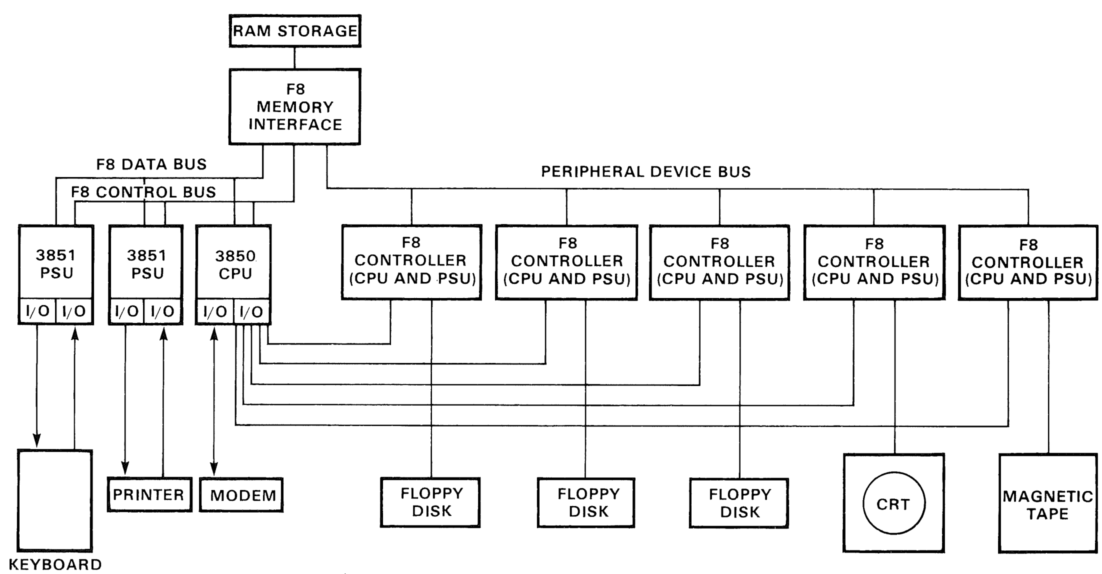


Fig. 4. Multi Microprocessor System

F8 CUSTOMER SUPPORT

Fairchild's F8 system is supported by extensive hardware and software aids. F8 devices, standard RAMs, ROMs and PROMs are available now.

F8 DEVELOPMENT HARDWARE

- F8M Development Module
  The F8M offers a basic development system for microprocessor projects.
- F8S Development Module*
  This unit provides expanded capability for memory-intensive applications.
- F8C Microcomputer*
  The F8C is a complete microcomputer system including power supplies and control panel. I/O ports are brought out to connectors. The F8C is provided with a Native Assembler, Debug Package and Source Editor.

F8 SOFTWARE

- Cross Assembler (FORTRAN IV)
  Accessible now on the G.E. and NCSS Timeshare Networks. Additional networks available as required.

*Available soon.

- Cross Simulator (FORTRAN IV)
  Accessible now on the same basis as Cross Assembler.

F8 DOCUMENTATION

- Microprocessor User's Manual
  The User's Manual provides device specifications, the instruction set in detail, and descriptions of the Cross Assembler and Simulator.
- Microprocessor Application Manual
  The Applications Manual provides initial details concerning bit manipulation, RAM expansion, extension of I/O ports, subroutines and boot strap loaders.

F8 FIELD SUPPORT

- Training
  A complete, hands-on, in-depth workshop to enable F8 users and potential users to design both hardware and software using the F8 microprocessor.
- Field Application Engineers
  Fairchild's knowledgeable FAEs will provide on-the-spot assistance with any F8 system application.

F8 INSTRUCTION SET SUMMARY

The F8 instruction set contains over 60 different instructions which may be subdivided into 10 categories: Accumulator, Scratchpad Register, Indirect Scratchpad Address Register, Memory Reference, Data Counter, Status Register, Program Counter, Branch, Interrupt Control and Input/Output instructions. Because 55% of the F8 instructions are only one byte long, programs are short and memory requirements significantly reduced. An alphabetic listing of the instructions is shown below. The following pages contain a complete description of the F8 instructions, including the cycle time. Each cycle is 2 μs for a system with a 2 MHz clock frequency.

F8 ADDRESSING MODES

The F8 instruction set has eight modes of referencing either I/O, CPU registers or bulk memory.

Implied Addressing – The data for this one-byte instruction is implied by the actual instruction. For example, the POP instruction automatically implies that the content of the Program Counter will be set to the value contained in the Stack Register.

Direct Addressing – In these two-byte instructions, the address of the operand is contained in the second byte of the instruction. The Direct Addressing mode is used in the Input/Output class of instructions.

Short Immediate Addressing – Instructions whose addressing mode is Short Immediate have the instruction op code as the first four bits and the operand as the last four bits. They are all one-byte instructions.

Long Immediate Addressing – In these two-byte instructions, the first instruction byte is the op code and the second byte is the 8-bit operand.

Direct Register Addressing – This mode of addressing may be used to directly reference the Scratchpad Registers. By including the register number in the one-byte instruction, 12 of the 64 Scratchpad Registers may be referenced directly.

Indirect Register Addressing – All 64 Scratchpad Registers may be indirectly referenced, using the Indirect Scratchpad Register in the CPU. This 6-bit register, which acts as a pointer to the scratchpad memory, may either be incremented, decremented, or left unchanged while accessing the scratchpad register.

Indirect Memory Addressing – A 16-bit Indirect Address Register, the Data Counter, points to either data or constants in bulk memory. A group of one-byte instructions is provided to manipulate this area of memory. These instructions imply that the Data Counter is pointing to the desired memory byte. The Data Counter is self-incrementing, allowing for an entire data field to be scanned and manipulated without requiring special instructions to increment its content. The memory interface circuit contains two interchangeable data counters.

Relative Addressing – All F8 Branch Instructions use the relative addressing mode. Whenever a branch is taken, the Program Counter is updated by an 8-bit relative address contained in the second byte of the instruction. A branch may extend 128 locations forward or 127 locations back.

ALPHABETIC LIST OF INSTRUCTIONS

ADC	Add Data Counter with Accumulator
AI	Add Immediate with Accumulator
AM	Add Binary Accumulator with Memory
AMD	Add Decimal Accumulator with Memory
AS	Add Binary Accumulator with Scratchpad Register
ASD	Add Decimal Accumulator with Scratchpad Register
BC	Branch on Carry
BF	Branch on False Condition
BM	Branch if Negative
BNC	Branch if no Carry
BNO	Branch if no Overflow
BNZ	Branch if no Zero
BP	Branch if Positive
BR	Absolute Branch
BR7	Branch if ISAR is not 7
BT	Branch on True Condition
BZ	Branch on Zero Condition
CI	Compare Immediate
CLR	Clear Accumulator
CM	Compare with Memory
COM	Complement Accumulator
DCI	Load Data Counter Immediate
DI	Disable Interrupt
DS	Decrement Scratchpad Register
EI	Enable Interrupt
INC	Increment Accumulator
IN	Input
INS	Input Short
JMP	Jump
LI	Load Accumulator Immediate
LIS	Load Accumulator Short
LISL	Load ISAR – Lower 3 Bits
LISU	Load ISAR – Upper 3 Bits
LM	Load Memory
LNK	Link Carry into Accumulator
LR	Load Register (5 Types)
	Scratchpad
	Program Counter
	ISAR
	Status
	Data Counter
NI	Logical AND Accumulator Immediate
NM	Logical AND Memory Accumulator
NOP	No Operation
NS	Logical AND Scratchpad and Accumulator
OI	Logical OR Immediate
OM	Logical OR Memory with Accumulator
OUT	Output
OUTS	Output Short
PI	Push Program Counter into Stack Register Set Program Counter to New Location
PK	Push Program Counter into Stack Register Set Program Counter from Scratchpad
POP	Put Stack Register into Program Counter
SL	Shift Left
SR	Shift Right
XDC	Exchange Data Counters
XI	Exclusive OR Immediate
XM	Exclusive OR Accumulator with Memory
XS	Exclusive OR Accumulator with Scratchpad

ACCUMULATOR GROUP INSTRUCTIONS

OPERATION	MNEMONIC OP CODE	OPERAND	FUNCTION	MACHINE CODE	BYTES	CYCLES	STATUS BITS			
							OVF	ZERO	CRY	SIGN
ADD CARRY	LNK		ACC←(ACC) + CRY	19	1	1	1/0	1/0	1/0	1/0
ADD IMMEDIATE	AI	ii	ACC←(ACC) + H'ii'	24ii	2	2.5	1/0	1/0	1/0	1/0
AND IMMEDIATE	NI	ii	ACC←(ACC) ∧ H'ii'	21ii	2	2.5	0	1/0	0	1/0
CLEAR	CLR		ACC←H'00'	70	1	1	–	–	–	–
COMPARE IMMEDIATE	CI	ii	H'ii' + $\overline{\text{ACC}}$ + 1	25ii	2	2.5	1/0	1/0	1/0	1/0
COMPLEMENT	COM		ACC←(ACC) ⊕ H'FF'	18	1	1	0	1/0	0	1/0
EXCLUSIVE-OR IMMEDIATE	XI	ii	ACC←(ACC) ⊕ H'ii'	23ii	2	2.5	0	1/0	0	1/0
INCREMENT	INC		ACC←(ACC) + 1	1F	1	1	1/0	1/0	1/0	1/0
LOAD IMMEDIATE	LI	ii	ACC←H'ii'	20ii	2	2.5	–	–	–	–
LOAD IMMEDIATE SHORT	LIS	i	ACC←H'0i'	7i	1	1	–	–	–	–
OR IMMEDIATE	OI	ii	ACC←(ACC) ∨ H'ii'	22ii	2	2.5	0	1/0	0	1/0
SHIFT LEFT ONE	SL	1	SHIFT LEFT 1	13	1	1	0	1/0	0	1/0
SHIFT LEFT FOUR	SL	4	SHIFT LEFT 4	15	1	1	0	1/0	0	1/0
SHIFT RIGHT ONE	SR	1	SHIFT RIGHT 1	12	1	1	0	1/0	0	1
SHIFT RIGHT FOUR	SR	4	SHIFT RIGHT 4	14	1	1	0	1/0	0	1

BRANCH INSTRUCTIONS

In all conditional branches PC_0←(PC_0) + 2 if the test condition is not met. Execution is complete in 3.0 cycles.

OPERATION	MNEMONIC OP CODE	OPERAND	FUNCTION	MACHINE CODE	BYTES	CYCLES	STATUS BITS			
							OVF	ZERO	CRY	SIGN
BRANCH ON CARRY	BC	aa	PC_0←[(PC_0) + 1] + H'aa' if CRY = 1	82aa	2	3.5	–	–	–	–
BRANCH ON POSITIVE	BP	aa	PC_0←[(PC_0) + 1] + H'aa' if SIGN = 1	81aa	2	3.5	–	–	–	–
BRANCH ON ZERO	BZ	aa	PC_0←[(PC_0) + 1] + H'aa' if ZERO = 1	84aa	2	3.5	–	–	–	–
BRANCH ON TRUE	BT	taa	PC_0←[(PC_0) + 1] + H'aa' if any test is true	8taa	2	3.5	–	–	–	–
			t = TEST CONDITION 2^2 2^1 2^0 ZERO CRY SIGN							
BRANCH IF NEGATIVE	BM	aa	PC_0←[(PC_0) + 1] + H'aa' if SIGN = 0	91aa	2	3.5	–	–	–	–
BRANCH IF NO CARRY	BNC	aa	PC_0←[(PC_0) + 1] + H'aa' if CARRY = 0	92aa	2	3.5	–	–	–	–
BRANCH IF NO OVERFLOW	BNO	aa	PC_0←[(PC_0) + 1] + H'aa' if OVF = 0	98aa	2	3.5	–	–	–	–
BRANCH IF NOT ZERO	BNZ	aa	PC_0←[(PC_0) + 1] + H'aa' if ZERO = 0	94aa	2	3.5	–	–	–	–
BRANCH IF FALSE TEST	BF	taa	PC_0←[(PC_0) + 1] + H'aa' if all false test bits	9taa	2	3.5	–	–	–	–
			t = TEST CONDITION 2^3 2^2 2^1 2^0 OVF ZERO CRY SIGN							
BRANCH IF ISAR (LOWER) ≠ 7	BR7	aa	PC_0←[(PC_0) + 1] + H'aa' if ISARL ≠ 7 PC_0←(PC_0) + 2 if ISARL = 7	8Faa	2	2.5 2.0	– –	– –	– –	– –
BRANCH RELATIVE	BR	aa	PC_0←[(PC_0) + 1] + H'aa'	90aa	2	3.5	–	–	–	–
JUMP*	JMP	aaaa	PC_0←H'aaaa'	29aaaa	3	5.5	–	–	–	–

*Privileged instruction

MEMORY REFERENCE INSTRUCTIONS

In all Memory Reference Instructions, the Data Counter is incremented $DC \leftarrow DC + 1$.

OPERATION	MNEMONIC OP CODE	OPERAND	FUNCTION	MACHINE CODE	BYTES	CYCLES	STATUS BITS OVF	ZERO	CRY	SIGN
ADD BINARY	AM		$ACC \leftarrow (ACC) + [(DC)]$	88	1	2.5	1/0	1/0	1/0	1/0
ADD DECIMAL	AMD		$ACC \leftarrow (ACC) + [(DC)]$	89	1	2.5	1/0	1/0	1/0	1/0
AND	NM		$ACC \leftarrow (ACC) \wedge [(DC)]$	8A	1	2.5	0	1/0	0	1/0
COMPARE	CM		$[(DC)] + \overline{(ACC)} + 1$	8D	1	2.5	1/0	1/0	1/0	1/0
EXCLUSIVE OR	XM		$ACC \leftarrow (ACC) \oplus [(DC)]$	8C	1	2.5	0	1/0	0	1/0
LOAD	LM		$ACC \leftarrow [(DC)]$	16	1	2.5	–	–	–	–
LOGICAL OR	OM		$ACC \leftarrow (ACC) \vee [(DC)]$	8B	1	2.5	0	1/0	0	1/0
STORE	ST		$(DC) \leftarrow (ACC)$	17	1	2.5	–	–	–	–

ADDRESS REGISTER GROUP INSTRUCTIONS

OPERATION	MNEMONIC OP CODE	OPERAND	FUNCTION	MACHINE CODE	BYTES	CYCLES	STATUS BITS OVF	ZERO	CRY	SIGN
ADD to DATA COUNTER	ADC		$DC \leftarrow (DC) + (ACC)$	8E	1	2.5	–	–	–	–
CALL to SUBROUTINE*	PK		$PC_0U \leftarrow (r12)$; $PC_0L \leftarrow (r13)$; $PC_1 \leftarrow (PC_0)$	0C	1	4	–	–	–	–
CALL to SUBROUTINE IMMEDIATE*	PI	aaaa	$PC_1 \leftarrow (PC_0)$; $PC_0 \leftarrow H'aaaa$	28aaaa	3	6.5	–	–	–	–
EXCHANGE DC	XDC		$DC_0 \rightleftarrows DC_1$	2C	1	2	–	–	–	–
LOAD DATA COUNTER	LR	DC,Q	$DCU \leftarrow (r14)$; $DCL \leftarrow (r15)$	0F	1	4	–	–	–	–
LOAD DATA COUNTER	LR	DC,H	$DCU \leftarrow (r10)$; $DCL \leftarrow (r11)$	10	1	4	–	–	–	–
LOAD DC IMMEDIATE	DCI	aaaa	$DC \leftarrow H'aaaa'$	2Aaaaa	3	6	–	–	–	–
LOAD PROGRAM COUNTER	LR	P0,Q	$PC_0U \leftarrow (r14)$; $PC_0L \leftarrow (r15)$	0D	1	4	–	–	–	–
LOAD STACK REGISTER	LR	P,K	$PC_1U \leftarrow (r12)$; $PC_1L \leftarrow (r13)$	09	1	4	–	–	–	–
RETURN FROM SUBROUTINE*	POP		$PC_0 \leftarrow (PC_1)$	1C	1	2	–	–	–	–
STORE DATA COUNTER	LR	Q,DC	$r14 \leftarrow (DCU)$; $r15 \leftarrow (DCL)$	0E	1	4	–	–	–	–
STORE DATA COUNTER	LR	H,DC	$r10 \leftarrow (DCU)$; $r11 \leftarrow (DCL)$	11	1	4	–	–	–	–
STORE STACK REGISTER	LR	K,P	$r12 \leftarrow (PC_1U)$; $r13 \leftarrow (PC_1L)$	08	1	4	–	–	–	–

SCRATCHPAD REGISTER INSTRUCTIONS

(Refer to Scratchpad Addressing Modes)

OPERATION	MNEMONIC OP CODE	OPERAND	FUNCTION	MACHINE CODE	BYTES	CYCLES	STATUS BITS OVF	ZERO	CRY	SIGN
ADD BINARY	AS	r	$ACC \leftarrow (ACC) + (r)$	Cr	1	1	1/0	1/0	1/0	1/0
ADD DECIMAL	ASD	r	$ACC \leftarrow (ACC) + (r)$	Dr	1	2	1/0	1/0	1/0	1/0
DECREMENT	DS	r	$r \leftarrow (r) + H'FF'$	3r	1	1.5	1/0	1/0	1/0	1/0
LOAD	LR	A,r	$ACC \leftarrow (r)$	4r	1	1	–	–	–	–
LOAD	LR	A,KU	$ACC \leftarrow (r12)$	00	1	1	–	–	–	–
LOAD	LR	A,KL	$ACC \leftarrow (r13)$	01	1	1	–	–	–	–
LOAD	LR	A,QU	$ACC \leftarrow (r14)$	02	1	1	–	–	–	–
LOAD	LR	A,QL	$ACC \leftarrow (r15)$	03	1	1	–	–	–	–
LOAD	LR	r,A	$r \leftarrow (ACC)$	5r	1	1	–	–	–	–
LOAD	LR	KU,A	$r12 \leftarrow (ACC)$	04	1	1	–	–	–	–
LOAD	LR	KL,A	$r13 \leftarrow (ACC)$	05	1	1	–	–	–	–
LOAD	LR	QU,A	$r14 \leftarrow (ACC)$	06	1	1	–	–	–	–
LOAD	LR	QL,A	$r15 \leftarrow (ACC)$	07	1	1	–	–	–	–
AND	NS	r	$ACC \leftarrow (ACC) \wedge (r)$	Fr	1	1	0	1/0	0	1/0
EXCLUSIVE OR	XS	r	$ACC \leftarrow (ACC) \oplus (r)$	Er	1	1	0	1/0	0	1/0

*Privileged instruction

MISCELLANEOUS INSTRUCTIONS

OPERATION	MNEMONIC OP CODE	OPERAND	FUNCTION	MACHINE CODE	BYTES	CYCLES	STATUS BITS OVF	ZERO	CRY	SIGN
DISABLE INTERRUPT	DI		RESET ICB	1A	1	2	–	–	–	–
ENABLE INTERRUPT*	EI		SET ICB	1B	1	2	–	–	–	–
INPUT	IN	aa	ACC←(INPUT PORT aa)	26aa	2	4	0	1/0	0	1/0
INPUT SHORT	INS	a	ACC←(INPUT PORT a)	Aa	1	4***	0	1/0	0	1/0
LOAD ISAR	LR	IS,A	ISAR←(ACC)	0B	1	1	–	–	–	–
LOAD ISAR LOWER	LISL	a	ISARL←a	1101a**	1	1	–	–	–	–
LOAD ISAR UPPER	LISU	a	ISARU←a	01100a**	1	1	–	–	–	–
LOAD STATUS REGISTER*	LR	W,J	W←(r9)	1D	1	2	1/0	1/0	1/0	1/0
NO-OPERATION	NOP		PC_0←(PC_0) + 1	2B	1	1	–	–	–	–
OUTPUT	OUT	aa	OUTPUT PORT aa←(ACC)	27aa	2	4	–	–	–	–
OUTPUT SHORT	OUTS	a	OUTPUT PORT a←(ACC)	Ba	1	4***	–	–	–	–
STORE ISAR	LR	A,IS	ACC←(ISAR)	0A	1	1	–	–	–	–
STORE STATUS REG	LR	J,W	r9←(W)	1E	1	1	–	–	–	–

*Privileged instruction
**3-bit octal digit
***2 machine cycles for CPU ports

NOTES

Each lower case character represents a Hexadecimal digit
Each cycle equals 4 machine clock periods
Lower case denotes variables specified by programmer

Function Definitions

←	is replaced by
( )	the contents of
(–)	Binary "1"s complement of
+	Arithmetic Add (Binary or Decimal)
⊕	Logical "OR" exclusive
∧	Logical "AND"
∨	Logical "OR" inclusive
H' '	Hexadecimal digit

Register Names

a	Address Variable
A	Accumulator
DC	Data Counter (Indirect Address Register)
DC_0	Data Counter #0 (Indirect Address Register #0)
DC_1	Data Counter #1 (Indirect Address Register #1)
DCL	Least significant 8 bits of Data Counter Addressed
DCU	Most significant 8 bits of Data Counter Addressed
H	Scratchpad Register #10 and #11
i and ii	immediate operand
ICB	Interrupt Control Bit
IS	Indirect Scratchpad Address Register
ISAR	Indirect Scratchpad Address Register
ISARL	Least Significant 3 bits of ISAR
ISARU	Most Significant 3 bits of ISAR
J	Scratchpad Register #9
K	Registers #12 and #13
KL	Register #13
KU	Register #12
PC_0	Program Counter
PC_0L	Least Significant 8 bits of Program Counter
PC_0U	Most Significant 8 bits of Program Counter
PC_1	Stack Register
PC_1L	Least Significant 8 bits of Program Counter
PC_1U	Most Significant 8 bits of Active Stack Register
Q	Registers #14 and #15
QL	Register #15
QU	Register #14
r	Scratchpad Register (any address thru 11)
W	Status Register

Scratchpad Addressing Modes (Machine Code Format)

r = C	(Hexadecimal), Register Addressed by ISAR (Unmodified)
r = D	(Hexadecimal), Register Addressed by ISAR; ISARL Incremented
r = E	(Hexadecimal). Register Addressed by ISAR; ISARL Decremented
r = F	(No operation performed)
r = 0 thru B	(Hexadecimal), Register 0 thru 11 addressed directly from the Instruction

Status Register

–	No change in condition
1/0	is set to "1" or "0" depending on conditions
CRY	Carry Flag
OVF	Overflow Flag
SIGN	Sign of Result Flag
ZERO	Zero Flag

POWER REQUIREMENTS: V_{DD} = +5.0 V ±5%; V_{GG} = +12.0 V ±5%; V_{SS} = 0 V; T_A = 0°C to 70°C; f = 2 MHz

PART TYPE	SYMBOL	PARAMETER	TYP	MAX	UNITS	TEST CONDITIONS (Outputs Unloaded)
3850	I_{DD} I_{GG}	V_{DD} Current V_{GG} Current	30 15	80 25	mA mA	2 MHz
3851	I_{DD} I_{GG}	V_{DD} Current V_{GG} Current	30 10	70 18	mA mA	2 MHz
3852 3853	I_{DD} I_{GG}	V_{DD} Current V_{GG} Current	35 13	70 30	mA mA	2 MHz
3854	I_{DD} I_{GG}	V_{DD} Current V_{GG} Current	20 15	40 28	mA mA	2 MHz

SIGNAL ELECTRICAL SPECIFICATIONS : V_{DD} = +5.0 V ±5%; V_{GG} = +12.0 V ±5%; V_{SS} = 0 V; T_A = 0°C to 70°C; f = 2 MHz

SIGNAL NAME (NUMBER, TYPE)	SOURCE OR RECEIVING DEVICE	V_{OH} MIN	V_{IH} MIN	V_{OL} MAX	V_{IL} MAX	LOAD
DATA BUS (8 INPUTS/OUTPUTS)	3850 3851 3852/3 3854	3.9	3.5	0.4	0.8	100 pF I_{SOURCE} = −100 μA I_{SINK} = 900 μA
CONTROL BUS (5 OUTPUTS)	3850	3.9		0.4		100 pF, I_{SINK} = 900 μA I_{SOURCE} = −100 μA
CONTROL BUS (5 INPUTS)[1]	3851 3852/3		3.5		0.8	
I/O PORTS (16 INPUTS/OUTPUTS)	3850 3851	2.9 (1 TTL) 3.9 (unloaded)	3.5[2]	0.4	0.8	100 pF plus 1 H-TTL Load
CLOCK REFERENCE (INPUT)	3850		4.0		0.8	
SYSTEM CLOCKS (PHI AND WRITE OUTPUTS)	3850	4.4		0.4		100 pF, I_{SINK} = 900 μA I_{SOURCE} = −100 μA
SYSTEM CLOCKS (PHI AND WRITE INPUTS)	3851 3852/3 3854		4.0		0.8	
RESET (INPUT)	3850		3.5[2]		0.8	I_{IL} = 0.3 mA Max at V_{IN} = V_{SS}
INTERRUPT CONTROL BIT (OUTPUT)	3850	3.9		0.4		50 pF plus 100 μA I_{SOURCE} or I_{SINK}
INTERRUPT REQUEST (INPUT)	3850		3.5[2]		0.8	I_{IL} = 1 mA Max at V_{IN} = 0.4
INTERRUPT REQUEST (OUTPUT)	3851 3853	OPEN DRAIN		0.4		100 pF plus I_{SINK} = 1 mA
EXTERNAL INTERRUPT (INPUT)	3851 3853		3.5		1.2	
PRIORITY IN (INPUT)	3851 3853		3.5		0.8	
PRIORITY OUT (OUTPUT)	3851	3.9		0.4		50 pF plus 100 μA I_{SOURCE} or I_{SINK}
DBDR (OUTPUT)	3851	OPEN DRAIN[3]		0.4		100 pF plus I_{SINK} = 2.5 mA
ADDRESS LINES and RAM WRITE (16 OUTPUTS)	3852/3 3854	4.0		0.4		500 pF plus 2 TTL Loads
REGDR (INPUT/OUTPUT)	3852/3	3.9	3.5	0.4	0.8	100 pF plus 1 H-TTL Load
CPU READ (OUTPUT)	3852/3	3.9		0.4		50 pF plus 1 H-TTL Load
MEM IDLE, CYCLE REQ and CPU SLOT (OUTPUTS)	3852	3.9		0.4		50 pF plus 1 H-TTL Load
MEM IDLE (INPUT)	3854		3.5		0.8	
ENABLE, DIRECTION, TRANSFER, DMA WRITE SLOT, STROBE (OUTPUTS)	3854	3.9		0.4		50 pF plus 1 H-TTL Load
XFER REQ, P1,P2 (INPUTS)	3854		3.5		0.8	
LOAD REG, READ REG (INPUTS)	3854		3.5		0.8	

[1]3854 receives two control signals from external decoding device. [2]Internal pull-up resistor to V_{DD}. [3]External pull-up resistor required.

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