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FUJITSU

PRODUCT PROFILE

MB86684

Integrated Terminal Controller (ITC_25)

Integrated Terminal Controller

The FUJITSU MB86684 is a highly integrated terminal controller for broadband ATM terminal equipment. It provides segmentation and re-assembly functions together with physical layer functions for the IBM 25.6 Mbps format.

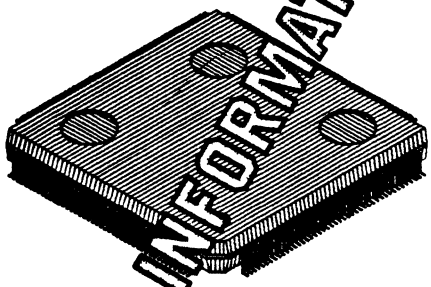
By incorporating a multiplexed ISA/PCMCIA compliant 8/16-bit slave interface the ITC is ideally suited to applications in ATM adapter cards for PC's.

The device conforms to all relevant ATM Forum, CCITT, and ANSI standards.

FEATURES

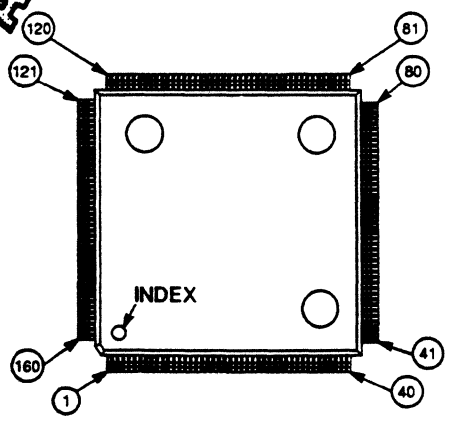
- Combines a full-duplex segmentation and re-assembly controller with physical layer framing functions.
- Supports segmentation and reassembly on up to 1K simultaneous VCs, with 32 separate traffic profiles.
- Implements AAL5 adaptation layer protocols on each VC.
- Implements 4B/5B encoding and decoding, NRZI serialiser and scrambler/descrambler functions.
- Supports local DRAM interface for temporary storage of reordered transmit and receive cell data, allowing system bus decoupling from transceiver interface.
- Performs traffic shaping for each VC using peak and sustainable cell rate parameters, including peak rate control of CLP0 and CLP0+1 traffic.
- Glueless multiplexed ISA/PCMCIA compliant 8/16-bit slave interface in accordance with P996 and PCMCIA Revision 2.1, respectively. Also supports a 32-bit generic interface.
- Serial E^2PROM interface for device configuration. Implement the Microsoft™ Plug & Play version 1.08 for ISA cards.
- Fabricated in sub-micron CMOS technology with CMOS/TTL compatible I/O and single +5V power supply.

PLASTIC PACKAGE
QFP160 (TBD)



ADVANCE INFORMATION

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1. OVERVIEW

The ITC is a bus slave device. A system diagram is shown in Fig 1.

It is a highly integrated ATM terminal controller, providing support for AAL5 adaptation layer and IBM 25.6 Mb/s physical layer interface functions. AAL5 frame processing, segmentation and re-assembly is supported on up to 1024 full duplex Virtual Channels (VC's) simultaneously. Traffic shaping on each VC can be controlled by 32 separate traffic profiles, using Peak, Sustainable, CLP0 and CLP1 parameters, based on a "Leaky Bucket" principle, for CBR and VBR traffic. ABR traffic is also supported.

Transceiver data can be temporarily buffered in Local Ram memory, on a channel basis, allowing data to be transferred across the system bus independently of the transceiver interface ordering.

Two unframed modes of operation are also provided, cell transparent and protocol transparent, which do not support AAL5 functions.

Microsoft™ Plug & Play operations are supported, as defined in version 1.08 of the specification.

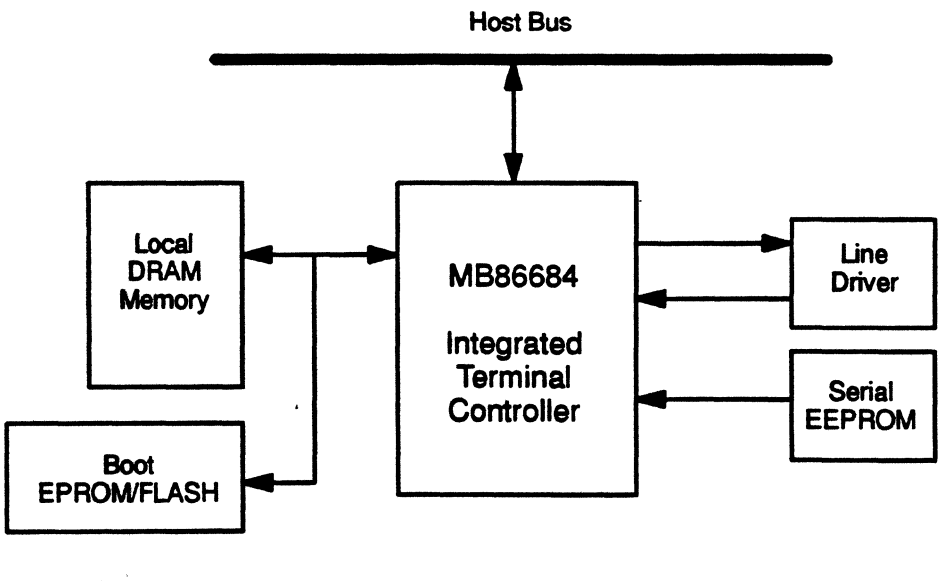


Fig 1 – ITC system configuration

2. EXTERNAL INTERFACES

2.1 Logical Outline

A logical view of the ITC's external pins is illustrated in Fig 2, and a physical pin assignment diagram is shown in Appendix NO TAG In the diagram below, common signals refer to the ISA / PCMCIA / GENERIC buses respectively.

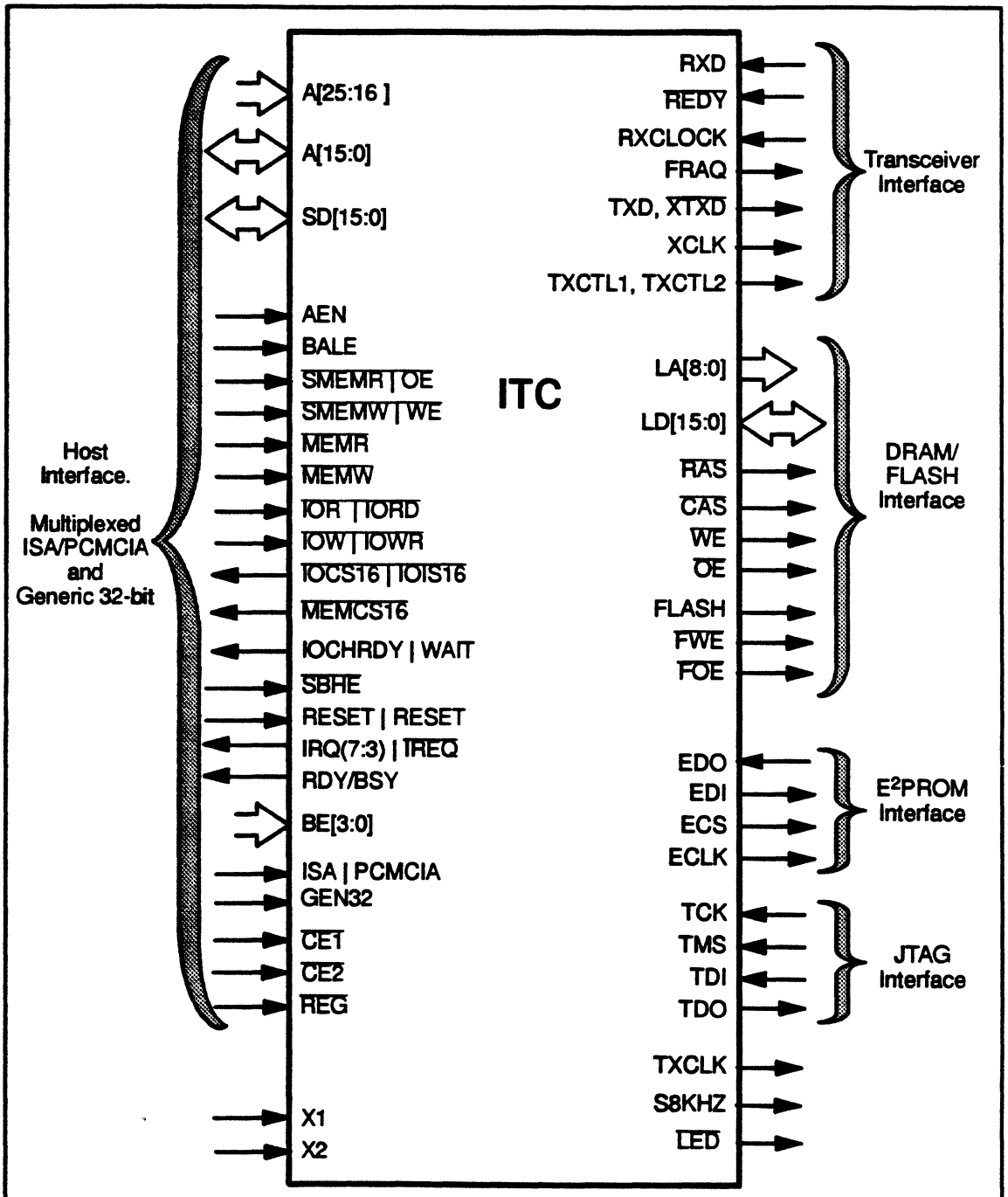


Fig 2 – ITC external interfaces

2.2 Detailed Description

2.2.1 Host System Interface

The host system interface consists of three separate bus protocols. These are an ISA or PCMCIA 8 or16 bit interface, and a 32 bit GEN32 generic interface. Signal commonality enables many of the chip pins to be multiplexed. Bus mode selection is by the ISA/PCMCIA pin, or the GEN32 pin.

ISA, PCMCIA, and GEN32 Buses
The ISA bus conforms to the IEEE P996 Bus Specification.

The PCMCIA bus conforms to version 2.1 of the specification.

The Generic bus enables a simple multiplexed address and data operation to be performed.

Signals
The host interface consists of the following signals :-

A[25:0]
These address pins control either I/O or memory accesses to the ITC.

In ISA mode, the signals LA[23:17] are mapped to A[23:17], and the signals SA[16:0] are mapped to A[16:0].

ISA, GEN32
I/O accesses are specified by the SA[15:0] pins. The ITC is mapped to the range 0B00h to 0BF0h.

Memory accesses are specified by the bits A[23:0], giving a range of 16 MB. The ITC is mapped to the range 0C0000h to 0DE000h, via an 8KB window.

In GEN32 mode, the pins A[15:0] are also used for the most significant 16 data bits of a 32 bit transfer.

PCMCIA
I/O accesses are specified by the bits A[3:0], and the pins REG, CE1 and CE2.

Memory accesses are specified by all the bits A[25:0], giving a range of 64 MB. The ITC is mapped to the range 00C0000h to 00DE000h, via an 8KB window.

SD[15:0]
Bi-directional pins for transferring data between the ITC and host. Both 8-bit and 16-bit data transfers can be performed for ISA/PCMCIA, and in GEN32 mode the pins form the least significant 16 data bits of a 32 bit transfer.

AEN
Active high Address Enable signal for ISA and GEN32 modes.

BALE
Bus Address Latch Enable indicates valid A[23:0], AEN and $\overline{\text{SBHE}}$ signals. Address is latched on the falling edge of BALE. Applies to ISA and GEN32 modes.

$\overline{\text{SMEMR}}$ | $\overline{\text{OE}}$
Active low System Memory Read signal for first 1Mbyte of memory. In PCMCIA mode this signal is used to gate memory read data (Memory Read).

$\overline{\text{SMEMW}}$ | $\overline{\text{WE}}$
Active low System Memory Write signal for first 1Mbyte of memory. In PCMCIA mode this signal is used to strobe write data in to the ITC (Memory Write).

$\overline{\text{MEMR}}$
Active low Memory Read signal for accesses above 1Mbyte in ISA/GEN32.

$\overline{\text{MEMW}}$
Active low Memory Write signal for accesses above 1Mbyte in ISA/GEN32.

$\overline{\text{IOR}}$ | $\overline{\text{IORD}}$
This signal is driven low by the bus master during an I/O Read in ISA/GEN32. In PCMCIA mode this input signal is used to perform I/O read accesses.

$\overline{\text{IOW}}$ | $\overline{\text{IOWR}}$
This signal is driven low by the bus master during an I/O Write. In PCMCIA mode this input signal is used to perform I/O write accesses.

$\overline{\text{MEMCS16}}$
The ITC can accept a 16 bit memory access, in ISA mode.

$\overline{\text{IOCS16}}$ | $\overline{\text{IOIS16}}$
This output indicates a 16-bit I/O access cycle. Open drain output in ISA and GEN32 modes. In PCMCIA mode it is asserted by the ITC to indicate 16-bits wide accesses from the ITC's I/O space.

IOCHRDY | WAIT
Indicates to the bus master that the ITC will extend the bus cycle time. Open drain output in ISA and GEN32 modes. In PCMCIA mode this signal is used by the ITC to extend the host bus cycle.

$\overline{\text{SBHE}}$
This input indicates that valid data is being transferred on SD[15:8], the high byte lane, in ISA mode.

RESET | RESET
This signal is used to initialise the ITC. This pin is Active High in all modes.

IRQ[7:3] | $\overline{\text{IREQ}}$
Active high interrupt signals to the host processor in ISA and GEN32 modes. In PCMCIA mode Active low interrupt signal (shared with IRQ3) to the host processor.

BE[3:0]
Byte enables for GEN32 interface.

RDY/BSY
To be defined tbd

$\overline{\text{CE1}}$
In PCMCIA mode this is an active low Card Enable input used for even numbered byte addressing.

$\overline{\text{CE2}}$
In PCMCIA mode this is an active low Card Enable input used for odd numbered byte addressing.

$\overline{\text{REG}}$
In PCMCIA mode this active low signal is used to perform limited accesses to Attribute Memory.

ISA/PCMCIA
Selects between the ISA bus (Low), and the PCMCIA bus (High). The GEN32 pin must be Low.

GEN32
Selects the GEN32 bus mode when High.

2.2.2 Local Memory Interface.

The local memory interface is used to provide temporary storage for receive and transmit cell data, and to access the Flash PROM. All control descriptors are also stored in the memory. After chip initialisation, the interface requires no further host attention.

LA[9:0]
Address signals, for the Ram or Flash.

LD[15:0]
16-bit bi-directional data bus, for the Ram or Flash.

$\overline{RAS}$
Provides the Row Address Strobe signal to the local DRAM.

$\overline{CAS}$
Provides the Column Address Strobe signal to the local DRAM.

$\overline{WE}$
This signal is the active low Write Enable to the DRAM.

$\overline{OE}$
Output enable for the DRAM.

FLASH
This signal is the select signal for the external Flash PROM.

$\overline{FWE}$
This signal is the active low Write Enable to the Flash PROM.

$\overline{FOE}$
Output enable for the Flash PROM

2.2.3 Serial E^2PROM Interface

The serial E^2PROM Interface allows the implementation of 'jumperless' designs. The interface comprises the following signals.

ECLK
This output signal is used to transfer serial data between the ITC and the serial E^2PROM.

ECS
Used to select the serial E^2PROM.

EDI
This output pin is used to transfer serial data to the serial E^2PROM.

EDO
This input pin is used to transfer serial data from the serial E^2PROM to the ITC.

2.2.4 Transceiver Interface

This interface is used to transfer transmit and receive data between the ITC and an external line driver/transceiver device. The transceiver interface comprises the following signals.

RXD
Recovered data. Serial receive data signal.

$\overline{REDY}$
Active low ready signal.

RXCLOCK
Clock recovered from transceiver device to the ITC.

FRAQ
Frequency Acquisition Control.

TXD, $\overline{XTXD}$
Differential serial data outputs to the transceiver device.

XCLK
32 MHz clock, used by the PLL in the transceiver, gated by FRAQ.

TXCTL1, TXCTL2
User definable outputs, programmed via host. These may be used to control the transceiver/buffer devices operating mode (eg WRAP loopback mode control).

S8KHZ
The 8 KHz timing pulse from the transceiver.

2.2.5 JTAG Interface

A 4-pin general purpose TAP (test access port) is provided to access the functional blocks of the ITC. The port conforms to IEEE P1149.1-1990 and includes the following signals.

TCK
Test Clock Input provides the clock for the test logic.

TMS
Test Mode Select. TMS is decoded by the TAP to control test operations.

TDI
Test Data Input. Serial input port for test instructions and data.

TDO
Test Data Output. Serial output for test instructions and data.

2.2.6 Miscellaneous

X1
32 MHz external crystal input.

X2
32 MHz external crystal input.

TXCLK
Used for debug purposes only. This is the clock used to control the transmit path logic within the ITC, and is either the recovered clock from the receive path, or the XCLK signal.

$\overline{\text{LED}}$
Used to control an LED. When lit, the LED signifies that the receive link is operating, and that the transmit path is using the recovered receive clock.

3. FUNCTIONAL DESCRIPTION

The ITC is divided into the following functional units, as shown in Fig 3:-

- Host Interface
- Local Ram Interface
- Address Map
- Traffic Management
- Transceiver Interface
- Miscellaneous
  - OAM
  - Transparent Modes
  - Initialisation
  - Statistics

3.1 Host Interface

The ITC is a bus slave device, and will only transfer data across the system bus under host control.

Access can be via an I/O or memory mapped mechanism, as defined in the Functional Operations section.

3.2 Local Ram Interface

The local ram is used to store cell data, channel descriptors, and all other housekeeping information required by the ITC.

The organisation of the local ram is as shown in the Functional Operations section.

The interface is autonomously controlled by the ITC, using local ram descriptors, and once initialised does not require host attention.

The local ram consists of 256 K words by 16 bits of Dram.

3.3 Address Map Module

The ITC can support up to 1024 bi-directional channels. Virtual channels (VPI/VCI addresses) are mapped to physical channels (numbered from 0 upwards) using the following mechanism.

An ATM cell header contains an 8 bit VPI field, and a 16 bit VCI field. The ITC can only support a maximum of 13 address bits from the above two fields, as shown in Fig 4.

The bit selections within each field must be contiguous, and start at bit 0.

The Concatenated VPI/VCI (CPC) Size parameter is used to select the total number of CPC bits used for address translations. The VPI Size parameter is used to select the number of VPI bits within the CPC address.

The address formed from the concatenated P and C bits is used to directly address a block of pointers in local ram. These pointers are then used to access the local ram descriptors.

A descriptor pair (Rx and Tx) exists for each physical channel supported. The channels are numbered from 0 up to Maxch.

Reserved Channels
Three descriptor are reserved for OAM cells, RM cells and a Dump channel.

Maximum Channels
The ITC can be configured to support up to a maximum number of physical channels, using the Maxch parameter. The number of pointers initialised by the host must not exceed this value eg 3 in Fig 4.

This strategy allows a large spread of VPI/VCI address bits to be used, while allowing only a small number of actual VCC channels to be supported.

3.4 Traffic Management

The traffic management module is responsible for controlling all data transmitted by the ITC, and contains 32 traffic profiles. Each profile can be configured to control CBR, VBR or ABR traffic.

3.4.1 CBR Profile Parameters

Constant Bit Rate profiles operate on a leaky bucket principle, defined in terms of the following parameters.

Peak Transmission Rate
This parameter determines the rate at which cells can be transmitted. It consists of two 4-bit fields, a mantissa and an exponent. The method provides approximately a 6% resolution in cell transmission scheduling, and the time interval between transmitted cells can be varied between approximately 2 microseconds and 20 milliseconds.

Sustainable Cell Rate
This 5 bit counter determines the fractional tokens (N÷32) added to the leaky bucket, at peak rate intervals. Each time the counter overflows, a cell is added to the bucket, while the residue remains in the counter.

Leaky Bucket Capacity
This 8-bit register determines the size of the leaky bucket ie the maximum number of cells (represented by tokens) which can be sent at peak rate intervals. Each time a cell is transmitted the number of tokens in the bucket is decremented by one. A cell will only be transmitted if a token is available, and once empty, the bucket must be refilled before transmission can resume.

CLP0 Rate
This 7-bit counter determines the ratio of CLP0 to CLP1 cells. Normally, 1 in N cells will be scheduled to be sent as CLP1 ie the cell can be discarded in a congested network. Each time a cell is scheduled, the counter is decremented, and when it reaches zero, the cell is transmitted as CLP1.

The counter can be set to predefined values to enable cells to always be sent as either CLP0 (counter = 7E) or CLP1 (counter = 7F).

Profile Priority
This 2-bit field defines the profile priority. The lowest priority is 0, and the highest 3. Higher priority profile requests will pre-empt lower priority requests.

Pre-empted profile requests will be marked as pending, and serviced when no other higher priority profiles are scheduled.

3.4.2 ABR Profile Parameters

Available Bit Rate profiles operate on an opportunistic, dynamically varying peak rate, and are defined by the ATM Forum in terms of the following parameters.

Allowed Cell Rate, ACR
A dynamically adjusted rate (controlled by MDF or AIR) at which cells are actually transmitted by the traffic manager, on a VC basis.

Peak Cell Rate, PCR
A per VC maximum cell rate, which must not be exceeded by the ACR.

Minimum Cell Rate, MCR
A per VC minimum value for the ACR.

Initial Cell Rate, ICR
A per VC initial value for ACR. The channel will drop to this rate, when idle.

Additive Decrease Rate, ADR
A per VC factor, which is used to decrease the ACR, at ACR intervals.

Multiplicative Decrease Factor, MDF
A per VC factor, used to calculate ADR.

Additive Increase Rate, AIR
A per VC factor used to increase the ACR, on reception of an RM cell.

Nrm
A per VC counter value, decremented at ACR intervals, which when zero gives the opportunity for the generation of an RM cell.

3.4.3 GFC Protocol

A per link ABR control mechanism is also available, defined in terms of the GFC field.

Four codes are specified, as follows :-

0000 Null & No Halt
0100 Null & Halt
1000 Reset & No Halt
1100 Reset & Halt

Reset refers to a credit counter, which must contain tokens to allow ABR traffic to be scheduled. A reset command restores the initial value in the counter.

3.4.4 Parameter Values

At call setup, the host must agree the quality of service required with the network. Traffic conformance is then maintained by setting the values of the parameters to meet the agreed profile.

3.4.5 Channel Assignments

Any VC can be assigned to any traffic profile. If multiple VC's are assigned to the same profile, the cells are transmitted contiguously, unless interrupted by a higher priority profile. All channels assigned to the higher priority profile will be serviced, before the lower priority profile queue is restarted.

CBR Traffic
CBR traffic can be handled by assigning the channels to the highest priority profile. This will ensure that the channel cells are always transmitted when the peak rate counter terminates, unless a clash occurs with another high priority profile. In these circumstances, the channels will be handled in the order in which the profiles are found, using the ITC search algorithm. This continuously checks all profiles, in a circular fashion, looking for terminated peak rate counters.

VBR Traffic
This is the same as CBR traffic, except that the data will occur in bursts, provided that the sustainable rate is less than the peak rate.

ABR Traffic
ABR traffic can be handled by assigning the channels to a profile priority which is lower than CBR or VBR traffic (if any exists). This will ensure that the channel cells are only transmitted when other traffic is not scheduled.

If a channel assigned to a particular profile is required to alter its transmission rate, it is re-assigned to another profile automatically.

3.5 Transceiver Interface

The transceiver interface consists of two sections, a receive and a transmit port. Each port contains a single bit data bus, and associated control signals.

The interface is autonomously controlled by the ITC, and does not require host attention.

It conforms to the IBM 25.6 MHz physical layer interface specifications, using 4B/5B NRZI coding.

3.6 Miscellaneous

The following functions are also supported by the ITC.

OAM
All OAM cells are stored in a single area in local ram, for transfer to the host. All the ATM cell is stored, except for the HEC byte ie 52 bytes.

Transparent Modes
Two additional modes of operation are also possible, which are not covered by AAL5 framing. These are Cell Transparent and Payload Transparent.

In Cell transparent, 52 bytes (all the ATM cell, except for the HEC byte) are stored in the local ram, for transfer to host memory,

In Payload transparent mode, only the payload is stored.

Initialisation
All descriptors, including the free lists, must be initialised by the host, before operations can begin. This is defined in the Functional Operations section.

Statistics
Various statistics are maintained by the ITC, to enable the host to monitor the system. These are detailed in the Functional Operations section.

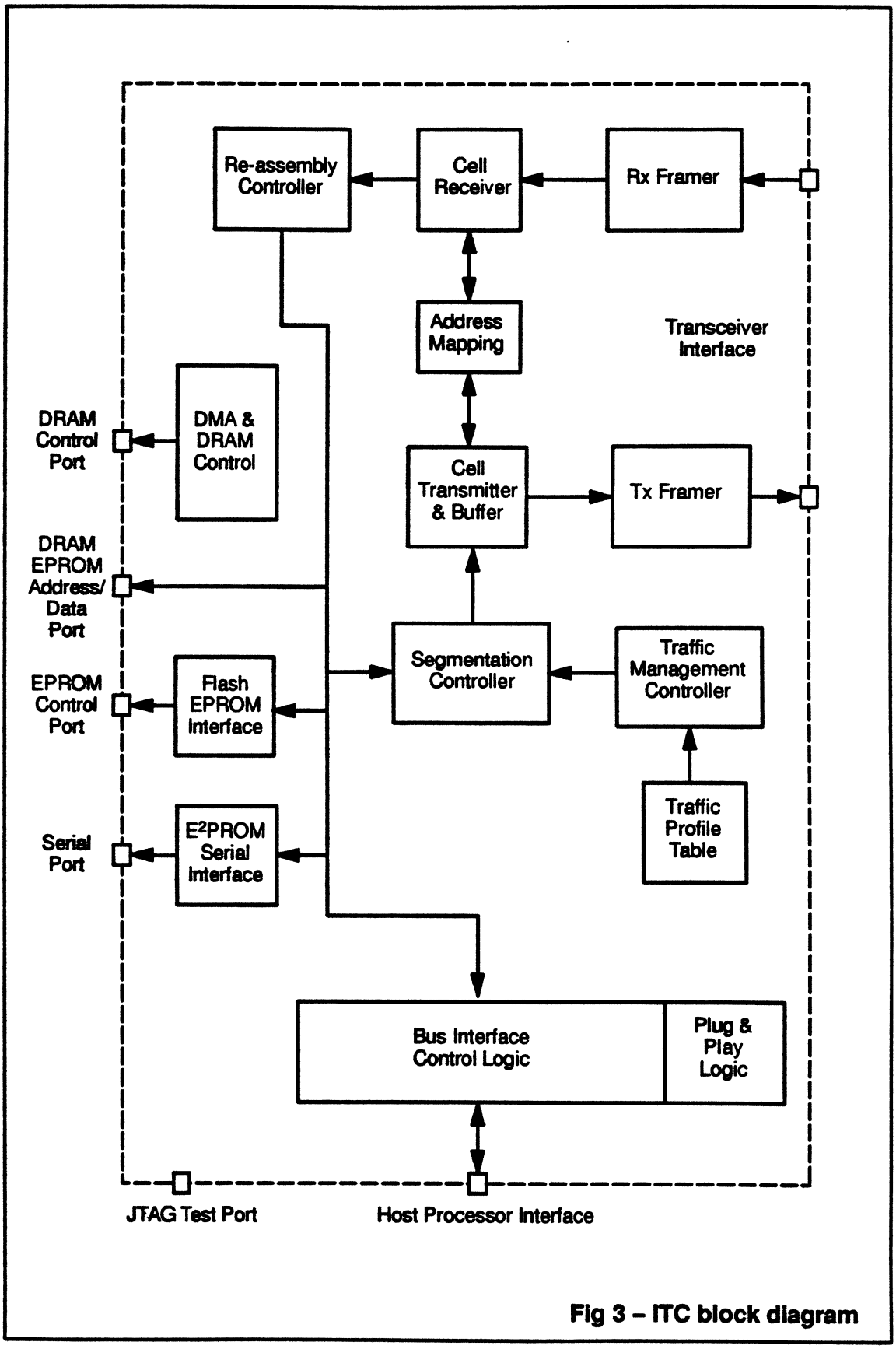
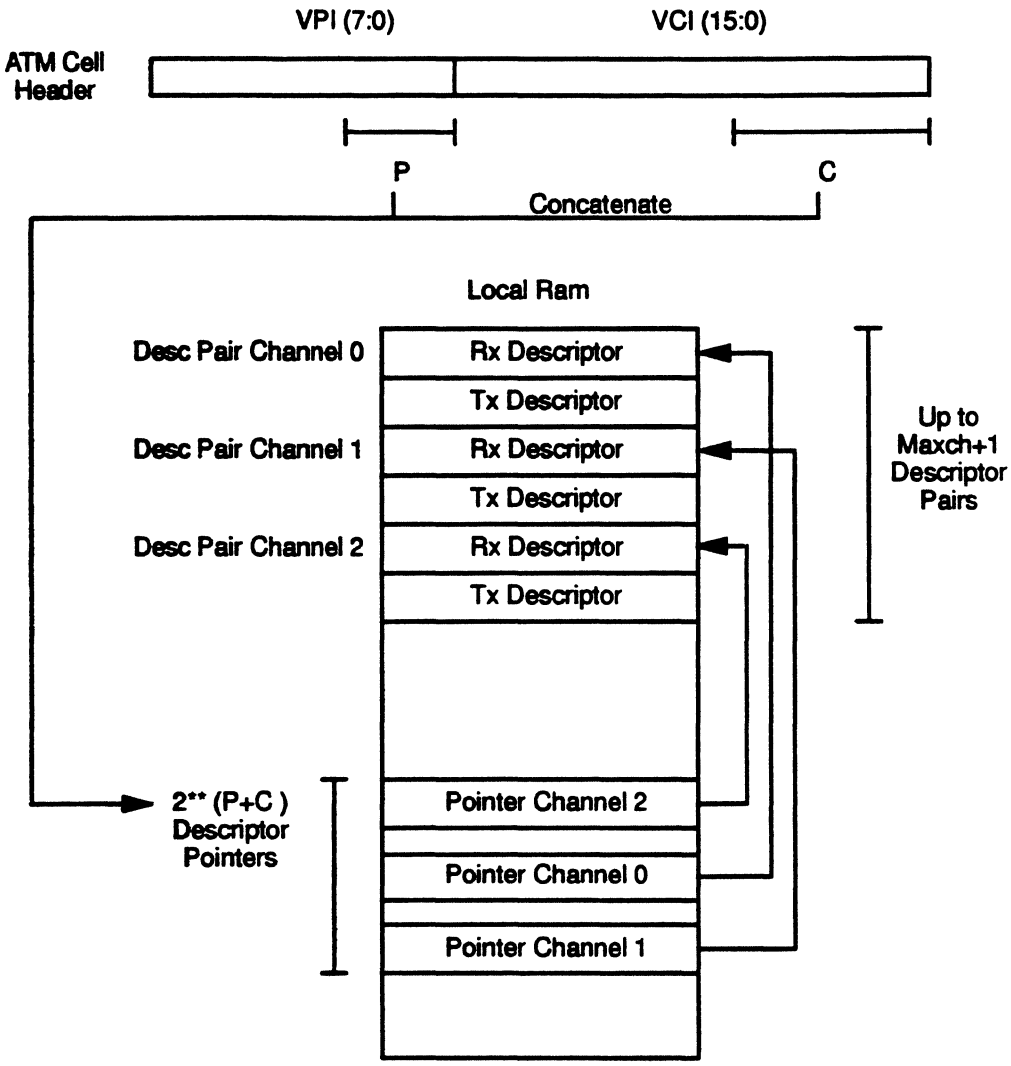


Fig 3 – ITC block diagram

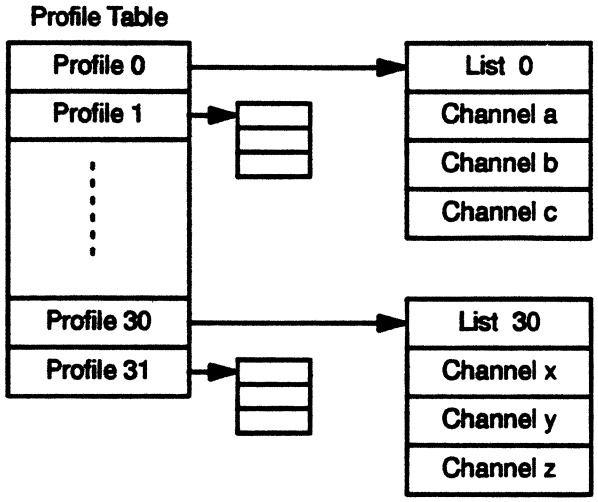


CPC Size	Total bits P + C	Pointers
0	7	128
1	8	256
2	9	512
3	10	1024
4	11	2048
5	12	4096
6	13	8192

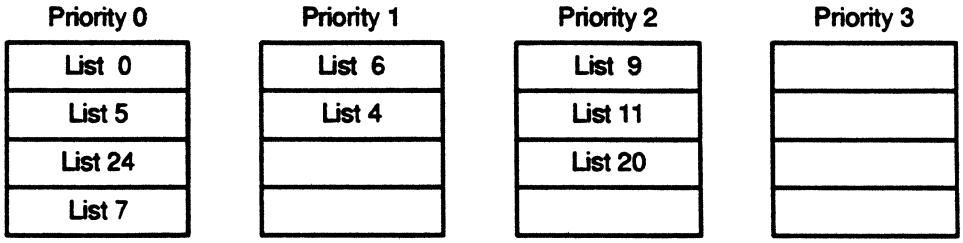
VPI Size	P bits
0	1
1	2
2	3
3	4

Address Translation field select codes

Fig 4 – Address Map Channel Selection



Channel Assignments



Transmit Priority Queues

Fig 5 – Channel Assignments and Priority Queues

4. FUNCTIONAL OPERATIONS

4.1 Receive Operations

The transceiver interface module decodes the physical layer framing functions, and the AAL5 adaption layer protocols. It supplies cell payload data in 48 byte blocks (in the order in which they were received on the transceiver interface) for storage in the local ram. The re-assembled data is stored on a logical channel basis, allowing it to be accessed independently of the transceiver interface reception ordering.

A local ram descriptor (one per channel) is used to facilitate the storage and forwarding of the data to host memory, when requested by the host.

Local Ram Organisation
The local ram contains all descriptors necessary for data reception by the ITC, and space for the data payloads, as shown symbolically in Fig 6.

Blocks of local ram are available for use by the ITC for payload data, organised as a linked list of 64 bytes each, called the receive free list, as shown in Fig 7. These blocks can be allocated to any channel as required, on a dynamic basis, when receive data is stored in local ram. Individual channel data will then itself be stored as a linked list of blocks. Each logical channel can store as many cells or frames of data as local ram capacity allows. Blocks are returned to the free list as data is transferred to host memory.

Local Ram Receive Descriptors
The descriptors used for linked list local ram operations are as shown in Fig 8. The fields in the descriptor have the following functionality :-

- Channel start
  The first host bus cell in a channel
- Channel finish
  The last transceiver cell in a channel
- Channel status 1
  Channel and frame status
- Channel status 2
  Channel and frame status
- Frame count
  The number of frames in a channel
- CRC (31:16)
  The most significant AAL5 CRC bits
- CRC (15:0)
  The least significant AAL5 CRC bits
- AAL5 control
  The control field from an AAL5 frame
- AAL5 length
  The number of bytes contained in the AAL5 frame
- Read frame finish
  The last cell of the current bus frame
- Read frame cell count
  The number of cells in the current frame being read by the host
- Read frame length
  The number of bytes remaining in the frame being read by the host
- Write frame start
  The start of the current transceiver interface frame
- Write frame cell count
  The number of cells in the transceiver interface frame
- Write frame length
  The number of bytes in the transceiver interface frame

- Status 1
  - 0 CLP1 cell received, transceiver interface
  - 1 Command byte error, transceiver interface
  - 2 Cell lost, transceiver interface
  - 3 Length register error, transceiver interface
  - 4 Congestion state
  - 5 On payload queue
  - 6 Channel empty
  - 7 Reserved (TCPF)
  - 8 Purge Channel
  - 9 Purge frame
  - 10 Interrupted frame
  - 11 Incomplete frame
  - 12 Reserved (WBF)
  - 13 Reserved (RBF)
  - 14 Payload Transparent
  - 15 Cell Transparent

- Status 2
  - 5 Priority [0]
  - 6 Priority [1]
  - 7 Threshold [0]
  - 8 Threshold [1]
  - 9 CLP1 cell received, host interface
  - 10 Cell lost, host interface
  - 11 CRC error
  - 12 Command byte error, host interface
  - 13 Abort, length zero
  - 14 Length formula error
  - 15 Length register error, host interface

Local Ram Receive Queue

A threshold level can be specified, on a channel basis, such that when the amount of data held in local ram exceeds a specified amount, it is scheduled for transfer to host memory. The ITC appends the channel number to the Receive Queue, which exists in local ram, and is formatted as shown in Fig 9.

This queue must be read by the host, to determine which channels require transferring to host memory.

Receive Queue Control

The queue consists of a 2 kilobyte circular buffer, and is controlled by two ITC registers. The LRRQS register points to the start of the queue, and the LRRQC counter gives the number of entries in the queue.

The LRRQS register is incremented automatically by the ITC, when the host reads items from the queue.

The LRRQC counter is incremented by the ITC when channel numbers are added to the queue, and decremented by the ITC when channel numbers are read from the queue by the host.

The queue must be located in local ram on a 2 KB boundary, using the LRRQB register.

Receive Queue Interrupt
When entries are first placed in the receive queue, an interrupt is generated for the host. The host must empty the queue before additional interrupts will be generated, which requires the host to check for additional entries (by reading the LRRQC), after reading the number of entries originally indicated by the LRRQC.

4.2 Transmit Operations

These are broadly the opposite of the receive sequence operations.

Local Ram Organisation
The local ram contains all descriptors necessary for data transmission by the ITC, and space for the data payloads, as shown in Fig 6.

A transmit free list exists in local ram, to hold data transferred from host memory, in individual logical channels, pending transmission. The list is organised and operated identically to the receive free list, as shown in Fig 7.

Local Ram Transmit Descriptors
The descriptors used for linked list local ram operations are as shown in Fig 10. The fields in the descriptor have the following functionality :-

- Channel start
  The first transceiver cell in a channel
- Channel finish
  The last host bus cell in a channel
- Channel status
  Channel and frame status
- CRC (31:16)
  The most significant AAL5 CRC bits
- CRC (15:0)
  The least significant AAL5 CRC bits
- AAL5 control
  The control field for an AAL5 frame
- Read frame finish
  The last cell of the transceiver frame
- Read frame cell count
  The number of cells in the current frame being sent to the transceiver
- Read frame length
  The number of bytes remaining in the frame being sent to the transceiver
- Write frame start
  The start of the current host interface frame
- Write frame cell count
  The number of cells in the host interface frame
- Write frame length
  The number of bytes in the host interface frame
- Status 1
  0 RM received
  1 EFCI sent
  2 Reserved (1st access)
  3 Unused
  4 Congestion received
  5 Delete from profile list (host)
  6 Channel empty
  7 Reserved (TCPF)
  8 Unused
  9 Unused
  10 Interrupted frame
  11 Incomplete frame
  12 Reserved (WBF)
  13 Reserved (RBF)
  14 Payload Transparent
  15 Cell Transparent

- Status 2
  - 5 On profile list
  - 6 Unused
  - 7 Unused
  - 8 Unused
  - 9 Unused
  - 10 Unused
  - 11 Unused
  - 12 Unused
  - 13 Host abort (AAL5 length zero)
  - 14 Unused
  - 15 Length register error, host interface

Transmission Sequences
Cells are scheduled for transmission under the control of the Traffic Management module.

Each traffic profile has a list of channels assigned to it (see chapter 3). When the peak rate counter reaches zero, all channels assigned to the profile are appended to a priority scheduling queue. The ITC services these queues in priority order, transmitting a cell if it is available in the local ram logical channels.

If the local ram does not contain data to be transmitted, the channel will be bypassed. If no channels are queued for transmission, an idle cell will be scheduled.

4.3 Data Transfers

Data Alignment
The ITC utilises a Little Endian address mechanism. Receive data transferred to system memory from the ITC can initially be aligned on any byte boundary in host memory. Transmit data to be transferred from system memory to the ITC can also initially be aligned at any byte boundary in memory.

Data Deletion
The ITC can delete frames which have been partially or wholly received in local ram, frames which have been partially transferred to system memory, or frames which have not yet been completely received in local ram, but which have also been partially transferred to system memory. The ITC can also delete all data in a given channel.

These operations are carried out by the ITC under host control, using the purge commands.

4.4 Traffic Management

The ITC can only approximate the Forum requirements for ABR traffic, and does not implement precisely the currently proposed scheme (ATM Forum / 94-0438R1).

The ITC can autonomously process ABR related traffic management functions eg congestion and RM cell generation. Alternatively, the automatic mechanism can be disabled, requiring these operations to be handled by the host.

Traffic Profiles
The traffic management module contains 32 profiles. A profile can be configured to control CBR, VBR or ABR traffic.

ABR profiles must form a contiguous block, within the profile tables, to enable the ABR traffic requirements to be met.

The organisation of the Profile Tables, Channel Lists, and list placements within the Local Ram are shown in Fig 11.

Parameters for all types of profiles are as shown in Fig 12, and have been defined in chapter 3.

Profile Channel Assignments
Each profile has a list of channels assigned to it by the host. A list can contain up to Maxch+1-4 entries.

Channels assigned by the host to CBR/VBR profiles will always remain attached to that profile.

Channels assigned by the host to ABR profiles can be moved by the ITC to different profiles. This allows the ITC to implement a strategy which is a close approximation of the ATM Forum requirements for ABR traffic.

Channel Movement
A channel is moved to a lower profile after a number of cells have been transmitted at ACR intervals. The number is specified by the ADR Count field in the channel traffic management descriptor.

A channel is moved to a higher profile when an RM cell is received.

RM Cell Generation
All ABR cells must normally be transmitted with the EFCI bit set to 1. One cell in every Nrm cells must be transmitted with the EFCI bit set to 0. The value of Nrm is specified by the Nrm Count field in the channel traffic management descriptor.

The EFCI = 0 cell is an opportunity for the destination end system to generate an RM cell, and hence increase the source ACR.

Profile Sequences
All ABR profiles must be arranged contiguously in the profile tables, as shown in Fig 11. The peak values for the profiles should form an approximate linear sequence, between the highest and lowest ABR rates required. Profile 31 represents the lowest throughput channels, and must therefore contain the largest peak rate interval counter value.

ACR Decrease
A channel is always moved down by one profile (from profile N to profile N+1) when the ACR must be reduced.

ACR Increase
An RM cell must cause a nett increase in the channel ACR since the previous RM cell. This is achieved by copying the value of the RM AIR parameter from the new profile, after an ACR increment.

A subsequent ACR increase will cause the channel to be assigned to the profile specified by the copied RM AIR parameter.

Data Unavailability
If data is unavailable for transmission while a channel's ACR is above it's ICR, the channel will be moved down the profiles towards its ICR profile, using the normal rate reduction mechanism.

If data is unavailable for transmission while the channel's ACR is at or below its ICR profile, it will be deleted from the profile lists. The channel will then be assigned to it's ICR profile, if new data becomes available.

Traffic Management Descriptors
The descriptors used for traffic management control are shown in Fig 13. The fields in the descriptor have the following meaning :-

- Initial Profile
  The profile to which a channel is initially assigned, and to which a channel will drop, when no data is available for transmission
- Minimum Profile
  The lowest profile to which a channel can drop, due to ACR decreases
- Maximum Profile
  The highest profile to which a channel can rise, due to ACR increases
- RM AIR Copy
  A copy of the RM AIR profile parameter
- ADR Count
  A count of the number of cells to be transmitted, before the ACR is decreased
- Nrm Count
  A count of the number of cells to be transmitted, before allowing an opportunity for an ACR increase.
- VCI
  The VCI address of the ATM cell
- VPI
  The VPI address of the ATM cell

CBR / VBR Profiles
These consist of the parameters shown in Fig 12, and as described in chapter 3.

ABR Profiles
These consist of the parameters shown in Fig 12, and as described in chapter 3.

There are also two counter decrement factors, held in the profile lists, associated with ABR profiles, as shown in Fig 11. These values are used to decrement the ADR and Nrm counters specified in the traffic management descriptors.

Decrementing the ADR and Nrm counters by values other than one allows greater flexibility in traffic management strategies.

4.5 Reserved Channels

The reserved channel descriptors are used for OAM cells, RM cells and to control a dump channel.

4.5.1 OAM

OAM cells are processed in Cell Transparent mode. The ITC also optionally checks/generates the CRC10 field.

Receive
All OAM F5 cells are transferred to host memory using the Receive Descriptor for physical channel zero, which must be reserved for this purpose.

Transmit
F5 cells must be assembled by the host, and transmitted on descriptor channel 0.

F4 Cells
OAM F4 cells can be combined with the F5 cells on channel 0, or they can be transferred on separate F4 channels, using the normal pointer / descriptor mechanism. The initialisation of the pointers in the address translation module determines which mechanism is used.

4.5.2 RM Cells

RM cells can be processed automatically by the ITC, or else by the host.

ITC Processed
On receiving an RM cell, the ITC will set a status bit in the corresponding transmit descriptor, to cause the channel to be moved to a new profile. The RM cell can also be scheduled for transmission to the host, for information purposes, if this mechanism is enabled.

Host Processed
Resource Management cells are processed in Cell Transparent mode. They are transferred to and from host memory on physical channel one, which must be reserved for this purpose.

Priority
It is up to the host to read RM cells on the receive channel. A bit is set in the chip status register when receive cells exist in channel one, and a programmable interrupt can be generated when data is received, if the channel is empty.

The host must set a status bit in the corresponding transmit descriptor, to cause the channel to be deleted from its current profile. The host must also append the channel to another profile.

RM cells passed to the ITC by the host will immediately be scheduled for transmission by the traffic manager.

4.5.3 Dump Channel

All cells received by the ITC which cannot be correctly processed on other channels are sent to the dump channel. Dump channel cells are transferred to host memory using the Receive Descriptor for physical channel two, which must be reserved for this purpose.

Cells in this channel will include those for which bits outside the CPC range in the cell header are set, cells within the CPC range but for which descriptors do not exist, and cells containing PTI fields equal to 7.

Dump channel data can be transferred to host memory in one of two formats, under mode register control :-

a) In cell transparent format

b) In cell header format, which consists of the 4 byte cell header only, excluding the HEC byte

4.6 Congestion Queue

A receive congestion queue exists in the local ram, which operates similarly to the local ram receive queue for payload data. The queue must be read by the host, to determine which channels have experienced congestion. The format is shown in Fig 14.

Entries are placed in the queue under two conditions :-

a) The state of the congestion bit changes, on CBR/VBR channels (priority 0, 1 or 2)

b) The EFCI bit is zero, on an ABR channel (priority 3)

Congestion on ABR channels can be handled automatically by the ITC, or else by the host. The congested ABR channel numbers can also be scheduled for transmission to the host, for information purposes, if this mechanism is enabled.

ITC Processed
On detecting the EFCI bit set to zero on an ABR channel, the ITC will set a status bit in the corresponding transmit descriptor. This will cause the ITC to automatically schedule an RM cell on the transmit channel. The RM cell payload will be copied from data contained in the local ram.

Host Processed
The host must generate an RM cell in cell transparent format, and send it to the ITC on physical channel one. It will be scheduled for immediate transmission by the traffic manager.

Congestion Queue Control
The queue consists of a 2 kilobyte circular buffer, and is controlled by two ITC registers. The LRCQS register points to the start of the queue, and the LRCQC counter gives the number of entries in the queue.

The LRCQS register is incremented automatically by the ITC, when the host reads items from the queue.

The LRCQC counter is incremented by the ITC when channel numbers are added to the queue, and decremented by the ITC when channel numbers are read from the queue by the host.

The queue must be located in local ram on a 2 KB boundary, using the LRCQB register.

Congestion Queue Interrupt
When entries are first placed in the congestion queue, an interrupt is generated for the host. The host must empty the queue before additional interrupts will be generated, which requires the host to check for additional entries (by reading the LRCQC), after reading the number of entries originally indicated by the LRCQC.

4.7 Statistics

Statistics for network management purposes are supported on 3 levels. These are the Physical layer, ATM layer and AAL5 layer, as follows :-

Physical Layer
- A count of the number of good command bytes received ie X_X or X_4, start of cell bytes
- A count of the number of bad command bytes received. This consists of 3 types of errors :-
  a) command bytes other than X_X, X_4 or X_8
  b) X_X or X_4 bytes within a cell
  c) any command byte skewed by a nibble, within a cell

ATM Layer
The following three counts (T, R, D) are required by the ATM Forum UNI 3.1 ILMI MIB :-

- The number of assigned ATM-layer cells transmitted (T)
- The number of assigned ATM-layer cells received and not dropped (R)

- The number of cells received and dropped (D), for any of the following reasons :-

  a) Uncorrectable cell header errors

  b) ATM-layer invalid cells ie physical layer cells

  c) ATM-layer cells with headers which the ITC cannot support

The following two counts are also supported :-

- The number of cells received with header errors detected (HED)
- The number of cells received with header errors corrected (HEC)

AAL5 Layer
The following conditions are detected on a per PDU basis. They can be read by the host on a per PDU basis, to maintain statistics on a per VCC basis.

- CRC error
- Length error
  The byte count does not match the length field contained in the PDU trailer
- Maximum length error
  The number of cells exceeds a user programmable value
- Abort
  The length field in the PDU trailer was set to zero
- Congestion
  PDU contains cells which have experienced congestion
- CLP1
  PDU contains cells which had the CLP bit set to 1
- Cells Lost
  PDU has lost at least one cell, due to lack of space in the local ram

A count of the total number of cells lost, due to lack of local ram space, will also be maintained on a per link basis.

4.7.1 Implementation

Statistics support is implemented by recording counts of events for the PHY and ATM levels, and setting status bits in PDU descriptors for the AAL5 level.

The counters are incremented when an event occurs, and reset to zero when read by the host. Each counter also contains an overflow bit.

A timer can be started when any counter is incremented from zero. All counters can be individually enabled to start the timer. When the timer interval expires, a maskable host interrupt can be generated.

The timer intervals can be varied as shown in Fig 15.

4.8 Loopback

Various loopback paths can be individually enabled within the ITC, as shown in Fig 16.

LR1
This is a loopback path between the receive path data input pin from the transceiver, and the transmit path data output pin to the transceiver.

LR2
This is a loopback path between the point at which receive path frame processing has been completed, and transmit path frame processing is about to start.

The functions performed on the receive data up to this loopback point are NRZI decoding, 4 bit/5 bit decoding, and descrambling using the equation $1+x^7+x^{10}$.

LR3
This is a loopback path between the point at which receive path cell processing has been completed, and transmit path cell processing is about to start.

The functions performed on the receive data up to this loopback point are payload descrambling using the equation $1+x^{43}$, and HEC checking.

LT1
This is a loopback path between the transmit path data output pin to the transceiver, and the receive path data input pin from the transceiver.

4.9 Transmit Test Patterns

The ITC can supply unscrambled, unencoded data to the transceiver transmit interface, for line test purposes.

The data pattern to be transmitted must be written to the TXTP register by the host. This data pattern is transmitted cyclically, from bit 0 to bit 7, when enabled under mode register control, as shown in Fig 16.

4.10 Plug & Play

The ITC has Plug & Play capability, which allows automatic configuration at power-on or reset. The ITC conforms to the Plug & Play ISA Specification version 1.08.

4.10.1 EEPROM Contents

The contents of the external EEPROM are copied into the local ram, during the P&P sequence. This allows fast read access to the data. Writes to the EEPROM are slower, as the data is written to the actual EEPROM.

The write mechanism is via the EEPROM register, defined in the I/O maps.

4.11 Initialisation

All control registers, base registers, pointers, descriptors, traffic profiles and profile lists must be initialised by the host after reset (ie after P&P has been completed), to configure the ITC for normal operation.

Control Registers
Control registers must be initialised as shown in Table 1.

Base Registers
Base registers must be initialised to address byte aligned buffer areas of the form 2^N. The areas must be sufficient to contain the byte requirements shown in Table 2.

The byte alignment requirements refer to the leading bytes within the buffer areas, starting at byte 0. The remaining bytes in the buffer areas are spare. Unused blocks, aligned on 64 byte boundaries within the spare areas, can be assigned to the Rx or Tx free lists.

Pointers
Pointers used to access receive physical channel descriptors must be initialised to contain the physical channel number, as shown in Table 3. All unused pointers (ie accessed by unconfigured ATM VCC's) must be initialised to the dump channel.

Descriptors
Receive descriptors must be initialised as shown in Table 4.

Transmit descriptors must be initialised as shown in Table 5.

Traffic management descriptors must be initialised as shown in Table 6.

Queues
Only the receive and congestion queue base registers need initialising by the host. The queue entries do not require initialisation.

Free Lists
The Rx and Tx free lists consist of byte aligned 64 byte blocks of local ram. The blocks must be initialised as shown in Table 7.

All unused 64 byte blocks of local ram, aligned on 64 byte boundaries, can be assigned to the free lists by the host. This can include spare blocks within other base register buffer areas, or within individual traffic management profile list areas.

Traffic Profiles
Traffic profile parameters must be initialised as shown in Table 8.

Profile Lists
Traffic profile lists must be initialised as shown in Table 9.

Channel numbers can only be assigned to a list from address locations 4 onwards. The list length and current list pointer entries must therefore be initialised to the value 3.

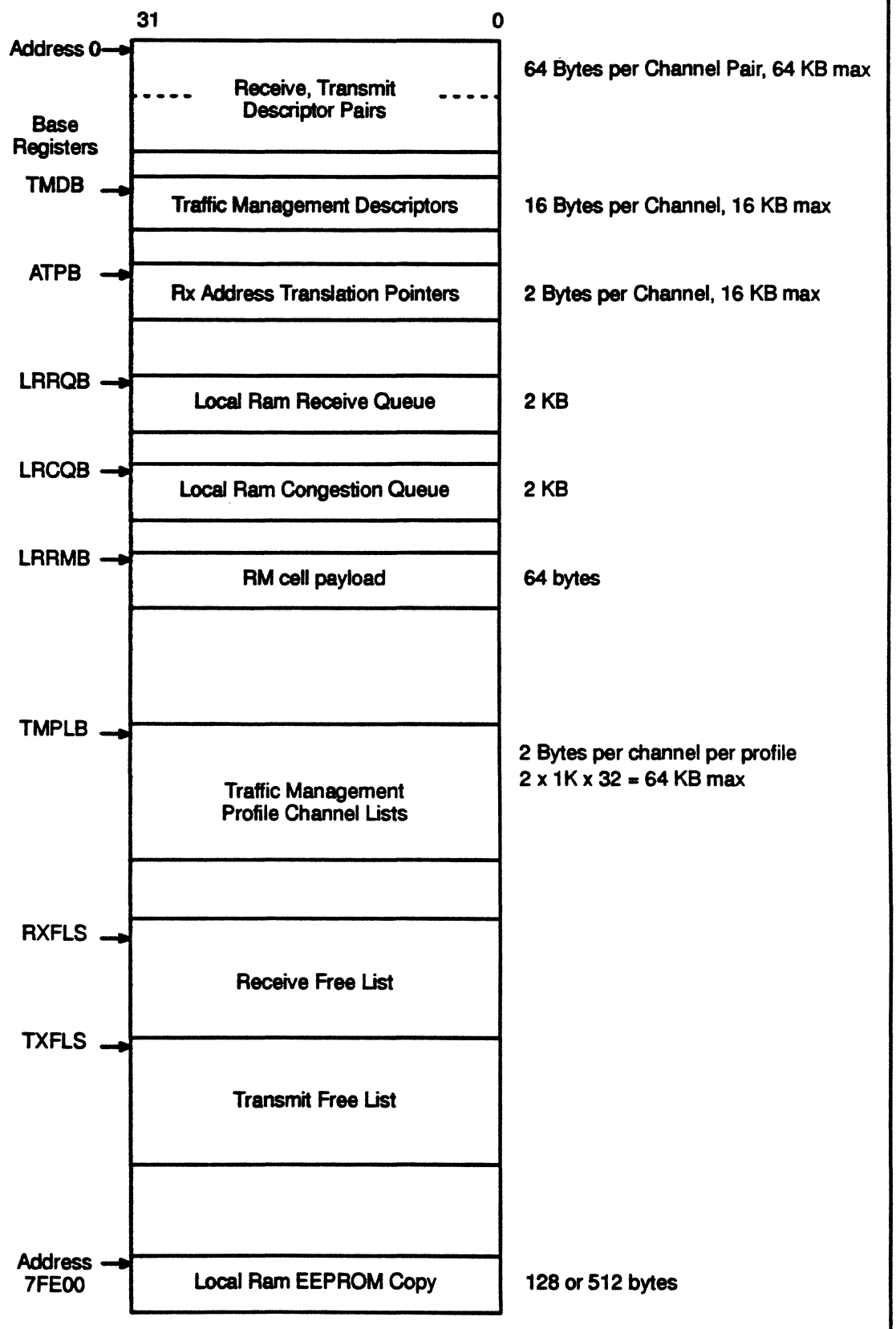


Fig 6 – Local Ram Symbolic Organisation

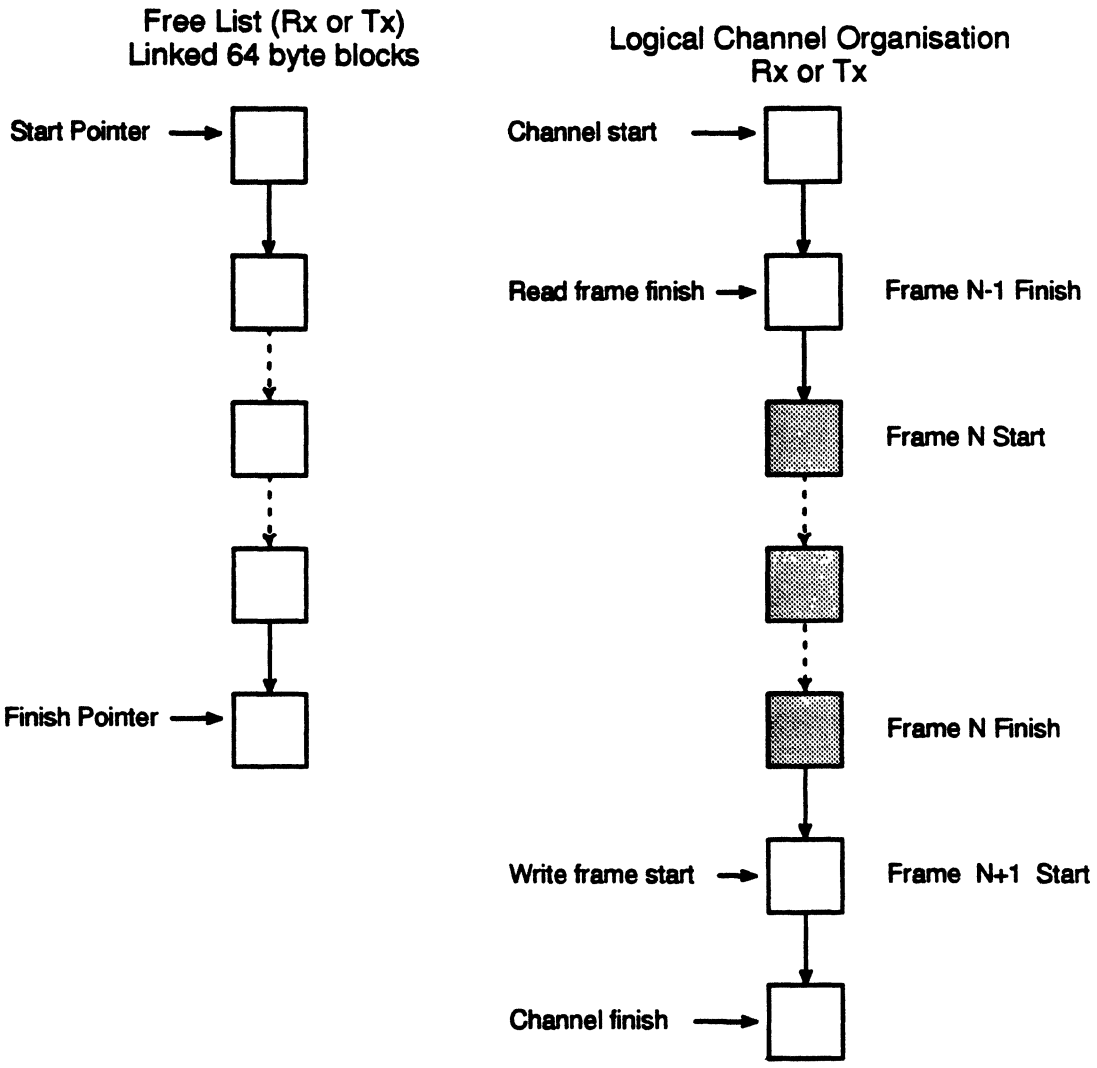


Fig 7 – Local Ram Logical Channel Organisation

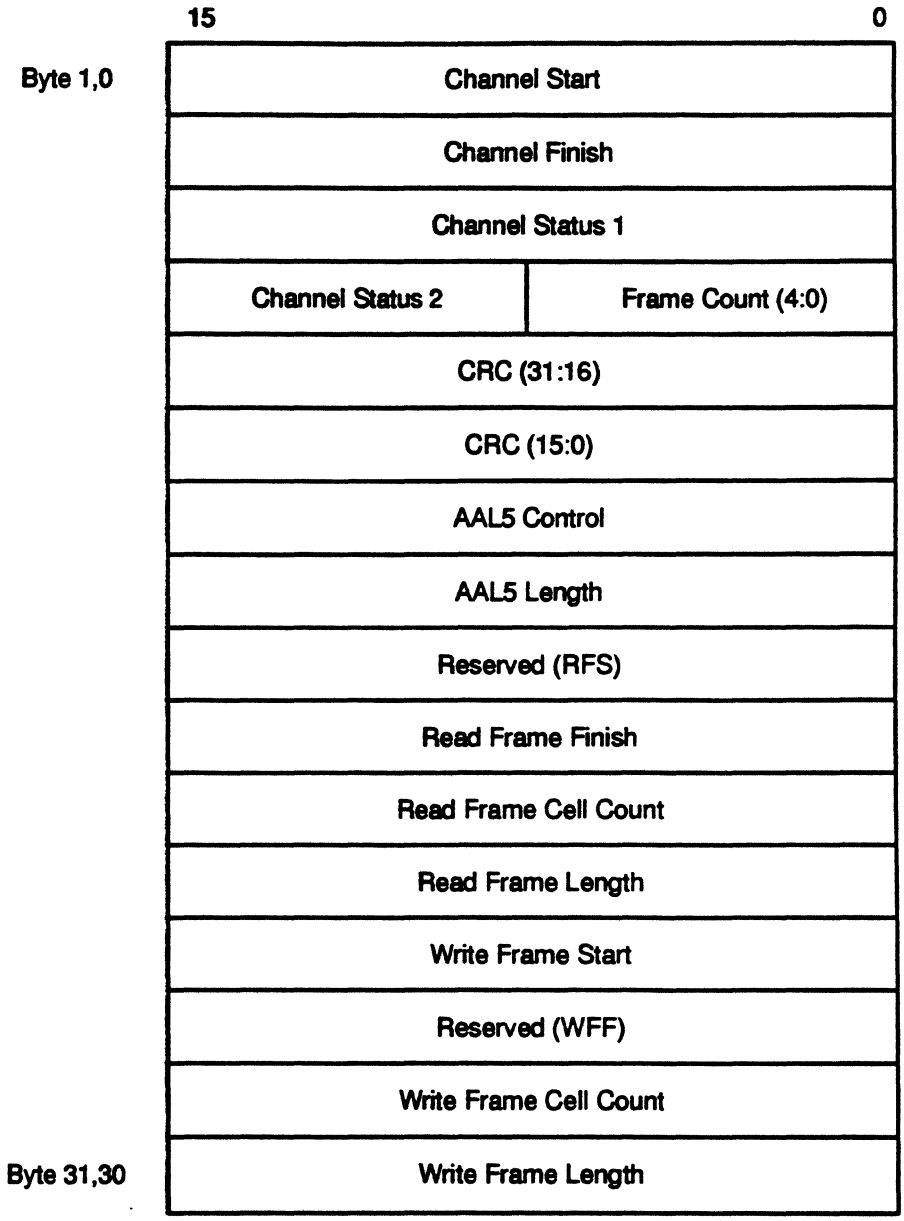


Fig 8 – Receive Local Ram Descriptor Format

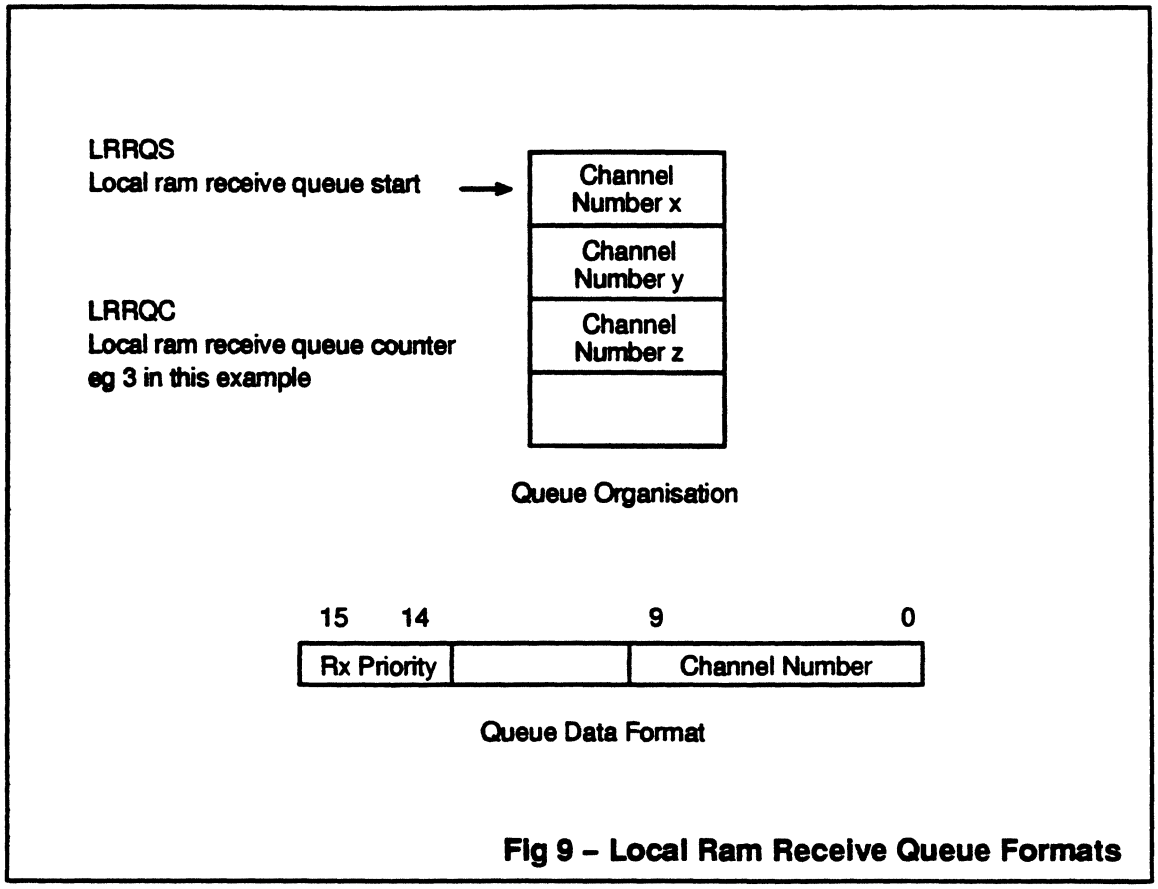


Fig 9 – Local Ram Receive Queue Formats

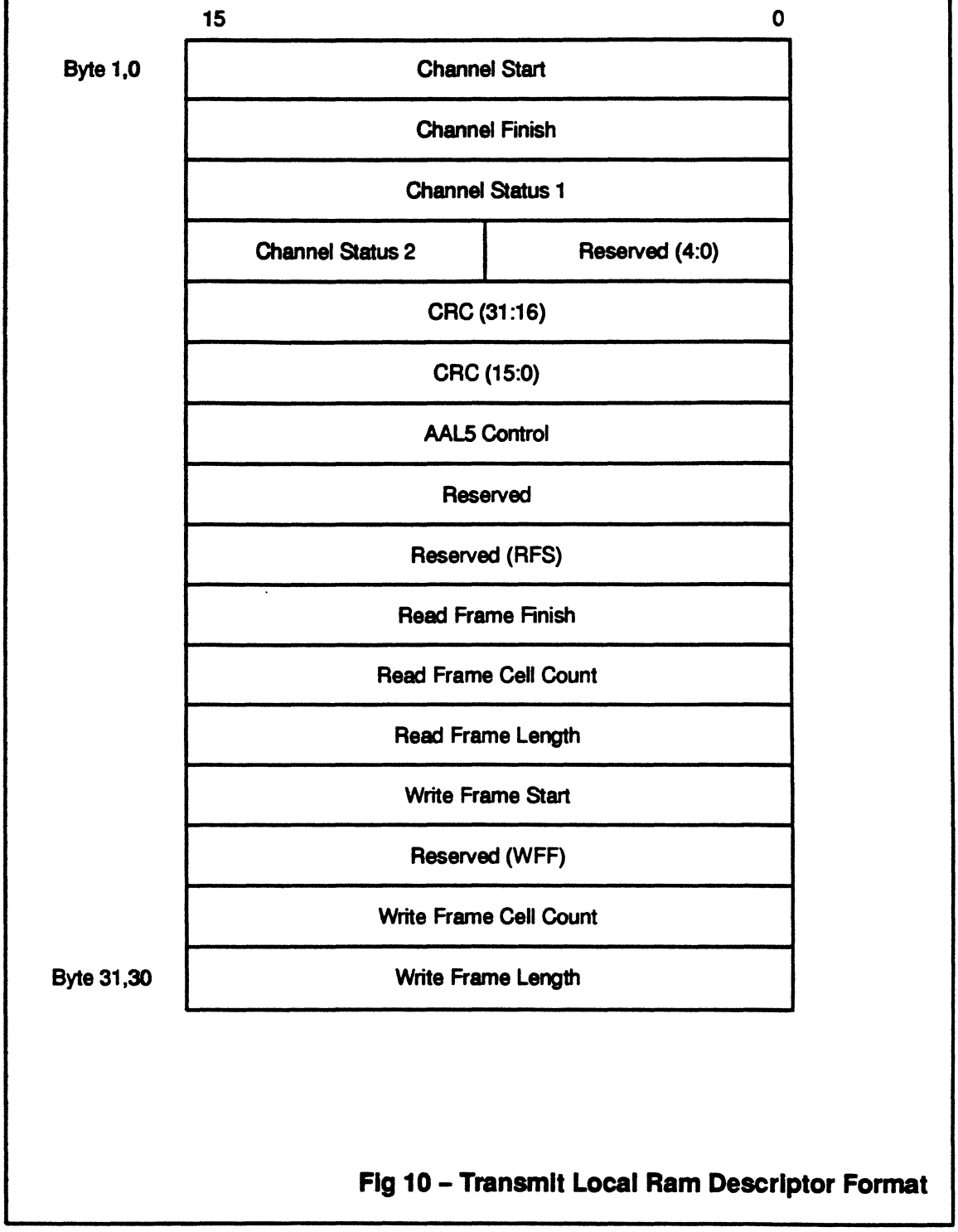
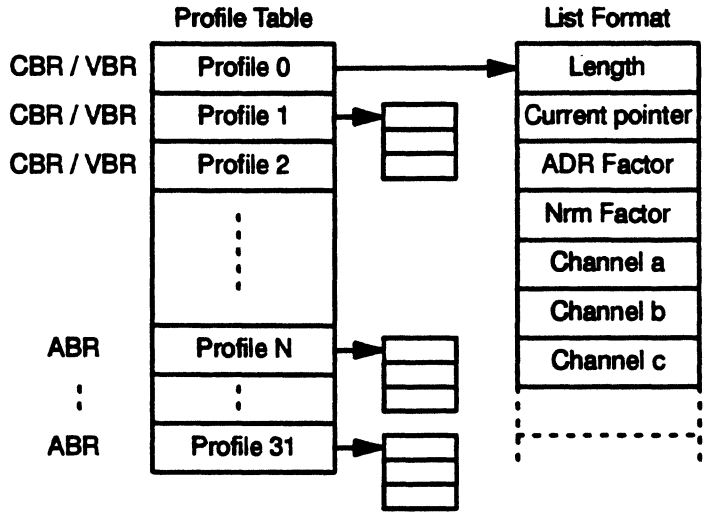


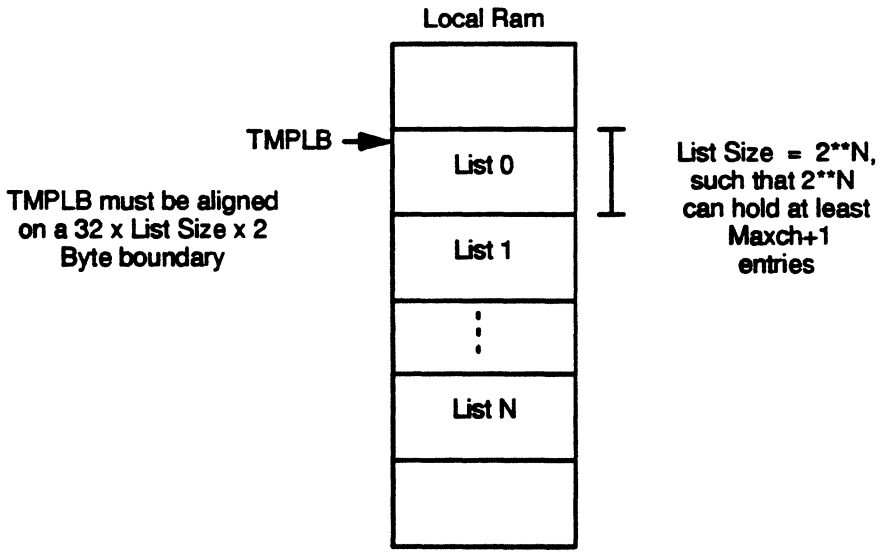
Fig 10 – Transmit Local Ram Descriptor Format



Profile Table and List Organisation

ADR Factor.
This is the amount by which the ADR Count is decremented

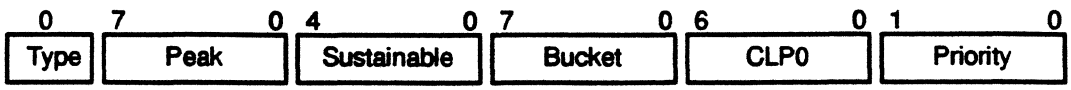
Nrm Factor
This is the amount by which the Nrm Count is decremented



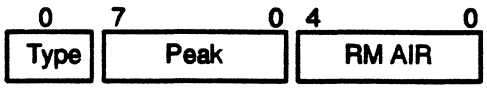
TM Local Ram Organisation

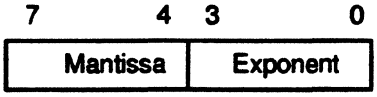
Fig 11 – Profile Tables and Lists Organisation

CBR / VBR Profile Parameters



ABR Profile Parameters





Peak Rate Counter

Exponent	Time Interval	Exponent	Time Interval
1	2 µs	A	1 ms
2	4	B	2
3	8	C	4
4	16	D	8
5	32	E	16
6	64	F	32
7	128		
8	256		
9	512		

Exponent = 0 is an inactive profile

Fig 12 - Profile Parameters

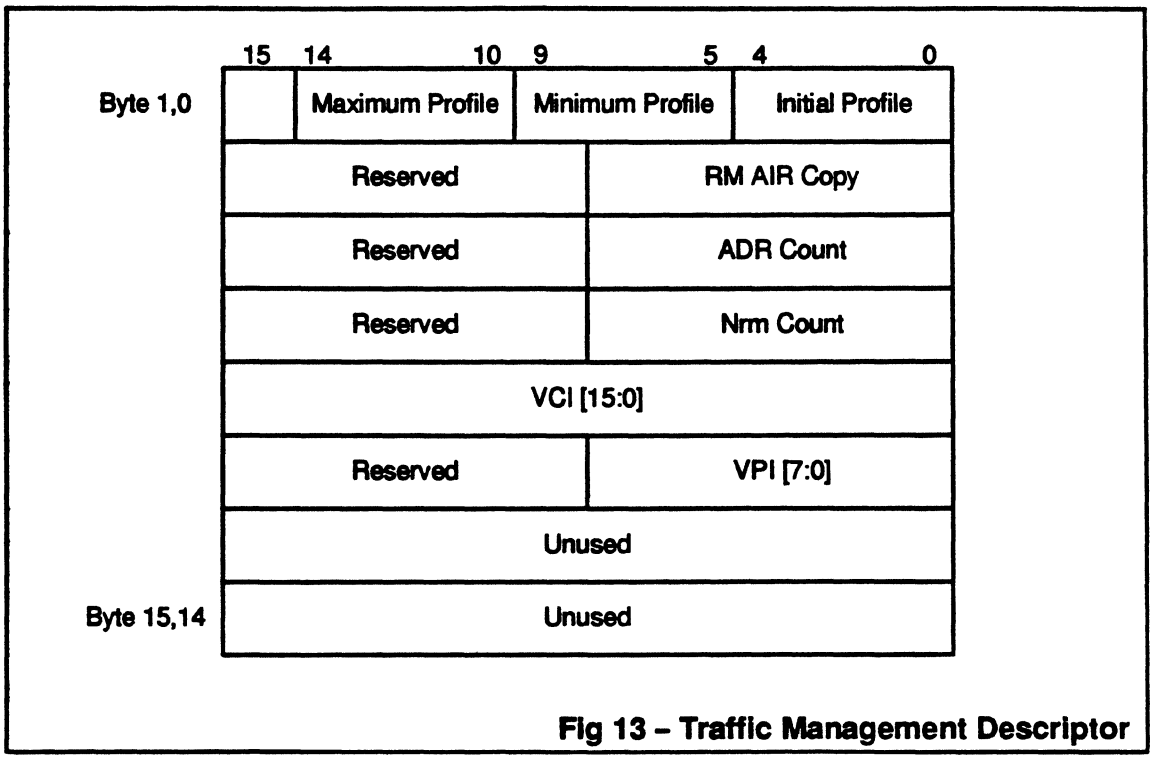


Fig 13 - Traffic Management Descriptor

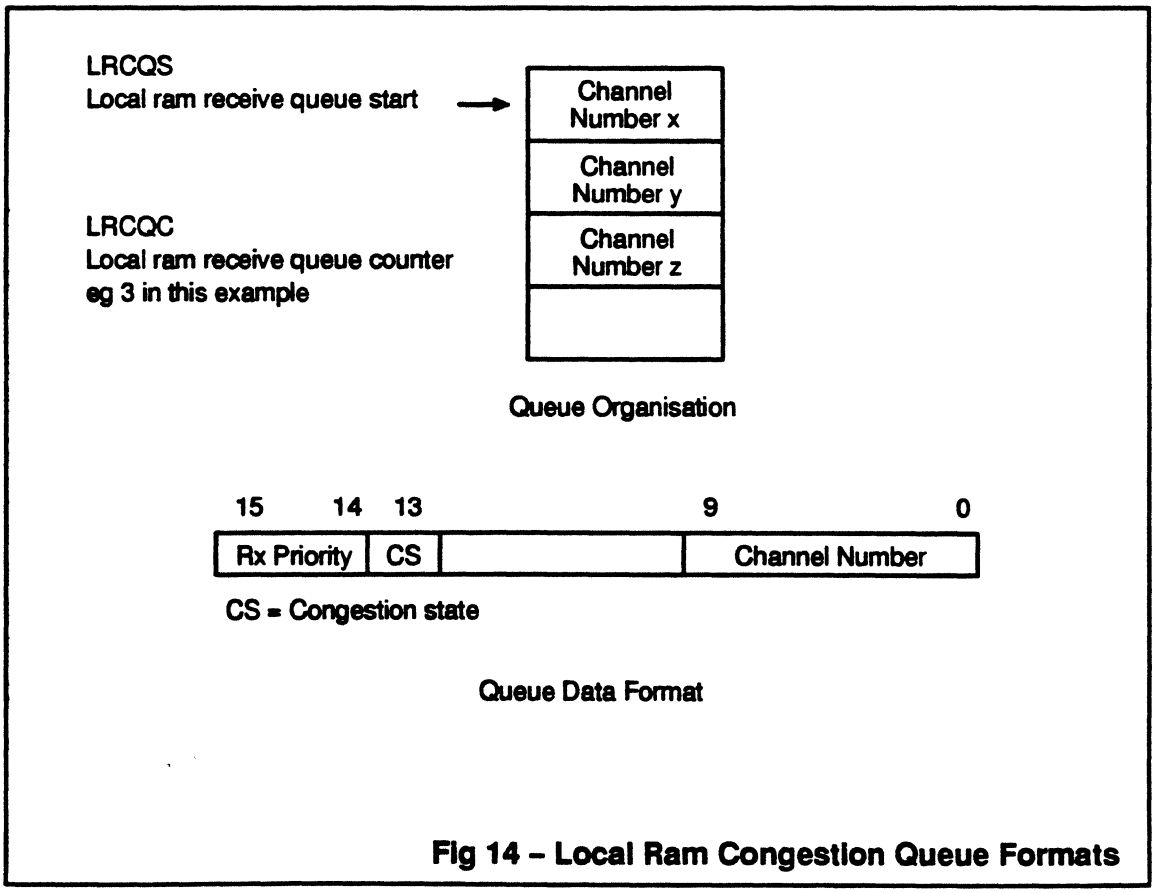
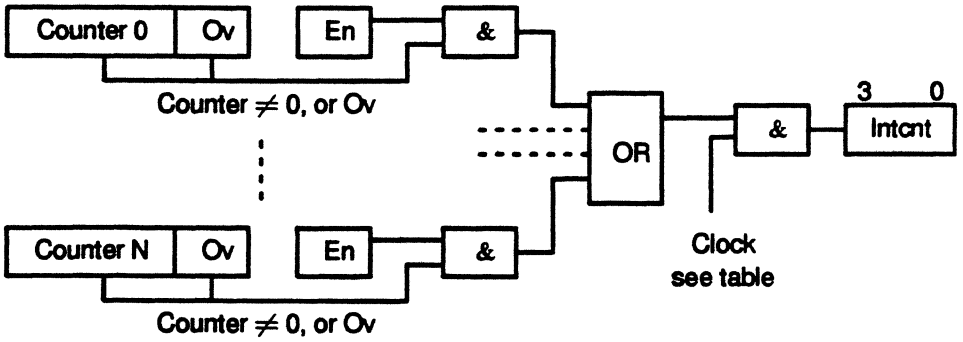


Fig 14 - Local Ram Congestion Queue Formats



ICLK	Clock µs	Intcnt ms
0	32	0.5
1	64	1
2	128	2
3	256	4
4	512	8
5	1024	16
6	2048	32
7	4096	64

Fig 15 – Statistics

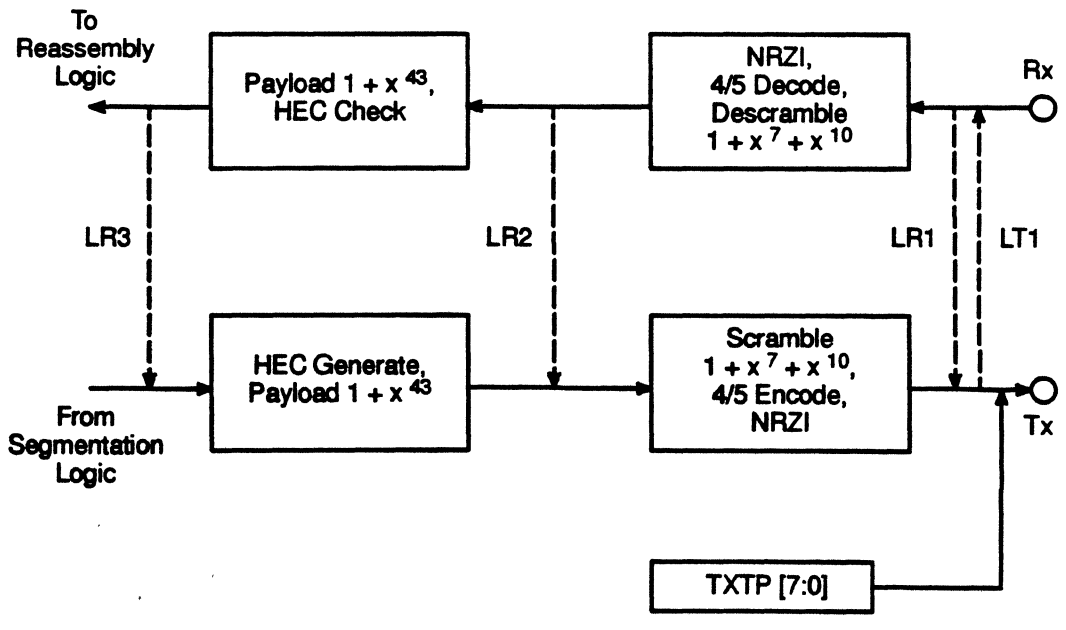


Fig 16 – Loopback Paths

Register Name	Initial Value	Register Function
CPC Size	0 - 6	Select Concatenated VPI / VCI fields, to address pointers. Number of pointers = 2**(CPC Size + 7).
VPI Size	0 - 3	Select VPI field for receive address translation
Maxch	31 - 1023	Maximum number of physical channels supported ie up to Maxch+1 descriptors, including reserved channels
RXFLS	Host	Receive free list start address Register x 2^6 gives local ram byte 0 address of block
RXFLF	Host	Receive free list finish address
RXFLC	Host	Count of 64 byte blocks in receive free list
TXFLS	Host	Transmit free list start address Register x 2^6 gives local ram byte 0 address of block
TXFLF	Host	Transmit free list finish address
TXFLC	Host	Count of 64 byte blocks in transmit free list

Table 1 - Control register initialisation

Register Name	Byte Alignment Requirements	Register Function
TMDB	(Maxch+1) x 16	Traffic management descriptor base
ATPB	2**(CPC Size + 8)	Address translation pointers base
LRRQB	2k	Local ram receive queue base
LRCQB	2k	Local ram congestion queue base
LRRMB	64	RM cell payload data
TMPLB	(Maxch+1) x 64	Traffic management profile lists base
Note :- Local ram channel descriptors require (Maxch+1) x 64 bytes, starting at local ram byte address 0.		

Table 2 - Base register initialisation

Pointers	Initialisation [15:0]	Pointer Function
Used	[15:10] = 0, [9:0] = Phy	Phy = Physical channel number
Unused	[15:10] = 0, [9:0] = Dump	Dump = Dump channel number

Table 3 - Address translation pointer initialisation

Bytes	Initialisation [15:0]	Descriptor Function
3:0	X	
5:4	CP11 0000 0100 0000	Channel status 1 C = Cell transparent P = Payload transparent
7:6	0000 000T TPP0 0000	Channel status 2, Frame count TT = Threshold [1:0] PP = Priority [1:0]
9:8	1111 1111 1111 1111	CRC [31:16]
11:10	1111 1111 1111 1111	CRC [15:0]
31:12	X	

Table 4 – Rx descriptor initialisation

Bytes	Initialisation [15:0]	Descriptor Function
3:0	X	
5:4	CP11 0000 0100 0000	Channel status 1 C = Cell transparent P = Payload transparent
7:6	0	Channel status 2 [15:5], Unused [4:0]
9:8	1111 1111 1111 1111	CRC [31:16]
11:10	1111 1111 1111 1111	CRC [15:0]
13:12	Host	AAL5 control
31:14	X	

Table 5 – Tx descriptor initialisation

Bytes	Initialisation [15:0]	Descriptor Function
1:0	0, Max[4:0], Min[4:0], In[4:0]	Max = Maximum profile, Min = Minimum profile, In = Initial profile
3:2	X	
5:4	[15:8] = X, Host	ADR count
7:6	[15:8] = X, Host	Nrm count
9:8	Host	ATM cell header VCI [15:0]
11:10	[15:8] = 0, Host	ATM cell header VPI [7:0]
15:12	X	

Table 6 – Traffic Management descriptor initialisation

Bytes	Initialisation [15:0]	Pointer Function
1:0	X	
3:2	Next block pointer	Pointer x 2^6 gives local ram byte 0 address of next block in free list
63:4	X	

Table 7 – Rx, Tx free list blocks initialisation

Parameter	Initialisation	Function
Type	0 or 1	0 = CBR / VBR 1 = ABR
Peak	Mantissa = 1 to 15 Exponent = 0 to 15	Interval counter, N down to 0 Select timer interval
Sustainable	0 to 31	Fractional bucket tokens (N ÷ 32) 0 = always add token to bucket
Bucket	0 to 255	0 = empty
CLP0	0 to 127	Ratio of CLP0 to CLP1 cells 7E = always CLP0 7F = always CLP1
Priority	0 to 3	0 = lowest
RM AIR	0 to 31	Profile to move to on receiving an RM cell

Table 8 – Profile initialisation

Bytes	Initialisation [N:0]	Function
1:0	3	Length of list (ie zero channels in list)
3:2	3	Current active entry
5:4	ADR factor	ADR count decrement amount
7:6	Nrm factor	Nrm count decrement amount
End:8	X	Channel numbers

Table 9 – Profile lists initialisation

5. I/O PORT MAP OPERATION

The host can access the ITC through a 16 byte I/O port map. The block of 16 consecutive byte addresses must be aligned on any 16 byte boundary in the 64k I/O space. In the ISA configuration the ITC will decode all 16 bits of the I/O address. In the PCMCIA configuration, the host PCMCIA controller handles the I/O decode.

The ITC channel data registers can also be accessed via an 8KB address map. This area can be aligned on any 8k boundary in the range C0000h to DE000h.

5.1 I/O Register Mapping

ITC registers will be accessible in different maps, each map having a particular layout. The first 2 bytes in all maps have the same common format. This consists of a 6 bit command register, and a 10 bit parameter register.

All codes and register maps are as defined in the following tables.

Command Code	Command Function
0	Null Command
1	Access common ITC registers
3:2	Reserved
4	Receive channel information, channel specified by Parameter
5	Purge receive frame, channel specified by Parameter, no I/O map available
6	Purge receive channel, channel specified by Parameter, no I/O map available
7	Reserved
8	Transmit channel information, channel specified by Parameter
9	End of frame, channel specified by Parameter, no I/O map available
B:A	Reserved
C	Profile information, profile specified by Parameter
F:D	Reserved
10	Local ram literal address access, with automatic 2^N address increment
13:11	Reserved
14	Control registers
15	Free lists information
16	Base registers
17	Physical interface
18	Statistics
19	Statistics
1A	tbd
3F	ITC busy ie unable to accept further host commands This value is returned if the host reads the command code register, while the ITC is processing an existing command.

Table 10 – I/O port map command codes

Byte	Bits 15:8	Bits 7:0	Command register function	I/O
1:0	C = 1, P = XX XXXX XXXS Write to S sets Status 13		Access Common ITC registers	R/W
3:2	Status		ITC status register	R
5:4	Mask		ITC mask register	W
7:6	LRRQC		Entries in receive queue	R
9:8	LRCQC		Entries in congestion queue	R
11:10	RXFLC		Cells available in receive free list	R
13:12	TXFLC		Cells available in transmit free list	R
15:14				

Status bits	Meaning
0	Data exists in Rx queue
1	Rx queue full
2	Data exists in Congestion queue, for CBR/VBR channels
3	Data exists in Congestion queue, for ABR channels
4	Congestion queue full
5	RM cells have been received
6	Data exists in OAM channel
7	Data exists in Dump channel
8	Rx free list is below threshold
9	Rx free list is zero, and cells have been lost
10	Tx free list is below threshold
11	Statistics information exists
12	Loss of REDY signal on transceiver interface
13	Software interrupt, caused by writing to Parameter 0
14	GFC halt received
15	ABR credit counter is zero

Table 11 – I/O port map

Byte	Bits 15:8	Bits 7:0	Command register function	I/O
1:0	C = 4, P = Rx channel		Receive channel information	R/W
3:2	Rxsts		Channel status	R
5:4	Rxlen		Bytes available	R
7:6	Rxfc		Frames available	R
9:8	Control		AAL5 control word	R
11:10				
13:12	Data 0		Receive data	R
15:14	Data 1		Receive data	R

Rxsts bits	Meaning
0	Frame completed
1	CRC error
2	Frame aborted
3	Frame length error
4	Frame exceeded maximum length register value
5	Channel empty
6	Congestion experienced (CBR/VBR channel)
7	CLP1 cell received
8	Cells lost
9	Physical interface error
10	
11	
12	
13	
14	
15	

Table 12 – I/O port map

Byte	Bits 15:8	Bits 7:0	Command register function	I/O
1:0	C = 8, P = Tx channel		Transmit channel information	R/W
3:2	Txsts		Channel status	R
5:4	Txflc		Blocks available in transmit free list	R
7:6	Mode AP see bitmap		0 Abort frame 1 Delete channel from profile list 2 Append channel to profile [12:8] 12:8 Profile number (bit 2 only)	W
9:8				
11:10				
13:12	Data 0		Transmit data	W
15:14	Data 1		Transmit data	W

Txsts bits	Meaning
0	Frame completed
1	RM cell received
2	EFCI = 0 sent
3	EFCI = 0 received
4	Maximum length error
5	Channel is on a profile list
6	Channel empty
7	
8	
9	
10	
11	
12	
13	
14	
15	

Table 13 – I/O port map

Byte	Bits 15:8	Bits 7:0	Command register function	I/O
1:0	C = C, P = Profile number		Profile information	R/W
3:2	Type		Type	W
5:4	Peak		Peak	W
7:6	Sustainable		Sustainable	W
9:8	Bucket		Bucket	W
11:10	CLP0		CLP0	W
13:12	Priority		Priority	W
15:14	RM AIR		RM AIR	W

Table 14 – I/O port map

Byte	Bits 15:8	Bits 7:0	Command register function	I/O
1:0	C = 10, P = 1 to 6 (2^P)		Local ram direct access	R/W
3:2	Add 18:16		Literal ram address bits 18:16	R/W
5:4	Add 15:1, bit 0 = 0		Literal ram address bits 15:0	R/W
7:6				
9:8				
11:10				
13:12	Data 0		Data	R/W
15:14	Data 1		Data	R/W

Parameter value

The parameter value specifies the literal ram address increment, in the form 2^P, when data is read or written to the data 0 or data 1 locations.

eg P = 1, increment address by 2
P = 6, increment address by 64

Table 15 – I/O port map

Byte	Bits 15:8	Bits 7:0	Command register function	I/O
1:0	C = 14, P = X		Control registers	R/W
3:2	VPI Size	CPC Size	ATM address translation fields	W
5:4	Maxch		Maximum physical channels supported	W
7:6				
9:8	Mode HER see bitmap		0 Read header only for unmapped cells 1 ITC to generate RM cells (EFCI = 0 received) 2 ITC to enter EFCI = 0 in congestion queue 3 ITC to process RM cells (increase channel ACR) 4 ITC to send RM cell to host	W
11:10		RXFT1	Receive frame threshold register 1	W
13:12		RXFT2	Receive frame threshold register 2	W
15:14	RXMFL		Receive maximum frame length	W

Table 16 – I/O port map

Byte	Bits 15:8	Bits 7:0	Command register function	I/O
1:0	C = 15, P = X		Free lists information	R/W
3:2	RXFLS		Receive free list start address	W
5:4	RXFLF		Receive free list finish address	W
7:6	RXFLC		Receive free list block count	W
9:8	TXFLS		Transmit free list start address	W
11:10	TXFLF		Transmit free list finish address	W
13:12	TXFLC		Transmit free list block count	W
15:14	RXFLT	TXFLT	Threshold values for free lists	W

Table 17 – I/O port map

Byte	Bits 15:8	Bits 7:0	Command register function	I/O
1:0	C = 16, P = X		Base registers	R/W
3:2	TMDB		Traffic management descriptor base	W
5:4	ATPB		Address translation pointers base	W
7:6	LRRQB		Local ram receive queue base	W
9:8	LRCQB		Local ram congestion queue base	W
11:10	LRRMB		RM cell payload data base	W
13:12	TMPLB		Traffic management profile lists base	W
15:14				

Table 18 – I/O port map

Byte	Bits 15:8	Bits 7:0	Command register function	I/O
1:0	C = 17, P = X		Physical interface	R/W
3:2	RX Framer see bitmap		1 Decoder 5/4 bypass, use 4 lsb's 2 Descrambler bypass $1+x^7+x^{10}$ 3 NRZI bypass 5:4 TXCTL[2:1]	R/W
5:4	Rx Cell Receiver see bitmap		1:0 = 01, Descrambler $1+x^{43}$ enabled, 2= 0, No mask = 1, HEC mask 01010101 3= 0, HEC detect = 1, HEC detect and correct	R/W
7:6	Rx Physical Layer see bitmap		0 FRAQ, ITC using recovered clock 1 XREDY,Transceiver rx data valid 2 Loopback, use recovered clock 3 LSU mode, look for X_(LSU_CVAL) command byte for link startup 7:4 LSU_CVAL, link startup byte 8 Link up, ITC ready to use link	R/W R R/W R/W R/W R/W
9:8	TX Framer see bitmap		0 Encoder 4/5 bypass, pass 1,nibble 1 Scrambler bypass $1+x^7+x^{10}$ 2 NRZI bypass	R/W
11:10	Tx Cell Transmitter see bitmap		1:0 = 01, Scrambler $1+x^{43}$ enabled, 2= 0, No mask = 1, HEC mask 01010101 3 Cell stuff, insert idle cells when no data exists	R/W
13:12	TXTP		Tx test pattern register	R/W
15:14	Loopback see bitmap		0 LR3 1 LR2 2 LR1 3 LT1 4 TXTP	R/W

Table 19 – I/O port map

1:0	C = 18, P = X	Statistics	R/W
3:2	T	Transmitted cells	R
5:4	R	Received cells	R
7:6	D1	Dropped 1	R
9:8	D2	Dropped 2	R
11:10	D3	Dropped 3	R
13:12	HED	Header errors detected	R
15:14	HEC	Header errors corrected	R

Table 20 – I/O port map

Byte	Bits 15:8	Bits 7:0	Command register function	I/O
1:0	C = 19, P = X		Statistics	R/W
3:2	VPHY		Valid physical command bytes	R
5:4	IPHY		Invalid physical command bytes	R
7:6				W
9:8				W
11:10				W
12:13				W
15:14	Statistics enables see bitmap		0 T 1 R 2 D1 3 D2 4 D3 5 HED 6 HEC 7 VPHY 8 IPHY 15:13 Intcnt clock	W

Table 21 – I/O port map

Byte	Bits 15:8	Bits 7:0	Command register function	I/O
1:0	C = 1A, P = X		to be defined later (tbd)	R/W
3:2	Select register			W
5:4	RPL control			W
7:6	RPL page			W
9:8	EEPROM register			W
11:10	Reset			W
12:13	Memory map			W
15:14	ID register			W

Table 22 – I/O port map

Byte	Bits 15:8	Bits 7:0	Command register function	I/O
1:0	C = 1?, P = X		Register initialisation	R/W
3:2				W
5:4				W
7:6				W
9:8				W
11:10				W
12:13				W
15:14				W

Table 23 – I/O port map

Byte	Bits 15:8	Bits 7:0	Command register function	I/O
1:0	C = 1?, P = X		Register initialisation	R/W
3:2				W
5:4				W
7:6				W
9:8				W
11:10				W
12:13				W
15:14				W

Table 24 – I/O port map

6. REGISTER MAP

Register Name	Register Function
CPC Size	Select Concatenated VPI / VCI fields, to address pointers. Number of pointers = 2**(CPC Size + 7).
VPI Size	Select VPI field for receive address translation
Maxch	Maximum number of physical channels supported ie up to Maxch+1 descriptors
RXFLS	Receive free list start address Local ram address of byte 0 of first 64 byte block in receive free list
RXFLF	Receive free list finish address
RXFLC	Count of 64 byte cells in receive free list
TXFLS	Transmit free list start address Local ram address of byte 0 of first 64 byte block in receive free list
TXFLF	Transmit free list finish address
TXFLC	Count of 64 byte cells in transmit free list