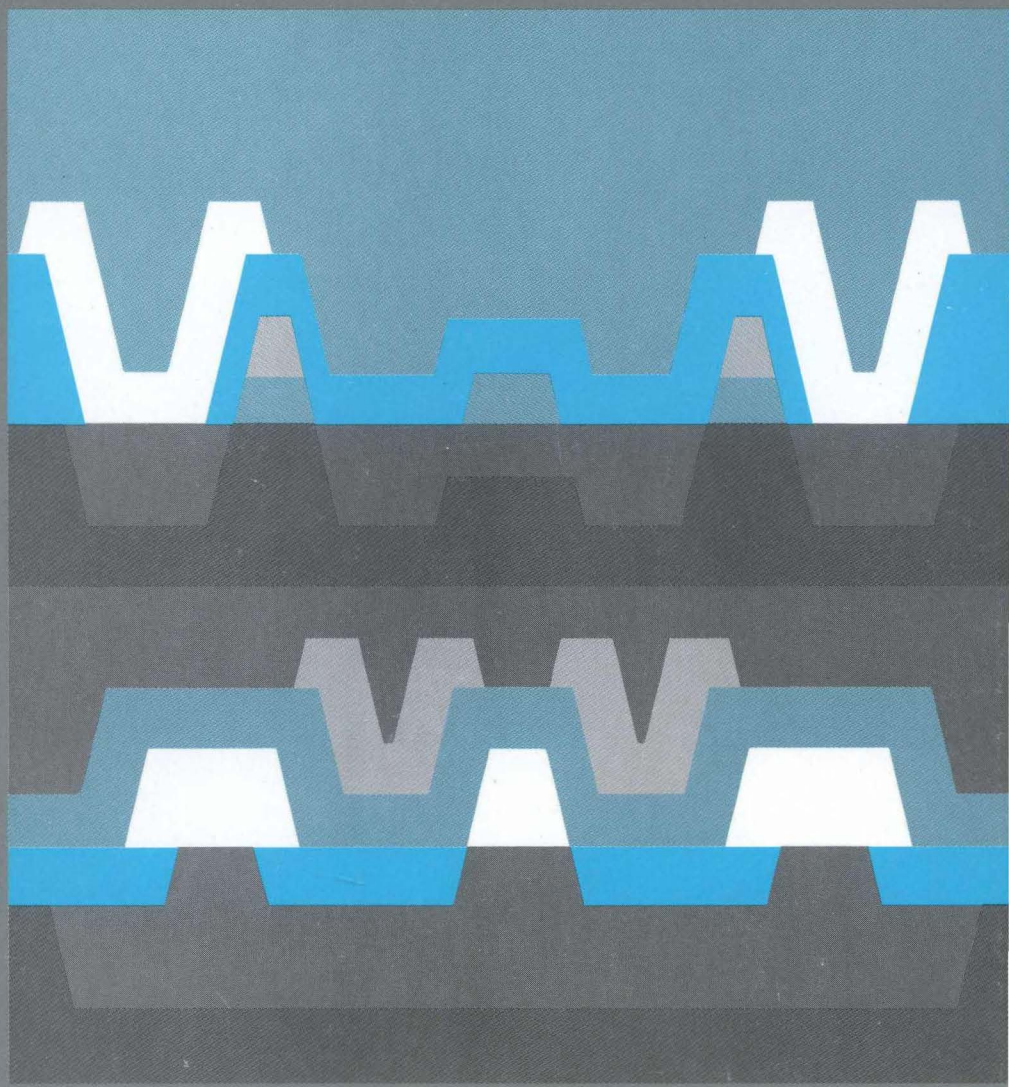
HITACHI®

NONVOLATILE MEMORY DATA BOOK

HITACHI®

NONVOLATILE MEMORY DATA BOOK



Nonvolatile Memory Data Book

When using this document, keep the following in mind:

1. This document may, wholly or partially, be subject to change without notice.

2. All rights are reserved: No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without Hitachi's permission.

3. Hitachi will not be held responsible for any damage to the user that may result from accidents or any other reasons during operation of the user's unit according to this document.

4. Circuitry and other examples described herein are meant to indicate the characteristics and performance of Hitachi's semiconductor products. Hitachi assumes no responsibility for any intellectual property claims or other problems that may result from applications based on the examples described herein.

5. No license is granted by implication or otherwise under any patents or other rights of any third party or Hitachi, Ltd.

6. MEDICAL APPLICATIONS: Hitachi's products are not authorized for use in MEDICAL APPLICATIONS without the written consent of the appropriate officer of Hitachi's sales company. Such use includes, but is not limited to, use in life support systems. Buyers of Hitachi's products are requested to notify the relevant Hitachi sales offices when planning to use products in MEDICAL APPLICATIONS.

 Printed in U.S.A.

HITACHI

Hitachi America, Ltd. • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

Nonvolatile Memory Data Book

HITACHI

Hitachi America, Ltd. • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

Nonvolatile Memory Data Book
Table of Contents

SECTION 1
Introduction

SECTION 2
Flash Memory

SECTION 3
Mask ROM

Nonvolatile Memory Data Book
Table of Contents *(Continued)*

SECTION 3 (continued)
Mask ROM

SECTION 4
EPROM (UV Erasable and OTP)

SECTION 5
EEPROM

Nonvolatile Memory Data Book

ALPHA-NUMERIC INDEX

Introduction

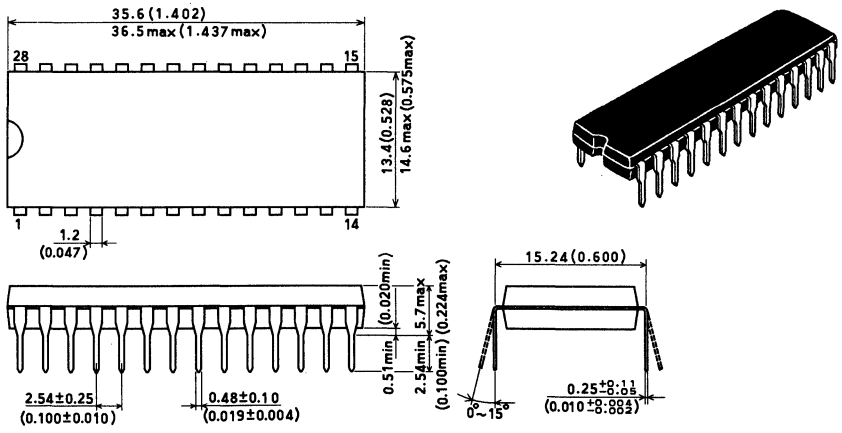
SECTION 1
Introduction

Package Information

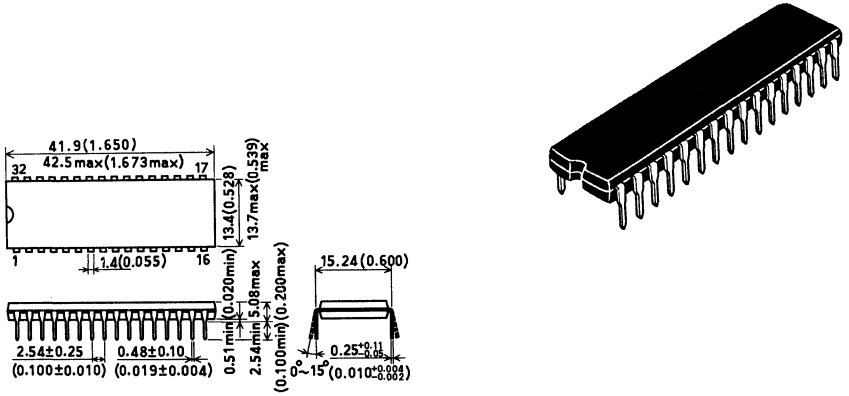
Package Information

- **Plastic Dual In-Line Package (PDIP)** **Unit: mm**

- **DP-28**

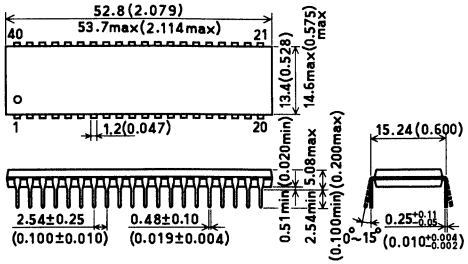


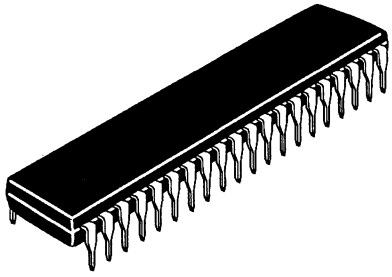
- **DP-32**



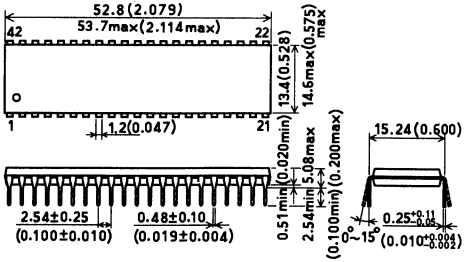
- **Plastic Dual In-Line Package (PDIP) - continued** **Unit: mm**

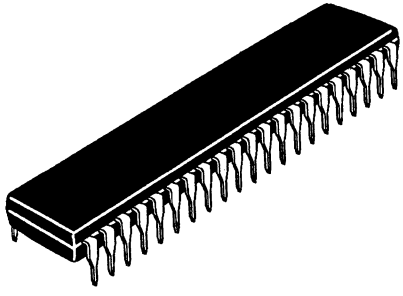
- **DP-40**





- **DP-42**

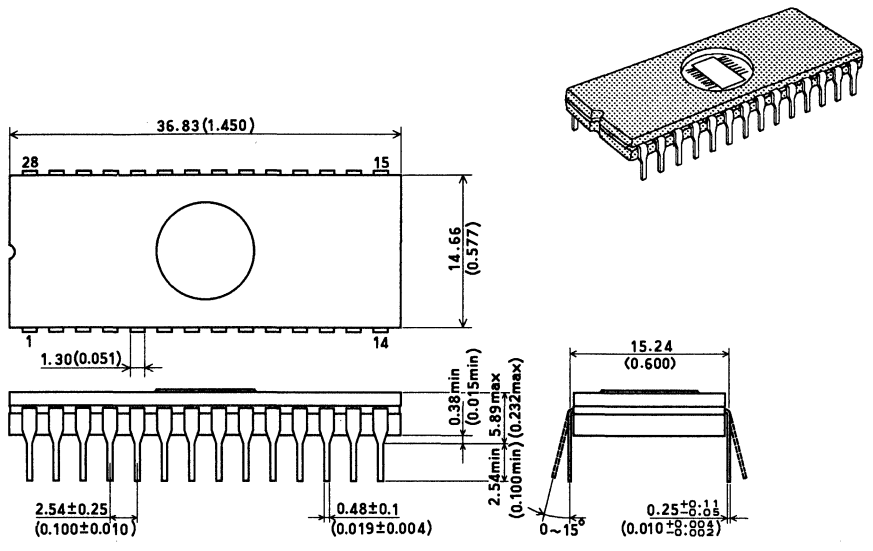




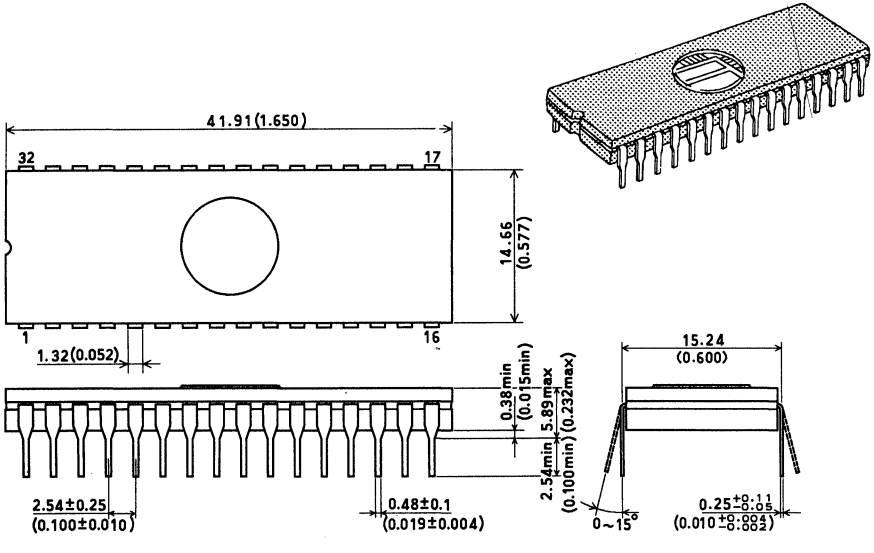
Package Information

- **Ceramic Dual In-Line Package (CerDIP)** **Unit: mm**

- **DG-28**

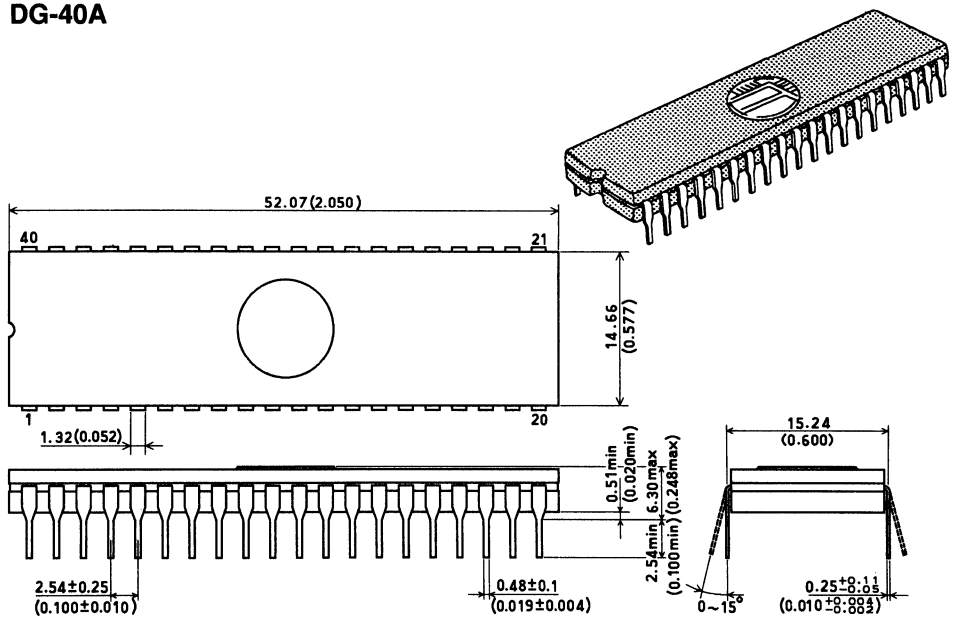


- **DG-32**



- **Ceramic Dual In-Line Package (CerDIP) - continued** **Unit: mm**

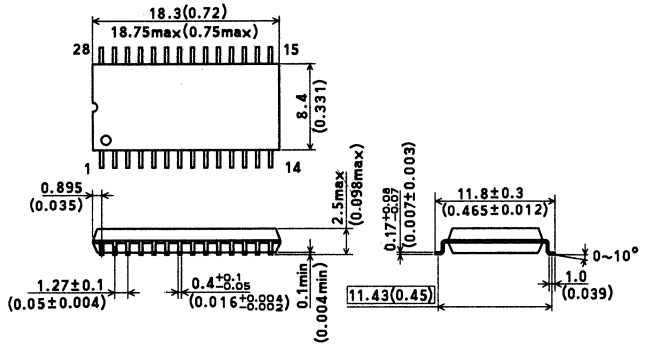
- **DG-40A**

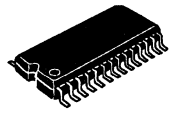


• Plastic Small Outline Package (SOP)

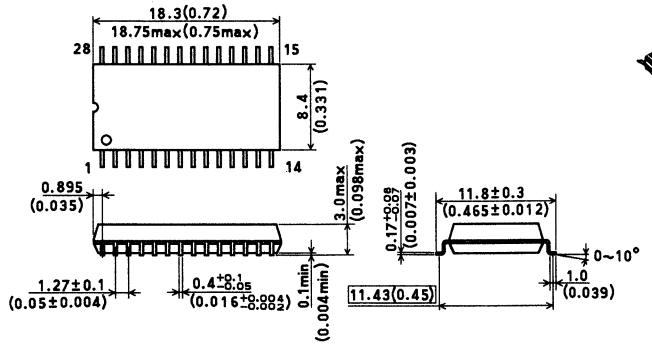
Unit: mm

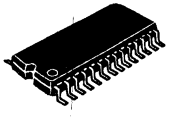
• FP-28DA





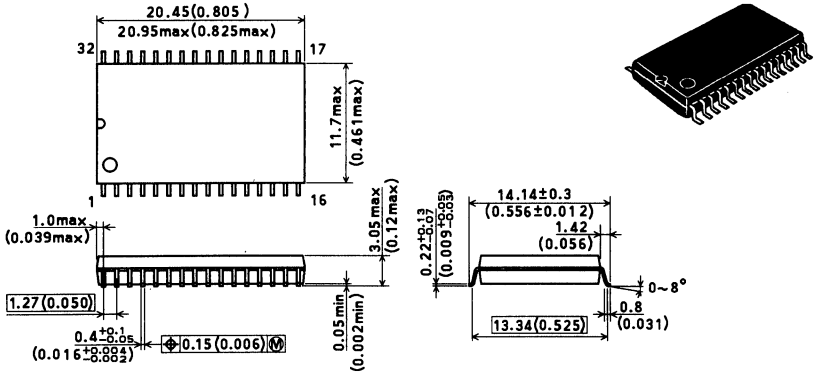
• FP-28D



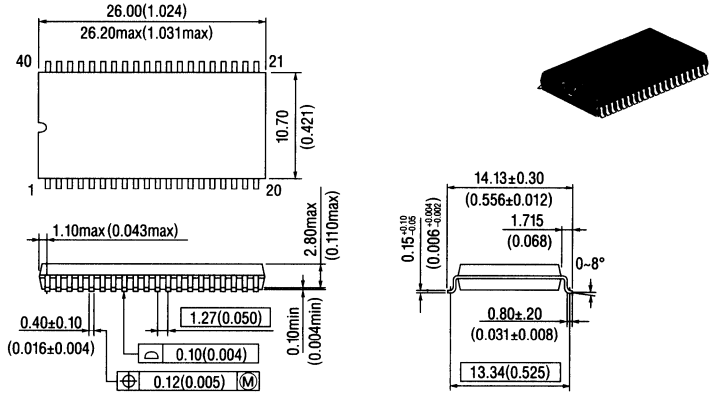


- **Plastic Small Outline Package (SOP) - continued** **Unit: mm**

- **FP-32D**



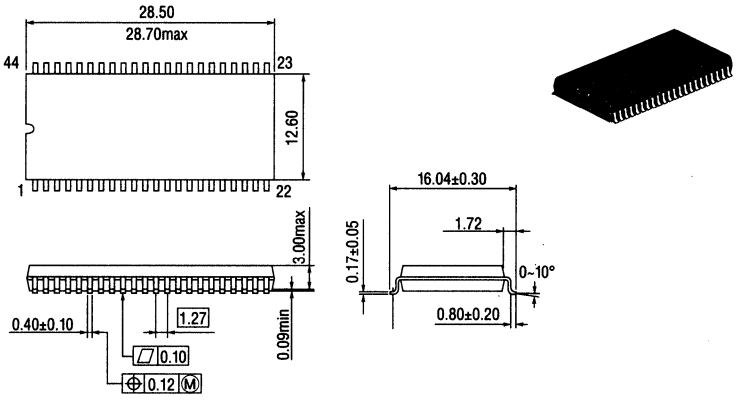
- **FP-40D**



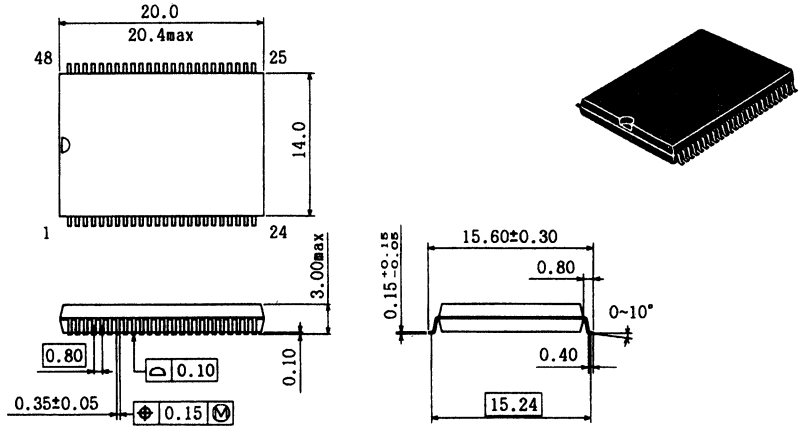
• Plastic Small Outline Package (SOP) - continued

Unit: mm

• FP-44D



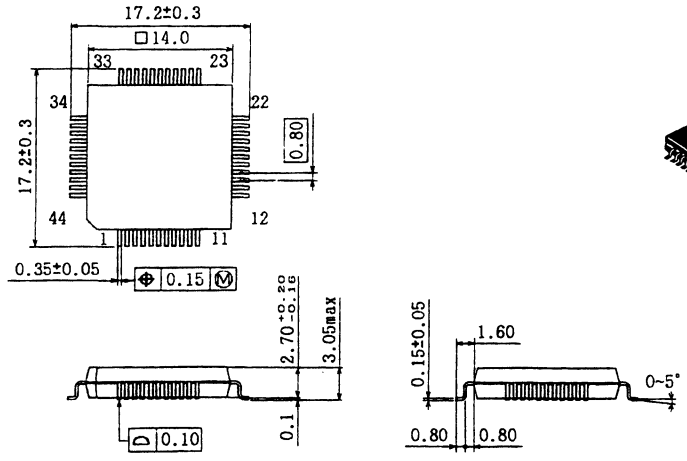
• FP-48DA



Hitachi America, Ltd. • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

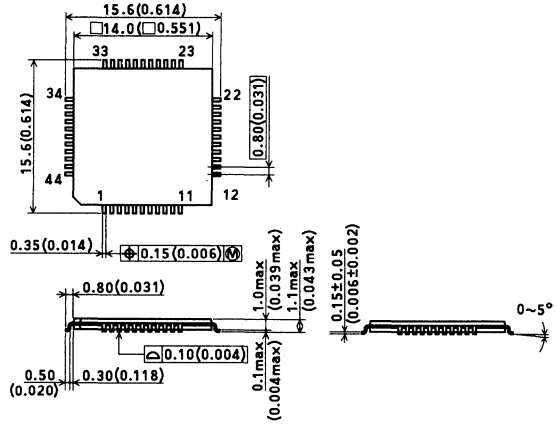
- **Plastic Quad Flat Package (QFP)** **Unit: mm**

- **FP-44A**



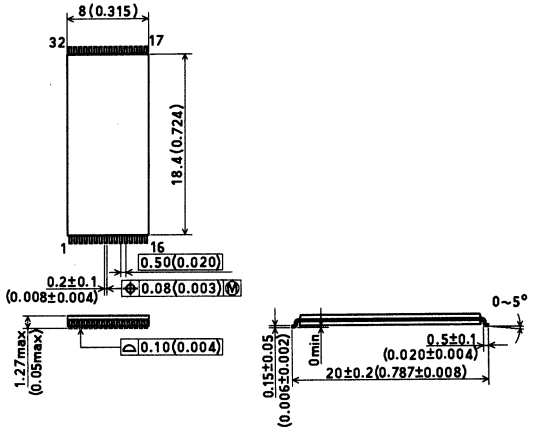
- **Plastic Thin Quad Flat Package (TQFP)** **Unit: mm**

- **TFP-44**

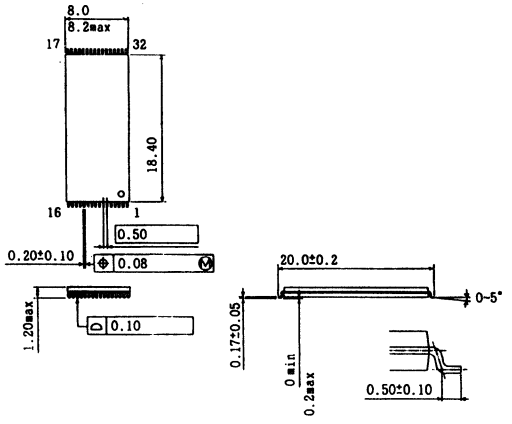


- **Plastic Thin Small Outline Package (TSOP) - Type I** **Unit: mm**

- **TFP-32D**

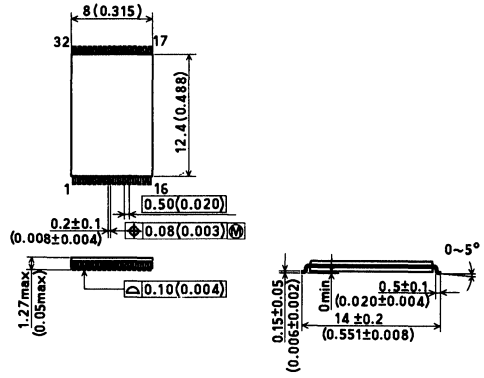


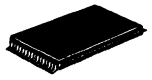
- **TFP-32DR**



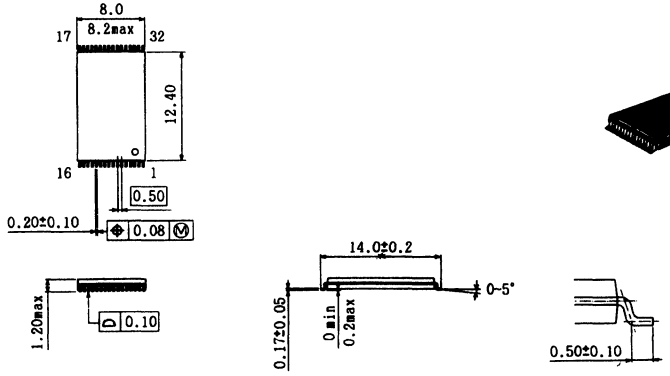
- **Plastic Thin Small Outline Package (TSOP) - Type I - continued** **Unit: mm**

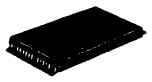
- **TFP-32DA**





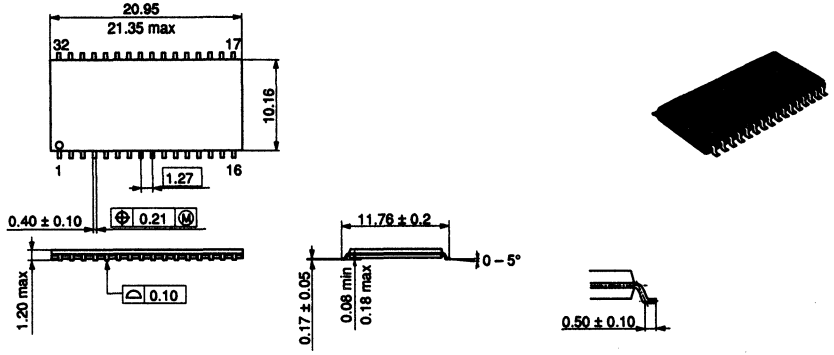
- **TFP-32DAR**



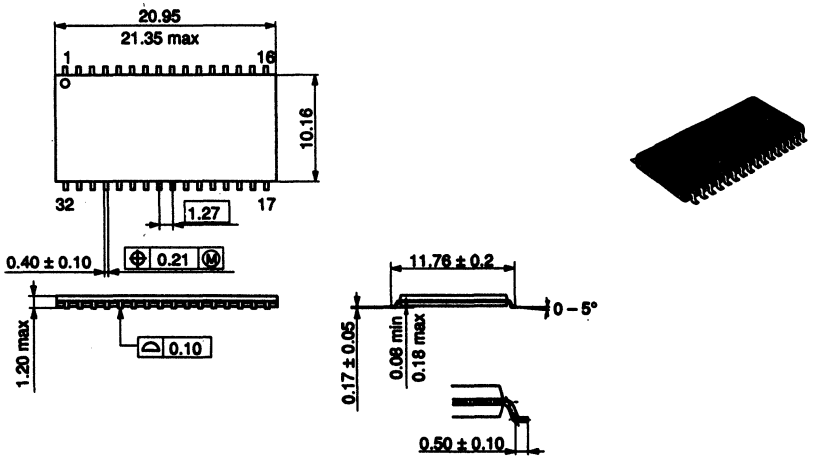


- **Plastic Thin Small Outline Package (TSOP) - Type II** **Unit: mm**

- **TTP-32D**

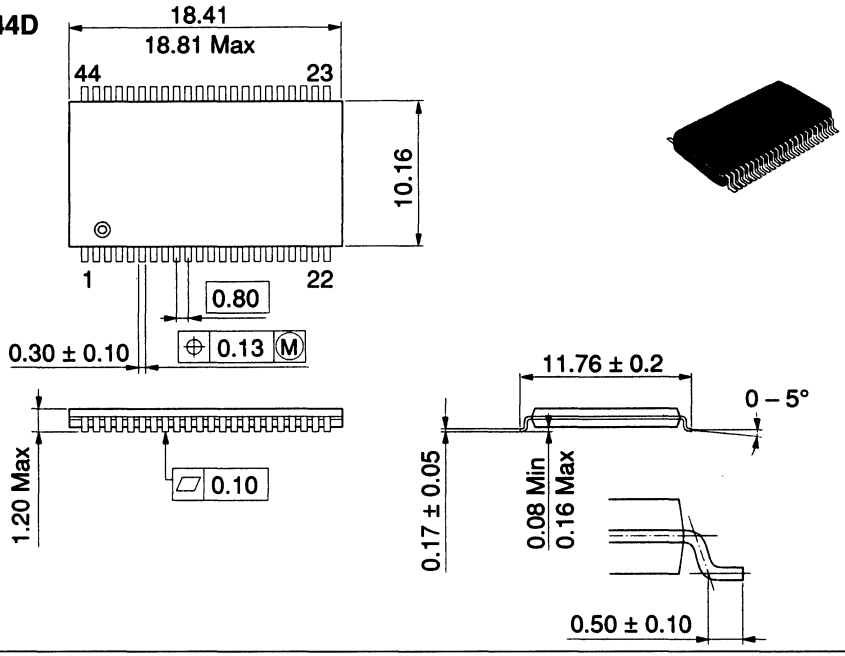


- **TTP-32DR**

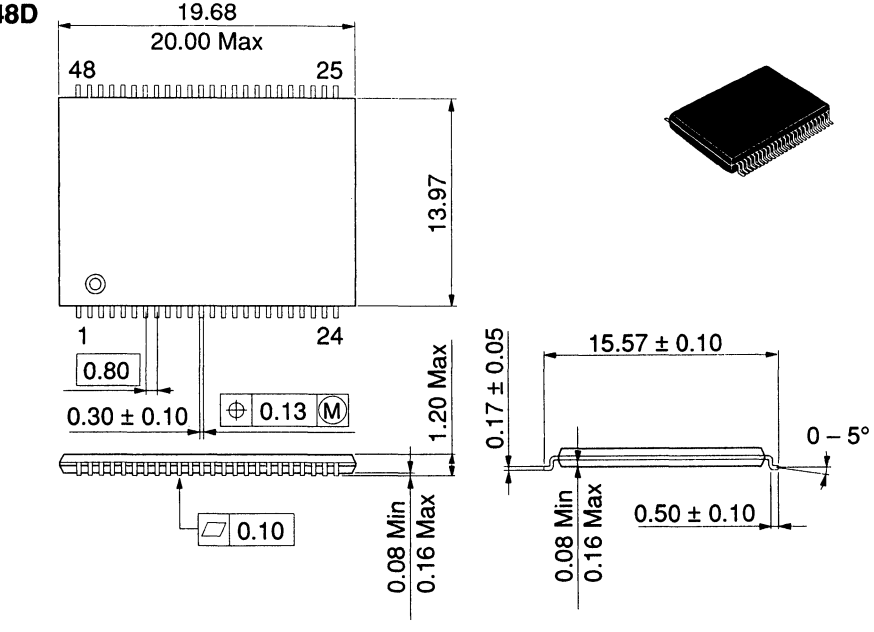


- **Plastic Thin Small Outline Package (TSOP) - Type II - continued** **Unit: mm**

- **TTP-44D**

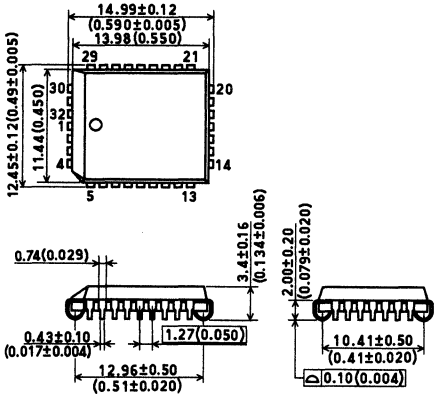


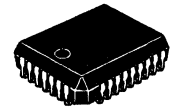
- **TTP-48D**



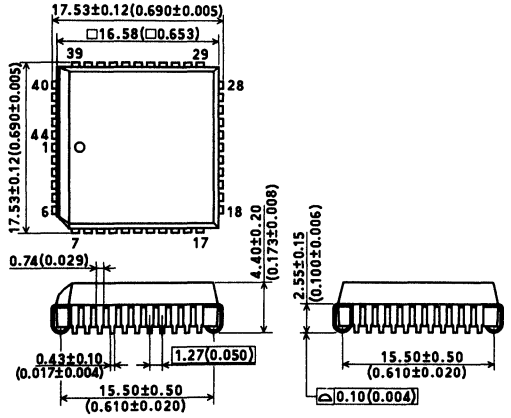
- **Plastic Leaded Chip Carrier (PLCC)** **Unit: mm**

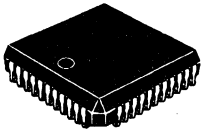
- **CP-32**





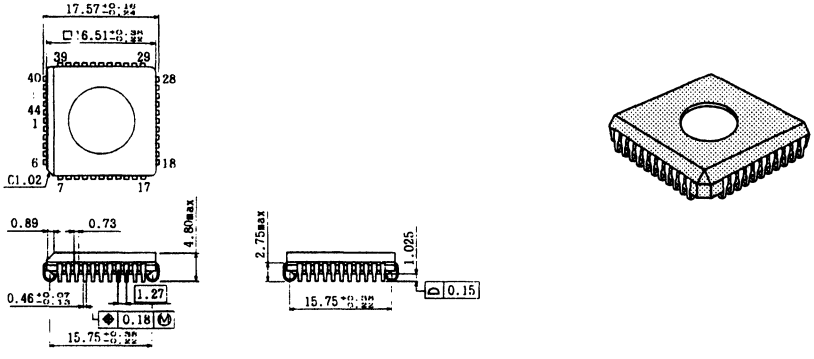
- **CP-44**





- **Ceramic Leaded Chip Carrier (LCC)** **Unit: mm**

- **CC-44**



RELIABILITY CHARACTERISTICS FOR SEMICONDUCTOR DEVICES

Hitachi semiconductor devices are designed, manufactured and inspected so as to achieve a high level of reliability. Accordingly, system reliability can be improved by combining highly reliable components along with proper environmental conditions. It is important to examine semiconductor device characteristics in light of their reliability.

- Semiconductor devices are essentially structure sensitive as seen in surface phenomenon. Fabricating the device requires precise control of a large number of process steps.
- Device reliability is partly governed by electrode materials and package materials, as well as by the coordination of these materials with the device materials.
- Devices employ thin-film and fine-processing techniques for metallization and bonding. Fine materials and thin film surfaces sometimes exhibit physically different characteristics from the bulks.
- Semiconductor device technology advances drastically: Many new devices have been developed using new processes over a short period of time. Thus, conventional device reliability data cannot be used in some cases.
- Semiconductor devices are characterized by volume production. Therefore, variations should be an important consideration.
- Initial and accidental failures are only considered to be semiconductor device failures based on the fact that semiconductor devices are essentially operable semipermanently. However, wear failures caused by worn materials and migration should also be reviewed when electrode and package materials are not suited for particular environmental conditions.
- Component reliability may depend on device mounting, conditions for use, and environment. Device reliability is affected by such factors as voltage, electric field strength, current density, temperature, humidity, gas, dust, mechanical stress, vibration, mechanical shock, and radiation magnetic field strength.

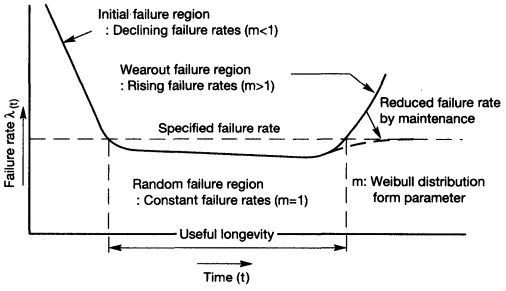


Figure 1 Typical failure rate curve

Device reliability is generally represented by the failure rate. 'Failure' means that a device loses its function, including intermittent degradation as well as complete destruction.

Generally, the failure rate of electric components and equipment is represented by the bathtub curve shown in Figure 1. For semiconductor devices, the configuration parameter of the Weibull distribution is smaller than 1, which means an initial failure type. Such devices ensure a long lifetime unless extreme environmental stress is applied. Therefore, initial and accidental failures can become a problem for semiconductor devices. Semiconductor device reliability can be physically represented as well as statistically. Both aspects of failures have been thoroughly analyzed to establish a high level of reliability.

SEMICONDUCTOR FAILURE TYPES AND THEIR MECHANISM

Semiconductor device failures are categorized as disconnection, short-circuit, deterioration and miscellaneous failures. These are summarized in Table 1. Typical failure mechanisms are:

Surface Deterioration

The pn junction has a charge density of 10^{14}–10^{20}/cm^3. If charges exceeding the above density are accumulated on the pn junction surface, particularly adjacent to the depletion layer, electric characteristics of the junction tend to be easily varied. Although the surface of such devices as planar transistors is generally covered with a SiO_2 film and is in an inactive state, the possibility of deterioration caused by surface channels still exists. Surface deterioration depends heavily on applied temperature and voltage and is often handled by the reaction model.

Table 1 Failure Modes, Mechanisms and Related Causes

Failure modes	Failure mechanisms	Failure related causes	
Withstanding voltage reduced, Short, Leak current increased, hFE degraded, Threshold voltage variation, Noise	Pin hole, Crack, Uneven thickness, Contamination, Surface inversion, Hot carrier injected	Passivation	Surface oxide film, Insulating film between wires
Open, Short, Resistance increased	Flaw, Void, mechanical damage, Break due to uneven surface, Non-ohmic contact, Insufficient adhesion strength, Improper thickness, Electromigration, Corrosion	Metallization	Interconnection, Contact, Through hole
Open, Short Resistance increased	Bonding runout, Compounds between metals, Bonding position mismatch, Bonding damaged	Connection	Wire bonding, Ball bonding
Open, Short	Disconnection, Sagging, Short	Wire lead	Internal connection
Withstanding voltage reduced, Short	Crystal defect, Crystallized impurity, Photo resist mismatching	Diffusion, Junction	Junction diffusion, Isolation
Open, Short, Unstable operation, Thermal resistance increased	Peeling, chip, Crack	Die bonding	Connection bertween die and package
Short, Leak current Increased, Open, Corrosion disconnection, Soldering failure	Integrity, moisture ingress, Impurity gas, High temperature, Surface contamination, Lead rust, Lead bend, break	Package sealing	Packaging, Hermetic Seal, Lead plating, Hermetic package & plastic package, Filler gas
Short, Leak current increased	Dirt, Conducting foreign matter, Oranic carbide	Foreign matter	Foreign matter in package
Short, Open, Fusing	Electron destroyed	Input/output pin	Electrostatics, Excessive Voltage, Surge
Soft error	Electron hole generated	Disturbance	alpha particle
Leak current increased	Surface inversion		High electric field

One example is surface deterioration caused by hot carriers. Hot carriers are generated when such devices as MOS dynamic RAMs are operated at a voltage near the minimum breakdown voltage (BV_{DS}) by raising internal voltage and when a strong electric field is established near the MOS device's drain resulting from reduced device geometry from 2 μm to 0.8 μm. Generated hot carriers may affect surface boundary characteristics on a part of the gate oxide film, resulting in degradation of threshold voltage (V_{TH}) and counter conductance (gm). Hitachi devices employ improved design and process techniques to prevent these problems. However, as processes becomes finer, surface deterioration may possibly become a serious problem.

Electrode-Related Failures

Electrode-related failures have become increasingly important as multi-layer wiring has become more complicated. Noticeable failures include electromigration and Al wiring corrosion in plastic sealed packages.

ELECTROMIGRATION

This is a phenomenon in which metal atoms are moved by a large current of about 10^6 A/cm^2 supplied to the metal. When ionized atoms collide with the current of scattering electrons, an 'electron wind' is produced. This wind moves the metal atoms in the opposite direction from the current flow, which generates voids at a negative electrode, and hillock and whiskers at an opposite one. The generated voids increase wiring resistance and cause excessive currents to flow in some areas, leading to disconnection. The generated whiskers may cause shortcircuits in multi-metal line.

MULTI-METAL LINE RELATED FAILURES

Major failures associated with multi-metal line include increased leak currents, shortcircuits caused by a failed dielectric interlayer, and increased contact metal resistance and disconnection between metal wirings.

AL LINE CORROSION AND DISCONNECTION

When plastic encapsulated devices are subjected to high-temperatures, high-humidity or a bias-applied condition, Al electrodes in devices can cause corrosion or disconnection (Figure 2). Under high-temperature and high-humidity, corrosion is randomly generated over the element surface. However, after an extended period of time, the corrosion has not significantly increased. Accordingly, this failure is possibly due to an initial failure associated with manufacturing. It is also verified that this type of failure can be generated when the adhesion surface between an element and resin is separated or when foreign materials are attached to the element with human saliva. Under a bias-applied, high-temperature, high-humidity condition, corrosion is generated in higher potential areas while in lower potential areas, grain corrosion occurs. Once this failure occurs in part of a device, the device can become worn out in a relatively short time. This failure proves to depend on the hydroscopic volume resistivity of sealed resin. The Al line corrosion mechanism described above is summarized in Figure 3.

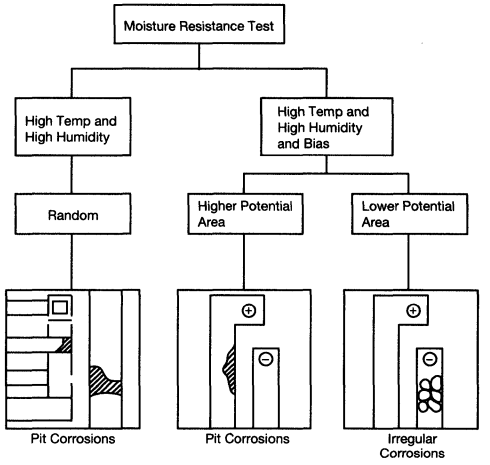


Figure 2 Categorized Al corrosion mode

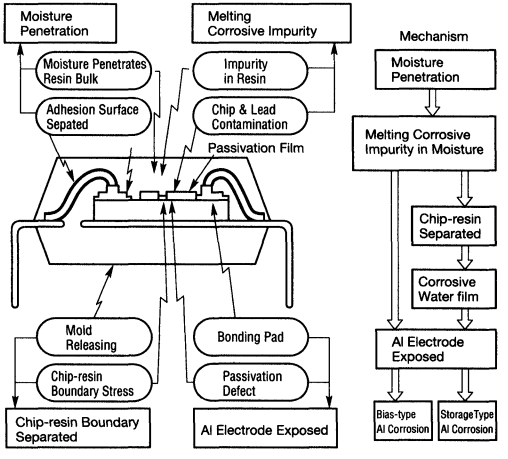


Figure 3 Plastic package section and Al corrosion mechanism

Bonding Related Failures

DEGRADATION CAUSED BY INTERMETALLIC FORMATION

Bonding strength degradation and contact resistance increase are caused by compounds formed in connections between Au wire and Al film. This is the most serious problem in terms of reliability. The compounds are formed rapidly during bonding and are increased through thermal treatment. Consequently, Hitachi products are subjected to a lower-temperature, shorter-period bonding whenever possible.

WIRE CREEP

Wire creep is wire neck destruction in an Au ball along an intergranular system occurring when a plastic sealed device is subjected to a long-term thermal cycling test. This failure results from increased crystal grains due to heat application when forming a ball at the top of an Au wire, or from an impurity introducing to the intergranular system. Bonding under usual conditions with no loop configuration failures does not cause this failure unless a severe long-term thermal cycling test is applied. Accordingly, wire creep is not a problem in actual usage.

CHIP CRACK

With the increase in chip size associated with the increased number of incorporated functions, more problems can occur during assembly, such as chip cracks during bonding. Bonding methods include Au-silicon eutectic, soldering and Ag-paste. Soldering and Ag-paste exhibit few chip crack problems. For Au-silicon eutectic, in contrast, large stress is applied to a pellet due to its strength and high temperature resistance for attachment, which may result in critical chip defects. Today, the chip destruction limit can be determined by finite-element analysis and by distortion measurement using a fine accuracy gauge. Ideally, Au-silicon eutectic should be evenly applied over the entire surface. However, this is difficult due to the existence of a silicon oxide film on the silicon back surface. Therefore, specifications for Au-silicon eutectic have been established based on stress analysis and thermal cycling test results.

REDUCED MAXIMUM POWER DISSIPATIONS

Heat fatigue due to thermal expansion coefficient mismatch among different materials deteriorates thermal resistance, resulting in decreased maximum power dissipations.

Sealing Related Failures

Hermetically sealed packages, including metal, glass, ceramic, and all other types, have the possibility of the following failures.

1. Al line corrosion on the chip surface due to slight moisture and reaction between different ionized materials.
2. Intermittent moving foreign metals short.
3. Al line corrosion due to extraneous H_2O caused by hermetic failure.

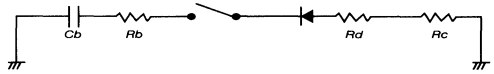
Moving foreign matter, even if it is a non-active solid, can be charged up within a cavity during movement, thereby inducing parastic effects and metal shorts. The foreign matter detection method is specified by MIL-STD-883C, PIND (Particle Impact Noise Detection) Test. The PIND test consists of filtering a particle impact waveform (ultrasonic waveform), detecting it with a microphone and then amplifying it.

Disturbance

ELECTROSTATIC DISCHARGE DESTRUCTION

Destruction caused by electrostatic discharge is a problem common to semiconductor devices. A recent report introduced three modes of this failure; the human body model, charged device model and field induced model.

The human body is easily charged. A person just walking across a carpet can be charged up to 15000 V. This voltage is high enough to destroy a device. An equivalent circuit of the human body model is shown in Fig. 4. The human body's capacitance Cb and resistance Rb are 100 to 200 pF and 1000 to 2000Ω, respectively. Assuming a body is charged with 2000V, the dissipated energy is obtained as follows: With a time constant of 10^{-7} sec, the dissipated energy is 2 KW, which is enough to destroy a small area of a chip.



Cb — Human Body Capacity
Rb — Human Body Resistance
Rd — Device Resistance
Rc — Resistance Between Device and Ground

$$E = \frac{1}{2} CbV^3 = 0.2 \times 10^{-3} J$$

Figure 4 Equivalent circuit of human body model

In the charged device model, charges are accumulated in a device, not a human body, and discharged through contact resistance during a short time. The equivalent circuit of this model is shown in Fig. 5. Device size and device position relative to GND are important parameters in this model since the model depends on device capacity.

In the field induced model, a device is left under a strong electric field or is affected by neighboring high voltage material. Since the capacitor of device or lead of device acts like an antenna, the following cases will possibly cause destruction: 1) a device is incorporated into a high electric field such as a CRT, 2) a device is left under a high-frequency electric field and 3) a device is moved with a container charged at high voltage, such as a tube.

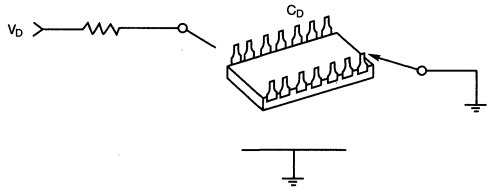


Figure 5 Equivalent circuit of charging model

LATCH-UP

Latch-up is a problem unique to CMOS devices. This problem is a thyristor phenomenon caused by a parasitic PNP or NPN transistor formed in the CMOS configuration. Latch-up can occur when: 1) an accidental surge voltage exceeds the maximum rating, 2) there is a power supply ripple, 3) an unregulated power supply and noise is applied or 4) a device is operated from two sources having different set-up voltages. These cases can cause input or output current to flow in the opposite direction from usual flow, which triggers parasitic thyristors. This results in excessive current flowing between a power supply and ground. This phenomenon continues until the power is turned off or the flowing current reduced to a certain level. Once latch-up occurs in an operating device, the device will be destroyed.

Much effort should be made in designing circuits to prevent latch-up. Latch-up triggering input or output currents start to flow under the following conditions:

$V <_{in} V_{CC}$ or $V_{in} <$ GND for input level
$V >_{out} V_{CC}$ or $V_{out} <$ GND for input level

Therefore, circuits should be designed so that no forward current flows through the input protection diodes or output parasitic diodes.

Soft errors

When α particles are generates from uranium or thorium in a package the silicon surface of an LSI chip, electron-hole pairs are formed which act as noise to data lines and other floating modes, causing temporary soft errors. This phenomenon is shown in Fig. 6. Only electrons from among the electron-hole pairs are only collected to a memory cell. As a result, the cell changes from a state of 1 to 0, which is a soft error.

Hitachi devices have been subjected to simulation and irradiation tests to prevent soft errors. In some cases, organic material, PIQ, is applied to the surface of the device.

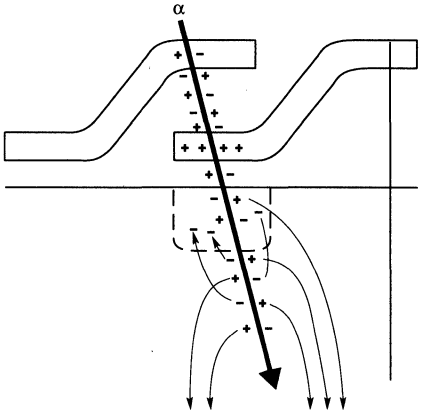


Figure 6 Soft error caused by α particles in dynamic memory

FINE GEOMETRY RELATED PROBLEMS

In response to higher integration requirements for memories and microcomputers, LSI geometry has been reduced in the way of 3 μm → 2 μm → 1.3 μm → 0.8 μm.

The problems associated with finer geometry are shown in Table 2.

Table 2 Finer geometry related problems

Item	Problems	Countermeasure
5V single supply voltage	• Breakdown voltage of gate oxide films • SiO_2 defects	Oxide film formation process improved • Cleaning • Gettering • Screening
Horizontal dimension reduction	• Soft errors by alpha particles • Al reliability reduced • CMOS latch up • Mask alignment margin reduced • Hot carriers	Surface passivation film improved • Metallization improved • Design/layout improved • Process improved
Vertical & horizontal dimension reduction	• Higher breakdown voltage not permitted • Electrostatic discharge resistance reduced	Use of low voltage examined • Configuration improved • Protection circuits enhanced

1. VIEWS ON QUALITY AND RELIABILITY

Hitachi basic views on quality are to meet individual users' purpose and required quality level and maintain that level for general application. Hitachi has made efforts to assure the standardized reliability of our IC memories in actual usage. To meet users' requests and to cover expanding application, Hitachi performs the followings:

(1) Design reliability in during new product development.
(2) Establish quality at all steps in the manufacturing process.
(3) Intensify the inspection and the assurance of reliability of all products.
(4) Improve the product quality based on marketing data.

Furthermore, to get higher quality and reliability, we cooperate with our research laboratories.

With the views and methods mentioned above, Hitachi makes the best efforts to meet the users' requirements.

2. RELIABILITY DESIGN OF SEMICONDUCTOR DEVICES

2.1 Reliability Target

Establishments of reliability target is important in manufacturing and marketing as well as function and price. It is not practical to determine the reliability target based on the failure rate under single common test condition. So, the reliability target is determined based on many factors such as each characteristics of equipment, reliability target of system, derating applied in design, operating condition and maintenance.

2.2 Reliability Design

Timely study and execution are essential to achieve reliability based on targets. The main items are the design standardization, device design including process and structural design, design review and reliability test.

(1) Design Standardization
Design standardization requires establishing design rules and standardizing parts, material, and process. When design rules are established on circuit, cell, and layout design, critical items about quality and reliability should be examined. Therefore, in using standardized process or material, even newly developed products would have high reliability.

(2) Device Design
It is important for device design to consider total balance of process design, structure design, circuit and layout design. Especially in case of applying new process or new material, we study the technology prior to development of the device in detail.

(3) Reliability Test by Test Pattern
Test Pattern is useful method for evaluating reliability of designing and processing ICs with complicated functions.

1. Purposes of Test Patterns are as follows:
   - Making clear about fundamental failure mode:
   - Analysis of relation between failure mode and manufacturing process condition.
   - Analysis of failure mechanism.
   - Establishment of QC point in manufacturing.
2. Effects of evaluation by Test Patterns are as follows:
   - Common fundamental failure mode and failure mechanism in devices can be evaluated.
   - Factors dominating failure mode can be picked up, and compared with the process having been experienced in field.
   - Able to analyze relation between failure causes and manufacturing factors.
   - Easy to run tests.

2.3 Design Review

Design review is a method to confirm systematically whether or not design satisfies the performance required including by users, follows the specified ways, and whether or not the technical items accumulated in test data and application data are effectively applied.

In addition, from the standpoint of competition with other products, the major purpose of design review is to insure quality and reliability of the product. In Hitachi, design review is performed in designing new products and also in changing products.

The followings are the items to consider at design review.

(1) Describe the products based on specified design documents.
(2) Considering the documents from the standpoint of each participant, plan and execute the subprogram such as calculation, experiments and investigation if unclear matter is found.
(3) Determine the contents and methods of reliability test based on design document and drawing.
(4) Check process ability of manufacturing line to achieve design goal.

(5) Arrange the preparation for production.
(6) Plan and execute the sub-programs of design changes proposed by individual specialists, for tests, experiments and calculation to confirm the design change.
(7) Refer to the past failure experiences with similar devices, confirm the prevention against them, and plan and execute the test program for confirmation of them.

In Hitachi, these study and decision at design review are made using the individual check lists according to its objects.

3. QUALITY ASSURANCE SYSTEM OF SEMICONDUCTOR DEVICES

3.1 Activity of Quality Assurance

The following items are the general views of overall quality assurance in Hitachi.

(1) Problems is solved in each process so that even the potential failure factors will be removed at final stage of production.
(2) Feedback of information is made to insure satisfied level of process ability.

At the result, we assure the reliability.

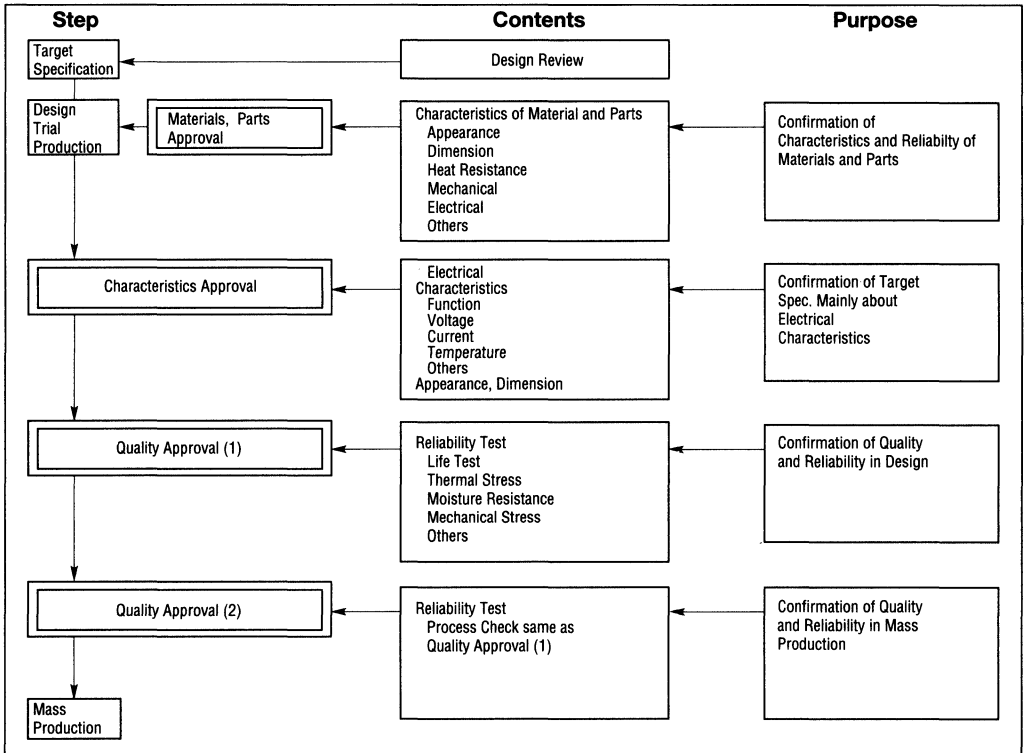


Figure 1 Flow Chart of Qualification3.2

3.2 Qualification

To assure the quality and reliability, the qualification tests are done at each stage of trial production and mass production based on the reliability design described in section 2.

The followings are the views on qualification in Hitachi:

(1) From the standpoint of customers, qualify the products objectively by a third party.
(2) Consider the failure experiences and data from customers.
(3) Qualify every change in design and work.
(4) Qualify intensively on parts and materials and process.
(5) Considering the process ability and factor of manufacturing fluctuation, establish the control points in mass production.

Consider the views mentioned above, qualification shown in Fig. 1 is done.

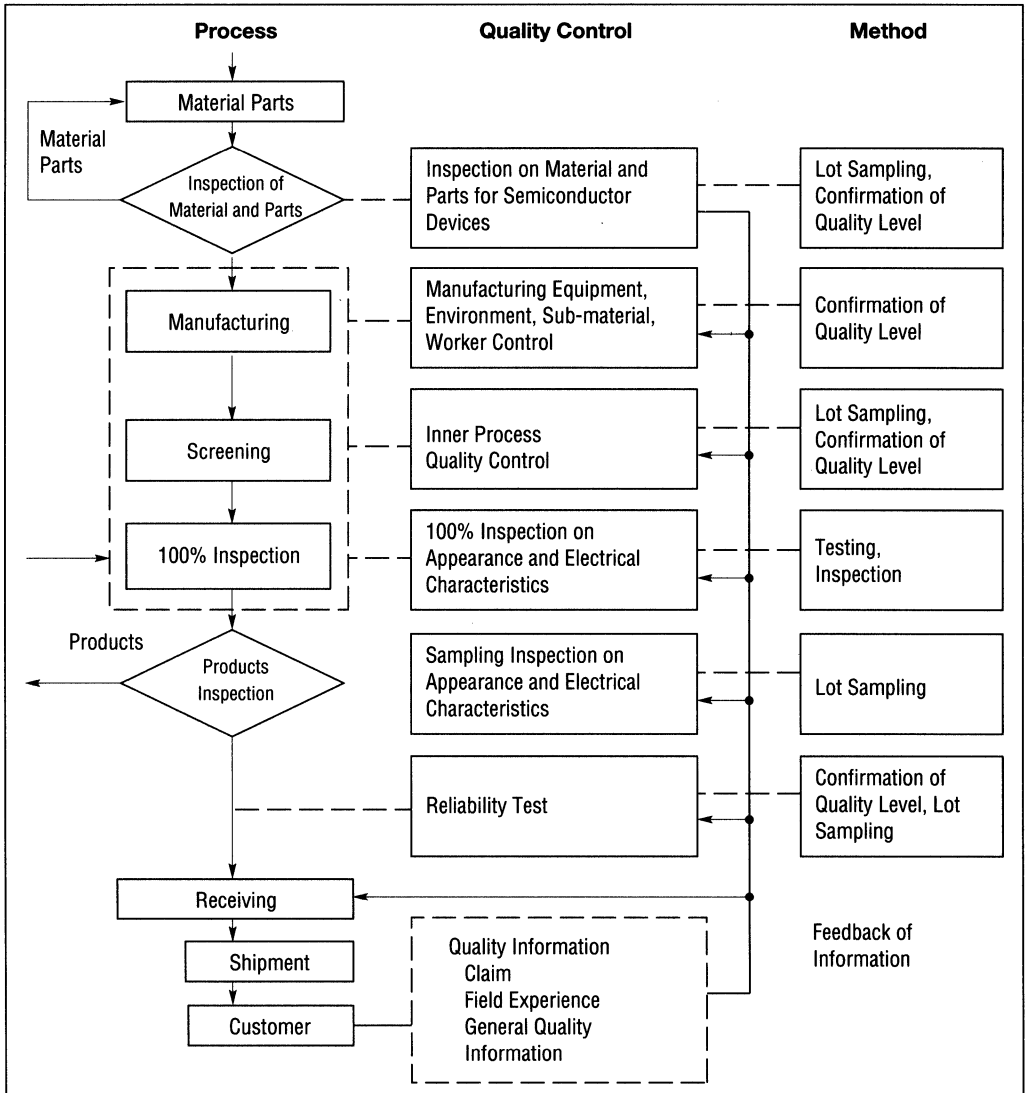


Figure 2 Flow Chart of Quality Control in Manufacturing Process

3.3 Quality and Reliability Control in Mass Production

To assure quality in mass production, quality is controlled functionally by each department, mainly by manufacturing department and quality assurance department. The total function flow is shown in Fig. 2.

3.3.1 Quality Control on Parts and Materials

With the tendency toward higher performance and higher reliability of devices, quality control of parts and materials becomes more important. The items such as crystal, lead frame, fine wire for wire bonding, package and materials required in manufacturing process like mask pattern and chemicals, are all subject to inspection and control.

Besides qualification of parts and materials stated in 3.2, quality control of parts and materials is defined in incoming inspection. Incoming inspection is performed based on its purchase specification, drawing and mainly sampling test based on MIL-STD-105D.

The other activities for quality assurance are as follows:

- **Table 1. Quality Control Check Points of Parts and Materials (example)**

Material, Parts	Important Control Items	Point for Check
Wafer	Appearance	Damage & Contamination on Surface
	Dimension	Flatness
	Sheet Resistance	Resistance
	Defect Density	Defect Numbers
	Crystal Axis	
Mask	Appearance	Defect Numbers, Scratch
	Dimension	Dimension Level
	Resistoration	
	Gradation	Uniformity of Gradation
Fine Wire for Wire Bonding	Appearance	Contamination, Scratch, Bend, Twist
	Dimension	
	Purity	Purity Level
	Elongation Ratio	Mechanical Strength
Frame	Appearance	Contamination, Scratch
	Dimension	Dimension Level
	Processing Accuracy	
	Plating	Bondability, Solderability
	Mounting Characteristics	Heat Resistance
Ceramic Package	Appearance	Contamination, Scratch
	Dimension	Dimension Level
	Leak Resistance	Airtightness
	Plating	Bondability, Solderability
	Mounting Characteristics	Heat Resistance
	Electrical Characteristics	
	Mechanical Strength	Mechanical Strength
Plastic	Composition	Characteristics of Plastic Material
	Electrical Characteristics	
	Thermal Characteristics	
	Molding Performance	Molding Performance
	Mounting Characteristics	Mounting Characteristics

(1) Technology Meeting with Vendors
(2) Approval and Guidance of Vendors
(3) Analysis and tests of physical chemistry.

The typical check points of parts and materials are shown in Table 1.

3.3.2 Inner Process Quality Control

To control inner process quality is very significant for quality assurance of devices. The quality control of products in every stage of production is explained below. Fig. 3 shows inner process quality control.

(1) Quality Control of Products in Every Stage of Production

Potential failure factors of devices should be removed in manufacturing process. Therefore, check points are set up in each process so as not to move the products with failure factors to the next process. Especially, for high reliability devices, manufacturing lines are rigidly selected in order to control the quality in process. Additionally we perform rigid check per process or per lot, 100% inspection in proper processes so as to remove failure factors caused by manufacturing fluctuation, and screenings depending on high temperature aging or temperature cycling.

Contents of controlling quality under processing are as follows:

- Control of conditions of equipment and workers and sampling test of uncompleted products.
- Proposal and execution of working improvement.
- Education of workers
- Maintenance and improvement of yield
- Picking up of quality problems and execution of countermeasures toward them.
- Communication of quality information.

(2) Quality Control of Manufacturing Facilities and Measuring Equipment

Manufacturing facilities have been developed with the need of higher devices in performance and the automated production. It is also important to determine quality and reliability.

In Hitachi, automated manufacturing is promoted to avoid manufacturing fluctuation, and the operation of high performance equipment is controlled to function properly.

As for maintenance inspection for quality control, daily and periodically inspections are performed based on specification on every check point.

As for adjustment and maintenance of measuring equipment, the past data and specifications are clearly checked to keep and improve quality.

(3) Quality Control of Manufacturing Circumstances and Sub-material.
Quality and reliability of devices are affected especially by manufacturing process. Therefore, we thoroughly control the manufacturing circumstances such as temperature, humidity, dust, and the sub-materials like gas or pure water used in manufacturing process.

Dust control is essential to realize higher integration and higher reliability of devices. To maintain and improve the clearness of manufacturing site, we take care buildings, facilities, air-conditioning system, materials, clothes and works. Moreover, we periodically check on floating dust in the air, fallen dust or dirtiness on floor.

Process	Control Point		Purpose of Control
Purchase of Material			
Wafer →	Wafer	Characteristics, Appearance	Scratch, Removal of Crystal Defect Wafer
Surface Oxidation	Oxidation		Assurance of Resistance
Inspection on Surface Oxidation		Appearance, Thickness of Oxide Film	Pinhole, Scratch
Photo Resist	Photo Resist		
Inspection on Photo Resist ◇PQC Level Check		Dimension, Appearance	Dimension Level Check of Photo Resist
Diffusion	Diffusion	Diffusion Depth, Sheet Resistance	Diffusion Status
Inspection on Diffusion ◇PQC Level Check		Gate Width Characteristics of Oxide Film, Breakdown Voltage	Control of Basic Parameters (V_{TH}, etc) Cleaness of surface Prior Check of V_{IH} Breakdown Voltage Check
Evaporation	Evaporation	Thickness of Vapor Film Scratch, Contamination	Assurance of Standard Thickness
Inspection on Evaporation ◇PQC Level Check			
Wafer Inspection	Wafer	Thickness, V_{TH} Characteristics	Prevention of Crack, Quality Assurance of Scribe
Inspection on Chip Electrical Characteristics	Chip	Electrical Characteristics	
Chip Scribe		Appearance of Chip	
Inspection on Chip Appearance ◇PQC Lot Judgement			
Frame →			
Assembling	Assembling	Appearance of Chip Bonding Appearance after Wire Bonding	Quality Check of Chip Bonding Quality Check of Wire Bonding
◇PQC Level Check		Pull Strength, Compression Width, Shear Strength Appearance after Assembling	Prevention of Open and Short
Inspection after Assembling ◇PQC Lot Judgement			
Package →			
Sealing	Sealing	Appearance after Sealing Outline, Dimension	Guarantee of Appearance and Dimension
◇PQC Level Check	Marking	Marking Strength	
Final Electrical Inspection Failure Analysis		Analysis of Failures, Failure Mode, Mechanism	Feedback of Analysis Information
Appearance Inspection			
Sampling Inspection on Products			
Receiving			
Shipment			

Figure 3 Example of Inner Process Quality Control

3.3.3 Final Test and Reliability Assurance

(1) Final Tests

Lot inspection is done by quality assurance department for the product passed in 100% test in final manufacturing process. Though 100% of passed products is expected, sampling inspection is subjected to prevent mixture of failed products by mistake. The inspection is executed not only to confirm that the products meet users requirement, but to consider potential factors. Our lot inspection is based on MIL-STD-105D.

(2) Reliability Assurance Tests

To assure reliability, the reliability tests are performed periodically, and performed on each manufacturing lot if user requires.

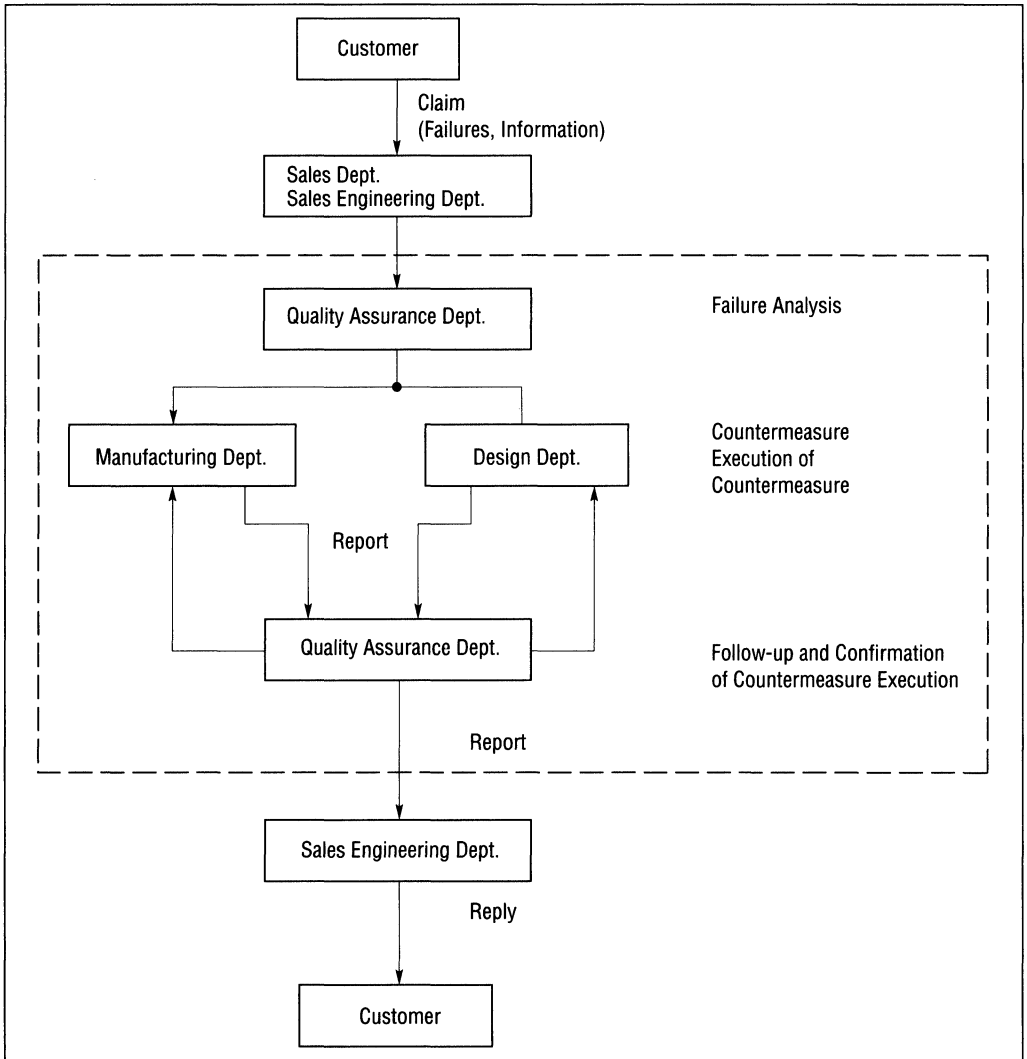


Figure 4 Process Flow Chart of Coping with Failure to a Customer

■ OUTLINE OF TESTING METHOD

1. INSPECTION METHOD

In memory IC inspection, quality cannot be judged by DC test on external pins only, because the number of elements (such as a transistor) which can be judged in the DC test is only 1/1000 of all elements. The following are the address patterns proposed to inspect whether the internal circuits are functioning correctly.

(1) All "Low", All "High"
(2) Checker Flag
(3) Stripe Pattern
(4) Marching Pattern
(5) Galloping
(6) Waling
(7) Ping-Pong

Those are not all, but representative ones. There are also patterns to check the mutual interference of bits and patterns for maximum power dissipation. Among the above mentioned patterns, numbers 1 to 4 are called N pattern, which can check one sequence of N bit IC memory with the several times of N patterns at most. Numbers 5 to 7 are called N^2 patterns, which need several times of N^2 patterns to check one sequence of N bit IC memory. Serious problem arises in using N^2 pattern in a large-capacity memory. For example, inspection of 16K memory with galloping pattern takes a lot of time—about 30 minutes. (1), (2) and (3) are rather simple and good methods, however, they are not perfect to find any failure in decoder circuits. Marching is the most simple and necessary pattern to check the function of IC memories.

2. MARCHING PATTERN

The marching pattern, as its name indicates, is a pattern in which "1"s march into all bits of "0"s. For example, a simple addressing of 16 bit memory is described below.

(1) Clear all bits. See Fig. 1 (a).
(2) Read "0" from 0th address and check that the read data is "0". Hereafter, "Read" means "checking and judging data"
(3) Write "1" on 0th address. See Fig. 1 (b).
(4) Read "0" from 1st address.
(5) Write "1" on 1st address.
(6) Read "0" from nth address.
(7) Write "1" on nth address. See Fig. 1 (c).
(8) Repeat (6) to (7) to the last address. Finally, all data will be "1".
(9) After all data is "1", repeat from (2) to (8) replacing "0" and "1".

With this method, 5N address patterns are necessary for the N-bit memory.

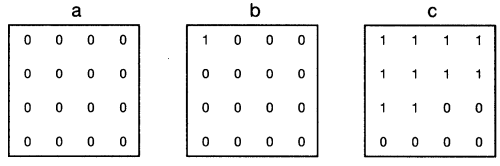


Figure 1 Addressing method of for 16 bit memory in the Marching pattern

1. EEPROM

1.1 EEPROM Memory Cell

An EEPROM is an electrically erasable and programmable ROM which can be erased or written remotely while the system is in operation.
Hitachi EEPROM memory cells are MNOS-type (Metal Nitride Oxide Semiconductor) as shown in Figure 1-1.

A MNOS memory cell consists of two layers of oxide film and nitride film. The thickness of the oxide film is about 20 Å and the nitride film is 300 to 500 Å. There are traps in the boundary of the oxide and nitride films to catch electrons. The electrons move by the tunneling phenomenon between the substrate and traps.

1.2 64-kbit CMOS EEPROM Function

Page Write Function: The 64-kbit HN58C65 can latch 32 bytes (max.) and write them in one write cycle. The write cycle time is specified as 10 ms (max.) The effective byte write speed of HN58C65 in page write mode is 10 ms/32 bytes = 0.31 ms/byte. Thus it takes only 2.56 seconds to write the entire HN58C65. Figure 1.2 shows the internal operation. The following describes the operation sequence:

1. The 32-byte memory cell data at the row address selected by address pins A_5–A_{12} are latched.
2. Latched data at the column address specified by address pins A_0–A_4 are altered with write data, which is put into the D_{in} buffer from I/O pins I/O_0–I/O_7. The 32 bytes (max.) of latched data are altered by repeating this operation 32 times.
3. 32 bytes of memory cell data in the selected row 1 are erased (all set to 1).
4. Latched data is written into the selected row 3.
5. CPU acknowledges completion of the write cycle based on the internal timer. The HN58C65 provides RDY/$\overline{BUSY}$ and $\overline{DATA}$ polling to indicate the write completion.

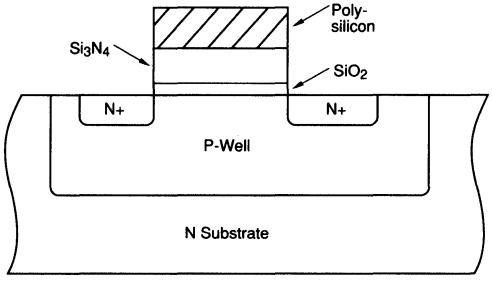


Figure 1-1 MNOS-Type Memory Transistor

Internal Timer: The HN58C65 indicates the completion of a data write to the CPU by using an internal timer. The HN58C65 enters the next cycle as soon as the completion of the write is detected. This function offers a high system throughput as the CPU can access other devices during a write cycle. The HN58C65 has two functions, RDY/$\overline{BUSY}$ and $\overline{DATA}$ polling, to indicate the completion of data write.
The RDY/$\overline{BUSY}$ approach indicates the completion of data write by using pin 1. It is low when the HN58C65 is in data write operation ($\overline{BUSY}$) and turns to the high impedance state at the end of data write (RDY). The RDY/$\overline{BUSY}$ pin should be pulled up as it uses open drain output. The RDY/$\overline{BUSY}$ pins can be OR-wired when using several HN58C65's.
The $\overline{DATA}$ polling approach, implemented in software, indicates the completion of data write through pin 19 (I/O_7). While the data write is not completed, I/O_7 shows an inverted version of what was written in the last cycle. In using this approach, the RDY/$\overline{BUSY}$ pin should be opened or grounded. The DATA polling approach can acknowledge the completion of a data write in an individual HN58C65, even if several HN58C65's are used in the system.
Data Protection: The EEPROM performs a data write with a higher voltage (V_{PP}) than the power supply voltage (V_{CC}). The HN58C65 internally generates V_{PP} by a high voltage generator with the combination of control pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$). It supports the following functions to avoid accidental data write (data protection).

1. Data protection against noise on the control pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during operation.
2. Data protection against noise at power on/off.

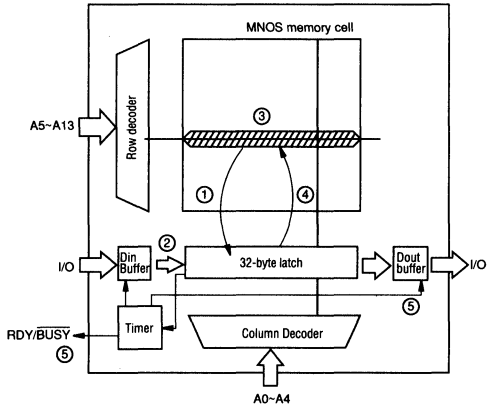


Figure 1-2 HN58C65 Page Write

2. EPROM/OTPROM

2.1 EPROM Programming

Figure 2-1 shows the sectional structure of an EPROM memory cell. The upper gate, one of the gates made of two-layered polycrystalline silicon, is called the control gate and is connected to a word line. The lower layer is called the floating gate and is not connected. This memory cell is programmed as follows.

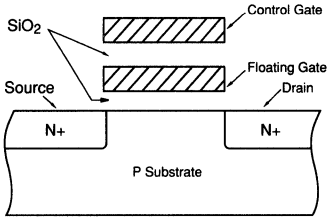


Figure 2-1 Cross Section of a EPROM Memory Cell

With the substrate and source grounded, apply a high voltage between the drain and control gate. An electrical potential incline will occur between the source and drain so that the intensity of the electric field will become high near the drain. Because of this electric field, electrons are accelerated and the so-called hot electrons will be generated, which jump over the energy barrier of SiO_2 film. The hot electrons are pulled by the electric potential of the control gate and poured into the floating gate. Electrons stored in the floating gate remain stable as they fall into a well surrounded by an energy barrier of SiO_2 film. Therefore, it is evident that the quality of the SiO_2 film surrounding the floating gate is essential for good data retention characteristics. To keep data retention in the 5- or 10-year range, high quality SiO_2 film is needed.

Figure 2-2 shows the fundamental characteristics of the EPROM transistor. While I_D in a non-programmed transistor begins to flow with V_G of about 1 V, the current in a programmed transistor does not flow until V_G rises to 7 to 10 V. Therefore, if the voltage of the word line applied to the control gate is about 5 V in the readout, a non-programmed memory transistor will be on, and the programmed memory transistor will be off. This means that the data can be read out by means of the same structure as a NOR-type mask ROM.

2.2 Erasing EPROM

When shipped, all bits of the EPROM are at logic 1 with all electrons in the floating gate released (erased). Changing the logic 1 to logic 0, through the application of the specified waveform and voltage, programs the necessary information. The higher the V_{PP} voltage and the longer the program pulse width t_{PW}, the more electrons can be programmed in as shown in Figure 2-3. If V_{PP} exceeds the rated value, such as by overshoot, the pn junction of the memory may yield to permanent breakdown. To avoid this, check V_{PP} overshoot of the PROM programmer. Also, check negative-voltage-induced noise at other terminals, which

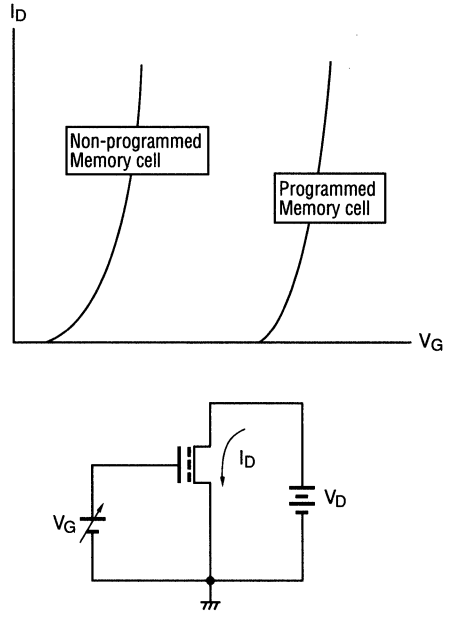


Figure 2-2 Fundamental Characteristics of a EPROM Memory Cell

can create a parasitic transistor effect and reduce the yield voltage. Hitachi's EPROMS can usually be written and erased more than 100 times.

EPROMS are erased by ultraviolet light exposure through a transparent window on the package. Electrons in the floating gate get energy from photons and become hot electrons again with enough energy to go over the energy barrier of SiO_2 film. The hot electrons go through to the control gate or the substrate and erasure is completed. Therefore, light with enough energy to get the electrons over the energy barrier of SiO_2 film is needed for erasure. Light energy is proportional to its frequency, and described as $E = h\upsilon$. E is the energy of light, h is Planck's constant, and υ is light frequency. Erasure is not caused by light over certain wavelengths and under certain wavelengths. However, the erasure time depends upon the quantity of photons, therefore the erasure time cannot be

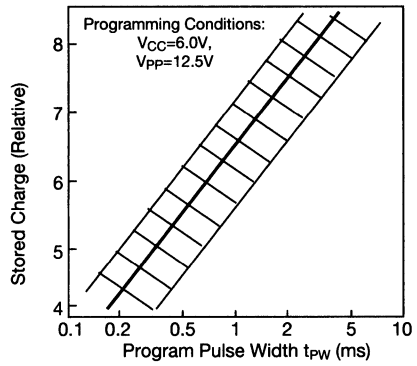


Figure 2-3 Standard Programming Characteristics of EPROMs

shortened by using a shorter wavelength. Figure 2-4 shows the relation between wavelength and erasure effectiveness. Erasure starts at about 4000 Å and is saturated at about 3000 Å.

For erasure, the wavelength and minimum irradiation rate of ultraviolet light must be 2537 Å. and 15 W•s/cm^2 respectively. These conditions can be met by placing the device 2 to 3 cm below a 12,000 W/cm^2 UV lamp for about 20 minutes.

The UV transmittance of the transparent lid materials is about 70%. However, it is influenced by contamination or foreign materials on the lid surface. The contamination or foreign materials should be removed with a solvent such as alcohol that does not damage the package.

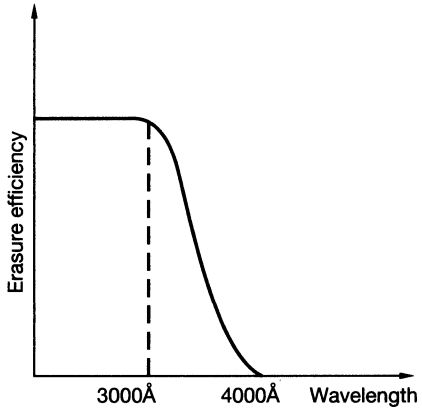


Figure 2-4 Erasure Efficiency of EPROM

Figure 2-5 shows the EPROM standard erasure characteristics.

2.3 EPROM Data Retention Characteristics

About 2 to 20 × 10^{-14} coulombs of electrons are accumulated in the floating gate when programmed. However, these electrons dissipate with time and the data may be inverted. The mechanism of electron dissipation is generally explained as follows.

Data Dissipation by Heat: The electrons at the floating gate are in a non-equilibrium state, so the dissipation of electrons by thermal energy is unavoidable. Therefore, the data retention time depends on temperature. Figure 2-6 shows typical data retention characteristics. The data retention time is proportional to the reciprocal of absolute temperature.

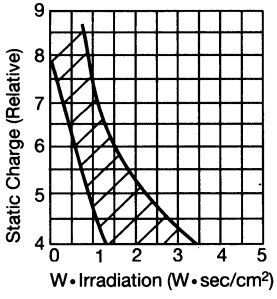


Figure 2-5 Standard Erasure Characteristics

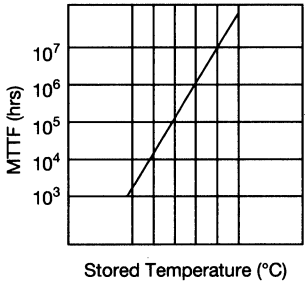


Figure 2-6 EPROM Data Retention Characteristics

Data Dissipation by Ultraviolet Light: Ultraviolet light at a wavelength no greater than 3000 to 4000 Å is capable of releasing the electric charge at the floating gate of the EPROM with varying efficiencies. Fluorescent light and sunlight contain some ultraviolet light, and so prolonged exposure to these lights can cause data corruption as a result of electric charge dissipation. Figure 2-7 shows the standard data retention time under an ultra-violet eraser, sunlight, and fluorescent lighting.

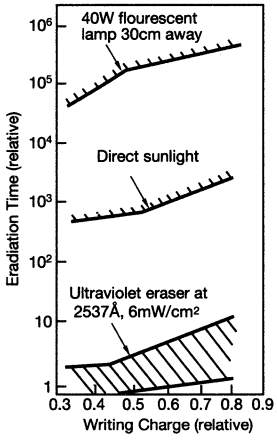


Figure 2-7 EPROM Data Retention Time

2.4 Optimized High Speed Programming

With the increase of EPROM density, the time for programming becomes more important. Methods for high speed programming have been developed and put into practical use for each EPROM generation. There are three methods for high speed programming. Figure 2-8 shows the relative programming times of these methods.

Please refer to the data sheet about each programming method.

2.5 Device Identifier Code

EPROM programming conditions depend on the EPROM manufacturers' standards and specific device types. Confusion on the proper use of varying methods required may cause poor or failing operation. As a countermeasure, some EPROMS provide embedded device identifier codes including such information as the manufacturer and device type. Some newly developed commercial EPROM programmers can set write conditions automatically by recognizing this code.

Different programming conditions are as follows.

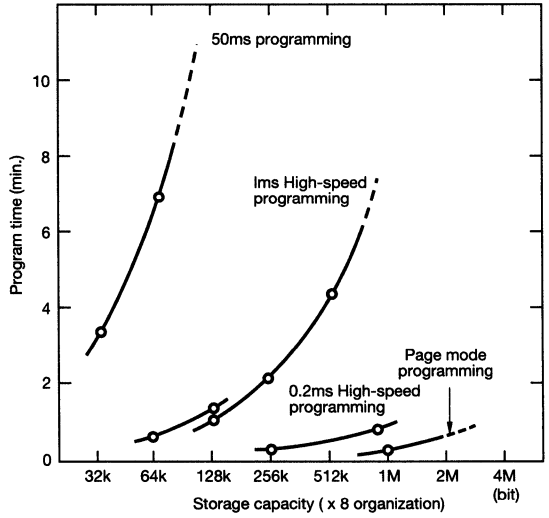
1. Program voltage
2. Program timing
3. High performance programming algorithm
4. Pin configuration

The Hitachi EPROM has a device identifier code area adjacent to the memory access area as shown in Figure 2-9.

Table 2-1 describes how to use the device identifier code. Setting A_9 at 12 V and A_1–A_8 and A_{10}–A_{13} at V_{IL}, access the device identifier code area and I/O_0–I/O_7, and output the programming condition code with V_{IL} or V_{IH} of A_0.

2.6 Shielding Label

When using an EPROM in an environment where it can be exposed to ultraviolet light, Hitachi recommends placing a shield label, over the transparent lid to absorb the ultraviolet light. In choosing a shielding label, the following points should be carefully checked.



Note: Actual programing time differs depending on the programmar.

Figure 2-8 Comparison of Shortened Programming Time

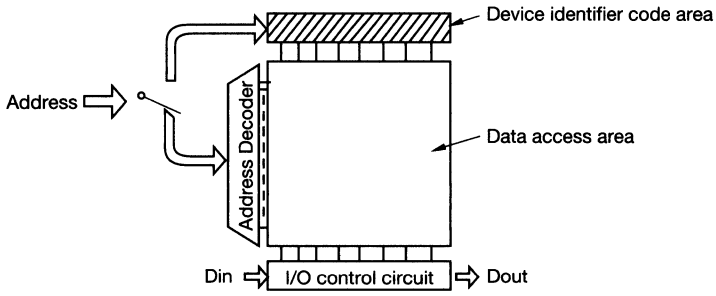


Figure 2-9 Device Identifier Code

1. Adhesiveness (mechanical strength)
   Avoid repeated removal and reattachments, or exposure to dust that may reduce the adhesive strength. Ultraviolet erasure and reprogramming are recommended after stripping off an attached label. (When the need arises to change a label, it is advisable to place a new one over the old one since peeling may create a static charge.)
2. Allowable temperature range
   Use the shielding label in an environment where temperature is stable within the specified allowable temperature range. Beyond the specified temperature range, the paste on the label may harden or stick too tightly. When it hardens, the label may come off easily. When it sticks too tightly, the paste may remain on the window glass after the label has been removed.
3. Moisture resistance
   Use the shielding label in an environment where humidity is stable within the specified allowable humidity range.

2.7 EPROM Programmer

The EPROM programmer stores the user's program in its internal RAM and writes the program in the EPROM. For this programming, at least three functions are necessary: the blank check function prior to programming, programming function, and verify function after programming. Figure 2-10 shows the programming flowchart. Some programmers check for pin contact failure or reverse insertion before the blank check.

The outline of each check is a follows.

1. Pin contact check
   In the ROM pin and socket connection test, checking is normally performed by detecting forward current at each EPROM pin. Care is necessary as this forward biased resistance differs in products of each company.
2. Reverse insertion check
   This check detects the reverse insertion of the device, then places the equipment in reset mode and protects the device and equipment if the condition is found.

Table 2-1 Hitachi EPROM Device Identifier Code

Manufacturer Code	Hitchi	A_0	I/O_8–I/O_{15}	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Hex Data
		V_{IH}	–	0	0	0	0	0	1	1	1	07
ROM code	HN27128A	V_{IH}	–	0	0	0	0	1	1	0	1	0D
	HN27256	V_{IH}	–	0	0	0	1	0	0	0	0	10
	HN27C256	V_{IH}	–	1	0	1	1	0	0	0	0	B0
	HN27C256H	V_{IH}	–	0	0	1	1	0	0	0	1	31
	HN27C256A	V_{IH}	–	0	0	1	1	0	0	0	1	31
	HN27512	V_{IH}	–	1	0	0	1	0	1	0	0	94
	HN27C1024H	V_{IH}	–	1	0	1	1	1	0	1	0	BA
	HN27C101A	V_{IH}	–	0	0	1	1	1	0	0	0	38
	HN27C301A	V_{IH}	–	1	0	1	1	1	0	1	1	B9
	HN27C4096	V_{IH}	–	1	0	1	0	0	0	1	0	A2

3. Blank check
   This check is performed before programming. It checks whether the device is an erased EPROM, or it prevents EPROM reprogramming. Since output data in the erased condition is high, the check is for whether the data in the EPROM are all 1s. It will fail even if one bit is 0. Normally, it is designed to provide a warning with a lamp or buzzer.
4. Programming
   The function of programming the data from the internal RAM of the programmer into the EPROM will fail when programming cannot be done. The normal flow is as shown in Figure 2-11. The EPROM data for a target location will be read out prior to programming and compared with the programming data intended for that location. If the data matches, programming will be skipped. If they differ, programming will be performed. Then, the data will be read back and compared with the original programming data, and if they match, the programmer will progress to the next address.
5. Verify
   This function checks after programming completion whether or not the programming is correct when comparing with the data in the internal RAM of the programmer. It will fail when they do not match. Normally, when it fails, it lights the fail lamp and displays the address and data.
6. How to input a program
   Table 2-2 shows several methods for inputting the program data to the internal RAM of the programmer. Normally, paper tape input and teletypewriter input are preferred options.

2.8 Handling EPROMs

If touched by a charged human body or rubbed with plastics or dry cloth, the glass window of an EPROM generates static electricity with causes device malfunctions. Typical malfunctions are faulty blanking and write margin setting that give the false impression that information has been correctly written in. As already reported at international conferences concerning the reliability of LSI chips, this is due to the prolonged retention of electric charge (resulting from static electricity) on the glass window. Such malfunctions can be eliminated by neutralizing the charges by irradiating the EPROM with ultraviolet rays for a short time. The EPROM should be reprogrammed after this irradiation since it also reduces the electric charges in the floating gates. The basic countermeasure is to prevent the charging of the window, which can be achieved by the following methods, as in the prevention of common static breakdown of ICs.

1. Ground operators who handle the EPROM. Avoid using things such as gloves that may generate static electricity.
2. Avoid rubbing the glass window with plastic or other materials that may generate static electricity.
3. Avoid the use of coolant sprays which may contain some free ions.
4. Use shielding labels (especially those containing conductive substances) that can evenly distribute any established charge.

Table 2-2 EPROM Data Input

Method	Content
Copy input	Input by copying the master ROM.
Manual input	Input by the keyswitches on the front pannel. Used for correction or revision of programs.
Paper tape input	Paper tape furnished from the host system is read with the tape reader.
Teletypewriter input	Input with the teletypewriter. Preparation, correction, and list preparation of the program can be made.

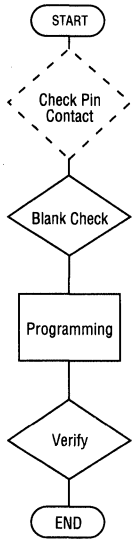


Figure 2-10 Programming Flowchart of EPROM Programmer (1)

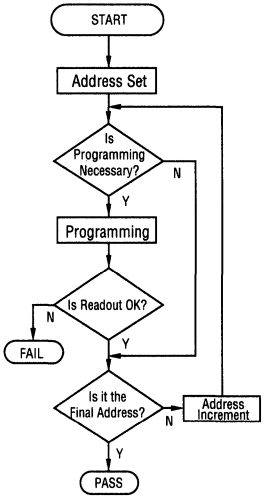


Figure 2-11 Programming Flowchart of EPROM Programmer (2)

2.9 Ensuring OTPROM Reliability

The one-time-programmable ROM (OTPROM) has two forms: standard dual in-line package (DIP) and small outline package (SOP). It is only one-time programmable because it has no window for ultraviolet light exposure; testing by programming and erasure cannot be performed after it is assembled.

As a means of improving reliability, Hitachi performs screening tests for programming, access time, and data retention on OTPROM wafers during the manufacturing process.

However, rare defects may occur in the assembly process that cannot be completely removed in the final test screening which is only a reading test.

Therefore, Hitachi recommends that users perform high temperature baking after programming these devices to ensure the highest reliability.

Detailed conditions and procedures for screening are shown in Figure 2-12. First, program and verify the devices. Then leave them without bias at 125 to 150°C for 24 to 48 hours.

After that, check the readout function, and discard chips with data retention failures.

From the results of devices in which the recommended screening test is properly performed, we find the data retention characteristics of OTPROMs are generally equal to EPROMs.

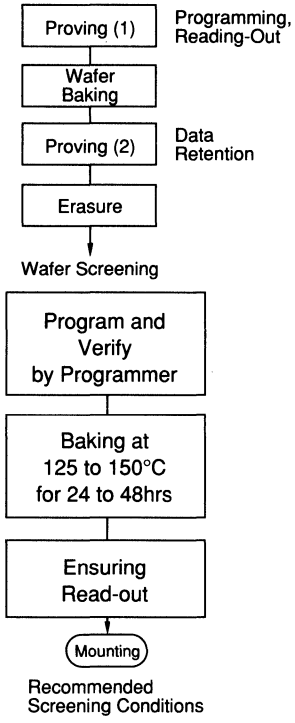


Figure 2-12 Screening Flowchart of OTPROM

3. Mask ROM Programming Instruction

The writing of custom program code into mask ROMs is performed by a CAD system on a large-scale computer. ROM code data should conform to the specifications given below, using either EPROM or floppy disk. Additional instructions, such as chip select or customer part numbers, should be noted on the "ROM Specification Identification Sheet."

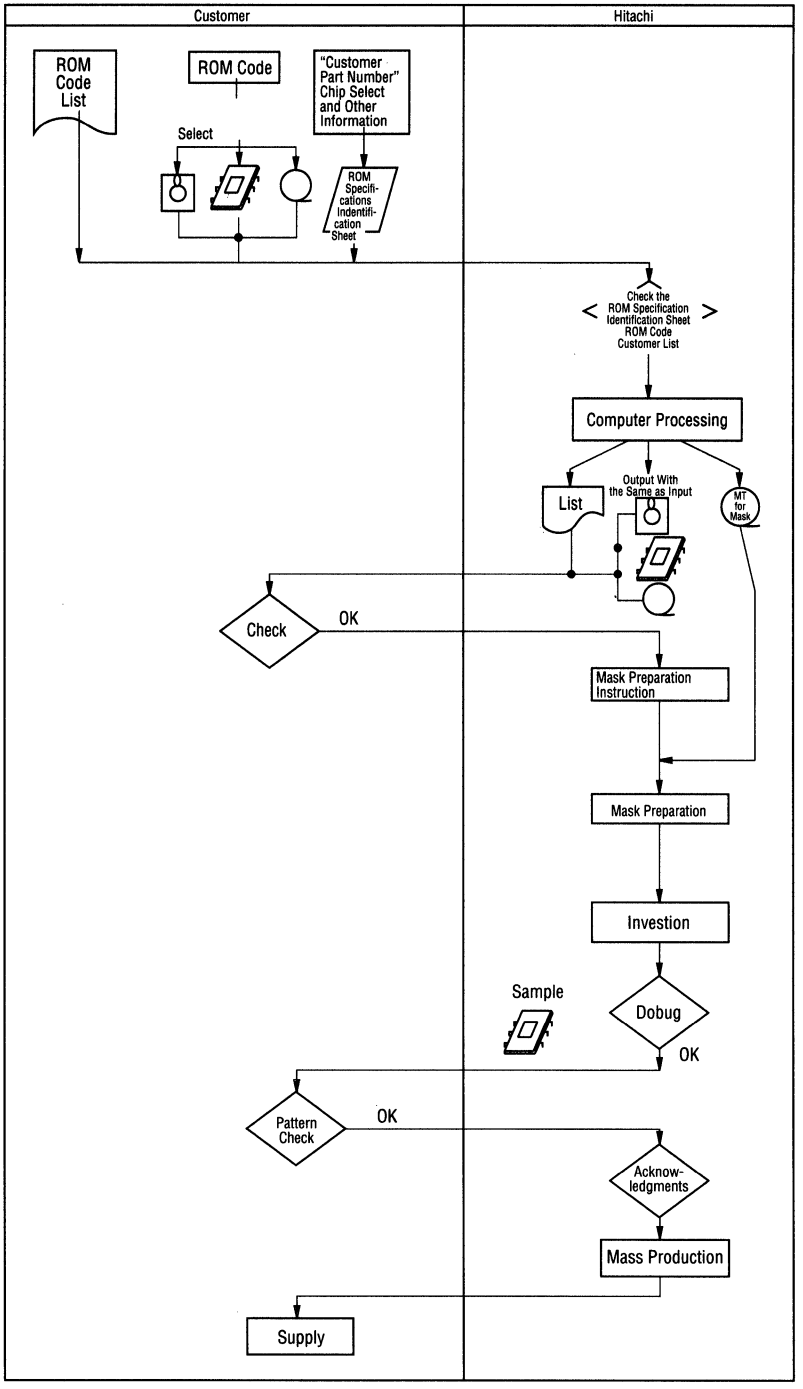


Figure 3-1 Mask ROM Development Flowchart

Flash Memory

SECTION 2
Flash Memory

2

HITACHI

Hitachi America, Ltd. • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

HITACHI

Hitachi America, Ltd. • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

HN28F101 Series

1M (128K x 8-bit) Flash Memory

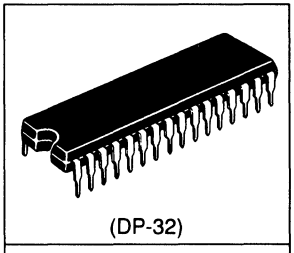
■ DESCRIPTION

The Hitachi HN28F101 is a 1-Megabit CMOS Flash Memory organized as 131,072 x 8-bit. The HN28F101 is capable of in-system electrical chip erasure and reprogramming.

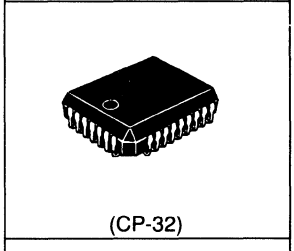
The HN28F101 programs and erases data with a 12 V V_{PP} supply and a 5 V V_{CC} supply. The HN28F101 conforms to the JEDEC Standard Dual-Supply EEPROM Command Set. Its fast, high-reliability programming algorithm is initiated with Command Inputs. There are two methods of erasing the HN28F101: Manual and Automatic, both are initiated with Command Inputs.

The Manual Chip Erase method follows a fast, high-reliability erase algorithm. The Automatic Chip Erase function erases all data automatically without external control; Status Polling is used to inform the CPU of erase completion. Both erase methods provide a fast erase time without voltage stress to the device or deterioration in data reliability.

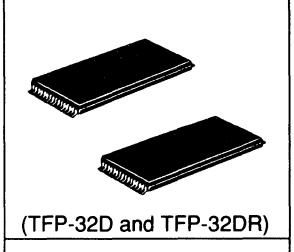
Hitachi's HN28F101 is offered in JEDEC-Standard Byte-Wide EPROM pinouts in 32-pin Plastic DIP and 32-lead PLCC, TSOP, and SOP packages. This allows an easy upgrade to the HN28F4001, 4 Megabit Flash Memory, as well as socket replacement with EPROMs and Mask ROMs. The HN28F101 TSOP package is offered in both standard and reverse bend pinouts.



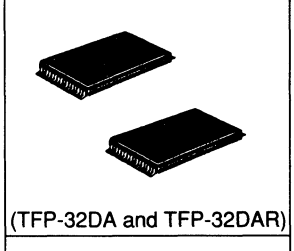
(DP-32)



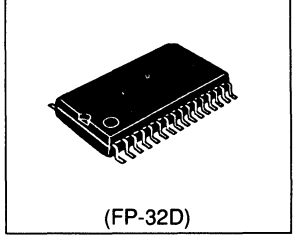
(CP-32)



(TFP-32D and TFP-32DR)



(TFP-32DA and TFP-32DAR)



(FP-32D)

■ FEATURES

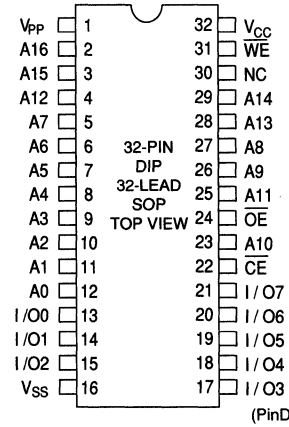
- Dual Power Supply:
  V_{CC} = 5 V ± 10%
  V_{PP} = 12.0 V ± 0.6 V (Erase/Program)
- Fast Access Times:
  120 ns/150 ns/200 ns (max)
- Low Power Dissipation:
  Read Current: 10 mA (typ)
  Standby Current: 20 µA (max)
- Byte Programming:
  Programming Time: 25 µs/Byte (typ)
  Address, Data, Control Latch Function
- Automatic Chip Erase Function:
  Erase Time: 1 sec (typ)
  Internal Pre-Write and Erase Verify
  Status Polling Function
- Erase Endurance:
  10,000 times (min)
- Pin Arrangement:
  JEDEC Standard Byte-Wide EPROM
  EPROM and Mask ROM Compatible
- Packages:
  32-pin Plastic DIP
  32-lead PLCC
  32-lead Plastic TSOP (Type I)
  32-lead Plastic SOP

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN28F101P-12	120 ns	32-pin Plastic DIP
HN28F101P-15	150 ns	(DP-32)
HN28F101P-20	200 ns	
HN28F101CP-12	120 ns	32-lead PLCC
HN28F101CP-15	150 ns	(CP-32)
HN28F101CP-20	200 ns	
HN28F101TD-12	120 ns	32-lead Plastic TSOP
HN28F101TD-15	150 ns	(TFP-32D)
HN28F101TD-20	200 ns	8 x 20 mm
HN28F101RD-12	120 ns	32-lead Plastic TSOP
HN28F101RD-15	150 ns	(TFP-32DR)
HN28F101RD-20	200 ns	8 x 20 mm
		Reverse bend
HN28F101T-12	120 ns	32-lead Plastic TSOP
HN28F101T-15	150 ns	(TFP-32DA)
HN28F101T-20	200 ns	8 x 14 mm
HN28F101R-12	120 ns	32-lead Plastic TSOP
HN28F101R-15	150 ns	(TFP-32DAR)
HN28F101R-20	200 ns	8 x 14 mm
		Reverse bend
HN28F101FP-12	120 ns	32-lead Plastic SOP
HN28F101FP-15	150 ns	(FP-32D)
HN28F101FP-20	200 ns	

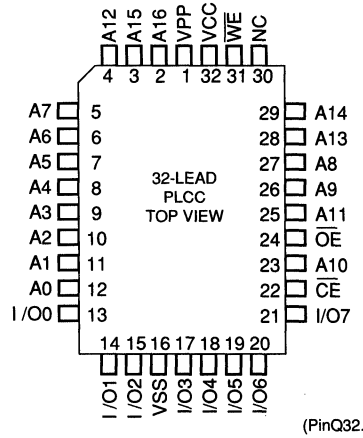
■ PIN ARRANGEMENT

HN28F101P Series
HN28F101FP Series



(PinD32.HN28F101)

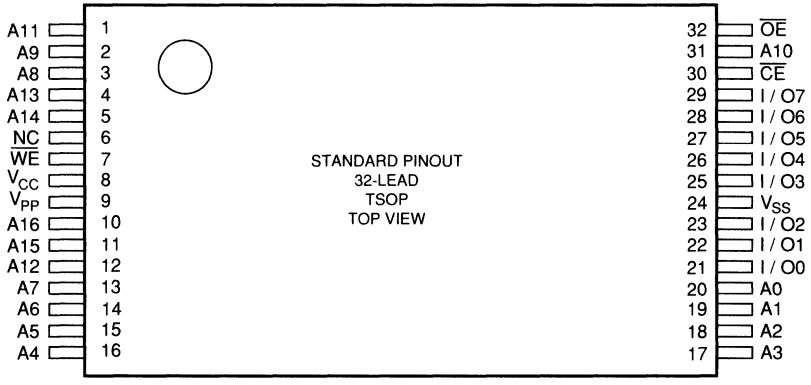
HN28F101CP Series



(PinQ32.HN28F101)

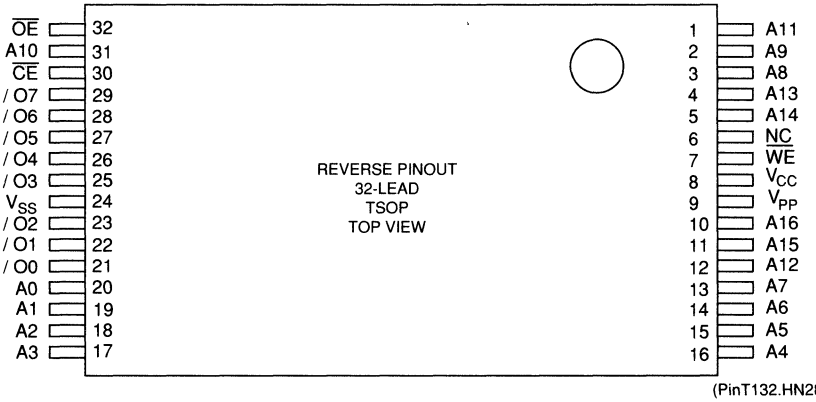
■ PIN ARRANGEMENT (continued)

HN28F101TD Series
HN28F101T Series



(PinT132.HN28F101T)

HN28F101RD Series
HN28F101R Series

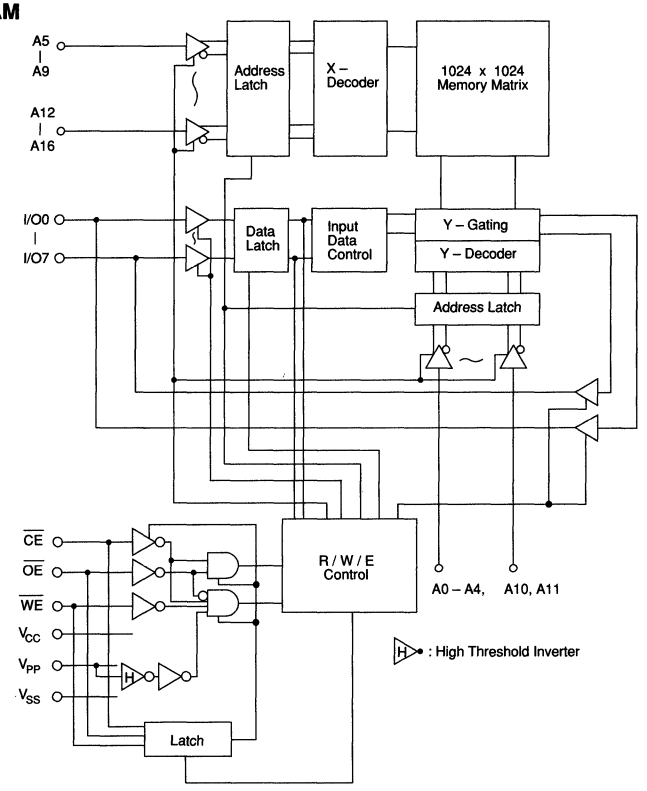


(PinT132.HN28F101R)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{16}	Address
I/O_0 - I/O_7	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{PP}	Programming Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



(BD.HN28F101)

■ MODE SELECTION

Mode		V_{PP}	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A_9	I/O_0 to I/O_7
Read	Read	V_{CC} [6]	V_{IL}	V_{IL}	V_{IH}	A_9	D_{OUT}
	Output Disable	V_{CC}	V_{IL}	V_{IH}	V_{IH}	X [6]	High-Z
	Standby	V_{CC}	V_{IH}	X	X	X	High-Z
	Identifier [1]	V_{CC}	V_{IL}	V_{IL}	V_{IH}	V_H [2]	ID
Command	Read [3,5]	V_{PP}	V_{IL}	V_{IL}	V_{IH}	A_9	D_{OUT}
	Output Disable	V_{PP}	V_{IL}	V_{IH}	V_{IH}	X	High-Z
	Standby	V_{PP}	V_{IH}	X	X	X	High-Z
	Write[4]	V_{PP}	V_{IL}	V_{IH}	V_{IL}	A_9	D_{IN}

Notes:
1. Device Identifier Code can be output in Command Program Mode. Refer to Command Address and Data Input Table.
2. $11.4\ V \leq V_H \leq 12.6\ V$
3. Data can also be read when 12 V is applied to V_{PP}. Device Identifier Code can be output by Command Inputs. See Device Identifier Mode Description Table for more details.
4. Refer to Command Address and Data Input Table. Data is programmed, erased, or verified after inputting Commands.
5. Status of Automatic Erase can be verified in this mode by Status Polling on I/O_7. I/O_6 to I/O_6 are in high impedance states.
6. X = Don't Care. $V_{PP} = 0\ V$ to V_{CC}.

■ COMMAND ADDRESS AND DATA INPUT

Command	Bus Cycles Required	First Cycle			Second Cycle		
		Operation Mode [1]	Address [2]	Data [3]	Operation Mode [1]	Address [2]	Data [3]
Read [4]	1	Write	X	00H	Read	RA	D_{OUT}
Read Identifier Codes	2	Write	X	90H	Read	IA	ID
Set-up Erase/Erase [5]	2	Write	X	20H	Write	X	20H
Erase Verify	2	Write	EVA	A0H	Read	X	EVD
Setup Auto Erase/Auto Erase [6]	2	Write	X	30H	Write	X	30H
Setup Program/Program [7]	2	Write	X	40H	Write	PA	PD
Program Verify [7]	2	Write	X	C0H	Read	X	PVD
Reset	2	Write	X	FFH	Write	X	FFH

Notes:
1. Refer to Command Program Mode in Mode Selection about operation mode.
2. Refer to Device Identifier Mode. IA = Identifier Address, PA = Programming Address, EVA = Erase Verify Address, RA = Read Address.
3. Refer to Device Identifier Mode. PA are latched by Programming Command. ID = Identifier Output Code, PD = Programming Data, PVD = Programming Verify Output Data, EVD = Erase Verify Output Data.
4. Command latch default value when applying 12 V to V_{PP} is "00H". Device is in Read Mode after V_{PP} is set to 12 V (before other Command is input).
5. All data in the chip is erased. Erase data according to the Manual Chip Erase Flowchart.
6. All data in the chip is erased. Data is automatically programmed to 00H and erased automatically by internal logic circuitry. External Manual Erase Verify is not necessary. Erasure completion is verified by Status Polling on I/O_7.
7. Program data according to the Programming Flowchart.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Programming Voltage [1]	V_{PP}	-0.6 to +14	V
All Input and Output Voltage [1,2]	V_{IN}, V_{OUT}	-0.6 to +7.0	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range [3]	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-10 to +80	°C

Notes:
1. Relative to V_{SS}.
2. V_{IN} and V_{OUT} = -2.0V for pulse width ≤ 20 ns.
3. Device storage temperature range before programming.

■ CAPACITANCE (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to 70°C, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	-	-	6	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	-	-	12	pF	V_{OUT} = 0V

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{CC} - 1 to V_{CC}, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{IN} = 0 V to V_{CC}
Output Leakage Current	I_{LO}	-	-	2	µA	V_{OUT} = 0 V to V_{CC}
Operating V_{CC} Current	I_{CC1}	-	6	15	mA	I_{OUT} = 0 mA, f = 1 MHz
	I_{CC2}	-	10	30	mA	I_{OUT} = 0 mA, f = 8 MHz
Standby V_{CC} Current	I_{SB1}	-	-	1	mA	$\overline{CE}$ = V_{IH}
	I_{SB2}	-	-	20	µA	$\overline{CE}$ = V_{CC}
V_{PP} Current	I_{PP1}	-	-	20	µA	V_{PP} = 5.5 V
Input Voltage [3]	V_{IL}	-0.3[1]	-	0.8	V	
	V_{IH}	2.2	-	V_{CC} + 0.3[2]	V	
Output Voltage	V_{OL}	-	-	0.45	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA

Notes:
1. V_{IL} min = -2.0 V for pulse width ≤ 20 ns.
2. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns. If V_{IH} is over the specified maximum value, Read operation can not be guaranteed.
3. Only defined for DC and long cycle function test. V_{IL} max = 0.45 V, V_{IH} min = 2.4 V for AC function test.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

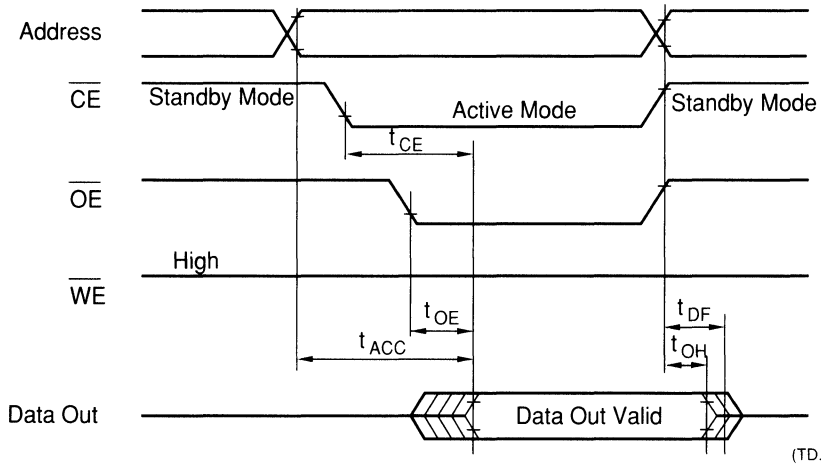
Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V / 2.0V

Item	Symbol	HN28F101-12		HN28F101-15		HN28F101-20		Test Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
Address Access Time	t_{ACC}	-	120	-	150	-	200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
Chip Enable Access Time	t_{CE}	-	120	-	150	-	200	ns	$\overline{OE}$ = V_{IL}
Output Enable Access Time	t_{OE}	-	60	-	70	-	80	ns	$\overline{CE}$ = V_{IL}
Output Disable to High-Z [1]	t_{DF}	0	40	0	50	0	60	ns	$\overline{CE}$ = V_{IL}
Output Hold to Address Change	t_{OH}	5	-	5	-	5	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



(TD.R.HN28F101)

■ DC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING AND ERASE OPERATIONS

(V_{CC} = 5V ± 10%, V_{PP} = 12.0 V ± 0.6 V, T_a = 0 to 70°C)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current		I_{LI}	-	-	2	µA	V_{IN} = 0 V to V_{CC}
Output Leakage Current		I_{LO}	-	-	2	µA	V_{OUT} = 0 V to V_{CC}
Operating V_{CC} Current	Read	I_{CC1}	-	6	15	mA	I_{OUT} = 0 mA, f = 1 MHz
		I_{CC2}	-	10	30	mA	I_{OUT} = 0 mA, f = 8 MHz
	Program	I_{CC3}	-	9	10	mA	
	Erase	I_{CC4}	-	10	40	mA	Automatic Erase
		I_{CC5}	-	5	15	mA	Manual Erase
Standby V_{CC} Current		I_{SB1}	-	-	1	mA	$\overline{CE}$ = V_{IH}
		I_{SB2}	-	-	200	µA	$\overline{CE}$ = V_{CC}
V_{PP} Current	Read	I_{PP1}	-	-	1	mA	V_{PP} = 12.6 V
	Program	I_{PP2}	-	5	30	mA	Programming
	Erase	I_{PP3}	-	35	80	mA	Automatic Erase
		I_{PP4}	-	10	30	mA	Manual Erase
Input Voltage [3]		V_{IL}	-0.3[4]	-	0.8	V	
		V_{IH}	2.2	-	V_{CC} + 0.3[5]	V	
Output Voltage		V_{OL}	-	-	0.45	V	I_{OH} = 2.1A
		V_{OH}	2.4	-	-	V	I_{OH} = -400 µA

Notes:
1. V_{CC} must be applied before V_{PP} and removed after V_{PP}, or V_{CC} and V_{PP} must be applied simultaneously.
2. V_{PP} must not exceed 14 V, including overshoot.
3. Device reliability may be adversely affected if the device is installed or removed while V_{PP} = 12 V.
4. V_{IL} min = -1.0 V for pulse width ≤ 20 ns.
5. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

■ AC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING AND ERASE OPERATIONS

(V_{CC} = 5V ± 10%, V_{PP} = 12.0 v ± 0.6 V, T_a = 0 to 70°C)

Test Conditions

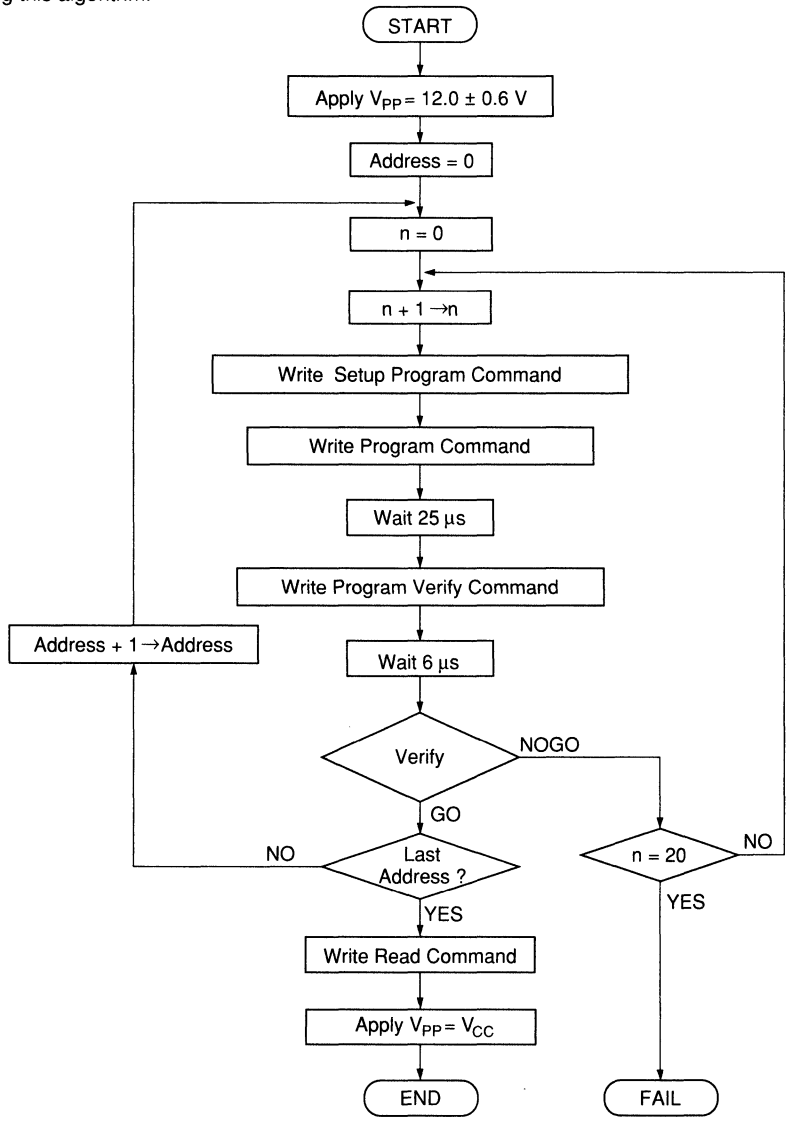
- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V / 2.0V

Item	Symbol	HN28F101-12		HN28F101-15		HN28F101-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Programming Cycle Time	t_{CWC}	120	-	150	-	200	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns
Address Hold Time	t_{AH}	60	-	60	-	60	-	ns
Data Setup Time	t_{DS}	50	-	50	-	50	-	ns
Data Hold Time	t_{DH}	10	-	10	-	10	-	ns
Chip Enable Setup Time	t_{CES}	0	-	0	-	0	-	ns
Chip Enable Hold Time	t_{CEH}	50	-	50	-	50	-	ns
V_{PP} Setup Time	t_{VPS}	100	-	100	-	100	-	ns
V_{PP} Hold Time	t_{VPH}	100	-	100	-	100	-	ns
Write Enable Pulse Width	t_{WEP}	70	-	70	-	80	-	ns
Write Enable High Time	t_{WEH}	40	-	40	-	40	-	ns
Output Enable Setup Time Before Command Prog.	t_{OEWS}	0	-	0	-	0	-	ns
Output Enable Setup Time Before Verify	t_{OERS}	6	-	6	-	6	-	µs
Verify Access Time	t_{VA}	-	120	-	150	-	200	ns
Output Enable Setup Time Before Status Polling	t_{OEPS}	120	-	120	-	120	-	ns
Status Polling Access Time	t_{SPA}	-	120	-	150	-	200	ns
Standby Time Before Prog.	t_{PPW}	25	-	25	-	25	-	µs
Erase Standby Time	t_{ET}	9	11	9	11	9	11	ms
Output Disable Time	t_{DF}	0	40	0	50	0	60	ns
Automatic Erase Time	t_{AET}	0.5	30	0.5	30	0.5	30	s

Notes:
1. $\overline{CE}$, $\overline{OE}$, $\overline{WE}$ must be fixed high during V_{PP} transition from 5 V to 12 V or from 12 V to 5 V.
2. Except for sending a Command Program, a Read operation at V_{PP} = 12 V is similar to a Read operation at $V_{PP} = V_{CC}$.
3. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.
4. Addresses are taken in on the falling edge of the Write Enable pulse and latched on the rising edge of the Write Enable pulse during Chip Enable low. Data is latched on the rising edge of the Write Enable pulse during Chip Enable low.

■ PROGRAMMING FLOWCHART

The HN28F101 can be programmed with the fast, high-reliability programming algorithm shown in the following flowchart. This algorithm provides faster programming time without voltage stress to the device or deterioration in reliability of programmed data. Random transition of $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ are not permitted when executing this algorithm.



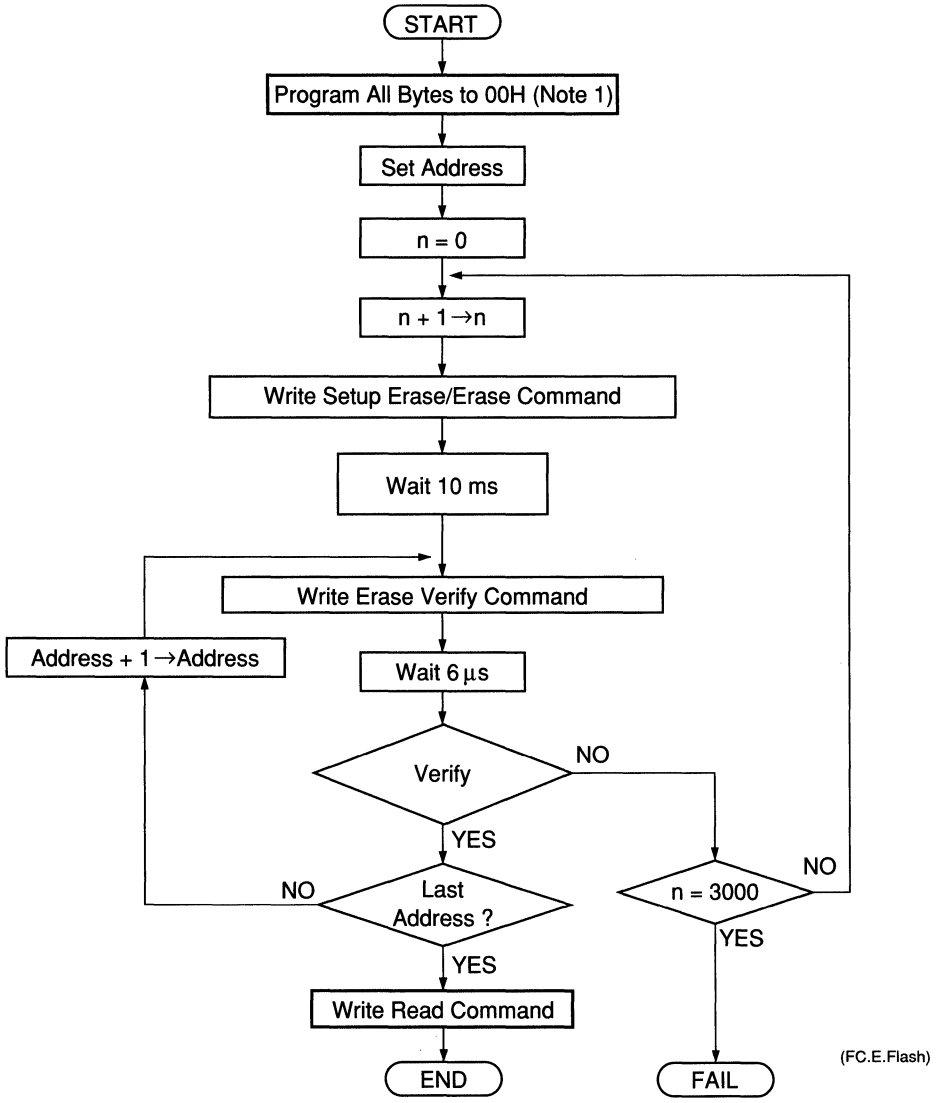
Note: In the case of programming two or more HN28F101 devices simultaneously, the following steps should be applied to the verified devices to avoid over programming:

1. Set-up Program Command: Write FFH
2. Program Command: Write FFH
3. Program Verify Command: Write 00H
4. Program Verify Address: Read Address

(EC P Flash)

■ MANUAL CHIP ERASE FLOWCHART

The HN28F101 can be erased with the fast, high-reliability erase algorithm shown in the following flowchart. This algorithm provides a fast erase time without voltage stress to the device or deterioration in reliability of programmed data. Random transition of $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ are not permitted when executing this algorithm.

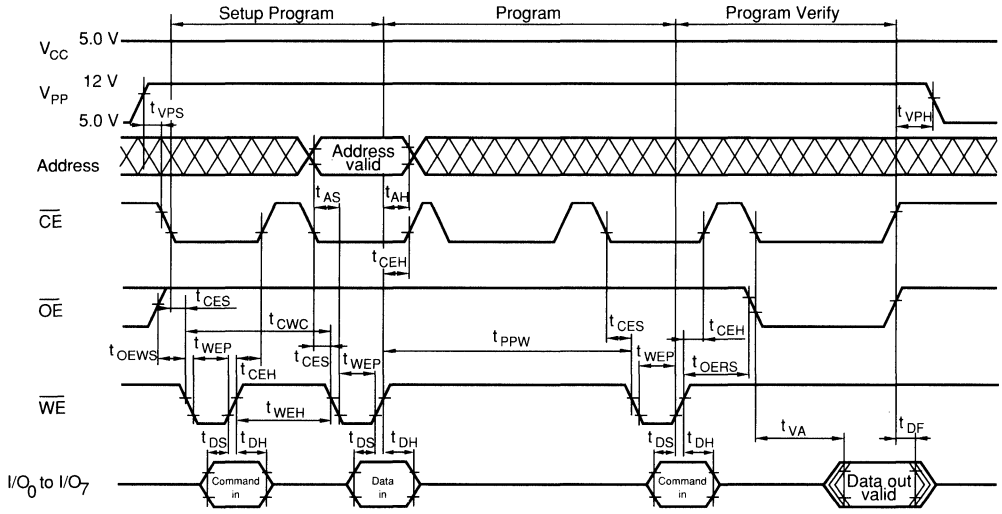


Note 1: Refer to Fast High-Reliability Programming Flowchart.

Note: In the case of erasing two or more HN28F101 devices simultaneously, the following steps should be applied to the verified devices to avoid over erasing:

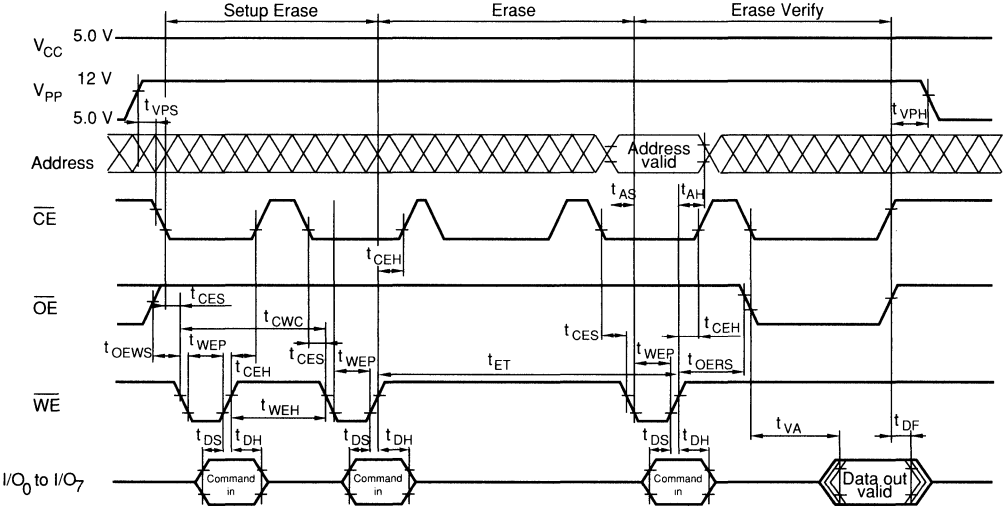
1. Set-up Erase Command: Write A0H
2. Erase Verify Address: Verify Address
3. Erase Command: Write A0H
4. EraseVerify Command: Write A0H

■ PROGRAMMING TIMING WAVEFORM



(TD.P.HN28F101)

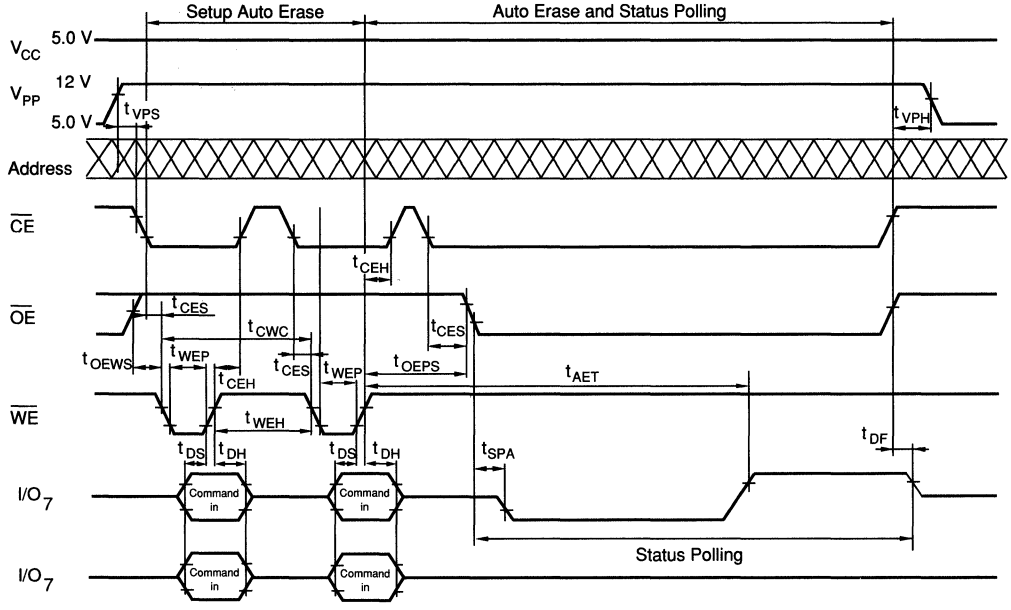
■ MANUAL CHIP ERASE TIMING WAVEFORM



(TD.E.HN28F101)

■ AUTOMATIC CHIP ERASE TIMING WAVEFORM

The fast Automatic Erase algorithm shown in the following timing waveform can be applied. All of the data in the chip is erased. External pre-write and erae verify are not required because the cells are pre-written, erased and verified automatically by internal control circuitry. Erasure completion can be verified by Status Polling after the Automatic Erase starts. Erasure completion can be verified by Status Polling. This algorithm provides a fast erase time without any voltage stress to the device or deterioration in data reliability.



(TD.AE.HN28F101)

■ STATUS POLLING

The HN28F101 features Status Polling as a method to indicate that the embedded algorithms are either in progress or completed. While the Automatic Chip Erase algorithm is in operation, the I/O_7 pin is lowered to V_{OL} until the erase operation is completed. Upon completion of the erase operation, the I/O_7 pin is set to V_{OH}. The Status Polling feature is only active during the Automatic Chip Erase algorithm.

■ DEVICE IDENTIFIER MODE DESCRIPTION

The Device Identifier Mode allows binary codes to be read from the outputs that identify the manufacturer and the type of device. Using this mode with programming equipment, the device will automatically match its own erase and programming algorithm.

■ HN28F101 SERIES IDENTIFIER CODE

Identifier	A_0	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	0	0	0	1	1	0	0	1	19

Notes: The HN28F101 Series Identifier Codes can be read by two methods:

1. Write 90H to the device with $\overline{CE} = V_{IL}$ and $A_0 = \overline{OE} = V_{IH}$ (all other addresses are Don't Care). The Device Code of 19H will appear after the fall of OE. The Manufacturer Code of 07H will appear after A_0 transitions to V_{IL}.
2. Apply 12.0 V ± 0.6 V to A_9 .With $A_0 = V_{IH}$ (all other addresses are LOW), $V_{PP} = V_{CC}$, $\overline{CE} = \overline{OE} = V_{IL}$ and $\overline{WE} = V_{IH}$. The Device Code of 19H will appear. After A_0 transitions to V_{IL} the Manufacturer Code of 07H will appear on the I/O lines.

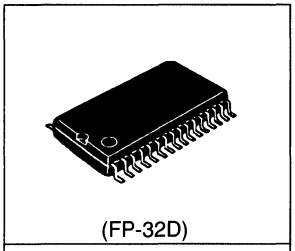
4M (512K x 8-bit) Flash Memory

■ DESCRIPTION

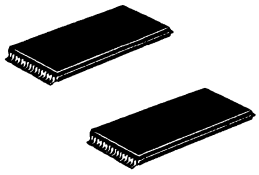
The Hitachi HN29C4001 is a 4-Megabit CMOS Flash Memory organized as 524,288 x 8-bit. The HN29C4001 is capable of in-system electrical chip erasure and reprogramming.

The HN29C4001 programs and erases data with a 12 V V_{PP} supply and a 5 V V_{CC} supply. The HN29C4001 conforms to the JEDEC Standard Dual-Supply EEPROM Command Set.

Hitachi's HN29C4001 is offered in JEDEC-Standard Byte-Wide EPROM pinouts in 32-lead SOP and TSOP packages. This allows an easy upgrade from the HN28F101, 1 Megabit Flash Memory, as well as socket replacement with EPROMs and Mask ROMs. The HN29C4001 TSOP is offered in both standard and reverse bend pinouts.



(FP-32D)



(TFP-32D) and (TFP-32DR)

■ FEATURES

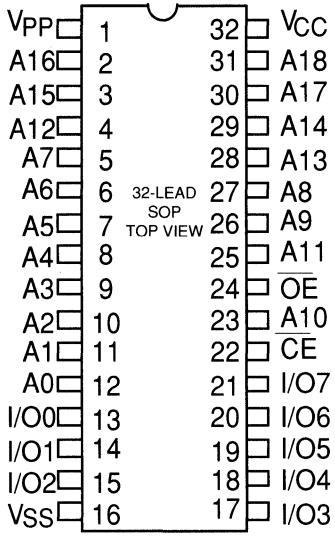
- Dual Power Supply:
  V_{CC} = 5 V ± 10%
  V_{PP} = 12.0 V ± 0.6 V (Erase/Program)
- Fast Access Times:
  150 ns/170 ns (max)
- Low Power Dissipation:
  Read Current: 50 mA (max)
  Standby Current: 20 µA (max)
- Byte Programming:
  Programming Time: 25 µs/Byte (typ)
  Address, Data, Control Latch Function
- Electrical Chip Erase:
  Erase Time: 1 sec (typ)
- Erase Endurance:
  10,000 times (min)
- Pin Arrangement:
  JEDEC Standard Byte-Wide EPROM
  EPROM and Mask ROM Compatible
- Packages:
  32-lead Plastic SOP
  32-lead Plastic TSOP (Type I)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN29C4001FP-15	150 ns	32-lead Plastic SOP
HN29C4001FP-17	170 ns	(FP-32D)
HN29C4001T-15	150 ns	32-lead Plastic TSOP
HN29C4001T-17	170 ns	(TFP-32D)
HN29C4001R-15	150 ns	32-lead Plastic TSOP
HN29C4001R-17	170 ns	(TFP-32DR)
		Reverse bend

■ PIN ARRANGEMENT

HN29C4001FP Series



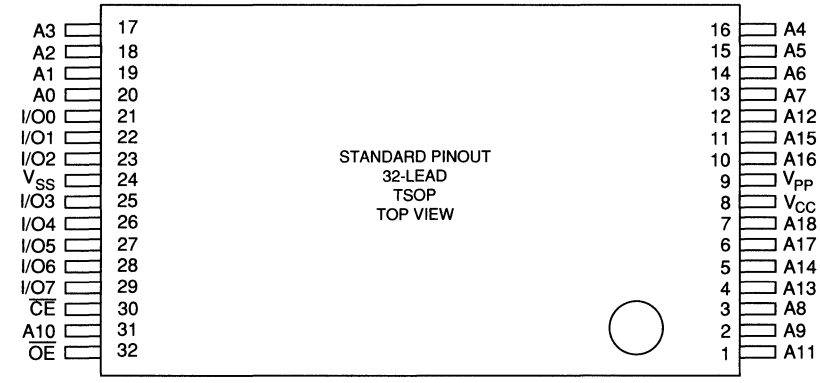
(PinD32.HN28F4001)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{18}	Address
I/O_0 - I/O_7	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{PP}	Programming Supply
V_{SS}	Ground

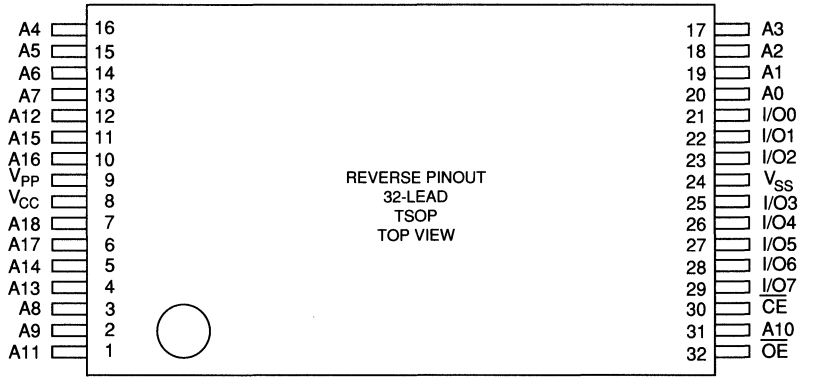
■ PIN ARRANGEMENT (continued)

HN29C4001T Series



(PinT132.HN28F4001T)

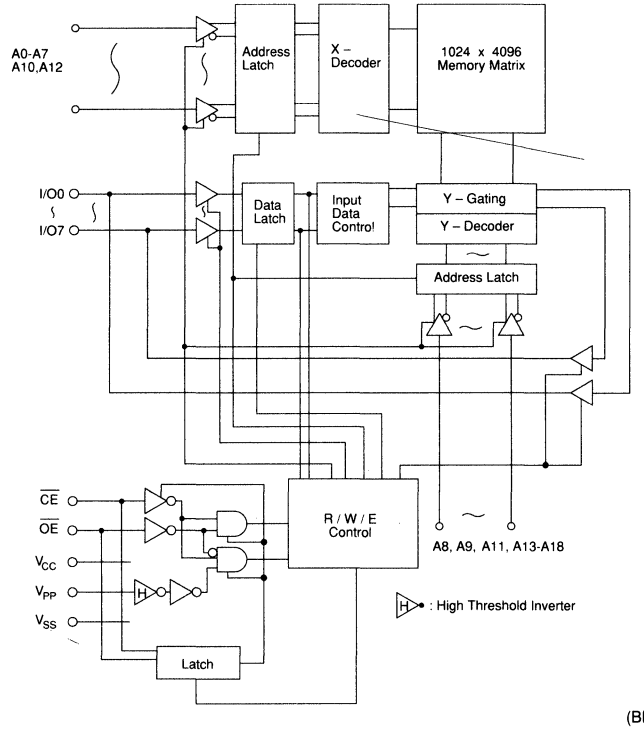
HN29C4001R Series



(PinT132.HN28F4001R)

2

■ BLOCK DIAGRAM



(BD.HN28F4001)

■ MODE SELECTION

Mode		$\overline{CE}$	$\overline{OE}$	A_9	A_0	V_{PP}	I/O_0 to I/O_7
Read	Read	V_{IL}	V_{IL}	A_9	A_0	V_{cc} [6]	D_{OUT}
	Output Disable	V_{IL}	V_{IH}	X	X	V_{cc}	High-Z
	Standby	V_{IH}	X	X	X	V_{cc}	High-Z
	Identifier [1]	V_{IL}	V_{IL}	V_H [2]	V_{IL}	V_{cc}	Code"07"
		V_{IL}	V_{IL}	V_H [2]	V_{IH}	V_{cc}	Code"08"
Command	Read [3,5]	V_{IL}	V_{IL}	A_9	A_0	V_{PP}	D_{OUT}
Program	Standby	V_{IH}	X	X	X	V_{PP}	High-Z
	Write [4]	V_{IL}	V_{IH}	A_9	A_0	V_{PP}	D_{IN}

Notes:
1. Device Identifier Code can be output in Command Program Mode. Refer to Command Address and Data Input Table.
2. $11.4\ V \leq V_H \leq 12.6\ V$
3. Data can also be read when 12 V is applied to V_{PP}. Device Identifier Code can be output by Command Inputs. See Device Identifier Mode Description Table for more details.
4. Refer to Command Address and Data Input Table. Data is programmed, erased, or verified after inputting Commands.
5. Status of Programming and Erase can be verified in this mode. Status Outputs on I/O_7. I/O_0 to I/O_6 are in high impedance states.
6. X = Don't Care. $V_{PP} = 0V$ to V_{CC}.

■ COMMAND ADDRESS AND DATA INPUT

Command	Bus Cycles Required	First Cycle			Second Cycle		
		Operation Mode [1]	Address [2]	Data [3]	Operation Mode [1]	Address [2]	Data [3]
Read (Memory) [4]	1	Write	X	00H	Read	RA	D_{OUT}
Read Identifier Codes	2	Write	X	90H	Read	IA	ID
Set-up Chip Erase/ Chip Erase [5]	2	Write	X	20H	Write	X	20H
Reserved [8]	2	Write	X	60H	Write	X	60H
Erase Verify [5]	2	Write	EVA	A0H	Read	X	EVD
Reserved [8]	2	Write	X	30H	Write	X	30H
Reserved [8]	2	Write	X	20H	Write	X	D0H
Setup Program/Program [6]	2	Write	X	40H	Write	PA	PD
Program Verify [6]	2	Write	PA	C0H	Read	X	PVD
Reserved [8]	2	Write	X	10H	Write	X	X
Reset	1 or 2	Write	X	FFH	Write[7]	X	FFH[11]

Notes:
1. Refer to Command Program Mode in Mode Selection about operation mode.
2. Refer to Device Identifier Mode. IA = Identifier Address, PA = Programming Address, EVA = Erase Verify Address, RA = Read Address. Addresses are latched on the rising edge of chip-enable pulse.
3. Refer to Device Identifier Mode. PA are latched by Programming Command. ID = Identifier Output Code, PD = Programming Data, PVD = Programming Verify Output Data, EVD = Erase Verify Output Data.
4. Command latch default value when applying 12 V to V_{PP} is "00H". Device is in Read Mode after V_{PP} is set to 12 V (before other Command is input).
5. All data in the chip is erased. Erase data according to the Manual Chip Erase Flowchart.
6. Program data according to the Manual Programming Flowchart.
7. Write Reset Command twice to exit from program setup state or auto verify program setup state. Write it once to exit from others.
8. Do not write the following Command sequences to the device: 60H + 60H, 30H + 30H, 20H + D_{IN}, 10H + D_{IN}. Data may be destroyed if these Commands are written.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Programming Voltage [1]	V_{PP}	-0.6 to +14.0	V
A_9 Voltage [1,2]	V_{ID}	-0.6 to +13.5	V
All Input and Output Voltage [1,2]	V_{IN}, V_{OUT}	-0.6 to +7.0	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range [3]	T_{STG}	-65 to +125	°C
Storage Temperature Under Bias	T_{BIAS}	-10 to +80	°C

Notes:
1. Relative to V_{SS}.
2. V_{IN}, V_{OUT} and V_{ID} min = -2.0V for pulse width ≤ 20 ns.
3. Device storage temperature range before programming.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Capacitance	C_{IN}	-	-	6	pF	V_{IN} = 0 V
Output Capacitance	C_{OUT}	-	-	12	pF	V_{OUT} = 0V

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Leakage Current	I_{LI}	-	-	2	µA	V_{IN} = V_{SS} to V_{CC}
Output Leakage Current	I_{LO}	-	-	2	µA	V_{OUT} = V_{SS} to V_{CC}
Operating V_{CC} Current	I_{CC1}	-	-	30	mA	I_{OUT} = 0 mA, f = 1 MHz
	I_{CC2}	-	-	50	mA	I_{OUT} = 0 mA, f = 8 MHz
Standby V_{CC} Current	I_{SB1}	-	-	1	mA	$\overline{CE}$ = V_{IH}
	I_{SB2}	-	-	20	µA	$\overline{CE}$ = V_{CC} ± 0.3V
V_{PP} Current	I_{PP1}	-	-	20	µA	V_{PP} = 5.5 V
Input Voltage [3]	V_{IL}	-0.5 [1]	-	0.8	V	
	V_{IH}	2.2 [3]	-	V_{CC} + 0.5 [2]	V	
Output Voltage	V_{OL}	-	-	0.45	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA

Notes:
1. V_{IL} min = -1.0 V for pulse width ≤ 50 ns. V_{IL} min = -2.0 V for pulse width ≤ 20 ns.
2. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns. If V_{IH} is over the specified maximum value, Read operation can not be guaranteed.
3. Only defined for DC and long cycle function test. V_{IL} max = 0.4 V, V_{IH} min = 3.0 V for AC function test.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

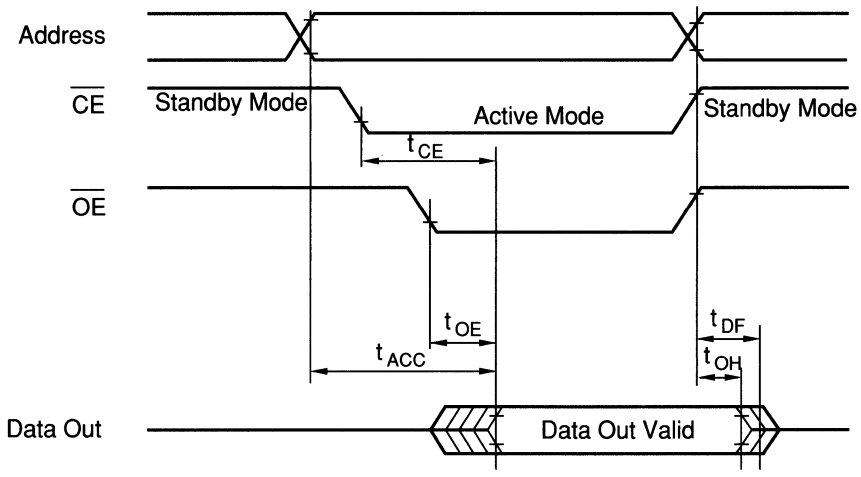
Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V, 2.0 V

Item	Symbol	HN29C4001-15		HN29C4001-17		Unit	Test Conditions
		Min.	Max.	Min.	Max.		
Address Access Time	t_{ACC}	-	150	-	170	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
Chip Enable Access Time	t_{CE}	-	150	-	170	ns	$\overline{OE}$ = V_{IL}
Output Enable Access Time	t_{OE}	-	70	-	70	ns	$\overline{CE}$ = V_{IL}
Output Disable to High-Z [1]	t_{DF}	0	50	0	60	ns	$\overline{CE}$ = V_{IL}
Output Hold to Address Change	t_{OH}	5	-	5	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



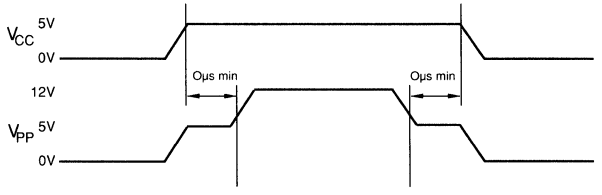
(TD.R.HN28F4001)

■ DC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING AND ERASE OPERATIONS

(V_{CC} = 5V ± 10%, V_{PP} = 12.0 V ± 0.6 V, T_a = 0 to +70°C)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Leakage Current		I_{LI}	-	-	2	µA	$V_{IN} = V_{SS}$ to V_{CC}
Output Leakage Current		I_{LO}	-	-	2	µA	$V_{OUT} = V_{SS}$ to V_{CC}
Operating V_{CC} Current	Read	I_{CC1}	-	-	30	mA	I_{OUT} = 0 mA, f = 1 MHz
		I_{CC2}	-	-	50	mA	I_{OUT} = 0 mA, f = 8 MHz
	Program	I_{CC3}	-	-	30	mA	Programming
	Erase	I_{CC4}	-	-	30	mA	Erasing
	Program Verify	I_{CC5}	-	-	15	mA	Programming Verify
	Erase Verify	I_{CC6}	-	-	15	mA	Erase Verify
Standby V_{CC} Current		I_{SB1}	-	-	1	mA	$\overline{CE} = V_{IH}$
		I_{SB2}	-	-	200	µA	$\overline{CE} = V_{CC} \pm 0.3$ V
V_{PP} Current	Read	I_{PP1}	-	-	200	µA	V_{PP} = 12.6 V
	Program	I_{PP2}	-	-	50	mA	Programming
	Erase	I_{PP3}	-	-	80	mA	Erasing
	Program Verify	I_{PP4}	-	-	10	mA	Program Verify
	Erase Verify	I_{CC5}	-	-	10	mA	Erase Verify
Input Voltage		V_{IL}	-0.5 [5]	-	0.8	V	
		V_{IH}	2.2[7]	-	V_{CC} + 0.5[6]	V	
Output Voltage		V_{OL}	-	-	0.45	V	I_{OL} = 2.1 mA
		V_{OH}	2.4	-	-	V	I_{OH} = -400 µA

Notes: 1. V_{CC}/V_{PP} power on/off timing: V_{CC} must be applied before or simultaneously with V_{PP}, and removed after or simultaneously with V_{PP}. These conditions must be satisfied at power on and off caused by power failure to the device.



2. V_{PP} must not exceed 14 V, including overshoot.
3. Device reliability may be adversely affected if the device is installed or removed while V_{PP} = 12 V.
4. When $\overline{CE} = V_{IL}$, do not change V_{PP} from V_{IL} to 12 V or 12 V to V_{IL}.
5. V_{IL} min = -1.0 V for pulse width ≤ 20 ns.
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.
7. Only defined for DC and long cycle function test. V_{IL} max = 0.4 V, V_{IH} min = 3.0 V for AC function test.

■ AC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING AND ERASE OPERATIONS

(V_{CC} = 5V ± 10%, V_{PP} = 12.0 v ± 0.6 V, T_a = 0 to 70°C)

Test Conditions

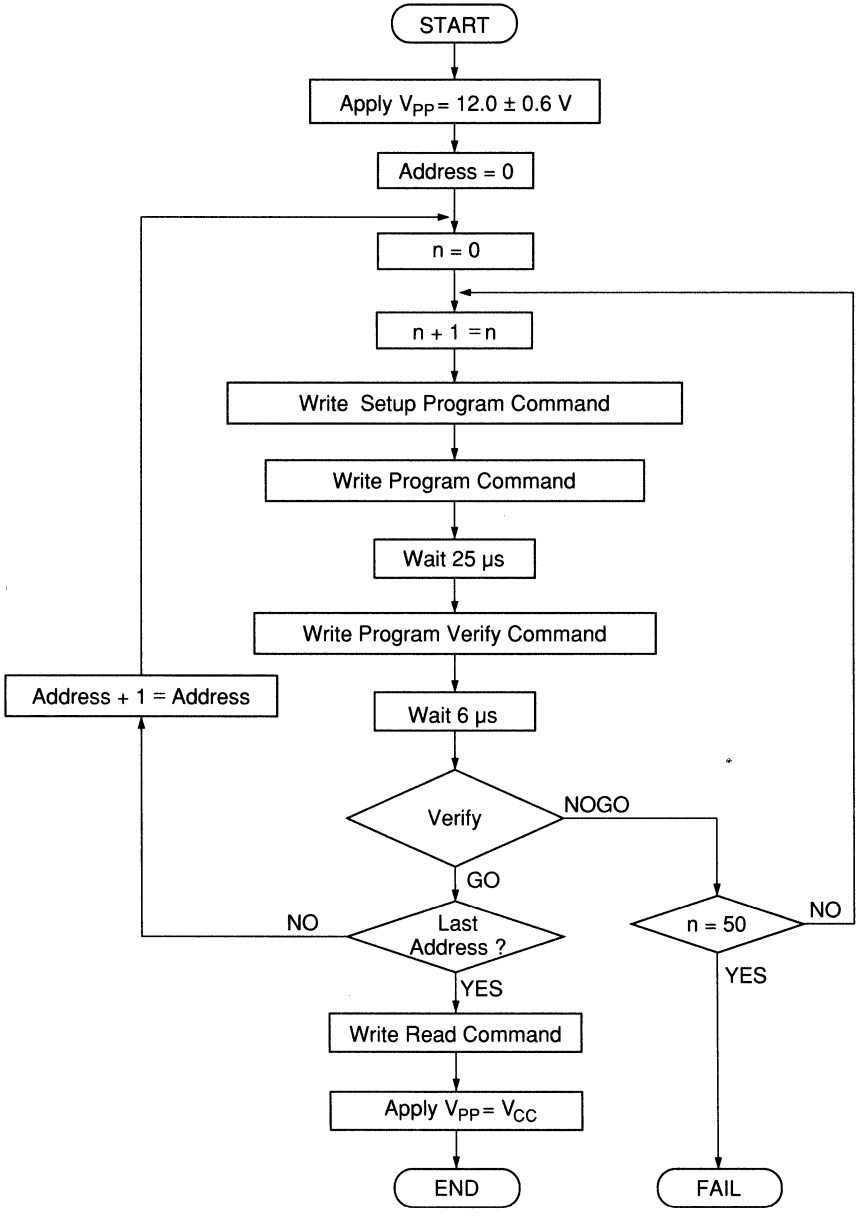
- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V, 2.0V

Item	Symbol	HN29C4001-15		HN29C4001-15		Unit	
		Min.	Max.	Min.	Max.		
V_{PP} Setup Time	t_{VPS}	100	-	100	-	ns	
Output Enable Setup Time	t_{OES}	100	-	100	-	ns	
$\overline{OE}$ Setup after Command	t_{OESA}	6	-	6	-	µs	
$\overline{CE}$ Setup after Command	t_{CESA}	6	-	6	-	µs	
Chip Enable Hold Time	t_{CEH}	60	-	60	-	ns	
Chip Enable Pulse Width	t_{CEP}	60	-	60	-	ns	
Address Setup Time	t_{AS}	50	-	50	-	ns	
Address Hold Time	t_{AH}	20	-	20	-	ns	
Data Setup Time	t_{DS}	50	-	50	-	ns	
Data Hold Time	t_{DH}	20	-	20	-	ns	
Chip Enable Setup Time before Command Write	t_{CESC}	100	-	100	-	ns	
$\overline{CE}$ Setup before Verify	t_{CESV}	6	-	6	-	µs	
$\overline{OE}$ Setup before Verify	t_{OESV}	6	-	6	-	µs	
V_{PP} Hold Time	t_{VPH}	100	-	100	-	ns	
Standby Time Before Programming	t_{PPW}	25	-	25	-	µs	
Erase Standby Time [2]	t_{ET}	0.95	-	0.95	-	ms	

Notes: 1. $\overline{CE}$ and $\overline{OE}$ must be fixed high during V_{PP} transition from 5 V to 12 V or from 12 V to 5 V.
2. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

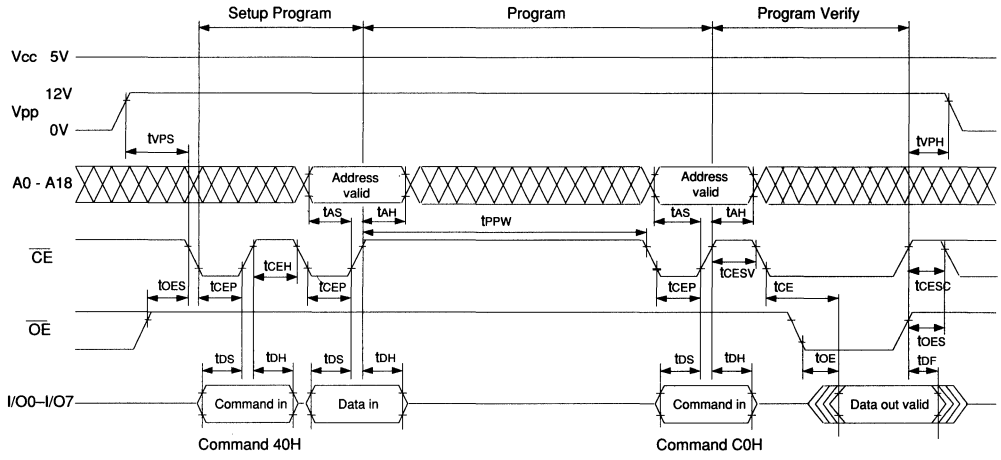
■ MANUAL PROGRAMMING FLOWCHART

The HN29C4001 can be programmed with the fast, high-reliability programming algorithm shown in the following flowchart. This algorithm provides fast programming time without any voltage stress to the device or deterioration in reliability of programmed data.



(FC.P.HN29C4001)

■ MANUAL PROGRAMMING TIMING WAVEFORM

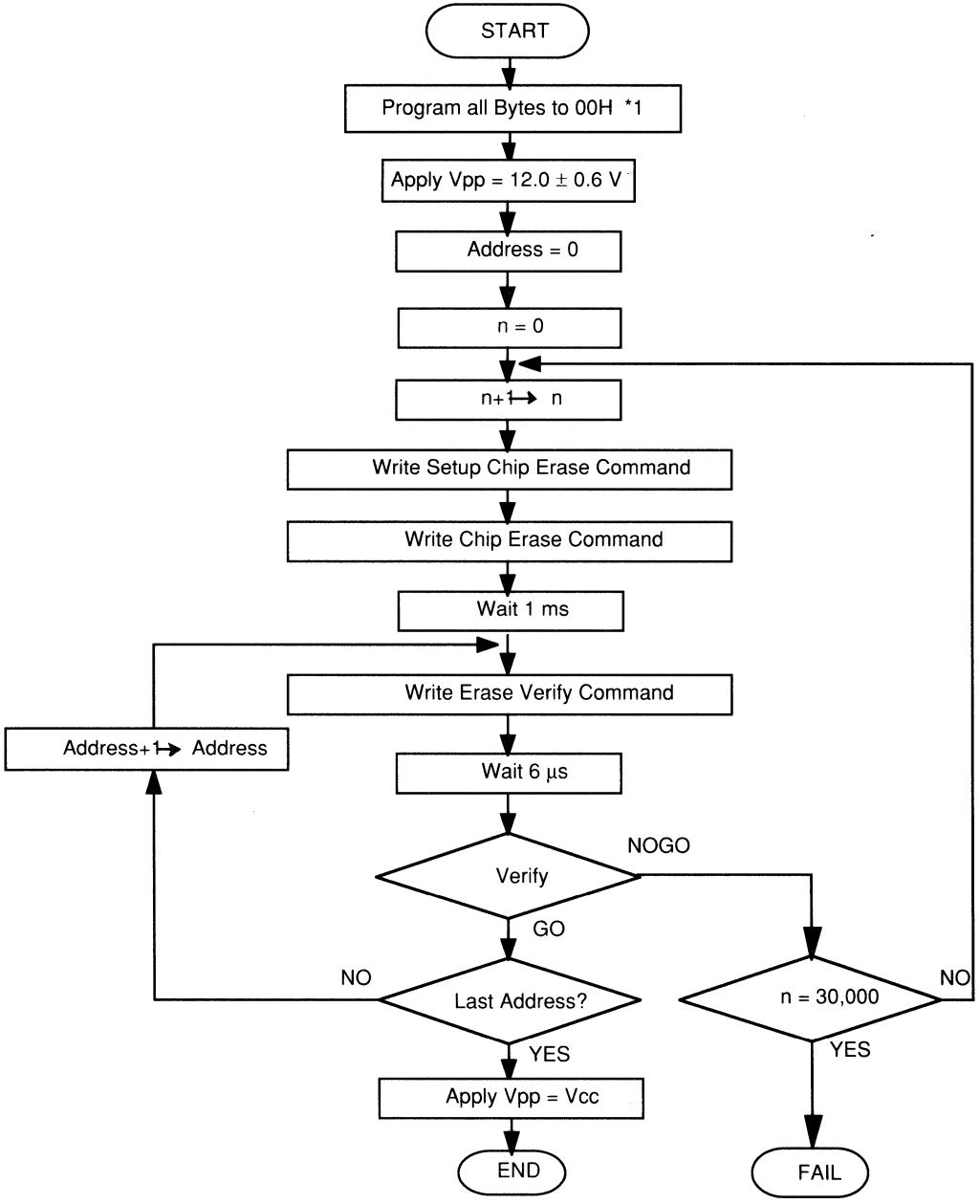


(TD.MP.HN28F4001)

2

■ MANUAL CHIP ERASE FLOWCHART

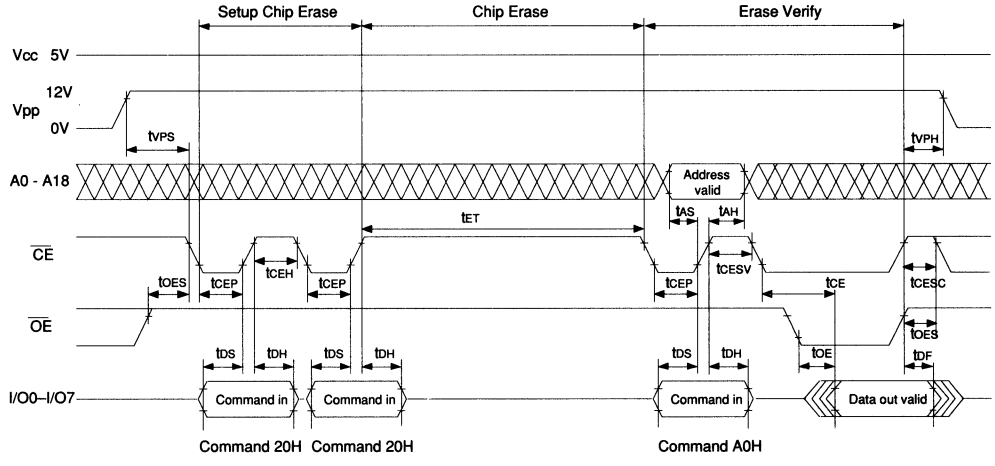
The HN29C4001 can be erased with the fast, high-reliability chip erase algorithm shown in the following flowchart. This algorithm provides a fast erase time without any voltage stress to the device or deterioration in data reliability.



*1. Refer to Manual Programming Flowchart

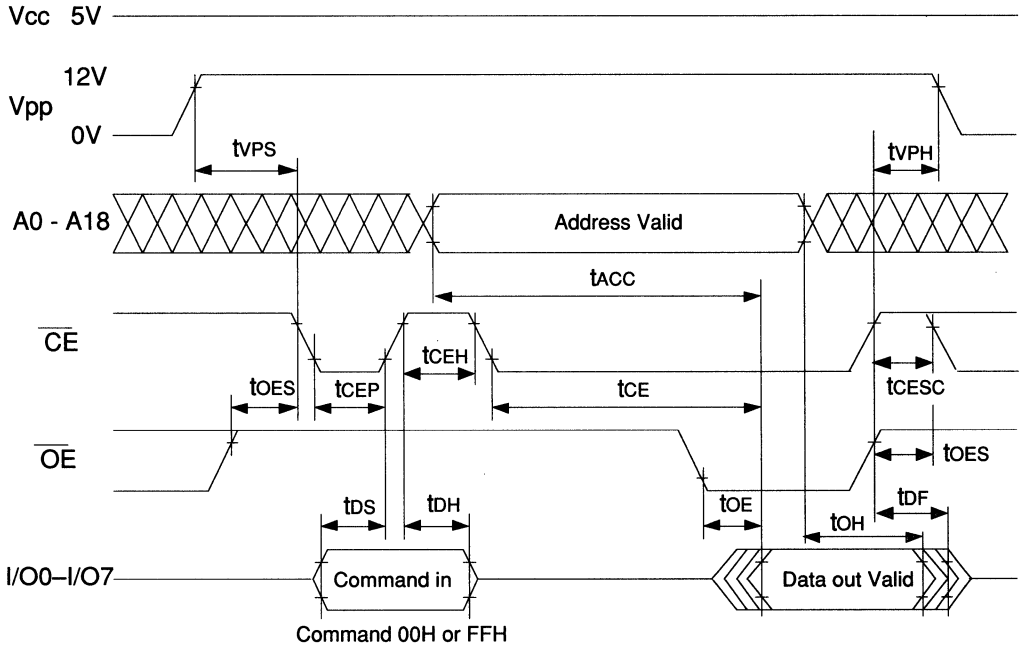
(FC.CE.HN29C4001)

■ MANUAL CHIP ERASE TIMING WAVEFORM



(TD.CE.HN28F4001)

■ READ TIMING WAVEFORM (V_{PP} APPLIED)



(TD.RTW.HN28F4001)

■ DEVICE IDENTIFIER MODE DESCRIPTION

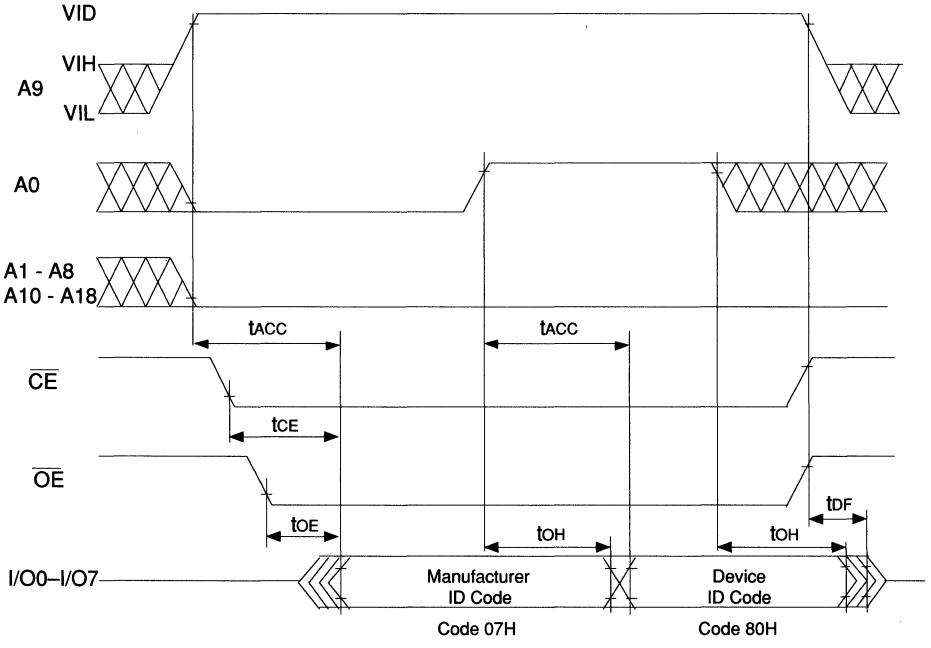
The Device Identifier Mode allows binary codes to be read from the outputs that identify the manufacturer and the type of device. Using this mode with programming equipment, the device will automatically match its own erase and programming algorithm.

■ HN28F4001 SERIES IDENTIFIER CODE

Identifier	A_0	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	1	0	0	0	0	0	0	0	80

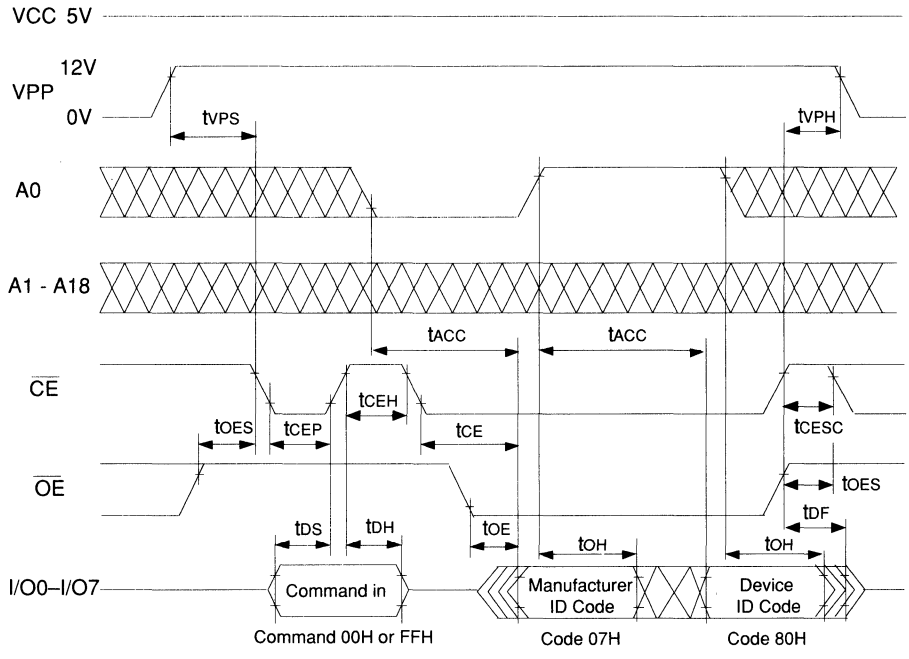
Notes:
1. Device identifier code can be read out by applying 12.0 V ± 0.5 V to A9 when V_{PP}=V_{CC}, or inputting command while V_{PP}=12 V.
2. V_{CC} = V_{PP}=5.0 V ± 10% when applying 12 V to A9.
   V_{CC} =5.0 V ± 10% and V_{PP}=12.0 V ± 0.6 V in command inputs.
3. A1 to A8, A10 to A18, $\overline{CE}$, and $\overline{OE}$ = V_{IL}.

■ IDENTIFIER CODE READ TIMING WAVEFORM (V_{PP} = V_{SS} to V_{CC})



(TD.ID1.HN28F4001)

■ IDENTIFIER CODE READ TIMING WAVEFORM (V_{PP} = 12V)



(TD.ID2.HN28F4001)

4M (512K x 8-bit) Flash Memory

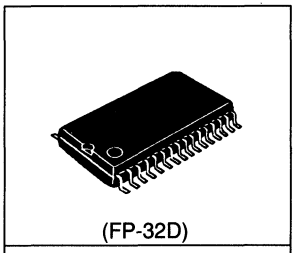
■ DESCRIPTION

The Hitachi HN28F4001 is a 4-Megabit CMOS Flash Memory organized as 524,288 x 8-bit. The HN28F4001 is capable of in-system electrical chip and block erasure and reprogramming.

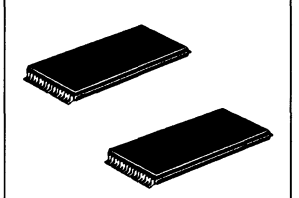
The HN28F4001 programs and erases data with a 12 V V_{PP} supply and a 5 V V_{CC} supply. The HN28F4001 conforms to the JEDEC Standard Dual-Supply EEPROM Command Set. Its Automatic Commands do not require complicated external control to program or erase data because of its automatic verify programming, chip erase and block erase functions.

The block architecture of the HN28F4001 segments the device into 32 blocks of 16KBytes each. This feature allows the user to erase and reprogram one random block of data and more than one block of data simultaneously.

Hitachi's HN28F4001 is offered in JEDEC-Standard Byte-Wide EPROM pinouts in 32-lead SOP and TSOP packages. This allows an easy upgrade from the HN28F101, 1 Megabit Flash Memory, as well as socket replacement with EPROMs and Mask ROMs. The HN28F4001 TSOP is offered in both standard and reverse bend pinouts.



(FP-32D)



(TFP-32D) and (TFP-32DR)

■ FEATURES

- Dual Power Supply:
  V_{CC} = 5 V ± 10%
  V_{PP} = 12.0 V ± 0.6 V (Erase/Program)
- Fast Access Times:
  120 ns/150 ns/170 ns (max)
- Low Power Dissipation:
  Read Current: 50 mA (max)
  Standby Current: 20 µA (max)
- Automatic Byte Programming:
  Programming Time: 10 µs/Byte (typ)
  Address, Data, Control Latch Function
  Internal Automatic Program Verify
  Data Polling Function
- Automatic Chip and Block Erase:
  Erase Time: 1 sec (typ)
  Internal Pre-Write and Erase Verify
  Status Polling Function
- Block Architecture:
  Block Size: 16KBytes x 32 Blocks
  Simultaneous Erase of Multiple Blocks
- Erase Endurance:
  10,000 times (min)
- Pin Arrangement:
  JEDEC Standard Byte-Wide EPROM
  EPROM and Mask ROM Compatible
- Packages:
  32-lead Plastic SOP
  32-lead Plastic TSOP (Type I)

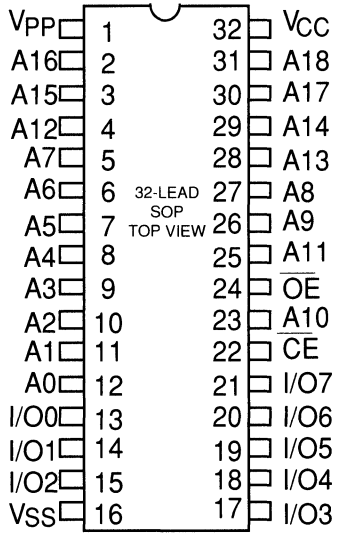
■ ORDERING INFORMATION

Type No.	Access Time	Package
HN28F4001FP-12	120 ns	32-lead Plastic SOP
HN28F4001FP-15	150 ns	(FP-32D)
HN28F4001FP-17	170 ns	
HN28F4001T-12	120 ns	32-lead Plastic TSOP
HN28F4001T-15	150 ns	(TFP-32D)
HN28F4001T-17	170 ns	
HN28F4001R-12	120 ns	32-lead Plastic TSOP
HN28F4001R-15	150 ns	(TFP-32DR)
HN28F4001R-17	170 ns	Reverse bend

2

■ PIN ARRANGEMENT

HN28F4001FP Series



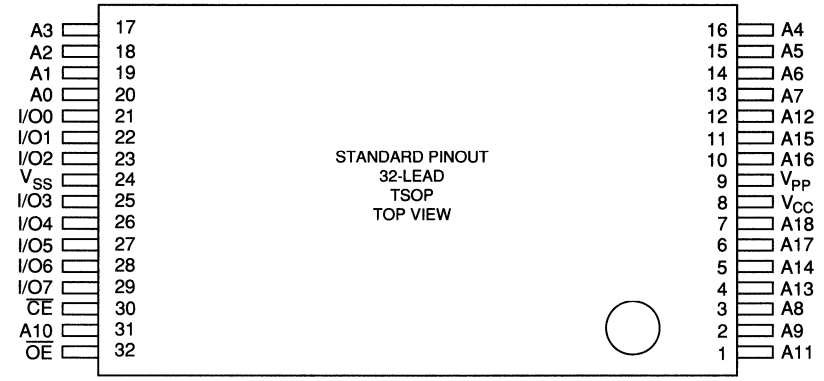
(PinD32.HN28F4001)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{18}	Address
I/O_0 - I/O_7	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{PP}	Programming Supply
V_{SS}	Ground

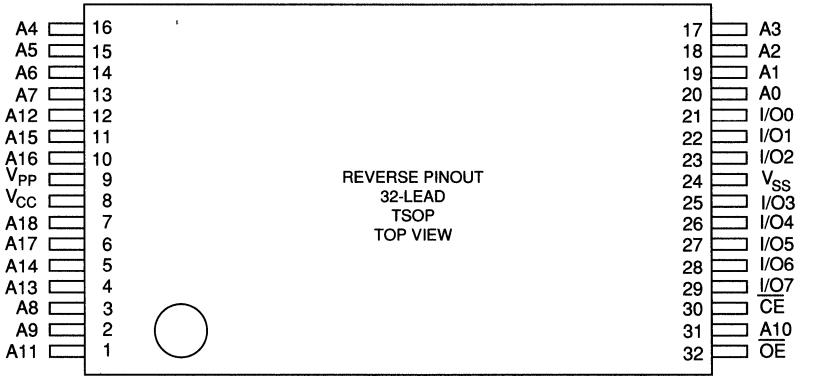
■ PIN ARRANGEMENT (continued)

HN28F4001T Series



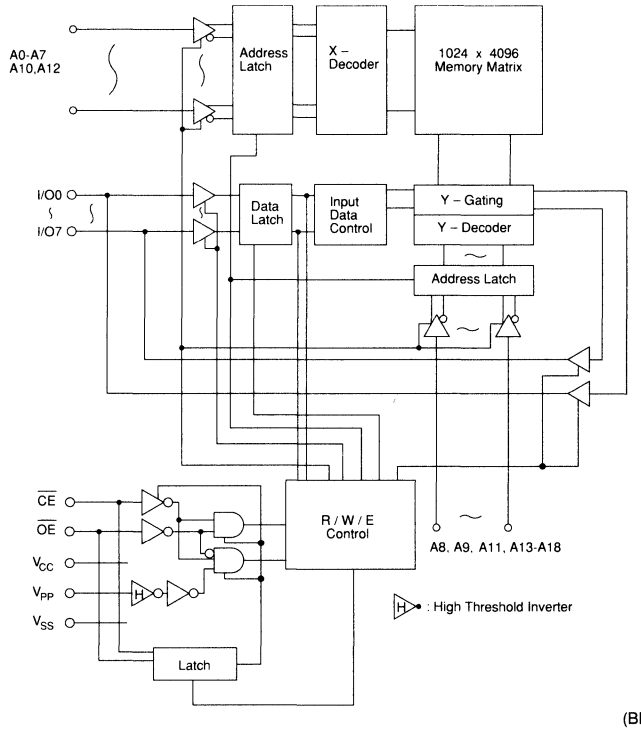
(PinT132.HN28F4001T)

HN28F4001R Series



(PinT132.HN28F4001R)

■ BLOCK DIAGRAM



(BD.HN28F4001)

■ MODE SELECTION

Mode		$\overline{CE}$	$\overline{OE}$	A_9	A_0	V_{PP}	I/O_0 to I/O_7
Read	Read	V_{IL}	V_{IL}	A_9	A_0	V_{cc} [6]	D_{OUT}
	Output Disable	V_{IL}	V_{IH}	X	X	V_{cc}	High-Z
	Standby	V_{IH}	X	X	X	V_{cc}	High-Z
	Identifier [1]	V_{IL}	V_{IL}	V_H [2]	V_{IL}	V_{cc}	Code"07"
		V_{IL}	V_{IL}	V_H [2]	V_{IH}	V_{cc}	Code"08"
Command	Read [3,5]	V_{IL}	V_{IL}	A_9	A_0	V_{PP}	D_{OUT}
Program	Standby	V_{IH}	X	X	X	V_{PP}	High-Z
	Write [4]	V_{IL}	V_{IH}	A_9	A_0	V_{PP}	D_{IN}

Notes:
1. Device Identifier Code can be output in Command Program Mode. Refer to Command Address and Data Input Table.
2. $11.4\ V \leq V_H \leq 12.6\ V$
3. Data can also be read when 12 V is applied to V_{PP}. Device Identifier Code can be output by Command Inputs. See Device Identifier Mode Description Table for more details.
4. Refer to Command Address and Data Input Table. Data is programmed, erased, or verified after inputting Commands.
5. Status of Programming and Erase can be verified in this mode. Status Outputs on I/O_7. I/O_0 to I/O_6 are in high impedance states.
6. X = Don't Care. V_{PP} = 0V to V_{CC}.

■ COMMAND ADDRESS AND DATA INPUT

Command	Bus Cycles Required	First Cycle			Second Cycle		
		Operation Mode [1]	Address [2]	Data [3]	Operation Mode [1]	Address [2]	Data [3]
Read (Memory) [4]	1	Write	X	00H	Read	RA	D_{OUT}
Read Identifier Codes	2	Write	X	90H	Read	IA	ID
Set-up Chip Erase/ Chip Erase [5]	2	Write	X	20H	Write	X	20H
Set-up Block Erase/ Block Erase [8]	2	Write	X	60H	Write	BA	60H
Erase Verify [5]	2	Write	EVA	A0H	Read	X	EVD
Setup Auto Chip Erase/ Auto Chip Erase [6]	2	Write	X	30H	Write	X	30H
Setup Auto Block Erase/ Auto Block Erase [9]	2	Write	X	20H	Write	BA	D0H
Setup Program/Program [7]	2	Write	X	40H	Write	PA	PD
Program Verify [7]	2	Write	PA	C0H	Read	X	PVD
Setup Auto Program/ Auto Program [10]	2	Write	X	10H	Write	PA	PD
Reset	1 or 2	Write	X	FFH	Write[11]	X	FFH[11]

Notes:
1. Refer to Command Program Mode in Mode Selection about operation mode.
2. Refer to Device Identifier Mode. IA = Identifier Address, PA = Programming Address, EVA = Erase Verify Address, RA = Read Address, BA = Block Address. Addresses are latched on the rising edge of chip-enable pulse.
3. Refer to Device Identifier Mode. PA are latched by Programming Command. ID = Identifier Output Code, PD = Programming Data, PVD = Programming Verify Output Data, EVD = Erase Verify Output Data.
4. Command latch default value when applying 12 V to V_{PP} is "00H". Device is in Read Mode after V_{PP} is set to 12 V (before other Command is input).
5. All data in the chip is erased. Erase data according to the Manual Chip Erase Flowchart.
6. All data in the chip is erased. Data is automatically programmed to 00H and erased by internal logic circuitry. External Manual Erase Verify is not required. Erasure completion must be verified by Status Polling on I/O_7.
7. Program data according to the Manual Programming Flowchart.
8. Block data indicated by BA is erased. Erase data according to the Manual Block Erase Flowchart.
9. Block data indicated by BA is erased. Data is automatically programmed to 00H and erased by internal logic circuitry. External Manual Erase Verify is not required. Erasure completion must be verified by Status Polling on I/O_7.
10. One Byte of data is programmed. Data is programmed automatically by internal logic circuit. External program verify is not required. Program completion must be verified by Data Polling on I/O_7.
11. Write Reset Command twice to exit from program setup state or auto verify program setup state. Write it once to exit from others.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Programming Voltage [1]	V_{PP}	-0.6 to +14.0	V
A_9 Voltage [1,2]	V_{ID}	-0.6 to +13.5	V
All Input and Output Voltage [1,2]	V_{IN}, V_{OUT}	-0.6 to +7.0	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range [3]	T_{STG}	-65 to +125	°C
Storage Temperature Under Bias	T_{BIAS}	-10 to +80	°C

Notes: 1. Relative to V_{SS}.
2. V_{IN}, V_{OUT} and V_{ID} min = -2.0V for pulse width ≤ 20 ns.
3. Device storage temperature range before programming.

2

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Capacitance	C_{IN}	-	-	6	pF	V_{IN} = 0 V
Output Capacitance	C_{OUT}	-	-	12	pF	V_{OUT} = 0V

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Leakage Current	I_{LI}	-	-	2	µA	V_{IN} = V_{SS} to V_{CC}
Output Leakage Current	I_{LO}	-	-	2	µA	V_{OUT} = V_{SS} to V_{CC}
Operating V_{CC} Current	I_{CC1}	-	-	30	mA	I_{OUT} = 0 mA, f = 1 MHz
	I_{CC2}	-	-	50	mA	$\overline{I_{OUT}}$ = 0 mA, f = 8 MHz
Standby V_{CC} Current	I_{SB1}	-	-	1	mA	$\overline{CE}$ = V_{IH}
	I_{SB2}	-	-	20	µA	CE = V_{CC} ± 0.3V
V_{PP} Current	I_{PP1}	-	-	20	µA	V_{PP} = 5.5 V
Input Voltage [3]	V_{IL}	-0.5 [1]	-	0.8	V	
	V_{IH}	2.2	-	V_{CC} + 0.5 [2]	V	
Output Voltage	V_{OL}	-	-	0.45	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA

Notes: 1. V_{IL} min = -1.0 V for pulse width ≤ 50 ns. V_{IL} min = -2.0 V for pulse width ≤ 20 ns.
2. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns. If V_{IH} is over the specified maximum value, Read operation can not be guaranteed.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

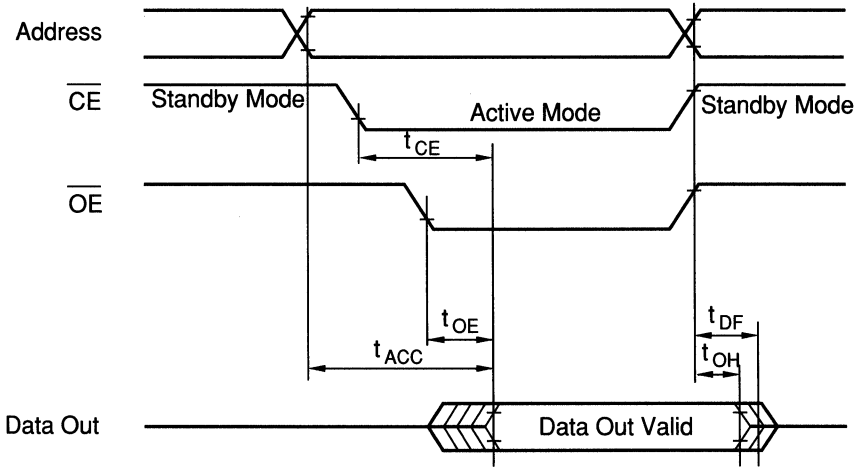
Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V, 2.0 V

Item	Symbol	HN28F4001-12		HN28F4001-15		HN28F4001-17		Unit	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
Address Access Time	t_{ACC}	-	120	-	150	-	170	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
Chip Enable Access Time	t_{CE}	-	120	-	150	-	170	ns	$\overline{OE}$ = V_{IL}
Output Enable Access Time	t_{OE}	-	60	-	70	-	70	ns	$\overline{CE}$ = V_{IL}
Output Disable to High-Z[1]	t_{DF}	0	30	0	35	0	40	ns	$\overline{CE}$ = V_{IL}
Output Hold to Address Change	t_{OH}	5	-	5	-	5	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



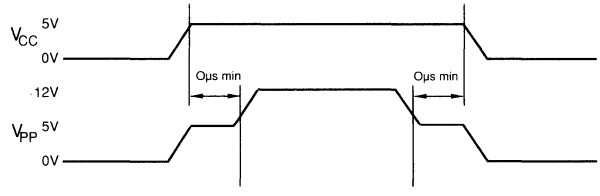
(TD.R.HN28F4001)

■ DC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING AND ERASE OPERATIONS

(V_{CC} = 5V ± 10%, V_{PP} = 12.0 V ± 0.6 V, T_a = 0 to +70°C)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Leakage Current		I_{LI}	-	-	2	µA	$V_{IN} = V_{SS}$ to V_{CC}
Output Leakage Current		I_{LO}	-	-	2	µA	$V_{OUT} = V_{SS}$ to V_{CC}
Operating V_{CC} Current	Read	I_{CC1}	-	-	30	mA	I_{OUT} = 0 mA, f = 1 MHz
		I_{CC2}	-	-	50	mA	I_{OUT} = 0 mA, f = 8 MHz
	Program	I_{CC3}	-	-	30	mA	Programming
	Erase	I_{CC4}	-	-	30	mA	Erasing
	Program Verify	I_{CC5}	-	-	15	mA	Programming Verify
	Erase Verify	I_{CC6}	-	-	15	mA	Erase Verify
Standby V_{CC} Current		I_{SB1}	-	-	1	mA	$\overline{CE} = V_{IH}$
		I_{SB2}	-	-	20	µA	$\overline{CE} = V_{CC} \pm 0.3$ V
V_{PP} Current	Read	I_{PP1}	-	-	20	µA	V_{PP} = 12.6 V
	Program	I_{PP2}	-	-	50	mA	Programming
	Erase	I_{PP3}	-	-	50	mA	Automatic Erase
	Program Verify	I_{PP4}	-	-	10	mA	Programming Verify
	Erase Verify	I_{CC5}	-	-	10	mA	Erase Verify
Input Voltage		V_{IL}	-0.5 [5]	-	0.8	V	
		V_{IH}	2.2	-	V_{CC} + 0.5 [6]	V	
Output Voltage		V_{OL}	-	-	0.45	V	I_{OL} = 2.1 mA
		V_{OH}	2.4	-	-	V	I_{OH} = -400 µA

Notes: 1. V_{CC}/V_{PP} power on/off timing: V_{CC} must be applied before or simultaneously with V_{PP}, and removed after or simultaneously with V_{PP}. These conditions must be satisfied at power on and off caused by power failure to the device.



2. V_{PP} must not exceed 14 V, including overshoot.
3. Device reliability may be adversely affected if the device is installed or removed while V_{PP} = 12 V.
4. When $\overline{CE} = V_{IL}$, do not change V_{PP} from V_{IL} to 12 V or 12 V to V_{IL}.
5. V_{IL} min = -1.0 V for pulse width ≤ 20 ns.
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

■ AC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING AND ERASE OPERATIONS

(V_{CC} = 5V ± 10%, V_{PP} = 12.0 v ± 0.6 V, T_a = 0 to 70°C)

Test Conditions

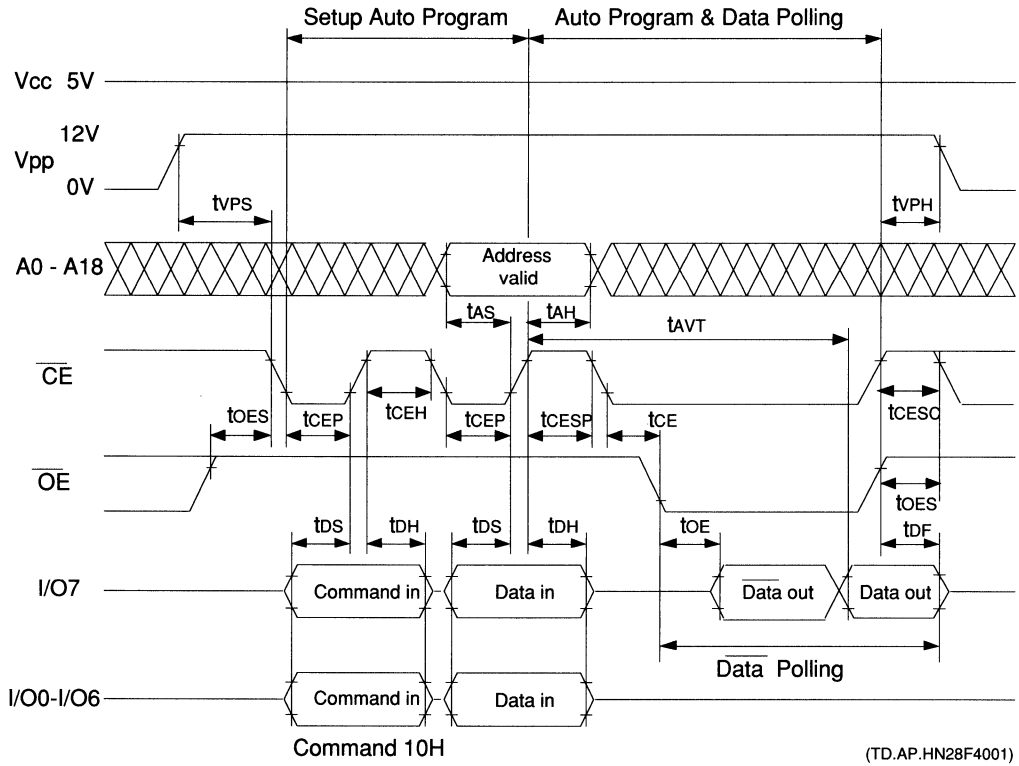
- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V, 2.0V

Item	Symbol	HN28F4001-12		HN28F4001-15		HN28F4001-17		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
V_{PP} Setup Time	t_{VPS}	100	-	100	-	100	-	ns
Output Enable Setup Time	t_{OES}	100	-	100	-	100	-	ns
Chip Enable Hold Time	t_{CEH}	40	-	40	-	40	-	ns
Chip Enable Pulse Width	t_{CEP}	50	-	50	-	50	-	ns
Address Setup Time	t_{AS}	50	-	50	-	50	-	ns
Address Hold Time	t_{AH}	10	-	10	-	10	-	ns
Data Setup Time	t_{DS}	50	-	50	-	50	-	ns
Data Hold Time	t_{DH}	10	-	10	-	10	-	ns
$\overline{CE}$ Setup Time before Status Polling	t_{CESP}	120	-	120	-	120	-	ns
Chip Enable Setup Time before Command Write	t_{CESC}	100	-	100	-	100	-	ns
Chip Enable Setup Time before Verify	t_{CESV}	6	-	6	-	6	-	µs
V_{PP} Hold Time	t_{VPH}	100	-	100	-	100	-	ns
Total Auto Chip Erase Time	t_{AETC}	0.5	10	0.5	10	0.5	10	s
Total Auto Block Erase Time	t_{AETB}	0.5	10	0.5	10	0.5	10	s
Total Auto Verify Programming Time	t_{AVT}	10	400	10	400	10	400	µs
Standby Time Before Programming	t_{PPW}	10	-	10	-	10	-	µs
Erase Standby Time	t_{ET}	0.95	-	0.95	-	0.95	-	ms
Block Address Load Cycle	t_{BALC}	0.09	3	0.09	3	0.09	3	µs
Block Address Load Time	t_{BAL}	10	-	10	-	10	-	µs

Notes:
1. $\overline{CE}$ and $\overline{OE}$ must be fixed high during V_{PP} transition from 5 V to 12 V or from 12 V to 5 V.
2. Except for sending a Command Program, a Read operation at V_{PP} = 12 V is similar to a Read operation at $V_{PP} = V_{CC}$.
3. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

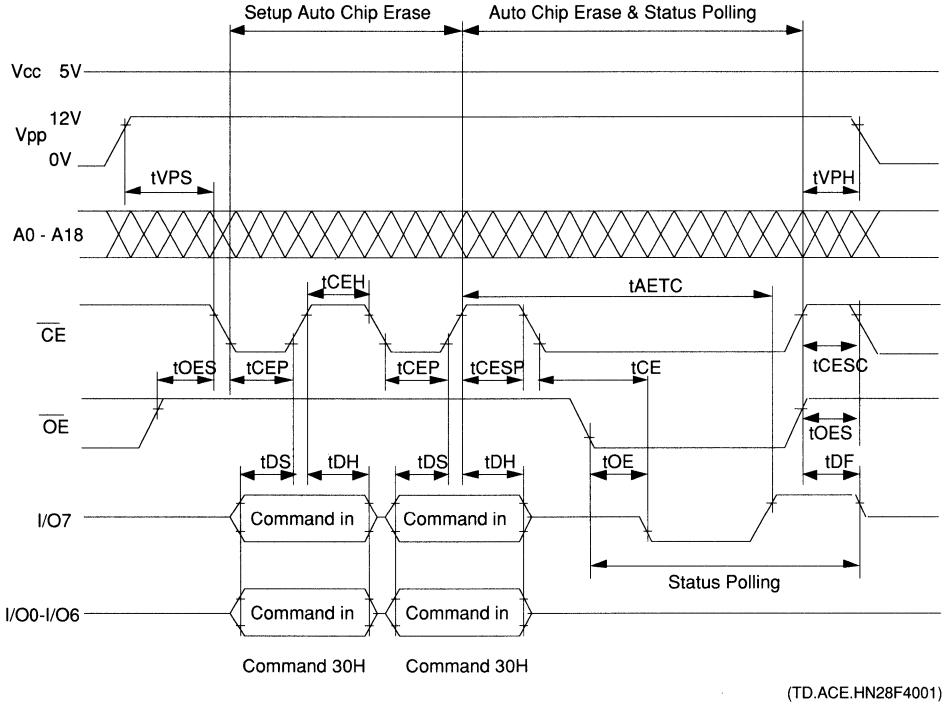
■ AUTOMATIC PROGRAMMING TIMING WAVEFORM

One Byte of data is programmed. External programming verification is not required because these operations are executed automatically by internal control circuitry. Programming completion can be verified by $\overline{\text{Data}}$ Polling after the Automatic Programming starts. Device outputs reverse input data during auto programming on I/O_7. I/O_0 to I/O_6 are high impedance.



■ AUTOMATIC CHIP ERASE TIMING WAVEFORM

The fast Automatic Chip Erase algorithm shown in the following timing waveform can be applied. All of the data in the chip is erased. External pre-write and erase verify are not required because the cells are pre-written and data is erased automatically by internal control circuitry. Erasure completion can be verified by Status Polling after the Automatic Erase starts. This algorithm provides a fast erase time without any voltage stress to the device or deterioration in data reliability.



(TD.ACE.HN28F4001)

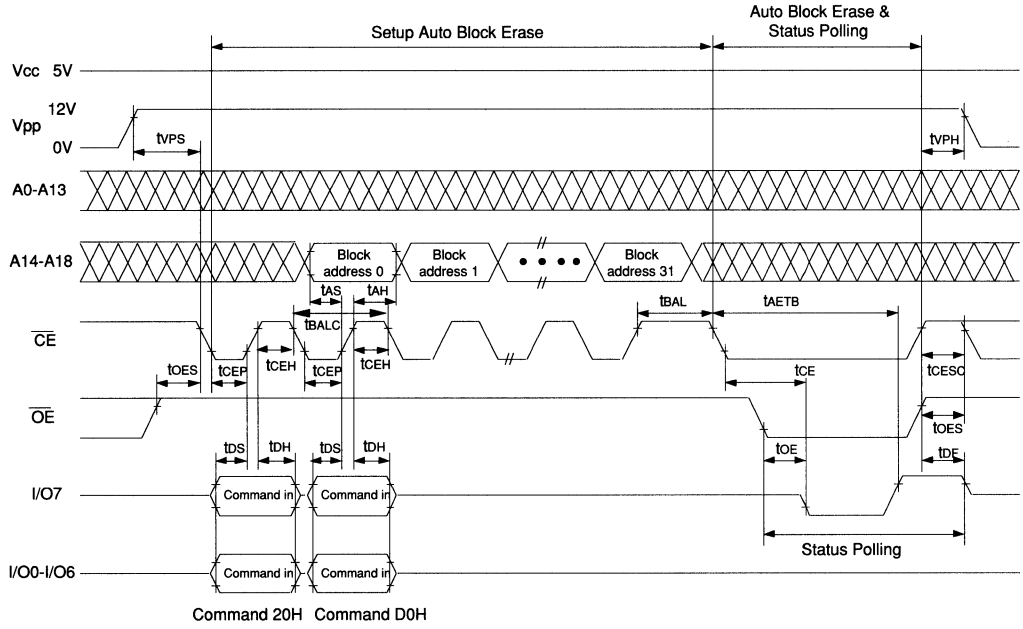
■ STATUS POLLING

The HN28F4001 features Status Polling as a method to indicate that the embedded algorithms are either in progress or completed. While the Automatic Chip or Block Erase algorithm is in operation, the I/O_7 pin is lowered to V_{OL} until the erase operation is completed. Upon completion of the erase operation, the I/O_7 pin is set to V_{OH}.

■ AUTOMATIC BLOCK ERASE TIMING WAVEFORM

The fast Automatic Block Erase algorithm shown in the following timing waveform can be applied. All of the data in the block (16KBytes) indicated by A_{14} to A_{18} is erased. External pre-write and erase verify is not required because the cells are pre-written and data in the block is erased automatically by internal control circuitry. Erasure completion can be verified by Status Polling after the automatic erase starts. This algorithm provides a fast erase time without any voltage stress to the device or deterioration in data reliability.

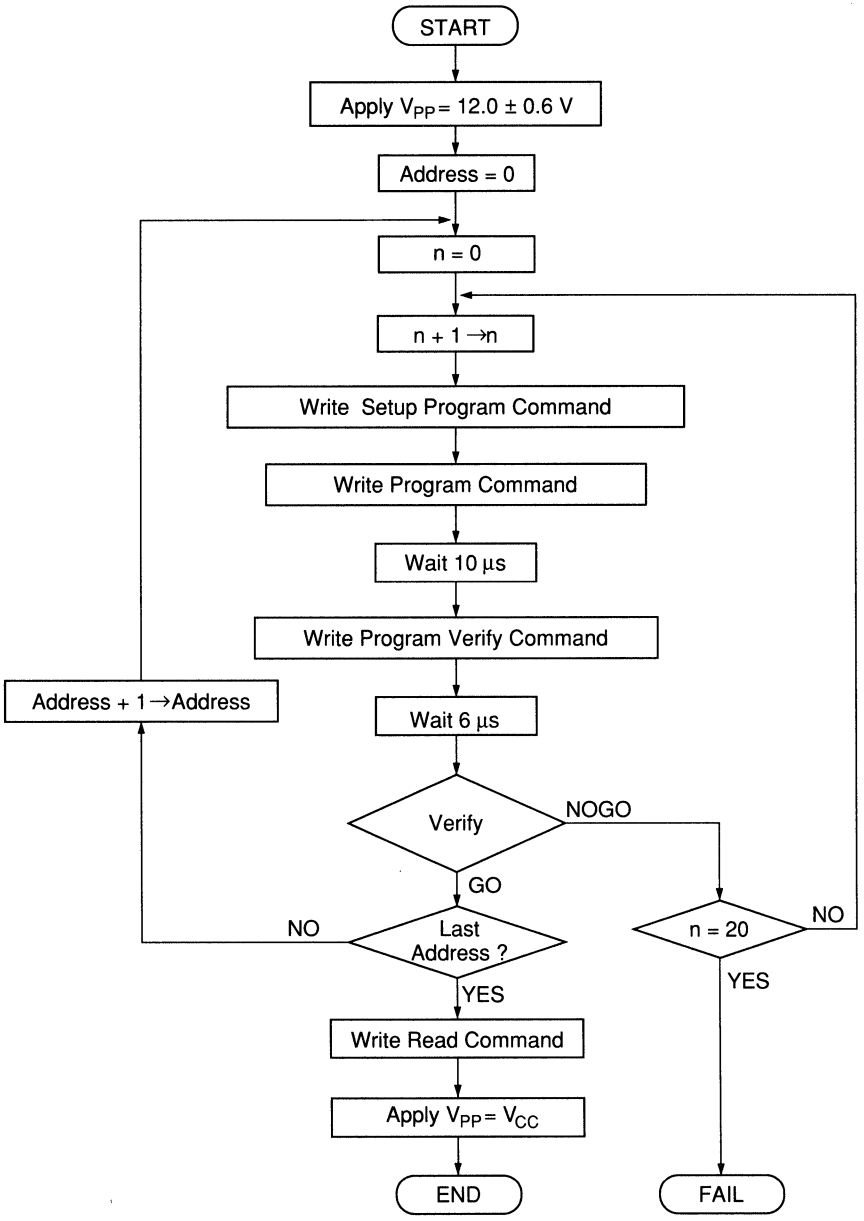
As indicated below, a single random block or any combination of multiple blocks can be erased simultaneously.



(TD.ABE.HN28F4001)

■ MANUAL PROGRAMMING FLOWCHART

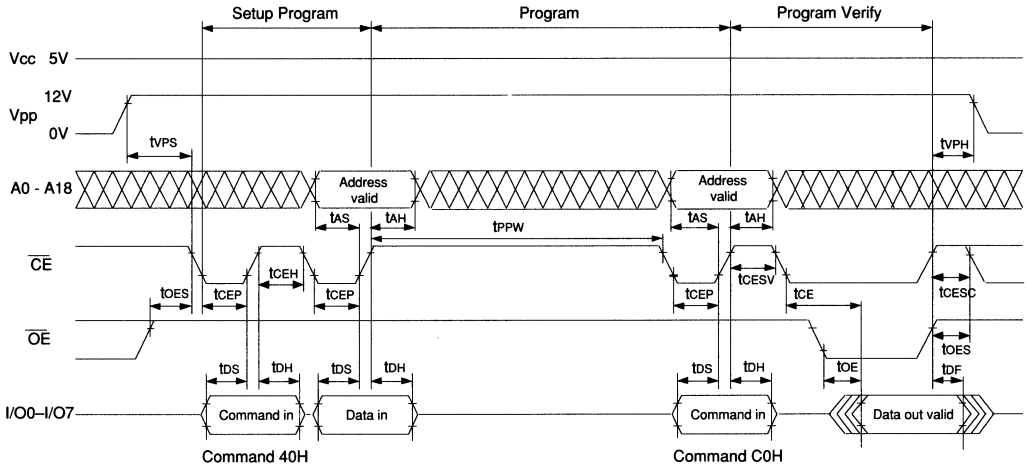
The HN28F4001 can be programmed with the fast, high-reliability programming algorithm shown in the following flowchart. This algorithm provides fast programming time without any voltage stress to the device or deterioration in reliability of programmed data.



(FC.P.HN28F4001)

Hitachi America, Ltd. • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

■ MANUAL PROGRAMMING TIMING WAVEFORM

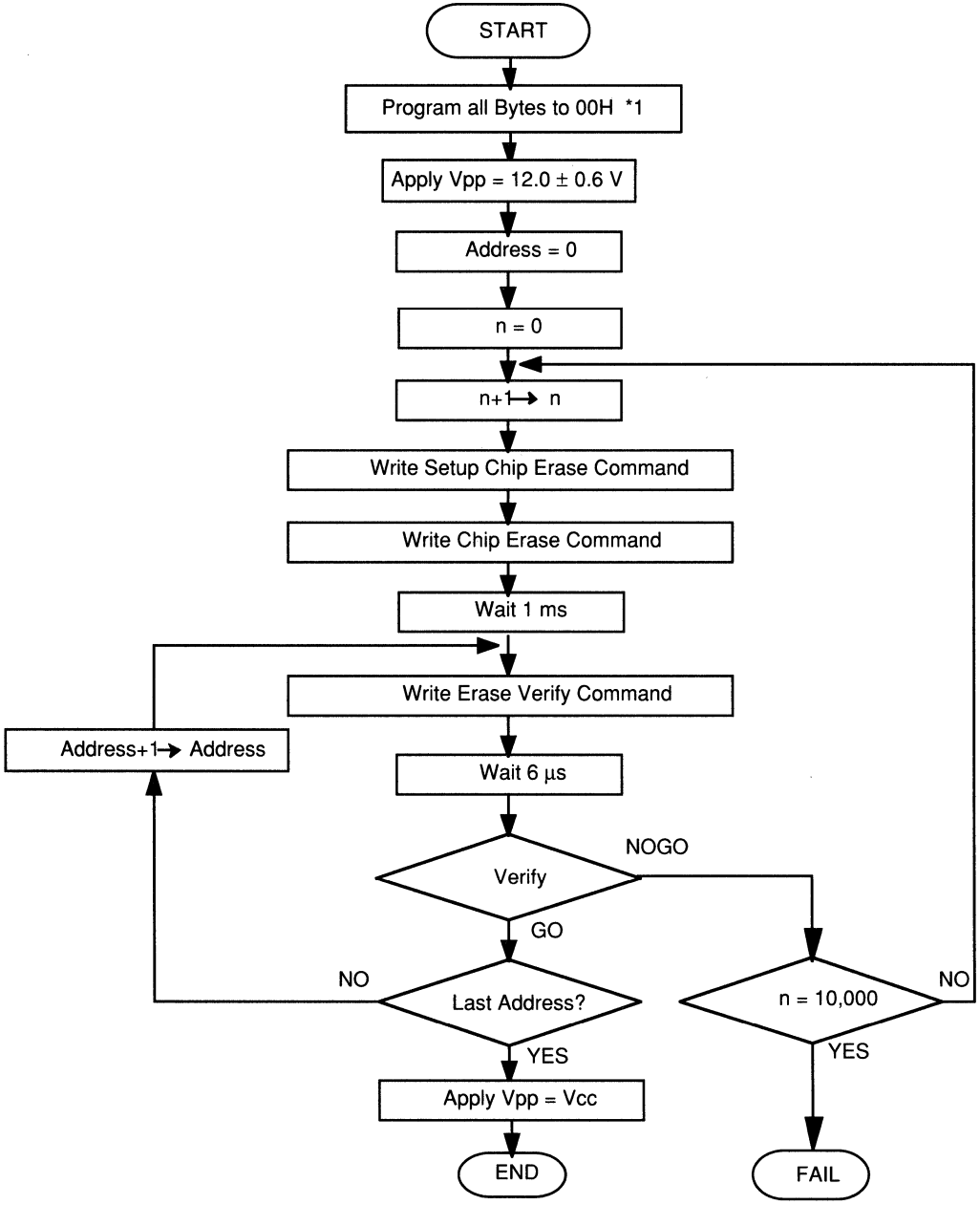


(TD.MP.HN28F4001)

2

■ MANUAL CHIP ERASE FLOWCHART

The HN28F4001 can be erased with the fast, high-reliability chip erase algorithm shown in the following flowchart. This algorithm provides a fast erase time without any voltage stress to the device or deterioration in data reliability.

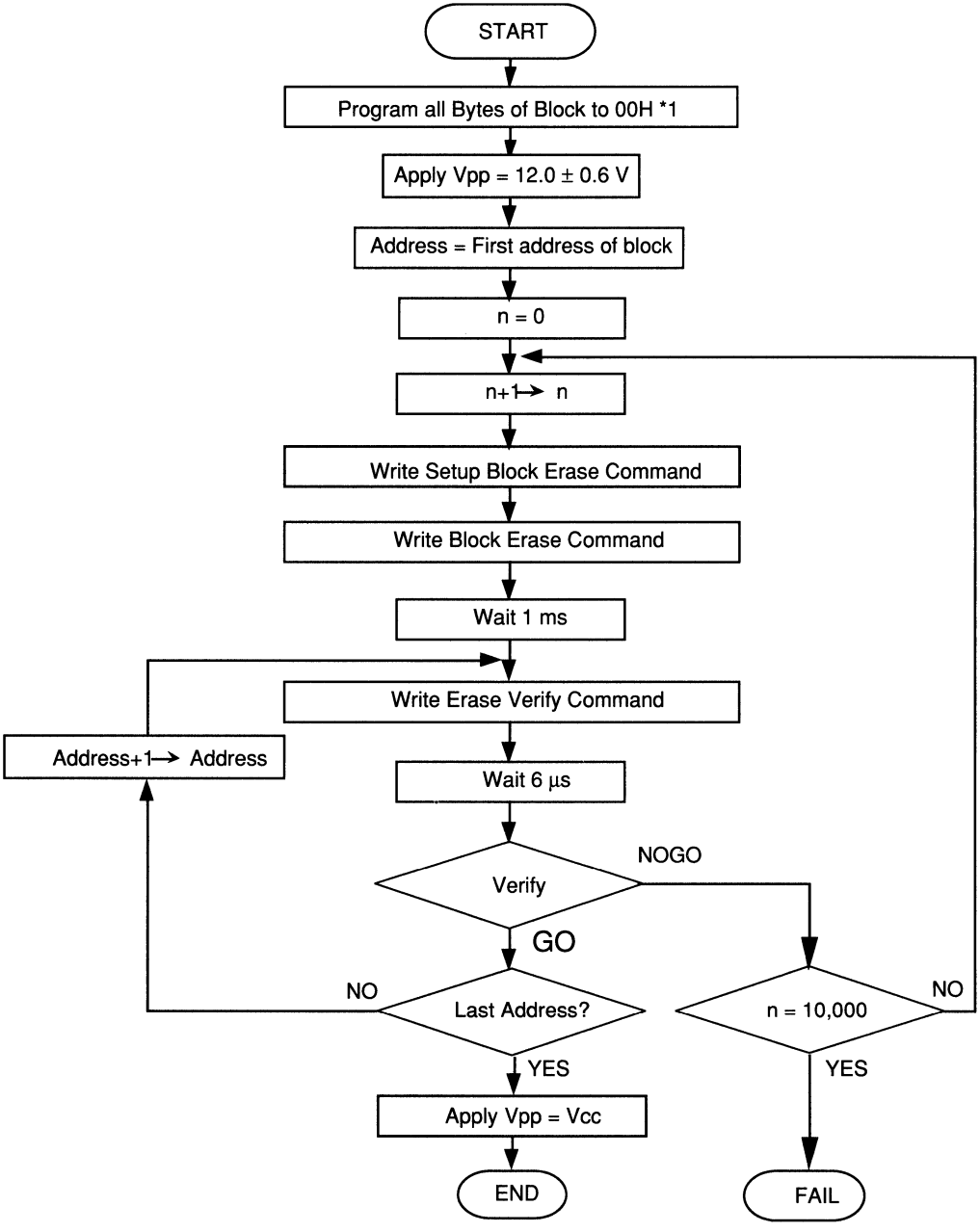


*1. Refer to Manual Programming Flowchart

(FC.CE.HN28F4001)

■ MANUAL BLOCK ERASE FLOWCHART

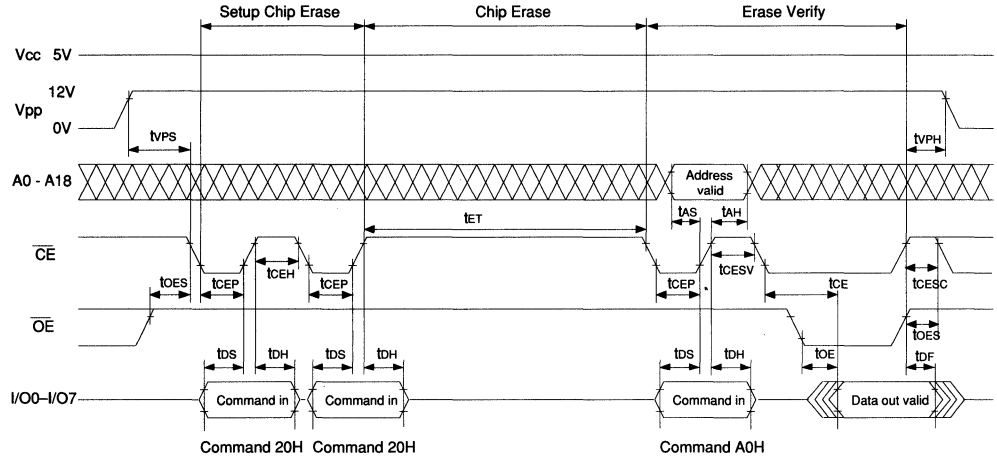
The HN28F4001 can be erased with the fast, high-reliability block erase algorithm shown in the following flowchart. This algorithm provides a fast block (16KBytes) erase time without any voltage stress to the device or deterioration in data reliability.



*1. Refer to Manual Programming Flowchart

(FC.BE.HN28F4001)

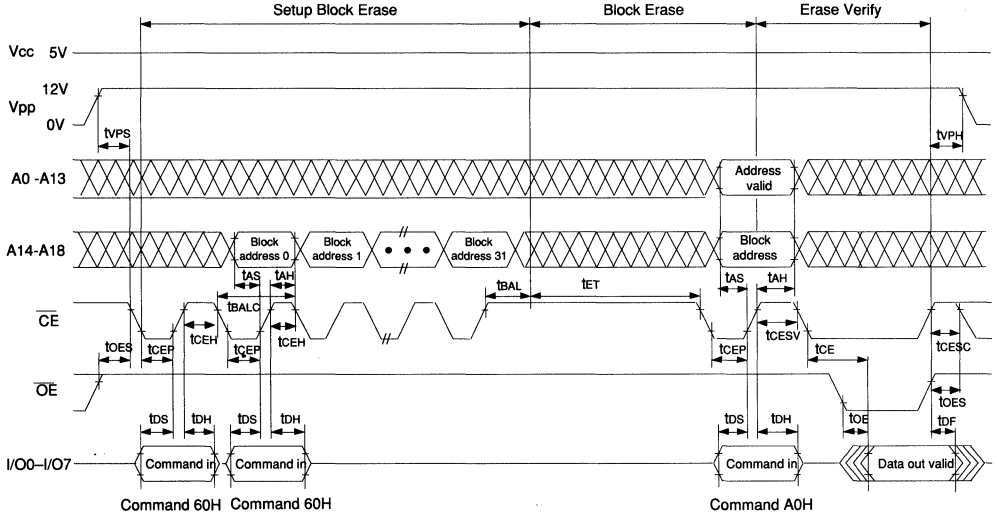
■ MANUAL CHIP ERASE TIMING WAVEFORM



(TD.CE.HN28F4001)

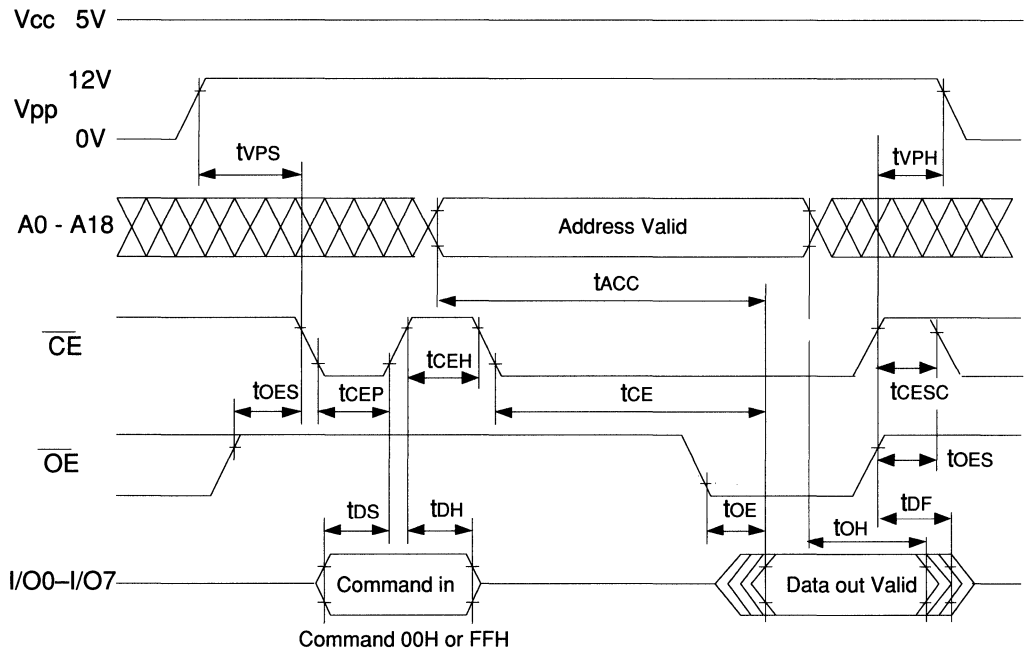
■ MANUAL BLOCK ERASE TIMING WAVEFORM

As indicated below, a single random block or any combination of multiple blocks can be erased simultaneously.



(TD.BE.HN28F4001)

■ READ TIMING WAVEFORM (V_{PP} APPLIED)



(TD.RTW.HN28F4001)

■ DEVICE IDENTIFIER MODE DESCRIPTION

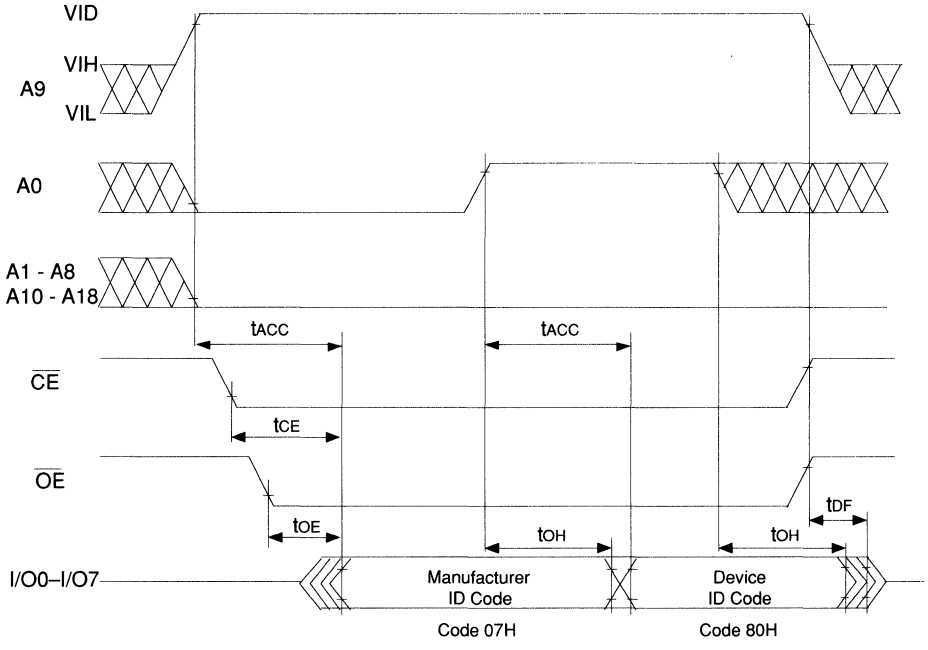
The Device Identifier Mode allows binary codes to be read from the outputs that identify the manufacturer and the type of device. Using this mode with programming equipment, the device will automatically match its own erase and programming algorithm.

■ HN28F4001 SERIES IDENTIFIER CODE

Identifier	A_0	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	1	0	0	0	0	0	0	0	80

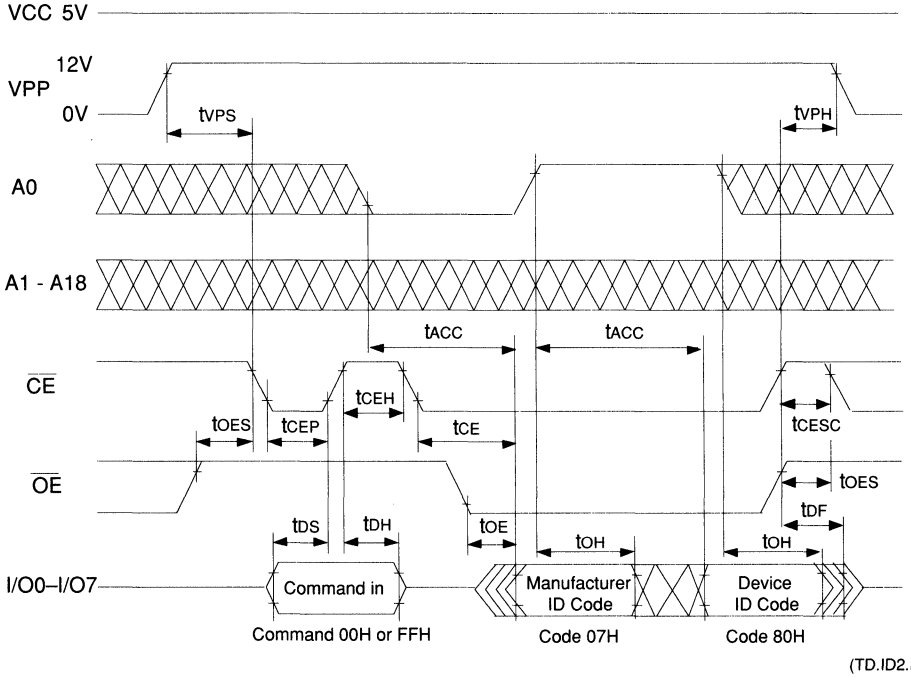
Notes: 1. Device identifier code can be read out by applying 12.0 V ± 0.5 V to A9 when V_{PP}=V_{CC}, or inputting command while V_{PP}=12 V.
2. V_{CC} = V_{PP}=5.0 V ± 10% when applying 12 V to A9.
V_{CC} =5.0 V ± 10% and V_{PP}=12.0 V ± 0.6 V in command inputs.
3. A1 to A8, A10 to A18, $\overline{CE}$, and $\overline{OE}$ = V_{IL}.

■ IDENTIFIER CODE READ TIMING WAVEFORM (V_{PP} = V_{SS} to V_{CC})



(TD.ID1.HN28F4001)

■ IDENTIFIER CODE READ TIMING WAVEFORM (V_{PP} = 12V)



(TD.ID2.HN28F4001)

Mask ROM

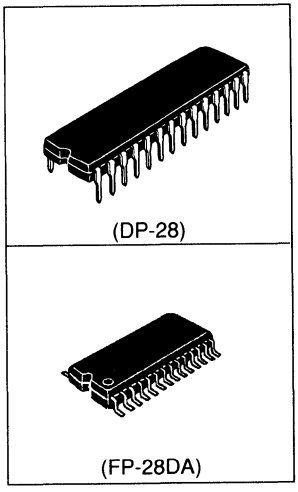
SECTION 3
Mask ROM

HITACHI

Hitachi America, Ltd. • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

HN62321 Series
HN62331 Series

1M (128K x 8-bit) Mask ROM



■ DESCRIPTION

The Hitachi HN62321/HN62331 Series is a 1-Megabit CMOS Mask Programmable Read Only Memory organized as 131,072 x 8-bit.

The low power consumption of this device makes it ideal for battery powered, portable systems. In addition, the high speed provides enough capacity and high performance to be used as a character generator in laser printers.

Hitachi's HN62321/HN62331 Series is offered with pinouts in 28-pin Plastic DIP and 28-lead Plastic SOP packages.

■ FEATURES

- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Fast Access Times:
  120/150/200 ns (max)
- Low Power Consumption:
  Active Current: 100 mW (typ)
  Standby Current: 5 µW (typ)
- Byte-Wide Data Organization
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Packages:
  28-pin Plastic DIP
  28-lead Plastic SOP

■ ORDERING INFORMATION

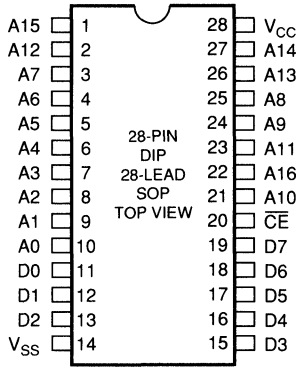
Type No.	Access Time	Package
HN62331P HN62331BP	120/150 ns 200 ns	28-pin Plastic DIP (DP-28)
HN62331F HN62331BF	120/150 ns 200 ns	28-lead Plastic SOP (FP-28DA)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{16}	Address
D_0 - D_7	Output
$\overline{CE}$	Chip Enable
V_{CC}	Power Supply
V_{SS}	Ground

■ PIN ARRANGEMENT

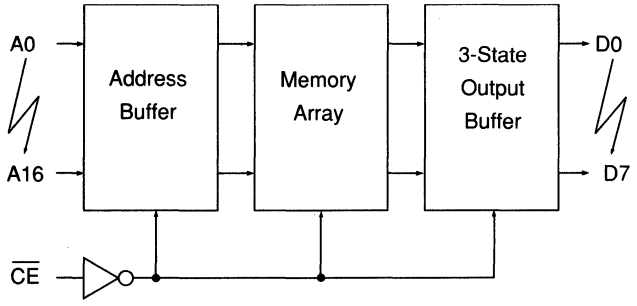
HN62321/331P Series
HN62321BP Series
HN62321/331F Series
HN62321BF Series



(PinD28.HN62321/331)

3

■ BLOCK DIAGRAM



(BD.HN62321/331)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
Terminal Voltage [1]	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Notes: 1. With respect to V_{SS}.

■ CAPACITANCE

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0 V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance [1]	C_{IN}	-	10	pF
Output Capacitance [1]	C_{OUT}	-	15	pF

Notes: 1. This parameter is sampled and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-	10	µA	$\overline{CE}$ = 2.2 [1] V, V_{OUT} = 0 to V_{CC}
Operating V_{CC} Current	I_{CC}	-	50	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC}= Min.
Standby V_{CC} Current	I_{SB}	-	30	µA	V_{CC} = 5.5 V, $\overline{CE}$ ≥ V_{CC}-0.2V
Input Voltage	V_{IH}	2.2 [1]	V_{CC}+0.3	V	
	V_{IL}	-0.3	0.8 [1]	V	
Output Voltage	V_{OH}	2.4	-	V	I_{OH} = -205 µA
	V_{OL}	-	0.4	V	I_{OL} = 3.2 mA

Notes: 1. HN62331 Series is V_{IH} = 2.4 V (min.) and V_{IL} = 0.45V (max.).

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

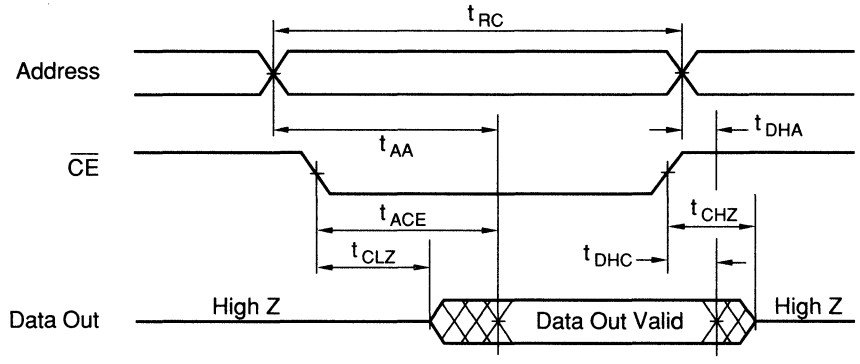
Test Conditions

- Input pulse levels: HN62321 Series: 0.8 V / 2.4 V; HN62331 Series: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

Item	Symbol	HN62331		HN62321		HN62321B		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	120	-	150	-	200	-	ns
Address Access Time	t_{AA}	-	120	-	150	-	200	ns
$\overline{CE}$ Access Time	t_{ACE}	-	120	-	150	-	200	ns
Output Hold Time from Address Change	t_{DHA}	0	-	0	-	0	-	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	-	0	-	0	-	ns
$\overline{CE}$ to Output in High Z	t_{CHZ} [1]	-	60	-	70	-	100	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	5	-	10	-	10	-	ns

Notes: 1. t_{CHZ} defines the time at which the output becomes an open circuit and is not referenced to output voltage levels.

■ READ TIMING WAVEFORM



(TD.R.HN62321/331)

Note: 1. t_{DHA}, t_{DHC} are determined by the faster time.
2. t_{AA}, t_{ACE} are determined by the slower time.

HN62321E Series

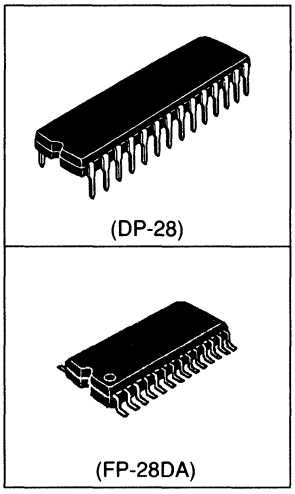
1M (128K x 8-bit) Mask ROM

■ DESCRIPTION

The Hitachi HN62321E Series is a 1-Megabit CMOS Mask Programmable Read Only Memory organized as 131,072 x 8-bit.

The low power consumption of this device makes it ideal for battery powered, portable systems. In addition, the high speed provides enough capacity and high performance to be used as a character generator in laser printers.

Hitachi's HN62321E is offered with pinouts in 28-pin Plastic DIP and 28-lead Plastic SOP packages.



(DP-28)

(FP-28DA)

■ FEATURES

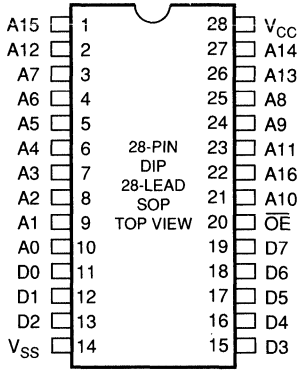
- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Fast Access Time:
  200 ns (max)
- $\overline{OE}$ Access Time:
  100 ns (max)
- Low Power Consumption:
  Active Current: 100 mW (typ)
- Byte-Wide Data Organization
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Packages:
  28-pin Plastic DIP
  28-lead Plastic SOP

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN62321EP	200 ns	28-pin Plastic DIP (DP-28)
HN62321EF	200 ns	28-lead Plastic SOP (FP-28DA)

■ PIN ARRANGEMENT

HN62321EP Series
HN62321EF Series

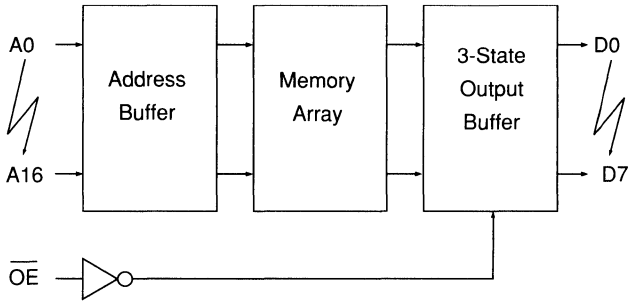


(PinD28.HN62321E)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{16}	Address
D_0 - D_7	Output
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground

■ BLOCK DIAGRAM



(BD.HN62321E)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
Terminal Voltage [1]	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Notes: 1. With respect to V_{SS}.

■ CAPACITANCE

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0 V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance [1]	C_{IN}	-	10	pF
Output Capacitance [1]	C_{OUT}	-	15	pF

Notes: 1. This parameter is sampled and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-	10	µA	$\overline{OE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Operating V_{CC} Current	I_{CC}	-	50	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = min.
Input Voltage	V_{IH}	2.2	V_{CC}+0.3	V	
	V_{IL}	-0.3	0.8	V	
Output Voltage	V_{OH}	2.4	-	V	I_{OH} = -205 µA
	V_{OL}	-	0.4	V	I_{OL} = 3.2 mA

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

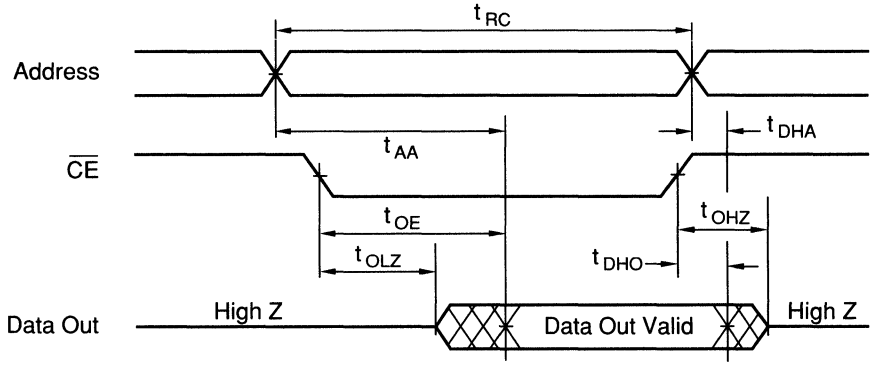
Test Conditions

- Input pulse levels: 0.8 V / 2.4 V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

Item	Symbol	Min.	Max.	Unit
Read Cycle Time	t_{RC}	200	-	ns
Address Access Time	t_{AA}	-	200	ns
$\overline{OE}$ Access Time	t_{OE}	-	100	ns
Output Hold Time from Address Change	t_{DHA}	0	-	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	-	ns
$\overline{OE}$ to Output in High Z	t_{OHZ} [1]	-	100	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	-	ns

Note: 1. t_{OHZ} defines the time at which the output becomes an open circuit and is not referenced to output voltage levels.

■ READ TIMING WAVEFORM

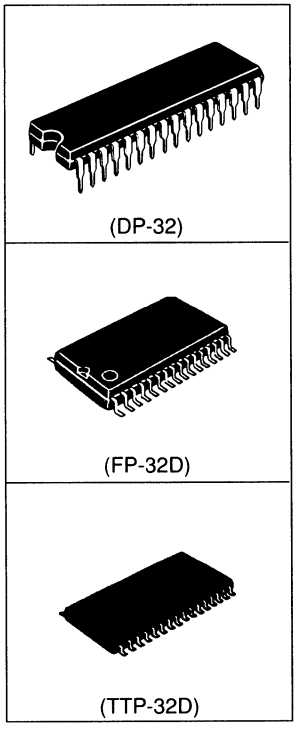


(TD.HN62321E)

Note: 1. t_{DHA}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{OE} are determined by the slower time.

HN62321A Series
HN62331A Series

1M (128K x 8-bit) Mask ROM



■ DESCRIPTION

The Hitachi HN62321A/HN62331A Series is a 1-Megabit CMOS Mask Programmable Read Only Memory organized as 131,072 x 8-bit.

The low power consumption of this device makes it ideal for battery powered, portable systems. In addition, the high speed provides enough capacity and high performance to be used as a character generator in laser printers.

Hitachi's HN62321A/HN62331A Series is offered in JEDEC-Standard Byte-Wide EPROM pinouts in 32-pin Plastic DIP and 32-lead Plastic SOP packages. This allows socket replacement with Flash Memory and EPROMs.

■ FEATURES

- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Fast Access Times:
  120/150 ns (max)
- Low Power Consumption:
  Active Current: 100 mW (typ)
  Standby Current: 5 µW (typ)
- Byte-Wide Data Organization
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:
  JEDEC Standard Byte-Wide EPROM
  Flash and EPROM Compatible
- Packages:
  32-pin Plastic DIP
  32-lead Plastic SOP

■ ORDERING INFORMATION

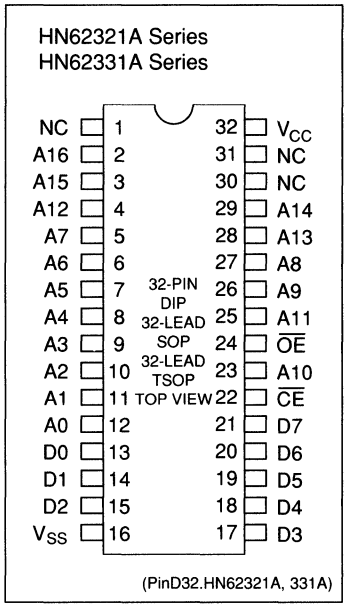
Type No.	Access Time	Package
HN62331AP	120 ns	32-pin Plastic DIP
HN62321AP	150 ns	(DP-32)
HN62331AF	120 ns	32-lead Plastic SOP
HN62321AF	150 ns	(FP-32D)
HN62331ATT	120 ns	32-lead Plastic TSOP
HN62321ATT	150 ns	(TTP-32D)

3

■ PIN DESCRIPTION

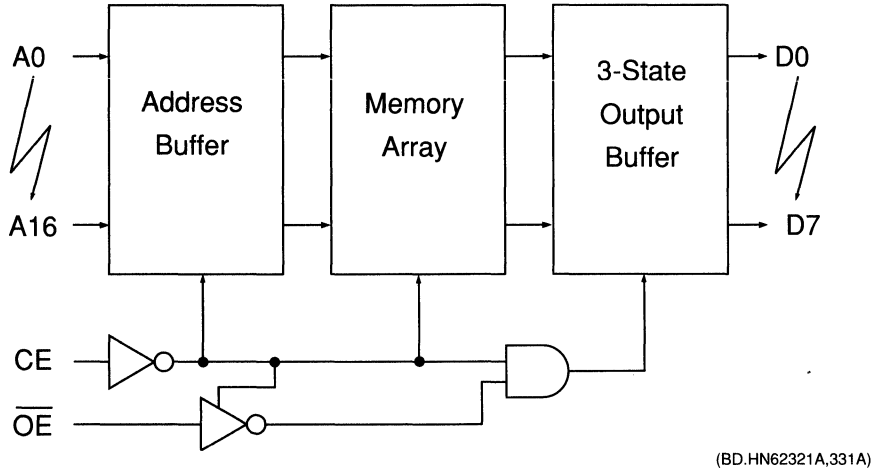
Pin Name	Function
A_0 - A_{16}	Address
D_0 - D_7	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ PIN ARRANGEMENT



(PinD32.HN62321A, 331A)

■ BLOCK DIAGRAM



(BD.HN62321A,331A)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
Terminal Voltage [1]	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Notes: 1. With respect to V_{SS}.

■ CAPACITANCE

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0 V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance [1]	C_{IN}	-	10	pF
Output Capacitance [1]	C_{OUT}	-	15	pF

Notes: 1. This parameter is sampled and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Operating V_{CC} Current	I_{CC}	-	50	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = Min.
Standby V_{CC} Current	I_{SB}	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$-0.2V
Input Voltage	V_{IH}	2.2 [1]	V_{CC}+0.3	V	
	V_{IL}	-0.3	0.8 [1]	V	
Output Voltage	V_{OH}	2.4	-	V	I_{OH} = -205 µA
	V_{OL}	-	0.4	V	I_{OL} = 3.2 mA

Notes: 1. HN62331A Series is V_{IH} = 2.4V (min) and V_{IL} = 0.45V (max).

3

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

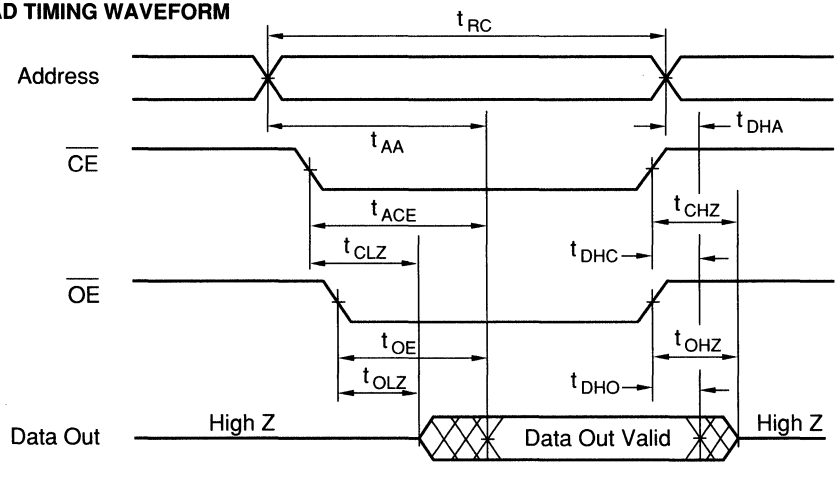
Test Conditions

- Input pulse levels: HN62321A Series: 0.8 V / 2.4 V; HN62331A Series: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

Item	Symbol	HN62331A		HN62321A		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	120	-	150	-	ns
Address Access Time	t_{AA}	-	120	-	150	ns
$\overline{CE}$ Access Time	t_{ACE}	-	120	-	150	ns
$\overline{OE}$ Access Time	t_{OE}	-	60	-	70	ns
Output Hold Time from Address Change	t_{DHA}	0	-	0	-	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	-	0	-	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	-	0	-	ns
$\overline{CE}$ to Input in High Z	t_{CHZ} [1]	-	60	-	70	ns
$\overline{OE}$ to Input in High Z	t_{OHZ} [1]	-	60	-	70	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	5	-	10	-	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	5	-	10	-	ns

Note: 1. t_{CHZ} and t_{OHZ} define the time at which the output becomes an open circuit and are not referenced to output voltage levels.

■ READ TIMING WAVEFORM



Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

(TD.HN62321A,331A)

HN62412 Series
HN62422 Series

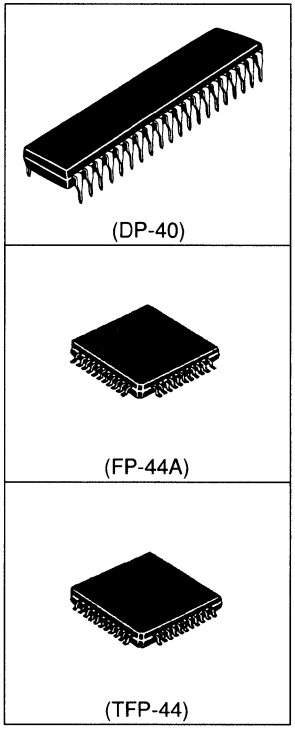
2M (128K x 16-bit) and (256K x 8-bit) Mask ROM

■ DESCRIPTION

The Hitachi HN62412/HN62422 Series is a 2-Megabit CMOS Mask ROM organized as 132,072 x 16-bit and 262,144 x 8-bit.

The low power consumption of this device makes it ideal for battery powered, portable systems. In addition , the high density and high speed provide enough capacity and high performance to be used as a character generator in laser printers.

Hitachi's HN62412/HN62422 Series is packaged in 40-pin Plastic DIP and 44-lead Plastic QFP and TQFP packages.



■ FEATURES

- Single Power Supply:
  V_{CC} = 5 V ± 10% (HN62412)
  V_{CC} = 5 V ± 5% (HN62422)
- Fast Access Times:
  150 ns/200 ns (max)
- Low Power Consumption:
  Active Current: 100 mW (typ)
  Standby Current: 5 µW (typ)
- User Selectable Organization:
  128K x 16-bit (Word-Wide)
  256K x 8-bit (Byte-Wide)
  Switchable with BHE pin
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Packages:
  40-pin Plastic DIP
  44-lead Plastic QFP
  44-lead Plastic TQFP

■ ORDERING INFORMATION

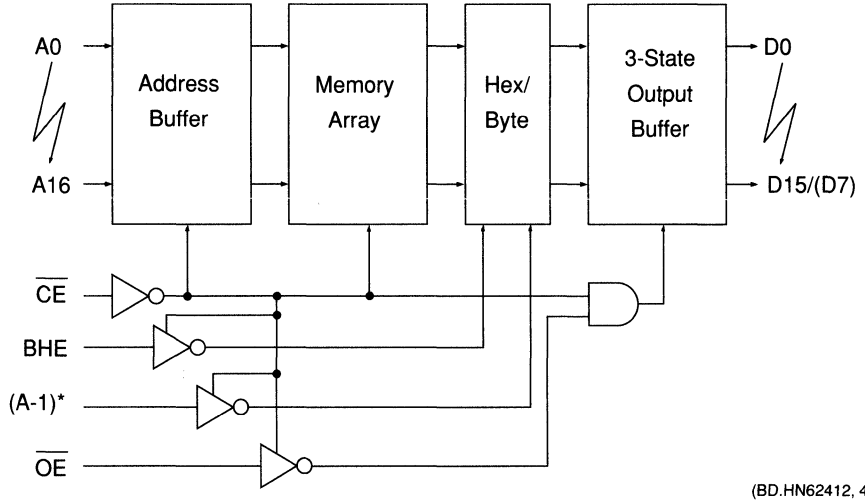
Type No.	Access Time	Package
HN62422P	150 ns	40-pin Plastic DIP
HN62412P	200 ns	(DP-40)
HN62422FP	150 ns	44-lead Plastic QFP
HN62412FP	200 ns	(FP-44A)
HN62422TFP	150 ns	44-lead Plastic TQFP
HN62412TFP	200 ns	(TFP-44)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{16}	Address
A_{-1}	Address (Word-Wide)
D_0 - D_{15}	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
BHE	Byte Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ PIN ARRANGEMENT

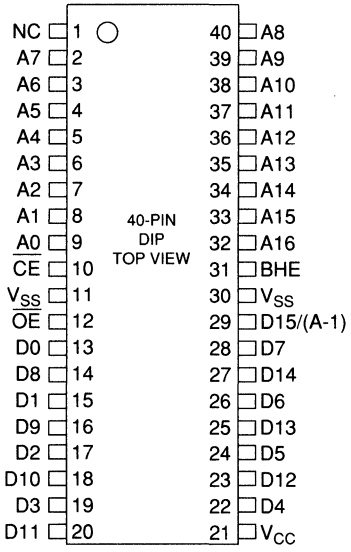
■ BLOCK DIAGRAM



(BD.HN62412, 422)

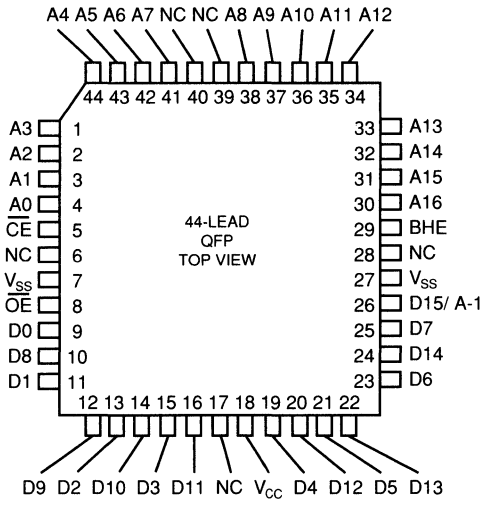
Notes: 1. * : A_{-1} is the Least Significant Address bit in Byte-Wide Mode.
2. BHE=V_{IH} : 16-bit (D_{15} - D_0)
BHE=V_{IL} : 8-bit (D_7 - D_0)
When BHE is low, D_{14} - D_8 are in high impedance states.

HN62412P Series
HN62422P Series



(PinD40.HN62412, 422)

HN62412/422FP Series
HN62412/422TFP Series



(PinQ44.HN62412, 422)

3

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage[1]	V_{CC}	-0.3 to +7.0	V
All Input and Output Voltage[1]	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	° C
Storage Temperature Range	T_{STG}	-55 to +125	° C
Temperature Under Bias	T_{BIAS}	-20 to +85	° C

Note: 1. Relative to V_{SS}.

■ CAPACITANCE

(V_{CC} = 5V ± 10%[2], V_{SS} = 0V, T_a = 25°C, V_{IN} = 0V, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit
Input Capacitance[1]	C_{IN}	-	-	15	pF
Output Capacitance[1]	C_{OUT}	-	-	15	pF

Note: 1. This parameter is sampled and not 100% tested.
2. HN62422 Series is 5V ± 5%.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%[1], V_{SS} = 0V, T_a = 0 to +70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-	-	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Active Current	I_{CC}	-	-	50	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC}=min
Standby Current	I_{SB}	-	-	30	µA	V_{CC} = 5.5 V,$\overline{CE}$ ≥ V_{cc} - 0.2V
Input Voltage	V_{IH}	2.2	-	V_{CC}+0.3	V	
	V_{IL}	-0.3	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -205 µA
	V_{OL}	-	-	0.4	V	I_{OL} = 1.6 mA

Note: 1. HN62422 Series is 5V ± 5%.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%[2], V_{SS} = 0V, T_a = 0 to +70°C)

Test Conditions

- Input pulse levels: 0.45 to 2.4V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

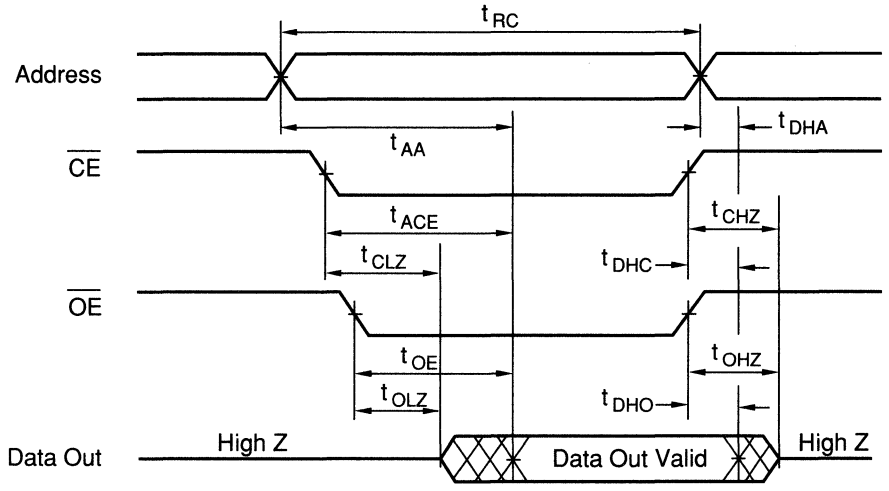
Item	Symbol	HN62422		HN62412		Test Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	150	-	200		ns
Address Access Time	t_{AA}	-	150	-	200	ns
Chip Enable Access Time	t_{ACE}	-	150	-	200	ns
Output Enable Access Time	t_{OE}	-	70	-	100	ns
BHE Access Time	t_{BHE}	-	150	-	200	ns
Output Hold Time from Address Change	t_{DHA}	0	-	0	-	ns
Output Hold Time from Chip Enable	t_{DHC}	0	-	0	-	ns
Output Hold Time from Output Enable	t_{DHO}	0	-	0	-	ns
Output Hold Time from BHE	t_{DHB}	0	-	0	-	ns
Chip Enable to Output in High-Z [1]	t_{CHZ}	-	70	-	70	ns
Output Enable to Output in High-Z [1]	t_{OHZ}	-	70	-	70	ns
BHE to Output in High-Z [1]	t_{BHZ}	-	70	-	70	ns
Chip Enable to Output in Low-Z	t_{CLZ}	10	-	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}	10	-	10	-	ns
BHE to Output in Low-Z	t_{BLZ}	10	-	10	-	ns

Note: 1. t_{CHZ}, t_{OHZ}, and t_{BHZ} are defined as the time at which the output becomes an open circuit and are not referred to output voltage levels.

2. HN62422 series is 5V± 5%

■ READ TIMING WAVEFORM

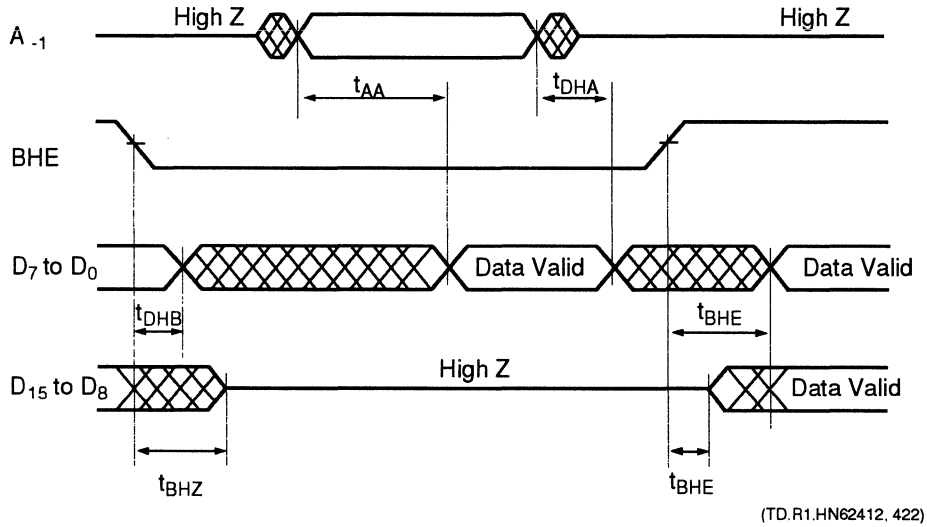
Word Mode (BHE = V_{IH}) or Byte Mode (BHE = V_{IL})



(TD.R.HN62412, 422)

Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

Word Mode/Byte Mode Switch



(TD.R1.HN62412, 422)

Note: 1. If $\overline{CE}$ and $\overline{OE}$ are enabled, A_{16} to A_0 are valid.
2. D_{15}/A-1 pin is in the output state when BHE is High, $\overline{CE}$ and $\overline{OE}$ are enabled. Therefore, the input signals of opposite phase to the output must not be applied to them.

HN62442B Series

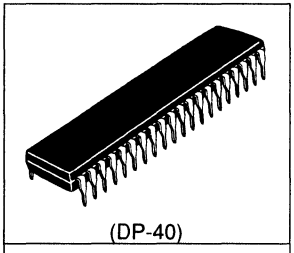
2M (128K x 16-bit) Mask ROM

■ DESCRIPTION

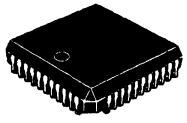
The Hitachi HN62442B is a 2-Megabit CMOS Mask Programmable Read Only Memory organized as 131,072 x 16-bit.

The low power consumption of this device makes it ideal for battery powered, portable systems. In addition , the high density and high speed provide enough capacity and high performance to be used as a character generator in laser printers.

Hitachi's HN62442B is offered with JEDEC-Standard pinouts in a 40-pin Plastic DIP and 44-lead PLCC packages.



(DP-40)



(CP-44)

■ FEATURES

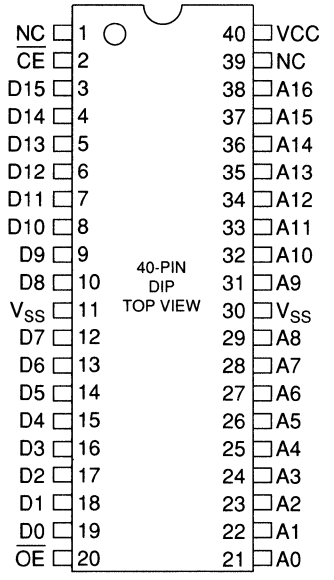
- Single Power Supply:
  V_{CC} = 5 V ± 10%
- High Speed Access Time:
  100 ns (max)
- Low Power Consumption:
  Active Current: 150 mW (typ)
  Standby Current: 5 μW (typ)
- Word-Wide Data Organization
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:
  JEDEC Standard Word-Wide EPROM Pinout
- Packages:
  40-pin Plastic DIP
  44-lead PLCC

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN62442BP	100 ns	40-pin Plastic DIP (DP-40)
HN62442BCP	100 ns	44-lead PLCC (CP-44)

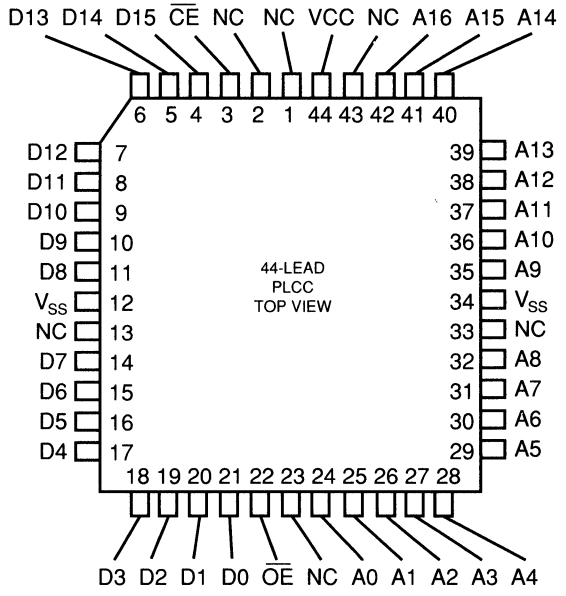
■ PIN ARRANGEMENT

HN62442BP Series



(PinD40.HN62442B)

HN62442BCP Series

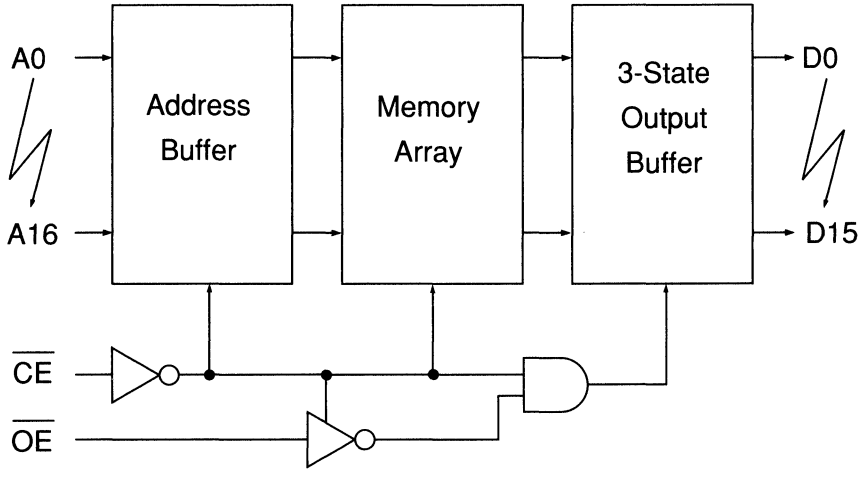


(PinQ44.HN62442B)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{16}	Address
D_0 - D_{15}	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



(BD.HN62442B)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
All Input and Output Voltage [1]	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	° C
Storage Temperature Range	T_{STG}	-55 to +125	° C
Temperature Under Bias	T_{BIAS}	-20 to +85	° C

Note: 1. Relative to V_{SS}.

■ CAPACITANCE

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0V, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit
Input Capacitance[1]	C_{IN}	-	-	15	pF
Output Capacitance[1]	C_{OUT}	-	-	15	pF

Note: 1. This parameter is sampled and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{IL}	-	-	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{OL}	-	-	10	µA	$\overline{CE}$ = 2.4V, V_{OUT} = 0 to V_{CC}
Operating V_{CC} Current	I_{CC}	-	-	100	mA	V_{CC} = 5.5 V, ID_{OUT} = 0mA, t_{RC} = Min.
Standby V_{CC} Current	I_{SB1}	-	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$ - 0.2V
	I_{SB2}	-	-	3	mA	V_{CC} = 5.5 V, $\overline{CE} \geq$ 2.4V
Input Voltage	V_{IH}	2.4	-	V_{CC}+0.3	V	
	V_{IL}	-0.3	-	0.45	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA
	V_{OL}	-	-	0.4	V	I_{OL} = 2.1 mA

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 0 to 70°C)

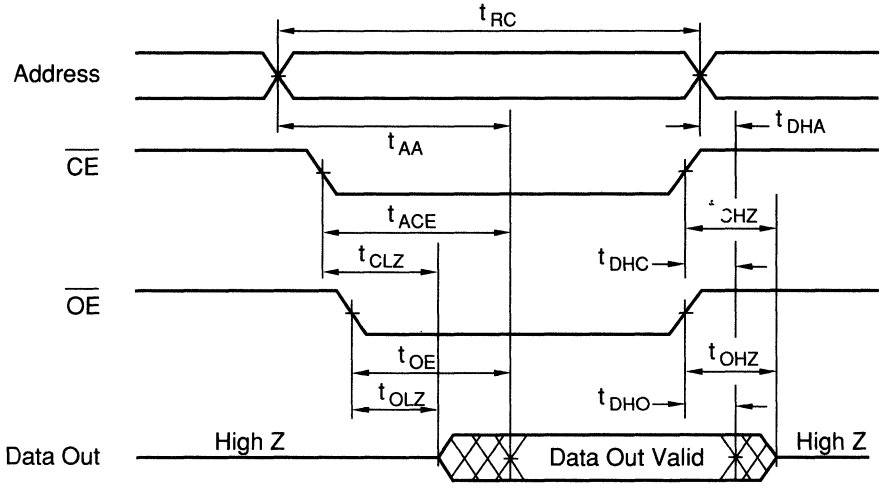
Test Conditions

- Input pulse levels: 0.45 / 2.4V
- Input rise and fall times: ≤10ns
- Output load: 1TTL gate + CL = 100pF (including jig capacitance)
- Input/Output Timing Reference level: 1.5V

Item	Symbol	Min.	Max.	Unit
Read Cycle Time	t_{RC}	100	-	ns
Address Access Time	t_{AA}	-	100	ns
Chip Enable Access Time	t_{ACE}	-	100	ns
Output Enable Access Time	t_{OE}	-	55	ns
Output Hold Time from Address Change	t_{DHA}	0	-	ns
Output Hold Time from Chip Enable	t_{DHC}	0	-	ns
Output Hold Time from Output Enable	t_{DHO}	0	-	ns
Chip Enable to Output in High-Z [1]	t_{CHZ}	-	40	ns
Output Enable to Output in High-Z [1]	t_{OHZ}	-	40	ns
Chip Enable to Output in Low-Z	t_{CLZ}	5	-	ns
Output Enable to Output in Low-Z	t_{OLZ}	5	-	ns

Note: 1. t_{CHZ} and t_{OHZ} are defined as the time at which the output becomes an open circuit and are not referenced to output voltage levels.

■ READ TIMING WAVEFORM



Notes: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

(TD.R.HN62442B)

HN62302B Series

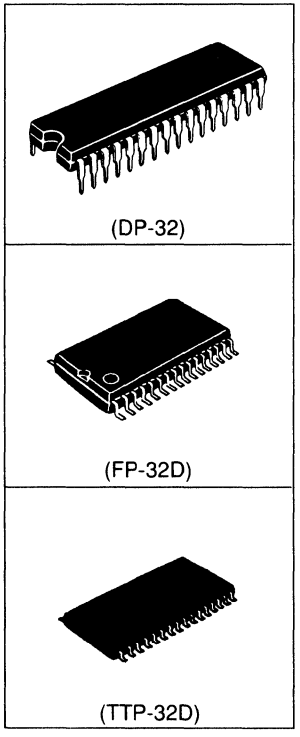
2M (256K x 8-bit) Mask ROM

■ DESCRIPTION

The Hitachi HN62302B is a 2-Megabit CMOS Mask Programmable ROM organized as 262,144 x 8 bit.

The low power consumption of this device makes it ideal for battery powered, portable systems. In addition , the high density and high speed provide enough capacity and high performance to be used as a character generator in laser printers.

Hitachi's HN62442B is offered with JEDEC-Standard pinouts in 32-pin Plastic DIP and 32-lead Plastic SOP and TSOP packages.



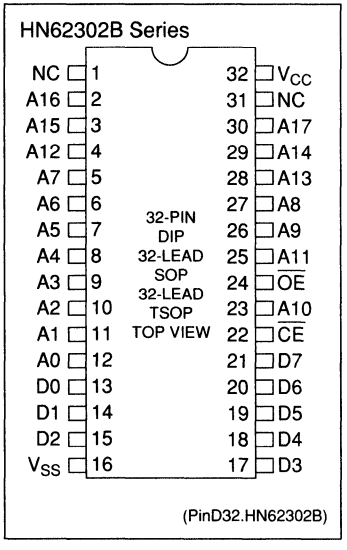
■ FEATURES

- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Fast Access Times:
  170 ns/200 ns (max)
- Low Power Consumption:
  Active Current: 100 mW (typ)
  Standby Current: 5 µW (typ)
- Byte-Wide Data Organization
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:
  JEDEC Standard Byte-Wide EPROM
- Packages:
  32-pin Plastic DIP
  32-lead Plastic SOP
  32-lead Plastic TSOP (Type II)

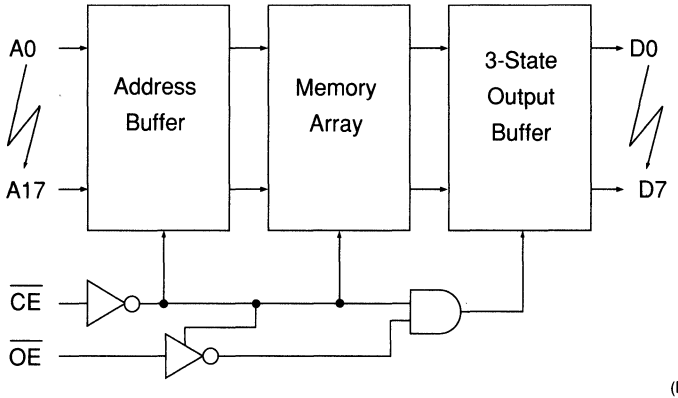
■ ORDERING INFORMATION

Type No.	Access Time	Package
HN62302BP	170 ns 200 ns	32-pin Plastic DIP (DP-32)
HN62302BF	170 ns 200 ns	32-lead Plastic SOP (FP-32D)
HN62302BTT	170 ns 200 ns	32-lead Plastic TSOP (TTP-32D)

■ PIN ARRANGEMENT



■ BLOCK DIAGRAM



(BD.HN62302B)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{17}	Address
D_0 - D_7	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
All Input and Output Voltage [1]	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Note: 1. Relative to V_{SS}.

■ CAPACITANCE

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0V, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit
Input Capacitance [1]	C_{IN}	-	-	15	pF
Output Capacitance [1]	C_{OUT}	-	-	15	pF

Note: 1. This parameter is sampled and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-	-	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Operating V_{CC} Current	I_{CC}	-	-	50	mA	V_{CC} = 5.5 V, ID_{OUT} = 0 mA, t_{RC}=min.
Standby V_{CC} Current	I_{SB}	-	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{cc}$ - 0.2V
Input Voltage	V_{IH}	2.2	-	V_{CC}+0.3	V	
	V_{IL}	-0.3	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -205 µA
	V_{OL}	-	-	0.4	V	I_{OL} = 1.6 mA

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

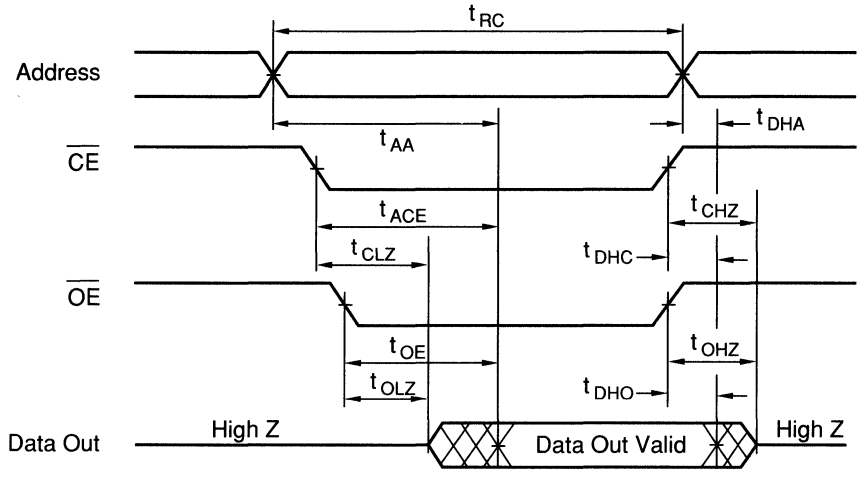
Test Conditions

- Input pulse levels: 0.8 / 2.4V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Reference level for measuring timing: 1.5 V

Item	Symbol	HN62302B-17		HN62302B-20		Test Unit
		Min.	Max.	Min.	Max.	
READ Cycle Time	t_{RC}	170	-	200		ns
Address Access Time	t_{AA}	-	170	-	200	ns
Chip Enable Access Time	t_{ACE}	-	170	-	200	ns
Output Enable Access Time	t_{OE}	-	70	-	100	ns
Output Hold Time from Address Change	t_{DHA}	0	-	0	-	ns
Output Hold Time from Chip Enable	t_{DHC}	0	-	0	-	ns
Output Hold Time from Output Enable	t_{DHO}	0	-	0	-	ns
Chip Enable to Output in High-Z [1]	t_{CHZ}	-	70	-	70	ns
Output Enable to Output in High-Z [1]	t_{OHZ}	-	70	-	70	ns
Chip Enable to Output in Low-Z	t_{CLZ}	10	-	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}	10	-	10	-	ns

Note: 1. t_{CHZ} and t_{OHZ} are defined as the time at which the output becomes an open circuit and are not referenced to output voltage levels.

■ READ TIMING WAVEFORM



(TD.R.HN62302B)

Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

HN62414 Series
HN62434 Series

4M (256K x 16-bit) and (512K x 8-bit) Mask ROM

■ DESCRIPTION

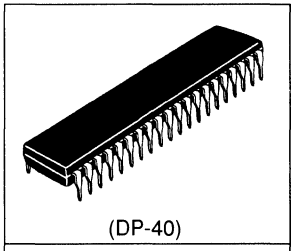
The Hitachi HN62414/HN62434 Series is a 16-Megabit CMOS Mask Programmable Read Only Memory organized as 262,144 x 16-bit and 524,288 x 8-bit.

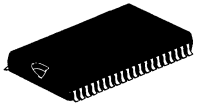
The low power consumption of this device makes it ideal for battery powered, portable systems. In addition , the high density and high speed provide enough capacity and high performance to be used as a character generator in laser printers.

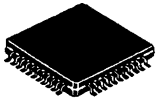
Hitachi's HN62414/HN62434 Series is offered in 40-pin Plastic DIP, 40-lead Plastic SOP, 44-lead Plastic QFP and TQFP, 48-lead Plastic SOP and 44-lead Plastic TSOP packages.

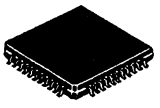
■ FEATURES

- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Fast Access Times:
  120 ns/150 ns/170 ns (max)
- Low Power Consumption:
  Active Current: 100 mW (typ)
  Standby Current: 5 µW (typ)
- User Selectable Organization:
  256K x 16-bit (Word-Wide)
  512K x 8-bit (Byte-Wide)
  Switchable with BHE pin
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Packages:
  40-pin Plastic DIP
  40-lead Plastic SOP
  44-lead Plastic QFP
  44-lead Plastic TQFP
  48-lead Plastic SOP
  44-lead Plastic TSOP (Type II)

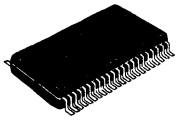

(DP-40)


(FP-40D)


(FP-44A)


(TFP-44)


(FP-48DA)


(TTP-44D)

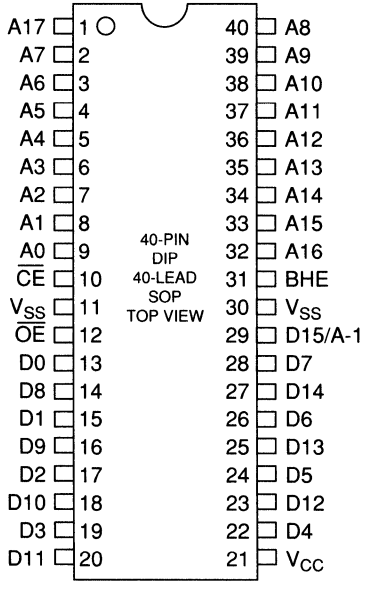
3

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN62434P	120/150 ns	40-pin Plastic
HN62414P	170 ns	DIP (DP-40)
HN62434FA	120/150 ns	40-lead Plastic
HN62414FA	170 ns	SOP (FP-40D)
HN62434FP	120/150 ns	44-lead Plastic
HN62414FP	170 ns	QFP (FP-44A)
HN62434TFP	120/150 ns	44-lead Plastic
HN62414TFP	170 ns	TQFP (TFP-44)
HN62434F	120/150 ns	48-lead Plastic
HN62414F	170 ns	SOP (FP-48DA)
HN62434TT	120/150 ns	44-lead Plastic
HN62414TT	170 ns	TSOP (TTP-44D)

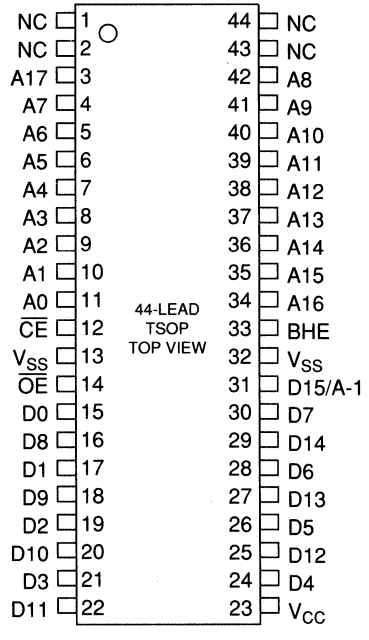
■ PIN ARRANGEMENT

HN62414/434P Series
HN62414/434FA Series



(PinD40.HN62414,434)

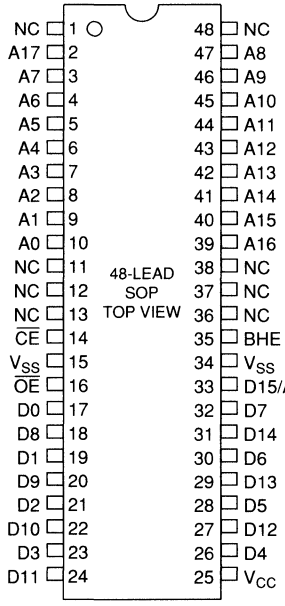
HN62414/434TT Series



(PinT240.HN62414,434)

■ PIN ARRANGEMENT (cont.)

HN62414/434F Series



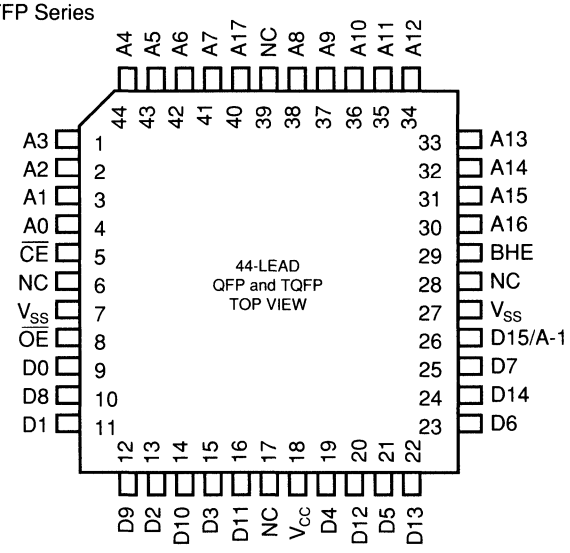
Note:
Pins 11, 12, 13, 36, 37, and 38 are connected to the inner lead frame.

(PinT248.HN62414,434)

■ PIN DESCRIPTION

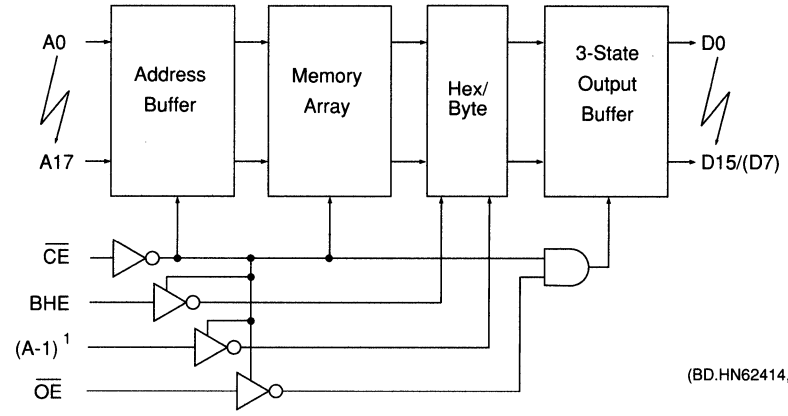
Pin Name	Function
A_0 - A_{17}	Address
A_{-1}	Address (Word-Wide)
D_0 - D_{15}	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
BHE	Byte Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

HN62414/434FP/TFP Series



(PinQ44.HN62414,434)

■ BLOCK DIAGRAM



Notes: 1. * : A_{-1} is the Least Significant Address bit in Byte-Wide Mode.
2. BHE=V_{IH} : 16-bit (D_{15} - D_0)
BHE=V_{IL} : 8-bit (D_7 - D_0)
When BHE is low, D_{14} - D_8 are in high impedance states.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
Terminal Voltage [1]	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	° C
Storage Temperature Range	T_{STG}	-55 to +125	° C
Temperature Under Bias	T_{BIAS}	-20 to +85	° C

Notes: 1. With respect to V_{SS}.

■ CAPACITANCE

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0 V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance [1]	C_{IN}	-	15	pF
Output Capacitance [1]	C_{OUT}	-	15	pF

Notes: 1. This parameter is sampled and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Operating V_{CC} Current	I_{CC}	-	50	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC}= Min.
Standby V_{CC} Current	I_{SB}	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$-0.2V
Input Voltage	V_{IH}	2.2	V_{CC}+0.3	V	
	V_{IL}	-0.3	0.8	V	
Output Voltage	V_{OH}	2.4	-	V	I_{OH} = -205 µA
	V_{OL}	-	0.4	V	I_{OL} = 1.6 mA

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Test Conditions

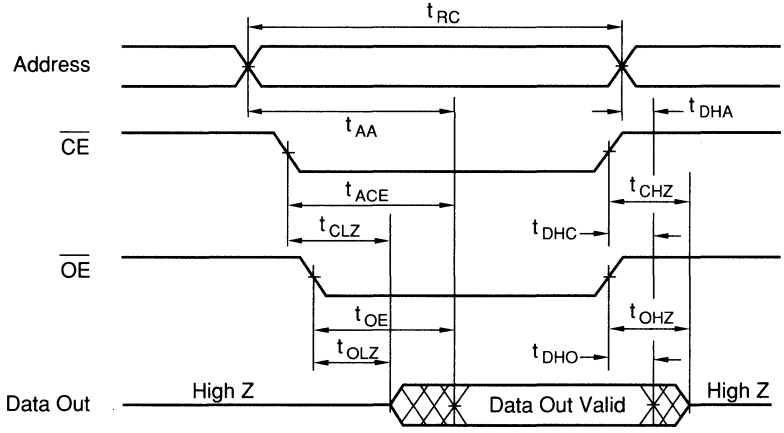
- Input pulse levels: 0.8 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

Item	Symbol	HN62434-12		HN62434-15		HN62414-17		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	120	-	150	-	170	-	ns
Address Access Time	t_{AA}	-	120	-	150	-	170	ns
$\overline{CE}$ Access Time	t_{ACE}	-	120	-	150	-	170	ns
$\overline{OE}$ Access Time	t_{OE}	-	60	-	70	-	70	ns
BHE Access Time	t_{BHE}	-	120	-	150	-	170	ns
Output Hold Time from Address Change	t_{DHA}	0	-	0	-	0	-	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	-	0	-	0	-	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	-	0	-	0	-	ns
Output Hold Time from BHE	t_{DHB}	0	-	0	-	0	-	ns
$\overline{CE}$ to Output in High Z[1]	t_{CHZ}	-	60	-	70	-	70	ns
$\overline{OE}$ to Output in High Z[1]	t_{OHZ}	-	60	-	70	-	70	ns
BHE to Output in High Z[1]	t_{BHZ}	-	60	-	70	-	70	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	5	-	10	-	10	-	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	5	-	10	-	10	-	ns
BHE to Output in Low Z	t_{BLZ}	5	-	10	-	10	-	ns

Note: 1. t_{CHZ}, t_{OHZ}, and t_{BHZ} are defined as the time at which the output becomes an open circuit and are not referenced to output voltage levels.

■ READ TIMING WAVEFORM

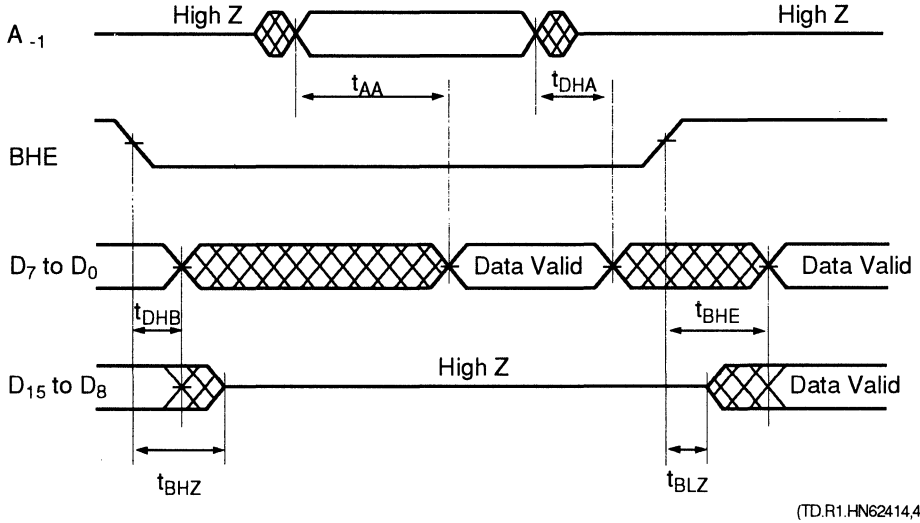
Word Mode (BHE = V_{IH}) or Byte Mode (BHE = V_{IL})



(TD.R.HN62414,434)

Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

Word Mode/Byte Mode Switch



(TD.R1.HN62414,434)

Note: 1. $\overline{CE}$ and $\overline{OE}$ are enabled, A_{17} to A_0 are valid.
2. D_{15}/A_{-1} pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enabled. Therefore, the input signals of opposite phase to the output must not be applied to them.

4M (256K x 16-bit) and (512K x 8-bit) Mask ROM

■ DESCRIPTION

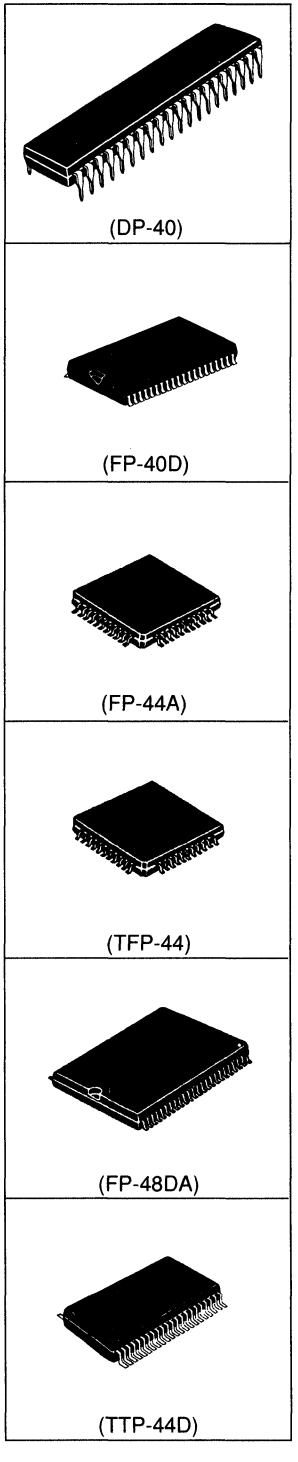
The Hitachi HN62415 Series is a 4-Megabit CMOS Mask Programmable Read Only Memory organized as 262,144 x 16-bit and 524,288 x 8-bit.

The low power consumption of this device makes it ideal for battery powered, portable systems. In addition , the high density and high speed provide enough capacity and high performance to be used as a character generator in laser printers.

Hitachi's HN62415 Series is offered in 40-pin Plastic DIP, 40-lead Plastic SOP, 44-lead Plastic QFP and TQFP, 48-lead Plastic SOP and 44-lead Plastic TSOP packages.

■ FEATURES

- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Fast Access Times:
  120 ns/150 ns/200 ns (max)
- Low Power Consumption:
  Active Current: 100 mW (typ)
  Standby Current: 5 µW (typ)
- User Selectable Organization:
  256K x 16-bit (Word-Wide)
  512K x 8-bit (Byte-Wide)
  Switchable with BHE pin
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:
  JEDEC Standard Word-Wide/Byte-Wide Pinout
- Packages:
  40-pin Plastic DIP
  40-lead Plastic SOP
  44-lead Plastic QFP
  44-lead Plastic TQFP
  48-lead Plastic SOP
  44-lead Plastic TSOP (Type II)

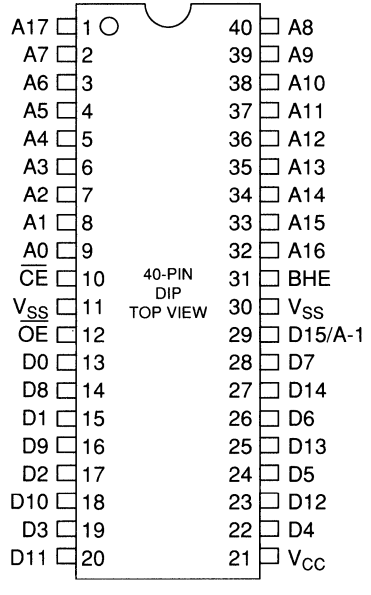


■ ORDERING INFORMATION

Type No.	Access Time	Package
HN62415P	120 ns 150 ns 200 ns	40-pin Plastic DIP (DP-40)
HN62415FA	120 ns 150 ns 200 ns	40-lead Plastic SOP (FP-40D)
HN62415FP	120 ns 150 ns 200 ns	44-lead Plastic QFP (FP-44A)
HN62415TFP	120 ns 150 ns 200 ns	44-lead Plastic TQFP (TFP-44)
HN62415F	120 ns 150 ns 200 ns	48-lead Plastic SOP (FP-48DA)
HN62415TT	120 ns 150 ns 200 ns	44-lead Plastic TSOP (TTP-44D)

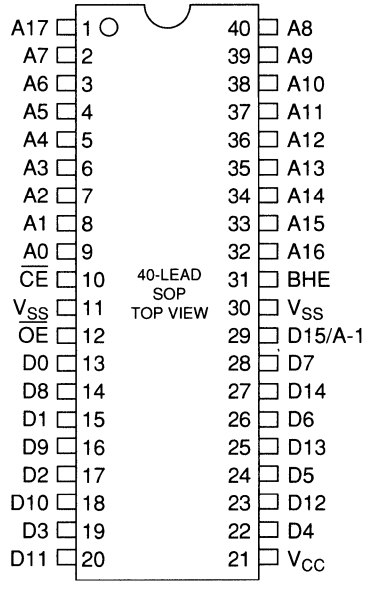
■ PIN ARRANGEMENT

HN62415P Series



(PinD40.HN62415)

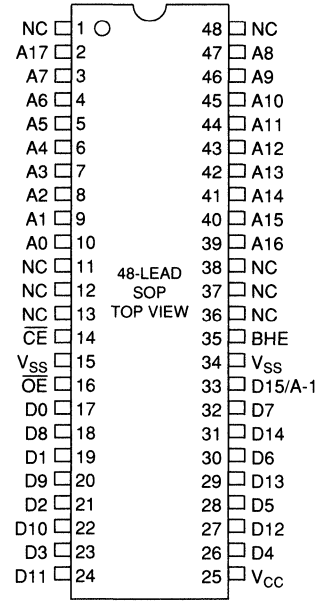
HN62415FA Series



(PinT240.HN62415)

■ PIN ARRANGEMENT (cont.)

HN62415F Series



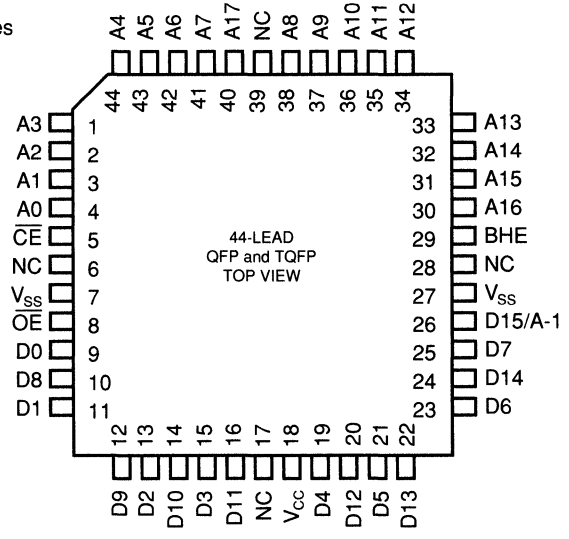
Note:
Pins 11, 12, 13, 36, 37, and 38 are connected to the inner lead frame.

(PinT248.HN62415)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{17}	Address
A_{-1}	Address (Word-Wide)
D_0 - D_{15}	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
BHE	Byte Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

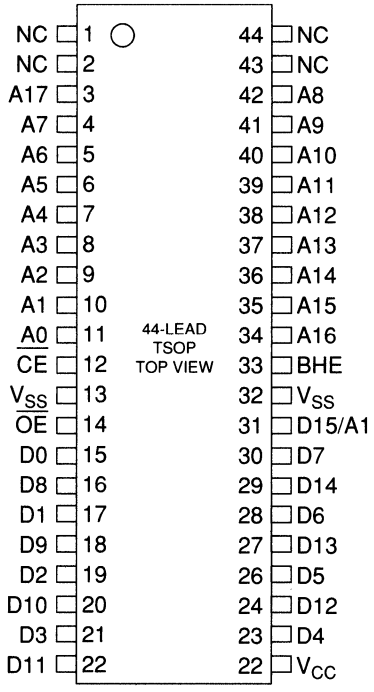
HN62415FP Series
HN62415TFP Series



(PinQ44.HN62415)

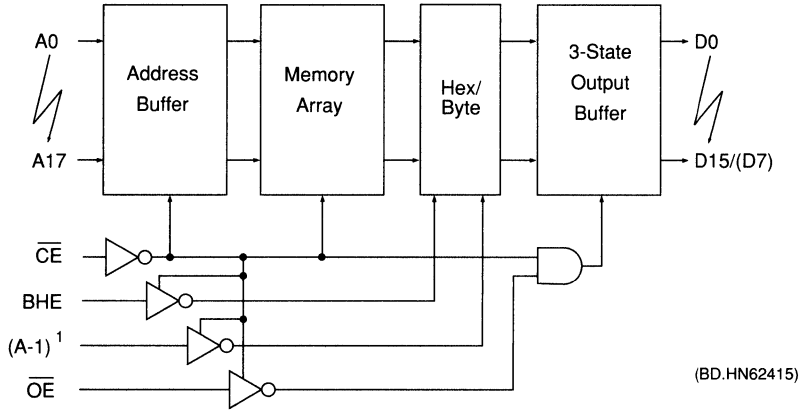
■ PIN ARRANGEMENT (cont.)

HN62415TT Series



(PinT244.HN62415)

■ BLOCK DIAGRAM



(BD.HN62415)

Notes: 1. * : A_{-1} is the Least Significant Address bit in Byte-Wide Mode.
2. BHE=V_{IH} : 16-bit (D_{15} - D_0)
BHE=V_{IL} : 8-bit (D_7 - D_0)
When BHE is low, D_{14} - D_8 are in high impedance states.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
Terminal Voltage [1]	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Notes: 1. With respect to V_{SS}.

■ CAPACITANCE

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0 V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance [1]	C_{IN}	-	15	pF
Output Capacitance [1]	C_{OUT}	-	15	pF

Notes: 1. This parameter is sampled and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Operating V_{CC} Current	I_{CC}	-	75	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = Min.
Standby V_{CC} Current	I_{SB}	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$-0.2V
Input Voltage	V_{IH}	2.2	V_{CC}+0.3	V	
	V_{IL}	-0.3	0.8	V	
Output Voltage	V_{OH}	2.4	-	V	I_{OH} = -205 µA
	V_{OL}	-	0.4	V	I_{OL} = 1.6 mA

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Test Conditions

- Input pulse levels: 0.8 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

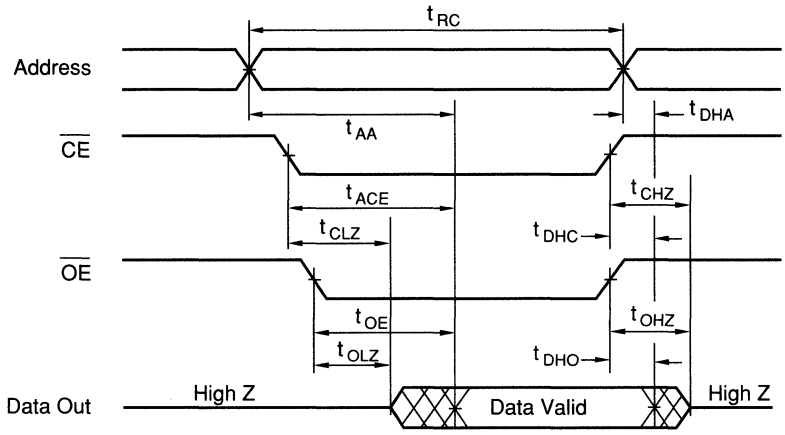
Item	Symbol	HN62415-12		HN62415-15		HN62415-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	120	-	150	-	200	-	ns
Address Access Time	t_{AA}	-	120	-	150	-	200	ns
$\overline{CE}$ Access Time	t_{ACE}	-	120	-	150	-	200	ns
$\overline{OE}$ Access Time	t_{OE}	-	60	-	70	-	100	ns
BHE Access Time	t_{BHE}	-	120	-	150	-	200	ns
Output Hold Time from Address Change	t_{DHA}	0	-	0	-	0	-	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	-	0	-	0	-	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	-	0	-	0	-	ns
Output Hold Time from BHE	t_{DHB}	0	-	0	-	0	-	ns
$\overline{CE}$ to Output in High Z[1]	t_{CHZ}	-	50	-	70	-	70	ns
$\overline{OE}$ to Output in High Z[1]	t_{OHZ}	-	50	-	70	-	70	ns
BHE to Output in High Z[1]	t_{BHZ}	-	50	-	70	-	70	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	5	-	10	-	10	-	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	5	-	10	-	10	-	ns
BHE to Output in Low Z	t_{BLZ}	5	-	10	-	10	-	ns

Note: 1. t_{CHZ}, t_{OHZ}, and t_{BHZ} are defined as the time at which the output becomes an open circuit and are not referenced to output voltage levels.

3

■ READ TIMING WAVEFORM

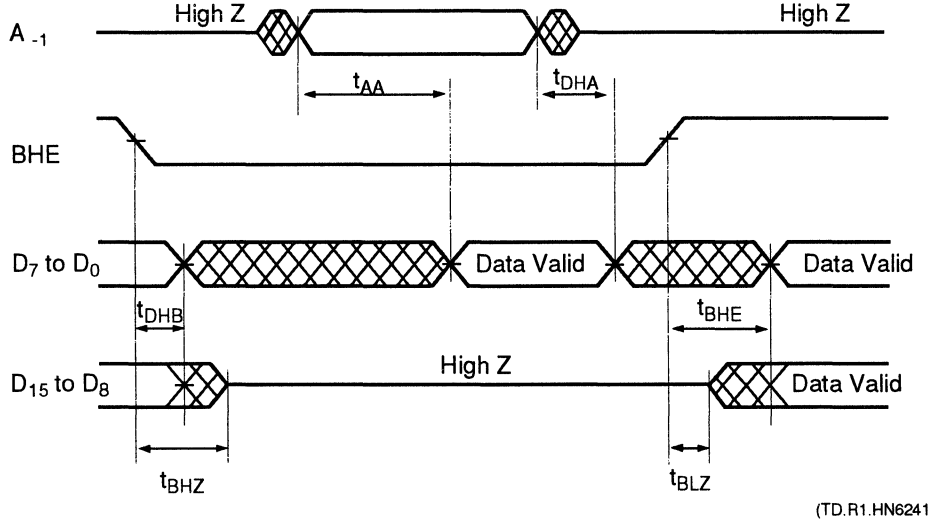
Word Mode (BHE = V_{IH}) or Byte Mode (BHE = V_{IL})



(TD.R.HN62415)

Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

Word Mode/Byte Mode Switch



(TD.R1.HN62415)

Note: 1. $\overline{CE}$ and $\overline{OE}$ are enabled, A_{17} to A_0 are valid.
2. D_{15}/A_{-1} pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enabled. Therefore, the input signals of opposite phase to the output must not be applied to them.

HN62444 Series

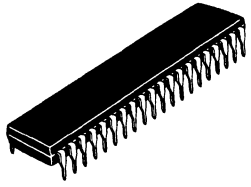
4M (256K x 16-bit) and (512K x 8-bit) Mask ROM

■ DESCRIPTION

The Hitachi HN62444 is a 4-Megabit CMOS Mask Programmable Read Only Memory organized as 262,144 x 16-bit and 524,288 x 8-bit.

The low power consumption of this device makes it ideal for battery powered, portable systems. In addition, the high density and high speed provide enough capacity and high performance to be used as a character generator in laser printers.

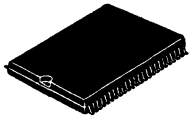
Hitachi's HN62444 is offered with JEDEC-Standard pinouts in 40-pin Plastic DIP and 48-lead Plastic SOP packages. The HN62444 is also packaged in a 44-lead Plastic TFP and a 44-lead Plastic TQFP.



(DP-40)

(FP-44A)

(TFP-44)



(FP-48DA)

■ FEATURES

- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Fast Access Time:
  100 ns (max)
- Low Power Consumption:
  Active Current: 150 mW (typ)
  Standby Current: 5 µW (typ)
- User Selectable Organization:
  256K x 16-bit (Word-Wide)
  512K x 8-bit (Byte-Wide)
  Switchable with BHE pin
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:
  JEDEC Standard Word-Wide/Byte-Wide Pinout
- Packages:
  40-pin Plastic DIP
  44-lead Plastic QFP
  44-lead Plastic TQFP
  48-lead Plastic SOP

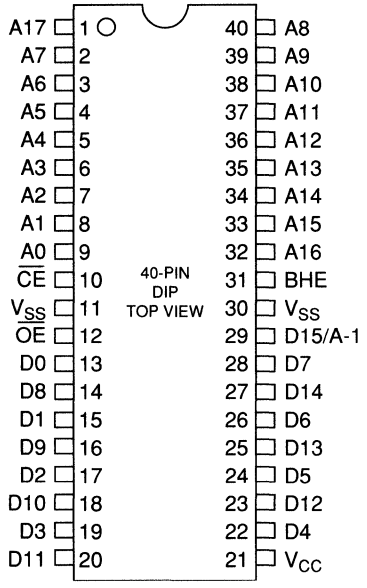
■ ORDERING INFORMATION

Type No.	Access Time	Package
HN62444P	100 ns	40-pin Plastic DIP (DP-40)
HN62444FP	100 ns	44-lead Plastic QFP (FP-44A)
HN62444TFP	100 ns	44-lead Plastic TQFP (TFP-44)
HN62444F	100 ns	48-lead Plastic SOP (FP-48DA)

3

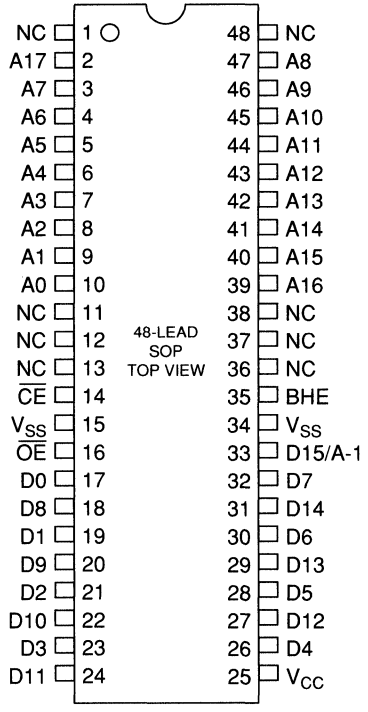
■ PIN ARRANGEMENT

HN62444P Series



(PinD40.HN62444)

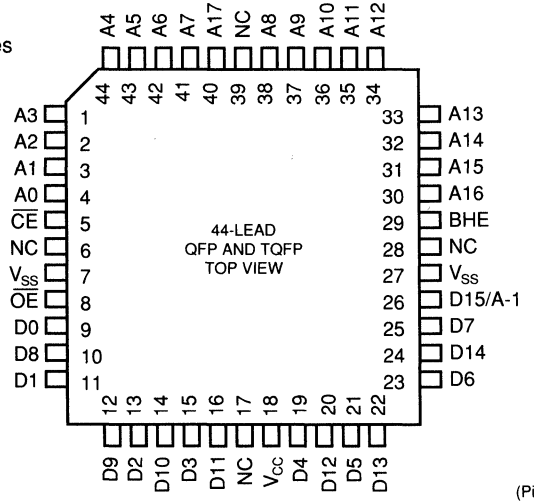
HN62444F Series



Note: Pins 11, 12, 13, 36, 37 and 38 are connected to the inner lead frame.

(PinT248.HN62444)

HN62444FP Series
HN62444TFP Series

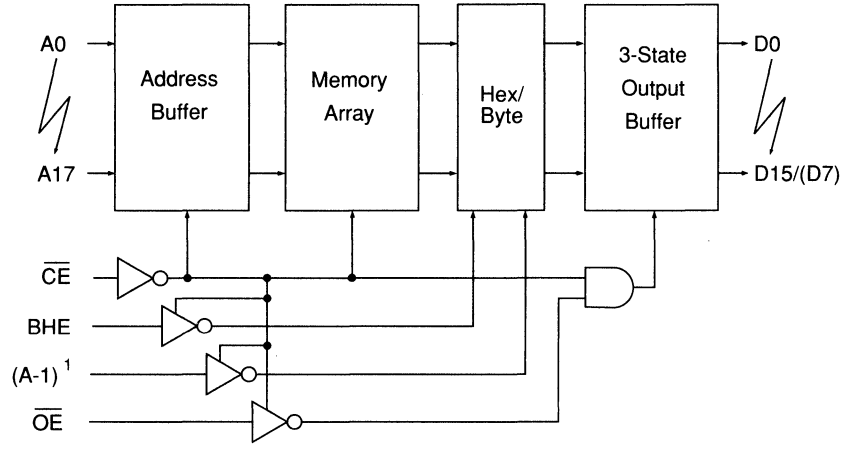


(PinQ44.HN62444)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{17}	Address
A_{-1}	Address (Word-Wide)
D_0 - D_{15}	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
BHE	Byte Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



(BD.HN62444)

Notes: 1. * : A_{-1} is the Least Significant Address bit in Byte-Wide Mode.
2. BHE=V_{IH} : 16-bit (D_{15} - D_0)
BHE=V_{IL} : 8-bit (D_7 - D_0)
When BHE is low, D_{14} - D_8 are in high impedance states.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
Terminal Voltage [1]	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Notes: 1. With respect to V_{SS}.

■ CAPACITANCE

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0 V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance [1]	C_{IN}	-	15	pF
Output Capacitance [1]	C_{OUT}	-	15	pF

Notes: 1. This parameter is sampled and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-	10	µA	$\overline{CE}$ = 2.4 V, V_{OUT} = 0 to V_{CC}
Operating V_{CC} Current	I_{CC}	-	60	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = min.
Standby V_{CC} Current	I_{SB}	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$ - 0.2V
Input Voltage	V_{IH}	2.4	V_{CC}+0.3	V	
	V_{IL}	-0.3	0.45	V	
Output Voltage	V_{OH}	2.4	-	V	I_{OH} = -205 µA
	V_{OL}	-	0.4	V	I_{OL} = 1.6 mA

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

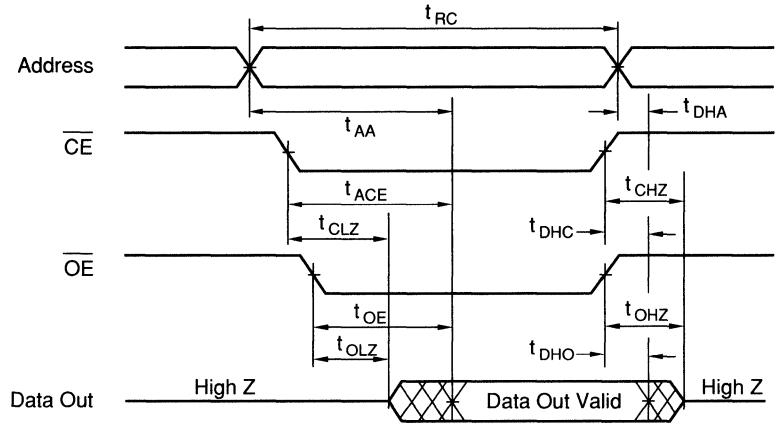
Item	Symbol	Min.	Max.	Unit
Read Cycle Time	t_{RC}	100	-	ns
Address Access Time	t_{AA}	-	100	ns
$\overline{CE}$ Access Time	t_{ACE}	-	100	ns
$\overline{OE}$ Access Time	t_{OE}	-	55	ns
BHE Access Time	t_{BHE}	-	100	ns
Output Hold Time from Address Change	t_{DHA}	0	-	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	-	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	-	ns
Output Hold Time from BHE	t_{DHB}	0	-	ns
$\overline{CE}$ to Output in High Z[1]	t_{CHZ}	-	40	ns
$\overline{OE}$ to Output in High Z[1]	t_{OHZ}	-	40	ns
BHE to Output in High Z[1]	t_{BHZ}	-	40	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	5	-	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	5	-	ns
BHE to Output in Low Z	t_{BLZ}	5	-	ns

Note: 1. t_{CHZ}, t_{OHZ}, and t_{BHZ} are defined as the time at which the output becomes an open circuit and are not referenced to output voltage levels.

3

■ READ TIMING WAVEFORM

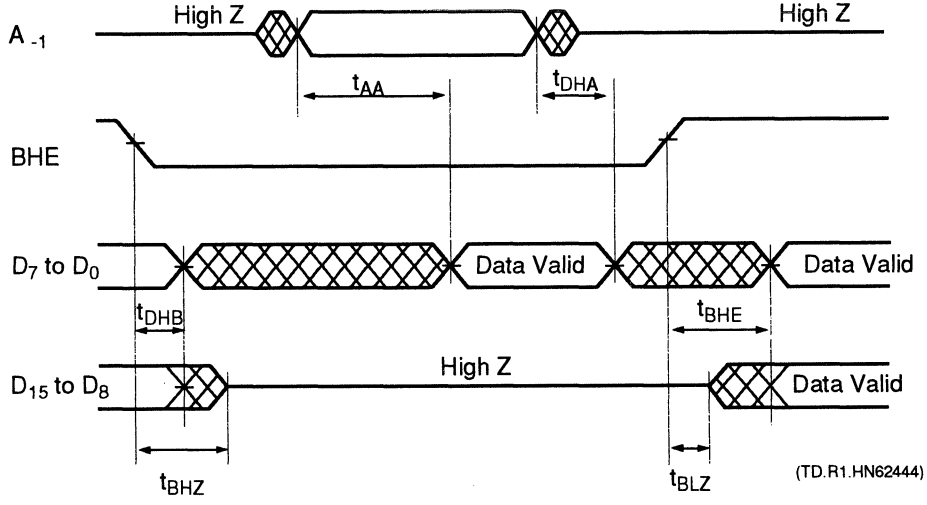
Word Mode (BHE = V_{IH}) or Byte Mode (BHE = V_{IL})



(TD.R.HN62444)

Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

Word Mode/Byte Mode Switch



(TD.R1.HN62444)

Note: 1. If $\overline{CE}$ and $\overline{OE}$ are enabled, A_{19} to A_0 are valid.
2. D_{15}/A_{-1} pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enabled. Therefore, the input signals of opposite phase to the output must not be applied to them.

HN62444B Series

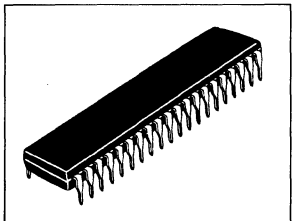
4M (256K x 16-bit) Mask ROM

■ DESCRIPTION

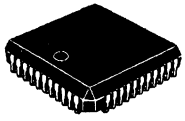
The Hitachi HN62444B is a 4-Megabit CMOS Mask Programmable Read Only Memory organized as 262,144 x 16 bit.

The low power consumption of this device makes it ideal for battery powered, portable systems. In addition , the high density and high speed provide enough capacity and high performance to be used as a character generator in laser printers.

Hitachi's HN62444B is offered with JEDEC-Standard pinouts in 40-pin Plastic DIP and 44-lead PLCC packages.



(DP-40)



(CP-44)

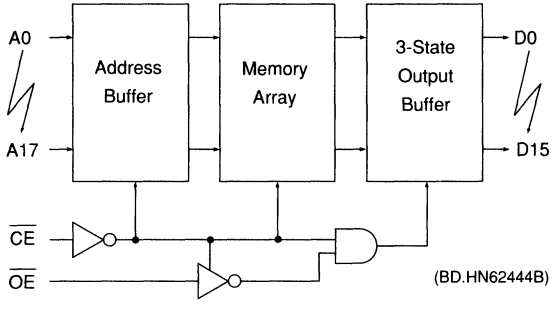
■ FEATURES

- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Fast Access Time:
  100 ns (max)
- Low Power Dissipation:
  Active Current: 150 mW (typ)
  Standby Current: 5 µW (typ)
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:
  JEDEC Standard Word-Wide EPROM Pinout
- Packages:
  40-pin Plastic DIP
  44-lead PLCC

■ ORDERING INFORMATION

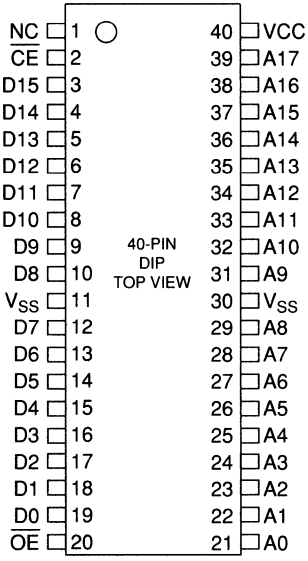
Type No.	Access Time	Package
HN62444BP	100 ns	40-pin Plastic DIP (DP-40)
HN62444BCP	100 ns	44-lead PLCC (CP-44)

■ BLOCK DIAGRAM



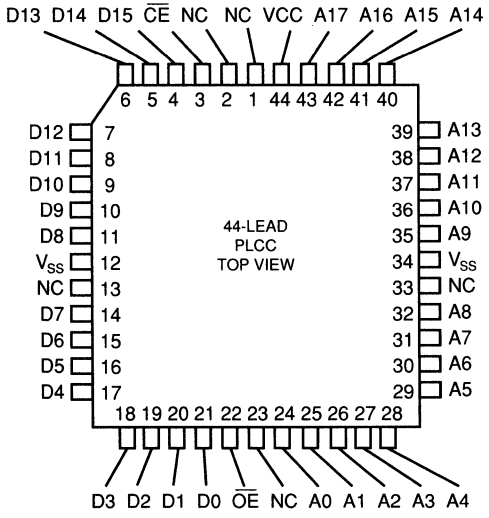
■ PIN ARRANGEMENT

HN62444BP Series



(PinD40.HN62444B)

HN62444BCP Series



(PinQ44.HN62444B)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{17}	Address
D_0 - D_{15}	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage[1]	V_{CC}	-0.3 to +7.0	V
All Input and Output Voltage[1]	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	° C
Storage Temperature Range	T_{STG}	-55 to +125	° C
Temperature Under Bias	T_{BIAS}	-20 to +85	° C

Note: 1. Relative to V_{SS}.

■ CAPACITANCE

(V_{CC} = 5V ± 5%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0V, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit
Input Capacitance	C_{IN}	-	-	15	pF
Output Capacitance	C_{OUT}	-	-	15	pF

Note: 1. This parameter is sampled and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 5%, V_{SS} = 0V, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-	-	10	µA	$\overline{CE}$ = 2.4, V_{OUT} = 0 to V_{CC}
Operating V_{CC} Current	I_{CC}	-	-	100	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = min.
Standby V_{CC} Current	I_{SB1}	-	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{cc}$ to -0.2V
	I_{SB2}	-	-	3	mA	V_{CC} = 5.5 V, $\overline{CE} \geq$ 2.4V
Input Voltage	V_{IH}	2.4	-	V_{CC}+0.3	V	
	V_{IL}	-0.3	-	0.45	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA
	V_{OL}	-	-	0.4	V	I_{OL} = 2.1 mA

3

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 5%, V_{SS} = 0V, T_a = 0 to 70°C)

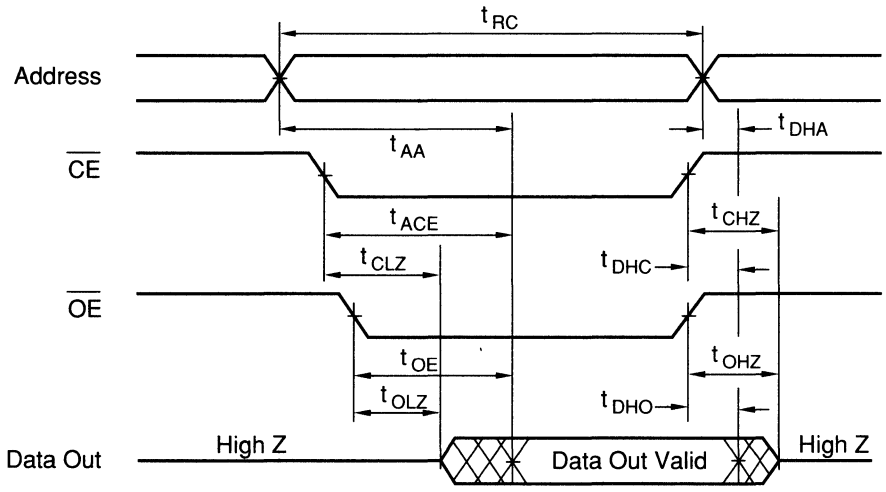
Test Conditions

- Input pulse levels: 0.45 / 2.4V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

Item	Symbol	HN62444B Min.	HN62444B Max.	Test Unit
Read Cycle Time	t_{RC}	100	-	ns
Address Access Time	t_{AA}	-	100	ns
Chip Enable Access Time	t_{ACE}	-	100	ns
Output Enable Access Time	t_{OE}	-	55	ns
Output Hold Time from Address Change	t_{DHA}	0	-	ns
Output Hold Time from Chip Enable	t_{DHC}	0	-	ns
Output Hold Time from Output Enable	t_{DHO}	0	-	ns
Chip Enable to Output in High-Z [1]	t_{CHZ}	-	40	ns
Output Enable to Output in High-Z [1]	t_{OHZ}	-	40	ns
Chip Enable to Output in Low-Z	t_{CLZ}	5	-	ns
Output Enable to Output in Low-Z	t_{OLZ}	5	-	ns

Note: 1. t_{CHZ}, t_{OHZ}, are defined as the time at which the output becomes an open circuit and are not referred to output voltage levels.

■ READ TIMING WAVEFORM



(TD.R.HN62444B)

Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

3

HN62444BN Series

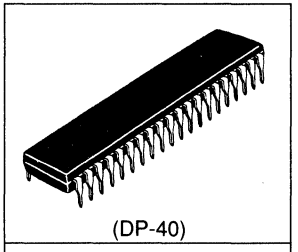
4M (256K x 16-bit) Mask ROM

■ DESCRIPTION

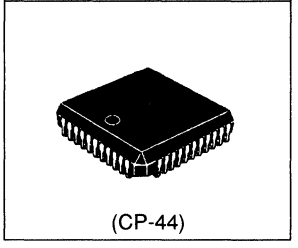
The Hitachi HN62444BN is a 4-Megabit CMOS Mask Programmable Read Only Memory organized as 262,144 x 16-bit.

The high density and high speed Fast Address Access provide enough capacity and high performance to be used in a system using a high speed 16-bit or 32-bit microcomputer. In addition the low power consumption of this device makes it ideal for battery powered, portable systems.

Hitachi's HN62444B is offered with JEDEC-Standard pinouts in 40-pin Plastic DIP and 44-lead PLCC packages.



(DP-40)



(CP-44)

■ FEATURES

- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Normal Access Time:
  120 ns (max)
- Fast Address Access Time (A_0, A_1):
  70 ns (max)
- Low Power Dissipation:
  Active Current: 150 mW (typ)
  Standby Current: 5 µW (typ)
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:
  JEDEC Standard Word-Wide EPROM Pinout
- Packages:
  40-pin Plastic DIP
  44-lead PLCC

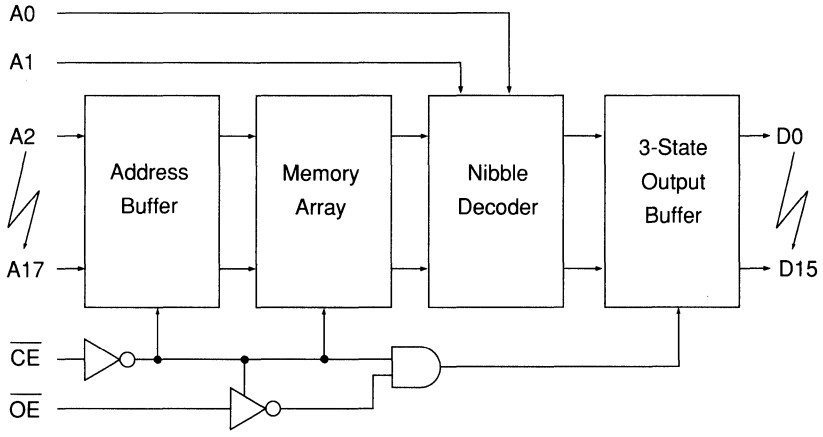
■ ORDERING INFORMATION

Type No.	Access Time	Package
HN62444BNP	120 ns	40-pin Plastic DIP (DP-40)
HN62444BNCP	120 ns	44-lead PLCC (CP-44)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{17}	Address
D_0 - D_{15}	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

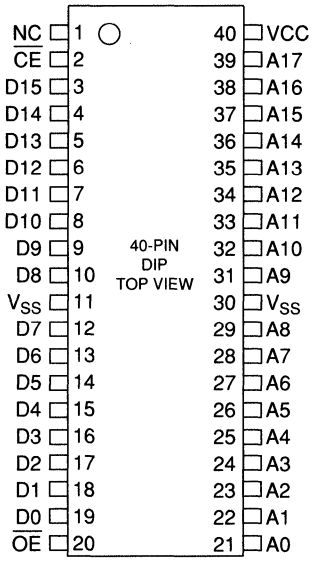
■ BLOCK DIAGRAM



(BD.HN62444BN)

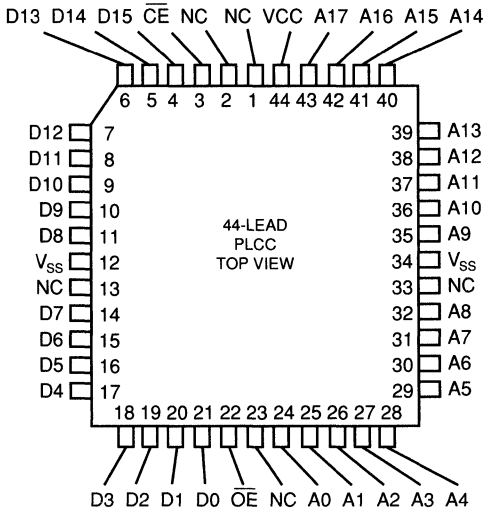
■ PIN ARRANGEMENT

HN62444BPN Series



(PinD40.HN62444BN)

HN62444BCPN Series



(PinQ44.HN62444BN)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage[1]	V_{CC}	-0.3 to +7.0	V
All Input and Output Voltage[1]	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Note: 1. Relative to V_{SS}.

■ CAPACITANCE

(V_{CC} = 5V ± 5%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0V, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit
Input Capacitance	C_{IN}	-	-	15	pF
Output Capacitance	C_{OUT}	-	-	15	pF

Note: 1. This parameter is sampled and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 5%, V_{SS} = 0V, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-	-	10	µA	$\overline{CE}$ = 2.4, V_{OUT} = 0 to V_{CC}
Operating V_{CC} Current	I_{CC}	-	-	120	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = min.
Standby V_{CC} Current	I_{SB1}	-	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{cc}$ to -0.2V
	I_{SB2}	-	-	3	mA	V_{CC} = 5.5 V, $\overline{CE} \geq$ 2.4V
Input Voltage	V_{IH}	2.4	-	V_{CC}+0.3	V	
	V_{IL}	-0.3	-	0.45	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA
	V_{OL}	-	-	0.4	V	I_{OL} = 2.1 mA

3

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 5%, V_{SS} = 0V, T_a = 0 to 70°C)

Test Conditions

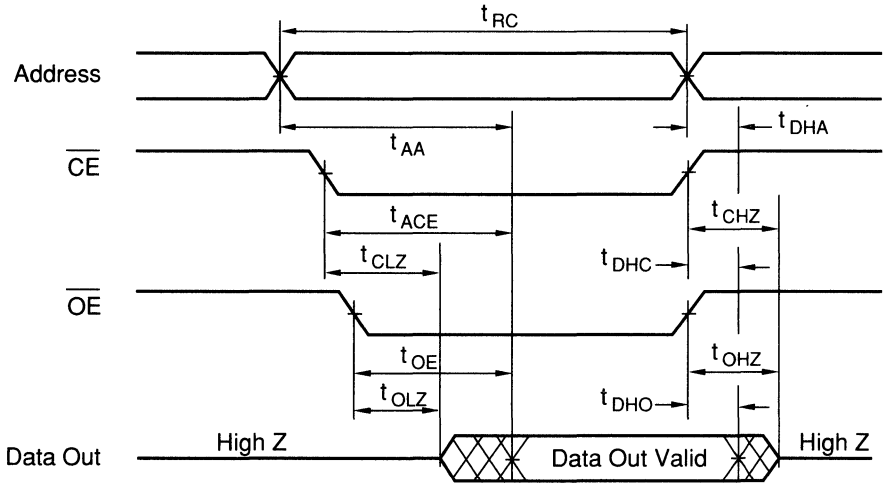
- Input pulse levels: 0.45 / 2.4V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

Item	Symbol	HN62444BN-12		Test Unit
		Min.	Max.	
Read Cycle Time	t_{RC}	120	-	ns
Burst Read Cycle Time	t_{BC}	70	-	ns
Address Access Time	t_{AA}	-	120	ns
Burst Address Access Time	t_{BA}	-	70	ns
Chip Enable Access Time	t_{ACE}	-	120	ns
Output Enable Access Time	t_{OE}	-	55	ns
Output Hold Time from Address Change	t_{DHA}	0	-	ns
Output Hold Time from Chip Enable	t_{DHC}	0	-	ns
Output Hold Time from Output Enable	t_{DHO}	0	-	ns
Chip Enable to Output in High-Z [1]	t_{CHZ}	-	40	ns
Output Enable to Output in High-Z [1]	t_{OHZ}	-	40	ns
Chip Enable to Output in Low-Z	t_{CLZ}	5	-	ns
Output Enable to Output in Low-Z	t_{OLZ}	5	-	ns

Note: 1. t_{CHZ}, t_{OHZ}, are defined as the time at which the output becomes an open circuit and are not referred to output voltage levels.

■ READ TIMING WAVEFORM

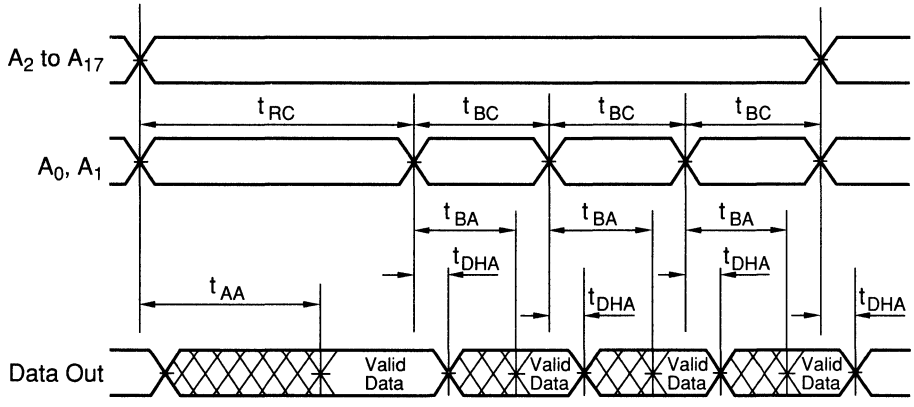
1) Normal Mode:



(TD.R.HN62444BN)

Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

2) Fast Address Access Mode:



(TD.RN.HN62444BN)

Note: $\overline{CE}$ and $\overline{OE}$ are enabled.

HN62314B Series
HN62334B Series

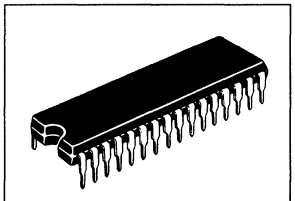
4M (512K x 8-bit) Mask ROM

■ DESCRIPTION

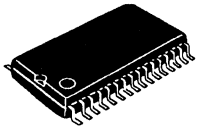
The Hitachi HN62314B/HN62334B Series is a 4-Megabit CMOS Mask Programmable Read Only Memory organized as 524,288 x 8-bit.

The low power consumption of this device makes it ideal for battery powered, portable systems. In addition , the high density and high speed provide enough capacity and high performance to be used as a character generator in laser printers.

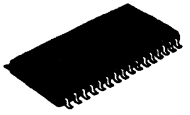
Hitachi's HN62314B/HN62334B Series are offered with JEDEC-Standard Byte-Wide EPROM pinouts in 32-pin Plastic DIP and 32-lead Plastic SOP and TSOP packages. This allows socket replacement with EPROMs and Flash Memory.



(DP-32)



(FP-32D)



(TTP-32D)

■ FEATURES

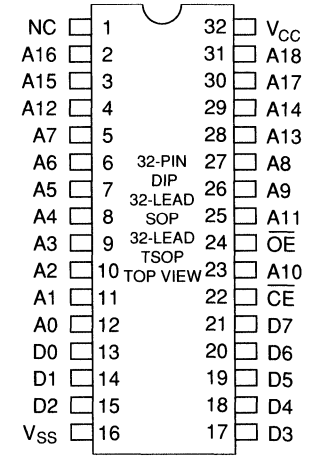
- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Fast Access Times:
  150 ns/170 ns/200 ns (max)
- Low Power Consumption:
  Active Current: 100 mW (typ)
  Standby Current: 5 µW (typ)
- Byte-Wide Data Organization
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangement:
  JEDEC Standard Byte-Wide EPROM
  EPROM and Flash Memory Compatible
- Packages:
  32-pin Plastic DIP
  32-lead Plastic SOP
  32-lead Plastic TSOP (Type II)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN62334BP	150 ns	32-pin Plastic DIP
HN62314BP	170 ns/200 ns	(DP-32)
HN62334BF	150 ns	32-lead Plastic SOP
HN62314BF	170 ns/200 ns	(FP-32D)
HN62334BTT	150 ns	32-lead Plastic TSOP
HN62314BTT	170 ns/200 ns	(TTP-32D)

■ PIN ARRANGEMENT

HN62314BP/F Series
HN62334BP/F Series

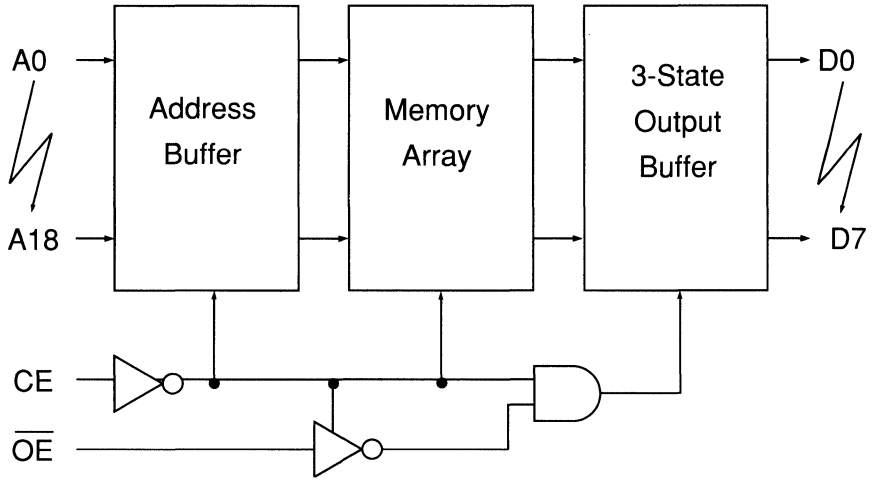


(PinD32.HN62314B,334B)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{18}	Address
D_0 - D_7	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



(BD.HN62314B,334B)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
Terminal Voltage [1]	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Notes: 1. With respect to V_{SS}.

■ CAPACITANCE

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0 V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance [1]	C_{IN}	-	15	pF
Output Capacitance [1]	C_{OUT}	-	15	pF

Notes: 1. This parameter is sampled and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Operating V_{CC} Current	I_{CC}	-	50	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = min.
Standby V_{CC} Current	I_{SB}	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$-0.2V
Input Voltage	V_{IH}	2.2	V_{CC}+0.3	V	
	V_{IL}	-0.3	0.8	V	
Output Voltage	V_{OH}	2.4	-	V	I_{OH} = -205 µA
	V_{OL}	-	0.4	V	I_{OL} = 1.6 mA

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

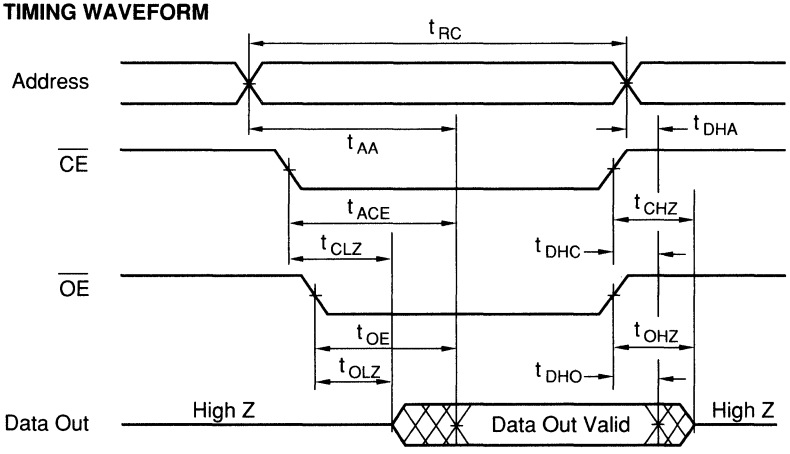
Test Conditions

- Input pulse levels: 0.8 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

Item	Symbol	HN62334B-15		HN62314B-17		HN62314B-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	150	-	170	-	200	-	ns
Address Access Time	t_{AA}	-	150	-	170	-	200	ns
$\overline{CE}$ Access Time	t_{ACE}	-	150	-	170	-	200	ns
$\overline{OE}$ Access Time	t_{OE}	-	70	-	70	-	100	ns
Output Hold Time from Address Change	t_{DHA}	0	-	0	-	0	-	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	-	0	-	0	-	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	-	0	-	0	-	ns
$\overline{CE}$ to Output in High Z	t_{CHZ} [1]	-	70	-	70	-	70	ns
$\overline{OE}$ to Output in High Z	t_{OHZ} [1]	-	70	-	70	-	70	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	10	-	10	-	10	-	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	-	10	-	10	-	ns

Note: 1. t_{CHZ} and t_{OHZ} define the time at which the output becomes an open circuit and are not referenced to output voltage levels.

■ READ TIMING WAVEFORM



(TD.R.HN62314B,334B)

Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

HN62344B Series

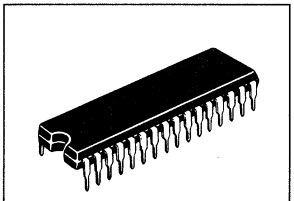
4M (512K x 8-bit) Mask ROM

■ DESCRIPTION

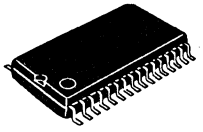
The Hitachi HN62344B is a 4-Megabit CMOS Mask Programmable Read Only Memory organized as 524,288 x 8-bit.

The low power consumption of this device makes it ideal for battery powered, portable systems. In addition, the high density and high speed provide enough capacity and high performance to be used as a character generator in laser printers.

Hitachi's HN62344B is offered with JEDEC-Standard Byte-Wide EPROM pinouts in 32-pin Plastic DIP and 32-lead Plastic SOP packages. This allows socket replacement with EPROMs and Flash Memory.



(DP-32)



(FP-32D)

■ FEATURES

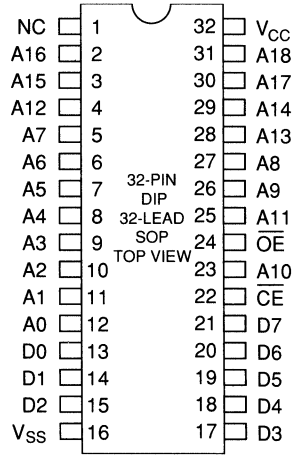
- Single Power Supply:
  V_{CC} = 5 V ± 5%
- High Speed Access Time:
  100 ns (max)
- Low Power Consumption:
  Active Current: 150 mW (typ)
  Standby Current: 5 μW (typ)
- Byte-Wide Data Organization
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:
  JEDEC Standard Byte-Wide EPROM
  EPROM and Flash Memory Compatible
- Packages:
  32-pin Plastic DIP
  32-lead Plastic SOP

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN62344BP-10	100 ns	32-pin Plastic DIP (DP-32)
HN62344BF-10	100 ns	32-lead Plastic SOP (FP-32D)

■ PIN ARRANGEMENT

HN62344BP Series
HN62344BF Series

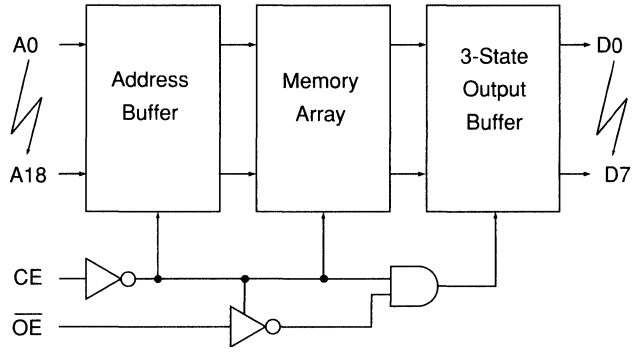


(PinD32.HN62344B)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{18}	Address
D_0 - D_7	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



(BD.HN62344B)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
All Input and Output Voltage [1]	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Notes: 1. With respect to V_{SS}.

■ CAPACITANCE

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0 V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance [1]	C_{IN}	-	15	pF
Output Capacitance [1]	C_{OUT}	-	15	pF

Notes: 1. This parameter is sampled and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 5%, V_{SS} = 0 V, T_a = 0 to 70°C)

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-	10	µA	$\overline{CE}$ = 2.4 V, V_{OUT} = 0 to V_{CC}
Operating V_{CC} Current	I_{CC}	-	60	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC}= min.
Standby V_{CC} Current	I_{SB1}	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$ - 0.2V
	I_{SB2}		3	mA	V_{CC} = 5.5 V, $\overline{CE} \geq$ 2.4V
Input Voltage	V_{IH}	2.4	V_{CC}+0.3	V	
	V_{IL}	-0.3	0.45	V	
Output Voltage	V_{OH}	2.4	-	V	I_{OH} = -205 µA
	V_{OL}	-	0.4	V	I_{OL} = 1.6 mA

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 5%, V_{SS} = 0 V, T_a = 0 to 70°C)

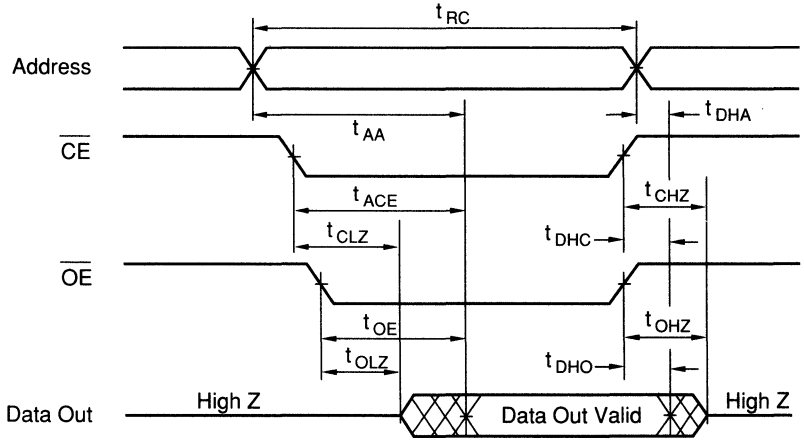
Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

Item	Symbol	Min.	Max.	Unit
Read Cycle Time	t_{RC}	100	-	ns
Address Access Time	t_{AA}	-	100	ns
Chip Enable Access Time	t_{ACE}	-	100	ns
Output Enable Access Time	t_{OE}	-	55	ns
Output Hold Time from Address Change	t_{DHA}	0	-	ns
Output Hold Time from Chip Enable	t_{DHC}	0	-	ns
Output Hold Time from Output Enable	t_{DHO}	0	-	ns
Chip Enable to Output in High Z	t_{CHZ} [1]	-	40	ns
Output Enable to Output in High Z	t_{OHZ} [1]	-	40	ns
Chip Enable to Output in Low Z	t_{CLZ}	5	-	ns
Output Enable to Output in Low Z	t_{OLZ}	5	-	ns

Note: 1. t_{CHZ}, and t_{OHZ} define the time at which the output becomes an open circuit and are not referenced to output voltage levels.

■ READ TIMING WAVEFORM



(TD.R.HN62344B)

Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

HN62418 Series
HN62428 Series

8M (512K x 16-bit) and (1M x 8-bit) Mask ROM

■ DESCRIPTION

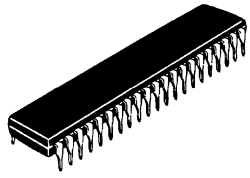
The Hitachi HN62418/428 Series is an 8-Megabit CMOS Mask Programmable Read Only Memory organized either as 524,288 x 16-bit or as 1,048,576 x 8-bit.

The low power consumption of this device makes it ideal for battery powered, portable systems. In addition , the high density and high speed provide enough capacity and high performance to be used as a character generator in laser printers.

Hitachi's HN62418/428 is offered with JEDEC-Standard pinouts in 42-pin Plastic DIP and 44-lead Plastic QFP packages. The HN62418 is also packaged in a 44-lead TQFP, a 44-lead Plastic SOP and TSOP and a 48-lead Plastic SOP.

■ FEATURES

- Single Power Supply
  V_{CC} = 5 V ± 10%
- Fast Access Time:
  150 ns (max)
- Low Power Consumption:
  Active Current: 100 mW (typ)
  Standby Current: 5 μW (typ)
- User Selectable Organization:
  1M x 16-bit (Word-Wide)
  2M x 8-bit (Byte-Wide)
  Switchable with BHE pin
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:
  JEDEC Standard Word-Wide/Byte-Wide Pinout
- Packages:
  42-pin Plastic DIP
  44-lead Plastic QFP
  44-lead TQFP
  44-lead Plastic SOP
  48-lead Plastic SOP
  44-lead Plastic TSOP (Type II)



(DP-42)

(FP-44A)

(TFP-44)

(FP-44D)

(FP-48DA)

(TTP-44D)

3

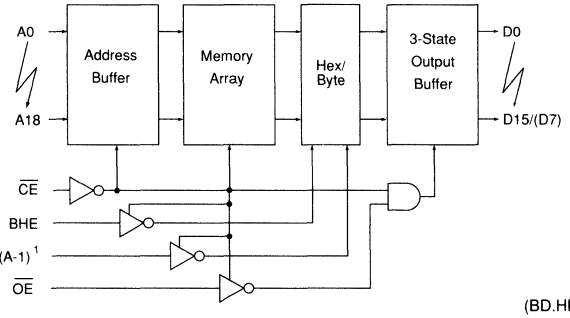
■ORDERING INFORMATION

Type No.	Access Time	Package
HN62418/428P	150 ns/200 ns	42-pin Plastic DIP (DP-42)
HN62418/428FP	150 ns/200 ns	44-lead Plastic QFP (FP-44A)
HN62418/428TFP	150 ns/200 ns	44-lead TQFP (TFP-44)
HN62418/428FB	150 ns/200 ns	44-lead Plastic SOP (FP-44D)
HN62418/428F	150 ns/200 ns	48-lead Plastic SOP (FP-48DA)
HN62418/428TT	150 ns/200 ns	44-lead Plastic TSOP (TTP-44D)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{18}	Address
A_{-1}	Address (Word-Wide)
D_0 - D_{15}	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
BHE	Byte Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM

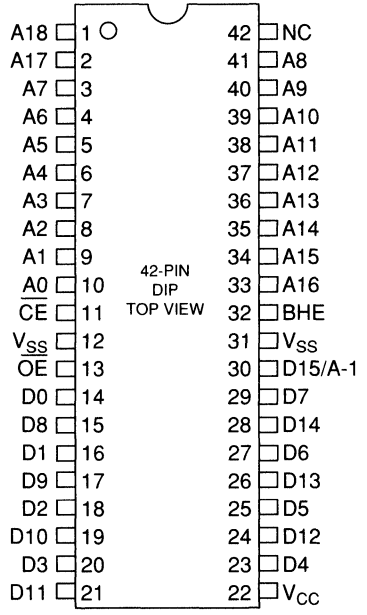


(BD.HN62418)

Notes: 1. * : A_{-1} is the Least Significant Address bit in Byte-Wide Mode.
2. BHE=V_{IH} : 16-bit (D_{15} - D_0)
BHE=V_{IL} : 8-bit (D_7 - D_0)
When BHE is low, D_{14} - D_8 are in high impedance states.

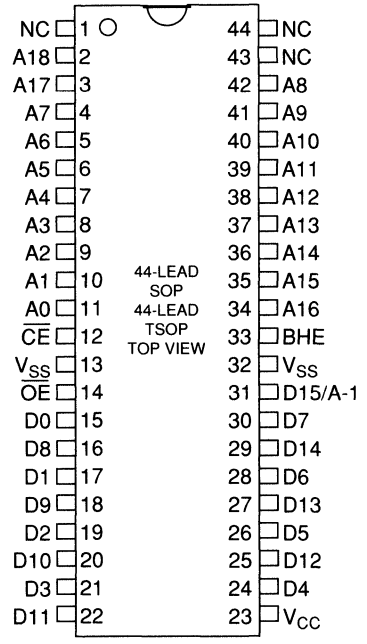
■ PIN ARRANGEMENT

HN62418/428P Series



(PinD42.HN62418)

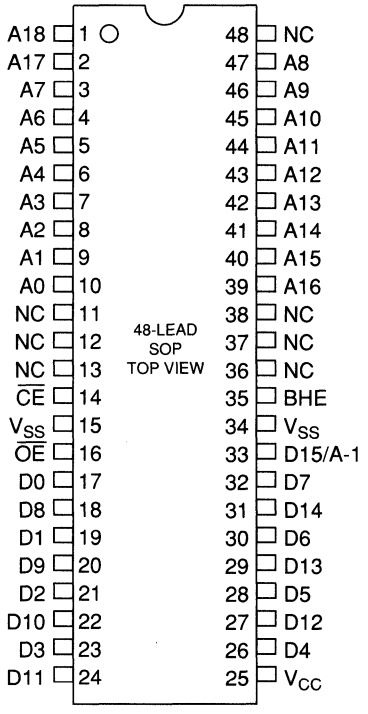
HN62418/428FB Series
HN62418/428TT Series



(PinD44.HN62418)

■ PIN ARRANGEMENT (cont.)

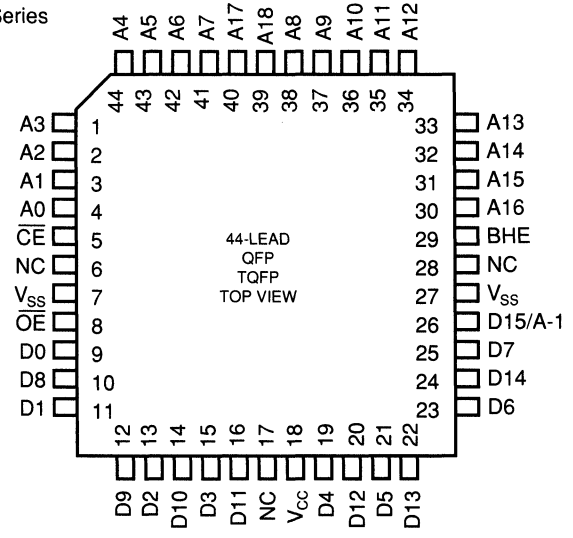
HN62418/428F Series



Note:
Pins 11, 12, 13, 36, 37 and 38 are connected to the inner lead frame.

(PinT248.HN62418)

HN62418/428FP Series
HN62418/428TFP Series



(PinQ44.HN62418)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
All Input and Output Voltage [1]	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	° C
Storage Temperature Range	T_{STG}	-55 to +125	° C
Temperature Under Bias	T_{BIAS}	-20 to +85	° C

Notes: 1. With respect to V_{SS}.

■ CAPACITANCE

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0 V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance [1]	C_{IN}	-	15	pF
Output Capacitance [1]	C_{OUT}	-	15	pF

Notes: 1. This parameter is sampled and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Operating V_{CC} Current	I_{CC}	-	50	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC}= Min.
Standby V_{CC} Current	I_{SB}	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$-0.2V
Input Voltage	V_{IH}	2.2	V_{CC}+0.3	V	
	V_{IL}	-0.3	0.8	V	
Output Voltage	V_{OH}	2.4	-	V	I_{OH} = -205 µA
	V_{OL}	-	0.4	V	I_{OL} = 1.6 mA

3

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Test Conditions

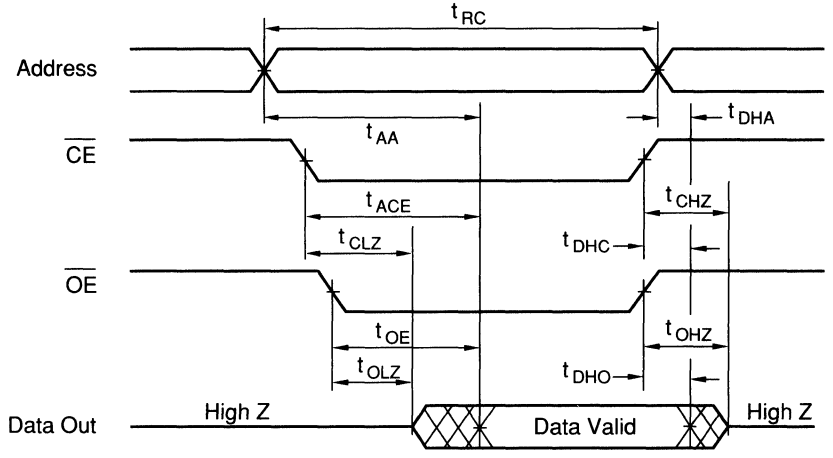
- Input pulse levels: 0.8 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

		HN62418		HN62428		
Item	Symbol	Min.	Max.	Min.	Max	Unit
Read Cycle Time	t_{RC}	150	-	200	-	ns
Address Access Time	t_{AA}	-	150	-	200	ns
CE Access Time	t_{ACE}	-	150	-	200	ns
OE Access Time	t_{OE}	-	70	-	100	ns
BHE Access Time	t_{BHE}	-	150	-	200	ns
Output Hold Time from Address Change	t_{DHA}	0	-	0	-	ns
Output Hold Time from CE	t_{DHC}	0	-	0	-	ns
Output Hold Time from OE	t_{DHO}	0	-	0	-	ns
Output Hold Time from BHE	t_{DHB}	0	-	0	-	ns
CE to Output in High Z	t_{CHZ}[1]	-	70	-	70	ns
OE to Output in High Z	t_{OHZ}[1]	-	70	-	70	ns
BHE to Output in High Z	t_{BHZ}[1]	-	70	-	70	ns
CE to Output in Low Z	t_{CLZ}[1]	10	-	10	-	ns
OE to Output in Low Z	t_{OLZ}[1]	10	-	10	-	ns
BHE to Output in Low Z	t_{BLZ}[1]	10	-	10	-	ns

Note: 1. t_{CHZ}, t_{OHZ}, and t_{BHZ} define the time at which the output becomes an open circuit and are not referenced to output voltage levels.

■ READ TIMING WAVEFORM

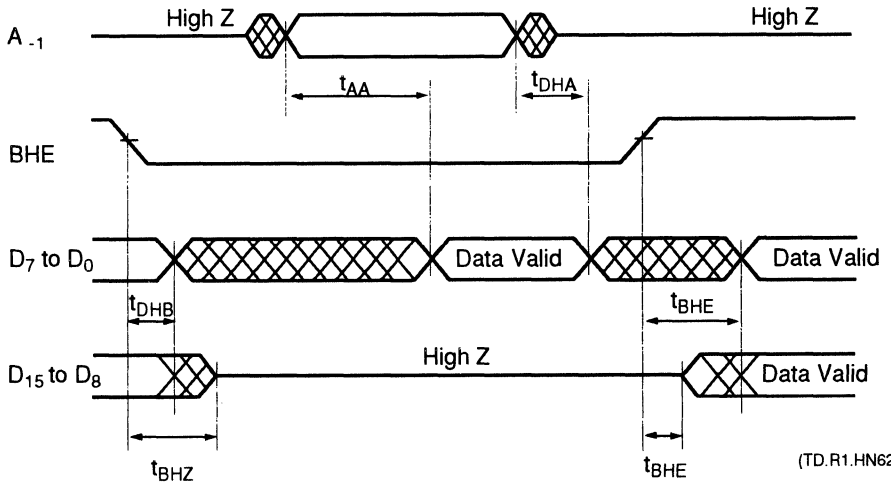
Word Mode (BHE = V_{IH}) or Byte Mode (BHE = V_{IL})



(TD.R.HN62418)

Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

Word Mode/Byte Mode Switch



(TD.R1.HN62418)

Note: 1. $\overline{CE}$ and $\overline{OE}$ are of select status. A_{18} to A_9 are fixed.
2. D_{15}/A-1 terminal is of output state when $\overline{BHE}$ = V_{IH}, $\overline{CE}$ and $\overline{OE}$ are of selected state. At this time, an input signal that is of the inverse phase to the output should not be impressed.

8M (512K x 16-bit) and (1M x 8-bit) Mask ROM

■ DESCRIPTION

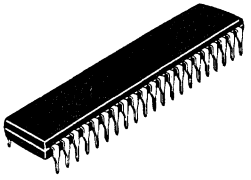
The Hitachi HN62W428 Series is an 8-Megabit CMOS Mask Programmable Read Only Memory organized either as 524,288 x 16-bit or as 1,048,576 x 8-bit.

The low voltage and low power consumption of this device makes it ideal for battery powered, portable systems. In addition , the high density and high speed provide enough capacity and high performance to be used as a character generator in laser printers.

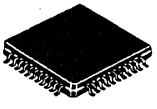
Hitachi's HN62W428 is offered with JEDEC-Standard pinouts in 42-pin Plastic DIP and 44-lead Plastic QFP packages. The HN62W428 is also packaged in a 44-lead TQFP, a 44-lead Plastic SOP and TSOP and a 48-lead Plastic SOP.

■ FEATURES

- Single Power Supply
  V_{CC} = 3.0 to 5.5V
- Access Time:
  300 ns (max)
- Low Power Consumption:
  Active Current: 100 mW (typ)
  Standby Current: 5 µW (typ)
- User Selectable Organization:
  1M x 16-bit (Word-Wide)
  2M x 8-bit (Byte-Wide)
  Switchable with BHE pin
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:
  JEDEC Standard Word-Wide/Byte-Wide Pinout
- Packages:
  42-pin Plastic DIP
  44-lead Plastic QFP
  44-lead TQFP
  44-lead Plastic SOP
  48-lead Plastic SOP
  44-lead Plastic TSOP (Type II)



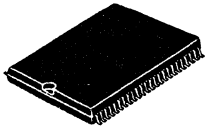
(DP-42)



(FP-44A)

(TFP-44)

(FP-44D)



(FP-48DA)

(TTP-44D)

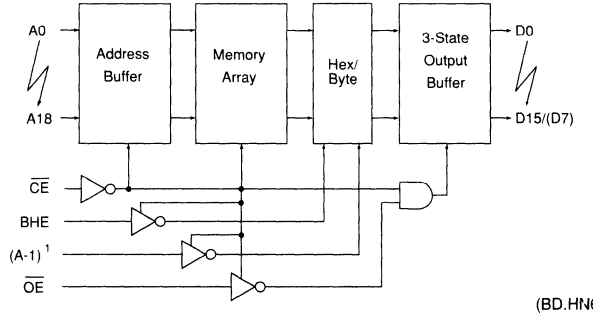
■ORDERING INFORMATION

Type No.	Access Time	Package
HN62W428P	300 ns	42-pin Plastic DIP (DP-42)
HN62W428FP	300 ns	44-lead Plastic QFP (FP-44A)
HN62W428TFP	300 ns	44-lead TQFP (TFP-44)
HN62W428FB	300 ns	44-lead Plastic SOP (FP-44D)
HN62W428F	300 ns	48-lead Plastic SOP (FP-48DA)
HN62W428TT	300 ns	44-lead Plastic TSOP (TTP-44D)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{18}	Address
A_{-1}	Address (Word-Wide)
D_0 - D_{15}	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
BHE	Byte Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM

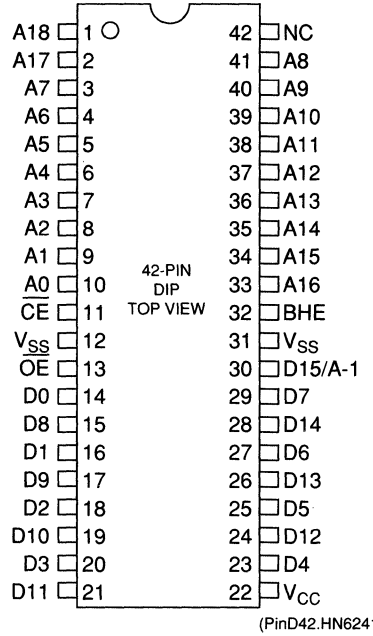


(BD.HN62418)

Notes: 1. * : A_{-1} is the Least Significant Address bit in Byte-Wide Mode.
2. BHE=V_{IH} : 16-bit (D_{15} - D_0)
BHE=V_{IL} : 8-bit (D_7 - D_0)
When BHE is low, D_{14} - D_8 are in high impedance states.

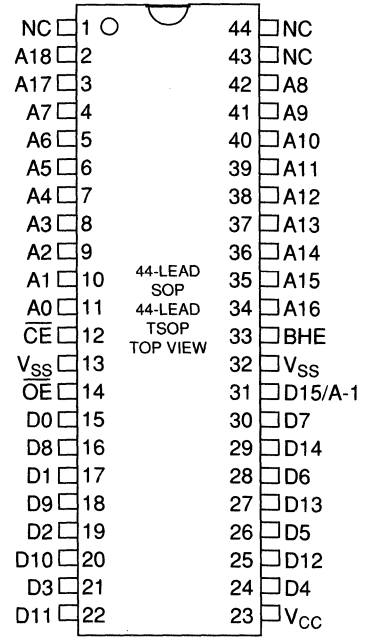
■ PIN ARRANGEMENT

HN62W428P Series



(PinD42.HN62418)

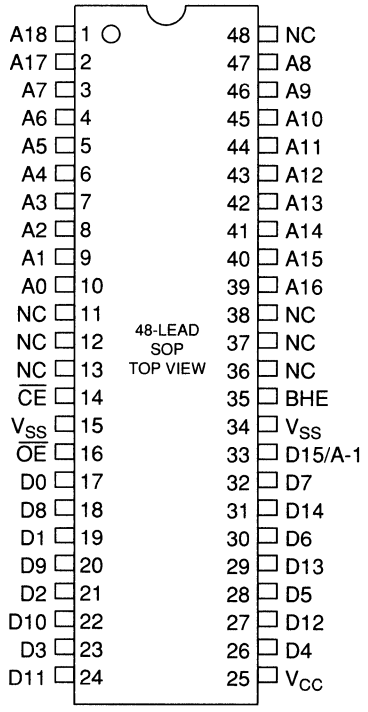
HN62W428FB Series
HN62W428TT Series



(PinD44.HN62418)

■ PIN ARRANGEMENT (cont.)

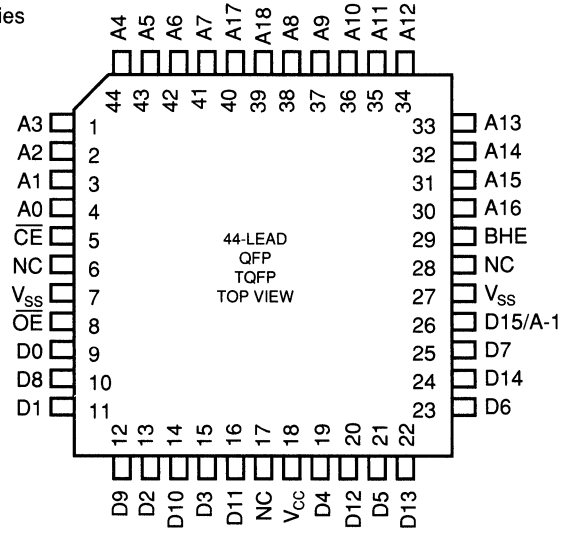
HN62W428F Series



Note:
Pins 11, 12, 13, 36, 37 and 38 are connected to the inner lead frame.

(PinT248.HN62418)

HN62W428FP Series
HN62W428TFP Series



(PinQ44.HN62418)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
All Input and Output Voltage [1]	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Notes: 1. With respect to V_{SS}.

■ CAPACITANCE

(V_{CC} = 3.0 to 5.5V, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0 V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance [1]	C_{IN}	-	15	pF
Output Capacitance [1]	C_{OUT}	-	15	pF

Notes: 1. This parameter is sampled and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 3.0 to 5.5V, V_{SS} = 0 V, T_a = 0 to 70°C)

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Operating V_{CC} Current	I_{CC}	-	25	mA	V_{CC} = 3.5 V, I_{DOUT} = 0 mA, t_{RC}= Min.
Standby V_{CC} Current	I_{SB}	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$-0.2V
Input Voltage	V_{IH}	2.2	V_{CC}+0.3	V	
	V_{IL}	-0.3	0.8	V	
Output Voltage	V_{OH}	2.4	-	V	I_{OH} = -205 µA
	V_{OL}	-	0.4	V	I_{OL} = 1.6 mA

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 3.0 to 5.5V, V_{SS} = 0 V, T_a = 0 to 70°C)

Test Conditions

- Input pulse levels: 0.8 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

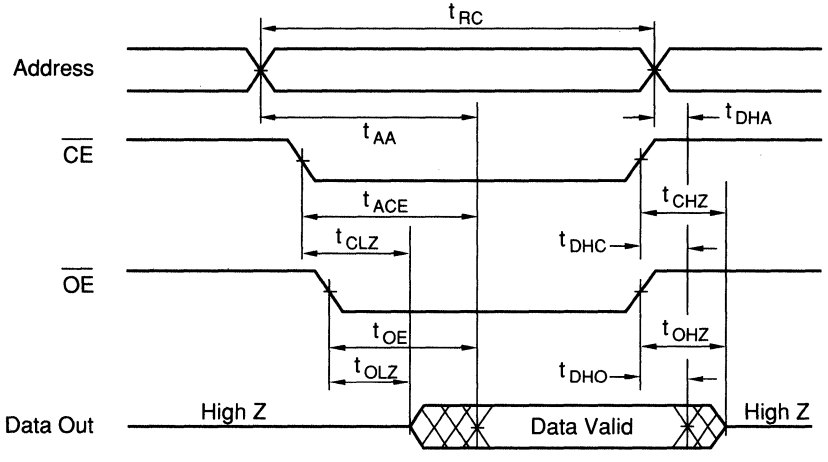
Item	Symbol	HN62W428 Min.	HN62W428 Max.	Unit
Read Cycle Time	t_{RC}	300	-	ns
Address Access Time	t_{AA}	-	300	ns
CE Access Time	t_{ACE}	-	300	ns
OE Access Time	t_{OE}	-	150	ns
BHE Access Time	t_{BHE}	-	300	ns
Output Hold Time from Address Change	t_{DHA}	0	-	ns
Output Hold Time from CE	t_{DHC}	0	-	ns
Output Hold Time from OE	t_{DHO}	0	-	ns
Output Hold Time from BHE	t_{DHB}	0	-	ns
CE to Output in High Z	t_{CHZ}[1]	-	100	ns
OE to Output in High Z	t_{OHZ}[1]	-	100	ns
BHE to Output in High Z	t_{BHZ}[1]	-	100	ns
CE to Output in Low Z	t_{CLZ}[1]	10	-	ns
OE to Output in Low Z	t_{OLZ}[1]	10	-	ns
BHE to Output in Low Z	t_{BLZ}[1]	10	-	ns

Note: 1. t_{CHZ}, t_{OHZ}, and t_{BHZ} define the time at which the output becomes an open circuit and are not referenced to output voltage levels.

3

■ READ TIMING WAVEFORM

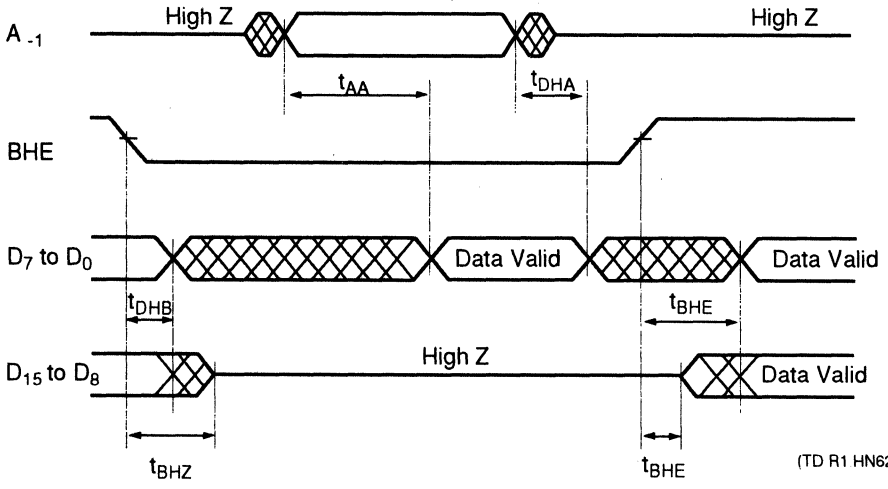
Word Mode (BHE = V_{IH}) or Byte Mode (BHE = V_{IL})



(TD.R.HN62418)

Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

Word Mode/Byte Mode Switch



(TD R1 HN62418)

Note: 1. $\overline{CE}$ and $\overline{OE}$ are of select status. A_{18} to A_0 are fixed.
2. D_{15}/A-1 terminal is of output state when $\overline{BHE}$ = V_{IH}, $\overline{CE}$ and $\overline{OE}$ are of selected state. At this time, an input signal that is of the inverse phase to the output should not be impressed.

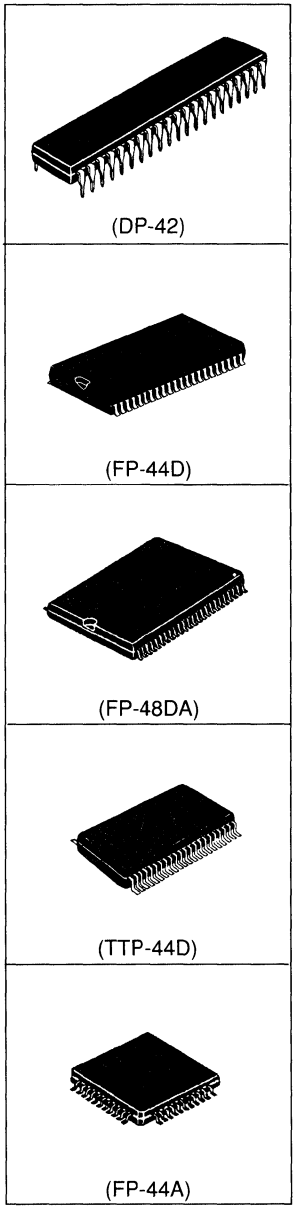
8M (512K x 16-bit) and (1M x 8-bit) Mask ROM

■ DESCRIPTION

The Hitachi HN62438 Series is an 8-Megabit CMOS Mask Programmable Read Only Memory organized either as 524,288 x 16-bit or as 1,048,576 x 8-bit.

The high density and high speed access provide enough capacity and high performance to be used in a system using a high speed 16-bit or 32-bit microcomputer. In addition the low power consumption of this device makes it ideal for battery powered, portable systems.

Hitachi's HN62438 is offered with JEDEC-Standard pinouts in 42-pin Plastic DIP, 44-lead Plastic SOP, 44-lead Plastic TSOP and 44-lead Plastic QFP packages. The HN62438 is also packaged in a 48-lead Plastic SOP.



■ FEATURES

- Single Power Supply
  V_{CC} = 5 V ± 10%
- Fast Access Times:
  100 ns/120 ns (max)
- Low Power Consumption:
  Active Current: 250 mW (typ)
  Standby Current: 5 µW (typ)
- User Selectable Organization:
  512K x 16-bit (Word-Wide)
  1M x 8-bit (Byte-Wide)
  Switchable with BHE pin
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:
  JEDEC Standard Word-Wide/Byte-Wide Pinout
- Packages:
  42-pin Plastic DIP
  44-lead Plastic SOP
  44-lead Plastic TSOP (Type II)
  48-lead Plastic SOP
  44-pin Plastic QFP

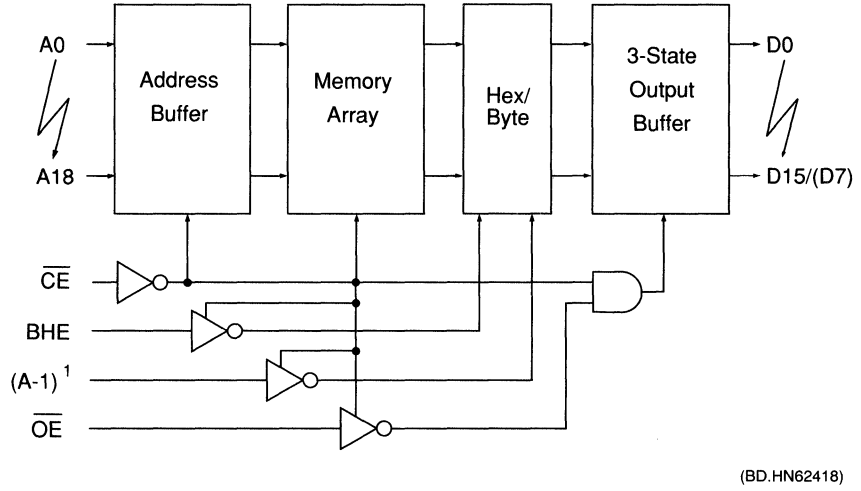
■ ORDERING INFORMATION

Type No	Access Time	Package
HN62438P	100 ns 120 ns	42-pin Plastic DIP (DP-42)
HN62438FB	100 ns 120 ns	44-lead Plastic SOP (FP-44D)
HN62438TT	100 ns 120 ns	44-lead Plastic TSOP (TTP-44D)
HN62438F	100 ns 120 ns	48-lead Plastic SOP (FP-48DA)
HN62438FP	100 ns 120 ns	44-pin Plastic QFP (FP-44A)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{18}	Address
A_{-1}	Address (Word-Wide)
D_0 - D_{15}	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
BHE	Byte Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM

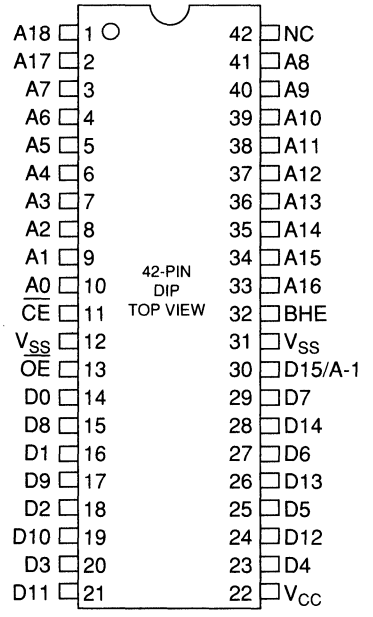


(BD.HN62418)

Notes: 1. * : A_{-1} is the Least Significant Address bit in Byte-Wide Mode.
2. BHE=V_{IH} : 16-bit (D_{15} - D_0)
BHE=V_{IL} : 8-bit (D_7 - D_0)
When BHE is low, D_{14} - D_8 are in high impedance states.

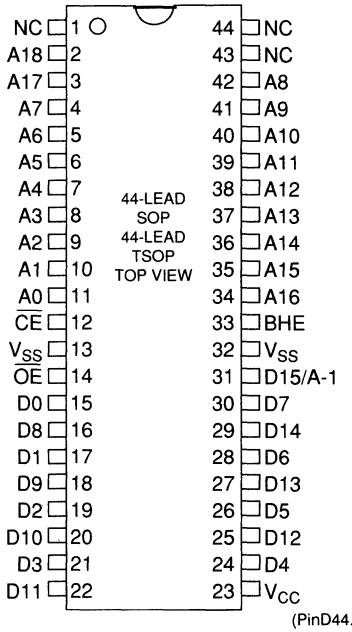
■ PIN ARRANGEMENT

HN62438P Series



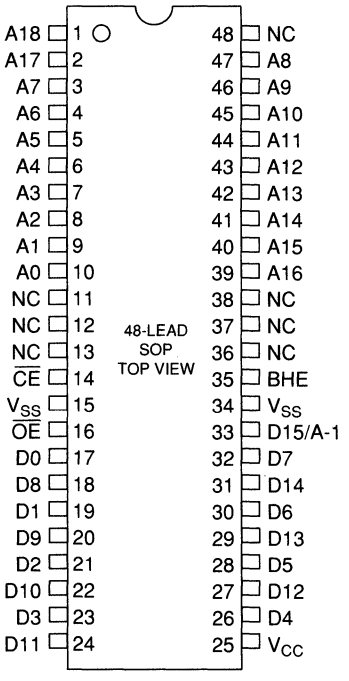
(PinD42.HN62438N)

HN62438FB Series
HN62438TT Series



(PinD44.HN62438N)

HN62438F Series

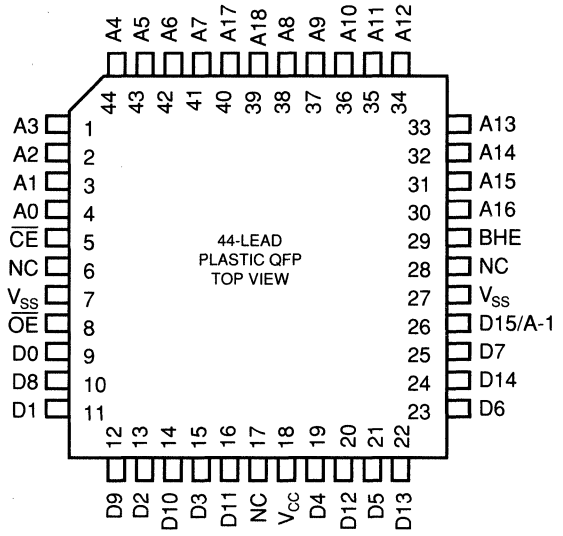


Note:
Pins 11, 12, 13, 36, 37 and 38 are connected to the inner lead frame.

(PinT248.HN62438N)

■ PIN ARRANGEMENT, contd.

HN62438FP Series



(PinQ44.HN62418)

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Operating V_{CC} Current	I_{CC}	-	80	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC}= Min.
Standby V_{CC} Current	I_{SB1}	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$-0.2V= Min.
Input Voltage	V_{IH}	2.4	V_{CC}+0.3	V	
	V_{IL}	-0.3	0.45	V	
Output Voltage	V_{OH}	2.4	-	V	I_{OH} = -205 µA
	V_{OL}	-	0.4	V	I_{OL} = 1.6 mA

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Test Conditions

- Input pulse levels: 0.8 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

Item	Symbol	HN62438-10		HN62438-12		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	100	-	120	-	ns
Address Access Time	t_{AA}	-	100	-	120	ns
$\overline{CE}$ Access Time	t_{ACE}	-	100	-	120	ns
$\overline{OE}$ Access Time	t_{OE}	-	55	-	60	ns
BHE Access Time	t_{BHE}	-	100	-	120	ns
Output Hold Time from Address Change	t_{DHA}	0	-	0	-	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	-	0	-	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	-	0	-	ns
Output Hold Time from BHE	t_{DHB}	0	-	0	-	ns
$\overline{CE}$ to Output in High Z	t_{CHZ}[1]	-	40	-	40	ns
$\overline{OE}$ to Output in High Z	t_{OHZ}[1]	-	40	-	40	ns
BHE to Output in High Z	t_{BHZ}[1]	-	40	-	40	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	5	-	5	-	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	5	-	5	-	ns
BHE to Output in Low Z	t_{BLZ}	5	-	5	-	ns

Note: 1. t_{CHZ}, t_{OHZ}, and t_{BHZ} define the time at which the output becomes an open circuit and are not referenced to output voltage levels.

3

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
All Input and Output Voltage [1]	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Notes: 1. With respect to V_{SS}.

■ CAPACITANCE

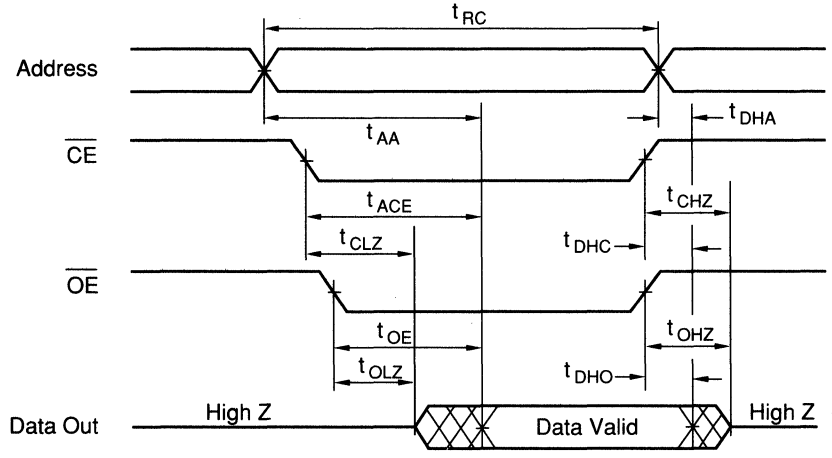
(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0 V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance [1]	C_{IN}	-	15	pF
Output Capacitance [1]	C_{OUT}	-	15	pF

Notes: 1. This parameter is sampled and not 100% tested.

■ READ TIMING WAVEFORM

Word Mode (BHE = V_{IH}) or Byte Mode (BHE = V_{IL})

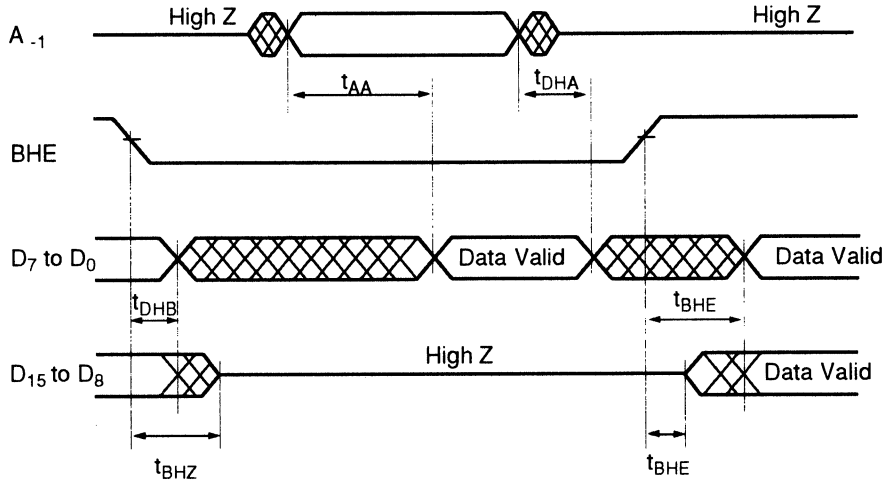


(TD.R.HN62438N)

Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

■ READ TIMING WAVEFORM

Word Mode/Byte Mode Switch



(TD.R1.HN62438N)

Note: 1. $\overline{CE}$ and $\overline{OE}$ are of select status. A_{18} to A_0 are fixed.
2. D_{15}/A_{-1} terminal is of output state when $\overline{BHE} = V_{IH}$, $\overline{CE}$ and $\overline{OE}$ are of selected state. At this time, an input signal that is of the inverse phase to the output should not be impressed.

3

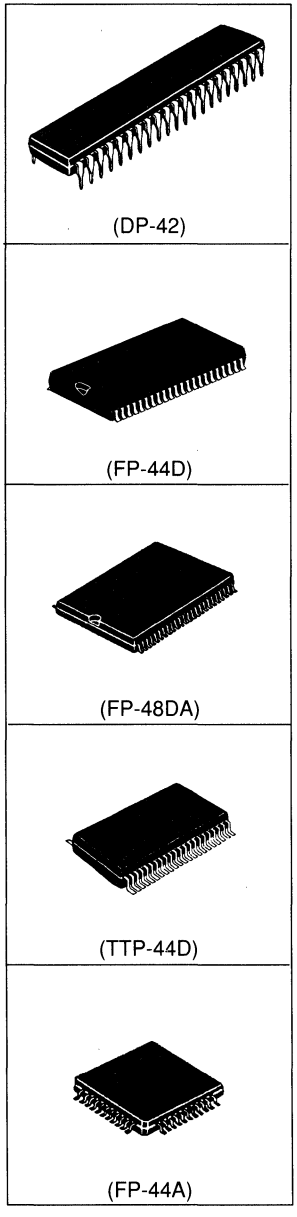
8M (512K x 16-bit) and (1M x 8-bit) Mask ROM

■ DESCRIPTION

The Hitachi HN62438N Series is an 8-Megabit CMOS Mask Programmable Read Only Memory organized either as 524,288 x 16-bit or as 1,048,576 x 8-bit.

The high density and high speed Fast Address Access provide enough capacity and high performance to be used in a system using a high speed 16-bit or 32-bit microcomputer. In addition the low power consumption of this device makes it ideal for battery powered, portable systems.

Hitachi's HN62438N is offered with JEDEC-Standard pinouts in 42-pin Plastic DIP, 44-lead Plastic SOP, 44-lead Plastic TSOP and 44-lead Plastic QFP packages. The HN62438N is also packaged in a 48-lead Plastic SOP.



■ FEATURES

- Single Power Supply
  V_{CC} = 5 V ± 10%
- Fast Access Times:
  120 ns/150 ns (max)
- Fast Address Access Times (A_0, A_1):
  60 ns/70 ns (max)
- Low Power Consumption:
  Active Current: 250 mW (typ)
  Standby Current: 5 µW (typ)
- User Selectable Organization:
  512K x 16-bit (Word-Wide)
  1M x 8-bit (Byte-Wide)
  Switchable with BHE pin
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:
  JEDEC Standard Word-Wide/Byte-Wide Pinout
- Packages:
  42-pin Plastic DIP
  44-lead Plastic SOP
  44-lead Plastic TSOP (Type II)
  48-lead Plastic SOP
  44-pin Plastic QFP

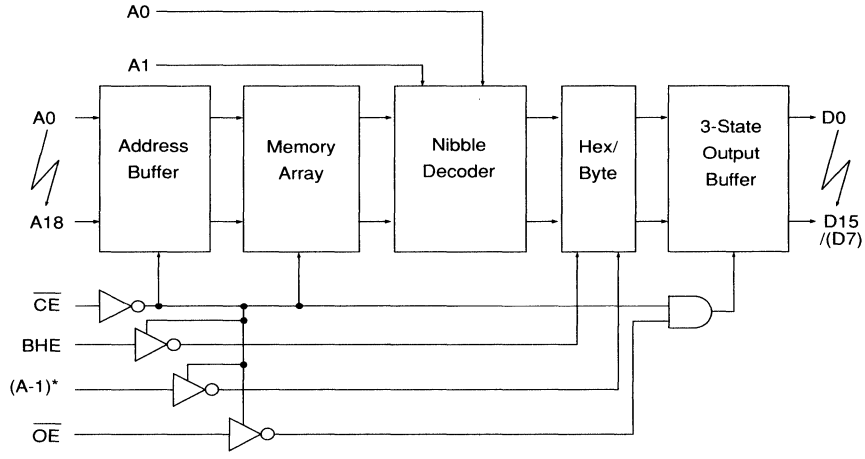
■ ORDERING INFORMATION

Type No	Access Time	Package
HN62438NP	120 ns 150 ns	42-pin Plastic DIP (DP-42)
HN62438NFB	120 ns 150 ns	44-lead Plastic SOP (FP-44D)
HN62438NTT	120 ns 150 ns	44-lead Plastic TSOP (TTP-44D)
HN62438NF	120 ns 150 ns	48-lead Plastic SOP (FP-48DA)
HN62438NFP	120 ns 150 ns	44-pin Plastic QFP (FP-44A)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{18}	Address
A_{-1}	Address (Word-Wide)
D_0 - D_{15}	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
BHE	Byte Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM

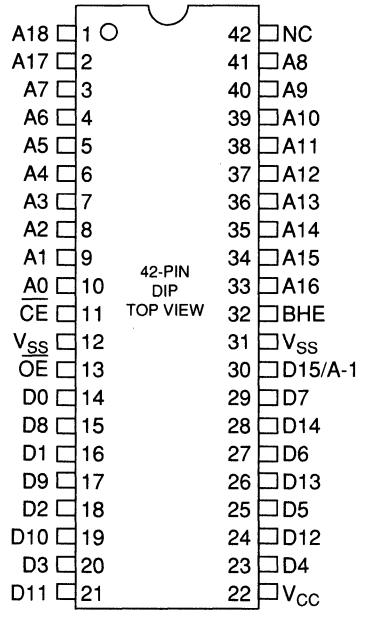


(BD.HN62438N)

Notes: 1. * : A_{-1} is the Least Significant Address bit in Byte-Wide Mode.
2. BHE=V_{IH} : 16-bit (D_{15} - D_0)
BHE=V_{IL} : 8-bit (D_7 - D_0)
When BHE is low, D_{14} - D_8 are in high impedance states.

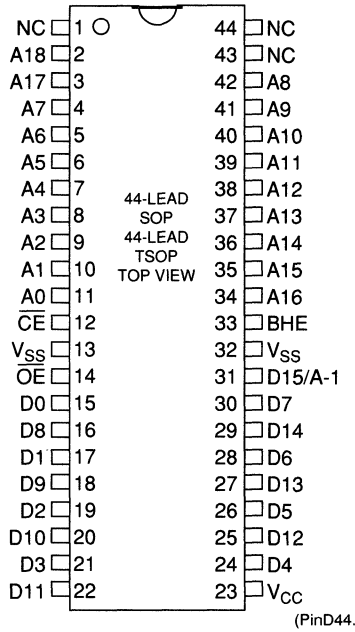
■ PIN ARRANGEMENT

HN62438NP Series



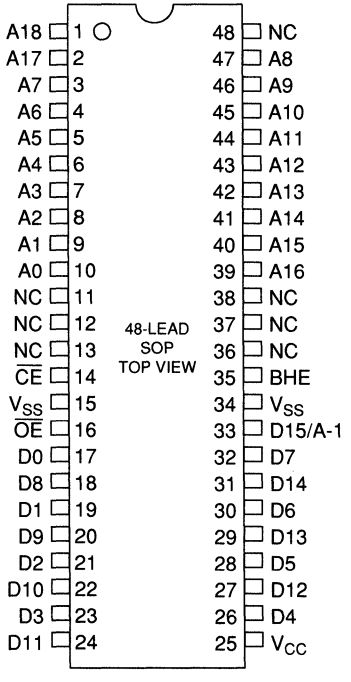
(PinD42.HN62438N)

HN62438NFB Series
HN62438NTT Series



(PinD44.HN62438N)

HN62438NF Series

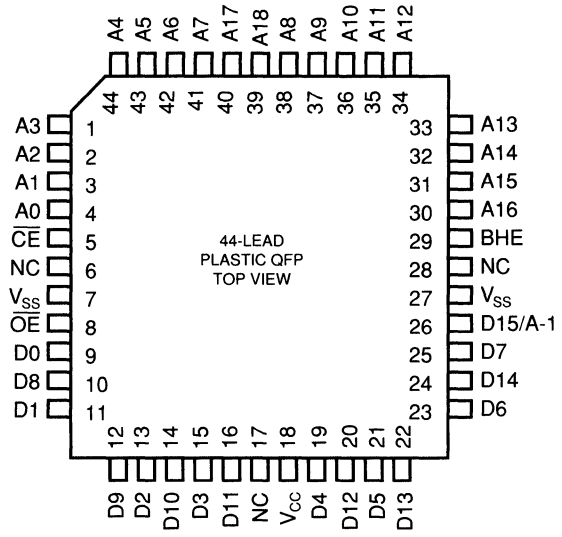


Note:
Pins 11, 12, 13, 36, 37 and 38 are connected to the inner lead frame.

(PinT248.HN62438N)

■ PIN ARRANGEMENT, contd.

HN62438NFP Series



(PinQ44.HN62418)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
All Input and Output Voltage [1]	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Notes: 1. With respect to V_{SS}.

■ CAPACITANCE

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0 V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance [1]	C_{IN}	-	15	pF
Output Capacitance [1]	C_{OUT}	-	15	pF

Notes: 1. This parameter is sampled and not 100% tested.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Test Conditions

- Input pulse levels: 0.8 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

Item	Symbol	HN62438N-12		HN62438N-15		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	120	-	120	-	ns
Fast Address Read Cycle Time	t_{BC}	60	-	70	-	ns
Address Access Time	t_{AA}	-	120	-	150	ns
Fast (Address Access) Time	t_{BA}	-	60	-	70	ns
$\overline{CE}$ Access Time	t_{ACE}	-	120	-	150	ns
$\overline{OE}$ Access Time	t_{OE}	-	60	-	70	ns
$\overline{BHE}$ Access Time	t_{BHE}	-	120	-	150	ns
Output Hold Time from Address Change	t_{DHA}	0	-	0	-	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	-	0	-	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	-	0	-	ns
Output Hold Time from $\overline{BHE}$	t_{DHB}	0	-	0	-	ns
$\overline{CE}$ to Output in High Z	t_{CHZ}[1]	-	60	-	70	ns
$\overline{OE}$ to Output in High Z	t_{OHZ}[1]	-	60	-	70	ns
$\overline{BHE}$ to Output in High Z	t_{BHZ}[1]	-	60	-	70	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	10	-	10	-	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	-	10	-	ns
$\overline{BHE}$ to Output in Low Z	t_{BLZ}	10	-	10	-	ns

Note: 1. t_{CHZ}, t_{OHZ}, and t_{BHZ} define the time at which the output becomes an open circuit and are not referenced to output voltage levels.

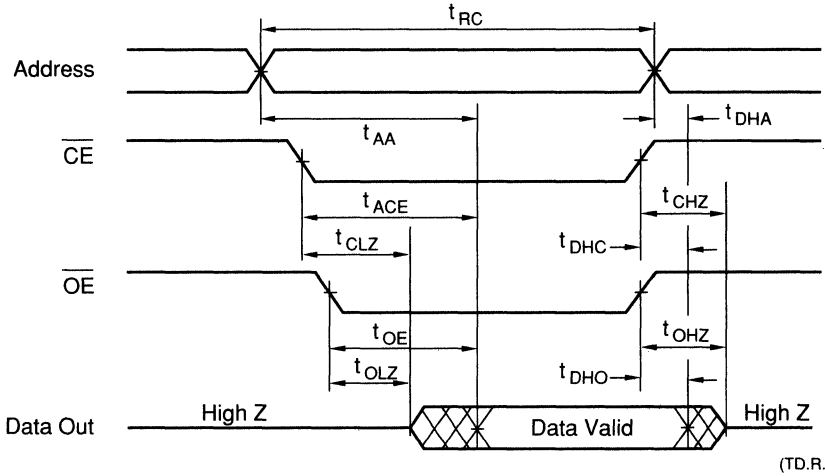
■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Operating V_{CC} Current	I_{CC}	-	100	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC}= Min.
Standby V_{CC} Current	I_{SB1}	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$-0.2V= Min.
	I_{SB2}	-	3	mA	V_{CC} = 5.5 V, $\overline{CE} \geq$ 2.4V
Input Voltage	V_{IH}	2.4	V_{CC}+0.3	V	
	V_{IL}	-0.3	0.45	V	
Output Voltage	V_{OH}	2.4	-	V	I_{OH} = -205 µA
	V_{OL}	-	0.4	V	I_{OL} = 1.6 mA

■ READ TIMING WAVEFORM

Word Mode (BHE = V_{IH}) or Byte Mode (BHE = V_{IL})



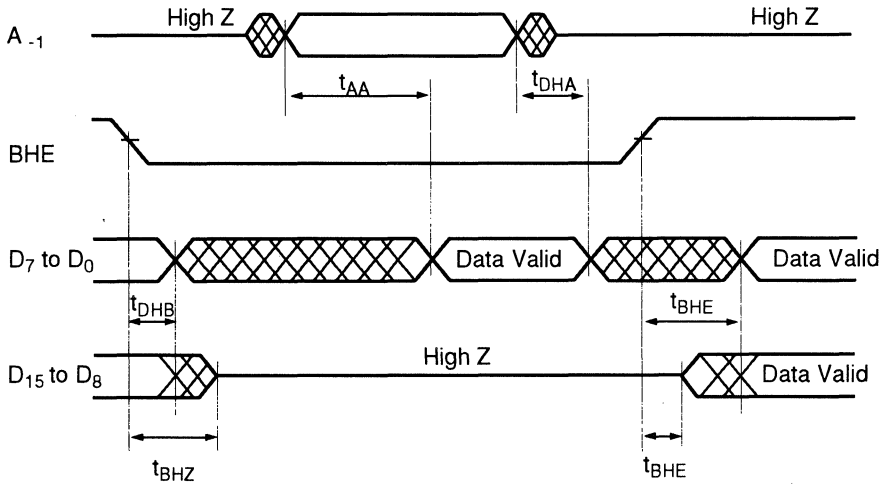
(TD.R.HN62438N)

Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

3

■ READ TIMING WAVEFORM

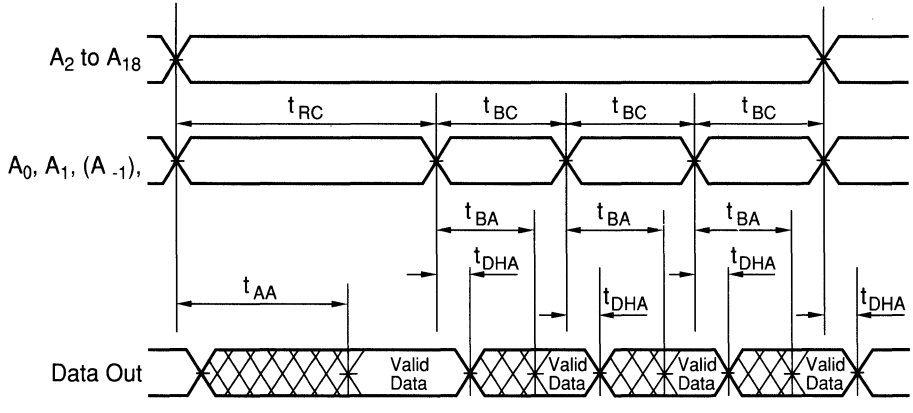
Word Mode/Byte Mode Switch



(TD.R1.HN62438N)

Note: 1. $\overline{CE}$ and $\overline{OE}$ are of select status. A_{18} to A_0 are fixed.
2. D_{15}/A_{-1} terminal is of output state when $\overline{BHE} = V_{IH}$, $\overline{CE}$ and $\overline{OE}$ are of selected state. At this time, an input signal that is of the inverse phase to the output should not be impressed.

Fast Address Access



(TD.RN.HN62438N)

Note: $\overline{CE}$ and $\overline{OE}$ are enabled.

HN62318B Series
HN62328B Series

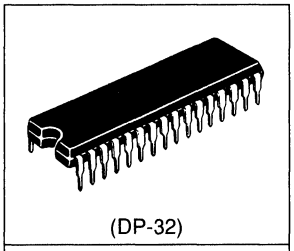
8M (1M x 8-bit) Mask ROM

■ DESCRIPTION

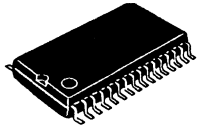
The Hitachi HN62318B/HN62328B Series is an 8-Megabit CMOS Mask Programmable Read Only Memory organized as 1,048,576 x 8-bit.

The low power consumption of this device makes it ideal for battery powered, portable systems. In addition , the high density and high speed provide enough capacity and high performance to be used as a character generator in laser printers.

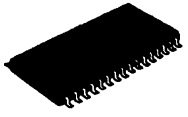
Hitachi's HN62318B/HN62328B is offered with JEDEC-standard pinouts in 32-pin Plastic DIP and 32-lead Plastic SOP and TSOP packages.



(DP-32)



(FP-32D)



(TTP-32D)

■ FEATURES

- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Fast Access Time:
  150 ns/200 ns (Max)
- Low Power Consumption:
  Active Current: 100 mW (typ)
  Standby Current: 5 µW (typ)
- Byte-Wide Data Organization
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Packages:
  32-pin Plastic DIP
  32-lead Plastic SOP
  32-lead Plastic TSOP (Type II)

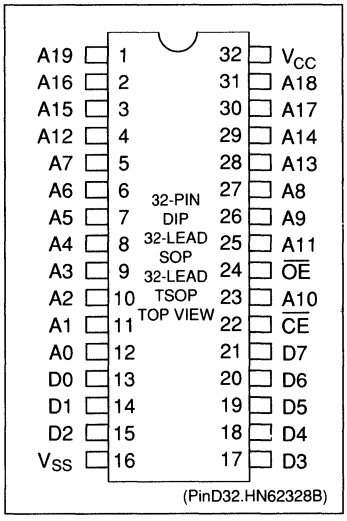
■ ORDERING INFORMATION

Type No.	Access Time	Package
HN62318BP	150 ns/200 ns	32-pin Plastic DIP
HN62328BP	150 ns/200 ns	(DP-32)
HN62318BF	150 ns/200 ns	32-lead Plastic SOP
HN62328BF	150 ns/200 ns	(FP-32D)
HN62318BTT	150 ns/200 ns	32-lead Plastic TSOP
HN62328BTT	150 ns/200 ns	(TTP-32D)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{19}	Address
D_0 - D_7	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

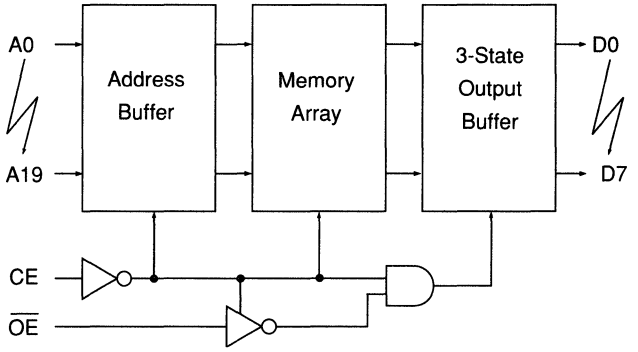
■ PIN ARRANGEMENT



(PinD32.HN62328B)

3

■ BLOCK DIAGRAM



(BD.HN62328B)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
Terminal Voltage [1]	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Notes: 1. With respect to V_{SS}.

■ CAPACITANCE

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0 V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance [1]	C_{IN}	-	15	pF
Output Capacitance [1]	C_{OUT}	-	15	pF

Notes: 1. This parameter is sampled and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Operating V_{CC} Current	I_{CC}	-	50	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = Min.
Standby V_{CC} Current	I_{SB}	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$-0.2V
Input Voltage	V_{IH}	2.2	V_{CC}+0.3	V	
	V_{IL}	-0.3	0.8	V	
Output Voltage	V_{OH}	2.4	-	V	I_{OH} = -205 µA
	V_{OL}	-	0.4	V	I_{OL} = 1.6 mA

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

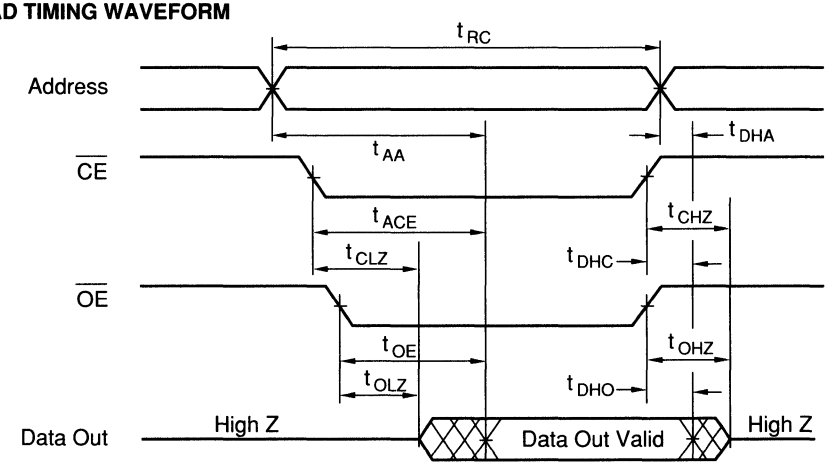
Test Conditions

- Input pulse levels: 0.8 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

Item	Symbol	HN62318B		HN62328B		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	150	-	200	-	ns
Address Access Time	t_{AA}	-	150	-	200	ns
$\overline{CE}$ Access Time	t_{ACE}	-	150	-	200	ns
$\overline{OE}$ Access Time	t_{OE}	-	70	-	100	ns
Output Hold Time from Address Change	t_{DHA}	0	-	0	-	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	-	0	-	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	-	0	-	ns
$\overline{CE}$ to Output in High Z	t_{CHZ} [1]	-	70	-	70	ns
$\overline{OE}$ to Output in High Z	t_{OHZ} [1]	-	70	-	70	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	10	-	10	-	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	-	10	-	ns

Note: 1. t_{CHZ}, and t_{OHZ} define the time at which the output becomes an open circuit and are not referenced to output voltage levels.

■ READ TIMING WAVEFORM



(TD.R.HN62328B)

Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

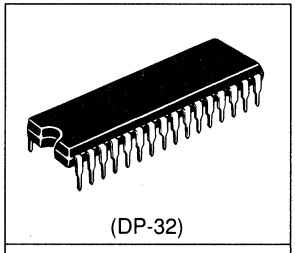
8M (1M x 8-bit) Mask ROM

■ DESCRIPTION

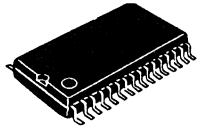
The Hitachi HN623W328B Series is an 8-Megabit CMOS Mask Programmable Read Only Memory organized as 1,048,576 x 8-bit.

The low voltage and low power consumption of this device makes it ideal for battery powered, portable systems. In addition , the high density and high speed provide enough capacity and high performance to be used as a character generator in laser printers.

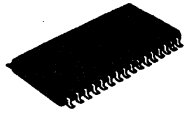
Hitachi's HN62W328B is offered with JEDEC-standard pinouts in 32-pin Plastic DIP and 32-lead Plastic SOP and TSOP packages.



(DP-32)



(FP-32D)



(TTP-32D)

■ FEATURES

- Single Power Supply:
  V_{CC} = 3.0 to 5.5V
- Access Time:
  300 ns (Max)
- Low Power Consumption:
  Active Current: 100 mW (typ)
  Standby Current: 5 µW (typ)
- Byte-Wide Data Organization
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Packages:
  32-pin Plastic DIP
  32-lead Plastic SOP
  32-lead Plastic TSOP (Type II)

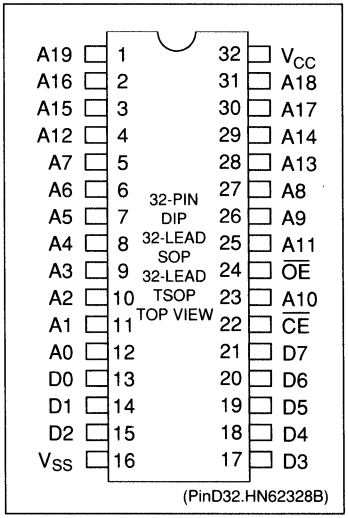
■ ORDERING INFORMATION

Type No.	Access Time	Package
HN62W328BP	300 ns	32-pin Plastic DIP (DP-32)
HN62W328BF	300 ns	32-lead Plastic SOP (FP-32D)
HN62W328BTT	300 ns	32-lead Plastic TSOP (TTP-32D)

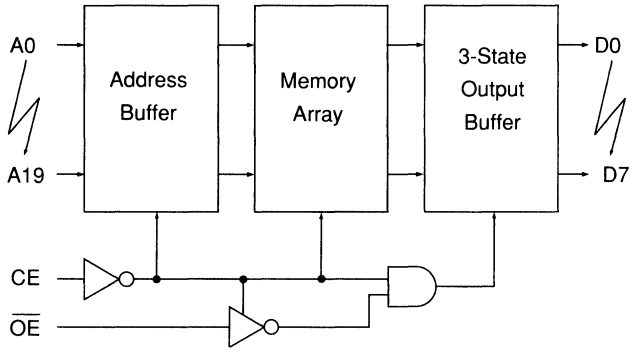
■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{19}	Address
D_0 - D_7	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ PIN ARRANGEMENT



■ BLOCK DIAGRAM



(BD.HN62328B)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
Terminal Voltage [1]	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Notes: 1. With respect to V_{SS}.

■ CAPACITANCE

(V_{CC} = 3.0 to 5.5V, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0 V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance [1]	C_{IN}	-	15	pF
Output Capacitance [1]	C_{OUT}	-	15	pF

Notes: 1. This parameter is sampled and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 3.0 to 5.5V, V_{SS} = 0 V, T_a = 0 to 70°C)

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Operating V_{CC} Current	I_{CC}	-	25	mA	V_{CC} = 3.5 V, I_{DOUT} = 0 mA, t_{RC} = Min.
Standby V_{CC} Current	I_{SB}	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$-0.2V
Input Voltage	V_{IH}	2.2	V_{CC}+0.3	V	
	V_{IL}	-0.3	0.8	V	
Output Voltage	V_{OH}	2.4	-	V	I_{OH} = -205 µA
	V_{OL}	-	0.4	V	I_{OL} = 1.6 mA

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 3.0 to 5.5V, V_{SS} = 0 V, T_a = 0 to 70°C)

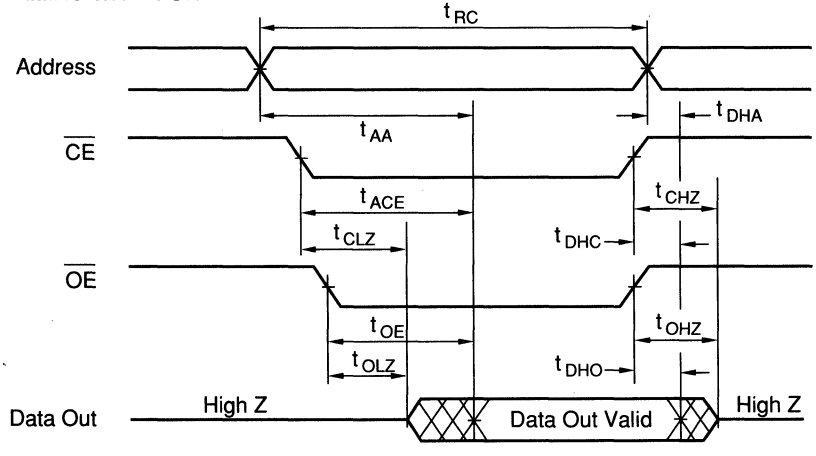
Test Conditions

- Input pulse levels: 0.8 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

Item	Symbol	HN62W328B Min.	HN62W328B Max.	Unit
Read Cycle Time	t_{RC}	300	-	ns
Address Access Time	t_{AA}	-	300	ns
$\overline{CE}$ Access Time	t_{ACE}	-	300	ns
$\overline{OE}$ Access Time	t_{OE}	-	150	ns
Output Hold Time from Address Change	t_{DHA}	0	-	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	-	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	-	ns
$\overline{CE}$ to Output in High Z	t_{CHZ} [1]	-	100	ns
$\overline{OE}$ to Output in High Z	t_{OHZ} [1]	-	100	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	10	-	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	-	ns

Note: 1. t_{CHZ}, and t_{OHZ} define the time at which the output becomes an open circuit and are not referenced to output voltage levels.

■ READ TIMING WAVEFORM



(TD.R.HN62328B)

Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

HN62338B Series — Preliminary

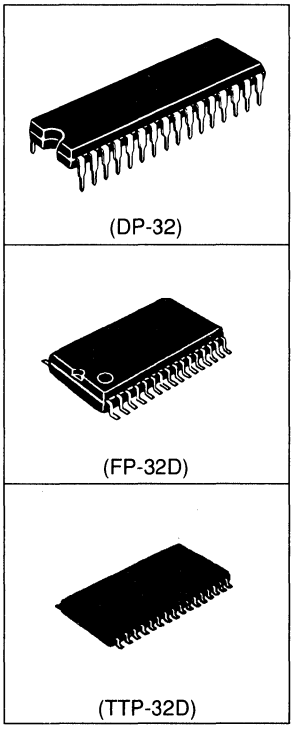
8M (1M x 8-bit) Mask ROM

■ DESCRIPTION

The Hitachi HN62338B Series is an 8-Megabit CMOS Mask Programmable Read Only Memory organized as 1,048,576 x 8-bit.

The low power consumption of this device makes it ideal for battery powered, portable systems. In addition , the high density and high speed provide enough capacity and high performance to be used as a character generator in laser printers.

Hitachi's HN62338B is packaged in 32-pin Plastic DIP and 32-lead Plastic SOP and TSOP packages.



■ FEATURES

- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Fast Access Time:
  100 ns/120 ns (Max)
- Low Power Consumption:
  Active Current: 250 mW (typ)
  Standby Current: 5 µW (typ)
- Byte-Wide Data Organization
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Packages:
  32-pin Plastic DIP
  32-lead Plastic SOP
  32-lead Plastic TSOP (Type II)

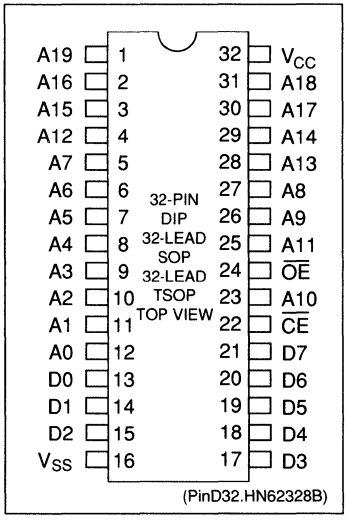
■ ORDERING INFORMATION

Type No.	Access Time	Package
HN62338BP	100 ns 120 ns	32-pin Plastic DIP (DP-32)
HN62338BF	100 ns 120 ns	32-lead Plastic SOP (FP-32D)
HN62338BTT	100 ns 120 ns	32-lead Plastic TSOP (TTP-32D)

■ PIN DESCRIPTION

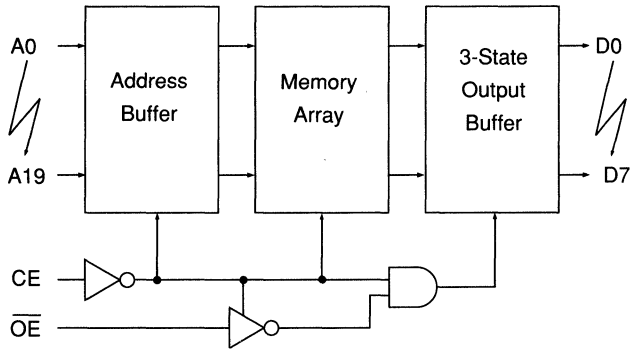
Pin Name	Function
A_0 - A_{19}	Address
D_0 - D_7	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ PIN ARRANGEMENT



3

■ BLOCK DIAGRAM



(BD.HN62328B)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
Terminal Voltage [1]	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Notes: 1. With respect to V_{SS}.

■ CAPACITANCE

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0 V, f = 1MHz)

Item	Symbol	Min.	Max.	Unit
Input Capacitance [1]	C_{IN}	-	15	pF
Output Capacitance [1]	C_{OUT}	-	15	pF

Notes: 1. This parameter is sampled and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Operating V_{CC} Current	I_{CC}	-	80	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = Min.
Standby V_{CC} Current	I_{SB}	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$-0.2V
Input Voltage	V_{IH}	2.2	V_{CC}+0.3	V	
	V_{IL}	-0.3	0.8	V	
Output Voltage	V_{OH}	2.4	-	V	I_{OH} = -205 µA
	V_{OL}	-	0.4	V	I_{OL} = 1.6 mA

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

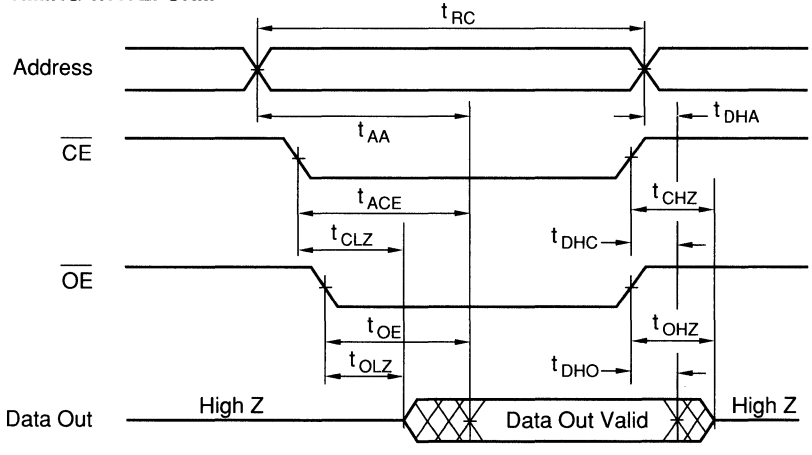
Test Conditions

- Input pulse levels: 0.8 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

Item	Symbol	HN62338B-10		HN62338B-12		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	100	-	120	-	ns
Address Access Time	t_{AA}	-	100	-	120	ns
$\overline{CE}$ Access Time	t_{ACE}	-	100	-	120	ns
$\overline{OE}$ Access Time	t_{OE}	-	55	-	60	ns
Output Hold Time from Address Change	t_{DHA}	0	-	0	-	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	-	0	-	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	-	0	-	ns
$\overline{CE}$ to Output in High Z	t_{CHZ} [1]	-	40	-	40	ns
$\overline{OE}$ to Output in High Z	t_{OHZ} [1]	-	40	-	40	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	5	-	5	-	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	5	-	5	-	ns

Note: 1. t_{CHZ}, and t_{OHZ} define the time at which the output becomes an open circuit and are not referenced to output voltage levels.

■ READ TIMING WAVEFORM



(TD.R.HN62328B)

Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

HN624116 Series

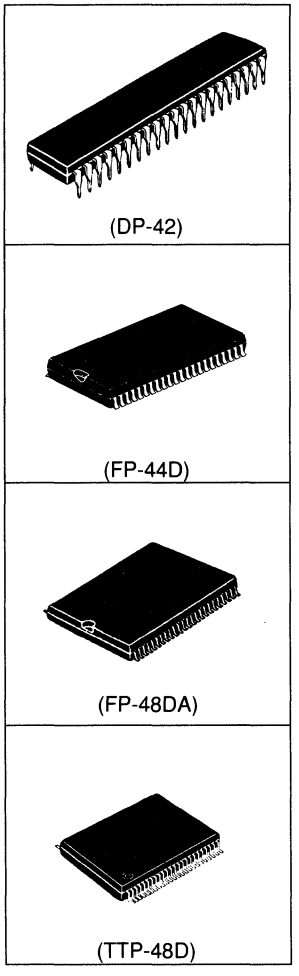
16M (1M x 16-bit) and (2M x 8-bit) Mask ROM

■ DESCRIPTION

The Hitachi HN624116 is a 16-Megabit CMOS Mask Programmable Read Only Memory organized as 1,048,576 x 16-bit and 2,097,152 x 8-bit.

The low power consumption of this device makes it ideal for battery powered, portable systems. In addition , the high density and high speed provide enough capacity and high performance to be used as a character generator in laser printers.

Hitachi's HN624116 is offered with JEDEC-Standard pinouts in 42-pin Plastic DIP, 44-lead Plastic SOP and 48-lead Plastic TSOP packages. The HN624116 is also packaged in a 48-lead Plastic SOP.



■ FEATURES

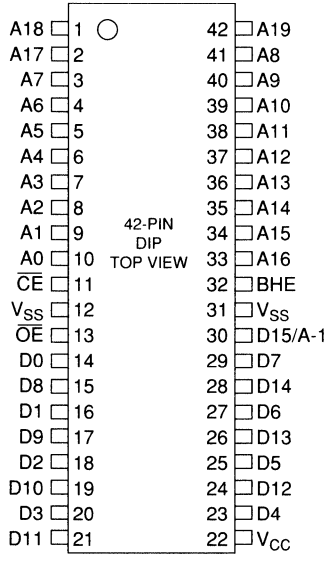
- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Fast Access Times:
  150 ns/200 ns (max)
- Low Power Consumption:
  Active Current: 275 mW (typ)
  Standby Current: 5 µW (typ)
- User Selectable Organization:
  1M x 16-bit (Word-Wide)
  2M x 8-bit (Byte-Wide)
  Switchable with BHE pin
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:
  JEDEC Standard Word-Wide/Byte-Wide Pinout
- Packages:
  42-pin Plastic DIP
  44-lead Plastic SOP
  48-lead Plastic SOP
  48-lead Plastic TSOP (Type II)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN624116P	150 ns 200 ns	42-pin Plastic DIP (DP-42)
HN624116FB	150 ns 200 ns	44-lead Plastic SOP (FP-44D)
HN624116F	150 ns 200 ns	48-lead Plastic SOP (FP-48DA)
HN624116TA	150 ns 200 ns	48-lead Plastic TSOP (TTP-48D)

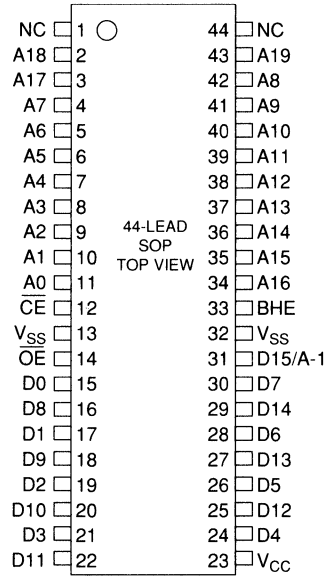
■ PIN ARRANGEMENT

HN624116P Series



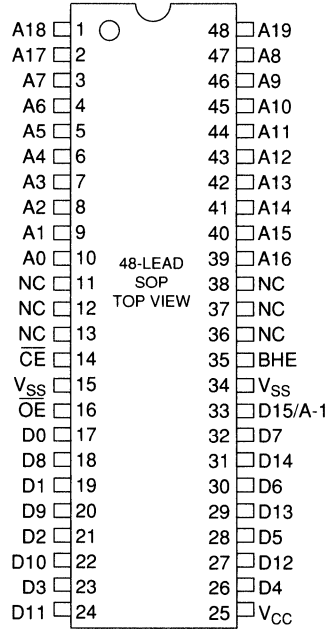
(PinD42.HN624116)

HN624116FB Series



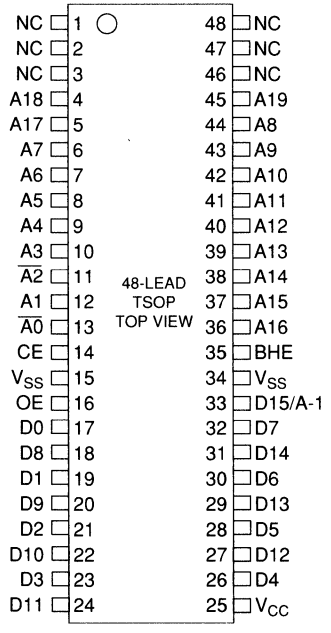
(PinT244.HN624116)

HN624116F Series



(PinT248.HN624116)

HN624116TA Series



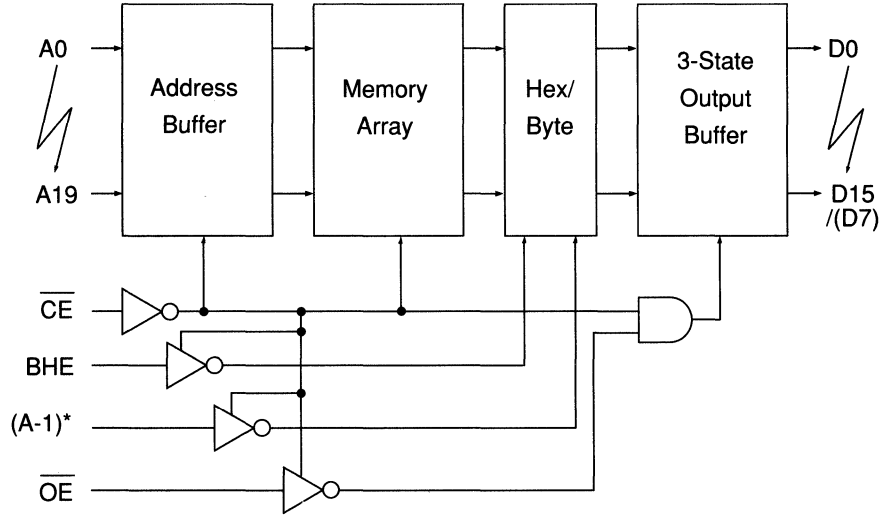
(PinT248.HN624116)

3

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{19}	Address
A_{-1}	Address (Word-Wide)
D_0 - D_{15}	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
BHE	Byte Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



(BD.HN624116)

Notes: 1. * : A_{-1} is the Least Significant Address bit in Byte-Wide Mode.
2. BHE=V_{IH} : 16-bit (D_{15} - D_0)
BHE=V_{IL} : 8-bit (D_7 - D_0)
When BHE is low, D_{14} - D_8 are in high impedance states.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
All Input and Output Voltage [1]	V_{IN}, V_{OUT}	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Notes: 1. Relative to V_{SS}.

■ CAPACITANCE

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0 V, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance [1]	C_{IN}	-	-	15	pF	V_{IN} = 0V
Output Capacitance [1]	C_{OUT}	-	-	15	pF	V_{OUT} = 0V

Notes: 1. This parameter is sampledand not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	10	µA	V_{IN} = 0 V to V_{CC}
Output Leakage Current	I_{LO}	-	-	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 V to V_{CC}
Operating V_{CC} Current	I_{CC}	-	-	75	mA	V_{CC} = 5.5 V, I_{DOUT}=0 mA, t_{RC}=150ns
		-	-	65	mA	V_{CC} = 5.5 V, I_{DOUT}=0 mA, t_{RC}=200ns
Standby V_{CC} Current	I_{SB}	-	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$-0.2V
Input Voltage	V_{IH}	2.2	-	V_{CC}+0.3	V	
	V_{IL}	-0.3	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -205 µA
	V_{OL}	-	-	0.4	V	I_{OL} = 1.6 mA

3

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Test Conditions

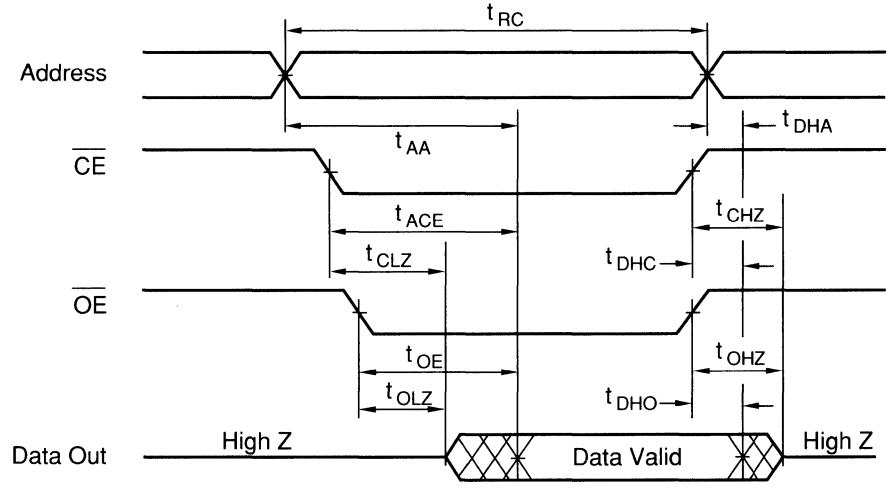
- Input pulse levels: 0.8 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Reference level for measuring timing: 1.5 V

Item	Symbol	HN624116-15		HN624116-20		Test Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	150	-	200		ns
Address Access Time	t_{AA}	-	150	-	200	ns
Chip Enable Access Time	t_{CE}	-	150	-	200	ns
Output Enable Access Time	t_{OE}	-	70	-	100	ns
BHE Access Time	t_{BHE}	-	150	-	200	ns
Output Hold Time from Address Change	t_{DHA}	0	-	0	-	ns
Output Hold Time from Chip Enable	t_{DHC}	0	-	0	-	ns
Output Hold Time from Output Enable	t_{DHO}	0	-	0	-	ns
Output Hold Time from BHE	t_{DHB}	0	-	0	-	ns
Chip Enable to Output in High-Z [1]	t_{CHZ}	-	70	-	70	ns
Output Enable to Output in High-Z [1]	t_{OHZ}	-	70	-	70	ns
BHE to Output in High-Z [1]	t_{BHZ}	-	70	-	70	ns
Chip Enable to Output in Low-Z	t_{CLZ}	10	-	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}	10	-	10	-	ns
BHE to Output in Low-Z	t_{BLZ}	10	-	10	-	ns

Note: 1. t_{CHZ}, t_{OHZ}, t_{BHZ} are defined as the time at which the output becomes an open circuit and are not referenced to output voltage levels.

■ READ TIMING WAVEFORM

Word Mode (BHE = V_{IH}) or Byte Mode (BHE = V_{IL})

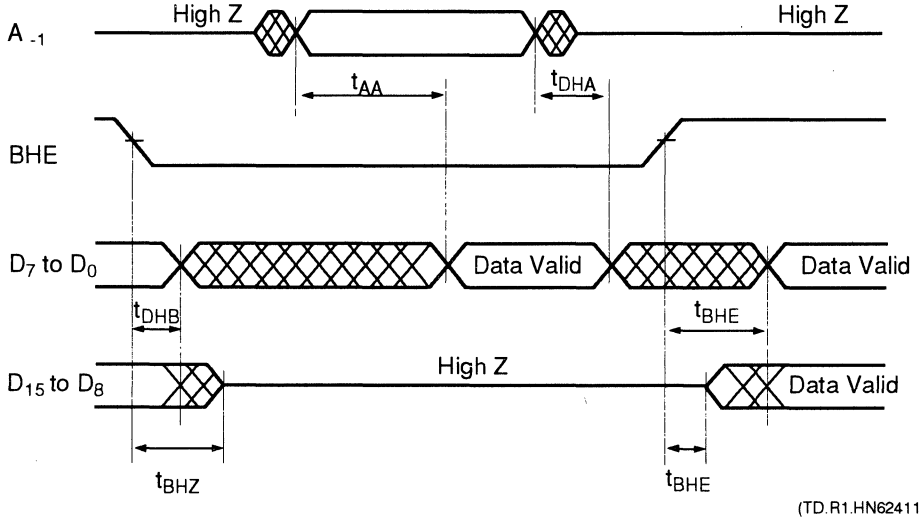


Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

(TD.R.HN624116)

3

Word Mode/Byte Mode Switch



(TD.R1.HN624116)

Note: 1. If $\overline{CE}$ and $\overline{OE}$ are enabled, A_{19} to A_0 are valid.
2. D_{15}/A_{-1} pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enabled. Therefore, the input signals of opposite phase to the output must not be applied to them.

HN62W4116 Series

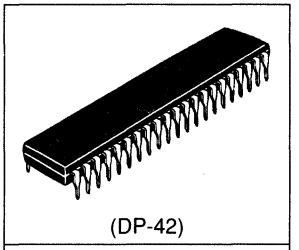
16M (1M x16-bit) and (2M x 8-bit) Mask ROM

■ DESCRIPTION

The Hitachi HN62W4116 is a 16-Megabit CMOS Mask Programmable Read Only Memory organized as 1,048,576 x 16-bit and 2,097,152 x 8-bit.

The HN62W4116 is capable of operating down to 3.0V, which makes it ideal for battery powered, portable systems. In addition, the high density provides enough capacity to be used as a character generator in laser printers.

Hitachi's HN62W4116 is offered with JEDEC-Standard pinouts in 42-pin Plastic DIP, 44-lead Plastic SOP and 48-lead Plastic TSOP packages. The HN62W4116 is also packaged in a 48-lead Plastic SOP.



(DP-42)

(FP-44D)

(FP-48DA)

(TTP-48D)

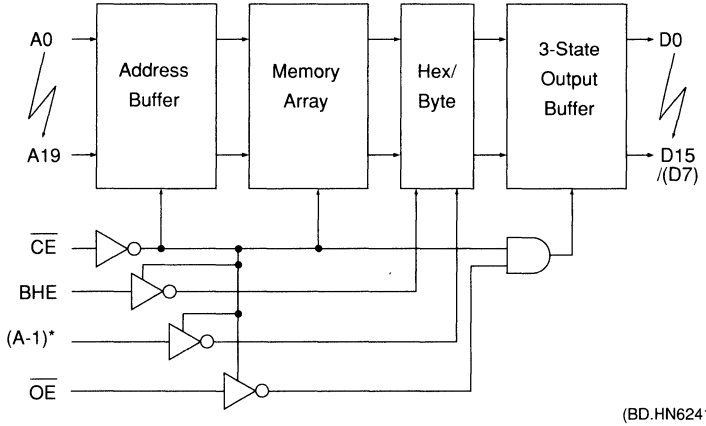
■ FEATURES

- Single Power Supply:
  V_{CC} = 3.0V to 5.5V
- Fast Access Times:
  300 ns (max)
- Low Power Consumption:
  Active Current: 275 mW (typ)
  Standby Current: 5 μW (typ)
- User Selectable Organization:
  1M x 16-bit (Word-Wide)
  2M x 8-bit (Byte-Wide)
  Switchable with BHE pin
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:
  JEDEC Standard Word-Wide/Byte-Wide Pinout
- Packages:
  42-pin Plastic DIP
  44-lead Plastic SOP
  48-lead Plastic SOP
  48-lead Plastic TSOP (Type II)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN62W4116P	300 ns	42-pin Plastic DIP (DP-42)
HN62W4116FB	300 ns	44-lead Plastic SOP (FP-44D)
HN62W4116F	300 ns	48-lead Plastic SOP (FP-48DA)
HN62W4116TA	300 ns	48-lead Plastic TSOP (TTP-48D)

■ BLOCK DIAGRAM



(BD.HN624116L)

Notes: 1. * : A_{-1} is the Least Significant Address bit in Byte-Wide Mode.
2. BHE=V_{IH} : 16-bit (D_{15} - D_0)
BHE=V_{IL} : 8-bit (D_7 - D_0)
When BHE is low, D_{14} - D_8 are in high impedance states.

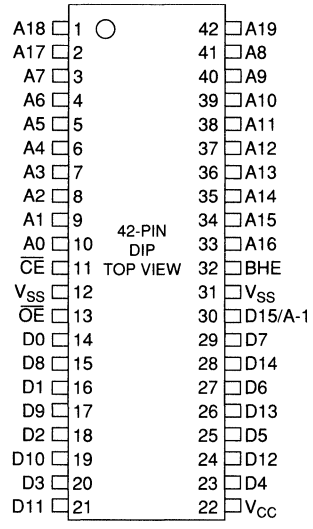
■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{19}	Address
A_{-1}	Address (Word-Wide)
D_0 - D_{15}	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
BHE	Byte Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

3

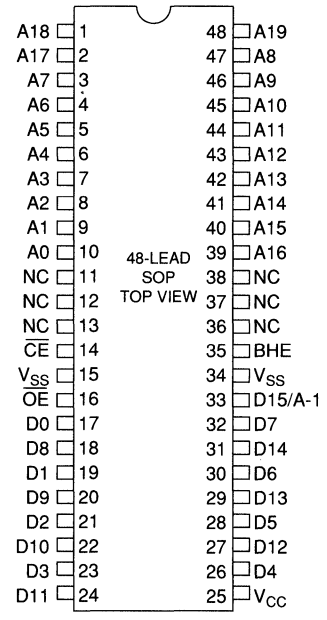
■ PIN ARRANGEMENT

HN62W4116P



(PinD42.HN624116L)

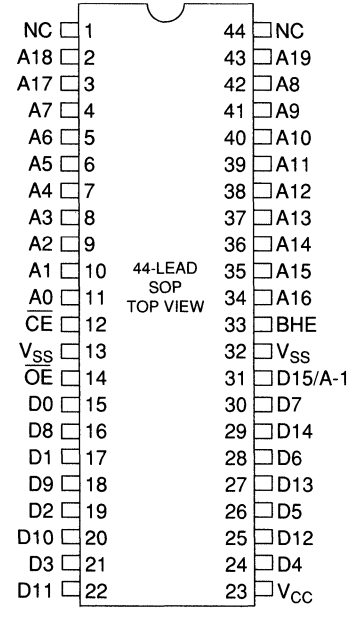
HN62W4116F



12-13 pin and 36-37 pin are connected to inner lead frame.

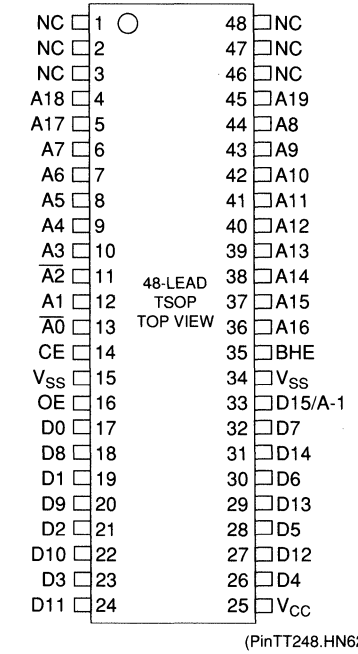
(PinT248.HN624116L)

HN62W4116FB



(PinT244.HN624116L)

HN62W4116TA



(PinTT248.HN624116)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
All Input and Output Voltage [1]	V_T	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Note: 1. Relative to V_{SS}.

■ CAPACITANCE

(V_{CC} = 3.0 to 5.5V, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0V, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit
Input Capacitance [1]	C_{IN}	-	-	15	pF
Output Capacitance [1]	C_{OUT}	-	-	15	pF

Note: 1. This parameter is sampled and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 3.0 to 5.5V, V_{SS} = 0V, T_a = 0 to +70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	10	µA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-	-	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Operating V_{CC} Current	I_{CC}	-	-	65	mA	V_{CC} = 5.5 V, ID_{OUT} = 0 mA, t_{RC}=min.
				35	mA	V_{CC} = 3.5 V, ID_{OUT} = 0 mA, t_{RC}=Min.
Standby V_{CC} Current	I_{SB}	-	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{cc}$ -0.2V
Input Voltage	V_{IH}	2.2	-	V_{CC}+0.3	V	
	V_{IL}	-0.3	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -205 µA
	V_{OL}	-	-	0.4	V	I_{OL} = 1.6 mA

3

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 3.0 to 5.5V, V_{SS} = 0V, T_a = 0 to +70°C)

Test Conditions

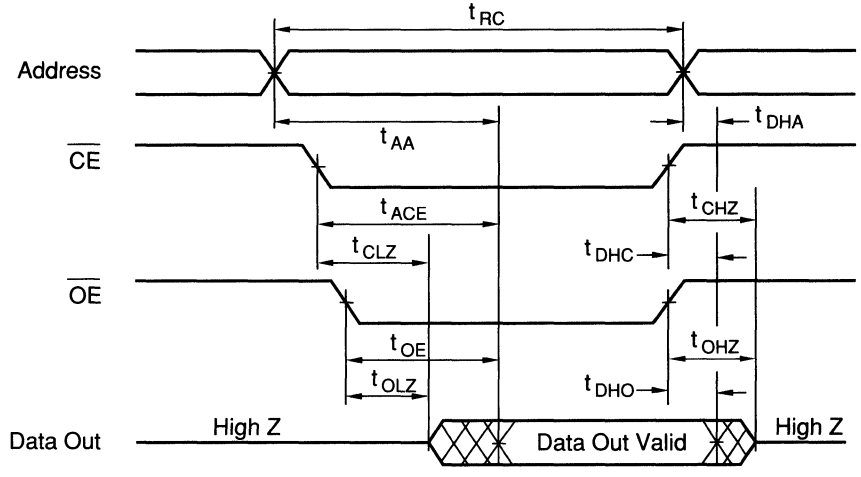
- Input pulse levels: 0.8 / 2.4V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Input/Output Timing Reference level: 1.5 V

Item	Symbol	HN62W4116 Min.	HN62W4116 Max.	Test Unit
Read Cycle Time	t_{RC}	300		ns
Address Access Time	t_{AA}	-	300	ns
Chip Enable Access Time	t_{ACE}	-	300	ns
Output Enable Access Time	t_{OE}	-	150	ns
BHE Access Time	t_{BHE}	-	300	ns
Output Hold Time from Address Change	t_{DHA}	0	-	ns
Output Hold Time from Chip Enable	t_{DHC}	0	-	ns
Output Hold Time from Output Enable	t_{DHO}	0	-	ns
Output Hold Time from BHE	t_{DHB}	0	-	ns
Chip Enable to Output in High-Z [1]	t_{CHZ}	-	100	ns
Output Enable to Output in High-Z [1]	t_{OHZ}	-	100	ns
BHE to Output in High-Z [1]	t_{BHZ}	-	100	ns
Chip Enable to Output in Low-Z	t_{CLZ}	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}	10	-	ns
BHE to Output in Low-Z	t_{BLZ}	10	-	ns

Note: 1. t_{CHZ}, t_{OHZ}, and t_{BHZ} are defined as the time at which the output becomes an open circuit and are not referenced to output voltage levels.

■ READ TIMING WAVEFORM

Word Mode (BHE = V_{IH}) or Byte Mode (BHE = V_{IL})

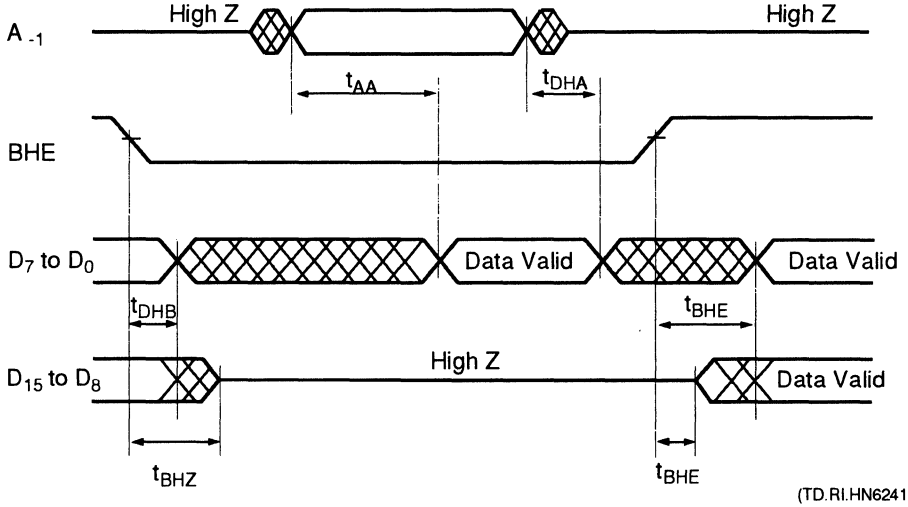


(TD.R.HN624116L)

Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

3

Word Mode/ Byte Mode Switch



(TD.RI.HN624116L)

Note: 1. If $\overline{CE}$ and $\overline{OE}$ are enabled, A_{19} to A_0 are valid.
2. D_{15}/A_{-1} pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enabled. Therefore, the input signals of opposite phase to the output must not be applied to them.

HN624316 Series — Preliminary

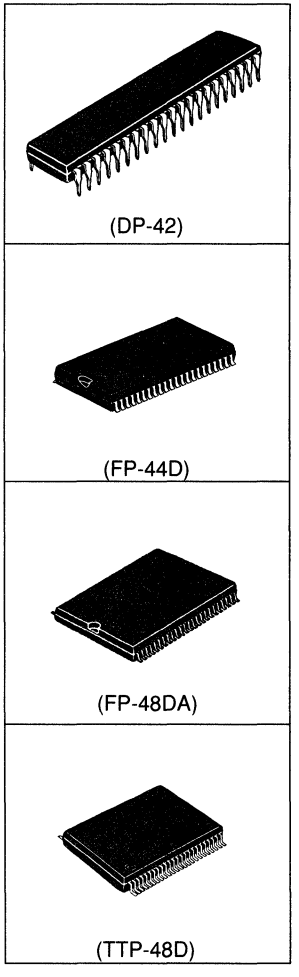
16M (1M x 16-bit) and (2M x 8-bit) Mask ROM

■ DESCRIPTION

The Hitachi HN624316 is a 16-Megabit CMOS Mask Programmable Read Only Memory organized as 1,048,576 x 16-bit and 2,097,152 x 8-bit.

The high density and high speed provide enough capacity and high performance to be used in a system using a high speed 16-bit or 32-bit microcomputer. In addition the low power consumption of this device makes it ideal for battery powered, portable systems.

Hitachi's HN624316 is offered with JEDEC-Standard pinouts in 42-pin Plastic DIP, 44-lead Plastic SOP and 48-lead Plastic TOP packages. The HN624316 is also packaged in a 48-lead Plastic SOP.



■ FEATURES

- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Fast Random Access Times:
  120 ns/150 ns (max)
- Low Power Consumption:
  Active Current: 300 mW (typ)
  Standby Current: 5 μW (typ)
- User Selectable Organization:
  1M x 16-bit (Word-Wide)
  2M x 8-bit (Byte-Wide)
  Switchable with BHE pin
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:
  JEDEC Standard Word-Wide/Byte-Wide Pinout
- Packages:
  42-pin Plastic DIP
  44-lead Plastic SOP
  48-lead Plastic SOP
  48-lead Plastic TSOP (Type II)

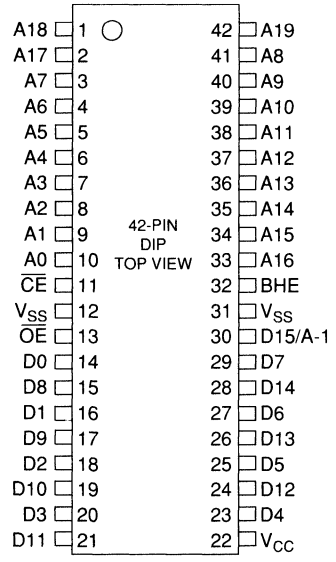
■ ORDERING INFORMATION

Type No.	Access Time	Package
HN624316P	120 ns 150 ns	42-pin Plastic DIP (DP-42)
HN624316FB	120 ns 150 ns	44-lead Plastic SOP (FP-44D)
HN624316F	120 ns 150 ns	48-lead Plastic SOP (FP-48DA)
HN624316TT	120 ns 150 ns	48-lead Plastic TSOP (TTP-48D)

Hitachi America, Ltd. • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

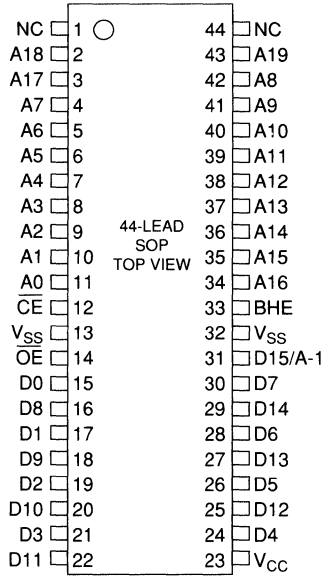
■ PIN ARRANGEMENT

HN624316P Series



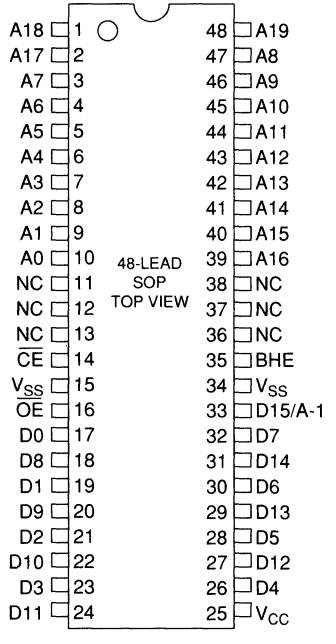
(PinD42.HN624316N)

HN624316FB Series



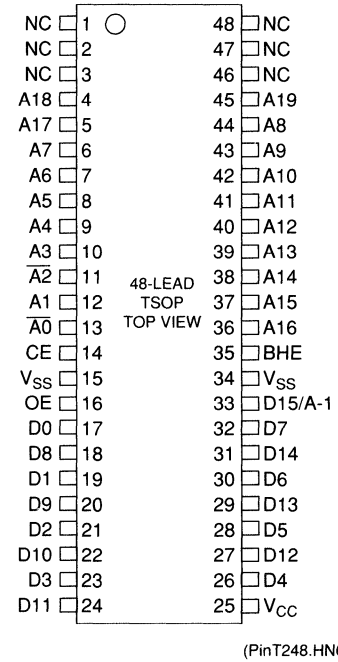
(PinT244.HN624316N)

HN624316F Series



(PinT248.HN624316N)

HN624316TT Series



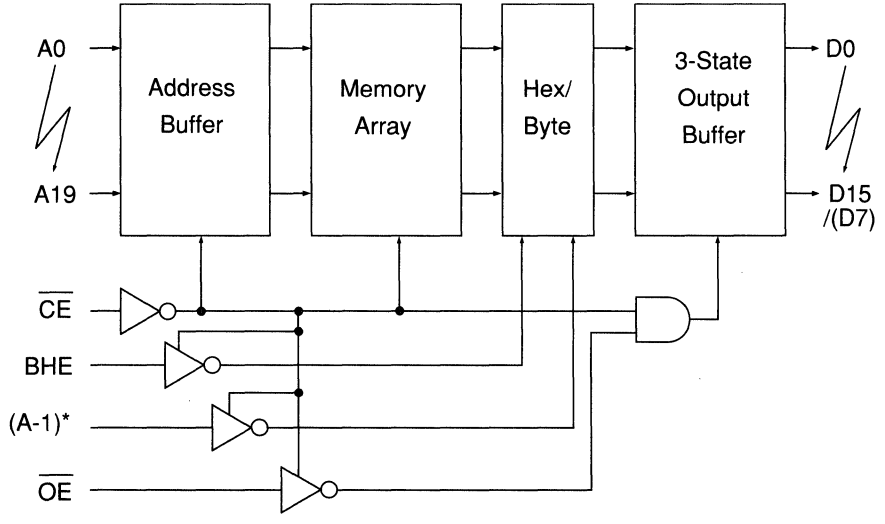
(PinT248.HN624116)

3

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{19}	Address
A_{-1}	Address (Word-Wide)
D_0 - D_{15}	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
BHE	Byte Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



(BD.HN624116)

Notes: 1. * : A_{-1} is the Least Significant Address bit in Byte-Wide Mode.
2. BHE=V_{IH} : 16-bit (D_{15} - D_0)
BHE=V_{IL} : 8-bit (D_7 - D_0)
When BHE is low, D_{14} - D_8 are in high impedance states.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
All Input and Output Voltage [1]	V_{IN}, V_{OUT}	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Notes: 1. Relative to V_{SS}.

■ CAPACITANCE

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0 V, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance [1]	C_{IN}	-	-	15	pF	V_{IN} = 0V
Output Capacitance [1]	C_{OUT}	-	-	15	pF	V_{OUT} = 0V

Notes: 1. This parameter is sampledand not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	10	µA	V_{IN} = 0 V to V_{CC}
Output Leakage Current	I_{LO}	-	-	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 V to V_{CC}
Operating V_{CC} Current	I_{CC}	-	-	100	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC}=min
Standby V_{CC} Current	I_{SB1}	-	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$-0.2V
	I_{SB2}	-	-	3	mA	V_{CC} = 5.5 V, CE ≥ 2.2V
Input Voltage	V_{IH}	2.2	-	V_{CC}+0.3	V	
	V_{IL}	-0.3	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -205 µA
	V_{OL}	-	-	0.4	V	I_{OL} = 1.6 mA

3

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Test Conditions

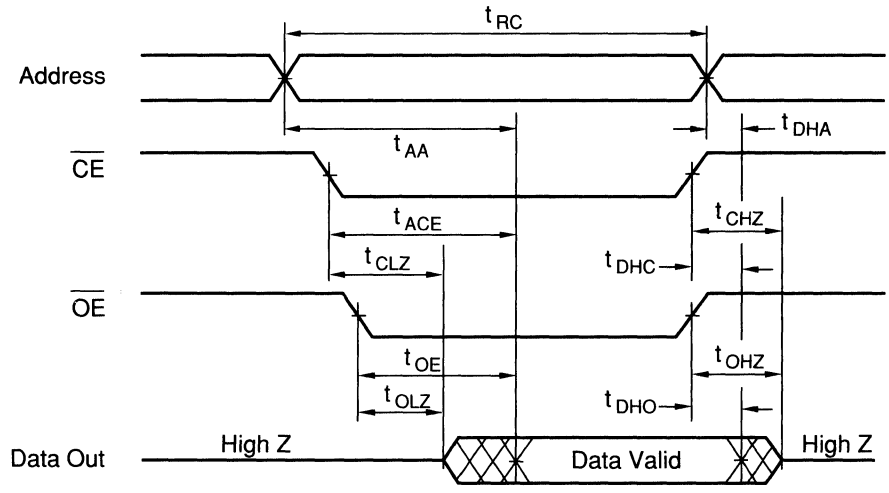
- Input pulse levels: 0.8 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Reference level for measuring timing: 1.5 V

Item	Symbol	HN624316-12		HN624316-15		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	120	-	150	-	ns
Address Access Time	t_{AA}	-	120	-	150	ns
Chip Enable Access Time	t_{ACE}	-	120	-	150	ns
Output Enable Access Time	t_{OE}	-	60	-	70	ns
BHE Access Time	t_{BHE}	-	120	-	150	ns
Output Hold Time from Address Change	t_{DHA}	0	-	0	-	ns
Output Hold Time from Chip Enable	t_{DHC}	0	-	0	-	ns
Output Hold Time from Output Enable	t_{DHO}	0	-	0	-	ns
Output Hold Time from BHE	t_{DHB}	0	-	0	-	ns
Chip Enable to Output in High-Z [1]	t_{CHZ}	-	60	-	70	ns
Output Enable to Output in High-Z [1]	t_{OHZ}	-	60	-	70	ns
BHE to Output in High-Z [1]	t_{BHZ}	-	60	-	70	ns
Chip Enable to Output in Low-Z	t_{CLZ}	10	-	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}	10	-	10	-	ns
BHE to Output in Low-Z	t_{BLZ}	10	-	10	-	ns

Note: 1. t_{CHZ}, t_{OHZ}, t_{BHZ} are defined as the time at which the output becomes an open circuit and are not referenced to output voltage levels.

■ READ TIMING WAVEFORM

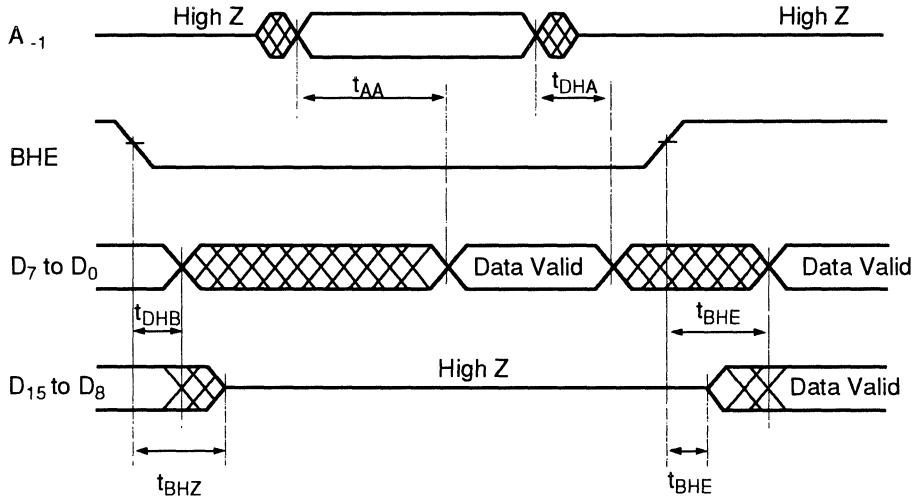
Word Mode (BHE = V_{IH}) or Byte Mode (BHE = V_{IL})



Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

(TD.R.HN624316N)

Word Mode/Byte Mode Switch



(TD.R1.HN624316N)

Note: 1. If $\overline{CE}$ and $\overline{OE}$ are enabled, A_{19} to A_0 are valid.
2. D_{15}/A_{-1} pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enabled. Therefore, the input signals of opposite phase to the output must not be applied to them.

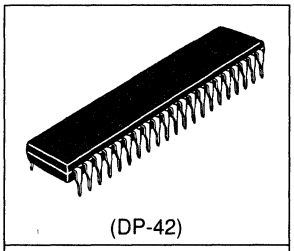
16M (1M x 16-bit) and (2M x 8-bit) Mask ROM

■ DESCRIPTION

The Hitachi HN624316N is a 16-Megabit CMOS Mask Programmable Read Only Memory organized as 1,048,576 x 16-bit and 2,097,152 x 8-bit.

The high density and high speed Fast Address Access provide enough capacity and high performance to be used in a system using a high speed 16-bit or 32-bit microcomputer. In addition the low power consumption of this device makes it ideal for battery powered, portable systems.

Hitachi's HN624316N is offered with JEDEC-Standard pinouts in 42-pin Plastic DIP, 44-lead Plastic SOP and 48-lead Plastic TOP packages. The HN624316N is also packaged in a 48-lead Plastic SOP.


(DP-42)


(FP-44D)


(FP-48DA)


(TTP-48D)

■ FEATURES

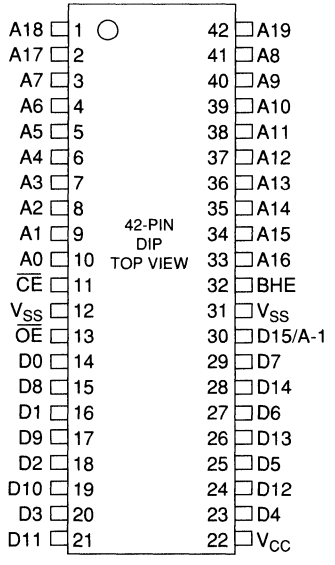
- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Fast Random Access Times:
  120 ns/150 ns (max)
- Fast Address Access Times (A_0, A_1):
  60 ns/70 ns (max)
- Low Power Consumption:
  Active Current: 300 mW (typ)
  Standby Current: 5 µW (typ)
- User Selectable Organization:
  1M x 16-bit (Word-Wide)
  2M x 8-bit (Byte-Wide)
  Switchable with BHE pin
- TTL-Compatible Inputs and Outputs
- Three-State Data Outputs
- Pin Arrangements:
  JEDEC Standard Word-Wide/Byte-Wide Pinout
- Packages:
  42-pin Plastic DIP
  44-lead Plastic SOP
  48-lead Plastic SOP
  48-lead Plastic TSOP (Type II)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN624316NP	120 ns 150 ns	42-pin Plastic DIP (DP-42)
HN624316NFB	120 ns 150 ns	44-lead Plastic SOP (FP-44D)
HN624316NF	120 ns 150 ns	48-lead Plastic SOP (FP-48DA)
HN624316NTT	120 ns 150 ns	48-lead Plastic TSOP (TTP-48D)

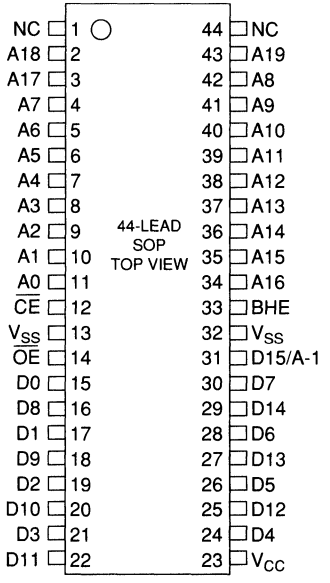
■ PIN ARRANGEMENT

HN624316NP Series



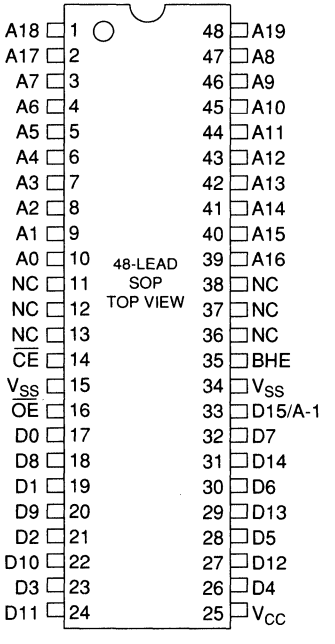
(PinD42.HN624316N)

HN624316NFB Series



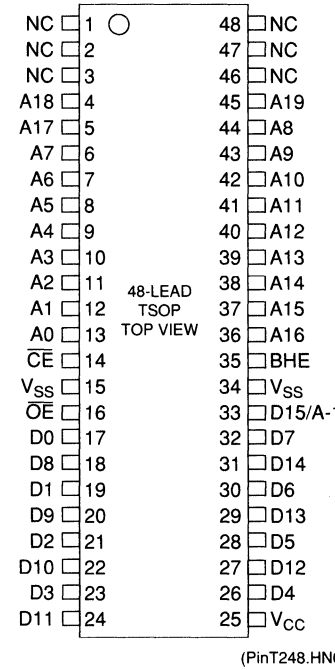
(PinT244.HN624316N)

HN624316NF Series



(PinT248.HN624316N)

HN624316NTT Series

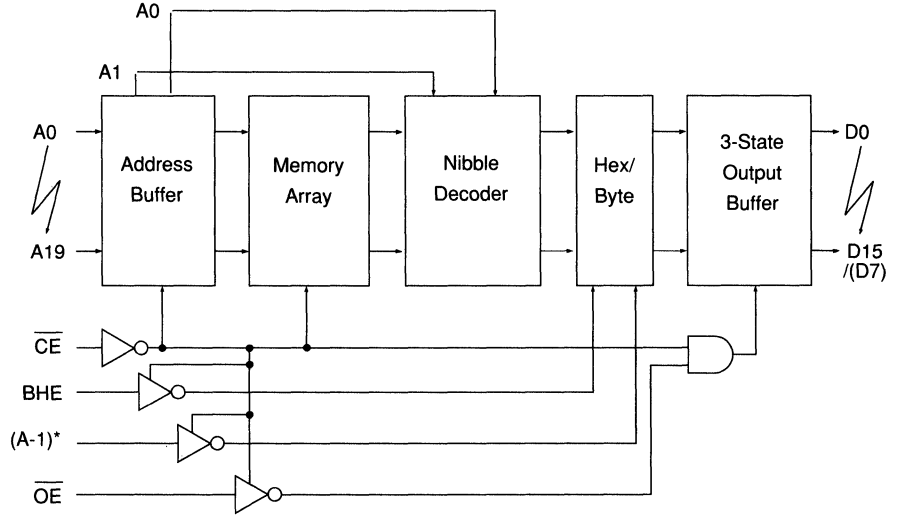


(PinT248.HN624116)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{19}	Address
A_{-1}	Address (Word-Wide)
D_0 - D_{15}	Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
BHE	Byte Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



(BD.HN624316N)

Notes: 1. * : A_{-1} is the Least Significant Address bit in Byte-Wide Mode.
2. BHE=V_{IH} : 16-bit (D_{15} - D_0)
BHE=V_{IL} : 8-bit (D_7 - D_0)
When BHE is low, D_{14} - D_8 are in high impedance states.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.3 to +7.0	V
All Input and Output Voltage [1]	V_{IN}, V_{OUT}	-0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Temperature Under Bias	T_{BIAS}	-20 to +85	°C

Notes: 1. Relative to V_{SS}.

■ CAPACITANCE

(V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 25°C, V_{IN} = 0 V, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance [1]	C_{IN}	-	-	15	pF	V_{IN} = 0V
Output Capacitance [1]	C_{OUT}	-	-	15	pF	V_{OUT} = 0V

Notes: 1. This parameter is sampledand not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	10	µA	V_{IN} = 0 V to V_{CC}
Output Leakage Current	I_{LO}	-	-	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 V to V_{CC}
Operating V_{CC} Current	I_{CC}	-	-	120	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC}=min
Standby V_{CC} Current	I_{SB}	-	-	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$-0.2V
Input Voltage	V_{IH}	2.2	-	V_{CC}+0.3	V	
	V_{IL}	-0.3	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -205 µA
	V_{OL}	-	-	0.4	V	I_{OL} = 1.6 mA

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{SS} = 0 V, T_a = 0 to 70°C)

Test Conditions

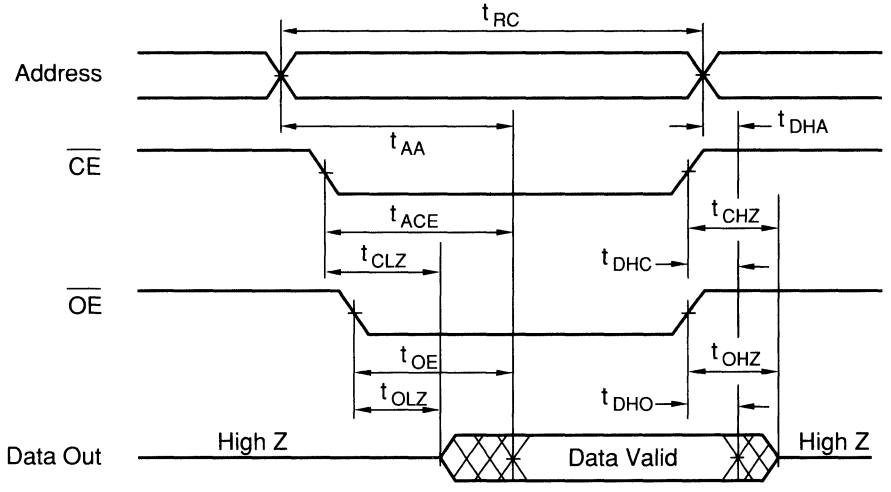
- Input pulse levels: 0.8 V / 2.4 V
- Input rise and fall times: ≤10 ns
- Output load: 1 TTL Gate + CL = 100 pF (Including jig capacitance)
- Reference level for measuring timing: 1.5 V

Item	Symbol	HN624316N-12		HN624316N-15		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	120	-	150	-	ns
Fast Address Read Cycle Time	t_{BC}	60	-	70	-	ns
Address Access Time	t_{AA}	-	120	-	150	ns
Fast Address Access Time	t_{BA}	-	60	-	70	ns
Chip Enable Access Time	t_{ACE}	-	120	-	150	ns
Output Enable Access Time	t_{OE}	-	60	-	70	ns
BHE Access Time	t_{BHE}	-	120	-	150	ns
Output Hold Time from Address Change	t_{DHA}	0	-	0	-	ns
Output Hold Time from Chip Enable	t_{DHC}	0	-	0	-	ns
Output Hold Time from Output Enable	t_{DHO}	0	-	0	-	ns
Output Hold Time from BHE	t_{DHB}	0	-	0	-	ns
Chip Enable to Output in High-Z [1]	t_{CHZ}	-	60	-	70	ns
Output Enable to Output in High-Z [1]	t_{OHZ}	-	60	-	70	ns
BHE to Output in High-Z [1]	t_{BHZ}	-	60	-	70	ns
Chip Enable to Output in Low-Z	t_{CLZ}	10	-	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}	10	-	10	-	ns
BHE to Output in Low-Z	t_{BLZ}	10	-	10	-	ns

Note: 1. t_{CHZ}, t_{OHZ}, t_{BHZ} are defined as the time at which the output becomes an open circuit and are

■ READ TIMING WAVEFORM

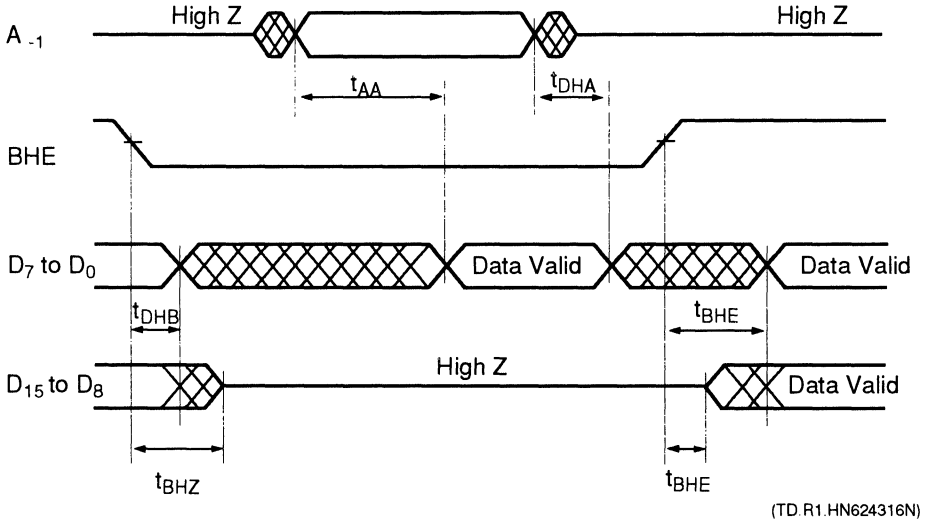
Word Mode (BHE = V_{IH}) or Byte Mode (BHE = V_{IL})



Note: 1. t_{DHA}, t_{DHC}, t_{DHO} are determined by the faster time.
2. t_{AA}, t_{ACE}, t_{OE} are determined by the slower time.
3. t_{CLZ}, t_{OLZ} are determined by the slower time.

(TD.R.HN624316N)

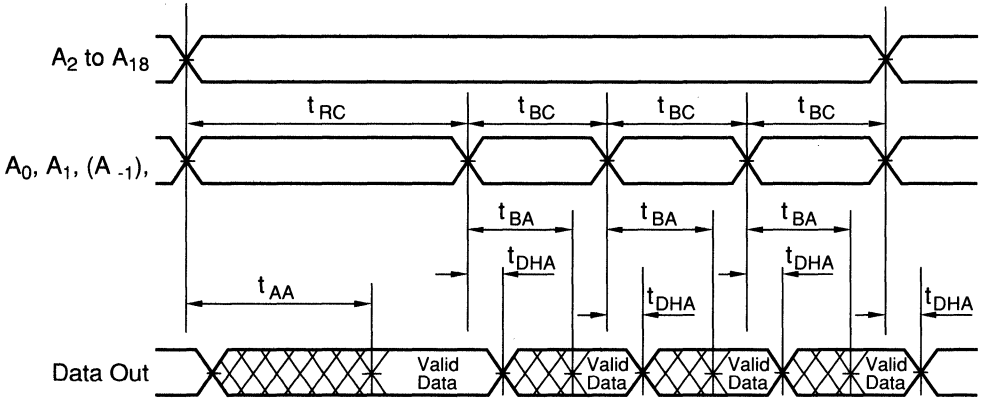
Word Mode/Byte Mode Switch



(TD.R1.HN624316N)

Note: 1. If $\overline{CE}$ and $\overline{OE}$ are enabled, A_{19} to A_0 are valid.
2. D_{15}/A_{-1} pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enabled. Therefore, the input signals of opposite phase to the output must not be applied to them.

Fast Address Access



(TD.RN.HN62438N)

Note: $\overline{CE}$ and $\overline{OE}$ are enabled.

EPROM (UV Erasable and OTP)

SECTION 4
EPROM (UV Erasable and OTP)

HITACHI

Hitachi America, Ltd. • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

HITACHI

Hitachi America, Ltd. • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

HN27C256A Series

Maintenance Only

256K (32K x 8-bit) UV and OTP EPROM

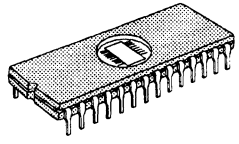
■ DESCRIPTION

The Hitachi HN27C256A is a 256-Kilobit Ultraviolet Erasable and One-Time Programmable Electrically Programmable Read Only Memory organized as 32,768 x 8-bits.

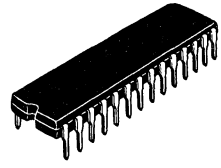
The HN27C256A features fast address access times and low power dissipation. This combination makes the HN27C256A suitable for high speed microcomputer systems. The HN27C256A also offers high speed programming.

Hitachi's HN27C256A is offered in JEDEC-Standard Byte-Wide EPROM pinouts in 28-pin Ceramic and Plastic DIP and 28-lead Plastic SOP packages.

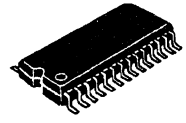
The Ceramic DIP package is erasable by exposure to Ultraviolet light. The Plastic DIP and SOP packaged devices are One-Time Programmable and once programmed, can not be rewritten.



(DG-28)



(DP-28)



(FP-28DA)

■ FEATURES

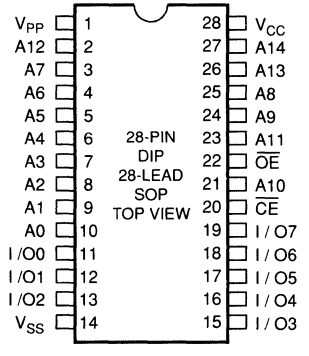
- Fast Access Times:
  100 ns/120ns/150 ns (max)
- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Low Power Dissipation:
  Active Mode: 25 mW/MHz (typ)
  Standby Mode: 5 µW (typ)
- High Speed Programming
- Programming Power Supply:
  V_{PP} = 12.5 V ± 0.5 V
- Pin Arrangement:
  JEDEC Standard Byte-Wide EPROM
- Packages:
  28-pin Ceramic DIP
  28-pin Plastic DIP
  28-lead Plastic SOP

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN27C256AG-10	100 ns	28-pin Ceramic DIP
HN27C256AG-12	120 ns	(DG-28)
HN27C256AP-12	120 ns	28-pin Plastic DIP
HN27C256AP-15	150 ns	(DP-28)
HN27C256AFP-12T	120 ns	28-lead Plastic SOP
HN27C256AFP-15T	150 ns	(FP-28DA)

■ PIN ARRANGEMENT

HN27C256AG/P Series
HN27C256AFP Series



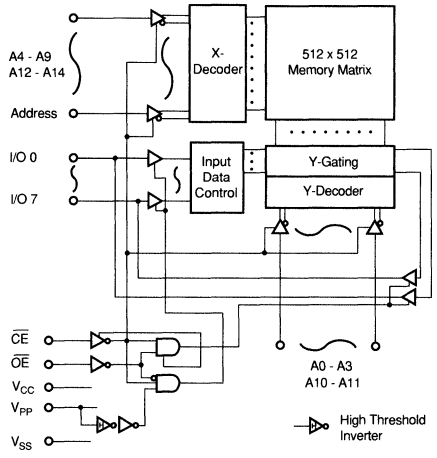
(PinD28.HN27C256A)

4

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{14}	Address
I/O_0 - I/O_7	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{PP}	Programming Supply
V_{SS}	Ground

■ BLOCK DIAGRAM



(BD.HN27C256H)

■ MODE SELECTION

Mode	V_{PP}	V_{CC}	$\overline{CE}$	$\overline{OE}$	A_9	I/O
Read	V_{CC}	V_{CC}	V_{IL}	V_{IL}	X[1]	D_{OUT}
Output Disable	V_{CC}	V_{CC}	V_{IL}	V_{IH}	X	High-Z
Standby	V_{CC}	V_{CC}	V_{IH}	X	X	High-Z
Program	V_{PP}	V_{CC}	V_{IL}	V_{IH}	X	D_{IN}
Program Verify	V_{PP}	V_{CC}	V_{IH}	V_{IL}	X	D_{OUT}
Optional Verify	V_{PP}	V_{CC}	V_{IL}	V_{IL}	X	D_{OUT}
Program Inhibit	V_{PP}	V_{CC}	V_{IH}	V_{IH}	X	High-Z
Identifier	V_{CC}	V_{CC}	V_{IL}	V_{IL}	V_H[2]	ID

Notes: 1. X = Don't Care.
2. $11.5\ V \leq V_H \leq 12.5\ V$

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Programming Voltage [1]	V_{PP}	-0.6 to +13.5	V
All Input and Output Voltage [1,2]	V_{IN}, V_{OUT}	-0.6 to +7.0	V
A_9 Input Voltage [2]	V_{ID}	-0.6 to +13.5	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-65 to +125 [3] -55 to +125 [4]	°C
Storage Temperature Under Bias	T_{BIAS}	-10 to +80	°C

Notes: 1. Relative to V_{SS}.
2. V_{IN}, V_{OUT}, and V_{ID} min = -1.0V for pulse width ≤ 50 ns.
3. HN27C256AG.
4. HN27C256AP and HN27C256AFP.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	4	8	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	8	12	pF	V_{OUT} = 0V

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{IN} = 0 V to V_{CC}
Output Leakage Current	I_{LO}	-	-	2	µA	V_{OUT} = 0 V to V_{CC}
Operating V_{CC} Current	I_{CC1}	-	-	30	mA	I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}
	I_{CC2}	-	-	30	mA	I_{OUT} = 0 mA, f = 10 MHz
	I_{CC3}	-	5	15	mA	I_{OUT} = 0 mA, f = 1 MHz
Standby V_{CC} Current	I_{SB}	-	-	1	mA	$\overline{CE}$ = V_{IH}
V_{PP} Current	I_{PP1}	-	1	20	µA	V_{PP} = 5.5 V
Input Voltage	V_{IH}	2.2	-	V_{CC} + 1 [2]	V	
	V_{IL}	-0.3 [1]	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = 1.0 mA
	V_{OL}	-	-	0.45	V	I_{OL} = 2.1 mA

Notes: 1. V_{IL} min = -1.0 V for pulse width ≤ 50 ns.
2. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns.
If V_{IH} is over the specified maximum value, Read operation can not be guaranteed.

4

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{CC}, T_a = 0 to 70°C)

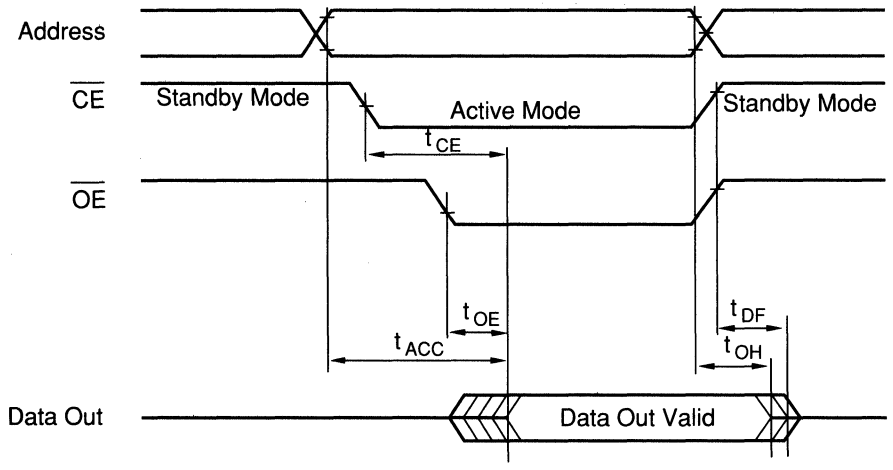
Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V / 2.0 V

Item	Symbol	-10 Min.	-10 Max.	-12 Min.	-12 Max.	-15 Min.	-15 Max.	Unit	Test Condition
Address Access Time	t_{ACC}	-	100	-	120	-	150	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
Chip Enable Access Time	t_{CE}	-	100	-	120	-	150	ns	$\overline{OE}$ = V_{IL}
Output Enable Access Time	t_{OE}	-	60	-	60	-	70	ns	$\overline{CE}$ = V_{IL}
Output Disable to High-Z [1]	t_{DF}	0	35	0	40	0	50	ns	$\overline{CE}$ = V_{IL}
Output Hold to Address Change	t_{OH}	5	-	5	-	5	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



(TD.R.HN27C256A)

■ DC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

(V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.5 V, T_a = 25 °C ± 5 °C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{IN} = 0 V to V_{CC}
Operating V_{CC} Current	I_{CC}	-	-	30	mA	
Operating V_{PP} Current	I_{PP}	-	-	30	mA	$\overline{CE}$ = V_{IL}
Input Voltage [3]	V_{IH}	2.2	-	V_{CC} +.5 [6]	V	
	V_{IL}	- 0.1[5]	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA
	V_{OL}	-	-	0.45	V	I_{OH} = 2.1 mA

Notes:
1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13 V, including overshoot.
3. Device reliability may be adversely affected if the device is installed or removed while V_{PP} = 12.5 V.
4. Do not change V_{PP} from V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = low.
5. V_{IL} min = -0.6 V for pulse width ≤ 20 ns.
6. If V_{IH} is over the specified maximum value, programming operation can not be guaranteed.

■ AC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

(V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.5 V, T_a = 25°C ± 5°C)

Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 20 ns
- Reference levels for measuring timing: 0.8 V / 2.0V

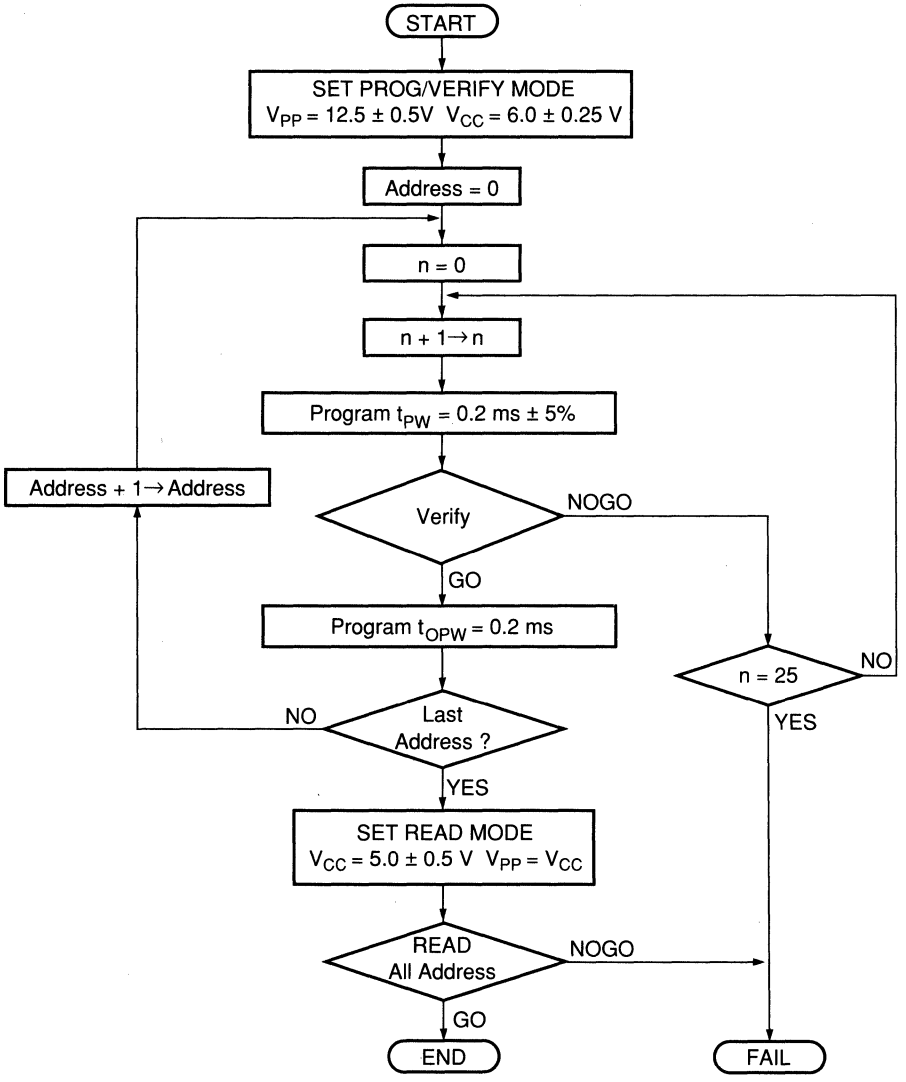
Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	2	-	-	µs	
Address Hold Time	t_{AH}	0	-	-	µs	
Data Setup Time	t_{DS}	2	-	-	µs	
V_{PP} Setup Time	t_{VPS}	2	-	-	µs	
V_{CC} Setup Time	t_{VCS}	2	-	-	µs	
Output Enable Setup Time	t_{OES}	2	-	-	µs	
Output Disable Time	t_{DF}	0	-	130	ns	
$\overline{CE}$ Initial Programming Pulse Width	t_{PW}	0.95	1.0	1.05	ms	
$\overline{CE}$ Overprogramming Pulse Width	t_{OPW}	2.85	-	78.75	ms	
Data Valid from Output Enable Time	t_{OE}	0	-	150	ns	

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

4

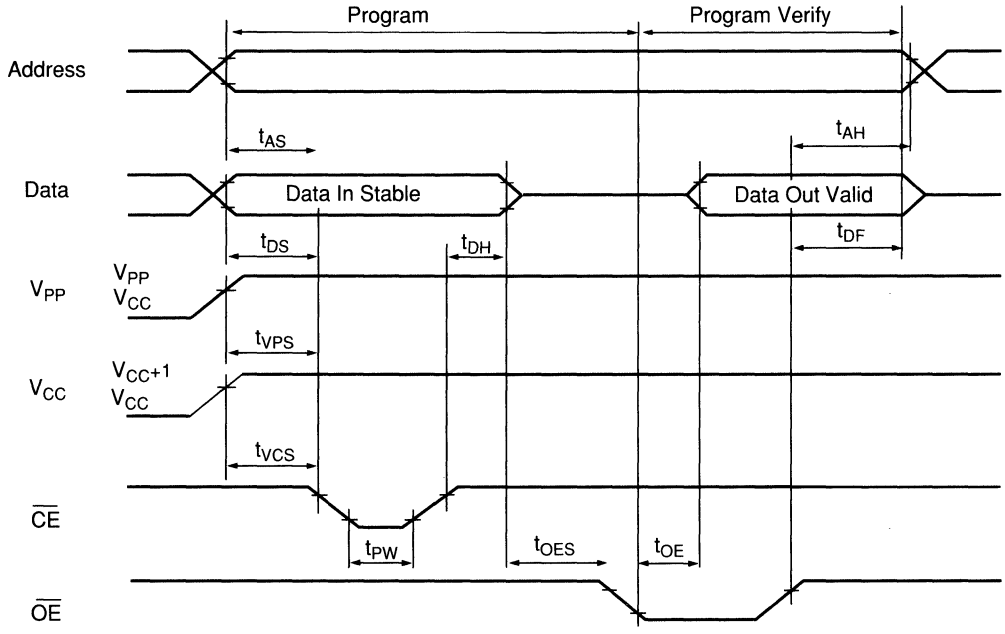
■ FAST HIGH-RELIABILITY PROGRAMMING FLOWCHART

The Hitachi HN27C256A can be programmed with the Fast High-Reliability Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data. This algorithm theoretically provides one-tenth the programming time of the conventional High Performance Programming algorithm.



(FC.P.HN27C256A)

■ FAST HIGH-RELIABILITY PROGRAMMING TIMING WAVEFORM

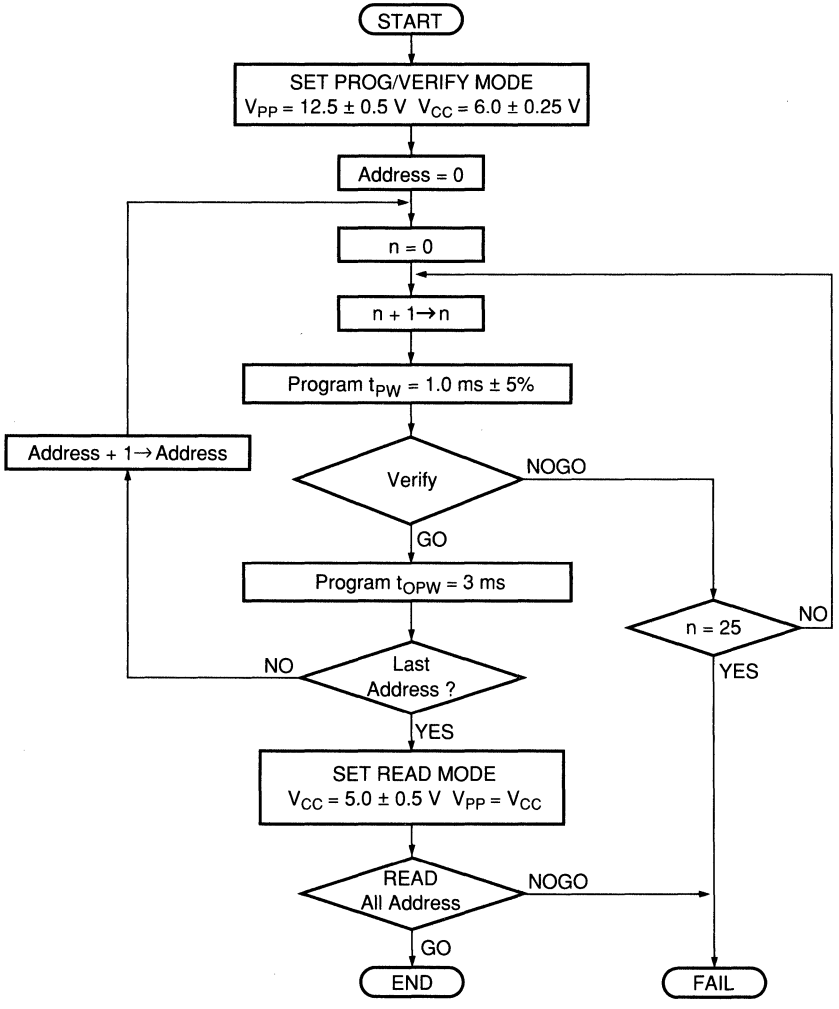


(TD.P.HN27C256A)

4

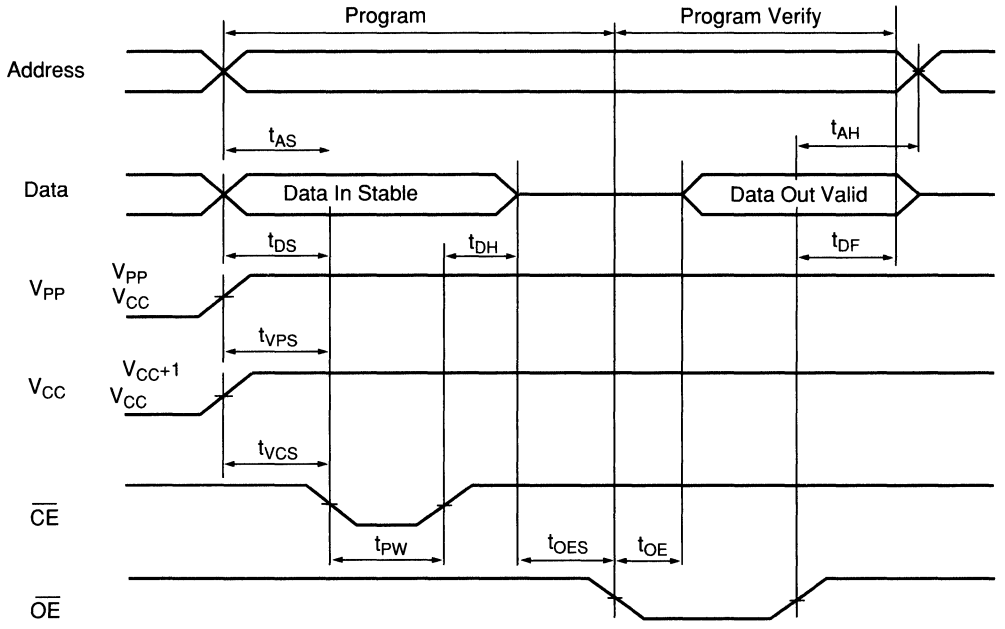
■ HIGH PERFORMANCE PROGRAMMING FLOWCHART

The Hitachi HN27C256A can be programmed with the High Performance Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.



(FC.PP.HN27C256A)

■ HIGH PERFORMANCE PROGRAMMING TIMING WAVEFORM



(TD.PP.HN27C256A)

4

■ ERASING THE HN27C256A

The Hitachi HN27C256A Ceramic DIP package allow the device to be erased by exposure to ultraviolet light of 2537Å. All of the data is changed to "1" after this erasure procedure. The minimum integrated dose (UV intensity x exposure time) for erasure is 15 W-sec/cm^2.

■ DEVICE IDENTIFIER MODE DESCRIPTION

The Device Identifier Mode allows binary codes to be read from the outputs that identify the manufacturer and the type of device. Using this mode with programming equipment, the device will automatically match its own erase and programming algorithm.

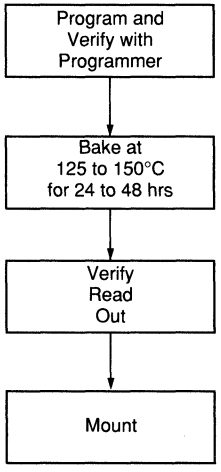
■ HN27C256A SERIES IDENTIFIER CODE

Identifier	A_0	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	0	0	1	1	0	0	0	1	31

Notes: 1. $A_9 = 12.0\ V \pm 0.5V$
3. A_1-A_8, A_{10}-A_{14}, $\overline{CE}$, $\overline{OE} = V_{IL}$

■ HN27C256AP/FP RECOMMENDED SCREENING CONDITIONS

Before mounting the HN27C256A plastic packages, please make the following screening (baking without bias) shown below:



(RSC.EPROM)

HN27C256H Series

256K (32K x 8-bit) UV and OTP EPROM

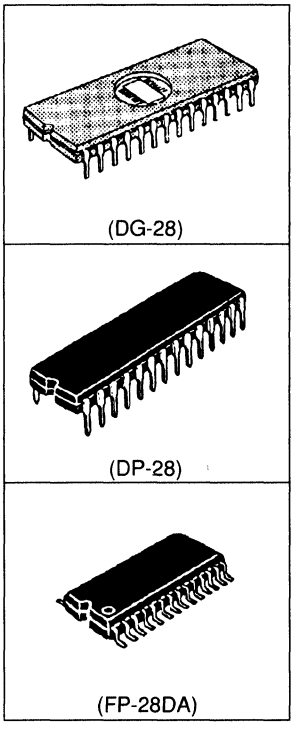
■ DESCRIPTION

The Hitachi HN27C256H is a 256-Kilobit Ultraviolet Erasable and One-Time Programmable Electrically Programmable Read Only Memory organized as 32,768 x 8-bits.

The HN27C256H features fast address access times and low power dissipation. This combination makes the HN27C256H suitable for high speed microcomputer systems. The HN27C256H also offers high speed programming.

Hitachi's HN27C256H is offered in JEDEC-Standard Byte-Wide EPROM pinouts in 28-pin Ceramic and Plastic DIP and 28-lead Plastic SOP packages.

The Ceramic DIP package is erasable by exposure to Ultraviolet light. The Plastic DIP and SOP packaged devices are One-Time Programmable and once programmed, can not be rewritten.



■ FEATURES

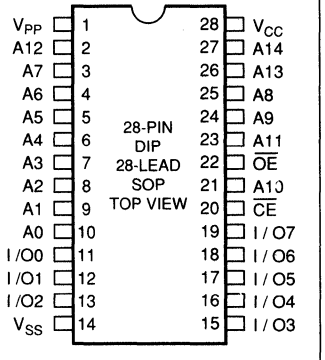
- Fast Access Times:
  70 ns/85 ns/100 ns (max)
- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Low Power Dissipation:
  Active Mode: 30 mW/MHz (typ)
  Standby Mode: 15 mA (max)
- High Speed Programming
- Programming Power Supply:
  V_{PP} = 12.5 V ± 0.5 V
- Pin Arrangement:
  JEDEC Standard Byte-Wide EPROM
- Packages:
  28-pin Ceramic DIP
  28-pin Plastic DIP
  28-lead Plastic SOP

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN27C256HG-70	70 ns	28-pin Ceramic DIP
HN27C256HG-85	85 ns	(DG-28)
HN27C256HP-85	85 ns	28-pin Plastic DIP
HN27C256HP-10	100 ns	(DP-28)
HN27C256HFP-85T	85 ns	28-lead Plastic SOP
HN27C256HFP-10T	100 ns	(FP-28DA)

■ PIN ARRANGEMENT

HN27C256HG/P Series
HN27C256HFP Series



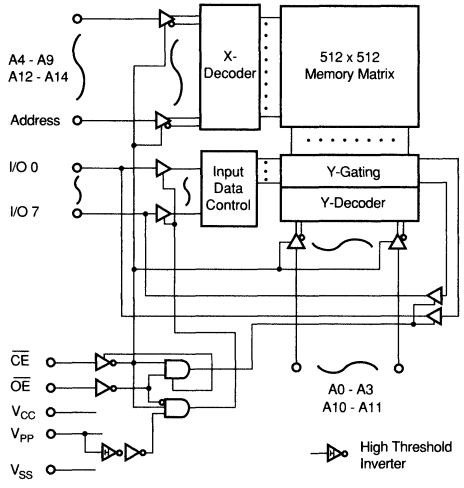
(PinD28.HN27C256H)

4

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{14}	Address
I/O_0 - I/O_7	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{PP}	Programming Supply
V_{SS}	Ground

■ BLOCK DIAGRAM



(BD.HN27C256H)

■ MODE SELECTION

Mode	V_{PP}	V_{CC}	$\overline{CE}$	$\overline{OE}$	A_9	I/O
Read	V_{CC}	V_{CC}	V_{IL}	V_{IL}	X[1]	D_{OUT}
Output Disable	V_{CC}	V_{CC}	V_{IL}	V_{IH}	X	High-Z
Standby	V_{CC}	V_{CC}	V_{IH}	X	X	High-Z
Program	V_{PP}	V_{CC}	V_{IL}	V_{IH}	X	D_{IN}
Program Verify	V_{PP}	V_{CC}	V_{IH}	V_{IL}	X	D_{OUT}
Optional Verify	V_{PP}	V_{CC}	V_{IL}	V_{IL}	X	D_{OUT}
Program Inhibit	V_{PP}	V_{CC}	V_{IH}	V_{IH}	X	High-Z
Identifier	V_{CC}	V_{CC}	V_{IL}	V_{IL}	V_H[2]	ID

Notes: 1. X = Don't Care.
2. $11.5\ V \leq V_H \leq 12.5\ V$

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Programming Voltage [1]	V_{PP}	-0.6 to +13.5	V
All Input and Output Voltage [1,2]	V_{IN}, V_{OUT}	-0.6 to +7.0	V
A_9 Input Voltage [2]	V_{ID}	-0.6 to +13.5	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-65 to +125 [3] -55 to +125 [4]	°C
Storage Temperature Under Bias	T_{BIAS}	-10 to +80	°C

Notes: 1. Relative to V_{SS}.
2. V_{IN}, V_{OUT}, and V_{ID} min = -1.0V for pulse width ≤ 50 ns.
3. HN27C256HG.
4. HN27C256HP and HN27C256HFP.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	4	8	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	8	12	pF	V_{OUT} = 0V

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{IN} = 0 V to V_{CC}
Output Leakage Current	I_{LO}	-	-	2	µA	V_{OUT} = 0 V to V_{CC}
Operating V_{CC} Current	I_{CC1}	-	-	30	mA	I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}
	I_{CC2}	-	-	40	mA	I_{OUT} = 0 mA, f = 11.8 MHz
	I_{CC3}	-	5	15	mA	I_{OUT} = 0 mA, f = 1 MHz
Standby V_{CC} Current	I_{SB}	-	-	15	mA	$\overline{CE}$ = V_{IH}
V_{PP} Current	I_{PP1}	-	1	100	µA	V_{PP} = 5.5 V
Input Voltage	V_{IH}	2.2	-	V_{CC} + 1 [2]	V	
	V_{IL}	-0.3 [1]	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA
	V_{OL}	-	-	0.45	V	I_{OL} = 2.1 mA

Notes: 1. V_{IL} min = -1.0 V for pulse width ≤ 50 ns.
2. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns.
If V_{IH} is over the specified maximum value, Read operation can not be guaranteed.

4

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{CC}, T_a = 0 to 70°C)

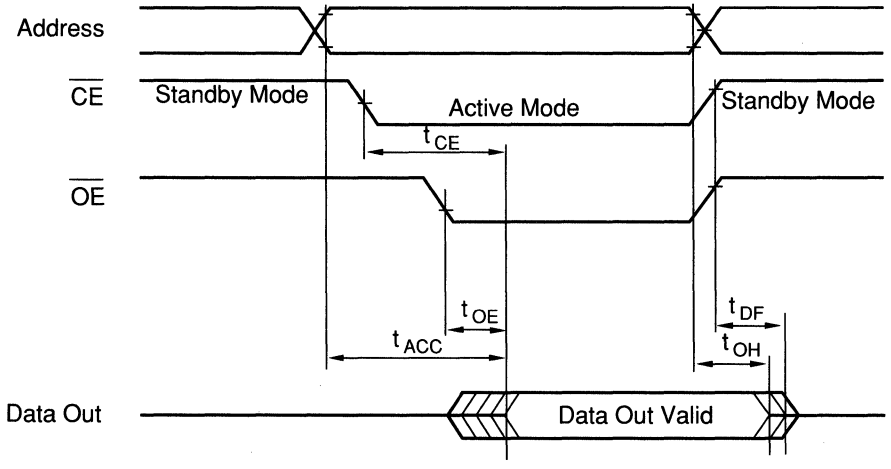
Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 1.5 V / 1.5V

Item	Symbol	-70 Min.	-70 Max.	-85 Min.	-85 Max.	-10 Min.	-10 Max.	Unit	Test Condition
Address Access Time	t_{ACC}	-	70	-	85	-	100	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
Chip Enable Access Time	t_{CE}	-	70	-	85	-	100	ns	$\overline{OE}$ = V_{IL}
Output Enable Access Time	t_{OE}	-	40	-	45	-	55	ns	$\overline{CE}$ = V_{IL}
Output Disable to High-Z [1]	t_{DF}	0	30	0	30	0	35	ns	$\overline{CE}$ = V_{IL}
Output Hold to Address Change	t_{OH}	5	-	5	-	5	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



(TD.R.HN27C256H)

■ DC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

(V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.5 V, T_a = 25 °C ± 5 °C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{IN} = 0 V to V_{CC}
Operating V_{CC} Current	I_{CC}	-	-	30	mA	
Operating V_{PP} Current	I_{PP}	-	-	30	mA	$\overline{CE}$ = V_{IL}
Input Voltage [3]	V_{IH}	2.2	-	V_{CC} +.5 [6]	V	
	V_{IL}	- 0.1[5]	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA
	V_{OL}	-	-	0.45	V	I_{OH} = 2.1 mA

Notes:
1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13 V, including overshoot.
3. Device reliability may be adversely affected if the device is installed or removed while V_{PP} = 12.5 V.
4. Do not change V_{PP} from V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = low.
5. V_{IL} min = -0.6 V for pulse width ≤ 20 ns.
6. If V_{IH} is over the specified maximum value, programming operation can not be guaranteed.

■ AC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

(V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 v ± 0.5 V, T_a = 25°C ± 5°C)

Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 20 ns
- Reference levels for measuring timing: 0.8 V / 2.0V

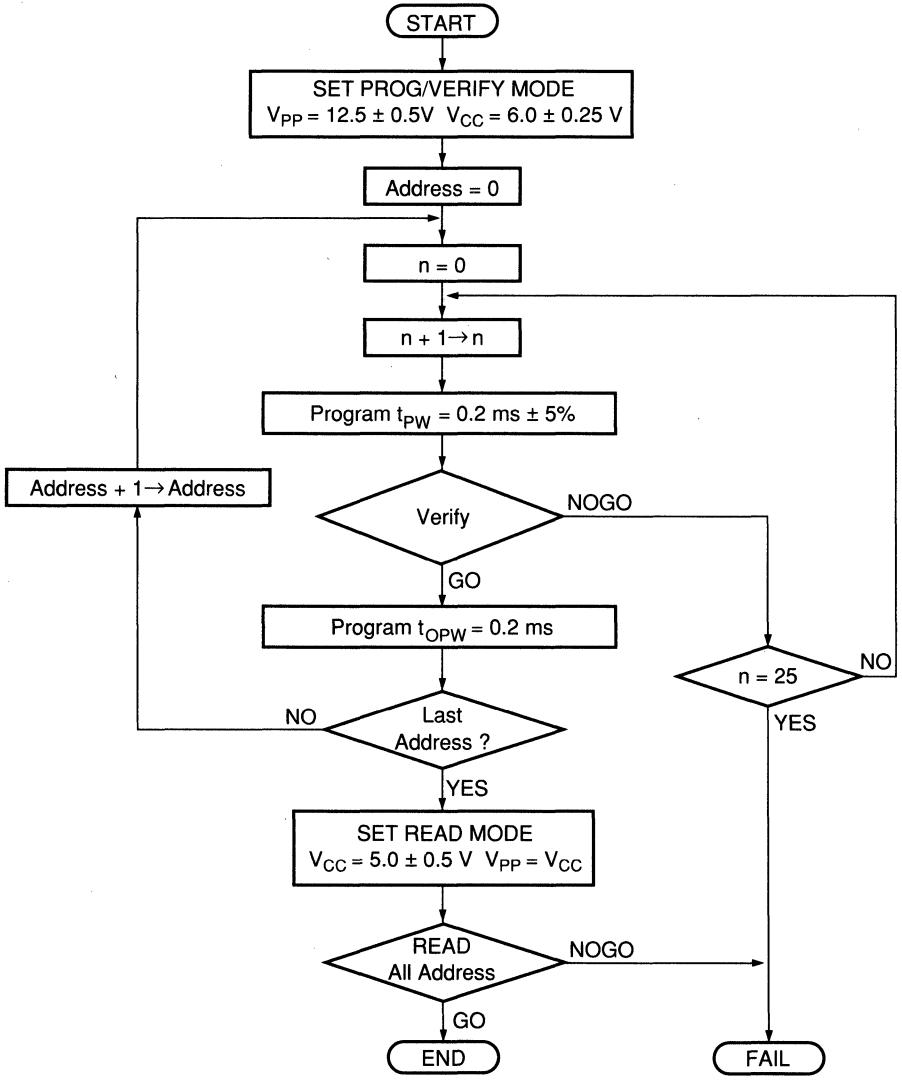
Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	2	-	-	µs	
Address Hold Time	t_{AH}	0	-	-	µs	
Data Setup Time	t_{DS}	2	-	-	µs	
V_{PP} Setup Time	t_{VPS}	2	-	-	µs	
V_{CC} Setup Time	t_{VCS}	2	-	-	µs	
Output Enable Setup Time	t_{OES}	2	-	-	µs	
Output Disable Time	t_{DF}	0	-	130	ns	
$\overline{CE}$ Initial Programming Pulse Width	t_{PW}	0.19	0.20	0.21	ms	
$\overline{CE}$ Overprogramming Pulse Width	t_{OPW}	0.19	-	5.25	ms	
Data Valid from Output Enable Time	t_{OE}	0	-	150	ns	

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

4

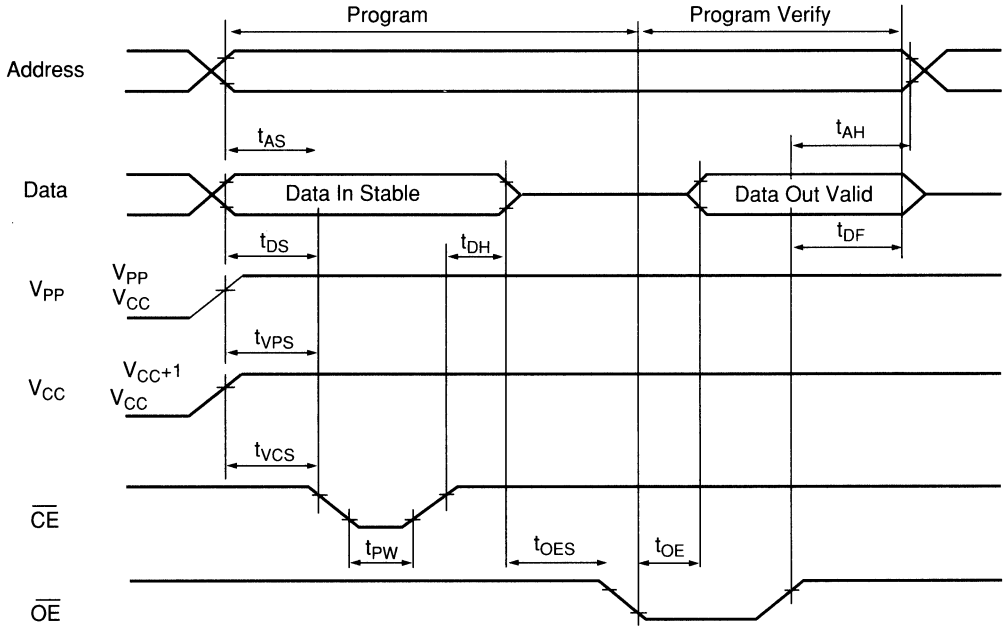
■ FAST HIGH-RELIABILITY PROGRAMMING FLOWCHART

The Hitachi HN27C256H can be programmed with the Fast High-Reliability Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data. This algorithm theoretically provides one-tenth the programming time of the conventional High Performance Programming algorithm.



(FC.P.HN27C256H)

■ FAST HIGH-RELIABILITY PROGRAMMING TIMING WAVEFORM

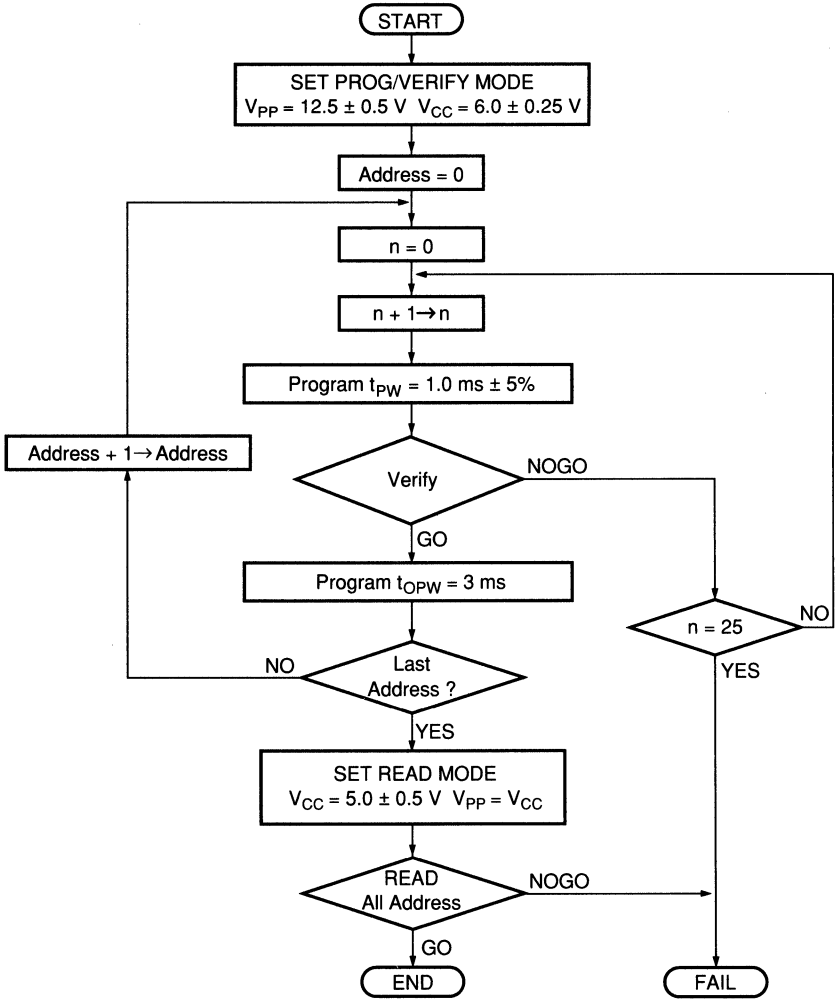


(TD.P.HN27C256H)

4

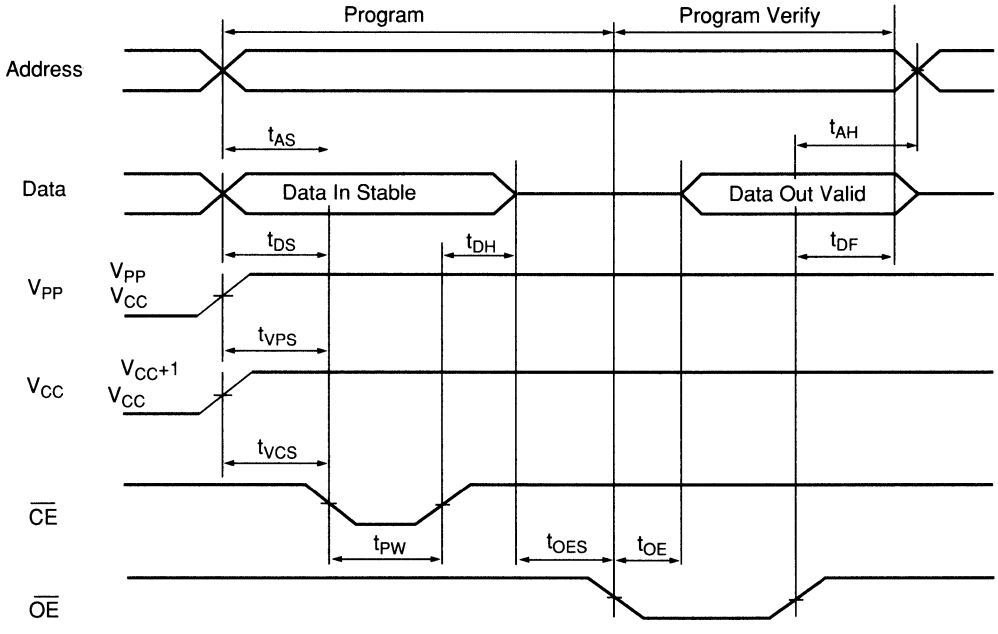
■ HIGH PERFORMANCE PROGRAMMING FLOWCHART

The Hitachi HN27C256H can be programmed with the High Performance Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.



(FC.PP.HN27C256H)

■ HIGH PERFORMANCE PROGRAMMING TIMING WAVEFORM



(TD.PP.HN27C256H)

4

■ ERASING THE HN27C256H

The Hitachi HN27C256H Ceramic DIP package allow the device to be erased by exposure to ultraviolet light of 2537Å. All of the data is changed to "1" after this erasure procedure. The minimum integrated dose (UV intensity x exposure time) for erasure is 15 W-sec/cm^2.

■ DEVICE IDENTIFIER MODE DESCRIPTION

The Device Identifier Mode allows binary codes to be read from the outputs that identify the manufacturer and the type of device. Using this mode with programming equipment, the device will automatically match its own erase and programming algorithm.

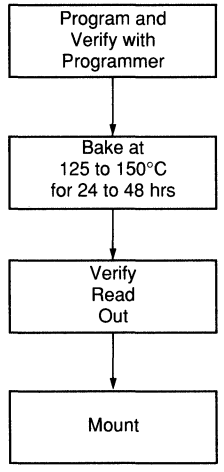
■ HN27C256H SERIES IDENTIFIER CODE

Identifier	A_0	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	0	0	1	1	0	0	0	1	31

Notes: 1. $A_9 = 12.0\ V \pm 0.5V$
3. A_1-A_8, A_{10}-A_{14}, $\overline{CE}$, $\overline{OE} = V_{IL}$

■ HN27C256HP/FP RECOMMENDED SCREENING CONDITIONS

Before mounting the HN27C256H plastic packages, please make the following screening (baking without bias) shown below:



(RSC.EPROM)

HN27512 Series

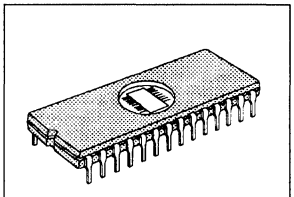
512K (64K x 8-bit) UV and OTP EPROM

■ DESCRIPTION

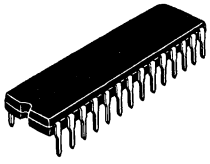
The Hitachi HN27512 is a 512-Kilobit Ultraviolet Erasable and One-Time Programmable Electrically Programmable Read Only Memory organized as 65,536 x 8-bits.

The HN27512 features low power dissipation and high speed programming.

Hitachi's HN27512 is offered in JEDEC-Standard Byte-Wide EPROM pinouts in a 28-pin Ceramic and Plastic DIP packages.



(DG-28)



(DP-28)

■ FEATURES

- Fast Access Times:
  250 ns/300 ns (max)
- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Low Power Dissipation:
  Active Mode: 45 mA (typ)
  Standby Mode: 40 mA (max)
- High Speed Programming
- Programming Power Supply:
  V_{PP} = 12.5 V ± 0.3 V
- Pin Arrangement:
  JEDEC Standard Byte-Wide EPROM
- Package:
  28-pin Ceramic DIP
  28-pin Plastic DIP

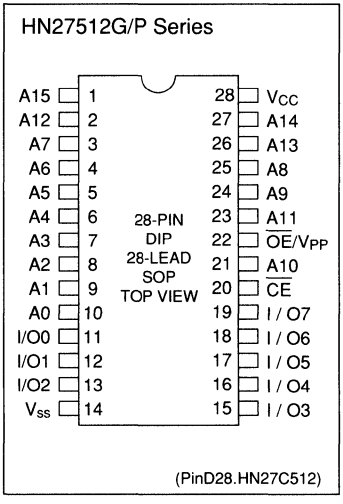
■ ORDERING INFORMATION

Type No.	Access Time	Package
HN27512G-25	250 ns	28-pin Ceramic DIP
HN27512G-30	300 ns	(DG-28)
HN27512P-25	250 ns	28-pin Plastic DIP
HN27512P-30	300 ns	(DP-28)

■ PIN DESCRIPTION

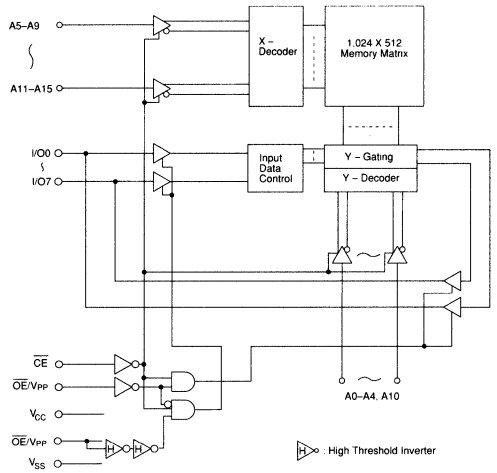
Pin Name	Function
A_0 - A_{15}	Address
I/O_0 - I/O_7	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{PP}	Programming Supply
V_{SS}	Ground

■ PIN ARRANGEMENT



4

■ BLOCK DIAGRAM



(BD.HN27512)

■ MODE SELECTION

Mode	V_{CC}	$\overline{CE}$	$\overline{OE}/V_{PP}$	A_9	I/O
Read	V_{CC}	V_{IL}	V_{IL}	X [1]	D_{OUT}
Output Disable	V_{CC}	V_{IL}	V_{IH}	X	High-Z
Standby	V_{CC}	V_{IH}	X	X	High-Z
Program	V_{CC}	V_{IL}	V_{PP}	X	D_{IN}
Program Verify	V_{CC}	V_{IL}	V_{IL}	X	D_{OUT}
Program Inhibit	V_{CC}	V_{IH}	V_{PP}	X	High-Z
Identifier	V_{CC}	V_{IL}	V_{IL}	V_H [2]	ID

Notes: 1. X = Don't Care.
2. $11.5\ V \leq V_H \leq 12.5\ V$

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Programming Voltage [1]	V_{PP}	-0.6 to +13.5	V
All Input and Output Voltage [1]	V_{IN}, V_{OUT}	-0.6 to +7.0	V
A_9 Input Voltage	V_{ID}	-0.6 to +13.5	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-65 to +125 [2] -55 to +125 [3]	°C
Storage Temperature Under Bias	T_{BIAS}	-10 to +80	°C

Notes: 1. Relative to V_{SS}.
2. HN27512G.
3. HN27512P.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	4	6	pF	V_{IN} = 0V, all pins except $\overline{OE}/V_{PP}$
Output Capacitance	C_{OUT}	8	12	pF	V_{OUT} = 0V

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	10	µA	V_{IN} = 0 V to V_{CC}
Output Leakage Current	I_{LO}	-	-	10	µA	V_{OUT} = 0 V to V_{CC}
Operating V_{CC} Current	I_{CC}	-	45	100	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
Standby V_{CC} Current	I_{SB}	-	-	40	mA	$\overline{CE}$ = V_{IH}
Input Voltage	V_{IH}	2.2	-	V_{CC} + 1 [2]	V	
	V_{IL}	-0.1 [1]	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = 1.0 mA
	V_{OL}	-	-	0.45	V	I_{OL} = 2.1 mA

Notes: 1. V_{IL} min = -0.6 V for pulse width ≤ 20 ns.
2. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns.
If V_{IH} is over the specified maximum value, Read operation can not be guaranteed.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, T_a = 0 to 70°C)

Test Conditions

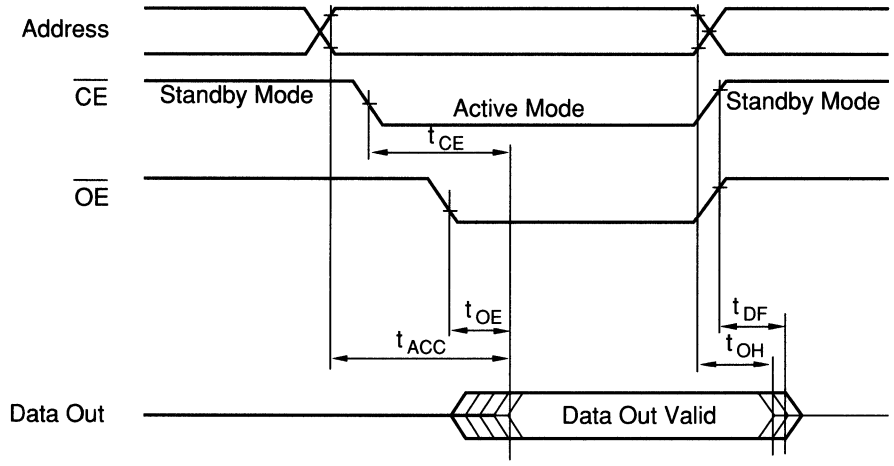
- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 20 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V / 2.0 V

Item	Symbol	-25 Min.	-25 Max.	-30 Min.	-30 Max.	Unit	Test Condition
Address Access Time	t_{ACC}	-	250	-	300	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
Chip Enable Access Time	t_{CE}	-	250	-	300	ns	$\overline{OE}$ = V_{IL}
Output Enable Access Time	t_{OE}	-	100	-	120	ns	$\overline{CE}$ = V_{IL}
Output Disable to High-Z [1]	t_{DF}	0	60	0	105	ns	$\overline{CE}$ = V_{IL}
Output Hold to Address Change	t_{OH}	0	-	0	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

4

■ READ TIMING WAVEFORM



(TD.R.HN27512)

■ DC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

(V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, T_a = 25 °C ± 5 °C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	10	µA	V_{IN} = 5.25 V
Operating V_{CC} Current	I_{CC}	-	-	100	mA	
Operating V_{PP} Current	I_{PP}	-	35	50	mA	$\overline{CE}$ = V_{IL}
Input Voltage [1]	V_{IH}	2.0	-	V_{CC} +.5 [2]	V	
	V_{IL}	- 0.1[1]	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA
	V_{OL}	-	-	0.45	V	I_{OH} = 2.1 mA

Notes: 1. V_{IL} min = -0.6 V for pulse width ≤ 20 ns.
2. If V_{IH} is over the specified maximum value, programming operation can not be guaranteed.

■ AC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

(V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 v ± 0.5 V, T_a = 25°C ± 5°C)

Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 20 ns
- Reference levels for measuring timing: 0.8 V / 2.0V

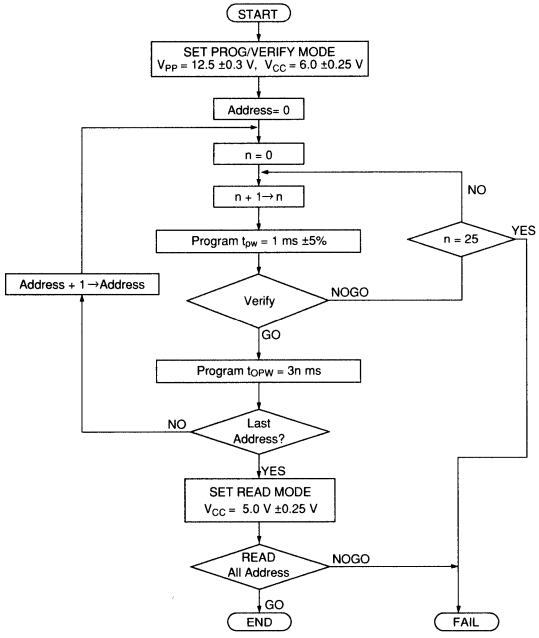
Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	2	-	-	µs	
Address Hold Time	t_{AH}	0	-	-	µs	
Data Setup Time	t_{DS}	2	-	-	µs	
V_{PP} Setup Time	t_{VPS}	2	-	-	µs	
V_{CC} Setup Time	t_{VCS}	2	-	-	µs	
Output Enable Hold Time	t_{OEH}	2	-	-	µs	
Output Disable Time	t_{DF}	0	-	130	ns	
$\overline{CE}$ Initial Programming Pulse Width	t_{PW}	0.95	1.0	1.05	ms	
$\overline{CE}$ Overprogramming Pulse Width	t_{OPW}	2.85	-	78.75	ms	
Data Hold Time	t_{DH}	2	-	-	µs	
V_{PP} Recovery Time	t_{VR}	2	-	-	µs	
Data Valid from Chip Enable	t_{DV}	-	-	1	µs	

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

4

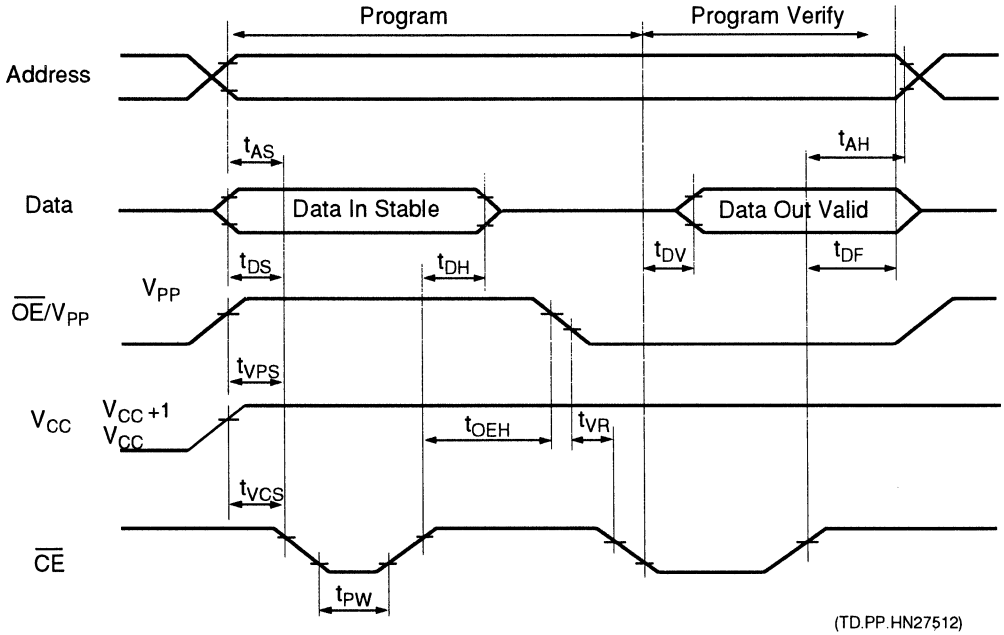
■ HIGH PERFORMANCE PROGRAMMING FLOWCHART

The Hitachi HN27512 can be programmed with the High Performance Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.



(FC.P.HN27512)

■ HIGH PERFORMANCE PROGRAMMING TIMING WAVEFORM



(TD.PP.HN27512)

HITACHI

Hitachi America, Ltd. • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

■ ERASING THE HN27512

The Hitachi HN27512 Ceramic DIP package allows the device to be erased by exposure to ultraviolet light of 2537Å. All of the data is changed to "1" after this erasure procedure. The minimum integrated dose (UV intensity x exposure time) for erasure is 15 W-sec/cm^2.

■ DEVICE IDENTIFIER MODE DESCRIPTION

The Device Identifier Mode allows binary codes to be read from the outputs that identify the manufacturer and the type of device. Using this mode with programming equipment, the device will automatically match its own erase and programming algorithm.

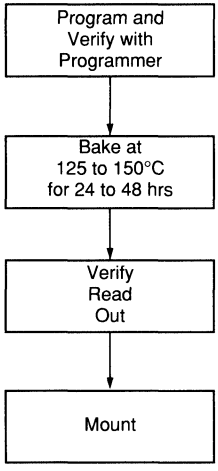
■ HN27512 SERIES IDENTIFIER CODE

Identifier	A_0	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	1	0	0	1	0	1	0	0	94

Notes: 1. $A_9 = 12.0\ V \pm 0.5V$
3. A_1-A_8, A_{10}-A_{15}, $\overline{CE}$, $\overline{OE}/V_{PP} = V_{IL}$

■ HN27512P RECOMMENDED SCREENING CONDITIONS

Before mounting the HN27512P package, please make the following screening (baking without bias) shown below:



(RSC.EPROM)

4

HN27C1024H Series

1M (64K x 16-bit) UV and OTP EPROM

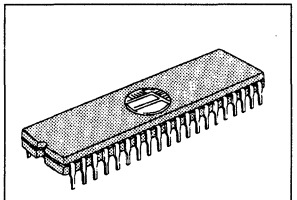
■ DESCRIPTION

The Hitachi HN27C1024H is a 1-Megabit Ultraviolet Erasable and One-Time Programmable Electrically Programmable Read Only Memory organized as 65,536 x 16-bits.

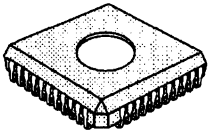
The HN27C1024H features fast address access times of 85, 100, 120 and 150 ns and low power dissipation. This combination makes the HN27C1024H suitable for high speed 16 and 32-bit microcomputer systems. The HN27C1024H offers high speed programming using page programming mode.

Hitachi's HN27C1024H is offered in JEDEC-Standard Word-Wide EPROM pinouts in 40-pin Ceramic DIP and 44-lead Ceramic and Plastic LCC packages. This allows socket replacement with Mask ROMs.

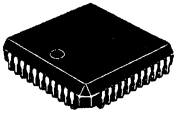
The Ceramic DIP and Ceramic LCC packages are erasable by exposure to Ultraviolet light. The PLCC packaged device is One-Time Programmable and once programmed, can not be rewritten.



(DG-40A)



(CC-44)



(CP-44)

■ FEATURES

- Fast Access Times:
  85 ns/100 ns/120 ns/150 ns (max)
- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Low Power Dissipation:
  Active Mode: 60 mW/MHz (typ)
  Standby Mode: 25 mA (max)
- High Speed Page and Word Programming:
  Page Programming Time: 14 sec (typ)
- Programming Power Supply:
  V_{PP} = 12.5 V ± 0.3 V
- Pin Arrangement:
  JEDEC Standard Word-Wide EPROM
  Mask ROM Compatible
- Packages:
  40-pin Ceramic DIP
  44-lead Ceramic LCC
  44-lead PLCC

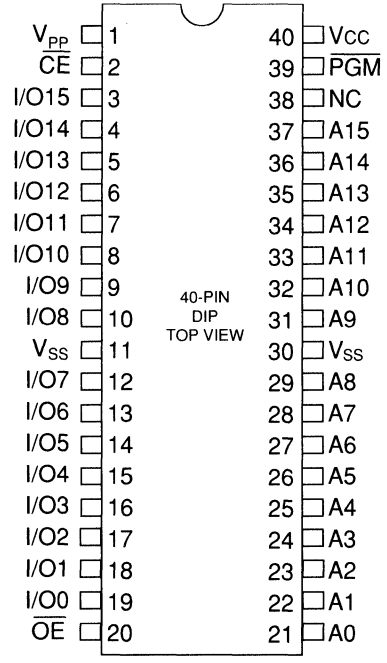
■ ORDERING INFORMATION

Type No.	Access Time	Package
HN27C1024HG-85	85 ns	40-pin Ceramic DIP (DG-40A)
HN27C1024HG-10	100 ns	
HN27C1024HG-12	120 ns	
HN27C1024HG-15	150 ns	
HN27C1024HCC-85	85 ns	44-lead Ceramic LCC (CC-44)
HN27C1024HCC-10	100 ns	
HN27C1024HCC-12	120 ns	
HN27C1024HCC-15	150 ns	
HN27C1024HCP-10	100 ns	44-lead PLCC (CP-44)
HN27C1024HCP-12	120 ns	
HN27C1024HCP-15	150 ns	

Hitachi America, Ltd. • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

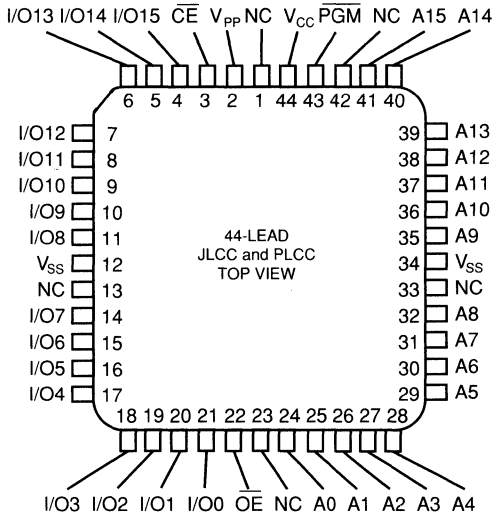
■ PIN ARRANGEMENT

HN27C1024HG Series



(PinD40.HN27C1024H)

HN27C1024HCC Series
HN27C1024HCP Series



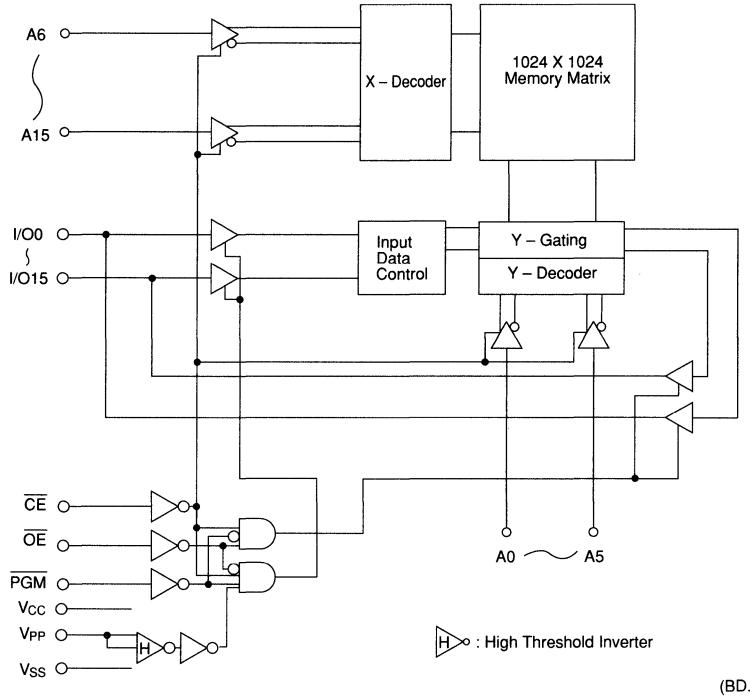
(PinQ44.HN27C1024H)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{15}	Address
I/O_0 - I/O_{15}	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{PP}	Programming Supply
V_{SS}	Ground
$\overline{PGM}$	Programming Enable
NC	No Connection

4

■ BLOCK DIAGRAM



(BD.HN27C1024H)

■ MODE SELECTION

Mode	V_{PP}	V_{CC}	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	I/O
Read	V_{CC}	V_{CC}	V_{IL}	V_{IL}	V_{IH}	X[1]	D_{OUT}
Output Disable	V_{CC}	V_{CC}	V_{IL}	V_{IH}	V_{IH}	X	High-Z
Standby	V_{CC}	V_{CC}	V_{IH}	X	X	X	High-Z
Program	V_{PP}	V_{CC}	V_{IL}	V_{IH}	V_{IL}	X	D_{IN}
Program Verify	V_{PP}	V_{CC}	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}
Page Data Latch	V_{PP}	V_{CC}	V_{IH}	V_{IL}	V_{IH}	X	D_{IN}
Page Program	V_{PP}	V_{CC}	V_{IH}	V_{IH}	V_{IL}	X	High-Z
Program Inhibit	V_{CC}	V_{CC}	V_{IL}	V_{IL}	V_{IL}	X	High-Z
	V_{PP}	V_{CC}	V_{IL}	V_{IH}	V_{IH}	X	High-Z
	V_{PP}	V_{CC}	V_{IH}	V_{IL}	V_{IL}	X	High-Z
	V_{PP}	V_{CC}	V_{IH}	V_{IH}	V_{IH}	X	High-Z
Identifier	V_{CC}	V_{CC}	V_{IL}	V_{IL}	V_{IH}	V_H	ID

Notes: 1. X = Don't Care. $V_{PP} = 0$ V to V_{CC}.
2. $11.5\ V \leq V_H \leq 12.5\ V$

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Programming Voltage [1]	V_{PP}	-0.6 to +13.5	V
All Input and Output Voltage [1,2]	V_{IN}, V_{OUT}	-0.6 to +7.0	V
A_9 and $\overline{OE}$ Voltage [2]	V_{ID}	-0.6 to +13.0	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range [3]	T_{STG}	-65 to +125 [4] -55 to +125 [5]	°C
Storage Temperature Under Bias	T_{BIAS}	0 to +80	°C

Notes: 1. Relative to V_{SS}.
2. V_{IN}, V_{OUT}, and V_{ID} min = -2.0V for pulse width ≤ 20 ns.
3. Device storage temperature range before programming.
4. HN27C1024HG and HN27C1024HCC.
5. HN27C1024HCP.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	HN27C1024HG/HCC		HN27C1024HCP		Unit	Test Condition
		Min.	Max.	Min.	Max.		
Input Capacitance	C_{IN}	-	12	-	6	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	-	15	-	12	pF	V_{OUT} = 0V

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{IN} = 5.5 V
Output Leakage Current	I_{LO}	-	-	2	µA	V_{OUT} = 5.5 V/0.45 V
Operating V_{CC} Current	I_{CC1}	-	-	50	mA	I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}
	I_{CC2}	-	-	100	mA	I_{OUT} = 0 mA, f = 10 MHz
	I_{CC3}	-	-	25	mA	I_{OUT} = 0 mA, f = 1 MHz
Standby V_{CC} Current	I_{SB}	-	-	25	mA	$\overline{CE}$ = V_{IH}
V_{PP} Current	I_{PP1}	-	1	20	µA	V_{PP} = 5.5 V
Input Voltage	V_{IH}	2.2	-	V_{CC} + 1 [2]	V	
	V_{IL}	-0.3 [1]	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA
	V_{OL}	-	-	0.45	V	I_{OL} = 2.1 mA

Notes: 1. V_{IL} min = -1.0 V for pulse width ≤ 50 ns.
2. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns.
If V_{IH} is over the specified maximum value, Read operation can not be guaranteed.

4

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

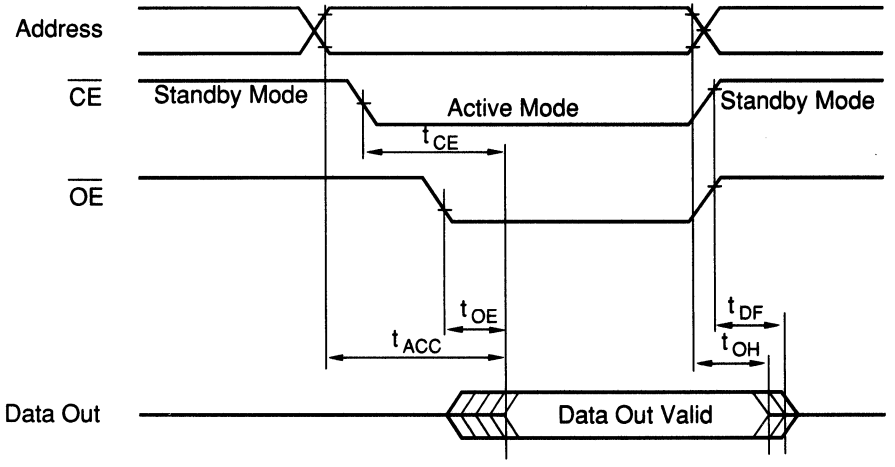
Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V/2.0 V

Item	Symbol	-85		-10		-12		-15		Unit	Test Condition
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Address Access Time	t_{ACC}	-	85	-	100	-	120	-	150	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
Chip Enable Access Time	t_{CE}	-	85	-	100	-	120	-	150	ns	$\overline{OE}$ = V_{IL}
Output Enable Access Time	t_{OE}	-	45	-	50	-	60	-	60	ns	$\overline{CE}$ = V_{IL}
Output Disable to High-Z [1]	t_{DF}	0	30	0	50	0	50	0	50	ns	$\overline{CE}$ = V_{IL}
Output Hold to Address Change	t_{OH}	0	-	0	-	0	-	0	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



(TD.R.HN27C1024H)

■ DC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

(V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, T_a = 25 °C ± 5 °C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{IN} = 6.5 V/ 0.45 V
Operating V_{CC} Current	I_{CC}	-	-	50	mA	
Operating V_{PP} Current	I_{PP}	-	-	40	mA	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}
Input Voltage [3]	V_{IH}	2.2	-	V_{CC} +.5 [6]	V	
	V_{IL}	- 0.1[5]	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA
	V_{OL}	-	-	0.45	V	I_{OH} = 2.1 mA

Notes:
1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13 V, including overshoot.
3. Device reliability may be adversely affected if the device is installed or removed while V_{PP} = 12.5 V.
4. Do not change V_{PP} from V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = low.
5. V_{IL} min = -0.6 V for pulse width ≤ 20 ns.
6. If V_{IH} is over the specified maximum value, programming operation can not be guaranteed.

4

■ AC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

(V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.5 v ± 0.3 V, T_a = 25°C ± 5°C)

Test Conditions

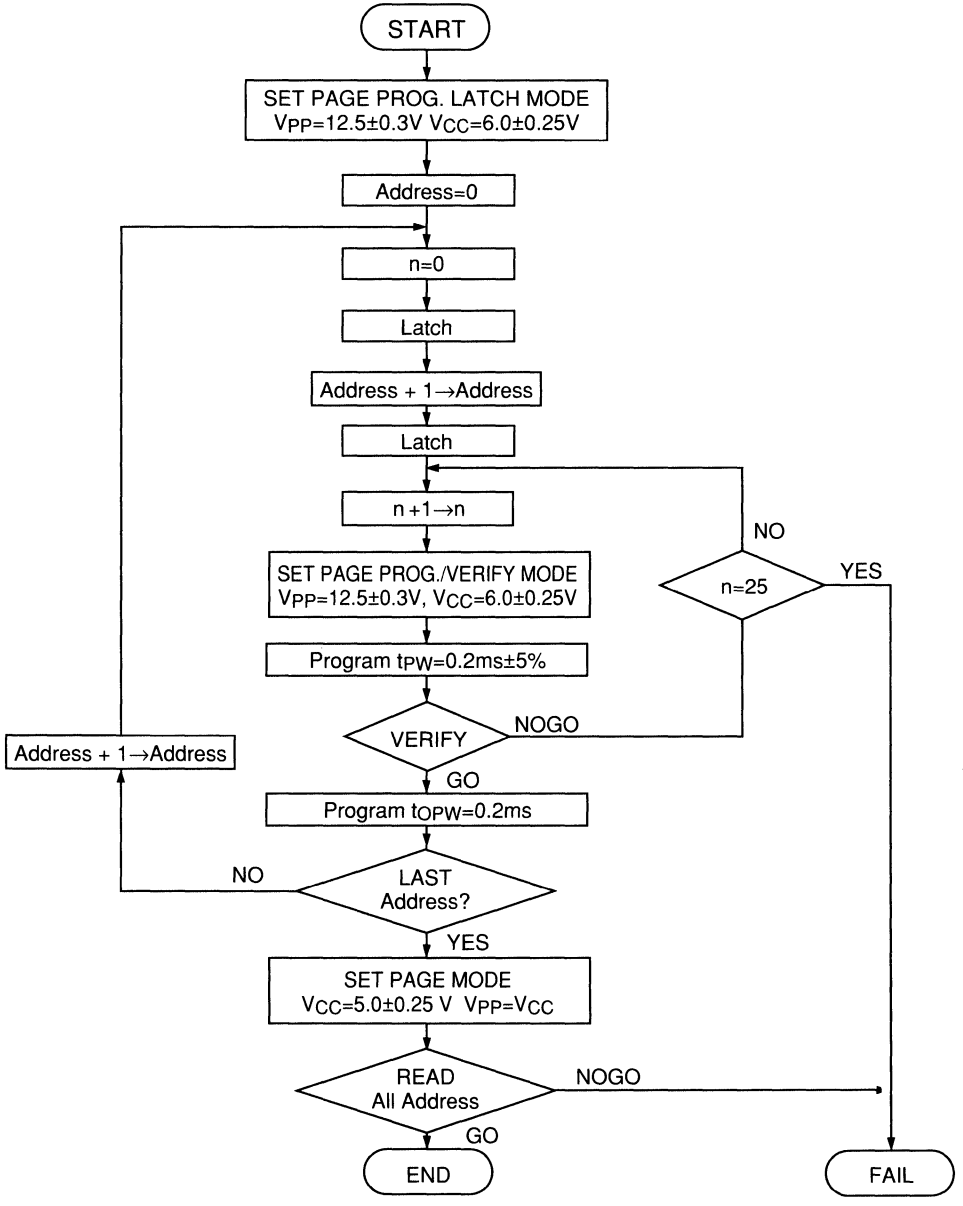
- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 20 ns
- Reference levels for measuring timing: 0.8 V / 2.0V

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	2	-	-	µs	
Address Hold Time	t_{AH}	0	-	-	µs	
Data Setup Time	t_{DS}	2	-	-	µs	
Data Hold Time	t_{DH}	2	-	-	µs	
Chip Enable Setup Time	t_{CES}	2	-	-	µs	
V_{PP} Setup Time	t_{VPS}	2	-	-	µs	
V_{CC} Setup Time	t_{VCS}	2	-	-	µs	
Output Enable Setup Time	t_{OES}	2	-	-	µs	
Output Disable Time	t_{DF}	0	-	130	ns	
$\overline{PGM}$ Initial Programming Pulse Width	t_{PW}	0.19	0.20	0.21	ms	
$\overline{PGM}$ Overprogramming Pulse Width	t_{OPW}	0.19	-	5.25	ms	
Data Valid from Output Enable Time	t_{OE}	0	-	150	ns	
Output Enable Pulse During Data Latch	t_{LW}	1	-	-	µs	
Output Enable Hold Time	t_{OEH}	2	-	-	µs	
Chip Enable Hold Time	t_{CEH}	2	-	-	µs	
$\overline{PGM}$ Setup Time	t_{PGMS}	2	-	-	µs	

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

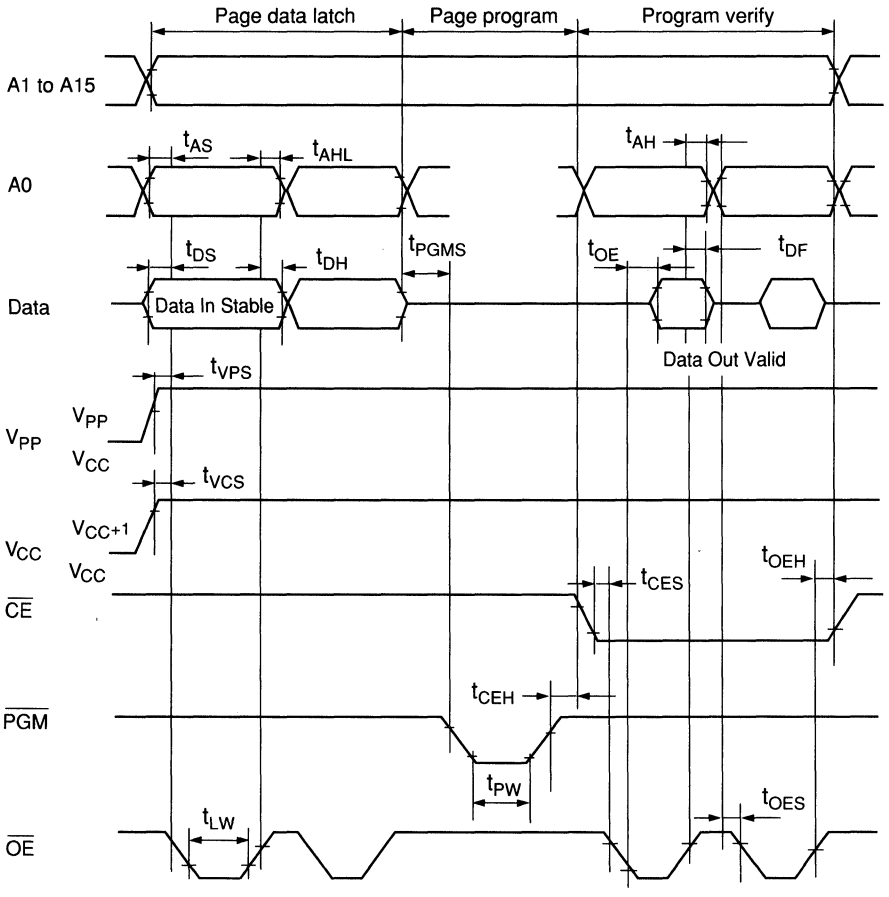
■ PAGE PROGRAMMING FLOWCHART

The Hitachi HN27C1024H can be programmed with the high performance Page Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.



(FC.PP.HN27C1024H)

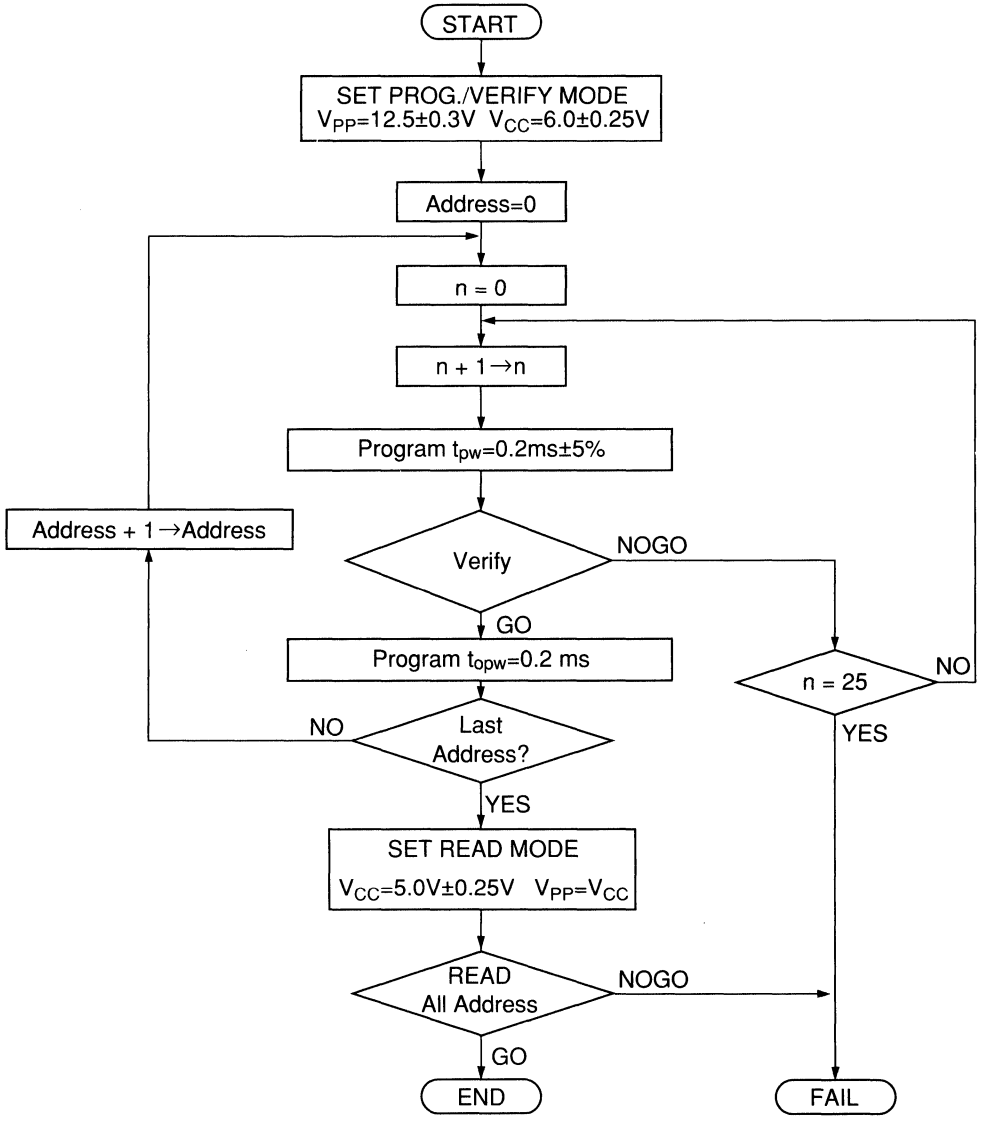
■ PAGE PROGRAMMING TIMING WAVEFORM



(TD.PP.HN27C1024H)

■ WORD PROGRAMMING FLOWCHART

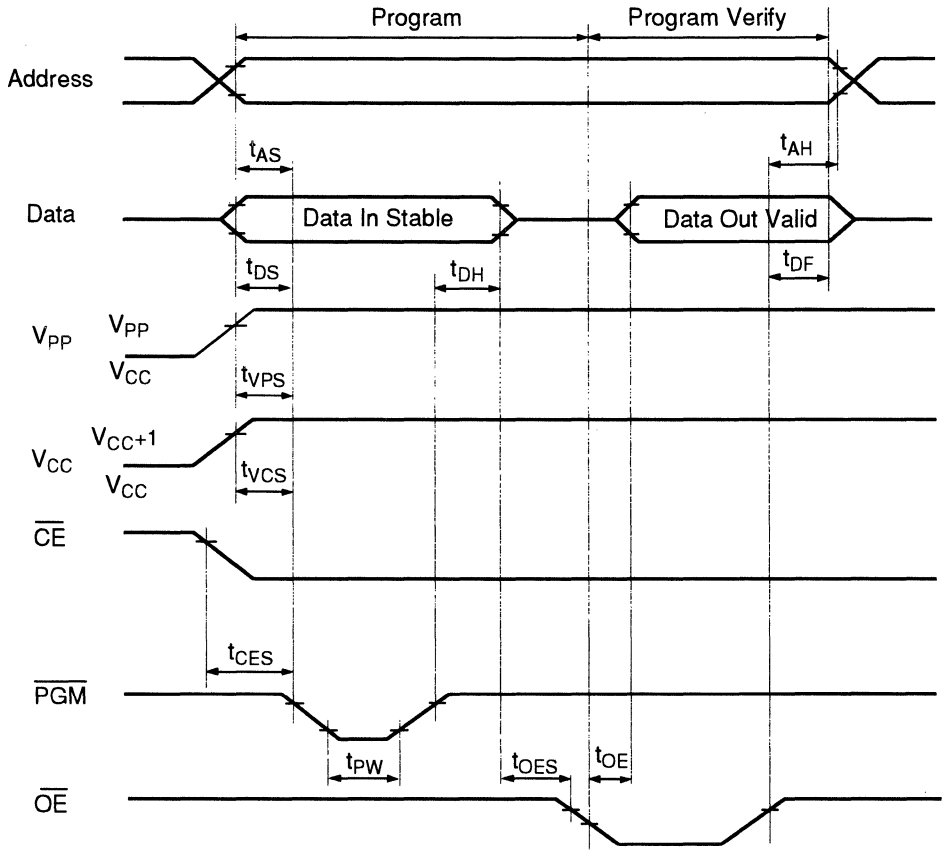
The Hitachi HN27C1024H can be programmed with the high performance Word Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.



(FC.P.HN27C1024H)

4

■ WORD PROGRAMMING TIMING WAVEFORM



(TD.P.HN27C1024H)

■ ERASING THE HN27C1024H

The Hitachi HN27C1024H Ceramic DIP and Ceramic LCC packages allow these devices to be erased by exposure to ultraviolet light of 2537Å. All of the data is changed to "1" after this erasure procedure. The minimum integrated dose (UV intensity x exposure time) for erasure is 15 W-sec/cm^2.

■ DEVICE IDENTIFIER MODE DESCRIPTION

The Device Identifier Mode allows binary codes to be read from the outputs that identify the manufacturer and the type of device. Using this mode with programming equipment, the device will automatically match its own erase and programming algorithm.

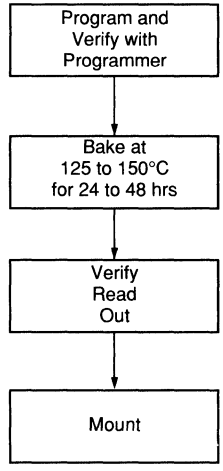
■ HN27C1024H SERIES IDENTIFIER CODE

Identifier	A_0	I/O_8-I/O_{15}	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Hex Data
Manufacturer Code	V_{IL}	X	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	X	1	0	1	1	1	0	1	0	BA

Notes: 1. V_{CC} = 5.0 V ± 10%
2. A_9 = 12.0 V ± 0.5V
3. A_1-A_8, A_{10}-A_{15}, $\overline{CE}$, $\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}
4. X = Don't Care

■ HN27C1024HCP RECOMMENDED SCREENING CONDITIONS

Before mounting the HN27C1024HCP package, please make the following screening (baking without bias) shown below:



(RSC.EPROM)

4

HN27C101A Series

1M (128K x 8-bit) UV and OTP EPROM

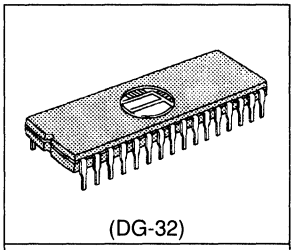
■ DESCRIPTION

The Hitachi HN27C101A is a 1-Megabit Ultraviolet Erasable and One-Time Programmable Electrically Programmable Read Only Memory organized as 131,072 x 8-bits.

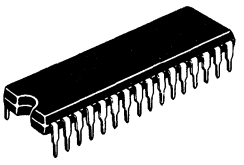
The HN27C101A features fast address access times and low power dissipation. This combination makes the HN27C101A suitable for high speed microcomputer systems. The HN27C101A offers high speed programming using page programming mode.

Hitachi's HN27C101A is offered in JEDEC-Standard Byte-Wide EPROM pinouts in 32-pin Ceramic and Plastic DIP and 32-lead Plastic SOP and TSOP packages. This allows socket replacement with Flash Memory and Mask ROMs. The HN27C101A TSOP package is offered in both standard and reverse bend pinouts.

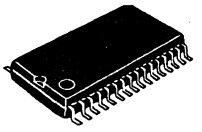
The Ceramic DIP package is erasable by exposure to Ultraviolet light. The Plastic DIP, SOP and TSOP packaged devices are One-Time Programmable and once programmed, can not be rewritten.



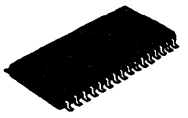
(DG-32)



(DP-32)



(FP-32D)



(TTP-32D) and (TTP-32DR)

■ FEATURES

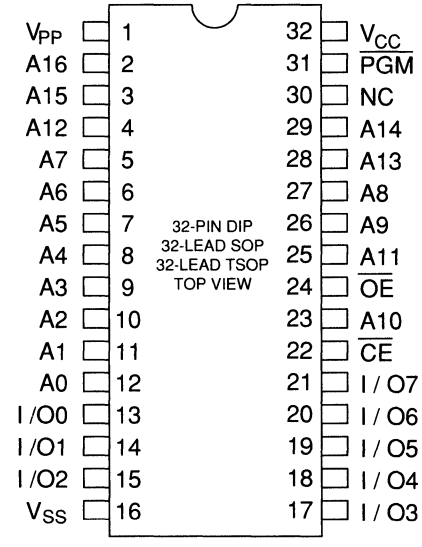
- Fast Access Times:
  100 ns/120 ns/150 ns/200 ns (max)
- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Low Power Dissipation:
  Active Mode: 50 mW/MHz (typ)
  Standby Mode: 5 µW (typ)
- High Speed Page and Word Programming:
  Page Programming Time: 14 sec (typ)
- Programming Power Supply:
  V_{PP} = 12.5 V ± 0.3 V
- Pin Arrangement:
  JEDEC Standard Byte-Wide EPROM
  Flash Memory and Mask ROM Compatible
- Packages:
  32-pin Ceramic DIP
  32-pin Plastic DIP
  32-lead Plastic SOP
  32-lead Plastic TSOP (Type II)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN27C101AG-10	100 ns	32-pin Ceramic DIP (DG-32)
HN27C101AG-12	120 ns	
HN27C101AG-15	150 ns	
HN27C101AG-20	200 ns	
HN27C101AP-12	120 ns	32-pin Plastic DIP (DP-32)
HN27C101AP-15	150 ns	
HN27C101AP-20	200 ns	
HN27C101AFP-12	120 ns	32-lead Plastic SOP (FP-32D)
HN27C101AFP-15	150 ns	
HN27C101AFP-20	200 ns	
HN27C101ATT-12	120 ns	32-lead Plastic TSOP (TTP-32D)
HN27C101ATT-15	150 ns	
HN27C101ATT-20	200 ns	
HN27C101ARR-12	120 ns	32-lead Plastic TSOP (TTP-32DR) Reverse bend
HN27C101ARR-15	150 ns	
HN27C101ARR-20	200 ns	

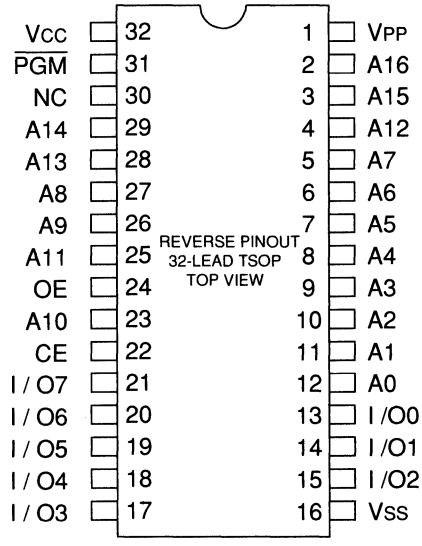
■ PIN ARRANGEMENT

HN27C101AG/P Series
HN27C101AFP Series
HN27C101ATT Series



(PinD32.HN27C101A)

HN27C101ARR Series

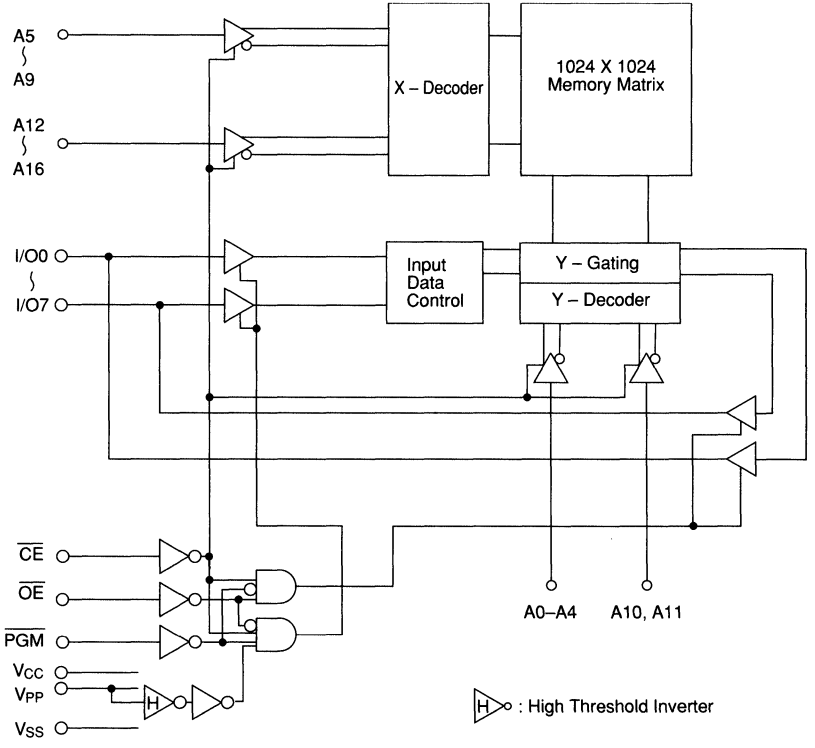


(PinT2.HN27C101A)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{16}	Address
I/O_0 - I/O_7	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{PP}	Programming Supply
V_{SS}	Ground
$\overline{PGM}$	Programming Enable
NC	No Connection

■ BLOCK DIAGRAM



(BD.HN27C101A)

■ MODE SELECTION

Mode	V_{PP}	V_{CC}	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	I/O
Read	V_{CC}	V_{CC}	V_{IL}	V_{IL}	V_{IH}	X[1]	D_{OUT}
Output Disable	V_{CC}	V_{CC}	V_{IL}	V_{IH}	V_{IH}	X	High-Z
Standby	V_{CC}	V_{CC}	V_{IH}	X	X	X	High-Z
Program	V_{PP}	V_{CC}	V_{IL}	V_{IH}	V_{IL}	X	D_{IN}
Program Verify	V_{PP}	V_{CC}	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}
Page Data Latch	V_{PP}	V_{CC}	V_{IH}	V_{IL}	V_{IH}	X	D_{IN}
Page Program	V_{PP}	V_{CC}	V_{IH}	V_{IH}	V_{IL}	X	High-Z
Program Inhibit	V_{CC}	V_{CC}	V_{IL}	V_{IL}	V_{IL}	X	High-Z
	V_{PP}	V_{CC}	V_{IL}	V_{IH}	V_{IH}	X	High-Z
	V_{PP}	V_{CC}	V_{IH}	V_{IL}	V_{IL}	X	High-Z
	V_{PP}	V_{CC}	V_{IH}	V_{IH}	V_{IH}	X	High-Z
Identifier	V_{CC}	V_{CC}	V_{IL}	V_{IL}	V_{IH}	V_H	ID

Notes: 1. X = Don't Care. V_{PP} = 0 V to V_{CC}.
2. 11.5 V ≤ V_H ≤ 12.5 V

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Programming Voltage [1]	V_{PP}	-0.6 to +13.5	V
All Input and Output Voltage [1,2]	V_{IN}, V_{OUT}	-0.6 to +7.0	V
A_9 and $\overline{OE}$ Voltage [2]	V_{ID}	-0.6 to +13.0	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-65 to +125[3] -55 to +125[4]	°C
Storage Temperature Under Bias	T_{BIAS}	0 to +80	°C

Notes: 1. Relative to V_{SS}.
2. V_{IN}, V_{OUT}, and V_{ID} min = -1.0V for pulse width ≤ 20 ns.
3. HN27C101AG.
4. HN27C101AP, HN27C101AFP, HN27C101ATT and HN27C101ARR.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	-	10	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	-	15	pF	V_{OUT} = 0V

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{IN} = 5.5 V
Output Leakage Current	I_{LO}	-	-	2	µA	V_{OUT} = 5.5 V/0.45 V
Operating V_{CC} Current	I_{CC1}	-	-	30	mA	I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}
	I_{CC2}	-	-	30	mA	I_{OUT} = 0 mA, f = 5 MHz
	I_{CC3}	-	-	50	mA	I_{OUT} = 0 mA, f = 10 MHz
Standby V_{CC} Current	I_{SB}	-	-	1	mA	$\overline{CE}$ = V_{IH}
V_{PP} Current	I_{PP1}	-	1	20	µA	V_{PP} = 5.5 V
Input Voltage	V_{IH}	2.2	-	V_{CC} + 1 [2]	V	
	V_{IL}	-0.3 [1]	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA
	V_{OL}	-	-	0.45	V	I_{OL} = 2.1 mA

Notes: 1. V_{IL} min = -1.0 V for pulse width ≤ 50 ns.
2. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns.
If V_{IH} is over the specified maximum value, Read operation can not be guaranteed.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

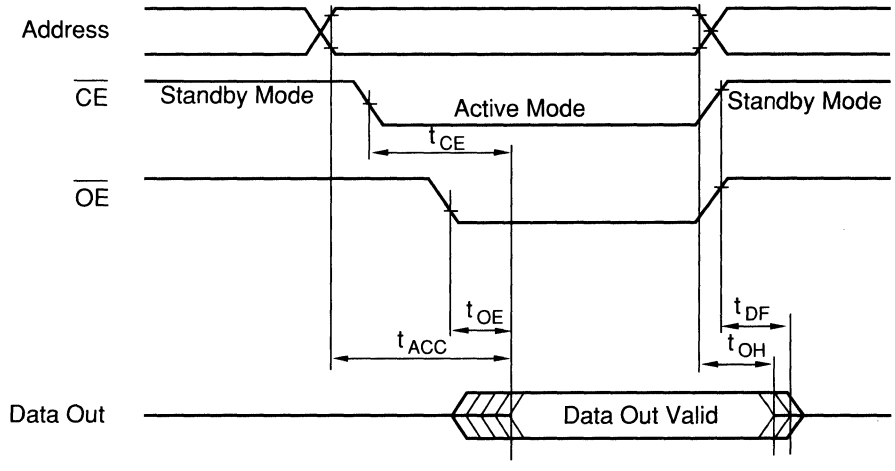
Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V/2.0 V

Item	Symbol	-10		-12		-15		-20		Unit	Test Condition
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Address Access Time	t_{ACC}	-	100	-	120	-	150	-	200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
Chip Enable Access Time	t_{CE}	-	100	-	120	-	150	-	200	ns	$\overline{OE}$ = V_{IL}
Output Enable Access Time	t_{OE}	-	60	-	60	-	70	-	70	ns	$\overline{CE}$ = V_{IL}
Output Disable to High-Z [1]	t_{DF}	0	50	0	50	0	50	0	50	ns	$\overline{CE}$ = V_{IL}
Output Hold to Address Change	t_{OH}	0	-	0	-	0	-	0	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



(TD.R.HN27C101A)

■ DC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

(V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, T_a = 25 °C ± 5 °C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{IN} = 0 V to V_{CC}
Operating V_{CC} Current	I_{CC}	-	-	30	mA	
Operating V_{PP} Current	I_{PP}	-	-	40	mA	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}
Input Voltage [3]	V_{IH}	2.2	-	V_{CC} +.5 [6]	V	
	V_{IL}	- 0.1[5]	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA
	V_{OL}	-	-	0.45	V	I_{OH} = 2.1 mA

Notes:
1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13 V, including overshoot.
3. Device reliability may be adversely affected if the device is installed or removed while V_{PP} = 12.5 V.
4. Do not change V_{PP} from V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = low.
5. V_{IL} min = -0.6 V for pulse width ≤ 20 ns.
6. If V_{IH} is over the specified maximum value, programming operation can not be guaranteed.

4

■ AC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

(V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.5 v ± 0.3 V, T_a = 25°C ± 5°C)

Test Conditions

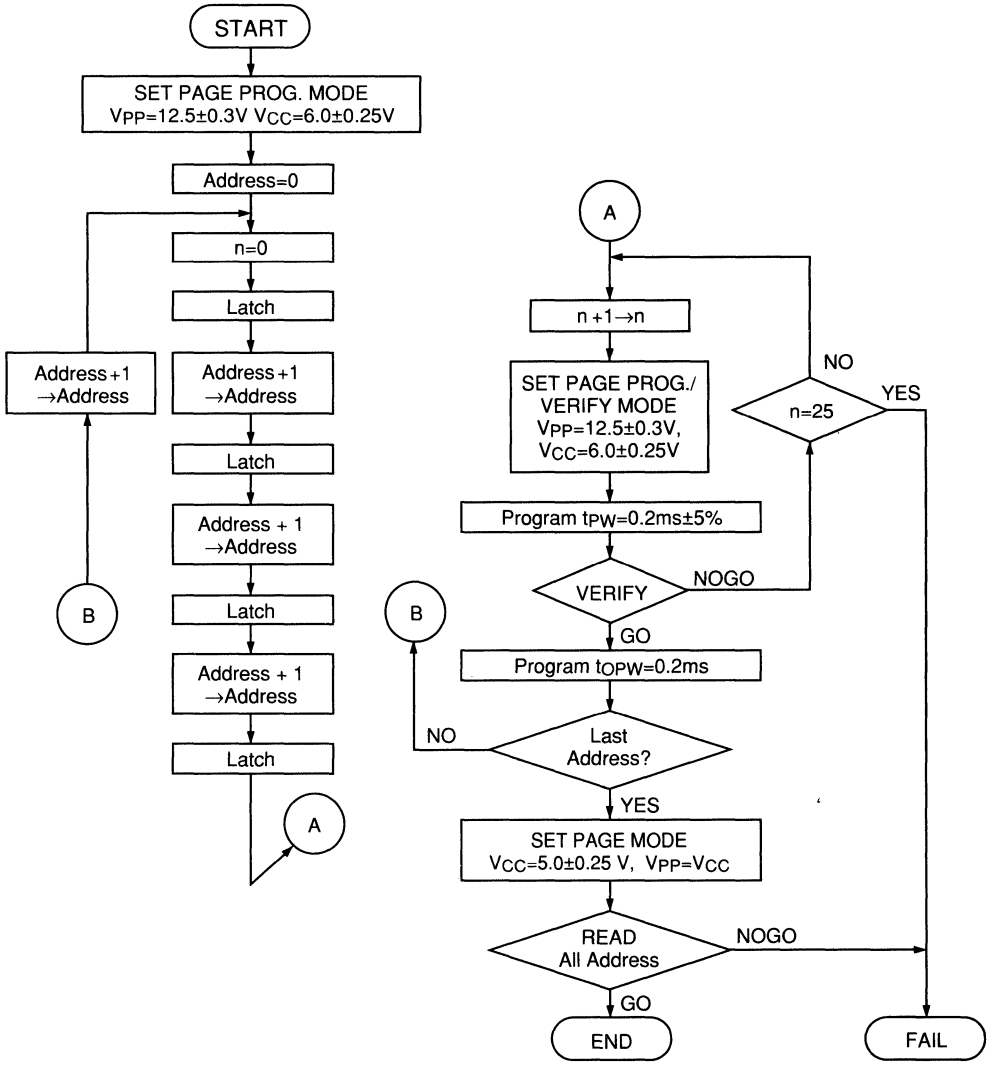
- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 20 ns
- Reference levels for measuring timing: 0.8 V / 2.0V

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	2	-	-	µs	
Address Hold Time	t_{AH}	0	-	-	µs	
Data Setup Time	t_{DS}	2	-	-	µs	
Data Hold Time	t_{DH}	2	-	-	µs	
Chip Enable Setup Time	t_{CES}	2	-	-	µs	
V_{PP} Setup Time	t_{VPS}	2	-	-	µs	
V_{CC} Setup Time	t_{VCS}	2	-	-	µs	
Output Enable Setup Time	t_{OES}	2	-	-	µs	
Output Disable Time	t_{DF}	0	-	130	ns	
$\overline{PGM}$ Initial Programming Pulse Width	t_{PW}	0.19	0.20	0.21	ms	
$\overline{PGM}$ Overprogramming Pulse Width	t_{OPW}	0.19	-	5.25	ms	
Data Valid from Output Enable Time	t_{OE}	0	-	150	ns	
Output Enable Pulse During Data Latch	t_{LW}	1	-	-	µs	
Output Enable Hold Time	t_{OEH}	2	-	-	µs	
Chip Enable Hold Time	t_{CEH}	2	-	-	µs	
$\overline{PGM}$ Setup Time	t_{PGMS}	2	-	-	µs	

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

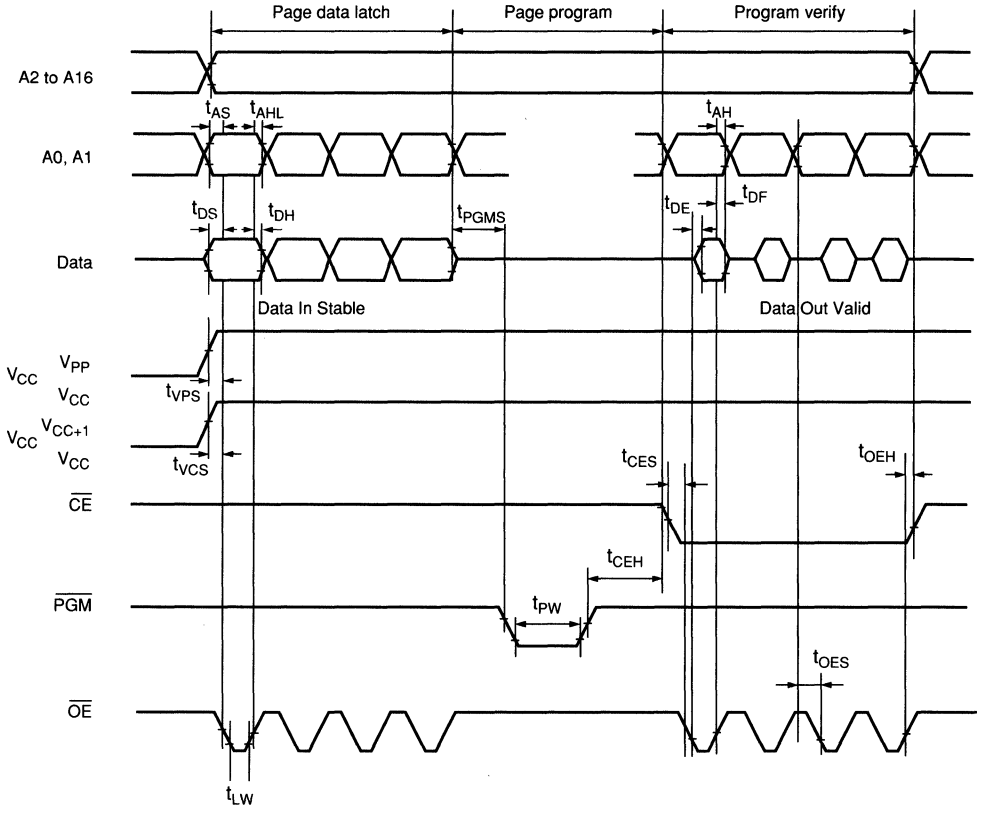
■ PAGE PROGRAMMING FLOWCHART

The Hitachi HN27C101A can be programmed with the high performance Page Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.



(FC.PP.HN27C101A)

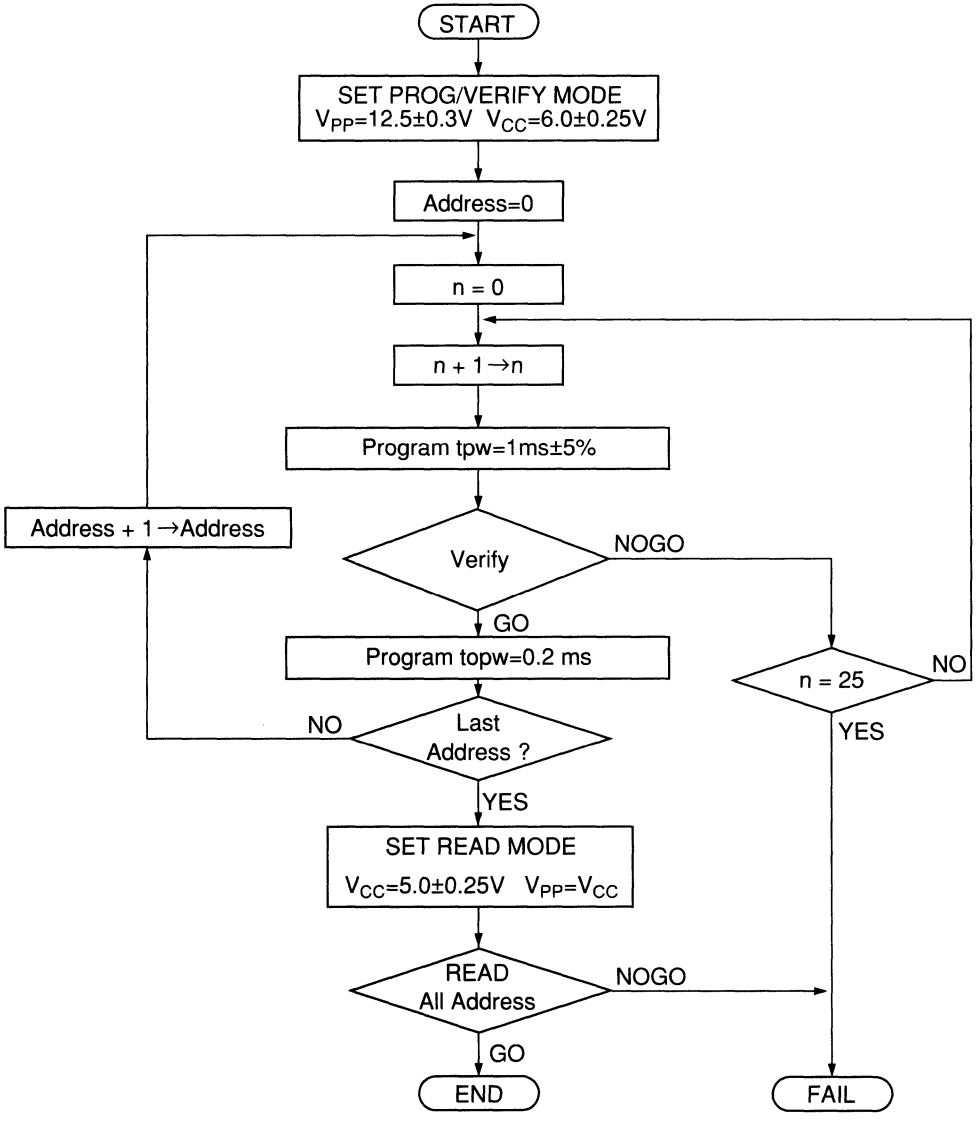
■ PAGE PROGRAMMING TIMING WAVEFORM



(TD.PP.HN27C101A)

■ BYTE PROGRAMMING FLOWCHART

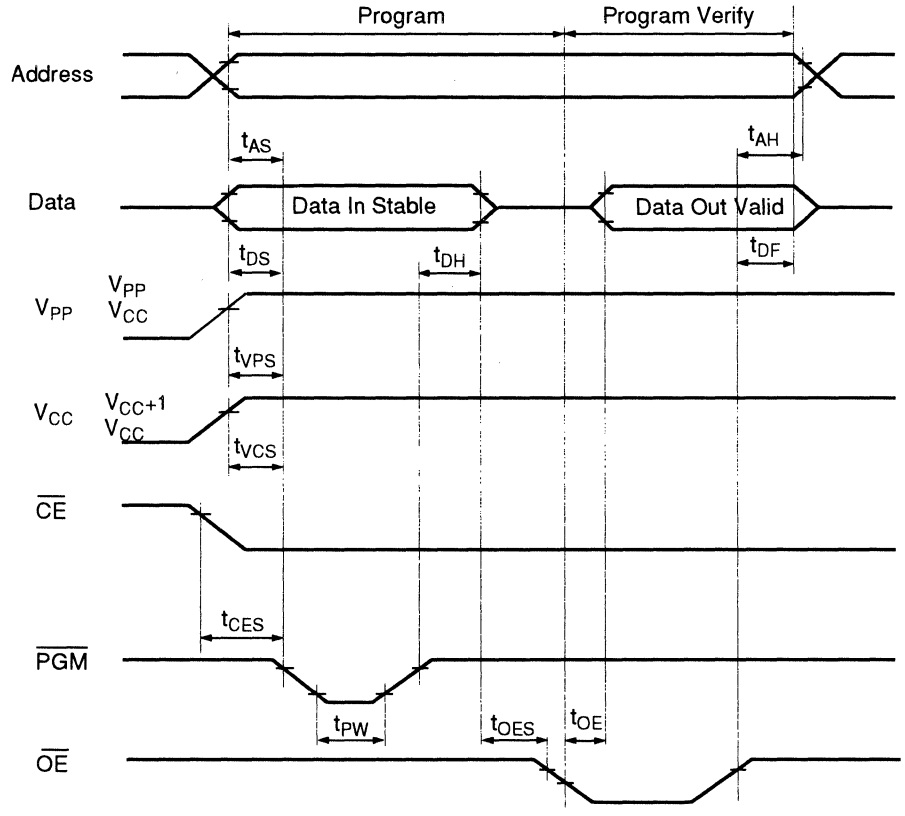
The Hitachi HN27C101A can be programmed with the high performance Byte Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.



(FC.P.HN27C101A)

4

■ BYTE PROGRAMMING TIMING WAVEFORM



(TD.P.HN27C101A)

Hitachi America, Ltd. • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

■ ERASING THE HN27C101A

The Hitachi HN27C101A Ceramic DIP package allow the device to be erased by exposure to ultraviolet light of 2537Å. All of the data is changed to "1" after this erasure procedure. The minimum integrated dose (UV intensity x exposure time) for erasure is 15 W-sec/cm^2.

■ DEVICE IDENTIFIER MODE DESCRIPTION

The Device Identifier Mode allows binary codes to be read from the outputs that identify the manufacturer and the type of device. Using this mode with programming equipment, the device will automatically match its own erase and programming algorithm.

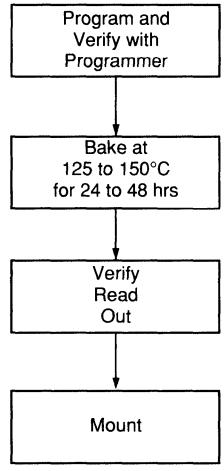
■ HN27C101A SERIES IDENTIFIER CODE

Identifier	A_0	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	0	0	1	1	1	0	0	0	38

Notes: 1. $V_{CC} = 5.0\ V \pm 10\%$
2. $A_9 = 12.0\ V \pm 0.5V$
3. A_1-A_8, A_{10}-A_{16}, $\overline{CE}$, $\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$
4. X = Don't Care

■ HN27C101AP/FP/TT/RR RECOMMENDED SCREENING CONDITIONS

Before mounting the HN27C101A plastic packages, please make the following screening (baking without bias) shown below:



(RSC.EPROM)

4

HN27C301A Series

1M (128K x 8-bit) UV and OTP EPROM

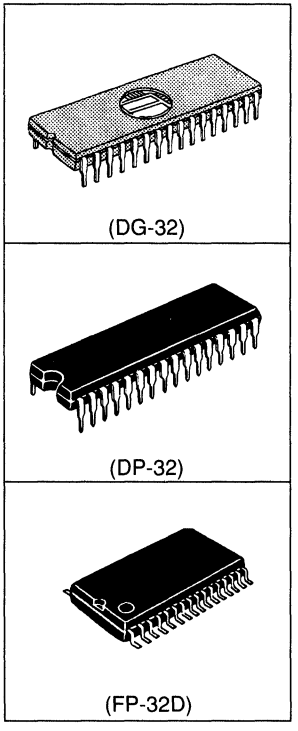
■ DESCRIPTION

The Hitachi HN27C301A is a 1-Megabit Ultraviolet Erasable and One-Time Programmable Electrically Programmable Read Only Memory organized as 131,072 x 8-bits.

The HN27C301A features fast address access times and low power dissipation. This combination makes the HN27C301A suitable for high speed microcomputer systems. The HN27C301A offers high speed programming using page programming mode.

Hitachi's HN27C301A is offered in 32-pin Ceramic and Plastic DIPs and plastic SOP packages.

The Ceramic DIP package is erasable by exposure to Ultraviolet light. The Plastic DIP and SOP packaged devices are One-Time Programmable and once programmed, can not be rewritten.



■ FEATURES

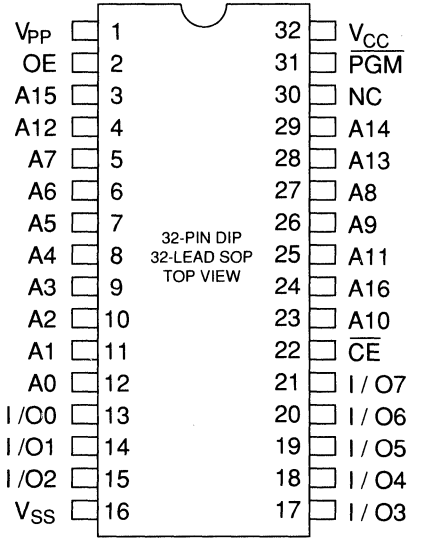
- Fast Access Times:
  100 ns/120 ns/150 ns/200 ns (max)
- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Low Power Dissipation:
  Active Mode: 50 mW/MHz (typ)
  Standby Mode: 5 μW (typ)
- High Speed Page and Word Programming:
  Page Programming Time: 14 sec (typ)
- Programming Power Supply:
  V_{PP} = 12.5 V ± 0.3 V
- Packages:
  32-pin Ceramic DIP
  32-pin Plastic DIP
  32-lead Plastic SOP

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN27C301AG-10	100 ns	32-pin Ceramic DIP (DG-32)
HN27C301AG-12	120 ns	
HN27C301AG-15	150 ns	
HN27C301AG-20	200 ns	
HN27C301AP-12	120 ns	32-pin Plastic DIP (DP-32)
HN27C301AP-15	150 ns	
HN27C301AP-20	200 ns	
HN27C301AFP-12	120 ns	32-lead Plastic SOP (FP-32D)
HN27C301AFP-15	150 ns	
HN27C301AFP-20	200 ns	

■ PIN ARRANGEMENT

HN27C301AG Series
HN27C301AP Series



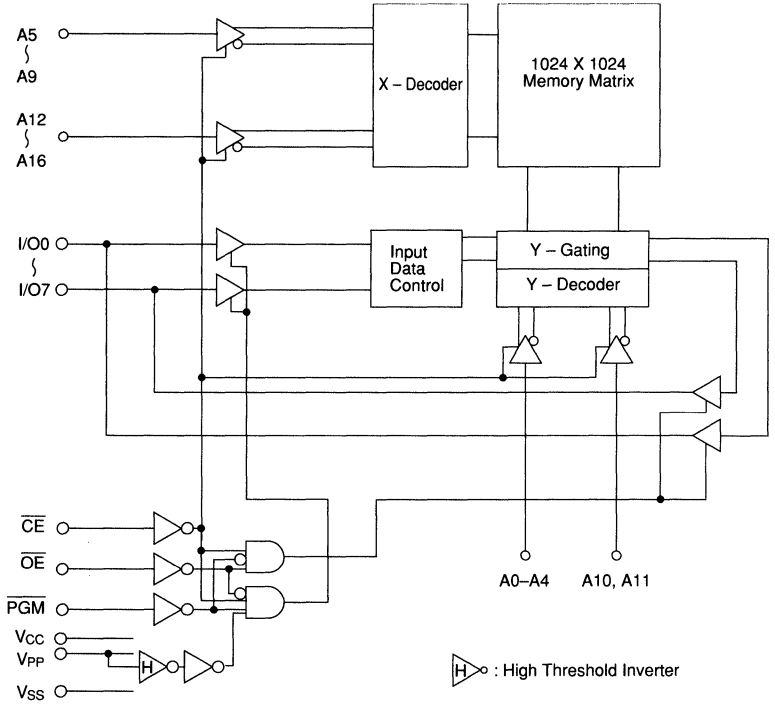
(PinD32.HN27C301A)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{16}	Address
I/O_0 - I/O_7	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{PP}	Programming Supply
V_{SS}	Ground
$\overline{PGM}$	Programming Enable
NC	No Connection

4

■ BLOCK DIAGRAM



(BD.HN27C301A)

■ MODE SELECTION

Mode	V_{PP}	V_{CC}	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	I/O
Read	V_{CC}	V_{CC}	V_{IL}	V_{IL}	V_{IH}	X[1]	D_{OUT}
Output Disable	V_{CC}	V_{CC}	V_{IL}	V_{IH}	V_{IH}	X	High-Z
Standby	V_{CC}	V_{CC}	V_{IH}	X	X	X	High-Z
Program	V_{PP}	V_{CC}	V_{IL}	V_{IH}	V_{IL}	X	D_{IN}
Program Verify	V_{PP}	V_{CC}	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}
Page Data Latch	V_{PP}	V_{CC}	V_{IH}	V_{IL}	V_{IH}	X	D_{IN}
Page Program	V_{PP}	V_{CC}	V_{IH}	V_{IH}	V_{IL}	X	High-Z
Program Inhibit	V_{CC}	V_{CC}	V_{IL}	V_{IL}	V_{IL}	X	High-Z
	V_{PP}	V_{CC}	V_{IL}	V_{IH}	V_{IH}	X	High-Z
	V_{PP}	V_{CC}	V_{IH}	V_{IL}	V_{IL}	X	High-Z
	V_{PP}	V_{CC}	V_{IH}	V_{IH}	V_{IH}	X	High-Z
Identifier	V_{CC}	V_{CC}	V_{IL}	V_{IL}	V_{IH}	V_H	ID

Notes: 1. X = Don't Care. $V_{PP} = 0$ V to V_{CC}.
2. $11.5\ V \leq V_H \leq 12.5\ V$

■ ELECTRICAL CHARACTERISTICS
REFER TO HN27C101A DATASHEET

■ ERASING THE HN27C301A

The Hitachi HN27C301A Ceramic DIP package allow the device to be erased by exposure to ultraviolet light of 2537Å. All of the data is changed to "1" after this erasure procedure. The minimum integrated dose (UV intensity x exposure time) for erasure is 15 W-sec/cm^2.

■ DEVICE IDENTIFIER MODE DESCRIPTION

The Device Identifier Mode allows binary codes to be read from the outputs that identify the manufacturer and the type of device. Using this mode with programming equipment, the device will automatically match its own erase and programming algorithm.

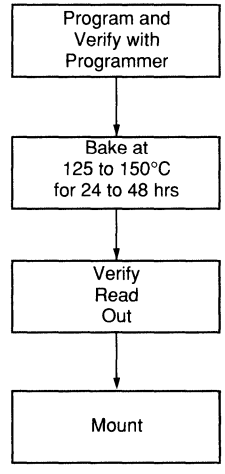
■ HN27C301A SERIES IDENTIFIER CODE

Identifier	A_0	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	1	0	1	1	1	0	0	1	B9

Notes: 1. $V_{CC} = 5.0\ V \pm 10\%$
2. $A_9 = 12.0\ V \pm 0.5V$
3. A_1-A_8, A_{10}-A_{16}, $\overline{CE}$, $\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$
4. X = Don't Care

■ HN27C301AP RECOMMENDED SCREENING CONDITIONS

Before mounting the HN27C101AP, please make the following screening (baking without bias) shown below:



(RSC.EPROM)

4

HN27V101A Series — Preliminary

1M (128K x 8-bit) OTP EPROM

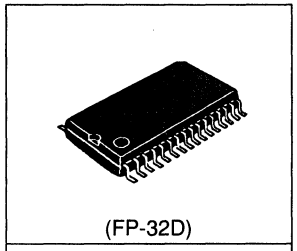
■ DESCRIPTION

The Hitachi HN27V101A is a 1-Megabit One-Time Programmable Electrically Programmable Read Only Memory organized as 131,072 x 8-bits.

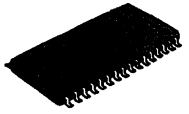
The HN27V101A features a low power supply voltage and low power dissipation. This combination makes the HN27V101A suitable for low power microcomputer systems. The HN27V101A offers high speed programming using page programming mode.

Hitachi's HN27V101A is offered in JEDEC-Standard Byte-Wide EPROM pinouts in 32-lead Plastic SOP and TSOP packages. The HN27V101A TSOP package is offered in both standard and reverse bend pinouts.

The Plastic SOP and TSOP packaged devices are One-Time Programmable and once programmed, can not be rewritten.



(FP-32D)



(TTP-32D)

(TTP-32DR)

■ FEATURES

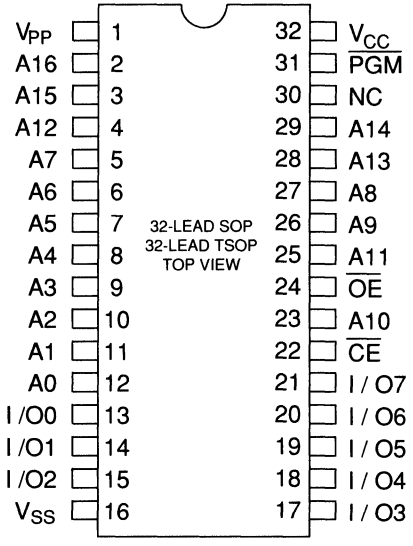
- Address Access Time:
  250 ns (max)
- Single Power Supply:
  V_{CC} = 2.7 to 5.5V
- Low Power Dissipation:
  Active Mode: 50 mW/MHz (typ)
  Standby Mode: 5 µW (typ)
- High Speed Page and Word Programming:
  Page Programming Time: 14 sec (typ)
- Programming Power Supply:
  V_{PP} = 12.5 V ± 0.3 V
- Pin Arrangement:
  JEDEC Standard Byte-Wide EPROM
- Packages:
  32-lead Plastic SOP
  32-lead Plastic TSOP (Type II)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN27V101AFP-25	250 ns	32-lead Plastic SOP (FP-32D)
HN27V101ATT-25	250 ns	32-lead Plastic TSOP (TTP-32D)
HN27V101ARR-25	250ns	32-lead Plastic TSOP (TTP-32DR) Reverse bend

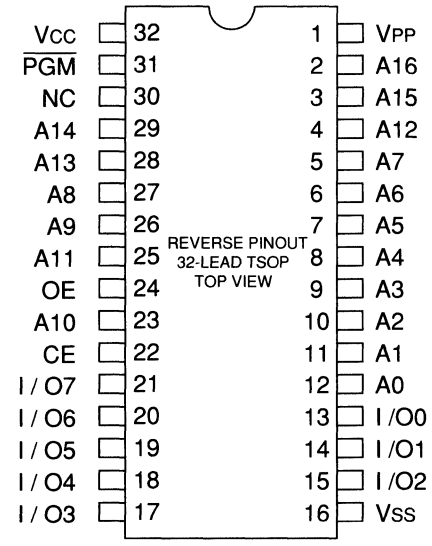
■ PIN ARRANGEMENT

HN27V101AFP Series
HN27V101ATT Series



(PinD32.HN27C101A)

HN27V101ARR Series



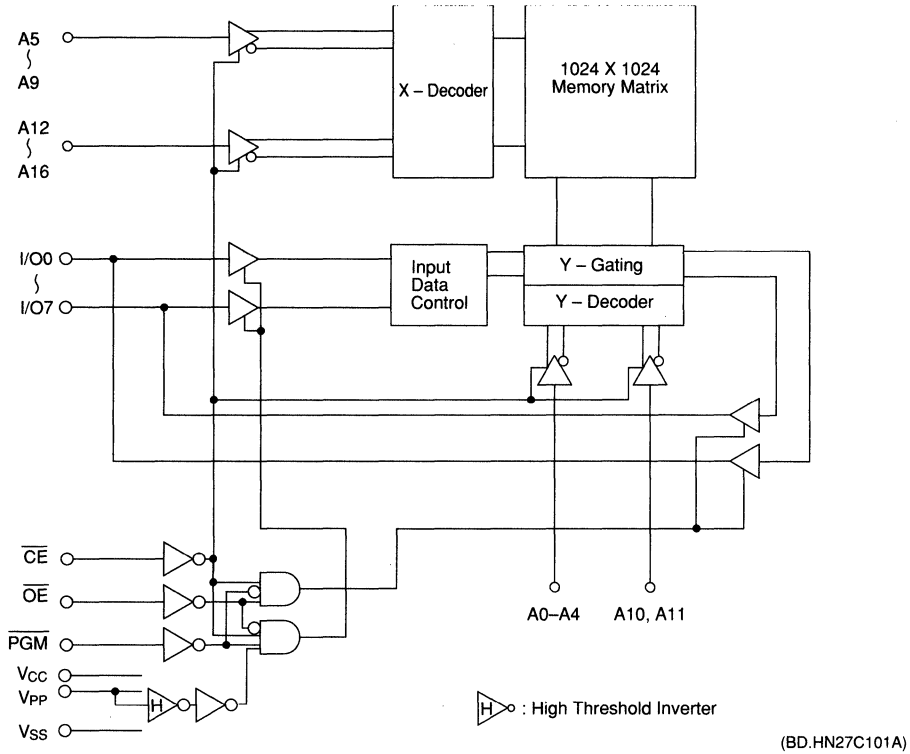
(PinT2.HN27C101A)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{16}	Address
I/O_0 - I/O_7	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{PP}	Programming Supply
V_{SS}	Ground
$\overline{PGM}$	Programming Enable
NC	No Connection

4

■ BLOCK DIAGRAM



(BD.HN27C101A)

■ MODE SELECTION

Mode	V_{PP}	V_{CC}	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	I/O
Read	V_{CC}	V_{CC}	V_{IL}	V_{IL}	V_{IH}	X[1]	D_{OUT}
Output Disable	V_{CC}	V_{CC}	V_{IL}	V_{IH}	V_{IH}	X	High-Z
Standby	V_{CC}	V_{CC}	V_{IH}	X	X	X	High-Z
Program	V_{PP}	V_{CC}	V_{IL}	V_{IH}	V_{IL}	X	D_{IN}
Program Verify	V_{PP}	V_{CC}	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}
Page Data Latch	V_{PP}	V_{CC}	V_{IH}	V_{IL}	V_{IH}	X	D_{IN}
Page Program	V_{PP}	V_{CC}	V_{IH}	V_{IH}	V_{IL}	X	High-Z
Program Inhibit	V_{CC}	V_{CC}	V_{IL}	V_{IL}	V_{IL}	X	High-Z
	V_{PP}	V_{CC}	V_{IL}	V_{IH}	V_{IH}	X	High-Z
	V_{PP}	V_{CC}	V_{IH}	V_{IL}	V_{IL}	X	High-Z
	V_{PP}	V_{CC}	V_{IH}	V_{IH}	V_{IH}	X	High-Z
Identifier	V_{CC}	V_{CC}	V_{IL}	V_{IL}	V_{IH}	V_H	ID

Notes: 1. X = Don't Care. $V_{PP} = 0$ V to V_{CC}.
2. $11.5\ V \leq V_H \leq 12.5\ V$

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Programming Voltage [1]	V_{PP}	-0.6 to +13.5	V
All Input and Output Voltage [1,2]	V_{IN}, V_{OUT}	-0.6 to +7.0	V
A_9 and $\overline{OE}$ Voltage [2]	V_{ID}	-0.6 to +13.0	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C
Storage Temperature Under Bias	T_{BIAS}	0 to +80	°C

Notes: 1. Relative to V_{SS}.
2. V_{IN}, V_{OUT}, and V_{ID} min = -1.0V for pulse width ≤ 20 ns.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	-	10	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	-	15	pF	V_{OUT} = 0V

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 2.7 to 5.5V, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{IN} = 5.5 V
Output Leakage Current	I_{LO}	-	-	2	µA	V_{OUT} = 5.5 V/0.45 V
Operating V_{CC} Current	I_{CC1}	-	-	30	mA	I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}
	I_{CC2}	-	-	30	mA	I_{OUT} = 0 mA, f = 4 MHz
Standby V_{CC} Current	I_{SB}	-	-	1	mA	$\overline{CE}$ = V_{IH}
	I_{SB2}	-	1	20	mA	$\overline{CE}$ = V_{CC} ± 0.3V
V_{PP} Current	I_{PP1}	-	1	20	µA	V_{PP} = 5.5 V
Input Voltage	V_{IH}	2.2	-	V_{CC} + 1 [2]	V	
	V_{IL}	-0.3 [1]	-	0.6/0.8	V	V_{CC} = 2.7 to 4.5 V/V_{CC} = 4.5 to 5.5 V
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA
	V_{OH}	V_{CC}-0.2	-	-	V	I_{OH} = -20 µA
	V_{OL}	-	-	0.45	V	I_{OL} = 1.0 mA
	V_{OL}	-	-	0.2	V	I_{OL} = 2.0 µA

Notes: 1. V_{IL} min = -1.0 V for pulse width ≤ 50 ns.
2. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns.
If V_{IH} is over the specified maximum value, Read operation can not be guaranteed.

4

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 2.7 to 5.5V, V_{PP} = V_{CC}, T_a = 0 to 70°C)

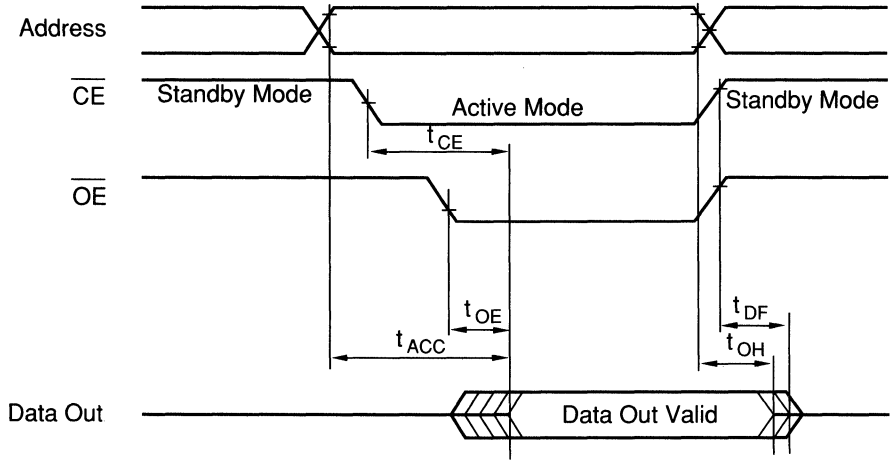
Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V/2.0 V

Item	Symbol	HN27V101A-25 Min.	HN27V101A-25 Max.	Unit	Test Condition
Address Access Time	t_{ACC}	-	250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
Chip Enable Access Time	t_{CE}	-	250	ns	$\overline{OE}$ = V_{IL}
Output Enable Access Time	t_{OE}	-	120	ns	$\overline{CE}$ = V_{IL}
Output Disable to High-Z [1]	t_{DF}	0	120	ns	$\overline{CE}$ = V_{IL}
Output Hold to Address Change	t_{OH}	0	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



(TD.R.HN27C101A)

■ DC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

(V_{CC} = 6.0 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, T_a = 25 °C ± 5 °C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{IN} = 0 V to V_{CC}
Operating V_{CC} Current	I_{CC}	-	-	30	mA	
Operating V_{PP} Current	I_{PP}	-	-	40	mA	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}
Input Voltage [3]	V_{IH}	2.2	-	V_{CC} +.5 [6]	V	
	V_{IL}	- 0.1[5]	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA
	V_{OL}	-	-	0.45	V	I_{OH} = 2.1 mA

Notes:
1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13 V, including overshoot.
3. Device reliability may be adversely affected if the device is installed or removed while V_{PP} = 12.5 V.
4. Do not change V_{PP} from V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = low.
5. V_{IL} min = -0.6 V for pulse width ≤ 20 ns.
6. If V_{IH} is over the specified maximum value, programming operation can not be guaranteed.

■ AC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

(V_{CC} = 6.0V ± 0.25 V, V_{PP} = 12.5 v ± 0.3 V, T_a = 25°C ± 5°C)

Test Conditions

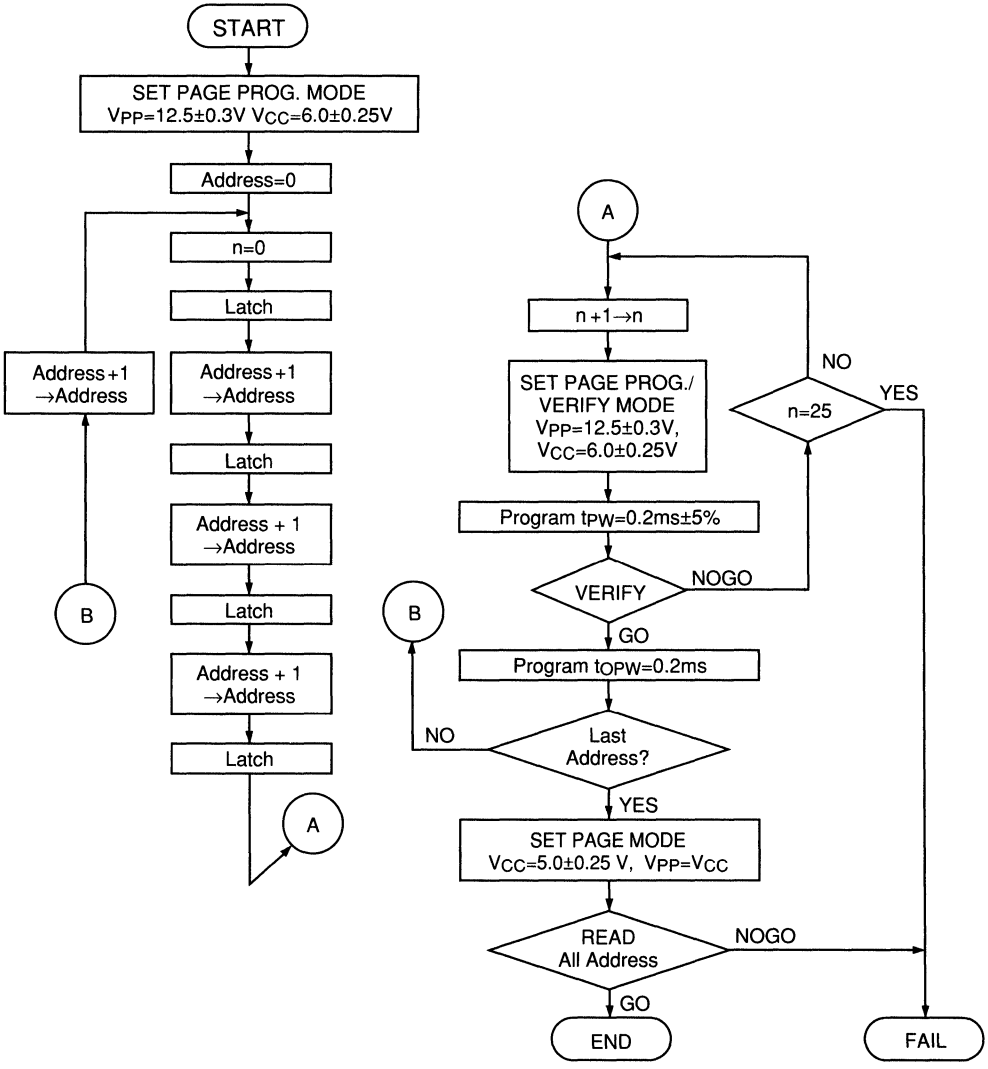
- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 20 ns
- Reference levels for measuring timing: 0.8 V / 2.0V

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	2	-	-	µs	
Address Hold Time	t_{AH}	0	-	-	µs	
Data Setup Time	t_{DS}	2	-	-	µs	
Data Hold Time	t_{DH}	2	-	-	µs	
Chip Enable Setup Time	t_{CES}	2	-	-	µs	
V_{PP} Setup Time	t_{VPS}	2	-	-	µs	
V_{CC} Setup Time	t_{VCS}	2	-	-	µs	
Output Enable Setup Time	t_{OES}	2	-	-	µs	
Output Disable Time	t_{DF}	0	-	130	ns	
$\overline{PGM}$ Initial Programming Pulse Width	t_{PW}	0.19	0.20	0.21	ms	
$\overline{PGM}$ Overprogramming Pulse Width	t_{OPW}	0.19	-	5.25	ms	
Data Valid from Output Enable Time	t_{OE}	0	-	150	ns	
Output Enable Pulse During Data Latch	t_{LW}	1	-	-	µs	
Output Enable Hold Time	t_{OEH}	2	-	-	µs	
Chip Enable Hold Time	t_{CEH}	2	-	-	µs	
$\overline{PGM}$ Setup Time	t_{PGMS}	2	-	-	µs	

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

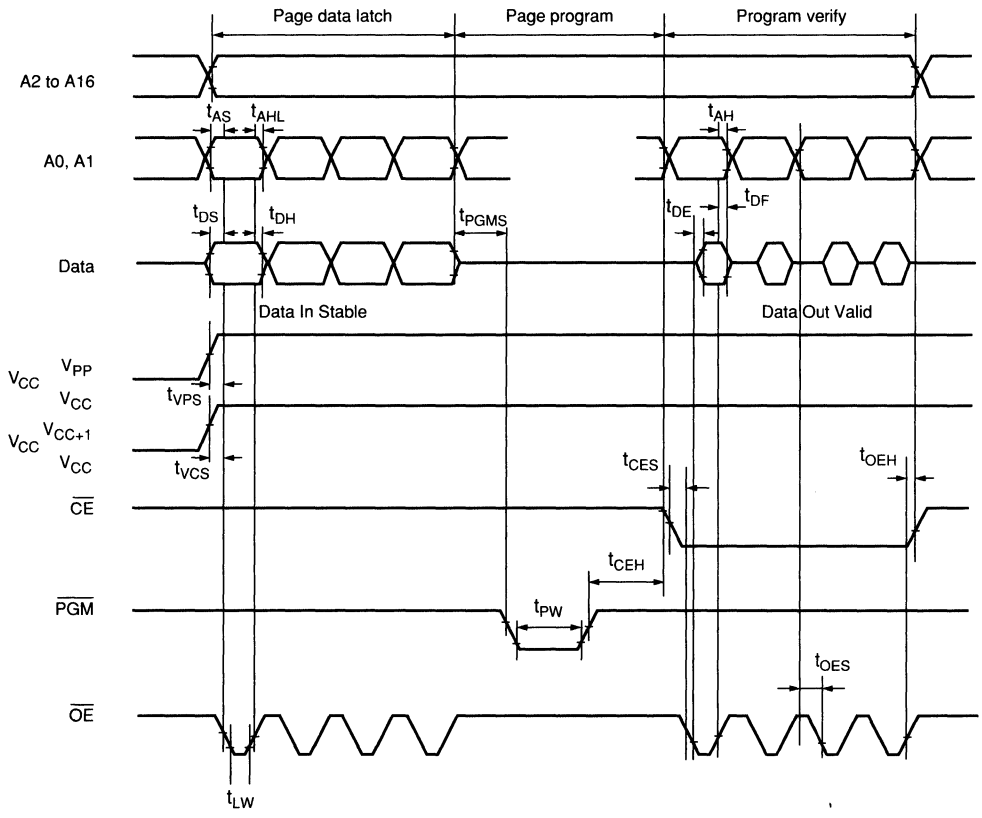
■ PAGE PROGRAMMING FLOWCHART

The Hitachi HN27V101A can be programmed with the high performance Page Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.



(FC.PP.HN27C101A)

■ PAGE PROGRAMMING TIMING WAVEFORM

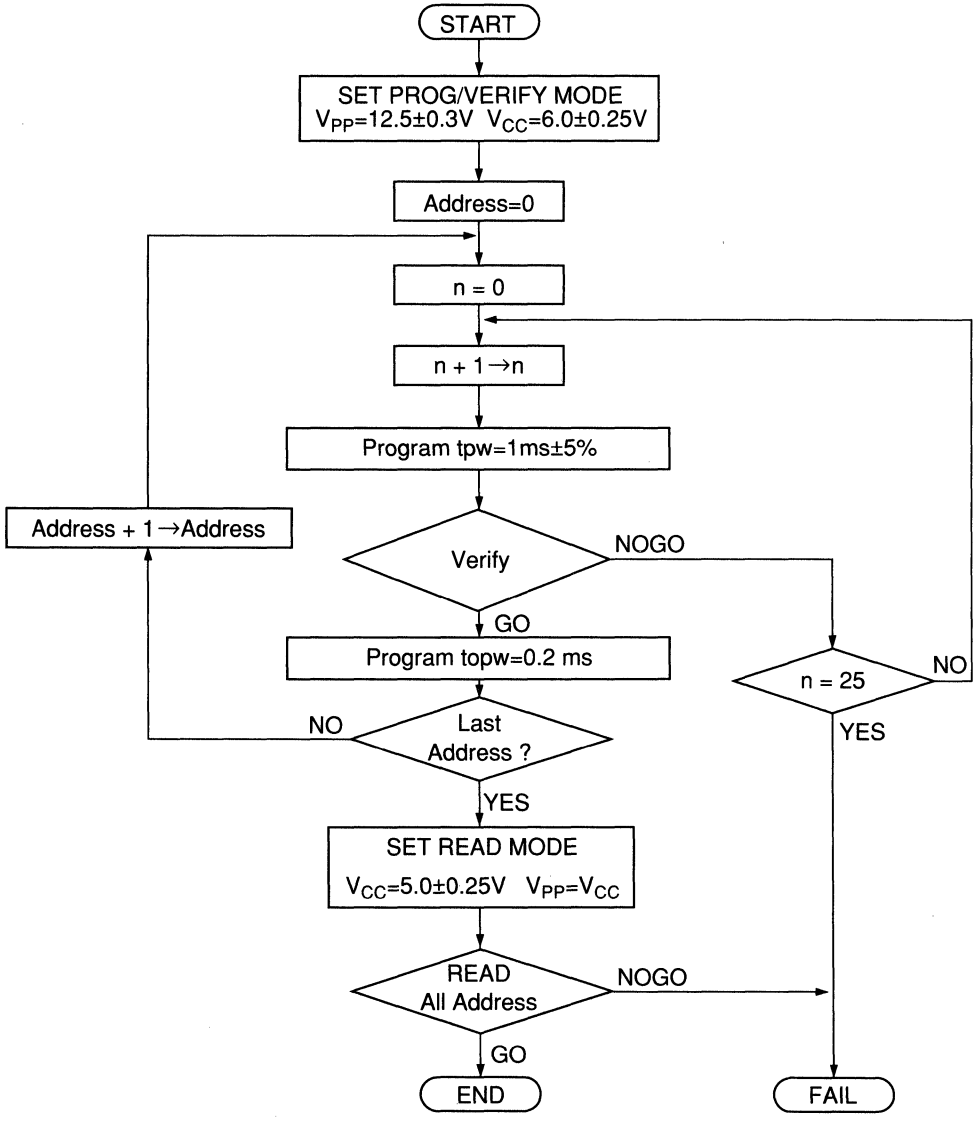


(TD.PP.HN27C101A)

4

■ BYTE PROGRAMMING FLOWCHART

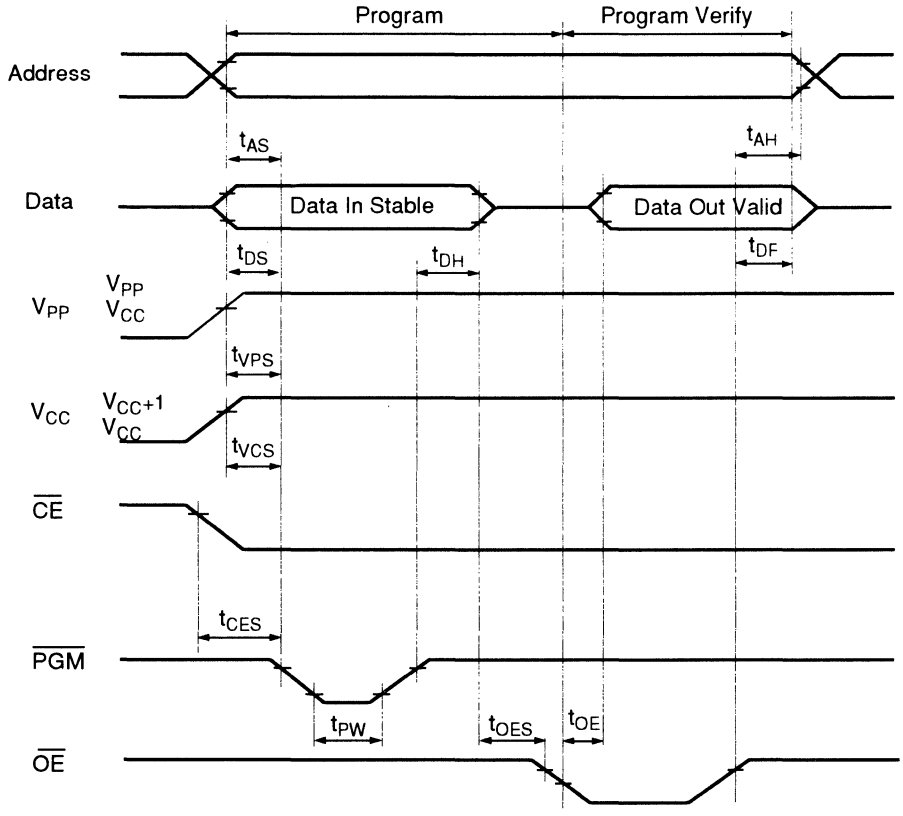
The Hitachi HN27V101A can be programmed with the high performance Byte Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.



(FC.P.HN27C101A)

Hitachi America, Ltd. • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

■ BYTE PROGRAMMING TIMING WAVEFORM



(TD P.HN27C101A)

4

■ DEVICE IDENTIFIER MODE DESCRIPTION

The Device Identifier Mode allows binary codes to be read from the outputs that identify the manufacturer and the type of device. Using this mode with programming equipment, the device will automatically match its own erase and programming algorithm.

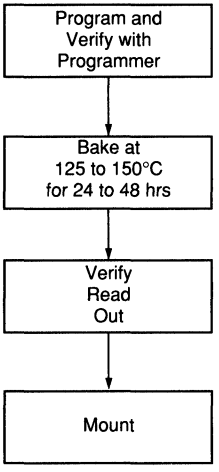
■ HN27C101A SERIES IDENTIFIER CODE

Identifier	A_0	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	0	0	1	1	1	0	0	0	38

Notes: 1. $V_H = 12.0\ V \pm 0.5V$
2. A_1-A_8, A_{10}-A_{16}, $\overline{CE}$, $\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$
4. X = Don't Care

■ HN27V101A RECOMMENDED SCREENING CONDITIONS

Before mounting the HN27V101A plastic packages, please make the following screening (baking without bias) shown below:



(RSC.EPROM)

HN27C4000 Series

Preliminary

4M (256K x 16-bit or 512K x 8-bit) UV and OTP EPROM

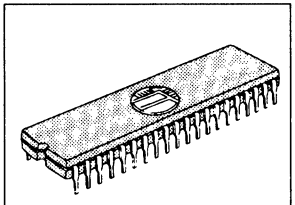
■ DESCRIPTION

The Hitachi HN27C4000 is a 4-Megabit Ultraviolet Erasable and One-Time Programmable Electrically Programmable Read Only Memory organized as 524,288 x 8-bits or as 262,144 x 16-bits.

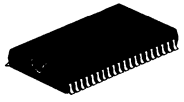
The HN27C4000 features high speed Fast Address Access and low power dissipation. This combination makes the HN27C4000 suitable for high speed 16 and 32-bit microcomputer systems. The HN27C4000 offers high speed programming using page programming mode.

Hitachi's HN27C4000 is offered in JEDEC-Standard Byte-Wide / Word-Wide EPROM pinouts in 40-pin Ceramic DIP and 40-lead Plastic SOP packages. This allows socket replacement with Mask ROMs.

The Ceramic DIP packaged device is erasable by exposure to Ultraviolet light. The SOP packaged device is One-Time Programmable and once programmed, can not be rewritten.



(DG-40A)



(FP-40D)

■ FEATURES

- Fast Random Access Times:
  100 ns/120 ns/150 ns (max)
- Fast Address Access Times (A_0, A_1):
  50 ns/60 ns (max)
- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Low Power Dissipation:
  Active Mode: 150 mW/MHz (typ)
  Standby Mode: 5 µW (max)
- High Speed Page and Word Programming:
  Page Programming Time: 3.5 sec (min)
- Programming Power Supply:
  V_{PP} = 12.5 V ± 0.3 V
- Pin Arrangement:
  JEDEC Standard Word-Wide EPROM
  Mask ROM Compatible
- Packages:
  40-pin Ceramic DIP
  40-lead Plastic SOP

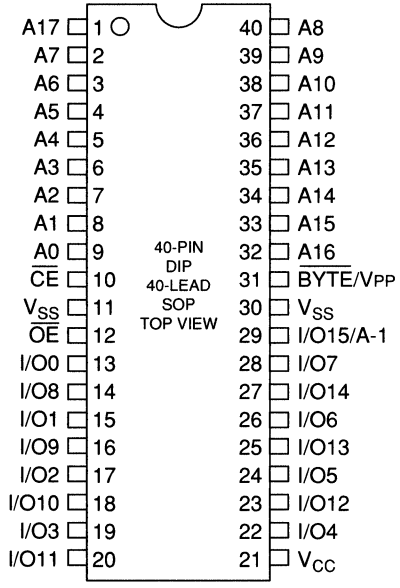
■ ORDERING INFORMATION

Type No.	Access Time	Package
HN27C4000G-10	100 ns	40-pin Ceramic DIP
HN27C4000G-12	120 ns	(DG-40A)
HN27C4000G-15	150 ns	
HN27C4000FP-12	120 ns	40-lead Plastic SOP
HN27C4000FP-15	150 ns	(FP-40D)

4

■ PIN ARRANGEMENT

HN27C4000G Series
HN27C4000FP Series

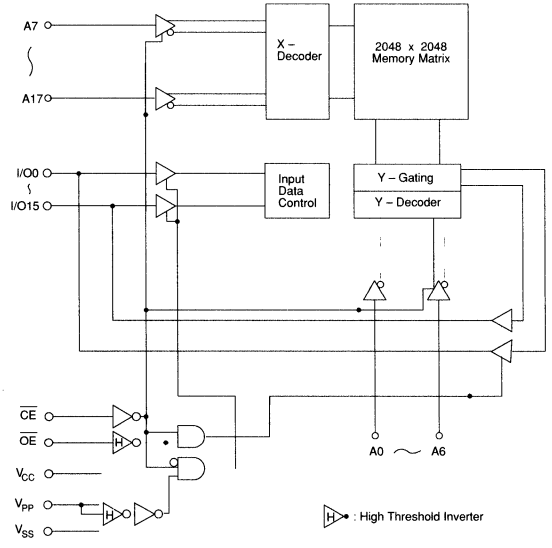


(PinD40.HN27C4000)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{17}	Address
A_{-1}	Address (Word-Wide)
I/O_0 - I/O_{15}	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
$\overline{BYTE}/V_{PP}$	Byte/Word Selection Programming Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



(BD.HN27C4096)

■ MODE SELECTION

Mode	$\overline{BYTE}/V_{PP}$	V_{CC}	$\overline{CE}$	$\overline{OE}$	A_9	I/O_0 - I/O_7	I/O_8 - I/O_{14}	I/O_{15} / A_{-1}
Read (x16)	V_{IH}	V_{CC}	V_{IL}	V_{IL}	X [1]	D_{OUT}	D_{OUT}	D_{OUT}
Read (x8)	V_{IL}	V_{CC}	V_{IL}	V_{IL}	X [1]	D_{OUT}	High-Z	V_{IH}/V_{IL}
Output Disable (x16)	V_{IH}	V_{CC}	V_{IL}	V_{IH}	X	High-Z	High-Z	High-Z
Output Disable (x8)	V_{IL}	V_{CC}	V_{IL}	V_{IH}	X	High-Z	High-Z	V_{IH}/V_{IL}
Standby	V_{SS} to V_{CC}	V_{CC}	V_{IH}	X	X	High-Z	High-Z	High-Z
Page Programming								
Page Prog. Set	V_{PP}	V_{CC}	V_{IH}	V_H [2]	X	High-Z	High-Z	High-Z
Page Data Latch	V_{PP}	V_{CC}	V_{IL}	V_H	X	D_{IN}	D_{IN}	D_{IN}
Page Program	V_{PP}	V_{CC}	V_{IL}	V_{IH}	X	High-Z	High-Z	High-Z
Page Prog. Verify	V_{PP}	V_{CC}	V_{IH}	V_{IL}	X	D_{OUT}	D_{OUT}	D_{OUT}
Page Prog. Reset	V_{CC}	V_{CC}	V_{IH}	V_{IH}	X	High-Z	High-Z	High-Z
Word Programming								
Program	V_{PP}	V_{CC}	V_{IL}	V_{IH}	X	D_{IN}	D_{IN}	D_{IN}
Program Verify	V_{PP}	V_{CC}	V_{IH}	V_{IL}	X	D_{OUT}	D_{OUT}	D_{OUT}
Optional Verify	V_{PP}	V_{CC}	V_{IL}	V_{IL}	X	D_{OUT}	D_{OUT}	D_{OUT}
Program Inhibit	V_{PP}	V_{CC}	V_{IH}	V_{IH}	X	High-Z	High-Z	High-Z
Identifier	V_{SS}-V_{CC}	V_{CC}	V_{IL}	V_{IL}	V_H	ID	ID	ID

Notes: 1. X = Don't Care. V_{PP} = 0 V to V_{CC}.
2. 11.5 V ≤ V_H ≤ 12.5 V

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Programming Voltage [1]	V_{PP}	-0.6 to +13.5	V
All Input and Output Voltage [1,2]	V_{IN}, V_{OUT}	-0.6 to +7.0	V
A_9 and $\overline{OE}$ Voltage [2]	V_{ID}	-0.6 to +13.0	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range [3]	T_{STG}	-65 to +125	°C
Storage Temperature Under Bias	T_{BIAS}	0 to +80	°C

Notes: 1. Relative to V_{SS}.
2. V_{IN}, V_{OUT}, and V_{ID} min = -2.0V for pulse width ≤ 20 ns.
3. Device storage temperature range before programming.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	-	-	12	pF	V_{IN} = 0V [1]
Output Capacitance	C_{OUT}	-	-	20	pF	V_{OUT} = 0V

Notes: 1. Except $\overline{BYTE}/V_{PP}$.

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{IN} = 5.5 V
Output Leakage Current	I_{LO}	-	-	2	µA	V_{OUT} = 5.5 V/0.45 V
Operating V_{CC} Current	I_{CC1}	-	-	35	mA	I_{OUT} = 0 mA, f = 1 MHz
	I_{CC2}	-	-	120	mA	I_{OUT} = 0 mA, f = 10 MHz
Standby V_{CC} Current	I_{SB1}	-	-	1	mA	$\overline{CE}$ = V_{IH}
	I_{SB2}	-	1	20	µA	$\overline{CE}$ = V_{CC} ± 0.3 V
V_{PP} Current	I_{PP1}	-	1	20	µA	V_{PP} = 5.5 V
Input Voltage	V_{IH}	2.2	-	V_{CC} + 1 [2]	V	
	V_{IL}	-0.3 [1]	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA
	V_{OL}	-	-	0.45	V	I_{OL} = 2.1 mA

Notes: 1. V_{IL} min = -1.0 V for pulse width ≤ 50 ns.
V_{IL} min = -2.0 V for pulse width ≤ 20 ns.
2. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns.
If V_{IH} is over the specified maximum value, Read operation can not be guaranteed.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

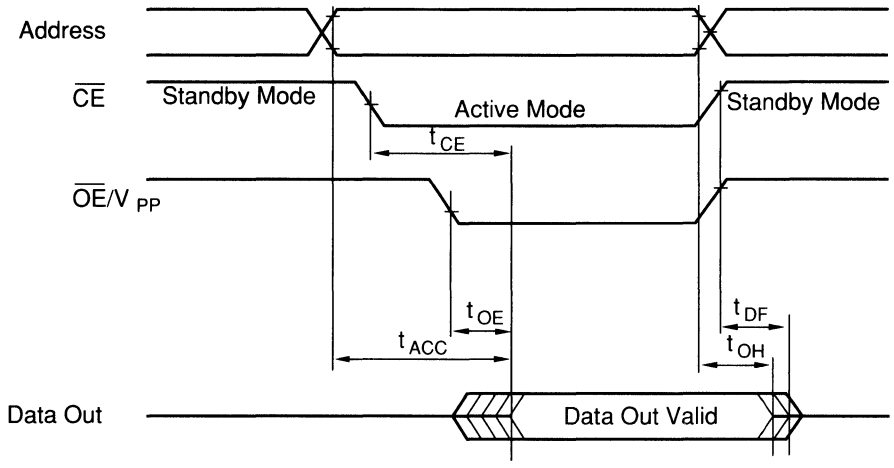
Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V/2.0 V

Item	Symbol	HN27C4000-10		HN27C4000-12		HN27C4000-15		Unit	Test Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
Address Access Time	t_{ACC}	-	100	-	120	-	150	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
Chip Enable Access Time	t_{CE}	-	100	-	120	-	150	ns	$\overline{OE}$ = V_{IL}
Output Enable Access Time	t_{OE}	-	60	-	60	-	70	ns	$\overline{CE}$ = V_{IL}
Fast Address Access	t_{BAC}	-	50	-	60	0	60	ns	$\overline{CE}$ = V_{IL}
Output Disable to High-Z [1]	t_{DF}	0	35	0	40	0	50	ns	$\overline{CE}$ = V_{IL}
Output Hold to Address Change	t_{OH}	5	-	5	-	5	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

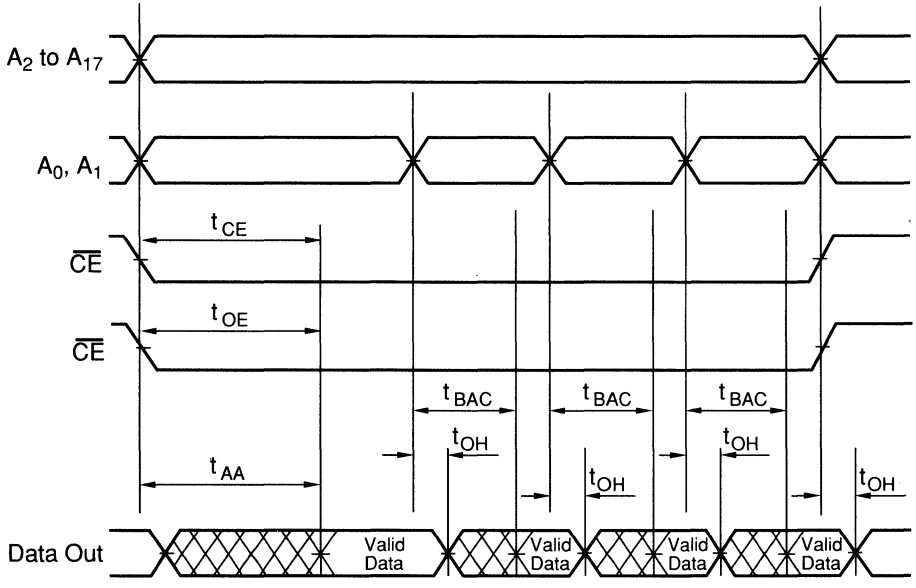
Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



(TD.R.HN27C4096)

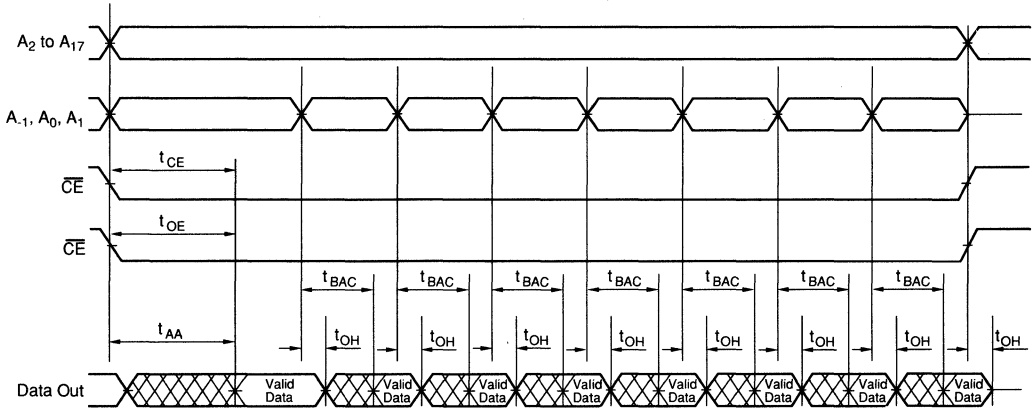
■ READ TIMING WAVEFORM (Fast Address Access in x16 mode)



(TD.RNW.HN27C4000)

4

■ READ TIMING WAVEFORM (Fast Address Access in x8 mode)



(TD.RNB.HN27C4000)

■ DC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

(V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, T_a = 25 °C ± 5 °C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{IN} = 6.5 V/ 0.45 V
Operating V_{CC} Current	I_{CC}	-	-	50	mA	
Operating V_{PP} Current	I_{PP}	-	-	70	mA	$\overline{CE}$ = V_{IL}
Input Voltage [3]	V_{IH}	2.2	-	V_{CC} +.5 [6]	V	
	V_{IL}	- 0.1[5]	-	0.8	V	
	V_H	11.5	12.0	12.5	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA
	V_{OL}	-	-	0.45	V	I_{OH} = 2.1 mA

Notes:
1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13 V, including overshoot.
3. Device reliability may be adversely affected if the device is installed or removed while V_{PP} = 12.5 V.
4. Do not change V_{PP} from V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = low.
5. V_{IL} min = -0.6 V for pulse width ≤ 20 ns.
6. If V_{IH} is over the specified maximum value, programming operation can not be guaranteed.

■ AC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

(V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.5 v ± 0.3 V, T_a = 25°C ± 5°C)

Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 20 ns
- Reference levels for measuring timing: 0.8 V / 2.0V

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	2	-	-	µs	
Address Hold Time	t_{AH}	0	-	-	µs	
Data Setup Time	t_{DS}	2	-	-	µs	
Data Hold Time	t_{DH}	2	-	-	µs	
Chip Enable Setup Time	t_{CES}	2	-	-	µs	
V_{PP} Setup Time	t_{VPS}	2	-	-	µs	
V_{CC} Setup Time	t_{VCS}	2	-	-	µs	
Output Enable Setup Time	t_{OES}	2	-	-	µs	
Output Disable Time	t_{DF}	0	-	130	ns	
Programming Pulse Width	t_{PW}	47.5	50.0	52.5	µs	
Data Valid from Output Enable Time	t_{OE}	0	-	150	ns	
Chip Enable Pulse Width During Data Latch	t_{LW}	1	-	-	µs	
Output Enable = V_H Setup Time	t_{OHS}	2	-	-	µs	
Output Enable = V_H Hold Time	t_{OHH}	2	-	-	µs	
Output Enable Hold Time	t_{OEH}	2	-	-	µs	
V_{PP} Hold Time	t_{VRS}	1	-	-	µs	
Page Programming Reset Time	t_{VLW}	1	-	-	µs	

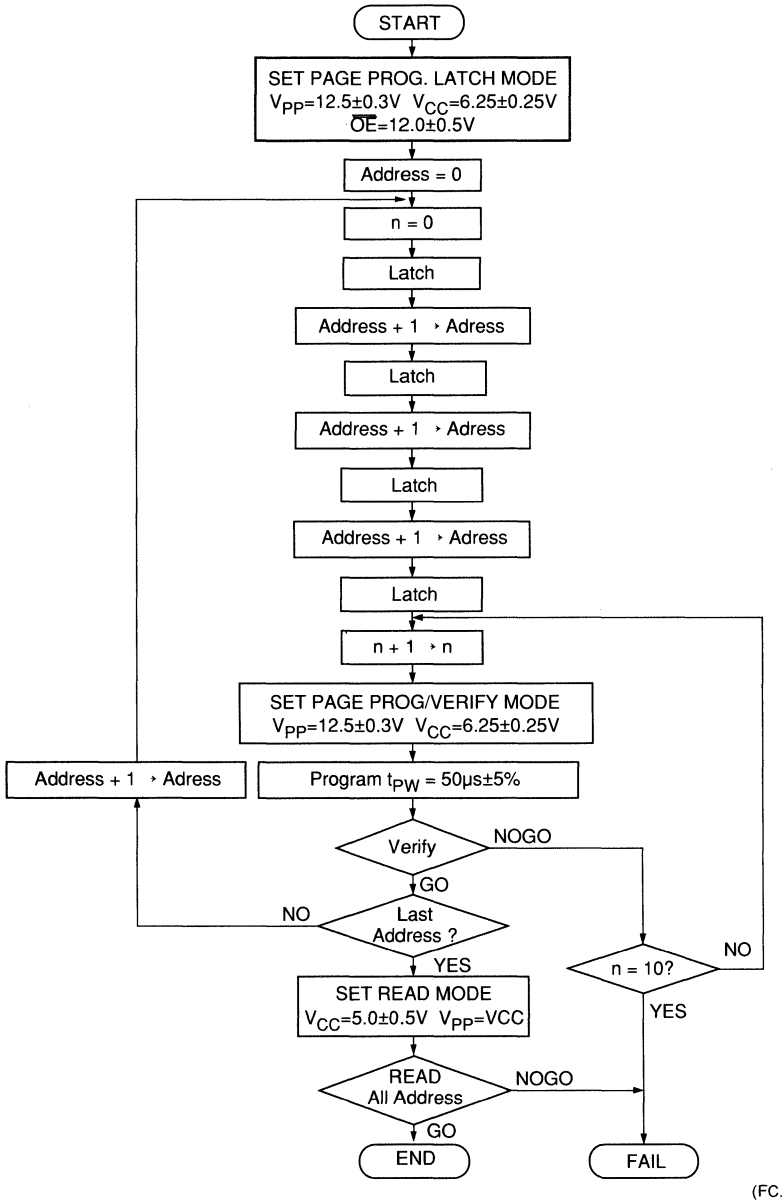
Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.
2. Page Program Mode will be reset when V_{PP} is set to V_{CC} or less.

4

■ PAGE PROGRAMMING FLOWCHART

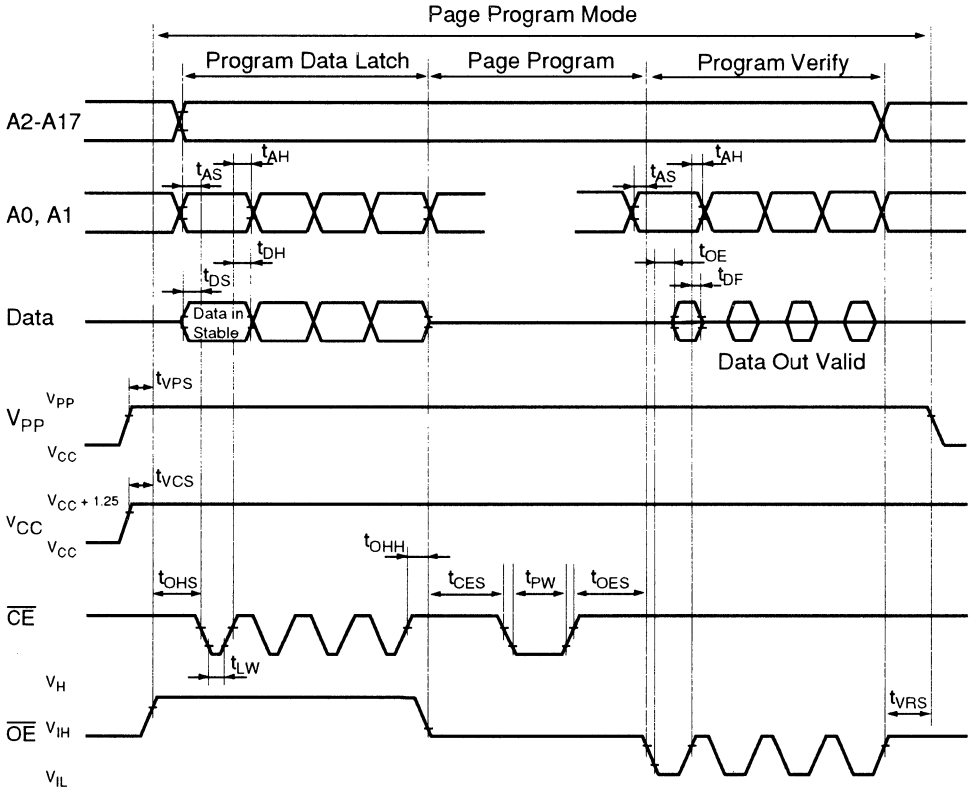
The Hitachi HN27C4000 can be programmed with the high performance Page Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.

Note: 1. To set the device into Page Programming, apply 12.5 V to V_{PP} then followed by applying 12 V to $\overline{OE}$. The device operates in Page Program Mode until reset.
2. To reset the Page Program Mode, set $V_{PP} = V_{CC}$ or less.



(FC.PP.HN27C4096)

■ PAGE PROGRAMMING TIMING WAVEFORM

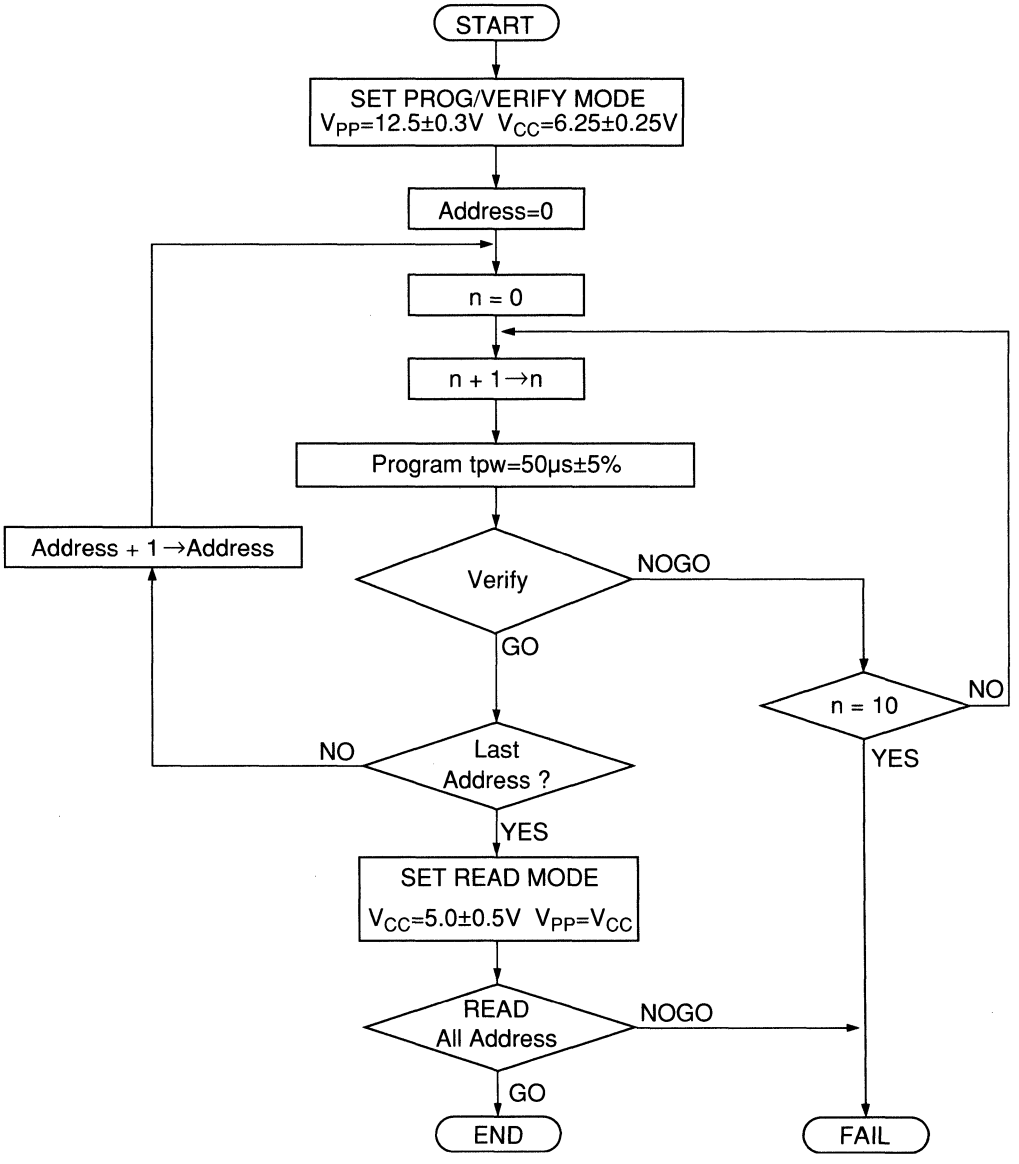


(TD.PP HN27C4096)

4

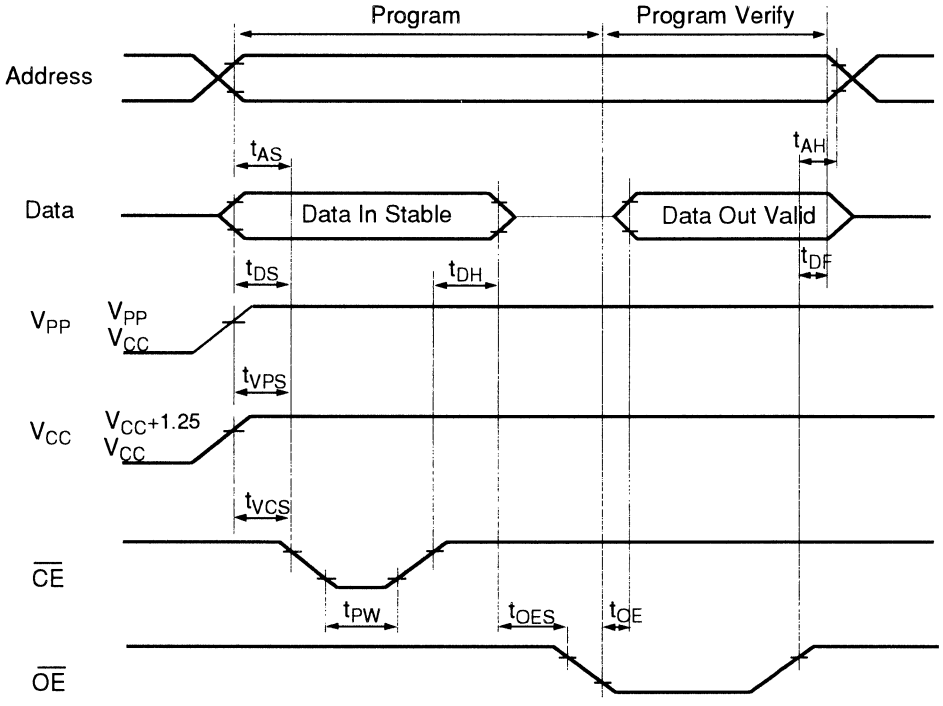
■ WORD PROGRAMMING FLOWCHART

The Hitachi HN27C4000 can be programmed with the high performance Word Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.



(FC.P.HN27C4096)

■ WORD PROGRAMMING TIMING WAVEFORM



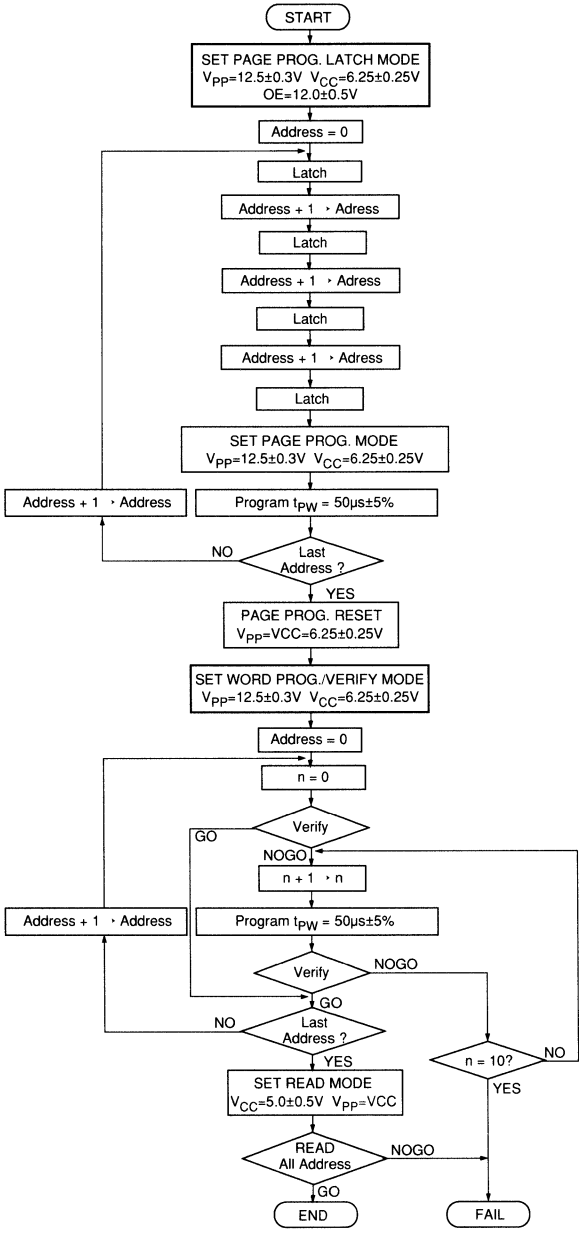
(TD.P HN27C4096)

■ OPTIONAL PAGE PROGRAMMING FLOWCHART

The Hitachi HN27C4000 can be programmed with the high performance Optional Page Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.

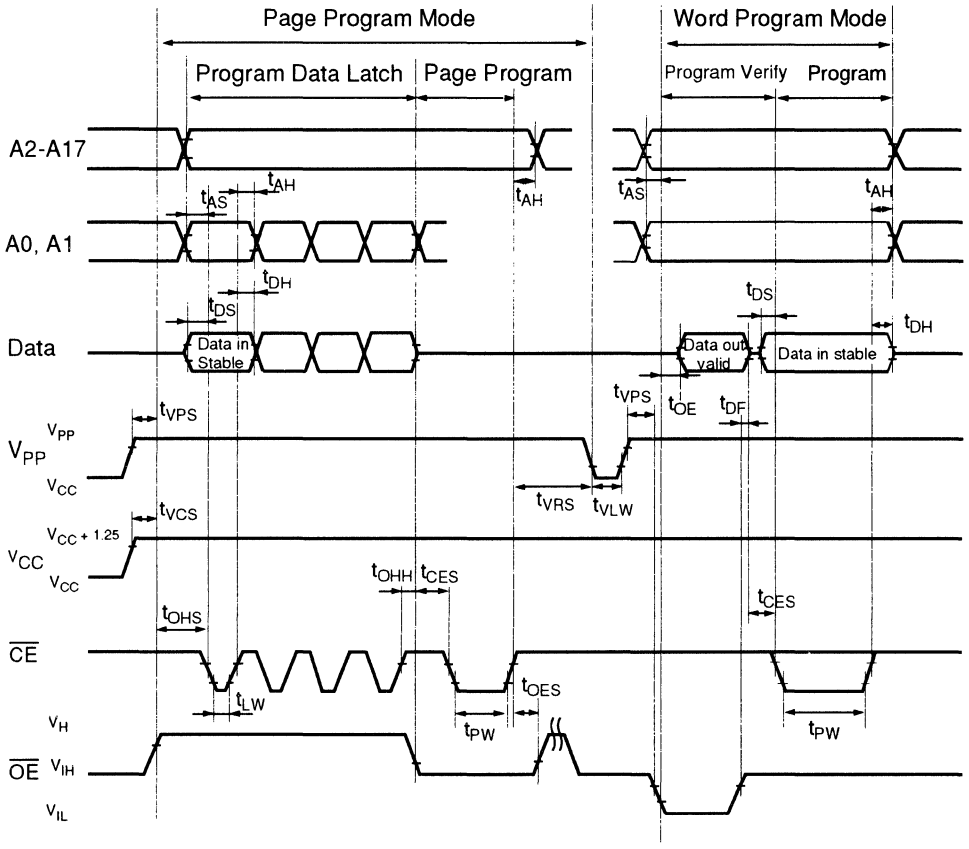
This programming algorithm is a combination of Page Programming and Word Verify. It can be used to avoid the increased programming verify time when a programmer with a slower machine cycle is used and shorten the total programming time.

Please refer to the timing specifications for page programming and word programming.



(FC.OPP.HN27C4096)

■ OPTIONAL PAGE PROGRAMMING TIMING WAVEFORM



(TD.OPP.HN27C4096)

4

■ ERASING THE HN27C4000

The Hitachi HN27C4000 Ceramic DIP package allows this devices to be erased by exposure to ultraviolet light of 2537Å. All of the data is changed to "1" after this erasure procedure. The minimum integrated dose (UV intensity x exposure time) for erasure is 15 W-sec/cm^2.

■ DEVICE IDENTIFIER MODE DESCRIPTION

The Device Identifier Mode allows binary codes to be read from the outputs that identify the manufacturer and the type of device. Using this mode with programming equipment, the device will automatically match its own erase and programming algorithm.

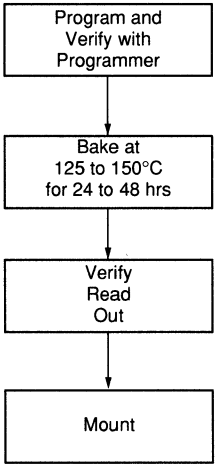
■ HN27C4096 SERIES IDENTIFIER CODE

Identifier	A_0	I/O_8-I/O_{15}	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Hex Data
Manufacturer Code	V_{IL}	X	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	X	1	0	1	0	0	0	0	1	A1

Notes:
1. V_{CC} = 5.0 V ± 10%
2. A_9 = 12.0 V ± 0.5V
3. A_1-A_8, A_{10}-A_{17}, $\overline{CE}$, $\overline{OE}$ = V_{IL}
4. X = Don't Care

■ HN27C4096CP RECOMMENDED SCREENING CONDITIONS

Before mounting the HN27C4096CP package, please make the following screening (baking without bias) shown below:



(RSC.EPROM)

HN27C4096 Series

4M (256K x 16-bit) UV and OTP EPROM

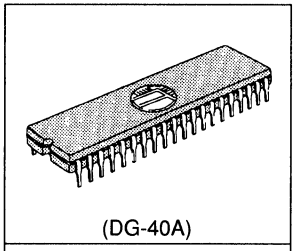
■ DESCRIPTION

The Hitachi HN27C4096 is a 4-Megabit Ultraviolet Erasable and One-Time Programmable Electrically Programmable Read Only Memory organized as 262,144 x 16-bits.

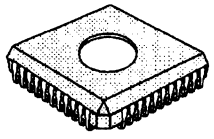
The HN27C4096 features fast address access times of 100, 120 and 150 ns and low power dissipation. This combination makes the HN27C4096 suitable for high speed 16 and 32-bit microcomputer systems. The HN27C4096 offers high speed programming using page programming mode.

Hitachi's HN27C4096 is offered in JEDEC-Standard Word-Wide EPROM pinouts in 40-pin Ceramic DIP and 44-lead Ceramic and Plastic LCC packages. This allows socket replacement with Mask ROMs.

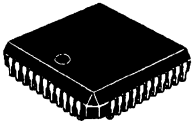
The Ceramic DIP and Ceramic LCC packages are erasable by exposure to Ultraviolet light. The PLCC packaged device is One-Time Programmable and once programmed, can not be rewritten.



(DG-40A)



(CC-44)



(CP-44)

■ FEATURES

- Fast Access Times:
  100 ns/120 ns/150 ns (max)
- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Low Power Dissipation:
  Active Mode: 35 mW/MHz (typ)
  Standby Mode: 5 µW (max)
- High Speed Page and Word Programming:
  Page Programming Time: 3.5 sec (min)
- Programming Power Supply:
  V_{PP} = 12.5 V ± 0.3 V
- Pin Arrangement:
  JEDEC Standard Word-Wide EPROM
  Mask ROM Compatible
- Packages:
  40-pin Ceramic DIP
  44-lead Ceramic LCC
  44-lead PLCC

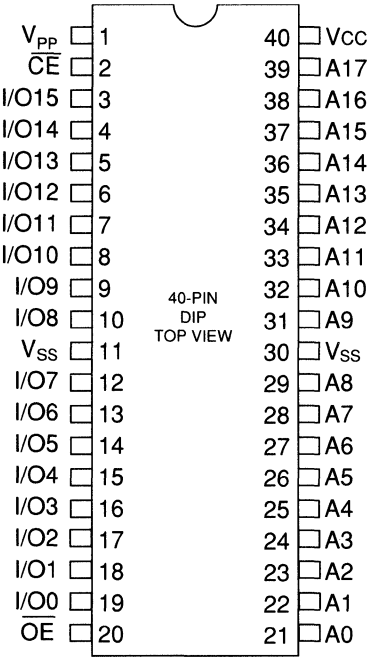
■ ORDERING INFORMATION

Type No.	Access Time	Package
HN27C4096G-10	100 ns	40-pin Ceramic DIP
HN27C4096G-12	120 ns	(DG-40A)
HN27C4096G-15	150 ns	
HN27C4096CC-10	100 ns	44-lead Ceramic LCC
HN27C4096CC-12	120 ns	(CC-44)
HN27C4096CC-15	150 ns	
HN27C4096CP-12	120 ns	44-lead PLCC
HN27C4096CP-15	150 ns	(CP-44)

4

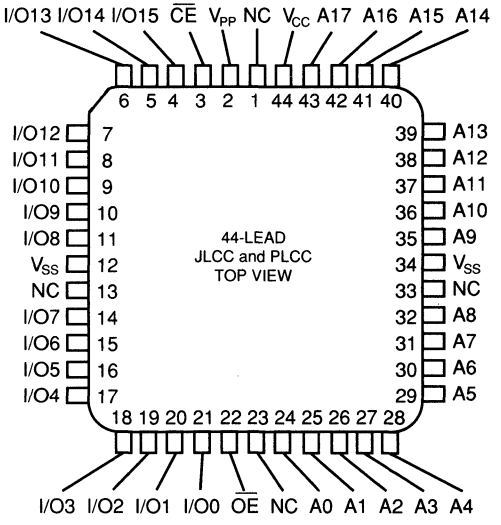
■ PIN ARRANGEMENT

HN27C4096G Series



(PinD40.HN27C4096)

HN27C4096CC Series
HN27C4096CP Series

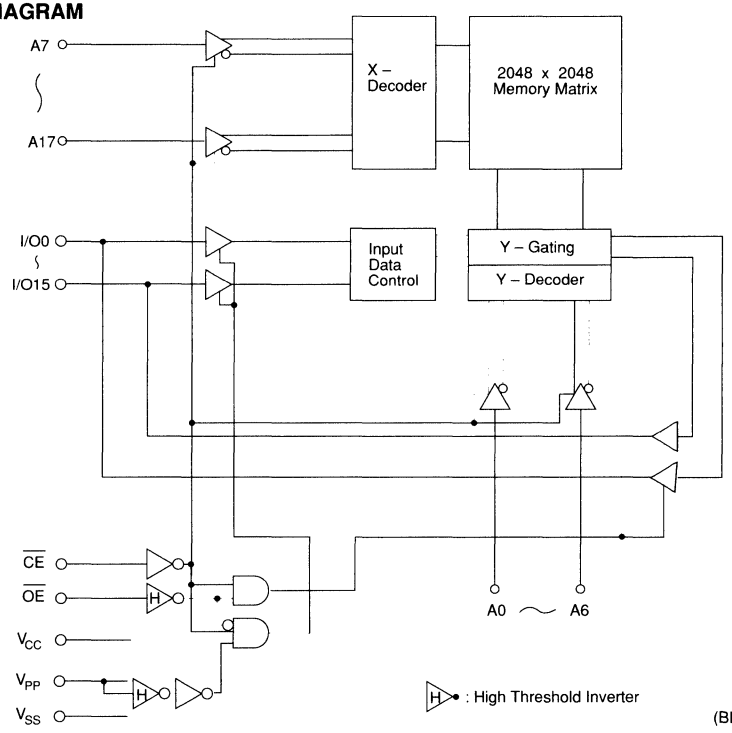


(PinQ44.HN27C4096)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{17}	Address
I/O_0 - I/O_{15}	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{PP}	Programming Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



(BD.HN27C4096)

■ MODE SELECTION

Mode		V_{PP}	V_{CC}	$\overline{CE}$	$\overline{OE}$	A_9	I/O
Read		V_{SS}-V_{CC}	V_{CC}	V_{IL}	V_{IL}	X[1]	D_{OUT}
Output Disable		V_{SS}-V_{CC}	V_{CC}	V_{IL}	V_{IH}	X	High-Z
Standby		V_{SS}-V_{CC}	V_{CC}	V_{IH}	X	X	High-Z
Page Prog.	Page Prog. Set	V_{PP}	V_{CC}	V_{IH}	V_H[2]	X	High-Z
	Page Data Latch	V_{PP}	V_{CC}	V_{IL}	V_H	X	D_{IN}
	Page Program	V_{PP}	V_{CC}	V_{IL}	V_{IH}	X	High-Z
	Page Prog. Verify	V_{PP}	V_{CC}	V_{IH}	V_{IL}	X	D_{OUT}
	Page Prog. Reset	V_{CC}	V_{CC}	V_{IH}	V_{IH}	X	High-Z
Word Prog.	Program	V_{PP}	V_{CC}	V_{IL}	V_{IH}	X	D_{IN}
	Program Verify	V_{PP}	V_{CC}	V_{IH}	V_{IL}	X	D_{OUT}
	Optional Verify	V_{PP}	V_{CC}	V_{IL}	V_{IL}	X	D_{OUT}
	Program Inhibit	V_{PP}	V_{CC}	V_{IH}	V_{IH}	X	High-Z
Identifier		V_{SS}-V_{CC}	V_{CC}	V_{IL}	V_{IL}	V_H	ID

Notes: 1. X = Don't Care. V_{PP} = 0 V to V_{CC}.
2. 11.5 V ≤ V_H ≤ 12.5 V

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Programming Voltage [1]	V_{PP}	-0.6 to +13.5	V
All Input and Output Voltage [1,2]	V_{IN}, V_{OUT}	-0.6 to +7.0	V
A_9 and $\overline{OE}$ Voltage [2]	V_{ID}	-0.6 to +13.0	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range [3]	T_{STG}	-65 to +125 [4] -55 to +125 [5]	°C
Storage Temperature Under Bias	T_{BIAS}	0 to +80	°C

Notes: 1. Relative to V_{SS}.
2. V_{IN}, V_{OUT}, and V_{ID} min = -2.0V for pulse width ≤ 20 ns.
3. Device storage temperature range before programming.
4. HN27C4096G and HN27C4096CC.
5. HN27C4096CP.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	-	-	12	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	-	-	20	pF	V_{OUT} = 0V

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{IN} = 5.5 V
Output Leakage Current	I_{LO}	-	-	2	µA	V_{OUT} = 5.5 V/0.45 V
Operating V_{CC} Current	I_{CC1}	-	-	30	mA	I_{OUT} = 0 mA, f = 1 MHz
	I_{CC2}	-	-	100	mA	I_{OUT} = 0 mA, f = 10 MHz
Standby V_{CC} Current	I_{SB1}	-	-	1	mA	$\overline{CE}$ = V_{IH}
	I_{SB2}	-	1	20	µA	$\overline{CE}$ = V_{CC} ± 0.3 V
V_{PP} Current	I_{PP1}	-	1	20	µA	V_{PP} = 5.5 V
Input Voltage	V_{IH}	2.2	-	V_{CC} + 1 [2]	V	
	V_{IL}	-0.3 [1]	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA
	V_{OL}	-	-	0.45	V	I_{OL} = 2.1 mA

Notes: 1. V_{IL} min = -1.0 V for pulse width ≤ 50 ns.
V_{IL} min = -2.0 V for pulse width ≤ 20 ns.
2. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns.
If V_{IH} is over the specified maximum value, Read operation can not be guaranteed.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

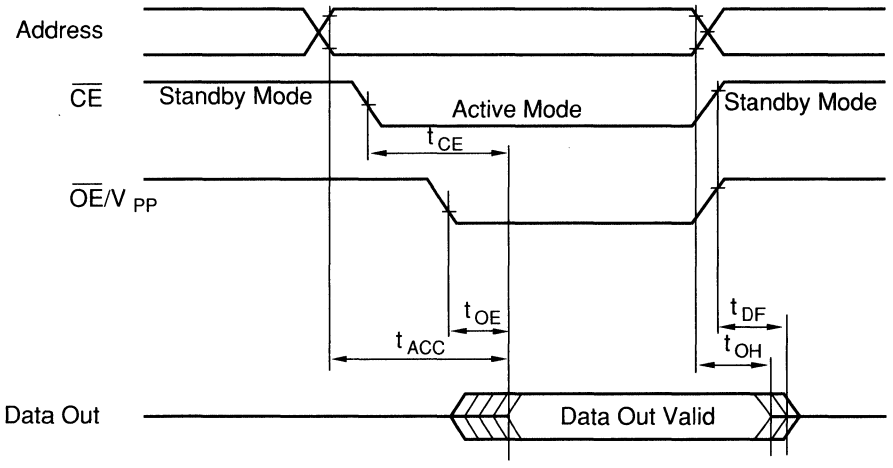
Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V/2.0 V

Item	Symbol	HN27C4096-10		HN27C4096-12		HN27C4096-12		Unit	Test Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
Address Access Time	t_{ACC}	-	100	-	120	-	150	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
Chip Enable Access Time	t_{CE}	-	100	-	120	-	150	ns	$\overline{OE}$ = V_{IL}
Output Enable Access Time	t_{OE}	-	60	-	60	-	70	ns	$\overline{CE}$ = V_{IL}
Output Disable to High-Z [1]	t_{DF}	0	35	0	40	0	50	ns	$\overline{CE}$ = V_{IL}
Output Hold to Address Change	t_{OH}	5	-	5	-	5	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



(TD.R.HN27C4096)

■ DC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

(V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, T_a = 25 °C ± 5 °C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{IN} = 6.5 V/ 0.45 V
Operating V_{CC} Current	I_{CC}	-	-	50	mA	
Operating V_{PP} Current	I_{PP}	-	-	70 [7]	mA	$\overline{CE}$ = V_{IL}
Input Voltage [3]	V_{IH}	2.2	-	V_{CC} +.5 [6]	V	
	V_{IL}	- 0.1[5]	-	0.8	V	
	V_H	11.5	12.0	12.5	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA
	V_{OL}	-	-	0.45	V	I_{OH} = 2.1 mA

Notes:
1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13 V, including overshoot.
3. Device reliability may be adversely affected if the device is installed or removed while V_{PP} = 12.5 V.
4. Do not change V_{PP} from V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = low.
5. V_{IL} min = -0.6 V for pulse width ≤ 20 ns.
6. If V_{IH} is over the specified maximum value, programming operation can not be guaranteed.
7. I_{PP} = 40 mA in Word Programming Mode.

■ AC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

(V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.5 v ± 0.3 V, T_a = 25°C ± 5°C)

Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 20 ns
- Reference levels for measuring timing: 0.8 V / 2.0V

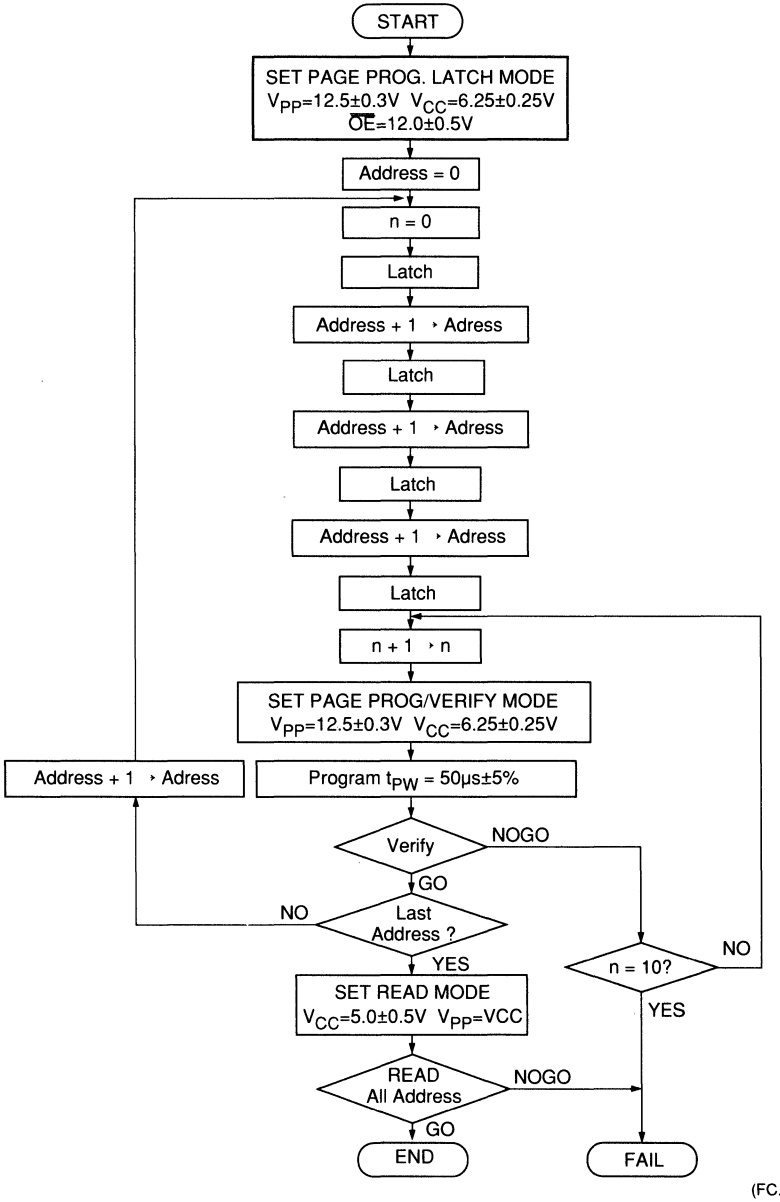
Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	2	-	-	µs	
Address Hold Time	t_{AH}	0	-	-	µs	
Data Setup Time	t_{DS}	2	-	-	µs	
Data Hold Time	t_{DH}	2	-	-	µs	
Chip Enable Setup Time	t_{CES}	2	-	-	µs	
V_{PP} Setup Time	t_{VPS}	2	-	-	µs	
V_{CC} Setup Time	t_{VCS}	2	-	-	µs	
Output Enable Setup Time	t_{OES}	2	-	-	µs	
Output Disable Time	t_{DF}	0	-	130	ns	
Programming Pulse Width	t_{PW}	47.5	50.0	52.5	µs	
Data Valid from Output Enable Time	t_{OE}	0	-	150	ns	
Chip Enable Pulse Width During Data Latch	t_{LW}	1	-	-	µs	
Output Enable = V_H Setup Time	t_{OHS}	2	-	-	µs	
Output Enable = V_H Hold Time	t_{OHH}	2	-	-	µs	
Output Enable Hold Time	t_{OEH}	2	-	-	µs	
V_{PP} Hold Time	t_{VRS}	1	-	-	µs	
Page Programming Reset Time	t_{VLW}	1	-	-	µs	

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.
2. Page Program Mode will be reset when V_{PP} is set to V_{CC} or less.

■ PAGE PROGRAMMING FLOWCHART

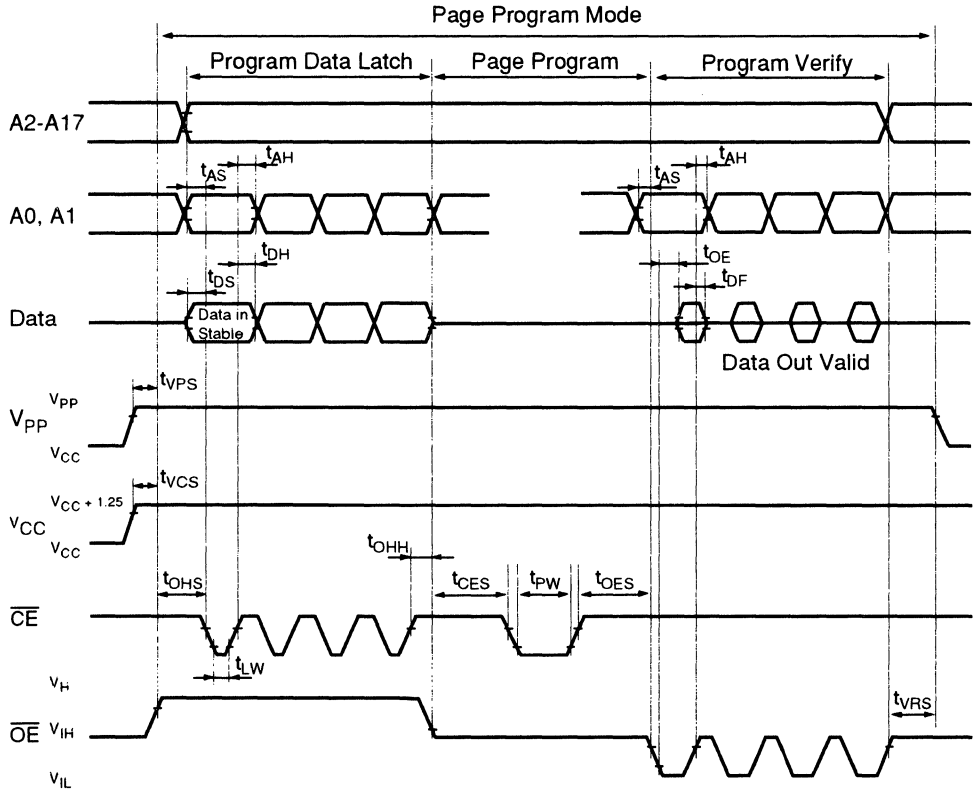
The Hitachi HN27C4096 can be programmed with the high performance Page Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.

Note: 1. To set the device into Page Programming, apply 12.5 V to V_{PP} then followed by applying 12 V to $\overline{OE}$. The device operates in Page Program Mode until reset.
2. To reset the Page Program Mode, set $V_{PP} = V_{CC}$ or less.



(FC.PP.HN27C4096)

■ PAGE PROGRAMMING TIMING WAVEFORM

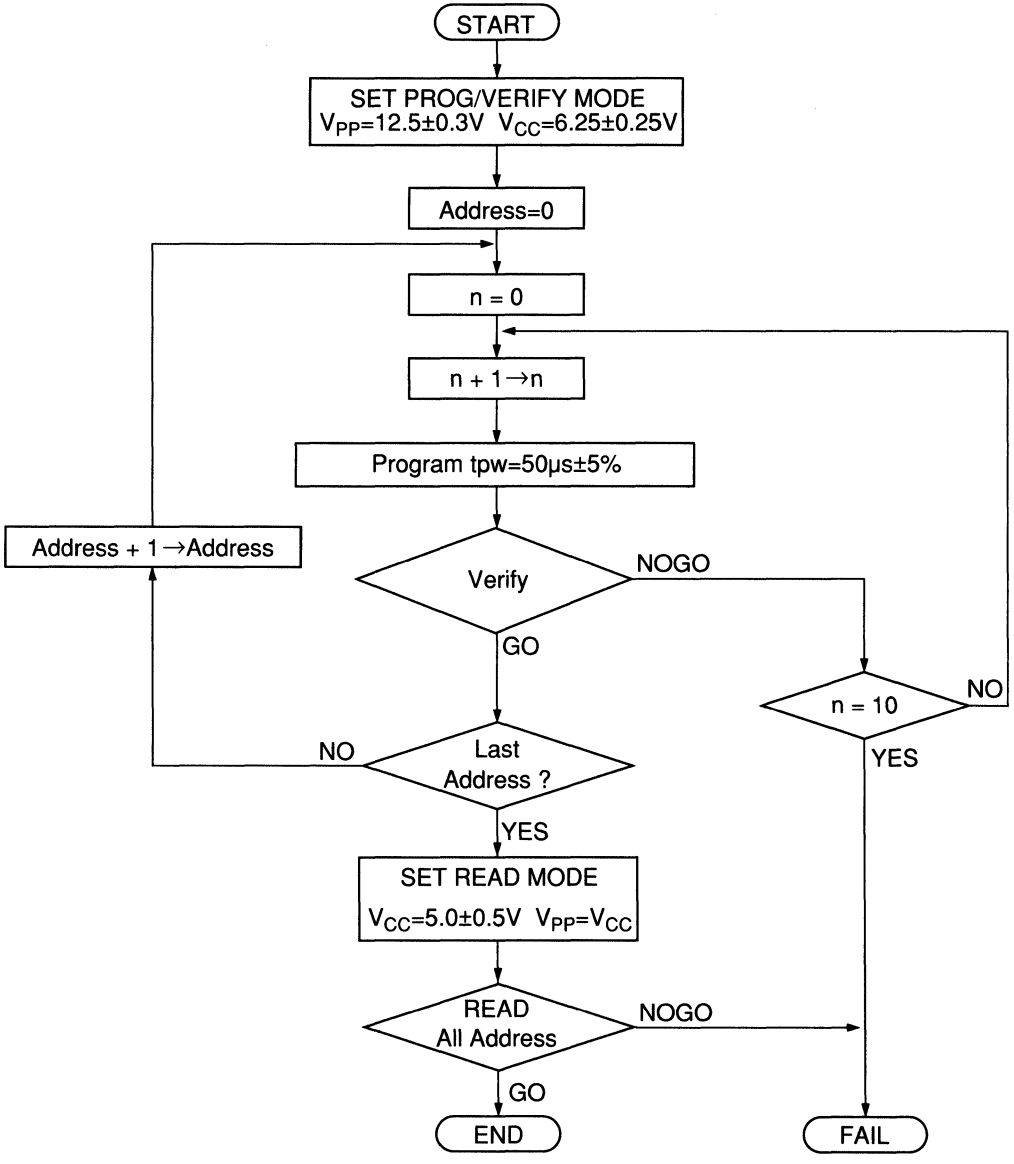


(TD.PP.HN27C4096)

4

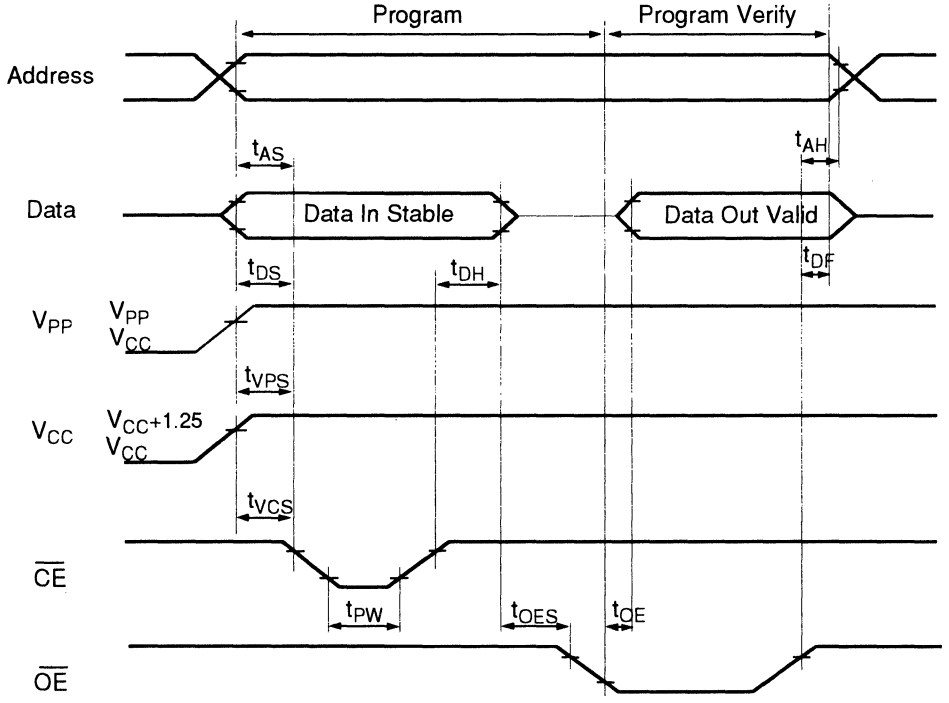
■ WORD PROGRAMMING FLOWCHART

The Hitachi HN27C4096 can be programmed with the high performance Word Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.



(FC.P.HN27C4096)

■ WORD PROGRAMMING TIMING WAVEFORM



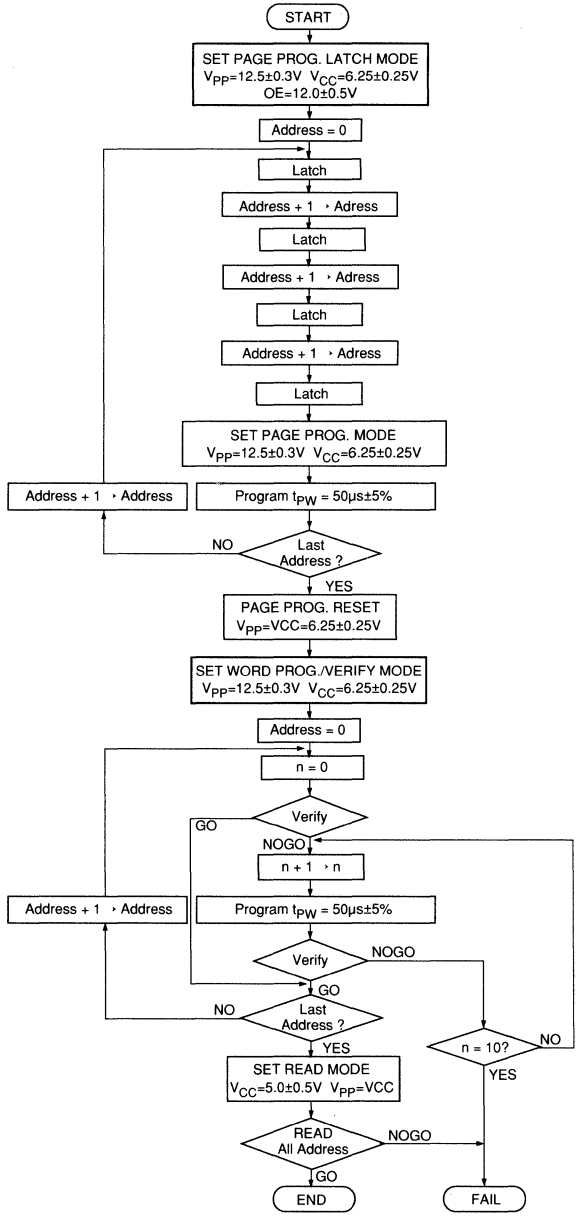
(TD.P.HN27C4096)

■ OPTIONAL PAGE PROGRAMMING FLOWCHART

The Hitachi HN27C4096 can be programmed with the high performance Optional Page Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.

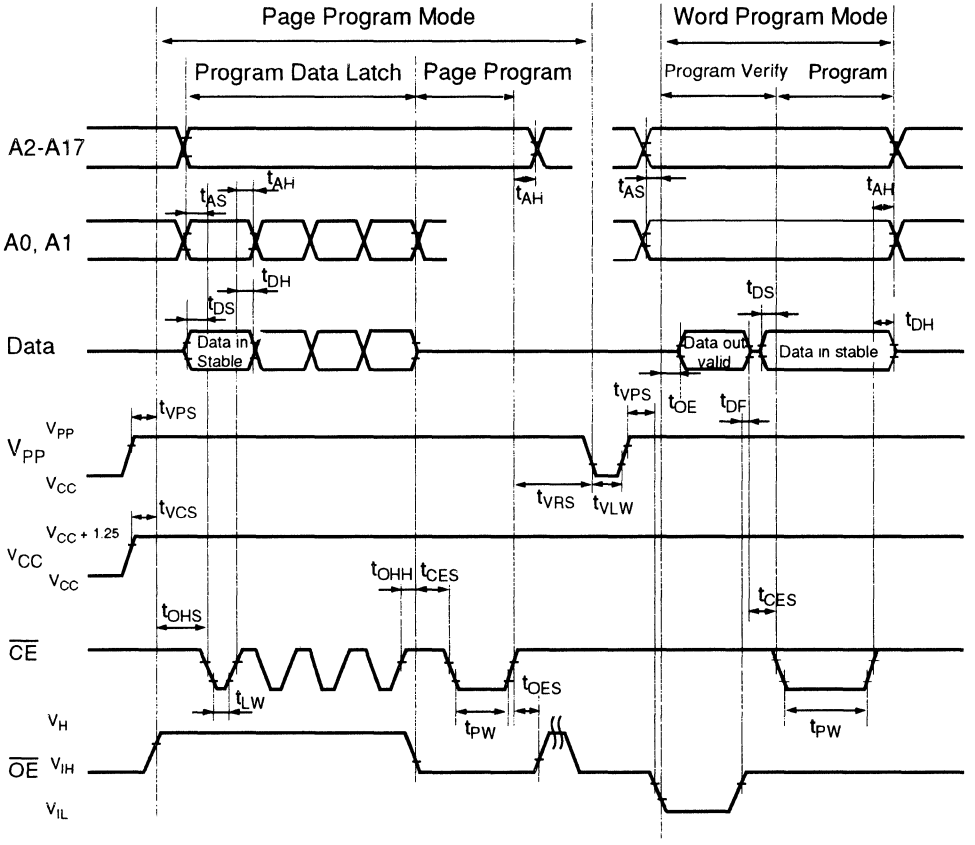
This programming algorithm is a combination of Page Programming and Word Verify. It can be used to avoid the increased programming verify time when a programmer with a slower machine cycle is used and shorten the total programming time.

Please refer to the timing specifications for page programming and word programming.



(FC.OPP.HN27C4096)

■ OPTIONAL PAGE PROGRAMMING TIMING WAVEFORM



(TD.OPP.HN27C4096)

4

■ ERASING THE HN27C4096

The Hitachi HN27C4096 Ceramic DIP and Ceramic LCC packages allow these devices to be erased by exposure to ultraviolet light of 2537Å. All of the data is changed to "1" after this erasure procedure. The minimum integrated dose (UV intensity x exposure time) for erasure is 15 W-sec/cm^2.

■ DEVICE IDENTIFIER MODE DESCRIPTION

The Device Identifier Mode allows binary codes to be read from the outputs that identify the manufacturer and the type of device. Using this mode with programming equipment, the device will automatically match its own erase and programming algorithm.

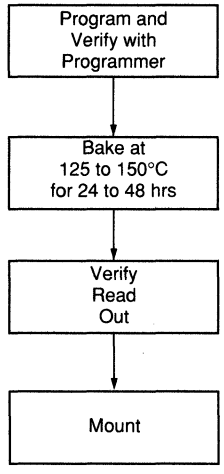
■ HN27C4096 SERIES IDENTIFIER CODE

Identifier	A_0	I/O_8-I/O_{15}	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Hex Data
Manufacturer Code	V_{IL}	X	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	X	1	0	1	0	0	0	1	0	A2

Notes: 1. V_{CC} = 5.0 V ± 10%
2. A_9 = 12.0 V ± 0.5V
3. A_1-A_8, A_{10}-A_{17}, $\overline{CE}$, $\overline{OE}$ = V_{IL}
4. X = Don't Care

■ HN27C4096CP RECOMMENDED SCREENING CONDITIONS

Before mounting the HN27C4096CP package, please make the following screening (baking without bias) shown below:



(RSC.EPROM)

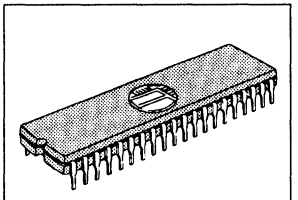
4M (256K x 16-bit) UV EPROM

■ DESCRIPTION

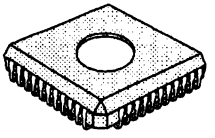
The Hitachi HN27C4096H is a 4-Megabit Ultraviolet Erasable and Electrically Programmable Read Only Memory organized as 262,144 x 16-bits.

The HN27C4096H features high speed access times of 70 and 85 ns and low power dissipation. This combination makes the HN27C4096H suitable for high speed 16 and 32-bit microcomputer systems. The HN27C4096H offers high speed programming using page programming mode.

Hitachi's HN27C4096H is offered in JEDEC-Standard Word-Wide EPROM pinouts in 40-pin Ceramic DIP and 44-lead Ceramic LCC packages. This allows socket replacement with Mask ROMs.



(DG-40A)



(CC-44)

■ FEATURES

- High Speed Access Times:
  85 ns (max)
- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Low Power Dissipation:
  Active Mode: 35 mW/MHz (typ)
  Standby Mode: 30 mA (max)
- High Speed Page and Word Programming:
  Page Programming Time: 3.5 sec (min)
- Programming Power Supply:
  V_{PP} = 12.5 V ± 0.3 V
- Pin Arrangement:
  JEDEC Standard Word-Wide EPROM
  Mask ROM Compatible
- Packages:
  40-pin Ceramic DIP
  44-lead Ceramic LCC

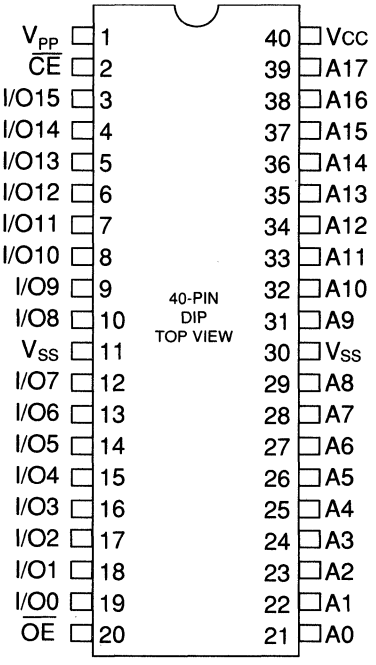
■ ORDERING INFORMATION

Type No.	Access Time	Package
HN27C4096HG-85	85 ns	40-pin Ceramic DIP (DG-40A)
HN27C4096HCC-85	85 ns	44-lead Ceramic LCC (CC-44)

4

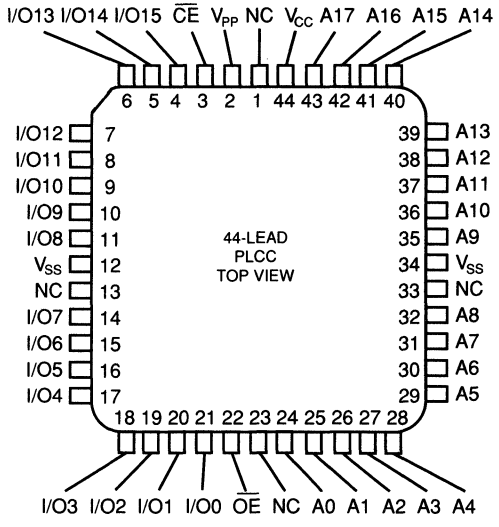
■ PIN ARRANGEMENT

HN27C4096HG Series



(PinD40.HN27C4096H)

HN27C4096HCC Series

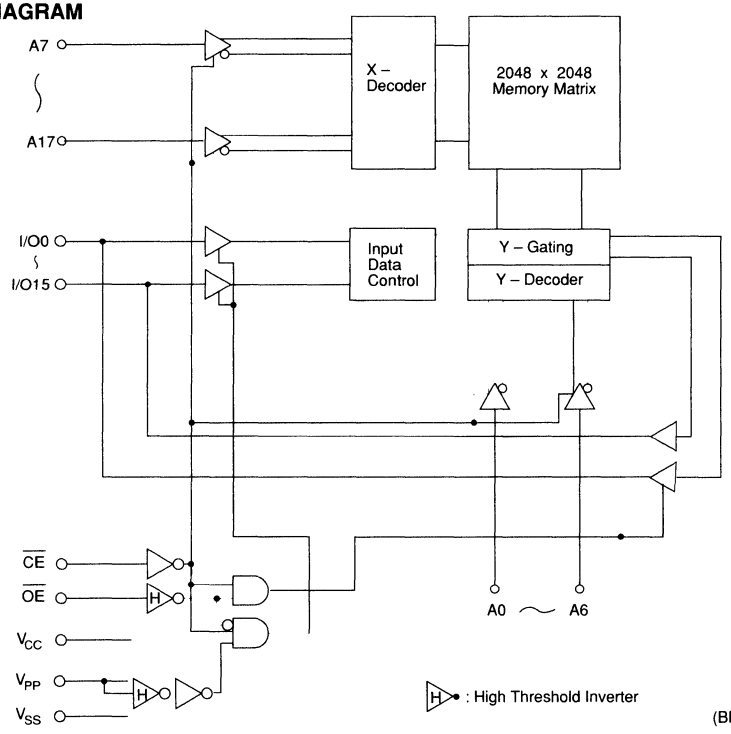


(PinQ44.HN27C4096H)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{17}	Address
I/O_0 - I/O_{15}	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{PP}	Programming Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



(BD.HN27C4096H)

■ MODE SELECTION

Mode		V_{PP}	V_{CC}	$\overline{CE}$	$\overline{OE}$	A_9	I/O
Read		V_{SS}-V_{CC}	V_{CC}	V_{IL}	V_{IL}	X[1]	D_{OUT}
Output Disable		V_{SS}-V_{CC}	V_{CC}	V_{IL}	V_{IH}	X	High-Z
Standby		V_{SS}-V_{CC}	V_{CC}	V_{IH}	X	X	High-Z
Page Prog.	Page Prog. Set	V_{PP}	V_{CC}	V_{IH}	V_H[2]	X	High-Z
	Page Data Latch	V_{PP}	V_{CC}	V_{IL}	V_H	X	D_{IN}
	Page Program	V_{PP}	V_{CC}	V_{IL}	V_{IH}	X	High-Z
	Page Prog. Verify	V_{PP}	V_{CC}	V_{IH}	V_{IL}	X	D_{OUT}
	Page Prog. Reset	V_{CC}	V_{CC}	V_{IH}	V_{IH}	X	High-Z
Word Prog.	Program	V_{PP}	V_{CC}	V_{IL}	V_{IH}	X	D_{IN}
	Program Verify	V_{PP}	V_{CC}	V_{IH}	V_{IL}	X	D_{OUT}
	Optional Verify	V_{PP}	V_{CC}	V_{IL}	V_{IL}	X	D_{OUT}
	Program Inhibit	V_{PP}	V_{CC}	V_{IH}	V_{IH}	X	High-Z
Identifier		V_{SS}-V_{CC}	V_{CC}	V_{IL}	V_{IL}	V_H	ID

Notes: 1. X = Don't Care. V_{PP} = 0 V to V_{CC}.
2. 11.5 V ≤ V_H ≤ 12.5 V

4

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Programming Voltage [1]	V_{PP}	-0.6 to +13.5	V
All Input and Output Voltage [1,2]	V_{IN}, V_{OUT}	-0.6 to +7.0	V
A_9 and $\overline{OE}$ Voltage [2]	V_{ID}	-0.6 to +13.0	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range [3]	T_{STG}	-65 to +125	°C
Storage Temperature Under Bias	T_{BIAS}	0 to +80	°C

Notes: 1. Relative to V_{SS}.
2. V_{IN}, V_{OUT}, and V_{ID} min = -2.0V for pulse width ≤ 20 ns.
3. Device storage temperature range before programming.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	-	-	12	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	-	-	20	pF	V_{OUT} = 0V

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{IN} = 5.5 V
Output Leakage Current	I_{LO}	-	-	2	µA	V_{OUT} = 5.5 V/0.45 V
Operating V_{CC} Current	I_{CC1}	-	-	30	mA	I_{OUT} = 0 mA, f = 1 MHz
	I_{CC2}	-	-	120	mA	I_{OUT} = 0 mA, f = 11.8 MHz
Standby V_{CC} Current	I_{SB}	-	-	30	mA	$\overline{CE}$ = V_{IH}
V_{PP} Current	I_{PP1}	-	1	20	µA	V_{PP} = 5.5 V
Input Voltage	V_{IH}	2.2	-	V_{CC} + 1 [2]	V	
	V_{IL}	-0.3 [1]	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA
	V_{OL}	-	-	0.45	V	I_{OL} = 2.1 mA

Notes: 1. V_{IL} min = -1.0 V for pulse width ≤ 50 ns.
V_{IL} min = -2.0 V for pulse width ≤ 20 ns.
2. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns.
If V_{IH} is over the specified maximum value, Read operation can not be guaranteed.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

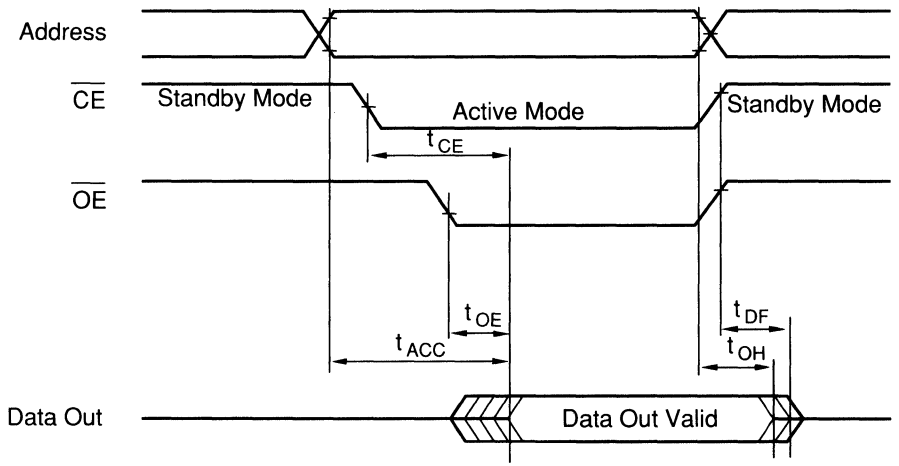
Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 1.5 V

Item	Symbol	HN27C4096H-85 Min.	HN27C4096H-85 Max.	Unit	Test Condition
Address Access Time	t_{ACC}	-	85	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
Chip Enable Access Time	t_{CE}	-	85	ns	$\overline{OE}$ = V_{IL}
Output Enable Access Time	t_{OE}	-	45	ns	$\overline{CE}$ = V_{IL}
Output Disable to High-Z [1]	t_{DF}	0	30	ns	$\overline{CE}$ = V_{IL}
Output Hold to Address Change	t_{OH}	5	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



(TD.R.HN27C4096H)

■ DC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

(V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, T_a = 25 °C ± 5 °C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{IN} = 6.5 V/ 0.45 V
Operating V_{CC} Current	I_{CC}	-	-	50	mA	
Operating V_{PP} Current	I_{PP}	-	-	70 [7]	mA	$\overline{CE}$ = V_{IL}
Input Voltage [3]	V_{IH}	2.2	-	V_{CC} +.5 [6]	V	
	V_{IL}	- 0.1[5]	-	0.8	V	
	V_H	11.5	12.0	12.5	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA
	V_{OL}	-	-	0.45	V	I_{OH} = 2.1 mA

Notes:
1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13 V, including overshoot.
3. Device reliability may be adversely affected if the device is installed or removed while V_{PP} = 12.5 V.
4. Do not change V_{PP} from V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = low.
5. V_{IL} min = -0.6 V for pulse width ≤ 20 ns.
6. If V_{IH} is over the specified maximum value, programming operation can not be guaranteed.
7. I_{PP} = 40 mA in Word Programming Mode.

■ AC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

(V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.5 v ± 0.3 V, T_a = 25°C ± 5°C)

Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 20 ns
- Reference levels for measuring timing: 0.8 V / 2.0V

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	2	-	-	µs	
Address Hold Time	t_{AH}	0	-	-	µs	
Data Setup Time	t_{DS}	2	-	-	µs	
Data Hold Time	t_{DH}	2	-	-	µs	
Chip Enable Setup Time	t_{CES}	2	-	-	µs	
V_{PP} Setup Time	t_{VPS}	2	-	-	µs	
V_{CC} Setup Time	t_{VCS}	2	-	-	µs	
Output Enable Setup Time	t_{OES}	2	-	-	µs	
Output Disable Time	t_{DF}	0	-	130	ns	
Programming Pulse Width	t_{PW}	47.5	50.0	52.5	µs	
Data Valid from Output Enable Time	t_{OE}	0	-	150	ns	
Chip Enable Pulse Width During Data Latch	t_{LW}	1	-	-	µs	
Output Enable = V_H Setup Time	t_{OHS}	2	-	-	µs	
Output Enable = V_H Hold Time	t_{OHH}	2	-	-	µs	
Output Enable Hold Time	t_{OEH}	2	-	-	µs	
V_{PP} Hold Time	t_{VRS}	1	-	-	µs	
Page Programming Reset Time	t_{VLW}	1	-	-	µs	

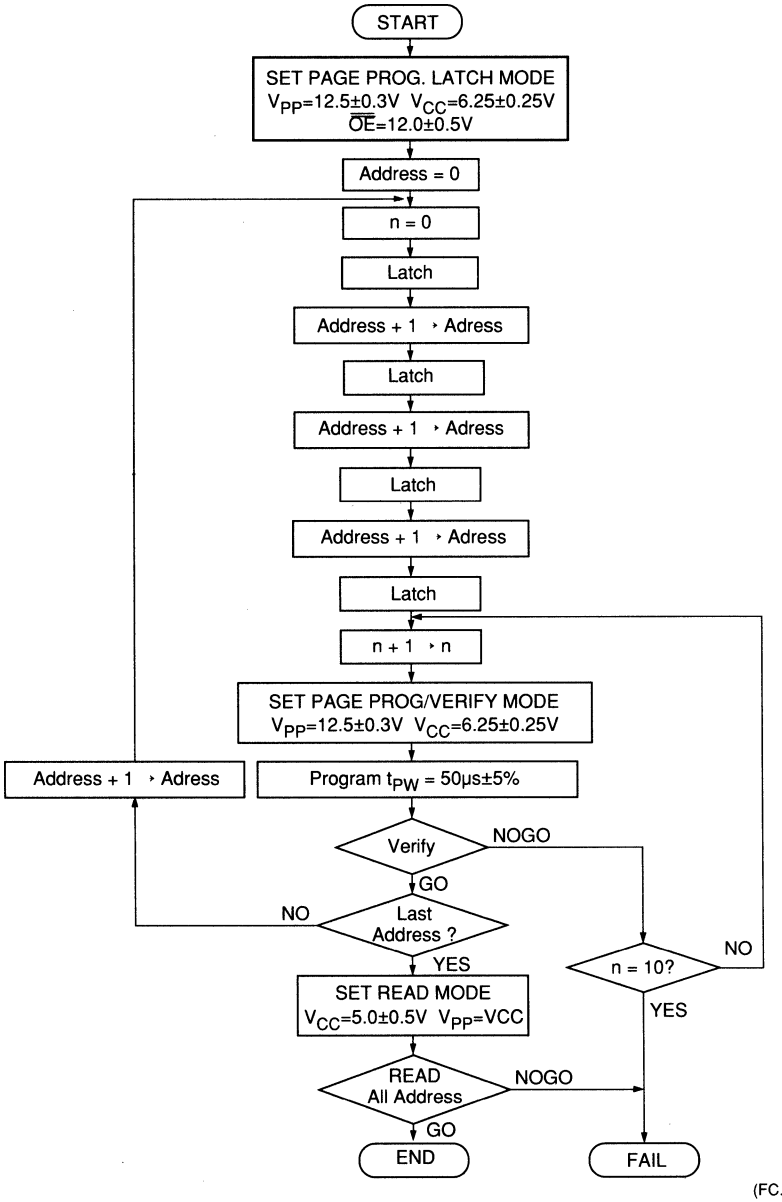
Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.
2. Page Program Mode will be reset when V_{PP} is set to V_{CC} or less.

4

■ PAGE PROGRAMMING FLOWCHART

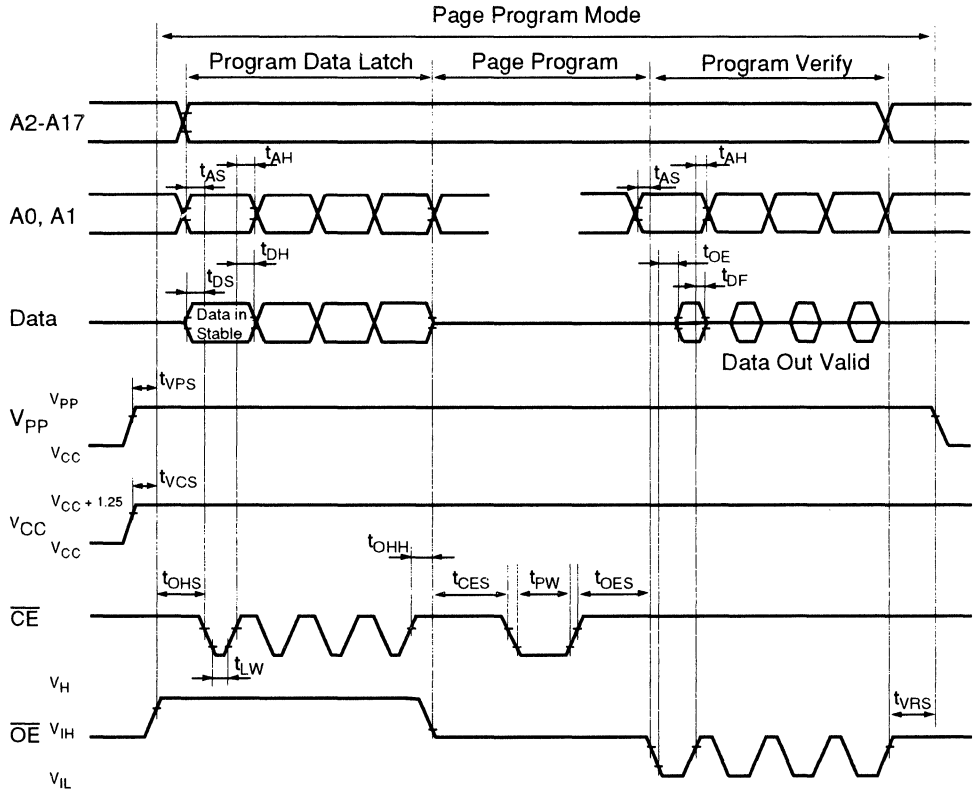
The Hitachi HN27C4096H can be programmed with the high performance Page Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.

Note: 1. To set the device into Page Programming, apply 12.5 V to V_{PP} then followed by applying 12 V to $\overline{OE}$. The device operates in Page Program Mode until reset.
2. To reset the Page Program Mode, set $V_{PP} = V_{CC}$ or less.



(FC.PP.HN27C4096H)

■ PAGE PROGRAMMING TIMING WAVEFORM

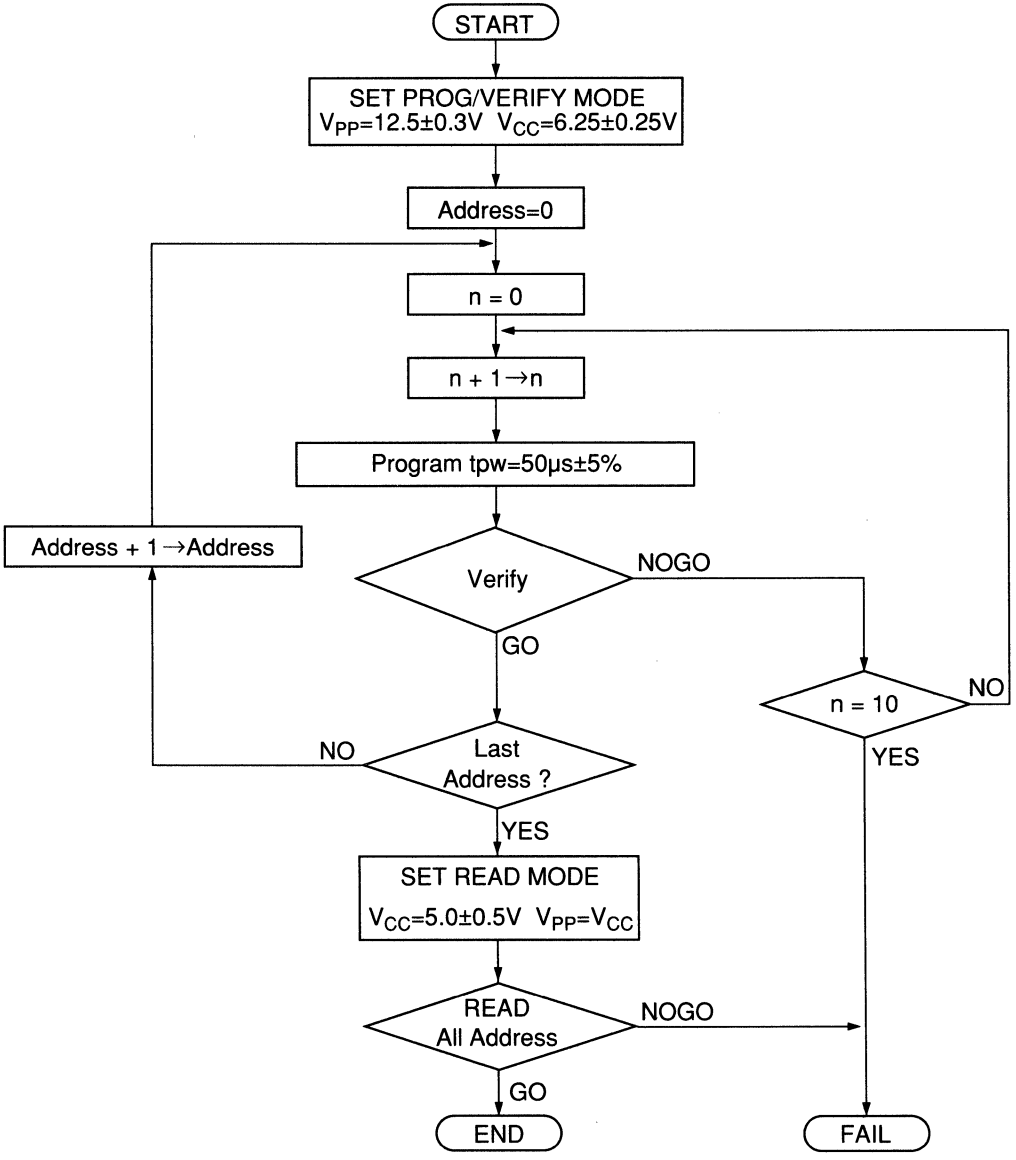


(TD.PP.HN27C4096H)

4

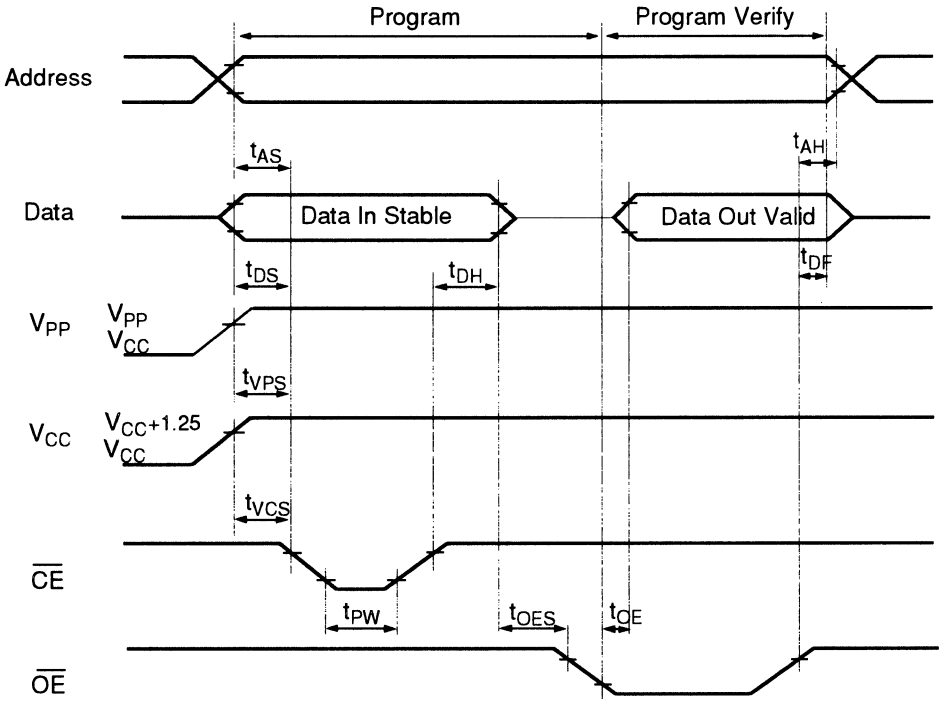
■ WORD PROGRAMMING FLOWCHART

The Hitachi HN27C4096H can be programmed with the high performance Word Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.



(FC.P.HN27C4096H)

■ WORD PROGRAMMING TIMING WAVEFORM



(TD.P.HN27C4096H)

4

■ OPTIONAL PAGE PROGRAMMING FLOWCHART

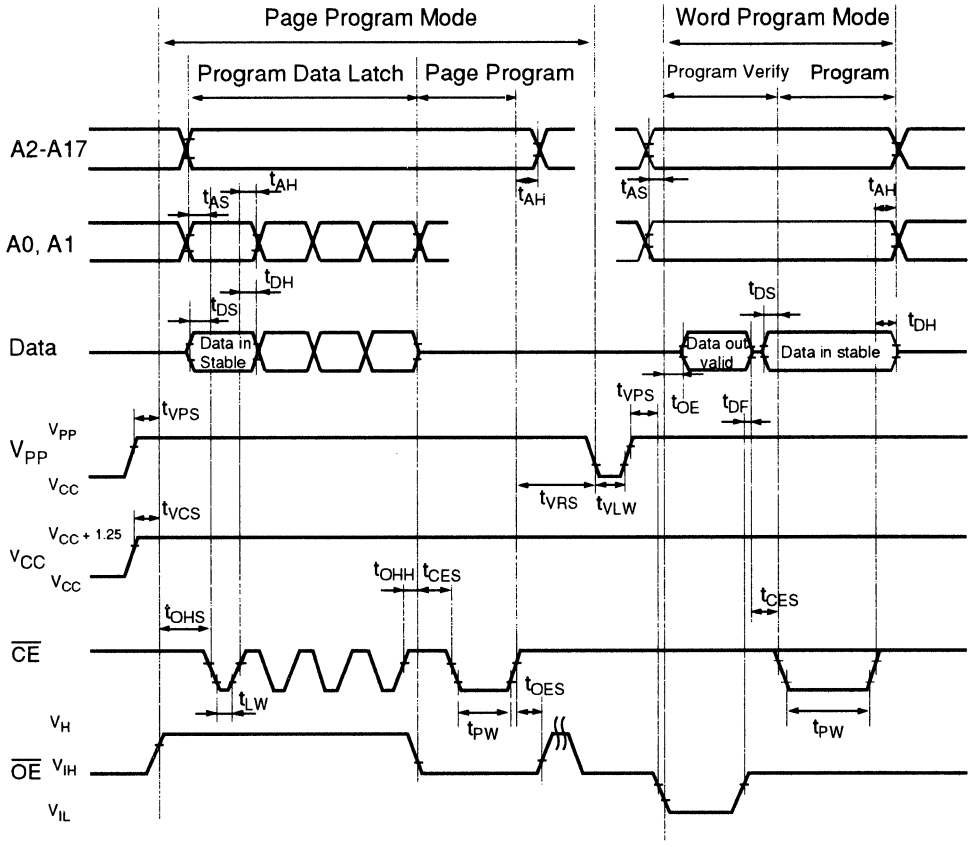
The Hitachi HN27C4096H can be programmed with the high performance Optional Page Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.

This programming algorithm is a combination of Page Programming and Word Verify. It can be used to avoid the increased programming verify time when a programmer with a slower machine cycle is used and shorten the total programming time.

Please refer to the timing specifications for page programming and word programming.

(FC.OPP.HN27C4096H)

■ OPTIONAL PAGE PROGRAMMING TIMING WAVEFORM



(TD.OPP.HN27C4096H)

4

■ ERASING THE HN27C4096H

The Hitachi HN27C4096H is erased by exposure to ultraviolet light of 2537Å. All of the data is changed to "1" after this erasure procedure. The minimum integrated dose (UV intensity x exposure time) for erasure is 15 W-sec/cm^2.

■ DEVICE IDENTIFIER MODE DESCRIPTION

The Device Identifier Mode allows binary codes to be read from the outputs that identify the manufacturer and the type of device. Using this mode with programming equipment, the device will automatically match its own erase and programming algorithm.

■ HN27C4096H SERIES IDENTIFIER CODE

Identifier	A_0	I/O_8-I/O_{15}	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Hex Data
Manufacturer Code	V_{IL}	X	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	X	1	0	1	0	0	0	1	0	A2

Notes:
1. V_{CC} = 5.0 V ± 10%
2. A_9 = 12.0 V ± 0.5V
3. A_1-A_8, A_{10}-A_{17}, $\overline{CE}$, $\overline{OE}$ = V_{IL}
4. X = Don't Care

HN27C4001 Series

4M (512K x 8-bit) UV and OTP EPROM

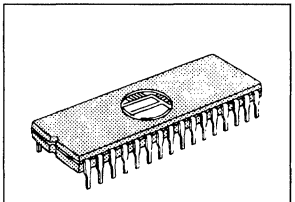
■ DESCRIPTION

The Hitachi HN27C4001 is a 4-Megabit Ultraviolet Erasable and One-Time Programmable Electrically Programmable Read Only Memory organized as 524,288 x 8-bits.

The HN27C4001 features fast address access times of 100, 120 and 150 ns and low power dissipation. This combination makes the HN27C4001 suitable for high speed 16 and 32-bit microcomputer systems. The HN27C4001 offers high speed programming using page programming mode.

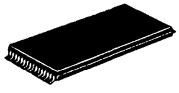
Hitachi's HN27C4001 is offered in JEDEC-Standard Byte-Wide EPROM pinouts in 32-pin Ceramic DIP. This allows socket replacement with Mask ROMs and Flash Memory. The HN27C4001 is also available in 32-lead Plastic TSOP packages with both standard and reverse bend leads.

The Ceramic DIP package is erasable by exposure to Ultraviolet light. The TSOP packaged device is One-Time Programmable and once programmed, can not be rewritten.



(DG-32)

(TFP-32D)



(TFP-32DR)

■ FEATURES

- Fast Access Times:
  100 ns/120 ns/150 ns (max)
- Single Power Supply:
  V_{CC} = 5 V ± 10%
- Low Power Dissipation:
  Active Mode: 35 mW/MHz (typ)
  Standby Mode: 5 µW (max)
- High Speed Page and Word Programming:
  Page Programming Time: 3.5 sec (min)
- Programming Power Supply:
  V_{PP} = 12.5 V ± 0.3 V
- Pin Arrangement:
  JEDEC Standard Byte-Wide EPROM
  Mask ROM and Flash Memory Compatible
- Packages:
  32-pin Ceramic DIP
  32-lead Plastic TSOP (Type II)

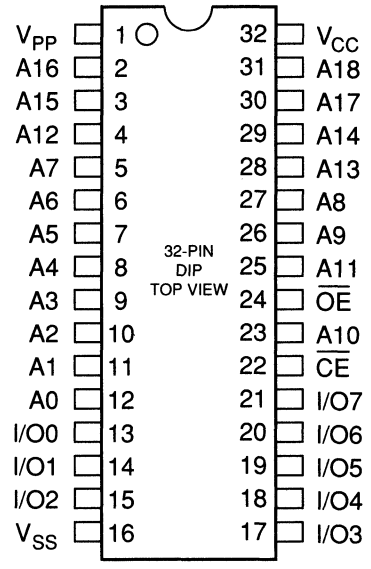
■ ORDERING INFORMATION

Type No.	Access Time	Package
HN27C4001G-10	100 ns	32-pin Ceramic DIP
HN27C4001G-12	120 ns	(DG-32)
HN27C4001G-15	150 ns	
HN27C4001TT-12	120 ns	32-lead Plastic TSOP
HN27C4001TT-15	150 ns	(TFP-32D)
HN27C4001RR-12	120 ns	32-lead Plastic TSOP
HN27C4001RR-15	150 ns	(TFP-32D)
		Reverse bend

4

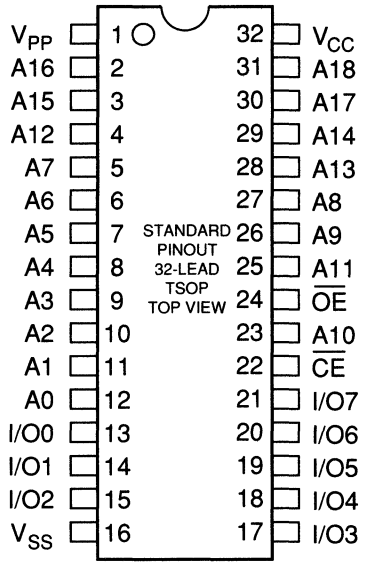
■ PIN ARRANGEMENT

HN27C4001G Series



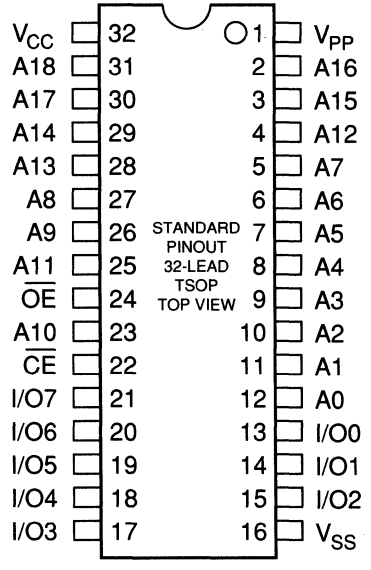
(PinD32.HN27C4001)

HN27C4001TT Series



(PinT232.HN27C4001T)

HN27C4001RR Series

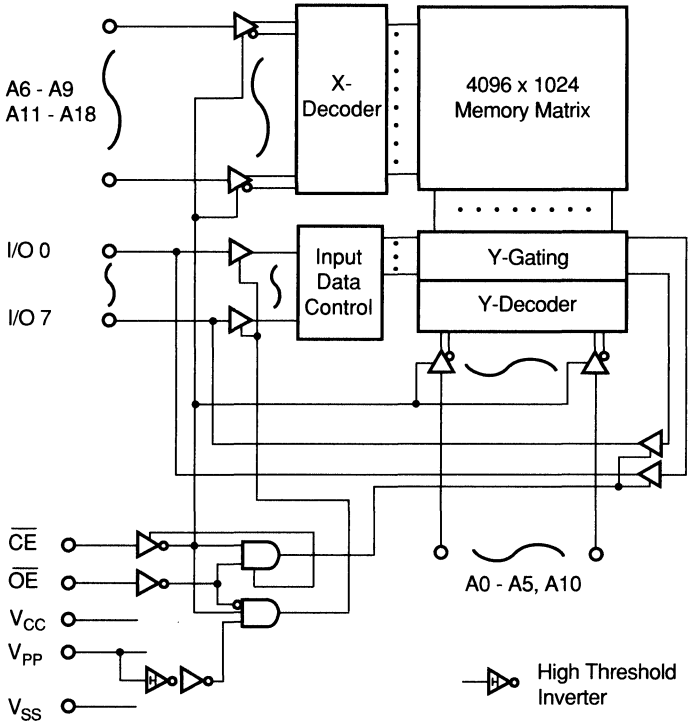


(PinT232.HN27C4001R)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{18}	Address
I/O_0 - I/O_7	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{PP}	Programming Supply
V_{SS}	Ground

■ BLOCK DIAGRAM



■ MODE SELECTION

Mode		V_{PP}	V_{CC}	$\overline{CE}$	$\overline{OE}$	A_9	I/O
Read		V_{SS}-V_{CC}	V_{CC}	V_{IL}	V_{IL}	X[1]	D_{OUT}
Output Disable		V_{SS}-V_{CC}	V_{CC}	V_{IL}	V_{IH}	X	High-Z
Standby		V_{SS}-V_{CC}	V_{CC}	V_{IH}	X	X	High-Z
Page Prog.	Page Prog. Set	V_{PP}	V_{CC}	V_{IH}	V_H[2]	X	High-Z
	Page Data Latch	V_{PP}	V_{CC}	V_{IL}	V_H	X	D_{IN}
	Page Program	V_{PP}	V_{CC}	V_{IL}	V_{IH}	X	High-Z
	Page Prog. Verify	V_{PP}	V_{CC}	V_{IH}	V_{IL}	X	D_{OUT}
	Page Prog. Reset	V_{CC}	V_{CC}	V_{IH}	V_{IH}	X	High-Z
Word Prog.	Program	V_{PP}	V_{CC}	V_{IL}	V_{IH}	X	D_{IN}
	Program Verify	V_{PP}	V_{CC}	V_{IH}	V_{IL}	X	D_{OUT}
	Optional Verify	V_{PP}	V_{CC}	V_{IL}	V_{IL}	X	D_{OUT}
	Program Inhibit	V_{PP}	V_{CC}	V_{IH}	V_{IH}	X	High-Z
Identifier		V_{SS}-V_{CC}	V_{CC}	V_{IL}	V_{IL}	V_H	ID

Notes: 1. X = Don't Care. V_{PP} = 0 V to V_{CC}.
2. 11.5 V ≤ V_H ≤ 12.5 V

4

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Programming Voltage [1]	V_{PP}	-0.6 to +13.5	V
All Input and Output Voltage [1,2]	V_{IN}, V_{OUT}	-0.6 to +7.0	V
A_9 and $\overline{OE}$ Voltage [2]	V_{ID}	-0.6 to +13.0	V
Operating Temperature Range	T_{OPR}	0 to +70	°C
Storage Temperature Range [3]	T_{STG}	-65 to +125 [4] -55 to +125 [5]	°C
Storage Temperature Under Bias	T_{BIAS}	-20 to +80 [4] -10 to +80 [5]	°C

Notes: 1. Relative to V_{SS}.
2. V_{IN}, V_{OUT}, and V_{ID} min = -2.0V for pulse width ≤ 20 ns.
3. Device storage temperature range before programming.
4. HN27C4001G.
5. HN27C4001TT and HN27C4001RR.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	-	-	12	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	-	-	20	pF	V_{OUT} = 0V

■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{IN} = 5.5 V
Output Leakage Current	I_{LO}	-	-	2	µA	V_{OUT} = 5.5 V/0.45 V
Operating V_{CC} Current	I_{CC1}	-	-	30	mA	I_{OUT} = 0 mA, f = 1 MHz
	I_{CC2}	-	-	100 [3] 90 [4]	mA mA	I_{OUT} = 0 mA, f = 10 MHz I_{OUT} = 0 mA, f = 8.4 MHz
Standby V_{CC} Current	I_{SB1}	-	-	1	mA	$\overline{CE}$ = V_{IH}
	I_{SB2}	-	1	20	µA	$\overline{CE}$ = V_{CC} ± 0.3 V
V_{PP} Current	I_{PP1}	-	1	20	µA	V_{PP} = 5.5 V
Input Voltage	V_{IH}	2.2	-	V_{CC} + 1 [2]	V	
	V_{IL}	-0.3 [1]	-	0.8	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA
	V_{OL}	-	-	0.45	V	I_{OL} = 2.1 mA

Notes: 1. V_{IL} min = -1.0 V for pulse width ≤ 50 ns.
V_{IL} min = -2.0 V for pulse width ≤ 20 ns.
2. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns.
If V_{IH} is over the specified maximum value, Read operation can not be guaranteed.
3. HN27C4001G.
4. HN27C4001TT and HN27C4001RR.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(V_{CC} = 5V ± 10%, V_{PP} = V_{SS} to V_{CC}, T_a = 0 to 70°C)

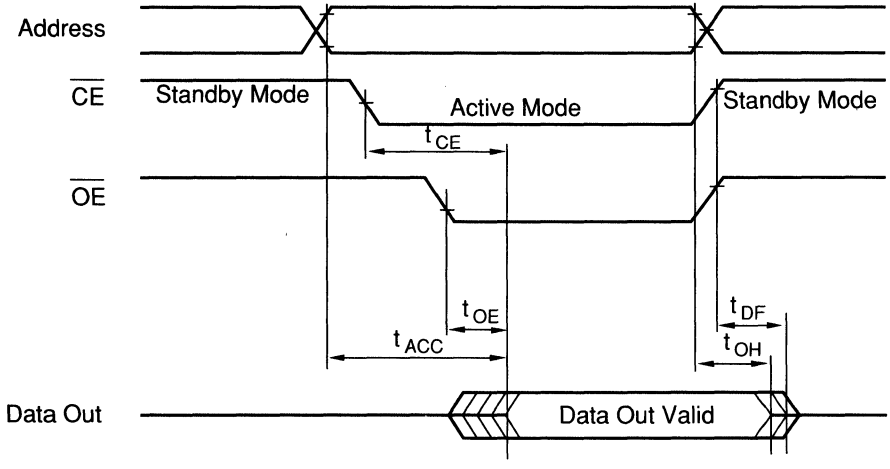
Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V/2.0 V

Item	Symbol	HN27C4001-10		HN27C4001-12		HN27C4001-15		Unit	Test Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
Address Access Time	t_{ACC}	-	100	-	120	-	150	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
Chip Enable Access Time	t_{CE}	-	100	-	120	-	150	ns	$\overline{OE}$ = V_{IL}
Output Enable Access Time	t_{OE}	-	60	-	60	-	70	ns	$\overline{CE}$ = V_{IL}
Output Disable to High-Z [1]	t_{DF}	0	35	0	40	0	50	ns	$\overline{CE}$ = V_{IL}
Output Hold to Address Change	t_{OH}	5	-	5	-	5	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



(TD.R.HN27C4001)

4

■ DC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

(V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, T_a = 25 °C ± 5 °C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{IN} = 6.5 V/ 0.45 V
Operating V_{CC} Current	I_{CC}	-	-	50	mA	
Operating V_{PP} Current	I_{PP}	-	-	70	mA	$\overline{CE}$ = V_{IL}
Input Voltage [3]	V_{IH}	2.2	-	V_{CC} +.5 [6]	V	
	V_{IL}	- 0.1[5]	-	0.8	V	
	V_H	11.5	12.0	12.5	V	
Output Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA
	V_{OL}	-	-	0.45	V	I_{OH} = 2.1 mA

Notes:
1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13 V, including overshoot.
3. Device reliability may be adversely affected if the device is installed or removed while V_{PP} = 12.5 V.
4. Do not change V_{PP} from V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = low.
5. V_{IL} min = -0.6 V for pulse width ≤ 20 ns.
6. If V_{IH} is over the specified maximum value, programming operation can not be guaranteed.

■ AC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

(V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.5 v ± 0.3 V, T_a = 25°C ± 5°C)

Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times: ≤ 20 ns
- Reference levels for measuring timing: 0.8 V / 2.0V

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	2	-	-	µs	
Address Hold Time	t_{AH}	0	-	-	µs	
Data Setup Time	t_{DS}	2	-	-	µs	
Data Hold Time	t_{DH}	2	-	-	µs	
Chip Enable Setup Time	t_{CES}	2	-	-	µs	
V_{PP} Setup Time	t_{VPS}	2	-	-	µs	
V_{CC} Setup Time	t_{VCS}	2	-	-	µs	
Output Enable Setup Time	t_{OES}	2	-	-	µs	
Output Disable Time	t_{DF}	0	-	130	ns	
Programming Pulse Width	t_{PW}	47.5	50.0	52.5	µs	
Data Valid from Output Enable Time	t_{OE}	0	-	150	ns	
Chip Enable Pulse Width During Data Latch	t_{LW}	1	-	-	µs	
Output Enable = V_H Setup Time	t_{OHS}	2	-	-	µs	
Output Enable = V_H Hold Time	t_{OHH}	2	-	-	µs	
Output Enable Hold Time	t_{OEH}	2	-	-	µs	
V_{PP} Hold Time	t_{VRS}	1	-	-	µs	
Page Programming Reset Time	t_{VLW}	1	-	-	µs	

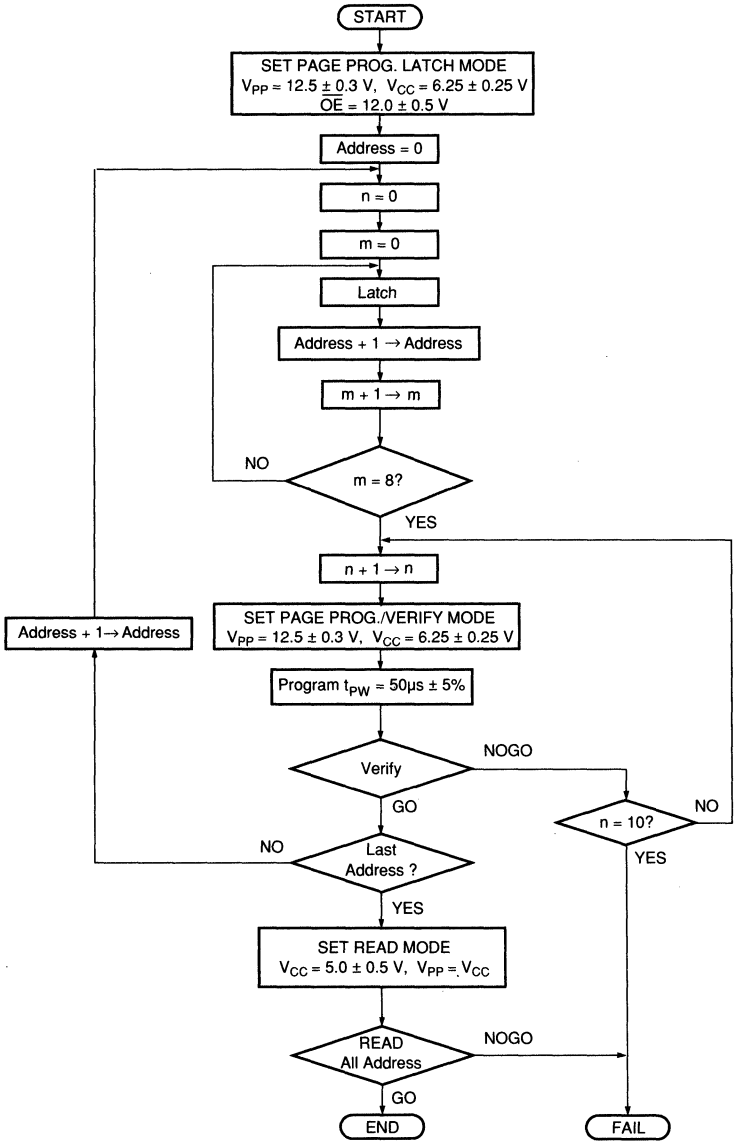
Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

4

■ PAGE PROGRAMMING FLOWCHART

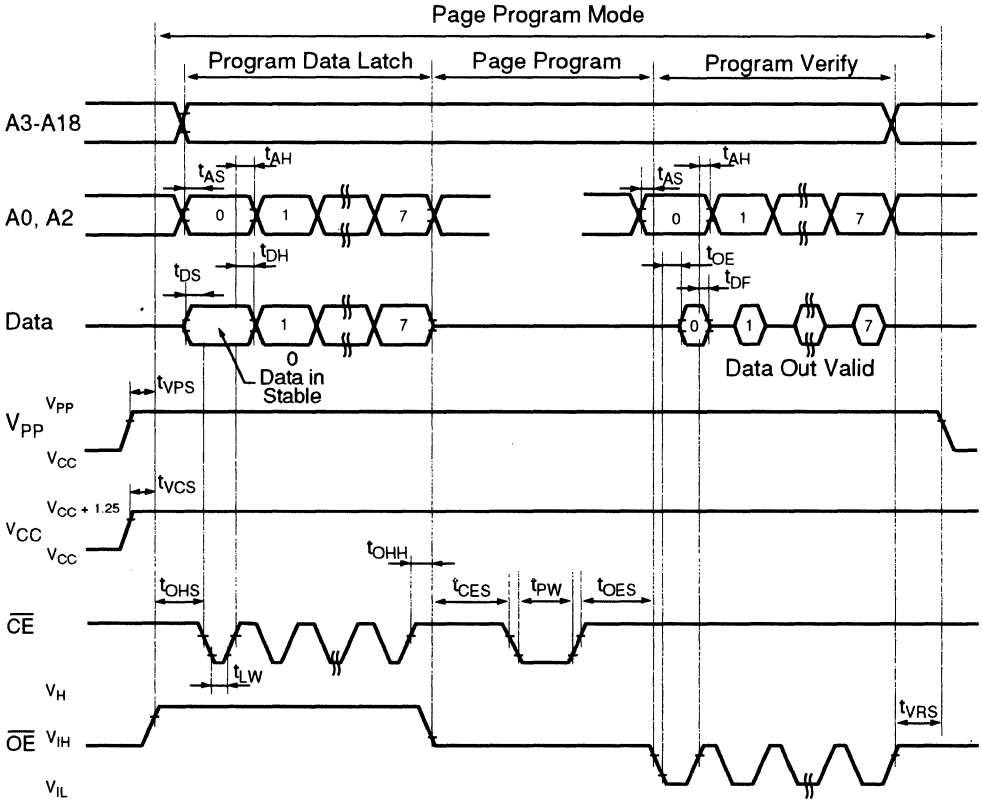
The Hitachi HN27C4001 can be programmed with the high performance Page Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.

Note: 1. To set the device into Page Programming, apply 12.5 V to V_{PP} then followed by applying 12 V to $\overline{OE}$. The device operates in Page Program Mode until reset.
2. To reset the Page Program Mode, set $V_{PP} = V_{CC}$ or less.



(FC.PP.HN27C4001)

■ PAGE PROGRAMMING TIMING WAVEFORM

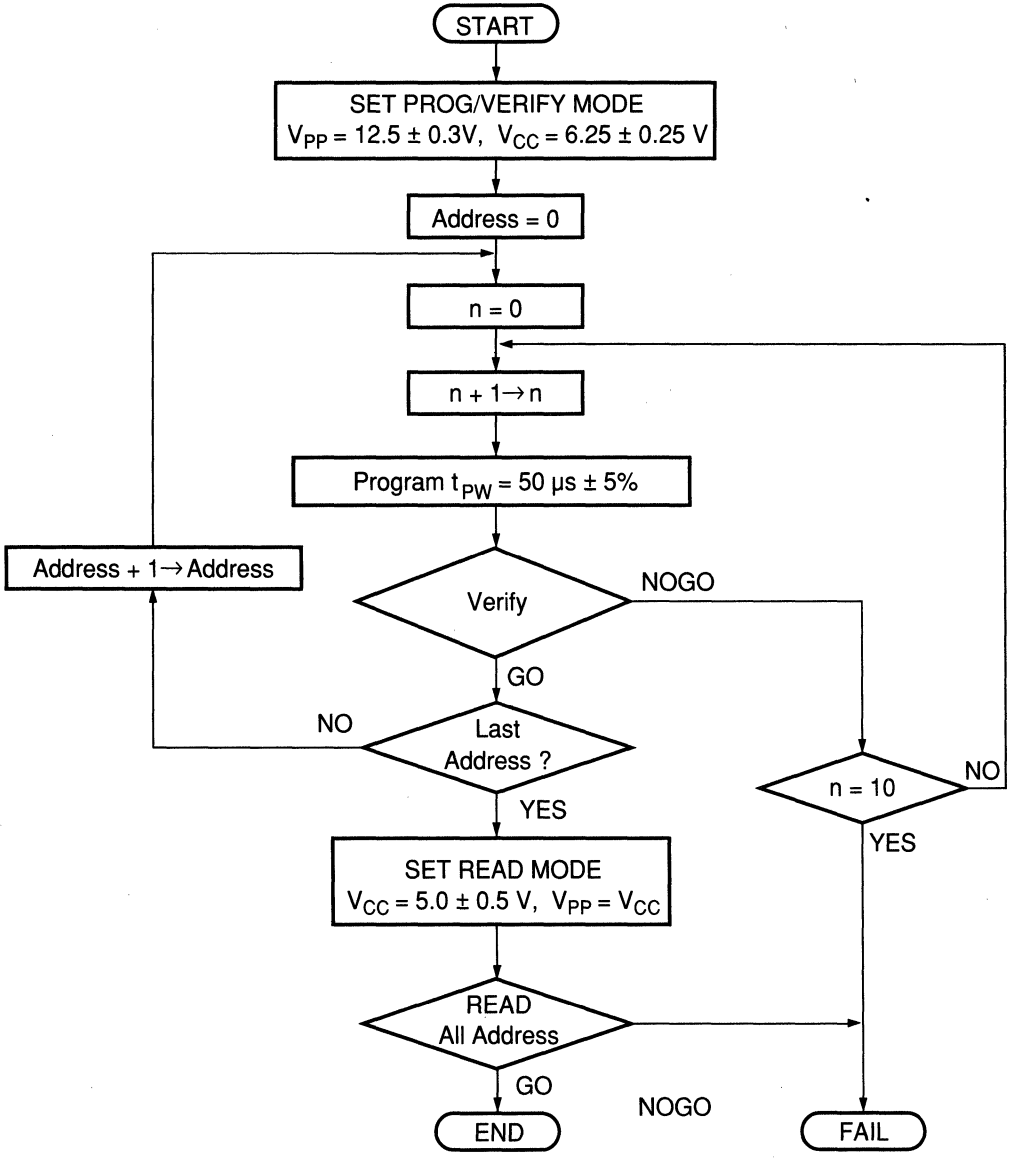


(TD.PP.HN27C4001)

4

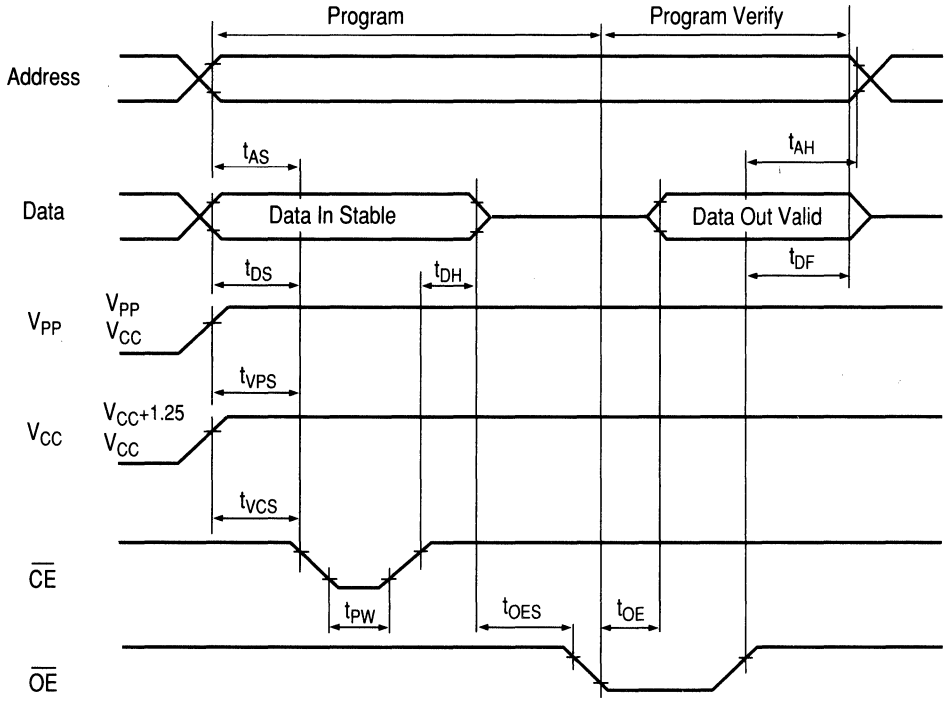
■ BYTE PROGRAMMING FLOWCHART

The Hitachi HN27C4096H can be programmed with the high performance Byte Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.



(FC.P.HN27C4001)

■ BYTE PROGRAMMING TIMING WAVEFORM



(TD.P.HN27C4001)

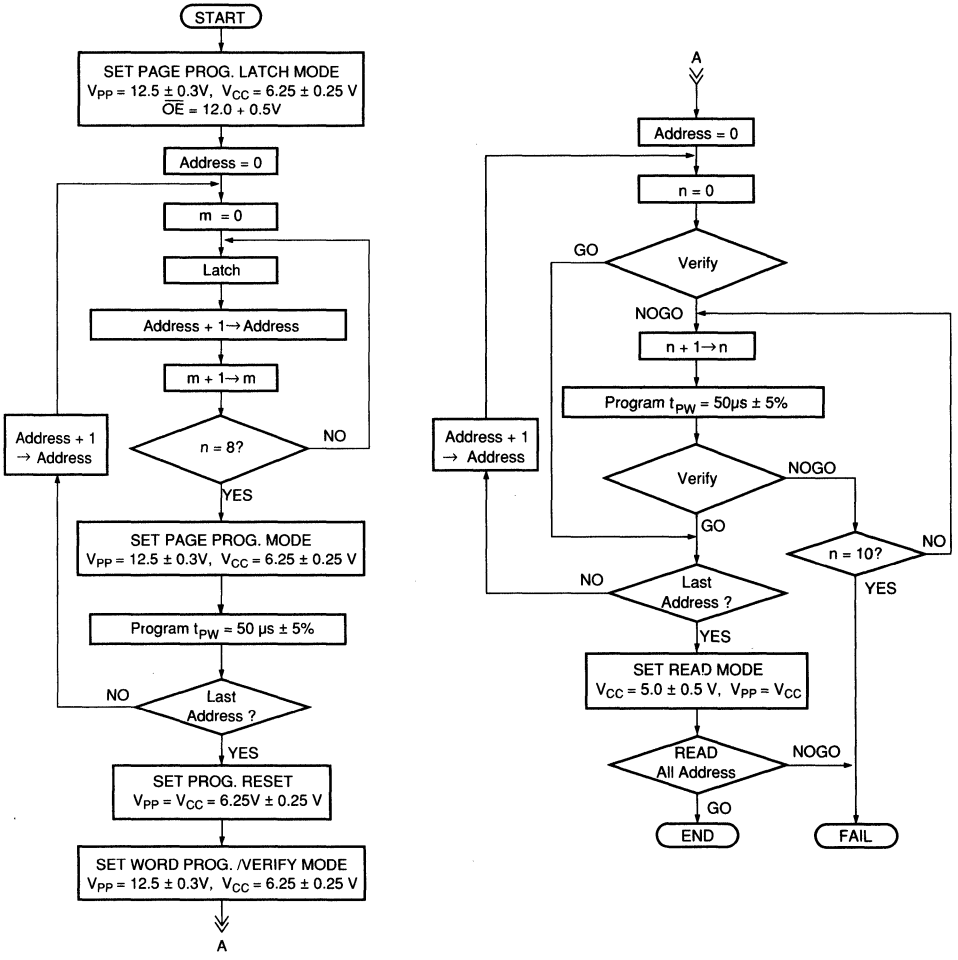
4

■ OPTIONAL PAGE PROGRAMMING FLOWCHART

The Hitachi HN27C4001 can be programmed with the high performance Optional Page Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.

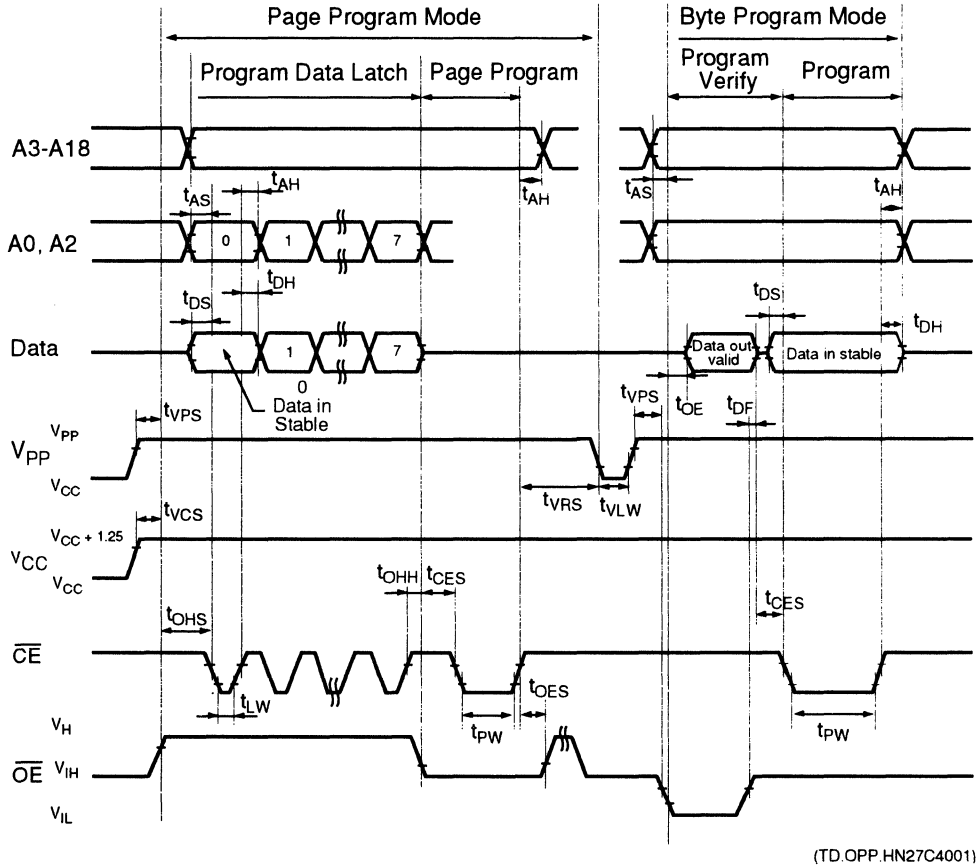
This programming algorithm is a combination of Page Programming and Byte Verify. It can be used to avoid the increased programming verify time when a programmer with a slower machine cycle is used and shorten the total programming time.

Please refer to the timing specifications for page programming and byte programming.



(FC.OPP.HN27C4001)

■ OPTIONAL PAGE PROGRAMMING TIMING WAVEFORM



(TD.OPP.HN27C4001)

4

■ ERASING THE HN27C4001

The Hitachi HN27C4001 Ceramic DIP package allows the device to be erased by exposure to ultraviolet light of 2537Å. All of the data is changed to "1" after this erasure procedure. The minimum integrated dose (UV intensity x exposure time) for erasure is 15 W-sec/cm^2.

■ DEVICE IDENTIFIER MODE DESCRIPTION

The Device Identifier Mode allows binary codes to be read from the outputs that identify the manufacturer and the type of device. Using this mode with programming equipment, the device will automatically match its own erase and programming algorithm.

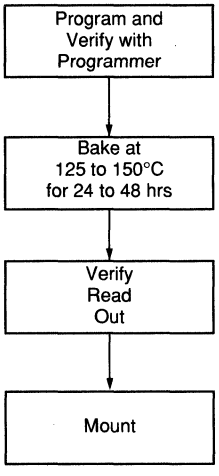
■ HN27C4001 SERIES IDENTIFIER CODE

Identifier	A_0	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	0	0	1	0	0	0	0	0	20

Notes:
1. V_{CC} = 5.0 V ± 10%
2. A_9 = 12.0 V ± 0.5V
3. A_1-A_8, A_{10}-A_{18}, $\overline{CE}$, $\overline{OE}$ = V_{IL}
4. X = Don't Care

■ HN27C4001TT/RR RECOMMENDED SCREENING CONDITIONS

Before mounting the HN27C4001TT/RR packages, please make the following screening (baking without bias) shown below:



(RSC.EPROM)

EEPROM

SECTION 5
EEPROM

HITACHI

Hitachi America, Ltd. • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

HN58C65 Series

64K (8K x 8-bit) EEPROM

■ DESCRIPTION

The Hitachi HN58C65 is a 64-Kilobit CMOS Electrically Erasable Programmable Read Only Memory (EEPROM) organized as 8,192 x 8-bits. The HN58C65 is capable of in-system electrical Byte and Page reprogrammability.

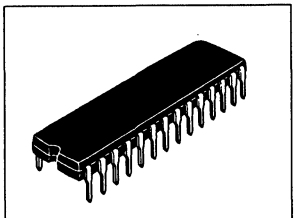
The HN58C65 achieves high speed access, low power consumption, and a high level of reliability by employing advanced MNOS memory technology and CMOS process and circuitry technology.

The HN58C65 has a 32-Byte Page Programming function to make its erase and write operations faster. The HN58C65 features $\overline{\text{Data}}$ Polling and a Ready/$\overline{\text{Busy}}$ signal to indicate completion of erase and programming operations.

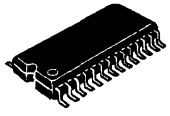
The HN58C65 provides several levels of data protection. Hardware data protection is provided noise protection on the $\overline{\text{WE}}$ signal and write inhibit on power on and off.

The HN58C65 is designed for high reliability in the most demanding applications. Data retention is specified for 10 years and erase/write endurance is guaranteed to a minimum of 100,000 cycles in the Page Mode.

The HN58C65 is offered in JEDEC-Standard Byte-Wide EEPROM pinouts in 28-pin Plastic DIP and 28-lead Plastic SOP packages.



(DP-28)



(FP-28DA)

■ FEATURES

- Single Power Supply:
  V_{CC} = 5V ± 10%
- Fast Access Time:
  250 ns (max)
- Low Power Dissipation:
  Active Current: 20 mW/MHz (typ)
  Standby Current: 2 mW (max)
- Automatic Programming:
  Automatic Page Write: 10 ms (max)
  32 Byte Page Size
  Automatic Byte Write: 10 ms (max)
- $\overline{\text{Data}}$ Polling and Ready/$\overline{\text{Busy}}$ Signals
- Data Protection Circuitry on Power On/Off
- Data Retention: 10 years
- Erase/Write Endurance:
  100,000 cycles in Page Mode
- Pinouts:
  JEDEC Standard Byte-Wide EEPROM
- Packages:
  28-pin Plastic DIP
  28-lead Plastic SOP

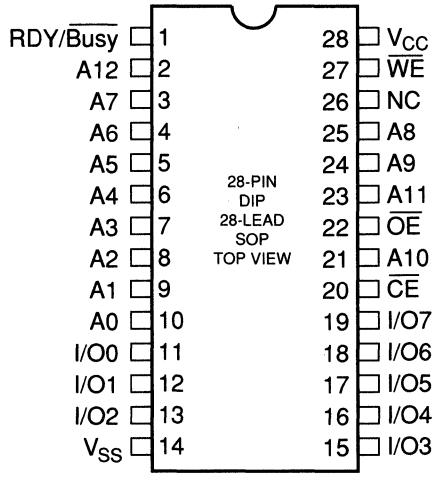
5

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN58C65P-25	250 ns	28-pin Plastic DIP (DP-28)
HN58C65FP-25	250 ns	32-lead Plastic SOP (FP-28DA)

■ PIN ARRANGEMENT

HN58C65P Series
HN58C65FP Series

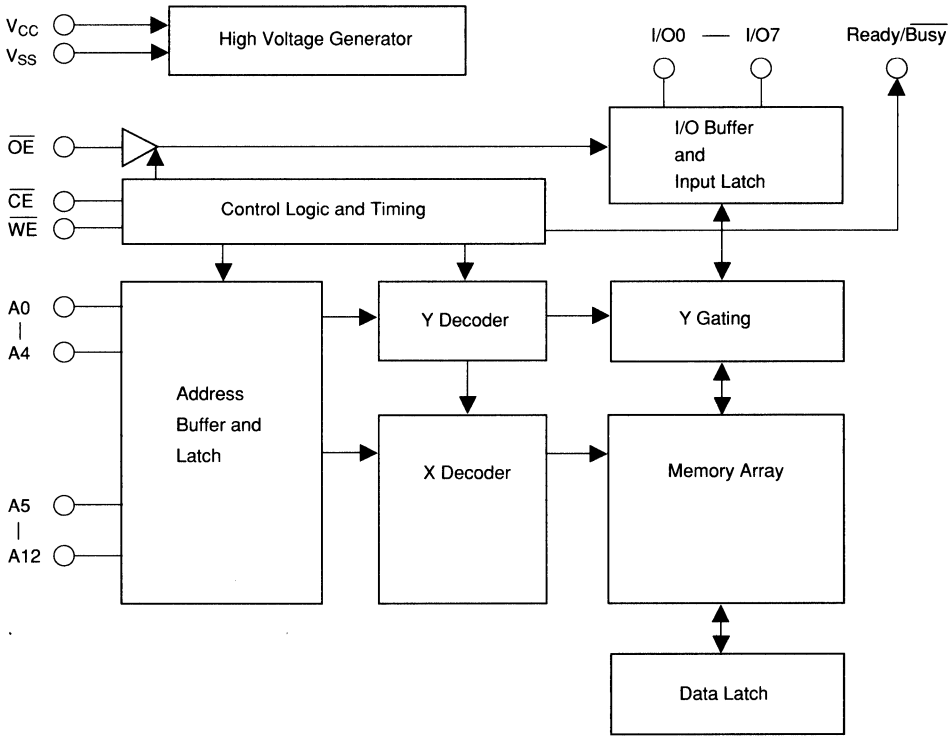


(PinD28.HN58C65)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{12}	Address
I/O_0 - I/O_7	Input/Output
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground
Rdy/$\overline{Busy}$	Ready/Busy
NC	No Connection

■ BLOCK DIAGRAM



(BD.HN58C65)

5

■ MODE SELECTION

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	RDY/$\overline{Busy}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	High-Z	D_{OUT}
Standby	V_{IH}	X	X	High-Z	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	High-Z→V_{OL}	D_{IN}
Deselect	V_{IL}	V_{IH}	V_{IH}	High-Z	High-Z
Write Inhibit	X	X	V_{IH}	-	-
	X	V_{IL}	X	-	-
$\overline{Data}$ Polling	V_{IL}	V_{IL}	V_{IH}	V_{OL}	Data Out (I/O_7)

Note: 1. X = Don't Care

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Input Voltage [1]	V_{IN}	-0.5[2] to +7.0	V
Operating Temperature Range [3]	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C

Notes: 1. Relative to V_{SS}.
2. V_{IN} min = -3.0V for pulse width ≤ 50 ns.
3. Including electrical characterisitics and data retention.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	-	-	6	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	-	-	12	pF	V_{OUT} = 0V

■ DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{CC} = 5.5 V, V_{IN} = 5.5 V
Output Leakage Current	I_{LO}	-	-	2	µA	V_{CC} = 5.5 V, V_{OUT} = 5.5 V/0.4 V
Standby V_{CC} Current	I_{CC1}	-	-	200	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	-	-	1	mA	$\overline{CE}$ = V_{IH}
Operating V_{CC} Current	I_{CC3}	-	-	8	mA	I_{OUT} = 0 mA, Duty = 100%, Cycle = 1 µs
		-	-	25	mA	I_{OUT} = 0 mA, Duty = 100%, Cycle = 250 ns
Input Voltage	V_{IL}	-0.3 [1]	-	0.8	V	
	V_{IH}	2.2	-	V_{CC} + 1	V	
	V_H	V_{CC} - 0.5	-	V_{CC} + 1	V	
Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA

Notes: 1. V_{IL} min = -1.0 V for pulse width ≤ 50 ns.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(T_a = 0 to 70°C, V_{CC} = 5V ± 10%)

Test Conditions

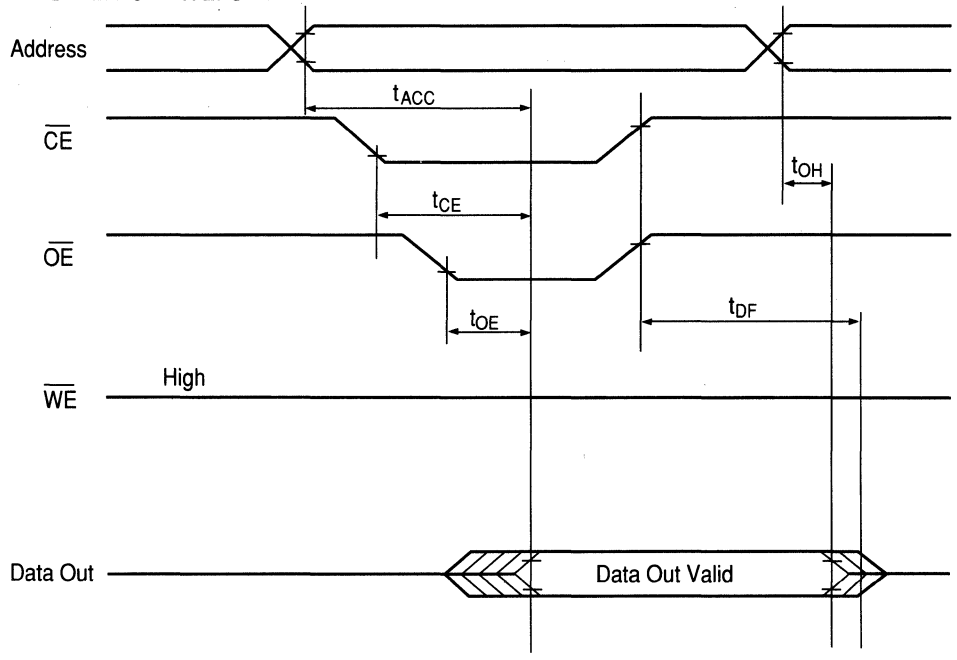
- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall times: ≤ 20 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V, 2.0 V

Item	Symbol	HN58C66-25 Min.	HN58C66-25 Max.	Unit	Test Condition
Address Access Time	t_{ACC}	-	250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Chip Enable Access Time	t_{CE}	-	250	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Enable Access Time	t_{OE}	10	100	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Hold to Address Change	t_{OH}	0	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Disable to High-Z[1]	t_{DF}	0	90	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

5

■ READ TIMING WAVEFORM



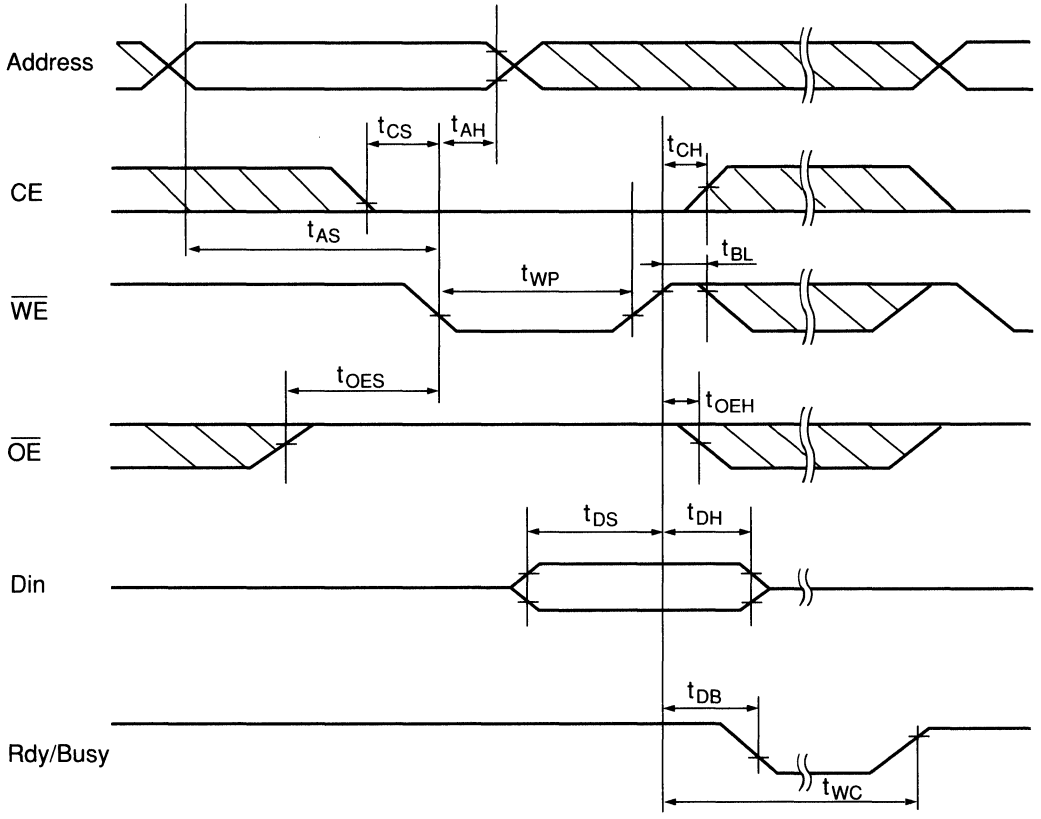
(TD.R.HN58C65)

■ AC ELECTRICAL CHARACTERISTICS FOR BYTE ERASE AND BYTE WRITE OPERATIONS

Item	Symbol	Min.[1]	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	0	-	-	ns	
Chip Enable to Write Setup Time	t_{CS}[2]	0	-	-	ns	
Write Enable to Write Setup Time	t_{WS}[3]	0	-	-	ns	
Write Pulse Width	t_{WP}[2]	200	-	-	ns	
	t_{CW}[3]	200	-	-	ns	
Address Hold Time	t_{AH}	150	-	-	ns	
Data Setup Time	t_{DS}	100	-	-	ns	
Data Hold Time	t_{DH}	20	-	-	ns	
Chip Enable Hold Time	t_{CH}[2]	0	-	-	ns	
Write Enable Hold Time	t_{WH}[3]	0	-	-	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Output Enable Hold Time	t_{OEH}	0	-	-	ns	
Write Cycle Time	t_{WC}	-	-	10	ms	
Byte Load Window	t_{BL}	100	-	-	µs	
Time to Device Busy	t_{DB}	120	-	-	µs	

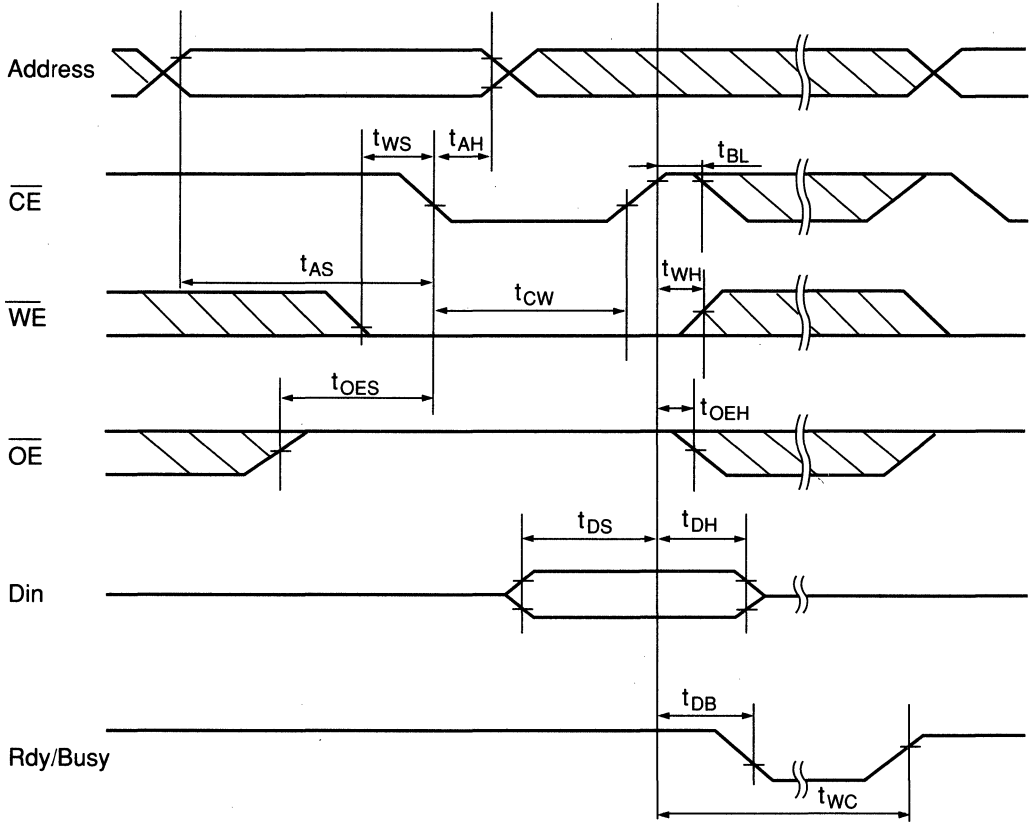
Note: 1. Use this device in a longer cycle than this value.
2. Write Enable controlled operation.
3. Chip Enable controlled operation.

■ **BYTE ERASE AND BYTE WRITE TIMING WAVEFORM ($\overline{WE}$ Controlled)**



(TD.BE1.HN58C65)

■ **BYTE ERASE AND BYTE WRITE TIMING WAVEFORM ($\overline{CE}$ Controlled)**



(TD.BE2.HN58C65)

Hitachi America, Ltd. • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

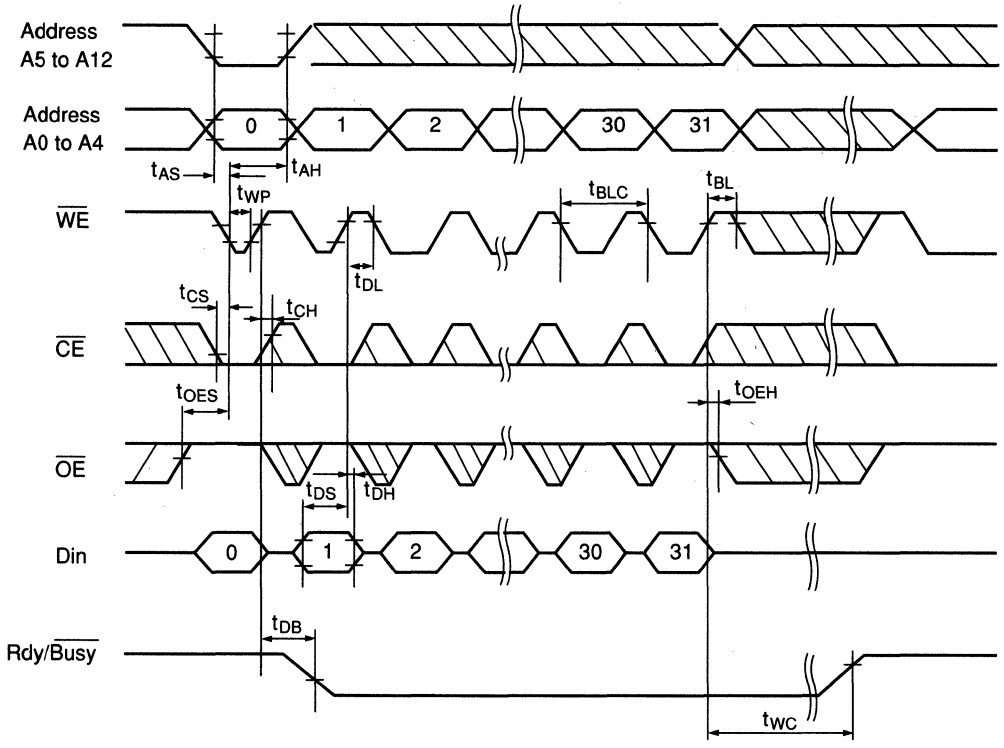
■ AC ELECTRICAL CHARACTERISTICS FOR PAGE ERASE AND PAGE WRITE OPERATIONS

Item	Symbol	Min.[1]	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	0	-	-	ns	
Chip Enable to Write Setup Time	t_{CS}[2]	0	-	-	ns	
Write Enable to Write Setup Time	t_{WS}[3]	0	-	-	ns	
Write Pulse Width	t_{WP}[2]	200	-	-	ns	
	t_{CW}[3]	200	-	-	ns	
Address Hold Time	t_{AH}	150	-	-	ns	
Data Setup Time	t_{DS}	100	-	-	ns	
Data Hold Time	t_{DH}	20	-	-	ns	
Chip Enable Hold Time	t_{CH}[2]	0	-	-	ns	
Write Enable Hold Time	t_{WH}[3]	0	-	-	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Output Enable Hold Time	t_{OEH}	0	-	-	ns	
Data Latch Time	t_{DL}	100	-	-	ns	
Write Cycle Time	t_{WC}	-	-	10	ms	
Byte Load Window	t_{BL}	100	-	-	µs	
Byte Load Cycle	t_{BLC}	0.3	-	30	µs	
Time to Device Busy	t_{DB}	120	-	-	ns	

Notes: 1. Use this device in longer cycle than this value.
2. Write Enable controlled operation.
3. Chip Enable controlled operation.

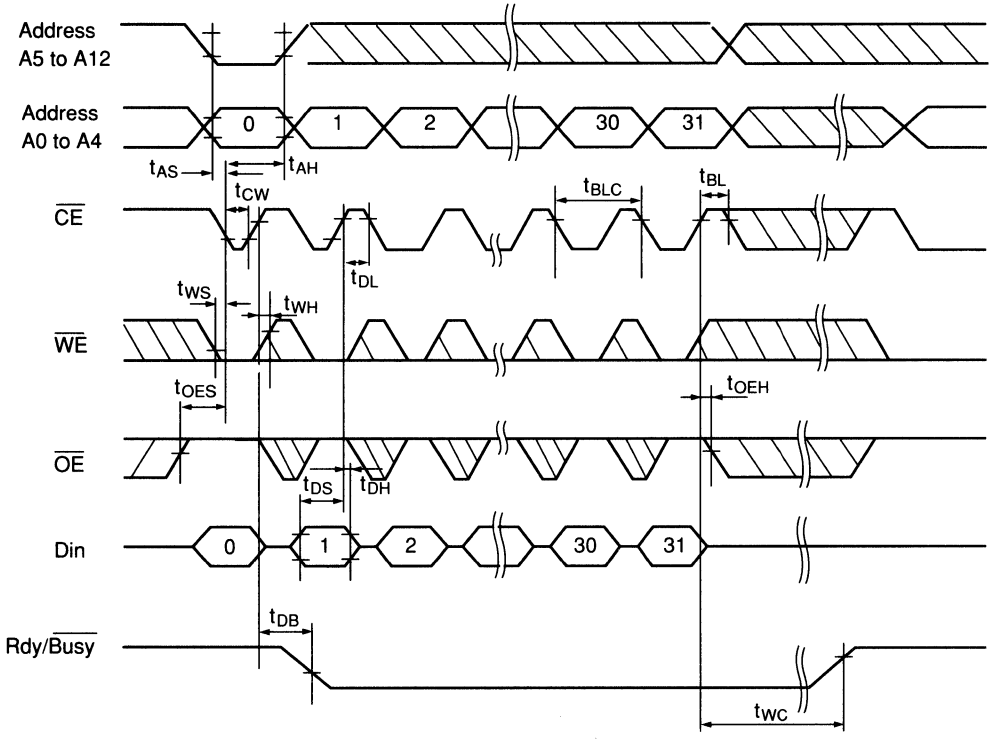
5

■ PAGE ERASE AND PAGE WRITE TIMING WAVEFORM ($\overline{WE}$ Controlled)



(TD.PE1.HN58C65)

■ PAGE ERASE AND PAGE WRITE TIMING WAVEFORM ($\overline{CE}$ Controlled)

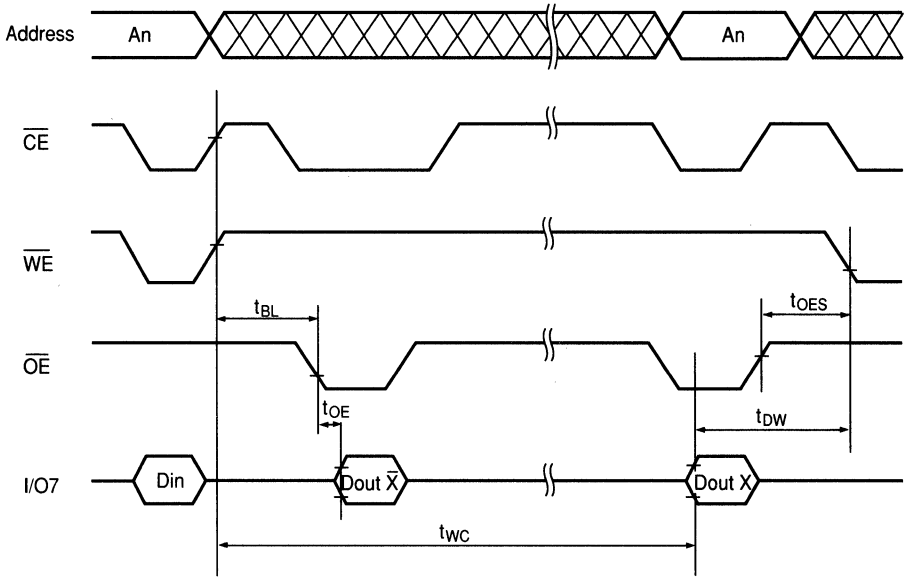


(TD.PE2.HN58C65)

■ AC ELECTRICAL CHARACTERISTICS FOR $\overline{\text{DATA}}$ POLLING OPERATION

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Output Enable to Output Delay	t_{OE}	10	-	90	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Write Start Time	t_{DW}	150	-	-	ns	
Write Cycle Time	t_{WC}	-	-	10	ms	

■ $\overline{\text{DATA}}$ POLLING TIMING WAVEFORM



(TD.DP.HN58C1001)

■ FUNCTIONAL DESCRIPTION

Automatic Page Write

The Page Write feature allows 1 to 32 Bytes of data to be written into the EEPROM in a single write cycle andthe undefined data within 32 Bytes to be written corresponding to the undefined address (A_0 to A_4). Each additional Byte load cycle must be started within 30 µs from the preceding falling edge of $\overline{WE}$ or $\overline{CE}$. If $\overline{CE}$ and $\overline{WE}$ are kept high for 100 µs after data input, the EEPROM automatically enters erase and write mode and only the input data is written into the EEPROM. Data can be written and accessed 10^5 times in 32 Byte units.

$\overline{\text{Data}}$ Polling

$\overline{\text{Data}}$ Polling allows the status of the EEPROM to be determined. If the EEPROM is set to Read mode during a Write cycle, an inversion of the last Byte of data to be loaded outputs from I/O_7 to indicate that the EEPROM is performing a Write operation.

Ready/$\overline{\text{Busy}}$ Signal

The Ready/$\overline{\text{Busy}}$ signal also allows the status of the EEPROM to be determined. The Ready/$\overline{\text{Busy}}$ signal is high impedence except in the write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, the Ready/$\overline{\text{Busy}}$ signal changes to high impedence.

$\overline{WE}$ and $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

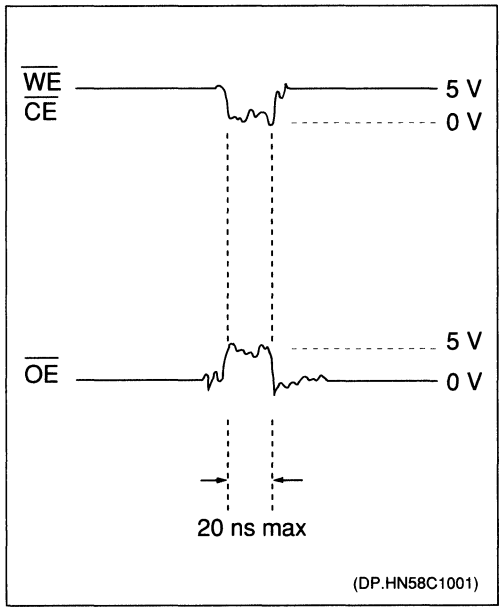
Write/Erase Endurance and Data Retention

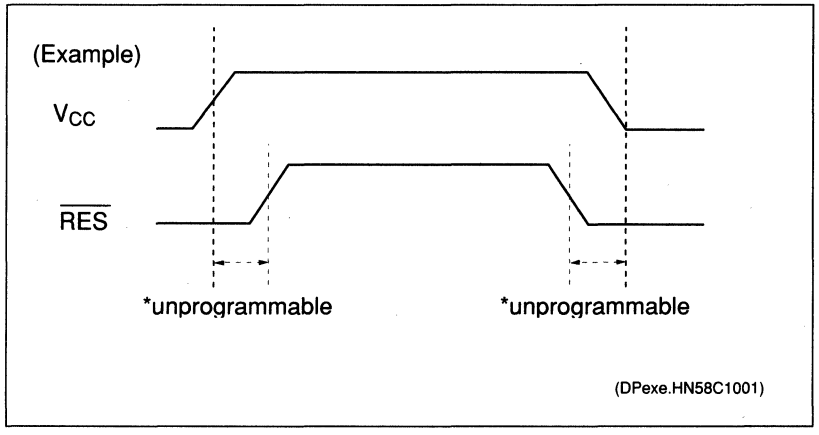
The endurance with page programming is 10^5 cycles (1% cumulative failure rate) and the data retention time is more than 10 years when a device is programmed less than 10^4 cycles.

Data Protection

To protect the data during operation and power on/off, the HN58C65 has:

1. Data protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation.
   During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. To prevent this phenomenon, the HN58C65 has a noise cancellation function that cuts noise if its width is 20 ns or less in programming mode. Be careful not to allow noise of a width of more than 20 ns on the control pins.





■ FUNCTIONAL DESCRIPTION (continued)

Data Protection (continued)

2. Data protection at V_{CC} on/off
   When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may turn the EEPROM to programming mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPU is in an unstable state.
   In addition, when RES is kept high at V_{CC} on/off timing, the input level of control pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) must be held as $\overline{CE}$=V_{CC} or $\overline{OE}$=Low or $\overline{WE}$=V_{CC} level.

HN58C66 Series

64K (8K x 8-bit) EEPROM

■ DESCRIPTION

The Hitachi HN58C66 is a 64-Kilobit CMOS Electrically Erasable Programmable Read Only Memory (EEPROM) organized as 8,192 x 8-bits. The HN58C66 is capable of in-system electrical Byte and Page reprogrammability.

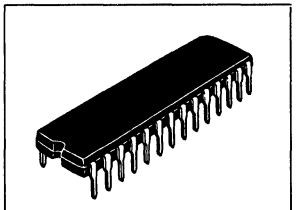
The HN58C66 achieves high speed access, low power consumption, and a high level of reliability by employing advanced MNOS memory technology and CMOS process and circuitry technology.

The HN58C66 has a 32-Byte Page Programming function to make its erase and write operations faster. The HN58C66 features $\overline{\text{Data}}$ Polling and a Ready/$\overline{\text{Busy}}$ signal to indicate completion of erase and programming operations.

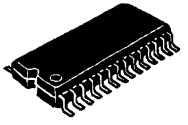
The HN58C66 provides several levels of data protection. Hardware data protection is provided with the $\overline{\text{RES}}$ pin, in addition to noise protection on the $\overline{\text{WE}}$ signal and write inhibit on power on and off.

The HN58C66 is designed for high reliability in the most demanding applications. Data retention is specified for 10 years and erase/write endurance is guaranteed to a minimum of 100,000 cycles in the Page Mode.

The HN58C66 is offered in JEDEC-Standard Byte-Wide EEPROM pinouts in 28-pin Plastic DIP and 28-lead Plastic SOP packages. The HN58C66 is also offered in a 32-lead Plastic TSOP package.



(DP-28)



(FP-28DA)

(TFP-32DA)

■ FEATURES

- Single Power Supply:
  V_{CC} = 5V ± 10%
- Fast Access Time:
  250 ns (max)
- Low Power Dissipation:
  Active Current: 20 mW/MHz (typ)
  Standby Current: 2 mW (max)
- Automatic Programming:
  Automatic Page Write: 10 ms (max)
  32 Byte Page Size
  Automatic Byte Write: 10 ms (max)
- $\overline{\text{Data}}$ Polling and Ready/$\overline{\text{Busy}}$ Signals
- Hardware Data Protection with $\overline{\text{RES}}$ pin
- Data Protection Circuitry on Power On/Off
- Data Retention: 10 years
- Erase/Write Endurance:
  100,000 cycles in Page Mode
- Pinouts:
  JEDEC Standard Byte-Wide EEPROM
- Packages:
  28-pin Plastic DIP
  28-lead Plastic SOP
  32-lead Plastic TSOP (Type I)

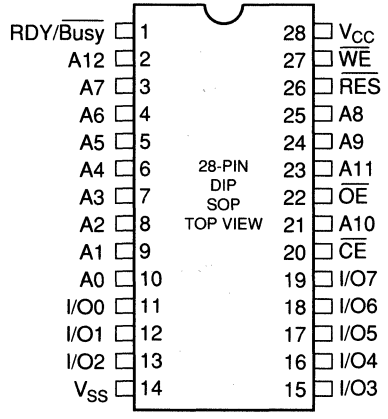
5

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN58C66P-25	250 ns	28-pin Plastic DIP (DP-28)
HN58C66FP-25	250 ns	28-lead Plastic SOP (FP-28DA)
HN58C66T-25	250 ns	32-lead Plastic TSOP (TFP-32DA)

■ PIN ARRANGEMENT

HN58C66P Series
HN58C66FP Series

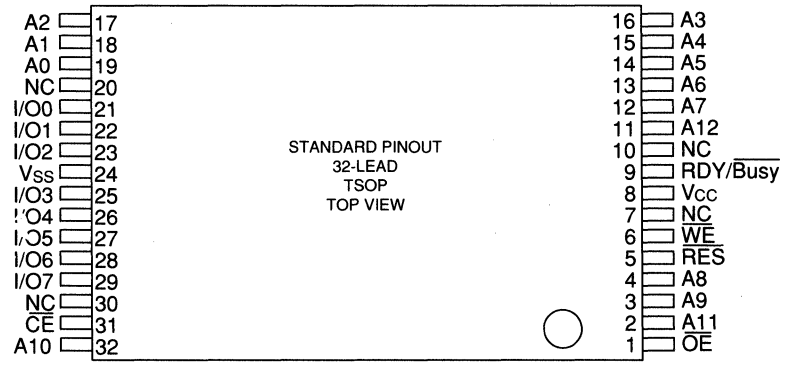


(PinD28.HN58C66)

■ PIN DESCRIPTION

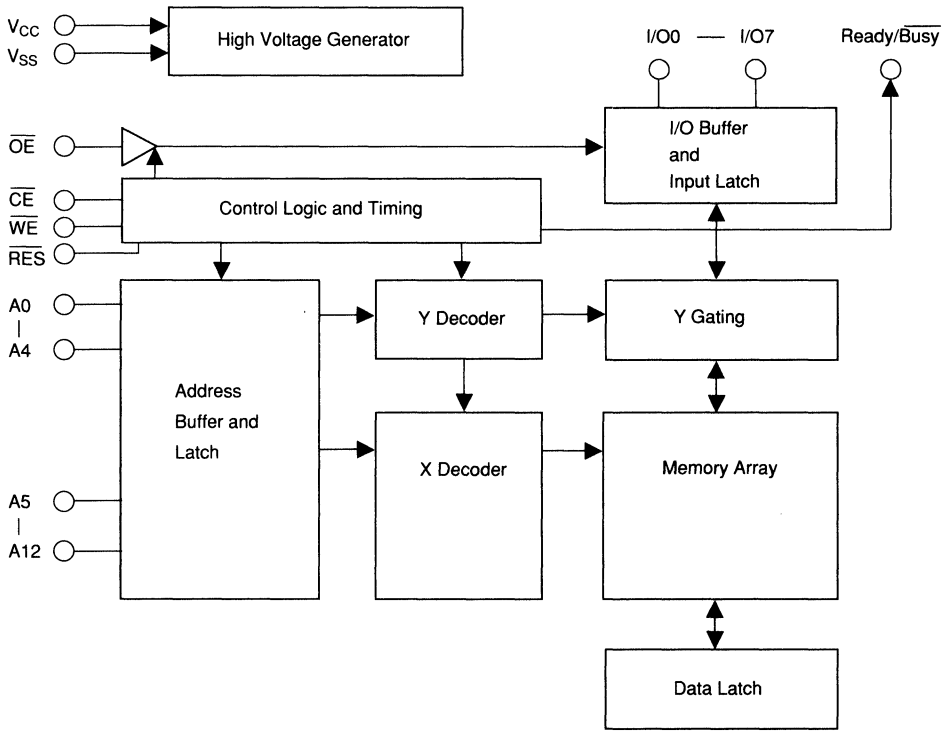
Pin Name	Function
A_0 - A_{12}	Address
I/O_0 - I/O_7	Input/Output
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground
Rdy/$\overline{Busy}$	Ready/Busy
$\overline{RES}$	Reset

HN58C66T Series



(PinT132.HN58C66T)

■ BLOCK DIAGRAM



(BD.HN58C66)

5

■ MODE SELECTION

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RES}$	RDY/$\overline{Busy}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_H	High-Z	D_{OUT}
Standby	V_{IH}	X	X	X	High-Z	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	V_H	High-Z→V_{OL}	D_{IN}
Deselect	V_{IL}	V_{IH}	V_{IH}	V_H	High-Z	High-Z
Write Inhibit	X	X	V_{IH}	X	-	-
	X	V_{IL}	X	X	-	
$\overline{Data}$ Polling	V_{IL}	V_{IL}	V_{IH}	V_H	V_{OL}	Data Out (I/O_7)
Program	X	X	X	V_{IL}	High-Z	High-Z

Note: 1. X = Don't Care

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Input Voltage [1]	V_{IN}	-0.5[2] to +7.0	V
Operating Temperature Range [3]	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C

Notes: 1. Relative to V_{SS}.
2. V_{IN} min = -3.0V for pulse width ≤ 50 ns.
3. Including electrical characterisitics and data retention.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	-	-	6	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	-	-	12	pF	V_{OUT} = 0V

■ DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI} [1]	-	-	2	µA	V_{CC} = 5.5 V, V_{IN} = 5.5 V
Output Leakage Current	I_{LO}	-	-	2	µA	V_{CC} = 5.5 V, V_{OUT} = 5.5 V/0.4 V
Standby V_{CC} Current	I_{CC1}	-	-	200	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	-	-	1	mA	$\overline{CE}$ = V_{IH}
Operating V_{CC} Current	I_{CC3}	-	-	8	mA	I_{OUT} = 0 mA, Duty = 100%, Cycle = 1 µs
		-	-	25	mA	I_{OUT} = 0 mA, Duty = 100%, Cycle = 250 ns
Input Voltage	V_{IL}	-0.3 [2]	-	0.8	V	
	V_{IH}	2.2	-	V_{CC} + 1	V	
	V_H	V_{CC} - 0.5	-	V_{CC} + 1	V	
Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA

Notes: 1. I_{LI} on $\overline{RES}$ = 100 µA max.
2. V_{IL} min = -3.0 V for pulse width ≤ 50 ns.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(T_a = 0 to 70°C, V_{CC} = 5V ± 10%)

Test Conditions

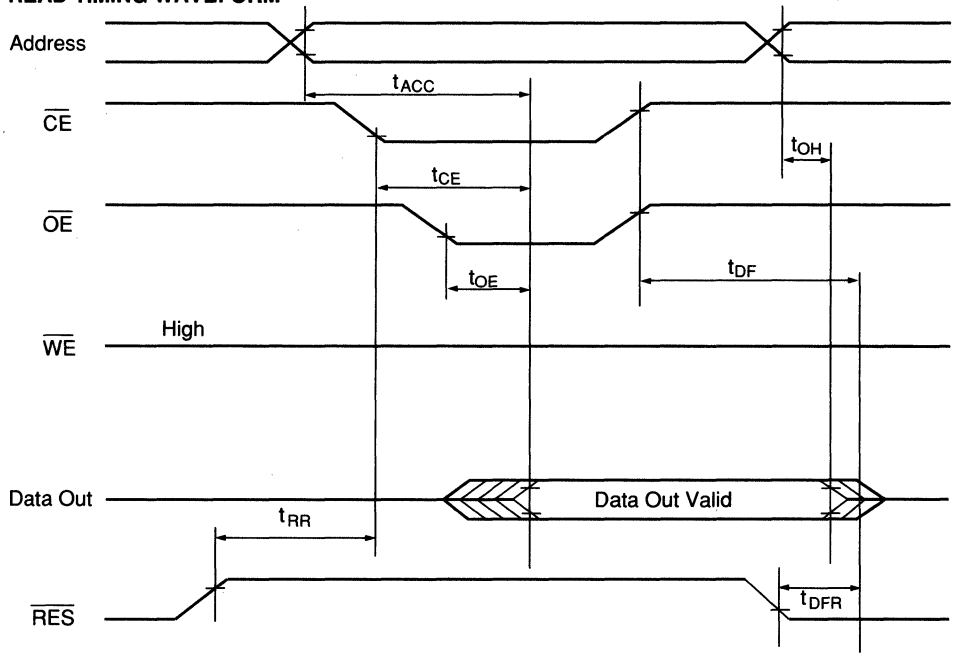
- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall times: ≤ 20 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V, 2.0 V

Item	Symbol	HN58C66-25 Min.	HN58C66-25 Max.	Unit	Test Condition
Address Access Time	t_{ACC}	-	250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Chip Enable Access Time	t_{CE}	-	250	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Enable Access Time	t_{OE}	10	100	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Hold to Address Change	t_{OH}	0	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Disable to High-Z[1]	t_{DF}	0	90	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
	t_{DFR}	0	350	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ to Output Delay	t_{RR}	0	450	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

5

■ READ TIMING WAVEFORM



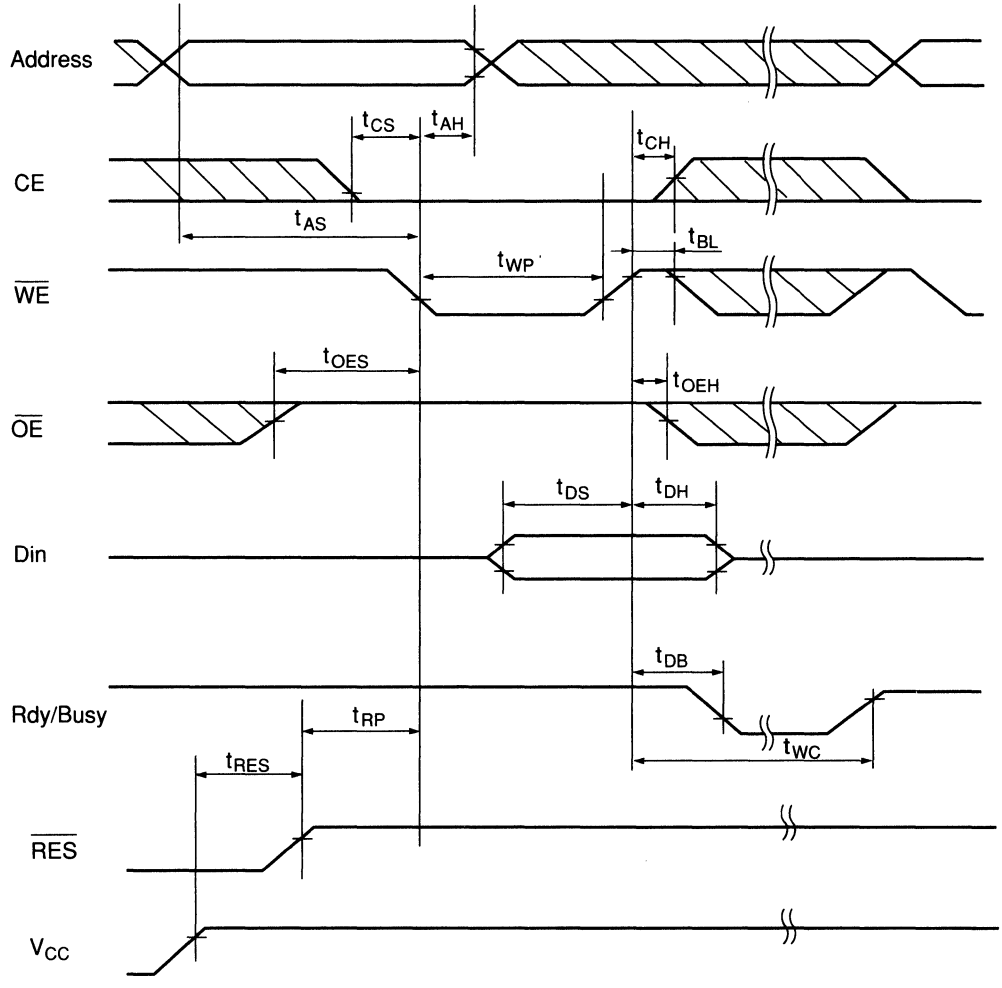
(TD.R.HN58C1001)

■ AC ELECTRICAL CHARACTERISTICS FOR BYTE ERASE AND BYTE WRITE OPERATIONS

Item	Symbol	Min.[1]	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	0	-	-	ns	
Chip Enable to Write Setup Time	t_{CS}[2]	0	-	-	ns	
Write Enable to Write Setup Time	t_{WS}[3]	0	-	-	ns	
Write Pulse Width	t_{WP}[2]	200	-	-	ns	
	t_{CW}[3]	200	-	-	ns	
Address Hold Time	t_{AH}	150	-	-	ns	
Data Setup Time	t_{DS}	100	-	-	ns	
Data Hold Time	t_{DH}	0	-	-	ns	
Chip Enable Hold Time	t_{CH}[2]	0	-	-	ns	
Write Enable Hold Time	t_{WH}[3]	0	-	-	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Output Enable Hold Time	t_{OEH}	0	-	-	ns	
Write Cycle Time	t_{WC}	10	-	-	ms	
Byte Load Window	t_{BL}	100	-	-	µs	
Time to Device Busy	t_{DB}	120	-	-	ns	
$\overline{RES}$ to Write Setup Time	t_{RP}	100	-	-	µs	
V_{CC} to $\overline{RES}$ Setup Time	t_{RES}	1	-	-	µs	

Note: See Characteristics for Page Erase and Page Write Operations

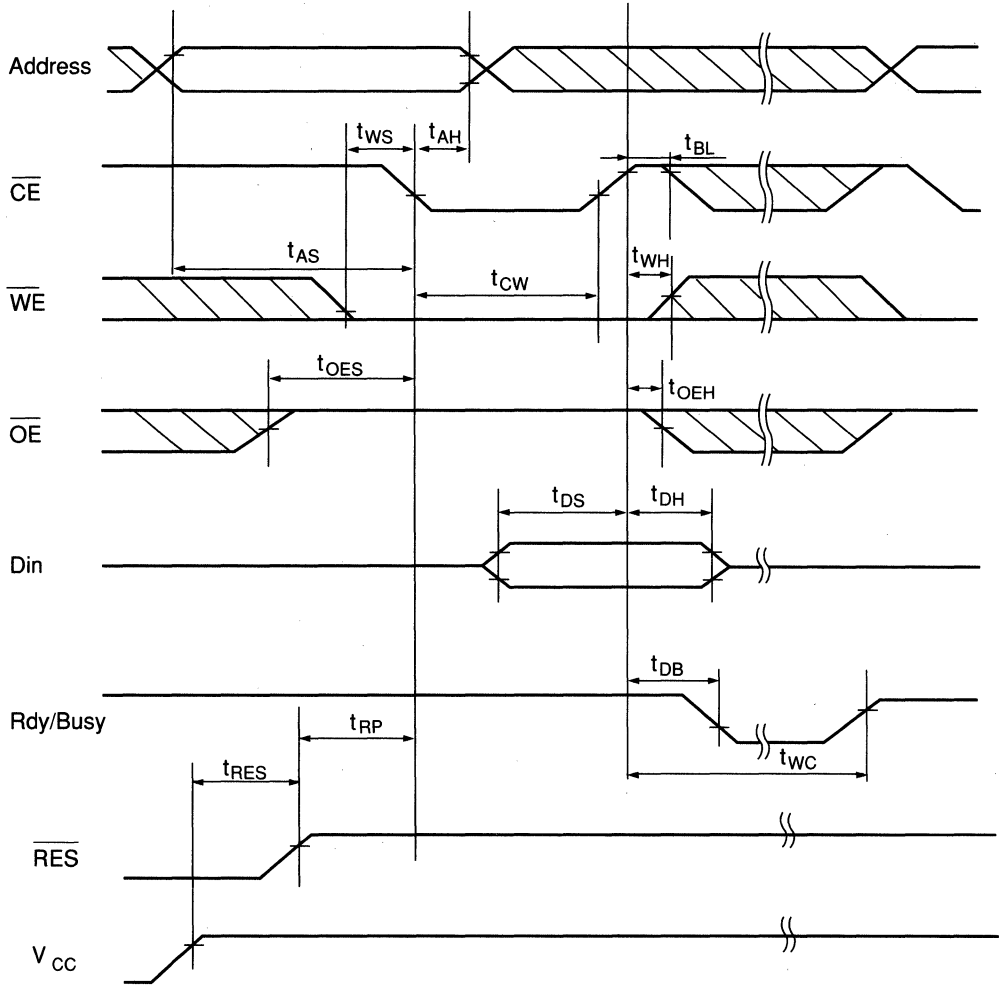
■ BYTE ERASE AND BYTE WRITE TIMING WAVEFORM ($\overline{WE}$ Controlled)



(TD.BE1.HN58C66)

5

■ BYTE ERASE AND BYTE WRITE TIMING WAVEFORM ($\overline{CE}$ Controlled)



(TD.BE2.HN58C66)

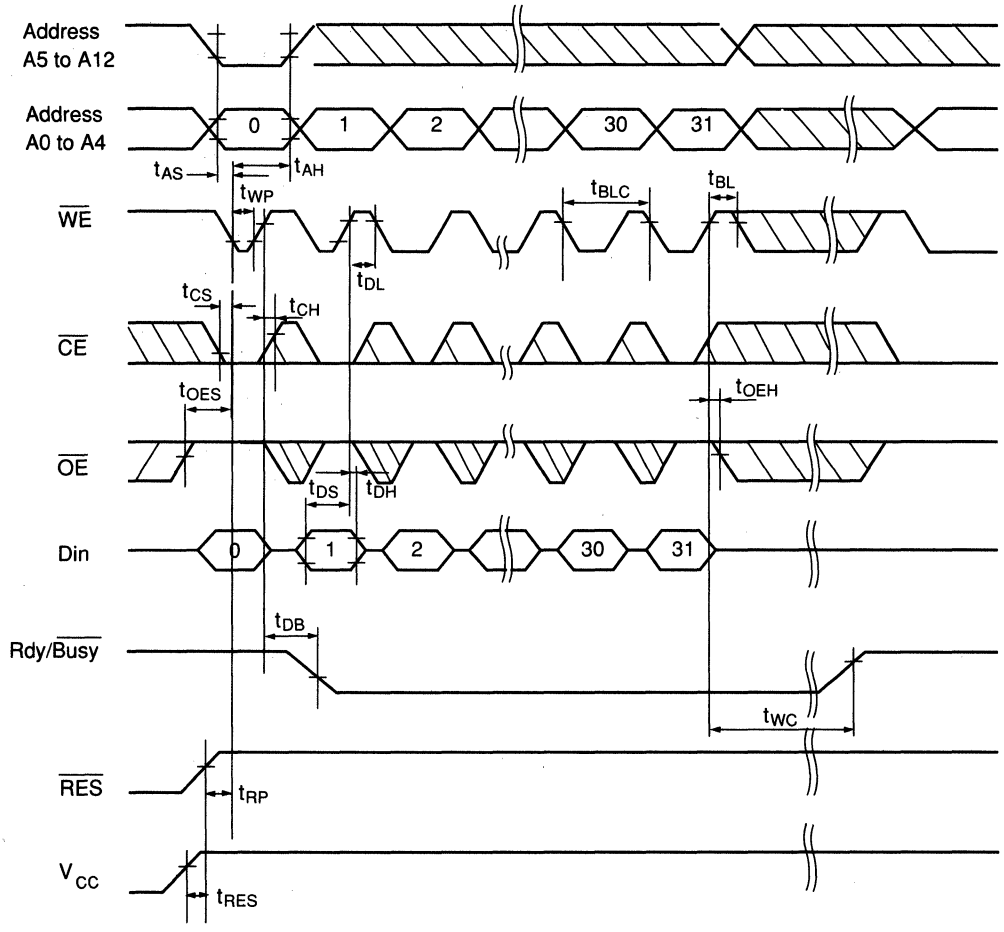
■ AC ELECTRICAL CHARACTERISTICS FOR PAGE ERASE AND PAGE WRITE OPERATIONS

Item	Symbol	Min.[1]	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	0	-	-	ns	
Chip Enable to Write Setup Time	t_{CS}[2]	0	-	-	ns	
Write Enable to Write Setup Time	t_{WS}[3]	0	-	-	ns	
Write Pulse Width	t_{WP}[2]	200	-	-	ns	
	t_{CW}[3]	200	-	-	ns	
Address Hold Time	t_{AH}	150	-	-	ns	
Data Setup Time	t_{DS}	100	-	-	ns	
Data Hold Time	t_{DH}	0	-	-	ns	
Chip Enable Hold Time	t_{CH}[2]	0	-	-	ns	
Write Enable Hold Time	t_{WH}[3]	0	-	-	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Output Enable Hold Time	t_{OEH}	0	-	-	ns	
Data Latch Time	t_{DL}	100	-	-	ns	
Write Cycle Time	t_{WC}	10	-	-	ms	
Byte Load Window	t_{BL}	100	-	-	µs	
Byte Load Cycle	t_{BLC}	0.3	-	30	µs	
Time to Device Busy	t_{DB}	120	-	-	ns	
$\overline{RES}$ to Write Setup Time	t_{RP}	100	-	-	µs	
V_{CC} to $\overline{RES}$ Setup Time	t_{RES}	1	-	-	µs	

Notes: 1. Use this device in longer cycle than this value.
2. Write Enable controlled operation.
3. Chip Enable controlled operation.

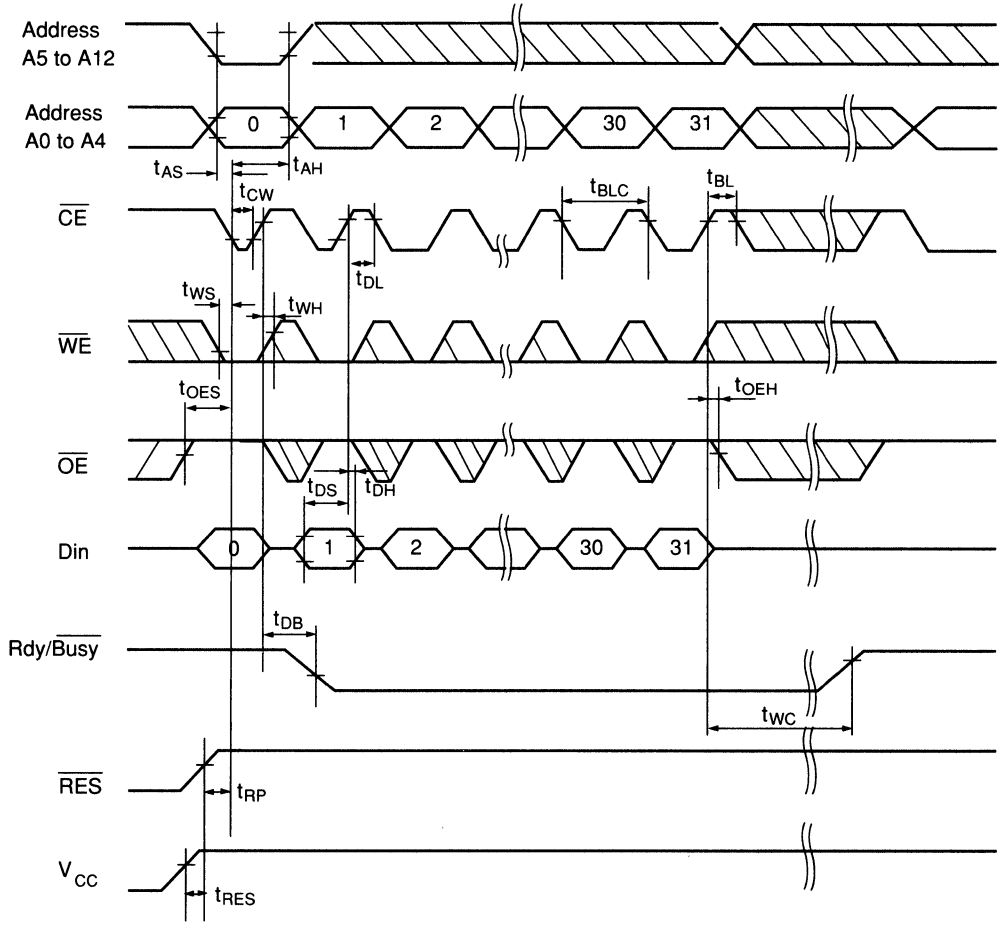
5

■ PAGE ERASE AND PAGE WRITE TIMING WAVEFORM ($\overline{WE}$ Controlled)



(TD.PE1.HN58C66)

■ PAGE ERASE AND PAGE WRITE TIMING WAVEFORM ($\overline{CE}$ Controlled)



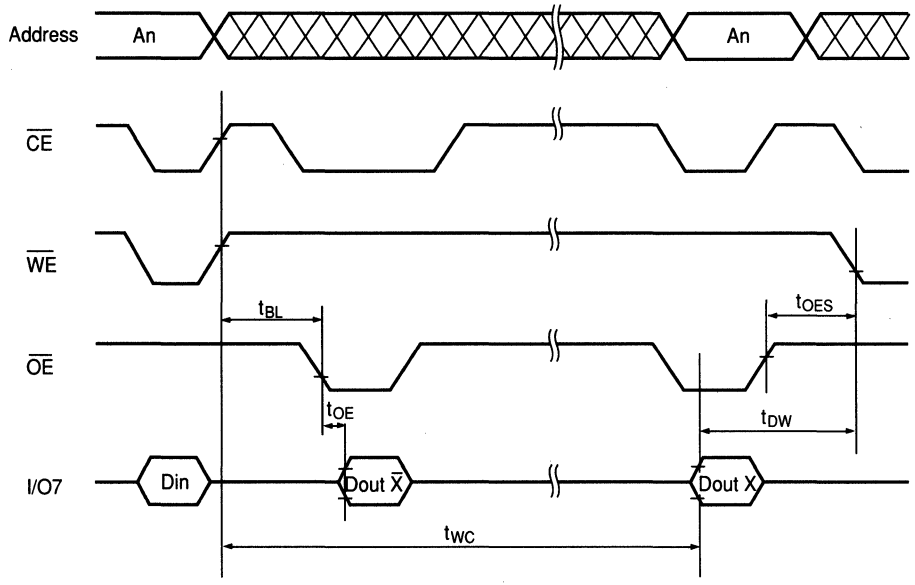
(TD.PE2.HN58C66)

5

■ AC ELECTRICAL CHARACTERISTICS FOR $\overline{\text{DATA}}$ POLLING OPERATION

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Byte Load Window	t_{BL}	100	-	-	µs	
Output Enable to Output Delay	t_{OE}	10	-	90	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Write Start Time	t_{DW}	150	-	-	ns	
Write Cycle Time	t_{WC}	-	-	10	ms	

■ $\overline{\text{DATA}}$ POLLING TIMING WAVEFORM



(TD.DP.EE)

■ FUNCTIONAL DESCRIPTION

Automatic Page Write

The Page Write feature allows 1 to 32 Bytes of data to be written into the EEPROM in a single write cycle andthe undefined data within 32 Bytes to be written corresponding to the undefined address (A_0 to A_4). Each additional Byte load cycle must be started within 30 µs from the preceding falling edge of $\overline{WE}$ or $\overline{CE}$. If $\overline{CE}$ and $\overline{WE}$ are kept high for 100 µs after data input, the EEPROM automatically enters erase and write mode and only the input data is written into the EEPROM. Data can be written and accessed 10^5 times in 32 Byte units.

$\overline{\text{Data}}$ Polling

$\overline{\text{Data}}$ Polling allows the status of the EEPROM to be determined. If the EEPROM is set to Read mode during a Write cycle, an inversion of the last Byte of data to be loaded outputs from I/O_7 to indicate that the EEPROM is performing a Write operation.

Ready/$\overline{\text{Busy}}$ Signal

The Ready/$\overline{\text{Busy}}$ signal also allows the status of the EEPROM to be determined. The Ready/$\overline{\text{Busy}}$ signal is high impedence except in the write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, the Ready/$\overline{\text{Busy}}$ signal changes to high impedence.

$\overline{\text{WE}}$ and $\overline{\text{CE}}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

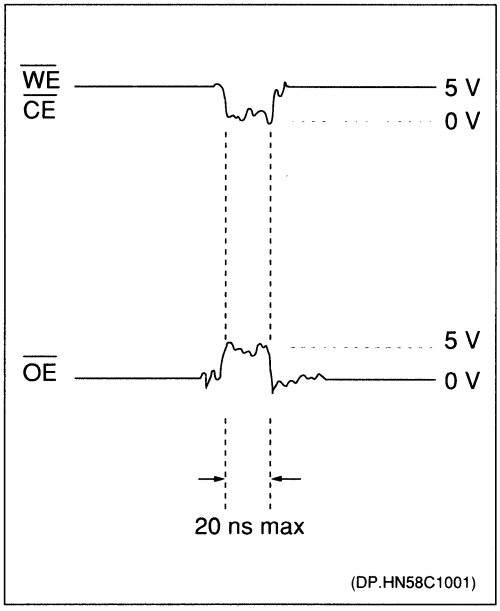
Write/Erase Endurance and Data Retention

The endurance with page programming is 10^5 cycles (1% cumulative failure rate) and the data retention time is more than 10 years when a device is programmed less than 10^4 cycles.

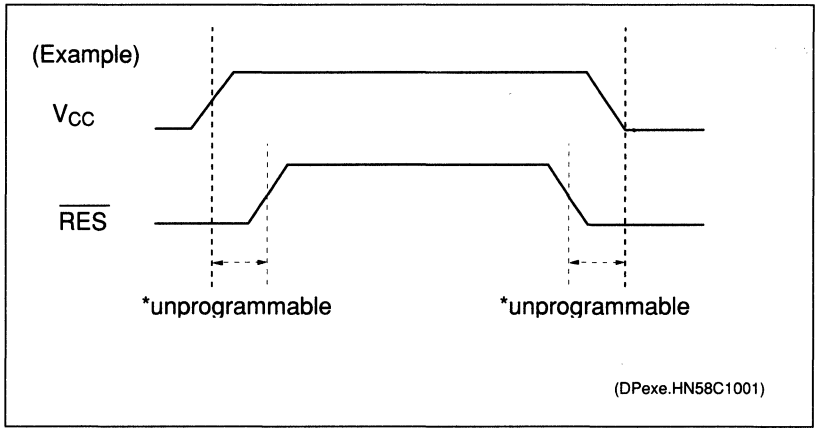
Data Protection

To protect the data during operation and power on/off, the HN58C66 has:

1. Data protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation.
   During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. To prevent this phenomenon, the HN58C66 has a noise cancellation function that cuts noise if its width is 20 ns or less in programming mode. Be careful not to allow noise of a width of more than 20 ns on the control pins.



5



■ **FUNCTIONAL DESCRIPTION (continued)**

Data Protection (continued)

2. Data protection at V_{CC} on/off
   When $\overline{RES}$ is low, the EEPROM cannot be erased and programmed. Therefore, data can be protected by keeping $\overline{RES}$ low when V_{CC} is switched. $\overline{RES}$ should be high during programming because it does not provide a latch function.
   When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may turn the EEPROM to programming mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable, standby or readout state by using a CPU reset signal to $\overline{RES}$ pin.
   In addition, when $\overline{RES}$ is kept high at V_{CC} on/off timing, the input level of control pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) must be held as $\overline{CE}$=V_{CC} or $\overline{OE}$=Low or $\overline{WE}$=V_{CC} level.

HN58C256 Series

256K (32K x 8-bit) EEPROM

■ DESCRIPTION

The Hitachi HN58C256 is a 256-Kilobit CMOS Electrically Erasable Programmable Read Only Memory (EEPROM) organized as 32,768 x 8-bits. The HN58C256 is capable of in-system electrical Byte and Page reprogrammability.

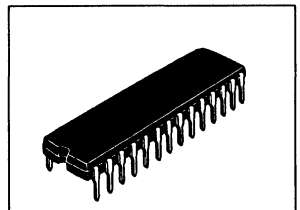
The HN58C256 achieves fast address access, low power consumption, and a high level of reliability by employing advanced MNOS memory technology and CMOS process and circuitry technology.

The HN58C256 has a 64-Byte Page Programming function to make its erase and write operations faster. The HN58C256 features $\overline{\text{Data}}$ Polling to indicate completion of erase and programming operations.

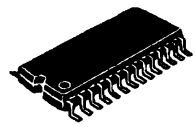
The HN58C256 provides several levels of data protection. Hardware data protection is provided with noise protection on the $\overline{\text{WE}}$ signal and write inhibit on power on and off.

The HN58C256 is designed for high reliability in the most demanding applications. Data retention is specified for 10 years and erase/write endurance is guaranteed to a minimum of 100,000 cycles in the Page Mode.

The Hitachi HN58C256 is offered in JEDEC-Standard Byte-Wide EEPROM pinouts in 28-pin Plastic DIP and 28-lead SOP packages.



(DP-28)



(FP-28D)

■ FEATURES

- Single Power Supply:
  V_{CC} = 5V ± 10%
- Fast Access Time:
  200 ns (max)
- Low Power Dissipation:
  Active Current: 20 mW/MHz (typ)
  Standby Current: 200 µW (typ)
- Automatic Programming:
  Automatic Page Write: 10 ms (max)
  64 Byte Page Size
  Automatic Byte Write: 10 ms (max)
- $\overline{\text{Data}}$ Polling
- Data Protection Circuitry on Power On/Off
- Data Retention: 10 years
- Erase/Write Endurance:
  100,000 cycles in Page Mode
- Pin Arrangement:
  JEDEC Standard Byte-Wide EEPROM
- Packages:
  28-pin Plastic DIP
  28-lead Plastic SOP

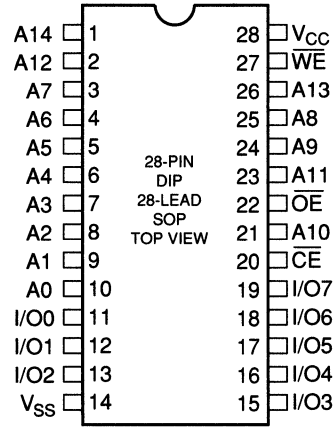
5

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN58C256P-20	200 ns	28-pin Plastic DIP (DP-28)
HN58C256FP-20	200 ns	28-lead Plastic SOP (FP-28D)

■ PIN ARRANGEMENT

HN58C256P Series
HN58C256FP Series

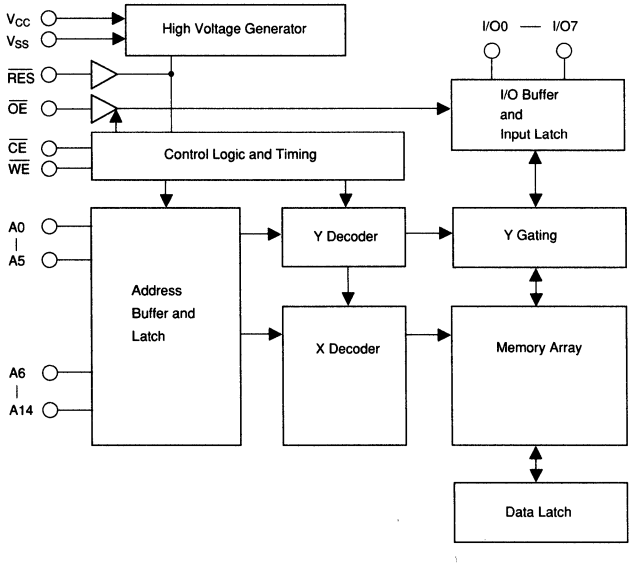


(PinD32.HN58C256)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{14}	Address
I/O_0 - I/O_7	Input/Output
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground

■ BLOCK DIAGRAM



(BD.HN58C256)

■ MODE SELECTION

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby	V_{IH}	X	X	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Deselect	V_{IL}	V_{IH}	V_{IH}	High-Z
Write Inhibit	X	X	V_{IH}	-
	X	V_{IL}	X	
$\overline{Data}$ Polling	V_{IL}	V_{IL}	V_{IH}	Data Out (I/O_7)

Note: 1. X = Don't Care

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Input Voltage [1]	V_{IN}	-0.5[2] to +7.0	V
Operating Temperature Range [3]	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C

Notes: 1. Relative to V_{SS}.
2. V_{IN} min = -3.0V for pulse width ≤ 50 ns.
3. Including electrical characterisitics and data retention.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	-	-	6	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	-	-	12	pF	V_{OUT} = 0V

5

■ DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{CC} = 5.5 V, V_{IN} = 5.5 V
Output Leakage Current	I_{LO}	-	-	2	µA	V_{CC} = 5.5 V, V_{OUT} = 5.5 V/0.4 V
Standby V_{CC} Current	I_{CC1}	-	-	200	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	-	-	1	mA	$\overline{CE}$ = V_{IH}
Operating V_{CC} Current	I_{CC3}	-	-	12	mA	I_{OUT} = 0 mA, Duty = 100%, Cycle = 1 µs
		-	-	30	mA	I_{OUT} = 0 mA, Duty = 100%, Cycle = 200 ns
Input Voltage	V_{IL}	-0.3 [1]	-	0.8	V	
	V_{IH}	2.2	-	V_{CC} + 1	V	
Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA

Notes: 1. V_{IL} min = -3.0 V for pulse width ≤ 50 ns.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(T_a = 0 to 70°C, V_{CC} = 5V ± 10%)

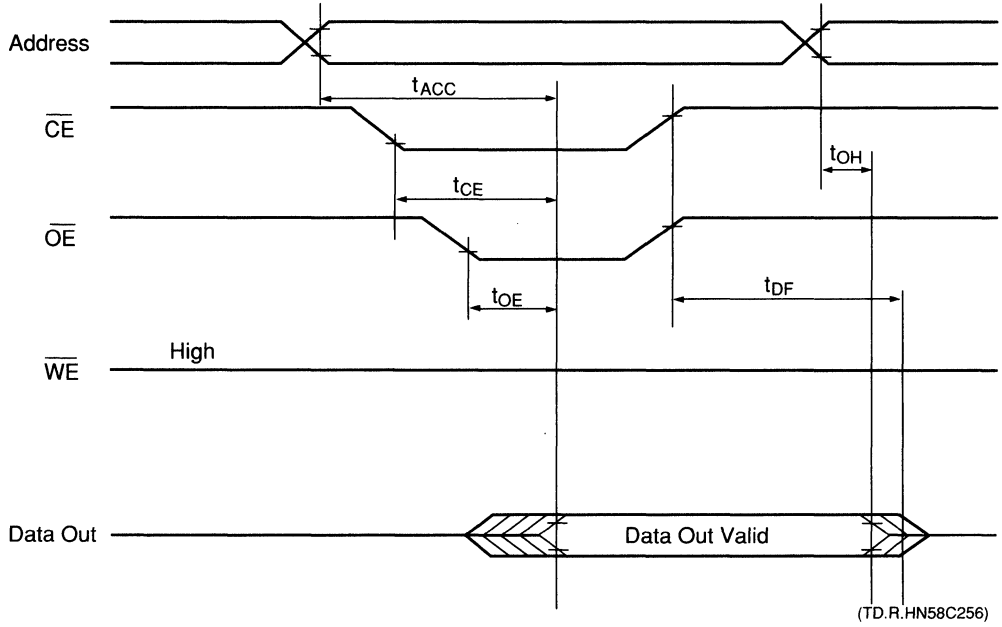
Test Conditions

- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall times: ≤ 20 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V, 2.0 V

Item	Symbol	HN58C256-20 Min.	HN58C256-20 Max.	Unit	Test Condition
Address Access Time	t_{ACC}	-	200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Chip Enable Access Time	t_{CE}	-	200	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Enable Access Time	t_{OE}	10	90	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Hold to Address Change	t_{OH}	0	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Disable to High-Z[1]	t_{DF}	0	60	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



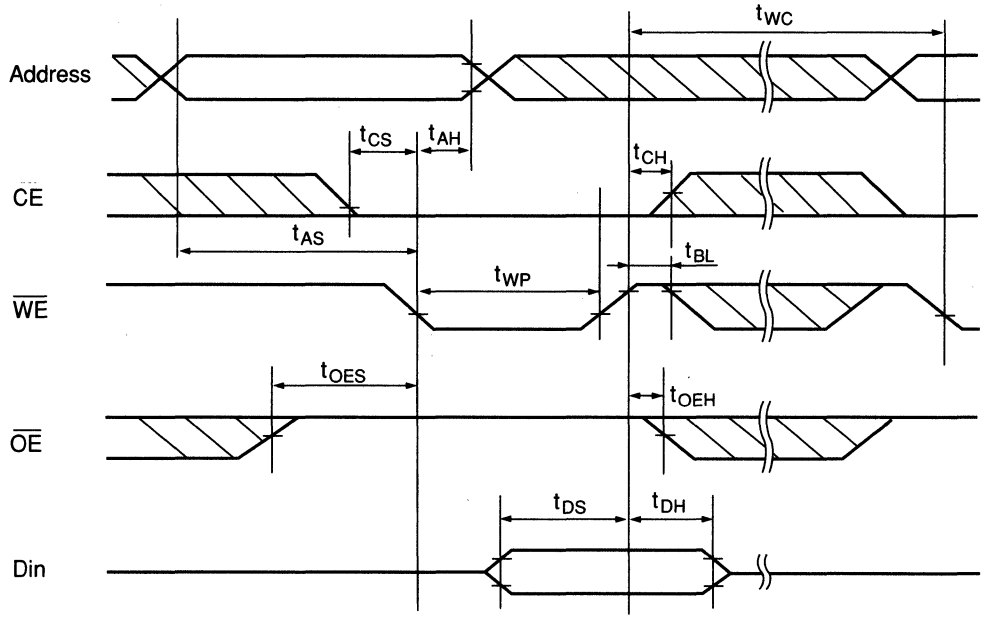
■ AC ELECTRICAL CHARACTERISTICS FOR BYTE ERASE AND BYTE WRITE OPERATIONS

Item	Symbol	Min.[1]	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	0	-	-	ns	
Write Enable to Write Setup Time	t_{WS}[3]	0	-	-	ns	
Chip Enable to Write Setup Time	t_{CS}[2]	0	-	-	ns	
Write Pulse Width	t_{CW}[3]	150	-	-	ns	
	t_{WP}[2]	150	-	-	ns	
Address Hold Time	t_{AH}	150	-	-	ns	
Data Setup Time	t_{DS}	100	-	-	ns	
Data Hold Time	t_{DH}	0	-	-	ns	
Write Enable Hold Time	t_{WH}[3]	0	-	-	ns	
Chip Enable Hold Time	t_{CH}[2]	0	-	-	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Output Enable Hold Time	t_{OEH}	0	-	-	ns	
Write Cycle Time	t_{WC}	10	-	-	ms	
Byte Load Window	t_{BL}	100	-	-	µs	

Note: 1. Use this device in a longer cycle than this value.
2. Write Enable controlled operation.
3. Chip Enable controlled operation.

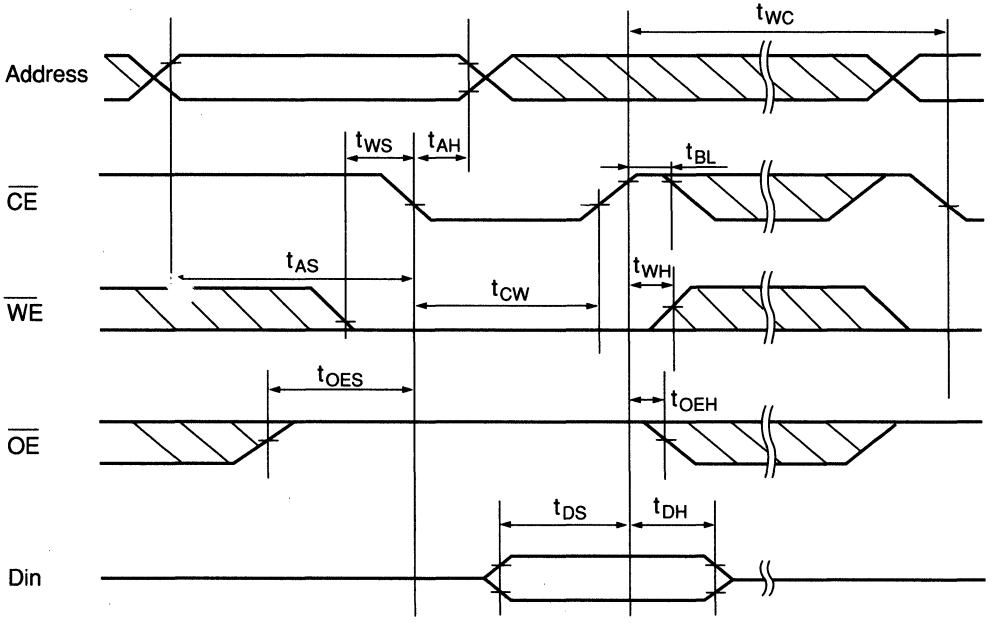
5

■ BYTE ERASE AND BYTE WRITE TIMING WAVEFORM ($\overline{WE}$ Controlled)



(TD.BE1.HN58C256)

■ BYTE ERASE AND BYTE WRITE TIMING WAVEFORM ($\overline{CE}$ Controlled)



(TD.BE2.HN58C256)

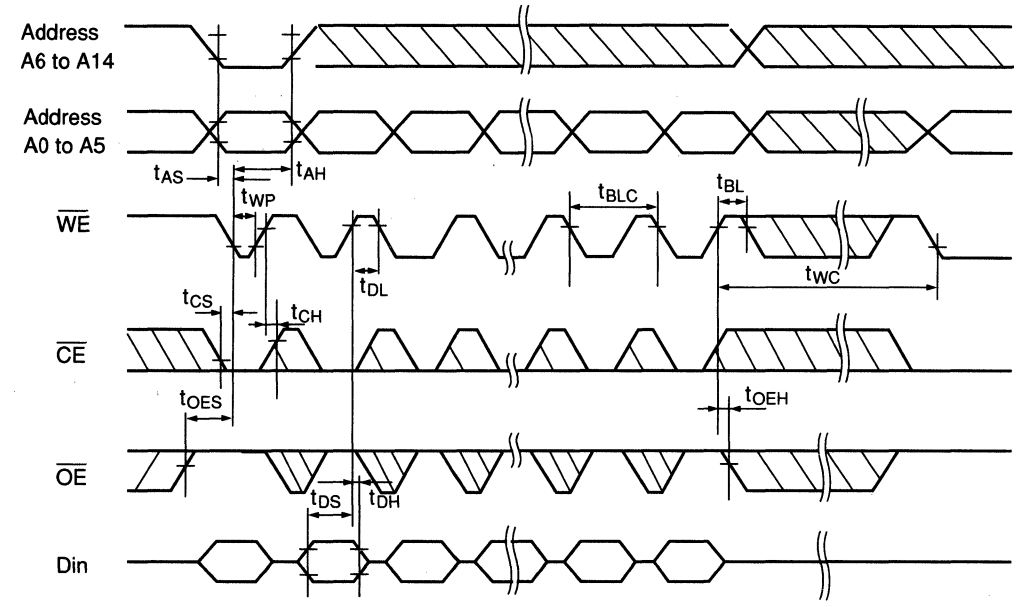
■ AC ELECTRICAL CHARACTERISTICS FOR PAGE ERASE AND PAGE WRITE OPERATIONS

Item	Symbol	Min.[1]	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	0	-	-	ns	
Write Enable to Write Setup Time	t_{WS}[3]	0	-	-	ns	
Chip Enable to Write Setup Time	t_{CS}[2]	0	-	-	ns	
Write Pulse Width	t_{WP}[2]	150	-	-	ns	
	t_{CW}[3]	150	-	-	ns	
Address Hold Time	t_{AH}	150	-	-	ns	
Data Setup Time	t_{DS}	100	-	-	ns	
Data Hold Time	t_{DH}	0	-	-	ns	
Write Enable Hold Time	t_{WH}[3]	0	-	-	ns	
Chip Enable Hold Time	t_{CH}[2]	0	-	-	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Output Enable Hold Time	t_{OEH}	0	-	-	ns	
Data Latch Time	t_{DL}	200	-	-	ns	
Write Cycle Time	t_{WC}	10	-	-	ms	
Byte Load Window	t_{BL}	100	-	-	µs	
Byte Load Cycle	t_{BLC}	0.3	-	30	µs	

Notes: 1. Use this device in longer cycle than this value.
2. Write Enable controlled operation.
3. Chip Enable controlled operation.

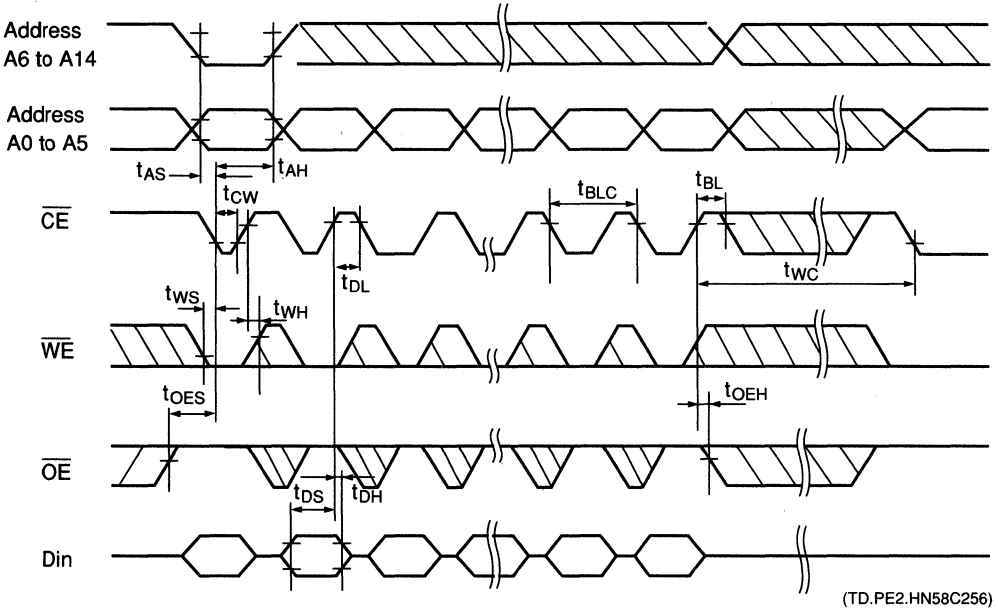
5

■ PAGE ERASE AND PAGE WRITE TIMING WAVEFORM ($\overline{WE}$ Controlled)



(TD.PE1.HN58C256)

■ PAGE ERASE AND PAGE WRITE TIMING WAVEFORM ($\overline{CE}$ Controlled)

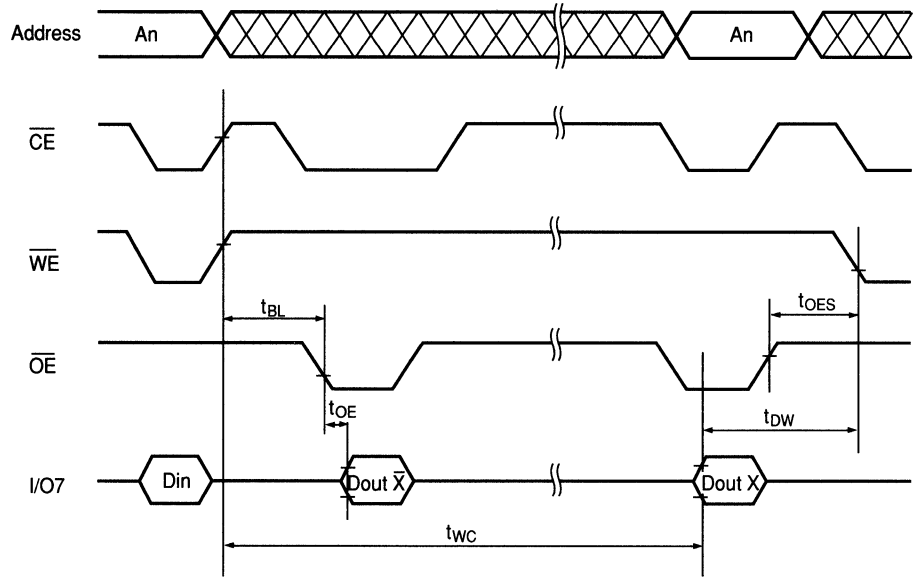


(TD.PE2.HN58C256)

■ AC ELECTRICAL CHARACTERISTICS FOR $\overline{DATA}$ POLLING OPERATION

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Byte Load Window	t_{BL}	100	-	-	µs	
Output Enable to Output Delay	t_{OE}	10	-	90	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Write Start Time	t_{DW}	150	-	-	ns	
Write Cycle Time	t_{WC}	-	-	10	ms	

■ $\overline{DATA}$ POLLING TIMING WAVEFORM



(TD.DP.EE)

5

■ FUNCTIONAL DESCRIPTION

Automatic Page Write

The Page Write feature allows 1 to 64 Bytes of data to be written into the EEPROM in a single write cycle. Following the initial Byte cycle, an additional 1 to 63 Bytes can be written in the same manner. Each additional Byte load cycle must be started within 30 µs from the preceding falling edge of $\overline{WE}$ or $\overline{CE}$. When $\overline{WE}$ or $\overline{CE}$ is high for 100 µs after data input, the EEPROM enters erase and write mode automatically and only the input data is written into the EEPROM. Data can be written and accessed 10^5 times in 64 Byte units.

$\overline{Data}$ Polling

Data Polling allows the status of the EEPROM to be determined. If the EEPROM is set to Read mode during a Write cycle, an inversion of the last Byte of data to be loaded outputs from I/O_7 to indicate that the EEPROM is performing a Write operation.

$\overline{WE}$ and $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

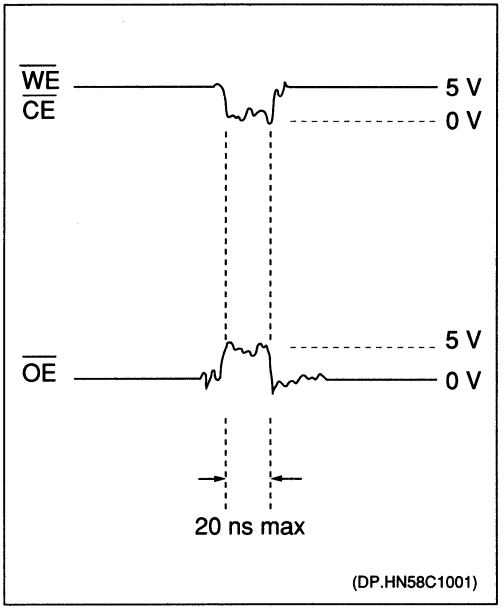
Write/Erase Endurance and Data Retention

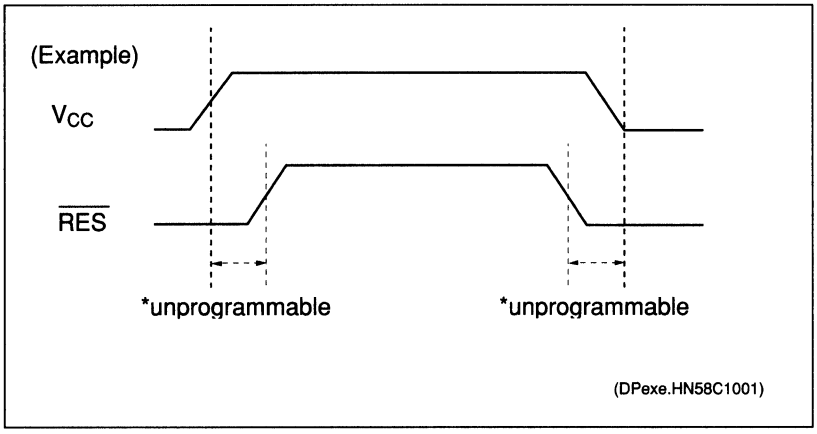
The endurance with page programming is 10^5 cycles (1% cumulative failure rate) and the data retention time is more than 10 years when a device is programmed less than 10^4 cycles.

Data Protection

To protect the data during operation and power on/off, the HN58C256 has:

1. Data protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation.
   During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. To prevent this phenomenon, the HN58C256 has a noise cancellation function that cuts noise if its width is 20 ns or less in programming mode. Be careful not to allow noise of a width of more than 20 ns on the control pins.





■ FUNCTIONAL DESCRIPTION (continued)

Data Protection (continued)

2. Data protection at V_{CC} on/off
   When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may turn the EEPROM to programming mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPU is in an unstable state.
   In addition, when V_{CC} is turned on or off, the input level of the control pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) must be held as $\overline{CE}$=V_{CC} or $\overline{OE}$=Low or $\overline{WE}$=V_{CC} level.

5

HN58C257 Series

256K (32K x 8-bit) EEPROM

■ DESCRIPTION

The Hitachi HN58C257 is a 256-Kilobit CMOS Electrically Erasable Programmable Read Only Memory (EEPROM) organized as 32,768 x 8-bits. The HN58C257 is capable of in-system electrical Byte and Page reprogrammability.

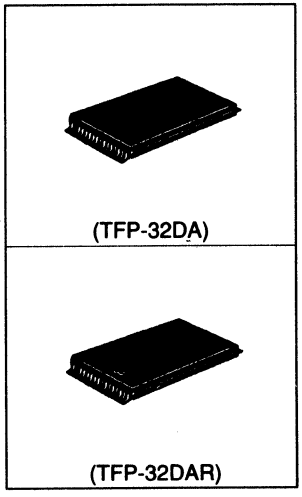
The HN58C257 achieves high speed access, low power consumption, and a high level of reliability by employing advanced MNOS memory technology and CMOS process and circuitry technology.

The HN58C257 has a 64-Byte Page Programming function to make its erase and write operations faster. The HN58C257 features $\overline{\text{Data}}$ Polling and a Ready/$\overline{\text{Busy}}$ signal to indicate completion of erase and programming operations.

The HN58C257 provides several levels of data protection. Hardware data protection is provided with the $\overline{\text{RES}}$ pin, in addition to noise protection on the $\overline{\text{WE}}$ signal and write inhibit on power on and off.

The HN58C257 is designed for high reliability in the most demanding applications. Data retention is specified for 10 years and erase/write endurance is guaranteed to a minimum of 100,000 cycles in the Page Mode.

The HN58C257 is offered in a 32-lead Plastic TSOP package in both standard and reverse bend pinouts.



(TFP-32DA)

(TFP-32DAR)

■ FEATURES

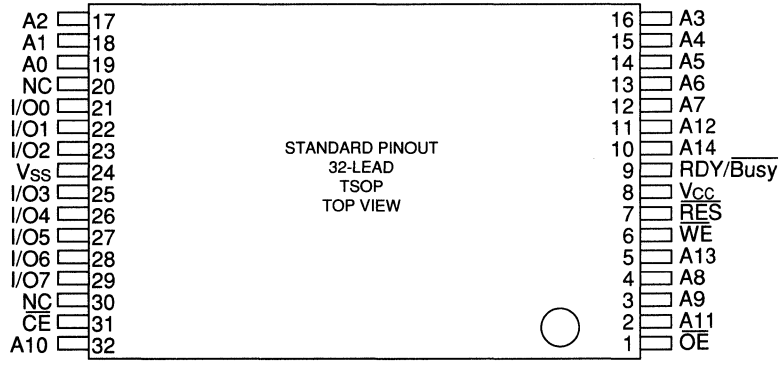
- Single Power Supply:
  V_{cc} = 5V ± 10%
- Fast Access Time:
  200 ns (max)
- Low Power Dissipation:
  Active Current: 20 mW/MHz (typ)
  Standby Current: 200 µW (typ)
- Automatic Programming:
  Automatic Page Write: 10 ms (max)
  64 Byte Page Size
  Automatic Byte Write: 10 ms (max)
- $\overline{\text{Data}}$ Polling and Ready/$\overline{\text{Busy}}$ Signals
- Hardware Data Protection with $\overline{\text{RES}}$ pin
- Data Protection Circuitry on Power On/Off
- Data Retention: 10 years
- Erase/Write Endurance:
  100,000 cycles in Page Mode
- Packages:
  32-lead Plastic TSOP (Type I)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN58C257T-20	200 ns	32-lead Plastic TSOP (TFP-32DA)
HN58C257R-20	200 ns	32-lead Plastic TSOP (TFP-32DAR) Reverse bend

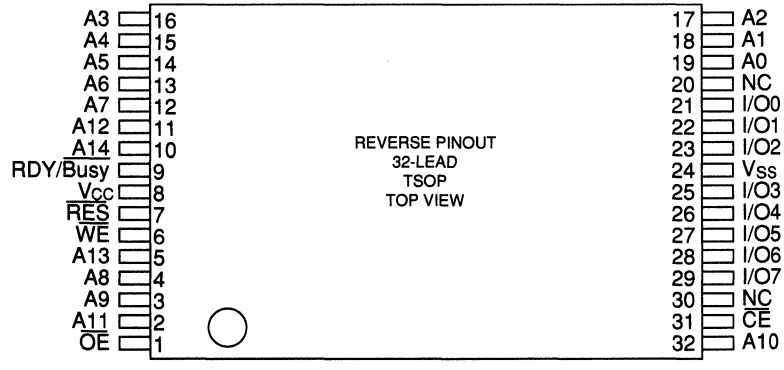
■ PIN ARRANGEMENT

HN58C257T Series



(PinT132.HN58C257T)

HN58C257R Series



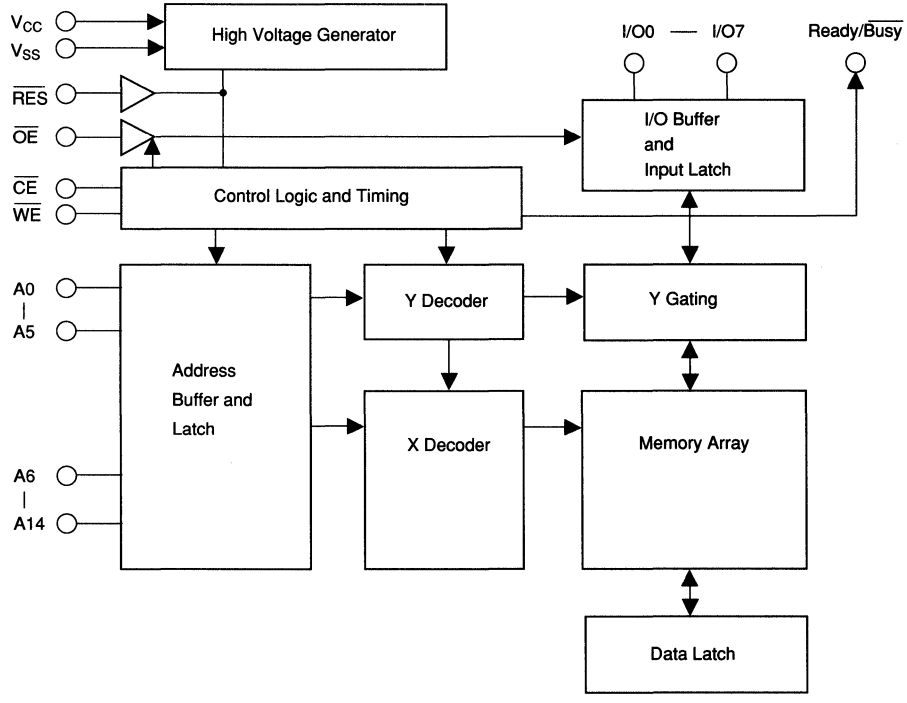
(PinT132.HN58C257R)

5

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{14}	Address
I/O_0 - I/O_7	Input/Output
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground
Rdy/$\overline{Busy}$	Ready/Busy
$\overline{RES}$	Reset

■ BLOCK DIAGRAM



(BD.HN58C257)

■ MODE SELECTION

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RES}$	RDY/$\overline{Busy}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_H	High-Z	D_{OUT}
Standby	V_{IH}	X	X	X	High-Z	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	V_H	High-Z→V_{OL}	D_{IN}
Deselect	V_{IL}	V_{IH}	V_{IH}	V_H	High-Z	High-Z
Write Inhibit	X	X	V_{IH}	X	High-Z	-
	X	V_{IL}	X	X	High-Z	-
$\overline{Data}$ Polling	V_{IL}	V_{IL}	V_{IH}	V_H	V_{OL}	Data Out (I/O_7)
Program	X	X	X	V_{IL}	High-Z	High-Z

Note: 1. X = Don't Care

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Input Voltage [1]	V_{IN}	-0.5[2] to +7.0	V
Operating Temperature Range [3]	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C

Notes: 1. Relative to V_{SS}.
2. V_{IN} min = -3.0V for pulse width ≤ 50 ns.
3. Including electrical characterisitics and data retention.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	-	-	6	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	-	-	12	pF	V_{OUT} = 0V

5

■ DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI} [1]	-	-	2	µA	V_{CC} = 5.5 V, V_{IN} = 5.5 V
Output Leakage Current	I_{LO}	-	-	2	µA	V_{CC} = 5.5 V, V_{OUT} = 5.5 V/0.4 V
Standby V_{CC} Current	I_{CC1}	-	-	200	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	-	-	1	mA	$\overline{CE}$ = V_{IH}
Operating V_{CC} Current	I_{CC3}	-	-	12	mA	I_{OUT} = 0 mA, Duty = 100%, Cycle = 1 µs
		-	-	30	mA	I_{OUT} = 0 mA, Duty = 100%, Cycle = 200 ns
Input Voltage	V_{IL}	-0.3 [2]	-	0.8	V	
	V_{IH}	2.2	-	V_{CC} + 1	V	
	V_H	V_{CC} - 0.5	-	V_{CC} + 1	V	
Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA

Notes: 1. I_{LI} on $\overline{RES}$ = 100 mA max.
2. V_{IL} min = -3.0 V for pulse width ≤ 50 ns.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(T_a = 0 to 70°C, V_{CC} = 5V ± 10%)

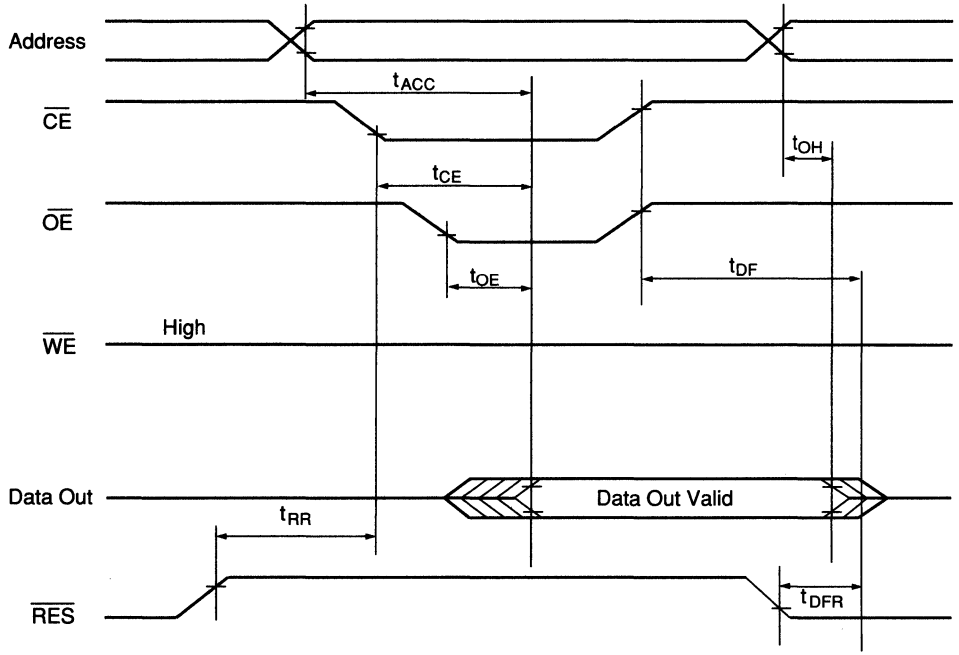
Test Conditions

- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall times: ≤ 20 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V, 2.0 V

Item	Symbol	HN58C257-20 Min.	HN58C257-20 Max.	Unit	Test Condition
Address Access Time	t_{ACC}	-	200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Chip Enable Access Time	t_{CE}	-	200	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Enable Access Time	t_{OE}	10	90	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Hold to Address Change	t_{OH}	0	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Disable to High-Z[1]	t_{DF}	0	70	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
	t_{DFR}	0	350	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ to Output Delay	t_{RR}	0	450	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



(TD.R.HN58C1001)

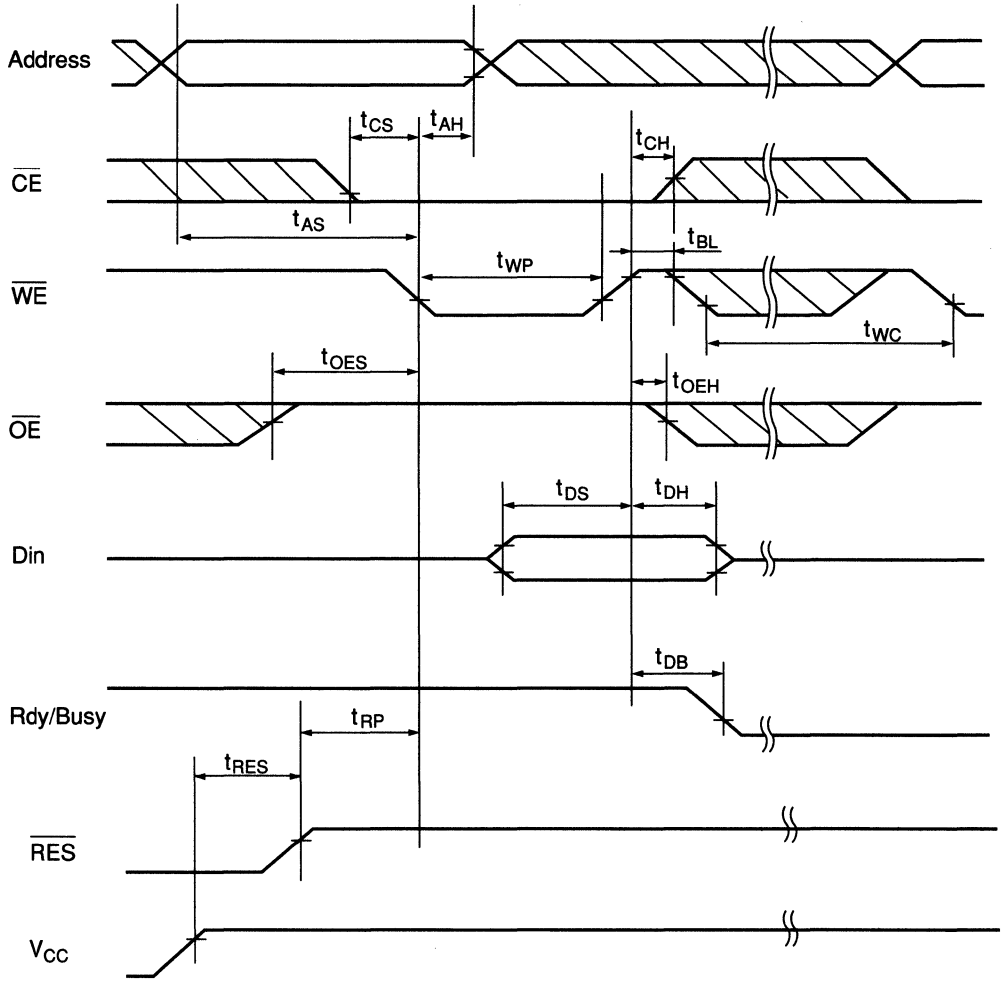
■ AC ELECTRICAL CHARACTERISTICS FOR BYTE ERASE AND BYTE WRITE OPERATIONS

Item	Symbol	Min.[1]	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	0	-	-	ns	
Write Enable to Write Setup Time	t_{WS}	0	-	-	ns	
Chip Enable to Write Setup Time	t_{CS}	0	-	-	ns	
Write Pulse Width	t_{CW}	150	-	-	ns	
	t_{WP}	150	-	-	ns	
Address Hold Time	t_{AH}	150	-	-	ns	
Data Setup Time	t_{DS}	100	-	-	ns	
Data Hold Time	t_{DH}	0	-	-	ns	
Write Enable Hold Time	t_{WH}	0	-	-	ns	
Chip Enable Hold Time	t_{CH}	0	-	-	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Output Enable Hold Time	t_{OEH}	0	-	-	ns	
Write Cycle Time	t_{WC}	10	-	-	ms	
Byte Load Window	t_{BL}	100	-	-	µs	
Time to Device Busy	t_{DB}	120	-	-	ns	
$\overline{RES}$ to Write Setup Time	t_{RP}	100	-	-	µs	
V_{CC} to $\overline{RES}$ Setup Time	t_{RES}	1	-	-	µs	

Note: 1. Use this device in a longer cycle than this value.
2. $\overline{WE}$ controlled operation.
3. $\overline{CE}$ controlled operation.

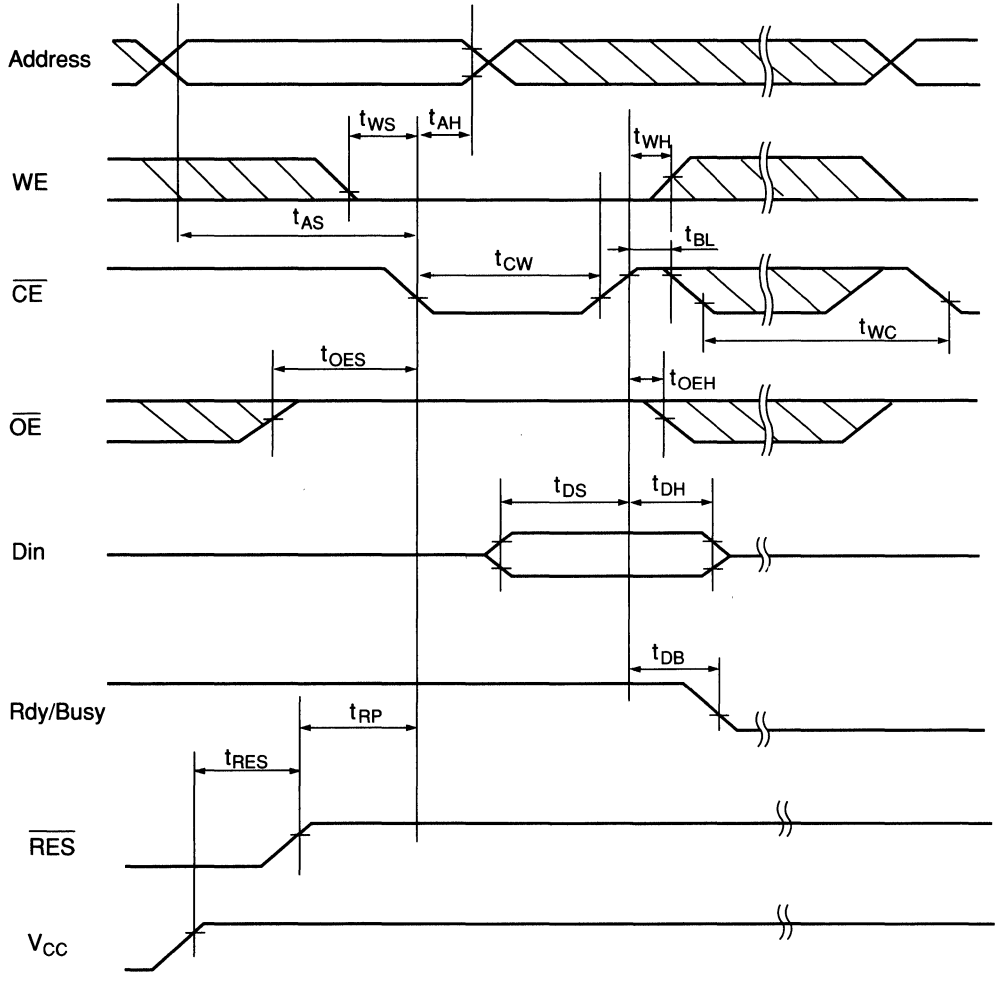
5

■ BYTE ERASE AND BYTE WRITE TIMING WAVEFORM ($\overline{WE}$ Controlled)



(TD.BE1.HN58C257)

■ BYTE ERASE AND BYTE WRITE TIMING WAVEFORM ($\overline{CE}$ Controlled)



(TD.BE2.HN58C257)

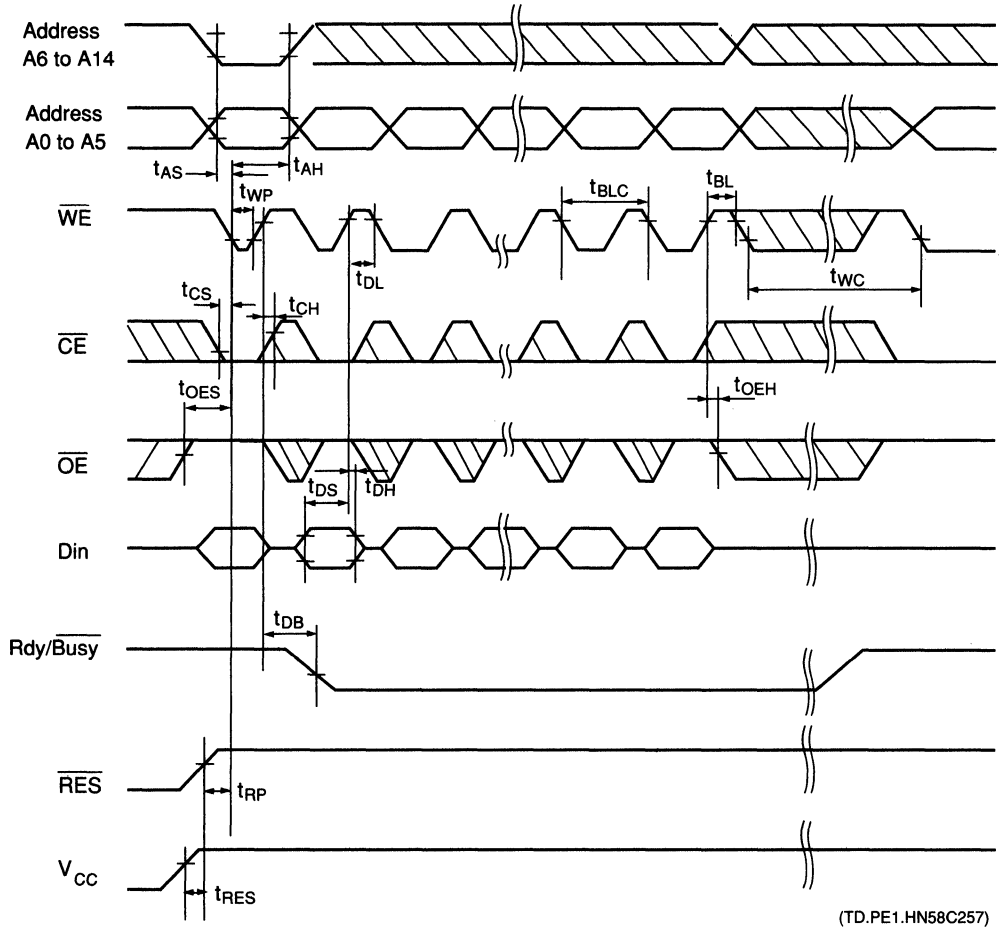
5

■ AC ELECTRICAL CHARACTERISTICS FOR PAGE ERASE AND PAGE WRITE OPERATIONS

Item	Symbol	Min.[1]	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	0	-	-	ns	
Write Enable to Write Setup Time	t_{WS}[3]	0	-	-	ns	
Chip Enable to Write Setup Time	t_{CS}[2]	0	-	-	ns	
Write Pulse Width	t_{WP}[2]	150	-	-	ns	
	t_{CW}[3]	150	-	-	ns	
Address Hold Time	t_{AH}	150	-	-	ns	
Data Setup Time	t_{DS}	100	-	-	ns	
Data Hold Time	t_{DH}	0	-	-	ns	
Write Enable Hold Time	t_{WH}[3]	0	-	-	ns	
Chip Enable Hold Time	t_{CH}[2]	0	-	-	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Output Enable Hold Time	t_{OEH}	0	-	-	ns	
Data Latch Time	t_{DL}	200	-	-	ns	
Write Cycle Time	t_{WC}	10	-	-	ms	
Byte Load Window	t_{BL}	100	-	-	µs	
Byte Load Cycle	t_{BLC}	0.3	-	30	µs	
Time to Device Busy	t_{DB}	120	-	-	ns	
$\overline{RES}$ to Write Setup Time	t_{RP}	100	-	-	µs	
V_{CC} to $\overline{RES}$ Setup Time	t_{RES}	1	-	-	µs	

Notes: 1. Use this device in longer cycle than this value.
2. $\overline{WE}$ controlled operation.
3. $\overline{CE}$ controlled operation.

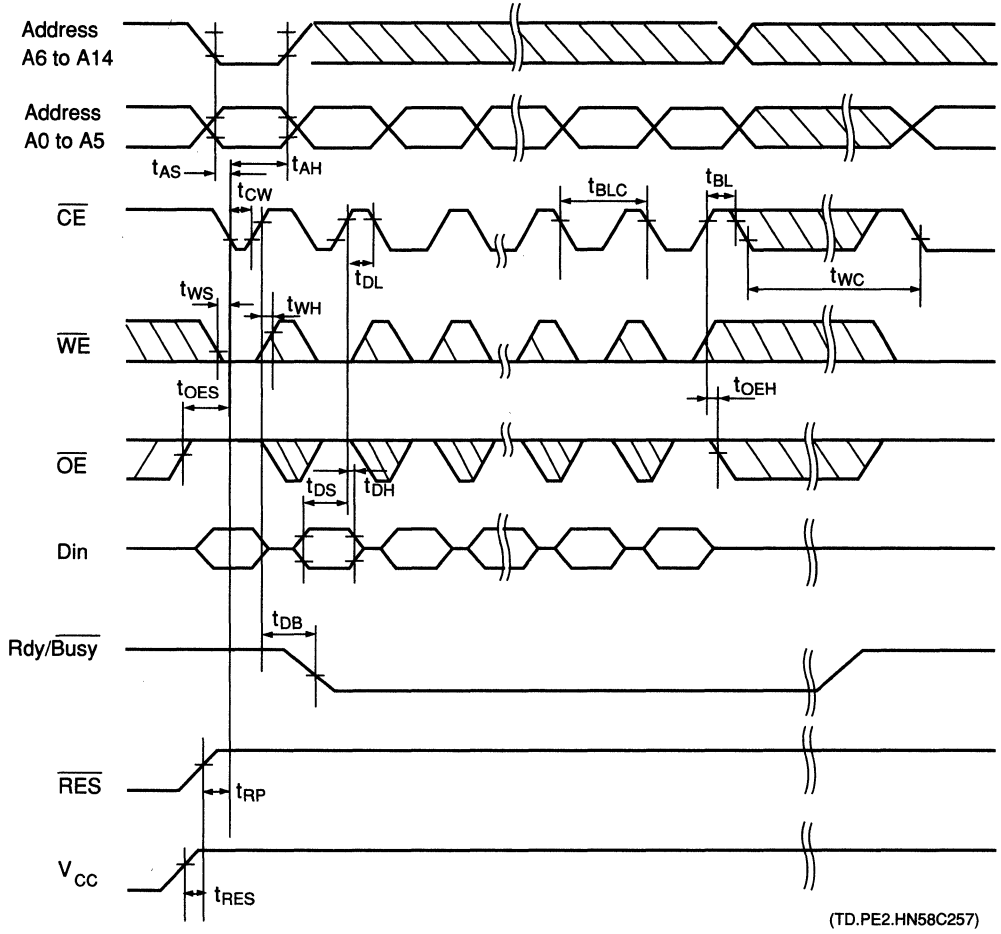
■ PAGE ERASE AND PAGE WRITE TIMING WAVEFORM ($\overline{WE}$ Controlled)



(TD.PE1.HN58C257)

5

■ PAGE ERASE AND PAGE WRITE TIMING WAVEFORM ($\overline{CE}$ Controlled)

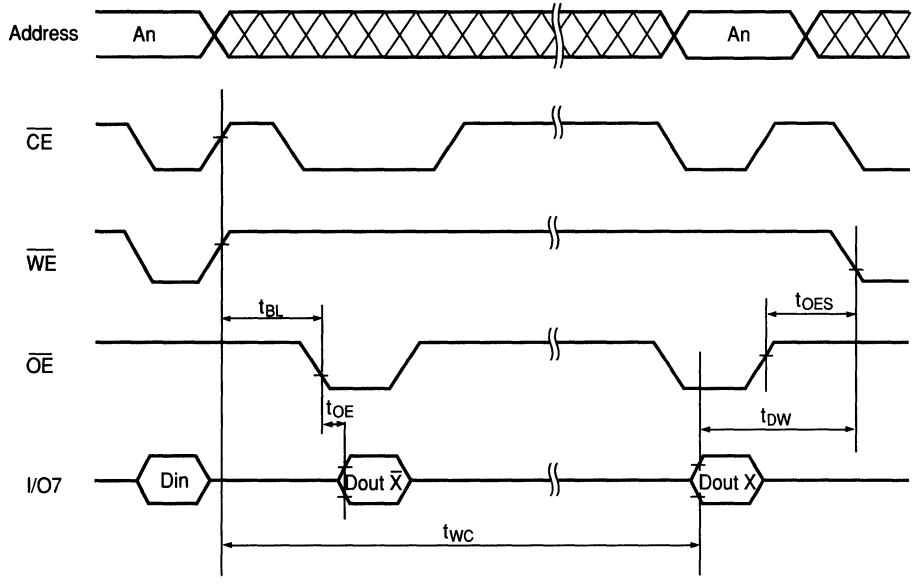


(TD.PE2.HN58C257)

■ AC ELECTRICAL CHARACTERISTICS FOR $\overline{DATA}$ POLLING OPERATION

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Byte Load Window	t_{BL}	100	-	-	µs	
Output Enable to Output Delay	t_{OE}	10	-	90	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Write Start Time	t_{DW}	150	-	-	ns	
Write Cycle Time	t_{WC}	-	-	10	ms	

■ $\overline{DATA}$ POLLING TIMING WAVEFORM



(TD.DP.EE)

5

■ FUNCTIONAL DESCRIPTION

Automatic Page Write

The Page Write feature allows 1 to 64 Bytes of data to be written into the EEPROM in a single write cycle. Following the initial Byte cycle, an additional 1 to 63 Bytes can be written in the same manner. Each additional Byte load cycle must be started within 30 µs from the preceding falling edge of $\overline{WE}$ or $\overline{CE}$. Data can be written and accessed 10^5 times in 64 Byte units.

$\overline{\text{Data}}$ Polling

$\overline{\text{Data}}$ Polling allows the status of the EEPROM to be determined. If the EEPROM is set to Read mode during a Write cycle, an inversion of the last Byte of data to be loaded outputs from I/O_7 to indicate that the EEPROM is performing a Write operation.

Ready/$\overline{\text{Busy}}$ Signal

The Ready/$\overline{\text{Busy}}$ signal also allows the status of the EEPROM to be determined. The Ready/$\overline{\text{Busy}}$ signal is high impedence except in the write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, the Ready/$\overline{\text{Busy}}$ signal changes to high impedence.

$\overline{WE}$ and $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

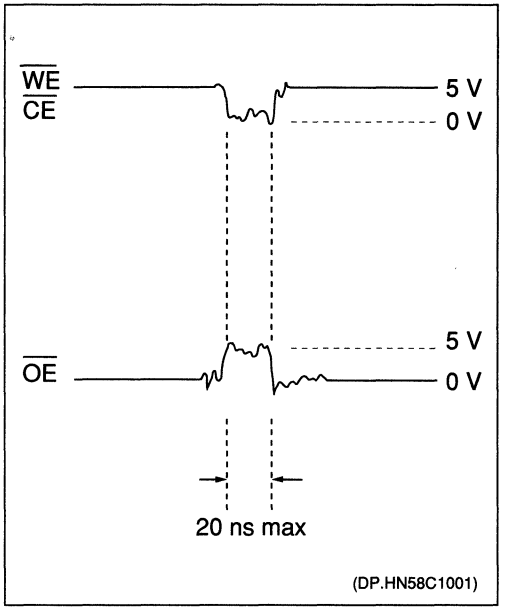
Write/Erase Endurance and Data Retention

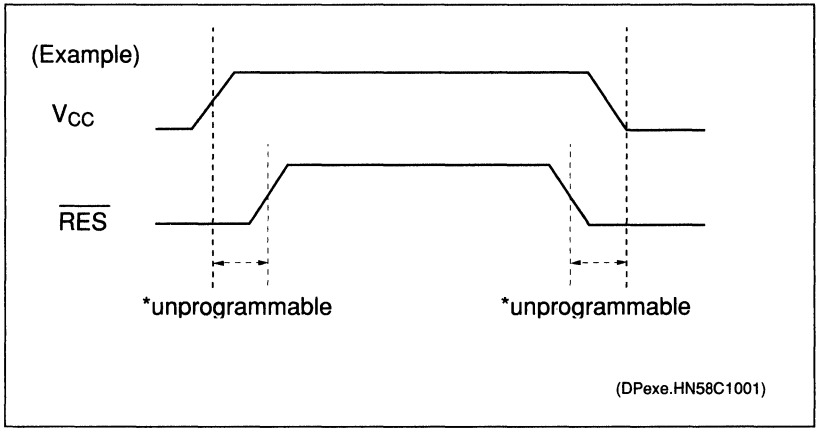
The endurance with page programming is 10^5 cycles (1% cumulative failure rate) and the data retention time is more than 10 years when a device is programmed less than 10^4 cycles.

Data Protection

To protect the data during operation and power on/off, the HN58C257 has:

1. Data protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation.
   During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. To prevent this phenomenon, the HN58C257 has a noise cancellation function that cuts noise if its width is 20 ns or less in programming mode. Be careful not to allow noise of a width of more than 20 ns on the control pins.





■ FUNCTIONAL DESCRIPTION (continued)

Data Protection (continued)

2. Data protection at V_{CC} on/off
   When $\overline{RES}$ is low, the EEPROM cannot be erased and programmed. Therefore, data can be protected by keeping $\overline{RES}$ low when V_{CC} is switched. $\overline{RES}$ should be high during programming because it does not provide a latch function.
   When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may turn the EEPROM to programming mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable, standby or readout state by using a CPU reset signal to $\overline{RES}$ pin.
   In addition, when $\overline{RES}$ is kept high at V_{CC} on/off timing, the input level of control pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) must be held as $\overline{CE}$=V_{CC} or $\overline{OE}$=Low or $\overline{WE}$=V_{CC} level.

5

HN58V257 Series

256K (32K x 8-bit) EEPROM

■ DESCRIPTION

The Hitachi HN58V257 is a 256-Kilobit CMOS Electrically Erasable Programmable Read Only Memory (EEPROM) organized as 32,768 x 8-bits. The HN58V257 is capable of in-system electrical Byte and Page reprogrammability.

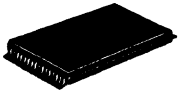
The HN58V257 achieves low supply voltage, low power consumption, and a high level of reliability by employing advanced MNOS memory technology and CMOS process and circuitry technology.

The HN58V257 has a 64-Byte Page Programming function to make its erase and write operations faster. The HN58V257 features $\overline{\text{Data}}$ Polling and a Ready/$\overline{\text{Busy}}$ signal to indicate completion of erase and programming operations.

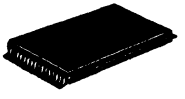
The HN58V257 provides several levels of data protection. Hardware data protection is provided with the $\overline{\text{RES}}$ pin, in addition to noise protection on the $\overline{\text{WE}}$ signal and write inhibit on power on and off.

The HN58V257 is designed for high reliability in the most demanding applications. Data retention is specified for 10 years and erase/write endurance is guaranteed to a minimum of 100,000 cycles in the Page Mode.

The HN58V257 is offered in a 32-lead Plastic TSOP package in both standard and reverse bend pinouts.



(TFP-32DA)



(TFP-32DAR)

■ FEATURES

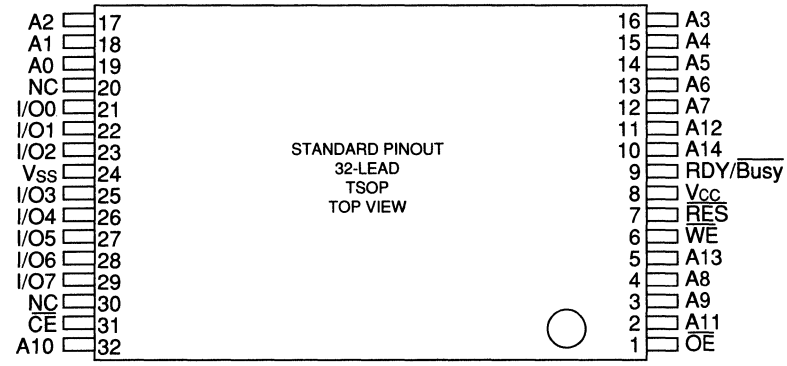
- Single Power Supply:
  V_{CC} = 3V ± 10%
- Access Time:
  350 ns (max)
- Low Power Dissipation:
  Active Current: 20 mW/MHz (typ)
  Standby Current: 100 µW (typ)
- Automatic Programming:
  Automatic Page Write: 15 ms (max)
  64 Byte Page Size
  Automatic Byte Write: 15 ms (max)
- $\overline{\text{Data}}$ Polling and Ready/$\overline{\text{Busy}}$ Signals
- Hardware Data Protection with $\overline{\text{RES}}$ pin
- Data Protection Circuitry on Power On/Off
- Data Retention: 10 years
- Erase/Write Endurance:
  100,000 cycles in Page Mode
- Packages:
  32-lead Plastic TSOP (Type I)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN58V257T-35	350 ns	32-lead Plastic TSOP (TFP-32DA)
HN58V257R-35	350 ns	32-lead Plastic TSOP (TFP-32DAR) Reverse bend

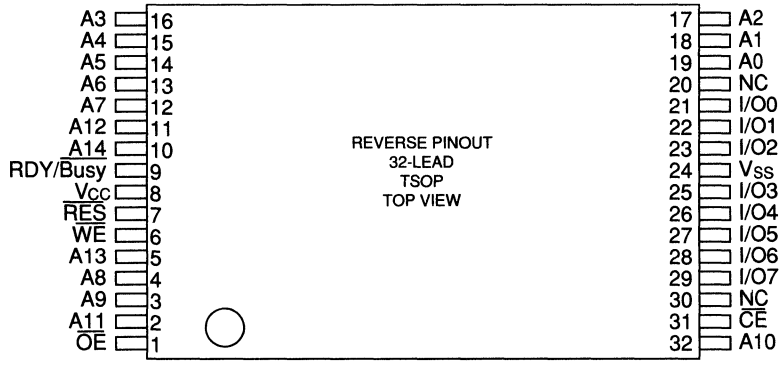
■ PIN ARRANGEMENT

HN58V257T Series



(PinT132.HN58C257T)

HN58V257R Series



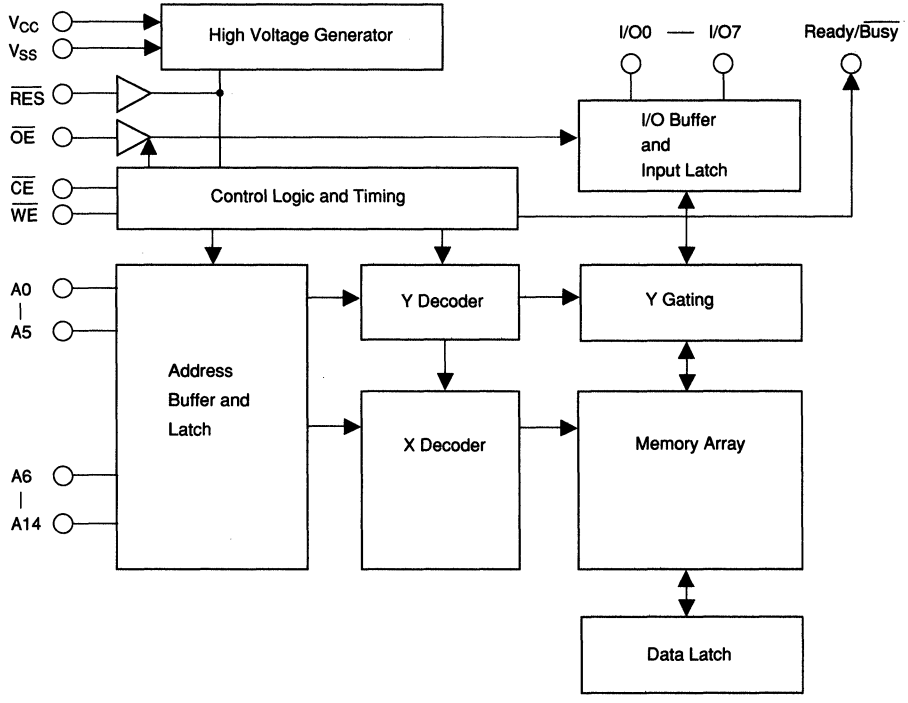
(PinT132.HN58C257R)

5

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{14}	Address
I/O_0 - I/O_7	Input/Output
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground
Rdy/$\overline{Busy}$	Ready/Busy
$\overline{RES}$	Reset

■ BLOCK DIAGRAM



(BD.HN58C257)

■ MODE SELECTION

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RES}$	RDY/$\overline{Busy}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_H	High-Z	D_{OUT}
Standby	V_{IH}	X	X	X	High-Z	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	V_H	High-Z→V_{OL}	D_{IN}
Deselect	V_{IL}	V_{IH}	V_{IH}	V_H	High-Z	High-Z
Write Inhibit	X	X	V_{IH}	X	High-Z	-
	X	V_{IL}	X	X	High-Z	-
$\overline{Data}$ Polling	V_{IL}	V_{IL}	V_{IH}	V_H	V_{OL}	Data Out (I/O_7)
Program	X	X	X	V_{IL}	High-Z	High-Z

Note: 1. X = Don't Care

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Input Voltage [1]	V_{IN}	-0.5[2] to +7.0	V
Operating Temperature Range [3]	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C

Notes: 1. Relative to V_{SS}.
2. V_{IN} min = -3.0V for pulse width ≤ 50 ns.
3. Including electrical characterisitics and data retention.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	-	-	6	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	-	-	12	pF	V_{OUT} = 0V

5

■ DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7 to 5.5V, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI} [1]	-	-	2	µA	V_{CC} = 5.5 V, V_{IN} = 5.5 V
Output Leakage Current	I_{LO}	-	-	2	µA	V_{CC} = 5.5 V, V_{OUT} = 5.5 V/0.4 V
Standby V_{CC} Current	I_{CC1}	-	-	20	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	-	-	1	mA	$\overline{CE}$ = V_{IH}
Operating V_{CC} Current	I_{CC3}	-	-	6	mA	I_{OUT} = 0 mA, V_{CC} = 3.3 V,Duty = 100%, Cycle = 1 µs
		-	-	15	mA	I_{OUT} = 0 mA, V_{CC} = 3.3 V,Duty = 100%, Cycle = 350 ns
Input Voltage	V_{IL}	-0.3 [2]	-	0.8	V	
	V_{IH}	2.2	-	V_{CC}+0.3	V	
	V_H	V_{CC}- 0.5	-	V_{CC}+0.3	V	
Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2.1 mA
	V_{OH}	V_{CC}x 0.8	-	-	V	I_{OH} = -400 µA

Notes: 1. I_{LI} on $\overline{RES}$ = 100 mA max.
2. V_{IL} min = -3.0 V for pulse width ≤ 50 ns.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(T_a = 0 to 70°C, V_{CC} = 2.7 to 5.5V)

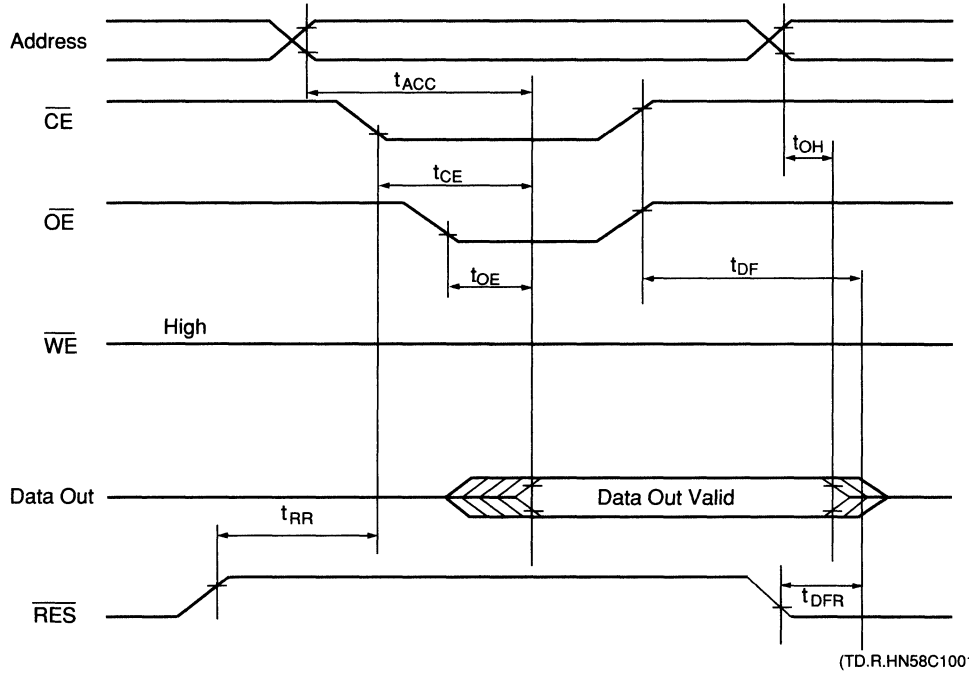
Test Conditions

- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall times: ≤ 20 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V, 2.0 V

Item	Symbol	HN58V257-35 Min.	HN58V257-35 Max.	Unit	Test Condition
Address Access Time	t_{ACC}	-	350	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Chip Enable Access Time	t_{CE}	-	350	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Enable Access Time	t_{OE}	10	150	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Hold to Address Change	t_{OH}	0	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Disable to High-Z[1]	t_{DF}	0	90	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
	t_{DFR}	0	350	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ to Output Delay	t_{RR}	0	600	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}

Note: 1.t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



(TD.R.HN58C1001)

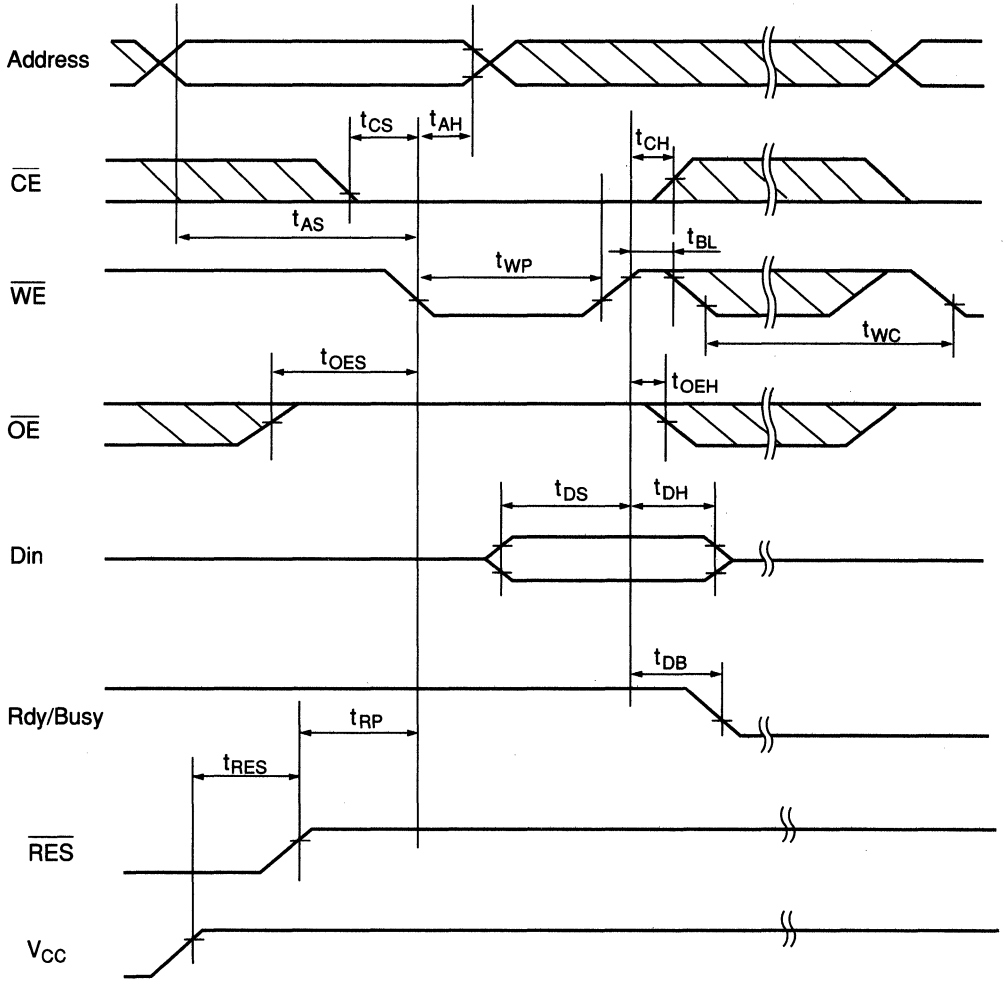
■ AC ELECTRICAL CHARACTERISTICS FOR BYTE ERASE AND BYTE WRITE OPERATIONS

Item	Symbol	Min.[1]	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	0	-	-	ns	
Write Enable to Write Setup Time	t_{WS}	0	-	-	ns	
Chip Enable to Write Setup Time	t_{CS}	0	-	-	ns	
Write Pulse Width	t_{CW}	250	-	-	ns	
	t_{WP}	250	-	-	ns	
Address Hold Time	t_{AH}	200	-	-	ns	
Data Setup Time	t_{DS}	150	-	-	ns	
Data Hold Time	t_{DH}	0	-	-	ns	
Write Enable Hold Time	t_{WH}	0	-	-	ns	
Chip Enable Hold Time	t_{CH}	0	-	-	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Output Enable Hold Time	t_{OEH}	0	-	-	ns	
Write Cycle Time	t_{WC}	15w	-	-	ms	
Byte Load Window	t_{BL}	100	-	-	µs	
Time to Device Busy	t_{DB}	120	-	-	ns	
$\overline{RES}$ to Write Setup Time	t_{RP}	100	-	-	µs	
V_{CC} to $\overline{RES}$ Setup Time	t_{RES}	1	-	-	µs	

Note: 1. Use this device in a longer cycle than this value.
2. $\overline{WE}$ controlled operation.
3. $\overline{CE}$ controlled operation.

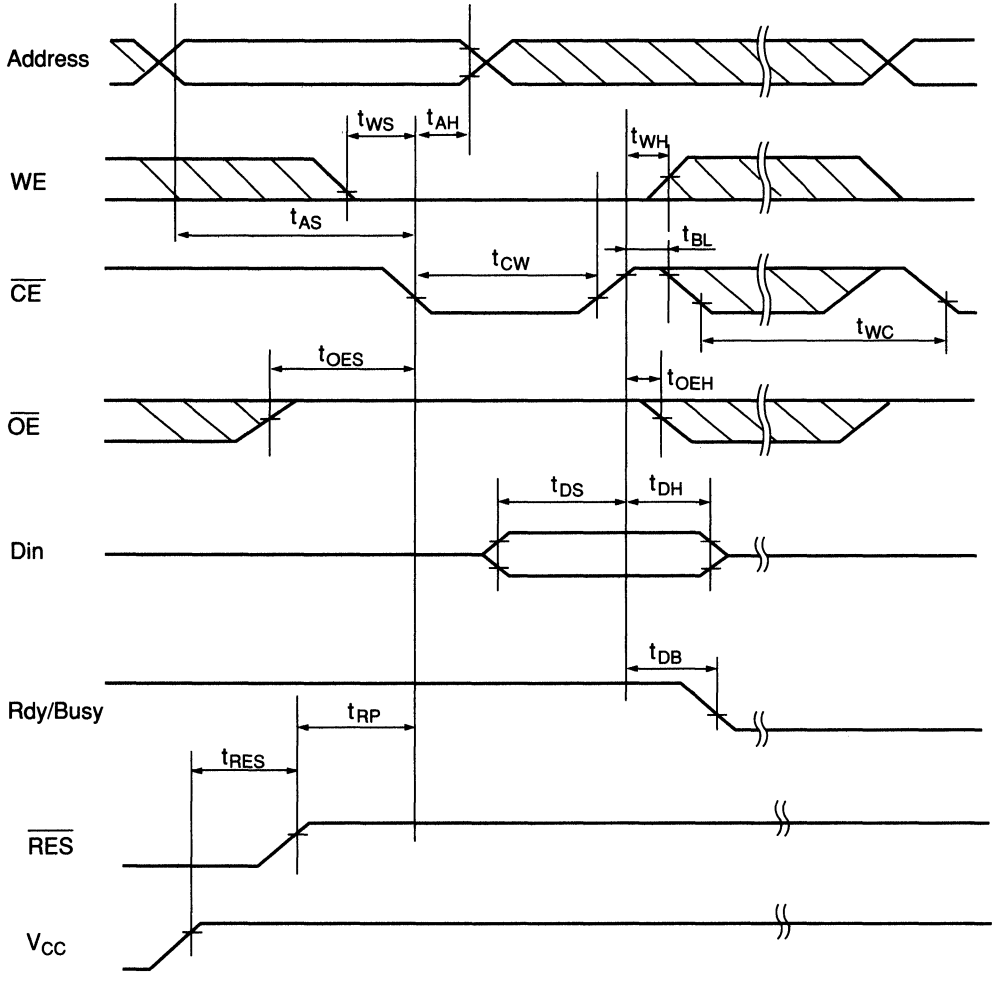
5

■ BYTE ERASE AND BYTE WRITE TIMING WAVEFORM ($\overline{WE}$ Controlled)



(TD.BE1.HN58C257)

■ BYTE ERASE AND BYTE WRITE TIMING WAVEFORM ($\overline{CE}$ Controlled)



(TD.BE2.HN58C257)

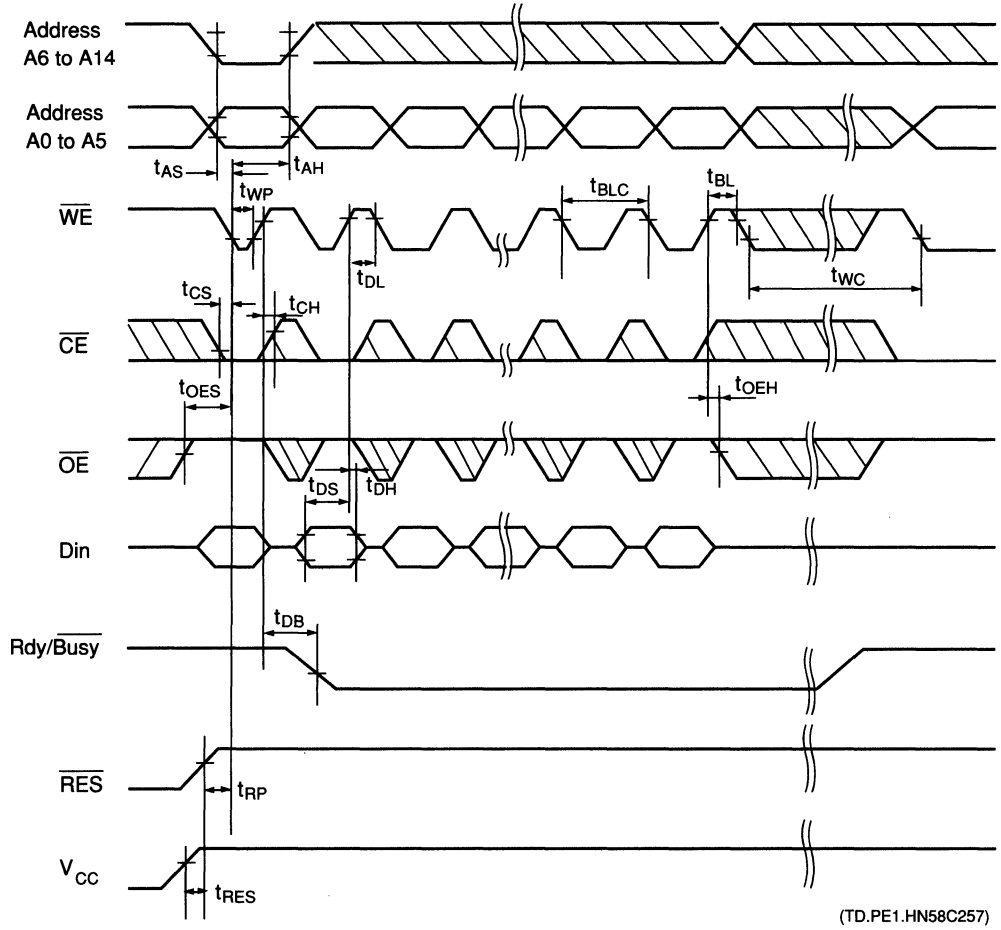
5

■ AC ELECTRICAL CHARACTERISTICS FOR PAGE ERASE AND PAGE WRITE OPERATIONS

Item	Symbol	Min.[1]	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	0	-	-	ns	
Write Enable to Write Setup Time	t_{WS}[3]	0	-	-	ns	
Chip Enable to Write Setup Time	t_{CS}[2]	0	-	-	ns	
Write Pulse Width	t_{WP}[2]	250	-	-	ns	
	t_{CW}[3]	250	-	-	ns	
Address Hold Time	t_{AH}	200	-	-	ns	
Data Setup Time	t_{DS}	150	-	-	ns	
Data Hold Time	t_{DH}	0	-	-	ns	
Write Enable Hold Time	t_{WH}[3]	0	-	-	ns	
Chip Enable Hold Time	t_{CH}[2]	0	-	-	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Output Enable Hold Time	t_{OEH}	0	-	-	ns	
Data Latch Time	t_{DL}	300	-	-	ns	
Write Cycle Time	t_{WC}	15	-	-	ms	
Byte Load Window	t_{BL}	100	-	-	µs	
Byte Load Cycle	t_{BLC}	0.55	-	30	µs	
Time to Device Busy	t_{DB}	120	-	-	ns	
$\overline{RES}$ to Write Setup Time	t_{RP}	100	-	-	µs	
V_{CC} to $\overline{RES}$ Setup Time	t_{RES}	1	-	-	µs	

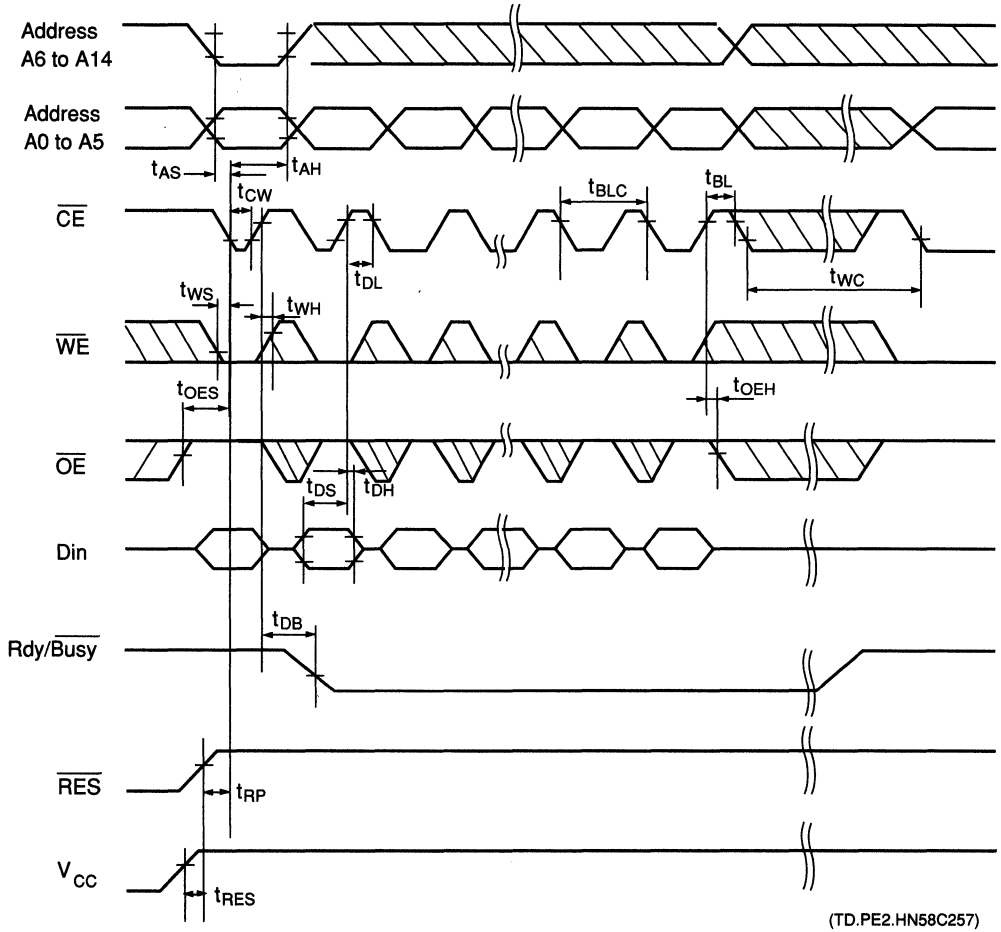
Notes: 1. Use this device in longer cycle than this value.
2. $\overline{WE}$ controlled operation.
3. $\overline{CE}$ controlled operation.

■ PAGE ERASE AND PAGE WRITE TIMING WAVEFORM ($\overline{WE}$ Controlled)



5

■ PAGE ERASE AND PAGE WRITE TIMING WAVEFORM ($\overline{CE}$ Controlled)

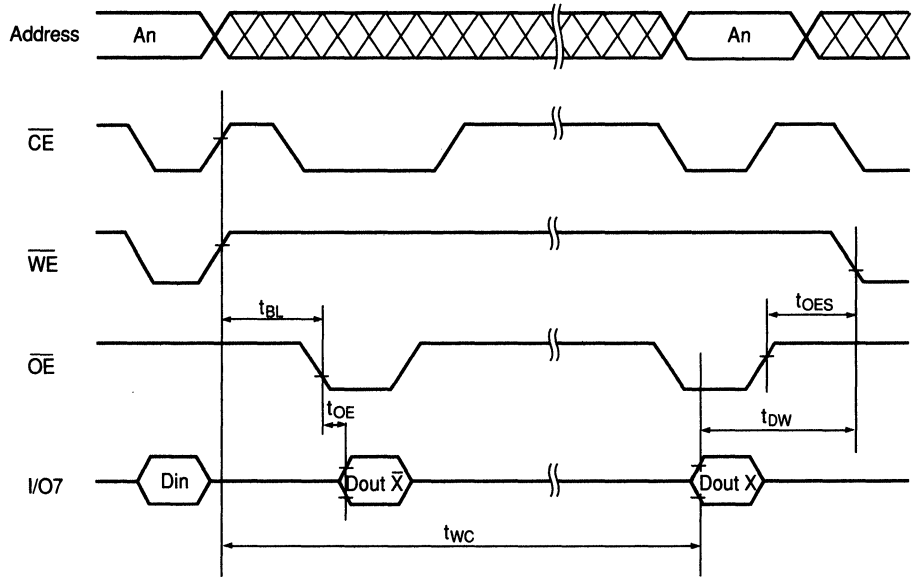


(TD.PE2.HN58C257)

■ AC ELECTRICAL CHARACTERISTICS FOR $\overline{DATA}$ POLLING OPERATION

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Byte Load Window	t_{BL}	100	-	-	µs	
Output Enable to Output Delay	t_{OE}	10	-	150	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Write Start Time	t_{DW}	150	-	-	ns	
Write Cycle Time	t_{WC}	-	-	15	ms	

■ $\overline{DATA}$ POLLING TIMING WAVEFORM



(TD.DP.EE)

5

■ FUNCTIONAL DESCRIPTION

Automatic Page Write

The Page Write feature allows 1 to 64 Bytes of data to be written into the EEPROM in a single write cycle. Following the initial Byte cycle, an additional 1 to 63 Bytes can be written in the same manner. Each additional Byte load cycle must be started within 30 µs from the preceding falling edge of $\overline{WE}$ or $\overline{CE}$. Data can be written and accessed 10^5 times in 64 Byte units.

$\overline{Data}$ Polling

$\overline{Data}$ Polling allows the status of the EEPROM to be determined. If the EEPROM is set to Read mode during a Write cycle, an inversion of the last Byte of data to be loaded outputs from I/O_7 to indicate that the EEPROM is performing a Write operation.

Ready/$\overline{Busy}$ Signal

The Ready/$\overline{Busy}$ signal also allows the status of the EEPROM to be determined. The Ready/$\overline{Busy}$ signal is high impedence except in the write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, the Ready/$\overline{Busy}$ signal changes to high impedence.

$\overline{WE}$ and $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

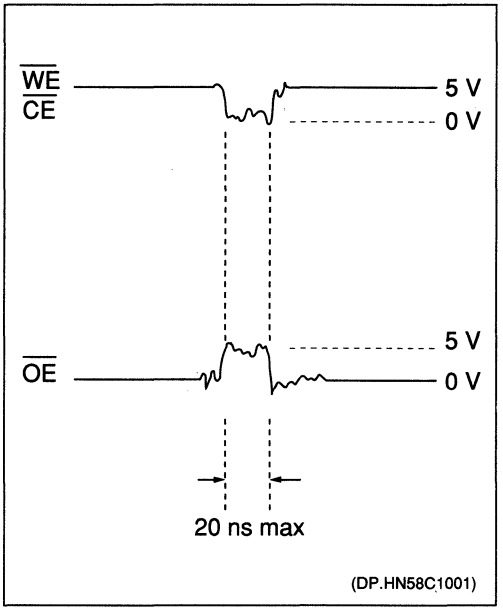
Write/Erase Endurance and Data Retention

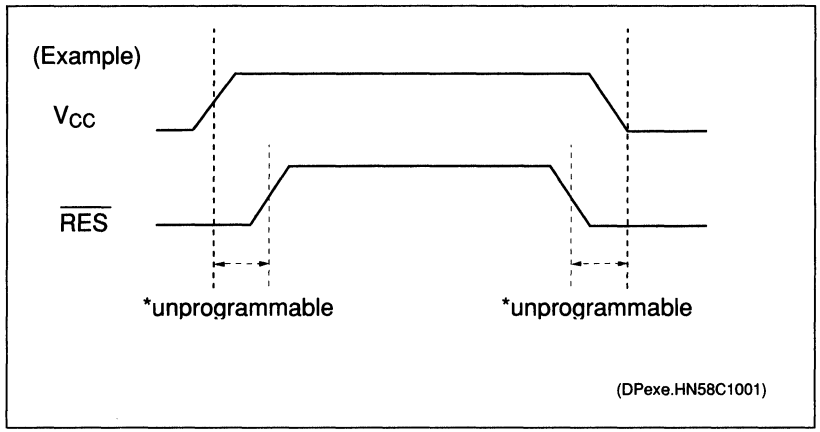
The endurance with page programming is 10^5 cycles (1% cumulative failure rate) and the data retention time is more than 10 years when a device is programmed less than 10^4 cycles.

Data Protection

To protect the data during operation and power on/off, the HN58V257 has:

1. Data protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation.
   During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. To prevent this phenomenon, the HN58V257 has a noise cancellation function that cuts noise if its width is 20 ns or less in programming mode. Be careful not to allow noise of a width of more than 20 ns on the control pins.





■ **FUNCTIONAL DESCRIPTION (continued)**

Data Protection (continued)

2. Data protection at V_{CC} on/off
   When $\overline{RES}$ is low, the EEPROM cannot be erased and programmed. Therefore, data can be protected by keeping $\overline{RES}$ low when V_{CC} is switched. $\overline{RES}$ should be high during programming because it does not provide a latch function.
   When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may turn the EEPROM to programming mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable, standby or readout state by using a CPU reset signal to $\overline{RES}$ pin.
   In addition, when $\overline{RES}$ is kept high at V_{CC} on/off timing, the input level of control pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) must be held as $\overline{CE}$=V_{CC} or $\overline{OE}$=Low or $\overline{WE}$=V_{CC} level.

5

1M (128K x 8-bit) EEPROM

■ DESCRIPTION

The Hitachi HN58C1001 is a 1-Megabit CMOS Electrically Erasable Programmable Read Only Memory (EEPROM) organized as 131,072 x 8-bits. The HN58C1001 is capable of in-system electrical Byte and Page reprogrammability.

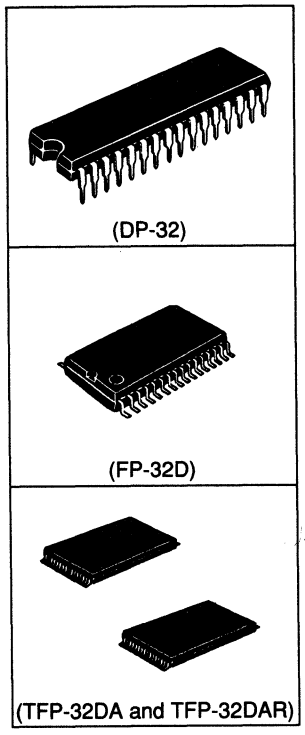
The HN58C1001 achieves high speed access, low power consumption, and a high level of reliability by employing advanced MNOS memory technology and CMOS process and circuitry technology.

The HN58C1001 has a 128-Byte Page Programming function to make its erase and write operations faster. The HN58C1001 features $\overline{\text{Data}}$ Polling and a Ready/$\overline{\text{Busy}}$ signal to indicate completion of erase and programming operations.

The HN58C1001 provides several levels of data protection. Hardware data protection is provided with the $\overline{\text{RES}}$ pin, in addition to noise protection on the $\overline{\text{WE}}$ signal and write inhibit on power on and off. Software data protection is implemented using the JEDEC Optional Standard algorithm.

The HN58C1001 is designed for high reliability in the most demanding applications. Data retention is specified for 10 years and erase/write endurance is guaranteed to a minimum of 100,000 cycles in the Page Mode.

The HN58C1001 is offered in 32-pin Plastic DIP and 32-lead Plastic SOP and TSOP packages. The HN58C1001 TSOP is offered in both standard and reverse bend pinouts.



■ FEATURES

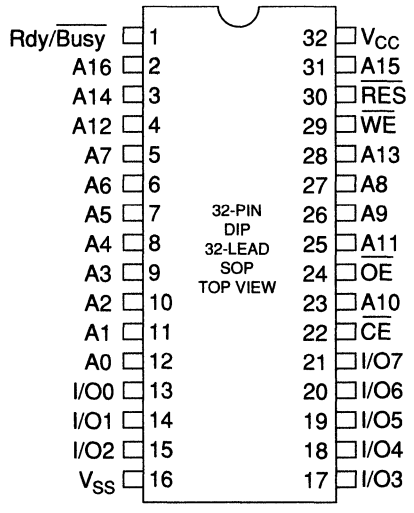
- Single Power Supply:
  V_{CC} = 5V ± 10%
- High Speed Access Times:
  150 ns (max)
- Low Power Dissipation:
  Active Current: 20 mW/MHz (typ)
  Standby Current: 100 µW (max)
- Automatic Programming:
  Automatic Page Write: 10 ms (max)
  128 Byte Page Size
  Automatic Byte Write: 10 ms (max)
- $\overline{\text{Data}}$ Polling and Ready/$\overline{\text{Busy}}$ Signals
- Hardware Data Protection with $\overline{\text{RES}}$ pin
- Data Protection Circuitry on Power On/Off
- Software Data Protection Algorithm
- Data Retention: 10 years
- Erase/Write Endurance:
  100,000 cycles in Page Mode
- Packages:
  32-pin Plastic DIP
  32-pin Plastic SOP
  32-lead Plastic TSOP (Type I)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN58C1001P-15	150 ns	32-pin Plastic DIP (DP-32)
HN58C1001FP-15	150 ns	32-lead Plastic SOP (FP-32D)
HN58C1001T-15	150 ns	32-lead Plastic TSOP (TFP-32DA)
HN58C1001R-15	150 ns	32-lead Plastic TSOP (TFP-32DAR) Reverse bend

■ PIN ARRANGEMENT

HN58C1001P Series
HN58C1001FP Series



(PinD32.HN58C1001)

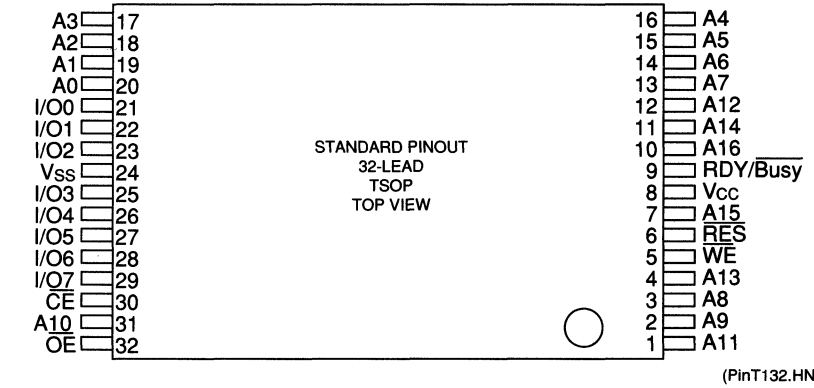
■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{16}	Address
I/O_0 - I/O_7	Input/Output
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground
Rdy/$\overline{Busy}$	Ready/Busy
$\overline{RES}$	Reset

5

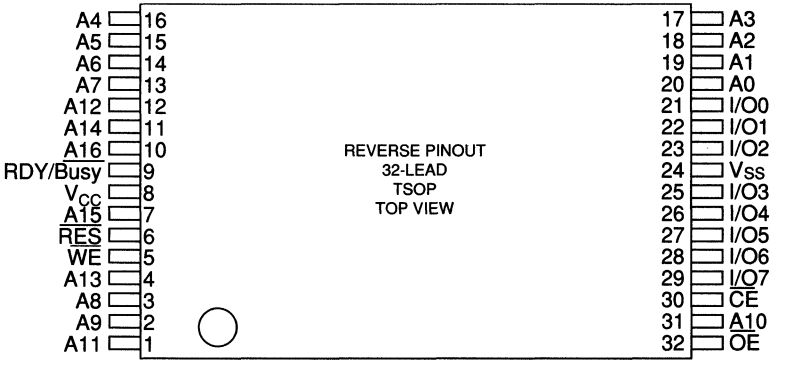
■ PIN ARRANGEMENT (cont.)

HN58C1001T Series



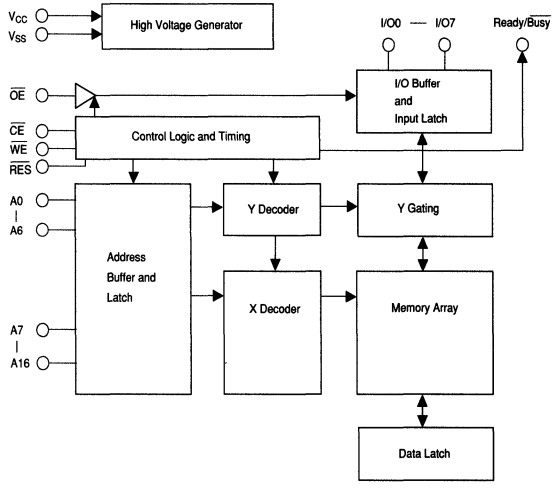
(PinT132.HN58C1001T)

HN58C1001R Series



(PinT132.HN58C1001R)

■ BLOCK DIAGRAM



(BD.HN58C1001)

■ MODE SELECTION

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RES}$	RDY/$\overline{Busy}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_H	High-Z	D_{OUT}
Standby	V_{IH}	X	X	X	High-Z	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	V_H	High-Z→V_{OL}	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	V_H	High-Z	High-Z
Write Inhibit	X	X	V_{IH}	X	-	-
	X	V_{IL}	X	X	-	-
$\overline{Data}$ Polling	V_{IL}	V_{IL}	V_{IH}	V_H	V_{OL}	Data Out (I/O_7)
Program	X	X	X	V_{IL}	High-Z	High-Z

Note: 1. X = Don't Care

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Input Voltage [1]	V_{IN}	-0.5[2] to +7.0	V
Operating Temperature Range [3]	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C

Notes: 1. Relative to V_{SS}.
2. V_{IN} min = -3.0V for pulse width ≤ 50 ns.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	-	-	6	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	-	-	12	pF	V_{OUT} = 0V

5

■ DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{CC} = 5.5 V, V_{IN} = 5.5 V
Output Leakage Current	I_{LO}	-	-	2	µA	V_{CC} = 5.5 V, V_{OUT} = 5.5 V/0.4 V
Standby V_{CC} Current	I_{CC1}	-	-	20	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	-	-	1	mA	$\overline{CE}$ = V_{IH}
Operating V_{CC} Current	I_{CC3}	-	-	15	mA	I_{OUT} = 0 mA, Duty = 100%, Cycle = 1 µs
		-	-	40	mA	I_{OUT} = 0 mA, Duty = 100%, Cycle = 200 ns
Input Voltage	V_{IL}	-0.3 [1]	-	0.8	V	
	V_{IH}	2.2	-	V_{CC} + 1	V	
	V_H	V_{CC}-1.0	-	V_{CC} + 1	V	
Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA

Notes: 1. V_{IL} min = -1.0 V for pulse width ≤ 50 ns.
2. I_{LI} on $\overline{RES}$ = 100 µA Max.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(T_a = 0 to 70°C, V_{CC} = 5V ± 10%)

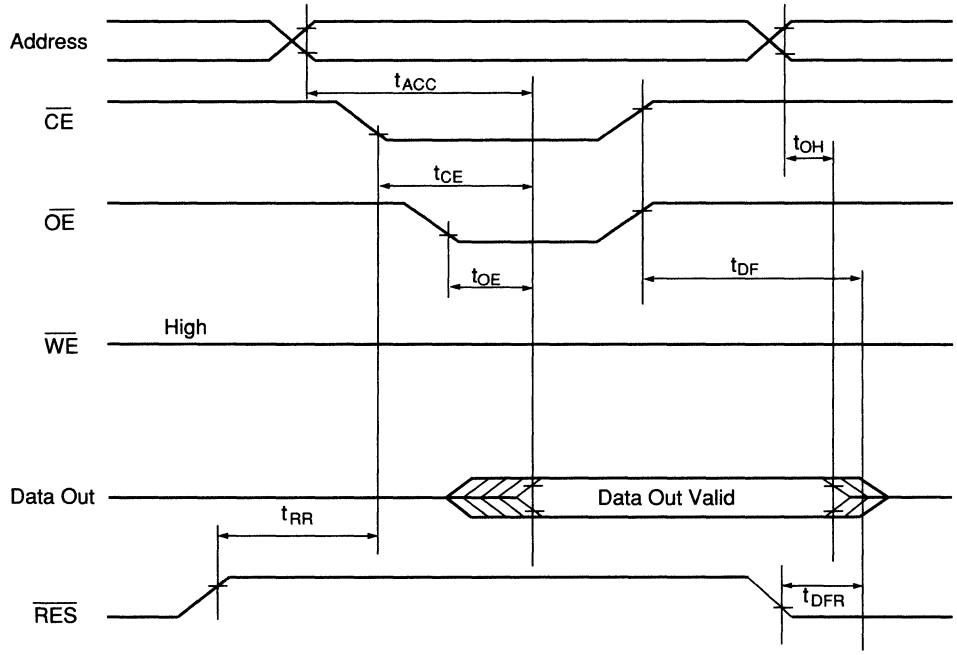
Test Conditions

- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall times: ≤ 20 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V, 1.8 V

Item	Symbol	HN58C1001-15 Min.	HN58C1001-15 Max.	Unit	Test Condition
Address Access Time	t_{ACC}	-	150	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Chip Enable Access Time	t_{CE}	-	150	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Enable Access Time	t_{OE}	10	75	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Hold to Address Change	t_{OH}	0	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Disable to High-Z[1]	t_{DF}	0	50	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
	t_{DFR}	0	350	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ to Output Delay	t_{RR}	0	450	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



(TD.R.HN58C1001)

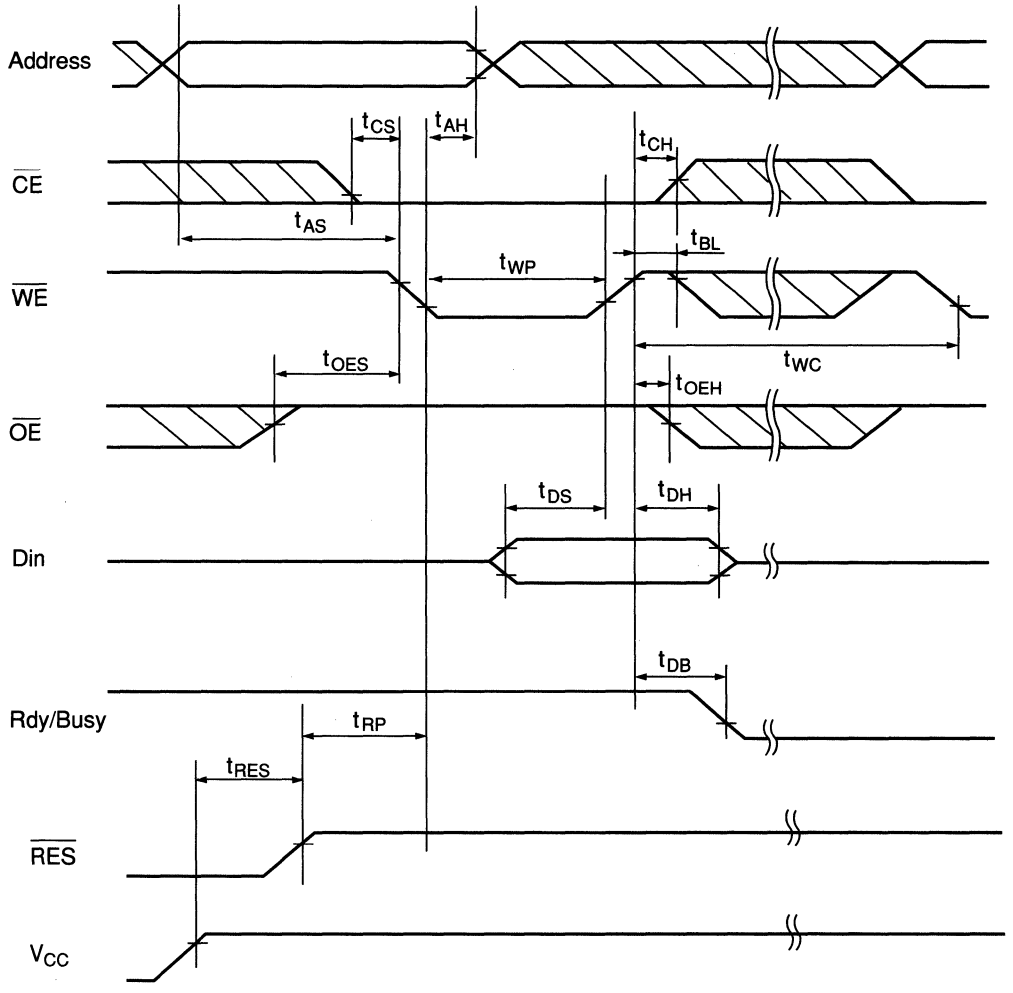
■ AC ELECTRICAL CHARACTERISTICS FOR BYTE ERASE AND BYTE WRITE OPERATIONS

Item	Symbol	Min.[1]	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	0	-	-	ns	
Chip Enable to Write Setup Time	t_{CS}[2]	0	-	-	ns	
Write Pulse Width	t_{CW}[3]	250	-	-	ns	
	t_{WP}[2]	250	-	-	ns	
Address Hold Time	t_{AH}	150	-	-	ns	
Data Setup Time	t_{DS}	100	-	-	ns	
Data Hold Time	t_{DH}	10	-	-	ns	
Chip Enable Hold Time	t_{CH}[2]	0	-	-	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Output Enable Hold Time	t_{OEH}	0	-	-	ns	
Write Cycle Time	t_{WC}	10	-	-	ms	
Byte Load Window	t_{BL}	100	-	-	µs	
Time to Device Busy	t_{DB}	120	-	-	ns	
$\overline{RES}$ to Write Setup Time	t_{RP}	100	-	-	µs	
V_{CC} to $\overline{RES}$ Setup Time	t_{RES}	1	-	-	µs	

Note: 1. Use this device in a longer cycle than this value.
2. WE controlled operation.
3. CE controlled operation.

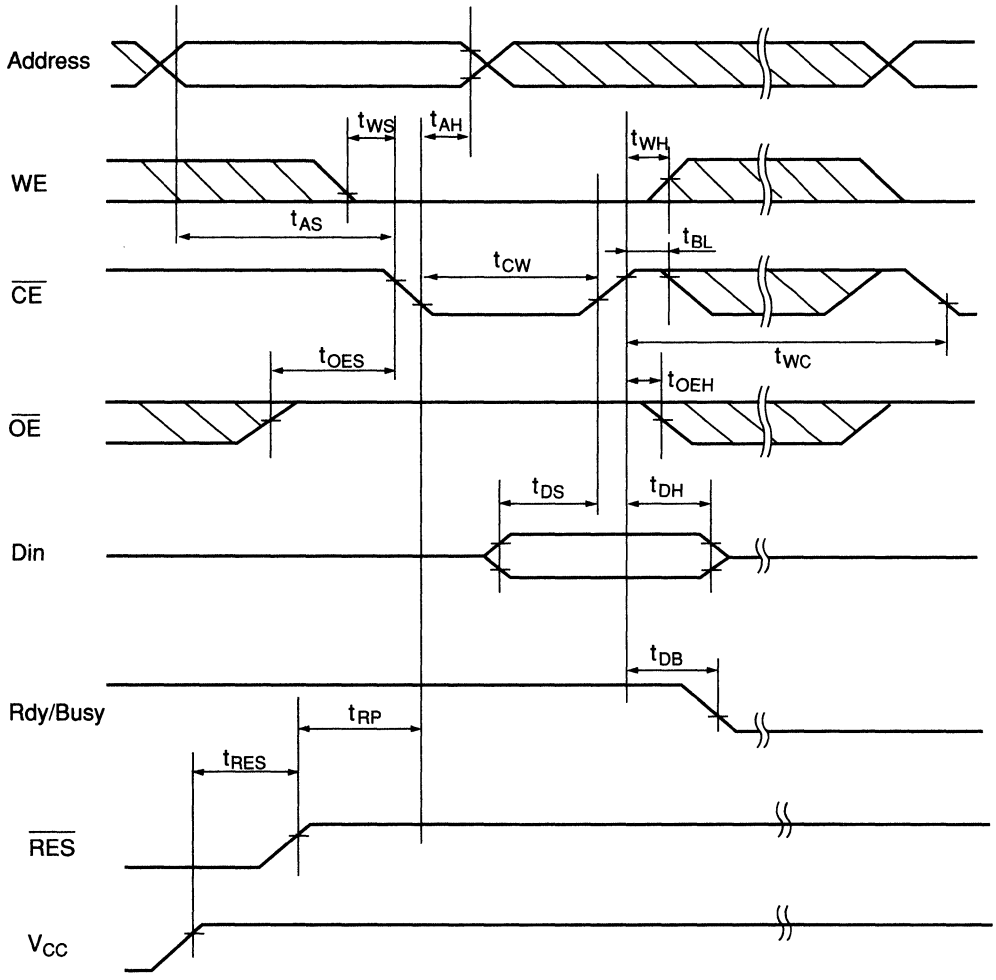
5

■ BYTE ERASE AND BYTE WRITE TIMING WAVEFORM ($\overline{WE}$ Controlled)



(TD.BE1.HN58C1001)

■ BYTE ERASE AND BYTE WRITE TIMING WAVEFORM ($\overline{CE}$ Controlled)



(TD.BE2.HN58C1001)

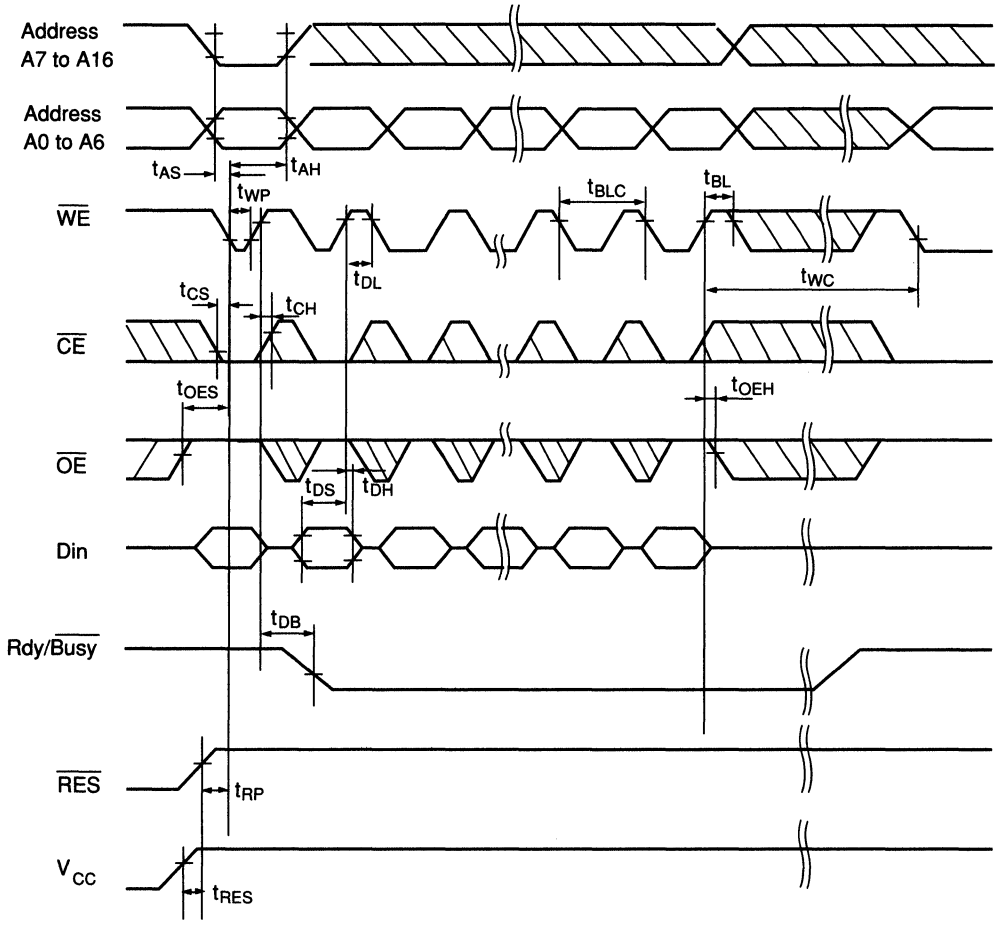
5

■ AC ELECTRICAL CHARACTERISTICS FOR PAGE ERASE AND PAGE WRITE OPERATIONS

Item	Symbol	Min.[1]	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	0	-	-	ns	
Write Enable to Write Setup Time	t_{WS}[3]	0	-	-	ns	
Chip Enable to Write Setup Time	t_{CS}[2]	0	-	-	ns	
Write Pulse Width	t_{WP}[2]	250	-	-	ns	
	t_{CW}[3]	250	-	-	ns	
Address Hold Time	t_{AH}	150	-	-	ns	
Data Setup Time	t_{DS}	100	-	-	ns	
Data Hold Time	t_{DH}	10	-	-	ns	
Write Enable Hold Time	t_{WH}[3]	0	-	-	ns	
Chip Enable Hold Time	t_{CH}[2]	0	-	-	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Output Enable Hold Time	t_{OEH}	0	-	-	ns	
Data Latch Time	t_{DL}	200	-	-	ns	
Write Cycle Time	t_{WC}	10	-	-	ms	
Byte Load Window	t_{BL}	100	-	-	µs	
Byte Load Cycle	t_{BLC}	0.55	-	30	µs	
Time to Device Busy	t_{DB}	120	-	-	ns	
$\overline{RES}$ to Write Setup Time	t_{RP}	100	-	-	µs	
V_{CC} to $\overline{RES}$ Setup Time	t_{RES}	1	-	-	µs	

Notes: 1. Use this device in longer cycle than this value.
2. $\overline{WE}$ controlled operation.
3. $\overline{CE}$ controlled operation.

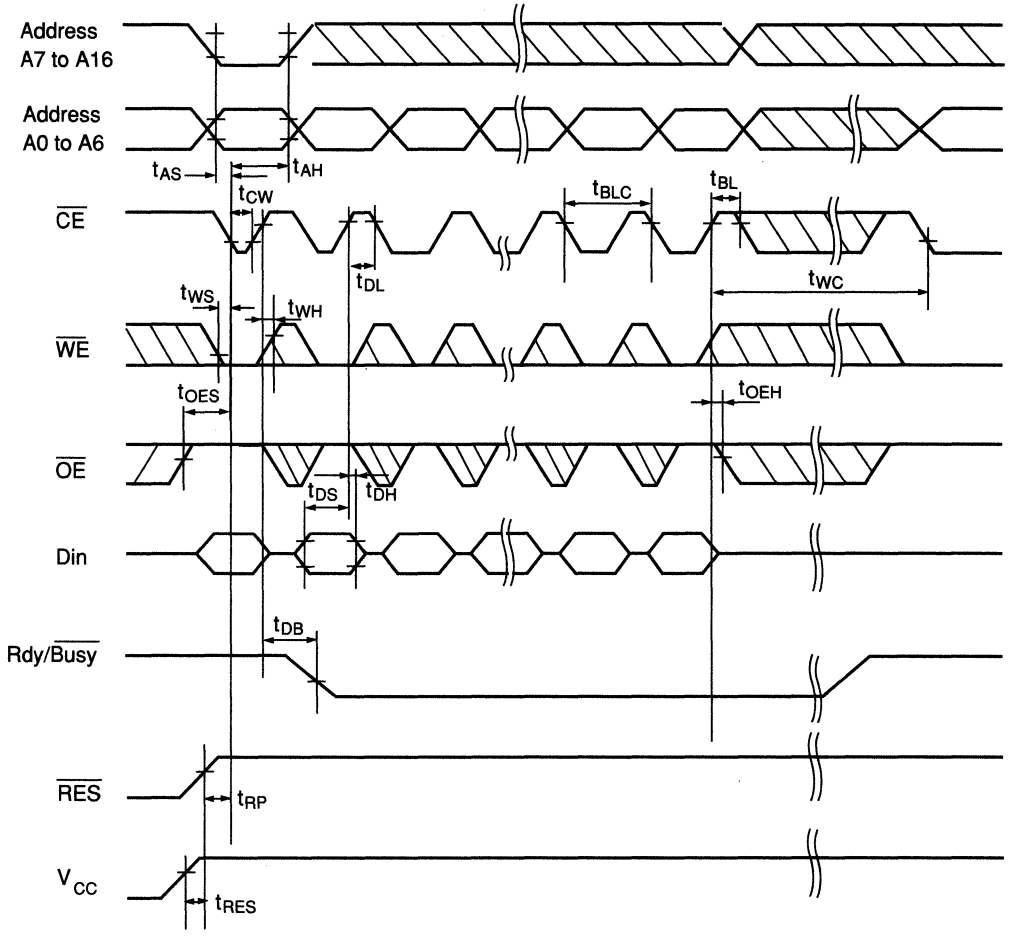
■ PAGE ERASE AND PAGE WRITE TIMING WAVEFORM ($\overline{WE}$ Controlled)



(TD.PE1.HN58C1001)

5

■ PAGE ERASE AND PAGE WRITE TIMING WAVEFORM ($\overline{CE}$ Controlled)

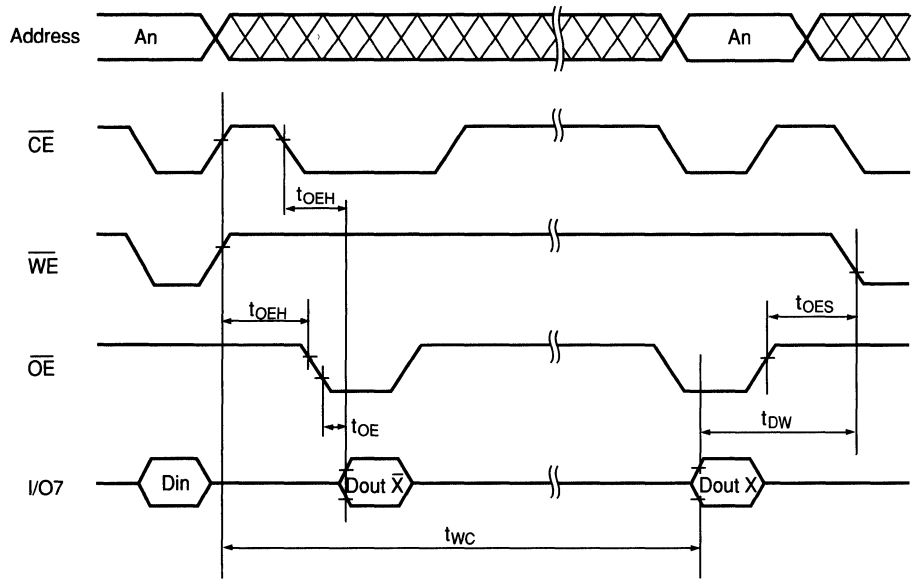


(TD.PE2.HN58C1001)

■ AC ELECTRICAL CHARACTERISTICS FOR $\overline{DATA}$ POLLING OPERATION

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Output Enable Hold Time	t_{OEH}	0	-	-	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Write Start Time	t_{DW}	150	-	-	ns	
Write Cycle Time	t_{WC}	-	-	10	ms	

■ $\overline{DATA}$ POLLING TIMING WAVEFORM



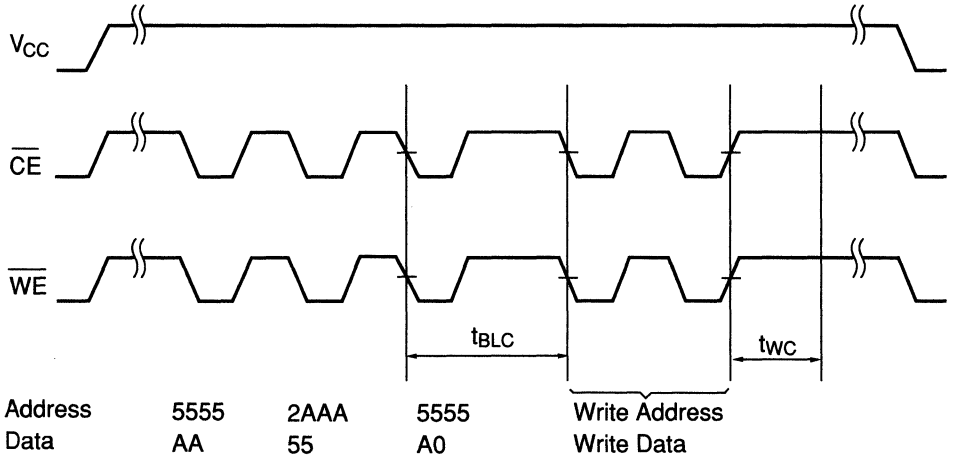
(TD.DP.HN58C1001)

5

■ AC ELECTRICAL CHARACTERISTICS FOR SOFTWARE DATA PROTECTION CYCLE OPERATION

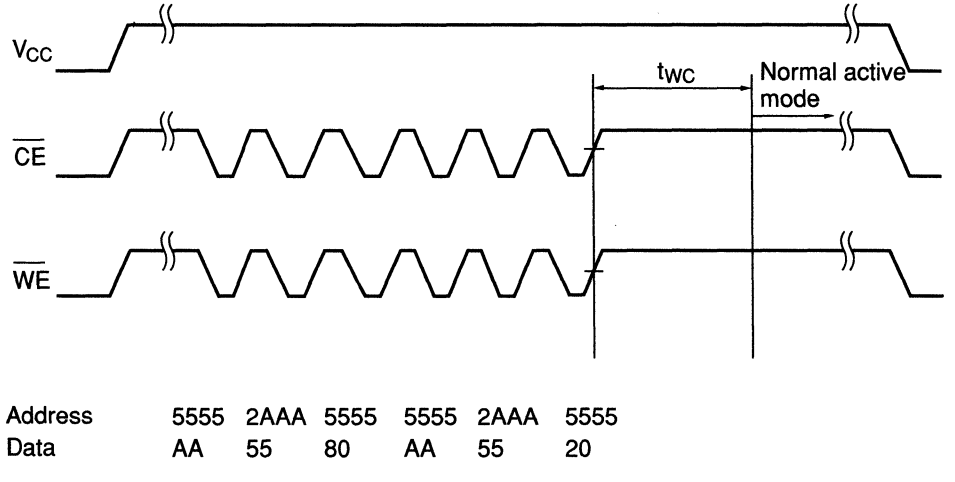
Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Byte Load Cycle Time	t_{BLC}	0.55	-	30	µs	
Write Cycle Time	t_{WC}	10	-	-	ms	

■ SOFTWARE DATA PROTECTION TIMING WAVEFORM (Protection Mode)



(TD.SD1.HN58C1001)

■ SOFTWARE DATA PROTECTION TIMING WAVEFORM (Non-Protection Mode)



(TD.SD2.HN58C1001)

■ FUNCTIONAL DESCRIPTION

Automatic Page Write

The Page Write feature allows 1 to 128 Bytes of data to be written into the EEPROM in a single cycle and allows the undefined data within 128 Bytes to be written corresponding to the undefined address (A_0 to A_6). Loading the first Byte of data, the data load window of 30 µs opens for the second. In the same manner each additional Byte of data can be loaded within 30 µs. In case $\overline{CE}$ and $\overline{WE}$ are kept high for 100 µs after data input, the EEPROM enters erase and write automatically and only the input data are written into the EEPROM. In Page mode the data can be written and accessed 10^5 times per page, and in Byte mode 10^4 times per Byte.

$\overline{\text{Data}}$ Polling

$\overline{\text{Data}}$ Polling allows the status of the EEPROM to be determined. If the EEPROM is set to Read mode during a Write cycle, an inversion of the last Byte of data to be loaded outputs from I/O_7 to indicate that the EEPROM is performing a Write operation.

Write Protection

(1) Noise protection: Noise on a write cycle will not act as a trigger with a $\overline{WE}$ pulse of less than 20 ns.
(2) Write inhibit: Holding $\overline{OE}$ low, $\overline{WE}$ high, or $\overline{CE}$ high, inhibits a write cycle during power on/off.

$\overline{WE}$ and $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

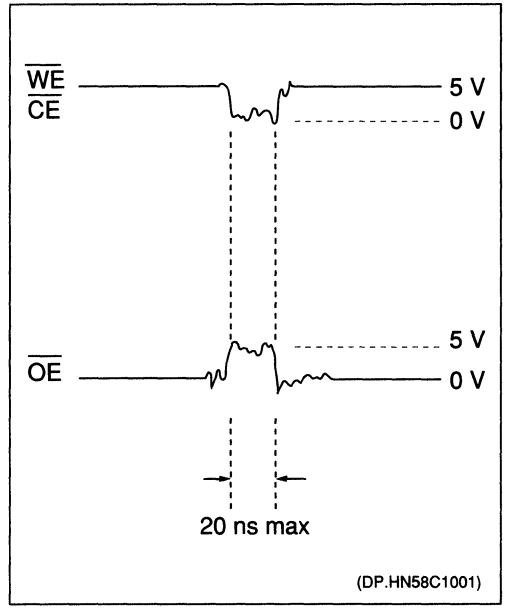
Write/Erase Endurance and Data Retention

The endurance with page programming is 10^5 cycles (1% cumulative failure rate) and the data retention time is more than 10 years when a device is programmed less than 10^4 cycles.

Data Protection

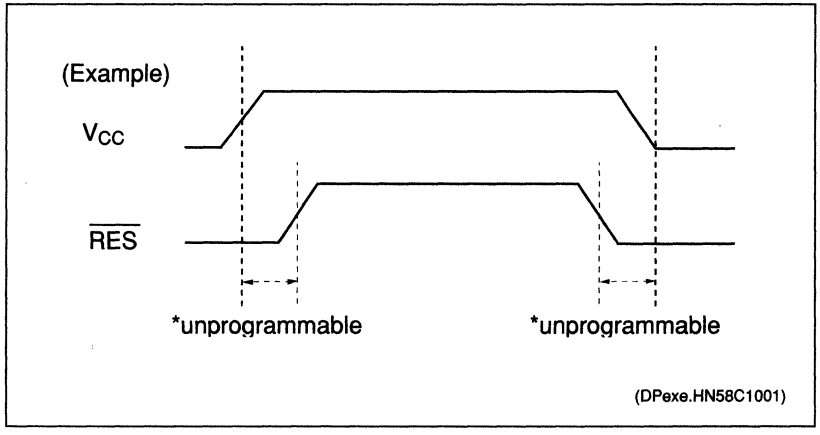
To protect the data during operation and power on/off, the HN58C1001 has:

1. Data protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation.
   During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. To prevent this phenomenon, the HN58C1001 has a noise cancellation function that cuts noise if its width is 20 ns or less in programming mode. Be careful not to allow noise of a width of more than 20 ns on the control pins.



(DP.HN58C1001)

5



■ FUNCTIONAL DESCRIPTION (continued)

Data Protection (continued)

2. Data protection at V_{CC} on/off
   When $\overline{RES}$ is low, the EEPROM cannot be erased and programmed. Therefore, data can be protected by keeping $\overline{RES}$ low when V_{CC} is switched. $\overline{RES}$ should be high during programming because it does not provide a latch function.
   When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may turn the EEPROM to programming mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable, standby or readout state by using a CPU reset signal to $\overline{RES}$ pin.
   In addition, when $\overline{RES}$ is kept high at V_{CC} on/off timing, the input level of control pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) must be held as $\overline{CE}$=V_{CC} or $\overline{OE}$=Low or $\overline{WE}$=V_{CC} level.

3. Software data protection
   To prevent unintentional programming caused by noise generated by external circuits, HN58C1001 has a Software data protection function. In Software data protection mode, 3 Bytes of data must be input before the Write data. These Bytes can switch the Non-Protection mode to the Protection mode.

Address	Data
5555	AA
⇓	⇓
2AAA	55
⇓	⇓
5555	A0
⇓	⇓
Write Address	**Write Data**

(Normal Data Input)

The Software data protection mode can be cancelled by inputting the following 6 Bytes. This changes the HN58C1001 turns to the Non-Protection mode and it can write data normally. When the data is input during the cancelling cycle, the data cannot be written.

Address	Data
5555	AA
⇓	⇓
2AAA	55
⇓	⇓
5555	80
⇓	⇓
5555	AA
⇓	⇓
2AAA	55
⇓	⇓
5555	20

1M (128K x 8-bit) EEPROM

■ DESCRIPTION

The Hitachi HN58V1001 is a 1-Megabit CMOS Electrically Erasable Programmable Read Only Memory (EEPROM) organized as 131,072 x 8-bits. The HN58V1001 is capable of in-system electrical Byte and Page reprogrammability.

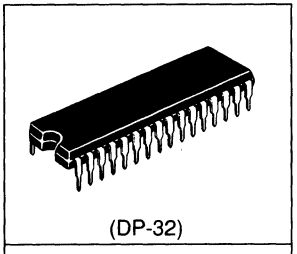
The HN58V1001 achieves low voltage, low power consumption, and a high level of reliability by employing advanced MNOS memory technology and CMOS process and circuitry technology.

The HN58V1001 has a 128-Byte Page Programming function to make its erase and write operations faster. The HN58V1001 features Data Polling and a Ready/Busy signal to indicate completion of erase and programming operations.

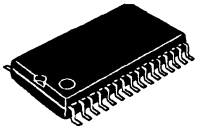
The HN58V1001 provides several levels of data protection. Hardware data protection is provided with the RES pin, in addition to noise protection on the WE signal and write inhibit on power on and off. Software data protection is implemented using the JEDEC Optional Standard algorithm.

The HN58V1001 is designed for high reliability in the most demanding applications. Data retention is specified for 10 years and erase/write endurance is guaranteed to a minimum of 100,000 cycles in the Page Mode.

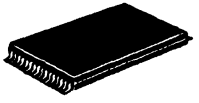
The HN58V1001 is offered in 32-pin Plastic DIP and 32-lead Plastic SOP and TSOP packages. The HN58V1001 TSOP is offered in both standard and reverse bend pinouts.



(DP-32)



(FP-32D)



(TFP-32DA and TFP-32DAR)

■ FEATURES

- Single Power Supply:
  V_{CC} = 2.7 to 5.5V
- Address Access Time:
  250 ns (max)
- Low Power Dissipation:
  Active Current: 20 mW/MHz (typ)
  Standby Current: 100 µW (max)
- Automatic Programming:
  Automatic Page Write: 15 ms (max)
  128 Byte Page Size
  Automatic Byte Write: 15 ms (max)
- Data Polling and Ready/Busy Signals
- Hardware Data Protection with RES pin
- Data Protection Circuitry on Power On/Off
- Software Data Protection Algorithm
- Data Retention: 10 years
- Erase/Write Endurance:
  100,000 cycles in Page Mode
- Packages:
  32-pin Plastic DIP
  32-pin Plastic SOP
  32-lead Plastic TSOP (Type I)

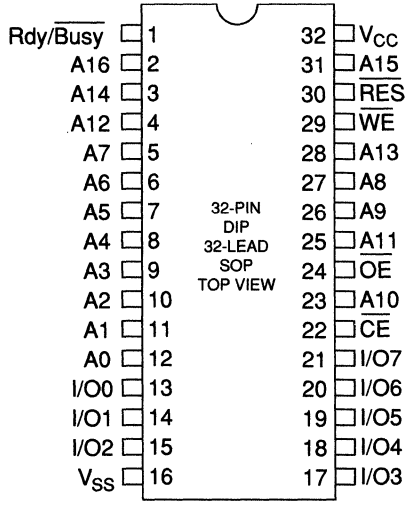
5

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN58V1001P-25	250 ns	32-pin Plastic DIP (DP-32)
HN58V1001FP-25	250 ns	32-lead Plastic SOP (FP-32D)
HN58V1001T-25	250 ns	32-lead Plastic TSOP (TFP-32DA)
HN58V1001R-25	250 ns	32-lead Plastic TSOP (TFP-32DAR) Reverse bend

■ PIN ARRANGEMENT

HN58V1001P Series
HN58V1001FP Series



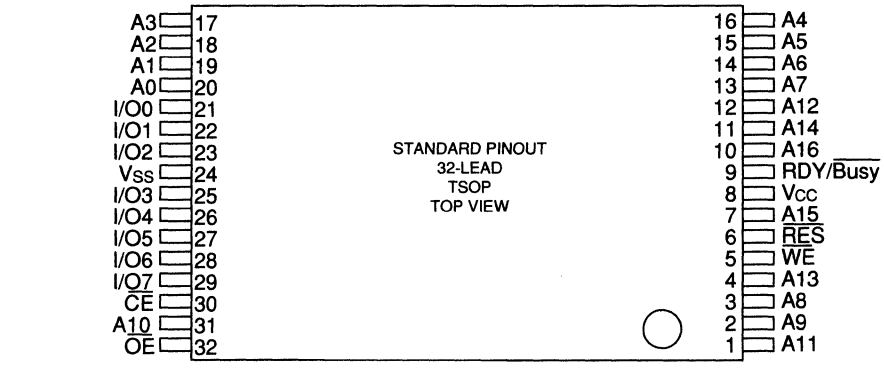
(PinD32.HN58C1001)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{16}	Address
I/O_0 - I/O_7	Input/Output
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground
Rdy/$\overline{Busy}$	Ready/Busy
$\overline{RES}$	Reset

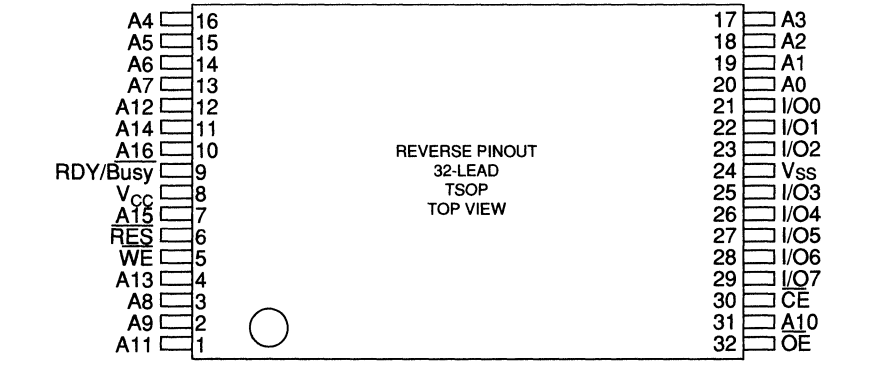
■ PIN ARRANGEMENT (cont.)

HN58V1001T Series



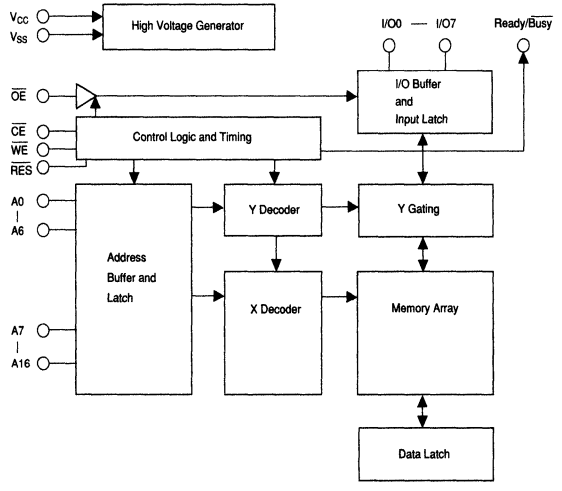
(PinT132.HN58C1001T)

HN58V1001R Series



(PinT132.HN58C1001R)

■ BLOCK DIAGRAM



(BD.HN58C1001)

5

■ MODE SELECTION

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RES}$	RDY/$\overline{Busy}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_H	High-Z	D_{OUT}
Standby	V_{IH}	X	X	X	High-Z	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	V_H	High-Z→V_{OL}	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	V_H	High-Z	High-Z
Write Inhibit	X	X	V_{IH}	X	-	-
	X	V_{IL}	X	X	-	
$\overline{Data}$ Polling	V_{IL}	V_{IL}	V_{IH}	V_H	V_{OL}	Data Out (I/O_7)
Program	X	X	X	V_{IL}	High-Z	High-Z

Note: 1. X = Don't Care

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Input Voltage [1]	V_{IN}	-0.5[2] to +7.0	V
Operating Temperature Range [3]	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C

Notes: 1. Relative to V_{SS}.
2. V_{IN} min = -3.0V for pulse width ≤ 50 ns.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	-	-	6	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	-	-	12	pF	V_{OUT} = 0V

■ DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7 to 5.5V, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{CC} = 3.6 V, V_{IN} = 3.6 V
Output Leakage Current	I_{LO}	-	-	2	µA	V_{CC} = 3.6 V, V_{OUT} = 3.6 V/0.4 V
Standby V_{CC} Current	I_{CC1}	-	-	20	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	-	-	1	mA	$\overline{CE}$ = V_{IH}
Operating V_{CC} Current	I_{CC3}	-	-	6	mA	I_{OUT} = 0 mA, Duty = 100%, Cycle = 1 µs at V_{CC} = 3.3 V
		-	-	15	mA	I_{OUT} = 0 mA, Duty = 100%, Cycle = 250 ns at V_{CC} = 3.3 V
Input Voltage	V_{IL}	-0.3 [1]	-	0.8	V	
	V_{IH}	2.0 [2]	-	V_{CC}+0.3	V	
	V_H	V_{CC}-0.5	-	V_{CC}+1	V	
Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2.1 mA
	V_{OH}	V_{CC}x0.8	-	-	V	I_{OH} = -400 µA

Notes: 1. V_{IL} min = -1.0 V for pulse width ≤ 50 ns.
2. V_{IH} min = 2.2 V for V_{CC} = 3.6 to 5.5V.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(T_a = 0 to 70°C, V_{CC} = 2.7 to 5.5V)

Test Conditions

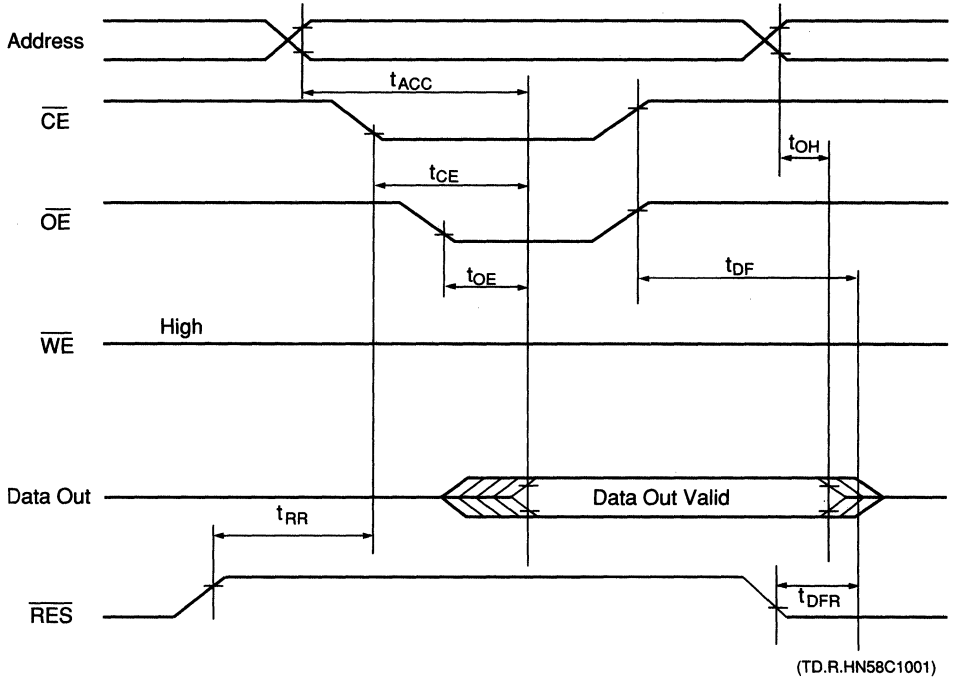
- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall times: ≤ 20 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V, 1.8 V

Item	Symbol	HN58V1001-25 Min.	HN58V1001-25 Max.	Unit	Test Condition
Address Access Time	t_{ACC}	-	250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Chip Enable Access Time	t_{CE}	-	250	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Enable Access Time	t_{OE}	10	120	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Hold to Address Change	t_{OH}	0	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Disable to High-Z[1]	t_{DF}	0	50	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
	t_{DFR}	0	350	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ to Output Delay	t_{RR}	0	600	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

5

■ READ TIMING WAVEFORM



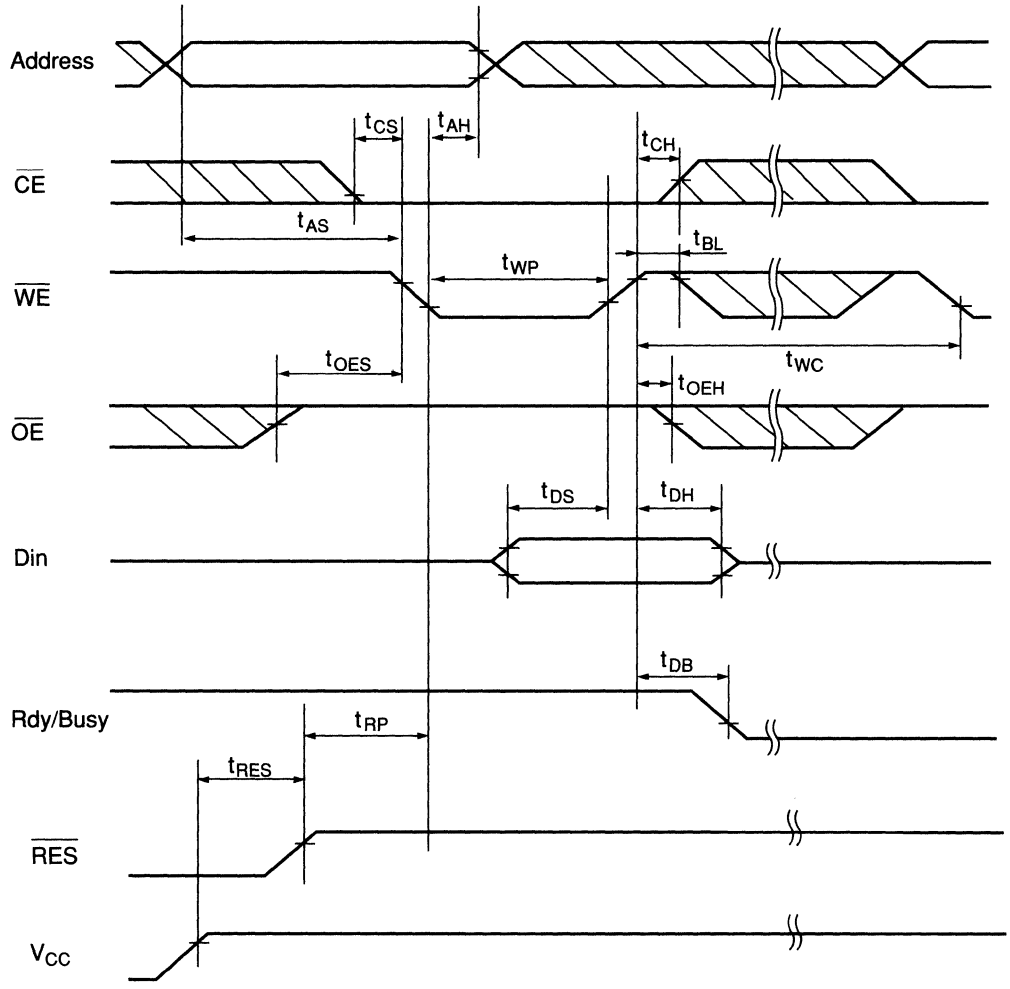
(TD.R.HN58C1001)

■ AC ELECTRICAL CHARACTERISTICS FOR BYTE ERASE AND BYTE WRITE OPERATIONS

Item	Symbol	Min.[1]	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	0	-	-	ns	
Chip Enable to Write Setup Time	t_{CS}[2]	0	-	-	ns	
Write Pulse Width	t_{CW}[3]	250	-	-	ns	
	t_{WP}[2]	250	-	-	ns	
Address Hold Time	t_{AH}	150	-	-	ns	
Data Setup Time	t_{DS}	100	-	-	ns	
Data Hold Time	t_{DH}	10	-	-	ns	
Chip Enable Hold Time	t_{CH}[2]	0	-	-	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Output Enable Hold Time	t_{OEH}	0	-	-	ns	
Write Cycle Time	t_{WC}	10	-	-	ms	
Byte Load Window	t_{BL}	100	-	-	µs	
Time to Device Busy	t_{DB}	120	-	-	ns	
$\overline{RES}$ to Write Setup Time	t_{RP}	100	-	-	µs	
V_{CC} to $\overline{RES}$ Setup Time	t_{RES}	1	-	-	µs	

Note: 1. Use this device in a longer cycle than this value.
2. WE controlled operation.
3. CE controlled operation.

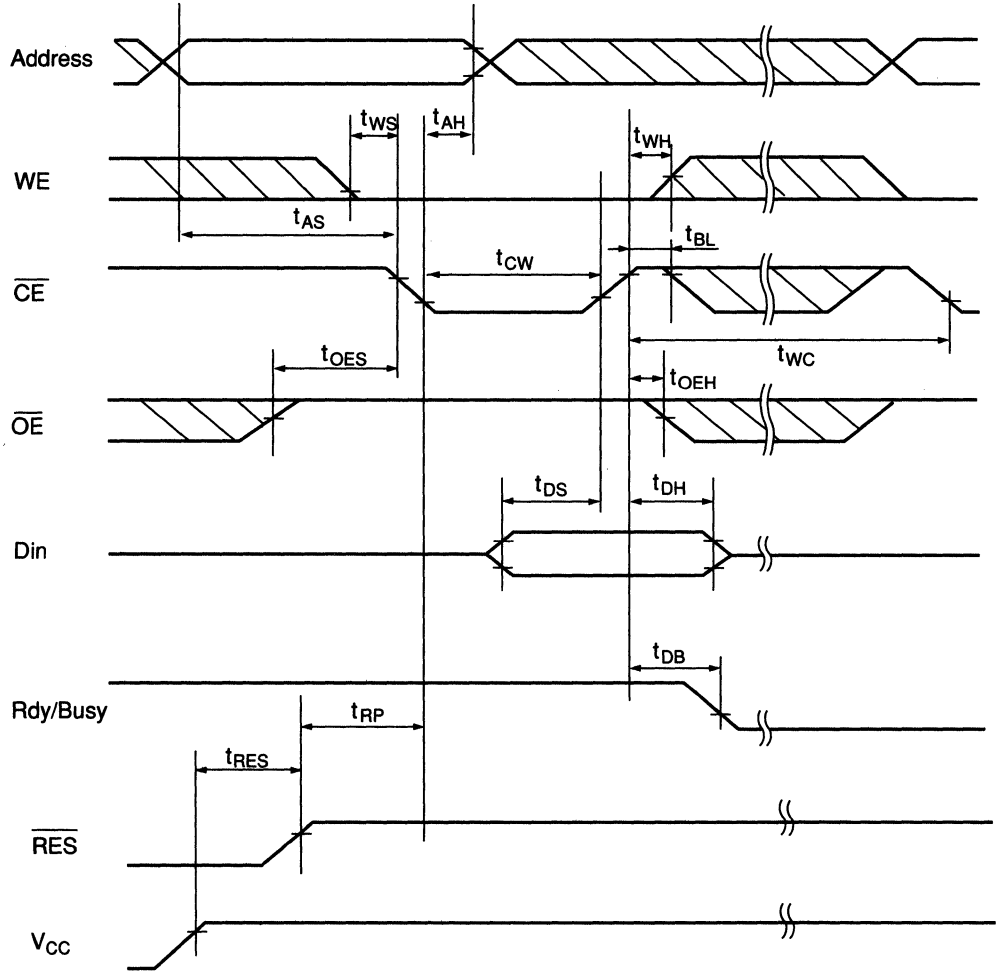
■ BYTE ERASE AND BYTE WRITE TIMING WAVEFORM ($\overline{WE}$ Controlled)



(TD.BE1.HN58C1001)

5

■ BYTE ERASE AND BYTE WRITE TIMING WAVEFORM ($\overline{CE}$ Controlled)



(TD.BE2.HN58C1001)

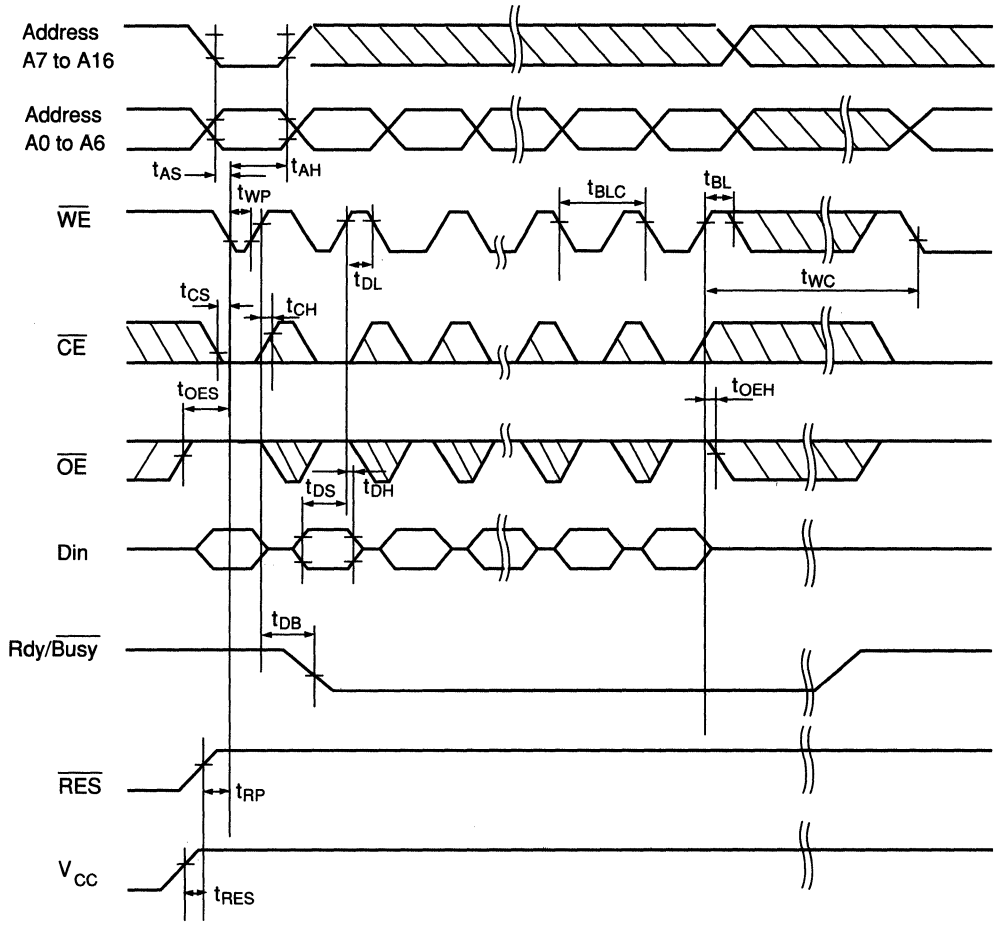
■ AC ELECTRICAL CHARACTERISTICS FOR PAGE ERASE AND PAGE WRITE OPERATIONS

Item	Symbol	Min.[1]	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	0	-	-	ns	
Write Enable to Write Setup Time	t_{WS}[3]	0	-	-	ns	
Chip Enable to Write Setup Time	t_{CS}[2]	0	-	-	ns	
Write Pulse Width	t_{WP}[2]	250	-	-	ns	
	t_{CW}[3]	250	-	-	ns	
Address Hold Time	t_{AH}	150	-	-	ns	
Data Setup Time	t_{DS}	100	-	-	ns	
Data Hold Time	t_{DH}	10	-	-	ns	
Write Enable Hold Time	t_{WH}[3]	0	-	-	ns	
Chip Enable Hold Time	t_{CH}[2]	0	-	-	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Output Enable Hold Time	t_{OEH}	0	-	-	ns	
Data Latch Time	t_{DL}	750	-	-	ns	
Write Cycle Time	t_{WC}	15	-	-	ms	
Byte Load Window	t_{BL}	100	-	-	µs	
Byte Load Cycle	t_{BLC}	1	-	30	µs	
Time to Device Busy	t_{DB}	120	-	-	ns	
$\overline{RES}$ to Write Setup Time	t_{RP}	100	-	-	µs	
V_{CC} to $\overline{RES}$ Setup Time	t_{RES}	1	-	-	µs	

Notes: 1. Use this device in longer cycle than this value.
2. $\overline{WE}$ controlled operation.
3. $\overline{CE}$ controlled operation.

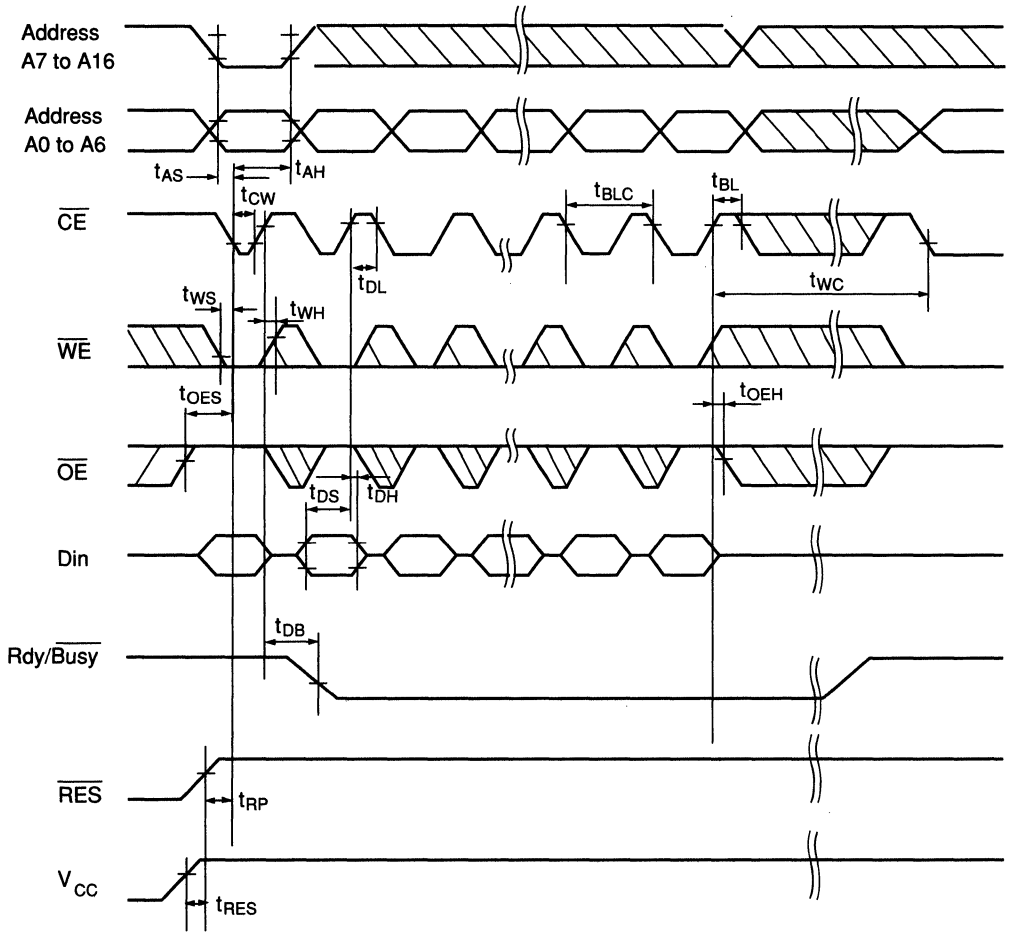
5

■ PAGE ERASE AND PAGE WRITE TIMING WAVEFORM ($\overline{WE}$ Controlled)



(TD.PE1.HN58C1001)

■ PAGE ERASE AND PAGE WRITE TIMING WAVEFORM ($\overline{CE}$ Controlled)



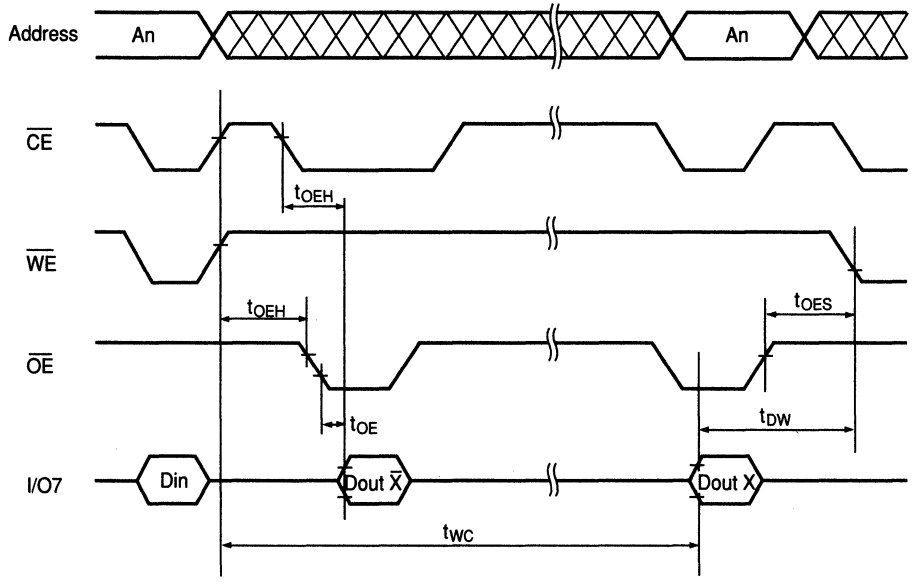
(TD.PE2.HN58C1001)

5

■ AC ELECTRICAL CHARACTERISTICS FOR $\overline{DATA}$ POLLING OPERATION

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Output Enable Hold Time	t_{OEH}	0	-	-	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Write Start Time	t_{DW}	150	-	-	ns	
Write Cycle Time	t_{WC}	-	-	15	ms	

■ $\overline{DATA}$ POLLING TIMING WAVEFORM

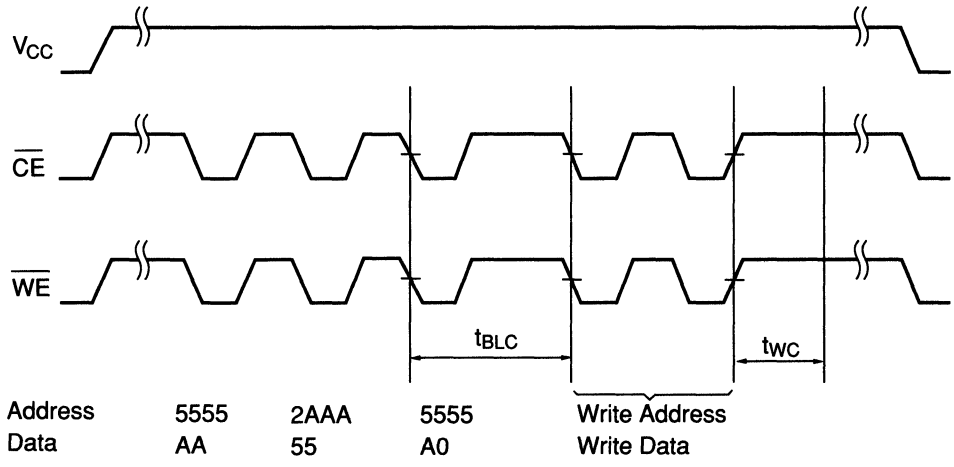


(TD.DP.HN58C1001)

■ AC ELECTRICAL CHARACTERISTICS FOR SOFTWARE DATA PROTECTION CYCLE OPERATION

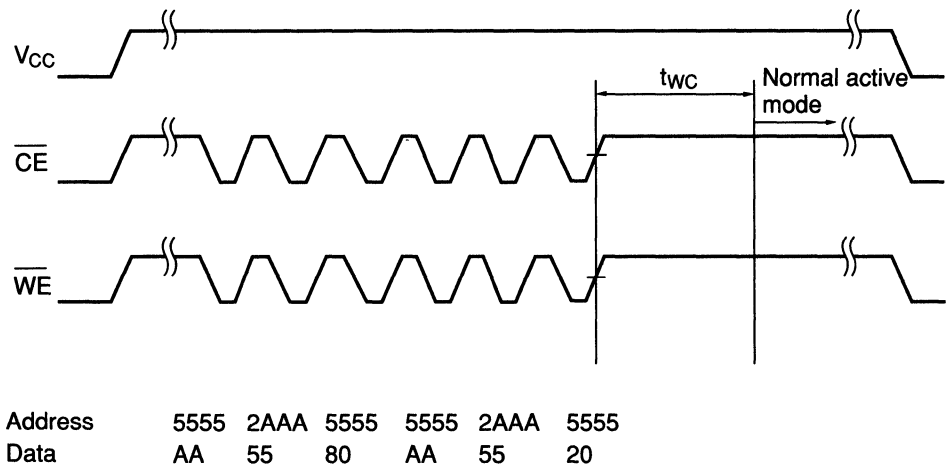
Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Byte Load Cycle Time	t_{BLC}	1	-	30	µs	
Write Cycle Time	t_{WC}	10	-	-	ms	

■ SOFTWARE DATA PROTECTION TIMING WAVEFORM (Protection Mode)



(TD.SD1.HN58C1001)

■ SOFTWARE DATA PROTECTION TIMING WAVEFORM (Non-Protection Mode)



(TD.SD2.HN58C1001)

5

■ FUNCTIONAL DESCRIPTION

Automatic Page Write

The Page Write feature allows 1 to 128 Bytes of data to be written into the EEPROM in a single cycle and allows the undefined data within 128 Bytes to be written corresponding to the undefined address (A_0 to A_6). Loading the first Byte of data, the data load window of 30 µs opens for the second. In the same manner each additional Byte of data can be loaded within 30 µs. In case $\overline{CE}$ and $\overline{WE}$ are kept high for 100 µs after data input, the EEPROM enters erase and write automatically and only the input data are written into the EEPROM. In Page mode the data can be written and accessed 10^5 times per page, and in Byte mode 10^4 times per Byte.

$\overline{\text{Data}}$ Polling

$\overline{\text{Data}}$ Polling allows the status of the EEPROM to be determined. If the EEPROM is set to Read mode during a Write cycle, an inversion of the last Byte of data to be loaded outputs from I/O_7 to indicate that the EEPROM is performing a Write operation.

Write Protection

(1) Noise protection: Noise on a write cycle will not act as a trigger with a $\overline{WE}$ pulse of less than 20 ns.

(2) Write inhibit: Holding $\overline{OE}$ low, $\overline{WE}$ high, or $\overline{CE}$ high, inhibits a write cycle during power on/off.

$\overline{WE}$ and $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

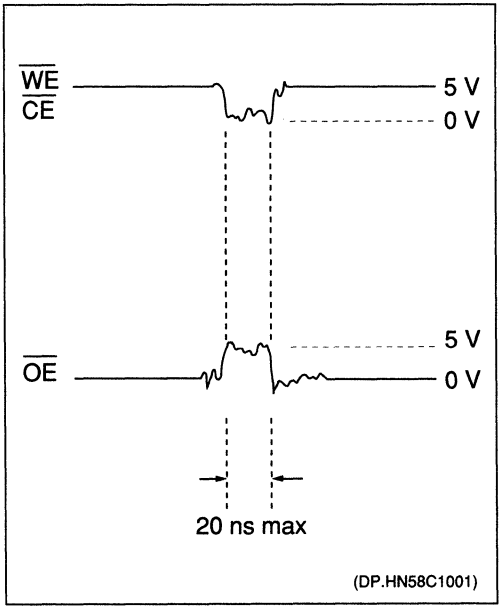
Write/Erase Endurance and Data Retention

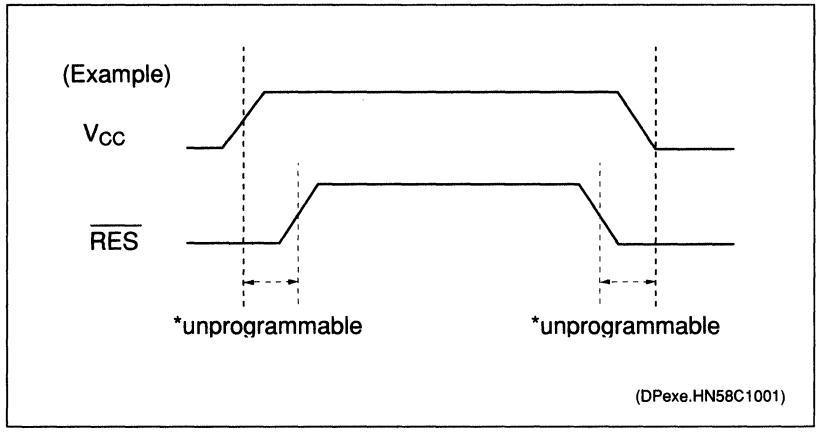
The endurance with page programming is 10^5 cycles (1% cumulative failure rate) and the data retention time is more than 10 years when a device is programmed less than 10^4 cycles.

Data Protection

To protect the data during operation and power on/off, the HN58V1001 has:

1. Data protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation.
   During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. To prevent this phenomenon, the HN58V1001 has a noise cancellation function that cuts noise if its width is 20 ns or less in programming mode. Be careful not to allow noise of a width of more than 20 ns on the control pins.





■ FUNCTIONAL DESCRIPTION (continued)

Data Protection (continued)

2. Data protection at V_{CC} on/off
   When $\overline{RES}$ is low, the EEPROM cannot be erased and programmed. Therefore, data can be protected by keeping $\overline{RES}$ low when V_{CC} is switched. $\overline{RES}$ should be high during programming because it does not provide a latch function.
   When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may turn the EEPROM to programming mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable, standby or readout state by using a CPU reset signal to $\overline{RES}$ pin.
   In addition, when $\overline{RES}$ is kept high at V_{CC} on/off timing, the input level of control pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) must be held as $\overline{CE}$=V_{CC} or $\overline{OE}$=Low or $\overline{WE}$=V_{CC} level.

3. Software data protection
   To prevent unintentional programming caused by noise generated by external circuits, HN58V1001 has a Software data protection function. In Software data protection mode, 3 Bytes of data must be input before the Write data. These Bytes can switch the Non-Protection mode to the Protection mode.

Address	Data
5555	AA
⇓	⇓
2AAA	55
⇓	⇓
5555	A0
⇓	⇓
Write Address	**Write Data**

(Normal Data Input)

The Software data protection mode can be cancelled by inputting the following 6 Bytes. This changes the HN58V1001 turns to the Non-Protection mode and it can write data normally. When the data is input during the cancelling cycle, the data cannot be written.

Address	Data
5555	AA
⇓	⇓
2AAA	55
⇓	⇓
5555	80
⇓	⇓
5555	AA
⇓	⇓
2AAA	55
⇓	⇓
5555	20

5

REGIONAL OFFICES

Northeast Region
Hitachi America, Ltd.
77 S. Bedford Street
Burlington, MA 01803
(617) 229-2150

Southeast Region
Hitachi America, Ltd.
5511 Capital Center Drive
Suite 204
Raleigh, NC 27606
(919) 233-0800

North Central Region
Hitachi America, Ltd.
500 Park Boulevard
Suite 415
Itasca, IL 60143
(708) 773-4864

South Central Region
Hitachi America, Ltd.
Two Lincoln Centre
5420 LBJ Freeway
Suite 1446
Dallas, TX 75240
(214) 991-4510

Pacific Mountain Region
Hitachi America, Ltd.
Metropoint
4600 S. Ulster Street
Suite 690
Denver, CO 80237
(303) 779-5535

Northwest Region
Hitachi America, Ltd.
1740 Technology Drive
Suite 500
San Jose, CA 95110
(408) 451-9570

Southwest Region
Hitachi America, Ltd.
2030 Main Street
Suite 450
Irvine, CA 92714
(714) 553-8500

IBM Region
Hitachi America, Ltd.
21 Old Main Street
Suite 104
Fishkill, NY 12524
(914) 897-3000

Automotive Region
Hitachi America, Ltd.
290 Town Center Drive
Suite 311
Dearborn, MI 48126
(313) 271-4410

THIRD-PARTY ASIC DESIGN CENTERS

Indiana Microelectronics Center
118 E. Ludwig Road
Fort Wayne, IN 46825
(219) 482-8200

LOCUS
1842 Hoffman Street
Madison, WI 53704
(608) 244-0500

DISTRICT OFFICES

Florida
Hitachi America, Ltd.
4901 N.W. 17th Way
Suite 302
Ft. Lauderdale, FL 33309
(305) 491-6154

Mid-Atlantic
Hitachi America, Ltd.
325 Columbia Turnpike
Suite 203
Florham Park, NJ 07032
(201) 514-2100

Minnesota
Hitachi America, Ltd.
3800 W. 80th Street
Suite 1050
Bloomington, MN 55431
(612) 896-3444

Texas
Hitachi America, Ltd.
10777 Westheimer Drive
Suite 1040
Houston, TX 77042
(713) 974-0534

Hitachi America, Ltd.
9600 Great Hills Trail
Suite 150 W
Austin, TX 78759
(512) 502-3033

Canada
Hitachi (Canadian) Ltd.
320 March Road
Suite 602
Kanata, Ontario, Canada
K2K2E3
(613) 591-1990

DISTRIBUTORS

Cronin Electronics, Inc.
ITT Multicomponents Canada
Marsh Electronics, Inc.
Marshall Industries
Milgray Electronics, Inc.
Reptron Electronics
Sterling Electronics
Vantage Components Inc.
Western Micro Technology

MAIN OFFICES

Hitachi America, Ltd.
Semiconductor & I.C. Division
San Francisco Center
2000 Sierra Point Parkway
Brisbane, CA 94005-1819
(415) 589-8300

Engineering Facility
Hitachi Micro Systems, Inc.
179 East Tasman Drive
San Jose, CA 95134

Manufacturing Facility
Hitachi Semiconductor
(America) Inc.
6431 Longhorn Drive
Irving, TX 75063

HITACHI®

Hitachi America, Ltd.
Semiconductor & I.C. Division
2000 Sierra Point Parkway
Brisbane, CA 94005–1819
415–589–8300

Printed on recycled paper.

993/GI/10M/PJM
Order Number: M13T028

HITACHI®

Our Standards Set Standards

Hitachi America, Ltd.
Semiconductor & I.C. Division
Hitachi Plaza
2000 Sierra Point Parkway, Brisbane, CA 94005-1819
1-415-589-8300

993/10M/GI/PJM
Order Number: M13T028
Printed on recycled paper.