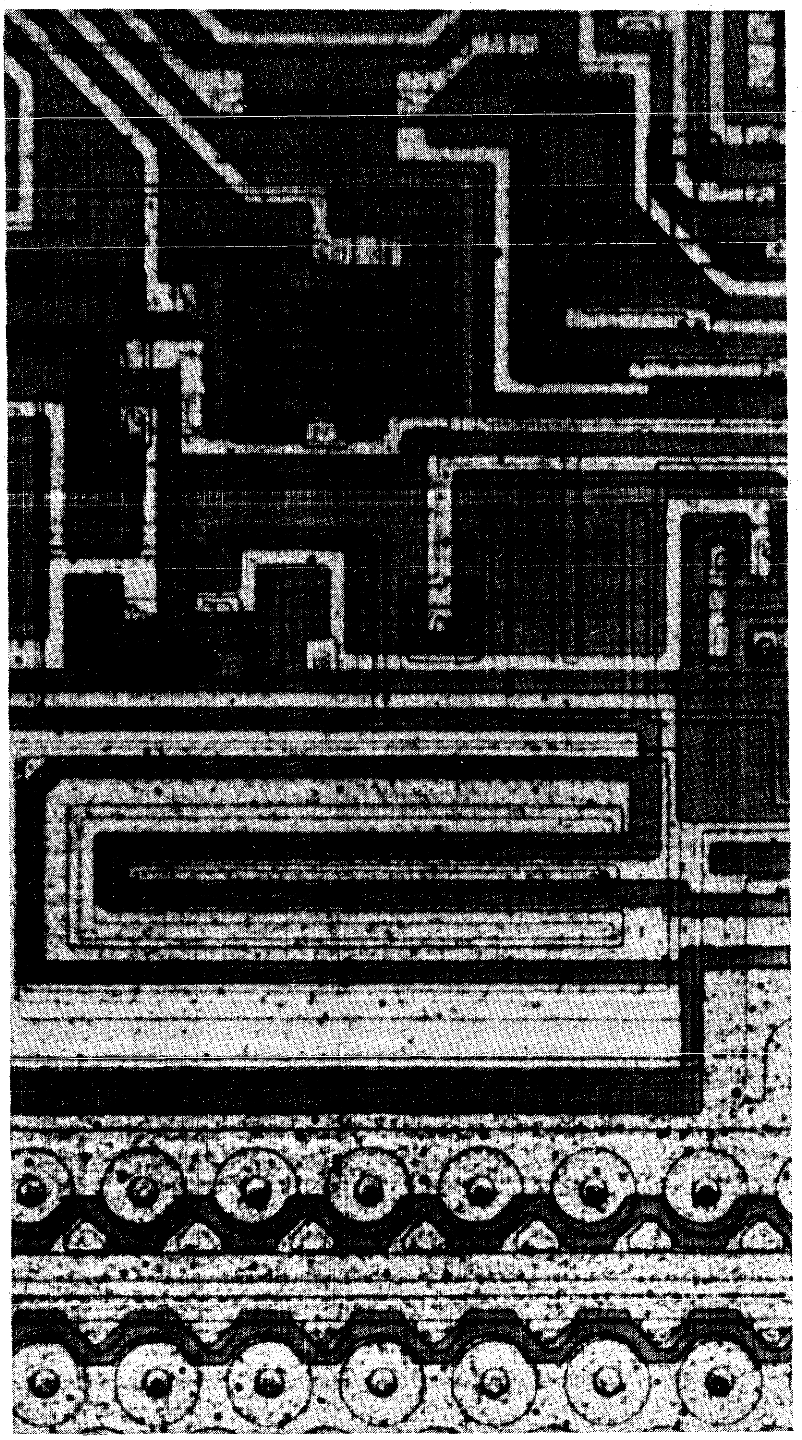
1984 IC MASTER

VOLUME II



Courtesy of Intel Corporation

CONTENTS

VOLUME I

VOLUME II

INTERFACE–Analog to Digital Converters

Bits Res.	Linearity Error ±LSB	Conversion Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source
Binary Output																	
3	1/8	0.02	—	x												**ADC-HU3B**	**Datel (2862)**
4	1/4	0.033*	250	x		x		x			x			x		**TDC1021**	**† TRW-LSI (3704)**
				x		x		x			x			x		TDC1021	TRW-LSI
	1/2	0.03*	800	x		x								x		UAB1005	Thomson-CSF
				x		x								x		UAC1005	† Thomson-CSF
6		0.004*	600*	x										x		**54F500**	**† Fairchild (762)**
				x										x		**74F500**	**Fairchild (762)**
	—	1	—										x			**MAH-0801**	**AD (2839)**
	1/8	—														**AD5010K**	**AD (2839)**
																AD6020K	**AD (2839)**
	1/4	0.02	450	x	x						x			x		SDA5010	Siemens
				x	x						x			x		SDA6020	Siemens
	1/2	0.01	1600	x	x		x							x		TDC1029	† TRW-LSI
		0.02	1000	x												ZN440CJ	Ferranti
		0.033*	1000	x		x		x			x			x		**TDC1014**	**† TRW-LSI (3704)**
				x		x		x			x			x		TDC1014	TRW-LSI
		0.066	315										x	x		**CA3300**	**RCA (3600)**
		90	120	x											x	NE5036	Signetics
		100	100	x										x		**NE5037**	**Signetics (3610)**
		100MHz	—	x	x		x							x		**TDC1029**	**† TRW-LSI (3704,3707)**
		1000	20*	x											x	TL507C	TI
7	1/4	—	1200	x										x		**MC10315L**	**Motorola (3070)**
				x										x		**MC10317L**	**Motorola (3070)**
	1/2	0.055	1604	x	x		x							x		TDC1027	† TRW-LSI
		20MHz	—	x	x		x							x		**TDC1027**	**† TRW-LSI (3704,3706)**
	1	—	100*											x	x	TM1070	Telmos
		6 MHz	150	x										x		TML1073	Telmos
8	—	1	—										x			**MAH-1001**	**AD (2839)**
	1/4	9	—		x	x							x	x		ZN447E-8	DDC
					x	x							x	x		ZN447J-8	† DDC
			125	x	x								x	x		**ADC-847B**	**Datel (2863)**
				x	x								x	x		**ADC-847M**	**† Datel (2863)**
			125*	x	x								x	x		ZN447E	Ferranti
				x	x								x	x		ZN447J	† Ferranti
		100*	875	x										x		**ADC0801**	**† Intersil (2993)**
				x										x		**ADC0801C**	**Intersil (2993)**
		110	875	x										x		ADC0801	† National
				x										x		ADC0801C	National
		200	0.3*	x						x						TL522	TI
	1/2	0.02	4500	x	x		x							x		TDC1025	† TRW-LSI
		0.033*	2500	x		x		x			x			x		**TDC1007**	**† TRW-LSI (3704)**
				x		x		x			x			x		TDC1007	TRW-LSI
		0.05	1320	x										x		**TDC1048**	**† TRW-LSI (3703)**
		0.066	315										x	x		**CA3308**	**RCA (3600)**
		0.4	400	x										x		**TDC1001**	**TRW-LSI (3704)**
		0.6	1250	x	x			x						x	x	ADC-815MC	Datel
				x	x			x						x	x	ADC-815MM	† Datel
						x	x	x					x	x	x	**MN5815**	**† MicroNet (3043)**
		0.9	1400			x	x						x	x	x	DDC-5101	† DDC
			1550	x	x									x	x	**ADC-5101**	**Datel (2860)**
				x	x									x	x	**ADC-5101E**	**Datel (2860)**
				x		x								x	x	**ADC-5101H**	**† Datel (2860)**
				x		x	x						x	x	x	**MN5101**	**MicroNet (3043)**
				x		x	x						x	x	x	**MN5101H**	**† MicroNet (3043)**

(Continued)

Bin.—Binary Off.—Offset Compl.—Complementary Magn.—Magnitude CTC—Compl. 2's Compl. Int. Ref.—Internal Reference Mux. In—Multiplexed Inputs S&H—Sample and Hold Par. Out—Parallel Output Ser. Out—Serial Output

ANALOG TO DIGITAL CONVERTERS

	MODEL NO.	RESOLUTION	CONVERSION TIME	LINEARITY	OPERATING TEMP. RANGE (°C)
	ADC-826MR	10 bits	1.4 μsec	± ½ LSB	−25 to + 85
	ADC-827MC	12 bits	3 μsec	± ½ LSB	0 to + 70
	ADC-827MR	12 bits	3 μsec	± ½ LSB	−25 to + 85
	ADC-830C	8 bits	100 μsec	± ½ LSB	0 to + 70
	ADC-833R	6 bits	66 nsec	± ½ LSB	−25 to + 85
NEW	ADC-847A	8 bits	9 μsec	± 1 LSB	0 to + 70
NEW	ADC-847B	8 bits	9 μsec	± ¼ LSB	0 to + 70
NEW	ADC-847M	8 bits	9 μsec	± ¼ LSB	−55 to + 125
	ADC-856C	10 bits	1μsec/LSB	± ½ LSB	0 to + 70
	ADC-856M	10 bits	1μsec/LSB	± ½ LSB	−55 to + 125
	ADC-5101	8 bits	900 nsec	± ½ LSB	0 to + 70
	ADC-5101E	8 bits	900 nsec	± ½ LSB	−25 to + 85
	ADC-5210	12 bits	13 μsec	± ½ LSB	0 to + 70
	ADC-5210E	12 bits	13 μsec	± ½ LSB	−25 to + 85
	ADC-5211	12 bits	13 μsec	± ½ LSB	0 to + 70
	ADC-5211E	12 bits	13 μsec	± ½ LSB	−25 to + 85
	ADC-5212	12 bits	13 μsec	± ½ LSB	0 to + 70
	ADC-5212E	12 bits	13 μsec	± ½ LSB	−25 to + 85
	ADC-5213	12 bits	13 μsec	± ½ LSB	0 to + 70
	ADC-5213E	12 bits	13 μsec	± ½ LSB	−25 to + 85
	ADC-5214	12 bits	13 μsec	± ½ LSB	0 to + 70
	ADC-5214E	12 bits	13 μsec	± ½ LSB	−25 to + 85
	ADC-5215	12 bits	13 μsec	± ½ LSB	0 to + 70
	ADC-5215E	12 bits	13 μsec	± ½ LSB	−25 to + 85
	ADC-5216	12 bits	13 μsec	± ½ LSB	0 to + 70
	ADC-5216E	12 bits	13 μsec	± ½ LSB	−25 to + 85

DIGITAL TO ANALOG CONVERTERS

	MODEL NO.	RESOLUTION	OUTPUT SETTLING TIME	LINEARITY	OPERATING TEMP. RANGE (°C)
	DAC-HA10BC	10 bits	1.3 μsec	± ½ LSB	0 to + 70
	DAC-HA10BR	10 bits	1.3 μsec	± ½ LSB	−25 to + 85
	DAC-HA12BC	12 bits	5 μsec	± ½ LSB	0 to + 70
	DAC-HA12BR	12 bits	5 μsec	± ½ LSB	−25 to + 85
	DAC-HA14BC	14 bits	7 μsec	± ½ LSB	0 to + 70
	DAC-HA14BR	14 bits	7 μsec	± ½ LSB	−25 to + 85
	DAC-HF8BMC	8 bits	25 nsec	± ½ LSB	0 to + 70
	DAC-HF8BMR	8 bits	25 nsec	± ½ LSB	−25 to + 85
	DAC-HF10BMC	10 bits	25 nsec	± ½ LSB	0 to + 70
	DAC-HF10BMR	10 bits	25 nsec	± ½ LSB	−25 to + 85
	DAC-HF12BMC	12 bits	50 nsec	± ½ LSB	0 to + 70
	DAC-HF12BMR	12 bits	50 nsec	± ½ LSB	−25 to + 85
	DAC-HK12BGC	12 bits	3 μsec	± ½ LSB	0 to + 70
	DAC-HK12BMC	12 bits	3 μsec	± ½ LSB	0 to + 70
	DAC-HK12BMR	12 bits	3 μsec	± ½ LSB	−25 to + 85
	DAC-HP16BGC	16 bits	15 μsec	± ½ LSB	0 to + 70
	DAC-HP16BMC	16 bits	15 μsec	± ½ LSB	0 to + 70
	DAC-HP16BMR	16 bits	15 μsec	± ½ LSB	−25 to + 85
	DAC-HZ12BGC	12 bits	3 μsec	± ½ LSB	0 to + 70
	DAC-HZ12BMC	12 bits	3 μsec	± ½ LSB	0 to + 70
	DAC-HZ12BMR	12 bits	3 μsec	± ½ LSB	−25 to + 85
	DAC-IC8BC	8 bits	300 nsec	± ½ LSB	0 to + 70
	DAC-IC8BM	8 bits	300 nsec	± ½ LSB	−55 to + 125
	DAC-IC10BC	10 bits	250 nsec	± 1 LSB	0 to + 70
	DAC-IC10B	10 bits	250 nsec	± ½ LSB	0 to + 70
	DAC-IC10BM	10 bits	250 nsec	± ½ LSB	−55 to + 125
	DAC-UP8BC	8 bits	2 μsec	± ½ LSB	0 to + 70
	DAC-UP8BM	8 bits	2 μsec	± ½ LSB	−55 to + 125
	DAC-UP10BC	10 bits	5 μsec	± ½ LSB	0 to + 70
	DAC-08BC	8 bits	150 nsec	± ½ LSB	0 to + 70
	DAC-08BM	8 bits	150 nsec	± ½ LSB	−55 to + 125
	DAC-85C-CBI-I	12 bits	300 nsec	± ½ LSB	0 to + 70
	DAC-85C-CBI-V	12 bits	3 μsec	± ½ LSB	0 to + 70
	DAC-85-CBI-I	12 bits	300 nsec	± ½ LSB	−25 to + 85
	DAC-85-CBI-V	12 bits	3 μsec	± ½ LSB	−25 to + 85
	DAC-562C	12 bits	400 nsec	± ½ LSB	0 to + 70
	DAC-562M	12 bits	400 nsec	± ½ LSB	−55 to + 125
	DAC-608	8 bits	1 μsec	± ½ LSB	0 to + 70
	DAC-610	10 bits	500 nsec	± ½ LSB	0 to + 70
	DAC-612	12 bits	1 μsec	± ½ LSB	−25 to + 85
NEW	DAC-7523	8 bits	200 nsec	±.1%	0 to + 70
NEW	DAC-7533	10 bits	800 nsec	±.01%	0 to + 70
NEW	DAC-7541	12 bits	1 μsec	±.012%	0 to + 70

DATEL 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

MITEL

MD54/74HCT245R

Octal Bus Transceivers with 3-State Buffered Outputs

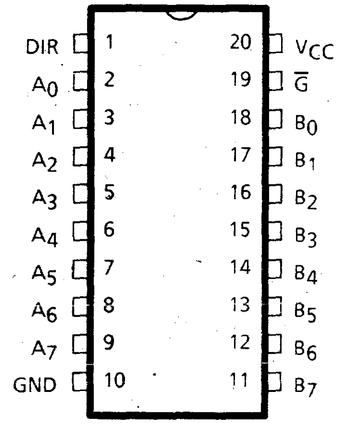
Preliminary Information

October'83

Features

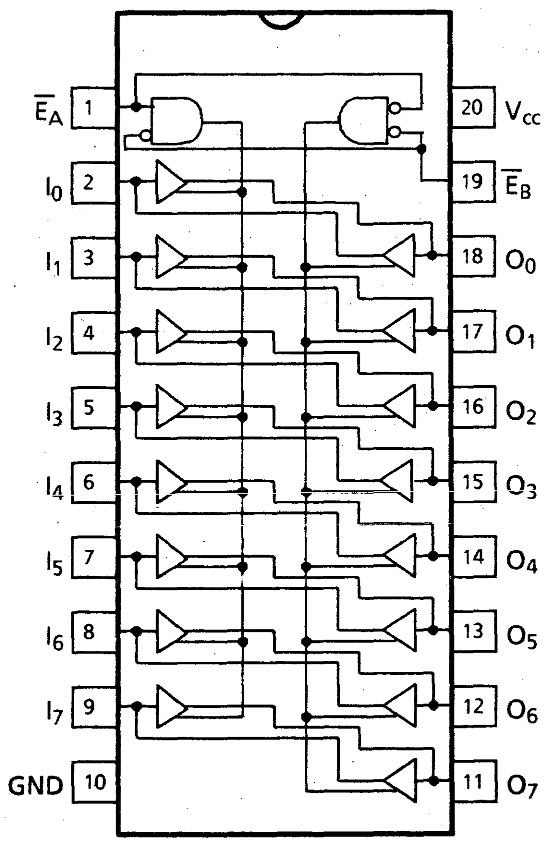
- High latch-up immunity
- High current outputs can drive 30 LSTTL loads
- Low power ISO-CMOS technology
- Bus oriented 3-state outputs
- Meets or exceeds all proposed JEDEC 40.2 specifications
- Fully TTL compatible inputs and outputs
- Pin compatible with 54/74LS245 types

CONNECTION DIAGRAM
DIP (TOP VIEW)



Description

These ISO-CMOS Octal line driver/buffers are designed for high speed asynchronous two-way communication between data buses. The control function inputs minimize external timing requirements. Data transmission from the A bus to the B bus, or from the B bus to the A bus, is provided depending upon the logic leve; at the direction control input (DIR) pin. The enable input (G) pin can be used to disable the device outputs so that the buses are effectively isolated from each other.



Ordering Information

MD54HCT245RCB, Cerdip
-55°C to 125°C
with MIL 883B option

MD74HCT245RE, Plastic Dip
-40°C to 85°C

PIN	DESCRIPTION
A_0 - A_7	Bus A, Data Inputs/Outputs
B_0 - B_7	Bus B, Data Inputs/Outputs
DIR	Direction Control Pin
$\overline{G}$	Enable Input, Active Low
V_{CC}	Supply Voltage
GND	System Ground

FUNCTION TABLE

INPUT	OUTPUT	
ENABLE (G)	CONTROL (DIR)	OPERATION
L	L	A to B
L	H	A to B
H	X	ISOLATION

H = logic "1", L = logic "0", X = don't care,
Z = high impedance

1984 IC MASTER

VOLUME II

Engineering design begins with the IC MASTER

Editor, **Dave Howell**
Technical Director, IC Division, **Jerry Metzger**
Assistant Editors, **Addie Bisignano, Gail LoBue, Kathy Schmidt**
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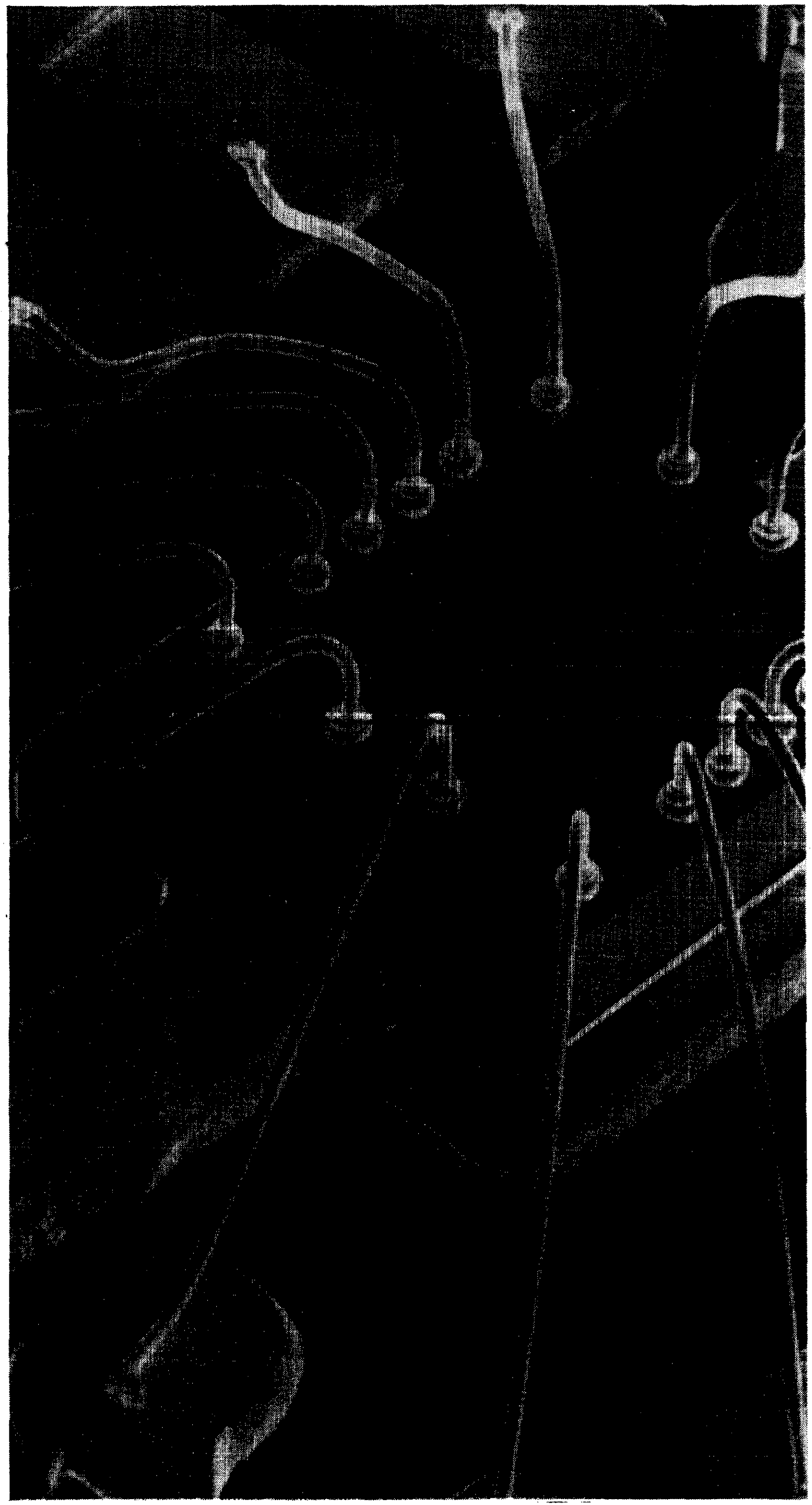
HEARST BUSINESS COMMUNICATIONS, INC./ UTP DIVISION
East Coast:
645 Stewart Avenue
Garden City, NY 11530
Tel: (516) 222-2500 Telex II 510-222-1673 (UTP GRCY)
West Coast:
1333 Lawrence Expressway, Suite 101
Santa Clara, CA 95051
Tel: (408) 248-8044 Telex II 910-338-0272



Courtesy of Delco Electronics

IMPORTANT FEATURES OF YOUR IC MASTER

ONE COMPLETE SOURCE
IC MASTER is the original and only complete guide to currently available integrated circuits, microcomputer boards, development systems. PROM programmers, gate arrays, and other related components of concern to the design engineer. It has become the first place to look in the critical selection of ICs, boards, systems, and equipment. If only one device can fit the requirements of a new design or if hundreds are available, you can find out in seconds by using the IC MASTER.

EASY TO USE
The IC MASTER saves you time. No longer do you have to spend long, tedious hours and days searching through manufacturers' catalogs and data sheets for information. The MASTER gives you—at your fingertips—an easy way to narrow your IC choices quickly, accurately, and systematically with the knowledge that you have just surveyed the entire industry.

PART NUMBER INDEX
This revolutionary index lists all device types made by over 225 manufacturers in numerical sequence excluding prefixes or suffixes. You can find a device number even though you do not know either the full part number or even the manufacturer. Once a basic device number is located in the index, you can obtain instant identification of all manufacturers making a device by that number, regardless of function, and determine the full part number designation. All page references to data sheet material and any existing application note abstracts are also provided. The Part Number Index should not be used as an alternate source directory because two manufacturers may use the same part number, by coincidence, for totally different devices.

PART NUMBER GUIDE
The information in this guide allows you to break down each company's part numbering system into product temperature ranges, packaging variations, and functions. It is an invaluable tool for the elimination of costly and time-consuming ordering errors caused by lack of standardization from manufacturer to manufacturer in part numbering systems.

APPLICATION NOTE DIRECTORY
Application note descriptions are arranged alphabetically by function and application category. Each note's description identifies the specific device or devices featured, provides a 25 to 30 word abstract, and identifies both the manufacturer that originated the note and the specific application note number. This section provides all the information necessary for you to update your application note files speedily, or thoroughly research the existence of application note material for a specific design problem.

MILITARY PARTS DIRECTORY
Cross reference chart identifies all IC devices having received JAN qualification. This chart includes a cross reference listing of device numbers and corresponding military standard 38510 slash numbers and vice versa.

MILITARY DEVICE TESTING TABLE
This table identifies IC manufacturers who test to military standard 38510 and the screening to military standard 883 that they provide.

MILITARY PARTS INDEX
This guide to JAN qualifed parts makes it possible to search devices by function, and to determine if a JAN qualified part exists for a particular functional need.

ADVERTISERS' PRODUCT INDEX
This index directs you to detailed product information for the parts whose manufacturers have included data sheets in IC MASTER. When you are looking for data on a particular manufacturer's products, this index provides the fastest way to find the information you seek.

ALTERNATE SOURCE DIRECTORY
The most comprehensive industry-wide, pin-for-pin, functional equivalent Alternate Source Directory ever compiled. This directory is updated by asking all IC manufacturers to identify each competitive device for which they make a pin-for-pin substitute.

MASTER SELECTION GUIDE
Each guide is organized by specifications and categories to direct you easily and quickly to the device most likely to fill your requirements for a particular application. Once you find those devices that are closest to your needs, you see available sources, and are directed to additional data if provided by advertisers.

MANUFACTURERS AND DISTRIBUTORS DIRECTORY
Locations and phone numbers are given for manufacturers' field sales offices, representatives, and distributors, both domestic and international.

Typical Problems Solved by IC MASTER

• Find All Products That Meet Desired Specifications
• Obtain Data For A Particular Device • Decode Part Numbers
• Determine Alternate Sources • Plus Much More

An engineer can use IC MASTER to solve a wide variety of problems. Answers provided to engineers by IC MASTER can range from finding the device that best meets a particular set of specifications to helping to determine which family of devices should be used in building a system.

Some of the typical problems that IC MASTER can solve are illustrated in the following examples:

Who makes a TTL 4-bit binary full-adder with look-ahead carry?

All functions are listed, in alphabetical order, in the Master Selection Guide Index. In this case, the engineer looks under adders; in the column adjacent to adders, he sees that all types of adders are listed. The particular adder being sought is covered in the Digital section of IC MASTER.

Now that the engineer knows that the devices he seeks are catalogued in the Digital section, he can turn to the Digital Master Selection Guide and see the page number where information on these devices can be obtained.

When he turns to this page, he will notice that certain device numbers and manufacturers are printed in bold face type while others appear in regular type face. Bold face type is used whenever a part's manufacturer has provided a data sheet for the device in IC MASTER. The page number assigned to the data sheet also appears in bold face type so that the engineer can turn to it directly.

Who Makes a High-Speed 12-Bit, Analog-to-Digital Converter With Guaranteed ±½ LSB Linearity and 13-μsec or Faster Conversion Time?

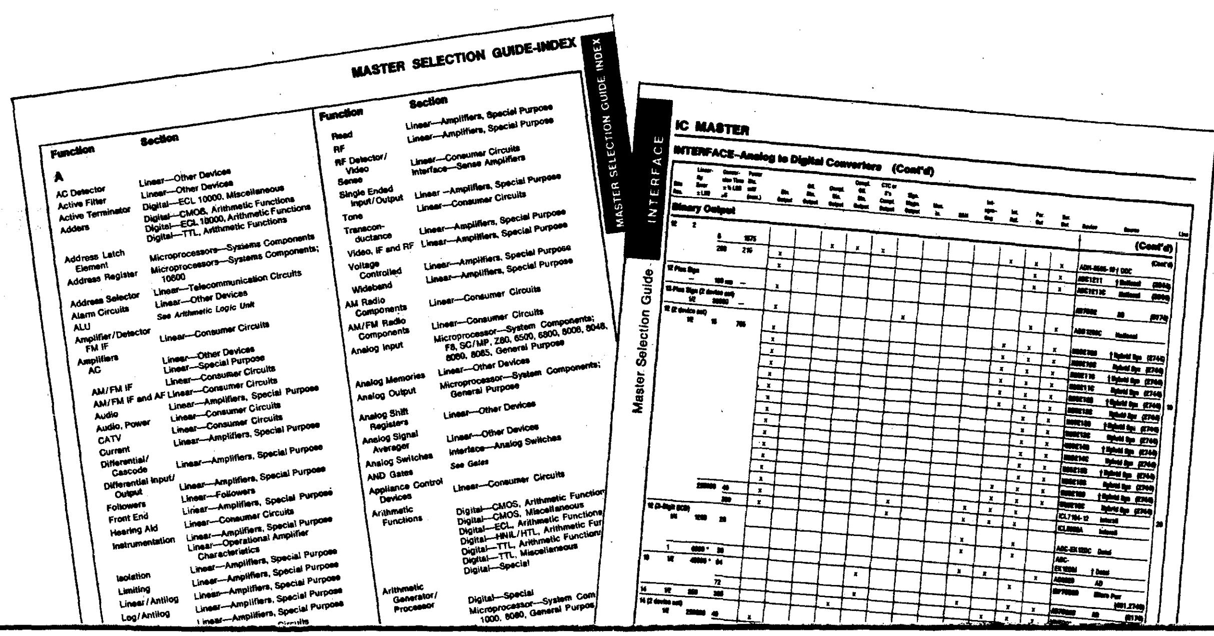
Many manufacturers make devices that meet these specifications including Analog Devices, Burr-Brown, Datel-Intersil, Data Device Corp., Harris, Hybrid Systems, Micro Networks, and Teledyne Philbrick.

The Master Selection Guide for Interface makes it possible for an engineer to find every device that meets the above specifications, regardless of who makes it, in seconds.

The Interface section is organized by product classification; an engineer can turn immediately to the category of interest such as analog switches with drivers, multiplexers, a/d converters with binary output a/d converters with decimal output, d/a converters, display drivers, error checking circuits, keyboard encoder-decoders, line drivers, line transceivers, memory and peripheral drivers, sense amplifiers, etc.

To find every 12-bit analog-to-digital converter with guaranteed ±½ LSB linearity and 13-μsec or faster conversion time, all an engineer has to do is turn directly to the analog-to-digital converter section of the Interface Master Selection Guide.

In this section, devices are organized by key parameters. Under resolution, the engineer finds 12-bit; next he looks under linearity error for ±½ LSB and then he looks under conversion time for devices with 13-μsec or faster specifications.



Ways to Use IC Master

What application notes are available on emulating logic functions with PROMs?

IC MASTER provides the most complete listing of application notes available in print. It is easy to find the right application notes by looking in IC MASTER because the application note directory is organized by function.

There are two ways to look up an application note. An engineer can turn to the index page and find the appropriate function or category such as instrumentation amplifiers, multiplexers, or PROMs.

If he knows the device number, he can look it up in the part number index at the front of IC MASTER and see all of the application notes concerning that device. For example, under 8275, a programmable CRT controller listed in the part number index, the reader is referred to the listing for an Intel application note entitled "CRT Terminal Design Using the 8275 and 8279."

To find an application note concerning the use of PROMs to emulate logic functions, the engineer can turn to the application note section on PROMs and see what notes can be of help.

Each listing in the application note directory provides a detailed descriptive passage for the note, gives its length and identifies the manufacturer who publishes it.

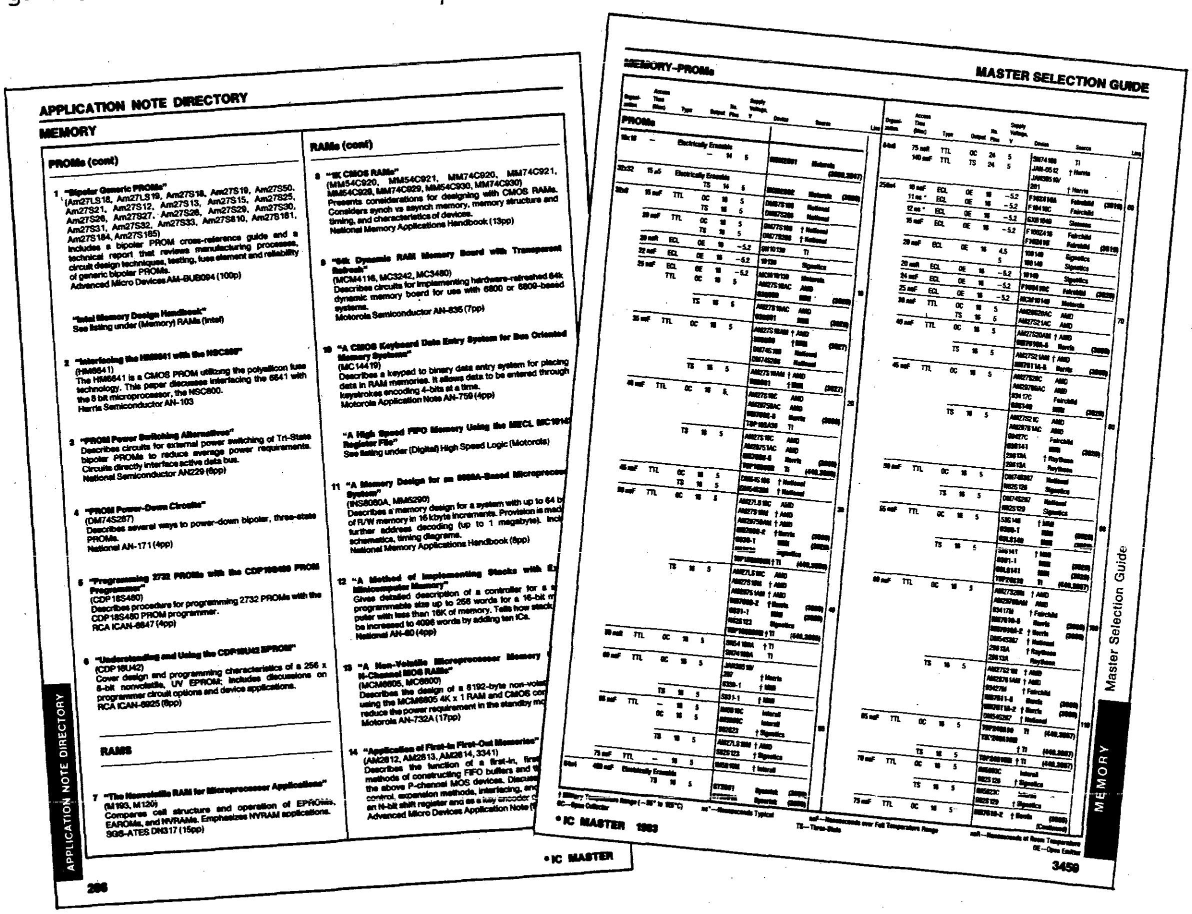
Who makes a 64K dynamic RAM with an access time of 120 ns or faster?

The Memory Section in IC MASTER has a Master Selection Guide which provides initial selection information and data on PROMs, RAMs, ROMs and other types of memories. Each device is characterized by organization (words and bit/word) and access time.

For example, if an engineer was looking for a 64K dynamic RAM, his first step would be to determine organization (words and bit/word). Next, he would locate the desired access time.

When devices are available made by various processes such as NMOS, CMOS, ECL, TTL, etc., the engineer can choose the device that best suits his needs. For further definition, output type, supply voltage and number of pins are listed along with the manufacturer's part number and name.

The engineer's next step in his memory selection process would be to study the applicable data for 64K dynamic RAMs provided by IC manufacturers and pick the most appropriate device. Literally hundreds of pages of engineering data on memories appear in IC MASTER.



Ways to Use IC Master

I need to choose between a full custom or a semi-custom/gate array solution to my design problem.

To help designers weigh custom solutions against semi-custom/gate array approaches, IC MASTER provides a Master Selection Guide on Custom/Semi-Custom and a special section entitled "Options for Going Custom." In this section the advantages and disadvantages of various custom/semi-custom techniques are covered.

The capabilities of IC manufacturers are tabulated for easy comparison; additional information such as available design aids and testing services is also provided.

My application requires microcomputer boards. How do I start?

Single and multiple board microcomputers are arranged by manufacturer. Under each manufacturer, boards are grouped in sequence according to data word size and, within that grouping, according to the microprocessor on which they are based. Hardware and software support are listed for each board.

A supplementary selection guide is included for microcomputer support boards. The boards are grouped according to supported computer systems.

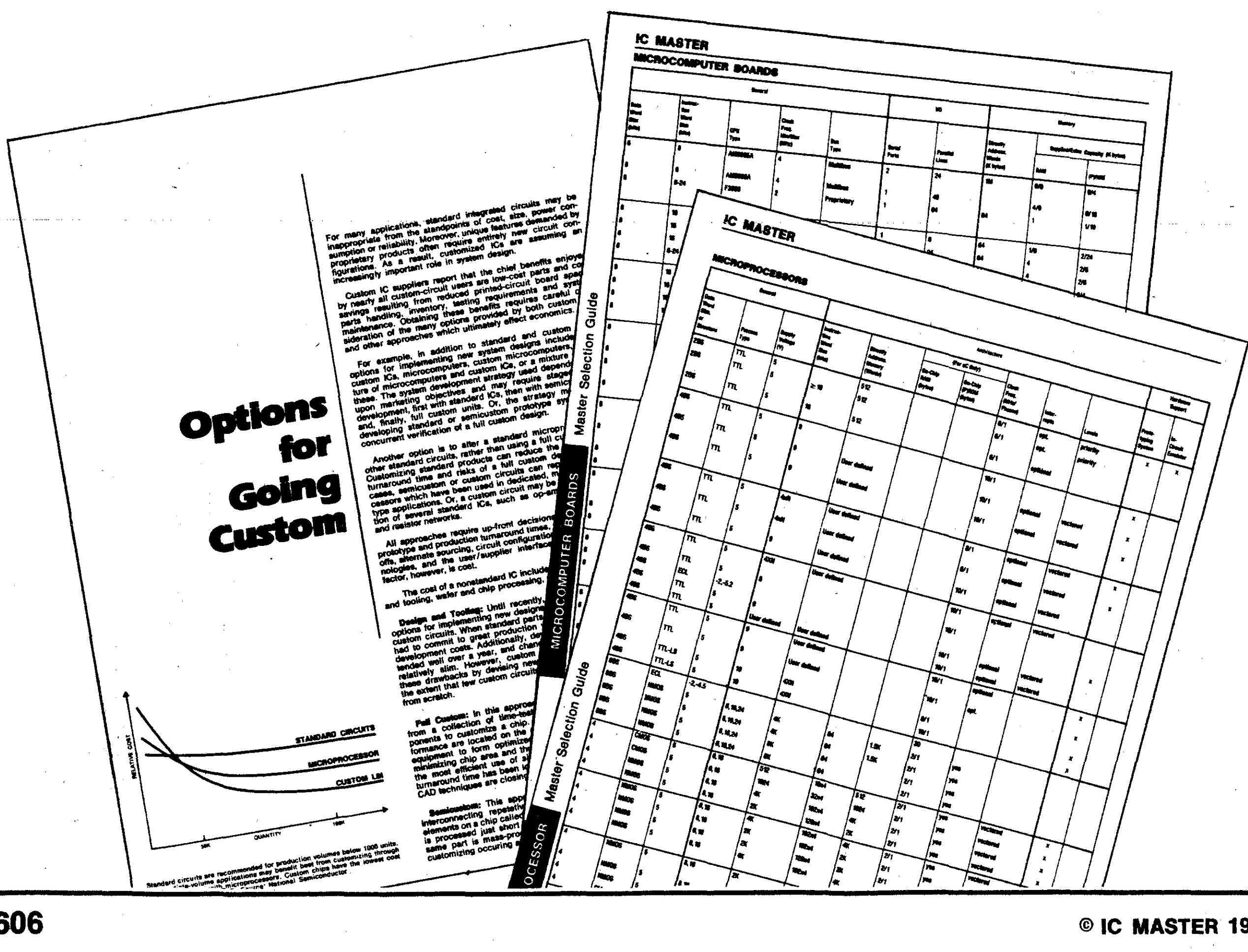
With so many mircoprocessors available, where do I begin?

Simply turn to the Master Selection Guide for Microprocessors. There you will find a listing of all microprocessors currently available and key parameters allowing you to narrow down your selection to a range of products that will meet your major requirements.

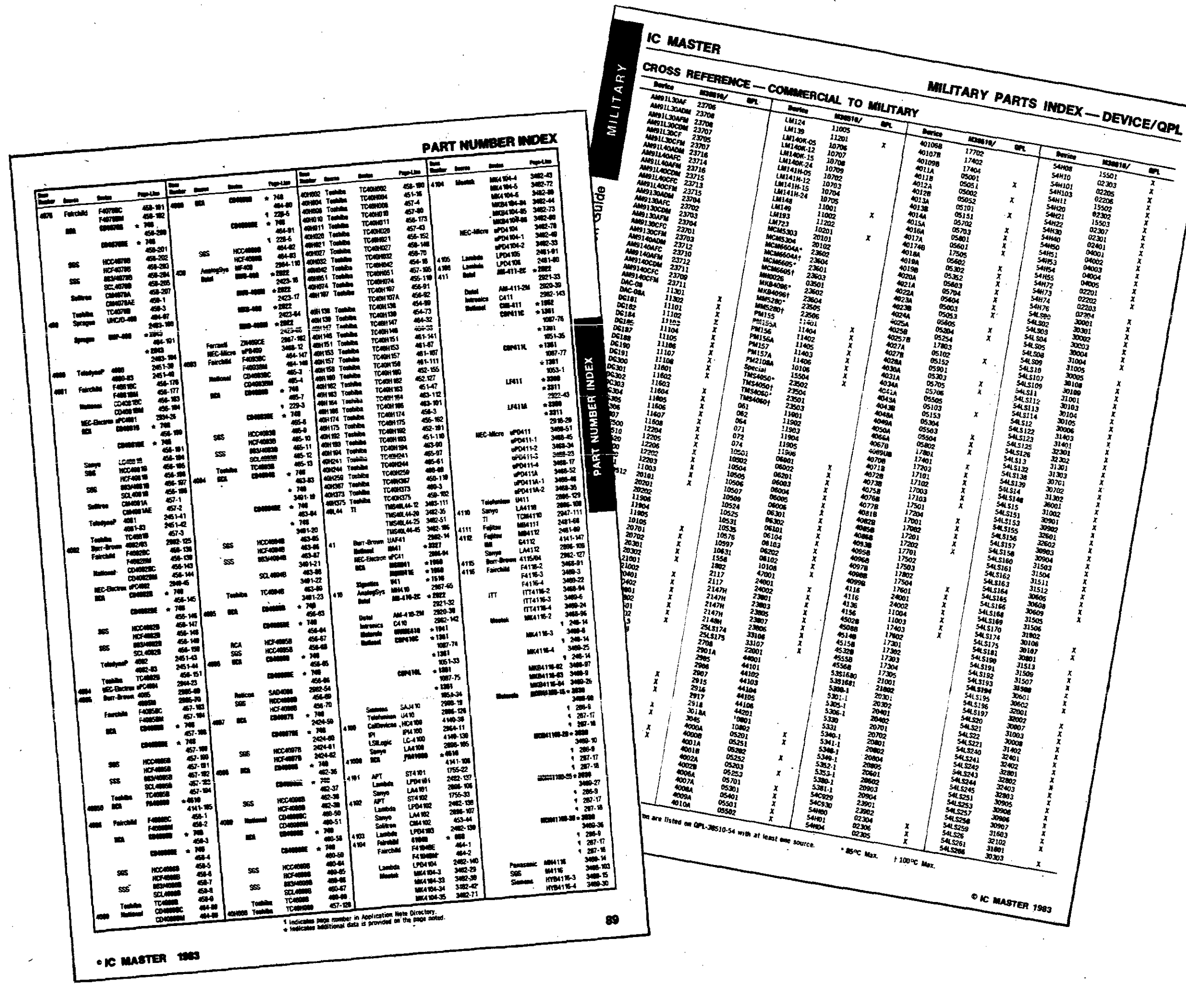
Once the microprocessor that best fits the application has been chosen, the next step is to go to the "system components" section. Here all of the available peripheral devices that work with each microprocessor are arranged by function. Thus, if the microprocessor that has been selected is the 8048, system components specifically developed for use with the 8048 are listed, organized by function.

A "general purpose" section follows the "system components" section and describes devices that can be used with more than one microprocessor family.

Finally, hundreds of pages of the latest microprocessor data sheets, provided by IC manufacturers, are presented, arranged in alphabetical order by manufacturer. Each data sheet is easily found thanks to boldfaced page-number references in the Master Selection Guide.



Ways to Use IC Master



If an engineer knows that the basic part number is 6508, where does he look first?

The place to look is the part number index. Here, all of the prefixes and suffixes have been stripped away to leave only the basic number. This makes it possible to see the manufacturer of every part with the same base number at a glance. Parts with the same base number, it should be kept in mind, are not necessarily identical; in fact, one could be a memory while another might be a linear device. (To find replacements, one should look in the alternate source directory, not in the part number index.)

Under 6508, the engineer would see a number of devices listed and the page and line numbers where data is given for each of the devices. If an application note concerning any of the devices is available, the location of its listing is also shown.

I design to military specs. Where can I find the latest QPL devices?

The IC MASTER includes a comprehensive military parts directory. Within this directory, tables and charts are provided to answer virtually every information need of the engineer involved in military or high-reliability equipment design.

All integrated circuits with JAN qualification are listed in IC MASTER. A cross reference table, relating device numbers to mil spec numbers, is arranged according to device number. A second table, arranged by M-38510 number, makes it possible to look up the part number when the mil spec number is known.

In addition, ICs are also organized by product section and function, which allows the user to find the proper IC without having to know either the commercial or the military part number.

This section of IC MASTER also includes a table showing the capability of manufacturers to perform MIL-STD-883 screening and high-reliability testing.

ADVERTISERS INDEX

INTRODUCTION TO INTERFACE

The Master Selection Guide provides sufficient information for making initial product selections. All devices that appear in this section, both in the initial selection guide and the data pages, are included in the indexes. These index listings lead to the page and line on that page where each device appears.

In the Interface Section the selection parameters differ drastically for each category; therefore each has its own format. The analog to digital converter category has two formats: one for binary output devices and another for decimal units. Some of the products in this section, primarily analog to digital and digital to analog converters, may be hybrids; the hybrids listed are only those packaged to be compatible with ICs.

This section is not complicated by reference to package styles; the package style suffixes are usually deleted. For more information on each companies' suffixes, see the Part Number Guide. Throughout the Master Selection Guide, each full military temperature range (−55°C to 125°C) device is indicated by a (†) before the manufacturer's name. Manufacturers' names are normally spelled out; however, a few are abbreviated and the abbreviations are explained on page 2809.

CATEGORY

Detailed Product Information provided by:

The manufacturers listed above have provided detailed information on their latest and most significant products.

EINFÜHRUNG INTERFACE-SCHALTUNGEN

Der Master Selection Guide für Interfaceschaltungen enhält alle Informationen, die Sie für die Erstauswahl Ihres Produkts benötigen. Die Bauteile, die in diesem Abschnitt erscheinen, sowohl im Selection Guide als auch auf den Datenblättern, sind in allen Master Indexes enthalten. Diese Register verweisen auf die Seite und Zeile, auf der das entsprechende Bauelement vorkommt.

Im Interface-Teil unterscheiden sich die Auswahl-Parameter drastisch für jede Kategorie; daher hat jede ihre eigene Tabelle. Für Analog-Digital-Wandler gibt es zwei Tabellen: eine für Bauteile mit Binär-Ausgang und eine weitere für Dezimal-Bauteile. Einige Produkte in diesem Teil, hauptsächlich Analog-Digital und Digital-Analog Wandler, können hybride Bauelemente sein. Es werden nur solche hybriden Bauteile aufgeführt, deren Gehäuse kompatibel zu ICs sind.

Dieser Abschnitt wird nicht durch Hinweise auf Gehäuseformen kompliziert. Die entsprechenden Suffixe sind meistens weggelassen. Weitere Information über die Suffixe jedes Herstellers erhalten Sie über das Numerische Typenverzeichnis. Im ganzen Master Selection Guide sind alle Bauteile mit militärischem Temperaturbereich (—55°C bis 125°C) durch ein Kreuz (†) vor dem Namen des Herstellers gekennzeichnet. Die Namen der Hersteller sind normalerweise ausgeschreiben; einge jedoch sind abgekürzt. Die Abkürzungen werden auf S. 2809 erklärt.

INTRODUCTION AUX INTERFACES

Le Guide Général de Sélection fournit suffisamment de renseignements pour permettre des sélections initiales de produits. Tous les appareils cités dans cette Section, à la fois dans la Premier Guide de Sélection et dans les feuilles de données, sont inclus dans tous les index. Ces index indiquent à quelle page et à quelle ligne sur cette page il a été fait mention de tel appareil.

Dans la Section "Interfaces", les paramètres de sélection changent pour chaque categorie, ce qui implique un format spécial pour chacun. Les convertisseurs analogues et digitaux ont deux formats : un pour les appareils à sortie binaire et un autre pour les unités décimales. Certains produits de cette Section, notamment les convertisseurs d'analogue à digital et de digital à analogue, peuvent être des hybrides. Les hybrides énumerés sont ceux qui possédent un boitier compatible aux circuits intégrés.

Cette Section ne fait pas référence aux types de boitier; les suffixes indiquant le type de boitier sont généralement omis. Pour plus d'information sur les suffixes employés par chaque société, reportez-vous au Guide des Numéros de Pièces. Dans tout le Guide Général de Sélection chaque appareil avec sélection compléte de températures imposées par l'Armée (—55°C à 125°C) est indiqué par le signe (†), juste avant le nom du fabricant, Les noms des fabricants sont généralement écrits en entier, certains cependant sont abrégés. Reportez-vous à la page 2809 pour connaître la signification de ces abréviations.

INTRODUCCIÓN A ZONA INTERFACIAL

La Guía Maestra de Selección provee suficiente información para hacer selecciones iniciales de producto. Todas las componentes que aparecen en esta sección, ya sea en la guía de selección inicial o en las páginas de datos, están incluídas entodos los ostros índices. Estas listas de índices los conduce a la página y linea de aquella página donde se encuentra cada componente.

En la sección de Zona Interfacial la selección de parámetros difiere drásticamente para cada categoría; de tal manera que cada una tiene su propio formato. La categoría de convertidores analógicos a digitales tiene dos formatos: uno para componentes de salida binaria y otro para unidades decimales. Algunos de los productos en esta sección, principalmente convertidores analógico a digital y digital a analógico, pueden ser híbridos; los híbridos en la lista son solo aquellos de estilo constructivo compatible con CI*.

Esta sección no es complicada por referencias al estilo constructivo; los sufijos que denotan estilo constructivo han sido generalmente omitidos. Para información adicional sobre sufijos de las compañías, refiérase a la Guía de Número de Pieza. A lo largo de la Guía de Selección Maestra, cada intérvalo completo de temperatura para uso militar (55°C a 125°C) de la componente aparece indicada por el signo (†) que precede al nombre del fabricante. Los nombres de los fabricantes no son generalmente deletreados; sin embargo, algunos aparecen abreviados y las abrieviaturas son explicadas en la página 2809 .

インターフェイスへの案内

マスターセレクションガイドは製品の選択にとりかかるのには充分な情報を備えています。最初のセレクションガイド並にデータ掲載ページとこのマスターセレクションに記載されている製品は全てのインデックスにのっており，その製品のページ数と行数がそのインデックスですぐ分ります。

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パッケージ形状にはふれていません。それを表すサフィックスも除いています。各社のパッケージを探したい時はパーツナンバーガイドを参照して下さい。マスターセレクション全部にわたり，ミリタリー温度範囲の製品はそのメーカ名の前に(　)印がついています。メーカー名は簡略化していませんがしてある場合には2809 ページを参照して下さい。

INTERFACE–Analog Switches

Switches with Drivers

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source
SPST	CMOS	50	±11	±15,5	**IH5140M**	**† Intersil (3028)**
			±15	±15,5	**DG5040A**	**† Siliconix (3077)**
					DG5040C	**Siliconix (3077)**
		75	±10	±15,5	**IH5140C**	**Intersil (3028)**
			±11	±15,5	**HI5040-2**	**† Harris (2882)**
					HI5040-5	**Harris (2882)**
					IH5040M	**† Intersil (3021)**
		80	±10	±15,5	**IH5040C**	**Intersil (3021)**
	JFET	6	−5 to 10	±15	CAG6	† TeledyneC
			−5 to 4	±15,5	CAG10A	† TeledyneC
		10	−5 to 10	±15	CAG6-10	† TeledyneC
			−5 to 4	±15,5	CAG10C	† TeledyneC
		15	−10 to 5	±15,5	CAG10D	† TeledyneC
		30	±5	±5,5	CAG10	† TeledyneC
			±8	−18,12	IH5001	Intersil
		50	−10 to 4	±15,5	CAG10B	† TeledyneC
			−10 to 5	−15,5	CAG14	† TeledyneC
			±8	−18,12	IH5002	Intersil
			±10	±15	2110BE	† TeledyneC
		60	±10	±18,5	CAG30	† TeledyneC
		100	±5	±15	2107BE	† TeledyneC
	PMOS	80-300	±10	−20,10	TL610I	TI
					TL610M	† TI
		100-400	±10	−20,10	TL610C	TI
2xSPST	CMOS	35	±10	±15,5	**IH5048M**	**† Intersil (3021)**
		45	±10	±15,5	**IH5048C**	**Intersil (3021)**
		50	±7.5	±15.5	DGM181B	Intersil
			±10	±15.5	DGM182A	† Intersil
			±11	±15,5	**IH5141M**	**† Intersil (3028)**
			±15	±15	**HI300**	**Harris (2872)**
					HI304	**Harris (2872)**
					HI381	**Harris (2877)**
					DG300A	**† Siliconix (3077)**
					DG300AA	**† Siliconix (3077)**
					DG300AB	**Siliconix (3077)**
					DG300AC	**Siliconix (3077)**
					DG300B	**Siliconix (3077)**
					DG300C	**Siliconix (3077)**
					DG304A	**† Siliconix (3077)**
					DG304AA	**† Siliconix (3077)**
					DG304AB	**Siliconix (3077)**
					DG304AC	**Siliconix (3077)**
					DG304B	**Siliconix (3077)**
					DG304C	**Siliconix (3077)**
					DG381A	**† Siliconix (3077)**
					DG381AA	**† Siliconix (3077)**
					DG381AB	**Siliconix (3077)**
					DG381AC	**Siliconix (3077)**
					DG381B	**† Siliconix (3077)**
					DG381C	**† Siliconix (3077)**
				±15,5	**HI5048-2**	**† Harris (2882)**
					HI5048-5	**Harris (2882)**
					DG5041A	**† Siliconix (3077)**
					DG5041C	**Siliconix (3077)**
		70	±14	±15	**DG200M**	**† Intersil (3031)**
					IH5200	**† Intersil (3031)**
			±15	±15	ADG200A	† AD
					HI200-2	**† Harris (2866)**
					MP200DIA	**MicroPwr (3047)**
					DG200A	**† Siliconix (3077)**
					DG200AA	**† Siliconix (3077)**
		75	±10	±15,5	DGM182B	Intersil
					IH5141C	**Intersil (3028)**
			±11	±15,5	**DG200**	**Intersil (3031)**

(Continued)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source
2xSPST	CMOS	75	±11	±15,5		(Cont'd)
					IH200M	† Intersil
					IH5041M	**† Intersil (3021)**
			±15	±15,5	**HI5041-2**	**† Harris (2882)**
					HI5041-5	**Harris (2882)**
		80	±10	±15,5	IH200C	Intersil
					IH5041C	**Intersil (3021)**
			±14	±15	**DG200C**	**Intersil (3031)**
					IH5200C	**Intersil (3031)**
			±15	±15	ADG200B	AD
					ADG200C	AD
					HI200-5	**Harris (2866)**
					MP200DIB	**MicroPwr (3047)**
					MP200DIC	**MicroPwr (3047)**
					DG200AB	**Siliconix (3077)**
					DG200AC	**Siliconix (3077)**
					DG200B	**Siliconix (3077)**
					DG200C	**Siliconix (3077)**
		90	±15	±15	AD7592DIB	AD
					AD7592DIK	AD
	JFET	6	−6 to 10	−18,15	CAG27	† TeledyneC
		10	−6 to 10	−18,15	CAG27-10	† TeledyneC
			−7.5 to 15	±15,5	DG180A	† Intersil
					DG180B	Intersil
					DG180A	**† Siliconix (3077)**
					DG180B	**Siliconix (3077)**
			±10	−18,12	DG141A	† Intersil
					IH5005	† Intersil
					AH0141	† National
					AH0141C	National
					DG141A	**† Siliconix (3077)**
				−20,10,5	DG180A	† Intersil
					DG180B	Intersil
					DG180A	† Siliconix
					DG180B	Siliconix
		15	±7.5	±15	DG151A	† Intersil
					AH0151	† National
					AH0151C	National
					DG151A	**† Siliconix (3077)**
			±8	−18,12	DG141B	Intersil
					DG441A	Intersil
					DG141B	**Siliconix (3077)**
		20	±5.5	±15	DG151B	Intersil
					DG451A	Intersil
					DG151B	**Siliconix (3077)**
		30	−6 to 10	−18,15	CAG24	† TeledyneC
			−7.5 to 15	±15,5	DG181A	† Intersil
					IH181M	† Intersil
					AM181	† National
					DG181A	**† Siliconix (3077)**
			−12.5 to 10	−20,10,5	DG181A	† Intersil
					IH181M	† Intersil
					AM181	† National
					DG181A	† Siliconix
			±10	−18,12	DG133A	† Intersil
					IH5003	† Intersil
					IH5006	† Intersil
					AH0133	† National
					AH0133C	National
					DG133A	**† Siliconix (3077)**
				−20	CDA2-3	† TeledyneC
		35	±8	−18,12	DG433A	† Intersil
		50	−7.5 to 15	±15,5	DG181B	Intersil
					IH181C	Intersil
					DG181B	**Siliconix (3077)**

(Continued)

DT' means four terminals with a pair of normally open and normally closed contacts.

INTERFACE–Analog Switches (Cont'd)

Switches with Drivers (Cont'd)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source	
2xSPST	JFET	50					(Cont'd)
			−10 to 15	±15,5	AM281	National	
			−12.5 to 10	−20,10,5	DG181B	Intersil	
					IH181C	Intersil	
					DG181B	Siliconix	
			−15 to 10	−20,10,5	AM281	National	
			±7.5	±15	DG152A	† Intersil	
					AH0152	† National	
					AH0152C	National	
					DG152A	**† Siliconix**	**(3077)**
			±8	−18,12	DG133B	Intersil	
					DG133B	**Siliconix**	**(3077)**
			±10	−18,12	IH5004	Intersil	
				−18,15	CAG13	† TeledyneC	
					CAG42	† TeledyneC	
					CAG45A	† TeledyneC	
		75	−7.5 to 15	±15,5	AM182	† National	
			−10 to 15	±15,5	DG182A	† Intersil	
					IH182M	† Intersil	
					DG182A	**† Siliconix**	**(3077)**
			−12.5 to 10	−20,10,5	AM182	† National	
			−15 to 10	−20,10,5	DG182A	† Intersil	
					IH182M	† Intersil	
					AM281	National	
					DG182A	† Siliconix	
			±10	±15	SW-05B	† PMI	
					TL182M	† TI	
		80	±8	−18,12	DG434A	Intersil	
			±10	−18,12	DG134A	† Intersil	
					IH5007	Intersil	
					AH0134	† National	
					AH0134C	National	
					DG134A	**† Siliconix**	**(3077)**
				±15	SW-05F	PMI	
					SW-05G	PMI	
		100	−10 to 15	±15,5	DG182B	Intersil	
					IH182C	Intersil	
					AM282	National	
					DG182B	**Siliconix**	**(3077)**
			−15 to 10	−20,10,5	DG182B	Intersil	
					IH182C	Intersil	
					AM282	National	
					DG182B	Siliconix	
			±5.5	±15	DG452A	Intersil	
					DG152B	**Siliconix**	**(3077)**
			±8	−18,12	DG134B	Intersil	
					DG134B	**Siliconix**	**(3077)**
			±10	±15,5	TL182C	TI	
					TL182I	TI	
		300	−7.5 to 15	±15,5	**DG281A**	**† Siliconix**	**(3077)**
					DG281B	**Siliconix**	**(3077)**
	PMOS	75-200	−5 to 10	±15,5	**DGM111A**	**† Siliconix**	**(3077)**
			±10	−20,10,5	DGM111A	† Siliconix	
		75-250	−5 to 10	±15,5	**DGM111B**	**Siliconix**	**(3077)**
			±10	−20,10,5	DGM111B	Siliconix	
		100-450	±10	−20,10,5	DG111	† Intersil	
					DG112	† Intersil	
4xSPST Common Output							
	PMOS	100-450	±10	−20,10	DG116	† Intersil	
				−20,10,5	DG118	† Intersil	
							(Continued)
4xSPST Common Output	PMOS						(Cont'd)
		150-450	±10	−20,10,5	**DG172A**	**† Siliconix**	**(3077)**
		150-500	±10	−20,10,5	**DG172B**	**Siliconix**	**(3077)**
		200-600	±10	−20,10,5	**DG172C**	**Siliconix**	**(3077)**
4xSPST Var. Comb. of Normally On/Off, with Disable							
	FET	85	±10	±15	SW03B	† PMI	
					SW03F	PMI	
					SW04B	† PMI	
					SW04F	PMI	
4xSPST Various Combinations of Normally On/Off							
	FET	80 *	±10	±15	SW-201B	† PMI	
					SW-202B	† PMI	
		85	±10	±15	SW01B	† PMI	
					SW01F	PMI	
					SW02B	† PMI	
					SW02F	PMI	
		100	±10	±15	SW-201F	PMI	
					SW-202F	PMI	
	JFET	100	±10	−18,15	CAG48A	† TeledyneC	
		200	±10	±15,0	LF11201	† National	
					LF11202	† National	
					LF11331	† National	
					LF11332	† National	
					LF11333	† National	
		250	±10	±15,0	LF13201	National	
					LF13202	National	
					LF13331	National	
					LF13332	National	
					LF13333	National	
	PMOS	200-600	±10	−20,10,5	AH0015	† National	
					AH0015C	National	
4xSPST	CMOS	50	±15	±15	**HI201HS-2**	**† Harris**	**(2868)**
					HI201HS-5	**Harris**	**(2868)**
		75	±11	±15,5	IH201M	† Intersil	
					IH202M	† Intersil	
					IH5052M	† Intersil	
					IH5053M	† Intersil	
		80	±10	±15	**MP201DIA**	**† MicroPwr**	**(3047)**
					MP201DIB	**MicroPwr**	**(3047)**
				±15,5	IH201C	Intersil	
					IH202C	Intersil	
					IH5052C	Intersil	
					IH5053C	Intersil	
			±14	±15	DG201M	† Intersil	
					IH5201M	† Intersil	
			±15	±15	ADG201A	† AD	
					HI201-2	**† Harris**	**(2868)**
		90	±15	±15	AD7590DIB	AD	
					AD7590DIK	AD	
					AD7591DIB	AD	
					AD7591DIK	AD	
					DG221A	**† Siliconix**	**(3077)**
					DG221C	**Siliconix**	**(3077)**
		100	±14	±15	DG201C	Intersil	
					IH5201C	Intersil	
			±15	±15	AD7510DIJ	AD	
					AD7510DIK	AD	
					AD7510DIS	† AD	
					AD7511DIJ	AD	
					AD7511DIK	AD	
					AD7511DIS	† AD	
					AD7511DIT	† AD	
					ADG201B	AD	
					ADG201C	AD	
					HI201-5	**Harris**	**(2868)**
					MP7510DIJ	**MicroPwr**	**(3047)**
					MP7510DIK	**MicroPwr**	**(3047)**
							(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Analog Switches (Cont'd)

Switches with Drivers (Cont'd)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source
4xSPST	CMOS	100	±15	±15		(Cont'd)
					MP7510DIS	† MicroPwr (3047)
					MP7511DIJ	MicroPwr (3047)
					MP7511DIK	MicroPwr (3047)
					MP7511DIS	† MicroPwr (3047)
					MP7511DIT	† MicroPwr (3047)
					DG308A	† Siliconix (3077)
					DG308C	Siliconix (3077)
					DG309A	† Siliconix (3077)
					DG309C	Siliconix (3077)
		175	±15	±15	DG201A	† Siliconix (3077)
					DG201AA	† Siliconix (3077)
					DG202A	† Siliconix (3077)
					DG202B	Siliconix (3077)
					DG211C	Siliconix (3077)
					DG212C	Siliconix (3077)
		200	±15	±15	DG201AB	† Siliconix (3077)
					DG201AC	† Siliconix (3077)
					DG201AHSA	† Siliconix (3077)
					DG201AHSB	Siliconix (3077)
					DG201AHSC	Siliconix (3077)
					DG201B	Siliconix (3077)
					DG201C	Siliconix (3077)
					DG202C	Siliconix (3077)
		280	±7.5	±7.5	F4066BC	Fairchild
					F4066BM	† Fairchild
					HD14066B	Hitachi
					MC14066BA	† Motorola
					MC14066BC	Motorola
					MC54HC4066	† Motorola
					MC74HC4066	Motorola
					CD4066BC	National
					CD4066BM	† National
					MN4066B	† Panasonic (828)
					MN74HC4066	Panasonic (831)
					CD4066A	† RCA (840)
					CD4066AE	RCA (840)
					CD4066B	† RCA (840)
					CD4066BE	RCA (840)
					CD74HC4066	RCA (843)
					HCC4066B	† SGS
					HCF4066B	SGS
					HEF4066B	Signetics (864,898)
					HEF4066BD	† Signetics (864)
					N4066A	Signetics
					883/4066B	† SSS
					SCL4066B	SSS
					TC4066B	Toshiba
		400	±7.5	±7.5	HD14016B	Hitachi
					MC14016BA	† Motorola
					MC14016BC	Motorola
					883/4016B	† SSS
					SCL4016B	SSS
					CM4016A	† Solitron
					CM4016AE	Solitron
					TC4016B	Toshiba
		800	±7.5	±7.5	F4016C	Fairchild
					F4016M	† Fairchild
		850	Inverted Control	±7.5		
				±7.5	883/4416B	† SSS
					SCL4416B	SSS
			±7.5	±7.5	MC54HC4016	† Motorola
					MC54HC4316	† Motorola
					MC74HC4016	Motorola
					MC74HC4316	Motorola
					CD4016BC	National
					CD4016BM	† National
						(Continued)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source
4xSPST	CMOS	850	±7.5	±7.5		(Cont'd)
					MN4016B	† Panasonic (828,834)
					CD4016A	† RCA (839,840)
					CD4016AE	RCA (839,840)
					CD4016B	† RCA (839,840)
					CD4016BE	RCA (839,840)
					HCC4016B	† SGS
					HCF4016B	SGS
					HEF4016	† Signetics (864)
					CM4016A	† Solitron
					CM4016AE	Solitron
					CM4116A	† Solitron
					CM4116AE	Solitron
	DMOS	70	±7.5	±15	SD5001	Siliconix (3080)
					SD5002	Siliconix (3080)
			±10	±15	SD5000	Siliconix (3080)
			±15	±15	SD5200	Siliconix (3080)
	JFET	10	±10	−18,2.8	CAM604A	† TeledyneC
		30	±7.5	±15,5	AM193	National
		50	−10 to 5	−15,5	CAG49	† TeledyneC
			±10	±18,−7	CAG50	† TeledyneC
		60	±10	−18,5	CAG49	† TeledyneC
		75	±10	±15	SW-7510A	† PMI
					SW-7510B	† PMI
					SW-7510E	PMI
					SW-7510F	PMI
					SW-7511A	† PMI
					SW-7511B	† PMI
					SW-7511E	PMI
					SW-7511F	PMI
				±15,5	AM194	National
5xSPST Common Output	PMOS	100-450	±10	−20,10	DG123	† Intersil
					DG123A	† Siliconix
				−20,10,5	DG125	† Intersil
					DG125A	† Siliconix (3078)
		125-500	±10	−20,10	DG123B	Intersil
					DG123B	Siliconix
				−20,10,5	DG125B	Intersil
					DG125B	Siliconix (3078)
SPDT for D/A	NPN-PNP	10	0 to -10	−15	CDA1-3	† TeledyneC
			10	10	CDA4A	† TeledyneC
			±10	−15,5	CDA23	† TeledyneC
				±15	CDA6	† TeledyneC
SPDT[1]	CMOS	35	±10	±15,5	IH5050M	† Intersil (3021)
		45	±10	±15,5	IH5050C	Intersil (3021)
		50	±11	±15,5	IH5142M	† Intersil (3028)
			±15	±15	HI301	Harris (2872)
					HI305	Harris (2872)
					HI387	Harris (2877)
					DG301AA	† Siliconix (3078)
					DG301AB	Siliconix (3078)
					DG301AC	Siliconix (3078)
					DG305AA	† Siliconix (3078)
					DG305AB	Siliconix (3078)
					DG305AC	Siliconix (3078)
					DG387AA	† Siliconix (3078)
					DG387AB	Siliconix (3078)
					DG387AC	Siliconix (3078)
				±15,5	HI5050-2	† Harris (2882)
					HI5050-5	Harris (2882)
					DG5042A	† Siliconix (3078)
					DG5042C	Siliconix (3078)
		75	±10	±15,5	IH5142C	Intersil (3028)
						(Continued)

DT[1] means four terminals with a pair of normally open and normally closed contacts.

INTERFACE-Analog Switches (Cont'd)

Switches with Drivers (Cont'd)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source	Line
SPDT[1]	CMOS	75				(Cont'd)	
			±11	±15,5	**IH5042M**	**† Intersil (3021)**	
			±15	±15,5	**HI5042-2**	**† Harris (2882)**	
					HI5042-5	**Harris (2882)**	
		80	±10	±15,5	**IH5042C**	**Intersil (3021)**	
	JFET	6	−5 to 10	±15	CAG7	† TeledyneC	5
		10	−5 to 10	±15	CAG7-10	† TeledyneC	
			−7.5 to 15	±15,5	DG186A	† Intersil	
					DG186B	Intersil	
					DG186A	**† Siliconix (3078)**	
					DG186B	**Siliconix (3078)**	10
			−12.5 to 10	−20,10,5	DG186A	† Intersil	
					DG186B	Intersil	
					DG186A	† Siliconix	
					DG186B	Siliconix	
			±10	±18,12	DG146A	† Intersil	15
					AH0146	† National	
					AH0146C	National	
					DG146A	**Siliconix (3078)**	
		15	±7.5	±15	DG161A	† Intersil	
					AH0161	† National	20
					AH0161C	National	
					DG161A	**Siliconix (3078)**	
			±8	±18,12	DG146B	Intersil	
					DG446A	Intersil	
					DG146B	**Siliconix (3078)**	25
		20	±5.5	±15	DG461A	Intersil	
					DG161B	**Siliconix (3078)**	
		30	−7.5 to 15	±15,5	DG187A	† Intersil	
					IH187M	† Intersil	
					AM187	† National	30
					DG187A	**† Siliconix (3078)**	
			−12.5 to 10	−20,10,5	DG187A	† Intersil	
					IH187M	† Intersil	
					AM187	† National	
					DG187A	† Siliconix	35
			±10	±18,12	DG144A	† Intersil	
					AH0144	† National	
					AH0144C	National	
					DG144A	**† Siliconix (3078)**	
		35	±8	±8,12	DG444A	Intersil	40
		50	−7.5 to 15	±15,5	DG187B	Intersil	
					IH187C	Intersil	
					DG187B	**Siliconix (3078)**	
			−10 to 15	±15,5	AM287	National	
			−12.5 to 10	−20,10,5	DG187B	Intersil	45
					IH187C	Intersil	
					DG187B	Siliconix	
			−15 to 10	−20,10,5	AM287	National	
			±7.5	±15	DG162A	† Intersil	
					AH0162	† National	50
					AH0162C	National	
					DG162A	**† Siliconix (3078)**	
			±8	±15	2126BG	† TeledyneC	
				±18,12	DG144B	Intersil	
					DG144B	**Siliconix (3078)**	55
		75	−7.5 to 15	±15,5	AM188	† National	
			−10 to 15	±15,5	DG188A	† Intersil	
					IH188M	† Intersil	
					DG188A	**† Siliconix (3078)**	
						(Continued)	
SPDT[1]	JFET	75				(Cont'd)	
			−12.5 to 10	−20,10,5	AM188	† National	60
			−15 to 10	−20,10,5	DG188A	† Intersil	
					IH188M	† Intersil	
					DG188A	† Siliconix	
			±10	±15,5	TL188M	† TI	
		80	±8	±18,12	DG443A	Intersil	65
			±10	−18,12	DG143	† Intersil	
					AH0143	† National	
					AH0143C	National	
					DG143A	**† Siliconix (3078)**	
		100	−10 to 15	±15,5	DG188B	Intersil	70
					IH188C	Intersil	
					AM288	National	
					DG188B	**Siliconix (3078)**	
			−15 to 10	−20,10,5	DG188B	Intersil	
					IH188C	Intersil	75
					AM288	National	
					DG188B	Siliconix	
			±5.5	±15	**DG162B**	**Siliconix (3078)**	
			±8	±15	DG462A	Intersil	
			±10	−18,12	**DG143B**	**Siliconix (3078)**	80
				±15	AH2114	† National	
				±15,5	TL188C	TI	
					TL188I	TI	
		125	±10	±15	AH2114C	National	
		300	−7.5 to 15	±15,5	**DG287A**	**† Siliconix (3078)**	85
					DG287B	**Siliconix (3078)**	
	NPN-PNP	10	±10	−15,5	CDA23	† TeledyneC	
	PMOS	100-400	±10	−20,10	TL604I	TI	
					TL604M	† TI	
		200-600	±10	−20,10	TL604C	TI	90
SPDT	JFET	50	−10 to 5	−15,5	CDA18	† TeledyneC	
	PMOS	100-400	±10	−20,10	TL601I	TI	
					TL601M	† TI	
					TL607I	TI	
					TL607M	† TI	95
		200-600	±10	−20,10	TL601C	TI	
					TL607C	TI	
2xSPDT[1]	CMOS	35	±10	±15,5	**IH5051M**	**† Intersil (3021)**	
		45	±10	±15,5	**IH5051C**	**Intersil (3021)**	
		50	±11	±15,5	**IH5143M**	**† Intersil (3028)**	100
			±15	±15	**HI303**	**Harris (2872)**	
					HI307	**Harris (2872)**	
					HI390	**Harris (2877)**	
					DG303AA	**† Siliconix (3078)**	
					DG303AB	**Siliconix (3078)**	105
					DG303AC	**Siliconix (3078)**	
					DG307AA	**† Siliconix (3078)**	
					DG307AB	**Siliconix (3078)**	
					DG307AC	**Siliconix (3078)**	
					DG390AA	**† Siliconix (3078)**	110
					DG390AB	**Siliconix (3078)**	
					DG390AC	**Siliconix (3078)**	
				±15,5	**HI5051-2**	**† Harris (2882)**	
					HI5051-5	**Harris (2882)**	
					DG243A	**† Siliconix (3078)**	115
					DG243C	**Siliconix (3078)**	
					DG5043A	**† Siliconix (3078)**	
					DG5043C	**Siliconix (3078)**	
		75	±10	±15,5	**IH5143C**	**Intersil (3028)**	
			±11	±15,5	**IH5043M**	**† Intersil (3021)**	120
			±15	±15,5	**HI5043-2**	**† Harris (2882)**	
					HI5043-5	**Harris (2882)**	
						(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Analog Switches (Cont'd)

Switches with Drivers (Cont'd)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source	Line
2xSPDT ¹	CMOS					(Cont'd)	
		80	± 10	± 15,5	**IH5043C**	**Intersil** (3021)	
		100	± 15	± 15	AD7512DIJ	AD	
					AD7512DIK	AD	
					AD7512DIS	† AD	
					AD7512DIT	† AD	5
					MP7512DIJ	**MicroPwr** (3047)	
					MP7512DIK	**MicroPwr** (3047)	
					MP7512DIS	**† MicroPwr** (3047)	
					MP7512DIT	**† MicroPwr** (3047)	
	JFET	10	− 7.5 to 15	± 15,5	DG189A	† Intersil	10
					DG189B	Intersil	
					DG189A	**† Siliconix** (3078)	
					DG189B	**Siliconix** (3078)	
			− 12.5 to 15	− 20,15,5	DG189A	† Intersil	
					DG189B	Intersil	15
					DG189A	† Siliconix	
					DG189B	Siliconix	
		30	− 7.5 to 15	± 15,5	DG190A	† Intersil	
					DG190B	Intersil	
					IH190M	† Intersil	20
					AM190	† National	
					DG190A	**† Siliconix** (3078)	
			− 12 to 15	− 20,15,5	DG190A	† Intersil	
					DG190B	Intersil	
					IH190M	† Intersil	25
					AM190	† National	
					DG190A	† Siliconix	
		50	− 7.5 to 15	± 15,5	**DG190B**	**Siliconix** (3078)	
			− 10 to 15	± 15,5	AM290	National	
			− 12.5 to 15	− 20,10,5	DG190B	Siliconix	30
			− 15 to 10	− 20,10,5	AM290	National	
		75	− 7.5 to 15	± 15,5	AM191	† National	
			− 10 to 15	± 15,5	DG191A	† Intersil	
					IH191M	† Intersil	
					DG191A	**† Siliconix** (3078)	35
			− 12.5 to 15	− 20,10,5	AM191	† National	
			− 15 to 10	− 20,10,5	DG191A	† Intersil	
					IH191M	† Intersil	
					DG191A	† Siliconix	
		100	− 10 to 15	± 15,5	DG191B	Intersil	40
					IH191C	Intersil	
					AM291	National	
					DG191B	**Siliconix** (3078)	
			− 15 to 10	− 20,10,5	DG191B	Intersil	
					IH191C	Intersil	45
					AM291	National	
					DG191B	Siliconix	
		125	± 10	± 15,5	TL191M	† TI	
		150	± 10	± 15,5	TL191C	TI	
					TL191I	TI	50
		300	− 7.5 to 15	± 15,5	**DG290A**	**† Siliconix** (3078)	
					DG290B	**Siliconix** (3078)	
	PNP	10	± 10	± 15	CDA29A	† TeledyneC	
3xSPDT	CMOS	280	±7.5	±7.5	F4053BC	Fairchild	
					F4053BM	† Fairchild	55
					HD14053B	Hitachi	
					MC14053BA	† Motorola	
					MC14053BC	Motorola	
					MC54HC4053	† Motorola	
					MC54HC4335	† Motorola	60
					MC74HC4053	Motorola	
						(Continued)	
3xSPDT	CMOS	280	± 7.5	± 7.5		(Cont'd)	
					MC74HC4353	Motorola	
					CD4053BC	National	
					CD4053BM	† National	
					MN4053B	**† Panasonic** (828)	65
					MN74HC4053	**Panasonic** (831)	
					CD4053B	**† RCA** (839)	
					CD4053BE	**RCA** (839)	
					CD74HC4053	**RCA** (843)	
					HCC4053B	† SGS	70
					HCF4053B	SGS	
					HEF4053B	**Signetics** (864,898)	
					HEF4053BD	**† Signetics** (864)	
					883/4053B	† SSS	
					SCL4053B	SSS	75
					CM4053A	† Solitron	
					CM4053AE	Solitron	
					TC4053B	Toshiba	
4xSPDT for D/A (current switch)	NPN	—	− 10 to -3	± 15	ULN-2140A	Sprague	
					ULS-2140H	† Sprague	80
4xSPDT for D/A	CMOS	100	0.1	8	AD7519J	AD	
4xSPDT	CMOS	—	—	8	MC14551BA	† Motorola	
					MC14551BC	Motorola	
	JFET	35	± 10	− 15,5	HCS310	HyComp	
	NMOS	—	—	8	**DG515A**	**† Siliconix** (3082)	85
					DG515B	**Siliconix** (3082)	
					DG515C	**Siliconix** (3082)	
	PNP	7	0 to -10	− 15	CDA11-S12	TeledyneC	
		10	0 to -10	− 15	CDA11	TeledyneC	
10xSPDT for D/A	NMOS	—	—	8	**DG516A**	**† Siliconix** (3082)	90
					DG516B	**Siliconix** (3082)	
					DG516C	**Siliconix** (3082)	
DPST	CMOS	50	± 15	± 15	**DG384AA**	**† Siliconix** (3079)	
					DG384AB	**Siliconix** (3079)	
					DG384AC	**Siliconix** (3079)	95
		75	± 11	± 15,5	**IH5044M**	**† Intersil** (3021)	
					IH5144C	**Intersil** (3028)	
					IH5144M	**† Intersil** (3028)	
					DG5044A	**† Siliconix** (3079)	
					DG5044C	**Siliconix** (3079)	100
			± 15	± 15,5	**HI5044-2**	**† Harris** (2882)	
					HI5044-5	**Harris** (2882)	
		80	± 10	± 15,5	**IH5044C**	**Intersil** (3021)	
					IH5044M	† Intersil	
2xDPST Common Output	PMOS	100-450	± 10	− 20,10,5	DGM122A	† Siliconix	105
		125-500	± 10	− 20,10,5	DGM122B	Siliconix	
		200-600	± 10	− 20,10,5	AH0019	† National	
					AH0019C	National	
2xDPST	CMOS	35	± 10	± 15,5	**IH5049M**	**† Intersil** (3021)	
		45	± 10	± 15,5	**IH5049C**	**Intersil** (3021)	110
		50	± 11	± 15,5	**IH5145M**	**† Intersil** (3028)	
			± 15	± 15	**HI302**	**Harris** (2872)	
					HI306	**Harris** (2872)	
					HI384	**Harris** (2877)	
					DG302A	**† Siliconix** (3079)	115
					DG302AA	**† Siliconix** (3079)	
					DG302AB	**Siliconix** (3079)	
					DG302AC	**Siliconix** (3079)	
					DG302B	**Siliconix** (3079)	
					DG302C	**Siliconix** (3079)	120
					DG306AA	**† Siliconix** (3079)	
					DG306AB	**Siliconix** (3079)	
					DG306AC	**Siliconix** (3079)	
						(Continued)	

DT¹ means four terminals with a pair of normally open and normally closed contacts.

INTERFACE–Analog Switches (Cont'd)

Switches with Drivers (Cont'd)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source	Page
2xDPST	CMOS	50	± 15	± 15		(Cont'd)	
					DG384B	**Siliconix**	**(3079)**
					DG384C	**Siliconix**	**(3079)**
				± 15,5	**HI5049-2**	**† Harris**	**(2882)**
					HI5049-5	**Harris**	**(2882)**
					DG5045A	**† Siliconix**	**(3079)**
					DG5045C	**Siliconix**	**(3079)**
		75	± 10	± 15,5	**IH5145C**	**Intersil**	**(3028)**
			± 11	± 15,5	**IH5045M**	**† Intersil**	**(3021)**
			± 15	± 15,5	**HI5045-2**	**† Harris**	**(2882)**
					HI5045-5	**Harris**	**(2882)**
		80	± 10	± 15,5	**IH5045C**	**Intersil**	**(3021)**
	JFET	10	− 7.5 to 15	± 15,5	DG183A	† Intersil	
					DG183B	Intersil	
					DG183A	**† Siliconix**	**(3079)**
					DG183B	**Siliconix**	**(3079)**
			− 12.5 to 10	− 20,10,5	DG183A	† Intersil	
					DG183B	Intersil	
					DG183A	† Siliconix	
					DG183B	Siliconix	
			± 10	− 18,12	DG140A	† Intersil	
					AH0140	† National	
					AH0140C	National	
					DG140A	**† Siliconix**	**(3079)**
		15	± 7.5	± 15	DG153A	† Intersil	
					AH0153	† National	
					AH0153C	National	
					DG153A	**† Siliconix**	**(3079)**
			± 8	− 18,12	DG440A	Intersil	
					DG140B	**Siliconix**	**(3079)**
		20	± 5.5	± 15	DG153B	Intersil	
					DG453A	Intersil	
					DG153B	**Siliconix**	**(3079)**
		30	− 7.5 to 15	± 15,5	DG184A	† Intersil	
					IH184M	† Intersil	
					AM184	† National	
					DG184A	**† Siliconix**	**(3079)**
			− 12.5 to 10	− 20,10,5	DG184A	† Intersil	
					IH184M	† Intersil	
					AM184	† National	
					DG184A	† Siliconix	
			± 10	− 18,12	DG129A	† Intersil	
					AH0129	† National	
					AH0129C	National	
					DG129A	**† Siliconix**	**(3079)**
		35	± 8	− 18,12	DG429A	Intersil	
		50	− 7.5 to 15	± 15,5	DG184B	Intersil	
					IH184C	Intersil	
					DG184B	**Siliconix**	**(3079)**
			− 10 to 15	± 15,5	AM284	National	
			− 12.5 to 10	− 20,10,5	DG184B	Intersil	
					IH184C	Intersil	
					DG184B	Siliconix	
			− 15 to 10	− 20,10,5	AM284	National	
			± 7.5	± 15	DG154A	† Intersil	
					AH0154	† National	
					AH0154C	National	
					DG154A	**† Siliconix**	**(3079)**
			± 8	− 18,12	**DG129B**	**Siliconix**	**(3079)**
		60	± 10	− 18,15	CS4R101A	† TeledyneC	
		75	− 7.5 to 15	± 15,5	AM185	† National	
			− 10 to 15	± 15,5	DG185A	† Intersil	

(Continued)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source	Page
2xDPST	JFET	75	− 10 to 15	± 15,5		(Cont'd)	
					IH185M	† Intersil	
					DG185A	**† Siliconix**	**(3079)**
			− 12.5 to 10	− 20,10,5	AM185	† National	
			− 15 to 10	− 20,10,5	DG185A	† Intersil	
					IH185M	† Intersil	
					DG185A	† Siliconix	
		80	± 8	− 18,12	DG426A	Intersil	
			± 10	− 18,12	DG126A	† Intersil	
					AH0126	† National	
					AH0126C	National	
					DG126A	**† Siliconix**	**(3079)**
		100	− 10 to 15	± 15,5	DG185B	Intersil	
					IH185C	Intersil	
					AM285	National	
					DG185B	**Siliconix**	**(3079)**
			− 15 to 10	− 20,10,5	DG185B	Intersil	
					IH185C	Intersil	
					AM285	National	
					DG185B	Siliconix	
			± 5.5	± 15	DG154B	Intersil	
					DG454A	Intersil	
					DG154B	**Siliconix**	**(3079)**
			± 8	− 18,12	**DG126B**	**Siliconix**	**(3079)**
		125	± 10	± 15,5	TL185M	† TI	
		150	± 10	± 15,5	TL185C	TI	
					TL185I	TI	
		300	− 7.5 to 15	± 15,5	**DG284A**	**† Siliconix**	**(3079)**
					DG284B	**Siliconix**	**(3079)**
3xDPST Common Output	PMOS	100-450	± 10	− 20,10	DG120	† Intersil	
				− 20,10,5	DG121	† Intersil	
DPDT ¹	CMOS	50	± 15	± 15,5	**HI5046A-2**	**† Harris**	**(2882)**
					HI5046A-5	**Harris**	**(2882)**
		75	± 11	± 15,5	**IH5046M**	**† Intersil**	**(3021)**
			± 15	± 15,5	**HI5046-2**	**† Harris**	**(2882)**
					HI5046-5	**Harris**	**(2882)**
		80	± 10	± 15,5	**IH5046C**	**Intersil**	**(3021)**
	JFET	10	± 10	− 18,12	DG145A	† Intersil	
					AH0145	† National	
					AH0145C	National	
					DG145A	**† Siliconix**	**(3079)**
		15	± 7.5	± 15	DG163A	† Intersil	
					AH0163	† National	
					AH0163C	National	
					DG163A	**† Siliconix**	**(3079)**
			± 8	− 18,12	DG445A	Intersil	
					DG145B	**Siliconix**	**(3079)**
		20	± 5.5	± 15	DG163B	Intersil	
					DG463A	Intersil	
					DG163B	**Siliconix**	**(3079)**
		30	± 10	− 18,12	DG139A	† Intersil	
					AH0139	† National	
					AH0139C	National	
					DG139A	**† Siliconix**	**(3079)**
		35	± 8	− 18,12	DG439A	Intersil	
		50	± 7.5	± 15	DG164A	† Intersil	
					AH0164	† National	
					AH0164C	National	
					DG164A	**† Siliconix**	**(3079)**
			± 8	− 18,12	**DG139B**	**Siliconix**	**(3079)**
		80	± 8	− 18,12	DG442A	Intersil	
			± 10	− 18,12	DG142A	† Intersil	

(Continued)

† Military Temperature Range (− 55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Analog Switches (Cont'd)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source
Switches with Drivers						**(Cont'd)**
DPDT[1]	JFET	80	±10	−18,12		(Cont'd)
					AH0142	† National
					AH0142C	National
					DG142A	**† Siliconix (3079)**
		100	±5.5	±15	DG164B	Intersil
					DG464A	Intersil
					DG164B	**Siliconix (3079)**
			±10	−18,12	**DG142B**	**Siliconix (3079)**
DPDT	PMOS	200-600	±10	−20,10,5	AH0014	† National
					AH0014C	National
2xDPDT	PMOS	150-1000	0 to -18	−(5-21)	TDA1195	Siemens
DP4T with Followers					TDA1029	Signetics
4xSPST Var. Comb. of Normally On/Off, with Disable						
	FET	80	±10	±15	SW-06B	† PMI
		100	±10	±15	SW-06F	PMI
		150	±10	±15	SW-06G	PMI
4xSPST	FET	80	±10	±15	SW-201B	† PMI
					SW-202B	† PMI
		100	±10	±15	SW-201F	PMI
					SW-202F	PMI
		150	±10	±15	SW-201G	PMI
4PDT for D/A						
	PNP	10	±10	±15,5	CDA28A	† TeledyneC
4PST	CMOS	50	±15	±15,5	**HI5047A-2**	**† Harris (2882)**
					HI5047A-5	**Harris (2882)**
		75	±11	±15,5	**IH5047M**	**† Intersil (3021)**
			±15	±15,5	**HI5047-2**	**† Harris (2882)**
					HI5047-5	**Harris (2882)**
		80	±10	±15,5	**IH5047C**	**Intersil (3021)**
Switches without Drivers						
SPST	JFET	30	±10		AM1000	† National
		50	±15		AM1001	† National
		100	0 to (Drive-4)		IH5037C	Intersil
					IH5037M	† Intersil
			±0.2		IH5021C	† Intersil
					IH5021M	† Intersil
					IH5023C	Intersil
					IH5023M	† Intersil
			±10		AM1002	† National
		150	0 to (Drive-4)		IH5038C	Intersil
					IH5038M	† Intersil
			±0.2		IH5022C	Intersil
					IH5022M	† Intersil
					IH5024C	Intersil
					IH5024M	† Intersil
2xSPST Common Output						
	JFET	100	0 to (Drive-4)		IH5035C	Intersil
					IH5035M	† Intersil
			±0.2		IH5019C	Intersil
					IH5019M	† Intersil
		150	0 to (Drive-4)		IH5034C	Intersil
					IH5034M	† Intersil
			±0.2		IH5018C	Intersil
					IH5018M	† Intersil
2xSPST	JFET	100	0 to (Drive-4)		IH5033C	Intersil
					IH5033M	† Intersil
			±0.2		IH5017C	Intersil
					IH5017M	† Intersil
		150	0 to (Drive-4)		IH5036C	Intersil
					IH5036M	† Intersil
			±0.2		IH5020C	Intersil
					IH5020M	† Intersil
3xSPST Common Output						
	JFET	100	0 to (Drive-4)		IH5029C	Intersil
					IH5029M	† Intersil
			±0.2		IH5013C	Intersil
					IH5013M	† Intersil
		150	0 to (Drive-4)		IH5030C	Intersil
					IH5030M	† Intersil
			±0.2		IH5014C	Intersil
					IH5014M	† Intersil
3xSPST	JFET	100	0 to (Drive-4)		IH5031C	Intersil
					IH5031M	† Intersil
			±0.2		IH5015C	Intersil
					IH5015M	† Intersil
		150	0 to (Drive-4)		IH5032C	Intersil
					IH5032M	† Intersil
			±0.2		IH5016C	Intersil
					IH5016M	† Intersil
	PMOS	200-600			MM455	† Intersil
					MM555	Intersil
4xSPST Common Output						
	JFET	—			G129	Intersil
					G130	† Intersil
					G131	† Intersil
					G132	† Intersil
					G1350	Intersil
					G1360	Intersil
		100	0 to (Drive-4)		IH5025C	Intersil
					IH5025M	† Intersil
			±0.2		IH5009C	Intersil
					IH5009M	† Intersil
					AH5009C	National
					AM9709C	National
					AM97C09	National
		150	0 to (Drive-4)		IH5026C	Intersil
					IH5026M	† Intersil
			±0.2		IH5010C	Intersil
					IH5010M	† Intersil
					AH5010C	National
					AM9710C	National
					AM97C10C	National
	PMOS	—			G124	Intersil
					MM451	† Intersil
					MM551	Intersil
4xSPST Two Outputs						
	JFET	—			G123	Intersil
	PMOS	—			**G123A**	**† Siliconix (3080)**
					G123B	**Siliconix (3080)**
4xSPST	JFET	—			G125	† Intersil
					G126	† Intersil
					G127	† Intersil
					G128	† Intersil
					G1330	Intersil
					G1340	Intersil
		100	0 to (Drive-4)		IH5027C	Intersil
					IH5027M	† Intersil
			±0.2		IH5011C	Intersil
					IH5011M	† Intersil
					AH5011C	National
					AM9711C	National
					AM97C11C	National
		150	0 to (Drive-4)		IH5028C	Intersil
					IH5028M	† Intersil
			±0.2		IH5012C	Intersil
					IH5012M	† Intersil
					AH5012C	National
					AM9712C	National
					AM97C12C	National

(Continued)

DT[1] means four terminals with a pair of normally open and normally closed contacts.

INTERFACE–Analog Switches (Cont'd)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source	Page
Switches without Drivers						**(Cont'd)**	
4xSPST							(Cont'd)
	PMOS	200-600			MM452	† Intersil	
					MM552	Intersil	
5xSPST Common Output plus Output Switch	PMOS	—			G117A	† Intersil	
					G117B	Intersil	
					G117A	† Siliconix	
5xSPST Common Output	PMOS	—			G116A	† Intersil	
					G116B	Intersil	
					G116A	† Siliconix	
					G116B	Siliconix	
6xSPST Common Output	PMOS	—			G115A	† Intersil	
					G115B	Intersil	
					G118A	† Intersil	
					G118B	Intersil	
					AM2009	† National	
					AM2009C	National	
					G115A	**† Siliconix**	**(3080)**
					G115B	**Siliconix**	**(3080)**
					G118A	**† Siliconix**	**(3080)**
2xDPST Common Output	PMOS	—			MM450	† Intersil	
					MM550	Intersil	
					G122A	**† Siliconix**	**(3080)**
3xDPST Common Output	PMOS	—			G119A	† Intersil	
					G119B	Intersil	
					G119A	**† Siliconix**	**(3080)**
					G119B	**Siliconix**	**(3080)**
Drivers							
High Current Switch (to drive power transistor switches)					SG1629	† SiliconG	
					SG3629	SiliconG	
Pulse Width Modulator, Switch Driver					**PWM125**	**Siliconix**	**(3081)**
					PWM127	**Siliconix**	**(3081)**
					PWM25	**Siliconix**	**(3081)**
					PWM27	**Siliconix**	**(3081)**
2 Channel					D112C	Intersil	
					D112M	† Intersil	
					D113C	Intersil	
					D113M	† Intersil	
					D120C	Intersil	
					D120M	† Intersil	
					D121C	Intersil	
					D121M	† Intersil	
					D139A	† Siliconix	
					D139B	Siliconix	
					D139C	Siliconix	
4 Channel					D129	Intersil	
					D129A	**† Siliconix**	**(3080)**
					D129B	**Siliconix**	**(3080)**
					D469	**Siliconix**	**(3080)**
					SI7250	**Siliconix**	**(3080)**
6 Channel					D123C	Intersil	
					D123M	† Intersil	
					D125C	Intersil	
					D125M	† Intersil	
					D123A	† Siliconix	
					D123B	Siliconix	
					D125A	**† Siliconix**	**(3080)**
					D125B	**Siliconix**	**(3080)**
					CDR125A	† TeledyneC	

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source	Page
Multiplexers							
4 channel. See Switches 4xSPST							
Crosspoint Switches					**MC142100**	**Motorola**	**(3536)**
					MC145100	**Motorola**	**(3536)**
					MC3416	**Motorola**	**(3060)**
					RC4444	Raytheon	
					RM4444	† Raytheon	
					CD22100	**RCA**	**(840)**
					CD22101	**RCA**	**(840)**
					CD22102	**RCA**	**(840)**
					EFB7310	Thomson-CSF	
4 Channel Differential	CMOS	230	± 15	± 15	**MP7502S**	**† MicroPwr**	**(3047)**
					MP7509S	**† MicroPwr**	**(3047)**
		250	± 15	± 15	**MVD-409**	**Datel**	**(2864)**
					MVD-409M	**† Datel**	**(2864)**
		270	± 7.5	± 7.5	MC14529BA	† Motorola	
					MC14529BC	Motorola	
					CD4529BC	National	
					CD4529BM	† National	
		280	± 7.5	± 7.5	F4052BC	Fairchild	
					F4052BM	† Fairchild	
					HD14052B	Hitachi	
					MC14052BA	† Motorola	
					MC14052BC	Motorola	
					MC54HC4052	† Motorola	
					MC54HC4352	† Motorola	
					MC74HC4052	Motorola	
					MC74HC4352	Motorola	
					CD4052BC	National	
					CD4052BM	† National	
					MN4052B	**† Panasonic**	**(828)**
					MN74HC4052	**Panasonic**	**(831)**
					CD4052B	**† RCA**	**(839)**
					CD4052BE	**RCA**	**(839)**
					CD74HC4052	**RCA**	**(843)**
					HCC4052B	† SGS	
					HCF4052B	SGS	
					883/4052B	† SSS	
					SCL4052B	SSS	
					CM4052B	† Solitron	
					CM4052BE	Solitron	
					TC4052B	Toshiba	
		300	± 15	± 15	**AD7502J**	**AD**	**(2841)**
					AD7502K	**AD**	**(2841)**
					AD7502S	**† AD**	**(2841)**
					HI509-2	**† Harris**	**(2893)**
					HI509-5	**Harris**	**(2893)**
					IH6208M	**† Intersil**	**(3039)**
		320	± 15	± 15	**MP7502J**	**MicroPwr**	**(3047)**
					MP7502K	**MicroPwr**	**(3047)**
					MP7509J	**MicroPwr**	**(3047)**
					MP7509K	**MicroPwr**	**(3047)**
		350	± 15	± 15	**IH6208C**	**Intersil**	**(3039)**
		400	± 15	± 15	**HI1828A-2**	**† Harris**	**(2903)**
					HI1828A-5	**Harris**	**(2903)**
					DG506AA	**† Siliconix**	**(3082)**
					DG509AA	**† Siliconix**	**(3082)**
		450	± 15	± 15	**DG506AB**	**Siliconix**	**(3082)**
					DG506AC	**Siliconix**	**(3082)**
					DG509AB	**Siliconix**	**(3082)**
					DG509AC	**Siliconix**	**(3082)**
		750	± 15	± 15	**MPC801**	**Burr-Brown**	**(2850)**
		900	± 10	± 15	**HI539-2**	**† Harris**	**(2917)**
					HI539-5	**Harris**	**(2917)**
		1000	± 13	± 15	**IH5208M**	**† Intersil**	**(3032)**
		1200	± 13	± 15	**IH5208C**	**Intersil**	**(3032)**

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Analog to Digital Converters (Cont'd)

Bits Res.	Linearity Error ± LSB	Conversion Time ± ½ LSB µS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source
Binary Output																	**(Cont'd)**
8	1/2																(Cont'd)
		1	400	x										x		**TDC1002**	**TRW-LSI (3704)**
			1250	x	x			x						x	x	**ADC-825MC**	**Datel (2860)**
				x	x			x						x	x	**ADC-825MM**	**† Datel (2860)**
						x	x	x					x	x	x	**MN5825**	**† MicroNet (3043)**
		1 *	—	x				x					x			**AM6108**	**AMD (3303)**
			1000	x				x					x	x		**AM6148**	**AMD (3303)**
		1.2	1800			x	x						x			**HAS-0802**	**AD (2839)**
		1.5	1550	x		x	x						x	x	x	**MN5100**	**MicroNet (3043)**
				x		x	x						x	x	x	**MN5100H**	**† MicroNet (3043)**
		2.5	35 *	x							x			x		ADC0820B	National
			650	x	x			x					x	x		ADC541B-8	† HybridSys
				x	x			x					x	x		ADC541C-8	HybridSys
						x	x	x					x	x	x	ADC542B-8	† HybridSys
						x	x	x					x	x	x	ADC542C-8	HybridSys
			915			x							x	x	x	**MN5140**	**MicroNet (3043)**
						x							x	x	x	**MN5140H**	**† MicroNet (3043)**
					x								x	x	x	**MN5141**	**MicroNet (3043)**
					x								x	x	x	**MN5141H**	**† MicroNet (3043)**
					x								x	x	x	**MN5142**	**MicroNet (3043)**
					x								x	x	x	**MN5142H**	**† MicroNet (3043)**
				x									x	x	x	**MN5143**	**MicroNet (3043)**
				x									x	x	x	**MN5143H**	**† MicroNet (3043)**
			1000			x							x	x	x	**MN5130**	**MicroNet (3043)**
						x							x	x	x	**MN5130H**	**† MicroNet (3043)**
					x								x	x	x	**MN5131**	**MicroNet (3043)**
					x								x	x	x	**MN5131H**	**† MicroNet (3043)**
					x								x	x	x	**MN5132**	**MicroNet (3043)**
					x								x	x	x	**MN5132H**	**† MicroNet (3043)**
				x									x	x	x	**MN5133**	**MicroNet (3043)**
				x									x	x	x	**MN5133H**	**† MicroNet (3043)**
				x	x	x							x	x	x	**MN5150**	**MicroNet (3043)**
		2.8	650			x	x	x					x	x	x	HSADC82	HybridSys
			1000 *			x	x	x					x	x	x	ADC83A	Burr-Brown
		6	1000			x							x	x	x	**MN5120**	**MicroNet (3043)**
						x							x	x	x	**MN5120H**	**† MicroNet (3043)**
					x								x	x	x	**MN5121**	**MicroNet (3043)**
					x								x	x	x	**MN5121H**	**† MicroNet (3043)**
					x								x	x	x	**MN5122**	**MicroNet (3043)**
					x								x	x	x	**MN5122H**	**† MicroNet (3043)**
				x									x	x	x	**MN5123**	**MicroNet (3043)**
				x									x	x	x	**MN5123H**	**† MicroNet (3043)**
		8	—	x									x			ZN437E	Ferranti
				x	x								x			ZN437J	† Ferranti
		9	4	x						x	x				x	**TLC540**	**TI (541,3103)**
			125 *	x	x								x	x		ZN448E	Ferranti
				x	x								x	x		ZN448E-8E	Ferranti
				x	x								x	x		ZN448J	† Ferranti
		15	30	x	x		x						x			**AD7574B**	**AD (2838)**
				x	x		x						x			**AD7574K**	**AD (2838)**
				x	x		x						x			**AD7574T**	**† AD (2838)**
				x	x		x						x			**MP7574B**	**MicroPwr (3046)**
				x	x		x						x			**MP7574K**	**MicroPwr (3046)**
					x		x						x			**MP7574T**	**MicroPwr (3046)**
			125 *	x	x								x	x		ZN427E-8	Ferranti
				x	x								x	x		ZN427J-8	† Ferranti

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE-Analog to Digital Converters (Cont'd)

Binary Output (Cont'd)

Bits Res.	Linearity Error ±LSB	Conversion Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source	Line
8	1/2																(Cont'd)	
		17	300	x										x		NE5034	Signetics (3609)	
		30	—	x									x			AD673J	AD (2838)	
				x									x			AD673S	† AD (2838)	
		40	5 *	x	x									x	x	AD7570J	AD	
				x	x									x	x	MP7570J	MicroPwr (3046)	5
			10 *	x						x				x		ADC0844B	National (3537)	
			175 *	x	x								x	x		AD570J	AD (2838)	
				x	x								x	x		AD570S	† AD (2838)	
				x	x								x	x		MCE570J	MCE	
				x	x								x	x		MCE570S	† MCE	10
		60MHz	—	x	x		x							x		TDC1025	† TRW-LSI (3704,3705)	
		66.6	—	x												AD8581L	AD	
		80	10	x											x	ADC0831B	National	
				x											x	ADC0832B	National	
				x											x	ADC0833B	National	15
				x											x	ADC0834B	National	
				x											x	ADC0838B	National	
		100	15	x						x				x		ADC0808	National	
				x						x				x		ADC0816C	National	
			30	x						x				x		ADC0816	† National	20
				x						x				x		ADC0808	TI	
			70			x							x	x	x	ADC-830	Datel (2863)	
							x						x	x	x	MN5065	MicroNet (3043)	
							x						x	x	x	MN5065H	† MicroNet (3043)	
						x							x	x	x	MN5066	MicroNet (3043)	25
						x							x	x	x	MN5066H	† MicroNet (3043)	
			75							x					x	MB4052	Fujitsu	
		100 *	875	x										x		ADC0802	† Intersil (2993)	
				x										x		ADC0802C	Intersil (2993)	
				x										x		ADC0803	† Intersil (2993)	30
				x										x		ADC0803C	Intersil (2993)	
				x										x		ADC0802	† National	
				x										x		ADC0802C	National	
				x										x		ADC0803C	National	
		108 *	6.8	x						x				x		MK50808	Mostek	35
				x						x				x		MK50816	Mostek	
		300	15 *	x						x						TL530	TI	
				x												TL532	TI	
		1250 *	20 *	x	x									x		4140	TeledyneP	
				x	x									x		4143	TeledyneP	40
				x	x									x		4143-01	† TeledyneP	
		1800	20	x	x							x		x		ADC-EK8B	Datel (2862)	
			25	x								x		x		TSC8700	TeledyneS	
				x								x		x		TSC8703	TeledyneS	
			43	x										x		ADC-ET8BM	† Datel (2862)	45
			50	x										x		ADC-ET8BC	Datel (2862)	
	3/4	15	30	x	x		x						x			AD7574A	AD (2838)	
				x	x		x						x			AD7574J	AD (2838)	
				x	x		x						x			AD7574S	† AD (2838)	
				x	x		x						x			MP7574A	† MicroPwr (3046)	50
				x	x		x						x			MP7574J	MicroPwr (3046)	
				x	x		x						x			MP7574S	† MicroPwr (3046)	

(Continued)

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
CTC—Compl. 2's Compl.
Int. Ref.—Internal Reference
Mux. In—Multiplexed Inputs
S&H—Sample and Hold
Par. Out—Parallel Output
Ser. Out—Serial Output

INTERFACE–Analog to Digital Converters (Cont'd)

Binary Output (Cont'd)

Bits Res.	Linearity Error ± LSB	Conversion Time ± ½ LSB μS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source
8	3/4																(Cont'd)
		66.6	—	x												**AD7581K**	**AD (2838)**
		70	2.5 *	x						x				x		**SI520**	**Siliconix (3083)**
				x						x				x		TL520	TI
	1	1.5	75	x							x			x		ADC0820C	National
		2.5	1010		x										x	HS5131B	† HybridSys
					x										x	HS5131C	HybridSys
		9	—		x	x							x	x		ZN449E-8	DDC
					x	x							x	x		ZN449J-8	† DDC
			125	x	x								x	x		**ADC-847A**	**Datel (2863)**
			125 *	x	x								x	x		ZN449E	Ferranti
				x	x								x	x		ZN449J	† Ferranti
		18	4	x						x	x				x	**TLC541**	**TI (541,3103)**
		32	12.5	x						x					x	ADC0831C	National
				x						x					x	ADC0832C	National
				x						x					x	ADC0833C	National
				x						x					x	ADC0834C	National
				x						x					x	ADC0838C	National
		40	12.5	x						x				x		ADC0844B	National
		100	2.5 *	x						x				x		TL521	TI
			15	x						x				x		ADC0809C	National
				x						x				x		ADC0817	National
		100 *	12.5	x										x		**ADC0804**	**† Intersil (2993)**
				x										x		**ADC0804C**	**Intersil (2993)**
				x										x		ADC0804C	National
		110	12.5	x										x		ADC0805C	National
				x										x		ADC0804C	TI
		112 *	15	x						x					x	μPD7001	NEC
		300	15 *	x						x						TL531	TI
				x												TL533	TI
		2000	6.5 *	x									x		x	TC5091	Toshiba
			300	x									x		x	TC5090	Toshiba
	2	50	255	x										x		ADC0800P	† National
				x										x		ADC0800PC	National
		300	25							x	x	x			x	MB4053	Fujitsu
8 (analog input for microprocessors)																	
	1/2	2.5	1350	x						x						**MP20**	**Burr-Brown (2849)**
				x						x						**MP21**	**Burr-Brown (2849)**
		32	50 *	x												MC14444	Motorola
		400	1000	x						x		x				AD7583K	AD
8 (analog to pulse width converter for microprocessor systems)																	
	1/2	—	15 *							x						MC14443	Motorola
		32	50 *							x						MC14447	Motorola
			75 *							x						μA9708C	Fairchild
										x						μA9708M	† Fairchild
		350	25 *	x						x	x					MB4053	Fujitsu
8 (D/A, A/D, with counter)																	
	1/2	500	150	x	x								x	x		**ADC-MC8BC**	**Datel (2862)**
				x	x								x	x		**ADC-MC8BM**	**† Datel (2862)**
8 (video digital converter)																	
	1/2	0.05	1320	x										x		TDC1048	TRW-LSI
9	1/2	1	500 *	x	x								x	x	x	ZN433BJ-9	† DDC
				x	x								x	x	x	ZN433CJ-9	† DDC
				x	x								x	x	x	ZN433J-9	† DDC
9 (video A/D converter)																	
	1/2	0.02	2500	x				x								**TDC1019J**	**TRW-LSI (3704)**

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Analog to Digital Converters (Cont'd)

Binary Output (Cont'd)

Bits Res.	Linearity Error ± LSB	Conversion Time ± ½ LSB µS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source	Line
8	1/2																(Cont'd)	
		17	300	x										x		**NE5034**	**Signetics (3609)**	
		30	—	x									x			**AD673J**	**AD (2838)**	
				x									x			**AD673S**	**† AD (2838)**	
		40	5 *	x	x									x	x	AD7570J	AD	
				x	x									x	x	**MP7570J**	**MicroPwr (3046)**	5
			10 *	x						x				x		**ADC0844B**	**National (3537)**	
			175 *	x	x								x	x		**AD570J**	**AD (2838)**	
				x	x								x	x		**AD570S**	**† AD (2838)**	
				x	x								x	x		MCE570J	MCE	
				x	x								x	x		MCE570S	† MCE	10
		60MHz	—	x	x		x							x		**TDC1025**	**† TRW-LSI (3704,3705)**	
		66.6	—	x												AD8581L	AD	
		80	10	x											x	ADC0831B	National	
				x											x	ADC0832B	National	
				x											x	ADC0833B	National	15
				x											x	ADC0834B	National	
				x											x	ADC0838B	National	
		100	15	x						x				x		ADC0808	National	
				x						x				x		ADC0816C	National	
			30	x						x				x		ADC0816	† National	20
				x						x				x		ADC0808	TI	
			70			x							x	x	x	**ADC-830**	**Datel (2863)**	
							x						x	x	x	**MN5065**	**MicroNet (3043)**	
							x						x	x	x	**MN5065H**	**† MicroNet (3043)**	
						x							x	x	x	**MN5066**	**MicroNet (3043)**	25
						x							x	x	x	**MN5066H**	**† MicroNet (3043)**	
			75							x					x	MB4052	Fujitsu	
		100 *	875	x										x		**ADC0802**	**† Intersil (2993)**	
				x										x		**ADC0802C**	**Intersil (2993)**	
				x										x		**ADC0803**	**† Intersil (2993)**	30
				x										x		**ADC0803C**	**Intersil (2993)**	
				x										x		ADC0802	† National	
				x										x		ADC0802C	National	
				x										x		ADC0803C	National	
		108 *	6.8	x						x				x		MK50808	Mostek	35
				x						x				x		MK50816	Mostek	
		300	15 *	x						x						TL530	TI	
				x												TL532	TI	
		1250 *	20 *	x	x									x		4140	TeledyneP	
				x	x									x		4143	TeledyneP	40
				x	x									x		4143-01	† TeledyneP	
		1600	20	x	x							x		x		**ADC-EK8B**	**Datel (2862)**	
			25	x								x		x		TSC8700	TeledyneS	
				x								x		x		TSC8703	TeledyneS	
			43	x										x		**ADC-ET8BM**	**† Datel (2862)**	45
			50	x										x		**ADC-ET8BC**	**Datel (2862)**	
	3/4	15	30	x	x		x						x			**AD7574A**	**AD (2838)**	
				x	x		x						x			**AD7574J**	**AD (2838)**	
				x	x		x						x			**AD7574S**	**† AD (2838)**	
				x	x		x						x			**MP7574A**	**† MicroPwr (3046)**	50
				x	x		x						x			**MP7574J**	**MicroPwr (3046)**	
				x	x		x						x			**MP7574S**	**† MicroPwr (3046)**	

(Continued)

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
CTC—Compl. 2's Compl.
Int. Ref.—Internal Reference
Mux. In—Multiplexed Inputs
S&H—Sample and Hold
Par. Out—Parallel Output
Ser. Out—Serial Output

INTERFACE–Analog to Digital Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Conversion Time ±½ LSB μS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source
Binary Output																	**(Cont'd)**
8	3/4																(Cont'd)
		66.6	—	x												**AD7581K**	**AD (2838)**
		70	2.5 *	x						x				x		**SI520**	**Siliconix (3083)**
				x						x				x		TL520	TI
	1	1.5	75	x							x			x		ADC0820C	National
		2.5	1010		x										x	HS5131B	† HybridSys
					x										x	HS5131C	HybridSys
		9	—		x	x							x	x		ZN449E-8	DDC
					x	x							x	x		ZN449J-8	† DDC
			125	x	x								x	x		**ADC-847A**	**Datel (2863)**
			125 *	x	x								x	x		ZN449E	Ferranti
				x	x								x	x		ZN449J	† Ferranti
		18	4	x						x	x				x	**TLC541**	**TI (541,3103)**
		32	12.5	x						x					x	ADC0831C	National
				x						x					x	ADC0832C	National
				x						x					x	ADC0833C	National
				x						x					x	ADC0834C	National
				x						x					x	ADC0838C	National
		40	12.5	x						x				x		ADC0844B	National
		100	2.5 *	x						x				x		TL521	TI
			15	x						x				x		ADC0809C	National
				x						x				x		ADC0817	National
		100 *	12.5	x										x		**ADC0804**	**† Intersil (2993)**
				x										x		**ADC0804C**	**Intersil (2993)**
				x										x		ADC0804C	National
		110	12.5	x										x		ADC0805C	National
				x										x		ADC0804C	TI
		112 *	15	x						x					x	μPD7001	NEC
		300	15 *	x						x						TL531	TI
				x												TL533	TI
		2000	6.5 *	x									x		x	TC5091	Toshiba
			300	x									x		x	TC5090	Toshiba
	2	50	255	x										x		ADC0800P	† National
				x										x		ADC0800PC	National
		300	25							x	x	x			x	MB4053	Fujitsu
8 (analog input for microprocessors)																	
	1/2	2.5	1350	x						x						**MP20**	**Burr-Brown (2849)**
				x						x						**MP21**	**Burr-Brown (2849)**
		32	50 *	x												MC14444	Motorola
		400	1000	x						x		x				AD7583K	AD
8 (analog to pulse width converter for microprocessor systems)																	
	1/2	—	15 *							x						MC14443	Motorola
		32	50 *							x						MC14447	Motorola
			75 *							x						μA9708C	Fairchild
										x						μA9708M	† Fairchild
		350	25 *	x						x	x					MB4053	Fujitsu
8 (D/A, A/D, with counter)																	
	1/2	500	150	x	x								x	x		**ADC-MC8BC**	**Datel (2862)**
				x	x								x	x		**ADC-MC8BM**	**† Datel (2862)**
8 (video digital converter)																	
	1/2	0.05	1320	x										x		TDC1048	TRW-LSI
9	1/2	1	500 *	x	x								x	x	x	ZN433BJ-9	† DDC
				x	x								x	x	x	ZN433CJ-9	† DDC
				x	x								x	x	x	ZN433J-9	† DDC
9 (video A/D converter)																	
	1/2	0.02	2500	x				x								**TDC1019J**	**TRW-LSI (3704)**

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Analog to Digital Converters (Cont'd)

Binary Output (Cont'd)

Bits Res.	Linearity Error ±LSB	Conversion Time ±½ LSB μS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source
10	—	3	—										x			MAS-1202	AD (2839)
	1/2	0.8	3600	x	x			x					x	x	x	ADC-816MC	Datel (2860)
				x	x			x					x	x	x	ADC-816MM	† Datel (2860)
		1	500 *	x	x								x	x	x	ADC-856C	Datel (2863)
				x	x								x	x	x	ADC-856M	† Datel (2863)
				x	x								x	x	x	ZN433BJ-10	Ferranti
				x	x								x	x	x	ZN433CJ-10	Ferranti
				x	x								x	x	x	ZN433J-10	† Ferranti
				x	x								x	x	x	ZN433CK-10	DDC
				x	x								x	x	x	ZN433K-10	DDC
		1.4	1800 *			x	x						x			HAS-1002	AD (2839)
			3600	x	x			x					x	x	x	ADC-826MC	Datel (2860)
				x	x			x					x	x	x	ADC-826MM	† Datel (2860)
		1.8	755 *	x	x								x	x	x	AD579B	AD (2839)
				x	x								x	x	x	AD579K	AD (2839)
				x	x								x	x	x	AD579T	† AD (2839)
		2.2	755 *	x	x								x	x	x	AD579J	AD (2839)
		5	1400 *			x	x	x					x	x	x	MN5240-10	MicroNet (3043)
			1600 *			x	x	x					x	x	x	DDC-5240-10	† DDC
		6	1100			x	x	x					x	x	x	ADC-84-10	Datel (2862)
						x	x	x					x	x	x	ADC-85C-10	Datel (2862)
			1200			x	x	x					x	x	x	DDCADC87-10	DDC
			1200 *			x	x	x					x	x	x	DDCADC85-10	DDC
		8	1400 *			x	x	x					x	x	x	MNADC84-10	MicroNet (3043)
						x	x	x					x	x	x	MNADC85-10	† MicroNet (3043)
		10	1100			x	x	x					x	x	x	ADC-87-10	Datel
			1500			x	x	x					x	x	x	ADADC84-10	AD (2839)
						x	x	x					x	x	x	ADC84K-10	Burr-Brown (2848)
			1800			x	x	x					x	x	x	ADADC85-10	AD (2839)
					x	x	x	x					x	x	x	ADC85-10	Burr-Brown (2848)
		15	—	x									x			AD573K	AD (2832,2838)
				x									x			AD573S	† AD (2832,2838)
													x	x		ZN442E	Ferranti
													x	x		ZN442J	† Ferranti
		20	350 *	x	x								x	x	x	ZN432BJ-10	Ferranti
				x	x								x	x	x	ZN432CJ-10	Ferranti
				x	x								x	x	x	ZN432E-10	Ferranti
				x	x								x	x	x	ZN432J-10	† Ferranti
				x	x								x	x	x	ZN432CK-10	DDC
				x	x								x	x	x	ZN432K-10	DDC
		21	800			x	x	x					x	x	x	ADADC80-15	AD (2838)
						x	x	x					x	x	x	ADADC80Z-10	† AD (2838)
		30	300	x	x								x	x		AD571K	AD
		40	300	x	x									x	x	μA571K	Fairchild
				x	x									x	x	μA571T	Fairchild
		80 *												x		AD7573K	AD (2835,2838)
														x		AD7573T	† AD (2835,2838)
		120	5 *	x	x									x	x	AD7570L	AD
				x	x									x	x	MP7570L	MicroPwr (3046)
		5000	20 *	x	x									x		4144	TeledyneP
		6000	20	x	x							x		x		ADC-EK10B	Datel (2862)
			25	x								x		x		TSC8701	TeledyneS
				x								x		x		TSC8704	TeledyneS
			43	x										x		ADC-ET10BM	† Datel (2862)
			50	x										x		ADC-ET10BC	Datel (2862)

(Continued)

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
CTC—Compl. 2's Compl.
Int. Ref.—Internal Reference
Mux. In—Multiplexed Inputs
S&H—Sample and Hold
Par. Out—Parallel Output
Ser. Out—Serial Output

INTERFACE–Analog to Digital Converters (Cont'd)

Binary Output (Cont'd)

Bits Res.	Linearity Error ±LSB	Conversion Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source	Line
10																	(Cont'd)	
	1	15	—	x									x			**AD573J**	**AD (2832,2838)**	
		30	300	x	x								x	x		AD571J	AD	
				x	x								x	x		AD571S	† AD	
				x	x								x	x		MCE571J	MCE	
				x	x								x	x		MCE571S	† MCE	5
		40	300	x	x									x	x	µA571J	Fairchild	
				x	x									x	x	µA571S	Fairchild	
		80 *												x		**AD7573J**	**AD (2835,2838)**	
														x		**AD7573S**	**† AD (2835,2838)**	
		200	—	x										x		ADC1001C	National	10
				x										x		ADC1021C	National	
10 Plus Sign	1/2	80	—	x	x		x							x	x	**AD7571K**	**AD (2834,2838)**	
				x	x		x							x	x	**AD7571T**	**† AD (2834,2838)**	
	1	80	—	x	x		x							x	x	**AD7571J**	**AD (2834,2838)**	
				x	x		x							x	x	**AD7571S**	**† AD (2834,2838)**	15
11	1	15	500	x	x								x	x		**HS574J**	**HybridSys (2981)**	
				x	x								x	x		**HS574S**	**† HybridSys (2981)**	
12	1/2	—	1500									x	x			MP2316	Analogic	
					x			x	x			x	x			MP2321	Analogic	
			2735	x	x			x		x	x		x	x		DAS5712	Intech	20
		0.5	1500	x	x								x	x		**MN5247**	**† MicroNet (3043)**	
		1/2	2500	x	x								x	x		AH8022	Analogic	
		1	1500			x	x	x					x	x	x	**MN5245A**	**MicroNet (3043)**	
		1.5	2350 *		x	x							x	x	x	**ADC803B**	**Burr-Brown (2848)**	
		2	1800 *	x	x			x					x	x	x	ADH-8516-12	DDC	25
			1900	x	x			x					x	x	x	**ADC-817MC**	**Datel (2860)**	
				x	x			x					x	x	x	**ADC-817MM**	**† Datel (2860)**	
			2000			x	x	x					x	x	x	**MN5243**	**† MicroNet (3043)**	
			2500			x	x	x					x	x	x	ADC00401	DDC	
			2700			x	x	x						x	x	**ADC-810MC**	**Datel (2860)**	30
						x	x	x						x	x	**ADC-810MM**	**† Datel (2860)**	
		2.2	1800 *			x	x						x			**HAS-1202**	**AD (2839)**	
		3	775 *	x	x								x	x		**AD578L**	**AD (2839)**	
			1900	x	x			x					x	x	x	**ADC-827MC**	**Datel (2860)**	
				x	x			x					x	x	x	**ADC-827MM**	**† Datel (2860)**	35
		3.5	1.8	x	x			x					x	x	x	**ADC60-12**	**Burr-Brown (2848)**	
		4	2700			x	x	x						x	x	**ADC-811MC**	**Datel (2860)**	
						x	x	x						x	x	**ADC-811MM**	**† Datel (2860)**	
		4.5	755 *	x	x								x	x	x	**AD578K**	**AD (2839)**	
			775 *	x	x								x	x	x	**AD578T**	**† AD (2839)**	40
		5	—													**AD5240K**	**AD (2839)**	
																AD5240S	**AD (2839)**	
			1400 *			x	x	x					x	x	x	**MN5240-12**	**MicroNet (3043)**	
			1600 *			x	x	x					x	x	x	DDC-5240-12	† DDC	
			2175			x	x	x					x	x	x	ADH-8586-12	† DDC	45
		6	775 *	x	x								x	x	x	**AD578J**	**AD (2839)**	
				x	x								x	x	x	**AD578S**	**† AD (2839)**	
		8	1400 *			x	x	x					x	x	x	**MNADC84-12**	**MicroNet (3043)**	
						x	x	x					x	x	x	**MNADC85-12**	**MicroNet (3043)**	
						x	x	x					x	x	x	**MNADC87**	**MicroNet (3043)**	50
			1500			x	x	x					x	x	x	**ADC87/MIL**	**† Burr-Brown (2853)**	
						x	x	x					x	x	x	**ADC87U**	**Burr-Brown (2853)**	
			2000			x	x	x					x	x	x	**ADC-HZ12BGC**	**Datel (2860)**	
						x	x	x					x	x	x	**ADC-HZ12BMM**	**† Datel (2860)**	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Analog to Digital Converters (Cont'd)

Binary Output (Cont'd)

Bits Res.	Linearity Error ±LSB	Conversion Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source
12	1/2																(Cont'd)
		9	2150			x	x				x		x	x	x	**ADC-HS12BMC**	**Datel (2860)**
						x	x				x		x	x	x	**ADC-HS12BMM**	**† Datel (2860)**
		9 *	2845	x	x					x	x		x	x		**HDAS-16MC**	**Datel (2861)**
				x	x					x	x		x	x		**HDAS-16MM**	**† Datel (2861)**
				x	x					x	x		x	x		**HDAS-8MC**	**Datel (2861)**
				x	x					x	x		x	x		**HDAS-8MM**	**† Datel (2861)**
		10	1100			x	x	x					x	x	x	**ADC-84-12**	**Datel (2862)**
						x	x	x					x	x	x	**ADC-85-12**	**Datel (2862)**
						x	x	x					x	x	x	**ADC-85C-12**	**Datel (2862)**
					x	x	x	x					x	x	x	ADC-87-12	Datel
			1200			x	x	x					x	x	x	**HSADC85B**	**† HybridSys (2983)**
						x	x	x					x	x	x	**HSADC85C**	**HybridSys (2983)**
			1200 *			x	x	x					x	x	x	DDCADC85-12	DDC
						x	x	x					x	x	x	DDCADC87-12	DDC
			1550			x	x	x					x	x	x	**ADADC84-12**	**AD (2839)**
						x	x	x					x	x	x	**ADC84K-12**	**Burr-Brown (2848)**
			1575			x	x	x					x	x	x	ADH-8585-12	† DDC
			1800			x	x	x					x	x	x	**ADADC85-12**	**AD (2839)**
						x	x	x					x	x	x	**ADC85-12**	**Burr-Brown (2848)**
			2000	x				x					x	x	x	**HI5712-2**	**† Harris (2961)**
				x				x					x	x	x	**HI5712-5**	**Harris (2961)**
				x				x					x	x	x	**HI5712-7**	**Harris (2961)**
				x				x					x	x	x	**HI5712-8**	**† Harris (2961)**
				x				x					x	x	x	**HI5712A-2**	**† Harris (2961)**
				x				x					x	x	x	**HI5712A-7**	**Harris (2961)**
				x				x					x	x	x	**HI5712A-8**	**† Harris (2961)**
		13	744			x	x							x	x	**ADC-5213**	**Datel (2860)**
						x	x							x	x	**ADC-5213E**	**Datel (2860)**
						x	x							x	x	**ADC-5213H**	**† Datel (2860)**
						x	x							x	x	**ADC-5214**	**Datel (2860)**
						x	x							x	x	**ADC-5214E**	**Datel (2860)**
						x	x							x	x	**ADC-5214H**	**† Datel (2860)**
						x	x							x	x	**ADC-5215**	**Datel (2860)**
						x	x							x	x	**ADC-5215E**	**Datel (2860)**
						x	x							x	x	**ADC-5215H**	**† Datel (2860)**
			745	x										x	x	**MN5213**	**MicroNet (3043)**
				x										x	x	**MN5213H**	**† MicroNet (3043)**
							x							x	x	**MN5214**	**MicroNet (3043)**
							x							x	x	**MN5214H**	**† MicroNet (3043)**
							x							x	x	**MN5215**	**MicroNet (3043)**
							x							x	x	**MN5215H**	**† MicroNet (3043)**
			913			x	x	x						x	x	**MN5610**	**† MicroNet (3043)**
			915			x	x						x	x	x	**ADC-5210**	**Datel (2860)**
						x	x						x	x	x	**ADC-5210E**	**Datel (2860)**
						x	x						x	x	x	**ADC-5210H**	**† Datel (2860)**
						x	x						x	x	x	**ADC-5211**	**Datel (2860)**
						x	x						x	x	x	**ADC-5211E**	**Datel (2860)**
						x	x						x	x	x	**ADC-5211H**	**† Datel (2860)**
						x	x						x	x	x	**ADC-5212**	**Datel (2860)**
						x	x						x	x	x	**ADC-5212E**	**Datel (2860)**
						x	x						x	x	x	**ADC-5212H**	**† Datel (2860)**
						x	x						x	x	x	**ADC-5216**	**Datel (2860)**
						x	x						x	x	x	**ADC-5216E**	**Datel (2860)**
						x	x							x	x	**ADC-5216H**	**† Datel (2860)**
						x							x	x	x	ADC582B-12	† HybridSys

(Continued)

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
CTC—Compl. 2's Compl.
Int. Ref.—Internal Reference
Mux. In—Multiplexed Inputs
S&H—Sample and Hold
Par. Out—Parallel Output
Ser. Out—Serial Output

IC MASTER

INTERFACE–Analog to Digital Converters (Cont'd)

Binary Output (Cont'd)

Bits Res.	Linearity Error ± LSB	Conversion Time ± ½ LSB µS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source
12	1/2	13	915														(Cont'd)
						x							x	x	x	ADC582C-12	HybridSys
						x	x						x	x	x	DDC-5210-1	† DDC
						x	x						x	x	x	DDC-5211-1	† DDC
						x	x						x	x	x	DDC-5212-1	† DDC
						x	x						x	x	x	DDC-5216-1	† DDC
						x	x						x	x	x	DDC5210-3	DDC
						x	x						x	x	x	DDC5211-3	DDC
						x	x						x	x	x	DDC5212-3	DDC
						x	x						x	x	x	DDC5216-3	DDC
						x	x						x	x	x	**MN5210**	**MicroNet (3043)**
						x	x						x	x	x	**MN5210H**	**† MicroNet (3043)**
						x	x						x	x	x	**MN5211**	**MicroNet (3043)**
						x	x						x	x	x	**MN5211H**	**† MicroNet (3043)**
						x	x						x	x	x	**MN5212**	**MicroNet (3043)**
						x	x						x	x	x	**MN5212H**	**† MicroNet (3043)**
						x	x						x	x	x	**MN5216**	**MicroNet (3043)**
						x	x						x	x	x	**MN5216H**	**† MicroNet (3043)**
						x	x						x	x	x	TP5210	† TeledyneP
			1000	x									x	x	x	**AD5210**	**AD (2838)**
							x						x	x	x	**AD5211**	**AD (2838)**
							x						x	x	x	AD5212	AD
				x										x	x	AD5213	AD
							x							x	x	**AD5214**	**AD (2838)**
							x							x	x	AD5215	AD
						x							x	x	x	AD5216	AD
		15	500	x	x								x	x		**HS574K**	**HybridSys (2981)**
				x	x								x	x		**HS574L**	**HybridSys (2981)**
		19	1250	x	x			x		x	x		x	x		AD/AM-822	Analogic
		20	725			x	x	x					x	x	x	ADC581B-12	† HybridSys
						x	x	x					x	x	x	ADC581C-12	HybridSys
			2000			x	x	x					x	x	x	**ADC-HX12BGC**	**Datel (2860)**
						x	x	x					x	x	x	**ADC-HX12BMM**	**† Datel (2860)**
		25	725	x	x								x		x	**AD574AK**	**AD (2833,2838)**
				x	x								x	x		**MN574A**	**† MicroNet (3043)**
			800			x	x	x					x	x	x	**ADADC80-12**	**AD (2838)**
						x	x	x					x	x	x	**ADADC80Z-12**	**† AD (2838)**
			925	x	x			x					x	x	x	**AD572A**	**AD (2838)**
				x	x			x					x	x	x	**AD572B**	**AD (2838)**
				x	x			x					x	x	x	**AD572S**	**† AD (2838)**
			950			x	x	x					x	x	x	**MNADC80**	**MicroNet (3043)**
			950 *			x	x	x					x	x	x	**ADC80A-12**	**Burr-Brown (2848)**
		30	780	x	x								x		x	**AD574AT**	**† AD (2833,2838)**
				x	x								x		x	**AD574K**	**AD (2833,2838)**
				x									x		x	**AD574L**	**AD (2833,2838)**
				x	x								x		x	**AD574S**	**† AD (2833,2838)**
				x	x								x		x	**AD574T**	**† AD (2833,2838)**
				x									x		x	**AD574U**	**† AD (2833,2838)**
				x	x								x		x	MCD574K	MCE
				x									x		x	MCE574L	MCE
				x	x								x		x	MCE574S	† MCE
				x	x								x		x	MCE574T	† MCE
				x									x		x	MCE574U	† MCE
		35	620	x	x								x		x	**AD574ZL**	**AD (2833,2838)**
				x	x								x		x	**AD574ZS**	**† AD (2833,2838)**
				x	x								x		x	**AD574ZT**	**† AD (2833,2838)**

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Analog to Digital Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Conversion Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source	Line
Binary Output																	(Cont'd)	
12	1/2	35	620														(Cont'd)	
				x	x								x		x	AD574ZU	†AD (2833,2838)	
				x	x								x		x	MCE574ZL	MCE	
				x	x								x		x	MCE574ZS	† MCE	
				x	x								x		x	MCE574ZT	† MCE	
				x	x								x		x	MCE574ZU	MCE	5
		50	725	x										x	x	AD504B	AD (3351)	
				x									x	x	x	AD5201B	AD	
				x									x	x	x	AD5201T	† AD	
				x									x	x	x	AD5202B	AD	
				x									x	x	x	AD5202T	† AD	10
				x										x	x	AD5204T	† AD	
				x										x	x	AD5205B	AD	
				x										x	x	AD5205T	† AD	
			745	x										x	x	MN5203	MicroNet (3043)	
				x										x	x	MN5203H	† MicroNet (3043)	15
							x							x	x	MN5204	MicroNet (3043)	
							x							x	x	MN5204H	† MicroNet (3043)	
							x							x	x	MN5205	MicroNet (3043)	
							x							x	x	MN5205H	† MicroNet (3043)	
			770	x	x			x					x	x	x	ADC10HT	† Burr-Brown (2848)	20
				x	x			x					x	x	x	ADC10HT-1	† Burr-Brown (2848)	
			915			x	x						x	x	x	DDC-5200-1	† DDC	
						x	x						x	x	x	DDC-5201-1	† DDC	
						x	x						x	x	x	DDC-5202-1	† DDC	
						x	x						x	x	x	DDC-5206-1	† DDC	25
						x	x						x	x	x	DDC5200-3	DDC	
						x	x						x	x	x	DDC5201-3	DDC	
						x	x						x	x	x	DDC5202-3	DDC	
						x	x						x	x	x	DDC5206-3	DDC	
				x									x	x	x	MN5200	MicroNet (3043)	30
				x									x	x	x	MN5200H	† MicroNet (3043)	
							x						x	x	x	MN5201	MicroNet (3043)	
							x						x	x	x	MN5201H	† MicroNet (3043)	
							x						x	x	x	MN5202	MicroNet (3043)	
							x						x	x	x	MN5202H	† MicroNet (3043)	35
						x							x	x	x	MN5206	MicroNet (3043)	
						x							x	x	x	MN5206H	† MicroNet (3043)	
			1000				x						x	x	x	AD5201	AD	
							x						x	x	x	AD5202	AD	
				x										x	x	AD5203	AD	40
							x							x	x	AD5204	AD	
							x							x	x	AD5205	AD	
						x							x	x	x	AD5206	AD	
		125	740	x									x		x	4161	† TeledyneP	
				x									x		x	4162	† TeledyneP	45
						x							x		x	4163	† TeledyneP	
							x	x					x		x	4164	† TeledyneP	
							x	x					x		x	4165	† TeledyneP	
		175	80			x							x	x		HS5250C	HybridSys	
							x						x	x		HS5251C	HybridSys	50
							x						x	x		HS5252C	HybridSys	
						x							x	x		HS5253C	HybridSys	
				x									x	x	x	MN5250	MicroNet	
				x									x	x	x	MN5250H	† MicroNet	
							x						x	x	x	MN5251	MicroNet	55

(Continued)

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
CTC—Compl. 2's Compl.
Int. Ref.—Internal Reference
Mux. In—Multiplexed Inputs
S&H—Sample and Hold
Par. Out—Parallel Output
Ser. Out—Serial Output

INTERFACE–Analog to Digital Converters (Cont'd)

Binary Output (Cont'd)

Bits Res.	Linearity Error ±LSB	Conversion Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source
12	1/2	175	80														(Cont'd)
							x						x	x	x	MN5251H	† MicroNet
							x						x	x	x	MN5252	MicroNet
							x						x	x	x	MN5252H	† MicroNet
						x							x	x	x	MN5253	MicroNet
						x							x	x	x	MN5253H	† MicroNet
		250	311													**MN5700**	**MicroNet (3043)**
		300	112	x	x			x					x	x	x	**ADC-HC12BMC**	**Datel (2860)**
				x	x			x					x	x	x	**ADC-HC12BMM**	**† Datel (2860)**
		2400	43	x										x		**ADC-ET12BM**	**† Datel (2862)**
		5000	15	x										x		µPD7002	NEC
		20000	20	x	x									x		4145	TeledyneP
		24000	20	x	x							x		x		**ADC-EK12B**	**Datel (2862)**
			25	x								x		x		TSC8702	TeledyneS
				x								x		x		TSC8705	TeledyneS
		100000	20	x					x			x	x	x		**ICL7109**	**Intersil (2996)**
				x								x	x	x	x	**TSC7109BC**	**TeledyneS (3094)**
				x					x			x	x	x	x	**TSC7109C**	**TeledyneS (3094)**
				x					x			x	x	x	x	**TSC7109M**	**† TeledyneS (3094)**
	3/4	1.5	2350 *		x	x							x	x	x	**ADC803C**	**Burr-Brown (2848)**
		200	210	x										x	x	ADC1210	† National
				x										x	x	ADC1210C	National
	1	—	500						x			x		x		ADC-7109	Datel
		2	2700	x	x			x					x	x	x	ADH-8516-11	DDC
		5	1600 *			x	x	x					x	x	x	DDC-5240-12	† DDC
		10	600	x				x					x	x		**AM6112**	**AMD (3306)**
		15	500	x	x								x	x		**HS574T**	**† HybridSys (2981)**
				x	x								x	x		**HS574U**	**† HybridSys (2981)**
			720	x	x								x	x		HI674AJ	Harris
				x	x								x	x		HI674AS	† Harris
		25	390	x									x			MCE574AS	† MCE
			720	x	x								x	x		**HI574AJ**	**Harris (2969)**
				x	x								x	x		**HI574AS**	**† Harris (2969)**
			725	x	x								x			**AD574AJ**	**AD (2833,2838)**
				x	x								x			**AD574AS**	**† AD (2833,2838)**
			750	x	x								x	x		**MP574J**	**MicroPwr (3046)**
				x	x								x	x		**MP574S**	**† MicroPwr (3046)**
		30	780	x	x								x		x	**AD574J**	**AD (2833,2838)**
				x	x								x		x	MCE574J	MCE
		35	620	x	x								x		x	**AD574ZJ**	**AD (2833,2838)**
				x	x								x		x	**AD574ZK**	**AD (2833,2838)**
				x	x								x		x	MCE574ZJ	MCE
				x	x								x		x	MCE574ZK	MCE
		50	725	x									x	x	x	AD5201A	AD
				x									x	x	x	AD5201S	† AD
				x									x	x	x	AD5202A	AD
				x									x	x	x	AD5202S	† AD
				x										x	x	AD5204A	AD
				x										x	x	AD5204S	† AD
				x										x	x	AD5205A	AD
				x										x	x	AD5205S	† AD
		175	80			x							x	x		HS5250B	† HybridSys
							x						x	x		HS5251B	† HybridSys
							x						x	x		HS5252B	† HybridSys
						x							x	x		HS5253B	† HybridSys
	1/2	15	720	x	x								x	x		HI674AK	Harris

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Analog to Digital Converters (Cont'd)

Binary Output (Cont'd)

Bits Res.	Linearity Error ±LSB	Conversion Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source	
12	1/2	15	720															(Cont'd)
				x	x								x	x		HI674AL	Harris	
				x	x								x	x		HI674AT	† Harris	
				x	x								x	x		HI674AU	† Harris	
		25	720	x	x								x	x		**HI574AK**	**Harris**	(2969)
				x	x								x	x		**HI574AL**	**Harris**	(2969)
				x	x								x	x		**HI574AT**	**† Harris**	(2969)
				x	x								x	x		**HI574AU**	**† Harris**	(2969)
			750	x	x								x	x		**MP574K**	**MicroPwr**	(3046)
				x	x								x	x		**MP574L**	**MicroPwr**	(3046)
				x	x								x	x		**MP574T**	**† MicroPwr**	(3046)
				x	x								x	x		**MP574U**	**† MicroPwr**	(3046)
	1 1/2	2400	50	x										x		**ADC-ET12BC**	**Datel**	(2862)
	2	3	2175			x	x	x					x	x	x	ADH-8586-10	† DDC	
		6	1575			x	x	x					x	x	x	ADH-8585-10	† DDC	
		200	210	x										x	x	ADC1211	† National	
				x										x	x	ADC1211C	National	
	4	21	950 *			x	x	x					x	x	x	**ADC80A-10**	**Burr-Brown**	(2848)
12 Plus Sign																		
	—	160 ms	—	x												**AD7552**	**AD**	(2838)
12 (2 device set)																		
	1/2	15	785	x									x	x	x	**HS5210B**	**† HybridSys**	(2982)
				x									x	x	x	**HS5210C**	**HybridSys**	(2982)
				x									x	x	x	**HS5211B**	**† HybridSys**	(2982)
				x									x	x	x	**HS5211C**	**HybridSys**	(2982)
				x									x	x	x	**HS5212B**	**† HybridSys**	(2982)
				x									x	x	x	**HS5212C**	**HybridSys**	(2982)
				x										x	x	**HS5213B**	**† HybridSys**	(2982)
				x										x	x	**HS5213C**	**HybridSys**	(2982)
				x										x	x	**HS5214B**	**† HybridSys**	(2982)
				x										x	x	**HS5214C**	**HybridSys**	(2982)
				x										x	x	**HS5215B**	**† HybridSys**	(2982)
				x										x	x	**HS5215C**	**HybridSys**	(2982)
				x									x	x	x	**HS5216B**	**† HybridSys**	(2982)
				x									x	x	x	**HS5216C**	**HybridSys**	(2982)
		250000	40	x					x			x	x	x		ICL7104-12	Intersil	
			360	x					x			x	x	x		ICL8052A	Intersil	
12 (3-Digit BCD)																		
	1/4	1200	20									x		x		**ADC-EK12DC**	**Datel**	(2862)
												x		x		**ADC-EK12DM**	**† Datel**	(2862)
	1	6000 *	50									x	x		x	AD2020	AD	
13	1/2	2	2000	x	x						x		x	x		MN5263	MicroNet	
		10	2400	x				x					x	x	x	MP2713C	Analogic	
		40000 *	64					x						x		**MP7550B**	**MicroPwr**	(3046)
			72					x				x		x	x	**AD7550B**	**AD**	(2838)
14	1/2	—	2735	x	x			x		x	x		x	x		DAS5714	Intech	
		7	2000	x				x					x	x		MP2734	Analogic	
		10	2400	x				x					x	x	x	MP2714C	Analogic	
			3000	x	x			x			x		x	x		AD/AM-724	Analogic	
				x	x			x					x	x	x	MP8014	Analogic	
		40		x										x		**ICL7115**	**Intersil**	(2997)
		50	1100	x	x			x			x		x	x		AD/AM-824	Analogic	
		60	800	x	x			x			x		x	x		AD/AM-834	Analogic	
		125 kHz									x					**HAS-1409**	**AD**	(2837)
		250	300				x						x	x	x	**MN5260**	**MicroNet**	(3043)

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
CTC—Compl. 2's Compl.
Int. Ref.—Internal Reference
Mux. In—Multiplexed Inputs
S&H—Sample and Hold
Par. Out—Parallel Output
Ser. Out—Serial Output

INTERFACE–Analog to Digital Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Conversion Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source	Line
Binary Output																	**(Cont'd)**	
14 (2 device set)																		
	1/2	250000	40	x					x			x	x	x		ICL7104-14	Intersil	
			360	x					x			x	x	x		ICL8052A	Intersil	
14 (3 1/2-Digit BCD)																		
	1/2	10000	20											x		4146	TeledyneP	
15	1/2	5	1750				x						x	x		MP2735-2	Analogic	
		8	1750				x				x		x	x		MP2735-1	Analogic	5
		15	3000	x	x			x					x	x	x	MP8015	Analogic	
		50	1100	x	x			x			x		x	x		AD/AM-825	Analogic	
		60	800	x	x			x			x		x	x		AD/AM-835	Analogic	
	2	400000	20	x					x						x	**TSC800AC**	**TeledyneS (3098)**	
				x					x						x	**TSC800AM**	**† TeledyneS (3098)**	10
	4	400000	20	x					x						x	**TSC800BC**	**TeledyneS (3098)**	
				x					x						x	**TSC800BM**	**† TeledyneS (3098)**	
16	1/2	–	2735	x	x			x		x	x		x	x		DAS5716	Intech	
		8	3000	x	x			x					x	x	x	A8016-9	Intech	
		10	3000	x	x			x					x	x	x	A8016-10	Intech	15
		16	3000	x	x			x					x	x	x	A8016-16	Intech	
		20	3000	x	x			x					x	x	x	A8016	Intech	
		2	3500	x	x			x			x		x	x		AD/AM-826	Analogic	
		2.8	1000 *			x	x	x					x	x	x	**ADC82A**	**Burr-Brown (2848)**	
		32	3000	x	x			x					x	x	x	MP8016	Analogic	20
		100	1200	x	x			x						x		**HS9516-4**	**HybridSys (2982)**	
		170	2500	x	x			x					x	x	x	**ADC731K**	**Burr-Brown (2848)**	
				x	x			x					x	x	x	**ADC73K**	**Burr-Brown (2848)**	
		3000	750									x	x		x	MP2344	Analogic	
	1	50	—	x		x	x	x						x	x	**ADADC71K**	**AD (2836,2838)**	25
				x		x	x	x						x	x	**ADADC72K**	**AD (2836,2838)**	
		100	1200	x	x			x						x		**HS9516-5**	**HybridSys (2982)**	
		170	2500	x	x			x					x	x	x	**ADC731J**	**Burr-Brown (2848)**	
				x	x			x					x	x	x	**ADC73J**	**Burr-Brown (2848)**	
	1 *	17	1550			x	x	x					x	x	x	**PCM75K**	**Burr-Brown (2849)**	30
	2	15	1550 *			x	x	x					x	x		**ADC76K**	**Burr-Brown (2848)**	
		40	1000			x	x	x					x	x	x	**MN5290**	**† MicroNet (3043)**	
						x	x	x					x	x	x	**MN5291**	**† MicroNet (3043)**	
		50	—	x		x	x	x						x	x	**ADADC71J**	**AD (2836,2838)**	
				x		x	x	x						x	x	**ADADC72J**	**AD (2836,2838)**	35
			1550 *			x	x	x					x	x	x	**ADC71K**	**Burr-Brown (2848)**	
						x	x	x					x	x		**ADC72B**	**Burr-Brown (2848)**	
		60	200			x	x	x					x	x	x	**MN5284**	**MicroNet (3043)**	
		100	1200	x	x			x						x		**HS9516-6**	**HybridSys (2982)**	
	2 *	17	1550			x	x	x					x	x	x	**PCM75J**	**Burr-Brown (2849)**	40
	4	15	1550 *			x	x	x					x	x		**ADC76J**	**Burr-Brown (2848)**	
		50	1440			x	x	x					x	x	x	**MN5282**	**MicroNet (3043)**	
			1550 *			x	x	x					x	x		**ADC72A**	**Burr-Brown (2848)**	
						x	x	x					x	x		**ADC72J**	**Burr-Brown (2848)**	
						x	x	x					x	x		**ADC72K**	**Burr-Brown (2848)**	45
			1800 *			x	x	x					x	x	x	**ADC71J**	**Burr-Brown (2848)**	
		100	1440			x	x	x					x	x	x	**MN5280**	**MicroNet (3043)**	
16 (2 device set)																		
	1/2	250000	40	x					x			x	x	x		ICL7104-16	Intersil	
			360	x					x			x	x	x		ICL8052A	Intersil	
17	1/2	400	1550						x			x	x	x		MP8037	Analogic	50

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Analog to Digital Converters (Cont'd)

Decimal Output

Digits	Device	Source	
3 1/2 Digits, Integrating	**ICL7106**	**Intersil**	**(2995)**
	ICL7107	**Intersil**	**(2995)**
	ICL7116	Intersil	
	ICL7117	Intersil	
	ICL7126	Intersil	
	ICL7136	**Intersil**	**(3005)**
	ICL7137	Intersil	
	MP7138	**MicroPwr**	**(3046)**
	MP7138A	**MicroPwr**	**(3046)**
	MC14433	Motorola	
	ADC3511	National	
	ADD3501	National	
	TSC1433A	TeledyneS	
	TSC14433	TeledyneS	
	TSC14433B	TeledyneS	
	TSC7106	TeledyneS	
	TSC7106A	TeledyneS	
	TSC7107	TeledyneS	
	TSC7107A	TeledyneS	
	TSC7116	TeledyneS	
	TSC7116A	TeledyneS	
	TSC7117	TeledyneS	
	TSC7126	TeledyneS	
	TSC7126A	TeledyneS	
3 Digits, Dual Slope, Building Block, for Microprocessor Systems, e.g. TMS1000	TL505C	TI	
3 Digits, Dual Slope, 2 Device Sets	**CA3161**	**RCA**	**(3600)**
	CA3162	**RCA**	**(3600)**
3 1/2 Digits, Drives LCD DVM Display	ZN450	Ferranti	
	ZN451	Ferranti	
3 1/2 Digits, Integrating, 2 Device Sets	ICL7101	Intersil	
	ICL7103	Intersil	
	ICL8052	Intersil	
	ICL8053	Intersil	
	ICL8068	Intersil	
	LD110	**Siliconix**	**(3083)**
	LD111A	**Siliconix**	**(3083)**
3 1/2 Digits, Dual Slope	TSC8751	TeledyneS	
3 1/2—4 1/2 Digits, Ramp type, 2 Device Sets	MC1405	Motorola	
	MC14435	Motorola	
	MC14435E	† Motorola	
	MC1505	† Motorola	
3 1/2	TSC8750	TeledyneS	
3 3/4 Digits, Integrating	ZNA216E	Ferranti	
	ZNA216J	† Ferranti	
	ADC3711	National	
	ADD3701	National	
4 1/2 Digits, Integrating, for microprocessor or UART systems	**SI7135**	**Siliconix**	**(3083)**
4 1/2 Digits, Successive Integration	**ICL7129**	**Intersil**	**(2999)**
4 1/2 Digits, Dual Slope	**ICL7135**	**Intersil**	**(3003)**
	TSC7135	**TeledyneS**	**(3095)**
4 1/2 Digits, Dual Slope, 2 Device Sets	ICL7103A	Intersil	
	ICL8053A	Intersil	
	ICL8068A	Intersil	
	LD120	**Siliconix**	**(3083)**
	LD121A	**Siliconix**	**(3083)**
	LD122	**Siliconix**	**(3083)**

† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE–Digital to Analog Converters

Bits Res.	Linear-ity Error ±LSB	Settling Time ±½ LSB μS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source
D/A Converters																	
4	1/4	0.3	85		x					x	X		x			ZN434E	Ferranti
	1/2	0.004				x						x			x	DAC-0405	Datel
			1040			x						x	x		x	**MN0405**	**MicroNet (3044)**
4 (triple color video DAC)																	
	1/2	0.005 *	1250	x						x					x	VDAC444	Intech
4 (triple color video RAM/DAC)																	
	1/2	0.005 *	3000	x						x					x	RGBDAC4T	Intech
4 (video digital converter)																	
	1/2	0.004 *	1040				x					x			x	**HDG-0405**	**AD (2830)**
						x						x			x	0405H	Intech
6	1/8	3	250			x	x			x			x			**DAC-01A**	**† PMI (3567)**
	1/4	3	250			x	x			x			x			DAC-01	MicroPwr
						x	x			x			x			DAC-01B	† MicroPwr
						x	x			x			x			DAC-01C	MicroPwr
						x	x			x			x			DAC-01D	MicroPwr
						x	x			x			x			DAC-01F	† MicroPwr
						x	x			x			x			DAC-01H	MicroPwr
						x	x	x		x			x			**MP5520A**	**† MicroPwr (3046)**
						x	x	x		x			x			**MP5520B**	**† MicroPwr (3046)**
						x	x	x		x			x			**MP5520C**	**MicroPwr (3046)**
						x	x	x		x			x			**MP5520F**	**† MicroPwr (3046)**
						x	x	x		x			x			**MP5520H**	**MicroPwr (3046)**
						x	x									μPC603	NEC
						x	x			x			x			~~**DAC-01**~~	~~**† PMI (3567)**~~
						x	x			x			x			**DAC-01B**	**† PMI (3567)**
						x	x			x			x			**DAC-01C**	**PMI (3567)**
						x	x			x			x			**DAC-01F**	**† PMI (3567)**
						x	x			x			x			**DAC-01H**	**PMI (3567)**
	1/2	0.006				x						x			x	DAC-0605	Datel
			1352			x						x	x		x	**MN0605**	**MicroNet (3044)**
		0.3	240			x	x							x		**MC1406**	**Motorola (3069)**
						x	x							x		**MC1506**	**† Motorola (3069)**
		1 *	45 *	x						x	x		x			ZN426E-6	Ferranti
		3	200			x	x	x		x			x			**MP5520D**	**MicroPwr (3046)**
			250			x	x			x			x			**DAC-01D**	**PMI (3567)**
6 (A/D,D/A,with counter)																	
	1/2	2.0	175	x						x	x		x			ZN425E-6	Ferranti
6 (video digital converter)																	
	1/2	0.006 *	1350			x						x			x	**HDG-0605**	**AD (2830)**
			1500			x						x			x	0605H	Intech
6/12-Binary Serial																	
	1/2	—	5							x	x			x	x	μA9706C	Fairchild
7	1/2	1 *	45 *	x						x	x		x			ZN426E-7	Ferranti
				x						x	x		x			ZN429E-7	Ferranti
7 (A/D,D/A,with counter)																	
	1/2	2.0	175	x						x	x		x			ZN425E-7	Ferranti
8	—	0.005	—	x								x	x	x		**AD9768**	**† AD (2823,2830)**
	1/8	0.15	1.5 *	x	x	x	x				x			x		**AD7523L**	**AD (2825)**
				x	x	x	x				x			x		AD7523L	Intersil
				x	x	x	x				x			x		AD7523U	† Intersil
				x	x	x	x				x			x		**MP7523L**	**MicroPwr (3046)**
			20	x	x	x	x				x			x	x	**MP7524C**	**MicroPwr (3046)**
		0.15 *	20 *	x	x					x	x			x	x	**AD7524C**	**AD (2825)**
				x	x	x	x				x			x	x	**AD7524L**	**AD (2825)**
				x	x	x	x			x	x			x	x	**AD7524U**	**† AD (2825)**
				x	x	x	x				x			x	x	**MP7524L**	**MicroPwr (3046)**
				x	x	x	x				x			x	x	**MP7524U**	**† MicroPwr (3046)**

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source
8	1/8	0.15 *															(Cont'd)
			670	x	x	x	x				x			x		AD7523J	Intersil
				x	x	x	x				x			x		AD7523S	† Intersil
		1	30	x						x	x			x		DAC0830	National
		1 *	—	x						x	x		x			ZN438	Ferranti
	1/4	0.01	850	x								x				**HDS-0810E**	**AD (2830)**
				x								x				**HDS-0810EM**	**† AD (2830)**
				x								x				**MC10318-9**	**Motorola (3069)**
		0.045	700	x							x	x				**HI5618A-2**	**† Harris (2929)**
				x							x	x				**HI5618A-5**	**Harris (2929)**
		0.065	610	x	x			x		x	x					4084-02	† TeledyneP
				x	x			x		x	x					4084-03	† TeledyneP
		0.085	33	x	x	x	x			x	x	x		x		DAC-080QF	AMD
		0.135	174	x	x	x	x			x	x	x		x		DAC-08A	† AMD
				x	x	x	x			x	x	x		x		**ADDAC08A**	**† AD (2825)**
					x	x	x			x	x	x		x		**ADDAC08H**	**AD (2825)**
				x	x	x	x			x	x	x		x		**DAC-08A**	**† Motorola (3069)**
				x	x	x	x			x	x	x		x		**DAC-08H**	**Motorola (3069)**
				x	x	x	x			x				x		DAC0802	† National
				x	x	x	x			x				x		DAC0802C	National
				x	x	x	x			x	x	x		x		DAC-08A	† PMI
				x	x	x	x			x	x	x		x		DAC-08H	PMI
				x	x	x	x			x	x	x		x		**DAC-08A**	**† Raytheon (3591)**
				x	x	x	x			x	x	x		x		**DAC-08H**	**Raytheon (3591)**
				x	x	x	x			x	x	x		x		DAC-08A	† Signetics
				x	x	x	x			x	x	x		x		DAC-08H	Signetics
		0.15	1.5 *	x	x	x	x				x			x		**AD7523K**	**AD (2825)**
				x	x	x	x				x			x		AD7523K	Intersil
				x	x	x	x				x			x		AD7523T	† Intersil
				x	x	x	x				x			x		**MP7523K**	**MicroPwr (3046)**
			20	x	x	x	x				x			x	x	**MP7524B**	**MicroPwr (3046)**
		0.15 *	20 *	x	x					x	x			x	x	**AD7524B**	**AD (2825)**
				x	x	x	x			x	x			x	x	**AD7524K**	**AD (2825)**
				x	x	x	x			x	x			x	x	**AD7524T**	**† AD (2825)**
				x	x	x	x				x			x	x	**MP7524K**	**MicroPwr (3046)**
				x	x	x	x				x			x	x	**MP7524T**	**† MicroPwr (3046)**
		0.16 *	123(5V)	x	x	x	x	x		x	x			x	x	AM6080AC	AMD
				x	x	x	x	x		x	x			x	x	AM6080AM	† AMD
				x	x	x	x	x	x	x	x			x	x	AM6081AC	AMD
				x	x	x	x	x	x	x	x			x	x	AM6081AM	† AMD
		0.2 *	255 *	x						x	x	x	x	x	x	**NE5119**	**Signetics (3611)**
				x						x	x	x	x	x	x	**SE5119**	**† Signetics (3611)**
			1300 *			x	x				x	x		x		**HDH-0802**	**AD (2830)**
						x	x				x	x		x		**HDH-0802M**	**† AD (2830)**
		0.25	170	x	x					x				x	x	**DAC-888A**	**† PMI (3567)**
				x	x					x				x	x	**DAC-888E**	**PMI (3567)**
		0.25 *	265	x	x					x	x			x		**AD1408-9**	**AD (2825)**
				x	x					x	x			x		**AD1508-9**	**† AD (2825)**
		1	30	x						x	x			x		DAC0831	National
		1.5	375	x						x	x		x		x	**AD558K**	**AD (2817,2825)**
		2 *	255	x						x	x	x	x	x	x	**NE5019**	**Signetics (3607)**
				x						x	x	x	x	x	x	**SE5019**	**† Signetics (3607)**
		20 *	735 *	x	x						x	x				**HDS-0820**	**AD (2830)**
				x	x						x	x				**HDS-0820M**	**† AD (2830)**

(Continued)

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
Int Ref.—Internal Reference
CTC—Compl. 2's Compl.
Mult.—Multiplying

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source	Line
8																	(Cont'd)	
	3/8	1.5	375	x						x	x		x		x	**AD558T**	**†AD (2817,2825)**	
	1/2									x				x		**AD7548K**	**AD (2822,2827)**	
										x				x		**AD7548T**	**†AD (2822,2827)**	
		0.005	—									x		x		SP9768	Plessey	
		0.008				x						x			x	DAC-0805	Datel	5
			800	x								x				**TDC1018**	**TRW-LSI (3702)**	
			1664			x						x	x		x	**MN0805**	**MicroNet (3044)**	
		0.01	700	x		x				x					x	**TDC1016-8**	**TRW-LSI (3704)**	
		0.01 *	675	x								x				**MC10318**	**Motorola (3069)**	
		0.025	630	x	x					x			x			**DAC-HF8BMM**	**† Datel (2860)**	10
				x	x					x			x			DAC-HFBMC	Datel	
		0.045	700	x						x	x					**HI5618B-2**	**† Harris (2929)**	
				x						x	x					**HI5618B-5**	**Harris (2929)**	
		0.065	610	x	x			x		x	x					4084	TeledyneP	
				x	x			x		x	x					4084-01	TeledyneP	15
		0.12	240			x	x			x			x			**DAC90S**	**† Burr-Brown (2848)**	
			255	x						x	x	x	x	x	x	NE5118	Signetics	
				x						x	x	x	x	x	x	SE5118	† Signetics	
		0.135	174	x	x	x	x			x	x	x		x		DAC-08	† AMD	
				x	x	x	x			x	x	x		x		**ADDAC08**	**† AD (2825)**	20
				x	x	x				x	x	x		x		DAC08	† Fairchild	
				x	x	x	x			x	x	x		x		**DAC-08**	**† Motorola (3069)**	
				x	x	x				x				x		DAC0800	† National	
				x	x	x	x			x	x	x		x		DAC-08	† PMI	
				x	x	x	x			x	x	x		x		**DAC-08**	**† Raytheon (3591)**	25
				x	x	x	x			x	x	x		x		DAC-08	† Signetics	
		0.14 *	130 *	x	x					x			x		x	**MC6890A**	**† Motorola (3068)**	
		0.15	1.5 *	x	x	x	x				x			x		**AD7523J**	**AD (2825)**	
				x	x	x	x				x			x		**AD7523S**	**† AD (2825)**	
				x	x	x	x				x			x		**MP7523J**	**MicroPwr (3046)**	30
			20	x	x	x	x				x			x	x	**MP7524A**	**MicroPwr (3046)**	
			136	x	x					x	x	x		x		**DAC-08BC**	**Datel (2863)**	
				x	x					x	x	x		x		**DAC-08BM**	**† Datel (2863)**	
			174	x	x	x	x			x	x	x		x		DAC-08E	AMD	
				x	x	x	x			x	x	x		x		**ADDAC08E**	**AD (2825)**	35
				x	x	x	x			x	x	x		x		DAC08E	Fairchild	
				x	x	x	x			x	x	x		x		**DAC-08E**	**Motorola (3069)**	
				x	x	x				x				x		DAC0800C	National	
				x	x	x				x				x		µPC624	NEC	
				x	x	x	x			x	x	x		x		DAC-08E	PMI	40
				x	x	x	x			x	x	x		x		**DAC-08E**	**Raytheon (3591)**	
				x	x	x	x			x	x	x		x		DAC-08E	Signetics	
		0.15 *	20 *	x	x					x	x			x	x	**AD7524A**	**AD (2825)**	
				x	x	x	x				x			x	x	**AD7524J**	**AD (2825)**	
				x	x	x	x				x			x	x	**AD7524S**	**† AD (2825)**	45
				x	x	x	x				x			x	x	**MP7524J**	**MicroPwr (3046)**	
				x	x	x	x				x			x	x	**MP7524S**	**† MicroPwr (3046)**	
			305	x						x	x			x		DAC0808	† National	
				x						x	x			x		DAC0808C	National	
		0.16 *	123	x	x	x	x	x		x	x			x	x	AM6080C	AMD	50
				x	x	x	x	x		x	x			x	x	AM6080M	† AMD	
				x	x	x	x	x	x	x	x			x	x	AM6081C	AMD	
				x	x	x	x	x	x	x	x			x	x	AM6081M	† AMD	
		0.2	240			x	x			x			x			**DAC90B**	**Burr-Brown (2848)**	
			670	x	x					x	x			x		**DAC-7523**	**Datel (2863)**	55

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source
8	1/2																(Cont'd)
		0.20 *	130 *	x	x					x			x		x	**MC6890**	**Motorola (3068)**
		0.22	20 *	x	x					x	x			x	x	**AD7528K**	**AD (2819,2825)**
				x	x					x	x			x	x	**AD7528L**	**AD (2819,2825)**
				x	x					x	x			x	x	**AD7528T**	**† AD (2819,2825)**
				x	x					x	x			x	x	**AD7528U**	**† AD (2819,2825)**
		0.25	170	x	x					x				x	x	**DAC-888B**	**† PMI (3567)**
				x	x					x				x	x	**DAC-888F**	**PMI (3567)**
		0.25 *	265	x						x	x			x		SSS1408A-8	AMD
				x						x	x			x		SSS1508A-8	† AMD
				x	x					x	x			x		**AD1408-8**	**AD (2825)**
				x	x					x	x			x		**AD1508-8**	**† AD (2825)**
				x	x					x	x			x		DAC-1408A-8	PMI
				x	x					x	x			x		DAC-1508A-8	† PMI
		0.25/1.0	900			x	x	x		x			x	x		**DAC82S**	**† Burr-Brown (2848)**
		0.25/2.0	900			x	x	x		x			x	x		**DAC82K**	**Burr-Brown (2848)**
		0.3 *	305	x						x	x			x		AM1408-8	AMD
				x						x	x			x		AM1508-8	† AMD
				x	x					x	x			x		**DAC-IC8BC**	**Datel (2863)**
				x	x					x	x			x		**DAC-IC8BM**	**† Datel (2863)**
				x						x	x			x		DAC1408	† Fairchild
				x						x	x			x		DAC1408A	Fairchild
				x										x		**MC1408-8**	**Motorola (3069)**
				x										x		**MC1508-8**	**† Motorola (3069)**
				x						x				x		MC1408-8	National
				x						x				x		MC1508-8	† National
				x						x				x		MC1408-8	Signetics
				x						x				x		MC1508-8	† Signetics
		0.6 *	500	x		x				x			x		x	XR9201	Exar
		0.8	100 *	x	x					x	x		x		x	ZN428E-8	Ferranti
				x	x					x	x		x		x	ZN428J-8	† Ferranti
		1	30	x						x	x			x		DAC0832	National
			45 *	x						x	x		x			ZN426E-8	Ferranti
				x						x	x		x			ZN426J-8	† Ferranti
				x						x	x					ZN429E-8	Ferranti
				x						x	x					ZN429J-8	† Ferranti
			750	x						x			x			**MN3008**	**MicroNet (3044)**
				x						x			x			**MN3008H**	**† MicroNet (3044)**
					x					x			x			**MN3009**	**MicroNet (3044)**
					x					x			x			**MN3009H**	**† MicroNet (3044)**
		1.5	75 *	x						x	x		x		x	**AD558J**	**AD (2817,2825)**
			300	x	x					x	x			x		DAC331B-8	† HybridSys
				x	x					x	x			x		DAC331C-8	HybridSys
		2 *	255	x	x					x			x			**DAC-UP8BC**	**Datel (2863)**
				x	x					x			x			**DAC-UP8BM**	**† Datel (2863)**
			255 *	x						x	x	x	x	x	x	NE5018	Signetics
				x						x	x	x	x	x	x	**SE5018**	**† Signetics (526)**
		2.5	570	x	x	x				x			x			**MN3014**	**MicroNet (3044)**
				x	x	x				x			x			**MN3014H**	**† MicroNet (3044)**
		3	680	x	x								x			HS3020B	† HybridSys
				x	x								x			HS3020C	HybridSys
			830	x	x	x				x			x		x	**MN3020**	**MicroNet (3044)**
				x	x	x				x			x		x	**MN3020H**	**† MicroNet (3044)**
		4	1080	x	x		x			x	x		x		x	DAC336B-8	† HybridSys
				x	x		x			x	x		x		x	DAC336C-8	HybridSys

(Continued)

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
Int Ref.—Internal Reference
CTC—Compl. 2's Compl.
Mult.—Multiplying

INTERFACE–Digital to Analog Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source
D/A Converters																	**(Cont'd)**
8	1/2																(Cont'd)
		20	285	x						x	x		x			DAC336B-1	† HybridSys
				x						x	x		x			DAC337B-0	† HybridSys
				x						x	x		x			DAC337B-2	† HybridSys
				x						x	x		x			DAC337C-0	HybridSys
				x						x	x		x			DAC337C-1	HybridSys
				x						x	x		x			DAC337C-2	HybridSys
		23 *	585			x				x	x		x			**MN3000**	**MicroNet (3044)**
						x				x	x		x			**MN3000H**	**† MicroNet (3044)**
					x					x	x		x			**MN3001**	**MicroNet (3044)**
					x					x	x		x			**MN3001H**	**† MicroNet (3044)**
				x						x	x		x			**MN3002**	**MicroNet (3044)**
				x						x	x		x			**MN3002H**	**† MicroNet (3044)**
					x					x	x		x			**MN3006**	**MicroNet (3044)**
					x					x	x		x			**MN3006H**	**† MicroNet (3044)**
		30	570	x	x	x				x			x			**MN3013**	**MicroNet (3044)**
				x	x	x				x			x			**MN3013H**	**† MicroNet (3044)**
		40	300		x					x	x		x			DAC337B-6	† HybridSys
					x					x	x		x			DAC337C-6	HybridSys
	3/4	1.5	375	x						x	x		x		x	**AD558S**	**† AD (2817,2825)**
	1									x				x		**AD7548J**	**AD (2822,2827)**
										x				x		**AD7548S**	**† AD (2822,2827)**
		0.01	—	x	x					x					x	TM1840	Telmos
		0.01 *	675	x								x		x		**MC10318C-7**	**Motorola (3069)**
		0.07	305	x						x	x			x		MC1408-7	Signetics
		0.15	174	x	x	x	x			x	x	x		x		DAC-08C	AMD
				x	x	x	x			x	x	x		x		**ADDAC08C**	**AD (2825)**
				x	x	x	x			x	x	x		x		DAC08C	Fairchild
				x	x	x	x			x	x	x		x		**DAC-08C**	**Motorola (3069)**
				x	x	x				x				x		DAC0801C	National
				x	x	x	x			x	x	x		x		DAC-08C	PMI
				x	x	x	x			x	x	x		x		**DAC-08C**	**Raytheon (3591)**
				x	x	x	x			x	x	x		x		DAC-08C	Signetics
		0.22	20 *	x	x					x	x			x	x	**AD7528J**	**AD (2819,2825)**
				x	x					x	x			x	x	**AD7528S**	**† AD (2819,2825)**
		0.25 *	265	x	x					x	x			x		SSS1408A-7	AMD
				x	x					x	x			x		**AD1408-7**	**AD (2825)**
				x	x					x	x			x		DAC1408B	Fairchild
				x	x					x	x			x		DAC-1408A-7	PMI
		0.3 *	305	x						x	x			x		AM1408-7	AMD
				x										x		**MC1408-7**	**Motorola (3069)**
				x						x				x		DAC0807C	National
				x						x				x		MC1408-7	National
	1 1/4	0.3 *	305	x							x			x		**MC3408**	**Motorola (3069)**
	2	0.01 *	675	x								x		x		**MC10318C-6**	**Motorola (3069)**
		0.25 *	265	x	x					x	x			x		DAC1408C	Fairchild
				x	x					x	x			x		DAC-1408A-6	PMI
		0.3 *	305	x						x	x			x		AM1408-6	AMD
				x										x		**MC1408-6**	**Motorola (3069)**
				x						x				x		DAC0806C	National
				x						x				x		MC1408-6	National
8 (A/D, D/A, with counter)																	
	1/2	2.0	175	x						x	x		x			ZN425E-8	Ferranti
	1	2.0	175	x						x	x		x			ZN425J-8	† Ferranti
8 (D/A, with counter/clock)																	
	1/2	0.8	—	x						x	x		x			ZN435E	Ferranti
				x						x	x		x			ZN435J	† Ferranti

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ± ½ LSB μS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source
8 (triple color video RAM/DAC)																	
	1/2	0.008 *	8000	x								x			x	RGBDAC8E	Intech
			10000	x						x					x	RGBDAC8T	Intech
8 (video digital converter)																	
	1/4	0.010	1976	x								x				HDD-0810	AD
				x								x				HDD-0810M	† AD
			2028	x								x				HDD-0810C	AD
				x								x				HDD-0810CM	† AD
	1/2	0.008	1660			x						x				**HDG-0805**	**AD (2830)**
		0.008 *	1800			x						x			x	0805H	Intech
		0.07	1000	x								x			x	AH8308E	Analogic
				x						x					x	AH8308T	Analogic
			1600	x								x			x	MP8308ECL	Analogic
				x								x			x	MP8318ECL	Analogic
			2200	x						x					x	MP8308	Analogic
				x						x					x	MP8318	Analogic
8 (Dual), Data Latches, Addressable																	
	1	—	1350	x						x			x		x	**MP10**	**Burr-Brown (2849)**
				x						x			x		x	**MP11**	**Burr-Brown (2849)**
8 (7-Bits plus Sign) Companding																	
	—	0.5 *	192							x						AM6072C	AMD
										x						AM6072M	† AMD
	1/2 step																
		0.5	192							x						AM6070AC	AMD
										x						AM6070AM	† AMD
										x	x	x		x		**DAC-86E**	**PMI (3567)**
			207							x	x	x		x		**DAC-88E**	**PMI (3567)**
			500							x	x	x		x		**DAC-89E**	**PMI (3567)**
	1 step	0.5	192							x						AM6070C	AMD
										x						AM6070M	† AMD
		0.5 *	192							x	x	x		x		**DAC-86C**	**PMI (3567)**
			207							x	x	x		x		**DAC-88C**	**PMI (3567)**
			500							x	x	x		x		**DAC-89C**	**PMI (3567)**
8-2 Digit BCD																	
	1/2	0.15	194							x	x	x		x		**DAC-20C**	**PMI (3567)**
9	1/2	0.01	700	x		x				x					x	**TDC1016-9**	**TRW-LSI (3704)**
9 (8-Bits plus Sign)																	
	1/4	0.75	500	x					x	x	x		x	x		**DAC-208A**	**† PMI (3567)**
				x					x	x	x		x	x		**DAC-208E**	**PMI (3567)**
	1/2	0.75	500	x					x	x	x		x	x		**DAC-208B**	**† PMI (3567)**
				x					x	x	x		x	x		**DAC-208F**	**PMI (3567)**
10	1/8	0.5	20	x	x	x	x			x	x			x		**MP7533R**	**MicroPwr (3046)**
				x	x	x	x			x	x			x		**MP7533Y**	**† MicroPwr (3046)**
	1/4 *	0.6 *	780	x						x	x			x		**HI5610-2**	**† Harris (2926)**
				x						x	x			x		**HI5610-4**	**Harris (2926)**
				x						x	x			x		**HI5610-5**	**Harris (2926)**
				x						x	x			x		**HI5610-8**	**† Harris (2926)**
	1/4	0.025 *	735	x	x					x	x					**HDS-1025**	**AD (2830)**
				x	x					x	x					**HDS-1025M**	**† AD (2830)**
		0.25 *	275	x	x					x	x		x			**AD561K**	**AD (2825)**
				x	x					x	x		x			**AD561T**	**† AD (2825)**
		0.3 *	1300			x	x			x	x		x			**HDH-1003**	**AD (2830)**
		0.5	20	x	x	x	x			x	x			x		**MP7533Q**	**MicroPwr (3046)**
				x	x	x	x			x	x			x		**MP7533W**	**† MicroPwr (3046)**
	1/2	0.01	450	x		x				x					x	**TDC1016-10**	**TRW-LSI (3704)**
		0.025	705	x	x					x			x			**DAC-HF10BMC**	**Datel (2860)**
				x	x					x			x			**DAC-HF10BMM**	**† Datel (2860)**
		0.15	450	x	x	x	x			x	x	x		x		**DAC-10B**	**† PMI (3567)**

(Continued)

Bin.—Binary Compl.—Complementary CTC—Compl. 2's Compl.
Off.—Offset Magn.—Magnitude Int Ref.—Internal Reference Mult.—Multiplying

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source
10	1/2	0.15	450														(Cont'd)
				x	x	x	x			x	x	x		x		**DAC-10C**	**†PMI (3567)**
				x	x	x	x			x	x	x		x		**DAC-10F**	**PMI (3567)**
				x	x	x	x			x	x	x		x		**DAC-10G**	**PMI (3567)**
		0.25	380	x							x			x		**MC3410**	**Motorola (3069)**
				x							x			x		**MC3510**	**†Motorola (3069)**
				x							x			x		MC3410	Signetics
			390	x	x					x	x					**DAC-IC10B**	**Datel (2863)**
				x	x					x	x					**DAC-IC10BM**	**†Datel (2863)**
		0.25 *	275	x	x					x	x		x			**AD561J**	**AD (2825)**
				x	x					x	x		x			**AD561S**	**AD (2825)**
		0.3	—	x	x						x			x		**AD7527C**	**AD (2825)**
				x	x						x			x		**AD7527GC**	**AD (2825)**
				x	x						x			x		**AD7527GL**	**AD (2825)**
				x	x						x			x		**AD7527GU**	**†AD (2825)**
				x	x						x			x		**AD7527L**	**AD (2825)**
				x	x						x			x		**AD7527U**	**†AD (2825)**
		0.375	300			x	x			x			x			**DAC-100A**	**†PMI (3567)**
						x	x			x			x			DAC-100A	PMI
		0.5	30	x	x					x	x			x		**DAC-HA10BC-1**	**Datel (2860)**
				x	x					x	x			x		**DAC-HA10BM-1**	**†Datel (2860)**
		0.5 *	0.025	x	x					x	x			x		**DAC-HA10BC**	**Datel (2860)**
				x	x					x	x			x		**DAC-HA10BM**	**†Datel (2860)**
			20 *	x	x	x	x			x	x			x		**AD7520L**	**AD (2825)**
				x	x	x	x			x	x			x		**AD7520U**	**†AD (2825)**
				x	x	x	x			x	x			x		**AD7530L**	**AD (2825)**
				x	x	x	x							x		AD7520L	Intersil
				x	x	x	x							x		AD7520U	†Intersil
				x	x	x	x			x	x			x		AD7530L	Intersil
				x	x	x	x			x	x			x		**MP7520L**	**MicroPwr (3046)**
				x	x	x	x			x	x			x		**MP7520U**	**†MicroPwr (3046)**
				x	x	x	x			x	x			x		**MP7530**	**MicroPwr (3046)**
			20 *	x						x	x			x	x	DAC1000	†National
				x						x	x			x	x	DAC1000C	National
				x	x	x	X			x	x			x	x	DAC1006	†National
				x	x	x	X			x	x			x	x	DAC1006C	National
			40	x	x	x	X			x	x			x	x	**AD7522L**	**AD (2825)**
				x	x	x	X			x	x			x	x	**AD7522U**	**†AD (2825)**
				x	x					x	x			x	x	**MP7522L**	**MicroPwr (3046)**
				x	x	x	x			x	x			x	x	**MP7522U**	**†MicroPwr (3046)**
		0.6	30	x	x	x	x			x	x			x		**AD7533C**	**AD (2825)**
				x	x	x	x			x	x			x		**AD7533L**	**AD (2825)**
				x	x	x	x			x	x			x		**AD7533U**	**†AD (2825)**
		0.8 *	30 *	x	x	x	x			x	x			x		AD7533L	Intersil
				x	x	x	x			x	x			x		AD7533U	†Intersil
				x	x	x	x			x	x			x		**MP7533L**	**MicroPwr (3046)**
				x	x	x	x			x	x			x		**MP7533U**	**†MicroPwr (3046)**
		1.5	30	x	x					x	x			x		DAC331B-10	†HybridSys
				x	x					x	x			x		DAC331C-10	HybridSys
		4 *	255	x						x	x	x	x	x	x	**NE5020**	**Signetics (3608)**
		10	715			x	x			x			x			**MN3040**	**MicroNet (3044)**
						x	x			x			x			**MN3040H**	**†MicroNet (3044)**
		15	165	x				x		x	x			x		DAC348B-10	†HybridSys
				x				x		x	x			x		DAC348C-10	HybridSys
		20	150			x	x			x	x		x			DAC347LPB-10B	†HybridSys

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Digital to Analog Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source
D/A Converters																	**(Cont'd)**
10	1/2	20	150														(Cont'd)
						x				x	x		x			DAC347LPB-10U	† HybridSys
						x	x			x	x		x			DAC347LPC-10B	HybridSys
						x				x	x		x			DAC347LPC-10U	HybridSys
			285		x					x	x		x			DAC337B-4	† HybridSys
				x						x	x		x			DAC337B-5	† HybridSys
					x					x	x		x			DAC337C-4	HybridSys
				x						x	x		x			DAC337C-5	HybridSys
		23 *	585			x				x			x			**MN3003**	**MicroNet (3044)**
						x				x			x			**MN3003H**	**† MicroNet (3044)**
					x					x			x			**MN3004**	**† MicroNet (3044)**
					x					x			x			**MN3004H**	**† MicroNet (3044)**
				x						x			x			**MN3005**	**MicroNet (3044)**
				x						x			x			**MN3005H**	**† MicroNet (3044)**
					x					x			x			**MN3007**	**MicroNet (3044)**
					x					x			x			**MN3007H**	**† MicroNet (3044)**
		30	—		x					x				x		M/D2005-1	HyComp
		40	300			x				x	x		x			DAC337B-3	† HybridSys
					x					x	x		x			DAC337B-7	† HybridSys
						x				x	x		x			DAC337C-3	HybridSys
					x					x	x		x			DAC337C-7	HybridSys
		500 *	24	x						x	x			x		AD7520L	National
				x						x	x			x		AD7520U	† National
				x						x	x			x		DAC1020	† National
				x						x	x			x		DAC1020C	National
	1/2	0.01	990	x								x				**HDS-1015E**	**AD (2830)**
				x								x				**HDS-1015EM**	**† AD (2830)**
		0.012		x								x	x	x		**SP9770**	**Plessey (3071)**
		0.135	276	x		x				x	x			x		**DAC-10B**	**Raytheon (3587)**
				x		x				x	x			x		**DAC-10C**	**Raytheon (3587)**
				x		x				x	x			x		**DAC-10F**	**Raytheon (3587)**
		0.25	380	x						x	x			x		MC3510	Signetics
		0.25 *	300	x						x	x		x	x		**NE5410**	**Signetics (3612)**
				x						x	x		x	x		**SE5410**	**Signetics (3612)**
		0.3 *	1300			x	x			x	x		x			**HDH-1003M**	**† AD (2830)**
		0.375	250			x	x	x		x			x			**ADDAC100K**	**AD (2825)**
						x	x	x		x			x			**ADDAC100L**	**AD (2825)**
						x	x	x		x			x			**ADDAC100T**	**† AD (2825)**
		0.5	20	x	x	x	x			x	x			x		**MP7520R**	**MicroPwr (3046)**
				x	x	x	x			x	x			x		**MP7520Y**	**† MicroPwr (3046)**
		0.8	670	x	x					x	x			x		**DAC-7533**	**Datel (2863)**
	1	0.01	700	x		x				x					x	TDC1016-9	TRW-LSI
		0.15	276	x		x				x	x			x		**DAC-10G**	**Raytheon (3587)**
		0.25	380	x							x			x		**MC3410C**	**Motorola (3069)**
				x						x	x			x		MC3410C	Signetics
			390	x	x					x	x			x		**DAC-IC10BC**	**Datel (2863)**
		0.3	—	x	x						x			x		**AD7527B**	**AD (2825)**
				x	x						x			x		**AD7527K**	**AD (2825)**
				x	x						x			x		**AD7527T**	**† AD (2825)**
			300			x	x			x			x			**DAC-100B**	**† PMI (3567)**
		0.375	250			x	x	x		x			x			**ADDAC100J**	**AD (2825)**
						x	x	x		x			x			**ADDAC100S**	**† AD (2825)**
		0.5	20	x	x	x	x			x	x			x		**MP7520Q**	**MicroPwr (3046)**
				x	x	x	x			x	x			x		**MP7520W**	**† MicroPwr (3046)**
		0.5 *	20 *	x	x	x	x			x	x			x		**AD7520K**	**AD (2825)**

(Continued)

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
Int Ref.—Internal Reference
CTC—Compl. 2's Compl.
Mult.—Multiplying

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB μS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source
10	1	0.5 *	20 *														(Cont'd)
				x	x	x	x			x	x			x		**AD7520T**	**† AD (2825)**
				x	x	x	x			x	x			x		**AD7530K**	**AD (2825)**
				x	x	x	x			x	x			x		AD7520K	Intersil
				x	x	x	x			x	x			x		AD7520T	† Intersil
				x	x	x	x			x	x			x		AD7530K	Intersil
				x	x	x	x			x	x			x		**MP7520K**	**MicroPwr (3046)**
				x	x	x	x			x	x			x		**MP7520T**	**† MicroPwr (3046)**
				x	x	x	x			x	x			x		**MP7530K**	**MicroPwr (3046)**
				x	x	x	x			x	x			x	x	DAC1001	† National
				x	x	x	x			x	x			x	x	DAC1001C	National
				x	x	x	x			x	x			x	x	DAC1007	† National
				x	x	x	x			x	x			x	x	DAC1007C	National
			40	x	x	x	x			x	x			x	x	**AD7522K**	**AD (2825)**
				x	x	x	x			x	x			x	x	**AD7522T**	**† AD (2825)**
			50	x	x	x	x			x	x			x	x	**MP7522K**	**MicroPwr (3046)**
				x	x	x	x			x	x			x	x	**MP7522T**	**† MicroPwr (3046)**
		0.6	30	x	x	x	x			x	x			x		**AD7533B**	**AD (2825)**
				x	x	x	x			x	x			x		**AD7533K**	**AD (2825)**
				x	x	x	x			x	x			x		**AD7533T**	**† AD (2825)**
		0.8 *	30 *	x	x	x	x			x	x			x		AD7533K	Intersil
				x	x	x	x			x	x			x		AD7533T	† Intersil
				x	x	x	x			x	x			x		**MP7533K**	**MicroPwr (3046)**
		1.5 *	300		x			x		x	x		x			**DAC-06E**	**PMI (3567)**
			350	x						x	x		x			**DAC-03AD**	**PMI (3567)**
				x						x	x		x			**DAC-03BD**	**PMI (3567)**
		5	435	x	x								x			**DAC-UP10B**	**Datel (2863)**
		500 *	24	x						x	x			x		AD7520K	National
				x						x	x			x		AD7520T	National
				x						x	x			x		DAC1021	† National
				x						x	x			x		DAC1021C	National
	2	0.01	700	x		x				x					x	TDC1016-8	TRW-LSI
		0.225	300			x	x			x			x			**DAC-100C**	**† PMI (3567)**
						x	x			x			x			DAC-100C	PMI
		0.5 *	20 *	x	x	x	x			x	x			x		**AD7520J**	**AD (2825)**
				x	x	x	x			x	x			x		**AD7520S**	**† AD (2825)**
				x	x	x	x			x	x			x		**AD7530J**	**AD (2825)**
				x	x	x	x			x	x			x		AD7520J	Intersil
				x	x	x	x			x	x			x		AD7520S	† Intersil
				x	x	x	x			x	x			x		AD7530J	Intersil
				x	x	x	x			x	x			x		**MP7520J**	**MicroPwr (3046)**
				x	x	x	x			x	x			x		**MP7520S**	**MicroPwr (3046)**
				x	x	x	x			x	x			x		**MP7530J**	**MicroPwr (3046)**
				x	x	x	x			x	x			x		DAC1002	† National
				x	x	x	x			x	x			x	x	DAC1002C	National
							x			x	x					DAC1008	† National
							x			x	x			x	x	DAC1008C	National
			40	x	x	x	x			x	x			x	x	**AD7522J**	**AD (2825)**
				x	x	x	x			x	x			x	x	**AD7522S**	**† AD (2825)**
			50	x	x	x	x			x	x			x	x	**MP7522J**	**MicroPwr (3046)**
				x	x	x	x			x	x			x	x	**MP7522S**	**† MicroPwr (3046)**
		0.6	30	x	x	x	x			x	x			x		**AD7533A**	**AD (2825)**
				x	x	x	x			x	x			x		**AD7533J**	**AD (2825)**
				x	x	x	x			x	x			x		**AD7533S**	**† AD (2825)**
		0.8 *	30 *	x	x	x	x			x	x			x		AD7533J	Intersil

(Continued)

† Military Temperature Range (–55° to 125°C)

* Typical Value

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INTERFACE–Digital to Analog Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source	Line
D/A Converters																	**(Cont'd)**	
10	2	0.8 *	30 *														(Cont'd)	
				x	x	x				x	x			x		AD7533S	† Intersil	
				x	x	x	x			x	x			x		**MP7533S**	**† MicroPwr (3046)**	
				x	x	x	x			x	x			x		**MP7533T**	**† MicroPwr (3046)**	
				x	x	x	x			x	x			x		MP7533T	MicroPwr	
		1.5 *	300		x			x		x	x		x			**DAC-06F**	**PMI (3567)**	5
			350	x						x	x		x			**DAC-03CD**	**PMI (3567)**	
		500 *	24	x						x	x			x		AD7520J	National	
				x						x	x			x		AD7520S	† National	
				x						x	x			x		DAC1022	† National	
				x						x	x			x		DAC1022C	National	10
	3	0.225	300			x	x			x			x			**DAC-100D**	**† PMI (3567)**	
						x	x			x			x			DAC-100D	PMI	
		0.5 *	50	x	x	x	x			x	x			x		**MP7520H**	**MicroPwr (3046)**	
		1.5 *	350		x			x		x	x		x			**DAC-06B**	**PMI (3567)**	
	4	0.2	—		x	x				x	x		x			DAC-10G	PMI	15
		1.5 *	300		x			x		x	x		x			**DAC-06G**	**PMI (3567)**	
			350	x						x	x		x			**DAC-03DD**	**PMI (3567)**	
	5	1.5 *	350					x		x	x		x			**DAC-06C**	**† PMI (3567)**	
	8	0.5 *	50	x	x	x	x			x	x			x		**MP7520G**	**MicroPwr (3046)**	
10 Companding	1 Step	0.5	260						x							DAC-78F	PMI	20
10 Plus Sign																		
	1/2	1.5 *	350	x					x	x	x		x			**DAC-05E**	**PMI (3567)**	
			500	x					x	x	x		x			**DAC-210A**	**† PMI (3567)**	
				x					x	x	x		x			**DAC-210B**	**† PMI (3567)**	
				x					x	x	x		x			**DAC-210E**	**PMI (3567)**	
		6	300	x												µPC610	NEC	25
	1	1.5 *	300	x					x	x	x		x			**DAC-210G**	**PMI (3567)**	
			350	x					x	x	x		x			**DAC-02AC**	**PMI (3567)**	
				x					x	x	x		x			**DAC-02BC**	**PMI (3567)**	
			500	x					x	x	x		x			**DAC-210F**	**PMI (3567)**	
	2	1.5 *	300	x					x	x	x		x			**DAC-02CC**	**PMI (3567)**	30
				x					x	x	x		x			**DAC-05F**	**PMI (3567)**	
			350	x					x	x	x		x			**DAC-05A**	**† PMI (3567)**	
	3	1.5 *	350	x					x	x	x		x			**DAC-05B**	**† PMI (3567)**	
				x					x	x	x		x			**DAC-05C**	**PMI (3567)**	
	4	1.5 *	300	x					x	x	x		x			**DAC-05G**	**PMI (3567)**	35
		2.5 *	350	x					x	x	x		x			**DAC-02DD**	**PMI (3567)**	
10 Video Digital Converter																		
	1/2	0.015	2340	x									x			HDD-1015	AD	
				x									x			HDD-1015C	AD	
				x									x			HDD-1015M	† AD	
	1/2	75 MHz		x								x	x	x		SP9770	Plessey	40
11 Plus Sign Dynamic Range (7-Bit plus sign format)	1/2 step																	
		0.5	207							x	x	x		x		DAC-88E	PMI	
										x	x	x		x		DAC-89E	PMI	
		0.5 *	207							x	x	x		x		DAC-86E	PMI	
	1 step	0.5	207							x	x	x		x		DAC-86C	PMI	
										x	x	x		x		DAC-88C	PMI	45
										x	x	x		x		DAC-89C	PMI	
12	1/8	0.15	375	x	x			x		x	x					4089-03	TeledyneP	
				x	x			x		x	x					4089-05	TeledyneP	
	1/4	0.01								x	x				x	**AD667K**	**AD (2818,2827)**	
		0.15	375	x	x			x		x	x					4089-02	TeledyneP	50
				x	x			x		x	x					4089-04	TeledyneP	

(Continued)

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
Int Ref.—Internal Reference
CTC—Compl. 2's Compl.
Mult.—Multiplying

INTERFACE

Master Selection Guide

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB μS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source	Line
12	1/4																(Cont'd)	
		0.25	345	x	x					x	x		x			**AD565AK**	**AD (2826,2828)**	
				x	x					x	x		x			**AD565AT**	**†AD (2826,2828)**	
		0.3	270	x						x	x			x		DAC1266A	National	
				x						x	x			x		DAC1266AC	National	
			345	x						x	x		x	x		DAC1265A	National	5
				x						x	x		x	x		DAC1265AC	National	
			800			x	x	x		x	x					TDDAC80I	TeledyneP	
		0.4	—	x	x					x	x					**DAC-562M**	**†Datel (2863)**	
			210	x	x					x	x		x			**MC3512**	**Motorola (3067)**	
			300	x	x					x	x		x	x		**AD566AK**	**AD (2827,2829)**	10
				x	x					x	x		x	x		**AD566AT**	**†AD (2827,2829)**	
				x	x					x	x		x			**AD566K**	**AD (2827,2829)**	
				x	x					x	x		x			**AD566T**	**†AD (2827,2829)**	
				x	x					x	x		x			MCE566AK	MCE	
				x	x					x	x		x	x		MCE566AT	† MCE	15
				x	x					x	x		x	x		MCE566K	MCE	
				x	x					x	x		x			MCE566T	† MCE	
			345	x	x					x	x		x			**AD565K**	**AD (2826,2828)**	
				x	x					x	x		x			**AD565T**	**†AD (2826,2828)**	
				x	x					x	x		x			μA565K	Fairchild	20
				x	x					x	x		x			μA565T	† Fairchild	
				x	x					x	x		x			MCE565K	MCE	
				x	x					x	x		x			MCE565T	† MCE	
			780	x						x	x			x		**HI562A-2**	**†Harris (2920)**	
				x						x	x			x		**HI562A-8**	**Harris (2920)**	25
		0.5	375	x	x					x	x		x			**HI565AK**	**Harris (2923)**	
				x	x					x	x		x			**HI565AT**	**†Harris (2923)**	
			495	x	x					x	x		x		x	**AD567K**	**AD (2827)**	
		1	64 *	x	x					x	x			x		**HI7541K**	**Harris (2953)**	
				x	x					x	x			x		**HI7541T**	**†Harris (2953)**	30
		1.5	465	x	x					x	x			x		**AD562S/BIN**	**AD (2827,2829)**	
				x	x					x	x			x		AD562S/BIN	MicroPwr	
			475	x	x					x	x		x			**AD563K/BIN**	**AD (2826)**	
				x	x					x	x		x			**AD563S/BIN**	**†AD (2826)**	
				x	x					x	x		x			**AD563T/BIN**	**†AD (2826)**	35
			800			x	x	x		x	x					TDDAC80V	TeledyneP	
	1/2	—	35		x			x	x	x					x	**AD7545C**	**AD (2821,2827,2827)**	
					x			x	x	x					x	**AD7545GC**	**AD (2821,2827,2827)**	
					x			x	x	x					x	**AD7545GL**	**AD (2821,2827,2827)**	
					x			x	x	x					x	**AD7545GU**	**AD (2821,2827,2827)**	40
					x			x	x	x					x	**AD7545L**	**AD (2821,2827,2827)**	
					x			x	x	x					x	**AD7545U**	**AD (2821,2827,2827)**	
			1000	x	x	x	x			x	x			x	x	**MP7622B**	**MicroPwr (3046)**	
			1000	x	x	x	x			x	x			x	x	**MP7622T**	**†MicroPwr (3046)**	
		—	1200	x	x	x	x			x	x			x	x	**MP7622K**	**MicroPwr (3046)**	45
		0.01								x	x				x	**AD667J**	**AD (2818,2827)**	
										x	x				x	**AD667S**	**†AD (2818,2827)**	
		0.035	—									x	x			**DAC63**	**Burr-Brown (2848)**	
			855	x	x					x	x					**HDS-1250**	**AD (2830)**	
				x	x					x	x					**HDS-1250M**	**†AD (2830)**	50

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Digital to Analog Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source
D/A Converters																	**(Cont'd)**
12	1/2																(Cont'd)
		0.045	1160			x	x					x	x			**DAC63S**	**Burr-Brown (2848)**
		0.05	—			x	x			x		x	x			ADH-030II-12	DDC
			1485			x	x					x	x			HC4000	HyComp
						x	x					x	x			HC4000-883	† HyComp
		0.050	780	x	x					x			x			**DAC-HF12BMC**	**Datel (2861)**
				x	x					x			x			**DAC-HF12BMM**	**† Datel (2861)**
			1200	x	x					x				x		DAC391B-12	† HybridSys
				x	x					x				x		DAC391C-12	HybridSys
			1350			x	x					x	x			DAC397B-12	† HybridSys
						x	x					x	x			DAC397C-12	HybridSys
		0.06/1	675			x	x			x			x			DAC-8528-12	† DDC
		0.060	395	x	x					x			x			4065	† TeledyneP
		0.1	600	x						x				x		AM6082C	AMD
		0.10	775			x	x			x			x			DDC-DAC87-CBI-I	† DDC
			850			x	x	x		x			x			DDC-DAC85LD-CBI-I	DDC
		0.18	—	x	x					x	x			x		**AD7544B**	**AD (2827)**
				x	x					x	x			x		**AD7544BG**	**AD (2827)**
				x	x					x	x			x		**AD7544GK**	**AD (2827)**
				x	x					x	x			x		**AD7544GT**	**† AD (2827)**
				x	x					x	x			x		**AD7544K**	**AD (2827)**
				x	x					x	x			x		**AD7544T**	**† AD (2827)**
		0.20	430 *	x	x			x		x	x					**DAC10HT**	**† Burr-Brown (2848)**
				x	x			x		x	x		x			**DAC10HT-1**	**† Burr-Brown (2848)**
		0.25	345	x	x					x	x		x			**AD565AJ**	**AD (2826,2828)**
				x	x					x	x		x			**AD565AS**	**† AD (2826,2828)**
				x	x					x	x		x			MCE565AJ	MCE
				x	x					x	x		x			MCE565AS	† MCE
			900			x	x			x			x			4080	† TeledyneP
						x	x			x			x			4080-83	† TeledyneP
						x	x			x			x			4081	TeledyneP
						x	x			x			x			4081-83	† TeledyneP
						x	x			x			x			4082	TeledyneP
						x	x			x			x			4082-83	† TeledyneP
		0.3	270	x						x	x			x		DAC1266L	National
				x						x	x			x		DAC1266LC	National
			345	x						x	x		x	x		DAC1265L	National
				x						x	x		x	x		DAC1265LC	National
			770 *			x				x	x		x			DAC-85C-CBI-I	Datel
						x				x	x		x			**DAC-87C-CBI-I**	**† Datel (2861,2861)**
			1000			x				x			x			**HI5680I-5**	**Harris (2932)**
						x				x	x		x			**HI5685I-4**	**Harris (2938)**
						x	x			x			x			HI5687I-2	† Harris
			1200			x	x	x			x		x			**DAC80Z-CBI-I**	**Burr-Brown (2848)**
		0.3 *	800 *			x	x	x		x			x			**DAC850-CBI-I**	**Burr-Brown (2848)**
						x	x	x		x			x			DAC851-CBI-I	† Burr-Brown
		0.3/1.5 *															
			800 *			x	x	x		x			x			**DAC800-CBI-I**	**Burr-Brown (2848)**
						x	x	x		x			x			**DAC800-CBI-V**	**Burr-Brown (2848)**
						x	x	x		x			x			**DAC851-CBI-I**	**† Burr-Brown (2848)**
		0.3/3 *	800			x	x	x		x			x			**DAC80/CBI**	**Burr-Brown (2848)**
						x	x	x		x			x			**DAC85C-CBI-I**	**Burr-Brown (2848)**
			850			x	x	x		x			x			**ADDAC87/CBI**	**† AD (2826)**
						x	x	x		x			x			**DAC85-CBI**	**MicroNet (3044)**
			925			x	x	x		x			x			**ADDAC80/CBI**	**AD (2825)**

(Continued)

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
Int Ref.—Internal Reference
CTC—Compl. 2's Compl.
Mult.—Multiplying

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB μS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source	Line
12	1/2	0.3/3 *	925														(Cont'd)	
						x	x	x		x			x			**ADDAC85/CBI**	**† AD (2825)**	
						x	x	x		x			x			**ADDAC85C/CBI**	**AD (2825)**	
		0.4	—	x	x					x	x					**DAC-562C**	**Datel (2863)**	
						x	x	x		x						HIDAC801	Harris	
			210	x	x					x	x		x			**MC3412**	**Motorola (3067)**	5
			300	x	x					x	x		x	x		**AD566AJ**	**AD (2827,2829)**	
				x	x					x	x		x	x		**AD566AS**	**† AD (2827,2829)**	
				x	x					x	x		x			**AD566J**	**AD (2827,2829)**	
				x	x					x	x		x			**AD566S**	**† AD (2827,2829)**	
				x	x					x	x		x			MCE565J	MCE	10
				x	x					x	x		x			MCE565S	† MCE	
				x	x					x	x		x	x		MCE566AJ	MCE	
				x	x					x	x		x	x		MCE566AS	† MCE	
				x	x					x	x		x			MCE566J	MCE	
				x	x					x	x		x			MCE566S	† MCE	15
			345	x	x					x	x		x			**AD565J**	**AD (2826,2828)**	
				x	x					x	x		x			**AD565S**	**† AD (2826,2828)**	
				x	x					x	x		x			μA565J	Fairchild	
				x	x					x	x		x			μA565S	† Fairchild	
			400	x	x					x	x			x		DAC862S	† Burr-Brown	20
				x	x	x	x			x	x	x		x		μPC648	NEC	
			780	x						x	x			x		**HI562A-4**	**Harris (2920)**	
				x						x	x			x		**HI562A-5**	**Harris (2920)**	
		0.5	0.05	x	x					x	x			x		**DAC-HA12BC**	**Datel (2860)**	
				x	x					x	x			x		**DAC-HA12BM**	**† Datel (2860)**	25
			20	x	x					x	x			x		**DAC-HA12BC-1**	**Datel (2860)**	
				x	x					x	x			x		**DAC-HA12BM-1**	**† Datel (2860)**	
			312 *	x	x	x	x	x		x	x	x		x		**AM6012C**	**AMD (3301)**	
				x	x	x	x	x		x	x	x		x		**AM6012M**	**† AMD (3301)**	
				x	x	x	x	x		x	x	x		x		MCE6012C	MCE	30
				x	x	x	x	x		x	x	x		x		MCE6012M	† MCE	
			375	x	x					x	x		x			**HI565AJ**	**Harris (2923)**	
				x	x					x	x		x			**HI565AS**	**† Harris (2923)**	
			495	x	x					x	x		x		x	**AD567J**	**AD (2827)**	
				x	x					x	x		x		x	**AD567S**	**† AD (2827)**	35
			1000	x						x	x			x		**AD562**	**Motorola (3069)**	
				x						x	x		x			**AD563**	**Motorola (3069)**	
		0.5 *	1300			x	x			x	x					**HDH-1205**	**AD (2830)**	
						x	x			x	x					**HDH-1205M**	**† AD (2830)**	
		0.6	1410	x	x					x				x		DAC392B-12	HybridSys	40
				x	x					x				x		DAC392C-12	HybridSys	
		1/2	20	x	x	x	x			x	x			x		**MP7541T**	**† MicroPwr (3046)**	
		1	20	x	x	x	x			x	x			x		**MP7541B**	**MicroPwr (3046)**	
				x	x	x	x			x	x			x		**MP7541K**	**MicroPwr (3046)**	
			20 *	x	x	x	x			x	x			x		**AD7541B**	**AD (2825,2827,3351)**	45
				x	x	x	x			x	x			x		**AD7541K**	**AD (2825,2827,3351)**	
				x	x	x	x			x	x			x		**AD7541T**	**† AD (2825,2827,3351)**	
				x	x	x	x			x	x			x		AD7541B	Intersil	
				x	x	x	x			x	x			x		AD7541K	Intersil	
				x	x	x	x			x	x			x		AD7541T	Intersil	50
				x	x	x	x			x	x			x		**MP7621B**	**MicroPwr (3046)**	
				x	x	x	x			x	x			x		**MP7621K**	**MicroPwr (3046)**	
				x	x	x	x			x	x			x		**MP7621T**	**† MicroPwr (3046)**	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source
																	(Cont'd)
12	1/2	1	20 *	x	x	x	x			x	x			x		7541T	† TeledyneS
				x	x	x	x			x	x			x		TSC7541B	TeledyneS
				x	x	x	x			x	x			x		TSC7541K	TeledyneS
				x	x	x	x			x	x			x		TSC8641B	† TeledyneS
				x	x	x	x			x	x			x		TSC8641C	TeledyneS
			30	x	x					x	x			x		HS7541B-2	† HybridSys
				x	x					x	x			x		HS7541C-2	HybridSys
				x						x	x			x		DAC1208	National
				x						x	x			x		DAC1218	National
				x						x	x			x		DAC1230	National
			30 *	x	x					x	x			x		HS7541-4	HybridSys
			64 *	x	x					x	x			x		**HI7541J**	**Harris (2953)**
				x	x					x	x			x		**HI7541S**	**† Harris (2953)**
			450	x	x					x	x			x		**DAC-7541**	**Datel (2863)**
				x	x	x	x			x	x			x		**MP7623B**	**MicroPwr (3046)**
				x	x	x	x			x	x			x		**MP7623K**	**MicroPwr (3046)**
				x	x	x	x			x	x			x		**MP7623T**	**† MicroPwr (3046)**
				x	x					x	x					TDP7541B	TeledyneP
				x	x					x	x					TDP7541K	TeledyneP
				x	x					x	x					TDP7541T	† TeledyneP
		1 *	750		x	x				x	x		x			HSDAC80CBI-I	HybridSys
		1/1.5 *	—			x	x			x			x			**HSDAC87BI/V**	**† HybridSys (2986)**
						x	x			x			x			**HSDAC87CI/V**	**HybridSys (2986)**
		1.5	65	x	x					x	x	x		x		**MP562H**	**MicroPwr (3046)**
				x	x					x	x	x		x		**MP562J**	**MicroPwr (3046)**
				x	x					x	x	x		x		**MP562K**	**MicroPwr (3046)**
			300			x	x			x	x		x			DAC335B-12	† HybridSys
						x	x			x	x		x			DAC335C-12	HybridSys
		1.5 *	—	x						x	x		x		x	**AD563J**	**AD (2826)**
			465	x	x					x	x			x		**AD562K/BIN**	**AD (2827,2829)**
			475	x	x					x	x		x			**AD563J/BIN**	**AD (2826)**
			750		x	x				x	x		x			HSDAC80CBI-V	HybridSys
			800 *			x	x	x		x			x			**DAC850-CBI-V**	**Burr-Brown (2848)**
						x	x	x		x			x			**DAC851-CBI-V**	**Burr-Brown (2848)**
		2	40	x	x					x	x			x		**AD7542B**	**AD (2827)**
				x	x					x	x			x		**AD7542K**	**AD (2827)**
				x	x					x	x			x		**AD7542T**	**† AD (2827)**
				x						x				x		**AD7543B**	**AD (2827)**
				x						x				x		**AD7543K**	**AD (2827)**
			375	x	x					x			x			4058	† TeledyneP
			375 *	x	x	x				x	x			x		HS3120B-2	† HybridSys
				x	x	x				x	x			x		HS3120C-2	HybridSys
			1900			x	x			x						**HDD-1206J**	**AD (2830)**
						x	x			x						**HDD-1206S**	**† AD (2830)**
		2 *	—			x	x			x						DAC345I-12	HybridSys
		2.5	—	x	x					x	x		x			**DAC338B-12-2**	**HybridSys (2983)**
		3	30	x	x					x	x			x		DAC331B-12	† HybridSys
				x	x					x	x			x		DAC331C-12	HybridSys
			770 *			x				x	x		x			DAC-85C-CBI-V	Datel
						x				x	x		x			**DAC-87C-CBI-V**	**† Datel (2861,2861)**
			775			x	x			x			x			DDC-DAC87-CBI-I	† DDC
			850			x	x	x		x			x			DDC-DAC85LD-CBI-V	DDC
						x	x			x			x			**DAC80**	**MicroNet (3044)**
						x	x	x		x			x			**MNDAC87**	**† MicroNet (3044)**

(Continued)

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
Int Ref.—Internal Reference
CTC—Compl. 2's Compl.
Mult.—Multiplying

INTERFACE–Digital to Analog Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source
D/A Converters																	**(Cont'd)**
12	1/2	3															(Cont'd)
			900	x	x					x			x		x	**DAC-HK12BGC**	**Datel (2861)**
								x		x			x		x	**DAC-HK12BGC-2**	**Datel (2861)**
				x	x					x			x		x	**DAC-HK12BMM**	**† Datel (2861)**
								x		x			x		x	HAC-HK12BMM-2	† Datel
				x	x					x			x		x	DAC-HK12BGC	Intech
				x	x					x			x		x	DAC-HK12BMM	† Intech
			1000			x				x			x			**HI5680V-5**	**Harris (2932)**
						x				x	x		x			**HI5685V-4**	**Harris (2938)**
						x	x			x			x			HI5687V-2	Harris
			1050			x	x			x			x			**DAC-HZ12BGC**	**Datel (2861)**
						x	x			x			x			HAC-HZ12BMM	† Datel
		3.5	465	x	x					x	x			x		**AD562A/BCD**	**AD (2827,2829)**
				x	x					x	x			x		**AD562A/BIN**	**AD (2827,2829)**
		4	300	x	x					x	x		x		x	DAC336B-12	† HybridSys
				x	x					x	x		x		x	DAC336C-12	HybridSys
			975			x	x			x			x		x	**DACHK**	**† MicroNet (3044)**
		5	450 *	x	x					x	x		x			**HS9338-2**	**HybridSys (2983)**
			1000		x	x							x			HS3860B	† HybridSys
					x	x							x			HS3860C	HybridSys
			1200			x	x	x			x		x			**DAC80-CBI-V**	**Burr-Brown (2848)**
						x	x	x			x		x			**DAC80Z-CBI-V**	**Burr-Brown (2848)**
						x	x	x		x			x			**DAC85C-CBI-V**	**Burr-Brown (2848)**
						x	x	x			x		x			**DAC85LD-CBI-V**	**Burr-Brown (2848)**
						x	x	x			x		x			**DAC85Z-CBI-V**	**Burr-Brown (2848)**
		5 *	—			x	x			x						DAC345V-12	HybridSys
			525 *			x	x			x	x		x			**MN3850**	**† MicroNet (3044)**
						x	x			x	x		x			**MN3850H**	**MicroNet (3044)**
			675 *			x	x			x			x		x	**MN3860**	**MicroNet (3044)**
						x	x			x			x		x	**MN3860H**	**† MicroNet (3044)**
		7		x						x	x		x	x	x	**ICL7146**	**Intersil (3010)**
			1000			x	x			x			x		x	**AD3860K**	**AD (2827)**
						x	x			x			x		x	**AD3860S**	**† AD (2827)**
			1025			x	x	x		x			x			**DAC87/CBI**	**† Burr-Brown (2853)**
		8	—	x						x	x					AD290T	† AD
				x						x	x					**AD390K**	**AD (2816,2827)**
			375			x	x			x			x			**MN3348**	**MicroNet (3044)**
						x	x			x			x			**MN3348H**	**† MicroNet (3044)**
		10	375			x	x			x			x			**MN3349**	**MicroNet (3044)**
						x	x			x			x			**MN3349H**	**† MicroNet (3044)**
			720	x	x			x		x			x			MP1812A	Analogic
			750			x	x	x		x			x		x	DAC-SL-12	† DDC
			760			x	x			x			x		x	**DAC88**	**† MicroNet (3044)**
						x	x		x				x		x	**MN3660**	**† MicroNet (3044)**
			1200			x	x			x			x			**DAC71**	**MicroNet (3044)**
		15	165	x				x		x	x			x		DAC348B-12	† HybridSys
				x				x		x	x			x		DAC348C-12	HybridSys
			300	x	x					x	x		x			DAC349B-12	† HybridSys
				x	x					x	x		x			DAC349C-12	HybridSys
				x	x					x	x		x			DAC9349-12	HybridSys
		20	150			x	x			x	x		x			DAC347LPB-12U	† HybridSys

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source
12	1/2	20	150													(Cont'd)	
						x	x			x	x		x			DAC347LPC-12B	HybridSys
						x	x			x	x		x			DAC347LPC-12U	HybridSys
						x	x			x	x		x			HAC347LPB-12B	† HybridSys
			355			x				x				x		**MN3412**	**MicroNet (3044)**
		25	—				x			x	x		x		x	DAC02701	DDC
			175 *			x				x	x		x			**DAC9356**	**HybridSys (2986)**
		30	—	x		x				x				x		M/DA2000	HyComp
		35	90			x				x			x			**MN371**	**MicroNet (3044)**
						x				x			x			**MN371H**	**† MicroNet (3044)**
			150				x			x	x		x			**AD370J**	**AD (2826)**
							x			x	x		x			**AD370K**	**AD (2826)**
							x			x	x		x			**AD370S**	**† AD (2826)**
						x				x	x		x			**AD371J**	**AD (2826)**
		35 *	—	x	x					x	x		x			DDC1250-12-1	DDC
				x	x					x	x		x			DDC1250-12-3	DDC
		50	265				x			x	x		x			DAC356B-12	† HybridSys
							x			x	x		x			DAC356C-12	HybridSys
			908				x			x	x		x			DAC356LPB-12	† HybridSys
							x			x	x		x			DAC356LPC-12	HybridSys
			1653			x	x					x	x			**HDS-1240E**	**AD (2830)**
						x	x					x	x			**HDS-1240EM**	**† AD (2830)**
		70	90				x			x	x		x			**MN370**	**MicroNet (3044)**
							x			x	x		x			**MN370H**	**† MicroNet (3044)**
	3/4	8	—	x						x	x					**AD390J**	**AD (2816,2827)**
				x						x	x					**AD390S**	**† AD (2816,2827)**
	1	—	35		x			x	x	x					x	**AD7545B**	**AD (2821,2827,2827)**
					x			x	x	x					x	**AD7545K**	**† AD (2821,2827,2827)**
					x			x	x	x					x	**AD7545T**	**AD (2821,2827,2827)**
		0.06/1	675			x	x			x			x			DAC-8528-11	† DDC
		0.18	—	x	x					x	x			x		**AD7544A**	**AD (2827)**
				x	x					x	x			x		**AD7544J**	**AD (2827)**
				x	x					x	x			x		**AD7544S**	**AD (2827)**
		1	20	x	x	x	x			x	x			x		**MP7541A**	**MicroPwr (3046)**
				x	x	x	x			x	x			x		**MP7541J**	**MicroPwr (3046)**
				x	x	x	x			x	x			x		**MP7541S**	**† MicroPwr (3046)**
			20 *	x	x	x	x			x	x			x		**AD7541A**	**AD (2825,2827,3351)**
				x	x	x	x			x	x			x		**AD7541J**	**AD (2825,2827,3351)**
				x	x	x	x			x	x			x		AD7541A	Intersil
				x	x	x	x			x	x			x		AD7541J	Intersil
				x	x	x	x			x	x			x		**MP7621A**	**MicroPwr (3046)**
				x	x	x	x			x	x			x		**MP7621J**	**MicroPwr (3046)**
				x	x	x	x			x	x			x		**MP7621S**	**† MicroPwr (3046)**
				x	x	x				x	x			x		7541S	† TeledyneS
				x	x	x				x	x			x		TSC7441S	† TeledyneS
				x	x	x				x	x			x		TSC7541A	TeledyneS
				x	x	x				x	x			x		TSC7541J	TeledyneS
				x	x	x				x	x			x		TSC8640B	† TeledyneS
				x	x	x				x	x			x		TSC8640C	TeledyneS
			30	x	x					x	x			x		HS7541B-1	† HybridSys
				x	x					x	x			x		HS7541C-1	HybridSys
				x						x	x			x		DAC1209	National

(Continued)

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
Int Ref.—Internal Reference
CTC—Compl. 2's Compl.
Mult.—Multiplying

INTERFACE–Digital to Analog Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source
D/A Converters																	**(Cont'd)**
12	1	1	30														(Cont'd)
				x						x	x			x		DAC1219	National
				x						x	x			x		DAC1231	National
			40 *	x	x	x	x			x	x			x	x	**MP7622A**	**MicroPwr (3046)**
				x	x	x	x			x	x			x	x	**MP7622J**	**MicroPwr (3046)**
				x	x	x	x			x	x			x	x	**MP7622S**	**† MicroPwr (3046)**
				x	x	x	x			x	x			x	x	**SI7622A**	**Siliconix (3083)**
				x	x	x	x			x	x			x	x	**SI7622S**	**† Siliconix (3083)**
				x	x	x	x			x	x			x	x	SI7722J	Siliconix
			50 *	x	x	x	x			x	x			x		**AD7541S**	**† AD (2825,2827,3351)**
				x	x	x	x			x	x			x		AD7541L	Intersil
				x	x	x	x			x	x			x		AD7541S	† Intersil
			450	x	x	x	x			x	x			x		**MP7623A**	**MicroPwr (3046)**
				x	x	x	x			x	x			x		**MP7623J**	**MicroPwr (3046)**
				x	x	x	x			x	x			x		**MP7623S**	**† MicroPwr (3046)**
				x	x					x	x					TDP75415	† TeledyneP
				x	x					x	x					TDP7541A	TeledyneP
				x	x					x	x					TDP7541J	TeledyneP
		1 *	500	x	x						x					MP1209A	MicroPwr
				x	x						x					MP1209J	MicroPwr
				x	x						x					MP1209S	† MicroPwr
				x	x						x				x	MP1231A	MicroPwr
				x	x						x				x	MP1231J	MicroPwr
				x	x						x				x	MP1231S	† MicroPwr
				x	x						x				x	MP1232H	MicroPwr
				x	x						x				x	MP1232R	† MicroPwr
				x	x						x				x	MP1232Z	MicroPwr
		2	40	x	x					x	x			x		**AD7542A**	**AD (2827)**
				x	x					x	x			x		**AD7542J**	**AD (2827)**
				x	x					x	x			x		**AD7542S**	**† AD (2827)**
				x	x					x				x		**AD7543A**	**AD (2827)**
				x	x					x				x		**AD7543J**	**AD (2827)**
			450	x	x						x			x		MP7542S	† Harris
				x	x						x			x		**MP7542A**	**MicroPwr (3046)**
				x	x						x			x	x	**MP7543A**	**MicroPwr (3046)**
				x	x						x			x	x	**MP7543J**	**MicroPwr (3046)**
				x	x						x			x	x	**MP7543S**	**† MicroPwr (3046)**
			670	x	x						x			x		**MP7542J**	**MicroPwr (3046)**
		2.5	—	x	x					x	x		x			**DAC3388-12-1**	**HybridSys (2983)**
		5	450 *	x	x					x	x		x			**HS9338-1**	**HybridSys (2983)**
		10	750			x	x	x		x			x		x	DAC-SL-11	† DDC
		20 *	500	x	x					x	x		x		x	**DAC9377-16-5**	**HybridSys (2984)**
		30	—	x		x				x				x		M/DA2005	HyComp
		35	150			x				x	x		x			**AD371K**	**AD (2826)**
						x				x	x		x			**AD371S**	**† AD (2826)**
		550 *	30													**AD7240K**	**AD (2820,2825)**
																AD7240T	**† AD (2820,2825)**
	1/2	0.5	330	x						x	x			x		**HI5660-2**	**† Harris (2950)**
				x						x	x			x		**HI5660-5**	**Harris (2950)**
				x						x	x			x		**HI5660A-2**	**† Harris (2950)**
				x						x	x			x		**HI5660A-S**	**Harris (2950)**
		1 *	500	x	x						x					**MP1208B**	**MicroPwr (3046)**
				x	x						x					**MP1208K**	**MicroPwr (3046)**
				x	x						x					**MP1208T**	**† MicroPwr (3046)**
				x	x						x				x	**MP1230B**	**MicroPwr (3046)**

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source
12	1/2	1 *	500														(Cont'd)
				x	x						x				x	**MP1230K**	**MicroPwr (3046)**
				x	x						x				x	**MP1230T**	**† MicroPwr (3046)**
		2	450	x	x						x			x		**MP7542B**	**MicroPwr (3046)**
				x	x						x			x		**MP7542T**	**† MicroPwr (3046)**
				x	x						x			x	x	**MP7543B**	**MicroPwr (3046)**
				x	x						x			x	x	**MP7543K**	**MicroPwr (3046)**
				x	x						x			x	x	**MP7543T**	**† MicroPwr (3046)**
			670	x	x						x			x		**MP7542K**	**MicroPwr (3046)**
	1/4	1 *	500	x	x						x					MP1210H	MicroPwr
				x	x						x					MP1210R	† MicroPwr
				x	x						x					MP1210Z	MicroPwr
	1 1/2	550 *	30													**AD7240J**	**AD (2820,2825)**
																AD7240S	**† AD (2820,2825)**
	2	—	35		x			x	x	x					x	**AD7545A**	**AD (2821,2827,2827)**
					x			x	x	x					x	**AD7545J**	**AD (2821,2827,2827)**
					x			x	x	x					x	**AD7545S**	**† AD (2821,2827,2827)**
		0.04	—	x	x							x	x			DA4000	HyComp
		0.05	—			x	x			x		x	x			ADH-030II-10	DDC
		0.25		x	X	x	x			x	x		x	x		**DAC-6012AC**	**Raytheon (3590)**
				x	X	x	x			x	x		x	x		**DAC-6012AM**	**Raytheon (3590)**
				x	X	x	x			x	x		x	x		**DAC-6012C**	**Raytheon (3590)**
				x	X	x	x			x	x		x	x		**DAC-6012M**	**Raytheon (3590)**
			375	x		x				x	x	x		x		**DAC-312B**	**† PMI (3567)**
				x		x				x	x	x		x		**DAC-312F**	**PMI (3567)**
		0.5	10 *	x						x	x			x		DAC1220	† National
				x						x	x			x		DAC1220C	National
			20 *	x	x	x	x			x	x			x		**MP7621Z**	**MicroPwr (3046)**
		0.5 *	20 *	x	x	x	x			x	x			x		**AD7521L**	**AD (2825)**
				x	x	x	x			x	x			x		**AD7521U**	**† AD (2825)**
				x	x	x	x			x	x			x		AD7521L	Intersil
				x	x	x	x			x	x			x		AD7521U	† Intersil
				x	x	x	x			x	x			x		AD7531L	Intersil
				x	x	x	x			x	x			x		**MP7521L**	**MicroPwr (3046)**
				x	x	x	x			x	x			x		**MP7521U**	**† MicroPwr (3046)**
				x	x	x	x			x	x			x		**MP7531L**	**MicroPwr (3046)**
		0.50	397	x	x	x		x		x	x	x		x		**AM6012**	**Signetics (3605)**
		1	30	x						x	x			x		DAC1210	National
				x						x	x			x		DAC1232	National
		2	40 *	x	x	x	x			x	x			x	x	**MP7622H**	**MicroPwr (3046)**
				x	x	x	x			x	x			x	x	**MP7622R**	**† MicroPwr (3046)**
				x	x	x	x			x	x			x	x	**MP7622Z**	**MicroPwr (3046)**
				x	x	x	x			x	x			x	x	~~**SI7622H**~~	~~**Siliconix (3083)**~~
				x	x	x	x			x	x			x	x	**SI7622R**	**† Siliconix (3083)**
				x	x	x	x			x	x			x	x	**SI7622Z**	**Siliconix (3083)**
			375 *	x	x	x				x	x			x		DAC3120B-0	† HybridSys
				x	x	x				x	x			x		DAC3120C-0	HybridSys
		2 *	—			x	x			x						DAC345I-10	HybridSys
		2.5	—	x	x					x	x		x			**DAC338B-12-0**	**HybridSys (2983)**
		5	450 *	x	x					x	x		x			**HS9338-0**	**HybridSys (2983)**
		5 *	—			x	x			x						DAC345V-10	HybridSys
		20 *	500	x	x					x	x		x		x	**DAC9377-16-4**	**HybridSys (2984)**
		35 *	—	x	x					x	x		x			DDC1250-10-1	DDC
				x	x					x	x		x			DDC1250-10-3	DDC

(Continued)

Bin.—Binary
Off.—Offset
Magn.—Magnitude
Compl.—Complementary
Int Ref.—Internal Reference
CTC—Compl. 2's Compl.
Mult.—Multiplying

IC MASTER

INTERFACE–Digital to Analog Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source
D/A Converters																	**(Cont'd)**
12	2																(Cont'd)
		500 *	24	x						x	x			x		AD7521L	National
				x						x	x			x		AD7521U	† National
	4	0.5 *	20 *	x	x	x	x			x	x			x		**AD7521K**	**AD (2825)**
				x	x	x	x			x	x			x		**AD7521T**	**† AD (2825)**
				x	x	x	x			x	x			x		**AD7531K**	**AD (2825)**
				x	x	x	x			x	x			x		AD7521K	Intersil
				x	x	x	x			x	x			x		AD7521T	† Intersil
				x	x	x	x			x	x			x		AD7531K	Intersil
				x	x	x	x			x	x			x		**MP7521K**	**MicroPwr (3046)**
				x	x	x	x			x	x			x		**MP7521T**	**† MicroPwr (3046)**
				x	x	x	x			x	x			x		**MP7531K**	**MicroPwr (3046)**
		500 *	24	x						x	x			x		AD7521K	National
				x						x	x			x		AD7521T	† National
				x						x	x			x		DAC1221	† National
				x						x	x			x		DAC1221C	National
	8	0.5 *	20 *	x	x	x	x			x	x			x		**AD7521J**	**AD (2825)**
				x	x	x	x			x	x			x		**AD7521S**	**† AD (2825)**
				x	x	x	x			x	x			x		**AD7531J**	**AD (2825)**
				x	x	x	x			x	x			x		AD7521J	Intersil
				x	x	x	x			x	x			x		AD7521S	† Intersil
				x	x	x	x			x	x			x		AD7531J	Intersil
				x	x	x	x			x	x			x		**MP7521J**	**MicroPwr (3046)**
				x	x	x	x			x	x			x		**MP7521S**	**† MicroPwr (3046)**
				x	x	x	x			x	x			x		**MP7531J**	**MicroPwr (3046)**
		500 *	24	x						x	x			x		AD7521J	National
				x						x	x			x		AD7521S	† National
				x						x	x			x		DAC1222	† National
				x						x	x			x		DAC1222C	National
12 Plus Sign Dynamic Range (7-Bit plus sign format)																	
	—	0.5	192							x						AM6072C	AMD
										x						AM6072M	† AMD
	1/2 step	0.5	192							x						AM6070AC	AMD
										x						AM6070AM	† AMD
			207							x	x	x		x		DAC-86E	PMI
	1 step	0.5	192							x						AM6070C	AMD
										x						AM6070M	† AMD
			207							x	x	x		x		DAC-86C	PMI
12-3 Digit BCD																	
	1/4	0.3	770 *			x				x	x		x			DAC-85C-CCD-I	Datel
						x				x	x		x			**DAC-87-CCD-I**	**† Datel (2861,2861)**
		0.3/3 *	925							x	x		x			**ADDAC80/CCD**	**AD (2825)**
						x				x	x		x			**ADDAC85/CCD**	**† AD (2825)**
						x				x	x		x			**ADDAC85C/CCD**	**AD (2825)**
		3	770 *			x				x	x		x			DAC-85C-CCD-V	Datel
						x				x	x		x			**DAC-87-CCD-V**	**† Datel (2861,2861)**
			900										x		x	**DAC-HK12DGC**	**Datel (2861)**
													x		x	**DAC-HK12DMM**	**† Datel (2861)**
		3 *	1050							x			x			**DAC-HZ12DGC**	**Datel (2861)**
										x			x			**DAC-HZ12DMC**	**Datel (2861)**
										x			x			**DAC-HZ12DMM**	**† Datel (2861)**
	1/2	0.3	1200								x		x			**DAC80-CCD-I**	**Burr-Brown (2848)**
											x		x			**DAC80Z-CCD-I**	**Burr-Brown (2848)**

(Continued)

† Military Temperature Range (−55° to 125°C) * Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source
12-3 Digit BCD																	
	1/2															(Cont'd)	
		0.3/3 *	800							x			x			DAC85C/CCD	Burr-Brown (2848)
			850 *							x			x			DA85C-CCD	MicroNet
										x			x			DAC85-CCD	† MicroNet (3044)
		0.5	30							x	x		x			DAC-HA12DC-1	Datel (2860)
										x	x		x			DAC-HA12DM-1	† Datel (2860)
		0.5 *	0.05							x	x		x			DAC-HA12DC	Datel (2860)
										x	x		x			DAC-HA12DM	† Datel (2860)
		15	300	x	x					x	x		x			DAC349B-3D	† HybridSys
				x	x					x	x		x			DAC349C-3D	HybridSys
				x						x	x		x			DAC9349-3D	HybridSys
	1/10	1.5 *	465							x	x			x		AD562K/BCD	AD (2827,2829)
										x	x			x		AD562S/BCD	† AD (2827,2829)
			475							x	x		x			AD563J/BCD	AD (2826)
										x	x		x			AD563K/BCD	AD (2826)
										x	x		x			AD563S/BCD	† AD (2826)
										x	x		x			AD563T/BCD	† AD (2826)
12-4 Digit BCD																	
	1/2	20 *	500	x	x					x	x		x		x	DAC9377-4D	HybridSys (2984)
13	1	0.1	980				x			x			x			2615-12	DDC
		1.6	1100				x			x			x			SDAC-12	DDC
	1/2	10	360	x	x					x	x					MP8526B	MicroPwr (3046)
				x	x					x	x					MP8526S	† MicroPwr (3046)
	1/4	10	360	x	x					x	x					MP8526C	MicroPwr (3046)
				x	x					x	x					MP8526T	† MicroPwr (3046)
	2	0.1	980				x			x			x			2615-11	DDC
		1.6	1100				x			x			x			SDAC-11	DDC
	4	0.1	980				x			x			x			2615-10	DDC
		1.6	1100				x			x			x			SDAC-10	DDC
13 (3 Device Set)																	
	1	1.8	3475					x		x			x			DDAC-12	DDC
	2	1.8	3475					x		x			x			DDAC-11	DDC
	4	1.8	3475					x		x			x			DDAC-10	DDC
14	1/2			x	x					x	x			x		DAC9331-14	HybridSys (2984)
		2	30 *	x	x					x	x			x		HS3140B-4	† HybridSys (2985)
				x	x					x	x			x		HS3140C-4	HybridSys (2985)
		3		x				x		x	x			x	x	ICL7134	Intersil (3001)
			30	x	x					x	x			x		DAC331B-14	† HybridSys
				x	x					x	x			x		DAC331C-14	HybridSys
		15	1135	x	x			x		x			x			MP1814	Analogic
			1950	x				x		x			x		x	MP1914A	Analogic
			2850	x				x		x			x		x	MP1914TC	Analogic
		200 kHz	600							x						HDD-1409	AD (2823)
	1	0.5	0.05	x	x					x	x			x		DAC-HA14BC	Datel (2860)
				x	x					x	x			x		DAC-HA14BM	† Datel (2860)
			30	x	x					x	x			x		DAC-HA14BC-1	Datel (2860)
				x	x					x	x			x		DAC-HA14BM-1	Datel (2860)
		2	30 *	x	x					x	x			x	x	MP3140B-4	† MicroPwr (3046)
				x	x					x	x			x	x	MP3140C-4	MicroPwr (3046)
			375 *	x	x	x				x	x			x		HS3140B-3	HybridSys (2985)
				x	x	x				x	x			x		HS3140C-3	HybridSys (2985)
	2	2	20	x	x					x	x			x	x	MP7614K	MicroPwr (3046)
				x	x					x	x			x	x	MP7614T	† MicroPwr (3046)
			30 *	x	x					x	x			x	x	MP3140B-3	† MicroPwr (3046)
				x	x					x	x			x	x	MP3140C-3	MicroPwr (3046)

(Continued)

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
Int Ref.—Internal Reference
CTC—Compl. 2's Compl.
Mult.—Multiplying

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source
14	2																(Cont'd)
		20	900	x						x				x		DAC-U12-1	† DDC
	4	2	20	x	x					x	x			x	x	**MP7614J**	**MicroPwr (3046)**
				x	x					x	x			x	x	**MP7614S**	**† MicroPwr (3046)**
		20	900	x	x					x				x		DAC-U11-1	† DDC
15	1/2	17	1950	x				x		x			x		x	MP1915A	Analogic
			2850	x				x		x			x		x	MP1915TC	Analogic
16	1/8	25	1425	x				x		x			x		x	MP8116	Analogic
	1/4	3.5	750		x			x	x	x	x		x			MP1936	Analogic
		5	500		x			x	x	x	x		x			MP1926A	Analogic
		50	500		x			x	x	x	x		x			MP1926S	Analogic
	1/2	2 *	60	x	x					x	x			x		DAC370B-16	† HybridSys
				x	x					x	x			x		DAC370C-16	HybridSys
				x	x					x	x			x		**DAC9331-16-6**	**HybridSys (2984)**
				x	x					x	x			x		**MP9331-6**	**MicroPwr (3046)**
		5 *	50 *	x	x					x	x			x	x	**AD7546B**	**AD (2827,2829)**
				x	x					x	x			x	x	**AD7546K**	**AD (2827,2829)**
		20	1950	x				x		x			x		x	MP1916A	Analogic
			2850	x				x		x			x		x	MP1916TC	Analogic
		20 *	500	x	x					x	x		x		x	**DAC9377-16-6**	**HybridSys (2984)**
				x	x					x	x		x		x	**MP9377-16**	**MicroPwr (3046)**
		50	1700			x	x			x	x		x			**DAC736K**	**Burr-Brown (2848)**
	1	1	465	x	x			x		x	x					**HIDAC16B**	**Harris (2946)**
		2 *	60	x	x					x	x			x		**DAC9331-16-5**	**HybridSys (2984)**
				x	x					x	x			x		**MP9331-5**	**MicroPwr (3046)**
		5 *	50 *	x	x					x	x			x	x	**AD7546A**	**AD (2827,2829)**
				x	x					x	x			x	x	**AD7546J**	**AD (2827,2829)**
		20	450	x	x						x			x	x	**MP9377-16-5**	**MicroPwr (3046)**
		50	2000			x	x			x	x		x		x	**DAC736J**	**Burr-Brown (2848)**
						x	x			x	x		x		x	**DAC73J**	**Burr-Brown (2848)**
	1/2	20	450	x	x						x			x	x	**MP9377-16-6**	**MicroPwr (3046)**
	2	0.3	940			x				x	x		x			**DAC700B**	**Burr-Brown (2848)**
						x				x	x		x			**DAC700K**	**Burr-Brown (2848)**
							x	x		x	x		x			**DAC702B**	**Burr-Brown (2848)**
							x	x		x	x		x			**DAC702K**	**Burr-Brown (2848)**
		1	—			x				x			x			DAC-71-COB-I	Datel
						x				x			x			DAC-71-CSB-I	Datel
						x				x			x			DAC-72C-COB-I	Datel
						x				x			x			DAC-72C-CSB-I	Datel
			465	x	x			x		x	x					**HIDAC16C**	**Harris (2946)**
			1175				x	x		x			x			**DAC72C-COB-I**	**Burr-Brown (2848)**
						x				x			x			**DAC72C-CSB-I**	**Burr-Brown (2848)**
			1225				x			x			x			**ADDAC71-COB-I**	**AD (2827,2829)**
						x				x			x			**ADDAC71-CSB-I**	**AD (2827,2829)**
							x			x			x			**ADDAC72-COB-I**	**AD (2827,2829)**
						x				x			x			**ADDAC72-CSB-I**	**AD (2827,2829)**
		2	20	x	x					x	x			x	x	**MP7616T**	**† MicroPwr (3046)**
			30	x	x					x	x			x		**HS3160B-4**	**† HybridSys (2985)**
				x	x					x	x			x		**HS3160C-4**	**HybridSys (2985)**
		2 *	60	x	x					x	x			x		**DAC9331-16-4**	**HybridSys (2984)**
				x	x					x	x			x		**MP9331-4**	**MicroPwr (3046)**
		3		x				x		x	x			x	x	**ICL7145**	**Intersil (3007)**
		4	790			x				x	x		x			**DAC701B**	**Burr-Brown (2848)**
						x				x	x		x			**DAC701K**	**Burr-Brown (2848)**
							x	x		x	x		x			**DAC703B**	**Burr-Brown (2848)**
							x	x		x	x		x			**DAC703K**	**Burr-Brown (2848)**

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Digital to Analog Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source	Line
D/A Converters																	**(Cont'd)**	
16	2																(Cont'd)	
		5	—			x				x			x			DAC-71-COB-V	Datel	
						x				x			x			DAC-71-CSB-V	Datel	
						x				x			x			DAC-72C-COB-V	Datel	
						x				x			x			DAC-72C-CSB-V	Datel	
			1225				x			x			x			ADDAC71-COB-V	AD (2827,2829)	5
						x				x			x			ADDAC71-CSB-V	AD (2827,2829)	
							x			x			x			ADDAC72-COB-V	AD (2827,2829)	
						x				x			x			ADDAC72-CSB-V	AD (2827,2829)	
		10	1175			x				x			x			DAC71-CSB-V	Burr-Brown (2848)	
							x	x		x			x			DAC72-COB-V	Burr-Brown (2848)	10
						x				x			x			DAC72-CSB-V	Burr-Brown (2848)	
							x	x		x			x			DAC72C-COB-V	Burr-Brown (2848)	
						x				x			x			DAC72C-CSB-V	Burr-Brown (2848)	
		20	450	x	x						x			x	x	MP9377-16-4	MicroPwr (3046)	
		35	1170			x	x			x			x			DAC-HP16BMC	Datel (2861)	15
						x	x			x			x			DAC-HP16BMC-1	Datel (2861)	
						x	x			x			x			DAC-HP16BMM	† Datel (2861)	
						x	x			x			x			DAC-HP16BMM-1	† Datel (2861)	
		50/100 *	575 *			x				x			x			DAC70-CSB-I	† Burr-Brown (2848)	
						x				x			x			DAC70C-CSB-I	Burr-Brown (2848)	20
	3	50/100 *	575 *				x			x			x			DAC70-COB-I	† Burr-Brown (2848)	
							x			x			x			DAC70C-COB-I	Burr-Brown (2848)	
	4	2	—	x	x					x	x			x		MP7616L	MicroPwr (3046)	
			20	x	x					x	x			x	x	MP7616J	MicroPwr (3046)	
				x	x					x	x			x	x	MP7616S	† MicroPwr (3046)	25
		3 *	425				x	x		x	x		x			PCM52	Burr-Brown (2849)	
							x	x		x	x		x			PCM53	Burr-Brown (2849)	
	8	2	—	x	x					x	x			x		MP7616K	MicroPwr (3046)	
			30	x	x					x	x			x		HS3160B-3	† HybridSys (2985)	
				x	x					x	x			x		HS3160C-3	HybridSys (2985)	30
16-4 Digit BCD	1/2	15	1170							x			x			DAC-HP16DGC	Datel (2861)	
										x			x			DAC-HP16DMC	Datel (2861)	
										x			x			DAC-HP16DMM	† Datel (2861)	
		50/100 *	575 *							x			x			DAC70-CCD-I	† Burr-Brown (2848)	
										x			x			DAC70C-CCD-I	Burr-Brown (2848)	35
	2	1	—			x				x			x			DAC-71-CCD-I	Datel	
						x				x			x			DAC-72C-CCD-I	Datel	
			1175							x			x			DAC72C-CCD-I	Burr-Brown (2848)	
		5	—			x				x			x			DAC-71-CCD-V	Datel	
						x				x			x			DAC-72C-CCD-V	Datel	40
		10	1175							x			x			DAC71-CCD-V	Burr-Brown (2848)	
							x			x			x			DAC71-COB-V	Burr-Brown (2848)	
										x			x			DAC72-CCD-V	Burr-Brown (2848)	
										x			x			DAC72C-CCD-V	Burr-Brown (2848)	
18	1	20	60	x	x					x	x		x		x	DAC370B-18	† HybridSys	45
				x	x					x	x		x		x	DAC370C-18	HybridSys	
				x	x					x	x		x		x	MP370B-18	† MicroPwr (3046)	
				x	x					x	x		x		x	MP370C-18	MicroPwr (3046)	
			500	x	x					x	x		x			DAC377-18	HybridSys (2984)	
				x	x					x	x		x		x	DAC377B-18	† HybridSys (2984)	50
				x	x					x	x		x		x	DAC377C-18	HybridSys (2984)	

(Continued)

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
Int Ref.—Internal Reference
CTC—Compl. 2's Compl.
Mult.—Multiplying

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB μS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source	Line
18	1	20	500														(Cont'd)	
				x	x					x	x		x		x	**MP377B-18**	† **MicroPwr** **(3046)**	
				x	x					x	x		x		x	**MP377C-18**	**MicroPwr** **(3046)**	

† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE–Display Drivers

Function	Device	Source	Page
Display Drivers			
Bargraph Fluorescent	XR2276	Exar	
Bargraph LED	LM3914	National	
	LM3915	National	
	AN6875	Panasonic	
	LB1405	Sanyo	
	LB1409	Sanyo	
	LB1415	Sanyo	
	LB1416	Sanyo	
	LB1419	Sanyo	
	LB1426	Sanyo	
	LB1436	Sanyo	
	UAA170	Siemens	
	UAA180	Siemens	
	U237B	Telefunken	
	U244	Telefunken	
	U247B	Telefunken	
	U254	Telefunken	
	U257B	Telefunken	
	U267B	Telefunken	
	TSC9403	Toshiba	
	TSC9404	Toshiba	
Bargraph LED or Vacuum Fluorescent (module)	AW580	AWI	
Bargraph or LED Dot Display Generators	**XR2277**	**Exar**	**(3375)**
	XR2278	**Exar**	**(3375)**
	XR2279	**Exar**	**(3375)**
Bargraph VF	HA12010	Hitachi	
	HA12011	Hitachi	
	LM3916	National	
	LB1470	Sanyo	
Bargraph 18-Element LCD Driver	HEF9754V	Signetics	
Clock Driver, Dual	DS3671	National	
Display Controllers and Keyboard Interface: See Microprocessors-General Purpose			
Driver, 16-Channel Electroluminescent Display Column Driver	HV1	Supertex	
Driver, 16-Channel Electroluminescent Display Row Driver	HV2	Supertex	
Electroluminescent Even Column Driver, 32 Outputs	SN75554	TI	
Electroluminescent Even Row Driver, 32 Outputs	SN75552	TI	
Electroluminescent Odd Column Driver, 32 Outputs	SN75553	TI	
Electroluminescent Odd Row Driver, 32 Outputs	SN75551	TI	
Lamp Driver	CSR301	TeledyneC	
LCD Column Driver	**ICM7231**	**Intersil**	**(3020)**
LCD Display Interface (drives 7 to 20-segment linear displays)	SAA1062	Signetics	
LCD Dot Matrix Driver	HLCD0488	Hughes	
	HLCD0515	Hughes	
	HLCD0538A	Hughes	
	HLCD0539A	Hughes	
	HLCD0540	Hughes	
	HLCD0548	Hughes	
	HLCD0550	Hughes	
	HLCD0551	Hughes	
	HLCD0607	Hughes	
	SED1100	SMOS	
	SED1300	SMOS	
LCD Driver, Multiplexed	PCF8576	Signetics	
LCD Driver, 32/64 Segment	PCF8577	Signetics	
LCD Graphics Driver	SED1500	SMOS	
LED Bar Display Driver, 10 LEDs	TA7612A	Toshiba	
LED, Cascadable	SDA2014	Siemens	
LED Display Driver, 5 LEDs	TA7654	Toshiba	
	TA7655	Toshiba	
LED Display Driver, 33 Outputs, 15 mA Sink Capability	MM5486	National	
LED Display/Interface (drives 7, 14, 16-segments for linear displays, bar graphs)	SAA1060	Signetics	
	SAA1061	Signetics	
LED Driver System, 8 Decade, 8x8 Memory, Decoder (versions either hardwire or processor controlled	**ICM7218A**	**Intersil**	**(786)**
	ICM7218B	**Intersil**	**(786)**
	ICM7218C	**Intersil**	**(786)**
	ICM7218D	**Intersil**	**(786)**
	ICM7218E	**Intersil**	**(786)**
LED, Static	U180M	Telefunken	
	U3080M	Telefunken	
Multiplexed LCD Driver, Master and Slave	MC145000	Motorola	
	MC145001	Motorola	
	MM58201	National	
Segment Driver for Gas Discharge Displays	DI232	Dionics	
	DI242	Dionics	
Universal (LED, LCD, or vacuum fluorescent)	S2809	AMI	
BCD (hexadecimal) to 7-Segment Decoder/Driver with Latch Active Low, Open Collector	9370C	Fairchild	
BCD (hexadecimal) to 7-Segment Latch/Decoder/Driver (CMOS with bipolar output)	MC14495	Motorola	
	UCN-4805A	Sprague	
	UCN-4806A	Sprague	
BCD (hexadecimal) to 7-Segment LED Decoder/Driver, Constant Current, with Latch	9368C	Fairchild	
BCD Plus 1 to 7-Segment	LM1017	National	
	U143	Telefunken	
BCD to 7-Segment Decoder/Driver	MC14547BA	† Motorola	
	MC14547BC	Motorola	
BCD to 7-Segment Decoder/Driver, Active High, Open Collector	5449	† Fairchild	
	54LS249	† Fairchild	
	54LS49	† Fairchild	
	74LS249	Fairchild	
	74LS49	Fairchild	
	HD74LS249	Hitachi	
	HD74LS49	Hitachi	
	MC7449	Motorola	
	SN54LS249	Motorola	
	SN54LS49	† Motorola	
	SN74LS249	† Motorola	
	SN74LS49	Motorola	
	DM54LS249	† National	
	DM54LS49	† National	
	DM74LS249	National	
(Continued)			
BCD to 7-Segment Decoder/Driver, Active High, Open Collector (Cont'd)	DM74LS49	National	
	SN54249	**† TI**	**(1002)**
	SN5449	**† TI**	**(935)**
	SN54LS249	**† TI**	**(1002)**
	SN54LS49	**† TI**	**(935)**
	SN74249	**TI**	**(1002)**
	SN7449	**TI**	**(935)**
	SN74LS249	**TI**	**(1002)**
	SN74LS49	**TI**	**(935)**
BCD to 7-Segment Decoder/Driver, Active High, Resistive Pull-Up	5448	† Fairchild	
	54LS248	† Fairchild	
	54LS48	† Fairchild	
	7448	Fairchild	
	74LS248	Fairchild	
	74LS48	Fairchild	
	9307C	Fairchild	
	9307M	† Fairchild	
	HD74LS248	Hitachi	
	HD74LS48	Hitachi	
	MC7448	Motorola	
	MC8307	Motorola	
	MC9307	† Motorola	
	SN54LS248	† Motorola	
	SN54LS48	† Motorola	
	SN74LS248	Motorola	
	SN74LS48	Motorola	
	DM5448	† National	
	DM54LS248	† National	
	DM54LS48	† National	
	DM7448	National	
	DM74LS248	National	
	DM74LS48	National	
	DS8856	National	
	S8T05	† Signetics	
	SN54248	**† TI**	**(1002)**
	SN5448	**† TI**	**(935)**
	SN54LS248	**† TI**	**(1002)**
	SN54LS48	**† TI**	**(935)**
	SN74248	**TI**	**(1002)**
	SN7448	**TI**	**(935)**
	SN74LS248	**TI**	**(1002)**
	SN74LS48	**TI**	**(935)**
BCD to 7-Segment Decoder/Driver, Active Low, Open Collector	54LS347	† Fairchild	
	54LS447	† Fairchild	
	74LS347	Fairchild	
	74LS447	Fairchild	
	MC4039	Motorola	
	S8T04	† Signetics	
	SN54LS347	**† TI**	**(1019)**
	SN54LS447	**† TI**	**(1038)**
	SN74LS347	**TI**	**(1019)**
	SN74LS447	**TI**	**(1038)**
BCD to 7-Segment Decoder/Driver, Active Low, Open Collector, 15 V Output	5447	† Fairchild	
	54LS247	† Fairchild	
	54LS47	† Fairchild	
	7447	Fairchild	
	74LS247	Fairchild	
	74LS47	Fairchild	
	9317BC	Fairchild	
	9317BM	† Fairchild	
	HD7447A	Hitachi	
	HD74LS247	Hitachi	
	HD74LS47	Hitachi	
	MC7447	Motorola	
	SN54LS247	† Motorola	
	SN54LS47	† Motorola	
	SN74LS247	Motorola	
(Continued)			

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Display Drivers (Cont'd)

Display Drivers (Cont'd)

Function	Device	Source	
BCD to 7-Segment Decoder/Driver, Active Low, Open Collector, 15 V Output (Cont'd)			
	SN74LS47	Motorola	
	DM5447A	† National	
	DM54LS247	† National	
	DM54LS47	† National	
	DM7447A	National	
	DM74LS247	National	
	DM74LS47	National	
	383A/C	TeledyneS	
	383B/M	† TeledyneS	
	SN54247	† **TI**	**(1001)**
	SN5447A	† **TI**	**(935)**
	SN54LS247	† **TI**	**(1001)**
	SN54LS247A	† **TI**	**(1001)**
	SN54LS47	† **TI**	**(935)**
	SN74247	**TI**	**(1001)**
	SN7447A	**TI**	**(935)**
	SN74L47	TI	
	SN74LS247	**TI**	**(1001)**
	SN74LS47	**TI**	**(935)**
BCD to 7-Segment Decoder/Driver, Active Low, Open Collector, 30 V Output			
	5446	† Fairchild	
	7446	Fairchild	
	9317CC	Fairchild	
	9317CM	† Fairchild	
	HD7446A	Hitachi	
	MC7446	Motorola	
	DM5446A	† National	
	DM7446A	National	
	SN54246	† **TI**	**(1001)**
	SN5446A	† **TI**	**(935)**
	SN54LS46	† **TI**	**(935)**
	SN74246	**TI**	**(1001)**
	SN7446A	**TI**	**(935)**
	SN74LS46	**TI**	**(935)**
BCD to 7-Segment Decoder/Driver, for Fluorescent Displays	CS250	Cherry	
	CS250-1	Cherry	
BCD to 7-Segment Decoder/Driver, for Liquid Crystal Displays	**CD4055B**	† **RCA**	**(839)**
	CD4055BE	**RCA**	**(839)**
	TC4055B	Toshiba	
BCD to 7-Segment Decoder/Driver, 2-Digit, Direct Driver for Common Anode LED Displays			
	DS8669	National	
BCD to 7-Segment Latch/Decoder/Driver			
	CS260	Cherry	
BCD to 7-Segment Latch/Decoder/Driver (CMOS with bipolar output)			
	F4511BC	Fairchild	
	F4511BM	† Fairchild	
	HD14511B	Hitachi	
	MC14511BA	† Motorola	
	MC14511BC	Motorola	
	MC14513BA	† Motorola	
	MC14513BC	Motorola	
	CD4511BC	National	
	CD4511BM	† National	
	CD4511B	† **RCA**	**(839)**
	CD4511BE	**RCA**	**(839)**
	883/4511B	† SSS	
	SCL4511B	SSS	
	CM4511B	† Solitron	
	CM4511BE	Solitron	
BCD to 7-Segment Latch/Decoder/Driver for Common Cathode LED Displays			
	NE589	Signetics	
BCD to 7-Segment Latch/Decoder/Driver, for Liquid Crystal Displays			
	CD4543BD	† **RCA**	**(839)**
	CD4543BE	**RCA**	**(839)**
BCD to 7-Segment Latch/Decoder/Driver, Output 1-16			
	SAB3211	Siemens	
BCD to 7-Segment Latch/Decoder/Driver (ripple blanking)			
	MC14544BA	† Motorola	
	MC14544BC	Motorola	
BCD to 7-Segment Latch/Decoder/Driver (strobed latch), for Liquid Crystal Displays			
	LS7100	**LSIComp**	**(803)**
	MC14543BA	† Motorola	
	MC14543BC	Motorola	
	CD4056B	† **RCA**	**(839)**
	CD4056BE	**RCA**	**(839)**
	883/4543B	† SSS	
	SCL4543B	SSS	
	TC4056B	Toshiba	
BCD to 7-Segment LED Decoder/Driver			
	CA3168	**RCA**	**(3599)**
BCD to 7-Segment LED Decoder/Driver, Constant Current			
	DS8857	National	
	NE587	Signetics	
BCD to 7-Segment LED Decoder/Driver with Latch, Output 0-9,—,E,H,L,P			
	9374C	Fairchild	
BCD to 7-Segment LED Driver Adjustable Current			
	DS8858	National	
BCD to 7-Segment LED Latch/Decoder/Driver, with Ripple Blanking	F4734BC	Fairchild	
	F4734BM	† Fairchild	
BCD-to-Decimal Decoder/Driver (for lamps)			
	380A/C	TeledyneS	
	380B/M	† TeledyneS	
	381A/C	TeledyneS	
	381B/M	† TeledyneS	
BCD-to-Decimal Decoder/Driver (nixie driver)			
	7441	Fairchild	
	DM5441A	† National	
	DM7441A	National	
	382A/C	TeledyneS	
	382B/M	† TeledyneS	
BCD-to-Decimal Decoder/Driver with Blanking (for cold cathode indicator tubes)			
	54141	† Fairchild	
	74141	Fairchild	
	HD74141	Hitachi	
	MC54141	† Motorola	
	MC74141	Motorola	
	DM54141	† National	
	DM74141	National	
	SN74141	TI	
Quad AC Plasma Display Axis Driver			
	SN55426B	† TI	
	SN55427B	† TI	
	SN75426B	TI	
	SN75427B	TI	
Hex TTL to LED Bulb Driver, with Latch			
	DS8859	National	
	DS8869	National	
2-Digit, 7-Segment Decoder/Driver Interfaces to CPU			
	MN1205E	Panasonic	
	MN1205P	Panasonic	
	MN1205Q	Panasonic	
3 1/2-Digit Liquid Crystal Clock			
	C1200	LSIComp	
4/5-Digit Fluorescent Display Driver			
	MM5474	National	
	MM5476	National	
	MM5477	National	
	MM5478	National	
4/5-Digit (serial data input)			
	MM5450	National	
	MM5451	National	
4/5-Digit Vacuum Fluorescent			
	MM5445	National	
	MM5446	National	
	MM5447	National	
	MM5448	National	
	SAA1063	Signetics	
4x5 Matrix LED Decoder/Driver, Interface to CPU			
	MN1205F	Panasonic	
4x8 Matrix LED Decoder/Driver, Interface to MPU			
	MN1205A	Panasonic	
4-Bit Multiplexed LCD Driver (4x7)			
	HLCD7211-1	Hughes	
	HLCD7211-2	Hughes	
4-Channel Incandescent Lamp Driver			
	CLD4	TeledyneC	
4-Channel Plasma			
	XR2284	Exar	
4-Character, 18-Segment Triplexed LCD Decoder/Driver			
	ICM7233	**Intersil**	**(798)**
4-Digit Driver (Quad Power Stroke)			
	HD6600-2	† Harris	
	HD6600-5	Harris	
	HD6600	National	
4-Digit Fluorescent			
	ICM7235	Intersil	
	ICM7235A	Intersil	
	ICM7235AM	Intersil	
	ICM7235M	Intersil	
4-Digit Gas Discharge Display Anode Driver			
	DI500	Dionics	
	DI502	Dionics	
4-Digit LCD Driver			
	ICM7211AM	**Intersil**	**(779)**
	ICM7211M	**Intersil**	**(779)**
	TSC7211AM	TeledyneS	
4-Digit LED Driver			
	SDA2004	Siemens	
4-Digit LED Driver, Multiplexed BCD or Binary to 7-Segment Decoder/Driver			
	ICM7212	**Intersil**	**(779)**
	ICM7212A	**Intersil**	**(779)**
4-Digit LED Driver, BCD or Binary to 7-Segment Decoder/Driver, Data and Digit Select Code Latches for IP Interface	**ICM7212AM**	**Intersil**	**(779)**
	ICM7212M	**Intersil**	**(779)**
	UDN-7183A	Sprague	
	UDN-7184A	Sprague	
	UDN-7186A	Sprague	
	UHP-482	Sprague	
	TSC701AM	**TeledyneS**	**(3093)**
	TSC7212A	TeledyneS	
	TSC7212AM	TeledyneS	
4-Digit Liquid Crystal, Multiplexed BCD to LCD Decoder/Driver, AC Drive			
	ICM7211	**Intersil**	**(779)**
	ICM7211A	**Intersil**	**(779)**
	DF412	Siliconix	
	SCL25411	SSS	
4-Digit/Segment Fluorescent			
	DI503	Dionics	
	DI504	Dionics	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Display Drivers (Cont'd)

Display Drivers (Cont'd)

Function	Device	Source
4-Digit Select Microprocessor Interface (4x7)		
	HLCD7211-3	Hughes
	HLCD7211-4	Hughes
4-Digit (stores segment and address data, drives 7-8 segment digits)		
	MM74C911	National
4-Digit, 17-Segment Alpha-Numeric with Memory, Decoder and LED Drivers		
	MM74C956	National
	NSM4307	National
	NSM4507	National
4-Digit, 7-Segment LCD Decoder/Driver		
	TSC7211A	TeledyneS
4-Digit, 7-Segment LED Decoder/Driver		
	TSC700A	**TeledyneS (3092)**
4-Digit/8-Segment Fluorescent		
	COP470	National
4-Segment Liquid Crystal		
	CD4054B	**RCA (839)**
	TC4054B	Toshiba
4-Segment MOS to LED Anode Driver		
	75491	Fairchild
	MC75491	Motorola
	DS55493	† National
	DS75491	National
	DS75493	National
	SN75491	TI
	SN75491A	TI
5x7 Dot Matrix LCD/Console Controller		
	CY300	Cybernetic
5x8 Dot Matrix Multiplexed LCD. On-board memory allows ASCII code and special symbols display without refresh circuitry. (2-chip set)		
	PE7901	Polycore
	PE7902	Polycore
5x12 Dot Matrix (up to 80 characters by cascading)		
	10938	Rockwell
	10939	Rockwell
5-Character, 18-Segment Triplexed LCD Decoder/Driver		
	ICM7234	**Intersil (798)**
5-Digit Gas Discharge Display Anode Driver		
	UHD-490	† Sprague
	UHP-490	Sprague
5-Line Plasma Display Axis Driver		
	DI5140	Dionics
	DI5180	Dionics
	DI5240	Dionics
	DI5280	Dionics
5-Segment Gas Discharge Display Cathode Driver		
	UHP-480	Sprague
5-Segment MOS to LED Anode Driver		
	DS8861	National
5-Step Logarithmic Dual LED Driver		
	TA7666	Toshiba
	TA7667	Toshiba
6-Digit Gas Discharge Display Anode Driver		
	DI505	Dionics
	DI507	Dionics
	DI603A	Dionics
	DI604A	Dionics
	DI605A	Dionics
	DS8891	National
	8891	Signetics
	UDN-6164A	Sprague
	UHD-491	† Sprague
	UHP-491	Sprague
	UHP-495	Sprague
6-Digit LED Driver (low voltage)		
	DS8646	National
6-Digit MOS to LED Cathode Driver		
	55492A	† Fairchild
	75492	Fairchild
	75492A	Fairchild
	MC75492	Motorola
	DS75492	National
	DS75494	National
	DS8870	National
	DS8877	National
	PS55494	† National
	SN75492	TI
	SN75492A	TI
	SN75494	TI
6-Digit/Segment Fluorescent		
	DI508	Dionics
	DI509	Dionics
	UDN-6116	Sprague
	UDN-6126	Sprague
6-Digit BCD (stores segment and address data, drives 7-8 segment digits)		
	MM74C912	National
6-Digit Hex (stores segment and address data, drives 7 segments)	MM74C917	National
6-Digit, 7-Segment LCD Driver with Decimal Points, or Three 16-Segment Characters. 48-Stage Shift Register, 48-Bit Data Latch and 48-Segment Driver		
	MSM5219	OKI
7-Digit Gas Discharge Display Anode Driver		
	MC3490	Motorola
	MC3494	Motorola
7-Digit MOS to Gas Discharge		
	XR2272	Exar
7-Digit MOS to LED Cathode Driver		
	SN75497	TI
7-Digit/Segment MOS to Fluorescent		
	XR2271	Exar
7-Line Dot Matrix or Segmented		
	SN75581	TI
7-Segment Gas Discharge Display Cathode Driver		
	DS8885	National
	8885	Signetics
	UHP-481	Sprague
	SN75584A	TI
7-Segment Gas Discharge Display Cathode Driver, with BCD Decoder	DS7880	† National
	DS8880	National
	DS8884A	National
	DS8980	National
	DS8880	Signetics
	SN75480	TI
7-Segment to BCD Converter/Driver		
	MM54C915	† National
	MM74C915	National
8-Bit Parallel In/Parallel Out Fluorescent (for μP systems)		
	UCN-4815A	Sprague
	UCS-4815H	† Sprague
8-Channel Plasma		
	XR2288	Exar
8-Character, 14/16 Segment LED Display Driver		
	ICM7243	**Intersil (3017)**
8-Digit Gas Discharge Display Anode Driver		
	DI510	Dionics
	DI512	Dionics
	DI803A	Dionics
	DI804A	Dionics
	DI805A	Dionics
	DS8887	National
	DS8897	National
	UDN-8184A	Sprague
8-Digit MOS to LED Cathode Driver		
	DS8863	National
	DS8871	National
	DS8963	National
8-Digit/Segment Fluorescent		
	DI513	Dionics
	DI514	Dionics
	DI514A	Dionics
	XR6118	**Exar (3376)**
	XR6128	**Exar (3376)**
	NE594	**Signetics (3623)**
	SA594	**Signetics (3623)**
	SG6118	SiliconG
	UDN-6118	Sprague
	UDN-6128	Sprague
	UDN-6138	Sprague
	UDN-6148	Sprague
8-Digit, 7-Segment Triplexed LCD Decoder/Driver		
	ICM7231	**Intersil (798)**
8-Line Fluorescent Driver		
	MSL912R	**OKI (4118)**
	MSL915R	**OKI (4118)**
	MSL916R	OKI
	MSL917R	**OKI (4118)**
8-Output Digit-Scan Counter/Decoder for Cold-Cathode Counter Tubes		
	MSL9510R	**OKI (4118)**
	MSL9511R	**OKI (4118)**
8-Segment Gas Discharge Display Cathode Driver		
	DI210	Dionics
	DI2210	Dionics
	DI230	Dionics
	DI240	Dionics
	DI300	Dionics
	DI302	Dionics
	MC3491	Motorola
	MC3492	Motorola
	DS7889	† National
	DS8889	National
	UDN-7180A	Sprague
8-Segment MOS to LED Anode Driver		
	MC676	Motorola
	DS8867	National
9-Digit MOS to LED Cathode Driver		
	DS8872	National
	DS8920	National
	DS8973	National
	DS8975	National
	SN75498	TI
9-Digit MOS to LED Cathode Driver, with Low Battery Indicator	DS8864	National
	DS8873	National
9-Digit MOS to LED Cathode Driver with Shift Register Decoding	DS8874	National
9-Line, 30 LED	U1096B	Telefunken
9-Segment LED Driver (low voltage)		
	DS8647	National
	DS8648	National
10-Bit High-Voltage, High-Current		
	S4534	**AMI (2811)**
10-Bit Serial In/Parallel Out Fluorescent (for μP systems)		
	UCN-4810A	Sprague
	UCN4810A	TI
10-Digit, 7-Segment Triplexed LCD Decoder/Driver		
	ICM7232	**Intersil (798)**
11-Segment LED Display Drivers		
	MM5485	National
12-Line Vacuum Fluorescent		
	SN75512A	TI
	SN75513A	TI
	SN75514	TI

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Display Drivers (Cont'd)

Display Drivers (Cont'd)

Function	Device	Source	
14-Digit Decoder/Driver	DS8665	National	
	DS8666	National	
14-Digit Decoder/Driver, with Low Battery Indicator	DS7664	† National	
	DS8664	National	
14-Segment Decoder/Driver, Interface to CPU	MN1205H	Panasonic	
16-Line Fluorescent	DS8881	National	
	8881	Signetics	
16-Segment LED Display Drivers	MM5484	National	
18-Segment Alphanumeric	AC5947	TI	
18-Segment, 16-Character Alphanumeric (30, 35 and 40 volt versions)	10937	Rockwell	
30-Bit LCD Driver/Register	MD4330B	Mitel	
32 Segment LCD	MM5452	National	
	MM5453	National	
	PCE2112	Signetics	
32-Bit High-Voltage	**S4521**	**AMI**	**(2810)**
	S4535	**AMI**	**(2812)**
32-Bit LCD	MM58438	National	
32-Line AC Plasma Display Axis Driver	SN75500A	TI	
	SN75501C	TI	
32-Line Vacuum Fluorescent	SN75518	TI	
32-Segment LCD Controller/Driver	μPD7255	NEC	
32-Segment LCD Driver	MM5483	National	
40-Segment LCD Duplex	PCE2100	Signetics	
60-Segment LCD Duplex	PCE2110	Signetics	
64-Segment LCD Duplex	PCF2111	Signetics	

† Military Temperature Range (−55° to 125°C)

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INTERFACE–Error Checking Circuits

Function	Max. Serial Data Rate, MHz	Supply Voltage, V	Device	Source
Error Checking Circuits				
CRC Generator/Checker	2 *	5	COM8004	SMC
	3	5	MC8500	Motorola
			SSI8500	**SiliconSys (4208)**
	10	5	9401C	Fairchild
			9401M	† Fairchild
			8X01A	Signetics
	12	5	54F401	† Fairchild
			74F401	Fairchild
			N9401	**Signetics (1656)**
			S9401	**† Signetics (1656)**
CRC Generator/Checker (expandable)	20	5	**54F402**	**Fairchild (738)**
			54F492	Fairchild
			74F402	**Fairchild (738)**
			74F492	Fairchild
Deskew-Queue Register	3 *	5	MC8520	Motorola
			SSI8520	**SiliconSys (4208)**
Error Detection and Support Logic, for Winchester Disk System	5	5	**WD1014**	**Western (1724)**
Error Detection/Correction Circuit	—	5	8206	Intel
			WD8206	**Western (4260)**
Error Detection/Correction Circuit (ECL)	—	−5.2	MC10163	Motorola
			MC10193	Motorola
			MC10563	† Motorola
			MC10593	Motorola
Error Detection/Correction Circuit (TTL)	—	5	54F416	Fairchild
			54F418	† Fairchild
			54F630	Fairchild
			54F631	Fairchild
			74F416	Fairchild
			74F418	Fairchild
			74F630	Fairchild
			74F631	Fairchild
			9428	Fairchild
			MC74F2960	**Motorola (822)**
			SN74ALS790	**Motorola (823)**
			MM54ALS632†	National
			MM54ALS633†	National
			MM54ALS634†	National
			MM54ALS635†	National
			MM74ALS632	National
			MM74ALS633	National
			MM74ALS634	National
			MM74ALS635	National
			54F630	**† Signetics (888)**
			54F631	**† Signetics (888)**
			74F630	**Signetics (880,888)**
			74F631	**Signetics (880,888)**
			SN54ALS632	**† TI (1070,374)**
			SN54ALS633	**† TI (374,1070)**
			SN54ALS634	**† TI (374,1071)**
			SN54ALS635	**† TI (374,1071)**
			SN54LS630	**† TI (1069)**
			SN54LS631	**† TI (1069)**
			SN54LS636	**† TI (1072,1153)**
			SN54LS637	**† TI (1072,1153)**
			SN74ALS632	**TI (374,1070)**
			SN74ALS633	**TI (374,1070)**
			SN74ALS634	**TI (374,1071)**
			SN74ALS635	**TI (374,1071)**
			SN74LS630	**TI (1069)**
			SN74LS631	**TI (1069)**
			SN74LS636	**TI (1072,1153)**
			SN74LS637	**TI (1072,1153)**
		7	MB1412A	Fujitsu
Error Detection/Correction Circuit (TTL), Serial Burst	—	5	54F430	Fairchild
			74F430	Fairchild

† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE–Error Checking Circuits (Cont'd)

Function	Max. Serial Data Rate, MHz	Supply Voltage, V	Device	Source
Error Checking Circuits				**(Cont'd)**
Error Detection/Correction Circuit, 32-Bit Memory	—	5	**54F418**	† **Fairchild** (757)
			74F418	**Fairchild** (757)
Error Pattern Register	3	5	MC8501	Motorola
Expandable Error Checker and Corrector	—	5	**DP8400**	**National** (1514)
			DP8400	TI
LRCC Data Register	3	5	MC8502	Motorola
			SSI8502	**SiliconSys** (4208)
Polynominal Generator	4 *	5	MC8506	Motorola
Polynominal Generator/Checker	3.5 *	5	**MC2653**	**Motorola** (1512)
			MC68653	**Motorola** (1506,1512)
			MC8503	Motorola
			SCN68653	**Signetics** (1671)
	4	5	**SCN2653**	**Signetics** (1671)
Universal Polynominal 4-Bit Generator	17 *	5	MC8504	Motorola
Single Error Hamming Code Detector and Generator	—	5	MC4041	Motorola

† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE–Keyboard Encoder-Decoders

No. of Keys	No. of Output Bits	Code	Max. Clock Rate, KHz	Supply Voltage, V	Comments	Device	Source
Keyboard Encoder- Decoders							
16	4	Binary	—	3-15	2 key rollover, 3 state output	MM54C922 MM74C922	† National National
		External ROM Programmable	—	5	Antibounce, mute, interlock	M190	SGS
		1 of 16	—	5	Strobe output, key rollover output, 2 of 8 keyboard to binary encoder, one of four row inputs and column inputs (telephone key pads) give binary output, strobe.	**HD0165** **MC14419**	**Harris** (2979) **Motorola** (3536)
20	5	Binary	—	3-15	2 key rollover, 3 state output	MM54C923 MM74C923	† National National
85	8	ASCII/HEX	1000	4-10.5	Scans and generates code for 53 key ASCII plus 32 non-ASCII keys	**CDP1871A**	**RCA** (1595)
				4-6.5	Scans and generates code for 53 key ASCII plus 32 non-ASCII keys	**CDP1871AC**	**RCA** (1595)
88	8 plus Parity	Mask, Programmable	100	−12.5	Programmable parity, strobe width, strobe delay. Two key rollover. 8 x 11 matrix, 3 levels.	KR2376	SMC
90	10	External ROM Programmable	100	−12.5	9 x 10 matrix, 4 Mode, 2 or N key rollover	KR3600-PRO	SMC
		Mask, Programmable	100	−12.5	9 x 10 matrix, 4 Mode, 2 or N key rollover	KR3600	SMC
112	10	Mask Programmable	66	5	112 bits for internal programming of function keys	AY3-4592	GI
128	8	Mask Programmable	400	5	16 x 18 matrix, 8-Bit bus interface, 4 rollover modes, UART on chip	**SCN2671A**	**Signetics** (1678)
	9	Mask Programmable	100	5	16 x 18 matrix, three-state I/O, 2 or 3 key alarm	**MSM3914A**	**OKI** (4118)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE-Line Circuits

Line Drivers—Single Ended

No. Per Device	Output	Party Line	Supply Voltage, V	Comments	Device	Source
2	High Current	Yes	5	Coax/Twisted Pair	MC8T23	Motorola
					DS75123	National
					N8T23	**Signetics (876)**
					N8T23	TI
					SN75123	TI
				Emitter Follower for Coax/Twisted Pair	MC8T13	Motorola
					DS55121	† National
					DS75121	National
					N8T13	**Signetics (876)**
					S8T13	**Signetics (876)**
					N8T13	TI
					SN55121	† TI
					SN75121	TI
	−0.5 to 5.5 V	No	5	RS422A, RS423A	μA9639C	TI
	±4 to 6 V	No	±9 to ±15	RS232, RS423, CCITT V.26, V.28	9636AC	Fairchild
					9636AM	† Fairchild
					μA9636AC	TI
	±6 V	No	±12	4 Input	**N8T15**	**Signetics (876)**
	±8 V	No	±12	RS232C	75150	Fairchild
					DS75150	National
					SN55150	† TI
					SN75150	TI
3	High Current	No	5	IBM360	HD2904	Hitachi
	±6 V	No	±12	RS232B/C, CCITT, MIL188	9616	Fairchild
					9616E	Fairchild
					9616M	† Fairchild
4	TTL	Yes	5	DS7831 w/o Vcc Clamp	DS7832	† National
					DS8832	National
					DS8832	TI
				Three-State	**N8T09**	**Signetics (876)**
					S8T09	**† Signetics (876)**
				2-Input NAND, 80 Ma	96101C	Fairchild
					96101M	† Fairchild
				4-Input AND, NAND	DS7831	† National
					DS8831	National
					DS8831	TI
	0.15 to 4 V	No	5	IBM360/370	**MC3481**	**Motorola (3064,3065)**
					MC3485	**Motorola (3064,3065)**
	3.11	No	5	IBM360/370	SN75126	TI
					SN75130	TI
	−7 to 12	Yes	5	RS422, Three-State	SN75174	TI
	−7 to ±12	Yes	5	RS422, Three-State	SN75172	TI
	±4 to 6 V	No	±5	RS423, RS422 with mode control	DS3691	National
			±5.5	RS423, RS422 with mode control	DS1691	† National
		Yes	±5	RS423, Three-State	AM26LS29C	AMD
					AM26LS29	Signetics
			±5.5	RS423, Three-State	AM26LS29M	† AMD
	±6 to 9 V	No	±9 to ±15	RS232C, CCITT V.24	**XR1488**	**Exar (3384)**
					μA1488	Fairchild
					HD75188	Hitachi
					MC1488	**Motorola (3064)**
					DS1488	National
					MC1488	Signetics
					SG1488	SiliconG
					MC1488	TI
					SN55188	† TI
					SN75188	TI
	±4 to 6 V	No	±5	RS423, RS422 with mode control	AM26LS30C	AMD
					AM26LS30	Signetics
			±5.5	RS423, RS422 with mode control	AM26LS30M	† AMD
6	NTDS	No	5, −15	NTDS	MOA-268B	† Interdesign
			5, −5	NTDS Hex Driver	MOF1305B	† Interdesign

† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE–Line Circuits (Cont'd)

Line Drivers—Single Ended (Cont'd)

No. Per Device	Output	Party Line	Supply Voltage, V	Comments	Device	Source	
8	TTL	Yes	5	Three-State (also see index for 74S244, 74LS244, 67S304, 67LS304)	54LS241	† Fairchild	
					54LS541	† Fairchild	
					74LS241	Fairchild	
					74LS244	Fairchild	
					74LS541	Fairchild	
					HD74LS241	Hitachi	
					HD74LS244	Hitachi	
					M74LS241	Mitel	
					M74LS244	Mitsubishi	
					SN54LS241	**† MMI**	**(804)**
					SN54LS244	**† MMI**	**(804)**
					SN54LS245	**† MMI**	**(804)**
					SN54LS341	**† MMI**	**(804)**
					SN54LS344	**† MMI**	**(804)**
					SN54S241	**† MMI**	**(804)**
					SN54S244	**† MMI**	**(804)**
					SN74LS241	**MMI**	**(804)**
					SN74LS244	**MMI**	**(804)**
					SN74LS245	**MMI**	**(804)**
					SN74LS341	**MMI**	**(804)**
					SN74LS344	**MMI**	**(804)**
					SN74S241	**MMI**	**(804)**
					SN74S244	**MMI**	**(804)**
					SN54LS241	† Motorola	
					SN54LS244	† Motorola	
					SN54LS541	† Motorola	
					SN74LS241	Motorola	
					SN74LS244	Motorola	
					SN74LS541	Motorola	
					DM54S241	† National	
					DM74LS241	National	
					DM74LS244	National	
					DM74S241	National	
					MM54C941	† National	
					MM74C941	National	
					74LS241	Signetics	
					74LS244	Signetics	
					74LS541	Signetics	
					SN54ALS241	**† TI**	**(999)**
					SN54ALS244	**† TI**	**(1000)**
					SN54ALS541	**† TI**	**(1050)**
					SN54AS241	**† TI**	**(999)**
					SN54LS241	† TI	
					SN54LS244	† TI	
					SN54LS541	**† TI**	**(1050)**
					SN54S241	† TI	
					SN74ALS241	**TI**	**(999)**
					SN74ALS244	**TI**	**(1000)**
					SN74ALS541	**TI**	**(1050)**
					SN74AS241	**TI**	**(999)**
					SN74LS241	TI	
					SN74LS244	TI	
					SN74LS541	**TI**	**(1050)**
					SN74S241	TI	
				Three-State, Inverting	**54F240**	**† Fairchild**	**(729)**
					54LS240	† Fairchild	
					54LS540	† Fairchild	
					74F240	**Fairchild**	**(729)**
					74LS240	Fairchild	
					74LS540	Fairchild	
					M74LS240	Mitsubishi	
					SN54LS240	**† MMI**	**(804)**
					SN54LS340	**† MMI**	**(804)**
					SN54S240	**† MMI**	**(804)**
					SN74LS240	**MMI**	**(804)**
					SN74S240	**MMI**	**(804)**
					SN54LS240	† Motorola	
					SN54LS540	† Motorola	
					SN74LS240	Motorola	
					SN74LS540	Motorola	

(Continued)

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INTERFACE–Line Circuits (Cont'd)

Line Drivers—Single Ended (Cont'd)

No. Per Device	Output	Party Line	Supply Voltage, V	Comments	Device	Source	
8	TTL	Yes	5	Three-State, Inverting			(Cont'd)
					DM54S240	† National	
					DM74S240	National	
					54LS540	† Signetics	
					74LS240	Signetics	
					74LS540	Signetics	
					SN54ALS240	† TI	**(998)**
					SN54ALS540	† TI	**(1050)**
					SN54AS240	† TI	**(998)**
					SN54LS240	† TI	
					SN54LS540	† TI	**(1050)**
					SN54S240	† TI	
					SN74ALS240	TI	**(998)**
					SN74ALS540	TI	**(1050)**
					SN74AS240	TI	**(998)**
					SN74LS240	TI	
					SN74LS540	TI	**(1050)**
					SN74S240	TI	
16	TTL	Yes	5	Three-State	**SN54LS365A**	† TI	**(1023)**
					SN54LS367A	† TI	**(1024)**
					SN74LS365A	TI	**(1023)**
					SN74LS367A	TI	**(1024)**
				Three-State, Inverting	**SN54LS366A**	† TI	**(1023)**
					SN54LS368A	† TI	**(1024)**
					SN74LS366A	TI	**(1023)**
					SN74LS368A	TI	**(1024)**

Line Drivers—Differential

See also Drivers under digital logic families

No. Per Device	Output	Party Line	Supply Voltage, V	Comments	Device	Source	
2	High Current CMOS						
		No	3-15	CMOS 50 mA, 4-Input AND, NAND	MM78C30	† National	
					MM88C30	National	
	High Current TTL	No	5	40 mA, Active Pull-up/Pull-down	9612C	Fairchild	
				40 mA, Open Collector/Active Pull-up	9614C	Fairchild	
					9614M	† Fairchild	
					DS55114	† National	
					DS75114	National	
					9614C	TI	
					SN55114	† TI	
					SN75114	TI	
				40 mA, RS422	SN55128	† TI	
					SN75158	TI	
				40 mA, 4-Input AND, NAND	54S140	† Fairchild	
					74S140	Fairchild	
					HD74S140	Hitachi	
					DM74S140	National	
					DS7830	† National	
					DS8830	National	
					54S140	**† Signetics**	**(531)**
					74S140	Signetics	
					DS8830	TI	
					SN54S140	† TI	**(969)**
					SN55183	† TI	
					SN74S140	TI	**(969)**
					SN75183	TI	
		Yes	5	Three-State	DS7831	† National	
					DS8831	National	
					DS8831	TI	
				DS7831 w/o Vcc Clamp	DS7832	† National	
					DS8832	TI	
				40 mA, Open Collector/Active Pull-Up, Three-State	DS55113	† National	
					DS75113	National	
					SN55113	† TI	
					SN75113	TI	
				40 mA, RS422, Three-State	9634C	Fairchild	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Line Circuits (Cont'd)

Line Drivers—Differential (Cont'd)

No. Per Device	Output	Party Line	Supply Voltage, V	Comments	Device	Source	
2	High Current TTL	Yes	5	40 mA, RS422, Three-State			(Cont'd)
					9634M	† Fairchild	
					DS8832	National	
					SN75159	TI	
	2.5 to 3.5	No	5	High Speed	μA9638C	TI	
	3.5 mA	Yes	±5	Twisted Pair	HD75109	Hitachi	
					MC75109	Motorola	
					SN55109A	† TI	
					SN74109A	**TI**	**(958)**
	6.5 mA	Yes	±5	Twisted Pair, Level Shifting	55110A	† Fairchild	
					75110A	Fairchild	
					HD75110	Hitachi	
					MC75110	Motorola	
					MC75S110	Motorola	
					SN55110A	† TI	
					SN75110A	TI	
	18 mA	Yes	±5	Higher Current 75110	SN75112	TI	
	±3 V	Yes	±5	RS422 at Low Data Rates, RS423	AM26LS30C	AMD	
					AM26LS30	Signetics	
			±5.5	RS422 at Low Data Rates, RS423	AM26LS30M	† AMD	
	±5V	No	±15, ±5	ARING 429, 1000K bits data rate	**HS3182**	**† Harris**	**(4644)**
4	High Current CMOS	No	3-15	CMOS, 25 mA	MM78C29	† National	
					MM88C29	National	
	High Current TTL	No	5	50 Ohm Lines	**74128**	**Signetics**	**(861)**
					SN74128	**TI**	**(964)**
				75 Ohm Lines	**54128**	**† Signetics**	**(861)**
					SN54128	**† TI**	**(964)**
		Yes	5	RS-422, RS-423, Three-State	**MC3487**	**Motorola**	**(3064)**
					DS3487	National	
					MC3487	TI	
				Three-State	DS1688	† National	
	11 mA	Yes	±5	Quad 75110	MC3453A	Motorola	
	20 mA	Yes	5	MIL 188-114, Three-State	DS1692	† National	
					DS3692	National	
				RS-422, Three-State	AM26LS31C	AMD	
					AM26LS31M	† AMD	
					AM26LS31	**Motorola**	**(3064)**
					AM26LS31C	**Motorola**	**(3064)**
					AM26LS31M	**† Motorola**	**(3064)**
					DS26LS31C	† National	
					DS26LS31M	National	
					AM26LS31	Signetics	
					AM26LS31C	TI	
					AM26LS31M	† TI	
	40 mA	Yes	5	RS-422, Fed. 1020, Three-State	SN75151	TI	
					SN75153	TI	

† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE–Line Circuits (Cont'd)

No. Per Device	Receiver Input Threshold	Common Mode Voltage, V	Supply Voltage, V	Comments	Device	Source	
Line Receivers—Single Ended							
Also see Line Receivers-Differential							
2	±0.1 V (ref)		5	Ext. Ref. Adj. 1.5 to 3.5 V with Optional Internal 2.5 V Reference	SN55142A	† TI	
					SN55143A	† TI	
					SN75142A	TI	
					SN75143A	TI	
				Ext. Reference Adjustable from 1.5 to 3.5 V	SN55140	† TI	
					SN55141	† TI	
					SN75140	TI	
					SN75141	TI	
	±2.0		5	Hysteresis, EIA/MIL	**N8T16**	**Signetics**	**(876)**
				RS232B	DS7822	† National	
					DS8822	National	
3	0.7 to 1.7		5	Hysteresis, IBM360/370	MC8T24	Motorola	
					DS75124	National	
					N8T24	**Signetics**	**(876)**
					SN75124	TI	
	0.75 to 2.25		5	Hysteresis, RS232C, CCITT V.24	9617C	Fairchild	
	0.8 to 2.0 V		5	Hysteresis, High-Speed	MC8T14	Motorola	
					DS55122	† National	
					DS75122	National	
					N8T14	Signetics	
					SN55122	† TI	
					SN75122	TI	
	0.86 to 2.40		5	High-Speed	HD2915	Hitachi	
	1.15 to 1.55		5	IBM360	HD2905	Hitachi	
4	0.75 to 1.5 V		5	RS232C, Programmable Threshold, Hysteresis	μA1489	Fairchild	
					HD75154	Hitachi	
					MC1489	**Motorola**	**(3064)**
					DS1489	National	
					MC1489	Signetics	
					SG1489	SiliconG	
					SN55189	† TI	
					SN75189	TI	
	0.75 to 2.25		5	RS232C, Programmable Threshold, Wider Hysteresis than 1489	**XR1489A**	**Exar**	**(3384)**
					μA1489A	Fairchild	
					HD75189	Hitachi	
					MC1489A	**Motorola**	**(3064)**
					DS1489A	National	
					MC1489A	Signetics	
					SG1489A	SiliconG	
					SN55189A	† TI	
	0.97 to 2.65		5	Hysteresis, 120 Ohm System	DS7836	† National	
	1.05 to 2.5		5	Hysteresis, 120 Ohm System	DS8836	National	
	1.2 to 1.8		5	120 Ohm System, No Hysteresis, NOR Input	DS7640	† National	
	1.3 to 1.7		5	120 Ohm System, No Hysteresis, NOR Input	DS8640	National	
	1.7		5	No Hysteresis, NOR Input	96106	Fairchild	
	1.75 to 2.25 V		5	RS232C, Programmable Threshold, Hysteresis	SN75189A	TI	
	5 to 7.5		15	Hysteresis, Interface to CMOS	367A	TeledyneS	
					367M	† TeledyneS	
				Hysteresis, Open Collector, Interface to CMOS	368A	TeledyneS	
	5.5 to 8		12	Hysteresis, Open Collector, Interface to CMOS	368C	TeledyneS	
				Hystersis, Interface to CMOS	367B	TeledyneS	
					367C	† TeledyneS	
	±3/0.8 to 3		5 or 12	RS232C, Hysteresis, Fail Safe Option	55154	† Fairchild	
					75154	Fairchild	
					DS75154	National	
					SG75154	SiliconG	
					SN54154	**† TI**	**(973)**
					SN75154	TI	
6	0.97 to 2.65		5	Hysteresis, 120 Ohm System	DS7837	† National	
	1.05 to 2.50		5	Hysteresis, 120 Ohm System	MC3437	Motorola	
					DS8837	National	
					N8T37	**Signetics**	**(876)**
	− 1 to 4.5/-1.5 to 13		5	NTDS	MOB-272	† Interdesign	

† Military Temperature Range (− 55° to 125°C)

* Typical Value

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INTERFACE-Line Circuits (Cont'd)

No. Per Device	Receiver Input Threshold	Common Mode Voltage, V	Supply Voltage, V	Comments	Device	Source
Line Receivers—Single Ended						**(Cont'd)**
7	0.7 to 1.7		5	IBM360/370	**MC75125**	**Motorola (3064)**
					MC75127	Motorola
					DS75125	National
					DS75127	National
					SN75125	TI
					SN75127	TI
8	0.7 to 1.7		5	IBM360/370	MC75128	Motorola
					MC75129	Motorola
					DS75128	National
					DS75129	National
					SN75128	TI
					SN75129	TI
Line Receivers—Differential						
See also Receivers-listed under Digital-ECL and Digital-HNIL/HTL Miscellaneous sections						
2	±0.010	±3	±5	10 mV, MOS Sense, Active Pull-up	DS75207	National
					DS75208	National
					SN75207	TI
				10 mV, MOS Sense, Open Collector	SN75208	TI
				10 mV, MOS Sense, Three-State	DS3604	National
				75207 with Diode Protected Input Stage.	SN75207B	TI
				75208 with Diode Protected Input Stage	SN75208B	TI
	±0.025 *	±3	±5	25 mV, Active Pull-up	55107A	† Fairchild
					75107A	Fairchild
					HD75107A	Hitachi
					MC55107	† Motorola
					MC75107	Motorola
				25 mV, Active Pull-Up	DS55107	† National
					DS75107	National
				25 mV, Active Pull-up	SN55107A	† TI
					SN75107A	TI
				25 mV, Open Collector	HD75108A	Hitachi
					MC55108	† Motorola
					MC75108	Motorola
					DS55108	† National
					DS75108	National
					SN55108A	† TI
					SN75108A	TI
				25 mV, Three-State 55107	DS1603	† National
					DS3603	National
				55107A with Diode Protected Input Stage	75107B	Fairchild
					DS55107	† National
					DS75107	National
					SN55107B	† TI
					SN75107B	TI
				55108A with Diode Protected Input Stage	75108B	Fairchild
					DS55108	† National
					DS75108	National
					SN55108B	† TI
					SN75108B	TI
	±0.2/0.3	±10/15	5	Twisted Pair, ±15 V CMV. Response Control	DS78LS120	† National
					DS88LS120	National
		±15	5	CMOS Compatible, Response Control	DS78C120	† National
					DS88C120	National
	±0.2/0.5	±7/15	5	RS232, RS422/3	9637AC	Fairchild
					9637AM	† Fairchild
					SN55157	† TI
					SN75157	TI
					μA9637AC	TI
	±0.3/0.3	±0/15	5	±15 V CMV, Response Control	DS78L20	† National
	±0.5/1	±0/15	5	±15 V CMV, Response Control	9615C	Fairchild
					9615M	† Fairchild
					DS55115	† National
					DS75115	National
					9615C	TI

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE–Line Circuits (Cont'd)

Line Receivers—Differential (Cont'd)

No. Per Device	Receiver Input Threshold	Common Mode Voltage, V	Supply Voltage, V	Comments	Device	Source
2	±0.5/1	±0/15	5	±15 V CMV, Response Control	(Cont'd)	
					SN55115	† TI
					SN75115	TI
		±3/15	5	Twisted Pair, ±3/15 V CMV, Response Control	DS7820A	† National
					DS8820A	National
					DS8820	TI
					SN55152	† TI
					SN55182	† TI
					SN75182	TI
		±10/15	5	Twisted Pair, ±15 V CMV, Response Control	DS7820	† National
					DS78C20	† National
					DS8820	National
					DS88C20	National
	±0.5/3	±25	±12	Adjusts RS232C/MIL-188, ±25 V CMV, Hysteresis	SN75152	TI
4			±15/12-24	Quad Comparator, 3mV Hysteresis	ESM1600	Thomson-CSF
					ESM1602	Thomson-CSF
	±0.025	±3	±5	Four 75107, Active Pull-up	MC3450	Motorola
					DS1650	† National
					DS3650	National
				Four 75108, Open Collector	MC3452	Motorola
					DS1652	† National
					DS3652	National
	±0.2	±3	±5	Three-State, RS422/423	**MC3486**	**Motorola (3064)**
					DS3486	National
					MC3486	TI
		±7	±5	Three-State, RS-422/423	AM26LS32C	AMD
					AM26LS32M	† AMD
					DS26LS32C	National
					DS26LS32M	† National
					AM26LS32C	TI
					AM26LS32M	† TI
		±12	±5	Three-State, RS-422	SN55173	† TI
					SN75173	TI
					SN75175	TI
		±15	±5	50 mV Hysteresis	DS1689	† National
					DS1690	† National
					DS3689	National
					DS3690	National
	±0.5	±15	±5	Three-State	AM26LS33C	AMD
					AM26LS33M	† AMD
					DS26LS33C	National
					DS26LS33M	† National
					AM26LS33C	TI
					AM26LS33M	† TI
	±0.8	−12, ±7.5	±5, −5	NTDS	MOF1623B	† Interdesign

† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE–Line Circuits (Cont'd)

No. Per Device	Receiver Input Threshold, V	Output	Supply Voltage, V	Comments	Device	Source	
Line Transceivers—Single Ended							
4	0.05 to 2.50	TTL	5	Open Collector, 1 V Hysteresis	MC3438	Motorola	
					DS8838	National	
					N8T38	**Signetics**	**(876)**
	0.21 to 1.84	TTL	5	Open Collector (Inverting), Common Enable	96103M	† Fairchild	
	0.4 to 2.05	TTL	5	Open Collector, Hysteresis	AM26S12AC	AMD	
					AM26S12AM	† AMD	
	0.5 to 2.0	TTL	5	Bus Transceiver, Tridirectional, Open Collector	**SN54LS440**	**† TI**	**(1035,1036)**
					SN54LS441	**† TI**	**(1035,1036)**
					SN54LS448	**† TI**	**(1039)**
				Bus Transceiver, Tridirectional, Three-State	**SN54LS442**	**† TI**	**(1035,1036)**
					SN54LS443	**† TI**	**(1035,1036)**
					SN54LS444	**† TI**	**(1035,1036)**
	0.6 to 2.0	TTL	5	Bus Transceiver, Tridirectional, Open Collector	**SN74LS440**	**TI**	**(1035,1036)**
					SN74LS441	**TI**	**(1035,1036)**
					SN74LS448	**TI**	**(1039)**
				Bus Transceiver, Tridirectional, Three-State	**SN74LS442**	**TI**	**(1035,1036)**
					SN74LS443	**TI**	**(1035,1036)**
					SN74LS444	**TI**	**(1035,1036)**
				General Purpose Interface Bus, Open Collector, for MOS Input	**MC3446A**	**Motorola**	**(3064)**
					MC3446	TI	
	0.7 to 2.0	TTL	5	Three-State, Bus Transceiver	**AM2915AM**	**† AMD**	**(1411)**
				Three-State, Bus Transceiver, Parity Generator/Checker	**AM2916AM**	**† AMD**	**(1411)**
					AM2917AM	**† AMD**	**(1412)**
				Three-State, Hysteresis	54LS242	† Fairchild	
					54LS243	† Fairchild	
					SN54LS242	† Motorola	
					SN54LS243	† Motorola	
					SN54ALS242	**† TI**	**(999)**
					SN54ALS243	**† TI**	**(1000)**
					SN54LS242	† TI	
					SN54LS243	† TI	
	0.8 to 1.8	TTL/MOS	5	Bus Transceiver, Individual Direction Controls	**SN54LS446**	**† TI**	**(1038)**
					SN54LS449	**† TI**	**(1039)**
				General Purpose Interface Bus, Bidirectional Bus Transceiver, Three-State	AM3448A	AMD	
					μA3448A	Fairchild	
					MC3448A	**Motorola**	**(3064)**
	0.8 to 2.0	TTL	5	Bus Transceiver, Individual Direction Controls	**SN74LS446**	**TI**	**(1038)**
					SN74LS449	**TI**	**(1039)**
				General Purpose Interface Bus, Open Collector, 100 mA Output	DS8641	Motorola	
					MC3440A	**Motorola**	**(3064)**
					MC3441A	Motorola	
					MC3443A	Motorola	
					DS3662	National	
					DS7641	† National	
					DS8641	National	
					MC3443	TI	
				Three-State, Bus Transceiver	**AM2915AC**	**AMD**	**(1411)**
				Three-State, Bus Transceiver, Parity Generator/Checker	**AM2916AC**	**AMD**	**(1411)**
					AM2917AC	**AMD**	**(1412)**
				Three-State, Dual Rank Latches	**SN74S226**	**TI**	**(996)**
				Three-State, Hysteresis	74LS242	Fairchild	
					74LS243	Fairchild	
					HD74LS242	Hitachi	
					M74LS242	Mitel	
					M74LS243	Mitel	
					SN74LS242	Motorola	
					SN74LS243	Motorola	
					DM74LS242	National	
					DM74LS243	National	
					74LS242	Signetics	
					74LS243	Signetics	
					SN74ALS242	**TI**	**(999)**
					SN74ALS243	**TI**	**(1000)**
					SN74LS242	TI	
					SN74LS243	TI	
				Three-State (Inverting)	μA8T26A	Fairchild	

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† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE–Line Circuits (Cont'd)

Line Transceivers—Single Ended (Cont'd)

No. Per Device	Receiver Input Threshold, V	Output	Supply Voltage, V	Comments	Device	Source	
4	0.8 to 2.0	TTL	5	Three-State (Inverting) (Cont'd)	μA8T26AM	† Fairchild	
					HD268T26	Hitachi	
					MC6880	Motorola	
					MC8T26A	Motorola	
					DS8T26A	National	
					DS8T26AM	† National	
					N8T126	**Signetics**	**(876)**
					N8T127	**Signetics**	**(876)**
					N8T26A	**Signetics**	**(876)**
					S8T126	**† Signetics**	**(876)**
					S8T127	**† Signetics**	**(876)**
					SN75136	TI	
				Three-State (Non-Inverting)	μA8T28	Fairchild	
					μA8T28M	† Fairchild	
					MC6889	Motorola	
					MC8T28	Motorola	
					DS8T28	National	
					DS8T28M	† National	
					N8T128	**Signetics**	**(876)**
					N8T129	**Signetics**	**(876)**
					N8T28	**Signetics**	**(876)**
					S8T128	**† Signetics**	**(876)**
					S8T129	**† Signetics**	**(876)**
	0.97 to 2.65	TTL	5	Open Collector, 1 V Hysteresis	AM7838	† AMD	
					DS7838	† National	
	1.05 to 2.50	TTL	5	Inverting 7833/8833	DS7835	† National	
					DS8835	National	
				Inverting 7839/8839	DS7834	† National	
					DS8834	National	
					N8T34	**Signetics**	**(876)**
				Three-State, NOR Gate, Transmit Disable, Hysteresis	DS7839	† National	
					DS8839	National	
				Three-State, T/R Disables, Hysteresis	DS7833	† National	
					DS8833	National	
	1.5 to 2.4	TTL	5	Open Collector, 100 mA Output, Parity Generator/Checker	**AM2907M**	**† AMD**	**(1406)**
				Q-bus Compatible 2907	**AM2908M**	**† AMD**	**(1406)**
				2-Input, Open Collector 100 mA Drivers	**AM2905M**	**† AMD**	**(1405)**
				2-Input, Open Collector 100 mA Drivers, Parity Generator/Checker	**AM2906M**	**† AMD**	**(1405)**
	1.5 to 3.2	TTL	5	Open Collector, 100 mA Output	SN55138	† TI	
	1.6 to 1.8	TTL	5	Open Collector, Hysteresis	AM26S12C	AMD	
					AM26S12M	† AMD	
	1.6 to 2.3	TTL	5	Open Collector, 100 MA Output, Parity Generator/Checker	**AM2907C**	**AMD**	**(1406)**
				Q-bus Compatible 2907	**AM2908C**	**AMD**	**(1406)**
				2-Input, Open Collector 100 mA Drivers	**AM2905C**	**AMD**	**(1405)**
				2-Input, Open Collector 100 mA Drivers, Parity	**AM2906C**	**AMD**	**(1405)**
	1.6 to 2.4	TTL	5	Open Collector, 100 mA Output	AM26S10M	† AMD	
					AM26S11M	† AMD	
					9640M	† Fairchild	
					DS26S10M	† National	
					DS26S11M	† National	
					AM26S10M	† TI	
					AM26S11M	† TI	
	1.75 to 2.25	TTL	5	Open Collector, 100 mA Output	AM26S10C	AMD	
					AM26S11C	AMD	
					9640C	Fairchild	
					MC26S10	Motorola	
					MC26S11	Motorola	
					DS26S10C	National	
					DS26S11C	National	
					AM26S10C	TI	
					AM26S11C	TI	
	1.8 to 2.9	TTL	5	Open Collector, 100 mA Output	SN75138	TI	

† Military Temperature Range (−55° to 125°C)   * Typical Value

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INTERFACE–Line Circuits (Cont'd)

Line Transceivers—Single Ended (Cont'd)

No. Per Device	Receiver Input Threshold, V	Output	Supply Voltage, V	Comments	Device	Source	
8	—	TTL/CMOS	5	**General Purpose Interface Bus**	DS3666	National	
					DS75160A	National	
					DS75161A	National	
					DS75162A	National	
	TTL	TTL	5	Bidirectional Bus Transceiver, Three-State	DP7304B	† AMD	
					DP8304B	AMD	
					DP8304	National	
	0.5 to 2.0	TTL	5	**Bidirectional Bus Transceiver, Open Collector**	54LS641	† Signetics	
					54LS642	† Signetics	
					74LS641	Signetics	
					74LS641-1	Signetics	
					74LS642	Signetics	
					74LS642-1	Signetics	
					SN54LS621	**† TI**	**(1066)**
					SN54LS622	**† TI**	**(1066)**
					SN54LS641	**† TI**	**(1074)**
					SN54LS642	**† TI**	**(1074)**
					SN54LS644	**† TI**	**(1074)**
				Bidirectional Bus Transceiver, Three-State	DP7303	† AMD	
					DP7307	† AMD	
					DP7308	† AMD	
					DP8303	AMD	
					DP8307	AMD	
					DP8308	AMD	
					SN54LS645	**† MMI**	**(804)**
					SN54LS645-1	**† MMI**	**(804)**
					DP7303	† National	
					DP7304B	† National	
					DP7307	† National	
					DP7308	† National	
					DP8303	National	
					DP8304B	National	
					DP8307	National	
					DP8308	National	
					SN54ALS1645	**† TI**	**(1124)**
					SN54ALS245	**† TI**	**(1001)**
					SN54ALS645	**† TI**	**(1074)**
					SN54LS620	**† TI**	**(1066)**
					SN54LS623	**† TI**	**(1066)**
					SN54LS640	**† TI**	**(1074)**
					SN54LS643	**† TI**	**(1074,1074,1075)**
					SN54LS645	**† TI**	**(1074)**
					SN54SL245	† TI	
	0.6 to 2.0	TTL	5	Bidirectional Bus Transceiver, Open Collector	**SN74LS621**	**TI**	**(1066)**
					SN74LS622	**TI**	**(1066)**
					SN74LS641	**TI**	**(1074)**
					SN74LS641-1	**TI**	**(1074)**
					SN74LS642	**TI**	**(1074)**
					SN74LS642-1	**TI**	**(1074)**
					SN74LS644	**TI**	**(1074)**
					SN74LS644-1	**TI**	**(1074)**
				Bidirectional Bus Transceiver, Three-State	**SN74LS645**	**MMI**	**(804)**
					SN74LS645-1	**MMI**	**(804)**
					74LS640	Signetics	
					74LS640-1	Signetics	
					74LS645	Signetics	
					SN74LS245	TI	
					SN74LS620	**TI**	**(1066)**
					SN74LS623	**TI**	**(1066)**
					SN74LS640	**TI**	**(1074)**
					SN74LS640-1	**TI**	**(1074)**
					SN74LS643	**TI**	**(1074)**
					SN74LS643-1	**TI**	**(1074)**
					SN74LS645	**TI**	**(1074)**
					SN74LS645-1	**TI**	**(1074)**
	0.7 to 2.0	TTL	5	Bidirectional Bus Transceiver, Open Collector	SN54LS641	† Motorola	
					SN54LS642	† Motorola	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Line Circuits (Cont'd)

No. Per Device	Receiver Input Threshold, V	Output	Supply Voltage, V	Comments	Device	Source
Line Transceivers—Single Ended						**(Cont'd)**
8	0.7 to 2.0	TTL	5			(Cont'd)
				Bidirectional Bus Transceiver/Register, Open Collector	**SN54LS647**	† **TI (1076)**
					SN54LS649	† **TI (1076)**
				Bidirectional Bus Transceiver, Three-State	54LS245	† Fairchild
					SN54LS245	† Motorola
					SN54LS640	† Motorola
					SN54LS645	† Motorola
					SN54LS646	† **TI (1076)**
					SN54LS648	† **TI (1076)**
	0.8 to 2.0	TTL	5	Bidirectional Bus Transceiver, Open Collector	SN74LS641	Motorola
					SN74LS642	Motorola
				Bidirectional Bus Transceiver/Register, Open Collector	**SN74LS647**	**TI (1076)**
					SN74LS649	**TI (1076)**
				Bidirectional Bus Transceiver, Three-State	74LS245	Fairchild
					G74SC245	GTEMicro
					HD74LS243	Hitachi
					HD74LS245	Hitachi
					M74LS245	Mitsubishi
					SN74LS245	Motorola
					SN74LS640	Motorola
					SN74LS645	Motorola
					DM74LS245	National
					DS3667	† National
					74LS245	Signetics
					N8T125	**Signetics (876)**
					S8T125	† **Signetics (876)**
					SN54AS245	† **TI (1001)**
					SN74ALS1645	**TI (1124)**
					SN74ALS245	**TI (1001)**
					SN74ALS645	**TI (1074)**
					SN74AS245	**TI (1001)**
					SN74LS646	**TI (1076)**
					SN74LS648	**TI (1076)**
				Bidirectional Bus Transceiver, Three-State, CMOS	MD54SC245	† Mitel
					MD74SC245	Mitel
				General Purpose Interface Bus	**MC3447**	**Motorola (3064,3066)**
					SN75160A	TI
					SN75161A	TI
					SN75162A	TI
					SN75163	TI
Line Transceivers—Differential						
1		TTL	5	Designed to meet proposed EIA Standard RS485	DS3695	National
					DS3696	National
					DS3697	National
					DS3698	National
	0.8 to 2	TTL	5	Bidirectional Bus Transceiver, Three State	**SN75176**	**Motorola (3064)**
					SN75177	Motorola
					SN75178	Motorola
					SN75176A	TI
					SN75177	TI
					SN75178	TI
	±0.5/±1 V	TTL	5	Independent Three-State 55113 Driver and 55115 Receiver	SN55116	† TI
					SN75116	TI
				Same as 55116 with Three-State Receiver	SN55118	† TI
					SN75118	TI
				Same as 55117 with Three-State Receiver	SN55119	† TI
					SN75119	TI
				Three-State 8 Pin, 40 MA	SN55117	† TI
					SN75117	TI

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Memory and Peripheral Drivers

Memory & Peripheral Drivers

Function	Device	Source
Addressable Peripheral Driver (latched, 8-output driver)		
	NE590	**Signetics (3625)**
	NE591	**Signetics (3625)**
	SE590	† Signetics
Bidirectional Interface Circuit, High Voltage		
	TEA1512	Thomson-CSF
BiMOS Latched Driver		
	UCN-5810A	Sprague
	UCN-5812A	Sprague
	UCN-5818A	Sprague
	UCS-4401H	† Sprague
	UCS-4801H	Sprague
	UCS-4810H	Sprague
BiMOS Segment Latch Driver		
	CA3208	**RCA (3599)**
BiMOS Sequencer Driver		
	CA3207	**RCA (3599)**
Bridged Motor Driver		
	MD346	AnalogSys
Bubble Memory Coil Driver		
	DS3616	National
Bubble Memory Coil Predriver		
	SC42468	Motorola
Bubble Memory Controller		
	7220	Intel
	SC42584	Motorola
	SC42585	Motorola
Bubble Memory Controller (chevron)		
	SN54LS361	† TI
Bubble Memory Controller (t-bar)		
	SN54LS360	† TI
Bubble Memory Current Pulse Generator		
	7230	Intel
Bubble Memory Function Driver		
	DS3615	National
	DS3618	National
Bubble Memory Predriver		
	7250	Intel
	SI7250	Siliconix
Bubble Memory Sense Amplifier		
	MC34044	Motorola
	DS3617	National
Bubble Memory (Single) Operation Drivers		
	MC34046S	Motorola
	MC34047S	Motorola
Bubble Memory Dual Formatter/Sense Amplifier		
	7424	Intel
Bubble Memory Quad VMOS Drive Transistors		
	7254	Intel
Clock Generator/Oscillator, to 10 MHz, 8 and 1 Divider, for Microprocessors		
	ICM7209	**† Intersil (3015)**
Data Acquisition Controller (intelligent) for A/D Converter		
	CY600	Cybernetic
DC Motor Switch Mode Control		
	UAA4004	Thomson-CSF
Disc Memory Read/Write		
	μPC751	**NEC (3543)**
	μPC752	**NEC (3543)**
Disk Drive, Disk Data Controller		
	DP8466	National
Disk Drive, Disk Pulse Detector		
	DP8464	**National (1514)**
Disk Drive, Encoder/Decoder, 2, 7		
	DP8463	National
Disk Drive, MFM Data Separator		
	DP8460	National
Driver, Control Circuit for Fast Switching Transistors		
	UAA4002	Thomson-CSF
Driver, Half Bridge, 2 A		
	SG1635	† SiliconG
	SG3635	SiliconG
Driver, Open Collector/Emitter, for 150 mA (load connected to negative supply)		
	PBD3520	RIFA
Driver, Serial Input/16-Bit Parallel Output, High-Voltage, High-Current Outputs		
	TSC9403	**TeledyneS (3101)**
	TSC9404	**TeledyneS (3101)**
Driver, Solenoid and Motor, to 40 V, 4 A		
	SG3640	SiliconG
	SG3641	SiliconG
Driver, Switching Transistor		
	LAS8100	Lambda
	LAS8101	Lambda
Driver, to 80 V, 0.2 A		
	DI445	Dionics
Driver, Single, 125 mA, for Relays, Motors, Lamps		
	PBD3510	RIFA
	PBD3511	RIFA
Driver, Dual, to 80 V, 0.2 A		
	DI446	Dionics
Driver, Dual, 2-Input, Sink or Source 500 mA		
	SG1627	† SiliconG
	SG3627	SiliconG
Driver, 1 Channel (lamp relay driver)		
	TDE3207	Thomson-CSF
Driver, 2 Channel (hammer), to 35 V, 1 A		
	SG3700	SiliconG
Driver, 2 Channel (solenoid and motor driver, 4 A)		
	SG3638	SiliconG
	SG3638A	SiliconG
	SG3639	SiliconG
	SG3639A	SiliconG
	SG3643	SiliconG
	SG3643A	SiliconG
Driver, 4 Channel, 40 V, 2 A		
	SG3637	SiliconG
Driver, 5 Channel, CMOS/PMOS Input (lamp, relay driver, load to negative supply)		
	UDN-2956A	Sprague
Driver, 5 Channel, CMOS/TTL Input (lamp, relay driver, load to negative supply)		
	UDN-2957A	Sprague
Driver, 5 Channel Darlington, to 400 mA		
	XR2200	Exar
	XR2200M	† Exar
	LB1287	Sanyo
	LB1288	Sanyo
Driver, 7 Channel, CMOS/PMOS Input (hammer, lamp, relay driver)	MD402	AnalogSys
	XR2204	Exar
	XR2204M	† Exar
	9668	Fairchild
	9668M	† Fairchild
	MC1416	**Motorola (3064)**
	PBD352304	RIFA
	ULN2004	Signetics
	SG2004	SiliconG
	SG2014	SiliconG
	SG2024	SiliconG
	ULN-2004A	Sprague
	ULN-2014A	Sprague
	ULN-2024A	Sprague
	ULS-2004H	† Sprague
	ULS-2014H	† Sprague
	ULS-2024H	† Sprague
		(Continued)
Driver, 7 Channel, CMOS/PMOS Input (hammer, lamp, relay driver) (Cont'd)		
	SN75469	TI
	ULN2004A	TI
Driver, 7 Channel, CMOS/TTL Input (hammer, lamp, relay driver)	**XR2003M**	**† Exar (3383)**
	XR2203	Exar
	9667	Fairchild
	9667M	† Fairchild
	MC1413	**Motorola (3064)**
	PBD352303	RIFA
	L203	SGS
	ULN2003	Signetics
	SG2003	SiliconG
	SG2005	SiliconG
	SG2013	SiliconG
	SG2015	SiliconG
	SG2023	SiliconG
	SG2025	SiliconG
	SG3853	SiliconG
	ULN-2003A	Sprague
	ULN-2005A	Sprague
	ULN-2013A	Sprague
	ULN-2015A	Sprague
	ULN-2023A	Sprague
	ULN-2025A	Sprague
	ULS-2003H	† Sprague
	ULS-2005H	† Sprague
	ULS-2013H	† Sprague
	ULS-2015H	† Sprague
	ULS-2023H	† Sprague
	ULS-2025H	† Sprague
	SN75468	TI
	ULN2003A	TI
Driver, 7 Channel, MOS/TTL Input (hammer, lamp, relay driver)	XR2201	Exar
	XR2201M	† Exar
	9665	Fairchild
	MC1411	**Motorola (3064)**
	PBD352301	RIFA
	L201	SGS
	SG2001	SiliconG
	SG2011	SiliconG
	SG2021	SiliconG
	SG3851	SiliconG
	ULN-2001A	Sprague
	ULN-2011A	Sprague
	ULN-2021A	Sprague
	ULS-2001H	† Sprague
	ULS-2011H	† Sprague
	ULS-2012H	† Sprague
	ULS-2021H	† Sprague
	SN75466	TI
	ULN2001A	TI
Driver, 7 Channel, PMOS Input (hammer, lamp, relay driver)	XR2202	Exar
	XR2202M	† Exar
	9666	Fairchild
	9666M	† Fairchild
	MC1412	**Motorola (3064)**
	PBD352302	RIFA
	L202	SGS
	SG2002	SiliconG
	SG2012	SiliconG
	SG2022	SiliconG
	SG3852	SiliconG
	ULN-2002A	Sprague
	ULN-2012A	Sprague
	ULN-2022A	Sprague
	ULS-2002H	† Sprague
	ULS-2022H	† Sprague
	SN75467	TI
	ULN2002A	TI

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

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INTERFACE–Memory and Peripheral Drivers (Cont'd)

Function	Device	Source
Memory & Peripheral Drivers (Cont'd)		
Driver, 8 Channel, CMOS/PMOS Input (hammer, lamp, relay driver)	ULN2804	Motorola
	ULN-2804A	Sprague
	ULN-2814A	Sprague
	ULN-2824A	Sprague
	ULS-2804H	† Sprague
	ULS-2814H	† Sprague
	ULS-2824H	† Sprague
Driver, 8 Channel, CMOS/PMOS Input (lamp, relay driver)	UDN-2982A	Sprague
	UDN-2984A	Sprague
	UDS-2982H	† Sprague
	UDS-2984H	† Sprague
Driver, 8 Channel, CMOS/TTL Input (hammer, lamp, relay driver)	ULN2803	Motorola
	NE5090	**Signetics (3624)**
	SE5090	Signetics
	ULN-2803A	Sprague
	ULN-2805A	Sprague
	ULN-2813A	Sprague
	ULN-2815A	Sprague
	ULN-2823A	Sprague
	ULN-2825A	Sprague
	ULS-2803H	† Sprague
	ULS-2805H	† Sprague
	ULS-2813H	† Sprague
	ULS-2815H	† Sprague
	ULS-2823H	† Sprague
	ULS-2825H	† Sprague
Driver, 8 Channel, CMOS/TTL Input (lamps, relay driver)	UDN-2981A	Sprague
	UDN-2983A	Sprague
	UDS-2981H	† Sprague
	UDS-2983H	† Sprague
Driver, 8 Channel, MOS/TTL Input (hammer, lamp, relay driver)	ULN2801	Motorola
	ULN-2801A	Sprague
	ULN-2811A	Sprague
	ULN-2821A	Sprague
	ULS-2801H	† Sprague
	ULS-2811H	† Sprague
	ULS-2821H	† Sprague
Driver, 8 Channel, PMOS Input (hammer, lamp, relay driver)	ULN2802	Motorola
	ULN-2802A	Sprague
	ULN-2812A	Sprague
	ULN-2822A	Sprague
	ULS-2802H	† Sprague
	ULS-2812H	† Sprague
	ULS-2822H	† Sprague
Driver, 8-Bit, BiMOS Addressable Latched	UCN-4807A	Sprague
	UCN-4808A	Sprague
Driver, 8-Channel Current-Sink Driver	UDN-2595A	Sprague
Driver, 10-Bit, High-Voltage, High-Current	S4534	AMI
Driver, 10-Bit Serial-In Latched Source	UCS-4810H	Sprague
Driver, 32-Bit for Displays, Relays, Solenoids, Print Heads and Motors	S4521	AMI
	S4535	AMI
Dynamic RAM Controller Interface Circuit	DP84312	National
	DP84322	National
	DP84332	National
Dynamic RAM Programmable Refresh Timer	DP84300	National
Gated Decoder, for SSI104/5	SSI106	SiliconSys
Hall Effect Digital Latches (logic to electromechanical interface)	UGN-3075	Sprague
	UGN-3076	Sprague
	UGS-3075	† Sprague
	UGS-3076	† Sprague
Hammer Driver (to 6 A-pulsed output)	DH0028C	National
High Current Switch Driver (to drive high power, high speed NPN switching transistors)	SG1629	† SiliconG
	SG3629	SiliconG
High-Voltage, High-Current Source Driver	UDQ-2956R	Sprague
	UDQ-2957	Sprague
High-Voltage Source Drivers	UDN-6510A	Sprague
	UDN-6514A	Sprague
Memory Driver, FIFO RAM Controller	**N8X60**	**Signetics (1647)**
	S8X60	**† Signetics (527,1647)**
Memory Driver Dual, 400 mA Sink/Source, Decode (for magnetic memories)	DS3629	National
Memory Driver, Dual 600 mA Sink/Source	MC55325	† Motorola
	MC75325	Motorola
	DS55325	† National
	DS75325	National
	SG55325	† SiliconG
	SG75325	SiliconG
	SN55325	† TI
	SN75325	TI
Memory Driver, Quad, 600 mA Sink	SG55326	† SiliconG
	SG55327	† SiliconG
	SG75326	SiliconG
	SG75327	SiliconG
	SN55326	† TI
	SN55327	† TI
	SN75326	TI
	SN75327	TI
Memory Timing Controller (with EDAC)	AM2969	AMD
	MC74F2969	**Motorola (822)**
Memory Timing Controller (without EDAC)	AM2970	AMD
	MC74F2970	**Motorola (822)**
Modified Frequency Modulation Decoder Data Separator	**DP8460**	**National (1514)**
MOS Clock Driver	MH0007	† National
	MH0007C	National
	MH0012	† National
	MH0012C	National
MOS Dynamic Memory, Address Refresh Logic Circuitry	MC8505	Motorola
MOS Dynamic Memory Controller	AM2968	AMD
	MC74F2968	**Motorola (822)**
MOS Dynamic Memory Interface, Microprocessor to 16 K RAM	MC3480	Motorola
MOS Dynamic Memory, 4 K Address Multiplexer and Refresh Counter	96LS32	† Fairchild
	96LS32C	Fairchild
	MC3232A	Motorola
MOS Dynamic Memory, 16 K Address Multiplexer and Refresh Counter	96LS42C	Fairchild
	96LS42M	† Fairchild
	MC3242A	Motorola
MOS Dynamic RAM Controller	8202A	Intel
	8203	Intel
	8205	Intel
	TMS4500A	**TI (4221)**
	VL4500A	**VTI (4254)**
	WD8207	**Western (4262)**
MOS Dynamic RAM Controller/Driver	DP8408	MMI
	SN74S408	**MMI (819)**
	SN74S408-3	**MMI (819)**
	DP8408	National
MOS Dynamic RAM Controller/Driver, Multimode	74S409	MMI
	DP8409	MMI
	SN74S409	**MMI (819)**
	DP8409	**National (1514)**
MOS Dynamic RAM Controller, Two Port	**74LS764**	**Signetics (895)**
Motor Controller (intelligent) for 4-Phase Stepper Motors	CY500	Cybernetic
	CY512	Cybernetic
Multi-Mode Dynamic RAM Controller/Driver	**DP8408**	**National (1514)**
Power Peripheral Driver, CMOS/TTL Input (to 150 V, versions: 0.01 to 16 A)	VF01	Supertex
	VF02	Supertex
	VF03	Supertex
	VF12	Supertex
	VF13	Supertex
Printer Controller, for 5x7 Dot Matrix Printers	CY480	Cybernetic
Printer Driver, 5 Channel	HD2919	Hitachi
Printer Solenoid Driver	DS3654	National
Printing Calculator Circuits	DS8654	National
	DS8656	National
	DS8692	National
	DS8693	National
	DS8694	National
Relay and Lamp Driver, Dual, to 32 V, 2/4 A	TDE1777	Thomson-CSF
Relay and Lamp Driver, to 30 V, 0.15 A	TDE1647	Thomson-CSF
Relay and Lamp Driver, to 30 V, 0.3 A	TDE1607	Thomson-CSF
Relay and Lamp Driver, to 45 V, 0.3 A	TDE1647A	Thomson-CSF
	TDE1737	Thomson-CSF
Relay and Lamp Driver, to 50 V, 0.3 A	TDE1787	Thomson-CSF
Relay and Lamp Driver, to 50 V, 0.5 A	TDE1767	Thomson-CSF
Relay and Lamp Driver, to 60 V, 0.3 A	TDE1787A	Thomson-CSF
Relay and Lamp Driver, to 60 V, 0.5 A	TDE1767A	Thomson-CSF
Relay Driver, to 65 V, Sinks 300 mA, OR Input for 48 V Telephone Relays	DS1686	† National
	DS1687	† National
	DS3686	National

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Memory and Peripheral Drivers (Cont'd)

Memory & Peripheral Drivers (Cont'd)

Function	Device	Source
Relay Driver, to 65 V, Sinks 300 mA, OR Input for 48 V Telephone Relays (Cont'd)	DS3687	National
Relay Driver, to 70 V, 500 mA	CSR301	TeledyneC
Relay Driver, 5 Channel, to 65 V, 70 mA	ITT7163	ITT
	ITT7164	ITT
Solenoid Driver	MC3484V2	Motorola
	MC3484V4	Motorola
Thermal Print Head Driver	SN75270	TI
	SN75490	TI
	SN75590	TI
Triac Controller	TEA1511	Thomson-CSF
Winchester Disc Memory Fault Detector	SSI103	SiliconSys
Winchester Disc Memory Head Read/Write Circuit, for thin film heads	**SSI114**	**SiliconSys (4208)**
Winchester Disc Memory Head Selector	SSI102	SiliconSys
Winchester Disc Memory Read/Write Circuit	**SSI104**	**SiliconSys (4208)**
Winchester Disc Memory Video Amplifier, for Magnetic Servo Head	**SSI101A**	**SiliconSys (4208)**
Winchester Disc Memory Video Amplifier, for Thin Film Magnetic Heads	**SSI116**	**SiliconSys (4208)**
Winchester Disk Memory Read/Write Circuit	MB4111	Fujitsu
	MB4112	Fujitsu
	SSI105	SiliconSys
	SSI108	**SiliconSys (4208)**
	SSI114	SiliconSys
	SSI115	**SiliconSys (4208)**
Winchester, Read/Write Circuit for thin-film heads	**MC4290**	**NEC (3549)**
Winchester Read/Write Circuit, 6-Channel	**SSI117**	**SiliconSys (4208)**
Dual AND Driver, HNIL, 250 mA, Open Collector	391A/C	TeledyneS
Dual AND TTL to MOS Driver (NMOS memory interface)	9643	Fairchild
	SN55363	† TI
	SN75322	TI
	SN75363	TI
Dual Buffer, to 40 V, 2 A	LPD4106	Lambda
Dual CCD Memory Driver, with Enable Inputs	SN75430	TI
Dual CCD Memory Driver, with Enable Inputs and Protect	SN75431	TI
Dual Channel ECL to MOS Driver (MOS memory interface	MC75358	Motorola
Dual CMOS or TTL Driver/Translator, up to 30 V	IH6201C	Intersil
	IH6201M	† Intersil
Dual Darlington Switch, to 80 V, 1.5 A	ULN-2061M	Sprague
	ULN-2062M	Sprague
Dual ECL to TTL/MOS Driver	SN75441	TI
Dual Half Bridge Driver, 1.5 A	SG3636	SiliconG
Dual Inverter, to 40 V, 2 A	LPD4105	Lambda
Dual Memory Driver, 400 mA Sink (for magnetic memories)	MC4043	Motorola
Dual MOS Clock Driver	0026	Fairchild
	MMH0026C	Motorola
	DS0025	† National
	DS0025C	National
	DS0026	† National
	DS0026C	National
	DS0056	† National
	DS0056C	National
	MH0009	† National
	MH0009C	National
	MH0013	† National
	MH0013C	National
	SN55369	† TI
	SN75369	TI
Dual MOS Clock Driver, Bootstrapped for Single Supply Systems	DS1642	National
	DS1671	National
	DS1672	National
Dual NAND Driver, HNIL, 250 mA, Open Collector	392A/C	TeledyneS
Dual NOR Driver, HNIL, 250 mA, Open Collector	394A/C	TeledyneS
Dual OR Driver, HNIL, 250 mA, Open Collector	393A/C	TeledyneS
Dual Peripheral AND Driver	55450B	† Fairchild
	75450B	Fairchild
	75451A	Fairchild
	75451B	Fairchild
	75461	Fairchild
	75471	Fairchild
	HD75450A	Hitachi
	HD75451A	Hitachi
	DS55450	† National
	DS55451	† National
	DS55461	† National
	DS75450	National
	DS75451	National
	DS75461	National
	PBD3513	RIFA
	SG55450	† SiliconG
	SG55450B	† SiliconG
	SG55451	† SiliconG
	SG55460	† SiliconG
	SG55460B	† SiliconG
	SG55461	† SiliconG
	SG75450	SiliconG
	SG75450B	SiliconG
	SG75451	SiliconG
	SG75460	SiliconG
	SG75460B	SiliconG
	SG75461	SiliconG
	SN55450B	† TI
	SN55451B	† TI
	SN55460	† TI
	SN55461	† TI
	SN55470	† TI
	SN55471	† TI
	SN75401	TI
	SN75411	TI
	SN75450B	TI
	SN75451B	TI
	SN75460	TI
	SN75461	TI
	SN75466	TI
	SN75470	TI
		(Continued)
Dual Peripheral AND Driver (Cont'd)	SN75471	TI
	SN75476	TI
Dual Peripheral AND Driver, for CMOS	DS1631	† National
	DS3631	National
Dual Peripheral AND Driver, to 70 V 300 mA	SN75446	TI
Dual Peripheral AND Driver, to 70 V 500 mA	SN75416	TI
Dual Peripheral AND Driver, to 80 V 300 mA	DS1611	† National
	DS3611	National
	UDN-3611M	Sprague
	UDN-5711M	Sprague
	UDS-3611H	† Sprague
	UDS-5711H	† Sprague
Dual Peripheral and Power Drivers	UDN-5732M	Sprague
	UDN-5742M	Sprague
Dual Peripheral NAND Driver	55452B	† Fairchild
	75452A	Fairchild
	75452B	Fairchild
	75462	Fairchild
	75472	Fairchild
	HD75452	Hitachi
	DS55452	† National
	DS55462	† National
	DS75452	National
	DS75462	National
	SG55452	† SiliconG
	SG55462	† SiliconG
	SG75452	SiliconG
	SG75462	SiliconG
	SN55452B	† TI
	SN55462	† TI
	SN55472	† TI
	SN75402	TI
	SN75407	TI
	SN75412	TI
	SN75432	TI
	SN75447	TI
	SN75452B	TI
	SN75462	TI
	SN75472	TI
Dual Peripheral NAND Driver, for CMOS	DS1632	† National
	DS3632	National
Dual Peripheral NAND Driver, to 70 V, 300 mA	**MC1472**	**Motorola (3064)**
	UDN-5722M	Sprague
	SN75477	TI
Dual Peripheral NAND Driver, to 70 V, 500 mA	SN75417	TI
Dual Peripheral NAND Driver, to 80 V, 300 mA	DS1612	† National
	DS3612	National
	UDN-3612M	Sprague
	UDN-5712M	Sprague
	UDS-3612H	† Sprague
	UDS-5712H	† Sprague
Dual Peripheral NOR Driver	75474B	Fairchild
	HD75454	Hitachi
	DS55454	† National
	DS55464	† National
	DS75454	National
	DS75464	National
	SG55454	† SiliconG
	SG55464	† SiliconG
		(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Memory and Peripheral Drivers (Cont'd)

Function	Device	Source
Memory & Peripheral Drivers (Cont'd)		
Dual Peripheral NOR Driver (Cont'd)		
	SG75454	SiliconG
	SG75464	SiliconG
	SN55454B	† TI
	SN55464	† TI
	SN55474	† TI
	SN75404	TI
	SN75407	TI
	SN75414	TI
	SN75434	TI
	SN75449	TI
	SN75454B	TI
	SN75464	TI
	SN75474	TI
	SN75479	TI
Dual Peripheral NOR Driver, for CMOS		
	DS1634	† National
	DS3634	National
Dual Peripheral NOR Driver, to 30 V, 300 mA		
	SN75479	TI
Dual Peripheral NOR Driver, to 30 V, 500 mA		
	SN75419	TI
Dual Peripheral NOR Driver, to 80 V, 300 mA		
	DS1614	† National
	DS3614	National
	UDN-3614M	Sprague
	UDN-5714M	Sprague
	UDS-3614H	† Sprague
	UDS-5714H	† Sprague
Dual Peripheral OR Driver		
	75453A/B	Fairchild
	HD75453	Hitachi
	MC75453	Motorola
	DS55453	† National
	DS55463	† National
	DS75453	National
	DS75463	National
	SG55453	SiliconG
	SG55463	SiliconG
	SG75453	SiliconG
	SG75463	SiliconG
	SN55453B	† TI
	SN55463	† TI
	SN55473	† TI
	SN75403	TI
	SN75408	TI
	SN75413	TI
	SN75433	TI
	SN75448	TI
	SN75453B	TI
	SN75463	TI
	SN75473	TI
	SN75478	TI
Dual Peripheral OR Driver, ECL Input		
	SN75441	TI
Dual Peripheral OR Driver, for CMOS		
	DS1633	† National
	DS3633	National
Dual Peripheral OR Driver, to 30 V, 300 mA		
	SN75478	TI
Dual Peripheral OR Driver, to 30 V, 500 mA		
	SN75418	TI
Dual Peripheral OR Driver, to 80 V, 300 mA		
	DS1613	† National
	DS3613	National
	UDN-3613M	Sprague
	UDN-5713M	Sprague
	UDS-3613H	† Sprague
	UDS-5713H	† Sprague
Dual Power MOS Driver		
	ICL7667	**Intersil (3013)**
Dual Power MOSFET Driver		
	TSC450C	TeledyneS
	TSC450M	† TeledyneS
Dual TTL to MOS Driver (MOS memory interface)		
	DS75361	National
	DS75362	National
	MH8805	National
	SN75350	TI
	SN75361A	TI
Dual 2-Input AND Power Driver (40 V, 2 A)		
	LPD4101	Lambda
Dual 2-Input NAND Power Driver (40 V, 2 A)		
	LPD4102	Lambda
Dual 2-Input NOR Power Driver (40 V, 2 A)		
	LPD4103	Lambda
Dual 2-Input OR Power Driver (40 V, 2 A)		
	LPD4104	Lambda
Dual 4 A Solenoid Driver		
	UDN-2975W	Sprague
	UDN-2976W	Sprague
Dual 4-Input AND Driver, HNIL 250 mA Open Collector		
	390A/C	TeledyneS
Dual 4-Input NAND Driver, HNIL, 250 mA Open Collector		
	395A/C	TeledyneS
Quad Bipolar Driver		
	SG293A	SiliconG
Quad Darlington Driver, to 100 V, 1.5 A		
	FT5753	Fujitsu
Quad Darlington Driver, to 100 V, 3 A		
	FT5754	Fujitsu
Quad Darlington Driver, to 100 V, 5 A		
	FT5755	Fujitsu
Quad Darlington Switch, to 50 V, 1.5 A		
	SN75064	TI
	SN75066	TI
	SN75068	TI
Quad Darlington Switch, to 50 V, 4 A		
	UDN-2878	**Sprague (3088)**
Quad Darlington Switch, to 80 V, 1.5 A		
	SG2064	SiliconG
	SG2065	SiliconG
	SG2066	SiliconG
	SG2067	SiliconG
	SG2068	SiliconG
	SG2069	SiliconG
	SG2070	SiliconG
	SG2071	SiliconG
	SG2072	SiliconG
	SG2073	SiliconG
	SG2074	SiliconG
	SG2075	SiliconG
	SG2076	SiliconG
	SG2077	SiliconG
	ULN-2064B	Sprague
	ULN-2065B	Sprague
	ULN-2066B	Sprague
	ULN-2067B	Sprague
	ULN-2068B	Sprague
	ULN-2069B	Sprague
	ULN-2070B	Sprague
	ULN-2071B	Sprague
	ULN-2074B	Sprague
	ULN-2075B	Sprague
	ULN-2076B	Sprague
	ULN-2077B	Sprague
	ULS-2064H	† Sprague
	ULS-2065H	† Sprague
	ULS-2066H	† Sprague
	ULS-2067H	† Sprague
(Continued)		
Quad Darlington Switch, to 80 V, 1.5 A (Cont'd)		
	ULS-2068H	† Sprague
	ULS-2069H	† Sprague
	ULS-2070H	† Sprague
	ULS-2071H	† Sprague
	ULS-2074H	† Sprague
	ULS-2075H	† Sprague
	ULS-2076H	† Sprague
	ULS-2077H	Sprague
	SN75065	TI
	SN75067	TI
	SN75069	TI
	ULN2064	TI
	ULN2065	TI
	ULN2066	TI
	ULN2067	TI
	ULN2068	TI
	ULN2069	TI
	ULN2074	TI
	ULN2075	TI
Quad Darlington Switch, to 80 V, 4 A		
	UDN-2879	**Sprague (3088)**
Quad Darlington Switch, to -50 V, 1.75 A		
	SG2841	SiliconG
Quad Darlington Switch		
	TEB1013	Thomson-CSF
Quad Driver for Automotive Applications		
	DS3656	National
Quad ECL to MOS Clock Driver		
	HD2923	Hitachi
Quad Fault Protected Peripheral Driver		
	DS3668	National
Quad High Current Peripheral Driver		
	DS3658	National
	DS3669	National
	SN75436	TI
	SN75437A	TI
	SN75438	TI
Quad Latch/Driver		
	MD121	AnalogSys
	UCN-4401A	Sprague
	UCS-4401H	† Sprague
Quad MOS Clock Driver		
	DS3245	National
Quad, MOS Memory Decoder/Clock Driver		
	DS36143	National
Quad MOS Memory I/O Register		
	DS16147	† National
	DS16177	† National
	DS1647	† National
	DS1677	† National
	DS36147	National
	DS36177	National
	DS3647	National
	DS3677	National
Quad Multiplexer/Driver, for MOS Systems		
	DS1648	† National
	DS1678	† National
	DS3648	National
	DS3678	National
Quad NAND Gate 60 V Power Driver		
	UDN-2541	Sprague
Quad NAND Gate 80 V Power Driver		
	UDN-2542	Sprague
Quad NAND TTL to MOS Driver (MOS memory interface-clock driver)		
	HD2912	Hitachi
	HD2916	Hitachi
	DS75365	National
	3207A	Signetics
	3207A-1	Signetics
	SN55355	† TI
(Continued)		

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Memory and Peripheral Drivers (Cont'd)

Memory & Peripheral Drivers (Cont'd)

Function	Device	Source
Quad NAND TTL to MOS Driver (MOS memory interface-clock driver) (Cont'd)		
	SN55365	† TI
	SN75365	TI
Quad Negative Voltage Relay Driver		
	DS3680	National
	DS3680	TI
Quad NMOS Memory Driver		
	MC3459	Motorola
	MC3460	Motorola
	DS1644	† National
	DS1674	† National
	DS36144	National
	DS3644	National
	DS3674	National
Quad PIN Diode Driver (also see: linear-other devices)		
	UDS-5790H	† Sprague
	UDS-5791H	† Sprague
Quad Port Driver, for 5270 RAM		
	DS1640	† National
	DS1670	† National
Quad Power NAND Driver		
	CA3219	**RCA (3602)**
Quad Power Peripheral Driver		
	7254	Intel
	VQ1000	Siliconix
	VQ1001	**Siliconix (3085)**
	VQ1004	**Siliconix (3085)**
	VQ1006	**Siliconix (3085)**
	VQ2001	**Siliconix (3085)**
	VQ2004	**Siliconix (3085)**
	VQ2006	**Siliconix (3085)**
	VQ3001	**Siliconix (3085)**
	VQ7254	**Siliconix (3085)**
	VC01	Supertex
	VC02	Supertex
	VC13	Supertex
	VQ1000	Supertex
	VQ7254	Supertex
Quad Power Strobe		
	HD6600-2	† Harris
	HD6600-5	Harris
	HD6600	National
Quad Predriver, Open Collector, 50 mA Sink (for magnetic memories)	MC4042	Motorola
Quad TTL to MOS Driver, Three-State		
	SN75367	TI
Quad TTL to NMOS Memory Driver (for 2105, 2107, etc.)		
	3245	Fairchild
	9645	Fairchild
Quad TTL to NMOS Memory Driver (for 7001, etc.)		
	MC3466	Motorola
Quad 2-Input AND Driver (to 70 V, sinks 300 mA)		
	UDN-5706A	Sprague
	UDS-5706H	† Sprague
Quad 2-Input AND Power Driver, Open Collector (to 100 V, sinks 500 mA)		
	UHC/D-400	† Sprague
	UHC/D-406	† Sprague
	UHC/D-500	Sprague
	UHC/D-506	Sprague
	UHP-400	Sprague
	UHP-406	Sprague
	UHP-500	Sprague
	UHP-506	Sprague
Quad 2-Input NAND Driver (for 70 V, sinks 300 mA)		
	UDN-5707A	Sprague
	UDS-5707H	† Sprague
Quad 2-Input NAND Driver, to 30 V, sinks 250 mA		
	MC693	Motorola
Quad 2-Input NAND Power Driver, Open Collector, to 100 V, Sinks 500 mA		
	UHC/D-407	† Sprague
	UHC/D-408	† Sprague
	UHC/D-507	† Sprague
	UHC/D-508	† Sprague
	UHP-407	Sprague
	UHP-408	Sprague
	UHP-507	Sprague
	UHP-508	Sprague
Quad 2-Input NOR Driver, to 70 V, Sinks 300 mA		
	UDN-5733M	Sprague
	UDS-5733H	† Sprague
Quad 2-Input NOR Power Driver, Open Collector, to 100 V, Sinks 500 mA	UHC/D-432	† Sprague
	UHC/D-433	† Sprague
	UHC/D-532	† Sprague
	UHC/D-533	† Sprague
	UHP-432	Sprague
	UHP-433	Sprague
	UHP-532	Sprague
	UHP-533	Sprague
Quad 2-Input OR Driver, to 70 V, Sinks 300 mA		
	UDN-5703A	Sprague
	UDS-5703H	† Sprague
Quad 2-Input OR Power Driver, Open Collector, to 100 V, Sinks 500 mA	UHC/D-402	† Sprague
	UHC/D-403	† Sprague
	UHC/D-502	Sprague
	UHC/D-503	Sprague
	UHP-402	Sprague
	UHP-403	Sprague
	UHP-502	Sprague
	UHP-503	Sprague
Hex Driver, CMOS/TTL (line, LED, Relay Driver)		
	MD-210	AnalogSys
Hex Inverter/MOS Driver, Disable Causes Logic 1 State		
	DS16149	† National
	DS16179	† National
	DS36149	National
	DS36179	National
	SN54S436	**† TI (1035,1036)**
	SN54S437	**† TI (1035,1036)**
	SN74S436	**TI (1035,1036)**
	SN74S437	**TI (1035,1036)**
Hex Inverter/MOS Driver, Three-State		
	DS1649	† National
	DS1679	† National
	DS3649	National
	DS3679	National
Hex Latch/Driver, for MOS Memories		
	DS1645	† National
	DS1675	† National
	DS3645	National
	DS3675	National
Octal Dynamic Memory Driver, Three-State		
	AM2965C	AMD
	AM2965M	† AMD
	AM2966C	AMD
	AM2966M	† AMD
Octal Dynamic RAM Driver, Three-State		
	SN54S700	**† MMI (804,819)**
	SN54S730	**† MMI (804,819)**
	SN54S731	**† MMI (804,819)**
	SN54S734	**† MMI (804,819)**
	SN74S700	**MMI (804,819)**
	SN74S730	**MMI (804,819)**
	SN74S731	**MMI (804,819)**
	SN74S734	**MMI (804,819)**
Octal High-Voltage Driver for Electrostatic Printers		
	DH0069	National
Octal Latched Peripheral Driver		
	DP7310	National
	DP7311	National
	DP8310	National
	DP8311	National
Octal MOS Driver, Three-State		
	DP84240	National
	DP84244	National
	DS1628	† National
	DS3628	National
Two Phase Oscillator/Clock Driver (for MOS systems)		
	DS7803	† National
	DS7807	† National
	DS8803	National
	DS8807	National
Eight Latch/Drivers		
	UCN-4801A	Sprague
4-Input AND Current Driver (45 V, to 1.5 A peak)		
	DH0006	† National
	DH0006C	National
4-Input AND High Voltage-High Current Driver (4.5 V, to 3 A peak)	DH0008	† National
4-Input NAND High Voltage, High Current Drivers (40 V, 0.15 to 0.25 A)		
	DH0011	† National
4-Input NAND High Voltage, High Current Drivers (50, 70 or 100 V, 0.25 to 0.5 A)		
	DH0017C	National
	DH0018C	National
6-Bit MOS Refresh Counter/Driver		
	DS1646	† National
	DS1676	† National
8-Bit Serial Input, Latched Sink Driver		
	UCN-4821A	Sprague
	UCN-4822A	Sprague
	UCN-4823A	Sprague
	UCS-4821H	† Sprague
	UCS-4822H	† Sprague
	UCS-4823H	† Sprague

† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE–Sense Amplifiers

Sense Amplifiers

Function	Device	Source
MOS to TTL Level Converter, High Speed, Three-State	MC4000	Motorola
	MC4300	† Motorola
Translators: See also Digital-TTL (Translators)		
Dual Core Memory Sense Amplifier, Complementary Output, Latch Capability	55S20	Fairchild
	75S20	† Fairchild
	SG5520	† SiliconG
	SG5521	† SiliconG
	SG7520	SiliconG
	SG7521	SiliconG
	SN5520	† TI
Dual Core Memory Sense Amplifier/Data Register	SG55236	† SiliconG
	SG75236	SiliconG
	SN55236	† TI
	SN55237	† TI
Dual Core Memory Sense Amplifier, Separate Inverted Outputs	55S234	Fairchild
	75S234	† Fairchild
	SN55234	† TI
	SN75234	TI
Dual Core Memory Sense Amplifier, Separate Inverted Outputs, Test Points	75239	Fairchild
Dual Core Memory Sense Amplifier, Separate Open Collector Outputs	SG5534	† SiliconG
	SG5535	† SiliconG
	SG7534	SiliconG
	SG7535	SiliconG
	SN55232	† TI
Dual Core Memory Sense Amplifier, Separate Open Collector Outputs, Test Points	SG5538	† SiliconG
	SG5539	† SiliconG
	SG7538	SiliconG
	SG7539	SiliconG
Dual Core Memory Sense Amplifier, Separate Outputs	55S24	Fairchild
	75S24	† Fairchild
	HA1902	Hitachi
	SG5524	† SiliconG
	SG5525	† SiliconG
	SG7524	SiliconG
	SG7525	SiliconG
	SN5524	† TI
Dual Core Memory Sense Amplifier, Separate Outputs, Test Points	SG5528	† SiliconG
	SG5529	† SiliconG
	SG7528	SiliconG
	SG7529	SiliconG
	SN5528	† TI
Dual Core Memory Sense Amplifier, Single Open Collector Output	SG5522	† SiliconG
	SG5523	SiliconG
	SG7522	SiliconG
	SG7523	SiliconG
	SN5522	† TI
Dual Formatter/Sense Amplifier for Bubble Memories	7242	Intel
Dual MOS to TTL Level Converter, Latch, Three-State (Sense Amp)	MC74468	Motorola
	N8T25	SiliconG
Dual Sense Amplifier (for MOS memory or line receiver)	DS75207	National
	DS75208	National
	SN75207	TI
(Continued)		
Dual Sense Amplifier (for MOS memory or line receiver) (Cont'd)	SN75208	TI
	DS3604	National
	DS1603	† National
	DS3603	National
Dual Sense Amplifier (NMOS memories to ECL 10K)	HD103461	Hitachi
Triple Current Sense Latch	SG3551	SiliconG
Quad Sense Amplifer, Three-State	MC3430	Motorola
	MC3431	Motorola
	MC3432	Motorola
	MC3433	Motorola
	DS1651	† National
	DS1653	† National
	DS3651	National
	DS3653	National
Hex MOS Sense Amplifier (MOS to TTL Converter) Three-State	DS3605	National
	DS3606	National
	DS3607	National
	DS3608	National
Octal Core Memory Driver	SN55329	† TI
4-Input Sense Amplifier (for plated wire or thick/thin film memories)	MC1444	Motorola
	MC1544	† Motorola

† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE–Transmitters-Receivers

Serial Transmitters- Receivers

Function	Max Serial Data Rate in kHZ	Supply Voltage, V	Device	Source
(ACIA) Asynchronous Communications Interface Adapter (Links 8-Bit bidirectional data bus to serial asynchronous data communications, including to 6860)	50	5	**S6551**	**AMI** (1449)
			S6551A	**AMI** (1449)
			S6850	AMI
			F6850	**Fairchild** (1463)
			MC6850	**Motorola** (1505)
			EF6850	Thomson-CSF
Advanced Data Link Controller	2 Mb/s	5	MC854	Motorola
ARINC-429 Buffer Receiver 1-15			EF4440	Thomson-CSF
ARINC-429 Receiver/Transmitter	100	5	HS3182	† Harris
			HS3282	**† Harris** (4648)
			EF4442	Thomson-CSF
			WD1993-01	Western
			WD1993-02	Western
			WD1993-03	Western
ASTRO (asynchronous/synchronous receiver/transmitter) to Interface Serial Communications Channel with a Parallel Digital System (i.e. microprocessors)	1000	12,5	WD1931	Western
		12, ±5	COM1671	SMC
			UC1671	Western
Asynchronous Addressable Receiver/Transmitter	—	4.75-11.5	MM54240	National
	4.8	3-18	MC14469	Motorola
Asynchronous Communications Element	56	5	WD8250	Western
Asynchronous Serial Interface Component			**MA2232**	**National** (2049)
Asynchronous Serial Manchester Adapter	1000	5	**HD6408**	**Harris** (1492,1496)
Baud Rate Generator (programmable divider)	1000	5	COM8046	SMC
			COM8046T	SMC
			COM8126	SMC
			COM8126T	SMC
			COM8146	SMC
			COM8146T	SMC
		12,5	COM5026	SMC
			COM5026T	SMC
			COM5046	SMC
			COM5046T	SMC
		12, ±5	F4702BC	Fairchild
			F4702BM	† Fairchild
			HD4702-2	**† Harris** (1492)
			HD4702-9	**Harris** (1492)
			IM4702	Intersil
			IM4703	Intersil
			MC14411	**Motorola** (3536)
			MM5307	National
Baud Rate Generator (programmable divider), Dual	307/19.2	5	WD1943-00	Western
			WD1943-02	Western
			WD1943-05	Western
		12,5	BR1941-00	Western
			BR1941-02	Western
			BR1941-05	Western
	614/19.2	5	WD1943-04	Western
			WD1943-06	Western
		12,5	BR1941-04	Western
			BR1941-06	Western
	1000	5	AY5-8116	GI

(Continued)

Function	Max Serial Data Rate in kHZ	Supply Voltage, V	Device	Source
Baud Rate Generator (programmable divider), Dual	1000	5		(Cont'd)
			AY5-8116T	GI
			AY5-8136	GI
			AY5-8136T	GI
			COM8116	SMC
			COM8116T	SMC
			COM8136	SMC
			COM8136T	SMC
			WD1945	Western
		12,5	COM5016	SMC
			COM5016T	SMC
			COM5036	SMC
			COM5036T	SMC
BOART (Bus Orientated Programmable Asynchronous Receiver/Transmitter	9.6	5	TR1983	Western
Bus Interface Circuit (MIL-STD1553B)	5000	5	HS3273	† Harris
Command/Response Manchester II Converter (MIL-STD-1553B)	1000	5	BUS-8937	† DDC
			SSM-2012	SSM
Digital Modem (Modulation, demodulation and supervisory control, up to 600 BPS.)	0.6	5	**MC6860**	**Motorola** (1505;3536)
DUART (Dual Universal Asynchronous Receiver and Transmitter). Two-channel UART, baud-rate generator, 16-Bit counter/timer, I/O ports.	1000	5	26810	Signetics
			26814	Signetics
			26818	Signetics
			SCN2681	**Signetics** (1675)
			SCN68681	**Signetics** (1694)
EPCI (Enchanced Programmable Communications Interface) Serial/Parallel receiver/transmitter-Synchronous and asynchronous with baud rate generator.			MC2261A	Motorola
			MC2261B	Motorola
			MC2261C	Motorola
	1 Kb/s	5	**MC68661A**	**Motorola** (1506,1512)
	15.6 Kb/s	5	**MC68661C**	**Motorola** (1506,1512)
	62.5 Kb/s	5	**MC68661B**	**Motorola** (1506,1512)
			SCN68661	**Signetics** (1673)
	1000 b/s	5	**SCN2661A**	**Signetics** (1673)
			SCN2661B	**Signetics** (1673)
			SCN2661C	**Signetics** (1673)
IBM 3274/3276 Compatible COAX Receiver/Transmitter	2358	5	COM9004	SMC
Link Controller, X.25 level 2	100	5,12	WD2501-01	Western
			WD2511-01	**Western** (1174)
	500	5,12	WD2501-03	Western
			WD2511-05	**Western** (1174)
	1000	5,12	WD2501-11	Western
			WD2511-11	**Western** (1174)
Manchester Encoder-Decoder	1000	5	**AM7991**	**AMD** (1433,3327)
			MB501	Fujitsu
			HD6409-2	**† Harris** (1493,1497)
			HD6409-9	**Harris** (1493,1497)
			HS15530RH	**† Harris** (4660)
	1250	5	**HD15530-2**	**† Harris** (1493,1498)

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Transmitters–Receivers (Cont'd)

Serial Transmitters- Receivers (Cont'd)

Function	Max Serial Data Rate in kHZ	Supply Voltage, V	Device	Source
Manchester Encoder-Decoder	1250	5		(Cont'd)
			HD15530-9	**Harris (1493,1498)**
			HD15531-2	† Harris
			HD15531-9	Harris
	2500	5	**HD15531B**	**Harris (1493,1499)**
MIL-STD-1553 Dumb Remote Terminal Unit (hybrid)			BUS65101	† DDC
MIL-STD-1553 Encoder/Decoder			MT32008	DDC
MIL-STD-1553 Terminal Bit Processor			BUS-64100	DDC
MPCC (multi-protocol communications controller) Bit and Byte Oriented	1 Mb/s	5	SCN2652A	Signetics
	2 Mb/s	5	**MC2652**	**Motorola (1511)**
			MC2652-2	**Motorola (1511)**
			MC68652	**Motorola (1506,1511)**
			MC68652-2	**Motorola (1506,1511)**
			μPD7201	**NEC (1531)**
			SCN2652A	**Signetics (1670)**
			SCN68652	**Signetics (1670)**
Parallel to Serial Interface	—	5 V	CY232	Cybernetic
PCI (Programmable Communications Interface) Serial/parallel receiver/transmitter—synchronous and asynchronous with baud rate generator.	1000 b/s	5	**SCN2651C**	**Signetics (1669)**
PKCC (Programmable Keyboard and Communications Controller) UART, baud rate generator and keyboard encoder	1000 b/s	5	SC2671ACS	SiliconG
PSAR (Programmable Synchronous-Asynchronous Receiver) Synchronous/Asynchronous serial to parallel converter with programmable character length and programmable serial data rate.	100	−12,5	PT1472B	Western
	640	−12,5	PT1472B-01	Western
		−12,±5	NC2259	Nitron
PSART (Programmable Synchronous-Asynchronous Receiver-Transmitter) Serial to parallel and parallel to serial converter that can operate in Full Duplex Mode.	50	5	8251	Intel
			μPD8251	NEC
PSAT (Programmable Synchronous-Asynchronous Transmitter) Synchronous/Asynchronous parallel to serial converter that has programmable character length and programmable serial data rate.	100	−12,5	PT1482B	Western
	200	−12,±5	NC2257	Nitron
			NC2260	Nitron
	640	−12,5	PT1482B-01	Western
Receiver/Decoder (Bi-Phase)	3500	5	DP8343	National
Receiver/Decoder (Bi-Phase, IBM 3270)	—	5	DP8341	National
SDLC/HDLC/ADCCP Controller	500	5	WD193X-00/10	Western
	1000	5	WD193X-01/11	Western
	1500	5	WD193X-02/12	Western
	2000	5	WD193X-03/13	Western
SPCC (Sync-Protocol Communications Controller) Bit and Byte Oriented	1000	5	F3846	Fairchild
			F6856	**Fairchild (1460)**
Synchronous Receiver/Transmitter (Bi-Sync/SDLC)	800	±5,12	μPD379	NEC
Synchronous Serial Data Adaptor	2 Mb/s	5	**MC6852**	**Motorola (1505)**

Function	Max Serial Data Rate in kHZ	Supply Voltage, V	Device	Source
Transceiver, MIL-STD-1553A/B	1000	±12	BUS-8557	† DDC
		±15/±12	BUS-63105	† DDC
		±15,5	BUS-8553	† DDC
			BUS-8554	† DDC
			BUS-8555/56	† DDC
			BUS-8559	† DDC
Transmitter/Decoder (Bi-Phase, IBM 3270)	—	5	DP8340	National
Transmitter/Encoder (Bi-Phase)	3500	5	DP8342	National
UART, MIL-STD-1553A	1000	5	COM1553A	† SMC
			COM1553B	SMC
UART (Universal Asynchronous Receiver-Transmitter) (complete serial to parallel and parallel to serial interface)	1.2	−12,5	10371	Rockwell
	20	−12,5	TR1402	Western
			TR1602	Western
	30	5	AY3-1015D	GI
		−12,5	MM5303	National
	40	5	COM1863	SMC
			COM8017	SMC
			COM8018	SMC
			COM8502	SMC
		−12,5	COM2017	SMC
			COM2017H	SMC
			COM2502	SMC
			COM2502H	SMC
	56	5	**INS8250**	**National (1514)**
			WD2123	Western
	60	5	TR1863-00	Western
			TR1865-00	Western
	100	5	**82C52**	**† Harris (1482,1494)**
			HD6406	**† Harris (1492,1495)**
			CDP1854AC	**† RCA (1595)**
	125	5	**HD6402C-9**	**Harris (1492)**
	150	5	TR1863-02	Western
			TR1865-02	Western
	200	5	**HD6402-2**	**† Harris (1492)**
			HD6402-9	**Harris (1492)**
			IM6402	**Intersil (3041)**
			IM6402M	**† Intersil (3041)**
			IM6403	**Intersil (3041)**
			IM6403M	**† Intersil (3041)**
			CDP6402D	**† RCA (1595)**
			CDP6402E	**RCA (1595)**
			TR1863-04	Western
			TR1865-04	Western
	800	5	S1602	AMI
			MB8868A	Fujitsu
Universal Communications Interface (Receives or transmits data to serial data bus when addressed and commanded by bus. Links the bus to serial or parallel I/O devices.)	500	−10,5	UMC-16	Trans-Data
Universal Data Bus Dumb Remote Terminal Unit (hybrid)			BUS65201	† DDC
Universal Data Bus Transceiver (hybrid)			BUS63102	† DDC
Universal Digital-Loop Transceiver	80	5	**MC145422**	**Motorola (3536)**
			MC145423	Motorola
			MC145426	**Motorola (3536)**
USRT (universal synchronous receiver-transmitter) Complete serial to parallel and parallel to serial interface.	250	−12,5	COM2601	SMC
	500	5	S2350	AMI

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Transmitters–Receivers (Cont'd)

Function	Max Serial Data Rate in kHZ	Supply Voltage, V	Device	Source	Line
Serial Transmitters- Receivers (Cont'd)					
USYNRT (universal synchronous receiver/transmitter) Multi-Protocol, Bit and Byte Oriented	1500	5,12	COM5025	SMC	
Dual Channel Asynchronous Serial Interface Circuit			MC2681	Motorola	
			MC68681	**Motorola (1506.1512)**	
			SCN68681	Signetics	
Dual Redundant MIL-STD-1553 Remote Terminal Unit (hybrid)			BUS65122	† DDC	5

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

Last Page This Section. Next Page 2801

ABBREVIATIONS OF COMPANY NAMES

Action Ins	Action Instruments
AD	Analog Devices
ADT	Advanced Digital Technology
Advent	Advent Products, Inc.
Alphatron	Alphatron
AMA	American Automation
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
Amperex	Amperex Electronic Corp.
Analogic	Analogic
Analog Sys	Analog Systems
APC	Applied Micro Circuits
Apex	Apex Microtechnology
APM	Applied Microsystems Corp.
Appl Sys	Applied Systems Corp.
APT	Applied Microtechnology
Aptek	Aptek Microsystems
Array Tech	Array Technology
AWI	AWI Electronics
Barvon	Barvon Research
Bedford	Bedford Computer Systems Inc.
Burr-Brown	Burr-Brown
CAE	Computer Aided Engineering
Cal Devices	California Devices
Cermetek	Cermetek
CGRS	CGRS Microtech Inc.
Cherry	Cherry Semiconductor
CIC	Custom Integrated Circuits
CirTech	Circuit Technology
Citel	Citel
Comlinear	Comlinear Corporation
CMA	Custom MOS Arrays
Comark	Comark Corp.
Comdial	Comdial Semiconductor
Comp Auto	Computer Automation
Compas	Compas Microsystems
Cont Logic	Control Logic Inc.
Control Sys	Control Systems Microsystems Div.
CreMicro	Creative Micro Systems
Cromemco	Cromemco, Inc.
Cubit	Cubit Inc.
Curtis	Curtis Electro Devices, Inc.
Cybernetic	Cybernetic Micro Systems
Cybersys	Cybersystems
Cybertek	Cybertek Inc.
Data General	Data General
Data I/O	Data I/O
Data Trans	Data Translation
Datel	Datel
Datricon	Datricon Corporation
DDC	Data Devices Corporation
DEC	Digital Equipment Corporation
Die-Tech	Die-Tech
Digelec	Digelec Corp.
Digitek	Digitek, Inc.
Dionics	Dionics Inc.
Dist Comp	Distributed Computer Systems
Divers Tech	Diversified Technology
E-HI	E-H International, Inc.
EDI	Electronic Designs Inc.
Elind	Elind Elettronica Industriale
EMM-SESCO	EEM-SESCO
Emulogic	Emulogic Inc.
ETI Micro	ETI Micro
Exar	Exar Integrated Systems
Exel	Exel Microelectronics
Fairchild	Fairchild
Ferranti	Ferranti Electric
Force	Force Computers
Fujitsu A	Fujitsu America
Fujitsu	Fujitsu Microelectronics, Inc.
GI	General Instrument
GTE Micro	GTE Microcircuits
Harris	Harris Semiconductor
Heurikon	Heurikon Corp.
Hilevel	Hilevel Technology, Inc.
Hitachi	Hitachi America, Ltd.
Holt	Holt Inc.
HP	Hewlett-Packard
Hughes	Hughes Aircraft, Solid State Products
Hybrid Sys	Hybrid Systems
HyComp	HyComp
ICC	International Cybernetics
IDT	Integrated Device Technology
IMI	International Microcircuits, Inc.
IMP	International Microelectronic Products
IMS	Industrial MicroSystems Inc.
Infosphere	Infosphere
Inmos	Inmos
IntCirEng	Integrated Circuit Engineering
IntCirSys	Integrated Circuit Systems
IntCompSys	Integrated Computer Systems
Int Tech	Integrated Technology Corp.
Intech	Intech Microcircuits Div.
Intel	Intel
Interdesign	Interdesign
Intersil	Intersil
Intronics	Intronics
ITT	ITT Semiconductors
Kinetic Sys	Kinetic Systems
Kontron	Kontron Electronics
Lambda	Lambda Semiconductor
Linear Tech	Linear Technology
LSI Comp	LSI Computer Systems
LSI Logic	LSI Logic Corporation
Master Logic	Master Logic Corporation
Matrix	Matrix Corp.
Matrox	Matrox Electronic Systems
Maxim	Maxim Integrated Products
MCC	Micro-Computer Control
MCE	MCE Electronics
Micrel	Micrel
Micro Innov	Micro Innovators
Micropac	Micropac Industries
Micro Net	Micro Networks
Micro Pwr	Micro Power Systems
Micro Sci	Micro Sciences Corp.
Micro Tech	Microcircuits Technology
Micro-Link	Micro-Link Corporation
Micron	Micron Technology
MilerTron	MilerTronics
Miller	Miller Technology
Mitel	Mitel Semiconductor
Mitsubishi	Mitsubishi Electronics
MMI	Monolithic Memories, Inc.
Mostek	Monolithic Systems Corp.
Motorola	Mostek
MRC	Motorola Semiconductor
Murray	MRC Systems
Monosil	Murray Consulting
National	National Semiconductor
NCM	NCM Corp.
NCR	NCR Corp., Microelectronics Division
NEC	NEC Electronics
Nitron	Nitron
OAE	Oliver Advanced Engineering
Octagon	Octagon Systems Corp.
OEI	Optical Electronics Inc.
Ohio Sci	Ohio Scientic
OKI	OKI Semiconductor
Omnibyte	Omnibyte Corp.
Onset	Onset Computer Corp.
Panasonic	Panasonic
Pico Design	Pico Design
Polycore	Polycore Electronics
Plessey	Plessey Semiconductors
PMI	Precision Monilithics, Inc.
PragDes	Pragmatic Design Inc.
Pro-Log	Pro-Log Corp.
Quay	Quay Corp.
Raytheon	Raytheon Semiconductor
RCA	RCA Solid State Division
RCI Data	RCI Data
RELMS	Relational Memory Systems
Reticon	Reticon
RIFA	RIFA
Rockwell	Rockwell, Microelectronic Devices
RTC	Riehl Time Corporation
Sanyo	Sanyo
SBE	SBE, Inc.
SEEQ	SEEQ Technology, Inc.
SPI	Semi Processes Inc.
Siemens	Siemens
Si-Fab	Si-Fab
Signetics	Signetics
SGS	SGS Semiconductor
Sharp	Sharp
Silicon G	Silicon General
Siliconix	Siliconix
Silicon Sys	Silicon Systems Inc.
Siltronics	Siltronics
SMC	Standard Microsystems Corp.
S MOS	S MOS Systems
Solarise	Solarise Enterprises
Solitron	Solitron Devices
Sprague	Sprague Electric Company
SSM	Solid State Micro Technology for Music
SSS	Solid State Scientific
Stag	Stag Microsystems
STC	Storage Technology Corp.
STD	STD Microsystems
Struc Des	Structured Design Inc.
Stynetic	Stynetic Systems
Sunrise	Sunrise Electronics
Sunshine	Sunshine Semiconductor
Supertex	Supertex Inc.
Symtek	Symtek Corp.
Synertek	Synertek
Sys Innov	Systems Innovations
Tau Zero	Tau Zero Inc.
Technitrol	Technitrol
Tektronix	Tektronix
Teledyne C	Teledyne Crystalonics
Teledyne P	Teledyne Philbrick
Teledyne S	Teledyne Semiconductor
Telefunken	Telefunken
Telmos	Telmos
Teltone	Teltone Corporation
TI	Texas Instruments
Third Domain	Third Domain
Thomson-CSF	Thomson-CSF Components Corp.
Toshiba	Toshiba America
Trans-Data	Trans-Data
TRW	TRW LSI Products
Unitrode	Unitrode
Universal	Universal Semiconductor, Inc.
Varix	Varix Corp.
VLSI Design	VLSI Design Associates
VTI	VLSI Technology, Inc.
Votrax	Votrax
Weitek	Weitek Corporation
Western	Western Digital
Wintek	Wintek Corp.
Xicor	Xicor, Inc.
Xycom	Xycom
Zendex	Zendex Corp.
Zilog	Zilog
ZyMOS	ZyMOS Corporation
Zytrex	Zytrex Corp.

Advanced Micro Devices

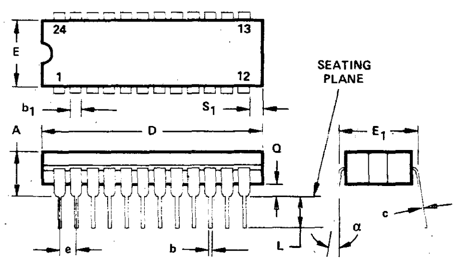
BIPOLAR LSI AND SUPPORT PRODUCTS
High Performance Bus Interface Circuits
The Am29800 Family

DISTINCTIVE CHARACTERISTICS

- Standard I/O pin-out organization
- 48mA Commercial I_{OL}
- 32mA Mil I_{OL}
- Standard clock and output enable pin-outs
- 24-pin slim 0.3 inch wide DIP package
- IMOX Speed
  - 7.5ns typical CP to Y for registers
  - 4.0ns typical D to Y for buffers
- Wide data paths and flexible control
  - 10 bits for video or wide addresses
  - 9 bits for byte plus parity buses
  - 8-bit with multiple enables
- 100% Product assurance screening to MIL-STD-883 requirements

PHYSICAL DIMENSIONS
Dual-In-Line

D-24-SLIM



HERMETIC DUAL IN-LINE PACKAGE

AMD Pkg	D-24-Slim	
Common Name	SLIM CERDIP	
38510 Appendix C	–	
Parameters	Min	Max
A	.140	.220
b	.016	.020
b_1	.045	.065
c	.009	.011
D	1.230	1.285
E	.245	.285
E_1	.290	.320
e	.090	.110
L	.120	.150
Q	.015	.060
S_1	.010	
α	3°	13°

FUNCTIONAL DESCRIPTION

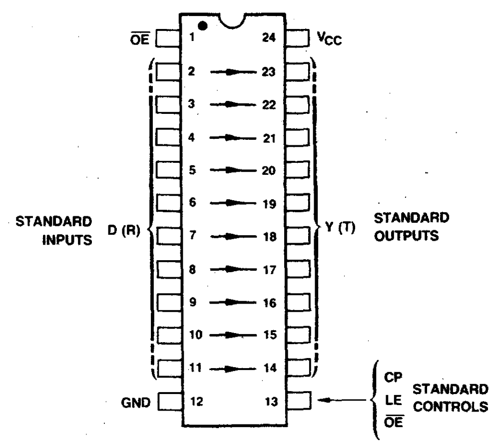
The Am29800 Family provides a completely standardized functional family of registers, latches, buffers, transceivers and parity check-and-regenerate functions optimized for bus interface applications. Each is packaged in the standard 24-pin x 0.3″ wide DIP package to allow LSI functionality in the minimum board area. Board layout is eased by the standardization of inputs on the left and outputs on the right, directly across from each other. Output drive levels are standardized at 48mA Commercial and 32mA Military.

All functions are implemented in AMD's new proprietary IMOX™ (Implanted Micro OXide) process to provide the optimum in speed power product. Typical benchmark speeds are 7.5ns typical CP-to-Y for registers, and 4.0ns typical D-to-Y for buffers.

The basic 29800 Family functions are available in 10-bit, 9-bit and 8-bit configurations with broad control flexibility aimed at minimizing the SSI/MSI content of LSI systems. The 10-bit devices make it easy to interface data plus controls or for 2 parts to interface 20-bit address lines. The 9 bits function are ideal for byte plus parity bus structures. The parity check-and-regenerate functions are designed for interfacing non-parity peripherals to parity organized buses.

All of the functional types have the pin-out format shown below.

STANDARDIZED PIN-OUTS FOR EASY BOARD LAYOUT



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Advanced Micro Devices

BIPOLAR LSI AND SUPPORT PRODUCTS
High Performance Bus Interface Circuits
The Am29800 Family

Am29821/822/823/824/825/826

- High-speed parallel registers with positive edge-triggered D-type flip-flops
  - Noninverting CP-Y t_{PD} = 7.5ns typ
  - Inverting CP-Y t_{PD} = 7.5ns typ
- Buffered common Clock Enable ($\overline{EN}$)
- Buffered common asynchronous Clear input ($\overline{CLR}$)
- Three-state outputs glitch free during power-up and down
- Outputs have Schottky clamp to ground
- 48mA Commercial I_{OL}, 32mA MIL I_{OL}
- High capacitance load capability
- Low capacitance inputs and outputs
- I_{OH} specified 2.0V and 2.4V
- 24-pin 0.3" space saving package

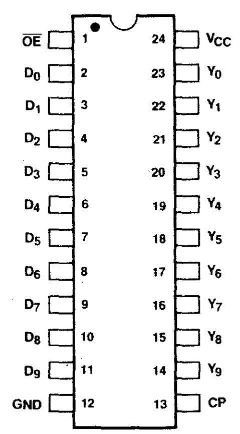
FUNCTIONAL DESCRIPTION

The Am29820 Series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The Am29821 and Am29822 are buffered, 10-bit wide version of the popular '374 function. The Am29823 and Am29824 are 9-bit wide buffered registers with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high performance microprogrammed systems. The Am29825 and Am29826 are 8-bit buffered registers with all the '823/4 controls plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

All of the Am29800 high performance interface family are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

	Device		
	10-Bit	9-Bit	8-Bit
Noninverting	Am29821	Am29823	Am29825
Inverting	Am29822	Am29824	Am29826

Am29821/Am29822
10-BIT REGISTERS



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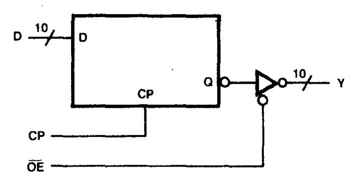

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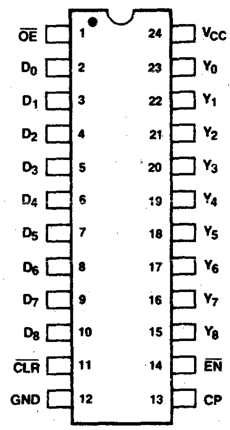
Advanced Micro Devices

BIPOLAR LSI AND SUPPORT PRODUCTS
High Performance Bus Interface Circuits
The Am29800 Family

Am29823/Am29824
9-BIT REGISTERS



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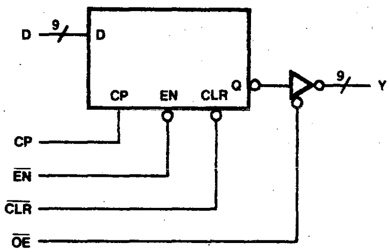
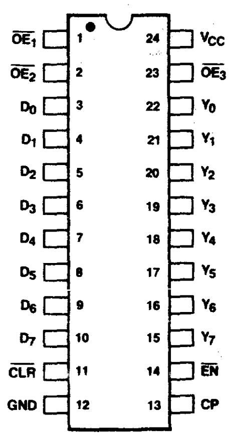
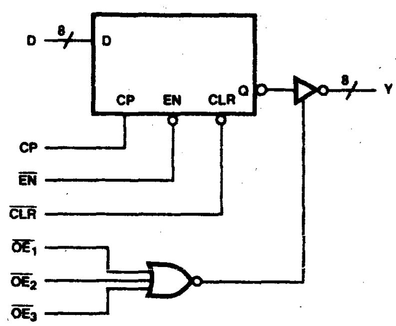


BLI-228

Am29825/Am29826
8-BIT REGISTERS



BLI-229



BLI-230

Advanced Micro Devices

BIPOLAR LSI AND SUPPORT PRODUCTS
High Performance Bus Interface Circuits
The Am29800 Family

Am29827/828,
Am29861/862/863/864

- High-speed symmetrical bidirectional transceivers
  - Noninverting t_{PD} = 4.5ns typ
  - Inverting t_{PD} = 3.0ns typ
- High speed buffers and inverters
  - Noninverting t_{PD} = 4.5ns typ
  - Inverting t_{PD} = 3.0ns typ
- 200mV minimum input hysteresis on input data ports
- Three-state outputs glitch-free during power-up and down
- Outputs have Schottky clamp to ground
- 48mA Commercial I_{OL}, 32mA MIL I_{OL}
- High capacitance load capability
- Low capacitance inputs and outputs
- I_{OH} specified 2.0V and 2.4V
- 24-pin 0.3″ space saving package

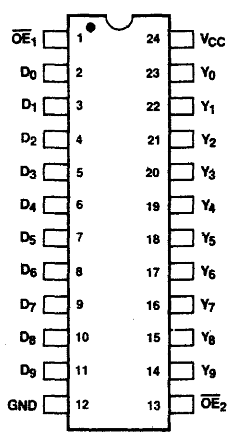
FUNCTIONAL DESCRIPTION

The Am29827 and Am29828 10-bit bus buffers and Am29860 Series bus transceivers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers and 9-bit transceivers have NOR-ed output enables for maximum control flexibility. All buffer and transceiver data inputs have 200mV minimum input hysteresis to provide improved noise rejection.

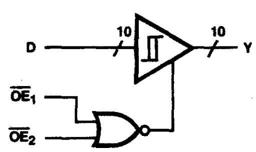
All of the Am29800 high performance interface family are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

	Device		
	10-Bit Buffers	10-Bit Transceivers	9-Bit Transceivers
Noninverting	Am29827	Am29861	Am29863
Inverting	Am29828	Am29862	Am29864

Am29827/Am29828
10-BIT BUS DRIVERS



BLI-237



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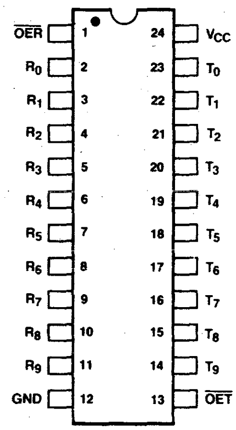
Advanced Micro Devices

INTERFACE

Advanced Micro Devices

BIPOLAR LSI AND SUPPORT PRODUCTS
High Performance Bus Interface Circuits
The Am29800 Family

Am29861/Am29862
10-BIT TRANSCEIVERS



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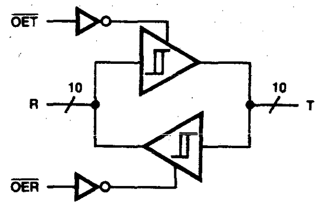
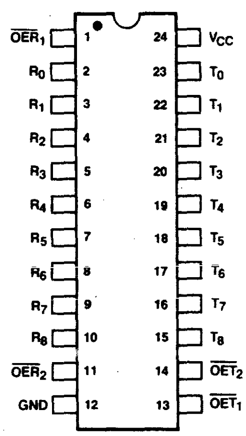
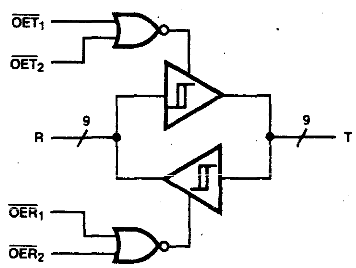


BLI-240

Am29863/Am29864
9-BIT TRANSCEIVERS



BLI-241



BLI-242

Advanced Micro Devices

BIPOLAR LSI AND SUPPORT PRODUCTS
High Performance Bus Interface Circuits
The Am29800 Family

Am29833/834

- High speed bidirectional transceivers for 8-bit non-parity to 9-bit with parity ports
  - Noninverting data t_{PD} = 6.0ns typ
  - Inverting data t_{PD} = 6.0ns typ
  - Parity generate t_{PD} = 9.0ns typ
- High speed parity generation for Transmit mode
- High speed parity fault detection for Receive mode
- Clearable, open-collector output, Fault Flag register
- 200mV minimum input hysteresis
- Three-state outputs glitch-free during power-up and down
- Outputs have Schottky clamp to ground
- 48mA Commercial I_{OL}, 32mA MIL I_{OL}
- High capacitance load capability
- Low capacitance inputs and outputs
- I_{OH} specified 2.0V and 2.4V
- 24-pin 0.3″ space saving package

FUNCTIONAL DESCRIPTION

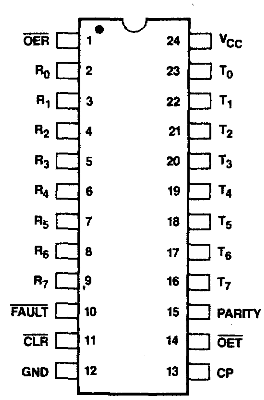
The Am29833 and Am29834 bidirectional transceivers are designed to interface an 8-bit data path without parity to a byte-parity 9-bit data path. All outputs – R_i, T_i and PARITY – have high I_{OL} drive capability and are ideal for device-to-bus or bus-to-bus interfacing.

The internal $\overline{FAULT}$ flag register is configured as a "one's catcher" to capture and hold any odd-parity fault occurring at the rising edge of the clock, CP. A registered $\overline{FAULT}$ output remains LOW until cleared. Also, the $\overline{FAULT}$ output is an open-collector output for wired-OR configurations where byte-parity is used for 16-bit or wider data fuses or where multiple port flags are wired-OR tied together.

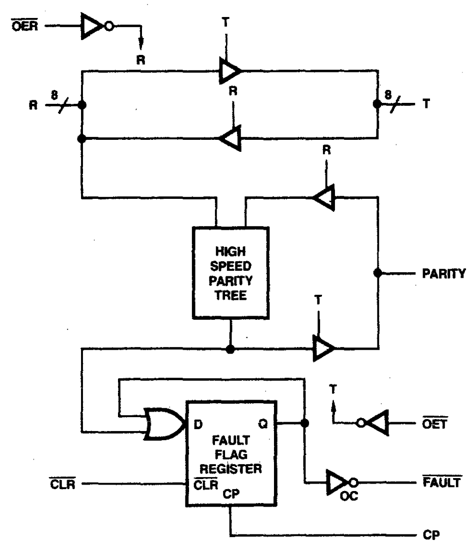
All of the Am29800 high performance interface familiy are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

	Device
Noninverting	Am29833
Inverting	Am29834

Am29833/Am29834
8-BIT TO 9-BIT PARITY TRANSCEIVERS



BLI-243



BLI-244

BIPOLAR LSI AND SUPPORT PRODUCTS
High Performance Bus Interface Circuits
The Am29800 Family

Am29841/842/843/844/845/846

- High-speed parallel latches
  - Noninverting transparent t_{PD} = 4.5ns typ
  - Inverting transparent t_{PD} = 6.0ns typ
- Buffered common latch enable input
- Buffered common clear input
- Buffered common preset input
- Three-state outputs glitch-free during power-up and down
- Outputs have Schottky clamp to ground
- 48mA Commercial I_{OL}, 32mA MIL I_{OL}
- High capacitance load capability
- Low capacitance inputs and outputs
- I_{OH} specified 2.0V and 2.4V
- 24-pin 0.3″ space saving package

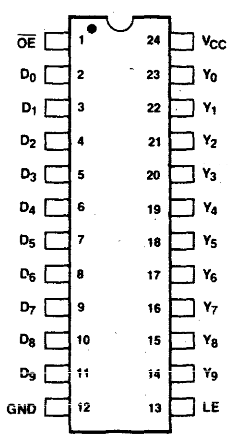
FUNCTIONAL DESCRIPTION

The Am29840 Series bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The Am29841 and Am29842 are buffered, 10-bit wide version of the popular '373 function. The Am29843 and Am29844 are 9-bit wide buffered latches with Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high performance systems. The Am29845 and Am29846 are 8-bit buffered latches with all the '843/4 controls plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

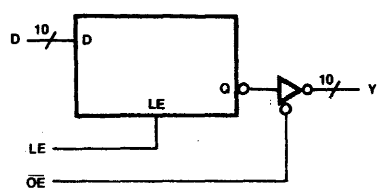
All of the Am29800 high performance interface family are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

	Device		
	10-Bit	**9-Bit**	**8-Bit**
Noninverting	Am29841	Am29843	Am29845
Inverting	Am29842	Am29844	Am29846

Am29841/Am29842
10-BIT LATCHES



BLI-231

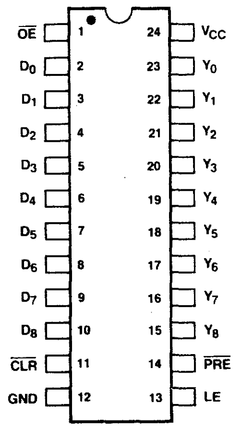


BLI-232

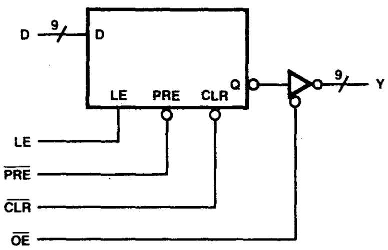
Advanced Micro Devices

BIPOLAR LSI AND SUPPORT PRODUCTS
High Performance Bus Interface Circuits
The Am29800 Family

Am29843/Am29844
9-BIT LATCHES

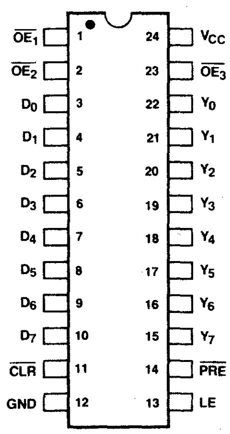


BLI-233

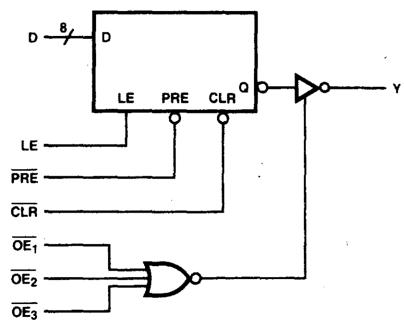


BLI-234

Am29845/Am29846
8-BIT LATCHES



BLI-235



BLI-236

ABBREVIATIONS OF COMPANY NAMES

Action Ins	Action Instruments
AD	Analog Devices
ADT	Advanced Digital Technology
Advent	Advent Products, Inc.
Alphatron	Alphatron
AMA	American Automation
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
Amperex	Amperex Electronic Corp.
Analogic	Analogic
Analog Sys	Analog Systems
APC	Applied Micro Circuits
Apex	Apex Microtechnology
APM	Applied Microsystems Corp.
Appl Sys	Applied Systems Corp.
APT	Applied Microtechnology
Aptek	Aptek Microsystems
Array Tech	Array Technology
AWI	AWI Electronics
Barvon	Barvon Research
Bedford	Bedford Computer Systems Inc.
Burr-Brown	Burr-Brown
CAE	Computer Aided Engineering
Cal Devices	California Devices
Cermetek	Cermetek
CGRS	CGRS Microtech Inc.
Cherry	Cherry Semiconductor
CIC	Custom Integrated Circuits
CirTech	Circuit Technology
Citel	Citel
Comlinear	Comlinear Corporation
CMA	Custom MOS Arrays
Comark	Comark Corp.
Comdial	Comdial Semiconductor
Comp Auto	Computer Automation
Compas	Compas Microsystems
Cont Logic	Control Logic Inc.
Control Sys	Control Systems Microsystems Div.
CreMicro	Creative Micro Systems
Cromemco	Cromemco, Inc.
Cubit	Cubit Inc.
Curtis	Curtis Electro Devices, Inc.
Cybernetic	Cybernetic Micro Systems
Cybersys	Cybersystems
Cybertek	Cybertek Inc.
Data General	Data General
Data I/O	Data I/O
Data Trans	Data Translation
Datel	Datel
Datricon	Datricon Corporation
DDC	Data Devices Corporation
DEC	Digital Equipment Corporation
Die-Tech	Die-Tech
Digelec	Digelec Corp.
Digitek	Digitek, Inc.
Dionics	Dionics Inc.
Dist Comp	Distributed Computer Systems
Divers Tech	Diversified Technology
E-HI	E-H International, Inc.
EDI	Electronic Designs Inc.
Elind	Elind Elettronica Industriale
EMM-SESCO	EEM-SESCO
Emulogic	Emulogic Inc.
ETI Micro	ETI Micro
Exar	Exar Integrated Systems
Exel	Exel Microelectronics
Fairchild	Fairchild
Ferranti	Ferranti Electric
Force	Force Computers
Fujitsu A	Fujitsu America
Fujitsu	Fujitsu Microelectronics, Inc.
GI	General Instrument
GTE Micro	GTE Microcircuits
Harris	Harris Semiconductor
Heurikon	Heurikon Corp.
Hilevel	Hilevel Technology, Inc.
Hitachi	Hitachi America, Ltd.
Holt	Holt Inc.
HP	Hewlett-Packard
Hughes	Hughes Aircraft, Solid State Products
Hybrid Sys	Hybrid Systems
HyComp	HyComp
ICC	International Cybernetics
IDT	Integrated Device Technology
IMI	International Microcircuits, Inc.
IMP	International Microelectronic Products
IMS	Industrial MicroSystems Inc.
Infosphere	Infosphere
Inmos	Inmos
IntCirEng	Integrated Circuit Engineering
IntCirSys	Integrated Circuit Systems
IntCompSys	Integrated Computer Systems
Int Tech	Integrated Technology Corp.
Intech	Intech Microcircuits Div.
Intel	Intel
Interdesign	Interdesign
Intersil	Intersil
Intronics	Intronics
ITT	ITT Semiconductors
Kinetic Sys	Kinetic Systems
Kontron	Kontron Electronics
Lambda	Lambda Semiconductor
Linear Tech	Linear Technology
LSI Comp	LSI Computer Systems
LSI Logic	LSI Logic Corporation
Master Logic	Master Logic Corporation
Matrix	Matrix Corp.
Matrox	Matrox Electronic Systems
Maxim	Maxim Integrated Products
MCC	Micro-Computer Control
MCE	MCE Electronics
Micrel	Micrel
Micro Innov	Micro Innovators
Micropac	Micropac Industries
Micro Net	Micro Networks
Micro Pwr	Micro Power Systems
Micro Sci	Micro Sciences Corp.
Micro Tech	Microcircuits Technology
Micro-Link	Micro-Link Corporation
Micron	Micron Technology
MilerTron	MilerTronics
Miller	Miller Technology
Mitel	Mitel Semiconductor
Mitsubishi	Mitsubishi Electronics
MMI	Monolithic Memories, Inc.
Mostek	Monolithic Systems Corp.
Motorola	Mostek
MRC	Motorola Semiconductor
Murray	MRC Systems
Monosil	Murray Consulting
National	National Semiconductor
NCM	NCM Corp.
NCR	NCR Corp., Microelectronics Division
NEC	NEC Electronics
Nitron	Nitron
OAE	Oliver Advanced Engineering
Octagon	Octagon Systems Corp.
OEI	Optical Electronics Inc.
Ohio Sci	Ohio Scientific
OKI	OKI Semiconductor
Omnibyte	Omnibyte Corp.
Onset	Onset Computer Corp.
Panasonic	Panasonic
Pico Design	Pico Design
Polycore	Polycore Electronics
Plessey	Plessey Semiconductors
PMI	Precision Monilithics, Inc.
PragDes	Pragmatic Design Inc.
Pro-Log	Pro-Log Corp.
Quay	Quay Corp.
Raytheon	Raytheon Semiconductor
RCA	RCA Solid State Division
RCI Data	RCI Data
RELMS	Relational Memory Systems
Reticon	Reticon
RIFA	RIFA
Rockwell	Rockwell, Microelectronic Devices
RTC	Riehl Time Corporation
Sanyo	Sanyo
SBE	SBE, Inc.
SEEQ	SEEQ Technology, Inc.
SPI	Semi Processes Inc.
Siemens	Siemens
Si-Fab	Si-Fab
Signetics	Signetics
SGS	SGS Semiconductor
Sharp	Sharp
Silicon G	Silicon General
Siliconix	Siliconix
Silicon Sys	Silicon Systems Inc.
Siltronics	Siltronics
SMC	Standard Microsystems Corp.
S MOS	S MOS Systems
Solarise	Solarise Enterprises
Solitron	Solitron Devices
Sprague	Sprague Electric Company
SSM	Solid State Micro Technology for Music
SSS	Solid State Scientific
Stag	Stag Microsystems
STC	Storage Technology Corp.
STD	STD Microsystems
Struc Des	Structured Design Inc.
Stynetic	Stynetic Systems
Sunrise	Sunrise Electronics
Sunshine	Sunshine Semiconductor
Supertex	Supertex Inc.
Symtek	Symtek Corp.
Synertek	Synertek
Sys Innov	Systems Innovations
Tau Zero	Tau Zero Inc.
Technitrol	Technitrol
Tektronix	Tektronix
Teledyne C	Teledyne Crystalonics
Teledyne P	Teledyne Philbrick
Teledyne S	Teledyne Semiconductor
Telefunken	Telefunken
Telmos	Telmos
Teltone	Teltone Corporation
TI	Texas Instruments
Third Domain	Third Domain
Thomson-CSF	Thomson-CSF Components Corp.
Toshiba	Toshiba America
Trans-Data	Trans-Data
TRW	TRW LSI Products
Unitrode	Unitrode
Universal	Universal Semiconductor, Inc.
Varix	Varix Corp.
VLSI Design	VLSI Design Associates
VTI	VLSI Technology, Inc.
Votrax	Votrax
Weitek	Weitek Corporation
Western	Western Digital
Wintek	Wintek Corp.
Xicor	Xicor, Inc.
Xycom	Xycom
Zendex	Zendex Corp.
Zilog	Zilog
ZyMOS	ZyMOS Corporation
Zytrex	Zytrex Corp.

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S4521

32 BIT DRIVER

Features

- ☐ Drives Up to 32 Devices
- ☐ Cascadable
- ☐ On Chip Oscillator
- ☐ Requires Only 3 Control Lines
- ☐ CMOS Construction For:
  Wide Supply Range
  High Noise Immunity
  Wide Temperature Range

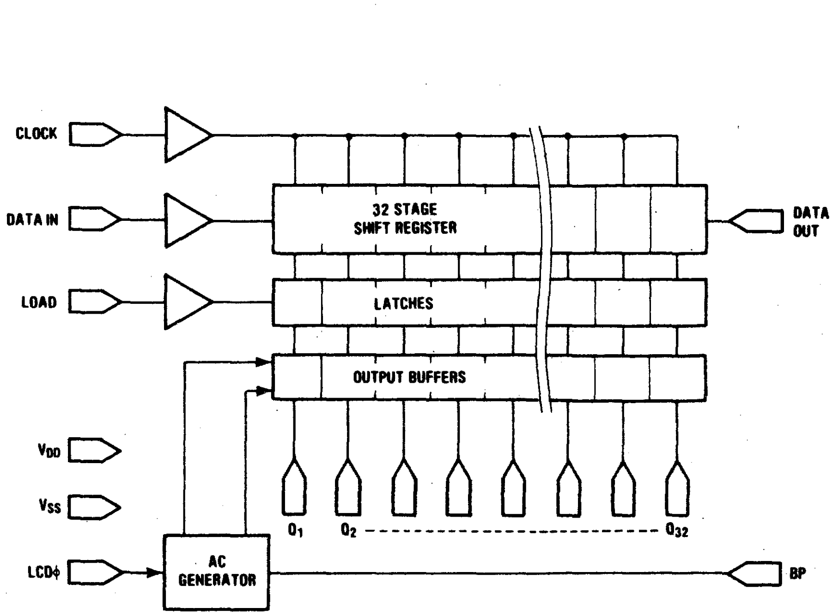
Applications:

- ☐ Liquid Crystal Displays
- ☐ LED and Incandescent Displays
- ☐ Solenoids
- ☐ Print Head Drives
- ☐ DC and Stepping Motors
- ☐ Relays

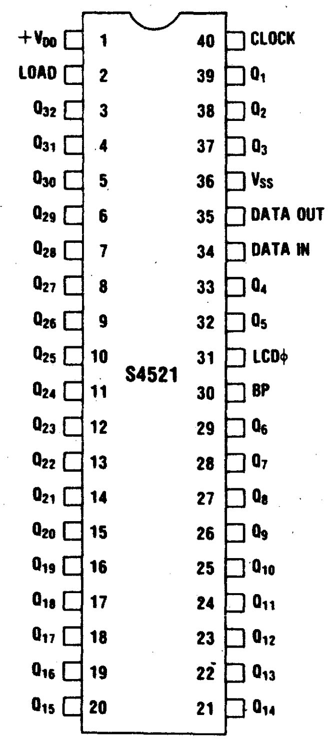
General Description

The AMI S4521 is an MOS/LSI circuit that drives a variety of output devices, usually under microprocessor control. This device requires only three control lines due to its serial input construction. It latches the data to be output, relieving the microprocessor from the task of generating the required waveform, or it may be used to bring data directly to the drivers. The part acts as a versatile peripheral to drive displays, motors, relays and solenoids within its output limitations. It is especially well suited to driving liquid crystal displays, with a backplane A.C. signal option that is provided. The A.C. frequency of the backplane output that can be user supplied or generated by attaching a capacitor to the LCDϕ input, which controls the frequency of the internal oscillator. One circuit will drive up to 32 devices and more can be driven by cascading several drivers together.

Functional Block Diagram



Pin Configuration



S4534

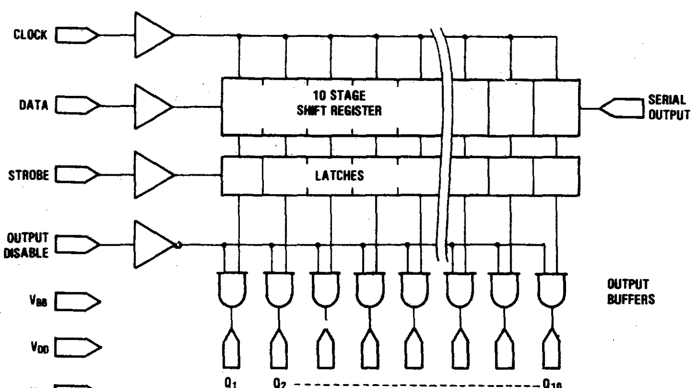
10 BIT, HIGH VOLTAGE HIGH CURRENT DRIVER

Features
- ☐ Outputs Capable of 60 Volt Swings at 25mA
- ☐ Drives Up to 10 Devices
- ☐ Cascadable
- ☐ Requires Only 4 Control Lines

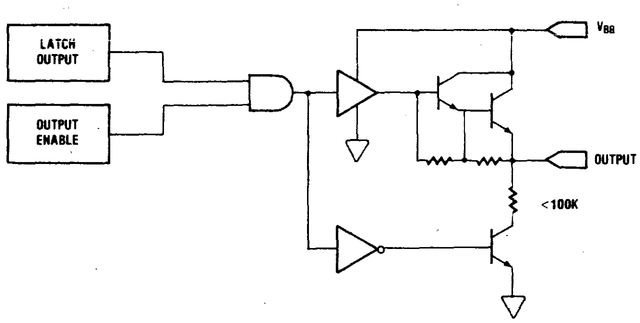
Applications:
- ☐ Vacuum Fluorescent Displays
- ☐ LED and Incandescent Displays
- ☐ Solenoids
- ☐ Print Head Drives
- ☐ DC and Stepping Motors
- ☐ Relays

General Description
The AMI S4534 is a high voltage, high current MOS/LSI circuit that drives a variety of output devices, usually under microprocessor control, by converting low level signals such as TTL, and CMOS to high voltage, high current drive signals. This device requires only four control lines due to its serial input construction. It latches the data to be output, or it may be used to bring data directly to the driver. The part acts as a versatile peripheral to drive displays, motors, relays and solenoids within its output limitations of a 60 volt swing and up to 50mA per drive. It is especially well suited to drive vacuum fluorescent displays due to its high voltage output capability. One circuit will drive up to 10 devices and more can be driven by cascading several drivers together.

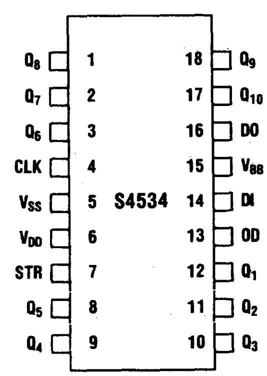
Functional Block Diagram



Output Buffer (Functional Diagram)



Pin Configuration



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S4535

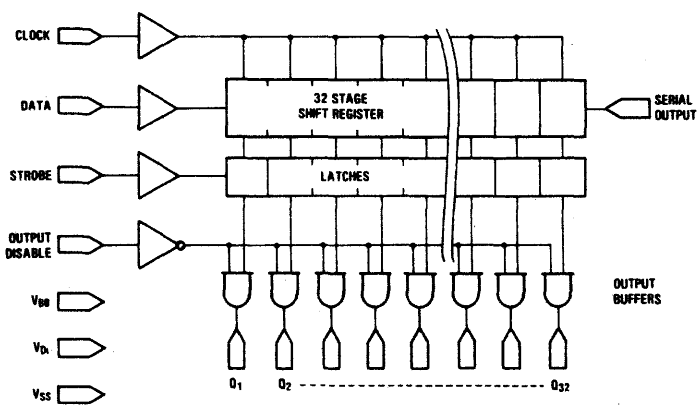
32 BIT, HIGH VOLTAGE DRIVER

Features
- ☐ High Voltage Outputs Capable of 60 Volt Swing
- ☐ Drives Up to 32 Devices
- ☐ Cascadable
- ☐ Requires Only 4 Control Lines

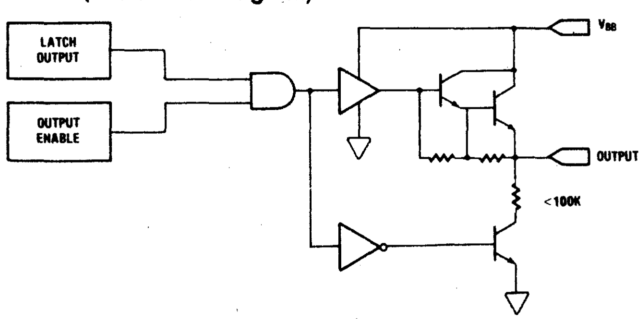
Applications:
- ☐ Vacuum Fluorescent Displays
- ☐ LED and Incandescent Displays
- ☐ Solenoids
- ☐ Print Head Drives
- ☐ DC and Stepping Motors
- ☐ Relays

General Description
The AMI S4535 is a high voltage MOS/LSI circuit that drives a variety of output devices, usually under microprocessor control, by converting low level signals such as TTL, and CMOS to high voltage, high current drive signals. This device requires only four control lines due to its serial input construction. It latches the data to be output, or it may be used to bring data directly to the driver. The part acts as a versatile peripheral to drive displays, motors, relays and solenoids within its output limitations of a 60 volt swing and up to 25mA per drive. It is especially well suited to drive vacuum fluorescent displays due to its high voltage output capability. One circuit will drive up to 32 devices and more can be driven by cascading several drivers together.

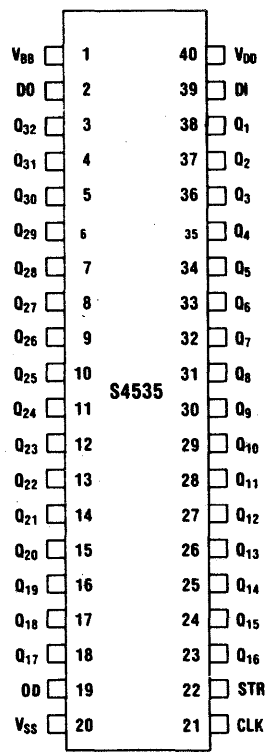
Functional Block Diagram



Output Buffer (Functional Diagram)



Pin Configuration



LPC-10 SPEECH SYNTHESIZER WITH ON-CHIP 20K SPEECH DATA ROM

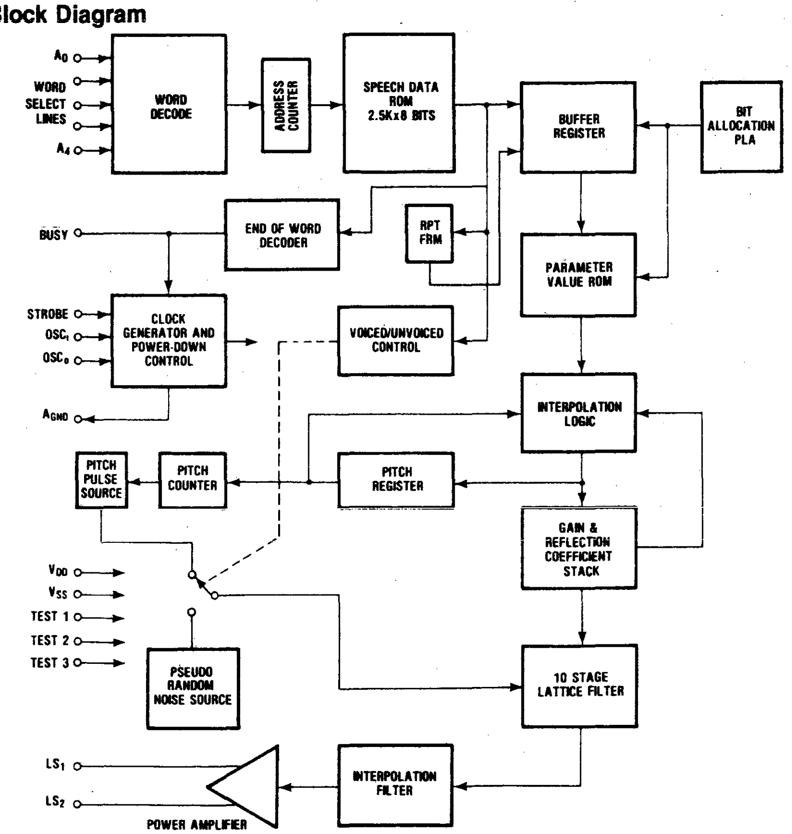
Features

- ☐ Simple Digital Interface
- ☐ CMOS Switched-Capacitor Filter Technology
- ☐ Automatic Powerdown
- ☐ 5-8 Volts Single Power Supply Operation
- ☐ Direct Loudspeaker Drive
- ☐ 20mW Audio Output
- ☐ 20K Bits Speech ROM
- ☐ Low Data Rate
- ☐ Up to 32 Word Vocabulary

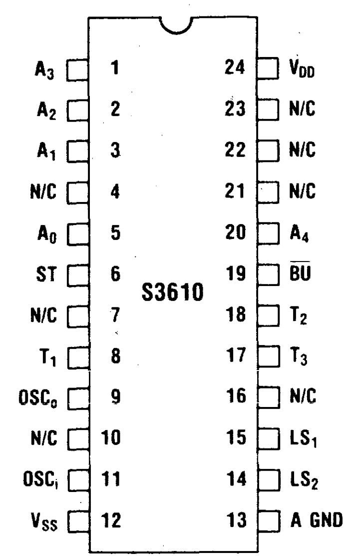
General Description

The S3610 LPC-10 Speech Synthesizer generates speech of high quality and intelligibility from LPC (Linear Predictive Coding) data stored in an internal 20K bit ROM. The simple digital interface consists of 5 word-select lines, a strobe input to load the address data and initiate operation, and a busy output signal. At the end of enunciation the chip automatically goes into the powerdown mode until a new word select address is strobed in. The data rate from the speech ROM into the synthesizer is 2.0K bits/sec max. Typically the average data rate will be reduced to about 1.2K bits/sec. by means of the data rate reduction techniques used internally.

Block Diagram



Pin Configuration



N/C = NO CONNECTION

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S3620

LPC-10 SPEECH SYNTHESIZER

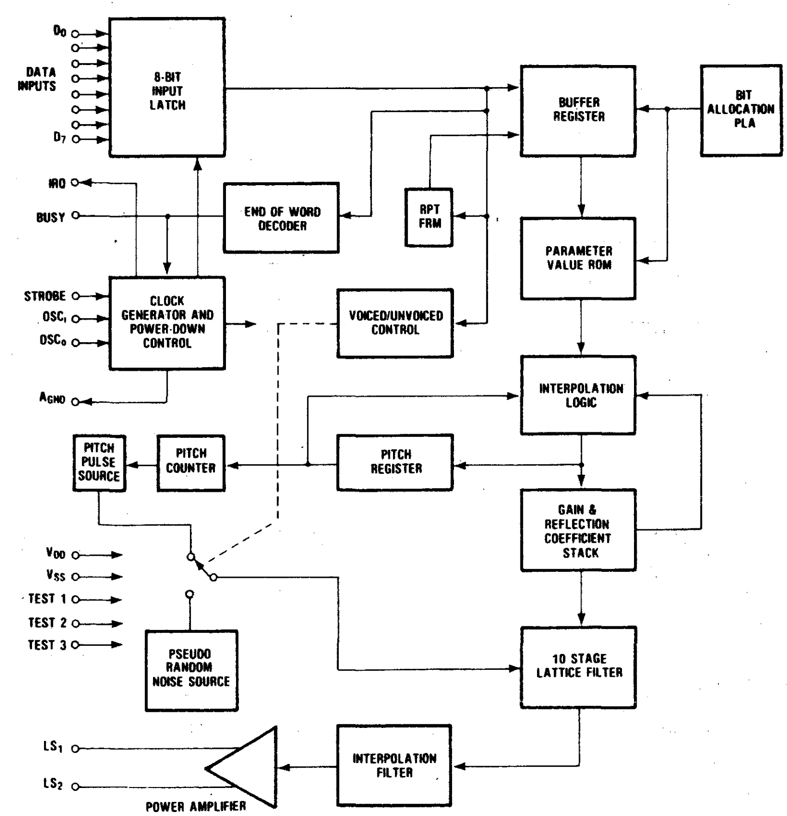
Features

- ☐ Simple Microprocessor Interface
- ☐ CMOS Switched-Capacitor Filter Technology
- ☐ Automatic Powerdown
- ☐ 5-8 Volts Single Power Supply Operation
- ☐ Direct Loudspeaker Drive
- ☐ 20mW Audio Output
- ☐ Low Data Rate

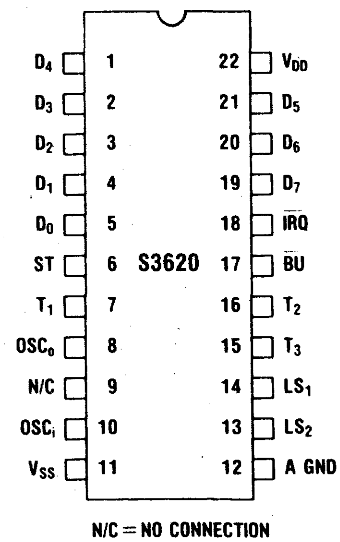
General Description

The S3620 LPC-10 Speech Synthesizer generates speech of high quality and intelligibility from LPC (Linear Predictive Coding) data stored in an external memory. The digital interface circuitry is fully microprocessor compatible and allows the processor to load the data with or without a DMA controller. The loading takes place on a handshake basis, and in the absence of a response from the processor the synthesizer automatically shuts down and goes into the powerdown mode. A busy signal allows the processor to sense the status of the synthesizer.

Block Diagram



Pin Configuration



N/C = NO CONNECTION

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Telex (842) 614596F

HOLLAND
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HONG KONG
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TURKEY
EMPA Elektronik (Mamulleri Pazarlama AS)
Tersane Cad. Kuthan 38/408
Tr-Kara Koy — Istanbul, Turkey
Tel. (11) 496249
Telex 24429

WEST GERMANY
Astronic GmbH
Winzererstrasse 47d
8000 Munich 40,
West Germany
Tel. (089) 309031
Telex (841) 5216187

Hearst
HEARST BUSINESS COMMUNICATIONS, INC./UTP DIVISION
645 Stewart Avenue, Garden City, NY 11530 (516) 222-2500 TWX: 510-222-1673

ANALOG DEVICES

Quad 12-Bit Microprocessor-Compatible D/A Converter

AD390*

FEATURES
Four Complete 12-Bit DACs in One IC Package
Linearity Error ±1/2LSB T_{min} – T_{max} (AD390K, T)
Factory-Trimmed Gain and Offset
Buffered Voltage Output
Monotonicity Guaranteed Over Full Temperature Range
Double-Buffered Data Latches
Includes Reference and Buffer
Fast Settling: 8µs max to ±1/2LSB
Low Cost

PRODUCT DESCRIPTION

The AD390 contains four 12-bit high speed voltage-output digital-to-analog converters in a compact 28-pin hybrid package. The design is based on a proprietary latched 12-bit DAC chip which reduces chip count and provides high reliability. The AD390 is ideal for systems requiring digital control of many analog voltages where board space is at a premium. Such applications include automatic test equipment, process controllers, and vector-scan displays.

The AD390 is laser-trimmed to ±1/2LSB max nonlinearity (AD390KD, TD) and absolute accuracy of ±0.05 percent of full scale. The high initial accuracy is made possible by the use of thin-film scaling resistors on the monolithic DAC chips. The internal buried zener voltage reference provides excellent temperature drift characteristics (20ppm/°C) and an initial tolerance of ±0.03% maximum. The internal reference buffer allows a single common reference to be used for multiple AD390 devices in large systems.

The individual DACs are accessed by the $\overline{CS1}$ through $\overline{CS4}$ control inputs and the $\overline{A0}$ and $\overline{A1}$ lines. These control signals permit the registers of the four DACs to be loaded sequentially and the outputs to be simultaneously updated.

The AD390 outputs are calibrated for a ±10V output range with positive-true offset binary input coding. A 0 to +10V version is available on special order.

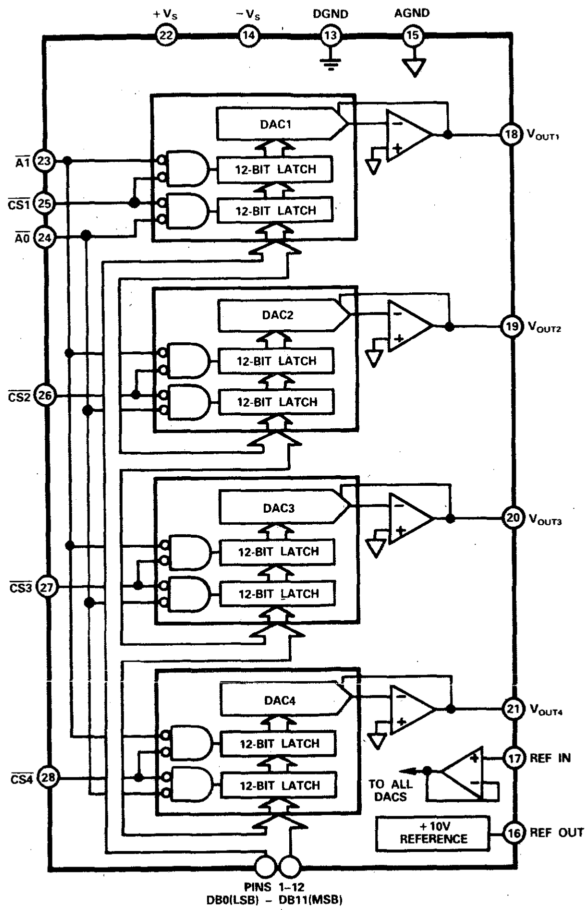
The AD390 is packaged in a 28-lead ceramic package and is specified for operation over the 0 to +70°C and −55°C to +125°C temperature range.

ORDERING GUIDE

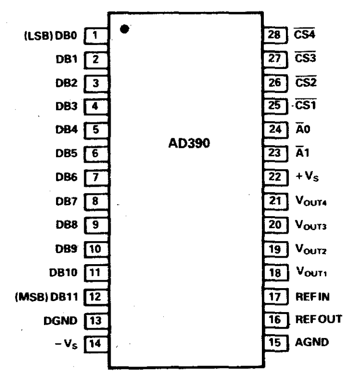
Model	Temperature Range	Gain Error 25°	Linearity Error $T_{min}-T_{max}$
AD390JD	0 to +70°C	±4LSB	±3/4LSB
AD390KD	0 to +70°C	±2LSB	±1/2LSB
AD390SD	−55°C to +125°C	±4LSB	±3/4LSB
AD390TD	−55°C to +125°C	±2LSB	±1/2LSB

*Covered by patent numbers 3,803,590; 3,890,611; 3,932,863; 3,978,473; 4,020,486 and other patents pending.

AD390 FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION TOP VIEW



ANALOG DEVICES

DACPORT™ Low Cost Complete μP-Compatible 8-Bit DAC

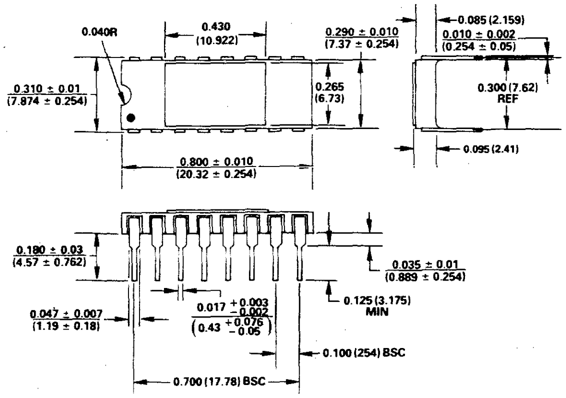
AD558*

FEATURES
Complete 8-Bit DAC
Voltage Output – 2 Calibrated Ranges
Internal Precision Band-Gap Reference
Single-Supply Operation: +5V to +15V
Full Microprocessor Interface
Fast: 1μs Voltage Settling to ±1/2LSB
Low Power: 75mW
No User Trims
Guaranteed Monotonic Over Temperature
All Errors Specified T_{min} to T_{max}
Small 16-Pin DIP Package
Single Laser-Wafer-Trimmed Chip for Hybrids
Low Cost

PRODUCT DESCRIPTION
The AD558 DACPORT is a complete voltage-output 8-bit digital-to-analog converter, including output amplifier, full microprocessor interface and precision voltage reference on a single monolithic chip. No external components or trims are required to interface, with full accuracy, an 8-bit data bus to an analog system.

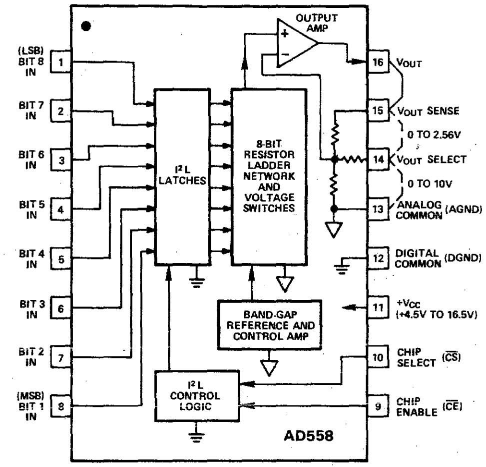
The performance and versatility of the DACPORT is a result of several recently-developed monolithic bipolar technologies. The complete microprocessor interface and control logic is implemented with integrated injection logic (I^2L), an extremely dense and low-power logic structure that is process-compatible with linear bipolar fabrication. The internal precision voltage reference is the patented low-voltage band-gap circuit which permits full-accuracy performance on a single +5V to +15V power supply. Thin-film silicon-chromium resistors provide the stability required for guaranteed monotonic operation over the entire operating temperature range (all grades), while recent advances in laser-wafer-trimming of these thin-film resistors permit absolute calibration at the factory to within ±1LSB; thus no user-trims for gain or offset are required. A new circuit design provides voltage settling to ±1/2LSB for a full-scale step in 800ns.

OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).



*Covered by U.S. Patent Nos. 3,887,863; 3,685,045; 4,323,795; Patents Pending. DACPORT is a trademark of Analog Devices, Inc.

AD558 FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS
1. The 8-bit I^2L input register and fully microprocessor-compatible control logic allow the AD558 to be directly connected to 8- or 16-bit data buses and operated with standard control signals. The latch may be disabled for direct DAC interfacing.
2. The laser-trimmed on-chip SiCr thin-film resistors are calibrated for absolute accuracy and linearity at the factory. Therefore, no user trims are necessary for full rated accuracy over the operating temperature range.
3. The inclusion of a precision low-voltage band-gap reference eliminates the need to specify and apply a separate reference source.
4. The voltage-switching structure of the AD558 DAC section along with a high-speed output amplifier and laser-trimed resistors give the user a choice of 0V to +2.56V or 0V to +10V output ranges, selectable by pin-strapping. Circuitry is internally compensated for minimum settling time on both ranges; typically settling to ±1/2LSB for a full-scale 2.55 volt step in 800ns.
5. The AD558 is designed and specified to operate from single +4.5V to +16.5V power supply.

AD558 ORDERING GUIDE

Model	Temperature	Relative Accuracy Error Max T_{min} to T_{max}	Full-Scale Error, Max T_{min} to T_{max}
AD558JN	0 to +70°C	±1/2LSB	±2.5LSB
AD558KN	0 to +70°C	±1/4LSB	±1LSB
AD558JD	0 to +70°C	±1/2LSB	±2.5LSB
AD558KD	0 to +70°C	±1/4LSB	±1LSB
AD558SD	−55°C to +125°C	±3/4LSB	±2.5LSB
AD558TD	−55°C to +125°C	±3/8LSB	±1LSB

ANALOG DEVICES

Microprocessor-Compatible Voltage Output 12-Bit D/A Converter

AD667

FEATURES

- Single Chip Construction
- Double-Buffered Latch for 8-Bit µP-Compatibility
- On Chip Output Amplifier
- High Stability Buried Zener Reference On Chip
- Monotonicity Guaranteed Over Temperature
- Linearity Guaranteed Over Temperature: 1/2LSB max (AD667K)
- Guaranteed for Operation with ±12V or ±15V Supplies
- Low Power
- TTL/5V CMOS Compatible Logic Inputs
- Low Cost

PRODUCT DESCRIPTION

The AD667 is a complete voltage output 12-bit digital-to analog converter including a high stability buried zener voltage reference, an output amplifier and double-buffered input latch on a single chip. The converter uses 12 precision high speed bipolar current steering switches and a laser trimmed thin film resistor network to provide fast settling time and high accuracy.

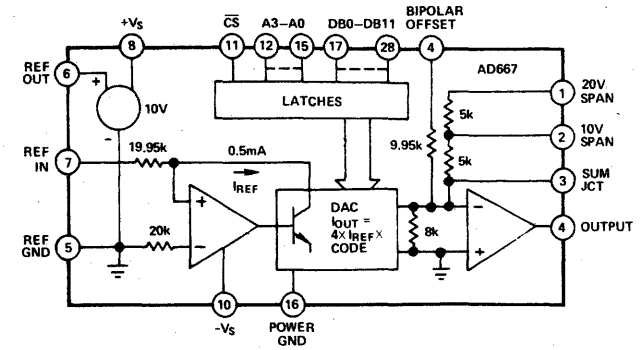
Microprocessor compatibility is achieved by the on-chip double-buffered latch. The design of the input latch allows direct interface to 4-, 8-, 12-, or 16-bit buses. The 12 bits of data from the first rank of latches can then be transferred to the second rank, avoiding generation of spurious analog output values. The latch responds to strobe pulses as short as 100ns, allowing use with the fastest available microprocessors.

The functional completeness and high performance in the AD667 results from a combination of advanced switch design, high speed bipolar manufacturing process, and the proven laser wafer-trimming (LWT) technology. The AD667 is trimmed at the wafer level and is specified to ±1/4LSB maximum linearity error (K grade) at 25°C and ±1/2LSB over the full operating temperature range.

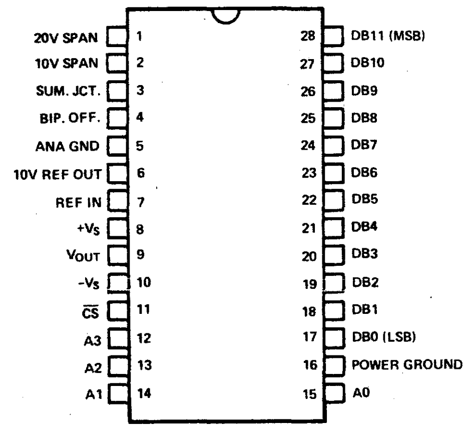
The subsurface (buried) Zener diode on the chip provides a low-noise voltage reference which has long-term stability and temperature drift characteristics comparable to the best discrete reference diodes. The laser trimming process which provides the excellent linearity is also used to trim both the absolute value of the reference as well as its temperature coefficient. The AD667 is thus well suited for wide temperature range performance with ±1/2LSB maximum linearity error and guaranteed monotonicity over the full temperature range. Typical full scale gain T.C. is 10ppm/°C.

The AD667 is available in four performance grades. The AD667J and K are specified for use over the 0 to +70°C temperature range and is available in a 28-pin hermetically-sealed, ceramic DIP. The AD667S grade is specified for the -55°C to +125°C range and is available in the ceramic package.

AD667 FUNCTIONAL BLOCK DIAGRAM



AD667 PINOUT

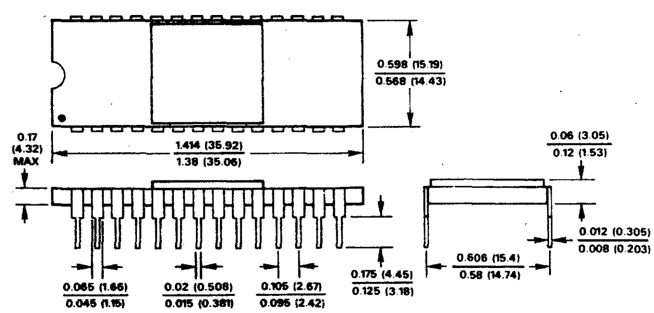


AD667 ORDERING GUIDE

Model	Package	Temp. Range	Linearity Error max @ 25°C	Gain T.C. max
AD667JD	Ceramic	Com	±1/2LSB	50ppm/°C
AD667KD	Ceramic	Com	±1/4LSB	20ppm/°C
AD667SD	Ceramic	Mil	±1/2LSB	30ppm/°C

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



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ANALOG DEVICES

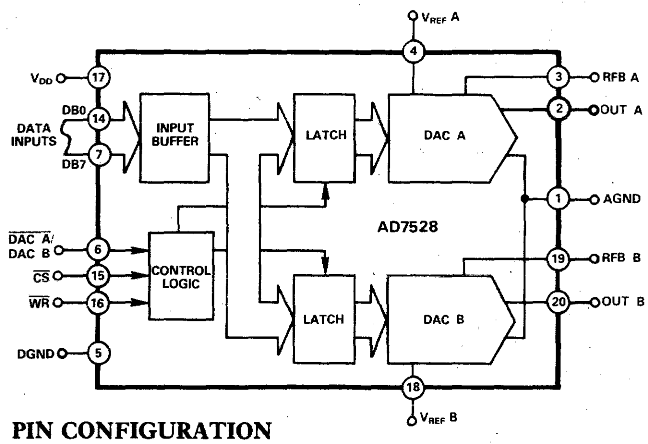
CMOS Dual 8-Bit Buffered Multiplying DAC

AD7528

FEATURES
On-Chip Latches for Both DACs
+5V to +15V Operation
DACs Matched to 1%
Four Quadrant Multiplication
TTL/CMOS Compatible
Latch Free (Protection Schottkys not Required)

APPLICATIONS
Digital Control of:
- Gain/Attenuation
- Filter Parameters
- Stereo Audio Circuits
- X–Y Graphics

AD7528 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION
The AD7528 is a monolithic dual 8-bit digital/analog converter produced in a small 0.3" wide 20-pin DIP, featuring excellent DAC-to-DAC matching.

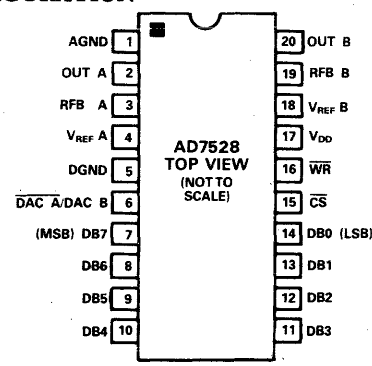
Separate on-chip latches are provided for each DAC to allow easy microprocessor interface.

Data is transferred into either of the two DAC data latches via a common 8-bit TTL/CMOS compatible input port. Control input DAC A/DAC B determines which DAC is to be loaded. The AD7528's load cycle is similar to the write cycle of a random access memory and the device is bus compatible with most 8-bit microprocessors, including 6800, 8080, 8085, Z80.

The device operates from a +5V to +15V power supply, dissipating only 20mW of power.

Both DACs offer excellent four quadrant multiplication characteristics with a separate reference input and feedback resistor for each DAC.

PIN CONFIGURATION

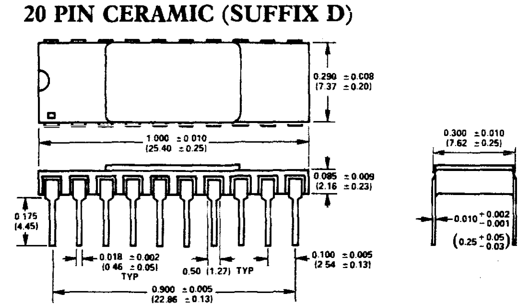


ORDERING INFORMATION

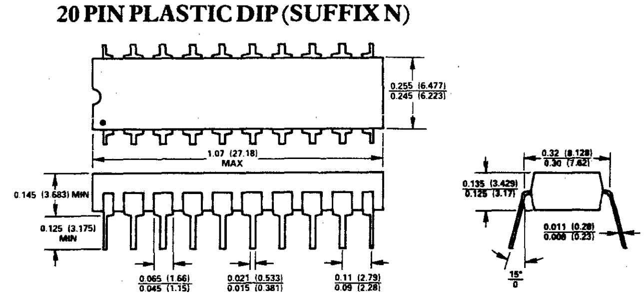
Relative Accuracy	Gain Error $T_A = +25°C$	Temperature Range and Package: Plastic 0 to +70°C	Cerdip −25°C to +85°C	Ceramic −55°C to +125°C
±1LSB	±4LSB	AD7528JN	AD7528AQ	AD7528SD
±1/2LSB	±2LSB	AD7528KN	AD7528BQ	AD7528TD
±1/2LSB	±1LSB	AD7528LN	AD7528CQ	AD7528UD

MECHANICAL INFORMATION
OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

20 PIN CERAMIC (SUFFIX D)



20 PIN PLASTIC DIP (SUFFIX N)



ANALOG DEVICES

LC²MOS High Speed 12-Bit Voltage DAC

AD7240

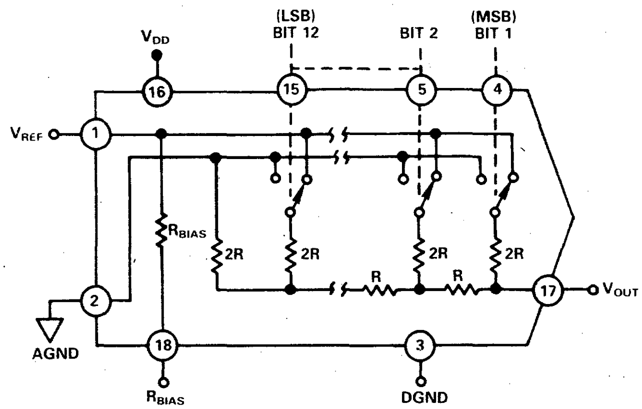
FEATURES

- Fast Voltage Settling Time: 550ns to 0.01%
- Total Unadjusted Error: 1LSB max
- Single Supply Operation
- Latch Up Proof (No Protection Schottky Required)
- Superb Differential Nonlinearity: 1/2LSB max over Temperature
- Low Power Dissipation: 30mW

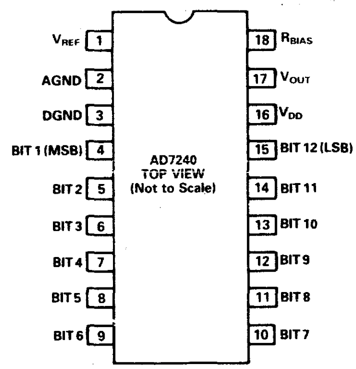
APPLICATIONS

- Battery Powered Instrumentation
- High Speed A/D Converters
- Programmable Gain Amplifiers
- Vector Graphics
- S/D Converters

AD7240 FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



GENERAL DESCRIPTION

The Analog Devices AD7240 is a fast settling (550ns typically to 1/2LSB) 12-bit voltage output digital to analog converter. It is fabricated using an advanced high speed Linear Compatible CMOS process (LC²MOS) which has been specifically developed to allow high speed digital logic circuits and precision analog circuits to be integrated on the same chip.

The AD7240 operates with single +15 volts V_{DD} supply and exhibits exceptionally fast settling times due to the small (and code independent) value of capacitance at the output of the DAC.

The AD7240 also gives superior performance to other CMOS DACs when configured in the current steering mode as a multiplying DAC.

ORDERING INFORMATION

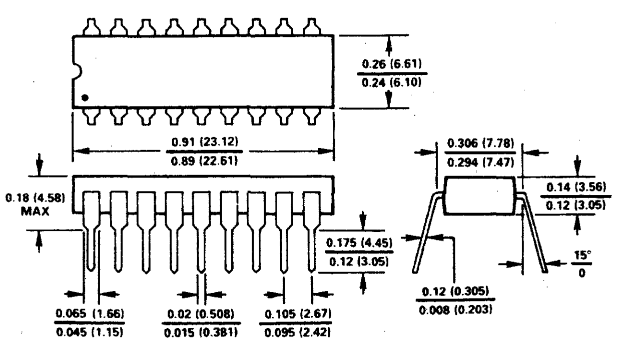
Total Unadjusted Error	Plastic	Cerdip	Side Brazed Ceramic
$T_A = T_{MIN}$ to T_{MAX}	0 to +70°C	−25°C to +85°C	−55°C to +125°C
+1/2, −2LSB	AD7240JN	AD7240AQ	AD7240SD
+1/4, −1 1/2LSB	AD7240KN	AD7240BQ	AD7240TD

MECHANICAL INFORMATION

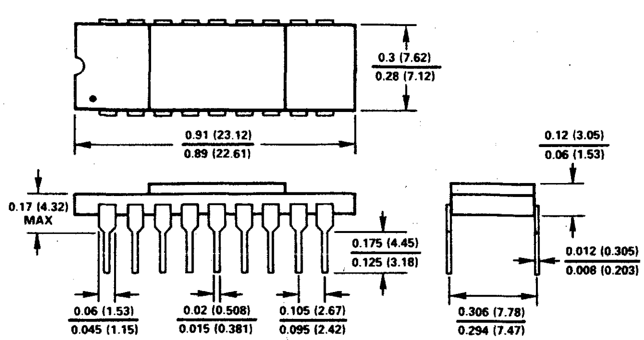
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

18-PIN PLASTIC DIP – SUFFIX N



18-PIN CERAMIC DIP – SUFFIX D



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ANALOG DEVICES

CMOS 12-Bit Buffered Multiplying DAC

AD7545

FEATURES
- 12-Bit Resolution
- Low Gain T.C.: 2ppm/°C typ
- Fast TTL Compatible Data Latches
- Single +5V to +15V Supply
- Small 20-Pin 0.3″ DIP
- Latch Free (Schottky Protection Diode Not Required)
- Low Cost
- Ideal for Battery Operated Equipment

GENERAL DESCRIPTION

The AD7545 is a monolithic 12-bit CMOS multiplying DAC with on-board data latches. It is loaded by a single 12-bit wide word and interfaces directly to most 12- and 16-bit bus systems. Data is loaded into the input latches under the control of the $\overline{CS}$ and $\overline{WR}$ inputs; tying these control inputs low makes the input latches transparent allowing direct unbuffered operation of the DAC.

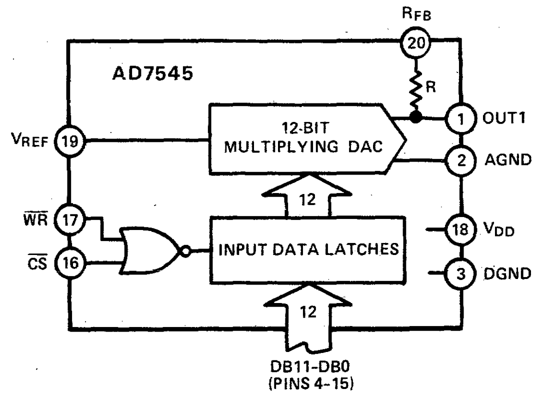
The AD7545 is particularly suitable for single supply operation and applications with wide temperature variations.

The AD7545 can be used with any supply voltage from +5V to +15V. With CMOS logic levels at the inputs the device dissipates less than 0.5mW for V_{DD} = +5V.

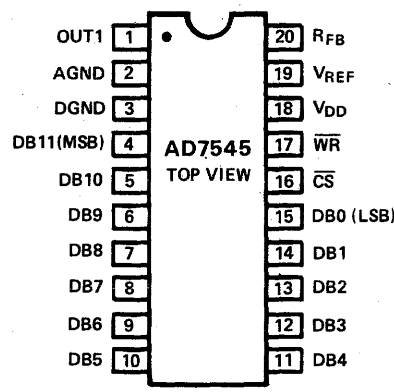
ORDERING INFORMATION

Relative Accuracy	Maximum Gain Error T_A = +25°C V_{DD} = +5V	Temperature Range and Package: Plastic 0 to +70°C	Cerdip -25°C to +85°C	Ceramic -55°C to +125°C
±2LSB	±20LSB	AD7545JN	AD7545AQ	AD7545SD
±1LSB	±10LSB	AD7545KN	AD7545BQ	AD7545TD
±1/2LSB	±5LSB	AD7545LN	AD7545CQ	AD7545UD
±1/2LSB	±1LSB	AD7545GLN	AD7545GCQ	AD7545GUD

AD7545 FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

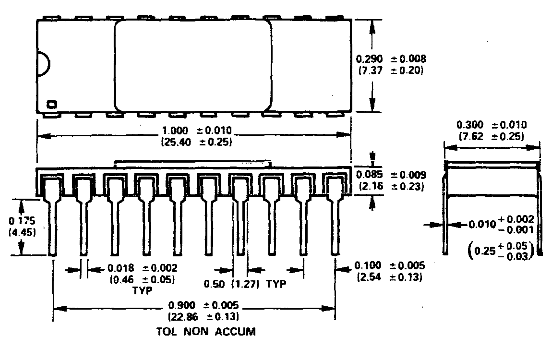


MECHANICAL INFORMATION

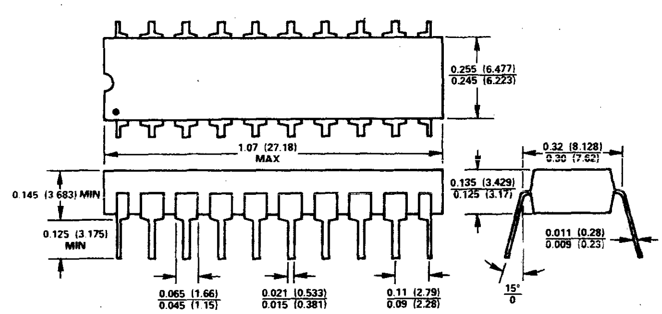
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

20-PIN CERAMIC DIP (SUFFIX D)



20-PIN PLASTIC DIP (SUFFIX N)



ANALOG DEVICES

LC² MOS 8-Bit μP Compatible 12-Bit DAC

AD7548

FEATURES
8-Bit Bus Compatible 12-Bit DAC
All Grades 12-Bit Monotonic Over Full Temperature Ranges
Operation Specified at +5V, +12V or +15V Power Supply
Low Gain Drift of 5ppm/°C Maximum
Full 4 Quadrant Multiplication
Small 20-Pin Package

APPLICATIONS
8-Bit Microprocessor Based Control Systems
Programmable Amplifiers
Function Generation
Servo Control

GENERAL DESCRIPTION
The AD7548 is a 12-bit monolithic CMOS D/A converter for use with 8-bit bus microprocessors. Data is loaded in two bytes to input holding registers as shown in the block diagram opposite. The AD7548 can be configured to accept either left- or right-justified data, least significant byte or most significant byte first, using standard TTL compatible control inputs.

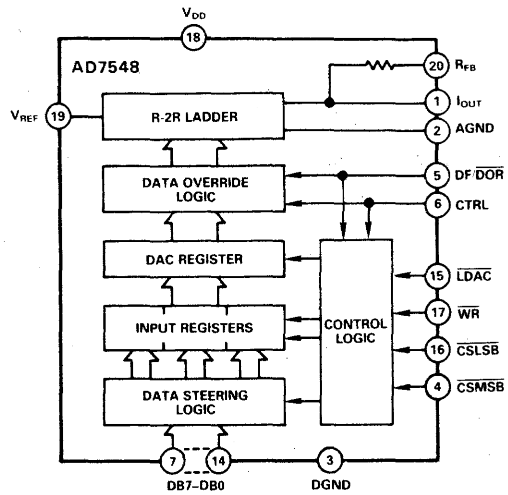
A separate load DAC control input allows the user the choice of updating the analog output coincident with loading new data to the DAC input register or at any time after the data loading event. This feature is especially important in multi-DAC systems where simultaneous update of all DACs is required.

The new Linear Compatible CMOS (LC² MOS) process used in the manufacture of the AD7548 allows precision thin-film linear circuitry and high-speed low-power CMOS logic to be integrated on the same small chip. The high-speed logic allows direct interfacing to most of the popular 8-bit microprocessors.

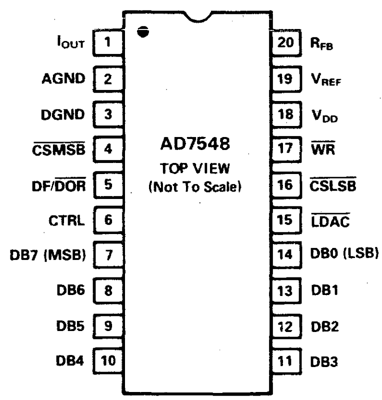
ORDERING INFORMATION

Relative Accuracy T_{MIN} to T_{MAX}	Full Scale Error T_{MIN} to T_{MAX}	Temperature Range and Package		
		Plastic 0 to +70°C	Cerdip −40°C to +85°C	Ceramic −55°C to +125°C
±1LSB	±6LSB	AD7548JN	AD7548AQ	AD7548SD
±1/2LSB	±3LSB	AD7548KN	AD7548BQ	AD7548TD

AD7548 FUNCTIONAL BLOCK DIAGRAM

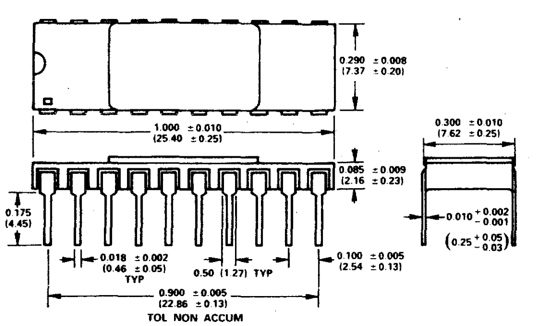


PIN CONFIGURATION

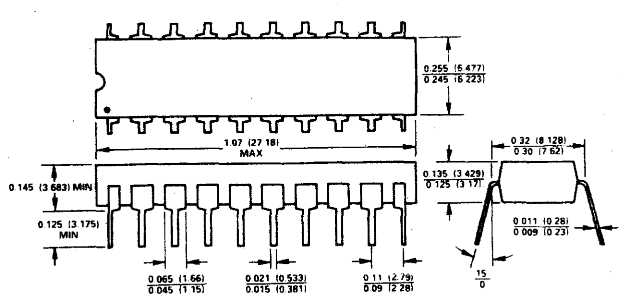


MECHANICAL INFORMATION
OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

20-PIN CERAMIC DIP (SUFFIX D)



20-PIN PLASTIC DIP (SUFFIX N)



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ANALOG DEVICES

14-Bit, 200kHz Digital-to-Analog Converter

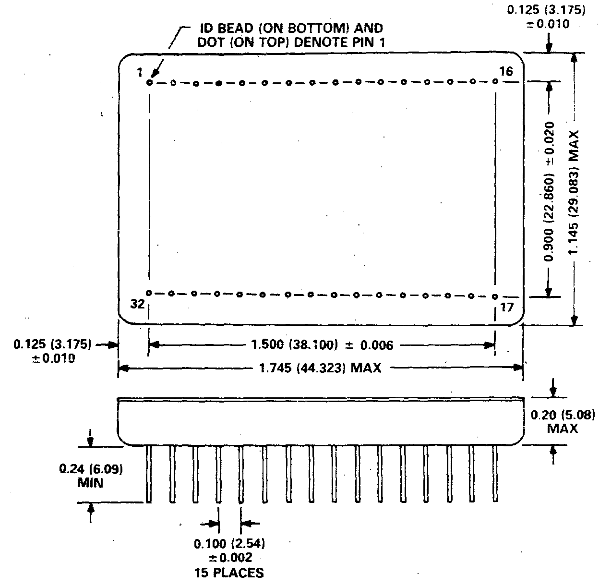
HDD-1409

FEATURES
- 14-Bit Resolution
- 200kHz Word Rates
- RZ Gated Output
- 32-Pin DIP

APPLICATIONS
- FDM/TDM Transmultiplexers
- Digital Signal Processing
- PCM Systems
- Digital Audio

OUTLINE DIMENSIONS

Dimensions shown in inches and mm



GENERAL DESCRIPTION

The HDD-1409KM D/A converter is a voltage-output, 32-pin hybrid digital-to-analog converter complete with input registers, current-output D/A, switching circuits, and output amplifier. The unit is capable of converting 14-bit digital inputs into gated analog output voltages at update rates from dc through 200kHz.

Monolithic ICs and hybrid microelectronic packaging have been combined in a grounded metal case hybrid which provides cost, space, and power savings for the system designer. The HDD-1409 is a complete solution for converting high-resolution digital data into "clean" analog voltages and accomplishes it with maximum power dissipation of only 600 milliwatts.

The HDD-1409 D/A has been characterized with a companion A/D converter, the HAS-1409KM, to emphasize the superior ac performance which makes the A/D – D/A combination especially attractive for use in Frequency Division Multiplex/Time Division Multiplex (FDM/TDM) transmultiplexer systems. But the design concepts and versatility which are incorporated into it also make the HDD-1409 useful in Pulse Code Modulation (PCM) and other digital signal processing applications.

The analog output voltage range is ±5V; output impedance is 600 ohms, ideal for filter matching. The D/A output operates in a return-to-zero (RZ) mode, which provides deglitching and allows selecting the optimum duty cycle for FDM/TDM and PCM applications.

Small size, low power, and multiple functions in a single package make the HDD-1409 D/A converter attractive for a wide range of data processing uses.

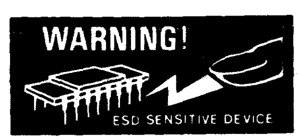
HDD-1409 PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	SIGNAL	17	DIGITAL GROUND
2	$\overline{\text{SIGNAL}}$	18	BIT 8
3	GATE	19	BIT 7
4	DIGITAL GROUND	20	BIT 6
5	ANALOG GROUND	21	BIT 5
6	N/C	22	BIT 4
7	+5V	23	BIT 3
8	DIGITAL GROUND	24	BIT 2
9	LOW STROBE	25	$\overline{\text{BIT 1 (MSB)}}$
10	BIT 14 (LSB)	26	HIGH STROBE
11	BIT 13	27	−15V
12	BIT 12	28	+15V
13	BIT 11	29	ANALOG OUTPUT
14	BIT 10	30	ANALOG GROUND
15	BIT 9	31	ANALOG GROUND
16	DIGITAL GROUND	32	ANALOG GROUND

NOTES:
WHEN USING WITH HAS-1409 A/D, CONNECT $\overline{\text{BIT 1 (MSB)}}$ OF A/D (PIN 22) to BIT 1 (MSB) OF HDD-1409 D/A (PIN 25).
TO USE HDD-1409 D/A AS STAND-ALONE DEVICE WITH OFFSET BINARY INPUT, APPLY BIT 1 DIGITAL INPUT SIGNAL TO $\overline{\text{SIGNAL}}$ (PIN 1) AND CONNECT SIGNAL (PIN 2) TO $\overline{\text{BIT 1 (MSB)}}$ (PIN 25).
TO LOAD 14-BIT DATA FULLY PARALLEL, CONNECT HIGH STROBE (PIN 26) AND LOW STROBE (PIN 9) TOGETHER EXTERNALLY.

CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.



ANALOG DEVICES

Ultra High-Speed IC D/A Converter

AD9768

FEATURES

5ns Settling Time
100MHz Update Rate
20mA Output Current
ECL-Compatible
40MHz Multiplying Mode

APPLICATIONS

Raster Scan & Vector Graphic Displays
High-Speed Waveform Generation
Digital VCOs
Ultra-Fast Digital Attenuators

GENERAL DESCRIPTION

The Analog Devices AD9768SD D/A converter is a monolithic current-output converter which can accept 8 bits of ECL-level digital input voltages and convert them into analog signals at update rates as high as 100MHz. In addition to its use as a standard D/A converter, it can also be utilized as a two-quadrant multiplying D/A at multiplying bandwidths as high as 40MHz.

An inherently low glitch design is used, and the complementary current outputs are suitable for driving transmission lines directly. Nominal full-scale output is 20mA, which corresponds to a 1-volt drop across a 50Ω load, or ±1 volt across 100Ω returned to +1 volt. The actual output current is determined by the on-chip reference voltage ($V_{REF} \approx -1.26V$) and an external current setting resistor, R_{SET}.

Full-scale output current I_{OUT} with digital "1" at all inputs is calculated with the equation:

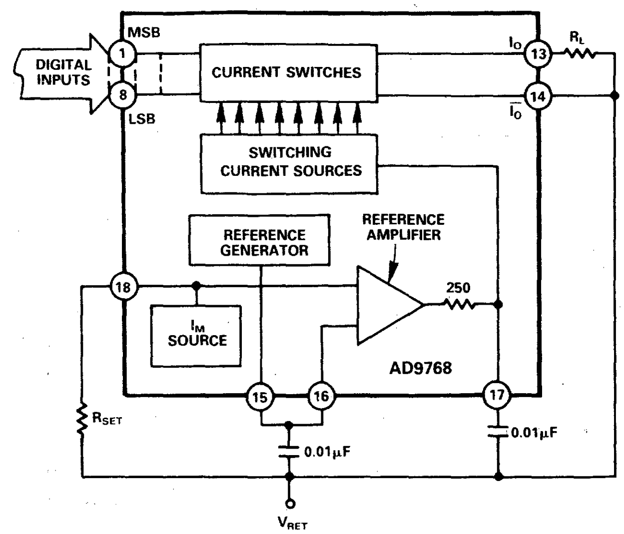
$$I_{OUT} = 4 \times \frac{V_{RET} - V_{REF}}{R_{SET}}$$

The setting resistor R_{SET} and the output load resistor should both have low temperature coefficients. A complementary $\overline{I_{OUT}}$ is also provided.

The reference voltage source is a modified bandgap type and is nominally −1.26 volts. This reference supply requires no external regulation. To reduce the possibility of noise generation and/or instability, pin 15 (REFERENCE OUT) can be decoupled using a high-quality ceramic chip capacitor. Stabilization of the internal loop amplifier is by a single capacitor connected from pin 17 (COMPENSATION) to ground. The minimum value for this capacitor is 3900pF, although a 0.01μF ceramic chip capacitor is recommended.

The incredible speed characteristics of the AD9768SD D/A converter make it attractive for a wide range of high-speed applications. The ability of the unit to operate as a two-quadrant multiplying D/A converter adds another dimension to its usefulness and makes the AD9768SD a truly versatile device.

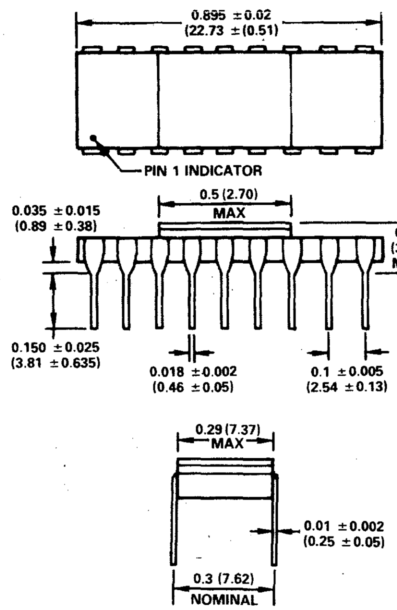
AD9768 FUNCTIONAL BLOCK DIAGRAM



(Conventional Operation)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



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Digital-to-Analog Converters

FEATURE SELECTION CHART

		AD1408	AD DAC80-I	AD DAC80-V	AD DAC85-I	AD DAC85-V	AD DAC-08	AD561	AD DAC100	AD558	AD7524	AD7522	AD7527 SYSTEMS DAC	AD7528 DUAL DAC	AD7523	AD7520	AD7530	AD7533	AD7521	AD7531	AD7541	AD7541A	AD7240
		GENERAL PURPOSE					FAST			µP BUS COMPATIBLE			SPECIAL PURPOSE			MULTIPLYING							
Resolution	8 Bits	•					•			•	•			•	•								
	10 Bits							•	•			•	•			•	•	•					
	12 Bits		•	•	•	•													•	•	•	•	•
Accuracy	8 Bits	•					•			•	•	•		•	•	•	•	•	•	•			
	10 Bits							•	•		•	•	•		•	•	•	•	•	•			
	12 Bits		•	•	•	•															•	•	•
Output Format	Current	•	•		•		•	•	•		•	•	•	•	•	•	•	•	•	•	•	•	
	Voltage			•		•				•													•
Internal Reference			•	•	•	•		•	•	•													
Multiplication Capability	2 Quadrant	•					•	•	•		•	•	•	•	•	•	•	•	•	•	•	•	•
	4 Quadrant										•	•	•	•	•	•	•	•	•	•	•	•	
Logic Compatible with	TTL	•	•	•	•	•	•	•	•	•	•	•		•		•	•	•	•	•	•	•	•
	CMOS	•					•	•		•	•	•	•	•	•	•	•	•	•	•	•	•	
Input Coding	Binary	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	BCD		•	•	•	•																	
Second Source		•	•	•	•	•	•		•		•	•			•	•	•	•	•	•	•	•	
Single Power Supply										•													•
Input Data Latch Structure	Serial											•											
	Parallel									•	•	•	•	•									
Operating Temperature Ranges[1]	C = 0 to +70°C	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	I = −25°C to +85°C				•	•					•	•	•	•	•	•	•	•	•	•	•	•	•
	M = −55°C to +125°C	•			•	•	•	•	•	•	•	•	•	•	•	•		•	•		•	•	•
Low Power										•	•	•	•	•	•	•	•	•	•	•	•	•	•
Dice Availability							•	•		•	•	•			•	•		•	•		•		

NOTE
[1] C = Commercial I = Industrial M = Military

GENERAL PURPOSE SPECIFICATIONS (maximum @ +25°C unless otherwise noted as typical)

Model	Resolution	Relative Accuracy	Differential Nonlinearity	Gain T.C. ppm/°C	Settling Time	Temp Range[1]	I/V Out	Input Logic	Package
AD DAC-08	8 Bits	±0.19%	Monotonicity	50	135ns	M	I	TTL &	DIP
AD DAC-08A	8 Bits	±0.1%	Guaranteed	50	135ns	M	I	CMOS	DIP
AD DAC-08C	8 Bits	±0.39%		80	135ns	C	I		DIP
AD DAC-08E	8 Bits	±0.19%		50	135ns	C	I		DIP
AD DAC-08H	8 Bits	±0.1%		50	135ns	C	I		DIP
AD1408-7	8 Bits	±0.39%	±2LSB	20 typ	250ns typ	C	I	TTL &	DIP
AD1408-8	8 Bits	±0.19%	±1LSB	20 typ	250ns typ	C	I	CMOS	DIP
AD1408-9	8 Bits	±0.1%	±1/2LSB	20 typ	250ns typ	C	I		DIP
AD1508-8	8 Bits	±0.19%	±1LSB	20 typ	250ns typ	M	I		DIP
AD1508-9	8 Bits	±0.1%	±1/2LSB	20 typ	250ns typ	M	I		DIP
AD DAC80(Z)-CBI-V[2]	12 Bits	±0.012%	±3/4LSB	30	3µs typ	C	V	TTL	DIP
AD DAC80(Z)-CBI-I[2]	12 Bits	±0.012%	±3/4LSB	30	300ns typ	C	I		DIP
AD DAC80(Z)-CCD-V[2]	3 Digits	±0.024%	±1/2LSB	30	3µs typ	C	V		DIP
AD DAC80(Z)-CCD-I[2]	3 Digits	±0.024%	±1/2LSB	30	300ns typ	C	I		DIP
AD DAC85C-CBI-V	12 Bits	±0.012%	±1/2LSB	20	3µs typ	C	V	TTL	DIP
AD DAC85C-CBI-I	12 Bits	±0.012%	±1/2LSB	20	300ns typ	C	I		DIP
AD DAC85C-CCD-V	3 Digits	±0.024%	±1/2LSB	20	3µs typ	C	V		DIP
AD DAC85C-CCD-I	3 Digits	±0.024%	±1/2LSB	20	300ns typ	C	I		DIP
AD DAC85(LD)-CBI-V	12 Bits	±0.012%	±1/2LSB	20 (10)	3µs typ	I	V		DIP
AD DAC85(LD)-CBI-I	12 Bits	±0.012%	±1/2LSB	20 (10)	300ns typ	I	I		DIP
AD DAC85-CCD-V	3 Digits	±0.024%	±1/2LSB	20	3µs typ	I	V		DIP
AD DAC85-CCD-I	3 Digits	±0.025%	±1/2LSB	20	300ns typ	I	I		DIP
AD DAC85MIL-CBI-V	12 Bits	±0.012%	±1/2LSB	20	3µs typ	M	V		DIP
AD DAC85MIL-CBI-I	12 Bits	±0.012%	±1/2LSB	20	300ns typ	M	I		DIP
AD DAC100JD	10 Bits	±0.1%	GMOT[3]	±60	375ns	I	I	TTL &	DIP
AD DAC100KD	10 Bits	±0.05%	GMOT[3]	±30	375ns	I	I	DTL	DIP
AD DAC100LD	10 Bits	±0.05%	GMOT[3]	±15	375ns	I	I		DIP
AD DAC100SD	10 Bits	±0.1%	GMOT[3]	±60	375ns	M	I		DIP
AD DAC100TD	10 Bits	±0.05%	GMOT[3]	±30	375ns	M	I		DIP
AD561JD	10 Bits	±0.05%	±1/2LSB	80	250ns typ	C	I	TTL &	DIP
AD561KD	10 Bits	±0.025%	±1/2LSB	30	250ns typ	C	I	CMOS	DIP
AD561SD	10 Bits	±0.05%	±1/2LSB	60	250ns typ	M	I		DIP
AD561TD	10 Bits	±0.025%	±1/2LSB	30	250ns typ	M	I		DIP

NOTES
[1] C = 0 to +70°C, I = −25°C to +85°C, M = −55°C to +125°C
[2] "Z" models specified for operation on ±12V supplies
[3] Guaranteed Monotonic Over Temperature

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ANALOG DEVICES

Digital-to-Analog Converters

MULTIPLYING SPECIFICATIONS (maximum @ +25°C unless otherwise noted as typical)

Model	Resolution	Relative Accuracy	Differential Nonlinearity	Gain T.C. ppm/°C	Settling Time	Temp Range[1]	I/V Out	Input Logic	Package
AD7523JN(AD)(SD)	8 Bits	±0.2%	Monotonicity	66/50/30	150ns typ	C/I/M	I	CMOS	DIP
AD7523KN(BD)	8 Bits	±0.1%	Guaranteed	66/50	150ns typ	C/I	I		DIP
AD7523LN(CD)	8 Bits	±0.05%		66/50	150ns typ	C/I	I		DIP
AD7520JN(JD)(SD)	10 Bits	±0.2%	±0.4%	10	500ns typ	C/I/M	I	CMOS &	DIP
AD7520KN(KD)(TD)	10 Bits	±0.1%	±0.2%	10	500ns typ	C/I/M	I	TTL	DIP
AD7520LN(LD)(UD)	10 Bits	±0.05%	±0.1%	10	500ns typ	C/I/M	I		DIP
AD7530JN(JD)	10 Bits	±0.2%	±0.4%	10	500ns typ	C/I	I	CMOS &	DIP
AD7530KN(KD)	10 Bits	±0.1%	±0.2%	10	500ns typ	C/I	I	TTL	DIP
AD7530LN(LD)	10 Bits	±0.05%	±0.1%	10	500ns typ	C/I	I		DIP
AD7533JN(AD)(SD)	10 Bits	±0.2%	±0.4%	22/16/10	600ns	C/I/M/M	I	CMOS & TTL	DIP
AD7533KN(BD)(TD)	10 Bits	±0.1%	±0.2%	22/16/10	600ns	C/I/M/M	I	CMOS & TTL	DIP
AD7533LN(LD)(UD)	10 Bits	±0.05%	±0.1%	22/16/10	600ns	C/I/M/M	I	CMOS & TTL	DIP
AD7521JN(JD)(SD)	12 Bits	±0.2%	±0.4%	10	500ns typ	C/I/M	I		DIP
AD7521KN(KD)(TD)	12 Bits	±0.1%	±0.2%	10	500ns typ	C/I/M	I	CMOS &	DIP
AD7521LN(LD)(UD)	12 Bits	±0.05%	±0.1%	10	500ns typ	C/I/M	I	TTL	DIP
AD7531JN(JD)	12 Bits	±0.2%	±0.4%	10	500ns typ	C/I	I		DIP
AD7531KN(KD)	12 Bits	±0.1%	±0.2%	10	500ns typ	C/I	I	CMOS &	DIP
AD7531LN(LD)	12 Bits	±0.05%	±0.1%	10	500ns typ	C/I	I	TTL	DIP

NOTE
[1] C = 0 to +70°C, I = –25°C to +85°C, M = –55°C to +125°C

μP COMPATIBLE SPECIFICATIONS (maximum @ +25°C unless otherwise noted as typical)

Model	Resolution	Relative Accuracy	Differential Nonlinearity	Gain T.C. ppm/°C	Settling Time	Temp Range[1]	I/V Out	Input Logic	Package
AD558JD(SD)	8 Bits	±1/2LSB	Monotonicity	±2LSB	800ns typ	C/M	V	TTL &	DIP
AD558KD(TD)	8 Bits	±1/4LSB	Guaranteed	±2LSB	800ns typ	C/M	V	CMOS	DIP
AD7524JN(AD)(SD)	8 Bits	±0.2%	Monotonicity	10	100ns	C/I/M	I	TTL &	DIP
AD7524KN(BD)(TD)	8 Bits	±0.1%	Guaranteed	10	100ns	C/I/M	I	CMOS	DIP
AD7524LN(CD)(UD)	8 Bits	±0.05%		10	100ns	C/I/M	I		DIP
AD7522JN(JD)(SD)	10 Bits	±0.2%	±0.4%	10	500ns typ	C/I/M	I	TTL &	DIP
AD7522KN(KD)(TD)	10 Bits	±0.1%	±0.2%	10	500ns typ	C/I/M	I	CMOS	DIP
AD7522LN(LD)(UD)	10 Bits	±0.05%	±0.1%	10	500ns typ	C/I/M	I		DIP
DUAL MULTIPLYING									
AD7528JN(AQ)(SD)	8 Bits	±1LSB	±1LSB	±35[2]	200ns[2]	C/I/M	I	TTL &	DIP
AD7528KN(LN)	8 Bits	±1/2LSB	±1LSB	±35[2]	200ns[2]	C	I	CMOS	DIP
AD7528BQ(CQ)	8 Bits	±1/2LSB	±1LSB	±35[2]	200ns[2]	I	I	TTL &	DIP
AD7528TD(UD)	8 Bits	±1/2LSB	±1LSB	±35[2]	200ns[2]	M	I	CMOS	DIP
SYSTEMS DAC[3]									
AD7527KN(BD)(TD)	10 Bits	±1LSB	±2LSB	5	–	C/I/M	I	CMOS	DIP
AD7527LN(CD)(UD)	10 Bits	±0.5LSB	±1LSB	5	–	C/I/M	I	CMOS	DIP
AD7527GLN(GCD)(GUD)	10 Bits	±0.5LSB	±1LSB	5	–	C/I/M	I	CMOS	DIP

NOTES
[1] C = 0 to +70°C, I = –25°C to +85°C, M = –55°C to +125°C
[2] +15V supply
[3] Has double-buffered latches, data readback, data override, L/R - justified data, increment/decrement

HIGH PERFORMANCE SPECIFICATIONS (maximum @ +25°C unless otherwise noted as typical)

Model	Resolution	Relative Accuracy	Differential Nonlinearity	Gain T.C. ppm/°C	Settling Time	Temp Range[1]	I/V Out	Input Logic	Package
AD563JD-BIN/BCD	12 Bits/3 Digits	±1/2LSB	±1/2LSB	50	1.5μs typ	C	I	TTL &	DIP
AD563KD(SD)(TD)-BIN/BCD	12 Bits/3 Digits	±1/4LSB	±1/2LSB	20/30/10	1.5μs typ	C/M	I	CMOS	DIP
AD565JD(SD)	12 Bits	±1/2LSB	±3/4LSB	30	400ns	C/M/M	I	TTL	DIP
AD565KD(TD)	12 Bits	±1/4LSB	±1/2LSB	20/15/15	400ns	C/M/M	I		DIP
AD565AJD(SD)	12 Bits	±1/2LSB	±3/4LSB	50/30/30	250ns	C/M/M	I	TTL	DIP
AD565AKD(TD)	12 Bits	±1/4LSB	±1/2LSB	20/15/15	250ns	C/M/M	I	TTL	DIP
AD DAC87-CBI-I	12 Bits	±1/2LSB	±3/4LSB	25	3μs	M/M	I	TTL &	DIP
AD DAC87-CBI-V	12 Bits	±1/2LSB	±3/4LSB	25	300ns	M/M	V	CMOS	DIP
AD370JN(JD)	12 Bits	±1LSB			35μs	C/C	V	TTL &	DIP
AD370KN(KD)(SD)	12 Bits	±1/2LSB	Monotonic		35μs	C/C/M/M	V	CMOS	DIP
AD371JN(JD)	12 Bits	±1LSB			35μs	C/C	V	TTL &	DIP
AD371KN(KD)(SD)	12 Bits	±1/2LSB	Monotonic		35μs	C/C/M/M	V	CMOS	DIP

NOTES
[1] C = 0 to +70°C, M = –55°C to +125°C

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HIGH PERFORMANCE DACS FEATURE SELECTION CHART

HIGH PERFORMANCE — μP COMPATIBLE — FAST — MULTI-PLYING

Feature		AD563	AD DAC87	AD370	AD371	AD DAC71/DAC72	AD7546	AD3860	AD567	AD667	AD565	AD565A	AD566	AD566A
Resolution	0.375dB Steps to 88.5dB													
	1.5dB Steps to 88.5dB													
	8 Bits													
	10 Bits													
	12 Bits	•	•	•	•			•	•	•	•	•	•	•
	16 Bits					•	•							
	18 Bits													
Output Format	Current	•	•			•			•		•	•	•	•
	Voltage		•	•	•	•	•	•		•				
Internal Reference		•	•	•	•	•		•	•	•	•	•		
Multiplication Capability	2 Quadrant						•						•	•
	4 Quadrant													
Logic Compatible with	TTL	•	•	•	•	•	•	•	•	•	•	•	•	•
	CMOS	•	•	•	•	•	•							
Input Code	Binary	•	•	•	•	•	•	•	•	•	•	•	•	•
	BCD	•	•											
Second Source		•	•	•	•	•		•			•	•	•	•
Single Power Supply														
Input Data Latch Structure	Serial													
	Parallel						•	•	•	•				
Operating Temperature Ranges[1]	C = 0 to +70°C	•	•	•	•	•	•	•	•	•	•	•	•	•
	I = −25°C to +85°C					•	•							
	M = −55°C to +125°C	•	•	•	•			•	•	•	•	•	•	•
Low Power				•	•		•	•						
Input/Output Isolation														
Dice Availability									•			•		•

NOTE
[1] C = Commercial I = Industrial M = Military

HIGH PERFORMANCE DACS FEATURE SELECTION CHART (Continued)

HIGH PERFORMANCE — MULTIPLYING — μP BUS COMPATIBLE — LOG DAC™ ATTENUATORS — SPECIAL PURPOSE — QUAD DAC

Feature		AD562	AD7541	AD7541A	AD7525	AD7542	AD7543	AD7544[1]	AD7545	AD7548	AD7115	AD7111	AD7110	AD7118	AD390
Resolution	0.1dB Steps to 19.9dB										•				
	0.375dB Steps to 88.5dB											•			
	1.5dB Steps to 88.5dB												•	•	
	8 Bits														
	10 Bits				•										
	12 Bits	•	•	•		•	•	•	•	•					•
	16 Bits														
	18 Bits														
Output Format	Current	•	•	•	•	•	•	•	•	•	•	•	•	•	
	Voltage														•
Internal Reference															•
Multiplication Capability	2 Quadrant	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	4 Quadrant		•	•	•	•	•	•	•	•					
Logic Compatible with	TTL	•	•	•		•	•	•	•	•	•	•		•	•
	CMOS	•	•	•	•	•	•	•	•	•	•	•	•	•	
Input Code	Binary	•	•	•		•	•	•	•	•		•	•	•	•
	BCD	•			•						•				
Second Source		•	•	•											
Single Power Supply											•	•		•	
Input Data Latch Structure	Serial						•								
	Parallel					•		•	•	•	•	•			•
Operating Temperature Ranges[2]	C = 0 to +70°C	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	I = −25°C to +85°C		•	•	•	•	•	•	•	•	•	•		•	
	M = −55°C to +125°C	•	•	•	•	•	•	•	•	•	•	•		•	•
Low Power			•	•	•	•	•	•	•	•	•	•	•	•	
Input/Output Isolation															
Dice Availablity			•			•	•								

NOTE
[1] Six-Stage FIFO Input Register [2] C = Commercial I = Industrial M = Military

ANALOG DEVICES

Digital-to-Analog Converters

µP BUS COMPATIBLE

SPECIFICATIONS (maximum @ +25°C unless otherwise noted as typical)

Model	Resolution	Relative Accuracy	Differential Nonlinearity	Gain T.C. ppm/°C	Settling Time	Temp Range[1]	I/V Out	Input Logic	Package
AD567J(S)	12 Bits	±1/2LSB	±3/4LSB	50/30/30	500ns	C/M/M	I	TTL &	DIP
AD567K(T)	12 Bits	±1/4LSB	±1/2LSB	20	500ns	C/M/M	I	CMOS	DIP
AD667J(S)	12 Bits	±1/2LSB	±3/4LSB	50/30	2µs[2]	C/M	V	TTL	DIP
AD667K	12 Bits	±1/2LSB	±1/2LSB	40	2µs[2]	C	V	TTL	DIP
AD3860K	12 Bits	±1/2LSB	±1LSB	±10	5µs[2]	C	V	TTL	DIP
AD3860S	12 Bits	±1/2LSB	GMOT[3]	±10	5µs[2]	M	V	TTL	DIP
AD7542JN(AD)(SD)	12 Bits	±1LSB	±0.048%	5	2µs	C/I/I/ M/M	I	CMOS	DIP
AD7542KN(BD)(TD)	12 Bits	±1/2LSB	±0.024%	5	2µs	C/I/I/ M/M	I	CMOS	DIP
AD7543JN(AD)(SD)	12 Bits	±1LSB	±0.048%	5	2µs	C/I/I/ M/M	I	CMOS	DIP
AD7543KN(BD)(TD)	12 Bits	±1/2LSB	±0.024%	5	2µs	C/I/I/ M/M	I	CMOS	DIP
AD7544JN(AD)(SD)[4]	12 Bits	±1LSB	±0.048%	5	2µs	C/I/M	I	CMOS	DIP
AD7544KN(BD)(TD)[4]	12 Bits	±1/2LSB	±0.024%	5	2µs	C/I/M	I	CMOS	DIP
AD7544GKN(GBD)(GTD)[4]	12 Bits	±1/2LSB	±0.024%	5	2µs	C/I/M	I	CMOS	DIP
AD7545J(A)(S)	12 Bits	±2LSB	±4LSB	±5[5]		C/I/M	I	TTL &	DIP
AD7545K(B)(T)	12 Bits	±1LSB	±1LSB	±5[5]		C/I/M	I	CMOS	DIP
AD7545L(C)(U)	12 Bits	±1/2LSB	±1LSB	±5[5]		C/I/M	I		DIP
AD7545GL(GC)(GU)[6]	12 Bits	±1/2LSB	±1LSB	±5[5]		C/I/M	I		DIP
AD7548J(A)(S)	12 Bits	±1LSB	±1LSB	±5[5]		C/I/M	I	TTL	DIP
AD7548(K)(B)(T)	12 Bits	±1/2LSB	±1/2LSB	±5[5]		C/I/M	I	TTL	DIP
AD7546JN(AD)	16 Bits	±0.05% FSR	±0.006% FSR	±2	10µs typ[7]	C/I	V	TTL &	DIP
AD7546KN(BD)	16 Bits	±0.012% FSR	GMOT[3]	±2	10µs typ[7]	C/I	V	CMOS	DIP
LOG DAC™ STEP ATTENUATORS									
AD7111K(B)(T)	0.375dB	30dB ± 0.17dB	GMOT[8]			C/I/M	I	CMOS	DIP
AD7111L(C)(U)	0.375dB	36dB ± 0.17dB	GMOT[9]			C/I/M	I	CMOS	DIP
AD7115K(B)(T)	0.1dB	±0.05dB	Monotonic			C/I/M	I	TTL & CMOS	DIP
QUAD DAC (FOUR DACS IN ONE PACKAGE)									
AD390JD(SD)	12 Bits	±3/4LSB	GMOT[3]	±40/±10[10]	8µs	C/M	V	TTL &	DIP
AD390KD(TD)	12 Bits	±1/2LSB	GMOT[3]	±10/±5[10]	8µs	C/M	V	CMOS	DIP

NOTES

[1] C = 0 to +70°C, I = -25°C to +85°C, M = -55°C to +125°C
[2] To 0.01% for 10-V Step
[3] Guaranteed Monotonic Over Temperature
[4] Six-Stage FIFO Input Register
[5] 5 Volt Supply
[6] 2LSB max gain error (multiplying DAC)
[7] To 0.00076% of final value
[8] 0 to -48dB at 0.375dB, 0 to -60dB at 0.75dB, 0 to -72dB at 1.5dB
[9] 0 to -54dB at 0.375dB, 0 to -72dB at 0.75dB, 0 to -88.5dB at 1.5dB
[10] Internal/External reference

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HIGH RESOLUTION
SPECIFICATIONS (maximum @ +25°C unless otherwise noted as typical)

Model	Resolution	Relative Accuracy	Differential Nonlinearity	Gain T.C. ppm/°C	Settling Time	Temp Range[1]	I/V Out	Input Logic	Package
AD7546JN(AD)	16 Bits	±0.05%	±0.006%	±2	10μs typ[2]	C/I	V	CMOS or	DIP
AD7546KN(BD)	16 Bits	±0.012%	±0.0015%	±2	10μs typ[2]	C/I	V	TTL	DIP
AD DAC71	16 Bits	±0.003%	Note 3	±15	10/1μs[4]	C	V/I	TTL	DIP[5]
AD DAC71H	16 Bits	±0.003%	Note 3	±15	10/1μs[4]	C	V/I	TTL	DIP[5]
AD DAC72C	16 Bits	±0.003%	Note 3	±15	10/1μs[4]	C	V/I	TTL	DIP[5]
AD DAC72	16 Bits	±0.003%	Note 6	±15[6]	10/1μs[4]	I	V/I	TTL	DIP[5]

NOTES
[1] C = 0 to +70°C, I = -25°C to +85°C
[2] to 0.00076% of final value
[3] Guaranteed 14-bit monotonic 0 to +50°C
[4] Voltage/current, to ±0.003% FSR
[5] AD DAC71 polymer sealed, AD DAC71H and AD DAC72 hermetic
[6] Guaranteed 14-bit monotonic 0 to +70°C, Gain tempco ±15ppm/°C, T_{min} to +25°C, ±7ppm/°C, +25°C to T_{max}

SPECIAL PURPOSE
SPECIFICATIONS (maximum @ +25°C unless otherwise noted as typical)

Model	Resolution	Relative Accuracy	Differential Nonlinearity	Gain T.C. ppm/°C	Settling Time	Temp Range[1]	I/V Out	Input Logic	Package
LOG DAC™ STEP ATTENUATORS									
AD7110KN	1.5dB	±0.7dB, 0 to -48dB	Monotonic	NA	NA	0 to +50°C	I	CMOS	DIP
AD7118KN(BD)(TD)	1.5dB	±0.75dB, 0 to -42dB	Monotonic	NA	NA	C/I/M	I	CMOS & TTL	DIP
AD7118LN(CD)(UD)	1.5dB	±0.7dB, 0 to -48dB	Monotonic	NA	NA	C/I/M	I	CMOS & TTL	DIP

These devices are digitally controlled attenuators for use in high performance audio systems and wide dynamic range applications.

NOTE
[1] C = 0 to +70°C, I = -25°C to +85°C, M = -55°C to +125°C

MULTIPLYING

Model	Resolution	Relative Accuracy	Differential Nonlinearity	Gain T.C. ppm/°C	Settling Time	Temp Range[1]	I/V Out	Input Logic	Package
AD562KD(AD)-BIN	12 Bits	±1/2LSB	±1/2LSB	3	1.5μs typ	C/I	I	TTL &	DIP
AD562SD-BIN	12 Bits	±1/4LSB	±1/2LSB	3	1.5μs typ	M	I	CMOS	DIP
AD562KD(AD)-BCD	3 Digits	±1/2LSB	±1/2LSB	3	1.5μs typ	C/I	I		DIP
AD562SD-BCD	3 Digits	±1/10LSB	±1/2LSB	3	1.5μs typ	M	I		DIP
AD566JD(SD)	12 Bits	±1/2LSB	±3/4LSB	10	400ns	C/M/M	I	TTL	DIP
AD566KD(TD)	12 Bits	±1/4LSB	±1/2LSB	3	400ns	C/M/M	I		DIP
AD566AJD(SD)	12 Bits	±1/2LSB	±3/4LSB	10	350ns	C/M/M	I	TTL	DIP
AD566AKD(TD)	12 Bits	±1/4LSB	±1/2LSB	3	350ns	C/M/M	I	TTL	DIP
AD7541JN(AD)	12 Bits	±1LSB	±2LSB	10	1μs	C/I/M/M	I	TTL &	DIP
AD7541KN(BD)	12 Bits	±1/2LSB	±1LSB	10	1μs	C/I/M/M	I	CMOS	DIP
AD7541AJN(AQ)	12 Bits	±1LSB	±1LSB	5	0.6μs typ[2]	C/I	I	TTL &	DIP
AD7541AKN(BQ)	12 Bits	±1/2LSB	±1/2LSB	5	0.6μs typ[2]	C/I	I	CMOS	DIP
AD7541ASD	12 Bits	±1LSB	±1LSB	5	0.6μs typ[2]	M/M	I		DIP
AD7541ATD	12 Bits	±1/2LSB	±1/2LSB	5	0.6μs typ[2]	M/M	I		DIP
AD7240J(A)(S)	12 Bits	+1/2, -1 1/4	±1/2LSB	6	900ns	C/I/M	V	TTL	DIP
AD7240K(B)(T)	12 Bits	+1/2, -1LSB	±1/2LSB	6	900ns	C/I/M	V	TTL	DIP
AD7525KN(BD)(TD)	3 1/2 Digits	±1LSB	±1LSB	25	1μs	C/I/M/M	I	CMOS	DIP
AD7525LN(CD)(UD)	3 1/2 Digits	±1/2 LSB	±1/2LSB	25	1μs	C/I/M/M	I		DIP

[1] C = 0 to +70°C, I = -25°C to +85°C, M = -55°C to +125°C

ANALOG DEVICES

Digital-to-Analog Converters

ULTRA FAST/VIDEO DACS FEATURE SELECTION CHART

		Current Out										
		HDG-0405	HDG-0605	HDG-0805	HDS-0820	HDS-0810E	HDD-0810	HDD-0810C	HDS-1025	HDS-1015E	HDD-1015	AD9768
Settling Time to Resolution in Bits	<550ns											
	<210ns											
	<75ns								•			
	<21ns				•	•	•	•		•	•	
	<8ns	•	•	•								•
Resolution	4 Bits	•										
	6 Bits		•									
	8 Bits			•	•	•	•	•				•
	10 Bits								•	•	•	
	11 Bits											
	12 Bits											
Application	General Purpose				•	•	•		•	•	•	•
	Lowest Glitch	•	•	•				•				
	Multiplying											•
	Composite Video	•	•	•				•				
Output Format	Current	•	•	•	•	•	•	•	•	•	•	•
	Voltage											
Binary Logic	TTL				•				•			
	ECL	•	•	•		•	•	•		•	•	•
	Latched	•	•	•			•	•			•	
Single Power Supply		•	•	•		•	•	•		•	•	
Operating Temperature Ranges	0 to +70°C	•	•	•	•	•	•	•	•	•	•	
	-25°C to +85°C						•	•			•	
	-55°C to +125°C				•	•			•	•		•

ULTRA FAST/VIDEO DACS FEATURE SELECTION CHART (Continued)

		Current Out			Voltage Out			
		HDD-1015C	HDS-1250	HDS-1240E	HDH-0802	HDH-1003	HDH-1205	HDD-1206
Settling Time to Resolution in Bits	<2µs						•	•
	<210ns				•	•		
	<75ns		•	•				
	<21ns	•						
	<8ns							
Resolution	4 Bits							
	6 Bits							
	8 Bits				•			
	10 Bits	•				•		
	11 Bits							
	12 Bits		•	•			•	•
Application	General Purpose		•	•	•	•	•	
	Lowest Glitch							•
	Multiplying							
	Composite Video	•						
Output Format	Current	•	•	•				
	Voltage				•	•	•	•
Binary Logic	TTL		•		•	•	•	•
	ECL	•		•				
	Latched	•						•
Single Power Supply		•						
Operating Temperature Ranges	0 to +70°C	•	•	•	•	•	•	•
	-25°C to +85°C	•						
	-55°C to +125°C		•	•[1]	•	•	•	•

NOTE
[1] -55°C to +100°C

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ULTRA FAST/VIDEO

SPECIFICATIONS (maximum @ +25°C unless otherwise noted as typical)

Model	Resolution	Relative Accuracy	Differential Nonlinearity	Gain T.C. ppm/°C Typical	Settling Time ns Typical	Temp Range[1]	I/V Out	Input Logic	Package
AD9768	8 Bits	±1/2LSB	GMOT[2]	80	5	M	I	ECL	DIP
HDG-0405[3,4]	4 Bits	±1/2LSB	GMOT[2]	25	4	C	I	ECL	DIP
HDG-0605[3,4]	6 Bits	±1/2LSB	GMOT[2]	25	6	C	I	ECL	DIP
HDG-0805[3,4]	8 Bits	±1/2LSB	GMOT[2]	25	8	C	I	ECL	DIP
HDS-0820(0820M)	8 Bits	±1/4LSB	GMOT[2]	30	20	C/M	I	TTL	DIP
HDS-0810E(0810EM)	8 Bits	±1/4LSB	GMOT[2]	80	10	C/M	I	ECL	DIP
HDD-0810(0810M)[4]	8 Bits	±1/4LSB	GMOT[2]	80	10	C/M	I	ECL	DIP
HDD-0810C(0810CM)[3,4]	8 Bits	±1/4LSB	GMOT[2]	80	10	C/M	I	ECL	DIP
HDS-1025(1025M)	10 Bits	±1/2LSB	GMOT[2]	30	25	C/M	I	TTL	DIP
HDS-1015E(1015EM)	10 Bits	±1/2LSB	GMOT[2]	80	15	C/M	I	ECL	DIP
HDD-1015(1015M)[4]	10 Bits	±1/2LSB	GMOT[2]	80	15	C/M	I	ECL	DIP
HDD-1015C(1015CM)[3,4]	10 Bits	±1/2LSB	GMOT[2]	80	15	C/M	I	ECL	DIP
HDS-1250(1250M)	12 Bits	±1/2LSB	GMOT[2]	30	35	C/M	I	TTL	DIP
HDS-1240E(1240EM)	12 Bits	±1/2LSB	GMOT[2]	25	35	C/MR	I	ECL	DIP
HDD-1206JW	12 Bits	±1/2LSB	GMOT[2]	40	60[5]	C	V	TTL	DIP
HDD-1206SM	12 Bits	±1/2LSB	GMOT[2]	40	60[5]	M	V	TTL	DIP
HDH-0802(0802M)	8 Bits	±1/4LSB	GMOT[2]	30	200	C/M	V	TTL	DIP
HDH-1003(1003M)	10 Bits	±1/2LSB	GMOT[2]	30	300	C/M	V	TTL	DIP
HDH-1205(1205M)	12 Bits	±1/2LSB	GMOT[2]	30	500	C/M	V	TTL	DIP

NOTES

[1] C = 0 to +70°C, I = −25°C to +85°C, M = −55°C to +125°C, MR = −55°C to +100°C
[2] Guaranteed Montonic Over Temperature
[3] Composite video
[4] Latched input
[5] 1LSB settling

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ANALOG DEVICES

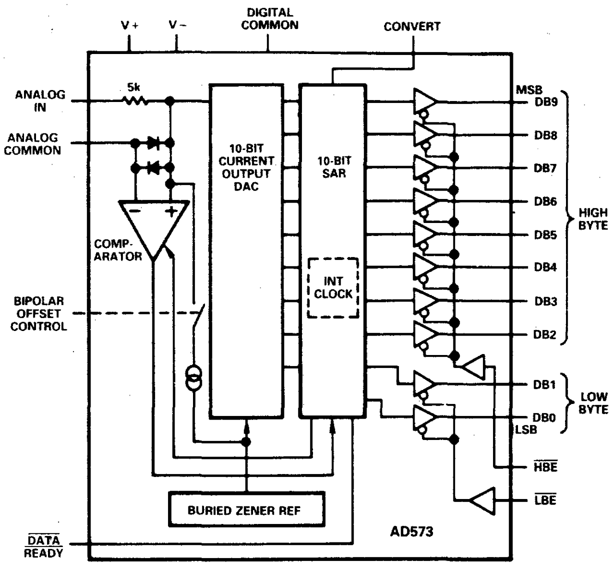
Fast, Complete 10-Bit A/D Converter with Microprocessor Interface

AD573*

FEATURES

- Complete 10-Bit A/D Converter with Reference, Clock and Comparator
- Full 8- or 16-Bit Microprocessor Bus Interface
- Fast Successive Approximation Conversion – 20μs
- No Missing Codes Over Temperature
- Operates on +5V and −12V to −15V Supplies
- Low Cost Monolithic Construction

AD573 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD573 is a complete 10-bit successive approximation analog to digital converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register (SAR) and 3 state output buffers–all fabricated on a single chip. No external components are required to perform a full accuracy 10-bit conversion in 20μs.

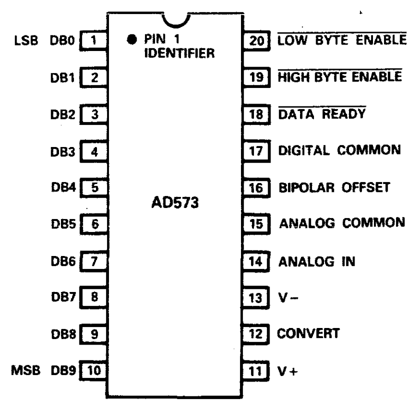
The AD573 incorporates the most advanced integrated circuit design and processing technology available today. The successive approximation function is implemented with I^2L (integrated injection logic). Laser trimming of the high stability SiCr thin film resistor ladder network at the wafer stage (LWT) insures high accuracy, which is maintained with a temperature compensated sub-surface Zener reference.

Operating on supplies of +5V and −12V to −15V, the AD573 will accept analog inputs of 0 to +10V or −5V to +5V. A positive pulse on the CONVERT line initiates the 20μs conversion cycle. $\overline{\text{DATA READY}}$ indicates completion of the conversion. $\overline{\text{HIGH BYTE ENABLE}}$ ($\overline{\text{HBE}}$) and $\overline{\text{LOW BYTE ENABLE}}$ ($\overline{\text{LBE}}$) control the 8-bit and 2-bit three state output buffers.

The AD573 is available in two versions for the 0 to +70°C temperature range, the AD573J and AD573K. The AD573S guarantees 10-bit relative accuracy and no missing codes from −55°C to +125°C.

Two package configurations are offered. The AD573J and AD573K are also available in a 20-pin plastic DIP. All versions are offered in a 20-pin hermetically sealed ceramic DIP.

AD573 PINOUT



AD573 ORDERING GUIDE

Model	Package Option	Temperature Range	Relative Accuracy
AD573JN	20-Pin Plastic DIP	0 to +70°C	±1LSB max
AD573KN	20-Pin Plastic DIP	0 to +70°C	±1/2LSB max
AD573JD	20-Pin Ceramic DIP	0 to +70°C	±1LSB max
AD573KD	20-Pin Ceramic DIP	0 to +70°C	±1/2LSB max
AD573SD	20-Pin Ceramic DIP	−55°C to +125°C	±1LSB max

*Protected by U.S. Patent Nos. 3,940,760; 4,213,806 and 4,136,349

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ANALOG DEVICES

Fast, Complete 12-Bit A/D Converter with Microprocessor Interface

AD574A

FEATURES

- Complete 12-Bit A/D Converter with Reference and Clock
- Full 8- or 16-Bit Microprocessor Bus Interface
- 250ns Bus Access Time
- Guaranteed Linearity Over Temperature
  - 0 to +70°C – AD574AJ, AK, AL
  - −55°C to +125°C – AD574AS, AT, AU
- No Missing Codes Over Temperature
- Fast Successive Approximation Conversion – 25μs
- Buried Zener Reference for Long-Term Stability and Low Gain T.C. 10ppm/°C max AD574AL
  12.5ppm/°C max AD574AU
- Low Profile 28-Pin Ceramic DIP
- Low Power: 390mW
- Low Cost

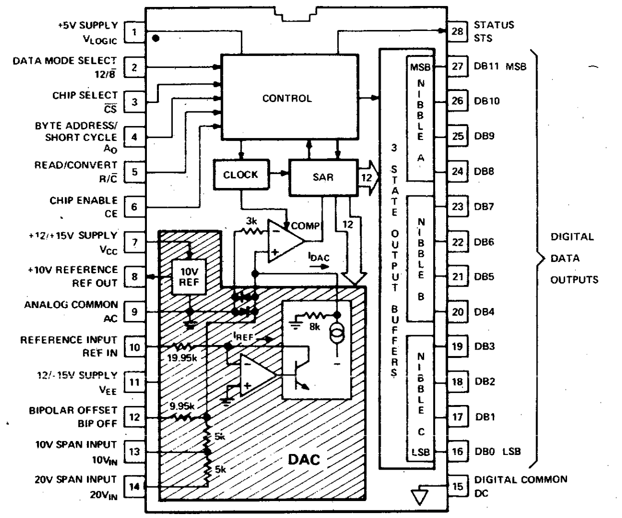
PRODUCT DESCRIPTION

The AD574A is a complete 12-bit successive-approximation analog-to-digital converter with 3-state output buffer circuitry for direct interface to an 8-, 12-or 16-bit microprocessor bus. The AD574A design is implemented with two LSI chips each containing both analog and digital circuitry, resulting in the maximum performance and flexibility at the lowest cost.

One chip is the high performance AD565A 12-bit DAC and voltage reference. It contains the high speed current output switching circuitry, laser-trimmed thin film resistor network, low T.C. buried zener reference and the precision input scaling and bipolar offset resistors. This chip is laser-trimmed at the wafer stage (LWT) to adjust ladder network linearity, voltage reference tolerance and temperature coefficient, and the calibration accuracy of input scaling and bipolar offset resistors.

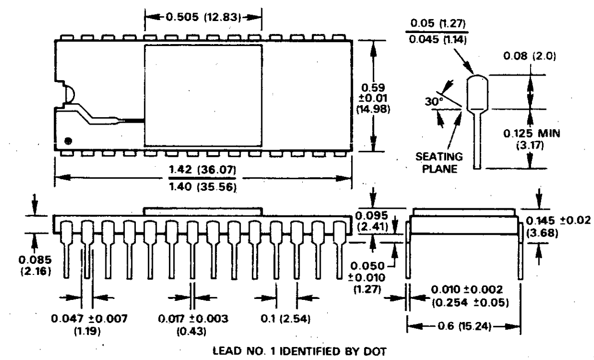
The second chip uses the proven LCI (linear-compatible integrated injection logic) process to provide the low-power I^2L successive-approximation register, converter control circuitry, clock, bus interface, and the high performance latching comparator. The precision, low-drift comparator is adjusted for initial input offset error at the wafer stage by the "zener-zap" technique which trims the comparator input stage to 1/10 LSB typical error. This form of trimming, while cumbersome for complex ladder networks, is an attractive alternative to thin film resistor trimming for a simple offset adjustment and eliminates the need for thin film processing for this portion of the circuitry.

AD574A FUNCTIONAL BLOCK DIAGRAM AND PINOUT



AD574A PACKAGE OUTLINE

Dimensions shown in inches and (mm).



The AD574A is available in six different grades. The AD574AJ, AK, and AL grades are specified for operation over the 0 to +70°C temperature range. The AD574AS, AT, and AU are specified for the −55°C to +125°C range. All grades are packaged in a low-profile, 0.600 inch wide, 28-pin hermetically-sealed ceramic DIP.

AD574A ORDERING GUIDE

Model	Temp. Range	Linearity Error Max (T_{min} to T_{max})	Resolution No Missing Codes (T_{min} to T_{max})	Max Full Scale T.C. (ppm/°C)
AD574AJD	0 to +70°C	±1LSB	11 Bits	50.0
AD574AKD	0 to +70°C	±1/2LSB	12 Bits	27.0
AD574ALD	0 to +70°C	±1/2LSB	12 Bits	10.0
AD574ASD	−55°C to +125°C	±1LSB	11 Bits	50.0
AD574ATD	−55°C to +125°C	±1LSB	12 Bits	25.0
AD574AUD	−55°C to +125°C	±1LSB	12 Bits	12.5

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ANALOG DEVICES

CMOS µP Compatible 10-Bit Plus Sign ADC

AD7571

FEATURES

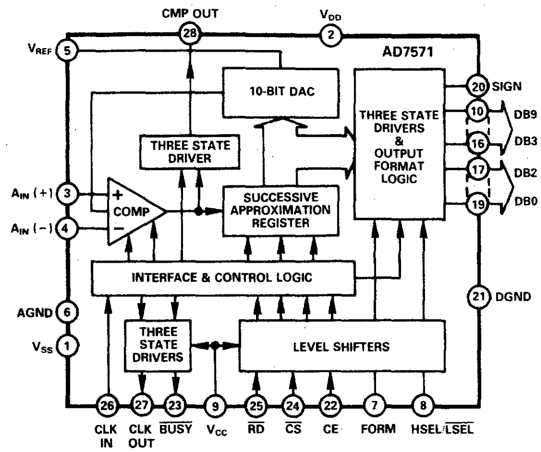
- 10-Bit Plus Sign Resolution
- No Missed Codes Over Full Temperature Range
- Conversion Time 80µs
- Differential Analog Voltage Inputs, ±10V Range
- Serial and Parallel Data Outputs
- Easy Interface to Most Microprocessors
- Internal Clock Oscillator
- Single Supply Operation for Positive-Only Signals
- Monolithic Construction

GENERAL DESCRIPTION

The AD7571 is a high speed, low cost 10-bit plus sign CMOS A/D converter which uses the successive approximation technique to provide a conversion time of 80µs. The device is designed for easy microprocessor interface allowing full parallel or double byte reading over three-state outputs. Conversion results are also available in serial form allowing opto-isolated operation using as few as two wires for the interconnect.

A new differential analog input configuration is used in the AD7571, increasing the common-mode rejection performance and allowing the analog zero input voltage to be offset from true analog ground. Analog input voltage range is ±10V using a single positive reference. With positive-only input signals the AD7571 can be operated from a single positive power supply.

AD7571 FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

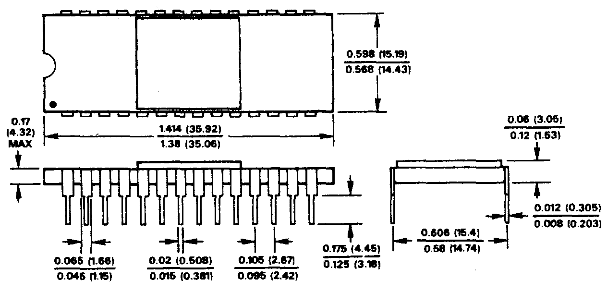
Relative Accuracy (T_{min} to T_{max})	Temperature Range and Package: Plastic 0 to +70°C	Cerdip[1] −25°C to +85°C	Side-Brazed Ceramic −55°C to +125°C
±1LSB	AD7571JN	AD7571AQ	AD7571SD
±1/2LSB	AD7571KN	AD7571BQ	AD7571TD

NOTE
[1]Analog Devices reserves the right to ship ceramic packages in lieu of cerdip packages.

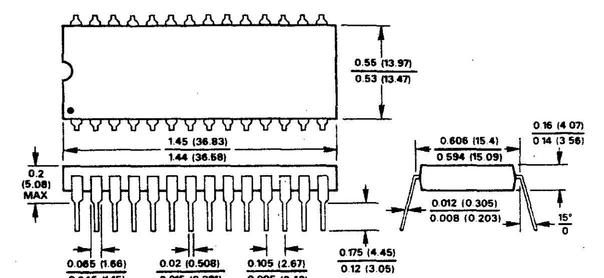
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

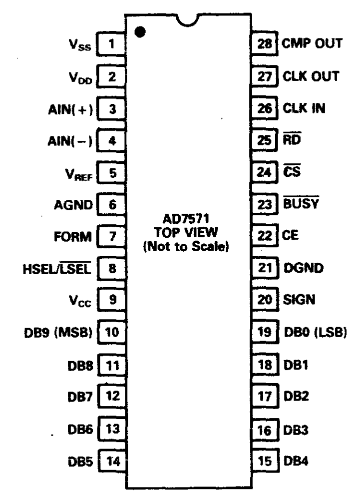
28-PIN CERAMIC DIP (SUFFIX D)



28-PIN PLASTIC DIP (SUFFIX N)



PIN CONFIGURATION



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ANALOG DEVICES

CMOS μP Compatible 10-Bit ADC

AD7573

INTERFACE

Analog Devices

FEATURES

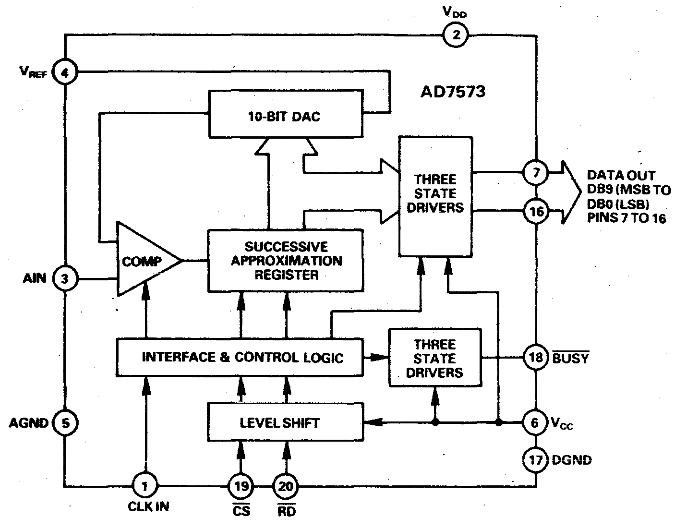
- 10-Bit Resolution
- No Missing Codes Over Full Temperature Range
- Conversion Time 80μs
- 0V to +10.24V Analog Input Voltage Range with Reference Voltage of +5.12V
- 10-Bit Parallel Data Output
- Easy Interface to Most Microprocessors
- Internal Clock Oscillator
- Single Supply Operation
- Monolithic

GENERAL DESCRIPTION

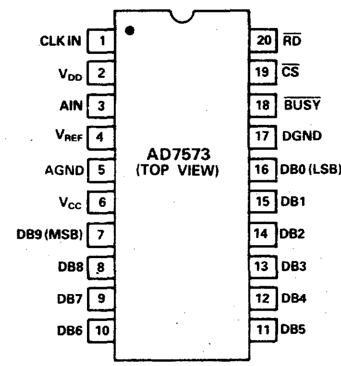
The AD7573 is a high speed, low cost 10-bit CMOS A/D converter which uses the successive approximation technique to provide a conversion time of 80μs. The device is designed for easy microprocessor interface using two standard control signals; $\overline{CS}$ (decoded device address) and $\overline{RD}$ ($\overline{READ}$/WRITE control), for conversion start and data read operations. Conversion results are available via a 10-bit wide three-state output bus.

The analog input voltage range is from 0V to +10.24V when using a reference voltage of +5.12V. Single +15V power supply operation is possible with all logic inputs and outputs being CMOS compatible. Using +5V/+15V supplies allows control inputs and data outputs to be TTL/CMOS compatible. The device is packaged in a small 20-pin 0.3" wide DIP.

AD7573 FUNCTIONAL BLOCK DIAGRAM



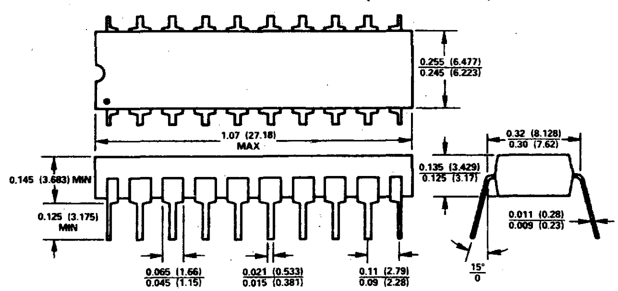
PIN CONFIGURATION



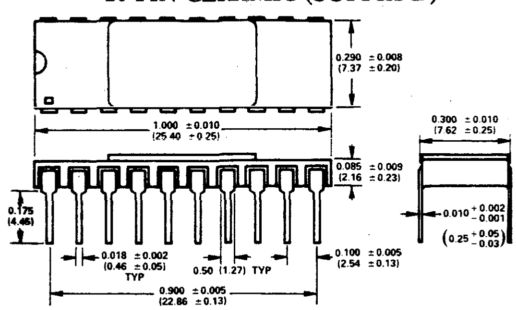
MECHANICAL INFORMATION OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

20-PIN PLASTIC DIP (SUFFIX N)



20-PIN CERAMIC (SUFFIX D)



ORDERING INFORMATION

Relative Accuracy (T_{min} to T_{max})	Temperature Range and Package: Plastic 0 to +70°C	Cerdip[1] −25°C to +85°C	Side-Brazed Ceramic −55°C to +125°C
±1LSB	AD7573JN	AD7573AQ	AD7573SD
±1/2LSB	AD7573KN	AD7573BQ	AD7573TD

NOTE:
[1]Analog Devices reserves the right to ship ceramic packages in lieu of cerdip packages.

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ANALOG DEVICES

Complete, High Resolution 16-Bit A/D Converter

AD ADC71/AD ADC72

FEATURES

Complete 16-Bit Converter With Reference and Clock
±0.003% Maximum Nonlinearity
No Missing Codes to 14 Bits Over Full Temp Range
Fast Conversion – 35μs (14 Bit)
Short Cycle Capability
Parallel or Serial Logic Outputs
Low Power: 850mW Typical
Industry Standard Pin Out

PRODUCT DESCRIPTION

The AD ADC71 and AD ADC72 are high resolution 16-bit hybrid IC analog to digital converters including reference, clock, and laser-trimmed thin-film components. The package is a compact 32-pin bottom-brazed ceramic (AD ADC71) or hermetic ceramic (AD ADC72) DIP. The thin-film scaling resistors allow analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V, and 0 to +20V.

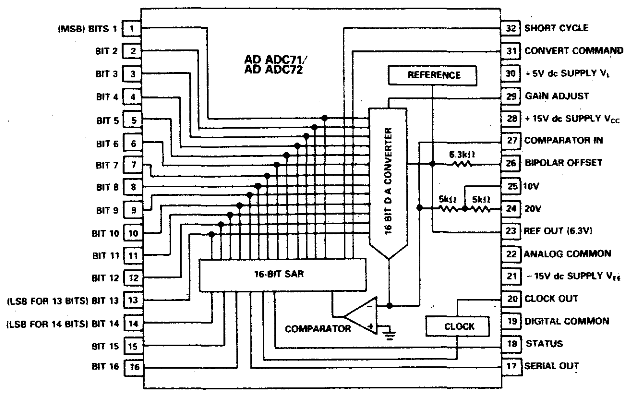
Important performance characteristics of the devices are maximum linearity error of ±0.003% of FSR (AD ADC71K, AD ADC72K and B), and maximum conversion time of 50μs. This performance is due to innovative design and the use of proprietary monolithic D/A converter chips. Laser-trimmed thin-film resistors provide the linearity and wide temperature range for no missing codes.

The AD ADC71 and AD ADC72 provide data in both parallel and serial form with corresponding clock and status output. All digital inputs and outputs are TTL compatible.

PRODUCT HIGHLIGHTS

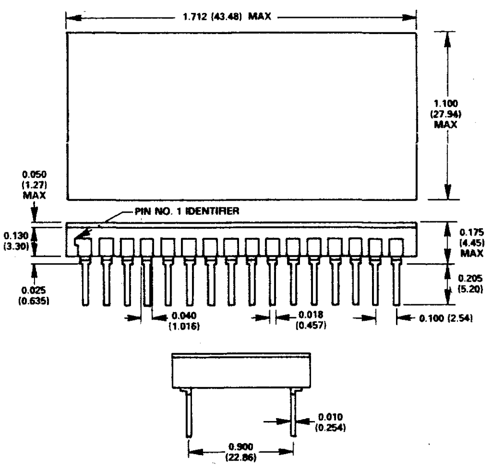
1. The AD ADC71 and AD ADC72 provide 16-bit resolution with maximum linearity error less than ±0.003% (±0.006% for J and A grades) at 25°C.
2. Conversion time is 45μs typical to 14 bits with short cycle capability.
3. The AD ADC72 (KD, BD) have no missing codes (to 14 bits) over the full specification temperature range.
4. Two binary codes are available on the AD ADC71 and AD ADC72 output. They are complementary straight binary (CSB) for unipolar input voltage ranges and complementary offset binary (COB) for bipolar input ranges. Complementary two's complement (CTC) coding may be obtained by inverting pin 1 (MSB).
5. The proprietary chips used in this hybrid design provide excellent stability over temperature and lower chip count for improved reliability.

AD ADC71/AD ADC72 FUNCTIONAL BLOCK DIAGRAM



OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



ORDERING GUIDE

Model	Linearity Error (Max)	Specification Temp Range	Package
AD ADC71JW	±0.006% of FSR	0 to +70°C	Ceramic
AD ADC71KW	±0.003% of FSR	0 to +70°C	Ceramic
AD ADC72JD	±0.006% of FSR	0 to +70°C	Hermetic
AD ADC72KD	±0.003% of FSR	0 to +70°C	Hermetic
AD ADC72AD	±0.006% of FSR	−25°C to +85°C	Hermetic
AD ADC72BD	±0.003% of FSR	−25°C to +85°C	Hermetic

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ANALOG DEVICES

14-Bit, 125kHz Analog-to-Digital Converter

HAS-1409

FEATURES
14-Bit Resolution
125kHz Word Rates
Internal Track-and-Hold
40-Pin DIP

APPLICATIONS
FDM/TDM Transmultiplexers
CAT/NMR Scanners
PCM Systems
Digital Audio

GENERAL DESCRIPTION

The HAS-1409KM and HAS-1409AKM hybrid A/D converters offer designers performance characteristics which have never before been available.

Now, for the first time, high resolution and high speed come together in a hybrid package which includes an internal track-and-hold. The HAS-1409 units have resolutions of 14 bits, are capable of word rates up to 125kHz, and are complete with track-and-hold; all of these features are housed in a single 40-pin DIP package which dissipates only two watts.

The HAS-1409KM includes an internal clock, which allows the converter to be operated at any word rate from dc through 120kHz; the HAS-1409AKM is designed for applications which use an external system clock whose frequency establishes the user's optimum word rate, up to 125kHz.

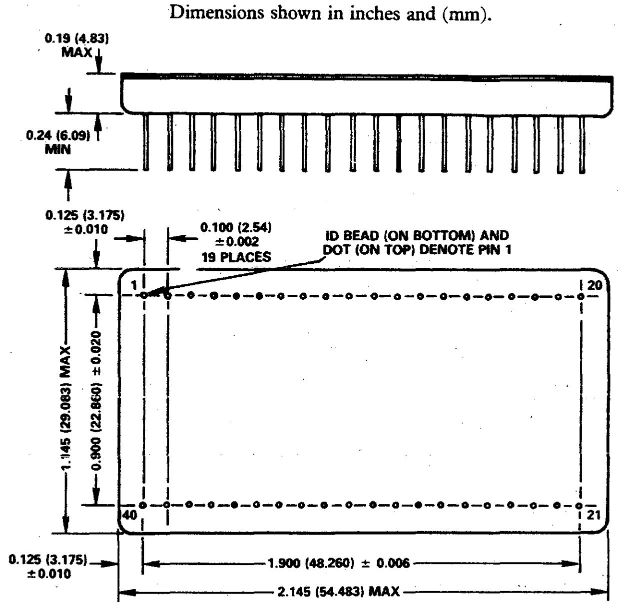
The HAS-1409 A/D has been characterized with a companion D/A converter, the HDD-1409KM, to emphasize the superior ac performance needed for use in Frequency Division Multiplex/Time Division Multiplex (FDM/TDM) transmultiplexer systems. Although specifically designed for these kinds of applications, it can also be used for other digital signal processing such as Computer Aided Tomography (CAT) and Nuclear Magnetic Resonance (NMR) scanners, and Pulse Code Modulation (PCM).

Conventional data converters often display errors at midscale which make them inadequate for use in the types of systems cited above. The unique Digitally Corrected Subranging technique pioneered by Analog Devices, used with other proprietary techniques, virtually cancels midscale errors in the HAS-1409, thereby eliminating a major source of system errors.

The logic outputs are TTL-compatible and are presented as 14 bits of parallel data. Buffer output registers and a 3-state format provide dual advantages of good drive and bus compatibility.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



HAS-1409 PIN DESIGNATION

PIN	FUNCTION	PIN	FUNCTION
1	±10V INPUT	21	DIGITAL GROUND
2	±5V INPUT	22	$\overline{\text{BIT 1}}$ (MSB)
3	ANALOG GROUND	23	BIT 1 (MSB)
4	DIGITAL GROUND	24	BIT 2
5	+5V	25	BIT 3
6	+5V	26	BIT 4
7	N/C	27	BIT 5
8	N/C	28	BIT 6
9	+5V	29	$\overline{\text{ENABLE HIGH}}$ (MSBs)
10	DIGITAL GROUND	30	CLOCK/ENCODE
11	$\overline{\text{ENABLE LOW}}$ (LSBs)	31	$\overline{\text{ENCODE}}$
12	BIT 14 (LSB)	32	+5V
13	BIT 13	33	DIGITAL GROUND
14	BIT 12	34	−15V
15	BIT 11	35	+15V
16	BIT 10	36	DIGITAL GROUND
17	BIT 9	37	ANALOG GROUND
18	BIT 8	38	ANALOG GROUND
19	BIT 7	39	+5V
20	DIGITAL GROUND	40	ANALOG GROUND

PIN 30 USED FOR CLOCK INPUT ON HAS-1409AKM; USED FOR ENCODE INPUT ON HAS-1409KM.
ALL +5V PINS ARE CONNECTED TOGETHER INTERNALLY (5, 6, 9, 32, 39). MUST ALSO BE CONNECTED TOGETHER EXTERNALLY CLOSE TO CASE.
ALL ANALOG GROUND PINS ARE CONNECTED TOGETHER INTERNALLY (3, 37, 38, 40).
ALL DIGITAL GROUND PINS ARE CONNECTED TOGETHER INTERNALLY (4, 10, 20, 21, 33, 36).
FOR BEST PERFORMANCE, ANALOG GROUND AND DIGITAL GROUND PINS MUST ALL BE CONNECTED TOGETHER AND TO GROUND EXTERNALLY AS CLOSE TO THE CASE AS POSSIBLE.

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ANALOG DEVICES

Analog-to-Digital Converters

HIGH PERFORMANCE/HIGH RESOLUTION FEATURE SELECTION CHART

		GENERAL PURPOSE				μP BUS COMPATIBLE				MULTI CHAN	HIGH PERFORMANCE				μP BUS COMPATIBLE			HIGH RESOLUTION	
		AD570	AD571	AD7573	AD ADC80	AD673	AD573	AD7571	AD7574	AD7581	AD5200	AD5210	AD572	AD574/AD574A	AD7550	AD7552	AD7555	AD ADC71	AD ADC72
Resolution	8 Bits	•				•			•	•									
	10 Bits		•	•			•												
	10 Bits & Sign							•											
	12 Bits				•						•	•	•	•					
	13 Bits														•	•			
	14 Bits																		
	16 Bits																	•	•
	4 1/2 Digits																•		
	5 1/2 Digits																•		
Conversion Time	1800ms																•		
	50ms														•	•			
	100μs			•				•[1]		•[2]									
	50μs										•							•	•
	25μs	•	•		•	•	•						•	•					
	15μs								•			•							
Internal Reference		•	•		•	•	•				•	•	•	•				•	•
Ratiometric Capability				•				•	•	•	•	•			•	•	•		
Low Power								•	•	•					•	•	•		
Second Source					•						•	•		•				•	•
Logic Compatibility	TTL	•	•	•	•	•	•	•		•	•	•	•	•	•	•		•	•
	CMOS		•	•				•	•	•					•	•	•		
Operating Temperature Ranges	C = 0 to +70°C	•	•	•		•	•	•	•	•				•			•	•	•
	I = -25°C to +85°C				•			•	•	•	•	•	•		•	•	•		•
	M = -55°C to +125°C	•	•	•		•	•	•	•		•	•	•	•					
Dice Availability		•	•				•		•						•				

NOTES
[1] 80μs conversion time
[2] 66.6μs/channel

GENERAL PURPOSE SPECIFICATIONS (maximum @ +25°C unless otherwise noted)

Model	Resolution	Relative Accuracy	Differential Nonlinearity	Gain T.C. ppm/°C	Conversion Time	Logic	Temp Range[1]	Package
AD570JD	8 Bits	±1/2LSB	Note 2	176	40μs	TTL	C	DIP
AD570SD	8 Bits	±1/2LSB	Note 2	80	40μs	TTL	M	DIP
AD571JD(SD)	10 Bits	±1/2LSB	Note 3	88/50/50	40μs	TTL &	C/M/M	DIP
AD571KD	10 Bits	±1/2LSB	Note 2	44	40μs	CMOS	C	DIP
AD ADC80-10(Z)	10 Bits	±1/2LSB	±1/2LSB	30	21μs	TTL	I	DIP
AD ADC80-12(Z)	12 Bits	±1/2LSB	±1/2LSB	30	25μs	TTL	I	DIP
μP COMPATIBLE								
AD673J	8 Bits	±1/2LSB	Note 2	2[4]	30μs	TTL	C	DIP
AD673S	8 Bits	±1/2LSB	Note 2	2[4]	30μs	TTL	M	DIP
AD7574JN(AD)(SD)	8 Bits	±3/4LSB	±7/8LSB	Note 5	15μs	CMOS	C/I/M/M	DIP
AD7574KN(BD)(TD)	8 Bits	±1/2LSB	±3/4LSB	Note 5	15μs	CMOS	C/I/M/M	DIP
AD573J	10 Bits	±1LSB	Note 6	4[4]	20μs	TTL	C	DIP
AD573K	10 Bits	±1/2LSB	Note 2	2[4]	20μs	TTL	C	DIP
AD573S	10 Bits	±1LSB	Note 2	5[4]	20μs	TTL	M	DIP
AD7571JN	10 Bits & Sign	±1LSB	Note 2	5[4]	80μs	TTL &	C	DIP
AD7571KN	10 Bits & Sign	±1/2LSB	Note 2	4[4]	80μs	CMOS	C	DIP
AD7571AQ	10 Bits & Sign	±1LSB	Note 2	5[4]	80μs	TTL &	I	DIP
AD7571BQ	10 Bits & Sign	±1/2LSB	Note 2	4[4]	80μs	CMOS	I	DIP
AD7571SD	10 Bits & Sign	±1LSB	Note 2	5[4]	80μs	TTL &	M	DIP
AD7571TD	10 Bits & Sign	±1/2LSB	Note 2	4[4]	80μs	CMOS	M	DIP
AD574AJD	12 Bits	±1LSB	Note 7	9[4]	35μs	TTL	C	DIP
AD574AKD	12 Bits	±1/2LSB	Note 2	5[4]	35μs	TTL	C	DIP
AD574ALD	12 Bits	±1/2LSB	Note 2	2[4]	35μs	TTL	C	DIP
AD574ASD	12 Bits	±1LSB	Note 7	20[4]	35μs	TTL	M	DIP
AD574ATD	12 Bits	±1/2LSB	Note 2	10[4]	35μs	TTL	M	DIP
AD574AUD	12 Bits	±1/2LSB	Note 2	5[4]	35μs	TTL	M	DIP
AD7552	12 Bits & Sign	1 Count	Note 2	1[4]	160[8]	TTL & CMOS	C	DIP
MULTI-CHANNEL								
AD7581JN(AD)[9]	8 Bits	±1 7/8LSB	±1 7/8LSB	Note 5	66.6μs[10]	TTL &	C/I	DIP
AD7581KN(BD)[9]	8 Bits	±3/4LSB	±7/8LSB	Note 5	66.6μs[10]	CMOS	C/I	DIP
AD7581LN(CD)[9]	8 Bits	±1/2LSB	±3/4LSB	Note 5	66.6μs[10]		C/I	DIP
HIGH PERFORMANCE								
AD5200BD Series	12 Bits	±1/2LSB	Note 2	Note 11	50μs	TTL	I	DIP
AD5200TD Series	12 Bits	±1/2LSB	Note 2	Note 11	50μs	TTL	M	DIP
AD574JD(SD)	12 Bits	±1/2LSB	±1LSB	50	35μs	TTL	C/M/M	DIP
AD574KD(LD)	12 Bits	±1/2LSB	Note 2	27/10	35μs	TTL	C	DIP
AD574TD(UD)	12 Bits	±1/2LSB	Note 2	25/12.5	35μs	TTL	M	DIP
AD572AD(BD)	12 Bit	±1/2LSB	±1/2LSB	30/15	25μs	TTL	I	DIP
AD572SD	12 Bits	±1/2LSB	±1/2LSB	15	25μs	TTL	M	DIP
AD5211B, AD5212B	12 Bits	±1/2LSB	Note 2	0.4%[12]	13μs	TTL	I	DIP
AD5211T, AD5212T	12 Bits	±1/2LSB	Note 2	0.4%[12]	13μs	TTL	M	DIP
AD5214B, AD5215B	12 Bits	±1/2LSB	Note 2	0.1%[12]	13μs	TTL	I	DIP
AD5214T, AD5215T	12 Bits	±1/2LSB	Note 2	0.1%[12]	13μs	TTL	M	DIP

NOTES
[1] C = 0 to +70°C, I = -25°C to +85°C, M = -55°C to +125°C
[2] No missing codes over temperature
[3] No missing codes
[4] Gain error in LSB, T_{min} to T_{max}, max
[5] ±2LSB max gain change from +25°C to T_{min} or T_{max}
[6] No missing codes over temperature, 9-bit resolution
[7] No missing codes over temperature, 11-bit resolution
[8] Milliseconds, typical
[9] 8 channels
[10] Per channel
[11] Absolute Accuracy = ±0.2%/0.1% of full scale input voltage over temperature range
[12] Absolute accuracy error, T_{min} to T_{max}, max

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Analog-to-Digital Converters

HIGH RESOLUTION SPECIFICATIONS (maximum @ +25°C unless otherwise noted)

Model	Resolution	Relative Accuracy	Differential Nonlinearity	Gain T.C. ppm/°C	Conversion Time	Logic	Temp Range[1]	Package
AD7550BD	13 Bits	±1LSB		1	40ms typ	TTL & CMOS	I	DIP
AD7555KN(BD)	5 1/2 Digits	±10 Counts	Note 2	0.2	1760ms	CMOS	C/I	DIP
	4 1/2 Digits	±1 Count	Note 3	0.2	610ms	CMOS		
AD ADC71JW	16 Bits	±0.006[5]	Note 6	15	50µs	DTL & TTL	C	DIP
AD ADC71KW	16 Bits	±0.003[5]	Note 7	15	50µs	DTL & TTL	C	DIP
AD ADC72JD(AD)	16 Bits	±0.006[5]	Note 6	20(15)	50µs	DTL & TTL	C(I)	DIP
AD ADC72KD(BD)	16 Bits	±0.003[5]	Note 7	20(15)	50µs	DTL & TTL	C(I)	DIP

NOTES
[1] C = 0 to +70°C; I = -25°C to +85°C
[2] Count uncertainty due to noise: ±2 counts
[3] Count uncertainty due to noise: ±1/2 count
[4] No missing codes
[5] % of FSR
[6] No missing codes (to 13 bits) over temperature (0 to +50°C - JW; 0 to +70°C - JD; -25°C to +85°C - AD)
[7] No missing codes (to 14 bits) over temperature (+10°C to +40°C - KW; 0 to +70°C - KD; -25°C to +85°C - BD)

HIGH SPEED/VIDEO FEATURE SELECTION CHART

		HIGH SPEED											
		AD579	AD578	AD ADC84/85[1]	AD5240[1]	HAS-0802	HAS-1002	HAS-1202	MAH-0801	MAH-1001	MAS-1202	AD6020	AD5010
Resolution	6 Bits											●	●
	8 Bits					●			●				
	9 Bits									●			
	10 Bits	●		●			●				●		
	12 Bits		●	●	●			●	●	●	●		
Conversion Time	≤8µs		●	●	●								
	≤3µs	●	●			●	●	●			●		
	≤1.1µs								●	●			
Word Rate	≥5MHz												
	≥16MHz												
	≥50MHz											●	
	≥100MHz												●
Internal Reference		●	●	●	●	●	●	●	●	●	●		
Logic Compatibility	TTL	●	●	●	●	●	●	●	●	●	●		
	ECL											●	●
Operating Temperature Ranges	C = 0 to +70°C	●	●	●	●	●	●	●	●	●	●	●	●
	I = -25°C to +85°C			●		●	●	●					
	M = -55°C to +125°C	●	●	●	●								

NOTES
[1] Second Source
[2] Complete with Track and Hold.

HIGH SPEED SPECIFICATIONS (maximum @ +25°C unless otherwise noted)

Model	Resolution	Relative Accuracy	Differential Nonlinearity	Gain T.C. ppm/°C	Conversion Time, min	Logic	Temp Range[1]	Package
AD578JN(JD)	12 Bits	±1/2LSB	Note 2	30	6µs	TTL	C	DIP
AD578KN(KD)	12 Bits	±1/2LSB	Note 2	30	4.5µs	TTL	C	DIP
AD578LN(LD)	12 Bits	±1/2LSB	Note 2	30	3µs	TTL	C	DIP
AD578SD(SD/883B)	12 Bits	±1/2LSB	Note 2	50	6µs	TTL	M	DIP
AD578TD(TD/883B)	12 Bits	±1/2LSB	Note 2	30	4.5µs	TTL	M	DIP
AD5240KD	12 Bits	±1/2LSB	Note 2	30	5	TTL	C	DIP
AD5240SD	12 Bits	±1/2LSB	Note 2	25	5	TTL	M	DIP
AD ADC84-10(84-12)	10/12 Bits	±1/2LSB	Note 2	30/30	6/10	TTL	C	DIP
AD ADC85C-10(85C-12)	10/12 Bits	±1/2LSB	Notes 2 & 3	40/25	6/10	TTL	C	DIP
AD ADC85-10(85-12)	10/12 Bits	±1/2LSB	Notes 2 & 3	20/15	6/10	TTL	I	DIP
AD ADC85S-10(85S-12)	10/12 Bits	±1/2LSB	Note 2	25	8/10	TTL	M	DIP
AD579JN	10 Bits	±1/2LSB	Note 2	30	2.2	TTL	C	DIP
AD579KN	10 Bits	±1/2LSB	Note 2	30	1.8	TTL	C	DIP
AD579BD	10 Bits	±1/2LSB	Note 2	30	1.8	TTL	I	DIP
AD579TD	10 Bits	±1/2LSB	Note 2	30	1.8	TTL	M	DIP
HAS-0802	8 Bits	±1/4LSB	Note 2	30 typ	1.2µs typ	TTL	C[4]	DIP
HAS-1002	10 Bits	±1/2LSB	Note 2	30 typ	1.4µs typ	TTL	C[4]	DIP
HAS-1202	12 Bits	±1/2LSB	Note 2	30 typ	2.2µs typ	TTL	C[4]	DIP

NOTES
[1] C = 0 to +70°C, I = -25°C to +85°C, M = -55°C to +125°C
[2] No missing codes over temperature
[3] No missing codes
[4] Extended temperature ranges available

IC ADC FLASH ENCODERS SPECIFICATIONS (typical @ +25°C unless otherwise noted)

Model	Resolution	Relative Accuracy %	Aperture Uncertainty ps max	Word Rate	Output Code	Temperature Range °C	Size & Package Inches	Input Voltage Volts	Input Impedance
AD6020KD	6 Bits	±1/8LSB	20	dc to 50MHz	BIN	0 to +70	16-Pin DIP	±2.5 max	25pF[1]
AD5010KD	6 Bits	±1/8LSB	20	dc to 100MHz	BIN	0 to +70	16-Pin DIP	±2.5 max	25pF[1]

NOTE
[1] Input Capacitance

ANALOG DEVICES

Voltage-to-Frequency and Frequency-to-Voltage Converter

AD650

FEATURES
V/F Conversion to 1MHz
Reliable Monolithic Construction
Very Low Nonlinearity
- **0.002% typ at 10kHz**
- **0.005% typ at 100kHz**
- **0.07% typ at 1MHz**

Input Offset Trimmable to Zero
CMOS or TTL Compatible
Unipolar, Bipolar, or Differential V/F
V/F or F/V Conversion

PRODUCT DESCRIPTION
The AD650 V/F/V (voltage-to-frequency or frequency-to-voltage converter) provides a combination of high frequency operation and low nonlinearity previously unavailable in monolithic form. The inherent monotonicity of the V/F transfer function makes the AD650 useful as a high-resolution analog-to-digital converter. A flexible input configuration allows a wide variety of input voltage and current formats to be used, and an open-collector output with separate digital ground allows simple interfacing to either standard logic families or opto-couplers.

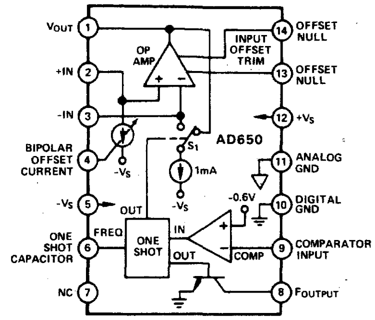
The linearity error of the AD650 is typically 20ppm (0.002% of full scale) and 50ppm (0.005%) maximum at 10kHz full scale. This corresponds to approximately 14-bit linearity in an analog-to-digital converter circuit. Higher full-scale frequencies or longer count intervals can be used for higher resolution conversions. The AD650 has a useful dynamic range of six decades, allowing extremely high resolution measurements. Even at 1MHz full scale, linearity is guaranteed less than 1000ppm (0.1%) on the AD650KN, BD and SD grades.

In addition to analog-to-digital conversion, the AD650 can be used in isolated analog signal transmission applications, phased-locked-loop circuits, and precision stepper motor speed controllers. In the F/V mode, the AD650 can be used in precision tachometer and FM demodulator circuits.

The input signal range and full-scale output frequency are user-programmable with two external capacitors and one resistor. Input offset voltage can be trimmed to zero with an external potentiometer.

The AD650JN and AD650KN are offered in a plastic 14-pin DIP package and are specified for the commerical (0 to +70°C) temperature range. For industrial temperature range (−25°C to +85°C) applications, the AD650AD and AD650BD are offered in a ceramic package. The AD650SD is specified for the full −55°C to +125°C extended temperature range.

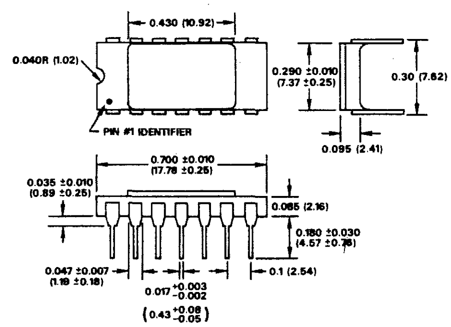
AD650 FUNCTIONAL BLOCK DIAGRAM



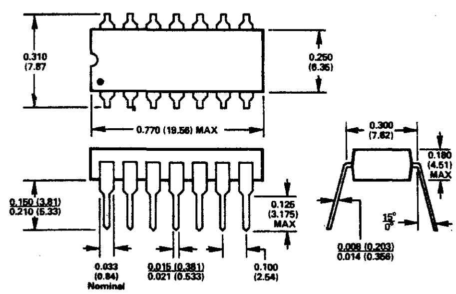
ORDERING GUIDE

Part Number	Gain Tempco ppm/°C 100kHz	1MHz Linearity	Specified Temperature Range °C	Package
AD650JN	150 typ	0.1% typ	0 to +70	Plastic DIP
AD650KN	150 typ	0.1% max	0 to +70	Plastic DIP
AD650AD	150 max	0.1% typ	−25 to +85	Ceramic
AD650BD	150 max	0.1% max	−25 to +85	Ceramic
AD650SD	150 max	0.1% max	−55 to +125	Ceramic

OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).



"D" PACKAGE (TO-116) CERAMIC DIP



"N" PACKAGE PLASTIC DIP

ANALOG DEVICES

V/F CONVERTERS

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise noted)

Model	High Performance 500kHz ADVFC32K(B)(S)	Wide Band 1MHz AD650J(K)(S)	Economy/Versatile 0 to 150kHz AD537JH(KH)(SH)(JD)(KD)(SD)
Analog Input			
Voltage Signal Range - V min	0 to -10V	0 to -10V	$-V_S$ to ($+V_S$ -4V) min
Current Signal Range - mA min	0 to +0.25	0 to +0.25	0.1μA to 1000μA
Overrange - % min	–	–	100
Accuracy			
Nonlinearity, max - at rate F.S. range			@ F = 10kHz
Voltage Input - %	±0.2	±0.5(±0.1)(±0.2)	
Current Input - %	±0.2	±0.5(±0.1)(±0.2)	0.15(0.07)(0.07)(0.15)(0.07)(0.07)
Gain vs. temperature, ppm/°C, max	150(100)(150)	150(100)(150)	±150(±50)(±150)(±150)(±50)(±150)
Input Offset Voltage - mV	±4 max	±4 max	±5(±2)(±2)(±5)(±2)(±2) max
vs. Temperature (0 to +70°C) - μV/°C	±30 max	±30 max	±5(±1)(±10max)[1] (±5)(±1)(±10 max)[1]
Response			
Settling Time - μs	1	1	–
Overload Recovery - ms	1μs	1μs	–
Output			
Waveform	← TRAIN OF TTL/DTL COMPATIBLE PULSES →		Symmetrical
Pulse Width - μs	0.1 to 0.15/f max	0.1 to 0.15/f max	Square Wave, TTL, DTL, CMOS,
Pulse Polarity	← POSITIVE →		ECL, HNIL Compatible by Selection
Logic "1" (HIGH) Level - V min	Compatible by	Compatible by	of External Resistor
Logic "0" (LOW) Level) Level - V max	Resistor Selection	Resistor Selection	
Power Supply			
Voltage, Rated Performance - V dc	±9 to ±18	±9 to ±18	+5 to +36 or ±5 to ±18
Current, Quiescent - mA	6	6	1.2
Temperature Range[2]			
Rated Performance - °C	C(I)(M)	C(C)(M)	C(C)(M)(C)(C)(M)
Case Size - Inches	D–14-Pin DIP H–TO-100 Can	D–14-Pin DIP	D–14-Pin DIP: H–TO-100 Can

NOTES

[1] Guaranteed over -55°C to +125°C temperature range

[2] C = 0 to +70°C, M = -55°C to +125°C

MULTIPLEXERS AND SWITCHES

SPECIFICATIONS
(T_A = +25°C, V_{SUPPLY} = ±15V unless otherwise noted)

Type[1]	Function	R_{ON} Ω, max	Off Leakage nA, max	Temp Range[2]	Logic Compatibility
AD7501JN(JD)			10	C/I	CMOS
AD7501KN(KD)	8-Channel	300	10	C/I	TTL/CMOS
AD7501SD			5	M	TTL/CMOS
AD7502JN(JD)	Dual		5	C/I	CMOS
AD7502KN(KD)	4-Channel	300	5	C/I	TTL/CMOS
AD7502SD	(differential)		3	M	TTL/CMOS
AD7503JN(JD)			10	C/I	CMOS
AD7503KN(KD)	8-Channel	300	10	C/I	TTL/CMOS
AD7503SD			5	M	TTL/CMOS
AD7506JN(JD)		450	20	C/I	CMOS
AD7506KN(KD)	16-Channel	450	20	C/I	TTL/CMOS
AD7506SD		400	10	M	CMOS
AD7506TD		400	10	M	TTL/CMOS
AD7507JN(JD)	Dual	450	10	C/I	CMOS
AD7507KN(KD)	8-Channel	450	10	C/I	TTL/CMOS
AD7507SD	(differential)	400	5	M	CMOS
AD7507TD		400	5	M	TTL/CMOS

NOTES

[1] Suffix "N": plastic DIP; Suffix "D": ceramic DIP

[2] C: Commerical (0 to +70°C)
I: Industrial (-25°C to +85°C)
M: Military (-55°C to +125°C)

SPECIFICATIONS
(T_A = +25°C, V_{SUPPLY} = ±15V unless otherwise noted)

Type[1]	Function	R_{ON} Ω, max	OFF Leakage	Temp Range[2]	Logic Compatibility
ADG200CJ		80	5nA, max	C	TTL/CMOS
ADG200BP		80	5nA, max	I	TTL/CMOS
ADG200BA	Dual SPST	80	5nA, max	I	TTL/CMOS
ADG200AP		70	2nA, max	M	TTL/CMOS
ADG200AA		70	2nA, max	M	TTL/CMOS
ADG201CJ		100	5nA, max	C	TTL/CMOS
ADG201BP	Quad SPST	100	5nA, max	I	TTL/CMOS
ADG201AP		80	1nA, max	M	TTL/CMOS
AD7510DIJN(JD)	Quad SPST		5nA, max	C/I	CMOS
AD7510DIKN(KD)	Note 3	100	5nA, max	C/I	TTL/CMOS
AD7510DISD			3nA, max	M	TTL/CMOS
AD7511DIJN(JD)	Quad SPST		5nA, max	C/I	CMOS
AD7511DIKN(KD)	Note 3	100	5nA, max	C/I	TTL/CMOS
AD7511DISD			3nA, max	M	CMOS
AD7511DITD			3nA, max	M	TTL/CMOS
AD7512DIJN(JD)	Dual SPDT		15nA, max	C/I	CMOS
AD7512DIKN(KD)	Note 3	100	15nA, max	C/I	TTL/CMOS
AD7512DISD			9nA, max	M	CMOS
AD7512DITD			9nA, max	M	TTL/CMOS
AD7590DIKN	Quad SPST	90	5nA, max	C	TTL/CMOS
AD7590DIBD	with Data	90	5nA, max	I	TTL/CMOS
AD7591DIKN	Latches	90	5nA, max	C	TTL/CMOS
AD7591DIBD		90	5nA, max	I	TTL/CMOS
AD7592DIKN	Dual SPDT	90	5nA, max	C	TTL/CMOS
AD7592DIBD	with Data Latches	90	5nA, max	I	TTL/CMOS

NOTES

[1] Suffixes: N – Plastic DIP
P, D – Ceramic DIP
A, H – TO-100

[2] C: Commercial (0 to +70°C)
I: Industrial (-25°C to +85°C)
M: Military (-55°C to +125°C)

[3] Dielectrically isolated features latchup-free overvoltage proof operation.

[4] $V_{DD} - V_{SS}$ (supply voltages) = +15V

[5] V_{DD} (supply voltage) = 8V

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ANALOG DEVICES

Voltage References

INTEGRATED CIRCUIT REFERENCES

The accuracy of all measurements is determined by the reference employed. Analog Devices' references use buffered low TC precision zener diodes or patented laser wafer trimmed monolithic bandgap circuitry. Both include output operational amplifiers for optimum load regulation.

The AD2720 precision hybrid reference provides the highest initial accuracy and lowest temperature coefficient. The proprietary temperature compensated design and active laser trimming result in ultra high precision performance previously available only in oven-regulated modules.

AD584 V_{OUT} = 10.000V or 7.500V or 5.000V or 2.500V

The AD584 is a unique bandgap reference. Depending on user requirements it may be connected to provide any one of four standard voltages without additional external parts.

SPECIFICATIONS

(typical @ V_{IN} = +15V and +25°C unless otherwise noted)

Model	Maximum Error in mV for Nominal Output of: 2.5V	5V	7.5V	10V	Temp Stability ppm/°C max	Temp Range[1]
AD584JH	±7.5	±15	±22	±30	30	C
AD584KH	±3.5	±6	±8	±10	15	C
AD584LH	±2.5	±3	±4	±5	5	C
AD584SH	±7.5	±15	±22	±30	30	M
AD584TH	±3.5	±6	±8	±10	15	M

NOTE
[1] C = 0 to +70°C, M = –55°C to +125°C

SPECIFICATIONS

(min–max @ E_{IN} = +15V or –15V and +25°C unless otherwise noted)

Model	Output Voltage Volts	Output Voltage Tolerance % Error	Output Current mA	Temp Stability ppm/°C	Time Stability (typ)	Temp Range[1]
AD580JH(KH)(LH)(MH)	2.5	3.0(1.0)(0.4)(0.4)	10	85(40)(25)(10)	25μV/Month 250μV Long Term	C
AD580SH(TH)(UH)	2.5	1.0(0.4)(0.4)	10	55(25)(10)	25μV/Month 250μV Long Term	M
AD581JH(KH)(LH)	10.000	±0.3(0.1)(0.05)	10	30(15)(5)	25ppm per 1000 Hours Noncumulative	C
AD581SH(TH)(UH)	10.000	±0.3(0.1)(0.05)	10	30(15)(5)	25ppm per 1000 Hours Noncumulative	M
AD589JH(KH)(LH)(MH)	1.235	-2.8, +1.2	5	100(50)(25)(10)		C
AD589SH(TH)(UH)	1.235 typ	-2.8, +1.2	5	100(50)(25)		M
AD2700J(S)	10.000	±0.05	10	10(3)	100ppm per	I/M
AD2700L(U)	10.000	±0.025	10	3	1000 Hours @ +55°C	I/M
AD2701J(S)	-10.000	±0.05	10	10(3)	100ppm per	I/M
AD2701L(U)	-10.000	±0.025	10	3	1000 Hours @ +55°C	I/M
AD2702J(S)	±10.000	±0.05	10	10(5)	100ppm per	I/M
AD2702L(U)	±10.000	±0.025	10	5(3)	1000 Hours @ +55°C	I/M
AD2710KN(LN)	+10.000	±0.01	10	2(1)		C
AD2712KN(LN)	±10.000	±0.01	10	2(1)		C
AD2720AH	+10.000	±0.02	5	4	25ppm per	I
AD2720BH	+10.000	±0.01	5	2	1000 Hours	I
AD2720CH	+10.000	±0.01	5	1	@ +25°C	I
AD2720SH	+10.000	±0.02	5	4		M
AD2720TH	+10.000	±0.01	5	2		M

NOTES
[1] C = 0 to +70°C, I = -25°C to +85°C, M = -55°C to +125°C

FEATURE SELECTION CHART

Feature		AD589	AD580	AD1403	AD581	AD584	AD2700	AD2710	AD2720
Output Voltage Range	1.235V	•				•			
	2.5V		•	•		•			
	5.0V					•			
	7.5V					•			
	+10.00V				•	•	•	•	•
	-10.00V						•		
	±10.00V						•	•	
Output Voltage Tolerance	≤±0.4%		•	•	•	•	•	•	•
	≤±0.05%				•	•	•	•	•
	≤±0.025%						•	•	•
	≤±0.012%							•	•
Temperature Stability	≤25ppm/°C	•	•	•	•	•	•	•	•
	≤10ppm/°C		•		•	•	•	•	•
	≤5ppm/°C				•	•	•	•	•
	≤1ppm/°C							•	•
Temperature Range	0 to +70°C	•	•	•	•	•	•	•	•
	-25°C to +85°C						•		•
	-55°C to +125°C	•	•		•	•			•
Package Style	Hermetic Package	•	•		•	•	•	•	•
	Plastic Package			•					
Dice Available		•	•		•	•			

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ANALOG DEVICES

High Speed Sample-and-Hold Amplifier

AD585

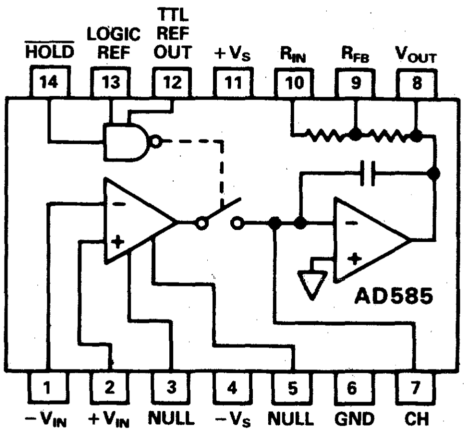
FEATURES

Fast 2.5μs Acquisition Time to ±0.01%
Low Droop Rate: 0.5mV/ms
Low Offset: 1mV
Sample/Hold Offset Step: 1mV
Aperture Jitter: 0.5ns
Military Temperature Range: −55°C to +125°C
Internal Hold Capacitor

APPLICATIONS

Data Acquisition Systems
Data Distribution Systems
Analog Delay & Storage
Peak Amplitude Measurements

AD585 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

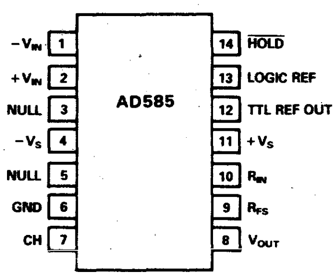
The AD585 is a monolithic sample-and-hold circuit consisting of a high performance operational amplifier in series with an ultra-low leakage analog switch and a FET input integrating amplifier. An internal holding capacitor and connections to the internal feedback resistors, completes the sample and hold.

With the analog switch closed, the AD585 functions like a standard op amp; any feedback network may be connected around the device to control gain and frequency response. With the switch open, the capacitor holds the output at its previous level.

The AD585 offers performance previously unavailable in monolithic sample-and-hold amplifiers. The combination of a fast acquisition time (2.5μs to 0.01%) and low offset step (1mV) are suitable for high speed 12-bit data acquisition systems.

The device is available in two versions: the "J" specified for operation over the 0 to +70°C commercial temperature range and the "S" specified over the full extended temperature range −55°C to +125°C.

PIN CONFIGURATION

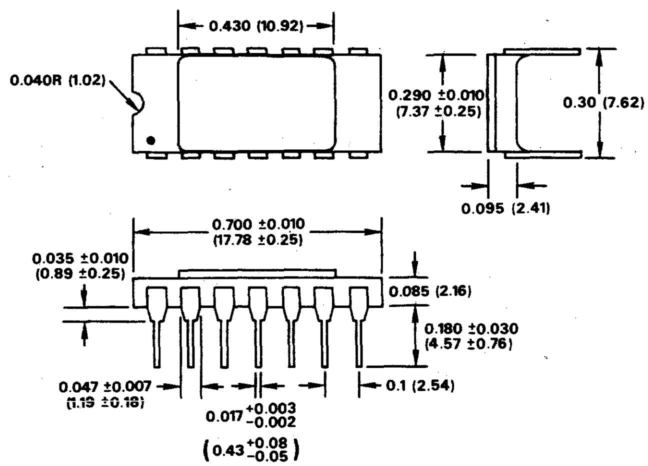


PRODUCT HIGHLIGHTS

1. The droop rate is only 0.5mV/ms so that it may be used in slower high accuracy systems without the loss of accuracy.
2. The fast acquisition time and low aperture make it suitable for very high speed data acquisition systems.
3. The AD585 has internal pretrimmed application resistors for applications versatility.
4. The AD585 is complete with an internal hold capacitor for ease of use and capacitance can be added externally to achieve higher accuracy.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



ANALOG DEVICES

Ultra High Speed Hybrid Track-and-Hold Amplifiers

HTS-0010

FEATURES
Aperture Jitter of 5ps
Acquisition Time 10ns
Output Current ±40mA
Slew Rate 300V/μs

APPLICATIONS
Data Acquisition Systems
Radar Systems
Instrumentation Systems
Medical Electronics

GENERAL DESCRIPTION

The Analog Devices HTS-0010 Track-and-Hold is another example of Analog's continuing efforts to advance the state of the art in high-speed circuits.

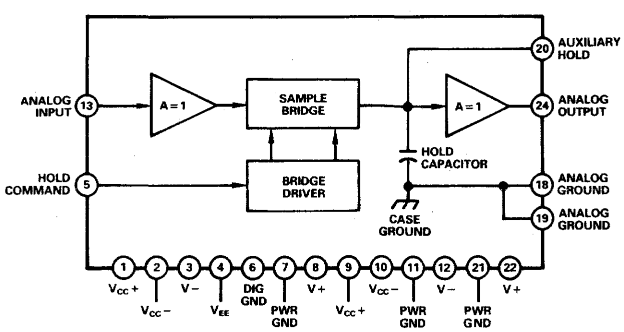
The HTS-0010 adds breadth to a line of devices which offers designers the industry's widest range of track-and-hold and sample-and-hold units.

Its pinouts are similar to its predecessor HTS-0025 Track-and-Hold, but it provides enchanced performance in many of the characteristics established by that device. Two pins which are unused on the HTS-0025 are used on the HTS-0010, but with those exceptions, the two devices have identical pin assignments. This plug-in compatibility gives designers remarkable flexibility in selecting those parameters which are optimum for their applications.

The HTS-0010 Track-and-Hold (T/H) uses many of the proven design concepts which have made the HTS-0025 T/H the standard of comparison for high-speed circuits of this type. A dc-coupled Schottky diode bridge is driven by a high impedance buffer amplifier and followed by a low impedance output amplifier to achieve the best possible combination of speed and drive capabilities.

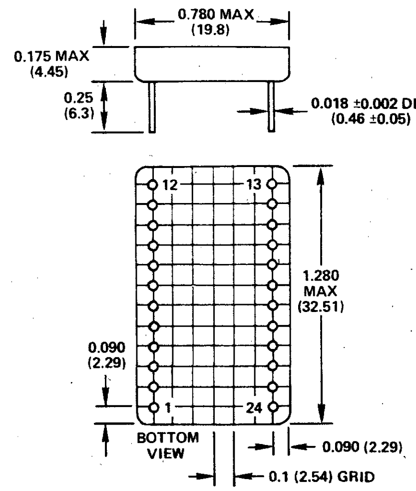
All models of the HTS-0010 are housed in a standard 24-pin metal DIP. The unit operating over a temperature range of 0 to +70°C is HTS-0010KD; the unit for a range of −55°C to +100°C is HTS-0010SD.

HTS-0100 FUNCTIONAL BLOCK DIAGRAM



OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



DOT ON TOP AND CERAMIC BEAD ON BOTTOM INDICATE POSITION OF PIN 1. PINS ARE GOLD PLATED.

PIN DESIGNATIONS

PIN	FUNCTION
1	V_{CC}+ (+5V)
2	V_{CC}− (−5V)
3	V− (−15V)
4	V_{EE} (−5.2V)
5	HOLD COMMAND
6	DIGITAL GROUND
7	POWER GROUND
8	V+ (+15V)
9	V_{CC}+ (+5V)
10	V_{CC}− (−5V)
11	POWER GROUND
12	V− (−15V)
13	ANALOG INPUT
14	N/A
15	N/A
16	N/A
17	N/A
18	ANALOG GROUND
19	ANALOG GROUND
20	AUXILIARY HOLD
21	POWER GROUND
22	V+ (+15V)
23	N/A
24	ANALOG OUTPUT

POWER GROUND (PINS 7, 11 AND 21), ANALOG GROUND (PINS 18 AND 19), AND DIGITAL GROUND (PIN 6) MUST BE CONNECTED TOGETHER AND TO A LOW-IMPEDANCE GROUND FOR PROPER OPERATION. MAKE CONNECTIONS AS CLOSE TO DEVICE AS POSSIBLE. HYBRID CASE IS CONNECTED TO ANALOG GROUND INTERNALLY.

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High Speed Hybrid Track-and-Hold Amplifiers

HTC-0500

INTERFACE

Analog Devices

ANALOG DEVICES

FEATURES
700ns Acquisition Time
<750mW Power Dissipation
14-Pin DIP
0.01% Linearity

APPLICATIONS
Data Acquisition Systems
Data Distribution Systems
Analog Delay and Storage
Peak Amplitude Measurements

GENERAL DESCRIPTION

The Analog Devices HTC-0500 Track/Sample Hold is a remarkable combination of speed and low power dissipation in a 14-pin DIP. Its low cost makes it extremely attractive for a wide range of applications which were often uneconomical until now.

Exceptional speed and minimum power in a small, cost-effective package are not the only characteristics which make this unit worth serious consideration for a variety of uses. The innovative design ideas which have been included make it possible for the user to vary the gain of this inverting amplifier.

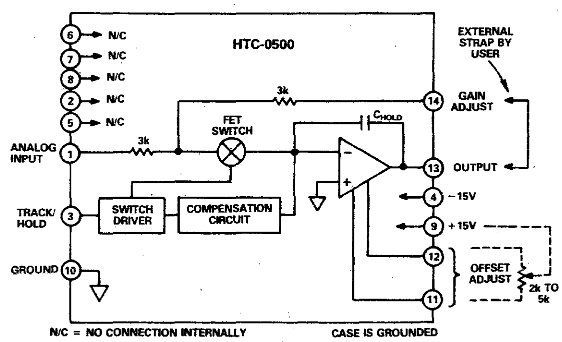
In many instances, Track/Sample-Hold devices may allow the user to decrease the gain, but increasing the gain is impossible. This is because the majority of these units close the feedback loop internally.

The HTC-0500, however, gives the designer flexibility when it is incorporated into its system application because it can be varied around its normal unity gain. In fact, as shown in Figure 1, the user must close the feedback loop externally with a strap to get proper operation.

The HTC-0500 is a perfect choice for use with Analog Devices' converters such as the HAS-1202, AD578, and AD579 in applications which do not require the speed of the model HTC-0300 Track-and-Hold, but require higher speed than the ADSHC-85.

The standard unit is housed in a metal dual in-line package; its model number is HTC-0500AM. A temperature range of −55°C to +125°C is available with model HTC-0500SM.

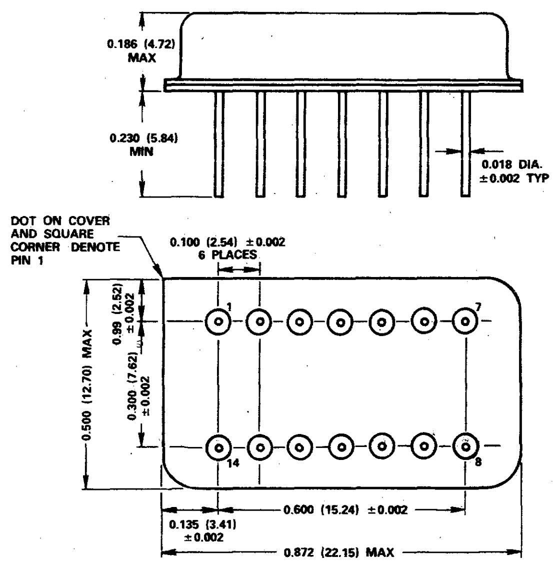
HTC-0500 FUNCTIONAL BLOCK DIAGRAM



NORMAL GAIN (−1) OPERATION

MECHANICAL DIMENSIONS

Dimensions shown in inches and (mm).



BOTTOM VIEW

ANALOG DEVICES

Fast, Complete, 16-Channel µP Compatible 12-Bit Data Acquisition System

AD364

ADVANCED TECHNICAL DATA

FEATURES
- Complete Data Acquisition System in 2-Package IC Form
- Full 8- or 16-Bit Microprocessor Bus Interface
- 16 Single-Ended or 8 Differential Channels with Switchable Mode Control
- True 12-Bit Operation: Nonlinearity ≤±0.012%
- Guaranteed No Missing Codes Over Specified Temperature Range
- High Throughput Rate: 20kHz
- Fast Successive Approximation Conversion: 25µs
- Buried Zener Reference for Long-Term Stability and Low Gain TC
- Small Size: Requires Only 2.8 Square Inches
- Short-Cycle Capability
- Low Power: 1.4 Watts
- Extended Temperature Range: -55°C to +125°C

PRODUCT DESCRIPTION

The AD364 is a complete 16 channel, microprocessor compatible, 12-bit data acquisition system in integrated circuit form. The AD364 design is implemented with linear compatible LSI chips, active laser trimming and hybrid technology resulting in maximum performance and flexibility.

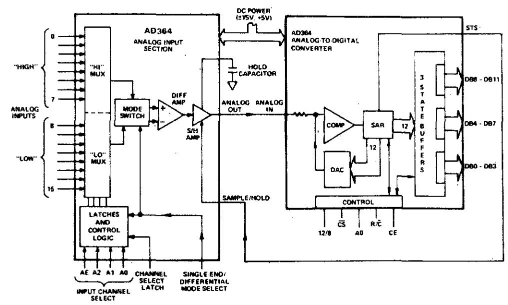
The AD364 consists of two separate functional blocks, each in a hermetically sealed dual-in-line package. The analog input section contains two eight-channel multiplexers, a differential amplifier, a sample-and-hold, a channel address register and control logic. The multiplexers may be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A unique feature of the AD364 is an internal user-controllable analog switch that connects the multiplexers in either a single-ended or differential mode. This allows a single device to perform in either mode without hard-wire programming and permits a mixture of single-ended and differential sources to be interfaced to an AD364 by dynamically switching the input mode control.

The ADC section contains a complete 12-bit successive approximation ADC, including internal clock, precision 10 volt reference, comparator and bus interface. The ADC uses the newly-developed LCI (Linear-Compatible Integrated Injection Logic) process to provide the low power logic necessary to make a high speed 12-bit ADC and 3-state output buffer circuitry for direct interface to an 8-, 12- or 16-bit microprocessor bus.

AD364 ORDERING GUIDE

Model	Linearity	Temp. Range
AD364JD	±0.024%	0 to +70°C
AD364KD	±0.012%	0 to +70°C
AD364SD	±0.024%	-55°C to +125°C
AD364TD	±0.024%	-55°C to +125°C

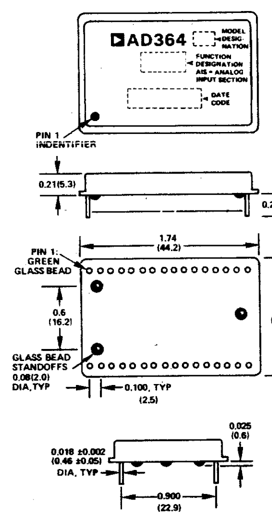
AD364 FUNCTIONAL BLOCK DIAGRAM



OUTLINE DIMENSIONS PACKAGE SPECIFICATIONS

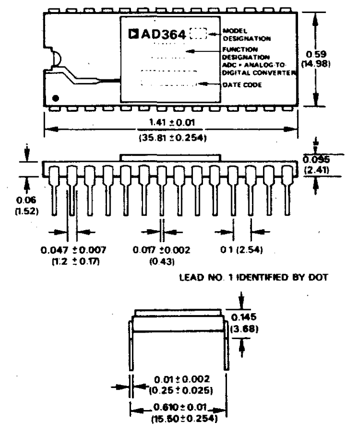
Dimensions shown in inches and (mm).

ANALOG INPUT SECTION

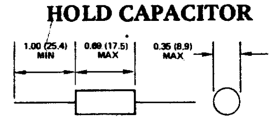


NOTES:
1) PACKAGE: KOVAR WITH 100µIN. MIN., NICKEL PLATE
2) PINS: KOVAR WITH 50µIN. MIN 24K GOLD PLATE
3) PACKAGE AND PINS MEET ALL REQUIREMENTS OF MIL-STD-883
4) TOLERANCES, UNLESS OTHERWISE NOTED:
a) .XX: ±.01 (.25)
b) .XXX: ±.005 (.13)

ANALOG-TO-DIGITAL CONVERTER

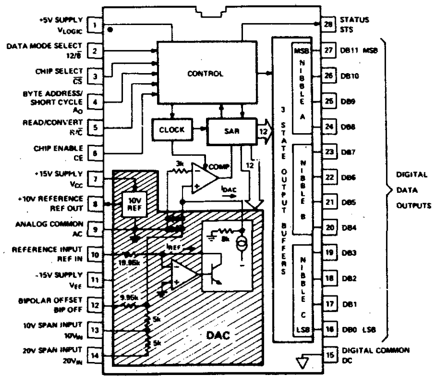


HOLD CAPACITOR



*THIS DIMENSION IS FOR POLYSTYRENE CAPACITOR SUPPLIED WITH J AND K GRADES.

MAX BODY LENGTH OF TEFLON CAPACITOR SUPPLIED WITH S AND T GRADES IS 1.00".



ONE TECHNOLOGY WAY • P.O. BOX 280 • NORWOOD, MA 02062 • (617) 329-4700

Sample/Track-Hold Amplifiers

IC SAMPLE-HOLD AMPLIFIERS

The AD582, AD583 and AD585 are monolithic sample-and-hold amplifiers with high performance internal amplifiers and a low leakage analog switch. An external hold capacitor is used with the AD582 and AD583, while the AD585 includes an on-chip hold capacitor.

The AD582 is the lowest cost SHA; yet it can replace many modular and hybrid units. For faster acquisition time or greater precision, the AD583 and AD585 are recommended.

Greater speed is provided by the HTC-0500, with an acquisition time of 700ns. The highest speed IC track-and-holds are the HTC-0300, HTC-0300A and HTS-0025. These units have acquisition times, respectively, of 170ns, 150ns and 30ns.

The HTC-0500, HTC-0300 and HTC-0300A are used with fast ADC's such as the HAS Series, the AD578, or AD579. The HTS-0025 is optimized for use with "video" ADC's and is also an excellent choice for use as a deglitcher at the output of high-speed current output DAC's. The ADSHC-85 is a second source for a generic industry-standard device.

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

Model	Open Loop Gain RL=2kΩ k min	Output V_{min}/mA min	Gain Bandwidth MHz	Acquisition Time (0.1%)[1]	Aperture Time ns	Aperture Uncertainty	Droop Rate mV/ms	Oper. Temp[2]	Package
AD582K	25[3]	±10/±10	1.5	6μs	150	15ns	100pA[4]	C	14-Pin DIP TO-100
AD582S	25[3]	±10/±10	1.5	6μs	150	15ns	100pA[4]	M	14-Pin DIP TO-100
AD583K	25[3]	±10/±10	2	4μs	50	5ns	50pA[4]	C	14-Pin DIP
AD585J	30[3]	±10/±10	2.5	2.5μs[5]	10	1ns	0.5	C	14-Pin DIP
AD585S	30[3]	±10/±10	2.5	2.5μs[5]	10	1ns	0.5	M	14-Pin DIP
ADSHC-85	+1	±10/±10[6]	0.2	4.5μs[5]	25	0.5ns	0.2	C	14-Pin DIP
ADSHC-85ET	+1	±10/±10[6]	0.2	4.5μs[5]	25	0.5ns	0.2	M	14-Pin DIP
HTS-0010KD/SD	0.96	±2/±40	60	15ns	-2	5ps	0.1	C/M	24-Pin DIP
HTS-0025	0.92	±2/±50	30	30ns	10	20ps	200	C	24-Pin DIP
HTS-0025M	0.92	±2/±50	20	30ns	10	20ps	200	MR	24-Pin DIP
HTC-0300	-1	±10/±50	8	170ns	10	100ps	5	C	24-Pin DIP
HTC-0300A	-1	±10/±50	10	150ns	6	100ps	1	C	24-Pin DIP
HTC-0300AM	-1	±10/±50	10	150ns	6	100ps	1	M	24-Pin DIP
HTC-0300M	-1	±10/±50	8	170ns	6	100ps	5	MR	24-Pin DIP
HTC-0500AM	-1	±12/±15	2	700ns	30	60ps	0.5	I	14-Pin DIP
HTC-0500SM	-1	±12/±15	2	700ns	30	60ps	0.5	M	14-Pin DIP

NOTES
[1] A_V=1, R_L=2k, C_L=50pF
[2] C = 0 to +70°C, I = -25°C to +85°C, M = -55°C to +125°C, MR = -55°C to +100°C
[3] Open-loop gain – k min, R_L = 2kΩ
[4] Droop current; rate depends on external capacitance
[5] Acquisition Time to 0.01%
[6] Typical outputs

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BURR-BROWN®

DATA CONVERSION

ANALOG-TO-DIGITAL CONVERTERS

Description	Model	Resolution (Bits)	Linearity Error (% of FSR) max	Conversion Time (μsec) max	Tempco Bipolar (ppm of FSR/°C) max	Input Range (V)	Package
−55°C to +200°C	ADC10HT	12	±0.012 to ±0.048	50	±34 to ±63	±5, ±10, +10, +20	Hermetic DIP
High Speed	ADC60	8 - 12	±0.195 to ±0.0244	0.88 - 3.5	±15 to ±20	±2.5 to +20	Module
High Resolution	ADC71 ADC72 ADC73/731	16 16 16	±0.003 to ±0.006 ±0.003 to ±0.006 ±0.0015 to ±0.00075	50 50 170	±15 ±12 to ±17 ±10	±2.5 to ±20 ±2.5 to ±20 ±5, ±10, +10, +20	DIP Hermetic DIP Module
High Speed, High Resolution	ADC76	16	±0.003 to ±0.006	15	±15	±2.5 to +20	DIP
Low Cost	ADC80	10 - 12	±0.048 to ±0.012	21 - 25	±23	±2.5 to ±10	DIP
High Speed, Low Cost	ADC82 ADC84	8 10 - 12	±0.2 ±0.012 to ±0.048	2.8 6 - 10	±60 ±21	±2.5 to +20 ±2.5 to ±10	DIP Hermetic DIP
High Speed, Low Drift	ADC85	10 - 12	±0.012 to ±0.048	6 - 10	±13 to ±26	±2.5 to ±10	Hermetic DIP
Ultra-High Speed	ADC803	12	±0.015 to ±0.02	1.5	±30	0 to −10V, ±5V	Hermetic DIP

DIGITAL-TO-ANALOG CONVERTERS

Description	Model	Resolution	Linearity Error (% of FSR) max	Tempco (ppm of FSR/°C) max	Output Range	Settling Time (FSR ±1/2LSB)	Package
−55°C to +200°C	DAC10HT	12 Bits	±0.012 to ±0.048	±20 to ±50	±2.5, ±5, ±10, +5, +10	200nsec	Hermetic DIP
Very High Speed	DAC60	10 - 12 Bits	±0.012 to ±0.048	±15	−5 to ±2.5mA	40 - 150nsec	Module
Ultra High Speed	DAC63	12 Bits	±0.01	25	0 to −10, ±5mA	40nsec	DIP
High Resolution	DAC70 DAC71 DAC72 DAC73 DAC736	16 Bits, 4 Digits 16 Bits, 4 Digits 16 Bits, 4 Digits 16 Bits 16 Bits	±0.003 to ±0.005 ±0.003 to ±0.005 ±0.003 to ±0.005 ±0.00075 to ±0.0015 ±0.00075 to ±0.[illegible]5	±12 to ±24 ±15 to ±50 ±10 to ±40 ±24 ±24	0 to −2mA, ±1mA 0 to ±10V, −2 to ±1mA 0 to ±10V, −2 to ±1mA ±2.5 to ±10V, −2 to ±1mA ±2.5 to ±10V, −2 to ±1mA	50μsec 1 - 10μsec 1 - 10μsec 50μsec 50μsec	Hermetic DIP DIP Hermetic DIP Module Module
High Resolution Monolithic	DAC701/703 DAC700/702	16 Bits 16 Bits	±0.003 ±0.003	±18 to ±28 ±18 to ±28	0 to +10V, ±10V 0 to −2mA, ±1mA	8μsec 300nsec	Hermetic DIP Hermetic DIP
High Resolution Self-Calibrating	DAC74	16 Bits	±0.0075	0 after self-calibration +15°C to +45°C	0 to +10V, ±10V	50μsec	Module
Low Cost	DAC80	12 Bits, 3 Digits	±0.012 to ±0.025	±25	±2.5 to ±10V, −2 to ±1mA	300nsec to 5μsec	DIP
Voltage and Current Output	DAC82	8 Bits	±0.16	±50	±2.5 to ±10V, −1.6 to ±0.8mA	2.5μsec	Hermetic DIP
Low Drift	DAC85	12 Bits, 3 Digits	±0.012 to ±0.025	±5 to ±20	±2.5 to ±10V, −2 to ±1mA	300nsec to 5μsec	Hermetic DIP
Monolithic	DAC90 DAC800	8 Bits 12 Bits	±0.2 ±0.012	±50 ±25	−2 to ±1mA −2.5 to ±10V, −2.35 to ±1.175mA	200nsec 300nsec to 5μsec	Hermetic DIP DIP
Very Low Cost Monolithic	DAC800P	12 Bits	±0.012	±25	±2.5, ±5, ±10, 0 to +5, 0 to +10	3μsec	Plastic DIP
Monolithic	DAC850 DAC851	12 Bits 12 Bits	±0.012 ±0.012	±17 ±30	±2.5 to ±10V, −2.35 to ±1.175mA ±2.5 to ±10V, −2.35 to ±1.175mA	300nsec to 5μsec 300nsec to 5μsec	Hermetic DIP Hermetic DIP

[This table continued on next page]

FOR ADDITIONAL DETAILS REFER TO THE BURR-BROWN PRODUCT DATA BOOK OR CONTACT YOUR NEAREST BURR-BROWN SALES OFFICE.

DATA CONVERSION [cont]

DIGITAL-AUDIO CONVERTERS

Description	Model	Resolution (Bits)	Total Harmonic Distortion (max)	Conversion Time (max)	Input Range (V)	Dynamic Range
PCM-Audio A/D Converter(2)	PCM75KG PCM75JG	16 14(3)	0.02% at −15dB 0.05% at −15dB	17μsec(1) 15μsec(1)	±2.5, ±5, ±10 ±2.5, ±5, ±10	90dB 90dB
Description	**Model**	**Resolution (Bits)**	**Total Harmonic Distortion (max)**	**Settling Time(5)**	**Output Range (V)**	**Dynamic**
PCM-Audio D/A Converter	PCM50KG	16(4)	0.02% at −15dB	5μsec	±5, ±10	96dB
Low Cost PCM-Audio D/A Converter	PCM52JG-V/53JG-V	16	0.04% at −20dB	3μsec	±5, ±10	96dB

NOTES: (1) Can be reduced to 8μsec. (2) With internal 16-bit DAC. (3) Can operate at 16 bits. (4) Can operate at 14 bits. (5) 20V step.

VOLTAGE-TO-FREQUENCY CONVERTERS

Description	Model	V_{IN} Range (V)	F_{OUT} Range (kHz)	Linearity (% of FSR) max	Tempco (ppm of FSR/°C) max	Package
High Linearity Monolithic	VFC320	0 to +10	0 to 1000	±0.005% at 10kHz ±0.03% at 100kHz ±0.1% typ at 1MHz	±20 to ±50	DIP & TO-100
High Linearity Monolithic Totem Pole Output	VFC62	0 to +10	0 to 1000	±0.005% at 10kHz ±0.03% at 100kHz ±0.1% typ at 1MHz	±20 to ±50	DIP & TO-100
Low Cost, Monolithic	VFC32	0 to +10	0 to 500	±0.01 at 10kHz ±0.05 at 100kHz	±75 to ±150	DIP & TO-100
Low Cost, Complete Hybrid	VFC42 VFC52	0 to +10 0 to +10	0 to 10 0 to 100	±0.01 ±0.05	±100 ±150	DIP DIP
Low Drift, Complete	VFC12 VFC15	0 to +10 0 to +20	0 to 10 0 to 20	±0.01 ±0.01	50 50	Module Module

MICROPROCESSOR-INTERFACED ANALOG INPUT SYSTEMS

Compatible With	Model	Channels	Resolution (Bits)	Accuracy (% of FSR) max	Accuracy Drift (ppm/°C) max	Package
8080, SC/MP Compatible	MP20	8 Differential, 16 Single-ended	8	±0.8 at high gain, ±0.4 at low gain	±40	DIP
6800, 6502 Compatible	MP21	8 Differential, 16 Single-ended	8	±0.8 at high gain, ±0.4 at low gain	±40	DIP
Universal	MP22 MP32	8 Differential, 16 Single-ended 8 Differential, 16 Single-ended	12 12	±0.4 at high gain, ±0.1 at low gain ±0.4 at high gain, ±0.05 at low gain	±25 ±25	DIP DIP

MICROPROCESSOR-INTERFACED ANALOG OUTPUT SYSTEMS

8080, SC/MP Compatible	MP10	2	8	±0.4	±80	DIP
6800, 6502 Compatible	MP11	2	8	±0.4	±80	DIP

DATA ACQUISITION SYSTEMS

Description	Model	Channels	Resolution (Bits)	Accuracy (% of FSR)	Throughput Rate (kHz)	Package
Modular, Low Level	SDM853	8 Differential, 16 Single-ended	12	±0.025	30	Module
Hybrid, ±10V Input	SDM854	8 Differential, 16 Single-ended	12	±0.024 to ±0.048	25 to 33	DIP
Hybrid, ±5V Input	SDM856	8 Differential, 16 Single-ended	12	±0.024 to ±0.048	25 to 33	DIP
Hybrid, Low Level	SDM857	8 Differential, 16 Single-ended	12	±0.024 to ±0.048	18 to 22	DIP
Modular, Low Level	SDM858	8 Differential, 16 Single-ended	12	±0.025 (at G = 100)	8	Module

SAMPLE/HOLD CIRCUITS

Description	Model	Gain Offset Error (%) (mV)	Charge Offset (mV)	Droop Rate (mV/msec)	Tempco (ppm of 20V/°C)	Acquisition Time (μsec)	Package
Low Cost, Complete	SHC80	±0.01, ±2 max	±2 max	0.5max	±3	10 max	DIP
High Speed, Complete	SHC85	±0.01, ±2 max	±2 max	0.5 max	±3	4.5 max	Hermetic DIP
Low Cost, Monolithic	SHC298	±0.01 max, ±7 max	±25 max	0.125 max	±4	10 max	TO-99
Very High Speed	SHM60	±0.01 max, ±1.5	±1.5	0.005/0.001	±2	1 max	Module

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DATA CONVERSION [cont]

MULTIPLEXERS							
Type	Model	Channels	Input Range (V)	On Resistance (kμ) max	Crosstalk (% of Off Channel Signal)	Settling Time (to 0.01%) (μsec)	Package
CMOS	MPC8S	8 Single-ended	±15	1.8	0.005	5	Hermetic DIP
	MPC4D	4 Differential	±15	1.8	0.005	5	Hermetic DIP
	MPC16S	16 Single-ended	±15	1.8	0.005	7	Hermetic DIP
	MPC8D	8 Differential	±15	1.8	0.005	7	Hermetic DIP
CMOS (−55 to +125°C)	MPC800	16 Single-ended, 8 Differential	±15	0.75	0.0005	0.8	Hermetic DIP
	MPC801	8 Single-ended, 4 Differential	±15	0.75	0.0005	0.8	Hermetic DIP

OPERATIONAL AMPLIFIERS

Description	Model	Rated Output		Offset Voltage		Bias Current at 25°C	Frequency Response		Package
		±V	±mA	at 25°C mV	Temp. Drift μV/°C	pA	Unity Gain MHz	Slew Rate V/μsec	
LOW DRIFT									
Low Power	OPA21	13.5	1.3	0.1 - 0.5	1-5	50 - 100nA	0.6	0.25	TO-99, DIP
Low Noise	OPA27	12	11.5	0.025 - 0.1	0.6 - 1.8	40 - 80nA	5	1.7	TO-99, DIP
Low Noise (AV = 5 min)	OPA37	12	11.5	0.025 - 0.1	0.6 - 1.8	40 - 80nA	40	11	TO-99, DIP
Switchable-Input (SWOP-Amp)	OPA201	±10	±5	0.1 - 0.5	1 - 5	25 - 50nA	0.5	0.1 min	DIP
Chopper-Stabilized	3291	10	5	0.02 - 0.10	0.10 - 1	±50 to ±100	3	6	Module
	3354	10	5	0.03 - 0.10	0.10 - 1	±20 to ±50	3	6	Module
	3271	50 - 110	20	0.05	1	±80	1	20	Module
Bipolar	3500	10	10	0.5 - 5	1 - 20	±15 to ±50nA	1.5	0.6 - 1	TO-99
	3501	10	5	2 - 5	5 - 20	±3 to ±15nA	0.5	0.1	TO-99
	3510	10	10	0.06 - 0.15	0.5 - 2	±15 to ±35nA	0.4	0.5	TO-99
FET	3521	10	10	0.25 - 0.50	1 - 10	−10 to −20	1.5	0.6	TO-99
	3527	10	10	0.25 - 0.50	2 - 10	−2 to −5	1	0.6	TO-99
LOW BIAS CURRENT									
−55°C to +200°C	OPA11HT	10	15	5	5	±25nA	12	7	TO-99
Low Bias, Low Drift, Enhanced Bi FET	OPA100	10	5	0.25 - 1	5 - 15	±1 to ±3	1	2	TO-99, DIP
Low Noise	OPA101/102	12	12	0.25 - 0.5	5 - 10	−10 to −15	10	5 - 10	TO-99
Low Bias	OPA103	10	5	0.25 - 0.5	2 - 25	−1 to −2	1	0.9	TO-99
Ultra-Low Bias	OPA104	10	5	0.5 - 1.0	10 - 25	−0.075 to −0.3	1	1.6	TO-99
FET Ultra-Low Bias	3528	10	5	0.25 - 0.50	5 - 15	±0.075 to −0.30	0.7	0.3	TO-99
Low Bias	3527	10	10	0.25 - 0.50	5 - 15	−2 to −5	1	0.6	TO-99
Low Bias	3522	10	10	0.5 - 1	10 - 50	−1 to −10	1	0.6	TO-99
Low Drift	3521	10	10	0.25 - 0.50	1 - 10	−10 to −20	1.5	0.6	TO-99
Low Cost	3542	10	10	20	50	−25	1	0.5	TO-99
Varactor	3430	10	5	Adj. to 0	10 - 30	±0.01	2kHz	0.4V/msec	Module
	3431	10	5	Adj. to 0	10 - 30	±0.01	2kHz	0.4V/msec	Module
HIGH VOLTAGE									
FET	3584	65 - 145	15	3	25	−20	7	150	TO-3
	3583	40 - 140	75	3	25	−20	5	30	TO-3
	3580	10 - 145	15 - 60	3 - 10	25 - 30	−20 to −50	5	15 - 20	TO-3
HIGH CURRENT									
High Power	OPA501	32	10A	5 - 10	40 - 65	20 - 40nA	1	1.5	TO-3
FET	3573	20	2A	10	65	40nA	1	1.5	TO-3
	3572	30	2A	2	40	−100	0.5	3	TO-3
	3571	30	1A	2	40	−100	0.5	3	TO-3
Buffer	3553	10	200	50	300	−200	32	2000	TO-3
	3329	10	100	50	—	Bipolar	1	63	DIP

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OPERATIONAL AMPLIFIERS [cont]

WIDEBAND										
		Rated Output		Offset Voltage		Frequency Response		ts	Com-	
				at 25°C	Temp. Drift	A - BW	Slew Rate	±0.1%	pensa-	
Description	Model	±V	±mA	mV	μV/°C	MHz	V/μsec	nsec	tion	Package
−55° to +200°C	OPA12HT	10	10	10	30	20, A = 10	80	200	int.	TO-99
Fast Settling	OPA605	10	30	0.5 - 1.0	5 - 25	200, A = 1000	300	500	ext.	DIP
Differential	3554	10	100	1 - 2	15 - 50	1000, A = 1000	1000	120	ext.	TO-3
	3551	10	10	1	50	50, A = 10	250	400	ext.	TO-99
	3550	10	10	1	50	10 - 20, A = 1	65 - 100	400	int.	TO-99
	3508	10	10	5	30	100, A = 100	20	—	ext.	TO-99
	3507	10	10	10	30	20, A = 10	80	200	ext.	TO-99
Buffer	3553	10	200	50	300	32(1)	2000	—	—	TO-3

(1) Full power bandwidth

INSTRUMENTATION AMPLIFIERS

LOW DRIFT								
		Gain			Input Parameters			
			Non-Linearity	Rated Output	CMR, DC to 60Hz, G = 10	Offset Voltage vs. Temp.	Dynamic Response G = 100	
Description	Model	Range (V/V)	G = 100, max	V/mA	1kΩ Unbal.	max (μV/°C)	±3dB, BW	Package
Monolithic, Low Cost Very High Accuracy	INA101	1 - 1000	±0.003%	±10/±5	96dB, min	±0.25 ±10/G	25kHz	TO-100, DIP
Low Drift,	3636	5 - 1000	±0.04%	±10/±5	80dB, min.	±(1 + 5/G)	14kHz	DIP
Low Cost	3629	5 - 1000	±0.004%	±10/±10	90dB, min.	±(0.75 + 5/G)	30kHz	DIP
General Purpose,	3660	1 - 1000	±0.03%	±10/±10	90dB, min.	±(2 + 500/G)	72kHz	TO-100
Low Cost	3662	1 - 1000	±0.05%	±10/±10	84dB, min.	±(2 + 400/G)	74kHz	DIP
Buffer, Unity Gain, Differential	3627	1 (fixed)	±0.001% G = 1	±10/±5	100dB, min.	20	800kHz G = 1	TO-99
Very High Accuracy	3630	1 - 1000	±0.003%	±10/±5	96dB, min.	±(0.25 + 10/G)	25kHz	DIP
PROGRAMMABLE GAIN								
Digitally Controlled (4-Bit TTL Input)	3606(1)	1 - 1024 (11 Gains)	0.004%	±10/±5	100dB, min.	±(1 + 20/G)	40kHz	DIP
Digitally Controlled Programmable Gain Multiplexed Input	PGA100	1 - 128 (8 Gains)	±0.005%	±10/±2	—	±6	50kHz	DIP

4 to 20mA TRANSMITTER

Description	Model	Input V	Non-Linearity, max	Output	Input CMRR	Input V_{OS} vs Temp	Input V_{OS}	Package
Precision Self-Powered Two-Wire Transmitter	XTR100	0 - 1	0.01%	4 - 20mA	90dB min.	±0.5μV/°C	±25μV	DIP

(1) 3606 offers software gain control with "G" set by 4-bit TTL inputs.

ISOLATION AMPLIFIERS

TRANSFORMER COUPLED AMPLIFIERS														
		Input Voltage		Input Impedance		Isolation Voltage		Isolation Mode Rejection, min.		Leakage Current at 240VAC	Gain Nonlinearity		±3dB Freq.	External Isolation Power Required	
Description	Model	Common Mode (V)	Differential (V)	Common Mode (Ω)	Differential (Ω)	Continuous (V) Peak	Pulse/Test (V) Peak	DC (dB)	60Hz (dB)	(μA)	Max (%)	Typ (%)	(kHz)		Package
Low Drift, Bipolar	3450	±10	±15	5×10^9	10^7	±500	±2000	160	120	2.5	±0.005	±0.0015	1.5	No	Module
Low Bias, FET	3451	±10	±15	10^{11}	10^{11}	±500	±2000	160	120	2.5	±0.025	±0.005	2.5	No	Module
	3452	±10	±15	10^{11}	10^{11}	±2000 (2)	±5000 (2)	160	120	2.5	±0.025	±0.005	2.5	No(1)	Module
	3455	±10	±15	10^{11}	10^{11}			160	120	2	±0.025	±0.005	2.5	No(1)	Module
True 3-wire Inst. Amp.	3456	±10	±20	5×10^9	10^7	±2000	±5000	160	130	2.5	±0.02	±0.01	2.5	No(1)	Module
IC with Power Supply	3656	±8	±8	10^8	10^8	±3500	±8000	160	125	1	±0.05 to ±0.15	±0.03	30	No(1)	DIP

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ISOLATION AMPLIFIERS [cont]

OPTICALLY COUPLED AMPLIFIERS															
		Input Voltage		Input Impedance		Isolation Voltage		Isolation Mode Rejection, min.		Leakage Current at 240VAC	Gain Nonlinearity				
Description	Model	Common Mode (V)	Differential (V)	Common Mode (Ω)	Differential (Ω)	Continuous (V) Peak	Pulse/Test (V) Peak	DC (dB)	60Hz (dB)	(μA)	Max (%)	Typ (%)	±3dB Freq. (kHz)	External Isolation Power Required	Package
Miniature Low Cost	ISO100	Current Input: ±10μA or 0 - 20 μA				±750	±2500	5pA/V	400pA/V	0.3	0.07	0.02	60	Yes[4]	DIP
Balanced Current Input	3650	±10	±15	10^9	25[3]	±2000	±5000	140	120	0.35	±0.05 to ±0.2	±0.02 to ±0.05	15	Yes[4]	DIP
Balanced FET Input	3652	±10	[5]	10^{11}	10^{11}	±2000	±5000	140	120	0.35	±0.1 to ±0.2	±0.05	15	Yes[4]	DIP

NOTES: (1) Isolated power available to power external circuitry. (2) Isolation voltage tested at both ±5000Vp pulse test and 2500V, rms, 60Hz; leakage current is 2μA max, at 240V, rms, 60Hz. (3) 3650 is a current input device: to reduce input errors, very low input impedance is desirable. (4) Models 722 or 724 isolated DC/DC converters may be used to provide isolated power. (5) Protected up to ±6000V.

VOLTAGE REFERENCE

Description	Model	Output (V)	Minimum Output (mA)	Maximum Drift (ppm/°C)	Power Supply (V)	Power Supply (mA)	Package
Precision	REF101	+10.000 ±0.005	10	1 - 6	+13.5 to +35	4.5	TO-99

ANALOG CIRCUIT FUNCTIONS

MULTIPLIER/DIVIDERS			
Model	Accuracy at 25°C, max, No Trimming Required	Specification Temp. Range (°C)	Package
4214	0.50 - 1%	−25 to +85, −55 to +125	DIP
4203/05	1 - 2%	0 to +70, −55 to +125	TO-100
4204	0.25 - 0.50%	−25 to +85, −55 to +125	DIP
4206	0.25% - 0.50%	0 to +70	DIP
4213	0.50 - 1%	−25 to +85, −55 to +125	TO-100

SPECIAL FUNCTIONS			
Description	Model	Comments	Package
Logarithmic Amplifier	4127	0.50 - 1% accuracy, 2 current or 2 voltage input signals	DIP
Log Ratio Amplifier	LOG100	0.1% - 0.37% accuracy, 2 current input log ratio function	DIP
Divider	DIV100	E_O = 10 N/D, ±0.25 - 1% untrimmed accuracy	DIP
Multifunction Converters	4301	$E_o = V_y(V_z/V_x)^m$, hermetically sealed metal package, compatible with 4302	DIP
Multiply, divide, square root, etc.	4302	$E_o = V_y(V_z/V_x)^m$, plastic package	
Peak Detector	4085	Provide read-out of DC voltage equal to peak value of complex wave form	DIP
RMS-to-DC Converters	4340 4341	Laser-trimmed, no external trimming, metal package, pin compatible with 4341 Externally trimmed, low cost in plastic package	DIP DIP
Oscillators	4023/25 4423	Fixed-frequency (10Hz to 20kHz) Very-low cost, RC programmable, 0.002Hz to 20kHz	Module DIP
Comparators	4115/04 4082/03	Provides window or dual limit for comparison Drives lamps, relays or logic loads	Module Module
Fixed-Frequency Active Filters	ATF76 Series	Pre-tuned, multiple pole bandpass, low-pass, and notch filters	Module
Universal Active Filters	UAF11/21/31/41	Variable type, 4-resistor, programmable, 2-pole filters; Q and F_o can be programmed; 3 outputs provide low-pass, high-pass and bandpass transfer functions; complex filter response by cascading.	DIP

FOR ADDITIONAL DETAILS REFER TO THE BURR-BROWN PRODUCT DATA BOOK OR CONTACT YOUR NEAREST BURR-BROWN SALES OFFICE.

BURR-BROWN®

MILITARY PRODUCTS

Burr-Brown's Military products meet the demand for high quality products for high reliability applications. They feature exceptional electrical performance from −55°C to +125°C, Hi-Rel manufacture, MIL-STD-883 class B screening, and reasonable prices. They are designed to conservative and stringent MIL-M-38510 requirements, and are produced on a separate manufacturing line, which exceeds Burr-Brown's standard lines' quality. MIL-M-38510 and MIL-STD-883 processes and controls are used throughout.

ANALOG-TO-DIGITAL CONVERTERS

Model	Resolution Bits	Linearity ±LSB, max	Conversion Time μsec, max	Gain Drift ±ppm/°C, max	Input Range V	Package
ADC87/MIL, /883B ADC87U/883B, U	12	1/2	8	15	±2.5, ±5, ±10, 0 to +5, 0 to +10	32-pin DIP

DIGITAL-TO-ANALOG CONVERTERS

Model	Resolution Bits	Linearity ±LSB, max	Monotonicity	Gain Drift ±ppm/°C, max	Settling Time max	Output Ranges	Package
DAC87-CBI-V/MIL, -CBI-V/B, -CBI-V	12	1/2	−55°C/+125°C	20	7μsec	±2.5, ±5, ±10, +5, +10V	24-pin DIP
DAC87U-CBI-V/B, -CBI-V	12	1/2	−25°C/+85°C	20	7μsec		24-pin DIP
DAC87-CBI-I/B	12	1/2	−55°C/+125°C	20	400nsec	0 to −2mA ±1mA	24-pin DIP
DAC87-CBI-I	12	1/2	−55°C/+125°C	20	400nsec		24-pin DIP
DAC87U-CBI-I/B	12	1/2	−25°C/+85°C	20	400nsec		24-pin DIP
DAC87U-CBI-I	12	1/2	−25°C/+85°C	20	400nsec		24-pin DIP
DAC870V/MIL, /883B, /(none)	12	1/2	−55°C/+125°C	25	7μsec	±2.5, ±5, ±10, +5, +10V	24-pin DIP
DAC870U/883B, (none)	12	1/2	−25°C/+85°C	20	7μsec		24-pin DIP
DAC870VL/MIL, 883B, /(none)	12	1/2	−55°C/+125°C	25	7μsec		28-terminal LCC
DAC870UL/883B, /(none)	12	1/2	−25°C/+85°C	20	7μsec		28-terminal LCC
8300201XC*	12	1/2	−55°C/+125°C	20	7μsec	±2.5, ±5, ±10, +5, +10V	24-pin DIP

* DESC Drawing 83002 to DAC87-CBI-V/MIL.

MULTIPLIERS

Model	Accuracy at 25°C ±%, max	Accuracy at 125°C ±%, max	Feedthrough ±mV, max	Output Offset ±mV, max	Output V, mA, min	Package
4213WM/883B, WM	1/2	4	50	25	±10, ±5	TO-100
4213VM/MIL, VM/883B, VM	1	4	100	30	±10, ±5	TO-100
4213UM/883B, UM	1	2(1)	100	50	±10, ±5	TO-100

VOLTAGE-TO-FREQUENCY CONVERTERS

Model	V_{IN} Range V	F_{OUT} Range kHz, max	Linearity % FSR, max	Full Scale Drift ppm FSR/°C, max	Package
VFC32WM/883B, WM	±10	200	±0.006 at 10kHz	±100 at 10kHz	TO-100
VFC32VM/MIL, VM/883B, VM	±10	200	±0.01 at 10kHz	−400, +150 at 200kHz	TO-100
VFC32UM/883B, UM	±10	200	±0.01 at 10kHz	±150 at 10kHz	TO-100

OPERATIONAL AMPLIFIERS

Description	Model	Offset Voltage at 25°C ±mV, max	Offset Voltage drift ±μV/°C max	Bias Current nA, max	Bandwidth Unity Gain MHz, min	Slew Rate V/μs, min	ts ±0.01% ns	Compensation	V, mA, min	Package
Wideband	OPA600VM/MIL, VM/883B, VM	2	20	−100pA	5000(2), A = 1000	400	125	external	±10, ±200	16-pin DIP
	OPA600UM/883B, UM	5	80	−100pA	5000(2), A = 1000	400	150	external	±10, ±200	16-pin DIP
General Purpose Bipolar	3500R/MIL, /883B	5	20	±30	1	0.6	—	internal	±10, ±10	TO-99
	3500U/883B	5	20(3)	±30	1	0.6	—	internal	±10, ±10	TO-99
Precision Bipolar	3510VM/MIL, /883B	0.12	2	±25	0.25	0.5	—	internal	±10, ±10	TO-99
Low Drift, Low Bias	OPA105WM/MIL, WM/883B, WM	.250	2	−1pA	1	0.9	—	internal	±10, ±10	TO-99
	OPA105VM/MIL, VM/883B, VM	.250	5	−1pA	1	0.9	—	internal	±10, ±10	TO-99
	OPA105UM/883B, UM	.250	15(3)	−1pA	1	0.9	—	internal	±10, ±10	TO-99
Ultra Low Bias	OPA106WM/MIL, WM/883B, WM	.250	5	−100fA	1	1.2	—	internal	±10, ±5	TO-99
	OPA106VM/MIL, VM/883B, VM	.250	10	−150fA	1	1.2	—	internal	±10, ±5	TO-99
	OPA106UM/883B, UM	.250	20(3)	−300fA	1	1.2	—	internal	±10, ±5	TO-99

NOTES: (1) At +85°C. (2) Gain-bandwidth product. (3) −25°C to +85°C.

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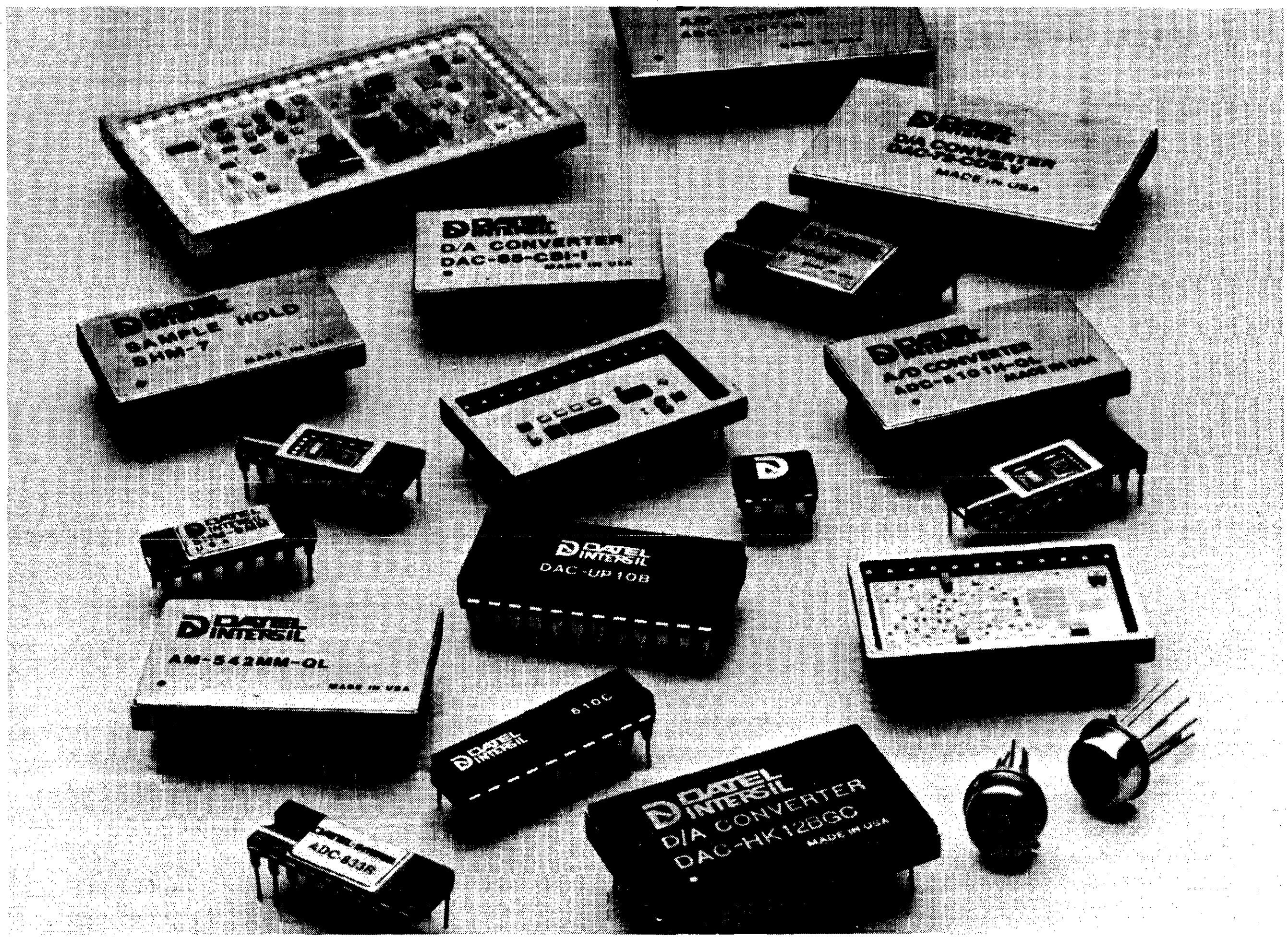
DATEL

Data Conversion Products

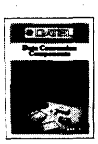


Datel is located in Mansfield, Massachusetts, approximately 35 miles from Boston. The modern, 120,000-square-foot facility houses our administrative offices, our components and systems engineering groups, modular and systems production facilities, and the most modern thin-film-hybrid production facility in the industry.

Datel offers one of the broadest lines of data-conversion products in the industry. Included are A/D and D/A converters, sample-and-holds, operational and instrumentation amplifiers, and data-acquisition systems — all packaged using the latest in thin-film, hybrid-microelectronic-circuit manufacturing technologies.

Datel also offers fast delivery. On standard products, delivery typically runs from stock to four weeks and from six to eight weeks for full military-grade products with Class 883B screening.

Datel is dedicated to maintaining its position as an international leader in data-conversion technology. You can depend on Datel-Intersil for a steady flow of new products to meet the growing demand for high-performance data-acquisition products.



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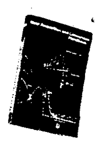

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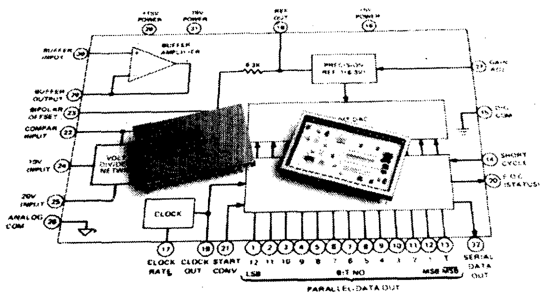
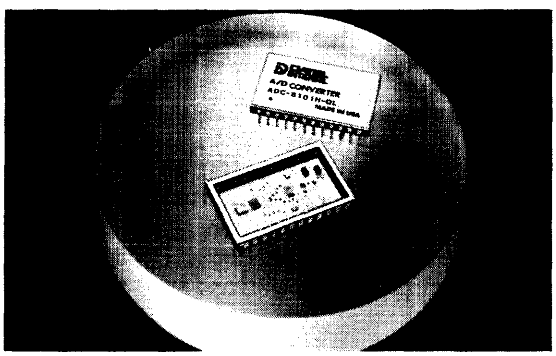
New Products from Datel



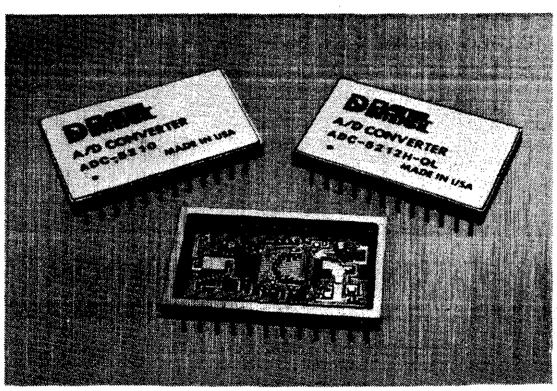
ADC-810, ADC-811
Ultra-fast, 12-bit Hybrid Analog to Digital Converters

The ADC-810 and ADC-811 are ultra-fast, hybrid, successive approximation, 12-bit analog to digital converters. The ADC-810 achieves a maximum conversion time of 2 μsec. Conversion time for the ADC-811 is 4 μsec maximum, which is the only difference between the two. Both models are pin-compatible with industry-standard ADC-85/87 converters, offering increased speed, high accuracy and reliability. Models are available subjected to 100% screening to MIL-STD-883B.



ADC-5101 high speed, 8-bit A/D offers high temperature operation at low cost

The ADC-5101 is a high speed, adjustment-free, 8-bit A/D converter. Pin compatible with standard ADC-5101 converters, these devices offer high accuracy and high speed over the full military operating temperature range of −55°C to +125°C. Designed for operation without external adjustment circuits, the ADC-5101 accomplishes an 8-bit conversion in only 900 ns maximum. Models are available subjected to 100% screening to MIL-STD-883 Class B.



ADC-5210 series adjustment-free 12-bit A/D features high accuracy over military temperature range

The ADC-5210 series are high performance, 12-bit successive approximation A/D converters. Completely pin and function compatible with standard ADC-5210 devices, these models offer significatly improved high-temperature operation at lower cost. Full scale absolute accuracy error is a maximum of ± 0.05% FSR at + 25°C and only ± 0.2% FSR over the full military operating temperature range of −55°C to + 125°C; an improvement of 10 LSBs over the error specified on competing devices. MIL-STD-883 screening is available.

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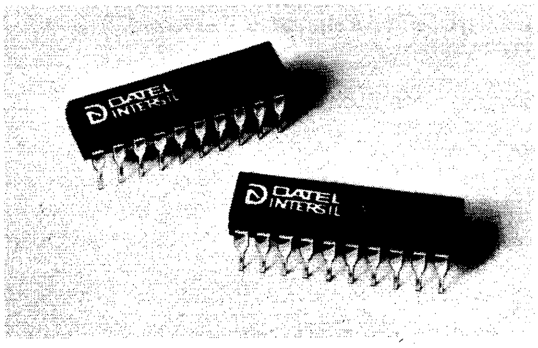
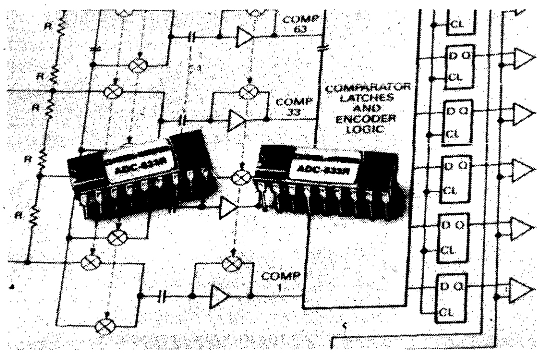


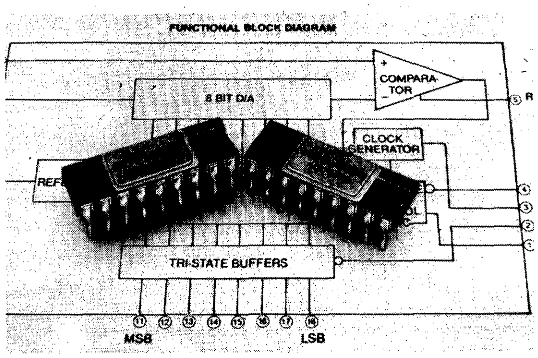
ADC-830 microprocessor compatible 8-bit A/D converter

DATEL's ADC-830 is a low-cost, monolithic 8-bit A/D converter designed to operate directly with the 8080A control bus via three-state outputs. The device appears as a memory location or I/O port to the microprocessor and thus does not require interfacing logic. Using the successive approximation technique and a modified potentiometric resistor ladder, the ADC-830 achieves an 8-bit conversion in 100 μs with a maximum total adjusted error of only ± ½ LSB. Its combination of low cost, small size, and interface versatility make the ADC-830 an ideal choice for many process control and instrumentation applications.



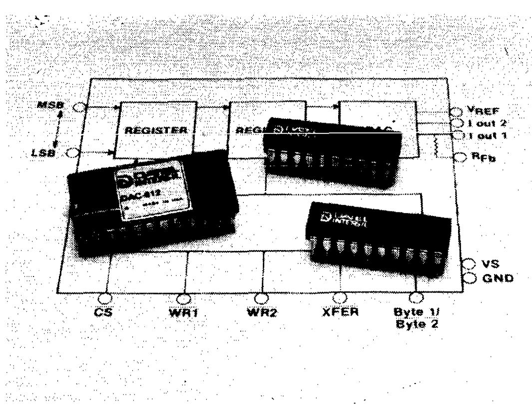
ADC-833 6-bit A/D features video speed at low power

The ADC-833 is a low-power, video-speed, 6-bit flash A/D manufactured with CMOS/SOS technology. The device is capable of digitizing an analog input signal at conversion rates up to 15MHz while its power consumption is only 200mW. The analog input voltage range is +2.5V to +10V, and typical differential linearity error is only ± ½ LSB. Outputs are buffered three-state and include an overflow output which allows the user to cascade two units to achieve 7-bit resolution.



ADC-847 Microprocessor Compatible, 8-Bit A/D Converter

The ADC-847 is a low cost, monolithic, 8-bit A/D converter designed to interface directly to a microprocessor via three-state outputs. Utilizing the successive approximation technique, the ADC-847 completes an 8-bit conversion in 9 μS with a maximum linearity error as low as ± ¼ LSB. The ADC-847 includes, an internal clock generator, reference circuit, successive approximation register, comparator, three-state buffers, 8 bit D/A converter and interface and control logic, making it an ideal choice for many process control and instrumentation applications. The ADC-847 is available for operation over the commercial, 0°C to + 70°C and military, –55°C to + 125°C temperature ranges and is packaged in either an 18 pin plastic or ceramic DIP.



DAC-608/610/612 Low Cost, Double-Buffered Microprocessor Compatible D/A Converters

The DAC-608, DAC-610 and DAC-612 are low cost monolithic 8, 10 and 12 bit multiplying D/A converters, designed to interface directly with most popular microprocessors. Double-Buffered inputs allow the converters to output an analog voltage corresponding to one digital word while holding the next. The converters consist of an input register, a D/A register, control logic and D/A converter. Settling time is 1 μS for the DAC-608 and DAC-612 and 500 nS for the DAC-610. The reference input of these converters is selectable over a range of ±10V and may also be used as the analog input for four quadrant multiplication applications.

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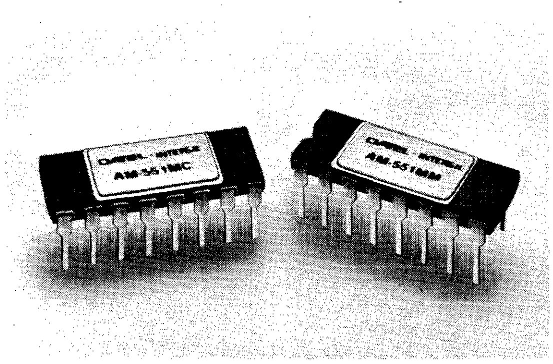
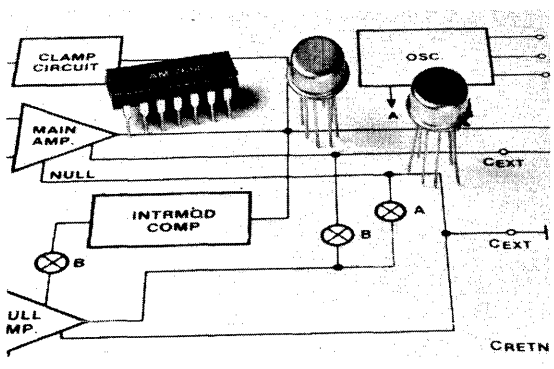


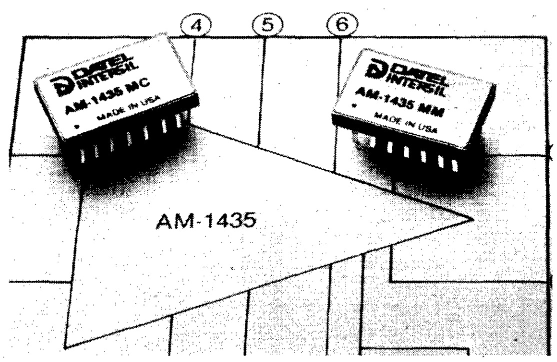
AM-551 Low Cost, Hybrid Programmable Instrumentation Amplifier

DATEL's AM-551 is a low cost, high performance, programmable gain nstrumentation amplifier manufactured with hybrid thin-film technology. Gain range is 1 to 1000 and is set externally by a single resistor and simple pin-strapping. Settling time is 2 μsec for a 20V output step to 0.01% accuracy, with a slew rate of 23V/μsec and a small signal bandwidth of 400 kHz. Applications include remote amplification of low-level signals produced by thermocouples, strain gages and RTD's, high performance data acquisition systems and remote instrumentation systems.



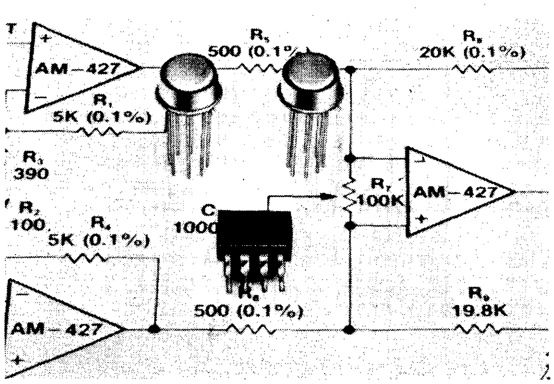
AM-7650 new, low cost chopper stabilized operational amplifier features ultra-low offcost voltage and drift

DATEL's AM-7650 is a low cost, high performance chopper stabilized amplifier featuring exceptionally low offset voltage and input bias specifications combined with excellent bandwidth and speed characteristics. Input offset voltage is typically ± 0.7 μV with an input offset voltage drift as low as 0.01 μV/°C. The AM-7650 achieves its low offset by comparing the inverting and non-inverting input voltages in a nulling amplifier, which is nulled by alternate clock phases from the internal clock oscillator. The 14 pin DIP version also includes a provision for the use of an external clock if an application requires. These devices are internally compensated for unity-gain operation.



AM-1435 Ultra High Speed, Wideband, Hybrid Operational Amplifier

DATEL's AM-1435 is an ultra-fast settling, wide-band operational amplifier. The AM-1435 achieves a settling time of only 70 nsec for a 10V step to 0.01% accuracy. High speed performance is optimized with high open loop gain, flat frequency response beyond 10 kHz and a roll-off of 6 dB/octave to beyond 100 MHz. Gain bandwidth product is typically 1GHz and slew rate is 300V/μsec. All models are packaged in hermetically sealed ceramic cases, with full screening to MIL-STD-883 level B available.



AM-427 Ultra-Low Noise Monolithic Operational Amplifier

The AM-427 is a low cost, ultra-low noise operational amplifier which is designed for instrumentation grade signal conditioning where low noise, low offset voltage and low offset voltage drift are required. The AM-427 combines exceptional DC performance with ultra-low noise operation. Maximum input noise voltage density and input noise current density at 10 HZ are 5.5 nV/√Hz and 0.4 pA/√Hz respectively. The AM-427 is available for operation over the industrial, −25°C to +85°C and military, −55°C to +125°C temperature ranges and is packaged in either an 8 pin TO-99 or an 8 pin ceramic DIP.

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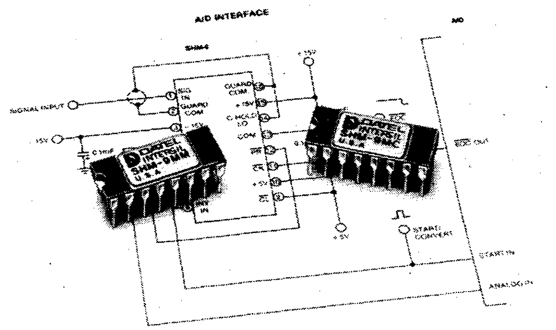
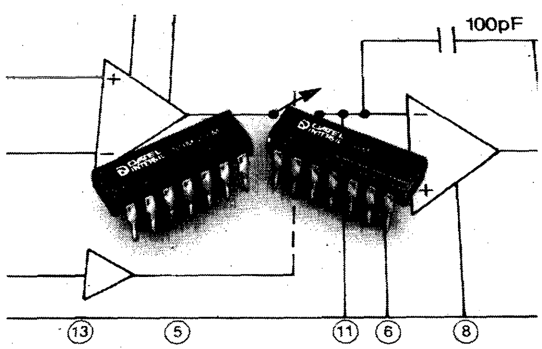


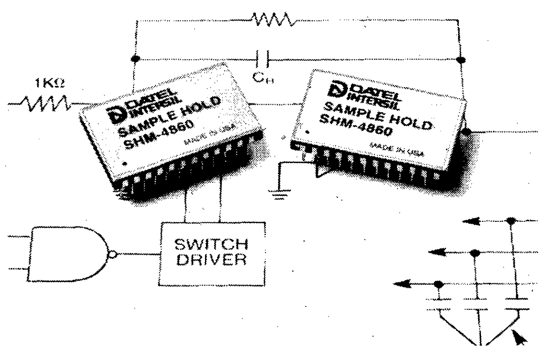
Low cost functionally complete hybrid sample-hold features .01% accuracy SHM-9

The SHM-9 is a complete, self-contained sample-hold amplifier that combines high performance versatility with low cost. The SHM-9 includes a bipolar input amplifier, a low-leakage electronic switch, a FET output amplifier, a precision 1000 pF hold capacitor and logic control circuitry. The internal control circuitry allows the SHM-9 to be interfaced with virtually any A/D converter using the converter's Start/Convert and E.O.C. (status) signals. Active laser trimming of highly stable thin-film resistor networks minimizes offset and sample-to-hold offset errors, eliminating the need for external adjustment circuits.



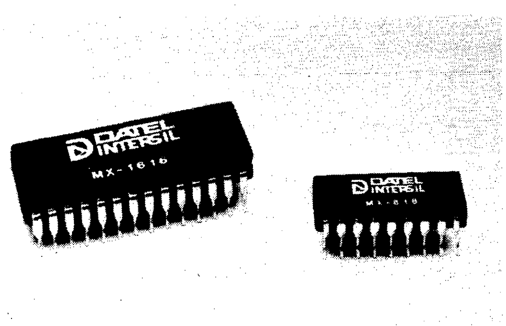
SHM-20, Fast, High Performance Sample and Hold Features Internal Hold Capacitor.

The SHM-20 is a complete monolithic sample and hold amplifier which includes an internal 100 pF MOS capacitor. Features include an acquisition time of typically 1.0 µS for a 10V input step to 0.01%. Aperture uncertainty is typically 1 nS and droop rate is as low as 0.08 µV/µS. Primarily designed for high speed analog signal processing applications, the SHM-20 combines monolithic reliability and size with high performance versatility and low cost. The SHM-20 is available for operation over the commercial, 0°C to +70°C and military, −55°C to +125°C temperature ranges and is packaged in a 14 pin ceramic DIP.



SHM-4860 new 0.01% Hybrid Sample-Hold features 200 nsec acquisition time

DATEL's SHM-4860 is a high-speed, high resolution sample-hold amplifier manufactured with modern hybrid technology. Designed mainly for precision, high speed analog signal processing applications, the SHM-4860 acquires a 10V input change to ±0.01% in only 200 nsec max. Maximum sample-to-hold settling time is 100 nsec to ±0.01% with an aperture uncertainty of typically ±50 psec. Feedthrough attenuation is typically 74 dB. The digital inputs of the SHM-4860 are TTL compatible.



8 and 16 Channel Multiplexers Feature High Speed, High Accuracy, MX-1616, MX-818

DATEL's MX-1616 and MX-818 are high speed, high performance analog multiplexers featuring transfer accuracies of 0.01% at sampling rates of up to 2.5 MHz over ±10V single ranges. The MX-1616 is user programmable either as a single-ended 16-channel or as a differential 8 channel multiplexer while the MX-818 is programmable as either a single-ended 8 channel or differential 4-channel multiplexer. All models feature an inhibit function, break-before-make switching and a maximum ON resistance of only 750Ω.

Hybrid military products

Datel is a recognized industry leader in the design and manufacture of thin film hybrid data conversion products which meet the most demanding reliability requirements for military and aerospace applications per MIL-specifications. Datel data conversion products are currently used in a wide number of military and aerospace flight systems and in high reliability ground support and test systems. Datel's modern 120,000 square foot manufacturing facility in Mansfield, Massachusetts includes the most automated and advanced manufacturing, test and calibration equipment available in the industry. This capability, supported by a Quality Assurance Program with full emphasis on product quality assurance and reliability, provides an experienced and reliable source for data converter products to the screening and qualification requirements of Methods 5004, 5005, and 5008 of MIL-STD-883B in compliance with MIL-M-38510 (specified by Datel as "Q.L." devices).

The Quality Assurance operation at Datel monitors all areas of manufacturing and test, controls manufacturing and screening standards, maintains lot traceability procedures, and sets material standards to assure product quality. All purchased and internally manufactured components are procured or manufactured to precise specification control drawings. All components are 100% electrically tested and 100% visually inspected either by the vendors or internally within Datel facilities. Assembly and test processes and work stations are carefully monitored by Quality Assurance using fully documented procedures to guarantee high standards of workmanship and quality in all of Datel's products.

Datel products with the suffix "Q.L." are fully screened in accordance with Methods 5004 and 5008 of MIL-STD-883B as amended by MIL-M-38510. The following list briefly summarizes Datel's hybrid military products.

ANALOG TO DIGITAL CONVERTERS

	MODEL NO.	RESOLUTION	CONVERSION TIME	LINEARITY	OPERATING TEMP. RANGE (°C)
	ADC-HC12BMM	12 bits	300 μsec	± ½ LSB	−55 to +125
	ADC-HC12BMM-QL	12 bits	300 μsec	± ½ LSB	−55 to +125
	ADC-HS12BMM	12 bits	9 μsec	± ½ LSB	−55 to +125
	ADC-HS12BMM-QL	12 bits	9 μsec	± ½ LSB	−55 to +100
	ADC-HX12BMM	12 bits	20 μsec	± ½ LSB	−55 to +100
	ADC-HX12BMM-QL	12 bits	20 μsec	± ½ LSB	−55 to +100
	ADC-HZ12BMM	12 bits	8 μsec	± ½ LSB	−55 to +100
	ADC-HZ12BMM-QL	12 bits	8 μsec	± ½ LSB	−55 to +100
	ADC-810MM	12 bits	2 μsec	± ½ LSB	−55 to +125
	ADC-810MM-QL	12 bits	2 μsec	± ½ LSB	−55 to +125
NEW	ADC-811MM	12 bits	4 μsec	± ½ LSB	−55 to +125
NEW	ADC-811MM-QL	12 bits	4 μsec	± ½ LSB	−55 to +125
	ADC-815MM	8 bits	700 nsec	± ½ LSB	−55 to +125
	ADC-815MM-QL	8 bits	700 nsec	± ½ LSB	−55 to +125
	ADC-816MM	10 bits	800 nsec	± ½ LSB	−55 to +125
	ADC-816MM-QL	10 bits	800 nsec	± ½ LSB	−55 to +125
	ADC-817MM	12 bits	2 μsec	± ½ LSB	−55 to +125
	ADC-817MM-QL	12 bits	2 μsec	± ½ LSB	−55 to +125
	ADC-825MM	8 bits	1 μsec	± ½ LSB	−55 to +125
	ADC-825MM-QL	8 bits	1 μsec	± ½ LSB	−55 to +125
	ADC-826MM	10 bits	1.4 μsec	± ½ LSB	−55 to +125
	ADC-826MM-QL	10 bits	1.4 μsec	± ½ LSB	−55 to +125
	ADC-827MM	12 bits	3 μsec	± ½ LSB	−55 to +125
	ADC-827MM-QL	12 bits	3 μsec	± ½ LSB	−55 to +125
	ADC-5101H	8 bits	900 nsec	± ½ LSB	−55 to +125
	ADC-5101H-QL	8 bits	900 nsec	± ½ LSB	−55 to +125
	ADC-5210H	12 bits	13 μsec	± ½ LSB	−55 to +125
	ADC-5210H-QL	12 bits	13 μsec	± ½ LSB	−55 to +125
	ADC-5211H	12 bits	13 μsec	± ½ LSB	−55 to +125
	ADC-5211H-QL	12 bits	13 μsec	± ½ LSB	−55 to +125
	ADC-5212H	12 bits	13 μsec	± ½ LSB	−55 to +125
	ADC-5212H-QL	12 bits	13 μsec	± ½ LSB	−55 to +125
	ADC-5213H	12 bits	13 μsec	± ½ LSB	−55 to +125
	ADC-5213H-QL	12 bits	13 μsec	± ½ LSB	−55 to +125
	ADC-5214H	12 bits	13 μsec	± ½ LSB	−55 to +125
	ADC-5214H-QL	12 bits	13 μsec	± ½ LSB	−55 to +125
	ADC-5215H	12 bits	13 μsec	± ½ LSB	−55 to +125
	ADC-5215H-QL	12 bits	13 μsec	± ½ LSB	−55 to +125
	ADC-5216H	12 bits	13 μsec	± ½ LSB	−55 to +125
	ADC-5216H-QL	12 bits	13 μsec	± ½ LSB	−55 to +125

DIGITAL-TO-ANALOG CONVERTERS

MODEL NO.	RESOLUTION	OUTPUT SETTLING TIME	LINEARITY	OPERATING TEMP. RANGE (°C)
DAC-HA10BM	10 bits	1.3 μsec	± ½ LSB	−55 to +125
DAC-HA10BM-QL	10 bits	1.3 μsec	± ½ LSB	−55 to +125
DAC-HA12BM	12 bits	5 μsec	± ½ LSB	−55 to +125
DAC-HA12BM-QL	12 bits	5 μsec	± ½ LSB	−55 to +125
DAC-HA14BM	14 bits	7 μsec	± 1 LSB	−55 to +125
DAC-HA14BM-QL	14 bits	7 μsec	± 1 LSB	−55 to +125
DAC-HF8BMM	8 bits	25 nsec	± ½ LSB	−55 to +125
DAC-HF8BMM-QL	8 bits	25 nsec	± ½ LSB	−55 to +125
DAC-HF10BMM	10 bits	25 nsec	± ½ LSB	−55 to +125
DAC-HF10BMM-QL	10 bits	25 nsec	± ½ LSB	−55 to +125

DATEL 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

SAMPLE-HOLD AMPLIFIERS

	MODEL NO.	ACCURACY	ACQUISITION TIME	HOLD-MODE DROOP	OPERATING TEMP. RANGE (°C)
	SHM-IC-1	0.01%	5 μsec	50μV/msec	0 to + 70
	SHM-IC-1M	0.01%	5 μsec	50μV/msec	−55 to + 125
	SHM-LM-2	0.01%	6 μsec	200μV/msec	0 to + 70
	SHM-LM-2M	0.01%	6 μsec	200μV/msec	−55 to + 125
	SHM-HUMC	0.1%	25 nsec	50μV/μsec	0 to + 70
	SHM-HUMR	0.1%	25 nsec	50μV/μsec	−25 to + 85
	SHM-6MC	0.01%	1 μsec	10μV/μsec	0 to + 70
	SHM-6MR	0.01%	1 μsec	10μV/μsec	−25 to + 85
	SHM-7MC	0.1%	40 nsec	100μV/μsec	0 to + 70
	SHM-7MR	0.1%	40 nsec	100μV/μsec	−25 to + 85
NEW	SHM-9MC	0.01%	6 μsec	0.2 mV/mS	0 to + 70
NEW	SHM-9MR	0.01%	6 μsec	0.2 mV/mS	−25 to + 85
NEW	SHM-20C	0.01%	1 μsec	0.08 μV/μS	0 to + 70
NEW	SHM-20M	0.01%	1 μsec	0.08 μV/μS	−55 to + 125
NEW	SHM-486OMC	0.01%	200 nsec	0.5 μV/μS	0 to + 70
NEW	SHM-486OMR	0.01%	200 nsec	0.5 μV/μS	−25 to + 85

ANALOG MULTIPLEXERS

MODEL NO.	INPUT CHANNELS	ACCESS TIME	CHANNEL ON RESISTANCE	OPERATING TEMP. RANGE (°C)
MV-808	8 Single-Ended	350 nsec	250Ω	0 to + 70
MV-808M	8 Single-Ended	350 nsec	250Ω	−55 to + 125
MV-1606	16 Single-Ended	300 nsec	270Ω	0 to + 70
MV-1606M	16 Single-Ended	300 nsec	270Ω	−55 to + 125
MVD-409	4 Differential	350 nsec	250Ω	0 to + 70
MVD-409M	4 Differential	350 nsec	250Ω	−55 to + 125
MVD-807	8 Differential	300 nsec	270Ω	0 to + 70
MVD-807M	8 Differential	300 nsec	270Ω	−55 to + 125
MX-808	8 Single-Ended	500 nsec	1.5kΩ	0 to + 70
MX-808M	8 Single-Ended	500 nsec	1.5kΩ	−55 to + 125
MX-818C	8 Single-Ended or 4 Differential	125 nsec	750Ω	0 to + 70
MX-818M	8 Single-Ended or 4 Differential	125 nsec	750Ω	−55 to + 125
MX-1606	16 Single-Ended	500 nsec	1.5kΩ	0 to + 70
MX-1606M	16 Single-Ended	500 nsec	1.5kΩ	−55 to + 125
MX-1616C	16 Single-Ended 8 Differential	150 nsec	750Ω	0 to + 70
MX-1616M	16 Single-Ended 8 Differential	150 nsec	750Ω	−55 to + 125
MXD-409	4 Diffential	500 nsec	1.5kΩ	0 to + 70
MXD-409M	4 Differential	500 nsec	1.5kΩ	−55 to + 125
MXD-807	8 Differential	500 nsec	1.5kΩ	0 to + 70
MXD-807M	8 Differential	500 nsec	1.5kΩ	−55 to + 125

OPERATIONAL AMPLIFIERS

MODEL NO.	INPUT OFFSET VOLTAGE	GAIN BANDWIDTH	OUTPUT	OPERATING TEMP. RANGE (°C)
AM-410-2C	1.5 mV	18 MHz	± 11V @ 8 mA	0 to + 70
AM-410-2M	1 mV	18 MHz	± 12V @ 10 mA	−55 to + 125
AM-411-2C	1.5 mV	50 MHz	± 11V @ 8 mA	0 to + 70
AM-411-2M	1 mV	60 MHz	± 12V @ 10 mA	−55 to + 125
AM-427-A	100 μV	5 MHz	± 11V @ 18 mA	−25 to + 85
AM-427-B	25 μV	5 MHz	± 11V @ 18 mA	−25 to + 85
AM-427-M	100 μV	5 MHz	± 11V @ 18 mA	−55 to + 125
AM-430A	75 μV	2.5 MHz	± 10V @ 18 mA	0 to + 70
AM-430B	25 μV	2.5 MHz	± 10V @ 18 mA	0 to + 70
AM-430M	75 μV	2.5 MHz	± 10V @ 25 mA	−55 to + 125
AM-450-2	4 mV	12 MHz	± 10V @ 10 mA	0 to + 70
AM-450-2M	4 mV	12 MHz	± 10V @ 10 mA	−55 to + 125
AM-452-2	5 mV	20 MHz	± 10V @ 10 mA	0 to + 70
AM-452-2M	5 mV	20 MHz	± 10V @ 10 mA	−55 to + 125
AM-453-2	4 mV	10 MHz	± 12V @ 20 mA	−55 to + 125
AM-453-2M	4 mV	10 MHz	± 12V @ 20 mA	−55 to + 125
AM-460-2	3 mV	12 MHz	± 10V @ 10 mA	0 to + 70
AM-460-2M	3 mV	12 MHz	± 10V @ 10 mA	−55 to + 125
AM-462-2	3 mV	100 MHz	± 10V @ 10 mA	0 to + 70
AM-462-2M	3 mV	100 MHz	± 10V @ 10 mA	−55 to + 125
AM-464-2	6 mV	4 MHz	± 35V @ 10 mA	0 to + 70

DATEL 11 CABOT BOULEVARD, MANSFIELD MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

OPERATIONAL AMPLIFIERS

	MODEL NO.	INPUT OFFSET VOLTAGE	GAIN BANDWIDTH	OUTPUT	OPERATING TEMP. RANGE (°C)
	AM-464-2M	4 mV	4 MHz	± 35V @ 12 mA	−55 to + 125
	AM-470-2C	5 mV	1 MHz	± 12V @ 10 mA	0 to + 70
	AM-470-2M	3 mV	1 MHz	± 12V @ 10 mA	−55 to + 125
	AM-490-2A	20 µV	3 MHz	± 10V @ 7 mA	0 to + 70
	AM-490-2B	20 µV	3 MHz	± 10V @ 7 mA	0 to + 70
	AM-490-2C	20 µV	3 MHz	± 10V @ 7 mA	0 to + 70
	AM-490-2M	20 µV	3 MHz	± 10V @ 7 mA	−55 to + 125
	AM-500GC	3 mV	130 MHz	± 10V @ 50 mA	0 to + 70
	AM-500MC	3 mV	130 MHz	± 10V @ 50 mA	0 to + 70
	AM-500MR	3 mV	130 MHz	± 10V @ 50 mA	−25 to + 85
NEW	AM-1435MC	5 mV	1000 MHz	± 7V @ 14 mA	0 to + 70
NEW	AM-1435MR	5 mV	1000 MHz	± 7V @ 14 mA	−25 to + 85
NEW	AM-7650-1	5 µV	2 MHz	± 4.7V	0 to + 70
NEW	AM-7650-2	5 µV	2 MHz	± 4.7V	0 to + 70

DIGITALLY PROGRAMMABLE INSTRUMENTATION AMPLIFIERS

MODEL NO.	GAIN RANGE	SETTLING TIME	OUTPUT	OPERATING TEMP. RANGE (°C)
AM-542MC	1 to 1024	150 µsec	± 10.5V @ 5 mA	0 to + 70
AM-542MR	1 to 1024	150 µsec	± 10.5V @ 5 mA	−25 to + 85
AM-543MC	1 to 128	6 µsec	± 11V @ 1 mA	0 to + 70
AM-543MR	1 to 128	6 µsec	± 11V @ 1 mA	−25 to + 85

PROGRAMMABLE GAIN INSTRUMENTATION AMPLIFIERS

	MODEL NO.	GAIN RANGE	SETTLING TIME	OUTPUT	OPERATING TEMP. RANGE (°C)
NEW	AM-551MC	1 to 1000	2 µsec	± 11V @ 5 mA	0 to + 70
NEW	AM-551MR	1 to 1000	2 µsec	± 11V @ 5 mA	−25 to + 85
NEW	AM-551MC	1 to 1000	2 µsec	± 11V @ 5 mA	0 to + 70

DATA ACQUISITION SUBSYSTEMS

MODEL NO.	RESOLUTION	INPUT CHANNELS	THROUGHOUT RATE	OPERATING TEMP. RANGE (°C)
DAS-952R	8 bits	16 Single-Ended	17 kHZ	−25 to + 85
HDAS-8MC	12 bits	8 Differental	50 kHZ	0 to + 70
HDAS-8MR	12 bits	8 Differential	50 kHZ	−25 to + 85
HDAS-16MC	12 bits	16 Single-Ended	50 kHZ	0 to + 70
HDAS-16MR	12 bits	16 Single-Ended	50 kHZ	−25 to + 85

VOLTAGE TO FREQUENCY CONVERTERS

MODEL NO.	LINEARITY	OUTPUT RANGE	GAIN TEMPCO	OPERATING TEMP. RANGE (°C)
VFQ-1C	0.05%	10 kHz to 100 kHz	40 ppm/°C	0 to + 70
VFQ-1R	0.05%	10 kHz to 100 kHz	40 ppm/°C	−25 to + 85
VFQ-2C	0.01%	10 kHz to 100 kHz	40 ppm/°C	0 to + 70
VFQ-3C	0.25%	10 kHz to 100 kHz	40 ppm/°C	0 to + 70

ACTIVE FILTERS

MODEL NO.	FREQUENCY RANGE	Fo ACCURACY	Q RANGE	OPERATING TEMP. RANGE (°C)
FLT-U2	0.01 Hz to 200 kHZ	± 5%	0.1 to 1000	0 to + 70
FLT-U2M	0.01 Hz to 200 kHZ	± 5%	0.1 to 1000	−55 to + 125

MONOLITHIC VOLTAGE CONVERTER

	MODEL NO.	INPUT VOLTAGE RANGE	INPUT CURRENT	OUTPUT VOLTAGE RANGE	OPERATING TEMP. RANGE (°C)
NEW	VI-7660	+ 1.5V to + 10.0V	500 µA	− 1.5V to − 10.0V	0 to + 70

DATEL 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341 TWX 710-346-1953 TLX 951340

HARRIS

HI-200

Dual SPST CMOS Analog Switch

FEATURES

- ANALOG VOLTAGE RANGE ±15V
- ANALOG CURRENT RANGE 80mA
- TURN-ON TIME 240ns
- LOW R_{ON} 55Ω
- LOW POWER DISSIPATION 15mW
- TTL/CMOS COMPATIBLE

APPLICATIONS

- HIGH FREQUENCY ANALOG SWITCHING
- SAMPLE AND HOLD CIRCUITS
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING NETWORKS

DESCRIPTION

HI-200 is a monolithic device comprising two independently selectable SPST switches which feature fast switching speeds (290ns) combined with low power dissipation (15mW at 25°C). Each switch provides low "ON" resistance operation for input signal voltages up to the supply rails and for signal currents up to 80mA. Employing Dielectric Isolation and CMOS processing, HI-200 operates without any applications problems induced by latch-up or SCR mode phenomena.

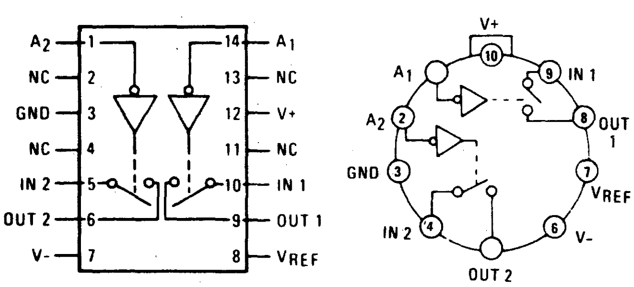
All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-200 is an ideal component for use in high frequency analog switching. Typical applications include signal path switching, sample and hold circuit, digital filters, and op amp gain switching networks.

HI-200 is available in DIP and metal (TO-100) cans. HI-200-2 is specified from -55°C to +125°C while HI-200-5 operates from 0°C to +75°C. HI-200 is functionally and pin compatible with other available "200 series" switches.

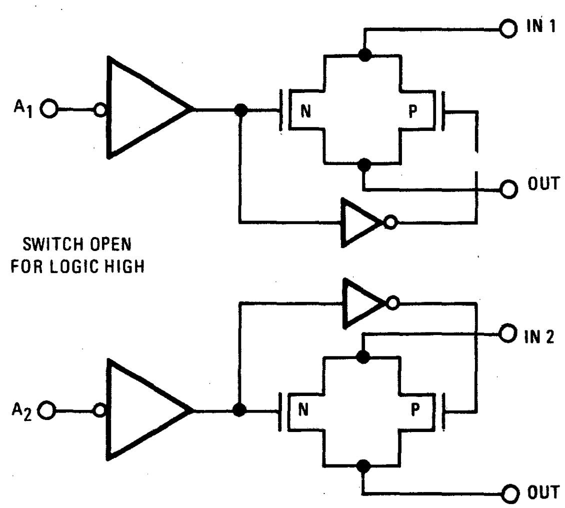
PINOUT

Section 11 for Packaging

Top View



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	44V (±22)	Total Power Dissipation*	450mW
V_{REF} to Ground	+20V, -5V	Operating Temperature	
Digital Input Voltage:	$+V_{Supply}$ +4V	HI-200-2	-55°C to +125°C
	$-V_{Supply}$ -4V	HI-200-4	-20°C to +85°C
Analog Input Voltage (One Switch)	$+V_{Supply}$ +2.0V	HI-200-5	0°C to +75°C
	$-V_{Supply}$ -2.0V	Storage Temperature	-65°C to +150°C

*Derate 6mW/°C Above T_A = 75°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified
Supplies = +15V, -15V; V_{REF} = Open; V_{AH}(Logic Level High) = 2.4V V_{AL}(Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics

PARAMETER	TEMP.	HI-200-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-200-5 ** 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG SWITCH CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON}, On Resistance (Note 1)	+25°C		55	70		55	80	Ω
	Full		80	100		72	100	Ω
$I_{S(OFF)}$, Off Input Leakage Current	+25°C		1			1		nA
(Note 6)	Full		100	500		10	500	nA
$I_{D(OFF)}$, Off Output Leakage Current	+25°C		1			1		nA
(Note 6)	Full		100	500		10	500	nA
$I_{D(ON)}$, On Leakage Current (Note 6)	+25°C		.02			.02		nA
	Full		6	500		6	500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.8			0.8	V
V_{AH}, Input High Threshold	Full	2.4			2.4			V
I_A, Input Leakage Current (High or Low) (Note 2)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break - Before Make Delay (Note 3)	+25°C		60			60		ns
t_{on}, Switch on Time	+25°C		240	500		240		ns
t_{off}, Switch off Time	+25°C		330	500		500		ns
"Off Isolation" (Note 4)	+25°C		70			70		dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C		11			11		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C		0.5			0.5		pF
POWER REQUIREMENTS (Note 5)	+25°C		15			15		mW
P_D, Power Dissipation	Full			60			60	mW
I^+, Current	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA
I^-, Current	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA

NOTES:
1. V_{OUT} = ±10V I_{OUT} = 1mA
2. Digital Inputs Are MOS Gates - Typical Leakage is Less Than 1nA
3. V_{AH} = 4.0V
4. V_A = +5V, R_L = 1KΩ, C_L = 10pF, V_S = 3VRMS, f = 100kHz
5. V_A = +3V or V_A = OV For Both Switches
6. Refer to leakage current measurement diagram on page (3-8)

** Note: HI-200-4 has same specifications as HI-200-5 over the temperature range -20°C to +85°C.

HARRIS

HI-201

Quad SPST CMOS Analog Switch

FEATURES

- ANALOG VOLTAGE RANGE ±15V
- ANALOG CURRENT RANGE 80mA
- TURN-ON TIME 185ns
- LOW R_{ON} 55 Ω
- LOW POWER DISSIPATION 15mW
- TTL/CMOS COMPATIBLE

APPLICATIONS

- HIGH FREQUENCY ANALOG SWITCHING
- SAMPLE AND HOLD CIRCUITS
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING NETWORKS

DESCRIPTION

HI-201 is a monolithic device comprising four independently selectable SPST switches which feature fast switching speeds (185ns) combined with low power dissipation (15mW at 25°C). Each switch provides low "ON" resistance operation for input signal voltages up to the supply rails and for signal currents up to 80mA. Employing Dielectric Isolation and CMOS processing, HI-201 operates without any applications problems induced by latch-up or SCR-mode phenomena.

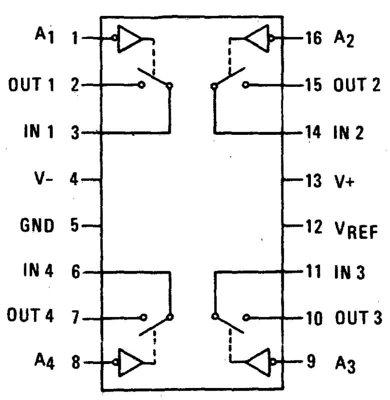
All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-201 is an ideal component for use in high frequency analog switching. Typical applications include signal path switching, sample and hold circuit, digital filters, and op amp gain switching networks.

HI-201 is available in a 16 lead dual-in-line package. HI-201-2 is specified from -55°C to +125°C while HI-201-5 operates from 0°C to +75°C. HI-201 is functionally and pin compatible with other available "200 series" switches.

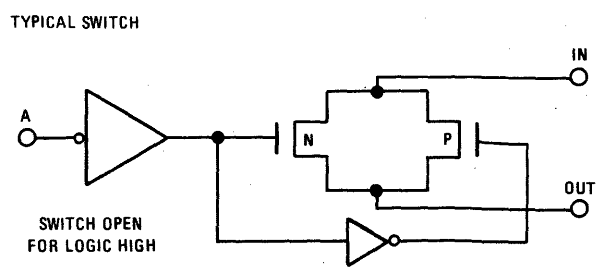
PIN OUT

Section 11 for Packaging

Top View



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	44V (±22)	Total Power Dissipation*	450mW
V_{REF} to Ground	+20V, -5V	Operating Temperature	
Digital Input Voltage:	$+V_{Supply}$ +4V	HI-200-2	-55°C to +125°C
	$-V_{Supply}$ -4V	HI-200-4	-20°C to +85°C
Analog Input Voltage (One Switch)	$+V_{Supply}$ +2.0V	HI-200-5	0°C to +75°C
	$-V_{Supply}$ -2.0V	Storage Temperature	-65°C to +150°C

*Derate 6mW/°C Above T_A = 75°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified

Supplies = +15V, -15V; V_{REF} = Open; V_{AH}(Logic Level High) = 2.4V V_{AL}(Logic Level Low) = +0.8V

For Test Conditions, consult Performance Characteristics

PARAMETER	TEMP.	HI-200-2 -55°C to +125°C MIN.	HI-200-2 TYP.	HI-200-2 MAX.	HI-200-5 ** 0°C to +75°C MIN.	HI-200-5 TYP.	HI-200-5 MAX.	UNITS
ANALOG SWITCH CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON}, On Resistance (Note 1)	+25°C		55	70		55	80	Ω
	Full		80	100		72	100	Ω
$I_{S(OFF)}$, Off Input Leakage Current (Note 6)	+25°C		1			1		nA
	Full		100	500		10	500	nA
$I_{D(OFF)}$, Off Output Leakage Current (Note 6)	+25°C		1			1		nA
	Full		100	500		10	500	nA
$I_{D(ON)}$, On Leakage Current (Note 6)	+25°C		.02			.02		nA
	Full		6	500		6	500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.8			0.8	V
V_{AH}, Input High Threshold	Full	2.4			2.4			V
I_A, Input Leakage Current (High or Low) (Note 2)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break - Before Make Delay (Note 3)	+25°C		60			60		ns
t_{on}, Switch on Time	+25°C		240	500		240		ns
t_{off}, Switch off Time	+25°C		330	500		500		ns
"Off Isolation" (Note 4)	+25°C		70			70		dB
$C_{S\,(OFF)}$, Input Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D\,(OFF)}$, Output Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C		11			11		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS\,(OFF)}$, Drain-To-Source Capacitance	+25°C		0.5			0.5		pF
POWER REQUIREMENTS (Note 5)								
P_D, Power Dissipation	+25°C		15			15		mW
	Full			60			60	mW
I^+, Current	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA
I^-, Current	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA

NOTES:
1. V_{OUT} = ±10V I_{OUT} = 1mA
2. Digital Inputs Are MOS Gates - Typical Leakage is Less Than 1nA
3. V_{AH} = 4.0V
4. V_A = +5V, R_L = 1KΩ, C_L = 10pF, V_S = 3VRMS, f = 100kHz
5. V_A = +3V or V_A = 0V For Both Switches
6. Refer to leakage current measurement diagram on page (3-8)

** Note: HI-200-4 has same specifications as HI-200-5 over the temperature range -20°C to +85°C.

HARRIS

HI-201

Quad SPST CMOS Analog Switch

FEATURES

- ANALOG VOLTAGE RANGE ±15V
- ANALOG CURRENT RANGE 80mA
- TURN-ON TIME 185ns
- LOW R_{ON} 55Ω
- LOW POWER DISSIPATION 15mW
- TTL/CMOS COMPATIBLE

APPLICATIONS

- HIGH FREQUENCY ANALOG SWITCHING
- SAMPLE AND HOLD CIRCUITS
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING NETWORKS

DESCRIPTION

HI-201 is a monolithic device comprising four independently selectable SPST switches which feature fast switching speeds (185ns) combined with low power dissipation (15mW at 25°C). Each switch provides low "ON" resistance operation for input signal voltages up to the supply rails and for signal currents up to 80mA. Employing Dielectric Isolation and CMOS processing, HI-201 operates without any applications problems induced by latch-up or SCR-mode phenomena.

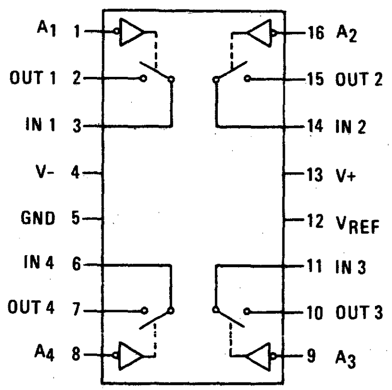
All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-201 is an ideal component for use in high frequency analog switching. Typical applications include signal path switching, sample and hold circuit, digital filters, and op amp gain switching networks.

HI-201 is available in a 16 lead dual-in-line package. HI-201-2 is specified from -55°C to +125°C while HI-201-5 operates from 0°C to +75°C. HI-201 is functionally and pin compatible with other available "200 series" switches.

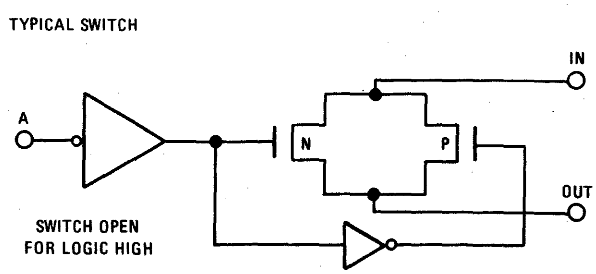
PIN OUT

Section 11 for Packaging

Top View



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 4 and 13	44V (±22)	Total Power Dissipation*		750mW
V_{REF} to Ground	+20V, -5V	Operating Temperature		
Digital Input Voltage:	$V_{Supply}(+)$ +4V		HI-201-2	-55°C to +125°C
	$V_{Supply}(-)$ -4V		HI-201-4	-20°C to +85°C
Analog Input Voltage (One Switch)	$+V_{Supply}$ +2.0V		HI-201-5	0°C to +75°C
	$-V_{Supply}$ -2.0V	Storage Temperature		-65°C to +150°C

*Derate 8mW/°C Above T_A = +75°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified
Supplies = +15V, -15V; V_{REF} = Open; V_{AH} (Logic Level High) = 2.4V V_{AL} (Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics

PARAMETER	TEMP.	HI-201-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-201-5 ** 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG SWITCH CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON}, On Resistance (Note 1)	+25°C		55	70		55	80	Ω
	Full		80	100		75	100	Ω
$I_{S(OFF)}$, Off Input Leakage Current (Note 6)	+25°C		2			2		nA
	Full			500			250	nA
$I_{D(OFF)}$, Off Output Leakage Current (Note 6)	+25°C		2			2		nA
	Full			500			250	nA
$I_{D(ON)}$, On Leakage Current (Note 6)	+25°C		2			2		nA
	Full			500			250	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.8			0.8	V
V_{AH}, Input High Threshold	Full	2.4			2.4			V
I_A, Input Leakage Current (High or Low) (Note 2)	Full			1.0			1.0	µA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break - Before Make Delay (Note 3)	+25°C		30			30		ns
t_{on}, Switch ON Time	+25°C		185	500		185		ns
t_{off}, Switch OFF Time	+25°C		220	500		220		ns
"Off Isolation" (Note 4)	+25°C		80			80		dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C		11			11		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C		0.5			0.5		pF
POWER REQUIREMENTS (Note 5)	+25°C		15			15		mW
P_D, Power Dissipation	Full			60			60	mW
I+, Current (Pin 13)	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA
I– Current (Pin 4)	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA

NOTES:
1. V_{OUT} = ±10V I_{OUT} = 1mA
2. Digital Inputs Are MOS Gates - Typical Leakage is Less Than 1nA
3. V_{AH} = 4.0V
4. V_A = 5V, R_L = 1KΩ, C_L = 10pF, V_S = 3VRMS, f = 100KHz
5. V_A = +3V or V_A = 0V For all Switches
6. Refer to leakage current measurement diagram on page (3-14)

** Note: HI-201-4 has same specifications as HI-201-5 over the temperature range -20°C to +85°C.

HARRIS

HI-201HS

High Speed Quad SPST CMOS Analog Switch

Preliminary

FEATURES

- ANALOG VOLTAGE RANGE ±15V
- ANALOG CURRENT RANGE 80mA
- TURN-ON TIME 30ns
- LOW R_{ON} 30Ω
- LOW POWER DISSIPATION 120mW
- TTL COMPATIBLE
- LOW CHARGE INJECTION 10pC

APPLICATIONS

- HIGH FREQUENCY ANALOG SWITCHING
- SAMPLE AND HOLD CIRCUITS
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING NETWORKS

DESCRIPTION

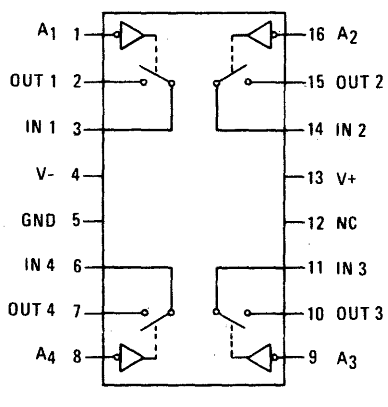
The Harris HI-201HS is a monolithic CMOS analog switch featuring very fast switching speeds and low ON resistance. The device consists of four independently selectable SPST switches and is identical in pinout to the HI-201 quad switch.

Fabricated using the Harris dielectric isolation technology, this TTL compatible device offers improved performance over previously available CMOS analog switches. Featuring switching speeds of 50ns max., low ON resistance of 50Ω max., and wide analog signal range of ±15V, the HI-201HS is designed for any application where improved switching performance, particularly switching speed, is required.

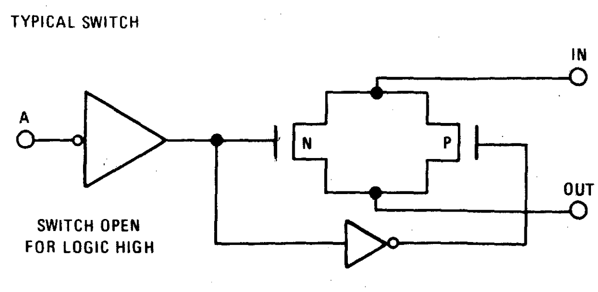
The HI-201HS is available in a 16 lead dual-in-line package. The HI-201HS-2 is specified for the temperature range of -55°C to +125°C and the HI-201HS-5 operates from 0°C to +75°C.

PIN OUT

Top View



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage Between Pins 4 and 13	+36V	Total Power Dissipation*		750mW
		Operating Temperature		
Digital Input Voltage:	$V_{Supply}(+)$ +4V		HI-201HS-2	-55°C to +125°C
	$V_{Supply}(-)$ -4V		HI-201HS-4	-20°C to +85°C
Analog Input Voltage (One Switch)	$+V_{Supply}$ +2.0V		HI-201HS-5	0°C to +75°C
	$-V_{Supply}$ -2.0V	Storage Temperature		-65°C to +150°C

*Derate 8mW/°C Above T_A = +75°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified, Supplies = +15V, -15V; V_{AH} (Logic Level High) = 5.0V; V_{AL} (Logic Level Low) = +0.8V

PARAMETER	TEMP.	HI-201HS-2 HI-201HS-5 MIN.	TYP.	MAX.	UNITS
ANALOG SWITCH CHARACTERISTICS					
V_S, Analog Signal Range	Full	-15		+15	V
R_{ON}, On Resistance (Note 2)	+25°C		30	50	Ω
	Full			75	Ω
$I_{S(OFF)}$, Off Input Leakage Current	+25°C		.3	10	nA
	Full			100	nA
$I_{D(OFF)}$, Off Output Leakage Current	+25°C		.3	10	nA
	Full			100	nA
$I_{D(ON)}$, On Leakage Current	+25°C		.1	10	nA
	Full			100	nA
DIGITAL INPUT CHARACTERISTICS					
V_{AL}, Input Low Threshold	Full			0.8	V
V_{AH}, Input High Threshold	+25°C	2.0			V
	Full	2.4			V
I_{AL}, Input Leakage Current (Low)	Full			500	μA
I_{AH}, Input Leakage Current (High)	Full			40	μA
SWITCHING CHARACTERISTICS					
t_{ON}, Switch ON Time (Note 3)	+25°C		30	50	ns
t_{OFF}, Switch OFF Time (Note 3)	+25°C		40	50	ns
"Off Isolation" (Note 4)	+25°C		72		dB
Crosstalk (Note 5)	+25°C		86		dB
Charge Injection (Note 6)	+25°C		10		pC
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		10		pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C		10		pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C		30		pF
C_A, Digital Input Capacitance	+25°C		18		pF
$C_{DS(OFF)}$, Drain-to-Source Capacitance	+25°C		.5		pF
POWER REQUIREMENTS (Note 7)					
P_D, Power Dissipation	+25°C		120		mW
	Full			240	mW
I^+, Current (Pin 13)	+25°C		4.5		mA
	Full			10.0	mA
I^-, Current (Pin 4)	+25°C		3.5		mA
	Full			6	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, I_{OUT} = 1mA
3. R_L = 1kΩ, C_L = 35pF, V_{IN} = +10V, V_A = +5V
4. V_A = 5V, R_L = 1KΩ, C_L = 10pF, V_S = 3 VRMS, f = 100kHz
5. V_A = 5V, R_L = 1kΩ, f = 100kHz, V_{IN} = $2V_{p-p}$
6. C_L = 1000pF, V_{IN} = 0V, R_{IN} = 0Ω; $\Delta Q = C_L \times \Delta V_O$
7. V_A = 5V or V_A = 0 for all switches.

HARRIS

HI-300 thru HI-307

CMOS Analog Switches

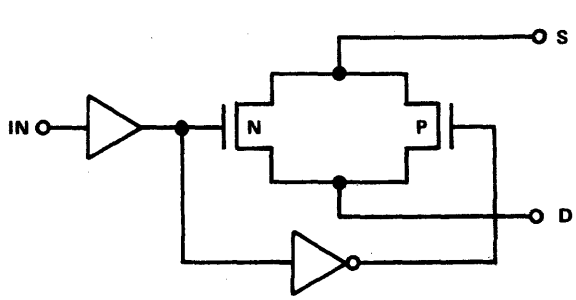
FEATURES

- ANALOG SIGNAL RANGE (±15V SUPPLIES) ±15V
- LOW LEAKAGE (TYP. @ 25°C) 40pA
- LOW LEAKAGE (TYP. @ 125°C) 1nA
- LOW ON RESISTANCE (TYP. @ 25°C) 35Ω
- BREAK-BEFORE-MAKE DELAY (TYP.) 60ns
- CHARGE INJECTION 30pC
- TTL, CMOS COMPATIBLE
- SYMETRICAL SWITCH ELEMENTS
- LOW OPERATING POWER 1.0mW
  (TYP. FOR HI-300 - 303)

APPLICATIONS

- SAMPLE AND HOLD i.e. LOW LEAKAGE SWITCHING
- OP AMP GAIN SWITCHING i.e. LOW ON RESISTANCE
- PORTABLE, BATTERY OPERATED CIRCUITS
- LOW LEVEL SWITCHING CIRCUITS
- DUAL OR SINGLE SUPPLY SYSTEMS

FUNCTIONAL DIAGRAM



TYPICAL SWITCH 300 SERIES

DESCRIPTION

The HI-300 through HI-307 series of switches are monolithic devices fabricated using CMOS technology and the Harris dielectric isolation process. These switches feature break-before-make switching, (HI-301, 303, 305 & 307 only), low and nearly constant ON resistance over the full analog signal range, and low power dissipation, (a few milliwatts for the HI-300-303, a few hundred microwatts for the HI-304-307).

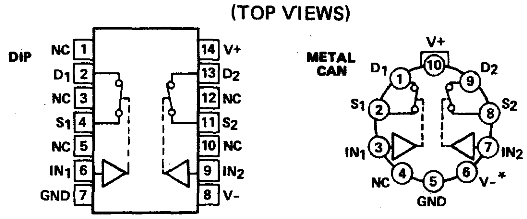
The HI-300-303 are TTL compatible and have a logic "0" condition with an input less than 0.8V and a logic "1" condition with an input greater than 4.0V. The HI-304-307 switches are CMOS compatible and have a low state with an input less than 3.5V and a high state with an input greater than 11V. (See pinouts for switch conditions with a logic "1" input.)

All the devices are available in a 14 pin epoxy or ceramic DIP. The HI-300, 301, 304 and 305 are also available in a 10 pin metal can. Each of the switch types are available in either the -55°C to +125°C or 0°C to +75°C operating ranges.

PINOUTS (SWITCH STATES ARE FOR A LOGIC "1" INPUT)

Section 11 for Packaging

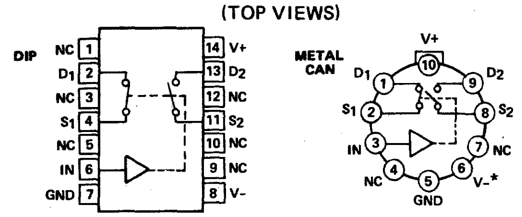
DUAL SPST HI-300 & HI-304
(TOP VIEWS)



LOGIC	SWITCH
0	OFF
1	ON

*The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

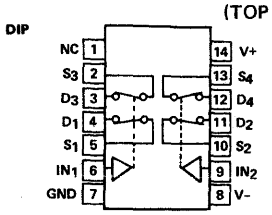
SPDT HI-301 & HI-305
(TOP VIEWS)



LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

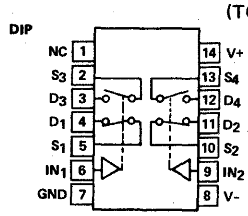
*The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

DUAL DPST HI-302 & HI-306
(TOP VIEW)



LOGIC	SWITCH
0	OFF
1	ON

DUAL SPDT HI-303 & HI-307
(TOP VIEW)



LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between Supplies	44V (±22V)	Total Power Dissipation	
Digital Input Voltage	V^+ +4.0V	14 Pin Epoxy DIP	526mW
	V^- -4.0V	14 Pin Ceramic DIP	588mW
		10 Pin Metal Can*	435mW
		*Derate 6.9mW/°C Above T_A = 70°C	
Analog Input Voltage	V^+ 1.5V	Operating Temperature HI-3XX-2	−55°C to +125°C
	V^- 1.5V	HI-3XX-5	0°C to +75°C
		Storage Temperature	−65°C to +150°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified; Supplies = +15V, -15V; V_{IN} = Logic Input.
HI-300-303 : V_{IN} - for Logic "1" = 4V, for Logic "0" = 0.8V
HI-304-307 : V_{IN} - for Logic "1" = 11V, for Logic "0" = 3.5V

PARAMETER	TEMP	-55°C to +125°C MIN	TYP	MAX	0°C to +75°C MIN	TYP	MAX	UNITS
ANALOG SWITCH CHARACTERISTICS								
Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON} ON Resistance (Note 2)	+25°C		35	50		35	50	Ω
	Full		40	75		40	75	Ω
IS_{OFF} OFF Input Leakage Current (Note 3)	+25°C		0.04	1		0.04	5	nA
	Full		1	100		0.2	100	nA
ID_{OFF} OFF Output Leakage Current (Note 3)	+25°C		0.04	1		0.04	5	nA
	Full		1	100		0.2	100	nA
ID_{ON} ON Leakage Current (Note 4)	+25°C		0.03	1		0.03	5	nA
	Full		0.5	100		0.2	100	nA
DIGITAL INPUT CHARACTERISTICS								
V_{INL} Input Low Level *	Full			0.8			0.8	V
V_{INH} Input High Level *	Full	4			4			V
V_{INL} Input Low Level **	Full			3.5			3.5	V
V_{INH} Input High Level **	Full	11			11			V
I_{INL} Input Leakage Current (Low) (Note 5)	Full			1			1	μA
I_{INH} Input Leakage Current (High) (Note 5)	Full			1			1	μA
SWITCHING CHARACTERISTICS								
t_{OPEN} Break-Before-Make Delay ***	+25°C		60			60		ns
t_{ON} Switch On Time *	+25°C		210	300		210	300	ns
t_{OFF} Switch Off Time *	+25°C		160	250		160	250	ns
t_{ON} Switch On Time **	+25°C		160	250		160	250	ns
t_{OFF} Switch Off Time **	+25°C		100	150		100	150	ns
Off Isolation (Note 6)	+25°C		60			60		dB
Charge Injection (Note 7)	+25°C		3			3		mV
CS_{OFF} Input Switch Capacitance	+25°C		16			16		pF
CD_{OFF} Output Switch Capacitance	+25°C		14			14		pF
CD_{ON} Output Switch Capacitance	+25°C		35			35		pF
C_{IN} (High) Digital Input Capacitance	+25°C		5			5		pF
C_{IN} (Low) Digital Input Capacitance	+25°C		5			5		pF
POWER REQUIREMENTS								
I+ Current * (Note 8)	+25°C		0.09	0.5		0.09	0.5	mA
	Full			1			1	mA
I- Current * (Note 8)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA
I+ Current * (Note 9)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA
I- Current * (Note 9)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA
I+ Current ** (Note 10)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA
I- Current ** (Note 10)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA
I+ Current ** (Note 11)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA
I- Current ** (Note 11)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA

* HI-300 thru HI-303 Only; ** HI-304 thru HI-307 Only; *** HI-301, HI-303, HI-305, HI-307 Only

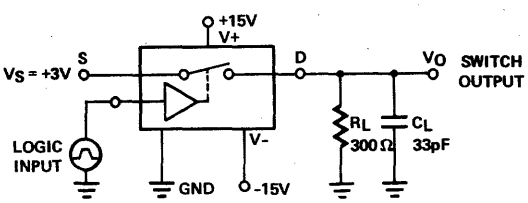
ELECTRICAL CHARACTERISTICS NOTES:

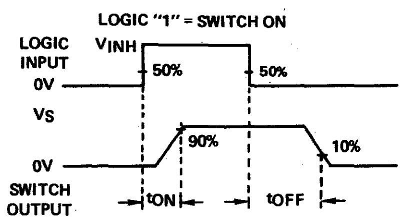
1. As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.
2. $V_S = \pm 10V$, $I_{OUT} = -10mA$ On resistance derived from the voltage measured across the switch under the above conditions.
3. $V_S = \pm 14V, V_D = \mp 14V$.
4. $V_S = V_D = \pm 14V$.
5. The digital inputs are diode protected MOS gates and typical leakages of 1nA or less can be expected.
6. $V_S = 1V_{RMS}$, f = 500kHz, C_L = 15pF, R_L = 1k. $C_L = C_{FIXTURE} + C_{PROBE}$, "Off Isolation" = 20logVS/VD.
7. V_S = 0V, C_L = 10,000pF, Logic Drive = 5V pulse. (HI-300 -303) Switches are symmetrical; S and D may be interchanged. Logic Drive = 15V (HI-304-307)
8. V_{IN} = 4V (one input) (all other inputs = 0V)
9. V_{IN} = 0.8V (all inputs).
10. V_{IN} = 15V (all inputs).
11. V_{IN} = 0V (all inputs).
12. To drive from DTL/TTL circuits, pull-up resistors to +5V supply are recommended.

TEST CIRCUITS

SWITCHING TEST CIRCUIT (t_{ON}, t_{OFF})

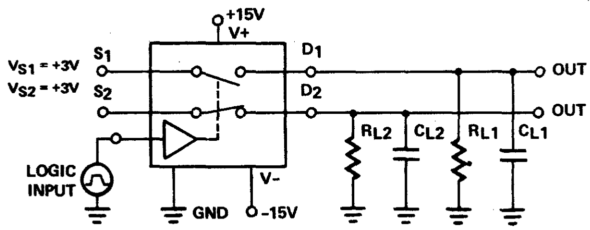
SWITCH TYPE	V_{INH}
HI-300 thru HI-303 HI-304 thru HI-307	4V 15V

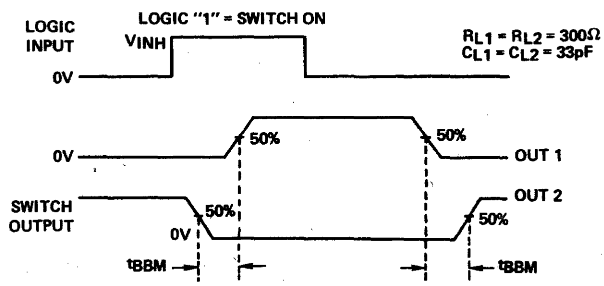




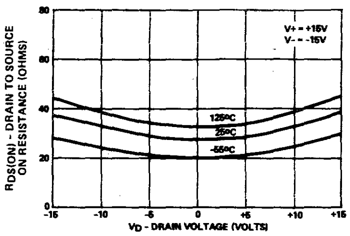
BREAK-BEFORE-MAKE TEST CIRCUIT (t_{BBM})

SWITCH TYPE	V_{INH}
HI-301, HI-303 HI-305, HI-307	5V 15V

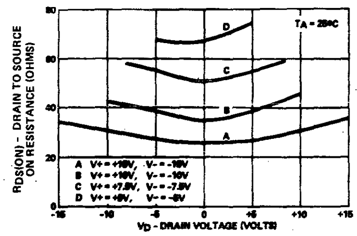




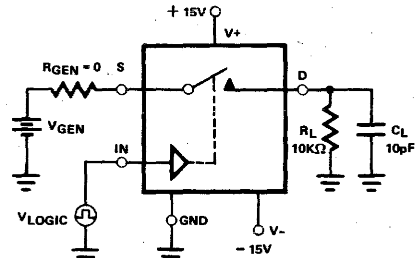
$R_{DS(ON)}$ VS. V_D AND TEMPERATURE



$R_{DS(ON)}$ VS. V_D AND POWER SUPPLY VOLTAGE

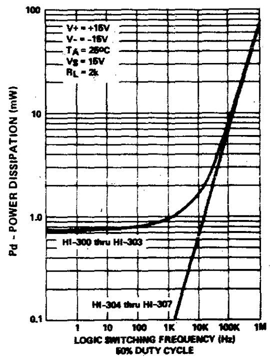


Typical delay, rise, fall, settling times, and switching transients in this circuit.

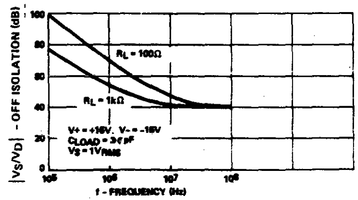


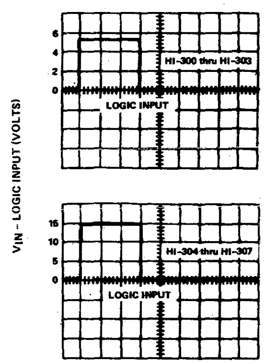
If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.

DEVICE POWER DISSIPATION VS. SWITCHING FREQUENCY SINGLE LOGIC INPUT

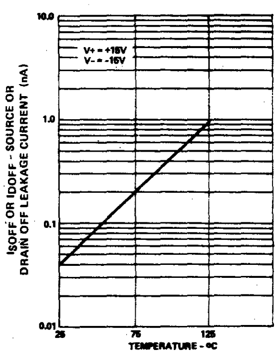


OFF ISOLATION VS. FREQUENCY

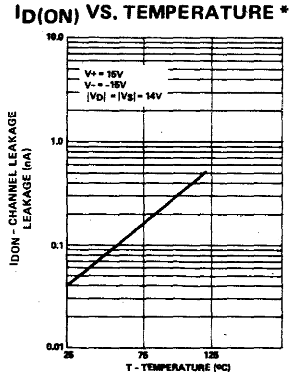


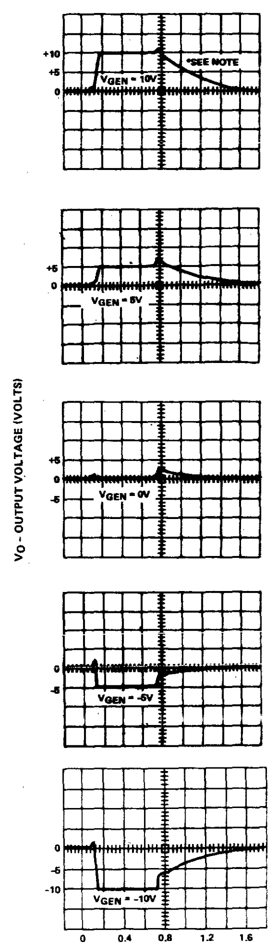


$I_{S(OFF)}$ OR $I_{D(OFF)}$ VS. TEMPERATURE *



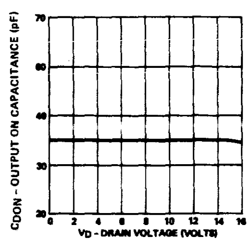
$I_{D(ON)}$ VS. TEMPERATURE *



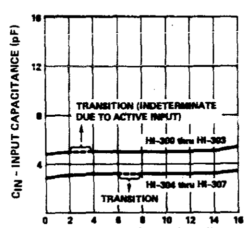


* The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

OUTPUT ON CAPACITANCE VS. DRAIN VOLTAGE

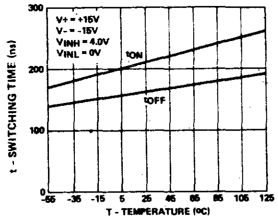


DIGITAL INPUT CAPACITANCE VS. INPUT VOLTAGE

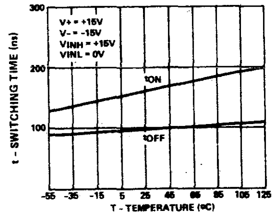


TYPICAL PERFORMANCE CURVES (Continued)

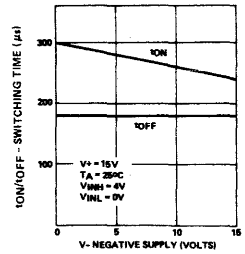
SWITCHING TIME VS. TEMPERATURE HI-300 thru HI-303



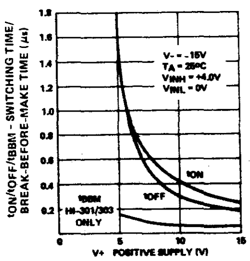
SWITCHING TIME VS. TEMPERATURE HI-304 thru HI-307



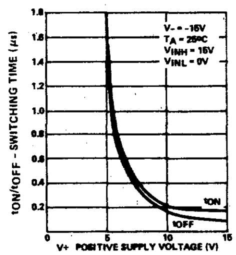
SWITCHING TIME VS. NEGATIVE SUPPLY VOLTAGE HI-300 thru HI-303



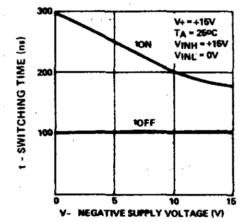
SWITCHING TIME AND BREAK BEFORE MAKE TIME VS. POSITIVE SUPPLY VOLTAGE HI-300 thru HI-303



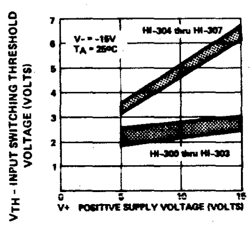
SWITCHING TIME VS. POSITIVE SUPPLY VOLTAGE HI-304 thru HI-307



SWITCHING TIME VS. NEGATIVE SUPPLY VOLTAGE HI-304 thru HI-307



INPUT SWITCHING THRESHOLD VS. POSITIVE SUPPLY VOLTAGE HI-300 thru HI-307



HARRIS

HI-381/384/387/390

CMOS Analog Switches

INTERFACE

Harris Semiconductor

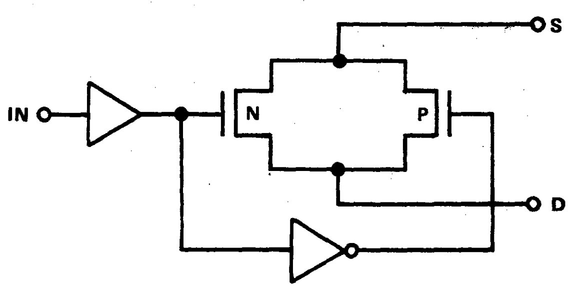
FEATURES

- ANALOG SIGNAL RANGE (±15V SUPPLIES) ±15V
- LOW LEAKAGE (TYP. @ 25°C) 40pA
- LOW LEAKAGE (TYP @ 125°C) 1nA
- LOW ON RESISTANCE (TYP. @ 25°C) 35Ω
- BREAK-BEFORE-MAKE DELAY (TYP.) 60ns
- CHARGE INJECTION 30pC
- TTL COMPATIBLE
- SYMMETRICAL SWITCH ELEMENTS
- LOW OPERATING POWER (TYP.) 1.0mW

APPLICATIONS

- SAMPLE AND HOLD i.e. LOW LEAKAGE SWITCHING
- OP AMP GAIN SWITCHING i.e. LOW ON RESISTANCE
- PORTABLE BATTERY OPERATED CIRCUITS
- LOW LEVEL SWITCHING CIRCUITS
- DUAL OR SINGLE SUPPLY SYSTEMS

FUNCTIONAL DIAGRAM



TYPICAL SWITCH - 300 SERIES

DESCRIPTION

The HI-381 through HI-390 series of switches are monolithic devices fabricated using CMOS technology and the Harris dielectric isolation process. These devices are TTL compatible and are available in four switching configurations. (See device pinout for particular switching function with a logic "1" input.)

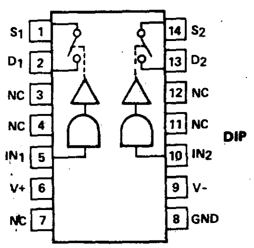
These switches feature low leakage and supply currents, low and nearly constant ON resistance over the analog signal range, break-before-make switching and low power dissipation.

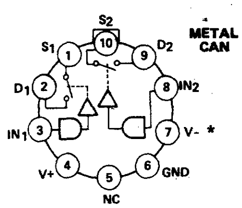
The HI-381 and HI-387 switches are available in a 14 pin epoxy or ceramic DIP or10 pin metal can. The HI-384 and HI-390 are available in a 16 pin epoxy or ceramic DIP. Each of the individual switch types are available in the -55°C to +125°C and 0°C to +75°C operating ranges.

PINOUTS (SWITCH STATES ARE FOR A LOGIC "1" INPUT)

Section 11 for Packaging

DUAL SPST HI-381
(TOP VIEWS)

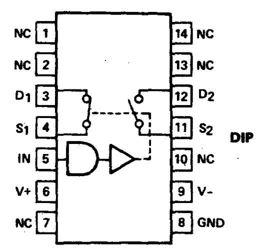


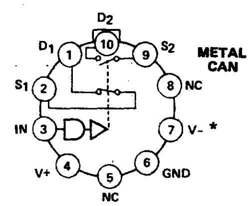


LOGIC	SW 1 SW 2
0	ON
1	OFF

*The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

SPDT HI-387
(TOP VIEWS)

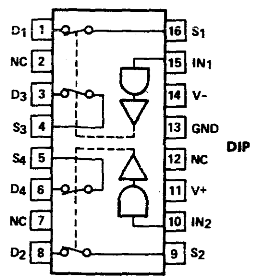




LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

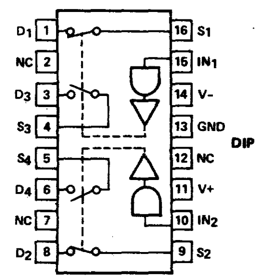
*The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

DUAL DPST HI-384
(TOP VIEW)



LOGIC	SW 1 - 4
0	OFF
1	ON

DUAL SPDT HI-390
(TOP VIEW)



LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between Supplies	44V (±22)	Total Power Dissipation		
			14 Pin Epoxy DIP	526mW
Digital Input Voltage			14 Pin Ceramic DIP	588mW
	V^++4.0V		16 Pin Epoxy DIP	625mW
	V^--4.0V		16 Pin Ceramic DIP	685mW
			10 Pin Metal Can*	435mW
Analog Input Voltage			*Derate 6.9mW/°C above T_A = 70°C	
	V^++1.5V			
	V^--1.5V	Operating Temperature		
			HI-3XX-2	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C		HI-3XX-5	0°C to +75°C

ELECTRICAL CHARACTERISITICS

Unless otherwise specified; Supplies = +15V, -15V; VIN = Logic Input, VIN for logic "1" = 4V, for logic 0 = .8V

		-55°C to +125°C			0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
ANALOG SWITCH CHARACTERISTICS								
Analog Signal Range	FULL	-15		+15	-15		+15	V
R_{ON} ON Resistance (Note 2)	+25°C		35	50		35	50	Ω
	FULL		40	75		40	75	Ω
IS_{OFF} OFF Input Leakage Current (Note 3)	+25°C		.04	1		.04	5	nA
	FULL		1	100		0.2	100	nA
ID_{OFF} OFF Output Leakage Current (Note 3)	+25°C		.04	1		.04	5	nA
	FULL		1	100		0.2	100	nA
ID_{ON} ON Leakage Current (Note 4)	+25°C		.03	1		.03	5	nA
	FULL		0.5	100		0.2	100	nA
DIGITAL INPUT CHARACTERISTICS								
V_{INL} Input Low Level	FULL			.8			.8	V
V_{INH} Input High Level	FULL	4			4			V
I_{INH} Input Leak. Current (High) (Note 5)	FULL			1			1	μA
I_{INL} Input Leak. Current (Low) (Note 5)	FULL			1			1	μA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break-Before Make Delay (HI-387/390 only)	+25°C		60			60		ns
t_{ON}, Switch ON Time	+25°C		210	300		210	300	ns
t_{OFF}, Switch OFF Time	+25°C		160	250		160	250	ns
OFF Isolation (Note 6)	+25°C		60			60		dB
Charge Injection (Note 7)	+25°C		3			3		mV
CS_{OFF} Input Switch Capacitance	+25°C		16			16		pF
CD_{OFF} Output Switch Capacitance	+25°C		14			14		pF
CD_{ON} Output Switch Capacitance	+25°C		35			35		pF
C_{IN} (High) Digital Input Capacitance	+25°C		5			5		pF
C_{IN} (Low) Digital Input Capacitance	+25°C		5			5		pF
POWER REQUIREMENTS								
I+ Current (Note 8)	+25°C		.09	.5		.09	.5	mA
	FULL			1			1	mA
I- Current (Note 8)	+25°C		.01	10		.01	100	μA
	FULL			100				μA
I+ Current (Note 9)	+25°C		.01	10		.01	100	μA
	FULL			100				μA
I- Current (Note 9)	+25°C		.01	10		.01	100	μA
	FULL			100				μA

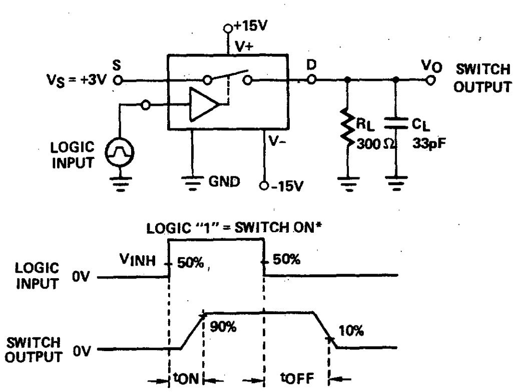
ELECTRICAL CHARACTERISTICS NOTES :

1. As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.
2. $V_S = \pm 10V$, $I_{OUT} = -10mA$ on resistance derived from the voltage measured across the switch under the above conditions.
3. $V_S = \pm 14V$, $V_D = \mp 14V$.
4. $V_S = V_D = \pm 14V$.
5. The digital inputs are diode protected MOS gates and typical leakages of 1nA or less can be expected.
6. $V_S = 1V_{RMS}$, f = 500kHz, C_L = 15pF, R_L = 1k, $C_L = C_{FIXTURE} + C_{PROBE}$, "off isolation" = $20\log V_S/V_D$.
7. V_S = 0V, C_L = 10,000pF, Logic Drive = 5V pulse. Switches are symmetrical; S and D may be interchanged.
8. V_{IN} = 4V. (one input) (all other inputs = 0)
9. V_{IN} = 0.8V. (all inputs)
10. To drive from DTL/TTL circuits, pull-up resistors to +5V Supply are recommended.

TEST CIRCUITS

SWITCHING TEST CIRCUIT (t_{ON}, t_{OFF})

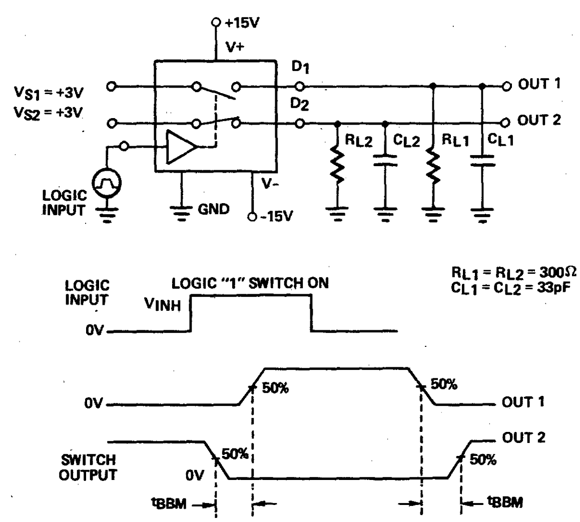
SWITCH TYPE	V_{INH}
HI-381 thru HI-390	5V



*Inverted logic for HI-381

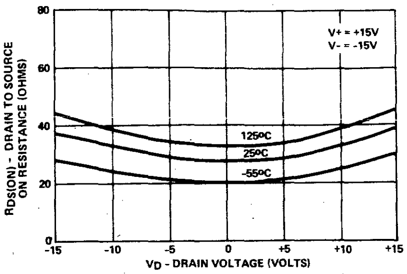
BREAK-BEFORE-MAKE TEST CIRCUIT (t_{BBM})

SWITCH TYPE	V_{INH}
HI-387 and HI-390	5V

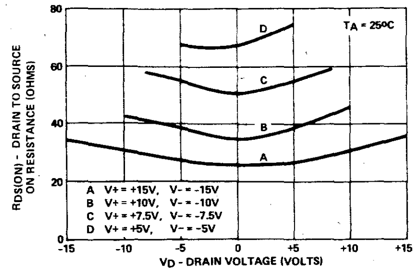


TYPICAL PERFORMANCE CURVES

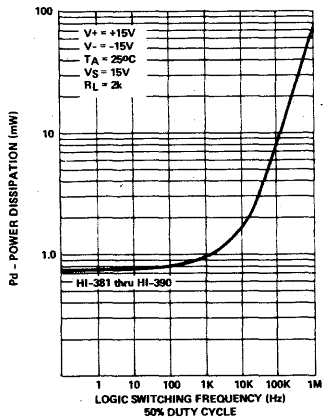
$R_{DS(ON)}$ VS. V_D AND TEMPERATURE



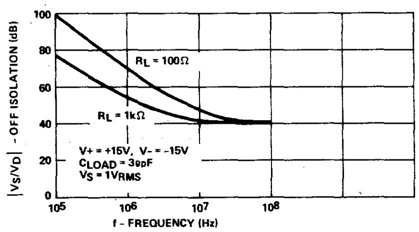
$R_{DS(ON)}$ VS. V_D AND POWER SUPPLY VOLTAGE



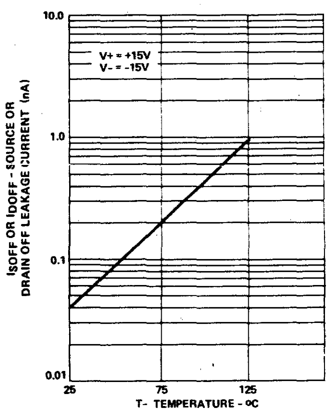
DEVICE POWER DISSIPATION VS. SWITCHING FREQUENCY SINGLE LOGIC INPUT



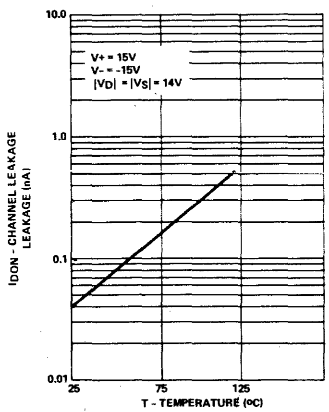
OFF ISOLATION VS. FREQUENCY



I_{SOFF} OR I_{DOFF} VS. TEMPERATURE*

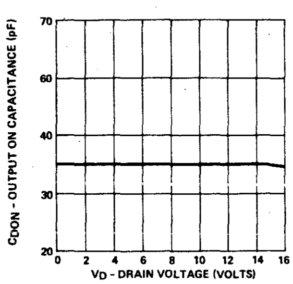


I_{DON} VS. TEMPERATURE*

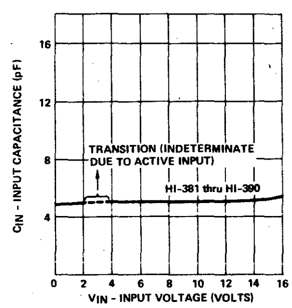


* The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

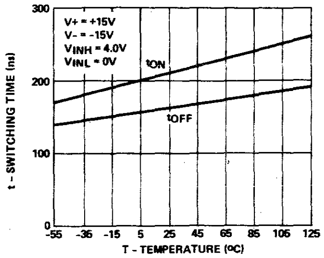
OUTPUT ON CAPACITANCE VS. DRAIN VOLTAGE



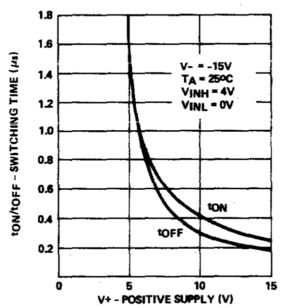
DIGITAL INPUT CAPACITANCE VS. INPUT VOLTAGE



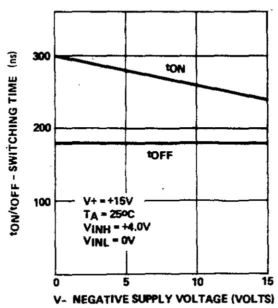
SWITCHING TIME VS. TEMPERATURE
HI-381 thru HI-390



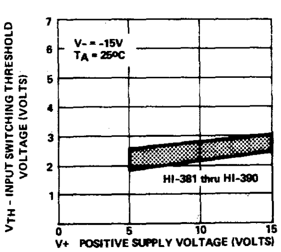
SWITCHING TIME VS. POSITIVE SUPPLY VOLTAGE
HI-381 thru HI-390



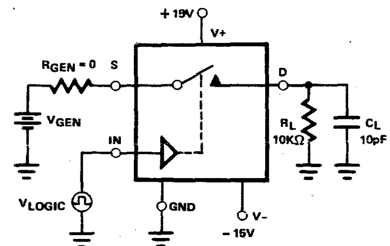
SWITCHING TIME VS. NEGATIVE SUPPLY VOLTAGE
HI-381 thru HI-390



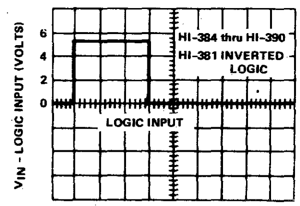
INPUT SWITCHING THRESHOLD VS. POSITIVE SUPPLY VOLTAGE
HI-381 thru HI-390

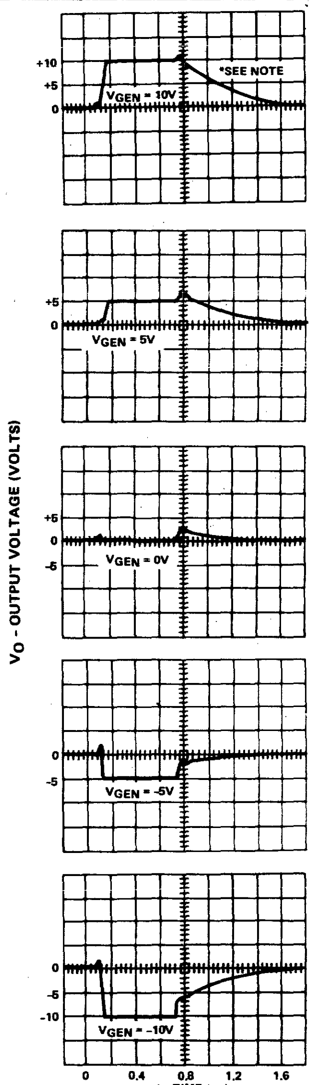


Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.





* NOTE: The turn-off time is primarily limited here by the RC time constant (100ns) of the load.

HARRIS

HI-5040 thru HI-5051 HI-5046A and HI-5047A

CMOS Analog Switches

FEATURES

- WIDE ANALOG SIGNAL RANGE ±15V
- LOW "ON" RESISTANCE (TYP) 25Ω
- HIGH CURRENT CAPABILITY (TYP) 80mA
- BREAK-BEFORE-MAKE SWITCHING
  - TURN-ON TIME (TYP) 370ns
  - TURN-OFF TIME (TYP) 280ns
- NO LATCH-UP
- INPUT MOS GATES ARE PROTECTED FROM ELECTROSTATIC DISCHARGE
- DTL, TTL, CMOS, PMOS COMPATIBLE

APPLICATIONS

- HIGH FREQUENCY SWITCHING
- SAMPLE AND HOLD
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING

DESCRIPTION

This family of CMOS analog switches offers low-resistance switching performance for analog voltages up to the supply rails and for signal currents up to 80mA. "ON" resistance is low and stays reasonably constant over the full range of operating signal voltage and current. R_{ON} remains exceptionally constant for input voltages between +5V and -5V and currents up to 50mA. Switch impedance also changes very little over temperature, particularly between 0°C and +75°C. R_{ON} is nominally 25 ohms for HI-5048 through HI-5051 and HI-5046A/5047A and 50Ω for HI-5040 through HI-5047.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. Performance is further enhanced by Dielectric Isolation processing which insures latch-free operation with very low input and output leakage currents (0.8nA at 25°C). This family of switches also features very low power operation (1.5mW at 25°C).

There are 14 devices in this switch series which are differentiated by type of switch action and value of R_{ON} (see Functional diagram). All devices are available in 16 pin D.I.P. packages. The HI-5040/5050 switches can directly replace IH-5040 series devices and are functionally compatible with the DG 180/190 family. Each switch type is available in the -55°C to +125°C and 0°C to +75°C performance grades.

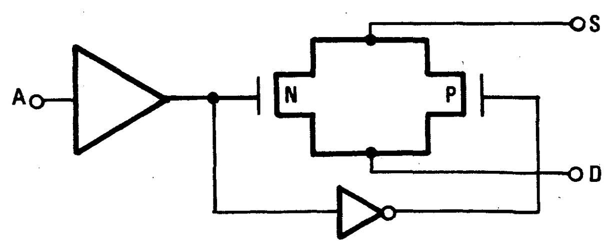
FUNCTIONAL DESCRIPTION

Section 11 for Packaging

PART NUMBER	TYPE	R_{ON}
HI-5040	SPST	75Ω
HI-5041	DUAL SPST	75Ω
HI-5042	SPDT	75Ω
HI-5043	DUAL SPDT	75Ω
HI-5044	DPST	75Ω
HI-5045	DUAL DPST	75Ω
HI-5046	DPDT	75Ω
HI-5046A	DPDT	30Ω
HI-5047	4PST	75Ω
HI-5047A	4PST	30Ω
HI-5048	DUAL SPST	30Ω
HI-5049	DUAL DPST	30Ω
HI-5050	SPDT	30Ω
HI-5051	DUAL SPDT	30Ω

FUNCTIONAL DIAGRAM

TYPICAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V^+ - V^-$)	36V
V_R to Ground	V^+, V^-
Digital and Analog Input Voltage	$V^+ +4V$ $V^- -4V$
Analog Current (S to D)	80mA
Total Power Dissipation*	450mW
Operating Temperature	
HI-50XX-2	-55°C to +125°C
HI-50XX-5	0°C to +75°C
Storage Temperature	-65°C to +150°C

*Derate 6mW/°C above T_A = 75°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified

Supplies = +15V, -15V; V_R = 0V; V_{AH} (Logic Level High) = 3.0V; V_{AL} (Logic Level Low) = +0.8V, V_L = +5V

For Test Conditions, consult Performance Characteristics

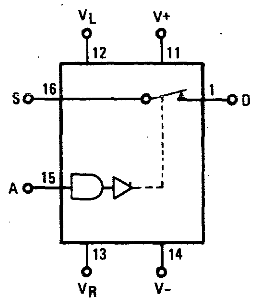
PARAMETER	TEMP	-55°C to +125°C			0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG SWITCH CHARACTERISTICS								
Analog Signal Range	Full	-15		+15	-15		+15	V
Ron, "ON" Resistance (Note 1a)	+25°C		50			50		Ω
	Full			75			75	Ω
Ron, "ON" Resistance (Note 1b)	+25°C		25			25		Ω
	Full			50			50	Ω
Ron, Channel-to-Channel Match (Note 1a)	+25°C		2	10		2	10	Ω
Ron, Channel-to-Channel Match (Note 1b)	+25°C		1	5		1	5	Ω
$I_{S(OFF)} = I_{D(OFF)}$, Off Input or Output Leakage Current	+25°C		0.8			0.8		nA
	Full		100	500		100	500	nA
$I_{D(ON)}$, On Leakage Current	+25°C		0.01			0.01		nA
	Full		2	500		2	500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.8			0.8	V
V_{AH}, Input High Threshold	Full	3.0			3.0			V
I_A, Input Leakage Current (High or Low)	Full		.01	1.0		.01	1.0	μA
SWITCHING CHARACTERISTICS								
t_{on}, Switch "ON" Time	+25°C		370	1000		370	1000	ns
t_{off}, Switch "OFF" Time	+25°C		280	500		280	500	ns
Charge Injection (Note 2)	+25°C		5	20		5		mV
"OFF Isolation" (Note 3)	+25°C	75	80			80		dB
"Crosstalk" (Note 3)	+25°C	80	88			88		dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		11			11		pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C		11			11		pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C		22			22		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C		0.5			0.5		pF
POWER REQUIREMENTS								
P_D, Quiescent Power Dissipation	+25°C		1.5			1.5		mW
I^+, +15V Quiescent Current	Full			0.3			0.5	mA
I^-, -15V Quiescent Current	Full			0.3			0.5	mA
I_L, +5V Quiescent Current	Full			0.3			0.5	mA
I_R, Gnd Quiescent Current	Full			0.3			0.5	mA

NOTES:
1. $V_{OUT} = \pm 10V$, I_{OUT} = 1mA
   a) For HI-5040 thru HI-5047
   b) For HI-5048 thru HI-5051, HI-5046A/5047A
2. V_{IN} = 0V, C_L = 10,000pF
3. $R_L = 100\Omega$, f= 100 KHz, $V_{IN} = 2\ V_{PP}$, C_L = 5pF

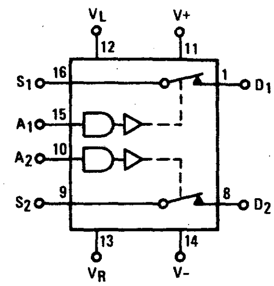
SWITCH FUNCTIONS

SWITCH STATES ARE FOR LOGIC "1" INPUT

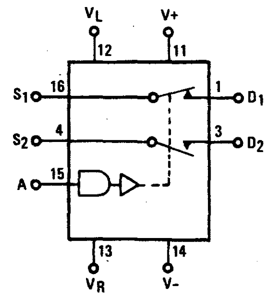
SPST
HI-5040 (75Ω)



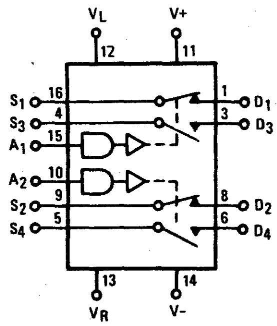
DUAL SPST
HI-5041 (75Ω)



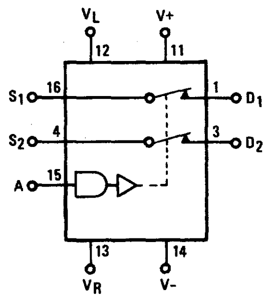
SPDT
HI-5042 (75Ω)



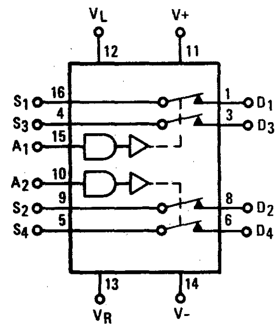
DUAL SPDT
HI-5043 (75Ω)



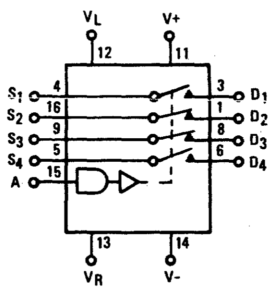
DPST
HI-5044 (75Ω)



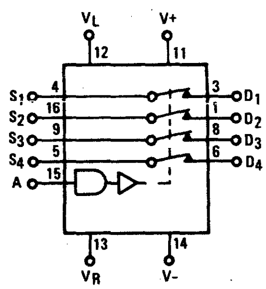
DUAL DPST
HI-5045 (75Ω)



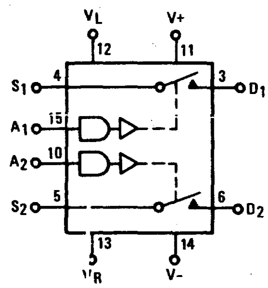
DPDT
HI-5046 (75Ω)
HI-5046A (30Ω)



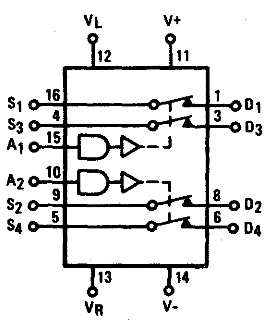
4PST
HI-5047 (75Ω)
HI-5047A (30Ω)



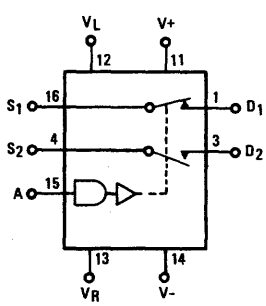
DUAL SPST
HI-5048 (30Ω)



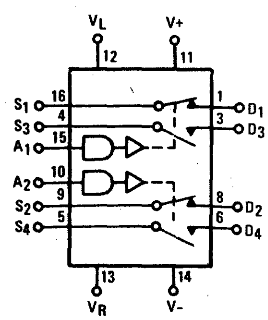
DUAL DPST
HI-5049 (30Ω)



SPDT
HI-5050 (30Ω)



DUAL SPDT
HI-5051 (30Ω)



HARRIS

HI-506/HI-507

Single 16/Differential 8 Channel CMOS Analog Multiplexers

FEATURES

- LOW ON RESISTANCE (TYP.) 170Ω
- WIDE ANALOG SIGNAL RANGE ±15V
- DIRECTLY TTL/CMOS COMPATIBLE 2.4V (LOGIC "1")
- ACCESS TIME (TYP.) 300ns
- HIGH CURRENT CAPABILITY (TYP.) 50mA
- BREAK-BEFORE-MAKE SWITCHING
- NO LATCH-UP

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- PRECISION INSTRUMENTATION
- DEMULTIPLEXING
- SELECTOR SWITCH

DESCRIPTION

These monolithic CMOS multiplexers each include an array of eight analog switches, a digital decode circuit for channel selection, a voltage reference for logic thresholds, and an ENABLE input for device selection when several multiplexers are present.

The Dielectric Isolation (DI) process used in fabrication of these devices eliminates the problem of latchup. Also, DI offers much lower substrate leakage and parasitic capacitance than conventional junction-isolated CMOS (See Application Note 521). With the low ON resistance (180Ω typical), this allows low static error, fast channel switching rates, and fast settling.

Switches are guaranteed to break-before-make, so two channels are never shorted together.

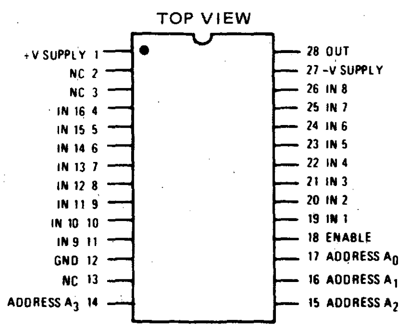
The switching threshold for each digital input is established by an internal +5V reference, providing a guaranteed minimum 2.4V for "1" and maximum 0.8V for "0". This allows direct interface without pullup resistors to signals from most logic families: CMOS, TTL, DTL and some PMOS. For protection against transient overvoltage, the digital inputs include a series 200Ω resistor and a diode clamp to each supply.

The HI-506 is a sixteen channel single-ended multiplexer, and the HI-507 is an eight channel differential version. Each device is packaged in a 28 pin DIP. The recommended supply voltage is ±15V, and reasonable performance is available down to ±7V; however, a power-up reset routine may be required for operation below ±10V. For more information, request Harris Analog Tech Brief # 20.

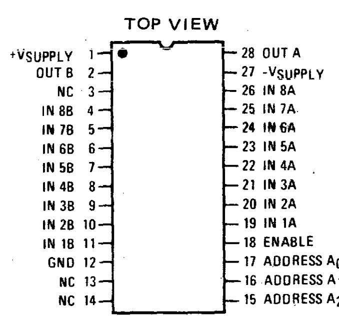
The HI-506/507 are specified for operation from 0°C to +70°C. The "-2" versions are specified from -55°C to +125°C. "Dash 8" (-8) designates -2 parts which have been screened per Mil-Std-883/Method 5004/Class B.

PINOUT

HI-506

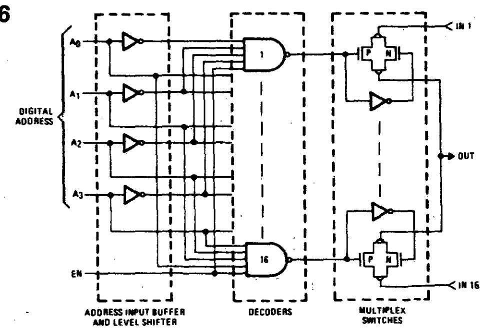


HI-507

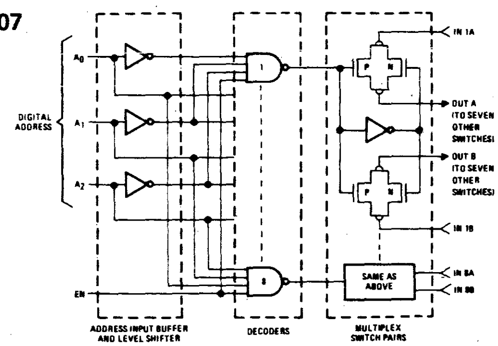


FUNCTIONAL DIAGRAM

HI-506



HI-507



ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 1 and 27	40V	Total Power Dissipation*	1200 mW
V_{EN}, V_A, Digital Input Overvoltage:		Operating Temperature:	
V_A { V_{Supply} (+) +4V		HI-506/HI-507-2	-55°C to +125°C
V_A { V_{Supply} (-) -4V		HI-506/HI-507-5	0°C to +75°C
Analog Input Overvoltage: (Note 6)		Storage Temperature	-65°C to +150°C
V_D or V_S { V_{Supply} (+) +2V			
V_D or V_S { V_{Supply} (-) -2V			

*Derate 19.7mW/°C above T_A = 110°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified: Supplies = +15V, -15V; V_{AH}(Logic Level High) = +2.4V, V_{AL}(Logic Level Low) = +0.8V. For Test Conditions, consult Performance Characteristics section.

		HI-506/HI-507-2 -55°C to +125°C			HI-506/HI-507-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS								
* V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
* R_{ON}, On Resistance (Note 1)	+25°C		170	300		270	400	Ω
	Full			400			500	Ω
* ΔR_{ON}, (Between Channels)	+25°C		6			6		%
* $I_{S(OFF)}$, Off Input Leakage Current	+25°C		0.03			0.03		nA
	Full			±50			±50	nA
* $I_{D(OFF)}$, Off Output Leakage Current	+25°C		0.3			1.0		nA
HI-506	Full			±500			±500	nA
HI-507	Full			±250			±250	nA
* $I_{D(ON)}$, On Channel Leakage Current	+25°C		0.3			1.0		nA
HI-506	Full			±500			±500	nA
HI-507	Full			±250			±250	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			+0.8			+0.8	V
V_{AH}, Input High Threshold	Full	+2.4			+2.4			V
* I_A, Input Leakage Current (High or Low)(Note 2)	Full			1.0			5.0	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		300	1000		300		ns
t_{OPEN}, Break-Before Make Delay	+25°C		80			80		ns
$t_{ON(EN)}$, Enable Delay (ON)	+25°C		300	1000		300		ns
$t_{OFF(EN)}$, Enable Delay (OFF)	+25°C		300	1000		300		ns
Settling Time (0.1%)	+25°C		1.2			1.2		μs
(0.025%)	+25°C		2.4			2.4		μs
"Off Isolation" (Note 3)	+25°C		75			75		dB
$C_{S(OFF)}$, Channel Input Capacitance	+25°C		4			4		pF
$C_{D(OFF)}$, Channel Output Capacitance HI-506	+25°C		44			44		pF
HI-507	+25°C		22			22		pF
C_A, Digital Input Capacitance	+25°C		2.2			2.2		pF
$C_{DS(OFF)}$, Input to Output Capacitance	+25°C		0.08			0.08		pF
POWER REQUIREMENTS								
* I+, Current Pin 1 (Note 4)	Full		1.7	3.0		3.4	5.0	mA
* I-, Current Pin 27 (Note 4)	Full		0.4	1.0		0.8	2.0	mA
* I+, Standby (Note 5)	Full		1.7	3.0		3.4	5.0	mA
* I-, Standby (Note 5)	Full		0.4	1.0		0.8	2.0	mA

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = -1mA
2. Digital Inputs are Mos Gates. Typical Leakage Less Than 1nA.
3. V_{EN} = 0.8V, R_L = 1K, C_L = 28pF, V_S = 7VRMS, f = 500kHz.
4. V_{EN} = 4.0V, All V_A = 4.0V
5. V_{EN} = 0V, All V_A = 0V
6. If Analog Input Overvoltage Conditions are Anticipated, Use of HI-506A/507A Protected Multiplexers is Recommended. See HI-506A/507A Data Sheet.

* 100% Tested for Dash 8 at +25°C and +125°C Only.

TRUTH TABLES

HI-506

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HARRIS

HI-506A/HI-507A

16 Channel CMOS Analog Multiplexer with Overvoltage Protection

FEATURES

- ANALOG/DIGITAL OVERVOLTAGE PROTECTION
- FAIL SAFE WITH POWER LOSS (NO LATCHUP)
- BREAK-BEFORE-MAKE SWITCHING
- DTL/TTL AND CMOS COMPATIBLE
- ANALOG SIGNAL RANGE ±15V
- ACCESS TIME (TYP.) 500ns
- SUPPLY CURRENT AT 1MHz ADDRESS TOGGLE (TYP.) 4mA
- STANDBY POWER (TYP.) 7.5mW

APPLICATIONS

- DATA ACQUISITION
- INDUSTRIAL CONTROLS
- TELEMETRY

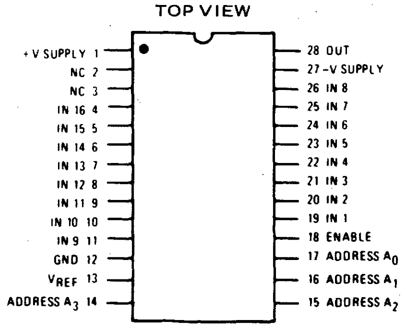
DESCRIPTION

The HI-506A and HI-507A are dielectrically isolated CMOS analog multiplexers incorporating an important feature; they withstand analog input voltages much greater than the supplies. This is essential in any system where the analog inputs originate outside the equipment. They can withstand a continuous input up to 10 volts greater than either supply, which eliminates the possibility of damage when supplies are off, but input signals are present. Equally important they can withstand brief input transient spikes of several hundred volts; which otherwise would require complex external protection networks. Necessarily, ON resistance is somewhat higher than similar unprotected devices, but very low leakage currents combine to produce low errors. Application Notes 520 and 521 further explain these features.

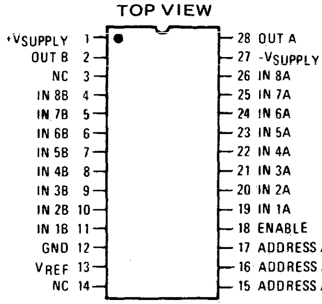
The HI-506A-2 and HI-507A-2 are specified over -55°C to +125°C while the -5 versions are specified over 0°C to +75°C.

PINOUT

HI-506A

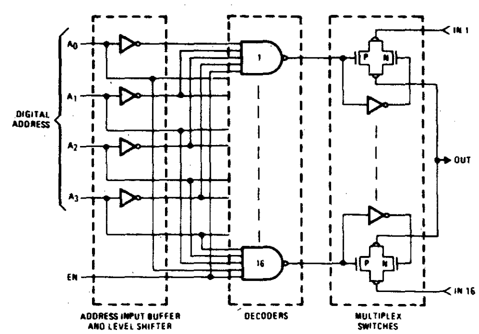


HI-507A

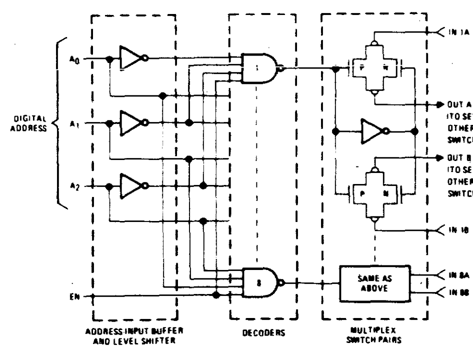


FUNCTIONAL DIAGRAM

HI-506A



HI-507A



ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 1 and 27	40V	Total Power Dissipation	1200mW
V_{REF} to Ground V+ to Ground	+20V	Operating Temperature	
V_{EN}, V_A, Digital Input Overvoltage:		HI-506A/507A-2	-55°C to +125°C
V_A V_{Supply} (+)	+4V	HI-506A/507A-5	0°C to +75°C
V_A V_{Supply} (−)	-4V	Storage Temperature	-65°C to +150°C
Analog Overvoltage:			
V_S V_{Supply} (+)	+20V		
V_S V_{Supply} (−)	-20V		

ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

Supplies = +15V, -15V; V_{REF} (Pin 13) = Open; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics section.

PARAMETER	TEMP.	HI-506A/507A-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-506A/507A-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON}, On Resistance (Note 1)	+25°C		1.2	1.5		1.5	1.8	KΩ
	Full		1.5	2.0		1.8	2.0	KΩ
*$I_{S\,(OFF)}$, Off Input Leakage Current	+25°C		0.03			0.03		nA
	Full			±50			±50	nA
*$I_{D\,(OFF)}$, Off Output Leakage Current	+25°C		1.0			1.0		nA
HI-506A	Full			±500			±500	nA
HI-507A	Full			±250			±250	nA
*$I_{D\,(OFF)}$ with Input Overvoltage Applied (Note 2)	+25°C		4.0			4.0		nA
	Full			2.0				μA
*$I_{D\,(ON)}$, On Channel Leakage Current	+25°C		0.1			0.1		nA
HI-506A	Full			±500			±500	nA
HI-507A	Full			±250			±250	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold TTL Drive	Full			0.8			0.8	V
V_{AH}, Input High Threshold (Note 7)	Full	4.0			4.0			V
V_{AL} MOS Drive (Note 3)	+25°C			0.8			0.8	V
V_{AH} MOS Drive (Note 3)	+25°C	6.0			6.0			V
*I_A, Input Leakage Current (High or Low)	Full			1.0			5.0	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		0.5	1.0		0.5		μs
t_{OPEN}, Break-Before Make Delay	+25°C		80			80		ns
$t_{ON\,(EN)}$, Enable Delay (ON)	+25°C		300			300		ns
$t_{OFF\,(EN)}$, Enable Delay (OFF)	+25°C		300			300		ns
Settling Time (0.1%)	+25°C		1.3			1.3		μs
(0.025%)	+25°C		4.4			4.4		μs
"Off Isolation" (Note 4)	+25°C		65			65		dB
$C_{S\,(OFF)}$, Channel Input Capacitance	+25°C		5			5		pF
$C_{D\,(OFF)}$, Channel Output Capacitance HI-506A	+25°C		50			50		pF
HI-507A	+25°C		25			25		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS\,(OFF)}$, Input to Output Capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7.5			7.5		mW
*I+, Current Pin 1 (Note 5)	Full		0.5	2.0		0.5	5.0	mA
*I-, Current Pin 27 (Note 5)	Full		0.02	1.0		0.02	2.0	mA
*I+, Standby (Note 6)	Full		0.5	2.0		0.5	5.0	mA
*I-, Standby (Note 6)	Full		0.02	1.0		0.02	2.0	mA

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = - 100 μA.
2. Analog Overvoltage = ±33V.
3. V_{REF} = +10V.
4. V_{EN} = 0.8V, R_L = 1K, C_L = 7pF, V_S = 3VRMS, f = 500KHz.
5. V_{EN} = +4.0V.
6. V_{EN} = 0.8V.
7. To drive from DTL/TTL circuits, 1KΩ pull-up resistors to +5.0V supply are recommended.

* 100% Tested for Dash 8 at +25°C and +125°C Only.

TRUTH TABLES

HI-506A

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507A

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HARRIS

HI-506L/HI-507L

Single 16/Differential 8 Channel CMOS Analog Multiplexers With Latches And Overvoltage Protection

FEATURES

- Analog Overvoltage protection
- Resettable Latches ($\overline{RS}$)
- TTL/DTL and CMOS Compatible
- Failsafe for conditions of Overvoltage & Loss of Power
- No SCR Latch-up
- Break-before-make switching
- Microprocessor Bus compatible
- Very low leakage - $I_{D(off)} \leq$ 8nA (typ) over full temp range
- Access time - t_A = 500nS (typ)
- Minimum write pulse width ($\overline{WR}$) = 300 nS
- OFF isolation = −100dB, typ @ 10kHz

DESCRIPTION

These monolithic CMOS multiplexers feature on-board address latches, plus overvoltage protection for the analog inputs and the output as well. Each mode accomodates digital inputs for channel selection and an Enable input for device selection under program control. In addition, Write ($\overline{WR}$) and Reset ($\overline{RS}$) inputs allow the program to store or clear the channel address.

The overvoltage performance of these multiplexers is particularly useful in redundant systems, where the inputs and output should present a very high impedance when power is off. This is achieved by a switch cell with three MOSFET's in series, rather than the conventional single transmission gate design.

Each channel can withstand a DC overvoltage up to a magnitude of 10VDC greater than the power supply (or to ± 25VDC with power off). An OFF channel remains OFF for this condition. If the channel is ON, the output voltage is clamped below the supply rail, which protects the load circuit.

The HI-506L offers 16 single-ended channels, and the HI-507L is an 8 channel differential version. The recommended supply voltages are ± 15V, through operation at reduced levels or with a single supply may also be implemented. The package is a 28 pin ceramic or plastic DIP.

Each product is specified for the commercial temperature range (0°C to +75°C, −5 suffix) and the military range (−55°C to +125°C, −2 suffix). Military parts screened per MIL-STD-883 method 5004, Class B are offered with a "−8" suffix.

PINOUT

HI-506L

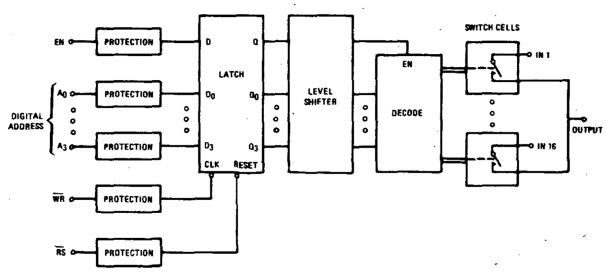
Signal	Pin	Pin	Signal
$+V_{SUPPLY}$	1	28	OUT
NC	2	27	$-V_{SUPPLY}$
$\overline{RS}$	3	26	IN 8
IN 16	4	25	IN 7
IN 15	5	24	IN 6
IN 14	6	23	IN 5
IN 13	7	22	IN 4
IN 12	8	21	IN 3
IN 11	9	20	IN 2
IN 10	10	19	IN 1
IN 9	11	18	ENABLE
GND	12	17	ADDRESS A_0
WR	13	16	ADDRESS A_1
ADDRESS A_3	14	15	ADDRESS A_2

HI-507L

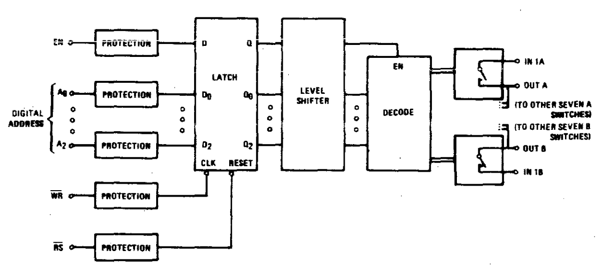
Signal	Pin	Pin	Signal
$+V_{SUPPLY}$	1	28	OUT A
OUT B	2	27	$-V_{SUPPLY}$
$\overline{RS}$	3	26	IN 8A
IN 8B	4	25	IN 7A
IN 7B	5	24	IN 6A
IN 6B	6	23	IN 5A
IN 5B	7	22	IN 4A
IN 4B	8	21	IN 3A
IN 3B	9	20	IN 2A
IN 2B	10	19	IN 1A
IN 1B	11	18	ENABLE
GND	12	17	ADDRESS A_0
$\overline{WR}$	13	16	ADDRESS A_1
NC	14	15	ADDRESS A_2

FUNCTIONAL DIAGRAM

HI-506L



HI-507L



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 1 and 27	44V	Operating Temperature	
Digital Input Overvoltage, V_A, V_{EN}, $V_{\overline{RS}}$, $V_{\overline{WR}}$:			
V supply (+)	+4V	HI-506L/507L-2	−55°C to 125°C
V supply (−)	−4V	HI-506L/507L-5	0°C to 75°C
Analog Overvoltage		Storage Temperature	−65°C to +150°C
Input to Ground	±25VDC		
Total Power Dissipation* (Package)	1200mW	*Derate-8mW/°C above T_A = +75°C	

ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

+V supply = 15V, −V supply = −15V, V_{AH} (Logic High) = 2.0V, V_{AL} (Logic Low) = 0.8V

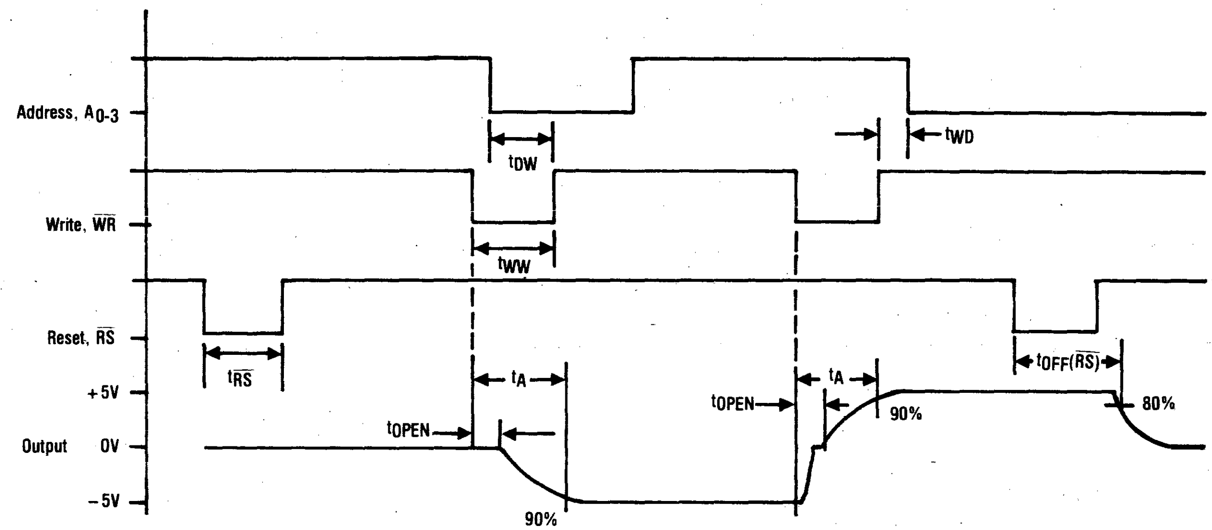
		HI-506L/507L-2 −55°C to +125°C			HI-506L/507L-5 0°C to +75°C			
PARAMETER	**TEMP**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
ANALOG CHANNEL CHARACTERISTICS								
V_S Analog Signal Range	Full		±10			±10		V
R_{ON}, ON Resistance (Note1)	+25°C			1.2			1.5	KΩ
	Full			1.8			1.8	KΩ
$\triangle R_{ON}$, Change In R_{ON} (Note 2) between channels	+25°C		5			5		%
$I_{S(off)}$, OFF input leakage current	+25°C			10			10	nA
	Full		7	50		7	50	nA
$I_{D(off)}$, OFF output leakage current	+25°C			10			10	nA
HI-506L	Full		8	200		8	200	nA
HI-507L	Full			100			100	nA
$I_{D(On)}$, ON Channel leakage current	+25°C		5	10		5	10	nA
HI-506L	Full		10	200		10	200	nA
HI-507L	Full			100			100	nA
FAULT CHARACTERISTICS								
$I_{S(Off)}$, with Power OFF	Full		10	1000		10	5000	nA
$I_{S(Off)}$, overvoltage (Note 3)	Full		10	750		10	2500	nA
$I_{D(Off)}$, with input over-	+25°C		5			5		nA
voltage applied (Note 3)	Full		10	750		10	2500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full		1.4	0.8		1.4	0.8	V
V_{AH}, Input High Threshold	Full	2.0	1.4		2.0	1.4		V
I_{AH}, Input High Current	Full		10	40		10	40	µA
I_{AL}, Input Low Current	Full		40	200		40	200	µA
DYNAMIC SWITCHING CHARACTERISTICS								
t_a, Access Time	+25°C		0.5	1.0		0.5	1.0	µS
t_{OPEN}, Break-Before-Make	+25°C	.025	0.1		0.25	0.1		µS
t_{ON}, (EN, $\overline{WR}$), Enable Delay (ON)	+25°C			1.0			1.0	µS
t_{OFF}, (EN, $\overline{RS}$), Enable and Reset Delay (OFF)	+25°C		0.5	1.0		0.5	1.0	µS
Settling Time (±0.1%)	+25°C		1.0			1.0		µS
(±0.01%)	+25°C		1.75			1.75		µS
Q Charge Injection	+25°C		10			10		pC
OFF Isolation (Note 4)	+25°C		−72			−72		dB
OFF Isolation POWER OFF (Note 5)	+25°C		−56			−56		dB
$C_{S(Off)}$, Channel Input Cap.	+25°C		5			5		pF
$C_{D(Off)}$, Channel Output Cap.								
HI-506L	+25°C		40			40		
HI-507L	+25°C		20			20		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(Off)}$, Input to Output capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation (Note 6)	Full		60	100		60	100	mW
I +, Current Pin 1 (Note 6)	Full		3.7	6.0		3.7	6.0	mA
I −, Current Pin 27 (Note 6)	Full		0.3	0.6		0.3	0.6	mA

Notes:
1. $V_{OUT} = \pm 10V$, I out = −100 µa
2. $\triangle R_{ON} = \frac{R_{ON}(Max) - R_{ON}(Min)}{R_{ON}(Avg)}$ $V_{IN} = \pm 10V$
3. Analog Overvoltage = ±25V
4. $V_{EN} = 0.8V$, $R_L = 1K\Omega$, $C_L = 50pF$
   V_S = 3Vrms, f = 500 kHz
   Off isolation = $20 \log \frac{|V_D|}{|V_S|}$
5. V+, V− = 0V, $R_L = 1K\Omega$
   $C_L = 50pF$, V_S = 3Vrms, f = 500 kHz.
6. See Test Circuit #8 for high toggle frequency applications.

Minimum Timing Requirements

PARAMETER	MEASURED TERMINAL	MIN LIMITS FULL TEMP RANGE	UNITS
t_{WW}, Write Pulse Width	$\overline{WR}$	300	nS
t_{DW}, A, EN Data Valid To WRITE (Stabilization Time)	A0, A1, A2, A3, EN $\overline{WR}$	225	nS
t_{WD}, A, EN Data Valid To WRITE (hold Time)	$\overline{WR}$ A0, A1, A2, A3, EN	100	nS
t_{RS}, RESET pulse width	$\overline{RS}$	400	nS

Timing Requirements



1. Inputs to HI-506L (507L) : Channel 1 = −5V; Channel 16, (8) = +5V.
2. $+V_{SUPPLY}$ = +15V; $-V_{SUPPLY}$ = −15V.
3. Logic Levels: V_{AL} = 0V; V_{AH} = +2.0V.
4. Time intervals are measured between 50% levels unless otherwise noted.
5. Minimum values for $t_{\overline{RS}}$, t_{DW}, t_{WW} and t_{WD} are guaranteed separately but not simultaneously.

Figure 1

SCHEMATIC DIAGRAM

Switch Cell

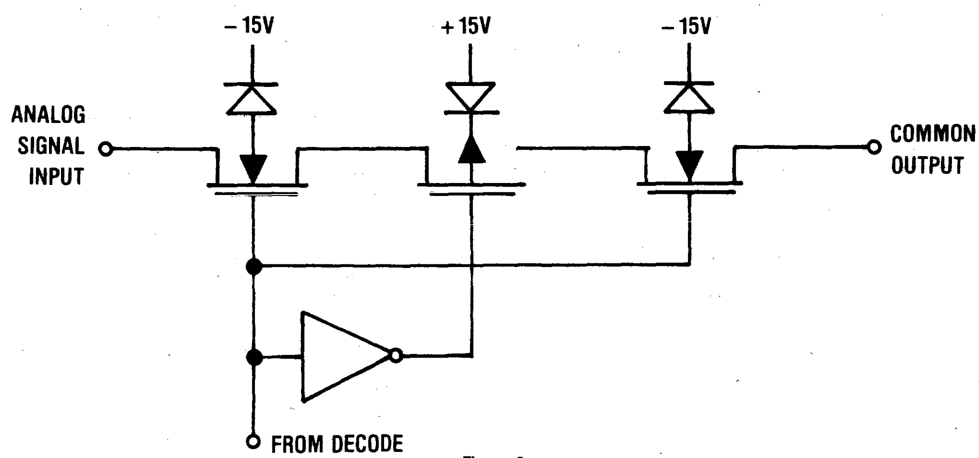


Figure 2

506L

A3	A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	OUTPUT - ON CHANNEL
X	X	X	X	L	L	H	None
X	X	X	X	X	_/¯	H	Previous On Channel.
X	X	X	X	X	X	L	None (latches cleared)
L	L	L	L	H	L	H	Channel 1
L	L	L	H	H	L	H	Channel 2
L	L	H	L	H	L	H	Channel 3
L	L	H	H	H	L	H	Channel 4
L	H	L	L	H	L	H	Channel 5
L	H	L	H	H	L	H	Channel 6
L	H	H	L	H	L	H	Channel 7
L	H	H	H	H	L	H	Channel 8
H	L	L	L	H	L	H	Channel 9
H	L	L	H	H	L	H	Channel 10
H	L	H	L	H	L	H	Channel 11
H	L	H	H	H	L	H	Channel 12
H	H	L	L	H	L	H	Channel 13
H	H	L	H	H	L	H	Channel 14
H	H	H	L	H	L	H	Channel 15
H	H	H	H	H	L	H	Channel 16

507L

A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	OUTPUT - ON CHANNEL PAIR
X	X	X	L	L	H	None
X	X	X	X	_/¯	H	Previous On Channel.
X	X	X	X	X	L	None (latches cleared)
L	L	L	H	L	H	Channel 1A and 1B
L	L	H	H	L	H	Channel 2A and 2B
L	H	L	H	L	H	Channel 3A and 3B
L	H	H	H	L	H	Channel 4A and 4B
H	L	L	H	L	H	Channel 5A and 5B
H	L	H	H	L	H	Channel 6A and 6B
H	H	L	H	L	H	Channel 7A and 7B
H	H	H	H	L	H	Channel 8A and 8B

DESCRIPTION AND APPLICATION

The switch cell of the HI-506L/507L has a different structure than earlier Harris designs (HI-506, HI506A). The new switch (Figure 2) consists of an N-channel, P-channel and N-channel MOSFET in series, as opposed to the transmission gate configuration with an N and P-channel device in parallel. The series N-P-N switch offers higher Off Isolation with power off, and better fault performance. Channel overvoltage protection is inherent since one of the three MOSFETs turn off in the presence of overvoltage. this turn-off process begins well below the supply rail so the V_{IN} range is less than the power supply range. Electrical performance is guaranteed to ±10V for each channel, and the usable range extends above ±11 Volts.

The address inputs A_0, A_1, A_2, A_3, and ENABLE are latched into an internal buffer when $\overline{WR}$ goes high. Each latch output is level shifted into the decode section, which activates the appropriate channel. The device may be reset (all channels OFF) by taking $\overline{RS}$ low. Usually, $\overline{RS}$ is tied to the system RESET line, to assure that all channels are OFF following a turn-on of power. The reset function overrides all others, just as $\overline{WR}$ overrides the address inputs (A_0-A_3 and EN are ignored when $\overline{WR}$ is high). With $\overline{WR}$ low and $\overline{RS}$ high, the switches respond immediately to a change in channel address; i.e. the latches are "transparent". Refer to Figure 1.

HARRIS

HI-508/HI-509

Single 8/Differential 4 Channel CMOS Analog Multiplexer

FEATURES

- FAST ACCESS 220ns
- FAST SETTLING (0.01%) 600ns
- LOW R_{ON} 180 Ω
- BREAK-BEFORE-MAKE SWITCHING
- NO LATCH-UP
- TTL/CMOS COMPATIBLE 2.4V (LOGIC "1")

APPLICATIONS

- PRECISION INSTRUMENTS
- DATA ACQUISITION SYSTEMS
- TELEMETRY

DESCRIPTION

These monolithic CMOS multiplexers each include an array of eight analog switches, a digital decode circuit for channel selection, a voltage reference for logic thresholds, and an ENABLE input for device selection when several multiplexers are present.

The Dielectric Isolation (DI) process used in fabrication of these devices eliminates the problem of latch-up. Also, DI offers much lower substrate leakage and parasitic capacitance than conventional junction-isolated CMOS (see Application Note 521). Combined with the low ON resistance (180Ω typical), these benefits allow low static error, fast channel switching rates, and fast settling.

Switches are guaranteed to break-before-make, so two channels are never shorted together.

The switching threshold for each digital input is established by an internal +5V reference, providing a guaranteed min. 2.4V for "1" and max. 0.8V for "0". This allows direct interface without pull-up resistors to signals from most logic families: CMOS, TTL, DTL, and some PMOS. For protection against transient overvoltage, the digital inputs include a series 200Ω resistor and a diode clamp to each supply.

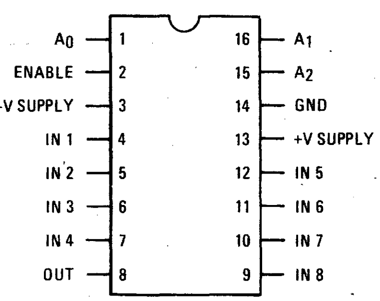
The HI-508 is an eight channel single-ended multiplexer, and the HI-509 is a four channel differential version. The recommended supply voltage is ±15V; however, reasonable performance is available down to ±7V. Each device is packaged in a 16 pin DIP.

The HI-508/509-5 are specified for operation from 0°C to 70°C. The "-2" versions are specified from -55°C to +125°C. "Dash 8" (-8) designates -2 parts which have been screened per MIL-STD-883/Method 5004/Class B.

PINOUTS

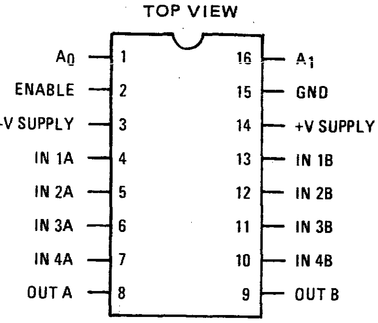
HI-508

TOP VIEW



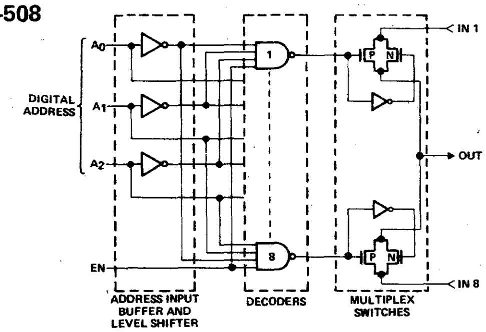
HI-509

TOP VIEW

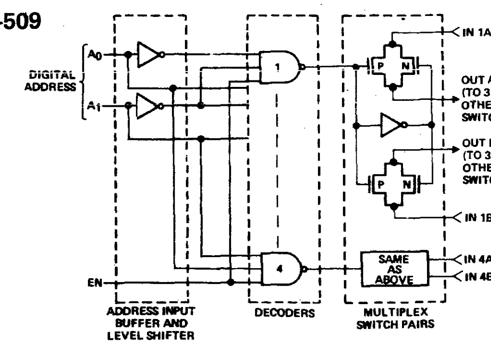


FUNCTIONAL DIAGRAMS

HI-508



HI-509



ABSOLUTE MAXIMUM RATINGS (Note 1)

$V_{Supply}(+)$ to $V_{Supply}(-)$	40V	Power Dissipation *	750mW
$V_{Supply}(+)$ to GND	20V	Operating Temperature Ranges:	
$V_{Supply}(-)$ to GND	20V	HI-508/509-2, -8	-55°C to +125°C
		HI-508/509-5, -6	0°C to 70°C
Digital Input Overvoltage:		HI-508/509-1	-55°C to +200°C
V_{EN}, V_A $V_{Supply}(+)$	+4V		
V_{EN}, V_A $V_{Supply}(-)$	-4V	Storage Temperature Range	-65°C to +150°C
Analog Input Overvoltage (Note 6):			
V_D, V_S $V_{Supply}(+)$	+2V		
V_D, V_S $V_{Supply}(-)$	-2V		

*Derate 9.6mW/°C above T_A = 95°C

ELECTRICAL CHARACTERISTICS Unless otherwise specified: Supplies = ± 15V, GND = 0V

		HI-508/HI-509-2 -55°C to +125°C			HI-508/HI-509-5 0°C to +70°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON}, On Resistance	+25°C		180	300		180	400	Ω
	Full		230	400		230	500	Ω
ΔR_{ON}, Any Two Channels	+25°C		5			5		%
$I_{S(OFF)}$, Off Input Leakage Current (Note 2)	+25°C			10			10	nA
	Full			50			50	nA
$I_{D(OFF)}$, Off Output Leakage Current	+25°C							
HI-508	Full		10	200		10	200	nA
HI-509	Full		10	100		10	100	nA
$I_{D(ON)}$, On Channel Leakage Current	+25°C							
HI-508	Full		10	200		10	200	nA
HI-509	Full		10	100		10	100	nA
I_{DIFF}, Differential Off Output Leakage Current (HI-509 Only)	+25°C		1	5		1	5	nA
	Full		5	50		5	50	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AH}, High Threshold	Full	2.4			2.4			V
V_{AL}, Low Threshold	Full			0.8			0.8	V
I_A, Input Leakage Current (High or Low) (Note 3)	Full			1			1	µA
SWITCHING CHARACTERISTICS								
t_A, Access (Transition) Time	+25°C		220	500		220	1000	ns
	Full			1000				ns
t_{OPEN}, Break-Before-Make Interval	+25°C		70			70		ns
$t_{ON(EN)}$, Enable Turn-On	+25°C		210			210		ns
$t_{OFF(EN)}$, Enable Turn-Off	+25°C		180			180		ns
t_S, Settling Tme to 0.1%	+25°C		360			360		ns
to 0.01%	+25°C		600			600		ns
Off Isolation (Note 4)	+25°C		68			68		dB
$C_{S(OFF)}$, Channel Input Capacitance	+25°C		5			5		pF
$C_{D(OFF)}$, Channel Output Capacitance	+25°C		21			21		pF
C_A, Digital Input Capacitance	+25°C		3			3		pF
$C_{DS(OFF)}$, Input to Output Capacitance	+25°C		.08			.08		pF
POWER REQUIREMENTS								
I+, Positive Supply Current (Note 5)	Full			2			2	mA
I-, Negative Supply Current (Note 5)	Full			1			1	mA
P_D, Power Dissipation	Full			45			45	mW

NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Ten nanoamps is the practical limit for high speed measurement in the production test environment. Actually, I_S (off) is below 100pA for most devices, at 25°C.
3. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at 25°C.
4. V_{EN} = 0.8V, R_1 = 1K, C_1 = 15pF, V_S = 7V_{RMS}, f = 500kHz. Worst case isolation occurs on channel 4 (HI-508) and channels 4, 8 (HI-509), due to proximity of the output pins.
5. V_{EN} = 0V or 5V. All V_A = 0.
6. If an overvoltage condition is anticipated (analog input exceeds either power supply voltage), the HARRIS HI-508A/509A multiplexers are recommended.

TRUTH TABLES

HI-508

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509

A_1	A_0	EN	"ON" CHANNEL
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

HARRIS

HI-508A/509A

8 Channel CMOS Analog Multiplexers with Overvoltage Protection

FEATURES

- ANALOG/DIGITAL OVERVOLTAGE PROTECTION
- FAIL SAFE WITH POWER LOSS (NO LATCHUP)
- BREAK-BEFORE-MAKE SWITCHING
- DTL/TTL AND CMOS COMPATIBLE
- ANALOG SIGNAL RANGE ±15V
- ACCESS TIME (TYP.) 500ns
- SUPPLY CURRENT AT 1MHz ADDRESS TOGGLE (TYP.) 4mA
- STANDBY POWER (TYP.) 7.5mW

APPLICATIONS

- DATA ACQUISITION
- INDUSTRIAL CONTROLS
- TELEMETRY

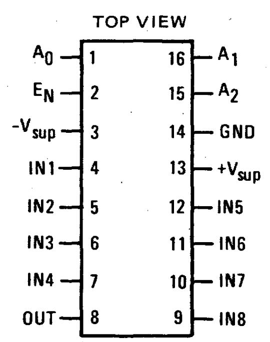
DESCRIPTION

The HI-508A and HI-509A are dielectrically isolated CMOS analog multiplexers incorporating an important feature; they withstand analog input voltages much greater than the supplies. This is essential in any system where the analog inputs originate outside the equipment. They can withstand a continuous input up to 10 volts greater than either supply, which eliminates the possibility of damage when supplies are off, but input signals are present. Equally important, they can withstand brief input transient spikes of several hundred volts; which otherwise would require complex external protection networks. Necesarily, ON resistance is somewhat higher than similar unprotected devices, but very low leakage currents combine to produce low errors. Application Notes 520 and 521 further explain these features.

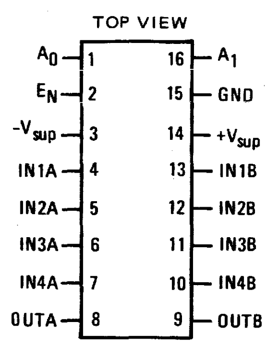
The HI-508A-2 and HI-509A-2 are specified over -55°C to +125°C while the -5 versions are specified over 0°C to +75°C.

PINOUT

HI-508A

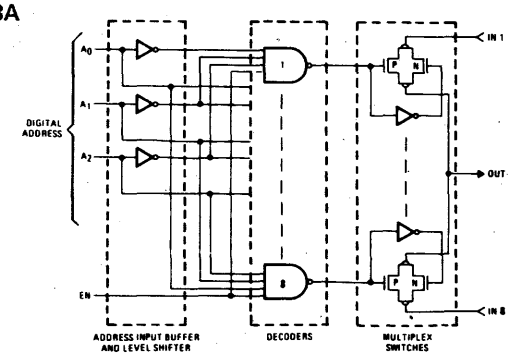


HI-509A

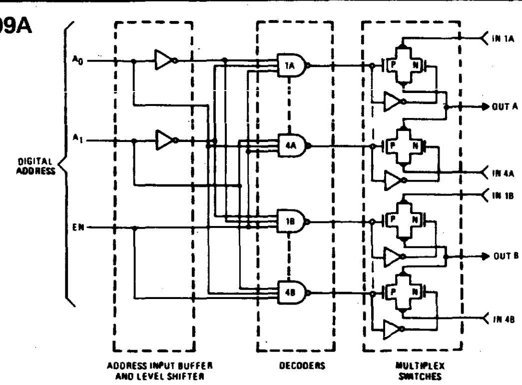


FUNCTIONAL DIAGRAM

HI-508A



HI-509A



ABSOLUTE MAXIMUM RATINGS

Voltage between Supply Pins	40V
V+ to Ground	20V
V_{EN}, V_A, Digital Input Overvoltage:	
V_A	$V_{Supply}(+)$ +4V
	$V_{Supply}(-)$ -4V
Analog Input Overvoltage:	
V_S	$V_{Supply}(+)$ +20V
	$V_{Supply}(-)$ -20V

Total Power Dissipation*	725 mW
Operating Temperature:	
HI-508A/HI-509A-2	-55°C to +125°C
HI-508A/HI-509A-5	0°C to +75°C
Storage Temperature	-65°C to +150°C

*Derate 9.6mW/°C above T_A = 95°C

ELECTRICAL CHARACTERISTICS (Unless Otherwise Specified)

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characterisitcs section.

		HI-508A/509A-2 -55°C to +125°C			HI-508A/509A-5 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
* R_{ON}, On Resistance (Note 1)	+25°C		1.2	1.5		1.5	1.8	KΩ
	Full		1.5	1.8		1.8	2.0	KΩ
* $I_{S(OFF)}$, Off Input Leakage Current	+25°C		0.03			0.03		nA
	Full			±50			±50	nA
* $I_{D(OFF)}$, Off Output Leakage Current	+25°C		1.0			1.0		nA
HI-508A	Full			±250			±250	nA
HI-509A	Full			±125			±125	nA
* $I_{D(OFF)}$ with Input Overvoltage Applied (Note 2)	+25°C		4.0			4.0		nA
	Full			2.0				μA
* $I_{D(ON)}$, On Channel Leakage Current	+25°C		0.1			0.1		nA
HI-508A	Full			±250			±250	nA
HI-509A				±125			±125	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold (Note 6)	Full			0.8			0.8	V
V_{AH}, Input High Threshold (Note 6)	Full	4.0			4.0			V
* I_A, Input Leakage Current (High or Low)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		0.5	1.0		0.5		μs
t_{OPEN}, Break - Before Make Delay	+25°C		80			80		ns
$t_{ON(EN)}$, Enable Delay (ON)	+25°C		300			300		ns
$t_{OFF(EN)}$, Enable Delay (OFF)	+25°C		300			300		ns
Settling Time (0.1%)	+25°C		1.2			1.2		μs
(0.025%)	+25°C		3.5			3.5		μs
"OFF Isolation" (Note 3)	+25°C		65			65		dB
$C_{S(OFF)}$, Channel Input Capacitance	+25°C		5			5		pF
$C_{D(OFF)}$, Channel Output Capacitance								
HI-508A	+25°C		25			25		pF
HI-509A	+25°C		12			12		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Input to Output Capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7.5			7.5		mW
*I+, Current (Note 4)	Full		0.5	2.0		0.5	5.0	mA
*I-, Current (Note 4)	Full		0.02	1.0		0.02	2.0	mA
*I+, Standby (Note 5)	Full		0.5	2.0		0.5	5.0	mA
*I-, Standby (Note 5)	Full		0.02	1.0		0.02	2.0	mA

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = -100μA
2. Analog Overvoltage = ±33V
3. V_{EN} = 0.8V, R_L = 1K, C_L = 7pF, V_S = 3V RMS, f = 500KHz
4. V_{EN} = +4.0V
5. V_{EN} = 0.8V
6. To drive from DTL/TTL Circuits, 1KΩ pull-up resistors to +5.0V supply are recommended

* 100% Tested for Dash 8 at +25°C and +125°C Only.

TRUTH TABLES

HI-508A

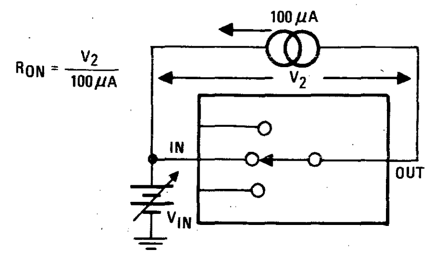
A_2	A_1	A_0	E_N	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509A

A_1	A_0	EN	ON SWITCH PAIR
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

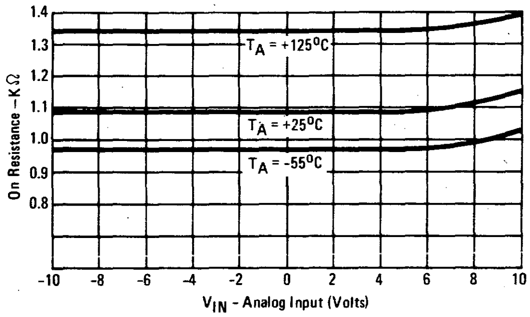
UNLESS OTHERWISE SPECIFIED: $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$

TEST CIRCUIT NO. 1

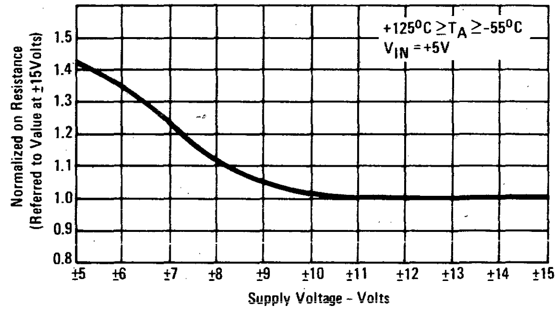


ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

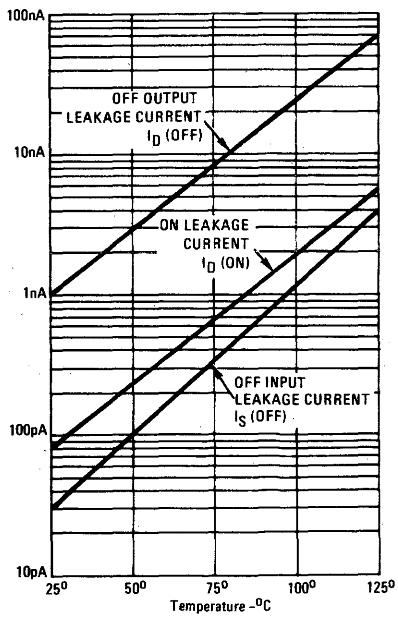
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



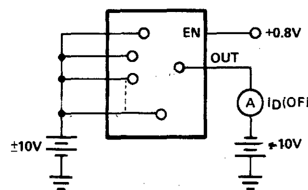
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



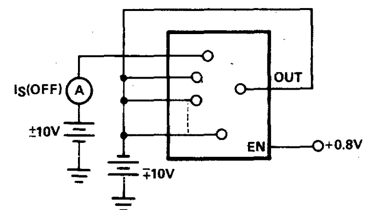
LEAKAGE CURRENT vs. TEMPERATURE



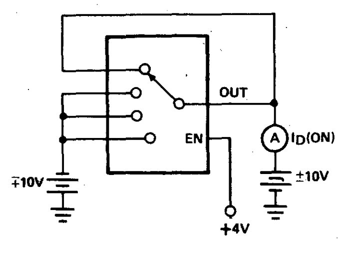
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 3*

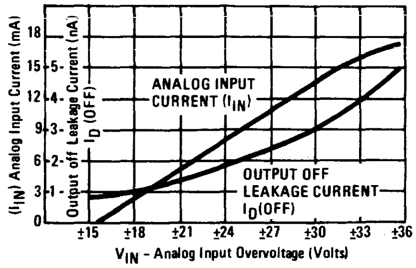


TEST CIRCUIT NO. 4*



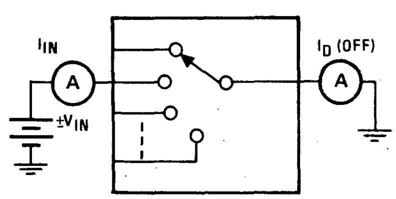
***Two measurements per channel: +10V/-10V and -10V/+10V. (Two measurements per device for ID(OFF): +10V/-10V and -10V/+10V.)**

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



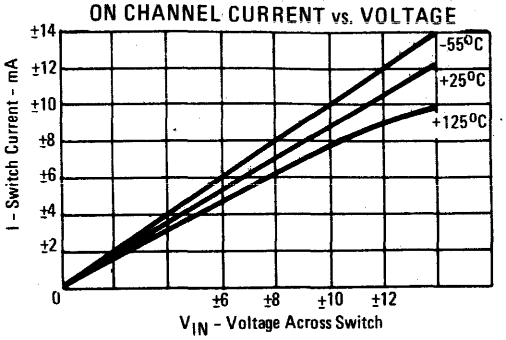
ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

TEST CIRCUIT NO. 5



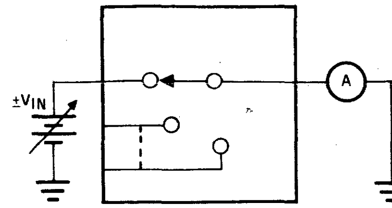
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (continued)

ON CHANNEL CURRENT vs. VOLTAGE

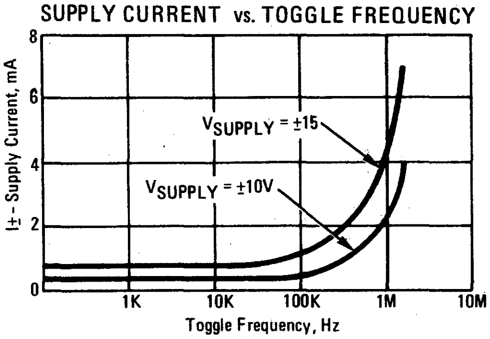


TEST CIRCUIT NO. 6

ON CHANNEL CURRENT vs. VOLTAGE

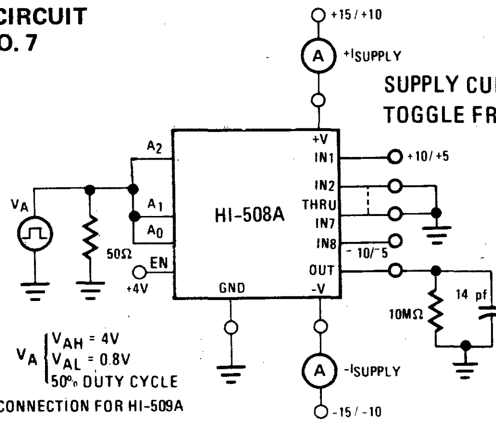


SUPPLY CURRENT vs. TOGGLE FREQUENCY



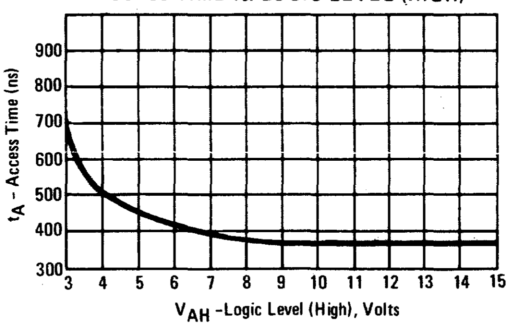
TEST CIRCUIT NO. 7

SUPPLY CURRENT vs. TOGGLE FREQUENCY



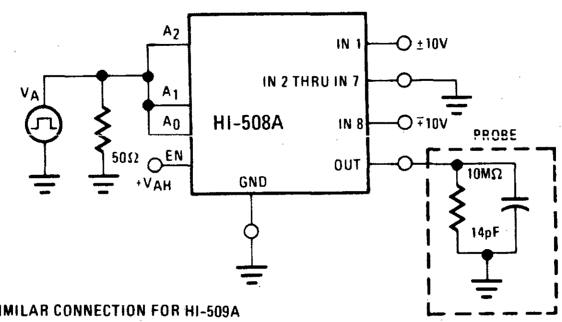
*SIMILAR CONNECTION FOR HI-509A

ACCESS TIME vs. LOGIC LEVEL (HIGH)



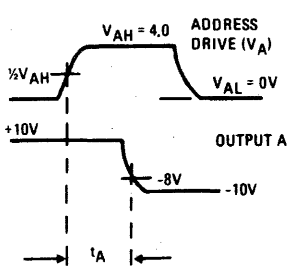
TEST CIRCUIT NO. 8

ACCESS TIME vs. LOGIC LEVEL(HIGH)

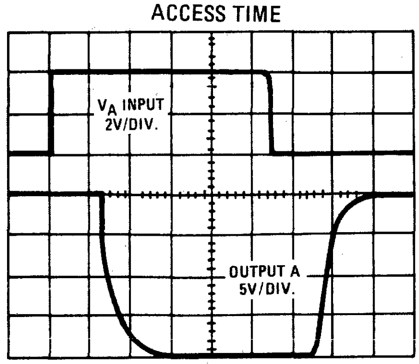


* SIMILAR CONNECTION FOR HI-509A

SWITCHING WAVEFORMS



ACCESS TIME



200ns/Div.

HARRIS

HI-508L/HI-509L

Single 8/Differential 4 Channel CMOS Analog Multiplexers With Latches And Overvoltage Protection

FEATURES

- Analog Overvoltage protection
- Resettable Latches ($\overline{RS}$)
- TTL/DTL and CMOS Compatible
- Failsafe for conditions of Overvoltage & Loss of Power
- No SCR Latch-up
- Break-before-make switching
- Microprocessor Bus compatible
- Very low leakage - $I_{D(off)} \leq$ 8nA (typ) over full temp range
- Access time - t_A = 500nS (typ)
- Minimum write pulse width ($\overline{WR}$) = 300 nS
- OFF isolation = −100dB, typ @ 10kHz

DESCRIPTION

These monolithic CMOS multiplexers feature on-board address latches, plus over-voltage protection for the analog inputs and the output as well. Each mode accomodates digital inputs for channel selection and an Enable input for device selection under program control. In addition, Write ($\overline{WR}$) and Reset ($\overline{RS}$) inputs allow the program to store or clear the channel address.

The overvoltage performance of these multiplexers is particularly useful in redundant systems, where the inputs and output should present a very high impedance when power is off. This is achieved by a switch cell with three MOSFET's in series, rather thant he conventional single transmission gate design.

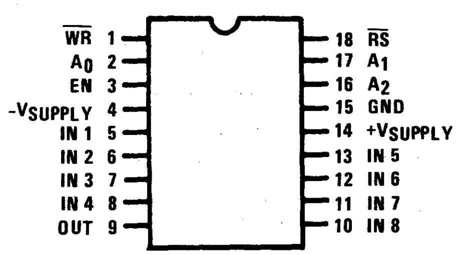
Each channel can withstand a DC overvoltage up to a magnitude of 10VDC greater than the power supply (or to ± 25VDC with power off). An OFF channel remains OFF for this condition. If the channel is ON, the output voltage is clamped below the supply rail, which protects the load circuit.

The HI-508L offers 8 single-ended channels, and the HI-509L is a 4 channel differential version. The recommended supply voltages are ± 15V, through operation at reduced levels or with a single supply may also be implemented. The package is an 18 pin ceramic or epoxy DIP.

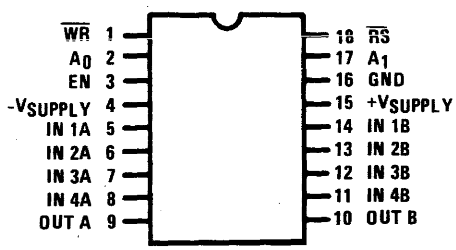
Each product is specified for the commercial temperature range (0°C to +75°C, −5 suffix) and the military range (−55°C to +125°C, −2 suffix). Military parts screened per MIL-STD-883 method 5004, Class B are offered with a "−8" suffix.

PINOUT

HI-508L

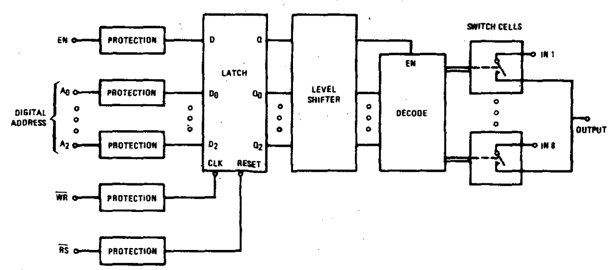


HI-509L

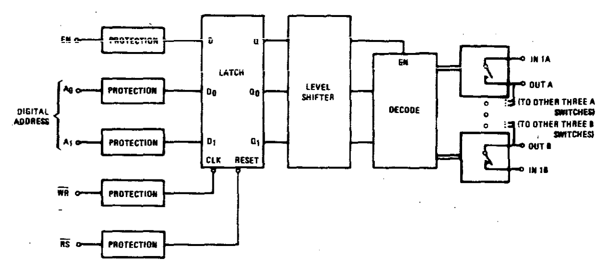


FUNCTIONAL DIAGRAM

HI-508L



HI-509L



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 4 and 14	44V	Operating Temperature	
Digital Input Overvoltage, V_A, V_{EN}, $V_{\overline{RS}}$, $V_{\overline{WR}}$:			
V supply (+)	+4V	HI-508L/509L-2	−55°C to 125°C
V supply (−)	−4V	HI-508L/509L-5	0°C to 75°C
Analog Overvoltage		Storage Temperature	−65°C to +150°C
Input to Ground	±25VDC		
Total Power Dissipation* (Package)	1200mW	*Derate-8mW/°C above T_A = +75°C	

ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

+V supply = 15V, −V supply = −15V, V_{AH} (Logic High) = 2.0V, V_{AL} (Logic Low) = 0.8V

	HI-508L/509L-2 −55°C to +125°C				HI-508L/509L-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS								
V_S Analog Signal Range	Full		±10			±10		V
R_{ON}, ON Resistance (Note1)	+25°C			1.2			1.5	KΩ
	Full			1.8			1.8	KΩ
$\triangle R_{ON}$, Change In R_{ON} (Note 2) between channels	+25°C		5			5		%
$I_{S(off)}$, OFF input leakage current	+25°C			10			10	nA
	Full		7	50		7	50	nA
$I_{D(off)}$, OFF output leakage current	+25°C			10			10	nA
HI-508L	Full		5	100		5	100	nA
HI-509L	Full			50			50	nA
$I_{D(On)}$, ON Channel leakage current	+25°C		5	10			10	nA
HI-508L	Full		5	100		5	100	nA
HI-509L	Full			50			50	nA
FAULT CHARACTERISTICS								
$I_{S(Off)}$, with Power OFF	Full		10	1000		10	5000	nA
$I_{S(Off)}$, overvoltage (Note 3)	Full		10	750		10	2500	nA
$I_{D(Off)}$, with input over-	+25°C		5			5		nA
voltage applied (Note 3)	Full		10	750		10	2500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full		1.4	0.8		1.4	0.8	V
V_{AH}, Input High Threshold	Full	2.0	1.4		2.0	1.4		V
I_{AH}, Input High Current	Full		10	40		10	40	μA
I_{AL}, Input Low Current	Full		40	200		40	200	μA
DYNAMIC SWITCHING CHARACTERISTICS								
t_a, Access Time	+25°C		0.5	1.0		0.5	1.0	μS
t_{OPEN}, Break-Before-Make	+25°C	.025	0.1		0.25	0.1		μS
t_{ON}, (EN, $\overline{WR}$), Enable Delay (ON)	+25°C			1.0			1.0	μS
t_{OFF}, (EN, $\overline{RS}$), Enable and Reset Delay (OFF)	+25°C		0.5	1.0		0.5	1.0	μS
Settling Time (±0.1%)	+25°C		1.0			1.0		μS
(±0.01%)	+25°C		1.75			1.75		μS
Q Charge Injection	+25°C		10			10		pC
OFF Isolation (Note 4)	+25°C		−72			−72		dB
OFF Isolation POWER OFF (Note 5)	+25°C		−56			−56		dB
$C_{S(Off)}$, Channel Input Cap.	+25°C		5			5		pF
$C_{D(Off)}$, Channel Output Cap.								
HI-508L	+25°C		20			20		
HI-509L	+25°C		10			10		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(Off)}$, Input to Output capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation (Note 6)	Full		60	100		60	100	mW
I +, Current Pin 14 (Note 6)	Full		3.7	6.0		3.7	6.0	mA
I −, Current Pin 4 (Note 6)	Full		0.3	0.6		0.3	0.6	mA

Notes:
1. V_{OUT} = ±10V, I out = −100 μa
2. $\triangle R_{ON} = \frac{R_{ON}(Max) - R_{ON}(Min)}{R_{ON}(Avg)}$ V_{IN} = ±10V
3. Analog Overvoltage = ±25V
4. V_{EN} = 0.8V, R_L = 1KΩ, C_L = 50pF

V_S = 3Vrms, f = 500 kHz

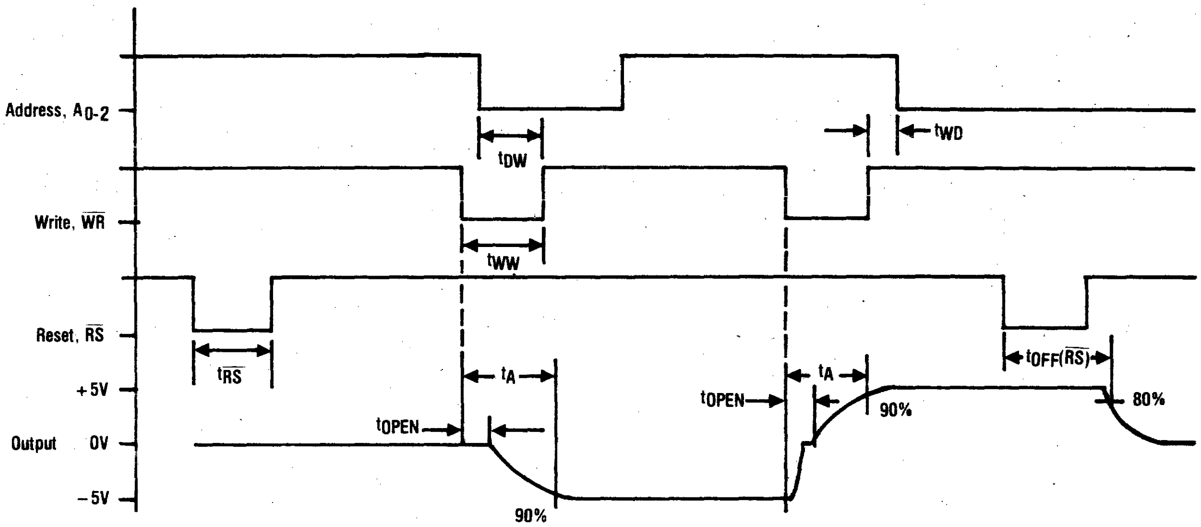
Off isolation = 20 log $\frac{|V_D|}{|V_S|}$

5. V+, V− = 0V, R_L = 1KΩ
C_L = 50pF, V_S = 3Vrms, f = 500 kHz.
6. See Test Circuit #8 for high toggle frequency applications.

Minimum Timing Requirements

PARAMETER	MEASURED TERMINAL	MIN LIMITS FULL TEMP RANGE	UNITS
t_{WW}, Write Pulse Width	$\overline{WR}$	300	nS
t_{DW}, A, EN Data Valid To WRITE (Stabilization Time)	A0, A1, A2, A3, EN $\overline{WR}$	225	nS
t_{WD}, A, EN Data Valid To WRITE (hold Time)	$\overline{WR}$ A0, A1, A2, A3, EN	100	nS
t_{RS}, RESET pulse width	$\overline{RS}$	400	nS

Timing Requirements



1. Inputs to HI-508L (509L) : Channel 1 = −5V; Channel 8, (4) = +5V.
2. $+V_{SUPPLY}$ = +15V; $-V_{SUPPLY}$ = −15V.
3. Logic Levels: V_{AL} = 0V; V_{AH} = +2.0V.
4. Time intervals are measured between 50% levels unless otherwise noted.
5. Minimum values for $t_{\overline{RS}}$, t_{DW}, t_{WW} and t_{WD} are guaranteed separately but not simultaneously.

Figure 1

SCHEMATIC DIAGRAM

Switch Cell

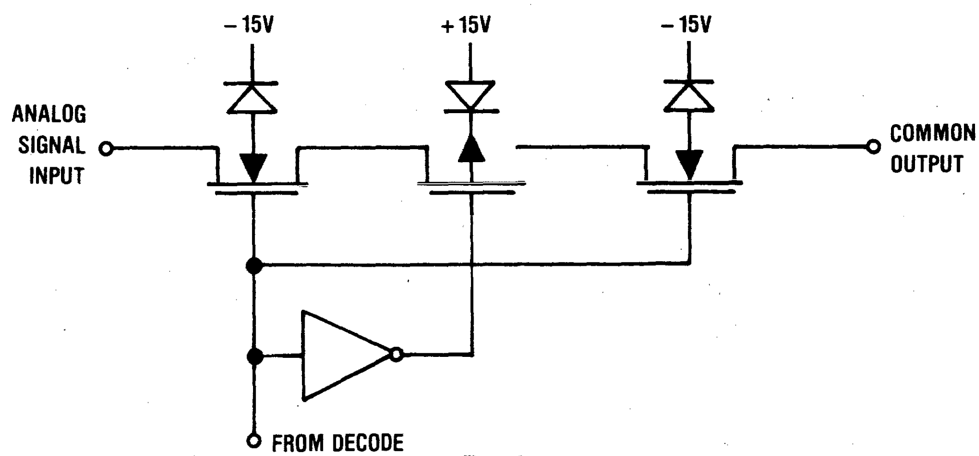


Figure 2

TRUTH TABLES

508L

A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	OUTPUT - ON CHANNEL
X	X	X	L	L	H	None
X	X	X	X		H	Previous On Channel.
X	X	X	X	X	L	None (latches cleared)
L	L	L	H	L	H	Channel 1
L	L	H	H	L	H	Channel 2
L	H	L	H	L	H	Channel 3
L	H	H	H	L	H	Channel 4
H	L	L	H	L	H	Channel 5
H	L	H	H	L	H	Channel 6
H	H	L	H	L	H	Channel 7
H	H	H	H	L	H	Channel 8

507L

A1	A0	EN	$\overline{WR}$	$\overline{RS}$	OUTPUT - ON CHANNEL PAIR
X	X	L	L	H	None
X	X	X		H	Previous On Channel.
X	X	X	X	L	None (latches cleared)
L	L	H	L	H	Channel 1A and 1B
L	H	H	L	H	Channel 2A and 2B
H	L	H	L	H	Channel 3A and 3B
H	H	H	L	H	Channel 4A and 4B

DESCRIPTION AND APPLICATION

The switch cell of the HI-508L/509L has a different structure than earlier Harris designs (HI-508, HI508A). The new switch (Figure 3) consists of an N-channel, P-channel and N-channel MOSFET in series, as opposed to the transmission gate configuration with an N and P-channel device in parallel. The series N-P-N switch offers higher Off Isolation with power off, and better fault performance. Channel overvoltage protection is inherent since one of the three MOSFETs turn off in the presence of overvoltage. this turn-off process begins well below the supply rail so the V_{IN} range is less than the power supply range. Electrical performance is guaranteed to ±10V for each channel, and the usable range extends above ±11 Volts.

The address inputs A_0, A_1, A_2, and ENABLE are latched into an internal buffer when $\overline{WR}$ goes high. Each latch output is level shifted into the decode section, which activates the appropriate channel. The device may be reset (all channels OFF) by taking $\overline{RS}$ low. Usually, $\overline{RS}$ is tied to the system RESET line, to assure that all channels are OFF following a turn-on of power. The reset function overrides all others, just as $\overline{WR}$ overrides the address inputs (A_0-A_2 and EN are ignored when $\overline{WR}$ is high). With $\overline{WR}$ low and $\overline{RS}$ high, the switches respond immediately to a change in channel address; i.e., the latches are "transparent". Refer to Figure 1.

HARRIS

HI-1818A/1828A

Low Resistance 8 Channel CMOS Analog Multiplexers

FEATURES

• SIGNAL RANGE	±15V
• "ON" RESISTANCE (TYP.)	250Ω
• INPUT LEAKAGE AT +125°C (TYP.)	20nA
• ACCESS TIME (TYP.)	350ns
• POWER CONSUMPTION (TYP.)	5mW
• DTL/TTL COMPATIBLE ADDRESS	
• -55°C to +125°C OPERATION	

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- PRECISION INSTRUMENTATION
- DEMULTIPLEXING
- SELECTOR SWITCH

DESCRIPTION

The HI-1818A/1828A are monolithic high performance CMOS analog multiplexers offering built-in channel selection decoding plus an inhibit (enable) input for disabling all channels. Dielectric Isolation (DI) processing is used for enhanced reliability and performance (see Application Note 521). Substrate leakage and parasitic capacitance are much lower, resulting in extremely low static errors and high throughput rates. Low output leakage (typically 0.1nA) and low channel ON resistance (250 Ω) assure optimum performance in low level or current mode applications.

The 1818A is a single-ended 8 channel multiplexer, while the HI-1828A is a differential 4 channel version. Either device is ideally suited for medical instrumentation, telemetry systems, and microprocessor based data acquisition systems.

The HI-1818A-2 and HI-1828A are specified over -55°C to +125°C, while the -5 versions are specified over 0°C to +75°C.

PINOUT

HI-1818A

Top View

ADDRESS A_1	1	16	ADDRESS A_0
+5.0V SUPPLY	2	15	-15V SUPPLY
$\overline{ENABLE}$	3	14	+15V SUPPLY
ADDRESS A_2	4	13	IN1
IN 8	5	12	OUT
IN 7	6	11	IN2
IN 6	7	10	IN 3
IN 5	8	9	IN 4

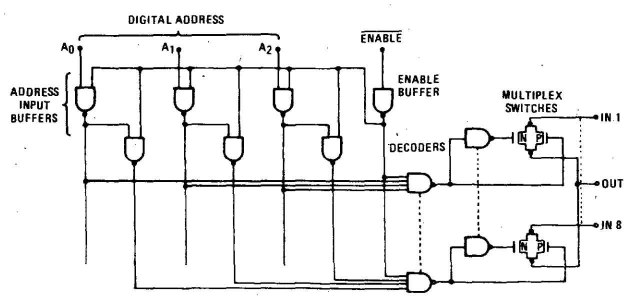
HI-1828A

Top View

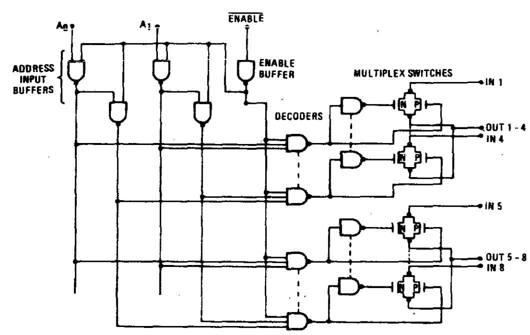
ADDRESS A_1	1	16	ADDRESS A_0
+5.0V SUPPLY	2	15	-15V SUPPLY
$\overline{ENABLE}$		14	+15V SUPPLY
OUT 5 THRU 8	4	13	IN 1
IN 8	5	12	OUT 1 THRU 4
IN 7	6	11	IN 2
IN 6	7	10	IN 3
IN 5	8	9	IN 4

FUNCTIONAL DIAGRAM

HI-1818A



HI-1828A



ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Supply Voltage Between Pins 14 and 15	40.0V	Digital Input Voltage	V-Supply to V+ Supply
Logic Supply Voltage, Pin 2	30.0V	Total Power Dissipation (Note 2)	750mW
Analog Input Voltage: V^+_{Supply} +2V		Storage Temperature Range	-65°C to +150°C
V^-_{Supply} -2V			

ELECTRICAL CHARACTERISTICS

Supplies = +15V, -15V, +5V

PARAMETER	TEMP.	HI-1818A-2/1828A-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-1818A-5/1828A-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
* V_{IN}, Analog Signal Range	Full	-15		+15	-15		+15	V
* R_{ON}, ON Resistance (Note 3)	+25°C		250	400		250	400	Ω
	Full		300	500		300	500	Ω
* I_S(OFF), Input Leakage Current	Full		20	50		20	50	nA
* I_D(ON), On Channel Leakage Current								
(HI-1818A)	Full		100	250		100	250	nA
(HI-1828A)	Full		50	125		50	125	nA
* I_D(OFF) Output Leakage Current								
(HI-1818A)	Full		100	250		100	250	nA
(HI-1828A)	Full		50	125		50	125	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.4			0.4	V
V_{AH}, Input High Threshold (Note 4)	Full	4.0			4.0			V
I_A, Input Leakage Current	Full		.01	1		.01	1	μA
SWITCHING CHARACTERISTICS								
T_S, Access Time (Note 5)	+25°C		350			350		ns
Break-Before-Make Delay	+25°C		100			100		ns
Settling Time (0.1%)	+25°C		1.08			1.08		μs
(0.025%)	+25°C		2.8			2.8		μs
C_{IN}, Channel Input Capacitance	+25°C		4			4		pF
C_{OUT}, Channel Output Capacitance								
(HI-1818A)	+25°C		20			20		pF
(HI-1828A)	+25°C		10			10		pF
C_{DS}(OFF), Drain-To-Source Capacitance	+25°C		0.6			0.6		pF
C_D, Digital Input Capacitance	+25°C		5			5		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		5			5		mW
P_{DS}, Standby Power (Note 6)	Full		5			5		mW
* I_+, Current Pin 14	Full		0.1	0.5		0.1	1	mA
* I_-, Current Pin 15	Full		0.3	1		0.3	2	mA
* I_L, Current Pin 2	Full		0.3	1		0.3	2	mA

NOTES:
1. Voltage ratings apply when voltages at all other pins are within their normal operating ranges.
2. Derate 12.3 mW/°C above 110°C.
3. $V_{OUT} = \pm 10V$ $I_{OUT} = -1mA$.
4. To drive from DTL/TTL circuits, 1K pull-up resistors to + 5.0V supply are recommended.
5. Time measured to 90% of final output level; V_{OUT} = - 5.0V to +5.0V, Digital Inputs = 0V to + 4.0V.
6. Voltage at Pin 3, $\overline{ENABLE}$ = + 4.0V.

* 100% Tested for Dash 8 at +25°C and +125°C Only.

TRUTH TABLES

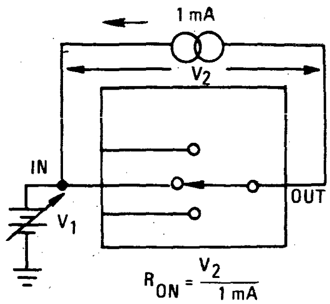
HI-1818A

A_2	A_1	A_0	$\overline{EN}$	"ON" CHANNEL
L	L	L	L	1
L	L	H	L	2
L	H	L	L	3
L	H	H	L	4
H	L	L	L	5
H	L	H	L	6
H	H	L	L	7
H	H	H	L	8
X	X	X	H	NONE

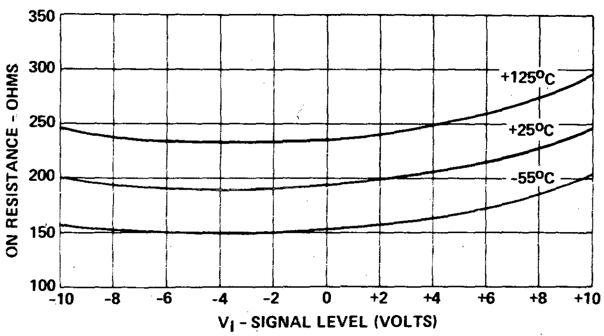
HI-1828A

A_1	A_0	$\overline{EN}$	"ON" CHANNELS
L	L	L	1 and 5
L	H	L	2 and 6
H	L	L	3 and 7
H	H	L	4 and 8
X	X	H	NONE

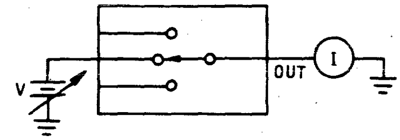
ON RESISTANCE vs ANALOG SIGNAL LEVEL



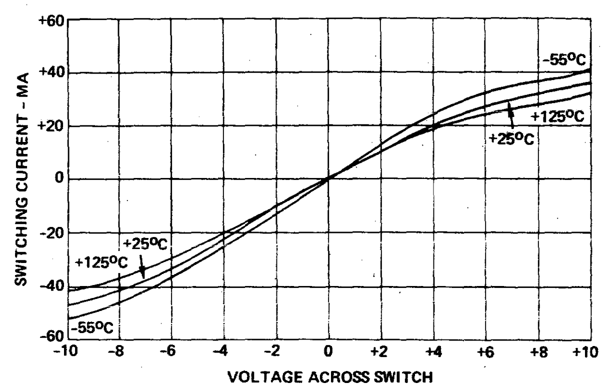
Test Circuit



ON CHANNEL CURRENT vs VOLTAGE

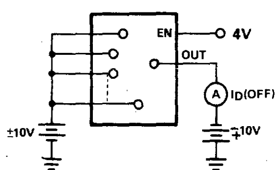


Test Circuit

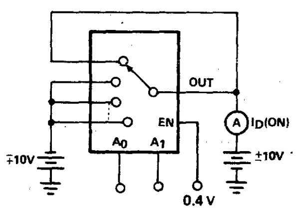


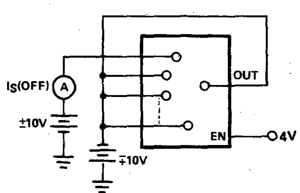
LEAKAGE CURRENTS vs TEMPERATURE

OFF LEAKAGE

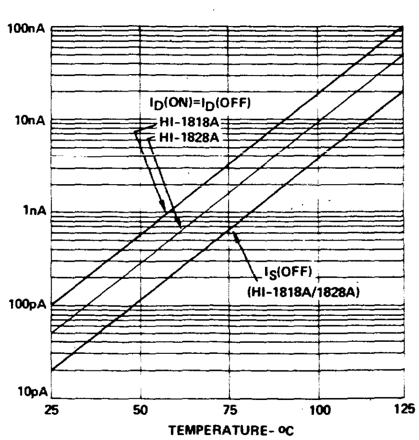


ON LEAKAGE

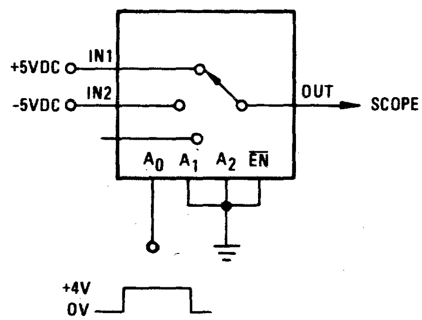


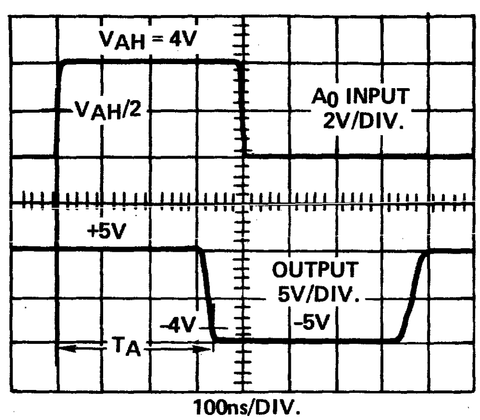


*Two measurements per channel: +10V/-10V and -10V/+10V. (Two measurements per device for ID(OFF): +10V/-10V and -10V/+10V.)



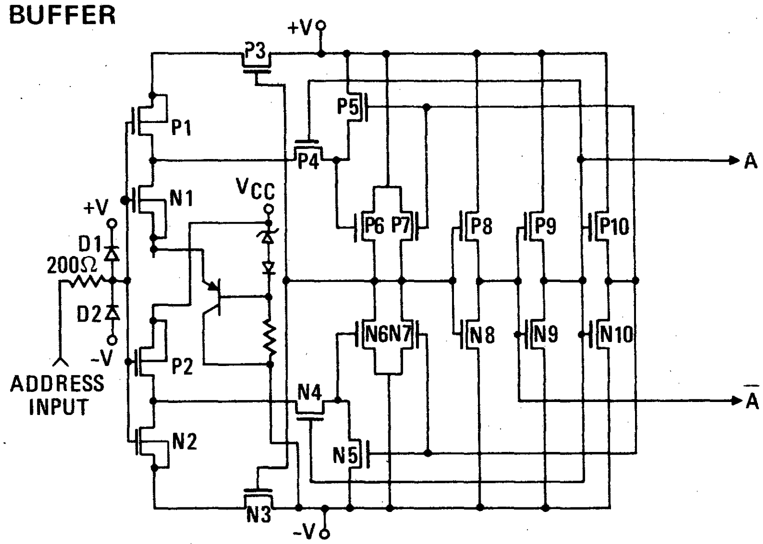
ACCESS TIME





SCHEMATIC DIAGRAM

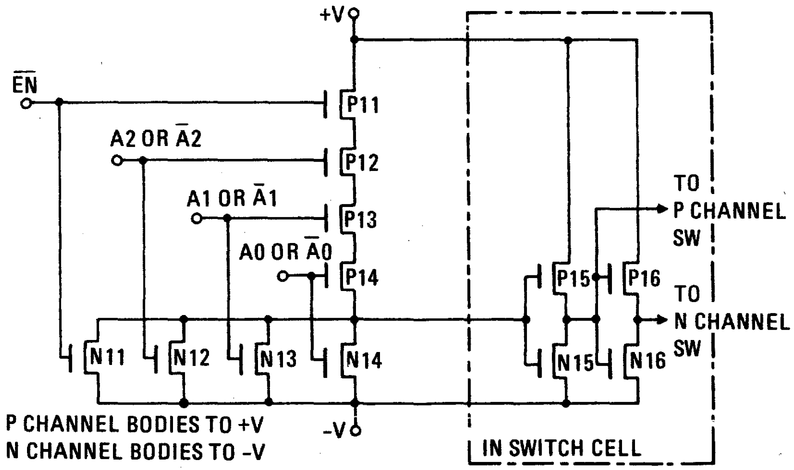
ADDRESS INPUT BUFFER



ALL N-CHANNEL BODIES TO V-

ALL P-CHANNEL BODIES TO V+ UNLESS OTHERWISE INDICATED.

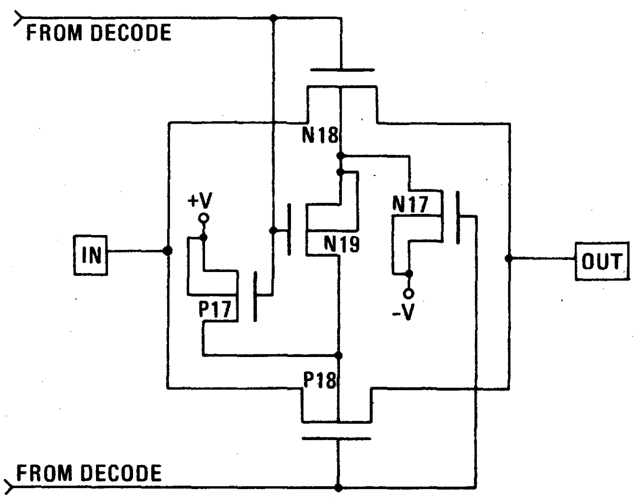
DECODER GATE



P CHANNEL BODIES TO +V
N CHANNEL BODIES TO -V

A2 OR Ā2 NOT USED FOR HI-1828A

MULTIPLEX SWITCH



HARRIS

HI-516

16 Channel/Differential 8 Channel CMOS High Speed Analog Multiplexer

FEATURES

- ACCESS TIME (TYP) 100ns
- SETTLING TIME (TYP TO 0.01%) 800ns
- LOW LEAKAGE I_S OFF 10pA; I_D OFF 35pA
- LOW CAPACITANCE C_S OFF 2.5pF; C_D OFF 18pF
- HIGH OFF ISOLATION AT 1MHz 80dB
- LOW CHARGE INJECTION 0.3pC
- SINGLE ENDED TO DIFFERENTIAL SELECTABLE (SDS)
- LOGIC LEVEL SELECTABLE (LLS)

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- PRECISION INSTRUMENTATION
- INDUSTRIAL CONTROL

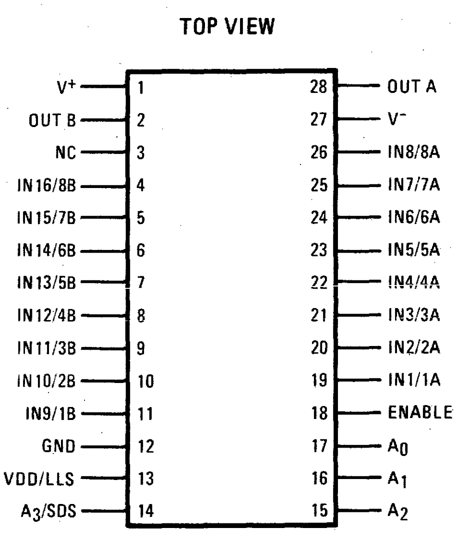
DESCRIPTION

The HI-516 is a monolithic dielectrically isolated, high speed, high performance CMOS analog multiplexer. It offers unique built-in channel selection decoding plus an inhibit input for disabling all channels. The dual function of address input A_3 enables the HI-516 to be user programmed either as a single ended 16-channel multiplexer, by connecting 'out A' to 'out B' and using A_3 as a digital address input, or as an 8-channel differential multiplexer by connecting A_3 to the V^- supply. The substrate leakages and parasitic capacitances are reduced substantially using the Harris dielectric isolation process to achieve optimum performances in both high and low level signal applications. The low output leakage current (I_D Off $< 100pA$ @ 25°C) and fast settling (t_{SETTLE} = 800ns to 0.01%) characteristics of the device make it an ideal choice for high speed data acquisition systems, precision instrumentation, and industrial process controls.

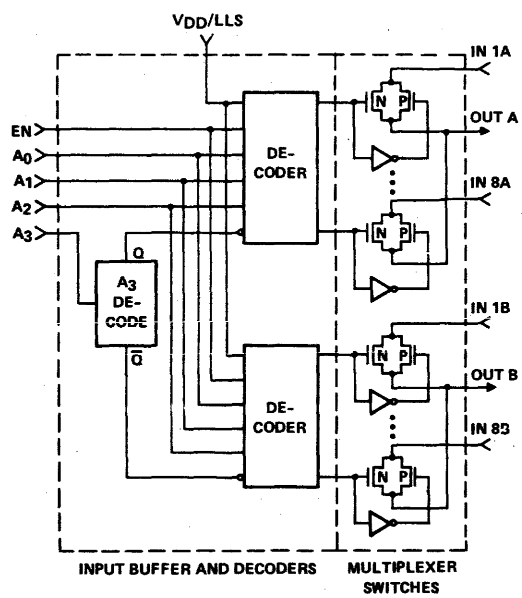
The HI-516 is available in a 28 lead dual-in-line package. HI-516-5 is specified for operation over 0°C to +75°C, and the HI-516-2 over -55°C to +125°C. Processing to MIL-STD-883A, Class B screening is available by selecting the HI-516-8.

PINOUT

Section 11 for Packaging



FUNCTIONAL DIAGRAM



A3 Decode		
A3	Q	$\overline{Q}$
H	H	L
L	L	H
V^-	L	L

INTERFACE

Harris Semiconductor

ABSOLUTE MAXIMUM RATINGS

Digital Input Overvoltage:

TTL	$-6V < V_{AH} < +6V$		
	A2 V_{SUPPLY} (-)	-2V	
CMOS	V_{SUPPLY}(+)	+2V	
	GND	-2V	

Analog Input Voltage:

V_S	V_{SUPPLY}(+)	+2V	
	V_{SUPPLY}(-)	-2V	

Voltage Between Supply Pins	33V
Total Power Dissipation*	1200mW
Operating Temperature Ranges:	
HI-516-2	-55°C to +125°C
HI-516-5	0°C to 75°C
Storage Temperature Range	-65°C to 150°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified) Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V; V_{DD}/LLS = Open (Note 6)

PARAMETER	TEMP	-55°C to +125°C			0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG CHANNEL CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON}, On Resistance (Note 1)	+25°C		620	750		620	750	Ω
	Full		770	1,000		700	1,000	Ω
I_S (OFF), Off Input Leakage Current	+25°C		0.01			0.01		nA
	Full		0.38	50		0.38	50	nA
I_D(OFF), Off Output Leakage Current	+25°C		0.035			0.035		nA
	Full		0.48	100		0.48	100	nA
I_D(ON), On Channel Leakage Current	+25°C		0.04			0.04		nA
	Full		0.56	100		0.56	100	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL} Input Low Threshold (TTL)	Full			0.8			0.8	V
V_{AH} Input High Threshold (TTL)	Full	2.4			2.4			V
V_{AH} Input Low Threshold (CMOS)	Full			$0.3V_{DD}$			$0.3V_{DD}$	V
V_{AH} Input High Threshold (CMOS)	Full	$0.7V_{DD}$			$0.7V_{DD}$			V
I_{AH} Input Leakage Current (High)	Full		0.05	1		0.05	1	μA
I_{AL} Current (Low)	Full		4	25		4	25	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		100	150		100	150	ns
	Full		120	200		120	200	ns
t_{OPEN}, Break before make delay	+25°C		20			20		ns
t_{ON}(EN), Enable Delay (IN)	+25°C		100	150		100		ns
t_{OFF}(EN), Enable Delay (OFF)	+25°C		80	125		80		ns
Settling Time (0.1%)	+25°C		250			250		ns
(0.01%)	+25°C		800			800		ns
Charge Injection (Note 2)	+25°C		0.33			0.33		pC
Off Isolation (Note 3)	+25°C		90			90		dB
C_S(OFF), Channel Input Capacitance	+25°C		2.5			2.5		pF
C_D(OFF), Channel Output Capacitance	+25°C		18			18		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS}(OFF), Input to Output Capacitance	+25°C		0.02			0.02		pF
POWER REQUIREMENTS								
PD, Power Dissipation	Full		525			525		mW
I^+, Current (Note 4)	Full		17.5	25		17.5	30	mA
I^-, Current (Note 4)	Full		17.5	25		17.5	30	mA
I^+, Standby (Note 5)	Full		17.0	25		17.0	30	mA
I^-, Standby (Note 5)	Full		17.0	25		17.0	30	mA

NOTES:

1. $V_{IN} = \pm 10V$, $I_{OUT} = -100\mu A$
2. $V_{IN} = 0V$, $C_L = 100pF$, Enable input pulse = 3V, f = 500kHz
3. $V_{EN} = 0.8V$, $V_S = 3V_{RMS}$, f = 500kHz, $C_L = 40pF$, $R_L = 1k$, Pin 3 grounded
4. $V_{EN} = +2.4V$
5. $V_{EN} = 0.8V$
6. V_{DD}/LLS Pin = Open or Grounded for TTL Compatibility
   V_{DD}/LLS Pin = V_{DD} for CMOS Compatibility

HI-516 USED AS A 16-CHANNEL MULTIPLEXER OR 8 CHANNEL DIFFERENTIAL MULTIPLEXER *

USE A_3 AS DIGITAL ADDRESS INPUT					ON CHANNEL TO	
ENABLE	A_3	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	X	NONE	NONE
H	L	L	L	L	1A	NONE
H	L	L	L	H	2A	NONE
H	L	L	H	L	3A	NONE
H	L	L	H	H	4A	NONE
H	L	H	L	L	5A	NONE
H	L	H	L	H	6A	NONE
H	L	H	H	L	7A	NONE
H	L	H	H	H	8A	NONE
H	H	L	L	L	NONE	1B
H	H	L	L	H	NONE	2B
H	H	L	H	L	NONE	3B
H	H	L	H	H	NONE	4B
H	H	H	L	L	NONE	5B
H	H	H	L	H	NONE	6B
H	H	H	H	L	NONE	7B
H	H	H	H	H	NONE	8B

* For 16-Channel single-ended function, tie 'out A' to 'out B', for dual 8-channel function use the A_3 address pin to select between MUX A and MUX B, where MUX A is selected with A_3 low.

HI-516 USED AS A DIFFERENTIAL 8-CHANNEL MULTIPLEXER

A_3 CONNECT TO V^- SUPPLY				ON CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	NONE	NONE
H	L	L	L	1A	1B
H	L	L	H	2A	2B
H	L	H	L	3A	3B
H	L	H	H	4A	4B
H	H	L	L	5A	5B
H	H	L	H	6A	6B
H	H	H	L	7A	7B
H	H	H	H	8A	8B

HARRIS

HI-518

8 Channel/Differential 4 Channel CMOS High Speed Analog Multiplexer

FEATURES

- ACCESS TIME (TYP) 80ns
- SETTLING TIME (0.1%) 250ns
- LOW LEAKAGE I_S (OFF) 50pA
  I_D (OFF) 100pA
- LOW CAPACITANCE (TYP) C_S (OFF) 2pF
  C_D (OFF) 10pF
- HIGH OFF ISOLATION @ (1MHz) 75dB
- SINGLE ENDED TO DIFFERENTIAL MODE SELECTABLE (SDS)
- LOGIC LEVEL SELECTABLE (LLS)
- LOW CHARGE INJECTION 0.3pC

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- INDUSTRIAL CONTROLS
- TELEMETRY

DESCRIPTION

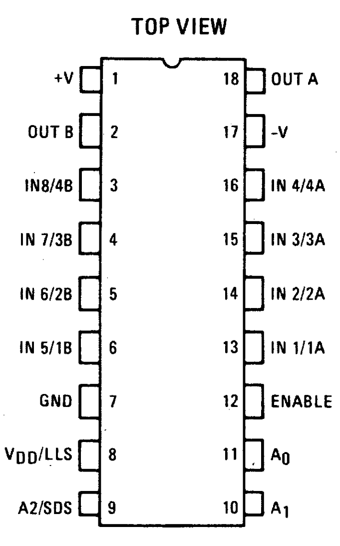
The HI-518 is a monolithic, high performance, high speed Analog Multiplexer, constructed utilizing the Harris Dielectrically isolated CMOS process.

This device has the added feature that it can be user programmed either as a single ended 8-channel multiplexer by connecting 'out A' to 'out B' and using A2 as a digital address input, or as a 4-channel differential multiplexer by connecting A2 to the V^- supply.

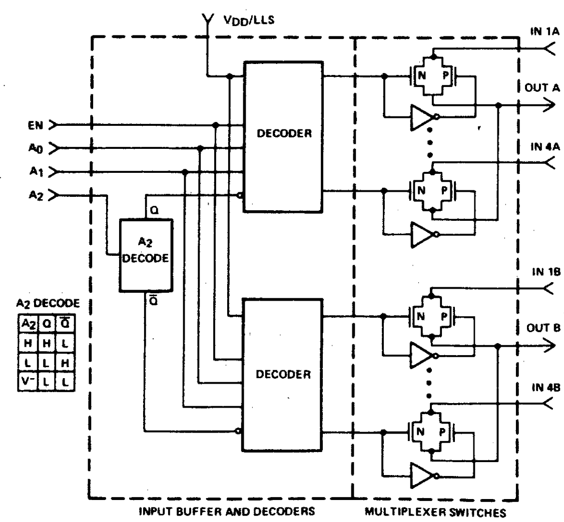
TTL or CMOS compatibility is also selectable. Low leakage current, I_D off < 100pA @ 25°C, and fast settling, 250ns to 0.1%, characteristics of this device make it an ideal choice for high speed data acquisition systems, precision instrumentation and industrial process controls.

The HI-518 is available in an 18 lead Dual-in-Line Package. The HI-518-5 is specified for operation over 0°C to +75°C, and the HI-518-2 over -55°C to +125°C. Processing to MIL-STD-883A Class B screening is available by selecting the HI-518-8.

PINOUT



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Digital Input Overvoltage:

TTL	$-6V < V_{AH} < +6V$	
	A2 V_{SUPPLY} (-)	-2V
CMOS	$V_{SUPPLY}(+)$	+2V
	GND	-2V

Analog Input Voltage:

V_S	$V_{SUPPLY}(+)$	+2V
	$V_{SUPPLY}(-)$	-2V

Voltage Between Supply Pins	33V
Total Power Dissipation*	725mW
Operating Temperature Ranges:	
HI-518-2	-55°C to +125°C
HI-518-5	0°C to 75°C
Storage Temperature Range	-65°C to 150°C

*Derate 13.6mW/°C above T_A = 120°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified) Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V; V_{DD}/LLS = Open (Note 6).

PARAMETER	TEMP	-55°C to +125°C MIN	TYP	MAX	0°C to +75°C MIN	TYP	MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS								
V_S Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON} On Resistance (Note 1)	+25°C		480	750		480	750	Ω
	Full		700	1000		700	1000	Ω
I_S (OFF) Off Input	+25°C		0.05			0.05		nA
Leakage Current	Full		0.60	50		0.60	50	nA
I_D (OFF) Off Output	+25°C		0.10			0.10		nA
Leakage Current	Full		0.30	50		0.30	50	nA
I_D (ON) On Channel	+25°C		0.10			0.10		nA
Leakage Current	Full		0.30	50		0.30	50	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL} Input Low Threshold (TTL)	Full			0.8			0.8	V
V_{AH} Input High Threshold (TTL)	Full	2.4			2.4			V
V_{AL} Input Low Threshold (CMOS)	Full			$0.3V_{DD}$			$0.3V_{DD}$	V
V_{AH} Input High Threshold (CMOS)	Full	$0.7V_{DD}$			$0.7V_{DD}$			V
I_{AH} Input Leakage Current (High)	Full		0.05	1		0.05	1	μA
I_{AH} Input Leakage Current (Low)	Full		4	20		4	20	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		80	125		80	125	
	Full		110	150		110	150	ns
t_{OPEN}, Break before make Delay	+25°C		20			20		ns
t_{ON} (EN), Enable Delay (ON)	+25°C		80	150		80	150	ns
t_{OFF} (EN), Enable Delay (OFF)	+25°C		60	125		60	125	ns
Settling Time (0.1%)	+25°C		250			250		ns
(0.01%)	+25°C		800			800		
Charge Injection (Note 2)	+25°C		0.3			0.3		pC
Off Isolation (Note 3)	+25°C		86			86		dB
C_S (OFF) Channel Input Capacitance	+25°C		1.9			1.9		pF
C_D (OFF) Channel Output Capacitance	+25°C		10			10		pF
C_A, Digital Input Capacitance	+25°C		3			3		pF
CDS (OFF) Input to Output Capacitance	+25°C		0.02			0.02		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		360	450		360	540	mW
I+, Current (Note 4)	Full		12	15		12	18	mA
I⁻, Current (Note 4)	Full		12	15		12	18	mA
I+, Standby (Note 5)	Full		11.5	15		11.5	18	mA
I⁻, Standby (Note 5)	Full		11.5	15		11.5	18	mA

NOTES:

1. $V_{IN} = \pm 10V$, $I_{OUT} = -100\mu A$
2. V_{IN} = 0V, C_L = 100pF, Enable Input pulse = 3V, f = 500kHz.
3. V_{EN} = 0.8V, V_S = 3VRMS, f = 500kHz, C_L = 40pF, R_L = 1k. Due to the pin to pin capacitance between IN 8/4B (Pin 3) and Out B (Pin 2) channel 8/4B exhibits 60dB of Off Isolation under the above test conditions.
4. V_{EN} = +2.4V.
5. V_{EN} = 0.8V.
6. VDD/LLS Pin = Open or grounded for TTL compatibility. VDD/LLS Pin = V_{DD} for CMOS compatibility.

HI-518 USED AS 8 CHANNEL MULTIPLEXER OR
4 CHANNEL DIFFERENTIAL MULTIPLEXER

USE A_2 AS DIGITAL ADDRESS INPUT				ON CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	NONE	NONE
H	L	L	L	1A	NONE
H	L	L	H	2A	NONE
H	L	H	L	3A	NONE
H	L	H	H	4A	NONE
H	H	L	L	NONE	1B
H	H	L	H	NONE	2B
H	H	H	L	NONE	3B
H	H	H	H	NONE	4B

HI-518 USED AS DIFFERENTIAL
4 CHANNEL MULTIPLEXER

A_2 CONNECT TO V^- SUPPLY			ON CHANNEL TO	
ENABLE	A_1	A_0	OUT A	OUT B
L	X	X	NONE	NONE
H	L	L	1A	1B
H	L	H	2A	2B
H	H	L	3A	3B
H	H	H	4A	4B

HARRIS

HI-524

4 Channel Video Multiplexer

FEATURES

- CROSSTALK (10MHz) > 60dB
- FAST ACCESS TIME 150ns
- FAST SETTLING TIME (0.01%) 600ns
- TTL COMPATIBLE

APPLICATIONS

WIDEBAND SWITCHING

- RADAR
- TV VIDEO
- ECM

DESCRIPTION

The HI-524 is a four channel CMOS analog multiplexer designed to process single-ended video signals with bandwidths up to 10MHz. The chip includes a 1 of 4 decoder for channel selection and an Enable input to inhibit all channels (chip select).

Three CMOS transmission gates are used in each channel, as compared to the single gate in more conventional CMOS multiplexers. This provides a double barrier to the unwanted coupling of signals from each input to the output. In addition, Dielectric Isolation (DI) processing helps to insure that Crosstalk exceeds 60dB at 10MHz.

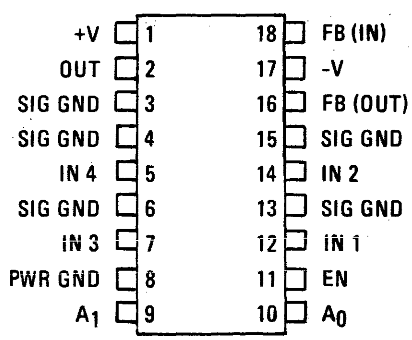
The HI-524 is designed to operate into a wideband buffer amplifier such as the HARRIS HA-5190. The multiplexer chip includes two "on" switches in series, for use as a feedback element with the amplifier. This feedback resistance matches and tracks the channel R_{ON} resistance, to minimize the amplifier V_{OS} and its variation with temperature.

The HI-524 is well suited to the rapid switching of video signals in telemetry, instrumentation, radar and video systems. It is packaged in an 18 pin ceramic DIP and operates on ±15V supplies.

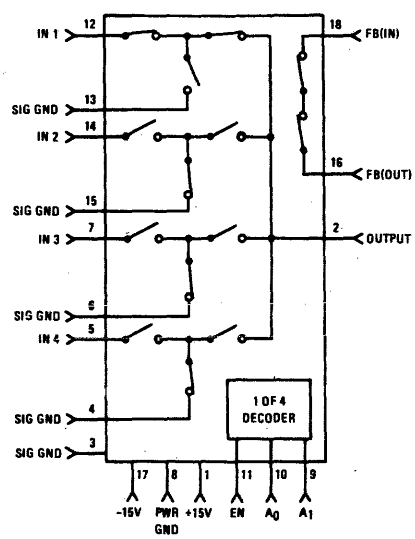
The performance levels available are: HI1-524-2, -55°C to +125°C operating range; HI1-524-5, 0°C to +75°C operating range and HI1-524-8, -55°C to +125°C operating range plus 100% screening per MIL-STD-883/Method 5004/Class B. Chips for hybrid applications are designated HI0-524-6.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



TRUTH TABLE

A_1	A_0	EN	ON CHANNEL
X	X	L	NONE
L	L	H	1*
L	H	H	2
H	L	H	3
H	H	H	4

*CHANNEL 1 IS SHOWN SELECTED IN THE DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Digital Input Overvoltage:
$-6V < V_{AH} < +6V$

Analog Input (V_S) or Output (V_O)
$+V_{SUPPLY}$ +2V
$-V_{SUPPLY}$ -2V

Voltage Between Supply Pins 33V

Either Supply to Ground 16.5V
Total Power Dissipation* 750mW
Operating Temperature Range:
HI-524-2, -8 -55°C to +125°C
HI-524-5 0°C to 75°C
Storage Temperature Range -65°C to 150°C
*Derate 13.6mW/°C above T_A = 120°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified) Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} = (Logic Level Low) = +0.8V; V_{EN} = +2.4V

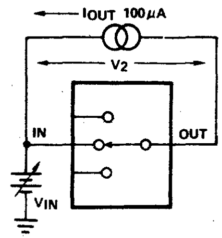
		HI-524-2, -8 -55°C to +125°C			HI-524-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Analog Channel Characteristics								
V_S, Analog Signal Range	Full	-10		+10	-10		+10	V
R_{ON}, On Resistance (Note 1)	+25°C		700			700		Ω
	Full			1.5K			1.5K	Ω
I_S (OFF), Off Input Leakage Current (Note 2)	+25°C		0.2			0.2		nA
	Full			50			50	nA
I_D (OFF), Off Output Leakage Current (Note 2)	+25°C		0.2			0.2		nA
	Full			50			50	nA
I_D (ON), On Channel Leakage Current (Note 2)	+25°C		0.7			0.7		nA
	Full			50			50	nA
3dB Bandwidth: (Note 3)	Full		20			20		MHz
Digital Input Characteristics								
V_{AL} Input Low Threshold (TTL)	Full			0.8			0.8	V
V_{AH} Input High Threshold (TTL)	Full	2.4			2.4			V
I_{AH} Input Leakage Current (High)	Full		0.05	1		0.05	1	μA
I_{AL} Current (Low)	Full		4	25		4	25	μA
Switching Characteristics								
t_A, Access Time (Note 4)	+25°C		150	300		150	300	ns
	Full							ns
t_{OPEN}, Break before make delay (Note 4)	+25°C		20			20		ns
t_{ON} (EN), Enable Delay (ON), R_L = 500Ω	+25°C		180	300		180		ns
t_{OFF} (EN), Enable Delay (OFF), R_L = 500Ω	+25°C		180	250		180		ns
Settling Time (0.1%) (Note 4)	+25°C		200			200		ns
(0.01%)	+25°C		600			600		ns
Crosstalk (Note 5)	+25°C		-65			-65		dB
C_S (OFF), Channel Input Capacitance	+25°C			6		6		pF
C_D (OFF), Channel Output Capacitance	+25°C			4		4		pF
C_A, Digital Input Capacitance	+25°C			5		5		pF
Power Requirements								
P_D, Power Dissipation	Full		540			540		mW
I^+, Current (V_{EN} = 2.4V) (Note 6)	Full		18	25		18	25	mA
I^-, Current (V_{EN} = 2.4V) (Note 6)	Full		18	25		18	25	mA
I^+, Standby (V_{EN} = 0.8V) (Note 6)	Full		18	25		18	25	mA
I^-, Standby (V_{EN} = 0.8V) (Note 6)	Full		18	25		18	25	mA

1. V_{IN} = 0V; I_{OUT} = 100μA (See Test Circuit # 1)
2. $V_O = \pm 10V$; $V_S = \mp 10V$ (See Test Circuits # 2, 3, 4)
3. MUX output is buffered with HA-5190 as shown in Applications section.
4. (See Test Circuit # 5)
5. V_{IN} = 10MHz, $3V_{p-p}$ on one channel, with any other channel selected. (Worst case is channel 3 selected with input on channel 4.) MUX output is buffered with HA-5190 as shown in Applications section. Terminate all channels with 75Ω .
6. Supply currents vary less than 0.5mA for switching rates from DC to 2MHz.

(UNLESS OTHERWISE SPECIFIED $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$, $V_{AH} = 2.4V$, $V_{AL} = 0.8V$)

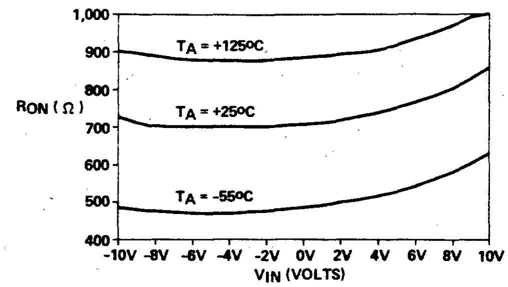
ON RESISTANCE

TEST CIRCUIT NO. 1

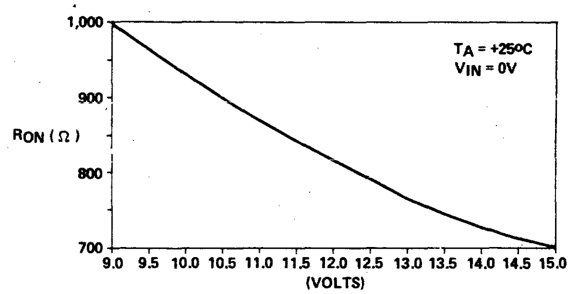


$$R_{ON} = \frac{V_2}{100\mu A}$$

ON RESISTANCE VS. ANALOG INPUT VOLTAGE

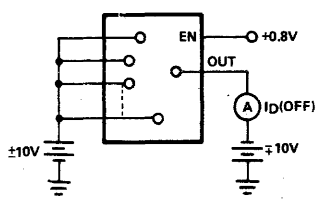


ON RESISTANCE VS. SUPPLY VOLTAGE



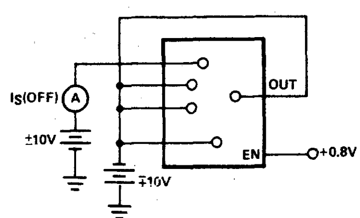
LEAKAGE CURRENT

TEST CIRCUIT NO. 2*

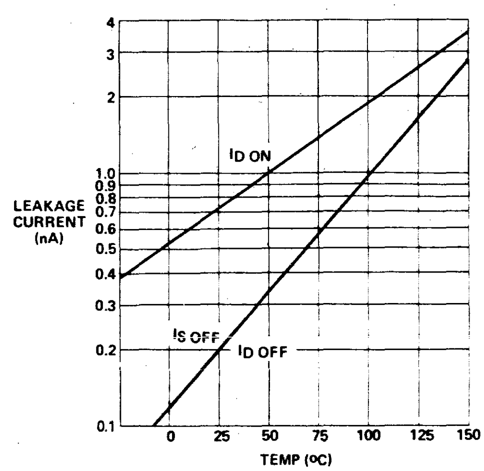


*Two measurements per channel:
+10V/-10V and -10V/+10V.
(Two measurements per device for ID(OFF):
+10V/-10V and -10V/+10V.)

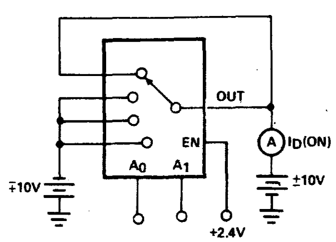
TEST CIRCUIT NO. 3*



LEAKAGE CURRENT VS. TEMPERATURE

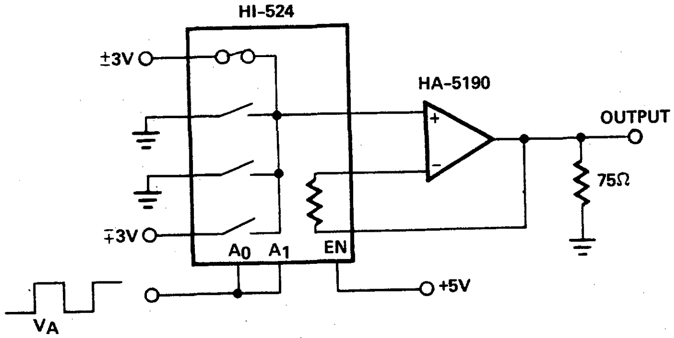


TEST CIRCUIT NO. 4*

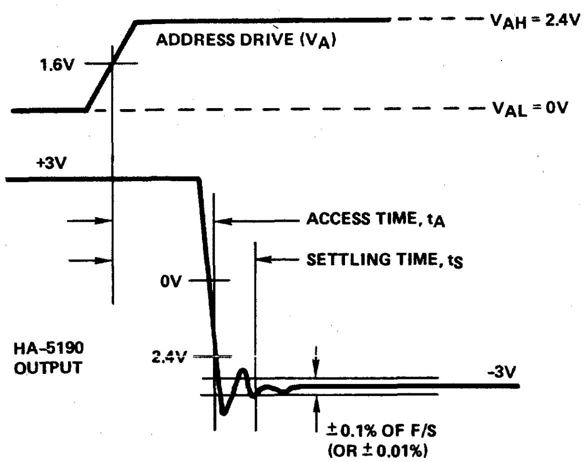


TEST CIRCUIT NO. 5

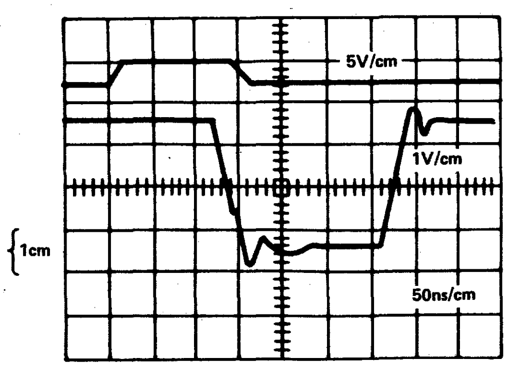
SETTLING TIME
ACCESS TIME
BREAK-BEFORE-MAKE DELAY



(USE DIFFERENTIAL COMPARATOR PLUG-IN ON SCOPE FOR SETTLING TIME MEASUREMENT.)



ACCESS TIME



HARRIS

HI-539

Monolithic, Four Channel, Low Level, Differential Multiplexer

FEATURES

- DIFFERENTIAL PERFORMANCE, TYP.:
  - LOW ΔR_{ON}, +125°C — 5.5Ω
  - LOW $\Delta I_{D(ON)}$, +125°C — 0.6nA
  - LOW Δ(CHARGE INJECTION) — 0.1pC
  - LOW CROSSTALK — -120dB
- SETTLING TIME, ±0.01% — 900ns
- WIDE SUPPLY RANGE — ±5V TO ±18V
- BREAK-BEFORE-MAKE SWITCHING
- NO LATCH-UP

APPLICATIONS

- LOW LEVEL DATA ACQUISITION
- PRECISION INSTRUMENTATION
- TEST SYSTEMS

DESCRIPTION

The Harris HI-539 is a monolithic, four channel, differential multiplexer. Two digital inputs are provided for channel selection, plus an Enable input to disconnect all channels.

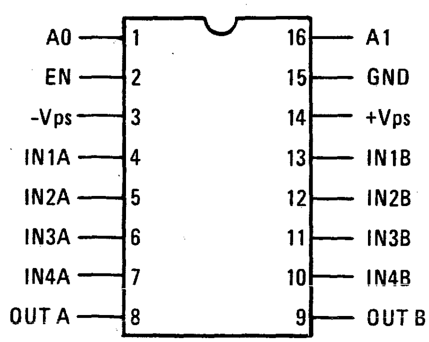
Performance is guaranteed for each channel over the range ± 10V, but is optimized for low level differential signals. Leakage current, for example, which varies slightly with input voltage, has its distribution centered at zero for zero input volts.

In most monolithic multiplexers, the net differential offset due to thermal effects becomes significant for low level signals. This problem is minimized in the HI-539 by symmetrical placement of critical circuitry with respect to the few heat producing devices.

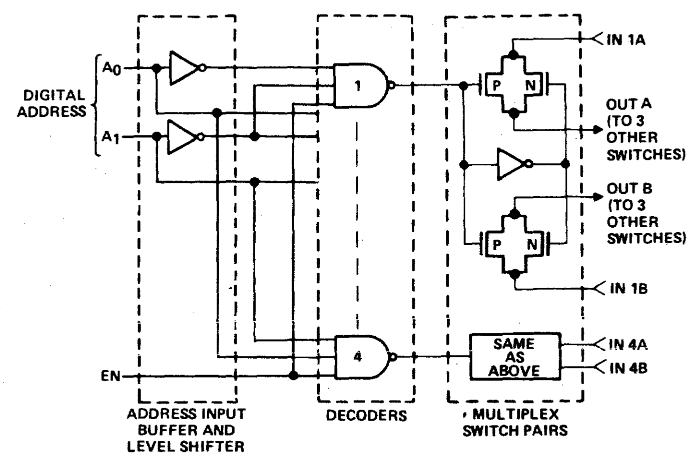
The HI-539 will be offered in both commercial and military temperature ranges, with screening available for MIL-STD-883, Class B. Supply voltages are ± 15V and power consumption is only 2.5mW. The package is a 16 pin ceramic DIP.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Voltage Between Supply Pins (V_{ps+}, V_{ps-})	40V
Voltage from either Supply to Ground	20V
Analog Input Voltage, V_S	$V_{ps-} \leq V_S \leq V_{ps+}$
Digital Input Voltage, V_A	$V_{ps-} \leq V_A \leq V_{ps+}$
Storage Temperature Range	-65°C to +150°C

Internal Power Dissipation*	725mW
Operating Temperature Range	
HI-539-2, -8	-55°C to +125°C
HI-539-4	-25°C to +85°C
HI-539-5	0°C to +75°C

*Derate 9.6mW/°C above T_A = 95°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified) Supplies = ± 15V, V_{EN} = +4.0V, V_{AH} (Logic Level High) = +4.0V, V_{AL} (Logic Level Low) = +0.8V. See the Performance Characteristics Section for test circuits and conditions. Selected parameters are defined in the Definitions Section.

PARAMETER	TEMP	HI-539-2, -8 TYP	HI-539-2, -8 MAX (MIN)	HI-539-4, -5 TYP	HI-539-4, -5 MAX (MIN)	UNITS
ANALOG CHANNEL CHARA'S						
V_S, Analog Signal Range	Full		(-10)/+10		(-10)/+10	V
R_{ON}, On Resistance V_{IN} = 0V	+25°C	650	850	650	850	Ω
V_{IN} = ± 10V	+25°C	700	900	700	900	Ω
V_{IN} = 0V	Full	950	1.3K	800	1K	Ω
V_{IN} = ± 10V	Full	1.1k	1.4k	900	1.1k	Ω
ΔR_{ON} [Side A - Side B]						
V_{IN} = 0V	+25°C	4.0	24	4.0	24	Ω
V_{IN} = ± 10V	+25°C	4.5	27	4.5	27	Ω
V_{IN} = 0V	Full	4.75	28	4.0	24	Ω
V_{IN} = ± 10V	Full	5.5	33	4.5	27	Ω
$I_{S(OFF)}$, Off Input Leakage Current (Note 1)						
Condition 0V	+25°C	30	200	30	200	pA
Condition ± 10V	+25°C	100		100		pA
Condition 0V	Full	2	10	0.2	1	nA
Condition ± 10V	Full	5	25	0.5	2.5	nA
$\Delta I_{S(OFF)}$, [Side A - Side B]						
Condition 0V	+25°C	3	100	3	100	pA
Condition ± 10V	+25°C	10		10		pA
Condition 0V	Full	0.2	2	0.02	0.2	nA
Condition ± 10V	Full	0.5	5	0.05	0.5	nA
$I_{D(OFF)}$, Off Output Leakage Current (Note 1)						
Condition 0V	+25°C	30	200	30	200	pA
Condition ± 10V	+25°C	100		100		pA
Condition 0V	Full	2	10	0.2	1	nA
Condition ± 10V	Full	5	25	0.5	2.5	nA
$\Delta I_{D(OFF)}$, [Side A - Side B]						
Condition 0V	+25°C	3	100	3	100	pA
Condition ± 10V	+25°C	10		10		pA
Condition 0V	Full	0.2	2	0.02	0.2	nA
Condition ± 10V	Full	0.5	5	0.05	0.5	nA
$I_{D(ON)}$, On Channel Leakage Current (Note 1)						
Condition 0V	+25°C	50	200	50	200	pA
Condition ± 10V	+25°C	150		150		pA
Condition 0V	Full	5	25	0.5	2.5	nA
Condition ± 10V	Full	6	40	0.8	4.0	nA
$\Delta I_{D(ON)}$ [Side A - Side B]						
Condition 0V	+25°C	10	100	10	100	pA
Condition ± 10V	+25°C	30		30		pA
Condition 0V	Full	0.5	5	0.05	0.5	nA
Condition ± 10V	Full	0.6	6	0.08	0.8	nA
ΔV_{OS}, Differential Offset Voltage	+25°C	0.02	0.04	0.02	0.04	μV
	Full	0.70	10	0.08	1.0	μV

PARAMETER	TEMP	HI-539-2, -8		HI-539-4, -5		UNITS
		TYP	MAX (MIN)	TYP	MAX (MIN)	
DIGITAL INPUT CHARACTERISTICS						
V_{AL}, Input Low Threshold	Full		0.8		0.8	V
V_{AH}, Input High Threshold	Full		(4.0)		(4.0)	V
I_{AH}, Input Leakage Current (High)	Full		1		1	μA
I_{AL}, Input Leakage Current (Low)	Full		1		1	μA
SWITCHING CHARACTERISTICS						
T_A, Access Time	+25°C	250	750	250	750	ns
	Full	450	1,000	450	1,000	ns
T_{open}, Break-Before-Make Delay	+25°C	85	(30)	85	(30)	ns
	Full		(30)		(30)	ns
$T_{ON(EN)}$, Enable Delay On	+25°C	250	750	250	750	ns
	Full		1,000		1,000	ns
$T_{OFF(EN)}$, Enable Delay Off	+25°C	160	650	160	650	ns
	Full		900		900	ns
Settling Time, to ±0.01%	+25°C	0.9		0.9		μs
Charge Injection (Output)	Full	3		3		pC
Δ Charge Injection (Output)	Full	0.1		0.1		pC
Charge Injection (Input)	Full	10		10		pC
Differential Crosstalk (Note 3)	+25°C	124		124		dB
Single Ended Crosstalk (Note 3)	+25°C	100		100		dB
$C_{S(OFF)}$, Channel Input Capacitance	Full	5		5		pF
$C_{D(OFF)}$, Channel Output Capacitance	Full	7		7		pF
$C_{D(ON)}$, Channel On Output Capacitance	Full	17		17		pF
C_{DS}, Input to Output Capacitance (Note 4)	Full	0.08		0.08		pF
C_A, Digital Input Capacitance	Full	3		3		pF
POWER REQUIREMENTS						
P_D, Power Dissipation	+25°C	2.5		2.5		mW
	Full		45		45	mW
I+ Current	+25°C	0.150		0.150		mA
	Full		2.0		2.0	mA
I- Current	+25°C	0.001		0.001		mA
	Full		1.0		1.0	mA
±V, Supply Voltage Range	Full	±15	(±5)/ ±18	±15	(±5)/ ±18	V

NOTES

1. See Test Circuits #2, 3, 4. The condition ±10V means:

   $I_{S(OFF)}$ and $I_{D(OFF)}$: (V_S = +10V, V_D = -10V), then (V_S = -10V, V_D = +10V)

   $I_{D(ON)}$: (+10V, then -10V)

2. ΔV_{OS} (Exclusive of thermocouple effects) = $R_{ON}\,\Delta I_{D(ON)} + I_{D(ON)}\,\Delta R_{ON}$.

   See Applications section for discussion of additional V_{OS} error.

3. V_{IN} = 1kHz, 15V_{p-p} on all but the selected channel. See Test Circuit #9.

4. Calculated from typical Single-Ended Crosstalk performance.

HARRIS

HI-562A

12 Bit High Speed Monolithic Digital-to-Analog Converter

FEATURES

- OUTPUT CURRENT 2mA, F.S.
- MONOLITHIC CONSTRUCTION
- EXTREMELY FAST SETTLING 300ns TO 0.01% (TYP.)
- LOW GAIN DRIFT ±10ppm/°C (MAX.)
- EXCELLENT LINEARITY ±1/2 LSB (MAX.)
- DESIGNED FOR MINIMUM GLITCHES
- MONOTONIC OVER TEMPERATURE
- NOTE: HI-562A IS RECOMMENDED FOR NEW DESIGNS

APPLICATIONS

- CRT DISPLAY GENERATION
- HIGH SPEED A/D CONVERTERS
- VIDEO SIGNAL RECONSTRUCTION
- WAVEFORM SYNTHESIZERS
- HIGH SPEED DATA ACQUISITION
- HIGH-REL APPLICATIONS
- PRECISION INSTRUMENTS

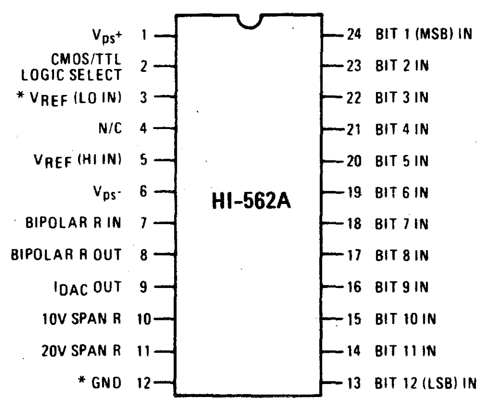
DESCRIPTION

The Harris HI-562A is the first monolithic digital-to-analog converter to combine both ultra-high speed performance and 12-bit accuracy on the same chip. The HI-562A's fast output current settling of 300ns to 0.01% is achieved using dielectric isolation processing to reduce internal parasitics for fast rise and fall times during switching. Output glitches are minimized in the HI-562A by incorporating equally weighted current sources switched into an R-2R ladder network for symmetrical turn-ON and turn-OFF switching times. This creates within the chip a very uniform constant thermal distribution for excellent linearity and also completely eliminates thermal transients during switching. High stability thin film resistor processing together with laser trimming provide the HI-562A with guaranteed true 12-bit linearity to within ±1/2 LSB maximum at +25°C for -4 and -5 parts, and to within ±1/4 LSB maximum at +25°C for -2 and -8 parts. The HI-562A is recommended as a replacement for higher cost hybrid and modular units for increased reliability and accuracy in applications such as CRT displays, precision instruments and data acquisition systems requiring throughput rates as a high as 3.3 MHz for full range transitions. Its small size makes it an ideal choice as the heart of high speed A/D converter designs or as a building block in high speed or high resolution industrial process control systems. The HI-562A is also ideally suited for aircraft and space instrumentation where operation over a wide temperature range is required.

The HI-562A-5 is specified for operation over 0°C to +75°C, the HI-562A-4 over -25°C to +85°C and the HI-562A-2 and HI-562A-8 over -55°C to +125°C. Processing MIL-STD-883A Class B screening is available by selecting the HI-562A-8. All are available in a hermetically sealed 24-lead dual-in-line package.

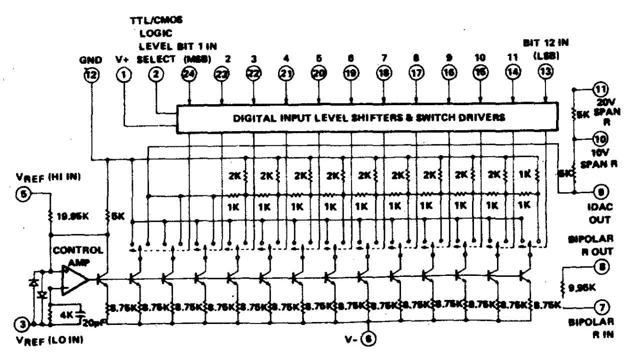
PINOUT

Section 11 for Packaging



*Pin 3 connected to bottom case for high frequency shielding.

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Referred to Ground)[1]

Power Supply Inputs	$V_{ps}+$	+20V	Power Dissipation	P_d, Package	1000mW
	$V_{ps}-$	-20V	Operating Temperature Range		
Reference Inputs	VREF (Hi)	$\pm V_{ps}$	HI-562A-2		-55°C to +125°C
Digital Inputs	Bits 1-12	-1V, +12V	HI-562A-4		-25°C to +85°C
	CMOS/TTL Logic Select	-1V, +12V	HI-562A-5		0°C to +75°C
Outputs	Pins 7, 8, 10, 11	$\pm V_{ps}$	HI-562A-8		-55°C to +125°C
	Pin 9	$+V_{ps}$, -5V	Storage Temperature Range		-65°C to +150°C

ELECTRICAL CHARACTERISTICS (@ +25°C, $V_{ps}+$, = +5V, $V_{ps}-$ = -15V, V_{REF} = +10V, pin 2 tied to pin 12 unless otherwise noted)

PARAMETER	CONDITIONS	HI-562A-2/HI-562A-8 MIN	TYP	MAX	HI-562A-4/HI-562A-5 MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Digital Inputs (3)	Bit ON "Logic 1" Bit OFF "Logic 0"							
TTL Input Voltage (2)								
Logic "1"	Over full temp. range Pin 2 tied to Pin 12	2.0			2.0			V
Logic "0"				0.8			0.8	V
TTL Input Current (2)								
Logic "1"			20	±500		20	±500	nA
Logic "0"			-50	-100		-50	-100	μA
CMOS Input Voltage								
Logic "1"	Connect pin 2 to pin 1 for $V_{ps+} \geq 9.5V$. Otherwise (for CMOS levels below 8V), connect pin 2 to pin 12.	$0.7V_{ps}+$			$0.7V_{ps}+$			V
Logic "0"				$0.3V_{ps}+$			$0.3V_{ps}+$	V
CMOS Input Current								
Logic "1"			20	±500		20	±500	nA
Logic "0"			-50	-100		-50	-100	μA
Reference Input								
Input Resistance			19.95K			19.95K		Ω
Input Voltage			+10			+10		V
TRANSFER CHARACTERISTICS								
Resolution	Over full temp. range			12			12	Bits
Nonlinearity (3)	@ +25°C			±1/4		±1/4	±1/2	LSB
	Over full temp. range		±1/2	±1			±1	LSB
Differential Nonlinearity (3)	@ +25°C			±1/4		±1/4	±1/2	LSB
	Over full temp. range		MONOTONICITY GUARANTEED					
Relative Accuracy (6)	With 50Ω (1%) Trim Resistors							
Gain Error	All Bits ON		±.024	±0.25		±.024	±0.25	% FSR (4)
Bipolar Offset Error	All Bits OFF		±.024	±0.25		±.024	±0.25	% FSR (4)
Unipolar Offset Error	All Bits OFF		±.012	±0.05		±.012	±0.05	% FSR (4)
Adjustment Range	See Operating Instructions							
Gain	With 100Ω Trim Potentiometers		±0.25			±0.25		% FSR
Bipolar Offset			±0.5			±0.5		% FSR
Temperature Stability	Drift specified with internal span resistors for voltage output							
Gain Drift (3)	Over full temp. range		±6	±10			±10	ppm of FSR/°C
Offset Drift (3)								
Unipolar Offset	All Bits OFF			±2			±2	ppm of FSR/°C
Bipolar Offset				±4			±4	ppm of FSR/°C
Differential Nonlinearity	Over full temp. range		±1	±2		±1	±2	ppm of FSR/°C
Settling Time (3) to ±1/2 LSB	All Bits ON-to-OFF or OFF-to-ON		300	400		300	400	ns

SPECIFICATIONS (continued)

PARAMETER	CONDITIONS	HI-562A-2/HI-562A-8 MIN	TYP	MAX	HI-562A-4/HI-562A-5 MIN	TYP	MAX	UNITS
Major Carry Transient								
Peak Amplitude	From 011...1 to 100...0 or 100...0 to 011...1		0.7			0.7		mA
Settling Time to 90% Complete			35			35		ns
Power Supply Sensitivity (3)								ppm of FSR/% V_{ps}
Unipolar Offset	All Bits OFF							
$V_{ps}+$ @ +5V			±0.5			±0.5		
$V_{ps}-$ @ -15V			±0.5			±0.5		
Bipolar Offset								
$V_{ps}+$ @ 5V	All Bits OFF, Bipolar mode		±1.5			±1.5		
$V_{ps}-$ @ -15V			±1.5			±1.5		
Gain								
$V_{ps}+$ @ +5V	All Bits ON			±3.5			±3.5	
$V_{ps}-$ @ -15V				±7.5			±7.5	
OUTPUT CHARACTERISTICS								
Output Current								mA
Unipolar		-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	
Bipolar		±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	
Resistance			2K			2K		ohms
Capacitance			20			20		pF
Output Voltage Ranges								
Unipolar	Using external op amp and internal scaling		0 to +5 0 to +10			0 to +5 0 to +10		V
Bipolar	resistors. See Figure 1 and Table 1 for connections		±2.5 ±5 ±10			±2.5 ±5 ±10		V
Compliance Limit (3)		-3		+10	-3		+10	V
Compliance Voltage (3)	Over full temp. range		±1.0			±1.0		V
Output Noise	0.1 to 10Hz (All Bits ON) 0.1 to 5MHz (All Bits ON)		30 100			30 100		μV (p-p)
POWER REQUIREMENTS								
$V_{ps}+$ (7) $V_{ps}-$	Over full temp. range	4.5 -13.5	5 -15	16.5 -16.5	4.75 -13.5	5 -15	16.5 -16.5	V
$I_{ps}+$ (5) $I_{ps}-$ (5)	All Bits ON or OFF in either TTL or CMOS mode (25°C)		8 16	15 23		8 16	15 23	mA
$I_{ps}+$ (5) $I_{ps}-$ (5)	Same as above except over full temp. range		11 20	20 30		11 20	20 30	mA
Power Dissipation	+25°C $V_{ps}+$ = +5V $V_{ps}-$ = -15V		280	420				mW

HARRIS

HI-565A

High Speed Monolithic Digital to Analog Converter with Reference

FEATURES

- DAC AND REFERENCE ON A SINGLE CHIP
- PIN COMPATIBLE WITH AD565A
- VERY HIGH SPEED: SETTLES TO 1/2 LSB IN 250ns, MAX. FULL SCALE SWITCHING TIME 30ns, TYP.
- GUARANTEED FOR OPERATION WITH ±12V SUPPLIES
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- 1/2 LSB MAX NONLINEARITY GUARANTEED OVER TEMPERATURE
- LOW GAIN DRIFT (MAX, DAC PLUS REFERENCE) 25ppm/°C
- LOW POWER DISSIPATION 250mW

APPLICATIONS

- CRT DISPLAYS
- HIGH SPEED A/D CONVERTERS
- SIGNAL RECONSTRUCTION
- WAVEFORM SYNTHESIS

DESCRIPTION

The HI-565A is a fast, 12 bit current output, digital to analog converter. The monolithic chip includes a precision voltage reference, thin-film R-2R ladder, reference control amplifier and twelve high-speed bipolar current switches.

The Harris Semiconductor dielectric isolation process provides latch-free operation while minimizing stray capacitance and leakage currents, to produce an excellent combination of speed and accuracy. Also, ground currents are minimized to produce a low and constant current through the ground terminal, which reduces error due to code-dependent ground currents.

HI-565A dice are laser trimmed for a maximum integral nonlinearity error of ±1/4 LSB at +25°C. In addition, the low noise buried zener reference is trimmed both for absolute value and minimum temperature coefficient.

The HI-565A is offered in both commercial and military grades. For high-reliability requirements, additional 100% screening per Mil-Std. 883, Method 5004, Class B is available. See Ordering Information.

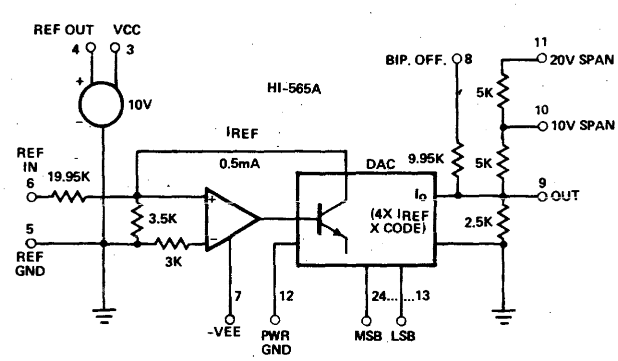
Package is a 24 pin side-brazed ceramic or plastic DIP. Power requirement is 250mW, typical with ±15V supplies.

PINOUT

TOP VIEW

Function	Pin	Pin	Function
NC	1	24	BIT 1 (MSB) IN
NC	2	23	BIT 2 IN
V_{CC}	3	22	BIT 3 IN
REF OUT (+10V)	4	21	BIT 4 IN
REF GND	5	20	BIT 5 IN
REF IN	6	19	BIT 6 IN
$-V_{EE}$	7	18	BIT 7 IN
BIPOLAR R IN	8	17	BIT 8 IN
IDAC OUT	9	16	BIT 9 IN
10V SPAN R	10	15	BIT 10 IN
20V SPAN R	11	14	BIT 11 IN
POWER GND	12	13	BIT 12 (LSB) IN

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

V_{CC} to Power Ground	0V to +18V	10V Span R to Reference Ground	±12V
V_{EE} to Power Ground	0V to -18V	20V Span R to Reference Ground	±24V
Voltage on DAC Output (Pin 9)	-3V to +12V	Ref Out	Indefinite Short to Power Ground Momentary Short to V_{CC}
Digital Inputs (Pins 13-24) to Power Ground	-1V to +7.0V	Package Power Dissipation	
Ref In to Reference Ground	±12V	Ceramic (D)	1000mW
Bipolar Offset to Reference Ground	±12V	Plastic (N)	750mW

**Absolute maximum ratings are limiting values beyond which the serviceability of the circuit may be impaired.*

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = +15V, V_{EE} = -15V, Unless Otherwise Specified)

MODEL	HI-565AJ, HI-565AS			HI-565AK, HI-565AT			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
DATA INPUTS (Note 1) (Pins 13 to 24)							
TTL or 5V CMOS (T_{MIN} to T_{MAX})							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"			+0.8			+0.8	V
Logic Current (Each Bit)							
Bit ON Logic "1"		.01	+1.0		.01	+1.0	μA
Bit OFF Logic "0"		-2.0	-20		-2.0	-20	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current Unipolar (All Bits On)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (All Bits on or Off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (Exclusive of Span Resistors)	1.8k	2.5k	3.2k	1.8k	2.5k	3.2k	Ω
Offset Unipolar		0.01	0.05		0.01	0.05	% of F.S.
Bipolar (Figure 2, R_3 = 50Ω Fixed)		0.05	0.15		0.05	0.1	% of F.S.
Capacitance		20			20		pF
Compliance Voltage, T_{MIN} to T_{MAX}	-1.5		+10	-1.5		+10	V
ACCURACY (Error Relative to Full Scale)							
+25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S.
T_{MIN} to T_{MAX}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% OF F.S.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{MIN} to T_{MAX}	MONOTONICITY GUARANTEED						
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		15	40		10	25	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2 LSB							
With High Z External Load (Note 2)		350	500		350	500	ns
With 75Ω External Load		150	250		150	250	ns

MODEL	HI-565AJ, HI-565AS			HI-565AK, HI-565AT			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
FULL SCALE TRANSITION (From 50% of Logic Input to 90% of Analog Output)							
Rise Time		15	30		15	30	ns
Fall Time		30	50		30	50	ns
TEMPERATURE RANGE							
Operating (HI-565AJ/K)	0		+75	0		+75	°C
(HI-565AS/T)	-55		+125	-55		+125	°C
Storage							
D Package (All)	-65		+150	-65		+150	°C
N Package (J, K)	-25		+150	-25		+150	°C
POWER REQUIREMENTS							
V_{CC}, +11.4 to +16.5V DC		7.0	10.5		7.0	10.5	mA
V_{EE}, -11.4 to -16.5V DC		-9.5	-14.5		-9.5	-14.5	mA
POWER SUPPLY GAIN SENSITIVITY (Note 3)							
V_{CC} = +11.4 to +16.5 VDC		3	10		3	10	ppm of F.S./%
V_{EE} = -11.4 to -16.5 VDC		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGES (See Table 1)		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Figure 1)		±0.1	±0.25		±0.1	±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resistor for R3 (Figure 2)		±0.05	±0.15		±0.05	±0.1	% of F.S.
Gain Adjustment Range (Figure 1)	±0.25			±0.25			% of F.S.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.
REFERENCE INPUT							
Input Impedance	15K	20K	25K	15K	20K	25K	
REFERENCE OUTPUT							
Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (Available for External Loads)	1.5	2.5		1.5	2.5		mA
POWER DISSIPATION		250	375		250	375	mW

NOTES:
1. Guaranteed but not tested over the operating temperature range.
2. See settling time discussion and Figure 3.
3. The Power Supply Gain Sensitivity is tested in reference to a V_{CC}, V_{EE} of ±15V.

HARRIS

HI-5610

10 Bit High Speed Monolithic Digital-to-Analog Converter

FEATURES

- MONOLITHIC CONSTRUCTION
- EXTREMELY FAST SETTLING . . . . 85ns TO ½LSB TYP.
- LOW GAIN DRIFT . . . . ±5ppm/°C TYP.
- EXCELLENT LINEARITY OVER TEMPERATURE . . . . ± ½LSB MAX.
- DESIGNED FOR MINIMUM GLITCHES
- MONOTONIC OVER TEMPERATURE

APPLICATIONS

- CRT DISPLAY GENERATION
- HIGH SPEED A/D CONVERTERS
- VIDEO SIGNAL RECONSTRUCTION
- WAVEFORM SYNTHESIZERS
- HIGH SPEED DATA ACQUISITION
- HIGH RELIABILITY APPLICATIONS
- PRECISION INSTRUMENTS

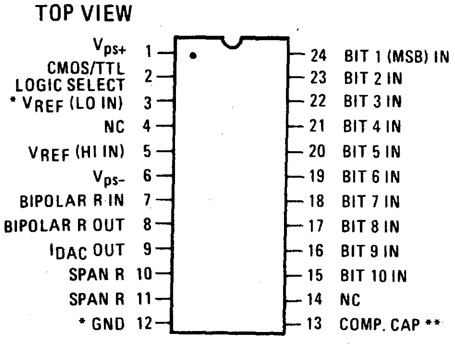
DESCRIPTION

The HI-5610 is an ultra-high speed 10 bit monolithic current output digital-to-analog converter. The fast output current settling of 85ns to ½LSB of its final value is achieved using dielectric isolation processing to reduce internal parasitics for fast rise and fall times during switching. Output glitches are minimized in the HI-5610 by incorporating equally weighted current sources switched into an R-2R ladder network for symmetrical turn-on and turn-off switching times. This creates within the chip a very uniform and constant thermal distribution for excellent linearity and also eliminates thermal transients during switching. High stability thin film resistor processing, together with laser trimming provide the HI-5610 with true 10 bit linearity to within ± ½LSB maximum over operating temperature range. The HI-5610's low offset and gain drift over the operating temperature range assures that its absolute accuracy when referred to a fixed 10V reference will not deviate more than ± 1LSB for both unipolar and bipolar operation.

The HI-5610 is recommended as a replacement for nigh cost hybrid and modular units for increased reliability and accuracy in applications such as CRT Displays, precision instruments and data acquisition system requiring through-put rates as high as 12MHz for full range transitions. Its small size makes it an ideal choice as the essential part of high speed A/D converter designs or as a building block in high speed or high resolution industrial process control systems. The HI-5610 is also ideally suited for aircraft and space instrumentation where operation over a wide temperature range is required.

The HI-5610-5 is specified for operation over 0°C to +75°C, the HI-5610-2 and HI-5610-8 over -55°C to +125°C. Processing to MIL-STD-883A class B screening is available by selecting the HI-5610-8. All are available in a hermetically sealed 24 lead dual-in-line package.

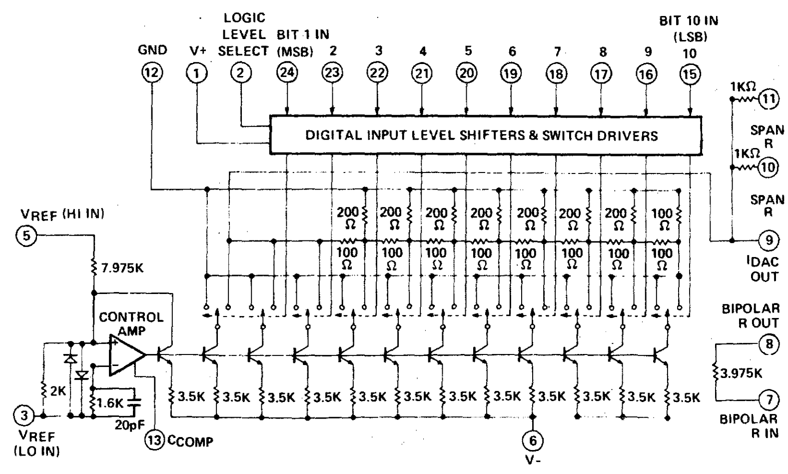
PINOUT



* Pin 3 connected to bottom case for high frequency shielding.

** For high speed operation, connect 0.01μF between Pin 13 and GND. Otherwise, leave Pin 13 open.

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Referred to Ground)[1]

Power Supply Inputs	$V_{ps}+$	+20V
	$V_{ps}-$	-20V
Reference Inputs	VREF (Hi)	± Vps
	VREF(Lo)	0V
Digital Inputs	Bits 1 - 12	-1V, +12V
	CMOS/TTL Logic Select	-1V, +12V
Outputs	Pins 7, 8, 10, 11	± Vps
	Pin 9	+Vps, -5V

Power Dissipation	Pd, Package	1000mW
Operating Temperature Range		
	HI-5610-2	-55°C to +125°C
	HI-5610-5	0°C to +75°C
	HI-5610-8	-55°C to +125°C
Storage Temperature Range		-65°C to +150°C

ELECTRICAL CHARACTERISTICS (@ +25°C, $V_{ps}+$, = +5V, $V_{ps}-$ = -15V, V_{REF} = +10V, pin 2 ground unless otherwise noted)

		HI-5610-2 HI-5610-8			HI-5610-5			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Digital Inputs (2)								
TTL Logic Input Voltage (3)								
Logic "1"	Full	2.0			2.0			V
Logic "0"	Full			0.8			0.8	V
Input Current								
Logic "1"	Full		20	500		20	500	nA
Logic "0"	Full		-50	-100		-50	-100	μA
CMOS Logic Input Voltage (4)								
Logic "1"	Full	0.7 $V_{ps}+$			0.7$V_{ps}+$			V
Logic "0"	Full			0.3 $V_{ps}+$			0.3$V_{ps}+$	V
Input Current								
Logic "1"	Full		20	500		20	500	nA
Logic "0"	Full		-50	-100		-50	-100	μA
Reference Input								
Input Resistance			8K			8K		Ω
Input Voltage (I_{OUT} = 5mA + 20%)			+10			+10		V
TRANSFER CHARACTERISTICS								
Resolution	Full			10			10	Bits
Nonlinearity (5)	25°C			± ½			±½	LSB
	25°C			± ½			± ½	LSB
Relative Accuracy (6)								
Gain Error								(9)
(Input Code 11....1)			± 0.05			± 0.05		% FSR
Unipolar Offset Error								
(Input Code 00....0)			± 0.05			± 0.05		% FSR
Bipolar Offset Error								
(Input Code 00....0)			± 0.05			± 0.05		% FSR
(Adjustable to zero, see Figure 4, 5)								
Adjustment Range								
Gain			± 0.25			± 0.25		% FSR
Bipolar Offset			± 0.25			± 0.25		% FSR
Temperature Stability								
Gain Drift	Full		± 5			± 5		ppm/°C
Unipolar Offset Drift	Full		± 3			± 3		ppm/°C
Bipolar Offset Drift	Full		± 3			± 3		ppm/°C
Differential Nonlinearity	Full		± 2			± 2		ppm/°C
MONOTONICITY - GUARANTEED OVER FULL OPERATING TEMPERATURE RANGE								
Settling Time to ½LSB (5)								
From all 0's to all 1's						85		ns
From all 1's to all 0's						85		ns
Major Carry Switching to 90% Complete			40			40		ns

PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Power Supply Sensitivity (5)								
$V_{ps}+ = +5V$, $V_{ps}- = -13.5V$ to $-16.5V$								
Gain (Input Code 11....1)				±3.5			±3.5	
Unipolar Offset (Input Code 00....0)			±0.5			±0.5		
Bipolar Offset (Input Code 00....0)			±1.5			±1.5		ppm of FSR/%V_{ps}
$V_{ps}- = -15V$, $V_{ps}+ = 4.5V$ to $5.5V$								
Gain (Input Code 11....1)				±7.5			±7.5	
Unipolar Offset (Input Code 00....0)			±0.5			±0.5		
Bipolar Offset (Input Code 00....0)			±1.5			±1.5		
OUTPUT CHARACTERISTICS								
Output Current								
Unipolar		-4.0	-5.0	-6.0	-4.0	-5.0	-6.0	mA
Bipolar		±2.0	±2.5	±3.0	±2.0	±2.5	±3.0	mA
Output Resistance			200			200		Ω
Output Capacitance			20			20		pF
Output Voltage Range (7)								
Unipolar			+5			+5		V
			+2.5			+2.5		V
Bipolar			±2.5			±2.5		V
			±1.25			±1.25		V
Output Compliance Limit (5)		-3		+10	-3		+10	V
Output Compliance Voltage (5)	Full		±1.5			±1.5		V
Output Noise Voltage (8)								
0.1Hz to 100Hz			10			10		μVp-p
0.1Hz to 1MHz			100			100		μVp-p
POWER REQUIREMENTS								
$V_{ps}+$ (4)	Full	4.5	5	16.5	4.75	5	16.5	V
$V_{ps}-$	Full	-13.5	-15	-16.5	-13.5	-15	-16.5	V
$I_{ps}+$ (All 1's or all 0's in	25°C		9			9		mA
(10) either TTL or CMOS Mode)	Full		20			20		mA
$I_{ps}-$ (Same as above)	25°C		25			25		mA
(10)	Full		30			30		mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. The HI-5610 accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight binary, offset binary, or two's complement binary. (See operating instructions).
3. For TTL and DTL compatibility connect +5V to pin 1 and ground pin 2. The $V_{ps}+$ tolerance is ±10% for HI-5610-2,-8. And ±5% for HI-5610-5.
4. For CMOS compatibility based on $V_{ps}+ \geq +8V$, (switching thresholds equal $V_{ps}+/2$), connect pins 1 and 2. For CMOS levels below +8V, connect pin 2 to ground only (this provides a threshold of approximately +1.4V).
5. See definitions.
6. Using an external op amp with internal span resistors and 24.9Ω ±1% external trim resistors in place of potentiometers R1 and R2. These errors are adjustable to zero using R1 and R2. (See operating instructions.)
7. Using an external op amp and internal span resistors. (See operating instructions for connections.)
8. Specified for digital input in all '1's or all '0's.
9. FSR is "Full Scale Range" and is 5V for ±2.5V range, 2.5V for ±1.25V range, etc., or 5mA (±20%) for current output.
10. After 30 seconds warm-up.

HARRIS

HI-5618A/5618B

8 Bit High Speed Digital-to-Analog Converters

INTERFACE

Harris Semiconductor

FEATURES

- VERY FAST SETTLING CURRENT OUTPUT 65ns
- MINIMUM NONLINEARITY ERROR
  - HI-5618A ±1/4 LSB MAX
  - HI-5618B ±1/2 LSB MAX
- LOW POWER OPERATION 340mW TYP
- ON-CHIP RESISTORS FOR GAIN AND BIPOLAR OFFSET
- GUARANTEED MONOTONIC OVER TEMPERATURE
- CMOS, TTL, OR DTL COMPATIBLE

APPLICATIONS

- HIGH SPEED PROCESS CONTROL
- CRT DISPLAY GENERATION
- HIGH SPEED A/D CONVERSION
- WAVEFORM SYNTHESIS
- HIGH RELIABILITY APPLICATIONS
- VIDEO SIGNAL RECONSTRUCTION

DESCRIPTION

The HI-5618A/B are very high speed 8 bit current output D/A converters. These monolithic devices are fabricated with dielectrically isolated bipolar processing, which reduces internal parasitic capacitance to allow fast rise and fall times. This achieves a typical full scale settling time of 65ns to ±1/2 LSB. Output glitches are minimized by incorporation of equally weighted current sources, switched to either an R-2R ladder network or ground for symmetrical turn ON and turn OFF times. High stability thin film resistors provide excellent accuracy without trimming. For example, the HI-5618A has ±1/4 LSB maximum nonlinearity error at +25°C, with ±3/8 LSB guaranteed over the full operating temperature range.

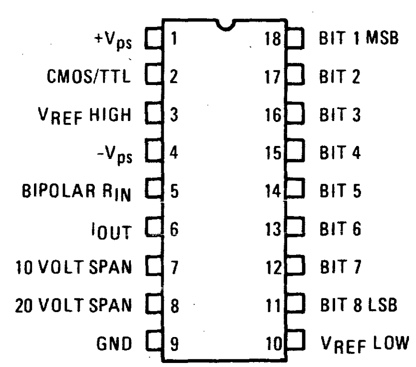
The HI-5618A/B are recommended for any application requiring high speed and accurate conversions. They can be used in CRT displays and systems requiring throughput rates as high as 20MHz for full scale transitions. Other applications include high speed process control, defense systems, avionics, and space instrumentation.

The HI-5618A-5 and HI-5618B-5 are specified for operation from 0°C to +75°C. The "-2" versions are specified from -55°C to +125°C. "Dash 8" (-8) designates parts which have been screened per MIL-STD-883, Method 5004/Class B.

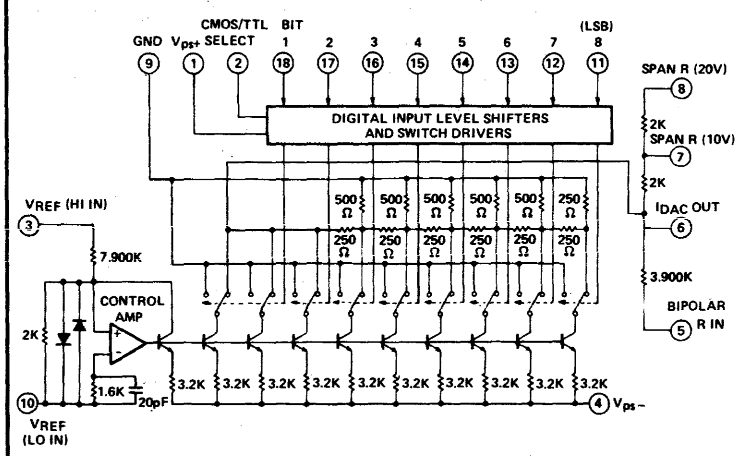
Power requirements are +5V and -15V. Package is an 18 pin DIP, in plastic or ceramic.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Referred to Ground) (1)

Power Supply Inputs	$V_{ps}+$	+20V
	$V_{ps}-$	-20V
Reference Inputs	V_{REF} (Hi)	$\pm V_{ps}$
	V_{REF} (Lo)	0V
Digital Inputs	Bits 1 - 8	-1V, +12V
CMOS/TTL Logic Select		-1V, +12V
Outputs	Pins 5, 7, 8	$\pm V_{ps}$
	Pin 6	$+V_{ps}$, -2.5V

Power Dissipation Pd, Package		700mW
Operating Temperature Range		
	HI-5618A/B-2	-55°C to +125°C
	HI-5618A/B-5	0°C to +75°C
	HI-5618A/B-8	-55°C to +125°C
Storage Temperature Range		-65°C to 150°C

ELECTRICAL CHARACTERISTICS ($V_{ps}+$ = +5V; $V_{ps}-$ = -15V; V_{REF} = +10V; Pin 2 to GND, unless otherwise noted)

PARAMETER		TEMP	HI-5618A/B-2 HI-5618A/B-8 MIN	TYP	MAX	HI-5618A/B-5 MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS									
Digital Inputs (2)									
TTL logic Input Voltage (3)	Logic "1"	Full	2.0			2.0			V
	Logic "0"	Full			0.8			0.8	V
TTL Logic Input Current	Logic "1"	Full		20	500		20	500	nA
	Logic "0"	Full		-50	-100		-50	-100	μA
CMOS Logic Input Voltage (4)	Logic "1"	Full	$0.7V_{ps}+$			$0.7V_{ps}+$			V
	Logic "0"	Full			$0.3V_{ps}+$			$0.3V_{ps}+$	V
CMOS Logic Input Current	Logic "1"	Full		20	500		20	500	nA
	Logic "0"	Full		-50	-100		-50	-100	μA
Reference Input									
Input Resistance		+25°C		8k			8k		Ω
Input Voltage (I_{OUT} = 5mA ± 20%)		+25°C		+10			+10		V
TRANSFER CHARACTERISTICS									
Resolution		Full		8			8		Bits
Nonlinearity, Integral and Differential	HI-5618A	25°C			±1/4			±1/4	LSB
		Full			±3/8			±3/8	LSB
	HI-5618B	25°C			±1/2			±1/2	LSB
		Full			±5/8			±5/8	LSB
Initial Accuracy (6) (Relative to External +10V Reference)									
Gain		25°C			±2			±2	LSB
Unipolar Zero		25°C			±1/8			±1/8	LSB
Bipolar Offset (Neg. Full Scale)		25°C			±2			±2	LSB
Temperature Stability									
Gain Drift		Full			±1/4			±1/4	LSB
Unipolar Zero Drift		Full			±1/16			±1/16	LSB
Bipolar Zero Drift		Full			±1/4			±1/4	LSB
Settling Time (5) to 1/2 LSB High Impedance (11)	(from all 0's to all 1's) or (from all 1's to all 0's)	+25°C		65	75		65	75	ns

PARAMETER	TEMP	HI-5618A/B-2 HI-5618A/B-8 MIN	TYP	MAX	HI-5618A/B-5 MIN	TYP	MAX	UNITS
TRANSFER CHARACTERISTICS (Continued)								
Glitch (5) - Major Carry Transition								
Duration	+25°C		20			20		ns
Amplitude (See Fig. 4)	+25°C		350			350		mV
Area	+25°C		3500			3500		mV–ns
Power Supply Sensitivity (5)								
$V_{ps}+$ = +5V, $V_{ps}-$ = -13V to -16.5V								
Gain (Input Code 11 . . . 1)	+25°C			±5			±5	
Unipolar Zero (Input Code 00 . . . 0)	+25°C		±0.5			±0.5		ppm of
Bipolar Offset (Input Code 00 . . . 0)	+25°C		±1.5			±1.5		FSR/% Vps
								(9)
$V_{ps}-$ = -15V, $V_{ps}+$ = 4.5V to 5.5V								
Gain (Input Code 11 . . . 1)	+25°C			±5			±5	
Unipolar Zero (Input Code 00 . . . 0)	+25°C		±0.5			±0.5		
Bipolar Offset (Input Code 00 . . . 0)	+25°C		±1.5			±1.5		
OUTPUT CHARACTERISTICS								
Output Current Unipolar	+25°C	-4	-5	-6	-4	-5	-6	mA
Bipolar	+25°C	±2.0	±2.5	±3.0	±2.0	±2.5	±3.0	mA
Output Resistance	+25°C		500			500		Ω
Output Capacitance	+25°C		20			20		pF
Output Voltage Range (7) Unipolar	+25°C		+10			+10		V
	+25°C		+5			+5		V
Bipolar	+25°C		±10			±10		V
	+25°C		±5			±5		V
	+25°C		±2.5			±2.5		V
Output Compliance Voltage (5)	+25°C		±1.5			±1.5		V
Output Noise Voltage (8) 0.1Hz to 100Hz	+25°C		30			30		μVp-p
0.1Hz to 1Mhz	+25°C		100			100		μVp-p
POWER REQUIREMENTS (4)								
$V_{ps}+$	Full	4.5	5	16.5	4.75	5	16.5	V
$V_{ps}-$	Full	–13.5	–15	–16.5	–14.25	–15	–15.75	V
$I_{ps}+$ (10) (All 1's or all 0's in either TTL or CMOS mode) (3, 4)	+25°C		9			9		mA
	Full			12			12	mA
$I_{ps}-$ (10) (All 1's or all 0's in either TTL or CMOS mode) (3, 4)	+25°C		19			19		mA
	Full			26			26	mA

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. The HI-5618 accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight binary, offset binary, or two's complement binary. (See operating instructions)
3. For TTL and DTL compatibility connect +5V to pin 1 and ground pin 2. The $V_{ps}+$ tolerance is ± 10% for HI-5618A/B -2, -8; and ± 5% for HI-5618A/B-5.
4. For CMOS compatibility based on $V_{ps}+ \geqslant +8V$, (switching thresholds equal $V_{ps}+/2$), connect pins 1 and 2. For CMOS levels below +8V, connect pin 2 to ground only (this provides a threshold of approximately +1.4V).
5. See definitions.
6. These errors may be adjusted to zero using external potentiometers R_1, R_2, R_3. R_1 and R_2 each provide more than ± 3 LSB's adjustment. (See Operating Instructions). The specifications listed under initial accuracy are based on use of an external op amp, internal span and offset resistors, and 100 Ω ± 1% resistors, in place of R_1 and R_2.
7. Using an external op amp with the internal span and offset resistors. See Operating Instructions.
8. Specified for all "1's" or all "0's" digital input.
9. FSR is "Full Scale Range", i.e., 20V for ± 10V range; 10V for ± 5V range, etc. Nominal full scale output current is 5mA.
10. After 30 seconds warm-up.
11. See Test Circuit, Figure 3.
12. See Test Circuit , Figure 4.

HARRIS

HI-5680

12 Bit Low Cost Monolithic Digital-to-Analog Converter

FEATURES

- DAC 80 ALTERNATE SOURCE
- MONOLITHIC CONSTRUCTION (SINGLE CHIP)
- FAST SETTLING
- GUARANTEED MONOTONIC 0°C to 75°C
- WAFER LASER TRIMMED
- APPLICATIONS RESISTORS ON-CHIP
- ON-BOARD REFERENCE
- DIELECTRIC ISOLATION (DI) PROCESSING
- ±12V POWER SUPPLY OPERATION

APPLICATIONS

- HIGH SPEED A/D CONVERTERS
- PRECISION INSTRUMENTATION
- CRT DISPLAY GENERATION

DESCRIPTION

The HI-5680 is a monolithic, direct replacement for the popular DAC80-CBI, DAC80Z-CBI, and DAC85C-CBI, incorporating the best features of each. Single chip construction, along with several design innovations, make the HI-5680 the optimum choice for low cost, high reliability applications.

Harris' unique Dielectric Isolation(DI) processing reduces internal parasitics, resulting in fast switching times and minimum glitch. On-board span resistors are provided for good tracking over temperature, and are laser trimmed to high accuracy. These may be used with the on-board op-amp (voltage output models; HI-5680V), or with a user supplied external amplifier (HI-5680I).

Internally, the HI-5680 eliminates code dependent ground currents by routing current from the positive supply to the internal ground node, as determined by an auxiliary R-2R ladder. This results in a cancellation of code dependent ground currents allowing virtually zero variation in current through the package common, pin 21.

The HI-5680 is available in both current and voltage output models which are guaranteed over the 0°C to +75°C temperature range. All models include a buried zener reference featuring low temperature coefficient. In addition, the voltage output models include an on-board output amplifier. Both versions operate with a +5V logic supply and a $\pm V_S$ in the range of ±(11.4V to 16.5V).

PINOUTS

TOP VIEW

Function	Pin	Pin	Function
(MSB) BIT 1	1	24	6.3V REF OUT
BIT 2	2	23	GAIN ADJUST
BIT 3	3	22	$+V_S$
BIT 4	4	21	COMMON
BIT 5	5	20	Σ JUNCTION
BIT 6	6	19	20V RANGE
BIT 7	7	18	10V RANGE
BIT 8	8	17	BIPOLAR OFFSET
BIT 9	9	16	REF INPUT
BIT 10	10	15	V_{OUT}
BIT 11	11	14	$-V_S$
(LSB) BIT 12	12	13	LOGIC SUPPLY

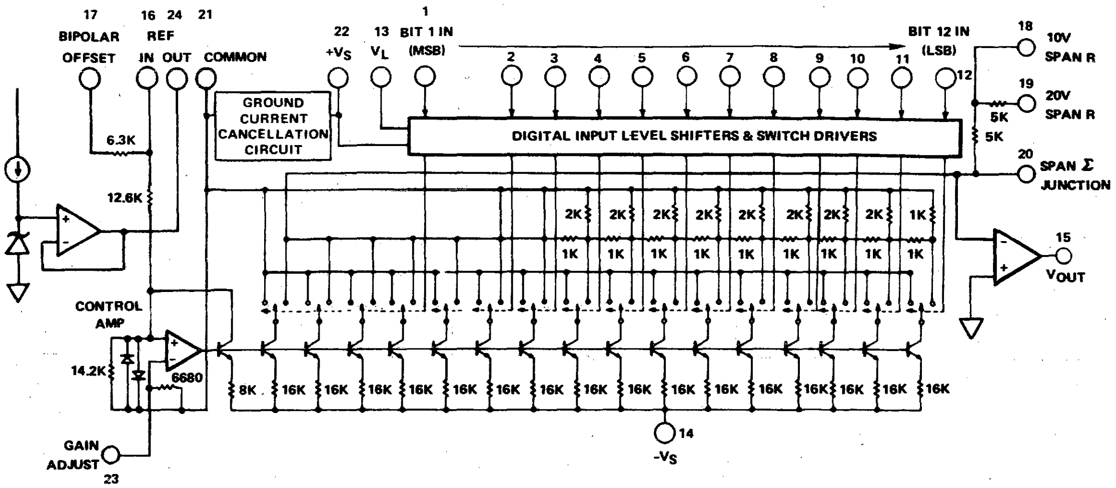
HI-5680V
VOLTAGE OUTPUT

TOP VIEW

Function	Pin	Pin	Function
(MSB) BIT 1	1	24	6.3V REF OUT
BIT 2	2	23	GAIN ADJUST
BIT 3	3	22	$+V_S$
BIT 4	4	21	COMMON
BIT 5	5	20	SCALING NETWORK
BIT 6	6	19	SCALING NETWORK
BIT 7	7	18	SCALING NETWORK
BIT 8	8	17	BIPOLAR OFFSET
BIT 9	9	16	REF INPUT
BIT 10	10	15	I_{OUT}
BIT 11	11	14	$-V_S$
(LSB) BIT 12	12	13	LOGIC SUPPLY

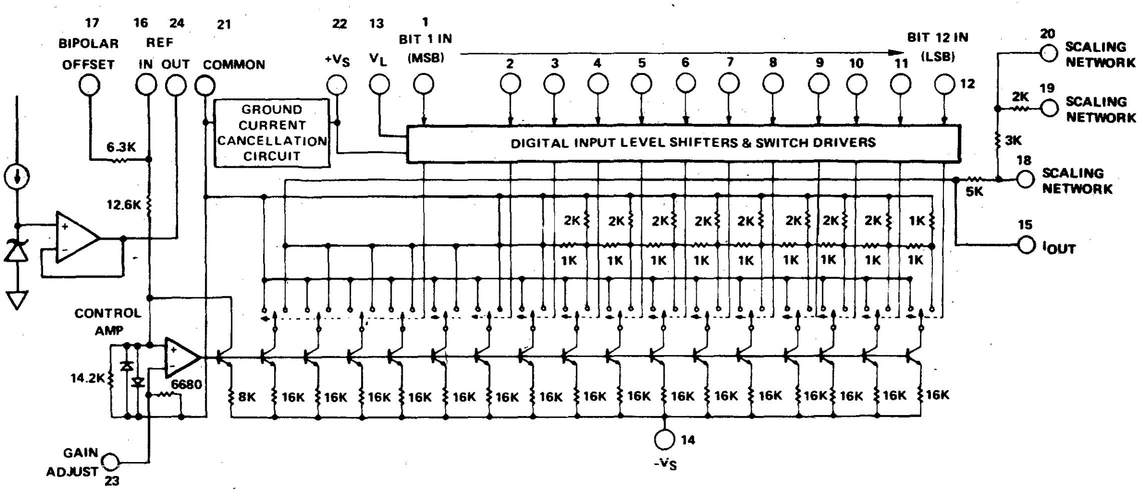
HI-5680I
CURRENT OUTPUT

FUNCTIONAL DIAGRAM VOLTAGE OUTPUT



HI-5680 V

FUNCTIONAL DIAGRAM CURRENT OUTPUT



HI-5680 I

ABSOLUTE MAXIMUM RATINGS (1)

Power Supply Inputs	$+V_s$	+20V
	$-V_s$	−20V
	$+V_{LOGIC}$	+20V
Reference	Input (pin 16)	$+V_s$
	Output drain	2.5mA
Digital Inputs	Bits 1 to 12	−1V to +12V

Power Dissipation	Pd, Package	1000mW
Operating Temperature Range	HI-5680I/V-5	0°C to +75°C
Storage Temperature Range		−65°C to +150°C

ELECTRICAL SPECIFICATIONS

(T_A = +25°C, V_s = ±15V, V_{LOGIC} = +5V, PIN 16 CONNECTED TO PIN 24 UNLESS OTHERWISE SPECIFIED.)

PARAMETER	CONDITIONS	HI-5680X MIN	TYP	MAX	UNITS
DIGITAL INPUT (3)					
Resolution				12	Bits
Logic Levels	TTL Compatible				
Logic "1"	at +1 μA	+2		+5.5	Volts
Logic "0"	at −100 μA	0		+0.8	Volts
ACCURACY (3)					
Linearity Error	0°C to +75°C		±¼	±½	LSB
Differential Lin. Error	0°C to +75°C		±½	±¾	LSB
Gain Error (2)			±0.1	±0.3	%FSR
Offset Error (2)			±.05	±0.15	%FSR
Monotonicity	0°C to +75°C		Guaranteed		
DRIFT (3)	0°C to +75°C				
Total Bipolar Drift (Includes gain, offset and linearity drifts.)				±20	PPM/°C
Total Error	0°C to +75°C				
Unipolar			±.08	±0.15	%FSR
Bipolar			±.06	±.1	%FSR
Gain	Including internal reference		±15	±30	PPM/°C
	Exclusive of internal reference		±5	±7	PPM/°C
Unipolar Offset			±1	±3	PPM/°C
Bipolar Offset			±5	±10	PPM/°C
CONVERSION SPEED (3)					
Voltage Models					
Settling time (3)	to ±0.01% of FSR for FSR Change				
With 10KΩ Feedback			3		μs
With 5KΩ Feedback			1.5		μs
For 1 LSB change			1.5		μs
Slew Rate		10	15		V/μs
Current Models					
Settling time (3)	to ±0.01% of FSR for FSR Change				
10 to 100Ω load			300		ns
1KΩ load			1000		ns
ANALOG OUTPUT					
Voltage Models					
Output current		±5			mA
Output Resistance			.05		Ω
Short Circuit Duration	to common		continuous		

PARAMETER	CONDITIONS	HI-5680X			UNITS
		MIN	TYP	MAX	
ANALOG OUTPUT					
Current Models					
Output Current					
Unipolar		-1.6	−2	-2.4	mA
Bipolar		±0.8	±1	±1.2	mA
Output Impedance					
Unipolar			2.0		KΩ
Bipolar			2.0		KΩ
Compliance (3)				±2.5	V
INTERNAL REFERENCE					
Output Voltage		+6.174	+6.3	+6.426	V
Output Impedance			1.5		Ω
External Current				+2.5	mA
Tempco of Drift			20		PPM/°C
POWER SUPPLY SENSITIVITY (3)					
+15V supply				.002	%FSR/ΔV_s
−15V supply				.002	
+5V supply				.002	
POWER SUPPLY REQUIREMENTS (5)					
Range					
+15V		+11.4	+15	+16.5	V
−15V		−11.4	−15	−16.5	V
+5V		+ 4.5	+ 5	+16.5	V
Current					
+15V			8	11	mA
- 15V			-12	−20	mA
+5V			4.5	8	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Adjustable to zero using external potentiometers.
3. See definitions.
4. FSR is "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc., or 2mA (±20%) for current output.
5. The HI-5680 will operate with supply voltages as low as ±11.4V. It is recommended that output voltage range −10V to +10V not be used if the supply voltages are less than ±12.5V.

DIGITAL INPUTS

The HI-5680 accepts digital input codes in complementary binary, complementary offset binary, and complementary two's complement binary.

DIGITAL INPUT	ANALOG OUTPUT		
	Complementary Binary	Complementary Offset Binary	Complementary Two's Complement*
MSB LSB			
000...000	+ Full Scale	+ Full Scale	– LSB
100...000	Mid Scale-1LSB	–1 LSB	+Full Scale
111...111	Zero	– Full Scale	Zero
011...111	+½ Full Scale	Zero	– Full Scale

*Invert MSB with external inverter to obtain CTC Coding

SETTLING TIME

That interval between application of a digital step input, and final entry of the analog output within a specified window about the settled value. Harris Semicondutor usually specifies a unipolar 10V full scale step, to be measured from 50% of the input digital transition, and a window of ±½ LSB about the final value. The device output is then rated according to the worst (longest settling) case: low to high, or high to low.

DRIFT

GAIN DRIFT – The change in full scale analog output over the specified temperature range expressed in parts per million of full scale per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H –25°C) and low ranges (+25°C–T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT – The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H –25°C) and low (+25°C –T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

ACCURACY

INTEGRAL NONLINEARITY – The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to "end-point linearity" for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00...0 and 11...1).

DIFFERENTIAL NONLINEARITY – The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY – The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in –15V, or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from inequal internal ON–OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably. (Measured as one half the product of duration and amplitude.)

DECOUPLING AND GROUNDING

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-5680 (preferrably to the device pins) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

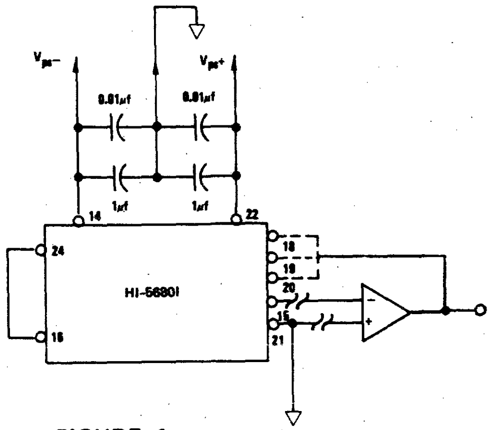


FIGURE 1

REFERENCE SUPPLY

An internal 6.3Volt reference is provided on board all HI-5680 models. This voltage (pin 24) is accurate to ±2% and must be connected to the reference input (pin 16) for specified operation. This reference may be used externally, provided current drain is limited to 2.5mA. An external buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven by the reference will result in gain variations of the HI-5680. All gain adjustments should be made under constant load conditions.

VOLTAGE OUTPUT HI-5680V

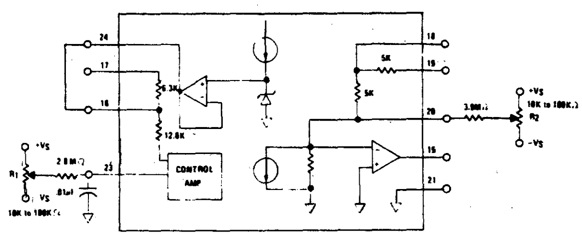


FIGURE 2

RANGE CONNECTIONS

	Range	Connect PIN 15	PIN 17	PIN 19
Unipolar	0 to +5V	18	N.C.	20
	0 to +10V	18	N.C.	N.C.
Bipolar	± 2.5V	18	20	20
	±5V	18	20	N.C.
	±10V	19	20	15

CURRENT OUTPUT HI-5680I

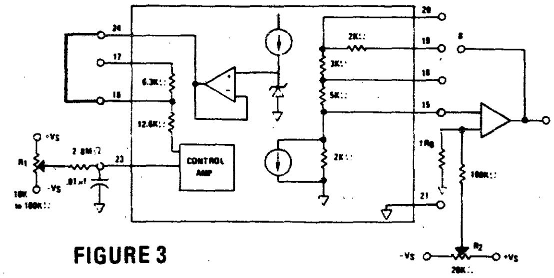


FIGURE 3

EXTERNAL AMPLIFIER CONNECTIONS

To use the HI-5680I with an external amplifier, connect as follows:

Range	Pin 17 to	Pin 18 to	Pin 19 to	Pin 20 to
0 to +10V	N.C.	B	18*	19*
0 to +5V	N.C.	B	15	N.C.
±10V	15	N.C.	B	N.C.
±5V	15	B	18*	19*
±2.5V	15	B	15	N.C.

*these connections help reduce stray capacitance in the feedback loop.
†R_B should equal the DAC's output resistance, which is 2KΩ // $R_{FEEDBACK}$.

GAIN AND OFFSET CALIBRATION

(Applies to Figure 2 and 3.)

UNIPOLAR CALIBRATION

Step 1: Offset
- Turn all bits OFF (11...1)
- Adjust R_2 for zero volts out

Step 2: Gain
- Turn all bits ON (00...0)
- Adjust R_1 for FS-1LSB
- That Is:
  - 4.9988 for 0 to +5V range
  - 9.9976 for 0 to +10V range

BIPOLAR CALIBRATION

Step 1: Offset
- Turn all bits OFF (11...1)
- Adjust R_2 for Negative FS
- That Is:
  - −10V for ±10V range
  - −5V for ±5V range
  - −2.5V for ±2.5 range

Step 2: Gain
- Turn all bits ON (00...0)
- Adjust R_1 for positive FS-1LSB
- That Is:
  - +9.9951V for ±10V range
  - +4.9976V for ±5V range
  - +2.4988V for ±2.5V range

This Bipolar procedure adjusts the output range end points. The maximum error at zero (half scale) will not exceed the Linearity error. See the "Accuracy" specifications.

HARRIS

HI-5685

High Performance Monolithic 12 Bit Digital-to-Analog Converter

FEATURES

- DAC 85 ALTERNATE SOURCE
- MONOLITHIC CONSTRUCTION (SINGLE CHIP)
- FAST SETTLING
- GUARANTEED MONOTONIC −25°C TO +85°C
- WAFER LASER TRIMMED
- APPLICATIONS RESISTORS ON-CHIP
- ON-BOARD REFERENCE
- DIELECTRIC ISOLATION (DI) PROCESSING
- ±12V POWER SUPPLY OPERATION

APPLICATIONS

- HIGH SPEED A/D CONVERTERS
- PRECISION INSTRUMENTATION
- CRT DISPLAY GENERATION

DESCRIPTION

The HI-5685 is a monolithic direct replacement for the popular DAC85-CBI and the ADDAC85LD-CBI. Single chip construction along with several design innovations make the HI-5685 the optimum choice for low cost, high reliability applications.

Harris' unique Dielectric Isolation (DI) processing reduces internal parasitics resulting in fast switching times and minimum glitch. On board span resistors are provided for good tracking over temperature, and are laser trimmed to high accuracy. These may be used with the on-board op-amp (voltage output models; HI-5685V), or with a user supplied external amplifier (HI-5685I).

Internally, the HI-5685 eliminates code dependent ground currents by routing current from the positive supply to the internal ground node, as determined by an auxiliary R-2R ladder. This results in a cancellation of code dependent ground currents allowing virtually zero variation in current through the package common, pin 21.

The HI-5685 and HI-5685A are available in both current and voltage output models which are guaranteed over the −25°C to +85°C temperature range. All models include a buried zener reference featuring low temperature coefficient. In addition, the voltage output models include an on-board output amplifier. Both versions operate with a +5V logic supply and a $\pm V_S$ in the range of ±(11.4V to 16.5V).

The HI-5685A offers exceptionally low drift over temperature. Gain drift is a maximum ±10ppm/°C, over −25°C to +85°C.

PINOUTS

TOP VIEW

Function	Pin	Pin	Function
(MSB) BIT 1	1	24	6.3V REF OUT
BIT 2	2	23	GAIN ADJUST
BIT 3	3	22	$+V_S$
BIT 4	4	21	COMMON
BIT 5	5	20	Σ JUNCTION
BIT 6	6	19	20V RANGE
BIT 7	7	18	10V RANGE
BIT 8	8	17	BIPOLAR OFFSET
BIT 9	9	16	REF INPUT
BIT 10	10	15	V_{OUT}
BIT 11	11	14	$-V_S$
(LSB) BIT 12	12	13	LOGIC SUPPLY

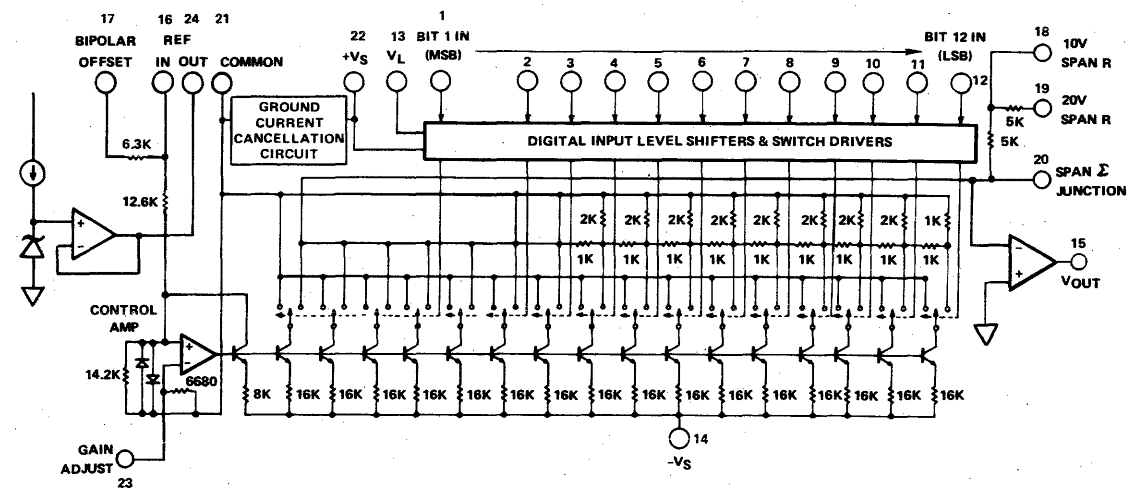
HI-5685V
VOLTAGE OUTPUT

TOP VIEW

Function	Pin	Pin	Function
(MSB) BIT 1	1	24	6.3V REF OUT
BIT 2	2	23	GAIN ADJUST
BIT 3	3	22	$+V_S$
BIT 4	4	21	COMMON
BIT 5	5	20	SCALING NETWORK
BIT 6	6	19	SCALING NETWORK
BIT 7	7	18	SCALING NETWORK
BIT 8	8	17	BIPOLAR OFFSET
BIT 9	9	16	REF INPUT
BIT 10	10	15	I_{OUT}
BIT 11	11	14	$-V_S$
(LSB) BIT 12	12	13	LOGIC SUPPLY

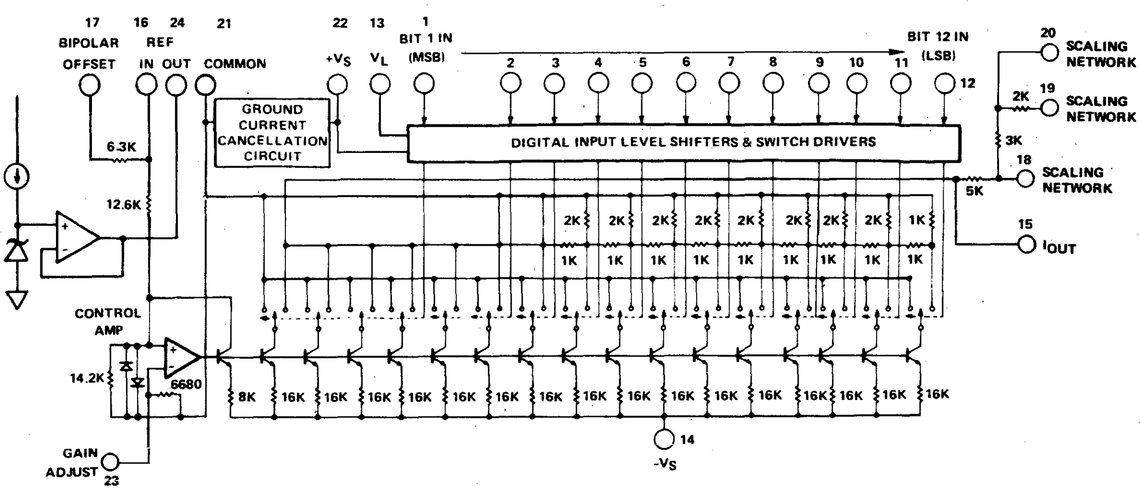
HI-5685I
CURRENT OUTPUT

FUNCTIONAL DIAGRAM VOLTAGE OUTPUT



HI-5685 V

FUNCTIONAL DIAGRAM CURRENT OUTPUT



HI-5685 I

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (1)

Power Supply Inputs	$+V_S$	+20V	Power Dissipation		
	$-V_S$	−20V		Pd, Package	1000mW
	$+V_{LOGIC}$	+20V	Operating Temperature Range		
Reference	Input (pin 16)	$\pm V_S$		HI-5685I/V−4	−25°C to +85°C
	Output drain	2.5mA		HI-5685AI/V−4	−25°C to +85°C
Digital Inputs	Bits 1 to 12	−IV to +12V	Storage Temperature Range		−65° to +150°C

ELECTRICAL SPECIFICATIONS

(T_A=+25°C, V_S = ±15V , V_{LOGIC} = 5V, PIN 16 CONNECTED TO PIN 24 UNLESS OTHERWISE SPECIFIED)

PARAMETER	CONDITIONS	HI-5685			
		MIN	TYP	MAX	UNITS
DIGITAL INPUT (3)					
Resolution				12	Bits
Logic Levels	TTL Compatible				
Logic "1"	at +1 μA	+2		+5.5	V
Logic "0"	at −100 μA	0		+0.8	V
Accuracy (3)					
Linearity Error	at +25°C			±½	LSB
	−25°C to +85°C			±½	LSB
Differential Lin. Error			±½		LSB
Gain Error (2)			±0.1		%FSR (4)
Offset Error (2)			±0.05		%FSR
Monotonicity	−25°C to +85°C		GUARANTEED		
DRIFT (3) HI-5685	−25°C to +85°C				
Gain				±20	
Offset					
Unipolar			±1	±3	PPM/°C
Bipolar			±5	±10	
DRIFT (3) HI-5685A (Low Drift)	−25°C to +85°C				
Gain				±10	
Offset					PPM/°C
Unipolar			±1		
Bipolar				±5	
CONVERSION SPEED					
Voltage Models					
Settling Time (3)	to ±0.01% of FSR for FSR Change				
With 10KΩ Feedback			3		μs
With 5KΩ Feedback			1.5		μs
For 1 LSB Change			1.5		μs
Slew Rate			15		V/μs
Current Models					
Settling Time (3)	to ±0.01% of FSR for FSR Change				
10 to 100Ω load			300		ns
1KΩ load			1.0		μs

PARAMETER	CONDITIONS	HI-5685			
		MIN	TYP	MAX	UNITS
ANALOG OUTPUT					
Voltage Models					
Output Current		±5			mA
Output Impedance (DC)			0.05		Ω
Current Models					
Output Current	Full Scale				
Unipolar		−1.6	−2	−2.4	mA
Bipolar		±0.8	±1	±1.2	mA
Output Resistance					
Unipolar			2.0		KΩ
Bipolar			2.0		KΩ
Compliance (3)		−2.5		+10	V
INTERNAL REFERENCE					
Output voltage		+6.174	+6.3	+6.426	V
Output Impedance			1.5		Ω
External Current				+2.5	mA
Tempco of Drift			±10	±20	PPM/°C
POWER SUPPLY SENSITIVITY (3)					
+15V				.002	$\frac{\%FSR}{\Delta V_S}$
−15V				.002	
+5V				.002	
POWER SUPPLY REQUIREMENTS(5)					
Range					
+15V		+11.4	+15	+16.5	V
−15V		−11.4	−15	−16.5	V
+5V		+4.5	+5	+16.5	V
Current					
+15V			8	11	mA
−15V			-12	−20	mA
+5V			4.5	8	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Adjustable to zero using external potentiometers.
3. See Definitions.
4. FSR is "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc., or 2mA (±20%) for current output.
5. The HI-5685 will operate with supply voltages as low as ±11.4V. It is recommended that output voltage range −10V to +10V not be used if the supply voltages are less than ±12.5V.

HARRIS

HI-5687

Wide Temperature Range Monolithic 12 Bit Digital-to-Analog Converter

FEATURES

- DAC 87 ALTERNATE SOURCE
- MONOLITHIC CONSTRUCTION (SINGLE CHIP)
- FAST SETTLING
- GUARANTEED SPECIFICATIONS -55°C to 125°C
- WAFER LASER TRIMMED
- APPLICATIONS RESISTORS ON-CHIP
- ON-BOARD REFERENCE
- DIELECTRIC ISOLATION (DI) PROCESSING
- ±12V POWER SUPPLY OPERATION
- MIL STD 883 PROCESSING AVAILABLE

APPLICATIONS

- HIGH SPEED A/D CONVERTERS
- PRECISION INSTRUMENTATION
- CRT DISPLAY GENERATION

DESCRIPTION

The HI-5687 is a monolithic direct replacement for the popular DAC87-CBI wide temperature range d-to-a converter. Single chip construction, along with several design innovations make the HI-5687 the optimum choice for low cost, high reliability applications.

Harris' unique Dielectric Isolation (DI) processing reduces internal parasitics resulting in fast switching times and minimum glitch. On board span resistors are provided for good tracking over temperature, and are laser trimmed to high accuracy. These may be used with the on-board op-amp (voltage output models; HI-5687V), or with a user supplied external amplifier (HI-5687I).

Internally, the HI-5687 eliminates code dependent ground currents by routing current from the positive supply to the internal ground mode, as determined by an auxiliary R-2R ladder. This results in a cancellation of code dependent ground currents allowing virtually zero variation in current through the package common, pin 21.

The HI-5687 is available in both current and voltage output models which are 100% tested over the -55°C to +125°C temperature range. All models include a buried zener reference featuring low temperature coefficient. In addition, the voltage output models include an on-board output amplifier. Both versions operate with a +5V logic supply and a $\pm V_S$ in the range of ±(11.4V to 16.5V).

Processing to MIL-STD-883A CLASS B is available. See Ordering Information.

PINOUTS

TOP VIEW

Function	Pin	Pin	Function
(MSB) BIT 1	1	24	6.3V REF OUT
BIT 2	2	23	GAIN ADJUST
BIT 3	3	22	$+V_S$
BIT 4	4	21	COMMON
BIT 5	5	20	Σ JUNCTION
BIT 6	6	19	20V RANGE
BIT 7	7	18	10V RANGE
BIT 8	8	17	BIPOLAR OFFSET
BIT 9	9	16	REF INPUT
BIT 10	10	15	V_{OUT}
BIT 11	11	14	$-V_S$
(LSB) BIT 12	12	13	LOGIC SUPPLY

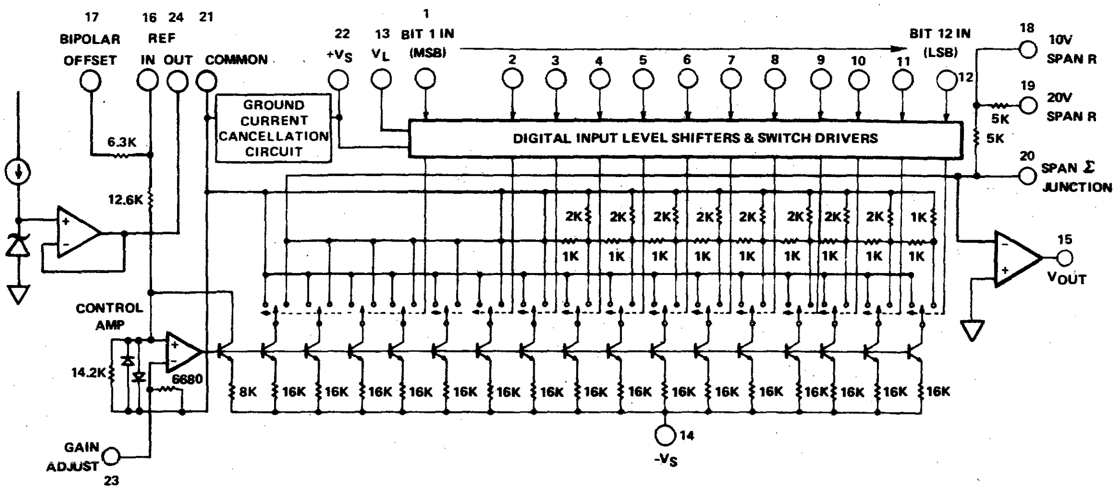
HI-5687V
VOLTAGE OUTPUT

TOP VIEW

Function	Pin	Pin	Function
(MSB) BIT 1	1	24	6.3V REF OUT
BIT 2	2	23	GAIN ADJUST
BIT 3	3	22	$+V_S$
BIT 4	4	21	COMMON
BIT 5	5	20	SCALING NETWORK
BIT 6	6	19	SCALING NETWORK
BIT 7	7	18	SCALING NETWORK
BIT 8	8	17	BIPOLAR OFFSET
BIT 9	9	16	REF INPUT
BIT 10	10	15	I_{OUT}
BIT 11	11	14	$-V_S$
(LSB) BIT 12	12	13	LOGIC SUPPLY

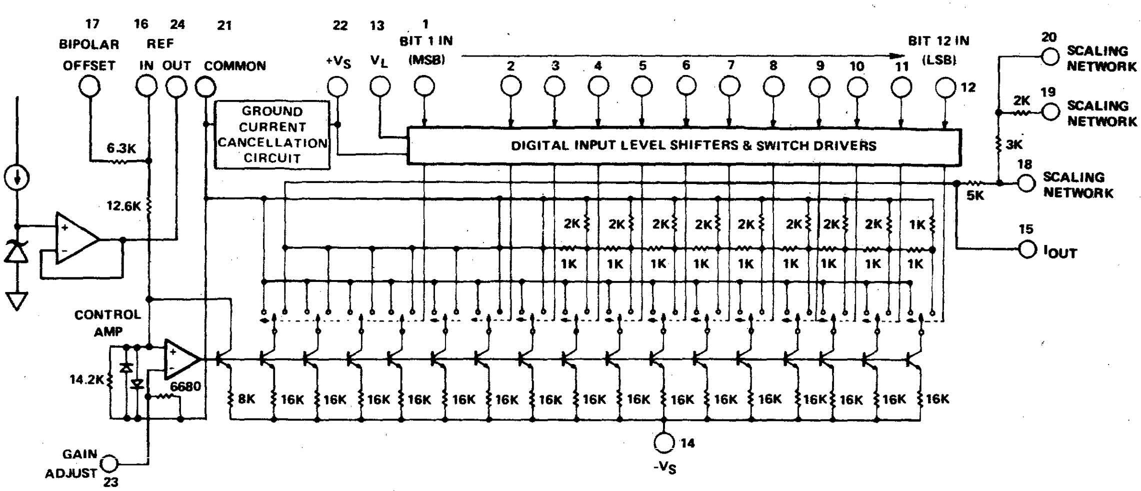
HI-5687I
CURRENT OUTPUT

FUNCTIONAL DIAGRAM VOLTAGE OUTPUT



HI-5687 V

FUNCTIONAL DIAGRAM CURRENT OUTPUT



HI-5687 I

ABSOLUTE MAXIMUM RATINGS (1)

Power Supply Inputs	$+V_S$	+20V
	$-V_S$	−20V
	$+V_{LOGIC}$	+20V
Reference	Input (pin 16)	$\pm V_S$
	Output drain	2.5mA
Digital Inputs	Bits 1 to 12	−1V to +12V

Power Dissipation	Pd, Package	1000mW
Operating Temperature Range		
	HI-5687I/V-2	−55°C to +125°C
	HI-5687I/V-8	−55°C to +125°C
Storage Temperature Range		−65°C to +150°C

ELECTRICAL SPECIFICATIONS

(T_A=+25°C, V_s=±15V, V_{LOGIC} = +5V, PIN 16 CONNECTED TO PIN 24 UNLESS OTHERWISE SPECIFIED.)

PARAMETER	CONDITIONS	HI-5687 MIN	TYP	MAX	UNITS
DIGITAL INPUT (3)					
Resolution				12	Bits
Logic Levels	TTL Compatible				
Logic "1"	at +1μA	+2		+5.5	V
Logic "0"	at −100μA	0		+0.8	V
ACCURACY (3)					
Linearity Error	At +25°C		±¼	±½	LSB
	−55°C to +125°C			+¾	LSB
Differential Lin. Error	at +25°C			±¾	LSB
	−55°C to +125°C		±½	±1	LSB (4)
Gain Error (2)			±0.1	±0.2	%FSR
Offset Error (2)			±0.05	±0.1	%FSR
Monotonicity	−55°C to +125°C		GUARANTEED		
DRIFT (3)	−55°C to +125°C				
Total Bipolar Drift (includes gain, offset and linearity drifts)			±15	±30	PPM/°C
Total Error					
Unipolar			±0.13	±0.3	%FSR
Bipolar			±0.12	±0.24	%FSR
Gain					
including internal reference			±10	±25	PPM/°C
excluding internal reference			±5	±10	PPM/°C
Unipolar Offset			±1	±3	PPM/°C
Bipolar Offset			±5	±10	PPM/°C
CONVERSION SPEED					
Voltage Models					
Settling Time (3)	to ±0.01% of FSR for FSR Change				
With 10KΩ Feedback			3		μs
With 5KΩ Feedback			1.5		μs
For 1 LSB Change			1.5		μs
Slew Rate			15		V/μs
Current Models					
Settling Time (3)	to ±0.01% of FSR for FSR Change				
10 to 100Ω load			300		ns
1KΩ load			1.0		μs

PARAMETER	CONDITIONS	HI-5687			
		MIN	TYP	MAX	UNITS
ANALOG OUTPUT					
Voltage Models					
Output Current		+5			mA
Output Impedance (DC)			0.05		Ω
Current Models					
Output Current	Full Scale				
Unipolar		−1.6	−2	−2.4	mA
Bipolar		±0.8	±1	±1.2	mA
Output Impedance					
Unipolar			2.0		KΩ
Bipolar			2.0		KΩ
Compliance (3)		−1.5		+ 10.5	V
INTERNAL REFERENCE					
Output Voltage		+6.174	+6.3	+6.426	V
Output Impedance			1.5		Ω
External Current				+2.5	mA
Tempco of Drift			±5	±10	PPM/°C
POWER SUPPLY SENSITIVITY (3)					
+15V				±.002	$\frac{\%FSR}{\Delta V_S}$
−15V				±.002	
+5V				±.002	
POWER SUPPLY REQUIREMENTS (5)					
Range					
+15V		+11.4	+15	+16.5	V
−15V		−11.4	−15	−16.5	V
+5V		+4.5	+5	+16.5	V
Current					
+15V			8	11	mA
−15V			-12	−20	mA
+5V			4.5	8	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.

2. Adjustable to zero using external potentiometers.

3. See Definitions.

4. FSR is a "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc., or 2mA (±20%) for current output.

5. The HI-5687 will operate with supply voltages as low as ±11.4V. It is recommended that output voltage ranges −10V to +10V and not be used if the supply voltages are less than ±12.5V.

HARRIS

HI-DAC16B/C

16-Bit D to A Converter

FEATURES

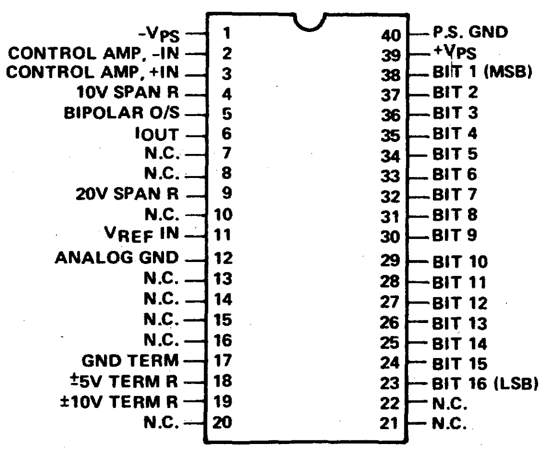
- 16 BIT RESOLUTION
- MONOLITHIC DI BIPOLAR CONSTRUCTION
- FAST SETTLING TIME 1 μs TO .003%FS
- LOW DIFF. NONLIN. DRIFT ± 0.3ppm/°C
- LOW GAIN DRIFT ± 1ppm/°C
- ON-CHIP SPAN & OFFSET RESISTORS
- TTL/5V-CMOS COMPATIBLE
- LOW UNIPOLAR OFFSET ≤ 1/2LSB@ +25°C
- LOW UNIPOLAR OFFSET T.C. ± 0.2ppm/°C
- EXCELLENT STABILITY

APPLICATIONS

- HIGH RESOLUTION CONTROL SYSTEMS
- HIGH FIDELITY AUDIO RECONSTRUCTION
- PRECISION FUNCTION GENERATION AND INSTRUMENTATION

PINOUT

TOP VIEW



DESCRIPTION

The HARRIS HI-DAC16 is a 16-bit, current output D/A converter. Single chip construction includes thin-film application resistors for use with an external op amp. These permit standard output voltage ranges of 0 to +5V, 0 to +10V, ±2.5V, ±5V and ±10V.

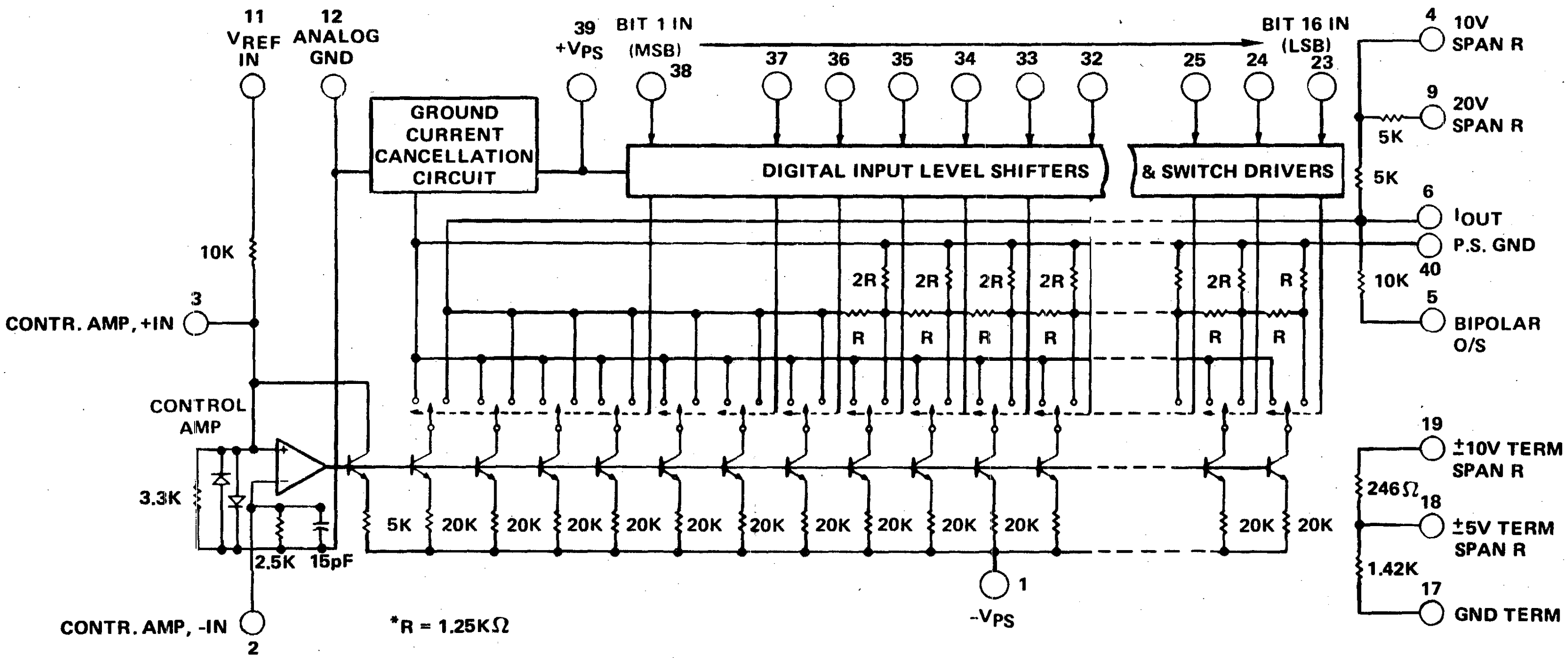
Reference and span resistors have adjacent placement on the chip for optimum match and thermal tracking. Futhermore, this layout feature helps minimize the superposition error caused by self-heating of the span resistor, reducing it to less than 1/10LSB. This and other design innovations have produced exceptionally stable operation over temperature. Typical temperature coefficients are ± 1ppm/°C for gain error and 0.3ppm/°C for differential non-linearity error.

The internal architecture is an extension of the earlier HI-562 with several major improvements. All code dependent ground currents are steered to a separate non-critical path, namely, power supply ground. This feature allows the precision ground of the converter to be sensed with virtually zero voltage drop referred to system ground. The result is the complete elimination of non-linearities due to code dependent ground currents while yielding an extremely low unipolar offset of less than 1/2LSB. Because of this separation, the user may route the precision ground some distance to the system ground without degrading converter accuracy.

The HARRIS HI-DAC16 delivers a stable, accurate output without sacrifice in speed. Settling time to within ±0.003% is one microsecond. Overall performance of this monolithic device should be attractive for applications such as high fidelity audio and high-resolution control systems.

Typical power requirement is 450 MW, from the +15V and -15V supplies combined. The package is a 40 pin ceramic DIP. Two accuracy grades are offered.

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Referred to Ground)

Power Supply Inputs	$V_{ps}+$	+20V
	$V_{ps}-$	−20V
Reference Inputs	V_{REF} (Hi)	$\pm V_{ps}$
Digital Inputs	Bits 1 to 16	−1V, +12V
Outputs		$\pm V_{ps}$

Power Dissipation Pd, Package	1000 mW
Operating Temperature Range	
HI-DAC 16B/C	0°C to +75°C
Storage Temperature Range	−65°C to +150°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{ps} = ±15V, V_{ref} = +10V, unless otherwise specified)

PARAMETER	CONDITIONS	HI-DAC 16B MIN	HI-DAC 16B TYP	HI-DAC 16B MAX	HI-DAC 16C MIN	HI-DAC 16C TYP	HI-DAC 16C MAX	UNITS
INPUT CHARACTERISTICS								
Digital Inputs	Bit ON "Logic 1" / Bit OFF "Logic 0"							
Input Voltage								
Logic "1"	Over full temp. range	2.0			2.0			V
Logic "0"	Over full temp. range			0.8			0.8	V
Input Current								
Logic "1"	Over full temp. range		20	500		20	500	nA
Logic "0"	Over full temp. range	−50			−50			μA
Reference Input								
Input Resistance			10			10		KΩ
Input Voltage			10			10		V
TRANSFER CHARACTERISTICS								
Resolution	Over full temp. range		16			16		Bits
Nonlinearity	@+25°C		±.0023			±.0045		%FSR(3)
	Over full temp. range			±.0045			±.009	%FSR(3)
Differential Nonlinearity	@+25°C		±.0015			±.003		%FSR
	Over full temp. range			±.003			±.006	%FSR
Relative Accuracy (5)	With 100Ω (1%) Trim Resistors							
Unipolar Gain Error	All Bits ON		±.1	±.25		±.1	±.25	%FSR
Bipolar Offset Error	All Bits OFF		±.15			±.15	±.42	%FSR
Unipolar Offset Error	All Bits OFF		±.002			±.002	±.05	%FSR
Adjustment Range	See Operating Instructions							
Gain	Using trim potentiometers as shown in Figure 1			±3			±3	%FSR
Bipolar Offset	Using trim potentiometers as shown in Figure 1			±.43			±.43	%FSR
Temperature Stability	Drift specified with internal span resistors for voltage output							
Gain Drift (2)	Over full temp. range		±1	± 5		±1	± 5	ppm of FSR/°C
Offset Drift (2)								
Unipolar Offset	All Bits OFF		±.2			±.2		ppm of FSR/°C
Bipolar Offset	All Bits OFF		±.5			±.5		ppm of FSR/°C
Differential Nonlinearity	Over full temp. range		±0.3			±0.3		ppm of FSR/°C
Settling Time (2) to ±.003%FS	All Bits ON-to-OFF or OFF-to-ON		1.0			1.0		μs

PARAMETER	CONDITIONS	HI-DAC 16B MIN	HI-DAC 16B TYP	HI-DAC 16B MAX	HI-DAC 16C MIN	HI-DAC 16C TYP	HI-DAC 16C MAX	UNITS
Glitch (2)	From 011 ... 1 to 100 ... 0 or 100 ... 0 to 011... 1		1300			1300		mV–ns
Power Supply (2) Rejection Ratio, PSRR (3) $V_{ps}+$ / $V_{ps}-$			1.5 / 1.5			1.5 / 1.5		ppm of FSR/% V_{ps}
OUTPUT CHARACTERISTICS								
Output Current Unipolar / Bipolar		−1.6 / ±0.8	−2 / ±1	−2.4 / ±1.2	−1.6 / ±0.8	−2 / ±1	−2.4 / ±1.2	mA
Resistance			2.5K			2.5K		ohms
Capacitance			10			10		pF
Output Voltage Ranges Unipolar / Bipolar	Using external op amp and internal scaling resistors. See Figure 1 and Table 1 for connections		0 to +5, 0 to +10 / ±2.5, ±5, ±10			0 to +5, 0 to +10 / ±2.5, ±5, ±10		V
Compliance Limit (2)		−3		+10	−3		+10	V
Compliance Voltage (2)	Over full temp. range		±1			±1		V
Output Noise	0.1 to 5MHz (All Bits ON)		30			30		μVRMS
POWER REQUIREMENTS								
$V_{ps}+$ (7) / $V_{ps}-$	Over full temp. range	13.5 / −13.5	+15 / −15	16.5 / −16.5	13.5 / −13.5	+15 / −15	16.5 / −16.5	V
$I_{ps}+$(4) / $I_{ps}-$(4)	All Bits ON or OFF full temp. range	−25	+13 / −18	+18	−25	+13 / −18	+18	mA
Power Dissipation			465			465		mW

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impared. Functional operation under any of these conditions is not necessarily implied.
2. See Definitions.
3. FSR is "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc., or 2mA (±20%) for current output.
4. After 30 seconds warm-up.
5. Using an external op amp with internal span resistors and specified external trim resistors in place of potentiometers R_1 and R_2. Errors are adjustable to zero using R_1 and R_2 potentiometers. (See Operating Instructions Figure 2.)

HARRIS

HI-5660

High Speed Monolithic Digital-to-Analog Converter

FEATURES

- MONOLITHIC CONSTRUCTION
- FAST SETTLING (TO ±1/2 LSB) 350ns
- ±1/2 LSB MAX. NONLINEARITY GUARANTEED OVER TEMPERATURE
- INTERNAL CANCELLATION OF GROUND CURRENT
- EXCELLENT POWER SUPPLY REJECTION 1ppm/%PS
- LOW COST

APPLICATIONS

- HIGH SPEED A/D CONVERTERS
- CRT DISPLAYS
- WAVEFORM SYNTHESIS

DESCRIPTION

The HI-5660 is a current output, 12 bit monolithic digital-to-analog converter. It offers high speed plus enhanced accuracy, through internal cancellation of ground currents.

Electrical performance is similar to that of the AD566A. Pinouts are identical except for pin 1, which requires a +5V supply (versus no connection on the AD566A).

Fabrication of the HI-5660 features the Harris bipolar dielectric isolation process, which eliminates latchup and minimizes parasitic capacitance and leakage currents. The chip includes nichrome thin-film resistors, laser trimmed at the wafer level to a maximum linearity error of ±1/4 LSB at +25°C.

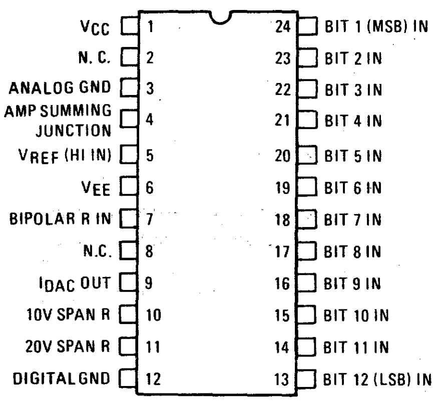
Near zero current in the Analog Ground terminal simplifies use of the HI-5660 by minimizing noise and offsets between the package and the system analog ground. This is accomplished by adding a complement current to the internal ground from an auxiliary R-2R ladder, and then supplying the resultant DC current from the positive power supply.

The Harris HA-1608 +10V precision reference is recommended for use with the HI-5660 in non-multiplying applications.

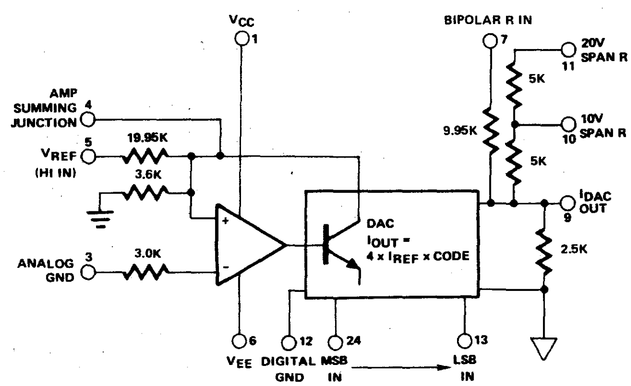
The HI-5660 is offered in two accuracy grades each for the commercial and military temperature ranges. Package is a 24 pin plastic or ceramic DIP, and power requirements are +15V, -15V.

PINOUT

TOP VIEW
24 LEAD DIP



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

V_{CC} to Power Ground	0V to +18V	10V Span R to Reference Ground	±12V
V_{EE} to Power Ground	0V to -18V	20V Span R to Reference Ground	±24V
Voltage on DAC Output (Pin 9)	-3V to +12V	Package Power Dissipation	
Digital Inputs (Pins 13-24) to Power Ground	-1V to +7.0V	Ceramic	1000mW
Ref In to Reference Ground	±12V	Plastic	750mW
Bipolar Offset to Reference Ground	±12V		

**Absolute maximum ratings are limiting values beyond which the serviceability of the circuit may be impaired.*

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = +15V, V_{EE} = -15V, Unless Otherwise Specified)

MODEL	HI-5660-5			HI-5660A-5			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
DATA INPUTS (Note 1) (Pins 13 to 24)							
TTL or 5V CMOS (T_{MIN} to T_{MAX})							
Input Voltage							
Bit ON Logic "1"	2.0		5.5	2.0		5.5	V
Bit OFF Logic "0"	0.0		0.8	0.0		0.8	V
Logic Current (Each Bit)							
Bit ON Logic "1"		2	10		2	10	μA
Bit OFF Logic "0"		-10	-50		-10	-50	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current Unipolar (All Bits On)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (All Bits on or Off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (Exclusive of Span Resistors)	2.0K	2.5K	3.0K	2.0K	2.5K	3.0K	Ω
Offset Unipolar		.01	.05		.01	.05	% of FS
Bipolar (Figure 2, R_3 = 50Ω Fixed)		.05	.15		.05	.15	% of FS
Capacitance		25			25		pF
Compliance Voltage, T_{MIN} to T_{MAX}	-3		+12	-3		+12	V
ACCURACY (Error Relative to Full Scale)							
+25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of FS
T_{MIN} to T_{MAX}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of FS
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{MIN} to T_{MAX}	MONOTONICITY GUARANTEED (±1 LSB MAX)						
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		7	10		7	10	ppm/°C
Differential Nonlinearity		2	6		2	2	ppm/°C
SETTLING TIME TO 1/2 LSB							
With High Z External Load (Note 2)		500			500		ns
With 75Ω External Load		250			250		ns

MODEL	HI-5660-5 MIN	HI-5660-5 TYP	HI-5660-5 MAX	HI-5660A-5 MIN	HI-5660A-5 TYP	HI-5660A-5 MAX	UNITS
TEMPERATURE RANGE							
Operating	0		+75	0		+75	°C
Storage	-25		+150	-25		+150	°C
POWER REQUIREMENTS							
V_{CC}, +4.5V to +16.5V_{DC}		7	12		7	12	mA
V_{EE}, -11.4 to -16.5V_{DC}		-13	-17		-13	-17	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC} = +4.5 to +16.5V_{DC}; V_{EE} = -15V		1	10		1	10	ppm of FS/%
V_{EE} = -11.4 to -16.5V_{DC}; V_{CC} = +15V		1	10		1	10	ppm of FS/%
PROGRAMMABLE OUTPUT RANGES (See Table 1)	0 to +5			0 to +5			V
	-2.5 to +2.5			-2.5 to +2.5			V
	0 to +10			0 to +10			V
	-5 to +5			-5 to +5			V
	-10 to +10			-10 to +10			V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R_2 (Figure 1)		±0.1	±0.25		±0.1	±0.25	% of FS
Bipolar Offset Error with Fixed 50Ω Resistor for R_3 (Figure 2)		±0.05	±0.15		±0.05	±0.1	% of FS
Gain Adjustment Range (Figure 1)	±0.25			±0.25			% of FS
Bipolar Offset Adjustment Range (Fig. 2)	±0.15			±0.15			% of FS
REFERENCE INPUT							
Input Impedance	16K	20K	24K	16K	20K	24K	Ω
POWER DISSIPATION		230	330		230	330	mW
CONTROL AMPLIFIER							
Full Power Bandwidth (+10V to +3V)		200			200		kHz
Small Signal Closed-Loop Bandwidth		2.4			2.4		MHz

MULTIPLYING MODE PERFORMANCE (All Models)

Quadrants	Two (2): Bipolar Operation at Digital Input Only.
Reference Voltage	Unipolar: +10V Max, +2V Min.
Accuracy	10 Bits (±0.05% of Reduced F.S.) for 2V_{DC} Reference Voltage.
Reference Feedthrough (Unipolar Mode, All Bits OFF, and +2V to +10V (p-p), Sinewave Frequency for 1/2 LSB (p-p) Feedthrough)	22kHz Typical
Output Slew Rate 10%-90%	1.3mA/µs
90%-10%	1.3mA/µs
Output Settling Time (All Bits ON and a +2V to +10V Step Change in Reference Voltage)	1.5µs to 0.01% F.S.

NOTES:
1. The Digital Input Levels are Guaranteed but not Tested Over the Temperature Range.
2. See Settling Time Section.

HARRIS

HI-7541

12 Bit Multiplying Monolithic Digital-to-Analog Converter

FEATURES

- FULL FOUR QUADRANT MULTIPLICATION
- .01% RELATIVE ACCURACY OVER TEMPERATURE
- LOW OUTPUT CAPACITANCE 100pF MAX
- TTL/CMOS COMPATIBLE
- MONOLITHIC CONSTRUCTION
- VERY LOW OUTPUT LEAKAGE CURRENT ±100nA MAX
- LOW GAIN ERROR 0.1%

APPLICATIONS

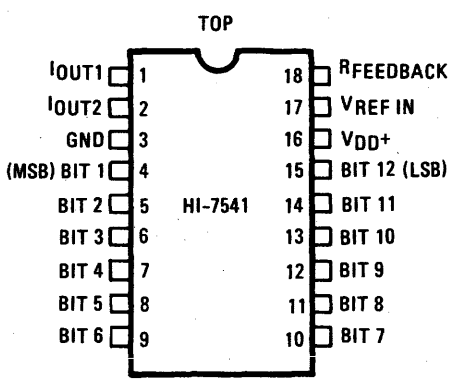
- PROGRAMMABLE GAIN AMPLIFIERS
- PROGRAMMABLE FUNCTION GENERATION

DESCRIPTION

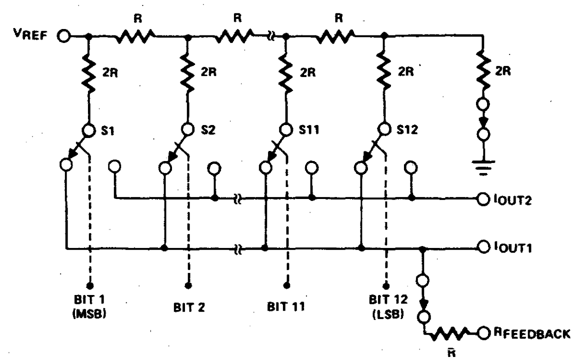
The Harris HI-7541 is a 12-Bit Monolithic Digital to Analog converter, offering full four quadrant multiplying capability. The chip features dielectrically isolated CMOS technology to assure fast settling time and freedom from latch-up. Included are thin film ladder and applications resistors, laser trimmed for accuracy over the full operating temperature range.

The HI-7541 is recommended as a high performance direct replacement for the AD7541 device. It operates on a single +15V supply and is available in an 18-pin ceramic package as well as in dice form. Screening to MIL-STD-883 method 5004 class B is available.

PINOUT



FUNCTIONAL DIAGRAM



DIGITAL INPUTS (DTL, TTL, CMOS COMPATIBLE)
LOGIC: A SWITCH IS CLOSED TO IOUT1 FOR ITS DIGITAL INPUT IN A HIGH (LOGIC 1) STATE.

ABSOLUTE MAXIMUM RATINGS (Referred to Ground)1

Power Supply Inputs V_{DD}	+17V
Reference Inputs VREF (Hi)	±25V
Digital Input Range Bits 1-12	V_{DD} to GND
Output Voltage (Pins 1 and 2)	-400mV to V_{DD}

Power Dissipation (Package) up to +75°C Derate above +75°C by 6mW/°C.	450mW
Operating Temperature Range	
HI-7541SD/TD/SO	-55°C to +125°C
HI-7541AD/BD	-25°C to +85°C
HI-7541JN/KN/JO	0°C to +75°C
HI-7541SD/883 AND TD/883.	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS (@25°C, V_{DD} = +15V, V_{REF} = +10V Unless otherwise noted)

PARAMETER	CONDITIONS	HI-7541KN/BD/TD MIN	HI-7541KN/BD/TD TYP	HI-7541KN/BD/TD MAX	HI-7541JN/AD/SD/JO/SO MIN	HI-7541JN/AD/SD/JO/SO TYP	HI-7541JN/AD/SD/JO/SO MAX	UNITS
INPUT CHARACTERISTICS								
Digital Inputs	Bit ON = "Logic 1" Bit OFF = " Logic 0"							
Input Voltage								
Logic 1, V_{AH}		2.4			2.4			V
Logic 0, V_{AL}				0.8			0.8	V
Input Current								
Logic 1	V_{IN}=15V			1			1	μA
Logic 0	V_{IN}=0V			-1			-1	μA
Reference Input								
Input Resistance		7	9	12	7	9	12	KΩ
Input Voltage		-10		+10	-10		+10	V
TRANSFER CHARACTERISTICS								
Resolution	Over Full Temp. Range	12			12			Bits
Integral (2) Nonlinearity	@+25°C Over Full Temp Range			±.01			±.02	%FSR
Differential (2) Nonlinearity	@ +25°C Over Full Temp Range			±.01			±.02	%FSR
Gain Error (2)	@ +25°C Over Full Temp. Range			±0.1 ±0.15			±0.2 ±0.25	%FSR
Gain Tempco (2)(5)	Over Full Temp. Range			±5			±5	PPM/°C
Settling Time (2) (5) to ±1/2 LSB				1			1	μs
PSRR (2)	14.5V≤V_{DD}≤15.5V;25°C Over Full Temp. Range			±.01 ±.02			±.01 ±.02	%FSR/ %ΔV_{DD}
OUTPUT CHARACTERISTICS								
Output (2) Leakage Current	V_{REF} = ±10V @ +25°C			±50			±50	nA
	Over Full Temp. Range			±100			±100	nA
Capacitance (2) (5)				100			100	pF
Feed Through (2)(5)	V_{REF} = 20 V_{pp} @ 10kHz			±1			±1	mVpp
POWER REQUIREMENTS								
V_{DD}	(See Fig. 6, 8, & 9)	+5	+15	+16	+5	+15	+16	V
I_{DD} (3)				2			2	mA

HARRIS

HA-2420/2425

Fast Sample and Hold

FEATURES

- LOW DROOP RATE (C_H = 1000pF) 5μV/ms
- FAST ACQUISITION TIME (10V STEP TO .01%) 5μs
- HIGH SLEW RATE 7V/μs
- BANDWIDTH 2.5MHz
- LOW EFFECTIVE APERTURE DELAY TIME 30ns
- TTL COMPATIBLE CONTROL INPUT

APPLICATIONS

- A TO D CONVERSION SYSTEMS
- D TO A DEGLITCHER
- AUTO ZERO SYSTEMS
- PEAK DETECTOR
- GATED OP AMP

DESCRIPTION

The HA-2420/2425 is a monolithic circuit consisting of a high performance operational amplifier with its output in series with an ultra-low leakage analog switch and a MOSFET input unity gain amplifier.

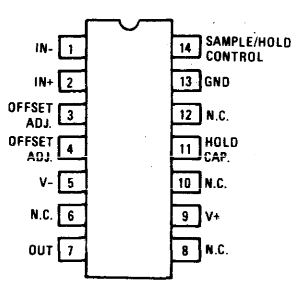
With an external holding capacitor connected to the switch output, a versatile, high performance sample-and-hold or track-and-hold circuit is formed. When the switch is closed, the device behaves as an operational amplifier, and any of the standard op amp feedback networks may be connected around the device to control gain, frequency response, etc. When the switch is opened the output will remain at its last level.

Performance as a sample-and-hold compares very favorably with other monolithic, hybrid, modular, and discrete circuits. Accuracy to better than 0.01% is achievable over the temperature range. Fast acquisition is coupled with superior droop characteristics, even at high temperatures. High slew rate, wide bandwidth, and low acquisition time produce excellent dynamic characteristics. The ability to operate at gains greater than 1 frequently eliminates the need for external scaling amplifiers.

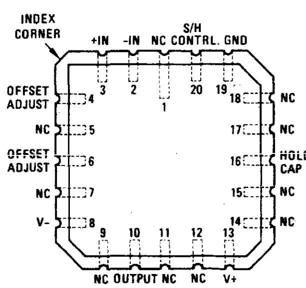
The device may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc.

PINOUT

TOP VIEW

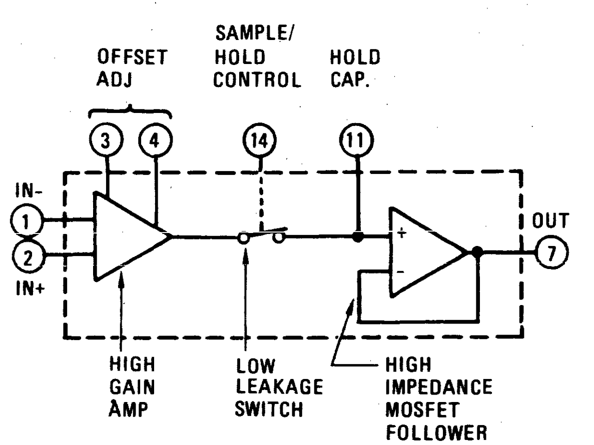


14 PIN DIP



LEADLESS CHIP CARRIER (LCC) PACKAGE

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40V
Differential Input Voltage	±24V
Digital Input Voltage (Pin 14)	+8V, -15V
Output Current	Short Circuit Protected
Internal Power Dissipation	300mW (Note 7)
Operating Temperature Range	
HA-2420-2/8	$-55^{o}C \leqslant T_A \leqslant +125^{o}C$
HA-2425-5	$0^{o}C \leqslant T_A \leqslant +75^{o}C$
Storage Temperature Range	$-65^{o}C \leqslant T_A \leqslant +150^{o}C$

ELECTRICAL CHARACTERISTICS

Test Conditions (Unless otherwise specified) $V_{SUPPLY} = \pm15.0V$; $C_H = 1000pF$; Digital Input (Pin 14), $V_{IL} = +0.8V$ (Sample), $V_{IH} = +2.0V$ (Hold)

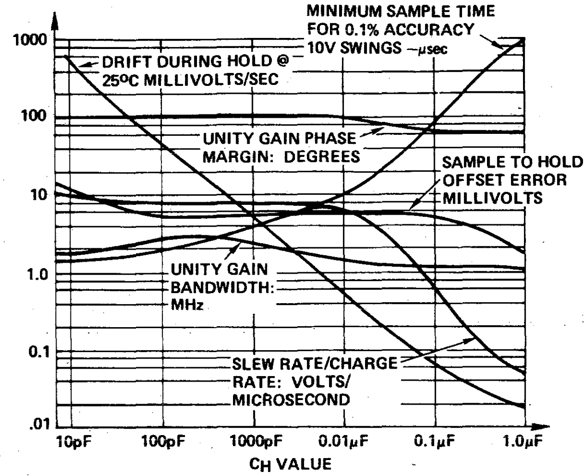
PARAMETER	TEMP	HA-2420-2 MIN	HA-2420-2 TYP	HA-2420-2 MAX	HA-2425-5 MIN	HA-2425-5 TYP	HA-2425-5 MAX	UNITS
INPUT CHARACTERISTICS								
*Offset Voltage	+25°C		2	4		3	6	mV
	Full		3	6		4	8	mV
*Bias Current	+25°C		40	200		40	200	nA
	Full			400			400	nA
*Offset Current	+25°C		10	50		10	50	nA
	Full			100			100	nA
Input Resistance	+25°C	5	10		5	10		MΩ
Common Mode Range	Full	±10			±10			V
TRANSFER CHARACTERISTICS								
*Large Signal Voltage Gain (Note 1, 4)	Full	25K	50K		25K	50K		V/V
*Common Mode Rejection (Note 2)	Full	80	90		74	90		dB
Hold Mode Feedthrough Attenuation (Note 9)	Full		-76			-76		dB
Gain Bandwidth Product (Note 3)	+25°C		2.5			2.5		MHz
OUTPUT CHARACTERISTICS								
*Output Voltage Swing (Note 1)	Full	±10			±10			V
Output Current	+25°C	±15			±15			mA
Full Power Bandwidth (Note 3, 4)	+25°C		100			100		kHz
Output Resistance (D.C.)	+25°C		.15			.15		Ω
TRANSIENT RESPONSE								
Rise Time (Note 3, 5)	+25°C		50	75		50	75	ns
Overshoot (Note 3, 5)	+25°C		25	40		25	40	%
Slew Rate (Note 3, 6)	+25°C	5	7		3	7		V/µs
DIGITAL INPUT CHARACTERISTICS								
Digital Input Current (V_{IN} = 0V)	Full			0.8			0.8	mA
Digital Input Current (V_{IN} = +5.0V)	Full			20			20	µA
Digital Input Voltage (Low)	Full			0.8			0.8	V
Digital Input Voltage (High)	Full	2.0			2.0			V
SAMPLE/HOLD CHARACTERISTICS								
Acquisition Time to .1% 10V Step (Note 3)	+25°C		4			4		µs
Acquisition Time to .01% 10V Step (Note 3)	+25°C		5			5		µs
Aperture time (Note 10)	+25°C		30			30		ns
Effective Aperture Delay Time	+25°C		30			30		ns
Aperture Uncertainty	+25°C		5			5		ns
*Drift Current (Note 3, 8)	+25°C		5	50		5	50	pA
	Full		0.5	4.0		0.5	1.0	nA
*Charge Transfer (Note 8)	+25°C		5	10		5	10	pC
POWER SUPPLY CHARACTERISTICS								
*Supply Current (+)	+25°C		3.5	5.5		3.5	5.5	mA
*Supply Current (-)	+25°C		2.5	3.5		2.5	3.5	mA
*Power Supply Rejection	Full	-80	-90		-74	-90		dB

NOTES:
1. $R_L = 2k\Omega$
2. $V_{CM} = \pm10VDC$
3. $A_V = +1$, $R_L = 2k\Omega$, $C_L = 50pF$
4. V_{OUT} = 20V peak-to-peak
5. V_{OUT} = 200mV peak-to-peak
6. V_{OUT} = 10.0V peak-to-peak
7. Derate Power Dissipation by 4.3mW/°C above +105°C Ambient Temperature
8. V_{IN} = 0V
9. $f_{IN} \leqslant 100kHz$
10. Derived from computer simulation only; not tested.

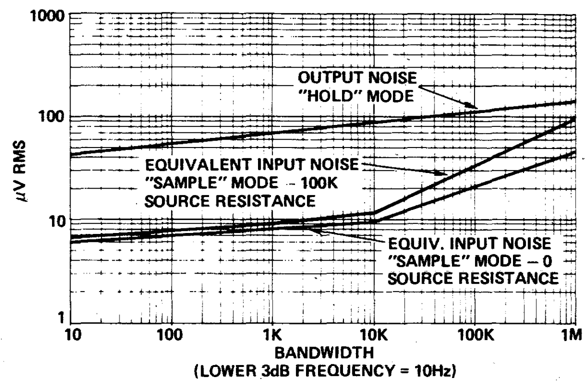
*100% Tested for DASH 8

V_{SUPPLY} = ±15VDC, T_A = +25°C, C_H = 1,000pF Unless Otherwise Specified

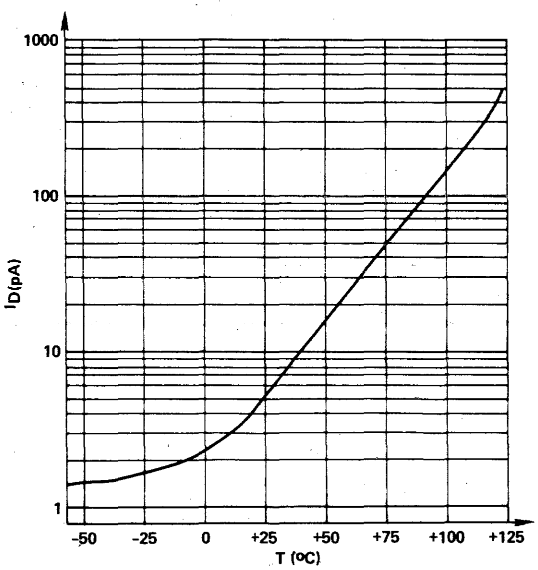
TYPICAL SAMPLE AND HOLD PERFORMANCE AS A FUNCTION OF HOLDING CAPACITOR



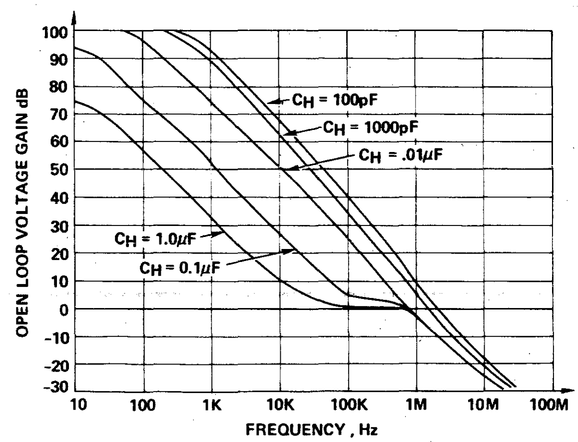
BROADBAND NOISE CHARACTERISTICS



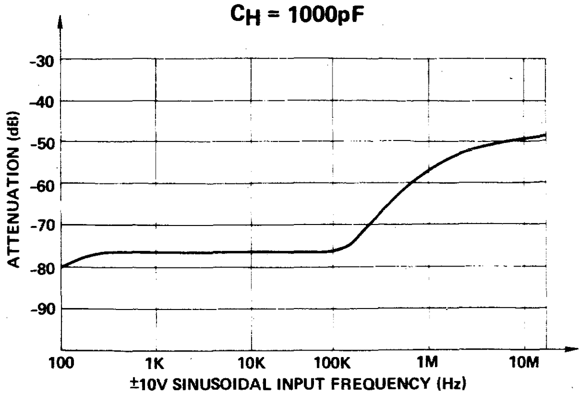
DRIFT CURRENT VS. TEMPERATURE



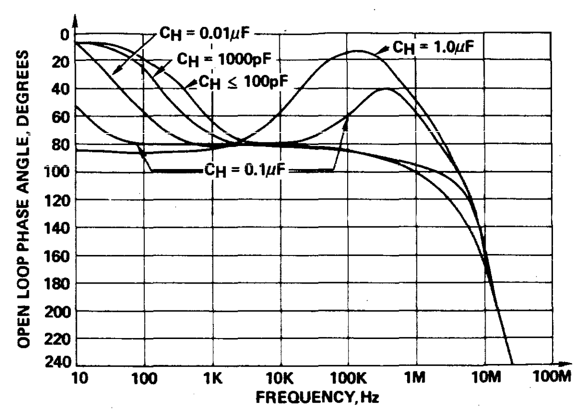
OPEN LOOP FREQUENCY RESPONSE



HOLD MODE FEED THROUGH ATTENUATION C_H = 1000pF



OPEN LOOP PHASE RESPONSE



HARRIS

HA-5320

High Speed Precision Monolithic Sample and Hold Amplifier

FEATURES

• GAIN, dc	2 x 10^6 V/V
• ACQUISITION TIME	1.0 µs (0.01%)
• DROOP RATE	0.08 µV/µs (25°C)
	17 µV/µs (FULL TEMP)
• APERTURE TIME	25ns
• PEDESTAL ERROR	1.0 mV

- INTERNAL HOLD CAPACITOR
- FULLY DIFFERENTIAL INPUT
- TTL COMPATIBLE

APPLICATIONS

- PRECISION DATA ACQUISITION SYSTEMS
- D/A CONVERTER DEGLITCHING
- AUTO-ZERO CIRCUITS
- PEAK DETECTORS

DESCRIPTION

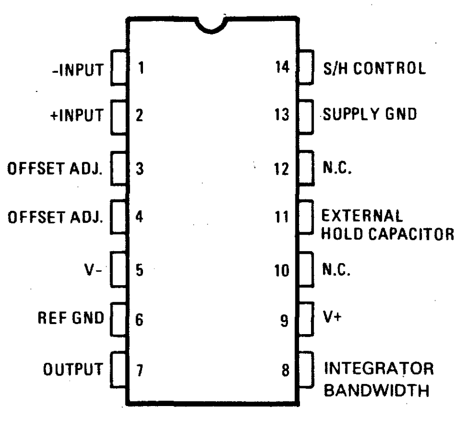
The HA-5320 was designed for use in precision, high speed data acquisition systems.

The circuit consists of an input transconductance amplifier capable of providing large amounts of charging current, a low leakage analog switch, and an output integrating amplifier. The analog switch sees virtual ground as its load; therefore, charge injection on the hold capacitor is constant over the entire input/output voltage range. The pedestal voltage resulting from this charge injection can be adjusted to zero by use of the offset adjust inputs. The device includes a hold capacitor. However, if improved droop rate is required at the expense of acquisition time, additional hold capacitance may be added externally.

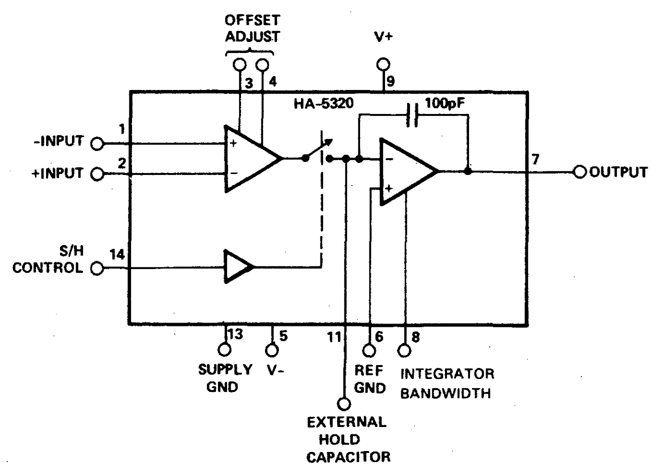
This monolithic device is manufactured using the Harris dielectric isolation process, minimizing stray capacitance and eliminating SCR's. This allows higher speed and latch-free operation. The HA-5320 requires ±15V, and is available in a ceramic or plastic 14-pin DIP.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Voltage between V^+ and V^- terminals	40V
Differential Input Voltage	±24V
Digital Input Voltage (Pin 14)	+8V, −15V
Output Current, continuous	±20mA (Note 1)
Internal Power Dissipation	450mW (Note 2)
Operating Temperature Range	
HA-5320-2/8	−55°C ≤ TA ≤ +125°C
HA-5320-5	0°C ≤ TA ≤ +75°C
Storage Temperature Range	−65°C ≤ TA ≤ +150°C

ELECTRICAL CHARACTERISTICS Test Conditions (unless otherwise specified)

V Supply = ±15V; C_H - Internal; Digital Input (Pin 14), V_{AL} = +0.8V (sample), V_{AH} = +2.0V (hold).

PARAMETER	TEMP	HA-5320-2/8 MIN	HA-5320-2/8 TYP	HA-5320-2/8 MAX	HA-5320-5 MIN	HA-5320-5 TYP	HA-5320-5 MAX	UNITS
INPUT CHARACTERISTICS								
Input Voltage Range	Full	±10			±10			V
Input Resistance	25°C	1	5		1	5		MΩ
Input Capacitance	25°C			3			3	pF
Offset Voltage	25°C		0.2	0.5		0.5	1.0	mV
	Full			2.0			1.5	mV
Bias Current	25°C		70	200		100	300	nA
	Full			200			300	nA
Offset Current	25°C		30	100		30	300	nA
	Full			100			300	nA
Common Mode Range	Full	±10			±10			V
CMRR (Note 3)	25°C	80	90		72	90		dB
Offset Voltage T.C.	Full		5	15		5	20	µV/°C
TRANSFER CHARACTERISTICS								
Gain, dC	25°C	10^6	2×10^6		3×10^5	2×10^6		V/V
Gain Accuracy, Av = +1	25°C		$.5 \times 10^{-4}$			$.5 \times 10^{-4}$		%FSR
Gain Accuracy, T.C.	Full		±.6			±.6		ppm/°C
Gain Bandwidth Product	25°C							
(Note 4, 5) CH = 100pF			2.0			2.0		MHz
CH = 1000pF			.18			.18		MHz
OUTPUT CHARACTERISTICS								
Output Voltage	Full	±10			±10			V
Output Current	25°C	±10			±10			mA
Full Power Bandwidth (Note 4, 6)	25°C		600			600		KHz
Output Resistance (Hold mode)	25°C		1.0			1.0		Ω
Total Output Noise, DC to 10 MHz								
Sample	25°C		125	200		125	200	µV RMS
Hold	25°C		125	200		125	200	µV RMS

SPECIFICATIONS (continued)

PARAMETER	TEMP	HA-5320-2/8 MIN	HA-5320-2/8 TYP	HA-5320-2/8 MAX	HA-5320-5 MIN	HA-5320-5 TYP	HA-5320-5 MAX	UNITS
TRANSIENT RESPONSE								
Rise Time (Note 5)	25°C		100			100		nS
Overshoot (Note 5)	25°C		15			15		%
Slew Rate (Note 7)	25°C		45			45		V/µs
DIGITAL INPUT CHARACTERISTICS								
Input Voltage (High), V_{AH}	Full	2.0			2.0			V
Input Voltage (Low), V_{AL}	Full			0.8			0.8	V
Input Current (V_{AL} = 0V)	Full			4			4	µA
Input Current (V_{AH}= +5V)	Full			0.1			0.1	µA
SAMPLE/HOLD CHARACTERISTICS								
Acquisition Time (.1%) (Note 7)	25°C		.8	1.2		.8		µS
Acquisition Time (.01%) (Note 7)	25°C		1.0			1.0		µS
Aperture Time (Note 8)	25°C		25			25		nS
Effective Aperture Delay Time (See Glossary)	25°C		-25			-25		nS
Aperture Uncertainty	25°C		1			1		nS
Droop Rate	25°C		.08			.08		µV/us
Droop Rate	Full		17			1.2		µV/us
Drift Current (Note 9)	25°C		8			8		pA
Drift Current (Note 9)	Full		1.7			.12		nA
Charge Transfer (Note 9)	25°C		0.1			0.1		pC
Hold Mode Settling Time (.01%)	Full		185			185		nS
Hold Mode Feedthrough 10Vp-p, 100KHz	Full		2			2		mV
POWER SUPPLY CHARACTERISTICS								
Positive Supply Voltage	Full	+14.5	+15	+16	+14.5	+15	+16	V
Negative Supply Voltage	Full	−14.5	−15	−16	-14.5	−15	−16	V
Positive Supply Current (Note 10)	25°C		11	13		11	13	mA
Negative Supply Current (Note 10)	25°C		−11	−13		−11	−13	mA
Power Supply Rejection V^+	Full	80			80			dB
(Note 11) V^-	Full	65			65			dB

NOTES:

1. Internal Power Dissipation may limit Output Current below +20mA.
2. Derate power dissipation by 4.3 mW/°C above 105°C ambient.
3. V_{cm} = +5V DC
4. A_V = +1; R_L = 1KΩ; C_L = 50pF
5. V_O = 200mVpp; R_L = 2KΩ; C_L = 50pF
6. V_O = 20Vpp.
7. V_O = 10V step; R_L = 2KΩ; C_L = 50pF
8. Derived from computer simulation only; not tested.
9. V_{IN} = OV, V_{AH} = +3.5V, t_r < 50ns (V_{AL} to V_{AH}).
10. Specified for a zero differential input voltage between pins 1 and 2. Supply current will increase with differential input (as may occur in the Hold mode) to approximately ±28mA at 20V.
11. Based on a one volt delta in each supply, ie: 15V ± 0.5 VDC.

![HARRIS]

HI-5712/5712A

High Performance 12 Bit Analog to Digital Converter

INTERFACE

Harris Semiconductor

FEATURES

- MICROPROCESSOR COMPATIBLE
- CONVERSION TIME 10μsec MAX OVER TEMP.
- NO MISSING CODES OVER TEMPERATURE
- INTERNAL +10V REFERENCE
- INTERNAL CLOCK WITH EXTERNAL OVERRIDE CAPABILITY
- SERIAL OUTPUT
- TTL/CMOS COMPATIBLE
- TRISTATE PARALLEL OUTPUTS
- 40 PIN DIP
- MIL-STD-883 PROCESSING AVAILABLE

APPLICATIONS

- MULTI-CHANNEL DATA ACQUISITION SYSTEMS
- STATUS MONITORING SYSTEMS
- PROCESS CONTROL SYSTEMS
- INSTRUMENTATION
- HIGH RELIABILITY DAS's

DESCRIPTION

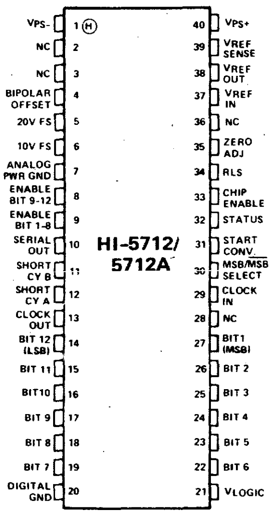
The HI-5712/5712A is a 12-bit successive approximation analog-to-digital converter (ADC) intended for high-speed, high-performance data conversion applications. An 8μs conversion time for an accurate 12 bit conversion with low gain and offset temperature coefficients are among its many features. Numerous functions can be software controlled to meet a variety of ADC requirements.

The highly flexible input design accepts user programmed unipolar and bipolar inputs of: 0 to +10V, 0 to +20V, ±5V and ±10V full scale signal levels. The internal precision +10V reference delivers up to 10mA of output current with ultra high temperature stability. This reference is intended for biasing the ADC reference input, although other configurations can be implemented. A remote sense line is provided for applications requiring usage of the precision reference elsewhere in the system.

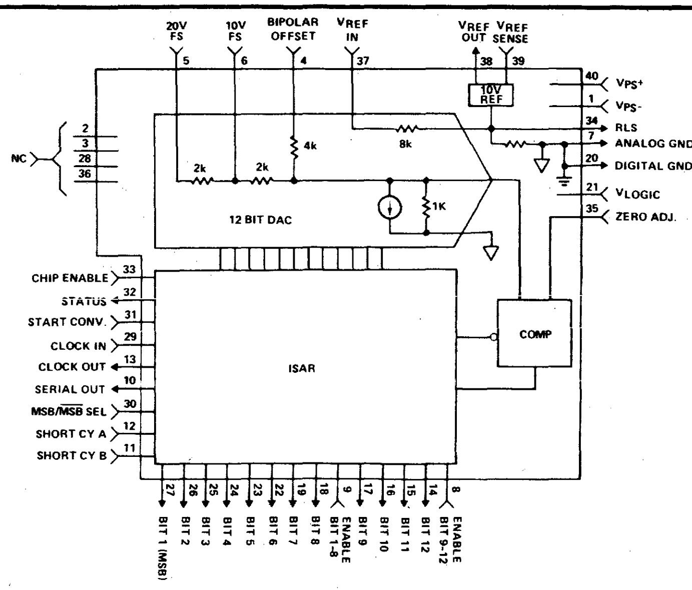
The output code select line and the short cycle control inputs are latched internally for microprocessor compatibility and provide selection of either binary or 2's complement output code, and resolution of 6, 8, 10 or 12 bits, respectively. A flexible interface is provided for 8, 12 and 16 bit systems via the chip select line and the word length control pins. The latter allows independent tri-state enabling of parallel output bits 1-8 and 9-12. A serial data output line is provided for applications requiring remote data transmission.

The HI-5712/5712A is manufactured with hermetically sealed leadless chip carriers (LCC's) mounted to both sides of a multi-layer ceramic substrate which results in a compact 40 pin dual-in-line package. The HI-5712A is intended for military, industrial and instrumentation applications. MIL-STD-883 class B and high reliability commercial grades are both available as standard products.

PINOUT



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Power Supply Inputs	
V_{ps}^+	+20V
V_{ps}^-	-20V
V_{LOGIC}	+10V
V_{REF} IN (Pin 37)	0V, V_{ps}^+
V_{REF} SENSE (Pin 39)	0V, V_{ps}^+
Digital Inputs	-1V, V_{LOGIC}

Power Dissipation (Pd) 2 Watts	
Operating Temperature Range	
HI-5712-2, HI-5712A-2	55°C to +125°C
HI-5712-5, HI-5712A-5	0°C to +75°C
HI-5712-7, HI-5712A-7	0°C to +75°C (Hi Rel)
HI-5712-8, HI-5712A-8	-55°C to +125°C (Hi Rel)
Storage Temperature Range	65°C to +150°C

ELECTRICAL CHARACTERISTICS

(T_A = +25°C, V_{ps} = +15V, V_{ps^-} = -15V, V_{LOGIC} = +5V, V_{REF} In = Internal V_{REF}, Full Scale = +10V, Conversion Speed = 9 μs TYP (Internal Clock), 12-BIT Conversion, Unless otherwise noted.)

PARAMETER		TEMP	HI-5712A-2 HI-5712-2 HI-5712A-8 HI-5712-8 MIN	TYP	MAX	HI-5712A-5 HI-5712-5 HI-5712A-7 HI-5712-7 MIN	TYP	MAX	UNITS
RESOLUTION		Full			12			12	BITS
NONLINEARITY	HI-5712A	+25°C		±1/4	±1/2		±1/4	±1/2	LSB
		Full		±1/4	±1/2		±1/4	±1/2	LSB
	HI-5712	+25°C		±1/4	±1/2		±1/4	±1/2	LSB
		Full		±1/2	±1		±1/2	±1	LSB
DIFFERENTIAL NONLINEARITY	HI-5712A	+25°C		±1/4	±1/2		±1/4	±1/2	LSB
		Full		±1/4	±1/2		±1/4	±1/2	LSB
	HI-5712	+25°C		±1/4	±1/2		±1/4	±1/2	LSB
		Full		±1/2	±1		±1/2	±1	LSB
		NO MISSING CODES GUARANTEED OVER TEMPERATURE							
INHERENT QUANTIZATION ERROR		Full			±1/2			±1/2	LSB
UNIPOLAR OFFSET ERROR (Note 2) (Adjustable to Zero)		+25°C		.3	.6		.3	.6	%FSR
BIPOLAR OFFSET ERROR (Note 2) (Adjustable to Zero)		+25°C		.3	.6		.3	.6	%FSR
GAIN ERROR (note 2) (Adjustable to Zero)		+25°C		.1	.3		.1	.3	%FSR
ADJUSTMENT RANGE									
UNIPOLAR OFFSET		+25°C	±1	±2		±1	±2		%FSR
BIPOLAR OFFSET		+25°C	±1	±2		±1	±2		%FSR
GAIN		+25°C			.3			.3	%FSR
TEMPERATURE STABILITY (With Internal V_{REF})									
UNIPOLAR OFFSET DRIFT	HI-5712A	Full		±2	±5		±2	±5	ppm FSR/°C
	HI-5712	Full		±4	±15		±4	±15	ppm FSR/°C
BIPOLAR OFFSET DRIFT	HI-5712A	Full		±4	±10		±4	±10	ppm FSR/°C
	HI-5712	Full		±8	±25		±8	±25	ppm FSR/°C
GAIN DRIFT	HI-5712A	Full		±5	±10		±5	±10	ppm FSR/°C
	HI-5712	Full		±10	±20		±10	±20	ppm FSR/°C
		NO MISSING CODES GUARANTEED OVER TEMPERATURE							

PARAMETER	TEMP	HI-5712A-2/-8 HI-5712-2/-8 MIN	TYP	MAX	HI-5712A-5/-7 HI-5712-5/-7 MIN	TYP	MAX	UNITS
CONVERSION SPEED (Internal Clock)								
12 BIT	+25°C		9.0	10.0		9.0	10.0	μs
10 BIT	"		6.8	8.5		6.8	8.5	μs
8 BIT	"		5.6	7.0		5.6	7.0	μs
6 BIT	"		4.4	5.4		4.4	5.4	μs
MAXIMUM CONVERSION SPEED AT 12 BITS WITH EXTERNAL CLOCK (Note 3)	Full		6.5			6.5		μs
ANALOG INPUT CHARACTERISTICS								
INPUT VOLTAGE RANGE								
UNIPOLAR	Full	10			10			V
	Full	20			20			V
BIPOLAR	Full	±5	±5		±5	±5		V
	Full	±10	±10		±10	±10		V
INPUT IMPEDANCE								
10V FS (PIN 6)	Full	1.6	2	2.4	1.6	2	2.4	KΩ
20V FS (PIN 5)	Full	3.2	4	4.8	3.2	4	4.8	KΩ
V_{REF} IN (PIN 37)	Full	6.4	8	9.6	6.4	8	9.6	KΩ
ANALOG OUTPUT CHARACTERISTICS								
V_{REF} OUTPUT VOLTAGE	+25°C	9.970	10.000	10.030	9.970	10.000	10.030	V
V_{REF} OUTPUT CURRENT	Full	10			10			mA
VREF OUTPUT TC HI-5712A	Full		±10	±15		±10	±15	ppm FSR/°C
VREF OUTPUT TC HI-5712	Full		±10	±15		±10	±15	ppm FSR/°C
DIGITAL INPUT CHARACTERISTICS								
INPUT VOLTAGE (Note 8)								
LOGIC 1	Full	3.3	2.7		3.3	2.7		V
LOGIC 0	Full		1.2	.8		1.2	.8	V
INPUT CURRENT (Note 8)								
LOGIC 1 (VCC)	Full	-25	0	+25	-25	0	+25	μA
LOGIC 0 (GND)	Full		-200	-400		-200	-400	μA
EXTERNAL CLOCK (Note 3)	Full			2.5			2.5	MHz
DIGITAL OUTPUT CHARACTERISTICS								
OUTPUT VOLTAGE								
LOGIC 1 I_{OH} = -800 A	Full	3.5	4.0		3.5	4.0		V
LOGIC 0 I_{OL} = +3.2mA	Full		.2	.4		.2	.4	V
OUTPUT CURRENT								
LOGIC 1 VO = 3.5V	Full	-800	-1000		-800	-1000		μA
LOGIC 0 VO = .4V	Full	3.2	4.0		3.2	4.0		mA
DIGITAL INPUT TIMING CHARACTERISTICS								
CHIP ENABLE TO START CONVERT t_{cd}	Full	50			50			nsec
START CONVERT PULSE LOW t_{scl}	Full	100			100			nsec
START CONVERT PULSE HIGH t_{sch}	Full	50			50			nsec
CONTROL SETUP TIME t_s	Full	100			100			nsec
CONTROL HOLD TIME t_h	Full	100			100			nsec
CLOCK INPUT LOW t_{pwl}	Full	125			125			nsec
CLOCK INPUT HIGH t_{pwh}	Full	150			150			nsec
CLOCK INPUT PERIOD t_{cl}	Full	400			400			nsec
ENABLE 1-8, 9-12 PULSE WIDTH t_{em}	Full	100			100			nsec

PARAMETER	TEMP	HI-5712A-2/-8 HI-5712-2/-8 MIN	TYP	MAX	HI-5712A-5/-7 HI-5712-5/-7 MIN	TYP	MAX	UNITS
DIGITAL OUTPUT TIMING CHARACTERISTICS (See Figure 6)								
THREE STATE ENABLE DELAY t_{oe}	Full		40	50		40	50	nsec
THREE STATE DISABLE DELAY t_{od}	Full		60	100		60	100	nsec
START CONVERT TO STATUS DELAY t_{sd}	Full		70	100		70	100	nsec
START CONVERT TO CLOCK OUT DELAY t_{scd}			200	500		200	500	nsec
CLOCK TO SERIAL OUT DELAY t_{psd}	Full	100	150	200	100	150	200	nsec
LAST CLOCK TO STATUS DELAY t_{scdt}	Full	50	75	100	50	75	100	nsec
PARALLEL DATA TO STATUS DELAY t_{ds}	Full	50	75		50	75		nsec
LAST SERIAL BIT TO STATUS DELAY t_{da}	Full	50	75		50	75		nsec
CLOCK INPUT TO CLOCK OUT DELAY t_{dcl}	Full		25	50		25	50	nsec
PARALLEL DATA OUTPUT CODES								
UNIPOLAR (Note 4)	Positive True Binary							
BIPOLAR (Note 4)	Positive True Offset Binary							
	Positive True Two's Complement Binary							
SERIAL DATA OUTPUT CODE	Positive True NRZ Code							
POWER SUPPLY REQUIREMENTS (Note 5)								
V_{ps+}	Full	+13.5	+15	+16.5	+13.5	+15	+16.5	V
V_{ps-}	Full	-13.5	-15	-16.5	-13.5	-15	-16.5	V
V_{LOGIC}	Full	+4.5	+5	+5.5	+4.75	+5	+5.25	V
I_{ps+}	Full		27	35		27	35	mA
I_{ps-}	Full		42	50		42	50	mA
I_{LOGIC}	Full		4.5	15		4.5	15	mA
POWER SUPPLY SENSITIVITY (Note 6)								
V_{ps+} = +13.5V to +16.5V, V_{ps-} = -15V, V_{LOGIC} = +5V								
UNIPOLAR OFFSET			2	5		2	5	ppm of FSR / %ΔP.S.
BIPOLAR OFFSET			2	4		2	4	ppm of FSR / %ΔP.S.
GAIN			1	3		1	3	ppm of FSR / %ΔP.S.
V_{ps-} = -13.5V to -16.5V, V_{ps+} = +15V, V_{LOGIC} = +5V								
UNIPOLAR OFFSET			2	5		2	5	
BIPOLAR OFFSET			2	4		2	4	
GAIN			1	3		1	3	
V_{LOGIC} = +4.5V to +5.5V, V_{ps+} = +15V, V_{ps-} = -15V CONVERSION SPEED (12 Bit with Internal Clock)			±5	±10		±5	±10	%

NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. See Fiqure 2 for connections. The initial errors are adjustable to zero by using external trim potentiometers as shown in Figure 3, and 4.
3. The HI-5712A will operate at these speeds (for 12 bit conversion), but parametric performance is not guaranteed.
4. See operating instructions for details.
5. After 60 seconds warm-up.
6. See definitions.
7. These terminals will be used in the future for additional functions. Do not make connections to these pins in your system.
8. TTL compatibility guaranteed.

PIN FUNCTIONS AND DESCRIPTIONS

PIN	SYMBOL	DESCRIPTION
1	V_{PS}-	-15V Power Supply Terminal
2	NC	No Connection See Note 7
3	NC	No Connection See Note 7
4	BIPOLAR OFFSET	Connect to V_{REF} for Bipolar Input Mode. See Operating Instructions for Details.
5	20V FS	20V Full Scale Analog Input
6	10V FS	10V Full Scale Analog Input
7	ANALOG GND	Analog Power Supply Return
8	ENABLE BIT 9-12	Output "Three State" Control. An Input "0" Enables Bits 9 through 12, whereas a "1" Switches these Bits to a High Impedance State.
9	ENABLE BIT 1-8	Output "Three State" Control. An Input "0" Enables Bits 1 through 8, whereas a "1" Switches these Bits to a High Impedance State.
10	SERIAL OUT	NRZ Serial Data Output. To be used in Conjunction with Clock Out for Remote Data Transmission
11	SHORT CY B	See Description for Pin 12
12	SHORT CY A	Digital Inputs Applied to short cycle A and B selects a conversion of 6, 8, 10, or 12-bits:

BITS	SHORT CY A	SHORT CY B
6	0	0
8	0	1
10	1	0
12	1	1

PIN	SYMBOL	DESCRIPTION
13	CLOCK OUT	SAR Clock Output. Used for Decoding Serial Out Data
14	BIT 12	Output Data Bit (LSB)
15	BIT 11	Output Data Bit
16	BIT 10	Output Data Bit
17	BIT 9	Output Data Bit
18	BIT 8	Output Data Bit
19	BIT 7	Output Data Bit
20	DIGITAL GND	Digital Power Supply Return
21	V_{LOGIC}	+5V Power Supply Terminal
22	BIT 6	Output Data Bit
23	BIT 5	Output Data Bit
24	BIT 4	Output Data Bit
25	BIT 3	Output Data Bit
26	BIT 2	Output Data Bit
27	BIT 1	Output Data Bit (MSB)
28	NC	No Connection. See Note 7.
29	CLOCK IN	An External Clock Signal Applied to this Input Overrides the Internal Clock.
30	MSB/$\overline{MSB}$ SEL	Digital Input Pin. A "1" Applied to this Terminal Selects a Straight Binary or Offset Binary Output Code. A "0" Inverts the MSB to Yield a 2's Complement Binary Output Code.
31	START CONV	Digital Input Pin. A High to Low Transition Initiates the ADC Conversion Cycle.
32	STATUS	Digital Output Pin. A "1" Indicates that the ADC is Busy, While a "0" Denotes that Conversion is Completed and Data is Ready for Retrieval.

PIN	SYMBOL	DESCRIPTION
33	CHIP ENABLE	Digital Input Pin. A "1" Forces the Output Data, Serial Out and Status Terminals to a High Impedance State and the ADC is Disabled. A "0" Enables these ADC Functions.
34	RLS	Reference Low Sense.
35	ZERO ADJ	External Zero Adjustment Pin, See Operating Instructions for Details.

PIN	SYMBOL	DESCRIPTION
36	NC	No Connection. See Note 7.
37	V_{REF} IN	+10V Reference Input to ADC.
38	V_{REF} OUT	Internal +10V Reference Output, Normally Connected to V_{REF} IN (Pin 37).
39	V_{REF} SENSE	Internal +10V Reference Sensing Terminal, Normally connected to V_{REF} Out (Pin 38). See Operating Instructions for Details.
40	V_{ps+}	+15V Power Supply Terminal.

APPLYING THE HI-5712/5712A

OPERATING INSTRUCTIONS

Conventional ADC systems provide maximum performance when the analog and digital ground lines are tied together at the ADC terminals. This minimizes analog interference due to digital switching noise. For optimum performance, this external grounding procedure should be followed in HI-5712/5712A installations to reinforce the unit's internal analog-to-digital ground connections. Under no circumstances should the Reference Low Sense (RLS) terminal (Pin 34) be connected to system ground.

In practice, the Reference Low Sense (RLS) terminal (Pin 34) normally is connected to zero adjust (or error amplifier) input terminal (Pin 35), either directly or through an appropriate resistor network. See figures 3 and 4.

On the HI-5712/5712A substrate, the power supply lines to each active component are bypassed to ground with 0.01 μF chip capacitors for high frequency noise rejection. For best accuracy, the grounding and decoupling schemes shown in Figures 3 and 4 are recommended. The 10μF bypass capacitors shown should be connected as close as possible to the HI-5712/5712A, preferably at the device pin.

For applications where usage of potentiometers is highly undesirable, the trim pots shown in Figures 3 and 4 can either be deleted or replaced by precision fixed resistors. (Delete R_3 and R_4; replace R_1 with 25 ohms). When precision fixed resistors are used, the initial offset error and gain error contributions are as specified in page 2.

NOTE: The HI-5712/5712A may latch up if the device is enabled before applying power. Disabling the device following power turn on will remedy this situation. Care supplies do not excessively overshoot their final value during turn on.

CONTROL AND INTERFACE

The HI-5712/5712A features a versatile set of controlling functions which allows a wide variety of applications, including microprocessor bus interfacing.

When the chip enable is set to low, the internal registers are enabled, and the output data lines can be enabled via the output enable control lines. The conversion cycle is initiated at the falling edge of the start conversion pulse. At this time, the MSB/$\overline{\text{MSB}}$ Select, Short Cycle A, and Short Cycle B control information is latched into the internal registers. The status line is also forced into an active high state indicating that a conversion is taking place. At the end of the conversion cycle the status line will be set to low to signify that the data is ready at the tri-state buffers. The various timing relationships are shown in Figure 1.

There are two distinct modes of operation, namely, continuous conversion and single step conversion. Continuous conversion can be easily achieved by connecting the Status line to the Start Convert pin. In this application, an indecision state may occur during the initial power-on conditions. Normal operation is restored by pulsing the chip enable pin to logic high for a period greater than 100 ns.

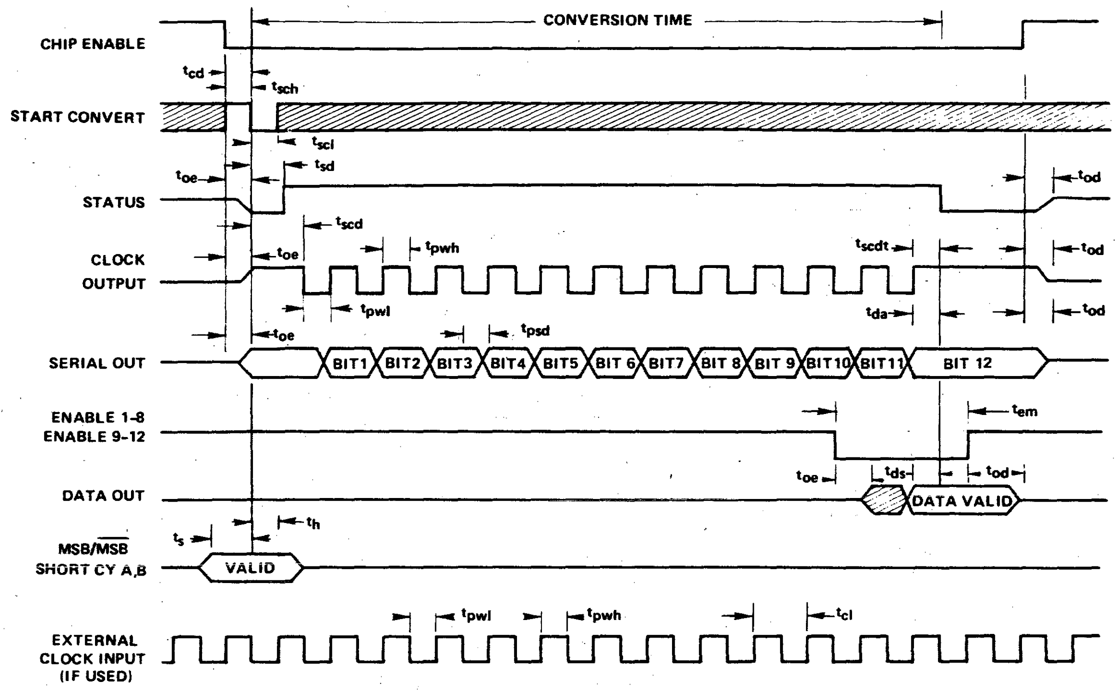


FIGURE 1. HI-5712/5712A TIMING DIAGRAM

REMOTE DATA TRANSMISSION

The Serial Data Out is mainly used for remote data transmission, where only a limited number of wires are available.

Serial Output is bit by bit (MSB first, LSB last) in a NRZ (nonreturn-to-zero) format. It changes state only at the positive going edges of the Clock Out, and remains valid during the whole clock period. Parallel data can be constructed by clocking the serial data into a receiving shift register.

In order to minimize transmission error, the negative-going edge of the clock should be used to clock data into the remote shift register. The parallel data will be valid once the status line returns to low. The clocking scheme is shown in Figure 1.

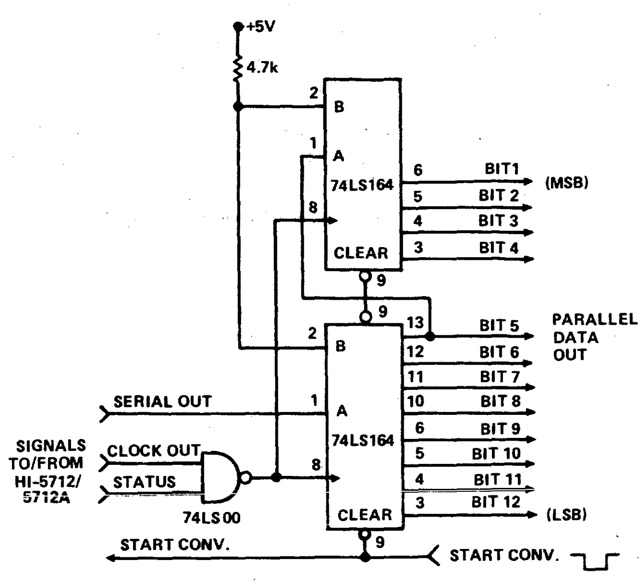


FIGURE 2. DECODING SERIAL DATA OUT

HI-5712/5712A CALIBRATION CHART

OPERATING MODE	ANALOG INPUT CONNECTION	R2 BIAS RESISTOR	MSB/$\overline{MSB}$ SELECT PIN 30	OFFSET ADJUST ANALOG INPUT VOLTAGE	ADJUST R3 FOR DITHER BETWEEN CODES	GAIN ADJUST ANALOG INPUT VOLTAGE	ADJUST R1 FOR DITHER BETWEEN CODES	LSB WEIGHT
UNIPOLAR STRAIGHT BINARY 0V to +10V	10VFS PIN 6	667Ω	HIGH	+1.22mV	0000 0000 0000 0000 0000 0001	+9.9963V	1111 1111 1110 1111 1111 1111	2.44mV
UNIPOLAR STRAIGHT BINARY 0V to +20V	20VFS PIN 5	800Ω	HIGH	+2.44mV	0000 0000 0000 0000 0000 0001	+19.9927V	1111 1111 1110 1111 1111 1111	4.88mV
BIPOLAR OFFSET BINARY -5V to +5V	10VFS PIN 6	580Ω	HIGH	-4.9988V	0000 0000 0000 0000 0000 0001	+4.9963V	1111 1111 1110 0111 1111 1111	2.44mV
BIPOLAR OFFSET BINARY -10V to +10V	20V FS PIN 5	667Ω	HIGH	-9.9976V	0000 0000 0000 0000 0000 0001	+9.9927V	1111 1111 1110 1111 1111 1111	4.88mV
BIPOLAR 2's COMPLEMENT -5V to +5V	10V FS PIN 5	580Ω	LOW	-4.9988V	1000 0000 0000 1000 0000 0001	+4.9963V	0111 1111 1110 0111 1111 1111	2.44mV
BIPOLAR 2's COMPLEMENT 10V to +10V	20V FS PIN 6	667Ω	LOW	-9.9976V	1000 0000 0000 1000 0000 0001	+9.9927V	0111 1111 1110 0111 1111 1111	4.88mV

CALIBRATION PROCEDURE- Refer to Calibration Chart and to Figures 3 and 4 for appropriate analog input connections, value of bias resistor, and MSB/$\overline{MSB}$ select.

STEP 1 OFFSET ADJUSTMENT

- Set analog input to the appropriate value for offset adjustment.
- Adjust R3 for dither between codes shown in calibration chart.

STEP 2 GAIN ADJUSTMENT

- Set analog input to the appropriate value for gain adjustment.
- Adjust R1 for dither between codes shown in calibration chart.

NOTE: This calibration procedure insures that the transfer characteristic produced by connecting the midpoints of all quantization intervals passes through the origin.

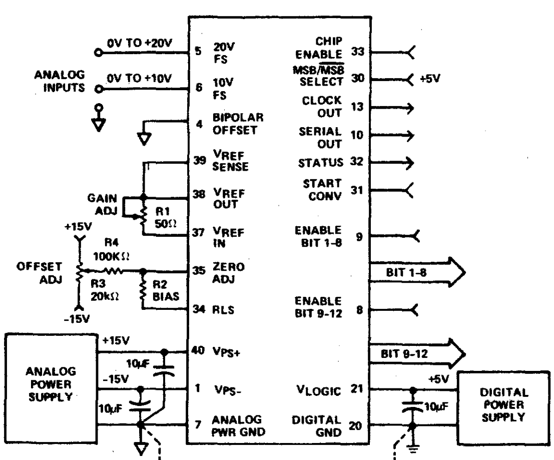


FIGURE 3. UNIPOLAR INPUT CONNECTIONS - STRAIGHT BINARY OUTPUT CODE

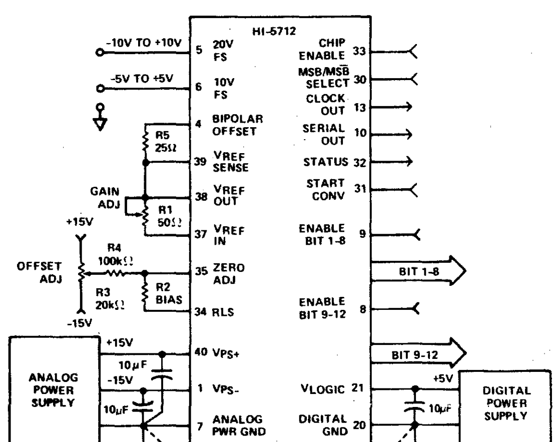


FIGURE 4. BIPOLAR INPUT CONNECTIONS

HARRIS

HI-574A

Fast, Complete 12-Bit A/D Converter with Microprocessor Interface

FEATURES

- COMPLETE 12 BIT A/D CONVERTER WITH REFERENCE AND CLOCK.
- FULL 8-, 12- or 16- BIT MICROPROCESSOR BUS INTERFACE.
- 150 nS BUS ACCESS TIME
- NO MISSING CODES OVER TEMPERATURE
- MINIMAL SETUP TIME FOR CONTROL SIGNALS
- 25 μS MAXIMUM CONVERSION TIME
- LOW NOISE, VIA CURRENT-MODE SIGNAL TRANSMISSION BETWEEN CHIPS
- BYTE ENABLE/SHORT CYCLE (A_0 INPUT)
  - GUARANTEES BREAK – BEFORE – MAKE ACTION, ELIMINATING BUS CONTENTION DURING READ OPERATION. LATCHED BY THE START CONVERT INPUT (TO SET THE CONVERSION LENGTH).
- IMPROVED SECOND SOURCE FOR AD574A AND HS574
- ±12V TO ±15V OPERATION

APPLICATIONS

- MILITARY AND INDUSTRIAL DATA ACQUISITION SYSTEMS
- ELECTRONIC TEST AND SCIENTIFIC INSTRUMENTATION.
- PROCESS CONTROL SYSTEMS.

DESCRIPTION

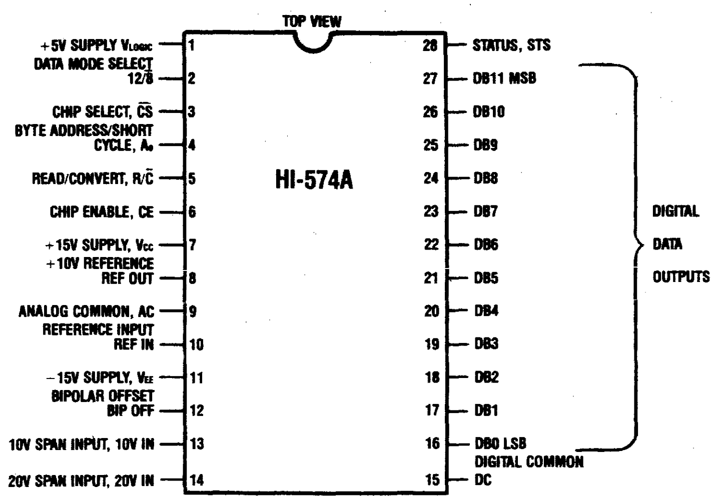
The HI-574A is a complete 12 bit Analog-to-Digital Converter, including a +10V reference, clock, three-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice housed in a 28-pin package. The bipolar analog die features the Harris Dielectric Isolation process, which provides enhanced AC performance and freedom from latch-up.

Custom design of each IC (bipolar analog and CMOS digital) has yielded improved performance over existing versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1 LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital IC's. Also, the clock oscillator is current-controlled for excellent stability over temperature. The oscillator is trimmed for a nominal conversion time of 20 ± 1 μs.

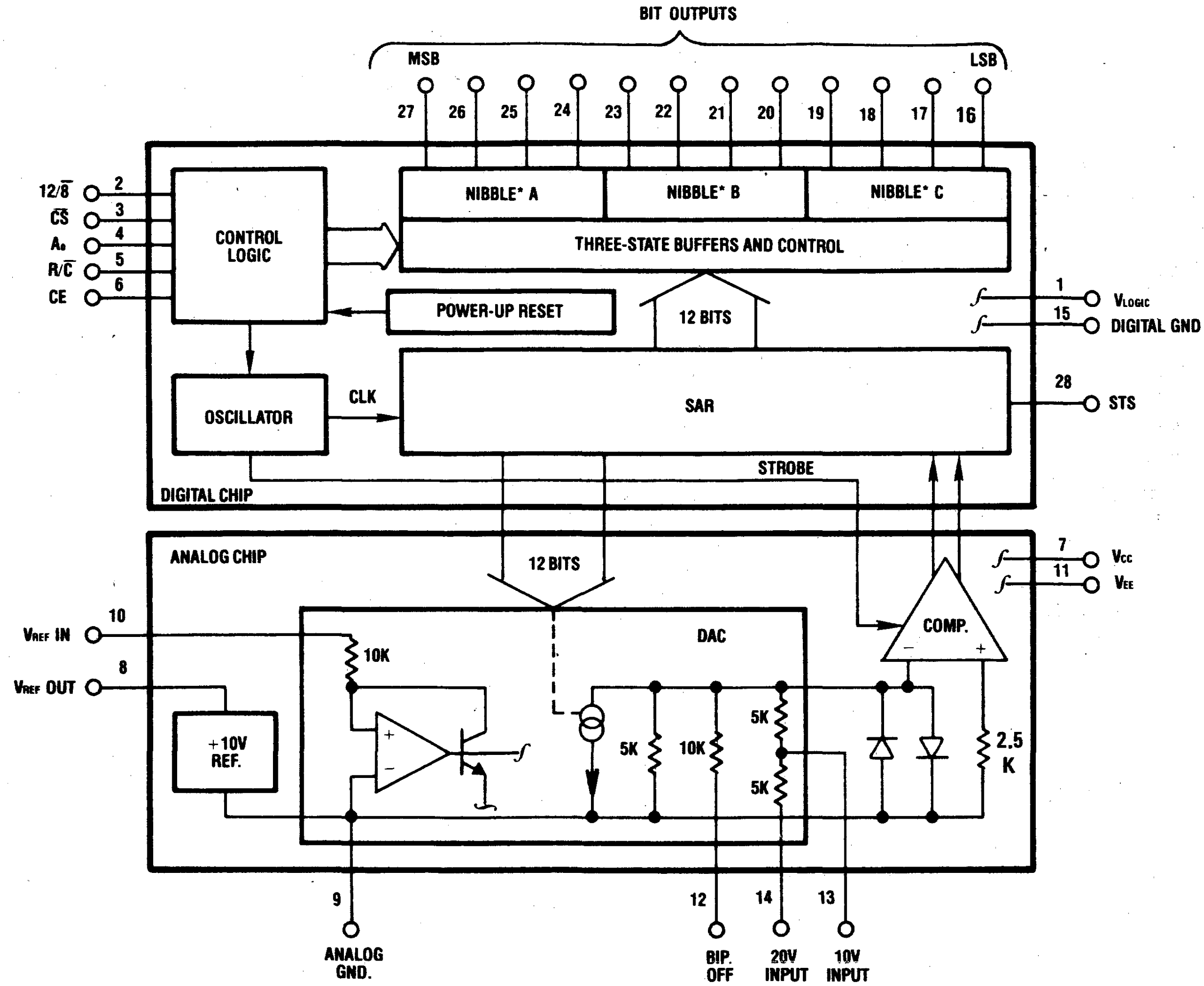
The HI-574A offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity, gain and offset accuracy. The buried zener reference circuit is trimmed for minimum temperature coefficient.

Power requirements are +5V and ±12V to ±15V, with typical dissipation of 515 mW. Three electrical grades each are offered for the commercial and military temperature ranges. All models are packaged in a 28 pin side-brazed, ceramic DIP. In addition, parts are available with screening per MIL-STD-883 Method 5004, Class B.

PINOUT



CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.



*("NIBBLE" IS A 4 BIT DIGITAL WORD.)

HI-574A BLOCK DIAGRAM

(Typical @ +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise specified)

DC AND TRANSFER ACCURACY SPECIFICATIONS

MODEL	HI-574AJ	HI-574AK	HI-574AL	UNITS
Temperature Range	0 TO +75			°C
Resolution (max)	12	12	12	Bits
Linearity Error 25°C (max) 0°C to +75°C (max)	 ±1 ±1	 ±1/2 ±1/2	 ±1/2 ±1/2	 LSB LSB
Differential Linearity Error (Maximum resolution for which no missing codes is guaranteed) 25°C T_{min} to T_{max}	 11 11	 12 12	 12 12	 Bits Bits
Unipolar Offset (max) (Adjustable to zero)	 ±2	 ±2	 ±2	 LSB
Bipolar Offset (max) (Adjustable to zero)	 ±10	 ±4	 ±4	 LSB
Full Scale Calibration Error 25°C (max), with fixed 50 Ω resistor from REF OUT to REF IN (Adjustable to zero) T_{min} to T_{max} (No adjustment at +25°C) (With adjustment to zero at +25°C)	 0.3 0.5 0.22	 0.3 0.4 0.12	 0.3 0.35 0.05	 % of F.S. % of F.S. % of F.S.
Temperature Coefficients Guaranteed max change, T_{min} to T_{max} (Using internal reference) Unipolar Offset Bipolar Offset Full Scale Calibration	 ±2 (10) ±2 (10) ±9 (45)	 ±1 (5) ±1 (5) ±5 (25)	 ±1 (5) ±1 (5) ±2 (10)	 LSB (ppm/°C) LSB (ppm/°C) LSB (ppm/°C)
Power Supply Rejection Max change in Full Scale Calibration +13.5V<V_{CC}<+16.5V or +11.4V<V_{CC}<+12.6V +4.5V<V_{LOGIC}<+5.5V −16.5V<V_{EE}<−13.5V or −12.6V<V_{EE}<−11.4V	 ±2 ±1/2 ±2	 ±1 ±1/2 ±1	 ±1 ±1/2 ±1	 LSB LSB LSB
Analog Inputs Input Ranges Bipolar Unipolar Input Impedance 10 Volt Span 20 Volt Span	 −5 to +5 −10 to +10 0 to +10 0 to +20 5K, ± 25% 10K, ± 25%			 Volts Volts Volts Volts Ohms Ohms
Power Supplies Operating Voltage Range V_{LOGIC} V_{CC} V_{EE} Operating Current I_{LOGIC} I_{CC} I_{EE}	 +4.5 to +5.5 +11.4 to +16.5 −11.4 to −16.5 7 TYP, 15 MAX 11 TYP, 15 MAX 21 TYP, 28 MAX			 Volts Volts Volts mA mA mA
Power Dissipation	515 TYP, 720 MAX			mW
Internal Reference Voltage Output current,[1] available for external loads (External load should not change during conversion).	+10.00 ± 0.1 MAX 2.0 MAX			Volts mA

1 When supplying an external load and operating on ±12V supplies, a buffer amplifier must be provided for the Reference Output.

(Typical @ +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise specified)

DC AND TRANSFER ACCURACY SPECIFICATIONS

MODEL (Applicable to /883B versions also)	HI-574AS	HI-574AT	HI-574AU	UNITS
Temperature Range	−55 TO +125			°C
Resolution (max)	12	12	12	Bits
Linearity Error				
25°C (max)	±1	±1/2	±1/2	LSB
−55°C to +125°C (max)	±1	±1	±1	LSB
Differential Linearity Error (Maximum resolution for which no missing codes is guaranteed)				
25°C	11	12	12	Bits
T_{min} to T_{max}	11	12	12	Bits
Unipolar Offset (max) (Adjustable to zero)	±2	±2	±2	LSB
Bipolar Offset (max) (Adjustable to zero)	±10	±4	±4	LSB
Full Scale Calibration Error				
25°C (max), with fixed 50 Ω resistor from REF OUT to REF IN (Adjustable to zero)	0.3	0.3	0.3	% of F.S.
T_{min} to T_{max}				
(No adjustment at +25°C)	0.8	0.6	0.4	% of F.S.
(With adjustment to zero at +25°C)	0.5	0.25	0.12	% of F.S.
Temperature Coefficients				
Guaranteed max change, T_{min} to T_{max} (Using internal reference)				
Unipolar Offset	±2	±1	±1	LSB
	(5)	(2.5)	(2.5)	(ppm/°C)
Bipolar Offset	±4	±2	±1	LSB
	(10)	(5)	(2.5)	(ppm/°C)
Full Scale Calibration	±20	±10	±5	LSB
	(50)	(25)	(12.5)	(ppm/°C)
Power Supply Rejection				
Max change in Full Scale Calibration				
$+13.5V<V_{CC}<+16.5V$ or $+11.4V<V_{CC}<+12.6V$	±2	±1	±1	LSB
$+4.5V<V_{LOGIC}<+5.5V$	±1/2	±1/2	±1/2	LSB
$-16.5V<V_{EE}<-13.5V$ or $-12.6V<V_{EE}<-11.4V$	±2	±1	±1	LSB
Analog Inputs				
Input Ranges				
Bipolar	−5 to +5			Volts
	−10 to +10			Volts
Unipolar	0 to +10			Volts
	0 to +20			Volts
Input Impedance				
10 Volt Span	5K Ω, ± 25%			Ohms
20 Volt Span	10K Ω, ± 25%			Ohms
Power Supplies				
Operating Voltage Range				
V_{LOGIC}	+4.5 to +5.5			Volts
V_{CC}	+11.4 to +16.5			Volts
V_{EE}	−11.4 to −16.5			Volts
Operating Current				
I_{LOGIC}	7 TYP, 15 MAX			mA
I_{CC}	11 TYP, 15 MAX			mA
I_{EE}	21 TYP, 28 MAX			mA
Power Dissipation	515 TYP, 720 MAX			mW
Internal Reference Voltage	+10.00 ± 0.1 (MAX)			Volts
Output current,[1] available for external loads (External load should not change during conversion).	2.0 MAX			mA

1 When supplying an external load and operating on ±12V supplies, a buffer amplifier must be provided for the Reference Output.

DIGITAL CHARACTERISTICS[1]
(ALL MODELS, OVER FULL TEMP. RANGE)

	MIN	TYP	MAX
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, A0, 12/$\overline{8}$)			
Logic "1"	+2.4V[2]		+5.5V
Logic "0"	−0.5V		+0.8V
Current	−5μA	0.1μA	+5μA
Capacitance		5pF	
Logic Outputs (DB11-DB0, STS)			
Logic "0" (I_{SINK} — 1.6mA)			+0.4V
Logic "1" (I_{SOURCE} — 500μA)	+2.4V		
Leakage (High - Z State, DB11-DB0 ONLY)	−5μA	0.1μA	+5μA
Capacitance		5pF	

[1] *See "HI-574A Timing Specifications" for a detailed listing of digital timing parameters.*
[2] *Although this guaranteed threshold is higher than standard TTL (+2.0V), bus loading is much less, i.e.,typical input current is only 0.25% of a TTL load.*

ABSOLUTE MAXIMUM RATINGS
(Specifications apply to all grades, except where noted)

V_{CC} to Digital Common .... 0 to +16.5V
V_{EE} to Digital Common .... 0 to −16.5V
V_{LOGIC} to Digital Common .... 0 to +7V
Analog Common to Digital Common .... ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to Digital Common .... −0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$) to Analog Common .... ±16.5V
$20V_{IN}$ to Analog Common .... ±24V
REF OUT .... Indefinite short to common
Momentary short to V_{CC}
Chip Temperature (J, K, L grades) .... 100°C
(S, T, U grades) .... 150°C
Power Dissipation 1000mW
Lead Temperature, Soldering .... 300°C, 10 sec.
Storage Temperature .... −65°C to +150°C
Thermal Resistance, Θ_{JA} .... 60°C/W

HI-574A ORDERING GUIDE

MODEL	TEMP. RANGE	LINEARITY ERROR MAX (T_{MIN} to T_{MAX})	RESOLUTION (NO MISSING CODES, T_{MIN} to T_{MAX})	FULL SCALE TC (PPM/°C MAX)
HI1-574AJD	0 to 75°C	±1 LSB	11 Bits	50.0
HI1-574AKD	0 to 75°C	±1/2 LSB	12 Bits	27.0
HI1-574ALD	0 to 75°C	±1/2 LSB	12 Bits	10.0
HI1-574ASD	−55 to +125°C	±1 LSB	11 Bits	50.0
HI1-574ASD/883B	−55 to +125°C	±1 LSB	11 Bits	50.0
HI1-574ATD	−55 to +125°C	±1 LSB	12 Bits	25.0
HI1-574ATD/883B	−55 to +125°C	±1 LSB	12 Bits	25.0
HI1-574AUD	−55 to +125°C	±1 LSB	12 Bits	12.5
HI1-574AUD/883B	−55 to +125°C	±1 LSB	12 Bits	12.5

DEFINITIONS OF SPECIFICATIONS

LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs ½LSB (1.22mV for 10 volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1½LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HI-574AK, AL, AT, and AU grades are guaranteed for maximum nonlinearity of ±½LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HI-574AJ and AS grades are guaranteed to ±1LSB max error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR
(NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HI-574AK, AL, AT, and AU grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HI-574AJ and AS grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

UNIPOLAR OFFSET

The first transition should occur at a level ½LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

BIPOLAR OFFSET

Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value ½LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

FULL SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1½LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figure 5. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 volt reference.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{min} or T_{max}.

POWER SUPPLY REJECTION

The standard specifications for the HI-574A assume use of +5.00 and ±15.00 or ±12.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

CODE WIDTH

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10 volts for a 12-bit ADC.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±½LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

LEFT-JUSTIFIED DATA

The data format used in the HI-574A is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

APPLYING THE HI-574A

For each application of this converter, the ground connections, power supply bypassing, analog signal source, digital timing and signal routing on the circuit board must be optimized to assure maximum performance. These areas are reviewed in the following sections, along with basic operating modes and calibration requirements.

PHYSICAL MOUNTING AND LAYOUT CONSIDERATIONS

Layout –

Unwanted, parasitic circuit components, (L, R, and C) can make 12 bit accuracy impossible, even with a perfect A/D converter. The best policy is to eliminate or minimize these parasitics through proper circuit layout, rather than try to quantify their effects.

The recommended construction is a double-sided printed circuit board with a ground plane on the component side. Other techniques, such as wire-wrapping or point-to-point wiring on vectorboard, will have an unpredictable effect on accuracy.

In general, sensitive analog signals should be routed between ground traces and kept well away from digital lines. If analog and digital lines must cross, they should do so at right angles.

Power Supplies

Supply voltages to the HI-574A (+15V, −15V and +5V) must be "quiet" and well regulated. Voltage spikes on these lines can affect the converter's accuracy, causing several LSB's to flicker when a constant input is applied. Digital noise and spikes from a switching power supply are especially troublesome. If switching supplies must be used, outputs should be carefully filtered to assure "quiet" DC voltage at the converter terminals.

Further, a bypass capacitor pair on each supply voltage terminal is necessary to counter the effect of variations in supply current. Connect one pair from pin 1 to 15 (V_{LOGIC} supply), one from pin 7 to 9 (V_{CC} to Analog Common) and one from pin 11 to 9 (V_{EE} to Analog Common). For each capacitor pair, a 10μF tantalum type in parallel with a 0.1μF ceramic type is recommended.

Ground Connections

The typical HI-574A ground currents are 5.5mADC into pin 9 (Analog Ground) and 7mADC out of pin 15 (Digital Common). These pins should be tied together at the package to guarantee specified performance for the converter. In addition, a wide PC trace should run directly from pin 9 to (usually) 15V common, and from pin 15 to (usually) the +5V Logic Common. If the converter is located some distance from the system's "single point" ground, make only these connections to pins 9 and 15: Tie them together at the package, and back to the system ground with a single path. This path should have low resistance since it will carry about 1.5mA of DC current. (Code dependent currents flow in the V_{CC}, V_{EE} and V_{LOGIC} terminals, but not through the HI-574A's Analog Common or Digital Common).

HARRIS

HI-5900

Analog Data Acquisition Signal Processor

FEATURES

- INPUT OVERVOLTAGE PROTECTION
- 50kHz THROUGHPUT
- 12-BIT ACCURACY
- OUTPUT TRACK/HOLD AMPLIFIER
- ZERO OFFSET ADJUSTMENT
- DIFFERENTIAL INPUT CHANNELS
- SOFTWARE CONTROLLED GAIN AND CHANNEL SELECT
- 85dB CMRR
- COMPACT 32 PIN DIP
- MIL-STD-883 SCREENING AVAILABLE

APPLICATIONS

- HIGH PERFORMANCE DATA ACQUISITION
- MILITARY SYSTEMS

DESCRIPTION

The HI-5900 comprises "front end" components of a data acquisition system including an eight channel differential multiplexer, programmable gain instrumentation amplifier (PGA), and Track and Hold amplifier. Adding a timing circuit and one A to D converter yields a complete data acquisition system. A 50kHz channel-to-channel throughput rate is achieved when the HI-5900 is used with a fast 12 bit A to D converter such as HARRIS HI-5712.

Each output line of the input multiplexer is buffered by a high-quality non-inverting amplifier. This isolates each line from source resistances external to the 5900, preserving the high CMRR of the instrumentation amplifier block. Also, the buffers provide a high input impedance for each channel.

The PGA, which includes an op amp, a monolithic resistor network and a four channel differential multiplexer, offers precision inverting gain values of -1, -2, -4, and -8. The voltage gain is selected by a two bit digital word. The output of the PGA drives the Track and Hold amplifier, and the ground side of the PGA is isolated by a buffer amplifier to maintain a high CMRR.

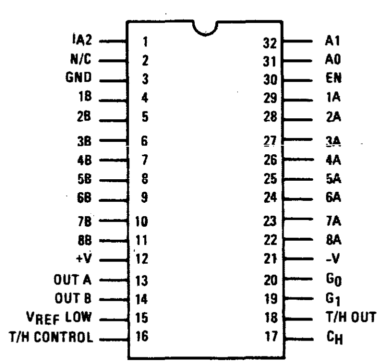
The output Track/Hold amplifier is a monolithic device, internally connected for non-inverting unity gain. In the sample mode is operates as a high performance buffer amplifier. With an external holding capacitor, it may be switched to HOLD with an effective aperture delay time of 30ns.

The packaging technique involves monolithic chips mounted in leadless chip carriers (LCC's) and soldered to both sides of a multilayer ceramic substrate. Each LCC may undergo reliability screening such as MIL-STD-883, Method 5004/Class B, before assembly on the substrate. The resulting package is a compact 32 pin DIP.

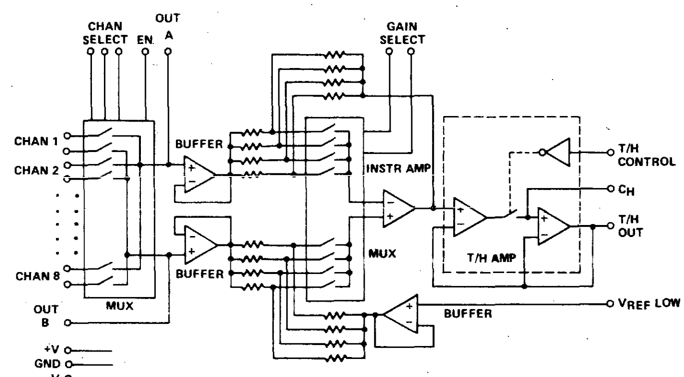
The HI-5900 is offered as a high performance front-end section for military and industrial data acquisition systems. It is designed for interface with computers and is well suited for high-rel applications.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V- Terminals	40V
Digital Input Overvoltage (Multiplexers)	
V_{Supply} (+)	+4V
V_{Supply} (-)	-4V
Analog Input Overvoltage	
V_{Supply} (+)	+20V
V_{Supply} (-)	-20V
Output Current	Short Circuit Protected
Operating Temperature Range	
HA-5900-5	$0^oC \leq T_A \leq +75^oC$
HA-5900-2	$-55^oC \leq T_A \leq +125^oC$
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$
Internal Power Dissipation	650mW
T/H Control Input	+8, -15V

ELECTRICAL CHARACTERISTICS Unless otherwise specified: $V_S = \pm15V$; C_H = 1000pF; V_{IH} = 4.0V; V_{IL} = 0.8V

		HI-5900-2 -55°C to +125°C			HI-5900-5 0°C to +70°C			
PARAMETER	TEMP	MIN	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
ANALOG INPUT CHAR. EACH CHANNEL								
Offset Voltage	+25°C		2	7		3	10	mV
	Full			9			12	mV
Bias Current	+25°C		80	300		80	300	nA
	Full		90	600		80	600	nA
Offset Current	+25°C		15	150		20	150	nA
	Full		30	300		30	300	nA
Common Mode Range	Full	±10			±10			V
Common Mode Rejection Ratio (V_{CM} = ±10V) Any Gain	Full	80	85		74	85		dB
DIGITAL INPUT CHAR.								
Multiplexer Digital Input Current (High or Low)	Full		0.5	1		0.5	1	μA
Track/Hold Digital Input Current								
$V_{IN} \leq 0.8V$	Full			0.8			0.8	mA
$V_{IN} \geq 4.0V$	Full			20			20	μA
TRANSFER CHARACTERISTICS								
Small Signal Bandwidth (Gain = 1)	+25°C		2			2		MHz
Full Power Bandwidth (Gain = 1, V_0 = ±10V)	+25°C		70			70		kHz
Crosstalk (Sample Mode, Gain = 8, 1kHz 20VP -P Input on all but Selected Channel)	+25°C	-80	-90		-80	-90		dB
"Off Isolation (Hold Mode, Gain = 1, 1kHz 20V P-P Input)	+25°C		-76			-76		dB
Acquisition Time (Note 2), to 0.01%	+25°C		9			9		μs
Gain - Absolute Error								
Inverting Gain Of -1, -2,	Full		0.01	0.1		0.01	0.2	%
Inverting Gain Of -4, -8	Full		0.01	0.2		0.01	0.2	%
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	±10			±10			V
Output Current	+25°C	±10			±10			mA
Output Resistance	+25°C		5			5		Ω
DYNAMIC CHARACTERISTICS								
t_{ON}, Enable (MUX)	+25°C		300			300		ns
t_{OFF}, Enable (MUX)	+25°C		300			300		ns
Slew Rate	+25°C		±4			±4		V/μs
Droop Rate (T/H)	+25°C		5			5		nV/μs
	Full			20			5	μV/μs
Charge Transfer (T/H)	25°C		10			10		pC
Effective Aperture Delay Time (T/H)	+25°C		30			30		ns
Aperture Uncertainty (T/H)	+25°C		5			5		ns
POWER SUPPLY CHARACTERISTICS								
I_+	+25°C			13			13	mA
	Full		8.5	15		8.0	15	mA
I_-	+25°C			13			13	mA
	Full		6.5	15		6.0	15	mA
Power Supply Rejection Ratio, V+	Full	76	90		70	90		dB
Power Supply Rejection Ratio, V-	Full	80	100		80	100		dB

NOTES: 1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

2. Acquisition Time is defined for a change of channel (+10V on chan. 1 to 0V on chan. 8) with simultaneous change from HOLD to TRACK mode. Gain = -1.

HARRIS

HI-5901

Analog Data Acquisition Signal Processor

INTERFACE

Harris Semiconductor

FEATURES

- INPUT OVERVOLTAGE PROTECTION
- SOFTWARE CONTROLLED GAIN AND INPUT CHANNEL SELECTION
- 16 PSEUDO-DIFFERENTIAL/SINGLE ENDED INPUT CHANNELS
- INVERTING GAINS OF -1, -2, -4 AND -8
- -90dB CROSSTALK
- 0.01% GAIN ERROR
- 9μs ACQUISITION TIME
- DROOP RATE: 5nV/μsec
- LOW POWER DISSIPATION 250mW
- COMPACT 32 PIN DIP
- MIL-STD-883 SCREENING AVAILABLE

APPLICATIONS

- MULTI-CHANNEL DATA ACQUISITION SYSTEMS
- STATUS MONITORING SYSTEMS
- PROCESS CONTROL SYSTEMS
- INSTRUMENTATION
- HIGH RELIABILITY DAS's

DESCRIPTION

The HI-5901 is a data acquisiton front end subsystem intended for multisensor based high-level applications, requiring conversion of analog input data to digital form for computer processing. It provides sixteen single-ended or pseudo-differential channels of fault-protected multiplexed inputs, programmable gains of-1,-2,-4,-8 and a buffered track and hold output block compatible with any commercially available A/D converter. All these functions are digitally selectable through appropriate coding of seven control terminals. Input channel expansion can be easily implemented through addition of external multiplexers and proper utilization of the enable-command pin.

Being self-contained units except for the holding capacitor, they facilitate user applications and eliminate the need for selection of high-priced precision resistors or labor intensive adjustments to achieve the accuracy levels specified.

This product provides channel to channel throughput rates of 50kHz at ±10 volt signal range when used in connection with a fast 12 bit A/D converter such as the HI-5712. In addition, it offers excellent input characteristics such as low input offset voltage with offset nulling capability, low input currents, very high input impedance, and very low crosstalk. Typical acquisition time and gain error are 9 microseconds and ±0.01%, respectively. The internal track and hold amplifier features an effective aperture delay time of 30ns and a droop rate of 5nV/μsec. Total power dissipation is only 250mW.

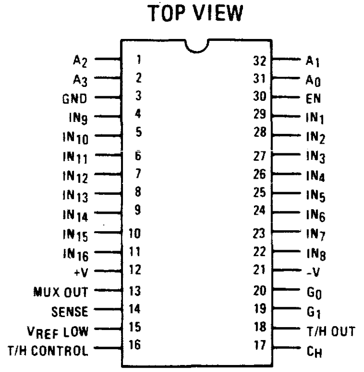
A complete high-speed and high precision data acquisition system with 15 bits of dynamic range can be easily implemented with only three components: the HI-5901, the HI-5712, and an offset nulling DAC. Board space required is 3 square inches and total weight is less than 25 grams.

The manufacturing technique adopted for the HI-5901 involves monolithic dice packaged in leadless chip carriers (LCC's) and soldered to both sides of a multilayer ceramic substrate. The resulting product is a compact and easy-to-use 32 pin DIP.

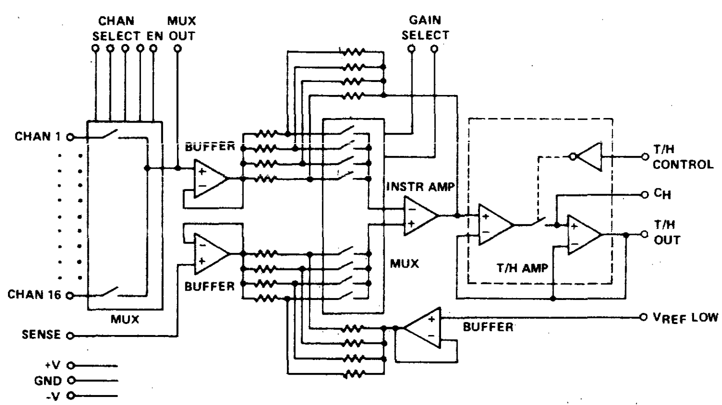
The HI-5901 is intended for military, aerospace, industrial and instrumentation applications. MIL-STD-883 Class B and high reliability commercial grades are both available as standard products.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V- Terminals	40V	Output Current	Short Circuit Protected
Digital Input Overvoltage (Multiplexers)		Operating Temperature Range	
V_{Supply} (+)	+4V	HA-5901-5, -7	$0^oC \leq T_A \leq +75^oC$
V_{Supply} (-)	-4V	HA-5901-2, -8	$-55^oC \leq T_A \leq +125^oC$
Analog Input Overvoltage		Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$
V_{Supply} (+)	+20V	Internal Power Dissipation	650mW
V_{Supply} (-)	-20V	T/H Control Input	+8, -15V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified: $V_S = \pm15V$; $C_H = 1000pF$; $V_{IH} = 4.0V$; $V_{IL} = 0.8V$

PARAMETER	TEMP	HI-5901-2, -8 -55°C to +125°C MIN	TYP.	MAX.	HI-5901-5, -7 0°C to +70°C MIN.	TYP.	MAX.	UNITS
ANALOG INPUT CHAR. EACH CHANNEL								
Offset Voltage	+25°C		2	7.5		3	10.5	mV
	Full			9.5			13	mV
Bias Current	+25°C		80	300		80	300	nA
	Full		90	600		80	600	nA
Offset Current	+25°C		15	150		20	150	nA
	Full		30	300		30	300	nA
Common Mode Range	Full	±10			±10			V
Common Mode Rejection Ratio (V_{CM} = ±10V) Any Gain	Full	80	85		74	85		dB
DIGITAL INPUT CHAR.								
Multiplexer Digital Input Current (High or Low)	Full		0.5	1		0.5	1	μA
Track/Hold Digital Input Current								
$V_{IN} \leq 0.8V$	Full			0.8			0.8	mA
$V_{IN} \geq 4.0V$	Full			20			20	μA
TRANSFER CHARACTERISTICS								
Small Signal Bandwidth (Gain = 1)	+25°C		2			2		MHz
Full Power Bandwidth (Gain = 1, V_0 = ±10V)	+25°C		70			70		kHz
Crosstalk (Sample Mode, Gain = 8, 1kHz 20VP -P Input on all but Selected Channel)	+25°C	-80	-90		-80	-90		dB
"Off Isolation (Hold Mode, Gain = 1, 1kHz 20V P-P Input)	+25°C		-76			-76		dB
Acquisition Time (Note 2), to 0.01%	+25°C		9			9		μs
Gain - Absolute Error								
Inverting Gain Of -1, -2,	Full		0.01	0.1		0.01	0.2	%
Inverting Gain Of -4, -8			0.01	0.2		0.01	0.2	%
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	±10			±10			V
Output Current	+25°C	±10			±10			mA
Output Resistance	+25°C		5			5		Ω
DYNAMIC CHARACTERISTICS								
t_{ON}, Enable (MUX)	+25°C		300			300		ns
t_{OFF}, Enable (MUX)	+25°C		300			300		ns
Slew Rate	+25°C		±4			±4		V/μs
Droop Rate (T/H)	+25°C		5			5		nV/μs
	Full			20			5	μV/μs
Charge Transfer (T/H)	25°C		10			10		pC
Effective Aperture Delay Time (T/H)	+25°C		30			30		ns
Aperture Uncertainty (T/H)	+25°C		5			5		ns
POWER SUPPLY CHARACTERISTICS								
I_+	+25°C			13			13	mA
	Full		8.5	15		8.0	15	mA
I_-	+25°C			13			13	mA
	Full		6.5	15		6.0	15	mA
Power Supply Rejection Ratio, V+	Full	76	90		70	90		dB
Power Supply Rejection Ratio, V-	Full	80	100		80	100		dB

NOTES: 1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Acquisition Time is defined for a change of channel (+10V on chan. 1 to 0V on chan.16) with simultaneous change from HOLD to TRACK mode. Gain = -1.

HARRIS

HD-0165

Keyboard Encoder

FEATURES

- STROBE OUTPUT
- KEY ROLLOVER OUTPUT
- EXPANDABLE: 2 PACKAGES REQUIRED FOR FULL TELETYPEWRITER, EIGHT-BIT ENCODING
- SINGLE +5.0V SUPPLY REQUIRED
- DTL/TTL OUTPUTS
- MONOLITHIC RELIABILITY

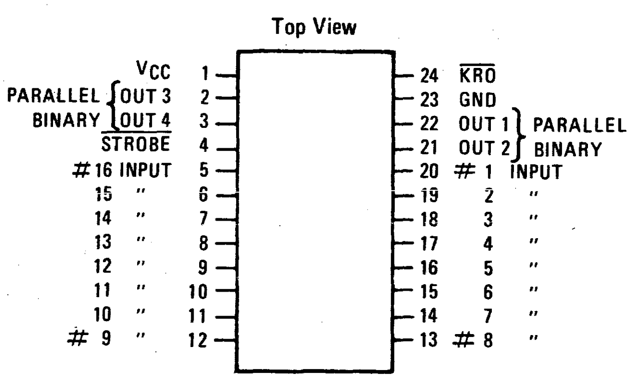
APPLICATIONS

- MICROPROCESSOR DATA ENTRY (16 KEY TO HEX CODE)
- BCD DATA ENTRY
- TYPEWRITER TYPE KEYBOARDS
- CONTROL PANELS

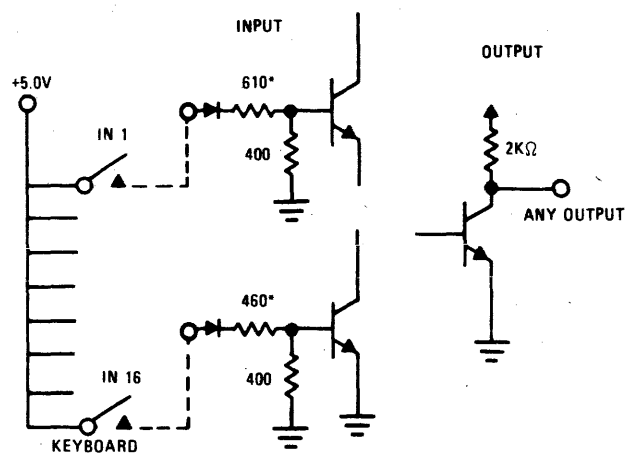
DESCRIPTION

The HD-0165 Keyboard Encoder is a 16 line to four-bit parallel encoder intended for use with manual data entry devices such as calculator or typewriter keyboards. In addition to the encoding function, there is a Strobe output and a Key Rollover output which energizes whenever two or more inputs are energized simultaneously. Any four-bit code can be implemented by proper wiring of the input lines. Inputs are normally wired through the key switches to the +5.0V power supply. Full typewriter keyboard encoding up to eight bits can be accomplished with two Encoder circuits by the use of double pole key switches or single pole switches with two isolation diodes per key. Outputs will interface with all popular DTL and TTL logic families. The circuit is packaged in a hermetic 24-pin dual-in-line package and operates over the temperature range of 0°C to +75°C.

PINOUT



EQUIVALENT CIRCUITS



* EQUIVALENT RESISTORS FOR OTHER INPUTS ARE BETWEEN THESE TWO VALUES

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V	Output Current	30mA
Input Voltage	+5.5V	Storage Temperature	-65° to $+150^{\circ}C$
Output Voltage	+5.5V	Operating Temperature (Case)	$0^{\circ}C$ to $+75^{\circ}C$

ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{CC} = +5.0V \pm 5\%$
$T_{Case} = 0^{\circ}C$ to $+75^{\circ}C$
Unless otherwise specified

	PARAMETER		SYM.	LIMITS MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
	Input Current	"1"	I_{IH}			17	mA	$V_{IN} = +5.0V$
D.C.	Output Voltage	"0"	V_{OL}		+0.2	+0.4	V	$V_{IH} = +4.5V$ $I_{OL} = 10mA$
						+0.4		$V_{IH} = +3.75V$ $I_{OL} = 3.2mA$
		"1"	V_{OH}	+2.4	+4.0			V_{IL} = Open Circuit, $I_{OH} = -240\mu A$
	Power Supply Current	Operating	I_{CC}			52	mA	One Input at +5.25V
		Maximum	I_{CCM}			88	mA	All Inputs at +5.25V
A.C.	Skew Time (Note 1)		T_{SK}		80	200	ns	$T_{Case} = 25^{\circ}C$, $V_{CC} = V_{IN} = +5.0V$, $C_L < 50pF$

NOTE: (1) Skew time is the maximum time differential between propagation delay times of any outputs including strobe and K_{RO}.

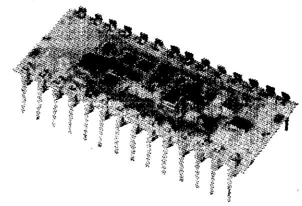
TRUTH TABLE

INPUTS																OUTPUTS					
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	1	2	3	4	$\overline{St.}$	$\overline{K_{RO}}$
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H
H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L	H
L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	L	H
L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	H	L	H
L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	L	H
L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	L	H	L	H
L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	H	L	H
L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	H	L	L	H	L	H
L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	H
L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	H	H	L	L	H
L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	H	L	L	H
L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	H	L	H	L	L	H
L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	H	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	H	H	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	H	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	L	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	H
ANY TWO OR MORE HIGH																X	X	X	X	L	L

INPUTS: L = Open Circuit or < +1.0V H = > +4.5V Current Source
OUTPUTS: L = < +0.4V H = > +2.4V X = Erroneous Data

8 Channel, 12 Bit DAS with μP Interface

HS 9410 Series

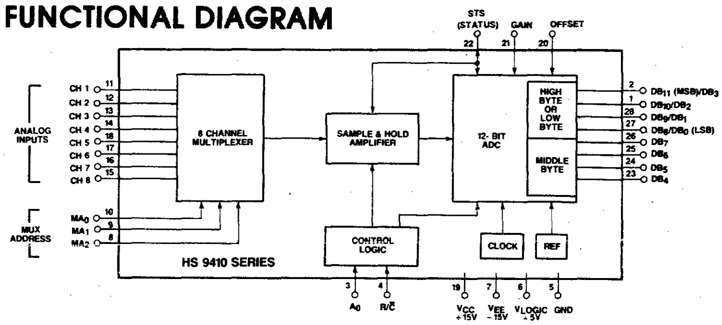


$99 (100's)

FEATURES

- Complete 8 Channel, 12-Bit Data Acquisition System with MUX, S/H, REF, Clock and three-state outputs
- Full 8- or 16-Bit Microprocessor Bus Interface
- Guaranteed Linearity Over Temperature
- High Throughput Rate: 30kHz
- Hermetic 28-pin Metal or Low Cost Epoxy DIP
- Low Power: 900mW

FUNCTIONAL DIAGRAM



SPECIFICATIONS

Resolution	12 Bits
Number of Channels	8 Single Ended
Throughput Rate	30 kHz
Power Supply	±15V, +5V
Package	28-pin DIP
Other Specifications	See Ordering Guide

ORDERING GUIDE

MODEL NUMBER[1]	INPUT RANGE	SYSTEM ACCURACY (% FSR)	FULL SCALE T.C. (PPM/°C)	TEMP. RANGE	SCREENING	PRICE (1-9)
HS 94XXJ	SEE NOTE 1	±0.025	50.0	0°C to +70°C	0.4% AQL*	$115.00
HS 94XXK		±0.012	20.0	0°C to +70°C	0.4% AQL*	125.00
HS 94XXS		±0.025	50.0	−55°C to +85°C	0.4% AQL*	215.00
HS 94XXT		±0.012	20.0	−55°C to +85°C	0.4% AQL*	265.00
HS 94XXS/B		±0.025	50.0	−55°C to +85°C	MIL-STD-883B	370.00
HS 94XXT/B		±0.012	20.0	−55°C to +85°C	MIL-STD-883B	450.00

NOTES:
1. MODEL HS 94XX

MODEL SUFFIX	INPUT RANGE
10	0 to +10V
11	±5V
12	±10V

Add letter suffix as required above.

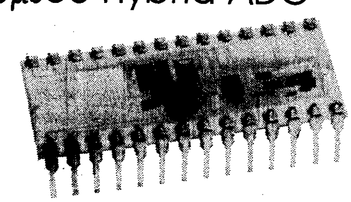
***0.4% AQL** All units have full burn-in at +85°C. Acceptable quality level (AQL) of 0.4% means that Hybrid Systems guarantees that there will be no rejects in a sample lot of 100 pieces. That's more than twice as tough as it has to be — even for military applications. Specifications subject to change without notice.

Technical knockouts from the Contenders!

Industry Standard 574

12-Bit, 30μsec Hybrid ADC

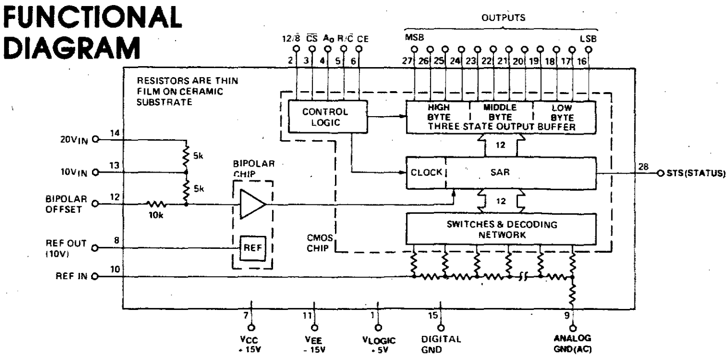
$34.50 (100's)



FEATURES

- Complete 12-Bit A/D Converter
- 30μSec Conversion Time
- Power 400mW
- No Missing Codes
- μP BUS Compatible
- Commercial and MIL-STD-883B Processing
- Hermetic, 28-pin DIP, Metal Package

FUNCTIONAL DIAGRAM



SPECIFICATIONS

Resolution	12 Bits
Linearity Error	
Differential	No Missing Codes
Integral	±0.013% F.S.R.
End Point Error	
Offset Bipolar	±0.1% F.S.R.
Unipolar	±0.05% F.S.R.
Full Scale	±0.3% F.S.R.
Conversion Time	30μsec
Temperature Stability	
Linearity	±0.5ppm/°C F.S.R.
Offset	±5ppm/°C F.S.R.
Full Scale	±10ppm/°C F.S.R.
Power	±15V, +5V/600mW
Package	28-pin DIP

ORDERING GUIDE

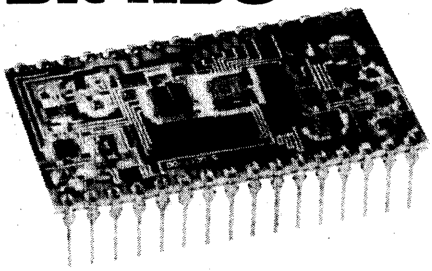
MODEL NUMBER	RESOLUTION NO MISSING CODES (T_{min} to T_{max})	LINEARITY ERROR	TEMP. RANGE	SCREENING	PRICE (1-9)
HS 574J	11 Bits	±1LSB	0°C to +70°C	0.4% AQL*	49.50
HS 574K	12 Bits	±½LSB	0°C to +70°C	0.4% AQL*	61.50
HS 574L	12 Bits	±½LSB	0°C to +70°C	0.4% AQL*	89.00
HS 574S	11 Bits	±1LSB	−55°C to +125°C	0.4% AQL*	136.00
HS 574T	12 Bits	±1LSB[1]	−55°C to +125°C	0.4% AQL*	183.00
HS 574U	12 Bits	±1LSB[1]	−55°C to +125°C	0.4% AQL*	265.00
HS 574S/B	11 Bits	±1LSB[1]	−55°C to +125°C	883B	164.00
HS 574T/B	12 Bits	±1LSB[1]	−55°C to +125°C	883B	220.00
HS 574U/B	12 Bits	±1LSB[1]	−55°C to +125°C	883B	315.00

[1]Note: ±½ LSB max error from −25°C to −85°C

Hybrid Systems CORPORATION 22 Linnell Circle, Billerica, MA 01821 (617)667-8700, TWX 710-347-1575

Complete 0.0008% 16-Bit ADC

HS 9516 Series



$239.00 (1-9)

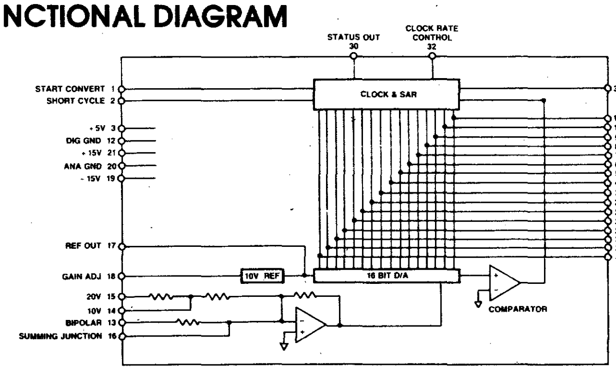
FEATURES

- True 16-bit (±0.0008†) Linearity Error
- Full 16-bit Resolution (1 part in 65,536)
- No Missing Codes (16-bits) 0°C to +70°C
- Six User Selectable Input Ranges
- 100μsec Conversion Time
- Low Full Scale Drift 10ppm/°C (Max)
- Low Power - 900mW Typical

SPECIFICATIONS

Resolution	16 Bits
Analog Inputs	
Unipolar	0 to +5V, 0 to +10V, 0 to +20V
Bipolar	±2.5V, ±5V, ±10V
Outputs	Parallel, OBIN, 2's Comp
Accuracy	
Scale Factor Error	±0.1% max (Adj. to Zero)
Zero Error (Unipolar or Bipolar)	±0.1% FSR max (Adj. to Zero)
Differential Linearity Error	
HS 9516-6	±0.0015% FSR (±1 LSB) max
HS 9516-5	±0.003% FSR (±2 LSB) max
HS 9516-4	±0.006% FSR (±4 LSB) max
No Missing Codes	0°C to +70°C
Integral Linearity Error	
HS 9516-6	±0.0008% FSR (±½ LSB) max
HS 9516-5	±0.0015% FSR (±1 LSB) max
HS 9516-4	±0.003% FSR (±2 LSB) max
Stability	
Scale Factor Tempco	±10ppm/°C max
Zero Tempco	
Unipolar	±2ppm FSR/°C
Bipolar	±5ppm FSR/°C
Integral Linearity Tempco	±1ppm FSR/°C max
Differential Linearity	±0.5ppm FSR/°C max
Power	±15V, +5V
Package	32-pin Triple DIP
Temperature Range	0°C to +70°C

FUNCTIONAL DIAGRAM



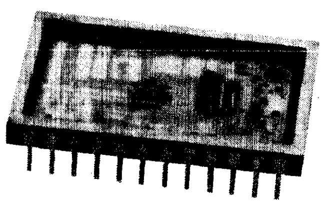
ORDERING GUIDE

MODEL	DESCRIPTION	PRICE
HS 9516-4	16-Bit ADC with 14-Bit Integral & Differential Linearity	$239.00
HS 9516-5	16-Bit ADC with 15-Bit Integral & Differential Linearity	249.00
HS 9516-6	16-Bit ADC with 16-Bit Integral & Differential Linearity	299.00

Technical knockouts from the Contenders!

12-Bit Adjustment Free ADC's

HS 5200 Series

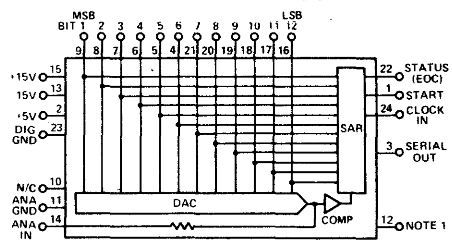


$160.00 (1-9)

FEATURES

- 12-Bit Conversion in 10μSec (Typical)
- Adjustment-Free (±0.0125%) Linearity
- Low Power 670mW (Typical)
- Hermetic, 24-pin DIP, Metal Package
- MIL-STD-883B Processing
- Pin Compatible to MN5200

FUNCTIONAL DIAGRAM



SPECIFICATIONS

Resolution	12 Bits
Linearity	±½LSB
Absolute Accuracy[1]	±0.4%
Conversion Time	13μsec
Temperature Range	
C-versions	0°C to +70°C
B-versions	−55°C to +125°C
Power	+15V, +5V/870mW
Package	24-pin DIP, Metal

[1] Includes all errors, gain, zero, and linearity over temperature.

0.4% A.Q.L.* All units have full power burn-in at +85°C. Acceptable quality level (AQL) of 0.4% means that Hybrid Systems guarantees that there will be no rejects in a sample lot of 100 pieces. That's more than twice as tough as it has to be—even for military applications.

ORDERING GUIDE

MODEL	RESOLUTION / CONVERSION TIME	INPUT RANGE	TEMP RANGE	PROCESSING	PRICE (1-9)
HS 5210C-12	12 Bits, 13μSec	0 to −10V	0°C to +70°C	0.4% AQL*	$160.00
HS 5211C-12	12 Bits, 13μSec	± 5V	0°C to +70°C	0.4% AQL*	$160.00
HS 5212C-12	12 Bits, 13μSec	±10V	0°C to +70°C	0.4% AQL*	$160.00
HS 5213C-12	12 Bits, 13μSec	0 to −10V	0°C to +70°C	0.4% AQL*	$160.00[1]
HS 5214C-12	12 Bits, 13μSec	± 5V	0°C to +70°C	0.4% AQL*	$160.00[1]
HS 5215C-12	12 Bits, 13μSec	±10V	0°C to +70°C	0.4% AQL*	$160.00[1]
HS 5216C-12	12 Bits, 13μSec	0 to +10V	0°C to +70°C	0.4% AQL*	$160.00
HS 5210B-12	12 Bits, 13μSec	0 to −10V	−55°C to +125°C	MIL-STD-883B	$190.00
HS 5211B-12	12 Bits, 13μSec	± 5V	−55°C to +125°C	MIL-STD-883B	$190.00
HS 5212B-12	12 Bits, 13μSec	±10V	−55°C to +125°C	MIL-STD-883B	$190.00
HS 5213B-12	12 Bits, 13μSec	0 to −10V	−55°C to +125°C	MIL-STD-883B	$190.00[1]
HS 5214B-12	12 Bits, 13μSec	± 5V	−55°C to +125°C	MIL-STD-883B	$190.00[1]
HS 5215B-12	12 Bits, 13μSec	±10V	−55°C to +125°C	MIL-STD-883B	$190.00[1]
HS 5216B-12	12 Bits, 13μSec	0 to +10V	−55°C to +125°C	MIL-STD-883B	$190.00

[1] 10V external reference user supplied

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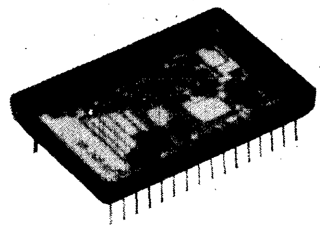
12-Bit 10μSec Hi Rel ADC

ADC85 Series



$134.00 (1-9)

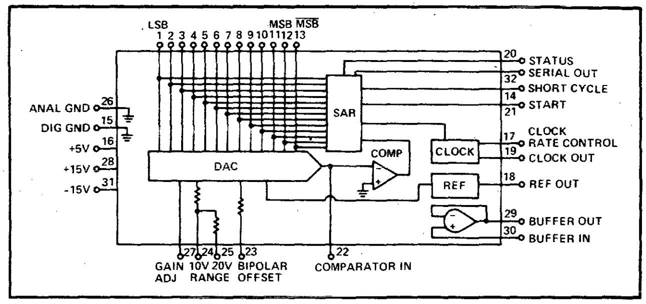
FEATURES

- −55°C to +125°C Operation
- No Missing Codes
- Replaces ADC84/85, HX12B, HZ12B
- Low Power 1.2W (maximum)

SPECIFICATIONS

Resolution	12 Bits
Analog Inputs	
Unipolar	0 to +5V, 0 to +10V
Bipolar	±2.5V, ±5V, ±10V
Outputs	Parallel, Serial/TTL
Coding	CBIN/COBIN
Linearity	±0.012% F.S.R. (maximum)
Conversion Time	8.8μSec, 10μSec (maximum)
Scale Factor Drift	15ppm/°C (maximum)
Linearity Drift	2ppm/°C (maximum)
Temperature Range	−55°C to +125°C
Power	±15V, +5V/1.2W (maximum)
Package	32-pin DIP

FUNCTIONAL DIAGRAM



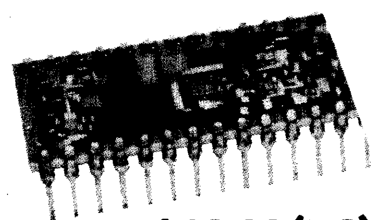
ORDERING GUIDE

MODEL	RESOLUTION	ACCURACY	TEMP RANGE	PROCESSING	PRICE
HS ADC85B	12 Bits	12 Bits	−55°C to +125°C	MIL-STD-883B	$205.00
HS ADC85C	12 Bits	12 Bits	0°C to +70°C	0.4% AQL*	$134.00

Technical knockouts from the Contenders!

Complete μP Compatible 12 Bit DAC

DAC338, HS 9338 Series



$39.00 (1-9)

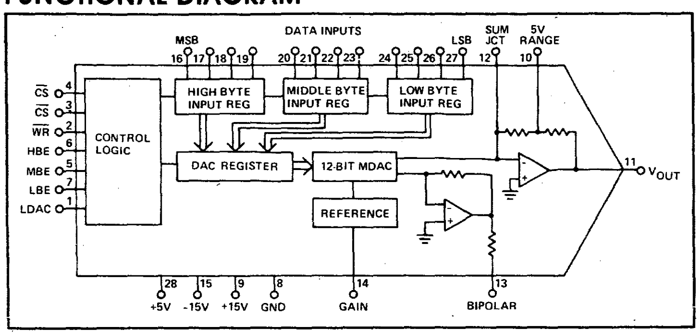
FEATURES

- μP BUS Compatible
- 0 to +10V, 0 to +5V, ±10V, ±5V Output Ranges
- Binary Coding
- Linearity ±0.01%
- 2.5μSec Settling Time

SPECIFICATIONS

Resolution	12 Bits
Coding	BIN, OBIN
Logic	CMOS, TTL
Output	0 to +10V, ±10V, ±5V
Linearity	
−0	±0.05% F.S.R.
−1	±0.02% F.S.R.
−2	±0.01% F.S.R.
Settling Time	20μSec
Scale Factor Drift	15ppm/°C
Temperature Range	0°C to +70°C
Power	+15V/450mW
Package	28-pin DIP

FUNCTIONAL DIAGRAM



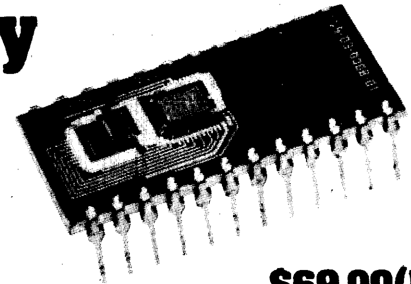
ORDERING GUIDE

MODEL	RESOLUTION	LINEARITY	TEMP RANGE	PROCESSING	PRICE (1-9)
DAC338B-12-0	12 Bits	10 Bits	−55°C to +125°C	MIL-STD-883B	$118.00
DAC338B-12-1	12 Bits	11 Bits	−55°C to +125°C	MIL-STD-883B	$126.00
DAC338B-12-2	12 Bits	12 Bits	−55°C to +125°C	MIL-STD-883B	$137.00
HS 9338-0	12 Bits	10 Bits	0°C to +70°C	0.4% AQL*	$ 39.00
HS 9338-1	12 Bits	11 Bits	0°C to +70°C	0.4% AQL*	$ 44.00
HS 9338-2	12 Bits	12 Bits	0°C to +70°C	0.4% AQL*	$ 49.00

Hybrid Systems CORPORATION 22 Linnell Circle, Billerica, MA 01821 (617)667-8700, TWX 710-347-1575

14, 15 and 16 Bit Linearity Latched MDAC's

DAC9331-16 Series



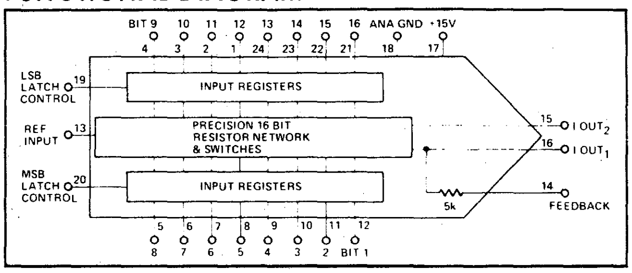
$69.00(1-9)

FEATURES
- Up to 16-Bit (0.0008%) Linearity
- Two-Chip Construction
- Input Registers
- 24-pin DIP, Metal Package
- 2 and 4-Quadrant Multiplication
- Single Supply Operation
- Low Power 60mW

SPECIFICATIONS

Resolution	16 Bits
Coding	BIN, OBIN
Logic	CMOS, TTL
Reference Input	0 to ±25V
Output	$200\mu A/V_{REF}$
Linearity	
DAC9331-16-4	±0.003% F.S.R.
DAC9331-16-5	±0.0015% F.S.R.
DAC9331-16-6	±0.0008% F.S.R.
Settling Time	2μSec
Scale Factor Drift	2ppm/°C
Temperature Range	0°C to +70°C
Power	+15V/60mW
Package	24-pin DIP

FUNCTIONAL DIAGRAM



ORDERING GUIDE

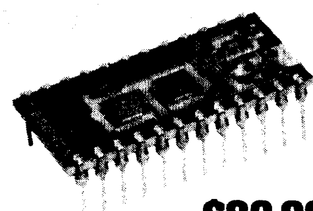
MODEL	RESOLUTION	LINEARITY	TEMP RANGE	PROCESSING	PRICE (1-9)
DAC9331-16-4	16 Bits	14 Bits	0°C to +70°C	0.4% AQL*	$ 69.00
DAC9331-16-5	16 Bits	15 Bits	0°C to +70°C	0.4% AQL*	$109.00
DAC9331-16-6	16 Bits	16 Bits	0°C to +70°C	0.4% AQL*	$169.00*

* $99.00 (100's)

Technical knockouts from the Contenders!

Complete Buffered 16 and 18 Bit DAC's

DAC9377, 377 Series



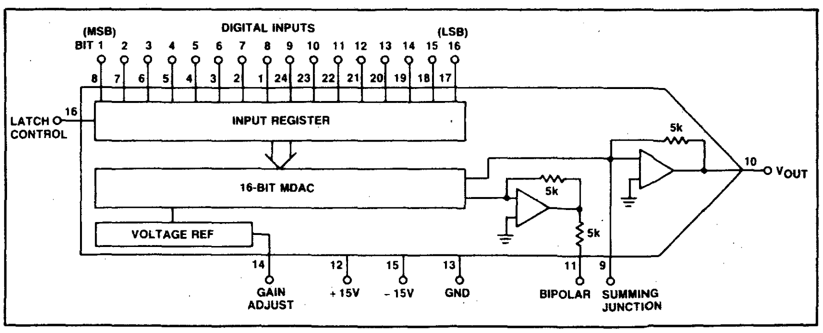
$89.00(1-9)

FEATURES
- True 16-Bit (0.0008%) Linearity
- μP Compatible
- Complete DAC
- 24-pin DIP, Metal Package
- Low Power 450mW

SPECIFICATIONS

Resolution	16 Bits, 18 Bits
Coding	BIN, OBIN
Logic	CMOS, TTL
Output	0 to +10V, ±10V
Linearity	
DAC377-18	±0.0008% F.S.R.
DAC9337-16-6	±0.0008% F.S.R.
DAC9337-16-5	±0.0015% F.S.R.
DAC9337-16-4	±0.003% F.S.R.
DAC9377-4D	±0.002% F.S.R.
Settling Time	20μSec
Scale Factor Drift	5ppm/°C
Temperature Range	0°C to +70°C
Power	+15V/450mW
Package	24-pin DIP (9377)
	28-pin DIP, Metal (377)

FUNCTIONAL DIAGRAM



ORDERING GUIDE

MODEL	RESOLUTION	LINEARITY	TEMP RANGE	PROCESSING	PRICE (1-9)
DAC9377-4D	4 BCD	±0.002%	0°C to +70°C	0.4% AQL*	$ 99.00
DAC9377-16-4	16 Bits	14 Bits	0°C to +70°C	0.4% AQL*	$ 89.00
DAC9377-16-5	16 Bits	16 Bits	0°C to +70°C	0.4% AQL*	$129.00
DAC9377-16-6	16 Bits	16 Bits	0°C to +70°C	0.4% AQL*	$199.00
DAC377B-18	18 Bits	16 Bits	-55°C to +125°C	MIL-STD-883B	$395.00
DAC377C-18	18 Bits	16 Bits	0°C to +70°C	0.4% AQL*	$205.00

Hybrid Systems CORPORATION 22 Linnell Circle, Billerica, MA 01821 (617)667-8700, TWX 710-347-1575

Integrating Analog-to-Digital Converters for Display

Maximum Electrical Specification at 25°C unless otherwise noted.

Model	ICL7136	ICL7137	ICL7135	ICL7129	ICL7106/ICL7116	ICL7107/ICL7117
Resolution	±3½ Digit	±3½ Digit	±4½ Digit	±4½ Digit	±3½ Digit	±3½ Digit
Accuracy						
Non-Linearity	±1 Count	±1 Count	±1 Count	±1 Count	±1 Count	±1 Count
Zero Input Reading	±0.000	±0.000	±0.000	±0.000	±0.000	±0.000
Ratiometric Reading	±1.000	±1.000	±1.000	±0.9997	±1.000	±1.000
$V_{IN} = V_{REF}$	±1 Count	±1 Count	±1 Count	±3 Counts	±1 Count	±1 Count
Rollover Error	±1 Count	±1 Count	±1 Count	±1 Count	±1 Count	±1 Count
Stability						
Offset vs. Temperature	1μV/°C	1μV/°C	1μV/°C	1μV/°C	1μV/°C	1μV/°C
Gain vs. Temperature	5 ppm/°C	5 ppm/°C	5 ppm/°C	5 ppm/°C	5 ppm/°C	5 ppm/°C
Conversion Time	0.1 to 3 conv/sec	0.1 to 3 conv/sec	0.1 to 15 conv/sec	0.1 to 6 conv/sec	0.1 to 15 conv/sec	0.1 to 15 conv/sec
Analog Input						
Voltage Range	±200mV to ±2V	±200mV to ±2V	±2V	±200mV to ±2V	±200mV to ±2V	±200mV to ±2V
Impedance	$10^{12}\Omega$	$10^{12}\Omega$	$10^{12}\Omega$	$10^{12}\Omega$	$10^{12}\Omega$	$10^{12}\Omega$
Leakage Current	2pA	2pA	3pA	1pA	2pA	3pA
Noise (peak-to-peak)	15μV typ.	15μV typ.	15μV typ.	7μV typ.	15μV typ.	15μV typ.
Digital Input	—	—	—	Decimal Points Continuity Hold, Range Select	Display Hold (7116)	Display Hold (7117)
Digital Outputs						
Format	Direct 7 Segment LCD Display	Direct 7 Segment LCD Display	Multiplex BCD	4½ Digit Triplexed LCD Display Drive w/Decimal Points, Low Battery and Continuity Indicators	Direct 7 Segment LCD Display	Direct 7 Segment LED Display Comm Anode
Logic Level	AC:4.5V Down from V+	AC:4.5V Down from V+	TTL/CMOS		AC:4.5V Down from V+	DTL/TTL/CMOS
Power Supply						
Voltage	+9V	±5V	±5V	+9V	+9V	±5V
Current	100μA	200μA	1.8mA	1.8mA	1.8mA	1.8mA
Package	40 pin DIP	40 pin DIP	28 pin DIP	40 pin DIP	40 pin DIP	40 pin DIP

*Also available LD110/111/114 (not recommended for new designs), and ICL7126 (recommended use ICL7136).

Integrating Analog-to-Digital Converters for Data Acquisition

Type	Single Chip	Two Chip System***	
Model	ICL7109	ICL8052A/8068 ICL7104-14	ICL8052A/8068 ICL7104-16
Resolution	±12-Bit Binary	±14-Bit	±16-Bit
Accuracy	±1 Count	±1 Count	±1 Count
Microprocessor Compatible	Yes	Yes	Yes
Output	Programmable: 1. Latched parallel 3 state Binary 2. Controlled 2-8 bit bytes	Programmable: 1. Latched parallel 3 state Binary 2. Controlled 2-8 Bit Byte for ICL7104-12/14 3-8 Bit Byte for ICL7104-16	
Control Lines	Run/Hold, Busy, Byte Enables, Mode, Load, Send Enable, Out of Range		
Conversion Time	10ms	80ms	330ms
UART Compatible	Yes	Yes	Yes
Noise (Typical)	15μV	2μV (8068)	2μV (8068)
Input Current	10pA	30pA (8052)	30pA (8052)
Input Voltage Range	+400mV to +4.1V	+100mV to +10V	+200mV to −10V

***ICL8052/8068 and ICL8053 can be combined as analog portion of dual-slope A/D converter under μp control. See ICL8052/8068 and ICL 7104-16 for performance characteristics.

Digital-to-Analog Converters*

Maximum Electrical Specification at 25°C unless otherwise noted.

Model	ICL7134U/B	7145	7146	AD7523	AD7533	AD7520 (7530)	AD7520 (7531)	AD7541
Resolution	14 bit	16 bit	12 bit	8 bit	10 bit	10 bit	12 bit	12 bit
Accuracy	J/K/L	J/K	J/K	J/K/L	J/K/L	J/K/L	J/K/L	J/K/L
Linearity	0.01/0.006/0.003%	0.006/0.003%	0.01%	0.2%/0.1%/0.05%	0.2%/0.1%/0.05%	0.02%/0.01%/0.05%	0.2%/0.1%/0.5%	0.02%/0.01%/0.01%
Zero Offset	10 nA	10 mV	120 µV	50 µA	200 nA	200 nA (300 nA)	200 nA (300 nA)	50 nA
Full Scale Reading	0.003%	0.04/0.02% FSR	0.04/0.02% FSR	1.5% max	1.4%	0.3% typ	0.3% typ	0.3%
Stability								
Gain vs. Temperature	5 ppm/°C	1 ppm/°C typ	5 ppm/°C typ	10 ppm/°C	10 ppm/°C	10 ppm/°C	10 ppm/°C	10 ppm/°C
Linearity vs. Temperature	1 ppm/°C	1 ppm/°C typ	1 ppm/°C typ	2 ppm/°C	2 ppm/°C	2 ppm/°C	2 ppm/°C	2 ppm/°C
Setting Time To 1/2 LSB	0.9 µs typ	3 µs	10 µ	150 ns	600 ns typ	500 ns typ	500 ns typ	1 µs
Input Code	DTL/TTL/CMOS	DTL/TTL/CMOS	DTL/TTL/CMOS	DTL/TTL/CMOS	DTL/TTL/CMOS	DTL/TTL/CMOS	DTL/TTL/CMOS	DTL/TTL/CMOS
Logic Compatibility	Binary (U)		Binary or	Binary	Binary	Binary	Binary	Binary
option	2's Complement (B)	2's Complement	2's Complement	Offset Binary	Offset Binary	Offset Binary	Offset Binary	Offset Binary
Power Supply								
Voltage	+3.5 to +6.0V	4.5 to 5.5V	±4.5 to 5.5V	+6 to +16V	+5 to +15V	+5 to +15V	+5 to +15V	+5 to +16V
Current	2mA	1.2mA	5mA	100 µA	2mA	2mA	2mA	2mA
Package	28 pin DIP	28 pin DIP	28 pin DIP	16 pin DIP	16 pin DIP	16 pin DIP	18 pin DIP	18 pin DIP

*R2R Ladder Multiplying Type

Successive Approximation Analog-to-Digital Converters

Model	ADC0801-4	ICL7115
Resolution	8 bit	14 bit binary
Accuracy	±¼/½/½/1 LSB	±½ LSB
Microprocessor Compatible	Yes	Yes
Output	Programmable: 1. Latched parallel 3' state Binary 2. One 8 bit byte	Programmable: 1. Two latched bytes 2. 15 bit parallel
Control Lines	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0, BUS
Conversion Time	100µs	40µs
UART Compatible	Yes	No
Input Voltage Range	5V span	0 - 5V

Quad Current Switches ICL8018/8019/8020

High speed precision current switches for use in current summing D/A converters. Can be purchased individually or in matched sets with accuracies of 0.01% (ICL8018), 0.1% (ICL8019), or 1.0% (ICL8020)

Sample and Hold

Type	V_{analog} (V_{p-p})	t_{acq}** (µs)	V_{inject}** (mV)	V_{OS} (mV)	Drift Rate (mV/sec)
IH5110	±7.5	6	5	40	5
IH5111	±10	6	5	40	5
IH5112	±7.5	6	5	10	5
IH5113	±10	6	5	10	5
IH5114	±7.5	6	5	5	5
IH5115	±10	6	5	5	5

**C_{STO} = 0.01 µF

Monolithic Voltage Converter—The ICL7660

Converts positive voltage into negative over a range of + 1.5V through + 10V. May be cascaded for higher negative output voltages, paralleled for greater output current, used as a positive voltage multiplier, or any combination of the above. Typical supply current is 170 µA, and output source resistance is 55Ω at T_A = 25°C and I_O = 20 mA

Analog Switches with Driver

Type	No. of Channels	Intersil Device No.	Switch Technology	$r_{DS(on)}$ Ω max(1)	$I_{D(off)}$ nA max	t_{on} μs max	t_{off} μs max	Logic Input: Logic Level	Logic Input: Input Type(2)	Power Consumption mW
		IH5021	P-JFET	100	0.2	0.5	0.5	TTL High Level	lo	
		IH5022	P-JFET	150	0.2	0.5	0.5	TTL Low Level	lo	
SPST	1	IH5023	P-JFET	100	0.2	0.5	0.5	TTL High Level	lo	
		IH5024	P-JFET	150	0.2	0.5	0.5	TTL Low Level	lo	
		IH5037	P-JFET	100	0.5	0.2	0.2	TTL High Level	lo	
		IH5038	P-JFET	150	0.5	0.2	0.2	TTL High Level	lo	
		IH5040	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS, PMOS	hi	.035
		IH5140	CMOS	50	0.1	0.1	0.075	TTL, CMOS	hi	.035
		DG180	N-JFET	10	10.0	0.3	0.25	DTL, TTL, RTL	lo	120
		DG181	N-JFET	30	1.0	0.15	0.13	DTL, TTL, RTL	lo	120
		DG182	N-JFET	75	1.0	0.25	0.13	DTL, TTL, RTL	lo	120
		DGM182	CMOS	75	0.1	0.25	0.13	DTL, TTL, RTL	lo	.035
		DG200	CMOS	70	1.0	0.7	0.5	DTL, TTL, RTL, CMOS, TTL High Level	lo	3.0
		IH5017	P-JFET	100	0.2	0.5	0.5	TTL, High Level	lo	
		IH5018	P-JFET	150	0.2	0.5	0.5	TTL, Low Level	lo	
		IH5019	P-JFET	100	0.2	0.5	0.5	TTL, High Level	lo	
SPST	2	IH5020	P-JFET	150	0.2	0.5	0.5	TTL, Low Level	lo	
		IH5033	P-JFET	100	0.5	0.2	0.2	TTL, High Level	lo	
		IH5034	P-JFET	150	0.5	0.2	0.2	TTL, High Level	lo	
		IH5035	P-JFET	100	0.5	0.2	0.2	TTL, High Level	lo	
		IH5036	P-JFET	150	0.5	0.2	0.2	TTL, High Level	lo	
		IH5041	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS, PMOS	hi	.035
		IH5048	CMOS	35	1.0	0.25	0.15	DTL, TTL, RTL, CMOS, PMOS	hi	.035
		IH5141	CMOS	50	0.1	0.1	0.075	TTL, CMOS	hi	.035
		IH5341	CMOS	75	0.1	0.3	0.15	TTL, CMOS	hi	.035
		IH5013	P-JFET	100	0.2	0.5	0.5	TTL, High Level	lo	
		IH5014	P-JFET	150	0.2	0.5	0.5	TTL, Low Level	lo	
		IH5015	P-JFET	100	0.2	0.5	0.5	TTL, High Level	lo	
		IH5016	P-JFET	150	0.2	0.5	0.5	TTL, Low Level	lo	
SPST	3	IH5029	P-JFET	100	0.5	0.2	0.2	TTL, High Level	lo	
		IH5030	P-JFET	150	0.5	0.2	0.2	TTL, High Level	lo	
		IH5031	P-JFET	100	0.5	0.2	0.2	TTL, High Level	lo	
		IH5032	P-JFET	150	0.5	0.2	0.2	TTL, High Level	lo	
		DG118	P-MOSFET	450	-4.0	0.3	1.0	DTL, TTL, RTL	lo	133
		DG201	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS	lo	.350
SPST	4	IH5009	P-JFET	100	0.2	0.5	0.5	TTL, High Level	lo	
		IH5010	P-JFET	150	0.2	0.5	0.5	TTL, Low Level	lo	
		IH5011	P-JFET	100	0.2	0.5	0.5	TTL, High Level	lo	
		IH5011	P-JFET	150	0.2	0.5	0.5	TTL, Low Level	lo	
		IH5025	P-JFET	100	0.5	0.2	0.2	TTL High Level	lo	
		IH5026	P-JFET	150	0.5	0.2	0.2	TTL High Level	lo	
		IH5027	P-JFET	100	0.5	0.2	0.2	TTL High Level	lo	
		IH5028	P-JFET	150	0.5	0.2	0.2	TTL High Level	lo	
		IH5052	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS, PMOS	lo	.350
		IH5053	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS, PMOS	hi	.350
		DG123	P-MOSFET	450	-4.0	0.3	1.0	DTL, TTL, RTL	hi	133
		DG125	P-MOSFET	450	-4.0	0.3	1.0	DTL, TTL, RTL	lo	133
		DG143A	N-JFET	80	1.0	0.4	0.8	DTL, TTL, RTL	(3)	84
		DG144A	N-JFET	30	1.0	0.4	0.8	DTL, TTL, RTL	(3)	84
SPST	5	DG146A	N-JFET	10	10.0	0.5	1.25	DTL, TTL, RTL	(3)	84
		DG161A	N-JFET	15	10.0	0.5	1.25	DTL, TTL, RTL	(3)	90
		DG162A	N-JFET	50	2.0	0.4	0.8	DTL, TTL, RTL	(3)	90
		DG186	N-JFET	10	10.0	0.3	0.25	DTL, TTL, RTL	(3)	73
		DG187	N-JFET	30	1.0	0.15	0.13	DTL, TTL, RTL	(3)	73
		DG188	N-JFET	75	1.0	0.25	0.13	DTL, TTL, RTL	(3)	73
		DGM188	CMOS	75	0.1	0.25	0.13	DTL, TTL, RTL	(3)	.035
SPDT	1	IH5042	CMOS	75	1.0	0.05	0.025	DTL, TTL, RTL PMOS, CMOS	(3)	.035
		IH5050	CMOS	35	1.0	0.25	0.15	DTL, TTL, RTL PMOS, CMOS	(3)	.035
		IH5142	CMOS	50	0.1	0.175	0.125	TTL, CMOS	(3)	.035

Analog Switches with Driver continued

Type	No. of Channels	Device No.	Switch Technology	$r_{DS(on)}$ Ω max(1)	$I_{D(off)}$ nA max	t_{on} μs max	t_{off} μs max	Logic Input: Logic Level	Logic Input: Input Type(2)	Power Consumption mW
		DG189	N-JFET	10	10.0	0.3	0.25	DTL, TTL, RTL	(3)	120
		DG190	N-JFET	30	1.0	0.15	0.13	DTL, TTL, RTL	(3)	120
		DG191	N-JFET	75	1.0	0.25	0.13	DTL, TTL, RTL	(3)	120
		DGM191	CMOS	75	0.1	0.25	0.13	DTL, TTL, RTL	(3)	.035
SPDT	2	IH5043	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, PMOS, CMOS	(3)	.035
		IH5051	CMOS	35	1.0	0.25	0.15	DTL, TTL, RTL, PMOS, CMOS	(3)	.035
		IH5143	CMOS	50	0.1	0.175	0.125	TTL, CMOS	(3)	.035
DPST	1	IH5044	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS, PMOS	hi	.035
		IH5144	CMOS	50	0.1	0.175	0.125	TTL, CMOS	hi	.035
		DG183	N-JFET	10	10.0	0.3	0.25	DTL, TTL, RTL	hi	84
		DG184	N-JFET	30	1.0	0.15	0.13	DTL, TTL, RTL	hi	84
		DG185	N-JFET	75	1.0	0.25	0.13	DTL, TTL, RTL	hi	84
DPST	2	DGM185	CMOS	75	0.1	0.25	0.13	DTL, TTL, RTL	hi	.035
		IH5045	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, PMOS, CMOS	hi	.035
		IH5049	CMOS	35	1.0	0.25	0.15	DTL, TTL, RTL, PMOS, CMOS	hi	.035
		IH5145	CMOS	50	0.1	0.175	0.125	TTL, CMOS	hi	.035
		DG139A	N-JFET	30	1.0	0.4	0.8	DTL, TTL, RTL	(3)	84
		DG142A	N-JFET	80	1.0	0.4	0.8	DTL, TTL, RTL	(3)	84
DPDT	1	DG145A	N-JFET	10	10.0	0.5	1.25	DTL, TTL, RTL	(3)	84
		DG163A	N-JFET	15	10.0	0.5	1.25	DTL, TTL, RTL	(3)	90
		DG164A	N-JFET	50	2.0	0.4	0.8	DTL, TTL, RTL	(3)	90
		IH5046	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL CMOS, PMOS	(3)	.035
4PST	1	IH5047	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL CMOS, PMOS	hi	.035

Multiplexers

Type	No. of Channels	Device No.	Switch Technology	$r_{DS(on)}$ Ω max(1)	$I_{D(off)}$ nA max	t_{on} μs max	t_{off} μs max	Logic Input: Logic Level	Logic Input: Input Type(2)	Power Consumption mW
CMOS	1 of 8	IH6108	CMOS	300	0.1	1.5	1.0	DTL, TTL, RTL, CMOS	hi	4.5
CMOS	1 of 16	IH6116	CMOS	600	0.2	1.5	1.0	DTL, TTL, RTL, CMOS	hi	4.5
CMOS	2 of 8	IH6208	CMOS	300	0.1	1.5	1.0	DTL, TTL, RTL, CMOS	hi	4.5
CMOS	2 of 16	IH6216	CMOS	600	0.2	1.5	1.0	DTL, TTL, RTL, CMOS	hi	4.5
CMOS Fault	1 of 8	IH5108	CMOS	700	0.1	1.5	1.0	DTL, TTL, RTL, CMOS	hi	4.5
Protected	2 of 8	IH5208	CMOS	700	0.1	1.5	1.0	DTL, TTL, RTL, CMOS	hi	4.5

Drivers for FET Switches

Electrical Characteristics @ +25°C—Military Temperature Devices

No. of Channels	Device No.	V_{OUT} Positive Volts	V_{OUT} Negative Volts	t_{on} ns max	t_{off} ns max	I_{INL} μA (max)	I_{INH} mA (max)	Logic Input Level	Power Consumption (mW)
2	IH6201	+14.0	-14.0	200	300	1.0	1.0	TTL	350
4	D129	V_{supply}	-19.3	250	1000	200	0.25μA	TTL/DTL	55
6	D123	V_{supply}	-19.7	250	600	1.0	1.0μA	TTL/DTL	20
	D125	V_{supply}	-19.7	250	600	1.0	1.5μA	TTL	50

RF/VIDEO SWITCH

Type	No. of Channels	Device No.	$r_{DS(ON)}$ Ω Max.	Off Isolation	Logic Input	Power Consumption (mW)
CMOS	2	IH5341	75	>60dB @ 10 MHz	TTL, CMOS	0.030

Notes:
1. Switch Resistance under worst case analog voltage.
2. Positive logic LO ("0") or HI ("1") voltage at driver input necessary to turn switch on.
3. Logic "0" or "1" can be arbitrarily assigned for double-throw switches.
4. Switch resistance under best case analog voltage.

INTERSIL

Counters, Timers and Display Drivers

Part Number	Circuit Description	Package	Crystal Frequency	Output
ICM7207 ICM7207A	Frequency counter timebase.	14-Pin DIP 14-Pin DIP	6.5536 MHz 5.2488 MHz	0.01, 0.1, or 1-second count window plus store, reset and MUX.
ICM7208	7-digit unit counter. With addition of 7207 the circuit becomes a complete timer-frequency counter.	28-Pin DIP	—	LED display drive
ICM7211 ICM7212	Four-digit display decoder drivers; ICM7211 is LCD; ICM7212 is LED; Non-multiplexed for low noise, BCD input, decoded display drive output.	40-Pin DIP (plastic)	—	Four-digit, seven-segment direct display drive; LED or LCD
ICM7216 ICM7226	Eight-digit universal counter measures frequency, period, frequency ratio, time interval, units; on-board time base.	28-Pin DIP 40-Pin DIP (Cerdip or plastic)	1 or 10 MHz	Eight-digit-common anode or common cathode direct LED drive; BCD output
ICM7217 ICM7227	Four-digit CMOS up/down counter; presettable start/count and compare register; for hard-wired or microprocessor control applications; cascadable.	28-Pin Cerdip or plastic	—	Four-digit, seven-segment common anode or common cathode direct LED display drive; equal, zero, carry/borrow
ICM7218A/D ICM7218E	LED display driver system with 8x8 memory; numeric or dot (1 of 64) decoding; microprocessor compatible.	28-Pin DIP 40-Pin DIP (Cerdip or plastic)	—	Eight-digit, seven-segment plus decimal point; common cathode or common anode
ICM7224 ICM7225	4½-digit high speed counter/decoder/driver, 25 MHz typ; ICM7224 is LCD, ICM7225 is LED; direct display drive, cascadable.	40-Pin DIP (plastic)	—	4½-digit seven-segment direct display driver; LED or LCD
ICM7231	8-digit CMOS multiplexed LCD driver. Parallel input.	40-Pin DIP (plastic)	—	Eight-digit, seven-segment plus two flags per digit
ICM7232	10½-digit CMOS multiplexed LCD driver. Serial input.	40-Pin DIP (plastic)	—	10½-digit, seven-segment plus two flags per digit
ICM7233	4-character CMOS multiplexed LCD driver. Parallel alphanumeric (6-bit ASCII) input.	40-Pin DIP (plastic)	—	Four-character, 16-segment plus colon
ICM7234	5-character CMOS multiplexed LCD driver. Serial alphanumeric (6-bit ASCII) input.	40-Pin DIP (plastic)	—	Five-character, 16-segment plus colon
ICM7235/A	4-digit CMOS decoder/driver for direct drive vacuum fluorescent displays. BCD input.	40-Pin DIP (plastic)	—	Four-digit, seven-segment, vacuum fluorescent display drive; either HEX or CODE B
ICM7235M/AM	Same as above but microprocessor compatible.			
ICM7236	4½-digit high speed CMOS counter/decoder/driver for vacuum fluorescent displays; 25 MHz typ. counting speed.	40-Pin DIP (plastic)	—	4½-digit, seven-segment, vacuum fluorescent display drive
ICM7236A	Same as above but counting to 15959.	40-Pin DIP (plastic)	—	4½-digit, seven-segment, vacuum fluorescent display drive
ICM7240 ICM7250 ICM7260	Programmable CMOS counter/timers using external RC time base. Programmable from µs to years.	16-Pin DIP	External	Timed output
ICM7242	Fixed CMOS counter/timer. Uses external RC time base; sequence timing from µs to minutes.	8-Pin DIP	External	Timed output
ICM7243	8-character multiplexed LED display driver with alphanumeric (6-bit ASCII) input.	40-Pin Cerdip	—	Eight-character, 14/16-segment common cathode alphanumeric LED display drive
ICM7281	LCD Dot Matrix Column Driver	40-Pin DIP	—	Up to 256 x 256 dots
ICM7555 ICM7556	Single or dual CMOS version of industry-standard 555 timer; 80 µA typ. supply current; 500 kHz guaranteed; 2-18V power supply.	8-Pin DIP 14-Pin DIP	—	

INTERSIL

ADC0801–ADC0804
8-Bit Microprocessor Compatible A/D Converters

FEATURES

- MCS-48 and MCS-80/85 bus compatible–no interfacing logic required
- Conversion time < 100μs
- Easy interface to all microprocessors
- Will operate "stand alone"
- Differential analog voltage inputs
- Works with bandgap voltage references
- TTL compatible inputs and outputs
- On-chip clock generator
- 0V to 5V analog voltage input range (single +5V supply)
- No zero-adjust required

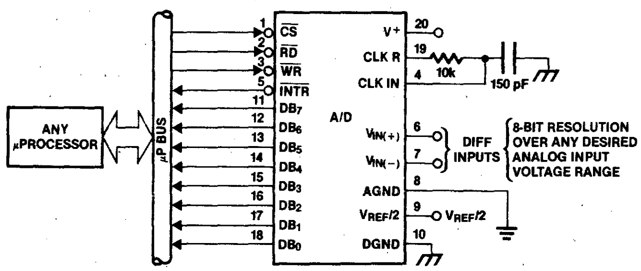
GENERAL DESCRIPTION

The ADC0801 family are CMOS 8-bit successive approximation A/D converters which use a modified potentiometric ladder, and are designed to operate with the 8080A control bus via three-state outputs. These converters appear to the processor as memory locations or I/O ports, hence no interfacing logic is required.

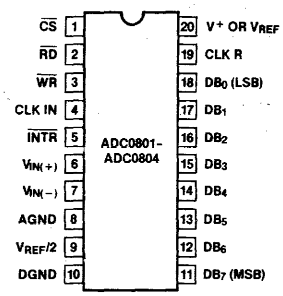
The differential analog voltage input has good common-mode-rejection, and permits offsetting the analog zero-input-voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

The ADC0801 family is available in the industry standard 20 pin CERDIP package.

TYPICAL APPLICATION



PIN CONFIGURATION



TOP VIEW

(Outline dwg. JP)

ORDERING INFORMATION

PART	ERROR	TEMPERATURE RANGE	PACKAGE	ORDER NUMBER
ADC0801	± 1/4 bit adjusted full-scale	0°C to +70°C	20 pin CERDIP	ADC0801LCN
		−40°C to +85°C	20 pin CERDIP	ADC0801LCD
		−55°C to +125°C	20 pin CERDIP	ADC0801LD
ADC0802	± 1/2 bit no adjust	0°C to +70°C	20 pin CERDIP	ADC0802LCN
		−40°C to +85°C	20 pin CERDIP	ADC0802LCD
		−55°C to +125°C	20 pin CERDIP	ADC0802LD
ADC0803	± 1/2 bit adjusted full-scale	0°C to +70°C	20 pin CERDIP	ADC0803LCN
		−40°C to +85°C	20 pin CERDIP	ADC0803LCD
		−55°C to +125°C	20 pin CERDIP	ADC0803LD
ADC0804	± 1 bit no adjust	0°C to +70°C	20 pin CERDIP	ADC0804LCN
		−40°C to +85°C	20 pin CERDIP	ADC0804LCD

ADC0801 – ADC0804

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6.5V
Voltage at Any Input . . . . $-0.3V$ to $(V^+ + 0.3V)$
Storage Temperature Range . . . . $-65°C$ to $+150°C$
Package Dissipation at $T_A = +25°C$ . . . . 875 mW
Lead Temperature (Soldering, 10 seconds) . . . . 300°C

OPERATING RATINGS

Temperature Range
ADC0801/02/03LD . . . . $-55°C$ to $+125°C$
ADC0801/02/03/04LCD . . . . $-40°C$ to $+85°C$
ADC0801/02/03/04LCN . . . . 0°C to +70°C
Supply Voltage Range . . . . 4.5V to 6.3V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SYSTEM ELECTRICAL CHARACTERISTICS (Notes 1 and 7)

Converter Specifications: $V^+ = 5V$, $V_{REF}/2 = 2.500V$, $T_{MIN} \le T_A \le T_{MAX}$ and $f_{CLK} = 640kHz$ unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC0801: Total Adjusted Error	With Full Scale Adjust			±1/4	LSB
ADC0802: Total Unadjusted Error	Completely Unadjusted			±1/2	LSB
ADC0803: Total Adjusted Error	With Full Scale Adjust			±1/2	LSB
ADC0804: Total Unadjusted Error	Completely Unadjusted			±1	LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	1.0	1.3		kΩ
Analog Input Voltage Range	(Note 2)	GND – 0.05		$V^+ + 0.05$	V
DC Common-Mode Rejection	Over Analog Input Voltage Range		±1/16	±1/8	LSB
Power Supply Sensitivity	$V^+ = 5V \pm 10\%$ Over Allowed Input Voltage Range		±1/16	±1/8	LSB

AC ELECTRICAL CHARACTERISTICS

Timing Specifications: $V^+ = 5V$ and $T_A = +25°C$ unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Clock Frequency	f_{CLK}	$V^+ = 6V$ (Note 3) $V^+ = 5V$	100 100	640 640	1280 800	kHz kHz
Clock Periods per Conversion (Note 4)	t_{conv}		66		73	
Conversion Rate In Free-Running Mode	CR	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS} = 0V$, $f_{CLK} = 640kHz$			8888	conv/s
Width of $\overline{WR}$ Input (Start Pulse Width)	$t_{W(\overline{WR})I}$	$\overline{CS} = 0V$ (Note 5)	100			ns
Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	t_{acc}	$C_L = 100pF$ (Use Bus Driver IC for Larger C_L)		135	200	ns
3-State Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	t_{1h}, t_{0h}	$C_L = 10pF$, $R_L = 10k$ (See **3-State Test Circuits**)		125	250	ns
Delay from Falling Edge of $\overline{WR}$ to Reset of $\overline{INTR}$	t_{WI}, t_{RI}			300	450	ns
Input Capacitance of Logic Control Inputs	C_{IN}			5	7.5	pF
3-State Output Capacitance (Data Buffers)	C_{OUT}			5	7.5	pF

ICL7106/7107

3½-Digit Single Chip A/D Converter

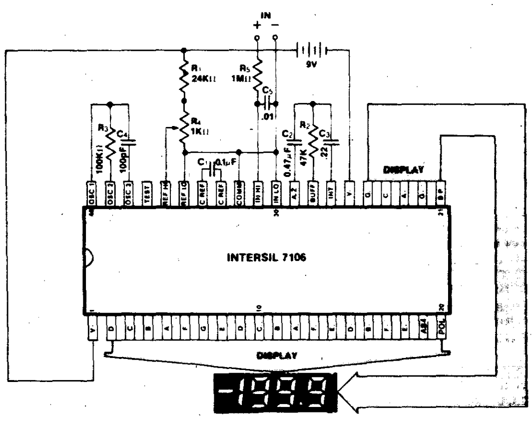
FEATURES

- **Guaranteed zero reading for 0 volts input on all scales.**
- **True polarity at zero for precise null detection.**
- **1 pA typical input current.**
- **True differential input and reference.**
- **Direct display drive - no external components required. — LCD ICL7106**
  — LED ICL7107
- **Low noise - less than 15μV p-p.**
- **On-chip clock and reference.**
- **Low power dissipation - typically less than 10mW.**
- **No additional active circuits required.**
- **Evaluation Kit available.**

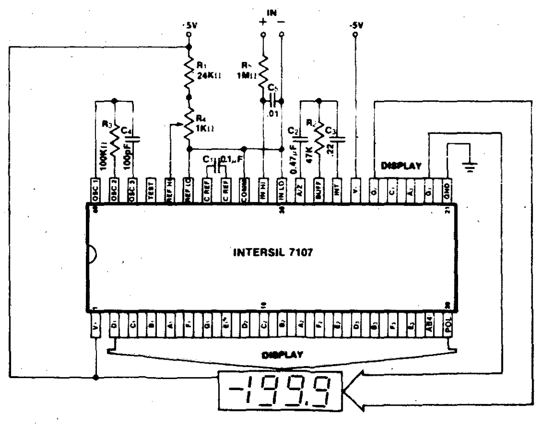
GENERAL DESCRIPTION

The Intersil ICL7106 and 7107 are high performance, low power 3½-digit A/D converters containing all the necessary active devices on a single CMOS I.C. Included are seven-segment decoders, display drivers, reference, and a clock. The 7106 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive; the 7107 will directly drive an instrument-size light emitting diode (LED) display.

The 7106 and 7107 bring together an unprecedented combination of high accuracy, versatility, and true economy. High accuracy like auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10 pA max., and roll-over error of less than one count. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of single power supply operation (7106), enabling a high performance panel meter to be built with the addition of only 7 passive components and a display.



ICL7106 with Liquid Crystal Display

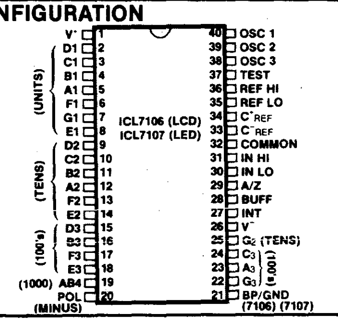


ICL7107 with LED Display

ORDERING INFORMATION

Part	Package	Temp. Range	Order Part #
7106	40 pin ceramic DIP	0°C to +70°C	ICL7106CDL
7106	40 pin plastic DIP	0°C to +70°C	ICL7106CPL
7106	40 pin CERDIP	0°C to +70°C	ICL7106CJL
7107	40 pin CERDIP	0°C to +70°C	ICL7107CJL
7107	40 pin ceramic DIP	0°C to +70°C	ICL7107CDL
7107	40 pin plastic DIP	0°C to +70°C	ICL7107CPL
7106 Kit 7107 Kit	Evaluation kits contain IC, display, circuit board, passive components and hardware.		ICL7106EV/Kit ICL7107EV/Kit

PIN CONFIGURATION



INTERSIL

ICL7109 12 Bit Binary A/D Converter for Microprocessor Interfaces

FEATURES

- **12 bit binary (plus polarity and overrange) dual slope integrating analog-to-digital converter.**
- **Byte-organized TTL-compatible three-state outputs and UART handshake mode for simple parallel or serial interfacing to microprocessor systems.**
- **RUN/HOLD input and STATUS output can be used to monitor and control conversion timing.**
- **True differential input and differential reference.**
- **Low noise — typically 15μV p-p.**
- **1pA typical input current.**
- **Operates at up to 30 conversions per second.**
- **On-chip oscillator operates with inexpensive 3.58MHz TV crystal giving 7.5 conversions per second for 60Hz rejection. May also be operated as RC oscillator for other clock frequencies.**
- **Fabricated using MAX-CMOS™ technology combining analog and digital functions on a single low power LSI CMOS chip.**
- **All inputs fully protected against static discharge; no special handling precautions necessary.**

GENERAL DESCRIPTION

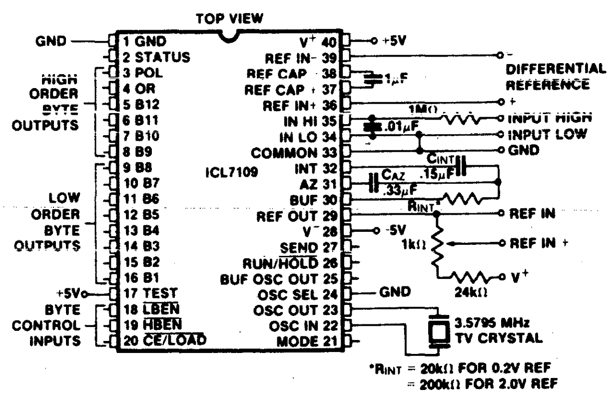
The ICL7109 is a high performance, low power integrating A/D converter designed to easily interface with microprocessors.

The output data (12 bits, polarity and overrange) may be directly accessed under control of two byte enable inputs and a chip select input for a simple parallel bus interface. A UART handshake mode is provided to allow the ICL7109 to work with industry-standard UARTs in providing serial data transmission, ideal for remote data logging applications. The RUN/HOLD input and STATUS output allow monitoring and control of conversion timing.

The ICL7109 provides the user with the high accuracy, low noise, low drift, versatility and economy of the dual-slope integrating A/D converter. Features like true differential input and reference, drift of less than 1μV/°C, maximum input bias current of 10pA, and typical power consumption of 20mW make the ICL7109 an attractive per-channel alternative to analog multiplexing for many data acquisition applications.

PIN CONFIGURATION AND TEST CIRCUIT:

(See Figure 1 for typical connection to a UART or Microcomputer)



(OUTLINE DWGS DL, JL, PL)

ORDERING INFORMATION

Part	Temp. Range	Package	Order Number
7109	−55°C to +125°C	40-Pin Ceramic DIP	ICL7109MDL
7109	−20°C to +85°C	40-Pin Ceramic DIP	ICL7109IDL
7109	−20°C to +85°C	40-Pin CERDIP	ICL7109IJL
7109	0°C to 70°C	40-Pin Plastic DIP	ICL7109CPL

INTERSIL

ICL7115

Fast CMOS Monolithic 14-Bit A/D Converter

FEATURES

- **14-bit linearity and resolution (0.003%)**
- **No missing codes**
- **Microprocessor compatible byte-organized buffered outputs**
- **Fast conversion (40μs)**
- **Auto-zeroed comparator for low offset voltage**
- **Low linearity and gain tempco (1ppm/°C, 4ppm/°C)**
- **Low power consumption (60mW)**
- **No gain or offset adjustment necessary (0.006% FS)**
- **Provides 3% useable overrange**
- **FORCE/SENSE and separate digital and analog ground pins for increased system accuracy**

GENERAL DESCRIPTION

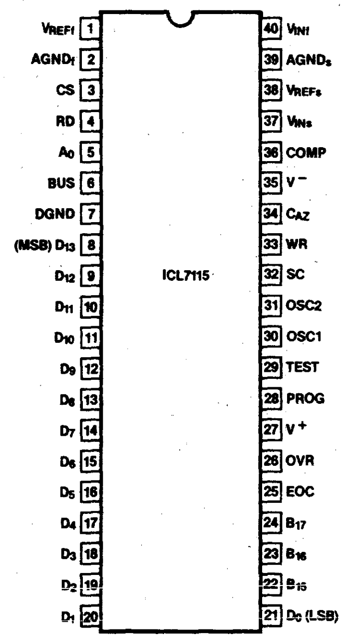
The ICL7115 is the first monolithic 14-bit accurate, fast successive approximation A/D converter. It uses thin film resistors and CMOS circuitry with an on-chip PROM calibration table circuit to achieve 14-bit linearity without laser trimming. Special design techniques used in the DAC and comparator result in high speed, while the fully static silicon-gate CMOS circuitry keeps the power dissipation very low.

Microprocessor bus interfacing is made easy by the use of standard WRite and ReaD cycle timing and control signals, combined with Chip Select and Address pins. The digital output pins are byte-organized and three-state gated for bus interface to 8, 12, and 16-bit systems.

The ICL7115 provides separate Analog and Digital grounds. Analog ground, voltage reference and input voltage pins are separated into force and sense lines for increased system accuracy. Operating with ±5V supplies, the ICL7115 accepts 0V to +5V input with a −5V reference or 0V to −5V input with a +5V reference.

The ICL7115 is available in several versions with different accuracies, temperature ranges and packages. A Leadless Chip Carrier (LCC) package is also available; consult factory.

PIN CONFIGURATION (outline dwg JL)



ORDERING INFORMATION

ACCURACY	PACKAGE	TEMPERATURE	PART NUMBER
0.01%	40-Pin CERDIP	0°C to +70°C	ICL7115JCJL
0.01%	40-Pin CERDIP	−25°C to +85°C	ICL7115JIJL
0.01%	LCC	—	—
0.006%	40-Pin CERDIP	0°C to +70°C	ICL7115KCJL
0.006%	40-Pin CERDIP	−25°C to +85°C	ICL7115KIJL
0.006%	LCC	—	—
0.003%	40-Pin CERDIP	0°C to +70°C	ICL7115LCJL
0.003%	40-Pin CERDIP	−25°C to +85°C	ICL7115LIJL
0.003%	LCC	—	—

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage V^+ to DGND . . . . −0.3V to +6.5V
Supply Voltage V^- to DGND . . . . +0.3V to −6.5V
V_{REFs}, V_{REFf}, V_{INs}, V_{INf} to DGND . . . . +25V to −25V
$AGND_s$, $AGND_f$ to DGND . . . . +1V to −1V
Current in FORCE and SENSE Lines 25mA
Digital I/O Pin Voltages . . . . −0.3V to V^+ +0.3V
PROG to DGND Voltage . . . . V^- to V^+ +0.3V

Operating Temperature Range
ICL7115XCXX . . . . 0°C to +70°C
ICL7115XIXX . . . . −25°C to +85°C
Storage Temperature Range . . . . −65°C to +150°C
Power Dissipation 500mW
derate above 70°C @ 100mW/°C
Lead Temperature (Soldering, 10 sec) . . . . 300°C

Note 1: All voltages with respect to DGND, unless otherwise noted.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

$V^+ = +5.0V$, $V^- = -5.0V$, $V_{REFs} = +5.0V$, $T_A = +25°C$ unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Resolution		$\overline{SC}$ = High $\overline{SC}$ = Low	14 12			Bits
Total Unadjusted Error					1	LSB
Differential Non-Linearity		Full Operating Temperature Range		1/2		LSB
Overall Accuracy (Note 3)		ICL7115J ICL7115K ICL7115L			0.01 0.006 0.003	% FSR
Full-Scale Error		$T_A = +25°C$ Operating Temperature Range (Note 2)		1/2 1	1 4	LSB ppm/°C
Zero Error		$T_A = +25°C$ Operating Temperature Range (Note 2)			1/8 4	LSB ppm/°C
Power Supply Rejection	PSRR	$T_A = +25°C$ Full Operating Temperature Range		1/16	1/8	LSB
V_{INs}, V_{REFs} Resistance	Z_{IN}, Z_{REF}	(Note 4) Operating Temperature Range	3	5 −300	7	kΩ ppm/°C
Low State Input Voltage	V_{il}	Operating Temperature Range			0.8	V
High State Input Voltage	V_{ih}	Operating Temperature Range	2.4			V
Logic Input Current	I_{lin}	$0 < V_{IN} < V^+$		1	10	μA
Low State Output Voltage	V_{ol}	$I_{OUT} = 3.2mA$ Operating Temperature Range			0.4	V
High State Output Voltage	V_{oh}	$I_{OUT} = -200\mu A$ Operating Temperature Range	2.8			V
Three-State Output Current	I_{ox}	$0 < V_{OUT} < V^+$		1		μA
Logic Input Capacitance	C_{in}	(Note 2)		15		pF
Logic Output Capacitance	C_{out}	Three-State (Note 2)		15		pF
Supply Voltage Range	V^+	Functional Operation	4.5		6.0	V
	V^-		−4.5		−6.0	V
Supply Current	I^+	Excluding Ladder Current		5		mA
	I^-	$F_{CLK} = 1kHz$		5		mA

Note 2: Assumes all leads soldered or welded to printed circuit board.
Note 3: Full-scale range (FSR) is 10V (+5V to −5V).
Note 4: Guaranteed by design, not 100% tested in production.

INTERSIL

PRELIMINARY
Specifications Subject to Change Without Notice

ICL7129

4½-Digit Single-Chip A/D Converter

FEATURES

- ±19,999 count A/D converter accurate to ±1 count
- 10μV resolution on 200mV scale
- 110dB CMRR
- Direct LCD display drive
- True differential input and reference
- Low power consumption
- Decimal point drive outputs
- Overrange and underrange outputs
- Low battery detection and indication
- 10:1 range change input

ORDERING INFORMATION

PART	PACKAGE	TEMPERATURE	ORDER NUMBER
7129	40-Pin CERDIP	0°C to +70°C	ICL7129CJL
7129	40-Pin Plastic	0°C to +70°C	ICL7129CPL
7129	40-Pin Plastic	0°C to +70°C	ICL7129RCPL
7129	Dice	0°C to +70°C	ICL7129C/D
7129	Flat Pack		

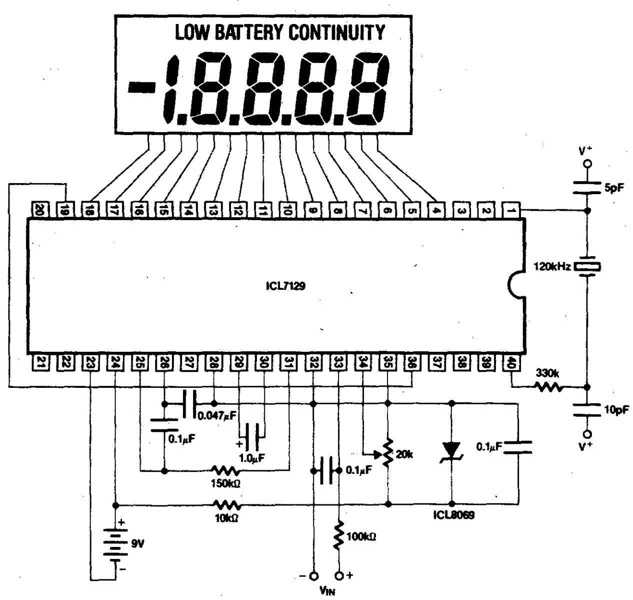
GENERAL DESCRIPTION

The Intersil ICL7129 is a very high-performance 4½-digit analog-to-digital converter that directly drives a multiplexed liquid crystal display. This single-chip CMOS integrated circuit requires only a few passive components and a reference to operate. And it is ideal for high-resolution hand-held digital multimeter applications.

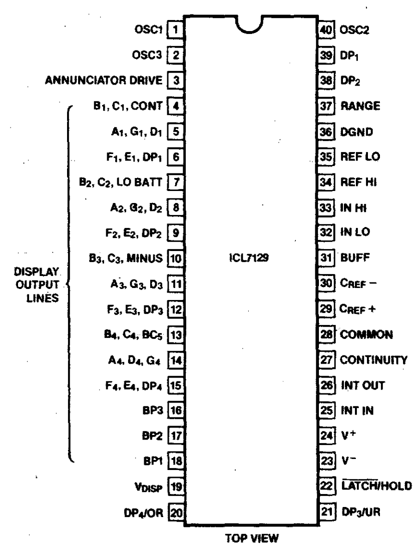
The performance of the ICL7129 has not been equaled before in a single-chip A/D converter. The successive integration technique used in the ICL7129 results in accuracy better than 0.005% of full-scale and resolution down to 10μV/count.

The ICL7129, drawing only 1mA from a 9V battery, is well suited for battery powered instruments. Provision has been made for the detection and indication of a "LOW BATTERY" condition. Autoranging instruments can be made with the ICL7129 which provides overrange and underrange outputs and 10:1 range changing input. The ICL7129 instantly checks for continuity, giving both a visual indication and a logic level output which can enable an external audible signal. These features and the high performance of the ICL7129 make it an extremely versatile and accurate instrument-on-a-chip.

TYPICAL APPLICATION



PIN CONFIGURATION (outline dwg JL, PL)



ICL7129

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Supply Voltages (V^+ to V^-) 15V
Reference Voltage (REF HI or REF LO) .... V^+ to V^-
Input Voltage (Note 1)
(IN HI or IN LO) .... V^+ to V^-
V_{DISP} .... V^+ to DGND − 0.3V
Digital Input Pins
1, 2, 19, 20, 21, 22, 27,
37, 38, 39, 40 .... DGND to V^+

Power Dissipation (Note 2)
CERDIP package 1000mW
Plastic package 800mW
Operating Temperature .... 0°C to +70°C
Storage Temperature .... −65°C to +160°C
Lead Soldering Temperature .... 300°C

Note 1: Input voltages may exceed the supply voltages provided that input current is limited to ± 400μA. Currents above this value may result in invalid display readings but will not destroy the device if limited to ± 1mA.

Note 2: Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS V^+ to V^- = 9V, V_{REF} = 1.00V. T_A = +25°C, f_{CLK} = 120kHz, unless otherwise noted.

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNIT
Zero Input Reading	V_{IN} = 0V 200mV Scale	−0000	0000	+0000	Reading
Zero Reading Drift	V_{IN} = 0V 0°C < T_A < +70°C		±0.5		μV/°C
Ratiometric Reading	V_{IN} = V_{REF} = 1000mV RANGE = 2V	9998	9999	10000	Reading
Range Change Accuracy	V_{IN} = 0.10000V on Low Range ÷ V_{IN} = 1.0000V on High Range	0.9999	1.0000	1.0001	Ratio
Rollover Error	$-V_{IN} = +V_{IN}$ = 199mV		0.5	1.0	Counts
Linearity Error	200mV Scale		0.5		Counts
Input Common-Mode Rejection Ratio	V_{CM} = 1.0V, V_{IN} = 0V 200mV Scale		110		dB
Input Common-Mode Voltage Range	V_{IN} = 0V 200mV Scale	$(V^-) + 1.5$		$(V^+) - 0.5$	V
Noise (p-p Value not Exceeding 95% of Time)	V_{IN} = 0V 200mV Scale		7.0		μV
Input Leakage Current	V_{IN} = 0V, Pin 32, 33		1	10	pA
Scale Factor Tempco	V_{IN} = 199mV 0°C < T_A < +70°C External V_{REF} = 0ppm/°C		2	5	ppm/°C
COMMON Voltage	V^+ to Pin 28	2.8	3.2	3.5	V
COMMON Sink Current	ΔCommon = +0.1V		0.6		mA
COMMON Source Current	ΔCommon = −0.1V		12		μA
DGND Voltage	V^+ to Pin 36 V^+ to V^- = 9V	4.5	5.3	5.8	V
DGND Sink Current	ΔDGND = +0.5V		1.2		mA
Supply Voltage Range	V^+ to V^-	6	9	14	V
Supply Current Excluding COMMON Current	V^+ to V^- = 9V		1.0	1.4	mA
Clock Frequency			120	360	kHz
Display Multiplex Rate	f_{CLK} = 120kHz		100		Hz
V_{DISP} Resistance	V_{DISP} to V^+		50		kΩ

INTERSIL

ICL7134

14-Bit μP-Compatible Multiplying D/A Converter

FEATURES

- **14-bit linearity (0.003% FSR)**
- **No gain adjustment necessary**
- **Microprocessor-compatible with double buffered inputs**
- **Bipolar application requires no extra adjustments or external resistors**
- **Output current settling-time 3μs max (0.9μs typ)**
- **Low linearity and gain temperature coefficients**
- **Low power dissipation**
- **Full four-quadrant multiplication**
- **Full temperature range operation**

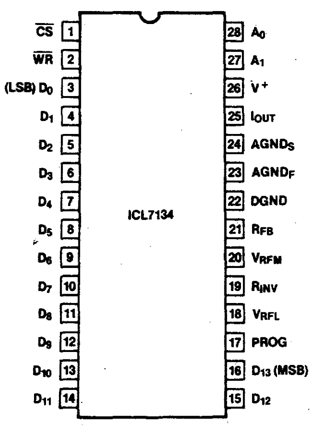
GENERAL DESCRIPTION

The ICL7134 combines a four-quadrant multiplying DAC using thin film resistors and CMOS circuitry with an on-chip PROM-controlled correction circuit to achieve true 14-bit linearity without laser trimming.

Microprocessor bus interfacing is eased by standard memory WRite cycle timing and control signal use. Two input buffer registers are separately loaded with the 8 least significant bits (LS register) and the 6 most significant bits (MS register). Their contents are then transferred to the 14-bit DAC register, which controls the output switches. The DAC register can also be loaded directly from the data inputs, in which case the registers are transparent.

The ICL7134 is supplied in two versions. The ICL7134U is programmed for unipolar operation while the ICL7134B is programmed for bipolar applications. The V_{REF} input to the most significant bit of the DAC is separated from the reference input to the remainder of the ladder. For unipolar use, the two reference inputs are tied together, while for bipolar operation, the polarity of the MSB reference is reversed, giving the DAC a true 2's complement input transfer function. Two resistors which facilitate the reference inversion are included on the chip, so only an external op-amp is needed. The PROM is coded to correct for errors in these resistors as well as the inversion of the MSB.

PIN CONFIGURATION



(outline dwg JI)

ORDERING INFORMATION

NON-LINEARITY	TEMPERATURE RANGE		
	0°C to +70°C	−25°C to +85°C	−55°C to +125°C
Bipolar Versions			
0.01% (12-bit)	ICL7134BJCJI	ICL7134BJIJI	ICL7134BJMJI
0.006% (13-bit)	ICL7134BKCJI	ICL7134BKIJI	ICL7134BKMJI
0.003% (14-bit)	ICL7134BLCJI	ICL7134BLIJI	ICL7134BLMJI
Unipolar Versions			
0.01% (12-bit)	ICL7134UJCJI	ICL7134UJIJI	ICL7134UJMJI
0.006% (13-bit)	ICL7134UKCJI	ICL7134UKIJI	ICL7134UKMJI
0.003% (14-bit)	ICL7134ULCJI	ICL7134ULIJI	ICL7134ULMJI

Package: 28-pin CERDIP only

ICL7134

INTERSIL

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V^+ to DGND) .... $-0.3V$ to $7.5V$
V_{RFL}, V_{RFM}, R_{INV}, R_{FB} to DGND .... ±25V
I_{OUT}, $AGND_F$, $AGND_S$ .... $-0.1V$ to V^+
Current in $AGND_S$, $AGND_F$ 25mA
An, Dn, $\overline{WR}$, $\overline{CS}$, PROG .... $-0.3V$ to $V^+ + 0.3V$
Operating Temperature Range
ICL7134XXC .... 0°C to +70°C
ICL7134XXI .... −20°C to +85°C
ICL7134XXM .... −55°C to +125°C

Storage Temperature Range .... −65°C to +150°C
Power Dissipation (Note 2) 500mW
Derate Linearly Above 70°C @ 10mW/°C
Lead Temperature (Soldering, 10 seconds) .... 300°C

Note 1: All voltages with respect to DGND.
Note 2: Assumes all leads soldered or welded to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS ($V^+ = 5V$, $V_{REF} = 10V$, $T_A = +25°C$ unless otherwise specified.)

PARAMETER		SYMBOL	TEST CONDITIONS	LIMITS			UNIT
				MIN	TYP	MAX	
Resolution				14			Bits
Non-Linearity	J		Test Figure 1			0.010	% FSR
	K		(Notes 1 and 2)			0.006	% FSR
	L					0.003	% FSR
Non-Linearity Temperature Coefficient			Operating Temperature Range		1	2	ppm/°C
Gain Error	J		Test Figure 1			0.020	% FSR
	K		(Notes 1 and 2)			0.012	% FSR
	L					0.006	% FSR
Gain Error Temperature Coefficient					2	8	ppm/°C
Monotonicity	J			14			Bits
	K			14			Bits
	L			14			Bits
I_{OUT} Leakage Current		I_{OLK}	$T_A = +25°C$			10	nA
			Operating Temperature Range		50		
Power Supply Rejection		PSRR	$T_A = +25°C$, $\Delta V^+ = \pm 10\%$		1	50	ppm/V
			Operating Temperature Range			100	
Output Current Settling Time					0.9	3	μs
Feedthrough Error	ICL7134U		$V_{REF} = \pm 10V$, 2kHz Sinewave		250		μVp-p
	ICL7134B				500		
Reference Input Resistance		Z_{REF}	$V_{RFL} = V_{RFM}$ (Unipolar Mode)	4.0		10	kΩ
Output Capacitance		C_{OUT}	DAC Register = All 0's		160		pF
			DAC Register = All 1's		235		
Output Noise			Equivalent Johnson Res.		7		kΩ
Low State Input		V_{INL}	Operating Temperature Range			0.8	V
High State Input		V_{INH}	Operating Temperature Range	2.4			V
Logic Input Current		I_{lin}	$0 \le V_{IN} \le V^+$			1.0	μA
Logic Input Capacitance		C_{lin}	(Note 3)		15		pF
Supply Voltage Range		V^+	Functional Operation	3.5		6.0	V
Supply Current		I^+	(Excluding Ladder)		0.06	0.5	mA
Long Term Stability			1000 Hours, +125°C (Note 3)		10		ppm/√month

Note 1: Full-Scale Range (FSR) is 10V for unipolar mode, 20V (±10V) for bipolar mode.
Note 2: Using internal feedback and reference inverting resistors.
Note 3: Guaranteed by design, not 100% tested in production.

INTERSIL

ICL7135

Precision 4½ Digit Single Chip A/D Converter

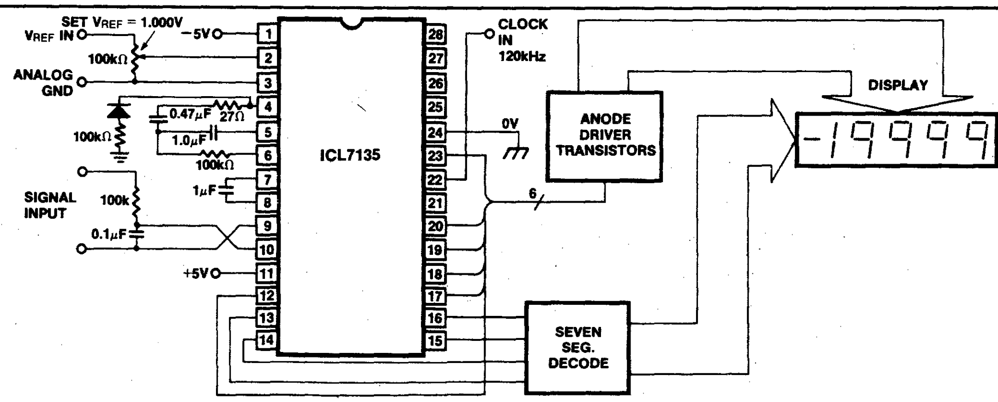
FEATURES

- **Accuracy guaranteed to ±1 count over entire ±20,000 counts (2.0000 volts full scale)**
- **Guaranteed zero reading for 0 volts input**
- **1 pA typical input current**
- **True differential input**
- **True polarity at zero count for precise null detection**
- **Single reference voltage required**
- **Over-range and under-range signals available for auto-ranging capability**
- **All outputs TTL compatible**
- **Blinking display gives visual indication of over-range**
- **Six auxiliary inputs/outputs are available for interfacing to UARTs, microprocessors or other complex circuitry**
- **Multiplexed BCD output versatility**

GENERAL DESCRIPTION

The Intersil ICL7135 precision A/D converter, with its multiplexed BCD output and digit drivers, combines dual-slope conversion reliability with ±1 in 20,000 count accuracy and is ideally suited for the visual display DVM/DPM market. The 2.0000V full scale capability, auto-zero and auto-polarity are combined with true ratiometric operation, almost ideal differential linearity and true differential input. All necessary active devices are contained on a single CMOS I.C., with the exception of display drivers, reference, and a clock.

The Intersil ICL7135 brings together an unprecedented combination of high accuracy, versatility, and true economy. High accuracy like auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10 pA max., and rollover error of less than one count. The versatility of multiplexed BCD outputs is increased by the addition of several pins which allow it to operate in more sophisticated systems. These include STROBE, OVERRANGE, UNDERRANGE, RUN/HOLD and BUSY lines, making it possible to interface the circuit to a microprocessor or UART.

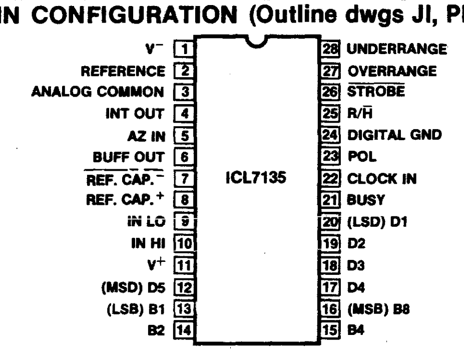


ICL7135 with LED Display

ORDERING INFORMATION

Part	Package	Temp. Range	Order Part #
7135	28-Pin CERDIP	0°C to +70°C	ICL7135CJI
7135	28-Pin Plastic DIP	0°C to +70°C	ICL7135CPI
EV/ KIT	Evaluation Kit (PC Board, active, passive components)		ICL135EV/ KIT

PIN CONFIGURATION (Outline dwgs JI, PI)



ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 2)
Ceramic Package .... 1000 mW
Plastic Package .... 800 mW
Operating Temperature .... 0°C to +70°C
Storage Temperature .... −65°C to +160°C
Lead Temperature (Soldering, 10 sec) .... 300°C

Supply Voltage V^+ .... +6V
V^- .... −9V
Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) .... V^+ to V^-
Clock Input .... Gnd to V^+

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to +100μA.
Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ICL7135 ELECTRICAL CHARACTERISTICS (Note 1)

$V^+ = +5V$, $V^- = -5V$, $T_A = 25°C$, Clock Frequency Set for 3 Reading/Sec

	CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG	Zero Input Reading		$V_{IN} = 0.0V$ Full Scale = 2.000V	−0.0000	±0.0000	+0.0000	Digital Reading
ANALOG	Ratiometric Reading (2)		$V_{IN} \equiv V_{REF}$ Full Scale = 2.000V	+0.9998	+0.9999	+1.0000	Digital Reading
ANALOG	Linearity over ± Full Scale (error of reading from best straight line)		$-2V \leq V_{IN} \leq +2V$		0.5	1	Digital Count Error
	Differential Linearity (difference between worse case step of adjacent counts and ideal step)		$-2V \leq V_{IN} \leq +2V$		.01		LSB
	Rollover error (Difference in reading for equal positive & negative voltage near full scale)		$-V_{IN} \equiv +V_{IN} \approx 2V$		0.5	1	Digital Count Error
(Note 1) (Note 2)	Noise (P-P value not exceeded 95% of time)	e_n	$V_{IN} = 0V$ Full scale = 2.000V		15		μV
	Leakage Current at Input	I_{ILK}	$V_{IN} = 0V$		1	10	pA
	Zero Reading Drift		$V_{IN} = 0V$ $0° \leq T_A \leq 70°C$		0.5	2	μV/°C
	Scale Factor Temperature Coefficient (3)	TC	$V_{IN} = +2V$ $0 \leq T_A \leq 70°C$ (ext. ref. 0 ppm/°C)		2	5	ppm/°C
DIGITAL INPUTS	Clock In, $\overline{Run}$/Hold, See Fig. 2	V_{INH}		2.8	2.2		V
DIGITAL INPUTS		V_{INL}			1.6	0.8	
DIGITAL INPUTS		I_{INL}	$V_{IN} = 0$		0.02	0.1	mA
DIGITAL INPUTS		I_{INH}	$V_{IN} = +5V$		0.1	10	μA
DIGITAL OUTPUTS	All Outputs	V_{OL}	$I_{OL} = 1.6ma$		0.25	0.40	V
DIGITAL OUTPUTS	B_1, B_2, B_4, B_8 D_1, D_2, D_3, D_4, D_5	V_{OH}	$I_{OH} = -1mA$	2.4	4.2		V
DIGITAL OUTPUTS	BUSY, $\overline{STROBE}$, OVER-RANGE, UNDER-RANGE POLARITY	V_{OH}	$I_{OH} = -10\mu A$	4.9	4.99		V
SUPPLY	+5V Supply Range	V^+		+4	+5	+6	V
SUPPLY	−5V Supply Range	V^-		−3	−5	−8	V
SUPPLY	+5V Supply Current	I^+	$f_C = 0$		1.1	3.0	mA
SUPPLY	−5V Supply Current	I^-	$f_C = 0$		0.8	3.0	
SUPPLY	Power Dissipation Capacitance	C_{PD}	vs. Clock Freq		40		pF
Clock	Clock Freq. (Note 4)			DC	2000	1200	kHz

Note 1: Tested in 4-1/2 digit (20,000 count) circuit shown in Fig. 1, clock frequency 120kHz.
Note 2: Tested with a low dielectric absorption integrating capacitor. See Component Selection Section.
Note 3: The temperature range can be extended to +70°C and beyond as long as the auto-zero and reference capacitors are increased to absorb the higher leakage of the ICL7135.
Note 4: This specification relates to the clock frequency range over which the ICL7135 will correctly perform its various functions. See "Max Clock Frequency" below for limitations on the clock frequency range in a system.

INTERSIL

ICL7136

3½-Digit Low Power A/D Converter

FEATURES

- **First-reading recovery from overrange gives immediate "OHMS" measurement**
- **Guaranteed zero reading for 0V input**
- **True polarity at zero for precise null detection**
- **1pA typical input current**
- **True differential input and reference**
- **Direct LCD display drive — no external components required**
- **Pin compatible with the ICL7106, ICL7126**
- **Low noise — 15μVp-p without hysteresis or overrange hangover**
- **On-chip clock and reference**
- **Low power dissipation, guaranteed less than 1mW — gives 8,000 hours typical 9V battery life**
- **No additional active circuits required**
- **Evaluation Kit available (ICL7136EV/Kit)**

GENERAL DESCRIPTION

The Intersil ICL7136 is a high performance, very low power 3½-digit A/D converter. All the necessary active devices are contained on a single CMOS IC, including seven-segment decoders, display drivers, reference, and clock. The 7136 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive. The supply current is under 100μA, ideally suited for 9V battery operation.

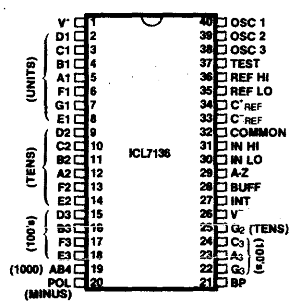
The 7136 brings together an unprecedented combination of high accuracy, versatility, and true economy. High accuracy, like auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10pA max., and rollover error of less than one count. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of single power supply operation allows a high performance panel meter to be built with the addition of only 7 passive components and a display.

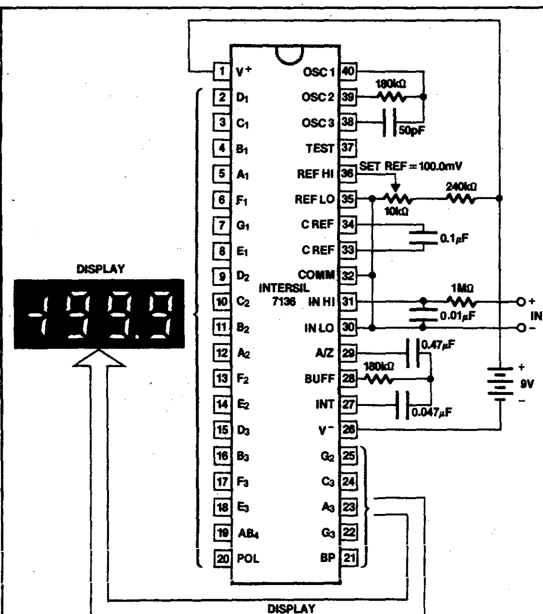
The ICL7136 is an improved version of the ICL7126, eliminating the overrange hangover and hysteresis effects, and should be used in its place in all applications. It can also be used as a plug-in replacement for the ICL7106 in a wide variety of applications, changing only the passive components.

ORDERING INFORMATION

PART	PACKAGE	TEMPERATURE RANGE	ORDER PART NUMBER
7136	40-pin CERDIP	0°C to +70°C	ICL7136CJL
7136	40-pin Ceramic DIP	0°C to +70°C	ICL7136CDL
7136	40-pin Plastic DIP	0°C to +70°C	ICL7136CPL
7136 Kit	Evaluation Kits		ICL7136EV/KIT

PIN CONFIGURATION (Outline dwgs. DL, JL PL)





ICL7136 with Liquid Crystal Display

TYPICAL APPLICATIONS (Continued)

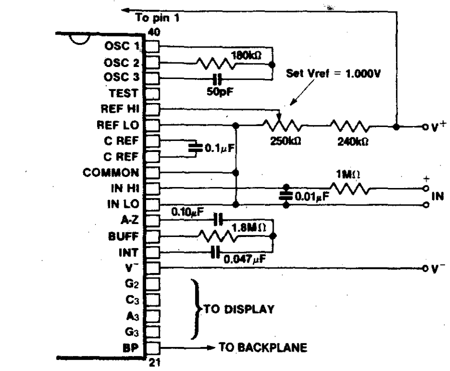


Figure 11. Recommended Component Values for 2.000V Full-Scale, 3 Readings/Sec. For 1 reading/sec, change C_{INT}, R_{OSC} to values of Figure 10.

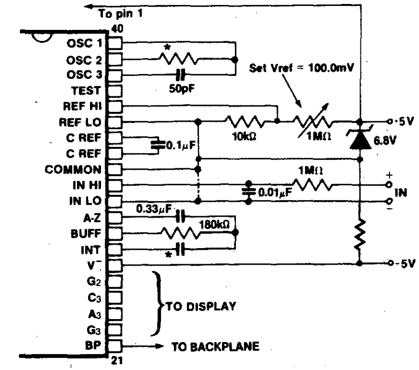


Figure 12. 7136 with Zener Diode Reference. Since low TC zeners have breakdown voltages ~6.8V, diode must be placed across the total supply (10V). As in the case of Figure 11, IN LO may be tied to COMMON.

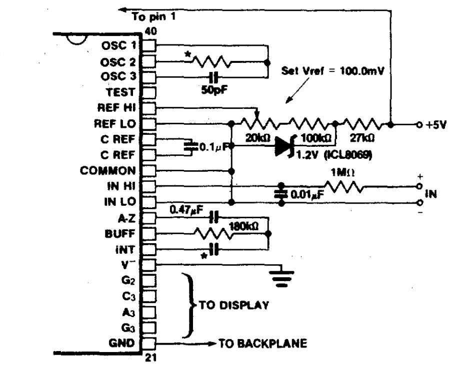


Figure 13. 7136 Operated from Single +5V Supply. An external reference must be used in this application, since the voltage between V^+ and V^- is insufficient for correct operation of the internal reference.

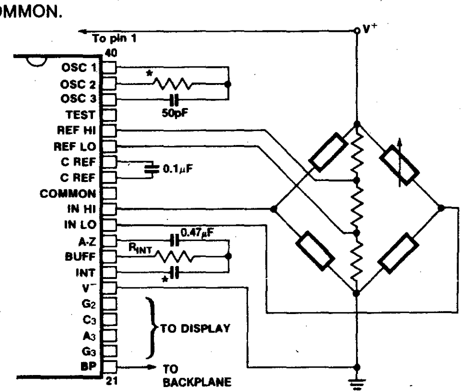


Figure 14. 7136 Measuring Ratiometric Values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.

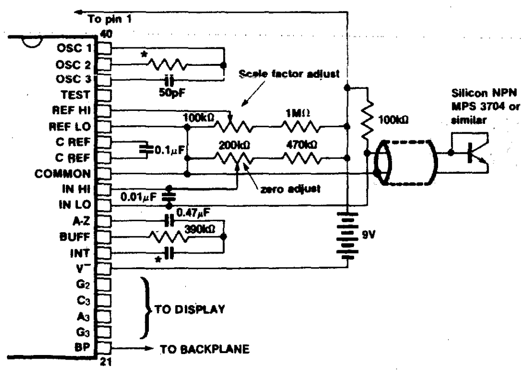


Figure 15. 7136 used as a Digital Centigrade Thermometer. A silicon diode-connected transistor has a temperature coefficient of about −2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for a 100.0 reading. See ICL8073/4 and AD590 data sheets for alternative circuits.

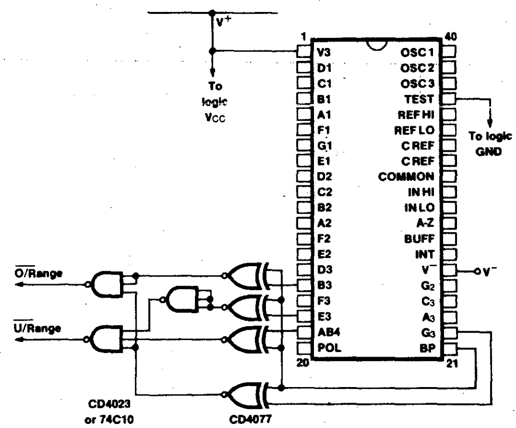


Figure 16. Circuit for Developing Underrange and Overrange Signals from 7136 Outputs.

*Values depend on clock frequency. See Figures 9, 10, 11.

INTERSIL

PRELIMINARY
Specifications Subject To Change Without Notice

ICL7145

16-Bit μP-Compatible Multiplying D/A Converter

FEATURES

- 16-bit resolution
- High linearity—0.003% FSR
- Microprocessor compatible with buffered inputs
- Bipolar application requires no external resistors
- Output current settling time 3μs max (1.0μs typ)
- Low linearity and gain temperature coefficients (1ppm/°C typ)
- Low power dissipation
- Full four-quadrant multiplication
- Full temperature range operation

GENERAL DESCRIPTION

The ICL7145 combines a four-quadrant multiplying DAC using thin film resistors and CMOS circuitry with an on-chip PROM-controlled correction circuit to achieve 0.003% linearity without laser trimming.

Microprocessor bus interfacing is eased by standard memory $\overline{WR}$ite cycle timing and control signal use. The input buffer register is loaded with the 16-bit input, and directly controls the output switches. The register is transparent if $\overline{WR}$ and $\overline{CS}$ are held low.

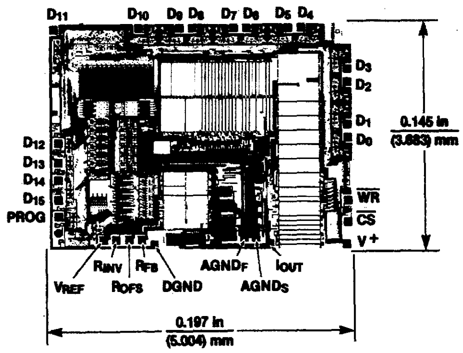
The ICL7145 is designed and programmed for bipolar operation. There is an offset resistor to the output with a reference input which should be connected to $-V_{REF}$, giving the DAC a true 2's complement input transfer function. Two extra resistors to facilitate the reference inversion are included on the chip, so that only an external op amp is needed.

ORDERING INFORMATION

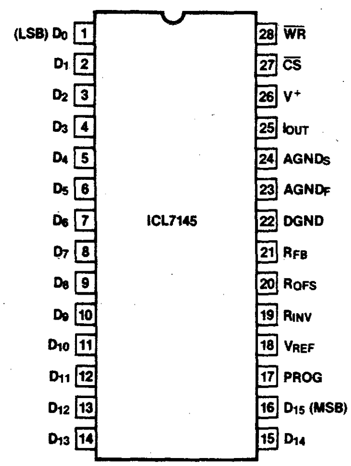
NON-LINEARITY	TEMPERATURE RANGE 0°C TO +70°C	TEMPERATURE RANGE −25°C TO +85°C
0.006%	ICL7145JCJI	ICL7145JIJI
0.003%	ICL7145KCJI	ICL7145KIJI

Package: 28-pin CERDIP only

CHIP TOPOGRAPHY



PIN CONFIGURATION (outline dwg JI)



INTERSIL

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage V^+ to DGND .... −0.3V to 7.5V
V_{REF}, R_{OFS}, R_{INV}, R_{FB} to DGND .... ±25V
Current in $AGND_F$, $AGND_S$ 25mA
D_N, $\overline{WR}$, $\overline{CS}$, PROG, I_{OUT}, $AGND_F$, $AGND_S$ .... −0.3V to V^+ +0.3V
Operating Temperature
ICL7145C .... 0°C to +70°C
ICL7145I .... −25°C to +85°C

Storage Temperature .... −65°C to +150°C
Power Dissipation (Note 2) 500mW
derate above 70°C @ 10mW/°C
Lead Temperature (soldering, 10 seconds) .... 300°C

Note 1: All voltages with respect to DGND.
Note 2: Assumes all leads soldered or welded to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS $V^+ = +5V$, $V_{REF} = +5V$, $T_A = +25°C$ unless otherwise specified.

PARAMETER		SYMBOL	CONDITIONS	LIMITS			UNIT
				MIN	TYP	MAX	
Resolution				16			Bits
Non-Linearity	J		(Notes 3 and 4)			0.006	% FSR
	K					0.003	
Differential Non-Linearity			(Notes 3 and 4)		0.003		% FSR
Non-Linearity Temperature Coefficient			Operating Temperature Range		1		ppm/°C
Gain Error	J		(Notes 3 and 4)			0.04	% FSR
	K					0.02	
Gain Error Temperature Coefficient			Operating Temperature Range		1		ppm/°C
Zero Output Offset		V_{OZ}	$T_A = +25°C$			10	mV
			Operating Temperature Range		10		
Power Supply Rejection Ratio		PSRR	$T_A = +25°C$, $V^+ = 5V \pm 10\%$		1	20	ppm/V
Output Current Settling Time					1	3	μs
Reference Input Resistance		Z_{REF}	V_{REF}	3		6	kΩ
Output Capacitance		C_{OUT}	D_N = All 0s		110		pF
			D_N = All 1s		260		
Output Noise			Equivalent Johnson Resistance		7		kΩ
Low State Input		V_{INl}	Operating Temperature Range			0.8	V
High State Input		V_{INh}	Operating Temperature Range	2.4			
Logic Input Current		I_{LIN}	$0 \le V_{IN} \le V^+$	−1.0		1.0	μA
Logic Input Capacitance		C_{LIN}			15		pF
Supply Voltage Range		V^+	Functional Operation	4.5		5.5	V
Supply Current		I^+	Excluding Ladder		0.5	1.2	mA

Note 3: Full-Scale Range (FSR) is 10V (±5V).
Note 4: Using internal feedback and reference inverting resistors.

AC ELECTRICAL CHARACTERISTICS $V^+ = +5V$, $T_A = +25°C$, see Timing Diagram.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
$\overline{C}$hip $\overline{S}$elect-$\overline{WR}$ite Set-Up Time	t_{CWs}				0	ns
$\overline{C}$hip $\overline{S}$elect-$\overline{WR}$ite Hold Time	t_{CWh}				0	
Write Pulse Width Low	$t_{\overline{WR}}$				200	
Data-$\overline{WR}$ite Set-Up Time	t_{DWs}				200	
Data-$\overline{WR}$ite Hold Time	t_{DWh}				0	

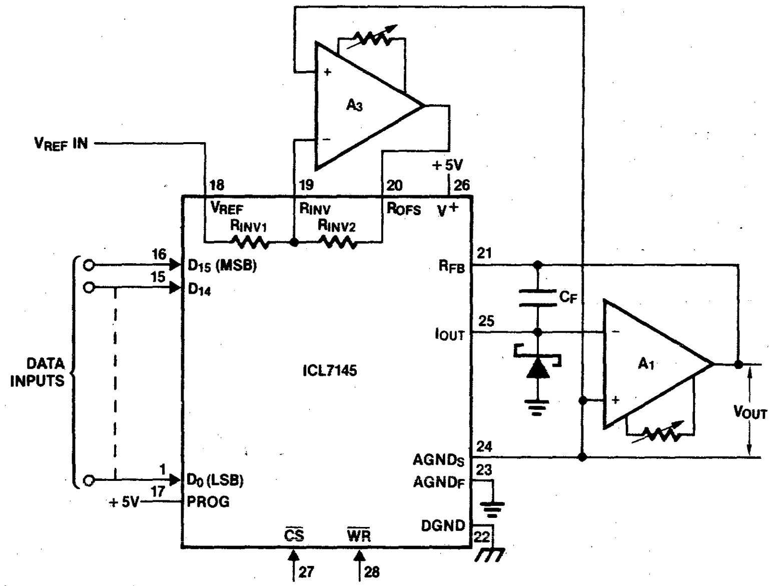


Figure 2. Bipolar Operation, Four-Quadrant

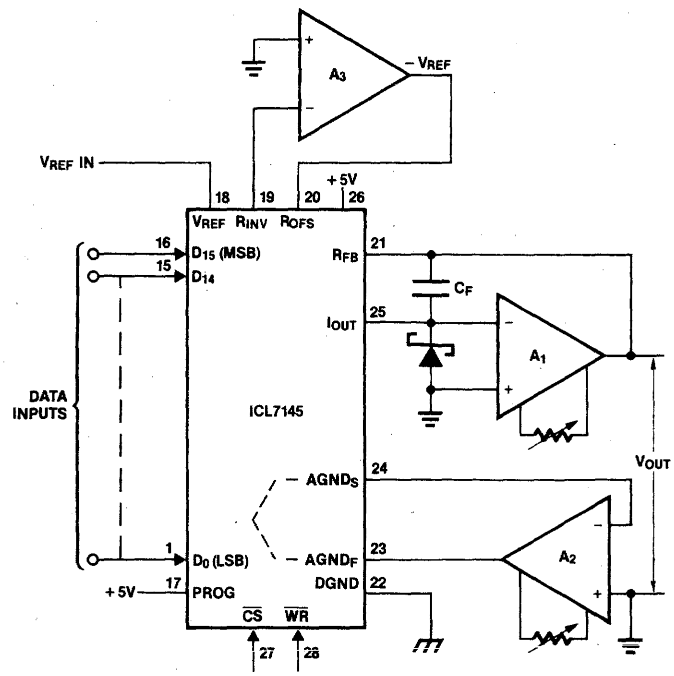


Figure 3. Operation with Forced Ground

INTERSIL

ICL7146 Complete 12-Bit Processor Compatible CMOS DAC

FEATURES

- Low Impedance Voltage Output
- Double-Buffered Processor Interface
- Easy-To-Use Bipolar Offset
- Multiplying Capability
- On-Chip Trimmed Reference
- 7μs Settling Time
- No External Gain or Offset Adjustment Required
- Low Power Dissipation 50mW
- No Critical External Components

ORDERING INFORMATION

Part Number	Linearity	Temperature Range	Package
ICL7146LCJI	0.01%	0 to +70°C	CERDIP
ICL7146LIJI		−40°C to +85°C	
ICL7146KCJI	0.02%	0 to +70°C	
ICL7146KIJI		−40°C to +85°C	
ICL7146JCJI	0.05%	0 to +70°C	
ICL7146JIJI		−40°C to +85°C	

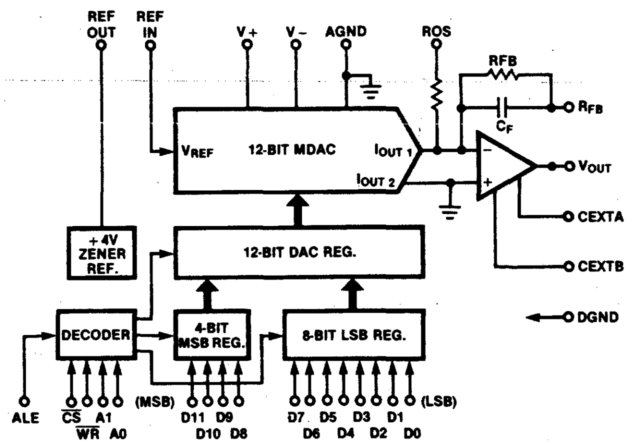
GENERAL DESCRIPTION

The ICL7146 is the first of a series of complete 12-Bit CMOS DAC's. These DAC's feature all of the needed support circuitry to interface to processors and give a voltage output. Contained on the chip are two levels of latches for double buffers, a trimmed reference, a latch controller, and an output buffer amplifier. All devices are accurately trimmed for both gain and offset so that no external trimming is required.

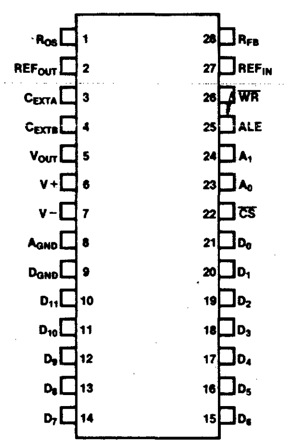
CMOS circuitry is used to keep the power dissipation low, and with all devices contained on a single chip, significant board size reductions are possible. As an alternative to this, many more analog channels could be added to a board and still decrease power consumption. Intersil's patented autostabilized op amp construction eliminates drifts in the zero offset and provides a fast (7 μs) settling time.

Processor interface is double-buffered with all 12-bits being brought out. The first level of latches is divided into 4 and 8 bit bytes with a 12 bit wide second buffer. Data can be directly entered into any of the three buffers or the buffers can be operated separately.

BLOCK DIAGRAM



PIN CONFIGURATION



its output value. Neither of these conditions are acceptable in a wide variety of applications. Hence the need for double buffering.

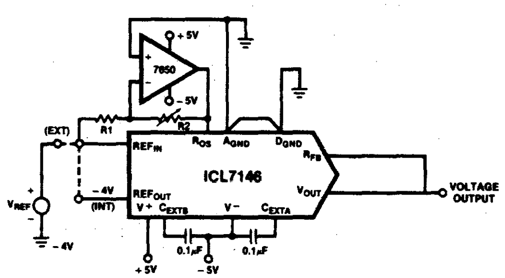
Buffer control is handled by a decoder to ease processor interface requirements. Operation of the decoder is shown in the truth table.

TYPICAL APPLICATIONS
Bipolar Output

Offset Binary Code Table

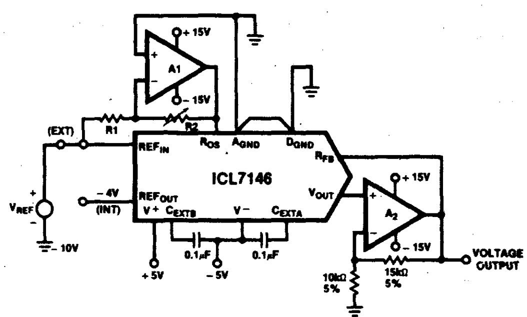
Binary Number In DAC Register (MSB … LSB)	Analog Output, V_{OUT}
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

± 4V BIPOLAR OUTPUT:



NOTE 1: A1 should be selected or trimmed for low offset voltage; R1 & R2 are 10kΩ resistors trimmed to a matching of 0.1% or better.

± 10V BIPOLAR OUTPUT:



NOTE 1: A1 should be selected or trimmed for low offset voltage; R1 & R2 are 10kΩ resistors trimmed to a matching of 0.1% or better.

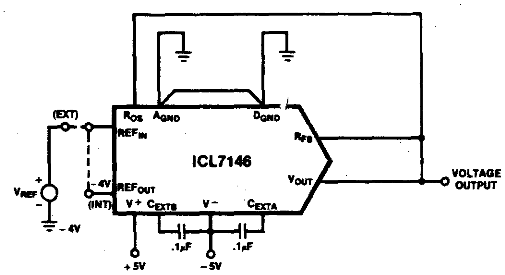
NOTE 2: A2 needs not to have a low offset voltage but it must be fast (>8MHz) to insure stability.

TYPICAL APPLICATIONS
Unipolar Output

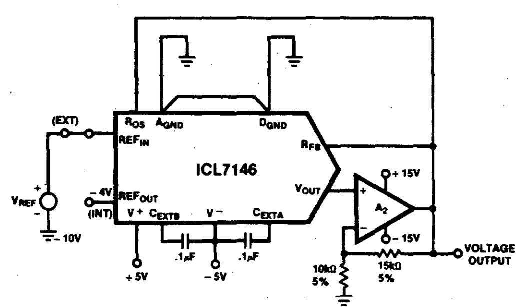
Code Table

Binary Number In DAC Register (MSB … LSB)	Analog Output, V_{OUT}
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -1/2\,V_{REF}$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0001	0V

+ 4V UNIPOLAR OUTPUT:



+ 10V UNIPOLAR OUTPUT:



NOTE 1: A2 needs not to have a low offset voltage but it must be fast (>8MHz) to insure stability.

Absolute Maximum Ratings (Note 1)

REF_{IN}, R_{FB}, R_{OS} .... ±25V
V^+ 6.2V
V^- .... −9.0V
REF_{OUT}, V_{OUT}, C_{EXT},
A_{GND} .... V^- −0.3V to V^+ + 0.3V
Digital Inputs .... V^+ +0.3V to D_{GND} − 0.3V
Storage Temperature Range ..... −65°C to +150°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: All Voltages with Respect to D_{GND}

Operating Characteristics

$V+ = 5V$, $V- = -5V$, $V_{ref} = 4.00V$, $T_A = 25°C$, $R_L = 20k$, $C_L = 50pF$

Parameter	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
Resolution			12			Bits
Non Linearity J K L					.05 .02 .01	% FSR % FSR % FSR
Differential Linearity J K L		Guaranteed Monotonic		±3/4 ±1/2 ±1/2	±2 ±1 ±1	LSB
Gain Error				0.1	0.2	% FSR
Unipolar Zero Error				60	120	μV
Bipolar Zero Code Error		R_{FB} Connected to V_{OUT} R_{OS} Connected to $-V_{REF}$		0.025	0.05	% FSR
Positive Power Supply Rejection Ratio		V+ = 4.5 to 5.5V External Reference		±0.001	0.005	% FSR/ % V+
Negative Power Supply Rejection Ratio		V− = −4.5 to −5.5V External Reference		0	±0.001	% FSR/ % V+
Voltage Setting Time (Note 1)		To 1/2 LSB		7	10	μs
Feedthrough Error		V_{REF} = 8V P-P, 10 kHz Sine Wave			1	mV P-P
Reference Input Resistance		−55°C to 125°C	5	10	20	KΩ
Internal Reference Voltage			−4.04	−4.00	−3.96	V
Internal Reference Tempco				25	50	PPM of FSR per °C
Positive Supply Voltage Range	V+	Functional Operation, Internal or External Reference	4.5	5.0	5.5	V
Negative Supply Voltage Range	V−	Functional Operation, External Reference	−4.5	−5.0	−7.5	V
		Functional Operation, Internal Reference	−4.75	−5.0	−7.5	V
Output Voltage Range		R_{FB} connected to V_{OUT}		±4		V
Output Drive Current			±2			mA

INTERSIL

ICL7667
Dual Power MOS Driver

FEATURES

- 1.5A Peak Output Current
- Fast Rise and Fall Times
  — 40ns with 1000pF load
- Wide Supply Voltage Range
  — V_{CC} = 4.5 to 20V
- Low Power Consumption
  — 4mW with inputs low
  — 120mW with inputs high
- TTL/CMOS Input Compatible Power Driver
  — R_{OUT} = 6Ω
- Direct Interface with Common Switching Regulators
- Pin Equivalent to DS0026/DS0056

TYPICAL APPLICATIONS

- Switching Power Supplies
- DC/DC Converters
- Motor Controllers

GENERAL DESCRIPTION

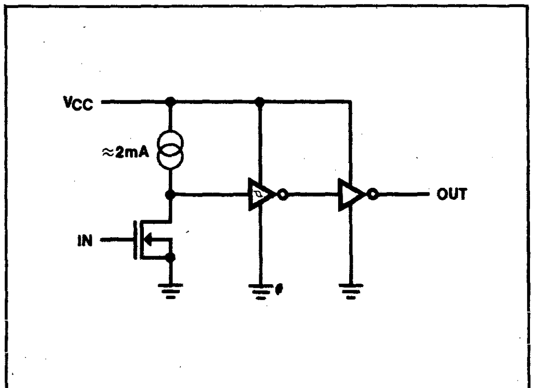
The ICL7667 is a dual monolithic high-speed driver designed to convert TTL level signals into high current outputs at voltages up to 20V. Its high speed and 1.5A peak current output enable it to drive large capacitive loads with high slew rates and low propagation delays. With an output voltage swing only millivolts less than the supply voltage and a maximum supply voltage of 20V, the ICL7667 is well suited for driving power MOSFETs in high frequency switching regulators. The ICL7667's high current (1.5A peak) outputs minimize power losses in the power MOSFETs by rapidly charging and discharging the gate capacitances, while the ICL7667's inputs are TTL compatible and can be directly driven by common switching regulator IC's.

ORDERING INFORMATION

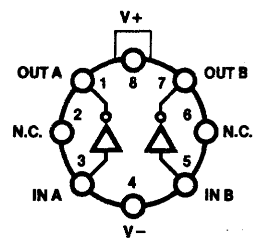
Temperature Range	Package	Order Number
−55°C to +125°C	TO-99 Can	ICL7667MTV
	8-Pin Cerdip	ICL7667MJA
0 to +70°C	8-Pin Plastic	ICL7667CPA
	8-Pin Cerdip	ICL7667CJA
	TO-99 Can	ICL7667CJA
0 to +70°C	Dice	ICL7667C/D

(pin configuration for TV and PA packages also on this page)

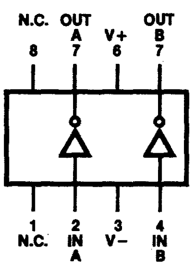
BLOCK DIAGRAM



PIN CONFIGURATION



TOP VIEW
TO-99
(TV)



TOP VIEW
8-PIN DIP
(PA, JA)

ICL7667

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 22V
Input Voltage .... 22V to (V^- −0.3V)
Peak Output Current 1.5A
Package Dissipation, $T_A = 25°C$ 500mW
Linear Derating Factors

TO-99	Plastic	Cerdip
6.7mW/°C	5.6mW/°C	6.7mW/°C
above 50°C	above 36°C	above 50°C

Storage Temperature .... −65°C to +150°C

Lead Temperature (Soldering, 10 seconds) ...... 300°C
Operating Temperature Range
C Series .... 0 to +70°C
M Series .... −55°C to +125°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC OPERATING CHARACTERISTICS

Test Conditions: V_{CC} = 4.5 to 20V, T_A = +25°C unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Logic 1 Input Voltage	V_{IH}		2.4	2.0		V
Logic 0 Input Voltage	V_{IL}			1.5	0.8	V
Input Current	I_{IL}	$0 < V_{IN} < V_{CC}$	−1	0	1	μA
Output Voltage High	V_{OH}	No Load	V_{CC} −0.05	V_{CC}		V
Output Voltage Low	V_{OL}	No Load		0	0.05	V
Output Resistance	R_{OUT}	$V_{IN} = V_{IL}$ I_{OUT} = −10mA V_{CC} = 20V		6	20	Ω
Output Resistance	R_{OUT}	$V_{IN} = V_{IH}$ I_{OUT} = 10mA V_{CC} = 20V		6	20	Ω
Power Supply Current	I_{CC}	V_{IN} = 3V (both inputs)		4	6	mA
Power Supply Current	I_{CC}	V_{IN} = 0V (both inputs)		150	400	μA

AC OPERATING CHARACTERISTICS

Test Conditions: V_{CC} = 20V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Delay Time	T_{D2}	Figure 1		50	75	ns
Delay Time	T_{D2}	Figure 2		50	75	ns
Rise Time	T_R	Figure 1		25	35	ns
Rise Time	T_R	Figure 2		35	50	ns
Fall Time	T_F	Figure 1		30	40	ns
Fall Time	T_F	Figure 2		40	55	ns
Delay Time	T_{D1}	Figure 1		20	35	ns
Delay Time	T_{D1}	Figure 2		20	35	ns

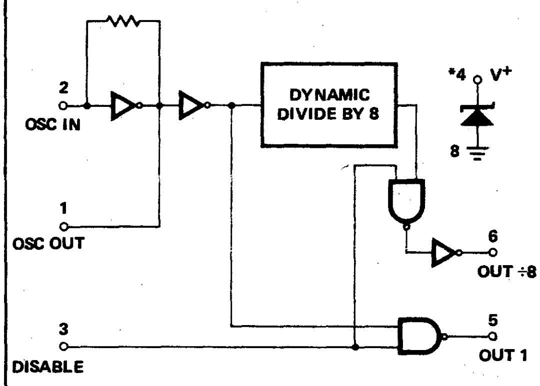
INTERSIL

ICM7209
CMOS Clock Generator

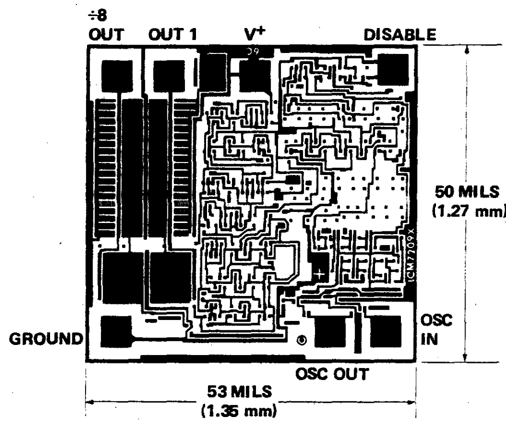
FEATURES
- High frequency operation — 10MHz guaranteed
- Easy to use oscillator — requires only a quartz crystal and two capacitors
- Bipolar, MOS and CMOS compatibility
- High output drive capability — 5 x TTL fanout with 10ns rise and fall times
- Low power — 50mW at 10MHz
- Choice of two output frequencies — osc., and osc. ÷8 frequencies
- Disable control for both outputs
- Wide industrial temperature range — −20°C to +85°C
- All inputs fully protected — circuits may be handled without any special precautions

GENERAL DESCRIPTION
The Intersil ICM7209 is a versatile CMOS clock generator capable of driving a number of 5 volt systems with a variety of input requirements. When used to drive up to 5 TTL gates, the typical rise and fall times are 10ns.

The ICM7209 consists of an oscillator, a buffered output equal to the oscillator frequency and a second buffered output having an output frequency one-eighth that of the oscillator. The guaranteed maximum oscillator frequency is 10MHz. Connecting the DISABLE terminal to the negative supply forces the ÷8 output into the '0' state and the output 1 into the '1' state.

SCHEMATIC DIAGRAM


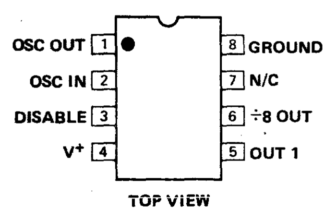
*ZENER VOLTAGE IS TYPICALLY 6.3 VOLTS

CHIP TOPOGRAPHY


ORDERING INFORMATION

ICM7209 I PA
- PA — Package (See Outline Drawing)
- I — Temperature Range (Industrial: -20 to +85°C)
- ICM7209 — TYPE

Order Devices by Following Part Number ICM7209 I PA
Order Dice by Following Part Number ICM7209/D

PIN CONFIGURATION (OUTLINE DRAWING PA)


Pin 1 is designated by either a dot or a notch.

ICM7209

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (25°C) 300mW
Supply Voltage .... 6 V
Output Voltages .... Equal to or less than supply
Input Voltages .... Equal to or less than supply
Storage Temp. .... −55°C to +125°C
Operating Temp. Range .... -20°C to +85°C
Lead Temp. (Soldering, 10 seconds) .... 300°C

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL OPERATING CHARACTERISTICS

TEST CONDITIONS: $V^+ = 5V \pm 10\%$, test circuit, $f_{osc} = 10MHz$, $T_A = 25°C$ unless otherwise specified.

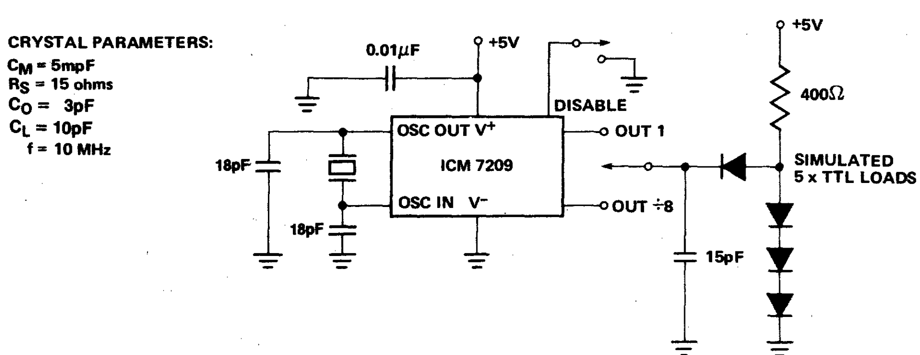
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP.	MAX	UNITS
Supply Current	I^+	Note 1 No Load		11	20	mA
Disable Input Capacitance	C_D				5	pF
Disable Input Leakage	I_{ILK}	Either '1' or '0' state			±10	μA
Output Low State	V_{OL}	Either OUT 1 or OUT ÷8 simulated 5 x TTL loads			0.4	V
Output High State	V_{OH}	Either OUT 1 or OUT ÷8 simulated 5 x TTL loads	4.0	4.9		V
Output Rise Time (Note 3)	t_r	Either OUT 1 or OUT ÷8 simulated 5 x TTL loads		10	25	ns
Output Fall Time (Note 3)	t_f	Either OUT 1 or OUT ÷8 simulated 5 x TTL loads		10	25	ns
Minimum OSC Frequency for ÷8 Output	f_{osc}	Note 2	2			MHz
Output ÷8 duty cycle		Any operating frequency Low state : High state		7:9		
Oscillator Transconductance	gm		80	200		μmho

NOTE 1: The power dissipation is a function of the oscillator frequency (1st ORDER EFFECT see curve) but is also effected to a small extent by the oscillator tank components.

NOTE 2: The ÷8 circuitry uses a dynamic scheme. As with any dynamic system, information or data is stored on very small nodal capacitances instead of latches (static systems) and there is a lower cutoff frequency of operation. Dynamic dividers are used in the ICM7209 to significantly improve high frequency performance and to decrease power consumption.

NOTE 3: Rise and fall times are defined between the output levels of 0.5 and 2.4 volts.

TEST CIRCUIT



INTERSIL

ICM7243

8-Character 14-/16-Segment Alphanumeric LED Display Driver

FEATURES

- **14- and 16-segment fonts with decimal point**
- **Mask programmable for other font-sets up to 64 characters**
- **Microprocessor compatible**
- **Directly drives small common cathode displays**
- **Cascadable without additional hardware**
- **Standby feature turns display off; puts chip in low power mode**
- **Serial entry or random entry of data into display**
- **Single +5V operation**
- **Character and segment drivers, all MUX scan circuitry, 8×6 static memory and 64-character ASCII font generator included on-chip**

GENERAL DESCRIPTION

The ICM7243 is an 8-character alphanumeric display driver and controller which provides all the circuitry required to interface a microprocessor or digital system to a 14- or 16-segment display. It is primarily intended for use in microprocessor systems, where it offloads the processor and minimizes hardware and software overhead. Incorporated on-chip are a 64-character ASCII decoder, an 8×6 memory, the high power character and segment drivers, and the multiplex scan circuitry.

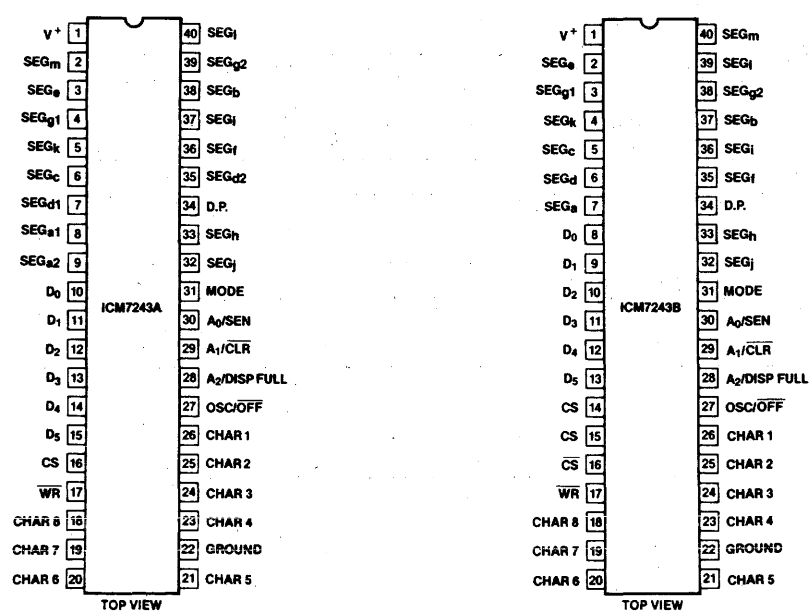
Six-bit ASCII data to be displayed is written into the memory directly from the microprocessor data bus. Data location depends upon the selection of either **Serial** (MODE = 1) or **Random** (MODE = 0). In the **Serial Access** mode the first entry is stored in the lowest location and displayed in the "left-most" character position. Each subsequent entry is automatically stored in the next higher location and displayed to the immediate "right" of the previous entry. A DISPlay FULL signal is provided after 8 entries; this signal can be used for cascading. A $\overline{\text{CLeaR}}$ pin is provided to clear the memory and reset the location counter. The **Random Access** mode allows the processor to select the memory address and display digit for each input word.

The character multiplex scan runs whenever data is not being entered. It scans the memory and CHARacter drivers, and ensures that the decoding from memory to display is done in the proper sequence. Intercharacter blanking is provided to avoid display ghosting.

ORDERING INFORMATION

Part Number	Display Segments	Package	Order Number
ICM7243A	16 + d.p.	40 Pin CERDIP	ICM7243AIJL
ICM7243B	14 + d.p.	40 Pin CERDIP	ICM7243BIJL
ICM7243B EV/KIT	Kit with Display		ICM7243B EV/KIT

PIN CONFIGURATIONS



ICM7243

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6V
CHARacter Output Current 300mA
SEGment Output Current 30mA
Input Voltage (Any Terminal) .... (V^+ +0.3V) to −0.3V
Power Dissipation 1W
Operating Temperature Range .... −20°C to +85°C
Storage Temperature Range .... −55°C to +125°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Supply Voltage	V^+		4.75	5.0	5.25	V
Operating Supply Current	I^+_{OP}	V^+ = 5.25V, 10 Segments ON, All 8 Characters		180		mA
Quiescent Supply Current	I_Q^+	V^+ = 5.25V, OSC/$\overline{OFF}$ Pin <1V		30	250	μA
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Input Current	I_{IN}	V^+ = 5.25V, V_{IH} = 5V			+1	μA
		V_{IL} = 0V	−1			
CHARacter Drive Current	I_{CHAR}	V^+ = 5V, V_{OUT} = 1V	140	190		mA
CHARacter Leakage Current	I_{CHLK}					μA
SEGment Drive Current	I_{SEG}	V^+ = 5V, V_{OUT} = 2.5V	14	19		mA
SEGment Leakage Current	I_{SLK}			0.01		μA
DISPlay FULL Output Low	V_{OL}	I_{OL} = 1.6mA			0.4	V
DISPlay FULL Output High	V_{OH}	I_{IH} = 100μA	2.4			V
Display Scan Rate	f_{ds}			400		Hz

AC CHARACTERISTICS (Drive levels 0.4V and 2.4V, timing measured at 0.8V and 2.0V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\overline{WR}$, $\overline{CLeaR}$ Pulse Width Low	t_{WPl}		250			ns
$\overline{WR}$, $\overline{CLeaR}$ Pulse Width High	t_{WPh}		250			ns
Data Hold Time	t_{Dh}		0	−20		ns
Data Setup Time	t_{Ds}		250	150		ns
Address, SEN, MODE Hold Time	t_{Ah}		125	80		ns
Address, SEN, MODE Setup Time	t_{As}		−20			ns
CS, $\overline{CS}$ Setup Time	t_{Cs}		0			ns
Pulse Transition Time	t_t				100	ns

CAPACITANCE

SYMBOL	TEST	MIN	TYP	MAX	UNIT
C_{IN}	Input Capacitance				pF
C_O	Output Capacitance				pF

APPLICATIONS (Continued)

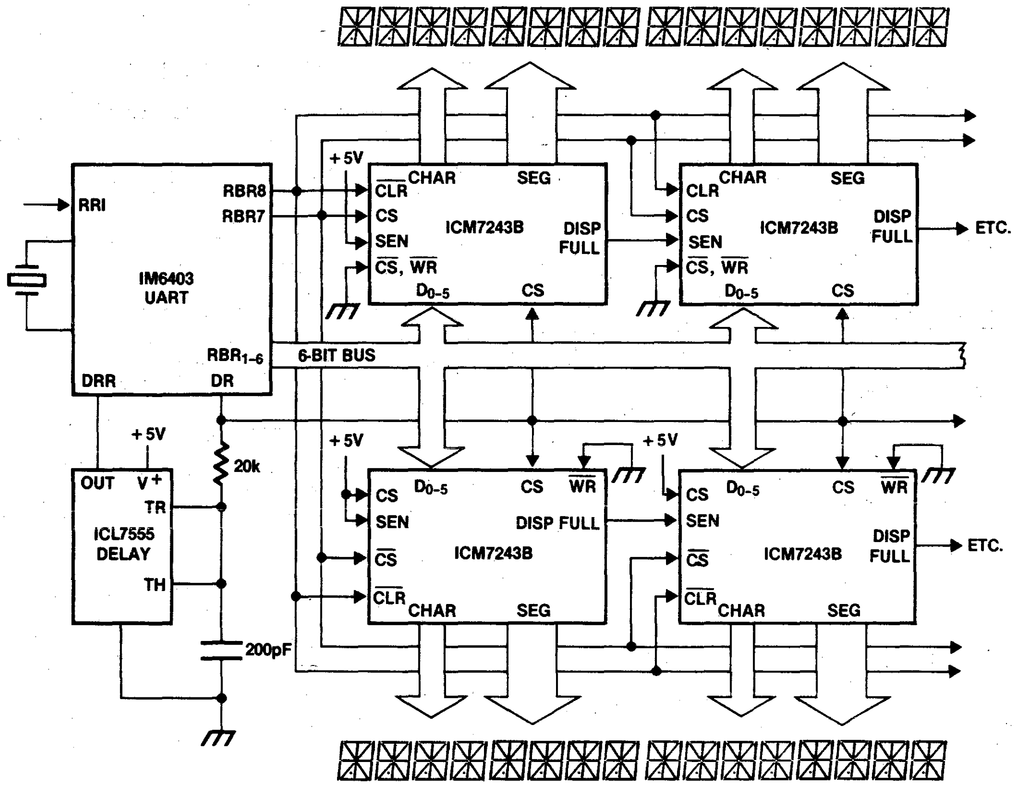


Figure 2. Driving Two Rows of Characters from a Serial Input. UART converts data stream to parallel bytes. Bit 7 of each word sets which row data will be entered into. Bit 8 will blank and reset whole display if low. Each MODE pin should be tied high. ICM7243A can also be used, with inverter on RBR7 for one row.

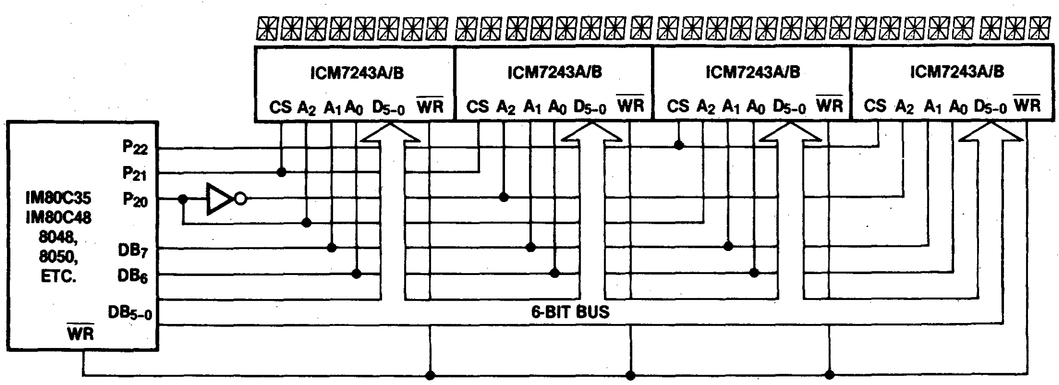


Figure 3. Random Access 32-Character Display in MCS-48 system. One port line controls A_2, other two are CS lines. 8-bit data bus drives 6 data and 2 address lines. MODE should be GrouNDed on each part.

INTERSIL

ICM7281
LCD Column Driver

FEATURES

- LCD Dot Matrix Column Driver
- 40 High Voltage LCD Column Drive Outputs For Up to 8 5xN Characters per IC
- Easy Interface
  —Serial Input Shift Register With parallel latch and carry outputs
- Directly Compatible with ICM7280 Row Driver
  —Up to 10 ICM7281's can be driven by an ICM7280 with no external components
- Low Resistance Outputs
  —Can drive both columns and rows of LCD graphics displays
- Will Drive 1.5V Threshold LCDs with Only Single 5V Supply
  —Can drive up to 4.5V threshold LCDs with 15V V_{DISP}

GENERAL DESCRIPTION

The ICM7281 LCD Dot Matrix Column Driver is designed to convert a serial data stream into drive signals for a multiplexed dot matrix LCD. Easily cascadable, up to 10 ICM7281's can be driven by one ICM7280 Intelligent Row Driver to make an 80 character dot matrix display. The ICM7281 also serves as both a Row Driver and Column Driver in LCD dot matrix graphics displays. The low output resistance and the 15V drive capability make it well suited for graphics displays with up to 256 x 256 dots (with 10pF/dot capacitance).

The ICM7281 consists of a 40 bit shift register, a 40 bit latch and 40 level-shifters/drivers. The 4 display drive voltages are generated externally, usually by a Row Driver. A serial data interface is used to minimize the number of pins needed for digital interfacing. Two data Carry Outputs are included for cascading several ICM7281's to drive large LCD displays.

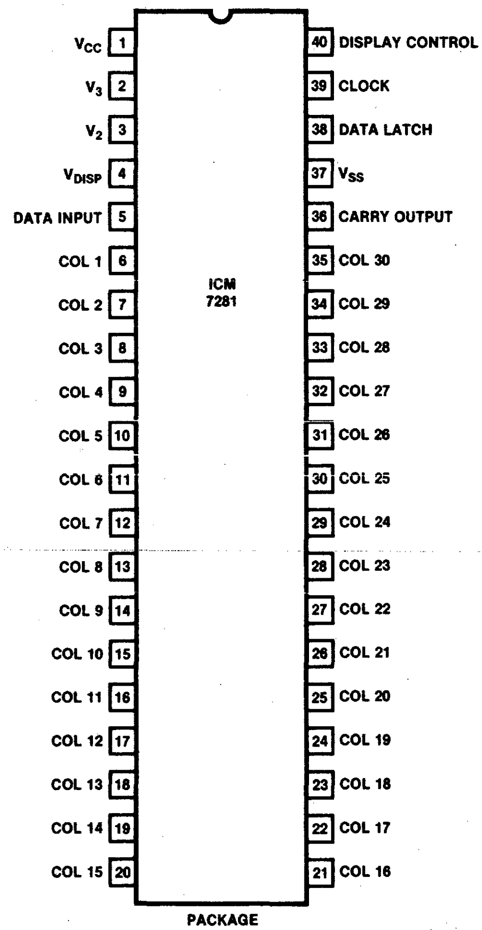
ORDERING INFORMATION

No. Of Columns	Package	Order Number
30	40 Pin Plastic	ICM7281IPL
40	Dice	ICM7281I/D
40	52-64 Pin Plastic Flatpack	—

TYPICAL APPLICATIONS

- Column Drivers for Dot Matrix Alphanumeric Displays using ICM7280 Row Driver
- Row and Column Drivers for LCD Dot Matrix Graphics Displays
- Segment Driver for LCD Bargraphs and Annunciators
- Serial Input I/O Expander

PIN CONFIGURATIONS
(Outline dwg. PL)



GE INTERSIL

IH5040-IH5051 Family High Level CMOS Analog Gates

FEATURES

- Switches Greater Than 20Vpp Signals With ±15V Supplies
- Quiescent Current Less Than 1μA
- Overvoltage Protection to ±25V
- Break-Before-Make Switching t_{off} 200 nsec, t_{on} 300 nsec Typical
- T^2L, DTL, CMOS, PMOS Compatible
- Non-Latching With Supply Turn-Off
- Low $r_{DS(on)}$ – 35Ω
- New DPDT & 4PST Configurations
- Complete Monolithic Construction IH5040 through IH5047

FUNCTIONAL DIAGRAM

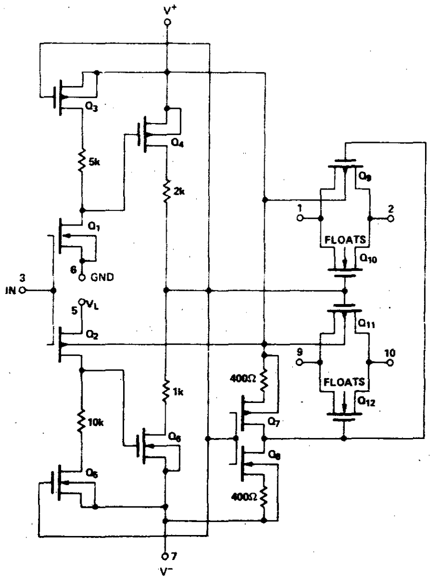
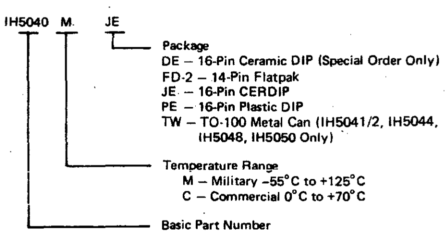


FIGURE 1. TYPICAL DRIVER, GATE – IH5042

ORDERING INFORMATION



GENERAL DESCRIPTION

The IH5040 family of solid state analog gates are designed using an improved, high voltage CMOS monolithic technology. These devices provide ease-of-use and performance advantages not previously available from solid state switches. This improved CMOS technology provides input overvoltage capability to ±25 volts without damage to the device, and destructive latch-up of solid state analog gates has been eliminated. Early CMOS gates were destroyed when power supplies were removed with an input signal present. The IH5040 CMOS technology has eliminated this serious systems problem.

Key performance advantages of the 5040 series are TTL compatibility and ultra low-power operation. The quiescent current requirement is less than 1μA. Also designed into the 5040 is guaranteed Break-Before-Make switching, which is accomplished by extending the t_{on} time (300 nsec TYP.) so that it exceeds t_{off} time (200 nsec TYP.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. This eliminates the need for external logic required to avoid channel to channel shorting during switching.

Many of the 5040 series improve upon and are pin-for-pin and electrical replacements for other solid state switches.

FUNCTIONAL DESCRIPTION

INTERSIL PART NO.	TYPE	$r_{DS(on)}$	PIN/FUNCTIONAL EQUIVALENT (Note 1)
IH5040	SPST	75Ω	
IH5041	Dual SPST	75Ω	
IH5042	SPDT	75Ω	DG 188AA/BA
IH5043	Dual SPDT	75Ω	DG 191AP/BP
IH5044	DPST	75Ω	
IH5045	Dual DPST	75Ω	DG 185AP/BP
IH5046	DPDT	75Ω	
IH5047	4PST	75Ω	
IH5048 Dual	SPST	35Ω	
IH5049 Dual	DPST	35Ω	DG 184AP/BP
IH5050	SPDT	35Ω	DG 187AA/BA
IH5051 Dual	SPDT	35Ω	DG 190AP/BP

NOTE 1. See Switching State diagrams for applicable package equivalency.

Pin and functional equivalent monolithic versions of the DG181, DG182, DG187 and DG188 are available. See data sheet for this and also IH181 to IH191.

IH5040-IH5051 Family

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Current (Any Terminal) . . . . < 30mA
Storage Temperature . . . . -65°C to +150°C
Operating Temperature . . . . -55°C to +125°C
Power Dissipation 450mW
(All Leads Soldered to a P.C. Board)
Derate 6mW/°C Above 70°C
Lead Temperature (Soldering, 10 sec) . . . . 300°C

$V^+ - V^-$	< 33V
$V^+ - V_D$	< 30V
$V_D - V^-$	< 30V
$V_D - V_S$	< ±22V
$V_L - V^-$	< 33V
$V_L - V_{IN}$	< 30V
V_L-GND	< 20V
V_{IN}-GND	< 20V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (@ 25°C, $V^+ = +15$ V, $V^- = -15$ V, $V_L = +5$ V)

PER CHANNEL		MIN./MAX. LIMITS							
		MILITARY			COMMERCIAL				
SYMBOL	CHARACTERISTIC	-55°C	+25°C	+125°C	0	+25°C	+70°C	UNITS	TEST CONDITIONS
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	µA	V_{IN} = 2.4 V Note 1
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	µA	V_{IN} = 0.8 V Note 1
$r_{DS(on)}$	Drain–Source On Resistance	75(35)	75(35)	150(60)	80 (45)	80 (45)	130 (45)	Ω	(IH5048 Thru IH5051) I_S = 10 mA V_{ANALOG} = -10 V to +10 V
$\Delta r_{DS(ON)}$	Channel to Channel $r_{DS(ON)}$ Match		25 (15) (typ)			30(15) (typ)		Ω	(IH5048 thru IH5051)
V_{ANALOG}	Min. Analog Signal Handling Capability		±11(±10)			±10(±10)		V	
$I_{D(OFF)}$	Switch OFF Leakage Current	1(1)	1(1)	100(100)	5(5)	5(5)	100(100)	nA	V_{ANALOG} = -10 V to +10 V (IH5048 thru IH5051
$I_{D(ON)}$ $+I_{S(ON)}$	Switch On Leakage Current	2(2)	2(2)	200(200)	10 (10)	10 (10)	100(200)	nA	$V_D = V_S$ = -10 V to + 10 V (IH5048 thru IH5051)
t_{on}	Switch "ON" Time		500(250)			500(300)		ns	R_L = 1 kΩ, V_{ANALOG} = -10 V to +10 V See Fig. A
t_{off}	Switch "OFF" Time		250(150)			250(150)		ns	R_L = 1 kΩ, V_{ANALOG} = -10 V to +10 V See Fig. A (IH5048 thru IH5051)
$Q_{(INJ.)}$	Charge Injection		15 (10)			20 (10)		mV	See Fig. B (IH5048 thru IH5051)
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	f = 1 MHz, R_L = 100Ω, C_L ≤ 5 pF See Fig. C, (Note 1)
I^+_Q	+ Power Supply Quiescent Current	1	1	10	10	10	100	µA	
I^-_Q	– Power Supply Quiescent Current	1	1	10	10	10	100	µA	V^+ = +15 V, V^- = -15 V, V_L = +5 V V_L = +5 V
I^-_{LQ}	+5 V Supply Quiescent Current	1	1	10	10	10	100	µA	
I_{GND}	Gnd Supply Quiescent Current	1	1	10	10	10	100	µA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off; Any Other Channel Switches as per Fig. E (Note 1)

Note 1: Not tested in production.

TEST CIRCUITS

FIG. A

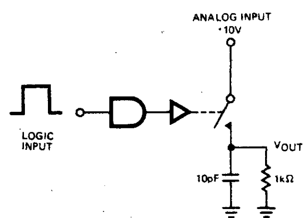


FIG. B

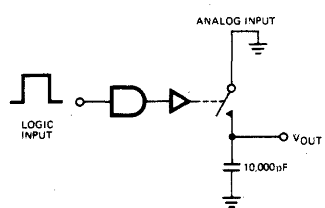
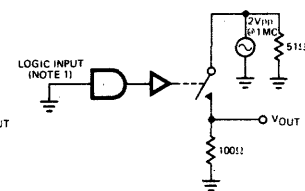


FIG. C

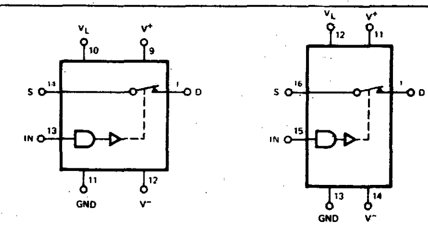


NOTE 1: Some channels are turned on by high "1" logic inputs and other channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to see absolute value of logic input required to produce "ON" or "OFF" state.

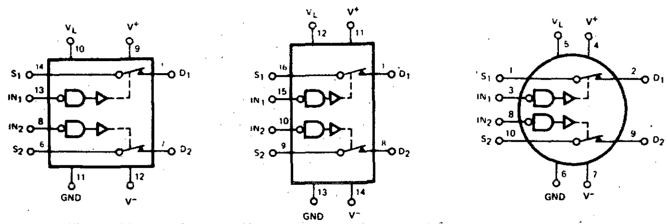
SWITCHING STATE DIAGRAMS

SWITCH STATES ARE FOR LOGIC "1" INPUT — (OUTLINE DWG FD-2) — (OUTLINE DWGS DE, JE, PE) — (OUTLINE DWG TO-100)

SPST
IH5040 ($r_{DS(on)} < 75\Omega$)

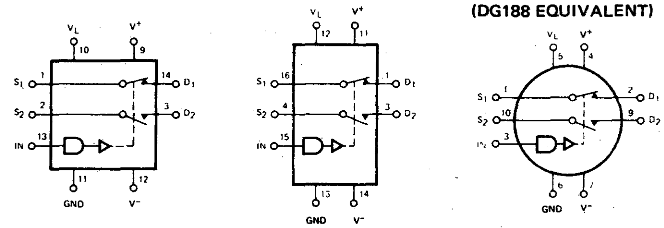


DUAL SPST
IH5041 ($r_{DS(on)} < 75\Omega$)



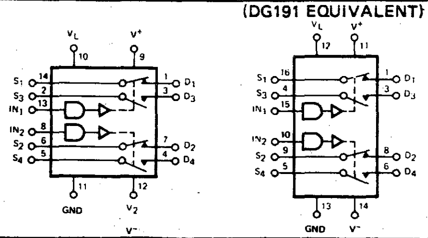
SPDT
IH5042 ($r_{DS(on)} < 75\Omega$)

(DG188 EQUIVALENT)

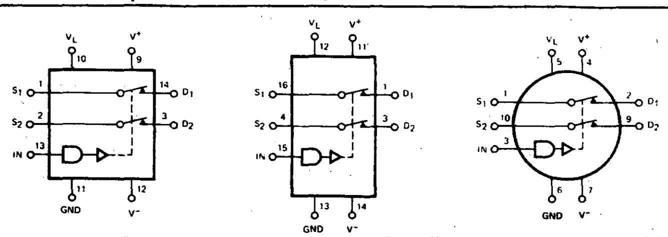


DUAL SPDT
IH5043 ($r_{DS(on)} < 75\Omega$)

(DG191 EQUIVALENT)

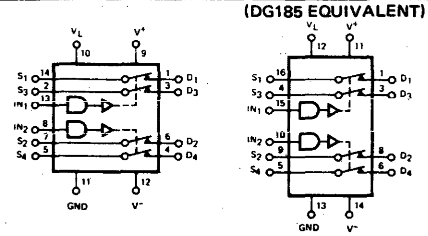


DPST
IH5044 ($r_{DS(on)} < 75\Omega$)



DUAL DPST
IH5045 ($r_{DS(on)} < 75\Omega$)

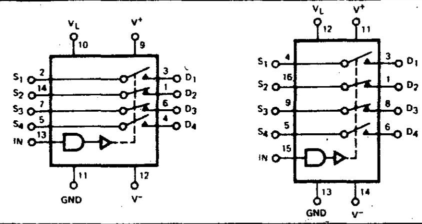
(DG185 EQUIVALENT)



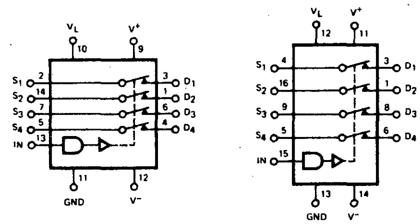
SWITCHING STATE DIAGRAMS (Cont.)

SWITCH STATES ARE FOR LOGIC "1" INPUT — FLAT PACKAGE (FD-2) — DIP (DE) PACKAGE — TO-100

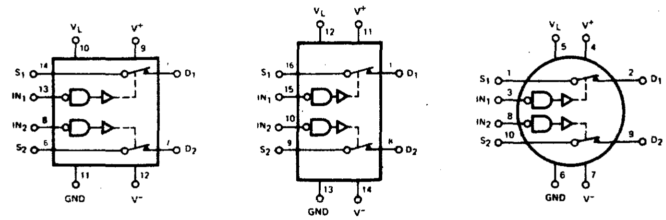
DPDT
IH5046 (r_{DS} (ON) <75Ω)



4PST
IH5047 (r_{DS} (ON) <75Ω)

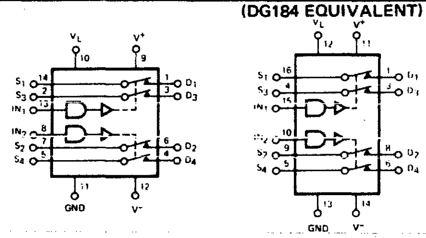


DUAL SPST
IH5048 (r_{DS} (ON) <35Ω)

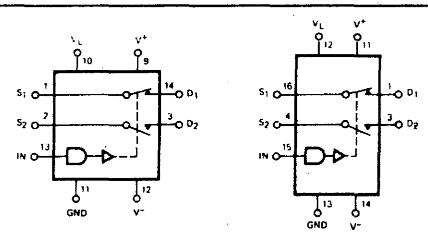


DUAL DPST
IH5049 (r_{DS} (ON) <35Ω)

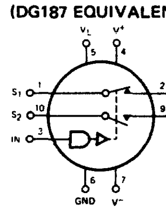
(DG184 EQUIVALENT)



SPDT
IH5050 (r_{DS} (ON) <35Ω)

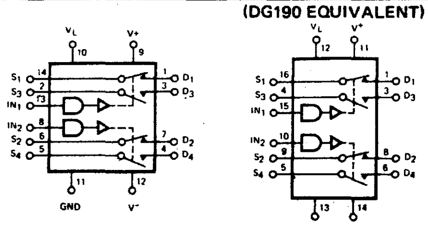


(DG187 EQUIVALENT)



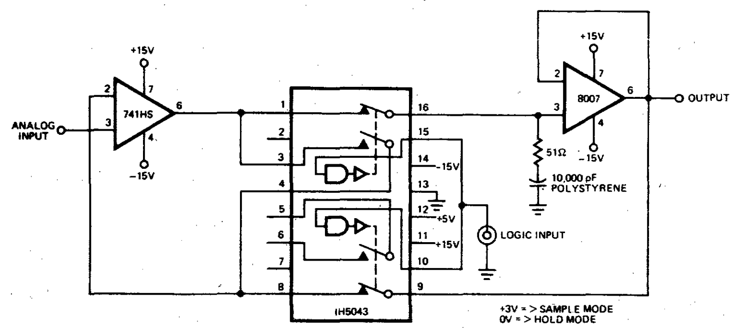
DUAL SPDT
IH5051 (r_{DS} (ON) <35Ω)

(DG190 EQUIVALENT)

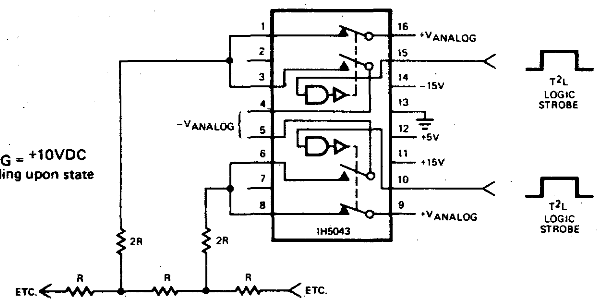


APPLICATIONS

IMPROVED SAMPLE & HOLD
USING IH5043

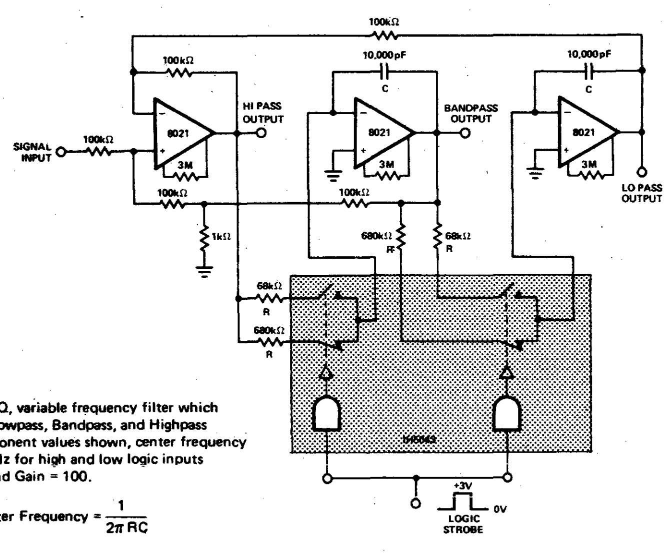


USING THE CMOS SWITCH TO DRIVE
AN R/2R LADDER NETWORK (2 LEGS)



EXAMPLE: If $-V_{ANALOG} = -10VDC$ and $+V_{ANALOG} = +10VDC$ then Ladder Legs are switched between ±10VDC, depending upon state of Logic Strobe.

DIGITALLY TUNED
LOW POWER ACTIVE FILTER



Constant gain, constant Q, variable frequency filter which provides simultaneous Lowpass, Bandpass, and Highpass outputs. With the component values shown, center frequency will be 235Hz and 23.5Hz for high and low logic inputs respectively, Q = 100, and Gain = 100.

$$f_n = \text{Center Frequency} = \frac{1}{2\pi RC}$$

IH5108

8-Channel Fault Protected CMOS Analog Multiplexer

FEATURES

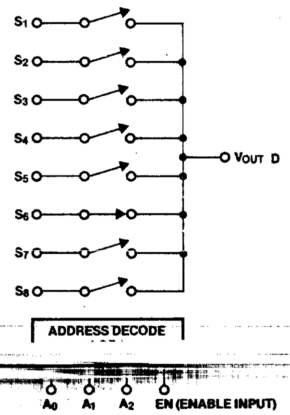
- Ultra low leakage— $I_{D(off)} \leq 100pA$
- Power supply quiescent current less than 1mA
- ±13V analog signal range
- No SCR latchup
- Break-before-make switching
- Pin compatible with DG508, HI508 and AD7508
- All channels OFF ($I_{ILK} \leq 100nA$) when power OFF, for analog signals up to ±25V
- Any channel turns OFF ($I_{ILK} \leq 100nA$) if input exceeds supply rails by up to ±25V. Throughput always < ±14V (±15V supplies)
- TTL and CMOS compatible binary Address and ENable inputs

GENERAL DESCRIPTION

The IH5108 is a dielectrically isolated CMOS monolithic analog multiplexer, designed as a plug-in replacement for the DG508 and similar devices, but adding fault protection to the standard performance. A unique serial MOSFET switch ensures that an OFF channel will remain OFF when the input exceeds the supply rails by up to ±25V, even with the supply voltage at zero. Further, an ON channel will be limited to a throughput of about 1.5V less than the supply rails, thus affording protection to any following circuitry such as op amps, D/A converters, etc. Cross talk onto "good" channels is also prevented.

A binary 3-bit address code together with the ENable input allows selection of any one channel or none at all. These 4 inputs are all TTL compatible for easy logic interface; the ENable input also facilitates MUX expansion and cascading.

FUNCTIONAL DIAGRAM



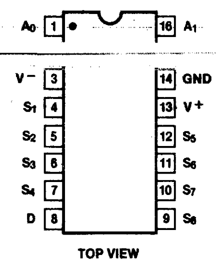
3 LINE BINARY ADDRESS INPUTS
(1 0 1) AND EN HI
ABOVE EXAMPLE SHOWS CHANNEL 6 TURNED ON

DECODE TRUTH TABLE

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

A_0, A_1, A_2, EN
Logic "1" = $V_{AH} \geq 2.4V$
Logic "0" = $V_{AL} \leq 0.8V$

PIN CONFIGURATION (outline dwg JE, PE)



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH5108MJE	−55°C to +125°C	16 pin CERDIP
IH5108IJE	−20°C to +85°C	16 pin CERDIP
IH5108CPE	0°C to 70°C	16 pin plastic DIP

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground . . . . −15V to 15V
V_S or V_D to V^+ . . . . +25V, −40V
V_S or V_D to V^- . . . . −25V, +40V
V^+ to Ground 16V
V^- to Ground . . . . −16V
Current (Any Terminal) 20mA

Operating Temperature . . . . −55 to 125°C
Storage Temperature . . . . −65 to 150°C
Power Dissipaton (Package)* 1200mW

*All leads soldered or welded to PC board. Derate 10mW/°C above 70°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS $V^+ = 15V$, $V^- = -15V$, $V_{EN} = 2.4V$, unless otherwise specified.

	CHARACTERISTIC	MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	MAX LIMITS M SUFFIX −55°C	MAX LIMITS M SUFFIX 25°C	MAX LIMITS M SUFFIX 125°C	MAX LIMITS I/C SUFFIX −20°C/0°C	MAX LIMITS I/C SUFFIX 25°C	MAX LIMITS I/C SUFFIX 85°C/70°C	UNIT	TEST CONDITIONS	
SWITCH	$r_{DS(on)}$	S to D	8	700	900	900	1200	1200	1200	1800	Ω	$V_D = 10V$, $I_S = -1.0mA$	Sequence each switch on
			8	500	900	900	1200	1200	1200	1800		$V_D = -10V$, $I_S = -1.0mA$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$
	$\Delta r_{DS(on)}$			5		10			10		%	$\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)avg.}}$ $V_S = \pm 10V$	
	$I_{S(off)}$	S	8	0.002		0.05	50		0.1	50	nA	$V_S = 10V$, $V_D = -10V$	
			8	0.002		0.05	50		0.1	50		$V_S = -10V$, $V_D = 10V$	
	$I_{D(off)}$	D	1	0.03		0.1	100		0.2	100		$V_D = 10V$, $V_S = -10V$	$V_{EN} = 0$
			1	0.03		0.1	100		0.2	100		$V_D = -10V$, $V_S = 10V$	
	$I_{D(on)}$	D	8	0.1		0.2	100		0.4	100		$V_{S(All)} = V_D = 10V$	Sequence each switch on
			8	0.1		0.2	100		0.4	100		$V_{S(All)} = V_D = -10V$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$
FAULT	I_S with Power OFF	S	8	1		100	1000	50	50	5000	nA	$V^+ = V^- = 0V$, $V_S = \pm 25V$, $V_{EN} = V_O = 0V$, $A_0, A_1, A_2 = 0V$ or 5V	
	$I_{S(off)}$ with Overvoltage (Note 1)	S	8	1		2000	5000		5000	5000		$V_S = \pm 25V$, $V_D = \mp 10V$	Sequence each switch
IN	$I_{EN(on)}$ $I_{A(on)}$	A_0, A_1, EN	4	.01		−10	−30		−10	−30	μA	$V_A = 2.4V$ or 0V	
	or $I_{EN(off)}$ $I_{A(off)}$		4	.01		10	30		10	30		$V_A = 15V$ or 0V	
DYNAMIC	$t_{transition}$	D		0.3		1					μs	See Figure 1	
	t_{open}	D		0.2								See Figure 2	
	$t_{on(EN)}$	D		0.6		1.5						See Figure 3	
	$t_{off(EN)}$	D		0.4		1							
	t_{on}-t_{off} Break-Before-Make Delay Settling Time	D	8	50		25			10		ns	$V_{EN} = +5V$, A_0, A_1, A_2 Strobed $V_{IN} = \pm 10V$, Figure 4	
	"OFF" Isolation	D		60							dB	$V_{EN} = 0$, $R_L = 200\Omega$, $C_L = 3pF$, $V_S = 3$ VRMS, f = 500 KHz	
	$C_{S(off)}$	S		5							pF	$V_S = 0$	$V_{EN} = 0V$,
	$C_{D(off)}$	D		25								$V_D = 0$	f = 140 KHz
	$C_{DS(off)}$	D to S		1								$V_S = 0$, $V_D = 0$	to 1 MHz
SUP	Supply Current +	V^+	1	500	900	750	600		1000		μA	All V_A, $V_{EN} = 0$ or 5V	
	Supply Current −	V^-	1	500	900	750	600		1000				

Note 1. Readings taken 400ms after the overvoltage occurs.

INTERSIL

IH5140 Family High Level CMOS Analog Gates

FEATURES

- Super fast break before make switching t_{on} 80ns typ, t_{off} 50ns typ (SPST switches)
- Power supply currents less than 1μA
- OFF leakages less than 100pA @ 25°C guaranteed
- Non-latching with supply turn-off
- Single monolithic CMOS chip
- Plug-in replacements for IH5040 family and part of the DG180 family to upgrade speed and leakage
- Greater than 1MHz toggle rate
- Switches greater than 20Vp-p signals with ±15V supplies
- T^2L, CMOS direct compatibility

GENERAL DESCRIPTION

The IH5140 Family of CMOS monolithic switches utilizes Intersil's latch-free junction isolated processing to build the fastest switches now available. These switches can be toggled at a rate of greater than 1 MHz with super fast t_{on} times (80ns typical) and faster t_{off} times (50ns typical), guaranteeing break before make switching. This family of switches therefore combines the speed of the hybrid FET DG 180 Family with the reliability and low power consumption of a monolithic CMOS construction.

OFF leakages are guaranteed to be less than 100pA at 25°C. No quiescent power is dissipated in either the ON or the OFF state of the switch. Maximum power supply current is 1μA from any supply and typical quiescent currents are in the 10nA range which makes these devices ideal for portable equipment and military applications.

The IH5140 Family is completely compatible with TTL (5V) logic, TTL open collector logic and CMOS logic gates. It is pin compatible with Intersil's IH5040 Family and part of the DG180/190 Famiiy as shown in the switching state diagrams.

ORDERING INFORMATION

Order Part Number	Function	Package	Temperature Range
IH5140 MJE	SPST	16 Pin CERDIP	-55°C to 125°C
IH5140 CJE	SPST	16 Pin CERDIP	0°C to 70°C
IH5140 CPE	SPST	16 Pin Plastic DIP	0°C to 70°C
IH5140 MFD	SPST	14 Pin Flat Pack	-55°C to 125°C
IH5141 MJE	Dual SPST	16 Pin CERDIP	-55°C to 125°C
IH5141 CJE	Dual SPST	16 Pin CERDIP	0°C to 70°C
IH5141 CPE	Dual SPST	16 Pin Plastic DIP	0°C to 70°C
IH5141 MFD	Dual SPST	14 Pin Flat Pack	-55°C to 125°C
IH5141 CTW	Dual SPST	TO-100	0°C to 70°C
IH5141 MTW	Dual SPST	TO-100	-55°C to 125°C
IH5142 MJE	SPDT	16 Pin CERDIP	-55°C to 125°C
IH5142 CJE	SPDT	16 Pin CERDIP	0°C to 70°C
IH5142 CPE	SPDT	16 Pin Plastic DIP	0°C to 70°C
IH5142 MFD	SPDT	14 Pin Flat Pack	-55°C to 125°C
IH5142 CTW	SPDT	TO-100	0°C to 70°C
IH5142 MTW	SPDT	TO-100	-55°C to 125°C
IH5143 MJE	Dual SPDT	16 Pin CERDIP	-55°C to 125°C
IH5143 CJE	Dual SPDT	16 Pin CERDIP	0°C to 70°C
IH5143 CPE	Dual SPDT	16 Pin Plastic DIP	0°C to 70°C
IH5143 MFD	Dual SPDT	14 Pin Flat Pack	-55°C to 125°C
IH5144 MJE	DPST	16 Pin CERDIP	-55°C to 125°C
IH5144 CJE	DPST	16 Pin CERDIP	0°C to 70°C
IH5144 CPE	DPST	16 Pin Plastic DIP	0°C to 70°C
IH5144 MFD	DPST	14 Pin Flat Pack	-55°C to 125°C
IH5144 CTW	DPST	TO-100	0°C to 70°C
IH5144 MTW	DPST	TO-100	-55°C to 125°C
IH5145 MJE	Dual DPST	16 Pin CERDIP	-55°C to 125°C
IH5145 CJE	Dual DPST	16 Pin CERDIP	0°C to 70°C
IH5145 CPE	Dual DPST	16 Pin Plastic DIP	0°C to 70°C
IH5145 MFD	Dual DPST	14 Pin Flat Pack	-55°C to 125°C

Note:
1. Ceramic (side braze) devices also available; consult factory.
2. MIL temp range parts also available with MIL-STD-883 processing.

FUNCTIONAL DIAGRAM

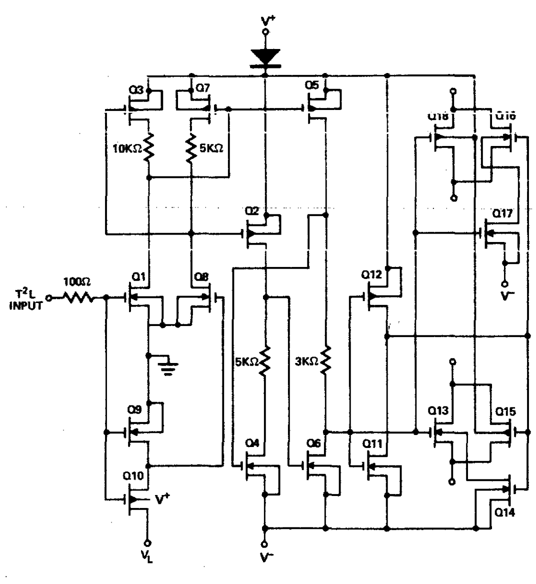
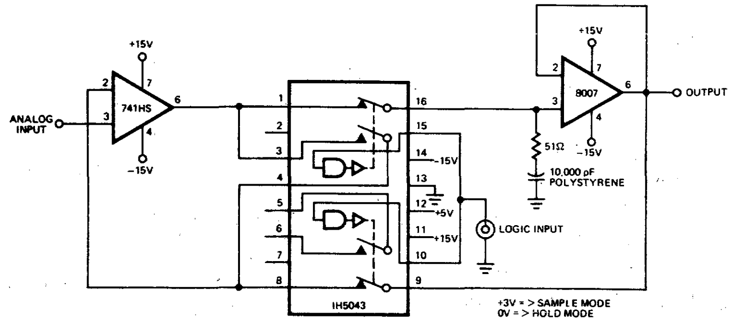


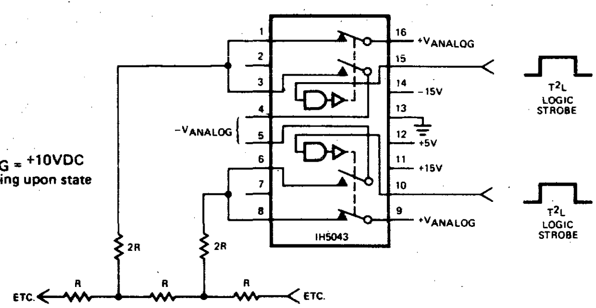
FIGURE 1. Typical Driver/Gate — IH5142

APPLICATIONS

IMPROVED SAMPLE & HOLD
USING IH5043

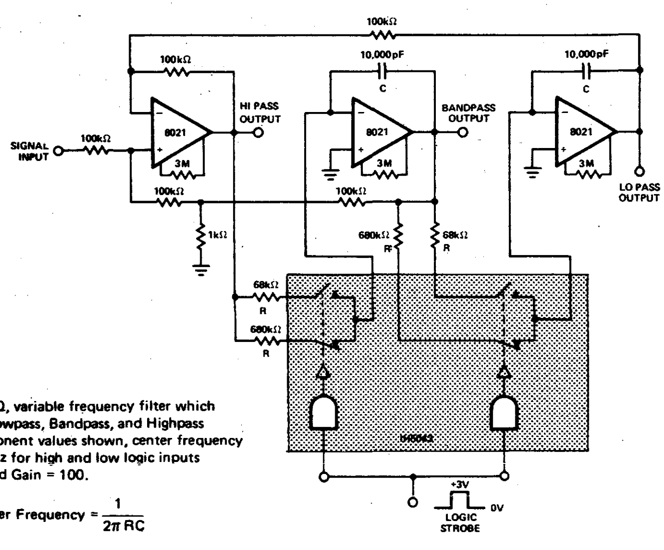


USING THE CMOS SWITCH TO DRIVE
AN R/2R LADDER NETWORK (2 LEGS)



EXAMPLE: If $-V_{ANALOG} = -10VDC$ and $+V_{ANALOG} = +10VDC$ then Ladder Legs are switched between ±10VDC, depending upon state of Logic Strobe.

DIGITALLY TUNED
LOW POWER ACTIVE FILTER



Constant gain, constant Q, variable frequency filter which provides simultaneous Lowpass, Bandpass, and Highpass outputs. With the component values shown, center frequency will be 235Hz and 23.5Hz for high and low logic inputs respectively, Q = 100, and Gain = 100.

$$f_n = \text{Center Frequency} = \frac{1}{2\pi RC}$$

INTERSIL

IH5108

8-Channel Fault Protected CMOS Analog Multiplexer

FEATURES

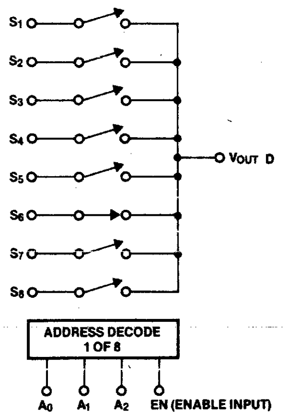
- Ultra low leakage—$I_{D(off)} \leq$ 100pA
- Power supply quiescent current less than 1mA
- ±13V analog signal range
- No SCR latchup
- Break-before-make switching
- Pin compatible with DG508, HI508 and AD7508
- All channels OFF ($I_{ILK} \leq$ 100nA) when power OFF, for analog signals up to ±25V
- Any channel turns OFF ($I_{ILK} \leq$ 100nA) if input exceeds supply rails by up to ±25V. Throughput always < ±14V (±15V supplies)
- TTL and CMOS compatible binary Address and ENable inputs

GENERAL DESCRIPTION

The IH5108 is a dielectrically isolated CMOS monolithic analog multiplexer, designed as a plug-in replacement for the DG508 and similar devices, but adding fault protection to the standard performance. A unique serial MOSFET switch ensures that an OFF channel will remain OFF when the input exceeds the supply rails by up to ±25V, even with the supply voltage at zero. Further, an ON channel will be limited to a throughput of about 1.5V less than the supply rails, thus affording protection to any following circuitry such as op amps, D/A converters, etc. Cross talk onto "good" channels is also prevented.

A binary 3-bit address code together with the ENable input allows selection of any one channel or none at all. These 4 inputs are all TTL compatible for easy logic interface; the ENable input also facilitates MUX expansion and cascading.

FUNCTIONAL DIAGRAM



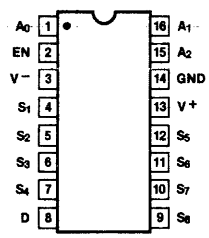
3 LINE BINARY ADDRESS INPUTS
(1 0 1) AND EN HI
ABOVE EXAMPLE SHOWS CHANNEL 6 TURNED ON

DECODE TRUTH TABLE

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

A_0, A_1, A_2, EN
Logic "1" = $V_{AH} \geq 2.4V$
Logic "0" = $V_{AL} \leq 0.8V$

PIN CONFIGURATION (outline dwg JE, PE)



TOP VIEW

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH5108MJE	−55°C to +125°C	16 pin CERDIP
IH5108IJE	−20°C to +85°C	16 pin CERDIP
IH5108CPE	0°C to 70°C	16 pin plastic DIP

IH5140-IH5145 Family

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Current (Any Terminal) .... < 30 mA
Storage Temperature ...... -65°C to +150°C
Operating Temperature .... -55°C to +125°C
Power Dissipation .... 450 mW
(All Leads Soldered to a P.C. Board)
Derate 6 mW/°C Above 70°C
Lead Temperature (Soldering 10 sec.) .. 300°C

V^+-V^- <33V
V^+-V_D <30V
V_D-V^- <30V
V_D-V_S <±22V
V_L-V^- <33V
V_L-V_{IN} <30V
V_L <20V
V_{IN} <20V

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (@ 25°C, V^+ = +15V, V^- = −15V, V_L = +5V)

PER CHANNEL		MIN./MAX. LIMITS							
		MILITARY			COMMERCIAL				
SYMBOL	CHARACTERISTIC	-55°C	+25°C	+125°C	0	+25°C	+70°C	UNITS	TEST CONDITIONS
I_{INH}	Input Logic Current	1	1	1	1	1	1	μA	V_{IN} = 2.4 V Note 1
I_{INL}	Input Logic Current	1	1	1	1	1	1	μA	V_{IN} = 0.8 V Note 1
$r_{DS(on)}$	Drain—Source On Resistance	50	50	75	75	75	100	Ω	I_S = -10 mA V_{ANALOG} = -10 V to +10 V
$\Delta r_{DS(on)}$	Channel to Channel $r_{DS(on)}$ Match		25 (typ)			30 (typ)		Ω	
V_{ANALOG}	Min. Analog Signal Handling Capability		±11			±10		V	
$I_{D(off)}$+ $I_{S(off)}$	Switch OFF Leakage Current	0.1 0.1	0.1 0.1	20 20	0.5 0.5	0.5 0.5	20 20	nA	V_D = +10 V, V_S = -10 V V_D = -10V, V_S = +10 V
$I_{D(on)}$+ $I_{S(on)}$	Switch On Leakage Current	0.2	0.2	40	1	1	40	nA	V_D = V_S = -10 V to +10 V
t_{on} t_{off}	Switch "ON" Time Switch "OFF" Time	See switching time specifications and timing diagrams.							
$Q_{(INJ.)}$	Charge Injection		100			150		pC	See Fig. 4, Note 2
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	f = 1 MHz, R_L = 100Ω, C_L ≤ 5 pF See Fig. 5, Note 2
I^+	+ Power Supply Quiescent Current	1.0	1.0	10.0	10	10	100	μA	
I^-	- Power Supply Quiescent Current	1.0	1.0	10.0	10	10	100	μA	V^+ = +15 V, V^- = -15 V, V_L = +5 V
I_L	+5 V Supply Quiescent Current	1.0	1.0	10.0	10	10	100	μA	See Fig. 6
I_{GND}	Gnd Supply Quiescent Current	1.0	1.0	10.0	10	10	100	μA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off; Any Other Channel Switches See Fig. 7, Note 2

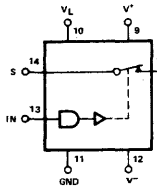
Note: 1. Some channels are turned on by high (1) logic inputs and other channels are turned on by low (0) inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to find logical value of logic input required to produce ON or OFF state.
2. Charge injection, OFF isolation, and Channel to Channel isolation are only sample tested in production.

IH5140-IH5145 Family

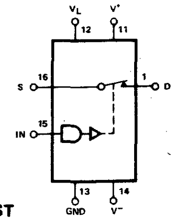
INTERSIL

SWITCHING STATE DIAGRAMS SWITCH STATES ARE FOR LOGIC "1" INPUT

FLATPACK (FD-2)

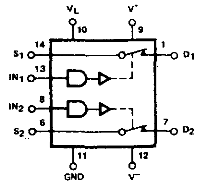


DIP (JE, PE)

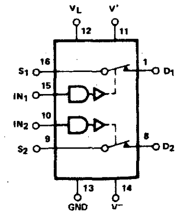


SPST
IH5140 ($r_{DS(on)} < 75\Omega$)

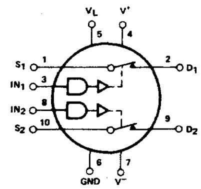
FLATPACK (FD-2)



DIP (JE, PE)

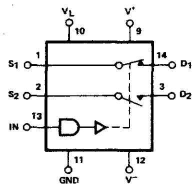


TO-100

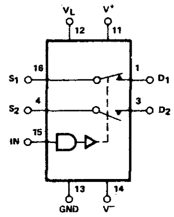


DUAL SPST
IH5141 ($r_{DS(on)} < 75\Omega$)

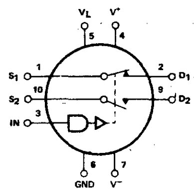
FLATPACK (FD-2)



DIP (JE, PE)

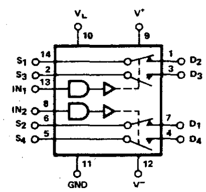


TO-100
(DG188 EQUIVALENT)

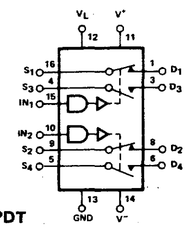


SPDT
IH5142 ($r_{DS(on)} < 75\ \Omega$)

FLATPACK (FD-2)

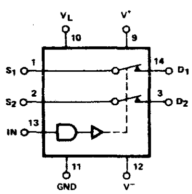


DIP (JE, PE)
(DG191 EQUIVALENT)

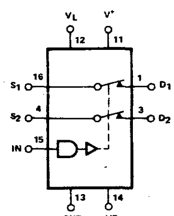


DUAL SPDT
IH5143 ($r_{DS(on)} < 75\Omega$)

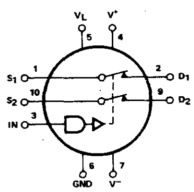
FLATPACK (FD-2)



DIP (JE, PE)

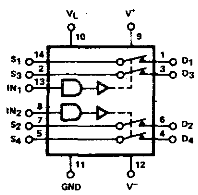


TO-100

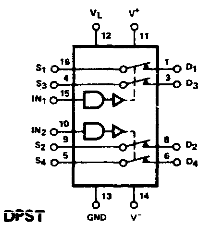


DPST
IH5144 ($r_{DS(on)} < 75\Omega$)

FLATPACK (FD-2)



DIP (JE, PE)
(DG185 EQUIVALENT)



DUAL DPST
IH5145 ($r_{DS(on)} < 75\Omega$)

INTERSIL

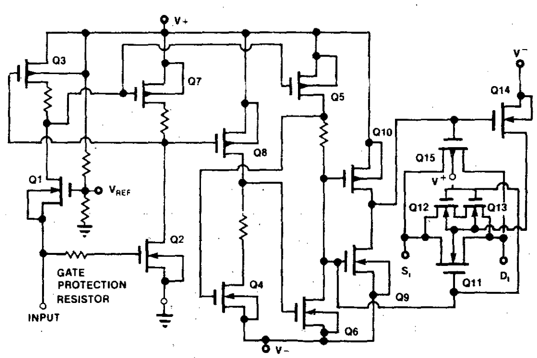
DG200/IH5200
CMOS Dual SPST Analog Switches

FEATURES
- Switches Greater Than 28Vpp Signals With ± 15V Supplies
- Break-Before-Make Switching t_{off} 250 nsec, t_{on} 700nsec Typical
- T^2L, DTL, CMOS, PMOS Compatible
- Non-Latching With Supply Turn-Off
- Complete Monolithic Construction
- Industry Standard (DG200)
- Improved Performance Version (IH5200)

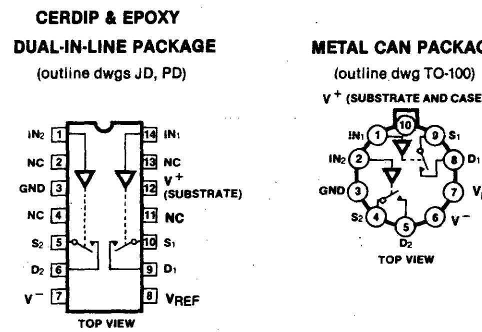
GENERAL DESCRIPTION
The DG200/IH5200 solid state analog gates are designed using an improved, high voltage CMOS monolithic technology. They provide ease-of-use and performance advantages not previously available from solid state switches. Destructive latch-up of solid state analog gates has been eliminated by INTERSIL's CMOS technology.

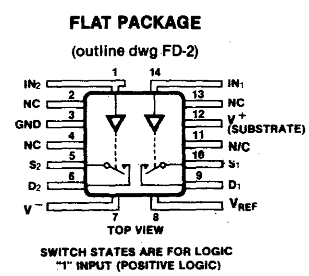
The DG200 is completely spec and pin-out compatible with the industry standard device, while the IH5200 offers significantly enhanced specifications with respect to ON and OFF leakage currents, switching times, and supply current.

SCHEMATIC DIAGRAM (½ DG200/IH5200)



PIN CONFIGURATIONS





ORDERING INFORMATION

INDUSTRY STANDARD PART	IMPROVED SPEC DEVICE	PACKAGE	TEMPERATURE RANGE
DG200AA	IH5200MTW	10-Pin Metal Can	−55 to +125°C
DG200AK	IH5200MJD	14-Pin CERDIP	−55 to +125°C
DG200AL	IH5200MFD	14-Pin Flat Pak	−55 to +125°C
DG200BA	IH5200ITW	10-Pin Metal Can	−25 to +85°C
DG200BK	IH5200IJD	14-Pin CERDIP	−25 to +85°C
DG200BL	IH5200IFD	14-Pin Flat Pak	−25 to +85°C
DG200CJ	IH5200CPD	14-Pin Epoxy DIP	0 to +70°C

INTERSIL

IH5208

4-Channel Differential Fault Protected CMOS Analog Multiplexer

FEATURES

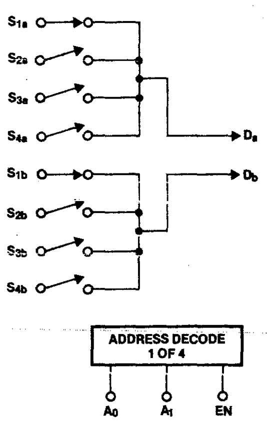
- Ultra low leakage — $I_{D(off)} \leq 100pA$
- Power supply quiescent current less than $1\mu A$
- ±13V analog signal range
- No SCR latchup
- Break-before-make switching
- TTL and CMOS compatible strobe control
- Pin compatible with HI509, DG509 and AD7509
- All channels OFF ($I_{ILK} \leq 100nA$) when power OFF, for analog signals up to ±25V
- Any channel turns OFF ($I_{ILK} \leq 100nA$) if input exceeds supply rails by up to ±25V. Throughput always < ±14V (±15V supplies)
- TTL and CMOS compatible binary Address and ENable inputs

GENERAL DESCRIPTION

The IH5208 is a dielectrically isolated CMOS monolithic analog multiplexer, designed as a plug-in replacement for the DG509 and similar devices, but adding fault protection to the standard performance. A unique serial MOSFET switch ensures that an OFF channel will remain OFF when the input exceeds the supply rails by up to ±25V, even with the supply voltage at zero. Further, an ON channel will be limited to a throughput of about 1.5V less than the supply rails, thus affording protection to any following circuitry such as op amps, D/A converters, etc. Cross talk onto "good" channels is also prevented.

A binary 2-bit address code together with the ENable input allows selection of any channel pair or none at all. These 3 inputs are all TTL compatible for easy logic interface; the ENable input also facilitates MUX expansion and cascading.

FUNCTIONAL DIAGRAM



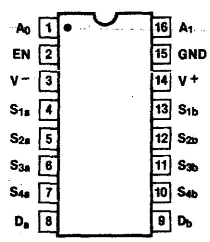
2 LINE BINARY ADDRESS INPUTS
(0 0) AND EN = 1
ABOVE EXAMPLE SHOWS CHANNELS 1a AND 1b ON

DECODE TRUTH TABLE

A_1	A_0	EN	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1a, 1b
0	1	1	2a, 2b
1	0	1	3a, 3b
1	1	1	4a, 4b

A_0, A_1, EN
Logic "1" = $V_{AH} \geq 2.4V$
Logic "0" = $V_{AL} \leq 0.8V$

PIN CONFIGURATION (outline dwg JE, PE)



TOP VIEW

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH5208MJE	−55°C to +125°C	16 pin CERDIP
IH5208IJE	−20°C to +85°C	16 pin CERDIP
IH5208CPE	0°C to 70°C	16 pin plastic DIP

INTERSIL

IH5341
CMOS Monolithic RF/Video Switch

FEATURES

- $r_{ds(on)} < 75\Omega$, flat from DC to 100MHz (< 3dB)
- "OFF" isolation > 60dB @ 10MHz
- Cross coupling isolation > 60dB @ 10MHz
- Directly compatible with TTL, CMOS
- Wide operating power supply range
- Power supply current < 1μA
- "Break-before-Make" switching
- Fast switching (80ns/150ns typ)

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH5341CPD	0 to +70°C	14-Pin DIP
IH5341ITW	−20°C to +85°C	TO-100
IH5341MTW	−55°C to +125°C	TO-100

GENERAL DESCRIPTION

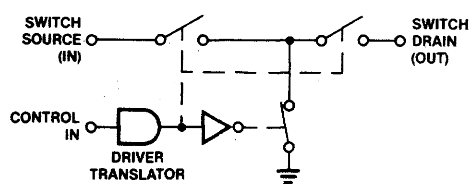
The IH5341 is a dual SPST, CMOS monolithic switch which uses a "Series/Shunt" ("T" switch) configuration to obtain high "OFF" isolation while maintaining good frequency response in the "ON" condition.

Construction of remote and portable video equipment with extended battery life is facilitated by the extremely low current requirements. Switching speeds are typical $t_{on} = 150ns$ and $t_{off} = 80ns$, and guaranteed "Break-before-Make" switching.

Switch "ON" resistance is typically 40Ω-50Ω with ±15V power supplies, increasing to typically 175Ω for ±5V supplies. The devices are available in TO-100 and 14-pin epoxy DIP packages.

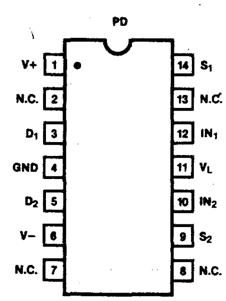
FUNCTIONAL DIAGRAM

Circuit of Switch Channel



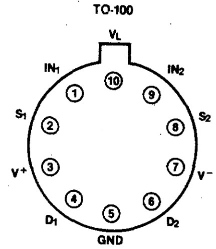
Note: Only one side shown.

PIN CONFIGURATIONS



TOP VIEW

TO-100



TOP VIEW

IH5341

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Supply Voltages V^+ and V^- .... ±17V
Current in any Terminal 50mA
Analog Input Voltage .... V^+ to V^-
Operating Temperature
  (M Version) .... −55°C to +125°C
  (I Version) .... −20°C to +85°C
  (C Version) .... 0 to +70°C

Storage Temperature .... −65°C to +160°C
Power Dissipation 250mW
  Derate above 25°C @ .... 7.5mW/°C
Logic Control Voltage .... V^+ to V^-
Voltage on Pin 10 .... V^+ to V^-
Lead Temperature (soldering, 10 seconds) .... 300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS $V^+ = +15V$, $V_L = +5V$, $V^- = -15V$, $T_A = 25°C$ unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	TYP	M GRADE DEVICE			I/C GRADE DEVICE			UNITS
				−55°C	+25°C	+125°C	−20/0°C	+25°C	+85/+70°C	
Supply Voltage Ranges										
Positive Supply	V^+		4.5>16		5 to 15			5 to 15		V
Logic Supply	V_L	(Note 3)	4.5>V^+		5 to V^+			5 to V^+		
Negative Supply	V^-		−4> −16		−5 to −15			−5 to −15		
Switch "ON" Resistance (Note 4)	$r_{ds(on)}$	V_D −5V to +5V		75	75	100	75	75	100	Ω
		I_S = 10mA, V_{IN} = 2.4V								
		V_D −15V to +15V		125	125	175	150	150	175	
Switch "ON" Resistance	$r_{ds(on)}$	$V^+ = V_L = 5V$, $V_{IN} = 3V$, $V^- = 5V$, $V_D = ±5V$		250	250	350	300	300	350	
On Resistance Match		I_S = 10mA, V_D = ±5V	5							
Switch "OFF" Leakage (Notes 2 and 4)	$I_{D(off)}$ or $I_{S(off)}$	$V_{S/D}$ = +5V to −5V		0.1	0.1	20	0.5	0.5	20	nA
		V_{IN} = 0.8V								
		$V_{S/D}$ = +14V to −14V		0.2	0.2	50	1.0	1.0	100	
Switch "ON" Leakage	$I_{D(on)}$ + $I_{S(on)}$	V_D = +5V or −5V		0.3	0.3	50	1.0	1.0	40	
		V_{IN} = 2.4V								
		V_D = +14V to −14V		0.5	0.5	100	1.0	1.0	100	
Input Logic Current	I_{IN}	V_{IN} > 2.4V or < 0		1	1	10	1	1	10	µA
Positive Supply Quiescent Current	I^+	V_{IN} = 0V or +5V		1	1	10	1	1	10	
Negative Supply Quiescent Current	I^-	V_{IN} = 0V or +5V		1	1	10	1	1	10	
Logic Supply Quiescent Current	I_L	V_{IN} = 0V or +5V		1	1	10	1	1	10	

Note 1: Typical values are not tested in production. They are given as a design aid only.
Note 2: Positive and negative voltages applied to opposite sides of switch, in both directions successively.
Note 3: These are the operating voltages at which the other parameters are tested, and are not directly tested.
Note 4: The logic inputs are either greater than or equal to 2.4V or less than or equal to 0.8V, as required, for this test.

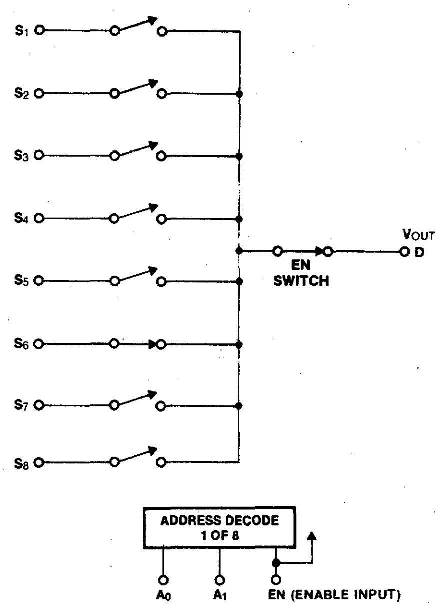
INTERSIL

IH6108
8-Channel CMOS Analog Multiplexer

FEATURES
- Ultra Low Leakage — $I_{D(off)} \leq 100pA$
- $r_{DS(on)} < 400$ ohms over full signal and temperature range
- Power supply quiescent current less than 100μA
- ±14V analog signal range
- No SCR latchup
- Break-before-make switching
- Binary Address control (3 Address inputs control 8 channels)
- TTL and CMOS compatible strobe control
- Pin compatible with DG508, HI-508 & AD7508

GENERAL DESCRIPTION
The IH6108 is a CMOS monolithic, one of 8 multiplexer. The part is a plug-in replacement for the DG508. Three line binary decoding is used so that the 8 channels can be controlled by 3 Address inputs; additionally a fourth input is provided to use as a system enable. When the ENable input is high (5V) the channels are sequenced by the 3 line Address inputs, and when low (0V) all channels are off. The 3 Address inputs are controlled by TTL logic or CMOS logic elements, a "0" corresponding to any voltage greater than 2.4V. Note that the ENable input (EN) must be taken to 5V to enable the system and less than 0.8V to disable the system.

FUNCTIONAL DIAGRAM



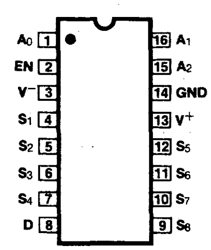
3 LINE BINARY ADDRESS INPUTS
(1 0 1) AND EN @ 5V
ABOVE EXAMPLE SHOWS CHANNEL 6 TURNED ON

DECODE TRUTH TABLE

A_2	A_1	A_0	EN	ON SWITCH
x	x	x	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

A_0, A_1, A_2
Logic "1" = $V_{AH} \geq 2.4V$ $V_{ENH} \geq 4.5V$
Logic "0" = $V_{AL} \leq 0.8V$

PIN CONFIGURATION



ORDERING INFORMATION

Ceramic package available as special order only (IH6108MDE/CDE)

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH6108MJE	−55°C to +125°C	16 pin CERDIP
IH6108CJE	0°C to 70°C	16 pin CERDIP
IH6108CPE	0°C to 70°C	16 pin plastic DIP

IH6108

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground .... −15V to 15V
V_S or V_D to V^+ .... 0, −32V
V_S or V_D to V^- 0, 32V
V^+ to Ground 16V
V^- to Ground .... −16V
Current (Any Terminal) .... 30 mA
Current (Analog Source or Drain) .... 20 mA
Operating Temperature .... −55 to 125°C
Storage Temperature .... −65 to 150°C
Lead Temp (Soldering, 10 sec) .... 300°C
Power Dissipation (Package)* .... 1200 mW

*All leads soldered or welded to PC board. Derate 10 mW/°C above 70°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS $V^+ = 15V$, $V^- = -15V$, $V_{EN} = +5V$ (Note 1), Ground = 0V, unless otherwise specified.

	CHARACTERISTIC	MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	MAX LIMITS M SUFFIX 55°C	M SUFFIX 25°C	M SUFFIX 125°C	C SUFFIX 0°C	C SUFFIX 25°C	C SUFFIX 70°C	UNIT	TEST CONDITIONS	
SWITCH	$r_{DS(ON)}$	S to D	8	180	300	300	400	350	350	450	Ω	$V_D = 10V$, $I_S = -1.0mA$	Sequence each switch on
			8	150	300	300	400	350	350	450		$V_D = -10V$, $I_S = -1.0mA$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$
	$\Delta r_{DS(ON)}$			20							%	$\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)avg.}}$ $V_S = \pm 10V$	
	$I_{S(OFF)}$	S	8	0.002		0.05	50		0.1	50	nA	$V_S = 10V$, $V_D = -10V$	$V_{EN} = 0$
			8	0.002		0.05	50		0.1	50		$V_S = -10V$, $V_D = 10V$	
	$I_{D(OFF)}$	D	1	0.03		0.1	100		0.2	100		$V_D = 10V$, $V_S = -10V$	
			1	0.03		0.1	100		0.2	100		$V_D = -10V$, $V_S = 10V$	
	$I_{D(ON)}$	D	8	0.1		0.2	100		0.4	100		$V_{S(All)} = V_D = 10V$	Sequence each switch on
			8	0.1		0.2	100		0.4	100		$V_{S(All)} = V_D = -10V$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$
INPUT	$I_{AN(ON)}$ or $I_{A(on)}$	A_0, A_1 or A_2	3	.01		−10	−30		−10	−30	μA	$V_A = 2.4V$ or 0V	
	$I_{AN(OFF)}$ $I_{A(off)}$	Inputs	3	.01		10	30		10	30		$V_A = 15V$ or 0V	
	I_A	A_0 A_1 A_2	3			−10	−30		−10	−30		$V_{EN} = 5V$	All $V_A = 0$ (Address pins)
		EN	1			−10	−30		−10	−30		$V_{EN} = 0$	
DYNAMIC	$t_{transition}$	D		0.3		1					μs	See Fig. 1	
	t_{open}	D		0.2								See Fig. 2	
	$t_{on(EN)}$	D		0.6		1.5						See Fig. 3	
	$t_{off(EN)}$	D		0.4		1							
	"OFF" Isolation	D		60							dB	$V_{EN} = 0$, $R_L = 200\Omega$, $C_L = 3pF$, $V_S = 3$ VRMS, f = 500 kHz	
	$C_{s(off)}$	S		5							pF	$V_S = 0$	$V_{EN} = 0V$, f = 140 kHz to 1 MHz
	$C_{d(off)}$	D		25								$V_D = 0$	
	$C_{DS(off)}$	D to S		1								$V_S = 0$, $V_D = 0$	
SUPPLY	Supply Current +	V^+	1	40		200			1000		μA	$V_{EN} = 5V$	All $V_A = 0$ or 5V
	Supply Current −	V^-	1	2		100			1000				
	Standby Current +	V^+	1	1		100			1000			$V_{EN} = 0$	
	Standby Current −	V^-	1	1		100			1000				

NOTE 1: See Enable Input Strobing Levels, Section 1.

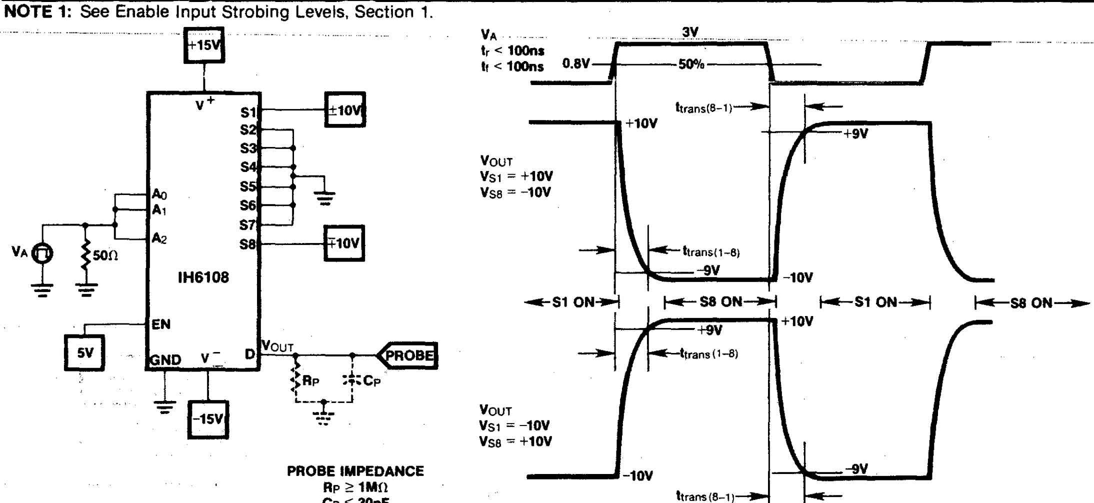


Figure 1. $t_{transition}$ Switching Test

INTERSIL

IH6116

16-Channel CMOS Analog Multiplexer

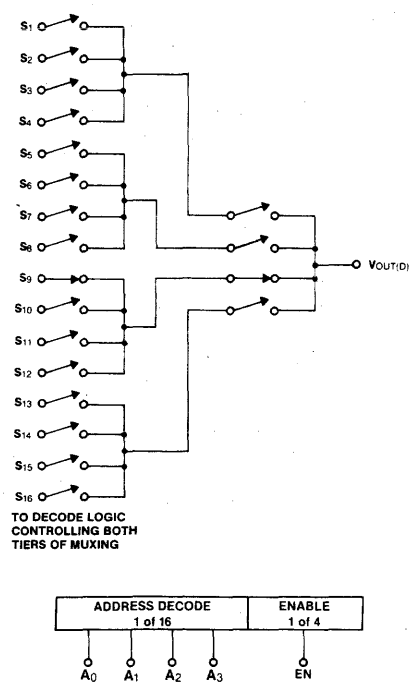
FEATURES

- **Pin compatible with DG506, HI-506 & AD7506**
- **Ultra Low Leakage — $I_{D(off)} \leq$ 100pA**
- **±11 analog signal range**
- **$r_{DS(on)}$ <700 ohms over full signal and temperature range**
- **Break-before-make switching**
- **TTL and CMOS compatible Address control**
- **Binary Address control (4 Address inputs control 16 channels)**
- **Two tier submultiplexing to facilitate expandability**
- **Power supply quiescent current less than 100μA**
- **No SCR latchup**

GENERAL DESCRIPTION

The IH6116 is a CMOS monolithic, one of 16 multiplexer. The part is a plug-in replacement for the DG506. Four line binary decoding is used so that the 16 channels can be controlled by 4 Address inputs; additionally a fifth input is provided to use as system enable. When the ENable input is high (5V) the channels are sequenced by the 4 line Address inputs, and when low (0V), all channels are off. The 4 Address inputs are controlled by TTL logic or CMOS logic elements with a "0" corresponding to any voltage less than 0.8V and a "1" corresponding to any voltage greater than 3.0V. Note that the ENable input must be taken to 5V to enable the system and less than 0,8V to disable the system.

FUNCTIONAL DIAGRAM



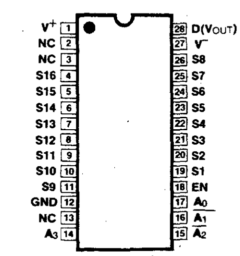
4 LINE BINARY ADDRESS INPUTS
(0 0 0 1) AND EN @ 5V
ABOVE EXAMPLE SHOWS CHANNEL 9 TURNED ON

DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	EN	ON SWITCH
x	x	x	x	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

Logic "1" = $V_{AH} \geq$ 3.0V $V_{ENH} \geq$ 4.5V
Logic "0" = $V_{AL} \leq$ 0.8V

PIN CONFIGURATION



TOP VIEW
V+ COMMON TO SUBSTRATE

ORDERING INFORMATION

Ceramic package available as special order only (IH6116MDI/CDI)

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH6116MJI	−55°C to +125°C	28 pin CERDIP
IH6116CJI	0°C to 70°C	28 pin CERDIP
IH6116CPI	0°C to 70°C	28 pin Plastic DIP

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground .... −15V to 15V
V_S or V_D to V^+ .... 0, −32V
V_S or V_D to V^- 0, 32V
V^+ to Ground 16V
V^- to Ground .... −16V
Current (Any Terminal) .... 30 mA
Current (Analog Source or Drain) .... 20 mA
Operating Temperature .... −55 to 125°C
Storage Temperature .... −65 to 150°C
Lead Temperature (Soldering, 10 secs) .... 300°C
Power Dissipation (Package)* .... 1200 mW

*All leads soldered or welded to PC board. Derate 10 mW/°C above 70°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

$V^+ = 15V$, $V^- = -15V$, $V_{EN} = +5V$ (Note 1), Ground = 0V, unless otherwise specified.

	CHARACTERISTIC	MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	MAX LIMITS M SUFFIX −55°C	M SUFFIX 25°C	M SUFFIX 125°C	C SUFFIX 0°C	C SUFFIX 25°C	C SUFFIX 70°C	UNIT	TEST CONDITIONS	
SWITCH	$r_{DS(ON)}$	S to D	16	480	600	600	700	650	650	750	Ω	$V_D = 10V$, $I_S = -10mA$	Sequence each switch on
			16	300	600	600	700	650	650	750		$V_D = -10V$, $I_S = 10mA$	$V_{AL} = 0.8V$, $V_{AH} = 3V$
	$\Delta r_{DS(ON)}$			20							%	$\Delta r_{DS(on)} = \frac{r_{DS(on)max} - r_{DS(on)min}}{r_{DS(on)avg.}}$ $V_S = \pm 10V$	
	$I_{S(OFF)}$	S	16	0.01		0.1	50		0.2	50	nA	$V_S = 10V$, $V_D = -10V$	$V_{EN} = 0$
			16	0.01		0.1	50		0.2	50		$V_S = -10V$, $V_D = 10V$	
	$I_{D(OFF)}$	D	1	0.1		0.2	100		0.4	100		$V_D = 10V$, $V_S = -10V$	
			1	0.1		0.2	100		0.4	100		$V_D = -10V$, $V_S = 10V$	
	$I_{D(ON)}$	D	16	0.1		0.2	100		0.4	100		$V_{S(All)} = V_D = 10V$	Sequence each switch on
			16	0.1		0.2	100		0.4	100		$V_{S(All)} = V_D = -10V$	$V_{AL} = 0.8V$, $V_{AH} = 3V$
INPUT	$I_{A(on)}$ or $I_{A(off)}$		4	.01		−10	−30		−10	−30	μA	$V_A = 3.0V$	
			4	.01		10	30		10	30		$V_A = 15V$	
	I_A	A_0 A_1 A_2 A_3	4			−10	−30		−10	−30		$V_{EN} = 5V$	All $V_A = 0$
		EN	1			−10	−30		−10	−30		$V_{EN} = 0$	
DYNAMIC	t_{trans}	D		0.6		1					μs	See Fig. 1	
	t_{open}	D		0.2								See Fig. 2	
	$t_{EN(on)}$	D		0.8		1.5						See Fig. 3	
	$t_{EN(off)}$	D		0.3		1							
	"OFF" Isolation	D		60							dB	$V_{EN} = 0$, $R_L = 200Ω$, $C_L = 3pF$, $V_S = 3$ VRMS, f = 500 kHz	
	$C_s(OFF)$	S		5							pF	$V_S = 0$	$V_{EN} = 0$, f = 140 kHz to 1 MHz
	$C_d(OFF)$	D		40								$V_D = 0$	
	$C_{ds}(OFF)$	D to S		1								$V_S = 0$, $V_D = 0$	
SUPPLY	Supply Current +	V^+	1	55		200			1000		μA	$V_{EN} = 5V$	All $V_A = 0$ or 3V
	Supply Current −	V^-	1	2		100			1000				
	Standby Current +	V^+	1	1		100			1000			$V_{EN} = 0$	
	Standby Current −	V^-	1	1		100			1000				

NOTE 1: See Section V. Enable Input Strobing Levels.

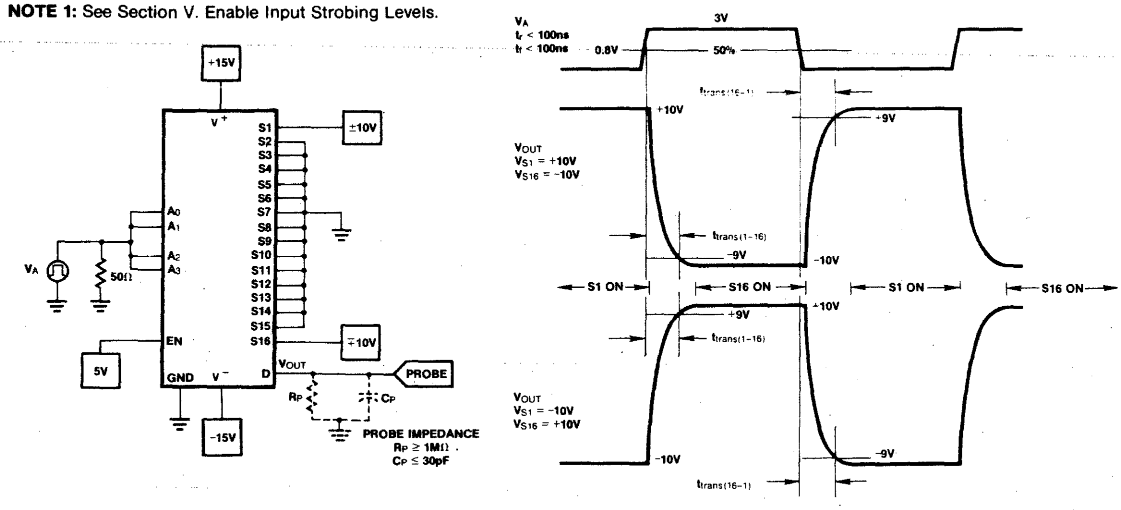


Figure 1

INTERSIL

IH6208

4-Channel Differential CMOS Analog Multiplexer

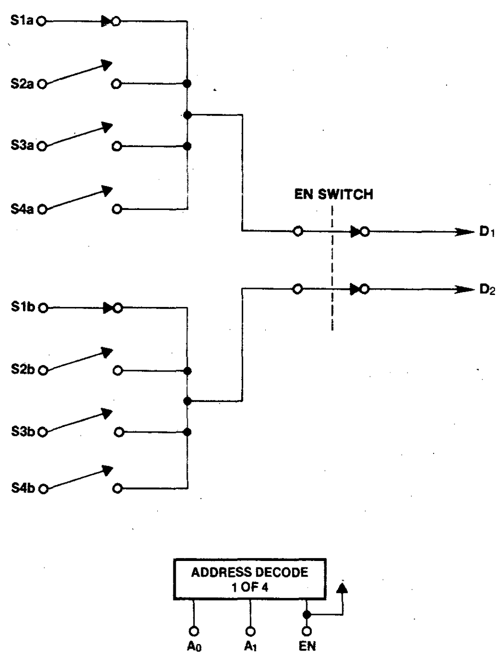
FEATURES

- **Ultra low leakage — $I_{D(off)} \leq$ 100pA**
- **$r_{DS(on)}$ < 400 ohms over full signal and temperature range**
- **Power supply quiescent current less than 100μA**
- **±14V analog signal range**
- **No SCR latch up**
- **Break-before-make switching**
- **Binary Address control (2 Address inputs control 2 out of 8 channels)**
- **TTL and CMOS compatible Address control**
- **Pin compatible with HI509, DG509 & AD7509**

GENERAL DESCRIPTION

The IH6208 is a monolithic 2 of 8 CMOS multiplexer. The part is a plug-in replacement for the DG509. Two line binary decoding is used so that the 8 channels can be controlled in pairs by the binary inputs; additionally a third input is provided to use as a system enable. When the ENable input is high (5V) the channels are sequenced by the 2 line binary inputs, and when low (0V) all channels are off. The 2 Address inputs are controlled by TTL logic or CMOS logic elements with a "0" corresponding to any voltage less than 0.8V and a "1" corresponding to any voltage greater than 2.4V. Note that the ENable input must be taken to 5V to enable the system, and less than 0.8V to disable the system.

FUNCTIONAL DIAGRAM



2 LINE BINARY ADDRESS INPUTS
(0 0) AND EN = 5V (EN = "1" FOR +5V, "0" FOR 0V)
ABOVE EXAMPLE SHOWS CHANNELS 1a & 1b ON.

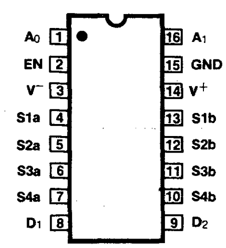
DECODE TRUTH TABLE

A_1	A_0	EN	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1a, 1b
0	1	1	2a, 2b
1	0	1	3a, 3b
1	1	1	4a, 4b

A_0, A_1

LOGIC "1" = $V_{AH} \geq 2.4V$ $V_{ENH} \geq 4.5V$
LOGIC "0" = $V_{AL} \leq 0.8V$

PIN CONFIGURATION



ORDERING INFORMATION

Ceramic package available as special order only (IH6208MDE/CDE)

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH6208MJE	-55°C to +125°C	16 pin CERDIP
IH6208CJE	0°C to 70°C	16 pin CERDIP
IH6208CPE	0°C to 70°C	16 pin Plastic DIP

INTERSIL

IH6216

8-Channel Differential CMOS Analog Multiplexer

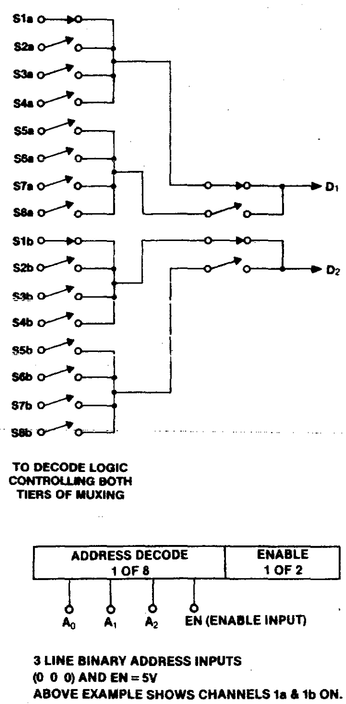
FEATURES

- Pin compatible with HI507, DG507 & AD7507
- ±11V analog signal range
- $r_{DS(on)}$ < 700 ohms over full signal and temperature range
- Break-before-make switching
- TTL and CMOS compatible Address control
- Binary Address control (3 Address inputs control 2 out of 16 channels)
- Two tier submultiplexing to facilitate expandability
- Power supply quiescent current less than 100μA
- No SCR latch up
- Very low leakage $I_{D(off)} \leq$ 100pA

GENERAL DESCRIPTION

The IH6216 is a CMOS monolithic 2 of 16 multiplexer. The part is a plug-in replacement for the DG507. Three line binary decoding is used so that the 16 channels can be controlled in pairs by the binary inputs; additionally a fourth input is provided to use as a system enable. When the ENable input is high (5V) the channels are sequenced by the 3 line binary inputs, and when low (0V) all channels are off. The 3 Address inputs are controlled by TTL logic or CMOS logic elements with a "0" corresponding to any voltage less than 0.8V and a "1" corresponding to any voltage greater than 3.0V. Note that the ENable input must be taken to 5V to enable the system and less than 0.8V to disable the system.

FUNCTIONAL DIAGRAM

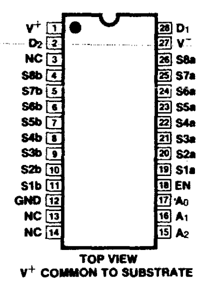


DECODE TRUTH TABLE

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

LOGIC "1" = V_{AH} > 3V V_{ENH} > 4.5V
LOGIC "0" = V_{AL} < 0.8V

PIN CONFIGURATION



ORDERING INFORMATION

Ceramic package available as special order only (IH6216MDI/CDI)

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH6216MJI	−55°C to +125°C	28 pin CERDIP
IH6216CJI	0°C to 70°C	28 pin CERDIP
IH6216CPI	0°C to 70°C	28 pin Plastic DIP

INTERSIL

IM6402/IM6403 Universal Asynchronous Receiver Transmitter (UART)

FEATURES

- Low Power — Less Than 10mW Typ. at 2MHz
- Operation Up to 4MHz Clock (IM6402A)
- Programmable Word Length, Stop Bits and Parity
- Automatic Data Formatting and Status Generation
- Compatible with Industry Standard UART's (IM6402)
- On-Chip Oscillator with External Crystal (IM6403)
- Operating Voltage —
  IM6402-1/03-1: 5V
  IM6402A/03A: 4-11V
  IM6402/03: 5V

GENERAL DESCRIPTION

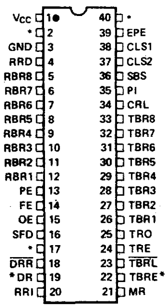
The IM6402 and IM6403 are CMOS/LSI UART's for interfacing computers or microprocessors to asynchronous serial data channels. The receiver converts serial start, data, parity and stop bits to parallel data verifying proper code transmission, parity, and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity, and stop bits.

The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even, and parity checking and generation can be inhibited. The stop bits may be one or two (or one and one-half when transmitting 5 bit code). Serial data format is shown in Figure 6.

The IM6402 and IM6403 can be used in a wide range of applications including modems, printers, peripherals and remote data acquisition systems. CMOS/LSI technology permits clock frequencies up to 4.0MHz (250K Baud), an improvement of 10 to 1 over previous PMOS UART designs. Power requirements, by comparison, are reduced from 670mW to 10mW. Status logic increases flexibility and simplifies the user interface.

The IM6402 differs from the IM6403 in the use of five device pins as indicated in Table 1 and Figure 1.

PIN CONFIGURATION (outline dwg DL, PL)



*See Table 1

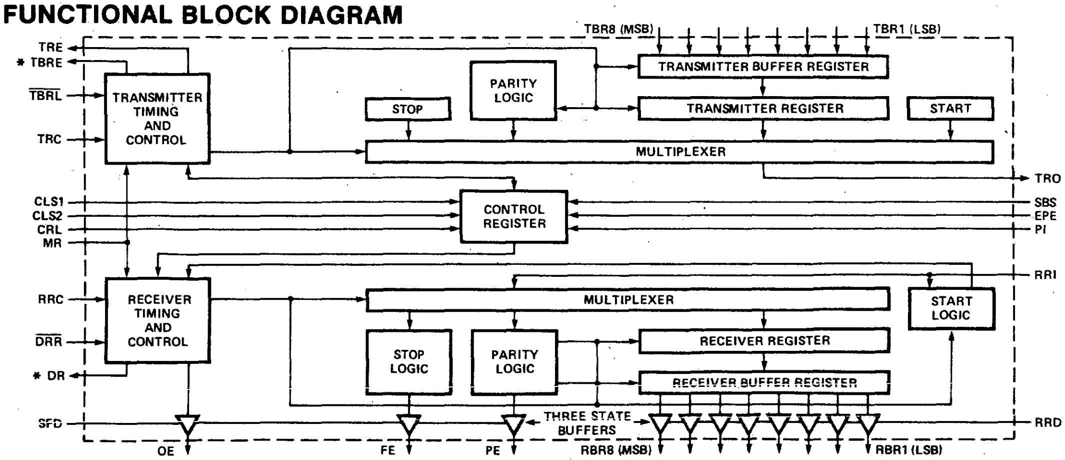
TABLE 1

PIN	IM6402	IM6403 w/XTAL	IM6403 w/EXT CLOCK
2	N/C	Divide Control	Divide Control
17	RRC	XTAL	External Clock Input
19	Tri-State	Always Active	Always Active
22	Tri-State	Always Active	Always Active
40	TRC	XTAL	GND

ORDERING INFORMATION

ORDER CODE	IM6402-1/03-1	IM6402A/03A	IM6402/03
PLASTIC PKG	IM6402-1/03-1IPL	IM6402/03-AIPL	IM6402/03-IPL
CERAMIC PKG	IM6402-1/03-1IDL	IM6402/03-AIDL	IM6402/03IDL
MILITARY TEMP.	IM6402-1/03-1MDL	IM6402/03-AMDL	—
MILITARY TEMP. WITH 883B	IM6402-1/03-1 MDL/883B	IM6402/03-AMDL/ 883B	—

FUNCTIONAL BLOCK DIAGRAM



* These outputs are three state (IM6402) or always active (IM6403)

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A DIVISION OF UNITRODE CORPORATION
324 Clark St., Worcester, MA 01606, TEL: (617) 852-5400

REGIONAL SALES OFFICE

324 CLARK STREET
WORCESTER, MA 01606
PHONE (617) 852-5400
TWX 710-340-0067 TLX 951808

Suite 460
13999 Goldmark
Dallas, Texas 75240
Phone (214) 231-1340
TWX 910-867-4738

15011 Park Way Loop
Suite F
Tustin, California 92680
Phone (714) 730-8021
TWX 910-595-1999

EUROPEAN OFFICE

Unitrode S.R.L.
Via Dei Carracci 5
20149 Milano Italy
Phone 39-2-434604
TLX 310085 UNITRD I

The Micro Networks Division of Unitrode Corporation is an established world leader in the design, development and manufacturing of high-performance, thin and thick-film, hybrid microcircuits for data acquisition/conversion applications. We are the largest supplier of such devices for military/aerospace applications, and are rapidly developing new processing technologies that will enable us to extend our reputation for quality and reliability to the high volume commercial/industrial marketplace. In the first half of 1984, for example, we will introduce the MN565A 12-bit D/A - our first monolithic data converter.

- Analog to Digital Converters
- Digital to Analog Converters
- Track and Hold Amplifiers
- Data Acquisition Systems
- Instrumentation Amplifiers
- Programmable-Gain Amplifiers

Data Acquisition System Selection Guide

RESOLUTION	DESCRIPTION	MODEL#	INPUT CHANNELS	ACQUISITION TIME to ±½LSB (μsec)	CONVERSION TIME (μsec)	THROUGHPUT (Channels/sec)	MAXIMUM LINEARITY ERROR (%FSR)	POWER (mW)	PKG.	SPECIFIED TEMP RANGE (°C)	MIL-STD-883 HI-REL OPTION
8 Bits	Complete 8 bit DAS, 8-Channel Mux, T/H, A/D, 3-State Buffer	**MN7120**	8 (Expandable)	5	6	90,000	±0.2	680	32 Pin	0 to +70 −55 to +125	Yes
12 Bits	16-Channel Multiplexer, Instrumentation Amp and T/H in DIP Package (Use with 12-Bit A/D to Configure a Low-Cost 2 Package DAS	**MN7130**	16 (Expandable)	6.5	—	—	±0.002	900	32 Pin	0 to +70 −55 to +125	Yes
	Complete 12-Bit DAS, Industry Standard 40-Pin DIP, for Military/Aerospace Applications	**MN7140**	8 (Expandable)	8	40	20,000	±0.012	900	40 Pin	0 to +70 −25 to +85 −55 to +125	Yes
✔	Complete 8 or 16-Channel DAS, Instru. Amp, T/H, A/D, 3-State Buffers, HDAS-8/16 Compatible	**MN7150-8** **MN7150-16**	8 16 (Expandable)	9	9	50,000	±0.012	1875	62 Pin	0 to +70 −25 to +85 −55 to +125	Yes

✔ = **New Product**

Instrumentation and Programmable-Gain Amplifier Selection Guide

GAIN RANGES	DESCRIPTION	MODEL#	MAX GAIN ERROR (%)	OFFSET VOLTAGE (RTI, μV)	OFFSET DRIFT (μV/°C)	SMALL SIGNAL BW (kHz)	POWER (mW)	SPECIFIED TEMP RANGE (°C)	PKG.	MIL-STD-883 HI-REL OPTION
1, 10, 100, 1000 Internal, 1 to 1000 with External Resistor	Precision Amp with Internal Gain Scaling Resistors, Excellent Gain Accuracy Over Temp.	**MN2200**	±0.01 to ±0.1 Depending on Range	±100 (G = 100)	±0.6 (G = 100)	750 (G = 1)	240	−25 to +85 −55 to +125	18 Pin	Yes
1, 2, 4, 8, 16, 32, 64, 128 Digitally Programmed	Digitally-Controlled Programmable-Gain Amplifier. Binary Weighted Gains Are Set with a 3-Bit Digital Word	**MN2020**	±0.005 to ±0.2 Depending on Range	±100	±5	5000 (G = 1)	275	0 to +70 −55 to +125	18 Pin	Yes

A/D Converter Selection Guide

	RESOLUTION	DESCRIPTION	MODEL#	MAXIMUM CONVERSION TIME (μsec) (1)	INTERNAL CLOCK	SPECIFIED TEMP RANGE (°C)	MAXIMUM LINEARITY ERROR (%FSR)	NO MISSING CODES OVER TEMP	INPUT RANGES (Volts)	POWER (mW)	PKG.	MIL-STD-883 HI-REL OPTION
✓	16 Bits	High Performance Guaranteed Over Extended Temperatures	MN5290 MN5291	40	Yes	0 to +70 −25 to +85 −55 to +125	±0.003	Yes (2) Yes (3)	6 Ranges	830	32 Pin	Yes
		General Purpose, Fast, Low Cost	MN5280 MN5282	100 50	Yes	0 to +70	±0.003	Yes (3)	6 Ranges	1400	32 Pin	No
✓		Ultra Low Power, 15-Bit Performance, ±12V Supplies	MN5284	50	Yes	0 to +70 −25 to +85	±0.003	Yes(4)	4 Ranges	150	40 Pin	Yes
	14 Bits	Ultra Low Power, TTL and CMOS Compatible, 24-Pin DIP	MN5260	250	No	0 to +70	±0.003	Yes (3)	±10	215	24 Pin	No
✓	12 Bits	Serial-Parallel Technique, Fastest 12-Bit DIP A/D Available, TTL, 3-State	MN5247 MN5248	0.5	(5)	0 to +70 −55 to +125	±0.012	Yes	0 to +5 ±2.5	2055	40 Pin	Yes
✓		Serial-Parallel Technique, Extremely Fast, TTL Compatible	MN5245 MN5246	1	(5)	0 to +70 −25 to +85 −55 to +125	±0.012	Yes	0 to +5 ±2.5	2055	40 Pin	Yes
✓		Low-Cost, ADC85 Pin-Compatible, Internal or External Clock	MN5243 MN5244	2	Yes No	0 to +70 −25 to +85 −55 to +125	±0.012	Yes	6 Ranges	2000	32 Pin	Yes
		Fast, Internal Clock, No Missing Codes, ADC85 Pin-Compatible	MN5240	5	Yes	0 to +70 −25 to +85	±0.012	Yes	5 Ranges	1400	32 Pin	Yes
		Fast, Internal Clock, Industry Standard for Industrial Applications	ADC84 ADC85	8	Yes	0 to +70 −25 to +85	±0.012	Yes	5 Ranges	1400	32 Pin	Yes
		ADC85 Pin-Compatible, Guaranteed −55°C to +125°C Operation	ADC87	10	Yes	−25 to +85 −55 to +125	±0.012	Yes	5 Ranges	1075	32 Pin	Yes
		Most Widely Used 12-Bit A/D for Military/Aerospace Applications, Fast	MN5210 Series	13	No	0 to +70 −55 to +125	±0.012	Yes	4 Ranges	695	24 Pin	Yes
		Industry-Standard Military A/D in Leadless Package	MN5610 Series	13	No	0 to +70 −55 to +125	±0.012	Yes	4 Ranges	695	24 Pin Leadless	Yes
		Industry Standard, Low Cost, Complete A/D	ADC80	25	Yes	0 to +70	±0.012	Yes	5 Ranges	950	32 Pin	No
✓		μP-Compatible, Address Decoding, 3-State, Low Cost	MN574A	35	Yes	0 to +70 −55 to +125	±0.012	Yes	4 Ranges	450	28 Pin	Yes
		Lower Cost Version of Industry Standard MN5210 Series	MN5200 Series	50	No	0 to +70 −55 to +125	±0.012	Yes	4 Ranges	695	24 Pin	Yes
		Extremely Low Power, Widely Used in Satellite and Battery Applications	MN5250 Series	175	No	0 to +70 −55 to +125	±0.012	Yes	4 Ranges	56	24 Pin	Yes
		Fully Guaranteed Performance −55°C to +200°C	MN5700	250	No	−55 to +200	±0.012	Yes (6)	4 Ranges	311	32 Pin	Yes
✓	8 Bits	Succ. Approx. A/D High Speed, Low Cost	MN5815 MN5825	0.7 1	Yes	0 to +70 −55 to +125	±0.2	Yes	6 Ranges	925	24 Pin	Yes
		Very Fast, Widely Used in Avionics Applications	MN5101 MN5100	0.9 1.5	No	0 to +70 −55 to +125	±0.2	Yes	9 Ranges	1125	24 Pin	Yes
		Fast, Low Cost Popular, 18-Pin DIP	MN5130 Series	2.5	No	0 to +70 −55 to +125	±0.2	Yes	4 Ranges	680	18 Pin	Yes
		±12V Supplies for Microprocessor and CMOS Applications	MN5140 Series	2.5	No	0 to +70 −55 to +125	±0.2	Yes	4 Ranges	680	18 Pin	Yes
		Internal 3-State Output Buffer for Data Bus Applications	MN5150	2.5	No	0 to +70 −55 to +125	±0.2	Yes	7 Ranges	680	24 Pin	Yes
		Most Popular 8-Bit A/D for Industrial and Military Applications	MN5120 Series	6	No	0 to +70 −55 to +125	±0.2	Yes	4 Ranges	680	18 Pin	Yes
		Ultra Low Power, Single +12V Supply, TTL and CMOS Compatible	MN5065 MN5066	100	No	0 to +70 −55 to +125	±0.2	Yes	±5 0 to +10	53	18 Pin	Yes

✓ = **New Product**

1. For units with an external clock, the table shows the minimum conversion time that will result in specified accuracy. For units with internal clock, maximum conversion time is given.
2. No Missing Codes for 14 bits guaranteed over temperature.
3. No Missing Codes for 14 bits guaranteed at +25°C. No Missing Codes for 13 bits guaranteed over temperature.
4. No Missing Codes for 15 bits guaranteed over temperature.
5. The serial-parallel conversion technique does not require a clock.
6. No Missing Codes for 10 bits guaranteed at +200°C.

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D/A Converter Selection Guide

RESOLU-TION	DESCRIPTION	MODEL#	MAXIMUM SETTLING TIME (μsec) (1)	INTERNAL REF. AND OUTPUT OP AMP	SPECIFIED TEMP RANGE (°C)	MAXIMUM LINEARITY ERROR (%FSR)	MONOTONIC OVER TEMP	OUTPUT RANGES (Volts)	POWER (mW)	PKG.	MIL-STD-883 HI-REL OPTION
16 Bits	Industry Standard for Industrial Applications	DAC71	10	Yes (2)	0 to +70	±0.003	(Note 3)	2V Ranges 2I Ranges	850	24 Pin	No
✔ 12 Bits	Industry-Standard Monolithic D/A, Current Output, On-Chip Reference	MN565A	0.25	Yes (2)	0 to +70 −55 to +125	±0.012	Yes	0 to −2mA ±1mA	225	24 Pin	Yes
	Industry Standard, Low Cost	DAC80	3 (Typ)	Yes	0 to +70	±0.012	Yes	5V Ranges 2I Ranges	850	24 Pin	No
	Industry Standard, Binary Coding, Voltage/Current Output	DAC85-CBI	3 (Typ)	Yes	0 to +70 −25 to +85	±0.012	Yes	5V Ranges 2I Ranges	850	24 Pin	Yes
	Industry Standard, 3 Decade BCD, Voltage/Current Output	DAC85-CCD	3 (Typ)	Yes	0 to +70 −25 to +85	±0.012	Yes	0 to +9.99 0 to −1.25mA	850	24 Pin	Yes
	Industry-Standard 12-Bit D/A for Military/Aerospace Applications	DAC87	4	Yes	−25 to +85 −55 to +125	±0.012	Yes	5 Ranges	900	24 Pin	Yes
	12-Bit D/A With Fast Input Register	DAC HK (4)	4 (Typ)	Yes	0 to +70 −55 to +125	±0.0012	Yes	5 Ranges	975	24 Pin	Yes
✔	Military-Standard Latched D/A in Leadless Package	MN3660 (5)	10	Yes	0 to +70 −55 to +125	±0.012	Yes	0 to +10 ±5, ±10	495	24 Pin Leadless	Yes
	For Military/Aerospace and Other High Reliability Applications	MN3850	7	Yes	0 to +70 −55 to +125	±0.012	Yes	5 Ranges	525	24 Pin	Yes
	Fast Input Register, For Military/Aerospace Hi-Rel Applications	MN3860 (5)	7	Yes	0 to +70 −55 to +125	±0.012	Yes	0 to +10 ±5, ±10	675	24 Pin	Yes
	Low-Cost, Low-Power, Superior Second Source for the DAC349	MN3349	10	Yes	0 to +70 −55 to +125	±0.012	(Note 6)	5 Ranges	195	24 Pin	Yes
	Low Cost, Low Power, DAC349 Compatible	MN3348	8	Yes	0 to +70 −55 to +125	±0.012	(Note 6)	5 Ranges	195	24 Pin	Yes
	12-Bit D/A Converter with Fast Input Register, Hi-Rel and Industrial Applications	DAC88 (5)	10	Yes	0 to +70 −55 to +125	±0.012	Yes	0 to +10 ±5, ±10	495	24 Pin	Yes
	4 Quadrant Multiplying, Voltage Output, High Accuracy	MN3412	20	(Note 7)	0 to +70 −55 to +125	±0.012	Yes	±10	335	32 Pin Module	Yes
	Industry-Standard Low-Power D/A, Voltage Output	MN370 MN371	60 35	Yes	0 to +70 −55 to +125	±0.012	Yes	−10 to +10 0 to +10	60	18 Pin	Yes
10 Bits	Fast Input Latch for Hi-Rel μP Applications	MN3040 (5)	10	Yes	0 to +70 −55 to +125	±0.05	Yes	0 to −10 ±10	450	18 Pin	Yes
	Excellent for Servo Applications, Very Accurate Zero	MN3003 Series	30	Yes	0 to +70 −55 to +125	±0.05	Yes	4 Ranges	450	16 Pin	Yes
✔ 8 Bits	Produces Composite Video Signal for Raster-Scan Displays	MN0805	8nsec	Yes (2)	−25 to +85	±0.2	Yes	0 to −17mA (8)	1660	24 Pin	Yes
	Fast Settling, 30 V/μsec Slew Rate	MN3008 MN3009	1	Yes	0 to +70 −55 to +125	±0.2	Yes	0 to +4 ±2	495	16 Pin	Yes
	Fast Input Latch, Popular in Avionics Applications, Complete in 18-Pin DIP	MN3020 (5)	3	Yes	0 to +70 −55 to +125	±0.2	Yes	4 Ranges	505	18 Pin	Yes
	Popular, Low Cost, General Purpose, Multirange	MN3013 MN3014	30 2.5	Yes	0 to +70 −55 to +125	±0.2	Yes	4 Ranges	420	16 Pin	Yes
	Excellent for Servo Applications, Very Accurate Zero, Small 14-Pin DIP	MN3000 Series	30	Yes	0 to +70 −55 to +125	±0.2	Yes	4 Ranges	450	14 Pin	Yes
✔ 6 Bits	Composite Video for Raster-Scan Displays	MN0605	6nsec	Yes (2)	−25 to +85	±0.8	Yes	0 to −17mA (8)	1350	24 Pin	Yes
✔ 4 Bits	Composite Video for Raster-Scan Displays	MN0405	4nsec	Yes (2)	−25 to +85	±3.2	Yes	0 to −17mA (8)	1040	24 Pin	Yes

✔ = New Product

1. Full scale change settling to ± ½LSB.
2. Current-output devices have no output op amps
3. Monotonicity for 14 bits guaranteed over temperature.
4. Latch timing parameters: minimum setup time 50nsec, maximum hold time 0nsec, minimum latch enable pulse width 60nsec.
5. Latch timing parameters: minimum setup time 40nsec, maximum hold time 0nsec, minimum latch enable pulse width 60nsec.
6. Monotonicity guaranteed at 25°C.
7. Internal output op amp.
8. Produces standard 1Vp-p video signal when driving 75Ω load.

Track-Hold Amplifier Selection Guide

7-9 Bit Applications

	MAXIMUM LINEARITY ERROR (%)	ACQUISITION TIME	GAIN AND VOLTAGE RANGE	DESCRIPTION	MODEL #	SPECIFIED TEMP RANGE (°C)	APERTURE JITTER (psec, max)	DROOP RATE ($\mu V/\mu s$)	POWER (mW)	PKG.	MIL-STD-883 HI-REL OPTION
✓	±0.1	35nsec 5V Step to ±0.1%	+1, ±2.5V	Ultra Fast, Designed to Drive Flash Converters, 500pF Cap Loading	MN379	0 to +70 −55 to +125	2	±500	1575	24 Pin	Yes

10-12 Bit Applications

	MAXIMUM LINEARITY ERROR (%)	ACQUISITION TIME	GAIN AND VOLTAGE RANGE	DESCRIPTION	MODEL #	SPECIFIED TEMP RANGE (°C)	APERTURE JITTER (psec, max)	DROOP RATE ($\mu V/\mu s$)	POWER (mW)	PKG.	MIL-STD-883 HI-REL OPTION
✓	±0.01	100nsec 5V Step to ±0.1%	−1, ±5V	Package Contains User-Optional Pin-Programmable Input Buffer	MN050	0 to +70 −55 to +125	100	±0.1	1400	24 Pin	Yes

12-Bit Applications

	MAXIMUM LINEARITY ERROR (%)	ACQUISITION TIME	GAIN AND VOLTAGE RANGE	DESCRIPTION	MODEL #	SPECIFIED TEMP RANGE (°C)	APERTURE JITTER (psec, max)	DROOP RATE ($\mu V/\mu s$)	POWER (mW)	PKG.	MIL-STD-883 HI-REL OPTION
✓	±0.01	90nsec 10V Step to ±0.01%	−1, ±10V	Fastest ±0.01% T/H Available, TTL Compatible	MN377	0 to +70 −55 to +125	50	±2	875	24 Pin	Yes
✓	±0.01	160nsec 10V Step to ±0.01%	−1, ±10V	Second Fastest ±0.01% T/H Available, TTL Compatible	MN376	0 to +70 −55 to +125	100	±0.5	730	24 Pin	Yes
✓	±0.01	250nsec 10V Step to ±0.01%	−1, ±10V	Third Fastest ±0.01% T/H, HTC-0300A Compatible	MN0300A	0 to +70 −55 to +125	100	±5	730	24 Pin	Yes
	±0.005	500nsec 10V Step to ±0.01%	−1, ±5V	Precision T/H Suitable for High-Speed 12-14 Bit Applications	MN375	0 to +70 −25 to +85	100	±0.5	1325	24 Pin	Yes
	±0.01	1μsec 10V Step to ±0.01%	−1, ±10V	Fast, Low Cost, Internal Hold Capacitor, 14-Pin DIP	MN346	0 to +70 −55 to +125	30 (1)	±0.1	640	14 Pin	Yes
	±0.01	1μsec 10V Step to ±0.05%	−1, ±10V	Fast, Low Cost, Internal Hold Capacitor, 14-Pin DIP	MN347	0 to +70 −55 to +125	30 (1)	±0.5	640	14 Pin	Yes
	±0.01	6.5μsec 20V Step to ±0.01%	−1, ±10V	16-Channel Mux, Instru. Amp and T/H in a Single DIP (Use with A/D to Make 2 Package DAS)	MN7130	0 to +70 −55 to +125	60 (1)	±4	900	32 Pin	Yes
	±0.01	7.5μsec 10V Step to ±0.01%	−1, ±10V	Moderate Speed, Very Low Droop, Internal Hold Capacitor	MN343	0 to +70 −55 to +125	60 (1)	±0.1	345	14 Pin	Yes
	±0.01	7.5μsec 10V Step to ±0.05%	−1, ±10V	Low Cost, Low Droop Internal Hold Capacitor	MN344	0 to +70 −55 to +125	60 (1)	±0.4	345	14 Pin	Yes

(1) Listed Specification is Aperture Delay Time

13-16 Bit Applications

	MAXIMUM LINEARITY ERROR (%)	ACQUISITION TIME	GAIN AND VOLTAGE RANGE	DESCRIPTION	MODEL #	SPECIFIED TEMP RANGE (°C)	APERTURE JITTER (psec, max)	DROOP RATE ($\mu V/\mu s$)	POWER (mW)	PKG.	MIL-STD-883 HI-REL OPTION
	±0.005	700nsec 10V Step to ±0.005%	−1, ±5V	Precision T/H Suitable for 12-14 Bit Applications	MN375	0 to +70 −25 to +85	100	±0.5	1325	24 Pin	Yes
✓	±0.003	8.5μsec 10V Step to ±0.003%	−1, ±10V	Precision T/H Compatible with MN5290, MN5291, MN5282 and other 16-Bit DIP A/D's	MN373	0 to +70 −55 to +125	1000	±0.5	300	14 Pin	Yes

✓ = New Product

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MICRO POWER SYSTEMS

D/A and A/D Converters

Note: See other MPS parts in Linear and Military Sections.

Digital-to-Analog Converters

- □ Second source to Analog Devices and PMI
- □ Improved temperature drift characteristics
- □ Superior stability — no laser trimming on monolithic DAC's
- □ .5 ppm gain tempco for MP7621

Model	Type	Resolution	Accuracy	Gain Tempco	Settling Time (typ)	Output	Power Dissipation	Replaces
MP370	CMOS, High Resolution	18 Bit	±.0008%	2 ppm	2 µsec	Current	60 mW (typ)	DAC-370-18
MP377-18	CMOS, Buffered, Complete	18 Bit	±.0008%	5 ppm	20 µsec	Voltage	500 mW (max)	DAC-377-18
MP562	Bipolar, Low Power	12 Bit	±.006%	5 ppm	1.5 µsec	Current	200 mW (typ)	AD562
MP1208	CMOS, µP Compatible	12 Bit	±.012%	2 ppm	1 µsec	Current	20 mW (typ)	DAC1208
MP1230	CMOS, µP Compatible	12 Bit	±.012%	2 ppm	1 µsec	Current	20 mW (typ)	DAC1230
MP3140	CMOS, Multiplying	14 Bit	±.006%	2 ppm	2 µsec	Current	30 mW (max)	HS3140
MP5520	CMOS and Bipolar, Internal amp and reference	6 Bit	±.2%	±80 ppm	3 µsec	Voltage	250 mW (max)	DAC01
MP7520	CMOS, Multiplying	10 Bit	±.05%	2 ppm	500 nsec	Current	20 mW (typ)	AD7520
MP7521	CMOS, Multiplying	12 Bit	±.05%	2 ppm	500 nsec	Current	20 mW (typ)	AD7521
MP7522	CMOS, µP Compatible, Double buffered input	10 Bit	±.05%	10 ppm	500 nsec	Current	20 mW (typ)	AD7522
MP7523	CMOS, Multiplying, Low Cost	8 Bit	±.05%	10 ppm	150 nsec	Current	10 mW (typ)	AD7523
MP7524	CMOS, µP Compatible, Latched input	8 Bit	±.05%	10 ppm	100 nsec	Current	10 mW (typ)	AD7524
MP7528	CMOS, Buffered Multiplying	8 Bit	±.02%	10 ppm	80 nsec	Current	15 mW (max)	AD7528
MP7530	CMOS, Multiplying, Low Cost	10 Bit	±.05%	2 ppm	500 nsec	Current	20 mW (typ)	AD7530
MP7531	CMOS, Multiplying, Low Cost	12 Bit	±.05%	2 ppm	500 nsec	Current	20 mW (typ)	AD7531
MP7533	CMOS, Multiplying, Low Cost	10 Bit	±.05%	2 ppm	600 nsec	Current	30 mW (typ)	AD7533
MP7541	CMOS, Multiplying	12 Bit	±.012%	2 ppm	1 µsec	Current	20 mW (typ)	AD7541
MP7542	CMOS, µP Compatible	12 Bit	±.012%	2 ppm	1 µsec	Current	20 mW (typ)	AD7542
MP7543	CMOS, Serial Input	12 Bit	±.012%	2 ppm	1 µsec	Current	20 mW (typ)	AD7543
MP7645	CMOS, Buffered Multiplying	12 Bit	±.012%	2 ppm	1 µsec	Current	20 mW (typ)	AD7545
MP7614	CMOS, Multiplying	14 Bit	±.006%	10 ppm	2 µsec	Current	40 mW (typ)	
MP7616	CMOS, Multiplying	16 Bit	±.006%	10 ppm	2 µsec	Current	40 mW (typ)	
MP7621	CMOS, Untrimmed, Multiplying	12 Bit	±.012%	.5 ppm	1 µsec	Current	20 mW (typ)	AD7541
MP7622	CMOS, Multiplying, Double Buffered	12 Bit	±.012%	2 ppm	1 µsec	Current	40 mW (typ)	HS3120
MP7623	CMOS, Multiplying	12 Bit	±.012%	.5 ppm	1 µsec	Current	20 mW (typ)	AD7541A
MP9331	CMOS, High Resolution	16 Bit	±.0008%	2 ppm	2 µsec	Current	60 mW (typ)	DAC-9331-16
MP9377-16	CMOS, Buffered, Complete	16 Bit	±.0008%	5 ppm	20 µsec	Voltage	500 mW (max)	DAC-9377-16
MP8526	Complete Bipolar DAC	13 Bit	±.006%	10 ppm	5 µsec	Voltage	300 mW	

Analog-to-Digital Converters

- □ Second source to Analog Devices
- □ Bright display digital panel meter
- □ Microprocessor compatible

Model	Type	Resolution	Accuracy	Conversion Time	Outputs	Power Dissipation	Replaces
MP574	CMOS, Complete, µP Interface	12 Bit	±.012	25 µsec	Parallel, Tristate	600 mW	AD574
MP7138	CMOS 3½ Digit Panel Meter	100 µV	±.05%	100 msec	BCD	10 mW (typ)	—
MP7550	CMOS, Quadslope, 2's Complement	13 Bit	±1 LSB	40 msec	Parallel	9 mW	AD7550
MP7570	CMOS, Successive Approximation	10 Bit	±.05%	40 µsec	Tristate, Serial & Parallel	40 mW	AD7570
MP7574	CMOS, Successive Approximation	8 Bit	±3/4 LSB	15 µsec	Tristate, Binary	25 mW	AD7574
MP7581	CMOS, 8 Channel, 8 Bit	8 Bit	±1/2 LSB		Tristate, Binary	40 mW (max)	AD7581

All Micro Power Systems' IC's are available with 883B processing, in dice form, or to customer's specifications.

MICRO POWER SYSTEMS
3100 Alfred Street
Santa Clara, CA 95050
(408) 727-5350

Note: See other MPS parts in Linear and Military Sections.

Analog Multiplexers

- Second source to Harris and Siliconix
- Low leakage; dielectric isolation
- 25 volt over-voltage protection
- Low ON resistance

NOTE: Dielectrically isolated switches are indicated by "DI" suffix.

Model	Type	Temperature Ranges	Packages	R_{ON} (max, full temp)	Off Output Leakage (max, full temp)	Access Time (typ, 25°C)	Replaces
MP7501	8 Channel	All	All	375 ohm	250 nA	800 nsec	AD7501
MP7502	4 Channel Diff.	All	All	375 ohm	125 nA	800 nsec	AD7502
MP7503	8 Channel (Inv. Enable)	All	All	375 ohm	250 nA	800 nsec	AD7503
MP7506	16 Channel	All	All	500 ohm	500 nA	800 nsec	AD7506 DG506
MP7507	8 Channel Diff.	All	All	500 ohm	250 nA	800 nsec	AD7507 DG507
MP7508DI	8 Channel	All	All	350 ohm	500 nA	500 nsec	HI508A DG508
MP7509DI	4 Channel Diff.	All	All	350 ohm	500 nA	500 nsec	HI509A DG509

Analog Switches

- Second source to Analog Devices, Harris and Siliconix
- Low ON resistance

NOTE: Dielectrically isolated switches are indicated by "DI" suffix.

Model	Type	Temperature Ranges	Packages	Off Output Leakage (max, full temp)	R_{ON} (max, full temp)	Switch ON Time (typ, 25°C)	Power Dissipation (typ, 25°C)	Replaces
MP200DI	Dual, SPST	All	All	500 nA	100 ohm	240 nsec	15 mW	DG200 HI200 MP7513
MP201DI	Quad, SPST	All	All	500 nA	125 ohm	185 nsec	15 mW	DG201 HI201 MP7516
MP7510DI	Quad, SPST	All	All	500 nA	175 ohm	180 nsec	3 mW	AD7510DI
MP7511DI	Quad, SPST	All	All	500 nA	175 ohm	180 nsec	3 mW	AD7511DI
MP7512DI	Dual, SPDT	All	All	500 nA	175 ohm	180 nsec	3 mW	AD7512DI

All Micro Power Systems' IC's are available with 883B processing, in dice form, or to customer's specifications.

MICRO POWER SYSTEMS
3100 Alfred Street
Santa Clara, CA 95050
(408) 727-5350

MITEL

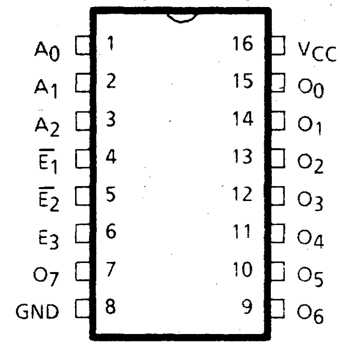
MD54/74HCT138R
1 of 8 Octal Decoder/Demultiplexer
Preliminary Information

October '83

Features

- High latch-up immunity
- High current outputs can drive 15 LSTTL loads
- Low power ISO-CMOS technology
- Meets or exceeds all proposed JEDEC 40.2 specifications
- Fully TTL compatible inputs and outputs
- Pin compatible with 54/74LS138 types

CONNECTION DIAGRAM
DIP (TOP VIEW)



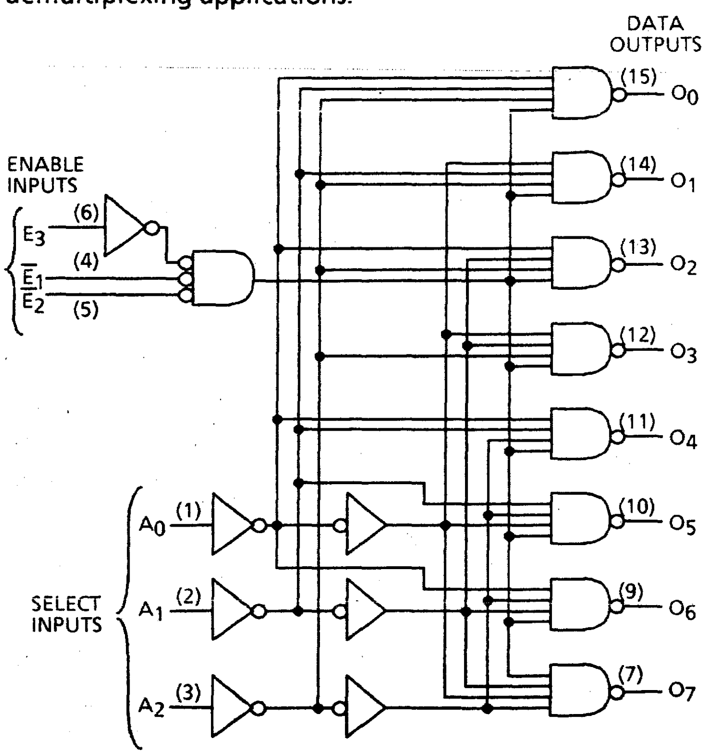
Description

This ISO-CMOS, MSI circuit is designed for use in high speed memory and peripheral address decoding systems. The MD54/74HCT138 will decode 3 binary inputs (A_0, A_1,A_2) to select one of eight mutually exclusive outputs (O_0 - O_7). Three enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3), reduce the need for external gates in an expanded system. A 1 of 32 decoder requires only four of these devices and one external inverter. The enable inputs can be used as the data input for demultiplexing applications.

Ordering Information

MD54HCT138RCB, Cerdip
-55°C to 125°C
with MIL 883B option

MD74HCT138RE, Plastic Dip
-40°C to 85°C



FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
E_3	$\overline{E}_1$	$\overline{E}_2$	A_2	A_1	A_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = logic "1", L = logic "0", X = don't care

MD54/74HCT139R

Dual 1 of 4 Decoder/Demultiplexer

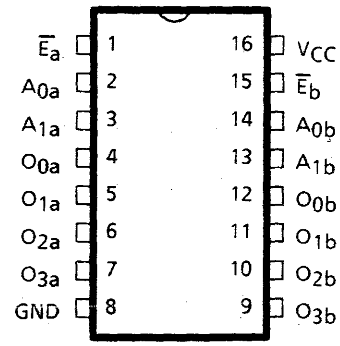
Preliminary Information

October '83

Features

- High latch-up immunity
- High current outputs can drive 15 LSTTL loads
- Low power ISO-CMOS technology
- Meets or exceeds all proposed JEDEC 40.2 specifications
- Fully TTL compatible inputs and outputs
- Pin compatible with 54/74LS139 types

CONNECTION DIAGRAM
DIP (TOP VIEW)



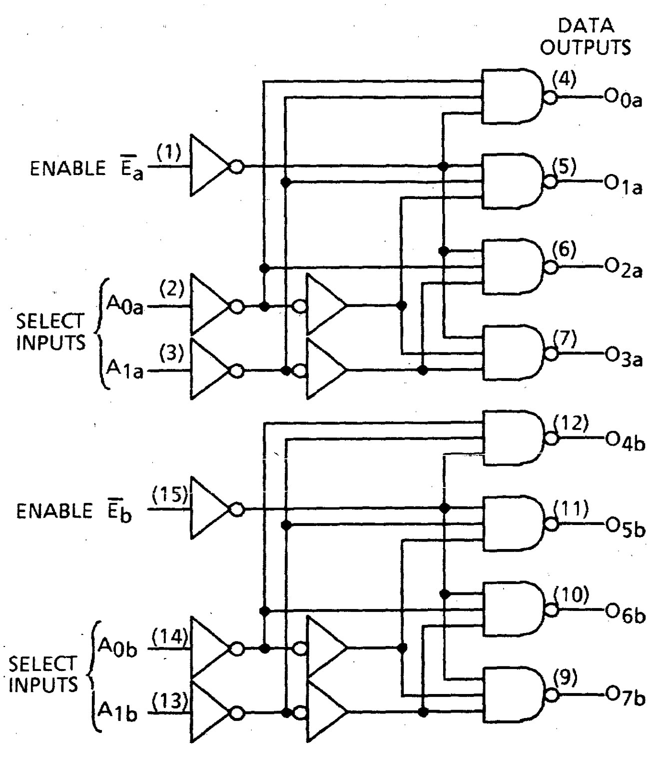
Ordering Information

MD54HCT139RCB, Cerdip
-55°C to 125°C
with MIL 883B option

MD74HCT139RE, Plastic Dip
-40°C to 85°C

Description

This ISO-CMOS, MSI circuit is designed for use in high speed memory and peripheral, address decoding systems. The MD54/74HCT139 will decode 2 binary inputs (A_0, A_1) to select one of four mutually exclusive outputs (O_0 - O_3). The enable inputs, active LOW ($\overline{E}_a$, $\overline{E}_b$) independantly control the two separate 1 of 4 decoder/demultiplexers.



FUNCTION TABLE
(each decoder/demultiplexer)

INPUTS			OUTPUTS			
ENABLE	SELECT					
$\overline{E}$	A_1	A_0	O_0	O_1	O_2	O_3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = logic "1", L = logic "0", X = don't care

MITEL

MD54/74HCT240R

Inverting Octal Line Driver/Buffer

Preliminary Information

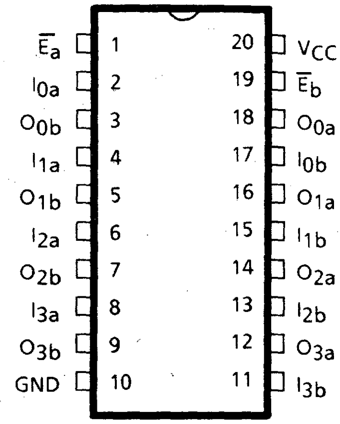
October '83

Features

- High latch-up immunity
- High current outputs can drive 30 LSTTL loads
- Low power ISO-CMOS technology
- Bus oriented 3-state outputs
- Meets or exceeds all proposed JEDEC 40.2 specifications
- Fully TTL compatible inputs and outputs
- Pin compatible with 54/74LS240 types

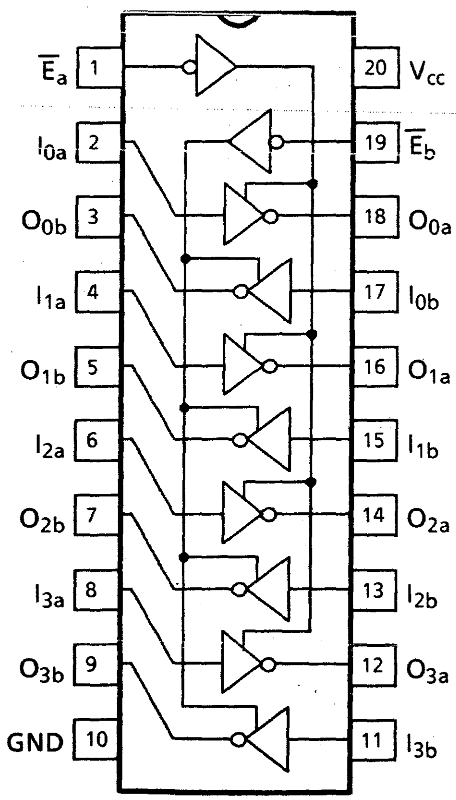
CONNECTION DIAGRAM

DIP (TOP VIEW)



Description

These ISO-CMOS Octal line driver/buffers are designed to improve P.C. board density and performance in three-state memory address drivers, clock drivers, and bus oriented receivers/transmitters. The MD54/74HCT240R offers inverting three-state buffers controlled by two active low enable pins.



Ordering Information

MD54HCT240RCB, Cerdip
-55°C to 125°C
with MIL 883B option

MD74HCT240RE, Plastic Dip
-40°C to 85°C

PIN	DESCRIPTION
$\overline{E}_a$, $\overline{E}_b$	Data Output Enable
I_{0a} to I_{3a}	Data Inputs (a)
I_{0b} to I_{3b}	Data Inputs (b)
O_{0a} to O_{3a}	Data Outputs (a)
O_{0b} to O_{3b}	Data Outputs (b)
V_{CC}	Supply Voltage
GND	System Ground

TRUTH TABLE (A or B buffers)

INPUTS		OUTPUTS
$\overline{E}$	I_{0-3}	O_{0-3}
L	L	H
L	H	L
H	X	Z

H = logic "1", L = logic "0", X = don't care,
Z = high impedance

MITEL

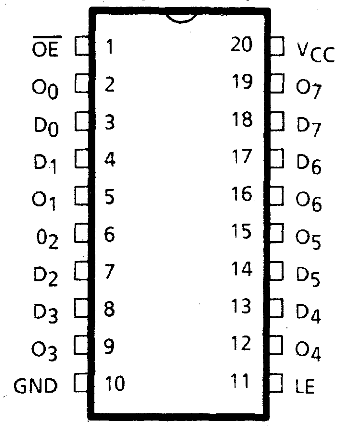
MD54/74HCT373R
Octal D-Type Transparent Latch
Preliminary Information

October '83

Features

- High latch-up immunity
- High current outputs can drive 30 LSTTL loads
- Low power ISO-CMOS technology
- Bus oriented 3-state outputs
- Meets or exceeds all proposed JEDEC 40.2 specifications
- Fully TTL compatible inputs and outputs
- Pin compatible with 54/74LS373 types

CONNECTION DIAGRAM
DIP (TOP VIEW)



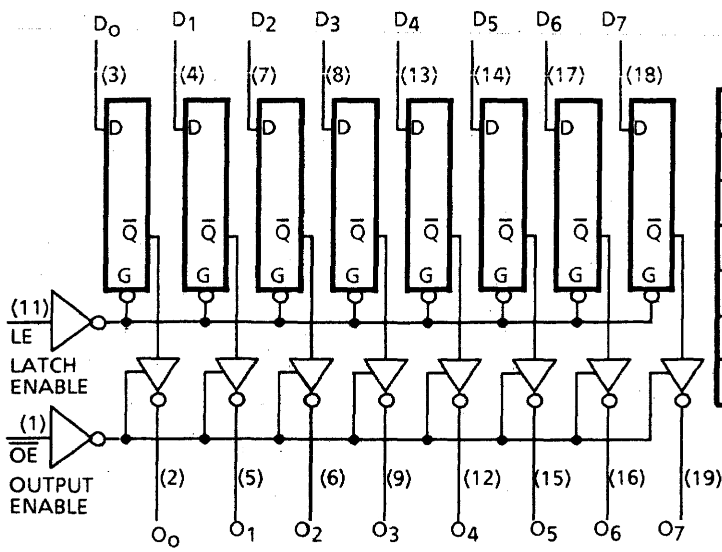
Description

This 8-bit latch features 3-state operation and is designed for use in high speed, bus oriented, systems. The MD54/74HCT373R appears transparent to data (outputs change asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, data meeting the set up times becomes latched. The state of the latches is unaffected by the active low Output Enable ($\overline{OE}$) pin, but when $\overline{OE}$ is HIGH the outputs are put into high impedance. Data may thus be latched even when the device is deselected.

Ordering Information

MD54HCT373RCB, Cerdip
-55°C to 125°C
with MIL 883B option

MD74HCT373RE, Plastic Dip
-40°C to 85°C



PIN FUNCTION

PIN	DESCRIPTION
D_0 to D_7	Data Inputs
O_0 to O_7	Data Outputs
LE	Latch Enable
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage
GND	System Ground

MITEL

MD54/74HCT374R

Octal D-Type Flip Flop

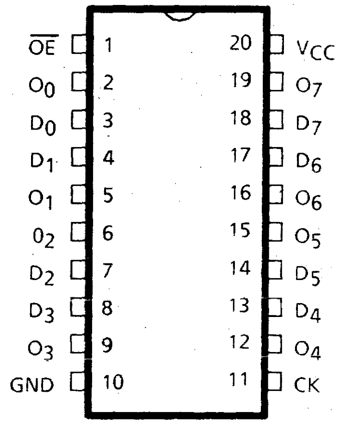
Preliminary Information

October '83

Features

- High latch-up immunity
- High current outputs can drive 30 LSTTL loads
- Low power ISO-CMOS technology
- Bus oriented 3-state outputs
- Meets or exceeds all proposed JEDEC 40.2 specifications
- Fully TTL compatible inputs and outputs
- Pin compatible with 54/74LS374 types

CONNECTION DIAGRAM
DIP (TOP VIEW)



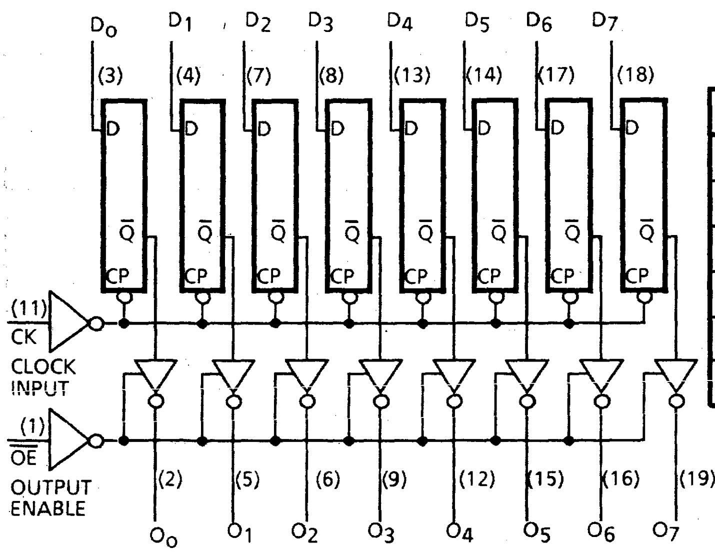
Description

This 8-bit latch features 3-state operation and is designed for use in high speed, bus oriented, systems. The latches hold their indivual data when meeting set up times with the clock (CK) LOW to HIGH transition. The state of the latches is uneffected by the active low Output Enable ($\overline{OE}$) pin, but when $\overline{OE}$ is HIGH the outputs are put into high impedance. Data may thus be latched even when the device is deselected.

Ordering Information

MD54HCT374RCB, Cerdip
-55°C to 125°C
with MIL 883B option

MD74HCT374RE, Plastic Dip
-40°C to 85°C



PIN FUNCTION

PIN	DESCRIPTION
D_0 to D_7	Data Inputs
O_0 to O_7	Data Outputs
CK	Clock Input
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage
GND	System Ground

MITEL

MD54/74HCT540R

Inverting Octal Line Driver/Buffer

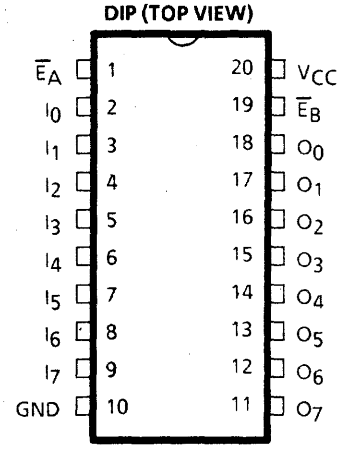
Preliminary Information

October '83

Features

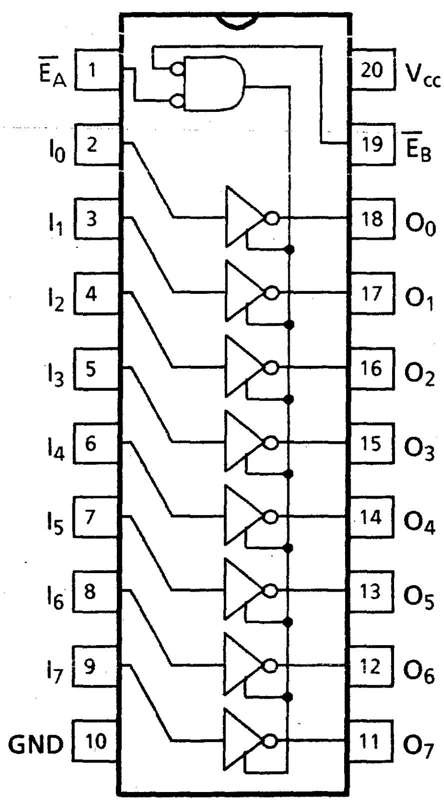
- High latch-up immunity
- High current outputs can drive 30 LSTTL loads
- Low power ISO-CMOS technology
- Bus oriented 3-state outputs
- Meets or exceeds all proposed JEDEC 40.2 specifications
- Fully TTL compatible inputs and outputs
- Pin compatible with 54/74LS540 types

CONNECTION DIAGRAM
DIP (TOP VIEW)



Description

These ISO-CMOS Octal line driver/buffers are designed to improve P.C. board density and performance in three-state memory address drivers, clock drivers, and bus oriented receivers/transmitters. The MD54/74HCT540R offers inverting three-state buffers controlled by two active low enable pins.



Ordering Information

MD54HCT540RCB, Cerdip
-55°C to 125°C
with MIL 883B option

MD74HCT540RE, Plastic Dip
-40°C to 85°C

PIN	DESCRIPTION
$\overline{E}_A$, $\overline{E}_B$	Data Output Enable
I_0 to I_7	Data Inputs
O_0 to O_7	Data Outputs
V_{CC}	Supply Voltage
GND	System Ground

TRUTH TABLE

INPUTS			OUTPUTS
$\overline{E}_A$	$\overline{E}_B$	I_0 to I_7	O_0 to O_7
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

H = logic "1", L = logic "0", X = don't care,
Z = high impedance

MITEL

MD54/74HCT541R

Octal Line Driver/Buffer

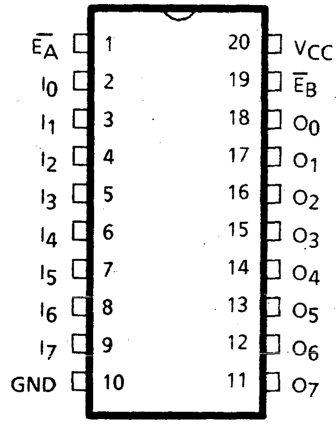
Preliminary Information

October '83

Features

- High latch-up immunity
- High current outputs can drive 30 LSTTL loads
- Low power ISO-CMOS technology
- Bus oriented 3-state outputs
- Meets or exceeds all proposed JEDEC 40.2 specifications
- Fully TTL compatible inputs and outputs
- Pin compatible with 54/74LS541 types

CONNECTION DIAGRAM
DIP (TOP VIEW)



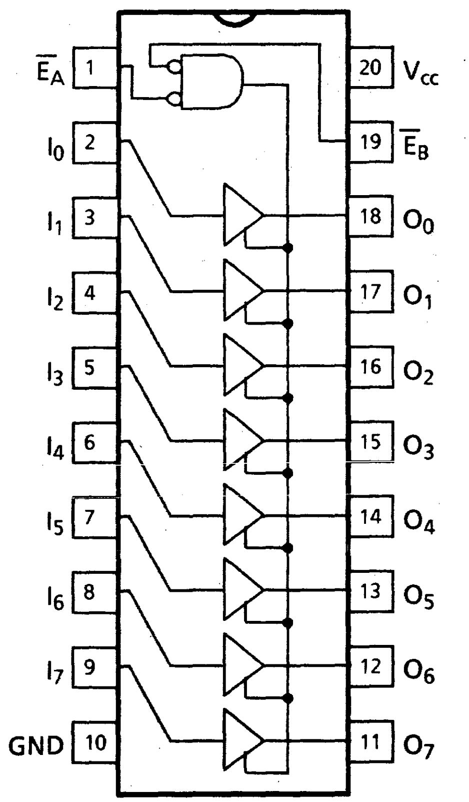
Description

These ISO-CMOS Octal line driver/buffers are designed to improve P.C. board density and performance in three-state memory address drivers, clock drivers, and bus oriented receivers/transmitters. The MD54/74HCT541R offers non-inverting three-state buffers controlled by two active low enable pins.

Ordering Information

MD54HCT541RCB, Cerdip
-55°C to 125°C
with MIL 883B option

MD74HCT541RE, Plastic Dip
-40°C to 85°C



PIN	DESCRIPTION
$\overline{E}_A, \overline{E}_B$	Data Output Enable
I_0 to I_7	Data Inputs
O_0 to O_7	Data Outputs
V_{CC}	Supply Voltage
GND	System Ground

TRUTH TABLE

INPUTS			OUTPUTS
$\overline{E}_A$	$\overline{E}_B$	I_0 to I_7	O_0 to O_7
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

H = logic "1", L = logic "0", X = don't care,
Z = high impedance

MITEL

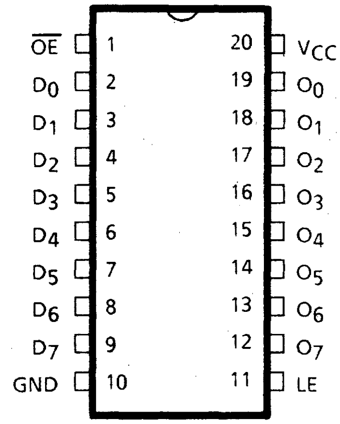
MD54/74HCT573R
Octal D-Type Transparent Latch
Preliminary Information

October '83

Features

- High latch-up immunity
- High current outputs can drive 30 LSTTL loads
- Low power ISO-CMOS technology
- Bus oriented 3-state outputs
- Meets or exceeds all proposed JEDEC 40.2 specifications
- Fully TTL compatible inputs and outputs
- Pin compatible with 54/74LS573 types

CONNECTION DIAGRAM
DIP (TOP VIEW)



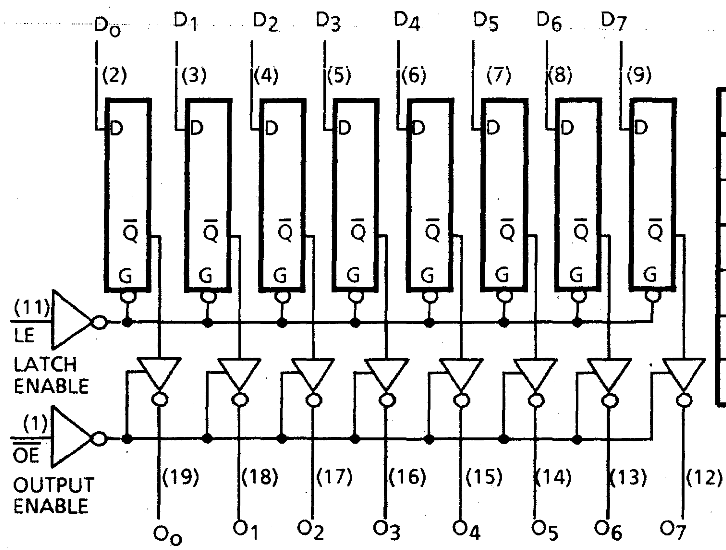
Description

This 8-bit latch features 3-state operation and is designed for use in high speed, bus oriented, systems. The MD54/74HCT573R appears transparent to data (outputs change asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, data meeting the set up times becomes latched. The state of the latches is unaffected by the active low Output Enable ($\overline{OE}$) pin, but when $\overline{OE}$ is HIGH the outputs are put into high impedance. Data may thus be latched even when the device is deselected.

Ordering Information

MD54HCT573RCB, Cerdip
-55°C to 125°C
with MIL 883B option

MD74HCT573RE, Plastic Dip
-40°C to 85°C



PIN FUNCTION

PIN	DESCRIPTION
D_0 to D_7	Data Inputs
O_0 to O_7	Data Outputs
LE	Latch Enable
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage
GND	System Ground

MITEL

MD54/74HCT574R
Octal D-Type Flip Flop
Preliminary Information

October '83

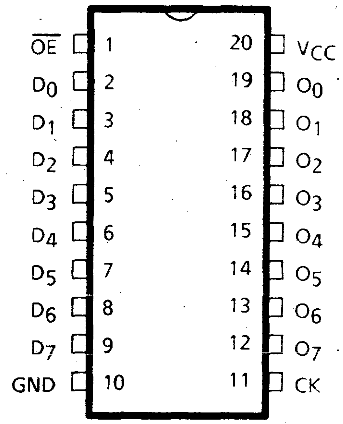
Features

- High latch-up immunity
- High current outputs can drive 30 LSTTL loads
- Low power ISO-CMOS technology
- Bus oriented 3-state outputs
- Meets or exceeds all proposed JEDEC 40.2 specifications
- Fully TTL compatible inputs and outputs
- Pin compatible with 54/74LS574 types

Description

This 8-bit latch features 3-state operation and is designed for use in high speed, bus oriented, systems. The latches hold their indivual data when meeting set up times with the clock (CK) LOW to HIGH transition. The state of the latches is uneffected by the active low Output Enable ($\overline{OE}$) pin, but when $\overline{OE}$ is HIGH the outputs are put into high impedance.Data may thus be latched even when the device is deselected.

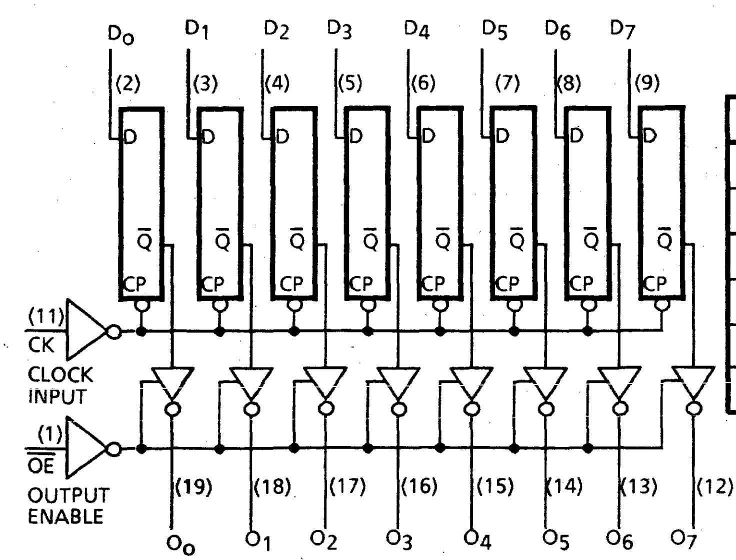
CONNECTION DIAGRAM
DIP (TOP VIEW)



Ordering Information

MD54HCT574RCB, Cerdip
-55°C to 125°C
with MIL 883B option

MD74HCT574RE, Plastic Dip
-40°C to 85°C



PIN FUNCTION

PIN	DESCRIPTION
D_0 to D_7	Data Inputs
O_0 to O_7	Data Outputs
CK	Clock Input
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage
GND	System Ground

MOTOROLA

SEMICONDUCTORS

P.O. BOX 20912 • PHOENIX, ARIZONA 85036

MC34010P
MC34011P

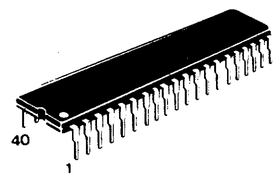
Advance Information

ELECTRONIC TELEPHONE CIRCUIT

- Provides All Basic Telephone Station Apparatus Functions in a Single IC, Including DTMF Dialer, Tone Ringer, Speech Network and Line Voltage Regulator
- DTMF Generator Uses Low-Cost Ceramic Resonator with Accurate Frequency Synthesis Technique
- Tone Ringer Drives Piezoelectric Transducer and Satisfies EIA RS-470 Impedance Signature Requirements
- Speech Network Provides Two-Four Wire Conversion with Adjustable Sidetone Utilizing an Electret Transmitter
- On-Chip Regulator Insures Stable Operation Over Wide Range of Loop Lengths
- I^2L Technology Provides Low 1.4 Volt Operation and High Static Discharge Immunity
- MC34010P Provides Microprocessor Interface Port for Automatic Dialing Features

ELECTRONIC TELEPHONE CIRCUIT

BIPOLAR LINEAR/I^2L



PLASTIC PACKAGE
CASE 711-03

TELECOM SELECTOR GUIDE

Station Set Products	
MC34011	Electronic Telephone Circuit
MC34010	Electronic Telephone Circuit with MPU Interface
MC34012	Tone Ringer
MC34017	Tone Ringer with Push-Pull Output
MC34013	DTMF Generator with Speech Network
Switching Products	
MC3419 Series	Subscriber Loop Interface Circuit
MC3416	4 x 4 x 2 Crosspoint Switch

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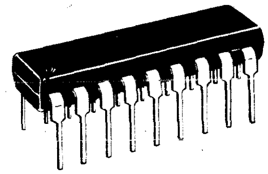
Specifications and Applications Information

FLOPPY DISK SUPPORT
MC3470P
MC3470AP

FLOPPY DISK READ AMPLIFIER SYSTEM

SILICON MONOLITHIC INTEGRATED CIRCUIT



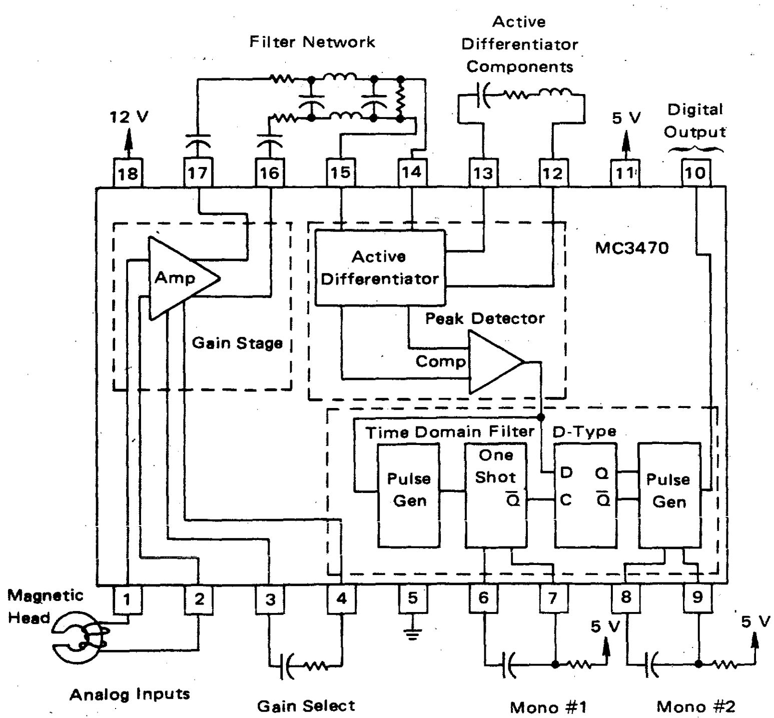
P SUFFIX
PLASTIC PACKAGE
CASE 701-01

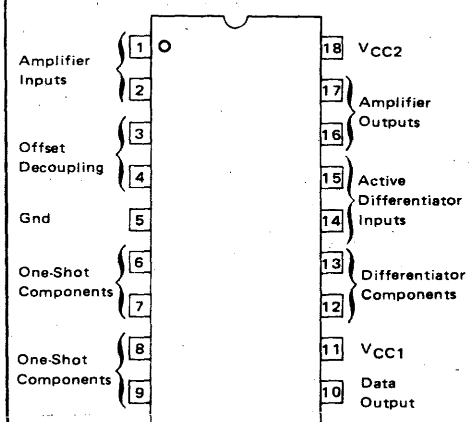
FLOPPY DISK READ AMPLIFIER

The MC3470 is a monolithic READ Amplifier System for obtaining digital information from floppy disk storage. It is designed to accept the differential ac signal produced by the magnetic head and produce a digital output pulse that corresponds to each peak of the input signal. The gain stage amplifies the input waveform and applies it to an external filter network, enabling the active differentiator and time domain filter to produce the desired output.

- Combines All the Active Circuitry To Perform the Floppy Disk Read Amplifier Function in One Circuit
- Guaranteed Maximum Peak Shift of 2.0% — MC3470A
- Improved (Positive) Gain T_C and Tolerance
- Improved Input Common Mode

TYPICAL APPLICATION





DS9588
(Replaces ADI-512)

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SEMICONDUCTORS
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FLOPPY DISK SUPPORT
MC3469P
MC3471P

Specifications and Applications Information

FLOPPY DISK
WRITE CONTROLLERS

SILICON MONOLITHIC
INTEGRATED CIRCUIT

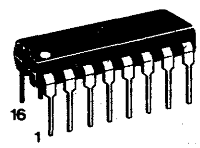
FLOPPY DISK WRITE CONTROLLER

The MC3469 and MC3471 are monolithic WRITE Current Controllers designed to provide the entire interface between floppy disk heads and the head control and write data signals for straddle-erase or tunnel-erase heads.

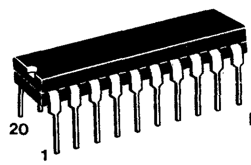
Provisions are made for selecting a range of accurately controlled write currents and for head selection during both read and write operation. Additionally, provisions are included for externally adjusting degauss period and inner/outer trace compensation.

The MC3471 provides the erase delay and inhibit functions required to interface with tunnel-erase heads.

- Head Selection — Current Steering Through Write Head and Erase Coil in Write Mode
- Provides High Impedance (Read Data Enable) during Read Mode
- Head Current (Write) Guaranteed Using Laser Trimmed Internal Resistor (3.0 mA using R_{ext} = 10 kΩ)
- IRW Select Input Provides for Inner/Outer Track Compensation
- Degauss Period Externally Adjustable
- Minimizes External Components
- MC3471 Provides On-Chip Adjustable Erase Delays

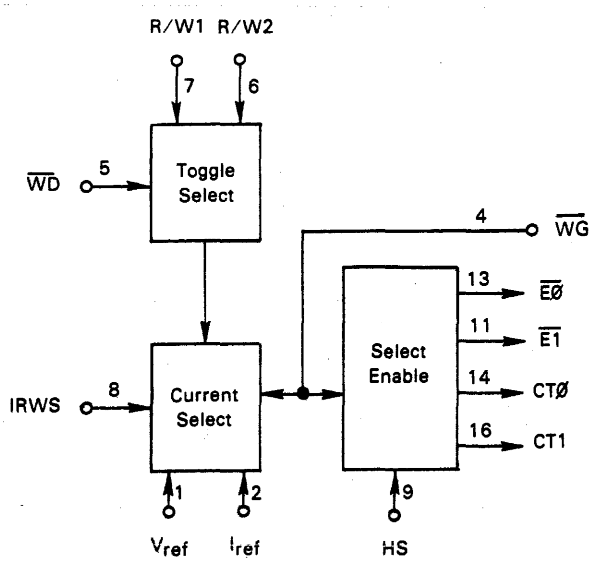


MC3469 only
P SUFFIX
PLASTIC PACKAGE
CASE 648

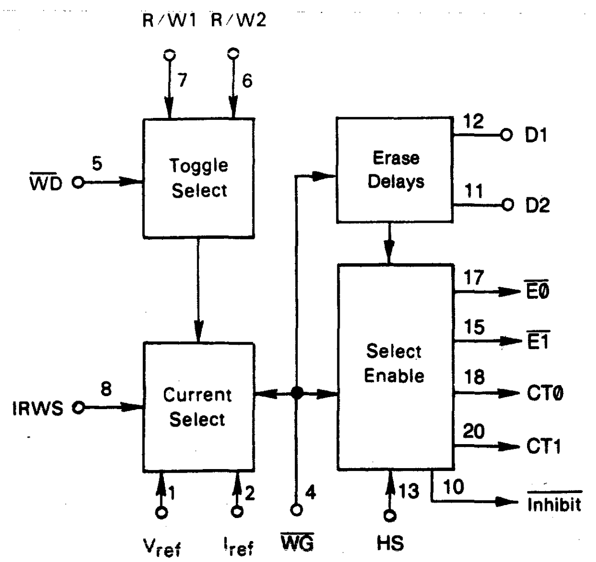


MC3471 only
P SUFFIX
PLASTIC PACKAGE
CASE 738

MC3469
BLOCK DIAGRAM



MC3471
BLOCK DIAGRAM



 DS9577

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MC3482A/MC6882A
MC3482B/MC6882B

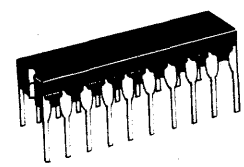
This device may be ordered under either of the above type numbers.

OCTAL THREE-STATE BUFFER/LATCH

This series of devices combines four features usually found desirable in bus-oriented systems: 1) High impedance logic inputs insure that these devices do not seriously load the bus; 2) Three-state logic configuration allows buffers not being utilized to be effectively removed from the bus; 3) Schottky technology allows for high-speed operation; 4) 48 mA drive capability.

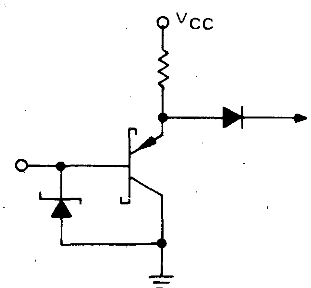
- Inverting and Non-Inverting Options of Data
- SN74S373 Function Pinouts
- Eight Transparent Latches/Buffers in a Single Package
- Full Parallel-Access for Loading and Reloading
- Buffered Control Inputs
- All Inputs Have Hysteresis to Improve Noise Rejection
- High Speed — 8.0 ns (Typ)
- Three-State Logic Configuration
- Single +5 V Power Supply Requirement
- Compatible with 74S Logic or M6800 Microprocessor Systems
- High Impedance PNP Inputs Assure Minimal Loading of the Bus

OCTAL THREE-STATE BUFFER/LATCH

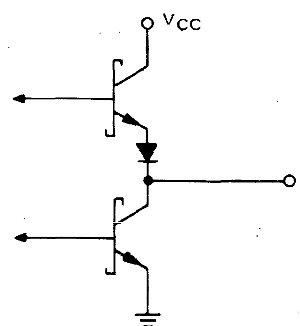


L SUFFIX
CASE 732

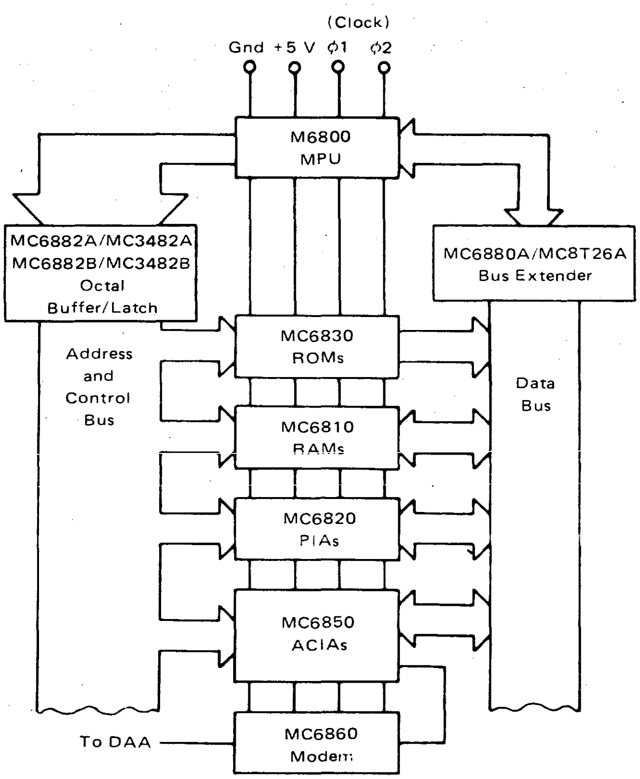
INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT



MICROPROCESSOR BUS EXTENDER APPLICATION



ORDERING INFORMATION

(Temperature Range for the following devices = 0 to +75°C.)

Device	Alternate	Package
MC6882AL	MC3482AL	Ceramic DIP
MC6882BL	MC3482BL	Ceramic DIP

MOTOROLA

MOTOROLA BROADLINE

BUS STANDARD LINE DRIVERS & RECEIVERS

STANDARD	INTRODUCED	1983 INTRODUCTION
RS232C	MC1488 DR MC1489 REC	
RS422	MC3486 REC MC3487 DR AM26LS31 DR	AM26LS32REC
RS423	MC3487 DR	μA9636A (MC3488A)
RS-485 (PARTY LINE)	SN75172 REC SN75174 REC SN75173 DR SN75175 DR	SN75176-8
IEEE 488-1978	MC3440-43A MC3446A IMC3448A MC3447	
IBM GA-22-6974-3	MC3481 MC3485 MC75125-9	

PERIPHERAL DRIVERS

PART NUMBER	DESCRIPTION	INPUT COMPATIBILITY
MC1411P (ULN2001A)	Seven Element Darlington Array (0.5 A Max)	General
MC1412P (ULN2002A)		PMOS
MC1413P (ULN2003A)		TTL/CMOS
MC1416P (ULN2004A)		NMOS
MC1472U/P1	Dual Positive NAND	H1 Z(1)
ULN2801A	Octal Darlington Array (0.5 A Max)	General
ULN2802A		PMOS
ULN2803A		TTL/CMOS
ULN2804A		CMOS/PMOS
ULN2068B	Quad 1.5 A Darlington(2)	TTL/CMOS/DTL
ULN2074B	Quad 1.5 A Darlington(3)	General

(1) PNP Bufferer for TTL/MOS Compatibility
(2) Open collector — Diode Clamped
(3) Open Collector — Open Emitter

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MICROPROCESSOR/COMPUTER INTERFACE
MC3481
MC3485

QUAD SINGLE-ENDED LINE DRIVER

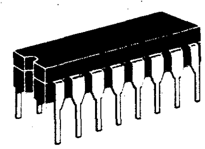
The MC3481 and MC3485 are quad single-ended line drivers specifically designed to meet the IBM 360/370 I/O specification (GA22-6974-3).

Output levels are guaranteed over the full range of output load and fault conditions. Compliance with the IBM requirements for fault protection, flagging, and power up/power down protection for the bus make this an ideal line driver for party line operations.

- Separate Enable and Fault Flags — MC3481
- Common Enable and Fault Flag — MC3485
- Power Up/Down Does Not Disturb Bus
- Schottky Circuitry for High-Speed — PNP Inputs
- Internal Bootstraps for Faster Rise Times
- Driver Output Current Foldback Protection
- MC3485 has LS Totem Pole Driver Output

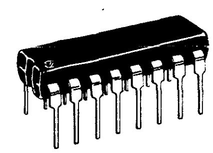
IBM 360/370 QUAD LINE DRIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

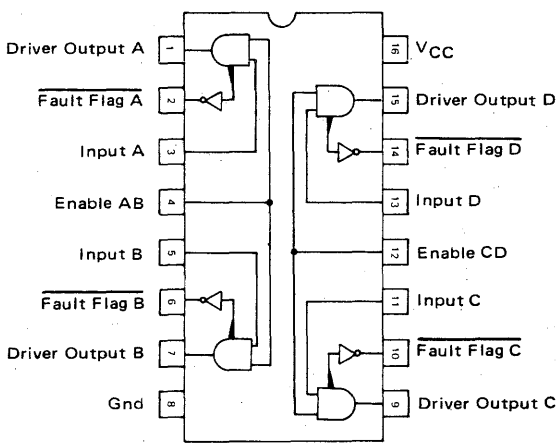


L SUFFIX
CERAMIC PACKAGE
CASE 620

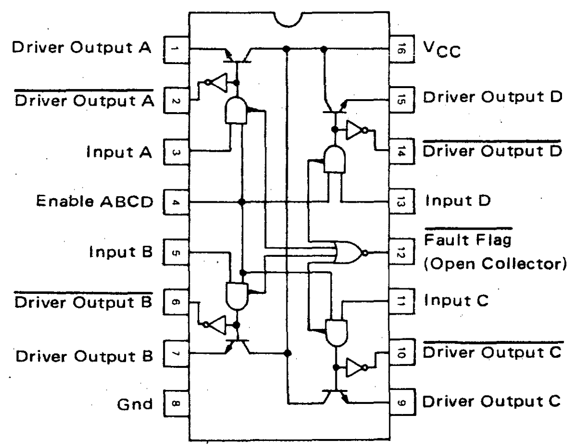
P SUFFIX
PLASTIC PACKAGE
CASE 648



MC3481
DUAL ENABLE
INDIVIDUAL FAULT FLAG



MC3485
COMMON ENABLE
COMMON FAULT FLAG



SUPPORTING IBM 360/370 LINE RECEIVERS

Device Number	No. of Channels	Input Resistance kΩ Min/Max	$I_{IH(R)}$ @V_{IH}=3.11 V mA Max	t_{PLH} @C_L=50 pF ns Max
MC75125/75127	Seven	7.4/20	0.42	25
MC75128/75129	Eight	7.4/20	0.42	25

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GPIB INSTRUMENTATION BUS INTERFACE
MC3447

BIDIRECTIONAL INSTRUMENTATION BUS (GPIB) TRANSCEIVER

This bidirectional bus transceiver is intended as the interface between TTL or MOS logic and the IEEE Standard Instrumentation Bus (488-1978, often referred to as GPIB). The required bus termination is internally provided.

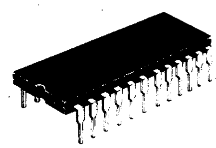
Low power consumption has been achieved by trading a minimum of speed for low current drain on non-critical channels. A fast channel is provided for critical ATN and EOI paths.

Each driver/receiver pair forms the complete interface between the bus and an instrument. Either the driver or the receiver of each channel is enabled by a Send/Receive input with the disabled output of the pair forced to a high impedance state. The receivers have input hysteresis to improve noise margin, and their input loading follows the bus standard specifications.

- Low Power – Average Power Supply Current = 30 mA Listening, 75 mA Talking
- Eight Driver/Receiver Pairs
- Three-State Outputs
- High Impedance Inputs
- Receiver Hysteresis – 600 mV (Typ)
- Fast Propagation Times – 15–20 ns (Typ)
- TTL Compatible Receiver Outputs
- Single +5 Volt Supply
- Open Collector Driver Output with Terminations
- Power Up/Power Down Protection (No Invalid Information Transmitted to Bus)
- No Bus Loading When Power is Removed From Device
- Required Termination Characteristics Provided

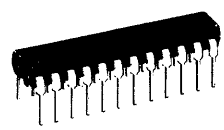
OCTAL BIDIRECTIONAL BUS TRANSCEIVER WITH TERMINATION NETWORKS

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 623

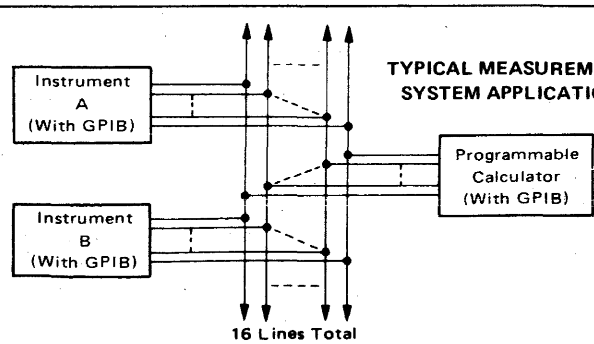
P3 SUFFIX
PLASTIC PACKAGE
CASE 724



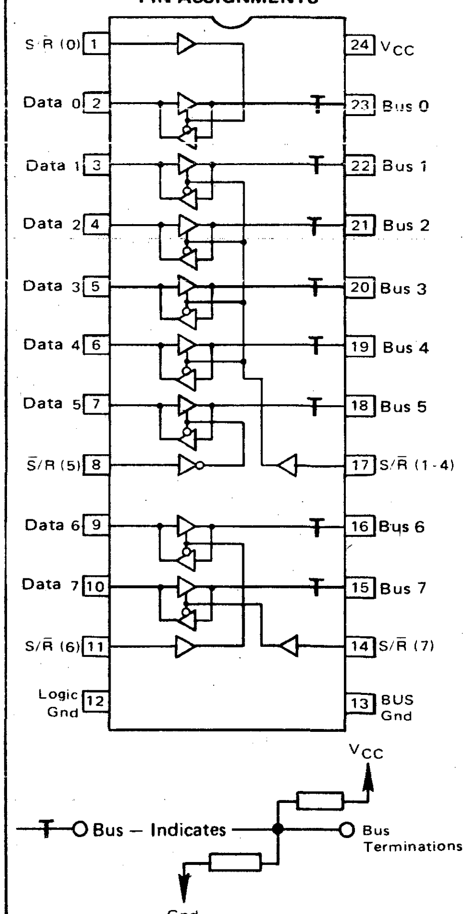
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Driver Output Current	$I_{O(D)}$	150	mA
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TYPICAL MEASUREMENT SYSTEM APPLICATION



PIN ASSIGNMENTS



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DATA CONVERSION MC3412 MC3512

Advance Information

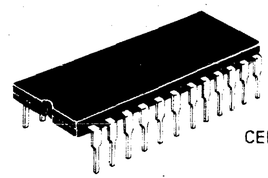
LASER TRIMMED HIGH-SPEED 12-BIT D/A CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT

COMPLETE 12-BIT HIGH-SPEED MONOLITHIC D/A CONVERTER

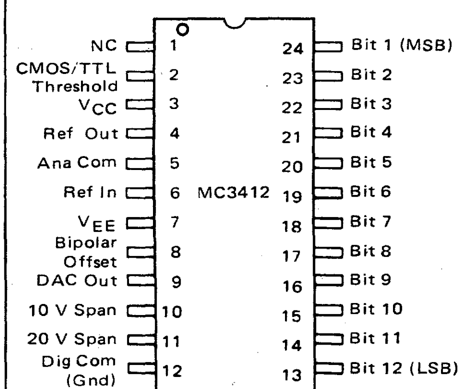
The MC3412/3512 is a monolithic 12-bit resolution D/A converter. It contains a high stability bandgap reference capable of supplying 1.5 mA externally, trimmed to ±0.25% maximum error. Active laser trimming of thin film ladder network, reference, span, bipolar offset, and bandgap resistors at wafer level provide accuracy and linearity of better than ±½ LSB. An innovative bit switching scheme provide fast settling time yet enables selection of CMOS or TTL thresholds. TTL threshold levels are retained over a wide V_{CC} range from 13.5 to 16.5 volts. Precision internal span resistors allow output voltage options of 0 to 5.0 V, 0 to 10 V, ±2.5 V, ±5.0 V, and ±10 V. 12-bit accuracy and a fast settling time of typically 200 ns (to ±½ LSB) make this converter ideal for applications such as a fast A/D building block or display driver.

- True 12-Bit Linearity: ±½ LSB Max
- Fast Settling Time: ±½ LSB in 200 ns Typ
- Fully Monotonic Over Temperature Range
- High-Stability Bandgap Voltage Reference On Chip
- Linearity Guaranteed Over Temperature
- Low Power Consumption: 210 mW
- Pinout Compatible with AD563 and AD565
- Selectable Digital Thresholds
- Internal Span Resistors for Generating Output Voltage

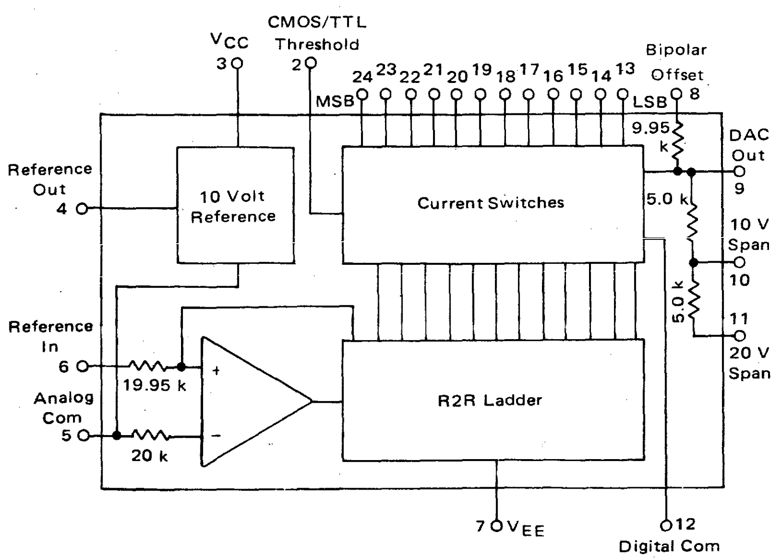


L SUFFIX
CERAMIC PACKAGE
CASE 623

PIN CONNECTIONS



BLOCK DIAGRAM



ORDERING INFORMATION

Device	Temperature Range	Package
MC3412L	0°C to +70°C	Ceramic DIP
MC3512L	−55°C to +125°C	Ceramic DIP

This is advance information and specifications are subject to change without notice.

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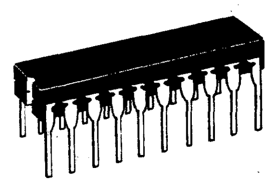
DATA CONVERSION
MC6890

Advance Information

8-BIT
MPU-BUS-COMPATIBLE
DAC

SILICON MONOLITHIC
INTEGRATED CIRCUIT



L SUFFIX
CASE 732

MPU-BUS-COMPATIBLE 8-BIT D-TO-A CONVERTER

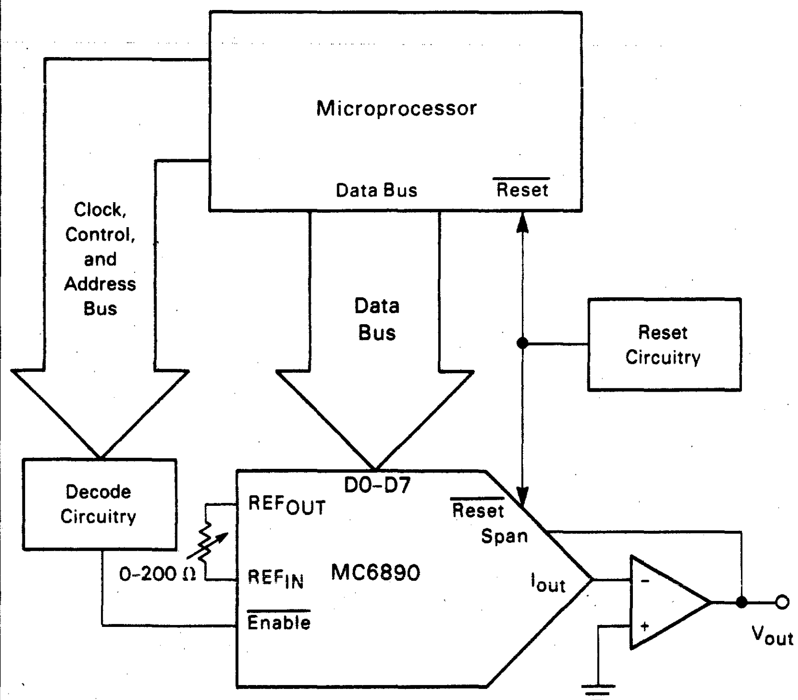
The MC6890 is a self-contained, bus-compatible, 8 bit (±0.19% accuracy) D-to-A converter system capable of interfacing directly with 8-bit microprocessors.

Available in both commercial and military temperature ranges, this monolithic converter contains master/slave registers to prevent transparency to data transitions during active enable; a laser-trimmed, low-TC, 2.5 V precision bandgap reference; and high stability, laser-trimmed, thin-film resistors for both reference input and output span and bipolar offset control.

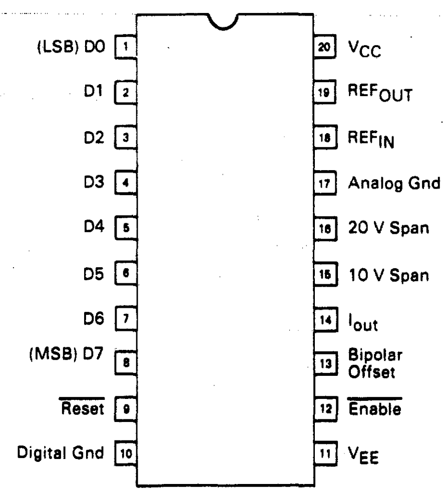
A reset pin provides for overriding stored data and forcing I_{out} to zero.

- Direct Data Bus Link with All Popular TTL Level MPU's
- ±1/2 LSB Nonlinearity Over Temperature
- Fast Settling Time: 200 ns Typ
- Internal 2.5-V Precision Laser-Trimmed Voltage Reference (May Also Be Used Externally)
- Minimum $\overline{\text{Enable}}$ Pulse Width: 70 ns
- Fast $\overline{\text{Enable}}$: 10 ns Maximum Data Hold Time
- $\overline{\text{Reset}}$ Pin to Override Data
- Output Voltage Ranges: +5, +10, +20, or ±2.5, ±5, ±10 Volts
- Low Power: 90 mW Typ
- +5 V and −5 V to −15 V Supplies

OPERATION WITH AN MPU



PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC6890L	0° to +70°C	Ceramic DIP
MC6890AL	−55° to +125°C	Ceramic DIP

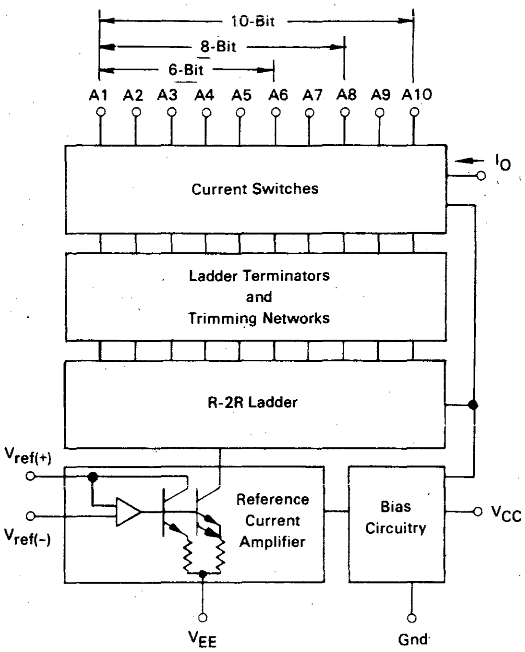
This document contains information on a new product. Specifications and information herein are subject to change without notice.

ADI-592R2

MOTOROLA

ADDITIONAL D-A CONVERTERS

General Purpose



Device Number	Error (%Max)	P_D @ V_{EE} = -5 V (mW Max)	$t_{Settling}$ (ns Typ)	I_O (mA)	Suffix	Case
6-Bit						
MC1506* MC1406	±0.78	120	150	1.9 to 2.1	L	632
8-Bit						
DAC-08A DAC-08*	±0.1 ±0.19	48	85	2.984 to 2.880	Q	620
DAC-08H DAC-08E DAC-08C	±0.1 ±0.19 ±0.39	48	85	1.940 to 2.040	P, Q	648,620
MC1508L8* MC1408L8	±0.19	170	300	1.9 to 2.1	L	620
MC1408L7 MC1408L6	±0.39 ±0.78	170	300	1.9 to 2.1	L, P	620, 648
MC3408	±0.5	170	300	1.9 to 2.1	L	620
10-Bit						
MC3510*	±0.05	220	250	3.8 to 4.2	L	690
MC3410	±0.05	220	250	3.8 to 4.2	L, P	690, 648
MC3410C	±0.1	220	250	3.8 to 4.2	L, P	690, 648
12-Bit						
AD562SD*	±0.006	210	200	1.6 to 2.4	D	716
AD562AD # **AD562KD**	±0.01	210	200	1.6 to 2.4	D	716
AD563TD* **AD563SD*** **AD563KD**	±0.006	210	200	1.6 to 2.4	D	716
AD563JD	±0.01	210	200	1.6 to 2.4	D	716

*T_A = -55 to +125°C #T_A = -25 to +85°C Devices without symbol: T_A = 0 to +70°C

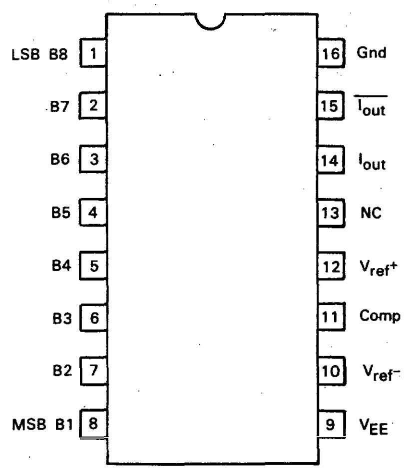
Bold Part Numbers Indicate New Products.

D-A CONVERTERS — HIGH SPEED

MC10318 series — A high speed 8-bit D/A converter capable of data conversion rates in excess of 25 MHz. It is intended for applications in high speed instrumentation and communication equipment, graphics displays, storage oscilloscopes, radar processing, and TV broadcast systems. The inputs are compatible with MECL 10,000 series logic, while the complementary current outputs have 51 mA full scale capability. Monotonic over the full temperature range, the outputs typically settle in 10 ns.

T_A = 0 to 70°C

Packages:
L Suffix — Case 620/690



Device Number	Error % Max	P_D @ V_{EE} = −5.2 V mW Max	$t_{Settling}$ ns Typ (to ½ LSB)	I_O & $\overline{I_O}$ @V_{Ref} = 10.56 V mA Typ
MC10318CL6	±0.78	675	10	51
MC10318CL7	±0.39	675	10	51
MC10318L	±0.19	675	10	51
MC10318L9	±0.10	675	10	51

Bold Part Numbers Indicate New Products.

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DATA CONVERSION

MC10315L MC10317L

Advance Information

HIGH SPEED 7-BIT ANALOG-TO-DIGITAL FLASH CONVERTER

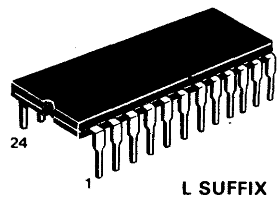
SILICON MONOLITHIC INTEGRATED CIRCUIT

SEVEN-BIT PARALLEL HIGH SPEED A/D CONVERTER (WITH OVERRANGE)

The MC10315L/MC10317L is a 7-bit high speed parallel A/D converter which employs ECL processing. The device consists of 128 parallel latched comparators across a high quality input reference network. The 128 comparator outputs are then fed to a 128-to-7 encoder and latched to the outputs which are ECL compatible. An overrange bit is provided to allow overrange sensing, or to facilitate the connection of an MC10315L and MC10317L in parallel to produce an 8-bit A/D converter. The MC10315L and MC10317L are identical devices except for the method of overranging used, which simplifies the utilization of two 7-bit converters to produce an 8-bit conversion. (See ordering information and technical description.)

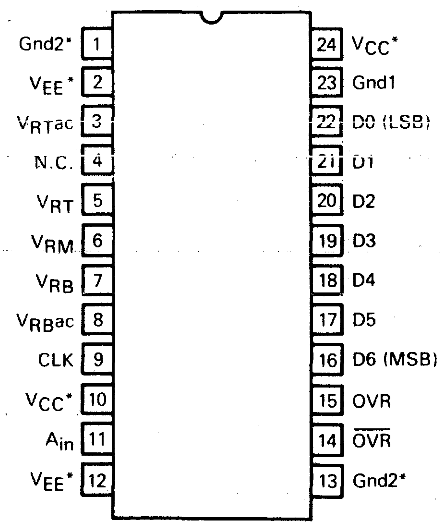
Applications include video display and radar signal processing, high speed instrumentation, and TV broadcast video encoding.

- 7-Bit Resolution/8-Bit Accuracy Plus Overrange
- Direct Interconnection for 8-Bit Conversion
- 15 MHz Sampling Rate
- Wide Range of Input Voltage: ±2.0 Volts
- Low Input Capacitance: ≤70 pF
- 1.2 Watt Power Dissipation
- No Sample and Hold Required for Video Bandwidth Signals
- Standard 24-Pin Package



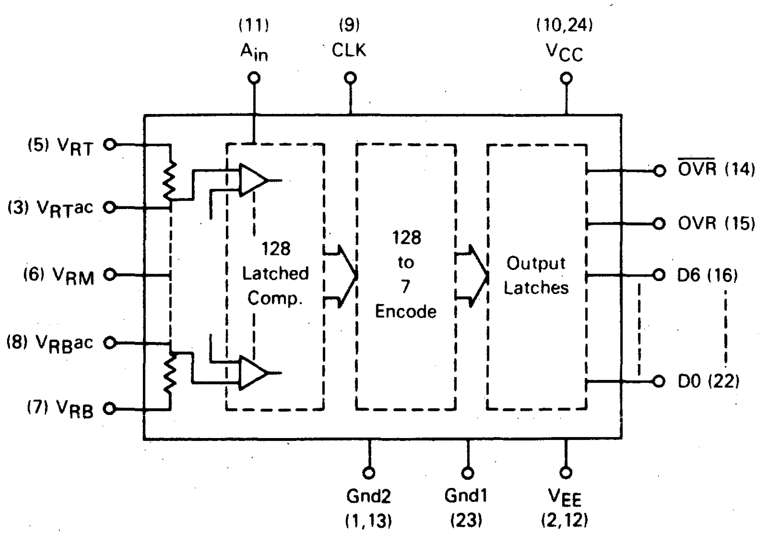
L SUFFIX
CERAMIC PACKAGE
CASE 623

PIN DIAGRAM



*V_{CC}, V_{EE} and Gnd2 are each available on two pins. Interconnections for the respective function are made on chip. To minimize I•R drops on chip and in the bonding wires, utilization of both pins for each function is recommended.

MC10315L/MC10317L DEVICE/APPLICATION CONFIGURATION



ORDERING INFORMATION**

Device	Overrange Function		
	Analog Input Condition	Logic Levels	
		OVR Bit	D0-D6 Bits
MC10315L	Overranged	High	High
MC10317L	Overranged	High	Low

**For information regarding an evaluation board, contact Linear Marketing.

ADI-654R1

This document contains information on a new product. Specifications and information herein are subject to change without notice.

SP9770

TEN BIT HIGH SPEED D TO A CONVERTER

The Plessey SP9770 10-bit D/A converter is capable of converting a digital signal into a analog voltage at a rate of over 75 mega-bits per second (MBPS). An inherently low glitch desing is used and the complementary current outputs are suitable for direct transmission line drive. Included on the chip is a high performance voltage reference and reference amplifier.

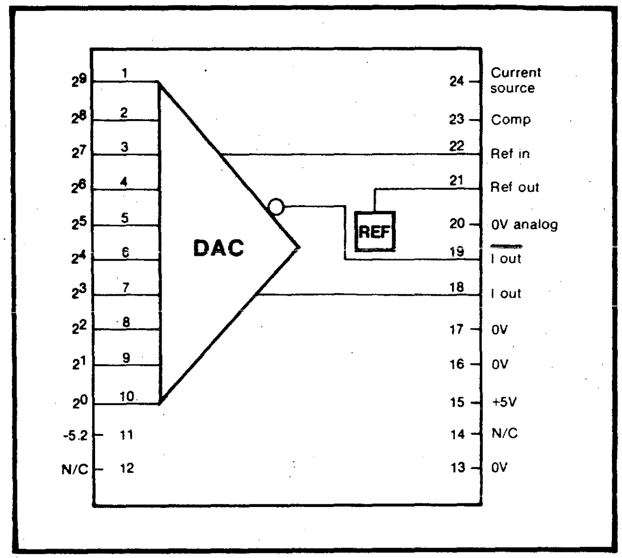


Fig. 1 SP9770 pin connections

FEATURES

- 12ns Settling time
- 10 bits to ±1/2 LSB absolute and differential non linearity
- 75 MBPS Update rate
- Current output
- ECL standard inputs
- Complementary outputs, 20 mA full scale
- Reference tempco. typically 40 ppm/°C
- DAC usable in multiplying mode to 25MHz
- 24 lead, 0.6 pitch package

ABSOLUTE MAXIMUM RATINGS

Postitive supply voltage	+ 5.5V
Negative supply voltage	—5.7V
Operating temperature range	—30°C to 85°C
Storage temperature	—55°C to 125°C
Lead temperature (soldering 60 sec)	300°C
Digital input voltage	0 to VEE
Min current set resistance	R SET 150Ω
Output reference supply	0 to +1V

OPERATING NOTES

The pinout of the device is shown in Fig. 1. External components are limited to the current setting resistor and decoupling capacitors.
The DAC has current outputs, with a nominal full scale of 20mA, corresponding with a 1 volt drop across a 50 ohm load.
The actual output current is determined by the on-chip reference voltage and an off-chip current setting resistor. Output current, I out, is given by

$$I_{OUT} = 4 \times \frac{V_{REF}}{R_{SET}}$$

A complementary $\overline{I_{OUT}}$ is also provided. The setting resistor, R_{SET}, is typically 240 ohms, giving a full scale output current of 20.75mA, and should have a temperature coefficient similar to that of the output load resistor.

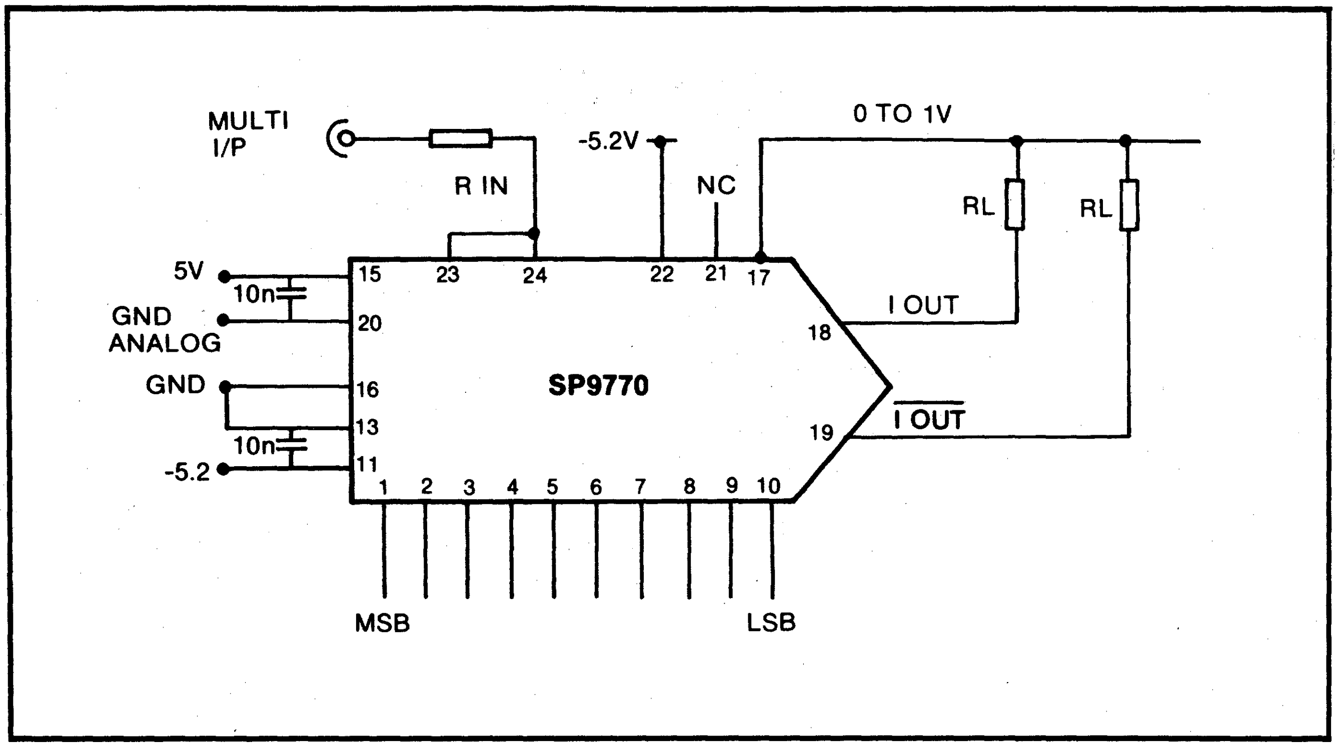


Figure 4. Multiplying Mode operation

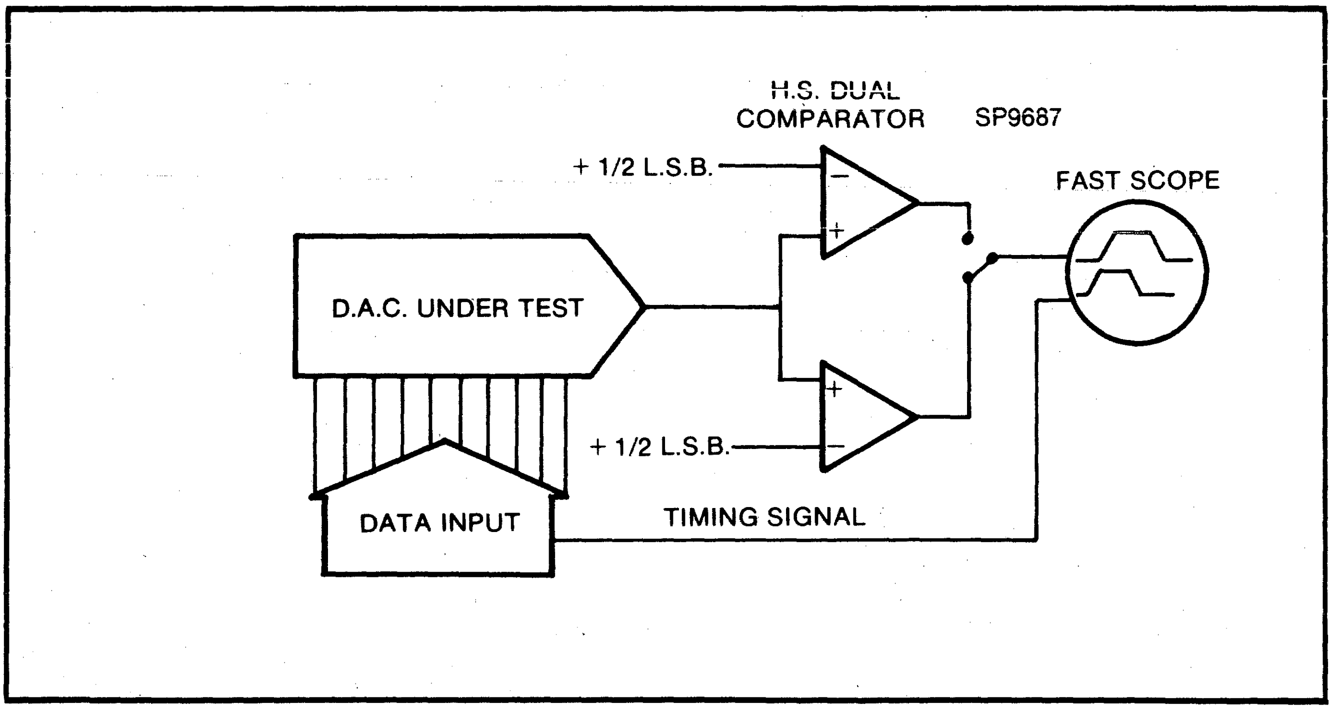


Figure 5. Window detection of D.A.C. output settling

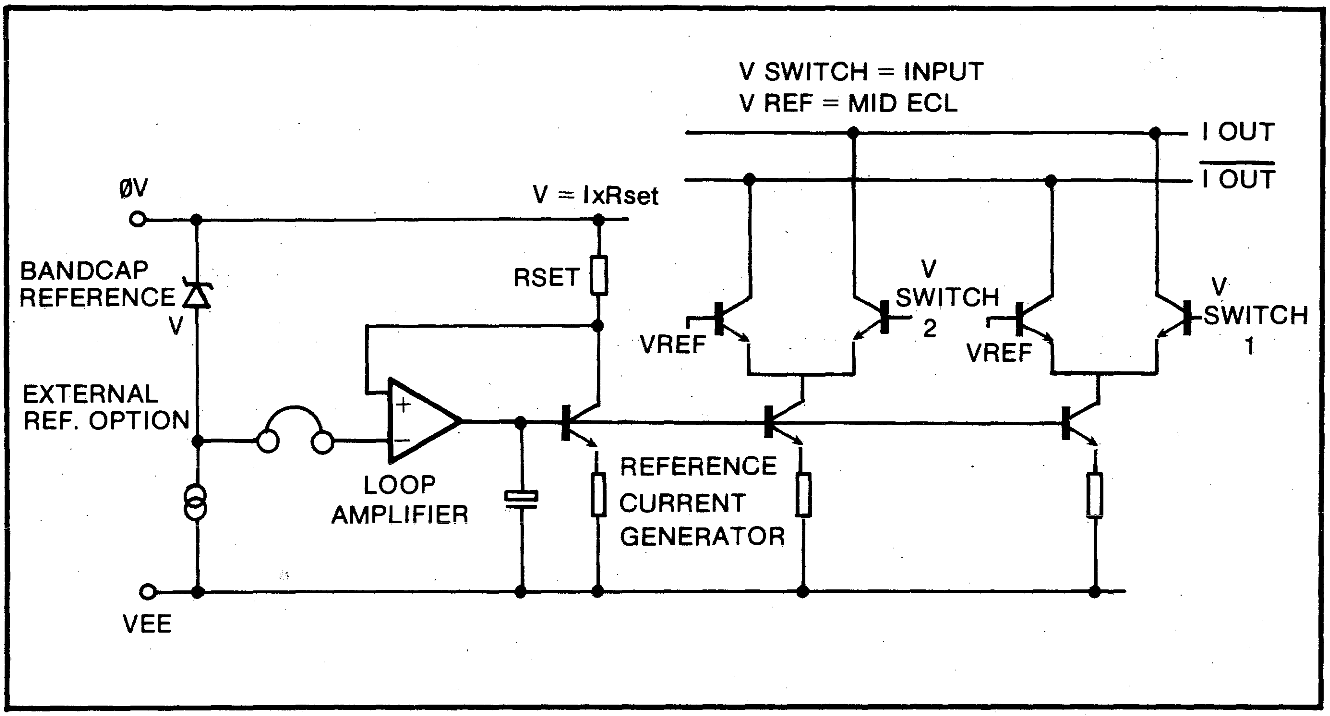


Figure 2. Basic Current Switched DAC

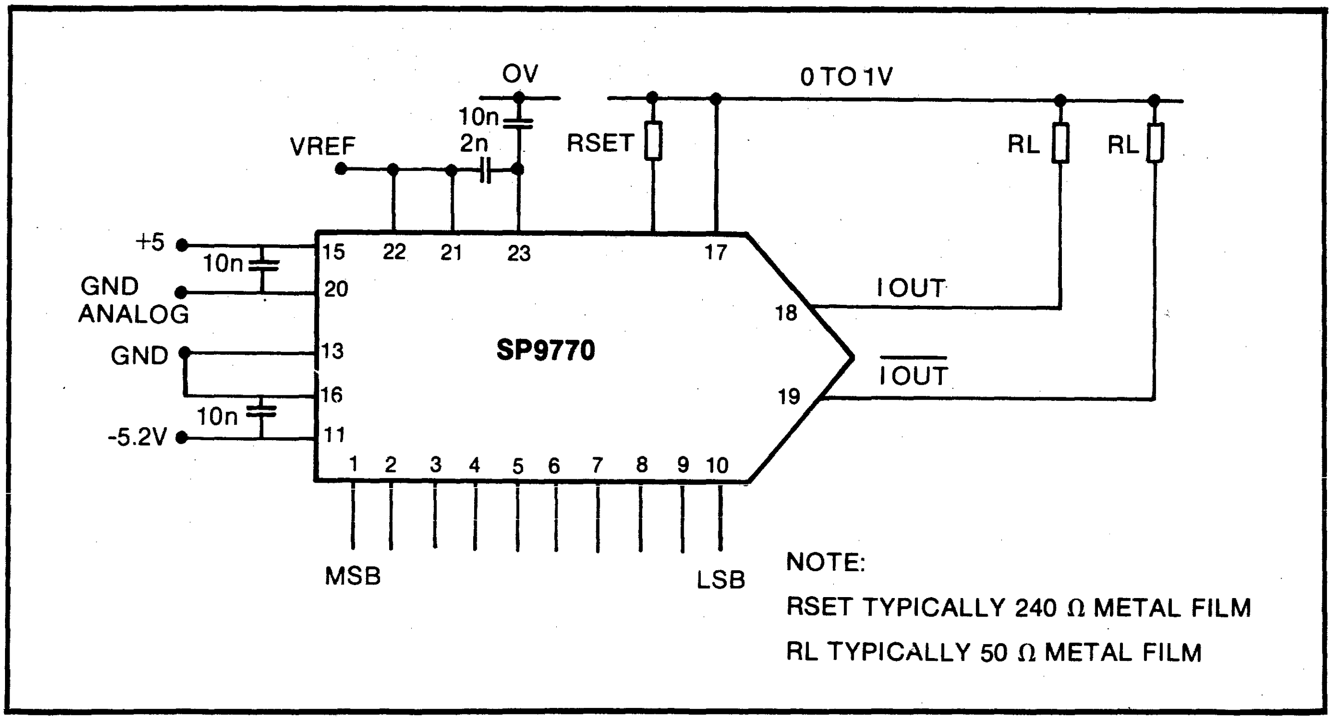


Figure 3. Conventional D/A operation using on-chip reference

PLESSEY
Solid State

The SP9770 has been designed to meet the dc specification shown in the test table below.

Parameter	Symbol	Test Limits			Unit	Comments
		Min.	Typ.	Max.		
Power Supply Current	ICC IEE	7 45	12 56	17 70	mA dc	
Digital Input Currents	IIN H	—	115	200	μAmps	All Inputs High
Reference Voltage	VREF	-1.250	-1.280	-1.300	Volts	
Reference Voltage Temp Coefficient	ΔVREF/ΔT	—	40	80	PPM/°C	
Resolution		—	0.098 10	— —	% Bits	
Non-Linearity	Differential Absolute	— —	— —	±0.05 ±0.05	% %	
Bit Size		19 0.9	21 1	23 1.1	μAmps mVolt	RL = 50Ω
Fullscale Settling Time	ts	—	12	20	nSec	To 1 LSB
Multiplying Bandwidth (3dB)	BM	—	25	—	MHz	Current Mode

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Test Limits			Unit	Comment
		Min.	Typ.	Max.		
Power Supply Voltage	VEE VCC	-4.85 +4.75	-5.3 +5.0	-5.45 +5.25	VOLTS dc	
Input Logic Levels	VIH VIL	-0.960 -1.850	-- --	-0.810 -1.650	VOLTS VOLTS	ECL. 10k Compatible
Fullscale o/p Current	Iout	2	20	30	mAmps	$Iout = \frac{4\ REF}{RSet}$
Output Compliance Voltage (at Pin Under Test) (See Note 1.)	Vc -1	-0.7 --	-- +1	+1	VOLTS VOLTS	at 85°C at 25°C
Ambient Operating Temperature	T	-30	--	+85	°C	

Note 1

Pin 17 should be connected to a reference supply at the most positive voltages required, with the load and Rset pin 24 returned similarly to this reference. Conveniently the reference is ground, but this limits the output to negative excursions only. Refer to figure 3.

The reference voltage source is nominally — 1.28 volts and is of a modified bandgap type. Samples show average temperature coefficients of 40ppm/°C over the range — 55°C to 125°C.

The reference supply is internally compensated; however, to reduce the possibility of instability or noise generation, pin 21 shouls be decoupled to pin 23 with 2nF ceramic chip capacitor. The current loop technique (Fig 2) has been used with a high performance loop amplifier. The current is set by an external resistor as described above. Stabilization of the loop amplifier is achieved by a single capacitor from pin 23 to ground. Minimum value is 3900pF, although a 20nF chip ceramic is recommended.

Multiplying operation of the DAC is available in two modes, either a voltage applied in place of the reference, or a current supplied via the current source pin. In the former case the 3dB bandwidth os 250kHz, while in the latter, operational use is typically 25MHz. A suggested circuit is shown ib Fig. 4.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T = 25°C, Rset = 240Ω

VIH MAX	VIL MIN	VEE	VCC
—0.81	—1.85	—5.2	+5.0

Measurement of Settling Time

Oscilloscopes, whether real time or sampling do not have sufficiently low input VSWR or on-screen resolution for precise settling time measurements. A measurement technique has been devised, shown diagrammatically in Fig. 4, in which the DAC can settle into nearly ideal 50 ohm load, with minimal interconnection paths; this also very closely related to the practical use of the device. Precision settling time measurements can be performed with a high speed comparator, conveniently a dual device, such as the SP9687, with a minimal delay time, in this case about 2ns. Two references are set up to detect the DAC output settling within a window, conveniently defined as the settling to ground of the output.

The lower comparator detects when the DAC output has settled within 1/2 LSB of the final settling point, while the upper device when switched in checks that there is no overshoot. In fact, the settling is very well behaved, and after correction for comparator delay, the results consistently show a DAC settling time of 12ns, defined from the 50% point of the DAC input switching waveform. No correction has been made for the excess loading capacitance at the output node, so these results are considered to be conservative.

Don't miss the Sections on Semicustom ICs

Digital Gate Arrays, Standard Cells, and Linear Arrays Are All Covered

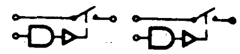
Vol. II, page 4425

Analog Switch Product Information

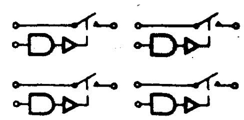
Drivers and Gates

Basic Part No. (Notes 1 & 2)	Switch Type	$r_{DS(on)}$ Max. (Ω) (Note 3)	Analog Voltage Range (p-p V) (Note 3)	Switching Time (μs) t_{ON}	Switching Time (μs) t_{OFF}	Logic Input for ON Switch	Logic Levels (V) V_{INL}	Logic Levels (V) V_{INH}	Opt. Sup. Voltage (V) (+) Sup. V_1	Opt. Sup. Voltage (V) (−) Sup. V_2	Opt. Sup. Voltage (V) Logic Sup. V_l	Comments
One Channel SPST												
DG5040	CMOS Plus-40	50	30	1.0	0.5	1	0.8	2.0	15	-15	5	
Two Channel SPST												
DGM111	PMOS	75-200	20	0.3	1.0	0	0.5	4.6	10	-20	5	
DG133	N-JFET	30	20	0.6	1.6	1	0.8	2.5	12	-18	—	See DG181 For New Design
DG134	N-JFET	80	20	0.6	1.6	1	0.8	2.5	12	-18	—	See DG182 For New Design
DG141	N-JFET	10	20	1.0	2.5	1	0.8	2.5	12	-18	—	See DG180 For New Design
DG151	N-JFET	15	15	1.0	2.5	1	0.8	2.5	15	-15	—	See DG180 For New Design
DG152	N-JFET	50	15	0.8	1.6	1	0.8	2.5	15	-15	—	See DG181 For New Design
DG180	N-JFET	10	20	0.3	0.25	0	0.8	2.0	10	-20	5	Break-Before-Make
		10	15	0.3	0.25	0	0.8	2.0	15	-15	5	15V Supplies
***DG181**	N-JFET	30	20	0.15	0.13	0	0.8	2.0	10	-20	5	Break-Before-Make
		30	15	0.15	0.13	0	0.8	2.0	15	-15	5	15V Supplies
***DG182**	N-JFET	75	20	0.25	0.13	0	0.8	2.0	10	-20	5	Break-Before-Make
		75	20	0.25	0.13	0	0.8	2.0	15	-15	5	15V Supplies
***DG200A**	CMOS Plus-40	70	30	1.0	0.5	0	0.8	2.0	15	-15	—	
DG281	N-JFET	300	20	0.15	0.13	0	0.8	2.0	15	-15	5	Break-Before-Make
***DG300A**	CMOS	50	30	0.300	0.250	1	0.8	4.0	15	-15	—	
***DG381A**	CMOS	50	30	0.300	0.250	0	0.8	4.0	15	-15	—	
***DG304A**	CMOS	50	30	0.250	0.150	1	3.5	11.0	15	-15	—	CMOS compatible
***DG5041**	CMOS Plus-40	50	30	1.0	0.5	1	0.8	2.0	15	-15	5	Break-Before-Make
Four Channel SPST												
***DG172**	PMOS	150-450	20	0.3	0.75	0	0.8	2.0	10	-20	5	
***DG201A**	CMOS Plus-40	175	30	0.6	0.45	0	0.8	2.0	15	-15	—	
*DG201HS	CMOS Plus-40	50	30	.05	.04	0	0.8	2.0	15	-15		Super Fast Switch
*DG221	CMOS Plus-40	100	30			0	0.8	2.4	15	-15		with input latches
***DG202**	CMOS Plus-40	175	30	0.6	0.45	1	0.8	2.0	15	-15	—	
***DG211**	CMOS Plus-40	175	30	1.0	0.5	0	0.8	2.0	15	-15	5	
***DG212**	CMOS Plus-40	175	30	1.0	0.5	1	0.8	2.0	15	-15	5	
***DG308A**	CMOS Plus-40	100	30	0.2	0.15	1	3.5	11.0	15	-15	—	Single Supply Operation
***DG309**	CMOS Plus-40	100	30	0.2	0.15	0	3.5	11.0	15	-15	—	Single Supply Operation

One Channel SPST



Two Channel SPST

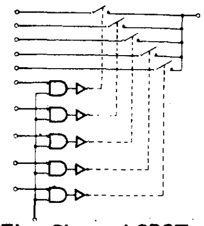


Four Channel SPST

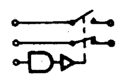
*Devices recommended for new designs are indicated in **bold face** type.

Analog Switch Product Information (Cont'd)

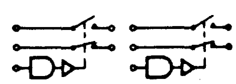
Drivers and Gates (Cont'd)



Five Channel SPST



One Channel SPDT



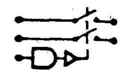
Two Channel SPDT

Basic Part No. (Notes 1 & 2)	Switch Type	$r_{DS(on)}$ Max. (Ω) (Note 3)	Analog Voltage Range (p-pV) (Note 3)	Switching Time (μs) t_{ON}	t_{OFF}	Logic Input for ON Switch	Logic Levels (V) V_{INL}	V_{INH}	Opt. Sup. Voltage (V) (+) Sup. V_1	(−) Sup. V_2	Logic Sup. V_l	Comments
Five Channel SPST												
DG125	PMOS	100-450	20	0.3	2.0	0	0.5	4.6	10	-20	5	
One Channel SPDT												
DG143	N-JFET	80	20	0.8	1.6	(Note 4)	2.0	3.0	12	-18	—	See DG188 For New Design
DG144	N-JFET	30	20	0.8	1.6	(Note 4)	2.0	3.0	12	-18	—	See DG187 For New Design
DG146	N-JFET	10	20	1.0	2.5	(Note 4)	2.0	3.0	12	-18	—	See DG186 For New Design
DG161	N-JFET	15	15	1.0	2.5	(Note 4)	2.0	3.0	15	-15	—	See DG186 For New Design
DG162	N-JFET	50	15	0.8	1.6	(Note 4)	2.0	3.0	15	-15	—	See DG187 For New Design
DG186	N-JFET	10	20	0.3	0.25	(Note 5)	0.8	2.0	10	-20	5	Break-Before-Make
	N-JEFT	10	15	0.3	0.25	(Note 5)	0.8	2.0	15	-15	5	15V Supplies
•DG187	N-JFET	30	20	0.15	0.13	(Note 5)	0.8	2.0	10	-20	5	Break-Before-Make
	N-JFET	30	15	0.15	0.13	(Note 5)	0.8	2.0	15	-15	5	15V Supplies
•DG188	N-JFET	75	20	0.25	0.13	(Note 5)	0.8	2.0	10	-20	5	Break-Before-Make
	N-JFET	75	20	0.25	0.13	(Note 5)	0.8	2.0	15	-15	5	15V Supplies
DG287	N-JFET	300	20	0.15	0.13	(Note 5)	0.8	2.0	15	-15	5	Break-Before-Make
•DG301A	CMOS	50	30	0.300	0.250	(Note 5)	0.8	4.0	15	-15	—	
•DG387A	CMOS	50	30	0.300	0.250	(Note 5)	0.8	4.0	15	-15	—	
•DG305A	CMOS	50	30	0.250	0.150	(Note 5)	3.5	11.0	15	-15	—	CMOS compatible
SI3002	PMOS	100-400	20	1.0	1.5	(Note 5)	0.8	2.0	10	-20	—	
•DG5042	CMOS Plus-40	50	30	1.0	0.5	(Note 5)	0.8	2.0	15	-15	5	Break-Before-Make
Two Channel SPDT												
DG189	N-JFET	10	20	0.3	0.25	(Note 5)	0.8	2.0	10	-20	5	Break-Before-Make
	N-JFET	10	15	0.3	0.25	(Note 5)	0.8	2.0	15	-15	5	15V Supplies
•DG190	N-JFET	30	20	0.15	0.13	(Note 5)	0.8	2.0	10	-20	5	Break-Before-Make
	N-JFET	30	15	0.15	0.13	(Note 5)	0.8	2.0	15	-15	5	15V Supplies
•DG191	N-JFET	75	20	0.25	0.13	(Note 5)	0.8	2.0	10	-20	5	Break-Before-Make
	N-JFET	75	20	0.25	0.13	(Note 5)	0.8	2.0	15	-15	5	15V Supplies
•DG243	CMOS Plus-40	50	30	1.0	0.5	(Note 5)	0.8	2.0	15	-15	5	Make-Before-Break
DG290	N-JFET	300	20	0.15	0.13	(Note 5)	0.8	2.0	15	-15	5	Break-Before-Make
•DG303A	CMOS	50	30	0.300	0.250	(Note 5)	0.8	4.0	15	-15	—	
•DG390A	CMOS	50	30	0.300	0.250	(Note 5)	0.8	4.0	15	-15	—	
•DG307A	CMOS	50	30	0.250	0.150	(Note 5)	3.5	11.0	15	-15	—	CMOS compatible
•DG5043	CMOS Plus-40	50	30	1.0	0.5	(Note 5)	0.8	2.0	15	-15	5	Break-Before-Make

•Devices recommended for new designs are indicated in **bold face** type.

Analog Multiplexer Product Information

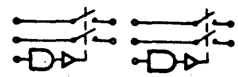
Basic Part No. (Notes 1 & 2)	Switch Type	$r_{DS(on)}$ Max. (Ω) (Note 3)	Analog Voltage Range (p-pV) (Note 3)	Switching Time (μs) t_{ON}	t_{OFF}	Logic Input for ON Switch	Logic Levels (V) V_{INL}	V_{INH}	Opt. Sup. Voltage (V) (+) Sup. V_1	(−) Sup. V_2	Logic Sup. V_l	Comments



One Channel DPST

One Channel DPST

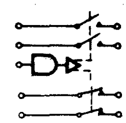
Basic Part No.	Switch Type	$r_{DS(on)}$	Analog Voltage Range	t_{ON}	t_{OFF}	Logic Input for ON Switch	V_{INL}	V_{INH}	V_1	V_2	V_l	Comments
***DG5044**	CMOS Plus-40	50	30	1.0	0.5	(Note 5)	0.8	2.0	15	−15	5	Break-Before-Make



Two Channel DPST

Two Channel DPST

Basic Part No.	Switch Type	$r_{DS(on)}$	Analog Voltage Range	t_{ON}	t_{OFF}	Logic Input for ON Switch	V_{INL}	V_{INH}	V_1	V_2	V_l	Comments
DG126	N-JFET	80	20	0.6	1.6	(Note 9)	0.8	2.5	12	−18	—	See DG185 For New Design
DG129	N-JFET	30	20	0.6	1.6	(Note 9)	0.8	2.5	12	−18	—	See DG184 For New Design
DG140	N-JFET	10	20	1.0	2.5	(Note 9)	0.8	2.5	12	−18	—	See DG183 For New Design
DG153	N-JFET	15	15	1.0	2.5	(Note 9)	0.8	2.5	15	−15	—	See DG183 For New Design
DG154	N-JFET	50	15	0.6	1.6	(Note 9)	0.8	2.5	15	−15	—	See DG185 For New Design
DG183	N-JFET	10	20	0.3	0.25	1	0.8	2.0	10	−20	5	Break-Before-Make
	N-JFET	10	15	0.3	0.25	1	0.8	2.0	15	−15	5	15V Supplies
***DG184**	N-JFET	30	20	0.15	0.13	1	0.8	2.0	10	−20	5	Break-Before-Make
	N-JFET	30	15	0.15	0.13	1	0.8	2.0	15	−15	5	15V Supplies
***DG185**	N-JFET	75	20	0.25	0.13	1	0.8	2.0	10	−20	5	Break-Before-Make
	N-JFET	75	20	0.25	0.13	1	0.8	2.0	15	−15	5	15V Supplies
DG284	N-JFET	300	20	0.15	0.13	1	0.8	2.0	15	−15	5	Break-Before-Make
***DG302A**	CMOS	50	30	0.300	0.250	1	0.8	4.0	15	−15	—	
***DG384A**	CMOS	50	30	0.300	0.250	1	0.8	4.0	15	−15	—	
***DG306A**	CMOS	50	30	0.250	0.150	1	3.5	11.0	15	−15	—	CMOS compatible
***DG5045**	CMOS Plus-40	50	30	1.0	0.5	1	0.8	2.0	15	−15	5	Break-Before-Make



One Channel DPDT

One Channel DPDT

Basic Part No.	Switch Type	$r_{DS(on)}$	Analog Voltage Range	t_{ON}	t_{OFF}	Logic Input for ON Switch	V_{INL}	V_{INH}	V_1	V_2	V_l	Comments
DG139	N-JFET	30	20	0.8	1.6	(Note 4)	2.0	3.0	12	−18	—	See DG191 For New Design
DG142	N-JFET	80	20	0.8	1.6	(Note 4)	2.0	3.0	12	−18	—	See DG190 For New Design
DG145	N-JFET	10	20	1.0	2.5	(Note 4)	2.0	3.0	12	−18	—	See DG189 For New Design
DG163	N-JFET	15	15	1.0	2.5	(Note 4)	2.0	3.0	15	−15	—	See DG189 For New Design
DG164	N-JFET	50	15	0.8	1.6	(Note 4)	2.0	3.0	15	−15	—	See DG191 For New Design

NOTES:

(1) *Devices recommended for new designs are indicated in **bold face** type.
(2) See individual data sheets for package and temperature designations.
(3) Analog voltage range is a function of supply voltages. Where a FET switch is PMOS or CMOS, r_{DS} is also a function of Supply Voltage and Analog Voltage. See individual data sheets for more detail.
(4) Input reference voltage of 2.5 V is required (see data sheets).
(5) See data sheet for switch state of differential switches.
(6) Current Driven Device I_{INH} = 1 mA.
(7) For truth table see data sheet.
(8) The appropriate switching characteristic for multiplexers is $t_{transition}$, not t_{ON}, t_{OFF}.
(9) Device normally operates with resistor to +10V.

Drivers for MOSFET Switches

These drivers were designed to function as a level shifter and buffer between low level logic and the control gate of FET analog switches. Output voltage ratings are as high as 50V.

Basic Part Number (Note 2)			Function and Uses	at Rated Current(s)	OFF Level $V_{(OUT)OFF}$ at Rated Current or $I_{(OUT)OFF}$ at Rated Voltage	Input Logic for V_{OUT} (low)	V_{INL} (V)	V_{INH} (V) (I_{INH}) (mA)	Optimum Supply Voltage (V) V_1	V_2	V_L	V_R	Switching Time (µs) t_{ON}	t_{OFF}
D125	6	6	Six Separate MOSFET Drivers	0.4V@5mA	0.1µA@10V	0	0.5	4.6	(Note 9)	-20	5	–	0.5	1.2
D129	7	4	Four Channel (BV = 50) MOSFET Driver with Decode	0.7V@10mA	0.1µA@10V	1	0.7	2.2	(Note 9)	-20	–	–	0.25	0.8
													t_d+	t_d-
*D169	2	4	Dual High-Speed Drivers with Complementary Outputs designed to drive high-capacity loads.	1.2V@1mA 3.0V@40mA	1.1V@1mA 2.5V@40mA	Output & Complement Available	0.8 0.8	2.0 2.0	15 15	-15 -15	5 5	0 0	0.17 0.17	0.20 0.20
				V_{OH}	V_{OL}									
*D469	4	4	Quad High Speed Driver	V_{DD} -2.0V @200mA V_{DD} -0.2V @10mA	2.0V@200mA 0.2V@10mA	1	0.8	2.0	+12V, GND				0.045	
Si7250	4	8	Quad High Speed Driver	V_{DD} -2.0V @200mA V_{DD} -0.2V @10mA	2.0V@200mA 0.2V@10mA	Output & Complement Available	0.8	2.0	+12V, GND				0.150	

Multiple FET Switches

Siliconix P-Channel MOSFET & DMOS Switches are available for such applications as sequential switching (commutation), signal processing, modulation, and A-to-D conversion. The MOSFET is normally OFF. These devices are also available with Siliconix drivers in a single package.

Basic Part Number (Note 2)	Circuit Function SOURCES	DRAINS	GATES	Switch Type	Pull Up On Gate	r_{DS} Max. (V) @ V_S = +10V	@ V_S = −10V	BV_{DSS}	$I_{S(off)}$ (nA)	$V_{GS(th)}$ Min.	Max.	C_{gs} Typ. (pF)	C_{ds} Typ. (pF)	C_{sb} Typ. (pF)
G115	6	1	6	SP6T	Yes	100	450	-30	0.5	-1.5	-4.0	0.9	0.4	2
G118	6	1	8	SP6T	No	100	450	-30	0.5	-1.5	-4.0	0.9	0.4	2
G119	6	2	3	DP3T	Yes	100	450	-30	0.5	-1.5	-4.0	1.8	0.4	2
G122	4	2	2	DPDT	Yes	100	450	-30	0.5	-1.5	-4.0	1.8	0.4	2
G123	4	2	4	2×SPDT	Yes	100	450	-30	0.5	-1.5	-4.0	1.8	0.4	2
***SD5000**	4	4	4	4×SPST	No	50		20	10.0	0.1	2.0	3.5	0.5	4
***SD5001**	4	4	4	4×SPST	No	50		10	10.0	0.1	2.0	3.5	0.5	4
***SD5002**	4	4	4	4×SPST	No	50		15	10.0	0.1	2.0	3.5	0.5	4
***SD5200**	4	4	4	4×SPST	No	80		30	1000	0.5	2.0	3.5	0.5	4

NOTES:

(1) *Devices recommended for new designs are indicated in **bold face** type.
(2) See individual data sheets for package and temperature designations.
(9) Device normally operates with resistor to +10V.

Pulse Width Modulators

Basic Part Number (Note 2)	Function and Uses	Operating Freq.	V_{OL} @ Rated Current	V_{OH} @ Rated Current	Supply Voltage
*PWM25	Pulse Width Modulator for SMPS to drive NPN or N channel MOSPOWER Devices	10Hz-400kHz with Dead Time Adjust	0.4V @ 20mA 2.5V @ 100mA	V+ −2V@20mA V+ −3V@100mA	+8.5V to +35V
*PWM27	Pulse Width Modulator for S SMPS to drive PNP or P channel MOSPOWER Devices	10Hz-400kHz with Dead Time	0.4V @ 20mA 2.5V @ 100mA	V+ −2V@20mA V+ −3V@100mA	+8.5V to +35V
*PWM125	Pulse Width Modulator for SMPS to drive N channel MOS-POWER Devices	10Hz - 800kHz with 100ns Dead Time	0.4V @ 20mA 2.5V @ 100mA	V+ −2V@20mA V+ −3V@100mA	+8.5V to +35V
*PWM127	Pulse Width Modulators for SMPS to drive P channel MOS-POWER Devices	10Hz - 800kHz with 100ns Dead	0.4V @ 20mA 2.5V @ 100mA	V+ −2V@20mA V+ −3V@100mA	+8.5V to +35V

Voltage Converters

Basic Part Number (Note 2)	Function and Uses	Input Voltage Range	Quiescent Current	Output Voltage	Output Voltage @ Output Current
Si7661	Voltage Doubler/Inverter	+4.5V to +20V	2mA Max	−20V to +20V	−18V to +18V @ 20mA
Si7660	Voltage Converter/Inverter	+1.5V to +10.0V	See Data Sheet	−1.5V to −10.0V	See Data Sheet

NOTES:

(1) *Devices recommended for new designs are indicated in **bold face** type.
(2) See individual data sheets for package and temperature designations.
(3) Analog voltage range is a function of supply voltages. Where a FET switch is PMOS or CMOS, r_{DS} is also a function of Supply Voltage and Analog Voltage. See individual data sheets for more detail.
(4) Input reference voltage of 2.5 V is required (see data sheets).
(5) See data sheet for switch state of differential switches.
(6) Current Driven Device i_{INH} = 1 mA.
(7) For truth table see data sheet.
(8) The appropriate switching characteristic for multiplexers is $t_{transition}$, not t_{ON}, t_{OFF}.
(9) Device normally operates with resistor to +10V.

Analog Multiplexer Product Information

Basic Part No. (Notes 1 & 2)	Switch Type	$r_{DS(on)}$ Max. (Ω) (Note 3)	Analog Voltage Range (p-pV) (Note 3)	Switching Time (μs) t_{ON}	Switching Time (μs) t_{OFF}	Logic Input for ON Switch	Logic Levels (V) V_{INL}	Logic Levels (V) V_{INH}	Opt. Sup. Voltage (V) (+) Sup. V_1	Opt. Sup. Voltage (V) (−) Sup. V_2	Opt. Sup. Voltage (V) Logic Sup. V_l	Comments
Eight Channel MUX + Enable												
DG501	PMOS	150-250	10	1.5	(Note 8)	(Note 7)	0.6	3.5	5	-20	—	Logic Pullup Resistors
DG503	PMOS	150-800	20	1.5	(Note 8)	(Note 7)	0.6	8.5	10	-20	—	Note 9
***DG508A**	CMOS Plus-40	400	30	1.0	(Note 8)	(Note 7)	0.8	2.0	15	-15	—	
***DG528**	CMOS Plus-40	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	-15	—	With Input Latches
SI3705	PMOS	150-400	10	1.5	(Note 8)	(Note 7)	0.6	3.5	5	-20	—	See DG501/No Pullup Resistors
Sixteen Channel MUX + Enable												
***DG506A**	CMOS Plus-40	400	30	1.0	(Note 8)	(Note 7)	0.8	2.0	15	-15	—	Break-Before-Make
*DG526	CMOS Plus-40	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	−15	—	Break-Before-Make
Four Channel Differential MUX												
***DG509A**	CMOS Plus-40	400	30	1.0	(Note 8)	(Note 7)	0.8	2.0	15	-15	—	Break-Before-Make
***DG529**	CMOS Plus-40	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	-15	—	With Input Latches
Eight Channel Differential MUX + Enable												
***DG507A**	CMOS Plus-40	400	30	1.0	(Note 8)	(Note 7)	0.8	2.0	15	-15	—	Break-Before-Make
*DG527	CMOS Plus-40	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	−15	—	With Input Latches
Four Channel SPDT D/A Converter Summing Node Switches												
DG515	NMOS	See Comments	—	0.120	0.170	(Note 5)	0.5	7.5	8.0	0	—	$R_1 = 6.25Ω$, $R_2 = 12.5Ω$, $R_3 = 25Ω$, $R_4 = 50Ω$
Ten Channel SPDT D/A Converter Summing Node Switches												
DG516	NMOS	See Comments	—	0.120	0.170	(Note 5)	0.5	7.5	8.0	0	—	$R_1 = 100Ω$, $R_2 = 200Ω$, $R_3 = 400Ω$, $R_4 = 800Ω$, $R_5 = 1600Ω$, $R_{6-10} = 3200Ω$

NOTES:

(1) *Devices recommended for new designs are indicated in **bold face** type.
(2) See individual data sheets for package and temperature designations.
(3) Analog voltage range is a function of supply voltages. Where a FET switch is PMOS or CMOS, r_{DS} is also a function of Supply Voltage and Analog Voltage. See individual data sheets for more detail.
(4) Input reference voltage of 2.5 V is required (see data sheets).
(5) See data sheet for switch state of differential switches.
(6) Current Driven Device I_{INH} = 1 mA.
(7) For truth table see data sheet.
(8) The appropriate switching characteristic for multiplexers is $t_{transition}$, not t_{ON}, t_{OFF}.
(9) Device normally operates with resistor to +10V.

Linear and Data Conversion Product Information

A/D and D/A Converters

3 1/2-Digit High Performance Integrating A/D Converter	**LD110/LD111A** 16-pin plastic DIPs	±3 1/2-Digit Resolution Accuracy 0.02% ±1 count Auto zero Auto polarity 10μV resolution Typical TC of 5 ppm/°C A usable 20mV scale	Three voltage ranges: 1.999V, 199.9mV & 19.99mV Sampling rate up to 40 samples/s Differential input capability Over-range & under-range signals TTL compatible
4 1/2-Digit Integrating A/D Converter	**LD120/121A** 16-pin & 18-pin plastic DIP respectively	±4 1/2-Digit Resolution Accuracy 0.005% ±1 count Auto zero Auto polarity TTL compatible Internal clock Linear to 28,500 counts	Two voltage ranges: 2.0V & 200.00mV 1 to 5 samples/s 25% inter-digit blanking MUX BCD outputs 0.5 count stability on 2.0V range Monolithic design
4 1/2-Digit Integrating A/D Converter	**LD122/121A** 16-pin & 18-pin plastic DIP respectively	±4 1/2-Digit Resolution Accuracy 0.005% ±1 count 1μV resolution for 20 mV FS Auto zero Auto polarity TTL compatibility Internal clock Linear to 28,500 counts	Same as LD120/121A but does not have internal input buffer amplifier
4 1/2-Digit Integrating A/D Converter	Si7135	±4 1/2-Digit Resolution Accuracy ±.005% ±1 count 2 Volts full scale Auto-zero TTL Compatible	Monolithic Construction Six Auxiliary I/O's are available for interfacing Micro-processors and UARTS 28 lead plastic pkg.
12 bit D/A Converter	Si7622	12 bit Multiplying D/A 12 bit Linearity Guaranteed Monotonic Single Supply Double Buffered Input Registers	Monolithic Construction 28 pin Plastic & Cerdip Micro-processor compatible
8 bit Data Acquisition System	Si520	8 bit by 8 Channel Data Acquisition System Ratiometric Conversion No Missing Codes Built-in 8-input Analog Multiplexer	28 pin Plastic Pkg. Latched 3 state outputs Latched Address Inputs Single 5V Supply

Micropower Linear IC's

Triple Op Amp	**L144** 14-pin plastic, ceramic, flat-pack & Dice	±1.5 to ±18V supply Programmable supply current Internally compensated 0.4V/μs slew rate	80dB gain with 20kΩ load Drive large capacitive loads ±30V differential input Monolithic construction
Quad Comparator	**L161** 16-pin plastic, ceramic, flat-pack & Dice	±1.5 to ±18V supply Single supply operation Programmable supply current 3V/μs slew rate	Gain greater than 20V/mV Sensing near ground ±30V differential input CMOS Logic compatible

Analog Switches and Multiplexers JAN38510

Several Siliconix Analog Switches and Multiplexers are available fully certified on the QPL (Qualified Parts List) published monthly by Defense Electronics Supply Center (DESC). The QPL numbers follow this format: JM38510/XXXXX. Refer to the current Siliconix Price List for available part types and order numbers.

JAN Part Numbering System

J M38510 / 111 07 B E C

- J — **"JAN" Certification Mark**
- M38510 — **Military Designator**
- 111 — **Detail Specification (Slash Sheet)**
  - /111—DG181 Series
  - /116—DG300 Series
  - /123—DG200 A Series
  - /190—DG506 A Series
- 07 — **Device Type**
- B — **Device Class**
  - S—Class S
  - B—Class B
  - C—Class C
- E — **Case Outline**
  - C—14-Lead side braze
  - E—16-Lead side braze
  - I—10-Lead can
- C — **Lead Finish**
  - A—Solder dip
  - B—Bright tin plate
  - C—Gold Plate

	Device Type	
/111	01—DG181	05—DG187
	02—DG182	06—DG188
	03—DG184	07—DG190
	04—DG185	08—DG191
/116	01—DG300	05—DG304
	02—DG301	06—DG305
	03—DG302	07—DG306
	04—DG303	08—DG307
/123	01—DG200A	02—DG201A

Part Number	Order Part Number	Generic Part Number
JM38510/11101BCC	SJM181BCC	DG181AP/883
JM38510/11101BIC	SJM181BIC	DG181AA/883
JM38510/11102BCC	SJM182BCC	DG182AP/883
JM38510/11102BIC	SJM182BIC	DG182AA/883
JM38510/11103BEC	SJM183BEC	DG184AP/883
JM38510/11104BEC	SJM185BEC	DG185AP/883
JM38510/11105BCC	SJM187BCC	DG187AP/883
JM38510/11105BIC	SJM187BIC	DG187AA/883
JM38510/11106BCC	SJM188BCC	DG188AP/883
JM38510/11106BIC	SJM188BIC	DG188AA/883
JM38510/11107BEC	SJM190BEC	DG190AP/883
JM38510/11108BEC	SJM191BEC	DG191AP/883
JM38510/11601BCC	SJM300BCC	DG300AP/883
JM38510/11601BIC	SJM300BIC	DG300AA/883
JM38510/11602BCC	SJM301BCC	DG301AP/883
JM38510/11602BIC	SJM301BIC	DG301AA/883
JM38510/11603BCC	SJM302BCC	DG302AP/883
JM38510/11604BCC	SJM303BCC	DG303AP/883
JM38510/11605BCC	SJM304BCC	DG304AP/883
JM38510/11605BIC	SJM304BIC	DG304AA/883
JM38510/11606BCC	SJM305BCC	DG305AP/883
JM38510/11606BIC	SJM305BIC	DG305AA/883
JM38510/11607BCC	SJM306BCC	DG306AP/883
JM38510/11608BCC	SJM307BCC	DG307AP/883
JM38510/12303BCC	SJM200BCC	DG200A AP/883
JM38510/12303BIC	SJM200BIC	DG200A AA/883
JM38510/12304BEC	SJM201BEC	DG201A AP/883

Fast CMOS Gate Arrays

The Siliconix family of CMOS gate arrays has been specifically designed to offer a fast and easy way to design your own custom integrated circuits. These FAST CMOS gate arrays offer virtually all the benefits of a full custom design at a fraction of the cost and time usually associated with full custom development programs.

Designing with our "State-of-the Art" silicon gate process is as easy as designing with standard "Off-the-Shelf" components. All the information necessary for you to begin your custom IC is contained in our design manual.

No Previous IC Design Experience Necessary

Our design manual walks you through the complete design process. All the information necessary to take your conceptual design through the breadboard stage to the final prototype evaluation is discussed, with numerous examples given. Over 100 macrocells are included in the manual to assist in converting your logic diagrams to the gate level. Our applications engineers are always available to answer any questions you may have concerning the design and integration of your gate array. Included in the design manual are 200X layout sheets, macrocell planning sheets, test planning sheets, and other tools developed by IC design experts.

A Wide Selection of Arrays to Choose From

Siliconix currently offers two families of oxide-isolated, silicon-gate arrays. Each family consists of seven different chips ranging in size from 360 to 1500 gates. A complete table of the arrays is shown in Table 1. The array family is determined by the process that is employed to fabricate the chips. The ISO-3 and ISO-5 refer to the design rules used for the gate masking step. Typical gate delays for each series are shown in Table 2 for V_{DD} of 5 volts.

Designation	Chip Size	Total Cells	Gate Equivalent	I/O Buffers	Bonding Pads
ISO5A/ISO3A	118x140	240	360	36	46
ISO5B/ISO3B	132x167	360	540	48	58
ISO5C/ISO3C	159x167	480	720	54	64
ISO5D/ISO3D	161x208	640	960	62	72
ISO5E/ISO3E	188x208	800	1200	68	78
ISO5F/ISO3F	188x244	1000	1500	76	86
ISO5G/ISO3G	214x244	1200	1800	84	92

TABLE 1

Family of Arrays

Typical Gate Delays (ns) F.O. = 2

ISO-5				ISO-3			
GATE TYPE	Tr	Td	Tpd	GATE TYPE	Tr	Td	Tpd
INVERTER	4.3	1.7	3.0	INVERTER	1.35	0.45	0.9
2-INPUT NAND	4.5	3.5	4.0	2-INPUT NAND	1.5	1.0	1.25
2-INPUT NOR	9.5	2.1	5.8	2-INPUT NOR	2.85	0.55	1.7
3-INPUT NAND	4.8	6.0	5.4	3-INPUT NAND	1.6	1.7	1.65
3-INPUT NOR	13	2.5	7.8	3-INPUT NOR	4.4	0.6	2.5
4-INPUT NAND	5.0	7.0	6.0	4-INPUT NAND	1.7	2.3	2.0

TABLE 2

Macrocells

Our design manual contains over 100 characterized, pre-designed macrocells for virtually all SSI functions. When these macrocells are used, all contact opening and metal routing within the cell is done automatically, eliminating the possibility of error when the function is implemented. The following example of the implementation of an exclusive-OR gate should help illustrate this point. The schematic is shown for reference only and is not necessary for the implementation of the function. The macrocell for an exclusive-OR gate is found in the design manual listing for exclusive-OR gates. Note that several different versions can be implemented. The macrocell chosen for this example is XO1A, as illustrated in Figure 3.

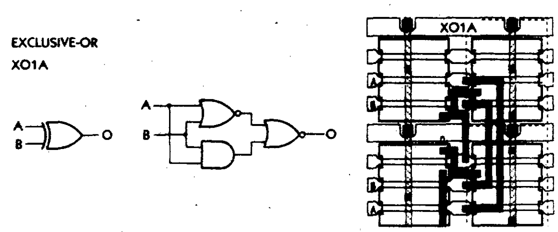


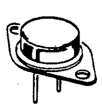
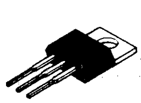
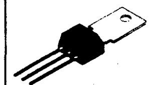
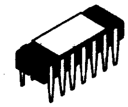
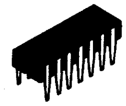
Figure 3

Input/Output Buffers

The ISO series has very powerful I/O buffers designed to be direct TTL-compatible, capable of sinking 6mA at 0.4V or 24mA at 2.5V (V_{DD} = 5.0V). Each p-buffer can source 2mA at 4.6V or 10mA at 2.5V. There are three transistors (one single and one double) in each buffer device which can be connected as desired for any particular application. All the output devices are fully guardbanded.

Siliconix MOSPOWER
Prime Products Selector Guide

* 200°C RATING

Packages:								
BV_{DSS} (Volts)	TO-3	TO-220	TO-39	TO-237	TO-92	TO-202	Quad Side Braze	Quad Plastic
600-650	VNT008A 6A, 1.5Ω, 650V	VNT008D 6A, 1.5Ω, 650V						
450-500	VNP006A 20A, 0.3Ω, 500V	IRF840 8A, 0.85Ω, 500V						
	IRF450 13A, 0.4Ω, 500V	VN5001D/IRF830 4.5A, 1.5Ω, 500V						
	IRF440 8A, 0.85Ω, 500V	IRF820 2.5A, 3Ω, 500V						
	VNP002A* 6.5A, 1.5Ω, 500V							
	VN5001A/IRF430 4.5A, 1.5Ω, 500V							
	IRF420 2.5A, 3Ω, 500V							
350-400	VNM005A 25A, 0.2Ω, 400V	IRF740 10A, 0.55Ω, 400V						
	IRF350 15A, 0.3Ω, 400V	VN4000D/IRF730 5.5A, 1.0Ω, 400V						
	IRF340 10A, 0.55Ω, 400V	IRF720 3A, 1.8Ω, 400V						
	VNM001A* 8A, 1.0Ω, 400V							
	VN4000A/IRF330 5.5A, 1.0Ω, 400V							
	IRF320 3.0A, 1.8Ω, 400V							
120-240	VNJ004A 45A, 0.06Ω, 200V	VN2406D 1.4A, 6Ω 240V	VN2406B 0.8A, 6Ω, 240V	VN2406M 0.3A, 6Ω, 240V	VN2406L 0.21A, 6Ω, 240V			
	IRF250 30A, 0.085Ω, 200V	IRF640 18A, 0.18Ω, 200V		VN2410M 0.25A, 10Ω, 240V	VN2410L 0.16A, 10Ω, 240V			
	IRF240 18A, 0.18Ω, 200V	IRF630 9A, 0.4Ω, 200V			BS107 .1A, 28Ω, 200V			
	IRF230 9A, 0.4Ω, 200V	IRF620 5A, 0.8Ω, 200V						
	IRF220 5A, 0.8Ω, 200V							
60-100	VNE003A 60A, 0.035Ω, 100V	IRF540 27A, 0.085Ω, 100V	IRFF130 8A, 0.18Ω, 100V	VP1008M 0.37A, 5Ω, - 100V	VP1008L 0.23A, 5Ω, - 100V	VN88AF 1.5A, 4Ω, 80V	VQ1006P 0.40A, 4.5Ω, 90V	VQ1006J 0.40A, 4.5Ω, 90V
	IRF150 40A, 0.055Ω, 100V	VN1000D/IRF530 12A, 0.18Ω, 100V	IRFF120 6A, 0.30Ω, 100V	VN0808M 0.35A, 4Ω, 80V	VN0610L * 0.2A, 5Ω, 60V	VN80AF 1.3A, 5Ω, 80V	VQ2006P 0.41A, 5Ω, - 90V	VQ2006J 0.41A, 5Ω, - 90V
	IRF140 27A, 0.085Ω, 100V	IRF520 8A, 0.30Ω, 100V	VNE011B 4A, 0.5Ω, 100V	VN0606M 0.4A, 3Ω, 60V	VN0610LL 0.2A, 5Ω, 60V	VN66AF 1.7A, 3Ω, 60V	VQ1004P 0.46A, 3.5Ω, 60V	VQ1004J 0.46A, 3.5Ω, 60V
	VN1000A/IRF130 12A, 0.18Ω, 100V	VN88AD 1.7A, 4Ω, 80V	VP1008B 0.9A, 5Ω, - 100V	VN10KM * 0.3A, 5Ω, 60V	BS170 .2A, 5Ω, 60V	VN67AF 1.6A, 3.5Ω, 60V	VQ1000P 0.225A, 5.5Ω, 60V	VQ1000J 0.225A, 5.5Ω, 60V
	IRF120 8A, 0.3Ω, 100V	VN0600D 16A, 0.12Ω, 60V	2N6661 ** 0.9A, 4Ω, 90V	VN10LM 0.3A, 5Ω, 60V	VN2222L * 0.15A, 7.5Ω, 60V		VQ2004P 0.41A, 5Ω, - 60V	VQ2004J 0.41A, 5Ω, - 60V
	VN0600A 16A, 0.12Ω, 60V	VN66AD 1.9A, 3Ω, 60V	2N6660 1.1A, 3Ω, 60V	VN2222LM 0.25A, 7.5Ω, 60V	VN2222LL 0.15A, 7.5Ω, 60V			
30-50	VN0400A 16A 0.12Ω, 40V	VN0400D 16A, 0.12Ω, 40V	2N6659 1.4A, 1.8Ω, 35V	VN0300M 0.7A, 1.2Ω, 30V	BS250 .1A, 14Ω, -45V	VN46AF 1.6A, 3Ω, 40V	VQ1001P 0.85A, 1.0Ω, 30V	VQ1001J 0.85A, 1.0Ω, 30V
	2N6656 2A, 1.8Ω, 35V	VN0300D 2.5A, 1.5Ω, 30V	VP0300B 1.3A, 2.5Ω, - 30V	VP0300M 0.48A, 2.5Ω, - 30V	VP0300L .3A, 2.5Ω, -30V	VN40AF 1.3A, 5Ω, 40V	VQ2001P 0.60A, 2Ω, -30V	VQ2001J 0.60A, 2Ω, - 30V
Specialty Products (N- and P-Channel Quad Arrays)							VQ3001P ± 30V, 3Ω Total	VQ3001J ± 30V, 3Ω Total
							VQ7254P ± 20V, 3Ω Total	VQ7254J ± 20V, 3Ω Total

* Zener Protected Gate ** JAN/JANTX/JANTXV QPL

(shaded) P-CHANNEL

Siliconix

SPRAGUE®
THE MARK OF RELIABILITY
a Penn Central unit

PERIPHERAL/DISPLAY DRIVER IC REFERENCE

Sink or Source in order of (1) output current rating, (2) output voltage rating, (3) number of drivers

SINK DRIVERS

TYPICAL DRIVING APPLICATIONS — DISPLAYS: LED	V. FLUOR.	GAS DIS.	INCAND.	INDUCTIVE: SOLENOID	MOTOR	PRINTERS: THERMAL	ELECTRO. SENS.	OUTPUTS* mA	V	#	SPRAGUE PART NUMBER	EXTENDED TEMP. MILITARY HERM. AVAILABLE
—	—	✓	—	—	—	—	—	20	−115	8	SERIES UDN-7180A	✓
✓	—	—	✓	—	—	✓	—	100	20	8¶	UDN-2595A	✓
✓	—	—	✓	✓	✓	✓	—	250	100	4¶	SERIES UHP-400/500	✓
SCR ARRAY			✓	✓	—	—	—	275	35	6†	UTN-2886B	—
SCR ARRAY			✓	✓	—	—	—		35	8†	UTN-2888A	—
✓	—	—	✓	✓	✓	✓	—	300	80	2¶	SERIES UDN-3610M	✓
✓	—	—	✓	✓	✓	✓	—		80	2¶	SERIES UDN-5710M	✓
✓	—	—	✓	✓	✓	✓	—		80	4¶	SERIES UDN-5700A	✓
PIN DIODE DRIVER				—	—	—	—		120	4	UDN-5791A	✓
✓	—	—	✓	✓	✓	✓	✓	350	50	4†	UCN-4401A	✓
✓	—	—	✓	✓	✓	✓	—		50	7	SERIES ULN-2000A	✓
✓	—	—	✓	✓	✓	✓	—		50	8	SERIES ULN-2800A	✓
✓	—	—	✓	✓	✓	✓	✓		50	8†	UCN-4801A	✓
✓	—	—	✓	✓	—	✓	✓		50	8†	UCN-4821A	✓
✓	—	—	✓	✓	✓	✓	—		70	2¶	SERIES UDN-5720M	✓
✓	—	—	✓	✓	—	—	✓		80	8†	UCN-4822A	✓
✓	—	✓	✓	✓	✓	—	—		95	7	SERIES ULN-2020A	✓
✓	—	✓	✓	✓	✓	—	—		95	8	SERIES ULN-2820A	✓
✓	—	✓	✓	✓	—	—	✓		100	8§	UCN-4823A	✓
STEPPER MOTOR DRIVER				—	✓	—	—	500	50	4	UCN-4202/03A	✓
✓	—	—	✓	✓	✓	✓	—		50	7	SERIES ULN-2010A	✓
✓	—	—	✓	✓	✓	✓	—		50	8	SERIES ULN-2810A	✓
✓	—	—	✓	✓	—	✓	—		50	8†¶	UCN-4807/08A	✓
✓	—	—	✓	✓	✓	✓	—	600	70	2¶	SERIES UDN-5730/40M	✓
✓	—	—	✓	✓	✓	—	—	1000	80	4¶	UDN-2542B	—
✓	—	—	✓	✓	✓	—	—	1250	50	2	ULN-2061M	—
✓	—	—	✓	✓	✓	—	—		50	4	SERIES ULN-2064B	✓
✓	—	—	✓	✓	✓	—	—		60	4¶	UDN-2541B	—
✓	—	—	—	✓	✓	—	✓	1500	−50	4	UDN-2841/45B	—
✓	—	—	✓	✓	✓	—	—		80	2	ULN-2062M	—
✓	—	—	✓	✓	✓	—	—		80	4	SERIES ULN-2065B	✓
HALF-BRIDGE				—	✓	—	—	±2000	30	1	UDN-2949Z	—
HALF-BRIDGE				—	✓	—	—		35	1	UDN-2935/50Z	—
FULL-BRIDGE				—	✓	—	—		40	1	UDN-2952B/W	—
—	—	—	—	✓	—	—	—	±4000	60	2	UDN-2975/76W	—
✓	—	—	✓	✓	✓	—	—	4000	80	4	UDN-2878/79W	—

SOURCE DRIVERS

LED	V. FLUOR.	GAS DIS.	INCAND.	SOLENOID	MOTOR	THERMAL	ELECTRO. SENS.	mA	V	#	SPRAGUE PART NUMBER	EXTENDED TEMP. MILITARY HERM. AVAILABLE
—	✓	—	—	—	—	—	—	−25	±40	8	UDN-6138/48A	—
✓	✓	—	—			DECODER/DRIVERS			60	8†	UCN-4805A	—
✓	✓	✓	—	—	—	✓	—		60	20§	UCN-5812A	✓
✓	✓	✓	—	—	—	✓	—		60	32§	UCN-5818A	✓
—	✓	✓	—	—	—	✓	—		80	8†	UCN-4815A	✓
✓	✓	✓	—	—	—	✓	—		80	10§	UCN-4810A	✓
✓	✓	✓	—	—	—	✓	—		80	10§	UCN-5810A	✓
—	✓	✓	—	—	—	—	—		115	6	UDN-6116A	✓
—	✓	✓	—	—	—	—	—		115	8	UDN-6118A	✓
—	✓	✓	—	—	—	—	—		140	8	UDN-6514A	—
—	—	✓	—	—	—	—	—		200	8	UDN-6510A	—
✓	—	—	✓	✓	✓	✓	—	−120	25	8¶	UDN-2585A	✓
✓	—	—	✓	✓	✓	✓	✓	−350	50	8	UDN-2981/82A	✓
✓	—	—	✓	✓	✓	✓	✓		50	8§	UCN-5890A	✓
✓	✓	—	✓	✓	✓	✓	✓		80	8	UDN-2983/84A	✓
—	—	—	—	✓	—	—	—		−80	5	UDN-2956/57A	—
✓	✓	—	✓	✓	—	—	—		−80	8	UDN-2580A	✓
✓	—	—	✓	✓	—	—	—		−80	8	UDN-2588A	✓
✓	—	—	✓	✓	✓	—	—	−1500	30	4	UDN-2941B/W	—
✓	—	—	—	✓	✓	—	✓		−50	4	UDN-2845B	—
HALF-BRIDGE				—	✓	—	—	±2000	30	1	UDN-2949Z	—
HALF-BRIDGE				—	✓	—	—		35	1	UDN-2935/50Z	—
FULL-BRIDGE				—	✓	—	—		40	1	UDN-2952B/W	—
—	—	—	—	✓	—	—	—	±4000	60	2	UDN-2975/76W	—

**Current is maximum tested condition, voltage is absolute maximum rating.* †*Latched Drivers.* §*Serial-input, latched parallel-outputs.* ¶*Saturated, non-Darlington outputs for low-voltage applications.*

For application engineering assistance, write or call Semiconductor Division, Sprague Electric Company, 115 Northeast Cutoff, Worcester, Mass. 01606. Tel. 617/853-5000.

For the name of your nearest Sprague Semiconductor Distributor, write or call Sprague Products Division, Sprague Electric Company, North Adams, Mass. 01247. Tel. 413/664-4481.

4SS-2159R1

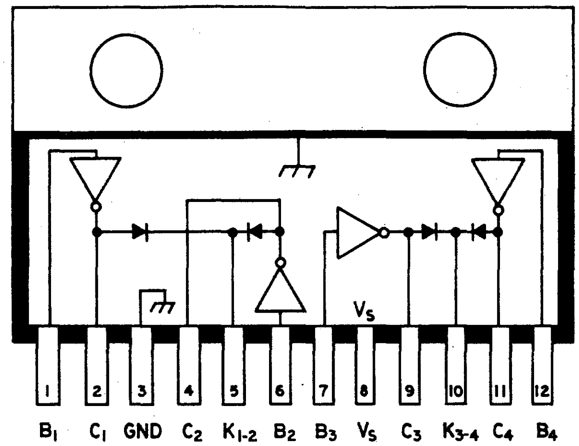
SPRAGUE THE MARK OF RELIABILITY a Penn Central unit

QUAD HIGH-CURRENT DARLINGTON SWITCH ICs

UDN-2878W AND UDN-2879W QUAD HIGH-CURRENT DARLINGTON SWITCHES

FEATURES

- Output Currents to 4 A
- Output Voltages to 80 V
- Loads to 1280 W
- TTL, DTL, or CMOS Compatible Inputs
- Internal Clamp Diodes
- Plastic Single In-Line Package
- Heat-Sink Tab



DWG. NO. A-11,974

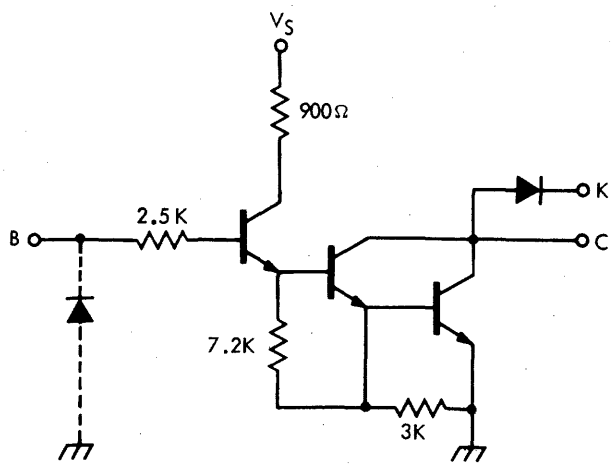
THESE QUAD DARLINGTON ARRAYS are designed to serve as interface between low-level logic and peripheral power devices such as solenoids, motors, incandescent displays, heaters, and similar loads of up to 320 W per channel. Both integrated circuits include transient-suppression diodes that enable use with inductive loads. The input logic is compatible with most TTL, DTL, LS TTL, and 5 V CMOS logic.

For maximum power-handling capability, all drivers are supplied in a 12-pin single in-line power-tab package. The tab is at ground potential and needs no insulation. External heat sinks are usually required for proper operation of these devices.

Similar integrated circuits (Types UDN-2068B and UDN-2069B) are available in 16-pin dual in-line packages for operation with load currents of up to 1.5 A per channel. They are described in the most recent issue of Sprague Engineering Bulletin 29305.

Device	Sustaining Voltage	Output Voltage	Output Current
UDN-2878W	35 V	50 V	4 A
UDN-2878W-2	35 V	50 V	3 A
UDN-2879W	50 V	80 V	4 A
UDN-2879W-2	50 V	80 V	3 A

PARTIAL SCHEMATIC
One of 4 Drivers



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Write for Engineering Bulletin 29305.10 to Technical Literature Service, Sprague Electric Company, 647 Marshall St., North Adams, Mass. 01247

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SPRAGUE® THE MARK OF RELIABILITY a Penn Central unit

FULL-BRIDGE MOTOR DRIVER INTEGRATED CIRCUITS

UDN-2952B AND UDN-2952W FULL-BRIDGE MOTOR DRIVERS

FEATURES

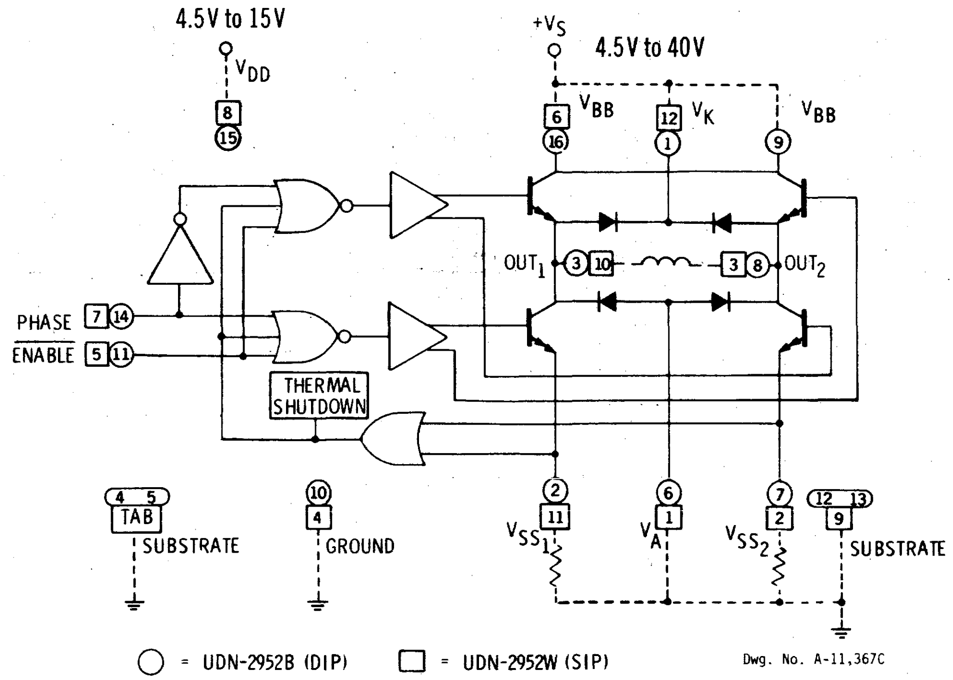
- Output Currents to ±3.5A
- Output Voltages to 40V
- Adjustable Short-Circuit Protection
- Thermal Protection
- Internal Clamp Diodes
- TTL, DTL, PMOS, CMOS Compatible
- DIP or SIP Packaging

FULL-BRIDGE MOTOR-DRIVER integrated circuits, Types UDN-2952B and UDN-2952W combine low-level logic circuitry and Darlington output power drivers for bidirectional control of d-c motors or solenoids operating with continuous load currents of up to 2A and peak start-up currents as high as 3.5A.

These monolithic integrated circuits have extensive circuit protection. Both drivers have thermal shutdown networks that disable motor drive if the package power dissipation ratings are exceeded. Internal diode transient suppression is provided on-chip. Output-current limiting is determined by the user's selection of a sensing resistor.

The Type UDN-2952B full-bridge power driver is supplied in a 16-pin dual in-line plastic package with copper heat-sink contact tabs. The lead configuration enables easy attachment of a heat sink while fitting a standard integrated circuit socket or printed wiring board layout. Type UDN-2952W, for higher power requirements, is in a 12-pin single in-line power tab package. The tab is at ground potential and needs no insulation.

FUNCTIONAL BLOCK DIAGRAM



Write for Engineering Bulletin 29319 to Technical Literature Service, Sprague Electric Company, 647 Marshall Street, North Adams, Mass. 01247

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4SS-3160

ABBREVIATIONS OF COMPANY NAMES

Action Ins	Action Instruments
AD	Analog Devices
ADT	Advanced Digital Technology
Advent	Advent Products, Inc.
Alphatron	Alphatron
AMA	American Automation
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
Amperex	Amperex Electronic Corp.
Analogic	Analogic
Analog Sys	Analog Systems
APC	Applied Micro Circuits
Apex	Apex Microtechnology
APM	Applied Microsystems Corp.
Appl Sys	Applied Systems Corp.
APT	Applied Microtechnology
Aptek	Aptek Microsystems
Array Tech	Array Technology
AWI	AWI Electronics
Barvon	Barvon Research
Bedford	Bedford Computer Systems Inc.
Burr-Brown	Burr-Brown
CAE	Computer Aided Engineering
Cal Devices	California Devices
Cermetek	Cermetek
CGRS	CGRS Microtech Inc.
Cherry	Cherry Semiconductor
CIC	Custom Integrated Circuits
CirTech	Circuit Technology
Citel	Citel
Comlinear	Comlinear Corporation
CMA	Custom MOS Arrays
Comark	Comark Corp.
Comdial	Comdial Semiconductor
Comp Auto	Computer Automation
Compas	Compas Microsystems
Cont Logic	Control Logic Inc.
Control Sys	Control Systems Microsystems Div.
CreMicro	Creative Micro Systems
Cromemco	Cromemco, Inc.
Cubit	Cubit Inc.
Curtis	Curtis Electro Devices, Inc.
Cybernetic	Cybernetic Micro Systems
Cybersys	Cybersystems
Cybertek	Cybertek Inc.
Data General	Data General
Data I/O	Data I/O
Data Trans	Data Translation
Datel	Datel
Datricon	Datricon Corporation
DDC	Data Devices Corporation
DEC	Digital Equipment Corporation
Die-Tech	Die-Tech
Digelec	Digelec Corp.
Digitek	Digitek, Inc.
Dionics	Dionics Inc.
Dist Comp	Distributed Computer Systems
Divers Tech	Diversified Technology
E-HI	E-H International, Inc.
EDI	Electronic Designs Inc.
Elind	Elind Elettronica Industriale
EMM-SESCO	EEM-SESCO
Emulogic	Emulogic Inc.
ETI Micro	ETI Micro
Exar	Exar Integrated Systems
Exel	Exel Microelectronics
Fairchild	Fairchild
Ferranti	Ferranti Electric
Force	Force Computers
Fujitsu A	Fujitsu America
Fujitsu	Fujitsu Microelectronics, Inc.

GI	General Instrument
GTE Micro	GTE Microcircuits
Harris	Harris Semiconductor
Heurikon	Heurikon Corp.
Hilevel	Hilevel Technology, Inc.
Hitachi	Hitachi America, Ltd.
Holt	Holt Inc.
HP	Hewlett-Packard
Hughes	Hughes Aircraft, Solid State Products
Hybrid Sys	Hybrid Systems
HyComp	HyComp
ICC	International Cybernetics
IDT	Integrated Device Technology
IMI	International Microcircuits, Inc.
IMP	International Microelectronic Products
IMS	Industrial MicroSystems Inc.
Infosphere	Infosphere
Inmos	Inmos
IntCirEng	Integrated Circuit Engineering
IntCirSys	Integrated Circuit Systems
IntCompSys	Integrated Computer Systems
Int Tech	Integrated Technology Corp.
Intech	Intech Microcircuits Div.
Intel	Intel
Interdesign	Interdesign
Intersil	Intersil
Intronics	Intronics
ITT	ITT Semiconductors
Kinetic Sys	Kinetic Systems
Kontron	Kontron Electronics
Lambda	Lambda Semiconductor
Linear Tech	Linear Technology
LSI Comp	LSI Computer Systems
LSI Logic	LSI Logic Corporation
Master Logic	Master Logic Corporation
Matrix	Matrix Corp.
Matrox	Matrox Electronic Systems
Maxim	Maxim Integrated Products
MCC	Micro-Computer Control
MCE	MCE Electronics
Micrel	Micrel
Micro Innov	Micro Innovators
Micropac	Micropac Industries
Micro Net	Micro Networks
Micro Pwr	Micro Power Systems
Micro Sci	Micro Sciences Corp.
Micro Tech	Microcircuits Technology
Micro-Link	Micro-Link Corporation
Micron	Micron Technology
MilerTron	MilerTronics
Miller	Miller Technology
Mitel	Mitel Semiconductor
Mitsubishi	Mitsubishi Electronics
MMI	Monolithic Memories, Inc.
Mostek	Monolithic Systems Corp.
Motorola	Mostek
MRC	Motorola Semiconductor
Murray	MRC Systems
Monosil	Murray Consulting
National	National Semiconductor
NCM	NCM Corp.
NCR	NCR Corp., Microelectronics Division
NEC	NEC Electronics
Nitron	Nitron

OAE	Oliver Advanced Engineering
Octagon	Octagon Systems Corp.
OEI	Optical Electronics Inc.
Ohio Sci	Ohio Scientic
OKI	OKI Semiconductor
Omnibyte	Omnibyte Corp.
Onset	Onset Computer Corp.
Panasonic	Panasonic
Pico Design	Pico Design
Polycore	Polycore Electronics
Plessey	Plessey Semiconductors
PMI	Precision Monilithics, Inc.
PragDes	Pragmatic Design Inc.
Pro-Log	Pro-Log Corp.
Quay	Quay Corp.
Raytheon	Raytheon Semiconductor
RCA	RCA Solid State Division
RCI Data	RCI Data
RELMS	Relational Memory Systems
Reticon	Reticon
RIFA	RIFA
Rockwell	Rockwell, Microelectronic Devices
RTC	Riehl Time Corporation
Sanyo	Sanyo
SBE	SBE, Inc.
SEEQ	SEEQ Technology, Inc.
SPI	Semi Processes Inc.
Siemens	Siemens
Si-Fab	Si-Fab
Signetics	Signetics
SGS	SGS Semiconductor
Sharp	Sharp
Silicon G	Silicon General
Siliconix	Siliconix
Silicon Sys	Silicon Systems Inc.
Siltronics	Siltronics
SMC	Standard Microsystems Corp.
S MOS	S MOS Systems
Solarise	Solarise Enterprises
Solitron	Solitron Devices
Sprague	Sprague Electric Company
SSM	Solid State Micro Technology for Music
SSS	Solid State Scientific
Stag	Stag Microsystems
STC	Storage Technology Corp.
STD	STD Microsystems
Struc Des	Structured Design Inc.
Stynetic	Stynetic Systems
Sunrise	Sunrise Electronics
Sunshine	Sunshine Semiconductor
Supertex	Supertex Inc.
Symtek	Symtek Corp.
Synertek	Synertek
Sys Innov	Systems Innovations
Tau Zero	Tau Zero Inc.
Technitrol	Technitrol
Tektronix	Tektronix
Teledyne C	Teledyne Crystalonics
Teledyne P	Teledyne Philbrick
Teledyne S	Teledyne Semiconductor
Telefunken	Telefunken
Telmos	Telmos
Teltone	Teltone Corporation
TI	Texas Instruments
Third Domain	Third Domain
Thomson-CSF	Thomson-CSF Components Corp.
Toshiba	Toshiba America
Trans-Data	Trans-Data
TRW	TRW LSI Products
Unitrode	Unitrode
Universal	Universal Semiconductor, Inc.
Varix	Varix Corp.
VLSI Design	VLSI Design Associates
VTI	VLSI Technology, Inc.
Votrax	Votrax
Weitek	Weitek Corporation
Western	Western Digital
Wintek	Wintek Corp.
Xicor	Xicor, Inc.
Xycom	Xycom
Zendex	Zendex Corp.
Zilog	Zilog
ZyMOS	ZyMOS Corporation
Zytrex	Zytrex Corp.

TELEDYNE SEMICONDUCTOR

Advance Product Information

TSC426/427/428
Dual Power MOSFET Driver
• 1.5 Amp Peak Drive Current
• 50 ns Rise Time

General Description

The TSC426/427/428 are dual high speed power MOSFET drivers. Each device converts CMOS/TTL input levels to a high voltage level drive signal. Switching times of 50 ns are typical with 1000 pf loads. Peak output drive current is 1.5 amp. Delay times have been matched for both inverting and non-inverting stages.

The TSC428 contains an inverting and non-inverting driver. The TSC426 is inverting and TSC427 non-inverting.

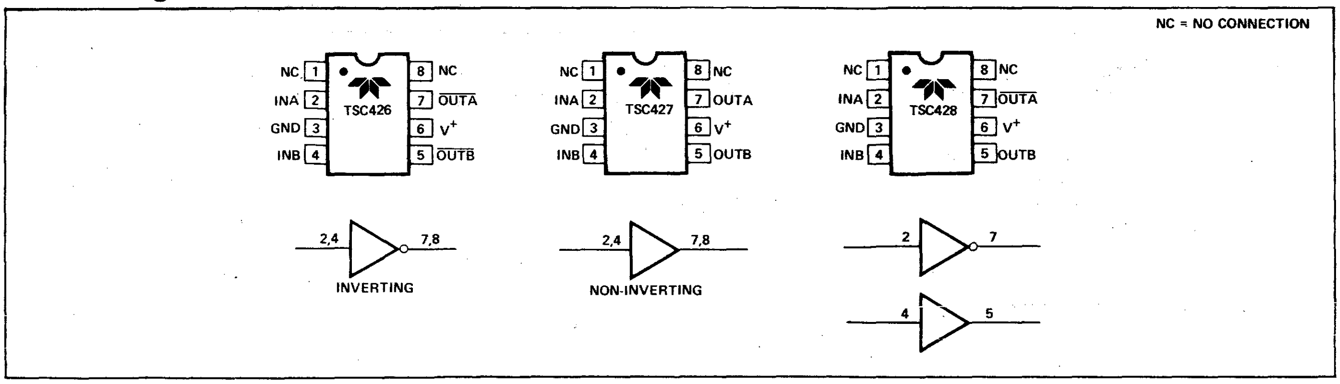
Features

- CMOS Construction for Low Current Drain ..... 6 mA
- High Output Voltage .... V_S -0.05 V
- High Peak Current Drive .... 1.5 A
- High Speed Switching (C_H = 1000 pF) .... 50 ns
- Available as Inverting/Non-Inverting Driver
- Wide Supply Voltage Operation .... 4.5 to 20 V
- TTL/CMOS Compatible Input Drive
- Pin-Out Equivalent to DS0026

Preliminary Ordering Information

Ordering Part No.	Operating Temp. Range	Package	Configuration	Peak Output Current	Rise Time (C_L = 1000 pF)
TSC426CPA	0°C to 70°C	8-Pin Plastic Dip	Inverting	1.5 A	50 ns
TSC426IJA	-25°C to 85°C	8-Pin CerDIP	Inverting	1.5 A	50 ns
TSC426MJA	-55°C to 125°C	8-Pin CerDIP	Inverting	1.5 A	50 ns
TSC427CPA	0°C to 70°C	8-Pin Plastic Dip	Non-Inverting	1.5 A	50 ns
TSC427IJA	-25°C to 85°C	8-Pin CerDIP	Non-Inverting	1.5 A	50 ns
TSC427MJA	-55°C to 125°C	8-Pin CerDIP	Non-Inverting	1.5 A	50 ns
TSC428CPA	0°C to 70°C	8-Pin Plastic Dip	Non-Inv. & Inv.	1.5 A	50 ns
TSC428IJA	-25°C to 85°C	8-Pin CerDIP	Non-Inv. & Inv.	1.5 A	50 ns
TSC428MJA	-55°C to 125°C	8-Pin CerDIP	Non-Inv. & Inv.	1.5 A	50 ns

Pin Configuration



TELEDYNE SEMICONDUCTOR

TSC700A
Four Digit LED Display Decoder and Driver
High Segment Drive Current

General Description

The TSC700A drives common anode LED displays with 28 high current, open-drain N channel output transistors. Four seven segment LED displays may be driven. Drive current is guaranteed to be 11 mA minimum. This is twice the minimum drive current available from comparable devices and will provide high LED luminance. High luminous intensity is an important factor when a dark contrasting background is unavailable or the LED is viewed at a distance. The TSC700A current capability makes it an ideal large character LED driver.

Four data bit inputs and four digit select signals permit interfacing to multiplexed BCD or binary output devices. The four bit data input is decoded into the seven segment alphanumeric code known as "Code B". A 0 to 9, —, E, H, L, P or "blank" reading may be displayed.

An added feature includes a brightness control input that adjusts segment drive current. The control pin may also be used as a digital display enable. The TSC700A is an improved pin compatible and functional equivalent to the ICM7212A and TSC7212A.

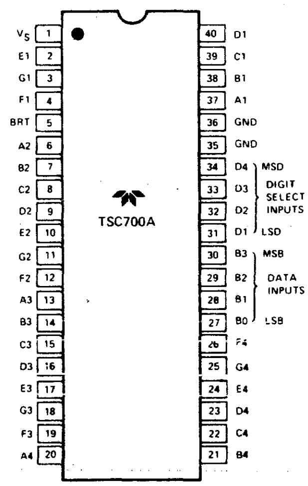
Ordering Information

Part No.	Package	Temp. Range	LED Segment Current	Output Code
TSC700AMJL	40 Pin CerDIP	-55°C to +125°C	14 mA	Code B
TSC700AIJL	40 Pin CerDIP	-25°C to +85°C	14 mA	Code B
TSC700 AMJL/883	40 Pin CerDIP	-55°C to +125°C	14 mA	Code B
TSC700A/Y	CHIP	25°C	14 mA	Code B

Features

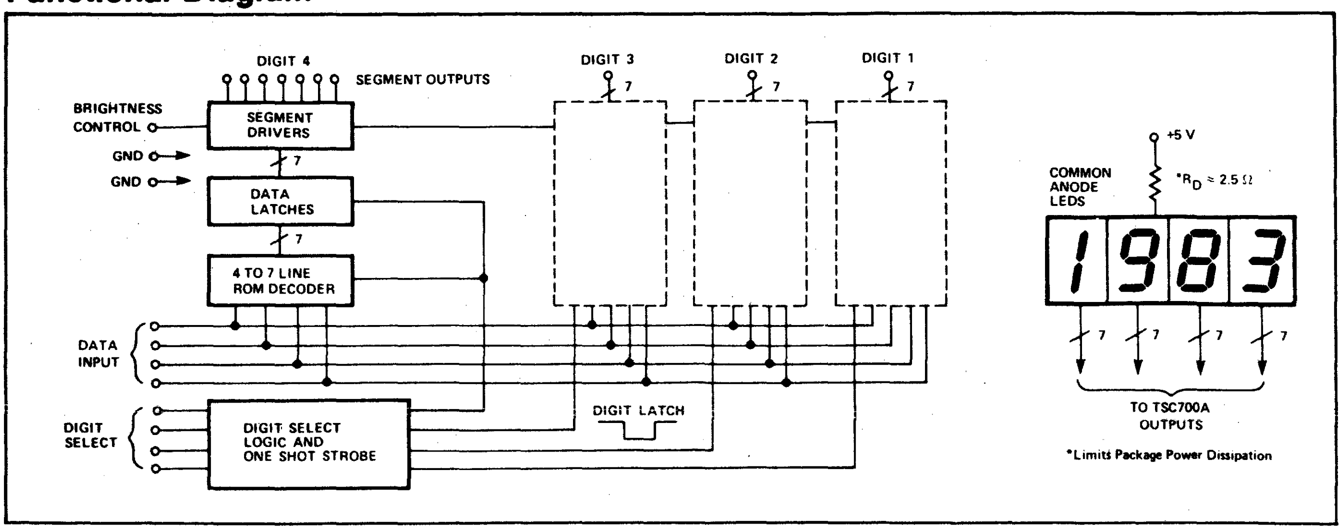
- High Drive Current for High Luminance LED Display
- Guaranteed High LED Segment Current 11 mA Minimum
- 28 Common Anode LED Drivers (4 Digits)
- Code B Output Format ... 0 to 9, —, E, H, L, P, "blank"
- BCD/Binary Input to Seven Segment LED Code
- Four Separate Digit Selects for Multiplexed Input
- Digital or Analog Brightness Control
- Digital Display Enable
- Low Thermal Resistance Package
- Military Temperature Range Devices Available
- Pin Compatible With TSC7212A, ICM7212A

Pin Configuration



If Brightness Control is not needed, connect BRT (pin 5) to Vs.

Functional Diagram



 TELEDYNE SEMICONDUCTOR

TELEDYNE SEMICONDUCTOR

TSC701AM
Bus Compatible Four Digit LED Display Driver
• High Segment Drive Current
• Input Data Latches

INTERFACE

Teledyne Semiconductor

General Description

The TSC701AM is a CMOS direct drive, four digit, seven segment LED display decoder and driver. The device is bus compatible making microprocessor controlled displays possible. Two chip select signals control data and digit select code latching prior to decoding and display. External data latches are unnecessary.

The TSC701AM drives common anode LED displays with 28 high current, open-drain N channel output transistors. Four seven segment LED displays may be driven. Drive current is guaranteed to be 11 mA minimum (18 mA TYP). This is twice the minimum drive current available from comparable devices and will provide high LED luminance. High luminous intensity is an important factor when a dark contrasting background is unavailable or the LED is viewed at a distance. The TSC701AM current capability makes it an ideal large character LED driver.

Four data bit inputs and four digit select signals permit interfacing to multiplexed BCD or binary output devices. The four bit data input is decoded into the seven segment alphanumeric code known as "Code B". A 0 to 9, —, E, H, L, P or "blank" reading may be displayed.

An added feature is the brightness control input that adjusts segment drive current. The control pin may also be used as a digital display enable. The TSC701AM is an improved pin compatible and functional equivalent to the ICM7212AM.

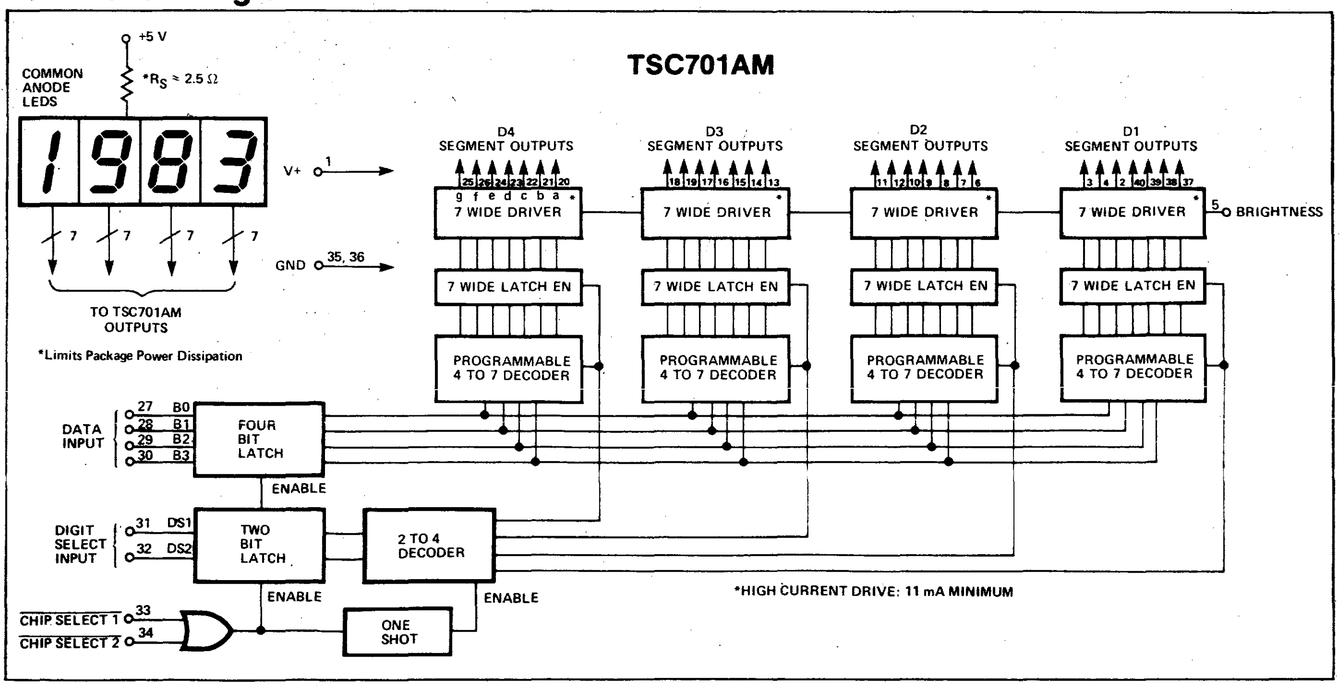
Features

- 28 Current Limited Outputs Drive Common-Anode LEDs at 18 mA Per Segment.
- Input and Digit Select Data Latches.
- Brightness Input Allows Potentiometer Control of LED Segment Current. Pin Also Serves as Digital Display Enable.
- Input and Digit Select Data Latches.
- Pin Compatible and Functionally Equivalent to ICM7212AM.
- Input Decoded to Seven Segment Code B Output (0 to 9, —, E, H, L, P, "Blank")

Ordering Information

Part No.	Package	Temp. Range	LED Segment Current	Output Code
TSC701AMIJL	40-Pin CerDIP	-25° C to +85° C	18 mA	Code B

Functional Diagram



TELEDYNE SEMICONDUCTOR

TELEDYNE SEMICONDUCTOR

TSC7109
12-Bit Plus Sign Integrating A/D Converter
• BUS Compatible
• Serial Data Transmission w/UART

General Description

The TSC7109 is a 12-bit plus sign CMOS low power A/D Converter. The single CMOS IC contains all the necessary active devices to interface with microprocessors.

In direct mode, Chip Select and High/Low Byte Enables control parallel bus interface. In the handshake mode the TSC7109 will operate with industry standard UART's in controlling serial data transmission, ideal for remote data logging. Control and monitoring of conversion timing is provided by the RUN/$\overline{\text{HOLD}}$ and STATUS outputs. The TSC7109 requires only the addition of eight passive components plus a crystal to operate as a dual slope integrating A/D converter. The TSC7109 has features that make it an attractive per-channel alternative to analog multiplexing for many data acquisition applications. These features include typical input bias current of 1 pA, drift of less than 1 μV/°C, input noise typically 15 μV p-p, and auto-zero. True differential input and reference allows the measurement of bridge-type transducers such as load cells, strain gauges and temperature transducers.

For applications requiring more resolution see the TSC800, 15-bit plus sign data sheet.

Ordering Information

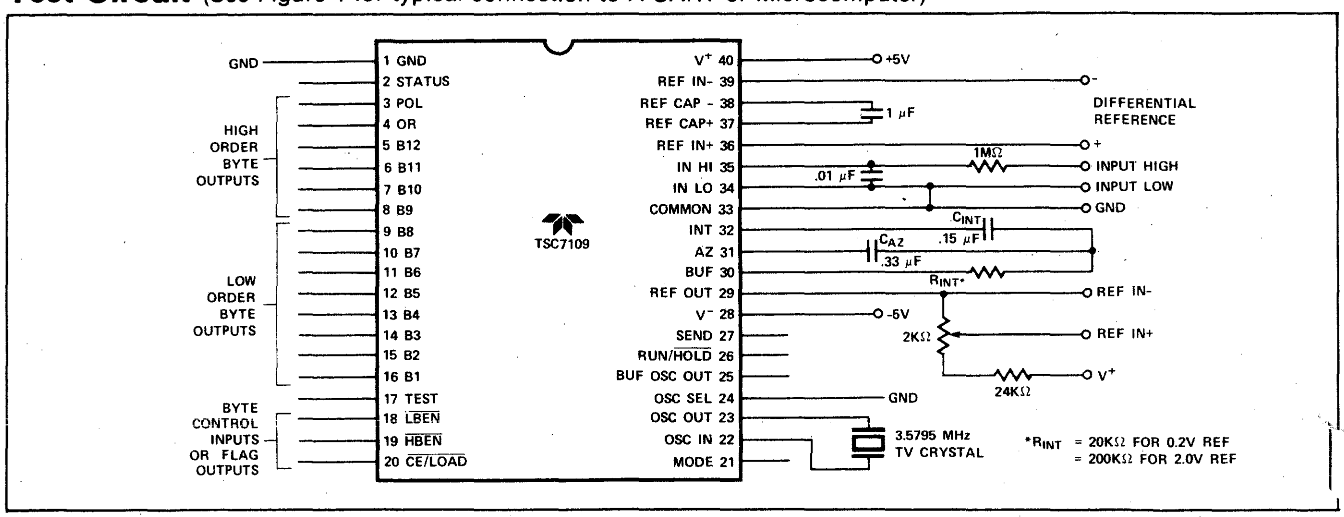
Part No.	Package	Temp. Range
TSC7109CPL	40-Pin Plastic Dip	0°C to + 70°C
TSC7109BCPL	40-Pin Plastic Dip	0°C to +70°C
TSC7109IJL	40-Pin CerDIP	-25°C to +85°C
TSC7109BIJL	40-Pin CerDIP	-25°C to +85°C
TSC7109MJL	40-Pin CerDIP	-55°C to +125°C

Features

- 12-Bit Plus Sign Integrating A/D Converter with Overrange Indication
- Sign Magnitude Coding Format
- True Differential Signal Input and Differential Reference Input
- Low Noise — Typically 15 μVp-p
- High Normal Mode Noise and Line Frequency Rejection
- 1 pA Typical Input Current
- No Zero Adjustment
- TTL Compatible Byte Organized Tri-State Outputs
- UART Handshake Mode for Simple Serial Data Transmission
- Direct Bus Connection for 8 or 16-Bit Bus — 3.58 mHz Crystal Provides 7.5 Conversions Per Second for 60 Hz Rejection — External RC Network Provides up to 30 Conversions Per Second
- Power Dissipation Typically Less Than 20 mW
- Internal Voltage Reference

Part No.	Package	Temp. Range
TSC7109CBQ	60-Pin Plastic Flat Package: Formed Leads	0°C to +70°C
TSC7109CSQ	60-Pin Plastic Flat Package: Unformed Leads	0°C to +70°C
Devices Available with 160 Hour, +125°C Burn-In		
TSC7109CPL/BI	40-Pin Plastic Dip	0°C to +70°C
TSC7109IJL/BI	40-Pin CerDIP	-25°C to +85°C
Devices with MIL-STD-883 Processing		
TSC7109MJL/883	40-Pin CerDIP	-55°C to +125°C

Test Circuit (See Figure 1 for typical connection to A UART or Microcomputer)



 TELEDYNE SEMICONDUCTOR

TELEDYNE SEMICONDUCTOR

TSC7135
4 1/2 Digit Precision Analog-to-Digital Converter

General Description

The TSC7135 4 1/2 digit analog converter offers 50 ppm (1 part in 20,000) resolution with a maximum linearity error of 1 count. An auto-zero cycle reduces the zero error to below 10 μV and zero drift to 0.5 μV/°C. Source impedance error sources are minimized by a 10 pA maximum input current. Rollover error is limited to ± 1 count.

By combining the TSC7135 with a TSC7211A (LCD), TSC7212A (LED) or TSC700A (High LED Segment Current) driver a 4 1/2 digit display DVM or DPM can be constructed. Overrange and underrange signals support automatic range switching and special display blanking/flashing applications.

Micro-processor based measurement systems are supported by the TSC7135 Busy, Strobe and Run/HOLD control signals. Remote data acquisition systems with data transfer via UARTs are also possible. The additional control pins and multiplexed BCD outputs make the TSC7135 the ideal converter for display or μ-processor based measurement systems.

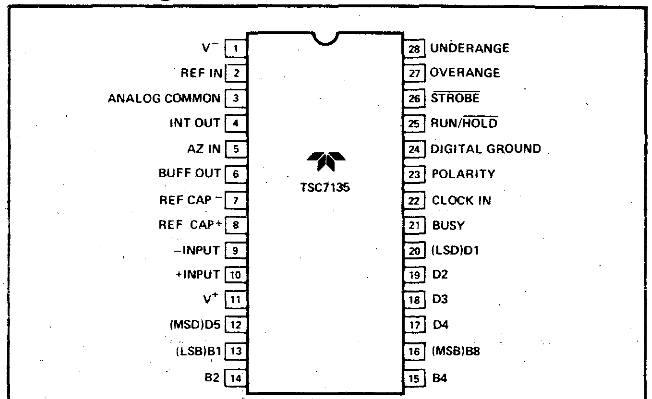
Ordering Information

Part No.	Package	Temperature Range
TSC7135CJI	28-Pin CerDIP	0°C to +70°C
TSC7135CPI	28-Pin Plastic	0°C to +70°C
TSC7135CBQ	60-Pin Plastic Flat Package w/ Formed Leads	0°C to +70°C
TSC7135CSQ	60-Pin Plastic Flat Package w/ Unformed Leads	0°C to +70°C

Features

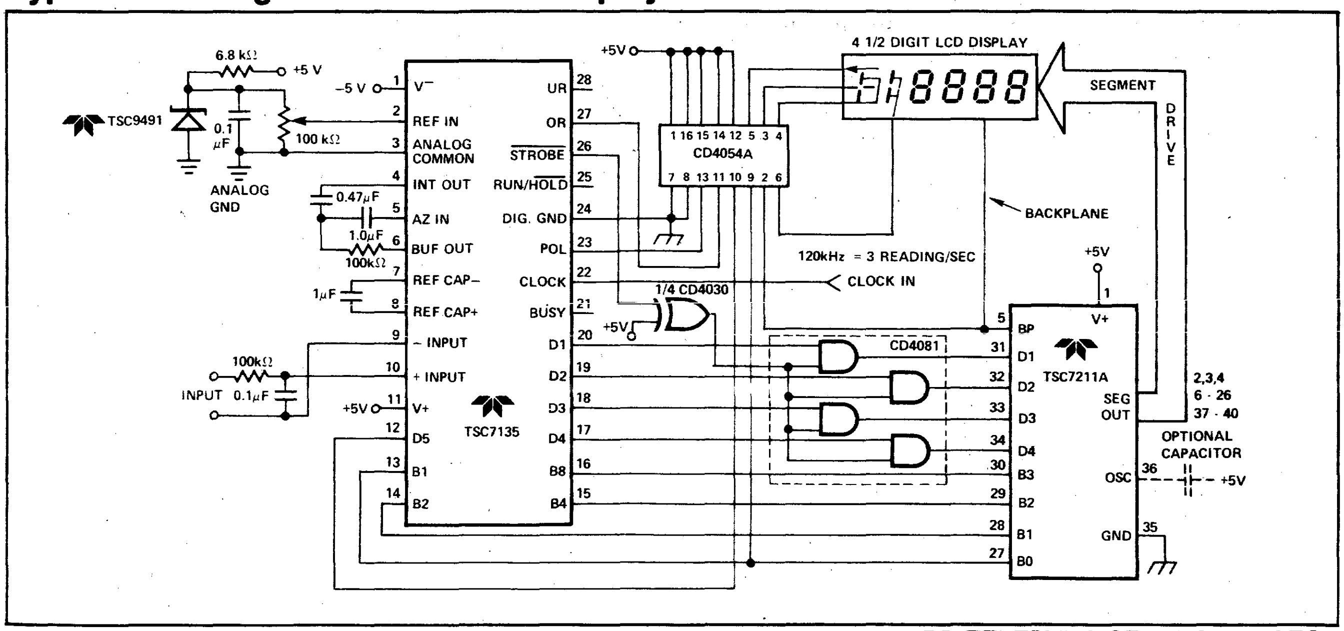
- Low Rollover Error .... ± 1 Count Maximum
- Guaranteed ± 1 Count Maximum Error
- Guaranteed Zero Reading for 0 V Input
- True Polarity Indication at Zero for Null Detection
- Multiplexed BCD Data Output
- TTL Compatible Outputs
- Differential Input
- Control Signals Permit Interface to UARTS and μ-Processors
- Auto-ranging Supported with Over and Underrange Signals
- Blinking Display Visually Indicates Overrange Condition
- Low Input Current .... 1 pA
- Low Zero Reading Drift .... 2 μV/°C
- Interface to TSC7211A, TSC7212A, and TSC700A Display Drivers
- Available in Compact Flat Package

Pin Configuration



SEE PAGE 5 FOR COMPACT FLAT PACKAGE

Typical 4 1/2 Digit DVM with LCD Display



 TELEDYNE SEMICONDUCTOR

TELEDYNE SEMICONDUCTOR

Preliminary

TSC7650
Precision Chopper-Stabilized Operational Amplifier
• 0.7 μV Offset Voltage
• 50 nV/° C Offset Voltage Drift

General Description

The TSC7650 CMOS chopper-stabilized operational amplifier practically removes offset voltage error terms from system error calculations. The 5 μV maximum V_{OS} specification, for example, represents a fifteen times improvement over the industry standard OPO7E. The 50 nV/° C offset drift specification is over twenty-five times lower than the OPO7E. The increased performance eliminates V_{OS} trim procedures, periodic potentiometer adjustment and the reliability problems caused by damaged trimmers.

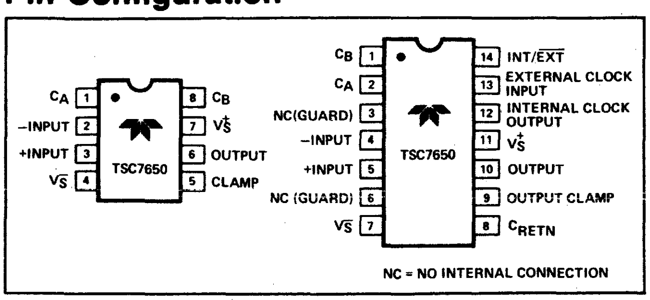
The TSC7650 performance advantages are achieved without the additional manufacturing complexity and cost incurred with laser or "zener zap" V_{OS} trim techniques. The TSC7650 is one of the lowest cost precision operational amplifiers available.

The TSC7650 nulling scheme corrects both dc V_{OS} errors and V_{OS} drift errors with temperature. A nulling amplifier alternately corrects its own V_{OS} errors and the main amplifier V_{OS} error. Offset nulling voltages are stored on two user supplied external capacitors. The capacitors connect to the internal amplifier V_{OS} null points. The main amplifier input signal is never switched. Switching spikes are not present at the TSC7650 output. The null scheme keeps V_{OS} errors low throughout the operating temperature range. Laser and "zener zap" trimming can correct for V_{OS} at only one temperature.

The nulling circuit oscillator and control circuits are integrated on chip. Only two external V_{OS} error storage capacitors are required. The TSC7650 operates as a conventional operational amplifier with vastly improved input specifications. The low V_{OS} and V_{OS} drift errors make the TSC7650 ideal for thermocouple, thermistor, and strain gauge applications. Low dc errors and high open loop gain make the TSC7650 an excellent preamplifier for precision analog to digital converters like the TSC7135 and TSC800.

The 14-pin dual in line package (DIP) has an external oscillator input to drive the nulling circuitry for optimum noise performance. Both the 8 and 14-pin DIP have an output voltage clamp circuit to minimize overload recovery time.

Pin Configuration



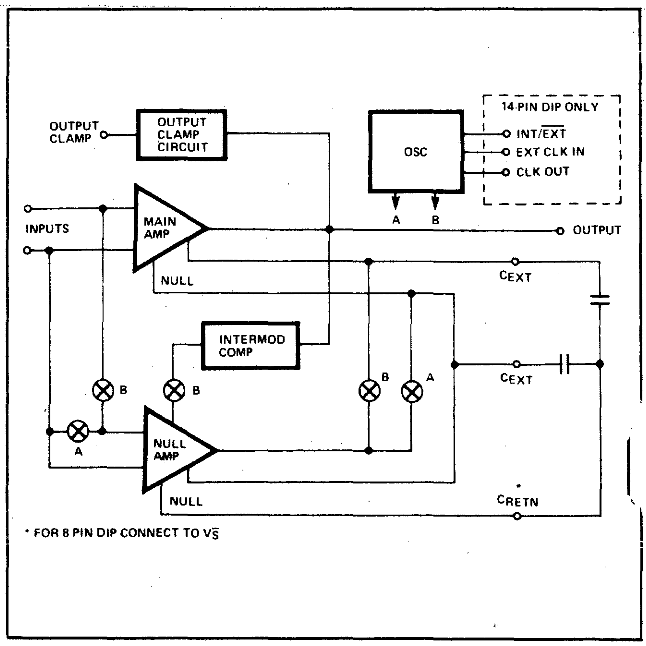
Features

- Low Input Offset Voltage .... 0.7 μV
- Low Input Offset Voltage Drift .... 0.05 μV/° C Max.
- Low Input Bias Current .... 10 pA Max.
- High Impedance Differential CMOS Inputs ..... 10^{12} Ω
- High Open Loop Voltage Gain .... 120 dB Min.
- Low Input Noise Voltage .... 2.0 μVp-p
- High Slew Rate .... 2.5 V/μs
- Low Power Operation .... 20 mW
- Output Clamp Speeds Recovery Time
- Compensated Internally for Stable Unity Gain Operation
- Direct Replacement for ICL7650
- Available in 8-Pin Dip

Ordering Information

Part No.	Package	Temp. Range	Max. Offset Voltage
TSC7650CPA	8-Pin Plastic Dip	0° C to + 70° C	5 μV
TSC7650IJA	8-Pin CerDIP	-25° C to +85° C	5 μV
TSC7650CPD	14-Pin Plastic Dip	0° C to +70° C	5 μV
TSC7650IJD	14-Pin CerDIP	-25° C to +85° C	5 μV

Functional Diagram



TELEDYNE SEMICONDUCTOR

Preliminary

TSC7660 DC to DC Voltage Converter

General Description

The TSC7660 DC to DC converter will generate a negative voltage from a positive source. With two external capacitors the TSC7660 will convert a 1.5 V to 10.0 V input signal to -1.5 V to -10.0 V level. The TSC7660 easily generates -5 V in +5 V digital systems.

Many analog to digital converters, digital to analog converters, operational amplifiers, and multiplexers require negative supply voltages. The TSC7660 allows +5 V digital logic systems to incorporate these analog components without adding an additional main power source. The TSC7660 can lower total system cost, ease engineering development and save space, power and weight.

The TSC7660 charges a capacitor to the applied supply voltage. Internal analog gates connect the capacitor across the output. Charge is transferred to an output storage capacitor completing the voltage conversion. Operation requires only two external capacitors for supply voltage <6.5 V.

Contained on-chip are a series DC power supply regulator, RC oscillator, voltage level translator, four output power MOS switches, and a unique logic element which senses the most negative voltage in the device and ensures that the output N-channel switches are not forward biased. This assures latch-up free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10 kHz for an input supply voltage of 5.0 volts. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be overdriven by an external clock.

The "LV" terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+3.5 to +10.0 volts), the LV pin is left floating to prevent device latchup.

Features

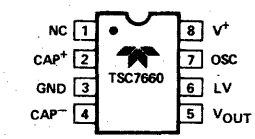
- Converts +5 V Logic Supply to ±5 V System
- Wide Input Voltage Range .... 1.5 V to 10.0 V
- Efficient Voltage Conversion 99.9%
- Excellent Power Efficiency 98%
- Low Supply Current .... 500 μA Max.
- Cascade for Output Voltage Multiplication
- Low Cost and Easy to Use
  — Only 2 External Capacitors Required

Ordering Information

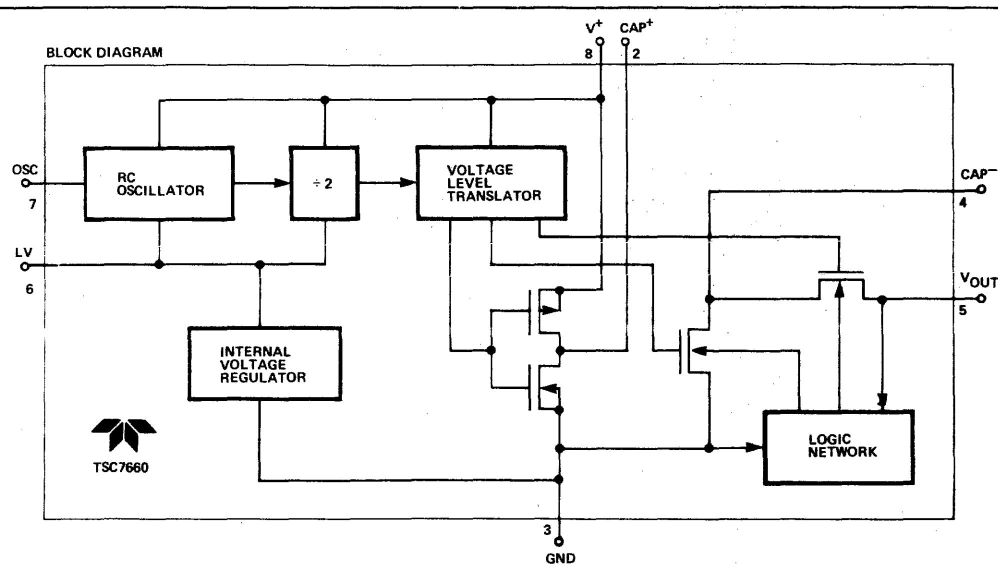
Part No.	Package	Temperature Range
TSC7660CPA	8-Pin Plastic Dip	0° C to +70° C
TSC7660IJA	8-Pin CerDIP	-40° C to +85° C
TSC7660MJA	8-Pin CerDIP	-55° C to +125° C
TSC7660/Y	Chip	25° C
Devices with MIL-STD-883 Processing		
TSC7660MJA/883	8-Pin CerDIP	-55° C to +125° C

The TSC7660 open circuit output voltage is equal to the input voltage to within 0.1%. The TSC7660 has a 98% power conversion efficiency for a 2 -5 mA load currents.

Pin Configuration



Block Diagram



TELEDYNE SEMICONDUCTOR

TSC800
15-Bit Plus Sign Integrating Analog to Digital Converter
• BUS Compatible
• UART Interface

General Description

The TSC800 is a 15-bit plus sign integrating analog to digital converter. The TSC800 improves the conventional two cycle dual slope conversion cycle by incorporating system zero and integrator output zero phases. Offset error sources are automatically zeroed and overrange recovery time is reduced. The integrating conversion technique is immune to the noise spikes that introduce conversion errors in successive approximation converters.

The externally adjustable clock allows integration periods which are integral multiples of 50 Hz or 60 Hz for maximum power-line noise rejection. By using the 2.4576 MHz crystal oscillator mode (2.5 CONV/SEC) 50, 60 and 400 Hz signals are rejected.

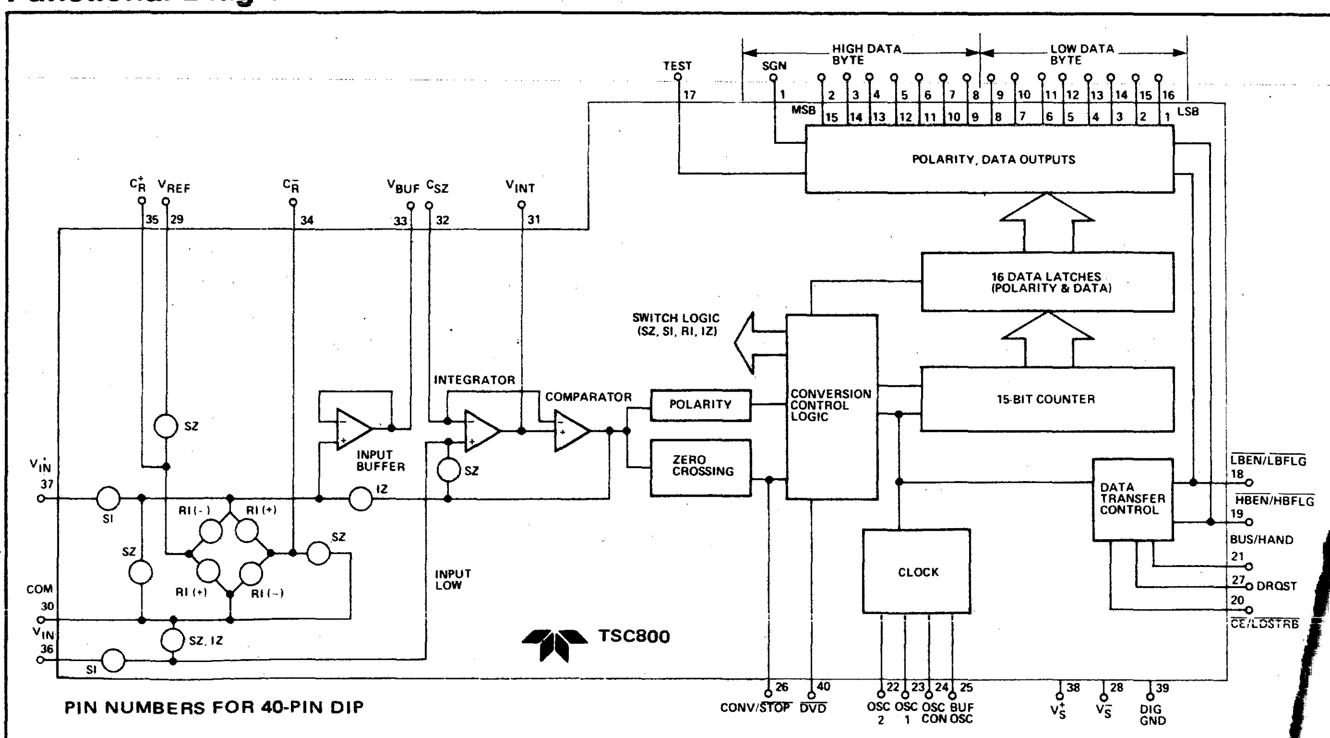
Micro-processor interface signals support single byte (16-bit) or two byte (8-bit) parallel data transfers. A "handshake" operating mode supports serial data transmission via a UART. A serial count output is derivable by gating the clock signal with data valid (DVD). The count output pulses may be used in serial fiber optic transmission systems.

The high impedance differential inputs, 5 pA input leakage current, 16-bit dynamic range and interface control signals make the high resolution TSC800 the ideal analog to digital converter for process control, data logging and "intelligent" measurement systems.

Features

- 15 Bit Resolution Plus Sign Bit
  - 96 dB Dynamic Range
- Integrating Dual Slope Converter
  - Monotonic
  - Eliminate 50/60 Hz "Line" Interference
  - High Noise Immunity
  - Auto Zero Cycle Eliminates Trimming
  - Incorporates Integrator Zero Cycle for Fast Overload Recovery
- Three State Data Bit/Sign Outputs
  - 8 or 16 Bit Parallel Data Transfer to μ-Processor Bus
- UART Control Signals
  - Serial Data Transmission
  - "Handshake" Data Transfer
  - Distributed Control Systems
  - Fiber Optic Transmission Systems
- Easy Conversion Cycle Monitoring and Control
  - Data Valid Output Signal
  - Continuous or Convert on Command Operation
- High Impedance Differential Input
  - 15 pA Maximum Input Current
- Low Input Noise
  - 15 μ V_{p-p}
- On Chip Crystal Oscillator for 2.5 Conversions/Sec.
  - f_{xtal} = 2.4576 MHz
  - 100 mSEC Integration Period Rejects 50, 60, 400 Hz Interference Signals
- Convenient ±5 V Supply Operation
  - Low Power Dissipation .... 20 mW
- Static Discharge Protected Inputs
- Available in 60-Pin Flat Package

Functional Diagram



PIN NUMBERS FOR 40-PIN DIP

TELEDYNE SEMICONDUCTOR

TSC805
Auto-Ranging Instrumentation Analog-to-Digital Converter
• 3 1/2 Digit Resolution
• Tri-Plex LCD Drive
• AC & DC Measurements

Advance Product Information

General Description

The TSC805 is a 3 1/2 digit integrating analog-to-digital converter with tri-plex LCD display drive and automatic ranging. The CMOS TSC805 contains all the logic and analog switches needed to manufacture an auto-ranging instrument for ohms and voltage measurements.

The auto-ranging feature automatically selects the proper display decimal point location. Auto-ranging is available during ohms (high and low voltage) and voltage (AC & DC) measurements. Auto-ranging eliminates expensive range switches in hand-held DMM designs and makes compact meters easier and less costly to design. Auto-ranging instruments are easy to operate and are ideal for non-technical end users. The auto-range feature may be bypassed allowing decimal point selection and input attenuator selection control through a single line input.

The TSC805 includes an AC to DC converter for AC audio frequency range measurements. Only inexpensive external diodes/resistors/capacitors are required.

A complete LCD annunciator set visually describes the TSC805 meter function and measurement range during ohms, voltage and current operation. AC or DC measurements are indicated. A low battery detection circuit also sets a low battery warning display annunciator.

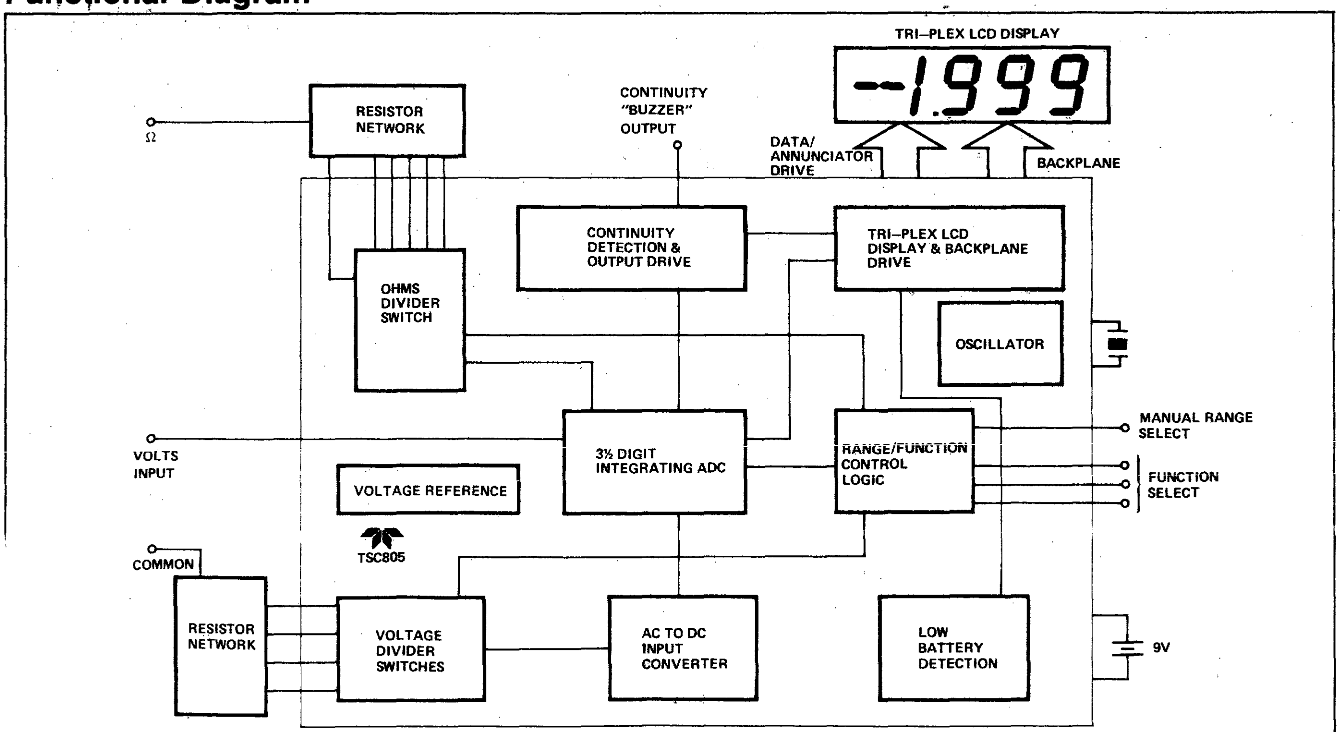
Features

- Auto-Ranging on volts (AC & DC) and Ohms Scale
- Automatic Sign, Function and Unit Display
- AC to DC Voltage Converter on Chip
- Low Voltage Ohms Range Option
- Continuity Detection & "Buzzer" Drive Output
- 3 1/2 Digit Resolution on 200 mV Full-Scale Range
- Low Noise Input Stage .... 15 μVp-p
- Precision Internal Reference .... 50 ppm/°C Max.
- Triplex LCD Drivers On Chip
- Low Battery Detection & LCD Annunciator
- Convenient 9 V Battery Operation
- Low Power Consumption .... 10 mW
- Compact 60-Pin Flat Package

The "low ohms" measurement option allows in circuit resistance measurements by preventing semiconductor junctions from being forward biased. A zero ohms adjust is included to compensate for lead resistance.

A continuity buzzer output is activated with inputs less than 5% of full-scale. An overrange input also enables the buzzer and flashes the MSD display. Offering single 9 V battery operation, 10 mW power consumption, a precision internal voltage reference (50 ppm/°C max. TC) and available in a compact 60-pin flat package the TSC805 is ideal for portable instruments.

Functional Diagram



INTERFACE

Teledyne Semiconductor

TELEDYNE SEMICONDUCTOR

TSC826
LCD Bar Graph Display Analog-to-Digital Converter
• 2.5% Resolution
• 1 mW Power Dissipation
• Direct LCD Drive

Advance Product Information

General Description

The TSC826 is a CMOS analog-to-digital converter that directly drives liquid crystal bar graph displays. LCD drivers are on-chip for forty data segment, zero, polarity, and overrange annunciators. A backplane oscillator and driver are included. All active components are on-chip for a 2.5% resolution bar graph display. Up to 16 conversions per second are possible.

An auto-zero cycle guarantees a zero display for zero volt input. No adjustment potentiometers are needed. The precision internal reference with a 35 ppm/°C temperature coefficient virtually eliminates full scale errors over temperature.

The CMOS TSC826 draws less than 100 μA from a 9 V battery guaranteeing long life in portable applications. Available in a 60-pin flat package compact portable designs with multiple bar graph indicators are possible.

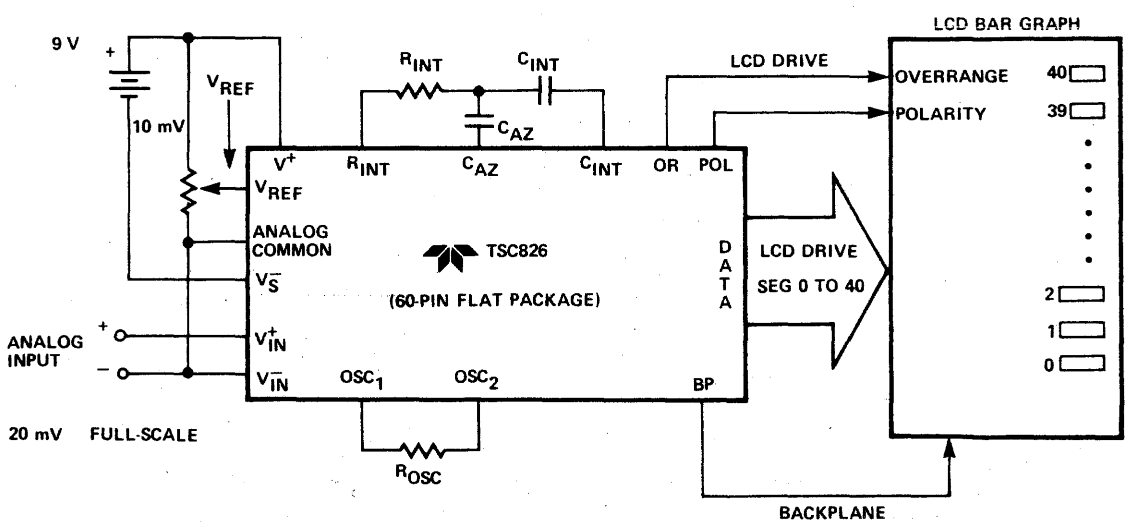
Features

- Bar Graph Data Display . . . 40 Segments plus zero
- Overrange Plus Polarity Indication
- Precision On-Chip Reference . . . 35 ppm/°C
- Auto-Zero Cycle Eliminates Zero Adjust Potentiometer
- Low Power Consumption . . . 1 mW
- Differential Analog Input
- LCD Drivers and Backplane Oscillator
- 9 V Battery Operation
- 20 mV Full-Scale Operation
- Compact Flat Package

Preliminary Ordering Information

Part No.	Package	Temperature Range
TSC826IBQ	60-Pin Plastic Flat Package (Formed Leads)	-40°C to +85°C

Typical Application



TELEDYNE SEMICONDUC

TELEDYNE SEMICONDUCTOR

TSC9403
TSC9404
Serial Input/16-Bit Parallel Output Peripheral Driver
• High Voltage, High Current Outputs

General Description

The Teledyne Semiconductor TSC9403 and TSC9404 are serial input, 16-bit parallel output shift registers. High output power MOS switching transistors make the TSC9403 and TSC9404 ideal interface circuits between microprocessor I/O ports and high current/voltage peripherals. The CMOS construction limits quiescent power dissipation to 20 mW.

The TSC9403 common source, open drain MOS outputs sustain 20 V in the OFF state and maintain leakage currents under 100 μA. The TSC9404 outputs are rated at 15 V. The 16 parallel outputs will continuously sink 60 mA. ($V_{SAT} \leq 0.5$ V).

Successive connection of serial data outputs to serial data inputs make longer length serial to parallel conversions possible. Device cascading makes the TSC9403 and TSC9404 ideal thermal printhead or high resolution LED bar graph drivers.

Ordering Information

Part	Package	Temperature Range	Output Voltage
TSC9403CJ	24-Pin Epoxy Dip	0°C to 70°C	20 V
TSC9403IL	24-Pin CerDIP	-25°C to 85°C	20 V
TSC9404CJ	24-Pin Epoxy Dip	0°C to 70°C	15 V
TSC9404IL	24-Pin CerDIP	-25°C to 85°C	15 V
TSC9404ML	24-Pin CerDIP	-55°C to 125°C	15 V
Devices Available with MIL-STD-883 Processing			
TSC9404ML/883	24-Pin CerDIP	-55°C to 125°C	15 V

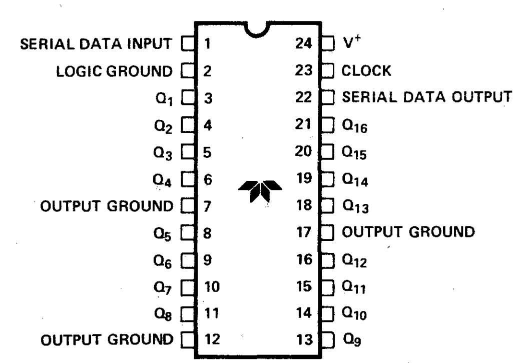
Features

- High Voltage Outputs: 20 V (TSC9403), 15 V (TSC9404)
- High Output Current Sink Capability: 60 mA
- Low Standby Power: 20 mW
- High Speed Operation: 3.0 MHz
- 16 Parallel Outputs
- Cascading Possible for Longer Data Words

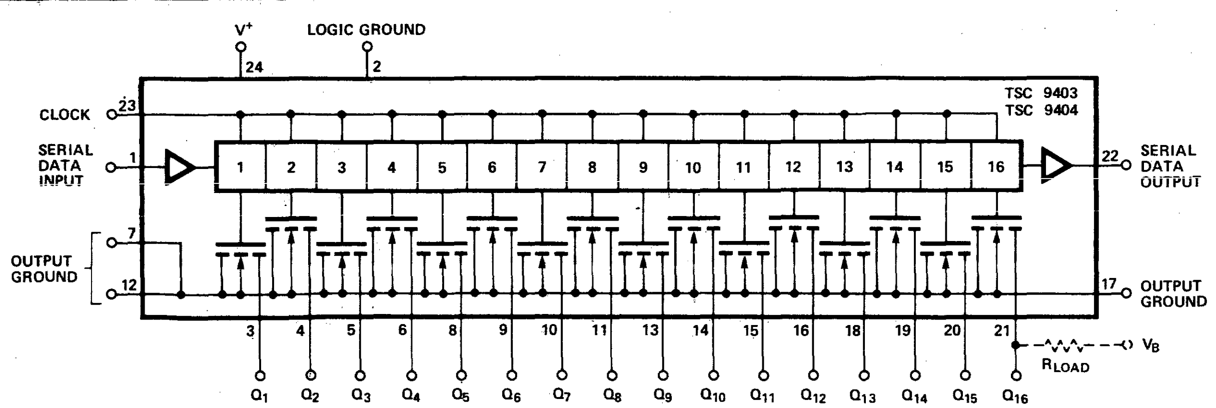
Applications

- Incandescent Lamp Driver
- Thermal Printhead Driver
- LED Bar Graph Driver
- High Current, Microprocessor Serial Port Expander
- Relay/Solenoid Driver
- Tungsten Lamp Driver
- SCR Gate Driver

Pin Configuration



Simplified Schematic



NOTE: LOGIC 1 SERIAL DATA INPUT BIT TURNS OUTPUT NMOS ON.

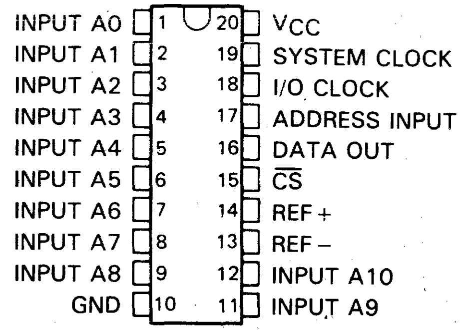
TYPES TLC540M, TLC540I, TLC541M, TLC541I 8-BIT ANALOG-TO-DIGITAL PERIPHERALS WITH SERIAL CONTROL AND 11 INPUTS

D2799, OCTOBER 1983

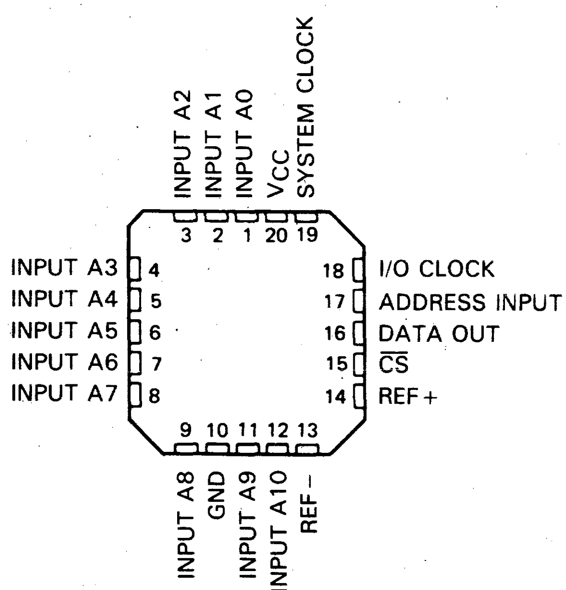
- LinCMOS™ Technology
- 8-Bit Resolution A/D Converter
- On-Chip 12-Channel Analog Multiplexer
- Built-In Self-Test Mode
- Software-Controllable Sample and Hold
- Total Unadjusted Error . . . ±0.5 LSB Max
- Direct Replacement for Motorola MC145040

TYPICAL PERFORMANCE:	TL540	TL541
Channel Acquisition Time	2 μs	7 μs
Conversion Time	10 μs	19 μs
Sampling Rate	71×10^3	29×10^3
Power Dissipation	6 mW	6 mW

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



FK OR FN PACKAGE
(TOP VIEW)



description

The TLC540 and TLC541 are LinCMOS™ A/D peripherals built around an 8-bit switched-capacitor successive-approximation A/D converter. They are designed for serial interface to a microprocessor or peripheral via a three-state output with up to four control inputs [including independent System Clock, I/O Clock, Chip Select ($\overline{CS}$), and Address Input]. A 4-megahertz system clock for the TLC540 and a 2.1-megahertz system clock for the TLC541 with a design that includes simultaneous read/write operation allow high-speed data transfers and sample rates of up to 71,910 samples per second for the TLC540 and 29,144 samples per second for the TLC541. In addition to the high-speed converter and versatile control logic, there is an on-chip 12-channel analog multiplexer that can be used to sample any one of 11 inputs or an internal "self-test" voltage, and a sample-and-hold that can operate automatically or under processor control.

The converters incorporated in the TLC540 and TLC541 feature differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and analog circuitry isolation from logic and supply noises. A totally switched-capacitor design allows guaranteed low-error (±0.5 LSB) conversion in 10 microseconds for the TLC540 and 19 microseconds for the TLC541 over the full operating temperature range.

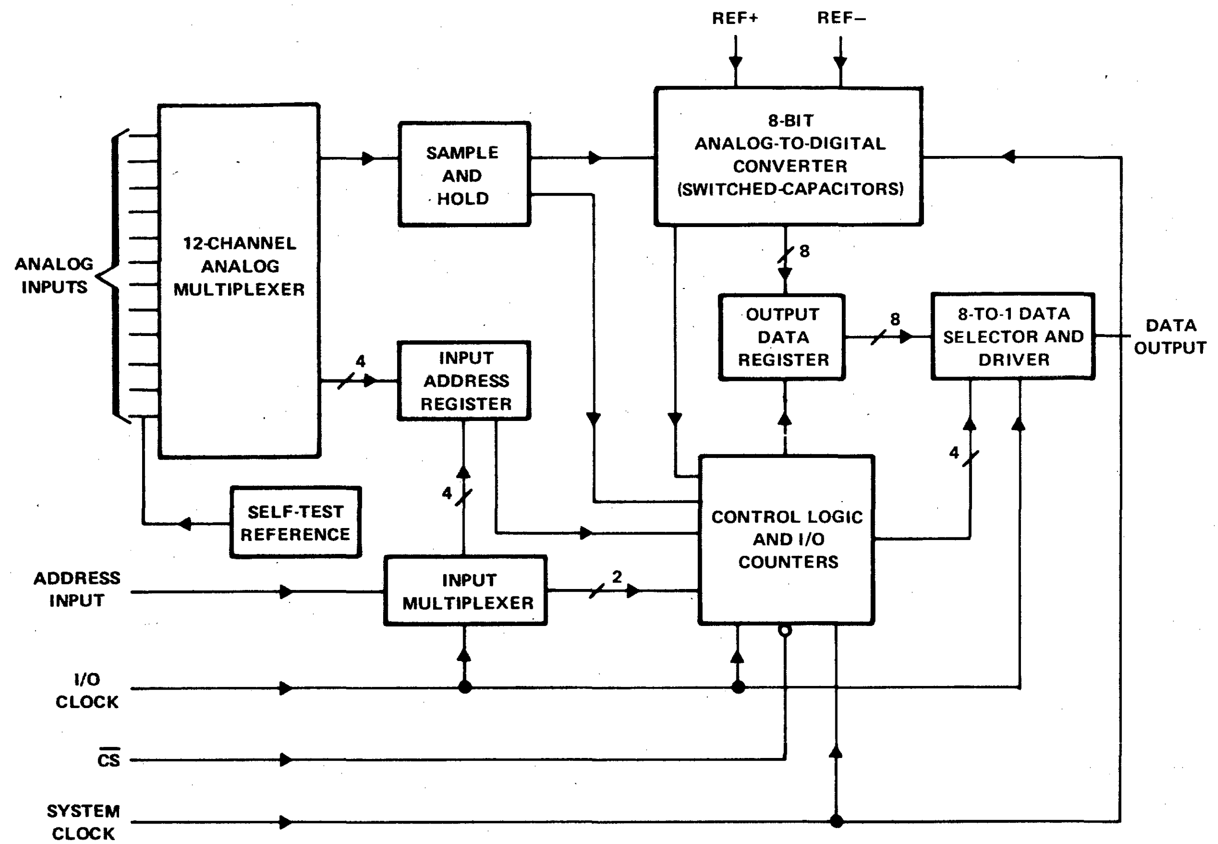
The TLC540M and the TLC541M are characterized for operation over the full military temperature range of −55 °C to 125 °C. The TLC540I and the TLC541I are characterized for operation from −40 °C to 85 °C.

ADVANCE INFORMATION

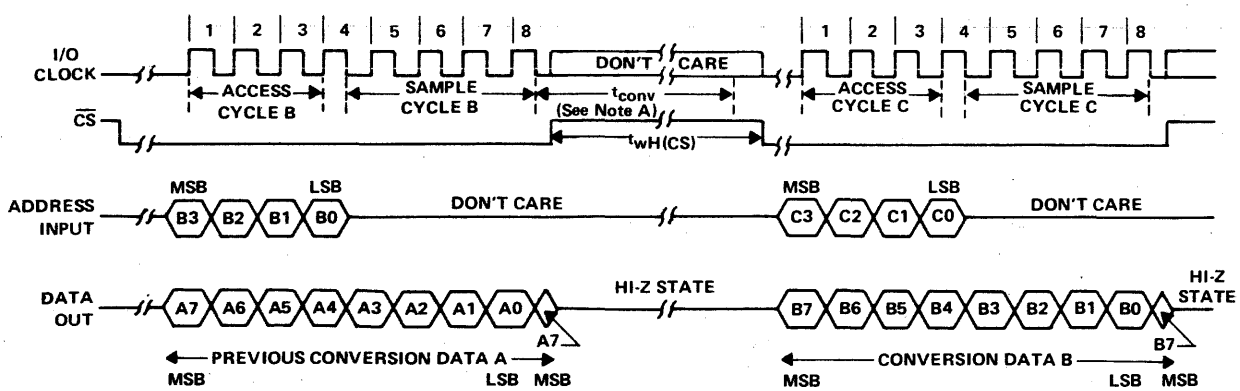
This document contains information on a new product. Specifications are subject to change without notice.

TYPES TLC540M, TLC540I, TLC541M, TLC541I 8-BIT ANALOG-TO-DIGITAL PERIPHERALS WITH SERIAL CONTROL AND 11 INPUTS

functional block diagram



operating sequence



NOTE A: The conversion cycle, which requires 40 system clock periods, is initiated with the 8th I/O clock↓after CS ↓ for the channel whose address exists in memory at that time.

absolute maximum ratings over operating free-air temperaure range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range (any input) . . . . . −0.3 V to V_{CC} + 0.3 V
Output voltage range . . . . . −0.3 V to V_{CC} + 0.3 V
Peak input current range (any input) . . . . . ±10 mA
Peak total input current (all inputs) . . . . . ±30 mA
Continuous total dissipation at 25°C (see Note 2) . . . . . 875 mW
Operating free-air temperature range: TLC540I, TLC541I . . . . . −40°C to 85°C
TLC540M, TLC541M . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: FK, FN, or N package . . . . 260°C

NOTES: 1. All voltage values are with respect to digital ground with REF− and GND wired together (unless otherwise noted).
2. For operation above 25°C free-air temperature, see Dissipation Derating Curves, Section 2. In the J package, TLC540M and TLC541M chips are alloy mounted, TLC540I and TLC541I chips are glass mounted.

recommended operating conditions

			TLC540			TLC541			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.75	5	5.5	4.75	5	5.5	V
Positive reference voltage, V_{REF+} (see Note 3)			1.25	V_{CC}	$V_{CC}+0.1$	1.25	V_{CC}	$V_{CC}+0.1$	V
Negative reference voltage, V_{REF-} (see Note 3)			−0.1	0	$V_{CC}-1.25$	0.1	0	$V_{CC}-1.25$	V
Differential reference voltage, $V_{REF+} - V_{REF-}$ (see Note 3)			1	V_{CC}	$V_{CC}+0.2$	1	V_{CC}	$V_{CC}+0.2$	V
Analog input voltage (see Note 3)			0		V_{CC}	0		V_{CC}	V
High-level control input voltage, V_{IH}			2			2			V
Low-level control input voltage, V_{IL}					0.8			0.8	V
Setup time, address bits at data input before I/O CLK↑, $t_{su(A)}$			200			400			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 4)			2			2			System clock cycles
Input/Output clock frequency, $f_{CLK(I/O)}$			0.005		2.048	0		0.525	MHz
System clock frequency, $f_{CLK(SYS)}$			$f_{CLK(I/O)}$			$f_{CLK(I/O)}$			MHz
System clock high, $t_{wH(SYS)}$			110			210			ns
System clock low, $t_{wL(SYS)}$			100			190			ns
Input/Output clock high, $t_{wH(I/O)}$			200			808			ns
Input/Output clock low, $t_{wL(I/O)}$			200			808			ns
Clock transition time (see Note 5)	System	$f_{CLK(SYS)} \le 1048$ kHz			30			30	ns
		$f_{CLK(SYS)} > 1048$ kHz			20			20	
	I/O	$f_{CLK(I/O)} \le 525$ kHz			100			100	ns
		$f_{CLK(I/O)} > 525$ kHz			40			40	
Operating free-air temperature, T_A		TLC540M, TLC541M	−55		125	−55		125	°C
		TLC540I, TLC541I	−40		85	−40		85	

NOTES: 3. Analog input voltages greater than that applied to REF+ convert as all "1"s (11111111), while input voltages less than that applied to REF− convert as all "0"s (00000000). For proper operation, REF+ voltage must be at least 1 volt higher than REF− voltage. Also, adjusted errors may increase as this differential reference voltage falls below 4.75 volts.
4. To minimize errors caused by noise at the Chip Select input, the internal circuitry waits for two system clock cycles (or less) after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the chip select setup time has elapsed.
5. This is the time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min.

TYPES TLC540M, TLC540I, TLC541M, TLC541I 8-BIT ANALOG-TO-DIGITAL PERIPHERALS WITH SERIAL CONTROL AND 11 INPUTS

electrical characteristics over recommended operating temperature range, $V_{CC} = V_{REF+} = 4.75$ V to 5.5 V (unless otherwise noted), $f_{CLK(I/O)} = 2.028$ MHz for TLC540 or $f_{CLK(I/O)} = 0.525$ MHz for TLC541

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (pin 16)		$V_{CC} = 4.75$ V,	$I_{OH} = 360$ μA	2.4			V
V_{OL}	Low-level output voltage		$V_{CC} = 4.75$ V,	$I_O = 3.2$ mA			0.4	V
I_{OZ}	Off-state (high-impedance state) output current		$V_O = V_{CC}$,	$\overline{CS}$ at V_{CC}			10	μA
			$V_O = 0$,	$\overline{CS}$ at V_{CC}			−10	
I_{IH}	High-level input current		$V_I = V_{CC} + 0.3$ V			0.005	2.5	μA
I_{IL}	Low-level input current		$V_I = 0$			−0.005	−2.5	μA
I_{CC}	Operating supply current		$\overline{CS}$ at 0 V			1.2	2	mA
	Selected channel leakage current		Selected channel at V_{CC}, Unselected channel at 0 V			0.4	1	μA
			Selected channel at 0 V, Unselected channel at V_{CC}			−0.4	−1	
$I_{CC} + I_{REF}$	Supply and reference current		$V_{REF+} = V_{CC}$, $\overline{CS}$ at 0 V			1.3	3	mA
C_i	Input capacitance	Analog inputs				7	55	pF
		Control inputs				5	15	

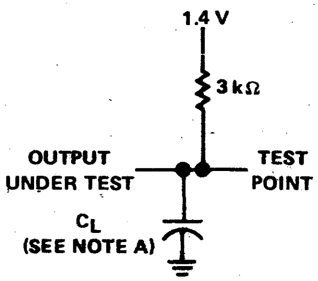
†All typical values are at $T_A = 25°C$.

operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{REF+} = 4.75$ V to 5.5 V, $f_{CLK(I/O)} = 2.048$ MHz for TLC540 or 0.525 MHz for TLC541, $f_{CLK(SYS)} = 4$ MHz for TLC540 or 2.097 MHz for TLC541.

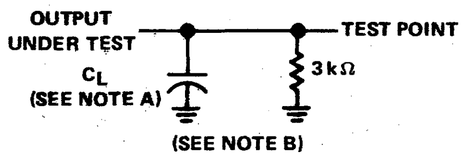
PARAMETER		TEST CONDITIONS	TLC540			TLC541			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
	Linearity error	See Note 6			±0.5			±0.5	LSB
	Zero error	See Note 7			±0.5			±0.5	LSB
	Full-scale error	See Note 7			±0.5			±0.5	LSB
	Total unadjusted error	See Note 8			±0.5			±0.5	LSB
	Self-test output code	input address = 1011 (A11) (See Note 9)	01111101 (125)		10000011 (131)	01111101 (125)		10000011 (131)	
t_{conv}	Conversion time				10			19	μs
t_{acq}	Channel acquisition time				4			4	I/O clock cycles
t_v	Time output data remains valid after I/O clock↓	See Parameter Measurement Information	10			10			ns
t_d	Delay time, I/O clock↓ to data output valid				200			400	ns
t_{acc}	Output access time (delay to valid output after chip select↓)		1		3	1		3	System clock cycles
t_{en}	Output enable time				150			150	ns
t_{dis}	Output disable time				150			150	ns
$t_{r(bus)}$	Data bus rise time				300			300	ns
$t_{f(bus)}$	Data bus fall time				300			300	ns

NOTES: 6. Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
7. Zero Error is the difference between the output of an ideal and an actual A/D for zero input voltage; full-scale error is that same difference for full-scale input voltage.
8. Total Unadjusted Error is the sum of linearity, zero, and full-scale errors.
9. Both the input address and the output codes are expressed in positive logic.

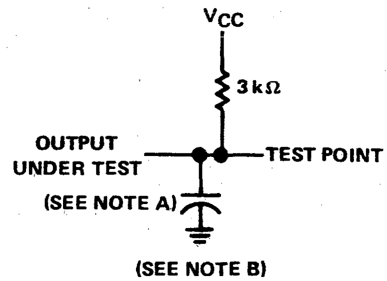
PARAMETER MEASUREMENT INFORMATION



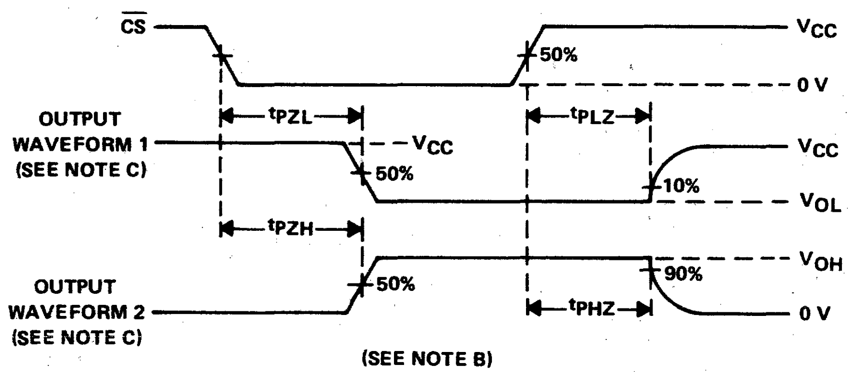
LOAD CIRCUIT FOR t_d, t_{acc}, t_r, t_f



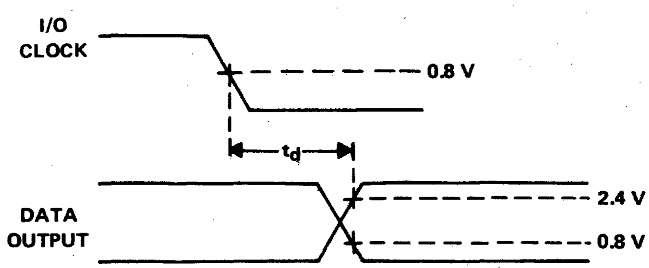
LOAD CIRCUIT FOR t_{PZH} AND t_{PHZ}



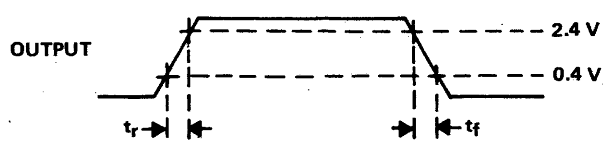
LOAD CIRCUIT FOR t_{PZL} AND t_{PLZ}



VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORM FOR DELAY TIME



VOLTAGE WAVEFORM FOR RISE AND FALL TIMES

NOTES: A. C_L = 50 pF for TLC540 and 100 pF for TLC541
B. $t_{en} = t_{PZH}$ or t_{PZL}, $t_{dis} = t_{PHZ}$ or t_{PLZ}
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

TYPES TLC540M, TLC540I, TLC541M, TLC541I 8-BIT ANALOG-TO-DIGITAL PERIPHERALS WITH SERIAL CONTROL AND 11 INPUTS

principles of operation

The TLC540 and TLC541 are each complete data acquisition systems on a single chip. They include such functions as analog multiplexer, sample-and-hold, 8-bit A/D converter, data and control registers, and control logic. For flexibility and access speed, there are four control inputs [two clocks, chip select ($\overline{CS}$), and address]. These control inputs and a TTL-compatible 3-state output are intended for serial communications with a microprocessor or microcomputer. With judicious interface timing, with TLC540 a conversion can be completed in 10 microseconds, while complete input-conversion-output cycles are being repeated every 14 microseconds. With TLC541 a conversion can be completed in 19 microseconds, while complete input-conversion-output cycles are repeated every 35 microseconds. Furthermore, this fast conversion can be executed on any of 11 inputs or its built-in "self-test," and in any order desired by the controlling processor.

Though they can be operated "tied" together, the System Clock and I/O Clock are normally used independently, with no special phase or speed relationship to be considered. This allows integrated circuit operation to continue independent of serial Input/Output timing, permitting manipulation of the I/O Clock as desired for a wide range of software and hardware needs.

The I/O Clock, Data Input, and Data Output are controlled by $\overline{CS}$. It floats the 3-state output and shuts off signals to other control inputs while it is high. This allows any pins except pin 15 to share lines with other integrated circuits. A normal control sequence is as follows: (1) $\overline{CS}$ goes low; (2) a new positive-logic multiplexer address is clocked in through the address input on the first four I/O Clock rising edges while previous conversion results are brought out on the first seven I/O Clock falling edges. Input and output most-significant bits (MSB) are first, with the output MSB available at the start of the cycle; (3) the on-chip sample-and-hold begins sampling a newly addressed input after the 4th falling edge, and goes into the hold mode on the 8th falling I/O Clock edge just before conversion; (4) $\overline{CS}$ must then go high or the I/O Clock must remain low for at least 40 system clock cycles to allow conversion. A new address may then be loaded or the previous conversion results read any time $\overline{CS}$ is brought low, but it should be noted that any pending conversion may stop.

The instant that the TLC540 or TLC541 holds a sample of the analog input, conversion can be determined under software control (or by external logic), by keeping the 8th I/O Clock cycle high. Any output data will have already been shifted out, and TLC540 or TLC541 will continue sampling a new analog input. At the desired time, the I/O Clock signal can then be lowered freezing the voltage and turning off all analog inputs. In this manner, signals can be sampled at precise intervals for a wide range of comparison or processing applications, in much the same manner as a strobe light is used to determine engine speed.

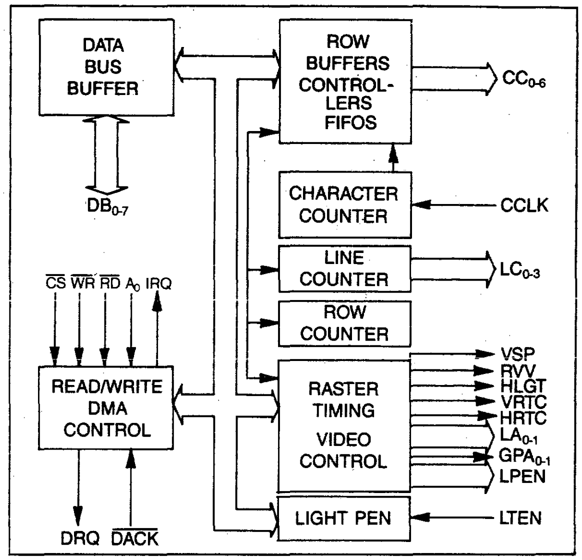
WESTERN DIGITAL
C O R P O R A T I O N

NEW PRODUCT BULLETIN

Programmable CRT Controller WD8275

FEATURES

- PROGRAMMABLE CHARACTER/SCREEN FORMAT
  - 1-16 LINES PER ROW
  - 1-64 ROWS PER FRAME
  - 1-80 CHARACTERS PER ROW
- SIX FIELD ATTRIBUTES
  - BLINK
  - HIGHLIGHT
  - REVERSE VIDEO
  - UNDERLINE
  - 2-USER PROGRAMMABLE
- ELEVEN CHARACTER ATTRIBUTES
  - RIGHT ANGLE LINE GRAPHIC SYMBOLS
- FOUR CURSOR CONTROLS
  - BLINK/NONBLINK UNDERLINE
  - BLINK/NONBLINK REVERSE VIDEO BLOCK
- LIGHT PEN DETECTION
- REQUIRES +5 VOLT ONLY
- 40 PIN CERDIP AND PLASTIC PACKAGES
- COMPATIBLE WITH INTEL D8275/P8275



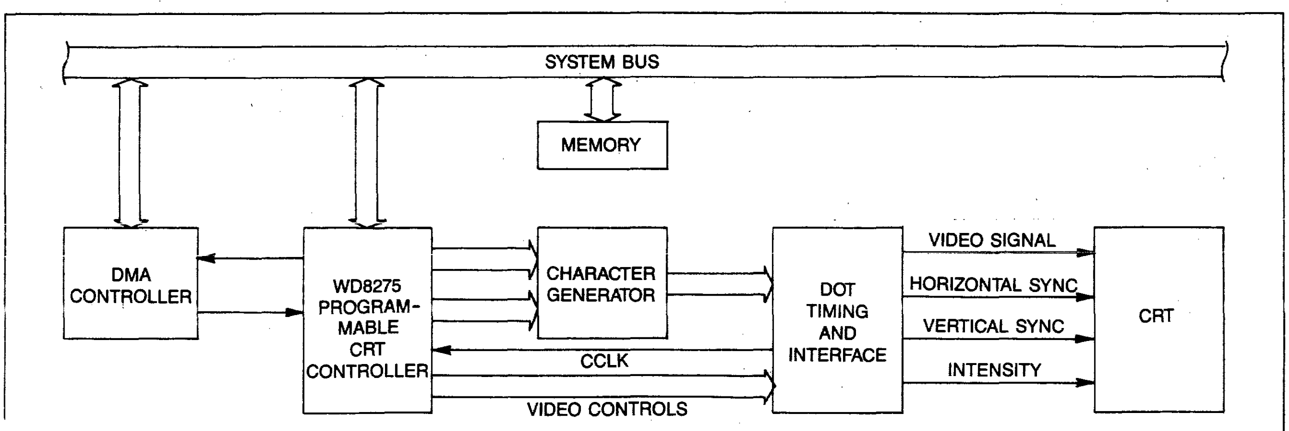
WD 8275 BLOCK DIAGRAM

DESCRIPTION

The WD8275 programmable CRT Controller is a single chip device used to interface raster scan displays with microcomputer systems. Its function is to re-fresh the display by buffering data from main memory and by tracking the display position on the screen. The design flexibility will allow simple interface to raster scan CRT's with a minimum of external hardware/software overhead.

PROPOSED APPLICATIONS

May be used in a wide variety of terminal applications both romote and resident to the computer system. Additionally, this is an ideal device for Light Pen applications. It is available in 2MHZ and 3MHZ versions (CCLK).



SIMPLIFIED SYSTEM DIAGRAM

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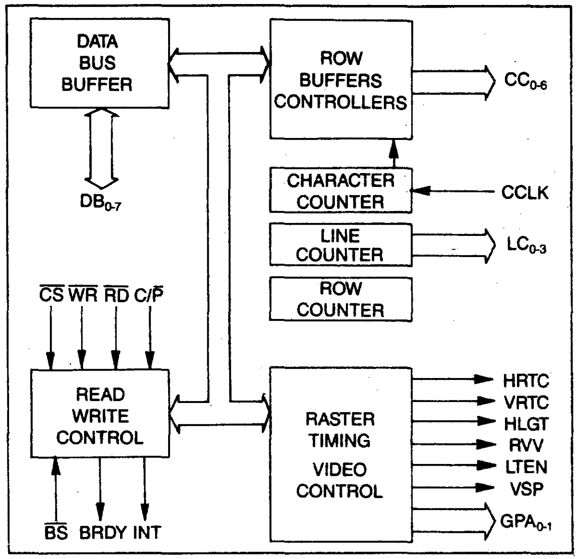
WESTERN DIGITAL
C O R P O R A T I O N

NEW PRODUCT BULLETIN

Small System CRT Controller WD8276

FEATURES

- PROGRAMMABLE CHARACTER/SCREEN FORMAT
  - 1-16 LINES PER ROW
  - 1-64 ROWS PER FRAME
  - 1-80 CHARACTERS PER ROW
- SIX FIELD ATTRIBUTES
  - BLINK
  - HIGHLIGHT
  - REVERSE VIDEO
  - UNDERLINE
  - 2-USER PROGRAMMABLE
- FOUR CURSOR CONTROLS
  - BLINK/NONBLINK UNDERLINE
  - BLINK/NONBLINK REVERSE VIDEO BLOCK
- REQUIRES +5 VOLT ONLY
- 40 PIN CERDIP AND PLASTIC PACKAGES
- COMPATIBLE WITH INTEL D8276/P8276



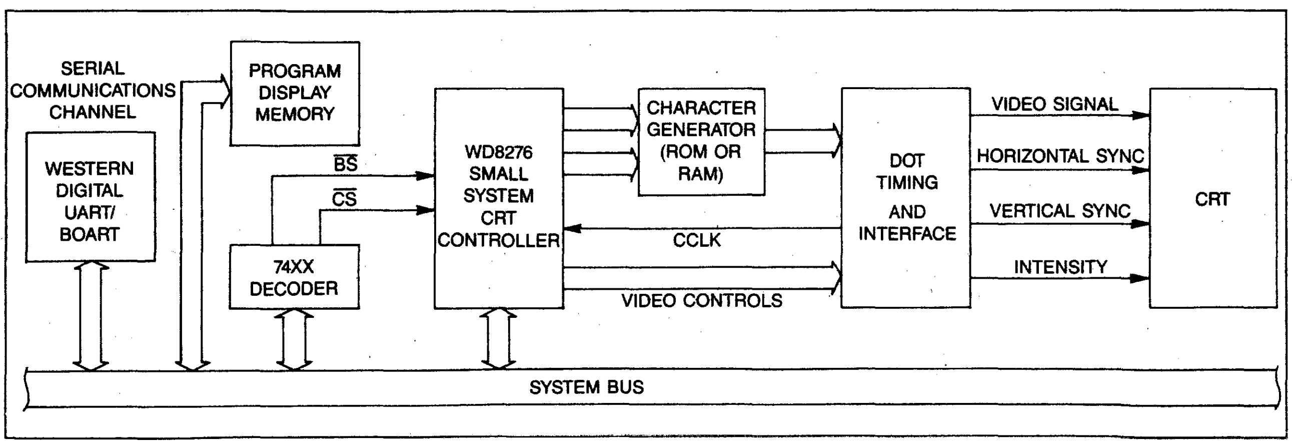
WD8276 BLOCK DIAGRAM

DESCRIPTION

The WD8276 Small System CRT Controller is a single chip device used to interface a raster scan CRT display with a microcomputer in minimum device count systems. It contains the necessary building blocks to refresh the display through character buffering and display position tracking. The flexible design allows simple interface between CRT display and system data bus with a minimum of external hardware.

PROPOSED APPLICATIONS

An ideal, low cost device for both terminal and small computer system designs. It is available in both 2MHZ and 3MHZ versions (CCLK).



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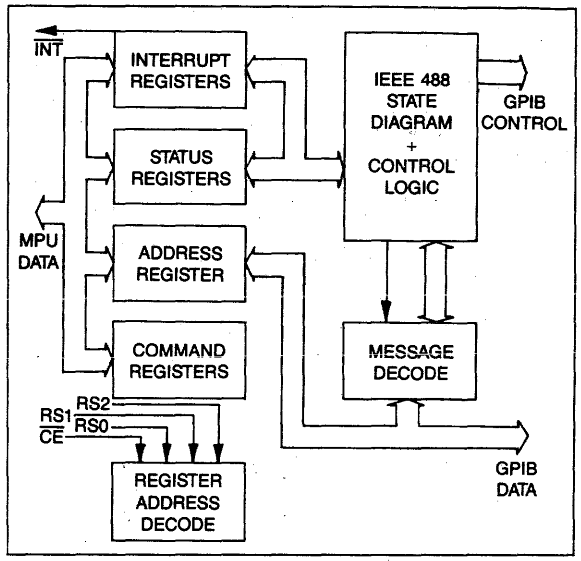
NEW PRODUCT BULLETIN

General Purpose Interface Bus (GPIB) Controller WD9914

FEATURES

- IEEE STD 488 (1975/8) COMPATIBLE
- TALKER/LISTENER FUNCTIONS WITH EXTENDED ADDRESSING
- SYSTEM CONTROLLER CAPABILITY
- SERVICE REQUEST
- SERIAL/PARALLEL POLLING
- DEVICE CLEAR/TRIGGER
- DMA FACILITIES
- COMPATIBLE WITH MOST MICROPROCESSORS
- REQUIRES +5VDC ONLY
- 40 PIN CERDIP/PLASTIC PACKAGING
- COMPATIBLE WITH TEXAS INSTRUMENTS TMS9914A



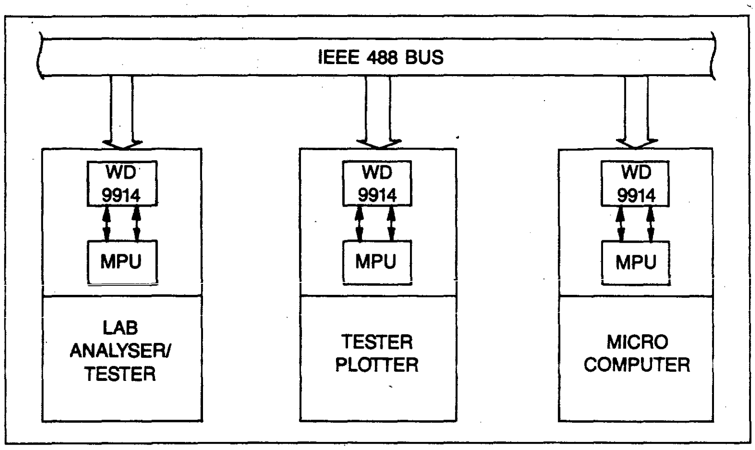
WD9914 BLOCK DIAGRAM

DESCRIPTION

The WD9914 GPIB Controller is a microprocessor controlled device designed to perform the interface function between a microprocessor and the IEEE 488 General Purpose Interface Bus. It automatically handles all Talker, Listener, and Controller operational modes. This relieves the microprocessor from maintaining bus/protocol.

PROPOSED APPLICATIONS

The WD9914 is used in a variety of instruments interconnected by the GPIB and remotely or automatically programmed and controlled. The following is an example:



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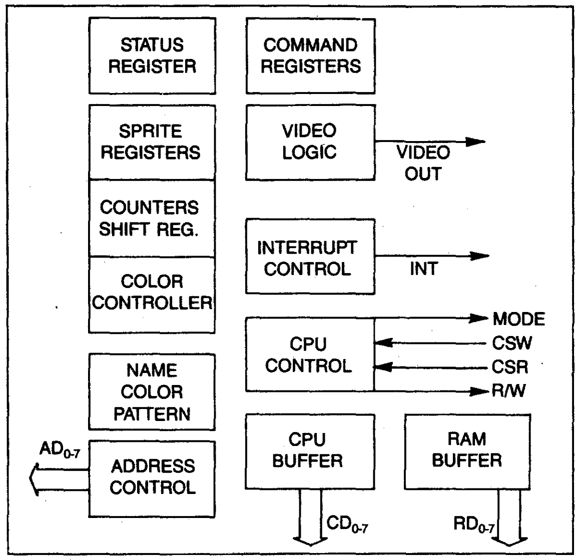
WESTERN DIGITAL
C O R P O R A T I O N

NEW PRODUCT BULLETIN

Video Display Processor
WD9918/9928/9929

FEATURES

- 32 SPRITE (OBJECT ANIMATION) PLANES
- 15 UNIQUE COLORS
- GENERAL 8 BIT CPU INTERFACE
- DIRECT INTERFACE TO 4K, I8K OR 16K RAMS
- 256 X 192 TV SCREEN RESOLUTION
- COMPOSITE VIDEO OUTPUT (WD9918)
- COLOR DIFFERENCE OUTPUTS (WD9928/9929)
- EUROPEAN PAL (625 LINE) TV (WD9929)
- REQUIRES +5 VOLT ONLY
- 40 PIN CERDIP/PLASTIC PACKAGES
- COMPATIBLE WITH TEXAS INSTRUMENTS (TMS9918A, 9928A, 9929A)



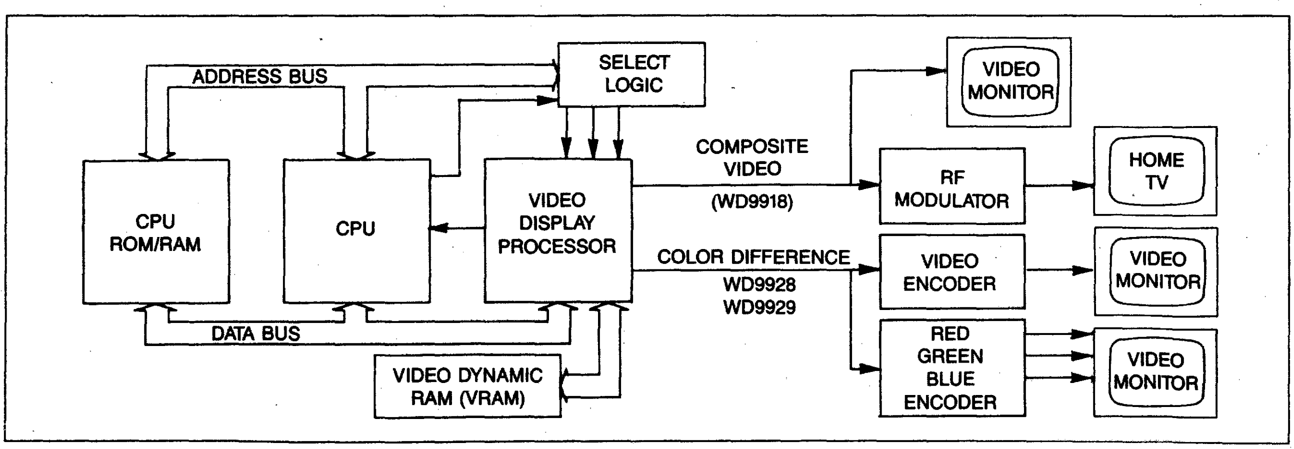
WD9918 BLOCK DIAGRAM

DESCRIPTION

The Video Display Processor is used to interface a microprocessor and screen refresh memory with a raster scan color CRT display. The device generates all necessary video, control and synchronization signals. Additionally, it controls the storage, retrieval, and refresh of display data in the dynamic screen refresh memory.

PROPOSED APPLICATIONS

The WD9918/28/29 are used in any video system requiring the display of digital data on a home color television or color monitor. This includes color computer terminals, home computers, process monitoring, and drafting aids.



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Last Page This Section. Next Page 3150

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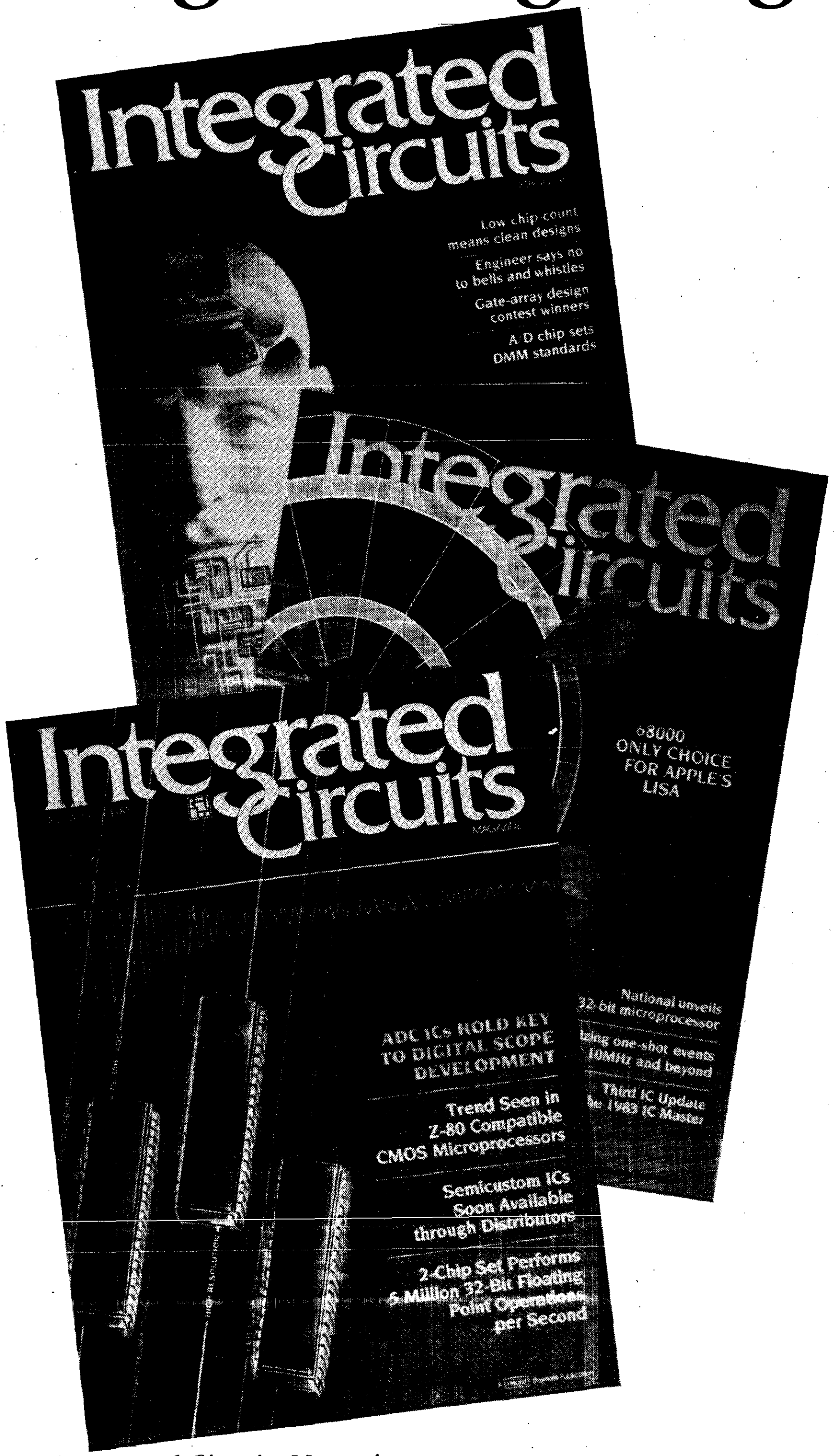

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INTRODUCTION TO LINEAR

The Master Selection Guide provides sufficient information to make initial product selections. All devices that appear in this section, both in the initial selection guide and the data pages, are included in the indexes. These index listings lead to the page and the line on that page where each device appears.

In the Linear section over 1100 operational amplifiers are covered. Since there are so many devices, the operational amplifier entries have been given special consideration. Separate lists are provided for those which have High Speed, High Voltage capability, Wide bandwidth, etc. Under General Purpose, four amplifier types are listed; these are the ones that the high volume manufacturers indicate are the most widely used; however, quad amplifiers should also be considered when appropriate. If you have located an op amp in a specialized category, you can review its characteristics by finding it in the Part Number or Product Indexes and looking it up in the Operational Amplifier Characteristics and in the Data Sections.

Following the special lists, the "Operational Amplifier Characteristics" listings categorize amplifiers by input parameters. They are arranged in order of increasing offset voltage, bias current, offset current and then voltage drift. The other parameters listed do not affect the sequence in which the devices are presented. The column labeled "Comp" indicates the number of external components normally used for compensation for example "0" means no compensation is required.

Consumer circuits such as audio amplifiers, AM, FM, and TV circuits as well as some digital devices (watches, calculators, etc.) are covered by model number in the Consumer Circuit Section. Linear devices and unusual circuits which do not fit elsewhere are listed under the heading "Other Linear Devices."

CATEGORY

Detailed Product Information provided by:

The manufacturers listed above have provided detailed information on their latest and most significant products.

LINEAR

Master Selection Guide

EINFÜHRUNG LINEAR-SCHALTUNGEN

Der Master Selection Guide für Linearschaltungen enthält alle Informationen, die Sie für die Erstauswahl Ihres Produkts benötigen. Die Bauteile, die in diesem Abschnitt erscheinen, sowohl im Selection Guide als auch auf den Datenblättern, sind in allen Master Indexes enthalten. Diese Register verweisen auf die Seite und Zeile, auf der das entsprechende Bauelement vorkommt.

Der Linear-Teil enthält über 1100 Operationsverstärker. Da es hier sehr viele Bausteine gibt, haben die Eintragungen über Operationsverstärker besondere Beachtung gefunden. Es gibt getrennte Listen für solche mit hoher Geschwindigkeit, hoher Spannung, großer Bandbreite usw. Unter "Allgemeine Verwendung" (General Purpose) finden sich vier Verstärkertypen. Laut Aussage der großen Hersteller sind dies die Gebräuchlichsten. Jedoch sollten auch Vierfach-Verstärker auf ihre Verwendbarkeit hin untersucht werden. Haben Sie einen Operationsverstärker in einer bestimmten Kategorie gefunden, so schlagen Sie ihn im numerishen Typenverzeichnis oder im Produktverzeichnis nach und überprüfen seine Eigenschaften unter der Rubrik "Operational Amplifier Characteristics" und in den Datenblättern.

Der Abschnitt "Eigenschaften von Operationsverstärkern" (Operational Amplifier Characteristics) bestimmt die Verstärker nach Eingangs-Parametern. Sie sind nach steigender Offsetspannung, Bias-Strom, offsetstrom und Spannungsdrift angeordnet. Die übrigen aufgeführten Parameter haben keinen Einfluß auf die Reihenfolge, in der die Bauteile genannt werden. Die Spalte "Comp" nennt die Anzahl externer Bausteine, die normalerweise für die Kompensation verwendet werden. "O" z.B. bedeutet, daß keine externe Kompensation erforderlich ist.

Consumer-Schaltkreise wie Audio-Verstärker, AM, FM und TV-Schaltungen sowie einige Digital-Bauteile (Uhren, Rechner usw.) erscheinen nach Typennummer im Abschnitt "Consumer Circuit Section." Solche Linear-Bauelemente und Schaltungen, die in keine entsprechende Rubrik passen, werden unter der Uberschrift "Sonstige Linear-Bauelmente" (Other Linear Devices) aufgeführt.

Neu in diesem Jahr sind erweiterte Listen von Sample/Hold Verstärkern und von festen und einstellbaren Spannungsreferenzen (Fixed and Adjustable Voltage References). Zusätzlich zu der Auflistung unter "Other Linear Devices" finden Sie wichtige Leistungsparameter für diese Produkte am Schluß des Linear-Hauptteils.

INTRODUCTION AUX SYSTEMES LINEAIRES

Le Guide Général de Sélection fournit suffisamment de renseignements pour permettre des sélections initiales de produits. Tous les appareils mentionés dans cette Section, à la fois das le Premier Guide de Selection et dans les feuilles de données, sont inclus dans tous les index. Ces index indiquent à quelle page et à quelle ligne il a été fait mention de tel ou tel appareil.

La Section "Linéaire" décrit plus de 1100 amplificateurs opérationnels. Du fait du nombre considérable d'appareils entrant dans cette catégorie, une attention toute spéciale a été apportée lors de leur classification. Des listes énumèrent séparément les appareils à grande vitesse, à capacité de haut voltage, à grande plage de fréquence, etc. Dans la rubrique "Applications Générales" (General Purpose), quatre types d'amplificateurs sont cités. Ce sont, d'après les gros fabricants, ceux qui sont le plus couramment usités. Les amplificateurs "QUAD" sont également dignes d'attention dans certains cas. Si vous recherchez un amplificateur opérationnel dans une categorie bien definie, vous pourrez en obtenir les caractéristiques en consultant les index des Numéros de Pièces ou de Produits, ainsi que la Section "Caractéristiques des Amplificateurs Opérationels" et les feuilles de données.

La Section "Caractéristiques des Amplificateurs Opérationnels", offre une liste d'amplificateurs classes par paramètre d'entrée. Ces derniers font apparaître dans l'ordre : la tension de compensation, l'ajustement intensité/courant, la compensation du courant, et enfin le changement de tension. Les autres paramètres indiqués n'affectent pas l'ordre dans lequel les appareils sont presentés. La colonne intitulee "COMP" indique le nombre de composants externes également utilisés dans un but de compensation, exemple : "0" signifie qu'aucune compensation n'est nécessaire.

Les circuits de grande consommation tels que les amplificateurs radio AM, FM, les amplificateurs télévision, ainsi que les appareils digitaux (montres, calculatrices, etc.) sont regroupés par numero de modèle dans la Section "Circuits de Grande Consommation" (Consumer Circuit Section). Les appareils linéaires et autres circuits de moins grande utilisation qui n'entrent pas dans les autres catégories, sont énumérés dans la Section "Autres Appareils Linéaires" (Other Linear Devices).

Un additif nouveau à l'édition de cette année : des références sur les amplificateurs partiels/continus, et avec voltage fixe ou ajustable. En plus des listes fournies dans la Section "Autres Appareils Linéaires", d'autres paramètres de performance relativement importants pour ces produits, apparaîssent à la fin du Guide Général de Sélection Linéaire.

INTRODUCCIÓN A LINEAL

La Guía Maestra de Selección provee suficiente información para hacer selecciones iniciales del producto. Todas las componentes que aparecen en esta sección, ya sea en la guía de selección inicial o en las páginas de datos, están incluídas en todos los otros índices. Estas listas de índices los refiere a la página y linea de aquella página donde se encuentra cada componente.

En la sección bajo Lineal, aparecen más de 1,100 amplificadores operacionales. Debido a que hay tantas componentes, se les ha dado consideración especial a los amplificadores operacionales. Listas apartes son provistas para equellos con Alta Velocidad, Capacidad de Alto Voltaje, Banda Ancha, etc. Bajo Propósito General, aparecen cuatro tipos de amplificadores, éstos son los que los fabricantes mayores piensan son los más usados; sin embargo, los amplificadores cuadrangulares deben también ser considerados cuando sea necesario. Si usted ha localizado un amp. op. en una categoría especializada, puede usted estudiar sus características encontrándolo en el Indice de Producto o Número de Pieza y buscándolo en la Sección de Datos de las Características de los Amplificadores Operacionales.

Siguiendo las listas especiales, la lista de "Características del Amplificador Operacional" categoriza los amplificadores por parámetros de entrada. Estos están arreglados por orden ascendente de tensión contrapuesta corriente de polarización, corriente contrapuesta, y también deslizamiento de voltaje o tensión. Los otros parametros mencionados no afectan la secuencia en que las componentes aparecen. La columna titulada "Comp" indica el número de componentes externas que normalmente se emplean para compensación; por ejemplo "O" significa que no requiere compensación.

Circuitos del Consumidor como audioamplificadores, AM, FM, y circuitos de TV así como también algunas componentes digitales (relojes, calculadoras, etc.) aparecen por número de modelo en la Sección de Circuitos del Consumidor. Componentes Lineales y circuitos poco comunes que no corresponden en otras secciones aparecen bajo el título "Otras Componentes Lineales."

Listas expandidas para Amplificadores de Muestra/Retención y Referencias de Voltaje Fijas y Ajustables son nuevas para este año. Además de las listas bajo Otras Componentes Lineales, parámetros de redimiento significantes para estos productos aparecen al final de la Guúa Maestra de Selección.

リニアへの案内

マスターセレクションガイドは素子選択にとりかかる充分な資料を揃えています。最初のセレクションガイド並にデータ掲載ページとこのセクションに記載されている製品はどのインデックにも入っていて，そのページ数と行数がすぐ分ります。

ここでは1,100種以上のオペアンプが収録されています。余りに多品種のため，特別の配慮をしました。それはオペアンプを高速，高耐圧，高域巾他と別々に掲載しました。搬用オペアンプには4種のアンプをのせてあります。大量生産している会社が最も巾広く使用されていると云う品種です。がクオドアンプももし適当なものがあれば考慮すべきかも知れません。
あるカテゴリーでオペアンプを見つけられたらその特性をパーツナンバーインデックスかプロダクトインデックスで探し検討し，オペアンプ特性表やデータセクションを良く調べて下さい。

特殊品種リストに続きオペアンプ特性表があり入出パラメーター毎にオペアンプが分類されています。製品はオフセット電圧，バイアス電流，オフセット電流，電圧ドリフト等小さな順に記載されています。"Comp" と表示されている項目の下の数字は0調整をする為に外付部品が何個必要かを示しています。例えば"0"となっていれば0調整不要を意味します。

民生用製品－オーディオアンプ，AM，FM，TV素子，ディジタル素子（時計用，電卓用等）は"コンシューマーサーキットセクション"に掲載されています。他のどのカテゴリーにも入らないリニアや特異な素子は"アザーリニアデバイス"の見出しに載っています。

本年新たに加わったものとしてサンプル／ホールドアンプと固定，調整可能なボルティジリファレンスが広くのっています。
"アザーリニアデバイス"欄にのっている製品中顕著な性能パラメーターはリニアマスターセレクションガイドの最後に掲載されています。

LINEAR-Amplifiers, Special Purpose

Special Purpose

Function	Device	Source	Page
AC Amplifier, Quad, Single Supply	**CA3048**	† **RCA**	(3601)
	CA3052	**RCA**	(3601)
AGC Amplifier, 20 Hz to 10 MHz, 6 dB Dynamic Range	MY108	AnalogSys	
AGC Generator, for SSB Receivers	SL621C	Plessey	
AGC Generator (voice operated gain adjusting device)	SL620C	Plessey	
	SL6270	Plessey	
Amplifier, CATV. See Linear—Consumer Circuits, TV			
Amplifier for IR Remote Control (1300 dB gain, 8 kHz bandwidth)	U250	Telefunken	
	U3043M	Telefunken	
	U3083M	Telefunken	
Amplifier with Photodiode	TFA1001	Siemens	
Audio Amplifier with Three NPN Transistors	LM389	National	
Current Amplifier (unity gain, 100 mA output)	3329	† Burr-Brown	
	HA-5033	† **Harris**	(3462)
	LH0002	† National	
	LH0002C	National	
Current Amplifier (unity gain, 200 mA output)	**3553**	† **Burr-Brown**	(2850,2851)
	9963	† OEI	
Current Amplifier (unity gain, 300 mA output)	MC1438	Motorola	
	MC1538	† Motorola	
	2003	TeledyneP	
	2003-01	† TeledyneP	
Current Amplifier (unity gain, 500 mA output)	9910	† OEI	
	9911	† OEI	
Current Amplifier (unity gain, 600 mA output)	**HA-2630**	† **Harris**	(3410)
	HA-2635	Harris	
Current Amplifier (wideband, 100 mA output)	**HOS-100AH**	**AD**	(3353)
	HOS-199SH	† AD	
Current Amplifiers, See also Linear-Followers			
Current Booster, 100 mA Output (for op amp)	2035	† TeledyneP	
Differential/Cascode Amplifier (dc to rf)	MC3330	Motorola	
	CA3028A	† **RCA**	(3603)
	CA3028B	† **RCA**	(3603)
	CA3053	† **RCA**	(3603)
Differential High Speed FET Input Amplifier	MP215	Analogic	
Differential Input/Differential Output Amplifier (bandwidth less than 2 MHz)	MC1590G	† Motorola	
	CA3000	† RCA	
Differential/Video Amplifier	CLC103A	Comlinear	
	CLC103AM	† Comlinear	
	μPC754	**NEC**	(3547)
Fiber Optic Receiver Amplifier	LH0082	† National	
	LH0082C	National	
Floppy Disc Read Amplifier System	**XR3470A**	**Exar**	(3372,3373)
	MC3470	**Motorola**	(3061)
	MC3470A	**Motorola**	(3061)
	MC3470	TI	
Floppy Disc Write Amplifier	**XR2247**	**Exar**	(3371,3372)
Front End Amplifier (for ultrasonic or infrared remote control systems)	TDA4180	Telefunken	
Hearing Aid Amplifiers. See Linear-Consumer Circuits			
Instrumentation Amplifier	**INA101SM**	† **Burr-Brown**	(2851)
	MPINA101A	† MicroPwr	
	MPINA101B	† MicroPwr	
	MPINA101C	† MicroPwr	
	MPINA101S	† MicroPwr	
Instrumentation (commutating auto zero)	ICL7605C	Intersil	
	ICL7605M	† Intersil	
	ICL7606C	Intersil	
	ICL7606M	† Intersil	
Instrumentation, (different input, independent gain adjustment)	AMP-01	† PMI	
Instrumentation, (differential input, independent gain adjustment)	AD521J	AD	
	AD521K	AD	
	AD521L	AD	
	AD521S	† AD	
	3626A	Burr-Brown	
	3626B	Burr-Brown	
	3626C	Burr-Brown	
	3629	† **Burr-Brown**	(2851)
	3630A	**Burr-Brown**	(2851)
	3630B	**Burr-Brown**	(2851)
	3630C	**Burr-Brown**	(2851)
	3630S	**Burr-Brown**	(2851)
	INA101	**Burr-Brown**	(2851)
	INA104	Burr-Brown	
	MN2200	**MicroNet**	(3042)
	MN2200H	† **MicroNet**	(3042)
	MN2201	MicroNet	
	MN2201H	† MicroNet	
	LH0036	† National	
	LH0036C	National	
	LH0037	† National	
	LH0037C	National	
	LH0038	† National	
	LH0038C	National	
	AD522A	AD	
	AD522B	AD	
	AD522S	† AD	
	HC3020	HyComp	
	LM163A	† National	
	LM363	National	
	LM363A	† National	
Instrumentation, Digitally Programmable Gain	**PGA100AG**	**Burr-Brown**	(2851)
	PGA100BG	**Burr-Brown**	(2851)
	LH0084	† National	
	LH0084C	National	
	LH0086	† National	
	LH0086C	National	
	AM-542MC	**Datel**	(2861)
	AM-542MM	† **Datel**	(2861)
	AM-542MR	**Datel**	(2861)
	AM-543MC	**Datel**	(2861)
	AM-543MM	† **Datel**	(2861)
	AM-543MR	**Datel**	(2861)
Instrumentation, Pin Programmable Gain	AD624A	AD	
	AD624B	AD	
	AD624C	AD	
	AD624S	† AD	
Instrumentation (unity gain)	**3627**	**Burr-Brown**	(2851)
Isolation Amplifier	MP225A	Analogic	
	MP227	Analogic	
Isolation Amplifier, High Gain	MP226	Analogic	
Isolation Amplifier, Optically Coupled	**3650HG**	**Burr-Brown**	(2852)
	3652HG	**Burr-Brown**	(2852)
	ISO100AP	**Burr-Brown**	(2852)
Isolation Amplifier, Transformer Coupled	**3456**	**Burr-Brown**	(2851)
	3656AG	**Burr-Brown**	(2851)
Isolation Amplifier, 4 Channel	AH427	Analogic	
Linear-Antilog Amplifier (current in, current out)	SSM2010	SSM	
	SSM2012	SSM	
Linear-Antilog Amplifier, Dual (differential input, separate control inputs)	SSM2000	SSM	
	SSM2020	SSM	
	SSM2022	SSM	
Log Amplifier	**XR7000**	**Exar**	(3385)
Log Amplifier, Bipolar (module)	2531A	OEI	
Log/Antilog Amplifier, (antilog)	ICL8049C	Intersil	
	2910	† OEI	
	2920	OEI	
	SSM2100	SSM	
Log/Antilog Amplifier, (log)	**4127**	**Burr-Brown**	(2852)
	ICL8048C	Intersil	
	2910	† OEI	
	2920	OEI	
	TL441M	† TI	
Log/Log Ratio Amplifier	**LOG100**	**Burr-Brown**	(2852)
Low Noise, Low Level, Chopper Stabilized Amplifier	MP221	Analogic	
Memory Read Amplifier, Four Head Disk	TL030	TI	
Microphone Amplifier, Electret	PBL3721	RIFA	
Microphone Amplifier (for microphones in telephones)	TDD0246	Telefunken	
Microphone/Headphone Amplifier	SL6310	Plessey	
Microphone Preamplifier	SSM2015	SSM	
Mixer (to 200 MHz)	S042	Siemens	
Operational Amplifier, Band-Select Switch, AFT Mode Switch (for frequency-synthesizer TV systems)	CA3166	RCA	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Amplifiers, Special Purpose (Cont'd)

Special Purpose (Cont'd)

Function	Device	Source
Operational Amplifier/Comparator with Shutdown Control and Isolated Transistor	CA3177	RCA
Operational Amplifier/Voltage Comparator, Dual	LM2924	National
	LM3924	National
	LM192	† National
	LM292	National
	LM392	National
Operational Amplifier, Dual with Dual Voltage Comparator	MC3405	Motorola
	MC3505	† Motorola
Operational Transconductance Amplifier	**HA-23080**	**† Harris (3464)**
Operational Transconductance Amplifier, Dual	LM13600	Raytheon
	LM13600A	Raytheon
Power Amplifier, Motor and Actuator Driver, to 12 V, 1.5 A	ICH8515I	Intersil
	ICH8515M	† Intersil
Power Amplifier, Motor and Actuator Driver, to 24 V, 3 A	**ICH8510I**	**Intersil (3479)**
	ICH8510M	**† Intersil (3479)**
	ICH8520I	**Intersil (3479)**
	ICH8520M	**† Intersil (3479)**
	ICH8530I	**Intersil (3479)**
	ICH8530M	**† Intersil (3479)**
Power Transistor Driver/Amplifier, Biases External MOSFET Devices	MA500	AnalogSys
Preamplifier, for IR Remote Control	TDA2320	SGS
Preamplifier, for Ultrasonic Remote Control	TDA3047	Signetics
Preamplifier, Infrared (74 dB gain, 100 kHz bandwidth)	TDA4050B	Siemens
Preamplifier, Low Noise (35 dB gain, 100 MHz bandwidth)	AH0013CA	OEI
	AH0013CB	OEI
	AH0013MA	† OEI
Preamplifier, Precision (to precede operational amplifiers)	LM121	† National
	LM121A	† National
	LM221	National
	LM221A	National
	LM321	National
	LM321A	National
Preamplifier, Temperature Controlled	μA727C	Fairchild
	μA727M	† Fairchild
Programmable Channel Op Amp (one of 4 input stages can be connected to single output)	**HA-2400**	**† Harris (3394)**
	HA-2404	Harris
	HA-2405	Harris
Programmable Gain Amplifier (digitally controlled gain)	**3606**	**Burr-Brown (2851)**
	HS2020	HybridSys
	MN2020	**MicroNet (3042)**
Read Amplifier/Preamplifier (for magnetic tape memory systems)	MC3467	Motorola
	MC3468	Motorola
RF Amplifier, Gated	MC1445	Motorola
	MC1545	† Motorola
	MC1445	TI
RF Amplifiers, Hybrids	MHW401	Motorola
	MHW590	Motorola
	MHW591	Motorola
	MHW592	Motorola
	MHW593	Motorola
	MHW601	Motorola
	MHW602	Motorola
	MHW603	Motorola
	MHW709	Motorola
	MHW710	Motorola
	CA2800	TRW-LSI
	CA2810	TRW-LSI
	CA2820	TRW-LSI
	CA2830	TRW-LSI
	CA2840	TRW-LSI
	CA2842	TRW-LSI
	CA2850	TRW-LSI
	CA2851	TRW-LSI
	CA2870	TRW-LSI
	CA2871	TRW-LSI
	CA2875	TRW-LSI
	CA2876	TRW-LSI
	CA2880	TRW-LSI
Signal Sources Switch, (buffer amplifiers with input switches)	TDA1028	Signetics
	TDA1029	Signetics
Thermocouple Amplifier with Cold Junction Compensation	**AD594A**	**AD (3356)**
	AD594C	**AD (3356)**
	AD595A	**AD (3356)**
	AD595C	**AD (3356)**
Video Buffer Amplifier	HA-5033-2	† Harris
	HA-5033-5	Harris
Video, IF and RF Amplifiers	CLC100	Comlinear
	CLC102	Comlinear
	CLC104A	Comlinear
	CLC104AM	† Comlinear
	CLC200A	Comlinear
	CLC200AM	† Comlinear
	CLC220A	Comlinear
	CLC220AM	† Comlinear
	μA733C	Fairchild
	μA733M	† Fairchild
	μA733	† Intersil
	μA733C	Intersil
	MC1550	† Motorola
	MC1733	† Motorola
	MC1733C	Motorola
	NE592	Motorola
	SE592	† Motorola
	LM733	† National
	μPC1651	NEC
	AN607	Panasonic
	AN608	Panasonic
	SL1550	Plessey
	SL541	Plessey
	SL550	Plessey
	SL560	Plessey
	SL610C	Plessey
	SL611C	Plessey
	SL612C	Plessey
	CA3001	† RCA
	CA3011	† RCA
	CA3020A	RCA
	CA3021	† RCA
	CA3022	† RCA
	CA3023	† RCA
	CA3040	† RCA
	NE592	**Signetics (3675)**
	SE592	**† Signetics (3675)**

(Continued)

Function	Device	Source
Video, IF and RF Amplifiers (Cont'd)	TDA3541	Signetics
	μA733	† Signetics
	μA733C	Signetics
	SG1401	† SiliconG
	SG2401	SiliconG
	SG3001	† SiliconG
	SG3401	SiliconG
	SG733	† SiliconG
	SG733C	SiliconG
	NE592	TI
	TL592	TI
	μA733C	TI
	μA733M	† TI
	TA7061A	Toshiba
Voltage Controlled Amplifier	SSM2013	SSM
Wideband Amplifier, Logarithmic Limiting (4 to 500 MHz)	SL1531	Plessey
	SL1532	Plessey
	SL531C	Plessey
	SL532C	Plessey
Wideband Amplifier with Low Level Video Detection (7 to 200 MHz for log IF amplifiers)	SL1521	† Plessey
	SL1522	Plessey
	SL1523	Plessey
	SL1524	Plessey
	SL1525	Plessey
	SL521	Plessey
	SL523	Plessey
Quad Current Controlled Amplifier	SSM2024	SSM
Hex Analog CMOS Amplifier	MA113	AnalogSys
Two Wire Transmitter (Sends current signal over same two lines from which it is powered.)	**XTR100AM**	**† Burr-Brown (2851)**
	XTR100AP	**Burr-Brown (2851)**
	XTR100BM	**† Burr-Brown (2851)**
	XTR100BP	**Burr-Brown (2851)**
	LH0045	† National
	LH0045C	National

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Arrays

Function	Device	Source
Transistor Arrays		
Darlington Pair and Two Matched NPN Transistors		
	CA3018	† **RCA** (3601)
	CA3018A	† **RCA** (3601)
	CA3118	† **RCA** (3601)
	CA3118A	† **RCA** (3601)
Differential Pair and Three NPN Transistors		
	μA3086M	Fairchild
	MC3346	† Motorola
	MC3386	† Motorola
	LM3045	† National
	LM3046	National
	LM3086	National
	LM3146	National
	SL3045	† Plessey
	SL3046	Plessey
	SL3145	† Plessey
	CA3045	† **RCA** (3601)
	CA3046	† **RCA** (3601)
	CA3086	† **RCA** (3601)
	CA3146	**RCA** (3601)
	CA3146A	**RCA** (3601)
	TBA331	SGS
	TCA671	Siemens
	TCA871	Siemens
	TCA971	Siemens
	TCA991	Siemens
	SG3045	SiliconG
	SG3046	SiliconG
	SG3086	† SiliconG
	SG3146	SiliconG
	SG3821	SiliconG
	SG3886	SiliconG
	ULN-2046A	Sprague
	ULN-2086A	Sprague
	ULS-2045H	† Sprague
Dual Darlington (NPN) and Two NPN Transistors		
	SG3823	SiliconG
Dual Darlington (NPN-PNP quasi complementary)		
	TDA1410	SGS
	TDA1420	SGS
Dual Darlington Switch		
	ULN-2061M	Sprague
	ULN-2062M	Sprague
Dual Differential Amplifiers (NPN), to 120 MHz		
	CA3054	Motorola
	CA3026	RCA
	CA3054	RCA
	SG3822	SiliconG
	ULN-2054A	Sprague
Dual Differential Amplifiers (NPN), to 500 MHz		
	CA3049	† **RCA** (3601)
	CA3102	† **RCA** (3601)
Dual Differential Amplifiers (NPN) with Diode Bias String		
	CA3050	† RCA
	CA3051	RCA
Dual Transistors (ft>5 GHz)		
	SL2363C	Plessey
	SL2364C	Plessey
Dual Transistors, Monolithic NPN, Logarithmic Conformance	MP318	MicroPwr
	MAT-01	† PMI
	MAT-01A	† PMI
	MAT-01F	† PMI
	MAT-01G	† PMI
	MAT-01H	PMI
Dual Transistors, Monolithic NPN Tightly Matched		
	IT120	Intersil
	IT120A	Intersil
	IT121	Intersil
	IT122	Intersil
(Continued)		
Dual Transistors, Monolithic NPN Tightly Matched (Cont'd)		
	MP301	MicroPwr
	MP302	MicroPwr
	MP303	MicroPwr
	MP310	MicroPwr
	MP311	MicroPwr
	MP312	MicroPwr
	MP313	MicroPwr
	MP361	MicroPwr
	MP362	MicroPwr
	LM194	† National
	LM394	National
	SL360	Plessey
	SL362	Plessey
Dual Transistors, Monolithic NPN, Tightly Matched, Low Noise	**MAT-02A**	† **PMI** (3569)
	MAT-02B	† **PMI** (3569)
	MAT-02E	**PMI** (3569)
	MAT-02F	**PMI** (3569)
Dual Transistors, Monolithic N-Channel JFET, Tightly Matched	MP3954	MicroPwr
	MP3954A	MicroPwr
	MP3955	MicroPwr
	MP3956	MicroPwr
	MP3958	MicroPwr
	MP5911	MicroPwr
	MP5912	MicroPwr
	MP5912C	MicroPwr
	MP830	MicroPwr
	MP831	MicroPwr
	MP832	MicroPwr
	MP833	MicroPwr
	MP840	MicroPwr
	MP841	MicroPwr
	MP843	MicroPwr
	MP844	MicroPwr
	MP845	MicroPwr
Dual Transistors, Monolithic PNP, Logarithmic Conformance	MP358	MicroPwr
Dual Transistors, Monolithic PNP, Tightly Matched		
	IT130	Intersil
	IT130A	Intersil
	IT131	Intersil
	IT132	Intersil
	MP350	MicroPwr
	MP351	MicroPwr
	MP352	MicroPwr
Quad Darlington Switch		
	ULN2068	Motorola
	ULN2074	Motorola
	L702	SGS
	SG2064	SiliconG
	SG2065	SiliconG
	SG2066	SiliconG
	SG2067	SiliconG
	SG2068	SiliconG
	SG2069	SiliconG
	SG2070	SiliconG
	SG2072	SiliconG
	SG2073	SiliconG
	SG2074	SiliconG
	SG2075	SiliconG
	SG2076	SiliconG
	SG2077	SiliconG
	UDN-2841B	Sprague
	UDN-2845B	Sprague
	ULN-2064B	Sprague
	ULN-2065B	Sprague
	ULN-2066B	Sprague
	ULN-2067B	Sprague
	ULN-2068B	Sprague
	ULN-2069B	Sprague
(Continued)		
Quad Darlington Switch (Cont'd)		
	ULN-2070B	Sprague
	ULN-2071B	Sprague
	ULN-2074B	Sprague
	ULN-2075B	Sprague
	ULN-2076B	Sprague
	ULN-2077B	Sprague
	UDN2841	TI
	UDN2845	TI
	ULN2064	TI
	ULN2065	TI
Hex NPN Darlington		
	LB1274	Sanyo
One Darlington PNP Pair, and One Current Mirror Pair with Shared Diode, and Two PNP Transistors		
	CA3084	RCA
Three Differential Amplifiers (NPN)		
	MC3350	Motorola
	ULN-2047A	Sprague
Three NPN and two PNP Transistors		
	CA3096	† **RCA** (3601)
	CA3096A	† **RCA** (3601)
	CA3096C	† **RCA** (3601)
Four High Current NPN Transistors (core driver)		
	FQ3724	Fairchild
	FQ3725	Fairchild
	MHQ4001A	Motorola
	MHQ4002A	Motorola
	MHQ4013	Motorola
	MHQ4014	Motorola
	MPQ3303	Motorola
	MPQ3725	Motorola
	MPQ3725A	Motorola
	MPQ4003	Motorola
	MPQ4004	Motorola
	DH3725C	National
	DH6376C	National
	CA1724G	† **RCA** (3601)
	CA1725G	† **RCA** (3601)
	CA3138	† RCA
	CA3138A	† RCA
	TPQ3724	Sprague
	TPQ3725	Sprague
	TPQ3725A	Sprague
Four High Current PNP Transistors (core driver)		
	FQ3467	Fairchild
	FQ3468	Fairchild
	MHQ3467	Motorola
	DH3467C	National
Five High Current NPN Transistors		
	CA3083	† RCA
	CA3183	† **RCA** (3601)
	TDA3083	Signetics
	SG3083	† SiliconG
	SG3183	† SiliconG
	SG3183A	† SiliconG
	ULN-2083A	Sprague
	ULS-2083H	† Sprague
Five High Frequency NPN Transistors, (ft>5 GHz)		
	SL3127	Plessey
	CA3127	**RCA** (3601)
	CA3227	**RCA** (3601)
	CA3246	**RCA** (3601)
Five High Voltage, High Current NPN Darlington Amplifiers		
	LB1287	Sanyo
	LB1288	Sanyo
Five High Voltage, High Current NPN Darlington Amplifiers, Source, for Load Connected to Negative Supply	UDN-2956A	Sprague
	UDN-2957A	Sprague
Five Low-Noise NPN Transistors		
	TDA3310	SGS

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR

Master Selection Guide

LINEAR–Arrays (Cont'd)

Function	Device	Source	
Transistor Arrays (Cont'd)			
Six NPN Darlingtons	LB1272	Sanyo	
	LB1273R	Sanyo	
Seven High Current Darlingtons	ULN-2031A	Sprague	
	ULN-2032A	Sprague	
	ULN-2033A	Sprague	
Seven High Current, High Voltage, NPN Darlington Amplifiers, Open Collector, to 100 V, 500 mA	SN75465	TI	
	SN75468	TI	
	SN75469	TI	
Seven High Current, High Voltage, NPN Darlington Amplifiers, Open Collector, to 50 V, 500 mA	**XR2001C**	**Exar**	**(3383)**
	XR2002C	**Exar**	**(3383)**
	XR2003C	**Exar**	**(3383)**
	XR2004C	**Exar**	**(3383)**
	XR2011C	**Exar**	**(3383)**
	XR2012C	**Exar**	**(3383)**
	XR2013C	**Exar**	**(3383)**
	XR2014C	**Exar**	**(3383)**
	XR2201	Exar	
	XR2201M	† Exar	
	XR2202	Exar	
	XR2202M	† Exar	
	XR2203	Exar	
	XR2203M	† Exar	
	XR2204	Exar	
	XR2204M	† Exar	
	9665	Fairchild	
	9666	Fairchild	
	9666M	† Fairchild	
	9667	Fairchild	
	9667M	† Fairchild	
	9668	Fairchild	
	9668M	† Fairchild	
	MC1411	**Motorola**	**(3064)**
	MC1412	**Motorola**	**(3064)**
	MC1413	**Motorola**	**(3064)**
	MC1416	**Motorola**	**(3064)**
	PBD352301	RIFA	
	PBD352302	RIFA	
	PBD352303	RIFA	
	RBD352301	RIFA	
	RBD352302	RIFA	
	RBD352303	RIFA	
	L201	SGS	
	L202	SGS	
	L203	SGS	
	L204	SGS	
	ULN2001	Signetics	
	ULN2003	Signetics	
	ULN2004	Signetics	
	SG2001	SiliconG	
	SG2002	SiliconG	
	SG2003	SiliconG	
	SG3851	SiliconG	
	SG3852	SiliconG	
	SG3853	SiliconG	
	ULN-2001A	Sprague	
	ULN-2002A	Sprague	
	ULN-2003A	Sprague	
	ULN-2004A	Sprague	
	ULN-2005A	Sprague	
	ULS-2001H	† Sprague	
	ULS-2002H	† Sprague	
	ULS-2003H	† Sprague	
	ULS-2004H	† Sprague	
	ULS-2005H	† Sprague	
	SN75466	TI	
(Continued)			
Seven High Current, High Voltage, NPN Darlington Amplifiers, Open Collector, to 50 V, 500 mA (Cont'd)	SN75467	TI	
	ULN2001A	TI	
	ULN2002A	TI	
	ULN2003A	TI	
	ULN2004A	TI	
	ULN2005A	TI	
Seven High Current, High Voltage NPN Darlington Amplifiers, Open Collector, to 50 V, 600 mA	ULN-2011A	Sprague	
	ULN-2012A	Sprague	
	ULN-2013A	Sprague	
	ULN-2014A	Sprague	
	ULN-2015A	Sprague	
	ULS-2011H	† Sprague	
	ULS-2012H	† Sprague	
	ULS-2013H	† Sprague	
	ULS-2014H	† Sprague	
	ULS-2015H	† Sprague	
Seven High Current, High Voltage NPN Darlington Amplifiers, Open Collector, to 95 V, 500 mA	ULN-2021A	Sprague	
	ULN-2022A	Sprague	
	ULN-2023A	Sprague	
	ULN-2024A	Sprague	
	ULN-2025A	Sprague	
	ULS-2021H	† Sprague	
	ULS-2022H	† Sprague	
	ULS-2023H	† Sprague	
	ULS-2024H	† Sprague	
	ULS-2025H	† Sprague	
Seven High Current NPN Transistors, Common Collector	**CA3082**	**† RCA**	**(3601)**
	SG3082	SiliconG	
	ULN-2082A	Sprague	
Seven NPN Darlingtons	LB1275	Sanyo	
Seven NPN Transistors, Common Emitter	**CA3081**	**† RCA**	**(3601)**
	CA3081	Signetics	
	SG3081	SiliconG	
	ULN-2081A	Sprague	
Seven-Stage Driver Array	LB1260	Sanyo	
	LB1261	Sanyo	
	LB1264	Sanyo	
Eight High Current, High Voltage NPN Darlington Amplifiers, Current Source	UDN-2981A	Sprague	
	UDN-2982A	Sprague	
	UDN-2983A	Sprague	
	UDN-2984A	Sprague	
	UDS-2981H	† Sprague	
	UDS-2982H	† Sprague	
	UDS-2983H	† Sprague	
	UDS-2984H	† Sprague	
Eight High Current, High Voltage NPN Darlington Amplifiers, Open Collector, to 50 V, 500 mA	ULN-2801A	Sprague	
	ULN-2802A	Sprague	
	ULN-2803A	Sprague	
	ULN-2804A	Sprague	
	ULN-2805A	Sprague	
	ULS-2801H	† Sprague	
	ULS-2802H	† Sprague	
	ULS-2803H	† Sprague	
	ULS-2804H	† Sprague	
	ULS-2805H	† Sprague	
Eight High Current, High Voltage NPN Darlington Amplifiers, Open Collector, to 50 V, 600 mA	ULN-2811A	Sprague	
	ULN-2812A	Sprague	
	ULN-2813A	Sprague	
	ULN-2814A	Sprague	
	ULN-2815A	Sprague	
	ULS-2811H	† Sprague	
	ULS-2812H	† Sprague	
	ULS-2813H	† Sprague	
	ULS-2814H	† Sprague	
	ULS-2815H	† Sprague	
Eight High Current, High Voltage NPN Darlington Amplifiers, Open Collector, to 500 mA	L601	SGS	
	L602	SGS	
	L603	SGS	
	L604	SGS	
Eight High Current, High Voltage NPN Darlington Amplifiers, Open Collector, to 95 V, 500 mA	ULN-2821A	Sprague	
	ULN-2822A	Sprague	
	ULN-2823A	Sprague	
	ULN-2824A	Sprague	
	ULN-2825A	Sprague	
	ULS-2821H	† Sprague	
	ULS-2822H	† Sprague	
	ULS-2823H	† Sprague	
	ULS-2824H	† Sprague	
	ULS-2825H	† Sprague	
Special Arrays			
CMOS (three p-channel and three n-channel enhancement MOS transistors tested for linear operation)	**CA3600**	**† RCA**	**(3601)**
Diode Array (one diode quad and two isolated)	**CA3019**	**† RCA**	**(3601)**
Diode Array (10 element)	**CA3141**	**RCA**	**(3601)**
Diode Array (16 element)	DN803	Panasonic	
SCR Array (eight SCRs with current-limiting resistors)	UTN-2886B	Sprague	
	UTN-2888A	Sprague	
Thyristor/Transistor Array (SCR, programmable unjunction transistor, PNP/NPN transistor pair, NPN transistor and zener diode)	**CA3097**	**† RCA**	**(3601)**

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Comparators

Offset Voltage mV (25°C)	Bias Current (25°C)	Offset Current (25°C)	Response Time ns	Max. Differential Voltage	Gain	Fan Out	Supply Voltage, V	Device	Source
Comparators-Single									
0.25	1.2 μA	80 nA	30	—	20K	—	5, −16	**RC4805A**	**Raytheon (3805)**
								RM4805A	† **Raytheon (3582)**
	1200 nA	80 nA	35 *	—	8000	—	5 to ±18	CMP-05A	† PMI
								CMP-05E	PMI
0.5 *	0.25 nA	0.1 nA	—	30	200K *	5	5, 0 to ±15	TL111	† TI
0.6	1.8 μA	150 nA	30	—	20K	—	5, −16	**RC4805**	**Raytheon (3805)**
								RM4805	† **Raytheon (3582)**
	1800 nA	150 nA	35 *	—	7000	—	5 to ±18	CMP-05B	† PMI
								CMP-05F	PMI
0.7	0.1 μA	40 nA	200	—	200K	5	5	LF2111	† National
0.8	50 nA	3 nA	270	11	200K		5 to ±18	CMP-02	† PMI
								CMP-02B	PMI
								CMP-02E	PMI
	600 nA	25 nA	180	11	200K		5 to ±18	CMP-01	† PMI
								CMP-01B	PMI
								CMP-01E	PMI
2.0	10 μA	1 μA	6.5	6			−5.2,6	AM685L	AMD
								AM685M	† AMD
			12	6		5	−6,5	AM686M	† AMD
	15 μA	3 μA	80	5	12.5K		−6,12	TL810M	† TI
	20 μA	3 μA	40	5	40K *	10	−3 to -12,12	LM106	† National
								LM206	National
			40 *	5	1250	1	−6,12	μA710M	† Fairchild
								MC1710	† Motorola
								LM710	† National
								SG710	† SiliconG
								μA710M	† TI
								SFC2710	† Thomson-CSF
	45 μA	3 μA	40	5	40K	10	−3 to -12,12	LM106	† TI
2.8	100 nA	15 nA	270	11	100K		5 to ±18	CMP-02C	PMI
	900 nA	80 nA	180	11	200K		5 to ±18	CMP-01C	PMI
3.0	5 μA	2 μA *	20	5	3K *	2	5,(−6, 5-±15)	LM161	† National
								LM261	National
	10 μA	1 μA	12	6			−6,5	AM686C	AMD
	50 nA	10 nA	200	10	35K		±5 to ±18	μA734M	† Fairchild
	100 nA	10 nA	165 *	30	200K *	5	5, 0 to ±15	LM111	† TI
			200 *	30	200K *	5	5, 0 to ±15	AD111	† AD
								AD211	AD
								μA111M	† Fairchild
								LM111	† Intersil
								LM111	† Motorola
								LM211	Motorola
								LM111	† National
								LM211	National
								LM111	† Raytheon
								LM111	† Signetics
								LM211	Signetics
								SG111	† SiliconG
								SG211	SiliconG
								SFC2111	† Thomson-CSF
								SFC2211	Thomson-CSF
			250	30	200K *	5	5, 0 to ±15	LM111	† AMD
								LM211	AMD
		20 nA	250 *	15	15K		5-15, ±5-±15	ICL8001M	† Intersil
3.5	20 μA	5 μA	80	5	10K		−6,12	TL810C	TI
4.0	2 μA	0.5 μA	26	5	5K *		5,(−6, 5-±10)	**SE527**	† **Signetics (3621)**
	12 μA	3 μA	22	5	5K *		5,(−6, 5-±10)	**SE529**	† **Signetics (3622)**
	25 pA	50 pA	200	—	200K	2	36 *	LF111	† National
								LF211	National
	50 pA	25 pA	200 *	30	200K *	5	5, 0 to ±15	LF111	† AMD
								LF211	AMD
5.0	10 μA	2 μA	20	5	3K *	2	(−6, 5 to ±15)	LM361	National
		5 μA	2.2	5	—	—	5, −5.2	**AD9685**	**AD (3357)**
			2.7	5	—	—	5, −5.2	**AD9687**	**AD (3357)**

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Comparators (Cont'd)

Offset Voltage mV (25°C)	Bias Current (25°C)	Offset Current (25°C)	Response Time ns	Max. Differential Voltage	Gain	Fan Out	Supply Voltage, V	Device	Source
Comparators-Single									**(Cont'd)**
5.0									(Cont'd)
	20 μA	3 μA	14 *	5	3K *	4	±5	LM160	† National
								LM260	National
								LM360	National
	25 μA	5 μA	40	5	40K *	10	−3 to -12,12	LM306	National
			40 *	5	1000	1	−6,12	μA710C	Fairchild
								MC1710C	Motorola
								LM710C	National
								μPC71	NEC
								SG710C	SiliconG
	40 μA	5 μA	28 *	5	40K	10	−3 to -12,12	LM306	TI
	75 μA	10 μA	40 *	5	750		−6,12	TL710M	† TI
	150 nA	25 nA	200 *	10	25K	2	±5 to ±15	μA734C	Fairchild
			1300 *	36	200K *		2 to 36	TL331M	† TI
		50 nA	1300 *	36	200K *		2 to 36	TL331C	TI
	200 nA		50000	32	200K *		2	MK404	AnalogSys
	250 nA	50 nA	250 *	15	15K		5-15, ±5-±15	ICL8001C	Intersil
6.0	2 μA	0.75 μA	26	5	5K *		5,(−6,5-±10)	**NE527**	**Signetics (3621)**
	20 μA	5 μA	22	5	5K *		5,(−6,5-±10)	**NE529**	**Signetics (3622)**
	60 μA	7.5 μA	25 *	5	5K *	2	±4.5 to ±6.5	μA760C	Fairchild
								μA760M	† Fairchild
	250 nA	100 nA	250	10	15K		±6 to ±18	AD351J	AD
								AD351K	AD
								AD351S	† AD
7.5	100 μA	15 μA	40 *	5	700		−6,12	TL710C	TI
	250 nA	50 nA	200 *	30	200K *	5	5, 0 to ±15	AD311	AD
								μA311C	Fairchild
								LM311	Intersil
								LM311	Motorola
								LM311	National
								μPC271	NEC
								μPC311	NEC
								LM311	Raytheon
								CA311	RCA (3598)
								LM311	Signetics
								SG311	SiliconG
								TL311M	† TI
								SFC2311	Thomson-CSF
	250 pA	50 pA	165 *	30	200K *	5	5, 0 to ±15	LM211	TI
								LM311	TI
			250	30	200K *	5	5, 0 to ±15	LM311	AMD
		100 pA	—	30	200K *	5	5, 0 to ±15	TL311A	TI
10	75 pA	150 pA	200	—	200K	2	36 *	LF311	National
	150 pA	75 pA	200 *	30	200K *	5	5, 0 to ±15	LF311	AMD
	250 pA	100 pA	—	30	200K *	5	5, 0 to ±15	TL311	TI
20	500 nA	100 nA	1300 *	Vcc	2K	2	2 to 28	LM3302	TI
Comparators-Dual									
2.0	10 μA	1 μA	8	6			−5.2, 5	AM687AM	† AMD
			10	6			−5.2, 5	AM687M	† AMD
	15 μA	3 μA	80	5	12.5K		−6,12	TL514M	† TI
								TL820M	† TI
	20 μA	3 μA	30 *	5	1250	1	−6,12	LM1514	† National
			40 *	5	1250		−6,12	MC1514	† Motorola
	100 nA	25 nA	1300 *	36	50K		2 to 36	μA193A	† Fairchild
								LM193A	† National
								LM193A	† Signetics
		250 nA	50 nA	1300 *	50K		2 to 36	μA293A	Fairchild
								μA393A	Fairchild
	250 nA	50 nA	1300 *	36	50K		2 to 36	LM293A	National
								LM393A	National
3.0	10 μA	1 μA	8	6			−5.2, 5	AM687AL	AMD
			10	6			−5.2, 5	AM687L	AMD
									(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Comparators (Cont'd)

Comparators-Dual (Cont'd)

Offset Voltage mV (25°C)	Bias Current (25°C)	Offset Current (25°C)	Response Time ns	Max. Differential Voltage	Gain	Fan Out	Supply Voltage, V	Device	Source
3.0									(Cont'd)
	45 μA	7 μA	40	5	40K *	10	−3 to -12, 12	TL506M	† TI
	100 nA	10 nA	200 *	30	200K *	5	5, 0 to ± 15	LH211	AMD
								LH2111	† AMD
								LH2211	AMD
								LH2111	† Intersil
								LH2111	† National
								LH2211	National
								LH2111	Raytheon
			250	30	200K *		5, 0 to ± 15	AM1500L	AMD
								AM1500M	† AMD
3.5	20 μA	3 μA	80	5	12.5K		−6, 12	TL811M	† TI
		5 μA	80	5	10K		−6, 12	TL514C	TI
								TL820C	TI
	75 μA	10 μA	40 *	5	700	1	−6, 12	MC1711	† Motorola
					750	1	−6, 12	μA711M	† Fairchild
								LM711	† National
			60	5	750	1	−6, 12	SG711	SiliconG
4.0	0.5 μA	75 nA	80	—	40K	2	± 15	LM119	† National
	500 nA	75 nA	80 *	5	10K	2	5, 0 to ± 15	LM119	† AMD
								LM219	AMD
								LM119	† National
								LM219	National
								LM119	† Signetics
								LM219	Signetics
								TDC0119	† Thomson-CSF
5.0	5 μA *	1 μA	2.7 *	30			−5.2,5	SP9685	Plessey
								SP9687	Plessey
	25 μA	5 μA	30 *	5	1000	1	−6,12	LM1414	National
			40 *	5	1000		−6,12	MC1414	Motorola
	30 μA	5 μA	33 *	5	10K		−6,12	TL811C	TI
	100 nA	25 nA	1300 *	36	50K		2 to 36	μA193	† Fairchild
								LM193	† National
								LM193	† Signetics
								LM193	† TI
								TDC0193	† Thomson-CSF
	100 μA	15 μA	40 *	5	700	1	−6,12	μA711C	Fairchild
								MC1711C	Motorola
								LM711C	National
								SG711C	SiliconG
								μA711C	TI
								SFC2711	Thomson-CSF
	250 nA	50 nA	1300 *	36	50K		2 to 36	μA293	Fairchild
								μA393	Fairchild
								LM293	National
								LM393	National
								LM293	Signetics
								LM293A	Signetics
								LM393A	Signetics
								LM293	TI
								LM393	TI
					200K *	2	2 to 36/ ± 1- ± 18	μPC393	NEC
6.0	30 pA	15 pA	200 *	36	50K	1	4 to 44	**CA3290B**	**RCA (3598)**
6.5	40 pA	7.5 pA	28 *	5	40K *	10	−3 to -12, 12	TL506C	TI
7.0	250 nA	50 nA	1500 *	36	25K		2 to 36	μA2903	Fairchild
								LM2903	National
								LM2903	Signetics
								LM2903	TI
								TDF2903	Thomson-CSF
7.5	20 μA	5 μA	18	6	5K *	10	±5	**NE521**	**Signetics (3620)**
								SE521	**† Signetics (526,3620)**
			25	6	5K *	10	±5	NE522	Signetics
								SE522	† Signetics
	250 nA	50 nA	200 *	30	200K *	5	5, 0 to ± 15	LH2311	AMD

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR

Master Selection Guide

LINEAR–Comparators (Cont'd)

Offset Voltage mV (25°C)	Bias Current (25°C)	Offset Current (25°C)	Response Time ns	Max. Differential Voltage	Gain	Fan Out	Supply Voltage, V	Device	Source
Comparators-Dual									**(Cont'd)**
7.5	250 nA	50 nA	200 *	30	200K *	5	5, 0 to ± 15		(Cont'd)
								LH2311	Intersil
								LH2311	National
			250	30	200K		5, 0 to ± 15	AM1500C	AMD
8.0	1 μA	0.2 μA	80 *	5	8K	2	5, 0 to ± 15	LM319	AMD
								LM319	National
								μPC319	NEC
								LM319	Signetics
	250 nA	25 nA	600 *	40	—	1	4.5 to 40	MC3324A	Motorola
								MC3424A	Motorola
								MC3524A	Motorola
10	40 pA	25 pA	200 *	36	50K	2	4 to 36	**CA3290A**	**RCA** **(3598)**
	100 nA	25 nA	300 *	38	—	1	4.5 to 40	MC3524	† Motorola
	250 nA	50 nA	300 *	38	—	1	4.5 to 40	MC3324	Motorola
								MC3424	Motorola
20	50 pA	30 pA	200 *	36	25K	2	4 to 36	**CA3290**	**RCA** **(3598)**
30	50 pA	100 pA	240	13	20K	1	± 1.5 to ± 7.5	MC14575	Motorola
			250	13	20K	1	± 1.5 to ± 7.5	MC14575	Motorola
Comparators-Quad									
0.8	100 nA	25 nA	1300	36	50K	2	2-36/± 1-± 18	CMP-04B	† PMI
								CMP-04F	PMI
2.0	100 nA	25 nA	1300 *	36	50K	2	2-36/± 1-± 18	LM139A	† AMD
								μA139A	† Fairchild
								LM139A	† Intersil
								LM139A	† Motorola
								LM139A	† National
								PM-139A	† PMI
								CA139A	**† RCA** **(3599)**
								SG139A	† SiliconG
								LM139A	† TI
	250 nA	50 nA	1300 *	36	50K	2	2-36/± 1-± 18	LM239A	AMD
								LM339A	AMD
								μA239A	Fairchild
								μA339A	Fairchild
								LM339A	Intersil
								LM239A	Motorola
								LM339A	Motorola
								LM239A	National
								LM339A	National
								PM-239A	PMI
								PM-339A	PMI
								CA239A	**RCA** **(3599)**
								CA339A	**RCA** **(3599)**
								SG239A	SiliconG
								SG339A	SiliconG
2.0 *	20 μA	1 μA *	55	5	1.2K *	10	± 5	MC3430	Motorola
								MC3431	Motorola
			65	5	1.2K *	10	± 5	MC3432	Motorola
								MC3433	Motorola
2.5	5 nA	0.5 nA	10 ms	36	25K		2 to 36	**L161**	**Siliconix** **(3083)**
3.0	75 nA	25 nA	130 *	15	400K *		5 to ± 15	**HA-4900-2**	**† Harris** **(3457)**
5.0	2.5 nA*	0.5 nA*	8000	36	500K	2	2-36/± 1.5-± 18	LP339	National
	100 nA	25 nA	1300 *	36	200K *	2	2-36/± 1, ± 18	LM139	† AMD
								μA139	† Fairchild
								LM139	† Intersil
								LM139	† Motorola
								LM139	† National
								PM-139	† PMI
								LM139	† Raytheon
								CA139	**† RCA** **(3599)**
								LM139A	**† Signetics** **(526)**
								SG139	† SiliconG
								LM139	† TI
								TDC0139	† Thomson-CSF

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Comparators (Cont'd)

Offset Voltage mV (25°C)	Bias Current (25°C)	Offset Current (25°C)	Response Time ns	Max. Differential Voltage	Gain	Fan Out	Supply Voltage, V	Device	Source
Comparators-Quad									**(Cont'd)**
5.0									(Cont'd)
	150 nA	35 nA	200	15	400K *	—	5 to ± 15	HA-4902-2	† Harris
	250 nA	50 nA	1300 *	15	200K *	1	3-15	MM54C909	† National
								MM74C909	National
				36	200K	1	1 to 18	MB4204	Fujitsu
					200K *	2	2-36/± 1, ± 18	LM239	AMD
								LM339	AMD
								μA239	Fairchild
								μA339	Fairchild
								LM339	Intersil
								LM239	Motorola
								LM339	Motorola
								LM239	National
								LM339	National
								μPC177	NEC
								μPC339	NEC
								AN6912	**Panasonic (3557)**
								PM-239	PMI
								PM-339	PMI
								LM239	Raytheon
								LM339	Raytheon
								CA239	**RCA (3599)**
								CA339	**RCA (3599)**
								LM239A	Signetics
								LM339	Signetics
								SG239	SiliconG
								SG339	SiliconG
								LM239	TI
								LM339	TI
5.0 (2 operational amplifiers, 2 comparators)									
	500 nA	75 nA	1300 *	36	200K *		3-36	MC3505	† Motorola
7.0	250 nA	50 nA	1300 *	36	50K	2	2-36/± 1-± 18	LM2901	Motorola
								LM2901	National
								μPC2901	NEC
								LM2901	Raytheon
								LM2901	Signetics
								LM2901	TI
								TDF2901	Thomson-CSF
7.5	150 nA	50 nA	130 *	15	400K *		5 to ± 15	HA-4905-5	Harris
9.0 (2 operational amplifiers, 2 comparators)									
	10	500 nA	1300 *	36			3-36	MC3405	Motorola
20	500 nA	3 nA *	2000 *	Vcc	2K	1	2 to 28	MC3302	Motorola
								MC3302	Signetics
								SG3302	SiliconG
								TDF3302	Thomson-CSF
		100 nA	1300 *	Vcc	2K	2	5 to ± 15	LM3302	National
30 (2 operational amplifiers, 2 comparators)									
	50 pA	100 pA	250	13	20K	1	± 1.5 to ± 7.5	MC14574	Motorola
Comparators-Hex									
5	100 nA	25 nA	1300	± 36	200K	4	2-36/± 1-± 18	TL336C	TI
	250 nA	25 nA	1300	± 36	200K	4	3-36/± 1-± 18	TL336M	† TI

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR

Master Selection Guide

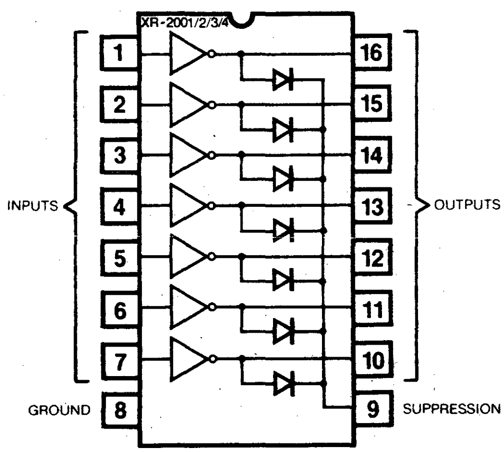
EXAR

High Current Drivers

XR-2001/2002/2003/2004 HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

The XR-2001/2002/2003/2004 are high-voltage, high-current Darlington transistor arrays, consisting of seven silicon npn Darlington pairs on a common monolithic substrate. All units feature open-collector outputs and integral protection diodes for driving inductive loads. Peak inrush currents of up to 600 mA are allowed, making the arrays ideal for driving tungsten filament lamps. The outputs may be paralleled to achieve high-load capability, although each driver has a maximum continuous collector-current rating of 500 mA. The arrays are directly price competitive with discrete transistor alternatives.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Peak Inrush Current Capability of 600 mA
Internal Protection Diodes for Driving Inductive Loads
Excellent Noise Immunity
Direct Compatibility with Most Logic Families
Opposing Pin Configuration Eases Circuit Board Layout

APPLICATIONS

Relay Drive
High-Current Logic Driver

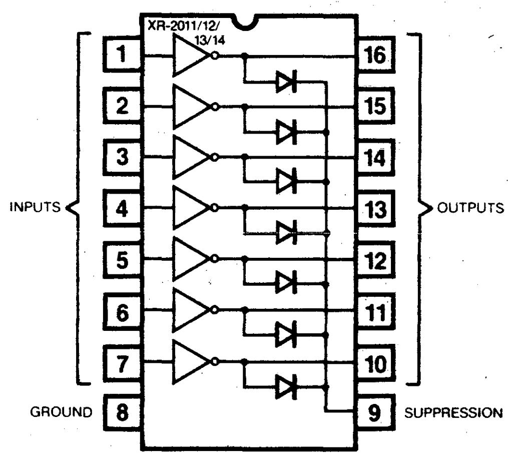
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2001CN	Ceramic	0°C to +70°C
XR-2002CN	Ceramic	0°C to +70°C
XR-2003CN	Ceramic	0°C to +70°C
XR-2004CN	Ceramic	0°C to +70°C

XR-2011/2012/2013/2014 HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

The XR-2011/2012/2013/2014 are high-voltage, high-current Darlington transistor arrays, consisting of seven silicon npn Darlington pairs on a common monolithic substrate. All units feature open-collector outputs and integral protection diodes for driving inductive loads. Peak inrush currents of up to 750 mA are allowed, making the arrays ideal for driving tungsten filament lamps. The outputs may be paralleled to achieve high-load capability, although each driver has a maximum continuous collector-current rating of 600 mA. The arrays are price competitive with discrete transistor alternatives.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Peak Inrush Current Capability of 750 mA
Internal Protection Diodes for Driving Inductive Loads
Excellent Noise Immunity
Direct Compatibility with Most Logic Families
Opposing Pin Configuration Eases Circuit Board Layout

APPLICATIONS

Relay Drive
High-Current Logic Driver

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2011CN	Ceramic	0°C to +70°C
XR-2012CN	Ceramic	0°C to +70°C
XR-2013CN	Ceramic	0°C to +70°C
XR-2014CN	Ceramic	0°C to +70°C

LINEAR

Exar Integrated Systems

EXAR

Full Custom Development

Exar offers a complete design and production capability for full custom IC development, using Exar's bipolar, I^2L, and CMOS technologies. This provides an excellent complement to Exar's unique semi-custom capability.

Exar's full custom IC development and production capabilities offer complete flexibility to meet changing customer needs or design problems. We can develop a complete custom IC starting from your black box specifications, or reduce your working breadboard prototype to a monolithic chip. Alternately, if you have the facilities and resourses to do the IC design and layout, Exar will provide you with the device characteristics and IC layout rules for the particular process suitable to your design, and review your IC layout for you. Then, Exar can generate the IC tooling and fabricate your IC prototypes for you.

WAFER FOUNDARY SERVICE

Exar's bipolar process technology is compatible with the manufacturing processes available from many of the other IC manufacturers. Thus, if you have developed a set of IC tooling with another manufacturer and would like an alternate (or substitute) supplier for your custom IC product, in most cases the existing IC tooling will be directly compatible with Exar's technology.

Exar's Engineering department has two custom IC design groups dedicated to the development of linear and digital custom LSI. We pride ourselves in our flexibility and quick response to your needs.

CONVERTING SEMI-CUSTOM TO FULL CUSTOM

Exar offers the unique ability to start a program using a combination of semi-custom bipolar and/or I^2L, and CMOS arrays, during the early phases of a customer's product, taking full advantage of the low tooling cost and short development cycle. As a customer's product matures, and its market expands, resulting in higher volume production run rates, Exar can convert the multiple semi-custom chip approach into a single custom IC, achieving a cost reduction, and in many cases a performance improvement. The significant advantage of this type of program is that the risk associated with a custom development is greatly reduced; the IC design approach has been proven, production "bugs" are out of your product, and your production line continues to flow during the full custom chip development. Once the custom chip is completely characterized and found acceptable, the semi-custom IC system in your product can be phased-out while the full custom IC is being phased-in.

Exar is the only company that can offer you the advantages of semi-custom and full custom bipolar design programs, because of our complete in-house semiconductor manufacturing capability.

YOUR FIRST STEP

The following technical data package is required in order for Exar to provide you with a firm quotation for your full custom development program:

1. Circuit block diagram with sub-blocks (as necessary).
2. Circuit schematic or logic diagram.
3. Description of circuit operation, and pertinent application information.
4. Preliminary or objective device specification indicating min/max conditions, and limits for the critical parameters (i.e., input/output voltage and current levels, operating frequency, timing diagrams, input/output impedances, power dissipation, etc.).
5. Production requirements and the desired development timetable.

TYPICAL FLOW FOR FULL CUSTOM DEVELOPMENT

TECHNICAL FEASIBILITY AND COST PROPOSAL

CUSTOMER/EXAR INITIAL DESIGN REVIEW

BREADBOARD ANALYSIS

COMPUTER SIMULATION FOR WORST CASE DESIGN ANALYSIS

CUSTOMER/EXAR PROPOSED INTEGRATION DESIGN REVIEW

CHIP ARCHITECTURE DEFINITION

CHIP DIGITIZING

PATTERN GENERATION PHOTOMASKING

PROTOTYPE WAFER FABRICATION

PROTOTYPE ASSEMBLY

PROTOTYPE EVALUATION

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V and V- pins	40V	Maximum Junction Temperature	200°C
Input Voltage	Equal to Supplies	Operating Temperature Range HA-5033-2	-55°C≤TA≤+125°C
Output Current	±200mA	HA-5033-5	0°C≤TA≤+75°C
Internal Power Dissipation (Note 2)		Storage Temperature Range	65°C≤TA≤150°C
TO-8 (+25°C)	1.75W		
Mini-dip (+25°C)	1.95W		

ELECTRICAL CHARACTERISTICS $V_{SUPPLY} = \pm 12V$, $R_S = 50\Omega$, $R_L = 100\Omega$, $C_L = 10pf$, unless otherwise specified.

PARAMETER	TEMP	-55°C TO +125°C			0°C TO +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		5	15		5	15	mV
	Full		7	25		7	25	mV
Average Offset Voltage Drift	Full		33			33		μV/°C
Bias Current	+25°C		10	35		10	35	μA
	Full		20	50		20	50	μA
Input Resistance	+25°C		1.5			1.5		MΩ
Input Capacitance	+25°C		1.6			1.6		pF
Input Noise Voltage(10Hz-10MHz)			20			20		μVp-p
TRANSFER CHARACTERISTICS								
Voltage Gain $R_L = 100\Omega$	+25°C	.93			.93			V/V
$R_L = 1K\Omega$	+25°C		.99			.99		V/V
$R_L = 100\Omega$	Full	.92			.92			V/V
-3db Bandwidth	+25°C		250			250		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing								
$R_L = 100\Omega$	Full		±10			±10		V
$R_L = 1K\Omega$(Note 3)	Full		±11			±11		V
Output Current	+25°C		±100			±100		mA
Output Resistance	+25°C		5			5		Ω
Full Power Bandwidth (Note 4)	+25°C		80			80		MHz
TRANSIENT RESPONSE								
Rise Time	+25°C		3			3		ns
Propagation Delay	+25°C		1			1		ns
Overshoot	+25°C		9			9		%
Slew Rate (Note 3)	+25°C	1.0	1.3		1.0	1.3		V/ns
Settling Time to .1%	+25°C		50			50		ns
Differential Phase Error	+25°C		.1			.1		degrees
Differential Gain Error	+25°C		.1			.1		%
POWER REQUIREMENTS								
Supply Current	+25°C		21	25		21	25	mA
	Full		21	30		21	30	mA
Power Supply Rejection Ratio	Full	54			54			db
Harmonic Distortion	25°C		<0.1			<0.1		%

NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. TO-8 $\theta_{JA} = 99°C/W$. $\theta_{JC} = 31°C/W$; mini-dip $\theta_{JA} = 90°C/W$, $\theta_{JC} = 27°C/W$
3. $V_S = \pm 15V$, $R_L = 1K\Omega$
4. $V_{IN} = 1$ VRMS

LINEAR

Harris Semiconductor

ROM Selection Guide

Commercial: T_A = 0° C to +70° C

Part Number	Organization	Access Time (ns) Max.	Maximum Current (mA) Operating	Maximum Current (mA) Standby	Power Supply (Volts)	Number of Pins	Package Type (Note 1)	Compatible EPROM/PROM
SY3308	1024 x 8	70	120	—	+5	24	C, D, P, K	82S181
SY3308R	1024 x 8	35[3]	130	—	+5	24	C, D, P, K	27S35
SY2316B	2048 x 8	450	98	—	+5	24	C, D, P	2716
SY2316B-2	2048 x 8	200	98	—	+5	24	C, D, P	2716
SY2316B-3	2048 x 8	300	98	—	+5	24	C, D, P	2716
SY3316	2048 x 8	80	120	—	+5	24	C, D, P, K	82S191
SY3316A	2048 x 8	80	120	20	+5	24	C, D, P, K	82S191
SY3316R	2048 x 8	35[3]	130	—	+5	24	C, D, P, K	27S45
SY2332	4096 x 8	450	100	—	+5	24	C, D, P	TMS2532
SY2332-2	4096 x 8	200	100	—	+5	24	C, D, P	TMS2532
SY2332-3	4096 x 8	300	100	—	+5	24	C, D, P	TMS2532
SY2333	4096 x 8	450	100	—	+5	24	C, D, P	2732/A
SY2333-2	4096 x 8	200	100	—	+5	24	C, D, P	2732/A
SY2333-3	4096 x 8	300	100	—	+5	24	C, D, P	2732/A
SY2364	8192 x 8	450	100	—	+5	24	C, D, P	TMS2564
SY2364-2	8192 x 8	200	100	—	+5	24	C, D, P	TMS2564
SY2364-3	8192 x 8	300	100	—	+5	24	C, D, P	TMS2564
SY2364A	8192 x 8	450	100	12	+5	24	C, D, P	TMS2564
SY2364A-2	8192 x 8	200	100	12	+5	24	C, D, P	TMS2564
SY2364A-3	8192 x 8	300	100	12	+5	24	C, D, P	TMS2564
SY2365	8192 x 8	450	100	—	+5	28	C, D, P	2764
SY2365-2	8192 x 8	200	100	—	+5	28	C, D, P	2764
SY2365-3	8192 x 8	300	100	—	+5	28	C, D, P	2764
SY2365A	8192 x 8	450	100	12	+5	28	C, D, P	2764
SY2365A-2	8192 x 8	200	100	12	+5	28	C, D, P	2764
SY2365A-3	8192 x 8	300	100	12	+5	28	C, D, P	2764
SY23128-2	16,384 x 8	200	100	—	+5	28	C, D, P	27128
SY23128-3	16,384 x 8	300	100	—	+5	28	C, D, P	27128
SY23128	16,384 x 8	450	100	—	+5	28	C, D, P	27128
SY23128A-2	16,384 x 8	200	100	10	+5	28	C, D, P	27128
SY23128A-3	16,384 x 8	300	100	10	+5	28	C, D, P	27128
SY23128A	16,384 x 8	450	100	10	+5	28	C, D, P	27128
SY23130	16,384 x 8	450	100	—	+5	28	C, D, P	—
SY23130-2	16,384 x 8	200	100	—	+5	28	C, D, P	—
SY23130-3	16,384 x 8	300	100	—	+5	28	C, D, P	—
SY23130A	16,384 x 8	450	100	10	+5	28	C, D, P	—
SY23130A-2	16,384 x 8	200	100	10	+5	28	C, D, P	—
SY23130A-3	16,384 x 8	300	100	10	+5	28	C, D, P	—
SY23256-2	32,768 x 8	200	100	—	+5	28	C, D, P	27256
SY23256-3	32,768 x 8	300	100	—	+5	28	C, D, P	27256
SY23256	32,768 x 8	450	100	—	+5	28	C, D, P	27256
SY23256A-2	32,768 x 8	200	100	10	+5	28	C, D, P	27256
SY23256A-3	32,768 x 8	300	100	10	+5	28	C, D, P	27256
SY23256A	32,768 x 8	450	100	10	+5	28	C, D, P	27256
SY6364[2]	8192 x 8	200	70	1mA/10μA[4]	+5	24	C, D, P	
SY6365[2]	8192 x 8	200	70	1mA/10μA[4]	+5	28	C, D, P	

NOTES:
1. C = Ceramic, D = Cerdip, P = Plastic, K = Leadless Chip Carrier.
2. Preliminary information.
3. Effective Access Time (t_{CPA}).
4. $\overline{CE}$ @ 2V/$\overline{CE}$ @ V_{CC}.

Synertek

MEMORY

Intersil (Cont)

CO **Englewood**
Kierulff Elctrns., 303-790-4444
CO **Thornton**
Wyle Distribution Grp., 303-424-1985
CO **Wheatridge**
Bell Inds., 303-424-1985
CT **Danbury**
Schweber Elctrns., 203-792-3742
CT **Wallingford**
Arrow Elctrns., 203-265-7741
CT **Wallingford**
Kierulff Electronics, 203-265-1115
FL **Altamonte Springs**
Schweber Elctrns., 305-331-7555
FL **Ft. Lauderdale**
Arrow Elctrns., 305-776-7790
FL **Ft. Lauderdale**
Kierulff Electronics, 305-486-4004
FL **Hollywood**
Schweber Elctrns., 305-921-0301
FL **Palm Bay**
Arrow Elctrns., 305-725-1480
FL **St. Petersburg**
Kierulff Electronics, 813-576-1966
GA **Norcross**
Arrow Elctrns., 404-449-8252
GA **Norcross**
Schweber Elctrns., 404-449-9170
IL **Chicago**
Newark Elctrns., 312-638-4411
IL **Elk Grove Village**
Kierulff Electrns., 312-640-0200
IL **Elk Grove Village**
Schweber Elctrns., 312-364-3774
IL **Schaumburg**
Arrow Elctrns., 312-397-3440
IN **Indianapolis**
Advent Elctrns., Inc., 317-872-4910
IN **Indianapolis**
Arrow Elctrns., 317-243-9353
IA **Cedar Rapids**
Advent Elctrns., 319-395-0197
IA **Cedar Rapids**
Arrow Electronics, 319-373-7230
IA **Cedar Rapids**
Schweber Elctrns., 319-373-1417
KS **Overland Park**
Schweber Electronics, 913-492-2922
MD **Baltimore**
Arrow Elctrns., 301-247-5200
MD **Baltimore**
Kierulff Electronics, 301-247-5020
MD **Gaithersburg**
Schweber Elctrns., 301-840-5900
MA **Bedford**
Schweber Elctrns., 617-275-5100
MA **Billerica**
Kierulff Elctrns., 617-667-8331
MA **Woburn**
Arrow Elctrns., 617-933-8130
MI **Ann Arbor**
Arrow Elctrns., 313-971-8220
MI **Grand Rapids**
Arrow Electronics, 616-243-0912
MI **Livonia**
Schweber Elctrns., 313-525-8100
MN **Eden Prairie**
Schweber Elctrns., 612-941-5280
MN **Edina**
Arrow Elctrns., 612-830-1819
MN **Edina**
Kierulff Elctrns., 612-941-7500
MO **Earth City**
Schweber Electronics, 314-739-0526
MO **Kansas City**
LCOMP, 816-221-2400
MO **Maryland Heights**
LCOMP, 314-291-6200
MO **St. Louis**
Arrow Elctrns., 314-567-6888
NH **Manchester**
Arrow Elctrns., 603-668-6968
NH **Manchester**
Schweber Electronics, 603-625-2250
NJ **Ezesham**
Arrow Elctrns., 609-596-8000
NJ **Fairfield**
Arrow Elctrns., 201-575-5300
NJ **Fairfield**
Schweber Elctrns., 201-227-7880
NM **Albuquerque**
Alliance Elctrns., Inc., 505-292-3360
NM **Albuquerque**
Arrow Elctrns., 505-243-4566
NM **Albuquerque**
Bell Inds., Century Elctrns. Div., 505-292-2700
NY **Binghamton**
Pioneer Harvey Elec., 607-748-8211
NY **Buffalo**
Summit Distrs., Inc., 716-887-2800
NY **Fairport**
Pioneer Harvey Elec., 716-381-7070
NY **Hauppauge**
Arrow Elctrns., 516-231-1000
NY **Liverpool**
Arrow Elctrns., 315-652-1000
NY **Melville**
Arrow Elctrns., 516-391-1609
NY **Rochester**
Arrow Elctrns., 716-275-0300
NY **Rochester**
Schweber Elctrns., 716-424-2222
NY **Westbury**
Schweber Elctrns., 516-334-7474
NC **Raleigh**
Arrow Elctrns., 919-876-3132
NC **Raleigh**
RESCO, 919-781-5700
NC **Raleigh**
Schweber Electronics, 919-876-0000
NC **Winston-Salem**
Arrow Elctrns., 919-725-8711
OH **Beachwood**
Schweber Elctrns., 216-464-2970
OH **Bedford Heights**
Kierulff Electronics, 216-587-6558
OH **Centerville**
Arrow Elctrns., 513-435-5563
OH **Centerville**
Schweber Electronics, 513-439-1800
OH **Solon**
Arrow Elctrns., 216-248-3990
OK **Tulsa**
Arrow Electronics, 918-665-7700
OK **Tulsa**
Kierulff Electronics, 918-252-7537
OK **Tulsa**
Schweber Electronics, 918-622-8000
OR **Hillsboro**
Wyle Distribution, 503-640-6000
OR **Lake Oswego**
Moore Electronics, Inc., 503-684-3131
OR **Portland**
Kierulff Elctrns., 503-641-9150
PA **Horsham**
Schweber Elctrns., 215-441-0600
PA **Monroeville**
Arrow Elctrns., 412-856-7000
PA **Pittsburgh**
Schweber Elctrns., 412-782-1600
TX **Austin**
Arrow Elctrns., 512-835-4180
TX **Austin**
Kierulff Electronics, 512-835-2090
TX **Austin**
Schweber Electronics, 512-458-8253
TX **Dallas**
Arrow Elctrns., 214-386-7500
TX **Dallas**
Kierulff Electronics, 214-343-2400
TX **Dallas**
Schweber Elctrns., 214-661-5010
TX **Houston**
Arrow Elctrns., 713-530-4700
TX **Houston**
Kierulff Electronics, 713-530-7030
TX **Houston**
Schweber Elctrns., 713-784-3600
UT **Salt Lake City**
Bell Inds. Century Elctrns. Div., 801-972-6969
UT **Salt Lake City**
Kierulff Elctrns., 801-973-6913
UT **Salt Lake City**
Wyle Distribution Group, 801-974-9953
VA **Richmond**
Arrow Electronics, 804-282-0413
WA **Bellevue**
Wyle Distribution Grp., 206-453-8300
WA **Tukwila**
Kierulff Elctrns., 206-575-4420
WI **Brookfield**
Schweber Elctrns., 414-784-9020
WI **Oak Creek**
Arrow Elctrns., 414-764-6600
WI **Waukesha**
Kierulff Elctrns., 414-784-8160
Can **Brampton, Ontario**
Zentronics, 416-451-9600
Can **Burnaby, British Columbia**
R.A.E. Ind. Elect. Ltd., 604-291-8866
Can **Calgary, Alberta**
Cardinal Elctrns., 403-259-6817
Can **Calgary, Alberta**
Zentronics, 403-272-1021
Can **Downsview, Ontario**
CESCO, 416-661-0220
Can **Edmonton, Alberta**
Cardinal Elctrns., 403-483-6266
Can **Edmonton, Alberta**
RAE Ind. Elec., 403-451-4001
Can **Montreal, Quebec**
CESCO, 514-735-5511
Can **Nepean, Ontario**
Cesco, 613-226-6903
Can **Nepean, Ontario**
Zentronics Ltd., 613-226-8840
Can **Quebec City, Quebec**
CESCO, 418-687-4231
Can **Richmond, British Columbia**
Zentronics, 604-273-5575
Can **St. Laurent, Quebec**
Zentronics, 514-735-5361
Can **Waterloo, Ontario**
Zentronics Ltd., 519-884-5700
Can **Winnipeg, Manitoba**
Zentronics Ltd., 204-775-8661
Intl **Australia, Burwood-Victoria**
R & D Electronics Pty. Ltd., TEL: 288-8232
Intl **Australia, Crows Nest-NSW**
R & D Electronics Pty. Ltd., TEL: 439-5488
Intl **Austria, Vienna**
Transistor Vertriebs GmbH, TEL: (02 22) 82 94 51
Intl **Belgium, Brussels**
Simac Elctrns. SPRL, TEL: 02-2192453
Intl **Denmark, Copenhagen**
E. V. Johanssen Electronik A-S, TEL: 45-1-839022
Intl **Finland, Espoo**
Nabla Elektronikka Oy, TEL: 90-46 28 29
Intl **France, Antony**
C.C.I., TEL: (1) 666.21.82
Intl **France, Sevres**
Tekelec-Airtronic, TEL: (1) 534.75.35
Intl **Hong Kong, Kowloon**
Conmos Prods. Ltd., TEL: 3-7560103-8
Intl **Hong Kong, Kowloon**
Electocon Products Ltd., TEL: 3-687214-6
Intl **India, Bombay**
Zenith Elctrns., TEL: 384214

LINEAR-Consumer Circuits

Function	Device	Source
Audio Circuits		
Amplifier and Preamplifier, Low Power		
	TCA210	Signetics
Amplifier, Headphone		
	LA4170	Sanyo
	LA4175	Sanyo
	LA4177	Sanyo
Amplifier, Hearing Aid		
	CS263	Cherry
	TCA1003	ITT
	TCA1004	ITT
	MPS5003	MicroPwr
	MPS5004	MicroPwr
	MPS5053	MicroPwr
	OM200	Panasonic
Amplifier, with AGC, for Recorders		
	HA1319	Hitachi
	HA1361	Hitachi
	TDA7137	Toshiba
	TDA7137-ST	Toshiba
Attenuator, Digital		
	AD7115K	**AD (2827)**
Attenuator, Digital (logarithmic D/A converter)		
	AD7111K	**AD (2827)**
	AD7111L	**AD (2827)**
	AD7111T	**† AD (2827)**
	AD7111U	**† AD (2827)**
	AD7118T	**† AD (2827,2829)**
	AD7118U	**† AD (2827,2829)**
Attenuator, Digital (with loudness compensation switch), 0 to 88.5 dB Attenuation in 1.5 dB Steps		
	AD7110K	**AD (2827,2829)**
	AD7118K	**AD (2827,2829)**
	AD7118L	**AD (2827,2829)**
Attenuator, Dual		
	LA2600	Sanyo
	LC7500	Sanyo
Audio Noise Reduction, Compander. See Linear-Telecommunications Circuits		
Controls (loudness, treble, bass)		
	TDA4290-5	Siemens
Controls, Stereo, DC Operated		
	LM1035	National
	TCA730A	Signetics
	TCA740A	Signetics
	TDA1074A	Signetics
	TDA1524	Signetics
Digital Audio ADC		
	PCM75	**Burr-Brown (2849)**
Digital Audio DAC		
	PCM501	Burr-Brown
	PCM52	**Burr-Brown (2849)**
	PCM53	**Burr-Brown (2849)**
Digital Compact Disc		
	SAA7000	Signetics
	SAA7010	Signetics
	SAA7020	Signetics
Digital Compact Disc, Filter Circuit		
	SAA7030	Signetics
Digital Noise Source		
	MM5437	National
Distortion Suppressor		
	MP201A	Analogic
Equalizer, Switchable		
	TDA2000	Siemens
Muting Circuit (switching noise suppressor)		
	TA7324	Toshiba
Noise reduction, DNR		
	LM832	National
Noise Reduction, Dolby		
	HA11226	Hitachi
	LM1111	National
	LM1121A	National
	LM1121B	National
	LM1121C	National
	LM1131A	National
	LM1131B	National
	LM1131C	National
	LM1894	National
	NE645	Signetics
	NE646	Signetics
	NE648	Signetics
	NE649	Signetics
	NE650	Signetics
	NE651	Signetics
	NE652	Signetics
	NE653	Signetics
	NE654	Signetics
	NE660	Signetics
Noise Reduction, Dual Dolby B-Type		
	NE657	Signetics
Pop Noise Canceller		
	AN6135	Panasonic
Power Amplifier Driver		
	ICL8063C	Intersil
	ICL8063M	† Intersil
	MC3221	Motorola
	MC3320	Motorola
	MC3321	Motorola
	LM391	National
Power Amplifier Driver, Dual		
	STK3042	Sanyo
	STK3062	Sanyo
	STK3082	Sanyo
Power Amplifier, Single, <5 Watts		
	TBA641	Fairchild
	TBA820	Fairchild
	HA1325	Hitachi
	HA1329	Hitachi
	MC1454	Motorola
	MC1554	† Motorola
	LM1879	National
	LM2001	National
	LM2895	National
	LM380	National
	LM386	National
	LM388	National
	LM389	National
	LM390	National
	AN214	Panasonic
	AN374	Panasonic
	AN7110	Panasonic
	AN7114	Panasonic
	AN7115	Panasonic
	AN7120	Panasonic
	AN7130	Panasonic
	CA3020	† RCA
	LA4100	Sanyo
	LA4101	Sanyo
	LA4102	Sanyo
	LA4110	Sanyo
	LA4112	Sanyo
	LA4126	Sanyo
	LA4137	Sanyo
	LA4138	Sanyo
	LA4180	Sanyo
	LA4182	Sanyo
	LA4200	Sanyo
	LA4201	Sanyo
(Continued)		
Power Amplifier, Single, <5 Watts (Cont'd)		
	LA4220	Sanyo
	LA4430	Sanyo
	TBA820	SGS
	TBA820M	SGS
	TCA830S	SGS
	TDA1013A	Signetics
	TDA1015	Signetics
	ULN-2280B	Sprague
	ULN-2283B	Sprague
	ULN-3705M	Sprague
	TCA830	Telefunken
	U410	Telefunken
	U411	Telefunken
	LM388-3	TI
	SN16923	TI
	SN76000	TI
	SN76002	TI
	SN76011	TI
	SN76021	TI
	SN76024	TI
	TA7140	Toshiba
	TA7207	Toshiba
	TA7208	Toshiba
	CA3094	**† RCA (3598)**
Power Amplifier, Single, 5-10 Watts		
	HA1366	Hitachi
	HA1368	Hitachi
	HA1371	Hitachi
	HA1372	Hitachi
	HA1389	Hitachi
	TBA800	Hitachi
	TBA810	Hitachi
	TDA2002	Hitachi
	TDA2002	Motorola
	TDA2002A	Motorola
	LM2002	National
	LM383	National
	LM383A	National
	LM384	National
	TDA2002	National
	TDA2002A	National
	TDA2003	National
	CA2002	RCA
	CA3131	RCA
	CA3132	RCA
	LA4140	Sanyo
	LA4230	Sanyo
	LA4250	Sanyo
	LA4420	Sanyo
	LA4422	Sanyo
	LA4440	Sanyo
	STK4017	Sanyo
	STK4019	Sanyo
	STK4332	Sanyo
	STK4352	Sanyo
	STK4362	Sanyo
	L149	SGS
	TBA800	SGS
	TBA810	SGS
	TCA940E	SGS
	TDA1905	SGS
	TDA1908	SGS
	TDA1910	SGS
	TDA2002	SGS
	TDA2002A	SGS
	TDA2003	SGS
	TDA2006	SGS
	TDA1037	Siemens
	TDA2003	Siemens
	TDA1020	Signetics
	TDA2002	Sprague
	TDA2002A	Sprague
(Continued)		

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Consumer Circuits (Cont'd)

Audio Circuits (Cont'd)

Function	Device	Source
Power Amplifier, Single, 5-10 Watts (Cont'd)		
	TDA2003	Sprague
	ULN-3701Z	Sprague
	ULN-3702Z	Sprague
	ULN-3703Z	Sprague
	ULN-3784B	Sprague
	ULX-3704B	Sprague
	TBA800	Telefunken
	TBA810	Telefunken
	TDA2002	Telefunken
	TDA2002A	Telefunken
	TDA2003	Telefunken
	TDA2004	Telefunken
	SN76005	TI
	TA7205A	Toshiba
	TA7217A	Toshiba
	TA7222A	Toshiba
	TA7238	Toshiba
Power Amplifier, Single, >10 Watts		
	μA7332	Fairchild
	MB3720	Fujitsu
	MB3730	Fujitsu
	MB3731	Fujitsu
	HA1388	Hitachi
	HA1392	Hitachi
	LM1875	National
	LM2005	National
	CA2004	RCA
	LA4460	Sanyo
	LA4461	Sanyo
	STK0030	Sanyo
	STK0040	Sanyo
	STK0050	Sanyo
	STK0055	Sanyo
	STK0059	Sanyo
	STK0060	Sanyo
	STK0070	Sanyo
	STK0080	Sanyo
	STK0150	Sanyo
	STK050	Sanyo
	STK058	Sanyo
	STK070	Sanyo
	STK075	Sanyo
	STK077	Sanyo
	STK078	Sanyo
	STK080	Sanyo
	STK082	Sanyo
	STK083	Sanyo
	STK084	Sanyo
	STK086	Sanyo
	STK4021	Sanyo
	STK4023	Sanyo
	STK4025	Sanyo
	STK4372	Sanyo
	STK4392	Sanyo
	TCA940	SGS
	TDA2008	SGS
	TDA2010	SGS
	TDA2020	SGS
	TDA2020D	SGS
	TDA2030	SGS
	TDA2040	SGS
	TDA2030	Siemens
	TDA3000	Siemens
	TDA1512	Signetics
	TDA1520	Signetics
	TDA2008	Sprague
	TDA2030	Telefunken
	TA7210	Toshiba
Power Amplifier, Dual, <5 Watts		
	HA1374	Hitachi
	LM1877	National
	LM1895	National
	LM1896	National
	LM2877	National
	LM2896	National
	LM377	National
	LM378	National
	AN7145L	Panasonic
	AN7146M	Panasonic
	LA4120	Sanyo
	LA4125	Sanyo
	LA4125T	Sanyo
	ULX-3783M	Sprague
	TA7203	Toshiba
	TA7214	Toshiba
	TA7215	Toshiba
Power Amplifier, Dual, 5-10 Watts		
	HA1377	Hitachi
	LM2878	National
	LM2879	National
	LM379	National
	AN7145M	Panasonic
	AN7156	Panasonic
	STK433	Sanyo
	STK435	Sanyo
	STK443	Sanyo
	STK457	Sanyo
	STK459	Sanyo
	STK463	Sanyo
	STK465	Sanyo
	TDA2004	SGS
	TDA2005	SGS
	TDA1510	Signetics
	TDA1515	Signetics
	TDA2005	Telefunken
	TA7227	Toshiba
Power Amplifier, Dual, >10 Watts		
	AN7145H	Panasonic
	AN7146H	Panasonic
	AN7156N	Panasonic
	STK437	Sanyo
	STK439	Sanyo
	STK441	Sanyo
Preamplifier	MA106	AnalogSys
	ZN459	† Ferranti
	ZN459C	Ferranti
	ZN459CP	Ferranti
	ZN460	† Ferranti
	ZN460C	Ferranti
	ZN460CP	Ferranti
	HA12017	Hitachi
	HA1406	Hitachi
	HA1457	Hitachi
	LM1837	National
	LM3080	National
	LM3080A	National
	μPC1023	NEC
	μPC1024	NEC
	μPC1032	NEC
	μPC566	NEC
	μPC592	NEC
	AN360	Panasonic
	AN370	Panasonic
	SL561	Plessey
	SL561B	Plessey
	SL561C	Plessey
	LA3110	Sanyo
	LA3120	Sanyo
	LA3130	Sanyo
	LA3150	Sanyo
	LA3170	Sanyo
(Continued)		
Preamplifier (Cont'd)		
	TDA2310	SGS
	TDA3410	SGS
	TDA3420	SGS
	TA7063	Toshiba
	TA7120	Toshiba
	TA7122A	Toshiba
	TA7122B	Toshiba
	TA7129	Toshiba
	TA7129A	Toshiba
	TA7136A	Toshiba
	TA7322	Toshiba
	CA3080	**RCA (3598)**
	CA3080A	† **RCA (3598)**
Preamplifier, Dual		
	XR4739	Exar
	XR4739M	† **Exar (3378)**
	UA739	Fairchild
	μA739	Fairchild
	μA749	† Fairchild
	HA12012	Hitachi
	HA1452W	Hitachi
	LM1301	National
	LM1303	National
	LM1897	National
	LM381	National
	LM382	National
	LM387	National
	AN7311	Panasonic
	LA3115	Sanyo
	LA3122	Sanyo
	LA3133	Sanyo
	LA3155	Sanyo
	LA3160	Sanyo
	LA3161	Sanyo
	TDA2320A	SGS
	NE542	Signetics
	TDA1522	Signetics
	SN76130	TI
	SN76131	TI
	SN76149	TI
	TA7312	Toshiba
	TA7325	Toshiba
	TA7685	Toshiba
Preamplifier, Quad		
	XR4212	**Exar (3378)**
Signal Delay	**MN3001**	**Panasonic (3559)**
	MN3010	**Panasonic (3559)**
	MN3204	Panasonic
	MN3207	Panasonic
Sound Generator		
	AY3-8910	GI
	AY3-8912	GI
Sound Generator Controller for Microprocessor-Based Systems	SN76489	TI
	SN76489A	TI
	SN76493	TI
	SN76494	TI
	SN76495	TI
Sound Generator w/Audio Amp		
	SN76487	TI
	SN76488	TI
Voltage Controlled Oscillator for Electronic Music		
	SSM2038	SSM
Dual DC Operated Tone/Volume/Balance Circuit		
	LM1036	National
Dual DC Operated Tone/Volume/Balance Circuit with Stereo Enhancement		
	LM1040	National

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR

Master Selection Guide

LINEAR–Consumer Circuits (Cont'd)

Automotive Circuits

Function	Device	Source
Automotive Lamp Monitor	ULN-2435A	Sprague
	ULN-2445A	Sprague
	ULN-2455A	Sprague
Clock	PCF1171	Signetics
	PCF1172	Signetics
Clock with Vacuum Fluorescent Display Drivers	S4003	AMI
	SCL5233	SSS
High Energy Ignition Circuit	MC3334	Motorola
Ignition Circuit	MC3333	Motorola
Injector Drive Controller	LM1949	National
Lamp Monitor	ULN-2401A	Sprague
Low Coolant Detector	ULN-2429A	Sprague
Solenoid Driver	MC3484V2	Motorola
	MC3484V4	Motorola
Speed Control Processor	MC14460	Motorola
Speedometer and Mileage Indicator	SAY115	ITT
Traffic Information Broadcast Decoders	UAA1009	ITT
	S0280	Siemens
	S0281	Siemens
	S551	Siemens
	S552	Siemens
Voltage Regulator	TCA700	ITT
	MC3325	Motorola
20-Watt Automotive Power Amplifier	LM2005	National

Calculator Circuits

Function	Device	Source
Calculator	MN5750	Panasonic
	TMS1018	TI
Calculator, Printing	HD38510	Hitachi
	HD38513	Hitachi
	HD38546	Hitachi
	HD38550	Hitachi
	HD38560	Hitachi
	HD38570	Hitachi
	HD38580	Hitachi
	HD38585	Hitachi

Camera Circuits

Function	Device	Source
Exposure Control	CS100	Cherry
	CS102	Cherry
	CS122	Cherry
	CS127	Cherry
	CS129	Cherry
	CS130	Cherry
	CS131	Cherry
	CS132	Cherry
	CS137	Cherry
	CS460	Cherry
	CS461	Cherry
	CS462	Cherry
	CS463	Cherry
	CS464	Cherry
	CS470	Cherry
	CS480	Cherry
	CS481	Cherry
	CS482	Cherry

(Continued)

Function	Device	Source
Exposure Control (Cont'd)	CS483	Cherry
	CS484	Cherry
	CS485	Cherry
	CS486	Cherry
	CS487	Cherry
	CS488	Cherry
	CS489	Cherry
	CS580	Cherry
	S0258A	Siemens
	S0289	Siemens
Strobe Light Controller	CS139	Cherry

CB Radio Circuits

Function	Device	Source
Channel Selector/Display Driver	FCB8010	Fairchild
	MN6080	Panasonic
	LC7181	Sanyo
	LC7184	Sanyo
	LC7191	Sanyo
Programmer, for PLL	MP7156	MicroPwr
	LC7120	Sanyo
Synthesizer Set, 40 Channel, BCD Channel Setting	MP7189	MicroPwr
Synthesizer Set, 40 Channel, BCD Channel Setting	LC7131	Sanyo
	LC7135	Sanyo
Transceiver Receiver	TMS1022	TI

Clock/Watch Circuits

Function	Device	Source
Alarm Clock	HD38980	Hitachi
	HD38991C	Hitachi
	HD43115	Hitachi
	HD43890	Hitachi
	ICM1115	Intersil
	ICM1115A	Intersil
	ICM1115B	Intersil
	ICM7038A	Intersil
	ICM7038B	Intersil
	ICM7049A	Intersil
	ICM7050	Intersil
	MM53108	National
	MM5316	National
	MM5387	National
	MM5402	National
	MM5405	National
	MM58143	National
	MM58144	National
	µPD5388	NEC
	µPD833	NEC
	MN6076	Panasonic
	MN6092	Panasonic
	LM8360	Sanyo
	LM8361	Sanyo
	MB561	Signetics
	MB562	Signetics
Alarm Clock Radio	ICM7223	Intersil
	ICM7223A	Intersil
	ICM7223VF	Intersil
	MM53113	National
	MM53124	National
	MM5455	National
	MM5456	National
	MM5457	National
	MM5462	National
	MM5463	National
	MM5464	National

(Continued)

Function	Device	Source
Alarm Clock Radio (Cont'd)	MM5465	National
	MM5466	National
	MSM5524	**OKI (4118)**
	LM8363	Sanyo
	LM8364	Sanyo
Automotive Clock with LCD Display Drivers	PCF1171	Signetics
	PCF1172	Signetics
Clock Automotive, with Vacuum Fluorescent Display Drivers	S2709	AMI
	MSM5557	**OKI (4118)**
	SCL5458	SSS
Clock Circuits (See Also: Digital—CMOS Oscillators/Dividers. Linear—Other Linear Devices—Oscillator)	**S4003**	**AMI (705)**
	HD44010	Hitachi
	ICM7045	Intersil
	ICM7051A	Intersil
	ICM7051B	Intersil
	ICM7052	Intersil
	SAJ300	ITT
	C1200	LSIComp
	MM5309	National
	MM5311	National
	MM53110	National
	MM5312	National
	MM5313	National
	MM5314	National
	MM5315	National
	MM5318	National
	MM5378	National
	MSM5509	**OKI (4118)**
	MSM5528	**OKI (4118)**
	MSM5529	OKI
	MSM5558	**OKI (4118)**
	MN6057	Panasonic
	MN6059	Panasonic
	MN6093	Panasonic
	MN6200	Panasonic
	MN6251	Panasonic
	MN6252	Panasonic
	CD22012	RCA
	CD22014	RCA
	8640	SMOS
	8650	SMOS
	8651	SMOS
	SAF3019	Signetics
	SCL5233	SSS
	SCL5238	SSS
	SCL5455	SSS
	SCL5463	SSS
	SCL5474	SSS
	SCL5601	SSS
	WD2412	Western
Color Bar Generator	MM5322	National
Color Control for VIR Broadcasts	HA11409	Hitachi
Digital Clock, Channel and Time Display	MM58106	National
Digital Tuner	MM58142	National
Melody Circuit, for Clocks	7910	SMOS
	7920	SMOS
	7930	SMOS
	SVM7940	SMOS
	SVM7950	SMOS
	SVM7960	SMOS
	SVM7970	SMOS
	SVM7990	SMOS

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Consumer Circuits (Cont'd)

Function	Device	Source
Clock/Watch Circuits (Cont'd)		
Melody Circuit, Westminister Chime	SVM5530	SMOS
	SVM7810	SMOS
Stopwatch/Clock (LCD)	ICM7045	Intersil
	WD2412	Western
Stopwatch (LED)	ICM7205	Intersil
	ICM7215	Intersil
Watch, Analog (See also Digital—CMOS Oscillators/Dividers)	HC43850	Hitachi
	ICM7047	Intersil
	ICM7245	Intersil
Watch (LCD), Digital	HC42022	Hitachi
	HC42030	Hitachi
	HC43032	Hitachi
	HC43802	Hitachi
	HC43803	Hitachi
	ICM1424B	Intersil
	ICM1424MB	Intersil
	ICM1424MC	Intersil
	ICM7210	Intersil
	ICM7210C	Intersil
	ICM7210M	Intersil
	ICM7210MC	Intersil
	ICM7220	Intersil
	ICM7220B	Intersil
	ICM7220M	Intersil
	ICM7220MA	Intersil
	ICM7220MC	Intersil
	ICM7269	Intersil
	ICM7270	Intersil
	ICM7272	Intersil
	MSM5803	**OKI** (4118)
	MS680	RTC
	MS681	RTC
	MS682	RTC
	MS683	RTC
	LC5621	Sanyo
	PCA1122	Signetics
	SCL54301	SSS
	SCL5482	SSS
	SCL5483	SSS
Watch (LCD), Digital Chronograph	ICM7220C	Intersil
	MP7160	MicroPwr
	LC5613	Sanyo
Watch (LCD), Digital Chronograph/Alarm	HI7000	Holt
	MP7216	MicroPwr
Watch (LCD), Digital with Alarm	HI7020	Holt
	ICM7220A	Intersil
	ICM7220FA	Intersil
	ICM7220MFA	Intersil
	ICM7221	Intersil
	ICM7222	Intersil
	MP7150	MicroPwr
Watch (LCD), Digital with Alarm and Music Enable	ICM7271	Intersil
	ICM7273	Intersil
Watch (LED), Digital	ICM7214	Intersil
	ICM7214A	Intersil
Organ Circuits		
Delay Circuit, See also Analog Shift Registers and Serial Analog Delay under Linear-Other Devices.	TDA1022	Signetics
Digital Accompaniment Interface	M109	SGS
Electronic Attenuator	XR13600	Exar
	MC3340	Motorola
	CA3080	RCA
	CA3080A	† RCA
Frequency Divider, 6-Stage	S10131	AMI
	LM3216	Sanyo
Frequency Divider, 7-Stage	M738	SGS
	M740	SGS
	M741	SGS
	M747	SGS
	SAJ410	Siemens
Frequency Divider, 8-Stage, with Staircase Generator	MN6004	Panasonic
Frequency Generator. See also Organ, Top Octave Generator	MN6005	Panasonic
Key Divider	S10430	AMI
Monophonic Synthesizer	M110	SGS
Noise Generator	S2688	AMI
	MM5837	National
Rhythm Circuit	S2567	AMI
	LM8372	Sanyo
	LM8471	Sanyo
	LM8972	Sanyo
	M258	SGS
	M259	SGS
	M268	SGS
	M269	SGS
Solo and Accompaniment	M108	SGS
Tone Generator	M082	SGS
	M082AA	SGS
	M083	SGS
	M083AA	SGS
	M086	SGS
	M086AA	SGS
Top Octave Generator	S50240	AMI
	S50241	AMI
	S50242	AMI
	MK50240	Mostek
	MK50241	Mostek
	MK50242	Mostek
	LM8071	Sanyo
Toy Organ	SAA1900	ITT
Dual Voltage Controlled Amplifier	SSM2020	SSM
	SSM2022	SSM
Radio Circuits, AM		
AM/SW Tuner	5054	Siemens
Amplifier with Demodulator and Volume Control	TDA1048	Siemens
CQUAM AM Stereo Decoder	MC13020	Motorola
Frequency Synthesizer	TC9131	Toshiba
Mixer, IF, AGC	ULN-2243A	Sprague
Radio System for Electronically Tuned Radios	LM1863	National
Receiver System	HA1151	Hitachi
	HA1197	Hitachi
	HA1199	Hitachi
	μPC1215V	NEC
	CA3088	† RCA
	CA3123	† RCA
	TCA440	Siemens
	TDA1046	Siemens
	TDA1072	Signetics
	TEA5550	Signetics
	ULN-2249A	Sprague
	ULN-3838A	Sprague
	TDA1072	Telefunken
	SN76635	TI
	TA7306	Toshiba
	TA7615	Toshiba
RF, IF Detector	LM3820	National
RF, IF, Detector, AGC	ZN414	Ferranti
SSB Detector	SL623C	Plessey
Stereo Decoder	LM1981	National
Stereo Demodulator	HS3604	Harris
Tuner for Car Radio	TA7402	Toshiba
	TA7616	Toshiba
Tuner System	LA1130	Sanyo
	LA1240	Sanyo
	LA1245	Sanyo
Radio Circuits, AM/FM		
AM/FM Phase and Signal Locked Loop (PSL[2]) Tuner	LC7210	Sanyo
AM/FM PLL Synthesizer Tuner	LC7220	Sanyo
	LC7225	Sanyo
AM/FM/SW Frequency Counter	MSM5526	OKI
Display Driver for Receiving Frequency Digital Display	TD6301A	Toshiba
FM/SW/MW/LW Frequency Display	LC7253	Sanyo
	LC7257	Sanyo
	LC7258	Sanyo
Frequency Counter	**MSM5525**	**OKI** (4118)
IF Amplifier	μA757	Fairchild
	LM1821	National
	LM1868	National
	μPC577	NEC
	AN7218	Panasonic
	AN7266	Panasonic
	LA1201	Sanyo
	TAA991	Siemens
Radio Frequency Display	MM5430	National
	MM5431	National
Radio Frequency Display Driver and Clock	HA12404	Hitachi
	HA12405	Hitachi
	T1400	Toshiba
Receiver System	HA11211	Hitachi
	HA11251	Hitachi
	HA12402	Hitachi

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR

Master Selection Guide

LINEAR–Consumer Circuits (Cont'd)

Radio Circuits, AM/FM (Cont'd)

Function	Device	Source	
Receiver System (Cont'd)	LM1866	National	
	AN217P	Panasonic	
	AN253	Panasonic	
	AN366	Panasonic	
	LA1210	Sanyo	
	TDA1220A	SGS	
	TEA5570	Signetics	
	TDA1083	Sprague	
	TDA1090	Sprague	
	ULN-2204A	Sprague	
	ULN-2240A	Sprague	
	ULN-2241A	Sprague	
	ULN-2242A	Sprague	
	ULX-3840A	Sprague	
	TDA1083	Telefunken	
	U416	Telefunken	
	U417	Telefunken	
	U418	Telefunken	
	TA7613	Toshiba	
	TA7614	Toshiba	
Search Tuning	TDA 1580	Signetics	
Signal Processor	ULX-3804A	Sprague	
Synthesizer (FM prescaler, preamplifier and reference oscillator)	AC5945	TI	
Tuner Control	LC7200	Sanyo	
	LC7201	Sanyo	
	LC7203	Sanyo	
	LC7207	Sanyo	
Tuner, Radio Frequency Display and Clock	LC7250	Sanyo	
TV Synthesizer	SAA1057	Signetics	

Radio Circuits, FM

Detector. See Linear-Phase Locked Loop Circuits and IF Amplifier/Detector below.

Function	Device	Source	
Front End	AN7213	Panasonic	
	TDA1571	Signetics	
	TDA1574	Signetics	
Front End Timer	TDA1094	Telefunken	
	TA7335	Toshiba	
IF Amplifier	HA1201	Hitachi	
	HA1211	Hitachi	
	MC1350	Motorola	
	AN278	Panasonic	
	AN377	Panasonic	
	CA3002	† RCA	
	CA3005	**† RCA**	**(3603)**
	CA3006	**† RCA**	**(3603)**
	CA3012	† RCA	
	CA3028	**† RCA**	**(3603)**
	CA3076	† RCA	
	LA1111	Sanyo	
	LA1222	Sanyo	
	TDA4200	Siemens	
	TDA1576	Signetics	
	TEA5560	Signetics	
	ULN-2243A	Sprague	
	SN76676	TI	
	SN76678	TI	
	TA7302	Toshiba	
	TA7303	Toshiba	
IF Amplifier/Detector	HA11225	Hitachi	
	HA1137	Hitachi	
	HA12411	Hitachi	
	LM1865	National	

(Continued)

Function	Device	Source	
IF Amplifier/Detector (Cont'd)	LM3011	National	
	LM3075	National	
	LM3089	National	
	LM3189	National	
	TBA120	National	
	μPC1028	NEC	
	TBA120	Plessey	
	TBA750	Plessey	
	CA2111A	† RCA	
	CA3013	RCA	
	CA3014	† RCA	
	CA3042	RCA	
	CA3065	RCA	
	CA3075	† RCA	
	CA3089	† RCA	
	CA3189	RCA	
	CA3209	RCA	
	CA3215	RCA	
	LA1140	Sanyo	
	LA1150	Sanyo	
	LA1230	Sanyo	
	LA1231N	Sanyo	
	TDA1200	SGS	
	S041	Siemens	
	TBA120S	Siemens	
	TDA1047	Siemens	
	CA3089	Signetics	
	CA3089D2	Signetics	
	CA3189	Signetics	
IF Amplifier Detector	TBA120U	Signetics	
IF Amplifier/Detector	TBA750C	Signetics	
	TCA770	Signetics	
	ULN-2111A	Sprague	
	ULN-2136A	Sprague	
	ULN-3889A	Sprague	
	TBA120	Telefunken	
	TDA1093	Telefunken	
	SN76642	TI	
	SN76643	TI	
	SN76669	TI	
	SN76675	TI	
	SN76689	TI	
IF Amplifier, Narrow Band	MC3359	Motorola	
	ULN-3859A	Sprague	
IF Amplifier, PLL, Squelch, Narrow Band	SL6640	Plessey	
IF System	LA1235	Sanyo	
	LA2300	Sanyo	
Interference Absorption Circuit	TDA1001B	Signetics	
LED Tuning Indicator	LB1450	Sanyo	
	LB1473	Sanyo	
Mixer, IF, AGC System	LA1160	Sanyo	
Modulator Circuit (VCO/modulator, 1.4 to 14 MHz)	MC1376	Motorola	
Noise Canceller	HA11219	Hitachi	
	LA2100	Sanyo	
	LA2101	Sanyo	
	LA2110	Sanyo	
Prescaler (for digital tuning)	TD6104	Toshiba	
Receiver System	**TDA7000**	**Signetics**	**(3663)**
	TDA7010T	**Signetics**	**(3666)**
Receiver System with Squelch and Scan Control	MP5071	MicroPwr	
	MC3357	Motorola	
RF/IF Amplifier	CA3127	RCA	
	TBA120U	Signetics	
	TCA770	Signetics	
Stereo Decoder	XR1310	Exar	
	HA11223	Hitachi	
	HA11227	Hitachi	
	HA1156	Hitachi	
	HA1196	Hitachi	
	MC1309	Motorola	
	MC1310	Motorola	
	TCA4500	Motorola	
	μA758A	Motorola	
	LM1310	National	
	LM1800	National	
	LM1870	National	
	LM4500A	National	
	μPC1026	NEC	
	AN362	Panasonic	
	CA1310A	RCA	
	CA3195	RCA	
	CA758	RCA	
	LA3301	Sanyo	
	LA3350	Sanyo	
	LA3361	Sanyo	
	LA3365	Sanyo	
	LA3370	Sanyo	
	LA3375	Sanyo	
	LA3380	Sanyo	
	LA3381	Sanyo	
	LA3390	Sanyo	
	TCA4500A	Siemens	
	TCA4510	Siemens	
	LM1870	Signetics	
	TDA1578A	Signetics	
	TEA5580	Signetics	
	μA758	Signetics	
	ULN-3809A	Sprague	
	ULN-3810A	Sprague	
	ULN-3812A	Sprague	
	SN76104	TI	
	SN76105	TI	
	SN76110	TI	
	SN76111	TI	
	SN76113	TI	
	SN76115	TI	
	SN76116	TI	
	TA7157A	Toshiba	
	TA7401A	Toshiba	
	TA7604A	Toshiba	
	TA7624	Toshiba	
Stereo Multiplexer (PLL)	TA7343	Toshiba	
Tuner	TUA1000	Siemens	
	TDA1062	Telefunken	
	TDA1062S	Telefunken	

Remote Control Circuits

Function	Device	Source	
Amplifier-Detector	MC3373	Motorola	
Receiver, Infrared	TDA3047	Signetics	
Receiver Infrared	TDA3048	Signetics	
Remote Control, Infrared	SAA3004	Signetics	
	SAA3027	Signetics	

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Consumer Circuits (Cont'd)

Remote Control Circuits (Cont'd)

Function	Device	Source	
RF Amplifier/Mixer	CA3005	† RCA	
	CA3006	† RCA	
	CA3049	† RCA	
Transceiver (ultrasonic)	LM1812	National	
Transmitter, Infrared	MM53226	National	
	SAA3006	Signetics	
	SN76881	TI	(387)
	SN76882	TI	(387)
	SN76891	TI	(387)

NOTE: In the following category ONLY, the dagger symbol in front of a company name indicates a transmitter/encoder. Absence of a dagger designates a receiver/decoder.

Function	Device	Source	
Transmitter/Receiver (encoder/decoder), 2 device sets	S2600	† AMI	
	S2601	AMI	
	S2602	† AMI	
	S2603	AMI	
	S2604	† AMI	
	S2605	AMI	
	S2742	AMI	
	S2743	† AMI	
	S2747	AMI	
	S2748	AMI	
	AY3-8470	† GI	
	AY3-8475	GI	
	SAA1250	† ITT	
	SAA1251	ITT	
	SAA1272	ITT	
	SAA1350	† ITT	
	SAA1351	ITT	
	MC14457	† Motorola	
	MC14458	Motorola	
	MC145026	Motorola	
	MC145027	Motorola	
	MC145028	Motorola	
	LM1871	National	
	LM1872	National	
	MM5425	National	
	MM58250	† National	
	MSL9362	OKI	(4118)
	MSL9363	OKI	(4118)
	MN6021	Panasonic	
	MN6025	Panasonic	
	ML920	Plessey	
	ML922	Plessey	
	ML926	Plessey	
	ML928	Plessey	
	ML929	Plessey	
	SL490	Plessey	
	M1124	† SGS	
	SAB3209	Siemens	
	SAB3210	† Siemens	
	SAB3271	Siemens	
	SAB4209	Siemens	
	SDA2008	† Siemens	
	SDA3205	Siemens	
	SDA3206	† Siemens	
	SAA5000	† Signetics	
	SAA5012	Signetics	
	SAF1032	Signetics	
	SAF1039	Signetics	
	U318	Telefunken	
	U321	† Telefunken	
	U327	† Telefunken	
	U328	Telefunken	
	SN76605	† TI	
	SN76606	TI	

(Continued)

Function	Device	Source	
Transmitter/Receiver (encoder/decoder), 2 device sets (Cont'd)	SN76730	TI	
	SN76831	† TI	
	SN76832A	TI	(387)
	TC9132	† Toshiba	
	TC9133	Toshiba	
	TC9134	Toshiba	
Transmitter/Receiver, Preamplifier	TEA1009	ITT	

Speech Circuits

Function	Device	Source	
Delta Modulation System, Continuously Variable Slope	HC55536	Harris	
	HC55564	Harris	
Preprogrammed Vocabulary ROM	VM61001	TI	
	VM61002	TI	(1718)
	VM61003	TI	(1718)
	VM61004	TI	(1718)
	VM61005	TI	(1718)
	VM71001	TI	
	VM71002	TI	
	VM71003	TI	(1718)
Speech Analyzer/Synthesizer, ADPCM	**MSM5218**	OKI	(4118)
Speech Circuit for Electronic Telephones	TCM1705A	TI	
Speech Evaluation Kit	DT1051	National	
	DT1054	National	
Speech FIFO Buffer Memory and Control Logic	SPB640	GI	
Speech Generator	UAA1003	ITT	
	UAA1103	ITT	
Speech Interface Control Logic	SPR000	GI	
Speech Synthesis Processor	SP-0250	GI	
	SP0256	GI	
	DT1000	National	
	MM54104	National	
	SVM9300	SMOS	
	MEA8000	Signetics	(3672)
	TMS5100	TI	
	TMS5110	TI	(1717)
	TMS5200	TI	
	TMS5220	TI	(1717)
	SC-01	Votrax	
Speech Synthesis System, Basic Numbers Kit	DT1052	National	
	DT1055	National	
Speech Synthesis System, Standard Vocabulary Kit	DT1050	National	
	DT1053	National	
	DT1056	National	
	DT1057	National	
Speech Synthesizer, ADPCM	**MSM5205**	OKI	(4118)
	MSM6202	OKI	(4118)
Speech Synthesizer, Linear Predictive Data Stored in ROM	**S3610**	AMI	(2813)
	S3620	AMI	(2814)
Synthesized-Speech ROM	**TMS6100**	TI	(1718)
	TMS6125	TI	(1718)

Tape Recorder Circuits, Audio

Function	Device	Source
Amplifier System	TA7223	Toshiba
	TA7628	Toshiba
Amplifier System (for cassette recorders)	TA7628H	Toshiba
Amplifier, with AGC, for Recorders	TDA2054	SGS
	TA7137	Toshiba
	TA7137-ST	Toshiba
Audio System	HA12006	Hitachi
	LM1818	National
	AN262	Panasonic
Automatic Cuing Circuit	LC7510	Sanyo
	LC7512	Sanyo
Automatic Leveling	S028-2	Siemens
Automatic Program Search	TC9138	Toshiba
	TC9139	Toshiba
Automatic Reverse/Eject for car stereo	TD6304	Toshiba
	TD6308	Toshiba
Auto-Reverse Cassette Control	TDA1508	Signetics
Broadband Compander	U401	Telefunken
Controller (mode change, absence recording)	HA12001	Hitachi
	TC9121	Toshiba
Head, Microphone, Headphone, Buffer, and Record Amplifiers	HA12005	Hitachi
	TA7617	Toshiba
IC Switch (cassette)	TC9143	Toshiba
	TC9144	Toshiba
Motor Speed Control (automatic stop, dc manual stop, biasing and erasing oscillator)	TDA7770	SGS
Motor Speed Control, Stop, Pause, Cassette Ejection	TDA7270	SGS
Power Amp, Preamp with ALC, Meter Driver	TA7225	Toshiba
Power Amp, Preamp with ALC, Meter Driver, Mute Control	TA7224	Toshiba
Power Amplifier (cassette)	TA7229	Toshiba
Power Amplifier (minicassette)	TA7331	Toshiba
Preamplifier with ALC	LA3201	Sanyo
	LA3210	Sanyo
	SSM2011	SSM
Preamplifier with ALC (cassette)	TDA1054M	SGS
Preamplifier with ALC (minicassette)	TA7330	Toshiba
System (power amp, preamp with ALC, for minicassette recorders)	TA7625	Toshiba
Tape Counter	LM8523	Sanyo
Tape Deck Amplifier System	TA7663	Toshiba
Tape Deck Amplifier, Dual Channel	TA7639	Toshiba
Tape Deck Automatic Reverse	AN6249	Panasonic
	AN6250	Panasonic

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR

Master Selection Guide

LINEAR–Consumer Circuits (Cont'd)

Function	Device	Source
Tape Recorder Circuits, Audio (Cont'd)		
Tape Deck Key Controller		
	AN6251	Panasonic
Tape Recorder Circuits, Video		
Color Processing Circuit		
	HA11704	Hitachi
	HA11705	Hitachi
	HA11706	Hitachi
	AN305	Panasonic
	AN337	Panasonic
	MN6061A	Panasonic
Dropout Compensation Circuit		
	AN316	Panasonic
FM Limiter	HA11703	Hitachi
	AN304	Panasonic
FM Recording Signal Processor		
	HA11701	Hitachi
	AN6321	Panasonic
	AN6331	Panasonic
Head Amplifier	AN6320	Panasonic
	AN6330	Panasonic
Luminance Processing		
	AN302	Panasonic
	AN303	Panasonic
Playback Signal Processor		
	HA11702	Hitachi
Servo Signal Processing		
	HA11707	Hitachi
	AN301	Panasonic
	AN318	Panasonic
	AN6341	Panasonic
	AN6342	Panasonic
	AN6344	Panasonic
Video Recording Processing		
	AN6300	Panasonic
16-Channel Precision Timer/Driver		
	CD22401	**RCA (838)**
Television Circuits		
AFT System	HA1108	Hitachi
	HA1126	Hitachi
	MC6190	Motorola
	MC6191	Motorola
	MC6192	Motorola
	MC6193	Motorola
	MC6194	Motorola
	MC6195	Motorola
	MC6196	Motorola
	LM3064	National
	AN321	Panasonic
	CA3064	† RCA
	CA3139	RCA
	LA1364	Sanyo
	SDA4260	Siemens
	SN76565	TI
	TA7070	Toshiba
Bandpass Filter		
	2002Z	NCM
Cable TV Channel Processor		
	SDA2110	Siemens
Camera	AN614	Panasonic
	AN616	Panasonic
Camera Sync. Generator		
	3262A	Fairchild
	3262B	Fairchild
	ZNA134E	Ferranti
	ZNA134J	† Ferranti

(Continued)

Function	Device	Source
Camera Sync. Generator (Cont'd)		
	HD44007	Hitachi
	MM5321	National
	MN6063	Panasonic
	MN6064	Panasonic
	S178A	Siemens
CATV Amplifiers (hybrid)		
	BGY54A	Amperex
	BGY55A	Amperex
	BGY56	Amperex
	BGY57	Amperex
	BGY58A	Amperex
	BGY74	Amperex
	BGY75	Amperex
	BGY78	Amperex
	MHW1121	Motorola
	MHW1127	Motorola
	MHW1171	Motorola
	MHW1172	Motorola
	MHW1182	Motorola
	MHW1221	Motorola
	MHW1222	Motorola
	MHW1341	Motorola
	MHW1342	Motorola
	MHW1343	Motorola
	MHW1391	Motorola
	MHW1392	Motorola
	MHW5181	Motorola
	MHW5182	Motorola
	MHW559	Motorola
	MHW560	Motorola
	MHW561	Motorola
	MHW562	Motorola
	MHW570	Motorola
	MHW572	Motorola
	MHW580	Motorola
	MHW594	Motorola
	MHW595	Motorola
	CA2100	TRW-LSI
	CA2300	TRW-LSI
	CA2301	TRW-LSI
	CA2418	TRW-LSI
	CA2600	TRW-LSI
	CA2601	TRW-LSI
Channel Display Driver/Decoder		
	LM1017	National
	U143	Telefunken
Channel Selection		
	µPC1009	NEC
	AN5010	Panasonic
	AN5011	Panasonic
	LB1500	Sanyo
	LB1515	Sanyo
	LB1550	Sanyo
	SN76701	TI
	SN76702	TI
	SN76710	TI
	SN76711	TI
	SN76721	TI
	SN76727	TI
	TA7171	Toshiba
	TA7172	Toshiba
	TA7177	Toshiba
	TA7178	Toshiba
Character Generator (indicates tuning voltage scale and band info on screen)		
	U191	Telefunken
Chroma Circuits (demodulators, IF amplifiers, luminance control, signal processors, and various combinations)		
	HA11247	Hitachi
	HA11409	Hitachi
	HA11412	Hitachi
	HA11417	Hitachi

(Continued)

Function	Device	Source
Chroma Circuits (demodulators, IF amplifiers, luminance control, signal processors, and various combinations) (Cont'd)		
	HA11580	Hitachi
	MC1377	Motorola
	MC1399	Motorola
	LM1828	National
	LM1848	National
	LM2887	National
	LM3126	National
	TBA510	National
	TBA530	National
	TBA540	National
	TBA560	National
	TBA990	National
	TDA2522	National
	TDA2523	National
	TDA2530	National
	TDA2560	National
	TDA3500	National
	TDA3501	National
	UPC580	NEC
	µPC1380	NEC
	AN236	Panasonic
	AN5310	Panasonic
	AN5311	Panasonic
	AN5320	Panasonic
	AN5330	Panasonic
	AN5620	Panasonic
	AN5630	Panasonic
	TDA2532	Plessey
	CA1398	RCA
	CA3067	RCA
	CA3070	RCA
	CA3071	RCA
	CA3072	RCA
	CA3121	RCA
	CA3125	RCA
	CA3126	RCA
	CA3128	RCA
	CA3135	RCA
	CA3137	RCA
	CA3143	RCA
	CA3144	RCA
	CA3145	RCA
	CA3151	RCA
	CA3153	RCA
	CA3156	RCA
	CA3158	RCA
	CA3170	RCA
	CA3172	RCA
	CA3194	RCA
	CA3201	RCA
	CA3217	RCA
	CA3221	RCA
	LA1368	Sanyo
	LA1369	Sanyo
	LA1390	Sanyo
	LB1332	Sanyo
	TDA2140	SGS
	TDA2151	SGS
	TDA2161	SGS
	TDA2522	Siemens
	TDA2530	Siemens
	TDA2560	Siemens
	TDA3500	Signetics
	TDA3505	Signetics
	TDA3510	Signetics
	TDA3520	Signetics
	TDA3562	Signetics
	TDA3563	Signetics
	TDA4550	Signetics
	TDA4560	Signetics

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

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Master Selection Guide

LINEAR–Consumer Circuits (Cont'd)

Television Circuits (Cont'd)

Function	Device	Source
Chroma Circuits (demodulators, IF amplifiers, luminance control, signal processors, and various combinations) (Cont'd)	ULN-2260A	Sprague
	ULN-3914A	Sprague
	TBA520	Telefunken
	TBA530	Telefunken
	TBA540	Telefunken
	TBA560	Telefunken
	TBA990	Telefunken
	TDA2140	Telefunken
	TDA2150	Telefunken
	TDA2151	Telefunken
	TDA2160	Telefunken
	TDA2161	Telefunken
	SN76242	TI
	SN76243	TI
	SN76246	TI
	SN76267	TI
	SN76298	TI
	SN76645	TI
	SN76889	TI
	TA7141A	Toshiba
	TA7148	Toshiba
	TA7149	Toshiba
	TA7150	Toshiba
	TA7161	Toshiba
	TA7167	Toshiba
	TA7168	Toshiba
	TA7169	Toshiba
	TA7173	Toshiba
	TA7174	Toshiba
	TA7192	Toshiba
	TA7193	Toshiba
	TA7607A	Toshiba
	TA7611A	Toshiba
	TA7621	Toshiba
	TA7622A	Toshiba
	TA7650	Toshiba
	TA7659	Toshiba
	TA7660	Toshiba
	TA7661	Toshiba
	TA7675	Toshiba
	TA7676	Toshiba
	TA7678	Toshiba
D/A Converter (converts an input to coarse and fine tune outputs)	SAB3013	Signetics
Decoder, 1 of 16	M054	SGS
	M055	SGS
Deflection Correction Circuit	TDA4610 •	Siemens
Digital Tuner and Signal Detector	LM1019	National
	TDA4431	SGS
Digital Tuning	SAB3035	Signetics
	SAB3036	Signetics
	SAB3037	Signetics
Digital Tuning Device Set	SAA1075	ITT
	SAA1274	ITT
	SAA1276	ITT
Digital Tuning System Memory Controller	TA7619A	Toshiba
Digital Tuning System (PLL)	TC9136	Toshiba
	TC9137	Toshiba
Frequency Synthesis Control (converts tuning data into frequency information for SDA100 system)	SM564	Siemens
Frequency Synthesis Control (interface between synthesizer and varicap diode tuner)	MC2801	Motorola
Frequency Synthesizer	SAB3035	Signetics
Frequency Synthesizer, interfaces to MPU	MN6044	Panasonic
	MN6049	Panasonic
Games, See Consumer Circuits, Video Games		
Horizontal & Vertical Processor	HA11235	Hitachi
	HA11244	Hitachi
	LM1880	National
	AN295	Panasonic
	AN5410	Panasonic
	AN5411	Panasonic
	AN5430	Panasonic
	AN5431	Panasonic
	AN5435	Panasonic
	CA3202	RCA
	CA3223	RCA
	TDA2577A	Signetics
	TDA2578A	Signetics
	TDA2595	Signetics
Horizontal Processor	TBA940	ITT
	TBA950	ITT
	TDA1950	ITT
	TDA9500	ITT
	TDA9503	ITT
	TDA9513	ITT
	MC1391	Motorola
	MC1394	Motorola
	LM1391	National
	TBA920	National
	TBA950-2	National
	TDA2590	National
	TDA2591	National
	AN5750	Panasonic
	AN5760	Panasonic
	TDA2591	Plessey
	CA1391	RCA
	CA1394	RCA
	CA3159	RCA
	CA3210	RCA
	CA920A	RCA
	TDA1180	SGS
	TDA2593	Signetics
	TDA2594	Signetics
	TDA2591	Telefunken
	TDA2593	Telefunken
	SN76525	TI
	TA7151	Toshiba
Intercarrier Frequency Modulator	4002Z	NCM
Line Selector	4003Z	NCM
MATV Amplifiers (hybrid)	OM320	Amperex
	OM321	Amperex
	OM322	Amperex
	OM323	Amperex
	OM323A	Amperex
	OM335	Amperex
	OM336	Amperex
	OM337	Amperex
	OM337A	Amperex
	OM339	Amperex
	OM345	Amperex
	OM350	Amperex
	OM360	Amperex
	OM361	Amperex
	OM370	Amperex
Modulator Circuit for Video Tape Recorders and Disc Players	MC1374	Motorola
Noise Reduction System	TA7652	Toshiba
On Screen Channel Display	M191	SGS
	M192	SGS
On Screen Display	SDA2005	Siemens
On Screen Tuning Voltage Bargraph Display	UAA190	Siemens
PAL Color Encoder and Video Summer	TEA1002	Signetics
Pattern Generator	4001Z	NCM
Picture Contrast/Brightness	TA7126	Toshiba
	TA7134	Toshiba
	TA7135	Toshiba
Power Supply Controller	LA5112	Sanyo
Prescalers		
Program Memory (17x16)	M193	SGS
Program Memory (20x12), D/A	SN76720	TI
Radio	M755	SGS
	M756	SGS
Signal Processor, Bilingual	CA3120	RCA
	CA3142	RCA
	CA3154	RCA
	LA7751	Sanyo
	LA7755	Sanyo
	TBA890	Signetics
	SN76524	TI
	SN76544	TI
	SN76545	TI
Small Signal Combination IC for Monochrome TV	TDA4500	Signetics
Sound Circuits	HA11229	Hitachi
	HA1124	Hitachi
	HA1125	Hitachi
	HA1364	Hitachi
	TDA1235	ITT
	TDA1236	ITT
	MC1357	Motorola
	MC1358	Motorola
	TDA1190	Motorola
	TDA11902	Motorola
	TDA1190P	Motorola
	TDA3190P	Motorola
	TBA120S	National
	μPC575	NEC
	AN240P	Panasonic
	AN241	Panasonic
	AN340	Panasonic
	AN5210	Panasonic
	AN5220	Panasonic
	AN5250	Panasonic
	AN5260	Panasonic
	AN5730	Panasonic
	TBA120	Plessey
	TBA750	Plessey
	CA1190	RCA
	CA1191	RCA
	CA3042	RCA
	CA3065	RCA
	CA3075	† RCA
	CA3134	RCA
	LA1320	Sanyo

(Continued)

† Military Temperature Range (–55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Consumer Circuits (Cont'd)

Television Circuits (Cont'd)

Function	Device	Source
Sound Circuits (Cont'd)	LA1363	Sanyo
	LA1365	Sanyo
	TDA1190	SGS
	TDA2190	SGS
	TDA3190	SGS
	TDA2840	Siemens
	TDA2841	Siemens
	TDA4280T/U	Siemens
	TDA4281T/U	Siemens
	TBA120U	Signetics
	TBA750C	Signetics
	TDA2546A	Signetics
	TDA3810	**Signetics (3613)**
	TDA1190Z	Sprague
	TDA3190	Sprague
	ULN-2111A	Sprague
	ULN-2290	Sprague
	TBA120	Telefunken
	SN76643	TI
	SN76651	TI
	SN76660	TI
	SN76665	TI
	SN76666	TI
	SN76688	TI
	TA7051	Toshiba
	TA7072	Toshiba
	TA7073A	Toshiba
	TA7130	Toshiba
	TA7146	Toshiba
	TA7176A	Toshiba
	TA7243	Toshiba
	TA7314	Toshiba
	TA7632	Toshiba
	TA7633	Toshiba
Surface Acoustic Wave Filter, IF	SW203	Plessey
Sychron Generator	2001Z	NCM
Sync Generator	SAA1043P	Signetics
Synchronization and Deflection Circuit	LA7801	Sanyo
	LA7802	Sanyo
	LA7806	Sanyo
	LA7810	Sanyo
Synchronous Demodulator	TDA0820T	Signetics
Teletext, Channel and Page Selector	TEA9241	Thomson-CSF
Teletext, DIDON Demodulator	TEA2585	Thomson-CSF
	TEA2586	Thomson-CSF
Test Pattern Generator	ZNA234	Ferranti
Timer, Programmable	MM53100	National
	MM53105	National
Tone Control	TDA1524	Signetics
	TA7125	Toshiba
Touch Tuner: See Switches, Capacitance or touch sensing and TV		
Traffic Camera Controller	4004Z	NCM
Tuner Band Switching	AN5700	Panasonic
	LA7900	Sanyo
	TA7315	Toshiba
Tuner Controller	SL952	Plessey

Function	Device	Source
Tuner Controller, Non-Volatile Storage for 16 Programs	U193	Telefunken
Tuner Controller (2 device set)	SAA1020	ITT
	SAA1121	ITT
	SAA1220	ITT
Tuning System	SDA100	Siemens
	SDA200	Siemens
TV Camera Sync Generator	CD22402	RCA
TV Channel Selection—See also: Switches, Capacitance or Touch Sensing and TV Tuning, both this section		
Universal Sync. Generator (NTSC)	SCN2622A	Signetics
Universal Sync. Generator (PAL)	SCN2621A	Signetics
Universal Video Interface	SCN2637A	Signetics
Vertical Deflection	MC1393	Motorola
	MC6190	Motorola
	MC6191	Motorola
	MC6192	Motorola
	MC6193	Motorola
	MC6194	Motorola
	μPC1031	NEC
	AN5510	Panasonic
	AN5512	Panasonic
	AN5520	Panasonic
	LA1385	Sanyo
	LA1463	Sanyo
	LA1464	Sanyo
	LA7800	Sanyo
	TDA1170	SGS
	TDA1270	SGS
	TDA1470	SGS
	TDA1470A	SGS
	TDA1670	SGS
	TDA1770	SGS
	TDA2653	Signetics
	TDA2653A	Signetics
	TDA2655A	Signetics
	TDA2655B	Signetics
	TDA3651	Signetics
	TDA3651A	Signetics
	TDA3652	Signetics
	TDA1170	Sprague
	ULN-2270	Sprague
	U2170B	Telefunken
	TA7152	Toshiba
	TA7242	Toshiba
VHF Tuner	TUA2000	Siemens
Video Circuits (IF amplifiers, detectors, AGC, AFC, and various combinations)	HA11215	Hitachi
	HA11220	Hitachi
	HA11221	Hitachi
	HA11238	Hitachi
	HA11405	Hitachi
	MC13001	Motorola
	MC13002	Motorola
	MC13010	Motorola
	MC1330A1	Motorola
	MC1330A2	Motorola
	MC1349	Motorola
	MC1350	Motorola
	MC1352	Motorola
	MC1372	Motorola
	MC1373	Motorola
	LM1822	National
	LM1886	National
	LM1889	National

(Continued)

Function	Device	Source
Video Circuits (IF amplifiers, detectors, AGC, AFC, and various combinations) (Cont'd)	LM2889	National
	TBA440	National
	TBA970	National
	TDA2540	National
	TDA2541	National
	TDA440	National
	μPC595	NEC
	μPC596	NEC
	AN5111	Panasonic
	AN5120	Panasonic
	AN5710	Panasonic
	AN5720	Panasonic
	SL1430	Plessey
	SL1431	Plessey
	SL1432	Plessey
	TDA440	Plessey
	CA1352	RCA
	CA270	RCA
	CA3068	RCA
	CA3136	RCA
	CA3191	RCA
	CA3192	RCA
	CA3216	RCA
	LA1352	Sanyo
	LA1353	Sanyo
	LA1354	Sanyo
	LA1357N	Sanyo
	TDA4420	SGS
	TDA4433	SGS
	SDA5500	Siemens
	TBA1440G	Siemens
	TBA1441	Siemens
	TDA5500	Siemens
	TDA5600	Siemens
	TDA5610	Siemens
	TDA5611	Siemens
	TDA2544	Signetics
	TDA3540	Signetics
	TDA3541	Signetics
	TDA3564	Signetics
	TDA440	Telefunken
	TDA4400	Telefunken
	TDA4410	Telefunken
	TDA4420	Telefunken
	TDA4421	Telefunken
	TDA4422	Telefunken
	TDA4430	Telefunken
	TDA4431	Telefunken
	TDA4432	Telefunken
	TDA4440	Telefunken
	TDA4450	Telefunken
	SN76600	TI
	SN76644	TI
	SN76650	TI
	TA7069	Toshiba
	TA7074	Toshiba
	TA7075	Toshiba
	TA7076	Toshiba
	TA7124	Toshiba
	TA7145	Toshiba
	TA7147	Toshiba
	TA7162	Toshiba
	TC5003	Toshiba
Video Disc Player/Microprocessor Interface (digital auxiliary information buffer)	CD3226	RCA
Video Pulse Generator	S178	Siemens
Y Signal Recording Processor	TA7637	Toshiba

† Military Temperature Range (−55° to 125°C)

* Typical Value

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Master Selection Guide

LINEAR–Consumer Circuits (Cont'd)

Function	Device	Source
Video Game Circuits		
Character Generator	**HS3819**	**Harris (4658)**
Clock Generator (for MM57100)	MM53104	National
Color Processor (generates single composite color signal from game chip input)	AY3-8915	GI
Dedicated (some may be used in programmable systems also)	AY3-8500	GI
	AY3-8500-1	GI
	AY3-8603	GI
	AY3-8605	GI
	AY3-8606	GI
	AY3-8607	GI
	AY3-8610	GI
Interface (processes graphics data and generates video signals)	AY3-8900	GI
	AY3-8900-1	GI
PAL Color Encoder and Video Summer	TEA1002	Signetics
Programmable Video Interface	SCN2636A	Signetics
	SCN2637A	Signetics
Sound Generator	AY3-8910	GI
	AY3-8912	GI
	SN76477	TI
TV/μP Interface	M106	SGS
Video Display Generator	**MC6847**	**Motorola (1505)**
Video Modulator (interfaces audio, color, difference, and luminance signals to TV antenna terminals)	MC1372	Motorola
	MC1373	Motorola
	LM1889	National
Miscellaneous		
Appliance Timer	FCM7040	Fairchild
Digital Lock	**LS7220**	**LSIComp (803)**
	LS7225	**LSIComp (803)**
	LS7226	**LSIComp (803)**
	LS7228	**LSIComp (803)**
	LS7229	**LSIComp (803)**
Facsimile	LM1011	National
	MN8023	Panasonic
General-Purpose A/D Converter and Digital-Scale Circuit	S4036	AMI
Ground Fault Interrupter	CS259	Cherry
	MC3426	Motorola
	LM1851	National
Motor, Induction Motor Energy Saver	HV1000	Harris
	HV1005	Harris
	HV1010	Harris
Motor Positioning System (3-chip set), Tachometer Converter, D/A Converter and Switch-Mode Driver for dc Motor	SG290N	SiliconG
	SG291N	SiliconG
	SG2925	SiliconG
Motor Speed Regulator	MC212	AnalogSys
	MC213	AnalogSys
	CS140	Cherry
	CS175	Cherry
	CS2917	Cherry
(Continued)		
Motor Speed Regulator (Cont'd)	MC2907	Cherry
	LM1014	Fairchild
	LM1014A	Fairchild
	μA7392	Fairchild
	LS7263	LSIComp
	LM1014	National
	MSM5819	**OKI (4118)**
	SL440	Plessey
	TDA1085A	Plessey
	TDA2085A	Plessey
	TCA900	SGS
	TCA910	SGS
	TDA1151	SGS
	S572	Siemens
	TCA955	Siemens
	TDA1506	Signetics
	SG1731	SiliconG
	SG2731	SiliconG
	SG3731	SiliconG
Motor Speed Regulator, for Record Players, Tape Recorders	TDA1533	Signetics
Motor Speed Regulator, PLL	TM4503	Toshiba
Motor Speed Regulator, PLL, for Record Players, VTR	**MSM5816**	**OKI (4118)**
Motor, Stepping Motor Drive	PBL3717	RIFA
Motor, Stepping Motor Driver	SAA1027	Signetics
	UDN-2949Z	Sprague
Music Chimes	SAB0600	Siemens
Music, Voltage Controlled Oscillator	SSM2030	SSM
	SSM2033	SSM
Music, Voltage Controlled Filter, Four Stage	SSM2040	SSM
	SSM2044	SSM
Music, Voltage Controlled Transient Generator	SSM2050	SSM
	SSM2055	SSM
	SSM2056	SSM
Optical Transceiver (intrusion alarm)	CS258A	Cherry
Peak Power Meter Driver, Dual (for hi-fi stereo)	TA7318	Toshiba
	TA7332	Toshiba
Protector Circuit (overcurrent detection for OCL and speaker)	HA12002	Hitachi
	TA7317	Toshiba
Revolution Counter Pulse Shaper	SAK215	ITT
Servo Driver	**NE544**	**Signetics (3632)**
Smoke Detector	CS179	Cherry
	MP7162	MicroPwr
	MC14466	Motorola
	MC14467	Motorola
	LM1801	National
	NF5301	National
	CA3164	**RCA (3604)**
	SCL5331-5	SSS
	SCL5331-6	SSS
	SCL5341	SSS
	SD2	Supertex
	SD3A	Supertex
Switch, Video	SAA1300	Signetics
Switches	SAS560	Hitachi
	SAS570	Hitachi
	MN1976	Panasonic
(Continued)		
Switches (Cont'd)	SAS560	Siemens
	SAS570	Siemens
	SAS580	Siemens
	SAS590	Siemens
	SAS6810	Siemens
	SAS660	Telefunken
	SAS6600	Telefunken
	SAS6610	Telefunken
	SAS670	Telefunken
	SAS6700	Telefunken
	SAS6710	Telefunken
Switches, Capacitive Touch Input (keyboard encoder and prioritizer)	TMS1976	TI
Switches, DC-Controlled, Audio	LM1037	National
	LM1038	National
	TDA1029	Signetics
Switches, Proximity	SAS221	Siemens
	TCA205AK	Siemens
	TDA0159	Thomson-CSF
	TDA0161	Thomson-CSF
	TDA0162	Thomson-CSF
Switches, Touch-Sensitive Light Dimmer	**LS7231**	**LSIComp (803)**
	LS7232	**LSIComp (803)**
	LS7233	**LSIComp (803)**
	LS7234	**LSIComp (803)**
	LS7235	**LSIComp (803)**
	S576A	Siemens
	S576B	Siemens
	S576C	Siemens
	TEA1010	Signetics
	TEA1058T	Signetics
Tachometer Circuit	CS189	Cherry
	CS2917	Cherry
	LM2907	National
	LM2917	National
	SN76810	TI
Thermo Controller (for air conditioners, refrigerators, etc.)	TA7165	Toshiba
Timers. See Appliance Timers, Clock, Watch circuits in this section and Linear-Timers		
Tone Synthesizer for Doorchimes, Toys	AY3-1350	GI
Traffic Light Control Circuit	4004Z	NCM
Tuning Voltage Stabilizer, for use with Variable Capacitance Diodes	TCA720	ITT
	TAA550	SGS

† Military Temperature Range (−55° to 125°C)

* Typical Value

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Master Selection Guide

LINEAR–Followers

Followers

See also Linear-Amplifiers, Special Purpose - Current Amplifiers

Bias Current nA 25°C	Offset Voltage mV 25°C	Voltage Drift μV/°C	Unity Gain Bandwidth MHz min	Slew Rate v/us	Output V mA	Supply Range, V	Comments	Device	Source
0.1	10	25 *	100 *	1000	9 @ 100	±5 to ±20	Fast Follower	**ADLH0033**	† **AD (3353)**
								LH0033	† National
								TP0033-80	† TeledyneP
	50	400	200	3000	10 @ 200	±11 to ±18	Very Fast, FET	9963	† OEI
0.15	20	25 *	100 *	1000	9 @ 100	±5 to ±20	Fast Follower	**ADLH0033C**	**AD (3353)**
								LH0033C	National
								TP0033	TeledyneP
0.2	25	300 *	200 *	2000	10 @ 200	±5 to ±20	Very Fast Follower	LH0063	† National
	50	300 *	200 *	2000	10 @ 200	±5 to ±20	Very Fast Follower	LH0063C	National
0.2 *	50	300 *	300 *	2000	10 @ 200	±5 to ±20	Gain 0.094 (50 Ohm)	3553	† Burr-Brown
0.4	6.0	90	55 *	220	10 @ 22	±6 to ±18	Very Fast Follower	BUF-03E	PMI
		100	55 *	220	10 @ 21	±6 to ±18	Very Fast Follower	BUF-03A	PMI
0.7	15.0	150	50 *	180	10 @ 25	±6 to ±18	Very Fast Follower	BUF-03F	PMI
			170	50 *	180	±6 to ±18	Very Fast Follower	BUF-03B	† PMI
3	4.0	6 *	12 *	30 *	10 @ 1	±5 to ±18	Follower, Replaces 102	SG210	SiliconG
			20 *	30 *	10 @ 1	±5 to ±18	Dual 210 Follower	LH2210	National
							Follower, Replaces 102	LM210	National
								SFC2210	Thomson-CSF
		10 *	20 *	30 *	10 @ 1	±5 to ±18	Follower, Replaces 102	LM110	† Intersil
		12 *	12 *	30 *	10 @ 1	±5 to ±18	Follower, Replaces 102	SG110	† SiliconG
			20 *	30 *	10 @ 1	±5 to ±18	Dual 110 Follower	LH2110	Intersil
								LH2110	† National
							Follower, Replaces 102	LM110	† National
5	20.0	100	200	1000	10 @ 500	±11 to ±18	Fast, High Current	9911	† OEI
7	7.5	10 *	12 *	30 *	10 @ 1	±5 to ±18	Follower, Replaces 102	SG310	SiliconG
			20 *	30 *	10 @ 1	±5 to ±18	Dual 310 Follower	LH2310	Intersil
								LH2310	† National
							Follower, Replaces 102	LM310	Intersil
								LM310	National
10	5.0	6 *	—	—	10 @ 1.25	±15	Follower	LM102	† Intersil
			8 *	10 *	10 @ 1	±15	Follower	SG102	† SiliconG
			10 *	10 *	10 @ 1.25	±12 to ±18	Follower	LM102	† National
15	10.0	15 *	8 *	10 *	10 @ 1	±15	Follower	SG202	SiliconG
			10 *	10 *	10 @ 1.25	±12 to ±18	Follower	LM202	National
20	20.0	100	60	2000	10 @ 100	±6 to ±18	Very Fast Follower	9910	† OEI
30	15.0	20 *	—	—	10 @ 1.25	±15	Follower	LM302	Intersil
			8 *	10 *	10 @ 1	±15	Follower	SG302	SiliconG
			10 *	10 *	10 @ 1.25	±12 to ±18	Follower	LM302	National
	20	100	25	1000	10 @ ±50	±3 to ±15	6 Identical Sections	MZ320	AnalogSys
35	15	33 *	250 *	1300	10 @ 100	±5 to ±16	Video Buffer	**HA-5033-2**	† **Harris (3462)**
								HA-5033-5	**Harris (3462)**
5000	5	25	125 *	1400	12 @ 100	—	Fast Follower	**HOS-100A**	**AD (3353)**
								HOS-100S	† **AD (3353)**
20000	20	100	24 *	1500 *	10 100	±6 to ±18	Follower, Current Booster	AH0010C	OEI
								AH0010F	OEI

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers

General Purpose

Dual Amplifiers. The 1458 (0°C to 70°C) and the 1558 (−55°C to 125°C) offer approximately the same performance as the 741. Compensation is built in.

Device	Source
XR1458	Exar
μA1458	Fairchild
MC1458	Motorola
LM1458	National
OP-14	**PMI (3566)**
RC1458	Raytheon
CA1458	RCA
NE5512	**Signetics (3638)**
NE5514	**Signetics (3640)**
SE5512	**† Signetics (526,3638)**
SE5514	**† Signetics (3640)**
MC1458	SiliconG
SG1458	SiliconG
MC1458	TI

The 101A series consists of the 101A (−55°C to 125°C), the 201A (−25°C to 85°C) and the 301 (0°C to 70°C). These units require an external compensation capacitor which permits the bandwidth to be optimized for particular applications.

Device	Source
AD101A	**† AD (3351)**
μA101A	Fairchild
LM101A	† LinearTech
LM101A	† Motorola
LM101A	† National
LM101A	† Raytheon
LM101	**† Signetics (526)**
SG101A	† SiliconG
LM101A	† TI
TA7506	Toshiba

The performance of the 741 series is similar to the 101. These units include internal compensation to make the device stable and to eliminate the need for an external capacitor.

Device	Source
AD741	**† AD (3351)**
μA741	Fairchild
ICL741	† Intersil
MP5502	**† MicroPwr (3529)**
MC1741	† Motorola
LM741	† National
μPC741	NEC
OP-02	**PMI (3566)**
PM-741	PMI
RC741	Raytheon
CA741	RCA
μA741	† Signetics
SG741	† SiliconG
SFC2741	Thomson-CSF
TA7504	Toshiba

FET Input. The "741" of the FET input devices has yet to be established. Such a device requires very low cost, several sources, and many users. Commercial devices in the 155 series above meet some of these criteria, however, devices from the series below are generally lower in cost.

Device	Source
μAF771	Fairchild
LF13741	National
LF351	National
CA3140	**† RCA (3595)**
CA3160	**† RCA (3596)**
CA3260	**RCA (3595)**
LF351	Motorola

FET Input. Bipolar/JFET available in standard (155), wideband (156) and uncompensated (157) versions, premium performance (A and B suffixes), and various temperature ranges (155, 255, 355, etc are available.) Some versions approach the low cost of the units below.

Device	Source
LF155	† AMD
LF155	† Intersil
LF155	† Motorola
PM-155	† PMI

High Output Current

mA V	Device	Source
10000 @ 26	OPA501S	† Burr-Brown
10000 @ 20	**OPA501**	**Burr-Brown (2850)**
	OPA501A	Burr-Brown
5000 @ 45	PA07	Apex
5000 @ 42	PA10A	† Apex
5000 @ 37	PA10	Apex
	PA10M	† Apex
5000 @ 22	PA11	Apex
	PA73	Apex
3500 @ 18	MCEL165	MCE
	MCEL2165	MCE
3000 @ 18	MCETCA2365	MCE
	MCETCA365	MCE
2700 @ 24	ICH8530I	Intersil
	ICH8530M	† Intersil
2000 @ 32	PA09	Apex
2000 @ 30	**3572A**	**Burr-Brown (2850)**
2000 @ 24	ICH8520I	Intersil
	ICH8520M	† Intersil
2000 @ 22	PA01	Apex
	LH0101	National
	LH0101A	† National
	LH0101AC	National
	LH0101C	National
2000 @ 20	**3573**	**Burr-Brown (2850)**
2000 @ 18	LH0021	† National
2000 @ 10	CLC103A	Comlinear
	CLC103AM	† Comlinear
1500 @ 44	PA12A	† Apex
1500 @ 34	PA12	Apex
	PA12M	† Apex
1000 @ 30	**3571A**	**Burr-Brown (2850)**
1000 @ 24	ICH8510I	Intersil
	ICH8510M	† Intersil
1000 @ 10	LH0021C	National
750 @ 34	1461	TeledyneP
500 @ 10	LH0061	† National
	LH0061C	National
200 @ 10	3553	† Burr-Brown
	μA759	† Fairchild
	μA759C	Fairchild
150 @ 140	PA08	Apex
130 @ 13	LH0041	† National
	LH0041C	National
100 @ 10	AD3554A	AD
	AD3554D	**AD (3353)**
	AD3554S	† AD
	HOS-060S	**† AD (3353)**
	3329	**† Burr-Brown (2850)**
	3554A	**Burr-Brown (2851)**
	3554B	**Burr-Brown (2851)**
	3554S	**Burr-Brown (2851)**
	CLC200A	Comlinear
	CLC200AM	† Comlinear
	LH0003	† National
	TP3554	TeledyneP
100 @ —	CA3094	† RCA

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR

Master Selection Guide

LINEAR–Operational Amplifiers (Cont'd)

High Output Current (Cont'd)

mA V	Device	Source
75 @ 40	3583	Burr-Brown
75 @ 10	PA83	Apex
	PA83M	† Apex
75 @ 145	1480	TeledyneP
60 @ 30	**3580J**	**Burr-Brown (2850)**
50 @ 10	**AD380**	**AD (3353)**
	AD380S	† AD
	AD382	**AD (3353)**
	AD382S	† AD
	AM-500	**Datel (2861,2865)**
	9914	OEI
	9918	OEI
	AMP-01	† PMI
	1430	TeledyneP
50 @ 5	LH0005	National
	LH0005A	† National
47 @ 14	LH0020	† National
	LH0020C	National
40 @ 143	PA84	Apex
40 @ 4	LH0005C	National
30 @ 70	3581J	Burr-Brown
25 @ 10	**AM-430**	**Datel (2864)**
	AM-430M	† Datel
20 @ 12	TAA2761	Siemens
	TAA2762	† Siemens
	TAA2765	Siemens
	TAA4761	Siemens
	TAA4765	Siemens
	TAA761	Siemens
	TAA762	† Siemens
	TCA311	Siemens
	TCA312	† Siemens
	TCA315	Siemens
	TCA325	Siemens
	TCA331	Siemens
	TCA332	† Siemens
	TCA335	Siemens
20 @ 8	TAA861	Siemens
	TAA862	† Siemens
	TAA865	Siemens
15 @ 30	LH0004C	National
15 @ 10	**HA-2620**	**† Harris (3408)**
	HA2620	† Intersil
15 @ 145	3582J	Burr-Brown
	3583	**Burr-Brown (2850)**
	3584	**Burr-Brown (2850)**

High Speed

Unity Gain Slew Rate (V/µs min)	Device	Source
8000	CLC220A	Comlinear
	CLC220AM	† Comlinear
6000	CLC103A	Comlinear
	CLC103AM	† Comlinear
4000	CLC200A	Comlinear
	CLC200AM	† Comlinear
	CLC210A	Comlinear
	CLC210AM	† Comlinear
1500	ADLH0033	† AD
	HOS-100S	† AD
1400	ADLH0033C	AD
	HOS-100A	AD
1000	**AD3554**	**AD (3353)**
	AD3554S	† AD
	3554	**Burr-Brown (2851)**
	AM-500GC	**Datel (2861,2865)**
	AM-500MC	**Datel (2861,2865)**
	9914	OEI
600	**HA-2539**	**Harris (3402)**
500	ADLH0032	† AD
	ADLH0032C	AD
	1430	TeledyneP
	1430-83	† TeledyneP
400	**HA-2540**	**Harris (3404)**
	LH0024	† National
350	LH0032	† National
	LH0032C	National
300	HOS-050	† AD
	HOS-050A	† AD
	HOS-050C	AD
	HOS-060S	† AD
	9916	† OEI
280	HA2530	† Intersil
250(g=5)	9906	† OEI
250	3551J	Burr-Brown
	3551S	† Burr-Brown
	LH0024C	National
	1435	† TeledyneP
200	AD380	AD
	AD380S	† AD
	HA-5190	**Harris (3455)**
	HA-5195	Harris
100(g=3)	**HA-2520**	**† Harris (3400)**
	HA2520	† Intersil
100	**AD509K**	**AD (3353)**
	AD509S	**† AD (3353)**
	3550K	**Burr-Brown (2851)**
	OPA605	**Burr-Brown (2851)**
	HA-5160	**Harris (3448)**
	HA-5162	Harris
80	**AD509J**	**AD (3353)**
	3507J	**Burr-Brown (2851)**
	1322	TeledyneP
	1322-01	† TeledyneP
65	**3550J**	**Burr-Brown (2851)**
	3550S	**† Burr-Brown (2851)**

High Voltage

Maximum Supply Voltage	Device	Source
± 150	PA08	Apex
	PA83	Apex
	PA83M	† Apex
	PA84	Apex
	3582J	Burr-Brown
	3583	Burr-Brown
	3584	Burr-Brown
± 75	3581J	Burr-Brown
± 50	PA07	Apex
	PA10A	† Apex
	PA12A	† Apex
± 45	PA10	Apex
	PA12	Apex
± 40	PA9	Apex
	3571A	Burr-Brown
	3572A	Burr-Brown
	CLC210A	Comlinear
	CLC210AM	† Comlinear
	AM-464-2	**Datel (2864)**
	AM-464-2M	**† Datel (2864)**
	HA-2640	**† Harris (3412)**
	HA-2645	Harris
	LM143	† Harris
	MC1536	† Motorola
	LH0004	† National
	LH0004C	National
	LM143	† National
	LM144	† National
	LM1536	† National
	SG1536	† SiliconG
	1332	TeledyneP
± 35	3580J	Burr-Brown
± 34	MC1436	Motorola
	LM344	National
	SG1436	SiliconG
± 30	PA11	Apex
	PA73	Apex
	ICH8510I	Intersil
	ICH8510M	† Intersil
	ICH8520I	Intersil
	ICH8520M	† Intersil
	ICH8530I	Intersil
	ICH8530M	† Intersil
	~~MC1436C~~	~~Motorola~~
	LM1436	National
	LM343	National
	SG1436C	SiliconG

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers

Low Bias Current

Rated values do not usually include thermal rise due to circuit operation.

Current pA 25°C	Device	Source	
0.01	**ICH8500A**	**Intersil**	**(3477)**
0.075	**3528C**	**Burr-Brown**	**(2850)**
	AD515L	**AD**	**(3351)**
	OPA104CM	**Burr-Brown**	**(2850)**
0.1	OPA106W	† Burr-Brown	
	AM-490-2C	Datel	
	3523L	Burr-Brown	
	ICH8500	**Intersil**	**(3477)**
0.15	3528B	Burr-Brown	
	OPA106V	† Burr-Brown	
	AD515K	**AD**	**(3351)**
	OPA104BM	**Burr-Brown**	**(2850)**
0.2	ADOP-07	† AD	
	HA-5180	**Harris**	**(3452)**
	HA-5180A	**Harris**	**(3452)**
0.25	AD523L	AD	
	3523K	Burr-Brown	
0.3	3528A	Burr-Brown	
	OPA103	**Burr-Brown**	**(2850)**
	OPA106U	† Burr-Brown	
	AM-490-2B	Datel	
	AD515J	**AD**	**(3351)**
	OPA104AM	**Burr-Brown**	**(2850)**
0.5	AD504M	AD	
	AD510L	AD	
	AD517L	AD	
	3510C	Burr-Brown	
	MP517L	MicroPwr	
	MP5505A	† MicroPwr	
	LH0044A	† National	
	LH0044AC	National	
	AD523K	AD	
	3523J	Burr-Brown	
1.0	AD545K	AD	
	AD545L	AD	
	AD545M	AD	
	OPA100	**Burr-Brown**	**(2850)**
	OPA100C	Burr-Brown	
	OPA103	Burr-Brown	
	OPA105	**† Burr-Brown**	**(2853)**
	AD523J	AD	
	3522L	**Burr-Brown**	**(2850)**
	ICL8007AC	Intersil	
	ICL8007AM	† Intersil	
	LH0052	† National	
2.0	OPA100	Burr-Brown	
	OPA100B	Burr-Brown	
	3527B	**Burr-Brown**	**(2850)**
	OPA103BM	**Burr-Brown**	**(2850)**
3.0	OPA100A	Burr-Brown	
	OPA103AM	**Burr-Brown**	**(2850)**
5.0	3522K	Burr-Brown	
	3522S	Burr-Brown	
	3527A	Burr-Brown	
	3527C	Burr-Brown	
	LH0052C	National	

(Continued)

Current pA 25°C	Device	Source	
5.0			(Cont'd)
	1425-01	TeledyneP	
	1425-02	TeledyneP	
	CA3080	RCA	
	CA3080A	† RCA	
	AD506L	**AD**	**(3351)**
10.0	OPA101BM	Burr-Brown	
	OPA102BM	Burr-Brown	
	OPA106/MIL	**† Burr-Brown**	**(2853)**
	MP5507A	**† MicroPwr**	**(3529)**

Low Drift

Function	Device	Source	
0.5	AD510L	AD	
	3510C	Burr-Brown	
	LT1002A	† LinearTech	
	LT1002AC	LinearTech	
	OP05A	† LinearTech	
	LH0044B	National	
	OP-05A	† PMI	
0.6	OPA27A	† Burr-Brown	
	OPA27E	Burr-Brown	
	OPA37A	† Burr-Brown	
	OPA37E	Burr-Brown	
	AM-430B	Datel	
	AM-490-2M	† Datel	
	μA714	† Fairchild	
	HA-5130-5	Harris	
	HA-5135-5	Harris	
	HA-OP07	Harris	
	LT1001AC	LinearTech	
	LT1001AM	† LinearTech	
	LT1007AC	LinearTech	
	LT1007AM	† LinearTech	
	LT1037AC	LinearTech	
	LT1037AM	† LinearTech	
	OP05E	LinearTech	
	OP07A	† LinearTech	
	OP27A	† LinearTech	
	OP27E	LinearTech	
	OP37A	† LinearTech	
	OP37E	LinearTech	
	OP27A	† Motorola	
	OP27E	Motorola	
	OP37A	† Motorola	
	OP37E	Motorola	
	OP-05E	PMI	
	OP-07A	† PMI	
	MP5507A	† MicroPwr	
	MP5507E	**MicroPwr**	**(3529)**
1.0	AD504L	AD	
	AD504S	† AD	
	AD517K	AD	
	AD517S	† AD	
	AD547L	AD	
	3291	**Burr-Brown**	**(2850)**
	3500E	Burr-Brown	
	3510B	Burr-Brown	
	3510S	† Burr-Brown	
	3521L	Burr-Brown	
	AM-490-2A	Datel	
	μA725A	† Fairchild	
	μA725E	Fairchild	
	OP05	† LinearTech	
	MP517K	MicroPwr	
	MP517S	† MicroPwr	
	MP5505A	† MicroPwr	
	LH0044	† National	
	LH0044C	National	
	LM11	† National	
	LM11C	National	
	OP-05	† PMI	
	AD510K	**AD**	**(3351)**
	AD510S	**† AD**	**(3351)**
	LM725A	National	
1.0 (dual unit)	**MP5510A**	**† MicroPwr**	**(3529)**
	MP5510B	**MicroPwr**	**(3529)**
	MP5510E	**MicroPwr**	**(3529)**
	OP-10	† PMI	
	OP-10A	† PMI	
	OP-10E	PMI	
1.3	AM-430M	† Datel	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers (Cont'd)

Low Power Non-Adjustable

Supply Current µA ±15V	Device	Source	
9	**OP-215B**	**† PMI**	**(3566)**
	OP-215C	**† PMI**	**(3566)**
	OP-215F	**PMI**	**(3566)**
	OP-215G	**PMI**	**(3566)**
45	OP-20B	† PMI	
	OP-20C	† PMI	
	OP-20F	PMI	
	OP-20G	PMI	
	OP-20H	PMI	
65	HA-5141A	Harris	
	HA-5142A	Harris	
	HA-5144A	Harris	
80	HA-5141	Harris	
	HA-5142	Harris	
	HA-5144	Harris	
200	TL061 Series	TI	
220	**OP-420B**	**† PMI**	**(3566)**
	OP-420C	**† PMI**	**(3566)**
	OP-420F	**PMI**	**(3566)**
	OP-420G	**PMI**	**(3566)**
230	OP21A	Burr-Brown	
	OP21E	Burr-Brown	
250	OP21B	Burr-Brown	
	OP21F	Burr-Brown	
275	OP21G	Burr-Brown	
350	OP-21B	† PMI	
	OP-21F	PMI	
400	OP-21G	PMI	
	LF442A	National	
500	LF442	National	
600	µA108	† Fairchild	
	MP5512	† MicroPwr	
	OP-08	**† PMI**	**(3566)**
	OP-12	**† PMI**	**(3566)**
	LM112	† National	
	LM212	National	
	LM316A	National	
	LM108	† AMD	
	AD108	**† AD**	**(3351)**
	LM108	† Harris	
	LM108	† Intersil	
	LM108	† Motorola	
	LM108	† National	
	PM-108	**† PMI**	**(3566)**
	SG108	† SiliconG	
	SFC2108	† Thomson-CSF	

Low Power Programmable

Supply Current µA ±15V	Device	Source	
The current drain limits of these units are approximately 10-300 µA.	µA776	† Fairchild	
	LM4250	† Harris	
	ICL8021C	**Intersil**	**(3516)**
	ICL8021M	**† Intersil**	**(3516)**
	MC1776C	Motorola	
	MC3476	Motorola	
	CA3078A	**† RCA**	**(3597)**
	CA6078A	† RCA	
	SG1250	† SiliconG	
	SG2250	SiliconG	
	CA3094	† RCA	
	CA3094A	**† RCA**	**(3598)**
	CA3094B	**† RCA**	**(3598)**
The current drain limits of these units are approximately 10-300 µA.	µA776C	Fairchild	
	HA-2720	**† Harris**	**(3416)**
	HA-2725	Harris	
	LM4250C	Harris	
	ICL4250	† Intersil	
	ICL4250C	† Intersil	
	MC1776	† Motorola	
	LM4250	† National	
	LM4250C	† National	
	SG3250	SiliconG	
	SG4250	† SiliconG	
	SG4250C	† SiliconG	
	CA3078	**† RCA**	**(3597)**
	UC4250	† Solitron	
	UC4250C	Solitron	
The current drain limits of these units are approximately 1-2000 µA.	**OP-32**	**PMI**	**(3566)**

Low Power µA @ ±8V

Supply Current µA ±15V	Device	Source	
20	**ICL7611M**	**† Intersil**	**(3481)**
	ICL7631M	**† Intersil**	**(3481)**
	ICL7632M	**† Intersil**	**(3481)**
	ICL7642M	**† Intersil**	**(3481)**
200	**ICL7612M**	**† Intersil**	**(3481)**
	ICL7613C	**Intersil**	**(3481)**
	ICL7613M	**† Intersil**	**(3481)**
	ICL7614C	**Intersil**	**(3481)**
	ICL7615C	**Intersil**	**(3481)**
	ICL7621C	**Intersil**	**(3481)**
	ICL7622C	**Intersil**	**(3481)**
	ICL7631C	**Intersil**	**(3481)**
	ICL7642C	**Intersil**	**(3481)**
	ICL7612C	**Intersil**	**(3481)**
	ICL7611C	**Intersil**	**(3481)**

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers (Cont'd)

Programmable

Function	Device	Source	
Adjustable Current/Performance			
Single (1 unit per package)			
	LM4250	† Harris	
	ICL7611M	† Intersil	
	ICL7612M	† Intersil	
	ICL7613C	Intersil	
	ICL7613M	† Intersil	
	ICL8021C	Intersil	
	ICL8021M	† Intersil	
	MC1776C	Motorola	
	MC3476	Motorola	
	CA3078A	† RCA	
	SG1250	† SiliconG	
	SG2250	SiliconG	
	ICL7612C	Intersil	
	CA3094	† RCA	
	CA3094A	† RCA	
	CA3094B	† RCA	
	μA776C	Fairchild	
	μA776M	† Fairchild	
	HA-2720	† Harris	
	HA-2725	Harris	
	LM4250C	Harris	
	ICL4250	† Intersil	
	ICL4250C	† Intersil	
	ICL7611C	Intersil	
	MC1776	† Motorola	
	LM4250	† National	
	LM4250C	† National	
	CA3080	RCA	
	CA3080A	† RCA	
	SG3250	SiliconG	
	SG4250	† SiliconG	
	SG4250C	† SiliconG	
	CA3078	† RCA	
Dual (2 units per package)			
	HA-2730	† **Harris**	**(3419)**
	HA-2735	Harris	
	ICL8022C	**Intersil**	**(3516)**
	ICL8022M	† **Intersil**	**(3516)**
	LH24250	† National	
	LH24250C	National	
Triple (3 units per package)			
	ICL7632C	**Intersil**	**(3481)**
	ICL7632M	† Intersil	
	ICL8023C	**Intersil**	**(3516)**
	ICL8023M	† **Intersil**	**(3516)**
	CA3060A	**RCA**	**(3597)**
	CA3060B	**RCA**	**(3597)**
	SG1253	† SiliconG	
	SG2253	SiliconG	
	SG3253	SiliconG	

(Continued)

Function	Device	Source	
Triple (3 units per package) (Cont'd)			
	L144A	† **Siliconix**	**(3083)**
	L144B	**Siliconix**	**(3083)**
	L144C	**Siliconix**	**(3083)**
	CA3060	† **RCA**	**(3597)**
Quad (4 units per package)			
	XR246	**Exar**	**(3377)**
	XR346	**Exar**	**(3377)**
	XR4202	**Exar**	**(3378)**
	XR4202M	† **Exar**	**(3378)**
	HA-2740	**Harris**	**(3422)**
	MC3575	† Motorola	
	LM146	† National	
	LM246	National	
	LM346	National	
	LM146	Raytheon	
	LM246	Raytheon	
	LM346	Raytheon	
	XR146	† **Exar**	**(3377)**

Single Supply

Single Units

Supply Voltage, V	Device	Source	
to 24	CA3094	† RCA	
to 30	OP-32	PMI	
to 36	μA759	† Fairchild	
	μA759C	Fairchild	
	CA3140	† RCA	
	CA3094A	† RCA	
to 44	CA3094B	† RCA	
1 to 16	ICL7612M	† Intersil	
	ICL7612C	Intersil	
2 to 30	HA-5141	Harris	
5 to 16	OP-20B	† PMI	
	OP-20C	† PMI	
	OP-20F	PMI	
	OP-20G	PMI	
	OP-20H	PMI	
	CA3130	† **RCA**	**(3596)**
	CA3130A	† **RCA**	**(3596)**

Dual Units

(Continued on next page)

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† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers (Cont'd)

Single Supply
Dual Units

Supply Voltage, V	Device	Source
to 20	OP-215B	† PMI
	OP-215C	† PMI
	OP-215F	PMI
	OP-215G	PMI
2 to 30	HA-5142	Harris
3 to 26	HA17902	Hitachi
	LM2902	Motorola
	LM2904	Motorola
	LM2902	National
	LM2904	National
	LM2902	Raytheon
	CA2904	RCA
	LM2902	TI
	LM2904	TI
	TDF2904	Thomson-CSF
3 to 30	LM158A	† National
	LM358	National
	CA358	RCA
	LM358	Signetics
	LM358	TI
	LM158	† Motorola
	LM258	Motorola
	LM358	Motorola
	LM158	† National
	LM258	National
	LM258A	National
	LM358A	National
	CA158	† RCA
	CA258	RCA
	LM158	† Signetics
	LM258	Signetics
	NE532	Signetics
	SE532	**† Signetics (526)**
	LM158	† TI
	TL321C	TI
	TL321M	† TI
3 to 36	µA798	Fairchild
	MC3458	Motorola
4 to 36	**CA3240**	**RCA (3595)**
5 to 30	**OP-220**	**PMI (3566)**
	OP-221	PMI
8 to 36	TBA231	SGS

Single Supply
Quad Units

Supply Voltage, V	Device	Source
2 to 30	HA-5144	Harris
3 to 26	TDF2902	Thomson-CSF
3 to 30	µA124	† Fairchild
	µA224	Fairchild
	µA324	Fairchild
	LM124	† Intersil
	LM324	Intersil
	LM124	† Motorola
	LM224	Motorola
	LM324	Motorola
	LM124	† National
	LM224	National
	LM324	National
	µPC324	NEC
	LM124	† Raytheon
	LM224	Raytheon
	LM324	Raytheon
	CA124	† RCA
	CA224	RCA
	CA324	RCA
	LM124	† Signetics
	LM224	Signetics
	LM324	Signetics
	SG124	† SiliconG
	SG224	SiliconG
	SG324	SiliconG
	LM124	† TI
	LM224	TI
	LM258	TI
	LM324	TI
3 to 36	**XR3403**	**Exar (3378)**
	XR3503	**† Exar (3378)**
	µA3303C	Fairchild
	µA3403C	Fairchild
	MC3303	Motorola
	MC3403	Motorola
	MC3503	† Motorola
	RC3403	Raytheon
	RM3503	† Raytheon
3 to 44	MC33074	Motorola
	MC34074	Motorola
	MC35074	† Motorola
4 to 18	MC3401	Motorola
	LM3401	National
	RC3401	Raytheon
	CA3401	† RCA
4 to 28	MC3301	Motorola
	LM3301	National
	RC3301	Raytheon
4 to 32	LM2900	National
	LM3900	National
	LM2900	Raytheon
	LM3900	Raytheon
	LM2900	TI
	LM3900	TI
4 to 36	LM1900	TI
5 to 30	OP-420B	† PMI
	OP-420C	† PMI
	OP-420F	PMI
	OP-420G	PMI

Wide Band

Unity Gain Bandwidth MHz	Device	Source
40 *	**AD380J**	**AD (3353)**
	AD380K	AD
	AD380L	AD
	AD380S	† AD
	HA-2400	† Harris
	HA-2404	Harris
	HA-2405	Harris
50 *	3551J	Burr-Brown
	3551S	† Burr-Brown
	CA3015	† RCA
	CA3015A	† RCA
	CA3030	RCA
	CA3030A	RCA
	CA3038	† RCA
	CA3038A	† RCA
60 *	1430	TeledyneP
	1430-83	† TeledyneP
65 *	µA715C	Fairchild
	µA715M	† Fairchild
70	**HA-5112**	**Harris (3459)**
	HA-5114	**Harris (3459)**
70 *	OPA605	Burr-Brown
	3554A	Burr-Brown
	3554B	Burr-Brown
	3554S	Burr-Brown
	LH0032	† National
	LH0032C	National
	ADLH0032	**† AD (3353)**
	ADLH0032C	**AD (3353)**
	LH0024	† National
	LH0024C	National
70 (−3db)	CLC210A	Comlinear
	CLC210AM	† Comlinear
90 *	AD3554	AD
	AD3554S	† AD
100	AM-500GC	Datel
	AM-500MC	Datel
	HA-5160	Harris
	HA-5162	Harris
	9906	† OEI
	NE5539	**Signetics (3678)**
	SE5539	**† Signetics (526,3678)**
100 *	HOS-050	† AD
	HOS-050C	AD
	HOS-060S	† AD
	HA-2620	† Harris
	HA-2622	† Harris
	HA-2625	Harris
100 (−3db)	CLC200A	Comlinear
	CLC200AM	† Comlinear
150 (−3db)	CLC103A	Comlinear
	CLC103AM	† Comlinear
200	9918	OEI
	9916	† OEI
200 (−3db)	CLC220A	Comlinear
	CLC220AM	† Comlinear
300	9914	OEI
400 *	HA-2540	Harris
500 *	1435	† TeledyneP
600 *	HA-2539	Harris
1000	**OPA600/MIL**	**Burr-Brown (2853)**

† Military Temperature Range (−55° to 125°C)

* Typical Value

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Master Selection Guide

LINEAR–Operational Amplifiers–Characteristics

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift μV/°C	Band-width MHz	Slew Rate V/μs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source
Single Units											
In this list the "Comp." column indicates the number of compensation components required at unity gain. Thus 0 indicates a fully compensated amplifier. The bandwidth and slew rate are listed with the amplifier compensated for unity gain.											
0.005	0.01	—	—	0.3 *	1 *	10M	110	0	Chopper Stabilized	TML7650-1	Telmos
				2.0 *	2.5 *	10M	120	0	Chopper Stabilized	TML7650	Telmos
		0.0005	0.05	2	2.5	10M	120	0	Chopper Stabilized	**TSC7650**	**TeledyneS (3096)**
		0.0005 *	0.05	2 *	2.5 *	5M	130 *	1	Chopper Stabilized	**AM-7650**	**Datel (2865)**
		0.005	0.01	2.0 *	2.5 *	10M	120	0	Chopper Stabilized	**ICL7650C**	**Intersil (3488)**
	3	—	0.1	0.3	—	30K	88 *	0	Commutating Auto Zero, Compensated	ICL7600C	Intersil
										ICL7600M	† Intersil
									Commutating Auto Zero, Uncompensated	ICL7601C	Intersil
										ICL7601M	† Intersil
0.01 *	10	—	0.2 *	8 *	2.8 *	1.5M *	120	0	Ultra-Low Noise	**MP5527**	**MicroPwr (3529)**
		-		63 *	17 *	1.5M *	120	0	Ultra-Low Noise	**MP5537**	**MicroPwr (3529)**
0.015	1	—	0.1	—	—	—	140	0	Instrumentation, 50 mA output	**AMP-01**	**† PMI (3568)**
	2	2	0.6	0.4	0.1	450K	114	0	Ultra Low Offset, Low Drift	LT1001AM	† LinearTech
0.020 *	0.15 *	0.05 *	0.1	3 *	2.5 *	1M	120	3	Chopper Stabilized	**AM-490-2C**	**Datel (2865)**
			0.3	3 *	2.5 *	1M	120	3	Chopper Stabilized	**AM-490-2B**	**Datel (2865)**
			0.6	3 *	2.5 *	1M	120	3	Chopper Stabilized	**AM-490-2M**	**† Datel (2865)**
			1.0	3 *	2.5 *	1M	120	3	Chopper Stabilized	**AM-490-2A**	**Datel (2865)**
0.025	1	0.25	0.5	0.25 *	0.1 *	1M	110	0	Ultra Low Offset Voltage, Low Drift	**AD517L**	**AD (3351)**
										MP517L	MicroPwr
	2	2	0.6	0.4	0.1	450K	114	0	Ultra Low Offset, Low Drift	LT1001AC	LinearTech
				0.6 *	0.17 *	300K	110	0	Ultra Low Offset Voltage, Low Drift	**ADOP-07A**	**† AD (3351)**
										OP-07A	† Intersil
					0.5	1M	110	0	Ultra Low Offset Voltage, Low Drift	HA-OP07A	Harris
										HA-OP07E	Harris
				1.2 *	0.25 *	300K	110	0	Ultra Low Offset Voltage, Low Drift	MP5507A	† MicroPwr
										OP-07A	**† MicroPwr (3529)**
										OP-07A	**† PMI (3566)**
				2.5 *	0.8 *	1M	100	0	Ultra Low Offset Voltage, Low Drift	**HA-5130-2**	**Harris (3444)**
										HA-5135-2	Harris
										HA-5130-5	**Harris (3444)**
										HA-5135-5	Harris
	10	2.5	2	0.3 *	0.1 *	1M	110	0	Trimmed Offset	**AD510L**	**AD (3351)**
	15	2.5	0.5	0.4 *	0.06 *	1M	120	1	Precision, Low Noise	LH0044A	† National
										LH0044AC	National
	20	20	0.75	—	—	5-1000	100	0	Instrumentation (2 amps available as pair)	**3629B**	**† Burr-Brown (2851)**
	25	30	0.5	—	—	5-1000	100	0	Instrumentation (2 amps available as pair)	**3629C**	**Burr-Brown (2851)**
										3629S	**† Burr-Brown (2851)**
	35	50	3	—	—	5-1000	100	0	Instrumentation (2 amps available as pair)	**3629A**	**Burr-Brown (2851)**
	40	35	—	63 *	11 *	—	—	0	Low Noise, High Slew Rate	**OP-37A**	**† Raytheon (3592)**
			0.2	25 *	18 *	1M	—	0	Ultra Low Noise, Low Offset	**OP-37A**	**† PMI (3566)**
										OP-37E	**PMI (3566)**
			0.6	5	1.7	1M	114	0	Ultra Low Noise	**AM-427-B**	**Datel (2864)**
										OP-27A	LinearTech
										OP-27E	LinearTech
										OP-27A	† Motorola
										OP-27E	Motorola
										OP-27A	**† PMI (3566)**
										OP-27E	**PMI (3566)**
						600K	114	0	Ultra Low Noise	**OP-27A**	**† Raytheon (3592)**
										OP-27E	**Raytheon (3592)**
				8 *	1.7	1000K	114	0	Ultra Low Noise	**OPA27A**	**† Burr-Brown (2850)**
										OPA27E	**Burr-Brown (2850)**
				40 *	11	1000K	114	0	Ultra Low Noise	**OPA37A**	**† Burr-Brown (2850)**
										OPA37E	**Burr-Brown (2850)**
				45	11	1M	114	0	Ultra Low Noise, Gain >5	OP-37A	† LinearTech
										OP-37E	LinearTech
										OP-37A	† Motorola
										OP-37E	Motorola

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers–Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift μV/°C	Band-width MHz	Slew Rate V/μs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source
Single Units											**(Cont'd)**
0.05	0.014	0.014	45	7	13 *	128	86	0	High Speed Instrumentation	AM-543MM	† Datel
										AM-543MR	Datel
	0.05	0.05	45	7	13 *	128	86	0	High Speed Instrumentation	AM-543MC	Datel
	2	0.75	1	0.25 *	0.1 *	1M	100	0	Ultra Low Offset Voltage, Low Drift	AD517K	AD (3351)
										AD517S	† AD (3351)
										MP517K	MicroPwr
										MP517S	† MicroPwr
	5	0.5	0.5	0.2	—	2M	126	0	Precision Instrumentation	LM163A	† National
										LM363A	† National
	13	4.0	1	0.3 *	0.1 *	1M	110	0	Trimmed Offset	AD510K	AD
										AD510S	† AD
	14	14	1	0.5 *	—	1024	86	0	Low Drift Instrumentation	AM-542MM	† Datel
										AM-542MR	Datel
	15	10	0.5	—	5	1000	90	0	Precision Insrumentation	AD524C	AD (3354)
	30	—	0.2	0.25	5	1K	115	0	Precision Instrumentation	AD624C	AD (3355)
		5	0.5	0.4 *	0.06 *	500K	114	1	Precision, Low Noise	LH0044B	National
			1	0.4 *	0.06 *	500K	114	1	Precision, Low Noise	LH0044	† National
	50	50	1	0.5 *	—	1024	86	0	Low Drift Instrumentation	AM-542MC	Datel
0.06	4	3.8	1	0.4	0.1	400K	110	0	Low Offset Voltage	LT1001C	LinearTech
										LT1001M	† LinearTech
	15	10	0.5	0.4 *	0.5 *	1M	110	1	Low Drift	3510C	Burr-Brown (2850,2853)
	55	50	—	63 *	11 *	—	—	0	Low Noise, High Slew Rate	OP-37B	† Raytheon (3592)
										OP-37F	Raytheon (3592)
			1.3	5	1.7	1M	106	0	Ultra Low Noise	OPA27B	† Burr-Brown (2850)
										OPA27F	Burr-Brown (2850)
										OP-27B	† Motorola
										OP-27F	Motorola
										OP-27B	PMI (3566)
										OP-27F	PMI (3566)
										OP-27B	† Raytheon (3592)
										OP-27F	Raytheon (3592)
				40 *	11	1000K	106	0	Ultra Low Noise	OPA37B	† Burr-Brown (2850)
										OPA37F	Burr-Brown (2850)
				45	11	1M	106	0	Ultra Low Noise, Gain >5	OP-37B	† Motorola
										OP-37F	Motorola
										OP-37B	† PMI (3566)
										OP-37F	PMI (3566)
0.075	3	2.8	1.3	0.4	0.1	200K	110	0	Low Offset Voltage	OP-07	† LinearTech
				0.6 *	0.17 *	200K	110	0	Ultra Low Offset Voltage, Low Drift	OP-07	† Intersil
										ADOP-07	† AD (3351)
					0.5	1M	110	0	Ultra Low Offset Voltage, Low Drift	HA-OP07	Harris
				1.2 *	0.25 *	200K	110	0	Ultra Low Offset Voltage, Low Drift	MP5507B	† MicroPwr (3529)
										OP-07	† MicroPwr (3529)
										OP-07	† PMI (3566)
										RC714	† Raytheon (3592)
										RC714C	Raytheon (3592)
										RC714E	Raytheon (3592)
										μA714	† Fairchild
	4	3.8	0.2	0.4	0.2	150K	106	0	Ultra-Low Offset Voltage	OP-07E	TI
			1.3	0.4	0.1	200K	110	0	Low Offset Voltage	OP-07E	LinearTech
				0.6 *	0.17 *	200K	123 *	0	Ultra Low Offset Voltage, Low Drift	ADOP-07E	AD (3351)
										OP-07E	Intersil
				1.2 *	0.25 *	200K	106	0	Ultra Low Offset Voltage, Low Drift	μA714E	Fairchild
										MP5507E	MicroPwr
										OP-07E	MicroPwr (3529)
										OP-07E	PMI (3566)
		6	1.3	0.6 *	0.5	1M	106	0	Ultra Low Offset Voltage, Low Drift	HA-OP07C	Harris
	15	3	2	1.2 *	0.25 *	1M	120	0	Precision Instrumentation	CA3193B	† RCA (3594)
										CA3493B	† RCA (3594)
0.08	0.050	0.01	1.5	1 *	0.3 *	500K	114	0	Improved LM11	LM11A	† National
	1	0.5	0.2 *	3 *	2.5 *	1M	120	3	Chopper Stabilized	AM-490	Datel (2865)
										1340	TeledyneP
	15	0.5	1.5	0.1 *	—	1M	105	0	Precision, Low Power	OP-20B	† PMI (3566)
										OP-20F	PMI (3566)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers–Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift μV/°C	Band-width MHz	Slew Rate V/μs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source
Single Units											**(Cont'd)**
0.10	3	2.8	0.4 *	1.2 *	0.25 *	500K	—	0	Ultra Low Offset Voltage	**OP-207A**	† **PMI (3566)**
										OP-207B	**PMI (3566)**
	5	1	3	0.2 *	—	2M	120	0	Precision Instrumentation	LM163	† National
	20	15	0.5	—	5	1000	90	0	Precision Insrumentation	**AD524B**	**AD (3354)**
	25	0.7	1	0.5 *	49	1000K	95	1	Selectable Input	**OPA201C**	**Burr-Brown (2850)**
		1	1	0.3 *	0.2	1M	100	0	Low Power	**OPA21A**	**Burr-Brown (2850)**
										OPA21E	**Burr-Brown (2850)**
		5	3	3 *	0.1 *	250K	94	0	Trimmed Offset	**AD510J**	**AD (3351)**
	35	5	1	0.4 *	0.06 *	500K	114	1	Precision, Low Noise	LH0044C	National
	40	1	0.8	—	1.7	1800	114	0	Ultra Low Noise	**OP-27**	**MicroPwr (3529)**
	50	—	0.5	0.25	5	1K	110	0	Precision Instrumentation	**AD624B**	**AD (3355)**
		35	0.5	—	5	1000	90	0	Precision Insrumentation	**AD524S**	† **AD (3354)**
	70	1	0.8	—	0.01	100K	120	4	High Gain Instrumentation	**OP-06A**	† **PMI (3566)**
	80	40	0.4 *	8 *	17	1800	114	0		**OP-37**	**MicroPwr (3529)**
		75	—	63 *	11 *	—	—	0	Low Noise, High Slew Rate	**OP-37C**	† **Raytheon (3592)**
										OP-37G	**Raytheon (3592)**
			0.4 *	8 *	3.2 *	1200K	120	0	Ultra Low Noise	OP-27G	Motorola
										OP-27G	**PMI (3566)**
						1200K *	120	0	Ultra Low Noise	OP-27C	Motorola
										OP-27C	**PMI (3566)**
				25 *	18 *	700K	120	0	Ultra Low Noise	**OP-37C**	† **PMI (3566)**
										OP-37G	**PMI (3566)**
			1.8	5	1.7	200K	100	0	Ultra Low Noise	**AM-427-A**	**Datel (2864)**
										AM-427-M	† **Datel (2864)**
						300K	100	0	Ultra Low Noise	**OP-27C**	† **Raytheon (3592)**
										OP-27G	**Raytheon (3592)**
						700K	100	0	Ultra Low Noise	OP-27C	† LinearTech
										OP-27G	LinearTech
				8 *	1.7	700K	100	0	Ultra Low Noise	**OPA27C**	† **Burr-Brown (2850)**
										OPA27G	**Burr-Brown (2850)**
										OPA37C	† **Burr-Brown (2850)**
										OPA37G	**Burr-Brown (2850)**
				45	11	700K	100	0	Ultra Low Noise, Gain > 5	OP-37C	† LinearTech
										OP-37G	LinearTech
									Ultra Low Noise, Gain >5	OP-37C	† Motorola
										OP-37G	Motorola
	100	—	1	0.25	5	1K	100	0	Precision Instrumentation	**AD624S**	† **AD (3355)**
	150	15	0.5	0.6 *	0.25	2M	110	0	Precision, Low Power	**OP-21B**	† **PMI (3566)**
										OP-21F	**PMI (3566)**
0.12	25	15	1	0.4 *	0.5	1M	110	1	Low Drift	**3510B**	**Burr-Brown (2850,2853)**
										3510S	† **Burr-Brown (2850,2853)**
			2	0.25	0.5	1M	110	1	Precision, Low Drift	**3510V**	† **Burr-Brown (2850,2853)**
0.13	12	6	0.2	0.4	0.2	100K	110	0	Low Offset Voltage	OP-07D	TI
0.15	0.075	0.01	0.7 *	1 *	0.3 *	500K	114	0	Improved LM11	LM11AC	National
	2	0.2	2.5	0.8 *	0.12 *	80K	104	0	Improved 108 A, Low Bias, Compensated	**OP-12A**	† **PMI (3566)**
										OP-12E	**PMI (3566)**
								1	Improved 108 A, Low Bias	**OP-08A**	† **PMI (3566)**
										OP-08E	**PMI (3566)**
							110	1	Improved 108 A, Low Bias	**MPOP-08A**	† **MicroPwr (3529)**
										MPOP-08E	**MicroPwr (3529)**
		2	0.9	0.4	0.1	300K	114	0	Instrumentation	OP-05A	† LinearTech
				0.5 *	0.1	500K	114	0	Ultra Low Noise	**OP-05A**	† **Raytheon (3592)**
				0.6	0.17	300K	126	0	Low Bias, Low Drift	OP-05A	† Intersil
				1.2 *	0.25 *	300K	114	0	Instrumentation	**OP-05A**	† **MicroPwr (3529)**
										MP5505A	† **MicroPwr (3529)**
										OP-05A	† **PMI (3566)**
	5	1	3	0.25 *	0.1 *	1M	94	0	Ultra Low Offset Voltage, Low Drift	**AD517J**	**AD (3351)**
										MP517J	MicroPwr
	7	6	0.2	0.4	0.2	100K	100	0	Ultra-Low Offset Voltage	OP-07C	TI

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers–Characteristics (Cont'd)

Single Units (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift μV/°C	Band-width MHz	Slew Rate V/μs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source
0.15	7	6									(Cont'd)
			1.8	0.4	0.1	120K	100	0	Low Offset Voltage, Low Drift	OP-07C	LinearTech
				0.5 *	0.1	100K	100	0	Ultra Low Noise	**OP-07C**	**Raytheon (3592)**
				0.6 *	0.17 *	120K	100	0	Ultra Low Offset Voltage, Low Drift	**ADOP-07C**	**AD (3351)**
										OP-07C	Intersil
				1.2 *	0.25 *	120K	100	0	Ultra Low Offset Voltage, Low Drift	**OP-07C**	**MicroPwr (3529)**
	7.0	6.0	0.5 *	0.5 *	0.17 *	120K	100	0	Low Noise	μPC354	NEC
	12	6	2.5	0.5 *	0.1	100K	94	0	Ultra Low Noise	**OP-07D**	**Raytheon (3592)**
				0.6 *	0.17 *	120K	94	0	Ultra Low Offset Voltage, Low Drift	**ADOP-07D**	**AD (3351)**
										OP-07D	Intersil
				1.2 *	0.25 *	120K	94	0	Ultra Low Offset, Low Drift	**MP5507D**	**MicroPwr (3529)**
										OP-07D	**PMI (3566)**
	35	20	2	0.4 *	0.5 *	1M	110	1	Low Drift	**3510A**	**Burr-Brown (2850,2853)**
	100	4	1	0.6	0.25 *	1M	100	0	High Speed, Low Power	**OP-21A**	**PMI (3566)**
										OP-21E	**PMI (3566)**
0.17	85	90	2	5	1.7	50K	100	1	Ultra Low Noise	OP-24G	Motorola
0.20	7	6	0.7 *	1.2 *	0.25 *	400K	—	0	Ultra Low Offset Voltage	**OP-207E**	**PMI (3566)**
										OP-207F	**PMI (3566)**
	10	3	3	0.2 *	—	1M	114	0	Precision Instrumentation	LM363	National
	15	15	2	0.3 *	0.1 *	1-1000	80	0	Instrumentation	AD522B	AD
	20	5	3	1.2 *	0.25	300K	110	0	Precision, Instrumentation	**CA3193A**	**RCA (3594)**
	25	2.5	5	0.1 *	—	400K	100	0	Precision, Low Power	**OP-20C**	† **PMI (3566)**
										OP-20G	**PMI (3566)**
		20	6	0.3 *	0.1 *	1-1000	75	0	Instrumentation	AD522S	† AD
	40	2	2	0.3 *	0.2	500K	90	0	Low Power	**OPA21B**	**Burr-Brown (2850)**
										OPA21F	**Burr-Brown (2850)**
				0.5 *	49	1000K	90	1	Selectable Input	**OPA201B**	**Burr-Brown (2850)**
										OPA201S	† **Burr-Brown (2850)**
	200	20	0.5	0.6 *	0.25	1.5M	105 *	0	Precision, Low Power	**OP-21G**	**PMI (3566)**
0.25	0.0001	0.00004	5	1 *	1.2	150K	76	0	Ultra Low Bias Military	**OPA106W**	† **Burr-Brown (2853)**
	0.00015	0.00004	5	0.5 *	0.3	—	80	—	Ultra Low Bias FET	**3528B**	**Burr-Brown (2850)**
		0.00008	10	1 *	1.2	150K	76	0	Low Bias Military	**OPA106V**	† **Burr-Brown (2853)**
	0.0003	0.00008	50	1 *	1.2	150K	76	0	Low Bias Military	**OPA106U**	† **Burr-Brown (2853)**
	0.001	0.0002	2	1 *	0.9	100K	76	0	Low Bias, FET Input	**OPA105W**	† **Burr-Brown (2853)**
						200K	76	0	Low Drift, Low Bias FET	**OPA103DM**	**Burr-Brown (2850)**
			5	1 *	0.9	100K	76	0	Low Bias, FET Input	**OPA105V**	† **Burr-Brown (2853)**
						200K	76	0	Low Drift, Low Bias FET	**OPA103CM**	**Burr-Brown (2850)**
			25	1 *	0.9	100K	76	1	Low Bias, FET Input	**OPA105UM**	† **Burr-Brown (2853)**
		0.0005	3	0.7 *	0.3	40K	76	0	Precision, Low Drift FET	**AD545M**	**AD (3351)**
			5	1 *	0.6	200K	94	0	Low Bias FET	**OPA100C**	**Burr-Brown (2850)**
	0.002	0.0003 *	5	1 *	0.6	100K	76 *	0	Low Drift FET	3527B	Burr-Brown
	0.010	0.002 *	1	1.5 *	0.6	100K	90 *	0	Ultra Low Drift FET	**3521L**	**Burr-Brown (2850)**
		0.004	5 *	10	5	50K	80	0	Low Noise, Wideband JFET	**OPA101BM**	**Burr-Brown (2850)**
										OPA102BM	**Burr-Brown (2850)**
	0.015	0.002 *	2	1.5 *	0.6	100K	90 *	0	Ultra Low Drift FET	**3521K**	**Burr-Brown (2850)**
	0.020	0.020 *	5	1.5 *	0.6	50K	90 *	0	Ultra Low Drift FET	**3521J**	**Burr-Brown (2850)**
										3521R	† **Burr-Brown (2850)**
	0.025	0.002	1	1	3	250K	80	2	Ultra Low Drift BIFET	**AD547L**	**AD (3350,3351)**
	2	2	0.6	0.5 *	0.1	150K	110	0	Ultra Low Noise	**OP-07A**	† **Raytheon (3592)**
				2.5 *	0.5	1M	100	0	Ultra Low Drift	**AM-430B**	**Datel (2864)**
		6	0.6	0.4	0.1	300K	110	0	Ultra Low Offset, Low Drift	OP-07A	LinearTech
	40	35	—	63 *	11 *	—	—	0	Low Noise, High Slew Rate	**OP-37E**	**Raytheon (3592)**
	50	0.005	5	5 *	30 *	60K	80	—	High Speed, Low Drift FET	**AD381L**	**AD (3353)**
		35	0.5	—	5	1000	90	0	Precision Instrumentation	**AD524A**	**AD (3354)**
	100	—	1	0.25	5	1K	100	0	Precision Instrumentation	**AD624A**	**AD (3355)**
0.30	0.050	0.010	1 *	1 *	0.3	100K	110	0	Improved 108 A, Low Power	LM11	Motorola
										LM11	† National
	0.1	0.03	5	3	10	100K	90	—	Precision JFET	MA337	AnalogSys
	2	0.2	3.5	0.8 *	0.12 *	80K	104	0	Improved 108 A, Low Power, Compensated	**OP-12B**	† **PMI (3566)**
										OP-12F	**PMI (3566)**
											(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers–Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift μV/°C	Bandwidth MHz	Slew Rate V/μs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source
Single Units											**(Cont'd)**
0.30	2	0.2	3.5	0.8 *	0.12 *	80K	104				(Cont'd)
								1	Improved 108 A, Low Power	**OP-08B**	**† PMI (3566)**
										OP-08F	**PMI (3566)**
									Improved 108 A, Low Dias	**MPOP-08B**	**† MicroPwr (3529)**
										MPOP-08F	**MicroPwr (3529)**
	5	1	1.5	—	0.7 *	1M	100	0	Programmable Micropower	**OP-32E**	**PMI (3566)**
			2	—	0.7 *	1M	100	0	Programmable Micropower	**OP-32A**	**† PMI (3566)**
	25	2	5	0.1 *	—	500K	90	0	Precision, Low Power	**OP-20H**	**PMI (3566)**
	1000	200	2	20	10	10K	90	1	Precision, Bipolar	MA327	AnalogSys
0.35	3	2	0.2	2.5	0.12 *	300K	104		Low Bias Current	**MP5508**	**MicroPwr (3529)**
0.40	5	1	1.5	0.25	0.08	900K *	82	0	Programmable Micropower	**OP-22A**	**PMI (3566)**
	25	20	6	0.3 *	0.1 *	1-1000	75	0	Instrumentation	AD522A	AD
0.5	0.000075	0.00002	10	0.5 *	0.3	—	70	—	Ultra Low Bias FET	3528C	Burr-Brown
		0.00004	10	1 *	1.6 *	100K	80	0	Ultra Low Bias FET	OPA104CM	Burr-Brown
	0.0001	0.00005	25	1 *	0.6	100K	80 *	0	Ultra Low Bias FET	3523L	Burr-Brown
	0.00015	0.00008	15	1 *	1.6 *	100K	66	0	Ultra Low Bias FET	OPA104BM	Burr-Brown
	0.00025	0.0001	25	1 *	0.6	100K	80 *	0	Ultra Low Bias FET	3523K	Burr-Brown
	0.0003	0.00008	10	0.5 *	0.3	—	66	—	Ultra Low Bias FET	**3528A**	**Burr-Brown (2850)**
	0.001	0.0001	5	1 *	1.5	100K	80	0	Precision FET	LH0052	† National
		0.0002	5	2	7	1M	110			1347	TeledyneP
										1347-01	† TeledyneP
			5 *	0.11	4	1M	90	1	Low Bias Current, Low Power	**HA-5180A-2**	**Harris (3452)**
										HA-5180A-5	**Harris (3452)**
		0.002 *	15	1 *	0.9	200K	76	0	Low Drift, Low Bias FET	OPA103BM	Burr-Brown
	0.002	0.0005	10	1 *	0.6	100K	88	0	Low Bins FET	**OPA100S**	**† Burr-Brown (2850)**
										OPA100B	**Burr-Brown (2850)**
		0.003 *	25	1 *	0.9	200K	76	0	Low Drift, Low Bias FET	OPA103AM	Burr-Brown
	0.005	0.0003 *	2	1 *	0.6	100K	76 *	0	Ultra Low Drift FET	**3527C**	**Burr-Brown (2850)**
			10	1 *	0.6	100K	76 *	0	Low Drift FET	**3527A**	**Burr-Brown (2850)**
		0.001 *	25	1 *	0.6	50K	90 *	0	Low Offset FET	**3522K**	**Burr-Brown (2850)**
										3522S	**Burr-Brown (2850)**
	0.01	0.01	10	—	20	800K	96	0	to ± 150V supply, 150mA output	PA08A	Apex
				1.3 *	3.5	100K	120 *	0	to ± 50V supply, 5A output	PA07A	Apex
	0.015	0.006	10 *	10 *	6.5 *	50K	80	0	Low Noise, Wideband JFET	**OPA101AM**	**Burr-Brown (2850)**
										OPA102AM	**Burr-Brown (2850)**
	0.02	0.01	10	—	100 *	—	104 *	2	to ± 50V supply, 4A output	PA09A	Apex
	0.020	0.002 *	10	1.5 *	0.6	50K	90 *	0	Ultra Low Drift FET	**3521H**	**Burr-Brown (2850)**
	0.025	0.002	2	1	3	250K	80	2	Ultra Low Drift BIFET	**AD547K**	**AD (3350,3351)**
			5	1	3	250K	80	2	Ultra Low Drift BIFET	**AD547S**	**AD (3350,3351)**
				2.0	17 *	50K	80	0	High Speed Precision Bipolar JFET	**AD544L**	**AD (3351)**
				5 *	30 *	40K	80	1	High Speed, Low Drift FET	**AD382T**	**† AD (3353)**
						60K	80	—	High Speed, Low Drift FET	**AD381T**	**† AD (3353)**
			10	5 *	30 *	40K	80	1	High Speed, Low Drift FET	**AD382K**	**AD (3353)**
						60K	80	—	High Speed, Low Drift FET	**AD381K**	**AD (3353)**
		0.010	5	1.0 *	3	200K	80	0	Precision Bipolar JFET	**AD542L**	**AD (3351)**
		0.03	3	5 *	0.11	5	100K	100	Precision JFET Input	**HA-5170-2**	**† Harris (3450)**
	0.035	0.002	5	1.5 *	94 *	10K	80	1	Wideband, Fast Settling	**OPA605C**	**Burr-Brown (2851)**
										OPA605K	**Burr-Brown (2851)**
			10	1.5 *	94 *	10K	80	1	Wideband, Fast Settling	**OPA605B**	**Burr-Brown (2851)**
										OPA605J	**Burr-Brown (2851)**
	0.050	0.01	5	—	45	100K	86	—	Wideband, Decompensated, Settles to 0.01% in 1.5 μs	OP-17A	† MicroPwr
										OP-17E	MicroPwr
										OP-17A	**† PMI (3566)**
										OP-17E	**PMI (3566)**
				14 *	10	100K	86	0	Bipolar-JFET, Bias Comp.	OP-15A	† MicroPwr
										OP-15E	MicroPwr
										OP-15A	**† PMI (3566)**
										OP-15E	**PMI (3566)**
				19 *	18	100K	86	0	Wideband-JFET, Bias Comp.	OP-16A	† MicroPwr
										OP-16E	MicroPwr
										OP-16A	**† PMI (3566)**
											(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers–Characteristics (Cont'd)

Single Units (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Bandwidth MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source
0.5	0.050	0.01	5	19 *	18	100K	86	0	Wideband-JFET, Bias Comp.		(Cont'd)
										OP-16E	**PMI (3566)**
			5 *	0.8 *	40	60K	86	1	Wideband-JFET, Comp. for G>10	**HA-5110-2**	**† Harris (3442)**
				18 *	12 *	75K	86	0	Wideband-JFET	**HA-5100-2**	**† Harris (3440)**
										HA-5100-5	**Harris (3440)**
			10 *	0.8 *	40	60K	86	0	Wideband-JFET, Comp. for G>10	**HA-5110-5**	**Harris (3442)**
		0.025	10	1	1	50K	80	0	Low Power BIFET	LF441A	National
				3	10	50K	80	0	Wideband JFET	LF411A	National
		0.06	3	5 *	0.11	7	80K	90	Precision JFET Input	**HA-5170-5**	**Harris (3450)**
	0.1	—	50	15 *	150 *	100K	90	1	High Speed, High Power	1461-83	† TeledyneP
	0.10	0.02	5 *	2.5 *	5 *	50K	85	0	Bipolar—JFET	LF155	† AMD
										LF155	† Intersil
										LF155	† Motorola
										PM-155	† PMI
	0.2	0.1	10 *	3 *	13 *	50K	70	0	Low Offset JFET	TL087M	† TI
	0.4	0.05	10 *	3 *	13 *	25K	70	0	Low Offset JFET	TL087C	TI
		0.1	15	3 *	10	25K	—	0	Low Offset JFET	TL087	AnalogSys
	2	0.2	5	1 *	0.3 *	80K	96	1	Precision Bipolar, Low Bias	LM108A	† AMD
										LM208A	AMD
										AD108A	**† AD (3351)**
										AD208A	**AD (3351)**
										µA108AM	† Fairchild
										µA208AM	Fairchild
										LM108A	† Harris
										LM108A	† Intersil
										LM108A	† LinearTech
										LM108A	† Motorola
										LM208A	Motorola
										LM108A	† National
										LM208A	National
										PM-108A	**† PMI (3566)**
										PM-208A	PMI
										SG108A	† SiliconG
										SG208A	SiliconG
										SFC2108A	† Thomson-CSF
										SFC2208A	Thomson-CSF
	3	2.8	1	0.6	0.1	200K	114	0	Low Bias, Low Drift	OP-05	† Intersil
			2	0.4	0.1	200K	114	0	Instrumentation	OP-05	† LinearTech
				0.5 *	0.1	500K	114	0	Ultra Low Noise	**OP-05**	**† Raytheon (3592)**
				0.6	0.25 *	200K	110	0	Instrumentation	**MP5505B**	**† MicroPwr (3529)**
										OP-05	**† MicroPwr (3529)**
										OP-05	**† PMI (3566)**
	4	3.8	0.9	0.5 *	0.1	500K	110	0	Ultra Low Noise	**OP-05E**	**Raytheon (3592)**
			1.5	0.6	0.1	200K	123	0	Low Bias, Low Drift	OP-05E	Intersil
			2	0.4	0.1	200K	110	0	Instrumentation	OP-05E	LinearTech
				0.6	0.25 *	200K	107	0	Instrumentation	**MP5505E**	**MicroPwr (3529)**
										OP-05E	**MicroPwr (3529)**
										OP-05E	**PMI (3566)**
	7	1	5	1 *	0.3 *	80K	96	1	Precision Bipolar	LM308A	AMD
										AD308A	**AD (3351)**
										µA308AC	Fairchild
										LM308A	Harris
										LM308A	Intersil
										LM308A	LinearTech
										LM308A	Motorola
										LM308A	National
										PM-308A	PMI
										SG308A	SiliconG
										SFC2308A	Thomson-CSF
	7.5	2	2	—	0.7 *	750K	95	0	Programmable Micropower	**OP-32B**	**† PMI (3566)**
										OP-32F	**PMI (3566)**
	30	2	8	0.8	0.25	100K	85	0	General Purpose	**MP5502A**	**† MicroPwr (3529)**
										MP5502E	**MicroPwr (3529)**
										OP-02A	**† MicroPwr (3529)**
										OP-02E	**MicroPwr (3529)**
		5	5	1 *	0.25 *	80K	90	1	High Accuracy 301	**AD301AL**	**AD (3351)**

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

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Master Selection Guide

LINEAR–Operational Amplifiers–Characteristics (Cont'd)

Single Units (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift μV/°C	Band-width MHz	Slew Rate V/μs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source
0.5											(Cont'd)
	35	2	8	0.8	0.25	100K	90	0	General Purpose	**OP-02A**	† **PMI** (3566)
										OP-02E	**PMI** (3566)
	40	10	5	1.2 *	0.25 *	100K	100	0	Precision, Instrumentation	**CA3193**	**RCA** (3594)
										CA3493	**RCA** (3594)
	50	4	5	0.3 *	0.2	500K	84	0	Low Power	**OPA21G**	**Burr-Brown** (2850)
				0.5 *	49	1000K	85	1	Selectable Input	**OPA201A**	**Burr-Brown** (2850)
		5	5	1 *	0.5 *	50K	90	0	Higher Accuracy 741	**AD741L**	**AD** (3351)
		30	1	1.5 *	0.8	100K *	100 *	0	Low Drift	**3500E**	**Burr-Brown** (2850,2853)
	75	5	2	1	0.005 *	1000K	110	4	High Accuracy Instrumentation	μA725AM	† Fairchild
	80	5	2	—	0.01	1000K	120	4	High Gain Instrumentation	**OP-06B**	† **PMI** (3566)
										OP-06F	**PMI** (3566)
		10	0.5	0.3 *	0.12 *	1000K	110	1	Precision Low Noise	**AD504M**	**AD** (3351)
			1.0	0.3 *	0.12 *	1000K	110	1	Precision Low Noise	**AD504L**	**AD** (3351)
										AD504S	† **AD** (3351)
	500	200	15	0.3	—	—	72	0	Instrumentation	HC3020	HyComp
0.6	0.100	0.01	5	1 *	0.3 *	100K	110	0	Precision, Low Input Current	LM11C	Motorola
										LM11C	National
	7.5	2	2.0	0.25	0.08	500K *	80	0	Programmable Micropower	**OP-22B**	**PMI** (3566)
0.7	30	2	5	2.5 *	18 *	50K	90	0	High Speed	**MP5501A**	**MicroPwr** (3529)
										MP5501H	† **MicroPwr** (3529)
										OP-01A	† **MicroPwr** (3529)
										OP-01H	**MicroPwr** (3529)
										OP-01H	**PMI** (3566)
0.75	0.075	2.8	1.3	0.5 *	0.1	150K	110	0	Ultra Low Noise	**OP-07**	† **Raytheon** (3592)
		3.8	1.3	0.5 *	0.1	150K	106	0	Ultra Low Noise	**OP-07E**	**Raytheon** (3592)
	4	4	1.3	2.5 *	0.5	1M	100	0	Ultra Low Drift	**AM-430A**	**Datel** (2864)
										AM-430M	† **Datel** (2864)
	80	5	—	0.44 *	0.3	50K	80	0	High Performance	μA741EC	Fairchild
				1 *	0.3 *	50K	80	0	High Performance	μA741AM	† Fairchild
1	0.003	0.0005	15	1 *	0.6	50K	76	0	Low Bias FET	**OPA100A**	**Burr-Brown** (2850)
	0.01	0.01	10	—	125 *	100K	130 *	2	to ± 150V supply, 40mA output	PA84A	Apex
				3	20	1M	130 *	0	to ± 150V supply, 75mA output	PA83A	Apex
1.0	0.000075	—	25	0.35	0.3	50K	70	0	FET Electrometer	AD515L	AD
	0.00015	—	15	0.35	0.3	100K	80	0	FET Electrometer	AD515K	AD
	0.0003	0.00008	25	1 *	1.6 *	100K	66	0	Ultra Low Bias FET	OPA104AM	Burr-Brown
	0.0005	0.0002	50	1 *	0.6	100K	80 *	0	Ultra Low Bias FET	3523J	Burr-Brown
	0.001	0.0005	15	0.7 *	0.3	40K	70	0	Precision Low Drift FET	**AD545K**	**AD** (3351)
	0.002	0.001	25	0.7 *	0.3	20K	66	0	Precision Low Drift FET	**AD545J**	**AD** (3351)
	0.005	—	10	1 *	3	75K	80	0	High Accuracy, FET	AD506L	AD
				2 *	3	50K	72	0	Low Bias Current, FET	1425-02	TeledyneP
			25	2 *	3	50K	72	0	Low Bias Current, FET	1425-01	TeledyneP
		0.0002	10	1 *	1	75K	76	0	Precision FET	LH0052C	National
	0.010	—	25	2 *	3	50K	72		Low Drift, FET	1426-01	TeledyneP
		0.002 *	50	1 *	0.6	50K	90 *	0	Low Offset FET	**3522J**	**Burr-Brown** (2850)
		0.005 *	25	10 *	65	25K	70 *	0	Fast Settling, 1 μs to 0.01%	3550J	Burr-Brown
										3550S	† Burr-Brown
				20 *	100	25K	70 *	0	Fast Settling, 0.6 μs to 0.01%	3550K	Burr-Brown
	0.015	—	25	10 *	50	50K	80	0	Fast Wide Band, High Accuracy, FET Input	AD528K	AD
									Fast Wideband, High Accuracy, FET Input	AD528S	† AD
	0.025	—	5	2 *	3	50K	72	0	Low Drift, FET	1426-03	TeledyneP
			10	2 *	3	50K	72	0	Low Drift, FET	1426-02	TeledyneP
		0.002	10	2	16	50K	80	0	High Speed Precision Bipolar JFET	**AD544K**	† **AD** (3351)
				5 *	30 *	40K	80	1	High Speed, Low Drift FET	**AD382S**	† **AD** (3353)
						60K	80	—	High Speed, Low Drift FET	**AD381S**	† **AD** (3353)
			15	2	16	50K	80	0	High Speed Precision Bipolar JFET	**AD544S**	**AD** (3351)
		0.01	10	1.0 *	3	50K	76	0	Precision Bipolar JFET	**AD542S**	† **AD** (3351)
						200K	80	0	Precision Bipolar JFET	**AD542K**	**AD** (3351)
	0.035	0.002	25	1.5 *	94	10K	70	1	Wideband, Fast Settling	**OPA605A**	**Burr-Brown** (2851)
										OPA605H	**Burr-Brown** (2851)

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers–Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source
Single Units											**(Cont'd)**
1.0	0.035										(Cont'd)
		0.005	5	1	3	100K	76	2	Ultra Low Drift BIFET	**AD547J**	**AD** (3350,3351)
	0.05	0.005	15	5 *	30 *	40K	76	1	High Speed, Low Drift FET	**AD382J**	**AD** (3353)
						60K	76	—	High Speed, Low Drift FET	**AD381J**	**AD** (3353)
	0.050	0.01	5 *	18 *	8 *	150K *	86 *	0	Wideband, FET	**AM-410-2M**	† **Datel** (2864)
				60 *	50 *	150K *	94 *	0	Wideband, FET	**AM-411-2M**	† **Datel** (2864)
			15	70	1000	100K	44	1	150 ns Settling to 0.05%	3554B	Burr-Brown
						30K	60	1	Wideband, Fast Settling FET	**AD3554B**	**AD** (3353)
			25	70	1000	100K	44	1	150 ns Settling to 0.05%	3554S	Burr-Brown
						30K	60	1	Wideband, Fast Settling FET	**AD3554S**	† **AD** (3353)
	0.1	0.02	15	0.4	23	—	100	0	Instrumentation Amplifier, Programmable Gain 1 to 1000	**AM-551MC**	**Datel** (2861)
										AM-551MM	† **Datel** (2861)
	0.10	0.01	50	50 *	250 *	100K	70 *	1	Wideband, Fast Settling	**3551J**	**Burr-Brown** (2851)
										3551S	† **Burr-Brown** (2851)
		0.02	—	35	75K	86	—	0	Wideband-JFET, Bias Comp.	OP-17B	† MicroPwr
										OP-17F	MicroPwr
			10	—	35	75K	86	—	Wideband, Decompensated, Settles to 0.01% in 1.5 µs	**OP-17B**	† **PMI** (3566)
										OP-17F	**PMI** (3566)
				13 *	7.5	75K	86	0	Bipolar-JFET, Bias Comp.	OP-15B	† MicroPwr
										OP-15F	MicroPwr
										OP-15B	† **PMI** (3566)
										OP-15F	**PMI** (3566)
				18 *	12	75K	86	0	Wideband-JFET, Bias Comp.	OP-16B	† MicroPwr
										OP-16F	MicroPwr
										OP-16B	† **PMI** (3566)
										OP-16F	**PMI** (3566)
			20	40	330 *	25K	60	1	Wideband, Fast Settling	**AD380K**	**AD** (3353)
										AD380L	† **AD** (3353)
										AD380S	† **AD** (3353)
		0.05	5 *	18 *	12 *	60K	80	0	Wideband-JFET	HA-5105-5	Harris
		0.05 *	15 *	0.6 *	35 *	50K	80	1	Wideband-JFET, Comp. for G>10	HA-5115-5	Harris
	0.3	0.050	15	13 *	10	150K	86	0	Precision JFET	**OP-215E**	**PMI** (3566)
	0.30	0.02	15	40 *	220 *	25K	60	1	Wideband, Fast Settling	1437	TeledyneP
										1437-80	† TeledyneP
	2	100	10	30	300 *	100K	70	2	Low Offset, Fast Settling	**HOS-060**	† **AD** (3353)
										HOS-060/883	† **AD** (3353)
	5	0.5	10	0.8 *	0.12 *	40K	84	0	Precision, Low Input Current	**OP-12C**	† **PMI** (3566)
										OP-12G	**PMI** (3566)
								1	Precision, Low Input Current	**MPOP-08C**	† **MicroPwr** (3529)
										MPOP-08G	**MicroPwr** (3529)
										OP-08C	† **PMI** (3566)
										OP-08G	**PMI** (3566)
	10	3	3	—	0.7 *	500	85	0	Programmable Micropower	**OP-32G**	**PMI** (3566)
	15	7 *	3	1.5 *	1	45K	100 *	0	Low Bias, Low Noise	**3500C**	**Burr-Brown** (2850,2853)
			5	1.5 *	1	45K	100 *	0	Low Bias, Low Noise	**3500T**	† **Burr-Brown** (2850,2853)
	100	20	4 *	1 *	0.25 *	30K	70	2	High Voltage	LH0004	† National
			5	—	—	1000K	110	4	Instrumentation	µPC154	NEC
										PM-725	† PMI
				0.5 *	0.01 *	1000K	110	4	Instrumentation	RM725	† Raytheon
				1 *	0.005 *	1000K	110	4	High Accuracy Instrumentation	µA725M	† Fairchild
										LM725	† National
	200	50	6	1 *	0.4 *	25K	80	3	General Purpose	RM709A	† Raytheon
	250	70	20	—	—	20K	70	1	General Purpose	TA7502B	Toshiba
1.2	0	3	2.0	0.35	0.08	250K *	80	0	Programmable Micropower	**OP-22H**	**PMI** (3566)
1.3	7	6	2	0.5 *	0.1	400K	100	0	Ultra Low Noise	**OP-05C**	**Raytheon** (3592)
			2.0	0.6	0.17	120K	100	0	Low Bias, Low Drift	OP-05C	Intersil
			4.5	0.4	0.1	120K	100	0	Instrumentation	OP-05C	LinearTech
				1.2 *	0.25 *	120K	100	0	Instrumentation	**MP5505C**	**MicroPwr** (3529)
										OP-05C	**MicroPwr** (3529)
										OP-05C	**PMI** (3566)
											(Continued)

† Military Temperature Range (−55° to 125°C) * Typical Value

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LINEAR–Operational Amplifiers–Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift μV/°C	Band-width MHz	Slew Rate V/μs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	
Single Units												**(Cont'd)**
1.3	7	6	4.5	1.2 *	0.25 *	120K						(Cont'd)
							120	0	Instrumentation	μPC254	NEC	
	110	13	1.4 *	—	0.01	500K	110	4	High Gain Instrumentation	**OP-06G**	**PMI**	**(3566)**
1.5	0.010	—	25	1 *	3	50K	80	0	High Accuracy, FET	**AD506K**	**AD**	**(3351)**
			50	1 *	3	50K	80	0	High Accuracy, FET	**AD506S**	**† AD**	**(3351)**
	0.10	0.05	15 *	18 *	8 *	100K *	86 *	0	Wideband, FET	**AM-410-2C**	**Datel**	**(2864)**
				50 *	40 *	100K *	94 *	0	Wideband, FET	**AM-411-2C**	**Datel**	**(2864)**
	80	5	2	0.5 *	0.005 *	1000K	120	4	Instrumentation	LM725A	National	
	100	15	3	0.3 *	0.12 *	500K	100	1	Low Drift, Low Noise	**AD504K**	**AD**	**(3351)**
	120	45	4 *	1 *	0.25 *	30K	70	2	High Voltage	LH0004C	National	
2.0	0.001	0.0007	4 *	0.5 *	0.5 *	20K	55	0	Low Supply Voltage, BIMOS	**CA3420B**	**† RCA**	**(3594)**
	0.001 *	0.001 *	0.7 *	0.1 *	0.04 *	30K	70	1	Programmable, Low Bias	**TLC251BC**	**TI**	**(3689)**
										TLC271BC	**TI**	
												(541,3687,3689)
			1 *	0.012 *	0.001 *	20K *	77	1	Prog., Low Bias, Supply Volt. = 1 V	TLC251BC	TI	
				0.075 *	0.01 *	10K *	77	1	Prog., Low Bias, Supply Volt. = 1 V	TLC251BC	TI	
			5 *	2.3 *	4.5 *	10K	70	1	Programmable, High Bias	TLC251BC	TI	
										TLC271BC	TI	
	0.010	—	50	2 *	3	50K	72	—	Low Bias Current, FET	1425	TeledyneP	
		0.0005 *	15	1 *	3	50K	70	0	Low Offset Voltage, FET	ICL8007	† Intersil	
	0.02	—	50	100	1000	100K	90	1	Fast-Settling, FET Input	1443-83	† TeledyneP	
	0.025	—	50	2	3	50K	72	0	Low Drift, FET	1426	TeledyneP	
	0.025 *	0.010 *	20	1.0 *	3	50K	76	0	Precision Bipolar JFET	**AD542J**	**AD**	**(3351)**
	0.030	0.01	4 *	0.063 *	0.03 *	32K	75	0	Manopower, BIMOS	**CA3440B**	**RCA**	**(3594)**
	0.05	0.01	5	2.5	3	50K	85	1	JFET Input	TDC0155A	† Thomson-CSF	
				4	10	50K	85	1	JFET Input	TDC0156A	† Thomson-CSF	
				15	40	50K	85	1	JFET Input	TDC0157A	† Thomson-CSF	
			50	70	1000	100	60	1	Wideband, Fast Settling FET	**AD3554A**	**AD**	**(3353)**
		0.05	30	—	30 *	800K	96	0	to ± 150V supply, 150mA output	PA08	Apex	
				1.3 *	5	100K	120 *	0	to ±50V supply, 5A output	PA07	Apex	
	0.050	0.005	20	2	15	30K	74	0	High Speed Precision Bipolar JFET	**AD544J**	**AD**	**(3351)**
		0.01	5	—	40	50K	85	—	Wideband Decompensated	LF157A	† Intersil	
										LF357A	Intersil	
										LF157A	† Motorola	
										LF357A	Motorola	
										LF157A	† National	
										LF357A	National	
										PM-157A	**† PMI**	**(3566)**
										PM-357A	PMI	
				2.5 *	3	50K	85	0	Bipolar - JFET	LF155A	† AMD	
										LF355A	AMD	
										LF155A	† Intersil	
										LF355A	Intersil	
										LF155A	† Motorola	
										LF355A	Motorola	
										LF155A	† National	
										LF355A	National	
										PM-155A	† PMI	
										PM355A	PMI	
				4	10	50K	85	0	Wideband - JFET	LF156A	† AMD	
										LF356A	AMD	
										LF156A	† Intersil	
										LF356A	Intersil	
										LF156A	† Motorola	
										LF356A	Motorola	
										LF156A	† National	
										LF356A	National	
										PM-156A	**† PMI**	**(3566)**
										PM-356A	PMI	
			50	70	1000	100K	44	1	150 ns Settling to 0.05%	3554A	Burr-Brown	
		0.03	10 *	1	1.6	80K *	70	0	Low Power	**ICL7611AC**	**Intersil**	**(3481)**
										ICL7611AM	**† Intersil**	**(3481)**
									Low Power, Extended CMVR	**ICL7612AC**	**Intersil**	**(3481)**
										ICL7612AM	**† Intersil**	**(3481)**
												(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR-Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift μV/°C	Band-width MHz	Slew Rate V/μs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source
Single Units											**(Cont'd)**
2.0	0.050	0.03	10 *	1	1.6	80K *	70	0			(Cont'd)
									Low Power, Input Protected	**ICL7613AC**	**Intersil (3481)**
								1	Low Power	**ICL7614AC**	**Intersil (3481)**
										ICL7614AM	**† Intersil (3481)**
									Low Power, Input Protected	**ICL7615**	**† Intersil (3481)**
										ICL7615AC	**Intersil (3481)**
	0.075	0.025	10 *	4 *	13 *	50K	80	0	Precision BIFET	MC35001A	† Motorola
	0.10	0.05	10 *	4 *	13 *	50K	80	0	Precision BIFET	MC34001A	Motorola
									Wideband Bipolar JFET	LF351A	National
			20	150	400	10K	60	3	Fast Settling, Wideband	**OPA600M**	**Burr-Brown (2853)**
										OPA600V/883B	**† Burr-Brown (2853)**
										OPA600V/MIL	**† Burr-Brown (2853)**
		0.05 *	40	0.5 *	3	50K	80	1	High Current, High Power	3571A	Burr-Brown
										3572A	Burr-Brown
		0.050	10 *	3 *	13 *	50K	80	0	Bipolar JFET	μA771A	Fairchild
										μA771AM	† Fairchild
	0.15	0.05	20	0.06	10	3K	100	—	JFET Input	MA403	AnalogSys
	0.2	0.02	50	40 *	225	30K	60	1	Wideband, Fast Settling	1438	TeledyneP
										1438-83	† TeledyneP
		0.1	20	3	10	50K	80	0	JFET Input, High Speed	TDB0351A	Thomson-CSF
	0.20	0.10	20	2.7	8	25K	70	0	Wideband JFET	LF411	National
			20 *	3	10	50K	80	0	Wideband Bipolar JFET	LF151A	† National
	0.30	0.02	15	40	220	25K	60	0	Wideband, settles to 0.1% in 110 ns	HC1437	HyComp
										HC1437-883	† HyComp
	0.50	—	75	60 *	500	200K	—	0	Inverting, Settles to 0.01% in 200 ns	1430	TeledyneP
										1430-83	† TeledyneP
	2	0.2	15	0.3 *	0.3 *	50K	85	1	Low Noise 108	ICL108LN	† Intersil
				1 *	0.2 *	50K	85	0	Micropower, Supply Current 600 μa	LM112	Motorola
										LM212	Motorola
										LM112	† National
										LM212	National
					0.3 *	50K	85	1	Precision Bipolar	LM108	† AMD
										LM208	AMD
										AD108	† AD
										AD208	**AD (3351)**
										μA108M	† Fairchild
										μA208M	Fairchild
										LM108	† Harris
										LM108	† Intersil
										LM108	† LinearTech
										LM108	† Motorola
										LM208	Motorola
										LM108	† National
										LM208	National
										PM-108	† PMI
										PM-208	PMI
										SG108	† SiliconG
										SG208	SiliconG
										SFC2108	† Thomson-CSF
										SFC2108M	† Thomson-CSF
										SFC2208	Thomson-CSF
	3	2	10	0.5 *	0.1	45K	100 *	0	Low Bias Current	**3501C**	**Burr-Brown (2850)**
	7	3	10	0.5 *	0.1	45K	100 *	0	Low Bias Current	**3501B**	**Burr-Brown (2850)**
										3501S	**† Burr-Brown (2850)**
	20	0.7	2.0 *	—	—	60K	89	0	Op Amp and Voltage Reference	LM10BL	National
						120K	93	0	Op Amp and Voltage Reference	MCELM10	MCE
										LM10	† National
										LM10B	National
		10 *	5	1.5 *	1	45K	100 *	0	Low Bias, Low Noise	**3500B**	**Burr-Brown (2850,2853)**
			10	1.5 *	1	45K	100 *	0	Low Bias, Low Noise	**3500S**	**† Burr-Brown (2850,2853)**
	25	3	15	0.5	0.5 *	50K	80	1	Low Offset Current	μA777M	† TI
	50	5	8	2.5 *	18 *	50K	80	0	High Speed	**MP5501E**	**MicroPwr (3529)**
											(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers–Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift μV/°C	Band-width MHz	Slew Rate V/μs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source
Single Units											**(Cont'd)**
2.0	50	5	8	2.5 *	18 *	50K	80	0	High Speed		(Cont'd)
										MP5501F	**† MicroPwr (3529)**
										OP-01E	**MicroPwr (3529)**
										OP-01F	**† MicroPwr (3529)**
										OP-01E	**PMI (3566)**
										OP-01F	**† PMI (3566)**
			10	0.8	0.25	50K	90	0	General Purpose	MP5502	† MicroPwr
										OP-02	**† MicroPwr (3529)**
										OP-02C	**MicroPwr (3529)**
										OP-02	PMI
										OP-02C	**PMI (3566)**
		10	15	4 *	1.5	25K	80	0	High Performance, High Gain	RM4131	† Raytheon
	60	10	15	—	40	50K	70	1	60 V/μs Comp. for g=5	SE538	† Signetics
				3 *	25	50K	70	0	High Slew Rate	SE530	† Signetics
	75	10	15	0.8 *	0.5 *	50K	80	1	Low Noise 101A	ICL101ALN	† Intersil
				1 *	0.5 *	25K	80	1	General Purpose, Uncompensated	SFC2101A	† Thomson-CSF
						50K	80	0	General Purpose, Compensated	LM107	† Intersil
										LM107	† LinearTech
										LM107	† Motorola
										LM207	Motorola
										LM107	† National
										LM207	National
										LM107	† Raytheon
										SG107	† SiliconG
										SG207	SiliconG
										LM107	† TI
										LM207	TI
										SFC2107	† Thomson-CSF
										SFC2207	Thomson-CSF
									Higher Accuracy 741	**AD741S**	**† AD (3351)**
								1	General Purpose, Improved 101, Uncompensated	AD101A	† AD
										AD201A	**AD (3351)**
										μA101AM	† Fairchild
										μA201AM	Fairchild
										LM101A	† Motorola
										LM201A	Motorola
										LM101A	† National
										LM201A	National
										LM101A	† Raytheon
										SG101A	† SiliconG
										SG201A	SiliconG
										LM101A	† TI
										LM201A	TI
										SFC2201A	Thomson-CSF
										LM101A	† LinearTech
							90	0	Higher Accuracy 741C	**AD741K**	**AD (3351)**
	200	50	10	5 *	0.3 *	25K	80	3	General Purpose	μA709AM	† Fairchild
										MC1709A	† Motorola
										LM709A	† National
										SFC2709A	† Thomson-CSF
			25	—	0.3 *	45K *	80	3	General Purpose	μA709AM	† TI
	800	200	—	10 *	13 *	50K	80	1	Wideband, Low Noise	**XR5534M**	**† Exar (3379)**
										RM5534	† Raytheon
										SE5534	**† Signetics (526)**
										SE5534A	**† Signetics (526,3646)**
										SE5534	† TI
	4000	1500	1.2 *	15 *	3 *	0.7K	70	1	6 Volt, Wideband	CA3010A	† RCA
										CA3029A	RCA
										CA3037A	† RCA
	6000	1600	1.2 *	50 *	7 *	2K	80	1	12 Volt, Wideband	CA3015A	† RCA
										CA3030A	RCA
										CA3038A	† RCA
2.5	125	35	2 *	1 *	0.005 *	250K	94	4	High Accuracy Instrumentation	μA725C	Fairchild
										LM725C	National
										μPC725	NEC

(Continued)

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LINEAR–Operational Amplifiers–Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Bandwidth MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source
Single Units											**(Cont'd)**
2.5	125	35	2 *	1 *	0.005 *	250K	94	4	High Accuracy Instrumentation		(Cont'd)
										PM-725C	PMI
										RC725	Raytheon
	200	40	5	0.3 *	0.12 *	250K	94	1	Low Drift, Low Noise	**AD504J**	**AD (3351)**
		75	2 *	8 *	1	100K	86	0	High Performance	**HS3546RH**	**† Harris (4714)**
	250	50	10 *	1 *	0.25 *	100K	90	2	High Gain Instrumentation, 50 mA	LH0020	† National
3	0.001	0.0002	5	2	7	1M	90			1346	TeledyneP
										1346-01	† TeledyneP
	0.05	0.01	10	100	120	150	74			1344-01	† TeledyneP
			20	100	120	150	74			1344	TeledyneP
3.0	0.0003	—	50	0.35	0.3	40K	66	0	FET Electrometer	AD515J	AD
	0.001	0.0002	5 *	0.11	4	1M	90	1	Low Bias Current, Low Power	**HA-5180-2**	**Harris (3452)**
										HA-5180-5	**Harris (3452)**
	0.020	0.020 *	25	3 *	20 *	100K	110 *	0	High Voltage FET	3582J	Burr-Brown
				5	20 *	50K	110 *	0	High Voltage FET	3581J	Burr-Brown
				5 *	20 *	400K	110 *	0	High Voltage FET	3583	Burr-Brown
				7 *	—	1000K	110 *	2	High Voltage FET	3584	Burr-Brown
	0.030	—	50	10 *	50	25K	70	0	Fast Wideband, High Accuracy FET	AD528J	AD
		0.01	10 *	5 *	13	200K	86 *	0	FET Input, Bipolar/MOS Output	**CA081B**	**RCA (3596)**
								1	FET Input, Bipolar/MOS Output	**CA080B**	**RCA (3596)**
	0.040	0.02	10 *	5 *	13 *	50K	80	0	FET Input, Bipolar/MOS Output	**CA081AT**	**† RCA (3596)**
								1	FET Input, Bipolar/MOS Output	**CA080AT**	**† RCA (3596)**
	0.05	—	75	90	900	56K	80	1	Fast-Settling, FET Input	1443	TeledyneP
		0.01	10 *	100 *	100	75K	74	1	Wideband, High Slew Rate	**HA-5160-2**	**† Harris (3448)**
			20 *	100 *	100	75K	74	1	Wideband, High Slew Rate	**HA-5160-5**	**Harris (3448)**
		0.05	25	—	125 *	100K	130 *	2	to ± 150V supply, 40mA output	PA84	Apex
				5	20	1M	130 *	0	to ± 150V supply, 75mA output	PA83	Apex
										PA83M	† Apex
	0.050	0.015	—	1 *	0.3 *	40K	80	0	High Performance, Low Input Current	LM316A	National
	0.1	0.05	30	—	100 *	—	104 *	2	to ±50V supply, 4A output	PA09	Apex
	0.15	0.03	10	0.11	10	3K	90	—	Low Wideband Noise	MA344	AnalogSys
	0.2	0.05	15	—	25	50K	82	—	Wideband, Decompensated, Settles to 0.01% in 1.6 µs	**OP-17C**	**† PMI (3566)**
										OP-17G	**PMI (3566)**
				12 *	5	50K	82	0	Bipolar-JFET, Bias Comp.	OP-15C	† MicroPwr
										OP-15G	MicroPwr
										OP-15C	**† PMI (3566)**
										OP-15G	**PMI (3566)**
				17 *	9	50K	82	0	Wideband-JFET, bias comp.	OP-16C	† MicroPwr
										OP-16G	MicroPwr
										OP-16C	**† PMI (3566)**
										OP-16G	**PMI (3566)**
				20	25	50K	82	—	Wideband, Decompensated, Settles to 0.01% in 1.6 µs	OP-17C	† MicroPwr
										OP-17G	MicroPwr
		0.1	—	3	13 *	50K	70	0	Bipolar JFET	TL081B	Motorola
										TL081BC	TI
			10 *	1 *	3.5 *	4K	80	0	Low Power, Bipolar-JFET	TL061BC	TI
									Programmable Bipolar JFET	TL066BC	TI
					4 *	20K	80	0	Low Power, JFET Input	**HA-5062B-5**	**Harris (3432)**
				3 *	13 *	50K	80	0	Bipolar-JFET	TL088C	TI
										TL088M	† TI
				4	15 *	50K	80	1	JFET Input	**HA-5082B-5**	**Harris (3436)**
	0.20	0.05	10 *	4 *	13 *	50K	80	0	Low Noise Bipolar-JFET	TL071BC	Motorola
										TL071BC	TI
	0.30	75	10 *	0.3	10	200K *	85	0	2.0 A Power	LH0101A	† National
										LH0101AC	National
	0.4	0.1	15	3 *	10	25K	—	0	Low Offset JFET	TL088	AnalogSys
	4	0.5	5	100	1000	1000K	0		Settles to 0.01% in 200 ns	AM-500GC	Datel
										AM-500MC	Datel
			7	100	1000	1000K	0	—	Fast Setting	**AM-500MR**	**Datel (2861,2865)**
			10	100	1000	1000K	0	—	Fast Setting	**AM-500MM**	**† Datel (2861,2865)**
											(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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Master Selection Guide

LINEAR–Operational Amplifiers–Characteristics (Cont'd)

Single Units (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift μV/°C	Band-width MHz	Slew Rate V/μs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source
3.0											(Cont'd)
	5	3	10 *	—	0.1 *	40K	80	0	Programmable Amplifier	HA-2720	† Harris
	7.5	3	—	0.25 *	0.16 *	100K	70	0	Programmable	ICL4250	† Intersil
										LM4250	† National
										SG4250	† SiliconG
										UC4250	† Solitron
	10	2	15	0.3 *	0.13 *	50K	80	0	Micropower	RM4132	† Raytheon
				12 *	4	100K	80	0	High Impedance	**HA-2600**	**† Harris (3406)**
										HA2600	† Intersil
		1000	50	1	500	300	80	2	High Slew Rate	MA207	AnalogSys
	15	4	15	0.05	0.015	—	70	0	High Output, Low Power	MA112	AnalogSys
		15	15	35 *	25	100K	80	1	Wideband, General Purpose	**AD507K**	**AD (3353)**
	20	5	—	0.85 *	0.55	80K	80	0	Low Power, Radiation Resistant	**HS3530RH**	**† Harris (4709)**
		10	40	4 *	2.5	70K	74	0	to ±50V supply, 15A output	PA12A	† Apex
				6 *	2.5	70K	74	0	to ±50V supply, 5A output	PA10A	† Apex
	25	5	10 *	—	—	4K	60	3	Matched Transistors	LH0005A	† National
	80	30	—	1 *	0.6	50K	80	0	to 500 mA, single supply	μA759	† Fairchild
			15	0.4	0.3	50K	80	0	Higher Performance	LM741A	† National
										LM741E	National
	100	100	—	10	22	10K	80	1	High Slew Rate, Wideband	**HS3516RH**	**† Harris (4705)**
	200	50	20	1 *	0.5 *	50K	80	0	High Current	AD512K	AD
									Higher Accuracy 741C	**AD741J**	**AD (3351)**
			25	1 *	0.5 *	50K	80	0	High Current	AD512S	† AD
	300	100	3 *	1 *	1.5 *	100K	70	1	0.2 A Power	LH0041	† National
			10	1 *	0.4 *	25K	70	3	High Gain	RM709	† Raytheon
			25	1 *	1.5	100K	70	1	1.0 A Power	LH0021	† National
	500	75	3 *	2 *	4.2 *	50K	80	2	General Purpose	MC1539	† Motorola
	1000	200	10	40	20	100K	70	0	Low Noise, Wideband	MA322	AnalogSys
		500	10	300	50	100K	90	2	Fast, Wideband	MA326	AnalogSys
	2000	200	4	10 *	—	20K	70	0	General Purpose Wide Bandwidth	LH0003	† National
										LH0003C	National
3.5	0.015	—	75	1*	3	20K	70	0	High Accuracy, FET	**AD506J**	**AD (3351)**
	12	2.5	6 *	—	0.04	150K	115 *	2	Micropower	**RC3078A**	**† Raytheon (3592)**
4.0	0.010	0.002	10	1 *	1.5	100K	80	0	Micropower	LH0022	† National
	3	—	12	20 *	30 *	—	70	0	Unity Gain, Noninverting	SFC2110M	Thomson-CSF
	15	2	10 *	1 *	2.5 *	100K	80	0	High Performance	MC1556	Motorola
		15	10 *	35 *	25	100K	80	1	Wide Band, High Impedance	HA2620	† Intersil
										HA-2620	† Harris
			20	35 *	20	100K	80	1	Wideband, General Purpose	**AD507S**	**† AD (3353)**
	25	12	15 *	4 *	5 *	100K	80	0	High Voltage	HA-2640	† Harris
	30	2.0	5.0	—	—	40K	80	0	Op Amp and Voltage Reference	LM10CL	National
						80K	90	0	Op Amp and Voltage Reference	LM10C	National
	200	50	15	12 *	10	50K	80	0	High Speed, Fast Setting	**AD518K**	**AD (3353)**
			20	12 *	10	50K	80	0	High Speed, Fast Settling	**AD518S**	**† AD (3353)**
	250	50	—	15 *	50	50K	80	0	Precision High Speed	LM118	† AMD
										LM218	AMD
										LM118	† Harris
										LM118	† LinearTech
										LM118	† National
										LM218	National
										LM118	† TI
										LM218	TI
										SFC2118	† Thomson-CSF
										SFC2218	Thomson-CSF
	300	100	5 *	1 *	25	50K	70	1	0.5 A Wideband	LH0061	† National
	350	100	3	—	0.5 *	50K	80	0	Short Circuit Protected	TBA222	† Siemens
					5.5 *	50K	90	1	Adjustable Input Offset Voltage	TBC0748	† Siemens
	700	100	10	—	—	25K	70	1	40mA Output	MA342	AnalogSys
			25	—	—	18K	70	1	20 mA Output	TAA762	† Siemens
										TAA862	† Siemens
					9 *	18K	70	1	General Purpose, OC Output	SFC2761M	† Thomson-CSF
										SFC2861M	† Thomson-CSF
	1500	300	—	10 *	6 *	25K	70	1	Low noise, Comp. for G=3	**XR5534**	**Exar (3379)**

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† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers–Characteristics (Cont'd)

Single Units (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source
4.0	1500	300	—	10 *	6 *	25K	70	1	Low noise, Comp. for G=3		(Cont'd)
										XR5534A	**Exar** (3379)
										XR5534C	**Exar** (3379)
										RC5534	**Raytheon** (3592)
										NE5534	Signetics
										NE5534A	**Signetics** (3646)
										NE5534	TI
										NE5534A	TI
					13 *	100K *	80	1	Low Noise, Comp. for G=3	**AM-453-2C**	**Datel** (2864)
										AM-453-2M	† **Datel** (2864)
	30000	5000	20 *	70 *	400	4K	60 *	3	High Slew Rate	LH0024	† National
4.5	170	32	6 *	—	0.04	—	110	2	Micropower	**RC3078**	**Raytheon** (3592)
					0.04 *	25K	80	1	Micropower	CA3078	† RCA
5	15000	4000	20	150	200	30K	74			1343-01	† TeledyneP
	20000	6000	20	9.5	600	30K	60			1342-01	† TeledyneP
				400	400	30K	60			1341-01	† TeledyneP
5.0	0.001	0.0005	5	0.7 *	0.3	40K	76	0	Precision, Low Drift FET	**AD545L**	**AD** (3351)
		0.0005 *	25	1 *	0.6	50K	90 *	0	Low Offset FET	3522L	Burr-Brown
	0.001 *	0.001 *	0.7 *	0.1 *	0.04 *	30K	70	1	Programmable, Low Bias	**TLC251AC**	**TI** (3689)
										TLC271AC	**TI** (541,3687,3689)
			1 *	0.012 *	0.001 *	20K *	77	1	Prog., Low Bias, Supply Volt. = 1 V	TLC251AC	TI
				0.075 *	0.01 *	10K *	77	1	Prog., Low Bias, Supply Volt. = 1 V	TLC251AC	TI
			5 *	2.3 *	4.5 *	10K	70	1	Programmable, High Bias	TLC251AC	TI
										TLC271AC	TI
	0.003	0.002	4 *	0.5 *	0.5 *	20K	70	0	Low Supply Voltage	**CA3420A**	† **RCA** (3594)
	0.005	0.0006		2 *	50 *	—	80	0	Micropower, Transconductance Amplifier	CA3080	RCA
										CA3080A	† RCA
	0.010	0.0005 *	0.05	2 *	1 *	200K	90	0	Chopper Stabilized, Low Power	TML7650-1	Telmos
					2.5 *	1M *	120	0	Chopper Stabilized	TML7650	Telmos
	0.025	0.002	25	15 *	50	50K	80	0	Precision, High Speed FET	LH0062	† National
	0.030	0.02	6 *	4 *	10 *	50K	80	0	MOS-Bipolar	**CA3160A**	† **RCA** (3596)
			10 *	4 *	10 *	50K	80	1	MOS, Single Supply, Strobe	CA3130A	† RCA
	0.040	0.02	4 *	0.063 *	0.03 *	10K	70	0	Nanopower BIMOS	**CA3440A**	**RCA** (3594)
			6 *	4.5 *	9 *	20K	70	0	MOS FET, Single Supply	**CA3140A**	**RCA** (3595)
	0.050	0.030	15 *	1	1.6	80K *	70	0	Low Power	**ICL7611BC**	**Intersil** (3481)
										ICL7611BM	† **Intersil** (3481)
									Low Power, Extended CMVR	**ICL7612BC**	**Intersil** (3481)
										ICL7612BM	† **Intersil** (3481)
									Low Power, Input Protected	**ICL7613BC**	**Intersil** (3481)
										ICL7613BM	† **Intersil** (3481)
								1	Low Power	**ICL7614BC**	**Intersil** (3481)
										ICL7614BM	† **Intersil** (3481)
									Low Power, Input Protected	**ICL7615BC**	**Intersil** (3481)
										ICL7615BM	† **Intersil** (3481)
	0.1	0.02	5 *	2	30	25K	80	1	JFET Input	TDC0157	† Thomson-CSF
				2.5	5 *	25K	80	1	JFET Input	TDC0155	† Thomson-CSF
				5	7.5	25K	80	1	JFET Input	TDC0156	† Thomson-CSF
	0.10	0.02	5 *	—	—	50K	85	—	Wideband Decompensated	LF157	† Intersil
										LF357B	Motorola
										LF157	† National
										LF257	National
										LF357B	National
										PM-157	† **PMI** (3566)
										PM-257	PMI
				2.5 *	5 *	50K	85	0	Bipolar-JFET	LF255	AMD
										LF355B	Motorola
										LF155	† National
										LF255	National
										LF355B	National
										PM-255	PMI
				5 *	7,5 *	50K	85	0	Wideband-JFET	LF156	† AMD

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† Military Temperature Range (−55° to 125°C) * Typical Value

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LINEAR–Operational Amplifiers–Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift μV/°C	Band-width MHz	Slew Rate V/μs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source
Single Units											**(Cont'd)**
5.0	0.10	0.02	5 *	5 *	7,5 *	50K	85	0	Wideband-JFET		(Cont'd)
										LF256	AMD
										LF156	† Intersil
										LF356B	Motorola
										LF156	† National
										LF256	National
										LF356B	National
										PM-156	**† PMI (3566)**
										PM-256	PMI
		0.025	10	1	1	25K	70	0	Low Power-BIFET	LF441	National
			25 *	70 *	350	1K	50	2	Ultra Fast FET	TP0032	† TeledyneP
									Ultra Fast-FET	LH0032	† National
										ADLH0032	† AD
		0.05	10 *	3 *	13 *	50K	80	0	Bipolar JFET	μ	Fairchild
									Bipolar-JFET	μA771B	Fairchild
										μA771BM	† Fairchild
				4 *	13 *	50K	80	0	Precision-BIFET	MC35001B	† Motorola
			80	150	400	10K	60	3	Fast Settling, Wideband	**OPA600U**	**Burr-Brown (2853)**
			100	150	400	10K	60	3	Fast Settling, Wideband	**OPA600U/883B**	**† Burr-Brown (2853)**
	0.15	—	50	20 *	210	10K	70	1	Wideband, Fast Settling	AH0605	OEI
	0.2	0.1	30	4 *	13 *	50K	80	0	JFET Input, High Speed	TDB0351B	Thomson-CSF
	0.20	0.025	3 *	1 *	0.3 *	25K	96	0	Precision Bipolar	LM11CL	National
		0.10	10 *	4 *	13 *	50K	80	0	Precision-BIFET	MC34001B	Motorola
									Wideband Bipolar-JFET	LF351B	National
					15 *	50K	100 *	0	Wideband Bipolar-JFET	LF151	† National
	4	1	10	1 *	0.5 *	20K	80	0	Low Input Current 741	AD502L	AD
	7	4	20	1 *	0.5 *	20K	80	0	Low Input Current 741	AD502K	AD
	7.5	3	—	1 *	0.1	20K	70	0	Multi-Purpose, Programmable	SFC2776M	† Thomson-CSF
	10	5	7 *	1 *	0.5 *	20K	70	0	Low Input Current	ICL8008M	† Intersil
			10 *	—	0.1 *	25K	74	0	Programmable Amplifier	HA-2725	Harris
			20 *	1 *	0.5 *	20K	80	0	Darlington 741	AD502S	† AD
		6	—	0.25 *	0.16 *	50K	70	0	Programmable	LM4250C	Harris
										ICL4250C	† Intersil
										LM4250C	† National
										SG4250C	† SiliconG
										UC4250C	Solitron
	15	5	20	0.5 *	0.1	45K	100 *	0	Low Bias Current	**3501A**	**Burr-Brown (2850)**
										3501R	**† Burr-Brown (2850)**
	20	3	—	—	2.5 *	100K	80	1	High Voltage	LM144	† National
				1 *	2 *	100K	80	0	High Voltage	MC1536	† Motorola
										LM1536	† National
										SG1536	† SiliconG
			40	1 *	1.5	60K	80	0	Output 26V @ 10A	**OPA501B**	**Burr-Brown (2850)**
										OPA501S	**† Burr-Brown (2850)**
	25	5	20	0.3 *	0.13 *	50K	70	0	Micropower	RC4132	Raytheon
		25	5 *	12 *	4	300K	100	0	Wide Temperature Range	**OPA11HT**	**† Burr-Brown (2850)**
			10 *	12 *	4	80K	74	0	High Impedance	**AM-460-2**	**Datel (2864)**
										AM-460-2M	**† Datel (2864)**
										HA-2602	† Harris
										HA-2605	Harris
										HA2602	† Intersil
										HA2605	Intersil
			15 *	35 *	20	80K	74	1	Wide Band, High Impedance	**AM-462-1**	**Datel (2864)**
										AM-462-1M	**† Datel (2864)**
										AM-462-2	**Datel (2864)**
										AM-462-2M	**† Datel (2864)**
										HA2622	† Intersil
										HA2625	Intersil
										HA-2622	† Harris
										HA-2625	Harris
			30 *	1	—	80K	74	1	Wideband	**3508J**	**Burr-Brown (2851)**
				70	20	80K	100 *	1	Wideband, High Gain	1321	TeledyneP
										1321-01	† TeledyneP

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† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers–Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift μV/°C	Band-width MHz	Slew Rate V/μs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source
Single Units											**(Cont'd)**
5.0											(Cont'd)
	30	15 *	20	1.5 *	0.6	45K	100 *	0	Low Bias, Low Noise	**3500A**	**Burr-Brown (2850,2853)**
										3500R	**† Burr-Brown (2850,2853)**
		30	20	2	0.4	50K	80	0	General Purpose	**3500R/MIL**	**† Burr-Brown (2850,2853)**
			60	2	0.4	50K	80	0	General Purpose	**3500U/883B**	**† Burr-Brown (2850,2853)**
	35	7	—	5 *	5 *	10K	67	0	High Power, Comp. G>30	CA3105	RCA
										CA3105M	RCA
	40	2.5 *	30 *	1 *	10	200K	80	0	Micropower FET High Current Out	1323	TeledyneP
		15	5	—	20	300K	106	0	High Speed	**AM-470-2C**	**Datel (2865)**
										AM-470-2M	**† Datel (2865)**
	50	15	—	0.2	0.35	50K	70	0	Programmable Low Power	MC1776	† Motorola
	100	20	10	2.5 *	18 *	25K	80	0	High Speed	**MP5501C**	**MicroPwr (3529)**
										MP5501G	**† MicroPwr (3529)**
										OP-01C	**MicroPwr (3529)**
										OP-01G	**† MicroPwr (3529)**
										OP-01C	**PMI (3566)**
										OP-01G	**† PMI (3566)**
			30	1 *	0.5 *	25K	70	1	Precision	μA777C	Intersil
		25	20	1.3	0.25	25K	70	0	General Purpose	**MP5502B**	**† MicroPwr (3529)**
										MP5502D	**MicroPwr (3529)**
										OP-02B	**† MicroPwr (3529)**
										OP-02D	**MicroPwr (3529)**
										OP-02B	**† PMI (3566)**
										OP-02D	**PMI (3566)**
		100	—	1 *	0.4 *	50K	70	0	Programmable	XR146	† Exar
	120	40	6 *	3 *	20	50K	70	0	High Slew Rate	NE530	Signetics
	150	20	20	4 *	2 *	25K	70	0	High Performance, High Gain	RC4131	Raytheon
		30	—	—	—	50K	70	0	Single Supply	TL321I	TI
										TL321M	† TI
		40	6 *	—	60 *	50K	70	1	60 V/μs, Comp. for G=5	NE538	Signetics
	200	—	10 *	10 *	130	25K	—	2	High Speed Inverting	ICL8017M	† Intersil
		25	20 *	12 *	25	20K	80	0	High Slew Rate	**HA-2500**	**† Harris (3396)**
										HA2500	† Intersil
		50	20 *	8 *	15 *	50K	80	1	Four Addressable Inputs, Single Amplifier	HA-2400	† Harris
										HA-2404	Harris
	250	20	20	1 *	0.5 *	25K	96	0	General Purpose	LM307	Raytheon
								1	General Purpose	LM301A	Raytheon
	500	150	20	—	—	20K	70	1	General Purpose	TA7502	Toshiba
										TA7502A	Toshiba
		200	—	0.5 *	35	50K	70	1	High Slew Rate	RM4531	† Raytheon
				1 *	0.5	50K	70	0	High Performance	SFC2741M	† Thomson-CSF
								1	General Purpose	SFC2748M	† Thomson-CSF
					0.7	50K	70	0	High Speed 741	ICL741MHS	† Intersil
					30 *	50K	70	1	High Slew Rate	SE531	† Signetics
			3 *	0.5 *	0.3 *	25K	70	3	General Purpose	μA709M	† Fairchild
										MC1709	† Motorola
										LM709	† National
				0.8 *	5 *	50K	70	0	Wideband 741	SG1217	† SiliconG
				1 *	0.5 *	50K	70	0	General Purpose Compensated	AD741	† AD
										μA741M	† Fairchild
										ICL741	† Intersil
										MC1741	† Motorola
										LM741	† National
										PM-741	PMI
										RM741	† Raytheon
										μA741	† Signetics
										SG741	† SiliconG
										μA741M	† TI
									Low Noise 741	ICL741LN	† Intersil

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers–Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source
Single Units											**(Cont'd)**
5.0	500	200	3 *	1 *	0.5 *	50K	70	0	Low Noise 741		(Cont'd)
										MC1741N	† Motorola
										CA6741	† RCA
								1	General Purpose, Uncompensated	µA101	† Fairchild
										LM101	† National
										LM101	† Signetics
										SG101	† SiliconG
									Uncompensated 741	µA748M	† Fairchild
										MC1748	† Motorola
										LM748	† National
										LM748C	National
										CA748	† RCA
										SG748	† SiliconG
										µA748M	† TI
					10	50K	70	0	High Slew Rate 741	MC1741S	† Motorola
										SG741S	† SiliconG
									Low Noise 741	MC1741NS	Motorola
				5 *	0.3 *	12K	80	3	General Purpose	SFC2709M	† Thomson-CSF
			4 *	30 *	0.7 *	20K	70	2	Programmable	CA3094A	† RCA
										CA3094B	† RCA
			6 *	—	0.3 *	45K *	70	3	General Purpose	µA709M	† TI
	700	100	25	—	50 *	10K	65	0	20 mA Output	TCA322	† Siemens
	750	250	6 *	65 *	15	15K	74	3	High Speed High Gain	µA715M	† Fairchild
	1000	300	20	30	15	50K	90	0	Precision, Audio	MA332	AnalogSys
		300 *	50	150	60	10K	70	1	High Power	1460	TeledyneP
	1000 *	5000 *	50	—	4000	50K	60	0	70 MHz -3db bandwidth, G=1-40	CLC210AI	Comlinear
									70 MHz -3db bandwidth, G=1-40, settles to 0.02% in 30 ns.	CLC210AM	† Comlinear
					8000	50K	60	0	200 MHz -3db bandwidth, G=1-40	CLC220AI	Comlinear
									200 MHz -3db bandwidth, G=1-40; settles to 0.02% in 15 ns.	CLC220AM	† Comlinear
	2000	400	—	38 *	25 *	0.6K	76	1	Large Signal Wideband	**CA3100**	**† RCA (3596)**
	5000 *	1000 *	20	150 *	160	15K	74	1	Wideband, Fast Settling	HA-5190	Harris
	6000 *	3000 *	50	—	4000	50K	60	0	100 MHz -3db bandwidth, G=1-40	CLC200AI	Comlinear
									100 MHz -3db bandwidth, G=1-40; settles to 0.02% in 25 ns.	CLC200AM	† Comlinear
	7000	2000	5 *	—	—	2K	70	1	702 Type	UPC51A	NEC
	10000	2000	10 *		1.7 *	1.4K	70	3	General Purpose	TL702M	† TI
	12000	5000	1.2 *	15 *	3 *	0.7K	70	1	6 Volt, Wideband	CA3010	† RCA
										CA3029	RCA
										CA3037	† RCA
	15000	4000	10 *	150 *	200 *	28K *	—	1	Wideband, Comp. for G>5	HA-5195	Harris
	20000	—	10	—	800	250	70	1	Fast, Slews 800 V/µs	NE5539	Signetics
										SE5539	† Signetics
		300 *	25	500 *	250	10K	80	1	Settles to 0.01% in 70 ns	1435	† TeledyneP
		6000	20	400 *	350	15K	60	—	Wideband, Fast Settling	**HA-2540-2**	**† Harris (3404)**
			20 *	600 *	550	15K	60	—	High Slew Rate, Wideband	**HA-2539-2**	**† Harris (3402)**
	24000	5000	3.5 *	50 *	7 *	2K	80	1	12 Volt, Wideband	CA3015	† RCA
										CA3030	RCA
										CA3038	† RCA
6	15000	4000	20	150	200	30K	74			1343	TeledyneP
6.0	0.025	0.002	15	1 *	1	75K	70	0	High Performance FET	LH0022C	National
	0.04	0.02	10 *	5 *	13 *	50K	80	1	MOS/FET Input, Bipolar/MOS Output	**CA080A**	**† RCA (3596)**
										CA080T	**† RCA (3596)**
										CA081A	**† RCA (3596)**
										CA081T	**† RCA (3596)**
	0.2	—	10 *	3 *	13 *	15K	80	0	Low Noise Bipolar-JFET	TL075M	† TI
		0.05	10 *	3 *	13	50K	80	0	Low Noise Bipolar-JFET	TL070M	† TI
										TL071M	† TI
		0.1	—	3	13 *	50K	70	0	Bipolar JFET	TL081A	Motorola
										TL081AC	TI
			10 *	1 *	3.5 *	40K	80	0	Low Power Bipolar JFET	TL061AC	TI
										TL061M	† TI

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† Military Temperature Range (−55° to 125°C)   * Typical Value

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LINEAR-Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift μV/°C	Band-width MHz	Slew Rate V/μs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source
Single Units											**(Cont'd)**
6.0	0.2	0.1	10 *	1 *	3.5 *	40K	80	0			(Cont'd)
									Programmable Bipolar JFET	MCE66	MCE
										TL066M	† TI
								1	Low Power Bipolar JFET	MCE60	MCE
										TL060AC	TI
										TL060M	† TI
					4 *	20K	80	0	Low Power, JFET Input	**HA-5062-2**	**† Harris (3432)**
										HA-5062A-5	**Harris (3432)**
				3 *	13 *	50K	80	0	Bipolar-JFET	MCE80	MCE
										TL080AC	TI
								1	Bipolar-JFET	TL080AC	TI
				4	15 *	25K	80	1	JFET Input	**HA-5082-2**	**† Harris (3436)**
						50K	80	1	JFET Input	**HA-5082A-5**	**Harris (3436)**
				4 *	13 *	25K	80	0	JFET Input	TL081M	† Motorola
	0.20	0.05	10 *	4 *	13 *	50K	80	0	Low Noise Bipolar-JFET	TL071AC	Motorola
										TL071AC	TI
	0.3	0.1	10 *	1 *	3.5 *	4K	80	0	Programmable Bipolar JFET	TL066AC	TI
	10	6	—	1 *	0.1	50K	70	0	Multi-Purpose, Programmable	SFC2776C	Thomson-CSF
	25	10	6 *	—	0.2 *	75K	70	0	Programmable	SG3250	SiliconG
		12	40	1 *	0.5 *	20K	80	0	Low Input Current 741	AD502J	AD
		20	15 *	—	0.5 *	20K	70	0	Low Input Current	ICL8008C	Intersil
		25	15 *	35 *	20	80K	74	1	Wideband, General Purpose	**AD507J**	**AD (3353)**
	30	30	—	0.05	4	70K	74	0	Wideband	HA2607	Intersil
			15 *	0.6	17	70K	74	0	Wideband	HA2627	Intersil
				4 *	5 *	100K	74	0	High Voltage	AM-464-2	Datel
										AM-464-2M	† Datel
										HA-2645	Harris
										1332	TeledyneP
			65	4 *	2.5	70K	74	0	to ±45V supply, 5A output	PA12	Apex
										PA12M	† Apex
				6 *	2.5	70K	74	0	to ±45V supply, 5A output	PA10	Apex
										PA10M	† Apex
	75	10	—	0.4	1.5	100K	80	—	Ultra-Low Power	**HA-5141A**	**Harris (3446)**
		20	—	—	—	60K	70	0	Programmable	μPC4250C	NEC
	100	30	5 *	—	0.3 *	25K	70	1	Supply to +-10 V	TCA520B	Signetics
	200	50	10	1	50	32	80	1	Differential Bipolar Input	MA318	AnalogSys
	250	50	—	1 *	0.5	25K	80	0	to 500 mA, Single Supply	μA759C	Fairchild
	500	200	—	—	0.5 *	5K	70	0	Short Circuit Protected	TBA221	Siemens
					5.5 *	5K	70	1	Adjustable Input Offset Voltage	TBB0748	Siemens
				1 *	0.5	20K	70	0	High Performance	SFC2741C	Thomson-CSF
								1	General Purpose	SFC2748C	Thomson-CSF
						20-50K	70	0	General Purpose Compensated	**AD741C**	**AD (3351)**
										IC450	Cherry
										μA741C	Fairchild
										HA17741	Hitachi
										MC1741C	Motorola
										LM741C	National
										μPC151	NEC
										μPC741	NEC
										PM-741C	PMI
										RC741	Raytheon
										CA741C	RCA
										μA741C	Signetics
										SG741C	SiliconG
										μA741C	TI
					0.5 *	20-50K	70	1	General Purpose	μA748C	Fairchild
										μA748C	Intersil
										MC1748C	Motorola
										CA748C	RCA
										SG748C	SiliconG
										μA748C	TI
					0.7	25K	70	0	High Speed 741	ICL741CHS	Intersil

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† Military Temperature Range (−55° to 125°C)   * Typical Value

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Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source
Single Units											**(Cont'd)**
6.0	500	200									(Cont'd)
				1 *	1	100K	70	1	0.2 amp Power	LH0041C	National
			3 *	1 *	10	20K	70	0	High Slew Rate 741	MC1741SC	Motorola
										SG741SC	SiliconG
									Low Noise 741	MC1741NC	Motorola
			5 *	0.8 *	5 *	20K	70	0	Wideband 741C	SG3217	SiliconG
			10 *	1 *	0.25	100K	90	2	High Gain, Instrumentation, 50 mA Output	LH0020C	National
					0.5 *	20K	—	0	Automotive Temperature Range (−40°C to 85°C)	SA741C	Signetics
						25K	70	0	Low Noise 741	ICL741CLN	Intersil
			15 *	0.2 *	0.2 *	20K	70	0	High Power	µA791C	Fairchild
										TBA0791	Thomson-CSF
			30	1 *	1 *	100K	70	0	1.0 amp Power	LH0021C	National
		300	10 *	12 *	50	25K	70	0	High Speed, Fast Setting	**AD518J**	**AD** (3353)
	1000	200	6	1 *	9 *	10K	70	1	General Purpose	SFC2861AM †	Thomson-CSF
		300	6 *	—	9 *	12K	65	1	General Purpose, OC Output	SFC2761C	Thomson-CSF
					18 *	12K	65	1	20 mA Output	TAA761	Siemens
	1200	500	5 *	4 *	100 *	10K	70	2	Gated	ZN424	Ferranti
	1500	200	—	0.5 *	35 *	20K	70	1	High Slew Rate	RC4531	Raytheon
				1 *	20 *	20K	70	1	High Slew Rate, High Performance	NE531	Signetics
7.0	100	10	—	0.4	1	100K	77	—	Ultra-Low Power	**HA-5141**	**Harris** (3446)
	200	10 *	10 *	10 *	130 *	25K	—	2	High Speed Inverting	ICL8017C	Intersil
	400	75	5 *	—	—	3K	63	0	250 mA Output, Electronic Shutdown	LM13080	National
				1 *	0.4 *	3K	63	0	250 mA Output, Electronic Shutdown	LM13080	AnalogSys
	6000	75	5 *	—	1.6	3K	63	0	450 mA Output, Electronic Shutdown	MA324	AnalogSys
7.5	7	—	10 *	20 *	30 *	—	70	0	Unity Gain, Noninverting	SFC2310	Thomson-CSF
		1	—	0.3 *	0.3 *	25K	80	1	Low Noise 308	LM308LN	Intersil
			30	1 *	0.3 *	25K	80	0	Micropower, Supply Current 800 µA	LM312	Motorola
										LM312	National
								1	Precision Bipolar	LM308	AMD
										AD308	**AD** (3351)
										LM308	Harris
										LM308	Intersil
										LM308	LinearTech
										LM308	Motorola
										LM308	National
										PM-308	PMI
										SG308	SiliconG
										SFC2308	Thomson-CSF
	250	50	—	0.8 *	0.5 *	25K	70	1	Low Noise 301A	ICL301ALN	Intersil
			30	1 *	0.5 *	25K	70	0	General Purpose, Compensated	LM307	Intersil
										LM307	LinearTech
										LM307	Motorola
										LM307	National
										CA307	RCA
										SG307	SiliconG
										LM307	TI
										SFC2307	Thomson-CSF
								1	General Purpose Uncompensated	**AD301A**	**AD** (3351)
										µA301A	Fairchild
										LM301A	LinearTech
										LM301A	Motorola
										LM301A	National
										µPC157	NEC
										µPC301	NEC
										CA301A	RCA
										SG301A	SiliconG
										LM301A	TI
										SFC2301A	Thomson-CSF
	1000	150	3 *	2 *	4.2 *	15K	80	2	General Purpose	MC1439	Motorola
		300	6 *	—	18 *	5K	60	0	20 mA Output	TCA321	Siemens
										TCA325	Siemens
	1500	250	6	65 *	10	10K	74	3	High Speed	µA715C	Fairchild
		500	6 *	—	0.3 *	15K	65	3	General Purpose	µA709C	TI
				1 *	0.5 *	20K	65	1	General Purpose	µA201	Fairchild

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† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers–Characteristics (Cont'd)

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Single Units (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift μV/°C	Band-width MHz	Slew Rate V/μs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source
7.5	1500	500	6 *	1 *	0.5 *	20K	65	1	General Purpose		(Cont'd)
										LM201	National
										SG201	SiliconG
			6-10 *	1 *	0.3 *	15K	65	3	General Purpose	μA709C	Fairchild
										LM709C	National
										RC709	Raytheon
								4	General Purpose	TAA521	Siemens
8.0	40	10	—	1 *	2.5 *	70K	70	1	High Voltage	LM344	National
	200	25	20 *	10 *	50	10K	80	0	High Slew Rate	**HA-2510**	**† Harris (3398)**
										HA2510	Intersil
				20 *	100	10K	80	1	100 v/μs, Gain =3	HA-2520	† Harris
										HA2520	† Intersil
			30	20 *	100	10K	80	1	High Speed, Fast Settling	AD509K	AD
										AD509S	† AD
	250	50	20 *	12 *	20	15K	74	0	High Slew Rate	**AM-450-2**	**Datel (2864)**
										AM-450-2M	**† Datel (2864)**
										HA-2502	† Harris
										HA-2505	Harris
										HA2502	† Intersil
										HA2505	Intersil
	40000	15000	25 *	70 *	250	3K	60 *	3	High Slew Rate	LH0024C	National
9.0	0.40	0.20	10 *	1 *	0.6 *	200K	70	0	JFET Input	TL091M	† TI
	250	50	30 *	8 *	15 *	50K	74	1	Four Addressable Inputs, single Amplifier	HA-2405	Harris
10.0	0.001 *	0.001 *	0.7 *	0.1 *	0.04 *	30K	70	1	Programmable, Low Bias	**TLC251C**	**TI (3689)**
										TLC271C	**TI (541,3687,3689)**
			1 *	0.012 *	0.001 *	20K *	77	1	Prog., Low Bias, Supply Volt. = 1 V	TLC251C	TI
				0.075 *	0.01 *	10K *	77	1	Prog., Low Bias, Supply Volt. = 1 V	TLC251C	TI
			5 *	2.3 *	4.5 *	10K	70	1	Programmable, High Bias	TLC251C	TI
										TLC271C	TI
	0.003	0.002	4 *	0.5 *	0.5 *	10K	70	0	Low Supply Voltage	**CA3420**	**† RCA (3594)**
	0.050	0.020 *	30	3 *	15 *	20K	86 *	0	High Voltage FET	3580J	Burr-Brown
		0.025	4 *	0.063 *	0.03 *	10K	70	0	Nanopower BiMOS	**CA3440**	**RCA (3594)**
	0.10	0.03	10	—	10	3K	90	1	FET Input, Low Noise	MA333	AnalogSys
				12	35	100K	90	0	JFET Input	MA334	AnalogSys
										MA400	AnalogSys
	0.15	0.05	20	1 *	0.3 *	20K	80	0	High Performance, Low Input Current	LM316	National
					10	30K	90	0	Low 1/f Noise	MA339	AnalogSys
	0.2	0.1	10 *	4 *	13 *	25K	70	0	Bipolar-JFET	MC35001	† Motorola
									JFET Input, High Speed	TDB0351	Thomson-CSF
	0.20	0.05	5 *	—	—	25K	80	—	Wideband Decompensated	LF357	Intersil
										LF357	Motorola
										LF357	National
										PM-357	PMI
				2.5	5 *	25K	80	0	Bipolar-JFET	LF355	AMD
										LF355	Intersil
										LF355	Motorola
										LF355	National
										PM355	PMI
				5	12 *	25K	80	0	Wideband-JFET	LF356	AMD
										LF356	Intersil
										LF356	Motorola
										LF356	National
										PM-356	PMI
										LF356	Signetics
			10 *	4 *	13 *	15K	80	0	Low Noise Bipolar-JFET	TL071	Motorola
										TL070AC	TI
										TL070C	TI
						25K	80	0	Low Noise Bipolar-JFET	TL071C	TI
			15	0.5	30	10K	80	0	Wideband Decompensated	LF357CP	AnalogSys
		0.1	10 *	3 *	13 *	50K	70	0	Bipolar JFET	μAF771	Fairchild
				4 *	13	25K	70	0	Bipolar-JFET	LF351	National
										LF351	Motorola

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LINEAR–Operational Amplifiers–Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source
Single Units											**(Cont'd)**
10.0	0.20	0.1	10 *	4 *							(Cont'd)
					13 *	25K	70	0	Precision BIFET	MC34001	Motorola
		2	10 *	4 *	13 *	15K	80	0	Low Noise Bipolar-JFET	TL075C	TI
	0.60	0.1	20 *	18 *	57 *	200K	80	0	Wideband-JFET	LF400	National
	1	0.25	10	5	10	50K	85	0	2.0 A Power	LH0101	National
										LH0101C	National
	10	3	150	—	250	0.7K	50	1	100 MHz	9906	† OEI
	30	10	—	1 *	2.5 *	70K	70	0	High Performance	MC1456	Motorola
	40	10	—	1 *	2 *	70K	70	0	High Voltage	MC1436	Motorola
										SG1436	SiliconG
			65	1 *	1.5	—	70	0	2 A Continuous	3573	Burr-Brown
						50K	70	0	Output 20V @ 10A	**OPA501R**	**† Burr-Brown (2850)**
										OPA501A	**Burr-Brown (2850)**
						500K	70	0	to ±30V supply, 5A adjustable output	PA11	Apex
									to ±30V supply, 5A output	PA73	Apex
	50	20	20 *	—	—	2K	55	3	Matched Input Transistors	LH0005	National
	100	25	25 *	—	—	2K	50	3	Matched Input Transistors	LH0005C	National
	250	50	20 *	20 *	80	7.5K	74	1	High Speed, Fast Settling	AD509J	AD
			25 *	12 *	15	15K	74	0	High Slew Rate	HA2507	Intersil
					40	7.5K	74	0	High Slew Rate	HA-2512	† Harris
										HA2512	Intersil
				20 *	80	7.5K	74	1	80 V/µs Gain=3	HA-2522	† Harris
										HA2522	† Intersil
			30 *	—	80	7K	74	1	Fast Slewing	3507J	Burr-Brown
				12 *	30	7.5K	74	0	High Slew Rate	HA2517	Intersil
					40	7.5K	74	0	High Slew Rate	HA-2515	Harris
										HA2515	Intersil
					80	7.5K	74	1	80 V/µs Gain = 3	HA-2525	Harris
										HA2525	Intersil
									80 V/µs Gain=3	**AM-452-2**	**Datel (2864)**
										AM-452-2M	**† Datel (2864)**
				20 *	60	7.5K	74	0	High Slew Rate	HA2527	Intersil
					80	7.5K	90 *	1	High Slew Rate	1322	TeledyneP
										1322-01	† TeledyneP
						70K	90 *	0	High Slew Rate/Temperature	**OPA12HT**	**† Burr-Brown (2851)**
	500	200	—	15 *	50	25K	70	0	Precision, High Speed	LM318	AMD
										µA318	Fairchild
										LM318	Harris
										LM318	LinearTech
										LM318	National
										LM318	TI
										SFC2318	Thomson-CSF
			5 *	1 *	25	25K	60	1	0.5 A, Wideband	LH0061C	National
		300	10	2	10	50K	70	1	Up to ±40 V Output	MA700	AnalogSys
	750	—	—	—	—	14K	—	1	Telephone Channel Amplifier	LS045	SGS
	1000	300	6 *	—	9 *	5.6K	60	1	General Purpose, OC Output	SFC2861C	Thomson-CSF
					18 *	0.56K	60	1	to 90 mA Output	TAA861	Siemens
										TAA865	Siemens
	1000 *	5000 *	50	—	6000	5K	60	0	150 MHz -3db bandwidth, G=1-40	CLC103AI	Comlinear
	1200	300	6	1 *	9 *	5.6K	65	1	General Purpose	SFC2861AC	Thomson-CSF
	3000	300	16	20	10	100K	60	2	Up to 400 mA Output	MA206	AnalogSys
	15000	5000	5 *	—	1.7 *	1K	65	3	General Purpose	TL702C	TI
12.0	50	15	65	1 *	1.5	500K	70	0	to ±28V supply, 5A adjustable output	PA01	Apex
	90	25	—	1 *	2 *	50K	50	0	High Voltage	MC1436C	Motorola
										SG1436C	SiliconG
		30	—	1 *	2.5	25K	110 *	0	High Performance	MC1456C	Motorola
										LM1436	National
14.0	200	15	50 *	—	—	10K	65	1	Darlington Input	TCA312	† Siemens
										TCA332	† Siemens
15	0.065	0.01	35	100	70	100	70			1345	TeledyneP
	20000	6000	20	9.5	600	30K	60			1342	TeledyneP
				400	400	30K	60			1341	TeledyneP
											(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

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Master Selection Guide

LINEAR-Operational Amplifiers-Characteristics (Cont'd)

Single Units (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift μV/°C	Band-width MHz	Slew Rate V/μs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	
15												(Cont'd)
	35000	—	33	80	1300	1				1359	TeledyneP	
										1359-01	† TeledyneP	
15.0	0.010	—	25	2 *	3	50K	72	0	High Performance, Low Bias	1421-02	TeledyneP	
	0.015	—	50	2 *	3	50K	72	0	High Performance, Low Bias	1421-01	TeledyneP	
	0.050	—	50	2 *	3	50K	72	0	High Performance FET	1421	TeledyneP	
		0.030	8 *	4 *	10 *	50K	70	0	MOS FET, Single Supply	CA3160	† RCA	
				4.5 *	9 *	20K	70	0	MOS FET, Single Supply	CA3140	† RCA	
			10 *	4 *	10 *	50K	70	1	MOS FET Single Supply, Strobe	CA3130	† RCA	
				5 *	13 *	50K	70	0	FET Input, Bipolar/MOS Output	**CA081**	**RCA**	**(3596)**
										CA081C	**RCA**	**(3596)**
								1	FET Input, Bipolar/MOS Output	**CA080**	**RCA**	**(3596)**
										CA080C	**RCA**	**(3596)**
			25 *	1	1.6	80K	70	0	Low Power	ICL7611C	Intersil	
									Low Power, Extended CMVR	ICL7612C	Intersil	
									Low Power, Input Protected	**ICL7613DC**	**Intersil**	**(3481)**
								1	Low Power	**ICL7614DC**	**Intersil**	**(3481)**
									Low Power, Input Protected	**ICL7615DC**	**Intersil**	**(3481)**
	0.065	0.005	35	15 *	50	25K	70	0	Precision, High Speed, FET	LH0062C	National	
		0.01	20 *	100 *	50	25K	70	1	Wideband, High Slew Rate	HA-5162-5	Harris	
	0.20	0.05	10 *	1 *	0.5 *	25K	70	0	JFET-741	LF13741	National	
			25 *	50 *	350	1K	50	2	Ultra Fast FET	LH0032C	National	
										ADLH0032C	AD	
		0.10	10 *	3 *	13 *	50K	70	0	Bipolar-JFET	μA771L	Fairchild	
	0.4	0.05	—	3 *	13 *	25K	70	1	Low Noise Bipolar-JFET	MCE70	MCE	
		0.2	—	3	13 *	25K	70	0	Bipolar JFET	TL081	Motorola	
										TL081	TI	
			10 *	1 *	3.5 *	3K	70	0	Low Power Bipolar-JFET	TL061C	TI	
									Programmable Bipolar JFET	TL066C	TI	
								1	Low Power Bipolar-JFET	TL060C	TI	
					4 *	10K	70	0	Low Power, JFET Input	**HA-5062-5**	**Harris**	**(3432)**
				3 *	13 *	25K	70	0	Bipolar-JFET	μPC4081	NEC	
								1	Bipolar-JFET	TL080C	TI	
				4	15 *	25K	70	—	JFET Input	**HA-5082-5**	**Harris**	**(3436)**
	50	25	12 *	—	—	2K	60	1	High Output Current	SFC2315	Thomson-CSF	
	750	150	30	300	15	10K	84	1	High Power	MA329	AnalogSys	
	20000	6000	20	400 *	350	10K	60	—	Wideband, Fast Settling	**HA-2540-5**	**Harris**	**(3404)**
			20 *	600 *	550	10K	60	—	High Slew Rate, Wideband	**HA-2539-5**	**Harris**	**(3402)**
20.0	0.00025	—	60	0.5 *	3	40K	80	0	Electrometer, FET	AD523L	AD	
	0.0005	—	30	0.5 *	3	40K	80	0	Electrometer, FET	AD523K	AD	
	0.010	—	25	0.75 *	0.5 *	50K	70	0	Low Noise FET	AD514L	AD	
		0.002 *	25	1 *	2.5	31K	86 *	0	High Performance, Low Bias FET	3503B	Burr-Brown	
										3503S	† Burr-Brown	
	0.020	—	25	0.75 *	0.5	50K *	70	0	Low Noise FET	AD514K	AD	
			50	0.75 *	0.5 *	50K *	70	0	Low Noise FET	AD514S	† AD	
		0.0005 *	75	1 *	6 *	50K	70	0	High Performance FET	ICL8007M	† Intersil	
	0.025	—	25	1 *	6 *	50K	70	0	Low Cost FET Input	**AD540K**	**AD**	**(3351)**
			50	1 *	0.5 *	25K	80	0	FET	AD3542J	AD	
					6 *	50K	70	0	Low Cost FET Input	**AD540S**	**† AD**	**(3351)**
		0.002 *	50	1 *	0.5 *	25K	80 *	0	Low Noise	**3542J**	**Burr-Brown**	**(2850)**
										3542S	**† Burr-Brown**	**(2850)**
		0.010	20	1 *	1.5	50K	70	0	Low Cost FET Input	LH0042	† Intersil	
										LH0042	† National	
	0.050	—	25	1 *	6 *	25K	70	0	Low Cost FET	AD0042C	AD	
		0.005	25	1 *	1	25K	70	0	Low Cost FET	LH0042C	Intersil	
										LH0042C	National	
	0.10	—	25	1 *	3	50K	80	0	Low Cost FET Input	**AD503K**	**AD**	**(3351)**
										AD503S	**† AD**	**(3351)**
	0.20	0.15	20 *	3 *	6 *	25K	64	0	High Slew Rate FET	μA740	† Intersil	
	0.30	—	100	10 *	250 *	80	80		FET Input	AH0008	OEI	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers–Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift μV/°C	Band-width MHz	Slew Rate V/μs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source
Single Units											**(Cont'd)**
20.0											(Cont'd)
	50	20	12 *	—	9 *	0.5K	60	1	Darlington Input	TBB1331A	Siemens
	200	25	12 *	—	—	6K	60	0	Darlington Input	TCA311 TCA315	Siemens Siemens
								1	Darlington Input	TCA331	Siemens
30.0	0.001	0.0002 *	50	1 *	2.5	20K	86	0	Low Bias FET	ICL8007AC ICL8007AM	Intersil † Intersil
	30000	10000	150	200	300	1K	50	0	Wideband	9916	† OEI
	50000	20000	100	300	1K	4K	90	1	Wideband	9914	OEI
35.0	2	0.1	150	100	300	100K	70	0	High Slew Rate	HDS-060	AD
50.0	0.00001 0.0001	— —	— —	— —	0.5 * 0.5 *	20K 20K	60 60	0 0	Ultra low Bias FET Ultra low Bias FET	ICH8500A ICH8500	Intersil Intersil
	0.001	0.0005 *	90	0.5 *	3	20K	70	0	Electrometer, FET	AD523J	AD
	0.015	—	75	1 *	3	20K	70	0	Low Cost FET Input	**AD503J**	**AD (3351)**
	0.025	0.005 *	75	1 *	2.5	20K	86 *	0	High Performance, Low Bias FET	3503A 3503R	Burr-Brown † Burr-Brown
	0.050	—	75	0.75 * 1 *	0.5 * 6 *	20K 20K	70 70 72	0 0 0	Low Noise FET Low Cost FET High Performance FET	AD514J **AD540J** 1424	AD **AD (3351)** TeledyneP
		0.0005 *	75	1 *	6 *	20K	70	0	High Performance, FET	ICL8007C	Intersil
110.0	0.20	0.15	20 *	3 *	6 *	25K	64	0	High Slew Rate FET	μA740C	† Intersil
Dual Units											
—	8000 *	—	—	30	60 *	4K	—	0	GB Product = 400 MHz	LM159 LM359	† National National
0.06	3	2.8	0.9	0.4	0.1	400K	110	0	Ultra Low Offset Matched	LT1002AM LT1002AC	† LinearTech LinearTech
0.08	40	35	1	5	1.7	250K	114	0	Ultra Low Noise Instrumentation	**MPOP-227A MPOP-227E OP-227A OP-227E**	**† MicroPwr (3529) MicroPwr (3529) † PMI (3566) PMI (3566)**
0.1	3.5	3.5	0.4	1.2	0.25	500K	—	0	Ultra Low Offset Voltage	**MPOP-207A MPOP-207E**	**† MicroPwr (3529) MicroPwr (3529)**
0.10	4.5	4.2	1.3	0.4	0.1	350K	110	0	Ultra Low Offset Matched	LT1002C LT1002M	LinearTech † LinearTech
	5	0.5	10	0.8	1.12 *	40K	104	0	Precision, Low Input Current	**MPOP-12C MPOP-12G**	**† MicroPwr (3529) MicroPwr (3529)**
0.12	55	50	1.5	5	1.7	250K	106	0	Ultra Low Noise Instrumentation	**MPOP-227B MPOP-227F OP-227B OP-227F**	**† MicroPwr (3529) MicroPwr (3529) † PMI (3566) PMI (3566)**
0.15	2	0.2	2.5	0.8	1.12 *	80K	104	0	Improved 108A, Low Bias, Compensated	**MPOP-12A MPOP-12E**	**† MicroPwr (3529) MicroPwr (3529)**
	7	6	1.8	1.2 *	0.25 *	120K	100	0	Ultra Low Offset Voltage, Low Drift	μA714C **MP5507C OP-07C**	Fairchild **MicroPwr (3529) PMI (3566)**
	7.0	6.0	0.5 *	0.5 *	0.17 *	120K	100	0	Low Noise	μPC454	NEC
	20	2	2	100 *	—	500K	96	0	Low Power, Single/Dual Supply	**OP-220A OP-220E**	**† PMI (3566) PMI (3566)**
	80	3	1.5	—	0.2	1.5M	95	0	Low Power, Precision Matched	OP-221A OP-221E	† PMI PMI
0.18	80	75	1.8	5	1.7	200K	106	0	Ultra Low Noise Instrumentation	**MPOP-227C MPOP-227D**	**† MicroPwr (3529) MicroPwr (3529)**
			2	5	1.7	200K	106	0	Ultra Low Noise Instrumentation	**OP-227C OP-227G**	**† PMI (3566) PMI (3566)**
0.25	0.035	0.002	2.5	1 *	3 *	250K	80	—	Ultra Low Drift BiFET	**AD647L**	**AD (3350,3351)**
0.3	0.050 6	0.010 6	3 1.3	1 * 1.2	0.3 * 0.25	300K 400K	110 —	0 0	Dual LM11, High Performance Ultra Low Offset Voltage	LH2011 **MPOP-207B MPOP-207F**	† National **† MicroPwr (3529) MicroPwr (3529)**
	25	2.5	5	100 *	—	300K	90	0	Low Power, Single/Dual Supply	**OP-220B OP-220F**	**† PMI (3566) PMI (3566)**

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers–Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift μV/°C	Band-width MHz	Slew Rate V/μs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source
Dual Units											**(Cont'd)**
0.3											(Cont'd)
	100	5	2	—	0.2	1M	90	0	Low Power, Precision Matched	OP-221B	† PMI
										OP-221F	PMI
0.30	2	0.2	3.5	0.8	1.12 *	80K	104	0	Improved 108A, Low Power, Compensated	**MPOP-12B**	**† MicroPwr (3529)**
										MPOP-12F	**MicroPwr (3529)**
0.5	0.035	0.002	5	1 *	3 *	250K	80	—	Ultra Low Drift BiFET	**AD647K**	**AD (3350,3351)**
										AD647S	**† AD (3350,3351)**
										AD647S/883B	**† AD (3350,3351)**
		0.005 *	5	2 *	3 *	250K	80	0	Dual 544	**AD644L**	**AD (3351)**
			5 *	1 *	3 *	300K *	80	0	Dual 542	**AD642L**	**AD (3351)**
			15	2 *	3 *	250K	80	0	Dual 544	**AD644S**	**† AD (3351)**
	0.06	0.025	5 *	—	13 *	50K	80	0	Precision BIFET	MC35022A	† Motorola
	0.075	0.03	5 *	—	13 *	50K	80	0	Precision BIFET	MC34003A	Motorola
										MC34022A	Motorola
	2	0.2	15	1 *	0.3 *	80K	96	1	Dual 108A	LH2108A	† Intersil
										LH2108A	† National
										LH2208A	National
										PM-2108A	**† PMI (3566)**
										PM-2208A	PMI
	3	2.8	2	0.6 *	0.17 *	150K	110	0	Dual Matched Instrumentation	**OP-10**	**† MicroPwr (3529)**
										OP-10A	**† MicroPwr (3529)**
										OP-10E	**MicroPwr (3529)**
	7	1	30	1 *	0.3 *	80K	96	1	Dual 308A	LH2308A	Intersil
										LH2308A	National
										PM-2308A	PMI
	20	0.1	10	3	13	50K	80	0	Bipolar-JFET	TL287C	TI
										TL287M	† TI
	120	7	3	—	0.2	800K	80	0	Low Power, Precision Matched	OP-221C	† PMI
										OP-221G	PMI
0.6	0.10	0.01	2	0.8 *	0.3	250K	110	0	Dual LM11, High Performance	LH2011B	† National
	40	4	10	100 *	—	500 *	76	0	Low Power, Single/Dual Supply	**OP-220C**	**† PMI (3566)**
										OP-220G	**PMI (3566)**
0.75	50	2	8	0.8	0.5	100K	90	0	Dual Matched	**OP-04A**	**† PMI (3566)**
										OP-04E	**PMI (3566)**
										OP-14A	**† PMI (3566)**
										OP-14E	**PMI (3566)**
									OP-04 with Internally Connected Vcc Terminals	MC35022	† Motorola
		5	8	0.8	0.25	100K	80	0	Dual Matched	**MPOP-03E**	**MicroPwr (3529)**
										MPOP-04A	**† MicroPwr (3529)**
										MPOP-04E	**MicroPwr (3529)**
										MPOP-14A	**† MicroPwr (3529)**
										MPOP-14E	**MicroPwr (3529)**
									MPOP-04 With Internally Connected Vcc Terminal	**MPOP-03A**	**† MicroPwr (3529)**
1.0	0.035	0.005 *	10	1 *	3 *	300K *	80 *	0	Dual 542	**AD642K**	**AD (3351)**
										AD642S	**† AD (3351)**
				2 *	3 *	250K	80	0	Dual 544	**AD644K**	**AD (3351)**
	0.05	0.025	10	1	1	50K	80	0	Low Power BIFET	LF422A	National
										LF442A	National
	0.075	0.005	10	1 *	3 *	100K	76	—	Ultra Low Drift BIFET	**AD647J**	**AD (3350,3351)**
		0.050	5 *	4 *	13 *	50K	80	0	BIFET	MC35022B	† Motorola
	0.18	0.02	3	0.8 *	0.3	90K	—	0	Dual LM11, High Performance	LH2011C	National
	0.2	0.1	10 *	4 *	13 *	25K	70	0	Bipolar-JFET	LF153	Harris
										LF253	Harris
		0.10	10	3	10	50K	80	0	Wideband JFET	LF412A	National
	40	5	10	0.15 *		300K	86 *	0	Micropower, Precision	**OP-220H**	**PMI (3566)**
	500	600	—	2 *	50 *	20K	80	0	Transconductance Amplifier	LM11700A	National
										LM13700A	National
1.3	7	6	4.5	1.2 *	0.25 *	120K	100	0	Dual Matched Instrumentation	OP-10C	PMI
						250K	100	0	Dual Matched Instrumentation	**MP5510C**	**MicroPwr (3529)**
										OP-10C	**MicroPwr (3529)**

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers–Characteristics (Cont'd)

Dual Units (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source
2.0	0.02	0.01	5 *	4 *	10 *	50K *	86	0	Dual 3160	**CA3260B**	**RCA** (3595)
	0.05	0.030	10 *	1	1.6	80K *	70	0	Low Power, Dual 747	**ICL7622AC**	**Intersil** (3481)
										ICL7622AM	† **Intersil** (3481)
									Low Power, Dual 1458	**ICL7621AC**	**Intersil** (3481)
										ICL7621AM	† **Intersil** (3481)
		0.1	20	3	10	50K	80	0	Dual 0351A	TDB0353A	Thomson-CSF
	0.075	0.025	10 *	4 *	13 *	50K	80	0	Precision BIFET	MC35002A	† Motorola
		0.030	5 *	4 *	13 *	50K	80	0	Precision BIFET	MC34022A	Motorola
		0.075 *	20 *	1 *	3 *	200K *	76 *	0	Dual 542	**AD642J**	**AD** (3351)
				2.0	3 *	100K	76	0	Dual 544	**AD644J**	**AD** (3351)
	0.10	0.05	10 *	3 *	13 *	50K	80	0	Bipolar-JFET	µA772A	Fairchild
										µA772AM	† Fairchild
				4 *	13 *	50K	80	0	Dual 351A	LF353A	National
									Precision BIFET	MC34002A	Motorola
	0.15	0.05	20	0.06	10	3K	100	—	JFET Input	MA406	AnalogSys
		0.07	5 *	4 *	13 *	25K	80	0	Precision BIFET	MC35022	† Motorola
	0.2	0.1	10 *	4 *	13 *	25K	80	0	Bipolar-JFET	LF353A	Harris
	2	0.2	15	1 *	0.3 *	50K	85	1	Dual 108	LH2108	† National
										LH2208	National
										PM-2108	**PMI** (3566)
										PM-2208	PMI
	50	10	15	1 *	—	50K	70	0	Low Power, Single Supply	CA158A	† RCA
		25	5	1.5 *	0.8	100K *	100 *		Matched Amplifier Pairs	**3500MP**	**Burr-Brown** (2850,2853)
	75	5	10	0.8	0.5	50K	80	0	Dual Matched	**MPOP-04**	† **MicroPwr** (3529)
										MPOP-04C	**MicroPwr** (3529)
										MPOP-14C	**MicroPwr** (3529)
									MPOP-04 With Internally Connected Vcc Terminal	**MPOP-03**	† **MicroPwr** (3529)
										MPOP-03C	**MicroPwr** (3529)
							90	0	Dual Matched	**OP-04**	**PMI** (3566)
										OP-04C	**PMI** (3566)
										OP-14C	**PMI** (3566)
		10	15	1 *	0.5 *	50K	80	1	Dual LM101A High Performance	LH2101A	Intersil
										LH2101A	† National
										LH2201A	National
										LH2101A	Raytheon
										LH2101A	**Signetics** (526)
	100	20	10	5.7 *	16 *	220K	100 *	0	Precision Bipolar-JFET	OP-215B	† PMI
										OP-215F	PMI
	200	75	3 *	8 *	1	100K	86	0	Low Noise, High Performance	**HA-5102-2**	† **Harris** (3459)
										HA-5102-5	**Harris** (3459)
				60 *	12	100K	86	1	Wideband	**HA-5112-2**	† **Harris** (3459)
										HA-5112-5	**Harris** (3459)
	800	200	—	10 *	13	50K	80	1	Dual 5534	**SE5532**	† **Signetics** (526,3644)
										SE5532A	† **Signetics** (526,3644,3644)
	5000	600	7 *	2 *	50 *	—	80	0	Transconductance Amplifier, G = 12000 µmho.	**LM13600A**	**Signetics** (3636)
3.0	0.03	0.01	10 *	5 *	13 *	50K	80	0	MOS/FET Input, Bipolar/MOS Output	**CA082B**	**RCA** (3596)
										CA083B	**RCA** (3596)
	0.04	0.02	10 *	5 *	13 *	50K	80	0	MOS/FET Input, Bipolar/MOS Output	**CA082AT**	† **RCA** (3596)
	0.15	0.03	10	0.11	10	3K	90	—	Low Wideband Noise	MA345	AnalogSys
	0.2	0.1	10 *	1 *	3.5 *	4K	80	0	Low Noise Bipolar-JFET	TL062BC	TI
				3 *	15 *	50K	80	0	Bipolar-JFET	TL082B	Motorola
										TL082BC	TI
										TL288C	TI
										TL288M	† TI
			20	0.7	8	25K	70	0	Wideband JFET	LF412	National
	0.20	0.05	10 *	4 *	13 *	50K	80	0	Low Noise Bipolar-JFET	TL072BC	Motorola
	5	3	10 *	25 *	0.1 *	40K	80	0	Programmable	HA-2730	† Harris
		5	—	1	1	100K	100	0	Low Noise	SE5512	† Signetics

(Continued)

† Military Temperature Range (−55° to 125°C)   * Typical Value

Bold face indicates additional data is provided on the page noted.

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LINEAR–Operational Amplifiers–Characteristics (Cont'd)

Dual Units (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Bandwidth MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source
3.0											(Cont'd)
	15	5	—	0.25	0.16	100K	—	0	Low Power	LH2250	† National
										LH2250C	National
				.25 *	0.16 *	100K	70	0	Programmable Dual LM4250	LH24250	† National
	20	7.5	5 *	0.27 *	0.16 *	50K	70	0	Low Power Adjustable Current	ICL8022M	† Intersil
	80	15	15	1 *	—	50K	70	0	Low Power, Single Supply	LM258A	National
										CA258A	RCA
		30	15	0.44	0.3	50K	80	0	Dual 741	µA747AM	† Fairchild
										µA747EC	Fairchild
										LM747A	† National
										LM747E	National
	100	30	8 *	8 *	2	25K	80	0	High Slew Rate	**HA-2650**	**† Harris** (3414)
			20	1 *	—	25K	65	0	Low Power, Single Supply	LM358A	National
										CA358A	RCA
	500	200	—	4	3 *	—	—	—	High Performance, Low Noise	**RC2041**	**Raytheon** (3592)
	750	400	3 *	—	2 *	20K	70	3	Audio Preamp	µA749C	Fairchild
	1000	200	—	8	6 *	—	—	—	High Performance, Low Noise	**RC2043**	**Raytheon** (3592)
	5000	700	5 *	9 *	125 *	50K	80	1	Transconductance Amp	**CA3280**	**RCA** (3597)
3.5	300	50	5 *	1.5	1 *	—	86	0	High Performance	TEB1033	Thomson-CSF
4.0	80	20	4 *	1 *	10	50K	70	0	High Slew Rate	SE5535	† Signetics
	150	25	—	—	—	50K	70	0	2 Op Amp/Comparators	LM192	† National
	200	50	20	5.4 *	15 *	200K	96 *	0	Precision Bipolar-JFET	OP-215C	† PMI
										OP-215G	PMI
	350	100	3 *	—	0.5 *	50K	80	0	Dual 222	TBC0747	† Siemens
	500	600	—	2 *	50 *	20K *	80	0	Transconductance Amplifier	LM13700	† National
	700	100	25	—	—	18K	70	0	20 mA Output	TAA2762	† Siemens
					9 *	18K	70	0	General Purpose, OC Output	TEC1761M	† Thomson-CSF
	800	150	—	10 *	9	25K	70	1	Low Noise	NE5532	TI
										NE5532A	TI
	1500	300	—	10 *	13 *	25K	70	1	Dual 5534	**XR5532**	**Exar** (3378)
										XR5532A	**Exar** (3378)
										XR5533	**Exar** (3379)
										XR5533A	**Exar** (3379)
										NE5532	**Signetics** (3644)
										NE5532A	**Signetics** (3644,3644)
										NE5533	**† Signetics** (3646)
			5 *	10 *	13 *	25K	70	3	Can be compensated with 1 capacitor, but reduces BW and slew rate.	**NE5533A**	**Signetics** (3646)
5.0	0.03	0.02	6 *	4 *	10 *	50K *	70	0	Dual 3160	**CA3260AE**	**RCA** (3595)
										CA3260AT	**† RCA** (3595)
	0.04	0.02	15 *	45 *	9 *	20K	70	0	Dual 3140A, MOS FET	**CA3240A**	**RCA** (3595)
	0.050	0.030	15 *	1	1.6	80K	70	0	Low Power, Dual 1458	**ICL7621BC**	**Intersil** (3481)
										ICL7621BM	**† Intersil** (3481)
									Low Power, Dual 747	**ICL7622BC**	**Intersil** (3481)
										ICL7622BM	**† Intersil** (3481)
	0.10	0.05	10 *	1 *	1 *	25K	70	0	Low Power JFET	LF442	National
		0.10	10 *	3 *	13 *	50K	80	0	Bipolar JFET	µA772B	Fairchild
										µA772BM	† Fairchild
	0.2	0.1	10 *	4 *	13 *	25K	80	0	Bipolar-JFET	LF353B	Harris
			30	4 *	13 *	50K	80	0	Dual 0351B	TDB0353B	Thomson-CSF
	0.20	0.1	10 *	4 *	13 *	25K	70	0	Bipolar-JFET	MC35002B	† Motorola
		0.10	10 *	3	10	50K	80	0	Dual 151	LF153	† National
				4 *	13 *	50K	80	0	Dual 351B	LF353B	National
	7.5	3	3 *	1 *	15 *	200K	70	0	Multi-Purpose Programmable	µA776M	† Fairchild
	10	5	10 *	—	0.1 *	25K	74	0	Programmable	HA-2735	Harris
		10	—	1	1	100K	100	0	Low Noise	NE5512	Signetics
										NE5517	**Signetics** (3642)
										NE5517A	**Signetics** (3642)
	100	25	10	0.8	0.25	50K	70	0	Dual Matched	**OP-04B**	**† PMI** (3566)
										OP-04D	**PMI** (3566)
			20	0.8	0.25	25K	70	0	Dual Matched, High Performance	**OP-14D**	**PMI** (3566)
						50K	70	0	Dual Matched	**MPOP-04B**	**† MicroPwr** (3529)
											(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Dual Units (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Bandwidth MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source
5.0	100	25	20	0.8	0.25	50K	70	0	Dual Matched		(Cont'd)
										MPOP-04B	**MicroPwr (3529)**
										MPOP-14B	† **MicroPwr (3529)**
										MPOP-14D	**MicroPwr (3529)**
									MPOP-04 With Internally Connected Vcc Terminal	**MPOP-03B**	**MicroPwr (3529)**
										MPOP-03D	**MicroPwr (3529)**
		40	—	0.8 *	0.5 *	4K	60	0	Low Power	TL022M	† TI
		50	20	0.8	0.25	25K	70	0	Dual Matched, High Performance	**OP-14B**	**PMI (3566)**
	150	30	7 *	1 *	—	50K	70	0	Half LM124	LM158	† Motorola
										LM158	† National
										LM258	National
										CA158	† RCA
										CA258	RCA
										LM158	† Signetics
										LM258	Signetics
										SE532	† Signetics
										LM158	† TI
										TDC0158	† Thomson-CSF
	200	60	8 *	8 *	2	20K	74	0	High Slew Rate	HA-2655	Harris
		80	—	0.8 *	0.5 *	1K	60	0	Low Power	TL022C	TI
	250	50	—	—	—	25K	65	0	2 Op Amp/Comparators	LM292	National
										LM392	National
	500	50	10 *	1 *	0.6 *	50K	70	0	Single Supply	MC3558	† Motorola
		200	—	—	10	50K	70	0	High Slew Rate 1558	MC1558S	† Motorola
				1 *	0.5 *	50K	70	0	Dual 741	SFC2747M	† Thomson-CSF
					0.8 *	50K	70	0	Dual 741	SFC2458M	† Thomson-CSF
				2	1.5 *	50K	70	0	Dual Wideband 741	RM4558	† Raytheon
				2.5	1	20K	70	0	General Purpose	SE4558	† Signetics
					1.5	50K	70	0	Dual Wideband 741	TDC4558	† Thomson-CSF
					1.5 *	50K	70	0	Dual Wideband 741	MC4558	† Motorola
										MC4558A	Motorola
									Low Noise	MC4558N	† Motorola
				3	1.5 *	50K	70	0	3 MHz Min. Bandwidth	RM4559	† Raytheon
			1.5 *	1 *	0.3 *	25K	70	3	Matched Dual 709	RM1537	† Raytheon
			2-15 *	1 *	0.5 *	50K	70	0	Dual 741	µA1558M	† Fairchild
										µA747M	† Fairchild
										MC1558	† Motorola
										MC1747	† Motorola
										LM1558	† National
										LM747	† National
										PM-1558	† PMI
										PM-747	† PMI
										RM1558	† Raytheon
										RM747	† Raytheon
										CA1558	† RCA
										CA747	† RCA
										MC1558	† Signetics
										µA747	† Signetics
										SG1558	† SiliconG
										SG747	† SiliconG
										MC1558	† TI
										µA747M	† TI
										TA75458	Toshiba
										TA75747	Toshiba
									Low Noise	MC1558N	† Motorola
				3 *	0.25	25K	70	3	Dual MC1709	MC1537	† Motorola
	1000	200	—	0.12	7 *	30K	80	0	Low Noise, High Speed	LM833	National
	5000	600	7 *	2 *	50 *	—	80	0	†Transconductance Amplifier, G = 13000 µmho.	**LM13600**	**Signetics (3636)**
	7000	8000	6000	—	2 *	50	80	0	Transconductance Amplifier	LM13600	National
6.0	0.04	0.02	10 *	5 *	13 *	50K	80	0	MOS/FET Input, Bipolar/MOS Output	**CA082A**	**RCA (3596)**
										CA082T	† **RCA (3596)**
										CA083A	**RCA (3596)**

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers–Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift μV/°C	Band-width MHz	Slew Rate V/μs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source
Dual Units											**(Cont'd)**
6.0											(Cont'd)
	0.2	0.05	10 *	3 *	13 *	50K	80	0	Low Noise Bipolar-JFET	TL072M	† TI
		0.1	10 *	1 *	3.5 *	4K	80	0	Low Power Bipolar-JFET	TL062AC	TI
										TL062M	† TI
				3 *	13 *	50K	80	0	Bipolar JFET	**XR082**	**Exar (3376)**
										XR082M	**† Exar (3376)**
										XR083	**Exar (3376)**
										XR083M	**† Exar (3376)**
										TL082A	Motorola
										TL082AC	TI
										TL082M	† TI
										TL083AC	TI
										TL083M	† TI
				4 *	13 *	25K	80	0	JFET Input	TL082M	† Motorola
	0.20	0.05	10 *	4 *	10	35K	70	0	Low Noise Bipolar JFET	TL072M	† Motorola
					13 *	50K	80	0	Low Noise Bipolar-JFET	TL072AC	Motorola
										TL072AC	TI
	10	6	3 *	1 *	15 *	50K	70	0	Multi-Purpose Programmable	μA776C	Fairchild
	30	10	—	0.25 *	0.16 *	75K	70	0	Programmable Dual LM4250	LH24250C	National
			5 *	0.27 *	0.16 *	50K	70	0	Low Power Adjustable Current	ICL8022C	Intersil
	75	10	—	0.4	1.5	100K	80	—	Ultra-Low Power	HA-5142A	Harris
	150	40	6 *	1 *	10	50K	70	0	High Slew Rate	NE5535	Signetics
	250	50	7 *	1 *	0.6 *	25K	65	0	Half LM244/324	LM258	Motorola
										LM358	Motorola
										NE532	Signetics
		75	10 *	1 *	0.6 *	20K	70	0	Single Supply, I/O Operates to Ground	μA798C	Fairchild
	500	200	—	—	0.5 *	5K	70	0	Dual 221	TBB0747	Siemens
										TBB1458	Siemens
					1 *	20K	70	0	Wideband 741	μPC4557	NEC
					2 *	20K	70	0	Wideband 741	μPC4559	NEC
					5 *	20K	70	0	Wideband 741	μPC4556	NEC
				1 *	0.5 *	20-50K	70	0	Dual 741C	IC900	Cherry
										XR1458	Exar
										μA1458C	Fairchild
										μA747C	Fairchild
										MC1458	Motorola
										MC1747C	Motorola
										LM1458	National
										LM747C	National
										μPC251	NEC
										AN6550	**Panasonic (3556)**
										AN6551	**Panasonic (3556)**
										AN6552	**Panasonic (3556)**
										RC747	Raytheon
										CA747C	RCA
										μA747C	Signetics
										SG747C	SiliconG
										μA747C	TI
						25K	70	0	Dual 741	SFC2747C	Thomson-CSF
					0.8 *	20K	70	0	Dual 741	SFC2458C	Thomson-CSF
				2	0.5 *	20K	70	0	Dual Wideband 741C	MC4558C	Motorola
									Low Noise	MC4558NC	Motorola
					1	20K	70	0	Dual Wideband 741	TDB4558	Thomson-CSF
						50K	70	0	General Purpose	NE4558	Signetics
				3	1.5	20K	70	0	3 MHz Min. Bandwidth	**RC4559**	**Raytheon (3592)**
				3 *	1	20K	70	0	Low Noise	**RC4739**	**Raytheon (3592)**
									Wideband 741	XR4558	Exar
										μPC4558	NEC
										RC4558	**Raytheon (3592)**
										RC4558	TI
									Low Noise	**XR4739**	**Exar (3378)**
				10 *	2.8 *	20K	70	0	Wideband 741	μPC4560	NEC
			10 *	1 *	0.5 *	25K	70	0	Automotive Temperature Range (−40°C to 85°C)	SA747C	Signetics
											(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers–Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift μV/°C	Bandwidth MHz	Slew Rate V/μs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	
Dual Units												**(Cont'd)**
6.0	500	200	10 *	1 *								(Cont'd)
					0.8 *	20K	70	0	Low Noise	MC1458N	Motorola	
					10	20K	70	0	High Slew Rate 1458	MC1458S	Motorola	
			12 *	1 *	0.8 *	20K	70	0	Automotive Temperature Range (−40°C to 85°C)	SA1458	Signetics	
	1000	300	6 *	—	9 *	10K	65	0	General Purpose, OC Output	TEC1761C	Thomson-CSF	
	2000	1000	—	—	1 *	6.5K	70	2	Low Noise	μA739	Fairchild	
7.0	100	10	—	0.4	1	100K	77	—	Ultra-Low Power	HA-5142	Harris	
	200	50	—	—	—	25K	65	0	Single Supply	TL321C	TI	
	250	50	7 *	—	—	100K *	50	0	Single Supply	TDF2904	Thomson-CSF	
				1 *	—	25K	65	0	Half LM224	μPC1251	NEC	
										μPC358	NEC	
										TDB0158	Thomson-CSF	
					0.3 *	25K	65	0	Automotive Temperature Range (−40°C to 85°C)	SA532	Signetics	
7.5	7	1	30	1 *	0.3 *	25K	80	1	Dual 308	LH2308	National	
										PM-2308	PMI	
	250	50	30	1 *	0.5 *	25K	70	1	Dual High Performance	LH2301A	Intersil	
										LH2301A	National	
	1500	500	1.5 *	1 *	0.25 *	15K	65	3	Matched Dual MC1709C	MC1437	Motorola	
					0.3 *	15K	65	3	Matched Dual 709	RC1437	Raytheon	
8.0	500	75	10 *	1 *	0.6 *	20K	70	0	Low Power	TL322M	TI	
9.0	0.40	0.20	10 *	1 *	0.6 *	200K	70	0	JFET Input	TL092M	† TI	
10.0	0.10	0.03	10	3	10	100K *	100 *	1	JFET Input	MA336	AnalogSys	
	0.2	0.1	10 *	4 *	13 *	25K	70	0	Dual 0351	TDB0353	Thomson-CSF	
	0.20	0.05	10 *	3 *	13 *	25K	70	0	Low Noise Bipolar-FET	MCE72	MCE	
				4 *	13 *	25K	70	0	Low Noise Bipolar-FET	TL072C	Motorola	
										TL072C	TI	
						50K	80	0	Low Noise Bipolar-JFET	TL072BC	TI	
		0.10	10 *	3 *	13 *	50K	70	0	Bipolar JFET	μA772	Fairchild	
				4 *	13 *	25K	70	0	Dual 351, Wide Band	LF353	Motorola	
										LF353	National	
	500	75	10 *	1 *	0.6 *	20K	70	0	Low Power	TL322C	TI	
	700	300	15 *	1.1 *	0.5 *	20K	60	0	General Purpose	MC1458C	Motorola	
	1500	600	—	—	—	10K	70	0	Audio Preamp	μA749D	Fairchild	
15.0	0.050	0.030	8 *	4 *	10 *	50K *	70	0	Dual 3160	**CA3260E**	**RCA**	**(3595)**
										CA3260T	† **RCA**	**(3595)**
			10 *	5 *	13 *	50K	70	0	MOS/FET Input, Bipolar/MOS Output	**CA082**	**RCA**	**(3596)**
										CA083	**RCA**	**(3596)**
						200K	76 *	0	MOS/FET Input, Bipolar/MOS Output	**CA082C**	**RCA**	**(3596)**
										CA083C	**RCA**	**(3596)**
			25 *	1 *	1.6	80K *	70	0	Low Power, Dual 1458	**ICL7621DC**	**Intersil**	**(3481)**
									Low Power, Dual 747	**ICL7622DC**	**Intersil**	**(3481)**
	0.20	0.10	10 *	3 *	13 *	50K	70	0	Bipolar JFET	μA772L	Fairchild	
	0.4	0.2	10 *	1 *	3.5 *	3K	70	0	Low Power Bipolar-JFET	TL062C	TI	
				3 *	11 *	25K	70	0	Bipolar-JFET	μPC4082	NEC	
					13 *	25K	70	0	Bipolar-JFET	**XR082C**	**Exar**	**(3376)**
										XR083C	**Exar**	**(3376)**
										MCE82	MCE	
										MCE83	MCE	
										TL082	Motorola	
										TL082C	TI	
										TL083C	TI	
	50	25	12 *	—	18 *	3K	65	0	Darlington Input	TBB2331	Siemens	
	200	100	30	—	2	10K	40	0	Power Op Amp, Comp. for G>30	MA208	AnalogSys	
20.0	0.02	0.0005 *	75	1 *	6 *	50K	70	0	FET Input Dual	ICL8043M	† Intersil	
50.0	0.05	0.0005 *	75	1 *	6 *	20K	70	0	FET Input Dual	ICL8043C	Intersil	
Triple Units												
5.0	0.050	0.030	10 *	1	1.6	80K *	70	0	Low Power	**ICL7631BC**	**Intersil**	**(3481)**
										ICL7631BM	† **Intersil**	**(3481)**
												(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers–Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Bandwidth MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source
Triple Units											**(Cont'd)**
5.0	0.050	0.030	10 *	1	1.6	80K *	70				(Cont'd)
								1	Low Power	**ICL7632BC**	**Intersil (3481)**
										ICL7632BM	**† Intersil (3481)**
	70	14	—	0.02 *	0.1 *	—	70	0	Micropower, Transconductance Amplifier	CA3060	† RCA
10.0	0.050	0.030	20 *	1	1.6	80K	70	0	Low Power	**ICL7631CC**	**Intersil (3481)**
										ICL7631CM	**† Intersil (3481)**
								1	Low Power	**ICL7632CC**	**Intersil (3481)**
										ICL7632CM	**† Intersil (3481)**
	2000	200 *	—	5	0.46	4K *	90 *	2	Supply + -6 V	TCA220	Signetics
20.0	0.050	0.030	30 *	1	1.6	80K	70	0	Low Power	**ICL7631EC**	**Intersil (3481)**
								1	Low Power	**ICL7632EC**	**Intersil (3481)**
Quad Units											
										HA4741-8	Raytheon
0.5	0.075	0.025	10 *	4 *	13 *	50K	80	0	Precision BIFET	MC35004A	† Motorola
	300	20	10	1.5	0.7	100K	100	0	Symmetrical, Matched	**MP5509A**	**† MicroPwr (3529)**
										MP5509E	**MicroPwr (3529)**
										MP5511A	**† MicroPwr (3529)**
										MP5511E	**MicroPwr (3529)**
										MPOP-11	† MicroPwr
										OP-09A	**† PMI (3566)**
										OP-09E	**PMI (3566)**
										OP-11A	**† PMI (3566)**
										OP-11E	**PMI (3566)**
2.0	0.2	0.1	8.3 *	0.24	15 *	50K	80	—	JFET Input	**HA-5084B-5**	**Harris (3438)**
			10 *	4 *	13 *	25K	80	0	Bipolar-JFET	LF347A	Harris
		2	10 *	4 *	13 *	50K	80	0	High Speed, JFET Input	TDB0347A	Thomson-CSF
	50	10	20	1 *	—	50K	70	0	Low Power	LM124A	† National
	500	50	10 *	3 *	8	50K	80	0	High Performance Bipolar	MC33074A	Motorola
										MC34074A	**Motorola (3530)**
										MC35074A	† Motorola
2.5	50	5	10	750 *	0.25 *	400K *	100K	0	Quad Micropower OP-21	**OP-421B**	**† PMI (3566)**
										OP-421F	**PMI (3566)**
	200	75	2 *	0.26	12	100K	86	0	Wideband, High Performance	**HA-4620-2**	**† Harris (3428)**
										HA-4620-5	**Harris (3428)**
				8 *	1	100K	86	0	High Performance	**HA-4600-2**	**† Harris (3426)**
										HA-4600-5	**Harris (3426)**
										HS4602RH	**† Harris (4721)**
					4 *	100K	86	0	Wideband	HA-4602-2	† Harris
			3 *	8 *	1	100K	86	0	Low Noise, High Performance	**HA-5104-2**	**† Harris (3459)**
										HA-5104-5	**Harris (3459)**
				60 *	12	100K	86	1	Wideband	**HA-5114-2**	**† Harris (3459)**
										HA-5114-5	**Harris (3459)**
	500	50	15	1.5	0.7	100K	100	0	Symmetrical, Matched	**OP-09B**	**† PMI (3566)**
										OP-09F	**PMI (3566)**
										OP-11B	**† PMI (3566)**
										OP-11F	**PMI (3566)**
3.0	0.03	0.02	10 *	5 *	13 *	50K	80	0	MOS/FET Input, Bipolar/MOS Output	**CA084B**	**RCA (3596)**
	0.2	0.1	10 *	0.63	2	20K	80	—	Low Power, JFET Input	**HA-5064B-5**	**Harris (3434)**
				1 *	3.5 *	4K	80	0	Low Power Bipolar-JFET	TL064BC	TI
				3 *	3	50K	80	0	JFET	TL084BC	TI
	0.20	0.05	10 *	4 *	13 *	25K	70	0	Low Noise Bipolar-JFET	TL074BC	TI
	20	10	—	1 *	0.8 *	30K	100 *	0	Programmable	**HA-2740-2**	**† Harris (3422)**
	80	15	20	1 *	—	50K	70	0	Low Power	LM224A	National
	100	30	30	—	—	100K	65	0	High Gain, Single Supply	TDB0124A	Thomson-CSF
				1 *	—	25K	65	0	Low Power	LM324A	National
										LM324A	TI
	200	30	5 *	3	1.2	25K	80	0	Noise 2µV Max	RM4156	† Raytheon
					1.6 *	50K	80	0	Quad 741	**XR4741M**	**† Exar (3378)**
				3.5 *	1.6 *	50K	80	0	Quad 741	**HA-4741-2**	**† Harris (3430)**
										HA4741-2	† Raytheon
											(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR

Master Selection Guide

LINEAR–Operational Amplifiers–Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift μV/°C	Band-width MHz	Slew Rate V/μs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	
Quad Units											**(Cont'd)**	
3.0	200	30	5 *								(Cont'd)	
				19 *	8 *	25K	80	0	Uncompensated 4156	RC4157	Raytheon	
										RM4157	† Raytheon	
	325	125	2 *	70 *	12	100K	86	0	Wideband, Comp. for g>10	HA-4622-2	† Harris	
3.5	300	100	2 *	8 *	4 *	75K	80	0	Wideband	HA-4605-5	Harris	
4.0	125	12	15	750 *	0.25 *	200K	96 *	0	Quad, Micropower OP-21	**OP-421C**	**† PMI**	**(3566)**
										OP-421G	**PMI**	**(3566)**
	400	50	5 *	1 *	1.2 *	50K	70	0	LM124 with Improved Output	RM3503A	† Raytheon	
		120	2 *	70 *	11	75K	80	0	Wideband, Comp. for g>10	HA-4625-5	Harris	
4.5	500	75	10 *	3 *	10	25K	70	0	High Performance Bipolar	MC33074	Motorola	
										MC34074	**† Motorola**	**(3530)**
										MC35074	† Motorola	
5.0	0.050	0.030	15 *	1	1.6	80K	70	0	Low Power	**ICL7641BC**	**Intersil**	**(3481)**
										ICL7641BM	**† Intersil**	**(3481)**
										ICL7642BC	**Intersil**	**(3481)**
										ICL7642BM	**† Intersil**	**(3481)**
		0.050	10	1	1	50K	80	0	Low Power BIFET	LF444A	National	
	0.10	0.05	10 *	4 *	13 *	50K	80	0	Precision BIFET	MC35004B	† Motorola	
		0.10	10 *	3 *	13 *	50K	80	0	Bipolar JFET	μA774B	Fairchild	
										μA774BM	† Fairchild	
	0.2	0.1	10 *	4 *	13 *	25K	80	0	Bipolar-JFET	LF347B	Harris	
		4	10 *	4 *	13 *	50K	80	0	High Speed, JFET Input	TDB0347B	Thomson-CSF	
	0.20	0.10	8.3 *	0.24	15 *	50K	80	—	JFET Input	**HA-5084-2**	**† Harris**	**(3438)**
										HA-5084A-5	**Harris**	**(3438)**
			10 *	4 *	13 *	50K	80	0	Precision BIFET	MC34004B	Motorola	
									Wideband, Quad 351B	LF347B	Motorola	
										LF347B	National	
	30	10	—	1 *	0.8 *	25K	74	0	Programmable	**HA-2740-5**	**Harris**	**(3422)**
	100	20	—	0.8	0.4 *	1M	70	0	High Gain, Programmable	TDC0146	† Thomson-CSF	
		25	—	1 *	0.5 *	50K	70	0	High Gain, Programmable	TDC0148	† Thomson-CSF	
										TDC0149	† Thomson-CSF	
									Quad 741 with Standard npn Input Stage	LM148	† AMD	
										μA148	† Fairchild	
										LM148	† Motorola	
										LM148	† Raytheon	
										LM148	† TI	
				4 *	2.0 *	50K	70	0	Wideband Quad 741 for Gains >5	LM149	† National	
										LM149	† Raytheon	
		40	—	0.8 *	0.5 *	4K	60	0	Low Power	TL044M	† TI	
	150	30	7 *	—	—	100K	70	0	High Gain, Single Supply	TDC0124	† Thomson-CSF	
	250	80	—	0.8 *	0.5 *	1K	60	0	Low Power	TL044C	TI	
	300	50	5 *	0.02	1.3	50K	80	0	General Purpose	**HA-4156-5**	**Harris**	**(3424)**
				3	1.2	25K	80	0	Noise 2 μV Max	RC4156	Raytheon	
				3 *	1.6 *	25K	80	0	Quad 741	μPC4741	NEC	
				3.5 *	1.6 *	25K	80	0	Quad 741	**XR4741C**	**Exar**	**(3378)**
										HA-4741-5	**Harris**	**(3430)**
										HA4741-5	Raytheon	
	500	50	—	2 *	1.5 *	5K	70	0	Programmable Quad 741	MC4202	Motorola	
					1.6 *	20K	70	0	Low Noise, Low Power	**XR4212M**	**† Exar**	**(3378)**
			10	1	0.6	200K	90	0	Low Power	MC3503	Signetics	
			10 *	1 *	0.6 *	—	70	0	Low Power, Single Supply	TDC3403	† Thomson-CSF	
		200	—	3 *	1.5 *	50K	70	0	Quad 741, High Gain	**XR4136M**	**† Exar**	**(3378)**
										μA4136M	† Fairchild	
										MP4136	**MicroPwr**	**(3529)**
										RM4136	† Raytheon	
				3.5	1.5	96	110	0	Programmable	TAB1042	Plessey	
										TAB1043	Plessey	
			4 *	1.5	0.7	50K	70	0	Quad Matched 741	**OP-09C**	**PMI**	**(3566)**
			15 *	1	0.5 *	50K	70	0	Quad 741	MC4741	† Motorola	

† Military Temperature Range (−55° to 125°C)   * Typical Value

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LINEAR–Operational Amplifiers–Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift μV/°C	Band-width MHz	Slew Rate V/μs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source
Quad Units											**(Cont'd)**
6.0	0.04	0.02	10 *	5 *	13 *	50K	80	0	MOS/FET Input, Bipolar/MOS Output	**CA084A**	**RCA (3596)**
	0.2	0.05	—	8	20	50K	80	0	FET, Wideband	MC3571	† Motorola
			10 *	3 *	13 *	50K	80	0	Low Noise Bipolar-JFET	MCE74	MCE
										TL074M	† TI
		0.1	10 *	0.63	2	20K	80	—	Low Power, JFET Input	**HA-5064-2**	**† Harris (3434)**
										HA-5064A-5	**Harris (3434)**
				1 *	3.5 *	4K	80	0	Low Power Bipolar-JFET	TL064AC	TI
				3 *	13 *	50K	80	0	Bipolar JFET	**XR084**	**Exar (3377)**
										XR084M	**† Exar (3377)**
										MCE84	MCE
										TL084A	Motorola
										TL084AC	TI
										TL084M	† TI
									Indiv. Program	**XR096**	**Exar (3377)**
										XR096M	**† Exar (3377)**
									Programmable, Bipolar - FJET	**XR094**	**Exar (3377)**
										XR094M	**† Exar (3377)**
										XR095	**Exar (3377)**
										XR095M	**† Exar (3377)**
	0.20	0.05	10 *	4 *	13 *	25K	70	0	Low Noise Bipolar-JFET	TL074AC	TI
						50K	80	0	Low Noise Bipolar JFET	TL074BC	Motorola
									Low Noise Bipolar-JFET	TL074AC	Motorola
	75	10	—	0.4	1.5	100K	80	—	Ultra-Low Power	HA-5144A	Harris
	200	0.1	10 *	3 *	13 *	50K	80	0	High Speed, JFET Input	TDC0084	Thomson-CSF
		50	—	1 *	0.5 *	25K	70	0	High Gain, Programmable	TDB0148	Thomson-CSF
										TDB0149	Thomson-CSF
									Quad 741 with Standard npn Input Stage	LM248	AMD
										LM348	AMD
										μA248	Fairchild
										μA348	Fairchild
										LM248	National
										LM348	National
										LM248	Raytheon
										LM348	Raytheon
										LM248	TI
										LM348	TI
				4 *	2 *	25K	70	0	Wideband Quad for Gains >5	LM249	National
										LM349	National
										LM249	Raytheon
										LM349	Raytheon
	250	20	25	750 *	0.25 *	200K *	90 *	0	Quad OP-21	**OP-421H**	**PMI (3566)**
		100	—	0.5	0.4 *	1M	70	0	High Gain, Programmable	TDB0146	Thomson-CSF
	500	50	—	1 *	1.2 *	25K	70	0	LM324 with Improved Output	RC3403A	† Raytheon
				2	1.6	5K	70	0	Quad 741	**XR4212C**	**Exar (3378)**
		100	—	1	0.4 *	20K	70	0	346 w/Sep Bias Resister for Each Pair	**XR346-2**	**Exar (3377)**
		200	—	1 *	0.5 *	20K	70	0	Quad 741	MC4741C	Motorola
				3 *	1 *	20K	60-70	0	Quad 741	**XR4136C**	**Exar (3378)**
										μA4136C	Fairchild
										MP4136C	**MicroPwr (3529)**
										RC4136	Raytheon
										SG4136	† SiliconG
										SG4136C	SiliconG
										RC4136	† TI
					2.4 *	20K	70	0	High Performance	TL136C	TI
7	250	50	7 *	—	—	100K *	50	0	Single Supply	TDF2902	Thomson-CSF
7.0	100	10	—	0.4	1	100K	77	—	Ultra-Low Power	HA-5144	Harris
	150	30	—	—	—	20K	60	0	Single Supply	TA75902	Toshiba
	250	50	—	—	—	25K	65	0	324 Type	TBB0324	Siemens
			7 *	—	—	100K	65	0	High Gain, Single Supply	TDB0124	Thomson-CSF
				1 *	0.3 *	25K	65	0	Automotive Temperature Range (−40°C to 85°C)	SA534	Signetics
	500	50	—	—	—	100K	50	0	Single Supply	μPC2902	NEC
						100K *	85 *	0	324 Type	μPC451	NEC

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers–Characteristics (Cont'd)

Quad Units (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift μV/°C	Band-width MHz	Slew Rate V/μs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source
8.0	500	75	10	1	0.6	200K	90	0	Low Power	MC3303	Signetics
			10 *	1 *	0.6 *	20K	70	0	Single Supply: I/O Operates to Ground	MC3303	TI
										TDF3403	Thomson-CSF
9.0	0.2	0.1	10 *	1 *	3.5 *	4K	80	0	Low Power Bipolar-JFET	TL064M	† TI
				4 *	13 *	25K	80	0	JFET Input	TL084M	† Motorola
	0.20	0.05	10 *	4 *	10	35K	70	0	Low Noise Bipolar JFET	TL074M	† Motorola
	0.40	0.20	10 *	1 *	0.6 *	200K	70	0	JFET Input	TL094M	† TI
10.0	0.050	0.030	20 *	1 *	1.6 *	80K	70	0	Low Power	**ICL7641CC**	**Intersil** (3481)
										ICL7641CM	† **Intersil** (3481)
										ICL7642CC	**Intersil** (3481)
										ICL7642CM	† **Intersil** (3481)
	0.10	0.05	10	1	1	25K	70	0	Low Power BIFET	LF444	National
	0.2	0.1	10 *	4 *	13 *	25K	70	0	Bipolar-JFET	LF147	Harris
										LF247	Harris
										MC34004	Motorola
										MC35004	† Motorola
		4	10 *	4 *	13 *	25K	70	0	High Speed, JFET Input	TDB0347	Thomson-CSF
	0.20	0.05	10 *	4 *	13 *	25K	70	0	Low Noise Bipolar-JFET	TL074C	Motorola
										TL074C	TI
										TL075C	TI
		0.1	10 *	4 *	13 *	25K	70	0	Bipolar-JFET, Quad 351	LF347	Motorola
										LF347	National
		0.10	10 *	3 *	13 *	50K	70	0	Bipolar JFET	μA774	Fairchild
	0.20 *	0.05 *	10 *	1 *	0.6 *	20K	70	0	JFET Input	TL094M	† TI
	500	50	10	1	0.6	200K	90	0	Low Power	MC3403	Signetics
			10 *	1 *	0.6 *	—	70	0	Low Power, Single Supply	TDB3403	Thomson-CSF
						20K	70	0	Single Supply: I/O Operates to Ground	μA3403	Fairchild
										MC3403	TI
15.0	0.05	0.03	10 *	5 *	13 *	25K	70	0	MOS/FET Input, Bipolar/MOS Output	**CA084**	**RCA** (3596)
	0.20	0.10	10 *	3 *	13 *	50K	70	0	Bipolar-JFET	μA774L	Fairchild
	0.40	0.2	8.3 *	0.24	15 *	25K	70	—	JFET Input	**HA-5084-5**	**Harris** (3438)
			10 *	1 *	3.5 *	3K	70	0	Low Power Bipolar-JFET	TL064C	TI
				3 *	11 *	25K	70	0	Bipolar-FET	μPC4084	NEC
					13 *	25K	70	0	Bipolar-FET	**XR084C**	**Exar** (3377)
										TL084	Motorola
										TL084C	TI
										TL085C	TI
									Indiv. Program.	**XR096C**	**Exar** (3377)
									Programmable Bipolar-JFET	**XR094C**	**Exar** (3377)
										XR095C	**Exar** (3377)
			20 *	0.63	2	10K	70	—	Low Power, JFET Input	**HA-5064-5**	**Harris** (3434)
	50	25	12 *	—	—	3K	65	0	Darlington Input	TBB4331	Siemens
										TBE4335	Siemens
	400	0.2	10 *	3 *	13 *	25K	70	0	High Speed, JFET Input	TDB0084	Thomson-CSF
20.0	0.050	0.030	30 *	1	1.6	80K	70	0	Low Power	**ICL7641EC**	**Intersil** (3481)
										ICL7642EC	**Intersil** (3481)
30.0	0.050	0.100	15 *	1 *	0.8 *	1K *	70 *	0	Low Power	MC14573	Motorola

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Phase Locked Loops/Synthesizers

Phase Locked Loops/ Synthesizers

CB device sets and support circuits are also found in Consumer Circuits

Function	Device	Source	
Count Extender, ÷4, ÷10/11 becomes ÷40/41	SP8790A	† Plessey	
	SP8790B	Plessey	
Count Extender, ÷8 (extends division ratio of a two modulus prescaler while retaining the difference, ie R10/11 becomes ÷80/81)	SP8794A	† Plessey	
	SP8794B	Plessey	
Counter Logic Control	SP8790	Plessey	
Counter Logic Control (use with MC12012 for high frequency programming)	MC12014	Motorola	
Crystal Oscillator (2 to 20 MHz)	MC12061	Motorola	
	MC12561	† Motorola	
Crystal Oscillator (250 kHz to 60 MHz)	CK1100A	Solarise	
	CK1114A	Solarise	
	CK1144A	Solarise	
	CK1145A	Solarise	
FSK Modulator/Demodulator	**XR210**	**Exar**	**(3365)**
	XR210M	**† Exar**	**(3365)**
	XR2211	† Exar	
	XR2211	Exar	
	XR2211C	Exar	
	XR2211M	† Exar	
	XR2212M	**† Exar**	**(3366)**
	XR2211C	Raytheon	
	XR2211M	† Raytheon	
Phase Comparator and Programmable Counter	MC14568BA	† Motorola	
	MC14568BC	Motorola	
Phase Locked Loop	**XR215**	**Exar**	**(3365)**
	XR215M	**† Exar**	**(3365)**
	SL652	Plessey	
	SDA2002	Siemens	
	SDA2112-2	Siemens	
	NE564	**Signetics**	**(3649)**
	SE564	**† Signetics**	**(3649)**
	SN54LS297	**† TI**	**(1015)**
	SN74LS297	**TI**	**(1015)**
Phase Locked Loop (CMOS)	F4046BC	Fairchild	
	F4046BM	† Fairchild	
	MC14046BA	† Motorola	
	MC14046BC	Motorola	
	CD4046BC	National	
	CD4046BM	† National	
	CD4046A	**† RCA**	**(840)**
	CD4046AE	**RCA**	**(840)**
	CD4046B	**† RCA**	**(840)**
	CD4046BE	**RCA**	**(840)**
	CD54HCT297	† RCA	
	CD74HCT297	**RCA**	**(842)**
	74HCT297	**Signetics**	**(907)**
	74HCT4046	**Signetics**	**(908)**
	883/4046B	† SSS	
	883/4446B	† SSS	
	SCL4046B	SSS	
	SCL4446B	SSS	
Phase Locked Loop for Motor Control—See Motor Speed Regulators in Linear-Consumer Circuits, Miscellaneous.			
Phase Locked Loop System (multiplier, VCO and Op Amp)	XRS200	Exar	
Phase-Frequency Detector	MC12040	Motorola	
	MC12540	† Motorola	
	MC4044	Motorola	
	MC4344	† Motorola	
PLL Peripheral (VCO, mixer, amp for CB)	AN103	Panasonic	
	TA7310	Toshiba	
Prescaler	SDA4041	Siemens	
Prescaler, Divide by 20	MC3396	Motorola	
Prescaler, Divide by 64	SDA2001	Siemens	
Prescaler, for AM/FM	TD6102	Toshiba	
Prescaler, for FM Radio	DS8626	National	
	DS8629	National	
	SP8629	Plessey	
Prescaler for PLL Tuner, Divide by 8	LB3500	Sanyo	
Prescaler for VHF/UHF, Divide by 64	MC12071	Motorola	
	DS8621	National	
	CA3179	RCA	
Prescaler for VHF/UHF, Divide by 4	**CA3199**	**RCA**	**(3603)**
Prescaler for VHF/UHF, Dual Modulus	DS8622	National	
Prescaler, Low Power (÷64), 1.1 GHz	MC12073	Motorola	
Prescaler, Low Power (÷64), 225 MHz	MC12023	Motorola	
Prescaler, Low Power (÷256), 1.1 GHz	MC12074	Motorola	
	MC12075	Motorola	
Prescaler, UHF (÷2), 740 MHz	MC12090	Motorola	
Prescaler, 0.05 to 1.3 GHz, Divide by 256	SP4742	Plessey	
Prescaler, 0.05 to 1.3 GHz, Divide by 4056 and 8192	SP4780	Plessey	
Prescaler, 0.08 to 1 GHz, Divide by 256	SP4642	Plessey	
	SP4652	Plessey	
	SP4653	Plessey	
Prescaler, 0.08 to 1 GHz, Divide by 64	SP4632	Plessey	
Prescaler, 1 GHz, Divide by 256	**CA3211**	**RCA**	**(3603)**
	SAB1256	Signetics	
Prescaler, 1 GHz, Divide by 64	SAB1164	Signetics	
Prescalers—see also Digital-Special, Dividers, Digital-ECL			
Programmer, for CB Synthesizer	MP7156	MicroPwr	
	MM57190	National	
Programmers and Controllers for Citizens Band—See Linear-Consumer Circuits			
Synthesizer, Mobile Radio (2 device set)	NJ8811	Plessey	
	NJ8812	Plessey	
	SP8901	Plessey	
	SP8906	Plessey	
Synthesizer, PLL	HCTR0347	Hughes	
	MC145104	Motorola	
	MC145106	Motorola	
	MC145107	Motorola	
	MC145109	Motorola	
	MC145112	Motorola	
	MC145143	Motorola	
	MC145144	Motorola	
	MC145145	Motorola	
	MC145146	Motorola	
	MC145151	Motorola	
	MC145152	Motorola	
	MC145155	Motorola	
	MC145156	Motorola	
	MC145157	Motorola	
	MC145158	Motorola	
	MC145159	Motorola	
	MC6195	Motorola	
	MC6196	Motorola	
	DS8906	National	
	DS8907	National	
	DS8908	National	
	MM55108	National	
	MM55110	National	
	MM55121	National	
	MM55123	National	
	MM55124	National	
	MM55126	National	
	MN6040	Panasonic	
	MN6040A	Panasonic	
	MN6040Z	Panasonic	
	MN6142	Panasonic	
	LC7210	Sanyo	
	LC7220	Sanyo	
	LC7225	Sanyo	
	HEF4750	**Signetics**	**(865,899)**
	SAA1057	Signetics	
	TC9106B	Toshiba	
	TC9109B	Toshiba	
	TC9111B	Toshiba	
Synthesizer (programmable divider, to 1021 channels, adder, phase comparator)	HCTR0320	Hughes	
Synthesizer (programmable dividers, phase comparator)	S187A	Siemens	
Synthesizer, 200 Channel, for AM/FM	8X08	Signetics	
Tone Decoder	XR2211C	Exar	
	XR2211M	† Exar	
	XR2213C	**Exar**	**(3366)**
	XR2213M	**† Exar**	**(3366)**
	XR567AC	**Exar**	**(3367)**
	XR567AM	**† Exar**	**(3367)**
	XRL567C	**Exar**	**(3367)**
	XRL567M	**† Exar**	**(3367)**
	LM567	† National	
	LM567C	National	
	XR2211C	Raytheon	
	XR2211M	† Raytheon	
	NE567	Signetics	
	SE567	† Signetics	
VCO	MC1648	Motorola	
	MC1648M	† Motorola	
	MC1658	Motorola	
	SP1658	Plessey	
	SN54LS324	† TI	
	SN54LS624	**† TI**	**(1067)**
	SN54LS628	**† TI**	**(1068)**
	SN74LS624	**TI**	**(1067)**
	SN74LS628	**TI**	**(1068)**

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR

Master Selection Guide

LINEAR–Phase Locked Loops/Synthesizers (Cont'd)

Phase Locked Loops/ Synthesizers (Cont'd)

Function	Device	Source	
VCO and Phase Comparator			
	LM565	Motorola	
	NE565	Motorola	
	LM565	National	
	LM565C	† National	
	NE565	Signetics	
	SE565	† Signetics	
	TA7133	Toshiba	
VCO Function Generator, (Includes square and triangular waveforms - but not sine.)			
	XR2207	Exar	
	XR2207C	Exar	
	XR2209C	**Exar**	**(3374)**
	XR2209M	**† Exar**	**(3374)**
	LM566	National	
	LM566C	† National	
	XR2207C	Raytheon	
	XR2207M	† Raytheon	
	NE566	Signetics	
	SE566	† Signetics	
VCO Phase Comparator, Multiplier			
	SL651	Plessey	
VCO Phase Comparator, Multiplier, with Auxiliary Amplifier			
	SL650	† Plessey	
VCO Waveform Generator (includes sinewave output among its functions)			
	XR205	Exar	
	XR2206	**† Exar**	**(3373)**
	XR2206	Exar	
	XR2206C	**Exar**	**(3373)**
	XR2206M	**† Exar**	**(3373)**
	XR8038	**Exar**	**(3374)**
	XR8038A	**Exar**	**(3374)**
	XR8038M	**† Exar**	**(3374)**
	ICL8038C	**Intersil**	**(3518)**
	ICL8038M	**† Intersil**	**(3518)**
VCO, Dual	MC4024	Motorola	
	MC4324	† Motorola	
	SN54LS325	TI	
	SN54LS326	† TI	
	SN54LS327	† TI	
	SN54LS625	**† TI**	**(1067)**
	SN54LS626	**† TI**	**(1067)**
	SN54LS627	**† TI**	**(1068)**
	SN54LS629	**† TI**	**(1068)**
	SN54S124	**† TI**	**(962)**
	SN74LS124	TI	
	SN74LS325	TI	
	SN74LS326	TI	
	SN74LS327	TI	
	SN74LS328	TI	
	SN74LS625	**TI**	**(1067)**
	SN74LS626	**TI**	**(1067)**
	SN74LS627	**TI**	**(1068)**
	SN74LS629	**TI**	**(1068)**
	SN74S124	**TI**	**(962)**
Dual Tone Decoder			
	XR2567C	**Exar**	**(3367)**
	XR2567M	**† Exar**	**(3367)**
Two Modulus Prescaler (÷3/4)			
	SP8720	Plessey	
Two Modulus Prescaler (÷4/8)			
	11C91C	Fairchild	
	11C91M	† Fairchild	
	MC12009	Motorola	
	MC12509	† Motorola	
	SP8740	Plessey	
	TD6102	Toshiba	
Two Modulus Prescaler (÷5/6)			
	MC12009	Motorola	
	MC12509	† Motorola	
Two Modulus Prescaler (÷6/7)			
	SP8741	Plessey	
Two Modulus Prescaler (÷8/9)			
	MC12011	Motorola	
	MC12511	† Motorola	
	SP8743	Plessey	
Two Modulus Prescaler (÷10/11)			
	11C90C	Fairchild	
	11C90M	† Fairchild	
	MC12013	Motorola	
	MC12513	† Motorola	
	SP8643	Plessey	
	SP8647	Plessey	
	SP8685	Plessey	
	SP8690	Plessey	
Two Modulus Prescaler (÷15/16)			
	MC3393	Motorola	
Two Modulus Prescaler (÷20/21), 225 MHz			
	MC12019	Motorola	
Two Modulus Prescaler (÷32/33), 225 MHz			
	MC12015	Motorola	
Two Modulus Prescaler (÷40/41)			
	SP8793	Plessey	
	SP8793A	Plessey	
Two Modulus Prescaler (÷40/41), 225 MHz			
	MC12016	Motorola	
Two Modulus Prescaler (÷64/256)			
	MC12071	Motorola	
	DS8621	National	
	CA3163	RCA	
	CA3179	**RCA**	**(3603)**
Two Modulus Prescaler (÷64/65), 225 MHz			
	MC12017	Motorola	
Two Modulus Prescaler (÷80/81)			
	SP8792	Plessey	
	SP8792A	Plessey	
Two Modulus Prescaler (÷128/129), 225 MHz			
	MC12018	Motorola	
Two Modulus Prescaler (÷248/256)			
	SAB1077	Signetics	
Two Modulus Prescaler, Low Power (÷128/129), 1 GHz			
	MC12022	Motorola	
Four Modulus Prescaler (÷256/512)			
	SP8901	Plessey	
	SP8906	Plessey	

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Telecommunication Circuits

Telecommunication Circuits

Function	Device	Source	
Amplifier, Microphone	SL792	Plessey	
	SL793	Plessey	
Amplifier, Telephone Handset	TEA1045	ITT	
Bandpass Filters	R5602A-1	Reticon	
	R5602A-3	Reticon	
	R5602A-7	Reticon	
	R5602A-8	Reticon	
Bandpass Filters (touchtone)	S3525A	AMI	
	S3525B	AMI	
	S3526A	**AMI**	**(3346)**
	S3526B	**AMI**	**(3346)**
	AMS3040A	Aptek	
	AMS3041A	Aptek	
	AMS3044	Aptek	
	AMS3045	Aptek	
	CH1295	Cermetek	
	CH1296	Cermetek	
	MT8865	Mitel	
	AF121	National	
	AF122	National	
Bandpass Filters Tunable, See also Filter, Modem Filters	R5626	Reticon	
Bandpass Filters Tunable, See also Filters, Modem Filters	R5604	Reticon	
	R5605	Reticon	
	R5606	Reticon	
	R5609	Reticon	
	R5611	Reticon	
	R5612	Reticon	
	R5613	Reticon	
	R5614	Reticon	
	R5615	Reticon	
	R5616	Reticon	
	R5620	Reticon	
	R5621	Reticon	
	R5622	Reticon	
Bandsplit Filter, DTMF	S3525A	AMI	
	S3525B	AMI	
	G8865X	GTEMicro	
	MV8865	Plessey	
	TT6177	Teltone	
Call Progress Tone Detector	M980	Teltone	
	M981	Teltone	
	M982	Teltone	
Click Suppressor	ZSY0	ITT	
Codec, A Law	5156	Fairchild	
	G8911	GTEMicro	
	HC5156A	Harris	
	HC5511	Harris	
	2911A	Intel	
	MK5156	Mostek	
	TP3021	National	
	TP5156	National	
	TP5156A	National	
	M090	SGS	
	M5156	SGS	
	S0291	Siemens	
	TCM2911A	TI	
	EFB7356	Thomson-CSF	
Codec/Filter, A Law	**S3506**	**AMI**	**(3348)**
	MT3506	Mitel	
	MT8961	Mitel	
	MT8963	Mitel	
	MT8965	Mitel	
	TCM2917	TI	
	TCM4917	TI	
Codec/Filter, A Law, Asynchronous	ZNPCM4	Ferranti	
Codec/Filter, A Law or µ255 Law metal option	**CD22301**	**RCA**	**(840)**
Codec/Filter, A Law PCM	S3503	AMI	
	S3504	AMI	
Codec/Filter, A Law, Synchronous	ZNPCM3	Ferranti	
Codec/Filter, Parallel Data Interface	TP3051	National	
	TP3056	National	
Codec/Filter, Pin Selectable µLaw or A Law	2913	Intel	
	2914	Intel	
	MC14403	**Motorola**	**(3536)**
	MC14405	**Motorola**	**(3536)**
	TCM2913	TI	
	TCM2914	TI	
	TCM2916	TI	
	TCM2917	TI	
	TCM4913	TI	
	TCM4914	TI	
	TCM4916	TI	
	TCM4917	TI	
Codec/Filter, Serial Interface	TP3052	National	
	TP3053	National	
	TP3054	National	
	TP3057	National	
Codec/Filter, µ255 Law	**S3507**	**AMI**	**(3348)**
	MT3507	Mitel	
	MT3507A	Mitel	
	MT8960	Mitel	
	MT8962	Mitel	
	MT8964	Mitel	
	MK5300	Mostek	
	TCM2916	TI	
	TCM4916	TI	
Codec/Filter, µ255 Law PCM	S3501	AMI	
	S3502	AMI	
Codec, µ255/A Law	ZNPCM1	Ferranti	
	AY3-9900	GI	
	MC14404	Motorola	
	MC14407	**Motorola**	**(3536)**
	TP5117A	National	
	S291	Siemens	
	SM61C	Siemens	
Codec, µ255 Law	5116	Fairchild	
	5151	Fairchild	
	G8910	GTEMicro	
	HC5116A	Harris	
	HC5510	Harris	
	2910	Intel	
	2910A	Intel	
	MK5116	Mostek	
	MK5151	Mostek	
	MC14406	Motorola	
	TP3020	National	
			(Continued)
Codec, µ255 Law (Cont'd)	TP5116	National	
	TP5116A	National	
	MSM6917	**OKI**	**(4118)**
	M5116	SGS	
	ST101	Signetics	
	TCM2910A	TI	
	TCM4110	TI	
	TCM4910	TI	
Companding A/D and D/A Converter	MM8100	National	
Companding Analog to Digital Converter	DF331A	Siliconix	
Companding Digital to Analog Converter	DF332A	Siliconix	
Compandor (signal expander/compressor)	XR2216	Exar	
	NE570	**Signetics**	**(3616)**
	NE571	**Signetics**	**(3616)**
	NE572	**Signetics**	**(3618)**
	SA571	**† Signetics**	**(3616)**
Crosspoint Switch (double 4x4 matrix)	RC4444	Raytheon	
	RM4444	Raytheon	
Crosspoint Switch (2x8 matrix)	M089	SGS	
	M099	SGS	
Crosspoint Switch (4x4 matrix with control memory)	**MC142100**	**Motorola**	**(3536)**
	MC145100	**† Motorola**	**(3536)**
	µPD22100	NEC	
	CD22100	**RCA**	**(840)**
	M22100	SGS	
	EFB7310	Thomson-CSF	
Crosspoint Switch (4x4x2 with control memory)	**CD22101**	**RCA**	**(840)**
	CD22102	**RCA**	**(840)**
Crosspoint Switch (8x4 switch matrix)	MT8804B	† Mitel	
CTCSS (continuous tone-controlled squelch system) Encoder/Decoder	MC1938	NEC	
	MC4137	NEC	
	MC4138	NEC	
Current Limiter (for electromechanical telephone bells)	ZN474E	Ferranti	
Delta Modulation System, Continuously Variable Slope	XR3417	Exar	
	XR3418	Exar	
	XR3517	Exar	
	XR3518	Exar	
	HC55536	**Harris**	**(3470)**
	HC55564	**Harris**	**(3469)**
	MC3417	Motorola	
	MC3418	Motorola	
	MC3517	† Motorola	
	MC3518	† Motorola	
Delta Sigma Modulator/Demodulator	ZNPCM2	Ferranti	
Dialer, Microcomputer (clock, duration, fee pulse counter, redial, storage)	SAA6002	ITT	
	MK5170	Mostek	
	PCD3340	Signetics	
Dialer, Microcomputer (clock, stopwatch, redial, 16/32 number)	TZ2003	TI	
Dialer, Loop Disconnect	DF820	ITT	
	DF821	ITT	
	DF822	ITT	
			(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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Master Selection Guide

LINEAR–Telecommunication Circuits (Cont'd)

Telecommunication Circuits (Cont'd)

Function	Device	Source
Dialer, Loop Disconnect (Cont'd)	DF823	ITT
	M760	SGS
	M760A	SGS
	PCD3324	Signetics
	PCD3325	Signetics
	EFB9158	Thomson-CSF
Dialer, Push Button Telephone Dialer Circuit (converts push button inputs to pulses)	AY5-9171	GI
	MC14409	**Motorola (3536)**
	MC34015	Motorola
	MM53143	National
	MM53144	National
	MM53190	National
	MM5393	National
	MM5394	National
	CRC8000	Rockwell
	CRC8001	Rockwell
	M761	SGS
	M761A	SGS
	PCD3320	Signetics
	PCD3321	Signetics
	PCD3322	Signetics
	PCD3323	Signetics
	TEA1021	Signetics
	TEA1043	Signetics
	TEA1044	Signetics
	DF320	Siliconix
	DF320A	Siliconix
	DF322	Siliconix
	DF328	Siliconix
	TCM1101	TI
	EFB9151	Thomson-CSF
	EFB91E51	Thomson-CSF
Dialer, Push Button Telephone Dialer Circuit (converts push button inputs to pulses)	**S2560A**	**AMI (3341)**
	AY5-9151	GI
	AY5-9153	GI
	AY5-9154	GI
	DF320	ITT
	MT4320	Mitel
	MT4322	Mitel
	MT4323	Mitel
	MT4325	Mitel
	MT4326	Mitel
	MT4327	Mitel
	MK50981	Mostek
	MK50982	Mostek
	MK50991	Mostek
	MK50992	Mostek
	MC14408	**Motorola (3536)**
Dialer, Repertory	**S25610**	**AMI (3342)**
	S25610E	**AMI (3342)**
	S2562	AMI
	S2563	AMI
	CET200	Fairchild
	MK5175	Mostek
	SFF19200	Thomson-CSF
Digital Filter with Utility Peripheral	S28215	AMI
Digital Line Interface Controllers	TP3110	National
	TP3120	National
Digital Line Interface Module	MH89700	Mitel
Digital Modulator, 1200/2400 bps	**MC6172**	**Motorola (3536)**
Digital Time/Space Crosspoint Switch	MT8981	Mitel
Digital Trunk-Interface Module (T1)	MH89750	Mitel
Echo Canceller Peripheral	S28216	AMI
Elastic Store (provides buffer store and justification function in a 2nd order PCM multiplexer)	TCM2401	TI
Electronic Phone Chip, Microprocessor Interface	**MC34010**	**Motorola (3060)**
Electronic Telephone Circuit (DTMF), Tone Ringer, Speech Network and DC Line Voltage Regulator	**MC34011**	**Motorola (3060)**
Encoder 8 of 8 Keyboard to Binary Encoder (4x4 key input to 4 line output)	**MC14419**	**Motorola (3536)**
Filter Array, mask programmable switched capacitor	R5625	† Reticon
Filter, Codec (A law/μlaw)	MB6001	Fujitsu
	MB6002	Fujitsu
	MC14400	**Motorola (3536)**
	MC14401	**Motorola (3536)**
	MC14402	**Motorola (3536)**
	MC14403	Motorola
	MC14405	Motorola
Filter, Low-Pass Programmable	**S3528**	**AMI (3347)**
Filter, PCM	AMS3064	Aptek
	AMS3065	Aptek
	AF132	National
	AF133	National
	AF134	National
	MC4264	NEC
	MSM6912	**OKI (4118)**
	SM153	Siemens
	TCM2912A	TI
Filter, PCM Transmit/Receive	G8912B	GTEMicro
	HC5512	**Harris (3468)**
	HC5512A	**Harris (3468,3468)**
	HC5512C	**Harris (3468)**
	2912A	Intel
	MK5912	Mostek
	MK8912	Mostek
	MC14413-1	**Motorola (3536)**
	MC14413-2	**Motorola (3536)**
	MC14414-1	**Motorola (3536)**
	MC14414-2	**Motorola (3536)**
	TP3040	National
	TP3040A	National
	CD22413	**RCA (840)**
	CD22414	**RCA (840)**
	M5912	SGS
	TCM2912B	TI
	EFB7912	Thomson-CSF
Filter, Speech (dual, tunable low-pass)	**MC145414**	**Motorola (3536)**
Filter, Tunable (lowpass/bandpass)	MC145431	Motorola
Filter, Tunable (notch, bandpass)	**MC145433**	**Motorola (3536)**
	MC145434	Motorola
Filter, Dual Low Pass Linear Phase	**MC145415**	**Motorola (3536)**
FSK Receiver, Wideband	MC3356	Motorola
Gyrator	AF120	National
HDB3/AMI Encoder/Decoder	TCM2202	TI
HDB3/AMI Encoder/Decoder (0 to 2.5 MHz, T1 Compatible)	TCM2202	TI
HDB3/AMI Equipment Line Interface (interfaces signal, clock to line)	TCM2203	TI
	TCM2204	TI
HDB3/AMI Line Interface	TCM2203	TI
	TCM2204	TI
HDB3 Transcoder	TCM2201	TI
IR Receiver	SM802	Siemens
IR Transmitter	SM801	Siemens
Limiter (limits voltage on two-wire speech)	U225	Telefunken
Microphone Amplifier (for telephone circuits)	ZN470AE	Ferranti
	ZN472E	Ferranti
	ZN475E	Ferranti
	ZN476E	Ferranti
	ZN477E	Ferranti
Modem Band-Pass Filter, 300 Baud	MC145440	Motorola
	MC145441	Motorola
Modem Circuit, V.21, V.23, Bell 103, 202	**AM7910**	**AMD (1433,3321)**
Modem Circuit, V23 or Bell 202	EFB7910	Thomson-CSF
Modem Circuits, CCITT FSK V.23 or Bell 202	TCM3101	TI
Modem Circuits, for CCITT FSK System	CH1225	Cermetek
	CH1253	Cermetek
	CH1258	Cermetek
	CH1259	Cermetek
	CH1263	Cermetek
	CH1268	Cermetek
	EFB7510	Thomson-CSF
Modem Circuits, for 103/113 and Other FSK Systems	CH1222	Cermetek
	CH1223	Cermetek
	CH1224	Cermetek
	CH1252	Cermetek
	CH1257	Cermetek
	CH1262	Cermetek
	CH1265	Cermetek
	CH1266	Cermetek
	CH1267	Cermetek
	CH1271	Cermetek
	CH1272	Cermetek
	CH1273	Cermetek
	CH1280	Cermetek
	AY7-1203	GI
	MC145445	**Motorola (3536)**
	MC145450	**Motorola (3536)**
	MM54HC942	† National
	MM74HC942	National
Modem Circuits, FSK CCITT V.21 or Bell 103	**TMS99532**	**TI (1712)**
	TMS99534	**TI (1712)**
Modem Circuits, PSK CCITT V.22, V.26 or Bell 212A, 201BC	**XR2123**	**Exar (3370)**
Modem Circuits, PSK Demodulator, Bell 212A	**XR2122**	**Exar (3370)**

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR

Master Selection Guide

LINEAR–Telecommunication Circuits (Cont'd)

Telecommunication Circuits (Cont'd)

Function	Device	Source	Page
Modem Circuits, PSK Modulator, Bell 212A	**XR2121**	**Exar**	**(3369)**
Modem Circuits, Sync/Async Converter	**XR2125**	**Exar**	**(3371)**
Modem Filter digitally programmable transversal filter	R5910	Reticon	
Modem Filter, FSK	**XR2103**	**Exar**	**(3368)**
Modem Filter, General Purpose (bandpass filter and MUX)	R5633	Reticon	
Modem Filter, PSK	**XR2120**	**Exar**	**(3368)**
Modem Filter with Equalizer, 212A/V.22	**S3522**	**AMI**	**(3345)**
Modem Filter (300 baud)	**MC145440**	**Motorola**	**(3536)**
	MC145441	**Motorola**	**(3536)**
	MC6170	Motorola	
	R5630	Reticon	
	R5631	Reticon	
Modem Filter (1200 baud)	CH1710	Cermetek	
	CH1720	Cermetek	
	CH1730	Cermetek	
	CH1740	Cermetek	
Modem Filter, 1200 Baud, 212/V.22	R5632	Reticon	
Modem Filter, (1200/150 Baud)	R5634	Reticon	
Modem Filter (1200/2400 baud)	**MC6862**	**Motorola**	**(1505)**
Modem (for serial communications at up to 600 b/s)	**MC6860**	**Motorola**	**(1505,3536)**
Modem, FSK Demodulator	XR2211	† Exar	
	XR2211	Exar	
	XR2211M	† Exar	
Modem, FSK Modulator	XR2206	† Exar	
	XR2206	Exar	
	XR2206M	† Exar	
	XR2207	Exar	
	XR2207M	Exar	
Modem Interface and Receiver Filter Circuit (300 baud modem)	CH1230	Cermetek	
Modem System, FSK	**XR14412F**	**Exar**	**(3369)**
	XR14412V	**Exar**	**(3369)**
	MC14412	**Motorola**	**(3536)**
Modem System, FSK, 1200 Baud	**SSI180**	**SiliconSys**	**(3665)**
Modem, 2400 bps Demodulator	**MC6173**	**Motorola**	**(3536)**
Multifrequency Interface Line Circuit	LS342	SGS	
Multifrequency Tone Generator (generates 15 tone pairs)	AMS3501	Aptek	
Multifrequency Tone Generator (module)	CM7050	Mitel	
PCM Repeater	XRC240	Exar	
	XRC262	Exar	
	XRC277	Exar	
	TCM2101	TI	
	TCM2102	TI	
PCM Signal Monitor	SP1450B	Plessey	
	SP1455B	Plessey	
Polynomial Generator/Checker (for character-oriented data communication links)	**SCN2653A**	**Signetics**	**(1671)**
RC Encoder, Programmable 7-Channel	**NE5044**	**Signetics**	**(3626)**
RD Decoder, Seven Channel	**NE5045**	**Signetics**	**(3629)**
Receiver, DTMF (hybrid)	MH88315	Mitel	
Relay Driver (for 48 V telephone relays)	DS1686	† National	
	DS1687	† National	
	DS3686	National	
	DS3687	National	
	UDN-2580A	Sprague	
	UDN-2585A	Sprague	
	UDN-2588A	Sprague	
	UDN-2956A	Sprague	
	UDN-2957A	Sprague	
Relay Driver, Quad Negative Voltage	DS3680	National	
	DS3680	TI	
Ring Detector (operates from 16 to 68 Hz)	TCM1520A	TI	
Serial Receiver (changes T1-D2 or T1-D3 input to parallel output)	R8060	Rockwell	
Serial Transmitter (generates 193-Bit data stream in T1-D2 or T1-D3 format)	R8050	Rockwell	
Signal Processing Peripheral (arithmetic processor, RAM, ROM, I/O)	**S28211A**	**AMI**	**(3349)**
	S28211B	**AMI**	**(3349)**
Speech Circuit for Electronic Telephones	TP5700	National	
	TP5710	National	
	PBL3725	RIFA	
	PBL3726	RIFA	
	TCM1705A	TI	
Subscriber Line Interface Circuit (hybrid SIP)	MH88505	Mitel	
	MH88506	Mitel	
	MH88510	Mitel	
Subscriber Line Interface Circuit (performs 2-wire to 4-wire conversion)	S2500A	AMI	
	S2550A	**AMI**	**(3344)**
	AMS2001	Aptek	
	AMS2002	Aptek	
	AMS2006	Aptek	
	AMS3081	Aptek	
	AMS3082	Aptek	
	AMS3084	Aptek	
	AMS3085	Aptek	
	HC5502	**Harris**	**(3466)**
	HC5504	**Harris**	**(3467)**
	MH88500	Mitel	
	MC34019	Motorola	
	MC3419	**Motorola**	**(3060)**
	MC3419A	**Motorola**	**(3060)**
	MC3419C	**Motorola**	**(3060)**
	MC3519	Motorola	
	LS285A	SGS	
	G150	Siemens	
	ST120	Signetics	
	TCM4204	TI	
	TCM4205	TI	
	TCM4207	TI	
Telephone Chipset (microcomputer-compatible)	TCM1707	TI	
	TCM1708	TI	
Telephone Restricter	CRN3300	Thomson-CSF	
Telephone Speech Circuit (programmable)	LS288	SGS	
Teletex Acquisition/Control	SAA5040B	Signetics	
Teletex Adaptive Data Slicer (provides data, clock and synchronizing signals)	SN76940	TI	
Teletex Character Generator, American	SAA5055	Signetics	
Teletex Timing Circuit, 525 Lines	SAA5025B	Signetics	
	SAA5025C	Signetics	
	SAA5025D	Signetics	
Teletex Timing Circuit, 625 Lines	SAA5020	Signetics	
Teletex Video Input Processor	SAA5030	Signetics	
Teletext GALA	SAA5045	Signetics	
Time Division Multiplexing, Demultiplexor	EFB7334	Thomson-CSF	
Time Division Multiplexing, Serial/Parallel Shift/Conversion	EFB7303	Thomson-CSF	
Time Division Multiplexing, Temporal Matrix for 8x8 frame switching	EF7331	Thomson-CSF	
Time Division Multiplexing, 2.048 MHz Clock Recovery	EF7332	Thomson-CSF	
Time Division Multiplexing, 2.048 MHz Communication Terminal	EF7332	Thomson-CSF	
Time Slot Access Circuit	MJ1446	Plessey	
Time Slot Assigner Circuit	**MC14416**	**Motorola**	**(3536)**
	MC14417	**Motorola**	**(3536)**
	MC14418	**Motorola**	**(3536)**
	EFB7336	Thomson-CSF	
Tone Caller	ZN473E	Ferranti	
Tone Decoder (operates from 0.01 Hz to 500 kHz)	XR2211C	Exar	
	XR2211M	† Exar	
	XR567AC	Exar	
	XR567AM	† Exar	
	LM567C	National	
	XR2211C	Raytheon	
	XR2211M	† Raytheon	
	NE567	Signetics	
	SE567	† Signetics	
Tone Decoder, Dual (operates from 0.01 Hz to 500 kHz)	**XR2567**	**Exar**	**(3367)**
	XR2567M	† Exar	
Tone Decoder, Dual	MT8860	Mitel	
	MT8862	Mitel	
	MT8863	Mitel	
	MV8860	Plessey	
	MV8862	Plessey	
	MV8863	Plessey	
	CRC8030	Rockwell	
	SSI202	SiliconSys	
Tone Receiver Circuit, Dual (combine with filters for touch tone receiver)	G8860	GTEMicro	
	G8860X	GTEMicro	
	MK5102-5	Mostek	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Telecommunication Circuits (Cont'd)

Telecommunication Circuits (Cont'd)

Function	Device	Source	
Tone Receiver Circuit, Dual (combine with filters for touch tone receiver) (Cont'd)			
	MK5103-5	Mostek	
	SM301A	Siemens	
	M967	Teltone	
	TT6174	Teltone	
Tone Receiver Circuit, Dual (with filters)			
	AMS3201	Aptek	
	AMS3210	Aptek	
	AMS88205-5NC	Aptek	
	G8870	GTEMicro	
	MH88210	Mitel	
	MH88305	Mitel	
	MT8870	Mitel	
	SSI201	**SiliconSys**	**(3685)**
	SSI202	**SiliconSys**	**(3685)**
	M927	Teltone	
	M937	Teltone	
	M947	Teltone	
	M948	Teltone	
	M956	Teltone	
	M957	Teltone	
Tone Ringer, (operates from ring signal, drives piezo element)	**MC34012**	**Motorola**	**(3060)**
Tone Ringer (operates from ring signal, drives speaker)			
	S2561A	**AMI**	**(3343)**
	S2561C	**AMI**	**(3343)**
	CS8204	Cherry	
	CS8205	Cherry	
	ML8204	Mitel	
	ML8205	Mitel	
	MC34012-1	**Motorola**	**(3060)**
	MC34012-2	**Motorola**	**(3060)**
	MC34012-3	**Motorola**	**(3060)**
	M764	SGS	
	M764A	SGS	
	TCM1501A	TI	
	TCM1506A	TI	
	TCM1512A	TI	
	TCM1513A	TI	
	TCM1520A	TI	
Transcoder, with Error Detection (10 kb/s to 2.048 Mb/s)	**CD22103**	**RCA**	**(840)**
Transmission Interface			
	TEA1042	Signetics	
	TEA1046	Signetics	
	TEA1055	Signetics	
Tri-Port Memory (T1 carrier)	R8040	Rockwell	
Universal Digital Loop Transceiver, Four Wire	MC145420	Motorola	
Universal Digital Loop Transceiver, Four Wire Slave	MC145425	Motorola	
Universal Digital-Loop Transceiver			
	MC145422	**Motorola**	**(3536)**
	MC145423	Motorola	
	MC145426	**Motorola**	**(3536)**
Videotex Decoder, Interactive	SAA5070	Signetics	
Single Channel Signaling Controller	EFB7335	Thomson-CSF	
Single Frequency Tunable Bandpass/Notch Filter/Tone Generator	**S3526**	**AMI**	**(3346)**
Dual Tone Generator (generates 12-16 tone pairs)			
	AY3-9400	GI	
	AY3-9410	GI	
Dual Tone Generator (touchtone frequencies)			
	S25089	**AMI**	**(3340)**
	S2559A	**AMI**	**(3339)**
	S2559B	**AMI**	**(3339)**
	S2559C	**AMI**	**(3339)**
	S2559D	**AMI**	**(3339)**
	S2559E	**AMI**	**(3339)**
	S2559F	**AMI**	**(3339)**
	S2559G	**AMI**	**(3339)**
	S2559H	**AMI**	**(3339)**
	S2859	AMI	
	S2860	AMI	
	AY5-9480	GI	
	AY5-9559	GI	
	ICM7206A	**Intersil**	**(3524)**
	ICM7206B	**Intersil**	**(3524)**
	ICM7206C	**Intersil**	**(3524)**
	ICM7206D	**Intersil**	**(3524)**
	SBA5089	ITT	
	SBA5091	ITT	
	MT5089	Mitel	
	MK5087	Mostek	
	MK5089	Mostek	
	MK5091	Mostek	
	MK5092	Mostek	
	MK5094	Mostek	
	MK5380	Mostek	
	MK5382	Mostek	
	MK5389	Mostek	
	MC14410	**Motorola**	**(3536)**
	MM53125	National	
	MM53130	National	
	MM5395	National	
	μPC767	NEC	
	CD22859	**RCA**	**(840)**
	PBD3534	RIFA	
	PBD3535	RIFA	
	M751	SGS	
	S359	Siemens	
	PCD3311	Signetics	
	PCD3312	Signetics	
	TCM5087	TI	
	TCM5089	TI	
	TCM5091	TI	
	TCM5092	TI	
	EFB7189	Thomson-CSF	
Dual Tone Generator with Redial			
	S2569	AMI	
	S2569A	AMI	
Two-Wire-to-Four Wire Converter (replaces hybrid transformer)	LS285A	SGS	
	ST120	Signetics	

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR

Master Selection Guide

LINEAR–Timers

Timers

Function	Device	Source	Page
Adjustable Threshold	MC1422	Motorola	
Delayed Switch ON/OFF (for driving relays, lamps, etc.)	PBA3008	RIFA	
	PBA3009	RIFA	
Internal Current Source	XR320	Exar	
Long Period (1 sec to 1 week)	AN6780	Panasonic	
Long Period (10 ms to 10,000 hours)	MW122	AnalogSys	
Low Power (supply 3 V)	SN76812	TI	
Micropower, Long Range (microseconds to days)	XR2243	Exar	
Microwave Oven Controller	TMS1117	TI	
	TMS1117NLP	TI	
Precision	MW107	AnalogSys	
	MW197	AnalogSys	
	LM122	† National	
	LM2905	National	
	LM322	National	
	LM3905	National	
Precision Decade, Direct 7 Segment and Digit Drivers	ICM7045A	Intersil	
Programmable (includes a counter for long time delays) Binary Control	XR2240C	Exar	
	XR2240M	† Exar	
	μA2240C	Fairchild	
	μA2240M	† Fairchild	
	ICM7240	Intersil	
	ICM7242	Intersil	
	ICM7250	Intersil	
	ICM7260	Intersil	
	LS7210	LSIComp	(803)
	MC14541BA	† Motorola	
	MC14541BC	Motorola	
	μA2240C	TI	
	μA2240M	† TI	
Timer	XR555C	Exar	
	XR555M	† Exar	
	XRL555	Exar	
	μA555C	Fairchild	
	NE555	Intersil	
	SE555	† Intersil	
	MC1455	Motorola	
	MC1555	† Motorola	
	LM555C	National	
	μPC1555	NEC	
	RC555	Raytheon	
	RM555	† Raytheon	
	CA555	† RCA	(3604)
	CA555C	RCA	(3604)
	NE555	Signetics	
	SE555	† Signetics	(526)
	SE555C	† Signetics	(526)
	SG555	† SiliconG	
	SG555C	SiliconG	
	ULN-2430M	Sprague	
	355A/C	TeledyneS	
	355B/M	† TeledyneS	
	NE555	TI	
	SE555	† TI	
	TD0555	Thomson-CSF	
	TA7326	Toshiba	
	TA7327	Toshiba	
Timer (CMOS 555), Low Power	ICM7555	Intersil	(3527)
	ICM7555M	† Intersil	(3527)
Timer with ÷ 12 Counter (time constant 7200 RC)	ZN1034E	Ferranti	
Timer with Counter, (time constant 128 RC)	XR2242C	Exar	
	XR2242M	† Exar	
Universal (includes two 4-digit counters, comparator, clock oscillator and divider)	MM5865	National	
Dual (CMOS 556) Low Power	ICM7556	Intersil	(3527)
	ICM7556M	† Intersil	(3527)
Dual (dual 555), Pinout Variations	XR2556C	Exar	
	XR2556M	† Exar	
Dual (dual 555)	XR556C	Exar	
	XR556M	† Exar	
	XRL556C	Exar	
	XRL556M	† Exar	
	μA556C	Fairchild	
	NE556	Intersil	
	SE556	† Intersil	
	MC3456	Motorola	
	MC3556	† Motorola	
	LM556	† National	
	LM556C	National	
	RC556	Raytheon	
	RM556	† Raytheon	
	NE556	Signetics	
	NE556-1	Signetics	
	SA556	Signetics	
	SA556-1	Signetics	
	SE556	† Signetics	(526)
	SE556-1	† Signetics	(526)
	SE556-1C	† Signetics	(526)
	SG556	† SiliconG	
	SG556C	SiliconG	
	NE556	TI	
	SE556	† TI	
	TD0556	Thomson-CSF	
Quad, Current Sink Output	XR558C	Exar	
	XR558M	† Exar	
	NE558	Signetics	(3670)
	SA558	Signetics	(3670)
	SE558	† Signetics	(3670)
Quad, Current Source Output	XR559C	Exar	
	XR559M	† Exar	

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR

Master Selection Guide

LINEAR–Voltage Regulators

Output Voltage, V	Output Current	Device	Source
Fixed, Positive			
For low amounts of current, voltage references can be used as voltage regulators. See Linear—Other Devices, Reference Diodes			
2.6	100	MC78L02C	Motorola
		μA78L02AC	TI
		μA78L02C	TI
		TA7316	Toshiba
5	100	μA78L05C	Fairchild
		LM2931-5	Motorola
		MC78L05AC	Motorola
		MC78L05C	Motorola
		LM140LA-5	National
		LM78L05A	National
		LM78L05C	National
		μPC78L05	NEC
		μA78L05AC	TI
		μA78L05C	TI
		TA78L005	Toshiba
		TA78L005A	Toshiba
	150	LM3931-5	National
		LM2930-5	TI
		LM330-5	TI
	200	**LM109H**	**Motorola** (3531)
		LM209H	**Motorola** (3531)
		LM309H	**Motorola** (3531)
		LM109H	† National
		LM209H	National
		LM2930-5	National
		LM309H	National
		LM330-5	National
		SG109T	† SiliconG
		SG209T	SiliconG
		SG309T	SiliconG
		SFC2109	† Thomson-CSF
		SFC2209	Thomson-CSF
		SFC2309	Thomson-CSF
	250	LM342-5	National
	400	L4805	SGS
	500	μA78M05C	Fairchild
		μA78M05M	† Fairchild
		TDD1605	ITT
		MC7705C	Motorola
		MC78M05C	Motorola
		LM341-5	National
		LM78M05	National
		μPC78M05	NEC
		L194-5	SGS
		L2605	SGS
		L4705	SGS
		L487	SGS
		SG140-05T	† SiliconG
		SG340-05T	SiliconG
		SG7805ACT	SiliconG
		SG7805AT	† SiliconG
		μA78M05C	TI
		μA78M05M	† TI
	750	LM2935	National
	850	L129	SGS
	1000	μA109M	† Fairchild
		μA209M	Fairchild
		μA309C	Fairchild
		LM109K	† **Motorola** (3531)
		LM209K	**Motorola** (3531)
		LM309K	**Motorola** (3531)
		LM109K	† National
		LM209K	National
		LM309K	National
		μPC7805	NEC
		(Continued)	
5	1000	(Cont'd)	
		L7805	† SGS
		L7805C	SGS
		SG109K	† SiliconG
		SG209K	SiliconG
		SG309K	SiliconG
		SG7805ACP	SiliconG
		SG7805AP	† SiliconG
		SG7805CP	† SiliconG
		SG7805P	SiliconG
		SFC2109M	Thomson-CSF
		SFC2805	† Thomson-CSF
		TA78005	Toshiba
		UC7805A	† **Unitrode** (3711)
		UC7805AC	**Unitrode** (3711)
	1500	μA7805C	Fairchild
		μA7805M	† Fairchild
		LAS1505	Lambda
		LAS15A05	Lambda
		LM140-5	† **Motorola** (3531)
		LM340-5	**Motorola** (3531)
		MC7805	† **Motorola** (3531)
		MC7805A	† **Motorola** (3531)
		MC7805AC	**Motorola** (3531)
		MC7805C	**Motorola** (3531)
		LM140-5	† National
		LM140A-5	† National
		LM2931-5	National
		LM340-5	National
		LM340A-5	National
		LM7805	National
		SG140-05K	SiliconG
		SG140-05R	SiliconG
		SG340-05K	SiliconG
		SG340-05R	SiliconG
		SG7805ACK	SiliconG
		SG7805ACR	SiliconG
		SG7805AK	† SiliconG
		SG7805CK	SiliconG
		SG7805CR	SiliconG
		SG7805K	† SiliconG
		SG78R05	† SiliconG
		LM340-5	TI
		TL780-05C	TI
		UC7805	† **Unitrode** (3711)
		UC7805C	**Unitrode** (3711)
	2000	HA17805P	Hitachi
		LAS1605	Lambda
		LAS1605B	Lambda
		L78S05	† SGS
		L78S05C	SGS
	3000	SH123	† Fairchild
		SH223	Fairchild
		SH323	Fairchild
		μA123	Fairchild
		μA223	† Fairchild
		μA323	Fairchild
		LAS1405	Lambda
		LAS1405B	Lambda
		LM123	† LinearTech
		LM123A	† LinearTech
		LM323	LinearTech
		LM323A	† LinearTech
		LM123	† **Motorola** (3531)
		LM123A	† **Motorola** (3531)
		LM223	**Motorola** (3531)
		LM223A	**Motorola** (3531)
		LM323	**Motorola** (3531)
		LM323A	**Motorola** (3531)
		MC78T05	† Motorola
		MC78T05A	† Motorola
		(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Voltage Regulators (Cont'd)

Fixed, Positive (Cont'd)

Output Voltage, V	Output Current	Device	Source	
5	3000	(Cont'd)		
		MC78T05AC	Motorola	
		MC78T05C	Motorola	
		LM123	† National	
		LM223	National	
		LM323	National	
		SG123	† SiliconG	
		SG153-05	† SiliconG	
		SG223	SiliconG	
		SG253-05	SiliconG	
		SG323	SiliconG	
		SG353-05	SiliconG	
	5000	µA78H05	Fairchild	
		µA78H05A	Fairchild	
		LAS1905	Lambda	
		LAS1905B	Lambda	
		LT1003C	LinearTech	
		LT1003M	† LinearTech	
		42050-055	Micropac	
		MLM138-05	Micropac	
		MLM338-05	Micropac	
	8000	LAS3905	Lambda	
		LAS3905K	Lambda	
	10000	µA78P05	Fairchild	
		42050-510	Micropac	
		LML196-05	Micropac	
		MLM396-05	Micropac	
		MPC100	Motorola	
	20000	42055-520	Micropac	
6	100	TA78L006	Toshiba	
		TA78L006A	Toshiba	
	500	µA78M06C	Fairchild	
		µA78M06M	† Fairchild	
		TDD1606	ITT	
		MC78M06C	Motorola	
		SG140-06T	† SiliconG	
		SG340-06T	SiliconG	
		SG7806ACT	SiliconG	
		SG7806AT	† SiliconG	
		SG7806CT	SiliconG	
		SG7806T	† SiliconG	
		µA78M06C	TI	
		µA78M06M	† TI	
	1000	SG7806ACP	SiliconG	
		SG7806AP	† SiliconG	
		SG7806CP	SiliconG	
		SG7806P	† SiliconG	
		SFC2806	Thomson-CSF	
	1500	µA7806C	Fairchild	
		LAS1506	Lambda	
		LM140-6	**† Motorola**	**(3531)**
		LM340-6	**Motorola**	**(3531)**
		MC7806	**† Motorola**	**(3531)**
		MC7806A	**† Motorola**	**(3531)**
		MC7806AC	**Motorola**	**(3531)**
		MC7806C	**Motorola**	**(3531)**
		SG140-06K	SiliconG	
		SG140-06R	SiliconG	
		SG340-06K	SiliconG	
		SG340-06R	SiliconG	
		SG7806ACK	SiliconG	
		SG7806ACR	SiliconG	
		SG7806AK	† SiliconG	
		SG7806CK	SiliconG	
		SG7806CR	SiliconG	
		SG7806K	† SiliconG	
		SG78R06	† SiliconG	
		µA7806C	TI	
		(Continued)		

Output Voltage, V	Output Current	Device	Source	
6		(Cont'd)		
	2000	HA17806P	Hitachi	
		CJSE017	Solitron	
		CJSE019	Solitron	
		CJSE021	Solitron	
	3000	LAS1406	Lambda	
		MC78T06	† Motorola	
		MC78T06C	Motorola	
	10000	42050-610	Micropac	
	20000	42055-620	Micropac	
6.2	100	µA78L62C	Fairchild	
		µA78L06AC	TI	
		µA78L06C	TI	
7	100	TA78L007	Toshiba	
		TA78L007A	Toshiba	
	10000	42050-710	Micropac	
	20000	42055-720	Micropac	
7.5	100	TA78L075	Toshiba	
		TA78L075A	Toshiba	
	1000	L7875	† SGS	
		L7875C	SGS	
		L78C75C	SGS	
		L78S75	† SGS	
8	100	MC78L08AC	Motorola	
		MC78L08C	Motorola	
		µPC78L08	NEC	
		µA78L08AC	TI	
		µA78L08C	TI	
		TA78L008	Toshiba	
		TA78L008A	Toshiba	
	150	LM2930-8	TI	
	200	LM2930-8	National	
	500	µA78M08C	Fairchild	
		µA78M08M	† Fairchild	
		TDD1608	ITT	
		MC78M08C	Motorola	
		µPC78M08	NEC	
		SG140-08T	† SiliconG	
		SG340-08T	SiliconG	
		SG7808ACT	SiliconG	
		SG7808AT	† SiliconG	
		SG7808CT	SiliconG	
		SG7808T	† SiliconG	
		µA78M08C	TI	
		µA78M08M	† TI	
		SFC2808	Thomson-CSF	
	1500	µA7808C	Fairchild	
		µA7808M	† Fairchild	
		HA17808	Hitachi	
		LAS1508	Lambda	
		LM140-8	**† Motorola**	**(3531)**
		LM340-8	**Motorola**	**(3531)**
		MC7808	**† Motorola**	**(3531)**
		MC7808A	**† Motorola**	**(3531)**
		MC7808AC	**Motorola**	**(3531)**
		MC7808C	**Motorola**	**(3531)**
		SG140-08K	SiliconG	
		SG140-08R	SiliconG	
		SG340-08K	SiliconG	
		SG340-08R	SiliconG	
		SG7808ACK	SiliconG	
		SG7808ACR	SiliconG	
		SG7808AK	† SiliconG	
		SG7808CK	SiliconG	
		SG7808CR	SiliconG	
		SG7808K	† SiliconG	
		SG78R08	SiliconG	
		µA7808C	TI	
		(Continued)		

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Voltage Regulators (Cont'd)

Output Voltage, V	Output Current	Device	Source
Fixed, Positive			**(Cont'd)**
8			(Cont'd)
	2000	LAS1608	Lambda
	3000	MC78T08	Motorola
		MC78T08C	Motorola
		SG153-08	† SiliconG
		SG253-08	SiliconG
		SG353-08	SiliconG
	5000	μA78H08C	Fairchild
	10000	μPC7808	NEC
		SG7808ACP	SiliconG
		SG7808AP	† SiliconG
		SG7808CP	SiliconG
		SG7808P	† SiliconG
	20000	42055-820	Micropac
8.2	100	μA78L82C	Fairchild
8.5	400	L4885	SGS
	500	L2685	SGS
		L4785	SGS
	1000	μA7885	Fairchild
		μA7885C	TI
9	100	μA78L09C	Fairchild
		μA78L09AC	TI
		μA78L09C	TI
		TA78L009	Toshiba
		TA78L009A	Toshiba
	1500	L7809	SGS
		L78S09	† SGS
		SL78S09C	SGS
	20000	42055-920	Micropac
10	100	μA78L10AC	TI
		μA78L10C	TI
		TA78L010	Toshiba
		TA78L010A	Toshiba
	200	LH0075	† National
	400	L4810	SGS
	500	TDD1610	ITT
		L2610	SGS
		L4710	SGS
		μA78M10C	TI
	1500	LAS1510	Lambda
		μA7810C	TI
	2000	L78S10	† SGS
		L78S10C	SGS
	9000	42050-109	Micropac
	20000	42055-1020	Micropac
12	100	μA78L12C	Fairchild
		MC78L12AC	† Motorola
		MC78L12C	Motorola
		LM140LA-12	† National
		LM340LA-12	National
		LM78L12A	National
		LM78L12C	National
		μPC78L12	NEC
		μA78L12AC	TI
		μA78L12C	TI
		TA78L012	Toshiba
		TA78L012A	Toshiba
	250	LM342-12	National
	500	μA78M12C	Fairchild
		μA78M12M	† Fairchild
		TDD1612	ITT
		MC78M12C	Motorola
		LM341-12	National
		LM78M12	National
		μPC78M12	NEC
12	500		(Cont'd)
		L194-12	SGS
		SG140-12T	† SiliconG
		SG340-12T	SiliconG
		SG7812ACT	SiliconG
		SG7812AT	† SiliconG
		SG7812CT	SiliconG
		SG7812T	† SiliconG
		μA78M12C	TI
		μA78M12M	† TI
	720	L130	SGS
	1000	μPC7812	NEC
		STK521	Sanyo
		STK541	Sanyo
		SG7812ACR	SiliconG
		SG7812AR	† SiliconG
		SG7812CR	SiliconG
		SG7812R	† SiliconG
		SFC2812	Thomson-CSF
		TA78012	Toshiba
		UC7812	**† Unitrode (3711)**
		UC7812C	**Unitrode (3711)**
	1500	μA7812C	Fairchild
		μA7812M	† Fairchild
		LAS1512	Lambda
		LAS15A12	Lambda
		LM140-12	**† Motorola (3531)**
		LM340-12	**Motorola (3531)**
		MC7812	**† Motorola (3531)**
		MC7812A	**† Motorola (3531)**
		MC7812AC	**Motorola (3531)**
		MC7812C	**Motorola (3531)**
		LM140-12	† National
		LM140A-12	† National
		LM340-12	National
		LM340A-12	National
		LM7812	National
		L7812	† SGS
		L7812C	SGS
		SG140-12K	† SiliconG
		SG140-12R	† SiliconG
		SG340-12K	SiliconG
		SG340-12P	SiliconG
		SG340-12R	SiliconG
		SG7812ACK	SiliconG
		SG7812ACP	SiliconG
		SG7812AK	† SiliconG
		SG7812CK	SiliconG
		SG7812CP	SiliconG
		SG7812K	† SiliconG
		SG78R12	SiliconG
		LM340-12	TI
		TL780-12C	TI
		μA7812C	TI
		UC7812A	**† Unitrode (3711)**
		UC7812AC	**Unitrode (3711)**
	2000	HA17812P	Hitachi
		LAS1612	Lambda
		LAS1612B	Lambda
		STK531	Sanyo
		L7812	† SGS
		L7812C	SGS
		L78S12C	SGS
	3000	LAS1412	Lambda
		LAS1412B	Lambda
		MC78T12	† Motorola
		MC78T12A	† Motorola
		MC78T12AC	Motorola
		MC78T12C	Motorola
		SG153-12	† SiliconG

(Continued)

† Military Temperature Range (−55° to 125°C)   * Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Voltage Regulators (Cont'd)

Output Voltage, V	Output Current	Device	Source
Fixed, Positive			**(Cont'd)**
12	3000		(Cont'd)
		SG253-12	SiliconG
		SG353-12	SiliconG
	5000	µA78H12A	Fairchild
		LAS1912	Lambda
		LAS1912B	Lambda
		MLM138-12	Micropac
		MLM338-12	Micropac
	8000	42050-128	Micropac
	10000	MLM196-12	Micropac
		MLM396-12	Micropac
	16000	42055-1216	Micropac
13.2	100	TA78L132	Toshiba
		TA78L132A	Toshiba
	1500	LAS15CB	Lambda
13.8	2000	LAS16CB	Lambda
14	2000	LAS16CB	Lambda
	8000	42050-148	Micropac
	16000	42055-1416	Micropac
15	100	µA78L15C	Fairchild
		MC78L15AC	Motorola
		MC78L15C	Motorola
		LM140LA-15	† National
		LM340LA-15	National
		LM78L15A	National
		LM78L15C	National
		µPC78L15	NEC
		µA78L15AC	TI
		µA78L15C	TI
		TA78L015	Toshiba
		TA78L015A	Toshiba
	250	LM342-15	National
	500	µA78M15C	Fairchild
		µA78M15M	† Fairchild
		TDD1615	ITT
		MC78M15C	Motorola
		LM341-15	National
		LM78M15	National
		µPC78M15	NEC
		L194-15	SGS
		SG140-15T	† SiliconG
		SG7815ACT	SiliconG
		SG7815AT	† SiliconG
		SG7815CT	SiliconG
		SG7815T	† SiliconG
		µA78M15C	TI
		µA78M15M	† TI
	600	L131	SGS
	1000	L7815	† SGS
		L7815C	SGS
		SG7815ACR	SiliconG
		SG7815AR	† SiliconG
		SG7815CR	SiliconG
		SG7815R	† SiliconG
		TA78015	Toshiba
		UC7815	**† Unitrode (3711)**
		UC7815A	**† Unitrode (3711)**
		UC7815AC	**Unitrode (3711)**
		UC7815C	**Unitrode (3711)**
	1500	µA7815C	Fairchild
		µA7815M	† Fairchild
		LAS1515	Lambda
		LAS15A15	Lambda
		LM140-15	**† Motorola (3531)**
		LM340-15	**Motorola (3531)**
		MC7815	**† Motorola (3531)**
			(Continued)

Output Voltage, V	Output Current	Device	Source
15	1500		(Cont'd)
		MC7815A	**† Motorola (3531)**
		MC7815AC	**Motorola (3531)**
		MC7815C	**Motorola (3531)**
		LM140-15	† National
		LM140A-15	† National
		LM340-15	National
		LM340A-15	National
		LM7815	National
		SG140-15K	† SiliconG
		SG140-15R	† SiliconG
		SG7815ACK	SiliconG
		SG7815ACP	SiliconG
		SG7815AK	† SiliconG
		SG7815CK	SiliconG
		SG7815CP	SiliconG
		SG7815K	† SiliconG
		SG78R15	SiliconG
		LM340-15	TI
		TL780-15C	TI
		µA7815C	TI
	2000	HA17815P	Hitachi
		LAS1615	Lambda
		LAS1615B	Lambda
		L78S15	† SGS
		L78S15C	SGS
		CJSE001	Solitron
		CJSE003	Solitron
		CJSE005	Solitron
	3000	LAS1415	Lambda
		LAS1415B	Lambda
		MC78T15	† Motorola
		MC78T15A	† Motorola
		MC78T15AC	Motorola
		MC78T15C	Motorola
		SG153-15	† SiliconG
		SG253-15	SiliconG
		SG353-15	SiliconG
	5000	LAS1915	Lambda
		LAS1915B	Lambda
		LML138-15	Micropac
		LML338-15	Micropac
	8000	42050-158	Micropac
	10000	MLM196-15	Micropac
		MLM396-15	Micropac
	16000	42055-1516	Micropac
16	8000	42050-168	Micropac
	12000	42055-1612	Micropac
18	100	MC78L18AC	Motorola
		MC78L18C	Motorola
		TA78L018	Toshiba
		TA78L018A	Toshiba
	500	TDD1618	ITT
		MC78M18C	Motorola
		µPC78M18	NEC
		SG140-18T	† SiliconG
		SG340-18T	SiliconG
		SG7818ACT	SiliconG
		SG7818AT	† SiliconG
		SG7818CT	SiliconG
		SG7818T	† SiliconG
	1000	µPC7818	NEC
		STK522	Sanyo
		STK542	Sanyo
		L7818	† SGS
		L7818C	SGS
		SG7817AP	† SiliconG
		SG7818ACP	† SiliconG
		SG7818AP	SiliconG
			(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Voltage Regulators (Cont'd)

Fixed, Positive (Cont'd)

Output Voltage, V	Output Current	Device	Source	
18	1000	(Cont'd)		
		SG7818P	SiliconG	
		SFC2818	Thomson-CSF	
	1500	μA7818C	Fairchild	
		μA7818M	† Fairchild	
		HA17818P	Hitachi	
		LAS1518	Lambda	
		LM140-18	**† Motorola**	**(3531)**
		LM340-18	**Motorola**	**(3531)**
		MC7818	**† Motorola**	**(3532)**
		MC7818A	**† Motorola**	**(3532)**
		MC7818AC	**Motorola**	**(3532)**
		MC7818C	**Motorola**	**(3532)**
		SG140-18K	SiliconG	
		SG140-18R	SiliconG	
		SG340-18K	SiliconG	
		SG340-18R	SiliconG	
		SG7818ACK	SiliconG	
		SG7818ACP	SiliconG	
		SG7818AK	† SiliconG	
		SG7818CK	SiliconG	
		SG7818CP	SiliconG	
		SG7818K	† SiliconG	
		SG78R18	SiliconG	
		μA7818C	TI	
	2000	MC78T18	† Motorola	
		MC78T18C	Motorola	
		STK532	Sanyo	
		L78S18	† SGS	
		L78S18C	SGS	
	3000	SG153-18	† SiliconG	
		SG253-18	SiliconG	
		SG353-18	SiliconG	
	8000	42050-188	Micropac	
	12000	42055-1812	Micropac	
		42055-1812	Toshiba	
20	100	TA78L020	Toshiba	
		TA78L020A	Toshiba	
	500	MC78M20C	Motorola	
		SG140-20T	† SiliconG	
		SG340-20T	SiliconG	
		SG7820ACT	SiliconG	
		SG7820AT	† SiliconG	
		SG7820CT	SiliconG	
		SG7820T	† SiliconG	
		μA78M20C	TI	
		μA78M20M	† TI	
	1000	LAS1520	Lambda	
		SG140-20K	† SiliconG	
		SG140-20R	† SiliconG	
		SG240-20K	SiliconG	
		SG340-20P	SiliconG	
		SG340-20R	SiliconG	
		SG7820K	† SiliconG	
		SG7820R	† SiliconG	
		SG78R20	† SiliconG	
	2000	CJSE009	Solitron	
		CJSE011	Solitron	
		CJSE013	Solitron	
	8000	42050-208	Micropac	
		42055-2010	Micropac	
22	4000	42050-224	Micropac	
	10000	42055-2210	Micropac	
24	100	MC78L24AC	Motorola	
		MC78L24C	Motorola	
		TA78L024	Toshiba	
		TA78L024A	Toshiba	
24		(Cont'd)		
	300	STK507	Sanyo	
	500	μA78M24C	Fairchild	
		μA78M24M	† Fairchild	
		TDD1624	ITT	
		MC78M24C	Motorola	
		μPC78M24	NEC	
		SG140-24T	† SiliconG	
		SG340-24T	SiliconG	
		SG7824ACT	SiliconG	
		SG7824AT	† SiliconG	
		SG7824CT	SiliconG	
		SG7824T	† SiliconG	
		μA78M24C	TI	
		μA78M24M	† TI	
	1000	μPC7824	NEC	
		STK523	Sanyo	
		L7824	† SGS	
		L7824C	SGS	
		SG7824ACP	SiliconG	
		SG7824AP	† SiliconG	
		SG7824CP	SiliconG	
		SG7824P	† SiliconG	
		SFC2824	Thomson-CSF	
	1500	μA7824C	Fairchild	
		μA7824M	† Fairchild	
		LAS1524	Lambda	
		LM140-24	**† Motorola**	**(3531)**
		LM340-24	**Motorola**	**(3531)**
		MC7824	**† Motorola**	**(3532)**
		MC7824A	**† Motorola**	**(3532)**
		MC7824AC	**Motorola**	**(3532)**
		MC7824C	**Motorola**	**(3532)**
		SG140-24K	SiliconG	
		SG140-24R	SiliconG	
		SG340-24K	SiliconG	
		SG340-24P	SiliconG	
		SG340-24R	SiliconG	
		SG7824ACK	SiliconG	
		SG7824ACR	SiliconG	
		SG7824AK	† SiliconG	
		SG7824CK	SiliconG	
		SG7824CR	SiliconG	
		SG7824K	† SiliconG	
		SG78R24	SiliconG	
		μA7824C	TI	
	2000	HA17824P	Hitachi	
		MC78T24	† Motorola	
		MC78T24C	Motorola	
		STK533	Sanyo	
		L78S24	† SGS	
		L78S24C	SGS	
	4000	42050-244	Micropac	
	10000	42055-2410	Micropac	
26	4000	42050-264	Micropac	
	8000	42055-2608	Micropac	
28	1500	LAS1528	Lambda	
	4000	42050-284	Micropac	
	8000	42055-2808	Micropac	
30	4000	42050-304	Micropac	
31	Shunt	TAA550	National	
32	4000	42050-324	Micropac	
33	Shunt	TAA550	National	
34	4000	42050-344	Micropac	
35	Shunt	TAA550	National	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Voltage Regulators (Cont'd)

Output Voltage, V	Output Current	Device	Source	
Fixed, Negative				
2	1000	MC7902C	Motorola	
	1500	LAS1802	Lambda	
	2000	μA79E02	† Fairchild	
		μA79E02C	Fairchild	
3	100	MC79L03AC	Motorola	
		MC79L03C	Motorola	
5	100	MC79L05AC	Motorola	
		MC79L05C	Motorola	
		LM320L05	National	
		LM79L05	National	
		LM79L05A	National	
		MC79L05AC	TI	
		MC79L05C	TI	
	250	LM320ML05	National	
	500	μA79M05C	Fairchild	
		μA79M05M	† Fairchild	
		LM120H5	† National	
		LM320H5	National	
		LM320MP5	National	
		LM79M05	National	
		SG120-05T	† SiliconG	
		SG220-05T	SiliconG	
		SG320-05T	SiliconG	
		μA79M05C	TI	
		μA79M05M	† TI	
	1000	μPC7905	NEC	
		SG120-05P	† SiliconG	
		SG220-05P	SiliconG	
		SG320-05P	SiliconG	
	1500	μA7905C	Fairchild	
		μA7905M	† Fairchild	
		LAS1805	Lambda	
		LAS18A05	Lambda	
		MC7905C	**Motorola**	(3531)
		LM120K5	† National	
		LM320K5	National	
		LM320T5	National	
		LM7905	National	
		SG120-05K	† SiliconG	
		SG220-05K	SiliconG	
		SG220-05R	SiliconG	
		SG320-05K	SiliconG	
		SG320-05R	SiliconG	
		SG7905	† SiliconG	
		SG7905A	† SiliconG	
		SG7905C	SiliconG	
		μA7905C	TI	
		TDC2905	Thomson-CSF	
		UC7905	† **Unitrode**	(3711)
		UC7905A	† **Unitrode**	(3711)
		UC7905AC	**Unitrode**	(3711)
		UC7905C	**Unitrode**	(3711)
	3000	MC79052C	Motorola	
		LM145K5	† National	
		LM345K5	National	
	5000	42051-055	Micropac	
5.2	500	SG120-5	† SiliconG	
		SG220-5	SiliconG	
		SG320-5	SiliconG	
	1000	SG120-5	† SiliconG	
		SG220-5	SiliconG	
		SG320-5	SiliconG	
	1500	LAS18052	Lambda	
		MC7905	**Motorola**	(3531)
		SG120-5	SiliconG	
		SG220-5	SiliconG	
		SG220-5	SiliconG	
			(Continued)	
5.2	1500			(Cont'd)
		SG320-5	SiliconG	
		SG320-5	SiliconG	
		SG7905	† SiliconG	
		SG7905	† SiliconG	
		SG7905	SiliconG	
		SG7905	SiliconG	
		μA7952C	TI	
	3000	LM145K5	† National	
		LM345K5	National	
6	500	μA79M06C	TI	
		μA79M06M	† TI	
	1500	LAS1806	Lambda	
		MC7906C	**Motorola**	(3531)
		μA7906C	TI	
	2000	CJSE018	Solitron	
		CJSE020	Solitron	
	5000	42051-065	Micropac	
7	5000	42051-075	Micropac	
8	500	μA7908M	† Fairchild	
		μA79M08C	Fairchild	
		SG120-08T	† SiliconG	
		SG320-08T	SiliconG	
		μA79M08C	TI	
		μA79M08M	† TI	
	1000	μA7908C	Fairchild	
		LAS1808	Lambda	
		MC7908C	**Motorola**	(3531)
		μPC7908	NEC	
		SG120-08K	† SiliconG	
		SG120-08R	† SiliconG	
		SG320-08K	SiliconG	
		SG320-08P	SiliconG	
		SG320-08R	SiliconG	
		SG7908	† SiliconG	
		SG7908A	† SiliconG	
		SG7908AC	SiliconG	
		SG7908C	SiliconG	
		μA7908C	TI	
	5000	42051-085	Micropac	
9	1500	42051-095	Micropac	
10	1500	LAS1810	Lambda	
	5000	42051-105	Micropac	
12	100	MC79L12AC	Motorola	
		MC79L12C	Motorola	
		LM320L12	National	
		LM79L12	National	
		LM79L12A	National	
		MC79L12AC	TI	
		MC79L12C	TI	
	200	LM120H12	† National	
		LM320H12	National	
		SG120-12T	† SiliconG	
		SG220-12T	SiliconG	
		SG320-12T	SiliconG	
	500	μA79M12C	Fairchild	
		μA79M12M	† Fairchild	
		LM320MP12	National	
		LM79M12	National	
		μA79M12C	TI	
		μA79M12M	† TI	
	1000	LM120K12	† National	
		LM320K12	National	
		LM320T12	National	
		μPC7912	NEC	
		SG120-12P	† SiliconG	
		SG220-12P	SiliconG	
		SG320-12P	SiliconG	
			(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Voltage Regulators (Cont'd)

Fixed, Negative (Cont'd)

Output Voltage, V	Output Current	Device	Source	
12 (Cont'd)	1500	µA7912C	Fairchild	
		µA7912M	† Fairchild	
		LAS1812	Lambda	
		LAS18A12	Lambda	
		MC7912AC	**Motorola**	(3531)
		MC7912C	**Motorola**	(3531)
		LM7912	National	
		SG120-12K	† SiliconG	
		SG220-12K	SiliconG	
		SG220-12R	SiliconG	
		SG320-12K	SiliconG	
		SG320-12R	SiliconG	
		SG7912	† SiliconG	
		SG7912A	† SiliconG	
		SG7912AC	SiliconG	
		SG7912C	SiliconG	
		µA7912C	TI	
		TDC2912	Thomson-CSF	
		UC7912	† **Unitrode**	(3711)
		UC7912A	† **Unitrode**	(3711)
		UC7912AC	**Unitrode**	(3711)
		UC7912C	**Unitrode**	(3711)
	4000	42051-124	Micropac	
14	4000	42051-144	Micropac	
15	100	MC79L15AC	Motorola	
		MC79L15C	Motorola	
		LM320L15	National	
		LM79L15	National	
		LM79L15A	National	
		MC79L15AC	TI	
		MC79L15C	TI	
	200	LM120H15	† National	
		LM320H15	National	
		SG120-15T	† SiliconG	
		SG220-15T	SiliconG	
		SG320-15T	SiliconG	
	250	LM320ML15	National	
	500	µA79M15C	Fairchild	
		µA79M15M	† Fairchild	
		LM320MP15	National	
		LM79M15	National	
		µA79M15C	TI	
		µA79M15M	† TI	
	1000	MC79L15A	Motorola	
		LM120K15	† National	
		LM320K15	National	
		LM320T15	National	
		µPC7915	NEC	
		SG120-15R	† SiliconG	
		SG220-15R	SiliconG	
		SG320-15R	SiliconG	
	1500	µA7915C	Fairchild	
		µA7915M	† Fairchild	
		LAS1815	Lambda	
		LAS18A15	Lambda	
		MC7915AC	**Motorola**	(3531)
		MC7915C	**Motorola**	(3531)
		LM7915	National	
		SG120-15K	† SiliconG	
		SG220-15K	SiliconG	
		SG220-15P	SiliconG	
		SG320-15K	SiliconG	
		SG320-15P	SiliconG	
		SG7915	† SiliconG	
		SG7915A	† SiliconG	
		SG7915AC	SiliconG	
		SG7915C	SiliconG	
			(Continued)	
15	1500 (Cont'd)	µA7915C	TI	
		TDC2915	Thomson-CSF	
		UC7915	† **Unitrode**	(3711)
		UC7915A	† **Unitrode**	(3711)
		UC7915AC	**Unitrode**	(3711)
		UC7915C	**Unitrode**	(3711)
	2000	42051-154	Micropac	
		CJSE002	Solitron	
		CJSE004	Solitron	
		CJSE006	Solitron	
16	4000	42051-164	Micropac	
18	100	MC79L18C	Motorola	
	500	SG120-18T	† SiliconG	
		SG320-18T	SiliconG	
	1000	µPC7918	NEC	
	1500	LAS1818	Lambda	
		MC7918C	**Motorola**	(3532)
		MC79L18AC	Motorola	
		SG120-18K	† SiliconG	
		SG120-18R	† SiliconG	
		SG320-18K	SiliconG	
		SG320-18P	SiliconG	
		SG320-18R	SiliconG	
		SG7918	† SiliconG	
		SG7918A	† SiliconG	
		SG7918AC	SiliconG	
		SG7918C	SiliconG	
		µA7918C	TI	
	4000	42051-184	Micropac	
20	500	SG120-20T	† SiliconG	
		µA79M20C	TI	
		µA79M20M	† TI	
	1500	LAS1820	Lambda	
		SG120-20K	† SiliconG	
		SG120-20R	† SiliconG	
		SG7920	† SiliconG	
		SG7920A	† SiliconG	
		SG7920AC	SiliconG	
		SG7920C	SiliconG	
	2000	CJSE010	Solitron	
		CJSE012	Solitron	
		CJSE014	Solitron	
	3000	42051-204	Micropac	
22	3000	42051-223	Micropac	
24	100	MC79L24AC	Motorola	
		MC79L24C	Motorola	
	500	µA79M24C	TI	
		µA79M24M	† TI	
	1000	µPC7924	NEC	
	1500	LAS1824	Lambda	
		MC7924C	**Motorola**	(3532)
		µA7924C	TI	
	3000	42051-243	Micropac	
26	3000	42051-263	Micropac	
28	1500	LAS1828	Lambda	
	3000	42051-283	Micropac	
30	3000	42051-303	Micropac	
31	Shunt	TAA550	National	
32	3000	42051-323	Micropac	
33	Shunt	TAA550	National	
35	Shunt	TAA550	National	
36	3000	42051-363	Micropac	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

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Master Selection Guide

Fixed, Dual

Output Voltage, V	Output Current	Device	Source
+5,+5	750,10	**LM2935**	**National (3540)**
	1000,50	LT1005C	LinearTech
		LT1005M	LinearTech
±6	5000	42051	Micropac
±12	100	LM126	† National
		LM326	National
±15	100	XR1468	Exar
		XR1568	† Exar
		XR4195	Exar
		MC1468	Motorola
		MC1568	† Motorola
		LM125	† National
		LM325	National
		RC4195	Raytheon
		RM4195	† Raytheon
		SG1468	SiliconG
		SG1568	† SiliconG
		SG4501	SiliconG
		TA7179	Toshiba
	200	SG1501A	† SiliconG
		SG2501A	SiliconG
		SG3501A	SiliconG

Adjustable, Positive

Arranged in sequence by Output Voltage-High, Output Current, and then Output Voltage-Low.

Suffixes designating package style differences are basically dropped in the Adjustable Voltage Regulator Section. Thus identical part numbers may be referenced more than once under different parameters. Consult manufacturers on availability of different grades.

Output Voltage Hi	Low	Output Current	Device	Source
16	1.3	40	**ICL7663**	**Intersil (3505)**
	4	8000	LAS39U	Lambda
20	1.2	10000	LM196	National
			LM396	National
	2	20	LM300	Intersil
			SG300	SiliconG
			SFC2300	Thomson-CSF
24	3	150	LM2931	National
26	1.8	12	**CA3085**	**† RCA (3602)**
27	0	200	LH0075	† National
			LH0075C	National
30	2	20	LM100	† Intersil
			SG100	† SiliconG
			SG200	SiliconG
			SFC2100	† Thomson-CSF
			SFC2200	Thomson-CSF
	2.6	3000	LAS14AU	Lambda
	3	Shunt	TL430C	TI
		1800	L200	SGS
	4	1500	LAS15U	Lambda
		2000	LAS16U	Lambda
		5000	LAS19U	Lambda
	4.5	12	μA305C	Fairchild
			LM305	Intersil
			LM305	National
			μPC141	NEC
			μPC305	NEC
			μPC325	NEC
			SG305	SiliconG
	5	500	μA78MG	Fairchild
		1000	μA78G	Fairchild
		5000	μ78HG	Fairchild
32	1.2	100	TL317	TI
		3000	LM150	† LinearTech
			LM150A	† LinearTech
			LM350	LinearTech
			LM350A	LinearTech
			LM150	**† Motorola (3532)**
			LM250	**Motorola (3532)**
			LM350	**Motorola (3532)**
			LM150	† National
			LM250	National
			LM350	National
			SG150	† SiliconG
			SG150A	SiliconG
			SG250	SiliconG
			SG250A	SiliconG
			SG350	SiliconG
			SG350A	SiliconG
			LM350	TI
			UC150	**† Unitrode (3711)**
			UC250	**Unitrode (3711)**
			UC350	**Unitrode (3711)**
		5000	LM138	† LinearTech
			LM338	LinearTech
			LT138A	† LinearTech
			LT338A	LinearTech
			LM138	† National
			LM238	National
			LM338	National
	2.5	200	**MC1469**	**Motorola (3532)**
		500	MC1469	Motorola
	3.3	200	TA7089	Toshiba
33	1.2	3000	LLM350	Lambda
		5000	LLM338	Lambda
36	1.7	100	**CA3085A**	**† RCA (3602)**
	2.5	100	μA431	Fairchild
			TL431C	**Motorola (3535)**
			TL431M	**† Motorola (3535)**
			TL431C	TI
			TL431M	† TI
	2.85	2000	TDA200	Thomson-CSF
37	1.2	100	**LM117L**	**† Motorola (3532)**
			LM217L	**Motorola (3532)**
			LM317L	**Motorola (3532)**
			LM317L	National
		500	SG117	† SiliconG
			SG217	SiliconG
			SG317	SiliconG
			TL117L	† TI
		1500	μA117	† Fairchild
			μA217	Fairchild
			μA317	Fairchild
			LLM317	Lambda
			LM117	† LinearTech
			LM317	LinearTech
			LT117A	† LinearTech
			LT317A	LinearTech
			MCELM117	MCE
			MCELM217	MCE
			MCELM317	MCE
			LM117	**† Motorola (3532)**
			LM217	**Motorola (3532)**
			LM317	**Motorola (3532)**
			LM117	† National
			LM217	National
			LM317	National
			SG117	† SiliconG
			SG217	SiliconG
			SG317	SiliconG
			LM217	TI
			LM317	TI

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Voltage Regulators (Cont'd)

Output Voltage Hi	Low	Output Current	Device	Source	Page
Adjustable, Positive (Cont'd)					
37	1.2	1500	(Cont'd)		
			TDC0117	† Thomson-CSF	
			TDC0137	† Thomson-CSF	
			UC117	† **Unitrode**	**(3711)**
			UC217	**Unitrode**	**(3711)**
			UC317	**Unitrode**	**(3711)**
	2	150	μA723C	Fairchild	
			μA723M	† Fairchild	
			μA723	Intersil	
			MC1723	† **Motorola**	**(3532)**
			MC1723C	**Motorola**	**(3532)**
			LM723	† National	
			LM723C	National	
			RC723	Raytheon	
			RM723	† Raytheon	
			CA723	† **RCA**	**(3602)**
			CA723C	**RCA**	**(3602)**
			SA723C	Signetics	
			μA723	† Signetics	
			μA723C	Signetics	
			SG723	† SiliconG	
			SG723C	SiliconG	
			μA723C	TI	
			μA723M	† TI	
			SFC2723C	† Thomson-CSF	
			SFC2723EC	Thomson-CSF	
	2.5	250	**LM117M**	† **Motorola**	**(3532)**
			LM217M	**Motorola**	**(3532)**
			LM317M	**Motorola**	**(3532)**
			MC1569	† **Motorola**	**(3532)**
		600	MC1569	† Motorola	
	5	25	μA376C	Fairchild	
			LM376	National	
38	2	100	SG3532	SiliconG	
		150	LAS1000	Lambda	
			LAS723	Lambda	
	3	150	L123CB	SGS	
			L123CT	SGS	
40	0	150	LAS3700	Lambda	
	4.5	12	μA105M	† Fairchild	
			LM105	† National	
			LM205	National	
			SG105	† SiliconG	
			SG205	SiliconG	
			SFC2105	† Thomson-CSF	
			SFC2205	Thomson-CSF	
		45	μA305AC	Fairchild	
			LM305A	National	
			SG305A	SiliconG	
			SFC2305	Thomson-CSF	
46	1.7	100	**CA3085B**	† **RCA**	**(3602)**
48	2	100	SG1532	† SiliconG	
			SG2532	SiliconG	
		150	LAS1100	Lambda	
			LAS723B	Lambda	
56	8	1000	CJCA001	Solitron	
			CJCA007	Solitron	
57	1.2	500	LM117HV	† LinearTech	
			LM317HV	LinearTech	
			LT117AHV	† LinearTech	
			LT317AHV	LinearTech	
		1500	LM117AHV	† LinearTech	
			LM317AHV	LinearTech	
			LT117AHV	† LinearTech	
77	2	150	L146	SGS	
			TDB1146	Thomson-CSF	
125	1.25	700	TL783C	TI	
1000	0	100	MC1466	Motorola	
			MC15666	† Motorola	
Adjustable, Negative					
16	1.3	40	**ICL7664**	**Intersil**	**(3505)**
24	2.2	5000	μA79HG	Fairchild	
27	0	200	LH0076	† National	
			LH0076C	National	
30	0.035	20	LM304	National	
			μPC142	NEC	
			SG304	SiliconG	
			SFC2304	Thomson-CSF	
	2.2	500	μA79MG	Fairchild	
		1000	μA79G	Fairchild	
	2.6	1500	LAS18U	Lambda	
32	3.8	250	**MC1463G**	**Motorola**	**(3532)**
		500	TA7085A	Toshiba	
33	3.6	250	**MC1563G**	**Motorola**	**(3532)**
34	3.8	600	**MC1463R**	**Motorola**	**(3532)**
37	1.2	500	LM137	† LinearTech	
			LM337	LinearTech	
			LT137A	† LinearTech	
			LT337A	LinearTech	
			LM137	† **Motorola**	**(3532)**
			LM137M	**Motorola**	**(3532)**
			LM237	**Motorola**	**(3532)**
			LM237M	**Motorola**	**(3532)**
			LM337	**Motorola**	**(3532)**
			LM337M	**Motorola**	**(3532)**
		1500	MCELM137	MCE	
			MCELM237	MCE	
			MCELM337	MCE	
			LM137	† National	
			LM237	National	
			LM337	National	
			LT137A	† National	
			LT337A	National	
			SG137	† SiliconG	
			SG237	SiliconG	
			SG337	SiliconG	
			LM137	† TI	
			LM237	TI	
			LM337	TI	
			UC137	† **Unitrode**	**(3711)**
			UC237	**Unitrode**	**(3711)**
			UC337	**Unitrode**	**(3711)**
	3.6	600	MC1536R	† Motorola	
40	0.015	20	LM104	† National	
			LM204	National	
			SG204	SiliconG	
			SG304	SiliconG	
			SFC2204	Thomson-CSF	
			SGC2104	† Thomson-CSF	
47	1.2	500	LM137HV	† LinearTech	
			LM337HV	LinearTech	
			LT137AHV	† LinearTech	
			LT337AHV	LinearTech	
		1500	LM137HV	† LinearTech	
			LM337HV	LinearTech	
			LT137AHV	† LinearTech	
			LT337AHV	LinearTech	
56	8	1000	CJCA002	Solitron	
			CJCA008	Solitron	
57	1.2	100	LM337L	National	
		1500	LM137	† National	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Voltage Regulators (Cont'd)

Output Voltage Hi	Low	Output Current	Device	Source	
Adjustable, Negative					**(Cont'd)**
57	1.2	1500			(Cont'd)
			LM237	National	
			LM337	National	
			UC137	† Unitrode	
			UC237	Unitrode	
			UC337	Unitrode	
Adjustable, Dual					
± 15.5	± 14.5	100	MC1468	Motorola	
			MC1568	† Motorola	
± 20	± 8	100	MC1468	Motorola	
			MC1568	† Motorola	
			SG1468	SiliconG	
			SG1568	† SiliconG	
	± 14.5	100	SG1468T	SiliconG	
			SG1568T	† SiliconG	
± 28	± 10	100	SG1502	† SiliconG	
			SG2502	SiliconG	
			SG3502	SiliconG	
			SG4501	SiliconG	
± 42	± 0.01	100	XR4194M	† Exar	
		200	MCE4194	MCE	
			RC4194	Raytheon	
			RM4194	† Raytheon	
			SG4194	† SiliconG	
			SG4194C	SiliconG	
Switching Regulators					
Switching Regulator Circuits			**AM6301**	**AMD**	**(3315)**
			XR1524	**† Exar**	**(3381)**
			XR1525A	**† Exar**	**(3381)**
			XR1527A	**† Exar**	**(3381)**
			XR2230	Exar	
			XR2235	Exar	
			XR2524	**Exar**	**(3381)**
			XR2525A	**Exar**	**(3381)**
			XR2527A	**Exar**	**(3381)**
			XR3524	**Exar**	**(3381)**
			XR3525A	**Exar**	**(3381)**
			XR3527A	**Exar**	**(3381)**
			XR494	**Exar**	**(3380)**
			XR495	**Exar**	**(3380)**
			SH1605A	Fairchild	
			μA494	Fairchild	
			μA494M	† Fairchild	
			μA78S40	Fairchild	
			μA78S40M	† Fairchild	
			ZN1060E	† Ferranti	
			ZN1066E	Ferranti	
			ZN1066J	† Ferranti	
			MB3759	Fujitsu	
			MB3760	Fujitsu	
			LAS3800	Lambda	
			LAS3820	Lambda	
			LAS3840	Lambda	
			LAS6300	Lambda	
			LAS6300L	Lambda	
			LAS6301	Lambda	
			LAS6302	Lambda	
			LAS6330	Lambda	
			LAS6331	Lambda	
			LAS6332	Lambda	
			MC33063	**Motorola**	**(3533)**
			MC34060	**Motorola**	**(3533)**
			MC34063	**Motorola**	**(3533)**
			MC3420	**Motorola**	**(3533)**
			MC35060	**Motorola**	**(3533)**
			MC35063	**† Motorola**	**(3533)**
					(Continued)

Output Voltage Hi	Low	Output Current	Device	Source	
Switching Regulator Circuits					(Cont'd)
			MC3520	**† Motorola**	**(3533)**
			SG1525A	**† Motorola**	**(3533)**
			SG1526	**Motorola**	**(3533)**
			SG1527A	**† Motorola**	**(3533)**
			SG2525A	**Motorola**	**(3533)**
			SG2526	**Motorola**	**(3533)**
			SG2527A	**Motorola**	**(3533)**
			SG3525A	**Motorola**	**(3533)**
			SG3526	**Motorola**	**(3533)**
			SG3527A	**Motorola**	**(3533)**
			TL494C	**Motorola**	**(3533)**
			TL494M	**† Motorola**	**(3533)**
			TL495C	**Motorola**	**(3533)**
			TL495M	**† Motorola**	**(3533)**
			μA78S40	Motorola	
			LH1605	† National	
			LH1605C	National	
			LM1524	† National	
			LM2524	National	
			LM3524	National	
			RC4191	**Raytheon**	**(3588)**
			RC4192	**Raytheon**	**(3588)**
			RC4193	**Raytheon**	**(3576,3588)**
			RM4191	† Raytheon	
			RM4192	† Raytheon	
			RM4193	Raytheon	
			CA1524	**† RCA**	**(3602)**
			CA2524	**RCA**	**(3602)**
			CA3524	**RCA**	**(3602)**
			TDA4600-2	Siemens	
			TDA4700	Siemens	
			TDA4700A	Siemens	
			TDA4718	Siemens	
			TDA4718A	Siemens	
			NE5560	**Signetics**	**(3652)**
			NE5561	Signetics	
			SE5560	**† Signetics**	**(526,3652)**
			SE5561	† Signetics	
			SG3524	**Signetics**	**(3661)**
			SG1524	† SiliconG	
			SG1525A	† SiliconG	
			SG1526	† SiliconG	
			SG1527A	† SiliconG	
			SG2524	SiliconG	
			SG2525A	SiliconG	
			SG2526	SiliconG	
			SG2527A	SiliconG	
			SG3524	SiliconG	
			SG3525A	SiliconG	
			SG3526	SiliconG	
			SG3527	SiliconG	
			SG3527A	SiliconG	
			PWM125A	**† Siliconix**	**(3081)**
			PWM125C	**Siliconix**	**(3081)**
			PWM127	**Siliconix**	**(3081)**
			PWM127A	**† Siliconix**	**(3081)**
			PWM127C	**Siliconix**	**(3081)**
			PWM25A	**† Siliconix**	**(3081)**
			PWM25C	**Siliconix**	**(3081)**
			PWM27A	**† Siliconix**	**(3081)**
			PWM27C	**Siliconix**	**(3081)**
			ULN-8126	Sprague	
			ULN-8160	Sprague	
			ULN-8161	Sprague	
			ULQ-8126	Sprague	
			ULS-8126	† Sprague	
			ULS-8160	† Sprague	
			MC34060	TI	
			SG1524	† TI	
					(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

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LINEAR–Voltage Regulators (Cont'd)

Switching Regulators (Cont'd)

Output Voltage Hi	Low	Output Current	Device	Source	Page
Switching Regulator Circuits					(Cont'd)
			SG2524	TI	
			SG3524	TI	
			SG3525A	TI	
			SG3527A	TI	
			TL493C	TI	
			TL494C	TI	
			TL494M	† TI	
			TL495C	TI	
			TL497AC	TI	
			TL497AM	† TI	
			TL593C	**TI**	**(541)**
			TL594C	**TI**	**(541)**
			TL594M	**† TI**	**(541)**
			TL595C	TI	
			TEA1001	Thomson-CSF	
			UAA4001	Thomson-CSF	
			UAA4003	Thomson-CSF	
			UAA4006	Thomson-CSF	
			PIC600	Unitrode	
			PIC601	Unitrode	
			PIC602	Unitrode	
			PIC610	Unitrode	
			PIC611	Unitrode	
			PIC612	Unitrode	
			PIC625	Unitrode	
			PIC626	Unitrode	
			PIC627	Unitrode	
			PIC635	Unitrode	
			PIC636	Unitrode	
			PIC637	Unitrode	
			PIC645	Unitrode	
			PIC646	Unitrode	
			PIC647	Unitrode	
			PIC655	Unitrode	
			PIC656	Unitrode	
			PIC657	Unitrode	
			PIC660	Unitrode	
			PIC661	Unitrode	
			PIC662	Unitrode	
			PIC670	Unitrode	
			PIC671	Unitrode	
			PIC672	Unitrode	
			PIC730	Unitrode	
			PIC740	Unitrode	
			PIC800	Unitrode	
			PIC801	Unitrode	
			PIC810	Unitrode	
			PIC811	Unitrode	
			UC1524	**Unitrode**	**(3709)**
			UC1524A	**Unitrode**	**(3709,3709)**
			UC1525A	**Unitrode**	**(3709)**
			UC1526	**Unitrode**	**(3709)**
			UC1527A	**Unitrode**	**(3709)**
			UC1535	Unitrode	
			UC1840	**Unitrode**	**(3709)**
			UC1842	**† Unitrode**	**(3709)**
			UC2524	Unitrode	
			UC2524A	Unitrode	
			UC2525A	Unitrode	
			UC2526	Unitrode	
			UC2527A	Unitrode	
			UC2840	Unitrode	
			UC2842	Unitrode	
			UC3524	Unitrode	
			UC3524A	Unitrode	
			UC3525A	Unitrode	
			UC3526	Unitrode	
			UC3527A	Unitrode	

(Continued)

Output Voltage Hi	Low	Output Current	Device	Source	Page
Switching Regulator Circuits					(Cont'd)
			UC3840	Unitrode	
			UC3842	Unitrode	
			UC493A	**† Unitrode**	**(3709)**
			UC493AC	**Unitrode**	**(3709)**
			UC494A	**† Unitrode**	**(3709)**
			UC494AC	**Unitrode**	**(3709)**
			UC495	**Unitrode**	**(3709)**
			UC495A	**† Unitrode**	**(3709)**
			UC495AC	**Unitrode**	**(3709)**
			UC495B	**† Unitrode**	**(3709)**
			UC495BC	**Unitrode**	**(3709)**

† Military Temperature Range (−55° to 125°C)

* Typical Value

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Master Selection Guide

Other Linear Devices

Function	Device	Source	Page
AC Amplifier, Quad, Single Supply	CA3048	† RCA	
AC Detector (Detects presence or absence of arc signals, includes adjustable threshold and time delay.)	3050	Intech	
AC Motor Speed Control	TDA1285	Motorola	
AC Phase Control	TEA1087	Telefunken	
	U111	Telefunken	
Active Filter, Resistor Programmable	R5621	Reticon	
	R5622	Reticon	
Active Filter, Universal	R5620	Reticon	
Active Filters (See also Linear - Telecommunications Circuits)	**ATF76**	**Burr-Brown**	**(2852)**
	UAF11	**Burr-Brown**	**(2852)**
	UAF11H	**† Burr-Brown**	**(2852)**
	UAF21	**Burr-Brown**	**(2852)**
	UAF21H	**† Burr-Brown**	**(2852)**
	UAF31	**Burr-Brown**	**(2852)**
	UAF41	**Burr-Brown**	**(2852)**
	CH1290	Cermetek	
	CH1295	Cermetek	
	CH1296	Cermetek	
	FLT-U2	**Datel**	**(2865)**
	FLT-U2M	**Datel**	**(2865)**
	AF100	† National	
	AF150	National	
	AF151	National	
	MF10	National	
	MF4	**National**	**(3541)**
	MF5	National	
	MF6	National	
	R5621	Reticon	
	R5622	Reticon	
ADC Subsystem, 5 1/2 Digit, Quad Slope Integrating	**AD7555**	**AD**	**(2838)**
Air Flow Sensor	SG3509	SiliconG	
Air-Core Meter Driver	LM1819	National	
Alarm Circuit (Single chip detector/alarm system)	**CA3164E**	**RCA**	**(3604)**
Alarm Circuits, Temperature	3030	Intech	
Alarm Circuits, Tone Alarm (Comparator with AC output)	3010	Intech	
Alarm Circuits, Tri-state Alert/Alarm (LED Driver)	3020	Intech	
Analog Memory, Triple (three analog outputs which can be stepped up or down)	S175	Siemens	
Analog Multiplexer, 16-Bit, Parallel-In, Serial Out	CCD16MUX	MicroTech	
Analog Multiplexer, 16-Bit, Serial-In, Parallel-Out	CCD16DMUX	MicroTech	
Analog Shift Register (Bucket Brigade Device) Dual 512 stage, acts as a variable delay line in the audio frequency range)	MN3001	Panasonic	
	MN3010	Panasonic	
Analog Shift Register (Bucket Brigade Device) (Dual 64 stage, acts as a variable delay line in the audio range)	**MN3003**	**Panasonic**	**(3559)**
Analog Shift Register (Bucket Brigade Device, 1024 stage)	**MN3007**	**Panasonic**	**(3559)**
	MN3204	Panasonic	
	MN3207	Panasonic	
Analog Shift Register (Bucket Brigade Device, 128 Stage)	MN3006	Panasonic	
Analog Shift Register (Bucket Brigade Device, 2048 stage)	**MN3008**	**Panasonic**	**(3559)**
Analog Shift Register (Bucket Brigade Device, 256 Stage)	**MN3009**	**Panasonic**	**(3559)**
Analog Shift Register (Bucket Brigade Device, 3328 stage)	**MN3011**	**Panasonic**	**(3559)**
Analog Shift Register (Bucket Brigade Device) (3,5,190 stages)	**MN3012**	**Panasonic**	**(3559)**
Analog Shift Register (Bucket Brigade Device, 4096 stage)	**MN3005**	**Panasonic**	**(3559)**
Analog Shift Register (Bucket Brigade Device, 512 stage)	**MN3002**	**Panasonic**	**(3559)**
	MN3004	**Panasonic**	**(3559)**
	TDA1022	Signetics	
Analog Shift Register Clock Generator/Driver	MN3101	Panasonic	
Analog Shift Register (Quad 64 stage)	CCD64	MicroTech	
Analog Shift Register (185 stage, 190x2 stage)	S10110	AMI	
Analog Shift Register (256 stage)	CCD256SERP	MicroTech	
	CCD256SPS	MicroTech	
Analog Signal Processor - contains two transconductance amplifiers, two current-mode switches, output voltage buffer amplifier, and precision comparator	GAP-01A	PMI	
	GAP-01B	† PMI	
	GAP-01E	PMI	
	GAP-01F	PMI	
Attenuator	AN829	Panasonic	
Attenuator, Dual	AN829S	Panasonic	
Attenuator, 3 1/2-Digit BCD, digitally controlled	AD7525K	AD	
	AD7525T	† AD	
	MP7525B	MicroPwr	
	MP7525K	MicroPwr	
	MP7525T	MicroPwr	
Automotive Lamp Monitor	ULN-2435A	Sprague	
	ULN-2445A	Sprague	
	ULN-2455A	Sprague	
Balanced Mixer	TL442M	TI	
Balanced Modulator/Demodulator	**AD630**	**AD**	**(3361)**
	MC1496	Motorola	
	MC1596	† Motorola	
	LM1496	National	
	LM1596	† National	
	AN610	Panasonic	
	AN612	Panasonic	
	SL640C	Plessey	
	SL641C	Plessey	
	LS025	SGS	
(Continued)			
Balanced Modulator/Demodulator (Cont'd)	S042	Siemens	
	MC1496	Signetics	
	MC1596	† Signetics	
	TCA240	Signetics	
	TDA0820T	Signetics	
	SG1496	SiliconG	
	SG1596	SiliconG	
	TA7320	Toshiba	
Blowout Resistant Transistor (simulates 40 V transistor with special protection)	LM195	† National	
	LM295	National	
	LM395	National	
Comparator, Cache Address	**TMS2150-4**	**TI**	**(4222)**
	TMS2150-5	**TI**	**(4222)**
	TMS2150-7	**TI**	**(4222)**
	TMS2150-9	**TI**	**(4222)**
Comparator, Drives Lamps, Relays or Logic Loads	**4082/03**	**Burr-Brown**	**(2852)**
Comparator, Window (Internally set limits)	MK104	AnalogSys	
	4115/04	**Burr-Brown**	**(2852)**
Comparators, Programmable with Memory (High/Low Comparator)	**CA3098**	**† RCA**	**(3599)**
	CA3099	**† RCA**	**(3599)**
Constant Current Source, 1 μA to 10 mA	LM134	† National	
	LM234	National	
	LM334	National	
Control Circuit for Switched-Mode Power Supply	TEA1039	Signetics	
Coordinate Converter (polar to cartesian)	5090A	OEI	
CRT Geometry/Focus Corrector	C310	Intronics	
	C311	Intronics	
	C312	Intronics	
	C410	† Intronics	
	C411	† Intronics	
CRT Vertical Countdown	SN76566	TI	
Current Mirror, Adjustable Ratio NPN	TL010	TI	
Current Sensing Latch	SG1549	† SiliconG	
	SG2549	SiliconG	
	SG3549	SiliconG	
Current Sensing Latch, Triple	HA-23551	† Harris	
Current Source, Programmable	MJ335	AnalogSys	
Current Source, 4-Bit	9650	Fairchild	
Current-Mode PWM Controller	**UC1846**	**† Unitrode**	**(3709)**
	UC1847	**† Unitrode**	**(3709)**
	UC2846	Unitrode	
	UC2847	Unitrode	
	UC3846	Unitrode	
	UC3847	Unitrode	
Data Acquisition Controller for A/D Converter (ASCII Output)	CY600	Cybernetic	
Data Acquisition System, front end. Multiplexer, instrumentation amp (digitally programmable) and sample/hold	**HI5900-2**	**† Harris**	**(2975)**
	HI5900-5	**Harris**	**(2975)**

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

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LINEAR–Other Devices (Cont'd)

Other Linear Devices (Cont'd)

Function	Device	Source	Page
Data Acquisition System front end. 16 pseudo-differential/single ended input channels.	**HI5901-2**	† **Harris**	(2977)
	HI5901-5	**Harris**	(2977)
Data Acquisition System, 6 Channel, Sample/Hold, Pulse Width Output	μA9708	Fairchild	
Data Acquisition System, 8 Channel Differential, Sample/Hold, 12-Bit Conversion	**HDAS-8MC**	**Datel**	(2861)
	HDAS-8MM	† **Datel**	(2861)
Data Acquisition System, 8 Channel Differential, 16 Channel Single Ended, Sample/Hold, 12-Bit Conversion (2 device set)	AD363K	AD	
	AD363S	† AD	
	AD364J	**AD**	(2846)
	AD364K	**AD**	(2846)
	AD364S	† **AD**	(2846)
	AD364T	† **AD**	(2846)
Data Acquisition System, 8 Channel (expandable), Sample/Hold, 8-Bit Conversion	**MN7120**	**MicroNet**	(3042)
	MN7120H	† **MicroNet**	(3042)
Data Acquisition System, 8 Channel, Sample/Hold, 12-Bit A/D	**MN7140**	**MicroNet**	(3042)
	MN7140H	† **MicroNet**	(3042)
Data Acquisition System, 8 Channel, 8-Bit Conversion	ADC0808	National	
	ADC0809	National	
Data Acquisition System, 8 Channel, 8-Bit Conversion, Microprocessor Compatible	**AD7581A**	**AD**	(2838)
	AD7581B	**AD**	(2838)
	AD7581C	**AD**	(2838)
	AD7581J	**AD**	(2838)
	AD7581K	**AD**	(2838)
	AD7581L	**AD**	(2838)
	MP75815	† MicroPwr	
	MP7581A	**MicroPwr**	(3046)
	MP7581B	**MicroPwr**	(3046)
	MP7581C	**MicroPwr**	(3046)
	MP7581J	**MicroPwr**	(3046)
	MP7581K	**MicroPwr**	(3046)
	MP7581L	**MicroPwr**	(3046)
	MP7581T	† **MicroPwr**	(3046)
	MP7581U	† **MicroPwr**	(3046)
	SI520	**Siliconix**	(3083)
	TL520	TI	
Data Acquisition System, 8-Channel, 12-Bit A/D Converter with Reference, Clock, Three-State Outputs, Microprocessor Interface	**HS9410J**	**HybridSys**	(2981)
	HS9410K	**HybridSys**	(2981)
	HS9410S/B	† **HybridSys**	(2981)
	HS9410T	† **HybridSys**	(2981)
Data Acquisition System, 12 Bit	**MN7150**	**MicroNet**	(3042)
Data Acquisition System, 16 Channel or 8 Channel Differential, 12-Bit A/D	AD362K	AD	
	AD362S	† AD	
	SDM854	**Burr-Brown**	(2849)
	SDM856	**Burr-Brown**	(2849)
	SDM856J	**Burr-Brown**	(2849)
	SDM856K	**Burr-Brown**	(2849)
	SDM857	**Burr-Brown**	(2849)
(Continued)			
Data Acquisition System, 16 Channel or 8 Channel Differential, 12-Bit A/D (Cont'd)	**SDM858**	**Burr-Brown**	(2849)
Data Acquisition System, 16 Channel, Sample/Hold, 12-Bit Conversion	**HDAS-16MC**	**Datel**	(2861)
	HDAS-16MM	† **Datel**	(2861)
Data Acquisition System, 16 Channel 8-Bit Conversion	**DAS-952R**	**Datel**	(2865)
	ADC0816C	National	
	ADC0817C	† National	
Data Acquisition System, 16 Element or 8 Channel Differential, Sample/Hold, 12-Bit Conversion	DAS5712	Intech	
Data Acquisition System, 16 Element or 8 Channel Differential, Sample/Hold, 14-Bit Conversion	DAS5714	Intech	
Data Acquisition System, 16 Element or 8 Channel Differential, Sample/Hold, 16-Bit Conversion	DAS5716	Intech	
Data Separator/Modified Frequency Modulation Encoder	TMD2010	Telmos	
DC to DC Converter: See Regulators, Switching, under Linear - Voltage Regulators.			
DC to DC Converter (12V to 5V)	A970	† Intech	
DC to DC Converter (15V to 5V)	A3069	Intech	
DC to DC Converter (±5-16V to dual outputs)	722	Burr-Brown	
DC to DC Converter (±5-16V to four outputs)	724	Burr-Brown	
Deglitcher (suppresses transients at outputs of D/A)	4902	TeledyneP	
	4902-83	TeledyneP	
Digital Gain Set, for setting gain of op-amps	**LF13006**	**National**	(3538)
	LF13007	**National**	(3538)
Divider (See also Multipliers/Dividers below.)	AD535J	AD	
	AD535K	AD	
	DIV100	**Burr-Brown**	(2852)
Driver, Control Circuit for Fast Switching Transistors	UAA4002	Thomson-CSF	
DVM Circuits-See Interface-Analog to Digital Converters, also Digital-Special			
Electronic Switching Circuit (for ignitions)	**CA3165**	**RCA**	(3602)
Electro-Optic Driver/Modulator	MU115	AnalogSys	
Fiber Optic Data Link	3712T/R	Burr-Brown	
	3713T/R	Burr-Brown	
	3714T	Burr-Brown	
Fiber Optic Data Link Controller	SN76333	TI	
	SN76334	TI	
Fiber Optic Detector/Preamplifier	TIED460	TI	
	TIED461	TI	
	TIED462	TI	
	TIED463	TI	
Fiber Optic Emitter	FOE380B-1	National	
	FOE380B-2	National	
Fiber Optic Receiver	FOR110	Burr-Brown	
	FOR120	Burr-Brown	
	FOR100B	National	
	FOR261F-1	National	
	FOR261F-2	National	
	FOR361B	National	
Fiber Optic Transmitter	FOT110	Burr-Brown	
	FOT114	Burr-Brown	
	FOT114-IR	Burr-Brown	
	FOT120	Burr-Brown	
	FOT180B	National	
Flasher (LED)	LM3909	National	
Fluid Detector (oscillator, balance detector)	CS166	Cherry	
	LM1830	National	
	ULN-2429A	Sprague	
Frequency Switch, Programmable	MC3344	Motorola	
Frequency to Voltage/Voltage to Frequency Converter	**VFC32**	**Burr-Brown**	(2849,2853)
	VFC3205	† Burr-Brown	
	VFC320B	**Burr-Brown**	(2849)
	VFC320S	† **Burr-Brown**	(2849)
	VFC32M	† **Burr-Brown**	(2849,2853)
	VFC42	**Burr-Brown**	(2849)
	VFC42M	† **Burr-Brown**	(2849)
	VFC52	**Burr-Brown**	(2849)
	VFC52M	† **Burr-Brown**	(2849)
	VFC62	**Burr-Brown**	(2849)
	VFC62B	**Burr-Brown**	(2849)
	VFC62C	**Burr-Brown**	(2849)
	VFC62S	† **Burr-Brown**	(2849)
	VFQ-1C	**Datel**	(2865)
	VFQ-3C	**Datel**	(2865)
	XR4151C	**Exar**	(3385)
	XR4151M	† **Exar**	(3385)
	A8400	Intech	
	A8402	Intech	
	A8404	Intech	
	MPVFC32B	MicroPwr	
	MPVFC32K	MicroPwr	
	MPVFC32S	MicroPwr	
	LM131	† National	
	LM131A	† National	
	LM231	National	
	LM231A	National	
	LM331	National	
	LM331A	National	
	RC4151	Raytheon	
	RC4152	Raytheon	
	RC4153	Raytheon	
	RM4151	† Raytheon	
	RM4152	† Raytheon	
	RM4153	† Raytheon	
	4780	TeledyneP	
	4781	TeledyneP	
	4782	TeledyneP	
	9400	TeledyneS	
(Continued)			

† Military Temperature Range (−55° to 125°C)

* Typical Value

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Master Selection Guide

LINEAR–Other Devices (Cont'd)

Other Linear Devices (Cont'd)

Function	Device	Source
Frequency to Voltage/Voltage to Frequency Converter (Cont'd)		
	9401	TeledyneS
	9402	TeledyneS
Frequency/Tone Operated Devices-See Linear-Telecommunication Circuits		
Frequency-to-Voltage Converter (precision)		
	CS2907	Cherry
	CS2917	Cherry
	LM2907	National
	LM2917	National
	L290	SGS
	L291	SGS
	L292	SGS
	L293	SGS
	4736	TeledyneP
Function Generator, D/A Controller		
	CY360	Cybernetic
Hall Effect Devices (sense magnetic field) See also Digital-Other Digital Devices		
	DN6835	**Panasonic (3558)**
	DN6837	**Panasonic (3558)**
	DN835	**Panasonic (3558)**
	UGN-3013T	Sprague
	UGN-3019	Sprague
	UGN-3030	Sprague
	UGN-3040T	Sprague
	UGN-3220S	Sprague
	UGN-3501	Sprague
	UGN-3604M	Sprague
	UGN-3605M	Sprague
	UGS-3019	† Sprague
	UGS-3030	† Sprague
	TL172C	TI
	TL173C	TI
Image Area Sensor, Linear Self-Scanning		
	RA100X100	Reticon
	RA128X128A	Reticon
	RA14X41	Reticon
	RA256X256	Reticon
	RL1024SFX	Reticon
	RL128SFX	Reticon
	RL512SFX	Reticon
Image Rotator	6125A	OEI
Image Sensor, Area, 525-Line US TV Compatible		
	TC201	TI
Image Sensor, Area, 625-Line European TV Compatible		
	TC202	TI
Image Sensor, CC Photodiode		
	CCPD128x2	Reticon
	CCPD128x4	Reticon
	CCPD128x8	Reticon
Image Sensor, Circular, Self Scanning		
	R064	Reticon
	R0720B	Reticon
Image Sensor, Linear Self Scanning		
	CCD111	Fairchild
	CCD112	Fairchild
	CCD122	Fairchild
	CCD123	Fairchild
	CCD133	Fairchild
	CCD134	Fairchild
	CCD142	Fairchild
	CCD143	Fairchild
	CCD145	Fairchild
	CCD151	Fairchild
	MEL1024K	Panasonic
	MEL1024KV	Panasonic
	MEL128	Panasonic

(Continued)

Function	Device	Source
Image Sensor, Linear Self Scanning (Cont'd)		
	MEL512KV	Panasonic
	MEL64A	Panasonic
	MEL864A	Panasonic
	MN512	Panasonic
	RA-128x128	Reticon
	RA-256x256	Reticon
	RA-32X32A	Reticon
	RA-50X50A	Reticon
	RL1024C	Reticon
	RL1024G	Reticon
	RL1024H	Reticon
	RL1024S	Reticon
	RL1024SF	Reticon
	RL128EC	Reticon
	RL128G	Reticon
	RL128L	Reticon
	RL128S	Reticon
	RL128SF	Reticon
	RL1728H	Reticon
	RL2048H	Reticon
	RL256C	Reticon
	RL256EC	Reticon
	RL256G	Reticon
	RL32WD	Reticon
	RL4096	Reticon
	RL512C	Reticon
	RL512EC	Reticon
	RL512G	Reticon
	RL512S	Reticon
	RL512SF	Reticon
	RL64A	Reticon
	RL64W	Reticon
Image Sensor, 128x1, CCD		
	TC102	TI
Image Sensor, 256x1, CCD		
	CCD111	Fairchild
	CCD112	Fairchild
Image Sensor, 488x380 Area Element, CCD		
	CCD222	Fairchild
Image Sensor, 1024x1, CCD		
	CCD133	Fairchild
	CCD134	Fairchild
Image Sensor, 1728x1, CCD		
	CCD122	Fairchild
	CCD123	Fairchild
Image Sensor, 1728x1, CCD		
	CCD121	Fairchild
	TC101	TI
Image Sensor, 2048x1, CCD		
	CCD142	Fairchild
	CCD143	Fairchild
	CCD145	Fairchild
	TC103	TI
Image Sensor, 2048x1, CCD		
	μPD792	NEC
	μPD794	NEC
	MN8027	Panasonic
Image Sensor, 3456x1, CCD		
	CCD151	Fairchild
	TC104	TI
Keyboard Interface, Capacitive		
	KB3710	GI
Level Detector, Logarithmic, 10 Step Analog		
	NSL4944	National
Level Detector, Precision, (with internal reference, schmitt trigger action)		
	CS127	Cherry
	CS401	Cherry
	CS402	Cherry

(Continued)

Function	Device	Source
Level Detector, Precision, (with internal reference, schmitt trigger action) (Cont'd)		
	CS450	Cherry
Level Detector, Precision Dual		
	CS122	Cherry
	CS129	Cherry
	CS130	Cherry
Level Detector, 12-Point (for fluorescent displays)		
	XR2276	Exar
	LC7555	Sanyo
	LC7556	Sanyo
Level Meter, Analog Input Drives a Bar of LED's		
	LB1405	Sanyo
	UAA170	Siemens
	UAA180	Siemens
Light Activated Switch		
	ZNP100	Ferranti
	ZNP102	Ferranti
	ZNP103	Ferranti
	ULN-3330Y	Sprague
Light Detector (with buffer amplifier)		
	U123	Telefunken
Light Sensor	ULN-3310	Sprague
Linear Filter (for sensor and control systems)		
	MF409	AnalogSys
Linear Isolator (for sensor and control systems)		
	MI900	AnalogSys
Linear Regulator, High Efficiency		
	UC1834	**† Unitrode (3710)**
	UC2834	**Unitrode (3710)**
	UC3834	**Unitrode (3710)**
Low Battery Indicator, Triggers on 3 V (for use with 3 NiCd cells)	ICM7201	Intersil
LVDT Signal Conditioner		
	NE5520	Signetics
Motor, AC Motor Control Circuit		
	HEF4752V	**Signetics (865,899)**
Motor and Solenoid Driver		
	CA3169	**RCA (3602)**
	CA3169M	**† RCA (3602)**
Motor Driver, Full Bridge		
	UDN-2952	**Sprague (3089)**
	PIC900	Unitrode
Motor Driver, Half Bridge		
	SG1635	SiliconG
	SG3635	SiliconG
	UDN-2935Z	Sprague
	UDN-2950Z	Sprague
Motor Driver, Half H		
	SN75603	TI
	SN75604	TI
Motor, Induction Motor Energy Saver (operates off 120 Vac line)	**HV1000**	**Harris (3471)**
Motor, Induction Motor Energy Saver (operates off 240 Vac line)	**HV1000A**	**Harris (3471,3471)**
Motor Speed Controller		
	MC213	AnalogSys
Motor Speed Regulator		
	LS7263	LSIComp
	TDA1085A	Motorola
	CA3228	**RCA (3602)**
Motor Speed Regulator (for small dc motors). See also Linear—Consumer Circuits.		
	MC212	AnalogSys
	CS140	Cherry
	CS175	Cherry
	CS2907	Cherry

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† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Other Devices (Cont'd)

Function	Device	Source	
Other Linear Devices (Cont'd)			
Motor Speed Regulator (for small dc motors). See also Linear—Consumer Circuits. (Cont'd)			
	CS2917	Cherry	
	µA7392	Fairchild	
	LS7263	**LSIComp**	**(803)**
	LM1014	National	
	SL440	Plessey	
	TCA900	SGS	
	TCA910	SGS	
	TCA955	Siemens	
	NE5520	**Signetics**	**(3635)**
	TDA1506	Signetics	
	SG1731	† SiliconG	
	SG2731	SiliconG	
	SG3731	SiliconG	
	EF4443	Thomson-CSF	
Motor, Stepping Motor Driver			
	TDA3717	MicroSci	
	TDA3717	Plessey	
	SAA1027	Signetics	
	UDN-2949Z	Sprague	
	TL376C	TI	
Motor, Stepping Motor Translator/Driver			
	UCN-4202A	Sprague	
	UCN-4203A	Sprague	
Multifunction Converter (generates output=(V1÷V2)			
	LH0094	National	
	LH0094C	National	
Multifunction Convertors (XY/Z)expM			
	4301	**Burr-Brown**	**(2852)**
	4302	**Burr-Brown**	**(2852)**
Multipliers	**AD539J**	**AD**	**(3362,3363)**
	AD539K	**AD**	**(3362,3363)**
	AD539S	**† AD**	**(3362,3363)**
	MM109	AnalogSys	
	XR2208	Exar	
	XR2208M	† Exar	
	XR2228	Exar	
	XR2228M	† Exar	
	A8495	Intech	
	ICL8013C	Intersil	
	ICL8013M	† Intersil	
	MC1494	Motorola	
	MC1495	Motorola	
	MC1594	† Motorola	
	MC1595	† Motorola	
	CA3091	**† RCA**	**(3604)**
	SG1402	† SiliconG	
	SG1495	SiliconG	
	SG1595	† SiliconG	
	SG2402	SiliconG	
	SG3402	SiliconG	
	TA7158	Toshiba	
Multipliers/Dividers			
	AD530J	AD	
	AD530K	AD	
	AD530L	AD	
	AD530S	† AD	
	AD531J	**AD**	**(3363)**
	AD531K	**AD**	**(3363)**
	AD531L	**AD**	**(3363)**
	AD531S	**† AD**	**(3363)**
	AD532J	**AD**	**(3363)**
	AD532K	**AD**	**(3363)**
	AD532S	**† AD**	**(3363)**
	AD533J	**AD**	**(3363)**
	AD533K	**AD**	**(3363)**
	AD533L	**AD**	**(3363)**
(Continued)			
Multipliers/Dividers (Cont'd)			
	AD533S	**† AD**	**(3363)**
	AD534J	**AD**	**(3363)**
	AD534K	**AD**	**(3363)**
	AD534L	**AD**	**(3363)**
	AD534S	**† AD**	**(3363)**
	AD534T	**† AD**	**(3363)**
	4203	**Burr-Brown**	**(2852)**
	4203S	**† Burr-Brown**	**(2852)**
	4204	**Burr-Brown**	**(2852)**
	4204S	**† Burr-Brown**	**(2852)**
	4205	**Burr-Brown**	**(2852)**
	4205S	**† Burr-Brown**	**(2852)**
	4206	**Burr-Brown**	**(2852)**
	4213	**Burr-Brown**	**(2852,2853)**
	4213S	**† Burr-Brown**	**(2852,2853)**
	4213U	**Burr-Brown**	**(2852,2853)**
	4213V	**Burr-Brown**	**(2852,2853)**
	4213W	**Burr-Brown**	**(2852,2853)**
	4214	**Burr-Brown**	**(2852)**
	4214M	**† Burr-Brown**	**(2852)**
	MPY100	Burr-Brown	
	MPY100A	Burr-Brown	
	MPY100S	† Burr-Brown	
	RC4200	Raytheon	
	RC4200A	Raytheon	
Noise Generator (psuedo-ramdom sequence generator for audio)	S2688	AMI	
	MM5837	National	
Oscillator, Crystal Clock (250 kHz to 60 MHz)			
	CK1100A	Solarise	
	CK1114A	Solarise	
	CK1144A	Solarise	
	CK1145A	Solarise	
Oscillator, Fixed Frequency (10 Hz to 20 kHz)			
	4023	**Burr-Brown**	**(2852)**
	4025	**Burr-Brown**	**(2852)**
Oscillator, Quadrature			
	4423	**Burr-Brown**	**(2852)**
Overvoltage Protector			
	L20V12	Lambda	
	L20V15	Lambda	
	L20V18	Lambda	
	L20V20	Lambda	
	L20V24	Lambda	
	L20V5	Lambda	
	L20V6	Lambda	
	L20V9	Lambda	
	L60V12	Lambda	
	L60V15	Lambda	
	L60V24	Lambda	
	L60V28	Lambda	
	L60V5	Lambda	
	L60V6	Lambda	
	MC3423	Motorola	
	MC3523	† Motorola	
(Continued)			
Overvoltage Protector (Cont'd)			
	SG1542	† SiliconG	
	SG2542	SiliconG	
	SG3423	SiliconG	
	SG3423A	SiliconG	
	SG3523	† SiliconG	
	SG3523A	† SiliconG	
	SG3542	SiliconG	
	MC3423	TI	
Peak Detector (senses and holds peak)			
	4085	**Burr-Brown**	**(2852)**
	4085M	**† Burr-Brown**	**(2852)**
	5006	OEI	
	5030A	OEI	
	5032A	OEI	
	5902	† OEI	
	PKD-01	PMI	
PIN Diode Driver			
	DH0035	† National	
	DH0035C	National	
	UDS-5790H	† Sprague	
	UDS-5791H	† Sprague	
Potentiometer, Dual Double			
	TDA1074A	Signetics	
Potentiometer, 3 1/2-Digit BCD			
	AD7525K	**AD**	**(2827,2829)**
	AD7525L	**AD**	**(2827,2829)**
	AD7525T	**† AD**	**(2827,2829)**
	AD7525U	**† AD**	**(2827,2829)**
Power Control Subsystem			
	AM6300	**AMD**	**(3312)**
Power Control Zero Voltage Switch			
	SL445A	Plessey	
Power Supply Control (voltage reference, over and under voltage sensing)			
	XR1543	**Exar**	**(3382)**
	XR2543	**Exar**	**(3382)**
	XR3543	**Exar**	**(3382)**
	SG1543	† SiliconG	
	SG1544	† SiliconG	
	SG2543	SiliconG	
	SG2544	SiliconG	
	SG3543	SiliconG	
	SG3544	SiliconG	
	UC1543	**† Unitrode**	**(3710)**
	UC1544	**† Unitrode**	**(3710)**
	UC1901	**† Unitrode**	**(3710)**
	UC1903	**† Unitrode**	**(3710)**
	UC2543	**Unitrode**	**(3710)**
	UC2544	**Unitrode**	**(3710)**
	UC2901	**Unitrode**	**(3710)**
	UC2903	**Unitrode**	**(3710)**
	UC3543	**Unitrode**	**(3710)**
	UC3544	**Unitrode**	**(3710)**
	UC3901	**Unitrode**	**(3710)**
	UC3903	**Unitrode**	**(3710)**
Power Supply Controller (voltage reference, pulse generator and timing circuitry, error amp)			
	LA5700	Sanyo	
	TL496C	TI	
Power Supply Overvoltage Sensing Circuit, Pin Programmable			
	MC34062	Motorola	
	MC35062	Motorola	
Power Supply Overvoltage Sensing Circuit, Three-Terminal			
	MC34061	Motorola	
	MC34061A	Motorola	
	MC35061	Motorola	
	MC35061A	Motorola	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Other Devices (Cont'd)

Other Linear Devices (Cont'd)

Function	Device	Source	
Power Supply Supervisory Circuit	MC3324	Motorola	
	MC3324A	Motorola	
	MC3424	Motorola	
	MC3424A	Motorola	
	MC3524	Motorola	
	MC3524A	Motorola	
Power Supply Supervisory/Over-Under Voltage Protection Circuit	MC3425	Motorola	
	MC3425A	Motorola	
	MC3525	Motorola	
	MC3525A	Motorola	
Pressure Transducers, Absolute	LX04XXA	National	
	LX05XXA	National	
	LX05XXA0	National	
	LX06XXXA	National	
	LX14XXA	National	
	LX14XXAF	National	
	LX14XXAS	National	
	LX1600A	National	
	LX16XXA	National	
	LX18XXA	National	
Pressure Transducers, Backward Gage	LX0603GB	National	
	LX06XXGB	National	
	LX16XXGB	National	
	LX18XXGB	National	
Pressure Transducers, Differential	LX16XXD	National	
	LX18XXD	National	
	LX96XXD	National	
Pressure Transducers, Gage	LX06002D	National	
	LX06002G	National	
	LX06XXXD	National	
	LX16XXG	National	
	LX18XXG	National	
Programmable Quad Comparator, Micropower	LP165	National	
	LP365	National	
Proximity Detector, Electromagnetic	CS191	Cherry	
	CS209	Cherry	
Pulse-Width Modulated Controller (for motors, heaters, lamps)	MC343	AnalogSys	
Pulse-Width Modulator Control System (for switching regulators, motor-speed controllers)	**XR2230**	**Exar**	**(3382)**
Quantizer, 4-Bit (Quantizes analog voltage into 15 equally-spaced levels and outputs 4-Bit binary digital word at sampling rates up to 100 MHz.)	**AM6688**	**AMD**	**(3309)**
	AM6688L-6	**AMD**	**(3309)**
	AM6688L-7	**AMD**	**(3309)**
	AM6688L-8	**AMD**	**(3309)**
	AM6688M-6	**† AMD**	**(3309)**
	AM6688M-7	**† AMD**	**(3309)**
	AM6688M-8	**† AMD**	**(3309)**
Read Chain Data Comparator	TL712	TI	
	TL721	TI	
Reference Voltage (two terminal active circuit 1.220 V±5%)	**MP5010**	**† MicroPwr**	**(3529)**
	MP5010A	**† MicroPwr**	**(3529)**
	LM113	† National	
	LM113-1	† National	
	LM113-2	National	
	LM313	National	

(Continued)

Function	Device	Source	
Reference Voltage (two terminal active circuit 1.220 V±5%) (Cont'd)	9491AM	† TeledyneS	
	9491B	TeledyneS	
	9491BM	TeledyneS	
Reference Voltage (two terminal active circuit) 1.235 V±2%	LM185-1	† LinearTech	
	LM385-1	LinearTech	
	LT1004C	LinearTech	
	LT1004M	† LinearTech	
	LM285-1	**Motorola**	**(3535)**
	LM385-1	**Motorola**	**(3535)**
	LM385B-1	**Motorola**	**(3535)**
	LM185	† National	
	LM285	National	
	LM385	National	
Reference Voltage (two terminal active circuit) 1.8 to 5.6 V	LM103	† National	
Reference Voltage, 1.23 V	**AD589J**	**AD**	**(2842)**
	AD589K	**AD**	**(2842)**
	AD589L	**AD**	**(2842)**
	AD589M	**AD**	**(2842)**
	AD589S	**† AD**	**(2842)**
	AD589T	**† AD**	**(2842)**
	AD589U	**† AD**	**(2842)**
	ICL8069	**Intersil**	**(3521)**
	ICL8069M	**† Intersil**	**(3521)**
	LM185-1	† National	
	LM285-1	National	
	LM385-1	National	
Reference Voltage, 1.26 V (two terminal active circuit)	ZN423	Ferranti	
Reference Voltage, 2.45 V (two terminal active circuit)	VR-182A	Datel	
	VR-182B	Datel	
	VR-182C	Datel	
	ZN404	Ferranti	
	ZN458	Ferranti	
	ZN458A	Ferranti	
	ZN458B	Ferranti	
Reference Voltage, 2.5 V	**AD1403**	**AD**	**(2842)**
	AD1403A	**AD**	**(2842)**
	AD580J	**AD**	**(2842)**
	AD580K	**AD**	**(2842)**
	AD580L	**AD**	**(2842)**
	AD580S	**† AD**	**(2842)**
	AD580T	**† AD**	**(2842)**
	AD580U	**† AD**	**(2842)**
	AD584	**AD**	**(2842)**
	LM136-2	† LinearTech	
	LM336-2	LinearTech	
	LM385-2	LinearTech	
	LT1004C-2	LinearTech	
	LT1004M-2	† LinearTech	
	LT1009C-2	LinearTech	
	LT1009M-2	† LinearTech	
	MP5540	MicroPwr	
	LM285-2	**Motorola**	**(3535)**
	LM385-2	**Motorola**	**(3535)**
	LM385B-2	**Motorola**	**(3535)**
	MC1400-2	**Motorola**	**(3534)**
	MC1400A-2	**Motorola**	**(3534)**
	MC1403	**Motorola**	**(3535)**
	MC1403A	**Motorola**	**(3535)**
	MC1500-2	**† Motorola**	**(3534)**
	MC1500A-2	**† Motorola**	**(3534)**
	MC1503	**† Motorola**	**(3535)**
	MC1503A	**† Motorola**	**(3535)**
	LM136-2	† National	
	LM136A-2	† National	

(Continued)

Function	Device	Source	
Reference Voltage, 2.5 V (Cont'd)	LM185-2	† National	
	LM236-2	National	
	LM236A-2	National	
	LM285-2	National	
	LM336-2	National	
	LM385-2	National	
	SG1503	SiliconG	
	SG2503	SiliconG	
	SG3503	SiliconG	
	TDB0136	Thomson-CSF	
	TDC0136	† Thomson-CSF	
Reference Voltage, 2.5 V (trimmable output)	ZNREF025	Ferranti	
Reference Voltage, 2.5, 5.0, 7.5, and 10.0 V	**AD584J**	**AD**	**(2842)**
	AD584K	**AD**	**(2842)**
	AD584L	**AD**	**(2842)**
	AD584S	**† AD**	**(2842)**
	AD584T	**† AD**	**(2842)**
	AD584U	**† AD**	**(2842)**
Reference Voltage, 4 V (trimmable output)	ZNREF040	Ferranti	
Reference Voltage, 5 V	AD584	AD	
	MP5531	**† MicroPwr**	**(3529)**
	MP5541	† MicroPwr	
	MP5543	† MicroPwr	
	MPREF-02	**† MicroPwr**	**(3529)**
	MPREF-02A	† MicroPwr	
	MPREF-02C	MicroPwr	
	MPREF-02D	MicroPwr	
	MPREF-02F	MicroPwr	
	MPREF-02H	MicroPwr	
	MC1400-5	**Motorola**	**(3534)**
	MC1400A-5	**Motorola**	**(3534)**
	MC1404-5	**Motorola**	**(3535)**
	MC1500-5	**† Motorola**	**(3534)**
	MC1500A-5	**Motorola**	**(3534)**
	MC1504-5	**† Motorola**	**(3535)**
	LM136-5	† National	
	LM136A-5	† National	
	LM168-5	† National	
	LM236-5	National	
	LM236A-5	National	
	LM268-5	National	
	LM336-5	National	
	LM336B-5	National	
	LM368-5	National	
	REF-02	† PMI	
	REF-02A	† PMI	
	REF-02C	PMI	
	REF-02D	PMI	
	REF-02E	PMI	
	REF-02H	PMI	
	REF-05A	PMI	
	REF-05B	† PMI	
	REF-02	**Raytheon**	**(3585)**
	REF-02A	**Raytheon**	**(3585)**
	REF-02C	**Raytheon**	**(3585)**
	REF-02D	**Raytheon**	**(3585)**
	REF-02E	**Raytheon**	**(3585)**
	REF-02H	**Raytheon**	**(3585)**
	9495A	† TeledyneS	
	9495C	TeledyneS	
	TSC9495	TeledyneS	
Reference Voltage, 5 V (trimmable output)	ZNREF050	Ferranti	
Reference Voltage, 6.1 V (trimmable output)	ZNREF061	Ferranti	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR

Master Selection Guide

LINEAR–Other Devices (Cont'd)

Function	Device	Source		Line
Other Linear Devices (Cont'd)				
Reference Voltage, 6.2 V				
	LM168-6	† National		
	LM268-6	National		
	LM368-6	National		
Reference Voltage, 6.25 V				
	MC1400-6	Motorola	(3534)	
	MC1400A-6	Motorola	(3534)	5
	MC1404-6	Motorola	(3535)	
	MC1500-6	† Motorola	(3534)	
	MC1500A-6	† Motorola	(3534)	
	MC1504-6	† Motorola	(3535)	
Reference Voltage, 6.9 V				
	LM129	† LinearTech		10
	LM329	LinearTech		
Reference Voltage, 6.9 V Temperature Stabilized				
	LM129	† National		
	LM199	† National		
	LM199A	† National		
	LM299	National		15
	LM299A	National		
	LM329	National		
	LM399	National		
	LM3999	National		
	LM399A	National		20
	LM329	Raytheon		
Reference Voltage, 6.95 V				
	LM199	† LinearTech		
	LM399	LinearTech		
Reference Voltage, 7.5 V				
	AD584	AD		
	MP5544	MicroPwr		25
Reference Voltage, 10 V (trimmable output)				
	REF101J	Burr-Brown	(2852)	
	REF101S	† Burr-Brown	(2852)	
	ZNREF100	Ferranti		
Reference Voltage, 10 V(or -10 V)				
	AD2700J	AD	(2842)	
	AD2700L	AD	(2842)	30
	AD2700S	† AD	(2842)	
	AD2700U	† AD	(2842)	
	AD2701J	AD		
	AD2701L	AD		
	AD2701S	† AD		35
	AD2701U	† AD		
	AD2710K	AD	(2842)	
	AD2710L	AD	(2842)	
	AD2720A	AD	(2842)	
	AD2720C	AD	(2842)	40
	AD2720S	† AD	(2842)	
	AD2720T	† AD	(2842)	
	AD27720B	AD		
	AD581J	AD	(2842)	
	AD581K	AD	(2842)	45
	AD581L	AD	(2842)	
	AD581S	† AD	(2842)	
	AD581T	† AD	(2842)	
	AD581U	† AD	(2842)	
	AD584	AD		50
	REF101	Burr-Brown	(2852)	
	HSREF01	HybridSys		
	R675B-1	† HybridSys		
	R675B-4	† HybridSys		
	R675B-5	† HybridSys		55
	R675C-1	HybridSys		
	R675C-5	HybridSys		
	HC2700	HyComp		
	HC2700-883	† HyComp		
(Continued)				
Reference Voltage, 10 V(or -10 V) (Cont'd)				
	HC2701	HyComp		60
	HC2701-883	† HyComp		
	HC2710	HyComp		
	HC2710-883	† HyComp		
	HC2711	HyComp		
	HC2711-883	† HyComp		65
	MP5532	† MicroPwr	(3529)	
	MP5542	† MicroPwr		
	MP5545	† MicroPwr		
	MPREF-01	† MicroPwr	(3529)	
	MPREF-10	† MicroPwr	(3529)	70
	MC1400-10	Motorola	(3534)	
	MC1400A-10	Motorola	(3534)	
	MC1404-10	Motorola	(3535)	
	MC1404A-10	Motorola	(3535)	
	MC1500-10	† Motorola	(3534)	75
	MC1500A-10	† Motorola	(3534)	
	MC1504-10	† Motorola	(3535)	
	MC1504A-10	† Motorola	(3535)	
	LH0070	† National		
	LM168-10	† National		80
	LM268-10	National		
	LM368-10	National		
	REF-01	† PMI		
	REF-01A	† PMI		
	REF-01C	PMI		85
	REF-01D	PMI		
	REF-01E	PMI		
	REF-01H	PMI		
	REF-10A	PMI		
	REF-10B	† PMI		90
	REF-01	Raytheon	(3584)	
	REF-01A	Raytheon	(3584)	
	REF-01C	Raytheon	(3584)	
	REF-01D	Raytheon	(3584)	
	REF-01E	Raytheon	(3584)	95
	REF-01H	Raytheon	(3584)	
	TSC9496	TeledyneS		
Reference Voltage, 10.24 V				
	LH0071	National		
	LH0071-0	National		
	LH0071-1	National		100
	LH0071-2	National		
Reference Voltage, ± 10 V				
	AD2702L	AD		
	AD2702S	† AD		
	AD2702U	AD		
	AD2712K	AD		105
	AD2712L	AD		
	AD2720	AD	(2842)	
	R675B-3	† HybridSys		
	R675C-3	HybridSys		
	HC2702	HyComp		110
	HC2702-883	† HyComp		
	HC2712	HyComp		
	HC2712-883	† HyComp		
Regulator Diode with Amplifier (6.8 to 11 V)				
	MCA-series	Motorola		
Resolver and Synchro Systems				
	SDC1740	AD		115
	SDC1741	AD		
	SDC1742	AD		
	DRC10500	DDC		
	HMSDC-8700	DDC		
	HRCDX-14	DDC		120
	HRCT-14	DDC		
	HRDC-10	DDC		
	HRDC-14	DDC		
	HSCDX-14	DDC		
	HSCT-14	DDC		125
	HSDC-10	DDC		
(Continued)				
Resolver and Synchro Systems (Cont'd)				
	HSDC-14	DDC		
	HSDC-360	DDC		
	HSDC-8915	DDC		
	HSDC-8916	DDC		130
	HSDC-8917	DDC		
	HSDC-8918	DDC		
	HSDC-8919	DDC		
	HSDC-8920	DDC		
	HSDC-8921	DDC		135
	HSDC-8922	DDC		
	HXCDX-14	DDC		
	HXCT-14	DDC		
	HXDC-10	DDC		
	HXDC-14	DDC		140
	SDC-14510	DDC		
	SDC-14520	DDC		
	SDC-19100	DDC		
Resolver, Digital to Resolver Converter (DRC)				
	DRC1765	† AD		
	DRC1766	† AD		145
RMS to DC Converter				
	AD536A	AD	(3363)	
	AD536AJ	AD	(3363)	
	AD536AK	AD	(3363)	
	AD536AS	† AD	(3363)	
	AD636J	AD	(3359,3363)	150
	AD636K	AD	(3359,3363)	
	AD637J	AD	(3360,3363)	
	AD637K	AD	(3360,3363)	
	4340	Burr-Brown	(2852)	
	4341	Burr-Brown	(2852)	155
	LH0091	† National		
	LH0091C	National		
Sample and Hold Circuits				
	LF198	AMD		
	LF298	AMD		
	LF398	† AMD		160
	AD582K	AD	(2847)	
	AD582S	† AD	(2847)	
	AD583K	AD	(2847)	
	AD583S	† AD	(2847)	
	AD585J	AD	(2842,2847)	165
	AD585S	† AD	(2842,2847)	
	ADSHC-85	AD	(2847)	
	ADSHC-85E	† AD		
	ADX346	AD		
	HTC-0300	AD	(2847)	170
	HTC-0500	AD	(2845,2847)	
	HTS-0025	AD	(2847)	
	MH410	AnalogSys		
	MN245	Analogic		
	MP250M	Analogic		175
	MP260	Analogic		
	MP261	Analogic		
	MP270	Analogic		
	MP271	Analogic		
	MP272	Analogic		180
	MP282A	Analogic		
	SHC298AM	Burr-Brown	(2849)	
	SHC80	Burr-Brown	(2849)	
	SHC85	Burr-Brown	(2849)	
	SHC85ET	Burr-Brown	(2849)	185
	SHM-20C	Datel	(2864)	
	SHM-20M	† Datel	(2864)	
	SHM-6MM	† Datel	(2861)	
(Continued)				

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Other Devices (Cont'd)

Other Linear Devices (Cont'd)

Function	Device	Source
Sample and Hold Circuits (Cont'd)		
	SHM-7MC	**Datel (2864)**
	SHM-7MR	† **Datel (2864)**
	SHM-8MC	Datel
	SHM-HUMC	**Datel (2861)**
	SHM-HUMM	† Datel
	SHM-IC-1	**Datel (2864)**
	SHM-IC-1M	† Datel
	SHM-LM-2	**Datel (2864)**
	SHM-LM-2M	† Datel
	μA198	† Fairchild
	μA298	Fairchild
	μAF398	Fairchild
	HA-2420	**Harris (2955)**
	HA-2425	† **Harris (2955)**
	HA-5310	Harris
	HA-5320-2	† **Harris (2958)**
	HA-5320-5	**Harris (2958)**
	SH-8518	DDC
	ASH240	Intech
	ASH250	Intech
	ASH271	Intech
	IH5110	† Intersil
	IH5111	† Intersil
	IH5112	Intersil
	IH5113	Intersil
	IH5114	Intersil
	IH5115	Intersil
	MN343	**MicroNet (3045)**
	MN343H	† **MicroNet (3045)**
	MN344	**MicroNet (3045)**
	MN344H	† **MicroNet (3045)**
	MN346	**MicroNet (3045)**
	MN346H	† **MicroNet (3045)**
	MN347	**MicroNet (3045)**
	MN347H	† **MicroNet (3045)**
	MN375A	**MicroNet (3045)**
	MN7130	**MicroNet (3042)**
	MN7130H	† **MicroNet (3042)**
	LF198	† National
	LF198A	† National
	LF298	National
	LF298A	National
	LF398	National
	LF398A	National
	LH0023	† National
	LH0023C	National
	LH0043	† National
	LH0043C	National
	LH0053	† National
	LH0053C	National
	SHM6401	National
	μPC649	NEC
	5021	OEI
	5025	OEI
	SMP10A	† PMI
	SMP10B	† PMI
	SMP10E	PMI
	SMP10F	PMI
	SMP11A	† PMI
	SMP11B	† PMI
	SMP11E	PMI
	SMP11F	PMI
	SMP11G	PMI
	SMP81E	PMI
	SMP81F	PMI
	LF198	† Signetics
	LF298	Signetics
	LF398	Signetics
	NE5537	**Signetics (3669)**
	SE5537	† Signetics
(Continued)		
Sample and Hold Circuits (Cont'd)		
	CSH101A	† TeledyneC
	4856	TeledyneP
	4857	TeledyneP
	4860	TeledyneP
	4860-83	† TeledyneP
SCR/TRIAC Control (burst control)	L121	SGS
SCR/TRIAC Control (for push-button control)	UAA4007	Thomson-CSF
	UAA4008	Thomson-CSF
SCR/TRIAC Control (phase control)	L120	SGS
	UAA145	Telefunken
	UAA146	Telefunken
SCR/TRIAC Control, (zero voltage control)	TEA1511	Thomson-CSF
Sensor/Controller, Air Temperature	MS120	AnalogSys
Sensor/Controller, Ground Moisture and Liquid Level	MS211	AnalogSys
Sensor/Controller, Relative Humidity	MS214	AnalogSys
Sensor, Ultrasonic Object Detector (position and distance)	MS118	AnalogSys
Sequencer, 10 Outputs, 100 μs to 100 Seconds	MC116	AnalogSys
Serial Analog Delay (analog storage units with read in/read out shift register) (See also Analog Shift Registers above)	R5106	Reticon
Serial Analog Delay, Tapped (bucket brigade with 32 taps)	TAD32A	Reticon
Servo Amplifier, for Motor Control	ZN409CE	Ferranti
Servo Controller, for VTR or dc Servos	AN6880	Panasonic
	LB1601	Sanyo
Servo Controller, Proportional Control	XR2264	Exar
	XR2265	Exar
Servo Controller, Radio Controlled Cars, 2 Channel	XR2266	Exar
Signal Processor, Real Time Digital Processing of Analog Signals (programmable)	2920	Intel
	2921	Intel
Smoke Detectors: See Linear-Consumer Circuit, Miscellaneous		
Solar Transceiver	M1812	National
Stepper Motor Controller	SSI183	SiliconSys
Stepper Motor Predriver	SSI184	SiliconSys
Stepping Motor Controller/Driver, 24 V	SAA1042A	Motorola
Stepping Motor Controller/Driver, 6-12 V	SAA1042	Motorola
Switch Driver, for Power Transistors	SG1629	† SiliconG
	SG3629	SiliconG
Switched Capacitor Array	**SCA-12**	**SiliconSys (3685,4872)**
	SCA-6	**SiliconSys (3685,4872)**
Switched Capacitor Filter Array (mask programmable)	R5626	Reticon
Switches	ICL8018AC	Intersil
	ICL8018AM	† Intersil
	ICL8019AC	Intersil
	ICL8019AM	† Intersil
	ICL8020AC	Intersil
	ICL8020AM	† Intersil
Switching Regulators. See Linear-Voltage Regulators, Switching		
Tachometer: See Frequency to Voltage and Frequency Switch above		
Temperature Controlled Differential Pair	μA726C	Fairchild
	μA726M	† Fairchild
Temperature Transducers	AD590I	† AD
	AD590J	† AD
	AD590K	† AD
	AD590L	† AD
	AD590M	AD
	AD590I	† Intersil
	AD590J	† Intersil
	AD590K	† Intersil
	AD590L	† Intersil
	AD590M	† Intersil
	ICL8073	Intersil
	ICL8074	Intersil
	MMBTS102	Motorola
	MMBTS103	Motorola
	MMBTS105	Motorola
	LM134	† National
	LM135	† National
	LM234	National
	LM334	National
	LM335	National
	LM35	National
	LM3911	National
	μPC3911	NEC
	REF-02	† PMI
	REF-02A	† PMI
	REF-02C	PMI
	REF-02D	PMI
	REF-02E	PMI
	REF-02H	PMI
	LA7011	Sanyo
	TDC0134	† Thomson-CSF
	TDC0135	† Thomson-CSF
Thermal Converter (matched transistors, diffused resistors)	4131	Burr-Brown
Threshold Switch (oscillator, switch with hysteresis)	TCA105	Siemens
Threshold Switch (2/3 supply voltage)	CS560	Cherry
	TCA345	Siemens
Tone Decoder (traffic signal control and detector)	LA2200	Sanyo
Track and Hold	**HTS-0010**	**AD (2842,2847)**
	ADH-050	DDC
	ADH-051	DDC
	TH-8530	DDC
	THA05203	DDC
	MN0300A	**MicroNet (3045)**
	MN050	**MicroNet (3045)**
	MN373	**MicroNet (3045)**
	MN374	MicroNet
	MN376	**MicroNet (3045)**
	MN377	**MicroNet (3045)**
	MN379	**MicroNet (3045)**
Traffic Information Control System (ARI-DK type)	LA2211	Sanyo

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Other Devices (Cont'd)

Other Linear Devices (Cont'd)

Function	Device	Source
Transversa[illegible]ter, Quad Chirped (for discrete fourier transform [illegible]l power spectral density applications)	R5601A-1	Reticon
	R5601A-2	Reticon
Triac Angle Firing Control Circuit	TDA1185	Motorola
Undervoltage Protector/Low Voltage Monitor	CS188	Cherry
Video Delay, CCD	CCD321A	Fairchild
Voltage Converter, +5 V to ±5 V	**VI-7660C**	**Datel (2865)**
	VI-7660M	**Datel (2865)**
	ICL7660	**Intersil (3498)**
	TSC7660	**TeledyneS (3097)**
Voltage Detector, Indicator, Regulator, (programmable zener)	**ICL8211C**	**Intersil (3522,3523)**
	ICL8211M	† **Intersil (3522,3523)**
	ICL8212C	**Intersil (3522,3523)**
	ICL8212M	† **Intersil (3522,3523)**
Voltage Doubler/Inverter, Converts 4.5-20V to 9 to 40V or -4.5 to -20V.	SI7661	Siliconix
Voltage Doubler/Inverter, 1.5-10V to 3 to 20V or -1.5 to -10V.	ICL7660	Intersil
	SI7660	**Siliconix (3081)**
Voltage Level Alarm	3041	Intech
Voltage Level Alarm, Quad	3040	Intech
Voltage Overvoltage Protector. (Crowbar) See Overvoltage Protector above		
Voltage to Frequency Converter	AD537J	AD
	AD537K	AD
	AD537S	† AD
	AD650	**AD (2840)**
	ADVFG32	AD
	VFC320	**Burr-Brown (2849)**
	VFQ-1	**Datel (2865)**
	VFQ-2	**Datel (2865)**
	VFQ-3	**Datel (2865)**
	7042H	Intech
	SSM2031	SSM
	4731	† TeledyneP
	4731-83	† TeledyneP
	4732	TeledyneP
	4732-83	† TeledyneP
	4733	† TeledyneP
	4733-83	† TeledyneP
	4734	TeledyneP
	4734-83	† TeledyneP
	4735	† TeledyneP
	4735-83	† TeledyneP
	4736-83	† TeledyneP
	4739	TeledyneP
	4739-80	† TeledyneP
	4743	TeledyneP
	4743-80	† TeledyneP
	TDB0131	Thomson-CSF
Voltage to Frequency/Frequency to Voltage Converter	**AD650J**	**AD (2840)**
	AD650K	**AD (2840)**
	AD650S	† **AD (2840)**

(Continued)

Function	Device	Source
Voltage to Frequency/Frequency to Voltage Converter (Cont'd)	VFC32	Burr-Brown
	VFC32M	† Burr-Brown
	VFC42	Burr-Brown
	VFC42M	† Burr-Brown
	VFC52	Burr-Brown
	VFC52M	† Burr-Brown
	VFV-100K	Datel
	VFV-10K	Datel
	XR4151	**Exar (3385)**
	XR4151M	† Exar
	A8400	Intech
	A8402	Intech
	A8404	Intech
	MCEVFC32	MCE
	MPVFC32B	MicroPwr
	MPVFC32K	MicroPwr
	MPVFC32S	MicroPwr
	LM131	† National
	LM131A	† National
	LM231	National
	LM231A	National
	LM331	National
	LM331A	National
	RC4151	Raytheon
	RC4152	Raytheon
	RC4153	Raytheon
	RM4151	† Raytheon
	RM4152	† Raytheon
	RM4153	† Raytheon
	4780	TeledyneP
	4781	TeledyneP
	4782	TeledyneP
	9400	TeledyneS
	9401	TeledyneS
	9402	TeledyneS
Voltage Variable Gain Block	MQ328	AnalogSys
Window Discriminator (indicates voltage above, below, inside, or outside two adjustable limits)	TCA965	Siemens
Window Discriminator (indicates when input is above or below two limits)	CS180	Cherry
Zero Voltage and Zero Crossing Triggers (triac and SCR control)	TDA2090	MicroSci
	TDA2091	MicroSci
	CA3059	Motorola
	CA3079	Motorola
	MC3370	Motorola
	UAA1016A	Motorola
	UAA1016B	Motorola
	SL441	Plessey
	SL443	Plessey
	SL446	Plessey
	CA3058	† **RCA (3603)**
	CA3059	† **RCA (3603)**
	CA3079	† **RCA (3603)**
	TCA780	Siemens
	TCA280A	Signetics
	TDA1023	Signetics
	TDA1024	Signetics
	SG3059	SiliconG
	SG3079	SiliconG
	U106	Telefunken
	U217	Telefunken
	TA7606	Toshiba
Dual Over/Under-Voltage Detector	**ICL7665**	**Intersil (3513)**
Dual Transistors, Monolithic, Matched, See Linear-Arrays		

Function	Device	Source
Dual Voltage Level indicator: See Window Discriminator below		
Quad Voltage Level Monitor/Alarm (activated if any of 4 inputs differs by more than ±5, ±10 or ±20% of selected value)	ULN-2401A	Sprague
Two-Wire Bidirectional Communication System	**LM1893**	**National (3539)**

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR

Master Selection Guide

Last Page This Section. Next Page 3301

Advanced Micro Devices

LINEAR
Am6012

Distinctive Characteristics

- All grades 12-bit monotonic over temperature
- Differential nonlinearity to ±.012% (13 bits) max. over temperature
- Trimless design is inherently monotonic
- Fast settling output current: 250nsec
- Full scale current 4mA
- High output impedance and compliance: −5 to +10V
- 100% MIL-STD-883 reliability assurance testing
- Differential current outputs
- Low cost
- High-speed multiplying capability
- Direct interface to TTL, CMOS, ECL, HTL, NMOS
- Performance unchanged over supply range
- Low power consumption: 230mW
- R_{OUT}, C_{OUT} independent of logic code

GENERAL DESCRIPTION

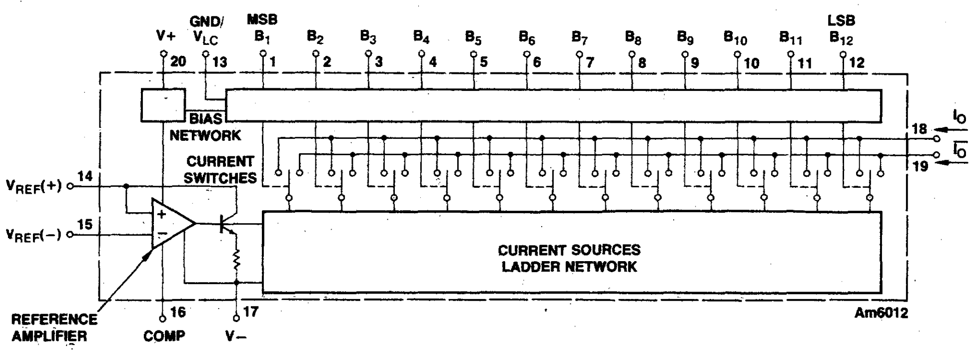
The Am6012 series of 12-bit monolithic multiplying Digital to Analog Converters represent a new level of high speed and accuracy coupled with low cost. The Am6012 is the first 12-bit D/A Converter ever built using standard processing without the requirements of thin film resistors and/or active trimming of individual devices. The Am6012 uses sophisticated new circuit design concepts that give inherent monotonicity without requiring ultra precision internal components.

The Am6012 design guarantees a more uniform step size than is possible with standard binarily weighted DAC's. This ±1/2 LSB differential nonlinearity is desirable in many applications where local linearity is critical. The uniform step size allows finer resolution of levels and in most applications is more useful than conformance to an ideal straight line from zero to full scale.

The Am6012 has high voltage compliance, high impedance dual complementary outputs which increase its versatility and enable differential operation to effectively double the peak to peak output swing. These outputs can be used directly without op amps in many applications. The dual complementary outputs can also be connected in A/D converter applications to present a constant load current and significantly reduce switching transients and increase system throughput. Output full scale current is specified at 4mA, allowing use of smaller load resistors to minimize the output RC delay which usually dominates settling time at the 12-bit level.

The Am6012 series guarantees full 12-bit monotonicity for all grades and differential nonlinearity as tight as ±.012% (13 bits) over the entire temperature range. Device performance is essentially independent of power supply voltage. The devices work over a wide operating range of +5, −12 volts to ±18 volts.

FUNCTIONAL DIAGRAM

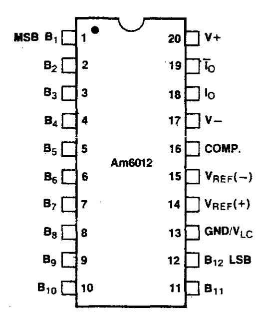


LIC-846

ORDERING INFORMATION

Order Number	Package	Temperature Range	Differential Nonlinearity
AM6012ADM	Ceramic	−55 to +125°C	±.012%
AM6012DM	Ceramic	−55 to +125°C	±.025%
AM6012ADC	Ceramic	0 to +70°C	±.012%
AM6012APC	Plastic	0 to +70°C	±.012%
AM6012DC	Ceramic	0 to +70°C	±.025%
AM6012PC	Plastic	0 to +70°C	±.025%

CONNECTION DIAGRAM – Top View



Note:
Pin 1 is marked for orientation.

LIC-847

LINEAR

Advanced Micro Devices

LINEAR
Am6012

MAXIMUM RATINGS above which useful life may be impaired

Operating Temperature		Power Supply Voltage	±18V
Am6012ADM, Am6012DM	−55 to + 125°C	Logic Inputs	−5 to +18V
Am6012ADC, Am6012DC	0 to +70°C	Analog Current Outputs	−8 to +12V
Am6012APC, Am6012PC	0 to +70°C	Reference Inputs V_{14}, V_{15}	V− to V+
Storage Temperature	−65 to +125°C	Reference Input Differential Voltage (V_{14} to V_{15})	±18V
Lead Temperature (Soldering, 60 sec)	300°C	Reference Input Current (I_{14})	1.25mA

ELECTRICAL CHARACTERISTICS

These specifications apply for $V_+ = +15V$, $V_- = -15V$, $I_{REF} = 1.0mA$, over the operating temperature range unless otherwise specified.

Parameter	Description	Test Conditions	Am6012A Min.	Am6012A Typ.	Am6012A Max.	Am6012 Min.	Am6012 Typ.	Am6012 Max.	Units
	Resolution		12	12	12	12	12	12	Bits
	Monotonicity		12	12	12	12	12	12	Bits
D.N.L.	Differential Nonlinearity	Deviation from ideal step size	–	–	±.012	–	–	±.025	%FS
			13	–	–	12	–	–	Bits
N.L.	Nonlinearity	Deviation from ideal straight line	–	–	±.05	–	–	±.05	%FS
I_{FS}	Full Scale Current	$V_{REF} = 10.000V$ $R_{14} = R_{15} = 10.000k\Omega$ $T_A = 25°C$	3.967	3.999	4.031	3.935	3.999	4.063	mA
TCI_{FS}	Full Scale Tempco		–	±5	±20	–	±10	±40	ppm/°C
			–	±.0005	±.002		±.001	±.004	%FS/°C
V_{OC}	Output Voltage Compliance	D.N.L. Specification guaranteed over compliance range R_{OUT} > 10 megohms typ.	−5	–	+10	−5	–	+10	Volts
I_{FSS}	Full Scale Symmetry	$I_{FS} - \overline{I_{FS}}$	–	±0.2	±1.0	–	±0.4	±2.0	μA
I_{ZS}	Zero Scale Current		–	–	0.10	–	–	0.10	μA
t_S	Settling Time	To ±1/2 LSB, all bits ON or OFF, $T_A = 25°C$	–	250	500	–	250	500	nsec
t_{PLH} t_{PHL}	Propagation Delay – all bits	50% to 50%	–	25	50	–	25	50	nsec
C_{OUT}	Output Capacitance		–	20	–	–	20	–	pF
V_{IL}	Logic Input Levels — Logic "0"		–	–	0.8	–	–	0.8	Volts
V_{IH}	Logic Input Levels — Logic "1"		2.0	–	–	2.0	–	–	Volts
I_{IN}	Logic Input Current	$V_{IN} = -5$ to $+18V$	–	–	40	–	–	40	μA
V_{IS}	Logic Input Swing	V− = −15V	−5	–	+18	−5	–	+18	Volts
I_{REF}	Reference Current Range		0.2	1.0	1.1	0.2	1.0	1.1	mA
I_{15}	Reference Bias Current		0	−0.5	−2.0	0	−0.5	−2.0	μA
dI/dt	Reference Input Slew Rate	$R_{14(eq)} = 800\Omega$ CC = 0pF	4.0	8.0	–	4.0	8.0	–	mA/μs
$PSSI_{FS+}$	Power Supply Sensitivity	V+ = +13.5V to +16.5V, V− = −15V	–	±.00005	±.001	–	±0.0005	±.001	%FS/%
$PSSI_{FS-}$		V− = −13.5V to −16.5V, V+ = +15V	–	±.00025	±.001	–	±.00025	±.001	%FS/%
V+	Power Supply Range	$V_{OUT} = 0V$	4.5	–	18	4.5	–	18	Volts
V−			−18	–	−10.8	−18	–	−10.8	Volts
I+	Power Supply Current	V+ = +5V, V− = −15V	–	5.7	8.5	–	5.7	8.5	mA
I−			–	−13.7	−18.0	–	−13.7	−18.0	mA
I+		V+ = +15V, V− = −15V		5.7	8.5	–	5.7	8.5	mA
I−			–	−13.7	−18.0	–	−13.7	−18.0	mA
P_D	Power Dissipation	V+ = +5V, V− = −15V	–	234	312	–	234	312	mW
		V+ = +15V, V− = −15V	–	291	397	–	291	397	mW

Advanced Micro Devices

LINEAR
Am6108 • Am6148

DISTINCTIVE CHARACTERISTICS

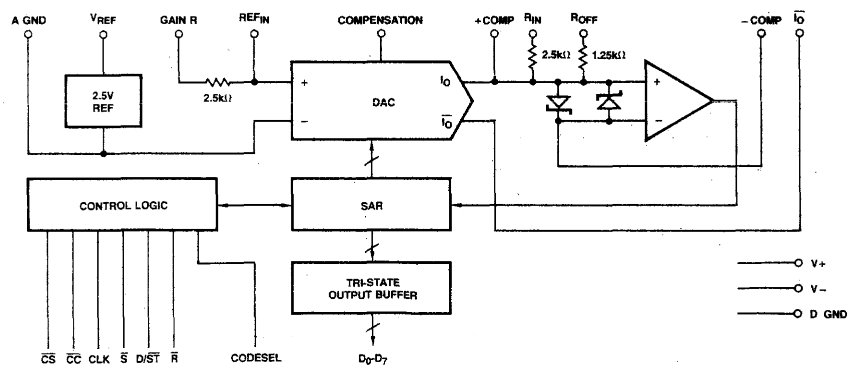
- 1μs conversion time
- Trimmed internal voltage reference
- 0.1% nonlinearity
- Ratiometric operation
- Low operating voltages
- Internal matched gain, reference and offset resistors
- Microprocessor compatible
- 3-state outputs
- Pin-programmable unipolar or bipolar two's complement conversion
- Conversion complete available as interrupt or as multiplexed output on data bus
- Available in slim, 24-pin, 0.3″ and standard, 28-pin, 0.6″ packages

FUNCTIONAL DESCRIPTION

The Am6108 and Am6148 are microprocessor-compatible, 8-bit, high-speed, analog-to-digital converters. They include a precision reference, DAC, comparator, SAR, scale resistors, 3-state output buffers and control logic. The Am6108 is available in a standard .600-inch-wide, 28-pin package, and the Am6148 is offered in a space-saving, .300-inch-wide, 24-pin package. The Am6108/Am6148 are capable of completing an 8-bit conversion in under one microsecond and can handle input voltage ranges of 0 to +10V, 0 to +5V, and ±5V without external components. With appropriate external resistors, the user can program the device to operate on other input signal ranges (2 or 3 precision resistors are required). Full 8-bit monotonic performance with no missing codes is guaranteed over temperature. Both devices have 3-state outputs for bus compatibility and a status output.

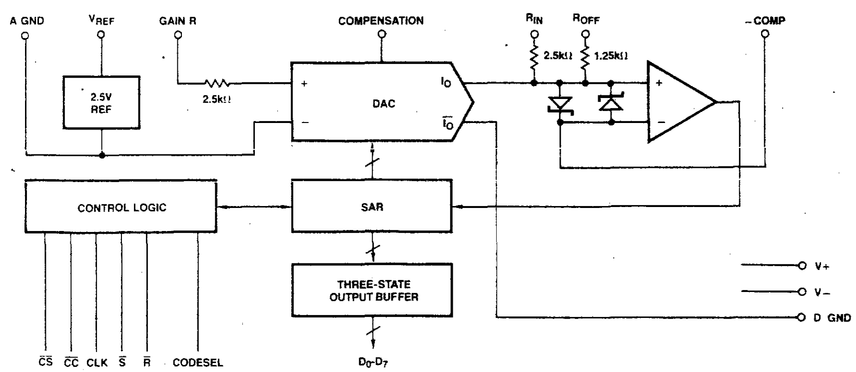
The Am6108/Am6148 are useful in microprocessor-based systems or can be used in a stand-alone mode. The conversion time is short enough to allow most microprocessors to accept data immediately after requesting a conversion. Applications include Analog I/O subsystems, process control and servo-control.

Am6108 EQUIVALENT CIRCUIT



ABI-092

Am6148 EQUIVALENT CIRCUIT



ABI-093

LINEAR

Advanced Micro Devices

Advanced Micro Devices

LINEAR

Am6108 • Am6148

MAXIMUM RATINGS above which useful life may be impaired

V+ to D GND	−0.3 to +7.0V	Voltage at GAIN R, REF_{IN}	V− to V+
V− to D GND	+0.3 to −7.0V	Voltage at R_{IN}, R_{OFF}	±12V
Max Differential V+ to V−	±12V	DAC Compliance Voltage	−2 to +12V
Digital Inputs to D GND	−0.5 to +6.0V	Operating Temperature	0 to +70°C
A GND to D GND	±1V	Storage Temperature	−65 to +150°C
V_{REF} Max Output Current	15mA	Lead Temperature (Soldering 60 sec)	300°C
Max Input Current at REF_{IN}	2mA	Minimum Operating Voltage	9.7V

ELECTRICAL CHARACTERISTICS (These specifications apply for $V^+ = +5V \pm 5\%$, $V^- = -5.2V \pm 5\%$, V_{REF} connected to GAIN R, $0°C \leq T_A \leq 70°C$ and $f_{CLOCK} = 500KHz$)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
Transfer Characteristics						
	Resolution		8	8	8	Bits
	Monotonicity		8	8	8	Bits
	Differential Nonlinearity			±1/4	±1/2	LSB
	Linearity			±1/4	±1/2	LSB
	Inherent Quantization Error				±1/2	LSB
	Unipolar Gain Error	V_{IN} = 0 to +5V		±1½	±4	LSB
		V_{IN} a= 0 to +10V		±1	±2	
	Unipolar Offset Error			±1/2	±1	LSB
	Bipolar Gain Error	V_{IN} = −5V to +5V		±1	±2	LSB
	Bipolar Offset Error			±3/4	±1½	LSB
	Positive Power Supply Sensitivity	$V^+ = +5V \pm 5\%$		0.02	0.2	%FS
	Negative Power Supply Sensitivity	$V^- = -5.2V \pm 5\%$		0.02	0.2	%FS
Internal Reference						
V_{REF}	Reference Voltage	I_{REF} = 1mA	2.485	2.5	2.515	Volts
V_{REF}/T_A	Reference Voltage Tempco			20		ppm/°C
$\Delta V_{REF}/V_{REF}$	Load Regulation	I_{REF} = 1mA to 5mA		0.05	0.2	$\%V_{REF}$
$\Delta V_{REF}/V_{REF}$	Line Regulation	$V^+ = +5V \pm 5\%$		0.05	0.2	$\%V_{REF}$
	Noise, f_n = 10KHz to 1MHz			20		μV_{rms}
Analog Inputs						
	Input Resistance					
	±5V			2.5		KΩ
	0 to 10V			2.5		KΩ
	0 to 5V			1.25		KΩ
	Input Capacitance					
	R_{IN}, R_{OFF}, REF_{IN}*, GAIN R			2		pF
	$\overline{I_O}$*			20		pF
	+COMP*			20		pF
	−COMP			2		pF
Digital Inputs						
	Logic Level Input Voltage					
V_{IH}	Logic 1		2.0			Volts
V_{IL}	Logic 0				0.8	Volts
	Logic Level Input Current					
I_{IH}	Logic 1	V_{IN} = 2.7V			40	μA
I_{IL}	Logic 0	V_{IN} = 0.4V			10	μA

*Function available on the Am6108 only.

LINEAR

Advanced Micro Devices

LINEAR
Am6108 • Am6148

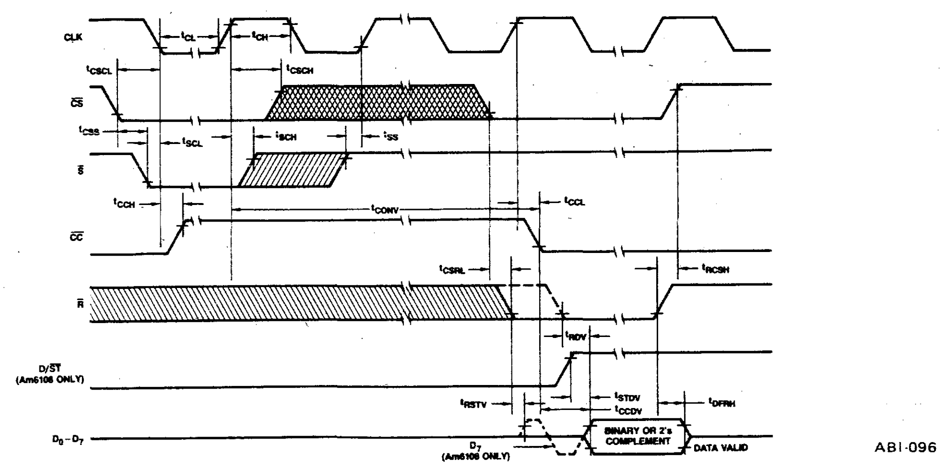
ELECTRICAL CHARACTERISTICS (Cont.)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
Digital Outputs						
	Logic Level Output Voltages					
V_{OH}	Logic 1	$I_{OH} = -400\mu A$	2.4			Volts
V_{OL}	Logic 0	$I_{OL} = 8mA$			0.5	Volts
I_{SC}	Output Short Circuit Current			−40		mA
I_{OZ}	**Off-State Output Current**					
		$V_O = 2.4V$		20		μA
		$V_O = 0.4V$		−20		μA
Power Requirements						
I^+	Positive Supply Current			44	60	mA
$I-$	Negative Supply Current			−65	−85	mA
	Power Dissipation			600	800	mW

SYSTEM TIMING

Parameters	Description	Min	Typ	Max	Units
t_{CONV}	Conversion Time		1	2	μs
t_{CSS}	$\overline{CS}$ Low to $\overline{S}$ Low	0			ns
t_{CSCL}	$\overline{CS}$ Low to CLK Low	0			ns
t_{SCL}	$\overline{S}$ Low to CLK Low	0			ns
t_{CCH}	$\overline{CC}$ High from CLK Low		35	40	ns
t_{SCH}	$\overline{S}$ High from CLK High	0			ns
t_{SS}	$\overline{S}$ High before CLK High	10			ns
t_{CSCH}	$\overline{CS}$ High from CLK High	0			ns
t_{CCL}	$\overline{CC}$ Low from CLK High	20	30	40	ns
t_{CSRL}	$\overline{CS}$ Low to $\overline{R}$ Low	0			ns
t_{RSTV}	$\overline{R}$ Low to Status Valid on D_7 (Am6108 Only)	15	30	40	ns
t_{STDV}	Status to Data Valid on D_7 (Am6108 Only)	15	30	40	ns
t_{CCDV}	$\overline{CC}$ Low to Data Valid	15	30	40	ns
t_{RDV}	$\overline{R}$ Low to Data Valid	15	30	40	ns
t_{DFRH}	Data Float from $\overline{R}$ High	20	30	40	ns
t_{RCSH}	$\overline{R}$ High to $\overline{CS}$ High	0			ns
t_{CL}	CLK Low	50			ns
t_{CH}	CLK High	50			ns

System Timing



*Function available on the Am6108 only.

Advanced Micro Devices

LINEAR
Am6112
PRELIMINARY DATA

DISTINCTIVE CHARACTERISTICS

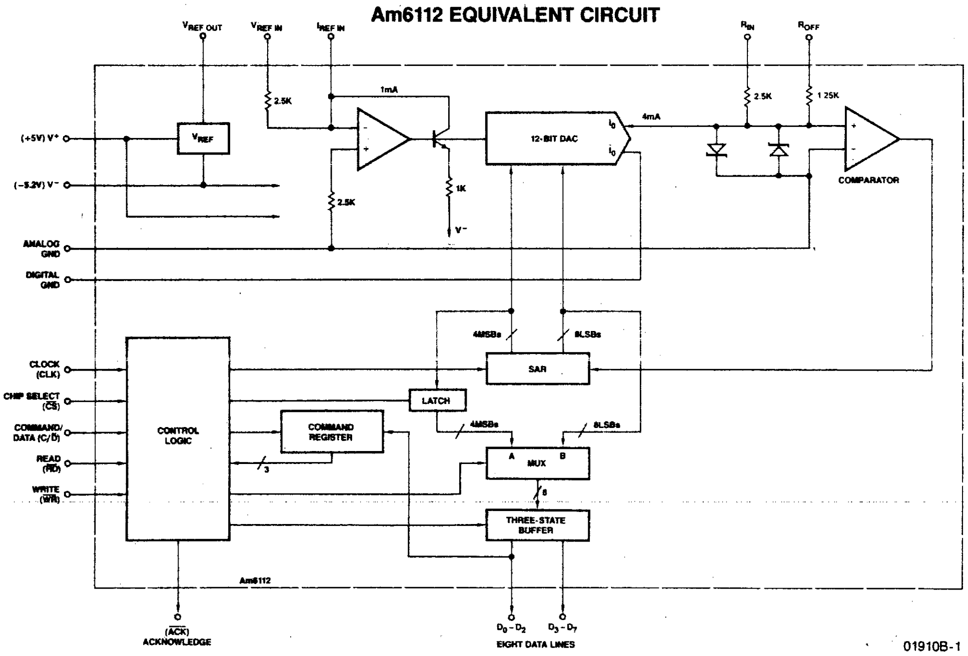
- First totally monolithic, high-speed 12-bit ADC
- 3μs typical conversion time
- Internal precision voltage reference
- No missing codes
- Easy interfacing with 8- and 16-bit microprocessors
- Internal command register for programmable modes of operation
- Offset binary or two's complement output code
- 0 to 10V, or ± 5V input range
- 24-pin package

FUNCTIONAL DESCRIPTION

The Am6112 is the first fully monolithic microprocessor compatible 12-bit high-speed analog-to-digital converter. The Am6112 high-speed A/D contains a precision reference, DAC, comparator, SAR, scale resistors, output three-state buffers and comprehensive control logic, enabling the device to be interfaced with a variety of microprocessors. The Am6112 is capable of completing a 12-bit conversion in typically three microseconds and can handle input voltage ranges of 0 to 10V, and ±5V without external components.

The Am6112 has four modes of microprocessor operation, and a stand-alone mode. These modes are software programmable, except for the stand-alone mode which is pin selectable. Applications include analog I/O subsystems, servo-control and high-speed digital signal processing of analog events.

Am6112 EQUIVALENT CIRCUIT



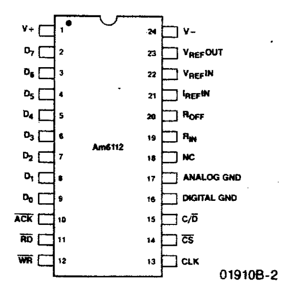
01910B-1

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type	Temperature Range
AM6112DC	Hermetic DIP	0 to +70°C
AM6112XC	Dice	0 to +70°C
AM6112DM	Hermetic DIP	−55 to +125°C

CONNECTION DIAGRAM – Top View
D-24-1



01910B-2

Note: Pin 1 is marked for orientation.

LINEAR
Am6112

ELECTRICAL CHARACTERISTICS (Cont.)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
Digital Outputs						
	Logic Level Output Voltages					
V_{OH}	Logic 1	$I_{OH} = -400\mu A$	2.4			Volts
V_{OL}	Logic 0	$I_{OL} = 8mA$			0.5	Volts
I_{SC}	Output Short Circuit Current			−40		mA
I_{OZ}	Off-State Output Current					
		$V_O = 2.4V$		20		μA
		$V_O = 0.4V$		−20		μA
Power Requirements						
I^+	Positive Supply Current			40	80	mA
I−	Negative Supply Current			−60	−80	mA
	Power Dissipation			500	800	mW

SYSTEM TIMING

Parameters	Description	Min	Typ	Max	Units
t_{CONV}	Conversion Time R_{OFF} connected to A_{GND} or $V_{REF\ OUT}$ (Bipolar)		3.3		μs
	R_{OFF} Open (Unipolar)		10		μs
t_{CL}	CLK Low		125		ns
t_{CH}	CLK High		125		ns

DEFINITION OF TERMS

Resolution: The number of possible analog input levels an A/D will resolve. Expressed as either the number of output bits, or 1 part in 2^n where n is the number of bits.

Monotonicity (Missing Codes): Monotonicity is a property of the DAC within a successive approximation ADC. Each increment in the digital code to the DAC is accompanied by an analog output that is greater than or equal to that of the proceeding code. Monotonicity of the DAC is a necessary requirement for a successive approximation ADC to have no missing codes.

Differential Nonlinearity: The deviation between the actual code width of an A/D from the ideal code width. The code width is defined as the range of analog input which produces a given digital output code. An ideal value of a code width is equivalent to FSR/2^n, where in is the number of bits.

Linearity: The deviation of each individual code from an ideal straight line transfer curve between zero and full scale, with the straight line measured from the middle of each particular code.

Inherent Quantization Error: Quantization Error is a direct consequence of the resolution of the A/D. All analog voltages within a given range are represented by a single digital output code. There is, therefore, an *inherent* ±1/2 LSB conversion error even for a perfect A/D.

Gain Error: Defined as the difference between the analog input levels required to produce the first and the last digital output code transitions. Gain error is a measure of the deviation between the actual gain from the ideal gain of FS-2 LSB.

Unipolar Offset Error: Difference between the ideal (+1/2 LSB) and the actual analog input level required to produce the first digital code transition (00 . . . . 00 to 00 . . . . 01) over the complete temperature range.

Bipolar Offset Error: Difference between the ideal (1/2 FSR − 1/2 LSB) and the actual analog input level required to produce the major carry output digital code transition (from 01 . . . . 11 to 10 . . . . 00).

Power Supply Sensitivity: A measure of the change in gain and offset of the A/D resulting from a change in supply voltage. Usually expressed in total %FS for a percentage change in supply voltage.

Conversion Time: The measure of how long it takes for the A/D to arrive at the correct digital output code. It is the time between the clock edge that starts a conversion after receiving a start command and the edge of the status line ($\overline{CC}$) which signifies that the conversion is completed.

Advanced Micro Devices

LINEAR
Am6112

MAXIMUM RATINGS above which useful life may be impaired

V+ to D GND	−0.3 to +7.0V	Voltage at R_{IN}, R_{OFF}	±12V
V− to D GND	+0.3 to −7.0V	Open Collector Current	20mA
Max Differential V+ to V−	±12V	Operating Temperature	0 to +70°C
Digital Inputs to D GND	−0.5 to +6.0V	Storage Temperature	−65 to +150°C
A GND to D GND	±1V	Lead Temperature (Soldering 60 sec)	300°C
V_{REF} Max Output Current	15mA	Minimum Operating Voltage	9.7V
Max Input Current at REF_{IN}	2mA	Max Package Dissipation	1W
Voltage at GAIN R, REF_{IN}	V− to V+		

ELECTRICAL CHARACTERISTICS (These specifications apply for $V^+ = +5V \pm 5\%$, $V^- = -5.2V \pm 5\%$, V_{REF} connected per connection diagram, $T_A = 25°C$, $F_{Clock} = 150kHz$, 0 to +10V input range, R_{OFF} open, stand-alone mode, unless otherwise stated)

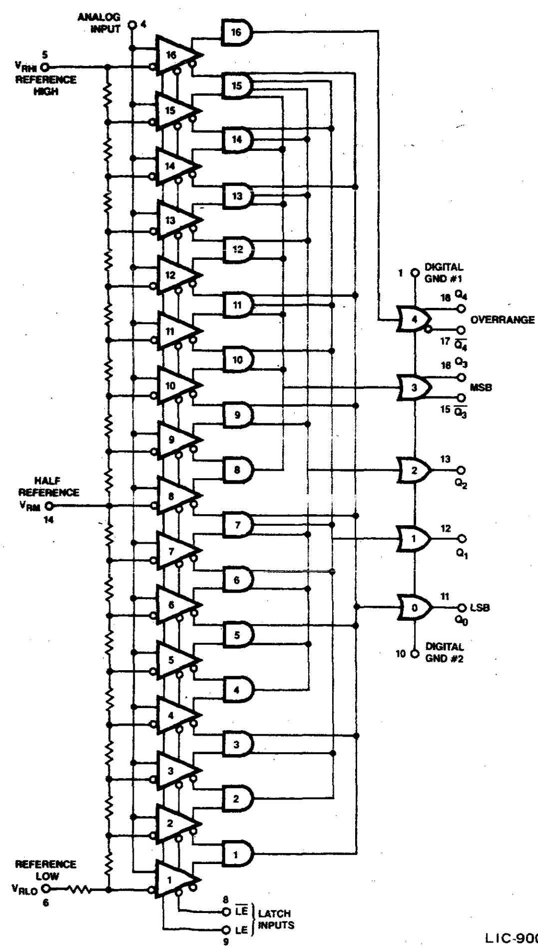
Parameters	Description	Test Conditions	Min	Typ	Max	Units
Transfer Characteristics						
	Resolution		12	12	12	Bits
	Monotonicity				12	Bits
	Differential Nonlinearity				±1	LSB
	Linearity			±1		LSB
	Inherent Quantization Error				±1/2	LSB
	Unipolar Gain Error			±2		LSB
	Unipolar Offset Error			±1/2		LSB
	Bipolar Gain Error	$V_{IN} = -5V$ to $+5V$		±4		LSB
	Bipolar Offset Error			±2		LSB
	Positive Power Supply Sensitivity	$V^+ = +5V \pm 5\%$		0.005		%FS
	Negative Power Supply Sensitivity	$V^- = -5.2V \pm 5\%$		0.005		%FS
Internal Reference						
V_{REF}	Reference Voltage	$I_{REF} = 1mA$	2.490	2.5	2.510	Volts
V_{REF}/T_A	Reference Voltage Tempco			8		ppm/°C
$\Delta V_{REF}/V_{REF}$	Load Regulation	I_{REF} = 1mA to 5mA		0.005		$\%V_{REF}$
$\Delta V_{REF}/V_{REF}$	Line Regulation	$V^+ = +5V \pm 5\%$, $-5.2 \pm 5\%$		0.005		$\%V_{REF}$
	Noise, N = 10kHz to 1MHz					μV_{RMS}
Analog Inputs						
R_{IN}	**Input Resistance**					
	±5V			2.5		KΩ
	0 to 10V			2.5		KΩ
C_{IN}	**Input Capacitance**					
	R_{IN}, R_{OFF}, REF_{IN}, GAIN R			2		pF
Digital Inputs						
	Logic Level Input Voltage					
V_{IH}	Logic 1		2.0			Volts
V_{IL}	Logic 0				0.8	Volts
	Logic Level Input Current					
I_{IH}	Logic 1	$V_{IN} = 2.7V$			40	μA
I_{IL}	Logic 0	$V_{IN} = 0.4V$			10	μA

Advanced Micro Devices

LINEAR
Am6688

Distinctive Characteristics:
- 100MHz sampling rate
- 5ns maximum encode delay
- 4-bit resolution, expansible to 8 bits
- 8-bit accuracy
- Large bipolar input voltage range
- Low input current
- Q and $\overline{Q}$ Outputs on MSB for 2's complement conversion
- 100% MIL-STD-883 reliability assurance testing

FUNCTIONAL DIAGRAM



LIC-900

FUNCTIONAL DESCRIPTION

The Am6688 4-bit quantizer consists of an array of 16 high-speed ECL sampling comparators, a resistor voltage divider, and an ECL-compatible binary encoder. It will accurately quantize an analog voltage into 15 equally-spaced levels and output a 4-bit binary digital word at sampling rates up to 100 MHz.

Resolution above 4-bits, up to a maximum of 8, may be obtained by stacking quantizers (n bits of resolution requires 2^{n-4} quantizers). An overrange output signal is provided to indicate that the input signal has exceeded the full-scale limit. This overrange output is also the enable gating signal used to encode the higher-order bits of the output in a stacked configuration.

The high speed latch enable inputs are intended to be driven from the complementary outputs of a standard ECL gate or a high-speed comparator such as the Am685. If LE is driven high and $\overline{LE}$ is driven low, the quantizer is in the sample mode and operates like a low-gain, high-bandwidth amplifier. When LE is driven low and LE is driven high, the quantizer will hold its existing digital binary output word.

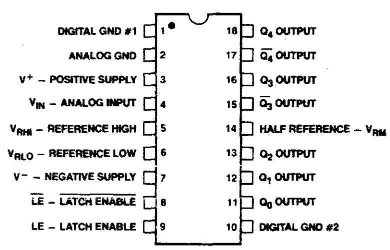
The outputs are open emitters, requiring external pull-down resistors of at least 200Ω to −2V or 500Ω to −5.2V.

These devices can be used in video data conversion and time-base correction, radar signal processing, nuclear pulse-height analysis, and other systems requiring very high-speed analog-to-digital conversion.

ORDERING INFORMATION

Order Number	Temperature Range	Maximum Error
Am6688DL-8	−30 to +85°C	±5mV
Am6688DL-7	−30 to +85°C	±10mV
Am6688DL-6	−30 to +85°C	±20mV
Am6688DM-8	−55 to +125°C	±5mV
Am6688DM-7	−55 to +125°C	±10mV
Am6688DM-6	−55 to +125°C	±20mV

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LIC-901

Advanced Micro Devices

LINEAR
Am6688

MAXIMUM RATINGS (Above which the useful life may be impaired)

Supply Voltage:	Positive	+7V
	Negative	−6V
Input Voltage:	Analog	−5V to +3V
	References	−5V to +3V
	Digital	−5V to 0V
Differential Voltage:	Analog Input to References	±6V
	Analog Gnd to Digital Gnds	±0.1V

Output Current (each output)		15mA
Temperature:	Operating, Am6688DL	−30 to +85°C
	Am6688DM	−55 to +125°C
	Storage	−65 to +150°C
	Junction	+175°C
	Lead (soldering, 60sec)	+300°C
Minimum Operating Voltage (V^+ to V^-)		10V

ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGES
(Unless otherwise specified)

DC Characteristics

Symbol	Parameter (see definitions)	Conditions (Note 1)	Am6688DL Min	Am6688DL Max	Am6688DM Min	Am6688DM Max	Units
	Resolution		4		4		Bits
V_{OS}	Error Voltage (each transition)	Am6688 − 8 − 7 − 6	−5 −10 −20	+5 +10 +20	−5 −10 −20	+5 +10 +20	mV mV mV
DNL	Differential Nonlinearity	$\Delta V_{REF} = \Delta V_{REF(min)}$	−0.5	0.5	−0.5	0.5	LSB
V_{IN}	Input Voltage		−3.3	+2.7	−3.3	+2.7	V
ΔV_{REF}	Reference Resistor Voltage ($V_{RHI}-V_{RLO}$)	Am6688 − 8 − 7 − 6	0.16 0.32 0.64	6.0 6.0 6.0	0.16 0.32 0.64	6.0 6.0 6.0	V V V
I_{REF}	Reference Current	$\Delta V_{REF} = 2.56V$	6.0	17	5.0	18	mA
I_B	Analog Input Current	$V_{IN} \geq V_{RHI}$		230		250	μA
I_L	Latch Input Current	$V_L \geq V_{OH}$		200		220	μA
V_{OH}	Output HIGH Voltage	$T_A = 25°C$ $T_A = T_{A(min)}$ $T_A = T_{A(max)}$	−0.93 −1.03 −0.86	−0.72 −0.80 −0.64	−0.93 −1.08 −0.83	−0.72 −0.83 −0.58	V V V
V_{OL}	Output LOW Voltage	$T_A = 25°C$ $T_A = T_{A(min)}$ $T_A = T_{A(max)}$	−1.90 −1.93 −1.86	−1.62 −1.65 −1.58	−1.90 −1.95 −1.84	−1.62 −1.66 −1.54	V V V
I^+	Positive Supply Current			100		100	mA
I^-	Negative Supply Current			100		100	mA
P_{DISS}	Power Dissipation	$\Delta V_{REF} = 2.56V$		1.2		1.2	W

Switching Characteristics (Note 2)

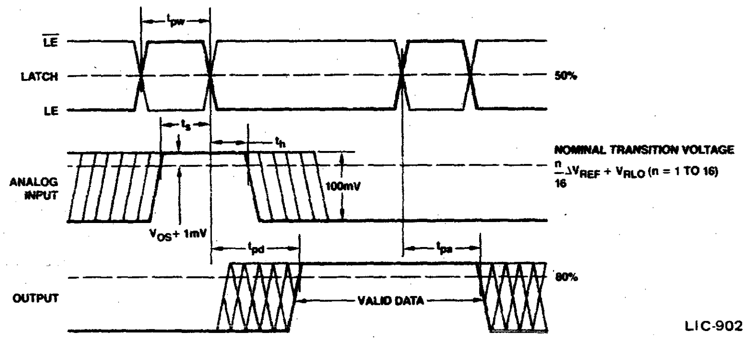
Symbol	Parameter	Conditions	Am6688DL Min	Am6688DL Max	Am6688DM Min	Am6688DM Max	Units
F_{MAX}	Maximum Sampling Frequency		100		100		MHz
t_{pw}	Minimum Sample Time			3		3	ns
t_{pd}	Encode Delay (each transition)	$T_{A(min)} \leq T_A \leq 25°C$ $T_A = T_{A(max)}$		5 6		5 8	ns ns
t_s	Minimum Set-up Time	$T_A = 25°C$		3		3	ns
t_h	Minimum Hold Time	$T_A = 25°C$		1		1	ns
t_{pa}	Analog Delay (each transition)	$T_{A(min)} \leq T_A \leq 25°C$ $T_A = T_{A(max)}$	3 4		3 4		ns ns

Notes: 1. Unless otherwise specified, $V^+ = +6.0V$, $V^- = -5.2V$, $V_{RHI} = +2.56V$, $V_{RM} = +1.28V$, $V_{RLO} = 0V$, $t_{pw} = 5ns$, and $R_L = 100\Omega$ to −2V at all outputs. The specifications given for V_{OS}, DNL, and t_{pd} apply over the full V_{IN} range and for ±5% supply voltages. The Am6688 is designed to meet the specifications given in the table after thermal equilibrium has been established with a transverse air flow of 500 LFPM or greater.

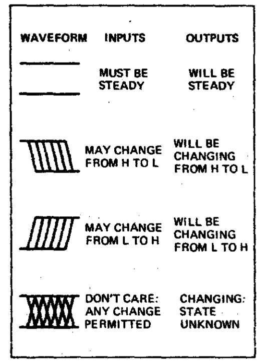
2. Switching characteristics are for a 100mV analog input pulse level-shifted at each transition point to provide an overdrive of 1mV past the maximum specified error voltage.

LINEAR
Am6688

TIMING DIAGRAM

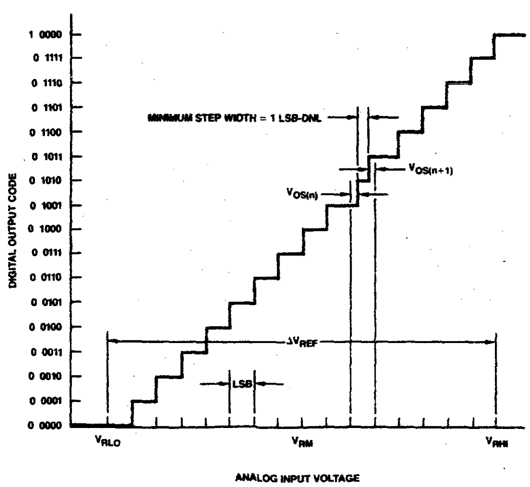


KEY TO TIMING DIAGRAM



During the sampling time, the quantizer acts like a low-gain, very wide-bandwidth linear amplifier. The gain is not high enough to hold the outputs in a stable logic state under all conditions; consequently, the outputs may be undefined during this period. The time that the outputs are unstable begins t_{pa} after the Latch Enable goes HIGH, and terminates t_{pd} after it goes LOW. It is best to minimize this time by using as narrow a sampling pulse as possible, since the possibility of oscillation due to external parasitic feedback is greater the longer the device is in the analog mode.

TYPICAL TRANSFER FUNCTION



LIC-903

TRUTH TABLE

Analog Input (relative to V_{RLO})	Q_4	Q_3	Q_2	Q_1	Q_0
$V_{IN} < \frac{1}{16}\Delta V_{REF}$	L	L	L	L	L
$\frac{1}{16}\Delta V_{REF} < V_{IN} < \frac{1}{8}\Delta V_{REF}$	L	L	L	L	H
$\frac{1}{8}\Delta V_{REF} < V_{IN} < \frac{3}{16}\Delta V_{REF}$	L	L	L	H	L
$\frac{3}{16}\Delta V_{REF} < V_{IN} < \frac{1}{4}\Delta V_{REF}$	L	L	L	H	H
$\frac{1}{4}\Delta V_{REF} < V_{IN} < \frac{5}{16}\Delta V_{REF}$	L	L	H	L	L
$\frac{5}{16}\Delta V_{REF} < V_{IN} < \frac{3}{8}\Delta V_{REF}$	L	L	H	L	H
$\frac{3}{8}\Delta V_{REF} < V_{IN} < \frac{7}{16}\Delta V_{REF}$	L	L	H	H	L
$\frac{7}{16}\Delta V_{REF} < V_{IN} \frac{1}{2}\Delta V_{REF}$	L	L	H	H	H
$\frac{1}{2}\Delta V_{REF} < V_{IN} < \frac{9}{16}\Delta V_{REF}$	L	H	L	L	L
$\frac{9}{16}\Delta V_{REF} < V_{IN} < \frac{5}{8}\Delta V_{REF}$	L	H	L	L	H
$\frac{5}{8}\Delta V_{REF} < V_{IN} < \frac{11}{16}\Delta V_{REF}$	L	H	L	H	L
$\frac{11}{16}\Delta V_{REF} < V_{IN} < \frac{3}{4}\Delta V_{REF}$	L	H	L	H	H
$\frac{3}{4}\Delta V_{REF} < V_{IN} < \frac{13}{16}\Delta V_{REF}$	L	H	H	L	L
$\frac{13}{16}\Delta V_{REF} < V_{IN} < \frac{7}{8}\Delta V_{REF}$	L	H	H	L	H
$\frac{7}{8}\Delta V_{REF} < V_{IN} < \frac{15}{16}\Delta V_{REF}$	L	H	H	H	L
$\frac{15}{16}\Delta V_{REF} < V_{IN} < \Delta V_{REF}$	L	H	H	H	H
$V_{IN} > \Delta V_{REF}$	H	L	L	L	L

Advanced Micro Devices

LINEAR
Am6300

DISTINCTIVE CHARACTERISTICS

- 2.5V ±0.25% temperature compensated reference
- Versatile 100mA output for driving external NPN or PNP power transistors
- Thermal shutdown
- Logic control power up enable
- Programmable delay and rise time for power supply
- ±5% or ±10% over/under voltage detection/protection
- Programmable current limit detection/protection
- Programmable delays for the over/under voltage and current shutdown circuits
- Status outputs for fault conditions and output state

GENERAL DESCRIPTION

The Am6300 Power Control Subsystem consists of a regulator section, an over/under voltage detection section, a current limit section and a reset and control section.

The regulator section contains a complete series pass voltage regulator with thermal shutdown, which uses external resistors to set the output voltage. Both the collector and emitter of the regulator output transistor are available to the user for flexibility in driving external power devices. The regulator also contains a precision, trimmed 2.5 volt reference which is capable of supplying 5mA of current for external purposes in addition to controlling the regulator and generating over and under voltage references.

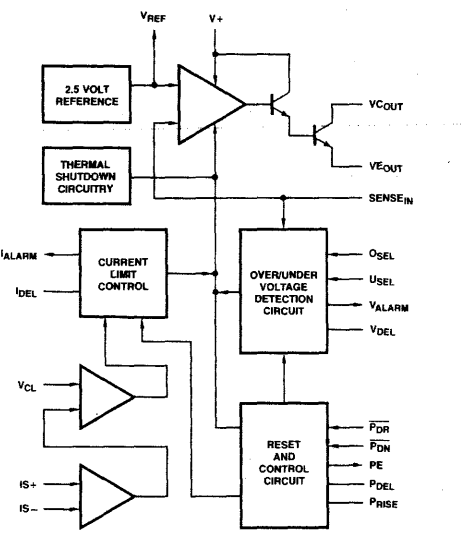
The over/under voltage section compares the voltage at the sense input of the regulator to the internal reference and determines if the difference exceeds the user programmed limits, ±5% or ±10%. If one of the limits is exceeded for a period longer than the user programmed delay, the regulator shuts down and the voltage alarm output is activated. The regulator is reset by activating the power down inputs or removing power from the device.

The current limit section detects overload current by means of an external sense resistor in series with V_{IN}, GND, or the output of the regulator. The user programs the threshold of this detection circuit with external resistors. The regulator shuts down if a current overload is detected for a period longer than a user programmed delay and the current alarm is activated. The regulator is reset by activating the power down inputs or removing power from the device.

The reset and control section provides to the user, the ability to turn the regulator on and off by logic control. The start up of the regulator is delayed by a user programmed interval after the power up signal is received. After this delay the regulator output ramps up at a rate which is also determined by the user. When the output voltage levels off at the preset value, the over/under voltage and current limit circuits are activated and a power up output is activated which can be used to signal to the user that the supply is operating or enable other circuits.

The Am6300 allows the user a great deal of flexibility in power supply configuration and control. It can be operated locally or remotely in a stand alone configuration or with external power transistors to increase the output current. The Am6300 can be cascaded with other Am6300s for a sequenced supply application.

BLOCK DIAGRAM

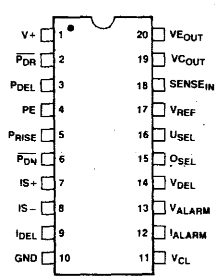


LIC-885

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	−55 to +125°C	AM6300DM
Hermetic DIP	0 to 70°C	AM6300DC
Plastic DIP	0 to 70°C	AM6300PC

CONNECTION DIAGRAM
Top View



Pin 1 is marked for orientation.

LIC-886

LINEAR

Advanced Micro Devices

LINEAR
Am6300

MAXIMUM RATINGS

Pulse Voltage at V+ (50ms)	50V	Input Voltage (all pins)	Gnd to V+
Continuous Voltage at V+	40V	Maximum Output Current	100mA
Input-Output Voltage Differential	37.5V	Internal Power Dissipation	1000mW (Note 1)

ELECTRICAL CHARACTERISTICS (Note 2)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
Voltage Regulator						
	Output Error (Note 3)		−1.0		+1.0	$\%V_{OUT}$
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation, $T_A = 25°C$	V_{IN} = 12 to 40V	.02	.2		$\%V_{OUT}$
$\Delta V_{OUT}/\Delta I_L$	Load Regulation, $T_A = 25°C$	I_L = 1mA to 50mA	.03	.15		$\%V_{OUT}$
	Ripple Rejection	f = 1kHz $T_A = 25°C$	74	86		dB
I_{BIAS}	Sense Input Bias Current			2	4	μA
V_{IN}	Input Operating Range		5		40	Volts
V_{OUT}	Output Operating Range		2.5		37.5	Volts
V_{IN}-V_{OUT}	Input-Output Differential		2.5		37.5	Volts
I_S	Supply Current			5	10	mA
Voltage Reference						
V_{REF}	Reference Voltage	$T_A = 25°C$	2.494	2.5	2.506	Volts
$\Delta V_{REF}/\Delta V_{IN}$	Line Regulation	V_{IN} = 12 to 40V				$\%V_{REF}$
$\Delta V_{REF}/\Delta I_{REF}$	Load Regulation	I_{REF} = 1mA to 5mA		.15	.30	$\%V_{REF}$
$\Delta V_{REF}/\Delta T_A$	Temperature Stability	0 to 70°C −55 to 125°C				ppm/°C
I_{SC}	Short Circuit Current	V_{REF} = 0V	10	30	60	mA
Current Overload Circuit						
V_{IS} (diff)/V_{CL}	Trip Point Ratio		.45	.5	.55	V/V
V_{CL}	Trip Point Input Range		0		.4	Volts
V_{IS} (diff)	Sense Voltage Input Range		0		.2	Volts
CMVR	Sense Input Common Mode Range		0		V_{IN}	Volts
I_{BIAS}	Input Bias Current (IS+, IS−)	V_{IS} = 0V to +2V V_{IS} = +2V to V_{IN}		−8 +8	−20 +20	μA
I_{OS}	Input Offset Current (IS+, IS−)			±1	±5	μA
I_{BIAS}	Input Bias Current (V_{CL})			−.25	−1.0	μA
Voltage Protection Circuit						
	+5% Error Trip Point	O_{SEL} = 5V	4.5	5	5.5	$\%V_{OUT}$
	−5% Error Trip Point	U_{SEL} = 5V	−4.5	−5	−5.5	$\%V_{OUT}$
	+10% Error Trip Point	O_{SEL} = 0V	9	10	11	$\%V_{OUT}$
	−10% Error Trip Point	U_{SEL} = 0V	−9	−10	−11	$\%V_{OUT}$
Digital Characteristics (Note 4)						
V_{IH}	Input High Level		2.0		V_{IN}	Volts
V_{IL}	Input Low Level		0		.8	Volts
V_{OL}	Open Collector Output Voltage	I_{OL} = 8mA I_{OL} = 15mA			.4 1.5	Volts

Notes: 1. Power dissipation ratings apply for $T_A = 25°C$. Derate linearly at 8mW/°C above 25°C for commercial parts and above 50°C for military parts.
2. All specifications are for V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 1mA, I_{REF} = 1mA and over the operating temperature range unless otherwise specified.
3. Includes all errors associated with on chip reference source and temperature effects.
4. Digital Inputs are $\overline{PDN}$, $\overline{PDR}$, OSEL, USEL
Digital Outputs are V_{ALARM}, I_{ALARM}, PE

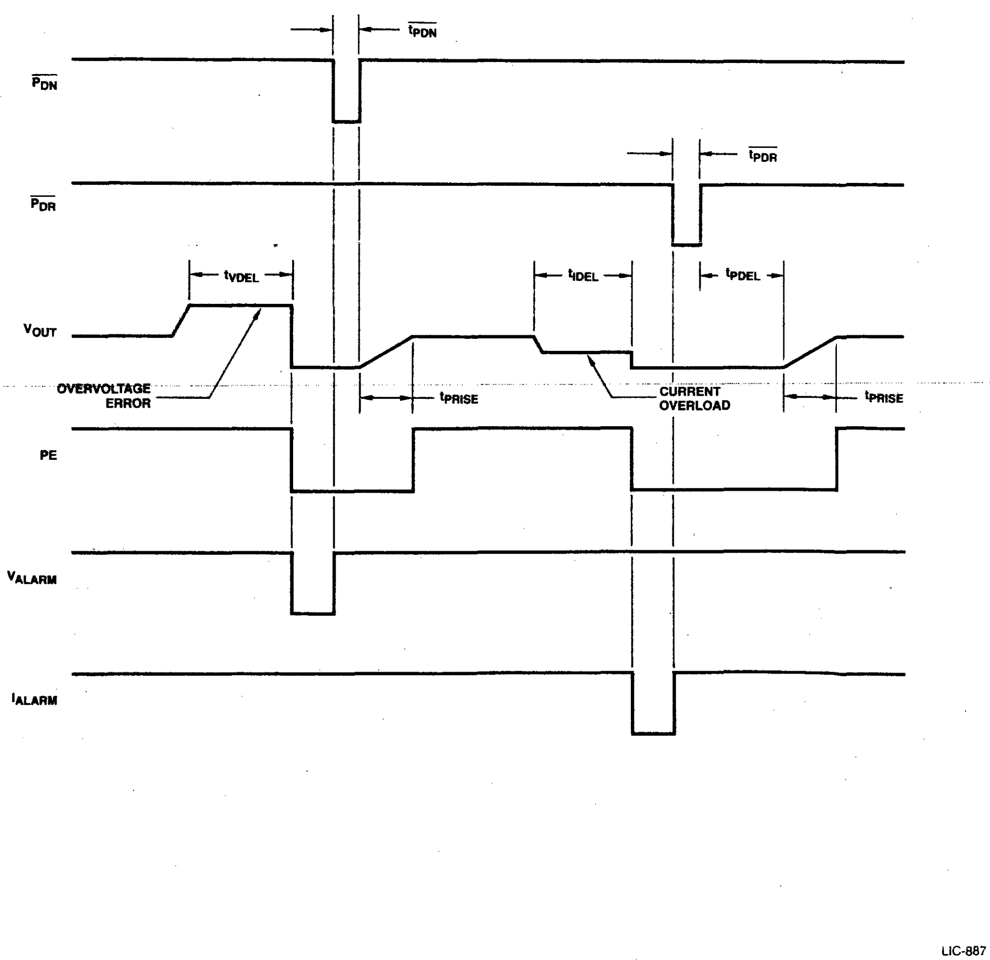
LINEAR
Am6300

TIMING CHARACTERISTICS

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{IDEL}, t_{VDEL}	Current Overload and Voltage Error Power Down Delays	Without external cap		1.2		µs
		With external cap, additional delay		.22		µs/pF
t_{PDEL}	Power Up Delay (Note 5)	Without external cap		1.2		µs
		With external cap, additional delay		.22		µs/pF
t_{PRISE}	Power Up Rise Time (Note 5)	Without external cap		1.5		µs
		With external cap		.22		µs/pF
t_{PDN}, t_{PDR}	Power Down Reset Pulse Width		10			µs

Note 5: It is necessary to make the total time t_{PDEL} + t_{PRISE} greater than the rise time of the supply to the Am6300 to insure proper power up.

TIMING WAVEFORMS



Advanced Micro Devices

LINEAR
Am6301

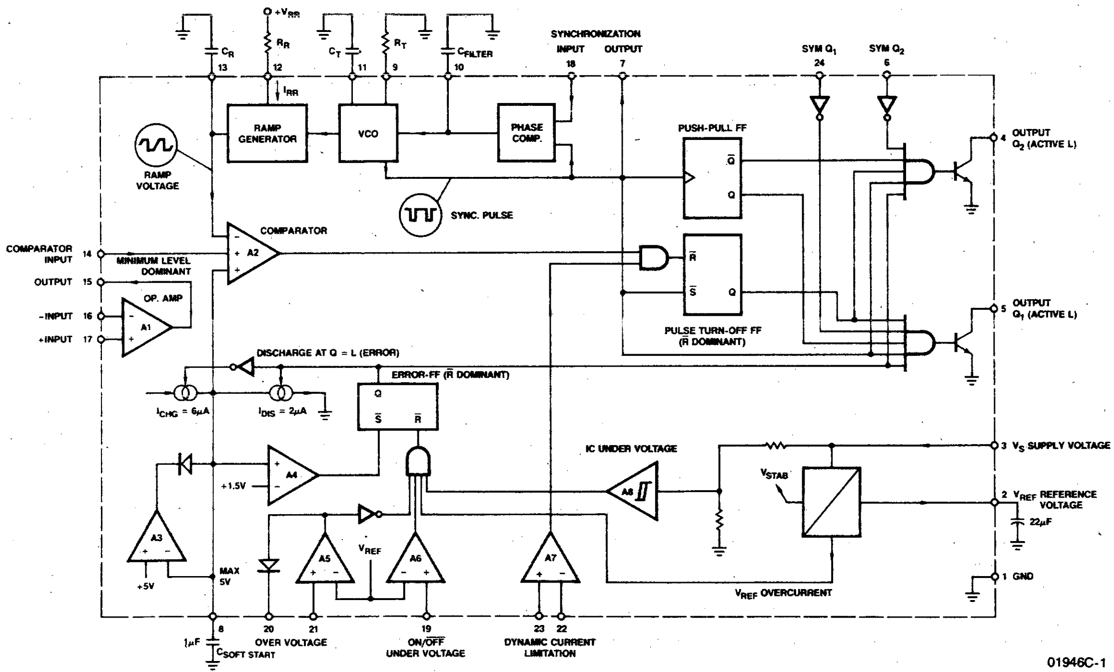
DISTINCTIVE CHARACTERISTICS

- Feed-forward (line hum suppression)
- Output over/under voltage protection
- Input under voltage protection
- Cycle-by-cycle current limiting
- Soft start
- 250kHz max. oscillator frequency
- Phase lock capability
- 96% max. duty cycle
- Double pulse suppression
- Symmetry inputs for push-pull converter
- Remote shutdown
- Pin equivalent to the Siemens' TDA 4700

GENERAL DESCRIPTION

The Am6301 Switching Power Supply Controller contains all the digital and analog functions necessary to control blocking, single-ended, or push-pull switching power supplies. It contains the voltage controlled oscillator, ramp generator, comparator, and reference for basic switched mode power supplies, as well as, a full complement of interface circuits and circuitry to protect both the power supply and its load.

BLOCK DIAGRAM



01946C-1

ORDERING INFORMATION

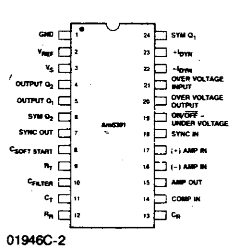
Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type	Temperature Range
Am6301DM	Hermetic DIP	−55 to +125°C
Am6301LC	Leadless*	0 to 70°C
Am6301DL	Hermetic DIP	−25 to +85°C
Am6301DC	Hermetic DIP	0 to 70°C
Am6301PC	Plastic DIP	0 to 70°C

*Availability of leadless packages will be announced.

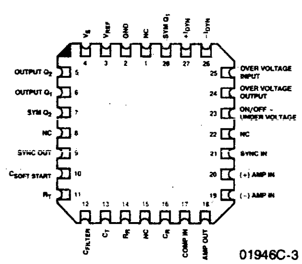
CONNECTION DIAGRAMS – Top Views

D-24-1, P-24-1



01946C-2

L-28-1



01946C-3

Note: Pin 1 is marked for orientation.

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LINEAR
Am6301

Am6301DC, DL, PC, LC
MAXIMUM RATINGS (Above which useful life may be impaired)

Supply Voltage V_S	33V	Voltage at Q_1, Q_2	33V
Input Voltage (all inputs)	Gnd to V_S	Current at Q_1, Q_2	70mA
Output Voltage A5	33V	Input Current R_{ramp}	1mA
Output Voltage A1	6.5V	Operating Temperature	
Storage Temperature	−65 to +125°C	Am6301DL	−25 to +85°C
Lead Temperature (soldering 60 sec)	300°C	Am6301DC, Am6301PC, Am6301LC	0 to +70°C
Power Dissipation	(Note 3)		

ELECTRICAL CHARACTERISTICS (Note 1)
These specifications apply for $11V \leq V_S \leq 30V$, $f_{VCO} = 15kHz$, over the operating temperature range unless otherwise specified.

Parameters	Description	Test Conditions	Min	Typ	Max	Units
Regulator						
V_S	Supply Voltage		11		30	Volts
I_S	Supply Current	C_T = 1nF, F = 100KHz	8	12	20	mA
f_{VCO}	Operating Frequency Range		40		250K	Hz
Reference						
V_{REF}	Reference Voltage	$0 \leq I_{REF} \leq 5mA$	2.35	2.50	2.65	Volts
ΔV_{REF}	Line Regulation	V_S = 25V ± 20%		5	15	mV
ΔV_{REF}	Load Regulation	I_{REF} = 0 to 5mA		10	20	mV
$\Delta V_{REF}/\Delta T_A$	Temperature Stability			250	400	µV/°C
Oscillator						
f_{VCO}	Operating Frequency Range		40		250K	Hz
Δf/f	Initial Tolerance	ΔC_T = 0%, ΔR_T = 0%			±7	%
Δf/f	Frequency Stability	V_S = 25V ± 20%	−1		1	%
t_{VCO}	Fall Time	C_T = 1nF		1		µs
Ramp Generator						
f_{ramp}	Frequency Range		40		250K	Hz
V_{ramp} Hi	Voltage at C_{ramp} High	$10\mu A \leq I_{ramp} \leq 400\mu A$		5.5		Volts
V_{ramp} Low	Voltage at C_{ramp} Low	$10\mu A \leq I_{ramp} \leq 400\mu A$		1.8		Volts
I_{ramp}	Input Current at R_{ramp}		10		400	µA
Synchronization						
V_{IH}	Synchronization Input		2			Volts
V_{IL}					0.8	Volts
V_{OH}	Synchronization Output	I_{OH} = 200µA	4			Volts
V_{OL}		I_{OL} = 1.6mA			0.4	Volts
I_B	Input Bias Current		−5	−1		µA
Comparator A2						
I_B	Input Bias Current		−2	−1		µA
t_{A2}	Turn-Off Delay (Note 2)	T_A = 25°C		470		ns
V_{IN}	Input Voltage for Duty Cycle	T_{On}/T_{Off} = 0%		1.8		Volts
		T_{On}/T_{Off} = Max		5.0		
Soft Start						
I_{CHG}	Charging Current			6		µA
I_{DIS}	Discharging Current			2		µA
V_{LIM}	Upper Limiting Voltage			5		Volts
V_{TH}	Reset Voltage			1.5		Volts

LINEAR
Am6301

ELECTRICAL CHARACTERISTICS (Cont.)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
Operational Amplifier						
A_{OL}	Open Loop Gain		60	80		dB
V_{OS}	Input Offset Voltage		−10		10	mV
$\Delta V_{OS}/\Delta T_A$	V_{OS} Tempco		−30		30	μV/°C
I_B	Input Bias Current		−2	−0.5		μA
V_{CM}	Common Mode Range		0		5	Volts
I_O	Output Current		−3		1.5	mA
$\Delta V/\Delta t$	Output Slew Rate			1		V/μs
BW	3dB Bandwidth			3		MHz
ϕ_t	Phase Shift at 3MHz			120		degrees
VSW	Output Voltage Swing	$-3mA \leq I_L \leq 1.5mA$	1.5		5.5	Volts
Symmetry						
V_{IH}	Input Voltage		2			Volts
V_{IL}	Input Voltage				0.8	Volts
I_{IL}	Input Low Current		−2	−1		μA
Output States Q_1, Q_2						
V_{OL}	Output Voltage	$I_O = 20mA$			1.1	Volts
I_{OH}	Output Current	$V_{OH} = 30V$			2	μA
ON/$\overline{OFF}$, Under Voltage						
V_{TH}	Threshold Voltage		V_{REF} − 30mV	V_{REF}	V_{REF} + 30mV	Volts
I_B	Input Bias Current		−2	−1		μA
t_{OFF}	Turn-Off Delay			250		ns
t_{ERR}	Error Recognition Time			50		ns
Dynamic Current Limiting						
V_{CM}	Common Mode Range		0		4	Volts
V_{OS}	Input Offset Voltage		−10		10	mV
I_B	Input Bias Current		−2	−1		μA
t_{OFF}	Turn-Off Delay			250		ns
t_{ERR}	Error Recognition Time			50		ns
Over Voltage						
V_{TH}	Threshold Voltage		V_{REF} − 30mV	V_{REF}	V_{REF} + 30mV	Volts
I_B	Input Bias Current		−2	−1		μA
I_{OH}	Output Current	$V_{OH} = 5V$	0		200	μA
t_{OFF}	Turn-Off Delay			250		ns
t_{ERR}	Error Recognition Time			50		ns
Supply Under Voltage						
V_{ON}	Turn-On Threshold, V_S Rising		8.8	9.6	10.5	Volts
V_{OFF}	Turn-Off Threshold, V_S Falling		8.5	9	10.0	Volts

Notes: 1. All typical values are specified at $V_S = 12V$ and $T_A = 25°C$.

2. The A2 comparator turn-off delay is measured from pin 14 to pin 4 or pin 5. The input signal on pin 14 is a negative-going pulse from 3V to 0.5V. The delay is measured from the 2V level on the input to the 2V level on the output. The output current is set at 4mA. The signal on pin 14 goes negative when the ramp voltage is equal to 2V.

3. For T_A greater than 25°C, derate to limit T_J to a maximum of 150°C. For P_D less than 750mW use typical thermal resistance as follows:

Typ	D-24-1	P-24-1	L-28-1	
θ_{JA}	50	120	100	°C/watt
θ_{JC}	15	60	40	°C/watt

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Am6301 FUNCTIONAL DESCRIPTION

VOLTAGE-CONTROLLED OSCILLATOR (VCO)

The VCO (voltage-controlled oscillator) generates a sawtooth voltage at C_T. The duration of the falling edge is determined by the selection of C_T. The duration of the rising edge and thus the oscillator frequency is determined by R_T and C_T. Maximum oscillator frequency is 250kHz. The oscillator frequency can be varied for frequency synchronization purposes by varying the voltage at C_{filter}. The falling edge of the VCO generates the synchronization pulse and triggers the ramp generator and other parts of the Am6301.

RAMP GENERATOR – FEED-FORWARD CONTROL

The ramp generator is triggered by the synchronization pulse of the VCO and oscillates at the same frequency. The duration of the falling edge of the ramp generator must be shorter than the fall time of the VCO. The voltage of the rising edge of the ramp generator and a DC voltage at comparator A2 are compared for pulse width control of the output. The slope of the rising edge is adjusted via the current through R_R. This enables an additional superimposed control of the duty cycle dependent on the input voltage of the Switched Mode Power Supplies (SMPS). This capability (feed-forward) allows for compensation of a known interference (e.g. line hum).

PHASE COMPARATOR – SYNCHRONIZATION

If the Am6301 is operated without external synchronization, the synchronization input must be connected to the synchronization output, so that the phase comparator sets the voltage at C_{filter}. The VCO then oscillates at the frequency set by R_T and C_T. Other circuits can be synchronized with the synchronization output. The Am6301 can be synchronized to an external signal of any duty cycle. The synchronization input and output are TTL compatible.

PUSH-PULL FLIP-FLOP

The push-pull flip-flop is toggled by the falling edge of the VCO. This guarantees that only one of the two push-pull outputs can be enabled at any one time.

COMPARATOR A2 – PULSE WIDTH MODULATION

The two noninverting inputs of the comparator are switched in such a manner that the lowest level is always compared with the inverting input. As soon as the voltage of the rising sawtooth at C_R exceeds the lower of the two levels, both outputs are disabled via the pulse turn-off flip-flop.

REGULATING AMPLIFIER A1

A1 is a high-quality regulating amplifier. It can be used in the control loop to transmit the amplified error voltage onto the free noninverting input of the comparator A2. A voltage change is thus transformed into a duty cycle change. The common mode range of A1 covers 0 to +5V. A1's low output impedance allows the use of feedback for the adjustment of the regulator loop-characteristics.

PULSE TURN-OFF FLIP-FLOP

This flip-flop enables the outputs at the beginning of each half period, and upon an error signal from A7 or a turn-off signal from A2 switches the outputs off for the remainder of the half period. Double pulses at the output cannot occur.

COMPARATOR A3

A3 limits the voltage at the $C_{soft\ start}$ pin (and also one input of A2) to a maximum of 5V. For a specified slope of the rising ramp generator edge, the duty cycle can be limited to a maximum value.

COMPARATOR A4

Comparator A4 has its switching threshold set to 1.5V and its output connected to the error flip-flop, so that when the voltage at capacitor $C_{soft\ start}$ is less than 1.5V the flip-flop is set. The error flip-flop only accepts the set pulse if no reset signal is present. Thus, an output turn-on is prevented as long as an error signal is present.

SOFT START

The output duty cycle is a function of the lower of the two voltages at the noninverting inputs of A2. At the time the Am6301 is turned on, the voltage at capacitor $C_{soft\ start}$ is equal to 0V. As long as no error exists, this capacitor is charged with a current of 6μA to the maximum value of 5V. In the case of an error, $C_{soft\ start}$ is discharged with a current of 2μA. The error flip-flop is set when the $C_{soft\ start}$ voltage is below 1.5V and the outputs are enabled if a reset signal is not present at the same time. The minimum ramp generator voltage is 1.8V, therefore, the soft start circuit only controls the duty cycle after the voltage at $C_{soft\ start}$ exceeds 1.8V.

ERROR FLIP-FLOP

Error signals to input $\overline{R}$ of the error flip-flop cause the outputs to be disabled immediately. The system turns on again using the soft start, after the error has been eliminated.

COMPARATOR A5 – OVER VOLTAGE

The input or output voltages of an SMPS can be monitored using A5. In the case of an over voltage, the error flip-flop immediately disables the IC outputs. After the over voltage is reduced, the SMPS turns back on using the soft start. The output of A5 can be fed back to the input. This causes the IC output stage to remain disabled even after elimination of the over voltage, until the supply voltage is briefly turned off, or the over voltage input is briefly connected to ground. To use this SCR-type action, the voltage to be monitored must be coupled resistively ($\geq$5KΩ) to the over voltage comparator.

COMPARATOR A6 – ON/$\overline{\text{OFF}}$ UNDER VOLTAGE

The comparator A6 reacts to an under voltage relative to V_{REF} and switches the IC outputs off. The input voltage of the SMPS can for example, be monitored, turning the outputs off if the input voltage is below a desired level. When the input voltage returns to the desired level, the Am6301 turns back on using the soft start. This input can also be used as a TTL compatible ON/$\overline{\text{OFF}}$ control.

COMPARATOR A7 – DYNAMIC CURRENT LIMITING CIRCUIT

A7 provides for the recognition of over current in the switching transistors. The system is turned on again at the beginning of the half period after the error is eliminated, the soft start is not used however. The A7 common mode range extends from 0 to +4V so that the smallest voltage drops can be recognized. The delay time from the occurrence of an error to the disabling of the outputs is only 250ns.

COMPARATOR A8 – IC UNDER VOLTAGE

Comparator A8 prevents undefined operating conditions of the IC outputs if the IC supply voltage becomes too low. If $V_S \leq 9V$, the output stage is disabled. This condition is maintained until V_S = 0V. Built-in hysteresis prevents permanent switching at the comparator's switching threshold. At a supply voltage of $V_S \geq 9.6V$, the Am6301 turns on using the soft start.

LINEAR
Am6301

ELECTRICAL CHARACTERISTICS (Cont.)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
Operational Amplifier						
A_{OL}	Open Loop Gain		60	80		dB
V_{OS}	Input Offset Voltage		−10		10	mV
$\Delta V_{OS}/\Delta T_A$	V_{OS} Tempco		−30		30	μV/°C
I_B	Input Bias Current		−2	−0.5		μA
V_{CM}	Common Mode Range		0		5	Volts
I_O	Output Current		−3		1.5	mA
$\Delta V/\Delta t$	Output Slew Rate			1		V/μs
BW	3dB Bandwidth			3		MHz
ϕ_t	Phase Shift at 3MHz			120		degrees
VSW	Output Voltage Swing	$-3mA \leq I_L \leq 1.5mA$	1.5		5.5	Volts
Symmetry						
V_{IH}	Input Voltage		2			Volts
V_{IL}					0.8	Volts
I_{IL}	Input Low Current		−2	−1		μA
Output States Q_1, Q_2						
V_{OL}	Output Voltage	I_O = 20mA			1.1	Volts
I_{OH}	Output Current	V_{OH} = 30V			2	μA
ON/$\overline{OFF}$, Under Voltage						
V_{TH}	Threshold Voltage		V_{REF} − 30mV	V_{REF}	V_{REF} + 30mV	Volts
I_B	Input Bias Current		−2	−1		μA
t_{OFF}	Turn-Off Delay			250		ns
t_{ERR}	Error Recognition Time			50		ns
Dynamic Current Limiting						
V_{CM}	Common Mode Range		0		4	Volts
V_{OS}	Input Offset Voltage		−10		10	mV
I_B	Input Bias Current		−2	−1		μA
t_{OFF}	Turn-Off Delay			250		ns
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COMPARATOR A3

A3 limits the voltage at the $C_{soft\ start}$ pin (and also one input of A2) to a maximum of 5V. For a specified slope of the rising ramp generator edge, the duty cycle can be limited to a maximum value.

COMPARATOR A4

Comparator A4 has its switching threshold set to 1.5V and its output connected to the error flip-flop, so that when the voltage at capacitor $C_{soft\ start}$ is less than 1.5V the flip-flop is set. The error flip-flop only accepts the set pulse if no reset signal is present. Thus, an output turn-on is prevented as long as an error signal is present.

SOFT START

The output duty cycle is a function of the lower of the two voltages at the noninverting inputs of A2. At the time the Am6301 is turned on, the voltage at capacitor $C_{soft\ start}$ is equal to 0V. As long as no error exists, this capacitor is charged with a current of 6μA to the maximum value of 5V. In the case of an error, $C_{soft\ start}$ is discharged with a current of 2μA. The error flip-flop is set when the $C_{soft\ start}$ voltage is below 1.5V and the outputs are enabled if a reset signal is not present at the same time. The minimum ramp generator voltage is 1.8V, therefore, the soft start circuit only controls the duty cycle after the voltage at $C_{soft\ start}$ exceeds 1.8V.

ERROR FLIP-FLOP

Error signals to input $\overline{R}$ of the error flip-flop cause the outputs to be disabled immediately. The system turns on again using the soft start, after the error has been eliminated.

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The input or output voltages of an SMPS can be monitored using A5. In the case of an over voltage, the error flip-flop immediately disables the IC outputs. After the over voltage is reduced, the SMPS turns back on using the soft start. The output of A5 can be fed back to the input. This causes the IC output stage to remain disabled even after elimination of the over voltage, until the supply voltage is briefly turned off, or the over voltage input is briefly connected to ground. To use this SCR-type action, the voltage to be monitored must be coupled resistively (≥5KΩ) to the over voltage comparator.

COMPARATOR A6 – ON/$\overline{\text{OFF}}$ UNDER VOLTAGE

The comparator A6 reacts to an under voltage relative to V_{REF} and switches the IC outputs off. The input voltage of the SMPS can for example, be monitored, turning the outputs off if the input voltage is below a desired level. When the input voltage returns to the desired level, the Am6301 turns back on using the soft start. This input can also be used as a TTL compatible ON/$\overline{\text{OFF}}$ control.

COMPARATOR A7 – DYNAMIC CURRENT LIMITING CIRCUIT

A7 provides for the recognition of over current in the switching transistors. The system is turned on again at the beginning of the half period after the error is eliminated, the soft start is not used however. The A7 common mode range extends from 0 to +4V so that the smallest voltage drops can be recognized. The delay time from the occurrence of an error to the disabling of the outputs is only 250ns.

COMPARATOR A8 – IC UNDER VOLTAGE

Comparator A8 prevents undefined operating conditions of the IC outputs if the IC supply voltage becomes too low. If V_S ≤9V, the output stage is disabled. This condition is maintained until V_S = 0V. Built-in hysteresis prevents permanent switching at the comparator's switching threshold. At a supply voltage of V_S ≥9.6V, the Am6301 turns on using the soft start.

SYMMETRY

Saturation of the transformer core must be prevented in push-pull converters. The degree of saturation of the transformer can be determined with an external circuit; and, in relation to this, the on times of the outputs can be asymmetrically shortened. If the symmetry correction circuit is not required, the symmetry inputs must be connected to ground. The input levels are TTL compatible.

OUTPUTS, DEADTIME

The two outputs Q_1 and Q_2 are transistors with open collectors. Their saturation voltage is 1V at 25mA. They operate in a push-pull mode and can be connected in parallel to drive single-ended converters with a maximum duty cycle of 96%. The time, during which only one of the two outputs is on, can be varied. The duration of the falling edge at the VCO is the same as the minimum time (dead time) during which both outputs are disabled simultaneously. The dead time, in push-pull SMPS, prevents the power transistors from being on at the same time.

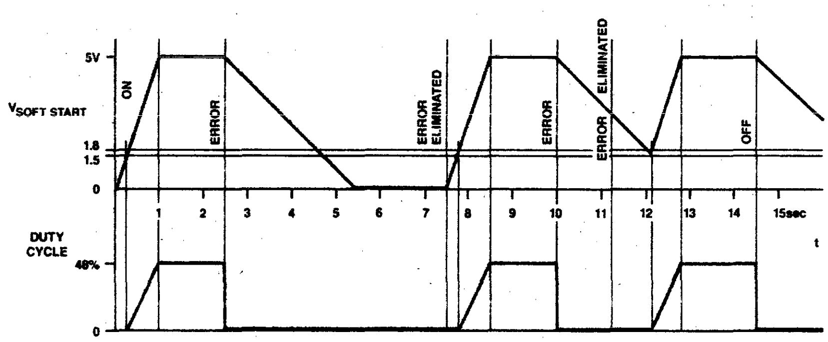


Figure 1. Am6301 System Timing Showing Soft Start, Error Timing, and Remote Shutdown. ($C_{soft\ start} = 1\mu F$.)

ABI-021

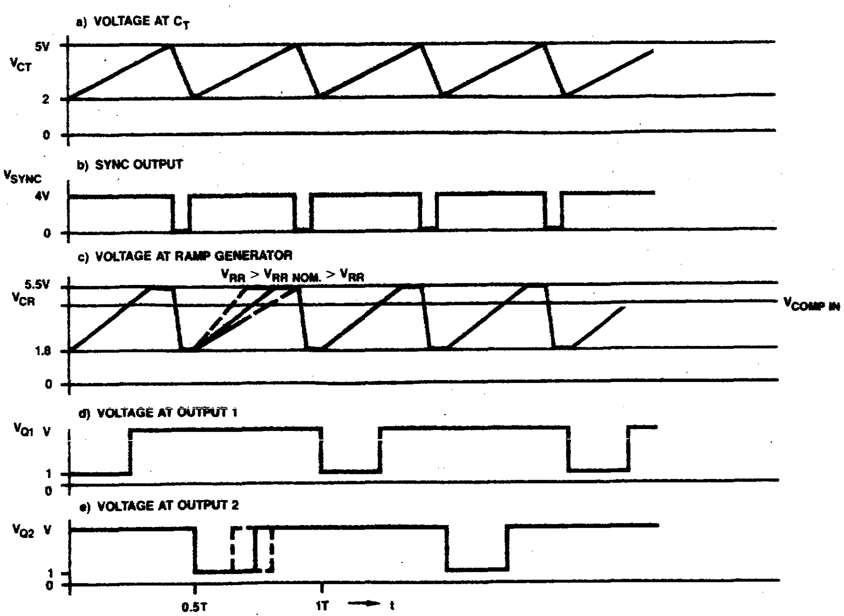


Figure 2. Am6301 Pulse Timing Diagram, Dotted Lines Show the Effect of Feed-Forward Control.

ABI-022

FUNCTIONAL PIN DESCRIPTION

V_{REF} The output of the internal 2.5V reference.

Output Q_1, Q_2 The open collector output transistors capable of sinking 70mA each.

SYMQ_1, Q_2 Transformer unbalance control inputs. With a small amount of external circuitry these inputs can be used to cause asymmetrical output duty cycles. This allows correction for imbalances in the push-pull circuitry.

SYNC OUT The VCO output, used for synchronizing other circuits to the Am6301.

$C_{soft\ start}$ An external capacitor at this pin causes the output duty cycle to increase linearly during power up.

R_T, C_T An external resistor and a capacitor at these pins control the VCO center frequency of the phase locked loop oscillator.

C_{filter} An external filter capacitor for the control voltage of the phase locked loop is connected to this pin.

SYNC IN This pin is connected to one input of the phase comparator in the phase locked loop, the other input is internally connected to the VCO output.

R_R, C_R An external resistor and a capacitor at these pins control the slope of the ramp generator. The feed-forward control works by changing the voltage across R_{ramp} which affects the ramp slope and causes a modulation of the duty cycle.

Comp In The noninverting input of the pulse width modulating comparator.

Amp Out The output of the uncommitted operational amplifier. This amplifier is used as the error amplifier in most systems.

(+) Amp In, (−) Amp In These are the inputs of the uncommitted operational amplifier.

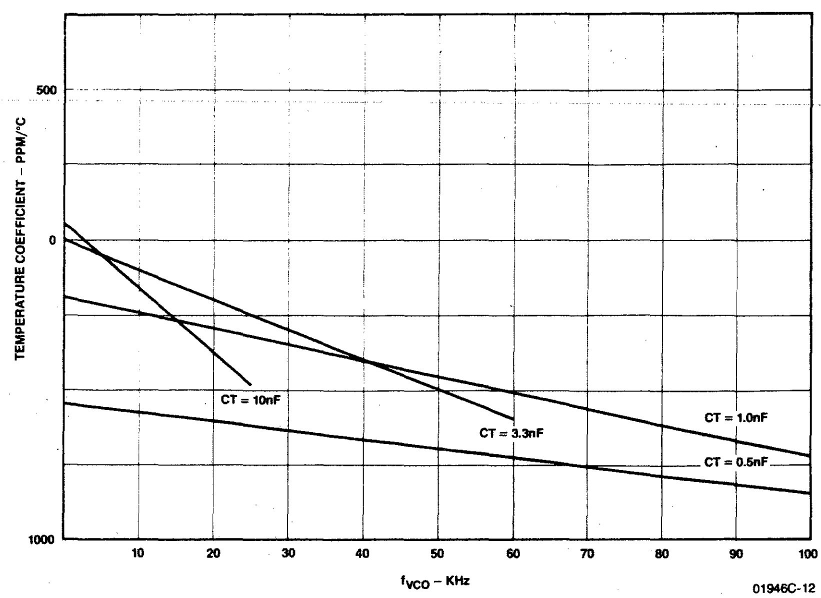
ON/$\overline{\text{OFF}}$ Under Voltage This input disables the outputs when it is connected to a voltage lower than V_{REF}. It can be connected as a remote shutdown or as an under voltage protection.

Over Voltage Input This input disables the outputs whenever it is higher than V_{REF}.

Over Voltage Output The output of the over voltage comparator. This pin can be connected back to the over voltage input for SCR-type protection.

$+I_{DYN}$, $-I_{DYN}$ Sense inputs for the dynamic current limiting circuit.

Figure 5. Am6301 f_{VCO} Temperature Coefficient.



Advanced Micro Devices

COMMUNICATIONS
Am7910
PRELIMINARY DATA (Revised)

Am7910
FSK Modem
WORLD-CHIP™

- Complete FSK MODEM in a 28-pin package (except line interface)
- Meets basic Bell 103/113/108, Bell 202, CCITT V.21, CCITT V.23 specifications (pin-programmable selection)
- No external filtering required
- All digital processing, including digital filters
- ADC/DAC on chip
- Includes essential RS-232/CCITT V.24 handshake signals
- Auto-answer capability
- Local copy/test modes
- 1200 bps full duplex on 4-wire line

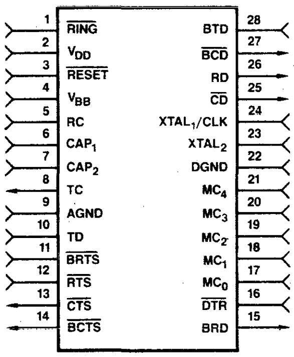


Figure 1. Am7910 Pinout

MMC-036

GENERAL DESCRIPTION

The Am7910 is a single-chip asynchronous Frequency Shift Keying (FSK) voiceband modem. Operating at rates up to 300, 600 or 1200 bits per second, it is compatible with the applicable Bell and CCITT recommended standards for 103/113/108, 202, V.21 and V.23 type modems. Five mode control lines select a desired modem configuration.

Digital signal processsing techniques are employed in the Am7910 to perform all major functions such as modulation, demodulation and filtering. The Am7910 contains on-chip analog-to-digital and digital-to-analog converter circuits to minimize the external components in a system. This device includes the essential RS-232/CCITT V.24 terminal control signals with TTL levels.

Clocking can be generated by attaching a crystal to drive the internal crystal oscillator or by applying an external clock signal.

A data access arrangement (DAA) or acoustic coupler must provide the phone line interface externally.

The Am7910 is fabricated using N-channel MOS technology in a 28-pin package. All the digital input and output signals (except the external clock signal) are TTL compatible. Power supply requirements are ±5 volts.

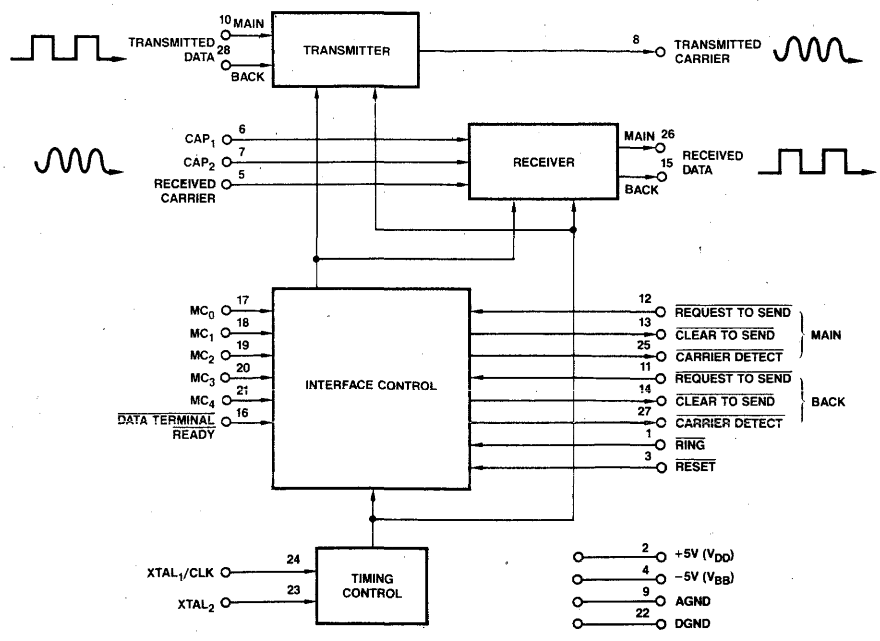


Figure 2. Am7910 Block Diagram

MMC-179

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Advanced Micro Devices

A COMPLETE FSK MODEM ON ONE WORLD-CHIP™

It's the World's First

The new Am7910 is the first complete, asynchronous Frequency Shift Keying modem ever offered on a single LSI chip. Our Am7910, a crystal, and a few inexpensive, non-critical components are all you need. No external filters, no hybrids, no tuned circuits are needed. Never before has the modem function been so easy to build into your products. See Figure 1.

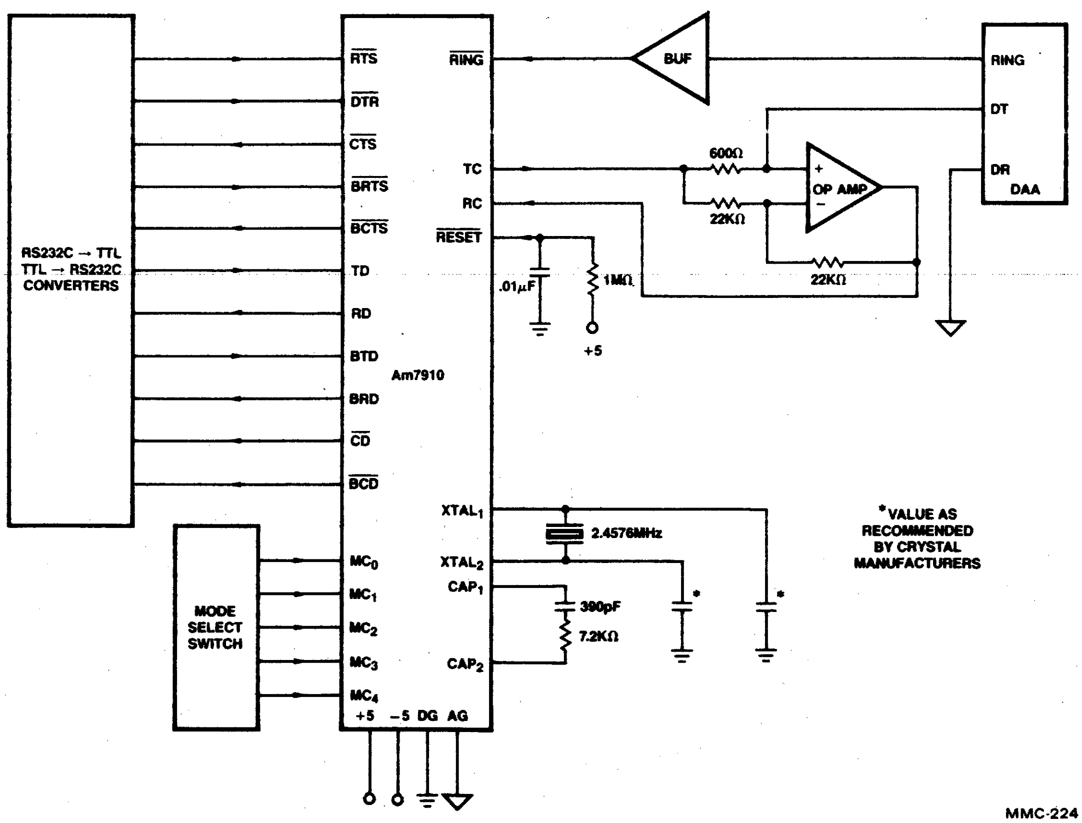
It's the World's Most Complete

All the features a modem should have are built right in. Filters are already there. Handshake signals already there. Auto-answer is already there. Local loopback is already there. Back channels are already there. No extra components are required to implement these functions. Even line equalization is available if you want it. No modem chip or chip set has ever offered you so many features.

It's a WORLD-CHIP™

No matter where you market your product, the Am7910 is the perfect modem solution. It's designed to meet communications performance standards around the world. Without any additional circuitry, it can be switched to any of 9 Bell or CCITT standards. The flexibility of Digital Signal Processing allows systems built with the Am7910 to be used all over the world without modification to the modem circuit.

Figure 1. Stand-Alone Am7910 Application



Advanced Micro Devices

COMMUNICATIONS
Am7910

DIGITAL SIGNAL PROCESSING FOR HIGH STABILITY, WITHOUT CRITICAL COMPONENTS

The Am7910 Doesn't Drift With Time or Temperature

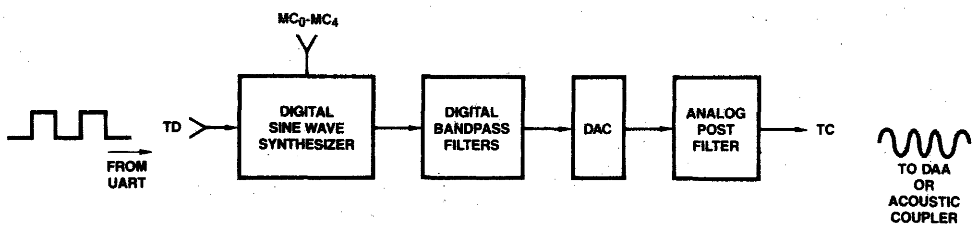
The Am7910 uses digital signal processing techniques (DSP) to perform all major functions, including modulation, demodulation and filtering. Because of the use of DSP, the performance of each section of the Am7910 is perfectly predictable and inherently stable over time and temperature. The modem performance specifications are designed into the digital signal processing algorithms, and that's where they stay, inside the chip, never changing, guaranteed. There's nothing to adjust, nothing to age or drift. See Figure 2.

No External Filters

Digital Signal Processing completely eliminates the need for external critical-tolerance filters that analog designs require. Since no critical tuned components are required, printed circuit board design with the Am7910 is easier than ever. And DSP does not produce the noise and supply voltage sensitivity that is commonly found in switched capacitor designs. The bottom line is, fewer components, therefore a lower cost system solution.

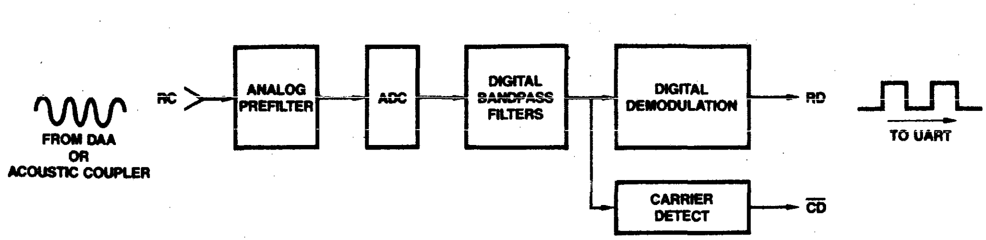
Figure 2.

a) Transmitter Block Diagram



MMC-033

b) Receiver Block Diagram



MMC-034

LINEAR

Advanced Micro Devices

SELECTABLE TO ANY OF 9 DIFFERENT WORLD STANDARDS

The Am7910 is designed to be used in equipment all over the world. The device operates in Bell 103 and 202, and CCITT V.21 and V.23 modem configurations at baud rates from 300 to 1200bps (with back channel). Mode selection is controlled by five simple programming inputs. No crystals need to be changed. No extra resistors, capacitors, or interface circuits. Just switch a few control lines.

MODEM CONFIGURATIONS

STD	BPS	DUPLEX	FEATURES
Bell 103	300	Full	Originate
Bell 103	300	Full	Answer
Bell 202	1200	Half	
Bell 202	1200	Half	Line Equalizer
CCITT V.21	300	Full	Originate
CCITT V.21	300	Full	Answer
CCITT V.23 mode 2	1200	Half	
CCITT V.23 mode 2	1200	Half	Line Equalizer
CCITT V.23 mode 1	600	Half	

MORE BUILT-IN FEATURES MAKE THE Am7910 THE EASIEST MODEM TO USE

Loopback for Simplified Testing

Ten loopback modes exist which permit both analog and digital loopback for each modem configuration. When a loopback mode is selected, the signal processing circuits for both the transmitter and receiver are set to operate on the same channel or frequency band. The analog output (Transmitted Carrier) and the analog input, (Received Carrier) can be externally connected together for local analog loopback. Alternatively, the digital data signals (TD and RD, or BTD and BRD,) can be connected externally, allowing a remote modem to test the local modem with its digital data signals looped back. Thus, the Am7910 reduces maintenance, service time, and cost. The 202 and V.23 loopback modes can also be used for 1200bps full duplex operation over 4-wire lines.

Back Channel Option Included

Low bit-rate back channels are provided by the Am7910 when the Bell 202 or CCITT V.23 modem configurations are selected. The back channel uses the remaining bandwidth of the line to return acknowledgement and control signals to the sender on another channel, while the sender continues to transmit at 1200 baud. Overall transmission speed is improved by not having to turn the line around to send an acknowledgement, nor is it necessary to complete transmission of a data block before receiving an error signal. The 202 back channel allows up to 5 bits per second and the V.23 back channel allows up to 75 bits per second.

Auto-Answer for Remote Installations

Auto-answer capability, important for equipment in remote places, is also built in. Upon receipt of a signal at its Ring Input, the Am7910 generates a silence interval followed by an answer tone of the proper duration at the Transmitted Carrier output. The auto-answer sequence meets Bell and V.25 specifications.

RS-232 and CCITT V.24 Terminal Control Signals Provided On-Chip

Essential terminal control signals such as Data Terminal Ready (DTR), Request to Send (RTS), Clear to Send (CTS) and Carrier Detect (CD), are included in the Am7910. All the specified delays, such as Request-to-Send ON to Clear-to-Send ON are automatically inserted. The control signals are TTL compatible.

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Am7910

SETS THE INTERNATIONAL STANDARD OF PERFORMANCE

The measure of a modem's performance is its ability to extract correct data from a signal received over a line with severe distortion, attenuation, and noise. The graphs below show the Bit Error Rate (BER) of the Am7910 under two sets of conditions. At the left is the data for a Bell 103 configuration over an undistorted line and a line with amplitude and group delay distortion. On the right is the data for a V.23 configuration for an undistorted and a severely distorted line. Compare this performance data with any other modem chip or chip set and you'll see why the Am7910 sets the standard.

Performance Curves

Figure 3. 103 ORIG, 300bps BER versus SNR, Different Lines

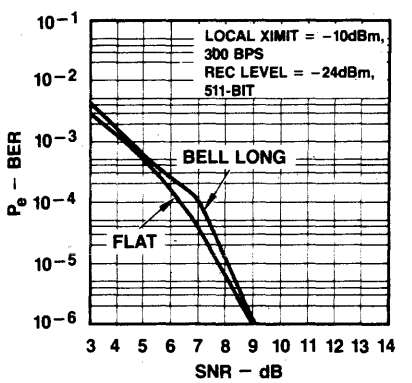
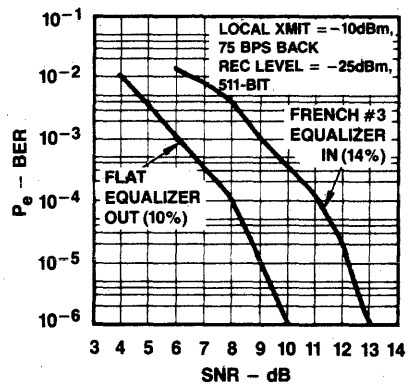


Figure 4. CCITT V.23, 1200bps Different Lines



MMC-054

COMMUNICATIONS
Am7910

THE WORLD-CHIP™ SERIES

Telephone systems around the world are evolving rapidly into something new: a huge digital data communications network. The crossbar switches of yesterday are being replaced by compact electronic switches that route digital bit streams from one subscriber to another. The wires that used to carry human speech alone now also carry streams of digital data via modems. Soon the telephone set itself will be changed from a simple device for talking and listening into a specialized data terminal, capable of doing much more.

As the information carried by our telephone networks has changed, new standards have been added to the old. Standards to digitize voice. Standards for sending digital data over voice-grade lines. Standards for multiplexing many data packets onto a single line. Around the world, two groups of standards are used – one developed by Bell in the U.S., another developed by the CCITT. Until now, the electronic components designed to make this revolution possible have been specialized for one group of standards or the other, and usually for only one standard or variation within that group.

Advanced Micro Devices' World-Chip™ Series is different. We're using a variety of technologies to create circuits that support the telecom revolution all over the world. We're using advanced architectural concepts, especially digital signal processing, to move critical filtering and signal conditioning directly onto the integrated circuit. Digital techniques provide guaranteed high stability and repeatability, and also allow changes to filtering characteristics under user program control. We're using our skills in both linear and digital circuit design to put the conversions between analog signals and digital data on the same IC as the digital processing circuits. And we're using our MOS and Bipolar process technologies to solve each part of the system problem in an optimum way with parts that are designed to work together. By the end of the decade AMD will have led the way to more efficient, effective and inexpensive methods for making the world an even smaller (and faster) place in which to communicate.

AMD has developed a set of components that work in any of the world's telecommunications systems. Each integrated circuit can be programmed to perform its function in conformance with any of the applicable standards. The state-of-the-art features built into our devices are available simultaneously to customers designing equipment for any of the world's telecom markets. And customers who themselves design equipment for more than one market can use a single set of circuits – Advanced Micro Devices' World-Chips™ – to meet all their needs.

RELATED WORLD-CHIP™ SERIES PRODUCTS:

- Am7901/7902 Subscriber Line Audio-Processing Circuit
- Am7950 SLIC

COMMUNICATIONS
Am7990 Family Ethernet Node

Advanced Micro Devices has developed a set of MOS and Bipolar high performance integrated circuits designed to minimize the cost of connecting multivendor devices to an Ethernet bus. This family is designed to provide in the minimum package count, all the logic, protocol and control functions required to interface all the popular 16-bit processors to an Ethernet local area network.

Am7990 Local Area Network Controller for Ethernet (LANCE)

- Buffer management
- On board DMA
- Limit Error Detection
- Address Detection
- Line Access Protocol (CSMA/CD)
- Collision handling

Am7991 Serial Interface Adaptor (SIA)

- Manchester encoding/decoding
- Differential to TTL signal conversion
- Transceiver cable interface

Am79XX Ethernet Transceiver

- Collision detection
- Line protection

Key System Level Features

16-Bit Bus Interface

Compatible with

- **Z8000**
- **8086**
- **68000**
- **LSI-II**

Broad Range of Diagnostics

Alternate Sourced

Meets the Ethernet Specification

Ethernet Data Link Layer Support

- Buffer management
- Data encapsulation
- Framing and packet control
- CRC generation/check
- Serial/deserialization

Ethernet Physical Link Layer Support

- Data rate: 10 Mb/s
- Carrier-sense multiple-access with collision detection
- Transceiver interface compatibility

Advanced Micro Devices

COMMUNICATIONS
Am7990 Family Ethernet Node
System Overview

Advanced Micro Devices is introducing a set of LSI devices that provides the Ethernet system designer, and designers of Ethernet compatible products, a low cost physical and link level interface to the Ethernet Bus.

The Am7990 Ethernet interface family is being designed using a combination of MOS and IMOX™ bipolar technologies. This family consists of the Am7990 Local Area Network Controller for Ethernet (LANCE), and the Am7991 Serial Interface Adapter (SIA). As shown in Figure 1, the Am7990 family provides the complete interface between the device System Bus and the Ethernet Transceiver Cable.

The Am7990 LANCE is a 10M-bit/sec MOS device in a 48-pin package, optimized to perform the link level Ethernet protocol. The CSMA/CD network access, memory management (onboard DMA), error reporting, packet handling, and microprocessor interface functions also reside in the LANCE.

The Am7991 Serial Interface Adaptor provides Manchester encoding and decoding of the serial bit stream and interfaces the TTL output of the LANCE to the differential inputs of the transceiver. It has an on board phase locked loop to recover clock from an incoming signal and can use an external crystal oscillator or TTL inputs to provide clock for transmission.

Coupling the Ethernet Node to the Ethernet Cable requires a transceiver. Commercially available board or module transceivers can be used with the LANCE and SIA. Advanced Micro Devices has a monolithic transceiver in an early phase of development which should lower the cost significantly in this area as well.

BASIC SYSTEM OPERATION

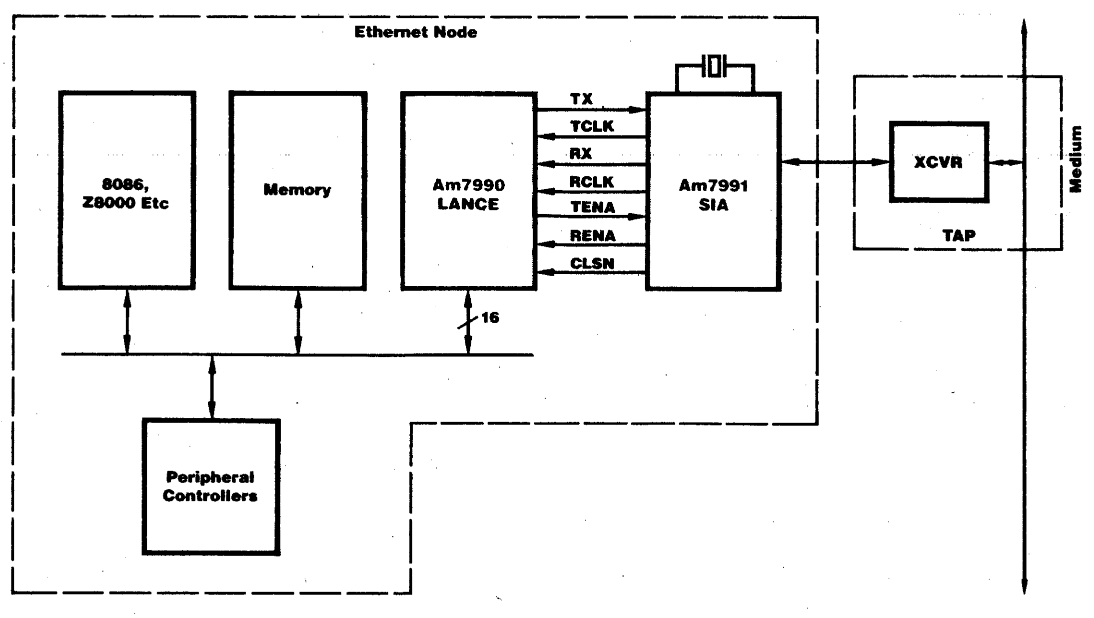
Ethernet is a send and receive half duplex system. The node must function in either transmit or receive mode at any instant in time. Before transmission the node must be sure there is no contention for the bus. The Ethernet CSMA/CD network access algorithm is implemented completely within the LANCE. In addition to listening for a clear coax before transmitting, Ethernet handles collisions in a predetermined way. Should two nodes attempt to transmit at the same time, the signals will collide and the data on the coax will be garbled. The transmitting nodes listen while they transmit and detect the collision. Both continue to transmit for a predetermined length of time to "jam" the network, insuring all nodes have recognized the collision. The transmitting nodes then delay a random amount of time according to the "truncated binary backoff" algorithm implemented in the LANCE, before attempting to transmit again. This minimizes the possibility of collision on retransmission.

TRANSMIT MODE

In the transmit mode, the LANCE initiates a DMA cycle to access data from a transmit buffer. It prefaces the data with a preamble, and sync pattern then calculates and appends a 32-bit CRC.

This packet is transmitted serially to the SIA. The Manchester encoder in the SIA takes the transmitted data from the LANCE and creates the Manchester encoded differential signals TRANSMIT+ and TRANSMIT− to drive the Transceiver cable. These differential signals are coupled through the transceiver cable, transceiver and on to the Ethernet coaxial cable.

Figure 1. Ethernet Node Architecture



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COMMUNICATIONS
Am7990 Family Ethernet Node

RECEIVE MODE

When carrier is present on the Ethernet coax, the Transceiver will create the differential signals RECEIVE+ and RECEIVE−. These inputs to the SIA are decoded by the Manchester decoder. A phase locked loop synchronizes to the Ethernet Preamble, allowing the decoder to recover clock and data from the encoded signals. These two signals are supplied to the LANCE as the TTL signals RECEIVE DATA and RECEIVE CLOCK. In addition, the SIA creates the signal CARRIER PRESENT while it is receiving data from the cable, indicating to the LANCE that receive data and clock are available. When these signals reach the LANCE, the CRC is calculated and compared to the CRC checksum at the end of the packet. If the calculated CRC doesn't agree with the packet CRC an error bit is set and an interrupt generated to the microprocessor.

ADDRESSING

There are three addressing modes. The first is physical addressing which requires a comparison of the 48-bit destination address in the packet with the node address programmed into the LANCE during initialization. The second mode is multi-cast addressing. This mode can be useful when sending packets to all of one type of a device simultaneously on the network, or for a broadcast situation where all nodes on the network receive the packet. In the final "promiscuous" mode of operation, a node will accept all packets on the coax regardless of their destination address.

ERROR REPORTING

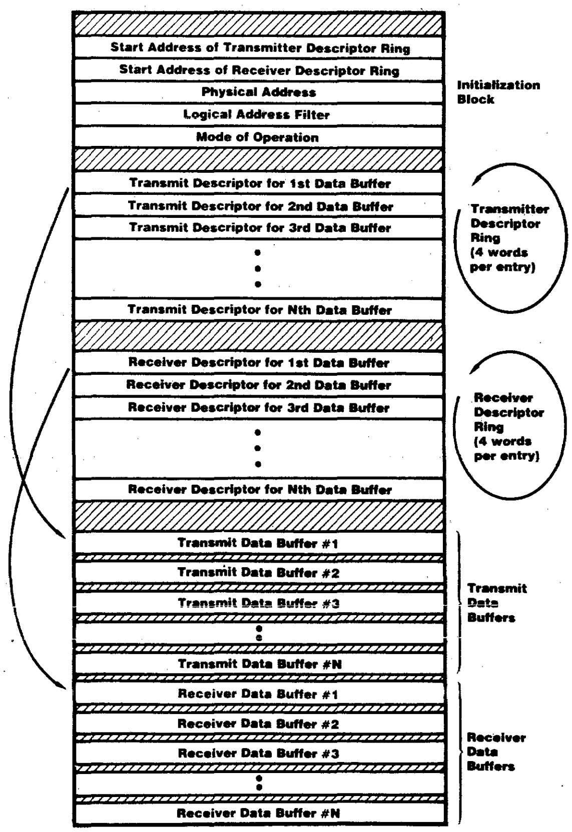
Extensive error reporting is provided by the LANCE through microprocessor interrupt and error bits in a status register. The following are the significant error conditions:

- CRC error on receive
- Babbling error
- Missed packet
- Memory error

BUFFER MANAGEMENT

A key feature of the LANCE and it's on board DMA channel is the flexibility and speed of communication between the LANCE and the host microprocessor through common memory locations. The basic organization of the buffer management consists of circular task queues called descriptor rings for transmit and receive operations. Up to 128 tasks may be queued on a descriptor ring awaiting execution by the LANCE. (Figure 2)

Figure 2. LANCE/Processor Memory Interface



MMC-105

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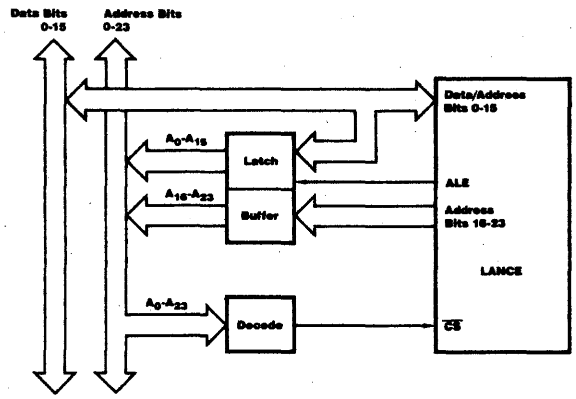
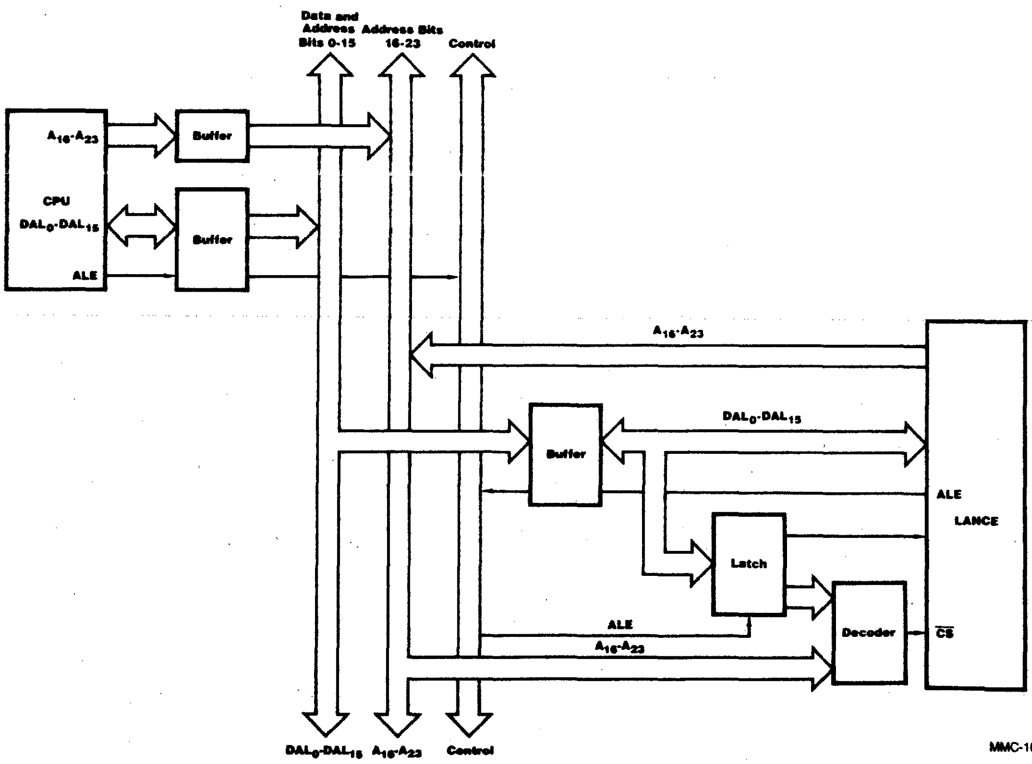
MICROPROCESSOR INTERFACE

The parallel interface of the LANCE has been designed to be "friendly" or easy to interface to a variety of popular 16-bit microprocessors. These microprocessors include the 68000, Z8000, 8086, and LSI-II devices.

The LANCE has a 24-bit wide linear address space when it is in the Bus Master Mode allowing it to DMA directly into the entire address space of the above microprocessors. The LANCE interfaces with both multiplexed and demultiplexed data busses (Figure 3) and features control signals for address/data bus transceivers.



a) Demultiplexed Bus



b) Multiplexed Bus System Overview

Figure 3.

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COMMUNICATIONS
Am7990 Family Ethernet Node
IN DEVELOPMENT

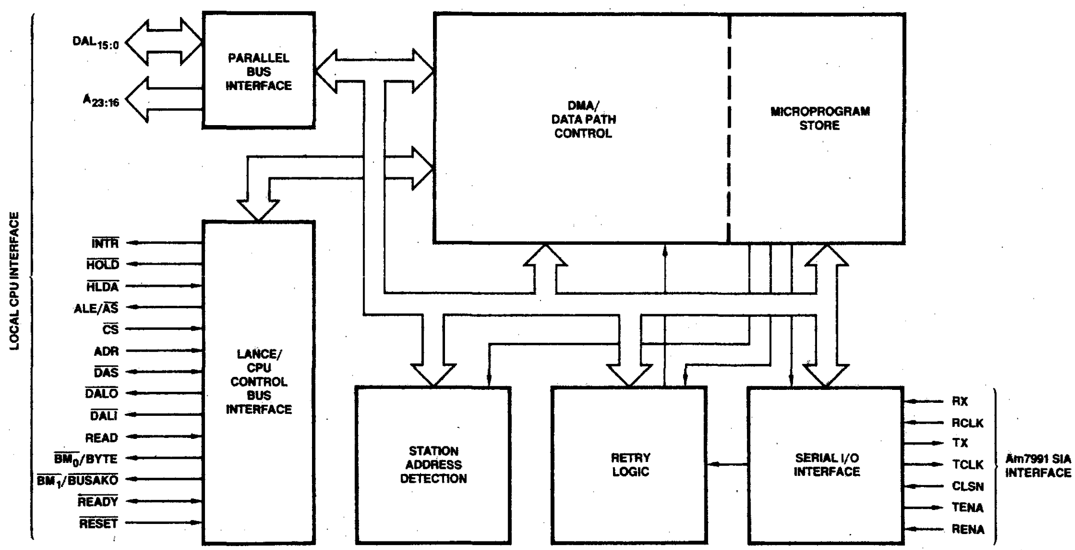
DISTINCTIVE CHARACTERISTICS

- IEEE 802.3 compatible
- Easily interfaced to 8086, 68000, Z8000, LSI-II microprocessors
- On-board DMA and buffer management
- 24-bit wide linear addressing (Bus Master Mode)
- Network and packet error reporting
- Diagnostic Routines
  - Internal/external loop back
  - CRC logic check
  - Time domain reflectometer

GENERAL DESCRIPTION

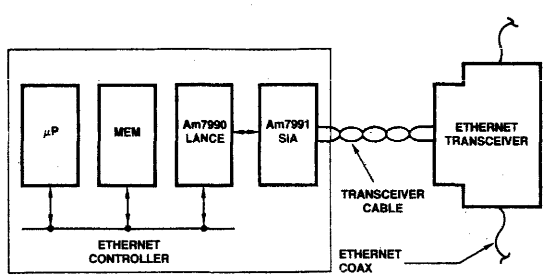
The Am7990 Local Area Network Controller for Ethernet (LANCE) is a 48-pin VLSI device designed to greatly simplify interfacing a microcomputer or minicomputer to an Ethernet Local Area Network. This chip, in conjunction with the Am7991 Serial Interface Adapter (SIA) and closely coupled local memory and microprocessor, is intended to provide the user with a complete interface module for an Ethernet network. The Am7990 is designed using a scaled N-Channel MOS technology and is compatible with a variety of microprocessors. On-board DMA, advanced buffer management and extensive error reporting and diagnostics facilitate design and improve system performance.

LANCE BLOCK DIAGRAM



03378B-5

TYPICAL ETHERNET NODE



03378B-6

COMMUNICATIONS
Am7990 Family Ethernet Node

PIN DEFINITIONS

DAL_{00} – DAL_{15} — **Data/Address Lines (Input/Output 3-State).** The time multiplexed Address/Data bus. During the address portion of a memory transfer, $DAL_{00}-DAL_{15}$ contains the lower 16 bits of the memory address. The upper 8 bits of address are contained in $A_{16}-A_{23}$.

During the data portion of a memory transfer, $DAL_{00}-DAL_{15}$ contains the read or write data, depending on the type of transfer.

The LANCE drives these lines as a Bus Master and as a Bus Slave.

$A_{16}-A_{23}$ — **High Order Address Bus (Output 3-State).** The additional address bits necessary to extend the DAL lines to access a 24-bit address. These lines are driven as a Bus Master only.

READ — **(Input/Output 3-State).** Indicates the type of operation to be performed in the current bus cycle. This signal is an output when the LANCE is a Bus Master.

High – Data is taken off the DAL by the chip
Low – Data is placed on the DAL by the chip

The signal is an input when the LANCE is a Bus Slave

High – Data is placed on the DAL by the chip
Low – Data is taken off the DAL by the chip

$\overline{BM_0}$/BYTE $\overline{BM_1}$/$\overline{BUSAKO}$ — I/O pins 15 and 16 are programmable through bit (00) of CSR_3.

If CSR_3 (00) BCON = 0
I/O PIN 15 = $\overline{BM_0}$ (Output 3-state)
I/O PIN 16 = $\overline{BM_1}$ (Output 3-state)

$\overline{BM_0}$, $\overline{BM_1}$ (Byte Mask). This indicates the byte(s) on the DAL are to be read or written during this bus transaction. The LANCE drives these lines only as a Bus Master. It ignores the Byte Mask lines when it is a Bus Slave, and assumes word transfers.

Byte selection using Byte Mask is done as described by the following table.

$\overline{BM_1}$	$\overline{BM_0}$	
LOW	LOW	Whole Word
LOW	HIGH	Upper Byte
HIGH	LOW	Lower Byte
HIGH	HIGH	None

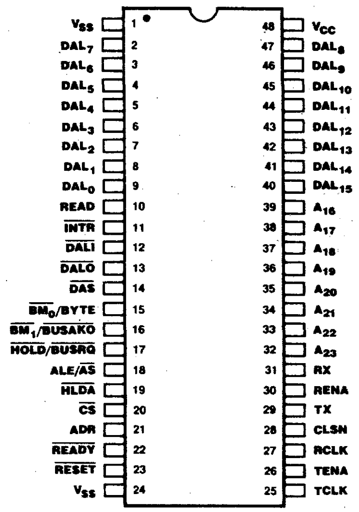
If CSR_3 (00) BCON = 1
I/O PIN 15 = BYTE (Output 3-state)
I/O PIN 16 = $\overline{BUSAKO}$ (Output)

Byte selection may also be done using the BYTE line and DAL_{00} line, latched during the address portion of the bus cycle. The LANCE drives BYTE only as a Bus Master and ignores it when a Bus Slave selection is done (similar to $\overline{BM_0}$, $\overline{BM_1}$).

Byte selection is done as outlined in the following table.

BYTE	DAL_{00}	
LOW	LOW	Whole Word
LOW	HIGH	Illegal Condition
HIGH	LOW	Lower Byte
HIGH	HIGH	Upper Byte

LANCE PIN DESCRIPTION
D-48-1



Note: Pin 1 is marked for orientation.

$\overline{BUSAKO}$ is a bus request daisy chain output. If the chip is not requesting the bus and it receives $\overline{HLDA}$, $\overline{BUSAKO}$ will be driven low. If the LANCE is requesting the bus when it receives $\overline{HLDA}$, $\overline{BUSAKO}$ will remain high.

Byte Swapping

In an effort to be compatible with the variety of 16-bit microprocessors available to the designer, the LANCE may be programmed to swap the position of the upper and lower order bytes on data involved in transfers with the internal FIFO.

Byte swapping is done when BSWP = 1. The most significant byte of the word in this case will appear on DAL lines 7-0 and the least significant byte on DAL lines 15-8.

When BYTE = H (indicating a byte transfer) the table indicates on which part of the 16 bit data bus the actual data will appear.

Whenever byte swap is activated, the only data that is swapped is data traveling to and from the FIFO.

Signal Line \ Mode Bits	BSWP = 0 and BCON = 1	BSWP = 1 and BCON = 1
BYTE = L and DAL_{00} = L	Word	Word
BYTE = L and DAL_{00} = H	Illegal	Illegal
BYTE = H and DAL_{00} = H	Upper Byte	Lower Byte
BYTE = H and DAL_{00} = L	Lower Byte	Upper Byte

$\overline{CS}$ — **Chip Select (Input).** Indicates, when asserted, that the LANCE is the slave device of the data transfer. $\overline{CS}$ must be valid throughout the data portion of the bus cycle.

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COMMUNICATIONS
Am7990 Family Ethernet Node

ADR — **Register Address Port Select (Input).** When LANCE is slave, ADR indicates which of the two register ports is selected. ADR LOW selects register data port, ADR HIGH selects register address port. ADR must be valid throughout the data portion of the bus cycle and is only used by the LANCE when CS is low.

ALE/$\overline{\text{AS}}$ — **Address Latch Enable (Output 3-State).** Used to demultiplex the DAL lines and define the address portion of the bus cycle. This I/O pin is programmable through bit (01) of CSR$_3$.

As ALE, (CSR$_3$ (01), ACON = 0) the signal transitions from a HIGH to a LOW during the address portion of the transfer and remains low during the data portion. ALE can be used by a Slave device to control a latch on the bus address lines. When ALE is high the latch is open and when ALE goes low the latch is closed.

As $\overline{\text{AS}}$ (CSR$_3$ (01), ACON = 1), the signal pulses LOW during the address portion of the bus transaction. The low to high transition of AS can be used by a slave device to strobe the address into a register.

The LANCE drives the ALE/$\overline{\text{AS}}$ line only as a Bus Master.

$\overline{\text{DAS}}$ — **Data Strobe (Input/Output 3-State).** Defines the data portion of the bus transaction. $\overline{\text{DAS}}$ is high during the address portion of a bus transaction and low during the data portion. The low to high transition can be used by a Slave device to strobe bus data into a register. $\overline{\text{DAS}}$ is driven only as a Bus Master.

$\overline{\text{DALO}}$ — **Data/Address Line Out (Output 3-State).** An external bus transceiver control line. $\overline{\text{DALO}}$ is asserted when the LANCE drives the DAL lines. $\overline{\text{DALO}}$ will be low only during the address portion if the transfer is a READ. It will be low for the entire transfer if the transfer is a WRITE. $\overline{\text{DALO}}$ is driven only when LANCE is a Bus Master.

$\overline{\text{DALI}}$ — **Data/Address Line In (Output 3-State).** An external bus transceiver control line. $\overline{\text{DALI}}$ is asserted when the LANCE reads from the DAL lines. It will be low during the data portion of a READ transfer and remain high for the entire transfer if it is a WRITE. $\overline{\text{DALI}}$ is driven only when LANCE is a Bus Master.

$\overline{\text{HOLD}}$/$\overline{\text{BUSRQ}}$ — **Bus Hold Request (Output Open Drain).** Asserted by the LANCE when if requires access to memory. $\overline{\text{HOLD}}$ is held LOW for the entire ensuing bus transaction. The function of this pin is programmed through bit (00) of CSR$_3$. Bit (00) of CSR$_3$ is cleared when $\overline{\text{RESET}}$ is asserted.

When CSR$_3$ (00) BCON = 0
I/O pin 17 = $\overline{\text{HOLD}}$ (Output Open Drain)

When CSR$_3$ (00) BCON = 1
I/O pin 17 = $\overline{\text{BUSRQ}}$ (Output Open Drain)

$\overline{\text{BUSRQ}}$ will be asserted only if I/O pin 17 is high prior to assertion.

$\overline{\text{HLDA}}$ — **Bus Hold Acknowledge (Input).** A response to $\overline{\text{HOLD}}$. When $\overline{\text{HLDA}}$ is low in response to the chip's assertion of $\overline{\text{HOLD}}$, the chip is the Bus Master. $\overline{\text{HLDA}}$ deasserts upon the deassertion of $\overline{\text{HOLD}}$.

$\overline{\text{INTR}}$ — **Interrupt (Output Open Drain).** An attention signal that indicates, when active, that one or more of the following CSR$_0$ status flags is set: BABL, MERR, MISS, RINT, TINT or IDON. $\overline{\text{INTR}}$ is enabled by bit 06 of CSR$_0$ (INEA = 1).

RX — **Receive (Input).** Receive Input Bit Stream.

TX — **Transmit (Output).** Transmit Output Bit Stream.

TENA — **Transmit Enable (Output).** Transmit Output Bit Stream enable. A level-asserted with the Transmit Output Bit Stream, TX, to enable the external transmit logic.

RCLK — **Receive Clock (Input).** A 10MHz square wave synchronized to the Receive data and only active while receiving an Input Bit Stream.

CLSN — **Collision (Input).** A logical input that indicates that a collision is occurring on the channel.

RENA — **Receive Enable (Input).** A logical input that indicates the presence of carrier on the channel.

TCLK — **Transmit Clock (Input).** 10MHz clock.

$\overline{\text{READY}}$ — **(Input/Output Open Drain).** When the LANCE is a Bus Master, $\overline{\text{READY}}$ is an asynchronous acknowledgement from the bus memory that it will accept data in a WRITE cycle or that it has put data on the DAL lines in a READ cycle.

As a Bus Slave, the LANCE asserts $\overline{\text{READY}}$ when it has put data on the DAL lines during a READ cycle or is about to take data off the DAL lines during a write cycle. $\overline{\text{READY}}$ is a response to $\overline{\text{DAS}}$ and will return HIGH after $\overline{\text{DAS}}$ has gone HIGH. $\overline{\text{READY}}$ is an input when the LANCE is a Bus Master and an output when the LANCE is a Bus Slave.

$\overline{\text{RESET}}$ — **(Input).** Bus Reset Signal. Causes the LANCE to cease operation and enter an idle state.

V_{CC} — Power supply pin +5 volts ± 5%.

V_{SS} — Ground. Pins 1 and 24 should be connected together externally, as close to the chip as possible.

FUNCTIONAL DESCRIPTION

The parallel interface of the Local Area Network Controller for Ethernet (LANCE) has been designed to be "friendly" or easy to interface to a variety of popular 16-bit microprocessors. These microprocessors include the following: Z8000, 8086, 68000 and LSI-11. The LANCE has a 24-bit wide linear address space when it is in the Bus Master Mode allowing it to DMA directly into the entire address space of the above microprocessors. A programmable mode of operation allows byte addressing in one of two ways: A Byte/Word control signal compatible with the 8086 and Z8000, or an Upper Data Strobe and Lower Data Strobe signal compatible with microprocessors such as the 68000. A programmable polarity on the Address Strobe signal eliminates the need for external logic. The LANCE interfaces with both multiplexed and demultiplexed data busses and features control signals for address/data bus transceivers.

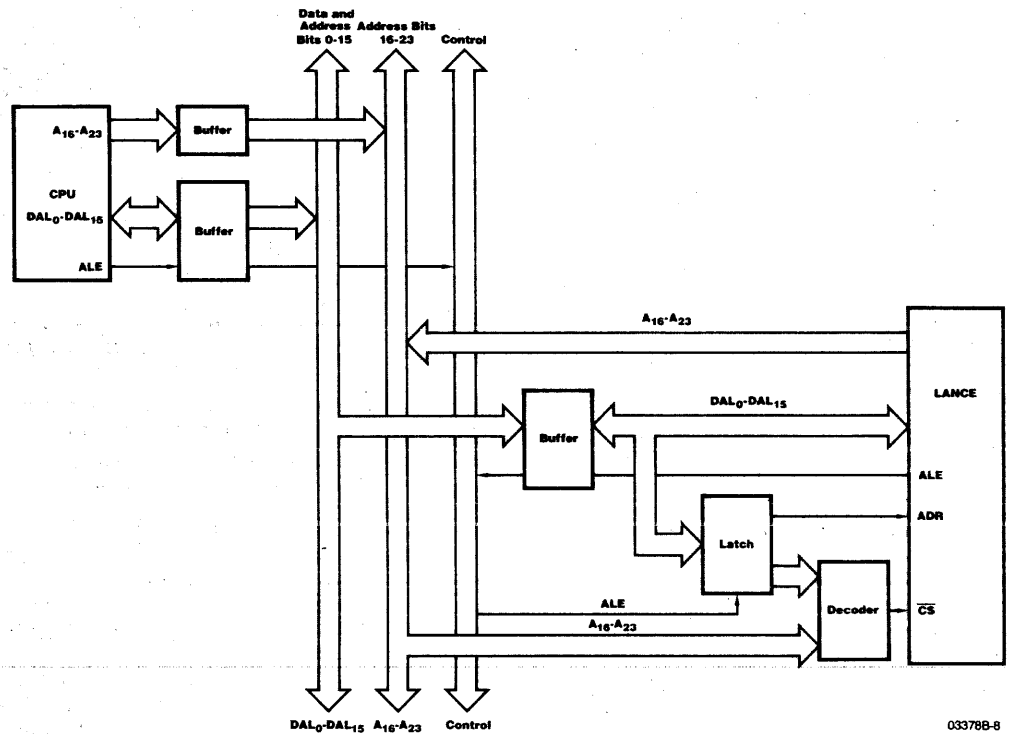
During initialization, the CPU loads the starting address of the initialization block into two internal control registers. The LANCE has four internal control and status registers ($CSR_{0,1,2,3}$) which are used for various functions such as the loading of the initialization block address, different programming modes and status conditions. The host processor communicates with the LANCE during the initialization phase, for demand transmission and periodically to read the status bits following interrupts. All other transfers to and from the memory are handled as DMA under microword control.

Interrupts to the microprocessor are generated by the LANCE: 1) upon completion of its initialization routine, 2) the reception of a packet, 3) the transmission of a packet, 4) transmitter timeout error, 5) a missed packet and 6) memory error.

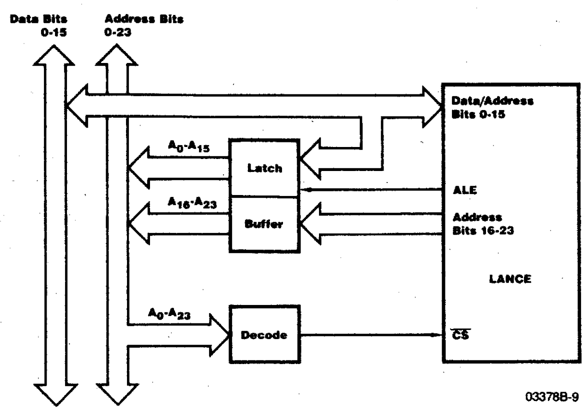
The cause of the interrupt is ascertained by reading CSR_0. Bit (06) of CSR_0, (INEA) enables or disables interrupts to the microprocessor. In systems where polling is used in place of

Figure 1. LANCE/CPU Interfacing

a) Multiplexed Bus



b) Demultiplexed Bus



interrupts, bit (07) of CSR_0 (INTR) indicates an interrupt condition.

The basic operation of the LANCE consists of two distinct modes: transmit and receive. In the transmit mode the LANCE chip directly accesses data in a transmit buffer in memory. It prefaces the data with a preamble, sync pattern, and calculates and appends a 32-bit CRC. This packet is then ready for transmission to the Am7991 SIA.

In the receive mode, packets are sent via the SIA to the LANCE. The packet is loaded into buffer memory. A CRC is calculated and compared with the CRC appended to the data packet. If the calculated CRC checksum doesn't agree with the packet CRC, an error bit is set.

ADDRESSING

Packets can be received using 3 different destination addressing schemes: physical, logical and promiscuous.

The first type is a full comparison of the 48-bit destination address in the packet with the node address that was programmed into the LANCE during an initialization cycle. There are two types of logical address, one is group type mask where the 48-bit address in the packet is put through a hash filter in order to map the 48-bit physical addresses into 1 of 63 logical groups. This mode can be useful if sending packets to all of a particular type of device simultaneously (i.e., send a packet to all file servers or all printer servers). The second logical address is a multicast address where all nodes on the network receive the packet. The last receive mode of operation is the so-called "promiscuous mode" in which a node will accept all packets on the coax regardless of their destination address.

COLLISION DETECTION AND IMPLEMENTATION

The Ethernet CSMA/CD network access algorithm is implemented completely within the LANCE. In addition to listening for a clear coax before transmitting, Ethernet handles collisions in a predetermined way. Should two transmitters attempt to seize the coax at the same time they will collide and the data on the coax will be garbled. The transmitting nodes listen while they transmit; detect the collision, then continue to transmit for a predetermined length of time to "jam" the network and ensure that all nodes have recognized the collision. The transmitting nodes then delay a random amount of time according to the Ethernet "truncated binary backoff" algorithm in order that the colliding nodes don't try to repeatedly access the network at the same time. Up to 16 attempts to access the network are made by the LANCE before reporting back an error due to excessive collisions.

ERROR REPORTING AND DIAGNOSTICS

Extensive error reporting is provided by the LANCE. Errors conditions reported relate either to the network as a whole or to data packets. Network-related errors are recorded as flags in the CSRs and are examined by the CPU following interrupt. Packet related errors are written into descriptor entries corresponding to the packet.

System errors include:

- Babbling Transmitter
  - Transmitter attempting to transmit more than 1518 data bytes.
- Collision
  - Collision detection circuitry nonfunctional
- Missed packet
  - Insufficient buffer space
- Memory timeout
  - Memory response failure

Packet related errors:

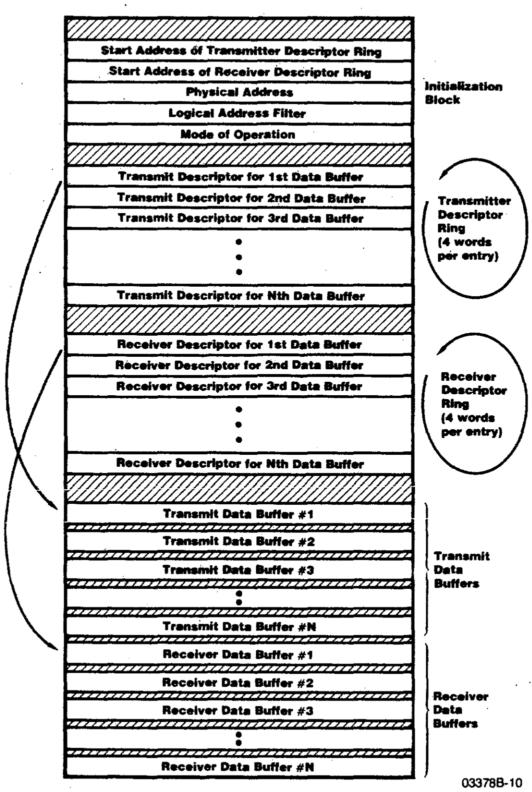
- CRC
  - Invalid data
- Framing
  - Packet did not end on a byte boundary
- Overflow/Underflow
  - Indicates abnormal latency in servicing a DMA request
- Buffer
  - Insufficient buffer space available

The LANCE performs several diagnostic routines which enhance the reliability and integrity of the system. These include a CRC logic check and two loop back modes (internal/external). Errors may be introduced into the system to check error detection logic. A Time Domain Reflectometer is incorporated into the LANCE to aid system designers locate faults in the Ethernet cable. Shorts and opens manifest themselves in reflections which are sensed by the TDR.

BUFFER MANAGEMENT

A key feature of the LANCE and its on-board DMA channel is the flexibility and speed of communication between the LANCE and the host microprocessor through common memory locations. The basic organization of the buffer management is a circular queue of tasks in memory called descriptor rings as shown in Figure 2. There are separate descriptor rings to describe transmit and receive operations. Up to 128 tasks may be queued up on a descriptor ring awaiting execution by the LANCE. Each entry in a descriptor ring holds a pointer to a data memory buffer and an

Figure 2. LANCE/Processor Memory Interface



entry for the length of the data buffer. Data buffers can be chained or cascaded in order to handle a long packet in multiple data buffer areas. The LANCE searches the descriptor rings in a "look ahead manner" to determine the next empty buffer in order to chain buffers together or to handle back to back packets. As each buffer is filled, an "own" bit is reset allowing the host processor to process the data in the buffer.

LANCE INTERFACE

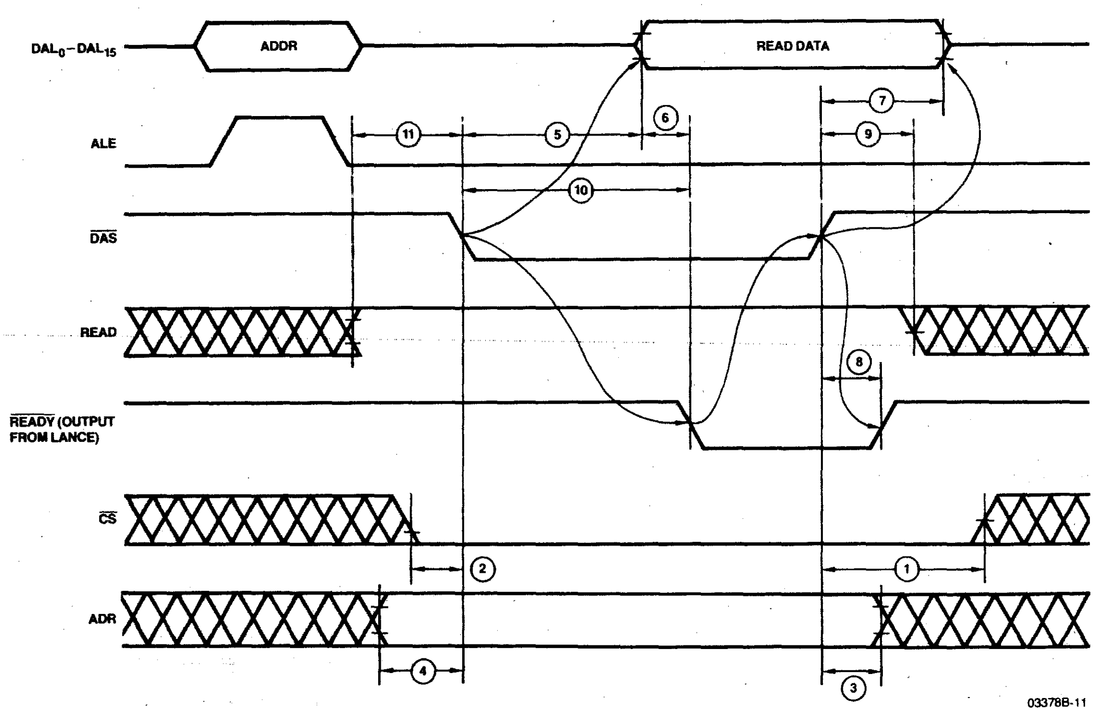
CSR bits such as ACON, BCON and BSWP are used for programming the pin functions used for different interfacing schemes. For example, ACON is used to program the polarity of the Address Strobe signal (ALE/$\overline{AS}$).

BCON is used for programming the pins for handling either the BYTE/$\overline{WORD}$ method for addressing word organized, byte addressable memories where the BYTE signal is decoded along with the least significant address bit to determine upper or lower byte, or an explicit scheme in which two signals labeled as BYTE MASK ($\overline{BM_0}$ and $\overline{BM_1}$) indicate which byte is addressed. When the BYTE scheme is chosen the $\overline{BM_1}$ pin can be used for performing the function $\overline{BUSAKO}$.

BCON is also used to program pins for different DMA modes. In a daisy chain DMA scheme, 3 signals ($\overline{BUSRQ}$, $\overline{HLDA}$, $\overline{BUSAKO}$), are used. In systems using a DMA controller for arbitration, only $\overline{HOLD}$ and $\overline{HLDA}$ are used.

All data transfers from the LANCE in the Bus Master mode are timed by ALE, $\overline{DAS}$ and $\overline{READY}$. The automatic adjustment of the LANCE cycle by the $\overline{READY}$ signal allows synchronization with variable cycle time memory due either to memory refresh or to dual port access. Bus cycles are a minimum of 600ns in length and can be increased in 100ns increments.

BUS SLAVE WRITE TIMING



Note: 1. There are two types of delays which depend on which internal register is accessed.
Typ 1 refers to access of CSR_0, CSR_1 and RAP.
Typ 2 refers to access of CSR_1 and CSR_2.

COMMUNICATIONS
Am7990 Family Ethernet Node

READ SEQUENCE

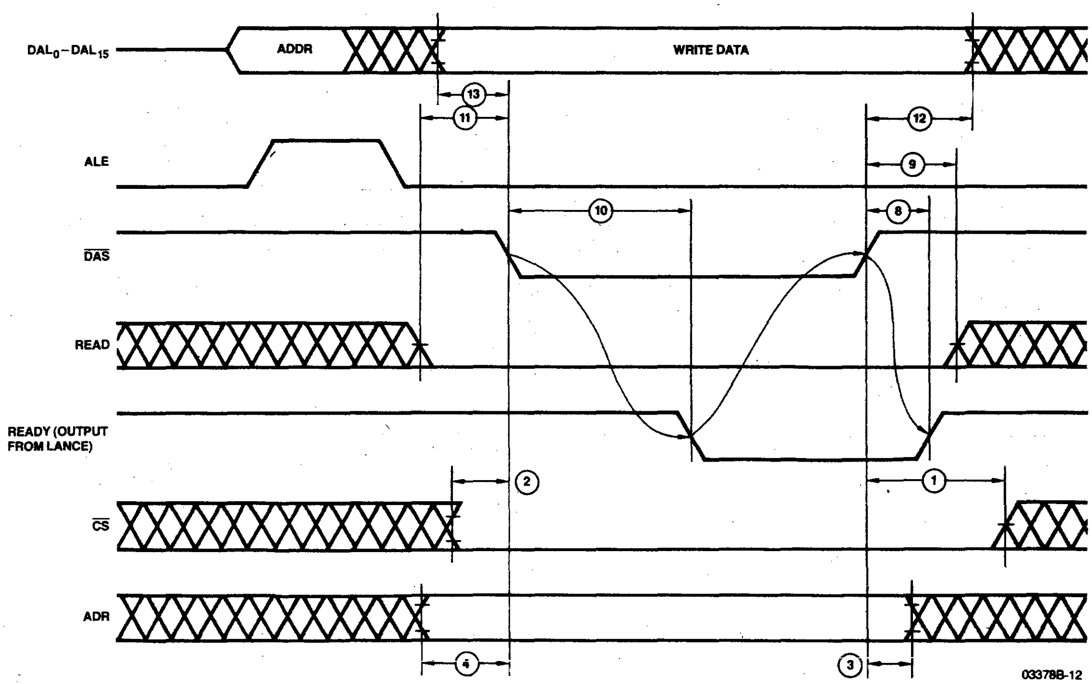
The read cycle is begun by valid addresses being placed on $DAL_{00}-DAL_{15}$ and $A_{16}-A_{23}$. The BYTE MASK signals are placed valid to indicate a word, upper byte or lower byte memory reference and READ indicates the type of cycle. ALE or $\overline{AS}$ are pulsed and the trailing edge of either can be used to latch addresses. $DAL_{00}-DAL_{15}$ go into a 3-state mode and $\overline{DAS}$ falls low to signal the beginning of the memory access. The memory responds by placing $\overline{READY}$ low to indicate that the DAL lines have valid data. The LANCE then latches memory data on the rising edge of $\overline{DAS}$ which in turn ends the memory cycle and $\overline{READY}$ returns high.

The bus transceiver controls, $\overline{DALI}$ and $\overline{DALO}$, are used to control the bus transceivers. $\overline{DALI}$ signals to strobe data toward the LANCE and $\overline{DALO}$ signals to strobe data or addresses away from the LANCE. During a read cycle $\overline{DALO}$ goes inactive before $\overline{DALI}$ becomes active to avoid "spiking" of the bus transceivers.

WRITE SEQUENCE

The write cycle is very similar except that the $DAL_{00}-DAL_{15}$ lines change from containing addresses to data after ALE or $\overline{AS}$ go inactive $\overline{DAS}$ goes active after data is valid on the bus. Data to memory is held valid after $\overline{DAS}$ goes inactive.

BUS SLAVE READ TIMING



Advanced Micro Devices

COMMUNICATIONS
Am7990 Family Ethernet Node

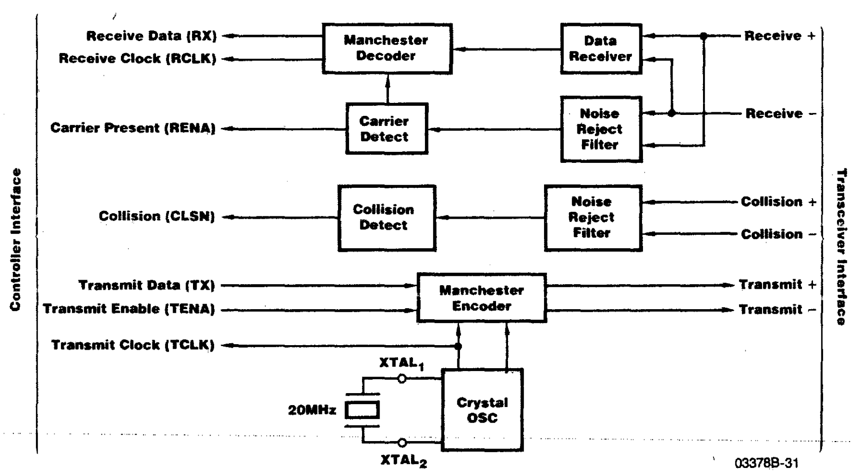
DISTINCTIVE CHARACTERISTICS

- Compatible with Ethernet/IEEE 802.3 specifications
- Crystal controlled Manchester Encoder
- Manchester Decoder acquires clock and data within six bit times with an accuracy of ±3ns
- Guaranteed carrier detection and collision detection threshold limits
  - Carrier/collision detected for greater than −300mV
  - No carrier/collision for less than −175mV
- Input signal conditioning rejects transient noise
  - Transients <10ns for collision detector inputs
  - Transients <16ns for carrier detector inputs
- Receiver decodes Manchester data with up to ±20ns clock jitter (at 10MHz)
- TTL comaptible host interface
- Transmit accuracy ±0.01% (without adjustments)

GENERAL DESCRIPTION

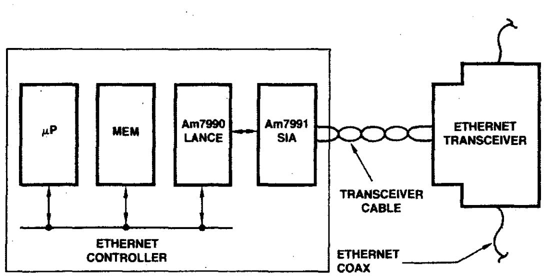
The Am7991 Serial Interface Adapter (SIA) is a Manchester Encoder/Decoder compatible with both Ethernet and IEEE-802.3 specifications. In an Ethernet/IEEE-802.3 application the Am7991 interfaces the Am7990 Local Area Network Controller for Ethernet (LANCE) to the Ethernet transceiver cable, acquires clock and data within 6 bit-times and decodes Manchester data with up to ±20ns phase jitter at 10MHz. SIA provides both guaranteed signal threshold limits and transient noise suppression circuitry in both data and collision paths to minimize false start conditions.

BLOCK DIAGRAM
Serial Interface Adapter (SIA)



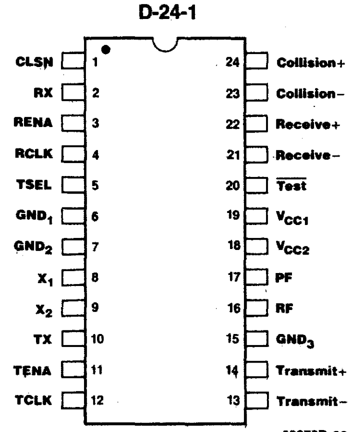
03378B-31

TYPICAL ETHERNET NODE



03378B-16

CONNECTION DIAGRAM – Top View
D-24-1



03378B-32

LINEAR

Advanced Micro Devices

AMI®

A Subsidiary of Gould Inc.

DTMF TONE GENERATOR

Features

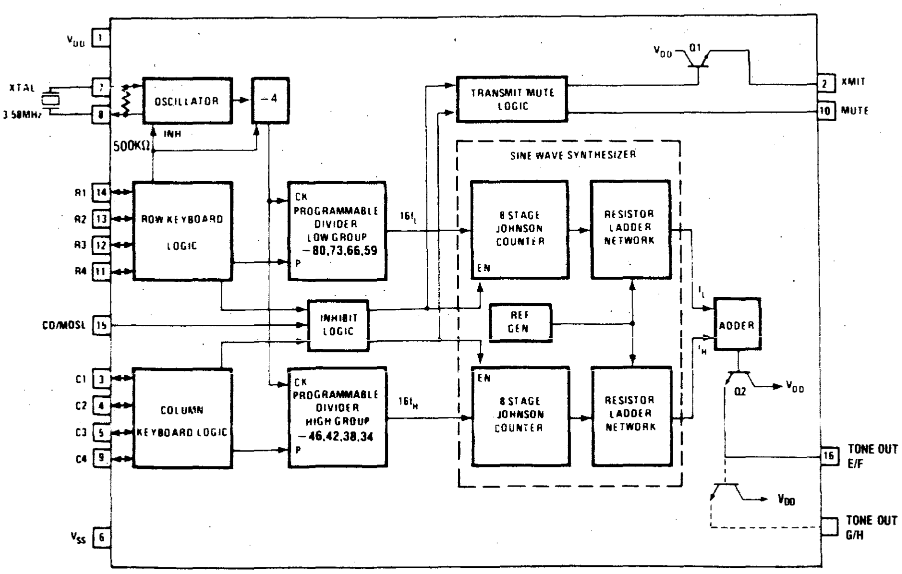
- ☐ Low Output Tone Distortion: 7%
- ☐ Wide Operating Supply Voltage Range: 2.5 to 10 Volts
- ☐ Oscillator Bias Resistor On-Chip
- ☐ Can be Powered Directly from Telephone Line or from Small Batteries
- ☐ Interfaces Directly to a Standard Telephone Push-Button or Calculator Type X-Y Keyboard
- ☐ Four Options Available on Pin 15 and Pin 16:
  - Bipolar Output
    - E: Mode Select
    - F: Chip Disable
  - Darlington Output
    - G: Mode Select
    - H: Chip Disable

General Description

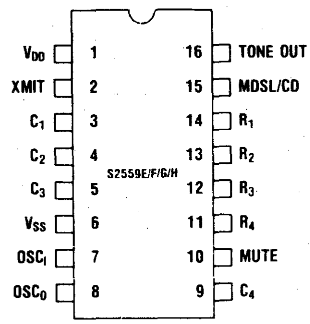
The S2559E, F, G and H are improved members of the S2559 Tone Generator Family. The new devices feature extended operating voltage range, lower tone distortion, and an on-chip oscillator bias resistor. The S2559E and F are pin and functionally compatible with the S2559C and D, respectively.

The S2559 G and H are identical to the E and F, except that there is a Darlington amplifier configuration on the tone out pin, rather than a single bipolar transistor as shown in the block diagram. In many applications this eliminates the need for a transistor in the telephone circuit. Tone distortion in the telephone is also likely to be lower.

Block Diagram



Pin Configuration



LINEAR

American Microsystems, Inc.

DTMF TONE GENERATOR

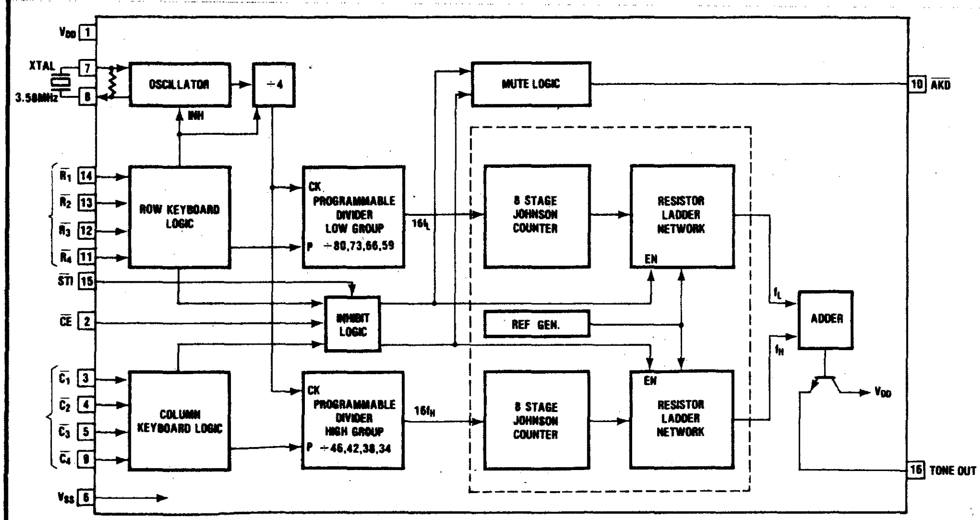
Features

- ☐ Wide Operating Voltage Range: 2.5 to 10 Volts
- ☐ Optimized for Constant Operating Supply Voltages, Typically 3.5V
- ☐ Tone Amplitude Stability is Within ±1.5dB of Nominal Over Operating Temperature Range
- ☐ Low Power CMOS Circuitry Allows Device Power to to be Derived Directly From the Telephone Lines or From Small Batteries
- ☐ Uses TV Crystal Standard (3.58MHz) to Derive All Frequencies Thus Providing Very High Accuracy and Stability
- ☐ Specifically Designed for Electronic Telephone Applications
- ☐ Interfaces Directly to a Standard Telephone Push-Button Keyboard With Common Terminal
- ☐ Low Total Harmonic Distortion
- ☐ Single Tone as Well as Dual Tone Capability
- ☐ Direct Replacement for Mostek MK5089 Tone Generator

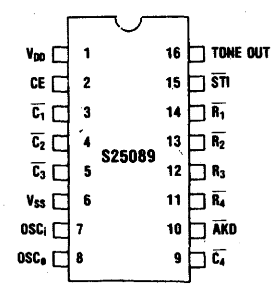
General Description

The S25089 DTMF Generator is specifically designed to implement a dual tone telephone dialing system in applications requiring fixed supply operation and high stability tone output level, making it well suited for electronic telephone applications. The device can interface directly to a standard pushbutton telephone keyboard with common terminal connected to V_{SS} and operates directly from the telephone lines. All necessary dual-tone frequencies are derived from the widely used TV crystal standard providing very high accuracy and stability. The required sinusoidal waveform for the individual tones is digitally synthesized on the chip. The waveform so generated has very low total harmonic distortion. A voltage reference is generated on the chip which is very stable over the operating temperature range and regulates the signal levels of the dual tones to meet the recommended telephone industry specifications.

Block Diagram



Pin Configuration



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S2560A

PULSE DIALER

Features

- ☐ Low Voltage CMOS Process for Direct Operation from Telephone Lines
- ☐ Inexpensive R-C Oscillator Design Provides Better than ± 5% Accuracy Over Temperature and Unit to Unit Variations
- ☐ Dialing Rate Can be Varied by Changing the Dial Rate Oscillator Frequency
- ☐ Dial Rate Select Input Allows Changing of the Dialing Rate by a 2:1 Factor Without Changing Oscillator Components
- ☐ Two Selections of Mark/Space Ratios (33⅓/66⅔ or 40/60)
- ☐ Twenty Digit Memory for Input Buffering and for Redial with Access Pause Capability
- ☐ Mute and Dial Pulse Drivers on Chip
- ☐ Accepts DPCT Keypad with Common Arranged in a 2 of 7 Format; Also Capable of Interface to SPST Switch Matrix

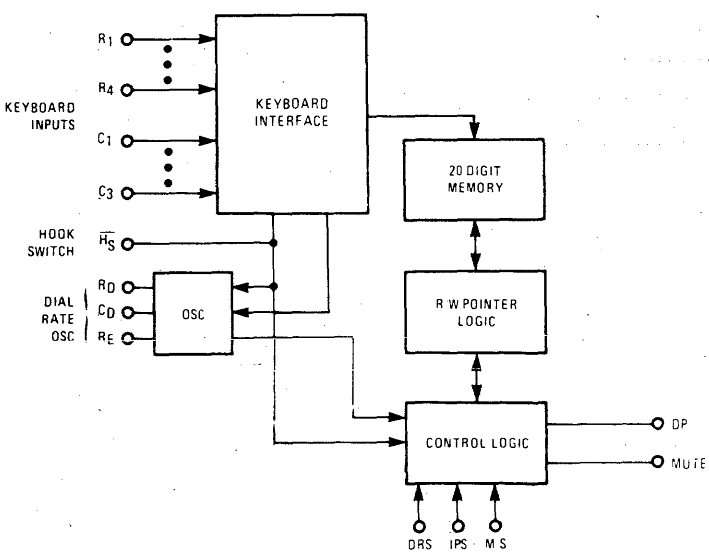
General Description

The S2560A Pulse Dialer is a CMOS integrated circuit that converts pushbutton inputs to a series of pulses suitable for telephone dialing. It is intended as a replacement for the mechanical telephone dial and can operate directly from the telephone lines with minimum interface. Storage is provided for 20 digits, therefore, the last dialed number is available for redial until a new number is entered. IDP is scaled to the dialing rate such as to produce smaller IDP at higher dialing rates. Additionally, the IDP can be changed by a 2:1 factor at a given dialing rate by means of the IDP select input.

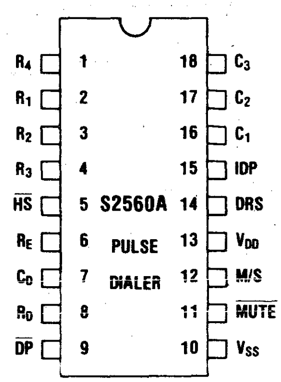
LINEAR

American Microsystems, Inc.

Block Diagram



Pin Configuration

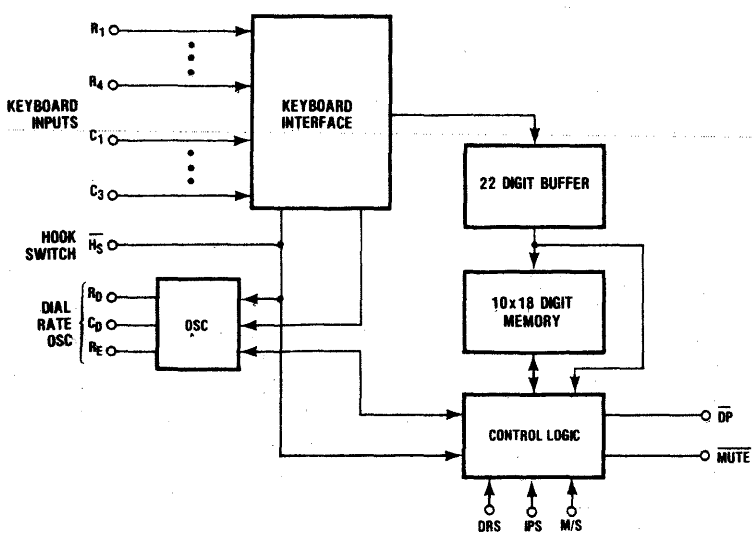


SINGLE CHIP REPERTORY DIALER

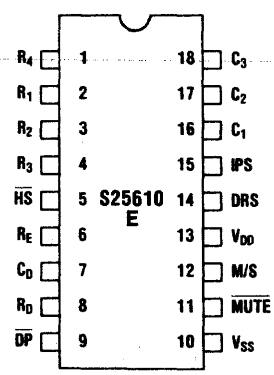
Features

- ☐ Complete Pin Compatibility With S2560A and S2560G Pulse Dialer Allowing Easy Upgrading of Existing Designs.
- ☐ Ten 18-Digit Number Memories Plus Last Number Redial (22 Digit) Memory On Chip.
- ☐ Low Voltage CMOS Process for Direct Operation From Telephone Lines.
- ☐ Inexpensive R-C Oscillator Design With Accuracy Better Than ±5% Over Temperature and Unit-Unit Variations.
- ☐ Independent Select Inputs for Variation of Dialing Rates (10pps/20pps), Mark/Space Ratio (33⅓-66⅔/40-60), Interdigit Pause (400ms/800ms).
- ☐ Can Interface With Inexpensive XY Matrix or Standard 2 of 7 Keyboard With Common. Also Capable of Logic Interface (Active High).
- ☐ Mute and Pulse Drivers On Chip.
- ☐ Call Disconnect by Pushing * and # Keys Simultaneously.

Block Diagram



Pin Configuration



AMI®

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S2561/S2561A/S2561C

TONE RINGER

Features

- ☐ CMOS Process for Low Power Operation
- ☐ Operates Directly from Telephone Lines with Simple Interface
- ☐ Also Capable of Logic Interface for Non-Telephone Applications
- ☐ Provides a Tone Signal that Shifts Between Two Predetermined Frequencies at Approximately 16Hz to Closely Simulate the Effects of the Telephone Bell
- ☐ Push-Pull Output Stage Allows Direct Drive, Eliminating Capacitive Coupling and Provides Increased Power Output
- ☐ 50mW Output Drive Capability at 10V Operating Voltage
- ☐ Auto Mode Allows Amplitude Sequencing such that the Tone Amplitude Increases in Each of the First Three Rings and Thereafter Continues at the Maximum Level
- ☐ Single Frequency Tone Capability

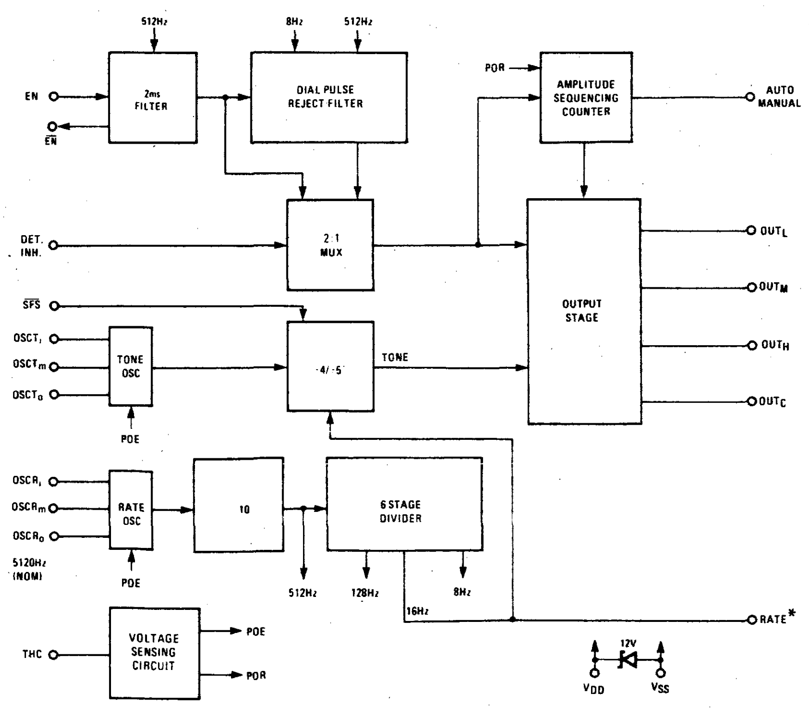
General Description

The S2561 Tone Ringer is a CMOS integrated circuit that is intended as a replacement for the mechanical telephone bell. It can be powered directly from the telephone lines with minimum interface and can drive a speaker to produce sound effects closely simulating the telephone bell.

LINEAR

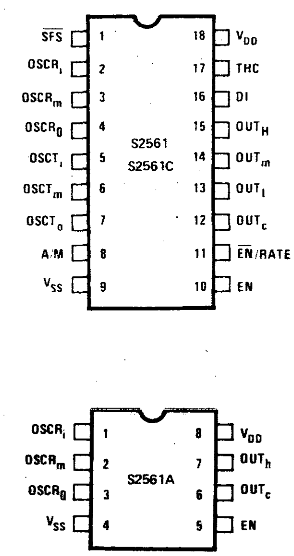
American Microsystems, Inc.

Block Diagram



*OPTIONAL OUTPUT FOR S2561C

Pin Configuration



AMI® A Subsidiary of Gould Inc.

Advanced Product Description **S2550A**

August 1983

TWO TO FOUR WIRE TELEPHONE HYBRID WITH TONE RINGER

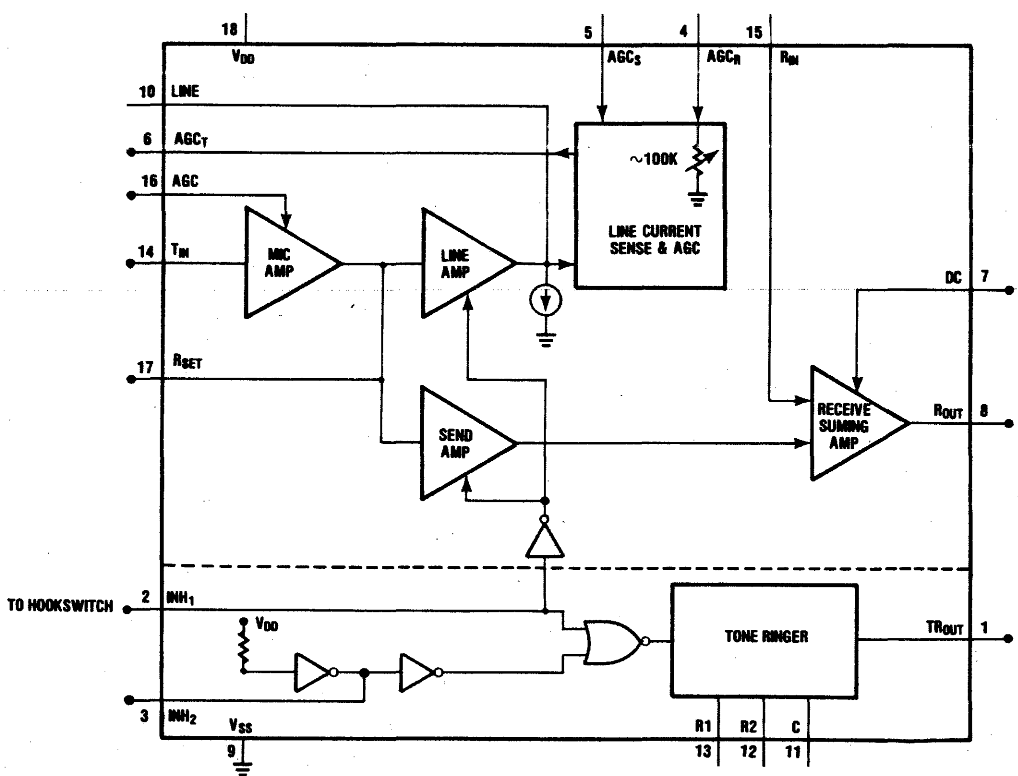
Features

- ☐ Monolithic IC Consisting of the Speech Network and Tone Ringer
- ☐ Interfaces With Inexpensive Condenser Electret Microphone, Electromagnetic Receiver and a Piezoelectric Ringer Transducer
- ☐ Automatic Gain Adjustment for Loop Loss Compensation
- ☐ Low Voltage CMOS Process for Operation Over Varying Loop Lengths and Currents
- ☐ Uses Inexpensive and Non-Critical External Components

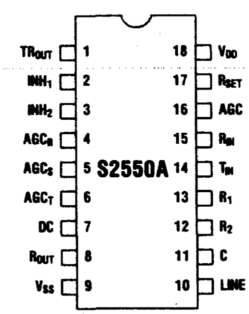
General Description

The S2550A is a monolithic integrated circuit specifically designed for implementing a low cost telephone set circuit. It consists of the hybrid circuit for speech transmission and reception and a tone ringer circuit that generates an audible tone coincident with the incoming ringing signal through a suitable piezoelectric transducer or high impedance speaker.

Functional Block Diagram



Pin Configuration



LINEAR

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AMI

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S3522

BELL 212A/CCITT V.22 COMPATIBLE MODEM FILTER WITH EQUALIZER

Features

- ☐ Bell 212A/V.22 Compatible
- ☐ Usable for Bell 103/113 Applications
- ☐ High and Low Band Filters with Compromise Group Delay Equalizers
- ☐ Originate/Answer Operating Modes
- ☐ Buffered Clock Output
- ☐ Excellent Rejection of CCITT Guard Tones
- ☐ Low Power CMOS 50mW Typ.
- ☐ ±5 Volt Operation
- ☐ Low Cost 16-Pin Package

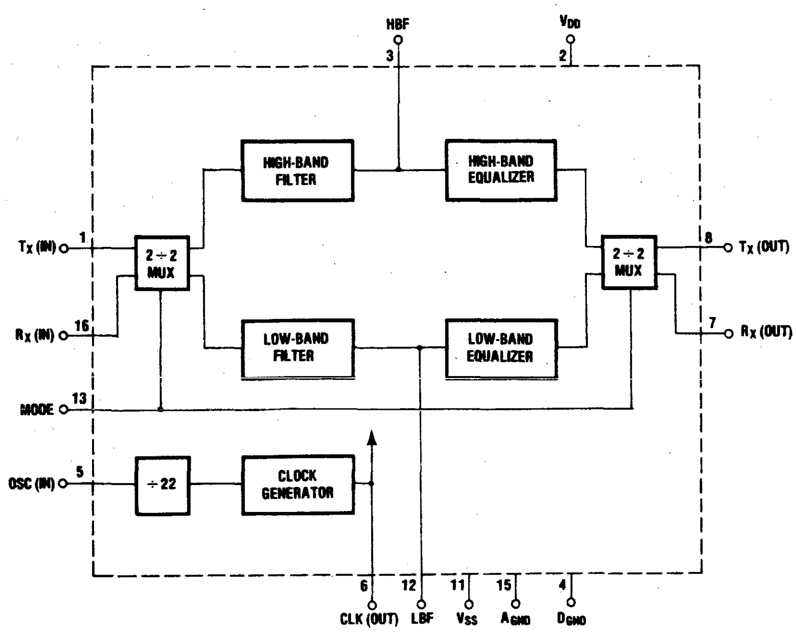
General Description

The AMI S3522 Modem Filter is a 16-pin monolithic CMOS integrated circuit designed to implement both the filtering and equalizing functions required in Bell 212A and CCITT V.22 Modems. The S3522 includes both the transmit signal shaping filter and the receive signal separation filter and features on-chip originate/answer mode selection logic. In addition, half-channel compromise amplitude and group delay equalization is included, giving full compromise equalization through the transmit and receive filter pair. The S3522 features excellent rejection of the CCITT Guard Tones at 550Hz: Low-Band (56dB), High-Band (61dB) and 1800Hz: Low-Band (48dB), High-Band (28dB).

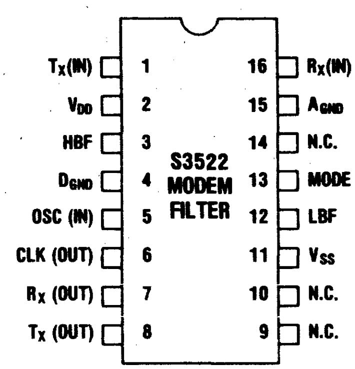
LINEAR

American Microsystems, Inc.

Block Diagram



Pin Configuration



SINGLE FREQUENCY TUNEABLE BANDPASS/NOTCH FILTER/TONE GENERATOR

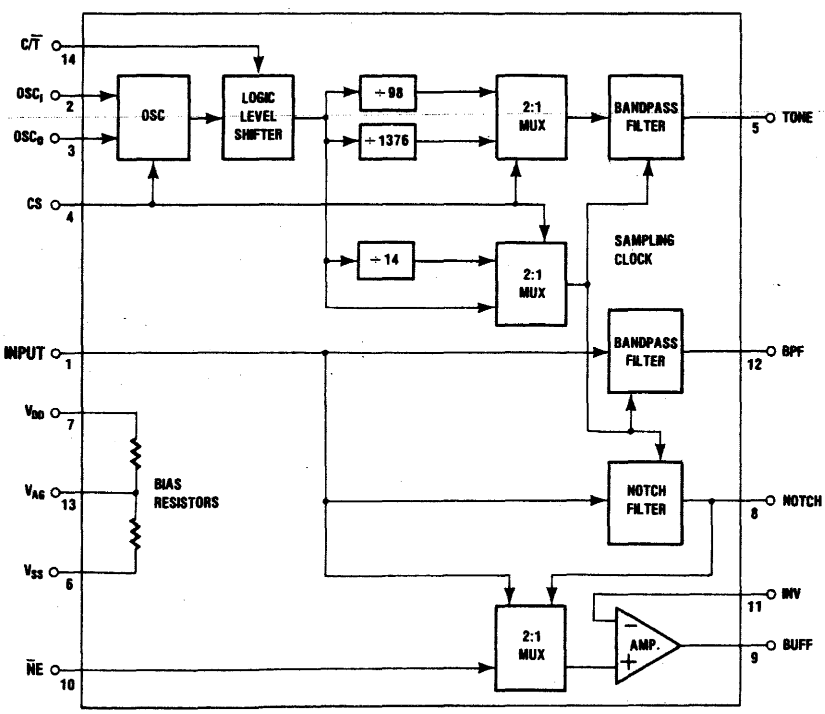
Features

- ☐ Center Frequency of Filters Match and Track Frequency of Generated Tone
- ☐ Tone Frequency Adjustable Over a 100Hz to 5kHz Range
- ☐ Unfiltered Input, Input with Notched Tone, Input Tone and Tone Generator Outputs
- ☐ Operation from a Crystal or External CMOS/TTL Clock
- ☐ Operation at 2600Hz from a Low Cost 3.58MHz TV Color Burst Crystal or 256kHz Ext. Clock
- ☐ Buffered Output Drives 600Ω Loads
- ☐ Single or Split Supply Operation
- ☐ Low Power CMOS Technology

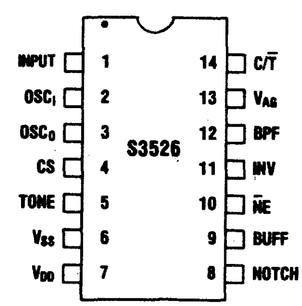
General Description

The S3526 is a low power CMOS Circuit which may be used in a variety of single frequency (SF) communication applications such as SF-Tone Receivers, Tone Remote Control in Mobile systems, Loopback Diagnostics in Modems, control of Echo Cancellers, dialing and privacy functions in Common Carrier Radio Telephone, etc. The main functional blocks of the S3526 include a low distortion tone (sinewave) generator whose frequency may be programmed using a crystal (i.e. 2600Hz using a low cost TV color burst crystal) or external clock time base; a bandpass filter used to extract tone information from the input signal; a band reject filter which is used to "Notch" out tone information from the input signal; and a buffer amplifier with selectable input (unfiltered input signal, or input signal with tone notched) capable of driving a 600Ω load.

Block Diagram



Pin Configuration



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S3528

PROGRAMMABLE LOW PASS FILTER

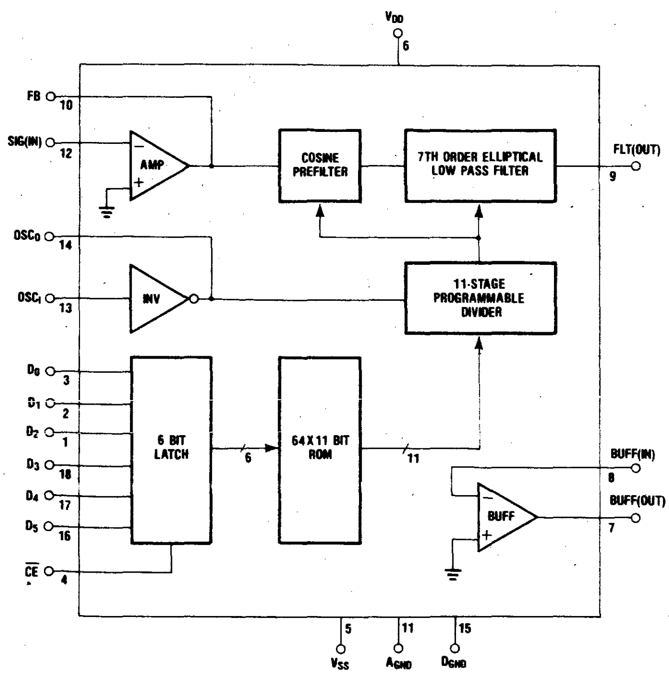
Features

- ☐ Seventh Order Ellipitical Ladder Filter with Cosine Prefiltering Stage
- ☐ Cutoff Frequency (f_C) Range of 10Hz to 20kHz, 40Hz to 20kHz Via 3.58MHz TV Crystal
- ☐ Passband Ripple: <0.1dB
- ☐ Stopband Attenuation: >51dB for $f>1.3f_C$
- ☐ Cutoff Frequency Selectable in 64 Steps Via Six Bit Control Word
- ☐ Steps May Be Custom Programmed from a Set of 2,048 Discrete Points Via Internal ROM
- ☐ Cutoff Frequency Continuously Variable Via External Clock (Crystal, Resonator, or TTL/CMOS Clock)
- ☐ Uncommitted Input and Output Op Amps for Anti-Aliasing and Smoothing Functions
- ☐ Low Power CMOS Technology

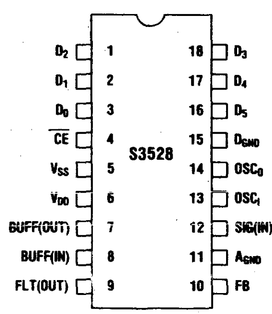
General Description

The S3528 is a programmable low pass filter which may be used in a wide variety of filtering applications commonly found in speech analysis, telecommunications, test equipment and instrumentation, etc. The 3528's CMOS design using switched capacitor design techniques allows easy programming of the filter's cutoff frequency (f_C), discretely, in 64 steps via a six bit control word or continuously by varying the external time base. The useful range of operation of the filter passband extends from 10Hz to 20kHz. When operating from a low cost TV crystal (3.58MHz) a range of 40Hz to 20kHz may be realized. For special applications the S3528 may be customized via the internal ROM to accomodate a specific set of cutoff frequencies from a choice of 2,048 possiblities.

Block Diagram



Pin Configuration



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S3506/S3507/S3507A

CMOS SINGLE CHIP μ-LAW/A-LAW SYNCHRONOUS COMBO CODECS WITH FILTERS

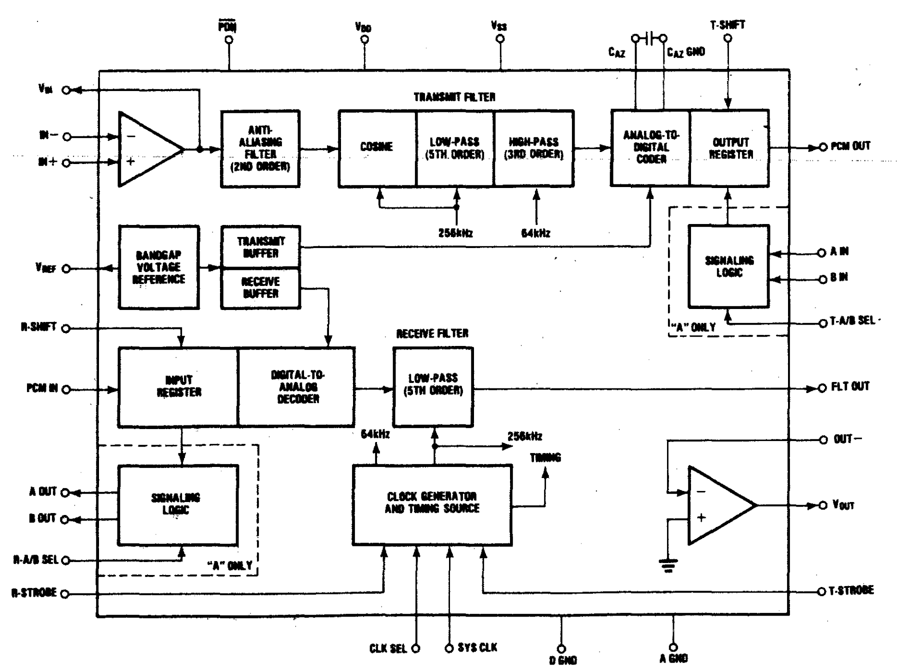
Features

- ☐ Independent Transmit and Receive Sections With 75dB Isolation
- ☐ Low Power CMOS 80mW (Operating) 8mW (Standby)
- ☐ Stable Voltage Reference On-Chip
- ☐ Meets or Exceeds AT&T D3, and CCITT G.711, G.712 and G.733 Specifications
- ☐ Input Analog Filter Eliminates Need for External Anti-Aliasing Prefilter
- ☐ Input/Output Op Amps for Programming Gain
- ☐ Output Op Amp Provides ±3.1V into a 600Ω Load or Can Be Switched Off for Reduced Power (70mW)
- ☐ Special Idle Channel Noise Reduction Circuitry for Crosstalk Suppression
- ☐ Encoder has Dual-Speed Auto-Zero Loop for Fast Acquisition on Power-Up
- ☐ Low Absolute Group Delay = 450μsec. @ 1kHz

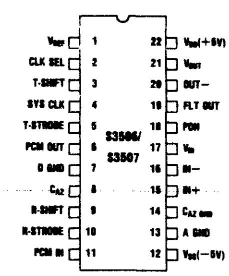
General Description

The S3506 and S3507 are monolithic silicon gate CMOS Companding Encoder/Decoder chips designed to implement the per channel voice frequency Codecs used in PCM systems. The chips contain the band-limiting filters and the analog↔digital conversion circuits that conform to the desired transfer characteristic. The S3506 provides the European A-Law companding and the S3507 provides the North American μ-Law companding characteristic.

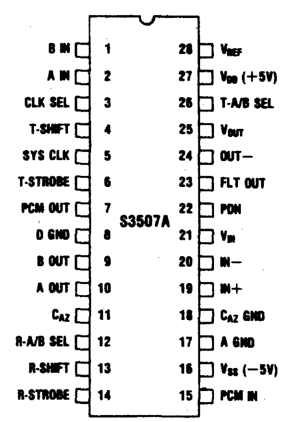
Block Diagram



Pin Configuration (22 Pin)



Pin Configuration (28 Pin)



LINEAR

American Microsystems, Inc.

AMI®

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S28211

SIGNAL PROCESSING PERIPHERAL

Features

- Single-Chip Programmable Digital Signal Processor
- May Be Customized (ROM Programmed) With Customer Generated Routines
- Self-Emulation Capability
- Standard Preprogrammed Processors Available
- Fetch/Multiply/Add/Store Cycle
- 512 Word × 18 Bit Instruction Memory
- Unique Three Port Data Memory 256 × 16 RAM/128 × 16 ROM
- 12 × 12 Pipelined Multiplier With 16 Bit Product
- 16 Bit Accumulator With Overflow Detect/Protect
- Double Buffered Asynchronous Serial I/O Port
- μP-Compatible I/O Port i.e. 6800 (A Version), 8080 (B Version), etc.

General Description

The S28211 is a single-chip microcomputer which has been optimized to execute digital signal processing algorithms commonly used in applications such as telecommunications speech processing, industrial process control instrumentation, etc. It may be used as a stand alone unit, or may be operated as a peripheral in a microprocessor based system. The latter configuration allows arrays of S28211s to be used together for increased processing throughput. The S28211's multibus, pipelined architecture and powerful multi-operation instructions make it possible to write very compact algorithms. This allows the available memory to be used efficiently and increases the execution speed of a given algorithm. The S28211 may be

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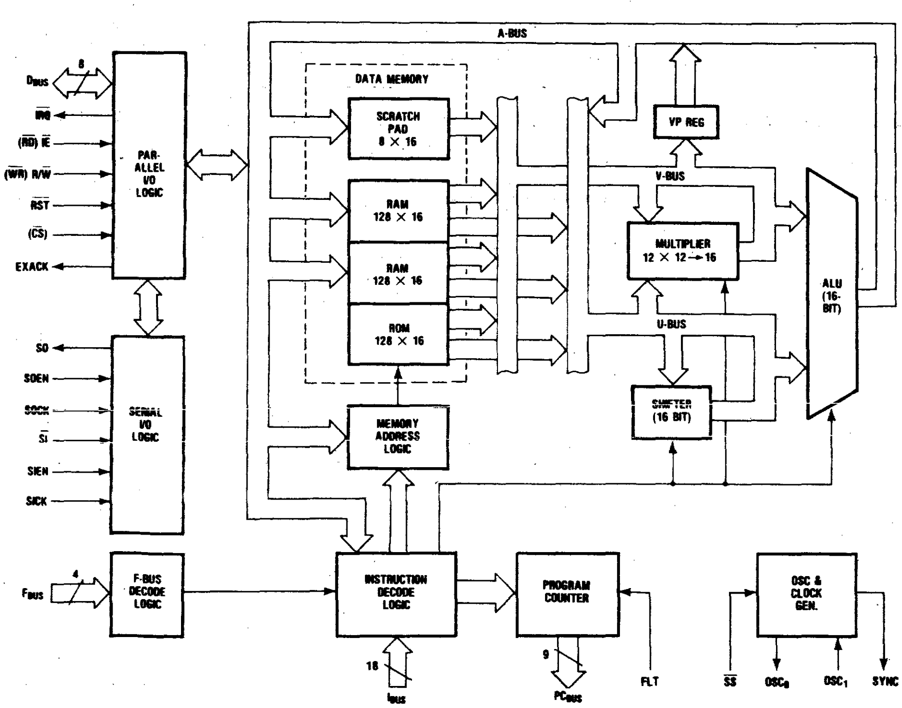
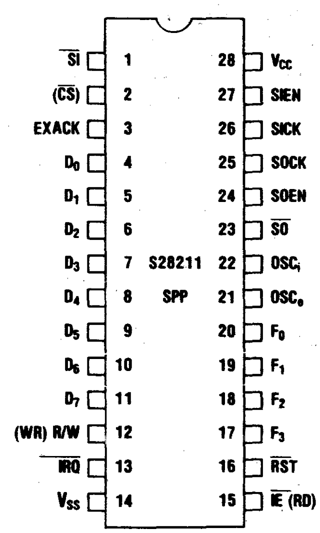
Simplified Block Diagram



Pin Configuration



NOTE:
PIN FUNCTIONS IN PARENTHESIS APPLY ONLY FOR B VERSION

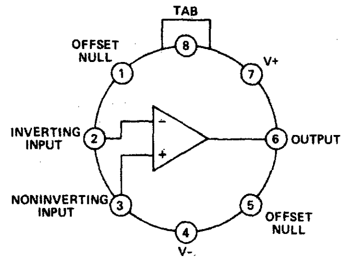
American Microsystems, Inc.

ANALOG DEVICES

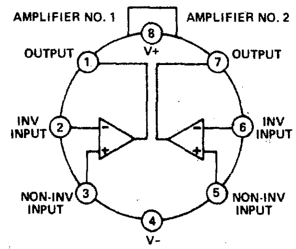
Ultra Low Drift BIFET Operational Amplifiers

AD547/AD647

FEATURES
Ultra Low Drift (1μV/°C)
Low Offset Voltage (0.25mV)
Low Input Bias Currents (25pA)
Low Quiescent Current
Low Noise (2μV p-p)
High Open Loop Gain (110dB)
Matched Offset Voltage – AD647
Matched Offset Voltage Over Temperature – AD647
Matched Bias Current – AD647
Crosstalk 124dB at 1kHz
Low Total Harmonic Distortion



AD547 SINGLE VERSION



AD647 DUAL VERSION

PRODUCT DESCRIPTION

The AD547 and AD647 are monolithic, FET input operational amplifiers combining the very low input bias current advantages of a BIFET op amp with offset and drift performance previously available only in high quality bipolar amplifiers.

The exclusive Analog Devices laser wafer trim process trims both the input offset voltage and offset voltage drift to levels far lower than any competing BIFET amplifier (1mV, 5μV/°C–J versions, 0.25mV, 1μV/°C–L versions).

In addition, the offset voltage is laser trimmed to less than 0.25mV and matched to 0.25mV for the AD647L, 0.5mV and matched to 0.25mV for the AD647K.

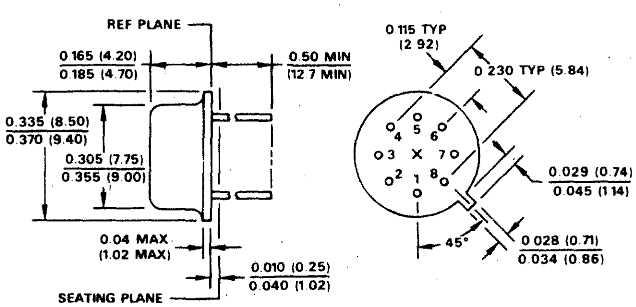
The AD547 offers the lowest guaranteed input bias currents of any BIFET amplifier with 50pA max for the J grade and 25pA max for the L grade. The AD647 offers matched bias currents that are significantly lower than currently available monolithic dual FET input operational amplifiers: 35pA max, matched to 15pA for the AD647K and L; 75pA max, matched to 25pA for the AD647J and S.

PRODUCT HIGHLIGHTS

1. Advanced laser wafer trimming techniques reduce offset voltage drift to 1μV/°C max and reduce offset voltage to only 0.25mV max on the AD547L.
2. Analog Devices BIFET processing provides 25pA max (10pA typical) bias currents specified after 5 minutes of warm-up.
3. Low voltage noise, high open loop gain and outstanding offset performance make the series true precision BIFET amplifiers.
4. The AD647 dual has tight matching specifications to ensure high performance, eliminating the need to match individual devices.
5. Laser-wafer-trimming reduces offset voltage to as low as 0.25mV max and matched side to side to 0.25mV (AD647L), thus eliminating the need for external nulling.
6. The standard dual amplifier pin out allows the AD647 to replace lower performance duals without redesign.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TO-99

ORDERING GUIDE

Model	Initial Offset Voltage	Offset Voltage Drift	Temperature Range
AD547JH	1.0mV	5μV/°C	0 to +70°C
AD547KH	0.5mV	2μV/°C	0 to +70°C
AD547LH	0.25mV	1μV/°C	0 to +70°C
AD547SH	0.5mV	5μV/°C	-55°C to +125°C
AD647JH	1.0mV	10μV/°C	0 to +70°C
AD647KH	0.5mV	5μV/°C	0 to +70°C
AD647LH	0.25mV	2μV/°C	0 to +70°C
AD647SH	0.5mV	10μV/°C	-55°C to +125°C

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ANALOG DEVICES

Operational Amplifiers

FEATURE SELECTION CHART

GENERAL PURPOSE: FET INPUT (AD503, AD506, AD540, AD542, AD642, AD644, AD544); WIDEBAND (AD644, AD544, AD101 Series); AD741

HIGH ACCURACY: LOW V_{OS} DRIFT (AD504, AD510, AD OP-07, AD517, AD545, AD547, AD647, AD515); FET INPUT (AD545, AD547, AD647, AD515)

Feature		AD503	AD506	AD540	AD542	AD642	AD644	AD544	AD101 Series	AD741	AD504	AD510	AD OP-07	AD517	AD545	AD547	AD647	AD515
Monolithic Technology	Bipolar Input								•	•	•	•	•	•				
	J-FET			•	•			•								•		
	Dual J-FET					•	•										•	
Multi-Device Technology	Hybrid	•	•												•			•
	Module																	
High Open Loop Gain	≥100dB				•	•					•	•	•	•		•	•	
	≥140dB																	
High CMR	>100dB										•	•	•	•				
Low Offset Voltage	≤5mV		•		•	•	•	•	•	•	•	•	•	•	•			•
	≤1mV				•	•	•	•								•	•	
	≤50μV												•	•				
Low Offset V, vs. Temp	≤5μV/°C				•	•	•	•			•	•	•	•	•	•	•	
	≤1μV/°C															•	•	
	≤0.6μV/°C										•	•	•					
Low Bias Current	≤50pA	•	•	•	•	•	•	•							•	•	•	•
	≤5pA														•			•
	≤0.5pA																	•
Fast Settling	≤1μs to 0.1%						•	•										
	≤5μs to 0.01%						•	•										
Wideband (Unity Gain)	≥2MHz						•	•	•									
	≥10MHz																	
High Slew Rate	≥10V/μs						•	•	•									
	≥30V/μs																	
	≥100V/μs																	
	≥1000V/μs															•	•	
Low Noise (0.1 to 10Hz) 2μV p-p					•	•	•	•	•		•	•	•	•				
High Voltage Out	≥100V																	
High Current Out	≥20mA																	
Low Power	≤75mW				•	•	•	•	•	•					•	•	•	•
Second Source									•	•			•					
Temperature Range	0 to +70°C	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	-25°C to +85°C								•									
	-55°C to +125°C	•	•	•	•	•	•	•	•	•	•	•	•	•		•	•	
Dice Availability				•	•	•	•	•					•	•		•		

GENERAL PURPOSE BIPOLAR INPUT SPECIFICATIONS (typical @ $V_S = \pm15V$, $T_A = +25°C$ unless otherwise noted)

Model	Gain min	Output V/mA min	Unity Gain MHz	Slew Rate V/μs	V_{OS} mV max	$\Delta V_{OS}/\Delta T$ μV/°C max	I_b nA max	CMR dB min	Temp Range[1]	Package[2]
AD101A	50k	10/5	1.0 to 8.0	0.5 to 10	2.0	15	75	80	M	H
AD201A	50k	10/5	1.0 to 8.0	0.5 to 10	2.0	15	75	80	I	H,N
AD301A	25k	10/5	1.0 to 8.0	0.5 to 10	7.5	30	250	70	C	H,N
AD301AL	80k	10/5	1.0 to 10.0	0.25 to 9.0	1.0	5.0	30	90	C	H,N
AD108	50k	13/1.3	0.3 to 3.0	0.3 to 1.3	2.0	15	2.0	85	M	H
AD208	50k	13/1.3	0.3 to 3.0	0.3 to 1.3	2.0	15	2.0	85	I	H
AD308	25k	13/1.3	0.3 to 3.0	0.3 to 1.3	7.5	30	7.0	80	C	H
AD108A	80k	13/1.3	0.3 to 3.0	0.3 to 1.3	0.5	5.0	2.0	96	M	H
AD208A	80k	13/1.3	0.3 to 3.0	0.3 to 1.3	0.5	5.0	2.0	96	I	H
AD308A	80k	13/1.3	0.3 to 3.0	0.3 to 1.3	0.5	5.0	7.0	96	C	H
AD741	50k	10/5	1.0	0.5	5.0	–	500	70	M	H,N
AD741C	20k	10/5	1.0	0.5	6.0	–	500	70	C	H,N
AD741J	50k	10/10	1.0	0.5	3.0	20	200	80	C	H,N
AD741K	50k	10/5	1.0	0.5	2.0	15	75	90	C	H,N
AD741L	50k	10/5	1.0	0.5	0.5	5.0	50	90	C	H,N
AD741S	50k	10/10	1.0	0.5	2.0	15	75	80	M	H

NOTES

[1] C = 0 to +70°C, I = -25°C to +85°C, M = -55°C to +125°C

[2] H = TO-99 can, N = 8-pin mini DIP

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GENERAL PURPOSE FET INPUT
SPECIFICATIONS (typical @ $V_S = \pm15V$, $T_A = +25^\circ C$ unless otherwise noted)

Model	Gain min	Output V/mA min	Unity Gain MHz	Slew Rate V/µs	V_{OS} mV max	$\Delta V_{OS}/\Delta T$ µV/°C max	I_b pA max	CMR dB min	Temp Range[1]	Package[2]
AD503J	20k	10/5	1.0	3.0	50	75	15	70	C	H
AD503K	50k	10/5	1.0	3.0	20	25	10	80	C	H
AD503S	50k	10/5	1.0	3.0	20	50	10	80	M	H
AD506J	20k	10/5	1.0	3.0	3.5	75	15	70	C	H
AD506K	50k	10/5	1.0	3.0	1.5	25	10	80	C	H
AD506L	75k	10/5	1.0	3.0	1.0	10	5	80	C	H
AD506S	50k	10/5	1.0	3.0	1.5	50	10	80	M	H
AD540J	20k	10/5	1.0	6.0	50	75	50	70	C	H
AD540K	50k	10/5	1.0	6.0	20	25	25	70	C	H
AD540S	50k	10/5	1.0	6.0	20	50	25	70	M	H
AD542J	100k	10/5	1.0	3.0	2.0	20	50	76	C	H
AD542K	300k	10/5	1.0	3.0	1.0	10	25	80	C	H
AD542L	300k	10/5	1.0	3.0	0.5	5	25	80	C	H
AD542S	300k	10/5	1.0	3.0	1.0	15	25	80	M	H
AD544J	30k	10/5	2.0	13	2.0	20	50	74	C	H
AD544K	50k	10/5	2.0	13	1.0	10	25	80	C	H
AD544L	50k	10/5	2.0	13	0.5	5	25	80	C	H
AD544S	50k	10/5	2.0	13	1.0	15	25	80	M	H
AD547J	100k	10/5	1.0	3.0	1.0	5	50	76	C	H
AD547K	250k	10/5	1.0	3.0	0.5	2	25	80	C	H
AD547L	250k	10/5	1.0	3.0	0.25	1	25	80	C	H
AD547S	250k	10/5	1.0	3.0	0.5	5	25	80	M	H
AD642J	100k	10/5	1.0	3.0	2.0^3	$3.5mV^4$	75	76	C	H
AD642K	300k	10/5	1.0	3.0	1.0^3	$2.0mV^4$	35	80	C	H
AD642L	300k	10/5	1.0	3.0	0.5^3	$1.0mV^4$	35	80	C	H
AD642S	300k	10/5	1.0	3.0	1.0^3	$3.5mV^4$	75	80	M	H
AD644J	30k	10/5	2.0	13	2.0^3	$3.5mV^4$	75	76	C	H
AD644K	50k	10/5	2.0	13	1.0^3	$2.0mV^4$	35	80	C	H
AD644L	50k	10/5	2.0	13	0.5^3	$1.0mV^4$	35	80	C	H
AD644S	50k	10/5	2.0	13	1.0^3	$3.5mV^4$	75	80	M	H
AD647JH	100k	10/5	1.0	3.0	1.0^3	10	75	76	C	H
AD647KH	250k	10/5	1.0	3.0	0.5^3	5	35	80	C	H
AD647LH	250k	10/5	1.0	3.0	0.25^3	2.5	35	80	C	H
AD647SH/	250k	10/5	1.0	3.0	0.5^3	10	35	80	M	H

NOTES
[1] C = 0 to +70°C; M = −55°C to +125°C
[2] H = TO-99 can; Z = Module
[3] Dual amplifiers with matched side to side offset voltage
[4] Guaranteed max offset error from T_{min} to T_{max}

HIGH ACCURACY LOW V_{OS} DRIFT
SPECIFICATIONS (typical @ $V_S = \pm15V$, $T_A = +25^\circ C$ unless otherwise noted)

Model	Gain min	Output V/mA min	Unity Gain MHz	Slew Rate V/µs	V_{OS} mV max	$\Delta V_{OS}/\Delta T$ µV/°C max	I_b nA max	CMR dB min	Temp Range[1]	Package[2]
AD504J	250k	10/5	0.3 to 1.0^3	0.12 to 2.5^3	2.5	5.0	200	94	C	H
AD504K	500k	10/5	0.3 to 1.0^3	0.12 to 2.5^3	1.5	3.0	100	100	C	H
AD504L	1000k	10/5	0.3 to 1.0^3	0.12 to 2.5^3	0.5	1.0	80	110	C	H
AD504M	1000k	10/5	0.3 to 1.0^3	0.12 to 2.5^3	0.5	0.5	80	110	C	H
AD504S	1000k	10/5	0.3 to 1.0^3	0.12 to 2.5^3	0.5	1.0	80	110	M	H
AD510J	250k	10/5	0.3	0.1	0.1	3.0	25	94	C	H
AD510K	1000k	10/5	0.3	0.1	0.05	1.0	13	110	C	H
AD510L	1000k	10/5	0.3	0.1	0.025	0.5	10	110	C	H
AD510S	1000k	10/5	0.3	0.1	0.05	1.0	13	110	M	H
AD517J	1000k	10/10	0.25	0.1	0.150	3.0	5	94	C	H
AD517K	1000k	10/10	0.25	0.1	0.075	1.8	2	110	C	H
AD517L	1000k	10/10	0.25	0.1	0.05	1.3	1	110	C	H
AD517S	1000k	10/10	0.25	0.1	0.075	1.8	2	110	M	H
AD547J	100k	10/5	1.0	3.0	1.0	5	50	76	C	H
AD547K	250k	10/5	1.0	3.0	0.5	2	25	80	C	H
AD547L	250k	10/5	1.0	3.0	0.25	1	25	80	C	H
AD547S	250k	10/5	1.0	3.0	0.5	5	25	80	M	H
AD647JH	100k	10/5	1.0	3.0	1.0^3	10	75	76	C	H
AD647KH	250k	10/5	1.0	3.0	0.5^3	5	35	80	C	H
AD647LH	250k	10/5	1.0	3.0	0.25^3	2.5	35	80	C	H
AD647SH	250k	10/5	1.0	3.0	0.5^3	10	35	80	M	H
AD OP-07EH	2000k	10/10	0.6	0.17	0.075	1.3	±4	106	C	H
AD OP-07CH	1200k	10/10	0.6	0.17	0.150	1.6	±7	100	C	H
AD OP-07DH	1200k	10/10	0.6	0.17	0.150	2.5	±12	94	C	H
AD OP-07AH	3000k	10/10	0.6	0.17	0.025	0.6	±2	110	M	H
AD OP-07H	2000k	10/10	0.6	0.17	0.075	1.3	±3	110	M	H

NOTES
[1] C = 0 to +70°C; M = −55°C to +125°C
[2] H = TO-99 can; N = 8-pin mini DIP
[3] Dependent on compensation capacitor selection

HIGH ACCURACY LOW BIAS CURRENT
SPECIFICATIONS (typical @ $V_S = \pm15V$, $T_A = +25^\circ C$ unless otherwise noted)

Model	Gain min	Output V/mA min	Unity Gain MHz	Slew Rate V/µs	V_{OS} mV max	$\Delta V_{OS}/\Delta T$ µV/°C max	I_b pA max	CMR dB min	Temp Range[1]	Package[2]
AD515J	20k	10/5	0.35	0.3	3.0	50	0.300	66	C	H
AD515K	40k	10/5	0.35	0.3	1.0	15	0.150	80	C	H
AD515L	25k	10/5	0.35	0.3	1.0	25	0.075	70	C	H
AD545J	20k	10/5	0.7	1.0	1.0	25	2	66	C	H
AD545K	40k	10/5	0.7	1.0	1.0	15	1	70	C	H
AD545L	40k	10/5	0.7	1.0	0.5	5	1	76	C	H
AD545M	40k	10/5	0.7	1.0	0.25	3	1	76	C	H

NOTES
[1] C = 0 to +70°C
[2] H = TO-99 can, Z = Module
[3] Adjustable to zero

FEATURE SELECTION CHART

FAST/WIDEBAND — FET INPUT — UNITY GAIN BUFFER

Feature	Criterion	AD507	AD509	AD518	AD380	AD381	AD382	AD3554	HOS-050	HOS-060	ADLH0032	ADLH0033	HOS-100
Monolithic Technology	Bipolar Input	●	●	●									
	J-FET												
	Dual J-FET												
Multi-Device Technology	Hybrid				●	●	●	●	●	●	●	●	●
	Module												
High Open Loop Gain	≥100dB	●				●	●	●	●	●			
	≥140dB												
High CMR	>100dB												
Low Offset Voltage	≤5mV	●	●		●		●	●			●	●	
	≤1mV					●				●			
	≤50µV												
Low Offset V, vs. Temp	≤5µV/°C					●	●						
	≤1µV/°C												
	≤0.6µV/°C												
Low Bias Current	≤50pA					●	●	●			●	●	
	≤5pA												
	≤0.5pA												
Fast Settling	≤1µs to 0.1%	●	●	●		●	●		●	●	●	●	●
	≤5µs to 0.01%				●			●	●	●	●		
Wideband (Unity Gain)	≥2MHz					●	●						
	≥10MHz	●	●	●	●			●	●	●	●	●	●
	≥50MHz												
High Slew Rate	≥10V/µs	●		●									
	≥30V/µs					●	●						
	≥100V/µs		●		●				●	●	●	●	●
	≥1000V/µs							●					
Low Noise (0.1 to 10Hz) ≥2µV p-p						●	●						
High Voltage Out	≥100V												
High Current Out	≥20mA	●			●		●	●	●	●		●	●
Low Power	≤75mW												
Second Source		●	●					●			●	●	
Temperature Range	0 to +70°C	●	●	●	●	●	●						
	−25°C to +85°C							●			●	●	
	−55°C to +125°C	●	●	●	●	●	●	●	●	●	●	●	●
Dice Availability				●									

FAST/WIDEBAND SPECIFICATIONS (typical @ $V_S = \pm15V$, $T_A = +25°C$ unless otherwise noted)

Model	Gain min	Output V/mA min	Unity Gain MHz	Slew Rate V/µs min	Settling Time µs to 0.1%	V_{OS} mV max	$\Delta V_{OS}/\Delta T$ µV/°C max	I_b nA max	CMR dB min	Temp Range[1]	Package[2]
AD380JH	25k	10/50	40	200	0.13	2.0	50	100	60	C	X
AD380KH	25k	10/50	40	200	0.13	1.0	20	100	60	C	X
AD380LH	25k	10/50	40	200	0.13	1.0	10	100	60	C	X
AD380SH	25k	10/50	40	200	0.13	1.0	50	100	60	M	X
AD381JH	60k	10/5	5	20	0.7	1.0	15	100	76	C	H
AD381KH	100k	10/5	5	20	0.7	0.5	10	100	80	C	H
AD381LH	100k	10/5	5	20	0.7	0.25	5	100	80	C	H
AD381SH	100k	10/5	5	20	0.7	1.0	10	100	80	M	H
AD382JH	25k	10/50	5	20	1.3[3]	1.0	15	100	76	C	X
AD382KH	35k	10/50	5	20	1.3[4]	0.5	10	50	80	C	X
AD382LH	35k	10/50	5	20	1.3[4]	0.25	5	50	80	C	X
AD382SH	35k	10/50	5	20	1.3[4]	1.0	10	50	80	M	X
AD507J	80k	10/10	35	20	0.9	5	15	25	74	C	H
AD507K	100k	10/10	35	25	0.9	3	15	15	80	C	H
AD507S	100k	10/10	35	20	0.9	4	20	15	80	M	H
AD509J	7.5k	10/5	20	80	0.2	10	20	250	74	C	H
AD509K	10k	10/5	20	80	0.2	8	30	200	80	C	H
AD509S	10k	10/5	20	100	0.5	8	30	200	80	M	H
AD518J	25k	10/10	12	50	0.8	10	10	500	70	C	H
AD518K	50k	10/10	12	50	0.8	4	15	250	80	C	H
AD518S	50k	10/10	12	50	0.8	4	20	250	80	M	H
AD3554AM	31.6k	10/100	90	1000	0.12	2.0	50	50	60	I	Y
AD3554BM	31.6k	10/100	90	1000	0.12	1.0	15	50	60	I	Y
AD3554SM	31.6k	10/100	90	1000	0.12	1.0	25	50	60	M	Y
~~ADLH0032CG~~	~~1k~~	~~12/10~~	~~70~~	~~500~~	~~0.3~~	~~5~~	~~25~~	~~0.025~~	~~60~~	~~I~~	X
ADLH0032G	1k	12/10	70	500	0.3	2	25	0.01	60	M	X
ADLH0033CG	0.98[5]	12/100	100[6]	1400	3.2ns[7]	12	50	0.05	–	I	X
ADLH0033G	0.98[5]	12/100	100[6]	1500	2.9ns[7]	5	50	0.05	–	M	X
HOS-050	100k	10/100	100	300	0.1	35	150	2	70	M	X
HOS-050A	100k	10/100	100	300	0.1	15	35	2	70	M	X
HOS-050C	100k	10/100	100	300	0.1	65	200	2*	70	I	X
HOS-060SH	100k	10/100	100	300	0.1	1.0	10	2*	70	M	X
HOS-100AH	0.96[5]	12/100	125[6]	1400	2.0ns[7]	10	25	5µA	–	I	X
HOS-100SH	0.97[5]	12/100	125[6]	1500	2.0ns[7]	5	25	5µA	–	M	X

NOTES
[1] C = 0 to +70°C, I = −25°C to +85°C, M = −25°C to +125°C
[2] H = TO-99 can, X = 12-lead TO-8 can, Y = TO-3 can, Z = Module
[3] Settling time to 0.01%
[4] Settling time to 0.01%; max
[5] Unity Gain Buffers
[6] Large Signal 3dB BW
[7] Rise Time

LINEAR

Analog Devices

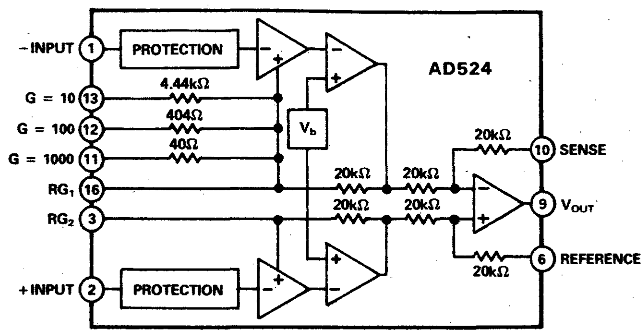
ANALOG DEVICES

Precision Instrumentation Amplifier

AD524

FEATURES
Low Noise: 0.3μV p-p 0.1Hz to 10Hz
Low Nonlinearity: 0.003% (G = 1)
High CMRR: 120dB (G = 1000)
Low Offset Voltage: 50μV
Low Offset Voltage Drift: 0.5μV/°C
Gain Bandwidth Product: 25MHz
Pin Programmable Gains of 1, 10, 100, 1000
Input Protection, Power On – Power Off
No External Components Required
Internally Compensated

AD524 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

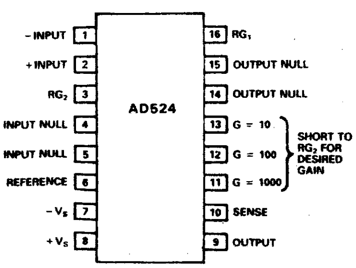
The AD524 is a precision monolithic instrumentation amplifier designed for data acquisition applications requiring high accuracy under worst-case operating conditions. An outstanding combination of high linearity, high common mode rejection, low offset voltage drift, and low noise makes the AD524 suitable for use in many data acquisition systems.

The AD524 has an output offset voltage drift of less than 25μV/°C, input offset voltage drift of less than 0.5μV/°C, CMR above 90dB at unity gain (120dB at G = 1000) and maximum nonlinearity of 0.003% at G = 1. In addition to the outstanding dc specifications the AD524 also has a 25MHz gain bandwidth product (G = 100). To make it suitable for high speed data acquisition systems the AD524 has an output slew rate of 5V/μs and settles in 15μs to 0.01% for gains of 1 to 100.

As a complete amplifier the AD524 does not require any external components for fixed gains of 1, 10, 100 and 1,000. For other gain settings between 1 and 1000 only a single resistor is required. The AD524 input is fully protected for both power on and power off fault conditions.

The AD524 IC instrumentation amplifier is available in four different versions of accuracy and operating temperature range. The economical "A" grade, the low drift "B" grade and lower drift, higher linearity "C" grade are specified from –25°C to +85°C. The "S" grade guarantees performance to specification over the extended temperature range –55°C to +125°C.

PIN CONFIGURATION

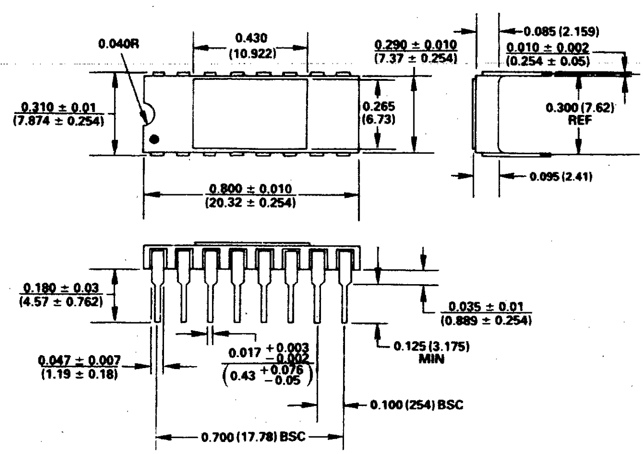


PRODUCT HIGHLIGHTS

1. The AD524 has guaranteed low offset voltage, offset voltage drift and low noise for precision high gain applications.
2. The AD524 is functionally complete with pin programmable gains of 1, 10, 100 and 1000, and single resistor programmable for any gain.
3. Input and output offset nulling terminals are provided for very high precision applications and to minimize offset voltage changes in gain ranging applications.
4. The AD524 is input protected for both power on and power off fault conditions.
5. The AD524 offers superior dynamic performance with a gain bandwidth product of 25MHz, full power response of 75kHz and a settling time of 15μs to 0.01% of a 10V step (G = 100).

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



16-PIN CERAMIC DIP PACKAGE

LINEAR

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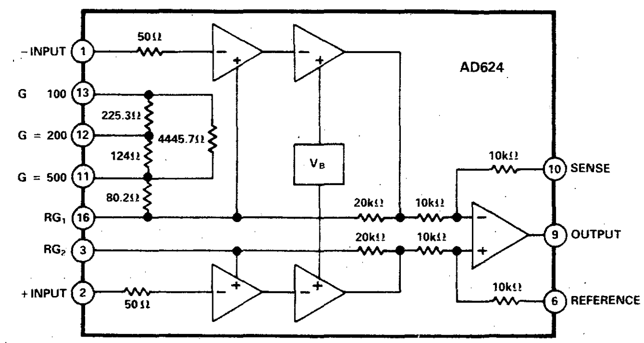
ANALOG DEVICES

Precision Instrumentation Amplifier

AD624

FEATURES
Low Noise: 0.2μV p-p 0.1Hz to 10Hz
Low Gain TC: 10ppm
Low Nonlinearity: 0.001% max (G = 1 to 500)
High CMRR: 130dB max (G = 500)
Low Offset Voltage: 25μV, max
Low Offset Voltage Drift: 0.25μV/°C max
Gain Bandwidth Product: 25MHz
Pin Programmable Gains of 1, 100, 200, 500, 1000
No External Components Required
Internally Compensated

AD624 FUNCTIONAL BLOCK DIAGRAM



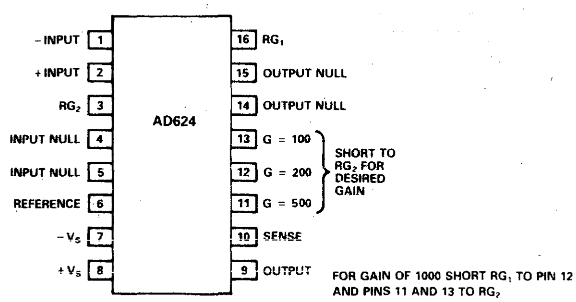
PRODUCT DESCRIPTION

The AD624 is a high precision ultra low noise instrumentation amplifier designed primarily for use with low level transducers, including load cells, strain gauges and pressure transducers. An outstanding combination of low noise, high gain accuracy, low gain temperature coefficient and high linearity make the AD624 ideal for use in high resolution data acquisition systems.

The AD624C has an input offset voltage drift of less than 0.25μV/°C, output offset voltage drift of less than 10μV/°C, CMR above 90dB at unity gain (130dB at G = 500) and a maximum nonlinearity of 0.001% at G = 1. In addition to these outstanding dc specifications the AD624 exhibits superior ac performance as well. A 25MHz gain bandwidth product, 5V/μs slew rate and 15μs settling time permit the use of the AD624 in high speed data acquisition applications.

The AD624 does not need any external components for pre-trimmed gains of 1, 100, 200, 500 and 1000. Additional gains such as 250 and 330 can be programmed within a few percent accuracy with external jumpers. A single external resistor can also be used to set the 624's gain to any value in the range of 1 to 1000.

PIN CONFIGURATION

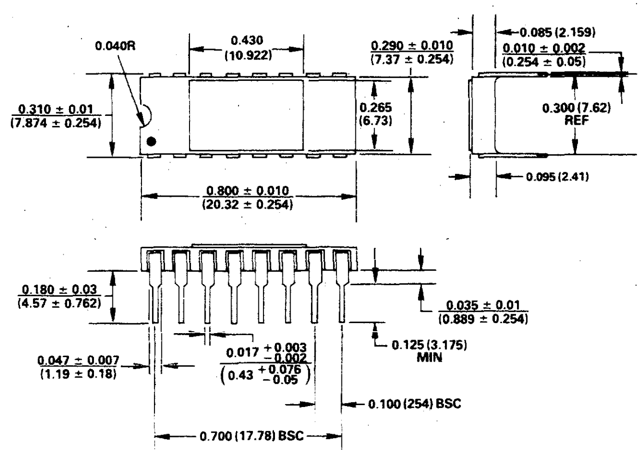


PRODUCT HIGHLIGHTS

1. The AD624 offers outstanding noise performance. Input noise is typically less than $4nV/\sqrt{Hz}$ at 1kHz.
2. The AD624 is a functionally complete instrumentation amplifier. Pin programmable gains of 1, 100, 200, 500 and 1000 are provided on the chip. Other gains are achieved through the use of a single external resistor.
3. The offset voltage, offset voltage drift, gain accuracy and gain temperature coefficients are guaranteed for all pre-trimmed gains.
4. The AD624 provides totally independent input and output offset nulling terminals for high precision applications. This minimizes the effect of offset voltage in gain ranging applications.
5. A sense terminal is provided to enable the user to minimize the errors induced through long leads. A reference terminal is also provided to permit level shifting at the output.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



16-PIN CERAMIC DIP PACKAGE

LINEAR

Analog Devices

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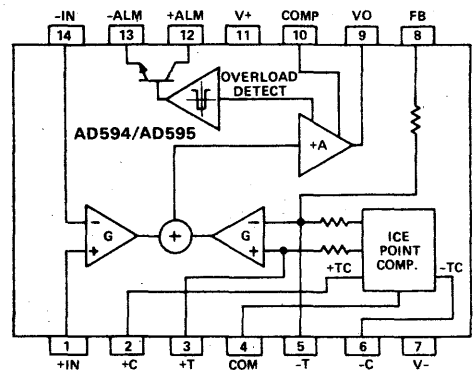
Monolithic Thermocouple Amplifier with Cold Junction Compensation

AD594*/AD595*

FEATURES
Pretrimmed for Type J (AD594) or Type K (AD595) Thermocouples
Can Be Used with Type T Thermocouple Inputs
Low Impedance Voltage Output: 10mV/°C
Built-In Ice Point Compensation
Wide Power Supply Range: +5V to ±15V
Low Power: <1mW typical
Thermocouple Failure Alarm
Laser Wafer Trimmed to 1°C Calibration Accuracy
Set-Point Mode Operation
Self-Contained Celsius Thermometer Operation
High Impedance Differential Input

AD594/AD595 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD594/AD595 is a complete instrumentation amplifier and thermocouple cold junction compensator on a monolithic chip. It combines an ice point reference with a precalibrated amplifier to produce a high level (10mV/°C) output directly from a thermocouple signal. Pin-strapping options allow it to be used as a linear amplifier-compensator or as a switched output set-point controller using either fixed or remote set-point control. It can be used to amplify its compensation voltage directly, thereby converting it to a stand-alone Celsius transducer with a low-impedance voltage output.

The AD594/AD595 includes a Thermocouple Failure Alarm that indicates if one or both thermocouple leads become open. The alarm output has a flexible format which includes TTL drive capability.

The AD594/AD595 can be powered from a single ended supply (including +5V) and by including a negative supply, temperatures below 0°C can be measured. To minimize self-heating, an unloaded AD594/AD595 will typically operate with a total supply current of 160μA, but is also capable of delivering in excess of ±5mA to a load.

The AD594 is precalibrated by laser wafer trimming to match the characteristic of type J (iron-constantan) thermocouples and the AD595 is laser trimmed for type K (chromel-alumel) inputs. The temperature transducer voltages and gain control resistors are available at the package pins so that the circuit can be recalibrated for other thermocouple types by the addition of two or three resistors. These terminals also allow more precise calibration for both thermocouple and thermometer applications.

The AD594/AD595 is available in two performance grades. The C and the A versions have calibration accuracies of ±1°C and ±3°C, respectively. Both are designed to be used from 0 to +50°C, and are available in a 14-pin, hermetically sealed, side-brazed ceramic DIP.

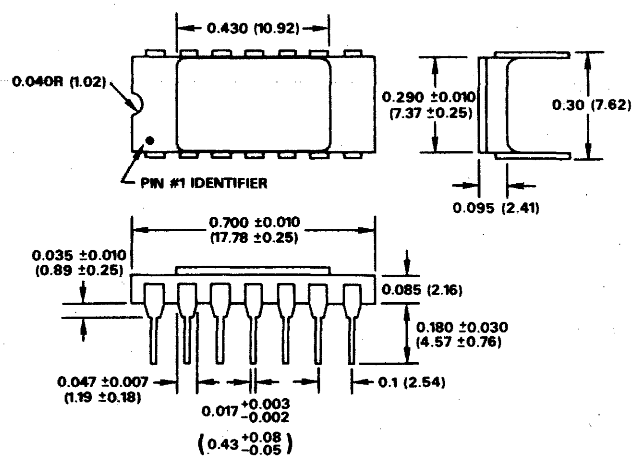
*Protected by U.S. Patent No. 4,029,974.

PRODUCT HIGHLIGHTS

1. The AD594/AD595 provides cold junction compensation, amplification, and an output buffer in a single IC package.
2. Compensation, zero, and scale factor are all precalibrated by laser wafer trimming (LWT) of each IC chip.
3. Flexible pin-out provides for operation as a set-point controller or a stand-alone temperature transducer calibrated in degrees Celsius.
4. Operation at remote application sites is facilitated by low quiescent current and a wide supply voltage range of +5V to dual supplies spanning 30V.
5. Differential input rejects common-mode noise voltage on the thermocouple leads.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TO-116

ANALOG DEVICES

Ultra-Fast Comparators

AD9685/AD9687

FEATURES
2.2ns Propagation Delay – AD9685BD/BH
2.7ns Propagation Delay – AD9687BD
0.5ns Latch Set-Up Time
Pin-Compatible to Am685/687 but FASTER
+5V, −5.2V Supply Voltages

APPLICATIONS
Ultra-High-Speed A/D Converters
Ultra-High-Speed Line Receivers
Peak Detectors
Threshold Detectors

GENERAL DESCRIPTION

The AD9685BD/BH and AD9687BD are ultra-fast comparators manufactured with a high performance bipolar process which makes it possible to obtain incredibly short propagation delays and latch set-up times.

The AD9685BD/BH is a single comparator which is pin-compatible with the Am685, but has speed capabilities that far outstrip the earlier unit. The AD9687BD is pin-for-pin compatible with the Am687 and, like its predecessor, is a dual comparator; its speed capabilities are far superior to the Am687.

Both Analog Devices units have differential inputs and complementary outputs fully compatible with ECL logic levels. Their output current levels are capable of driving 50Ω terminated transmission lines, and their high resolution make them ideally suited for a variety of analog-to-digital signal processing applications.

AD9685BD/BH Single Comparator

A latch function allows the AD9685BD/BH to be operated in a sample-hold mode. When the Latch Enable (LE) is ECL HIGH, the comparator functions normally. When the Latch Enable is driven LOW, its outputs are locked in the logic state dictated by the input conditions at the time of the latch input transition. If the latch function is not used, the Latch Enable input should be connected to ground.

In addition to its speed advantages over the earlier Am685, the AD9685BD/BH also dissipates less power because it operates on a positive 5 volt supply instead of the 6 volts required by the AMD device.

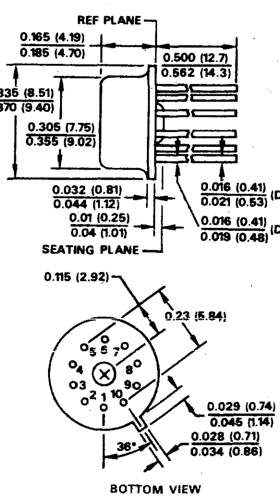
AD9687BD Dual Comparator

The latch function of the AD9687BD provides an ability to operate the unit in either a track-hold or sample-hold mode. The latch function inputs are separated on the two comparators and are designed to be driven from the complementary outputs of a standard ECL logic gate. When LE is High and $\overline{LE}$ is LOW, the normal comparator function is in operation. When LE is forced LOW and $\overline{LE}$ is driven HIGH, the outputs of the comparator being exercised are locked in their existing logical states, as determined by the input conditions present at the time of arrival of the latch signal. If the latch function is not used on either one of the two comparators in the AD9687BD, the appropriate Latch Enable input should be connected to ground; the companion $\overline{\text{Latch Enable}}$ input can be left open.

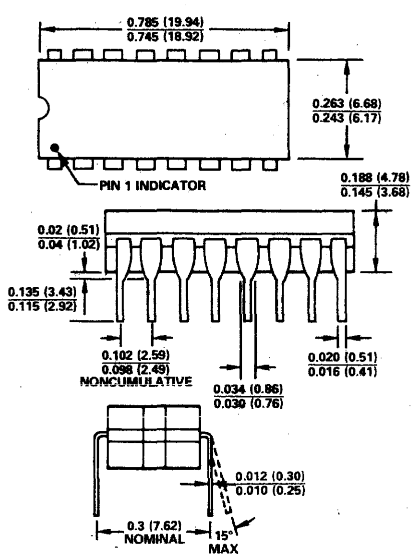
The AD9687BD is basically two AD9685BD/BH units in a single package and operates in a similar fashion to a pair of the single comparators.

OUTLINE DIMENSIONS

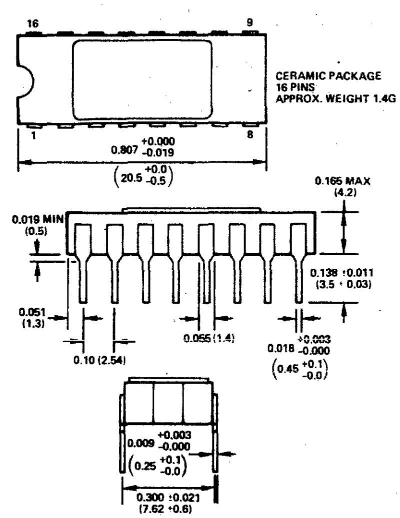
Dimensions shown in inches and (mm).



AD9685BH



AD9685BD



AD9687BD

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INSTRUMENTATION AMPLIFIERS

SPECIFICATIONS (typical @ $V_S = \pm15V$, $R_L = 2k\Omega$ and $T_A = 25^\circ C$ unless otherwise noted)

Model	Monolithic IC AD521J(K)(L)(S)[1]	Hybrid IC AD522A(B)(S)[1]	Monolithic AD524A(B)(C)(S)	Monolithic AD624A(B)(C)(S)
GAIN				
Range V/V	0.1 to 1000	1 to 1000	1 to 1000	1 to 1000
Nonlinearity (G = 100) – % max	0.2(0.2)(0.1)(0.2)	0.01(0.005)(0.005)	0.01(0.005)(0.003)(0.005)	0.01(0.005)(0.003)(0.005)
RATED OUTPUT – V dc/mA	±10/±10	±10/±5	±10/±5	±10/±5
DYNAMIC RESPONSE				
Small Signal (–3dB)				
G = 1000	40kHz	300Hz	25kHz	25kHz
Full Power Frequency	100kHz	1.5kHz	–	–
Slew Rate – V/μs	10	0.1	5	5
OFFSET VOLTAGE				
Input Offset Voltage	3(1.5)(1)(1.5)μV max	±400(200)(200)μV max	250(100)(50)(100)μV	100(50)(25)(100)μV
vs. Temperature	15(15)(2)(5)μV/°C	±6(2)(6)μV/°C	2(0.75)(0.5)(2)μV/°C	1(0.5)(0.2)(1)μV/°C
Output Offset Voltage	400(1200)(100)(200)μV max		5(3)(2)(3)mV	5(3)(2)(3)mV
vs. Temperature	400(150)(75)(150)μV/°C		100(50)(25)(50)μV/°C	100(50)(25)(50)μV/°C
INPUT BIAS CURRENT – nA max	±80(40)(40)(40)	±25(15)(25)	50(25)(15)(25)	100(50)(30)(100)
INPUT IMPEDANCE				
Common Mode – Ω	6×10^{10}	10^9	10^9/10pF	10^9/10pF
COMMON MODE REJECTION RATIO				
min @ 1kΩ Source Unbalance, CMV = ±10V				
G = 1 – dB	70(74)(74)(74)[2]	75(80)(85) dc to 30Hz	70(75)(80)(70)	
G = 10 – dB	90(94)(94)(94)[2]	90(95)(90) dc to 10Hz	90(95)(100)(90)	
G = 1000 – dB	100(110)(110)(110)[2]	100(110)(100) dc to 1Hz	100(115)(120)(110)	100(110)(115)(100)

NOTES
[1] Processing to MIL-STD-883B available.
[2] DC to 60Hz.

COMPARATORS

The AD9685BD/BH and AD9687BD are ultra-fast comparators which make it possible to obtain incredibly short propagation delays and latch setup times. The AD9685BD/BH is a single comparator, with the BD and BH suffixes indicating a DIP or TO-100 configuration; the AD9687BD is a dual comparator in a DIP.

The Analog Devices units are pin-for-pin compatible with the Am685 and Am687 comparators, but are far superior in speed to their forerunners. The ADI devices are an alternate source, not a second source, for the earlier units because of their greater speed capabilities but can be used as a higher-performance replacement for most applications.

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

Model Number	Input Offset Voltage	Max. Input Offset Current	Input Bias Current	Input Voltage Range	Output Levels (Volts) High	Output Levels (Volts) Low	Propagation Delays (ns) Input to Output High	Propagation Delays (ns) Input to Output Low	Latch Enable Times (nanoseconds) Setup	Latch Enable Times (nanoseconds) Hold
AD9685	5mV	5μA	10μA	±5V	–0.88	–1.75	2.2	2.2	0.5	1.0
AD9687	5mV	5μA	10μA	±5V	–0.88	–1.75	2.7	2.7	0.5	1.0

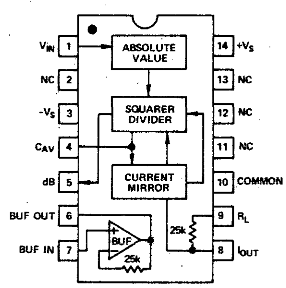
ANALOG DEVICES

Low Level True rms-to-dc Converter

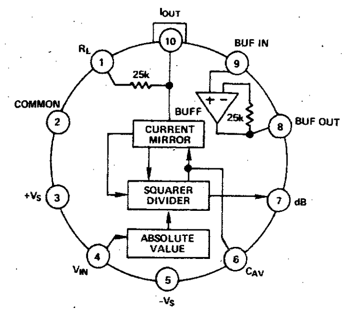
AD636

FEATURES
- True rms-to-dc Conversion
- 200mV Full Scale
- Laser-Trimmed to High Accuracy
  - 0.5% max Error (AD636K)
  - 1.0% max Error (AD636J)
- Wide Response Capability:
  - Computes rms of ac and dc Signals
  - 1MHz -3dB Bandwidth: V_{rms}>100mV
  - Signal Crest Factor of 6 for 0.5% Error
- dB Output with 50dB Range
- Low Power: 800μA Quiescent Current
- Single or Dual Supply Operation
- Monolithic Integrated Circuit
- Low Cost

AD636 FUNCTIONAL BLOCK DIAGRAMS



TO-116
TOP VIEW



TO-100
TOP VIEW

PRODUCT DESCRIPTION

The AD636 is a low power monolithic IC which performs true rms-to-dc conversion on low level signals. It offers performance which is comparable or superior to that of hybrid and modular converters costing much more. Similar in operation to the AD536A, the AD636 is specified for a signal range of 0 to 200 millivolts rms. Crest factors up to 6 can be accommodated with less than 0.5% additional error, allowing accurate measurement of complex input waveforms.

The low power supply current requirement of the AD636, typically 800μA, allows it to be used in battery-powered portable instruments. A wide range of power supplies can be used, from ±2.5V to ±12V or a single +5V to +24V supply. The input and output terminals are fully protected; the input signal can exceed the power supply with no damage to the device (allowing the presence of input signals in the absence of supply voltage) and the output buffer amplifier is short-circuit protected.

The AD636 includes an auxiliary dB output. This signal is derived from an internal circuit point which represents the logarithm of the rms output. The 0dB reference level is set by an externally supplied current and can be selected by the user to correspond to any input level from 0dBm (774.6mV) to -20dBm (77.46mV). Frequency response ranges from 1.2MHz at a 0dBm level to over 10kHz at -50dBm.

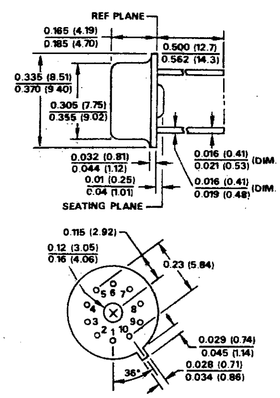
The AD636 is designed for ease of use. The device is factory-trimmed at the wafer level for input and output offset, positive and negative waveform symmetry (dc reversal), and full scale accuracy. Thus no external trims are required to achieve full rated accuracy.

The AD636 is available in two accuracy grades; the AD636J has a total error of ±0.5mV ±1.0% of reading, and the AD636K is accurate within ±0.2mV ±0.5% of reading. Both versions are specified for the 0 to 70°C temperature range, and are offered in either a hermetically sealed 14-pin DIP or a 10 pin TO-100 metal can.

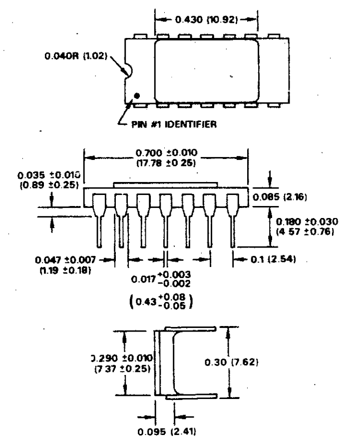
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

"H" PACKAGE
(TO-100)



"D" PACKAGE
(TO-116)



LINEAR

Analog Devices

Integrated Circuit True rms-to-dc Converter

AD637

FEATURES

High Accuracy
- **0.02% Max Nonlinearity, 0 to 2V rms Input**
- **0.10% Max Error to Crest Factor of 3**

Wide Bandwidth
- **8MHz at 2V rms Input**
- **600kHz at 100mV rms**

Computes:
- **True rms**
- **Square**
- **Mean Square**
- **Absolute Value**

dB Output (−60dB Range)

Chip Select-Power Down Feature Allows:
- **Analog "3-State" Operation**
- **Quiesent Current Reduction from 2.2mA to 350µA**

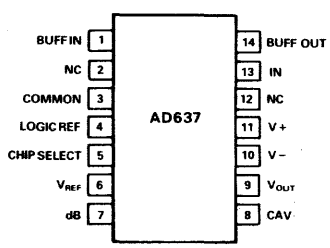
PRODUCT DESCRIPTION

The AD637 is a complete high accuracy monolithic rms to dc converter that computes the true rms value of any complex waveform. It offers performance that is unprecedented in integrated circuit rms to dc converters and comparable to discrete and modular techniques in accuracy, bandwidth and dynamic range. A crest factor compensation scheme in the AD637 permits measurements of signals with crest factors of up to 10 with less than 1% additional error. The circuit's wide bandwidth permits the measurement of signal up to 600kHz with inputs of 200mV rms and up to 8MHz when the input levels are above 2V rms.

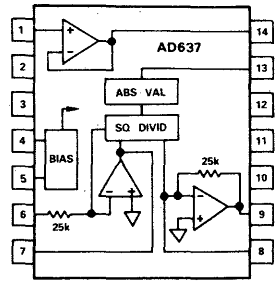
As with previous monolithic rms converters from Analog Devices, the AD637 has an auxiliary dB output available to the user. The logarithm of the rms output signal is brought out to a separate pin allowing direct dB measurement with a useful range of 60dB. An externally programmed reference current allows the user to select the 0dB reference voltage to correspond to any level between 0.1V and 2.0V rms.

A chip select connection on the AD637 permits the user to decrease the supply current from 2.2mA to 350µA during periods when the rms function is not in use. This feature facilitates the addition of precision rms measurement to remote or hand-held applications where minimum power consumption is critical. In addition when the AD637 is powered down the output goes to a high impedance state. This allows several AD637s to be tied together to form a wide-band true rms multiplexer.

PIN CONFIGURATION



AD637 FUNCTIONAL BLOCK DIAGRAM



The input circuitry of the AD637 is protected from overload voltages that are in excess of the supply levels. The inputs will not be damaged by input signals if the supply voltages are lost.

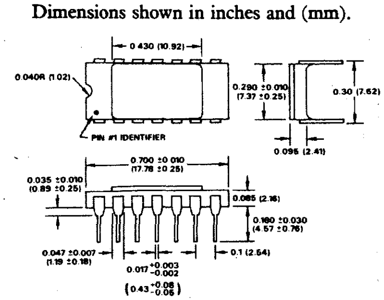
The AD637 is available in two accuracy grades (J, K) for commercial (0 to +70°C) temperature range applications and one (S) rated over the −55°C to +125°C military temperature range. All versions are available in ceramic 14-lead DIP packages.

PRODUCT HIGHLIGHTS

1. The AD637 computes the true root-mean-square, mean square, or absolute value of any complex ac (or ac plus dc) input waveform and gives an equivalent dc output voltage. The true rms value of a waveform is more useful than an average rectified signal since it relates directly to the power of the signal. The rms value of a statistical signal is also related to the standard deviation of the signal.
2. The AD637 is laser wafer trimmed to achieve rated performance without external trimming. The only external component required is a capacitor which sets the averaging time period. The value of this capacitor also determines low frequency accuracy, ripple level and settling time.
3. The chip select feature of the AD637 permits the user to power down the device down during periods of nonuse, thereby, decreasing battery drain in remote or hand-held applications.
4. The on-chip buffer amplifier can be used as either an input buffer or in an active filter configuration. The filter can be used to reduce the amount of ac ripple, thereby, increasing the accuracy of the measurement.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



14-PIN CERAMIC DIP

ANALOG DEVICES

Balanced Modulator-Demodulator

AD630

FEATURES
Recovers Signal from +100dB Noise
2MHz Channel Bandwidth
45V/μs Slew Rate
−120dB Crosstalk @ 1kHz
Pin Programmable Closed Loop Gains of ±1 and ±2
0.05% Closed Loop Gain Accuracy and Match
100μV Channel Offset Voltage (AD630BD)
350kHz Full Power Bandwidth

PRODUCT DESCRIPTION

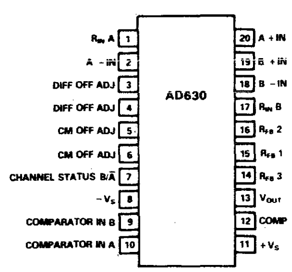
The AD630 is a high precision balanced modulator which combines a flexible commutating architecture with the accuracy and temperature stability afforded by laser wafer trimmed thin film resistors. Its signal processing applications include balanced modulation and demodulation, synchronous detection, phase detection, quadrature detection, phase sensitive detection, lock-in amplification and square wave multiplication. A network of on-board applications resistors provides precision closed loop gains of ±1 and ±2 with 0.05% accuracy (AD630B). These resistors may also be used to accurately configure multiplexer gains of +1, +2, +3 or +4. Alternatively, external feedback may be employed allowing the designer to implement his own high gain or complex switched feedback topologies.

The AD630 may be thought of as a precision op amp with two independent differential input stages and a precision comparator which is used to select the active front end. The rapid response time of this comparator coupled with the high slew rate and fast settling of the linear amplifiers minimize switching distortion. In addition, the AD630 has extremely low crosstalk between channels of −100dB @ 10kHz.

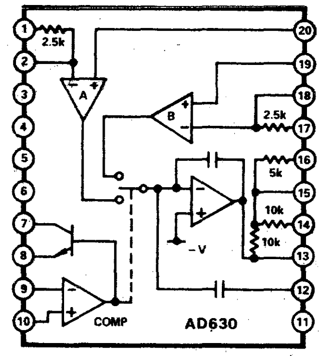
The AD630 is intended for use in precision signal processing and instrumentation applications requiring wide dynamic range. When used as a synchronous demodulator in a lock-in amplifier configuration, it can recover a small signal from 100dB of interfering noise (see lock-in amplifier application). Although optimized for operation up to 1kHz, the circuit is useful at frequencies up to several hundred kilohertz.

Other features of the AD630 include pin programmable frequency compensation, optional input bias current compensation resistors, common mode and differential offset voltage adjustment, and a channel status output which indicates which of the two differential inputs is active.

PIN CONFIGURATION



AD630 FUNCTIONAL BLOCK DIAGRAM

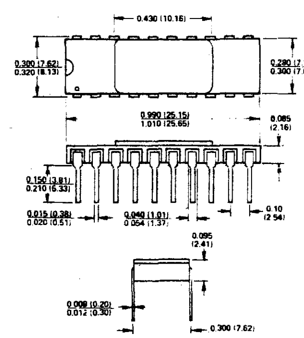


PRODUCT HIGHLIGHTS

1. The configuration of the AD630 makes it ideal for signal processing applications such as: balanced modulation and demodulation, lock-in amplification, phase detection, and square wave multiplication.
2. The application flexibility of the AD630 makes it the best choice for many applications requiring precisely fixed gain, switched gain, multiplexing, integrating-switching functions, and high-speed precision amplification.
3. The 100dB dynamic range of the AD630 exceeds that of any hybrid or IC balanced modulator/demodulator and is comparable to that of costly signal processing instruments.
4. The op-amp format of the AD630 ensures easy implementation of high gain or complex switched feedback functions. The application resistors facilitate the implementation of most common applications with no additional parts.
5. The AD630 can be used as a two channel multiplexer with gains of +1, +2, +3 or +4. The channel separation of 100dB @ 10kHz approaches the limit which is achievable with an empty IC package.
6. The AD630 has pin-strappable frequency compensation (no external capacitor required) for stable operation at unity gain without sacrificing dynamic performance at higher gains.
7. Laser trimming of comparator and amplifying channel offsets eliminates the need for external nulling in most cases.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



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ANALOG DEVICES

Wideband Dual-Channel Log-Linear Multiplier/Divider

AD539

FEATURES
Two Quadrant Multiplication/Division
Two Independent Signal Channels
Signal Bandwidth of 60MHz (I_{OUT})
Linear Control-Bandwidth of 5MHz
Fully-Calibrated, Monolithic Circuit

APPLICATIONS
Precise AGC and VCA Systems
Voltage-Controlled Filters
Video-Signal Processing
High-Speed Analog Division
Automatic Signal-Leveling
Square-Law Gain/Loss Control

PRODUCT DESCRIPTION
The AD539 is a low-distortion analog multiplier having two identical signal channels (Y1 and Y2), with a common X-input providing linear control of gain. Excellent ac characteristics up to video frequencies and a 3dB bandwidth of over 60MHz are provided. Although intended primarily for applications where speed is important the circuit exhibits good static accuracy in "computational" applications. Scaling is accurately determined by a band-gap voltage reference and all critical parameters are laser-trimmed during manufacture.

The full bandwidth can be realized over most of the gain range using the AD539 with simple resistive loads of up to 100Ω. Output voltage is restricted to a few hundred millivolts under these conditions. Using external op amps in conjunction with the on-chip scaling resistors, accurate multiplication and large output voltages can be achieved, but with a reduction in bandwidth typically to 25MHz.

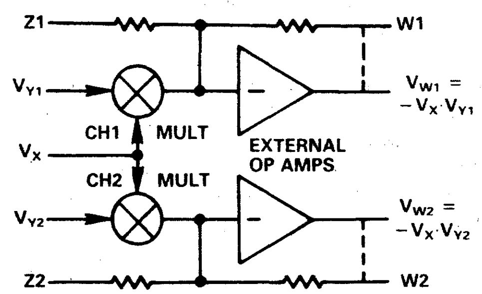
The two channels provide flexibility. In single-channel applications they may be used in parallel, to double the output current, or in series, to achieve a square-law gain function with a control range of over 100dB, or differentially, to reduce distortion. Alternatively, they may be used independently, as in audio stereo applications, with low crosstalk between channels. Voltage-controlled filters and oscillators using the "state-variable" approach are easily designed, taking advantage of the dual channels and common control. The AD539 can also be configured as a divider with signal bandwidths up to 15MHz.

Power consumption is only 135mW using the recommended ±5V supplies. The AD539 is available in three versions: the "J" and "K" grades are specified for 0 to +70°C operation and "S" grade is guaranteed over the extended range of −55°C to +125°C. All versions are packaged in 16-pin DIPs.

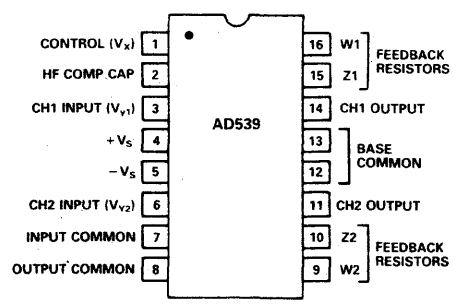
LINEAR

Analog Devices

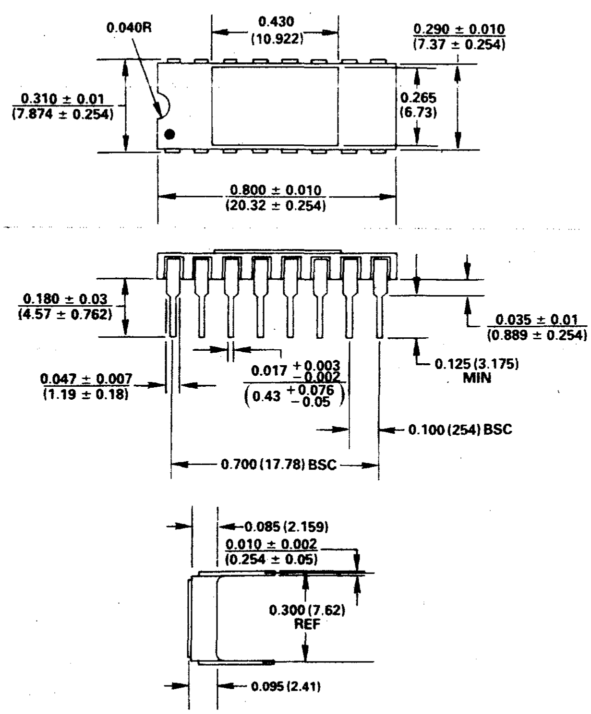
AD539 FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION & DIMENSIONS
Dimensions shown in inches and (mm).



TO-116



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ANALOG DEVICES

Analog Computational Circuits

COMPUTATIONAL CIRCUITS

SPECIFICATIONS (typical @ +25°C and rated supply voltage unless noted otherwise)

Model	Transfer Function	Full Scale Accuracy - % Max	Accuracy vs. Temperature %/°C	X Nonlinearity % of Full Scale	Y Nonlinearity % of Full Scale	Bandwidth Small Signal MHz	Operating Power Supply Volts	Operating Temperature Range[1]
AD531J	XY/kI_z	2	0.04	0.8	0.3	1	±15 to ±18	C
AD531K	XY/kI_z	1	0.03	0.5	0.2	1	±15 to ±18	C
AD531L	XY/kI_z	0.5	0.01	0.3	0.2	1	±15 to ±18	C
AD531S	XY/kI_z	1	0.03 max	0.5	0.2	1		M
AD532J	$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10}$	2	0.04	0.8	0.3	1	±15 to ±18	C
AD532K	$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10}$	1	0.03	0.5	0.2	1	±15 to ±18	C
AD532S	$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10}$	1	0.04 max	0.5	0.2	1		M
AD533J	XY/10	2	0.04	0.8	0.3	1	±15 to ±18	C
AD533K	XY/10	1	0.03	0.5	0.2	1	±15 to ±18	C
AD533L	XY/10	0.5	0.01	0.5	0.2	1	±15 to ±18	C
AD533S	XY/10	1	0.01	0.5	0.2	1		M
AD534J	$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10 + Z_2}$	1	0.022	0.4	0.01	1	±8 to ±18	C
AD534K	$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10 + Z_2}$	0.5	0.015	0.3 max	0.01 max	1	±8 to ±18	C
AD534L	$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10 + Z_2}$	0.25	0.008	0.12 max	0.01 max	1	±8 to ±18	C
AD534S	$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10 + Z_2}$	1	0.02 max	0.4	0.01	1	±8 to ±18	M
AD534T	$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10 + Z_2}$	0.5	0.01 max	0.3 max	0.01 max	1	±8 to ±18	M
AD539J	V_xV_{y1}, V_xV_{y2} (Note 2)	2.5	5% Total[3]	0.5dB[4]	–	30 min	±4.5 to ±16.5	C
AD539K	V_xV_{y1}, V_xV_{y2} (Note 2)	1.5	2% Total[3]	0.2dB[4]	–	30 min	±4.5 to ±16.5	C
AD539S	V_xV_{y1}, V_xV_{y2} (Note 2)	2.5	5% Total[3]	0.5dB[4]	–	30 min	±4.5 to ±16.5	M

NOTES
[1] C: 0 to +70°C, M: -55°C to +125°C [2] Channels 1 & 2 [3] Multiplier scaling voltage [4] Absolute gain error

RMS-TO-DC CONVERTERS

SPECIFICATIONS (typical @ +25°C and rated supply voltage unless otherwise noted)

Model	Transfer Function	Conversion Accuracy	Conversion Accuracy vs. Temperature	Input Signal Range	I_{OUT} Scale Factor	Bandwidth Full Scale	Operating Power Supply Volts	Operating Temperature Range[1]
AD536AJ	$V_{OUT} = \sqrt{avg. (V_{IN})^2}$	±5mV ±0.5% of RDG max	±(0.1mV ±0.01% of RDG)/°C	±10V	40μA/V rms	2MHz	+5 to ±18	C
AD536AK	$V_{OUT} = \sqrt{avg. (V_{IN})^2}$	±2mV ±0.2% of RDG max	±(0.05mV ±0.005% of RDG)/°C	±10V	40μA/V rms	2MHz	+5 to ±18	C
AD536AS	$V_{OUT} = \sqrt{avg. (V_{IN})^2}$	±5mV ±0.5% of RDG max	±(0.1mV ±0.01% of RDG)/°C	±10V	40μA/V rms	2MHz	+5 to ±18	M
AD636J	$V_{OUT} = \sqrt{avg. (V_{IN})^2}$	±0.5mV ±1.0% of RDG max	±(0.1mV ±0.001% of RDG)/°C	±200mV	100μA/V rms	1.3MHz	+2/-2.5 to ±12	C
AD636K	$V_{OUT} = \sqrt{avg. (V_{IN})^2}$	±0.2mV ±0.5% of RDG max	±(0.1mV ±0.0005% of RDG)/°C	±200mV	100μA/V rms	1.3MHz	+2/-2.5 to ±12	C
AD637J	$V_{OUT} = \sqrt{avg. (V_{IN})^2}$	±1mV ±0.2% of RDG max	±0.4%	±10V	–	5MHz	±3.0 to ±18	C
AD637K	$V_{OUT} = \sqrt{avg. (V_{IN})^2}$	±0.5mV ±0.1% of RDG max	±0.2%	±10V	–	5MHz	±3.0 to ±18	C

NOTE
[1] C: 0 to +70°C, M: -55°C to +125°C

BALANCED MODULATOR-DEMODULATOR

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

Model	AD630
Gain	
Gain Accuracy ±1, ±2	0.05%
Gain Match	0.03%
Input Characteristics, Amplifiers & Comparator	
Input Offset Voltage	250μV
Input Bias Current	250nA
Input Offset Current	50nA
Input Impedance	15MΩ‖1.5pF

Model	AD630
AC Characteristics	
Comparator Hysteresis	1mV (0 min)
Comparator Response Time	200ns
Small Signal -3dB Bandwidth	2MHz
Slew Rate	40V/μs
System Characteristics	
CMRR	90dB
PSRR	80dB
Channel Separation @ 10kHz	-80dB

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ABBREVIATIONS OF COMPANY NAMES

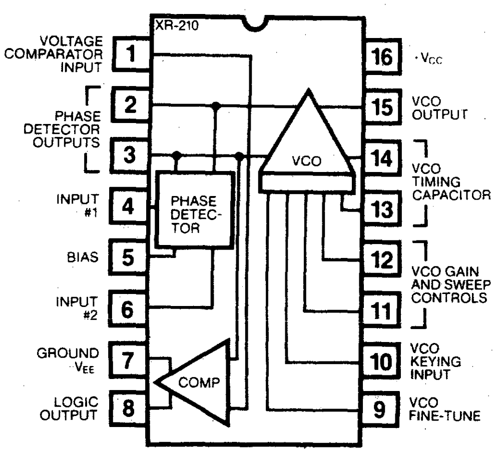
Action Ins	Action Instruments
AD	Analog Devices
ADT	Advanced Digital Technology
Advent	Advent Products, Inc.
Alphatron	Alphatron
AMA	American Automation
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
Amperex	Amperex Electronic Corp.
Analogic	Analogic
Analog Sys	Analog Systems
APC	Applied Micro Circuits
Apex	Apex Microtechnology
APM	Applied Microsystems Corp.
Appl Sys	Applied Systems Corp.
APT	Applied Microtechnology
Aptek	Aptek Microsystems
Array Tech	Array Technology
AWI	AWI Electronics
Barvon	Barvon Research
Bedford	Bedford Computer Systems Inc.
Burr-Brown	Burr-Brown
CAE	Computer Aided Engineering
Cal Devices	California Devices
Cermetek	Cermetek
CGRS	CGRS Microtech Inc.
Cherry	Cherry Semiconductor
CIC	Custom Integrated Circuits
CirTech	Circuit Technology
Citel	Citel
Comlinear	Comlinear Corporation
CMA	Custom MOS Arrays
Comark	Comark Corp.
Comdial	Comdial Semiconductor
Comp Auto	Computer Automation
Compas	Compas Microsystems
Cont Logic	Control Logic Inc.
Control Sys	Control Systems Microsystems Div.
CreMicro	Creative Micro Systems
Cromemco	Cromemco, Inc.
Cubit	Cubit Inc.
Curtis	Curtis Electro Devices, Inc.
Cybernetic	Cybernetic Micro Systems
Cybersys	Cybersystems
Cybertek	Cybertek Inc.
Data General	Data General
Data I/O	Data I/O
Data Trans	Data Translation
Datel	Datel
Datricon	Datricon Corporation
DDC	Data Devices Corporation
DEC	Digital Equipment Corporation
Die-Tech	Die-Tech
Digelec	Digelec Corp.
Digitek	Digitek, Inc.
Dionics	Dionics Inc.
Dist Comp	Distributed Computer Systems
Divers Tech	Diversified Technology
E-HI	E-H International, Inc.
EDI	Electronic Designs Inc.
Elind	Elind Elettronica Industriale
EMM-SESCO	EEM-SESCO
Emulogic	Emulogic Inc.
ETI Micro	ETI Micro
Exar	Exar Integrated Systems
Exel	Exel Microelectronics
Fairchild	Fairchild
Ferranti	Ferranti Electric
Force	Force Computers
Fujitsu A	Fujitsu America
Fujitsu	Fujitsu Microelectronics, Inc.
GI	General Instrument
GTE Micro	GTE Microcircuits
Harris	Harris Semiconductor
Heurikon	Heurikon Corp.
Hilevel	Hilevel Technology, Inc.
Hitachi	Hitachi America, Ltd.
Holt	Holt Inc.
HP	Hewlett-Packard
Hughes	Hughes Aircraft, Solid State Products
Hybrid Sys	Hybrid Systems
HyComp	HyComp
ICC	International Cybernetics
IDT	Integrated Device Technology
IMI	International Microcircuits, Inc.
IMP	International Microelectronic Products
IMS	Industrial MicroSystems Inc.
Infosphere	Infosphere
Inmos	Inmos
IntCirEng	Integrated Circuit Engineering
IntCirSys	Integrated Circuit Systems
IntCompSys	Integrated Computer Systems
Int Tech	Integrated Technology Corp.
Intech	Intech Microcircuits Div.
Intel	Intel
Interdesign	Interdesign
Intersil	Intersil
Intronics	Intronics
ITT	ITT Semiconductors
Kinetic Sys	Kinetic Systems
Kontron	Kontron Electronics
Lambda	Lambda Semiconductor
Linear Tech	Linear Technology
LSI Comp	LSI Computer Systems
LSI Logic	LSI Logic Corporation
Master Logic	Master Logic Corporation
Matrix	Matrix Corp.
Matrox	Matrox Electronic Systems
Maxim	Maxim Integrated Products
MCC	Micro-Computer Control
MCE	MCE Electronics
Micrel	Micrel
Micro Innov	Micro Innovators
Micropac	Micropac Industries
Micro Net	Micro Networks
Micro Pwr	Micro Power Systems
Micro Sci	Micro Sciences Corp.
Micro Tech	Microcircuits Technology
Micro-Link	Micro-Link Corporation
Micron	Micron Technology
MilerTron	MilerTronics
Miller	Miller Technology
Mitel	Mitel Semiconductor
Mitsubishi	Mitsubishi Electronics
MMI	Monolithic Memories, Inc.
Mostek	Monolithic Systems Corp.
Motorola	Mostek
MRC	Motorola Semiconductor
Murray	MRC Systems
Monosil	Murray Consulting
National	National Semiconductor
NCM	NCM Corp.
NCR	NCR Corp., Microelectronics Division
NEC	NEC Electronics
Nitron	Nitron
OAE	Oliver Advanced Engineering
Octagon	Octagon Systems Corp.
OEI	Optical Electronics Inc.
Ohio Sci	Ohio Scientic
OKI	OKI Semiconductor
Omnibyte	Omnibyte Corp.
Onset	Onset Computer Corp.
Panasonic	Panasonic
Pico Design	Pico Design
Polycore	Polycore Electronics
Plessey	Plessey Semiconductors
PMI	Precision Monilithics, Inc.
PragDes	Pragmatic Design Inc.
Pro-Log	Pro-Log Corp.
Quay	Quay Corp.
Raytheon	Raytheon Semiconductor
RCA	RCA Solid State Division
RCI Data	RCI Data
RELMS	Relational Memory Systems
Reticon	Reticon
RIFA	RIFA
Rockwell	Rockwell, Microelectronic Devices
RTC	Riehl Time Corporation
Sanyo	Sanyo
SBE	SBE, Inc.
SEEQ	SEEQ Technology, Inc.
SPI	Semi Processes Inc.
Siemens	Siemens
Si-Fab	Si-Fab
Signetics	Signetics
SGS	SGS Semiconductor
Sharp	Sharp
Silicon G	Silicon General
Siliconix	Siliconix
Silicon Sys	Silicon Systems Inc.
Siltronics	Siltronics
SMC	Standard Microsystems Corp.
S MOS	S MOS Systems
Solarise	Solarise Enterprises
Solitron	Solitron Devices
Sprague	Sprague Electric Company
SSM	Solid State Micro Technology for Music
SSS	Solid State Scientific
Stag	Stag Microsystems
STC	Storage Technology Corp.
STD	STD Microsystems
Struc Des	Structured Design Inc.
Stynetic	Stynetic Systems
Sunrise	Sunrise Electronics
Sunshine	Sunshine Semiconductor
Supertex	Supertex Inc.
Symtek	Symtek Corp.
Synertek	Synertek
Sys Innov	Systems Innovations
Tau Zero	Tau Zero Inc.
Technitrol	Technitrol
Tektronix	Tektronix
Teledyne C	Teledyne Crystalonics
Teledyne P	Teledyne Philbrick
Teledyne S	Teledyne Semiconductor
Telefunken	Telefunken
Telmos	Telmos
Teltone	Teltone Corporation
TI	Texas Instruments
Third Domain	Third Domain
Thomson-CSF	Thomson-CSF Components Corp.
Toshiba	Toshiba America
Trans-Data	Trans-Data
TRW	TRW LSI Products
Unitrode	Unitrode
Universal	Universal Semiconductor, Inc.
Varix	Varix Corp.
VLSI Design	VLSI Design Associates
VTI	VLSI Technology, Inc.
Votrax	Votrax
Weitek	Weitek Corporation
Western	Western Digital
Wintek	Wintek Corp.
Xicor	Xicor, Inc.
Xycom	Xycom
Zendex	Zendex Corp.
Zilog	Zilog
ZyMOS	ZyMOS Corporation
Zytrex	Zytrex Corp.

Phase-Locked Loops

XR-210 FSK MODULATOR/ DEMODULATOR

The XR-210 is a highly versatile monolithic phase-locked loop system especially designed for data communications. It is particularly well suited for FSK modulation/demodulation (MODEM) applications, frequency synthesis, tracking filters and tone decoding. The XR-210 operates over a power supply range of 5V to 26V, and over a frequency band of 0.5 Hz to 20 MHz. The circuit can accomodate analog signals between 300 μV and 3V, and can interface with conventional DTL, TTL, and ECL logic families.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Digital Programming Capability	
RS-232C Compatible Demodulator Output	
ON-OFF Keying & Sweep Capability	
Wide Tracking Range	± 1% to ± 50%
Good Temperature Stability	200 ppm/°C
High Current Logic Output	50 mA
Independent "Mark" and "Space" Frequency Adjustment	
VCO Duty Cycle Control	

APPLICATIONS

Data Synchronization	Signal Conditioning
FSK Generation	Tone Decoding
Frequency Synthesis	FSK Demodulation
Tracking Filter	FM Detection
FM and Sweep Generation	Wideband Discrimination

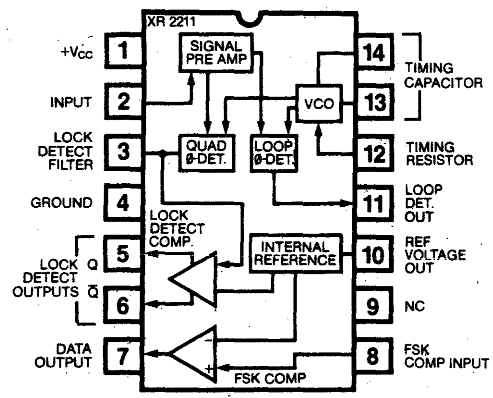
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-210M	Ceramic	-55°C to +125°C
XR-210CN	Ceramic	0°C to +70°C

XR-2211 FSK DEMODULATOR/ TONE DECODER

The XR-2211 is a monolithic phase-locked loop system especially designed for data communications, and particularly well-suited for FSK modem applications. It has a supply voltage range of 4.5V to 20V and a wide frequency range of 0.01 Hz to 300 kHz. The circuit accomodates analog signals between 2 mV and 3V, and interfaces with conventional DTL, TTL, and ECL logic families. The XR-2211 consists of a basic PLL for tracking an input signal within the passband, a quadrature phase detector for carrier detection, and an FSK voltage comparator for FSK demodulation. Independent external components set the center frequency, bandwidth, and output delay.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Wide Frequency Range	0.01 Hz to 300 kHz
Wide Supply Voltage Range	4.5V to 20V
DTL/TTL/ECL Logic Compatibility	
Wide Dynamic Range	2 mV to 3V rms
Adjustable Tracking Range	± 1% to ± 80%
Excellent Temperature Stability	20 ppm/°C, Typical
FSK Demodulation with Carrier-Detection	

APPLICATIONS

FSK Demodulation	FM Detection
Data Synchronization	Carrier Detection
Tone Decoding	

ORDERING INFORMATION

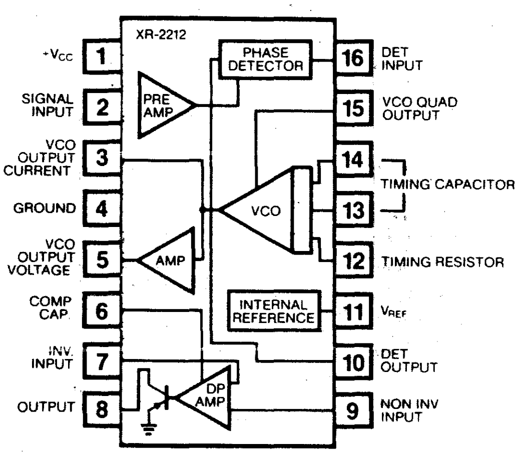
Part Number	Package	Operating Temperature
XR-2211M	Ceramic	-55°C to +125°C
XR-2211N	Ceramic	-40°C to +85°C
XR-2211P	Plastic	-40°C to +85°C
XR-2211CN	Ceramic	0°C to +70°C
XR-2211CP	Plastic	0°C to +70°C

Phase-Locked Loops

XR-2212 PRECISION PHASE-LOCKED LOOP

The XR-2212 is an ultra-stable monolithic phase-locked loop (PLL) system especially designed for data communication and control system applications. It is ideally suited for frequency synthesis, FM detection, and tracking filter applications. The circuit consists of a PLL system made up of an input preamplifier, a phase detector, a stable voltage-controlled oscillator (VCO), and a high-gain differential amplifier. The center frequency, bandwidth, and tracking range of the PLL are controlled independently by the choice of external components.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Quadrature VCO Outputs	
Wide Frequency Range	0.01 Hz to 300 kHz
Wide Supply Voltage Range	4.5V to 20V
Adjustable Tracking Range	± 1% to ± 80%
Excellent Temperature Stability	20 ppm/°C, Typical

APPLICATIONS

Frequency Synthesis	FSK Demodulation
Data Synchronization	Tracking Filters
FM Detection	Clock Extraction
Signal Conditioning	

ORDERING INFORMATION

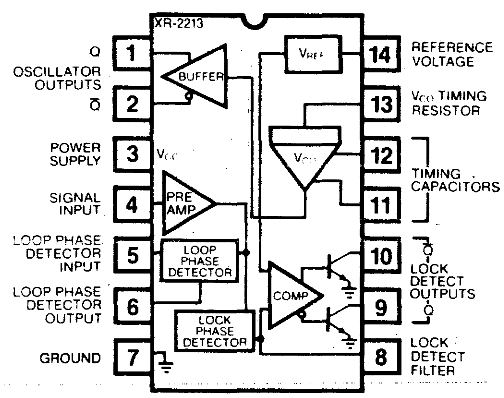
Part Number	Package	Operating Temperature
XR-2212M	Ceramic	-55°C to +125°C
XR-2212N	Ceramic	-40°C to +85°C
XR-2212P	Plastic	-40°C to +85°C
XR-2212CN	Ceramic	0°C to +70°C
XR-2212CP	Plastic	0°C to +70°C

XR-2213 PRECISION PHASE-LOCKED LOOP/TONE DECODER

The XR-2213 is a high-stability phase-locked loop system designed for control systems and tone detection applications. The circuit features a high-stability V_{CO}, an input preamplifier and a high-gain voltage comparator, in addition to loop and quadrature-phase detectors.

The XR-2213 has an operating frequency range of 0.01 Hz to 300 kHz. The input preamplifier allows an input signal range of 2 mV to 3 volts rms, while the V_{CO} and comparator supply TTL-compatible output signals. The V_{CO} and voltage comparator provide both Q and $\overline{Q}$ outputs for greater flexibility and reduced external parts count. All of the loop parameters are independently adjustable by the choice of external components.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Wide Frequency Range	0.01 Hz to 300 kHz
Wide Supply Voltage Range	4.5V to 15V
Uncommitted V_{CO} Q and $\overline{Q}$ Outputs	
Wide Dynamic Input Voltage Range	2 mV to 3V rms
Excellent V_{CO} Stability	20 ppm/°C, Typical

APPLICATIONS

Tone Detection	FM Detection
Frequency Synthesis	Tracking Filters

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2213M	Ceramic	-55°C to +125°C
XR-2213N	Ceramic	-40°C to +85°C
XR-2213P	Plastic	-40°C to +85°C
XR-2213CN	Ceramic	0°C to +70°C
XR-2213CP	Plastic	0°C to +70°C

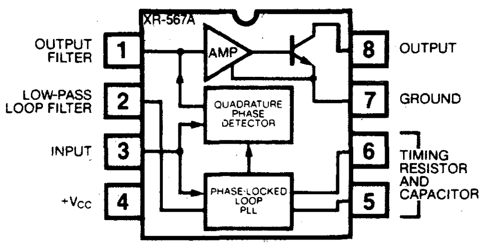
EXAR

Tone Decoders

XR-567/567A MONOLITHIC TONE DECODER

The XR-567 is a monolithic phase-locked loop system designed for general purpose tone and frequency decoding. It offers a wide frequency band of 0.01 Hz to 500 kHz, and has a logic compatible output capable of sinking up to 100 mA of load current. Four independent external components determine the bandwidth, center frequency, and output delay. The XR-567A offers improved frequency accurancy and drift characteristics over the standard 567. The improved design enhances overall circuit performance, while reducing initial circuit adjustments.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct Replacement for SE/NE567	
Adjustable Bandwidth	0% to 14%
Logic Compatible Output with Current Sinking Capability	100 mA
Adjustable Center Frequency	0.01 Hz to 500 kHz
Inherent Immunity to False Signals	
High Rejection of Out-of-Band Signals and Noise	
Adjustable Range Frequency by External Resistor	over 20:1 range

APPLICATIONS

Touch-Tone® Decoding
Sequential Tone Decoding
Communications Paging
Ultrasonic Remote Control and Monitoring
Carrier-Tone Transceiver
Wireless Intercom
Precision Oscillator

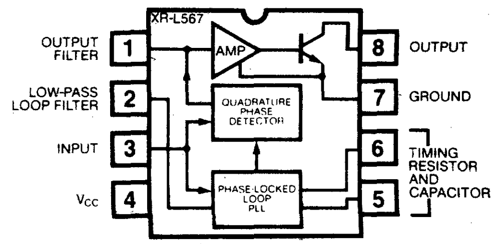
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-567M/AM	Ceramic	-55°C to +125°C
XR-567CN/ACN	Ceramic	0°C to +70°C
XR-567CP/ACP	Plastic	0°C to +70°C

XR-L567 MONOLITHIC TONE DECODER

The XR-L567 is a micropower phase-locked loop (PLL) circuit designed for general purpose tone and frequency decoding. It is a direct replacement for the popular 567-type tone decoder ICs, designed for applications requiring very low power dissipation. The XR-L567 offers approximately 1/10th the power dissipation of the conventional 567-type tone decoder, without sacrificing its key features, such as oscillator stability, frequency selectivity and detection threshold. At 5-volt operation, typical quiescent power dissipation is less than 4 mW.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Very Low Power Dissipation	< 4 mW at 5V
Adjustable Bandwidth	0% to 14%
Logic Compatible Output with 10 mA Current Sinking Capability	
Highly Stable Center Frequency	
Adjustable Center Frequency	0.01 Hz to 50 kHz
Inherent Immunity to False Signals	
High Rejection of Out-of-Band Signals and Noise	
Adjustable Frequency Range by External Resistor	over 20:1 range

APPLICATIONS

Battery Operated Tone Detection
Touch-Tone® Decoding
Communications Paging
Ultrasonic Remote Control
Telemetry Decoding

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-L567CN	Ceramic	0°C to +70°C
XR-L567CP	Plastic	0°C to +70°C

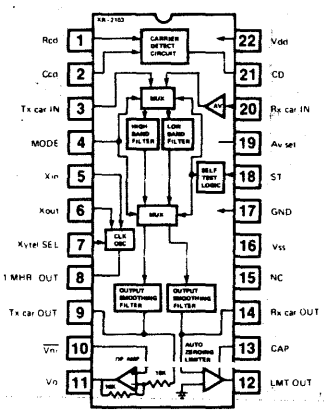
EXAR

Filters

XR-2103 FSK MODEM FILTER

The XR-2103 is a Monolithic Switched-Capacitor Filter designed to perform the complete filtering function necessary for a Bell 103 Compatible Modem. The XR-2103 is specifically intended for use with the XR-14412 Modulator/Demodulator to form a complete stand alone two-chip Modem. In addition to complete high and low bandpass filters, the XR-2103 contains internal mode switching, auto-zeroing limiter and dedicated duplexer op amp. An on-board carrier detect circuit is also included to complete the over-all system. Designed for crystal-controlled operation, the XR-2103 may operate from a 4.0 MHz crystal or 1 MHz input from the XR-14412. A self-test circuit is included to complement that of the XR-14412.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Single 5 Volt Operation
4.0 MHz/1 MHz Clock Input
Complete On-board Output
Active Filters
Low Supply Current
Internal Answer/Originate Mode Switching
Programmable Input Receive Gain

APPLICATIONS

Bell 103 Transmit/Receive Filtering
Complement to XR-14412 or other
Modulator/Demodulators

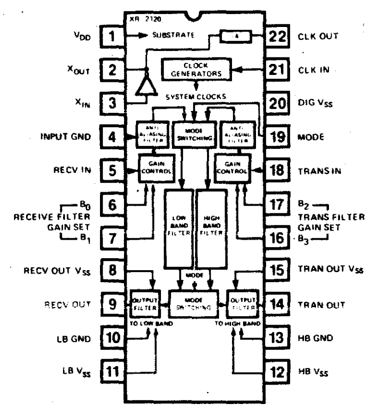
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2103CP	Plastic	0°C to 70°C
XR-2103CN	Ceramic	0°C to 70°C

XR-2120 PSK MODEM FILTER

The XR-2120 is a self-contained bandpass filter set designed for realization of Bell 212A compatible 1200 bits/sec PSK MODEMS. The XR-2120 utilizes CMOS technology and switched capacitor circuit techniques to minimize external components to a single crystal or frequency source. Contained in the device are two complete bandpass filters centered around the Bell standard 1200 Hz and 2400 Hz send and receive frequencies. These filters also provide compromise line equalization. Additional features included are digitally programmable transmit and receive gains as well as input anti-aliasing and complete output smoothing filters. Separate V_{SS} pins for transmit, receive, and digital sections are provided to minimize crosstalk.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

On-board Crystal Oscillator With Buffered Output
Internal Anti-aliasing Filters
Complete On-board Output Active Filters
Digitally Programmable Transmit and Receive Gains
MODE Input Internally Switches Filters
for Answer/Originate
Single or Split Supply Operation
Center Frequencies Movable with Input Clock
High-Impedance Inputs (100 kΩ min)
Low Supply Current
1% Center Frequency Accuracy
Separate CLK IN and CLK OUT Pins

APPLICATIONS

Bell 212A Transmit/Receive Filtering
Answer Back Signal Filtering

ORDERING INFORMATION

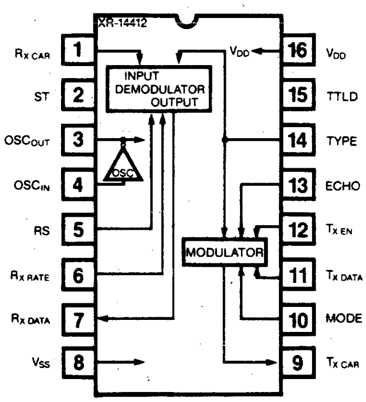
Part Number	Package	Operating Temperature
XR-2120CN	Ceramic	0°C to +70°C
XR-2120CP	Plastic	0°C to +70°C

Modem Circuits

XR-14412 FSK MODEM SYSTEM

The XR-14412 contains all the necessary circuitry to construct a complete FSK modulator/demodulator (MODEM) system. Included is circuitry for pin-programmable frequency bands, either U.S. or foreign (CCITT) standards for low-speed MODEMS. The XR-14412 provides TTL-compatible inputs and outputs. Included in the XR-14412 are features for self-testing and an echo suppression tone generator. The XR-14412 utilizes complementary MOS technology for low-power operation.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Simplex, Half-Duplex, and Full Duplex Operation
Crystal Controlled
Answer or Originate Modes
Single Supply Operation
Self-test Mode
Selectable Data Rates 300 or 600 bps
TTL, or CMOS-Compatible Inputs and Outputs
Echo Suppressor Disable Tone Generator
U.S. or Foreign (CCITT) Compatible

APPLICATIONS

Stand-Alone MODEMS
Remote Terminals
Acoustical Couplers
Built-in MODEMS

ORDERING INFORMATION

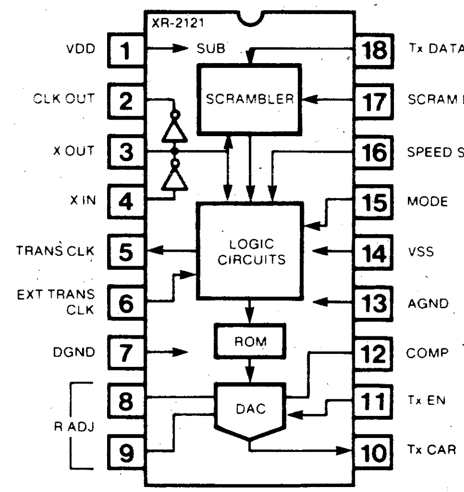
Part Number	Package	Operating Temperature
XR-14412FN	Ceramic	-40°C to +85°C
XR-14412VN	Ceramic	-40°C to +85°C
XR-14412FP	Plastic	-40°C to +85°C
XR-14412VP	Plastic	-40°C to +85°C

XR-2121 BELL 212A MODULATOR

The XR-2121 is designed to provide the complete modulator function for the Bell Standard 212A PSK Modem. It can be used with the XR-2120 PSK Filter, XR-2122 Demodulator, and XR-2125 Sync/Async Converter to provide a four chip solution for realizing this 1200/300 bps Modem System.

The XR-2121 Modulator provides either a 1200 bps PSK or 0 to 300 bps FSK output. Crystal controlled operation offers extremely accurate and stable 1200/2400 Hz carriers for the PSK and 1170/2125 Hz carriers for the FSK. An enable/disable pin is provided for blanking the modulator output. A transmit clock of 1200 Hz is also provided for synchronization of the terminal and other facilities. The XR-2121 is designed to operate from dual 5-volt power supplies and utilizes CMOS technology for low power consumption.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Bell Standard 212A Compatible
6-Bit Synthesized Sine Wave Output
Internal Scrambler
Enable/Disable Input
1200 Hz Transmit Clock Output
Crystal Controlled with Buffered Clock Output
External Clock Input
CMOS/TTL Compatible Inputs

APPLICATIONS

Stand-Alone Modems
Remote Terminals
Built-In Modems

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2121CN	Ceramic	0°C to +70°C
XR-2121CP	Plastic	0°C to +70°C

EXAR

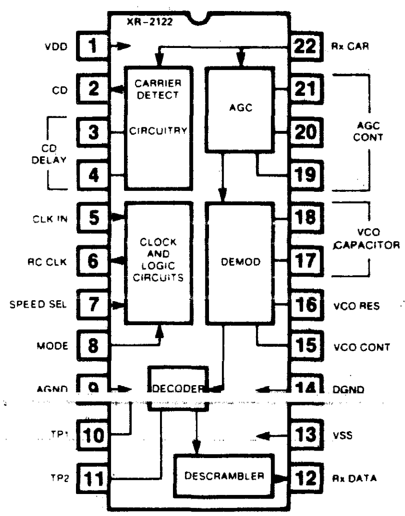
Modem Circuits

XR-2122 BELL 212A DEMODULATOR

The XR-2122 is designed to provide the complete demodulator function for the Bell Standard 212A PSK Modem. It can be used with the XR-2120 PSK Filter, XR-2121 Modulator, and XR-2125 Sync/Async Converter to provide a four chip solution for realizing this 1200/300 bps Modem System.

The XR-2122 Demodulator provides the complete demodulation function for either 1200 bps PSK or 0 to 300 bps FSK incoming carriers. An internal descrambler, automatic gain control circuit, and carrier detect circuit are also provided. The XR-2122 is designed to operate from dual 5-volt power supplies and utilizes CMOS technology for low power consumption.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Bell Standard 212A Compatible
Automatic Speed Selection in Answer Mode
36 dB (-9 to -45 dBm) Dynamic Input Range
On-Board Descrambler
Carrier Detect Output
Crystal Controlled Operation
CMOS/TTL Compatible Inputs and Outputs

APPLICATIONS

Stand-Alone Modems
Remote Terminals
Built-In Modems

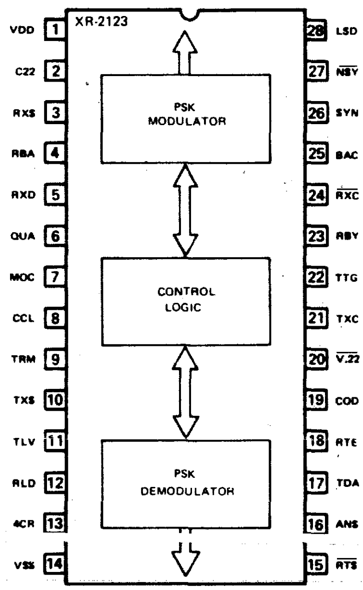
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2122CN	Ceramic	0°C to +70°C
XR-2122CP	Plastic	0°C to +70°C

XR-2123 PSK MODULATOR/DEMODULATOR

The XR-2123 provides the phase-shift keying (PSK) Modulator and Demodulator Functions for implementing a Full-Duplex 1200 bps or Half-Duplex 2400 bps Modem System. Using fully digital circuit techniques allows the XR-2123 to be externally programmed for operation for Bell Standards 201B and C or 212A (1200 bps only), and CCITT V.22 or V.26. Internal logic and timing functions minimize external parts while crystal controlled operation provides stable and accurate operation.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

CMOS Technology
Single +5 Volt Operation
Low Power Consumption (Typ 10mw)
1200 bps Full-Duplex
2400 bps Half-Duplex
Programmable for US or European Standards (CCITT)
Dibit PSK (DPSK) Operation
Crystal Controlled
Synthesized Sine Wave Modulator Output
Adjustable Modulator Output
Input Protection

APPLICATIONS

Bell Standard 201 or 212A Modems
CCITT Standard V.22 or V.26 Modems

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2123CN	Ceramic	0°C to +70°C
XR-2123CP	Plastic	0°C to +70°C

EXAR

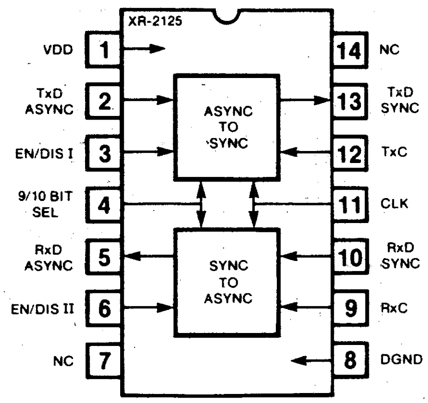
Modem Circuits

XR-2125 SYNC/ASYNC CONVERTER

The XR-2125 is designed to provide the interface between asynchronous digital equipment and the synchronous operation of the modulator and demodulator functions in a Bell Standard 212A PSK Modem. It can be used with the XR-2120 PSK Filter, XR-2121 Modulator, and XR-2122 Demodulator to provide a four chip solution for realizing this 1200/300 bps Modem System.

The XR-2125 maintains proper timing of data by inserting or removing stop bits when interfacing with asynchronous digital equipment. Enable/Disable pins are provided to allow straight-through operation when interfacing with synchronous equipment. Operation with character lengths of either 9 or 10 bits may be selected also. The XR-2125 is designed to operate from a single 5-volt supply and utilizes CMOS technology for low power consumption.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Bell Standard 212A Compatible
Enable/Disable Inputs
Crystal Controlled Operation
CMOS/TTL Compatible Inputs
9 or 10 Bit Selection

APPLICATIONS

Stand-Alone Modems
Remote Terminals
Built-In Modems

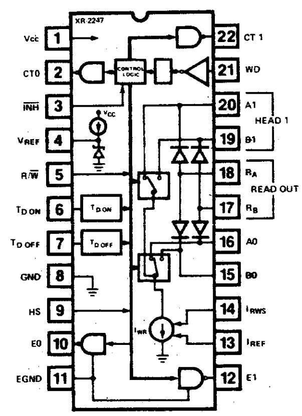
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2125CN	Ceramic	0°C to +70°C
XR-2125CP	Plastic	0°C to +70°C

XR-2247 FLOPPY DISK WRITE AMPLIFIER

The XR-2247 is a write amplifier designed to provide the complete interface between write data signals and tunnel-erase magnetic heads. Although primarily intended for floppy disk drive systems, the XR-2247 can also be used in other magnetic media systems such as tape drives. Complete internal active transistor switching is provided to minimize external parts for dual head systems. Write and erase currents are each externally programmable with a single resistor. Also included is circuitry for inner track write current compensation. To prevent false write current outputs on power-on, an inhibit input has been provided. Turn-on and turn-off times for the tunnel-erase systems are each externally programmable.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Fully Programmable Write and Erase Currents
Fully Programmable Tunnel Delay
for Turn-on/Turn-off
Internal Switching Diodes (active transistors)
for Dual Head Drives
Single Supply Operation
Inner Track Write Current Compensation
Inhibit Input
TTL Compatible Inputs
Low External Parts Count

APPLICATIONS

Floppy Disk Drives
Single/Double Head Systems
Magnetic Tape Write Amplifier

ORDERING INFORMATION

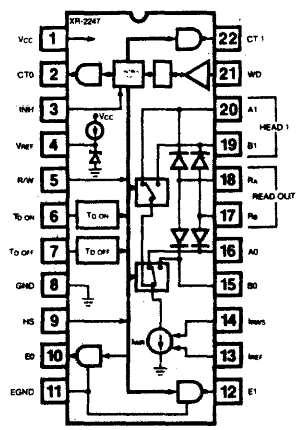
Part Number	Package	Operating Temperature
XR-2247CN	Ceramic	0°C to +70°C
XR-2247CP	Plastic	0°C to +70°C

Disk Drive Circuits

XR-2247A FLOPPY DISK WRITE AMPLIFIER

The XR-2247A is a write amplifier designed to provide the complete interface between write data signals and tunnel-erase magnetic heads. Although primarily intended for floppy disk drive systems, the XR-2247A can also be used in other magnetic media systems such as tape drives. Complete internal diode connected transistor switching is provided to minimize external parts for dual head systems. Write and erase currents are each externally programmable with a single resistor. Also included is circuitry for inner-track write current compensation. To prevent false write current outputs on power-on, an inhibit input has been provided. Turn-on and turn-off times for the tunnel-erase systems are each externally programmable.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Fully Programmable Write and Erase Currents
Fully Programmable Tunnel Delay
for Turn-on/Turn-off
Internal Switching Diodes (Diode connected transistors)
for Dual Head Drives
Single Supply Operation
Inner track Write Current Compensation
Inhibit Input
TTL Compatible Inputs
Low External Parts Count

APPLICATIONS

Floppy Disk Drives
Single/Double Head Systems
Magnetic Tape Write Amplifier

ORDERING INFORMATION

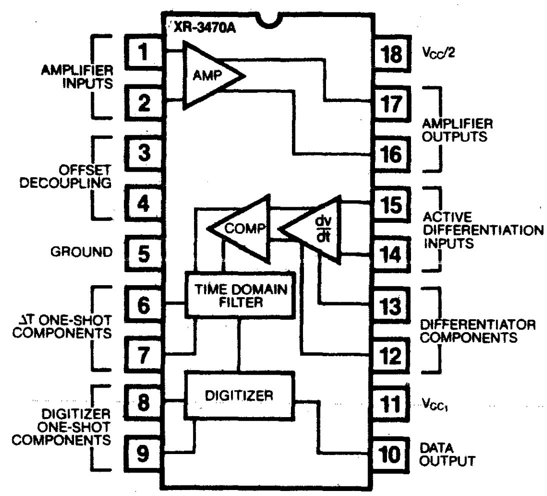
Part Number	Package	Operating Temperature
XR-2247ACN	Ceramic	0°C to +70°C
XR-2247ACP	Plastic	0°C to +70°C

XR-3470A FLOPPY DISK READ AMPLIFIER

The XR-3470A is a read amplifier system designed primarily for use in a floppy disk system. It is designed to perform the complete readback function, by accepting the readback signal from a magnetic head and converting it into digital output pulses. To perform this function, the XR-3470A contains a high frequency amplifier, an active differentiator, a zero-crossing detector, and a time domain filter.

The XR-3470A is suited for systems with data transfer rates up to 3 megabaud. High input sensitivity allows operation with signal levels as low as 1.4 mV pp, which gives it the flexability to be used for single or double density floppy disk systems.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Complete Floppy Disk Read Amplifier	
Low Input Voltage Detection	1.4 mV pp
Low Peak Shift	2.0% Maximum
Low Amplifier Gain Variation	100 V/V Min
	130 V/V Max
High Amplifier Frequency Response	10 MHz, Min

APPLICATIONS

Single/Double Density Floppy Disk Read Amplifier
Magnetic Read Amplifier

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-3470ACN	Ceramic	0°C to +70°C
XR-3470ACP	Plastic	0°C to +70°C

EXAR

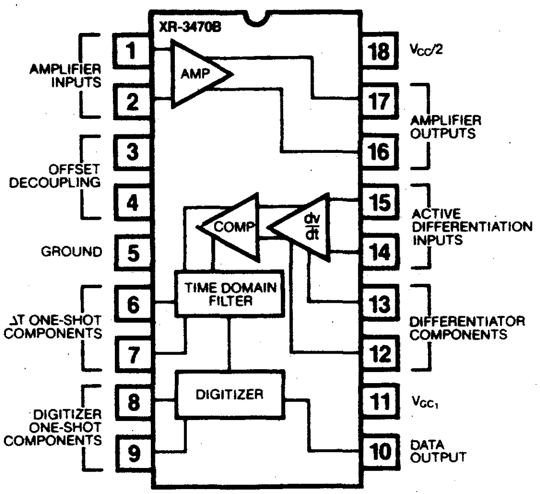
Disk Drive Circuits

XR-3470B FLOPPY DISK READ AMPLIFIER

The XR-3470B is a read amplifier system designed primarily for use in a floppy disk system. The circuit is designed to accept the readback signal from a magnetic head and convert the peaks of this signal to digital pulses. The circuit consists of a high-frequency amplifier, an active diffrentiator, a zero-crossing detector, and a time domain filter.

The XR-3470B can be used to transfer data up to 3 megabaud. This device can also detect voltage levels as low as 1.4 mV pp, which gives it the flexibility to be used for single or double density floppy disk systems. The chip contains all the circuitry essential for a floppy disk read amplifier system.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Less Than 4% Peak Shift	
Low Input Voltage Detection	
Complete Floppy Disk Read System	
Up to 3 MBaud Operation	
High Preamp Gain	110 V/V, Typical, (100 V/V, min)

APPLICATIONS

Single/Double Density Floppy Disk Read Amplifier
Magnetic Tape Read Amplifier

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-3470BCN	Ceramic	0°C to +70°C
XR-3470BCP	Plastic	0°C to +70°C

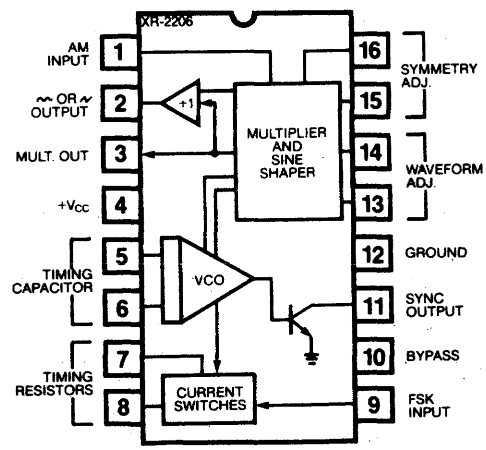
Function Generators

XR-2206 MONOLITHIC FUNCTION GENERATOR

The XR-2206 is a monolithic function generator integrated circuit capable of producing high quality sine, square, triangle, ramp, and pulse waveforms of high-stability and accuracy. The output waveforms can be both amplitude and frequency modulated by an external voltage. Frequency of operation can be selected externally over a range of 0.01 Hz to more than 1 MHz.

The circuit is ideally suited for communications, instrumentation, and function generator applications requiring sinusoidal tone, AM, FM, or FSK generation.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Low-Sine Wave Distortion	.5%, Typical
Excellent Stability	20 ppm/°C, Typical
Wide Sweep Range	2000:1, Typical
Linear Amplitude Modulation	
Adjustable Duty Cycle	1% to 99%

APPLICATIONS

Waveform Generation	V/F Conversion
Sweep Generation	FSK Generation
AM/FM Generation	Phase-Locked Loops

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2206M	Ceramic	-55°C to +125°C
XR-2206N	Ceramic	0°C to +70°C
XR-2206P	Plastic	0°C to +70°C
XR-2206CN	Ceramic	0°C to +70°C
XR-2206CP	Plastic	0°C to +70°C

EXAR

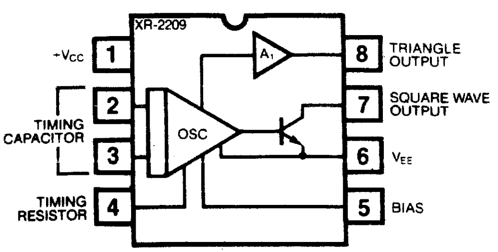
Function Generators

XR-2209 PRECISION OSCILLATOR

The XR-2209 is a monolithic variable frequency oscillator circuit featuring excellent temperature stability and a wide linear sweep range. The circuit provides simultaneous triangle and square wave outputs over a frequency range of 0.01 Hz to 1 MHz. The frequency is set by an external RC product. The device is ideally suited for frequency modulation, voltage-to-frequency or current-to-frequency conversion, sweep or tone generation, as well as for phase-locked loop applications when used in conjunction with a phase comparator such as the XR-2208.

The circuit is comprised of three functional blocks: A variable frequency oscillator and two buffer amplifiers. The XR-2209 has a typical drift specification of 20 ppm/°C. The frequency can be linearly swept over a 1000:1 range, by an external control signal.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Excellent Temperature Stability	20 ppm/°C
Linear Frequency Sweep	
Wide Sweep Range	1000:1, Minimum
Wide Supply Voltage Range	±4V to ±13V
Low Supply Sensitivity	0.15%/V
Wide Frequency Range	0.01 Hz to 1 MHz
Simultaneous Triangle and Square Wave Outputs	

APPLICATIONS

V/F Conversion	Waveform Generation
C/F Conversion	Stable Phase-Locked Loop
FM and Sweep Generation	

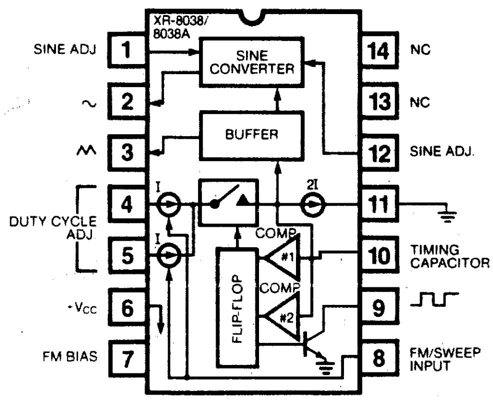
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2209M	Ceramic	-55°C to +125°C
XR-2209CN	Ceramic	0°C to +70°C
XR-2209CP	Plastic	0°C to +70°C

XR-8038/8038A PRECISION WAVEFORM GENERATOR

The XR-8038/8038A is a precision waveform generator IC capable of producing sine, square, triangular, sawtooth, and pulse waveforms with a minimum of external components and adjustments. Its operating frequency can be selected over nine decades of frequency, from 0.001 Hz to 1 MHz, by the choice of external RC components. The frequency of oscillation is highly stable over a wide temperature and supply voltage range. The frequency modulation and sweeping can be accomplished with an external control voltage, without affecting the quality of the output waveforms. The frequency can be programmed digitally through the use of either resistors or capacitors.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct Replacement for Intersil 8038	
Low Frequency Drift	50 ppm/°C
Simultaneous Sine, Triangle and Square Wave Outputs	
Low Distortion	THD 1%
High FM and Triangle Linearity	
Wide Frequency Range	0.001 Hz to 1 MHz
Minimum External Component Count	
Variable Duty Cycle	2% to 98%

APPLICATIONS

Precision Waveform Generation	Sweep Generation
Test Instrumentation Design	Precision PLL Design
Phase-Locked Clock Generation	Tone Generation

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-8038M/AM	Ceramic	-55°C to +125°C
XR-8038N/AN	Ceramic	0°C to +70°C
XR-8038P/AP	Plastic	0°C to +70°C
XR-8038CN/ACN	Ceramic	0°C to +70°C
XR-8038CP/ACP	Plastic	0°C to +70°C

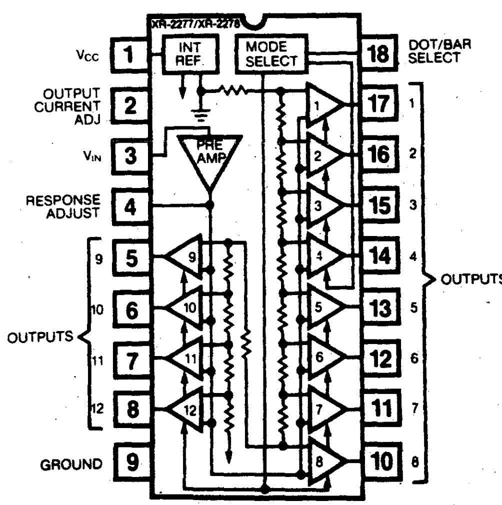
Display Drivers

XR-2277/XR-2278 DOT AND BAR-GRAPH DISPLAY GENERATORS

The XR-2277 and XR-2278 are 12-point level detector circuits designed for interfacing directly with LED moving dot or bar-graph displays. Each circuit is comprised of an input buffer amplifier, a set of 12 comparators which are biased from an internal voltage reference, and a resistor string. Each comparator provides a high-impedance current source output; each of the output currents is very closely matched and can be adjusted, simultaneously, with a single external setting resistor.

The XR-2277 has 12 discrete output levels, over a range of -30 dB to +6 dB, referenced to an externally set zero dB reference level. The XR-2278 has similar electrical characteristics, except for a dynamic range of -20 dB to +8 dB.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct LED Interface	Adjustable Zero dB Reference
Constant-Current Outputs	Adjustable Output Currents
External Mode-Select for Dot/Bar-Graph Format	High Input Impedance

APPLICATIONS

Bar-Graph Display Generator and Driver
Dot Display Generator

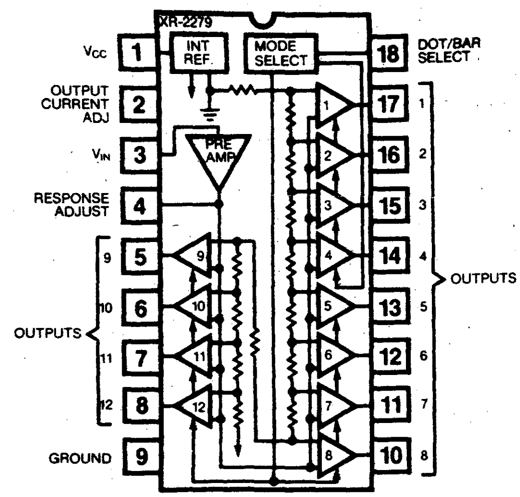
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2277CP	Plastic	0°C to +70°C
XR-2278CP	Plastic	0°C to +70°C

XR-2279 DOT AND BAR-GRAPH DISPLAY GENERATOR

The XR-2279 is a 12-point logarithmic level-detector circuit comprised of an input buffer amplifier and a set of 12 voltage comparators. The circuit produces 12 discrete output levels, spaced in three dB intervals, over a dynamic range of -27 dB to +6 dB, referenced to an externally adjusted zero dB level. It is designed for interfacing directly with LED moving dot or bar-graph displays. Each of the comparator outputs provides a high-impedance constant-current drive which is well-matched and can be adjusted by an external resistor setting. The circuit output is either a moving dot or a continuous bar-graph format, based on control voltage applied to the mode-select pin.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct LED Interface
Constant 3 dB per Step Logarithmic Scale
External Mode-Select for Dot/Bar-Graph Formats
Adjustable Output Current Levels
Adjustable Zero dB Reference

APPLICATIONS

Bar-Graph Generator	Logarithmic Level Indicator
Moving Dot Display Generator	Sequential Level Indicator

ORDERING INFORMATION

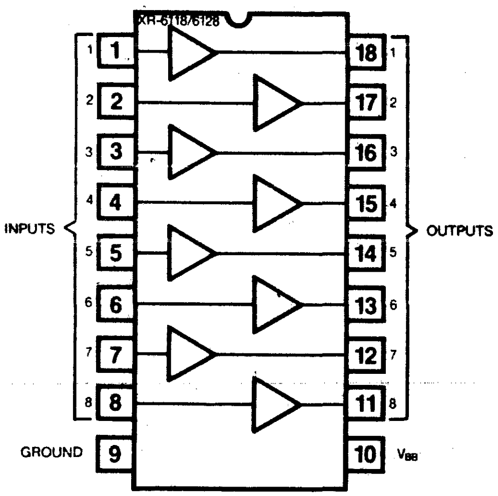
Part Number	Package	Operating Temperature
XR-2279CP	Plastic	0°C to +70°C

Display Drivers

XR-6118/6128 FLUORESCENT DISPLAY DRIVER

The XR-6118 and XR-6128 are high-voltage display driver arrays which are designed to interface between low-level digital logic and vacuum fluorescent displays. Each circuit consists of eight independent signal channels comprised of Darlington output stages and common-emitter inputs. All channels on the chip share common power supply and ground connections. Both device types are capable of driving digits and/or segments of fluorescent displays, and all of the eight outputs can be activated simultaneously. The XR-6118 is compatible with TTL and 5V CMOS logic while the XR-6128 interfaces with 6V to 15V PMOS or CMOS. The XR-6118 amd XR-6128 are designed to operate with a supply voltage of 80V, and the XR-6118-2 with a supply voltage of 60V.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct Replacement for Sprague 6118A/6128A
Digit or Segment Drivers
Low Power and Input Current
Internal Output Pulldown Resistors
High Output Breakdown Voltage 77V, Minimum

APPLICATIONS

Fluorescent Driver
High-Voltage Switching
Gas Discharge Display Driver

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-6118P	Plastic	-40°C to +85°C
XR-6128CP	Plastic	-40°C to +85°C
XR-6118CP	Plastic	0°C to +70°C
XR6128CP	Plastic	0°C to +70°C
XR-6128CP	Plastic	0°C to +70°C
XR-6118CP-2	Plastic	0°C to +70°C

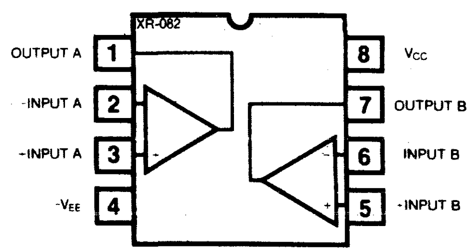
Operational Amplifiers

XR-082/083 DUAL BIPOLAR JFET OPERATIONAL AMPLIFIER

The XR-082/083 family of junction FET input dual operational amplifiers are designed to offer higher performance than conventional bipolar op amps. Each amplifier features high slew rate, low input bias and offset currents, and low offset voltage drift with temperature. These operational amplifier circuits are fabricated using ion implantation technology to combine well-matched junction FET's and high-performance bipolar transistors on the same monolithic chip.

The XR-082 family of dual bipolar JFET op amps are packaged in an 8-Pin dual-in-line package. The XR-083 family of op amps offers an independent offset adjustment for each of the individual op amps on the same chip, and are available in a 14-Pin dual-in-line package.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct Replacement for TL082/083 (See Chart)
Low Power Consumption
Wide Common-Mode and Differential Voltage Ranges
Low Input Bias and Offset Currents
Output Short Circuit Protection
High-Input Impedance . . . . FET Input Stage
Internal Frequency Compensation
Latch-Up-Free Operation
High Slew Rate 13V/µs, Typical

APPLICATIONS

Transducer Amplifier
High-Impedance Buffer

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-082M	Ceramic	-55°C to +125°C
XR-082N	Ceramic	-25°C to +85°C
XR-082P	Plastic	-25°C to +85°C
XR-082CN	Ceramic	0°C to +70°C
XR-082CP	Plastic	0°C to +70°C
XR-083	Available in 14-Pin	

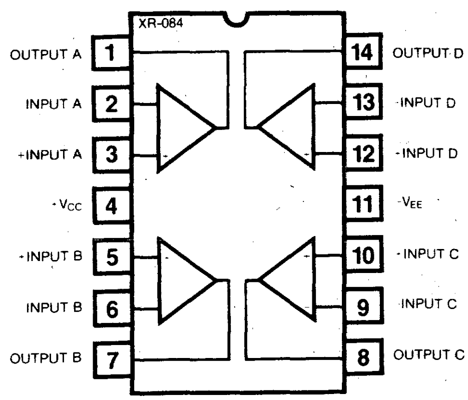
EXAR

Operational Amplifiers

XR-084 QUAD BIPOLAR JFET OPERATIONAL AMPLIFIER

The XR-084 junction FET input quad operational amplifier is designed to offer higher performance than conventional bipolar quad op amps. Each of the four op amps on the chip is closely matched in performance characteristics, and each amplifier features high slew rate, low input bias and offset currents, and low offset voltage drift with temperature. The XR-084 FET input quad op amp is fabricated using ion implantation bipolar/FET technology, to combine well-matched junction FET's and high-performance bipolar transistors on the same monolithic chip.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct Replacement for TL084 (See Table 1)
Same Pin Configuration as XR-3403 and LM324
High-Impedance Junction FET Input Stage
Low-Power Consumption
Wide Common-Mode and Differential Voltage Ranges
Low Input Bias and Offset Currents
Output Short-Circuit Protection
Internal Frequency Compensation
Latch-Up Free Operation
High Slew Rate 13V/μs, Typical

APPLICATIONS

Transducer Amplifier High-Impedance Buffer

ORDERING INFORMATION

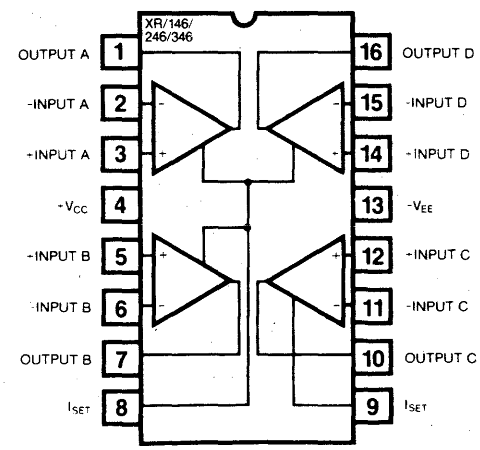
Part Number	Package	Operating Temperature
XR-084M	Ceramic	-55°C to +125°C
XR-084N	Ceramic	-25°C to +85°C
XR-084P	Plastic	-25°C to +85°C
XR-084CN	Ceramic	0°C to +70°C
XR-084CP	Plastic	0°C to +70°C

XR-146/246/346 PROGRAMMABLE QUAD OPERATIONAL AMPLIFIER

The XR-146 family of quad operational amplifiers contain four independent high-gain, low-power, programmable op amps on a monolithic chip. The use of external bias setting resistors permit the user to program the gain bandwidth product, supply current, input bias current, input offset current, input noise, and slew rate.

The basic XR-146 family of circuits offers partitioned programming of the internal op amps. One setting resistor is used to set the bias levels in the three op amps, and a second bias setting is used for the remaining op amp. Its modified version, XR-346-2, provides a separate bias setting resistor for each of the two op amp pairs.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct Replacement for LM146/246/346
Direct Replacement for LM346-2
Programmable Electrical Characteristics

Low Supply Current	350 μA per Amplifier
Large dc Voltage Gain	120 dB
Low Noise Voltage	25 nV/$\sqrt{Hz}$
Wide Power Supply Range	± 1.5V to ± 22V
Class AB Output Stage	No Crossover Distortion

ORDERING INFORMATION

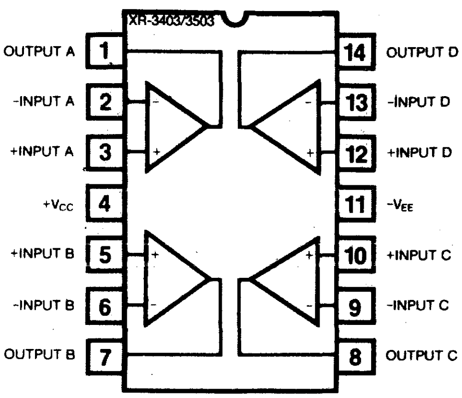
Part Number	Package	Operating Temperature
XR-146M	Ceramic	-55°C to +125°C
XR-246N	Ceramic	-25°C to +85°C
XR-246P	Plastic	-25°C to +75°C
XR-346CN	Ceramic	0°C to +70°C
XR-346CP	Plastic	0°C to +70°C
XR-346-2CN	Ceramic	0°C to +70°C
XR-346-2CP	Plastic	0°C to +70°C

Operational Amplifiers

XR-3403/3503 QUAD OPERATIONAL AMPLIFIER

The XR-3403 is an array of four independent operational amplifiers, each with true differential inputs. The device has electrical characteristics similar to the popular 741. However, the XR-3403 has several distinct advantages over standard operational amplifier types in single supply applications. The XR-3403 can operate at supply voltages as low as 3.0 volts, or as high as 36 volts. Quiescent currents remain about one-fifth of those associated with the 741 (on a per amplifier basis). The common-mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage swing extends to the negative supply.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct Pin for Pin Replacement for MC3403/3503, LM324 & RC4137	
Suitable for Single Supply Operation	
Short Circuit Protected Outputs	
Class AB Output Stage	No Crossover Distortion
Single Supply Operation	3.0V to 36V
Split Supply Operation	± 1.5V to ± 18V
Low Input Bias Currents	500 nA Maximum
Internally Compensated	

APPLICATIONS

Circuits Requiring Ground Sensing at Inputs
Low Supply Voltage Systems

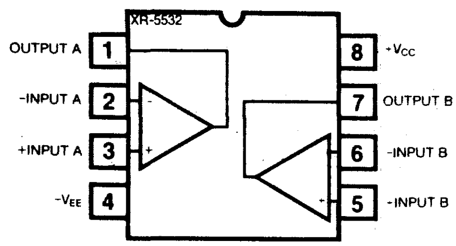
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-3503M	Ceramic	-55°C to +125°C
XR-3403CN	Ceramic	0°C to +70°C
XR-3403CP	Plastic	0°C to +70°C

XR-5532/5532A DUAL LOW-NOISE OPERATIONAL AMPLIFIER

The XR-5532 ultralow noise dual operational amplifier is especially designed for high quality audio and instrumentation applications. Compared to standard 741- or 301A-type op amps, these operational amplifiers offer an order of magnitude improvement in both noise performance and small signal bandwidth. Higher output drive capability and internal compensation are added features. The XR-5532A is specially screened for a guaranteed ultralow noise specification. This ultralow noise specification makes the XR-5532A ideally suited for audio preamplifier and other low level applications.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Pin for Pin Replacement MC1458, RC4558, TL072 TL082 & LF 353	
Direct Replacement for NE5532/NE5532A	
Ultralow Input Noise	4 nV/ Hz, Typical
Wide Small Signal Bandwidth	10 MHz, Typical
High Output Drive Capability	10V rms into 600Ω
Wide Supply Range	± 3V to ± 20V
Wide Power Bandwidth	200 kHz
High Slew Rate	6V/μsec

APPLICATIONS

Professional Audio Equipment
Instrumentation and Servo Control
Telephone Channel Amplifier
Low-Level Signal Processing
Audio Preamplification
Transducer Amplifiers

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-5532ACN	Ceramic	0°C to +70°C
XR-5532CN	Ceramic	0°C to +70°C
XR-5532ACP	Plastic	0°C to +70°C
XR-5532CP	Plastic	0°C to + 70°C

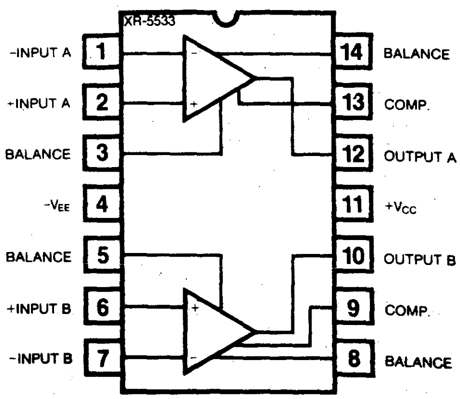
EXAR

Operational Amplifiers

XR-5533/5533A DUAL LOW-NOISE OPERATIONAL AMPLIFIER

The XR-5533 ultralow noise dual operational amplifier is especially designed for high quality audio and instrumentation applications. Compared to the standard 741- or 301A-type op amps, these operational amplifiers offer an order of magnitude improvement in noise performance, and small signal bandwidth, in addition to higher output drive capability. The XR-5533 is internally compensated for a voltage gain of three or more, and offers independent offset adjustments for each of the two op amps. The XR-5533A is specially screened for a guaranteed ultralow noise specification.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct Replacement for NE5533/NE5533A	
Dual Version of XR-5534 or NE5534	
Ultralow Input Noise	4 nV/ Hz, Typical
Wide Small Signal Bandwidth	10 MHz, Typical
High Output Drive Capability	10V rms into 600Ω
Wide Supply Range	± 3V to ± 20V
Wide Power Bandwidth	200 kHz
High Slew Rate	13V/μsec

APPLICATIONS

Professional Audio Equipment
Instrumentation and Servo Control
Telephone Channel Amplifier
Low-Level Signal Processing
Audio Preamplification

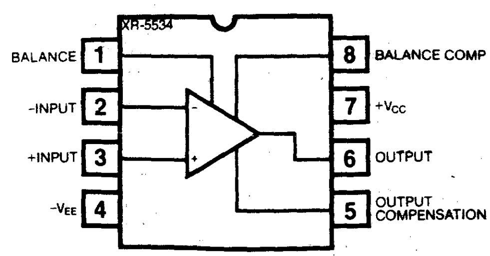
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-5533ACN	Ceramic	0°C to +70°C
XR-5533CN	Ceramic	0°C to +70°C
XR-5533ACP	Plastic	0°C to +70°C
XR-5533CP	Plastic	0°C to +70°C

XR-5534/5534A LOW-NOISE OPERATIONAL AMPLIFIER

The XR-5534 is a high performance, ultralow noise operational amplifier. Compared to the standard 741- or 301A-type op amps, it offers an order of magnitude improvement in noise performance, and small signal bandwidth, as well as significantly better output drive capability. The XR-5534 is ideally suited for applications in high quality and professional audio equipment, instrumentation, control circuits, and telephone channel amplifiers. The op amp is internally compensated for a gain of three or greater. The frequency response can be optimized with an external compensation capacitor for applications requiring unity-gain, low-overshoot response, or capacitive load driving. The XR-5534A is specially screened for a guaranteed ultralow noise specification.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct Replacement for NE5534/NE5534A	
Ultralow Input Noise	4 nV/$\sqrt{Hz}$, Typical
Wide Small Signal Bandwidth	10 MHz, Typical
High Output Drive Capability	10V rms into 600Ω
Wide Supply Range	± 3V to ± 20V
High-Voltage Gain	Av = 100,000 at dc
High Slew Rate	13V/μsec

APPLICATIONS

Professional Audio Equipment
Audio Preamplification

ORDERING INFORMATION

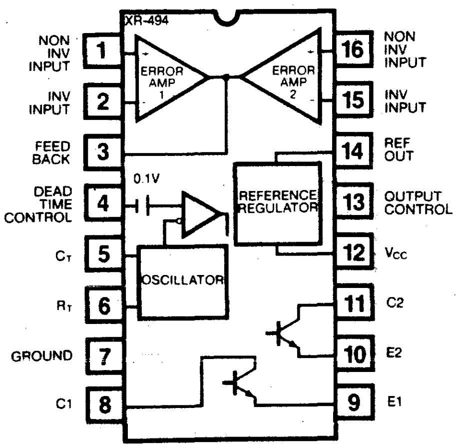
Part Number	Package	Operating Temperature
XR-5534AM	Ceramic	-55°C to +125°C
XR-5534M	Ceramic	-55°C to +125°C
XR-5534ACN	Ceramic	0°C to +70°C
XR-5534CN	Ceramic	0°C to +70°C
XR-5534ACP	Plastic	0°C to +70°C
XR-5534CP	Plastic	0°C to +70°C

Voltage Regulators

XR-494 PULSE-WIDTH MODULATING REGULATOR

All functions required to construct a pulse-width modulating regulator are incorporated on a single monolithic chip in the XR-494. The device is primarily designed for power supply control and contains an on-chip 5-volt regulator, two error amplifiers, an adjustable oscillator, a dead-time control comparator, a pulse-steering flip-flop, and output control circuits. Either common emitter or emitter follower output capability is provided by the uncommitted output transistors.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Complete PWM Power Control Circuitry
Uncommitted Outputs for 200 mA Sink or Source
Output Control Selects Single-ended
or Push-pull Operation
Internal Circuitry Prohibits Double Pulse at Either Output
Variable Dead-time Provides Control Over Total Range
Internal Regulator Provides a Stable 5V Reference Supply
Circuit Architecture Provides Easy Synchronization

APPLICATIONS

Pulse-Width Modulated Power Control Systems
Switching Regulators
Motor Speed Control
Power Inverters

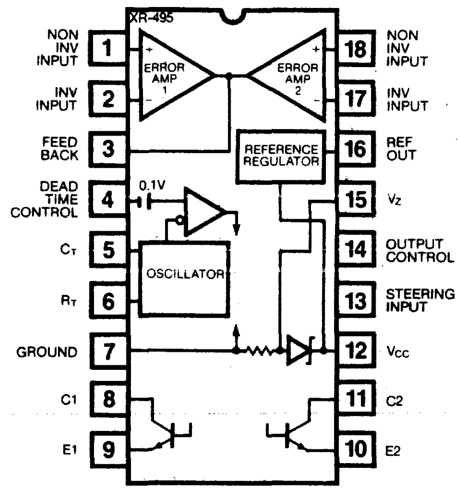
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-494M	Ceramic	-55°C to +125°C
XR-494CN	Ceramic	0°C to +70°C
XR-494CP	Plastic	0°C to +70°C

XR-495 PULSE-WIDTH MODULATING REGULATOR

All functions required to construct a pulse-width modulating regulator are incorporated on a single monolithic chip. The device is primarily designed for power supply control and contains an on-chip 5-volt regulator, two error amplifiers, an adjustable oscillator, a dead-time control comparator, a pulse-steering flip-flop, and output control circuits. Either common emitter or emitter follower output capability is provided by the uncommitted output transistors.
The XR-495 also contains an on-chip 39-volt Zener diode for high-voltage applications, where V_{CC} is greater than 40 volts, and an output steering control that overrides the internal control of the pulse-steering flip-flop.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Complete PWM Power Control Circuitry
Uncommitted Outputs for 200 mA Sink or Source
Output Control Selects Single-ended
or Push-pull Operation
Internal Circuitry Prohibits Double-Pulse at Either Output
Variable Dead-time Provides Control Over Total Range

APPLICATIONS

Pulse-Width Modulated Power Control Systems
Switching Regulators

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-495M	Ceramic	-55°C to +125°C
XR-495CN	Ceramic	0°C to +70°C
XR-495CP	Plastic	0°C to +70°C

EXAR

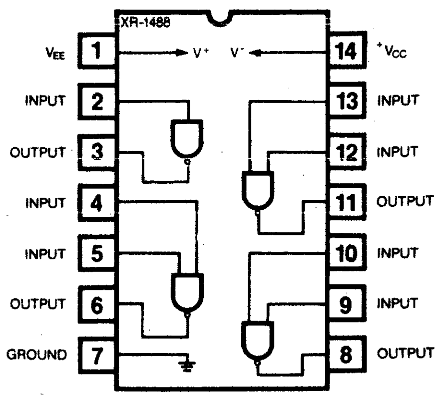
Line Interface Circuits

XR-1488 QUAD LINE DRIVER

The XR-1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment, in conformance with the specifications of EIA Standard No. RS232C. This extremely versatile integrated circuit can be used to perform a wide range of applications. The circuit features output current limiting circuitry, and independent positive and negative power supply driving elements. Compatibility with all DTL and TTL logic families enhances the versatility of the circuit.

The XR-1488 quad line driver along with its companion circuit, the XR-1489A quad line receiver, provides a complete interface system between DTL and TTL logic levels, and the RS232C defined voltage and impedance levels.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Current Limited Output
Independent Positive Power Supply Driving Elements
Independent Negative Power Supply Driving Elements
Compatible with DTL and TTL Logic Families
Data Terminal/Data Communication Interface
Conforms to EIA Standard No. RS232C

APPLICATIONS

RS232 C Interface

ORDERING INFORMATION

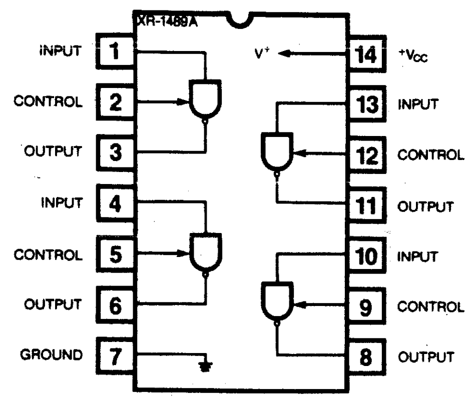
Part Number	Package	Operating Temperature
XR-1488N	Ceramic	0°C to +70°C
XR-1488P	Plastic	0°C to +70°C

XR-1489A QUAD LINE RECEIVER

The XR-1489A is a monolithic quad line receiver especially designed for data bus interface. Each of the line receiver sections has adjustable hysteresis characteristics for improved noise rejection. The input and output levels of the circuit are designed to provide direct interface between RS232C data bus standards and the DTL or TTL type logic levels.

The XR-1489A quad line receiver along with its companion circuit, the XR-1488 quad line driver, provides a complete interface between DTL and TTL logic levels, and the RS232C defined voltage and impedance levels.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct Replacement for MC1489A
Current Limited Output
Compatible with DTL and TTL Logic
Meets EIA Standard RS232C

APPLICATIONS

Data Bus Interface
Microprocessor Interface
Remote Terminal Interface
RS232 Interface

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1489AN	Ceramic	0°C to +70°C
XR-1489AP	Plastic	0°C to +70°C

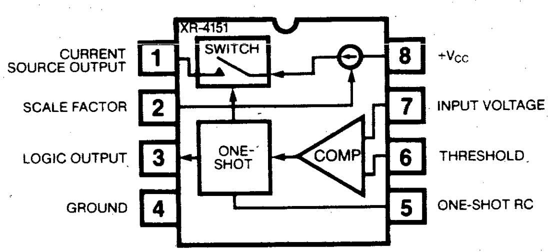
![EXAR]

Special Functions

XR-4151 VOLTAGE-TO-FREQUENCY CONVERTER

The XR-4151 is a device designed to provide a simple, low cost, method for converting a dc voltage into a proportional pulse repetition frequency. It is also capable of converting an input frequency into a proportional output voltage. The XR-4151 is useful in a wide range of applications, including A/D and D/A conversion and data transmission.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Single Supply Operation	+ 8V to + 22V
Pulse Output Compatible with all Logic Forms	
Programmable Scale Factor	
Linearity (Precision Mode)	± 0.05%, Typical
Temperature Stability	± 100 ppm/°C, Typical
High-Noise Rejection	
Inherent Monotonicity	
Easily Transmittable Output	
Simple Full Scale Trim	
Single-ended Input	
Frequency-to-Voltage Conversion	
Direct Replacement for RC/RV/RM4151	

APPLICATIONS

Voltage-to-Frequency Conversion
A/D and D/A Conversion
Data Transmission
Frequency-to-Voltage Conversion
Transducer Interface
System Isolation

ORDERING INFORMATION

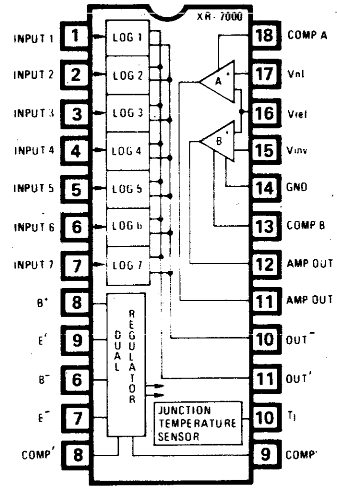
Part Number	Package	Operating Temperature
XR-4151P	Plastic	-40°C to +85°C
XR-4151CP	Plastic	0°C to +70°C

XR-7000 LOGARITHMIC AMPLIFIER

The XR-7000 provides an internal band-gap voltage reference, a differential video summing amplifier, and a precision die temperature sensor, to aid in its system interfacing. Also included is an internal power supply to provide excellent power supply rejection.
The XR-7000, available in a 24-Pin ceramic or plastic package, is designed to operate from dual 8-volt power supplies.

FUNCTIONAL BLOCK DIAGRAM

XR–7000 FUNCTIONAL BLOCK DIAGRAM



FEATURES

Seven Uncommitted Logging Elements Internal Band-Gap Voltage Reference Dual Tracking Regulator On-Board Precision Die Temperature Sensor

APPLICATIONS

Receiver Subsystems
Radar Subsystems
Spectrum Analyzers
Power Meters
Test Equipment
Video Cartridge Tape Recorders
Audio Tape Recorders
Smoke Detectors

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-7000M	Ceramic	-55°C to +125°C
XR-7000CP	Plastic	0°C to +70°C

Semi-Custom Development

SEMI-CUSTOM BIPOLAR PROGRAM

The Exar bipolar semi-custom design program offers a variety of semi-custom chips to fulfill various application performance requirements and complexities.

These semi-custom chips offer a unique method of manufacturing an almost unlimited variety of custom linear and digital integrated circuits, with greatly reduced cost and development time. Exar makes this possible by stocking wafers that are completely fabricated except for the final process step of device interconnection, which metalizes the selected components together in the required circuit configurations.

BIPOLAR SEMI-CUSTOM CHIPS

Chip Type	Chip Size in Mils	Breakdown Voltage	NPN	PNP	JFET's
A100	73 x 83	20V	60	18	
B100	85 x 85	20V	69	12	
C100A	56 x 62	20V	23	8	
D100	80 x 80	36V	50	16*	
E100	80 x 81	20V	48	15	
F100	91 x 110	20V	97	32*	
G100	90 x 90	20V	60	18*	
H100	82 x 92	20V	72	22*	
J100	61 x 65	20V	38	12*	
L100	86 x 105	20V	80	24	
M100	176 x 121	20V	149	52	
U100	**	36V	**	**	**
V100	130 x 100	36V	124	44	8
W100	130 x 160	36V	200	68	8
X100	115 x 95	75V	34	16	

*** Dual collector PNP transistors**
**** Contact Custom Product Application Engineering for more details.**

Exar offers a design kit which contains simple instructions and guidelines for designing the metal mask as well as the actual breadboard components (consisting of npn and pnp arrays and integrated resistors), which are representative of the devices available on the semi-custom chips. This provides the design engineer with the ability to closely evaluate his design's performance prior to integrating it on a monolithic chip.

SEMI-CUSTOM I^2L PROGRAM

With the introduction of the I^2L Gate Array chips, Exar has extended its semi-custom design program to the Integrated Injection Logic (I^2L) technology. This unique method of custom LSI development technique now makes it possible to manufacture an almost unlimited variety of digital or analog/digital circuits using I^2L technology, with greatly reduced development cost and time.

I^2L Semi-Custom Chips

Characteristics	CHIP SIZE XR-200	XR-300	XR-400	XR-500
Chip Size (mils)	98 x 119	104 x 146	119 x 156	122 x 185
I^2L Gates	192	288	256	520
Max. Operating Voltage	7V	7V	7V	7V
Bipolar I/O Interfaces	24	28	18	40
Bonding Pads	30	34	40	42

The XR-300 and XR-500 gate arrays are intended primarily for digital LSI designs. The XR-400 gate array features the advantage of combining analog and digital functions on the same IC chip. These I^2L gate array chips are customized by three custom mask patterns, which are simultaneously generated from a pencil layout, using Exar's unique computerized mask generation technique. In this manner, the chip layout is greatly simplified and gate utilization efficiency is increased.

Exar also offers an I^2L design kit which is intended to familiarize the designer with the basic features of I^2L technology, provides helpful design guidelines in reducing his design concept to breadboard and, finally, the IC layout stage.

TYPICAL FLOW FOR
SEMI-CUSTOM DEVELOPMENT

BREADBOARD
ANALYSIS

COMPUTER SIMULATION
FOR WORST CASE ANALYSIS
OR LOGIC SIMULATION

CHIP PENCIL LAYOUT

CUSTOMER DATA PACKAGE
SUBMITTAL

TECHNICAL FEASIBILITY
AND COST PROPOSAL

CUSTOMER/EXAR
INITIAL DESIGN REVIEW

MASK TAPING
OR DIGITIZING
FOR CUSTOM METALIZATION

MASK TOOLING

PROTOTYPE WAFER
FABRICATION

PROTOTYPE ASSEMBLY
AND EVALUATION

EXAR

Semi-Custom Development

SEMI-CUSTOM CMOS PROGRAMS

Metal Gate CMOS

Exar now offers two families of CMOS Gate Arrays. The first family consists of four chips featuring from 112 to 544 uncommitted logic gates, fabricated with 7.5μ metal gate technology.

CMOS Master-Chips

Chip Type	CMOS Gates	I/O Cells	Bonding Pads
XR-CMA	112	29	32
XR-CMB	162	34	38
XR-CMC	216	40	44
XR-CMD	544	46	53

A CMOS design kit is also available to familiarize the designer with the basic features of CMOS technology and to assist in the breadboarding layout of the IC chip.

Silicon Gate CMOS

The newest family of semi-custom Master-Chips to be added to Exar's product line is a series of four silicon gate arrays (4μ channel length drawn approximately 3μ actual) and range in size from 500 gates to 1600 gates. These devices feature dual layer metal and an extensive library of standard cells. Please contact Exar Custom Product Applications Engineering for more information.

ECONOMICS OF SEMI-CUSTOM

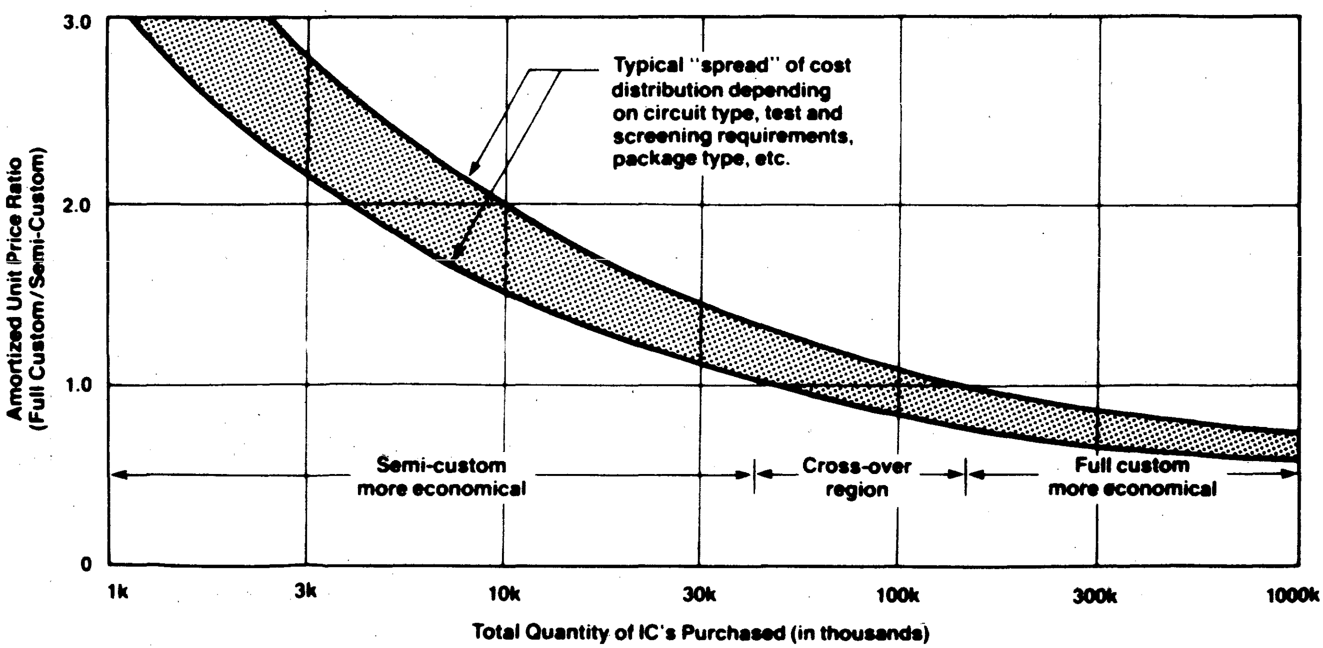
As the Amortized Unit Price Ratio graph in the figure below indicates, for production runs of 50,000 units or less, development costs are a significant influence, and a semi-custom program is clearly the best option. Over 150,000 pieces, production costs become the most important factor, and you are better off with a full custom chip.

Converting Semi-Custom To Full Custom

When production levels get closer to 150,000 units, converting from semi-custom to full custom is most cost effective. The conversion is simple and you get the lower production cost advantages of full custom without giving up the development benefits of semi-custom. In addition, the semi-custom prototypes often serve as a monolithic breadboard to optimize and debug the final design. The actual conversion is a relayout, rather than a redesign. The unused undedicated components are eliminated, and the circuit is laid out on a smaller chip.

Cost Savings Of Two-Step Conversion

Semi-custom design requires only 10-20% of the full custom development costs. Conversion from semi-custom to full custom costs about 50% of the total cost of full custom development. Therefore, the total development costs of the two-step conversion are only 60-70% of a complete full custom program.



Processing sparks improvement of semicustom linear chips

A number of modern semiconductor processing techniques previously not used for semicustom linear ICs were implemented in the XR-W100 and XR-V100 Master Chips.

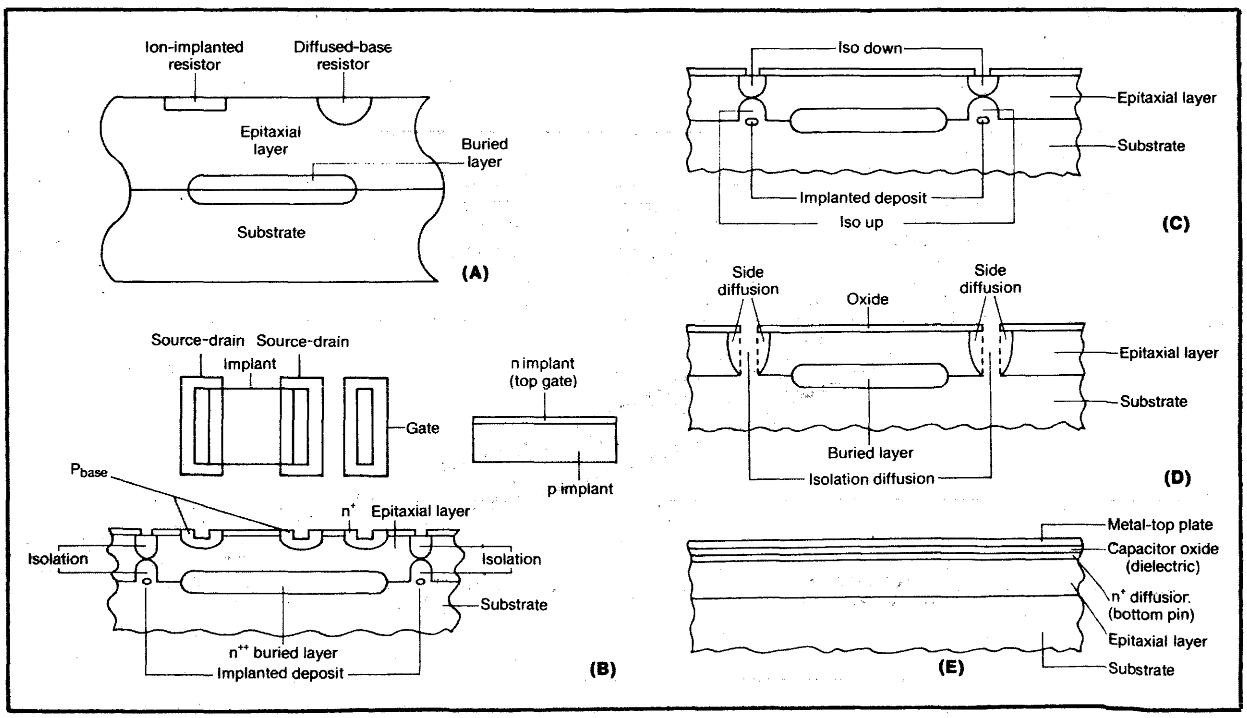
Ion implantation. Ion implantation ballistically introduces dopant ions into the surface of a semiconductor material. Because a machine similar to a linear accelerator shoots the dopant into the surface, their penetration and concentration can be precisely controlled by varying the particle-beam dosage and energy. This technology produces having very high sheet resistivity; thus high-value resistors can fit into much smaller areas on the chip than previously. In addition, ion-implanted resistors have about 300% better absolute-value tolerance and matching than their diffused coun terparts, which depend on the diffusion of dopants into the semiconductor surface (Fig. A).

With ion implantation, p-channel JFETs can be built on the same semiconductor surface as standard bipolar components. JFETs are basically implanted resistors with a second n-implant on top of the channel region that serves as a gate (Fig. B). They are useful in high-input-impedance amplifiers, automatic gaincontrol circuits, current sources, analog switches, multiplexers, and similar applications.

Double isolation. Double isolation, also called "iso-up," employs a rich ion-implanted p-type deposit in the substrate prior to growing the epitaxial layer. With conventional top-bottom diffusion, the bottom deposit diffuses downward. If everything is aligned correctly, the two deposits meet in the middle (Fig. C), leading not only to substantial reductions in lateral diffusions, but also to a smaller die.

Contrasting with that iso-up process is the traditional single isolation, which depends on a rich p-type diffusion penetrating through the epitaxial layer and into the substrate, thereby isolating regions of the epitaxial layer (Fig. D). This method does have its disadvantages, though. For one, it requires a long, high-temperature diffusion cycle. More critical to the user, however are the wider spacing needed between the isolation and subsequent diffusions to permit the significant lateral diffusion of the isolation. That extra spacing accumulates across the die, consuming a large amount of silicon. With the cost of manufacturing the die related largely to its area, the wasted space is reflected in a higher selling price to the user.

Oxide capacitance. By adding a special oxidation step to the processing, oxide capacitors are easily placed on a semicustom IC (Fig. E). These com-



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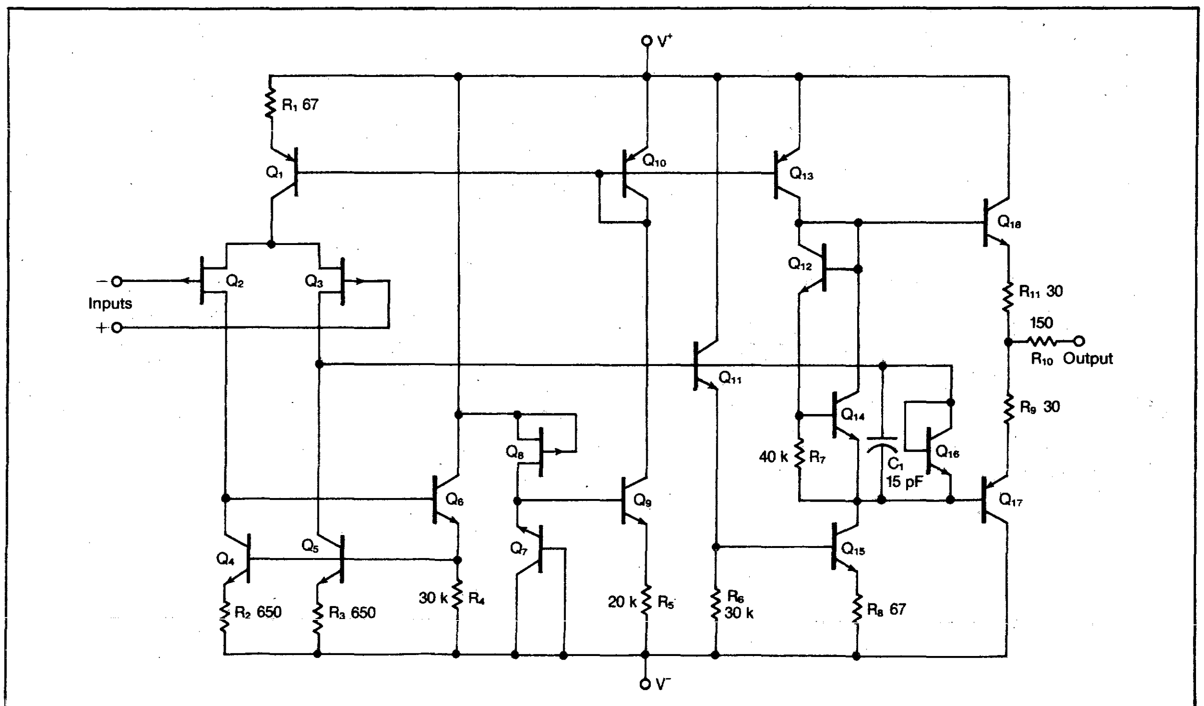
ponents are identical in constuction to those that internally compensate standard op amps; but unlike junction capacitors, they are not voltage-dependent.

36-V process. In the past, high-density semicustom linear ICs were offered only with 20-V processing. Users needing 24V or the standard ±15-V op-amp supply were forced to externally regulate down to a voltage compatible with the chip or to place all high-voltage components off chip. Both cases severely limited higher levels of system integration. With the new 36-V process, these limitations become a thing of the past.

Nitride passivation. Applied over the standard purposes: it helps to eliminate ionic contamination from the chip surface, and it seals the active chip area from moisture. Both functions are aimed at reducing failure rates and improving the chip's overall reliability. Furthermore, with nitride passivation, a user can employ a plastic package in applications that might otherwise require a more expensive, hermetically sealed ceramic housing.

IC components. Though many characteristics of integrated components are similar to those of their discrete counterparts, there are important differences. Discrete components are individually produced and connected into circuits as required. Each component is manufactured by the most suitable process, thus optimizing performance. In the microscopic setting of integrated circuitry, such luxuries do not exist. Because the components are produced simultaneously, compromises must be made on performance. Despite these limitations, integrated components have unique advantages that allow them to overcome most design problems.

Master Chip System typical building block cell



A typical building-block cell in the Master Chip system, this JFET operational amplifier is similar to one of Exar's standard discrete op amps. This type of high-performance device relieves designers of the difficult task of creating their own amplifiers to satisfy each new application.

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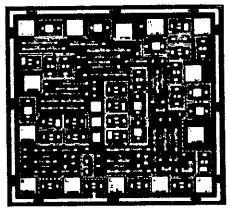
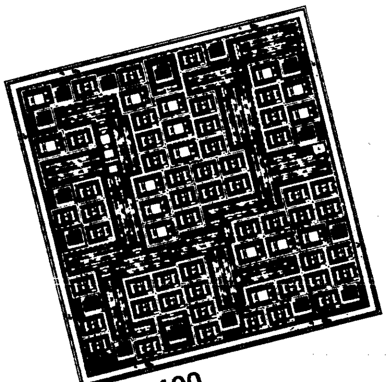
EXAR

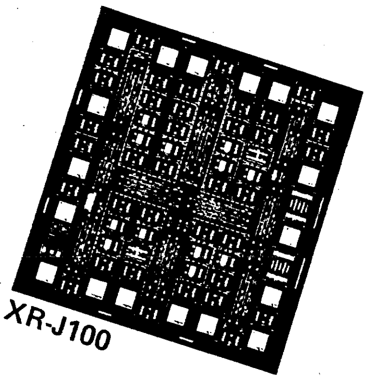
Semi-Custom Arrays



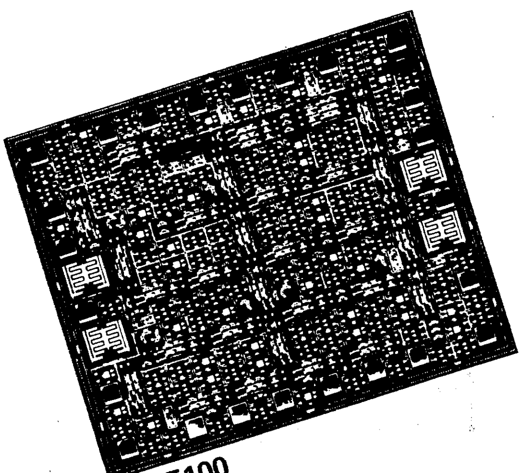
XR-C100A



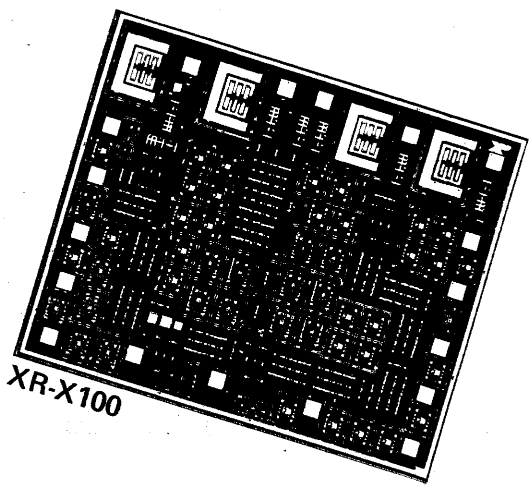
XR-D100



XR-J100



XR-F100



XR-X100

LINEAR

Exar Integrated Systems

HARRIS

HA-1608

+10V Adjustable Voltage Reference

FEATURES

- MONOLITHIC CONSTRUCTION
- INITIAL ACCURACY +10V ± 0.010V
- OUTPUT VOLTAGE ERROR, TOTAL ±1/4 LSB
- LOW NOISE $20\mu V_{p-p}$
- WIDE INPUT RANGE 12V TO 30V
- LOW POWER DISSIPATION 30mW
- OUTPUT SHORT CIRCUIT PROTECTION
- ADJUSTABLE OUTPUT

APPLICATIONS

- AN ECONOMICAL EXTERNAL REFERENCE FOR: HI-5608; DAC 08; AD1408; AD559
- VOLTAGE REGULATOR REFERENCE
- PORTABLE BATTERY OPERATED EQUIPMENT
- NEGATIVE 10V REFERENCE

DESCRIPTION

HA-1608 is a monolithic +10V adjustable voltage reference featuring accuracy and temperature stability specifications detailed exclusively for 8 bit data conversion systems. A stable +10V output is provided by a reference zener and buffer amplifier coupled with laser trimmed feedback and zener bias resistors. Long term stability is ensured through integration of all reference components into a monolithic design. Flexibility of HA-1608 is provided through an external trim control which allows the user to adjust the output voltage for binary or BCD applications without affecting overall performance.

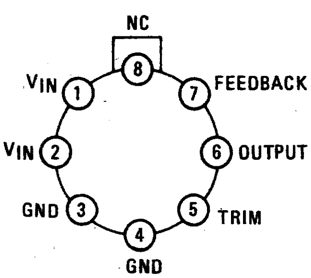
These devices provide a total output voltage error of ± 1/4 LSB for 8 bit D/A or A/D converters. Low standby power (0.3mW) makes HA-1608 a natural selection for portable battery operated equipment, comparator references, and reference stacking circuits. These devices can also be used on -10V references.

HA-1608 is packaged in 8 pin metal cans (TO-99) and the pinout is arranged for convenient replacement of other less accurate regulators in applications demanding minimal change with temperature and time. HA-1608-2 is specified for -55°C to +125°C operation while the HA-1608-5 operates from 0°C to +75°C.

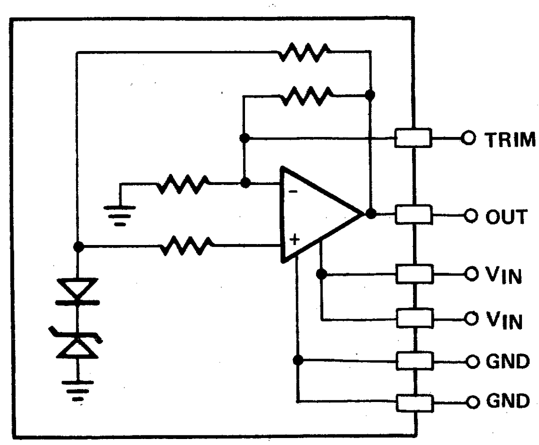
PINOUT

Section 11 for Packaging

TOP VIEW



FUNCTIONAL SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage	40V	Operating Temperature Range	
Output Short Circuit Duration	Indefinitely	HA-1608-2	-55°C to +125°C
Power Dissipation	500mW	HA-1608-5	0°C to +75°C
Storage Temperature Range	-65°C to +150°C		

ELECTRICAL CHARACTERISTICS (Note 2) (V_{IN} = +15V, I_L = 0mA, unless otherwise specified)

PARAMETER	TEMP	HA-1608-2 -55°C to +125°C MIN	TYP	MAX	HA-1608-5 0°C to +75°C MIN	TYP	MAX	UNITS
POWER INPUT CHARACTERISTICS								
Input Voltage Range, V_{IN}	Full	12	15	30	12	15	30	V
Quiescent Current, I_Q	25°C		1.9			1.9		mA
	Full			3.0			3.0	
REGULATED OUTPUT CHARA.'S								
Output Voltage, V_O	25°C	9.990	10.00	10.010	9.990	10.00	10.010	V
Output Load Current, I_L	Full	10	20		10	20		mA
Line Regulation (V_{IN} = 12V to 30V)	25°C		0.006			0.006		%/V
	Full			0.015			0.015	
Load Regulation (I_L = Open to 10mA)	25°C		0.006			0.006		%/mA
	Full			0.015			0.015	
Output Voltage Error Total I_L = 0mA (Relative to 8-bit accuracy, see Definition #3)	Full			±1/4 LSB			±1/4 LSB	
Output Noise Voltage, EN 0.1Hz to 10Hz	Full		35			35		μV_{p-p}
Dynamic Load Settling Time to ±0.1%	25°C		2.5			2.5		μs
to ±0.01%	25°C		5			5		
Warm-up Time (to ± 0.01%)	25°C		1			1		sec
	Full		3			3		

NOTES:
1. Absolute maximum ratings are limiting values beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. The specified electrical characteristics apply to suggested hook-up only.

HA-2400/2404/2405

PRAM Four Channel Programmable Amplifier

FEATURES

- PROGRAMMABILITY
- HIGH SLEW RATE 30V/μs
- WIDE GAIN BANDWIDTH 40MHz
- HIGH GAIN 150,000
- LOW OFFSET CURRENT 5nA
- HIGH INPUT IMPEDANCE 30MΩ
- SINGLE CAPACITOR COMPENSATION
- DTL/TTL COMPATIBLE INPUTS

APPLICATIONS

- THOUSANDS OF NEW APPLICATIONS; PROGRAM
  - SIGNAL SELECTION/MULTIPLEXING
  - OP AMP GAIN
  - OSCILLATOR FREQUENCY
  - FILTER CHARACTERISTICS
  - ADD-SUBTRACT FUNCTIONS
  - INTEGRATOR CHARACTERISTICS
  - COMPARATOR LEVELS

DESCRIPTION

HA-2400/2404/2405 comprise a series of four-channel programmable amplifiers providing a level of versatility unsurpassed by any other monolithic operational amplifier. Versatility is achieved by employing four input amplifier channels, any one (or none) of which may be electronically selected and connected to a single output stage through DTL/TTL compatible address inputs. The device formed by the output and the selected pair of inputs is an op amp which delivers excellent slew rate, gain bandwidth and power bandwidth performance. Other advantageous features for these dielectrically isolated amplifiers include high voltage gain and input impedance coupled with low input offset voltage and offset current. External compensation is not required on this device at closed loop gains greater than 10.

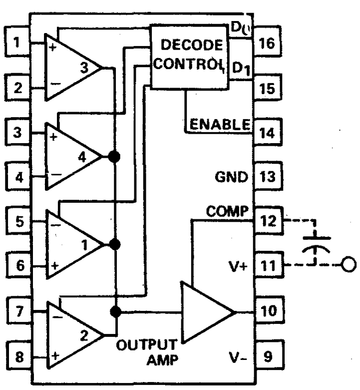
Each channel of the HA-2400/2404/2405 can be controlled and operated with suitable feedback networks in any of the standard op amp configurations. This specialization makes these amplifiers excellent components for multiplexing, signal selection, and mathematical function designs. With 30V/μs slew rate, 40MHz gain bandwidth, and 30M ohms input impedance these devices are ideal building blocks for signal generators, active filters, and data acquisition designs. Programmability coupled with 2mV typical offset voltage and 5nA offset current makes these amplifiers outstanding components for signal conditioning circuits.

HA-2400/2404/2405 are available in a 16 pin dual-in-line package. HA-2400 is specified from -55°C to +125°C. HA-2404 is specified over the -25°C to +85°C range, while HA-2405 operates from 0°C to +75°C.

PINOUT

TOP VIEW

Section 11 for Packaging



TRUTH TABLE

D_1	D_0	EN	SELECTED CHANNEL
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4
X	X	L	NONE

SCHEMATIC

Condensed circuit diagram for a programmable amplifier (PRAM HA-2400)

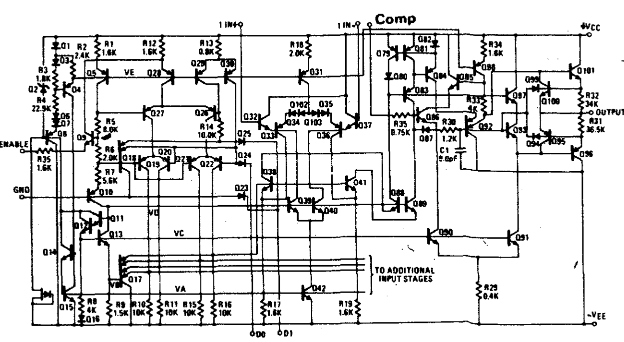


Diagram includes: ONE INPUT STAGE, DECODE CONTROL, BIAS NETWORK AND OUTPUT STAGE

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V− Terminals 45.0V

Differential Input Voltage $\pm V_{Supply}$

Digital Input Voltage −0.76V to +10.0V

Output Current Short Circuit Protected ($I_{SC} \leq \pm 33mA$)

Internal Power Dissipation (Note 13) 300mW

Operating Temperature Range $-55^oC \leq T_A \leq +125^oC$ (HA-2400)
$-25^oC \leq T_A \leq +85^oC$ (HA-2404)
$0^oC \leq T_A \leq +75^oC$ (HA-2405)

Storage Temperature Range $-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{Supply} = \pm 15.0V$ unless otherwise specified.

Digital inputs: $V_{IL} = +0.5V$, $V_{IH} = +2.4V$
Limits apply to each of the four channels, when addressed.

PARAMETER	TEMP.	HA-2400/HA-2404 LIMITS MIN.	TYP.	MAX.	HA-2405 LIMITS MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		4	9		4	9	mV
	Full			11			11	mV
Bias Current (Note 12)	+25°C		50	200		50	250	nA
	Full			400			500	nA
Offset Current (Note 12)	+25°C		5	50		5	50	nA
	Full			100			100	nA
Input Resistance (Note 12)	+25°C		30			30		MΩ
Common Mode Range	Full	±9.0			±9.0			V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 1,5)	+25°C	50K	150K		50K	150K		V/V
	Full	25K			25K			V/V
Common Mode Rejection Ratio (Note 2)	Full	80	100		74	100		dB
Gain Bandwidth (Note 3)	+25°C	20	40		20	40		MHz
(Note 4)	+25°C	4	8		4	8		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		V
Output Current	+25°C	10	20		10	20		mA
Full Power Bandwidth (Notes 3, 5)	+25°C	200	500		200	500		kHz
(Notes 4,5)	+25°C	100	200		100	200		kHz
TRANSIENT RESPONSE								
Rise Time (Notes 4,6)	+25°C		20	45		20	50	ns
Overshoot (Notes 4,6)	+25°C		25	40		25	40	%
Slew Rate (Notes 3,7)	+25°C	20	30		20	30		V/µs
(Notes 4,7)	+25°C	6	8		6	8		V/µs
Settling Time (Notes 4, 7, 8)	+25°C		1.5	2.5		1.5	2.5	µs
CHANNEL SELECT CHARACTERISTICS								
Digital Input Current (V_{IN} = 0V)	Full		1	1.5		1	1.5	mA
Digital Input Current (V_{IN} = +5.0V)	Full		5			5		nA
Output Delay (Note 9)	+25°C		100	250		100	250	ns
Crosstalk (Note 10)	+25°C	-80	-110		-74	-110		dB
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		4.8	6.0		4.8	6.0	mA
Power Supply Rejection Ratio (Note 11)	Full	74	90		74	90		dB

NOTES:
1. $R_L = 2K\Omega$
2. $V_{CM} = \pm 5V$.D.C.
3. $A_V = +10$, $C_{COMP} = 0$, $R_L = 2K\Omega$, $C_L = 50pF$
4. $A_V = +1$, $C_{COMP} = 15pF$, $R_L = 2K\Omega$, $C_L = 50pF$
5. V_{OUT} = 20V peak-to-peak
6. V_{OUT} = 200mV peak-to-peak
7. V_{OUT} = 10.0V peak-to-peak
8. To 0.1% of final value
9. To 10% of final value; output then slews at normal rate to final value.
10. Unselected input to output; $V_{IN} = \pm 10$ V.D.C.
11. $V_{SUPP} = \pm 10$V.D.C. to ± 20V.D.C.
12. Unselected channels have approximately the same input parameters.
13. Derate by 4.3mW/°C above 105°C

HARRIS

HA-2500/02/05

Precision High Slew Rate Operational Amplifiers

FEATURES

- HIGH SLEW RATE 30V/μS
- FAST SETTLING 330ns
- WIDE POWER BANDWIDTH 500kHz
- HIGH GAIN BANDWIDTH 12MHz
- HIGH INPUT IMPEDANCE 50 MΩ
- LOW OFFSET CURRENT 10nA
- INTERNALLY COMPENSATED

APPLICATIONS

- DATA ACQUISTION SYSTEMS
- R.F. AMPLIFIERS
- VIDEO AMPLIFIERS
- SIGNAL GENERATORS
- PULSE AMPLIFICATION

DESCRIPTION

HA-2500/2502/2505 comprise a series of monolithic operational amplifiers whose designs are optimized to deliver excellent slew rate, bandwidth, and settling time specifications. The outstanding dynamic features of this internally compensated device are complemented with low offset voltage and offset current.

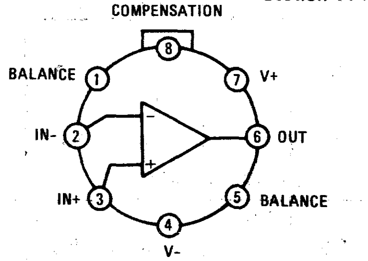
These dielectrically isolated amplifiers are ideally suited for applications such as data acquisition, R.F., video, and pulse conditioning circuits. Slew rate of ±25V/μs and 330ns (0.1%) settling time make these devices excellent components in fast, accurate data acquisition and pulse amplification designs. 12 MHz bandwidth and 500kHz power bandwidth make these devices well suited to R.F. and video applications. With 2mV typical offset voltage plus offset trim capability and 10nA offset current, HA-2500/2502/2505 are particularly useful components in signal conditioning designs.

The gain and offset voltage figures of the HA-2500 series are optimized by internal component value changes while the similar design of the HA-2510 series is maximized for slew rate.

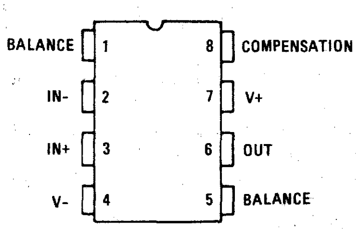
HA-2500/2502/2505 are available in metal can (TO-99) packages. HA-2500 and HA-2502 are specified over the -55°C to +125°C range. HA-2505 is specified from 0°C to +75°C.

PINOUT

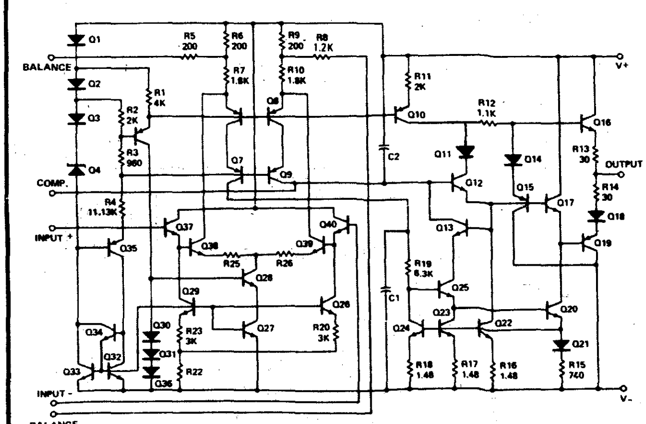
Section 11 for Packaging



TOP VIEWS



SCHEMATIC



LINEAR

Harris Semiconductor

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V	Operating Temperature Range –	HA-2500/HA-2502	$-55^oC \leq T_A \leq +125^oC$
Differential Input Voltage	±15.0V		HA-2505	$0^oC \leq T_A \leq +75^oC$
Peak Output Current	50mA	Storage Temperature Range		$-65^oC \leq T_A \leq +150^oC$
Internal Power Dissipation	300mW			

ELECTRICAL CHARACTERISTICS

V+ = +15V D.C., V- = -15V D.C.

PARAMETER	TEMP.	HA-2500 -55°C to +125°C LIMITS MIN.	TYP.	MAX.	HA-2502 -55°C to +125°C LIMITS MIN.	TYP.	MAX.	HA-2505 0°C to +75°C LIMITS MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		2	5		4	8		4	8	mV
	Full			8			10			10	mV
Offset Voltage Average Drift	Full		20			20			20		μV/°C
Bias Current	+25°C		100	200		125	250		125	250	nA
	Full			400			500			500	nA
Offset Current	+25°C		10	25		20	50		20	50	nA
	Full			50			100			100	nA
Input Resistance (Note 10)	+25°C	25	50		20	50		20	50		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 1,4)	+25°C	20K	30K		15K	25K		15K	25K		V/V
	Full	15K			10K			10K			V/V
Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4)	+25°C	350	500		300	500		300	500		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	50		25	50	%
Slew Rate (Notes 1,5,8 & 12)	+25°C	±25	±30		±20	±30		±20	±30		V/μs
Settling Time to 0.1% (Notes 1,5,8 & 12)	+25°C		0.33			0.33			0.33		μs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		4	6		4	6		4	6	mA
Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

NOTES:
1. $R_L = 2K$
2. $V_{CM} = \pm 10V$
3. $A_V > 10$
4. $V_O = \pm 10.0V$
5. $C_L = 50pF$
6. $V_O = \pm 200mV$
7. $V_O \pm 200mV$
8. See transient response test circuits and waveforms page four.
9. $\Delta V = \pm 5.0V$
10. This parameter value is based on design calculations.
11. Full power bandwidth guaranteed based on slew rate measurement using $FPBW = S.R./2\pi V_{peak}$.
12. $V_{OUT} = \pm 5V$

HA-2510/2512/2515

High Slew Rate Operational Amplifiers

FEATURES

- HIGH SLEW RATE 60V/μs
- FAST SETTLING 250ns
- WIDE POWER BANDWIDTH 1,000kHz
- HIGH GAIN BANDWIDTH 12MHz
- HIGH INPUT IMPEDANCE 100MΩ
- LOW OFFSET CURRENT 10nA
- INTERNALLY COMPENSATED

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- R.F. AMPLIFIERS
- VIDEO AMPLIFIERS
- SIGNAL GENERATORS
- PULSE AMPLIFICATION

DESCRIPTION

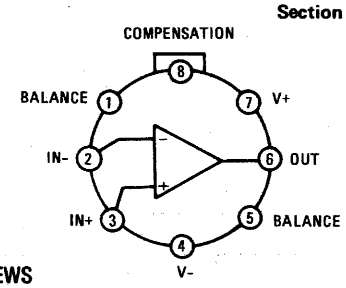
The HA-2510/2512/2515 are a series of high performance operational amplifiers which set the standards for maximum slew rate, highest accuracy and widest bandwidth for internally compensated monolithic devices. In addition to excellent dynamic characteristics, these dielectrically isolated amplifiers also offer low offset current and high input impedance.

The ±60V/ μs slew rate and 250ns (0.1%) settling time of these amplifiers is ideally suited for high speed D/A, A/D, and pulse amplification designs. HA-2510/2512/2515's superior 12MHz gain bandwidth and 1000kHz power bandwidth is extremely useful in R.F. and video applications. For accurate signal conditioning these amplifiers also provide 10nA offset current, coupled with 100MΩ input impedance, and offset trim capability.

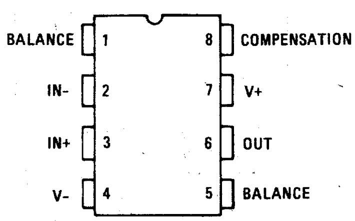
The HA-2510/2512 are available in metal can (TO-99) and 14-pin flat packages. HA-2510 and HA-2512 are specified from -55°C to +125°C. HA-2515 is specified over the 0°C to +75°C range, and is available in the TO-99 package.

PINOUT

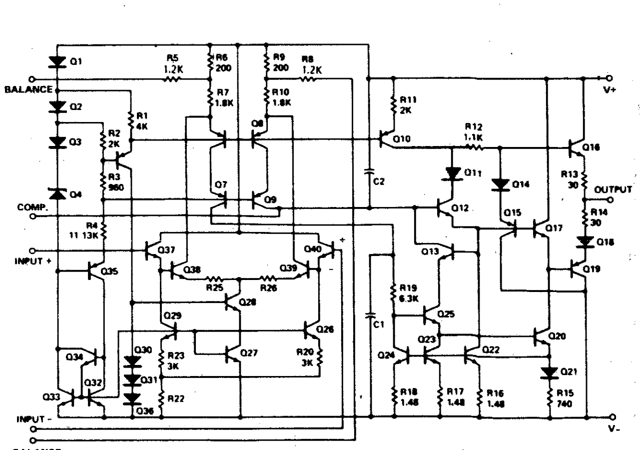
Section 11 for Packaging



TOP VIEWS



SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V	Peak Output Current	50mA
Differential Input Voltage	±15.0V	Internal Power Dissipation	300mW
Operating Temperature Range		Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$
HA-2510/HA-2512	$-55^oC \leq T_A \leq +125^oC$		
HA-2515	$0^oC \leq T_A \leq +75^oC$		

ELECTRICAL CHARACTERISTICS

V+ = +15V D.C., V– = 15V D.C.

PARAMETER	TEMP.	HA-2510 -55°C to +125°C LIMITS MIN.	TYP.	MAX.	HA-2512 -55°C to +125°C LIMITS MIN.	TYP.	MAX.	HA-2515 0°C to +75°C LIMITS MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C Full		4	8 11		5	10 14		5	10 14	mV mV
Offset Voltage Average Drift	Full		20			25			30		μV/°C
Bias Current	+25°C Full		100	200 400		125	250 500		125	250 500	nA nA
Offset Current	+25°C Full		10	25 50		20	50 100		20	50 100	nA nA
Input Resistance (Note 10)	+25°C	50	100		40	100		40	100		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 1,4)	+25°C Full	10K 7.5K	15K		7.5K 5K	15K		7.5K 5K	15K		V/V V/V
Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4, 11)	+25°C	750	1000		600	1000		600	1000		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	50		25	50	%
Slew Rate (Notes 1, 5, 8 & 12)	+25°C	±50	±65		±40	±60		±40	±60		V/μs
Settling Time (Notes 1, 5, 8 & 12)	+25°C		0.25			0.25			0.25		μs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		4	6		4	6		4	6	mA
Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

NOTES:
1. $R_L = 2K$
2. $V_{CM} = \pm 10V$
3. $A_V > 10$
4. $V_O = \pm 10.0V$
5. $C_L = 50pF$
6. $V_O = \pm 200mV$
7. $V_O = \pm 200mV$
8. See transient response test circuits and waveforms
9. $\Delta V = \pm 5.0V$
10. This parameter value is based upon design calculations.
11. Full power bandwidth guaranteed based upon slew rate measurement $FPBW = S.R./2\pi V_{peak}$.
12. $V_{OUT} = \pm 5V$

LINEAR

Harris Semiconductor

HARRIS

HA-2520/22/25

Uncompensated High Slew Rate Operational Amplifiers

FEATURES

- HIGH SLEW RATE 120V/μs
- FAST SETTLING 200ns
- WIDE POWER BANDWIDTH 2,000kHz
- HIGH GAIN BANDWIDTH 20MHz
- HIGH INPUT IMPEDANCE 100MΩ
- LOW OFFSET CURRENT 10nA

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- R.F. AMPLIFIERS
- VIDEO AMPLIFIERS
- SIGNAL GENERATORS
- PULSE AMPLIFICATION

DESCRIPTION

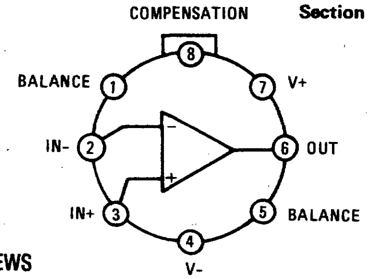
HA-2520/2522/2525 comprise a series of monolithic operational amplifiers delivering an unsurpassed combination of specifications for slew rate, bandwidth and settling time. These dielectrically isolated amplifiers are controlled at closed loop gains greater than 3 without external compensation. In additon, these high performance components also provide low offset current and high input impedance.

120V/μs slew rate and 200ns (0.1%) settling time of these amplifiers make them ideal components for pulse amplification and data acquisition designs. These devices are valuable components for R.F. and video circuitry requiring up to 20MHz gain bandwidth and 2MHz power bandwidth. For accurate signal conditioning designs the HA-2520/2522/2525's superior dynamic specifications are complimented by 10nA offset current, 100MΩ input impedance and offset trim capability.

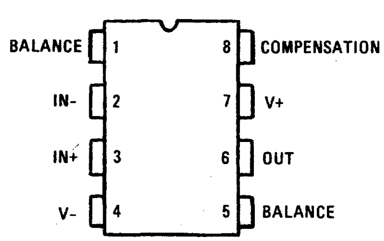
The HA-2520/2522 are available in metal can (TO-99) and 14-pin flat packages. HA-2520 and HA-2522 are specified over -55°C to +125°C range. HA-2525 is specified from 0°C to +75°C, and is available in the TO-99 package.

PINOUT

Section 11 for Packaging



TOP VIEWS



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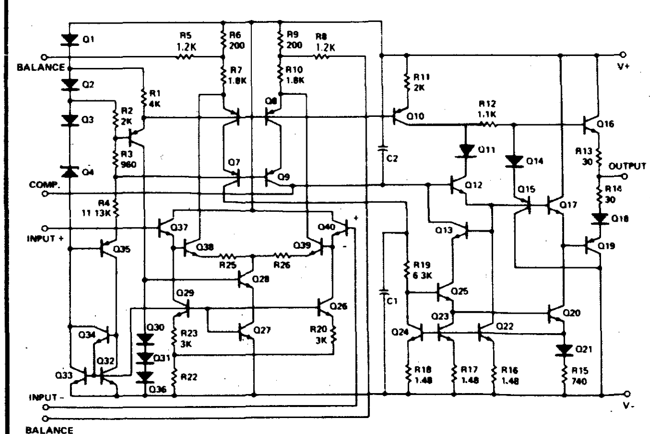


ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V	Peak Output Current	50mA
Differential Input Voltage	±15.0V	Internal Power Dissipation	300mW
Operating Temperature Range			
HA-2520/2522	$-55^oC \leq T_A \leq +125^oC$	Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$
HA-2525	$0^oC \leq T_A \leq +75^oC$		

ELECTRICAL CHARACTERISTICS

V+ = +15V D.C., V- = -15V D.C.

PARAMETER	TEMP.	HA-2520 -55°C to +125°C LIMITS MIN.	TYP.	MAX.	HA-2522 -55°C to +125°C LIMITS MIN.	TYP.	MAX.	HA-2525 0°C to +75°C LIMITS MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		4	8		5	10		5	10	mV
	Full			11			14			14	mV
Offset Voltage Average Drift	Full		20			25			30		μV/°C
Bias Current	+25°C		100	200		125	250		125	250	nA
	Full			400			500			500	nA
Offset Current	+25°C		10	25		20	50		20	50	nA
	Full			50			100			100	nA
Input Resistance (Note 9)	+25°C	50	100		40	100		40	100		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 1,4)	+25°C	10K	15K		7.5K	15K		7.5K	15K		V/V
	Full	7.5K			5K			5K			V/V
Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C	10	20		10	20		10	20		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4, 10)	+25°C	1500	2000		1200	1600		1200	1600		kHz
TRANSIENT RESPONSE ($A_V = +3$)											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 6 & 8)	+25°C		25	40		25	50		25	50	%
Slew Rate (Notes 1, 5, 8 & 11)	+25°C	±100	±120		±80	±120		±80	±120		V/μs
Settling Time (Notes 1, 5, 8 & 11)	+25°C		0.20			0.20			0.20		μs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		4	6		4	6		4	6	mA
Power Supply Rejection Ratio (Note 7)	Full	80	90		74	90		74	90		dB

NOTES:
1. $R_L = 2K$
2. $V_{CM} = \pm 10V$
3. $A_V > 10$
4. $V_O = \pm 10.0V$
5. $C_L = 50pF$
6. $V_O = \pm 200mV$
7. $\Delta V = \pm 5.0V$
8. See transient response test circuits and waveforms
9. This parameter value is based upon design calculations.
10. Full power bandwidth guaranteed based upon slew rate measurement $FPBW = S.R./2\pi V_{peak}$.
11. $V_{OUT} = \pm 5V$

HARRIS

HA-2539

Very High Slew Rate Wideband Operational Amplifiers

FEATURES

- VERY HIGH SLEW RATE 600V/μs
- OPEN LOOP GAIN 30kV/V
- WIDE GAIN-BANDWIDTH 600MHz
- POWER BANDWIDTH 9.5MHz
- LOW OFFSET VOLTAGE 3mV
- INPUT VOLTAGE NOISE 15nV/$\sqrt{Hz}$
- OUTPUT VOLTAGE SWING $\pm$10V

APPLICATIONS

- PULSE AND VIDEO AMPLIFIERS
- WIDEBAND AMPLIFIERS
- HIGH SPEED SAMPLE-HOLD CIRCUITS
- RF OSCILLATORS

GENERAL DESCRIPTION

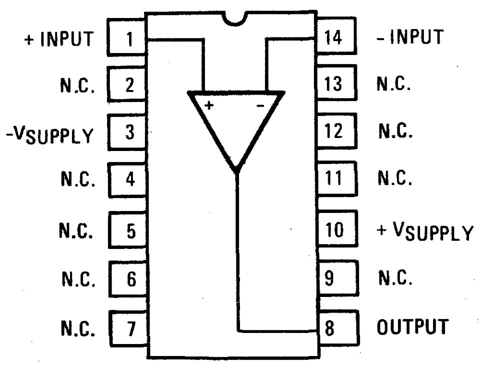
The Harris HA-2539 represents the ultimate in high slew rate wideband, monolithic, operational amplifiers. It has been designed and constructed with the Harris high frequency BIPDIP (Bipolar dielectric isolation process), and features dynamic parameters never before available from a truly differential device.

With a 600V/ μs slew rate and a 600MHz gain-bandwidth-product, the HA-2539 is ideally suited for use in video and RF amplifier designs. Full $\pm$ 10V output swing coupled with outstanding A.C. parameters and complemented by high open loop gain makes these devices useful in high speed data acquisition systems.

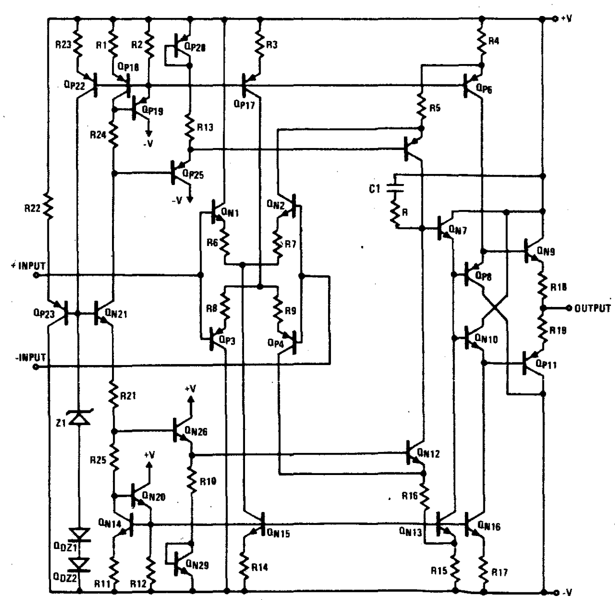
The HA-2539 is available in the 14 pin CERDIP. The HA-2539-2 denotes -55°C to +125°C operation while the HA-2539-5 operates over the 0°C to +75°C range.

PINOUT

TOP VIEW



SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage between V+ and V- Terminals	35V
Differential Input Voltage	6V
Output Current	50mA (Peak)
Internal Power Dissipation (Note 2)	870mW (Cerdip)
Operating Temperature Range: (HA-2539-2)	$-55^oC \leq T_A \leq +125^oC$
(HA-2539-5)	$0^oC \leq T_A \leq +75^oC$
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS $V_{SUPPLY} = \pm 15$ Volts; R_L = 1K ohms, unless otherwise specified.

		HA-2539-2 -55°C to +125°C			HA-2539-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		3	5		3	15	mV
	FULL			10			20	mV
Average Offset Voltage Drift	FULL		20			20		μV/°C
Bias Current	+25°C		5	20		5	20	μA
	FULL			25			25	μA
Offset Current	+25°C		1	6		1	6	μA
	FULL			8			8	μA
Input Resistance	+25°C		10			10		Kohms
Input Capacitance	+25°C		1.0			1.0		pF
Common Mode Range	FULL	±10			±10			V
Input Voltage Noise (f = 1kHz, $R_g = 0\Omega$)	+25°C		15			15		$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	15K	30K		10K	30K		V/V
	FULL	5K			5K			V/V
Common-Mode Rejection Ratio (Note 4)	FULL	60			60			dB
Gain-Bandwidth-Product (Notes 5 & 6)	+25°C		600			600		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 3)	FULL	±10			±10			V
Output Current (Note 3)	+25°C	10			10			mA
Output Resistance	+25°C		30			30		Ohms
Full Power Bandwidth (Note 3 & 7)	+25°C	8.7	9.5		8.7	9.5		MHz
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C		7			7		ns
Overshoot	+25°C		15			8		%
Slew Rate	+25°C	550	600		550	600		V/μs
Settling Time: 10V Step to 0.1%	+25°C		350			350		ns
POWER REQUIREMENTS								
Supply Current	FULL		20	25		20	25	mA
Power Supply Rejection Ratio (Note 9)	FULL	60			60			dB

LINEAR

Harris Semiconductor

HARRIS

HA-2540

Wideband, Fast Settling Operational Amplifiers

Preliminary

FEATURES

- VERY HIGH SLEW RATE 400V/μs
- FAST SETTLING TIME 250ns
- WIDE GAIN-BANDWIDTH 400MHz
- POWER BANDWIDTH 6MHz
- LOW OFFSET VOLTAGE 5mV
- INPUT VOLTAGE NOISE 15nV/$\sqrt{Hz}$
- OUTPUT VOLTAGE SWING $\pm$10V
- MONOLITHIC BIPOLAR CONSTRUCTION

APPLICATIONS

- PULSE AND VIDEO AMPLIFIERS
- WIDEBAND AMPLIFIERS
- HIGH SPEED SAMPLE-HOLD CIRCUITS
- FAST, PRECISE D/A CONVERTERS

GENERAL DESCRIPTION

The Harris HA-2540 is a wideband, very high slew rate, monolithic operational amplifier featuring superior speed and bandwidth characteristics. Bipolar construction coupled with dielectric isolation allows this truly differential device to deliver outstanding performance. Additionally, the HA-2540 has a drive capability of $\pm$10V into a 1K ohm load. Other desirable characteristics include low input voltage noise, low offset voltage, and fast settling time.

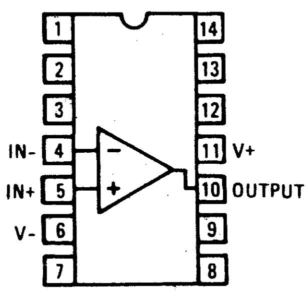
A 400V/μs slew rate ensures high performance in video and pulse amplification circuits, while the 400MHz gain-bandwidth-product is ideally suited for wideband signal amplification. A settling time of 250ns also makes the HA-2540 an excellent selection for high speed Data Acquisition Systems.

The HA-2540-2 is specified over the -55°C to +125°C range while the HA-2540-5 is specified from 0°C to +75°C.

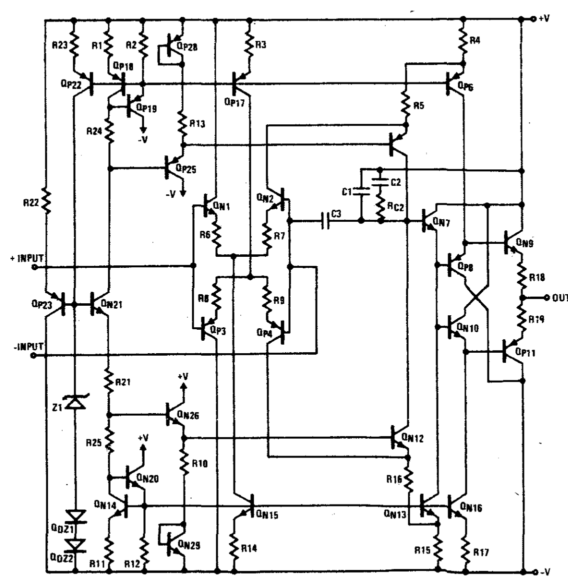
PINOUT

Section 11 for Packaging

TOP VIEW



SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage between V+ and V- Terminals	35V
Differential Input Voltage	6V
Output Current	50mA (Peak)
Internal Power Dissipation (Note 2)	870mW (Cerdip)
Operating Temperature Range: (HA-2540-2)	$-55^oC \leq T_A \leq +125^oC$
(HA-2540-5)	$0^oC \leq T_A \leq +75^oC$
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS $V_{SUPPLY} = \pm 15$ Volts; R_L = 1K ohms, unless otherwise specified.

		HA-2540-2 -55°C to +125°C			HA-2540-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		3	5		3	15	mV
	FULL			10			20	mV
Average Offset Voltage Drift	FULL		20			20		μV/°C
Bias Current	+25°C		5	20		5	20	μA
	FULL			25			25	μA
Offset Current	+25°C		1	6		1	6	μA
	FULL			8			8	μA
Input Resistance	+25°C		10			10		Kohms
Input Capacitance	+25°C		1.0			1.0		pF
Common Mode Range	FULL	±10			±10			V
Input Noise Voltage (f = 1kHz, R_g = 0Ω)	+25°C		15			15		nV/√Hz
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	15K	30K		10K	30K		V/V
	FULL	5K			5K			V/V
Common-Mode Rejection Ratio (Note 4)	FULL	60			60			dB
Gain-Bandwidth-Product (Notes 5 & 6)	+25°C		400			400		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 3)	FULL	±10			±10			V
Output Current (Note 3)	+25°C	10			10			mA
Output Resistance	+25°C		30			30		Ohms
Full Power Bandwidth (Note 3 & 7)	+25°C	5.5	6		5.5	6		MHz
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C		14			14		ns
Overshoot	+25°C		5			5		%
Slew Rate	+25°C	350	400		350	400		V/μs
Settling Time: 10V Step to 0.1%	+25°C		250			250		ns
POWER REQUIREMENTS								
Supply Current	FULL		20	25		20	25	mA
Power Supply Rejection Ratio (Note 9)	FULL	60			60			dB

LINEAR

Harris Semiconductor

HARRIS HA-2600/2602/2605

WideBand, High Impedance Operational Amplifiers

FEATURES

- WIDE BANDWIDTH 12MHz
- HIGH INPUT IMPEDANCE 500MΩ
- LOW INPUT BIAS CURRENT 1nA
- LOW INPUT OFFSET CURRENT 1nA
- LOW INPUT OFFSET VOLTAGE 0.5mV
- HIGH GAIN 150K V/V
- HIGH SLEW RATE 7V/μs
- OUTPUT SHORT CIRCUIT PROTECTION

APPLICATIONS

- VIDEO AMPLIFIER
- PULSE AMPLIFIER
- AUDIO AMPLIFIERS AND FILTERS
- HIGH-Q ACTIVE FILTERS
- HIGH-SPEED COMPARATORS
- LOW DISTORTION OSCILLATORS

DESCRIPTION

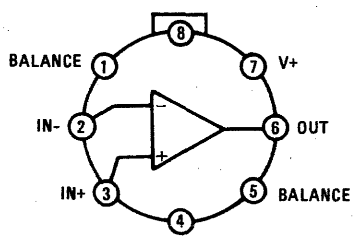
HA-2600/2602/2605 are internally compensated bipolar operational amplifiers that feature very high input impedance (500 MΩ, HA-2600) coupled with wideband AC performance. The high resistance of the input stage is complemented by low offset voltage (0.5mV, HA-2600) and low bias and offset current (1nA, HA-2600) to facilitate accurate signal processing. Input offset can be reduced further by means of an external nulling potentiometer. 12MHz unity gain-bandwidth product, 7V/μs slew rate and 150,000V/V open-loop gain enables HA-2600/2602/2605 to perform high-gain amplification of fast, wideband signals. These dynamic characterisitics, coupled with fast settling times, make these amplifiers ideally suited to pulse amplification designs as well as high frequency (e.g. video) applications. The frequency response of the amplifier can be tailored to exact design requirements by means of an external bandwidth control capacitor.

In addition to its application in pulse and video amplifier designs, HA-2600/2602/2605 is particularly suited to other high performance designs such as high-gain low distortion audio amplifiers, high-Q and wideband active filters and high-speed comparators.

HA-2600 and HA-2602 are guaranteed over -55°C to +125°C. HA-2605 is specified from 0°C to +75°C. All devices are available in TO-99 cans, and HA-2600/2602 are available in 10 lead flat packages.

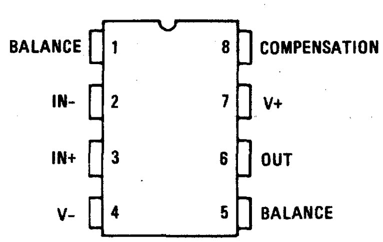
PINOUT

Section 11 for Packaging

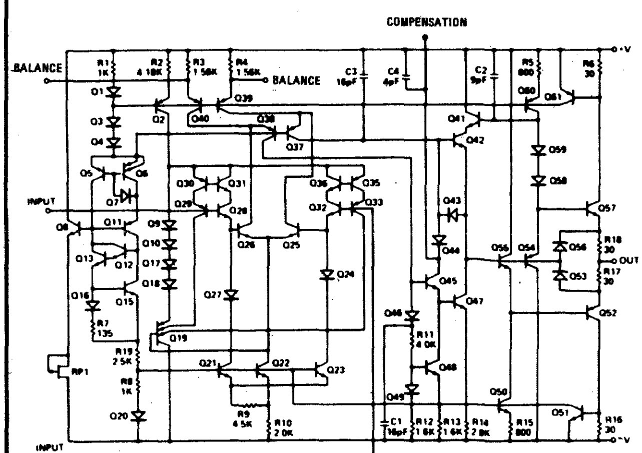


Case Connected to V-

TOP VIEWS



SCHEMATIC



LINEAR

Harris Semiconductor

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V− Terminals	45.0V
Differential Input Voltage	±12.0V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation	300mW
Operating Temperature Range – HA-2600/HA-2602	$-55^oC \leq T_A \leq +125^oC$
HA-2605	$0^o \leq T_A \leq +75^oC$
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS V+ = +15VDC, V- = -15VDC

PARAMETER	TEMP.	HA-2600 −55°C to +125°C LIMITS MIN.	TYP.	MAX.	HA-2602 −55°C to +125°C LIMITS MIN.	TYP.	MAX.	HA-2605 0°C to +75°C LIMITS MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		0.5	4		3	5		3	5	mV
	Full		2	6			7			7	mV
Offset Voltage Average Drift	Full		5								μV/°C.
Bias Current	+25°C		1	10		15	25		5	25	nA
	Full		10	30			60			40	nA
Offset Current	+25°C		1	10		5	25		5	25	nA
	Full		5	30			60			40	nA
Input Resistance (Note 10)	+25°C	100	500		40	300		40	300		MΩ
Common Mode Range	Full	±11.0			±11.0			±11.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Notes 1, 4)	+25°C	100K	150K		80K	150K		80K	150K		V/V
	Full	70K			60K			70K			V/V
Common Mode Rejection Ratio (Note 2)	Full	80	100		74	100		74	100		dB
Unity Gain Bandwidth (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 4)	+25°C	±15	±22		±10	±18		±10	±18		mA
Full Power Bandwidth (Note 4 & 11)	+25°C	50	75		50	75		50	75		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		30	60		30	60		30	60	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	40		25	40	%
Slew Rate (Notes 1, 5, 8 & 12)	+25°C	±4	±7		±4	±7		±4	±7		V/μs
Settling Time (Notes 1, 5, 8 & 12)	+25°C		1.5			1.5			1.5		μs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		3.0	3.7		3.0	4.0		3.0	4.0	mA
Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

TEST CONDITIONS

NOTES:
1. $R_L = 2K$
2. $V_{CM} = \pm 10V$
3. $V_O < 90mV$
4. $V_O = \pm 10V$
5. $C_L = 100pF$
6. $V_O = \pm 200mV$
7. $V_O = \pm 200mV$
8. See Transient response test circuits and waveforms
9. $\Delta VS = \pm 5V$
10. This parameter value guaranteed by design calculations.
11. Full power bandwidth guaranteed by slew rate measurement. $FPBW = S.R./2\pi V_{peak}$.
12. $V_{OUT} = \pm 5V$

HARRIS HA-2620/2622/2625

Very WideBand, Uncompensated Operational Amplifiers

FEATURES

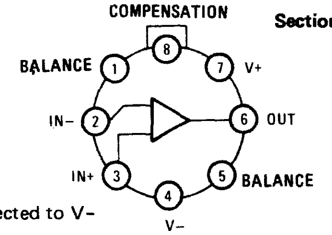
- GAIN BANDWIDTH PRODUCT(A_V = 5) 100MHz
- HIGH INPUT IMPEDANCE 500MΩ
- LOW INPUT BIAS CURRENT 1nA
- LOW INPUT OFFSET CURRENT 1nA
- LOW INPUT OFFSET VOLTAGE 0.5mV
- HIGH GAIN 150K V/V
- HIGH SLEW RATE 35V/μs
- OUTPUT SHORT CIRCUIT PROTECTION

APPLICATIONS

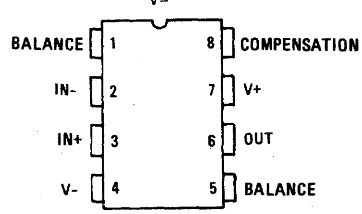
- VIDEO AND R.F. AMPLIFIERS
- PULSE AMPLIFIER
- AUDIO AMPLIFIERS AND FILTERS
- HIGH-Q ACTIVE FILTERS
- HIGH-SPEED COMPARATORS
- LOW DISTORTION OSCILLATORS

PINOUT

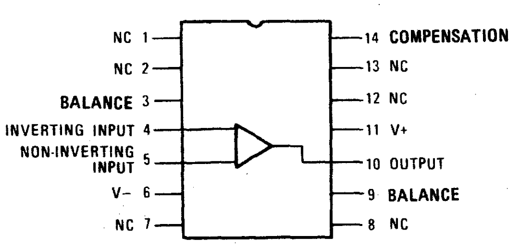
Section 11 for Packaging



Case Connected to V-



TOP VIEWS



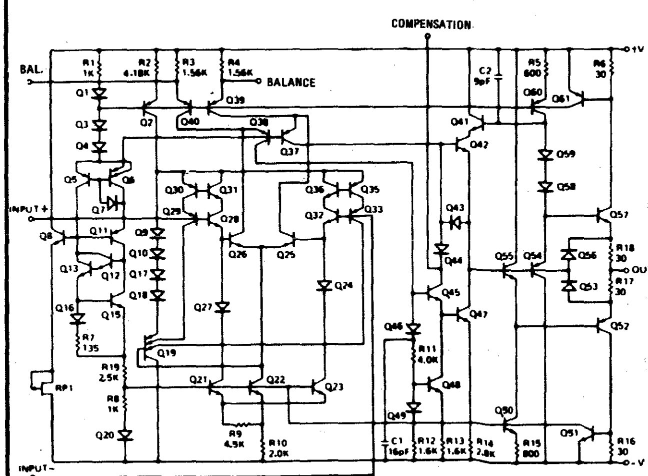
DESCRIPTION

HA-2620/2622/2625 are bipolar operational amplifiers that feature very high input impedance (500MΩ, HA-2620) coupled with wideband AC performance. The high resistance of the input stage is complemented by low offset voltage (0.5mV, HA-2620) and low bias and offset current (1nA, HA-2620) to facilitate accurate signal processing. Input offset can be reduced further by means of an external nulling potentiometer. 100MHz gain-bandwidth product (HA-2620/2622/2625 are stable for closed loop gains greater than 5), 35V/ μs slew rate and 150,000V/V open-loop gain enables HA-2620/2622/2625 to perform high-gain amplification of very fast, wideband signals. These dynamic characterisitcs, coupled with fast settling times, make these amplifiers ideally suited to pulse amplification designs as well as high frequency (e.g. video) applications. The frequency response of the amplifier can be tailored to exact design requirements by means of an external bandwidth control capacitor.

In addition to its application in pulse and video amplifier designs HA-2620/2622/2625 is particularly suited to other high performance designs such as high-gain low distortion audio amplifiers, high-Q and wideband active filters and high-speed comparators.

HA-2620 and HA-2622 are guaranteed over -55°C to +125°C. HA-2625 is specified from 0°C to +75°C. All devices are available in TO-99 cans, and 14 lead D.I.P. packages.

SCHEMATIC



LINEAR

Harris Semiconductor

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	45.0V
Differential Input Voltage	±12.0V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation	300mW
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

$V^+ = +15$ VDC, $V^- = -15$ VDC

PARAMETER	TEMPERATURE	HA-2620 −55°C to +125°C MIN.	TYP.	MAX.	HA-2622 −55°C to +125°C MIN.	TYP.	MAX.	HA-2625 0°C to +75°C MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS											
Offset Voltage (Note 1)	+25°C		0.5	4		3	5		3	5	mV
	Full			6			7			7	mV
Bias Current	+25°C		1	15		5	25		5	25	nA
	Full		10	35			60			40	nA
Offset Current	+25°C		1	15		5	25		5	25	nA
	Full		5	35			60			40	nA
Input Resistance (Note 11)	+25°C	65	500		40	300		40	300		MΩ
Common Mode Range	Full	±11.0			±11.0			±11.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Notes 2 & 3)	+25°C	100K	150K		80K	150K		80K	150K		V/V
	Full	70K			60K			70K			V/V
Common Mode Rejection Ratio (Note 4)	Full	80	100		74	100		74	100		dB
Gain Bandwidth Product (Notes 2, 5, &6)	+25°C		100			100			100		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 2)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 3)	+25°C	±15	±22		±10	±18		±10	±18		mA
Full Power Bandwidth (Notes 2, 3, 7 &12)	+25°C	400	600		320	600		320	600		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 2, 7 & 8)	+25°C		17	45		17	45		17	45	ns
Slew Rate (Notes 2, 7, 8 & 10)	+25°C	±25	±35		± 20	±35		± 20	±35		V/μs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		3.0	3.7		3.0	4.0		3.0	4.0	mA
Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

NOTES:
1. Offset may be externally adjusted to zero.
2. $R_L = 2K\Omega$, $C_L = 50pF$
3. $V_O = \pm 10.0V$
4. $V_{CM} = \pm 10V$
5. $V_O < 90mV$
6. 40dB Gain
7. See transient response test circuits and waveforms
8. $A_V = 5$ (The HA-2620 family is not stable at unity gain without external compensation.)
9. $\Delta V_{Sup} = \pm 5V$
10. $V_{OUT} = \pm 5V$.
11. This parameter value based upon design calculations.
12. Full power bandwidth guaranteed based upon slew rate measurement $FPBW = S.R./2\pi V_{peak}$.

HARRIS

HA-2630/2635

High Performance Current Booster

FEATURES

• OUTPUT CURRENT	±400mA
• SLEW RATE	500V/μs
• BANDWIDTH	8MHz
• FULL POWER BANDWIDTH	8MHz
• INPUT RESISTANCE	$2.0 \times 10^6\Omega$
• OUTPUT RESISTANCE	2.0Ω
• POWER SUPPLY RANGE	±5V to ±20V
• PACKAGE IS ELECTRICALLY ISOLATED	

APPLICATIONS

- COAXIAL CABLE DRIVERS
- AUDIO OUTPUT AMPLIFIERS
- SERVO MOTOR DRIVERS
- POWER SUPPLIES (BIPOLAR)
- PRECISION DATA RECORDING

DESCRIPTION

HA-2630 and HA-2635 are monolithic, unity voltage gain current amplifiers delivering extremely high slew rate, wide bandwidth, and full power bandwidth even under heavy output loading conditions. This dielectrically isolated current booster also offers high input impedance and low output resistance. These devices are intended to be used in series with an operational amplifier and inside the feedback loop whenever additional output current is required. Output current levels are programmable by selecting two optional external resistors.

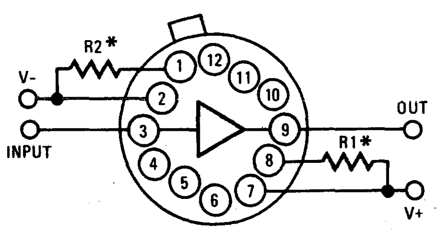
These current amplifiers offer an exceptional 500V/μs slew rate and 8MHz bandwidth which allows them to be used with many high performance op amps in precision data recording and high speed coaxial cable driver designs. 2.0M ohm input resistance and 2 ohm output resistance coupled with ±400mA output current make HA-2630 and HA-2635 ideal components in high fidelity audio output amplifier designs.

HA-2630 and HA-2635 are available in an electrically isolated TO-8 type can for ease of mounting with or without a heat sink. HA-2630 is specified over the -55°C to +125°C range. HA-2635 is specified from 0°C to +75°C.

PINOUT

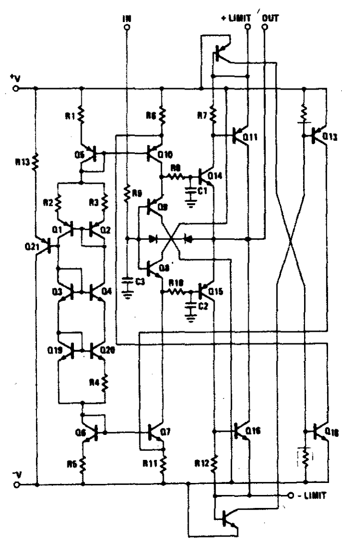
Section 11 for Packaging

TOP VIEW



* Optional Current Limiting Resistor

SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40V
Input Voltage Range	± V Supply
Output Current (Note 2)	±700mA
Internal Power Dissipation (Note 6) Free Air:	1W
In Heat Sink:	4W

Operating Temperature Range:
$-55^oC \leq T_A \leq +125^oC$ (HA-2630)
$0^oC \leq T_A \leq +75^oC$ (HA-2635)
Storage Temperature Range:
$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

$V_{Supply} = \pm15$ Volts $R_L = 50$ Ohms $R_1 = R_2 = 0$ Ohms   Unless otherwise specified.

PARAMETER	TEMP.	HA-2630 -55°C to +125°C MIN.	TYP.	MAX.	HA-2635 0°C to +75°C MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
Bias Current	+25°C		30	150		30	150	µA
	Full			200			200	µA
Input Resistance	+25°C		2.0			2.0		MΩ
Input Capacitance	+25°C		5.0			5.0		pF
TRANSFER CHARACTERISTICS								
Voltage Gain (Note 1)	Full	.85	.95		.85	.95		V/V
Offset Voltage ($V_{OUT} - V_{IN}$)	+25°C		70	±200		70	±200	mV
	Full			±300			±300	mV
Bandwidth (-3dB)	+25°C		8.0			8.0		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	±10	±12		±10	±12		V
Output Current (Note 1)	Full	±300	±400		±300	±400		mA
Output Resistance	+25°C		2.0			2.0		Ω
Full Power Bandwidth (Note 1)	+25°C		8.0			8.0		MHz
TRANSIENT RESPONSE								
Rise Time (Note 3)	+25°C		30			30		ns
Slew Rate (Note 4)	+25°C	200	500		200	500		V/µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full		15	20		15	23	mA
Supply Voltage Range	Full	±5		±20	±5		±20	V
Power Supply Rejection Ratio (Note 5)	Full		66			66		dB

NOTES:
1. $V_O = \pm10V$
2. Heat sink is required for continuous short circuit protection, regardless of current limit setting.
3. $V_O = 0.4V$ p-p.
4. $V_O = 10V$ p-p.
5. $\Delta V_{SUPPLY} = \pm5V$.
6. Without heat sink, derate by 14mW/°C ambient temperature above 100°C ambient, with heat sink, derate by 67mW/°C case temperature above 115°C case.

LINEAR

Harris Semiconductor

HARRIS

HA-2640/2645

High Voltage Operational Amplifier

FEATURES

- OUTPUT VOLTAGE SWING ±35V
- SUPPLY VOLTAGE ±10V TO ±40V
- OFFSET CURRENT 5nA
- BANDWIDTH 4MHz
- SLEW RATE 5V/μs
- COMMON MODE INPUT VOLTAGE SWING ±35V
- OUTPUT OVERLOAD PROTECTION

APPLICATIONS

- INDUSTRIAL CONTROL SYSTEMS
- POWER SUPPLIES
- HIGH VOLTAGE REGULATORS
- RESOLVER EXCITATION
- SIGNAL CONDITIONING

DESCRIPTION

HA-2640 and HA-2645 are monolithic operational amplifiers which are designed to deliver unprecedented dynamic specifications for a high voltage internally compensated device. These dielectrically isolated devices offer very low values for offset voltage and offset current coupled with large output voltage swing and common mode input voltage.

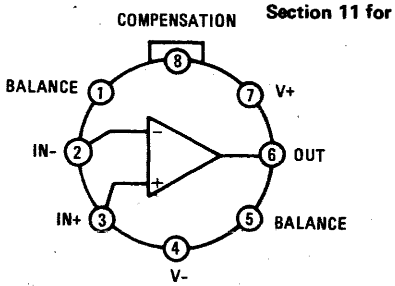
For maximum reliability, these amplifiers offer unconditional output overload protection through current limiting and a chip temperature sensing circuit. This sensing device turns the amplifier "off", when the chip reaches a certain temperature level.

These amplifers deliver ±35V common mode input voltage swing, ±35V output voltage swing, and up to ±40V supply range for use in such designs as regulators, power supplies, and industrial control systems. 4MHz gain bandwidth and 5V/μs slew rate make these devices excellent components for high performance signal conditioning applications. Outstanding input and output voltage swings coupled with a low 5nA offset current make these amplifiers excellent components for resolver excitation designs.

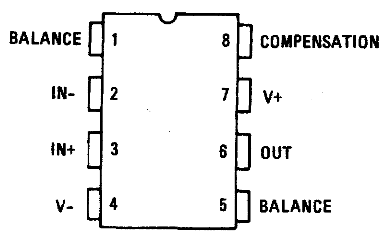
HA-2640 and HA-2645 are available in metal can (TO-99) packages and can be used as high performance pin-to-pin replacements for many general purpose op amps. HA-2640 is specified from -55°C to +125°C and HA-2645 is specified over the 0°C to +75°C range.

PINOUT

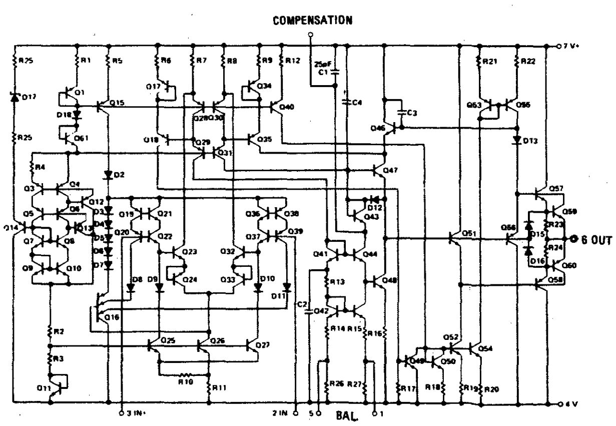
Section 11 for Packaging



TOP VIEWS



SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals 100V
Input Voltage Range ±37V
Output Current/Full Short Circuit Protection
Internal Power Dissipation 680mW*

*Derate by 4.6mW/°C above +25°C

Operating Temperature Range
$-55^oC \leq T_A \leq +125^oC$ (HA-2640)
$0^oC \leq T_A \leq +75^oC$ (HA-2645)
Storage Temperature Range
$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

$V_{Supply} = \pm 40V$, $R_L = 5K$, Unless Otherwise Specified.

PARAMETER	TEMP.	HA-2640 -55°C to +125°C MIN.	TYP.	MAX.	HA-2645 0°C to +75°C MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		2	4		2	6	mV
	Full			6			7	mV
Offset Voltage Average Drift	Full		15			15		µV/°C
Bias Current	+25°C		10	25		12	30	nA
	Full			50			50	nA
Offset Current	+25°C		5	12		15	30	nA
	Full			35			50	nA
Input Resistance **(Note 10)**	+25°C	50	250		40	200		MΩ
Common Mode Range	Full	±35			±35			V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain **(Note 8)**	+25°C	100K	200K		100K	200K		V/V
	Full	75K			75K			V/V
Common Mode Rejection Ratio (Note 1)	Full	80	100		74	100		dB
Unity Gain Bandwidth (Note 2)	+25°C		4			4		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	±35			±35			V
Output Current **(Note 9)**	+25°C	±12	±15		±10	±12		mA
Output Resistance	+25°C		500			500		Ω
Full Power Bandwidth **(Notes 3 & 11)**	+25°C		23			23		kHz
TRANSIENT RESPONSE (Note 7)								
Rise Time (Notes 4, 6)	+25°C		60	**100**		60	**100**	ns
Overshoot (Notes 4, 6)	+25°C		15	**30**		15	**40**	%
Slew Rate (Note 6)	+25°C	**±3**	**±5**		**±2.5**	**±5**		V/µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		3.2	3.8		3.2	4.5	mA
Supply Voltage Range	Full	±10		±40	±10		±40	V
Power Supply Rejection Ratio (Note 5)	Full	80	90		74	90		dB

NOTES:
1. $V_{CM} = \pm 20V$
2. $V_O = 90mV$
3. $V_O = \pm 35V$
4. $V_O = \pm 200mV$
5. $V_S = \pm 10V$ to $\pm 40V$
6. $A_V = 1$
7. $C_L = 50pF$
8. $V_O = \pm 30V$
9. $R_L = 1K$
10. This parameter based upon design calculations.
11. Full power bandwidth guaranteed based upon slew rate measurement. $FPBW = S.R./2\pi V_{peak}$.

LINEAR

Harris Semiconductor

HARRIS

HA-2650/2655

Dual High Performance Operational Amplifier

LINEAR

Harris Semiconductor

FEATURES

- SLEW RATE 5V/μs
- BANDWIDTH 8MHz
- BIAS CURRENT 35nA
- AV. OFFSET VOLTAGE DRIFT 8μV/^{o}C
- POWER CONSUMPTION 75mW
- SUPPLY VOLTAGE RANGE ±2V TO ±20V

APPLICATIONS

- VIDEO AMPLIFIERS
- HIGH IMPEDANCE, WIDEBAND BUFFERS
- INTEGRATORS
- AUDIO AMPLIFIERS
- ACTIVE FILTERS

DESCRIPTION

HA-2650/2655 contains two internally compensated operational amplifiers offering high slew rate and high frequency performance combined with exceptional DC characteristics. 5V/μ sec slew rate and 8MHz bandwidth make these amplifiers suitable for processing fast, wideband signals extending into the video frequency spectrum. Signal processing accuracy is enhanced by front-end performance that includes 1.5mV offset voltage, 8μ V/^{o}C offset voltage drift and low offset and bias current (1nA and 35nA respectively). Offset voltage can be trimmed to zero on the devices offered in dual-in-line packages. Signal conditioning is further enhanced by 500MΩ input impedance.

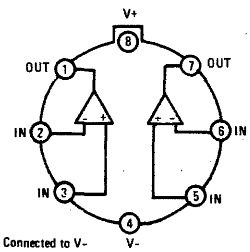
Applications for HA-2650/2655 include video circuit designs such as high impedance buffers, integrators, tone generators and filters. These amplifiers are also ideal components for active filtering of audio and voice signals.

HA-2650/2655 are offered in 14 pin D.I.P. and metal TO-99 packages and are also available in dice form. HA-2650 is specified from -55^{o}C to +125^{o}C. HA-2655 operates from 0^{o}C to +75^{o}C.

PINOUT

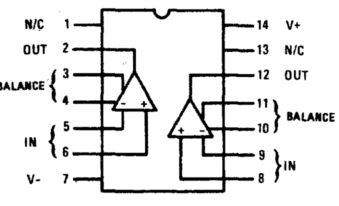
TOP VIEW

Section 11 for Packaging



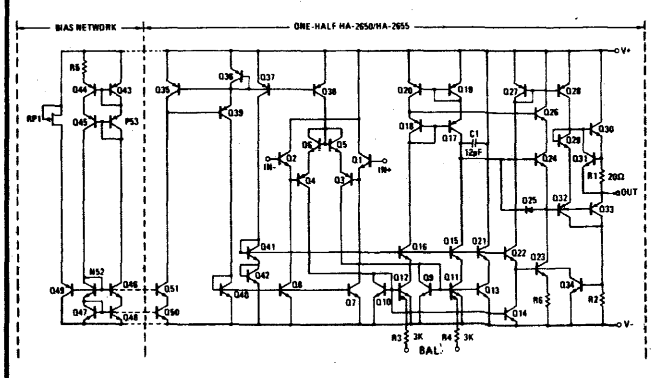
NOTE: Case Connected to V-

TOP VIEW



NOTE: Bottom of package is connected to V-.

SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

$T_A = +25^oC$ Unless Otherwise Stated

Voltage Between V+ and V- Terminals	40.0V
Differential Input Voltage	±30.0V
Input Voltage (Note 1)	±15.0V
Output Short Circuit Duration	Indefinite

Power Dissipation (Note 2)	TO-99	300 mW
	TO-116	300 mW
Operating Temperature Range:		
HA-2650		$-55^oC \leq T_A \leq +125^oC$
HA-2655		$0^oC \leq T_A \leq +75^oC$
Storage Temperature Range		$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

V+ = 15V V- = -15V

PARAMETER	TEMP.	HA-2650 -55°C to +125°C MIN.	TYP.	MAX.	HA-2655 0°C to +75°C MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		1.5	3		2	5	mV
	Full			5			7	mV
Av. Offset Voltage Drift	Full		8			8		μV/°C
Bias Current	+25°C		35	100		50	200	nA
	Full			200			300	nA
Offset Current	+25°C		1	30		2	60	nA
	Full			60			100	nA
Common Mode Range	Full	±13			±13			V
Differential Input Resistance (Note 9)	+25°C	5	20		5	20		MΩ
Common Mode Input Resistance	+25°C		500			500		MΩ
Input Capacitance	+25°C		5			5		pF
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3ab)	+25°C	20K	40K		15K	40K		V/V
	Full	15K			10K			V/V
Common Mode Rejection Ratio (Note 4)	+25°C	80	100		74	100		dB
	Full	80			74			dB
OUTPUT CHARACTERISTICS								
*Output Voltage Swing (Note 3c)	+25°C	±13	±14		±13	±14		V
	Full	±13			±13			V
Full Power Bandwidth (Notes 5 &10)	+25°C	30	80		30	80		KHz
Output Current (Note 3a)	+25°C		±20			±18		mA
Output Resistance	+25°C		100			100		Ω
TRANSIENT RESPONSE (Note 6)								
Rise Time (Note 7)	+25°C		40	80		40	90	ns
Overshoot (Note 7)	+25°C		15	30		15	40	%
Slew Rate	+25°C	±2	±5		±2	±5		V/μs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		2.5	4		3	5	mA
Power Supply Rejection Ratio (Note 8)	+25°C	80	100		74	100		dB
	Full	80			74			dB

NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Derate at 4.7mW/°C at ambient temperatures above +110°C.
3. (a) $V_O = \pm10V$ (b) $R_L = 2K$ (c) $R_L = 10K$
4. $V_{CM} = \pm5.0V$
5. $A_V = 1, R_L = 2K, V_O = 20V_{pp}$
6. See transient response/slew rate circuit.
7. $V_{in} = 200mV$
8. $\Delta V = \pm5.0V$
9. This parameter value based upon design calculations.
10. Full power bandwidth guaranteed based upon slew rate measurement $FPBW = S.R./2\pi V_{peak}$.

LINEAR

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HARRIS

HA-2720/25

Wide Range Programmable Operational Amplifier

FEATURES

- WIDE PROGRAMMING RANGE

SLEW RATE	0.06 TO 6V/μs
BANDWIDTH	5kHz TO 10MHz
BIAS CURRENT	0.4 TO 50nA
SUPPLY CURRENT	1μA TO 1.5mA

- WIDE POWER SUPPLY RANGE ±1.2 TO ±18V
- CONSTANT AC PERFORMANCE OVER SUPPLY RANGE

APPLICATIONS

- ACTIVE FILTERS
- CURRENT CONTROLLED OSCILLATORS
- VARIABLE ACTIVE FILTERS
- MODULATORS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

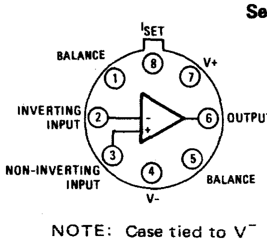
HA-2720/2725 programmable amplifiers are internally compensated monolithic devices offering a wide range of performance, that can be controlled by adjusting the circuits' "set" current (I_{SET}). By means of adjusting an external resistor or current source, power dissipation, slew rate, bandwidth, output current and input noise can be programmed to desired levels. This versatile adjustment capability enables HA-2720/2725 to provide optimum design solutions by delivering the required level of performance with minimum possible power dissipation. HA-2720 and HA-2725 can, therefore, be utilized as the standard amplifier for a variety of designs simply by adjusting their programming current.

A major advantage of HA-2720/2725 is that operating characteristics remain virtually constant over a wide supply range (±1.2V to ±15V), allowing the amplifiers to offer maximum performance in almost any system including battery-operated equipment. A primary application for HA-2720/2725 is in active filters for a wide variety of signals that differ in frequency and amplitude. Also, by modulating the "set" current, HA-2720/2725 can be used for designs such as current controlled oscillators modulators, sample and hold circuits and variable active filters.

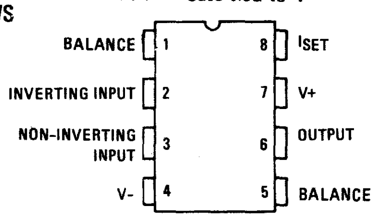
HA-2720 is guaranteed over -55°C to +125°C. HA-2725 is specified from 0°C to +75°C. Both parts are available in TO-99 cans or dice form.

PINOUT

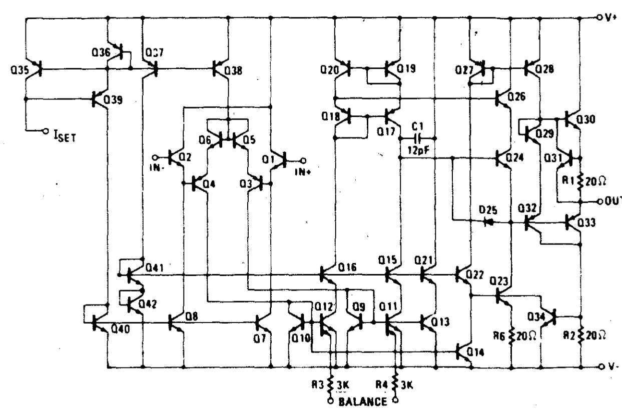
Section 11 for Packaging



TOP VIEWS



SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	45.0V	Power Dissipation (Note 2)	300mW
Differential Input Voltage	±30.0V	Operating Temperature Range:	
Input Voltage (Note 1)	±15.0V	HA-2720	$-55^oC \leq T_A \leq +125^oC$
I_{SET} (Current at I_{SET})	500μA	HA-2725	$0^oC \leq T_A \leq +75^oC$
V_{SET} (Voltage to Gnd. at I_{SET})	$V+ - 2.0V \leq V_{SET} \leq V+$	Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

V+ = +3.0V, V- = -3.0V

PARAMETER	TEMP.	HA-2720 -55°C to +125°C I_{SET} = 1.5μA MIN.	TYP.	MAX.	I_{SET} = 15μA MIN.	TYP.	MAX.	HA-2725 0°C to +75°C I_{SET} = 1.5μA MIN.	TYP.	MAX.	I_{SET} = 15μA MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS														
Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance (Note 10)	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Note 9)	25°C	15K	40K		15K	40K		15K	40K		15K	40K		V/V
	Full	10K			10K			10K			10K			V/V
Common Mode Rejection Ratio (Note 4)	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 3)	25°C	±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		V
	Full	±2.0			±1.9			±2.0			±2.0			V
Output Current (Note 5)	25°C		±0.2			±2.0			±0.2			±2.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		2.8			14			2.8			14		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.5			0.25			2.5			0.25		μs
Overshoot (Note 6)	25°C		5			10			5			10		%
Slew Rate (Note 7)	25°C		0.07			0.70			0.07			0.70		V/μs
POWER SUPPLY CHARACTERISTICS														
Supply Current	25°C		15			170			15			170		μA
	Full			25			250			25			250	μA
Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150			μV/V

LINEAR

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ELECTRICAL CHARACTERISTICS

V+ = +15.0V, V- = -15.0V

PARAMETER	TEMP.	HA-2720 -55°C to +125°C I_{SET} = 1.5μA MIN.	TYP.	MAX.	I_{SET} = 15μA MIN.	TYP.	MAX.	HA-2725 0°C to +75°C I_{SET} = 1.5μA MIN.	TYP.	MAX.	I_{SET} = 15μA MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS														
Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance (Note 10)	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Notes 3 & 9)	25°C	30K	100K		30K	120K		25K	100K		25K	120K		V/V
	Full	20K			20K			20K			20K			V/V
Common Mode Rejection Ratio (Note 4)	25°C		90			90			90			90		dB
	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 3)	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
	Full	±10			±10			±10			±10			V
Output Current (Note 5)	25°C		±0.5			±5.0			±0.5			±5.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		3.7			19			3.7			19		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.0			0.2			2.0			0.2		μs
Overshoot (Note 6)	25°C		5			15			5			15		%
Slew Rate (Note 7)	25°C		0.1			0.8			0.1			0.8		V/μs
POWER SUPPLY CHARACTERISTICS														
Supply Current	25°C		20			210			20			210		μA
	Full			50			450			50			450	μA
Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150			μV/V

NOTES:

1. For supply voltages less than ±15.0V, the absolute maximum input voltage is equal to supply voltage.
2. Derate at 6.8mW/°C for operation ambient temperatures above 75°C.

	V_{SUPPLY} = ±3.0V	V_{SUPPLY} = ±15.0V	I_{SET} = 1.5μA	I_{SET} = 15μA
3.	T = +25°C and Full	T = +25°C	R_L = 75KΩ	R_L = 5KΩ
	—	T = Full	R_L = 75KΩ	R_L = 75KΩ
4.	V_{CM} = ±1.5V	V_{CM} = ±5.0V		
5.	V_O = ±2.0V	V_O = ±10.0V		
6.	← A_V = +1, V_{IN} = 400mV, R_L = 5K, C_L = 100pF →			
7.	V_O = ±2.0V	V_O = ±10.0V	R_L = 20K	R_L = 5K
8.	ΔV = ±1.5V	ΔV = ±5.0V		
9.	V_O = ±1.0V	V_O = ±10.0V		

10. This parameter based upon design calculations.

LINEAR

Harris Semiconductor

HARRIS

HA-2730/35

Wide Range Dual Programmable Operational Amplifier

FEATURES

- WIDE PROGRAMMING RANGE

SET CURRENT	0.1 TO 100μA
SLEW RATE	0.06 TO 6V/μs
BANDWIDTH	5kHz TO 10MHz
BIAS CURRENT	0.4 TO 50nA
SUPPLY CURRENT	1μA TO 1.5mA

- WIDE POWER SUPPLY RANGE ±1.2 TO ±18V
- CONSTANT AC PERFORMANCE OVER SUPPLY RANGE

APPLICATIONS

- ACTIVE FILTERS
- CURRENT CONTROLLED OSCILLATORS
- VARIABLE ACTIVE FILTERS
- MODULATORS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

HA-2730/2735 Dual Programmable Amplifiers are internally compensated monolithic devices offering a wide range of performance, that can be controlled by adjusting the circuits' "set" current (I_{SET}). By means of adjusting an external resistor or current source, power dissipation, slew rate, bandwidth, output current and input noise can be programmed to desired levels. Each amplifier on the chip can be adjusted independently. This versatile adjustment capability enables HA-2730/2735 to provide optimum design solutions by delivering the required level of performance with minimum possible power dissipation. HA-2730/2735 can, therefore, be utilized as the standard amplifier for a variety of designs simply by adjusting their programming current.

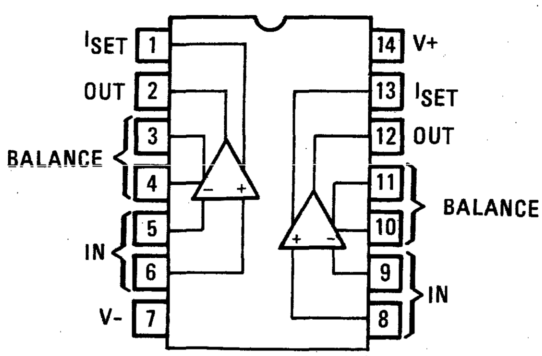
A major advantage of HA-2730/2735 is that operating characteristics remain virtually constant over a wide supply range (±1.2V to ±15V), allowing the amplifiers to offer maximum performance in almost any system including battery-operated equipement. A primary application for HA-2730/2735 is in active filters for a wide variety of signals that differ in frequency and amplitude. Also, by modulating the "set" current, HA-2730/2735 can be used for designs such as current controlled oscillators, modulators, sample and hold circuits and variable active filters.

HA-2730 is guaranteed over -55°C to +125°C. HA-2735 is specified from 0°C to +75°C. Both parts are available in 14 lead D.I.P. package or dice form.

PINOUT

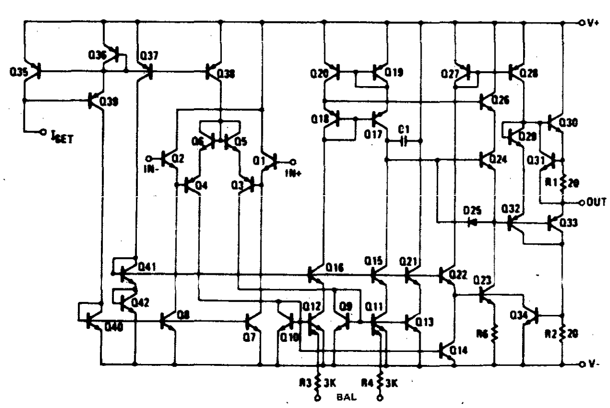
Section 11 for Packaging

TOP VIEW



NOTE: Bottom of package is connected to V-.

SCHEMATIC



(ONE HALF ONLY) HA-2730/35

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ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	45.0V
Differential Input Voltage	±30.0V
Input Voltage (Note 1)	±15.0V
I_{SET} (Current at I_{SET})	500µA
V_{SET} (Voltage to Gnd. at I_{SET})	$V+ - 2.0V \leq V_{SET} \leq V+$
Power Dissipation (Note 2)	500mW
Operating Temperature Range:	
HA-2730	$-55^\circ C \leq T_A \leq +125^\circ C$
HA-2735	$0^\circ C \leq T_A \leq +75^\circ C$
Storage Temperature Range	$-65^\circ C \leq T_A \leq +150^\circ C$

ELECTRICAL CHARACTERISTICS (Each Side)

V+ = +3.0V, V- = -3.0V

PARAMETER	TEMP.	HA-2730 -55°C to +125°C, I_{SET} = 1.5µA MIN.	TYP.	MAX.	HA-2730, I_{SET} = 15µA MIN.	TYP.	MAX.	HA-2735 0°C to +75°C, I_{SET} = 1.5µA MIN.	TYP.	MAX.	HA-2735, I_{SET} = 15µA MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS														
Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance (Note 10)	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Notes 3 & 9)	25°C	15K	40K		15K	40K		15K	40K		15K	40K		V/V
	Full	10K			10K			10K			10K			V/V
Common Mode Rejection Ratio (Note 4)	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 3)	25°C	±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		V
	Full	±2.0			±1.9			±2.0			±2.0			V
Output Current (Note 5)	25°C		±0.2			±2.0			±0.2			±2.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		2.8			14			2.8			14		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.5			0.25			2.5			0.25		µs
Overshoot (Note 6)	25°C		5			10			5			10		%
Slew Rate (Note 7)	25°C		0.07			0.70			0.07			0.70		V/µs
POWER SUPPLY CHARACTERISTICS														
Supply Current (Each Amp)	25°C		15			170			15			170		µA
	Full			25			250			25			250	µA
Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150			µV/V

ELECTRICAL CHARACTERISTICS (Each Side)

V+ = +15.0V, V- = -15.0V

PARAMETER	TEMP.	HA-2730 -55°C to +125°C I_{SET} = 1.5μA MIN.	TYP.	MAX.	HA-2730 I_{SET} = 15μA MIN.	TYP.	MAX.	HA-2735 0°C to +75°C I_{SET} = 1.5μA MIN.	TYP.	MAX.	HA-2735 I_{SET} = 15μA MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS														
Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance (Note 10)	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Notes 3 & 9)	25°C	30K	100K		30K	120K		25K	100K		25K	120K		V/V
	Full	20K			20K			20K			20K			V/V
Common Mode Rejection Ratio (Note 4)	25°C		90			90			90			90		dB
	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 3)	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
	Full	±10			±10			±10			±10			V
Output Current (Note 5)	25°C		±0.5			±5.0			±0.5			±5.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		3.7			19			3.7			19		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.0			0.2			2.0			0.2		μs
Overshoot (Note 6)	25°C		5			15			5			15		%
Slew Rate (Note 7)	25°C		0.1			0.8			0.1			0.8		V/μs
POWER SUPPLY CHARACTERISTICS														
Supply Current (Each Amp)	25°C		20			210			20			210		μA
	Full			50			450			50			450	μA
Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150			μV/V

NOTES:
1. For supply voltages less than ±15.0V, the absolute maximum input voltage is equal to supply voltage.
2. Derate at 4.7mW/°C at ambient temperature above 68°C.

	V_{SUPPLY} = ±3.0V	V_{SUPPLY} = ±15.0V	I_{SET} = 1.5μA	I_{SET} = 15μA
3.	T = +25°C and Full	T = +25°C	R_L = 75KΩ	R_L = 5KΩ
	—	T = Full	R_L = 75KΩ	R_L = 75KΩ
4.	V_{CM} = ±1.5V	V_{CM} = ±5.0V		
5.	V_O = ±2.0V	V_O = ±10.0V		
6.	← A_V = +1, V_{IN} = 400mV, R_L = 5K, C_L = 100pF →			
7.	V_O = ±2.0V	V_O = ±10.0V	R_L = 20K	R_L = 5K
8.	ΔV = ±1.5V	ΔV = ±5.0V		
9.	V_O = ±1.0V	V_O = ±10.0V		

10. This parameter value based upon design calculations.

LINEAR

Harris Semiconductor

HARRIS

HA-2740

Quad Programmable Operational Amplifier

FEATURES

- WIDE PROGRAMMING RANGE
  - ▶ SLEW RATE 0.8V/μs
  - ▶ BANDWIDTH 1MHz
  - ▶ BIAS CURRENT 8nA
  - ▶ SUPPLY CURRENT 250μA
- WIDE POWER SUPPLY RANGE
- CONSTANT AC PERFORMANCE OVER SUPPLY RANGE

DESCRIPTION

The Harris HA-2740 programmable amplifier is an internally compensated monolithic device offering a wide range of performance, that can be controlled by adjusting the circuit "set" current (I_{SET}). By means of adjusting an external resistor or current source, power dissipation, slew rate, bandwidth, output current and input noise can be programmed to desired levels. This versatile adjustment capability enables the HA-2740 to provide optimum design solutions by delivering the required level of performance with minimum possible power dissipation. The HA-2740 can, therefore, be utilized as the standard amplifier for a variety of designs simply by adjusting programming current.

A major advantage of the HA-2740 is that operating characteristics remain virtually constant over a wide supply range (±1.2V to ±18V), allowing the amplifier to offer maximum performance in almost any system including battery-operated equipment. A primary application for the HA-2740 is in active filters for a wide variety of signals that differ in frequency and amplitude. Also, by modulating the "set" current, the HA-2740 can be used for designs such as current controlled oscillators, modulators, sample and hold circuits and variable active filters.

The HA-2740-2 is guaranteed over -55°C to +125°C. The HA-2740-5 is specified from 0°C to +75°C. Both parts are available in a 16 pin dual-in-line package.

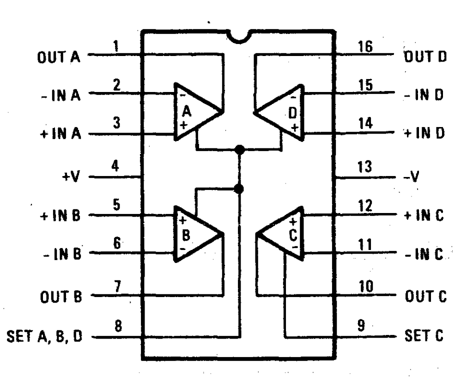
APPLICATIONS

- ACTIVE FILTERS
- CURRENT CONTROLLED OSCILLATORS
- VARIABLE ACTIVE FILTERS
- MODULATORS
- BATTERY-POWERED EQUIPMENT

PINOUT

Section 11 for Packaging

TOP VIEW



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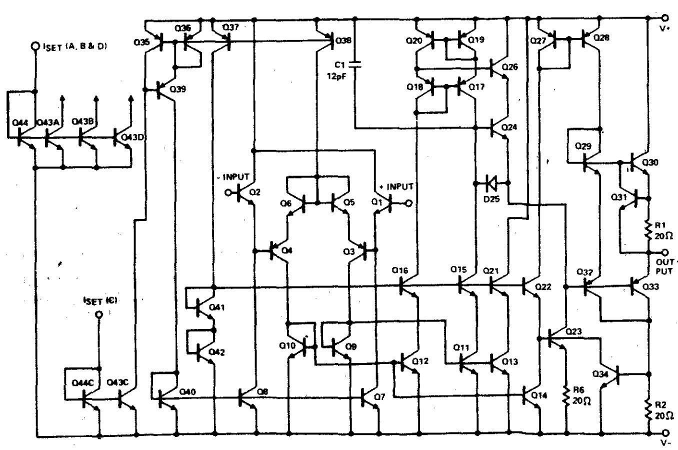


ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V- Terminals	45.0V
Differential Input Voltage	±30.0V
Input Voltage (Note 2)	±15.0V
I_{SET} (Current at I_{SET})	500μA
V_{SET} (Voltage to Gnd. at I_{SET})	$V+ - 2.0 \leq V_{SET} \leq V+$
Power Dissipation	300mW
Operating Temperature Range:	
HA-2740-2	$-55^oC \leq T_A \leq +125^oC$
HA-2740-5	$0^oC \leq T_A \leq +75^oC$
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS V+ = +15.0V, V- = -15.0V

PARAMETER	TEMP	HA-2740-2 -55°C to +125°C I_{SET} = 1.5μA MIN	TYP	MAX	HA-2740-2 I_{SET} = 15μA MIN	TYP	MAX	HA-2740-5 0°C to +75°C I_{SET} = 1.5μA MIN	TYP	MAX	HA-2740-5 I_{SET} = 15μA MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS														
Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			30	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance (Note 3)	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Note 4)	25°C	30K	100K		30K	120K		25K	100K		25K	120K		V/V
	Full	20K			20K			20K			20K			V/V
Common Mode Rejection Ratio (Note 5)	25°C		100			100			100			100		dB
	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 6)	25°C	±12	±14		±12	±14		±12	±14		±12	±14		V
	Full	±10			±10			±10			±10			V
Channel Separation (Note 7)	25°C		110			110			110			110		dB
Output Current (Note 8)	25°C		±0.5			±5.0			±0.5			±5.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short Circuit Current	25°C		3.6			16			3.6			16		mA
TRANSIENT RESPONSE														
Rise Time (Note 9)	25°C		2.0			0.2			2.0			0.2		μs
Overshoot (Note 9)	25°C		2			10			2			10		%
Slew Rate (Note 10)	25°C		0.1			0.8			0.1			0.8		V/μs
POWER SUPPLY CHARACTERISTICS														
Supply Current (each amp)	25°C		25			250			25			250		μA
	Full			50			450			50			450	μA
Power Supply Rejection Ratio (Note 11)	Full	100				100		150			150			μV/V

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. This parameter based upon design calculations.
4. V_O = ±10V, R_L = 5K @ I_{SET} = 15μA
   R_L = 75K @ I_{SET} = 1.5μA
5. VCM = ±5V
6. R_L = 5kΩ @ I_{SET} = 15μA, R_L = 75K @ I_{SET} = 1.5μA
7. RS = 1kΩ, f = 100Hz.
8. V_O = ±10V
9. AV = 1, VIN = 200mV, RL = 5k, CL = 100pF.
10. V_O = ±10V, R_L = 5K @ I_{SET} = 15μA,
    R_L = 20K @ I_{SET} = 1.5μA
11. AV = ±5V.

HARRIS

HA-4156

High Performance Quad Operational Amplifier

FEATURES

- SLEW RATE 1.6 V/μs (TYP.)
- BANDWIDTH 3.5 MHz (TYP.)
- INPUT VOLTAGE NOISE (f = 1KHz) 9 NV/$\sqrt{Hz}$ (TYP.)
- INPUT OFFSET VOLTAGE 0.5 mV (TYP.)
- INPUT BIAS CURRENT 60 nA (TYP.)
- SUPPLY RANGE ±2V to ±20V
- NO CROSSOVER DISTORTION
- STANDARD QUAD PIN-OUT

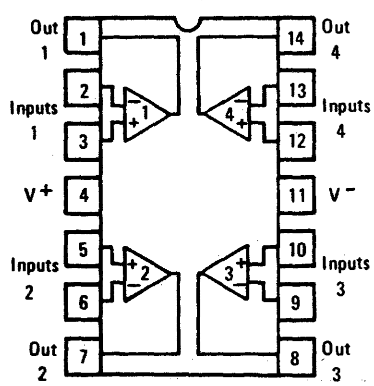
DESCRIPTION

The HA-4156 contains four general purpose operational amplifiers on a monolithic chip. The performance of each amplifier is equal to or better than the 741 type amplifier in all respects. Its superior bandwidth, slew rate and noise characteristics make it an excellent choice for active filter or audio amplifier applications.

The HA-4156-5 is guaranteed over 0°C to +75°C.

PINOUT

PIN OUT Section 11 for Packaging



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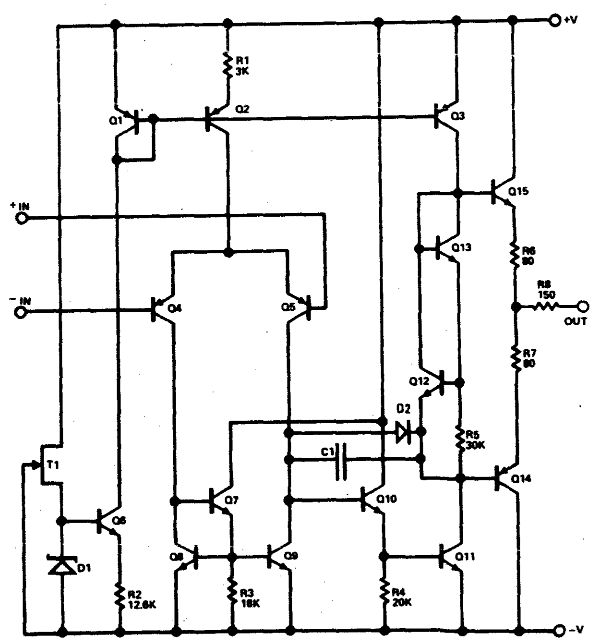


(¼) HA-4156

LINEAR

Harris Semiconductor

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C Unless Otherwise Stated		Power Dissipation (Note 3)	880mW
Voltage Between V+ and V− Terminals	40.0V	Operating Temperature Range	
Differential Input Voltage	±30.0V	HA-4156-5	$0°C \leq T_A \leq +75°C$
Input Voltage (Note 1)	±15.0V		
Output Short Circuit Duration (Note 2)	Indefinite	Storage Temperature Range	$-65°C \leq T_A \leq +150°C$

ELECTRICAL CHARACTERISTICS

V+ = 15V, V− = −15V PARAMETER	TEMP.	HA-4156-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS					
Offset Voltage	+25°C		1.0	5.0	mV
	Full		5.0	6.5	mV
Av. Offset Voltage Drift	Full		5		µV/°C
Bias Current	+25°C		60	300	nA
	Full			400	nA
Offset Current	+25°C		30	50	nA
	Full			100	nA
Common Mode Range	Full	±12			V
Differential Input Resistance	+25°C		5		MΩ
Input Noise Voltage (f = 1KHz)	+25°C		9		nV/√Hz
(f = 20Hz to 20kHz)	+25°C		1.4	2.0	µVRMS
TRANSFER CHARACTERISTICS					
Large Signal Voltage Gain (Note 4)	+25°C	25K	50K		V/V
	Full	15K			V/V
Common Mode Rejection Ratio (Note 8)	+25°C	80			dB
	Full	74			dB
Channel Separation (Note 5)	+25°C		-108		dB
Small Signal Bandwidth	+25°C	2.8	3.5		MHz
OUTPUT CHARACTERISTICS					
Output Voltage Swing (R_L = 10K)	Full	±12	±13.7		V
(R_L = 2K)	Full	±10	±12.5		V
Full Power Bandwidth (Note 4)	+25°C	20	25		KHz
Output Current (Note 6)	Full	±5	±15		mA
Output Resistance	+25°C		300		Ω
TRANSIENT RESPONSE (Note 7)					
Rise Time	+25°C		75		ns
Overshoot	+25°C		25		%
Slew Rate	+25°C	1.3	±1.6		V/µs
POWER SUPPLY CHARACTERISTICS					
Supply Current (I^+ or I^-)	+25°C			7.0	mA
Power Supply Rejection Ratio (Note 8)	Full	80			dB

NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. One amplifier may be shorted to ground indefinitely.
3. Derate 5.8mW/°C above T_A = +25°C.
4. V_{OUT} = ±10, R_L = 2K
5. Referred to input; f = 10KHz, R_S = 1K
6. V_{OUT} = ±10
7. See pulse response characteristics
8. ΔV = ±5.0V

LINEAR

Harris Semiconductor

HARRIS

HA-4600/02/05

High Performance Quad Operational Amplifier

FEATURES

- LOW OFFSET VOLTAGE 0.3mV
- HIGH SLEW RATE ±4V/μs
- WIDE BANDWIDTH 8MHz
- LOW DRIFT 2μV/°C
- FAST SETTLING (0.01%, 10V STEP) 4.2μs
- LOW POWER CONSUMPTION 35mW/AMP
- SUPPLY RANGE ±5V TO ±20V

APPLICATIONS

- HIGH Q, WIDE BAND FILTERS
- INSTRUMENTATION AMPLIFIERS
- AUDIO AMPLIFIERS
- DATA ACQUISITION SYSTEMS
- INTEGRATORS
- ABSOLUTE VALUE CIRCUITS
- TONE DETECTORS

DESCRIPTION

The HA-4600 series are high performance dielectrically isolated monolithic quad operational amplifiers with superior specifications not previously available in a quad amplifier. These amplifiers offer excellent dynamic performance coupled with low values for offset voltage and drift, input noise voltage and power consumption.

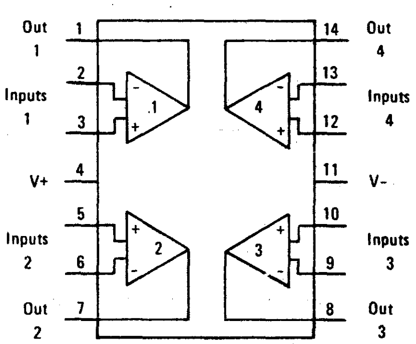
A wide range of applications can be achieved by using the features made available by the HA-4600 series. With wide bandwidth (8MHz), low power (35mW/amp), and internal compensation, these devices are ideally suited for precision active filter designs. For audio applications these amplifiers offer low noise (8nV/$\sqrt{Hz}$) and excellent full power bandwidth (60kHz). The HA-4602/4605 is particularly useful in designs requiring low offset voltage (0.3mV) and drift (2μV/°C), such as instrumentation and signal conditioning circuits. The high slew rate (4V/μs) and fast settling time (4.2μs to 0.01%, 10V step) makes these amplifiers useful compoinents in fast, accurate data acquisition systems.

The HA-4600 series are available in 14 pin CERDIP packages which are interchangeable with most other quad op amps. HA-4600/4602-2 is specified from -55°C to +125°C and HA-4600/4605-5 is specified over 0°C to +75°C range.

PINOUT

Section 11 for Packaging

TOP VIEW



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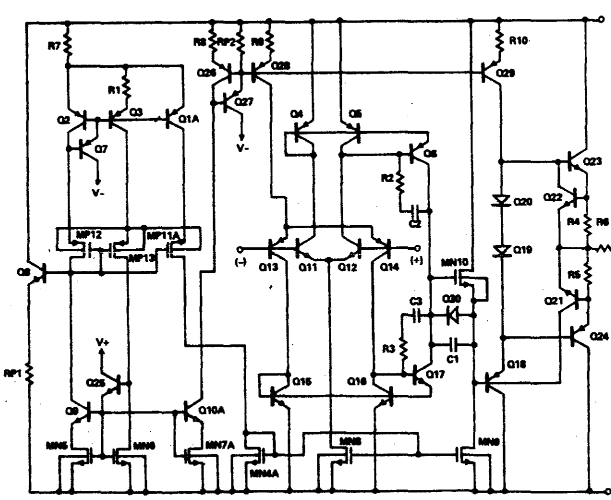


ONE FOURTH ONLY (HA-4600)

ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless Otherwise Stated		Power Dissipation (Note 4)	880mW
Voltage Between V+ and V- Terminals	40.0V	Operating Temperature Range	
Differential Input Voltage	±7V	HA-4600/4602-2	$-55°C \leq T_A \leq +125°C$
Input Voltage (Note 2)	±15.0V	HA-4600/4605-5	$0°C \leq T_A \leq +75°C$
Output Short Circuit Duration (Note 3)	Indefinite	Storage Temperature Range	$-65°C \leq T_A \leq +150°C$

ELECTRICAL CHARACTERISTICS V+ = +15V, V- = -15V

PARAMETER	TEMP	HA-4600-2 HA-4600-5 MIN	TYP	MAX	HA-4602-2 HA-4605-5 MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		0.3	2.5		3.0	9	mV
	Full			3.0			10	mV
Av. Offset Voltage Drift	Full		2			5		μV/°C
Bias Current	+25°C		130	200		200	400	nA
	Full			325			500	nA
Offset Current	+25°C		30	75		70	150	nA
	Full			125			175	nA
Common Mode Range	Full	±12			±12			V
Input Noise Voltage (f = 1kHz)	+25°C		8			8		$nV/\sqrt{Hz}$
Input Resistance			500			500		kΩ
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 5)	Full	100K	250K		75K	250K		V/V
Common Mode Rejection Ratio (Note 9)	Full	86			80			dB
Channel Separation (Note 6)	+25°C		-108			-108		dB
Small Signal Bandwidth	+25°C		8			8		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (R_L = 10K)	Full	±12	±13		±12	±13		V
(R_L = 2K)	Full	±10	±12		±10	±12		V
Full Power Bandwidth (Note 5)	+25°C		60			60		kHz
Output Current (Note 7)	Full	±10	±15		±8	±15		mA
Output Resistance	+25°C		200			200		Ω
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C		50			50		ns
Overshoot	+25°C		30			30		%
Slew Rate	+25°C	1	±4			±4		V/μs
Settling Time (Note 10)			4.2			4.2		μs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		4.6	5.5		5.0	7.5	mA
Power Supply Rejection Ratio (Note 9)	Full	86			74			dB

LINEAR

Harris Semiconductor

HARRIS

HA-4620/22/25

Wideband, High Performance Quad Operational Amplifier

FEATURES

- Wide Gain Bandwidth Product 70MHz
- High Slew Rate ±20V/μs
- Low Offset Voltage 0.3mV
- Fast Settling (0.01%, 10V Step) 2.5μs
- Total Harmonic Distortion <.01% to 30kHz
- Low Drift 2μV/°C
- Low Power Consumption 35mW/Amp
- Supply Range ±5V to ±20V

APPLICATIONS

- High Q Wide Band Filters
- Pulse Amplifiers
- Audio Amplifiers
- Data Acquisition Systems
- Absolute Value Circuits
- Video and R.F. Amplifiers

DESCRIPTION

The HA-4620 series are wide band quad operational amplifiers featuring high slew rate, wide bandwidth and fast settling time specifications complemented by low input offset voltage, low drift and input noise voltage.

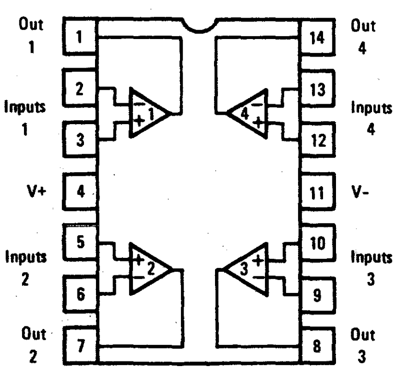
These dielectrically isolated devices are optimized to offer excellent features suitable for applications where a gain of 10 or greater is to be used. The 35mW/amp and a 70MHz gain-bandwidth-product make these monolithic amplifiers valuable components for many active filter circuits. HA-4620 series offers 0.3mW offset voltages and 2μV/°C offset voltage drift for very accurate signal conditioning designs. In high performance audio applications, these amplifiers deliver 260kHz full power bandwidth and $8nV\sqrt{Hz}$ noise voltage. For fast accurate data acquisition systems HA-4620 series offer 20Vμs slew rate and settling time of 2.5μsecs to 0.1% 10V step.

HA-4620 series are available in 14 pin CERDIP packages and are interchangeable with most other quad op amps. HA-4625 is also available in chip form. HA-4620/4622-2 is specified from -55°C to +125°C and HA-4620/4625-5 is specified over 0°C to +75°C range.

PINOUT

Section 11 for Packaging

TOP VIEW



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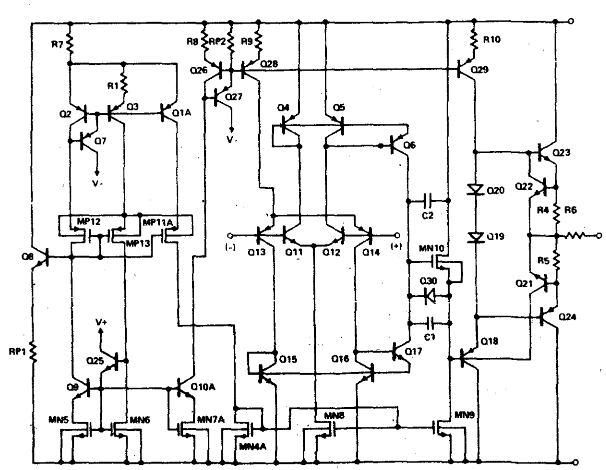


ONE FOURTH ONLY (HA-4620)

ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless otherwise stated.		Power Dissipation (Note 4)	880mW
Voltage between V+ and V- Terminals	40.0V	Operating Temperature Range	
Differential Input Voltage	±7V	HA-4620/4622-2	$-55°C \leq T_A \leq +125°C$
Input Voltage (Note 2)	±15.0V	HA-4620/4625-5	$0°C \leq T_A \leq +75°C$
Output Short Circuit Duration (Note 3)	Indefinite	Storage Temperature Range	$-65°C \leq T_A \leq +150°C$

ELECTRICAL CHARACTERISTICS

		HA-4620-2 HA-4620-5			HA-4622-2 HA-4625-5			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		0.3	2.5		3.0	9	mV
	Full			3.0			10	mV
Av. Offset Voltage Drift	Full		2			5		μV/°C
Bias Current	+25°C		130	200		200	400	nA
	Full			325			500	nA
Offset Current	+25°C		30	75		70	150	nA
	Full			125			175	nA
Common Mode Range	Full	±12			±12			V
Input Noise Voltage (f = 1kHz)	+25°C		8			8		$nV/\sqrt{Hz}$
Input Resistance	+25°C		500			500		kΩ
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 5)	Full	100K	250K		75K	250K		V/V
Common Mode Rejection Ratio (Note 6)	Full	86			80			dB
Channel Separation (Note 7)	+25°C		-108			-108		dB
Gain Bandwidth Products (Note 8)	+25°C		70			70		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (R_L = 10K)	Full	±12	±13		±12	±13		V
(R_L = 2K)	Full	±10	±12		±10	±12		V
Full Power Bandwidth (Note 9)	+25°C		260			260		kHz
Output Current (Note 7)	Full	±10	±15		±8	±15		mA
Output Resistance	+25°C		200			200		Ω
TRANSIENT RESPONSE (Note 11)								
Rise Time	+25°C		38	60		38		ns
Overshoot	+25°C		45	60		45		%
Slew Rate	+25°C	±12	±20		±12	±20		V/μs
Settling Time (Note 10)			2.5			2.5		μs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		4.6	5.5		5.0	7.5	mA
Power Supply Rejection Ratio (Note 9)	Full	86			74			dB

HARRIS

HA-4741

Quad Operational Amplifier

LINEAR

Harris Semiconductor

FEATURES

- SLEW RATE 1.6V/μs (TYP.)
- BANDWIDTH 3.5MHz (TYP.)
- INPUT VOLTAGE NOISE 9nV√Hz (TYP.)
- INPUT OFFSET VOLTAGE 0.5mV (TYP.)
- INPUT BIAS CURRENT 60nA (TYP.)
- SUPPLY RANGE ±2V TO ±20V
- NO CROSSOVER DISTORTION
- STANDARD QUAD PIN-OUT

APPLICATIONS

- UNIVERSAL ACTIVE FILTERS
- D3 COMMUNICATIONS FILTERS
- AUDIO AMPLIFIERS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

The HA-4741, which contains four amplifiers on a monolithic chip, provides a new measure of performance for general purpose operational amplifiers. Each amplifier in the HA-4741 has operating specifications that equal or exceed those of the 741-type amplifier in all categories of performance.

HA-4741 is well suited to applications requiring accurate signal processing by virtue of its low values of input offset voltage (0.5mV), input bias current (60nA) and input voltage noise (9nV/ √Hz at 1kHz). 3.5MHz bandwidth, coupled with high open-loop gain, allow the HA-4741 to be used in designs requiring amplification of wide band signals, such as audio amplifiers. Audio application is further enhanced by the HA-4741's negligible output crossover distortion. These excellent dynamic characteristics also make the HA-4741 ideal for a wide range of active filter designs. Performance integrity of multi-channel designs is assured by a high level of amplifier-to-amplifier isolation (108dB at 1kHz).

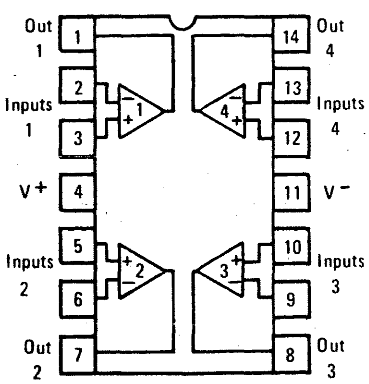
A wide range of supply voltages (±2V to ±20V) can be used to power the HA-4741, making it compatible with almost any system including battery-powered equipment.

The HA-4741 has guaranteed operation over -55°C to +125°C and can be furnished to meet MIL-STD-883 (HA-4741-8). The HA-4741-5 is guaranteed over 0°C to +75°C and is available in ceramic and plastic dual-in-line packages and in dice form.

PINOUT

Section 11 for Packaging

TOP VIEW



QUAD OP AMP

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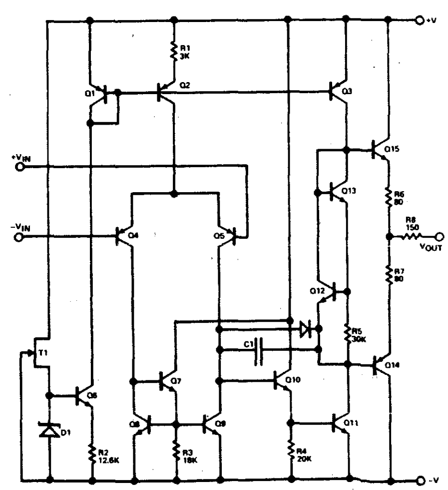


(¼) HA-4741

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V− Terminals	40.0V
Differential Input Voltage	±30.0V
Input Voltage (Note 1)	±15.0V
Output Short Circuit Duration (Note 2)	Indefinite
Power Dissipation For Epoxy Package. (Note 3)	880mW
Operating Temperature Range	
HA-4741-2	$-55°C \leq T_A \leq +125°C$
HA-4741-5	$0°C \leq T_A \leq +75°C$
Storage Temperature Range	$-65°C \leq T_A \leq +150°C$

ELECTRICAL CHARACTERISTICS

V+ = 15V, V− = −15V		HA-4741-2 −55°C to +125°C			HA-4741-5 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		0.5	3.0		1.0	5.0	mV
	Full		4.0	5.0		5.0	6.5	mV
Av. Offset Voltage Drift	Full		5			5		μV/°C
Bias Current	+25°C		60	200		60	300	nA
	Full			325			400	nA
Offset Current	+25°C		15	30		30	50	nA
	Full			75			100	nA
Common Mode Range	Full	±12			±12			V
Differential Input Resistance	+25°C		5			5		MΩ
Input Noise Voltage (f = 1KHz)	+25°C		9			9		$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 4)	+25°C	50K	100K		25K	50K		V/V
	Full	25K			15K			V/V
Common Mode Rejection Ratio (Note 8)	+25°C	80			80			dB
	Full	74			74			dB
Channel Separation (Note 5)	+25°C	90	−108		90	−108		dB
Small Signal Bandwidth	+25°C	2.5	3.5		2.5	3.5		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (R_L = 10K)	Full	±12	±13.7		±12	±13.7		V
(R_L = 2K)	Full	±10	±12.5		±10	±12.5		V
Full Power Bandwidth (Notes 4 & 9)	+25°C	14	25		14	25		kHz
Output Current (Note 6)	Full	±5	±15		±5	±15		mA
Output Resistance	+25°C		300			300		Ω
TRANSIENT RESPONSE (Notes 7 & 10)								
Rise Time (Note 11)	+25°C		75	140		75	140	ns
Overshoot (Note 11)	+25°C		25	40		25	40	%
Slew Rate (Note 12)	+25°C		±1.6			±1.6		V/μs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C			5.0			7.0	mA
Power Supply Rejection Ratio (Note 8)	Full	80			80			dB

NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. One amplifier may be shorted to ground indefinitely.
3. Derate 5.8mW/°C above T_A = +25°C.
4. V_{OUT} = ±10, R_L = 2K
5. Referred to input; f = 10KHz, R_S = 1K
6. V_{OUT} = ±10
7. See pulse response characteristics
8. ΔV = ±5.0V
9. Full power bandwidth guaranteed based upon slew rate measurement FPBW = S.R./2πVpeak
10. R_L = 2K, C_L = 50pf.
11. V_{OUT} = ±200mV
12. V_{OUT} = ±5V

HARRIS

HA-5062 Series

Low Power JFET Input Dual Operational Amplifiers

Preliminary

FEATURES

- HIGH INPUT IMPEDANCE $10^{12}\Omega$
- LOW INPUT BIAS CURRENT 200pA
- LOW INPUT OFFSET CURRENT 100pA
- VERY LOW POWER CONSUMPTION
  TYPICAL SUPPLY CURRENT 200μA
- INTERNAL FREQUENCY COMPENSATION
- HIGH SLEW RATE 4V/μs
- PIN COMPATIBLE WITH LM1458
- DIRECT REPLACEMENT FOR TL062

APPLICATIONS

- ACTIVE FILTERS
- INSTRUMENTATION AMPLIFIERS
- AUDIO AMPLIFIERS
- BATTERY OPERATED EQUIPMENT
- SIGNAL CONDITIONING

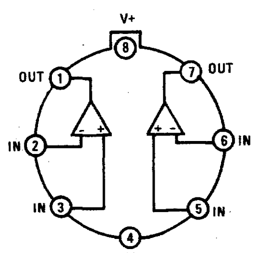
DESCRIPTION

The HARRIS HA-5062 operational amplifiers are a series of dual monolithic JFET-input amplifiers featuring low input bias and offset currents, high input impedence and very low power operation. In addition to being a direct replacement for the TL062 series, the HA-5062 series offers improved performance with a minimum open loop gain 20K V/V and a slew rate of 4v/μs.

This improved performance is a result of the HARRIS FET/Bipolar technology and makes the HA-5062 series of amplifiers ideally suited for applications in industrial control, communication, and battery powered instrumentation equipment.

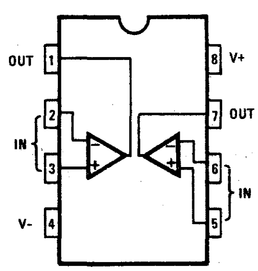
The HA-5062-2 is characterized for operation over the full military temperature range of -55°C to +125°C. The HA-5062A-5, HA-5062B-5 and HA-5062-5 are all characterized over the commercial temperature range of 0°C to +75°C.

PINOUT

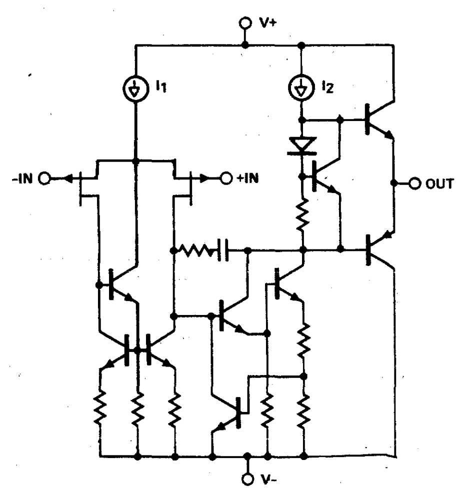


NOTE: Case Connected to V-

TOP VIEWS



SIMPLIFIED SCHEMATIC



(ONE HALF ONLY)

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V- Terminals	± 20V
Differential Input Voltage	± 40V
Input Voltage (Note 2)	±15.0V
Output Short Circuit Duration	Indefinite
Power Dissipation	600mW*
Operating Temperature Range:	
HA-5062-2	$-55^{o}C \leq T_A \leq +125^{o}C$
HA-5062-5	$0^{o}C \leq T_A \leq +75^{o}C$
Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

* To-99 Derate by 6.75mW/°C above +85°C
Dip Derate by 5.57mW/°C above +65°C

ELECTRICAL CHARACTERISTICS

V+ = 15V V- = 15V

Parameters are guaranteed at indicated ambient temperature after warm-up.

PARAMETER	TEMP.	HA-5062-2 -55°C to +125°C MIN.	TYP.	MAX.	HA-5062A-5 0°C to 75°C MIN.	TYP.	MAX.	HA-5062B-5 0°C to 75°C MIN.	TYP.	MAX.	HA-5062-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS														
Offset Voltage (Note 3)	+25°C		3	6		3	6		2	3		3	15	mV
	Full			9			7.5			5			20	mV
Av. Offset Voltage Drift	Full		10			10			10			10		μV/°C
Bias Current	+25°C		30	200		30	200		30	200		30	400	pA
	Full			50			7			7			10	nA
Offset Current	+25°C		5	100		5	100		5	100		5	200	pA
	Full			20			3			3			5	nA
Common Mode Range	Full	±10	±12		±10	±12		±10	±12		±10	±12		V
Input Resistance	+25°C		10^{12}			10^{12}			10^{12}			10^{12}		MΩ
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Note 4)	+25°C	20K	25K		20K	25K		20K	25K		10K	25K		V/V
	Full	10K			15K			15K			5K			V/V
Common Mode Rejection Ratio (Note 5)	Full	80	86		80	86		80	86		70	76		dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 6)	+25°C	±10	±12		±10	±12		±10	±12		±10	±12		V
	Full	±10			±10			±10			±10			V
Unity Gain Bandwidth (Note 6)	+25°C		1			1			1			1		MHz
Full Power Bandwidth (Note 7)	+25°C		63			63			63			63		KHz
TRANSIENT RESPONSE														
Rise Time (Note 8)	+25°C		80			80			80			80		nsec
Overshoot (Note 8)	+25°C		10			10			10			10		%
Slew Rate (Note 9)	+25°C		4			4			4			4		V/μs
Settling Time (Note 10)	+25°C		3.5			3.5			3.5			3.5		μsec
POWER SUPPLY CHARACTERISTICS														
Supply Current (Note 11)	+25°C			0.4			0.4			0.4			0.5	mA
Power Supply Rejection Ratio (Note 12)	Full	80	95		80	95		80	95		70	95		dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. $R_S = 50\Omega$.
4. $R_L \geq 10K\Omega$, $V0 = \pm 10V$.
5. $\Delta V_{IN} = \pm 10V$.
6. $R_L = 10K\Omega$.
7. $R_L = 10K$; Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{SLEW RATE}}{2 \pi V_{PEAK}}$.
8. $V_{IN} = 50mV$, $C_L = 50pF$, $R_L = 10K\Omega$.
9. $V_{IN} = 10V$, $C_L = 50pF$, $R_L = 10K\Omega$.
10. Settling time is measured to 0.1% of final value for a 10 volt output step and $A_V = -1$.
11. No load, No signal.
12. $V_{SUPP} = \pm 5V.D.C.$ to ± 15 V.D.C.

HARRIS

HA-5064 Series

Low Power, JFET Input Quad Operational Amplifiers

JULY 1982

Preliminary

FEATURES

- LOW INPUT BIAS CURRENT 100pA
- LOW POWER DISSIPATION 24mW/Pkg.
- FAST SLEWING 4V/μs
- LOW VIO DRIFT 10μV/^{o}C
- HIGH INPUT IMPEDANCE $10^{12}\Omega$
- GOOD CHANNEL SEPARATION 120dB
- POWER SUPPLY RANGE ±5V TO ±20V

APPLICATIONS

WHERE DENSITY AND POWER REQUIREMENTS ARE DEMANDING:

- ACTIVE FILTERS
- SIGNAL CONDITIONING
- SIGNAL GENERATION
- INSTRUMENTATION AMPLIFIERS

DESCRIPTION

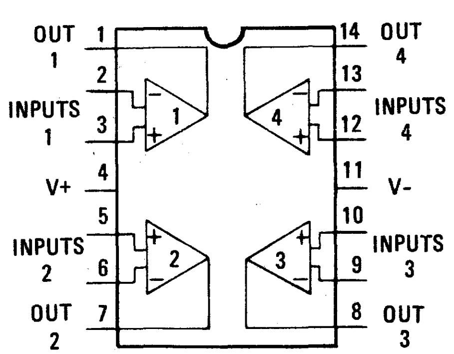
The HARRIS HA-5064 series JFET input monolithic, quad operational amplifiers feature very low power requirements coupled with excellent AC and DC characteristics. Maximum power dissipation of 24 mW/package is achieved by using complementary design, process, and layout techniques.

A 4V/μs slew rate coupled with 1MHz gain-bandwidth makes these devices most suitable for active filter and signal conditioning designs. The HA-5064 series is ideally suited for those applications demanding low power and high density without compromising other performance characteristics. High input impedance and low drift also makes the HA-5064 series useful as instrumentation amplifiers.

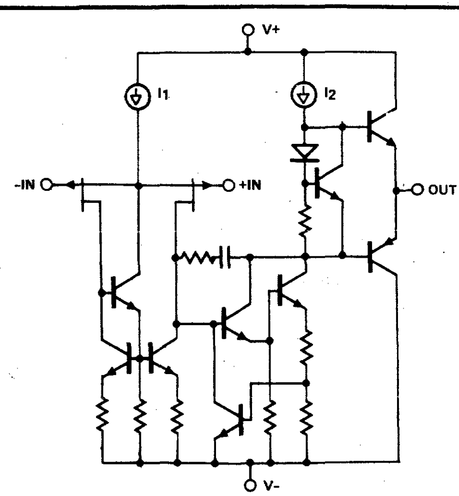
The HA-5064 is packaged in a 14-pin DIP and is pin compatible with most other quad operational amplifiers. The HA-5064-2 is specified for -55^{o}C to +125^{o}C operation while the HA-5064 A-5/HA-5064B-5/HA-5064-5 are specified over the 0^{o}C to +75^{o}C range.

PINOUT

TOP VIEW



SIMPLIFIED SCHEMATIC



ONE-FOURTH ONLY

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V-	40V
Differential Input Voltage (Note 2)	±30V
Output Current (Note 3)	Continuous
Internal Power Dissipation (Note 4)	500mW
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS

V+ = 15VDC; V- = -15VDC

PARAMETER	TEMP	HA-5064-2 -55°C to +125°C MIN	TYP	MAX	HA-5064A-5 0°C to +75°C MIN	TYP	MAX	HA-5064B-5 0°C to +75°C MIN	TYP	MAX	HA-5064-5 0°C to +75°C MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS														
Offset Voltage	+25°C		2	6		2	6		2	3			15	mV
	Full			9			7.5			5			20	mV
Offset Voltage Average Drift	Full		10			10			10			20		µV/°C
Bias Current	+25°C			200			200			200			400	pA
	Full			50			7			7			10	nA
Offset Current	+25°C			100			100			100			200	pA
	Full			20			3			3			5	nA
Input Resistance	+25°C		10^{12}			10^{12}			10^{12}			10^{12}		Ω
Common Mode Range	Full	±10			±10			±10			±10			V
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Note 5)	+25°C	20K	25K		20K	25K		20K	25K		10K	25K		V/V
	Full	10K			15K			15K			5K			V/V
Common Mode Rejection Ratio (Note 6)	Full	80			80			80			70			dB
Gain Bandwidth	+25°C		1			1			1			1		MHz
Channel Separation (Note 7)	+25°C		120			120			120			120		dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 8)	+25°C	±10	±12		±10	±12		±10	±12		±10	±12		V
	Full	±10			±10			±10			±10			V
Output Current (Note 9)	Full	±1			±1			±1			±1			mA
Full Power Bandwidth (Note 10)	+25°C		63			63			63			63		kHz
Output Resistance (Note 11)	+25°C		300			300			300			300		Ω
TRANSIENT RESPONSE (Note 12)														
Rise Time (10% TO 90%)	+25°C		80			80			80			80		nsec
Slew Rate	+25°C	2	4		2	4		2	4		2	4		V/µsec
Settling Time (Note 13)	+25°C		3.5			3.5			3.5			3.5		µsec
POWER SUPPLY CHARACTERISTICS														
Supply Current	+25°C			.8			.8			.8			1	mA
P. S. R. R. (Note 14)	Full	80			80			80			70			dB

LINEAR

Harris Semiconductor

HARRIS

HA-5082 Series

JFET Input Dual Operational Amplifiers

Preliminary

FEATURES

- HIGH INPUT IMPEDANCE $10^{12}\Omega$
- LOW INPUT BIAS CURRENT 200pA
- LOW INPUT OFFSET CURRENT 100pA
- LOW POWER CONSUMPTION TYPICAL SUPPLY CURRENT 3.5mA
- HIGH SLEW RATE 15V/μs
- PIN COMPATIBLE WITH LM1458
- DIRECT REPLACEMENT FOR TL082

APPLICATIONS

- ACTIVE FILTERS
- INSTRUMENTATION AMPLIFIERS
- AUDIO AMPLIFIERS
- SIGNAL CONDITIONING

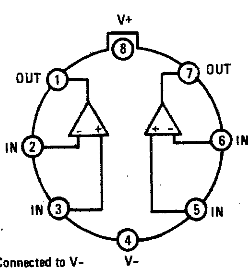
DESCRIPTION

The HARRIS HA-5082 operational amplifiers are a series of dual monolithic JFET-input amplifiers featuring low input bias and offset currents, high input impedance and, high slew rate. In addition to being a direct replacement for the TL082 series, the HA-5082 series offers improved performance with an input offset voltage of 2mV, a slew rate of 15V/μs, and bandwidths of 4MHz.

This improved performance is a result of the HARRIS FET/Bipolar technology and makes the HA-5082 series of amplifiers ideally suited for applications in industrial control, communication, and computer peripheral equipment.

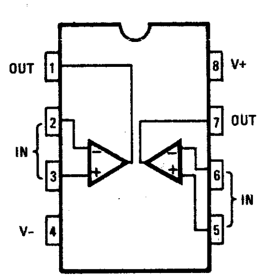
The HA-5082-2 is characterized for operation over the full military temperature range of -55°C to +125°C. The HA-5082A-5, HA-5082B-5 and HA-5082-5 are all characterized over the commercial temperature range of 0°C to +75°C.

PINOUT

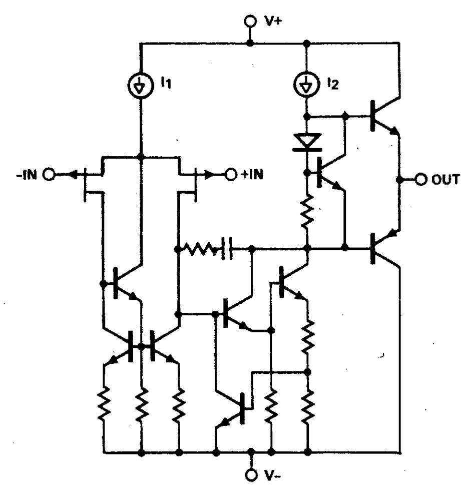


NOTE: Case Connected to V-

TOP VIEWS



SIMPLIFIED SCHEMATIC



(ONE HALF ONLY)

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V- Terminals	±20V
Differential Input Voltage	±40V
Input Voltage (Note 2)	±15.0V
Output Short Circuit Duration	Indefinite

Power Dissipation	600mW*
Operating Temperature Range:	
HA-5082-2	$-55^oC \le T_A \le +125^oC$
HA-5082-5	$0^oC \le T_A \le +75^oC$
Storage Temperature Range	$-65^oC \le T_A \le +150^oC$

* To-99 Derate by 6.75mW/°C above +85°C
Dip Derate by 5.57mW/°C above +65°C

ELECTRICAL CHARACTERISTICS

V+ = 15V V- = -15V
Parameters are guaranteed at indicated ambient temperature after warm-up.

PARAMETER	TEMP.	HA-5082-2 -55°C to +125°C MIN.	TYP.	MAX.	HA-5082A-5 0°C to 75°C MIN.	TYP.	MAX.	HA-5082B-5 0°C to 75°C MIN.	TYP.	MAX.	HA-5082-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS														
Offset Voltage (Note 3)	+25°C		3	5		3	5			2		5	15	mV
	Full			8			7			4			20	mV
Av. Offset Voltage Drift	Full		10			10			10			10		µV/°C
Bias Current	+25°C		30	200		30	200		30	200		30	400	pA
	Full			50			8			4			10	nA
Offset Current	+25°C		5	100		5	100		5	100		5	200	pA
	Full			20			4			2			5	nA
Common Mode Range	Full	±10	±12		±10	±12		±10	±12		±10	±12		V
Input Resistance	+25°C		10^{12}			10^{12}				10^{12}		10^{12}		MΩ
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Note 4)	+25°C	50K	200K		50K	200K		50K	200K		25K	200K		V/V
	Full	15K			25K			25K			15K			V/V
Common Mode Rejection Ratio (Note 5)	+25°C	80	86		80	86		80	86		70	76		dB
Unity Gain Bandwidth	+25°C		4			4			4			4		MHz
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 6)	+25°C	±10	±12		±10	±12		±10	±12		±10	±12		V
	Full	±10			±10			±10			±10			V
Output Current (Note 7)	Full	±5			±5			±5			±5			mA
Full Power Bandwidth (Note 8)	+25°C		240			240			240			240		KHz
TRANSIENT RESPONSE														
Rise Time (Note 9)	+25°C		60			60			60			60		nsec
Overshoot (Note 9)	+25°C		10			10			10			10		%
Slew Rate (Note 10)	+25°C		15			15			15			15		V/µs
Settling Time (Note 11)	+25°C		2			2			2			2		µsec
POWER SUPPLY CHARACTERISTICS														
Supply Current (Note 12)	+25°C		3.5	5.6		3.5	5.6		3.5	5.6		3.5	5.6	mA
Power Supply Rejection Ratio (Note 13)	+25°C	80	86		80	86		80	86		70	76		dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. $R_S = 50\Omega$.
4. $R_L \geq 2K\Omega$, $V_O = \pm 10V$.
5. $\Delta V_{IN} = \pm 10V$.
6. $R_L = 2K\Omega$.
7. $V_{OUT} = \pm 10V$
8. $R_L = 2K$; Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$
9. $V_{IN} = 50mV$, $C_L = 100pF$, $R_L = 2K\Omega$.
10. $V_{IN} = 10V$, $C_L = 100pF$, $R_L = 2K\Omega$.
11. Settling time is measured to 0.1% of final value for a 10 volt output step and $A_V = -1$.
12. No load, No signal.
13. $V_{SUPP} = \pm 5V.D.C.$ to $\pm 15\ V.D.C.$

LINEAR

Harris Semiconductor

HARRIS

HA-5084 Series

JFET Input Quad Operational Amplifiers

Preliminary

FEATURES

- LOW INPUT BIAS CURRENT 200pA
- HIGH SLEW RATE 15V/μs
- WIDE BANDWIDTH 4MHz
- LOW DRIFT 10μV/°C
- HIGH INPUT IMPEDANCE $10^{12}\Omega$
- LOW SUPPLY CURRENT 7.2mA
- SUPPLY RANGE ±5V TO ±20V

APPLICATIONS

- HIGH Q, WIDEBAND FILTERS
- INTEGRATORS
- TONE DETECTORS
- SAMPLE/HOLD CIRCUITS
- DATA ACQUISITION SYSTEMS
- ABSOLUTE VALUE CIRCUITS

DESCRIPTION

The Harris HA-5084 is a JFET input, monolithic, quad operational amplifier featuring low input bias and offset currents, high input impedance, and high slew rate. Manufactured using FET/Bipolar technology coupled with advanced layout considerations, these devices also feature excellent channel separation and offset voltage drift specifications.

High slew rate (15V/ μs) coupled with excellent input bias (30pA) and offset current (3pA) make the HA-5084 ideally suited for high speed analog designs such as integrators, fast D/A converters, and sample-and-hold circuits.

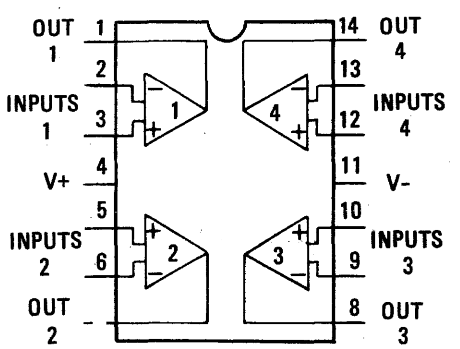
The HA-5084 is available in ceramic and plastic 14 pin DIP's and is pin compatible with the LM324, LM348, and MC3403 quad operational amplifier pinout.

The HA-5084-2 is specified from -55°C to +125°C while the HA-5084-5 operates from 0°C to +75°C.

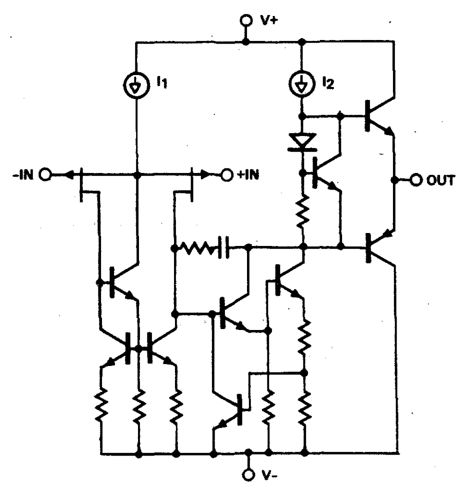
PINOUT

Section 11 for Packaging

TOP VIEW



SIMPLIFIED SCHEMATIC



(ONE FOURTH ONLY)

LINEAR

Harris Semiconductor

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V-	40V
Differential Input Voltage (Note 2)	±40V
Output Current (Note 3)	Full Short Circuit Protection
Internal Power Dissipation (Note 4)	500mW
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS

V+ = 15VDC; V- = -15VDC

		HA-5084-2 -55°C to +125°C			HA-5084A-5 0°C to +75°C			HA-5084B-5 0°C to +75°C			HA-5084-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS														
Offset Voltage	+25°C			5			5			2			15	mV
	Full			8			7			4			20	mV
Offset Voltage Average Drift	Full		8.3			8.3			8.3			8.3		µV/°C
Bias Current	+25°C			200			200			200			400	pA
	Full			50			8			4			10	nA
Offset Current	+25°C			100			100			100			200	pA
	Full			20			4			2			5	nA
Input Resistance	+25°C		10^{12}			10^{12}			10^{12}			10^{12}		Ω
Common Mode Range	Full	±10			±10			±10			±10			V
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Note 5)	+25°C	25K			50K			50K			25K			V/V
	Full	15K			25K			25K			15K			V/V
Common Mode Rejection Ration (Note 6)	Full	70			80			80			70			dB
Unity Gain Bandwidth	+25°C		4			4			4			4		MHz
Channel Separation (Note 7)			-120			-120			-120			-120		dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note8)	+25°C	10			10			10			10			V
	Full	10			10			10			10			V
Output Current (Note 9)	Full	±5			±5			±5			±5			mA
Full Power Bandwidth (Note 10)	+25°C		240			240			240			240		kHz
Output Resistance (Note 11)	+25°C		300			300			300			300		Ω
TRANSIENT RESPONSE (Note 12)														
Rise Time	+25°C		60			60			60			60		nsec
Slew Rate	+25°C		15			15			15			15		V/µsec
Settling Time (Note 13)	+25°C		2			2			2			2		µsec
POWER SUPPLY CHARACTERISTICS														
Supply Current	+25°C		7.2	11		7.2	11		7.2	11		7.2	12	mA
P. S. R. R. (Note 14)	Full	80			80			80			70			dB

HARRIS

HA-5100/5105

Wideband, JFET Input Operational Amplifier

FEATURES

- LOW INPUT OFFSET VOLTAGE 0.5mV
- LOW OFFSET DRIFT . . . . $5\mu V/^oC$
- LOW INPUT BIAS CURRENT 50pA
- LARGE VOLTAGE GAIN . . . . 150K V/V
- WIDE BANDWIDTH 18MHz
- HIGH SLEW RATE . . . . $8V/\mu sec$
- FAST LARGE SIGNAL SETTLING TIME: $1.7\mu sec$

APPLICATIONS

- PRECISION, HIGH SPEED, DATA ACQUISITION SYSTEMS
- PRECISION SIGNAL GENERATION
- PULSE AMPLIFICATION

GENERAL DESCRIPTION

The HA-5100/5105 are monolithic wideband operational amplifiers manufactured with FET/Bipolar technologies and dielectric isolation. Precision laser trimming of the input stage complements the amplifier high frequency capabilities with excellent input characteristics.

The HA-5100/5105 offer a number of important advantages over similar FET input op amps from other manufacturers. In addition to superior bandwidth and settling characteristics the Harris devices have quite constant slew rate, bandwidth, and settling characteristics over the operating range. This provides the user predictable performance in applications where settling time, full power bandwidth, closed loop bandwidth, or phase shift is critical. The slewing waveform is symmetrical to provide reduced distortion. Note also that Harris specifies all parameters at ambient (rather than junction) temperature to provide the designer meaningful data to predict actual operating performance.

Complementing HA-5100/5105's predictable and excellent dynamic characteristics are very low input offset voltage, very low input bias current, and extremely high input impedance. This ideal combination of features make these amplifiers most suitable for precision, high speed, data acquisition system designs and for a wide variety of signal conditioning applications.*

* -2 denotes a range of -55^oC to $+125^oC$ and -5 denotes a 0^oC to $+75^oC$ range.

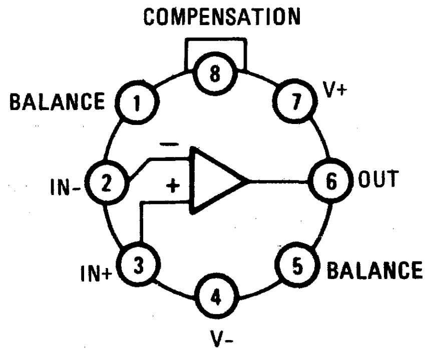
LINEAR

Harris Semiconductor

PINOUT

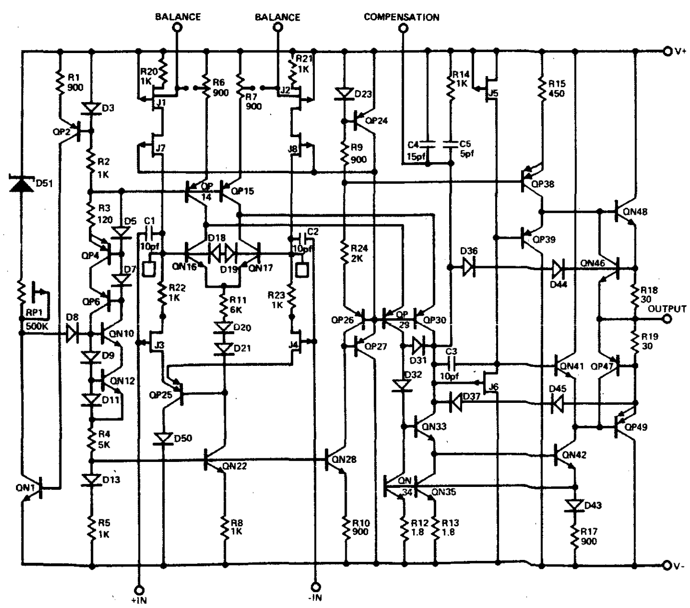
Section 11 for Packaging

TOP VIEW



CASE CONNECTED TO V-

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V-	40V
Differential Input Voltage	±40V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation (Note 2)	510mW
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS

PARAMETER	TEMP	HA-5100-2 -55°C to +125°C MIN	TYP	MAX	HA-5100-5 0°C to +75°C MIN	TYP	MAX	HA-5105-5 0°C to +75°C MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		0.5	1.0		0.5	1.0		0.5	1.5	mV
	Full		0.50	2.0		0.50	2.0		0.75	3.5	mV
Offset Voltage Average Drift	Full		5			10			15		µV/°C
Bias Current	+25°C		20	50		20	50		50	100	pA
	Full		5	10			10		10	20	nA
Offset Current	+25°C		2	10		2	10		5	50	pA
	Full		2	5		2	5		5	10	nA
Input Resistance	+25°C		10^{12}			10^{12}			10^{12}		Ω
Common Mode Range	Full	±10	±11		±10	±11		±10	±10.5		V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 3)	+25°C	75K	150K		75K	150K		50K	100K		V/V
	Full	60K	100K		60K	100K		40K	80K		V/V
Common Mode Rejection Ratio (Note 4)	Full	80	86		80	86		80	86		dB
Gain Bandwidth Product at A_V = 10	Full		18			18			18		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 5)	+25°C	±12	±13		±12	±13		±11	±12		V
	Full	±12	±13		±12	±13		±11	±12		V
Short Circuit Output Current (Note 6)	Full	±10	±15		±10	±15		±8	±15		mA
Full Power Bandwidth (Note 7)	+25°C	90	150		90	150		75	125		kHz
Output Resistance (Note 8)	+25°C		30			30			40		Ω
TRANSIENT RESPONSE (Note 9)											
Rise Time	+25°C		15	35		15	35		20		nsec
Slew Rate	+25°C	6	8		6	8		5	8		V/µsec
Settling Time (Note 10)	+25°C		1.7			1.7			2.0		µsec
POWER SUPPLY CHARACTERISTICS											
Supply Current	Full		5	7		5	7		6	8	mA
P.S.R.R. (Note 11)	Full	80	86		80	86		80	86		dB

HARRIS

HA-5110/5115

Wideband, JFET Input, Uncompensated, Operational Amplifier

FEATURES

- WIDE GAIN BANDWIDTH 60MHz
- HIGH SLEW RATE 50V/μs
- SETTLING TIME 850ns
- POWER BANDWIDTH 800KHz
- OFFSET VOLTAGE 0.5mV
- BIAS CURRENT 50pA

APPLICATIONS

- VIDEO AND RF AMPLIFIERS
- DATA ACQUISITION
- PULSE AMPLIFIERS
- PRECISION SIGNAL GENERATION

DESCRIPTION

HA-5110/5115 are wideband, uncompensated, operational amplifiers manufactured with FET/Bipolar technologies and dielectric isolation. These monolithic amplifiers feature superior high frequency capabilities further enhanced by precision laser trimming of the input stage to provide excellent input characteristics. These devices are controlled at closed loop gains greater than 10 without compensation.

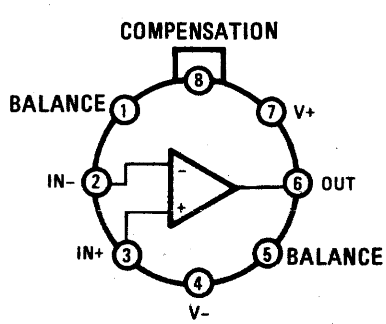
With excellent dynamic and input characteristics, HA-5110/5115 are well suited for many wideband, pulse, and video applications. These amplifiers are ideal components for video and RF circuitry requiring up to 60MHz gain-bandwidth-product and 800KHz power bandwidth. 50V/μs slew rate and 850ns settling time make these devices useful in pulse amplification and data acquisition designs. HA-5110/5115's 0.5mV offset voltage, 10pA offset current, and extremely high impedance coupled with excellent AC parameters make these amplifiers ideal selections for accurate signal conditioning designs. For applications requiring less critical input characteristics, HA-5115 is available in untrimmed form.

HA-5110/5115 are available in metal can (TO-99) packages. Suffix -2 denotes a range to -55°C to +125°C and -5 denotes a 0°C to +75°C range.

PINOUT

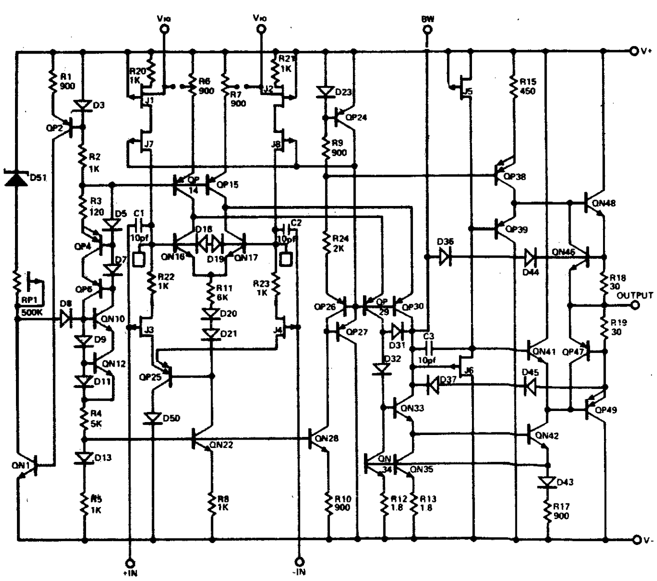
Section 11 for Packaging

TOP VIEW



CASE CONNECTED TO V-

SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^-	40V	Internal Power Dissipation (Note 2)	510mW
Differential Input Voltage	±40V	Storage Temperature Range	-65°C to +150°C
Peak Output Current	Full Short Circuit Protection		

ELECTRICAL CHARACTERISTICS

V+ = 15VDC; V- = -15VDC
Parameters are guaranteed at indicated ambient temperature after warm-up.

PARAMETER	TEMP	HA-5110-2 -55°C to +125°C MIN	TYP	MAX	HA-5110-5 0°C to +75°C MIN	TYP	MAX	HA-5115-5 0°C to +75°C MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		0.5	1.0		0.5	1.0		0.5	1.5	mV
	Full		0.50	2.0		0.50	2.0		0.75	3.5	mV
Offset Voltage Average Drift	Full		5			10			15		μV/°C
Bias Current	+25°C		20	50		20	50		50	100	pA
	Full		5	10			10		10	20	nA
Offset Current	+25°C		2	10		2	10		5	50	pA
	Full		2	5		2	5		5	10	nA
Input Resistance	+25°C		10^{12}			10^{12}			10^{12}		Ω
Common Mode Range	Full	±10	±11		±10	±11		±10	±10.5		V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 3)	+25°C	75K	150K		75K	150K		50K	100K		V/V
	Full	60K	100K		60K	100K		40K	80K		V/V
Common Mode Rejection Ratio (Note 4)	Full	80	86		80	86		80	86		dB
Gain Bandwidth Product (A_V = 10)	Full		60			60			50		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 5)	+25°C	±12	±13		±12	±13		±11	±12		V
	Full	±12	±13		±12	±13		±11	±12		V
Output Current (Note 6)	+25°C	±10	±15		±10	±15		±8	±15		mA
Full Power Bandwidth (Note 7)	+25°C	550	625		550	625		550	625		kHz
Output Resistance (Note 8)	+25°C		30			30			40		Ω
TRANSIENT RESPONSE (Note 9)											
Rise Time (A_V = 10)	+25°C		20			20			20		nsec
Slew Rate (A_V = 10)	+25°C	35	50		35	50		35	40		V/μsec
Settling Time (Note 10)	+25°C		.85			.85			1.0		μsec
POWER SUPPLY CHARACTERISTICS											
Supply Current	Full		5	7		5	7		6	8	mA
Power Supply Rejection Ratio (Note 11)	+25°C	80	94		80	94		80	94		dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8mW/°C for operation at ambient temperatures above +75°C.
3. V_{OUT} = ±10V. R_L = 2K
4. V_{CM} = ±10 V.D.C.
5. R_L = 10K
6. V_{OUT} = 0V
7. R_L = 2K; Full power bandwidth guaranteed, based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$
8. Output resistance measured under open loop conditions.
9. Refer to Test Circuits section of the data sheet.
10. Settling Time is measured to 0.1% of final value for a 10 volt output step and A_V = -10.
11. V_{SUPP} = ±10 V.D.C. to ±20 V.D.C.

HARRIS

HA-5130/5135

Precision Operational Amplifier

FEATURES

- LOW OFFSET VOLTAGE 25μV
- LOW OFFSET VOLTAGE DRIFT 0.4μV/°C
- LOW NOISE 9nV/$\sqrt{Hz}$
- OPEN LOOP GAIN 10^7
- BANDWIDTH (UNITY GAIN) 2.5MHz
- ALL BIPOLAR CONSTRUCTION

APPLICATIONS

- HIGH GAIN INSTRUMENTATION
- PRECISION DATA ACQUISITION
- PRECISION INTEGRATORS
- BIOMEDICAL AMPLIFIERS
- PRECISION THRESHOLD DETECTORS

DESCRIPTION

HA-5130/5135 are precision operational amplifiers manufactured using a combination of key technological advancements to provide outstanding input characteristics.

A Super Beta input stage is combined with laser trimming, dielectric isolation, and matching techniques to produce 25μV (Max.) input offset voltage and 0.4 μV/°C input offset voltage average drift. Other features enhanced by this process include 9nV (Typ.) Input Noise Voltage, 1nA Input Bias Current, and 140dB Open Loop Gain.

These features coupled with 120dB CMRR and PSRR make HA-5130/5135 an ideal device for precision DC instrumentation amplifiers. Excellent input characteristics in conjunction with 2.5MHz bandwidth and 0.8V/μs slew rate, makes this amplifier extremely useful for precision integrator and biomedical amplifier designs. These amplifiers are also well suited for precision data acquisition and for accurate threshold detector applications.

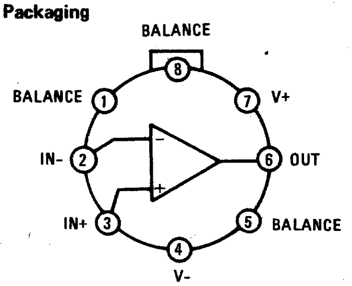
HA-5130/35 is packaged in an 8 pin (TO-99) can and an 8 lead Cerdip and is pin compatible with many existing op amp configurations.

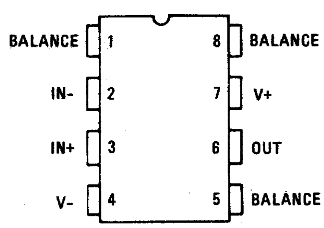
HA-5130/5135-2 is specified for -55°C to +125°C operation while HA-5130/5135-5 operate from 0°C to +75°C.

PINOUT

Section 11 for Packaging

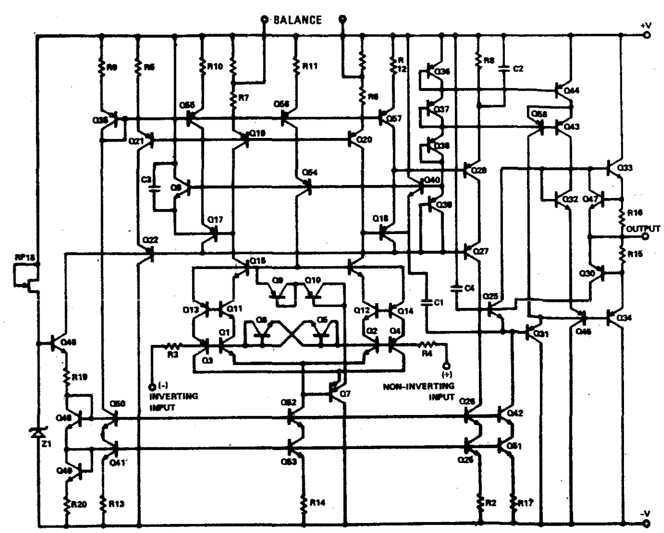
TOP VIEW





* Pins 5 and 8 are internally connected

SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless otherwise stated		Power Dissipation (Note 2)	300mW
Voltage Between V+ and V- Terminals	40.0V	Operating Temperature Range	
Differential Input Voltage	± 15.0V	HA-5130/5135-2	-55°C ≤ T_A ≤ +125°C
		HA-5130/5135-5	0°C ≤ T_A ≤ +75°C
Output Short Circuit Duration	Indefinite	Storage Temperature Range	-65°C ≤ T_A ≤ +150°C

ELECTRICAL CHARACTERISTICS V+ = 15V, V- = -15V

PARAMETER	TEMP.	HA-5130-2/-5 MIN.	HA-5130-2/-5 TYP.	HA-5130-2/-5 MAX.	HA-5135-2/-5 MIN.	HA-5135-2/-5 TYP.	HA-5135-2/-5 MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		10	25		10	75	μV
	Full		50	60		50	130	μV
Average Offset Voltage Drift	Full		0.4	0.6		0.4	1.3	μV/°C
Bias Current	+25°C		±1	±2		±1	±4	nA
	Full			±4			±6	nA
Bias Current Average Drift	Full		0.02	0.04		0.02	0.04	nA/°C
Offset Current	+25°C			2			4	nA
	Full			4			5.5	nA
Offset Current Average Drift	Full		0.02	0.04		0.02	0.04	nA/°C
Common Mode Range	Full	±12			±12			V
Differential Input Resistance	+25°C	20	30		20	30		MΩ
Input Noise Voltage 0.1Hz to 10Hz (Note 3)	+25°C			0.6			0.6	μV_{p-p}
Input Noise Voltage Density (Note 3)	+25°C							$nV/\sqrt{Hz}$
f_0 = 10Hz			13.0	18.0		13.0	18.0	
f_0 = 100Hz			10.0	13.0		10.0	13.0	
f_0 = 1000Hz			9.0	11.0		9.0	11.0	
Input Noise Current (Note 3) 0.1Hz to 10Hz	+25°C		15	30		15	30	pA_{p-p}
Input Noise Current Density (Note 3)	+25°C							$pA/\sqrt{Hz}$
f_0 = 10Hz			0.4	0.8		0.4	0.8	
f_0 = 100Hz			0.17	0.23		0.17	0.23	
f_0 = 1000Hz			0.14	0.17		0.14	0.17	
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 4)	+25°C	120	140		120	140		dB
	Full	120			120			dB
Common Mode Rejection Ratio (Note 5)	Full	110	120		106	120		dB
Closed Loop Bandwidth (A_{VCL} = +1)	+25°C	0.6	2.5		0.6	2.5		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 6)	+25°C	±10	±12		±10	±12		V
	Full	±10			±10			V
Full Power Bandwidth (Note 7)	+25°C	8	10		8	10		kHz
Output Current (Note 8)	+25°C	±25	±30		±25	±30		mA
Output Resistance (Note 9)	+25°C		45			45		Ω
TRANSIENT RESPONSE (Note 10)								
Rise Time	+25°C		340			340		ns
Slew Rate	+25°C	0.5	0.8		0.5	0.8		V/μs
Settling Time (Note 11)	+25°C		11			11		μs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full		1.0	1.3		1.0	1.7	mA
Power Supply Rejection Ratio (Note 12)	Full	100	130		94	130		dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8mW/°C for operation at ambient temp.'s above +75°C.
3. Not tested. 90% of units meet or exceed these specifications.
4. V_{OUT} = ± 10V; R_L = 2k. Gain dB = 20 $\log_{10}$ Average
   ∴ 120dB = 1000V/mV
   140dB = 10,000V/mV
5. V_{CM} = ± 10V DC
6. R_L = 600Ω
7. R_L = 2k; Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$
8. V_{OUT} = 10V
9. Output resistance measured under open loop conditions (f = 100Hz)
10. Refer to test circuits section of the data sheet.
11. Settling time is measured to 0.1% of final value for a 10V output step and A_V = -1.
12. V_{SUPP} = ± 5V DC to ± 20V DC.

LINEAR

Harris Semiconductor

HARRIS

HA-5141/42/44

ADVANCE

Ultra-Low Power Operational Amplifier

FEATURES

- LOW SUPPLY CURRENT 60μA
- WIDE OPERATING VOLTAGE RANGE 2V to 30V
- SINGLE SUPPLY OPERATION
- HIGH SLEW RATE 1.5V/μs
- HIGH GAIN 100K V/V
- AVAILABLE IN SINGLES, DUALS AND QUADS

APPLICATIONS

- PORTABLE INSTRUMENTS
- METER AMPLIFIERS
- TELEPHONE HEADSETS
- MICROPHONE AMPLIFIERS
- INSTRUMENTATION

DESCRIPTION

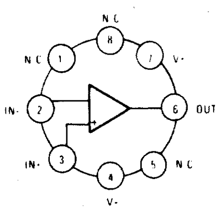
The HA-5141/42/44 ultra-low power operational amplifiers provide AC and DC performance characteristics similar to or better than most general purpose amplifiers while only drawing 1/30 of the supply current of most general purpose amplifiers. These amplifiers are well suited to applications which require low power dissipation and good electrical characteristics.

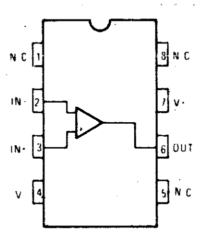
The HA-5141/42/44 provides accurate signal processing by virtue of its low input offset voltage (0.5mV), low input bias current (50nA), high open loop gain (100KV/V) and low noise, for low power operational amplifiers (20nV/$\sqrt{Hz}$). These characteristics coupled with 1.5V/μs slew rate and 400KHz bandwidth make the HA-5141/42/44 ideal for use in low power instrumentation, audio amplifier and active filter designs. The wide range of supply voltages (2V to 30V) also allow these amplifiers to be very useful in low voltage battery powered equipment.

These amplifiers are available in singles (HA-5141, can or minidip), duals (HA-5142, can or minidip) or quads (HA-5144, 14 pin dip) with industry standard pinouts which allow the HA-5141/42/44's to be interchangeable with most other operational amplifiers.

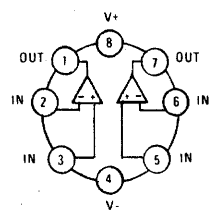
PINOUTS

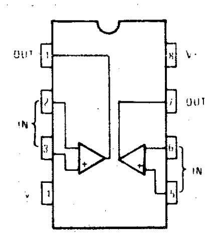
TOP VIEW



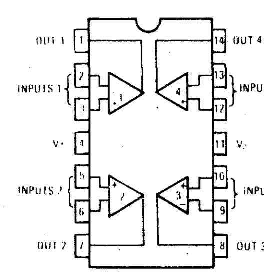


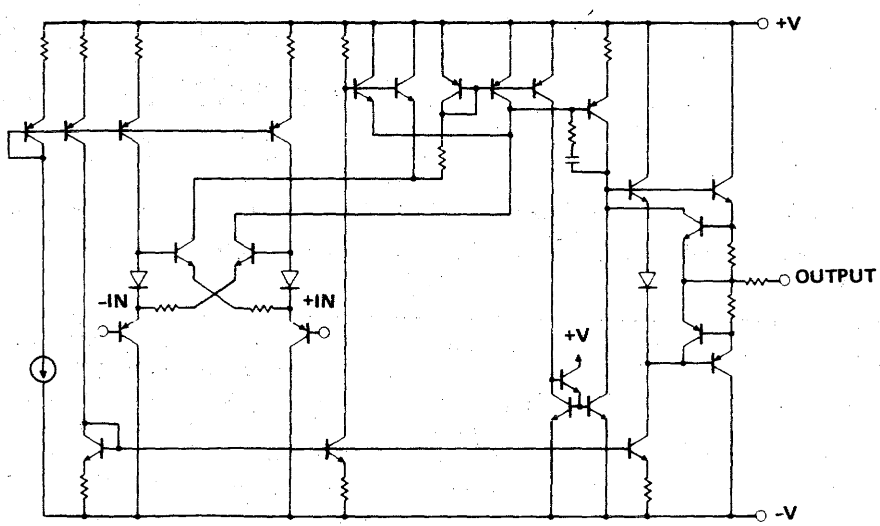
TOP VIEW





TOP VIEW





SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40V	Operating Temperature Range	$0^oC \leq T_A \leq +75^oC$
Differential Input Voltage	±7V		$-55^oC \leq T_A \leq +125^oC$
Output Current	S/C Protected	Storage Temperature Range	$-65^o \leq T_A \leq +150^oC$
Internal Power Dissipation	500mW		

ELECTRICAL CHARACTERISTICS V+ = +5V

		HA-5141/42/44A			HA-5141/42/44			
PARAMETER	TEMP.	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		0.5	6		0.7	7	mV
	Full			8			9	mV
Bias Current	+25°C		45	75		45	100	nA
	Full			100			125	nA
Offset Current	+25°C		0.3	10		0.3	10	nA
	Full			15			20	nA
Common Mode Range	Full	0 to 4			0 to 3			V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain	+25°C	50	100		20	100		KV/V
(Note 1)	Full	30			15			KV/V
Common Mode Rejection	Full	80	105		77	105		dB
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	Full	0 to 4			0 to 3			V
TRANSIENT RESPONSE								
Slew Rate (Notes 1,2,3)	+25°C	1	1.5		0.5	1		V/μs
POWER SUPPLY CHARACTERISTICS								
Supply Current (per Amplifier)	+25°C		45	65		50	80	μA
	Full			75			100	μA
Power Supply Rejection Ratio	Full	80	105		77	105		dB

NOTES:
1. RL = 50K
2. CL = 50pf
3. VIN = +3V Pulse

HARRIS

HA-5160/5162

Wideband, JFET Input, High Slew Rate, Uncompensated, Operational Amplifier

FEATURES

- WIDE GAIN BANDWIDTH 100MHz
- HIGH SLEW RATE 120V/μs
- SETTLING TIME (0.2%) 280ns
- POWER BANDWIDTH 1000kHz
- OFFSET VOLTAGE 1.0mV
- BIAS CURRENT 20pA

APPLICATIONS

- VIDEO AND RF AMPLIFIERS
- DATA ACQUISITION
- PULSE AMPLIFIERS
- PRECISION SIGNAL GENERATION

DESCRIPTION

The HA-5160/5162 is a wideband, uncompensated, operational amplifier manufactured with FET/Bipolar technologies and dielectric isolation. This monolithic amplifier features superior high frequency capabilities further enhanced by precision laser trimming of the input stage to provide excelent input characteristics. This device has excellent phase margin at a closed loop gain of 10 without external compensation.

The HA-5160/5162 offers a number of important advantages over similar FET input op amps from other manufacturers. In addition to superior bandwidth and settling characteristics, the HARRIS devices have nearly constant slew rate, bandwidth, and settling characteristics over the operating temperature range. This provides the user predictable performance in applications where settling time, full power bandwidth, closed loop bandwidth, or phase shift is critical. Note also that HARRIS specified all parameters at ambient (rather than junction) temperature to provide the designer meaningful data to predict actual operating performance.

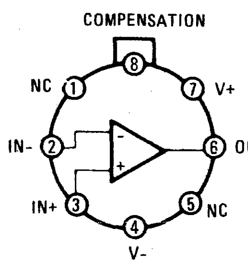
Complementing the HA-5160/5162's predictable and excellent dynamic characteristics are very low input offset voltage, very low input bias current, and extremely high input impedance. This ideal combination of features make these amplifiers most suitable for precision, high speed, data acquisition system designs and for a wide variety of signal conditioning applications.* The HA-5160 provides excellent performance for applications which require both precision and high speed performance. The HA-5162 meets or exceeds the performance specifications of National's hybrid op amp, the LH0062.

* -2 denotes a range of -55°C to +125°C and -5 denotes a 0°C to +75°C range.

PINOUT

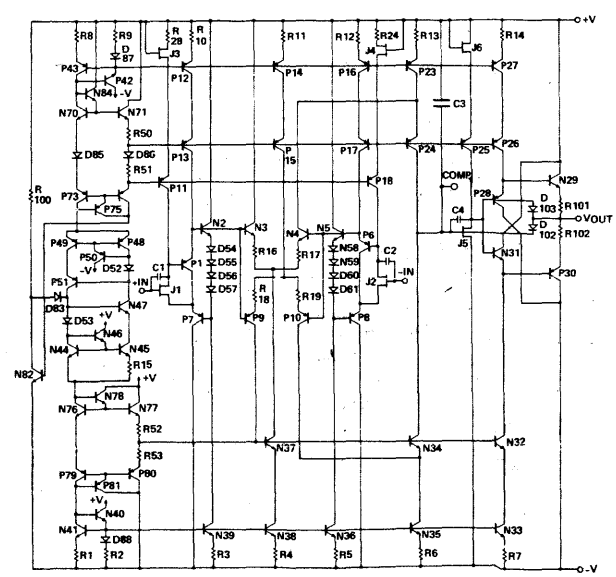
Section 11 for Packaging

TOP VIEW



Case connected to V-

SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V-	40V
Differential Input Voltage	±40V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation (Note 2)	675mW
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS V+ = +15V, V- = -15V

PARAMETER	TEMP	HA-5160-2 -55°C to +125°C MIN	TYP	MAX	HA-5160-5 0°C to +75°C MIN	TYP	MAX	HA-5162-5 0°C to 75°C MIN	MAX	TYP	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		1.0	3.0		1.0	3.0		3	15	mV
	Full		3.0	5.0		3.0	5.0		5	20	mV
Offset Voltage Average Drift	Full		10			20			20	35	μV/°C
Bias Current	+25°C		20	50		20	50		20	65	pA
	Full		5	10			10			10	nA
Offset Current	+25°C		2	10		2	10		2	10	pA
	Full		2	5		2	5		2	5	nA
Input Resistance	+25°C		10^{12}			10^{12}			10^{12}		Ω
Common Mode Range	Full	±10	±11		±10	±11		±10	±11		V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 3)	+25°C	75K	150K		75K	150K		25K	100K		V/V
	Full	60K	100K		60K	100K		25K	75K		V/V
Common Mode Rejection Ratio (Note 4)	Full	74	80		74	80		70	80		dB
Gain Bandwidth Product (A_V = 10)	Full		100			100			100		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 5)	+25°C	±10	±11		±10	±11		±10	±11		V
	Full	±10	±11		±10	±11		±10	±11		V
Output Current (Note 6)	+25°C	±15	±20		±15	±20		±15	±20		mA
Full Power Bandwidth (Note 7)	+25°C		1000			1000			1000		kHz
Output Resistance (Note 8)	+25°C		50			50			50		Ω
TRANSIENT RESPONSE (Note 9)											
Rise Time (A_V = 10)	+25°C		20			20			20		ns
Slew Rate (A_V = 10)	+25°C	100	120		100	120		50	70		V/μs
Settling Time (Note 10)	+25°C		280			280			400		ns
POWER SUPPLY CHARACTERISTICS											
Supply Current	Full		8.0	10		8.0	10		8.0	12	mA
Power Supply Rejection Ratio (Note 11)	+25°C	74	86		74	86		70	86		dB

HARRIS

HA-5170

Precision JFET Input Operational Amplifier

FEATURES

- LOW OFFSET VOLTAGE 100μV
- LOW OFFSET VOLTAGE DRIFT 2μV/°C
- LOW NOISE 10nV/$\sqrt{Hz}$
- HIGH OPEN LOOP GAIN 600K V/V
- WIDE BANDWIDTH 5MHz

APPLICATIONS

- HIGH GAIN INSTRUMENTATION AMPLIFIERS
- PRECISION DATA ACQUISITION
- PRECISION INTEGRATORS
- PRECISION THRESHOLD DETECTORS

DESCRIPTION

The Harris HA-5170 is a precision, JFET input, operational amplifier which features low noise, low offset voltage and low offset voltage drift. Constructed using FET/Bipolar technology, the Harris Dielectric Isolation (DI) process, and laser trimming this amplifier offers low input bias and offset currents. This operational amplifier design also completely eliminates the troublesome errors due to warm-up drift.

Complementing these excellent input characteristics are dynamic performance characteristics never before available from precision operational amplifiers. An 8V/μ s slew rate and 5MHz bandwidth allow the designer to extend precision instrumentation applications in both speed and bandwidth. These characteristics make the HA-5170 well suited for precision integrator amplifier designs.

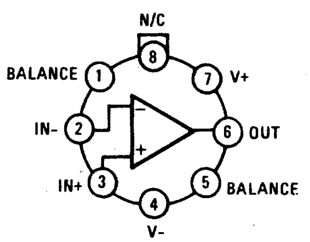
The superior input characteristics also make the HA-5170 ideally suited for transducer signal amplifiers, precision voltage followers and precision data acquisition systems.

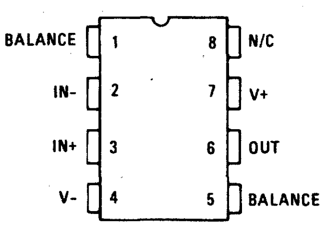
Packaged in an 8-pin (TO-99) can or an 8 lead Minidip, the HA-5170 is pin compatible with most existing op amp configurations.

PINOUT

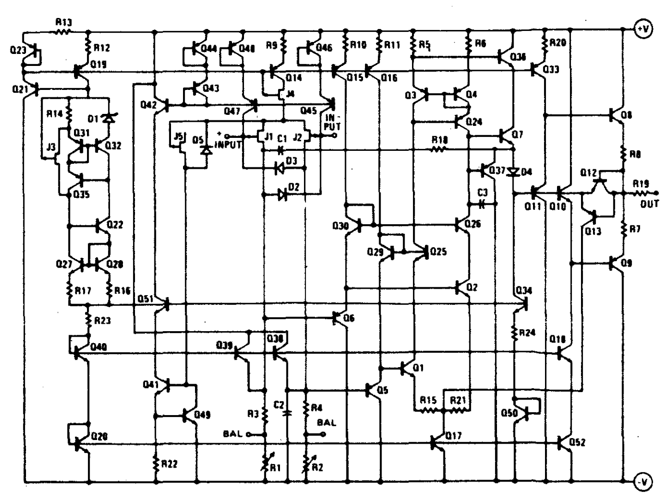
Section 11 for Packaging

TOP VIEW





SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless otherwise stated		Power Dissipation (Note 2)	675mW
Voltage Between V+ and V- Terminals	44.0V	Operating Temperature Range	
Differential Input Voltage	± 30.0V	HA-5170-2	$-55°C \leq T_A \leq +125°C$
		HA-5170-5	$0°C \leq T_A \leq +75°C$
Output Short Circuit Duration	Indefinite	Storage Temperature Range	$-65°C \leq T_A \leq +150°C$

ELECTRICAL CHARACTERISTICS V+ = 15V, V- = -15V

PARAMETER	TEMP.	HA-5170-2 MIN	HA-5170-2 TYP	HA-5170-2 MAX	HA-5170-5 MIN	HA-5170-5 TYP	HA-5170-5 MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		0.1	0.3		0.1	0.3	mV
	Full			0.5			0.5	mV
Average Offset Voltage Drift (Note 3)	Full		2	5		2	5	μV/°C
Bias Current	+25°C		20	100		20	100	pA
	Full		3	30		0.1	2	nA
Bias Current Average Drift	Full		3			3		pA/°C
Offset Current	+25°C		3	30		3	60	pA
	Full			5			0.1	nA
Offset Current Average Drift	Full		0.3			0.3		pA/°C
Common Mode Range	Full	±10	+15.1 -12		±10	+15.1 -12		V
Differential Input Resistance	+25°C		6×10^{10}			6×10^{10}		Ω
Input Capacitance	+25°C		12			12		pF
Input Noise Voltage 0.1Hz to 10Hz (Note 3)	+25°C		0.5	5		0.5	5	μV_{p-p}
Input Noise Voltage Density (Note 3)	+25°C							
f_0 = 10Hz			20	150		20	150	nV/√Hz
f_0 = 100Hz			12	50		12	50	nV/√Hz
f_0 = 1000Hz			10	25		10	25	nV/√Hz
Input Noise Current Density (Note 3)	+25°C							
f_0 = 10Hz			.05			.05		pA/√Hz
f_0 = 100Hz			.01			.01		pA/√Hz
f_0 = 1000Hz			.01			.01		pA/√Hz
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 4)	+25°C	300K	600K		300K	600K		V/V
	Full	200K			250K			V/V
Common Mode Rejection Ratio (Note 5)	Full	85	100		90	100		dB
Closed Loop Bandwidth (A_{VCL} = +1)	+25°C	4	8		4	8		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 6)	+25°C	±10	±12		±10	±12		V
Full Power Bandwidth (Note 7)	+25°C	80	120		80	120		kHz
Output Current (Note 8)	+25°C	±10			±10			mA
Output Resistance (Note 9)	+25°C		45			45		Ω
TRANSIENT RESPONSE								
Rise Time	+25°C		45	100		45	100	ns
Slew Rate	+25°C	5	8		5	8		V/μs
Settling Time (Note 10)	+25°C		1			1		μs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full		1.9	2.5		1.9	2.5	mA
Power Supply Rejection Ratio (Note 11)	Full	85	105		90	105		dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8 mW/°C for operation at ambient temperatures above +75°C.
3. Parameter is not 100% tested. 90% of all units meet or exceed these specifications.
4. V_{OUT} = ±10V; R_L = 2k.
5. V_{CM} = ±10V D. C.
6. R_L = 2kΩ.
7. R_L = 2k; Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$
8. V_{OUT} = 10V.
9. Output resistance measured under open loop conditions (f = 100Hz).
10. Settling time is measured to 0.1% of final value for a 10V output step and A_V = -1.
11. V_{SUPP} = ±5V D. C. to ±20V D. C.

HARRIS

HA-5180/5180A

Low Bias Current, Low Power JFET Input Operational Amplifier

APRIL 1982 **Preliminary**

FEATURES

- ULTRA LOW BIAS CURRENT 250fA
- LOW POWER SUPPLY CURRENT 0.8mA
- LOW OFFSET VOLTAGE 0.5mV (max.)
- BANDWIDTH 2 MHz
- SLEW RATE 7V/μs

APPLICATIONS

- ELECTROMETER AMPLIFIER DESIGNS
- PHOTO CURRENT DETECTORS
- PRECISION LONG-TERM INTEGRATORS
- LOW DRIFT SAMPLE & HOLD CIRCUITS
- VERY HIGH IMPEDANCE BUFFERS
- HIGH IMPEDANCE BIOLOGICAL MICRO PROBES

DESCRIPTION

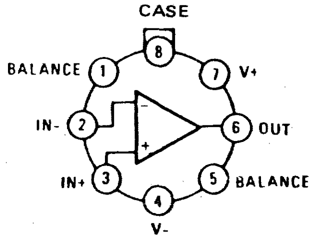
The HARRIS HA-5180/5180A is an ultra low input bias current, JFET input, monolithic operational amplifier which also features low power, low offset voltage and excellent AC characteristics. Employing FET/Bipolar construction coupled with dielectric isolation this operational amplifier offers the lowest input bias currents (250fA typ.) available in any monolithic operational amplifier. The HA-5180/5180A has another unique feature in which the offset bias current may be nulled by externally adjusting the offset voltage. For applications which require precision performance the HA-5180A offers an input offset voltage of 0.5 mV (max) while the HA-5180 offers 3 mV (max.)

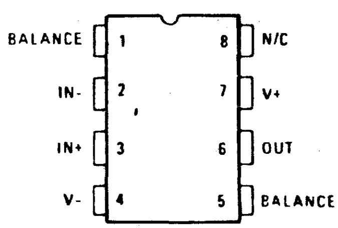
The HA-5180/5180A also offers excellent AC performance not previously available in similar hybrid or monolithic op amp designs. The 2 MHz bandwidth and 7V/μs slew rate of the HA-5180/5180A extends the bandwidth and speed for applications such as very low drift sample and hold amplifiers and photo-current detectors. Other applications include use in electrometer designs, pH/Ion sensitive electrodes, low current oxygen sensors, long term precision integrators and very high impedance buffer measurement designs.

The HA-5180/5180A is packaged in an 8-pin (TO-99) can and an 8-lead cerdip and is pin compatible with most existing op amp configurations. The case of the TO-99 package is internally connected to pin 8 so that it may be connected to the same potential as the input. This feature helps minimize stray leakage to the case, helps shield the amplifier from external noise and reduces common mode input capacitance.

PINOUT

TOP VIEW





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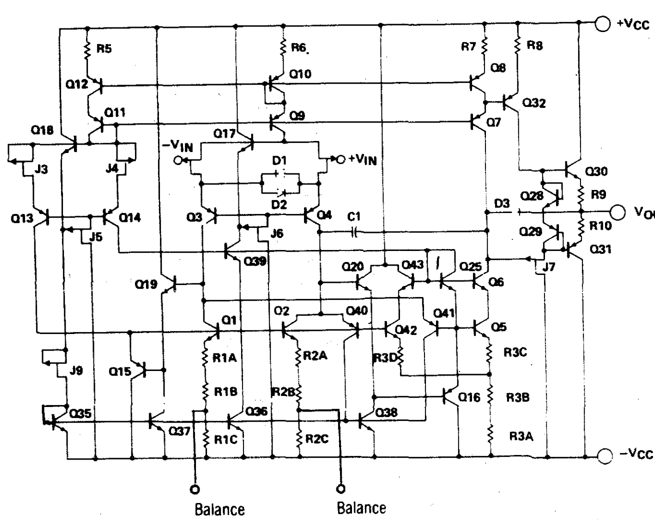


ABSOLUTE MAXIMUM RATINGS (Note 1)

$T_A = +25°C$ Unless otherwise stated

Voltage Between V+ and V− Terminals	40.0V	Power Dissipation (Note 2)	300mW
Differential Input Voltage	±40V	Operating Temperature Range	
		HA-5180/5180A-2	$-55°C \le T_A \le +125°C$
		HA-5180/5180A-5	$0°C \le T_A \le +75°C$
Output Short Circuit Duration	Indefinite	Storage Temperature Range	$-65°C \le T_A \le +150°C$

ELECTRICAL RATINGS V+ = 15V, V− = −15V

PARAMETER	TEMP.	5180A-2 MIN	5180A-2 TYP	5180A-2 MAX	5180A-5 MIN	5180A-5 TYP	5180A-5 MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		**0.1**	0.5		**0.1**	0.5	mV
	Full			1			1	mV
Average Offset Voltage Drift	Full		5			5		μV/°C
Bias Current (Note 3)	+25°C		250	1000		250	1000	fA
	Full		100	500		6	**30**	pA
Offset Current (Note 3)	+25°C		30	200		30	200	fA
	Full		6	30		1	5	pA
Common Mode Range	Full	±10	±12		±10	±12		V
Differential Input Resistance	+25°C		10^{12}			10^{12}		Ω
Input Noise Voltage (f = 1kHz)	+25°C		70			70		nV/√Hz
Input Noise Current (f = 1kHz)	+25°C		0.01			0.01		pA/√Hz
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 4)	+25°C	200k	1M		200k	1M		V/V
	Full	150k			150k			V/V
Common Mode Rejection Ratio (Note 5)	Full	90	110		90	110		dB
Closed Loop Bandwidth ($A_{VCL} = +1$)	+25°C		2			2		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 6)	+25°C	±10	±12		±10	±12		V
	Full	±10			±10			V
Full Power Bandwidth (Note 7)	+25°C		110			110		kHz
Output Current (Note 8)	+25°C	±10	±15		±10	±15		mA
Output Resistance (Note 9)	+25°C		25			25		Ω
TRANSIENT RESPONSE								
Rise Time	+25°C	-	75			75		ns
Slew Rate	+25°C	4	7		4	7		V/μs
Settling Time (Note 10)	+25°C		2			2		μs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full		0.7	1		0.8	1	mA
Power Supply Rejection Ratio (Note 11)	Full	85	105		85	105		dB

LINEAR

Harris Semiconductor

ELECTRICAL RATINGS   V+ = 15V, V− = −15V

PARAMETER	TEMP	5180A-2 MIN	5180A-2 TYP	5180A-2 MAX	5180A-5 MIN	5180A-5 TYP	5180A-5 MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		1	3		1	3	mV
	Full			4			4	mV
								mV
								mV
Average Offset Voltage Drift	Full		5			5		μV/°C
Bias Current (Note 3)	+25°C		250	1000		250	1000	fA
	Full		100	500		6	30	pA
Offset Current (Note 3)	+25°C		30	200		30	200	fA
	Full		6	30		1	5	pA
Common Mode Range	Full	±10	±12		±10	±12		V
Differential Input Resistance	+25°C		10^{12}			10^{12}		Ω
Input Noise Voltage (f = 1kHz)	+25°C		70			70		$nV/\sqrt{Hz}$
Input Noise Current (f = 1kHz)	+25°C		0.01			0.01		$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 4)	+25°C	200k	1M		200k	1M		V/V
	Full	150k			150k			V/V
Common Mode Rejection Ratio (Note 5)	Full	90	110		90	110		dB
Closed Loop Bandwidth (A_{VCL} = +1)	+25°C		2			2		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 6)	+25°C	±10	±12		±10	±12		V
	Full	±10			±10			V
Full Power Bandwidth (Note 7)	+25°C		110			110		kHz
Output Current (Note 8)	+25°C	±10	±15		±10	±15		mA
Output Resistance (Note 9)	+25°C		25			25		Ω
TRANSIENT RESPONSE								
Rise Time	+25°C		75			75		ns
Slew Rate	+25°C	4	7		4	7		V/μs
Settling Time (Note 10)	+25°C		2			2		μs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full		0.7	1		0.8	1	mA
Power Supply Rejection Ratio (Note 11)	Full	85	105		85	105		dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Deraie at 6.9 mW/°C for operation at ambient temperatures above +75°C.
3. This parameter is guaranteed by design and is not 100% tested.
4. $V_{OUT} = \pm 10V$; $R_L = 2k$. Gain dB = 20 $\log_{10}$Av.
5. $V_{CM} = \pm 10V$ D.C.
6. R_l = 2k
7. R_L = 2k; Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$
8. $V_{OUT} = \pm 10V$.
9. Output resistance measured under open loop conditions (f = 100Hz)
10. Settling time is measured to 0.1% of final value for a 10V output step and $A_V = -1$.
11. V_{SUPP} = + 5V D.C. to ±20V D.C.

HARRIS

HA-5190/5195

Wideband, Fast Settling Operational Amplifier

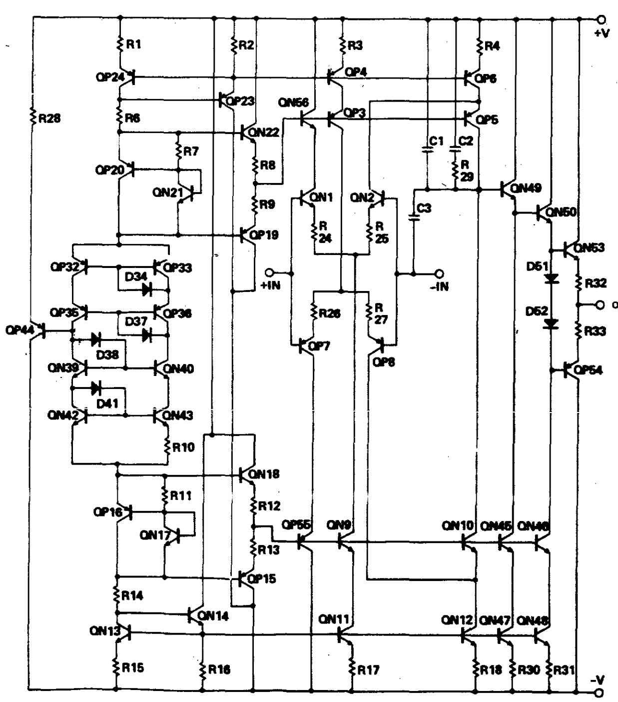
FEATURES

- FAST SETTLING TIME 70ns
- VERY HIGH SLEW RATE 200V/μs
- WIDE GAIN-BANDWIDTH 150MHz
- POWER BANDWIDTH 6.5MHz
- LOW OFFSET VOLTAGE 5mV
- INPUT VOLTAGE NOISE 15nV/$\sqrt{Hz}$
- MONOLITHIC BIPOLAR CONSTRUCTION

APPLICATIONS

- FAST, PRECISE D/A CONVERTERS
- HIGH SPEED SAMPLE-HOLD CIRCUITS
- PULSE AND VIDEO AMPLIFIERS
- WIDEBAND AMPLIFIERS
- REPLACE COSTLY HYBRIDS

SCHEMATIC



GENERAL DESCRIPTION

HA-5190/5195 are monolithic operational amplifiers featuring an ultimate combination of speed, precision, and bandwidth. Employing monolithic bipolar construction coupled with dielectric isolation, these devices are capable of delivering an unparalleled 200V/μs slew rate with a settling time of 70ns (0.1%, 5V output step). These truly differential amplifiers are designed to operate at gains $\geq$5 without the need for external compensation. Other outstanding HA-5190/5195 features are 150MHz gain-bandwidth-product and 6.5MHz full power bandwidth. In addition to these dynamic characteristics, these amplifiers also have excellent input characteristics such as 5mV offset voltage and 15nV input voltage noise (at 1kHz).

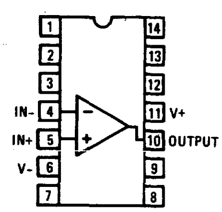
With 200V/μs slew rate and 70ns settling time, these devices make ideal output amplifiers for accurate, high speed D/A converters or the main components in high speed sample/hold circuits. 150MHz gain-bandwidth-product, 6.5MHz power bandwidth, and 5mV offset voltage make HA-5190/5195 ideally suited for a variety of pulse and wideband video amplifier applications.

At temperatures above +75°C, a heat sink is required for HA-5190. (See note 2). HA-5190 is specified over the -55°C to +125°C range while HA-5195 is specified from 0°C to +75°C.

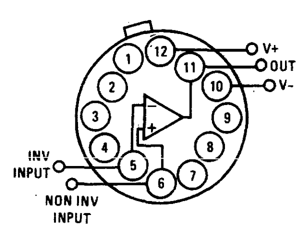
PINOUTS

Section 11 for Packaging

TOP VIEW



TOP VIEW



CASE TIED TO V-

LH0032 PINOUT

LINEAR

Harris Semiconductor

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage between V+ and V- Terminals	35V
Differential Input Voltage	6V
Output Current	50mA (Peak)
Internal Power Dissipation (Note 2)	870mW (Cerdip); 1W (TO-8) Free Air
Operating Temperature Range: (HA-5190)	$-55^{o}C \leq T_A \leq +125^{o}C$
(HA-5195)	$0^{o}C \leq T_A \leq +75^{o}C$
Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS $V_{SUPPLY} = \pm 15$ Volts; R_L = 1K ohms, unless otherwise specified.

PARAMETER	TEMP	HA-5190 -55°C to +125°C MIN	TYP	MAX	HA-5195 0°C to +75°C MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		3.0	5.0		3.0	6	mV
	FULL			10.0			10.0	mV
Average Offset Voltage Drift	FULL		20			20		µV/°C
Bias Current	+25°C		5	15		5	15	µA
	FULL			20			20	µA
Offset Current	+25°C		1	4		1	4	µA
	FULL			6			6	µA
Input Resistance	+25°C		10			10		Kohms
Input Capacitance	+25°C		1.0			1.0		pF
Common Mode Range	FULL	±5			±5			V
Input Noise Voltage (f = 1kHz, R_g = 0Ω)	+25°C		15			15		$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	15K	30K		10K	30K		V/V
	FULL	5K			5K			V/V
Common-Mode Rejection Ratio (Note 4)	FULL	74			74			dB
Gain-Bandwidth-Product (Notes 5 & 6)	+25°C		150			150		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 3)	FULL	±5	±8		±5	±8		V
Output Current (Note 3)	+25°C	25	30		25	30		mA
Output Resistance	+25°C		30			30		Ohms
Full Power Bandwidth (Note 3 & 7)	+25°C	5	6.5		5	6.5		MHz
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C		13	18		13	18	ns
Overshoot	+25°C		8			8		%
Slew Rate	+25°C	160	200		160	200		V/µs
Settling Time:								
5V Step to 0.1%	+25°C		70			70		ns
5V Step to 0.01%	+25°C		100			100		ns
2.5V Step to 0.1%	+25°C		50			50		ns
2.5V Step to 0.01%	+25°C		80			80		ns
POWER REQUIREMENTS								
Supply Current	FULL		19	28		19	28	mA
Power Supply Rejection Ratio (Note 9)	FULL	70	90		70	90		dB

LINEAR

Harris Semiconductor

HARRIS

HA-4900/02/05

Precision Quad Comparator

FEATURES

- FAST RESPONSE TIME 130ns
- LOW OFFSET VOLTAGE 2.0mV
- LOW OFFSET CURRENT 10nA
- SINGLE OR DUAL-VOLTAGE SUPPLY OPERATION
- SELECTABLE OUTPUT LOGIC LEVELS
- ACTIVE PULL-UP/PULL-DOWN OUTPUT CIRCUIT - NO EXTERNAL RESISTORS REQUIRED

APPLICATIONS

- THRESHOLD DETECTOR
- ZERO-CROSSING DETECTOR
- WINDOW DETECTOR
- ANALOG INTERFACES FOR MICROPROCESSORS
- HIGH STABILITY OSCILLATORS
- LOGIC SYSTEM INTERFACES

DESCRIPTION

The HA-4900 series are monolithic, quad, precision comparators offering fast response time, low offset voltage, low offset current, and virtually no channel-to-channel crosstalk for applications requiring accurate, high speed, signal level detection. These comparators can sense signals at ground level while being operated from either a single +5 volt supply (digital systems) or from dual supplies (analog networks) up to ±15 volts. The HA-4900 series contains a unique current driven output stage which can be connected to logic system supplies ($V_{Logic}+$ and $V_{Logic}-$) to make the output levels directly compatible (no external components needed) with any standard logic or special system logic levels. In combination analog/digital systems, the design employed in the HA-4900 series input and output stages prevents troublesome ground coupling of signals between analog and digital portions of the system.

These comparators' combination of features makes them ideal components for signal detection and processing in data acquisition systems, test equipment, and microprocessor/analog signal interface networks.

All devices are available in 16 pin dual-in-line ceramic packages. The HA-4900/4902-2 operates from -55°C to +125°C and the HA-4905-5 operates over a 0°C to +75°C temperature range.

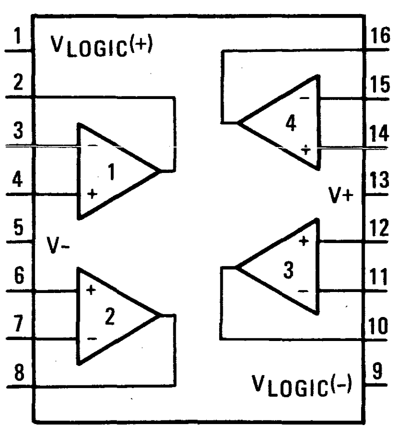
LINEAR

Harris Semiconductor

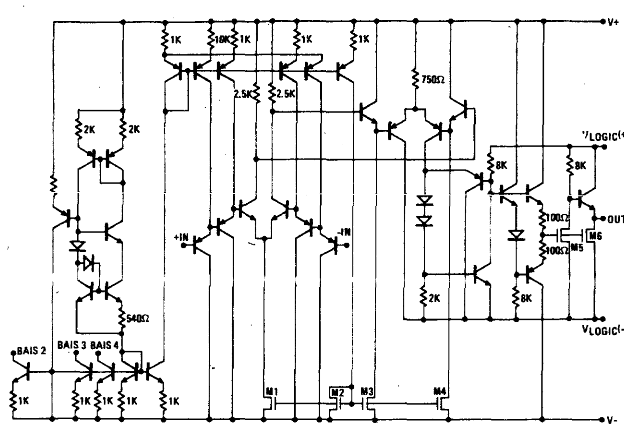
PINOUT

Section 11 for Packaging

Top View



SCHEMATIC



ONE FOURTH ONLY (HA-4900 SERIES)

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V-	33V
Voltage Between $V_{Logic}(+)$ and $V_{Logic}(-)$	18V
Differential Input Voltage	±15V
Peak Output Current	±50mA
Internal Power Dissipation (Note 7, 8)	880mW
Storage Temperature Range	$-65^oC \leq T_A \leq 150^oC$

ELECTRICAL CHARACTERISTICS V+ = +15.0V, V- = -15.0V, $V_{Logic}(+)$ = 5.0V, $V_{Logic}(-)$ = GND.

PARAMETER	TEMP	HA-4900-2 -55°C to +125°C			HA-4902-2 -55°C to +125°C			HA-4905-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage (Note 2)	25°C		2	3		2	5		4	7.5	mV
	Full			4			8			10	mV
Offset Current	25°C		10	25		10	35		25	50	nA
	Full			35			35			70	nA
Bias Current (Note 3)	25°C		50	75		50	150		100	150	nA
	Full			150			200			300	nA
Input Sensitivity (Note 4)	25°C			Vio +.3			Vio +.5			Vio +.5	mV
	Full			Vio +.4			Vio +.6			Vio +.7	mV
Common Mode Range	Full	V-		V+ -2.4	V-		V+ +2.4	V-		V+ +2.4	V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain	25°C		400K			400K			400K		V/V
Response Time ($T_{pd}0$) (Note 5)	25°C		130	200		130	200		130	200	ns
Response Time ($T_{pd}1$) (Note 5)	25°C		180	215		180	215		180	215	ns
OUTPUT CHARACTERISITICS											
Output Voltage Level											
Logic "Low State" (V_{OL}) (Note 6)	Full		0.2	0.4		0.2	0.4		0.2	0.4	V
Logic "High State" (V_{OH}) (Note 6)	Full	3.5	4.2		3.5	4.2		3.5	4.2		V
Output Current											
I_{Sink}	Full	3.0			3.0			3.0			mA
I_{Source}	Full	3.0			3.0			3.0			mA
POWER SUPPLY CHARACTERISTICS											
Supply Current, I_{ps} (+)	25°C		6.5	20		6.5	20		7	20	mA
Supply Current, I_{ps} (-)	25°C		4	8		4	8		5	8	mA
Supply Current, I_{ps} (Logic)	25°C		2.0	4		2.0	4		2.0	4	mA
Supply Voltage Range											
V_{Logic} (+) (Note 7)	Full	0		+15.0	0		+15.0	0		+15.0	V
V_{Logic} (-) (Note 7)	Full	-15.0		0	-15.0		0	-15.0		0	V

LINEAR

Harris Semiconductor

HARRIS

HA-5102/04/12/14

Low Noise High Performance Operational Amplifiers

Preliminary

FEATURES

- LOW NOISE — 4.3 nV/√Hz
- WIDE BANDWIDTH — 8MHz (COMP.), 60MHz (UNCOMP.)
- HIGH SLEW RATE — 3V/μs (COMP.), 20V/μs (UNCOMP.)
- LOW OFFSET VOLTAGE — 2mV
- SINGLE SUPPLY OPERATION
- AVAILABLE IN DUALS OR QUADS

APPLICATIONS

- HIGH Q, ACTIVE FILTERS
- AUDIO AMPLIFIERS
- INSTRUMENTATION AMPLIFIERS
- INTEGRATORS
- SIGNAL GENERATORS

DESCRIPTION

Low noise and high performance are key words describing HA-5102/04/12/14. These general purpose amplifiers offer an array of dynamic specifications ranging from 3V/μs slew rate and 8MHz bandwidth (5102/04) to 20V/μs slew rate and 60MHz gain-bandwidth-product (HA-5112/14). Complementing these outstanding parameters is a very low noise specification of 4.3 nV/√Hz at 1KHz.

Fabricated using the Harris standard high frequency process, these operational amplifiers also offer excellent input specifications such as 2.0mV offset voltage and 30nA offset current. Complementing these specifications are 108dB open loop gain and 108dB channel separation. Consuming a very modest amount of power (90mW/package for duals and 150mW/package for quads), HA-5102/04/12/14 also provide the flexibility of operating from a single +5V supply.

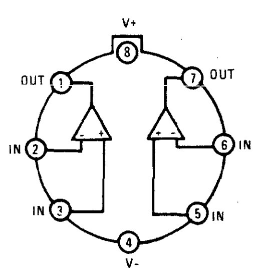
This impressive combination of features make this series of amplifiers ideally suited for designs ranging from audio amplifiers and active filters to the most demanding signal conditioning and instrumentation circuits.

These operational amplifiers are available in dual or quad form with industry standard pinouts allowing for immediate interchangeability with most other dual and quad operational amplifiers.

HA-5102	Dual, Compensated
HA-5112	Dual, Uncompensated
HA-5104	Quad, Compensated
HA-5114	Quad, Uncompensated

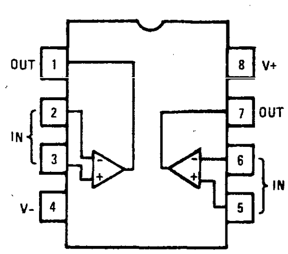
PINOUTS

TOP VIEW



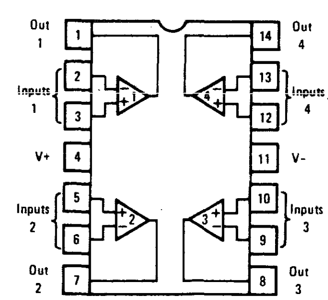
HA-5102/12

TOP VIEW



HA-5102/12

TOP VIEW



HA-5104/14

ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless Otherwise Stated		Power Dissipation (Note 4)	880mW
Voltage Between V+ and V- Terminals	40.0V	Operating Temperature Range	
Differential Input Voltage	±7V	HA-5102/5104/5112/5114-2	$-55°C \leq T_A \leq +125°C$
Input Voltage (Note 2)	±15.0V	HA-5102/5104/5112/5114-5	$0°C \leq T_A \leq +75°C$
Output Short Circuit Duration (Note 3)	Indefinite	Storage Temperature Range	$-65°C \leq T_A \leq +150°C$

ELECTRICAL CHARACTERISTICS

V+ = 15VDC; V- = -15VDC

		HA-5102-2 HA-5112-2 -55°C to +125°C			HA-5104-2 HA-5114-2 -55°C to +125°C			HA-5102-5 HA-5112-5 0°C to +75°C			HA-5104-5 HA-5114-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS														
Offset Voltage	+25°C		0.5	2.0		0.5	2.5		0.5	2.0		0.5	2.5	mV
	Full			2.5			3.0			2.5			3.0	mV
Offset Voltage Average Drift	Full		3			3			3			3		μV/°C
Bias Current	+25°C		130	200		130	200		130	200		130	200	nA
	Full			325			325			325			325	nA
Offset Current	+25°C		30	75		30	75		30	75		30	75	nA
	Full			125			125			125			125	nA
Input Resistance	+25°C		500			500			500			500		kΩ
Common Mode Range	Full	±12			±12			±12			±12			V
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Note 5)	†25°C													
	Full	100K	250K		100K	250K		100K	250K		100K	250K		V/V
Common Mode Rejection Ratio (Note 6)	Full	86			86			86			86			dB
Small Signal Bandwidth	+25°C													
HA-5102/5104			8			8			8			8		MHz
Gain Bandwidth Product	+25°C													
HA-5112/5114 A_V = 10			60			60				60		60		MHz
Channel Separation (Note 7)	+25°C		108			108			180			108		dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (R_L = 10K)	Full	±12	±13		±12	±13		±12	±13		±12	±13		V
(R_L = 2K)	Full	±10	±12		±10	±12		±10	±12		±10	±12		V
Output Current (Note 8)	Full	±10	±15		±10	±15		±10	±15		±10	±15		mA
Full Power Bandwidth														
(Note 9) HA-5102/5104	+25°C		50			50			50			50		kHz
HA-5112/5114	+25°C		250			250			250			250		kHz
Output Resistance	+25°C		110			110			110			110		Ω

ELECTRICAL CHARACTERISTICS

V+ = 15VDC; V- = -15VDC

PARAMETER	TEMP	HA-5102-2 HA-5112-2 -55°C to +125°C			HA-5104-2 HA-5114-2 -55°C to +125°C			HA-5102-5 HA-5112-5 0°C to +75°C			HA-5104-5 HA-5114-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TRANSIENT RESPONSE (Note 10)														
Rise time														
HA-5102/5104	+25°C		50	100		50	100		50	100		50	100	ns
HA-5112/5114	+25°C		38	60		38	60		38	60		38	60	ns
Overshoot														
HA-5102/5104	+25°C		20	35		20	35		20	35		20	35	%
HA-5112/5114	+25°C		30	40		30	40		30	40		30	40	%
Slew Rate														
HA-5102/5104	+25°C	±1	±3		±1	±3		±1	±3		±1	±3		V/μs
HA-5112/5114	+25°C	±12	±20		±12	±20		±12	±20		±12	±20		V/μs
Settling Time (Note 11)														
HA-5102/5104	+25°C		4.5			4.5			4.5			4.5		μs
HA-5112/5114	+25°C		0.6			0.6			0.6			0.6		μs
NOISE CHARACTERISTICS														
Input Noise Voltage	+25°C													
f = 10Hz			17			17			17			17		$nV/\sqrt{Hz}$
f = 1KHz			4.3			4.3			4.3			4.3		$nV/\sqrt{Hz}$
Input Noise Current	+25°C													
f = 10Hz			5.1			5.1			5.1			5.1		$pA/\sqrt{Hz}$
f = 1KHz			.57			.57			.57			.57		$pA/\sqrt{Hz}$
Broadband Noise Voltage	+25°C													
f = DC to -30KHz			870			870			870			870		nVrms
POWER SUPPLY CHARACTERISTICS														
Supply Current														
HA-5102/5112	+25°C		3.0	5.0		3.0	5.0		3.0	5.0		3.0	5.0	mA
HA-5104/5114	+25°C		5.0	6.5		5.0	6.5		5.0	6.5		5.0	6.5	mA
Power Supply Rejection Ratio (Note 6)	Full	86			86			86			86			dB

HARRIS

HA-5033

Preliminary

Video Buffer

FEATURES

- DIFFERENTIAL PHASE ERROR .1°
- DIFFERENTIAL GAIN ERROR .1%
- HIGH SLEW RATE 1000V/μs
- WIDE POWER BANDWIDTH DC TO 80MHz
- FAST RISE TIME 3ns
- WIDE POWER SUPPLY RANGE ±5 to ±16V

APPLICATIONS

- VIDEO BUFFER
- HIGH FREQUENCY BUFFER
- OP AMP ISOLATION BUFFER
- HIGH SPEED LINE DRIVER
- IMPEDANCE MATCHING

DESCRIPTION

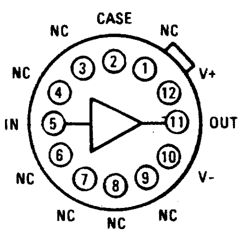
The HA-5033 is a high performance voltage follower designed for use in high frequency applications requiring a high speed wideband buffer. Specifically designed for driving coaxial cable and featuring a bandwidth of 250MHz and outstanding differential gain and phase characteristics, the HA-5033 is an excellent device for the line driver and buffer applications common to video circuit design. In addition, the HA-5033 offers a minimum slew rate of 1000V/μs.

This device is fabricated using the HARRIS dielectric isolation process. Reduced parasitic capacitance and leakage currents along with improved high frequency PNP transistor performance are among the benefits derived from the superior electrical isolation of the D.I. process.

Available in a 12 pin (TO-8) metal can or an 8 pin epoxy mini-dip, the HA-5033-2 is specified over the military temperature range of -55°C to +125°C. The HA-5033-5 is characterized over the commerical temperature range of 0°C to +75°C.

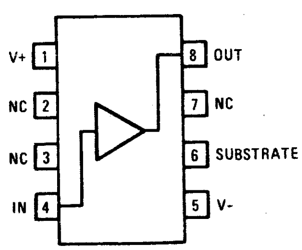
PINOUT

VIDEO BUFFER PINOUT



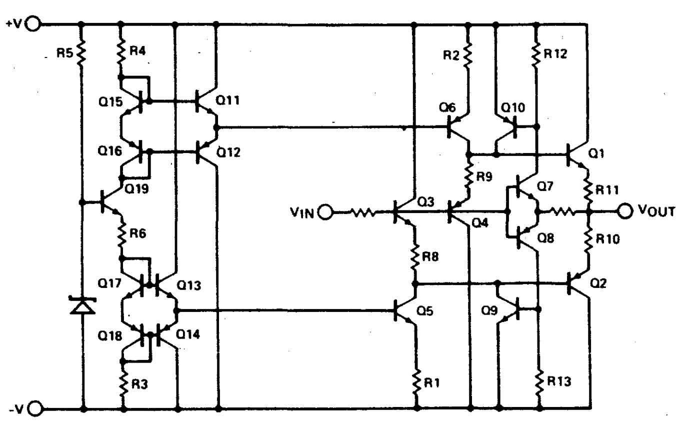
METAL CAN PACKAGE

TOP VIEWS



MINI - DIP

SCHEMATIC



LINEAR

Harris Semiconductor

HARRIS

HA-23080

Operational Transconductance Amplifier

Preliminary

FEATURES

- LOW OFFSET VOLTAGE 0.3mV
- HIGH SLEW RATE 50V/μs
- ADJUSTABLE/GATEABLE GAIN
- LOW OFFSET CURRENT 120nA
- ADJUSTABLE POWER CONSUMPTION

APPLICATIONS

- USE AS BUILDING BLOCKS FOR:
- MULTIPLEXERS
- SAMPLE AND HOLD CIRCUITS
- COMPARATORS
- VOLTAGE FOLLOWERS

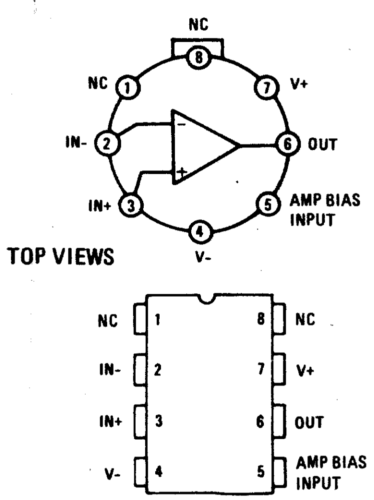
DESCRIPTION

HA-23080 is an operational transconductance amplifier offering an unique blend of DC and AC electrical characteristics coupled with a bias input control for additional versatility. Fabricated using Harris Semiconductor's standard dielectric isolation process, these gateable-gain blocks provide input characteristics such as 0.3mV offset voltage, 120nA offset current and 150μV/V offset voltage sensitivity. Combined with these input characteristics are outstanding dynamic specifications including 50V/μs slew rate and 2MHz bandwidth.

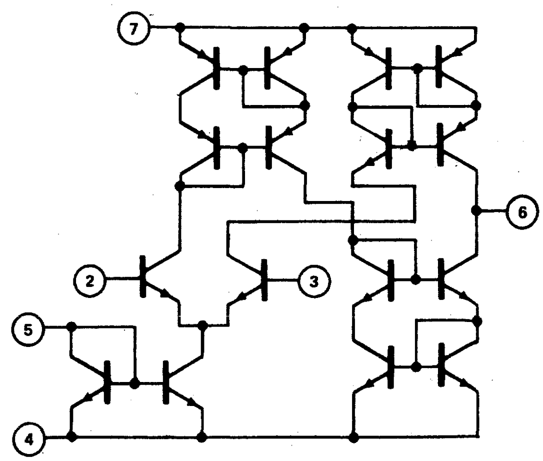
Using these features plus the flexibility afforded by the amplifier bias input, HA-23080 may be easily employed as the main component in multiplexer, comparator, multiplier, and sample/hold designs. This OTA is also useful as a fast voltage follower.

Using the popular operational amplifier pinout, HA-23080 comes available in 8 pin (TO-99) cans and 8 pin cerdips. Its specified temperature range is 0°C to +75°C for -5 and -55°C to +125°C for -2.

PINOUT



SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V- Terminals	36V	Power Dissipation	125mW
Differential Input Voltage	±5V	Operating Temperature Range	
Common Mode Input Voltage	V+ to V-	HA-23080-2	$-55^oC \leq T_A \leq +125^oC$
Input Signal Current	1mA	HA-23080-5	$0^oC \leq T_A \leq +75^oC$
Amplifier Bias Current	2mA	Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$
Output Short Circuit Duration	Indefinite		

ELECTRICAL CHARACTERISTICS V+ = 15V, V- = -15V

$I_{ABC} = 500\mu A$ (Unless Indicated Otherwise) (Note 2)

PARAMETER	TEMP.	HA-23080-2/-5 MINIMUM	TYPICAL	MAXIMUM	UNITS
INPUT CHARACTERISTICS					
Offset Voltage – $I_{ABC} = 5\mu A$	+25°C		0.3	2	mV
			0.4	2	mV
	Full			5	mV
Offset Voltage Change $I_{ABC} = 5\mu A$ to $I_{ABC} = 500\mu A$	+25°C		0.1	3	mV
Average Offset Voltage Drift – $I_{ABC} = 100\mu A$	Full		3	18	μV/°C
Bias Current	+25°C		2	5	μA
	Full			8	μA
$I_{ABC} = 500nA$	+25°C		2	5	nA
Offset Current	+25°C		0.12	0.6	nA
Common Mode Range	+25°C	±12	±13.6		V
Differential Input Current $I_{ABC} = 0$, $V_{DIFF} = 4V$	+25°C		0.008	5	nA
Leakage Current (See Test Circuit) $I_{ABC} = 0$, $V_{TP} = 0V$	+25°C		0.08	5	nA
$I_{ABC} = 0$, $V_{TP} = 36V$	+25°C		0.3	5	nA
Input Capacitance (Note 3)	+25°C		3.6		pF
Input Resistance	+25°C	10	26		kΩ
TRANSFER CHARACTERISTICS					
Forward Transconductance (Large Signal)	+25°C	7700	9900	15000	μmho
	Full	4000			μmho
Common Mode Rejection Ratio	+25°C	80	110		dB
Open Loop Bandwidth	+25°C		20		MHz
OUTPUT CHARACTERISTICS					
Output Voltage Swing (Note 4) – $I_{ABC} = 5\mu A$	+25°C	±12	±13.8		V
	+25°C	±12	±13.5		V
Output Current (Note 5) – $I_{ABC} = 5\mu A$	+25°C	3	5	7	μA
	+25°C	350	500	750	μA
	Full	300			μA
Output Capacitance (Note 3)	+25°C		5.6		pF
Output Resistance	+25°C		15		MΩ
Input-to-Output Capacitance (Note 3)	+25°C		0.024		pF
TRANSIENT RESPONSE (See Test Circuit)					
Slew Rate – Compensated	+25°C		50		V/μs
Uncompensated	+25°C		75		V/μs
NOISE CHARACTERISTICS					
Total Input Noise Voltage (Note 6)	+25°C			12	μVPEAK
POWER SUPPLY CHARACTERISTICS					
Supply Current	+25°C	0.8	1	1.5	mA
Input Offset Voltage Sensitivity	+25°C			150	μV/V
Amplifier Bias Voltage	+25°C		0.71		V

NOTES:

1. Absolute maximum ratings are limiting values applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. I_{ABC} (Amplifier Bias Current) The current supplied to the amplifier bias terminal (Pin 5) to establish its operating point.
3. f = 1MHz
4. $R_L = \infty$
5. $R_L = 0$
6. $V_S = \pm 8.5V$, $I_{ABC} = 500nA$, Bandwidth = 1kHz, $R_{SOURCE} = 100k\Omega$, Test Time = 30 sec.

LINEAR

Harris Semiconductor

HARRIS

HC-5502

SLIC-LC Subscriber Line Interface Circuit

FEATURES

- MONOLITHIC INTEGRATED DEVICE
- UNIQUE DI HIGH VOLTAGE PROCESS
- COMPATIBLE WITH WORLDWIDE PABX PERFORMANCE REQUIREMENTS
- CONTROLLED SUPPLY OF BATTERY FEED CURRENT FOR SHORT LOOPS
- INTERNAL RING RELAY DRIVER
- LOW POWER CONSUMPTION DURING STANDBY
- SWITCH HOOK, GROUND KEY AND RING TRIP DETECTION FUNCTIONS
- SELECTIVE DENIAL OF POWER TO SUBSCRIBER LOOPS

APPLICATIONS

- SOLID STATE LINE INTERFACE CIRCUIT FOR ANALOG AND DIGITAL PBX SYSTEMS

DESCRIPTION

The HARRIS SLIC-LC incorporates many of the BORSHT functions on a single IC chip. This includes DC battery feed, a ring relay driver, supervisory and hybrid functions. Using the unique HARRIS dielectric isolation process, the SLIC-LC can operate directly with a wide range of station battery voltagees.

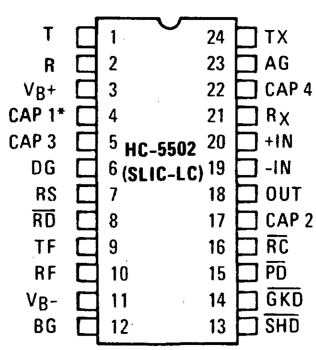
The SLIC-LC also provides selective denial of power. If the PABX system becomes overloaded during an emergency, the SLIC-LC will provide system protection by denying power to selected subscriber loops.

The HARRIS SLIC-LC is ideally suited in the design of new digital PABX systems, by eliminating bulky, expensive hybrid transformers.

SLIC-LC is available in either a 24 pin dual-in-line plastic or ceramic package.

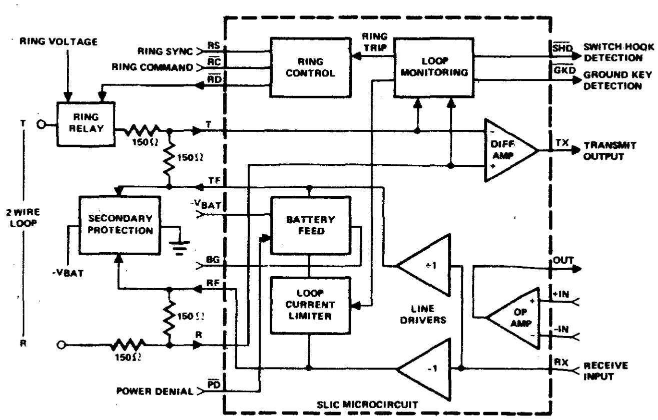
PINOUT

TOP VIEW



*Optional

FUNCTIONAL DIAGRAM



HARRIS

HC-5504

SLIC-LC Subscriber Line Interface Circuit

FEATURES

- MONOLITHIC INTEGRATED DEVICE
- UNIQUE DI HIGH VOLTAGE PROCESS
- COMPATIBLE WITH WORLDWIDE PABX PERFORMANCE REQUIREMENTS
- CONTROLLED SUPPLY OF BATTERY FEED CURRENT FOR SHORT LOOPS
- INTERNAL RING RELAY DRIVER
- ALLOWS INTERFACING WITH NEGATIVE SUPERIMPOSED RINGING SYSTEMS
- LOW POWER CONSUMPTION DURING STANDBY
- SWITCH HOOK, GROUND KEY AND RING TRIP DETECTION FUNCTIONS
- SELECTIVE DENIAL OF POWER TO SUBSCRIBER LOOPS

APPLICATIONS

- SOLID STATE LINE INTERFACE CIRCUIT FOR ANALOG AND DIGITAL PBX SYSTEMS

DESCRIPTION

The HARRIS SLIC-LC incorporates many of the BORSHT functions on a single IC chip. This includes DC battery feed, a ring relay driver, supervisory and hybrid functions. Using the unique HARRIS dielectric isolation process, the SLIC-LC can operate directly with a wide range of station battery voltages.

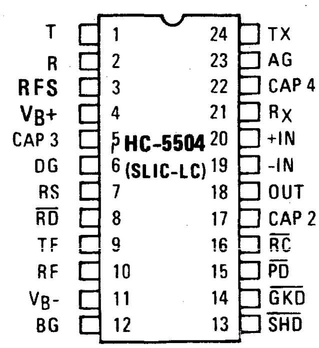
The SLIC-LC also provides selective denial of power. If the PABX system becomes overloaded during an emergency, the SLIC-LC will provide system protection by denying power to selected subscriber loops.

The HARRIS SLIC-LC is ideally suited for the design of new PABX systems, by eliminating bulky, expensive hybrid transformers.

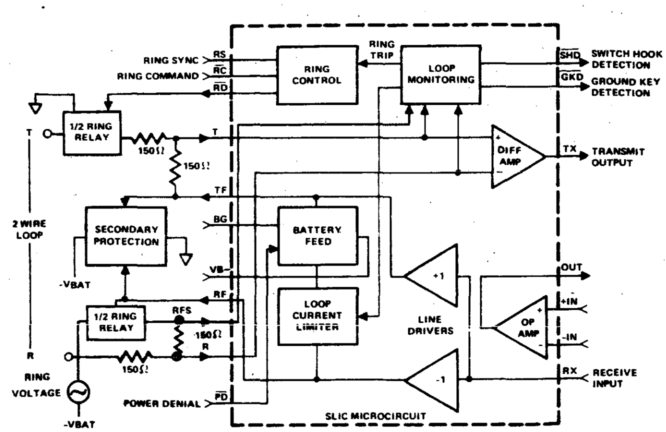
SLIC-LC is available in either a 24 pin dual-in-line plastic or ceramic package. The SLIC-LC is also available in die form.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



HARRIS

HC-5512/5512A

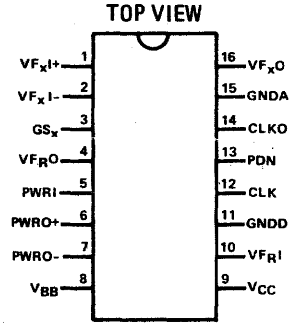
PCM Monolithic Filter

FEATURES

- EXCEEDS ALL D3/D4 AND CCITT SPECIFICATIONS
- +5V, -5V POWER SUPPLIES
- LOW POWER CONSUMPTION:
  45mW (600Ω 0dBm LOAD)
  30mW (POWER AMPS DISABLED)
- POWER DOWN MODE: 0.5mW
- 20dB GAIN ADJUST RANGE
- NO EXTERNAL ANTI-ALIASING COMPONENTS
- SIN x/x CORRECTION IN RECEIVE FILTER
- 50/60Hz REJECTION IN TRANSMIT FILTER
- TTL AND CMOS COMPATIBLE LOGIC
- ALL INPUT PROTECTED AGAINST STATIC DISCHARGE DUE TO HANDLING

PINOUT

DUAL-IN-LINE PACKAGE
TOP VIEW



DESCRIPTION

The HC-5512/HC-5512A filter is a monolithic circuit containing both transmit and receive filters specifically designed for PCM CODEC filtering applications in 8kHz sampled systems.

The filter is manufactured using double-poly silicon gate CMOS technology. Switched capacitor integrators are used to simulate classical LC ladder filters which exhibit low component sensitivity.

TRANSMIT FILTER STAGE

The transmit filter is a fifth order elliptic low pass filter in series with a fourth order Chebyshev high pass filter. It provides a flat response in the passband and rejection of signals below 200Hz and above 3.4kHz.

RECEIVE FILTER STAGE

The receive filter is a fifth order elliptic low pass filter designed to reconstruct the voice signal from the decoded/demultiplexed signal which, as a result of the sampling process, is a stair-step signal having the inherent sin x/x frequency response. The receive filter approximates the function required to compensate for the degraded frequency response and restore the flat passband response.

FUNCTIONAL DIAGRAM

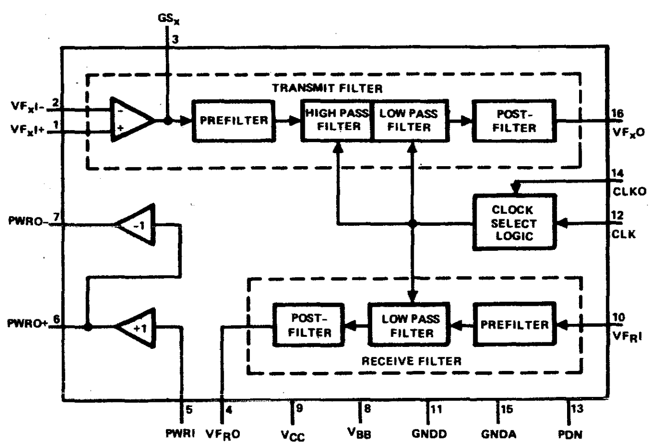


FIGURE 1

HARRIS

HC-55564

All-Digital Continuously Variable Slope Delta Modulator (CVSD)

Preliminary

FEATURES

- REQUIRES FEW EXTERNAL PARTS
- LOW POWER DRAIN: 6mW FROM SINGLE 4.5V-7V SUPPLY
- TIME CONSTANTS DETERMINED BY CLOCK FREQUENCY; NO CALIBRATION OR DRIFT PROBLEMS; AUTOMATIC OFFSET ADJUSTMENT
- HALF DUPLEX OPERATION UNDER DIGITAL CONTROL
- FILTER RESET UNDER DIGITAL CONTROL
- AUTOMATIC OVERLOAD RECOVERY
- AUTOMATIC "QUIET" PATTERN GENERATION
- AGC CONTROL SIGNAL AVAILABLE

APPLICATIONS

- VOICE TRANSMISSION OVER DATA CHANNELS
- VOICE ENCRYPTION/SCRAMBLING
- VOICE I/O FOR DIGITAL SYSTEMS AND SPEECH SYNTHESIS
- AUDIO MANIPULATIONS: DELAY LINES, TIME COMPRESSION, ECHO GENERATION/SUPPRESSION, SPECIAL EFFECTS, ETC.

DESCRIPTION

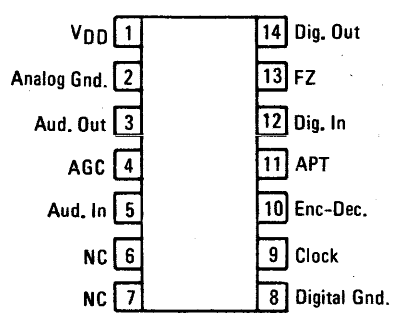
The HC-55564 is a half duplex modulator/demodulator CMOS integrated circuit used to convert voice signals into serial NRZ digital data, and to reconvert that data into voice. The conversion is by delta modulation, using the continuously variable slope (CVSD) method of companding.

While the signals are compatible with other CVSD circuits, the internal design is unique. The analog loop filters have been replaced by digital filters, using very low power, and requiring no external timing components. This approach allows inclusion of many desirable features which would be difficult to implement using other approaches.

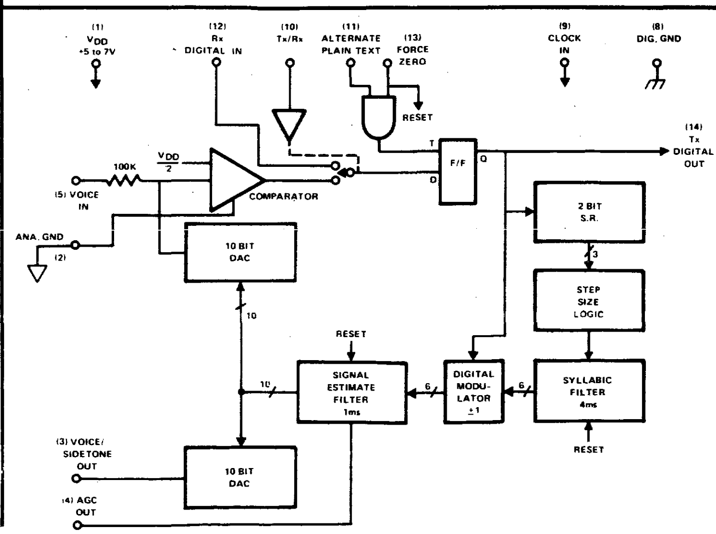
The HC-55564 is usable from 9K bits/sec to above 64K bits/sec. The unit is available in a 14 pin ceramic or plastic DIP package in commercial and military temperature ranges including MIL-STD 883-B processing.

PINOUT

Top View



FUNCTIONAL DIAGRAM



HARRIS

HC-55536

All-Digital Continuously Variable Slope Delta Demodulator (CVSD)

FEATURES

- REQUIRES FEWER EXTERNAL PARTS
- LOW POWER DRAIN: 6mW FROM SINGLE 5V-7V SUPPLY
- TIME CONSTANTS DETERMINED BY CLOCK FREQUENCY; NO CALIBRATION OR DRIFT PROBLEMS; AUTOMATIC OFFSET ADJUSTMENT
- FILTER RESET BY DIGITAL CONTROL
- AUTOMATIC OVERLOAD RECOVERY
- AUTOMATIC "QUIET" PATTERN GENERATION

APPLICATIONS

- SPEECH SYNTHESIS
- AUDIO MANIPULATIONS; DELAY LINES, ECHO GENERATION/SUPPRESSION, SPECIAL EFFECTS, ETC.

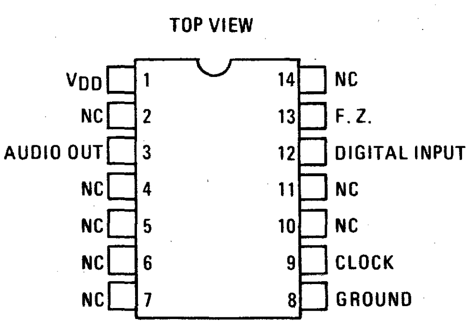
DESCRIPTION

The HC-55536 is a CMOS integrated circuit used to convert serial NRZ digital data to an analog (voice) signal. Conversion is by delta demodulation, using the continuously variable slope (CVSD) method.

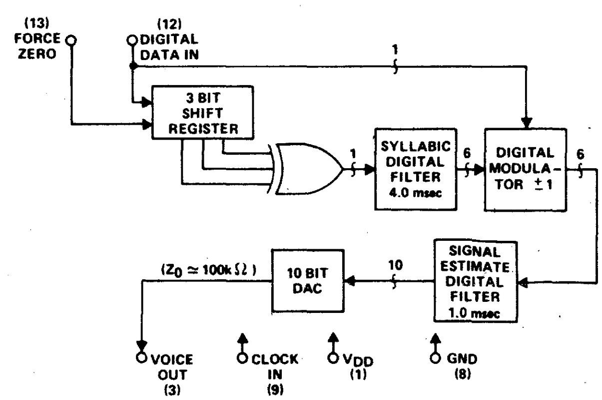
While signals are compatible with other CVSD circuits, the internal design is unique. The analog loop filters have been replaced by digital filters which use very low power and require no external timing components. This digital approach allows inclusion of many desirable features, which otherwise would be difficult to implement. Internal time constants are optimized for a 16K bit/sec data rate. However, the device is usable from 9K bits/sec to above 64K bits/sec.

The package is a 14 pin DIP, available in plastic (0°C to +70°C) or ceramic (-40°C to +85°C). Chips are available, probe tested at +25°C.

PINOUT AND PIN DESCRIPTION



FUNCTIONAL DIAGRAM



HARRIS

HV-1000/1000A

Induction Motor Energy Saver

FEATURES

- OPERATES DIRECTLY OFF 120V/240V AC LINE – NO POWER SUPPLY REQUIRED
- 50Hz OR 60Hz OPERATION
- PRODUCES POWER SAVINGS FROM 10% TO 50% FOR MOTORS WITH LIGHT OR VARIABLE LOADS
- SCR OUTPUT STAGE TRIGGERS TRIAC DIRECTLY
- LOAD ANTICIPATOR SENSES SHOCK LOADS AND RESPONDS INSTANTLY WITH FULL POWER
- WITHSTANDS LINE SURGES TO 3500V
- CAUSES MOTOR TO RUN QUIETER, COOLER
- CAN BE MOUNTED INSIDE MOTOR
- NEEDS ONLY 3 RESISTORS, 3 CAPACITORS AND A TRIAC TO ASSEMBLE COMPLETE CONTROLLER

DESCRIPTION

The HV-1000 and HV-1000A are energy saving induction motor control circuits designed to reduce the power consumed by single phase induction motors. HV-1000 is for 120V AC use and HV-1000A for 240V AC use.

The controller circuit senses the load on the motor and then controls a TRIAC to apply reduced voltage to lightly loaded motors, full voltage to heavily loaded motors.

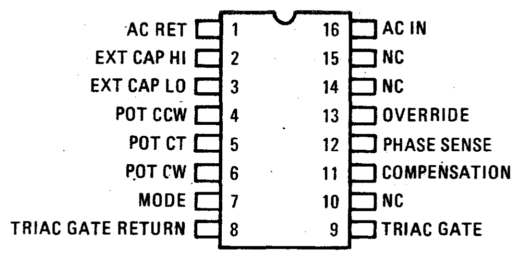
The HV-1000/1000A are available in a 16 lead plastic DIP. Ideal for mounting inside induction motors, they can also be mounted in a heat sunk circuit box for external, after market application.

APPLICATIONS

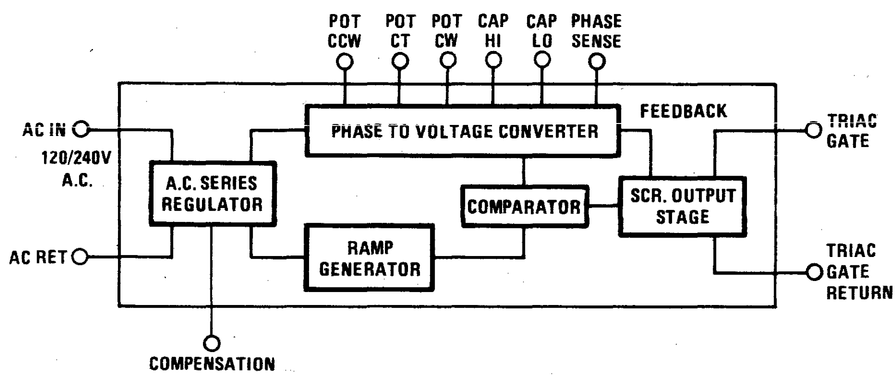
- MACHINE TOOLS
- INDUSTRIAL SEWING MACHINES
- HEAT PUMPS
- PRESSES
- CONVEYORS
- DISC PACK DRIVES
  - ► ANY APPLICATION WHERE FOR SOME OF THE TIME THE MOTOR IS DRIVING LESS THAN ITS RATED LOAD

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



Operational Amplifiers — General Purpose

Type	Description	V_{OS} (mV)	I_b (nA)	A_{VOL} (V/V)	GBW (typ) (MHz)	I_{SUPP} (mA)	T_A (°C)	Packages*	Remarks
108	Low Level, Uncompensated	2.0	2.0	50,000	1.0	0.6	−55, +125	J, F, T	
108LN	Guaranteed Noise 108	2.0	2.0	50,000	1.0	0.6	−55, +125	T	70nV/$\sqrt{Hz}$ @10Hz
308	Low Level, Uncompensated	7.5	7.0	25,000	1.0	0.8	0, +70	F, J, P, T	
308LN	Guaranteed Noise 308	7.5	7.0	25,000	1.0	0.8	0, +70	T	70nV/$\sqrt{Hz}$ @10Hz
777	General Purpose Comparator	0.7	25	150,000	0.8	2.5	−55, +125	P, T	
777C	General Purpose Comparator	0.7	25	150,000	0.8	2.5	0, +70	P, T	
8008M	Low Bias Current, Compensated	5.0	10	20,000	1.0	2.8	−55, +125	J, T	
8008C	Low Bias Current, Compensated	6.0	25	20,000	1.0	2.8	0, +70	J, P, T	
LH2108	Dual Super Beta	2.0	3.0	25,000	1.0	0.4	−55 to +125	D	Build to Order
LH2108A	Dual Super Beta	0.5	3.0	40,000	1.0	0.4	−55 to +125	D	Build to Order
LH2308	Dual Super Beta	7.5	10	15,000	1.0	0.4	0 to +70	D	Build to Order
LH2308A	Dual Super Beta	0.5	10	60,000	1.0	0.4	0 to +70	D	Build to Order

Operational Amplifiers — Low Power Programmable

Type	Description	V_{OS} (mV)	I_b (nA)	A_{VOL} (V/V)	GBW (MHz)	I_{SUPP} (μA)	@ I_{set} (μA)	@ V_s (V)	T_A (°C)	Packages*
8021M	Programmable, Compensated	3.0	20	50,000	0.27	40	30	+6.0	−55 to +125	J, T
8021C	Programmable, Compensated	6.0	30	50,000	0.27	50	30	+6.0	0, +70	T
8022M	Dual 8021M	3.0	20	50,000	0.27	40	30	+6.0	−55 to +125	J, F
8022C	Dual 8021C	6.0	30	50,000	0.27	50	30	+6.0	0, +70	J, P
8023M	Triple 8021M	3.0	20	50,000	0.27	40	30	+6.0	−55 to +125	J
8023C	Triple 8021C	6.0	30	50,000	0.27	50	30	+6.0	0 to +70	J, P
7611	CMOS	2.0	0.001	100,000	1.4	20	–	–	C,I,M	T, P
7612	CMOS, Extended CMVR	2.0	0.001	100,000	1.4	20	–	–	C,I,M	T, P
7613	CMOS, Input Protected to ± 200V	2.0	0.001	100,000	1.4	20	–	–	C,I,M	T, P
7631	CMOS, Triple	5.0	0.001	100,000	1.4	60	–	–	C,I,M	D, P
7632	CMOS, Triple, Uncompensated	5.0	0.001	100,000	1.4	60	–	–	C,I,M	D, P

Operational Amplifiers — CMOS

Type	Description	Compensation	Offset Null	V_{OS} Selection	I_{OS}	I_B	Output Swing	Input CMR	Packages*
7611	Single, Selectable I_Q	Internal	Yes	2, 5, 15mV	0.5pA	1pA	V_{SUPP}−100mV	V_{SUPP}−100mV	P, T
7612	Single, Selectable I_Q Extended CMVR	Internal	Yes	2, 5, 15mV	0.5pA	1pA	V_{SUPP}+300mV	V_{SUPP}−100mV	P, T
7613	Single, Selectable I_Q Input Protected to ±200V	Internal	Yes	2, 5, 15mV	0.5pA	1pA	V_{SUPP}−100mV	V_{SUPP}−100mV	P, T
7614	Single, Fixed I_Q	External	Yes	2, 5, 15mV	0.5pA	1pA	V_{SUPP}−100mV	V_{SUPP}−100mV	P, T
7615	Single, Fixed I_Q Input Protected	External	Yes	2, 5, 15mV	0.5pA	1pA	V_{SUPP}−100mV	V_{SUPP}−100mV	P, T
7621	Dual, Fixed I_Q	Internal	No	2, 5, 15mV	0.5pA	1pA	V_{SUPP}−100mV	V_{SUPP}−100mV	P, T
7622	Dual, Fixed I_Q	Internal	Yes	2, 5, 15mV	0.5pA	1pA	V_{SUPP}−100mV	V_{SUPP}−100mV	P, J
7631	Triple, Selectable I_Q	Internal	No	5, 10, 20mV	0.5pA	1pA	V_{SUPP}−100mV	V_{SUPP}−100mV	P, J
7632	Triple, Selectable I_Q	None	No	5, 10, 20mV	0.5pA	1pA	V_{SUPP}−100mV	V_{SUPP}−100mV	P, J
7641	Quad, Fixed I_Q	Internal	No	5, 10, 20mV	0.5pA	1pA	V_{SUPP}−100mV	V_{SUPP}−100mV	P, J
7642	Quad, Fixed I_Q	Internal	No	5, 10, 20mV	0.5pA	1pA	V_{SUPP}−100mV	V_{SUPP}−100mV	P, J
7650	Chopper Stabilized	Internal	–	0.01mV	–	10pA	V_{SUPP}-100mV	–	P, T

*Package Key: D—Solder lid side brazed ceramic dual-in-line. F—Ceramic flat package. J—Glass frit seal ceramic dual-in-line. P—Plastic dual-in-line. T—Metal can.

Operational Amplifiers — FET Input (also see Operational Amplifier, CMOS)

Type	Description	V_{OS} (mV)	I_b (μA)	A_{VOL} (V/V)	GBW (typ) (MHz)	Slew Rate (V/μs)	I_{SUPP} (mA)	T_A (°C)	Packages*	Remarks
8007M	General Purpose, Compensated	20	20	50,000	1.0	6	5.2	−55, +125	T	All BIFET amplifiers offer low noise—see data sheets
8007AM	8007M, Low I_b	30	1.0	20,000	1.0	2.5	6	−55, +125	T	
8007C	General Purpose, Compensated	50	50	20,000	1.0	6	6	0, +70	T	
8007AC	8007C, Low I_b	30	1.0	20,000	1.0	2.5	6	0, +70	T	
8043M	Dual 8007M	20	20	50,000	1.0	6.0	6	−55, +125	J	
8043C	Dual 8007C	50	50	20,000	1.0	6.0	6.8	−55, +125	J, P	
8500	MOSFET Input, Compensated	50	0.1	20,000	0.7	0.5	2.7	−25, +85	T	
8500A	MOSFET Input, Super Low I_b	50	0.01	20,000	0.7	0.5	2.7	−25, +85	T	

Operational Amplifiers — High Performance

Type	Description	V_{OS} (mV)	I_b (pA)	A_{VOL} (V/V)	GBW (MHz)	Slew Rate (V/μs)	I_{SUPP} (mA)	T_A (°C)	Packages*
8017M	High Speed, Inverting	5.0	200	25,000	10	130	7.0	−55, +125	T, F
8017C	High Speed, Inverting	7.0	200	25,000	10	130	8.0	0, +70	T, F
OP-05	Low Bias, Low Drift	0.07	700	500,000	0.6	0.2	4.0	−55, +125	T, J
OP-07	Ultra Stable	0.025	300	500,000	0.6	0.17	4.0	−55, +125	T, J

Operational Amplifiers—High Slew Rate

Type	Description	V_{OS} (mV)	I_b (pA)	A_{VOL} (V/V)	GBW (MHz)	Slew Rate (V/μS)	I_{SUPP} (mA)	T_A (°C)	Packages*
8017M	High speed, inverting	5.0	200	25,000	10	130	7.0	-55 + 125	T,F
8017C	High speed, inverting	7.0	200	25,000	10	130	8.0	0 + 70	T,F

*Package Key: D—Solder lid side brazed ceramic dual-in-line. F—Ceramic flat package. J—Glass frit seal ceramic dual-in-line. P—Plastic dual-in-line. T—Metal can.

Precision Operational Amplifiers, V_{SUPP} = ±2V to ±8V

Type	Description	V_{OS} (μV)	ΔV_{OS} (μV/°C)	ΔV_{OS} (μV/year)	A_V (dB min)	Slew Rate Rate (V/μs)	I_{BIAS} (pA)	Packages*	T_A (°C)
ICL7650C	Chopper Stabilized	±1	±0.01	100nV/$\sqrt{month}$	126	2.5	+1.5	J, P, T	0 to +70
ICL7650I	Chopper Stabilized	±1	±0.01	100nV/$\sqrt{month}$	126	2.5	+1.5	J, P, T	−25 to +85
ICL7652	Chopper Stabilized	±1	±0.7	100nV/$\sqrt{month}$	120	0.5	+1.5	J, P, T	−20 to +85

Precision Instrumentation Amplifiers, V_{SUPP} = ±2V to ±5V, I_{SUPP} = 1.7mA

Type	Description	V_{OS} (μV)	ΔV_{OS} (μV/°C)	ΔV_{OS} (μV/year)	A_V (dB min)	Packages*	T_A (°C)
ICL7605C	Compensated	±2	±0.01	0.5	90	J, P	0 to +70
ICL7605I	Compensated	±2	±0.01	0.5	90	J, P	−25 to +85
ICL7605M	Compensated	±2	±0.05	0.5	90	J, P	−55 to +125
ICL7606C	Uncompensated	±2	±0.01	0.5	90	J, P	0 to +70
ICL7606I	Uncompensated	±2	±0.01	0.5	90	J, P	−25 to +85
ICL7606M	Uncompensated	±2	±0.05	0.5	90	J, P	−55 to +125

Precision Voltage References

Type	Description	
ICL8069	Low Voltage Reference	The ICL8069 is a 1.2V temperature compensated voltage reference. It uses the band-gap principle to achieve excellent stability and low noise at reverse currents down to 50μA.
ICL8075-9	Ultra Precision Temperature Stabilized Voltage References	The ICL8075-9 is a family of precision laser-trimmed voltage references that incorporate a substrate heater to produce extremely low overall voltage temperature coefficients. The series of devices is produced so that exact voltages are available for the most popular A/D and D/A converters. This avoids the necessity to perform adjustments in most cases, and reduces the problems with trim range and temperature coefficient loss in all others.

Video Amplifiers

Type	Description	Gains (typ) (V/V)	Bandwidths (typ) (MHz)	e_n μV(rms)	Output Offset (V)	I_{SUPP} (mA)	T_A (°C)	Packages*
NE/SE592	Gain Selectable Video Amp	400, 100, 10	40, 90	12	0.75	10	0, +70/−55, +125	J,T
NE592-8	Gain Selectable Video Amp	400, 100, 10	40	12	0.75	10	0, +70	P

*Package Key: D—Solder lid side brazed ceramic dual-in-line. F—Ceramic flat package. J—Glass frit seal ceramic dual-in-line. P—Plastic dual-in-line. T—Metal can.

Comparators

Type	Description	V_{OS} (mV)	I_b (nA)	A_V (V/mV)	t_{pd} (ns)(typ)	I_{SUPP} (mA)	V_{OL} (V)	I_{OL} (mA)	T_A (°C)	Packages*
8001M	Low Power Comparator	3	100	15	250	2	0.5	2	−55, +125	T
8001C	Low Power Comparator	5	250	15	250	2	0.4	2	0, +70	T

Notes: t_{pd} measured for 100mV step with 5mV overdrive.
I_{SUPP} measured for V_{SUPP} + ± 15V.

Power Amplifiers

Type	Description	Use	Output Current (A)	Output Swing (V)	V_{OS} (mV)	I_b (nA)	A_{VOL} (V/V)	Slew Rate (V/μs)	Quiescent I_{SUPP} (mA)	T_A (°C)
ICH8510M	Hybrid Power Amplifier		1.0	±26	3.0	250	100,000	0.5	40	−55, +125
ICH8510I	Hybrid Power Amplifier		1.0	±26	6.0	500	100,000	0.5	50	−25, +85
ICH8515I	Hybrid Power Amplifier		1.25	±12	6.0	500	100,000	0.5	80	−20°C - +85°C
ICH8515M	Hybrid Power Amplifier	Servo	1.5	±12	3.0	250	100,000	0.5	70	−55°C - +125°C
ICH8520M	Hybrid Power Amplifier	and	2.0	±26	3.0	250	100,000	0.5	40	−55, +125
ICH8520I	Hybrid Power Amplifier	Actuator	2.0	±26	6.0	500	100,000	0.5	50	−25, +85
ICH8530M	Hybrid Power Amplifier		2.7	±25	3.0	250	100,000	0.5	40	−55, +125
ICH8530I	Hybrid Power Amplifier	Power	2.7	±25	6.0	500	100,000	0.5	50	−25, +85
ICL8063C	Monolithic Power Amplifier	Transistors	2.0	±27	50		6		250	0, +70
ICL8063M	Monolithic Power Amplifier		2.0	±27	75		6		300	−55, +125

Note 1: Specifications apply at ±30V supplies.
Note 2: All units packaged in 8 lead TO-3 can.
Note 3: Fully protected against inductive current flow.
Note 4: Externally settable output current limiting.

*Package Key: D—Solder lid side brazed ceramic dual-in-line. F—Ceramic flat package. J—Glass frit seal ceramic dual-in-line. P—Plastic dual-in-line. T—Metal can.

LINEAR

Intersil

INTERSIL

Special Function Circuits

Type	Description	Accuracy	V_{SUPP} (V)	T_A (°C)	Packages*
AD590	Temperature transducer—output linear at 1μA/°K	±1°C	40 to 30	−55 to +150	F, H
ICL7667C	Dual Power MOS Driver	—	22	0, +70	J, P, T
ICL7667M	Dual Power MOS Driver	—	22	−55, +125	J, T
8013AM	Four quadrant multiplier. Output proportional to algebraic products	±0.5%	±15	−55, +125	T
8013BM	of two input signals. Features ±0.5% accuracy; internal op amp	±1.0%	±15	−55, +125	T
8013CM	for level shift, division and square root functions; full ±10V	±2.0%	±15	−55, +125	T
8013AC	input/output range; 1MHz bandwidth.	±0.5%	±15	0, +70	T
8013BC		±1.0%	±15	0, +70	T
8013CC		±2.0%	±15	0, +70	T
8038AM	Simultaneous Sine, Square, and Triangle wave outputs T^2L com-	1.5%	±5 to ±15	−55, +125	J
8038AC	patible to 28V over frequency range from 0.01Hz to 1.0MHz.	1.5%	±5 to ±15	0, +70	J
8038BM	Low distortion (< 1%); high linearity (0.1%); low frequency drift with temperature (50ppm/°C max); variable duty cycle (2%-98%).	3.0%	±5 to ±15	−55, +125	J
8038BC		3.0%	±5 to ±15	0, +70	P
8038CC	External frequency modulation.	5.0%	±5 to ±15	0, +70	P
8048BC	Log amp 1V/decade (Adjustable). 120dB range.	±30mV	±15	0, +70	J, P
8048CC	with current input. Error referred to output.	±60mV	±15	0, +70	J, P
8049BC	Antilog amplifier adjustable scale factor.	±10mV	±15	0, +70	J, P
8049CC	Error referred to input.	±30mV	±15	0, +70	J, P
8211M	Micropower voltage detector/indicator/voltage regulator/		2 to 30	−55, +125	T
8211C	programmable zener. Contains 1.15V micropower reference		2 to 30	0, +70	P, T
8212M	plus comparator and hysteresis output. Main output		2 to 30	−55, +125	T
8212C	inverting (8212) or non-inverting (8211).		2 to 30	0, +70	P, T

Note: All parameters are specified at $V_{SUPP} = \pm 15V$ and $T_A = +25°C$ unless otherwise noted.

*Package Key: D—Solder lid side brazed ceramic dual-in-line. F—Ceramic flat package. J—Glass frit seal ceramic dual-in-line. P—Plastic dual-in-line. T—Metal can.

LINEAR

Intersil

CMOS Power Supply Circuits

Type	Description	
ICL7660	Voltage Converter	The ICL7660 performs the complete supply voltage conversion from positive to negative for an input range of +1.5V to +10.0V, resulting in complementary output voltages of −1.5V to −10.0V.
ICL7663 ICL7664	Positive Regulator Negative Regulator	The ICL7663 (positive) and ICL7664 (negative) series regulators are low-power, high-efficiency devices which accept inputs from 1.6V to 16V and provide adjustable outputs over the same range at currents up to 40mA. Operating current is typically less than 40μA, regardless of load.
ICL7665	Programmable Micropower Voltage Detector	The ICL7665 contains two individually programmable voltage detectors on a single chip. Requiring only ~3μA for operation, the device is intended for battery-operated systems and instruments which require high or low voltage warnings, settable trip points, or fault monitoring and correction.

INTERSIL

ICH8500/A
Ultra Low Bias Current Operational Amplifier

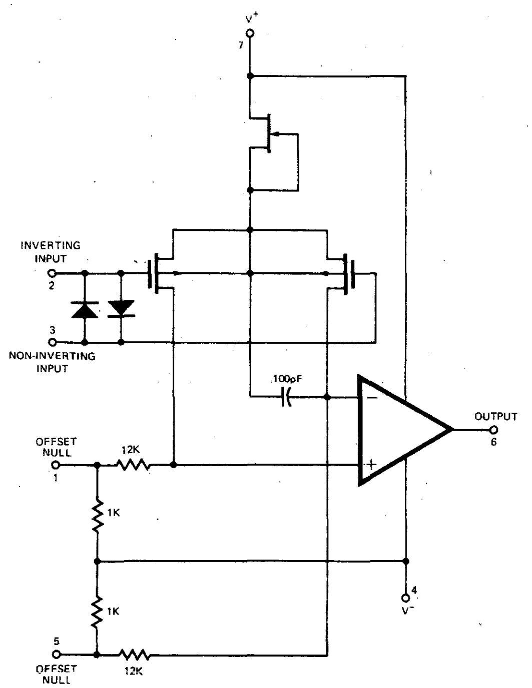
FEATURES

- Input diode protection
- Input bias current less than 0.01 pA at all operating temperatures
- No frequency compensation required
- Offset voltage null capability
- Short circuit protection
- Low power consumption

APPLICATIONS

- Femto Ammeter
- Electrometers
- Long time integrators
- Flame detectors
- pH meter
- Proximity detector
- Sample and Hold Circuits

SCHEMATIC DIAGRAM



GENERAL DESCRIPTION

The ICM8500 and ICH8500A are hybrid circuits designed for ultra low input bias current operational amplifier applications. They are ideally suited for analog and electrometer applications where high input resistance and low input current are of prime importance.

Functionally, they are pin for pin identical to the popular 741 monolithic amplifier. These amplifiers are unconditionally stable and the input offset voltage can be adjusted to zero with an external 20k potentiometer. The input bias current for the inverting and non-inverting inputs is 0.1 pA maximum for the ICH8500, and 0.01 pA maximum for the ICH8500A and are constant over the operating temperature range of -25°C to +85°C.

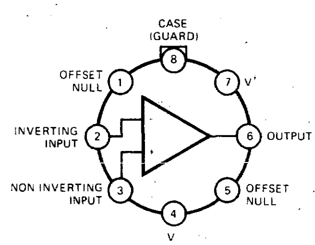
Pin 8 is connected to the case. This permits the designer to operate the case at any desired potential, the key to achieving the ultra low input currents associated with these two amplifiers. Forcing the case to the same potential as the inputs eliminates current flow between the case and the input pins, and leakage currents that may have otherwise existed between any of the other pins and the inputs are intercepted by the case.

ORDERING INFORMATION

ICH 8500A TV

- TV — PACKAGE: TV=TO-99 metal can
- 8500A — DEVICE TYPE
- ICH — INTERSIL HYBRID CIRCUIT

PIN CONFIGURATION (outline dwg TV)



LINEAR

Intersil

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... ±18V
Internal Power Dissipation[1] .... 500 mW
Differential Voltage .... ±0.5V
Storage Temperature .... -65°C to +150°C
Operating Temperature .... -25°C to +85°C
Lead Temperature (Soldering 10 sec) ...... 300°C
Output Short Circuit Duration .... Indefinite

Note: 1. Rating applies for ambient temperature to +70°C.

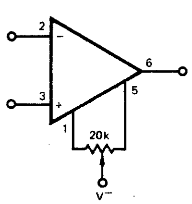
NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified, V_{SUPP} = ±15V)

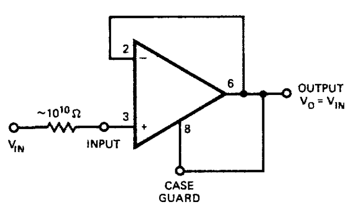
CHARACTERISTICS	SYMBOL	ICH8500 MIN	ICH8500 TYP.	ICH8500 MAX	ICH8500A MIN	ICH8500A TYP	ICH8500A MAX	UNITS	TEST CONDITIONS
Input Leakage Current (Inverting and Non-Inverting)	I_{ILK}			0.1			0.01	pA	Case at same potential as inputs
Input Offset Voltage	V_{OS}			50			50	mV	
Offset Voltage Adjustment Range	$\pm V_{OS}$			±50			±50	mV	20kΩ Potentiometer
Change in Input Offset Voltage Over Temperature	$\Delta V_{OS} / \Delta T$						±5.0 ±5.0	mV mV	+25 to +85°C -25 to +25°C
Common Mode Rejection Ratio	CMRR	60	75		60	75		dB	±5 volts common mode voltage
Output Voltage Swing	$\pm V_O$	±11			±11			V	$R_L \geq 10k\Omega$
Common Mode Voltage Range	CMVR	±10			±10			V	
Large Signal Voltage Gain	A_{VOL}	20,000	10^5		20,000	10^5		—	
Feedback Capacitance	C_{fb}			0.1			0.1	pF	Case guarded
Long Term Input Offset Voltage Stability	$\Delta V_{OS}/\Delta t$			±3.0			±3.0	mV	At 25°C
Slew Rate	SR		0.5			0.5		V/μs	$R_L \geq 2k\Omega$
Input Capacitance	C_{IN}		0.7			0.7		pF	Case guarded
Input Capacitance	C_{IN}		1.5			1.5		pF	Case grounded

CIRCUIT NOTES

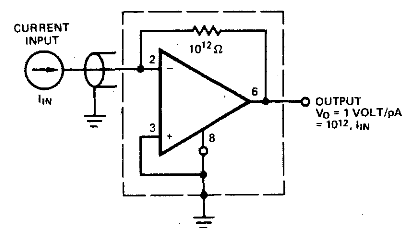
VOLTAGE OFFSET NULL CIRCUIT



VOLTAGE FOLLOWER



LOW LEVEL CURRENT MEASURING CIRCUIT



NOTE: Adjust input offset voltage to 0V ± 10μV before measuring leakage.

INTERSIL

ICH8510/8520/8530 Power Amplifier/ Motor & Actuator Driver

KEY FEATURES:

- Delivers up to 2.7 amps @ 24-28V DC (30V supplies)
- Protected against inductive kick back with internal power limiting
- Programmable current limiting (short circuit protection)
- Package is electrically isolated (allowing easy heat sinking)
- DC gain > 100dB
- 20mA typical standy quiescent current
- Popular 8 pin TO-3 package
- Internal frequency compensation
- Can drive up to 0.1 horsepower motors.

DESCRIPTION:

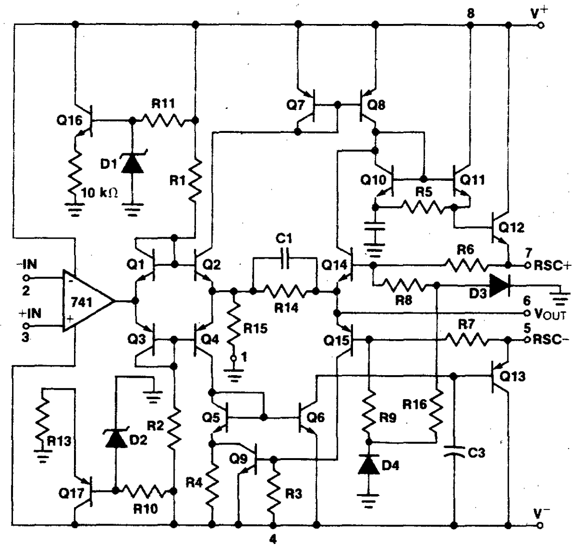
The ICH8510/8520/8530 is a family of hybrid power amplifiers that have been specifically designed to drive linear and rotary actuators, electronic valves, push-pull solenoids, and DC & AC motors.

There are three models available for up to +30V power supply operation: 2.7 amps @ 24 volt output levels, 2 amps @ 24V and 1 amp @ 24V. All amplifiers are protected against shorts to ground by the addition of 2 external protection resistors. For a device operating at lower voltages, see the ICH8515.

The design uses a conventional 741 operational amplifier, a special monolithic driver chip (BL8063), NPN & PNP power transistors, and internal frequency compensating capacitors. The chips are mounted on a beryllium oxide substrate for optimum heat transfer to the metal package; this substrate provides electrical isolation between amplifiers and metal package.

The I.C. power driver chip has built-in regulators to drive the 741 @ typically ±13V supply voltages.

SCHEMATIC DIAGRAM



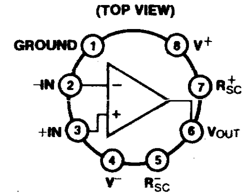
ORDERING INFORMATION

ICH8510 M KA

- Package: KA = 8 lead TO-3 can
- Temperature Range: M = Military −55°C to +125°C; I = Industrial −20°C to +85°C
- Basic Part Number: 8510 = 1A output; 8520 = 2A output; 8530 = 2.7A output

PIN CONFIGURATION (outline dwg KA)

(TOP VIEW)



ICH8510/8520/8530

INTERSIL

ABSOLUTE MAXIMUM RATINGS @ $T_A = 25°C$

Supply Voltage	±32V
Power Dissipation, Safe Operating Area	See Curves
Differential Input Voltage	±30V
Input Voltage	±15V (Note 1)
Peak Output Current	See Curves (Note 2)
Output Short Circuit Duration (to ground)	Continuous (Note 2)
Operating Temperature Range M	−55°C → +125°C
I	−20°C → +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Max Case Temperature	150°C

Note 1: Rating applies to supply voltages of ±15V. For lower supply voltages, $V_{INMAX} = V_{SUPP}$.
Note 2: Ratings apply as long as package dissipation is not exceeded. Device must be mounted on heat sink, see Figures 8 and 12.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL SPECIFICATIONS $T_A = +25°C$. $V_{SUPP} = \pm30V$ (unless otherwise stated)

DESCRIPTION	SYMBOL	CONDITIONS	ICH8510I MIN.	ICH8510I MAX.	ICH8510M MIN.	ICH8510M MAX.	ICH8520I MIN.	ICH8520I MAX.	ICH8520M MIN.	ICH8520M MAX.	ICH8530I MIN.	ICH8530I MAX	ICH8530M MIN.	ICH8530M MAX.	UNITS
Input Offset Voltage Change with Power Dissipation	$\Delta V_{OS}/\Delta P_d$	Mtd. on Wakefield 403 Heat Sink		4		2		4		2		4		2	mV/W
Input Offset Voltage	V_{OS}	$R_S \le 10\ k\Omega$, $P_d \le 1W$	−6	+6	−3	+3	−6	+6	−3	+3	−6	+6	−3	+3	mV
Input Bias Current	I_{BIAS}	$R_S \le 10\ k\Omega$, $P_d \le 1W$		500		250		500		250		500		250	nA
Input Offset Current	I_{OS}	$R_S \le 10\ k\Omega$, $P_d \le 1W$		200		100		200		100		200		100	nA
Large Signal Voltage Gain	A_{VOL}	$R_L = 20\Omega$, $V_O \ge 2/3\ V_{SUPP}$	100		100		100		100		100		100		dB
Input Voltage Range	V_{CMR}		−10	+10	−10	+10	−10	+10	−10	+10	−10	+10	−10	+10	V
Common Mode Rejection Ratio	CMRR	$R_S = 10\ k\Omega$	70		70		70		70		70		70		dB
Power Supply Rejection Ratio	PSRR	$R_S = 10\ k\Omega$	77		77		77		77		77		77		dB
Slew Rate	SR	$C_L = 3\ pF$, $A_V = 1$, $R_L = 10\Omega$, $V_O \ge 2/3\ V_{SUPP}$	0.5		0.5		0.5		0.5		0.5		0.5		V/μs
Output Voltage Swing	V_{OMAX}	$R_L = 20\Omega$, $A_V = 10$	($R_L = 30\Omega$) ±26V		($R_L = 30\Omega$) ±26V		±26V		±26V		±25V		±25V		V
Output Current (3)	I_{MAX}	$R_L = 8\Omega$, $A_V = 10$	1.0		1.0		2.0		2.0		2.7		2.7		A
Power Supply Quiescent Current	I_Q	$R_L = \infty$, $V_{IN} = 0V$		125		100		125		100		125		100	mA

Note 3: See Figure #9 if Power Supplies are less than ±30V.

ELECTRICAL SPECIFICATIONS (continued) $T_A = -55°C$. to $+125°C$.(M) or $T_A = -20°C$. to $+85°C$.(I)

Input Offset Voltage	V_{OS}	$P_d < 1W$	−10	+10	−9	+9	−10	+10	−9	+9	−10	+10	−9	+9	MV
Input Bias Current	I_{BIAS}	$P_d < 1W$		1500		750		1500		750		1500		750	nA
Input Offset Current	I_{OS}			500		200		500		200		500		200	nA
Large Signal Voltage Gain	A_{VOL}	$R_L = 20\Omega$, $\Delta V_O = 2/3\ V_{SUPP}$	90		90		90		90		90		90		dB
Output Voltage Swing	V_{OMAX}	$R_L = 20\Omega$, $A_V = 10$	±24		±24		±24		±24		±24		±24		V
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Without Heat Sink		40		40		40		40		40		40	°C/W
Thermal Resistance Junction to Case	$R_{\theta JC}$			2.5		2.5		2.5		2.5		2.5		2.5	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Mtd. on Wakefield 403 Heat Sink		(Typ.) 4.0		(Typ.) 4.0		(Typ.) 4.0		(Typ.) 4.0		(Typ.) 4.0		(Typ.) 4.0	°C/W
Supply Voltage Range	V_{SUPP}		±18	±30	±18	±30	±18	±30	±18	±30	±18	±30	±18	±30	V

ICL761X/ 762X/763X/764X Low Power CMOS™ Operational Amplifiers

FEATURES

- Wide operating voltage range ±1.0V to ±8V
- High input impedance — $10^{12}\Omega$
- Programmable power consumption — as low as 20μW
- Input current lower than BIFETs — typ 1pA
- Available as singles, duals, triples, and quads
- Output voltage swing ranges to within millivolts of V- to V+
- Low power replacement for many standard op amps
- Compensated and uncompensated versions

APPLICATIONS

- Portable instruments
- Telephone headsets
- Hearing aid/microphone amplifiers
- Meter amplifiers
- Medical instruments
- High impedance buffers

A number of special options are available. They include:

- Single, dual, triple, and quad configurations
- Internally compensated and uncompensated versions
- Inputs protected to ±200V (ICL7613/15)
- Input common mode voltage range greater than supply rails (ICL7612)

SCHEMATIC

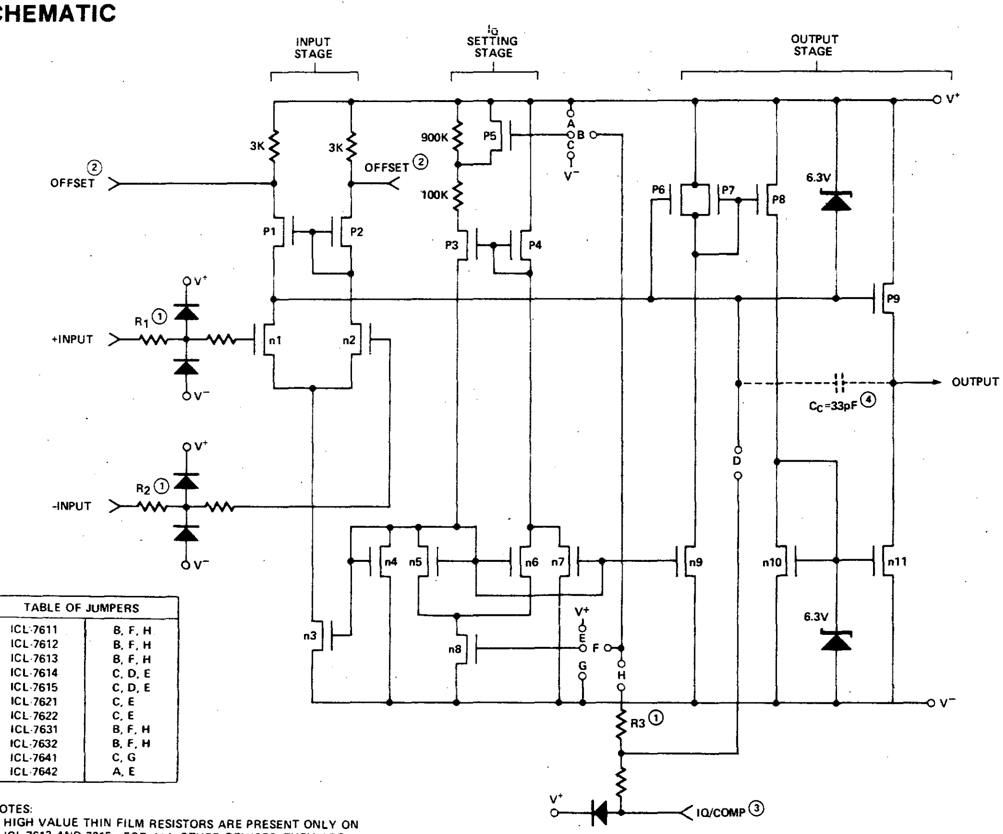


TABLE OF JUMPERS	
ICL7611	B, F, H
ICL7612	B, F, H
ICL7613	B, F, H
ICL7614	C, D, E
ICL7615	C, D, E
ICL7621	C, E
ICL7622	C, E
ICL7631	B, F, H
ICL7632	B, F, H
ICL7641	C, G
ICL7642	A, E

NOTES:
1. HIGH VALUE THIN FILM RESISTORS ARE PRESENT ONLY ON ICL7613 AND 7615. FOR ALL OTHER DEVICES, THEY ARE REPLACED BY DIRECT CONNECTIONS.
2. OFFSET NULLING PINS ARE NOT AVAILABLE ON TRIPLE (ICL763X) AND QUAD (ICL764X) VERSIONS.
3. I_Q AND COMP TERMINALS ARE METAL MASK OPTIONS OF THE SAME BONDING PAD; ONLY ONE OF THESE FUNCTIONS IS AVAILABLE IN A GIVEN DEVICE.
4. FOR INTERNALLY COMPENSATED VERSIONS ONLY. THIS CAPACITOR IS ABSENT FOR ALL OTHER DEVICES.

ICL761X/762X/763X/764X

GENERAL DESCRIPTION

The ICL761X/762X/763X/764X series is a family of monolithic CMOS op amps. These amplifiers provide the designer with high performance operation at low supply voltages and selectable quiescent currents, and are an ideal design tool when ultra low input current and low power drain are essential.

The basic amplifier will operate at supply voltages ranging from ±1.0V to ±8V, and may be operated from a single Lithium cell.

A unique quiescent current programming pin allows setting of standby current to 1 mA, 100 μA, or 10 μA, with no external components. This results in power drain as low as 20 μW. Output swings range to within a few millivolts of the supply voltages.

Of particular significance is the extremely low (1 pA) input current, input noise current of .01 pA/ $\sqrt{Hz}$, and $10^{12}\Omega$ input impedance. These features optimize performance in very high source impedance applications.

The inputs are internally protected and require no special handling procedures. Outputs are fully protected against shorts to ground or to either supply.

AC performance is excellent, with a slew rate of 1.6V/μs, and unity gain bandwidth of 1 MHz at I_Q= 1 mA.

Because of the low power dissipation, operating temperatures and drift are quite low. Applications utilizing these features may include stable instruments, extended life designs, or high density packages.

SELECTION GUIDE

BASIC TYPE

76XX

OFFSET NULL CAPABILITY
Y = YES
N = NO

I_Q SETTING
L = 10μA FIXED
M = 100μA FIXED
H = 1mA FIXED
P = PROGRAMMABLE

ORDERING INFORMATION[2]

ICL76XX M N O P

V_{OS} SELECTION
A = 2mV
B = 5mV
C = 10mV
D = 15mV
E = 20mV

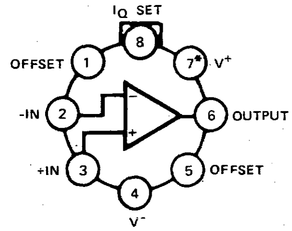
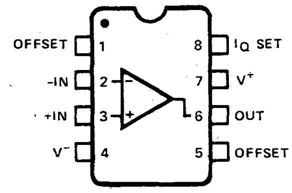
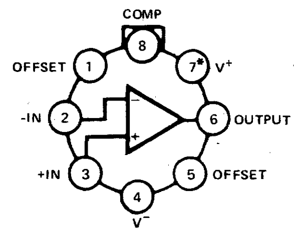
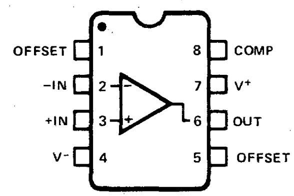
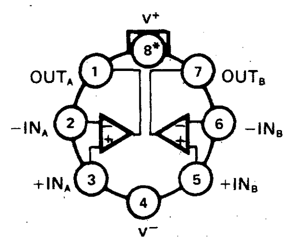
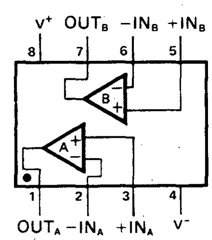
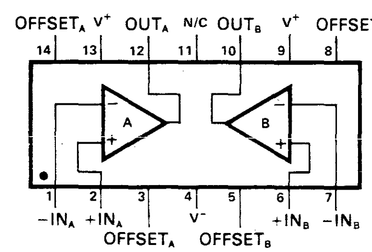
TEMP. RANGE
C = 0°C TO 70°C
M = -55°C TO +125°C

PACKAGE CODE
TV – TO-99, 8 PIN
PA – PLASTIC 8 PIN MINIDIP
PD – 14 PIN PLASTIC
PE – 16 PIN PLASTIC
JD – 14 PIN CERDIP
JE – 16 PIN CERDIP

	BASIC TYPE					ORDER SUFFIX							
						TO-99		MINI DIP	PLASTIC DIP[1]	CERAMIC DIP[1]		DIE	
	COMPENSATED	EXTERNALLY COMPENSATED	COMPENSATED/ INPUT PROTECTED	EXTERNALLY COMPENSATED INPUT PROTECTED	EXTENDED CMVR	0°C to +70°C	55°C to +125°C	0°C to +70°C	0°C to +70°C	0°C to +70°C	55°C to +125°C	0°C to +70°C	55°C to +125°C
SINGLE	7611 Y P	7614 Y M	7613 Y P	7615 Y M	7612 Y P	ACTV BCTV DCTV	AMTV BMTV —	ACPA BCPA DCPA				DC/D	
DUAL 1458 PINOUT	7621 N M					ACTV BCTV DCTV	AMTV BMTV —	ACPA BCPA DCPA				DC/D	
DUAL 747 PINOUT	7622 Y M								ACPD BCPD DCPD	ACJD BCJD DCJD	AMJD BMJD —	DC/D	
TRIPLE	7631 N P	[3] 7632 N P							BCPE CCPE ECPE	BCJE CCJE ECJE	BMJE CMJE —	EC/D	
QUAD High I_Q	7641 N H								BCPD CCPD ECPD	BCJD CCJD ECPD	BMJD CMJD —	EC/D	
QUAD Low I_Q	7642 N L								BCPD CCPD ECPD	BCJD CCJD ECJD	BMJD CMJD —	EC/D	

NOTES: 1. Duals and quads are available in 14 pin DIP packages, triples in 16 pin only.
2. Ordering code must consist of basic device and order suffix, e.g., ICL7611BCPA.
3. ICL7632 is not compensatable. Recommended for use in high gain circuits only.

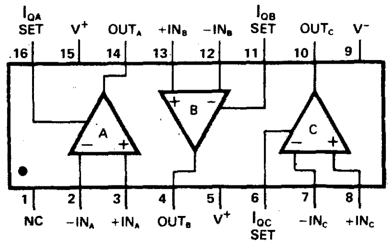
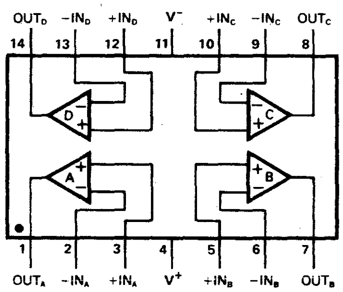
PIN CONFIGURATIONS

DEVICE	DESCRIPTION	PIN ASSIGNMENTS
ICL7611XCPA ICL7611XCTV ICL7611XMTV ICL7612XCPA ICL7612XCTV ICL7612XMTV ICL7613XCPA ICL7613XCTV ICL7613XMTV	Internal compensation, plus offset null capability and external I_Q control.	**TO-99** (TOP VIEW) (outline dwg TV)  *Pin 7 connected to case. **8 PIN DIP** (TOP VIEW) (outline dwg PA) 
ICL7614XCPA ICL7614XCTV ICL7614XMTV ICL7615XCPA ICL7615XCTV ICL7615XMTV	Fixed I_Q (100μA), external compensation, and offset null capability.	**TO-99** (TOP VIEW) (outline dwg TV)  * Pin 7 connected to case. **8 PIN DIP** (TOP VIEW) (outline dwg PA) 
ICL7621XCPA ICL7621XCTV ICL7621XMTV	Dual op amps with internal compensation; I_Q fixed at 100μA Pin compatible with Texas Inst. TL082 Motorola MC1458 Raytheon RC4558	**TO-99** (TOP VIEW) (outline dwg TV)  * Pin 8 connected to case. **8 PIN DIP** (TOP VIEW) (outline dwg PA) 
ICL7622XCPD	Dual op amps with internal compensation and offset null capability; I_Q fixed at 100μA Pin compatible with Texas Inst. TL083 Fairchild μA747	**14 PIN DIP** (TOP VIEW) (outline dwgs JD, PD)  Note: Pins 9 and 13 are internally connected.

LINEAR

Intersil

PIN CONFIGURATIONS (Cont.)

DEVICE	DESCRIPTION	PIN ASSIGNMENTS
ICL7631XCPE ICL7632XCPE	Triple op amps with internal compensation (ICL7631) and no compensation (ICL7632). Adjustable I_Q Same pin configuration as ICL8023.	16 PIN DIP (TOP VIEW) (outline dwgs JE, PE)  Note: Pins 5 and 15 are internally connected.
ICL7641XCPD ICL7642XCPD	Quad op amps with internal compensation. I_Q fixed at 1mA (ICL7641) I_Q fixed at 10μA (ICL7642) Pin compatible with Texas Instr. TL084 National LM324 Harris HA4741	14 PIN DIP (TOP VIEW) (outline dwg JD, PD) 

GENERAL INFORMATION

STATIC PROTECTION

All devices are static protected by the use of input diodes. However, strong static fields should be avoided, as it is possible for the strong fields to cause degraded diode junction characteristics, which may result in increased input leakage currents.

LATCHUP AVOIDANCE

Junction-isolated CMOS circuits employ configurations which produce a parasitic 4-layer (p-n-p-n) structure. The 4-layer structure has characteristics similar to an SCR, and under certain circumstances may be triggered into a low impedance state resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails may be applied to any pin. (An exception to this rule concerns the inputs of the ICL7613 and ICL7615, which are protected to ±200V.) In general, the op amp supplies must be established simultaneously with, or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to 2 mA to prevent latchup.

CHOOSING THE PROPER I_Q

Each device in the ICL76XX family has a similar I_Q set-up scheme, which allows the amplifier to be set to nominal quiescent currents of 10 μA, 100 μA or 1 mA. These current settings change only very slightly over the entire supply voltage range. The ICL7611/12/13 and ICL7631/32 have an external I_Q control terminal, permitting user selection of each amplifiers' quiescent current. (The ICL7614/15, 7621/22, and 7641/42 have fixed I_Q settings — refer to selector guide for details.) To set the I_Q of programmable versions, connect the I_Q terminal as follows:

I_Q = 10μA — I_Q pin to V+

I_Q = 100μA — I_Q pin to ground. If this is not possible, any voltage from V+ -0.8 to V^- +0.8 can be used.

I_Q = 1mA — I_Q pin to V^-

NOTE: The negative output current available is a function of the quiescent current setting. For maximum p-p ouput voltage swings into low impedance loads, I_Q of 1 mA should be selected.

OUTPUT STAGE AND LOAD DRIVING CONSIDERATIONS

Each amplifiers' quiescent current flows primarily in the output stage. This is approximately 70% of the I_Q settings. This allows output swings to almost the supply rails for output loads of 1M, 100K, and 10K, using the output stage in a highly linear class A mode. In this mode, crossover distortion is avoided and the voltage gain is maximized. However, the output stage can also be operated in Class AB, which can supply higher output currents. (See graphs under Typical Operating Characteristics). During the transition from Class A to Class B operation, the output transfer characteristic is non-linear and the voltage gain decreases.

A special feature of the output stage is that it approximates a transconductance amplifier, and its gain is directly proportional to load impedance. Approximately the same open loop gains are obtained at each of the I_Q settings if corresponding loads of 10K, 100K, and 1M are used.

INPUT OFFSET NULLING

For those models provided with OFFSET NULLING pins, nulling may be achieved by connecting a 25K pot between the OFFSET terminals with the wiper connected to V^+. At quiescent currents of 1 mA and 100 μA, the nulling range provided is adequate for all V_{OS} selections; however with $I_Q = 10\ \mu A$, nulling may not be possible with higher values of V_{OS}.

FREQUENCY COMPENSATION

The ICL7611/12/13, 7621/22, 7631, 7641/42 are internally compensated, and are stable for closed loop gains as low as unity for capacitive loads up to 100pF

The ICL7614 and 15 are externally compensated by connecting a capacitor between the COMP and OUT pins. A 39pF capacitor is required for unity gain compensation; for greater than unity gain applications, increased bandwidth and slew rate can be obtained by reducing the value of the compensating capacitor.

Since the g_m of the first stage is proportional to $\sqrt{I_Q}$, greatest compensation is required when $I_Q = 1$mA. The ICL7632 is not compensated internally, nor can it be compensated externally. The device is stable when used as follows:

I_Q of 1 mA for gains ≥ 20
I_Q of 100 μA for gains ≥ 10
I_Q of 10 μA for gains ≥ 5

HIGH VOLTAGE INPUT PROTECTION

The ICL7613 and 7615 include on-chip thin film resisitors and clamping diodes which allow voltages of up to ±200 to be applied to either input for an indefinite time without device failure. These devices will be useful where high common mode voltages, differential mode voltages, or high transients may be experienced. Such conditions may be found when interfacing separate systems with separate supplies. Unity gain stability is somewhat degraded with capacitive loads because of the high value of input resistors.

EXTENDED COMMON MODE INPUT RANGE

The ICL7612 incorporates additional processing which allows the input CMVR to exceed each power supply rail by 0.1 volt for applications where $V_{SUPP} \geq \pm 1.5$V. For those applications where $V_{SUPP} \leq \pm 1.5$V, the input CMVR is limited in the positive direction, but may exceed the negative supply rail by 0.1 volt in the negative direction (eg. for $V_{SUPP} = \pm 1.0$V, the input CMVR would be + 0.6 volts to -1.1 volts).

OPERATION AT $V_{SUPP} = \pm 1.0$ VOLTS

Operation at $V_{SUPP} = \pm 1.0$V is guaranteed at $I_Q = 10\mu A$ only. This applies to these devices with selectable I_Q, and those devices are set internally to $I_Q = 10\mu A$ (i.e., ICL7611 , 7612, 7613, 7631, 7632, 7642).

Output swings to within a few millivolts of the supply rails are achievable for $R_L \geq 1$ MegΩ. Guaranteed input CMVR is ±0.6V minimum and typically +0.9V to -0.7 at $V_{SUPP} = \pm 1.0$V. For applications where greater common mode range is desirable, refer to description of ICL7612 above.

The user is cautioned that, due to extremely high input impedances, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup.

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ABSOLUTE MAXIMUM RATINGS [1]

Total Supply Voltage V^+ to V^- 18V
Input Voltage .... V^-+0.3 to V^- -0.3V
Input Voltage ICL7613/15 Only .... V^++200 to V^- -200V
Differential Input Voltage [2] ... ±[(V^++0.3) - (V^- -0.3)]V
Differential Input Voltage [2]
ICL7613/15 Only .... ±[(V^++200) - (V^- - 200)]V
Duration of Output Short Circuit [3] .... Unlimited
Continuous Power Dissipation @ 25°C

		Above 25°C derate as follows:
TO-99	250mW	2mW/°C
8 Lead Minidip	250mW	2mW/°C
14 Lead Plastic	375mW	3mW/°C
14 Lead Cerdip	500mW	4mW/°C
16 Lead Plastic	375mW	3mW/°C
16 Lead Cerdip	500mW	4mW/°C

Storage Temperature Range .... -55°C to +150°C

Operating Temperature Range
M Series .... -55°C to +125°C
C Series .... 0°C to +70°C
Lead Temperature (Soldering, 10 sec) .... 300°C

Notes:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Long term offset voltage stability will be degraded if large input differential voltages are applied for long periods of time.
3. The outputs may be shorted to ground or to either supply, for $V_{SUPP} \leq 10$V. Care must be taken to insure that the dissipation rating is not exceeded.

ELECTRICAL CHARACTERISTICS $V_{SUPP} = \pm 5.0V$, $T_A = 25°C$, unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	76XXA MIN.	76XXA TYP.	76XXA MAX.	76XXB MIN.	76XXB TYP.	76XXB MAX.	76XXD MIN.	76XXD TYP.	76XXD MAX.	UNITS
Input Offset Voltage	V_{OS}	$R_S \le 100K\Omega$, $T_A=25°C$ $T_{MIN} \le T_A \le T_{MAX}$			2 3			5 7			15 20	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \le 100K\Omega$		10			15			25		$\mu V/°C$
Input Offset Current	I_{OS}	$T_A=25°C$ $\Delta T_A=C$ [2] $\Delta T_A=M$ [2]		0.5	30 300 800		0.5	30 300 800		0.5	30 300 800	pA
Input Bias Current	I_{BIAS}	$T_A=25°C$ $\Delta T_A=C$ $\Delta T_A=M$		1.0	50 400 4000		1.0	50 400 4000		1.0	50 400 4000	pA
Common Mode Voltage Range (Except ICL7612)	V_{CMR}	$I_Q=10\mu A$ [1] $I_Q=100\mu A$ $I_Q=1mA$ [1]	±4.4 ±4.2 ±3.7			±4.4 ±4.2 ±3.7			±4.4 ±4.2 ±3.7			V
Extended Common Mode Voltage Range (ICL7612 Only)	V_{CMP}	$I_Q=10\mu A$	±5.3			±5.3			±5.3			V
		$I_Q=100\mu A$	+5.3 -5.1			+5.3 -5.1			+5.3 -5.1			
		$I_Q=1mA$	+5.3 -4.5			+5.3 -4.5			+5.3 -4.5			
Output Voltage Swing	V_{OUT}	(1) $I_Q = 10\mu A$, $R_L = 1M\Omega$ $T_A = 25°C$ $\Delta T_A = C$ $\Delta T_A = M$	 ± 4.9 ± 4.8 ± 4.7			 ±4.9 ±4.8 ±4.7			 ± 4.9 ± 4.8 ± 4.7			V
		$I_Q = 100\mu A$, $R_L = 100k\Omega$ $T_A = 25°C$ $\Delta T_A = C$ $\Delta T_A = M$	 ± 4.9 ± 4.8 ± 4.5			 ±4.9 ±4.8 ±4.5			 ± 4.9 ± 4.8 ± 4.5			
		(1) $I_Q = 1mA$, $R_L = 10k\Omega$ $T_A = 25°C$ $\Delta T_A = C$ $\Delta T_A = M$	 ± 4.5 ± 4.3 ± 4.0			 ±4.5 ±4.3 ±4.0			 ± 4.5 ± 4.3 ± 4.0			
Large Signal Voltage Gain	A_{VOL}	$V_O=\pm 4.0V$, $R_L=1M\Omega$ $I_Q=10\mu A$ [1], $T_A=25°C$ $\Delta T_A=C$ $\Delta T_A=M$	 86 80 74	 104		 80 75 68	 104		 80 75 68	 104		dB
		$V_O=\pm 4.0V$, $R_L=100k\Omega$ $I_Q=100\mu A$, $T_A=25°C$ $\Delta T_A=C$ $\Delta T_A=M$	 86 80 74	 102		 80 75 68	 102		 80 75 68	 102		
		$V_O=\pm 4.0V$, $R_L=10k\Omega$ $I_Q=1mA$ [1] $T_A=25°C$ $\Delta T_A=C$ $\Delta T_A=M$	 80 76 72	 83		 76 72 68	 83		 76 72 68	 83		
Unity Gain Bandwidth	G_{BW}	$I_Q=10\mu A$ [1] $I_Q=100\mu A$ $I_Q=1mA$ [1]		0.044 0.48 1.4			0.044 0.48 1.4			0.044 0.48 1.4		MHz
Input Resistance	R_{IN}			10^{12}			10^{12}			10^{12}		Ω
Common Mode Rejection Ratio	CMRR	$R_S \le 100K\Omega$, $I_Q=10\mu A$ [1] $R_S \le 100K\Omega$, $I_Q=100\mu A$ $R_S \le 100K\Omega$, $I_Q=1mA$ [1]	76 76 66	96 91 87		70 70 60	96 91 87		70 70 60	96 91 87		dB
Power Supply Rejection Ratio	PSRR	$R_S \le 100K\Omega$, $I_Q=10\mu A$ [1] $R_S \le 100K\Omega$, $I_Q=100\mu A$ $R_S \le 100K\Omega$, $I_Q=1mA$ [1]	80 80 70	94 86 77		80 80 70	94 86 77		80 80 70	94 86 77		dB
Input Referred Noise Voltage	e_n	$R_S=100\Omega$, f=1KHz		100			100			100		$nV/\sqrt{Hz}$
Input Referred Noise Current	i_n	$R_S=100\Omega$, f=1KHz		0.01			0.01			0.01		$pA/\sqrt{Hz}$
Supply Current (Per Amplifier)	I_{SUPP}	No Signal, No Load $I_Q=10\mu A$ [1] $I_Q=100\mu A$ $I_Q=1mA$ [1]		 0.01 0.1 1.0	 0.02 0.25 2.5		 0.01 0.1 1.0	 0.02 0.25 2.5		 0.01 0.1 1.0	 0.02 0.25 2.5	mA
Channel Separation	V_{O1}/V_{O2}	$A_{VOL}=100$		120			120			120		dB
Slew Rate [3]	SR	$A_{VOL}=1$, $C_L=100pF$, $V_{IN} = 8V_{p-p}$ $I_Q=10\mu A$ [1], $R_L=1M\Omega$ $I_Q=100\mu A$, $R_L=100K\Omega$ $I_Q=1mA$ [1], $R_L=10K\Omega$		 0.016 0.16 1.6			 0.016 0.16 1.6			 0.016 0.16 1.6		$V/\mu s$
Rise Time [3]	t_r	$V_{IN}=50mV$, $C_L=100pF$ $I_Q=10\mu A$ [1], $R_L=1M\Omega$ $I_Q=100\mu A$, $R_L=100K\Omega$ $I_Q=1mA$ [1], $R_L=10K\Omega$		 20 2 0.9			 20 2 0.9			 20 2 0.9		μs
Overshoot Factor [3]		$V_{IN}=50mV$, $C_L=100pF$ $I_Q=10\mu A$ [1], $R_L=1M\Omega$ $I_Q=100\mu A$, $R_L=100K\Omega$ $I_Q=1mA$ [1], $R_L=10K\Omega$		 5 10 40			 5 10 40			 5 10 40		%

Note: 1. ICL7611, 7612, 7613 only.
2. C = Commercial Temperature Range: 0°C to +70°C
M = Military Temperature Range: -55°C to +125°C
3. ICL7614/15; 39pF from pin 6 to pin 8.

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ELECTRICAL CHARACTERISTICS $V_{SUPP} = \pm 1.0V$, $I_Q = 10\mu A$, $T_A = 25°C$, unless otherwise specified.
Specs apply to ICL7611/7612/7613 only.

PARAMETER	SYMBOL	CONDITIONS	76XXA MIN.	76XXA TYP.	76XXA MAX.	76XXB MIN	76XXB TYP.	76XXB MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \le 100K\Omega$, $T_A=25°C$ $T_{MIN} \le T_A \le T_{MAX}$			2 3			5 7	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \le 100K\Omega$		10			15		$\mu V/°C$
Input Offset Current	I_{OS}	$T_A=25°C$ $\Delta T_A=C$		0.5	30 300		0.5	30 300	pA
Input Bias Current	I_{BIAS}	$T_A=25°C$ $\Delta T_A=C$		1.0	50 500		1.0	50 500	pA
Common Mode Voltage Range (Except ICL7612)	V_{CMR}		±0.6			±0.6			V
Extended Common Mode Voltage Range (ICL7612 Only)	V_{CMR}		+0.6 to -1.1			+0.6 to -1.1			V
Output Voltage Swing	V_{OUT}	$R_L=1M\Omega$, $T_A=25°C$ $\Delta T_A=C$		±0.98 ±0.96			±0.98 ±0.96		V
Large Signal Voltage Gain	A_{VOL}	$V_O=\pm0.1V$, $R_L=1M\Omega$ $T_A=25°C$ $\Delta T_A=C$		90 80			90 80		dB
Unity Gain Bandwidth	G_{BW}			0.044			0.044		MHz
Input Resistance	R_{IN}			10^{12}			10^{12}		Ω
Common Mode Rejection Ratio	CMRR	$R_S \le 100K\Omega$		80			80		dB
Power Supply Rejection Ratio	PSRR	$R_S \le 100K\Omega$		80			80		dB
Input Referred Noise Voltage	e_n	$R_S=100\Omega$, f=1KHz		100			100		$nV/\sqrt{Hz}$
Input Referred Noise Current	i_n	$R_S=100\Omega$, f=1KHz		0.01			0.01		$pA/\sqrt{Hz}$
Supply Current (Per Amplifier)	I_{SUPP}	No Signal, No Load		6	15		6	15	μA
Slew Rate	SR	$A_{VOL}=1$, $C_L=100pF$, $V_{IN}=0.2Vp\text{-}p$ $R_L=1M\Omega$		0.016			0.016		$V/\mu s$
Rise Time	t_r	$V_{IN}=50mV$, $C_L=100pF$ $R_L=1M\Omega$		20			20		μs
Overshoot Factor		$V_{IN}=50mV$, $C_L=100pF$ $R_L=1M\Omega$		5			5		%

Note: C = Commercial Temperature Range (0°C to +70°C); M = Military Temperature Range (-55°C to +125°C).

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ICL7650
Chopper Stabilized Operational Amplifier

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FEATURES

- **Extremely low input offset voltage – 1μV over temperature range**
- **Low long-term and temperature drifts of input offset voltage**
- **Low DC input bias current – 10pA**
- **Extremely high gain, CMRR and PSRR – min 120dB**
- **High slew rate – 2.5V/μs**
- **Wide bandwidth – 2MHz**
- **Internally compensated for unity-gain operation**
- **Very low intermodulation effects (open loop phase shift <10° @ chopper frequency)**
- **Clamp circuit to avoid overload recovery problems and allow comparator use**
- **Extremely low chopping spikes at input and output**

GENERAL DESCRIPTION

The ICL7650 chopper-stabilized amplifier is a high-performance device which offers exceptionally low offset voltage and input-bias parameters, combined with excellent bandwidth and speed characteristics. Intersil's unique CMOS approach to chopper-stabilized amplifier design yields a versatile precision component which can replace more expensive hybrid or modular parts, while at the same time out-performing them and other monolithic devices.

The chopper amplifier achieves its low offset by comparing the inverting and non-inverting input voltages in a nulling amplifier, nulled by alternate clock phases. Two external capacitors are required to store the correcting potentials on the two amplifier nulling inputs; these are the only external components necessary.

The clock oscillator and all the other control circuitry is entirely self-contained, however the 14-pin version includes a provision for the use of an external clock, if required for a particular application. In addition, the ICL7650 is internally compensated for unity-gain operation.

ORDERING INFORMATION

PART	TEMP RANGE	PACKAGE
ICL 7650 CPA	0° - 70°C	8-Pin Plastic
ICL 7650 CPD	0° - 70°C	14-Pin Plastic
ICL 7650 CTV	0° - 70°C	8-Pin TO-99
ICL 7650 IJA	– 20°C - 85°C	8-Pin Cerdip
ICL 7650 IJD	– 20°C - 85°C	14-Pin Cerdip
ICL 7650 ITV	– 20°C - 85°C	8-Pin TO-99
ICL 7650 MJD	– 55°C - 125°C	14-Pin Cerdip
ICL 7650 MTV	– 55°C - 125°C	8-Pin TO-99
ICL 7650 CPA-1	0° - 70°C	8-Pin Plastic
ICL 7650 CTV-1	0° - 70°C	8-Pin TO-99
ICL 7650 IJD-1	– 20°C - 85°C	8-Pin Cerdip
ICL 7650 ITV-1	– 20°C - 85°C	8-Pin TO-99
ICL 7650 MTV-1	– 55°C - 125°C	8-Pin TO-99

NOTE: By using the ICL 7650-1 versions and connecting C_{RETN}, better noise performance can be attained.

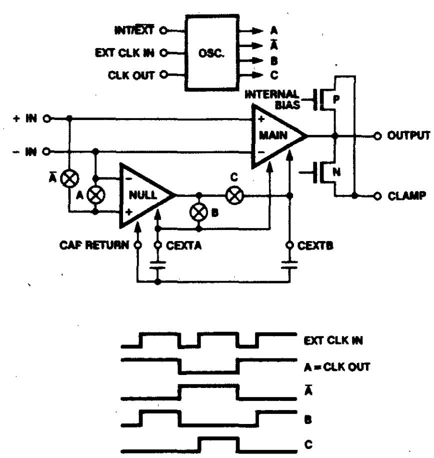
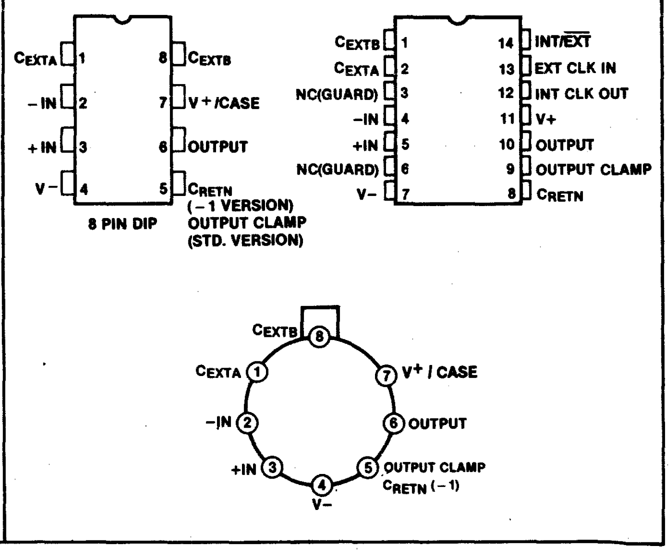


FIG. 1 BLOCK DIAGRAM

PIN CONFIGURATION



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ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) .... 18 Volts
Input Voltage .... (V^+ + 0.3) to (V^- – 0.3) Volts
Storage Temp. Range .... –55°C to 150°C
Operating Temp. Range .... See Note 1
Lead Temperature (Soldering, 10 sec) .... 300°C
Voltage on oscillator control pins .... V^+ to V^-
except EXT CLOCK IN: .(V^+ + 0.3) to (V^+ – 6.0) Volts
Duration of Output short circuit .... Indefinite
Current into any pin 10mA
— while operating (Note 4) .... 100 μA

Cont. Total Power Dissipn (T_A = 25°C)
CERDIP Package .... 500 mW
Plastic Package .... 375 mW
TO-99 .... 250 mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS: Test Conditions: V^+ = +5V, V^- = –5V, T_A = +25°C, Test Ckt (unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	LIMITS TYP.	MAX.	UNIT
Input Offset Voltage	V_{OS}	T_A = +25°C –55°C < T_A < +85°C –55°C < T_A < +125°C		±0.7 ±1.0	±5 5.0	μV
Average Temp. Coefficient of Input Offset Voltage	$\Delta V_{OS}/\Delta T$	–20°C < T_A < +85°C		0.01	0.05	μV/°C
				50		
Input Bias Current (doubles every 10°C)	I_{BIAS}	T_A = +25°C 0°C < T_A < +70°C –20°C < T_A < +85°C		1.5 35 100	10	pA
Input Offset Current	I_{OS}	T_A = 25°C		0.5		pA
Input Resistance	R_{IN}			10^{12}		Ω
Large Signal Voltage Gain	A_{VOL}	R_L = 10kΩ	1x10⁶	5x10⁶		V/V
Output Voltage Swing (Note 3)	V_{OUT}	R_L = 10kΩ R_L = 100kΩ	±4.7	±4.85 ±4.95		V
Common Mode Voltage Range	CMVR		–5.0	–5.2 to +2.0	1.6	V
Common Mode Rejection Ratio	CMRR	CMVR = –5V to +1.6	120	130		dB
Power Supply Rejection Ratio	PSRR	±3V to ±8V	120	130		dB
Input Noise Voltage	$e_{n_{p-p}}$	R_S = 100Ω 0 to 10Hz		2		μVp-p
Input Noise Current	i_n	f = 10Hz		0.01		pA/√Hz
Unity Gain Bandwidth	GBW			2.0		MHz
Slew Rate	SR	C_L = 50pF, R_L = 10kΩ		2.5		V/μs
Rise Time	t_r			0.2		μs
Overshoot				20		%
Operating Supply Range	V+ to V–		4.5		16	V
Supply Current	I_{SUPP}	no load		2.0	3.5	mA
Internal Chopping Frequency	f_{ch}	pins 12-14 open (DIP)	120	200	375	Hz
Clamp ON Current (note 2)		R_L = 100kΩ	25	70	200	μA
Clamp OFF Current (note 2)		–4.0V < V_{OUT} < +4.0V		1		pA
Offset Voltage vs Time				100		nV/√month

NOTE 1: Operating temperature range for M series parts is –55°C to +125°C, for I series is –20°C to +85°C, for C series is 0°C to +70°C
NOTE 2: See OUTPUT CLAMP under detailed description.
NOTE 3: OUTPUT CLAMP not connected. See typical characteristic curves for output swing vs clamp current characteristics.
NOTE 4: Limiting input current to 100μA is recommended to avoid latch-up problems. Typically 1mA is safe, however this is not guaranteed.
NOTE 5: I_{OS} = 2 • I_{BIAS}

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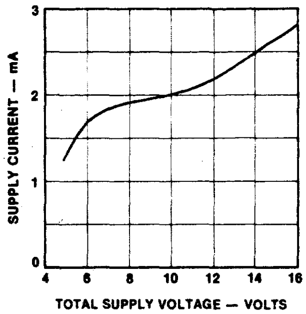
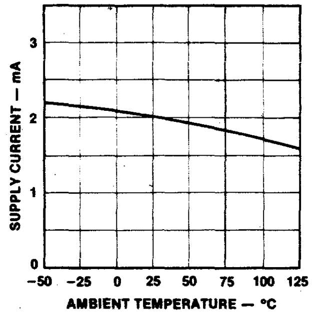
TYPICAL OPERATING CHARACTERISTICS

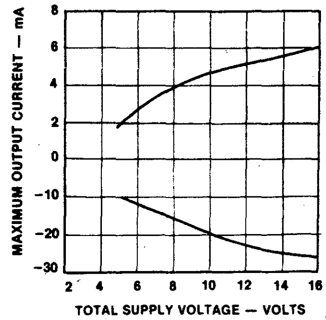
SUPPLY CURRENT vs. SUPPLY VOLTAGE



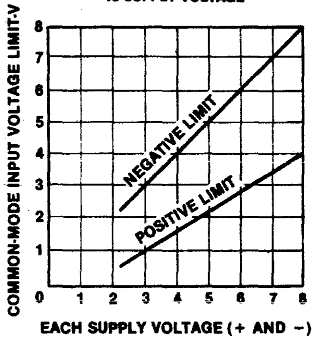
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



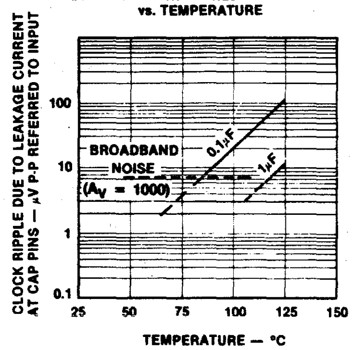
MAXIMUM OUTPUT CURRENT vs. SUPPLY VOLTAGE



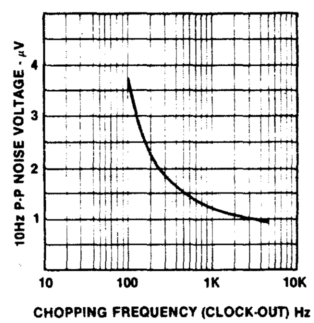
COMMON-MODE INPUT-VOLTAGE RANGE vs SUPPLY VOLTAGE



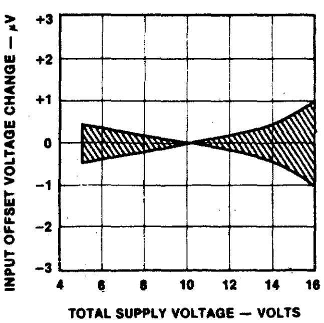
CLOCK RIPPLE REFERRED TO THE INPUT vs. TEMPERATURE



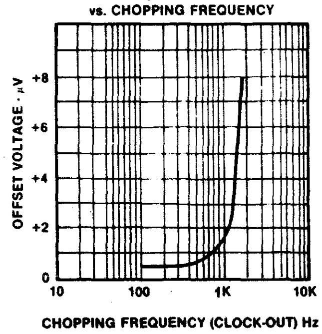
10Hz P-P NOISE VOLTAGE vs. CHOPPING FREQUENCY



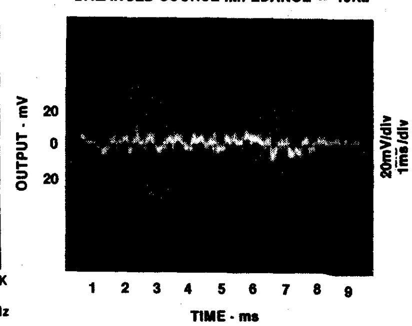
INPUT OFFSET VOLTAGE CHANGE vs. SUPPLY VOLTAGE



INPUT OFFSET VOLTAGE vs. CHOPPING FREQUENCY



OUTPUT WITH ZERO INPUT; GAIN = 1000; BALANCED SOURCE IMPEDANCE = 10KΩ



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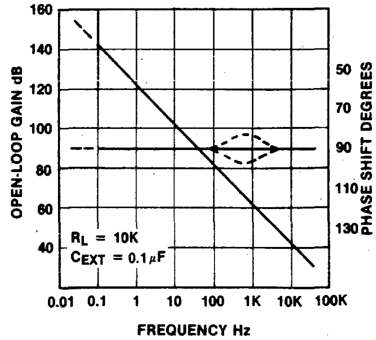
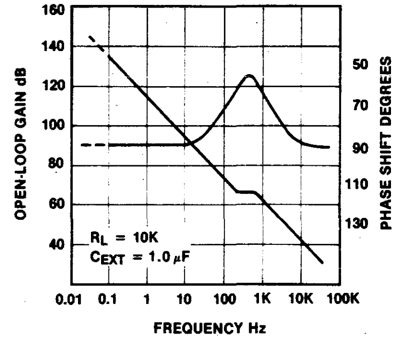
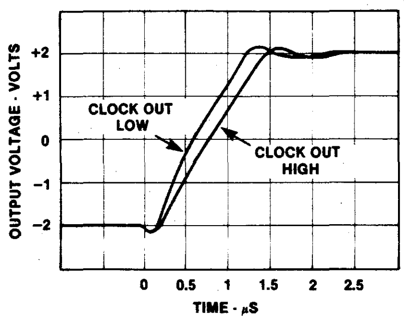
OPEN LOOP GAIN AND PHASE SHIFT
vs. FREQUENCY



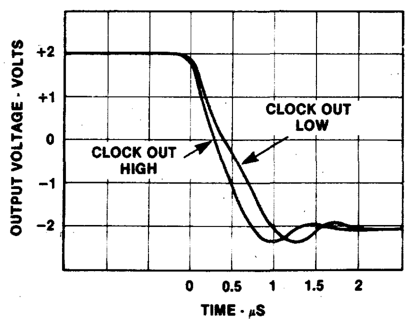
OPEN LOOP GAIN AND PHASE SHIFT
vs. FREQUENCY



VOLTAGE FOLLOWER LARGE SIGNAL
PULSE RESPONSE *

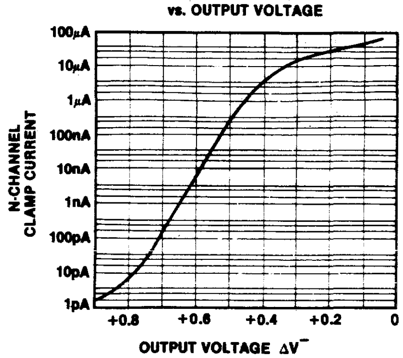


VOLTAGE FOLLOWER LARGE SIGNAL
PULSE RESPONSE *

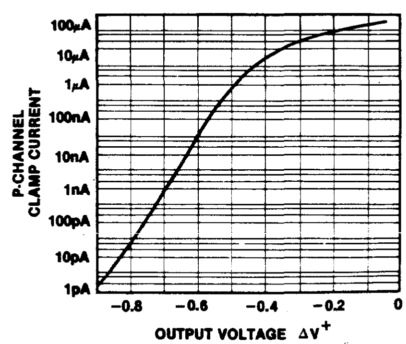


* THE TWO DIFFERENT RESPONSES CORRESPOND TO THE TWO PHASES OF THE CLOCK.

N-CHANNEL CLAMP CURRENT
vs. OUTPUT VOLTAGE



P-CHANNEL CLAMP CURRENT
vs. OUTPUT VOLTAGE



LINEAR

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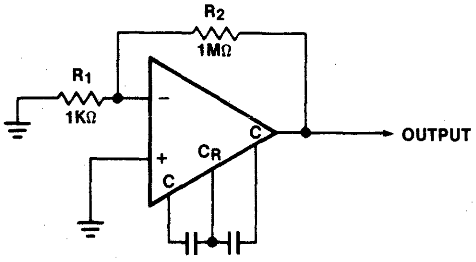
TEST CIRCUIT



DETAILED DESCRIPTION

AMPLIFIER

The block diagram shows the major elements of the ICL7650. There are two amplifiers, the main amplifier, and the nulling amplifier; both have offset-null capability. The main amplifier is connected full-time from the input to the output, while the nulling amplifier, under the control of the chopping frequency oscillator and clock circuit, alternately nulls itself and the main amplifier. The nulling connections, which are MOSFET back gates, are inherently high impedance, and two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants. The nulling arrangement operates over the full common-mode and power-supply ranges, and is also independent of the output level, thus giving exceptionally high CMRR, PSRR, and A_{VOL}.

Careful balancing of the input switches, and the inherent balance of the input circuit, minimizes chopper frequency charge injection at the input terminals, and also the feedforward-type injection into the compensation capacitor, which is the main cause of output spikes in this type of circuit.

INTERMODULATION

Previous chopper-stabilized amplifiers have suffered from intermodulation effects between the chopper frequency and input signals. These arise because the finite AC gain of the amplifier necessitates a small AC signal at the input. This is seen by the zeroing circuit as an error signal, which is chopped and fed back, thus injecting sum and difference frequencies and causing disturbances to the gain and phase vs. frequency characteristics near the chopping frequency. These effects are sustantially reduced in the ICL7650 by feeding the nulling circuit with a dynamic current, corresponding to the compensation capacitor current, in such a way as to cancel that portion of the input signal due to finite AC gain. Since that is the major error contribution to the ICL7650, the intermodulation and gain/phase disturbances are held to very low values, and can generally be ignored.

CAPACITOR CONNECTION

The null-storage capacitors should be connected to the C_{EXTA} and C_{EXTB} pins, with a common connection to the C_{RETN} pin (in the case of 14-pin devices) or the V^- pin (in the case of the 8-pin devices). This connection should be made directly by either a separate wire or PC trace to avoid injecting load current IR drops into the capacitive circuitry. The outside foil, where available, should be connected to C_{RETN} (or V^-).

OUTPUT CLAMP

The OUTPUT CLAMP pin allows reduction of the overload recovery time inherent with chopper-stabilized amplifiers. When tied to the inverting input pin, or summing junction, a current path between this point and the OUTPUT pin occurs just before the device output saturates. Thus uncontrolled input differential inputs are avoided, together with the consequent charge build-up on the correction-storage capacitors. The output swing is slightly reduced.

CLOCK

The ICL7650 has an internal oscillator giving a chopping frequency of 200 Hz, available at the CLOCK OUT pin on the 14-pin devices. Provision has also been made for the use of an external clock in these parts. The INT/$\overline{EXT}$ pin has an internal pull-up and may be left open for normal operation, but to utilize an external clock this pin must be tied to V^- to disable the internal clock. The external clock signal may then be applied to the EXT. CLOCK IN pin. At low frequencies, the duty cycle of the external clock is not critical, since an internal divide-by-two provides the desired 50% switching duty cycle. However, since the capacitors are charged only when EXT CLK IN is HIGH, a 50-80% positive duty cycle is favored for frequencies above 500Hz to ensure that any transients have time to settle before the capacitors are turned OFF. The external clock should swing between V^+ and GROUND for power supplies up to ±6V, and between V^+ and V^+ −6V for higher supply voltages. Note that a signal of about 400Hz will be present at the EXT CLK IN pin with INT/$\overline{EXT}$ high or open. This is the internal clock signal before the divider.

In those applications where a strobe signal is available, an alternate approach to avoid capacitor misbalancing during overload can be used. If a strobe signal is connected to EXT CLK IN so that it is low during the time that the overload signal is applied to the amplifier, neither capacitor will be charged. Since the leakage at the capacitor pins is quite low at room temperature, the typical amplifier will drift less than 10μV/sec, and relatively long measurements can be made with little change in offset.

BRIEF APPLICATION NOTES

COMPONENT SELECTION

The two required capacitors, C_{EXTA} and C_{EXTB}, have optimum values depending on the clock or chopping frequency. For the preset internal clock, the correct value is 0.1μF, and to maintain the same relationship between the chopping frequency and the nulling time constant this value should be scaled approximately in proportion if an external clock is used. A high-quality film-type capacitor such as mylar is preferred, although a ceramic or other lower-grade capacitor may prove suitable in many applications. For quickest settling on initial turn-on, low dielectric absorbtion capacitors (such as poly propylene) should be used. With ceramic capacitors, several seconds may be required to settle to 1μV.

STATIC PROTECTION

All device pins are static-protected by the use of input diodes. However, strong static fields and discharges should be avoided, as they can cause degraded diode junction characteristics, which may result in increased input-leakage currents.

LATCH-UP AVOIDANCE

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low-impedance state, resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 1mA to avoid latchup, even under fault conditions.

OUTPUT STAGE/LOAD DRIVING

The output circuit is a high-impedance stage (approximately 18kΩ), and therefore, with loads less than this the chopper amplifier behaves in some ways like a transconductance amplifier whose open-loop gain is proportional to load resistance. For example, the open-loop gain will be 17dB lower with a 1kΩ load than with a 10kΩ load. If the amplifier is used strictly for DC, this lower gain is of little consequence, since the DC gain is typically greater than 120dB even with a 1KΩ load. However, for wideband applications, the best frequency response will be achieved with a load resistor of 10K or higher. This will result in a smooth 6dB/octave response from 0.1Hz to 2MHz, with phase shifts of less than 10° in the transition region where the main amplifier takes over from the null amplifier.

THERMO-ELECTRIC EFFECTS

The ultimate limitations to ultra-high precision DC amplifiers are the thermo-electric or Peltier effects arising in thermocouple junctions of dissimilar metals, alloys, silicon, etc. Unless all junctions are at the same temperature, thermoelectric voltages typically around 0.1μV/°C, but up to tens of μV/°C for some materials, will be generated. In order to realize the extremely low offset voltages that the chopper amplifier can provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially that caused by power-dissipating elements in the system. Low thermoelectric-coefficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High-impedance loads are preferable, and good separation from surrounding heat-dissipating elements is advisable.

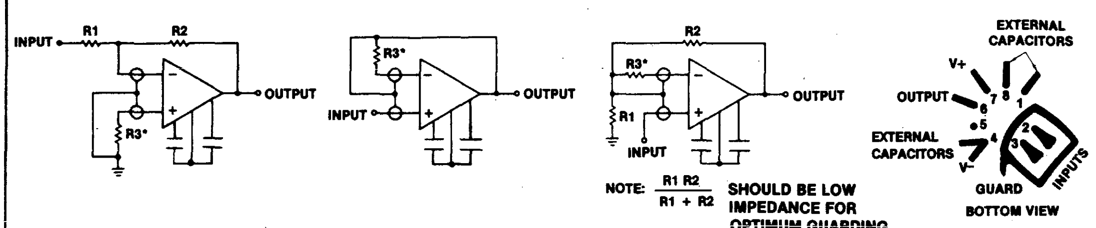
GUARDING

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the ICL7650. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

The pin configuration of the 14-pin dual in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration, but corresponds to that of the LM108).

CONNECTION OF INPUT GUARDS



*USE R3 TO COMPENSATE FOR LARGE SOURCE RESISTANCES, OR FOR CLAMP OPERATION (see FIG. 2)

BOARD LAYOUT FOR INPUT GUARDING WITH TO-99 PACKAGE

INVERTING AMPLIFIER FOLLOWER NON-INVERTING AMPLIFIER

PIN COMPATIBILITY

The basic pinout of the 8-pin device corresponds, where possible, to that of the industry-standard 8-pin devices, the LM741, LM101, etc. The null-storing external capacitors are connected to pins 1 and 8, usually used for offset null or compensation capacitors, or simply not connected. The output-clamp pin (5) is similarly used. In the case of the OP-05 and OP-07 devices, the replacement of the offset-null pot, connected between pins 1 and 8 and V+, by two capacitors from those pins to V−, will provide easy compatibility. As for the LM108, replacement the compensation capacitor between pins 1 and 8 by the two capacitors to V− is all that is necessary. The same operation, with the removal of any connection to pin 5, will suffice for the LM101, μA748, and similar parts.

The 14-pin device pinout corresponds most closely to that of the LM108 device, owing to the provision of "NC" pins for guarding between the input and all other pins. Since this device does not use any of the extra pins, and has no provision for offset-nulling, but requires a compensation capacitor, some changes will be required in layout to convert to the ICL7650.

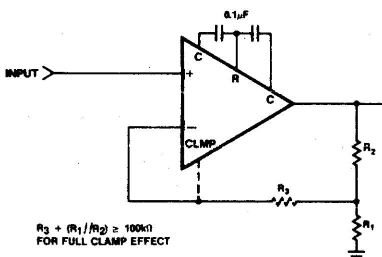
TYPICAL APPLICATIONS

Clearly the applications of the ICL7650 will mirror those of other op. amps. Thus, anywhere that the performance of a circuit can be significantly improved by a reduction of input-offset voltage and bias current, the ICL7650 is the logical choice. Basic non-inverting and inverting amplifier circuits are shown in Figs. 2 and 3. Both circuits can use the output clamping circuit to enhance the overload recovery performance. The only limitations on the replacement of other op. amps by the ICL7650 are the supply voltage (± 8V max.) and the output drive capability (10kΩ load for full swing). Even these limitations can be overcome using a simple booster circuit, as shown in Fig. 4, to enable the full output capabilities of the LM741 (or any other standard device) to be combined with the input capabilities of the ICL7650. The pair form a composite device, so loop gain stability, when the feedback network is added, should be watched carefully.

Fig. 5 shows the use of the clamp circuit to advantage in a zero-offset comparator. The usual problems in using a chopper stabilized amplifier in this application are avoided, since the clamp circuit forces the inverting input to follow the input signal. The threshold input must tolerate the output clamp current ≈ V_{IN}/R without disturbing other portions of the system.

Normal logarithmic amplifiers are limited in dynamic range in the voltage-input mode by their input-offset voltage. The built-in temperature compensation and convenience features of the ICL8048 can be extended to a voltage-input dynamic range of close to 6 decades by using the ICL7650 to offset-null the ICL8048, as shown in Fig. 6. The same concept can also be used with such devices as the HA2500 or HA2600 families of op amps. to add very low offset voltage capability to their very high slew rates and bandwidths. Note that these circuits will also have their DC gains, CMRR, and PSRR enhanced.

Mixing the ICL7650 with circuits operating at ±15V supplies requires the provision of a lower voltage. Although this can be met fairly easily, a highly efficient voltage divider can be built using the ICL7660 voltage converter circuit 'backwards'. A suitable connection is shown in Fig. 7.



NOTE: $R_1//R_2$ INDICATES THE PARALLEL COMBINATION OF R_1 AND R_2

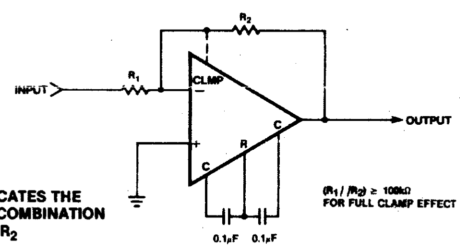


FIG. 2 NON INVERTING AMPLIFIER WITH (OPTIONAL) CLAMP

FIG. 3 INVERTING AMPLIFIER WITH (OPTIONAL) CLAMP

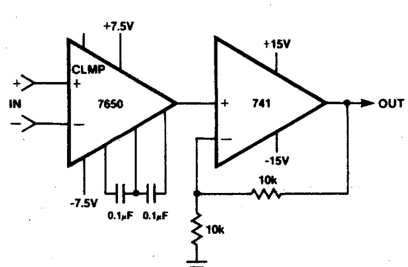


FIG. 4 USING 741 TO BOOST OUTPUT DRIVE CAPABILITY

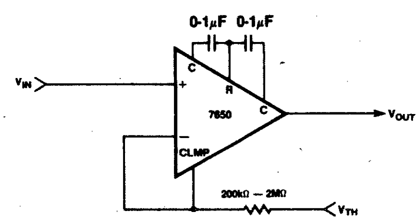


FIG. 5 LOW OFFSET COMPARATOR

TYPICAL APPLICATIONS (Continued)

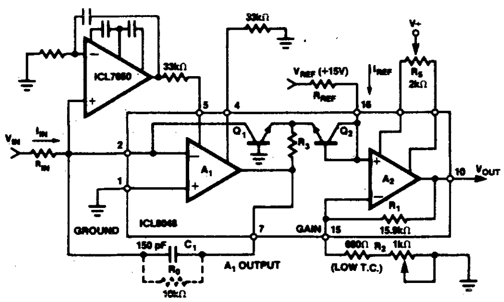


FIG. 6 ICL8048 OFFSET NULLED BY ICL7650

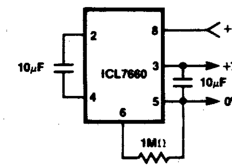
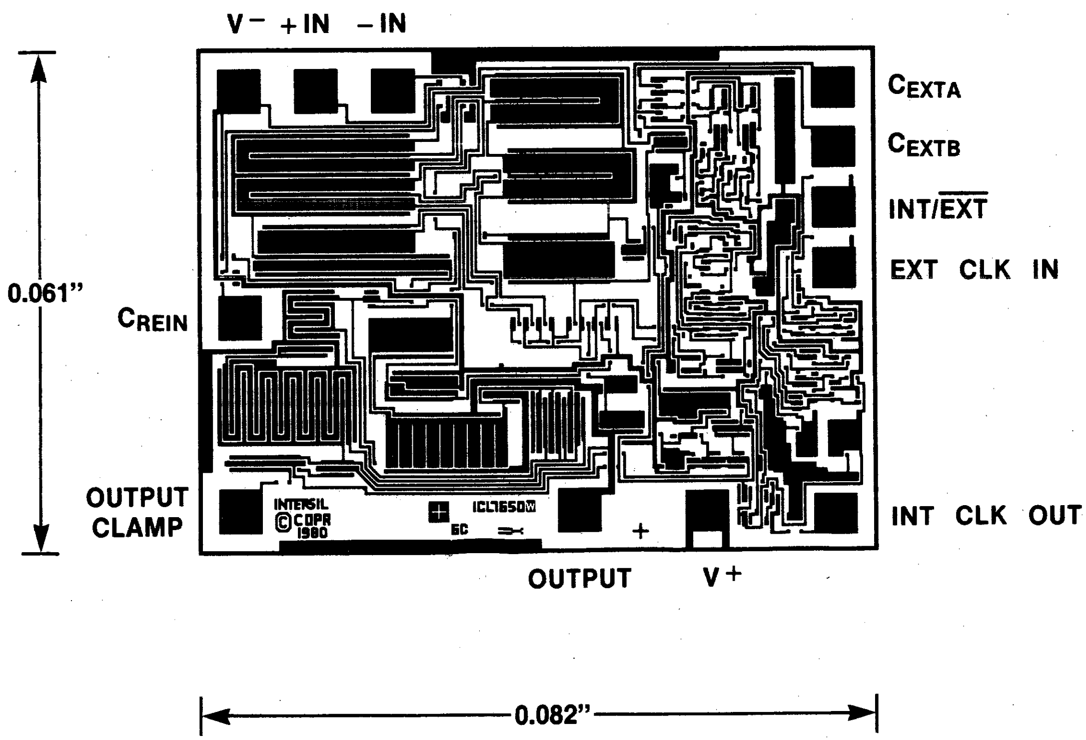


FIG. 7 SPLITTING +15V WITH ICL7660. SAME FOR −15V. >95% EFF.

FOR FURTHER APPLICATIONS ASSISTANCE, SEE A053 AND R017



INTERSIL

ICL7652

Chopper-Stabilized Operational Amplifier

FEATURES

- **Extremely low input offset voltage—1μV over temperature range**
- **Ultra low long-term and temperature drifts of input offset voltage (100nV/√month, 10nV/°C)**
- **Low DC input bias current—15pA**
- **Extremely high gain, CMRR and PSRR—min 110dB**
- **Low input noise voltage—0.2μVp-p (DC—1Hz)**
- **Internally compensated for unity-gain operation**
- **Very low intermodulation effects (open-loop phase shift < 2° @ chopper frequency)**
- **Clamp circuit to avoid overload recovery problems and allow comparator use**
- **Extremely low chopping spikes at input and output**

GENERAL DESCRIPTION

The ICL7652 chopper-stabilized amplifier offers exceptionally low input offset voltage and is extremely stable with respect to time and temperature. It is similar to INTERSIL's ICL7650 but offers improved noise performance and a wider common-mode input voltage range. The bandwidth and slew rate are reduced slightly.

INTERSIL's unique CMOS chopper-stabilized amplifier circuitry is user-transparent, virtually eliminating the traditional chopper amplifier problems of intermodulation effects, chopping spikes, and overrange lock-up.

The chopper amplifier achieves its low offset by comparing the inverting and non-inverting input voltages in a nulling amplifier, nulled by alternate clock phases. Two external capacitors are required to store the correcting potentials on the two amplifier nulling inputs; these are the only external components necessary.

The clock oscillator and all the other control circuitry is entirely self-contained, however the 14-pin version includes a provision for the use of an external clock, if required for a particular application. In addition, the ICL7652 is internally compensated for unity-gain operation.

ORDERING INFORMATION

TEMP RANGE	PACKAGE	ORDER#
0°C to +70°C	14-pin plastic	ICL7652CPD
−20°C to +85°C	14-pin CERDIP	ICL7652IJD
0°C to +70°C	8-pin TO-99	ICL7652CTV
−20°C to +85°C	8-pin TO-99	ICL7652ITV

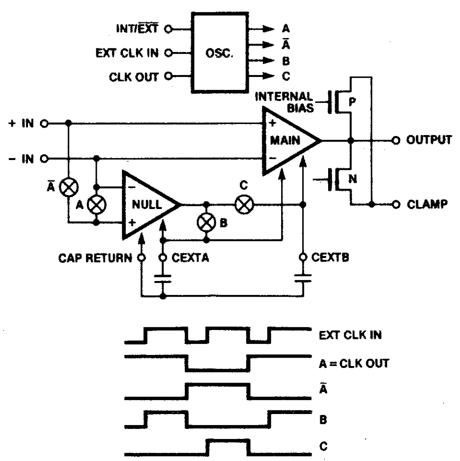
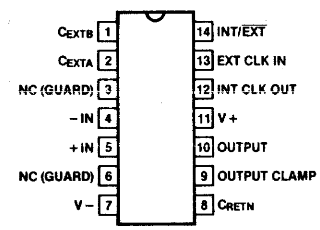
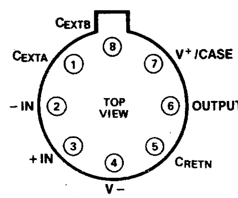


Figure 1. Block Diagram

PIN CONFIGURATIONS



14 Lead



TO-99

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
Input Voltage .... (V^+ + 0.3) to (V^- − 0.3) V
Storage Temperature Range .... −55°C to 150°C
Operating Temperature Range .... See Note 1
Lead Temperature (Soldering, 10 sec) ....300°C
Voltage on Oscillator Control Pins .... V^+ to V^-
Duration of Output Short Circuit .... Indefinite

Current into Any Pin 10mA
—while operating (Note 4) 100μA
Continuous Total Power Dissipation (T_A = 25°C)
CERDIP Package 500mW
Plastic Package 375mW
TO-99 .... 250mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS: Test Conditions: V^+ = +5V, V^- = −5V, T_A = +25°C, Test Circuit (unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Input Offset Voltage	V_{OS}	T_A = +25°C		±0.7	±5	μV
		Over Operating Temperature Range (Note 1)		±1.0		
Average Temperature Coefficient of Input Offset Voltage	$\frac{\Delta V_{OS}}{\Delta T}$	Operating Temperature Range (Note 1)		0.01	0.05	μV/°C
Input Bias Current (Doubles every 10°C above about 60°C)	I_{BIAS}	T_A = +25°C		15	30	pA
		0°C < T_A < +70°C		35		
		−20°C < T_A < +85°C		100		
Input Offset Current	I_{OS}	T_A = +25°C		25	60	pA
Input Resistance	R_{IN}			10^{12}		Ω
Large Signal Voltage Gain	A_{VOL}	R_L = 10kΩ, V_{OUT} = ±4V	120	150		dB
Output Voltage Swing (Note 3)	V_{OUT}	R_L = 10kΩ	±4.7	±4.85		V
		R_L = 100kΩ		±4.95		
Common-Mode Voltage Range	CMVR		−4.3	−4.8 to +4.0	3.5	V
Common-Mode Rejection Ratio	CMRR	CMVR = −4.3V to +3.5V	110	130		dB
Power Supply Rejection Ratio	PSRR	±3V to ±8V	110	130		dB
Input Noise Voltage	$e_{n_{p-p}}$	R_S = 100Ω, DC to 1Hz		0.2		μVp-p
		DC to 10Hz		0.7		
Input Noise Current	i_n	f = 10Hz		0.01		pA/√Hz
Unity-Gain Bandwidth	GBW			0.45		MHz
Slew Rate	SR	C_L = 50pF, R_L = 10kΩ		0.5		V/μs
Rise Time	t_r			0.8		μs
Overshoot				20		%
Operating Supply Range	V^+ to V^-		5.0		16	V
Supply Current	I_{SUPP}	No Load		2.0	3.5	mA
Internal Chopping Frequency	f_{ch}	Pins 12-14 Open (DIP)		400		Hz
Clamp ON Current (Note 2)		R_L = 100kΩ	25	100		μA
Clamp OFF Current (Note 2)		−4.0V < V_{OUT} < +4.0V		1		pA
Offset Voltage vs Time				100		nV/√month

Note 1: Operating temperature range for I series parts is −20°C to +85°C, for C series is 0°C to +70°C.
Note 2: See OUTPUT CLAMP under detailed description.
Note 3: OUTPUT CLAMP not connected. See typical characteristics curves for output swing vs clamp current characteristics.
Note 4: Limiting input current to 100μA is recommended to avoid latch-up problems. Typically 1mA is safe, however this is not guaranteed.

LINEAR

Intersil

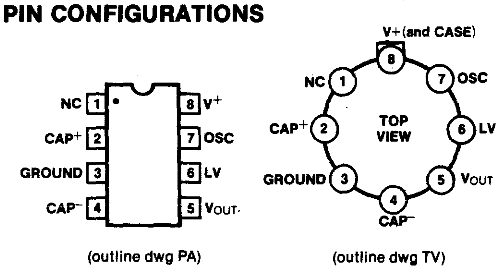
INTERSIL

ICL7660
Monolithic MAXCMOS™ Voltage Converter

FEATURES
- **Simple Conversion of +5V Logic Supply to ±5V Supplies**
- **Simple Voltage Multiplication (V_{OUT} = (−) nV_{IN})**
- **99.9% Typical Open Circuit Voltage Conversion Efficiency**
- **98% Typical Power Efficiency**
- **Wide Operating Voltage Range 1.5V to 10.0V**
- **Easy to use - Requires only 2 External Non-Critical Passive Components**

APPLICATIONS
- On Board Negative Supply for up to 64 Dynamic RAMs.
- Localized μ-Processor (8080 type) Negative Supplies
- Inexpensive Negative Supplies
- Data Acquisition Systems

PIN CONFIGURATIONS



ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE
ICL7660CTV	−20° to +70°C	TO-99
ICL7660CPA	−20° to +70°C	8 PIN MINI DIP
ICL7660MTV	−55° to +125°C	TO-99
ICL7660/D		DICE

GENERAL DESCRIPTION

The Intersil ICL7660 is a monolithic MAXCMOS™ power supply circuit which offers unique performance advantages over previously available devices. The ICL7660 performs the complete supply voltage conversion from positive to negative for an input range of +1.5V to +10.0V, resulting in complementary output voltages of −1.5 to −10.0V with the addition of only 2 non-critical external capacitors needed for the charge pump and charge reservoir functions. Note that an additional diode is required for V_{SUPPLY} >6.5V.

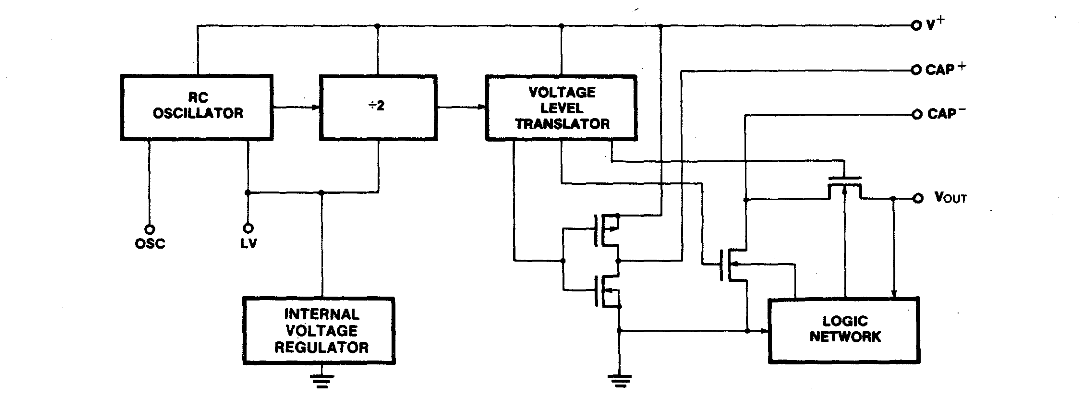
Contained on chip are a series DC power supply regulator, RC oscillator, voltage level translator, four output power MOS switches, and a unique logic element which senses the most negative voltage in the device and ensures that the output N-channel switches are not forward biased. This assures latch-up free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 5.0 volts. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be overdriven by an external clock.

The "LV" terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+3.5 to +10.0 volts), the LV pin is left floating to prevent device latchup.

Typical applications for the ICL7660 will be data acquisition and microprocessor based systems where there is a +5 volt supply available for the digital functions and an additional −5 volt supply is required for the analog functions. The ICL7660 is also ideally suited for providing low current, −5V body bias supply for dynamic RAMs.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage 10.5V
LV and OSC Input Voltage
(Note 1) .... -0.3V to (V+ +0.3V) for $V^+ < 5.5V$
(V+ -5.5V) to (V+ +0.3V) for $V^+ > 5.5V$
Current into LV (Note 1) .... 20μA for $V^+ > 3.5V$
Output Short Duration ($V_{SUPPLY} \leq 5.5V$) .... Continuous
Power Dissipation (Note 2)
ICL7660CTV 500mW
ICL7660CPA 300mW
ICL7660MTV 500mW

Operating Temperature Range
ICL7660M .... -55°C to +125°C
ICL7660C .... 0°C to 70°C
Storage Temperature Range .... -65°C to 150°C
Lead Temperature
(Soldering, 10 sec.) .... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

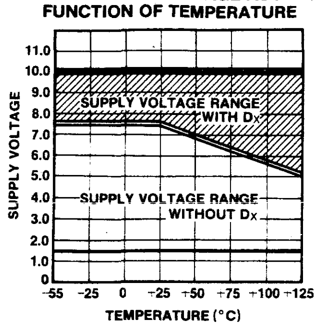
OPERATING CHARACTERISTICS $V^+ = 5V$, $T_A = 25°C$, $C_{OSC} = 0$, Test Circuit Figure 1 (unless otherwise specified)

SYMBOL	PARAMETER	LIMITS MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I^+	Supply Current		170	500	μA	$R_L = \infty$
V^+_{H1}	Supply Voltage Range - Hi	3.0		6.5	V	$0°C \leq T_A \leq 70°C$, $R_L = 10k\Omega$, LV Open
	(D_X out of circuit) (Note 3)	3.0		5.0	V	$-55°C \leq T_A \leq 125°C$, $R_L = 10k\Omega$, LV Open
V^+_{L1}	Supply Voltage Range - Lo (D_X out of circuit)	1.5		3.5	V	MIN ≤ T_A ≤ MAX, $R_L = 10k\Omega$, LV to GROUND
V^+_{H2}	Supply Voltage Range - Hi (D_X in circuit)	3.0		10.0	V	MIN ≤ T_A ≤ MAX, $R_L = 10k\Omega$, LV Open
V^+_{L2}	Supply Voltage Range - Lo (D_X in circuit)	1.5		3.5	V	MIN ≤ T_A ≤ MAX, $R_L = 10k\Omega$, LV to GROUND
R_{OUT}	Output Source Resistance		55	100	Ω	$I_{OUT} = 20mA$, $T_A = 25°C$
				120	Ω	$I_{OUT} = 20mA$, $-20°C \leq T_A \leq +70°C$
				150	Ω	$I_{OUT} = 20mA$, $-55°C \leq T_A \leq +125°C$ (Note 3)
				300	Ω	$V^+ = 2V$, $I_{OUT} = 3mA$, LV to GROUND $-20°C \leq T_A \leq +70°C$
				400	Ω	$V^+ = 2V$, $I_{OUT} = 3mA$, LV to GROUND, $-55°C \leq T_A \leq +125°C$, D_X in circuit (Note 3)
f_{OSC}	Oscillator Frequency		10		kHz	
P_{Ef}	Power Efficiency	95	98		%	$R_L = 5k\Omega$
$V_{OUT\ Ef}$	Voltage Conversion Efficiency	97	99.9		%	$R_L = \infty$
Z_{OSC}	Oscillator Impedance		1.0		MΩ	$V^+ = 2$ Volts
			100		kΩ	V = 5 Volts

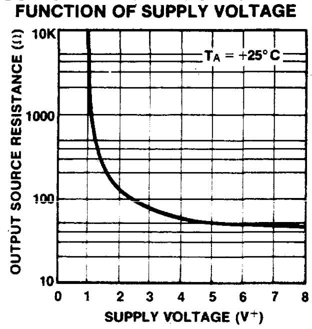
Notes: 1. Connecting any input terminal to voltages greater than V+ or less than GROUND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the ICL7660.
2. Derate linearly above 50°C by 5.5mW/°C.
3. ICL7660M only.

TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 1)

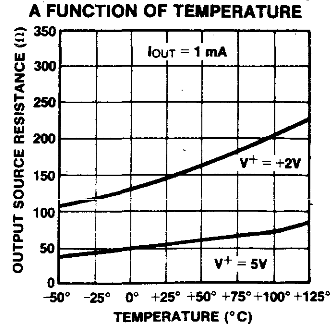
OPERATING VOLTAGE AS A FUNCTION OF TEMPERATURE



OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT SOURCE RESISTANCE AS A FUNCTION OF TEMPERATURE



TYPICAL APPLICATIONS

1. Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the ICL7660 for generation of negative supply voltages. Figure 4 shows typical connections to provide a negative supply where a positive supply is available. A similar scheme may be employed for supply voltages anywhere in the operating range of +1.5V to +10.0 volts, keeping in mind that pin 6 (LV) is tied to the supply negative (GND) only for supply voltages below 3.5 volts, and that diode D_X must be included for proper operation at higher voltages and/or elevated temperatures.

The output characteristics of the circuit in Figure 4 are those of a nearly ideal voltage source in series with 70 ohms. Thus for a load current of −10mA and a supply voltage of +5 volts, the output voltage will be −4.3 volts. The dynamic output impedance due to the capacitor impedances is approximately $1/\omega C$ where

$$C = C_1 = C_2$$

$$\text{giving} \quad \frac{1}{\omega C} = \frac{1}{2\pi f_{OSC} \times 10^{-5}} = 3 \text{ ohms}$$

for $C = 10\mu F$ and $f_{OSC} = 5kHz$ (1/2 of oscillator frequency)

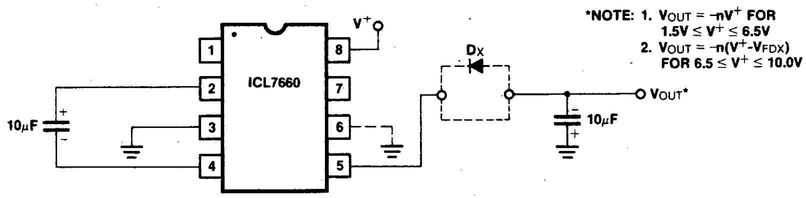


Figure 4: Simple Negative Converter

2. Paralleling Devices

Any number of ICL7660 voltage convertors may be paralleled to reduce output resistance. The reservoir capacitor, C_2, serves all devices while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately

$$R_{OUT} = \frac{R_{OUT} \text{ (of ICL7660)}}{n \text{ (number of devices)}}$$

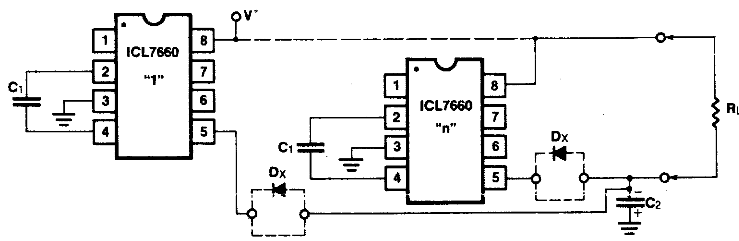


Figure 5: Paralleling Devices

3. Cascading Devices

The ICL7660 may be cascaded as shown to produce larger negative multiplication of the initial supply voltage, however, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n\,(V_{IN}),$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual ICL7660 R_{OUT} values.

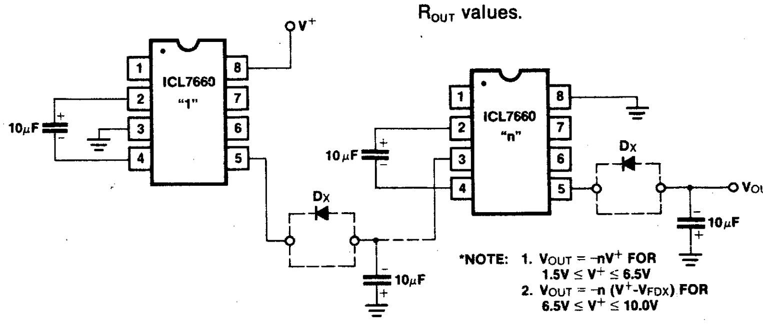
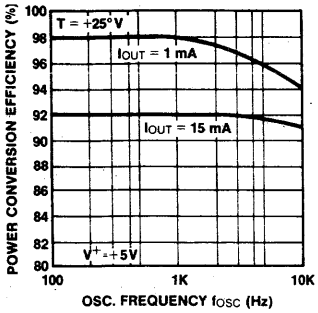
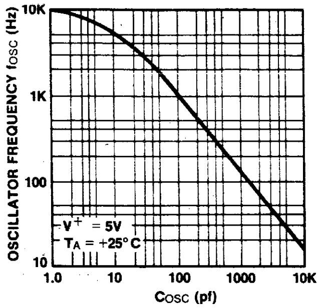


Figure 6: Cascading Devices for Increased Output Voltage

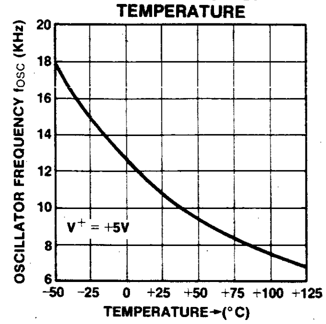
POWER CONVERSION EFFICIENCY AS A FUNCTION OF OSC. FREQUENCY



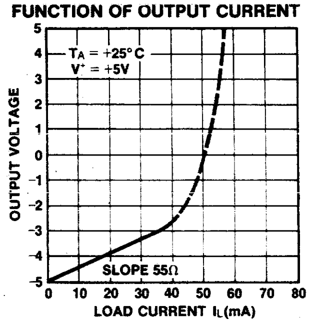
FREQUENCY OF OSCILLATION AS A FUNCTION OF EXTERNAL OSC. CAPACITANCE



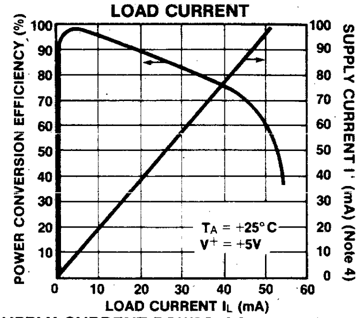
UNLOADED OSCILLATOR FREQUENCY AS A FUNCTION OF TEMPERATURE



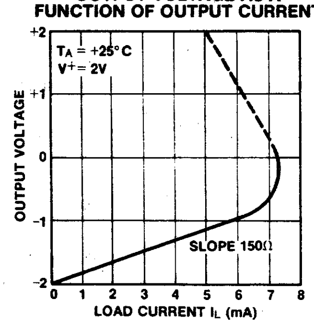
OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



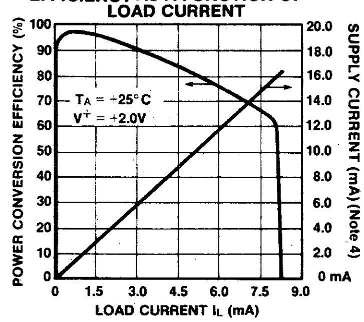
OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

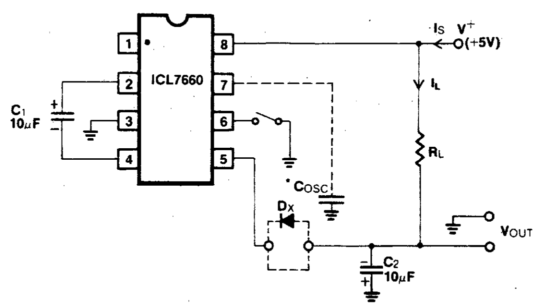


NOTE 4.

Note that the curves on the right include in the supply current that current fed directly into the load (R_L) from V^+ (see Figure 1). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the ICL7660, to the negative side of the load. Ideally, $V_{OUT} \simeq 2 V_{IN}$, $I_S \simeq 2 I_L$, so $V_{IN} \cdot I_S \simeq V_{OUT} \cdot I_L$.

SUPPLY CURRENT POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT





NOTES: 1. For large value of C_{OSC} (>1000pF) the values of C_1 and C_2 should be increased to 100μF.
2. D_X is required for supply voltages greater than 6.5V @ $-55° \leq T_A \leq +70°C$; refer to performance curves for additional information.

Figure 1: ICL7660 Test Circuit

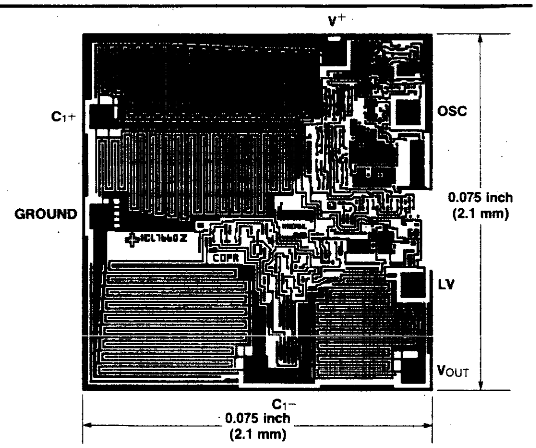


Figure 2: Chip Topography

LINEAR

Intersil

CIRCUIT DESCRIPTION

The ICL7660 contains all the necessary circuitry to complete a voltage doubler, with the exception of 2 external capacitors which may be inexpensive 10μF polarized electrolytic capacitors. The mode of operation of the device may be best understood by considering Figure 3, which shows an idealized voltage doubler. Capacitor C_1 is charged to a voltage, V^+, for the half cycle when switches S_1 and S_3 are closed. (Note: Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V^+ volts. Charge is then transferred from C_1 to C_2 such that the voltage on C_2 is exactly V^+, assuming ideal switches and no load on C_2. The ICL7660 approaches this ideal situation more closely than existing non-mechanical circuits.

In the ICL7660, the 4 switches in Figure 3 are MOS power switches; S_1 is a P-channel device and S_2, S_3 & S_4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 & S_4 must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit startup, and under output short circuit conditions ($V_{OUT} = V^+$), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

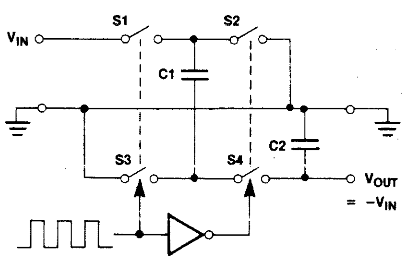


Figure 3. Idealized Voltage Doubler

This problem is eliminated in the ICL7660 by a logic network which senses the output voltage (V_{OUT}) together with the level translators and switches the substrates or S_3 & S_4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the ICL7660 is an integral part of the anti-latchup circuitry, however it's inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation the "LV" pin should be connected to GROUND, disabling the regulator. For supply voltages greater than 3.5 volts the LV terminal must be left open to insure latchup proof operation, and prevent device damage.

THEORETICAL POWER EFFICIENCY CONSIDERATIONS

In theory a voltage multiplier can approach 100% efficiency if certain conditions are met:

A The drive circuitry consumes minimal power

B The output switches have extremely low ON resistance and virtually no offset.

C The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The ICL7660 approaches these conditions for negative voltage multiplication if large values of C_1 and C_2 are used. **ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS.** The energy lost is defined by:

$$E = 1/2\, C_1\, (V_1{}^2 - V_2{}^2)$$

where V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Fig. 3) compared to the value of R_L, there will be a substantial difference in the voltages V_1 and V_2. Therefore it is not only desirable to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

DO'S AND DONTS

1 Do not exceed maximum supply voltages.
2 Do not connect LV terminal to GROUND for supply voltages greater than 3.5 volts.
3 Do not short circuit the output to V^+ supply for supply voltages above 5.5 volts for extended periods, however, transient conditions including startup are okay.
4 When using polarized capacitors, the + terminal of C_1 must be connected to pin 2 of the ICL7660 and the + terminal of C_2 must be connected to GROUND.
5 Add diode D_X as shown in Fig. 1 for hi-voltage, elevated temperature applications.

CONSIDERATIONS FOR HI VOLTAGE & ELEVATED TEMPERATURE

The ICL7660 will operate efficiently over its specified temperature range with only 2 external passive components (storage & pump capacitors), provided the operating supply voltage does not exceed 6.5 volts at +70°C and 5.0 volts at +125°C. Exceeding these maximums at the temperatures indicated may result in destructive latch-up of the ICL7660. (Ref: Graph "Operating Voltage Vs. Temperature")

Operation at supply voltages of up to 10.0 volts over the full temperature range without danger of latch-up can be achieved by adding a general purpose diode in series with the ICL7660 output, as shown by "D_X" in the circuit diagrams. The effect of this diode on overall circuit performance is the reduction of output voltage by one diode drop (approximately 0.6 volts).

4. Changing the ICL7660 Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to increase the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 7. In order to prevent possible device latchup, a 1kΩ resistor must be used in series with the clock output. In the situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10kΩ pullup resistor to V^- supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency. Output transitions occur on the positive-going edge of the clock.

It is also possible to increase the conversion efficiency of the ICL7660 at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is achieved by connecting an additional capacitor, C_{OSC}, as shown in Figure 8. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and reservoir (C_2) capacitors; this is overcome by increasing the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (Osc) and V^+ will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate a corresponding increase in the value of C_1 and C_2 (from 10μF to 100μF).

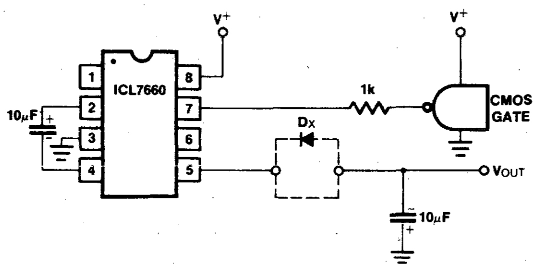


Figure 7: External Clocking

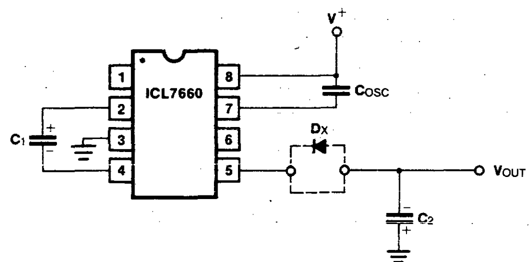


Figure 8: Lowering Oscillator Frequency

5. Positive Voltage Multiplication

The ICL7660 may be employed to achieve positive voltage multiplication using the circuit shown in Figure 9. In this application, the pump inverter switches of the ICL7660 are used to charge C_1 to a voltage level of $V^+ - V_F$ (where V^+ is the supply voltage and V_F is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage (V^+) is applied through diode D_2 to capacitor C_2. The voltage thus created on C_2 becomes $(2V^+) - (2V_F)$ or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for $V^+ = 5$ volts and an output current of 10mA it will be approximately 60 ohms.

6. Combined Negative Voltage Conversion and Positive Supply Multiplication

Figure 10 combines the functions shown in Figures 4 and 9 to provide negative voltage conversion and positive voltage multiplication simultaneously. This approach would be, for example, suitable for generating +9 volts and −5 volts from an existing +5 volt supply. In this instance capacitors C_1 and C_3 perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir respectively for the multiplied positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

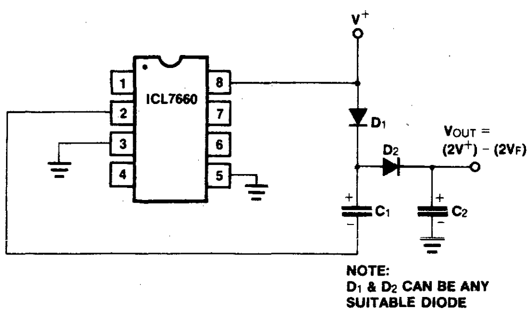


Figure 9: Positive Voltage Multiplier

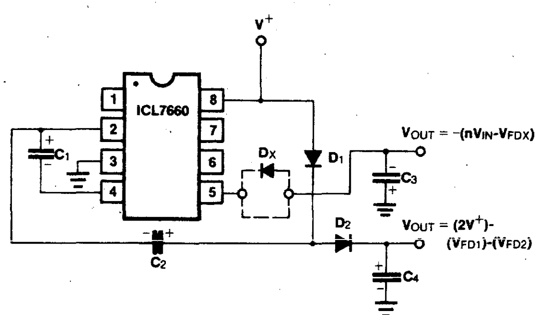


Figure 10: Combined Negative Converter and Positive Multiplier

7. Voltage Splitting

The bidirectional characteristics can also be used to split a higher supply in half, as shown in Figure 11. The combined load will be evenly shared between the two sides. Once again, a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 6, +15V can be converted (via +7.5, and −7.5) to a nominal −15V, though with rather high series resistance (~250Ω).

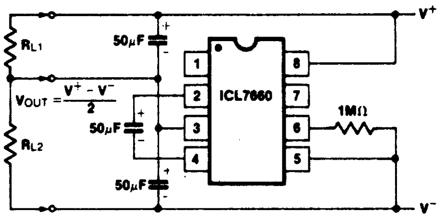


Figure 11: Splitting a Supply in Half.

ICL7660's output does not respond instantaneously to a change in input, but only after the switching delay. The circuit shown supplies enough delay to accommodate the 7660, while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown provides an output impedance of less than 5Ω to a load of 10mA.

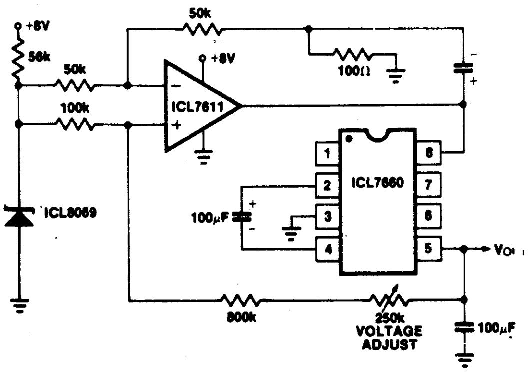


Figure 12: Regulating the Output Voltage

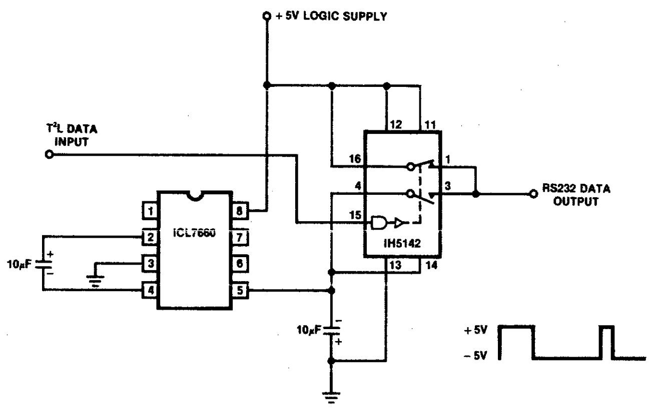


Figure 13: RS232 Levels from a Single 5V Supply

8. Regulated Negative Voltage Supply

In some cases, the output impedance of the ICL7660 can be a problem, particularly if the load current varies substantially. The circuit of Figure 12 can be used to overcome this by controlling the input voltage, via an ICL7611 low-power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is inadvisable, since the

OTHER APPLICATIONS

Further information on the operation and use of the ICL7660 may be found in A051 "Principals and Applications of the ICL7660 CMOS Voltage Converter" by Peter Bradshaw and Dave Bingham.

ICL7663/7664

CMOS Programmable Micropower Voltage Regulators

FEATURES

- **Ideal for battery-operated systems: less than 4µA typical current drain**
- **Will handle input voltages from 1.6V to 16V**
- **Very low input-output differential voltage**
- **1.3V bandgap voltage reference**
- **Up to 40mA output current**
- **Output shutdown via current-limit sensing or external logic signal**
- **Output voltages programmable from 1.3V to 16V**
- **Output voltages with programmable negative temperature coefficients (ICL7663 only)**

GENERAL DESCRIPTION

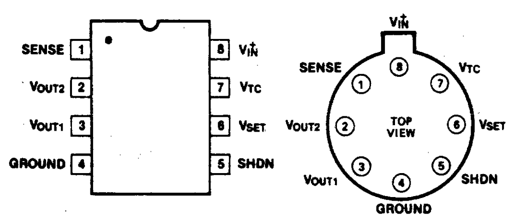
The ICL7663 (positive) and ICL7664 (negative) series regulators are low-power, high-efficiency devices which accept inputs from 1.6V to 16V and provide adjustable outputs over the same range at currents up to 40mA. Operating current is typically less than 4µA, regardless of load.

Output current sensing and remote shutdown are available on both devices, thereby providing protection for the regulators and the circuits they power. A unique feature, on the ICL7663 only, is a negative temperature coefficient output. This can be used, for example, to efficiently tailor the voltage applied to a multiplexed LCD through the driver (e.g., ICM7231/2/3/4) so as to extend the display operating temperature range many times.

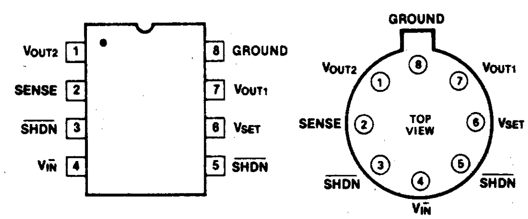
The ICL7663 and ICL7664 are available in either an 8-pin plastic minidip package or a TO-99 can.

PIN CONFIGURATIONS (outline dwgs PA, TV)

ICL7663 Positive Regulator



ICL7664 Negative Regulator



ORDERING INFORMATION

Positive Regulator		
ICL7663CPA	0°C to +70°C	8-pin minidip
ICL7663CTV	0°C to +70°C	TO-99
ICL7663/D		DICE

Negative Regulator		
ICL7664CPA	0°C to +70°C	8-pin minidip
ICL7664CTV	0°C to +70°C	TO-99
ICL7664/D		DICE

ABSOLUTE MAXIMUM RATINGS, ICL7663 POSITIVE REGULATOR

Input Supply Voltage .... +18V
Any Input or Output Voltage (Note 1) (GND − 0.3V) to
(Terminals 1, 2, 3, 5, 6, 7) .... (V_{IN}^{+} + 0.3V)
Output Source Current
(Terminal 2) 50mA
(Terminal 3) 25mA
Output Sinking Current (Terminal 7) .... −10mA
Power Dissipation (Note 2)
Minidip 200mW
TO-99 Can 300mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS V_{IN}^{+} = 9V, V_{OUT} = 5V, T_A = +25°C, test circuit unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Input Voltage	V_{IN}^{+}	T_A = +25°C 20°C ≤ T_A ≤ +70°C	1.5 1.6		16.0 16.0	V
Quiescent Current	I_Q	{ $R_L = \infty$, 1.4V ≤ V_{OUT} ≤ 8.5V } V_{IN}^{+} = 16V V_{IN}^{+} = 9V		4.0 3.5	12 10	μA
Reference Voltage	V_{SET}		1.2	1.3	1.4	V
Temperature Coefficient	$\frac{\Delta V_{SET}}{\Delta T}$	8.5V < V_{IN}^{+} < 9V		±200		ppm
Line Regulation	$\frac{\Delta V_{SET}}{V_{SET} \Delta V_{IN}}$	2V < V_{IN}^{+} < 15V		0.03		%/V
V_{SET} Input Current	I_{SET}			±0.01	10	nA
Shutdown Input Current	I_{SHDN}			±0.01	10	nA
Shutdown Input Voltage	V_{SHDN}	V_{SHDN}HI: Both V_{OUT} Disabled V_{SHDN}LO: Both V_{OUT} Enabled	1.4		 0.3	V
Sense Pin Input Current	I_{SENSE}			0.01	10	nA
Sense Pin Input Threshold Voltage	V_{CL}	$V_{CL} = V_{OUT2} - V_{SENSE}$ (Current-Limit Threshold)		0.7		V
Input-Output Saturation Resistance (Note 3)	R_{SAT}	V_{IN}^{+} = 2V V_{IN}^{+} = 9V V_{IN}^{+} = 15V		200 70 50		Ω
Load Regulation	$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	ΔI_{OUT1} = 100μA @ V_{OUT1} = 5V ΔI_{OUT2} = 10mA @ V_{OUT2} = 5V		2.0 1.0		Ω
Available Output Current (V_{OUT2})	I_{OUT2}	V_{IN}^{+} = 3V $V_{OUT} = V_{SET}$ V_{IN}^{+} = 9V V_{OUT} = 5V V_{IN}^{+} = 15V V_{OUT} = 5V	10 25 40			mA
Negative-Tempco Output (Note 4)	V_{TC}	Open-Circuit Voltage		0.9		V
	I_{TC}	Maximum Sink Current	0	8	2.0	mA
Temperature Coefficient	$\frac{\Delta V_{TC}}{\Delta T}$	Open Circuit		+2.5		mV/°C
Minimum Load Current	$I_{L(min)}$	(Includes V_{SET} Divider)			1.0	μA

Note 1: Connecting any terminal to voltages greater than (V_{IN}^{+} + 0.3V) or less than (GND − 0.3V) may cause destructive device latch-up. It is recommended that no inputs from sources operating on external power supplies be applied prior to ICL7663 power-up.

Note 2: Derate linearly above 50°C at 5mW/°C for minidip and 7.5mW/°C for TO-99 can.

Note 3: This parameter refers to the saturation resistance of the MOS pass transistor. The minimum input-output voltage differential at low current (under 5mA), can be determined by multiplying the load current (including set resistor current, but not quiescent current) by this resistance.

Note 4: This output has a positive temperature coefficient. Using it in combination with the inverting input of the regulator at V_{SET}, a negative coefficient results in the output voltage. See Figure 3 for details. Pin will not source current.

ABSOLUTE MAXIMUM RATINGS, ICL7664 NEGATIVE REGULATOR

Input Supply Voltage .... $-18V$
Any Input or Output Voltage (Note 1) (GND +0.3V) to
(Terminals 1, 2, 3, 5, 6, 7) .... (V_{IN}^{-} −0.3V)
Output Sink Current
(Terminals 1, 7) .... −25mA

Power Dissipation (Note 2)
Minidip 200mW
TO-99 Can 300mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CHARACTERISTICS $V_{IN}^{-} = -9V$, $V_{OUT} = -5V$, $T_A = +25°C$, test circuit unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}^{-}	$T_A = +25°C$ $0°C \le T_A \le +70°C$	−1.5 −1.6		−16.0 −16.0	V
Quiescent Current	I_Q	$\{R_L = \infty$, $-1.4V \le V_{OUT} \le -8.5V\}$ $V_{IN}^{-} = 16V$ $V_{IN}^{-} = 9V$		4.0 3.5	12 10	μA
Reference Voltage	V_{SET}		−1.2	−1.3	−1.4	V
Temperature Coefficient	$\frac{\Delta V_{SET}}{\Delta T}$	$-8.5V < V_{IN}^{-} < -9V$		±200		ppm
Line Regulation	$\frac{\Delta V_{SET}}{V_{SET}\Delta V_{IN}}$	$-2V < V_{IN}^{-} < -15V$		0.03		%/V
V_{SET} Input Current	I_{SET}			±0.01	10	nA
Shutdown Input Current	$I_{\overline{SHDN}}$			±0.01	10	nA
Shutdown Input Voltage	$V_{\overline{SHDN}}$	$V_{\overline{SHDN}}$HI: Both V_{OUT} Enabled $V_{\overline{SHDN}}$LO: Both V_{OUT} Disabled	−0.3		 −1.4	V
Sense Pin Input Current	I_{SENSE}			0.01	10	nA
Sense Pin Input Threshold Voltage	V_{CL}	$V_{CL} = V_{OUT2} - V_{SENSE}$ (Current-Limit Threshold)		−0.35		V
Input-Output Saturation Resistance (Note 3)	R_{SAT}	$V_{IN}^{-} = 2V$ $V_{IN}^{-} = 9V$ $V_{IN}^{-} = 15V$		150 40 30		Ω
Load Regulation	$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	$\Delta I_{OUT} = 100\mu A$ @ $V_{OUT} = -5V$		2.0		Ω
Output Current, V_{OUT1} or V_{OUT2}	I_{OUT}	$V_{IN}^{-} = 3V$ $V_{OUT} = V_{SET}$ $V_{IN}^{-} = 9V$ $V_{OUT} = -5V$ $V_{IN}^{-} = 15V$ $V_{OUT} = -5V$		−2 −20 −40		mA
Minimum Load Current (Includes V_{SET} Divider)	$I_{L(min)}$				1.0	μA

Note 1: Connecting any terminal to voltages greater than (GND +0.3V) or less than (V_{IN}^{-} −0.3V) may cause destructive device latch-up. It is recommended that no inputs from sources operating on external power supplies be applied prior to ICL7664 power-up.

Note 2: Derate linearly above 50°C at 5mW/°C for minidip and 7.5mW/°C for TO-99 can.

Note 3: This parameter refers to the saturation resistance of the MOS pass transistor. The minimum input-output voltage differential can be determined by multiplying the load current (including set resistor current, but not quiescent current) by this resistance.

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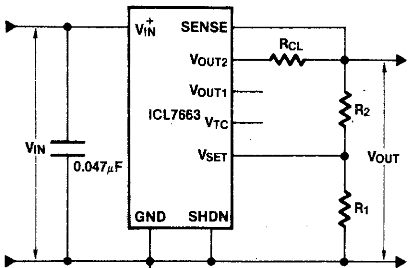
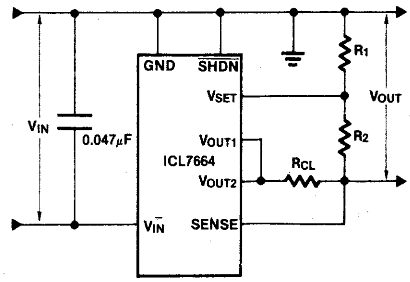
APPLICATIONS



$$V_{OUT} = \frac{R_2 + R_1}{R_1} V_{SET}$$

$$I_{CL} = \frac{0.7V}{R_{CL}}$$

Figure 4. Basic Application of ICL7663 as Positive Regulator with Current Limit



$$V_{OUT} = \frac{R_2 + R_1}{R_1} V_{SET}$$

$$I_{CL} = \frac{0.35V}{R_{CL}}$$

Figure 5. Basic Application of ICL7664 as Negative Regulator with Current Limit

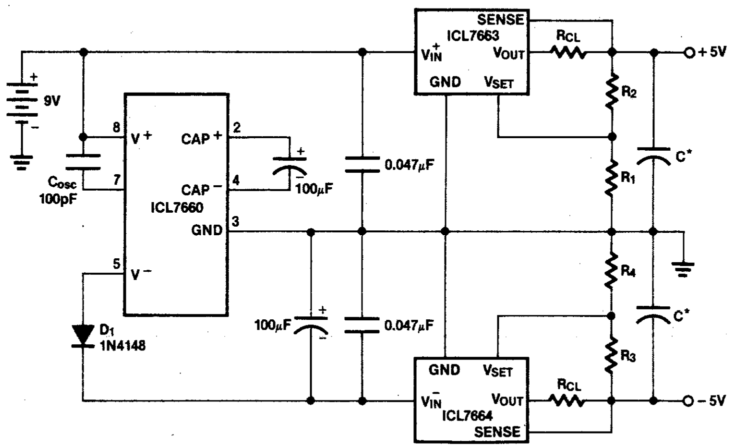


Figure 6. Generating regulated split supplies from a single supply. The oscillation frequency of the ICL7660 is reduced by the external oscillator capacitor, so that it inverts the battery voltage more efficiently.

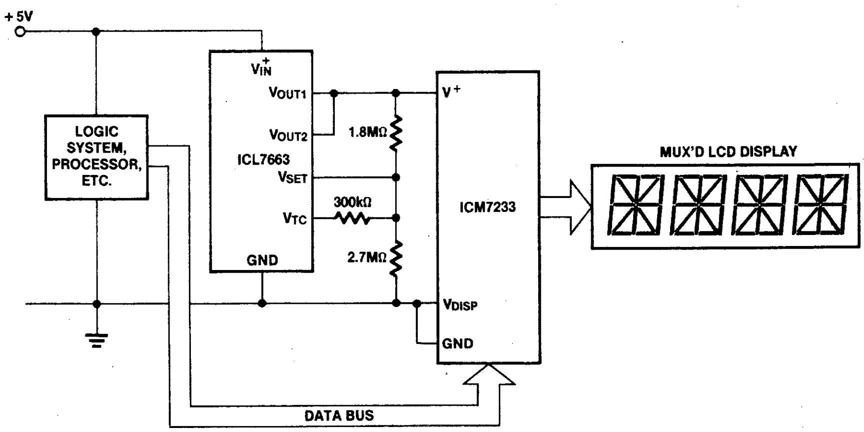


Figure 7. Driving a Multiplexed LCD Display. The negative temperature coefficient drive voltage to the displays allows consistent operation over more than 40°C temperature span, as opposed to about 10°C with a fixed drive voltage. Values based on EPSON LDB-728 display or similar.

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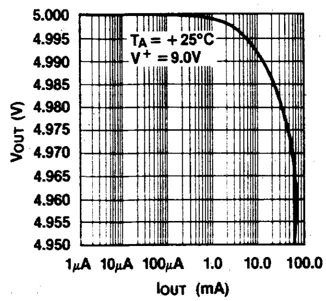
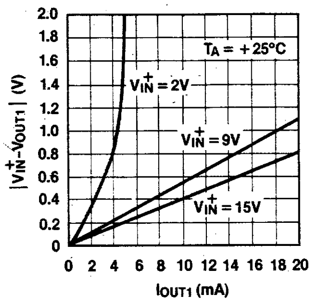
TYPICAL CHARACTERISTICS

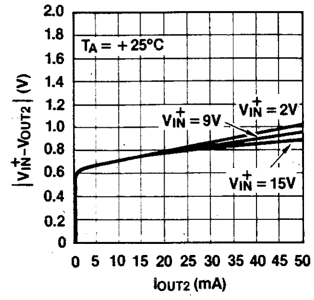
ICL7663
Output Voltage as a
Function of Output Current



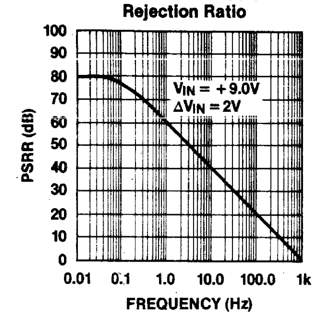
ICL7663
VOUT1 Input-Output Differential
vs Output Current



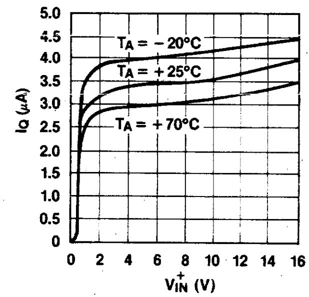
ICL7663
VOUT2 Input-Output Differential
vs Output Current



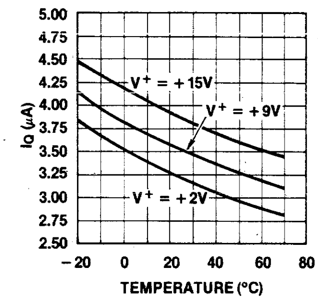
ICL7663
Input Power Supply
Rejection Ratio



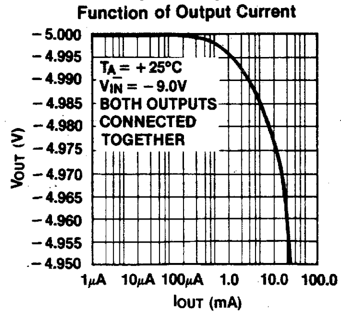
ICL7663
Quiescent Current as a
Function of Input Voltage



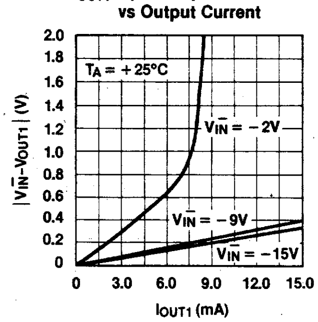
ICL7663
Quiescent Current as a
Function of Temperature



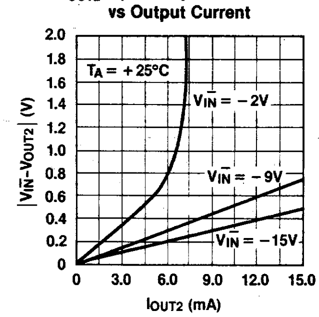
ICL7664
Output Voltage as a
Function of Output Current



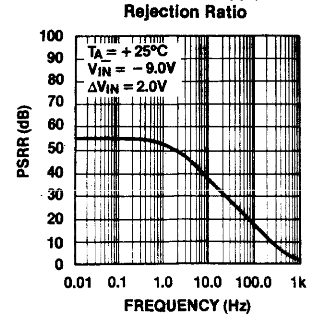
ICL7664
VOUT1 Input-Output Differential
vs Output Current



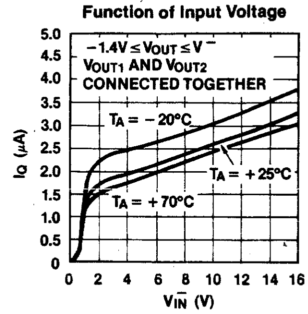
ICL7664
VOUT2 Input-Output Differential
vs Output Current



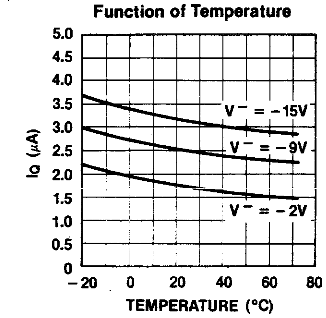
ICL7664
Input Power Supply
Rejection Ratio



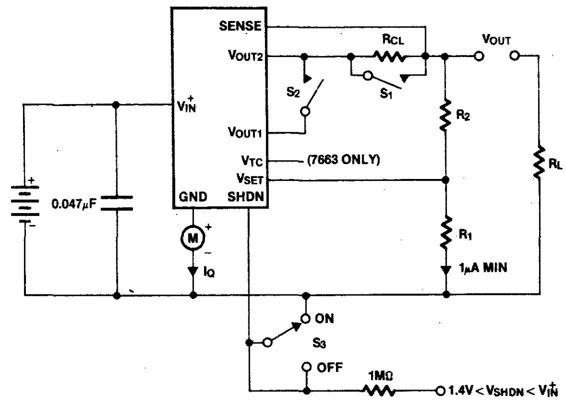
ICL7664
Quiescent Current as a
Function of Input Voltage



ICL7664
Quiescent Current as a
Function of Temperature



TEST CIRCUIT



Note 1: S_1 when closed, disables output current limiting
Note 2: For ICL7664, exchange V_{OUT1} and V_{OUT2}. S_2 action differs, as follows:

Device	S_2 Closed	S_2 Open
ICL7663	V_{OUT1}	V_{OUT2}
ICL7664	$V_{OUT1} + V_{OUT2}$	V_{OUT1}

Note 3: $V_{OUT} = \frac{R_2 + R_1}{R_1} V_{SET}$
Note 4: I_Q quiescent current is measured at GND pin by meter M
Note 5: S_3 when ON, permits normal operation, when OFF, shuts down both V_{OUT1} and V_{OUT2}

Test Circuit for ICL7663/64 (Polarities shown are for ICL7663. Reverse for ICL7664)

DETAILED DESCRIPTION

The ICL7663 and ICL7664 are CMOS integrated circuits which contain all the functions of a voltage regulator plus protection circuitry on a single monolithic chip. Referring to the block diagrams (Figures 1 and 2), each contains a bandgap-type voltage reference of 1.3 Volts; this voltage, therefore, is the lowest output voltage the regulators can control (−1.3V for the ICL7664). Error amplifier A drives either a P-channel (ICL7663) or an N-channel (ICL7664) pass transistor which is sufficient for low (under about 5mA) currents; this transistor is augmented by a duplicate in the ICL7664, which permits higher current outputs. In the ICL7663, the high current output is formed by an NPN transistor connected as a follower. This configuration gives more gain and lower output impedance.

Logic-controlled shutdown is implemented via an MOS transistor of the appropriate polarity. Current-sensing is achieved with comparator C, which functions with the V_{OUT2} line on each chip. Finally, the positive regulator (ICL7663 only) has an output (V_{TC}) from a buffer amplifier (B), which can be used to generate programmable-temperature-coefficient output voltages.

The amplifiers, reference and comparator circuitry all operate at bias levels well below 1μA to achieve the extremely low quiescent current. This does limit the dynamic response of the circuits, however, and transients are best dealt with outside the regulator loop.

BASIC OPERATION

The ICL7663 and ICL7664 are designed to regulate battery voltages in the 5V to 15V region at maximum load currents of about 5mA to 30mA. Although intended as low power devices, power dissipation limits must be observed. For example, the power dissipation in the case of a 15V supply regulated down to 5V with a load current of 30mA clearly exceeds the power dissipation rating of the minidip: (15-5) (30) (10^{-3}) = 300mW. The test circuit illustrates proper use of the devices. Although the following discussion refers to the ICL7663, it applies as well to the parallel features of the ICL7664 as long as the appropriate polarities are reversed. Individual features and precautions will be discussed where appropriate.

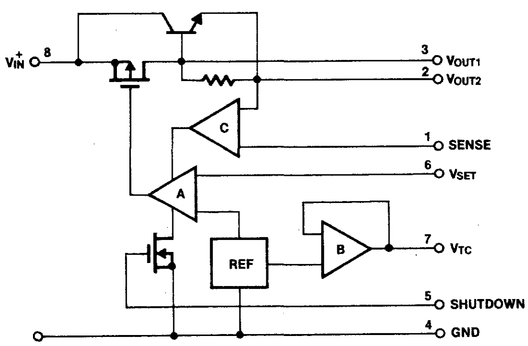


Figure 1. Block Diagram of the ICL7663

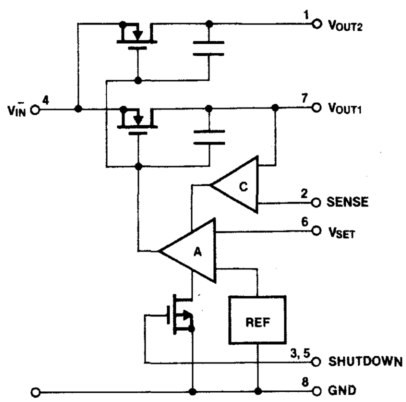


Figure 2. Block Diagram of the ICL7664

CMOS devices generally require two precautions: every input pin must go somewhere, and maximum values of applied voltages and current limits must be rigorously observed. Neglecting these precautions may lead to, at the least, incorrect or non-operation, and at worst, destructive device failure. To avoid the problem of latchup, do not apply inputs to any pins before supply voltage is applied.

Input Voltages—These regulators accept working inputs of about 1.4V to 16V. When power is applied, the rate-of-rise of the input may be hundreds of volts per microsecond. This is potentially harmful to the regulators, where internal operating currents are in the nanoampere range. The 0.047μF capacitor on the device side of the switch will limit inputs to a safe level around 2V/μs. Use of this capacitor is suggested in all applications. In severe rate-of-rise cases, it may be advisable to use an RC network on the SHutDowN pin to delay output turn-on. Battery charging surges, transients, and assorted noise signals should be kept from the regulators by RC filtering, zener protection, or even fusing.

Output Voltages—The resistor divider R_2/R_1 is used to scale the reference voltage, V_{SET}, to the desired output using the formula $V_{OUT} = (1 + R_2/R_1)\, V_{SET}$. In the ICL7664, V_{IN}^- and V_{SET} are negative, so V_{OUT} will be also. Suitable arrangements of these resistors, using a potentiometer, enables exact values for V_{OUT} to be obtained. Because of the low leakage current of the V_{SET} terminal, these resistors can be tens of megohms for minimum additional quiescent drain current. However, *some* load current is required for proper operation, so for extremely low-drain applications it is necessary to draw at least 1μA. This can include the current for R_2 and R_1.

Output voltages up to nearly the V_{IN} supply may be obtained at low load currents, while the low limit is the reference voltage. The minimum input-output differential in each regulator is obtained using the V_{OUT1} terminal.

Output Currents—For the ICL7663, low output currents of less than 5mA are obtained with the least input-output differential from the V_{OUT1} terminal (connect V_{OUT2} to V_{OUT1}). Either output may be used on the ICL7664, with the unused output connected to V_{IN}^-. Where higher currents are needed, use V_{OUT2} on the ICL7663 (V_{OUT1} should be left open in this case) and parallel V_{OUT1} and V_{OUT2} on the ICL7664.

High output currents can be obtained only as far as package dissipation allows. It is strongly recommended that output current-limit sensing be used in such cases.

Current-Limit Sensing—The on-chip comparator (C in the block diagrams) permits shutdown of the regulator output in the event of excessive current drain. As the test circuits show, a current-limiting resistor, R_{CL}, is placed in series with V_{OUT2}, and the SENSE terminal is connected to the load side of R_{CL}. When the current through R_{CL} is high enough to produce a voltage drop equal to V_{CL} (0.7V for ICL7663, 0.35V for ICL7664) the voltage feedback is bypassed and the regulator output will be limited to this current. Therefore, when the maximum load current (I_{LOAD}) is determined, simply divide V_{CL} by I_{LOAD} to obtain the value for R_{CL}.

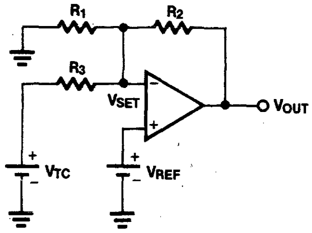
Logic-Controllable Shutdown—When equipment is not needed continuously (e.g., in remote data-acquisition systems), it is desirable to eliminate its drain on the system until it *is* required. This usually means switches, with their unreliable contacts. Instead, the ICL7663 and ICL7664 can be shut down by a logic signal, leaving only I_Q (under 4μA) as a drain on the power source. Since this pin must not be left open, it should be tied to ground if not needed. A voltage of less than 0.3V for the ICL7663, and greater than −0.3V for the ICL7664 will keep the regulator ON, and a voltage level of more than 1.4V but less than V_{IN}^+ for the ICL7663, and less than −1.4V but not less than V_{IN}^- for the ICL7664 control will turn the outputs OFF. If there is a possibility that the control signal could exceed the regulator input (V_{IN}^+ or V_{IN}^-), the current from this signal should be limited to 100μA maximum by a high-value (1MΩ) series resistor. This situation may occur when the logic signal originates from a separately-powered system from that of the regulator.

Additional Circuit Precautions—These regulators have poor rejection of voltage fluctuations from AC sources above 10Hz or so. To prevent the output from responding (where this might be a problem), a reservoir capacitor across the load is advised. The value of this capacitor is chosen so that the regulated output voltage reaches 90% of its final value in 20ms. From

$$I = C\frac{\Delta V}{\Delta t},\; C = I_{OUT}\frac{(20 \times 10^{-3})}{0.9V_{OUT}} = 0.022\frac{I_{OUT}}{V_{OUT}}.$$

In addition, where such a capacitor is used, a current-limiting resistor is also suggested (see **"Current-Limit Sensing"**).

Producing Output Voltages With Negative Temperature Coefficients—The ICL7663 has an additional output (not present on the ICL7664) which is 0.9V relative to GND and has a tempco of +2.5mV/°C. By applying this voltage to the inverting input of amplifier A (i.e., the V_{SET} pin), output voltages having negative TC may be produced. The TC of the output voltage is controlled by the R_2/R_3 ratio (see Figure 3 and its design equations).



EQ. 1: $V_{OUT} = V_{SET}\left(1 + \frac{R_2}{R_1}\right) + \frac{R_2}{R_3}(V_{SET} - V_{TC})$

EQ. 2: $TC\,V_{OUT} = -\frac{R_2}{R_3}(TC\,V_{TC})$ in mV/°C

WHERE: $V_{SET} = 1.3V$
$V_{TC} = 0.9V$
$TCV_{TC} = +2.5mV/°C$

Figure 3. Generating Negative Temperature Coefficients

APPLICATIONS (Continued)

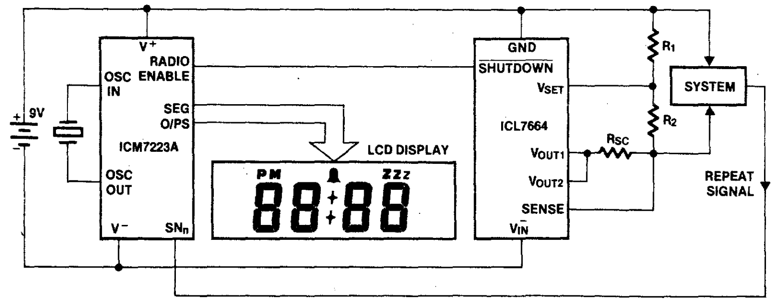
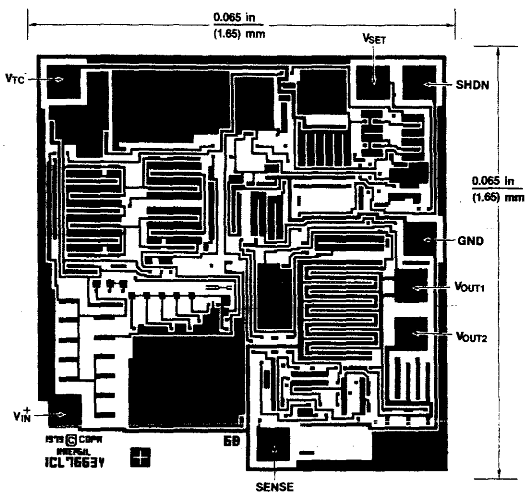
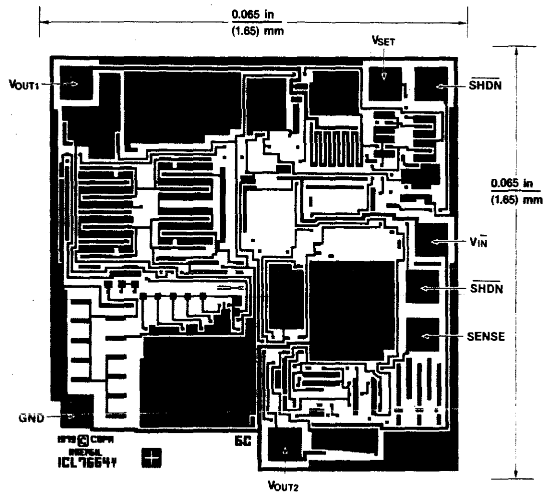


Figure 8. Once a Day System. This circuit will turn on a regulated supply to a system for one minute every day, via the SHUTDOWN pin on the ICL7664, and under control of the ICM7223A Alarm Clock circuit. If the system decides it needs another one minute activation, pulling the REPEAT line to V+ (GND) during one activation will trigger a subsequent activation after a **snooze** interval set by the choice of SN pins (2 mins shown). Alternatively, activation of the **Sleep** timer, without pause, can be achieved. See ICM7223A data sheet for details.

CHIP TOPOGRAPHIES



ICL7663



ICL7664

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ICL7665

Micropower Under-/ Over-Voltage Detector

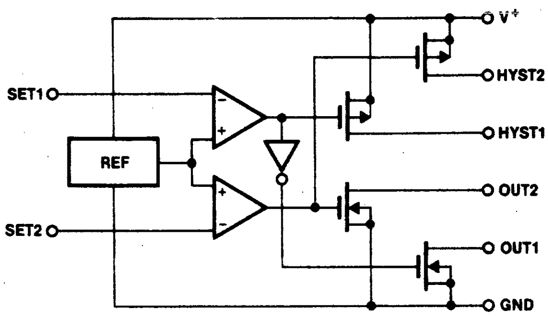
FEATURES

- Exceptionally low supply current ($<3\mu A$ typ)
- Individually programmable upper and lower trip voltages and hysteresis levels
- Accurate on-chip bandgap reference, used by both detectors
- Up to 20mA output current sinking ability
- Wide supply voltage range

GENERAL DESCRIPTION

The ICL7665 contains two individually programmable voltage detectors on a single chip. Requiring only $\sim 3\mu A$ for operation, the device is intended for battery-operated systems and instruments which require high or low voltage warnings, settable trip points, or fault monitoring and correction. Typical applications are battery-backup computer memories, battery-operated medical devices, radiation dosimeters, pocket pagers, portable calibrators and test instruments, and charging systems.

BLOCK DIAGRAM



Conditions*

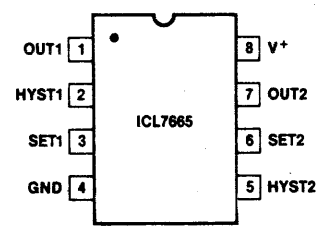
$V_{SET1} > 1.3V$, OUT1 switch ON — HYST1 switch ON
$V_{SET1} < 1.3V$, OUT1 switch OFF — HYST1 switch OFF
$V_{SET2} > 1.3V$, OUT2 switch OFF — HYST2 switch ON
$V_{SET2} < 1.3V$, OUT2 switch ON — HYST2 switch OFF

*See Operating Characteristics for exact thresholds.

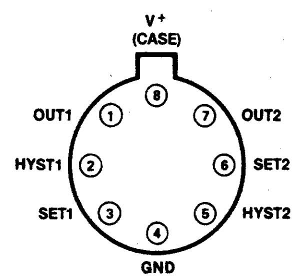
ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7665PA	−20°C to +70°C	8 Lead MiniDIP
ICL7665TV	−20°C to +70°C	8 Lead TO-99
ICL7665/D	—	DICE Only

PIN CONFIGURATIONS



(outline dwg PA)



(outline dwg TV)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . −0.3V to +18V
Output Voltages OUT1 and OUT2
(with respect to GND) (Note 2) . . . . −0.3V to +18V
Output Voltages HYST1 and HYST2
(with respect to V^+) (Note 2) . . . . +0.3V to −18V
Input Voltages SET1 and SET2
(Note 2) . . . . (GND − 0.3V) to (V^+ +0.3V)
Maximum Sink Output Current OUT1 and OUT2 . . . . . . 25mA
Maximum Source Output Current
HYST1 and HYST2 . . . . −25mA
Power Dissipation (Note 1) 200mW
Operating Temperature Range . . . . −20°C to +70°C
Storage Temperature Range . . . . −55°C to +125°C

Note 1: Derate above +25°C ambient temperature at 4mW/°C.

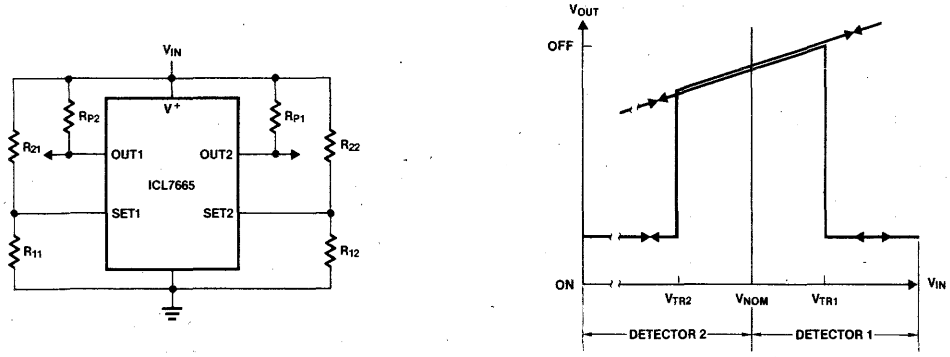
Note 2: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than (V^+ +0.3V) or less than (GND − 0.3V) may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICL7665 be turned on first. If this is not possible, currents into inputs and/or outputs must be limited to ±0.5mA and voltages must not exceed those defined above.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC OPERATING CHARACTERISTICS (V^+ = 5V, T_A = +25°C, test circuit unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Operating Supply Voltage	V^+	T_A = +25°C	1.6		16.0	V
		−20°C ≤ T_A ≤ +70°C	1.8		16.0	
Supply Current	I^+	GND ≤ V_{SET1}, V_{SET2} ≤ V^+ All Outputs Open Circuit				
		V^+ = 2V		2.5	10	μA
		V^+ = 9V		2.6	10	
		V^+ = 15V		2.9	15	
Input Trip Voltage	V_{SET1}		1.15	1.3	1.45	V
	V_{SET2}		1.2	1.3	1.4	
Temperature Coefficient of V_{SET}	$\frac{\Delta V_{SET}}{\Delta T}$			200		ppm/°C
Supply Voltage Sensitivity of V_{SET1}, V_{SET2}	$\frac{\Delta V_{SET}}{\Delta V_S}$	R_{OUT1}, R_{OUT2}, R_{HYST1}, R_{HYST2} = 1 MΩ		0.004		%/V
Output Leakage Currents on OUT and HYST	I_{OLK}	V_{SET} = 0V or V_{SET} ≥ 2V		10	200	nA
	I_{HLK}			−10	−100	
	I_{OLK}	V^+ = 15V, T_A = 70°C			2000	
	I_{HLK}	V^+ = 15V, T_A = 70°C			−500	
Output Saturation Voltages	V_{OUT1}	V^+ = 2V, V_{SET1} = 2V, I_{OUT1} = 2mA		0.2	0.5	V
	V_{OUT1}	V^+ = 5V, V_{SET1} = 2V, I_{OUT1} = 2mA		0.1	0.3	
	V_{OUT1}	V^+ = 15V, V_{SET1} = 2V, I_{OUT1} = 2mA		0.06	0.2	
	V_{HYST1}	V^+ = 2V, V_{SET1} = 2V, I_{HYST1} = −0.5mA		−0.15	−0.3	
	V_{HYST1}	V^+ = 5V, V_{SET1} = 2V, I_{HYST1} = −0.5mA		−0.05	−0.15	
	V_{HYST1}	V^+ = 15V, V_{SET1} = 2V, I_{HYST1} = −0.5mA		−0.02	−0.10	
	V_{OUT2}	V^+ = 2V, V_{SET2} = 0V, I_{OUT2} = 2mA		0.2	0.5	
	V_{OUT2}	V^+ = 5V, V_{SET2} = 0V, I_{OUT2} = 2mA		0.15	0.3	
	V_{OUT2}	V^+ = 15V, V_{SET2} = 0V, I_{OUT2} = 2mA		0.11	0.25	
	V_{HYST2}	V^+ = 2V, V_{SET2} = 2V, I_{HYST2} = −0.2mA		−0.25	−0.8	
	V_{HYST2}	V^+ = 5V, V_{SET2} = 2V, I_{HYST2} = −0.5mA		−0.43	−1.0	
	V_{HYST2}	V^+ = 15V, V_{SET2} = 2V, I_{HYST2} = −0.5mA		−0.35	−0.8	
V_{SET} Input Leakage Current	I_{SET}	GND ≤ V_{SET} ≤ V^+		0.01	10	nA
ΔV_{SET} Input for Complete Output Change	ΔV_{SET}	R_{OUT} = 4.7kΩ, R_{HYST} = 20kΩ V_{OUT}LO = 1% V^+, V_{OUT}HI = 99% V^+		1		mV
Difference in Trip Voltages	$V_{SET1} - V_{SET2}$	R_{OUT}, R_{HYST} = 1MΩ		±5	±50	
Output/Hysteresis Difference		R_{OUT}, R_{HYST} = 1MΩ		±1		

APPLICATIONS



(a) Circuit Configuration (b) Transfer Characteristics

Figure 1. Simple Threshold Detector

Figure 1 shows the simplest connection of the ICL7665 for threshold detection. From the graph (b), it can be seen that at low input voltages OUT1 is OFF, or high, while OUT2 is ON, or low. As the input rises (e.g. at power-on) toward V_{NOM} (usually the eventual operating voltage), OUT2 goes high on reaching V_{TR2}. If the voltage rises above V_{NOM} as much as V_{TR1}, OUT1 goes low. The equations giving V_{SET1} and V_{SET2} are, from Figure 1(a):

$$V_{SET1} = V_{IN} \frac{R_{11}}{(R_{11} + R_{21})} \qquad V_{SET2} = V_{IN} \frac{R_{12}}{(R_{12} + R_{22})}$$

Since the voltage to trip each comparator is nominally 1.3V, the value of V_{IN} for each trip point can be found from

$$V_{TR1} = V_{SET1} \frac{(R_{11} + R_{21})}{R_{11}} = 1.3 \frac{(R_{11} + R_{21})}{R_{11}} \text{ for detector 1 and}$$

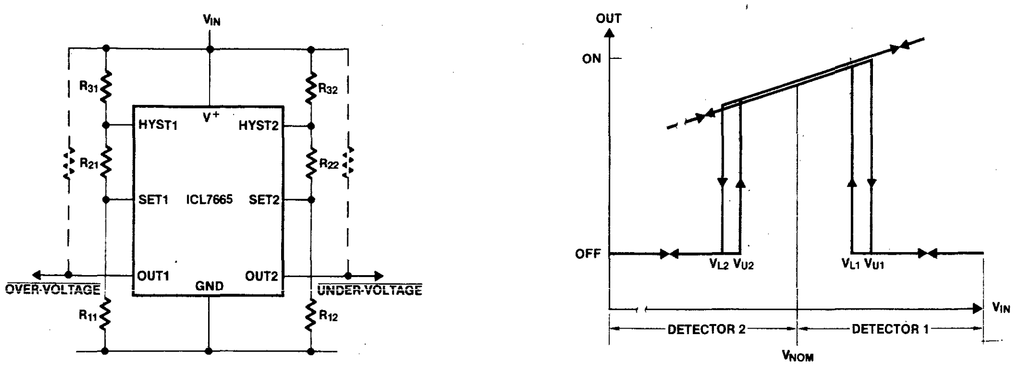
$$V_{TR2} = V_{SET2} \frac{(R_{12} + R_{22})}{R_{12}} = 1.3 \frac{(R_{12} + R_{22})}{R_{12}} \text{ for detector 2.}$$

Either detector may be used alone, as well as both together, in any of the circuits shown here.

When V_{IN} is very close to one of the trip voltages, normal variations and noise may cause it to wander back and forth across this level, leading to erratic output ON and OFF conditions. The addition of hysteresis, making the trip points slightly different for rising and falling inputs, will avoid this condition.

Figure 2(a) shows how to set up such hysteresis, while Figure 2(b) shows how the hysteresis around each trip point produces switching action at different points depending on whether V_{IN} is rising or falling (the arrows indicate direction of change). The HYST outputs are basically switches which short out R_{31} or R_{32} when V_{IN} is above the respective trip point. Thus if the input voltage rises from a low value, the trip point will be controlled by R_{1n}, R_{2n} and R_{3n}, until the trip point is reached. As this value is passed, the detector changes state, R_{3n} is shorted out, and the trip point becomes controlled by only R_{1n} and R_{2n}, a lower value. The input will then have to fall to this new point to restore the initial comparator state, but as soon as this occurs, the trip point will be raised again.

An alternative circuit for obtaining hysteresis is shown in Figure 3. In this configuration, the HYST pins put the extra resistor in parallel with the upper setting resistor. The values of the resistors differ, but the action is essentially the same. The governing equations are given in Table 1. These ignore the effects of the resistance of the HYST outputs, but these can normally be neglected if the resistor values are above about 100kΩ.



(a) Circuit Configuration (b) Transfer Characteristics

Figure 2. Threshold Detector with Hysteresis

INTERSIL

ICL8021—ICL8023 Low Power Operational Amplifiers

FEATURES

- ΔVos = 3 mV max (adjustable to zero).
- ±1V to ±18V Power Supply Operation.
- Power Consumption – 20 μW @ ± 1V.
- Input Bias Current – 30 nA max.
- Internal Compensation.
- Pin-For-Pin Compatible With 741.
- Short Circuit Protected.

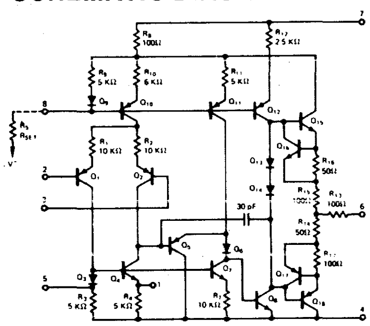
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Differential Input Voltage (Note 1)	±15V
Common Mode Input Voltage (Note 1)	±15V
Output Short Circuit Duration	Indefinite
Power Dissipation (Note 2)	300 mW
Operating Temperature Range	
8021M	−55°C to +125°C
8021C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

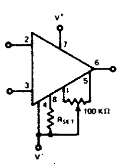
NOTE 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

NOTE 2: Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +95°C.

SCHEMATIC DIAGRAM



VOLTAGE OFFSET NULL CIRCUIT



ORDERING INFORMATION

ICL8021 C TY

- Basic Part Number: 8021—Single, 8022—Dual, 8023—Triple
- Package:
  - TY – TO-99 Metal Can, PA—8 pin Minidip — 8021 only
  - JD— 14 pin CERDIP, PD— 14 pin Plastic DIP — 8022 only
  - JE— 16 pin CERDIP, PE— 16 pin Plastic DIP — 8023 only
- Temperature:
  - C— Commercial — 0°C to 70°C
  - M— Military −55°C to +125°C

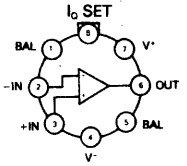
GENERAL DESCRIPTION

The Intersil 8021 integrated circuit is a low power operational amplifier specifically designed for applications requiring very low standby power consumption over a wide range of supply voltages. The electrical characteristics of the 8021 can be tailored to a particular application by adjusting an external resistor, R_{SET}, which controls the quiescent current. This is advantageous because I_Q can be made independent of the supply voltages: it can be set to an extremely low value where power is critical, or to a larger value for high slew rate or wideband applications.

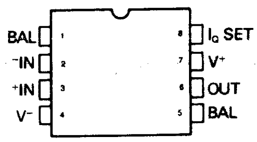
Other features of the 8021 include low input current that remains constant with temperature, low noise, high input impedance, internal compensation and pin-for-pin compatibility with the 741.

The Intersil 8022 (8023) consists of two (three) low power operational amplifiers in a single 14-pin DIP. Each amplifier is identical to an 8021 low power op amp, and has separate connections for adjusting its electrical characteristics by means of an external resistor, R_{SET}, which controls the quiescent current of that amplifier.

PIN CONFIGURATIONS

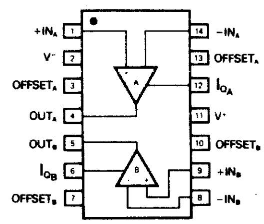


(outline dwg TY)

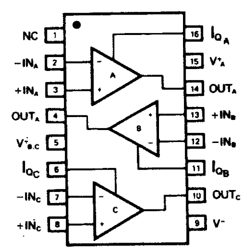


(outline dwg PA)

NOTE: Pin 4 connected to case.



(outline dwg JD, PD)



(outline dwg JE, PE)

LINEAR

Intersil

ELECTRICAL CHARACTERISTICS (V_S = ±6V, I_Q = 30 μA, unless otherwise specified.)

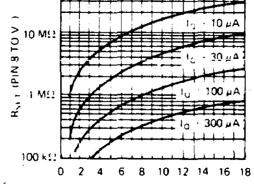
CHARACTERISTICS	CONDITIONS	8021M MIN	8021M TYP	8021M MAX	8021C MIN	8021C TYP	8021C MAX	UNITS
The following specifications apply for T_A = 25°C:								
Input Offset Voltage	$R_S \leq 100\ k\Omega$		2	3		2	6	mV
Input Offset Current			.5	7.5		.7	10	nA
Input Bias Current			5	20		7	30	nA
Input Resistance		3	10		3	10		MΩ
Input Voltage Range	V_S = ±15V	±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	80		70	80		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$		30	150		30	150	μV/V
Output Resistance	Open Loop		2			2		kΩ
Output Voltage Swing	$R_L \geq 20\ k\Omega$, V_S = ±15V	±12	±14		±12	±14		V
	$R_L \geq 10\ k\Omega$, V_S = ±15V	±11	±13		±11	±13		V
Output Short-Circuit Current			±13			±13		mA
Power Consumption	V_{OUT} = 0		360	480		360	600	μW
Slew Rate (Unity Gain)			0.16			0.16		V/μs
Unity Gain Bandwidth	R_L = 20 kΩ, V_{IN} = 20 mV		270			270		kHz
Transient Response (Unity Gain)	R_L = 20 kΩ, V_{IN} = 20 mV							
Risetime			1.3			1.3		μs
Overshoot			10			10		%
The following specifications apply for 0 C ≤ T_A < +70 C (8021C) -55 C < +125 C (8021M)								
Input Offset Voltage	$R_S \leq 10\ k\Omega$		2.0	4.0		2.0	7.5	mV
Input Offset Current			1.0	11		1.5	15	nA
Input Bias Current			10	32		15	50	nA
Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 10\ k\Omega$		5			5		μV/°C
Average Temperature Coefficient of Input Offset Current			1.7			0.8		pA/°C
Large Signal Voltage Gain	R_L = 10 kΩ	50	200		50	200		V/mV
Output Voltage Swing	$R_L \geq 10\ k\Omega$	±10	±13		±10	±13		V

QUIESCENT CURRENT ADJUSTMENT

QUIESCENT CURRENT SETTING RESISTOR (PIN 8 TO V⁻)

V_S \ I_Q	10 μA	30 μA	100 μA	300 μA
±1.5	1.5 MΩ	470 kΩ	150 kΩ	
± 3	3.3 MΩ	1.1 MΩ	330 kΩ	100 kΩ
± 6	7.5 MΩ	2.7 MΩ	750 kΩ	220 kΩ
± 9	13 MΩ	4 MΩ	1.3 MΩ	350 kΩ
± 12	18 MΩ	5.6 MΩ	1.5 MΩ	510 kΩ
± 15	22 MΩ	7.5 MΩ	2.2 MΩ	620 kΩ

QUIESCENT CURRENT SETTING RESISTOR (PIN 8 TO V⁻)



LINEAR

Intersil

ICL8038 Precision Waveform Generator/Voltage Controlled Oscillator

FEATURES

- Low frequency drift with temperature - 50ppm/°C
- Simultaneous sine, square, and triangle wave outputs
- Low distortion - 1% (sine wave output)
- High linearity - 0.1% (triangle wave output)
- Wide operating frequency range - 0.001Hz to 0.3MHz
- Variable duty cycle - 2% to 98%
- High level outputs - TTL to 28V
- Easy to use - just a handful of external components required

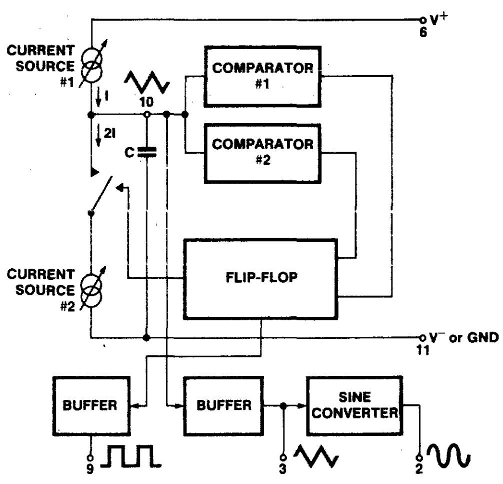
GENERAL DESCRIPTION

The ICL8038 Waveform Generator is a monolithic integrated circuit capable of producing high accuracy sine, square, triangular, sawtooth and pulse waveforms with a minimum of external components. The frequency (or repetition rate) can be selected externally from .001Hz to more than 300kHz using either resistors or capacitors, and frequency modulation and sweeping can be accomplished with an external voltage. The ICL8038 is fabricated with advanced monolithic technology, using Schottky-barrier diodes and thin film resistors, and the output is stable over a wide range of temperature and supply variations. These devices may be interfaced with phase locked loop circuitry to reduce temperature drift to less than 50ppm/°C.

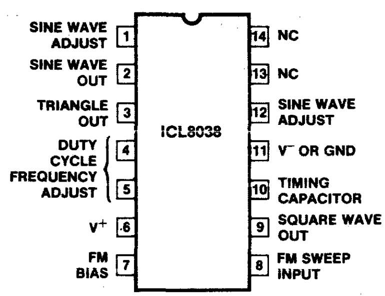
LINEAR

Intersil

BLOCK DIAGRAM



PIN CONFIGURATION (outline dwg JD)



ORDERING INFORMATION

TYPE	TEMPERATURE RANGE	STABILITY	PACKAGE	ORDER PART NUMBER
8038 CC	0°C to +70°C	250ppm/°C typ	CERDIP	ICL8038 CC JD
8038 BC	0°C to +70°C	150ppm/°C max	CERDIP	ICL8038 BC JD
8038 AC	0°C to +70°C	80ppm/°C max	CERDIP	ICL8038 AC JD
8038 BM	-55°C to +125°C	150ppm/°C max	CERDIP	ICL8038 BM JD
8038 AM	-55°C to +125°C	80ppm/°C max	CERDIP	ICL8038 AM JD

MAXIMUM RATINGS

Supply Voltage .... ±18V or 36V Total
Power Dissipation[1] 750mW
Input Voltage (any pin) .... Not To Exceed Supply Voltages
Input Current (Pins 4 and 5) 25mA
Output Sink Current (Pins 3 and 9) 25mA
Storage Temperature Range .... −65°C to +125°C
Operating Temperature Range:
  8038AM, 8038BM .... −55°C to +125°C
  8038AC, 8038BC, 8038CC .... 0°C to +70°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: Derate ceramic package at 12.5mW/°C for ambient temperatures above 100°C.

ELECTRICAL CHARACTERISTICS

(V_{SUPP} = ±10V or +20V, T_A = 25°C, R_L = 10kΩ, Test Circuit Unless Otherwise Specified)

SYMBOL	GENERAL CHARACTERISTICS	8038CC MIN	8038CC TYP	8038CC MAX	8038BC(BM) MIN	8038BC(BM) TYP	8038BC(BM) MAX	8038AC(AM) MIN	8038AC(AM) TYP	8038AC(AM) MAX	UNITS
V_{SUPP}	Supply Voltage Operating Range										
V^+	Single Supply	+10		+30	+10		30	+10		30	V
V^+, V^-	Dual Supplies	±5		±15	±5		±15	±5		±15	V
I_{SUPP}	Supply Current (V_{SUPP} = ±10V)(2)										
	8038AM, 8038BM					12	15		12	15	mA
	8038AC, 8038BC, 8038CC		12	20		12	20		12	20	mA
FREQUENCY CHARACTERISTICS (all waveforms)											
f_{max}	Maximum Frequency of Oscillation	100,000			100,000			100,000			Hz
f_{sweep}	Sweep Frequency of FM		10			10			10		kHz
	Sweep FM Range(3)		35:1			35:1			35:1		
	FM Linearity 10:1 Ratio		0.5			0.2			0.2		%
Δf/ΔT	Frequency Drift With Temperature(5) +25°C to +70°C (+125°C)		250				150			80	ppm/°C
	0°C (−40°C) to +25°C		250				200			120	ppm/°C
Δf/ΔV	Frequency Drift With Supply Voltage (Over Supply Voltage Range)		0.05			0.05			0.05		%/V_{SUPP}
	Recommended Programming Resistors (R_A and R_B)	1000		1M	1000		1M	1000		1M	Ω
OUTPUT CHARACTERISTICS											
I_{OLK}	**Square-Wave** Leakage Current (V_9 = 30V)			1			1			1	μA
V_{SAT}	Saturation Voltage (I_{SINK} = 2mA)		0.2	0.5		0.2	0.4		0.2	0.4	V
t_r	Rise Time (R_L = 4.7kΩ)		180			180			180		ns
t_f	Fall Time (R_L = 4.7kΩ)		40			40			40		ns
	Duty Cycle Adjust	2		98	2		98	2		98	%
	Triangle/Sawtooth/Ramp Amplitude (R_{TRI} = 100kΩ)	0.30	0.33		0.30	0.33		0.30	0.33		xV_{SUPP}
	Linearity		0.1			0.05			0.05		%
Z_{OUT}	Output Impedance (I_{OUT} = 5mA)		200			200			200		Ω
	Sine-Wave Amplitude (R_{SINE} = 100kΩ)	0.2	0.22		0.2	0.22		0.2	0.22		xV_{SUPP}
	THD (R_S = 1MΩ)(4)		2.0	5		1.5	3		1.0	1.5	%
	THD Adjusted (Use Fig. 8b)		1.5			1.0			0.8		%

NOTE 2: R_A and R_B currents not included.
NOTE 3: V_{SUPP} = 20V; R_A and R_B = 10kΩ, f ≅ 9kHz; Can be extended to 1000.1. See Figures 13 and 14.
NOTE 4: 82kΩ connected between pins 11 and 12, Triangle Duty Cycle set at 50%. (Use R_A and R_B.)
NOTE 5: Fig. 2, pins 7 and 8 connected, V_{SUPP} = ±10V. See Fig. 6c for T.C. vs V_{SUPP}.

APPLICATIONS

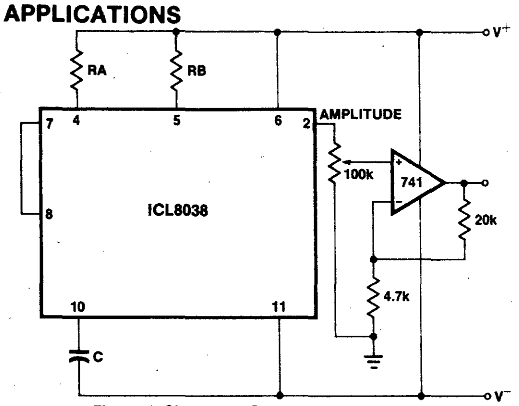


Figure 4: Sine Wave Output Buffer Amplifiers.

The sine wave output has a relatively high output impedance (1kΩ Typ). The circuit of Figure 4 provides buffering, gain and amplitude adjustment. A simple op amp follower could also be used.

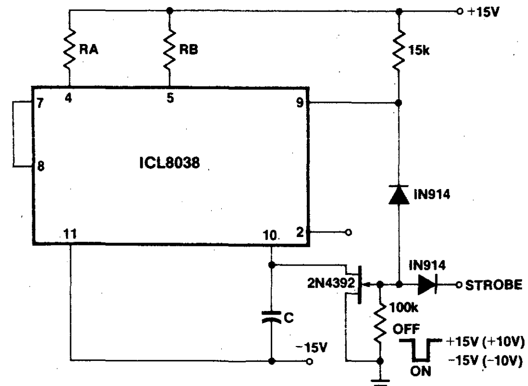


Figure 5: Strobe-Tone Burst Generator.

With a dual supply voltage the external capacitor on Pin 10 can be shorted to ground to halt the 8038 oscillation. Figure 5 shows a FET switch, diode ANDed with an input strobe signal to allow the output to always start on the same slope.

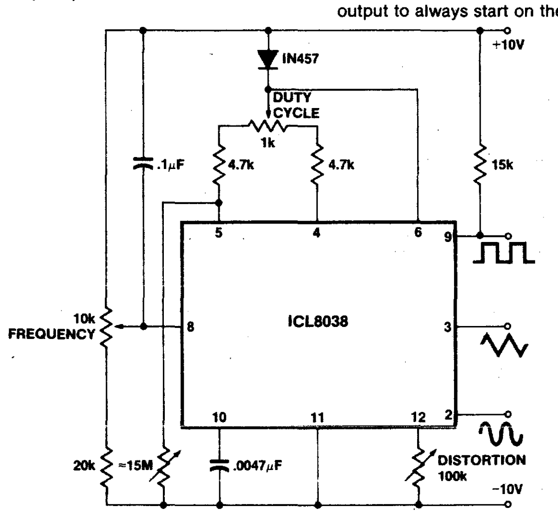


Figure 6: Variable Audio Oscillator, 20Hz to 20kHz.

To obtain a 1000:1 Sweep Range on the 8038 the voltage across external resistors R_A and R_B must decrease to nearly zero. This requires that the highest voltage on control Pin 8 exceed the voltage at the top of R_A and R_B by a few hundred millivolts.

The Circuit of Figure 6 achieves this by using a diode to lower the effective supply voltage on the 8038. The large resistor on pin 5 helps reduce duty cycle variations with sweep.

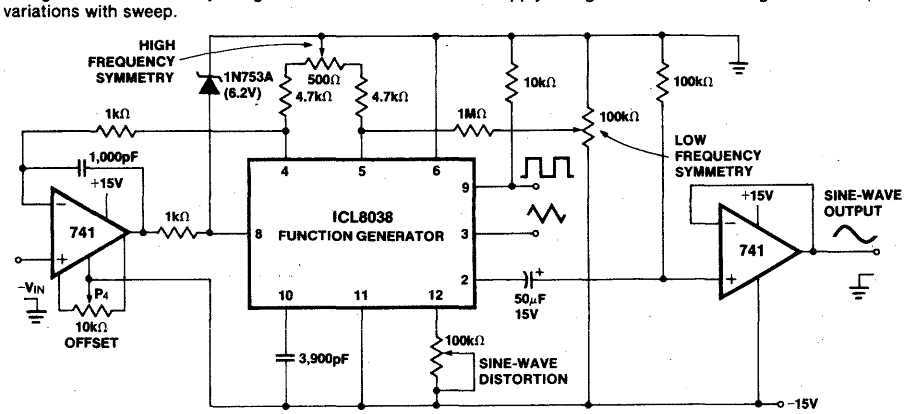


Figure 7: Linear Voltage Controlled Oscillator

The linearity of input sweep voltage versus output frequency can be significantly improved by using an op amp as shown in Figure 7.

LINEAR

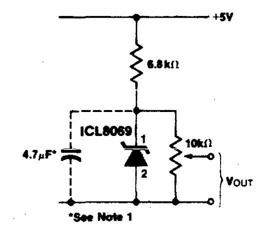
Intersil

ICL8069 Series
Low Voltage Reference

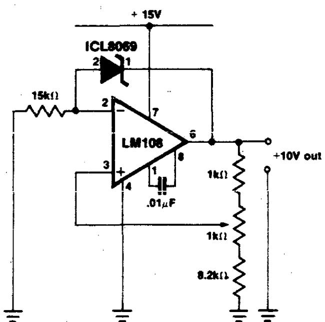
FEATURES
- **Temperature Coefficient guaranteed to 10 ppm/°C max.**
- **Low Bias Current . . . 50μA min**
- **Low Dynamic Impedance**
- **Low Reverse Voltage**
- **Low Cost**

GENERAL DESCRIPTION
The ICL8069 is a 1.2V temperature compensated voltage reference. It uses the band-gap principle to achieve excellent stability and low noise at reverse currents down to 50μA. Applications include analog-to-digital converters, digital-to-analog converters, threshold detectors, and voltage regulators. Its low power consumption makes it especially suitable for battery operated equipment.

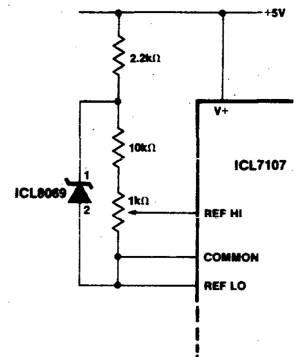
TYPICAL CONNECTION DIAGRAMS



(a) Simple Reference (1.2 volts or less)



(b) Buffered 10V Reference using a single supply.

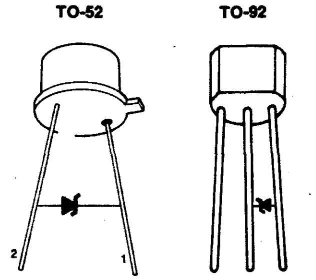


(c) Double regulated 100mV reference for ICL7107 one-chip DPM circuit.

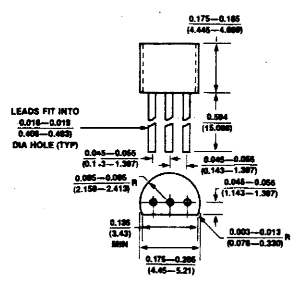
ORDERING INFORMATION

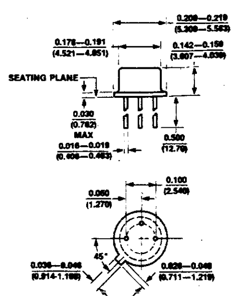
Max. Temp. Coeff. of V_{REF}	Temp. Range	Order P/N TO-92	Order P/N TO-52
0.001%/°C	0°C to +70°C		ICL8069ACSQ
0.0025%/°C	0°C to +70°C		ICL8069BCSQ
0.005%/°C	0°C to +70°C	ICL8069CCZR	ICL8069CCSQ
0.005%/°C	-55°C to +125°C	—	ICL8069CMSQ
0.01%/°C	0°C to +70°C	ICL8069DCZR	ICL8069DCSQ
0.01%/°C	-55°C to +125°C	—	ICL8069DMSQ

PIN CONFIGURATION

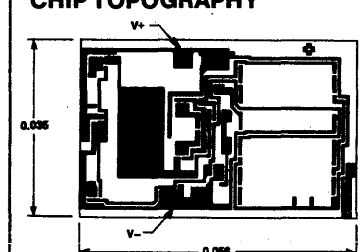


PACKAGE DIMENSIONS


TO-92


TO-52

CHIP TOPOGRAPHY



LINEAR

Intersil

ICL8211, ICL8212
Programmable Voltage Reference

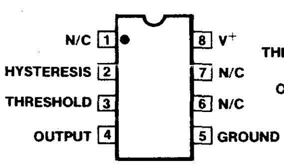
FEATURES
- High accuracy voltage sensing and generation: internal reference 1.15 volts typical
- Low sensitivity to supply voltage and temperature variations
- Wide supply voltage range: Typ. 1.8 to 30 volts
- Essentially constant supply current over full supply voltage range
- Easy to set hysteresis voltage range
- Defined output current limit - ICL8211
  High output current capability - ICL8212

GENERAL DESCRIPTION
The Intersil ICL8211/12 are micropower bipolar monolithic integrated circuits intended primarily for precise voltage detection and generation. These circuits consist of an accurate voltage reference, a comparator and a pair of output buffer/drivers.

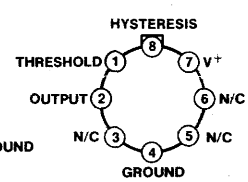
Specifically, the ICL8211 provides a 7mA current limited output sink when the voltage applied to the 'THRESHOLD' terminal is less than 1.15 volts (the internal reference). The ICL8212 requires a voltage in excess of 1.15 volts to switch its output on (no current limit). Both devices have a low current output (HYSTERESIS) which is switched on for input voltages in excess of 1.15V. The HYSTERESIS output may be used to provide positive and noise free output switching using a simple feedback network.

Applications include:
1. Low voltage sensor/indicator
2. High voltage sensor/indicator
3. Non volatile out-of-voltage range sensor/indicator
4. Programmable voltage reference or zener diode
5. Series or shunt power supply regulator
6. Fixed value constant current source

PIN CONFIGURATION



(outline dwg PA)

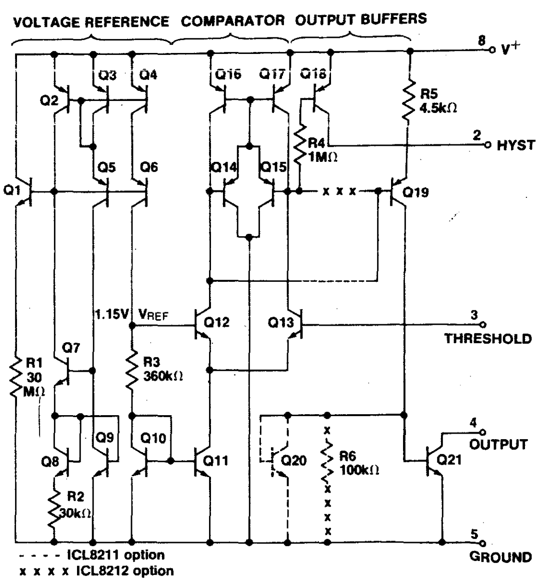


(outline dwg TY)

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL8211CPA	0 to +70°C	8 lead Mini DIP
ICL8211CTY	0 to +70°C	TO-99 Can
ICL8211MTY	-55° to +125°C	TO-99 Can
ICL8212CPA	0 to 70°C	8 lead Mini DIP
ICL8212CTY	0 to 70°C	TO-99 Can
ICL8212MTY	-55 to +125°C	TO-99 Can
ICL8211D	Dice only	
ICL8212D	Dice only	

SCHEMATIC DIAGRAM



ICL8211/ICL8212

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage .... −0.5 to +30 volts
Output Voltage .... −0.5 to +30 volts
Hysteresis Voltage .... +0.5 to −10 volts
Threshold Input Voltage .... +30 to −5 volts with respect to GROUND
and +0 to −30 volts with respect to V^+
Current into Any Terminal .... ±30mA
Power Dissipation (Note 1 & 2) 300mW
Operating Temperature Range ICL8211M/12M .... −55°C to +125°C
Operating Temperature Range ICL8211C/12C .... 0 to +70°C
Storage Temperature Range .... −65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: Rating applies for case temperatures to 125°C to ICL8211MTY/12MTY products. Derate linearly at −10mW/°C for ambient temperatures above 100°C.
NOTE 2: Derate linearly above 50°C by −10mW/°C for ICL8211C/12C products. The threshold input voltage may exceed +7 volts for short periods of time. However for continuous operation this voltage must be maintained at a value less than 7 volts.

TYPICAL OPERATING CHARACTERISTICS (V^+ = 5V, T_A = 25°C unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	ICL8211			ICL8212			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Supply Current	I^+	$2.0 < V^+ < 30$							
		$V_T = 1.3V$	10	22	40	50	110	250	μA
		$V_T = 0.9V$	50	140	250	10	20	40	μA
Threshold Trip Voltage	V_{TH}	$I_{OUT} = 4mA$ $V^+ = 5V$	0.98	1.15	1.19	1.00	1.15	1.19	V
		$V_{OUT} = 2V$ $V^+ = 2V$	0.98	1.145	1.19	1.00	1.145	1.19	V
		$V^+ = 30V$	1.00	1.165	1.20	1.05	1.165	1.20	V
Threshold Voltage Disparity Between Output & Hysteresis Output	V_{THP}	$I_{OUT} = 4$ mA $V_{OUT} = 2V$ $I_{HYST} = 7\mu A$ $V_{HYST} = 3V$		−8.0			−0.5		mV
Guaranteed Operating Supply Voltage Range	V_{SUPP}	+25°C	2.0		30	2.0		30	V
		0 to +70°C	2.2		30	2.2		30	V
		−55°C to +125°C	2.8		30	2.8		30	V
Typical Operating Supply Voltage Range	V_{SUPP}	+25°C	1.8		30	1.8		30	V
		+125°C	1.4		30	1.4		30	V
		−55°C	2.5		30	2.5		30	V
Threshold Voltage Temperature Coefficient	$\Delta V_{TH}/\Delta T$	$I_{OUT} = 4mA$ $V_{OUT} = 2V$		+200			+200		ppm/°C
Variation of Threshold Voltage with Supply Voltage	$\Delta V_{TH}/\Delta V^+$	$\Delta V^+ = 10\%$ at $V^+ = 5V$		1.0			1.0		mV
Threshold Input Current	I_{TH}	$V_{TH} = 1.15V$		100	250		100	250	nA
		$V_{TH} = 1.00V$		5			5		nA
Output Leakage Current	I_{OLK}	$V_{OUT} = 30V$ $V_{TH} = 1.0V$						10	μA
		$V_{OUT} = 30V$ $V_{TH} = 1.3V$			10				μA
		$V_{OUT} = 5V$ $V_{TH} = 1.0V$						1	μA
		$V_{OUT} = 5V$ $V_{TH} = 1.3V$			1				μA
Output Saturation Voltage	V_{SAT}	$I_{OUT} = 4mA$ $V_{TH} = 1.0V$		0.17	0.4				V
		$V_{TH} = 1.3V$					0.17	0.4	V
Max Available Output Current	I_{OH}	(Note 3 & 4) $V_{TH} = 1.0V$	4	7.0	12			mA	
		$V_{OUT} = 5V$ $V_{TH} = 1.3V$				15	35		mA
		$-55°C \le T_A \le 125°C$ $V_{TH} = 1.0V$			15	12			mA
Hysteresis Leakage Current	I_{LHYS}	$V^+ = 10V$ $V_{TH} = 1.0V$ $V_{HYST} = V^-$			0.1			0.1	μA
Hysteresis Sat Voltage	$V_{HYS\,(max)}$	$I_{HYST} = -7\mu A$ $V_{TH} = 1.3V$ measured with respect to V^+		−0.1	−0.2		−0.1	−0.2	V
Max Available Hysteresis Current	$I_{HYS\,(max)}$	$V_{TH} = 1.3V$	−15	−21		−15	−21		μA

NOTE 3: The maximum output current of the ICL8211 is limited by design to 15ma under any operating conditions. The output voltage may be sustained at any voltage up to +30 as long as the maximum power dissipation of the device is not exceeded.
NOTE 4: The maximum output current of the ICL8212 is not defined, and systems using the ICL8212 must therefore ensure that the output current does not exceed 30ma and that the maximum power dissipation of the device is not exceeded.

ICM7206 CMOS Touch Tone™ Encoder

FEATURES

- **Low cost system with minimum component count**
- **Fully integrated oscillator uses 3.58 MHz color TV crystal**
- **High current bipolar output driver**
- **Low output harmonic distortion**
- **Wide operating supply voltage range: 3 to 6 volts**
- **Uses inexpensive single contact per key calculator type keyboard (ICM7206/C/D)**
- **Extremely low power ≤ 5.5mW with a 5.5V supply**
- **Single and dual tone capabilities**
- **Multiple key lockout**
- **Disable output: provides output switch function whenever a key is pressed**
- **Custom options available**

GENERAL DESCRIPTION

The Intersil ICM7206/A/B/C/D are 2-of-8 sine wave tone encoders for use in telephone dialing systems. Each circuit contains a high frequency oscillator, two separate programmable dividers, a D/A converter, and a high level output driver.

The reference frequency is generated from a fully integrated oscillator requiring only a 3.58 MHz color TV crystal. This frequency is divided by 8 and is then gated into two divide by N counters (possible division ratios 1 through 128) which provide the correct division ratios for the upper and lower band of frequencies. The outputs from these two divide by N counters are further divided by 8 to provide the time sequencing for a 4 voltage level synthesis of each sinewave. Both sinewaves are added and buffered to a high current output driver, with provisions made for up to two external capacitors for low pass filtering, if desired. Typically, the total output harmonic distortion is 20% with no L.P. filtering and it may be reduced to typically less than 5% with filtering. The output drive level of the tone pairs will be approximately −3dBV into a 900 ohm termination. The skew between the high and low groups is typically 2.5 dB without low pass filtering.

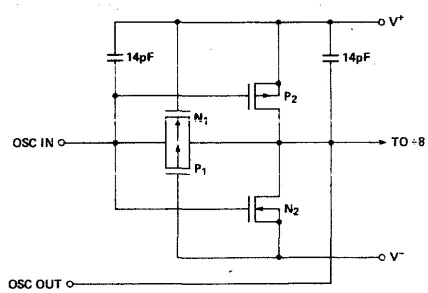
The 7206 uses either a 3 x 4 or 4 x 4 single contact keyboard; the oscillator will run whenever the power is applied, and the DISABLE output consists of a p-channel open drain FET whose source is connected to V^+.

The 7206A can also use a 3 x 4 or 4 x 4 keyboard, but requires a double contact type with the common line tied to V^+. The oscillator will be on whenever power is applied; the DISABLE output consists of a p-channel open drain FET; its' source is connected to V^+.

The 7206B requires a 4 x 4 double contact keyboard with the common line tied to V^-. The oscillator will be on only during the time that a ROW is enabled, and the DISABLE output consists of an n-channel open drain FET with its' source tied to V^-.

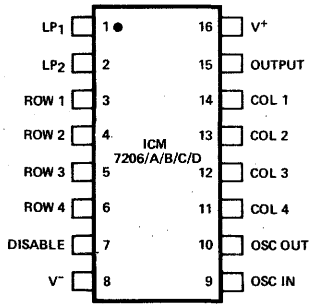
The 7206C uses either a 3 x 4 or 4 x 4 single contact keyboard; the oscillator will be on only during the time that a key is depressed. The DISABLE output consists of an n-channel open drain FET with its source tied to V^-.

The 7206D uses a single contact 3 x 4 or 4 x 4 keyboard. The oscillator will be on only during the time that a key is depressed. DISABLE output consists of a p-channel open drain FET with its source tied to V^+.



ICM7206 Oscillator

PIN CONFIGURATION (OUTLINE DRAWING PE)



Pin 1 is designated either by a dot or a notch.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7206 JPE	-40° C to +85° C	Plastic
ICM7206A JPE	-40° C to +85° C	Plastic
ICM7206B JPE	-40° C to +85° C	Plastic
ICM7206C JPE	-40° C to +85° C	Plastic
ICM7206D JPE	-40° C to +85° C	Plastic
ICM7206/D	-40° C to +85° C	DICE
ICM7206A/D	-40° C to +85° C	DICE
ICM7206B/D	-40° C to +85° C	DICE
ICM7206C/D	-40° C to +85° C	DICE
ICM7206D/D	-40° C to +85° C	DICE

LINEAR

Intersil

ICM7206 Family

INTERSIL

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Note 2) 6.0V
Supply Current V^- (terminal 8) 25mA
Supply Current V^+ (terminal 16) 40mA
Disable Output Volt. (term. 7) .. Not more pos. than V^+ nor more neg. than -6V with respect to V^+
Output Volt. (term. 15). Not more pos. than +5V with respect to V^+, nor more neg. than -1.0 with respect to V^-
Output Current (terminal 15) 25mA
Power Dissipation 300mW
Operating Temperature Range .... -40°C to +85°C
Storage Temperature Range .... -55°C to +125°C

NOTE 1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 2. The ICM7206 family has a zener diode connected between V^+ and V^- having a breakdown voltage between 6.2 and 7.0 volts. If the currents into terminals 8 and 16 are limited to 25 and 40mA maximum respectively, the supply voltage may be increased above 6 volts to zener voltage. With no such current limiting, the supply voltage must not exceed 6 volts.

TYPICAL OPERATING CHARACTERISTICS

TEST CONDITIONS: $V^+ = 5.5V$, Test Circuit, $T_A = 25°C$ unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	I^+	R_L disconnected		450	1000	μA
Guaranteed Operating Supply Voltage Range (Note 3)	V_{OP}	$-40°C \leq T_A \leq +85°C$	3.0		6.0	V
Peak to Peak Output Voltage	V_{OUT}	C_1, C_2 disconnected — Low Band	0.90	1.15	1.45	V
		$R_L = 1k\Omega$, no filtering — High Band	1.10	1.40	1.70	V
RMS Output Voltage		$R_L = 1k\Omega$, $f_{OUT} = 697Hz$ — C_2 Only		480		mV
		C_1 to C_2		480		mV
		No filtering		490		mV
		$R_L = 1k\Omega$, $f_{OUT} = 1633Hz$ — C_1		490		mV
		C_1 to C_2		580		mV
		No filtering		655		mV
Skew Between High and Low Band Output Voltages		$R_L = 1k\Omega$, C_1, C_2 disconnected		2.5	3.0	dB
Output Impedance	Z_O	$R_L = 1k\Omega$ — Operating		90	200	Ω
		Quiescent		25		KΩ
Total Output Harmonic Distortion	THD1	Either Hi or Low Bands, No Low Pass Filtering		20	25	%
Total Output Harmonic Distortion	THD2	$R_L = 1k\Omega$, $C_1 = .002\mu F$, $f_{OUT} = 697Hz$		2.3	10	%
		$C_2 = 0.02\mu F$, $f_{OUT} = 1633Hz$		1.0	10	%
Maximum Output Voltage Level	V_{OH}	$R_L = 1k\Omega$			4.6	V
Minimum Output Voltage Level	V_{OL}	$R_L = 1k\Omega$	0.5			V
Keyboard Input Pullup Resistors	R_{IN}	Terminals 3,4,5,6,11,12,13,14	35	100	150	KΩ
Keyboard Input Capacitance	C_{IN}	Terminals 3,4,5,6,11,12,13,14			5	pF
Guaranteed Oscillator Frequency Range (Note 4)	f_{OSC}	$3 \leq (V^+ - V^-) \leq 6V$	2.0		4.5	MHz
Guaranteed Oscillator Frequency Range		$4V \leq (V^+ - V^-) \leq 6V$	2.0		7	MHz
System Startup Time on Application of Power	t_{on}	ICM7206, ICM7206A		10		ms
System Startup Time on Application of Power and Key Depressed Simultaneously		ICM7206B, ICM7206C, ICM7206D			7	ms
DISABLE Output Saturation Resistance (ON STATE)	R_D	See Logic Table for Input Conditions, Current = 4mA		330	700	Ω
DISABLE Output Leakage (OFF STATE)	I_{OLK}	See Logic Table for Input Conditions			10	μA
Oscillator Load Capacitance	C_{OSC}	Measured between terminals 9 & 10, no supply voltage applied to circuit, $-40°C \leq T_A \leq 85°C$		7		pF
Guaranteed Output Frequency Tolerance	f_O	Any output frequency, Crystal tolerance ±60ppm, Crystal load capacitance CL = 30pF			±0.75	%
Oscillator Startup Time ICM7206B, C, D	t_{start}	$V^+ = 3V$ (Note 5)			7	ms

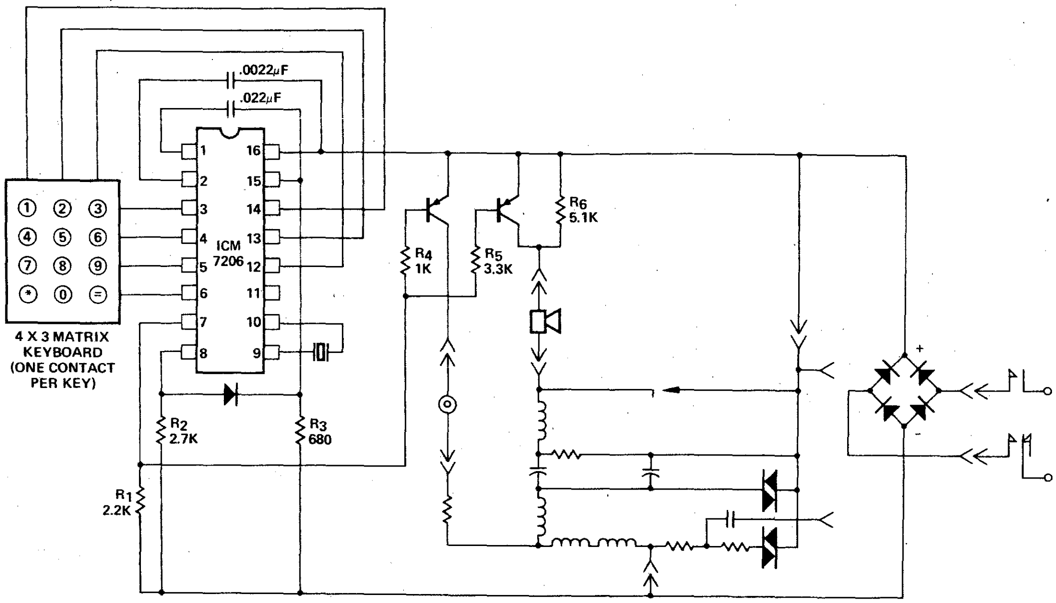
NOTE 3: Operation above 6 volts must employ supply current limiting. Refer to 'ABSOLUTE MAXIMUM RATINGS' and the Application Notes for further information.

NOTE 4: The ICM7206 family uses dynamic high frequency circuitry in the initial 2^3 divider resulting in low power dissipation and excellent performance over a restricted frequency range. Thus, for reliable operation with a 6 volt supply an oscillator frequency of not less than 2MHz must be used.

NOTE 5: After row input is enabled.

LINEAR

Intersil



NOTE: If dual contact keyboard is used, common should be left floating.

FIGURE 5: Telephone Handset Touch Tone Encoder

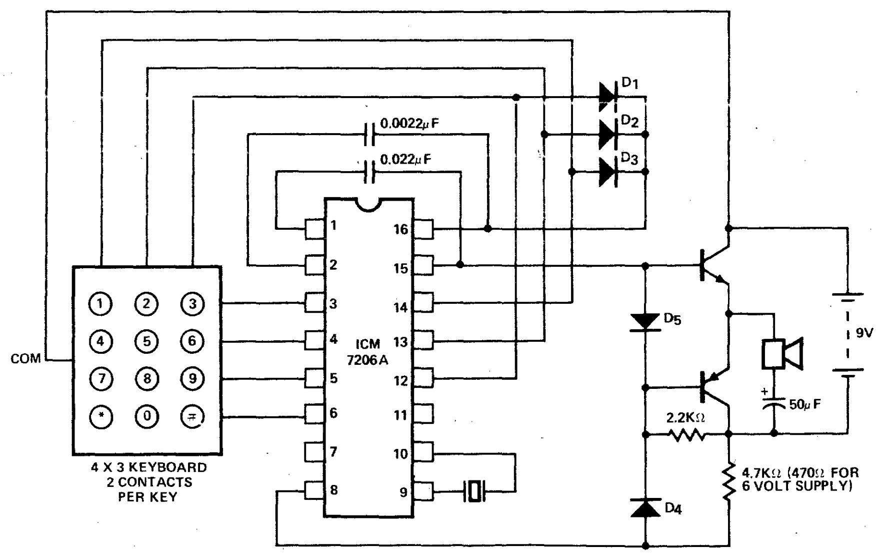


FIGURE 6: Portable Tone Generator

ICM7555/7556
CMOS
General Purpose Timers

FEATURES

- **Exact equivalent in most cases for SE/NE555/556 or the 355.**
- **Low Supply Current — 80μA Typ. (ICM7555) 160μA Typ. (ICM7556)**
- **Extremely low trigger, threshold and reset currents - 20pA Typical**
- **High speed operation - 500 kHz guaranteed**
- **Wide operation supply voltage range guaranteed 2 to 18 volts**
- **Normal Reset function - No crowbarring of supply during output transition.**
- **Can be used with higher impedance timing elements than regular 555/6 for longer RC time constants.**
- **Timing from microseconds through hours**
- **Operates in both astable and monostable modes**
- **Adjustable duty cycle**
- **High output source/sink driver can drive TTL/CMOS**
- **Typical temperature stability of 0.005% per °C at 25°C**
- **Outputs have very low offsets, HI and LO**

GENERAL DESCRIPTION

The ICM7555/6 are CMOS RC timers providing significantly improved performance over the standard SE/NE555/6 and 355 timers, while at the same time being direct replacements for those devices in most applications. Improved parameters include low supply current, wide operating supply voltage range, low THRESHOLD, $\overline{\text{TRIGGER}}$ and $\overline{\text{RESET}}$ currents, no crowbarring of the supply current during output transitions, higher frequency performance and no requirement to decouple CONTROL VOLTAGE for stable operation.

Specifically, the ICM7555/6 are stable controllers capable of producing accurate time delays or frequencies. The ICM7556 is a dual ICM7555, with the two timers operating independently of each other, sharing only V^+ and GND. In the one shot mode, the pulse width of each circuit is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled by two external resistors and one capacitor. Unlike the regular bipolar 555/6 devices, the CONTROL VOLTAGE terminal need not be decoupled with a capacitor. The circuits are triggered and reset on falling (negative) waveforms, and the output inverter can source or sink currents large enough to drive TTL loads, or provide minimal offsets to drive CMOS loads.

APPLICATIONS

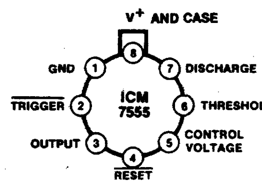
- Precision Timing
- Pulse Generation
- Sequential Timing
- Time Delay Generation
- Pulse Width Modulation
- Pulse Position Modulation
- Missing Pulse Detector

ORDERING INFORMATION

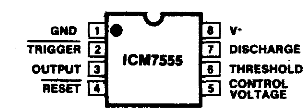
ORDER PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7555IPA	−20 to +85°C	8 Lead MiniDip
ICM7555ITV	−20 to +85°C	TO-99 Can
ICM7555MTV	−55 to +125°C*	TO-99 Can
ICM7556IPD	−20 to +85°C	14 Lead Plastic DIP
ICM7556MJD	−55 to +125°C*	14 Lead CERDIP
ICM7555/D		DICE
ICM7556/D		DICE

*Add /883B to order number if 883B processing is desired.

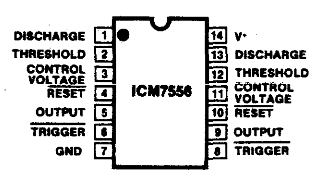
PIN CONFIGURATIONS (Top View)



(OUTLINE DRAWING TV)



(OUTLINE DRAWING PA)



(OUTLINE DRAWING JD, PD)

LINEAR

Intersil

APPLICATION NOTES

GENERAL

The ICM7555/6 devices are, in most instances, direct replacements for the NE/SE 555/6 devices. However, it is possible to effect economies in the external component count using the ICM7555/6. Because the bipolar 555/6 devices produce large crowbar currents in the output driver, it is necessary to decouple the power supply lines with a good capacitor close to the device. The 7555/6 devices produce no such transients. See Figure 2.

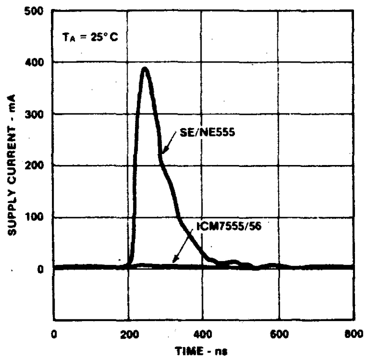


Figure 2. Supply Current Transient Compared with a Standard Bipolar 555 During an Output Transition

The ICM7555/6 produces supply current spikes of only 2-3 mA instead of 300-400 mA and supply decoupling is normally not necessary. Secondly, in most instances, the CONTROL VOLTAGE decoupling capacitors are not required since the input impedance of the CMOS comparators on chip are very high. Thus, for many applications 2 capacitors can be saved using an ICM7555, and 3 capacitors with an ICM7556.

POWER SUPPLY CONSIDERATIONS

Although the supply current consumed by the ICM7555/6 devices is very low, the total system supply can be high unless the timing components are high impedance. Therefore, use high values for R and low values for C in Figures 3 and 4.

OUTPUT DRIVE CAPABILITY

The output driver consists of a CMOS inverter capable of driving most logic families including CMOS and TTL. As such, if driving CMOS, the output swing at all supply voltages will equal the supply voltage. At a supply voltage of 4.5 volts or more the ICM7555/6 will drive at least 2 standard TTL loads.

ASTABLE OPERATION

The circuit can be connected to trigger itself and free run as a multivibrator, see Figure 3. The output swings from rail to rail, and is a true 50% duty cycle square wave. (Trip points and output swings are symmetrical). Less than a 1% frequency variation is observed, over a voltage range of +5 to +15V.

$$f = \frac{1}{1.4\,RC}$$

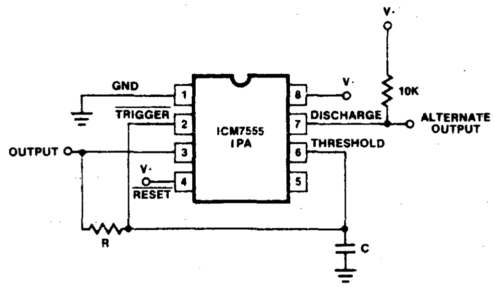


Figure 3: Astable Operation

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot. Initially the external capacitor (C) is held discharged by a transistor inside the timer. Upon application of a negative $\overline{\text{TRIGGER}}$ pulse to pin 2, the internal flip flop is set which releases the short circuit across the external capacitor and drives the OUTPUT high. The voltage across the capacitor now increases exponentially with a time constant $t = R_AC$. When the voltage across the capacitor equals 2/3 V^+, the comparator resets the flip flop, which in turn discharges the capacitor rapidly and also drives the OUTPUT to its low state. $\overline{\text{TRIGGER}}$ must return to a high state before the OUTPUT can return to a low state.

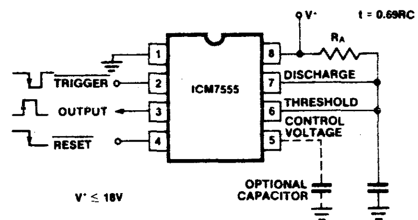


Figure 4: Monostable Operation

CONTROL VOLTAGE

The CONTROL VOLTAGE terminal permits the two trip voltages for the THRESHOLD and $\overline{\text{TRIGGER}}$ internal comparators to be controlled. This provides the possibility of oscillation frequency modulation in the astable mode or even inhibition of oscillation, depending on the applied voltage. In the monostable mode, delay times can be changed by varying the applied voltage to the CONTROL VOLTAGE pin.

$\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ terminal is designed to have essentially the same trip voltage as the standard bipolar 555/6, i.e. 0.6 to 0.7 volts. At all supply voltages it represents an extremely high input impedance. The mode of operation of the $\overline{\text{RESET}}$ function is, however, much improved over the standard bipolar 555/6 in that it controls only the internal flip flop, which in turn controls simultaneously the state of the OUTPUT and DISCHARGE pins. This avoids the multiple threshold problems sometimes encountered with slow falling edges in the bipolar devices.

Note: See other MPS parts in Interface and Military Sections.

Precision Voltage References

- ☐ Second source to PMI
- ☐ Low temperature coefficient
- ☐ Guaranteed long term-stability
- ☐ Low noise

Model	Packages	Output Voltage	Regulating Current	Temp Coefficient (max, full temp)	Reverse Dynamic Impedance	Noise	Replaces
MP5010	All	1.22V	50 μA – 500 μA	50 ppm/C°	2 ohm	5 μV	ICL8069 LM113 ZN423
MP5532/REF01	All	+10V	1.4 mA – 10 mA	8.5 ppm/C°	–	20 μV P-P	REF01
MP5531/REF02	All	+5V	1.4 mA – 10 mA	8.5 ppm/C°	–	20 μV P-P	REF02
MPREF05	All	+5V	1.4 mA – 10 mA	8.5 ppm/C°	–	20 μV P-P	REF05
MPREF10	All	+10V	1.4 mA – 10 mA	8.5 ppm/C°	–	20 μV P-P	REF10

Precision Operational Amplifiers

- ☐ Second source to PMI
- ☐ Lowest noise in the industry
- ☐ Improved long term-stability
- ☐ High slew rate DAC follower

Model	Type	V_{OS} (Max)	I_B (Max)	Noise (nV/$\sqrt{Hz}$ at 10 Hz)	Gain (Min)	CMRR (Min)	Slew Rate (typ)	Replaces
MP4136	Quad (741 Type)	6 mV	1.5 μA		25 V/mV	70 dB	1.5 V/μsec	PM4136
MP5501/OP01	DAC Follower, Hi-speed	1 mV	50 nA		30 V/mV	85 dB	18 V/μsec	OP01
MP5502/OP02	Low Noise, Gen. Purpose	1.0 mV	60 nA	25 (typ)	50 V/mV	80 dB	.25 V/μsec	OP02
MP5503/OP03	Dual, Matched	1.5 mV	60 nA	25 (typ)	50 V/mV	80 dB	.5 V/μsec	OP03
MP5504/OP04	Dual, Matched	1.5 mV	60 nA	25 (typ)	50 V/mV	80 dB	.5 V/μsec	OP04
MP5505/OP05	Low Noise, Instrumentation	.24 mV	±4 nA	18 (max)	200 V/mV	110 dB	.1 V/μsec	OP05
MP5507/OP07	Ultra Low Noise, Low V_{OS} Instr.	60 μV	4 nA	18 (max)	200 V/mV	106 dB	.1 V/μsec	OP07
MP5508/OP08	Low Input Current	.35 μV	3 nA	22 (typ)	40 V/mV	100 dB	.12 V/μsec	OP08
MP5509/OP09	Quad Matched	1 mV	375 nA	18	50 V/mV	100 dB	1.0 V/μsec	OP09
MP5510/OP10	Dual 5505/OP05	.7 mV	±6 nA	18 (max)	150 V/mV	106 dB	.2 V/μsec	OP10
MP5511/OP11	Quad Matched	1 mV	375 nA	18	50 V/mV	100 dB	1.0 V/μsec	OP11
MP5512/OP12	Low Input Current	.26 mV	2.6 nA	22 (typ)	25 V/mV	100 dB	.12 V/μsec	OP12
MP5514/OP14	Dual Matched High Performance	1.5 mV	60 nA	25	50 V/mV	80 dB	.5 V/μsec	OP14
MP5527/OP27	Ultra Low Noise	60 μV	50 nA	5.5 (max)	600 V/mV	108 dB	2.8 V/μsec	OP27
MP5537/OP37	Ultra Low Noise, High Speed	60 μV	50 nA	5.5 (max)	600 V/mV	108 dB	17 V/μsec	OP37
MP207/OP207	Dual, Matched OP07	230 μV	5.6 nA	18.0 (max)	150 V/mV	130 dB	0.2 V/μsec	OP207
MP227/OP227	Ultra Low Noise, Low V_{OS} Instr.	180 μV	±60 nA	6.0 (max)	600 V/mV	108 dB	2.8 V/μsec	OP227
MPLM108/208/308	Super Beta	1.0 mV	3 nA		40 V/mV	96 dB		LM108/208/308
MPOP2108/2208/2308	Low Input Current	1.0 mV	3 nA		40 V/mV	96 dB		OP2108/2208/2308

Note: All specifications: –55°C to +125°C

MICRO POWER SYSTEMS
3100 Alfred Street
Santa Clara, CA 95050
(408) 727-5350

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HIGH SLEW RATE, WIDE BANDWIDTH, SINGLE SUPPLY QUAD OPERATIONAL AMPLIFIER

A standard low-cost Bipolar technology with innovative design concepts is employed for the MC34074 series of monolithic quad operational amplifiers. These devices offer 4.5 MHz of gain bandwidth product, 13 V/μs slew rate, and fast settling time without the use of JFET device technology. In addition, low input offset voltage can economically be achieved. Although these devices can be operated from split supplies, they are particularly suited for single supply operation, since the common mode input voltage range includes ground potential (V_{EE}). The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, also provides high capacitive drive capability, excellent phase and gain margins, low open-loop high frequency output impedance and symmetrical source/sink ac frequency response.

The MC34074/33074/35074 series of devices are available in standard or prime performance (A Suffix) grades and specified over commercial, industrial/vehicular or military temperature ranges.

Features

- Wide Bandwidth: 4.5 MHz
- High Slew Rate: 13 V/μs
- Fast Settling Time: 1.1 μs to 0.10%
- Wide Single Supply Operating Range: 3.0 to 44 Volts
- Wide Input Common Mode Range Including Ground (V_{EE})
- Low Input Offset Voltage: 2.0 mV Maximum (A Suffix)
- Large Output Voltage Swing: −14.7 V to +14.0 V for $V_S = \pm 15$ V
- Large Capacitance Drive Capability: 0 to 10,000 pF
- Low T.H.D. Distortion: 0.02%
- Excellent Phase Margins: 60°

GENERAL OP-AMP SELECTOR GUIDE

General Purpose Op-Amps

Single		Dual	Quad
Compensated	LF351 LF355 LF356 LF357 MC1741 MC34001 TL081	LF353 LM358 MC1458 MC1747 MC3458 MC4558 MC34002 TL082	LF347 LM324 MC3403 MC4741 MC34004 TL084
Uncompensated	LM301A MC1709 MC1748	MC1437	

JFET (BIFET) INPUT — High Impedance		
Single	Dual	Quad
LF351 LF355 LF356 LF357 MC34001 TL071 TL081	LF353 MC34002 TL072 TL082	LF347 MC34004 TL074 TL084

High Slew Rate

Slew Rate (V/μs)			
5.0	8.0 to 20		50
LF355	LF347 LF351 LF353 LF356 MC1458S MC1741S MC34074	MC34001 MC34002 MC34004 OP-37 TL071 TL072 TL074 TL081 TL082 TL084	LF357

Programmable

Adjustable bias current varies noise bandwidth, power consumption, etc.

Single
MC1776 MC3476

Low Noise

Single	Dual	Quad
MC1741N OP-27/OP-37 TL071	MC1458N TL072	TL074

Wide Bandwidth

Bandwidth (MHz)				
3.0	4.0	5.0	20	100
MC4558S	MC34001 MC34002 MC34004	MC3401 LF356 MC34074	LF357	NE592 MC1733

Low Offset Voltage

V_{IO} Max (μV)			
≤ 200	500	2000	
OP-27/OP-37	LM11C LM308A	MC34001A MC34002A MC34074A	MC1709A LM301A LM308

Low Drift Over Temperature (TCV_{IO})

TCV_{IO} ≤ 5.0 μV/°C Max*	
LM11	LM308A OP-27/OP-37

*Input offset voltage temperature coefficient

Single-Supply

Dual	Quad
LM358 LM2904 MC3458 MC3405	LM324 LM2900 LM2902 LM3900 MC3301 MC3401 MC3403 MC34074

MOTOROLA

Voltage Regulators

Fixed Output Voltage Regulators

- Low-cost monolithic circuits for positive and/or negative regulation at currents from 100 mA to 3.0 A
- Ideal for on-card regulation of subsystems
- Internal current limiting thermal shutdown and safe-area compensation

Fixed/Voltage, 3-Terminal Regulators for Positive or Negative Polarity Power Supplies

V_{out} Volts	Tol.† Volts	I_O mA Max	Device Positive Output	Device Negative Output
2	±0.1	1500	—	MC7902C
3	±0.15	100	—	MC79L03AC
	±0.3			MC79L03C
5	±0.5	100	MC78L05C	MC79L05C
	±0.25		MC78L05AC	MC79L05AC
		500	MC78M05C	MC79M05C
	±0.4	1500	LM109	—
			LM209	—
	±0.25		LM309	—
	±0.35		MC7805*	—
	±0.25		MC7805B#	—
			MC7805C	MC7905C
	±0.2		MC7805A*	—
			MC7805AC	MC7905AC
	±0.25		LM140-5*	—
	±0.2		LM140A-5*	—
	±0.25		LM340-5	—
	±0.2		LM340A-5	—
	±0.1		TL780-05C	—
	±0.25	3000	MC78T05*	—
			MC78T05C	—
	±0.2		MC78T05A*	—
			MC78T05AC	—
	±0.4		LM123*	—
			LM223	—
	±0.25		LM323	—
	±0.2		LM123A	—
			LM223A	—
			LM323A	—
5.2	±0.26	1500	—	MC7905.2C
6	±0.3	500	MC78M06C	
	±0.35	1500	MC7806*	—
	±0.3		MC7806B#	—
			MC7806C	MC7906C
	±0.24		MC7806A*	—
			MC7806AC	—
	±0.3		LM140-6*	—
			LM340-6	—
		3000	MC78T06*	—
			MC78T06C	—

(continued)

V_{out} Volts	Tol.† Volts	I_O mA Max	Device Positive Output	Device Negative Output
8	±0.8	100	MC78L08C	—
			MC78L08AC	—
	±0.4	500	MC78M08C	—
		1500	MC7808*	—
			MC7808B#	—
			MC7808C	MC7908C
	±0.3		MC7808A*	—
			MC7808AC	—
	±0.4		LM140-8*	—
			LM340-8	—
		3000	MC78T08*	—
			MC78T08C	—
12	±1.2	100	MC78L12C	MC79L12C
	±0.6		MC78L12AC	MC79L12AC
		500	MC78M12C	MC79M12C
		1500	MC7812*	—
			MC7812B#	—
			MC7812C	MC7912C
	±0.5		MC7812A*	—
			MC7812AC	—
	±0.6		LM140-12*	—
	±0.5		LM140A-12*	—
	±0.6		LM340-12	—
	±0.5		LM340A-12	—
	±0.24		TL780-12C	—
	±0.6	3000	MC78T12*	—
			MC78T12C	—
	±0.5		MC78T12A*	—
			MC78T12AC	—
15	±1.5	100	MC78L15C	MC78L15C
	±0.75		MC78L15AC	MC78L15A
		500	MC78M15C	MC79M15C
		1500	MC7815*	—
			MC7815B#	—
			MC7815C	MC7915C
	±0.6		MC7815A*	—
			MC7815AC	—
	±0.75		LM140-15*	—
	±0.6		LM140A-15*	—
	±0.75		LM340-15	—
	±0.6		LM340A-15	
	±0.3		TL780-15C	—
	±0.75	3000	MC78T15*	—
			MC78T15C	—
	±0.6		MC78T15A*	—
			MC78T15AC	—

#T_J = −40 to +125°C
*T_J = −55 to +150°C
†Output Voltage Tolerance for Worst Case

Fixed Output Voltage Regulators (continued)

Vout Volts	Tol.† Volts	IO mA Max	Device Positive Output	Device Negative Output
18	±1.8	100	MC78L18C	MC79L18C
	±0.9		MC78L18AC	MC79L18AC
		500	MC78M18C	—
		1500	MC7818*	—
			MC7818B#	—
			MC7818C	MC7918C
	±0.7		MC7818A*	—
			MC7818AC	—
	±0.9		LM140-18*	—
			LM340-18	—
		3000	MC78T18*	—
			MC78T18C	—
20	±1.0	500	MC78M20C	—
24	±2.4	100	MC78L24C	MC79L24C
	±1.2		MC78L24AC	MC79L24AC
		500	MC78M24C	
		1500	MC7824*	—
			MC7824B#	—
			MC7824C	MC7924C
	±1.0		MC7824A*	—
			MC7824AC	—
	±1.2		LM140-24*	—
			LM340-24	—
		3000	MC78T24*	
			MC78T24C	

#T_J = −40 to +125°C †Output Voltage Tolerance for Worst Case
*T_J = −55 to +150°C

Positive Output Regulators (continued)

IO mA Max	Device	Suffix	Vout Volts Min	Vout Volts Max	Vin Volts Min	Vin Volts Max	Vin — Vout Differential Volts Min
500	LM317M	T	1.2	37	5.0	40	3.0
	LM317M	R					
	LM217M#						
	LM117M*						
600	MC1469	R	2.5	32	9.0	35	3.0
	MC1569			37	8.5	40	2.7
1500	LM317	T	1.2	37	5.0	40	3.0
	LM317	H, K					
	LM217#						
	LM117*						
3000	LM350	T	1.2	33	5.0	36	3.0
	LM350	K					
	LM250#						
	LM150*						

#T_J = −25 to +150°C
*T_J = −55 to +150°C

Adjustable Output Voltage Regulators

Positive Output Regulators

IO mA Max	Device	Suffix	Vout Volts Min	Vout Volts Max	Vin Volts Min	Vin Volts Max	Vin — Vout Differential Volts Min
100	LM317L	H,Z	1.2	37	5.0	40	3.0
	LM217L#						
	LM117L*						
150	MC1723	CP	2.0	37	9.5	40	3.0
		CG					
		G					
		CL					
		L					
		CD					
250	MC1469	G	2.5	32	9.0	35	3.0
	MC1569			37	8.5	40	2.7

#T_J = −40 to +125°C
*T_J = −55 to +150°C
†Output Voltage Tolerance for Worst Case

Negative Output Regulators

IO mA Max	Device	Suffix	Vout Volts Min	Vout Volts Max	Vin Volts Min	Vin Volts Max	Vin — Vout Differential Volts Min
250	MC1463	G	−3.8	−32	9.0	35	3.0
	MC1563		−3.6	−33	8.5	40	2.7
500	LM337M	T	−1.2	−37	5.0	40	3.0
	LM337M	R					
	LM237M#						
	LM137M*						
600	MC1463	R	−3.8	−34	9.0	35	3.0
	MC1563		−3.6	−37	8.5	40	2.7
1500	LM337	T	−1.2	−37	5.0	40	3.0
	LM337	H, K					
	LM237#						
	LM137*						

#T_J = −25 to +150°C
*T_J = −55 to +150°C

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Switching Regulators

Used as the control circuit in PWM, push-pull, bridge and series type switchmode supplies. The devices include the reference, oscillator, pulse-width modulator, phase splitter and output sections. Frequency and duty cycle are independently adjustable.

I_O mA Max	V_{CC} Volts Min	V_{CC} Volts Max	f_o kHz Min	f_o kHz Max	Device	Suffix	T_A °C	Case
40	1	30	2.0	100	MC3420	P	0 to +70	648
						L		620
					MC3520	L	−55 to +125	620
250*	7.0	40	1.0	300	MC34060	P	0 to +70	646
						L		632
					MC35060	L	−55 to +125	632
250	7.0	40	1.0	300	TL494	CN	0 to +70	648
						CJ		620
						IN	−25 to +.85	648
						IJ		620
						MJ	−55 to +125	620
250		>40	1.0	300	TL495**	CN	0 to +70	707
						CJ		726
						IN	−25 to +85	707
						IJ	−25 to +85	726
±400	8	40	0.1	400	SG3525A	N	0° to +70	648
					SG3525A	J	0 to +70	620
					SG2525A	N	−40 to +85	648
					SG2525A	J		620
					SG1525A	J	−55 to +125	620
±400	8	40	0.1	400	SG3527A	N	0 to +70	648
					SG3527A	J		620
					SG2527A	N	−40 to +85	648
					SG2527A	J		620
					SG1527A	J	−55 to +125	620
±200	8	40	0.001	400	SG3526	N	0 to +70	707
					SG3526	J		726
					SG2526	N	−40 to +85	707
					SG2526	J		726
					SG1526	J	−55 to +125	726
1500*	2.5	40	0.1	100	μA78S40	PC	0 to +70	648
					μA78S40	DC		620
					μA78S40	DM	−55 to +125	
1500*	2.5	40	0.1	100	MC34063	PI	0 to +70	626
					MC34063	U		693
					MC33063	PI	−40 to +85	626
					MC33063	U		693
					MC35063	U	−55 to +125	693

*Single output device
**Internal 39 V zener for <40 volt operation

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SEMICONDUCTORS
P.O. BOX 20912 • PHOENIX, ARIZONA 85036

PRECISION REFERENCES
MC1400 MC1400A
MC1500 MC1500A

Tight-Tolerance, Low-Drift Voltage Reference Family
The MC1400 series of ICs is a family of temperature-compensated voltage references for precision data conversion and instrumentation applications. Advances in thin-film resistors, laser-trimming techniques, ion-implanted devices, and monolithic fabrication techniques make this reference both temperature and time stable in applications demanding accuracy to the 12-bit level.

PRECISION VOLTAGE REFERENCES

2.5, 5.0, 6.25 and 10-VOLT

LASER-TRIMMED SILICON MONOLITHIC INTEGRATED CIRCUIT

Features
- Four Different Output Voltages: 2.5, 5.0, 6.25, 10 V
- Tight Absolute Accuracy: ±0.2% Maximum Initial Tolerance
- Single-Component Output Trimming Without Degrading Temperature Coefficient
- Wide Input Voltage Range: (V_{out} + 1.0 V) ≤ V_{in} ≤ 40 V
- Three-Terminal Operation: Positive References That Can Source and Sink Current
- Two-Terminal Operation: Positive or Negative References Floating References
- Low Current Consumption: 1.0 mA Typical
- Very Low Temperature Coefficient
- Low Output Noise Voltage
- Excellent Ripple Rejection: 87 dB Typical at 120 Hz
- Excellent Long Term Stability: 25 ppm/1000 Hrs Typical

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Motorola Semiconductor

Special Regulators

Floating Voltage and Current Regulators
Designed for laboratory type power supplies. Voltage is limited only by the break down voltage of associated, external, series-pass transistors.

V_{out} Volts Min	V_{out} Volts Max	I_O mA Max	Device	Suffix	V_{aux} Volts Min	V_{aux} Volts Max	P_D Watts Max	$\Delta V_{ref}/V_{ref}$ % Line	$\Delta V_{ref}/V_{ref}$ % Load	$\Delta I_L/I_L$ % Max	TC V_{out} %/°C Typ	Case
0	*	*	MC1466	L	21	30	0.75	0.015	0.015	0.2	0.001	632
			MC1566	L	20	35		0.004	0.004	0.1	0.006	

*Dependent on characteristics of external series-pass elements.

Dual ±15 V Tracking Regulators
Internally, the device is set for ±15 V, but an external adjustment can change both outputs simultaneously, from 8.0 V to 20 V.

V_{out} Volts Min	V_{out} Volts Max	I_O mA Max	V_{in} Volts Min	V_{in} Volts Max	Device	Suffix	P_D Watts Max	Reg_{line} mV	Reg_{load} mV	TC %/°C (T_{low} to T_{high}) Typ	T_A °C	Case
14.8	15.2	±100	17	30	MC1468	G	0.8	10	10	3.0	0 to +75	603C
						L	1.0					632
						R	2.4					614
					MC1568	G	0.8				−55 to +125	603C
						L	1.0					632
						R	2.4					614

(continued)

Special Regulators (continued)

Low Temperature Drift, Voltage References

V_{out} Volts Typ	I_O mA Max	$\Delta V_{out}/\Delta T$ ppm/°C Max	Device	Reg_{line} mV Max	Reg_{load} mV Max	T_A °C	Case
1.235 ± 12 mV	20	20 Typ	LM385BZ-1.2	(Note 1)	1.0 (Note 2)	0 to +70	29
			LM285Z-1.2			−40 to +85	
1.235 ± 25 mV			LM385Z-1.2			0 to +70	
2.5 ± 38 mV			LM385BZ-2.5		2.0 (Note 3)		
			LM285Z-2.5			−40 to +85	
2.5 ± 75 mV			LM385Z-2.5			0 to +70	
2.5 ± 5.0 mV	±10	25	MC1400G2	3.0 (Note 4)	10 (Note 7)	0 to +70	601
		10	MC1400AG2				
		40	MC1500G2			−55 to +125	
		10	MC1500AG2				
2.5 ± 25 mV	10	40	MC1403	3.0/4.5 (Note 5)	10 (Note 8)	0 to +70	693, 79, 751
		25	MC1403A				693, 79
		55	MC1503			−55 to +125	
		25	MC1503A				
5.0 ± 10 mV	±10	25	MC1400G5	4.0 (Note 4)	20 (Note 7)	0 to +70	693
		10	MC1400AG5				
		40	MC1500G5			−55 to +125	
		10	MC1500AG5				
5.0 ± 50 mV	10	40	MC1404U5	6.0 (Note 6)	10 (Note 8)	0 to +70	
		25	MC1404AU5				
		55	MC1504U5			−55 to +125	
		25	MC1504AU5				
6.25 ± 10 mV	±10	25	MC1400G6	4.0 (Note 4)	20 (Note 7)	0 to +70	601
		10	MC1400AG6				
		40	MC1500G6			−55 to +125	
		10	MC1500AG6				
6.25 ± 60 mV	10	40	MC1404U6	6.0 (Note 6)	10 (Note 8)	0 to +70	693
		25	MC1404AU6				
		55	MC1504U6			−55 to +125	
		25	MC1504AU6				
10 ± 20 mV	±10	25	MC1400G10	4.0 (Note 4)	20 (Note 7)	0 to +70	601
		10	MC1400AG10				
		40	MC1500G10			−55 to +125	
		10	MC1500AG10				
10 ± 100 mV	10	40	MC1404U10	6.0 (Note 6)	10 (Note 8)	0 to +70	693
		25	MC1404AU10				
		55	MC1504U10			−55 to +125	
		25	MC1504AU10				
2.5 to 37	100	50 Typ	TL431C	Shunt Reference Dynamic Impedance $z \leq 0.5\ \Omega$		0 to +70	29, 626
			TL431I			−40 to +85	693
			TL431M			−55 to +125	693

Notes:
1. Micro-Power Reference Diode Dynamic Impedance (z) $\leq 1.0\ \Omega$ at $I_R = 100\ \mu A$
2. $10\ \mu A \leq I_R \leq 1.0$ mA
3. $20\ \mu A \leq I_R \leq 1.0$ mA
4. $(V_{out} + 1.0\ V) \leq V_{in} \leq 40$ V
5. $4.5\ V \leq V_{in} \leq 15\ V / 15\ V \leq V_{in} \leq 40$ V
6. $(V_{out} + 2.5\ V) \leq V_{in} \leq 40$ V
7. $-10\ mA \leq I_L \leq +10$ mA
8. $0\ mA \leq I_L \leq 10$ mA

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MC14400/01/02/03/05 Mono-Circuit
- On-board Reference
- A-Law/Mu-Law Companding and D3/D4/CCITT Format
- Synchronous and Asynchronous Operation
- 16/18/22 Pin Packages

MC14407
- Per-Channel Full-Duplex Capability
- Power-Down Input
- Mu-Law Digital Format (MC14406/07)
- A-Law CCITT Digital Format (MC14404)

MC14408/09 Binary to Pulse Dialer
- On-Chip Oscillator
- Dialing of Numbers Up to 16 Digits
- Memory Storage and Re-Dialing of Last Telephone Number

MC14410 Tone Encoder
- Single-Tone Capability
- Fast Oscillator Turn-On and Turn-Off Times

MC14411 Baud Rate Generator
- Sixteen Different Output Clock Rates
- Programmable Time Bases for One-of-Four Multiple Output Rates
- Buffered Outputs Compatible with Low-Power TTL

MC14412 0-600 Baud Modem
- Originate and Answer Mode
- Simplex, Half-Duplex and Full-Duplex Operation

MC14413/14 and 145414 PCM Low Pass/Bandpass Filters
- Transmit Bandpass and Received Low Pass (MC14413)
- Transmit and Receive Low Pass (MC14414/5414
- Single-Supply Capability
- ±5 to ±8 Volt Power Supply Ranges
- Two Operational Amplifiers Available

MC14416/17/18 Time Slot Assigner Circuit
- Independent Transmit and Receive Frame Syncs and Enables
- Up to 64 Times Slots Per Frame
- TTL and CMOS Level Compatibility

MC14419 2-of-8 Tone Encoder
- Suppressed Output for Illegal Input Codes
- Codes for Numbers 0-9 Produce a Strobe Pulse

MC142100/5100 Crosspoint Switch
- Power-On Reset (MC145100 Only)
- Large Analog Range

MC145415 Linear Phase Filter
- Dual Low Pass Linear Phase Filter
- ±5 to ±8 Volt Power Supply Range
- Two Op Amps Available

MC145422 2-Wire UDLT
- 2-Wire Master Universal Data Loop Transceiver
- For Voice/Data Transceiver Applications
- Data Rate of 80 kbps

MC145426 2-Wire UDLT
- 2-Wire Slave Universal Data Loop Transceiver
- For Voice Data Transceiver Applications
- Data Rate of 80 kbps

MC145428 Data Set Interface Chip
- Provides Synchronous to Asynchronous Data Conversion
- Provides Asynchronous to Synchronous Data Conversion
- Synchronous Data Rates of 2.048 Mbps
- Asynchronous Data Rates of 128 kbps

MC145429 Telset Audio Interface Chip
- Provides CPU Control of an Analog Signal for Earpiece, Mouthpiece and Speaker Phone
- Provides CPU Control of Analog Signal Gain and Attenuation
- Loop Back Test Feature

MC145432 2600 Hz Tone Signaling Filter
- 2600 Hz Notch and Bandpass Filter
- 2600 Hz Sinewave Generator
- Uncommitted Op Amp Capable of Driving a 600 ohm Load
- On Board Crystal Oscillator or External Clock

MC145433 TuneableNotch/Bandpass Filter
- Independently Tuneable Notch and Bandpass Filter
- Clock Output Pin
- Includes an Uncommitted Op Amp Capable of Driving 600 Loads
- TTL or CMOS Compatible Digital Inputs
- On Board Crystal Oscillator or External Clocks

MC145440/441 300 Baud Modem Filter (Bell 103/CCITT)
- Answer or Originate Mode
- Low Band Bandpass Filter
- High Band Bandpass Filter

MC145445 0-600 Baud Modem
- Originate and Answer Mode
- Bell 103/113 and CCITT V.21

MC145450 0-1200 Baud Modem
- Bell 202 and CCITT V.23
- On Board Crystal Oscillator or External Clock

MC6860 0-600 bps Digital Modem
- Originate and Answer Modes
- Crystal or External Reference Control
- Full-Duplex or Half-Duplex Operation
- Automatic Answer and Disconnect

MC6172 2400 bps Digital Modulator (Formerly 6862)
- 511-Bit CCITT Test Pattern
- CCITT and U.S. Phase Options (Bell 201)
- 1200/2400 bps operation
- Answer-Back Tone

MC6173 2400 bps Demodulator
- Compatible with MC6172 Modulator
- CCITT and U.S. Phase Options
- Compatible Functions for 201B/C Data Sets

National Semiconductor

June 1983

ADC0844 8-Bit µP Compatible A/D Converter with 4-Channel Multiplexer

General Description

The ADC0844 is a CMOS 8-bit successive approximation A/D converter with a versatile analog input multiplexer. The 4-channel multiplexer can be software configured for single-ended, differential or pseudo-differential modes of operation.

The differential mode provides low frequency input common-mode rejection and allows offsetting the analog range of the converter. In addition, the A/D's reference can be adjusted enabling the conversion of reduced analog ranges with 8-bit resolution.

This A/D is designed to operate from the control bus of the NSC800™ and the wide variety of 8080 µP derivatives. TRI-STATE® output latches that directly drive the data bus permit this A/D to be configured as a memory location or as an I/O device to the microprocessor with no interface logic necessary.

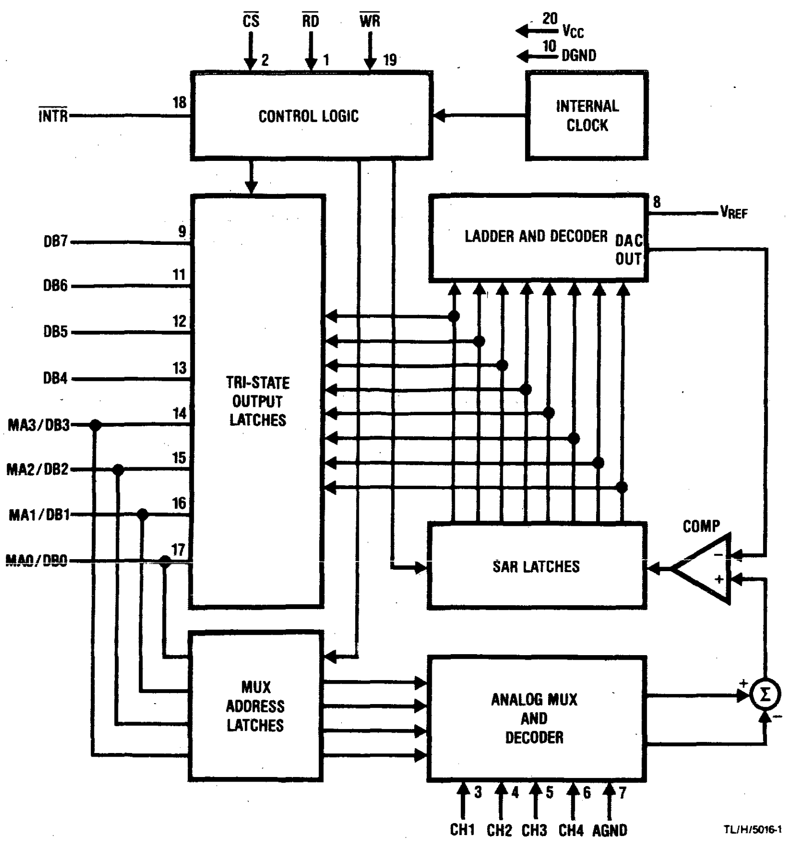
Features

- Compatible with 8080 µP derivatives—no interface logic needed
- Easy interface to all microprocessors
- Operates ratiometrically or with 5 V_{DC} voltage reference
- No zero or full-scale adjust required
- 4-channel multiplexer with address logic
- Internal clock
- 0V to 5V input range with single 5V power supply
- T^2L/MOS input/output compatible
- 0.3″ standard width 20-pin DIP

Key Specifications

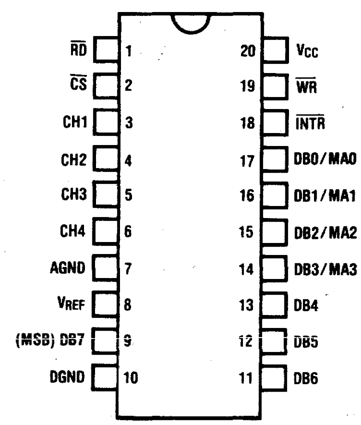
Resolution	8 Bits
Total Unadjusted Error	± 1/2 LSB and ± 1 LSB
Single Supply	5 V_{DC}
Low Power	10 mW
Conversion Time	40 µs

Block and Connection Diagrams



TL/H/5016-1

Dual-In-Line Package



TOP VIEW

TL/H/5016-2

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IM-B30M63/Printed in U.S.A.

National Semiconductor

PRELIMINARY
July 1983

LF13006, LF13007 Digital Gain Set

General Description

The LF13006, LF13007 are precision digital gain sets used for accurately setting non-inverting op amp gains. Gains are set with a 3-bit digital word which can be latched in with $\overline{WR}$ and $\overline{CS}$ pins. All digital inputs are TTL and CMOS compatible.

The LF13006 shown below will set binary scaled gains of 1, 2, 4, 8, 16, 32, 64, and 128. The LF13007 will set gains of 1, 2, 5, 10, 20, 50, and 100 (a common attenuator sequence). In addition, both versions have several taps and two uncommitted matching resistors which allow customization of the gain.

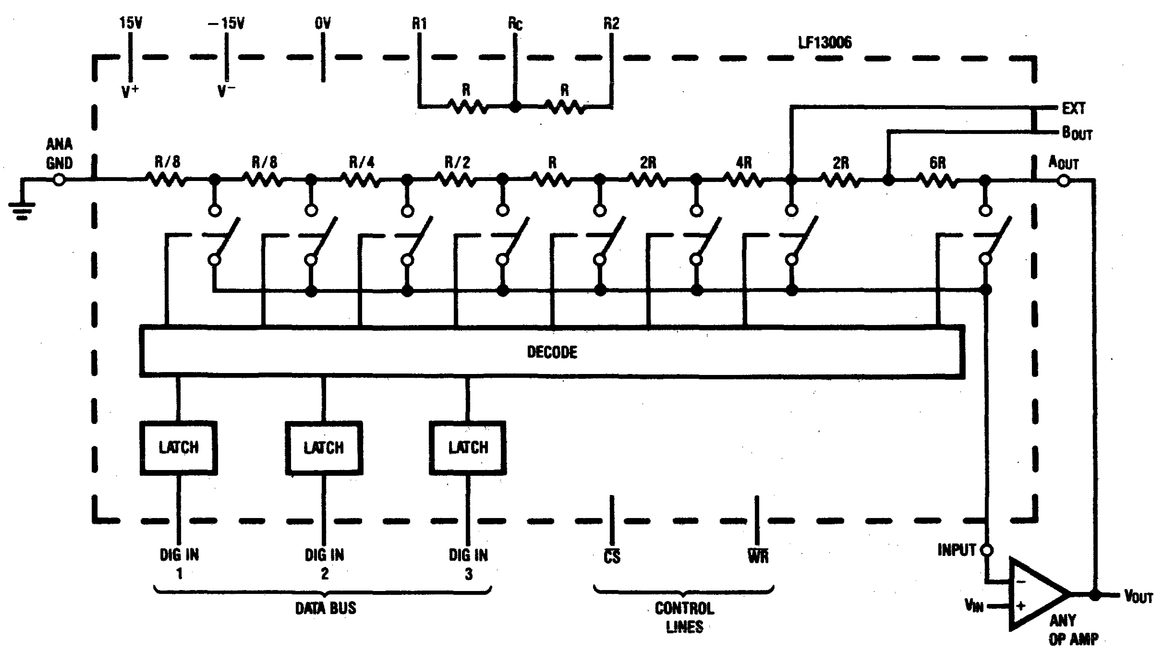
The gains are set with precision thin film resistors. The low temperature coefficient of the thin film resistors and their excellent tracking result in gain ratios which are virtually independent of temperature.

The LF13006, LF13007 used in conjunction with an amplifier not only satisfies the need for a digitally programmable amplifier in microprocessor based systems, but is also useful for discrete applications, eliminating the need to find 0.5% resistors in the ratio of 100 to 1 which track each other over temperature.

Features

- TTL and CMOS compatible logic levels
- Microprocessor compatible
- Gain error 0.5% max
- Binary or scope knob gains
- Wide supply range +5V to ±18V
- Packaged in 16-pin DIP

Block Diagram and Typical Application (LF13006)



IM-B30M73/Printed in U.S.A.

National Semiconductor

PRELIMINARY

Issue date: 4/1/83
Industrial Blocks

BI-LINE[1]

LM1893 CARRIER-CURRENT TRANSCEIVER[2]

General Description

Carrier-current systems use the power mains to transfer information between remote locations. This bipolar carrier-current chip performs as a power line interface for half-duplex (bi-directional) communication of serial bit streams of virtually any coding. In transmission, a sinusoidal carrier is FSK modulated and impressed on most any power line via a rugged on-chip driver. In reception, a PLL-based demodulator and impulse noise filter combine to give maximum range. A complete system may consist of the LM1893, a COPS[1] controller, and discrete components.

---

[1] BI-LINE and COPS are trademarks of National Semiconductor Corp.

[2] Carrier-current transceivers are also called power line carrier (PLC) transceivers.

Features

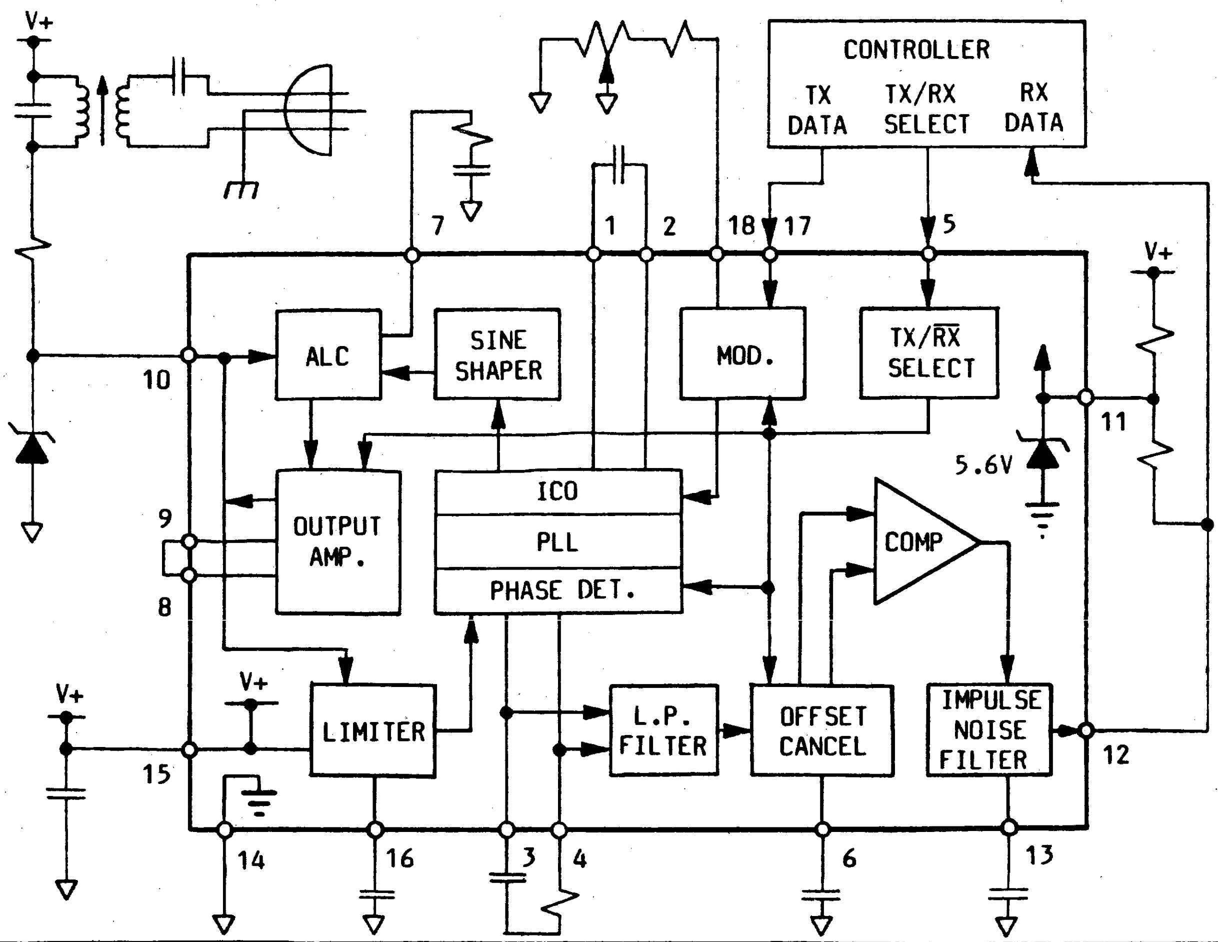
- o Noise resistant FSK modulation
- o User-selected impulse noise filtering
- o Up to 4.8 KBaud data transmission rate
- o Strings of 0's or 1's in data allowed
- o Sinusoidal line drive for low RFI
- o Output power easily boosted 10-fold
- o 50 to 300 KHz carrier frequency choice
- o TTL and MOS compatible digital levels
- o Regulated voltage to power logic
- o Drives all conventional power lines

Applications

- o Energy management systems
- o Home convenience control
- o Inter-office communication
- o Appliance control
- o Fire alarm systems
- o Security systems
- o Telemetry
- o Computer terminal interface

TYPICAL APPLICATION

FIGURE 1. Block diagram of carrier - current chip with a complement of discrete components making a complete transceiver. Use caution with this circuit - dangerous line voltage are present.



National Semiconductor

PRELIMINARY
October 1983

LM2935 Low Dropout Dual Regulator

General Description

The LM2935 positive voltage regulator features a low quiescent current of 3 mA or less when supplying 10 mA loads from the standby regulator output. This unique characteristic and the extremely low input-output differential required for proper regulation (0.55V for output currents of 10 mA) make the LM2935 the ideal regulator for power systems that include standby memory. Applications include processor power supplies demanding as much as 750 mA of output current.

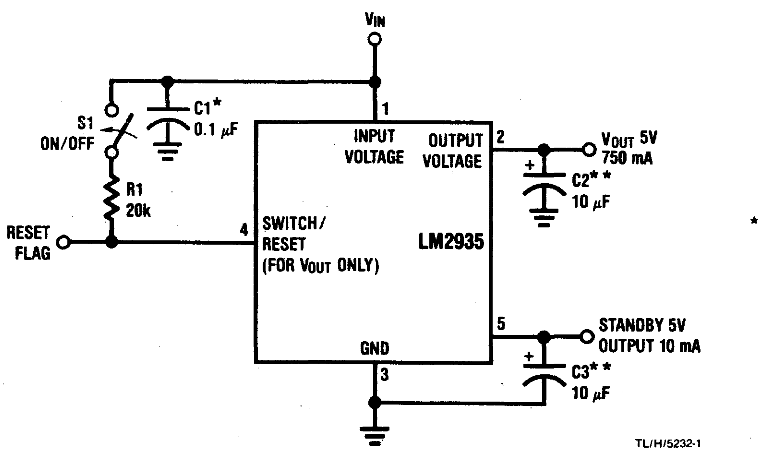
Designed primarily for automotive applications, the LM2935 and all regulated circuitry are protected from reverse battery installations or 2 battery jumps. During line transients, such as a load dump (60V) when the input voltage to the regulator can momentarily exceed the specified maximum operating voltage, the 0.75A regulator will automatically shut down to protect both internal circuits and the load while the standby regulator will continue to power any standby load. The LM2935 cannot be harmed by temporary mirror-image insertion. Familiar regulator features such as short circuit and thermal overload protection are also provided.

Fixed outputs of 5V are available in the plastic TO-220 power package.

Features

- Two regulated outputs
- Output current in excess of 750 mA
- Low quiescent current standby regulator
- Input-output differential less than 0.6V at 0.5A
- Reverse battery protection
- 60V load dump protection
- −50V reverse transient protection
- Short circuit protection
- Internal thermal overload protection
- Available in plastic TO-220
- ON/OFF switch for high current output
- Reset error flag
- 100% electrical burn-in

Typical Application Circuit



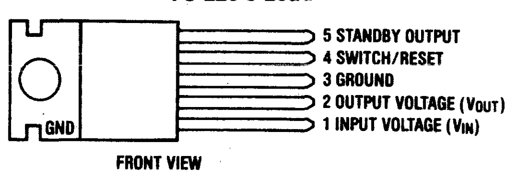
* Required if regulator is located far from power supply filter.

** Required for stability. May be increased without bound. Capacitor must be rated to operate at the minimum temperature expected for the regulator system.

FIGURE 1. Test and Application Circuit

Connection Diagram

TO-220 5-Lead



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PRELIMINARY
October 1983

MF4 4th Order Switched Capacitor Butterworth Lowpass Filter

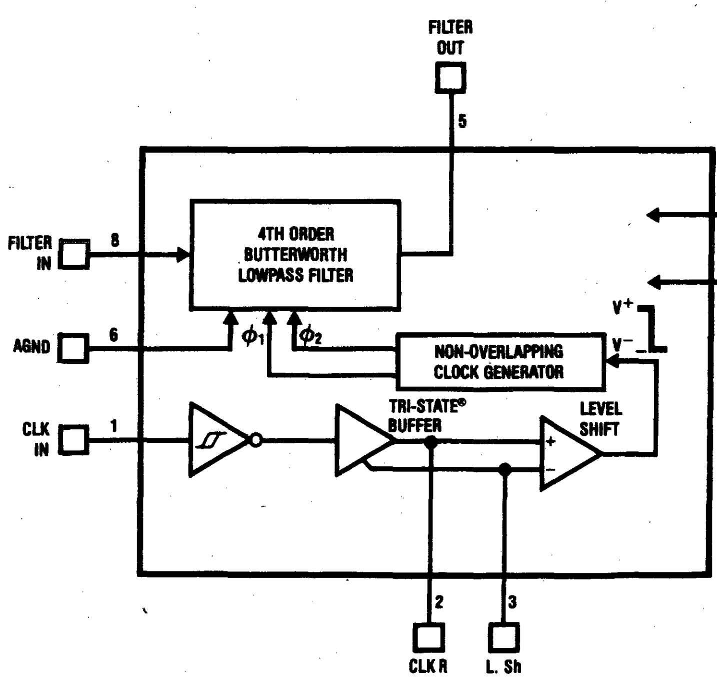
General Description

The MF4 is a versatile, easy to use, precision 4th order Butterworth lowpass active filter. Switched capacitor techniques eliminate external component requirements and allow a clock tunable cutoff frequency. The ratio of the clock frequency to the lowpass cutoff frequency is internally set to 50 to 1 (MF4-50) or 100 to 1 (MF4-100). A Schmitt trigger clock input stage allows two clocking options, either self-clocking (via an external resistor and capacitor) for stand-alone applications, or for tighter cutoff frequency control, a TTL or CMOS logic compatible clock can be directly applied. The maximally flat passband frequency response together with a DC gain of 1 V/V allows cascading MF4 sections for higher order filtering.

Features

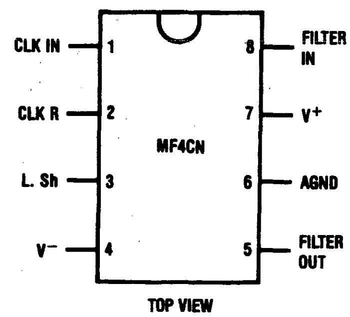
- Low Cost
- Easy to use
- No external components
- 8-pin mini-DIP
- Cutoff frequency accuracy of ±0.3%
- Cutoff frequency range of 0.1 Hz to 20 kHz
- 5V to 14V operation
- Cutoff frequency set by external or internal clock

Block and Connection Diagrams



TL/H/5064-1

Dual-In-Line Package



TL/H/5064-2

Order Number MF4CN
See NS Package N08E

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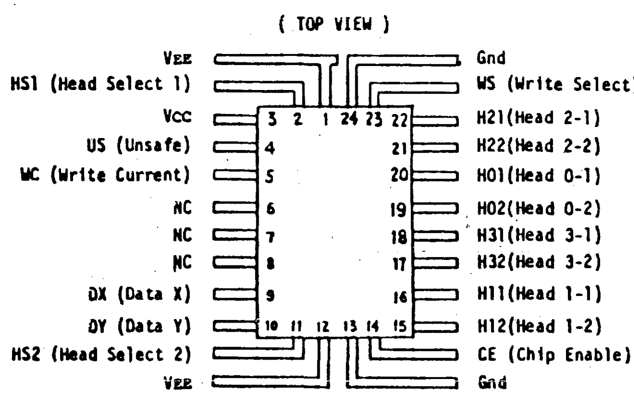
μPC751B/μPC752B BIPOLAR ANALOG INTEGRATED CIRCUITS

Read/Write IC For Disk Drive System

The μPC751B/752B is a monolithic bipolar integrated circuit writing and reading data in a high performance magnetic disk storage system. The circuit is intended for use on a data head support arm. Each circuit can be used with up to four independent heads. Each I.C. contains four write drivers, four read preamplifiers, an output line driver, head select logic, and some fault monitoring circuitry, and has three modes of operation: Read, Write and Idle. The μPC752B is similar to the μPC751B in function, but provides a lower differential gain in the read mode for use with higher inductance and higher output heads. All signal levels and currents are fully compatible with IBM Model 3350 head/arm assembly.

Pin Configuration



Absolute Maximum Ratings

Parameter	Min.	Max.	Units
Positive Supply Voltage, V_{CC}	-0.6	7.0	V
Negative Supply Voltage, V_{EE}	-5.5	0.6	V
Input Voltage	V_{EE}-0.3	V_{CC}+0.3	V
Storage Temperature Range	-65	150	°C
Operating Moving-air Temperature Range	0	70	°C
Operating Junction Temperature Range		150	°C

Recommended Operating Limits

Parameter	Mode	Min.	Max.	Units
V_{CC}	Read/Write/Idle	5.7	6.3	V
V_{EE}	Read/Write/Idle	-4.2	-3.8	V
Unsafe Voltage	Read/Write/Idle	4	V_{CC}+0.3	V
Head Center Tap Voltage	Write	3.2	3.8	V
Write Current (I_{WC})	Write		45	mA

AC Test Conditions
(Unless otherwise specified)

Parameter	Mode		Units
V_{CC}	Read/Write/Idle	6.00±0.01	V
V_{EE}	Read/Write/Idle	-4.00±0.01	V
V_{WS}	Read	0.00±0.01	V
V_{WS}	Write	3.50±0.01	V
V_{CE}	Read/Write	$0.00^{+0.01}_{-0.00}$	V
Lh	Read/Write/Idle	Max. 0.1	μH
Rh	Read/Write/Idle	Max. 0.01	Ω
V_{CT}	Read	0.00±0.01	V
V_{CT}	Write	3.50±0.01	V
V_{US}	Read/Write/Idle	6.00±0.01	V
R_{L1}	Read/Write/Idle	200 ± 1	Ω
R_{L2}	Read/Write/Idle	$101 \pm ^{1}_{0}$	Ω
I_{WC}	Read	0	mA
I_{WC}	Write	40 ± 1	mA
Ambient Temperature	Read/Write/Idle	25 ± 2	°C

Head Selection Table

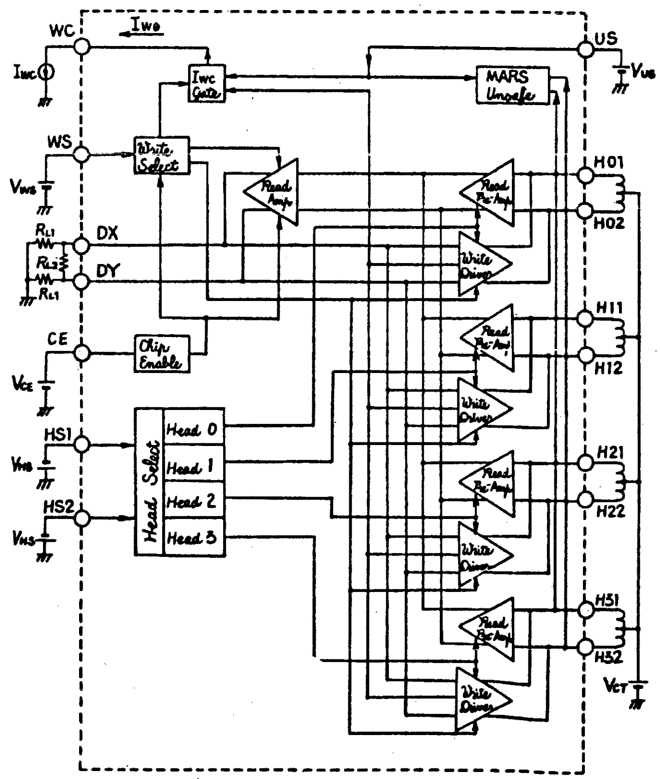
Head Selected	VHS1	VHS2
0	V_{HHS}	V_{HHS}
1	V_{LHS}	V_{HHS}
2	V_{HHS}	V_{LHS}
3	V_{LHS}	V_{LHS}

Mode Select

The Circuit has three modes of operation : Read, Write, and Idle. The state of the Chip Enable and Write Select determines the mode of operation as follows :

Characteristics	Conditions	Min.	Max.	Units
(Chip Enable)				
V_{HCE}	Idle	5.5	6.3	V
V_{LCE}	Read/Write	0.0	0.7	V
I_{HCE}	Idle, V_{CE}=V_{CC} - 0.5V	-110	-50	μA
I_{LCE}	Read/Write, V_{CE}=0.0V	-1.3	-0.7	mA
(Write Select)				
V_{HWS}	Write/Idle	3.2	3.8	V
V_{LWS}	Read/Idle	-0.1	0.1	V
I_{HWS}	Write/Idle (transition unsafe current off)	0.35	2.7	mA
	Write (transition unsafe current on)	0.7	3.5	mA
I_{LWS}	Read/Idle		0.1	mA
Switching Delay	All Modes		0.5	μS

Connection Diagram



Supply Current:

Characteristics	Conditions	Min.	Max.	Units
I_{CC}(R/W)	Read/Write	12	20	mA
I_{CC}(ID)	Idle		150	μA
I_{EE}(R/W)	Read/Write		70	mA
I_{EE}(ID)	Idle		40	mA

Total Head Input Current:

Sum of all head input currents with I_{WC}=0

Characteristics	Conditions	Min.	Max.	Units
I_{HC}(W)	Write, V_{CT}=3.5V		3.0	mA
I_{HC}(R)	Read, V_{CT}=0.0V		0.16	mA
I_{HC}(ID)	Idle, V_{CT}=3.5 or 0.0V		0.10	mA

Head Select:

One of four heads may be selected by controlling the state of two head select inputs. The head is selected as specified below :

Characteristics	Conditions	Min.	Max.	Units
V_{HHS}	Temp=0°C∿70°C	-0.97	-0.61	V
V_{LHS}	Temp=0°C∿70°C	-2.38	-1.52	V
I_{HHS}			240	μA
I_{LHS}			60	μA
Switching Delay			50	ns

Read Mode: (μPC751B)

In the Read mode the circuit functions as a low noise differential amplifier. The state of the head select inputs determines which amplifier is active.

Characteristics	Conditions		Min.	Max.	Units
Input Current	Vin=0v			20	μA
Differential Input Capacity	Vin=0v			18.8	pF
Differential Input Resistance (Damping Resistor)	Vin=0v	25°C 0°C 70°C	585 565 585	915 915 984	Ω Ω Ω
Output Offset Voltage	Vin=0v			100	mV
Common Mode Output Voltage	Vin=0v		-0.75	-0.50	V
Differential Gain	Vin=1mVp-p, OVDC f=300KHz	25°C 0°C 70°C	28 30 27	43 45 40	V/V V/V V/V
Gain Linearity (DC)	$\frac{Vo(Vin=5mV) - Vo(Vin=0mV)}{Vo(Vin=0.5mV)-Vo(Vin=0mV)} / \frac{5.0mV}{0.5mV}$		0.9	1.1	
Band Width	Zin=0Ω Vin=1mVp-p $\frac{Gain\ @\ f_{BW}}{Gain\ @\ 300KHz}$=-3dB		30		MHz
Input Noise	Vin=0v Zin=0Ω 15MHz Power Bandwidth			6.6	μVRMS
Common Mode Input to Differential Output Rejection Ratio	Vin=5mVp-p, OVDC, f≤5MHz		45		dB
Power Supply Rejection Ratio (referred to the input)	Vin=0v, f≤5MHz ΔVcc orΔV_{EE}=0.1Vp-p		45		dB
Channel Separation	Vin=1mVp-p, OVDC, f=300KHz, 3Channels driven		40		dB
Unsafe Current	Write Current = 0mA			0.1	mA
	Write Current = 45mA		40	45	mA

LINEAR

NEC Electronics

Read Mode : (μPC752B)

The same as μPC751B except for the following characteristics.

Characteristics	Conditions	Min.	Max.	Units
Output Offset Voltage	Vin=0v		50	mV
Differential Gain	Vin=1mVp-p, OVDC 25°C f=300KHz	8.5	12.5	V/V
	0°C	8.5	13.25	V/V
	70°C	7.5	12.5	V/V
Gain Linearity (DC)	$\frac{Vo(Vin=15mV) - Vo(Vin=0mV)}{Vo(Vin=0.5mV)-Vo(Vin=0mV)} / \frac{15.0mV}{0.5mV}$	0.9	1.1	
Input Noise	Vin=0v Zin=0Ω 15MHz Power Bandwidth		25	μVRMS

Write Mode:

In the Write mode the circuit functions as a current gate. Externally supplied Write current is gated by the state of the head select and data inputs to one side of one head.

Characteristics	Conditions	Min.	Max.	Units
Differential Input Voltage		0.225		V
Single Ended Input Voltage		-2.0	-0.45	V
DX DY Input Current		-2.0	+2.0	mA
Current Gain	Iwc=45mA	0.95	1.0	
Write Current Voltage	Iwc=45mA	-3.7	-3.0	V
Head Current Transition Time	Iwc=45mS, Lh=0 f=5MHz		15	nS
Head Current Switching Delay Time	Iwc=45mA, Lh=0 f=5MHz		15	nS
Head Current Switching Hysterisis	Iwc=45mA, Lh=0 f=5MHz Data rise & fall time≤1nS		2	nS
Unsafe Current	Iwc=30mA, f=2MHz, Lh=9μH		0.1	mA
	Iwc=30mA, f=2MHz, Lh=0μH	20		mA
	Iwc=45mA, Rh=∞ one side of head only	20		mA
Unsafe Switching Delay Time	Iwc=30mA, f=2MHz, Lh=9μH		1.0	μS
	Iwc=30mA, f=2MHz, Lh=0μH	1.0	4.0	μS
	Iwc=45mA, f=2MHz, Rh=∞	1.0	4.0	μS
Unselected Head Current	Iwc=45mA, f=2MHz Lh=9.5μH		1.5	mAo-p
Differential Head Voltage	Iwc=45mA, Lh=10μH		9.0	Vo-p

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μPC754D BIPOLAR ANALOG INTEGRATED CIRCUIT

General Description

The μPC754D is a two-stage wideband differential amplifier. It is intended for use as a pre-amplifier for the magnetic servo head of a magnetic disc memory system.

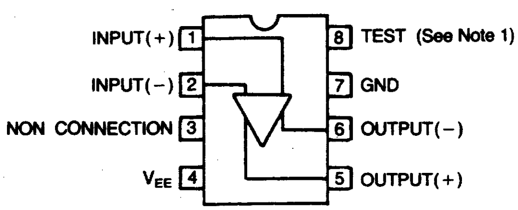
FEATURES

- Very narrow gain range
- 30 MHz bandwidth

ABSOLUTE MAXIMUM RATINGS

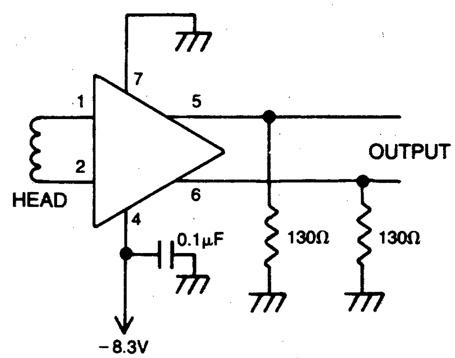
Power Supply Voltage (V_{EE})	−12 V
Differential Input Voltage	±1 V
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−65 to +150°C

CONNECTION DIAGRAM (Top View)



Note 1. Pin 8 can NOT be connected to any circuit.

CONNECTION DIAGRAM
Recommended Load Condition



Note. A 0.1μF ceramic capacitor is recommended for good power supply noise filtering.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage	V_{EE}	−7.45	−8.3	−9.15	V
Input Signal	V_I		2		mVpp
Ambient Temperature	Ta	0		70	°C

ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{EE} = −8.3V ± 10%)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Gain	R_L = 130Ω	77	93	110	
Bandwidth	Vi = 2mVpp	10	30		MHz
Input Resistance		800	1000	1250	Ω
Input Capacitance			3		pF
Output Dynamic Range (Differential)	R_L = 130Ω, V_{EE} = −8.3V	350			mVpp
Power Supply Current	V_{EE} = −9.15V		26	35	mA
Output Offset	R_S = 0, R_L = 130Ω			±600	mV
Equivalent Input Noise	R_S = 0, R_L = 130Ω, BW = 4MHz		8	14	μV
PSPR, Input Referred	R_S = 0, f ≦ 5 MHz	50	65		dB
Gain Sensitivity (Supply)	ΔV_{EE} = ±10%, R_L = 130Ω		±1.3		%
Gain Sensitivity (Temp)	Ta = 25°C to 70°C, R_L = 130Ω		−0.2		%/°C
CMRR, Input Referred	f ≦ 5MHz	55	70		dB

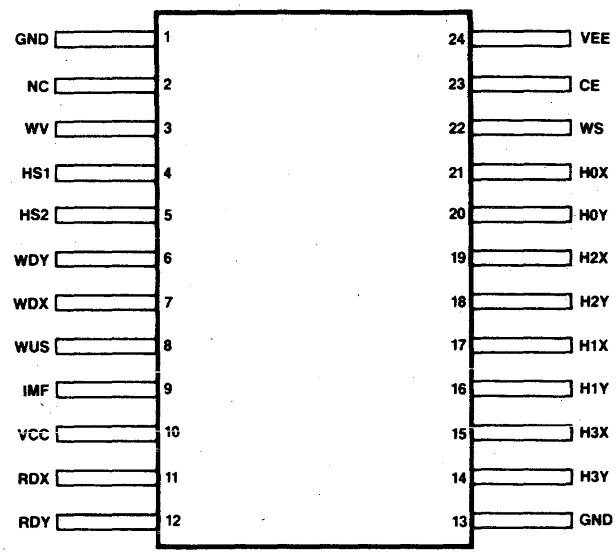
MC4290
BIPOLAR INTEGRATED CIRCUIT

Description

The circuit is an integrated Read/Write chip intended for use with non-center tapped thin film heads in disk drive systems. Each chip controls four heads, and has three modes of operation: read, write and idle.

The chip has four channels of read amplifiers and write drivers. It also has an internal write current source. The write current magnitude is determined by laser trimmed internal resistors. The chip contains fault detection circuits.

PIN CONFIGURATION (Top View)



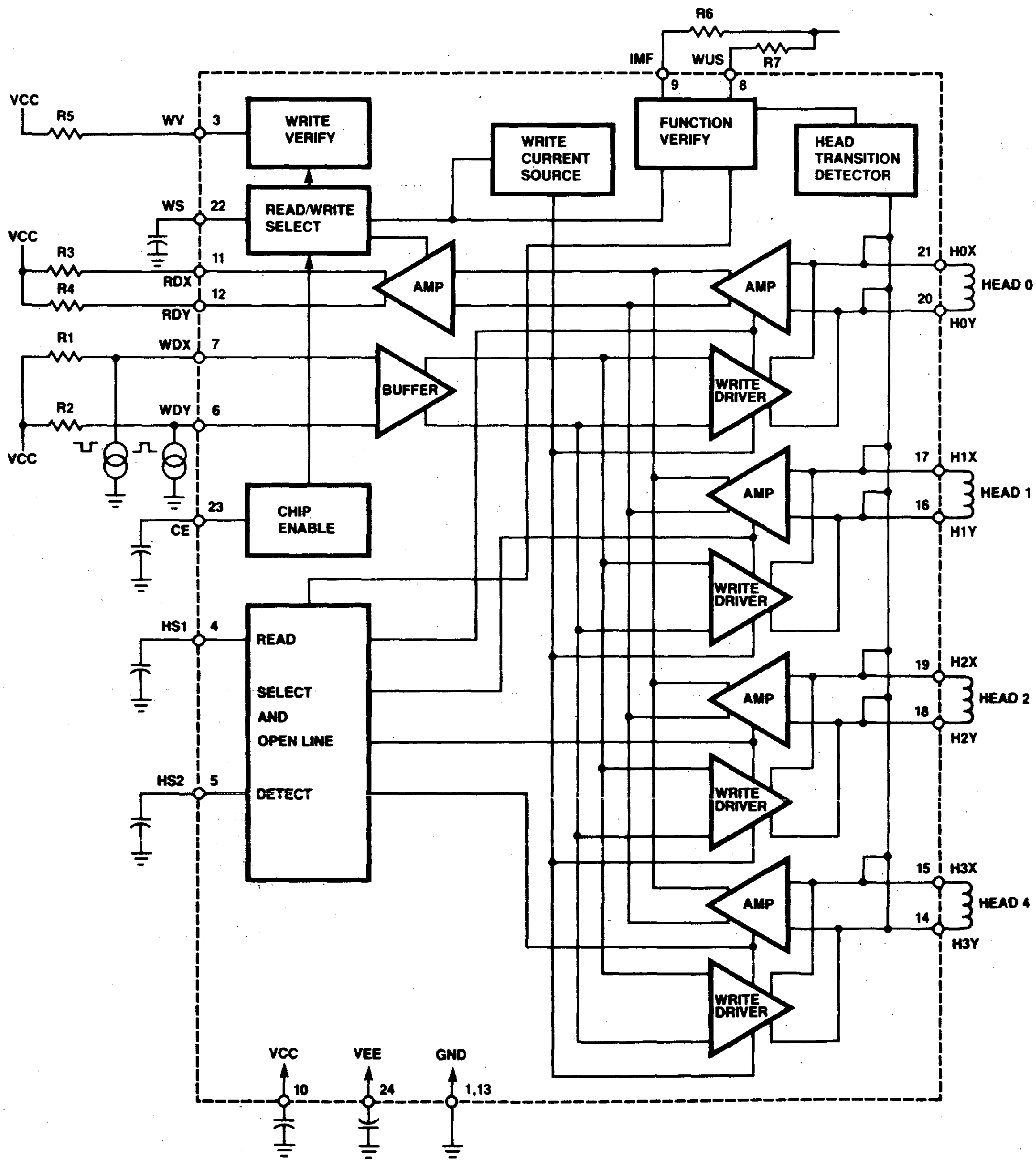
PIN NAMES AND DEFINITIONS

CE = Chip Enable
WS = Write Select
HS1 = Head Select 1
HS2 = Head Select 2
WDX = Write Data X
WDY = Write Data Y
RDX = Read Data X
RDY = Read Data Y
WV = Write Verify (write Select OK)
IMF = Input Multi Fault
WUS = Write Unsafe (Write Operation OK)

RECOMMENDED OPERATING LIMITS

PARAMETER	MODE	MIN	MAX	UNIT
V_{CC}	Read/Write/Idle	4.75	5.25	V
V_{EE}	Read/Write/Idle	−5.46	−4.75	V
Write Mode Duty			50	%

BLOCK DIAGRAM



PIN NAMES AND DEFINITIONS

CE	=	Chip Enable
WS	=	Write Select
HS1	=	Head Select 1
HS2	=	Head Select 2
WDX	=	Write Data X
WDY	=	Write Data Y
RDX	=	Read Data X
RDY	=	Read Data Y
WV	=	Write Verify (write Select OK)
IMF	=	Input Multi Fault
WUS	=	Write Unsafe (Write Operation OK)

RESISTOR VOLTAGE

R1	=	100Ω	±	1%
R2	=	100Ω	±	1%
R3	=	100Ω	±	1%
R4	=	100Ω	±	1%
R5	=	1k	±	1%
R6	=	330Ω	±	1%
R7	=	1k	±	1%

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, 4.75 V ≤ V_{CC} ≤ 5.25 V, −5.46 V ≤ V_{EE} ≤ − 4.75 V, 25°C ≤ T_J ≤ 125°C

POWER SUPPLY CURRENT

CHARACTERISTICS		CONDITION	TYP	UNIT
I_{CC}	Idle	V_{CE} = 2 V		mA
	Read	V_{CE} = 0 V, V_{WS} = 2 V	47	mA
	Write	V_{CE} = 0 V, V_{WS} = 0 V	37	mA
I_{EE}	Idle	V_{CE} = 2 V		mA
	Read	V_{CE} = 0 V, V_{WS} = 2 V	50	mA
	Write	V_{CE} = 0 V, V_{WS} = 0 V	120	mA

HEAD SELECT

CHARACTERISTICS	CONDITION	MIN	MAX	UNIT
V_{HS1H}, V_{HS2H}		2.0		V
V_{HS1L}, V_{HS2L}		−0.3	0.8	V
I_{HS1H}, I_{HS2H}			50	µA
I_{HS1L}, I_{HS2L}		−1.6		mA
Switching Delay	All Mode		0.4	µS

HEAD SELECTION TABLE

HEAD SELECTED	V_{HS1}	V_{HS2}
0	L	L
1	H	L
2	L	H
3	H	H

L = LOW level H = HIGH level

MODE SELECT

CHARACTERISTICS	CONDITION	MIN	MAX	UNIT
Chip Enable				
V_{CEH}	Idle	2.0		V
V_{CEL}	Read or Write	−0.3	0.8	V
I_{CEH}	Idle V_{CE} = 5.0 V		50	µA
I_{CEL}	Read or Write, V_{CE} = 0 V	−4.0		mA
Switching Delay	All Mode		0.5	µS
Write Select				
V_{WSH}	Read or Idle	2.0		V
V_{WSL}	Write or Idle	−0.3	0.8	V
I_{WSH}	Read or Idle		50	µA
I_{WSL}	Write or Idle	−1.6		mA
Switching Delay	All Mode		0.5	µS

WRITE MODE

CHARACTERISTICS	CONDITION	MIN	MAX	UNIT
Differential Input Voltage		0.2		V
Single-ended Input Voltage		−1.87	0.1	V
Input Current/Side		−20	120	μA
Input Capacitance/Side			10	pF
Write Current		67.9	72.1	mA o-p
Write Current Tolerance		−3	+3	%
Write Current Transition Time	I_{WC} = 70 mA o-p, R_H = 8 Ω, L_H = 0.1 μH		17	nS
Write Current Switching Delay Time	I_{WC} = 70 mA o-p, L_H = 0 μH		15	nS
Write Current Switching Delay Time Asymmetry	I_{WC} = 70 mA o-p, L_H = 0 μH		1	nS
Unselected Head Current	I_{WC} = 100 mA o-p, f = 5 MHz, R_H = 8 Ω, L_H = 0.1 μH		2	mA o-p
Output Resistance		840	1260	Ω
Output Capacitance			30	pF
Differential Head Voltage Swing			6	V o-p

READ MODE

CHARACTERISTICS	CONDITION		MIN	MAX	UNIT
Input Bias Current	V_{IN} = 0 V			36	μA
Input Offset Current	V_{IN} = 0 V			20	μA
Differential Input Resistance	V_{IN} = 0 V		520	1170	Ω
Differential Input Capacitance	V_{IN} = 0 V			40	pF
Differential Input Noise Voltage	V_{IN} = 0 V, Z_{IN} = 0 Ω, B_W = 15 MHz			6.6	μVrms
Differential Voltage Gain	V_{IN} = 1 mV p-p, f = 1 MHz				
	T_A = 25°C		100	150	V/V
	T_A = 0°C				V/V
	T_A = 70°C				V/V
Input Dynamic Range	Gain Is 90% of the Gain With 0.5 mV p-p Input Signal f = 1 MHz		6		mV p-p
Voltage Band Width	V_{IN} = 1 mV p-p	± 1 dB	25		MHz
		−3 dB	45		MHz
CMRR	V_{IN} = 5 mV p-p	f = 10 MHz	54		dB
		(f = 20 MHz)	48		dB
PSRR	V_{IN} = 0 mV	f = 10 MHz	58		dB
		(f = 20 MHz)	50		dB
Channel Separation	V_{IN} = 0 mV 3 Channel Driven	f = 10 MHz	40		dB
Output CM Voltage	R_L = 100 Ω to V_{CC}, T_j = 75°C		V_{CC} −0.75	V_{CC} −0.50	V
Output Offset Voltage	R_L = 100 Ω to V_{CC}		−360	360	mV
Output Leak Current	V_{CE} = 2 V (Idle)			10	μA
Output Resistance	Single-ended		10		kΩ
Output Capacitance	Single-ended			10	pF

FAULT DETECTION

CHARACTERISTICS	CONDITION	MIN	MAX	UNIT
I_{IMFH}	V_{CE} = 0 V, Read or Write	2.85	3.15	mA
I_{IMFL}	V_{CE} = 2 V, Idle		20	μA
IMF Switching Delay Time	Chip Enable ON/OFF		0.5	μS
V_{WVL} Write Select OK	V_{CE} = 0 V, V_{WS} = 0 V I_{WV} = 16 mA	0	0.4	V
I_{WVH} Write Select OK	V_{CE} = 0 V, V_{WS} = 2 V	0	250	μA
	V_{CE} = 2 V	0	250	μA
WV Switching Delay Time	Write Mode ON/OFF		0.5	μS
I_{WUSH} Write Operation OK	V_{CE} = 2 V	0	250	μA
	V_{CE} = 0 V, V_{WS} = 2 V	0	250	μA
	V_{CE} = 0 V, V_{WS} = 0 V L_H = 0 μH, R_H = 0 Ω f (Write Date) = 5 MHz	0	250	μA
	V_{CE} = 0 V, V_{WS} = 0 V R_H = ∞ f (Write Date) = 5 MHz	0	250	μA
	V_{CE} = 0 V, V_{WS} = 0 V L_H = 0.1 μH, R_H = 8 Ω f (Write Date) = 200 kHz	0	250	μA
	V_{CE} = 0 V, V_{WS} = 0 V L_H = 0.1 μH, R_H = 8 Ω f (Write Date) = 5 MHz Head Select Line → Open	0	250	μA
V_{WUSL} Write Operation OK	V_{CE} = 0 V, V_{WS} = 0 V L_H = 0.05 μH, R_H = 5 Ω f (Write Date) = 1 to 10 MHz	0	0.4	V
WUS Switching Delay Time	Unsafe → Safe		1	μS
	Safe → Unsafe	(1)	3.6	μS

μPC1651G BIPOLAR ANALOG INTEGRATED CIRCUIT

Description

The μPC1651G is a silicon monolithic integrated circuit especially designed as wide band amplifier covered from HF band to UHF band.

Features

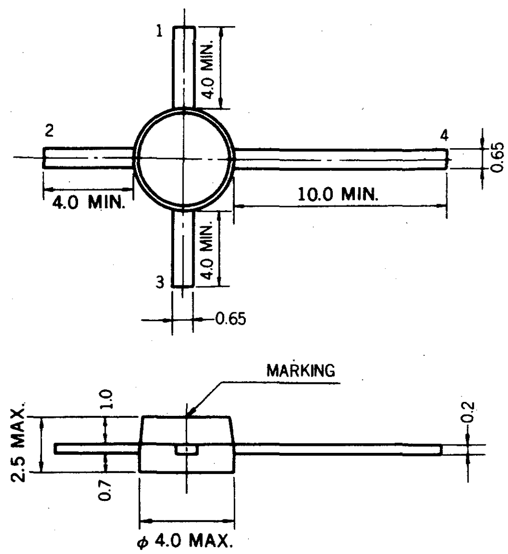
- ☐ Excellent frequency response; TYP. 1200 MHz @3 dB down
- ☐ High power gain; TYP. 19 dB @f = 500 MHz
- ☐ Low voltage operation; 5V
- ☐ Small package

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Supply Voltage	V_{CC}	6	V
Total Power Dissipation	P_T	250	mW
Operating Temperature	T_{opt}	-20 to + 75	°C
Storage Temperature	T_{stg}	-40 to + 125	°C

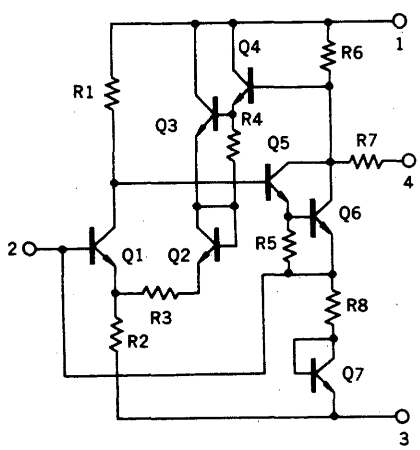
PACKAGE DIMENSIONS

in millimeters



1. V_{CC}
2. INPUT
3. GND
4. OUTPUT

EQUIVALENT CIRCUIT

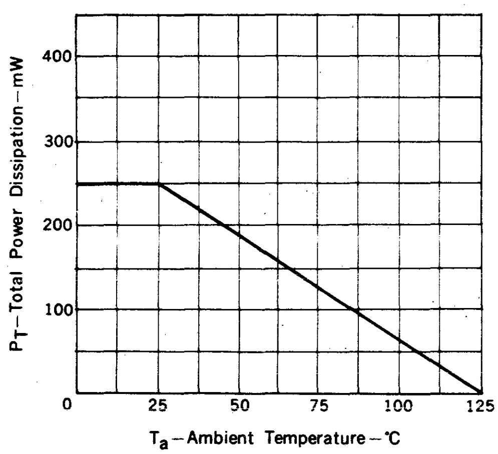


ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

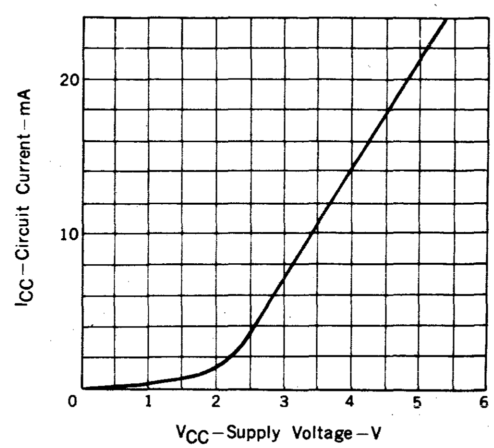
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Circuit Current	I_{CC}	15	20	25	mA	V_{CC} = 5 V
Gain	G_V	16	19		dB	V_{CC} = 5 V, f = 500 MHz
Noise Figure	NF		5.5	6.5	dB	V_{CC} = 5 V, f = 500 MHz
Band Width	BW	1 000	1 200		MHz	V_{CC} = 5 V, 3 dB down
Isolation	I_{so}	20	24		dB	V_{CC} = 5 V, f = 500 MHz
Input Return Loss	$\|S_{11}\|$		15		dB	V_{CC} = 5 V, f = 500 MHz
Output Return Loss	$\|S_{22}\|$		10		dB	V_{CC} = 5 V, f = 500 MHz
Maximum Output Level	V_{OM}		112		dBμV	V_{CC} = 5 V, f = 500 MHz

TYPICAL CHARACTERISTICS ($T_a = 25\,°C$)

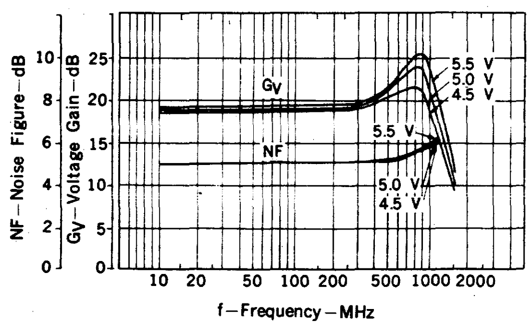
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



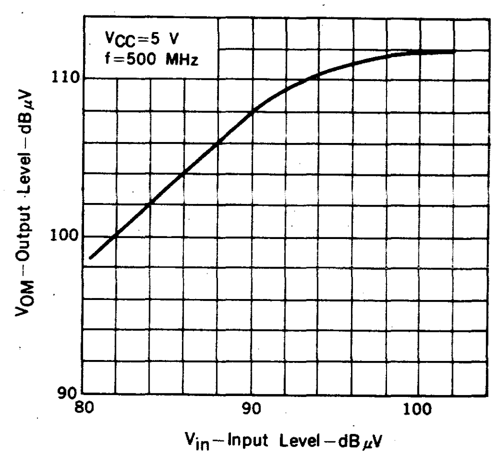
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



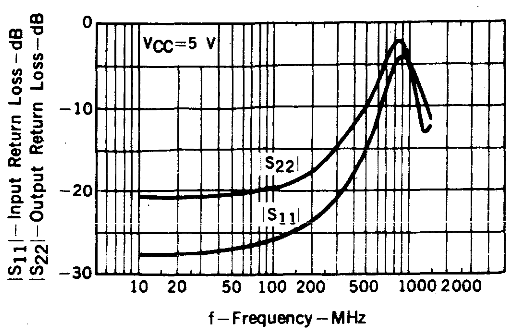
NOISE FIGURE AND VOLTAGE GAIN vs. FREQUENCY



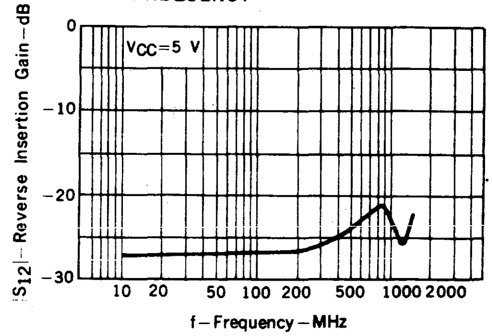
OUTPUT LEVEL vs. INPUT LEVEL



INPUT AND OUTPUT RETURN LOSS vs. FREQUENCY



REVERSE INSERTION GAIN vs. FREQUENCY



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Linear IC (OP AMPS/Comparators/Voltage Regulators)

Operational Amplifiers

				Package	Supply Voltage (V)	Power Consumption (mW)	Input Offset Voltage MAX (mV)	Input Offset Current MAX (nA)	Input Bias Current MAX (nA)	Output Voltage MIN (V)	Slew Rate TYP (V/μs)	Equiv. Vn (Input) TYP (μVrms)
Dual Power Supply	Low Noise Types	Dual	AN6550	9-SIP	±2 to ±12 4 to 24	15	6	200	500	±1	0.8	2.5
			AN6551		±4 to ±15 8 to 30	170	6	200	500	±10	1.0	2.5
			AN6555		±4 to ±15 8 to 30	170	6	200	500	±10	2.0	1.5
			AN6557	9-SIP(LP)	±4 to ±15 8 to 30	240	3	200	—	±10	6.0	0.9
			AN6558 (AN6552)	8-DIP	±4 to ±15 8 to 30	170	6	200	500	±10	1.0	2.5
			AN6553		±4 to ±15 8 to 30	170	6	200	500	±10	2.0	2.5
			AN6556		±4 to ±15 8 to 30	170	6	200	500	±10	2.0	1.5
			AN6558		±4 to ±15 8 to 30	240	3	200	—	±10	6.0	0.9
			AN6558S	SO-8D	±4 to ±15 8 to 30	170	6	200	500	±10	1.0	2.5
			AN6556S		±4 to ±15 8 to 30	170	6	200	500	±10	2.0	.5
		Quad	AN6554	14-DIP	±2 to ±15 4 to 30	240	5	50	300	±10	1.6	2.5
			AN6554NS	SO-14D	±2 to ±15 4 to 30	240	5	50	300	±10	1.6	2.5
	General Purpose	Single	AN6573	7-SIP	±2 to ±15 4 to 30	85	4	100	250	±10	0.7	4.0
			AN6593	9-SIP(LP)	±1 to ±18 2 to 36	3	6	20	75	±12	—	—
			AN1741 (AN6570)	8-DIP	±2 to ±15 4 to 30	85	4	100	250	±10	0.7	4.0
			AN4250		±1 to ±18 2 to 36	3	6	20	75	±12	—	—
			AN1741S	SO-8D	±2 to ±15 4 to 30	85	4	100	250	±10	0.7	4.0
			AN4250S	SO-8D	±1 to ±18 2 to 36	3	6	20	75	±12	—	—
		Dual	AN6571	9-SIP(LP)	±2 to ±15 4 to 30	170	4	100	250	±10	0.7	4.0
			AN1458 (AN6572)	8-DIP	±2 to ±15 4 to 30	170	4	100	250	±10	0.7	4.0
			AN1458S	SO-8D	±2 to ±15 4 to 30	170	4	100	250	±10	0.7	4.0
Single Power Supply	General Purpose	Dual	AN6561	9-SIP	±1.5 to ±15 3 to 30	6	7	50	250	$V_{CC}-1.5$	0.3	6.0
			AN1358 (AN6562)	8-DIP	±1.5 to ±15 3 to 30	6	7	50	250	$V_{CC}-1.5$	0.3	6.0
			AN1358S	SO-8D	±1.5 to ±15 3 to 30	6	7	50	250	$V_{CC}-1.5$	0.3	6.0
		Quad	AN1324 (AN6564)	14-DIP	±1.5 to ±15 3 to 30	10	7	50	250	$V_{CC}-1.5$	0.3	6.0
			AN1324NS	SO-14D	±1.5 to ±15 3 to 30	10	7	50	250	$V_{CC}-1.5$	0.3	6.0

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One Panasonic Way, Secaucus, N.J. 07094 • Tel: (201) 348-5269 • TWX: 710-992-8920

Linear IC (OP AMPS/Comparators/Voltage Regulators)

Comparators

		Package	Supply Voltage (V)		Supply Current MAX (mA)	Input Offset Voltage MAX (mV)	Input Offset Current MAX (nA)	Input Bias Current MAX (nA)	Output Current MIN (mA)	Response Time TYP (ms)
Dual	AN6913	9-SIP	±1 to ±18	2 to 36	1.5	5	50	250	10	1.3
	AN6915		±1 to ±18	2 to 36	5.3	5	50	200	70	2.0
	AN1393 (AN6914)		±1 to ±18	2 to 36	1.5	5	50	250	10	1.3
	AN6916	8-DIP	±1 to ±18	2 to 36	5.3	5	50	200	70	2.0
	AN1393S	SO-8D	±1 to ±18	2 to 36	1.5	5	50	250	10	1.3
	AN6916S		±1 to ±18	2 to 36	5.8	5	50	200	70	2.0
Quad-ruple	AN1339	14-DIP	±1 to ±18	2 to 36	1.5	5	50	250	6	1.3
	(AN6912)		±1 to ±18	2 to 36	1.5	5	50	250	6	1.3
	AN6918		±1 to ±18	2 to 36	10.0	5	50	200	70	2.0
	AN1339S	SO-14D	±1 to ±18	2 to 36	1.5	5	50	250	6	1.3

Voltage Regulators

Positive Output 3 Terminals (AN7800/AN78M00/AN78L00 Series)

I_O	Output Voltage (V)											
	4	5	6	7	8	9	10	12	15	18	20	24
1A	—	AN7805	AN7806	AN7807	AN7808	AN7809	AN7810	AN7812	AN7815	AN7818	AN7820	AN7824
0.5A	—	AN78M05	AN70M06	AN78M07	AN78M08	AN78M09	AN78M10	AN78M12	AN78M15	AN78M18	AN78M20	AN78M24
0.1A	AN78L04	AN78L05	AN78L06	AN78L07	AN78L08	AN78L09	AN78L10	AN78L12	AN78L15	AN78L18	AN78L20	AN78L24

Package: AN7800/AN78M00 Series = TO-220, AN78L00 Series = TO-92

Negative Output 3 Terminals (AN7900 Series)

I_O	Output Voltage (V)										
	−5	−6	−7	−8	−9	−10	−12	−15	−18	−20	−24
1A	AN7905	AN7906	AN7907	AN7908	AN7909	AN7910	AN7912	AN7915	AN7918	AN7920	AN7924

Package: TO-220

Hall IC Series

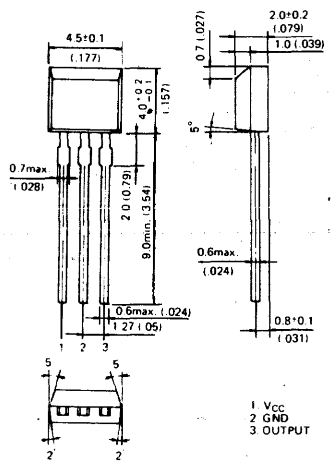
Specifications

Selection Guide

Package	Type No.	Type	Supply Voltage (V)	Operating Ambient Temp. Range (°C)	Magnetic Flux Density (Gauss)	Output Current (mA) (Value for One Output)	Output
4-Lead	DN834	Switch Type	4.5 to 5.5	−20 to +75	100 to 750	15	DTL
	DN835	Linear Type	4.5 to 5.5	−20 to +75	−350 to 350	−15 to 4.4	Emitter Follower
	DN837	Switch Type	4.5 to 5.5	−20 to +75	100 to 750	15	Open Collector
	DN838	Switch Type	8 to 16	−40 to +100	−300 to 300	−1 to 20	DTL
	DN839	Switch Type	4.5 to 16	−20 to +75	100 to 750	20	Open Collector
4-Lead	DN6835	Linear Type	4.5 to 5.5	−20 to +75	−500 to 500	−15 to 4.4	Emitter Follower
	DN6836	Linear Type	4.5 to 5.5	−20 to +75	−500 to 500	−15 to 4.4	Emitter Follower
	DN6837	Switch Type	4.5 to 5.5	−20 to +75	100 to 750	15	Open Collector
	DN6838	Switch Type	8 to 16	−40 to +100	−300 to 300	20	DTL
	DN6839	Switch Type	4.5 to 16	−20 to +75	100 to 750	20	Open Collector

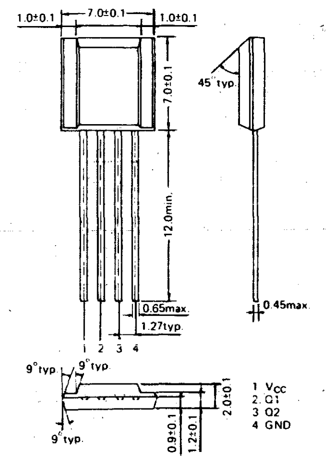
Dimensions

unit: mm (inch)



3-Lead Plastic Package

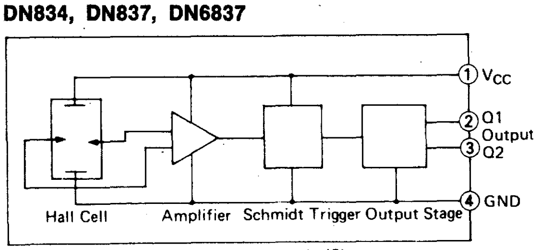
unit: mm



4-Lead Plastic Package

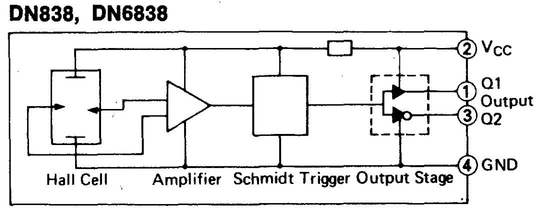
Circuit Block Diagram

DN834, DN837, DN6837



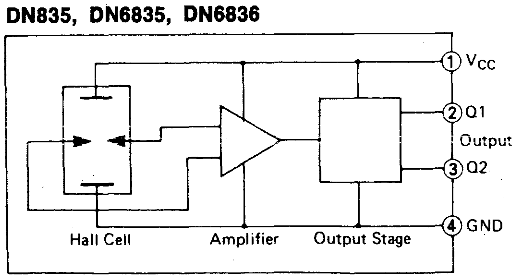
Note: DN6837 V_{CC} = (1), Output = only (3)
GND = (2)

DN838, DN6838



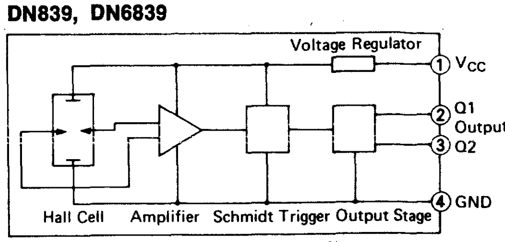
Note: DN6838 V_{CC} = (1), Output = only (3),
GND = (2)

DN835, DN6835, DN6836



Note: DN6835, DN6836 V_{CC} = (1)
Output = only (3) GNG = (3)

DN839, DN6839



Note: DN6839 V_{CC} = (1), Output = only (3),
GND = (2)

Specifications subject to change without notice.

BBD (Bucket Brigade Devices)

Panasonic®
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BBD QUICK REFERENCE TABLE

	Item	Symbol	MN3001	MN3002	MN3003	MN3004	MN3005	MN3007	MN3007	MN3008	MN3009	MN3010	MN3011	MN3012	Unit
	Number of BBD	N	Dual-512	512	Dual-64	512	4096	128	1024	2048	256	Dual-512	3328 6-Tap	190, 3, 5 3-Tap	Stage
Circuit Construction	Clock Generator		External		Built-in	External								Built-in	
	Output Terminal				Pair								6 Different Taps	3 Different Taps	
Operating Conditions	Drain Supply Voltage	V_{DD}	−15		−9	−15	−15	−15	−15	−15	−15	−15	−15	−15	V
	Gate Supply Voltage	V_{GG}	−14		−8	−14	−14	−14	−14	−14	−14	−14	−14	−	V
	Back-Gate Bias Voltage	V_{BB}	+5		Not Needed										V
	Clock Voltage "H" Level	V_{CPH}	0		0	0	0~−1	0~−1	0~−1	0~−1	0~−1	0~−1	0~−1.3	−0~−0.4	V
	Clock Voltage "L" Level	V_{CPL}	−15		−9	−15	−15	−15	−15	−15	−15	−15	−15	−15	V
	Input DC Bias	V_{Bias}	−3.3 ~ −4.9		−2.5~−6	−5~−10	−5~−10	−5~−10	−5~−10	−5~−10	−5~−10	−5~−10	−	−3~−12	V
Electrical Characteristics	Input Signal Frequency	fi	12				10	12			14	12	10	12	kHz (max.)
	Input Signal Swing	Vi	1.8		0.8	1.8	1.2	1.8	1.5	1.5	1.7	1.8	1.0	1.2	Vrms (max.)
	Insertion Loss	Li	8.5		3.5	1.5	0	0	0	0	0	0	0	0	dB (typ.)
	Total Harmonic Distortion	THD	0.4		0.5	0.4	1	0.2	0.5	0.5	0.3	0.4	0.4	0.4	% (typ.)
	Noise Voltage	Vno	250 (typ.)		140	210	400	200	300	300	150	210	0.4	0.14	μVrms (max.)
	Signal to Noise Ratio	S/N	70		75	85	75	90	80	78	88	85	76	OUT1=90 OUT2=97 OUT3=98	dB (typ.)
	Signal Delay Time	tD	51.2	25.6	6.4	25.6	204.8	6.4	51.2	102.4	12.8	51.2	t_{D1}=19.8/33.1 59.7/86.3 139.5/166.4	0.475~9.5 0.0125~0.25 0.0075~0.15	msec (max.)
Package (Molded Package)			14-Pin DIP				Larger 8-Pin DIP	8-Pin DIP		Larger 8-Pin DIP	8-Pin DIP	14-Pin DIP	12-Pin DIP	14-Pin DIP	

SP8612B

1800MHz ÷ 4

The SP8612B is an asynchronous emitter coupled logic counter which provides ECL 10K compatible outputs and can drive 100 ohm lines. They operate from a -6.8V or +5, -1.8V supply but are otherwise similar to the SP8610 and 8611.

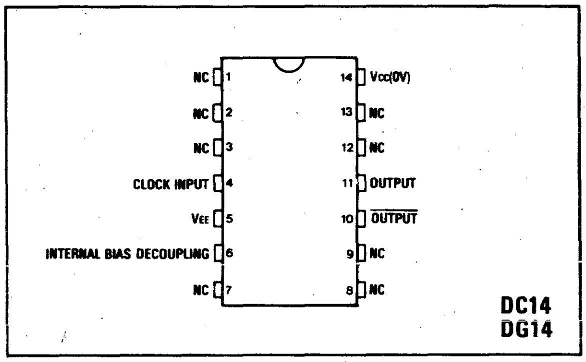

Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Output
- AC Coupled Input (Internal Bias)
- Typical Operating Frequency 2GHz

QUICK REFERENCE DATA

- Supply Voltage: -6.8V
- Power Consumption: 500mW
- Output Voltage Swing: 60mV typ.

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: (V_{CC}-V_{EE}) 8V
- Output Current: 15mA
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +150°C
- Max. Input Voltage: 2.5V p-p

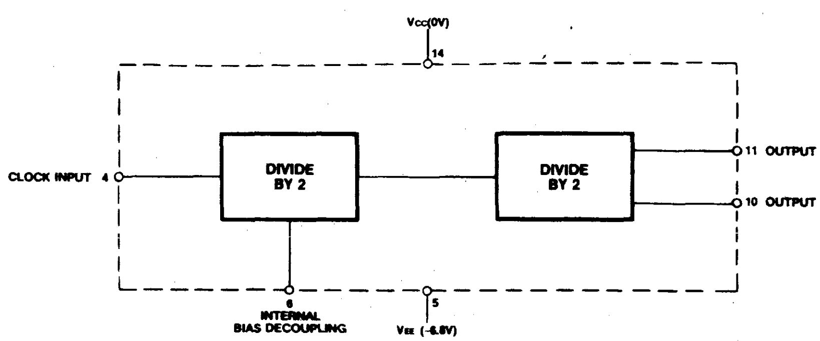

Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V, V_{EE} =-6.8V ± 0.25V
Temperature: T_{amb} = 0°C to +70°C

Characteristics	Symbol	Value Min.	Value Max.	Units	Conditions	Temperature
Maximum frequency sinewave input	f_{max}	1.8		GHz	Input = 800-1200mV p-p	As specified
Minimum frequency sinewave input	f_{min}		900	MHz	Input = 400-1200mV p-p	As specified
Power supply current	I_{EE}		110	mA	Outputs unloaded V_{EE} = -7.15V	As specified
Output low voltage	V_{OL}	-1.9	-1.62	V	Outputs loaded with 620Ω to V_{EE} = -6.8V	25°C
Output high voltage	V_{OH}	-0.93	-0.75	V	Outputs loaded with 620Ω to V_{EE} + -6.8V	25°C
Minimum output swing	V_{OUT}	500		mV	Outputs loaded with 620Ω to V_{EE} = -6.8V	As specified

NOTES
1. Unless otherwise stated, the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of V_{OH} = +1.2mV/°C and V_{OL} = +0.24mV/°C.
3. The test configuration for dynamic testing is shown in Fig. 5.

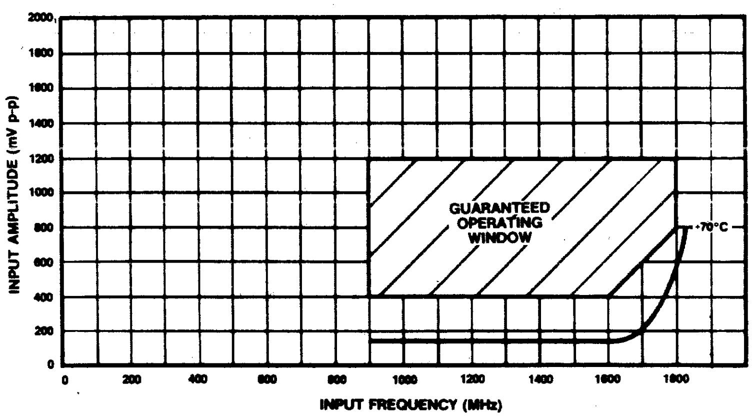

Fig.3 Typical input characteristics SP8612B

OPERATING NOTES

1. The clock input (pin 4) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 6 to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 10k resistor from the input to V_{EE} (i.e. pin 4 to pin 7). This reduces sensitivity by approximately 100mV.
3. The input can be operated at very low frequencies but slew rate must be better than 200V/µs.
4. The input impedance of the SP8612 is a function of frequency. See Fig. 4.
5. The emitter follower outputs require external load resistors. These should not be less than 330 ohms, and a value of 620 ohms is recommended. Interfacing to ECL III/10K is shown in Fig. 7.
6. These devices may be used with split supply lines by means of the circuit of Fig. 6. Some improvement in the upper frequency of operation may be obtained under these conditions, but suitable circuit layout must be employed to achieve this improvement.

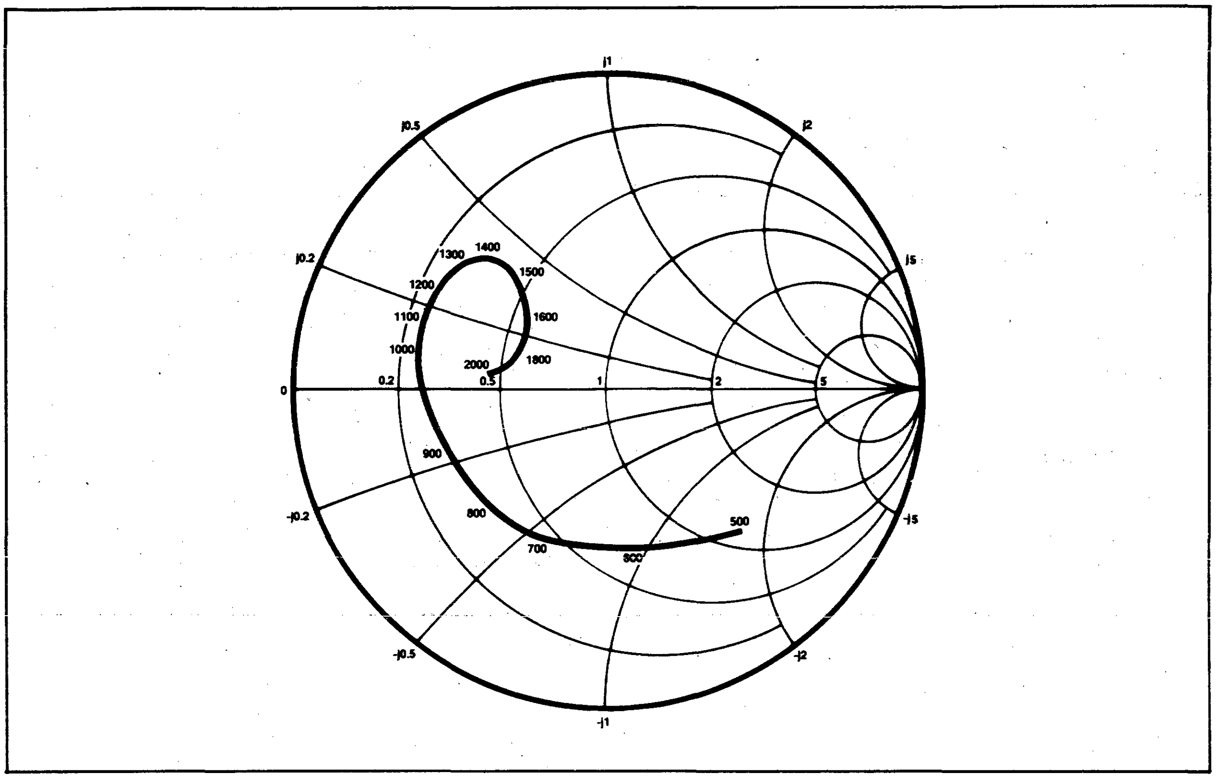

Fig.4 Typical input impedance. Test conditions: supply voltage .6.8V, ambient temperature 25° C. Frequencies in MHz, impedances normalised to 50 ohms.

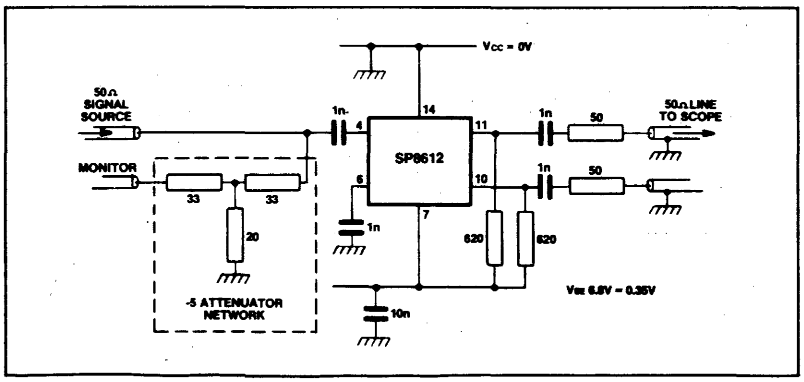

Fig.5 Toggle frequency test circuit

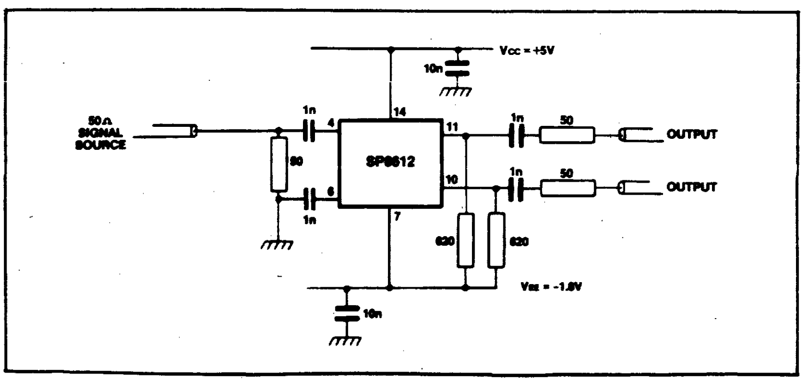

Fig.6 Operation on split supply voltages

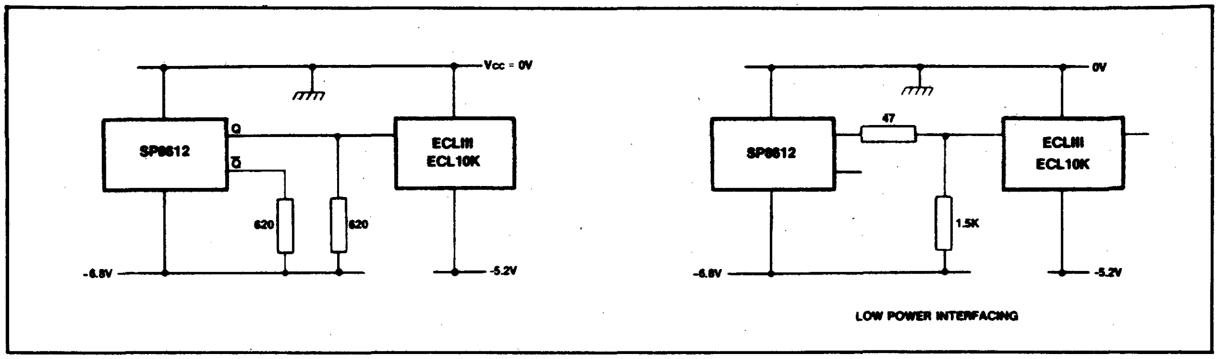

Fig.7 Interfacing SP8612 series to ECL 10K and ECL III

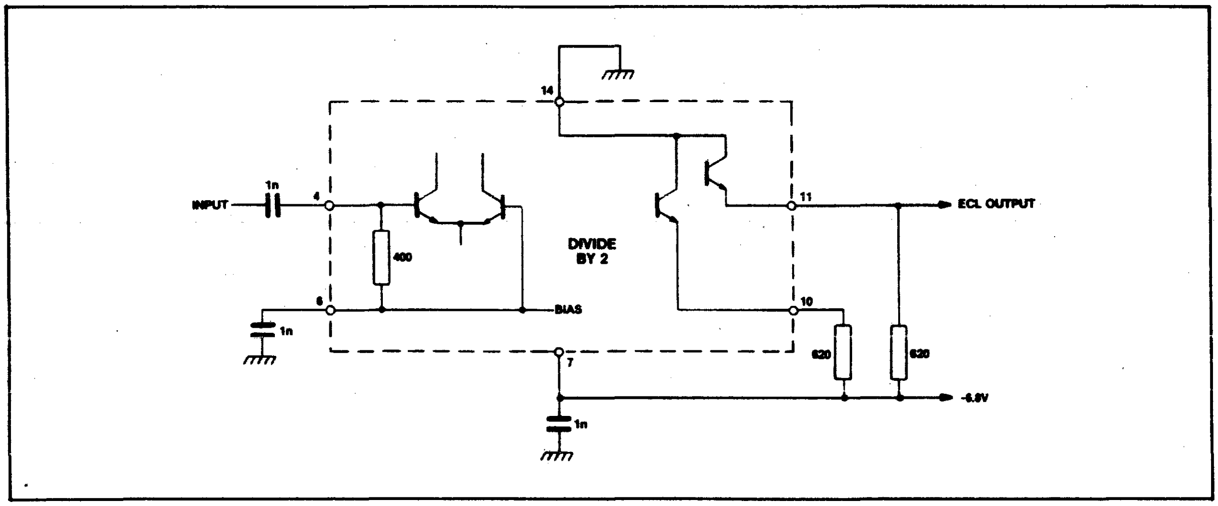

Fig.8 Typical application showing interfacing

LINEAR AND CONVERSION PRODUCTS FROM PMI

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Sample-and-Hold Amplifiers
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Applications range from instrumentation, data acquisition and process control to telecommunications and military/aerospace equipment.

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PMI Precision Monolithics Incorporated

OPERATIONAL —AMPLIFIERS

SELECTION GUIDE

The Operational Amplifier Selection Guide chart highlights PMI's line of operational amplifiers. The matrix indicates the most essential parametric differences for each product group.

"General Purpose" op amps are usually the least expensive and are recommended for applications where impedance levels are relatively low, closed-loop gain is low, and speed requirements are moderate. BIFET inputs provide lower input-bias-currents and better bandwidth than standard bipolar inputs, but input voltage offsets and noise are generally better for the bipolar input amplifiers.

The "High Accuracy" category presents the best amplifiers for high-gain applications. A combination of low input-offset-voltage, high open-loop gain, and high CMRR provide excellent DC accuracy even at high closed-loop gain. The OP-27/37 are best for minimum input voltage noise. The OP-08/12 provide an excellent combination of low input-bias-current, low offset voltage, and moderate power drain. The OP-07 offers a selection of the lowest offset voltages (60μV max to 250μV max) combined with low input-bias-current ($\pm$2nA max to $\pm$12nA max) and has become an industry standard for high-precision applications.

PMI is a leader in op amps featuring low power consumption. The OP-20/21/22 are micropower op amps that operate with only a few microamps of supply drain. PSRR and CMRR are high, and the input-voltage-range is wide. Such features work together to make these amplifiers ideal for battery-powered applications or for operation from a single supply voltage. The OP-22 can be programmed to operate over any supply current from 1μA to 400μA and is excellent for battery-powered designs.

	General Purpose						Precision High Speed BIFET Input			High Accuracy				Low Power Low Input Bias Current		Micropower						
	Bipolar				BIFET																	
Monolithic Technology	OP-01	OP-02	OP-04, OP-14	OP-09, OP-11	PM-155	PM-156, PM-157	OP-15	OP-16, OP-17	OP-215	OP-05, OP-06, OP-07	OP-08, OP-12	OP-27, OP-37	OP-207, OP-227	PM-108	PM-2108	OP-20	OP-21	OP-22, OP-32	OP-220	OP-221	OP-420	OP-421
Bipolar Input	●	●	●	●						●	●	●	●	●	●	●	●	●	●	●	●	●
BIFET					●	●	●	●	●													
Packages																						
Single	●	●			●	●	●	●		●	●	●		●		●	●	●				
Dual			●						●				●		●				●	●		
Quad				●																	●	●
Low Offset, $V_{OS} \leq$ 1mV	●			●			●	●	●	●	●	●	●			●	●	●	●	●		
Low Bias Current																						
$I_B <$ 100pA					●	●																
$I_B <$ 2nA							●	●	●		●			●	●							
High Gain, $A_{VOL} \geq$ 200,000										●		●	●			●	●	●	●	●	●	
High Slew Rate, SR $\geq$ 10V/μs	●					●		●				●										
Low Power																						
$I_{SY} \leq$ 1mA/Amplifier											●			●	●		●			●		●
$I_{SY} \leq$ 100μA/Amplifier																●		●	●		●	

PMI Precision Monolithics Incorporated

D/A CONVERTERS

SELECTION GUIDE

PMI offers a complete line of digital-to-analog converters (DACs), all which are guaranteed to be monotonic over their operating temperature ranges, and some which have become industry standards. The DACs have been arranged in a matrix which highlights their primary characteristics so that the user can easily narrow the selection according to specific requirements. More detailed specifications are then tabulated in each product group.

	Voltage Output						Current Output								
												μP Comp		Companding	
Resolution	DAC-01	DAC-02, DAC-03	DAC-05	DAC-06	DAC-208	DAC-210	DAC-08	DAC-10	DAC-20	DAC-100	DAC-312	DAC-808	DAC-888	DAC-86	DAC-88, DAC-89
6-Bits	●														
8-Bits					●		●		●			●	●	●	●
10-Bits		●	●	●		●		●		●					
12-Bits											●				
Input Coding															
BCD									●						
Binary							●	●			●	●	●		
Complementary Binary	●									●					
Sign Magnitude		●	●		●	●									
Companding														●	●
Two's Complement				●											
Complementary Current Outputs							●	●	●		●	●	●		
Internal Reference	●	●	●	●	●	●				●					
Logic Threshold Control							●	●	●		●			●	●
JAN Qualified							●								
Operating Temp. Range															
Military	●		●	●	●	●	●	●		●	●	●	●		
Industrial										●		●		●	●
Commercial	●	●	●	●	●	●	●	●	●	●	●	●	●	●	

LINEAR

Precision Monolithics

PMI Precision Monolithics Incorporated

AMP-01

LOW-NOISE PRECISION INSTRUMENTATION AMPLIFIER

PRELIMINARY

FEATURES

- **Low Offset Voltage** **15μV**
- **Very Low Offset Voltage Drift** .... **0.1μV/°C**
- **Low Noise** .... **$0.2\mu V_{p\text{-}p}$ (0.1Hz to 10Hz)**
- **Excellent Output Drive** .... **±10V at ±50mA**
- **Capacitive Load Stability** .... **to 1μF**
- **Gain Range** .... **0.1 to 10,000**
- **Excellent Linearity** .... **16-Bit at G = 1000**
- **High CMR** .... **140dB (G = 1000)**
- **Low Bias Current** **1nA**
- **May be Configured as a Precision Op-Amp**
- **Output-Stage Thermal Shutdown**

GENERAL DESCRIPTION

The AMP-01 is a monolithic instrumentation amplifier designed for high-precision data acquisition and general instrumentation applications. The design combines the conventional features of an instrumentation amplifier with a high-current output stage. The output remains stable with high capacitance loads (1μF), a unique ability for an instrumentation amplifier. Consequently, the AMP-01 can amplify low-level signals for transmission through long cables without requiring an output buffer. The output stage may be configured as a voltage or current generator.

Input offset voltage is very low (15μV) which generally eliminates the need for an external null potentiometer. Temperature changes have minimal effect on offset; TCV_{IOS} is typically 0.1μV/°C. Excellent low-frequency noise performance is achieved with a minimal compromise on input protection. Bias current is very low, less than 10nA over the industrial temperature range.

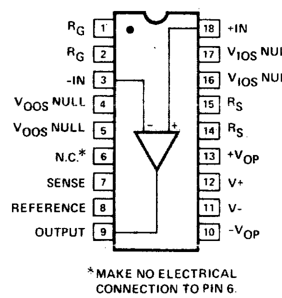
ORDERING INFORMATION†

PACKAGE CERDIP 18-PIN	OPERATING TEMPERATURE RANGE
AMP01AX*	MIL
AMP01BX*	MIL
AMP01EX	IND
AMP01FX	IND

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. Screening Procedure: 1984 Data Book, Section 3.

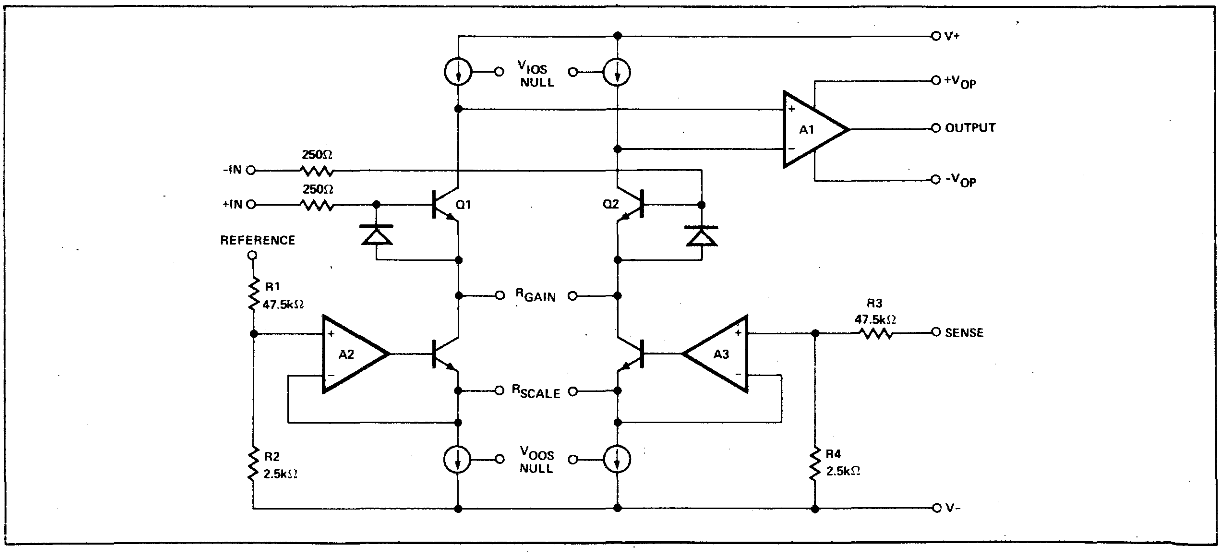
†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. Ordering Information: 1984 Data Book, Section 2.

PIN CONNECTIONS



18-PIN HERMETIC DIP (X-Suffix)

SIMPLIFIED SCHEMATIC



The premium performance of this product is achieved through an advanced processing technology. All Precision Monolithics products are guaranteed to meet or exceed published specifications. Patents applied for. Technical Specifications November 1983

PMI Precision Monolithics Incorporated

LOW-NOISE, MATCHED DUAL MONOLITHIC TRANSISTOR

MAT-02

PRELIMINARY

FEATURES

- **Low Offset Voltage** .... **50μV Max**
- **Low Noise Voltage at 100Hz** .... **1.8nV/$\sqrt{Hz}$ Typ**
- **High Gain (h_{FE})** .... **500 Min at I_C = 1mA**
  .... **300 Min at I_C = 1μA**
- **Excellent Log Conformance** .... **$r_{BE} \simeq 0.3\Omega$**

ORDERING INFORMATION

T_A = 25°C V_{OS} Max (μV)	PACKAGE	OPERATING TEMPERATURE RANGE
50	MAT02AH*	MIL
50	MAT02EH	IND
150	MAT02BH*	MIL
150	MAT02FH	IND

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. Screening Procedure: 1984 Data Book, Section 3.
†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. Ordering Information: 1984 Data Book, Section 2.

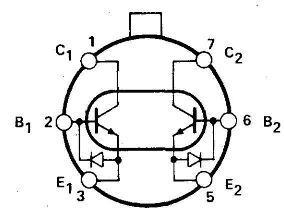
GENERAL DESCRIPTION

The design of the MAT-02 series of NPN dual monolithic transistors is optimized for very low noise, low drift, and low r_{BE}. Precision Monolithics' exclusive Silicon Nitride "Triple-Passivation" process stabilizes the critical device parameters over wide ranges of temperature and elapsed time. Also, the high current gain (h_{FE}) of the MAT-02 is maintained over a wide range of collector current. Exceptional characteristics of the MAT-02 include offset voltage of 50μV max (A/E grades) and 150μV max (B/F grades). Device performance is specified over the full military temperature range as well as at 25°C.

Input protection diodes are provided across the emitter-base junctions to prevent degradation of the device characteristics due to reverse-biased emitter current. The substrate is clamped to the most negative emitter by the parasitic isolation junction created by the protection diodes. This results in isolation between the transistors.

The MAT-02 should be used in any application where low noise is a priority. The MAT-02 can be used as an input stage to make an amplifier with noise voltage of less than 2.0nV/$\sqrt{Hz}$ at 100Hz. Other applications, such as log/antilog circuits may use the excellent logging conformity of the MAT-02. Typical excess emitter resistance is only 0.3Ω to 0.4Ω. The MAT-02 electrical characteristics approach those of an ideal transistor when operated over a collector current range of 1μA to 10mA.

PIN CONNECTIONS



TO-78
(H-Suffix)

NOTE: Substrate is connected to case. Substrate potential is held at one V_{BE} above the most negative emitter potential.

ELECTRICAL CHARACTERISTICS at V_{CB} = 15V, I_C = 10μA, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-02A/E MIN	MAT-02A/E TYP	MAT-02A/E MAX	MAT-02B/F MIN	MAT-02B/F TYP	MAT-02B/F MAX	UNITS
Offset Voltage	V_{OS}	I_C = 10μA	—	—	50	—	—	150	μV
Bias Current	I_B	I_C = 10μA	—	—	33	—	—	50	nA
Offset Current	I_{OS}	I_C = 10μA	—	—	0.6	—	—	2	nA
Current Gain	h_{FE}	I_C = 1mA	500	—	—	400	—	—	
		I_C = 100μA	500	—	—	400	—	—	
		I_C = 10μA	400	—	—	300	—	—	
		I_C = 1μA	300	—	—	200	—	—	
Current Gain Match	h_{FE} Match	10μA ≤ I_C ≤ 1mA	—	—	2	—	—	4	%
Excess Emitter Resistance	r_{BE}		—	0.3	0.5	—	0.3	0.5	Ω
Noise Voltage	e_n	I_C = 100μA, f = 100Hz	—	1.8	—	—	1.8	—	nV/$\sqrt{Hz}$
Collector Base Voltage	V_{CB}		—	—	40	—	—	40	V

The premium performance of this product is achieved through an advanced processing technology. All Precision Monolithics products are guaranteed to meet or exceed specifications.

 Technical Specifications November 1983

PMI Precision Monolithics Incorporated

OP-32

HIGH-SPEED PROGRAMMABLE MICROPOWER OPERATIONAL AMPLIFIER (SINGLE OR DUAL SUPPLY)

PRELIMINARY

FEATURES

- **Programmable Supply Current .... 1μA to 2mA**
- **Single Supply Operation .... +3V to +30V**
- **Dual Supply Operation .... ±1.5V to ±15V**
- **Low Input Offset Voltage 100μV**
- **Low Input Offset Voltage Drift .... 0.75μV/°C**
- **High Common-Mode Input Range ... V− to V+ (−1.5V)**
- **High CMRR and PSRR 115dB**
- **High Open-Loop Gain 2000V/mV**
- **±30V Input Overvoltage Protection**
- **Fast .... 1V/μs @ I_{SET} = 20μA**
- **LM4250 Pinout**
- **Compensated for Minimum Gain of 10**

GENERAL DESCRIPTION

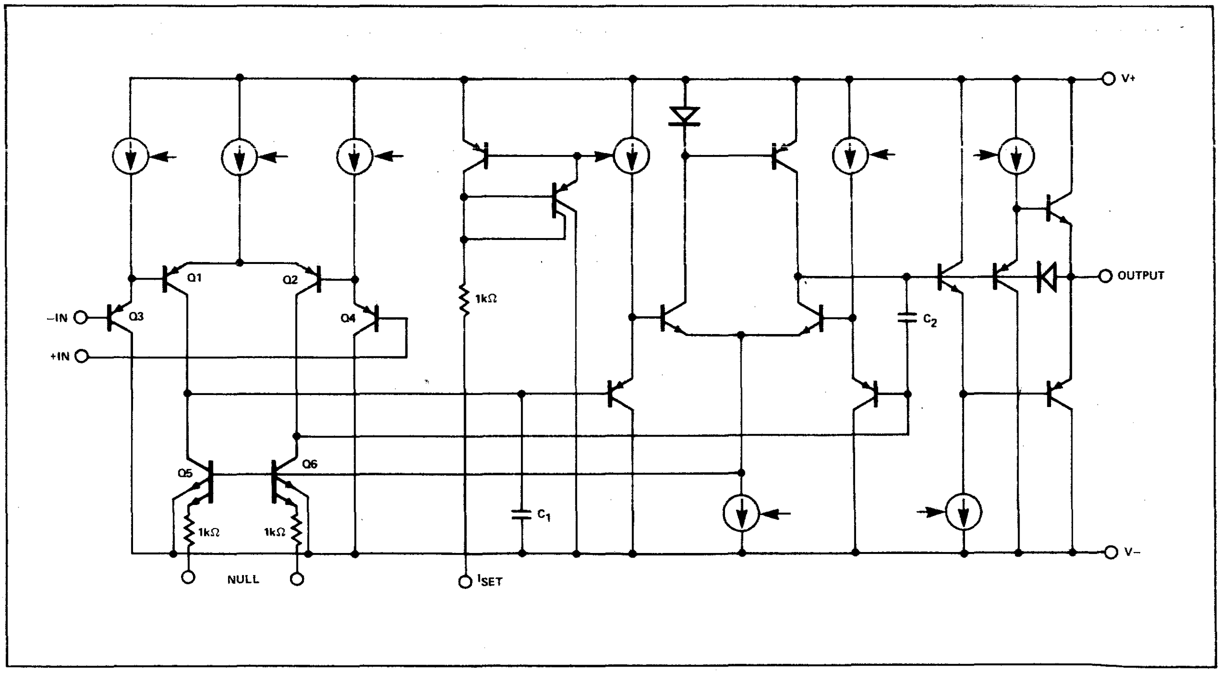
The OP-32 is a high-speed, high-gain programmable operational amplifier. Both offset voltage and offset current are low, and both are stable with changes in temperature, supply voltage, and set current. High CMRR and PSRR ensure precision performance when the OP-32 is used with an unregulated battery or vehicular electrical systems.

The wide input voltage range, including the negative supply or ground, allows use in single-battery applications. The OP-32 is characterized over a wide supply range of ±1.5V to ±15V. This guarantees predictable performance with any commonly available supply.

The ability to operate at relatively high speed with low power consumption makes this amplifier ideal for remote applications where power is limited. The programmability allows each amplifier in a system to be set for the minimum power consumption necessary for each specific application. Programmability also makes it possible to adjust the bandwidth and phase shift.

The OP-32 pinout is identical to the LM4250 and many other micropower operational amplifiers. This allows easy upgrading of system performance.

SIMPLIFIED SCHEMATIC



The premium performance of this product is achieved through an advanced processing technology. All Precision Monolithics products are guaranteed to meet or exceed published specifications.

 Technical Specifications November 1983

Precision Monolithics Incorporated

OP-32 HIGH-SPEED PROGRAMMABLE MICROPOWER OPERATIONAL AMPLIFIER — PRELIMINARY

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage .... ±18V
Power Dissipation 500mW
Differential Input Voltage .... ±30
Input Voltage .... Supply Voltage
Storage Temperature Range
  Z Package .... −65°C to +150°C
  P Package .... −55°C to +125°C

Operating Temperature Range
  OP-32A, B (Z package) .... −55°C to +125°C
  OP-32E, F & G (Z or P package) ...... −25°C to +85°C
Lead Temperature Range (Soldering, 60 sec) ...... 300°C
DICE Junction Temperature .... −65°C to +150°C

NOTE:
1. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V_S = ±1.5V to ±15V, 1μA ≤ I_{SET} ≤ 30μA, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-32A/E MIN	OP-32A/E TYP	OP-32A/E MAX	OP-32B/F MIN	OP-32B/F TYP	OP-32B/F MAX	OP-32G MIN	OP-32G TYP	OP-32G MAX	UNITS
Input Offset Voltage	V_{OS}		—	100	300	—	200	500	—	400	1000	μV
Input Offset current	I_{OS}	V_{CM} = 0	—	0.2	1	—	0.3	2	—	0.5	3	nA
Input Bias Current (Note 1)	I_B	I_{SET} = 1μA	—	2.6	5	—	3.0	7.5	—	4.0	10	nA
		I_{SET} = 10μA	—	19	30	—	24	35	—	30	50	
		I_{SET} = 30μA	—	45	75	—	50	100	—	60	125	
Input Voltage Range	IVR	V_S = ±15V	-15.0/13.5	—	—	-15.0/13.5	—	—	-15.0/13.5	—	—	V
Common-Mode Rejection Ratio	CMRR	V_S = ±15V, −15V ≤ V_{CM} ≤ +13.5V	100	115	—	95	110	—	85	100	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±1.5V to ±15V; and V− = 0V, V+ = 3V to 30V.	—	1	6	—	3	12	—	10	25	μV/V
Large-Signal Voltage Gain	A_{VO}	V_S = ±15V, R_L = 100kΩ, R_L = 10kΩ, 10μA ≤ I_{SET} ≤ 30μA	1000	2000	—	750	1500	—	500	1000	—	V/mV
Output Voltage Swing	V_O	V_S = ±1.5V, R_L = 100kΩ, I_{SET} = 1μA, R_L = 10kΩ, 10μA ≤ I_{SET} ≤ 30μA	±0.8	±0.88	—	±0.8	±0.88	—	±0.75	±0.85	—	V
		V_S ±15V, R_L = 100kΩ, I_{SET} = 1μA, R_L = 10kΩ, 10μA ≤ I_{SET} ≤ 30μA	±14	±14.2	—	±14	±14.2	—	±13.8	±14.2	—	V
Gain-Bandwidth Product		I_{SET} = 1μA, R_L = 100kΩ	—	100	—	—	100	—	—	100	—	kHz
		I_{SET} = 30μA, R_L = 10kΩ	—	4500	—	—	4500	—	—	4500	—	
Slew Rate	SR	V_S = ±15V, I_{SET} = 10μA, R_L = 10kΩ	—	0.6	—	—	0.6	—	—	0.6	—	V/μs
Supply Current No Load	I_{SY}	V_S = ±15V, I_{SET} = 1μA	—	15	17	—	15	19	—	15	21	μA
		I_{SET} = 10μA	—	150	170	—	150	190	—	150	200	
		I_{SET} = 30μA	—	450	525	—	450	600	—	450	650	
		V_S = ±1.5V, I_{SET} = 1μA	—	10.5	12.5	—	11	15	—	11	18	
		I_{SET} = 10μA	—	105	125	—	110	150	—	110	180	
		I_{SET} = 30μA	—	350	400	—	350	450	—	350	500	

NOTE:
1. I_B and I_{OS} are measured at V_{CM} = 0.

LINEAR

Precision Monolithics

PMI Precision Monolithics Incorporated

OP-32 HIGH-SPEED PROGRAMMABLE MICROPOWER OPERATIONAL AMPLIFIER — PRELIMINARY

ELECTRICAL CHARACTERISTICS at $V_S = \pm1.5V$ to $\pm15V$, $1\mu A \leq I_{SET} \leq 30\mu A$, $-55°C \leq T_A \leq +125°C$ for OP-32AZ and OP-32BZ, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-32A MIN.	OP-32A TYP	OP-32A MAX	OP-32B MIN	OP-32B TYP	OP-32B MAX	UNITS
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	Unnulled	—	0.75	2.0	—	1.0	2.0	μV/°C
Input Offset Voltage	V_{OS}		—	175	400	—	350	600	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.2	1	—	0.3	2	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 1)	—	1	10	—	3	15	pA/°C
Input Bias Current (Note 2)	I_B	$I_{SET} = 1\mu A$	—	2.8	5	—	3.3	7.5	nA
		$I_{SET} = 10\mu A$	—	21	30	—	27	35	
		$I_{SET} = 30\mu A$	—	40	75	—	50	100	
Input Voltage Range	IVR	$V_S = \pm15V$	−15.0/13.5	—	—	−15.0/13.5	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_S = \pm15V$, $-15V \leq V_{CM} \leq +13.5V$	90	110	—	86	105	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm1.5V$ to $\pm15V$ & $V- = 0V$, $V+ = 3V$ to $30V$	—	2	10	—	2.5	20	μV/V
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm15V$, $R_L = 100k\Omega$	200	400	—	200	500	—	V/mV
		$R_L = 10k\Omega$, $10\mu A \leq I_{SET} \leq 30\mu A$	500	1000	—	300	750	—	
Output Voltage Swing	V_O	$V_S = \pm1.5V$, $R_L = 100k\Omega$, $I_{SET} = 1\mu A$; $R_L = 10k\Omega$, $10\mu A \leq I_{SET} \leq 30\mu A$	±0.65	±0.75	—	±0.65	±0.75	—	V
		$V_S = \pm15V$, $R_L = 100k\Omega$, $I_{SET} = 1\mu A$; $R_L = 10k\Omega$, $10\mu A \leq I_{SET} \leq 30\mu A$	±13.6	±14.0	—	±13.0	±13.5	—	V
Supply Current No Load	I_{SY}	$V_S = \pm15V$, $I_{SET} = 1\mu A$	—	16	18	—	16	20	μA
		$I_{SET} = 10\mu A$	—	160	180	—	160	200	
		$I_{SET} = 30\mu A$	—	450	550	—	450	600	
		$V_S = \pm1.5V$, $I_{SET} = 1\mu A$	—	12	14	—	12	17	
		$I_{SET} = 10\mu A$	—	120	140	—	120	170	
		$I_{SET} = 30\mu A$	—	360	450	—	360	500	

NOTE:
1. Sample tested.
2. I_B and I_{OS} are measured at $V_{CM} = 0$.

LINEAR

Precision Monolithics

PMI Precision Monolithics Incorporated

OP-32 HIGH-SPEED PROGRAMMABLE MICROPOWER OPERATIONAL AMPLIFIER — PRELIMINARY

ELECTRICAL CHARACTERISTICS at $V_S = \pm1.5V$ to $\pm15V$, $1\mu A \le I_{SET} \le 30\mu A$, $-25°C \le T_A \le +85°C$ for OP-32EP/EZ, OP-32FP/FZ, OP-32GP and OP-32GZ, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-32E MIN	OP-32E TYP	OP-32E MAX	OP-32F MIN	OP-32F TYP	OP-32F MAX	OP-32G MIN	OP-32G TYP	OP-32G MAX	UNITS
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	Unnulled	—	0.75	1.5	—	1.0	2.0	—	1.5	3.0	μV/°C
Input Offset Voltage	V_{OS}		—	100	300	—	200	600	—	500	1200	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.2	1	—	0.3	2	—	0.5	3	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 1)	—	2	10	—	3	15	—	5	25	pA/°C
Input Bias Current (Note 2)	I_B	$I_{SET} = 1\mu A$ $I_{SET} = 10\mu A$ $I_{SET} = 30\mu A$	— — —	2.6 19 45	5 30 75	— — —	3.0 24 50	7.5 35 100	— — —	4.0 30 60	10 50 125	nA
Input Voltage Range	IVR	$V_S = \pm15V$	−15.0/13.5	—	—	−15.0/13.5	—	—	−15.0/13.5	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_S = \pm15V$ & $-15V \le V_{CM} \le +13.5V$	95	110	—	90	105	—	80	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm1.5V$ to $\pm15V$ & $V- = 0V$, $V+ = 3V$ to $30V$	—	3.2	10	—	10	32	—	32	56	μV/V
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm15V$ $R_L = 100k\Omega$ $R_L = 10k\Omega$, $10\mu A \le I_{SET} \le 30\mu A$	 750 750	 1000 1000	 — —	 500 500	 1200 1200	 — —	 400 400	 1000 1000	 — —	V/mV
Output Voltage Swing	V_O	$V_S = \pm1.5V$ $R_L = 100k\Omega$, $I_{SET} = 1\mu A$ $R_L = 10k\Omega$, $10\mu A \le I_{SET} \le 30\mu A$	±0.70	±0.75	—	±0.65	±0.75	—	±0.6	±0.7	—	V
		$V_S = \pm15V$ $R_L = 100k\Omega$, $I_{SET} = 1\mu A$ $R_L = 10k\Omega$, $10\mu A \le I_{SET} \le 30\mu A$	±13.8	±14.1	—	±13.6	±14.1	—	±13.0	±14.0	—	V
Supply Current No Load	I_{SY}	$V_S = \pm15V$, $I_{SET} = 1\mu A$ $I_{SET} = 10\mu A$ $I_{SET} = 30\mu A$ $V_S = \pm1.5V$, $I_{SET} = 1\mu A$ $I_{SET} = 10\mu A$ $I_{SET} = 30\mu A$	— — — — — —	16 160 450 12 120 360	18 180 550 14 140 450	— — — — — —	16 160 450 12 120 360	20 200 600 17 170 500	— — — — — —	16 160 450 12 120 360	25 250 650 25 200 550	μA

NOTE:
1. Sample tested.
2. I_B and I_{OS} are measured at $V_{CM} = 0$.

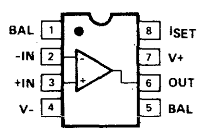
ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} MAX (μV)	PACKAGE EPOXY DIP 8-PIN	PACKAGE HERMETIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
300	OP32AP	OP32AZ*	MIL
300	OP32EP	OP32EZ	IND
500	OP32BP	OP32BZ*	MIL
500	OP32FP	OP32FZ	IND
1000	OP32GP	OP32GZ	IND

*Also available with MIL-STD-883B Processing. To order add /883 as a suffix to the part number. Screening Procedure: 1984 Data Book, Section 3.

†All commercial and industrial temperature range parts are available with burn-in per MIL-STD-883. Ordering Information: 1984 Data Book, Section 2.

PIN CONNECTIONS



8-PIN EPOXY DIP (P-Suffix)

8-PIN HERMETIC DIP (Z-Suffix)

SALES OFFICES

Headquarters, Factory and Regional Sales Offices

Santa Clara
1500 Space Park Dr.
Santa Clara, CA 95050
(408) 727-6616
TWX 910-338-2102

Los Angeles
6033 W. Century Blvd., Suite 595
Los Angeles, CA 90045
(213) 642-0124
TWX 910-328-6591

Chicago
1325 Remington Rd., Suite "D"
Schaumburg, IL 60195
(312) 885-8440, (800) 323-8755
TWX 910-222-1808

Dallas
11325 Pegasus St., Suite W-126
Dallas, TX 75238
(214) 341-1742, (800) 323-8755
TWX 910-861-4079

Boston
209 W. Central St.
Natick, MA 01760
(617) 655-8900
TWX 710-386-0114

Europe

Headquarters
Bourns/PMI
Zugerstrasse 74
6340 Baar
Switzerland
Phone: 042-33 33 33
Telex: 868 722

Benelux
Bourns (Nederland) B.V.
Van Tuyl van Serooskerkestr. 85
P.O. Box 37
2270 AA Voorburg
Phone: 070-87 44 00
Telex: 32 023

France
Ohmic SA
21/23 rue des Ardennes
75019 Paris
Phone: 01-203 96 33
Telex: 230 008

Germany
Bourns GmbH
Postfach 1155
Eberhardstrasse 63
7000 Stuttgart 1
Phone: 0711-24 29 36
Telex: 721 556

Switzerland
Bourns (Schweiz) AG
Zugerstrasse 74
6340 Baar
Phone: 042-33 33 33
Telex: 868 722

United Kingdom
Bourns Electronics Ltd.
Hodford House
17/27 High Street
Hounslow, Middlesex TW3 1TE
Phone: 01-572 65 31
Telex: 264 485

Japan

Nippon PMI Corporation
Haratetsu Building
4-1-11, Kudan Kita
Chiyoda-ku, Tokyo
Phone: (03) 234-1141
Telex: 781 J 27632

PMI Precision Monolithics Incorporated

RAYTHEON

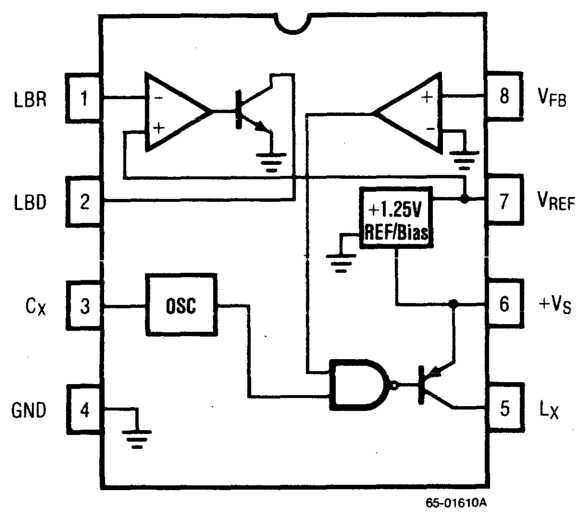
Inverting Switching Regulator

4391

Features

- Converts a Positive Voltage into a Negative Voltage
- Specifically Designed for Low Power Applications, Including Batteries
- Adjustable Output Voltage
- High Switch Current Capability
- Low Quiescent Supply Current — 175µA Typical
- Eight Pin Mini Package
- Low Battery Detection Circuitry

Functional Block Diagram



Thermal Characteristics

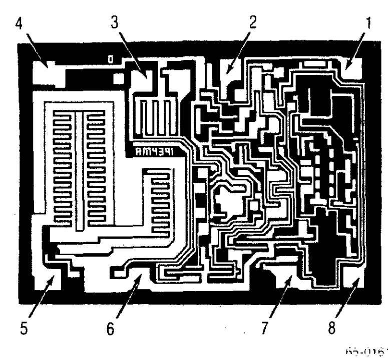
	8-Lead Plastic DIP	8-Lead Ceramic DIP
Max. Junction Temp.	125°C	175°C
Max. P_D $T_A < 50°C$	468mW	833mW
Therm. Res. θ_{JC}		45°C/W
Therm. Res. θ_{JA}	160°C/W	150°C/W
For $T_A > 50°C$ Derate at	6.25mW per °C	8.33mW per °C

Description

Raytheon's micro-power inverting switching regulator, RM/RC4391, is a monolithic low power switching regulator specifically designed for low power inverting applications. The RC4391 contains an internal 1.25 Volt bandgap voltage reference, switch transistor, comparator, free running oscillator and low battery detection circuitry. These components are interconnected to minimize the number of external components required in typical inverting applications (see Figure 2). The RC4391 requires an inductor, diode, timing capacitor, and an R2, R1 network to achieve a negative output voltage. The RC4391 allows the designer the flexibility in designing unconventional applications such as replacing the internal bandgap reference with an external or system reference, or using the low battery detection comparator and transistor as voltage level detectors or for signal generation.

A typical application would combine the RC4391 with the RC4193 micro-power switching regulator to convert a single input voltage into a ±12 Volt or ±15 Volt power supply. The single voltage can be either from a battery, bridge rectifier or existing +5.0 Volt line on card for this application (see Figure 3).

Mask Pattern



Die Size: 69 x 50 mils
Min. Pad Dimensions: 4 x 4 mils

RAYTHEON COMPANY • Semiconductor Division • 350 Ellis Street • Mountain View, CA 94039-7016
(415) 968-9211 TWX: 910-379-6484

Electrical Characteristics (Circuit of Figure 2., V_{IN} = 6.0V, T_A = +25° C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage	V_{IN}		3.0		30-$\lvert V_{OUT}\rvert$	Volts
Supply Current	I_{IN}	V_S = 4.0V, No External Loads		170	250	μA
		V_S = 25V, No External Loads		300	500	
Output Voltage	V_{OUT}	$V_{OUT\ nom}$ = -5.0V	-5.35	-5.0	-4.65	Volts
		$V_{OUT\ nom}$ = -15V	-15.85	-15	-14.15	
Line Regulation		$V_{OUT\ nom}$ = -5.0V, C_X = 150pF, V_{IN} = 5.8V to 20V		1.5	3.0	% V_{OUT}
		$V_{OUT\ nom}$ = -15V, C_X =150pF, V_{IN} = 5.8V to 15V		1.0	2.0	
Load Regulation		$V_{OUT\ nom}$ = -5.0V, C_X = 350pF, V_{IN} = 4.5V, P_{LOAD} = 0mW to 75mW		0.2	0.4	% V_{OUT}
		$V_{OUT\ nom}$ = -15V, C_X = 350pF, V_{IN} = 4.5V, P_{LOAD} = 0mW to 75mW		0.07	0.14	
Reference Voltage	V_{REF}		1.18	1.25	1.32	Volts
Switch Current	I_{SW}	Pin 5 = 5.5V	75			mA
Switch Leakage Current	I_{CO}	Pin 5 = -24V		0.01	5.0	μA
Timing Pin Current	I_{CX}	Pin 3 = 0V	10	12	14	μA
LBD Leakage Current		Pin 1 = 1.5V, Pin 2 = 6.0V		0.01	5.0	μA
LBD on Current		Pin 1 = 1.1V, Pin 2 = 0.4V	210	600		μA
LBR Bias Current		Pin 1 =1.5V		0.7		μA

Electrical Characteristics

(Circuit of Figure 2., V_{IN} = 6.0V, over the full operating temperature range unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage	V_{IN}		4.0		30-$\lvert V_{OUT} \rvert$	Volts
Supply Current	I_{IN}	V_{IN} = 25V		300	500	μA
Reference Voltage	V_{REF}		1.13	1.25	1.36	Volts
Output Voltage	V_{OUT}	$V_{OUT\ nom}$ = -5.0V	-5.5	-5.0	-4.5	Volts
		$V_{OUT\ nom}$ = -15V	-16.5	-15	-13.5	
Line Regulation		$V_{OUT\ nom}$ = -5.0V, C_X = 150pF, V_{IN} = 5.8V to 20V		2.0	4.0	% V_{OUT}
		$V_{OUT\ nom}$ = -15V, C_X =150pF, V_{IN} = 5.8V to 15V		1.5	3.0	
Load Regulation		$V_{OUT\ nom}$ = -5.0V, C_X = 350pF, V_{IN} = 4.5V, P_{LOAD} = 0mW to 75mW		0.2	0.5	mV
		$V_{OUT\ nom}$ = -15V, C_X = 350pF, V_{IN} = 4.5V, P_{LOAD} = 0mW to 75mW		0.15	0.3	
Switch Leakage Current	I_{CO}	Pin 5 = -24V		0.1	30	μA

Principles of Operation

The basic switching inverter circuit is the building block on which the complete inverting application is based.

A simplified diagram of the voltage inverter circuit with ideal components and no feedback circuitry is shown in (Figure 1). When the switch S is closed, charging current from the battery flows through the inductor L, which builds up a magnetic field, increasing as the switch is held closed. When the switch is opened, the magnetic field collapses, and the energy stored in the magnetic field is converted into a current which flows through the inductor in the same direction as the charging current. Because there is no path for this current to flow through the switch, the current must flow through the diode to charge the capacitor C. The key to the inversion is the ability of the inductor to become a source when the charging current is removed.

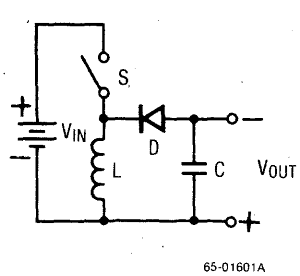
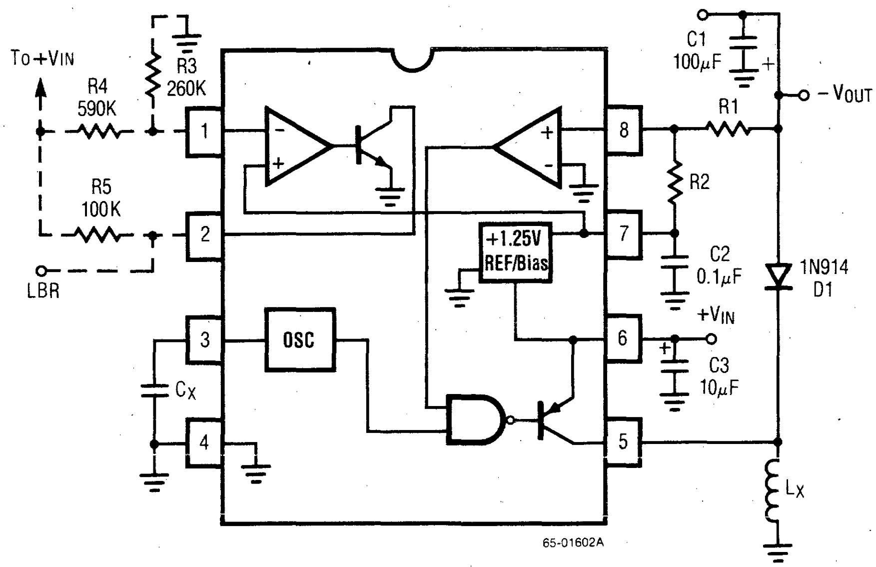


Figure 1. Simplified Voltage Inverter

The equation V = (L) (di/dt) gives the maximum possible voltage across the inductor; in the actual application, feedback circuitry and the output capacitor will decrease the output voltage to a regulated fixed value.

A complete schematic for the standard inverting application is shown in (Figure 3). The ideal switch in the simplified diagram is replaced by



Parts List	-5.0V Output	-15V Output
R1	30KΩ	90KΩ
R2	7.5KΩ	7.5KΩ
Cx	150PF	150PF
Lx	1.0mH Dale	TE3 Q4 TA

Optional

Figure 2. 4391 Standard Application Circuit

the PNP transistor switch between pins 5 and 6. C1 functions as the output filter capacitor, and D1 and L_X replace D and L.

When power is first applied, the ground sensing comparator (Pin 8) compares the output voltage to the +1.25V voltage reference. Because C1 is initially discharged a positive voltage is applied to the comparator, and the output of the comparator gates the square wave oscillator. This gated square wave signal turns on, then off, the PNP output transistor. This turning on and off of the output transistor performs the same function as opening and closing the ideal switch in the simplified diagram; i.e., it stores energy in the inductor during the on time and releases it into the capacitor during the off time.

The comparator will continue to gate the oscillator to the switch transistor until enough energy has been stored in the output capacitor to make the comparator input voltage decrease to less than zero volts. The voltage applied to the comparator is set by the output voltage, the reference voltage, and the ratio of R1 to R2. To adjust the output voltage, set R2 to about 10KΩ and change R1 according to the following equation:

$$R1 = \frac{(V_{OUT})\,(R2)}{V_{REF}}$$

Efficiency and load regulation will improve if a quality high Q inductor is used. A ferrite core toroid inductor is recommended. The inductor value and timing capacitor value must be carefully tailored to the ripple, input voltage range, output voltage, switch transistor maximum current, and output load current requirements of the application. The following equation will help select component, values for high output current at input voltages less than or equal to the output voltage.

$$I_{OUT\ (average)} \approx \frac{(V_{IN} - V_{SW})^2}{(L)\,(8.0)\,(f_O)\,(V_{OUT} + V_D)}$$

where L = Inductor Value in Henrys
f_O = Switching Frequency
V_{SW} = Saturation Voltage of Switching Transistor
V_D = Diode Voltage

The input voltage is a squared term; if the input voltage decreases, even by a small amount, the output current capability will decrease sharply. Since the L term is in the denominator, lower inductor values will increase the output current capability (until the inductor current rises so high that the inductor saturates — an air gapped core can help this). Lowering the switching frequency will also help, but will increase the ripple. Also, the frequency should not be so low that the inductor current rises too high and saturates the inductor or exceeds the maximum current rating of the switch transistor, which is 375 milliamps.

For $V_{IN} < |V_{OUT}|$

$$I_{MAX} \approx \frac{(V_{IN} - V_{SW})^2}{2 L f_O}$$

For $V_{IN} > |V_{OUT}|$

$$I_{MAX} \approx 2 \times I_{LOAD}$$

The value of the timing capacitor is set according to the following equation:

$$f_{OP}\,(Hz) = \frac{2.14 \times 10^{-6}}{C_X}$$

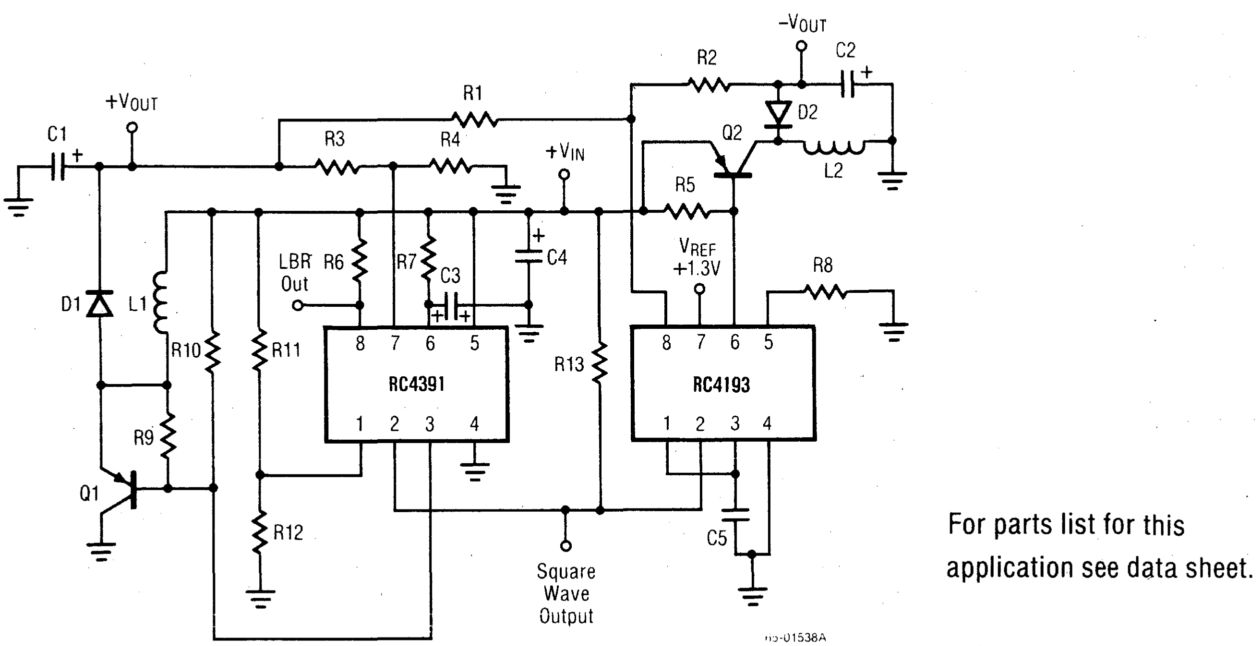
The square wave output of the oscillator is internal and cannot be directly measured, but is equal in frequency to the triangle waveform measurable at pin 3. The switch transistor is normally on when the triangle waveform is ramping up and off when ramping down. Capacitor selection depends on the application; higher operating frequencies will reduce the output voltage ripple while trading off efficiency and load regulation. Keep the capacitor lead length short.

The low battery detector provides a method of signaling a computer system or an LCD display when the battery voltage decays below a set voltage. This voltage is predetermined by a voltage divider tied to the battery input and by the +1.25V voltage reference:

$$V_{TH} = \left(\frac{R4}{R3} + 1.0\right) V_{REF}$$

The open collector output transistor must have an external load resistor selected according to the input drive requirement of the logic family used.

An inverting and non-inverting power supply circuit using a step up RC4193 and an inverting 4391 shown in (Figure 3). The component



For parts list for this application see data sheet.

Figure 3. RC4391/RC4193 Power Supply Schematic

values given will provide a positive 15 Volt output and a negative 15 Volt output. These voltages can be adjusted by changing the value of R1, $V_{OUT} = (R1/R2 + 1.0)(V_{REF})$, but note that the battery voltage must be less than the programmed positive output voltage. The reference for the negative output voltage is derived from the positive output voltage so that the output voltages will track with changes in temperature and battery voltage.

The inductor and timing capacitor values shown were chosen for best operation with a 12 Volt nominal battery input that decays to less than 8.0 Volts, with an output current of 60 milliamps and output ripple of less than 200 millivolts. The inductor value and timing should be adjusted for different applications (see the I_{OUT} equation). The maximum input voltage can be increased by adding a zener diode in series with the supply lead of each IC.

The oscillators are slaved together, using the low battery detection circuitry of the 4391, in order to reduce the electromagnetic interference that would otherwise be caused by having separate unsynchronized oscillator frequencies. The square wave output is available and can be used for other circuitry if the current drawn is low. Also available is the +1.25 Volt DC reference voltage (limit current to 100μA).

A circuit that allows higher input voltages and will deliver more power to the load than the standard application circuit is shown in (Figure 4). The circuit has an external switch transistor, Q1, with a higher maximum current rating than the internal switch transistor. Also, the optional zener diode D2 steps down the applied input voltage. If D2 is not used it should be shorted out.

The circuit operation is similar to that of the standard application circuit, except that the internal switch transistor now drives the base of the external transistor. Note that the on switch voltage will now equal the switch voltage of the internal transistor plus the V_{BE} of Q1. This higher switch voltage will reduce the circuits ability to supply output current with low input voltages. The external transistor circuit of (Figure 3) does not have this problem.

Note that even though the addition of the zener raises the maximum allowable supply voltage, it does not alter the maximum change of supply voltage, which equals the maximum supply voltage minus the minimum supply voltage (ΔV = 30V - 3.0V = 27V). So, with a 10V zener diode, the supply voltage range will be 13V to 40V.

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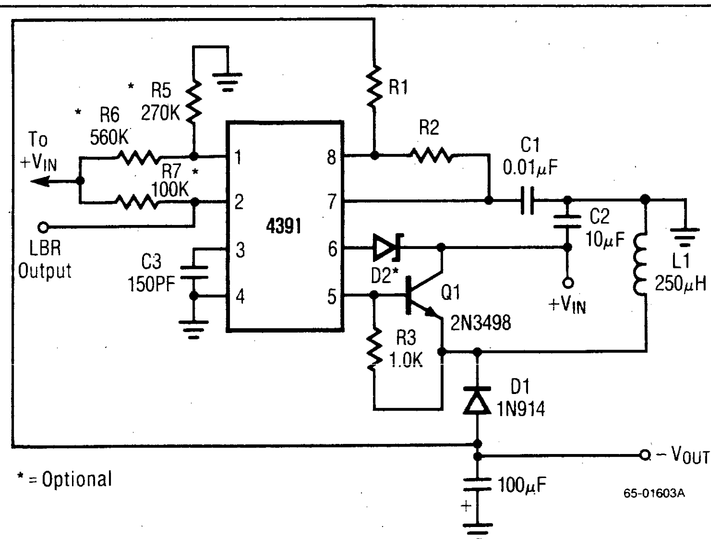


Figure 4. High Power/High Voltage Application Circuit
(Component Values Shown are for -5.0V Output)

RAYTHEON

Precision High Speed Latching Comparator

4805

Features

- 22nS Propagation Delay
- Low Offset Voltage — 100μV
- Low Offset Current — 15nA
- TTL Compatible Latch
- TTL Output

Description

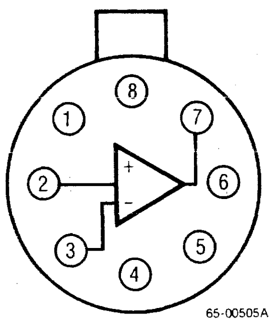
The RC/RM4805 is the ideal comparator for high speed, high precision applications. The input errors are factory trimmed to less than 1/10 LSB of a 12 bit, 10 volt system. The latch function allows the System Designer additional flexibility. When the latch input is a TTL low, the comparator functions normally. When the input is raised to a TTL high, the comparator output is latched in its current state. The latch functions over the full military temperature range.

The 4805 is ideal for ultra precise, very fast system designs. Typical applications include successive approximation A/D converters of 12 or more bits, zero crossing detectors, high speed sampling, or window detectors.

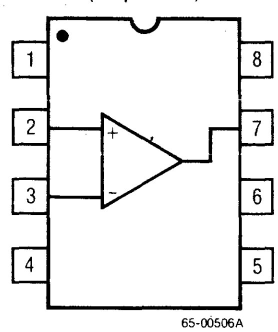
The 4805 high speed comparator is functionally equivalent to the more popular comparators, HA-4950, AM686, SE527, CMP-05 and μA760. Propagation delay is 35nS with a 1/2 LSB overdrive in a 12 bit, 10 volt system.

Connection Information

TO-99
Metal Can
(Top View)

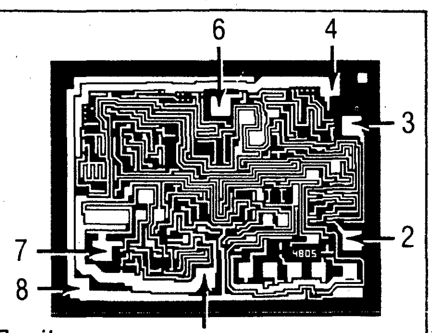


8-Lead
Dual-in-Line
Ceramic Package
(Top View)



Pin	Function
1	Ground
2	Non-Inverting Input
3	Inverting Input
4	V-
5	NC
6	Latch Enable
7	V_{OUT}
8	V+

Mask Pattern



Die Size: 51 x 67 mils
Min. Pad Dimensions: 4 x 4 mils

Thermal Characteristics

	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can
Max. Junction Temp.	175°C	175°C
Max. P_D $T_A < 50°C$	833mW	658mW
Therm. Res. θ_{JC}	45°C/W	50°C/W
Therm. Res. θ_{JA}	150°C/W	190°C/W
For $T_A > 50°C$ Derate at	8.33mW per °C	5.26mW per °C

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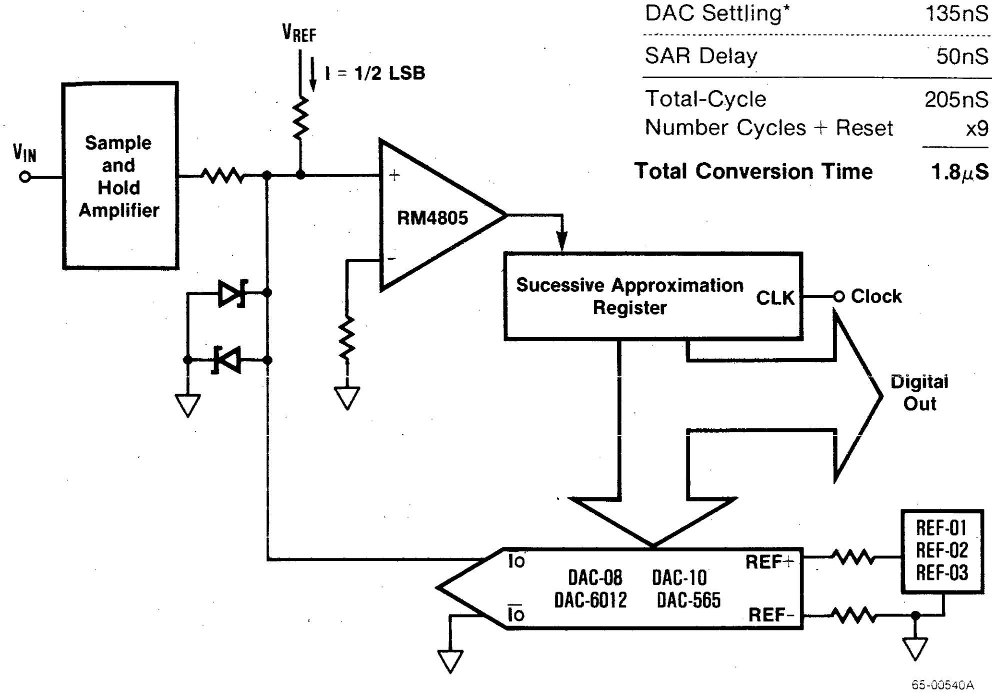
Typical Applications

	8-Bit	10-Bit	12-Bit
Conversion Time			
RM4805 Response	20nS	22nS	50nS
DAC Settling*	135nS	135nS	500nS
SAR Delay	50nS	50nS	50nS
Total-Cycle	205nS	207nS	600nS
Number Cycles + Reset	x9	x11	x13
Total Conversion Time	**1.8μS**	**2.3μS**	**7.8μS**



*Response will be affected by DAC's output capacitance and equivalent resistance.

RAYTHEON

+10V Precision Voltage References REF-01

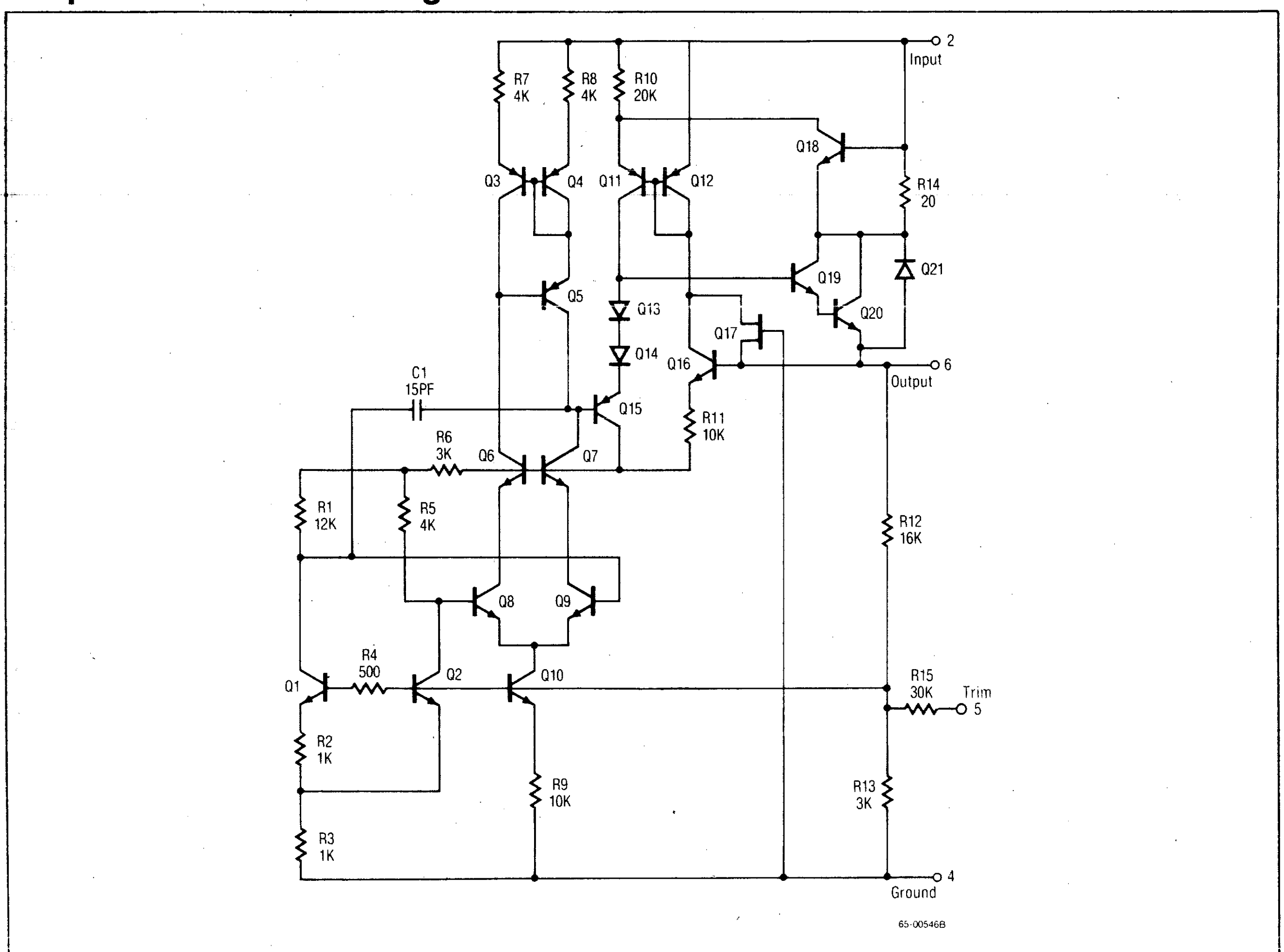
Features

- 10 Volt Output — ±0.3%
- Adjustable — ±3.0%
- Excellent Temperature Stability — 3.0ppm/°C
- Low Noise — 20μV_{p-p}
- Wide Input Voltage Range — 12V to 40V
- No External Components
- Short Circuit Proof
- Low Power Consumption — 15mW

Description

The REF-01 Precision Voltage Reference contains a band-gap reference using thin-film resistors, a step-up amplifier, short circuit protection, and a zener-trim network. The REF-01's 10V output shows excellent stability for large changes of temperature, load current, and input voltage. An adjust pin is provided that can change the output voltage by at least 3.0% with little effect on temperature coefficient.

Simplified Schematic Diagram



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+5.0V Precision Voltage References REF-02

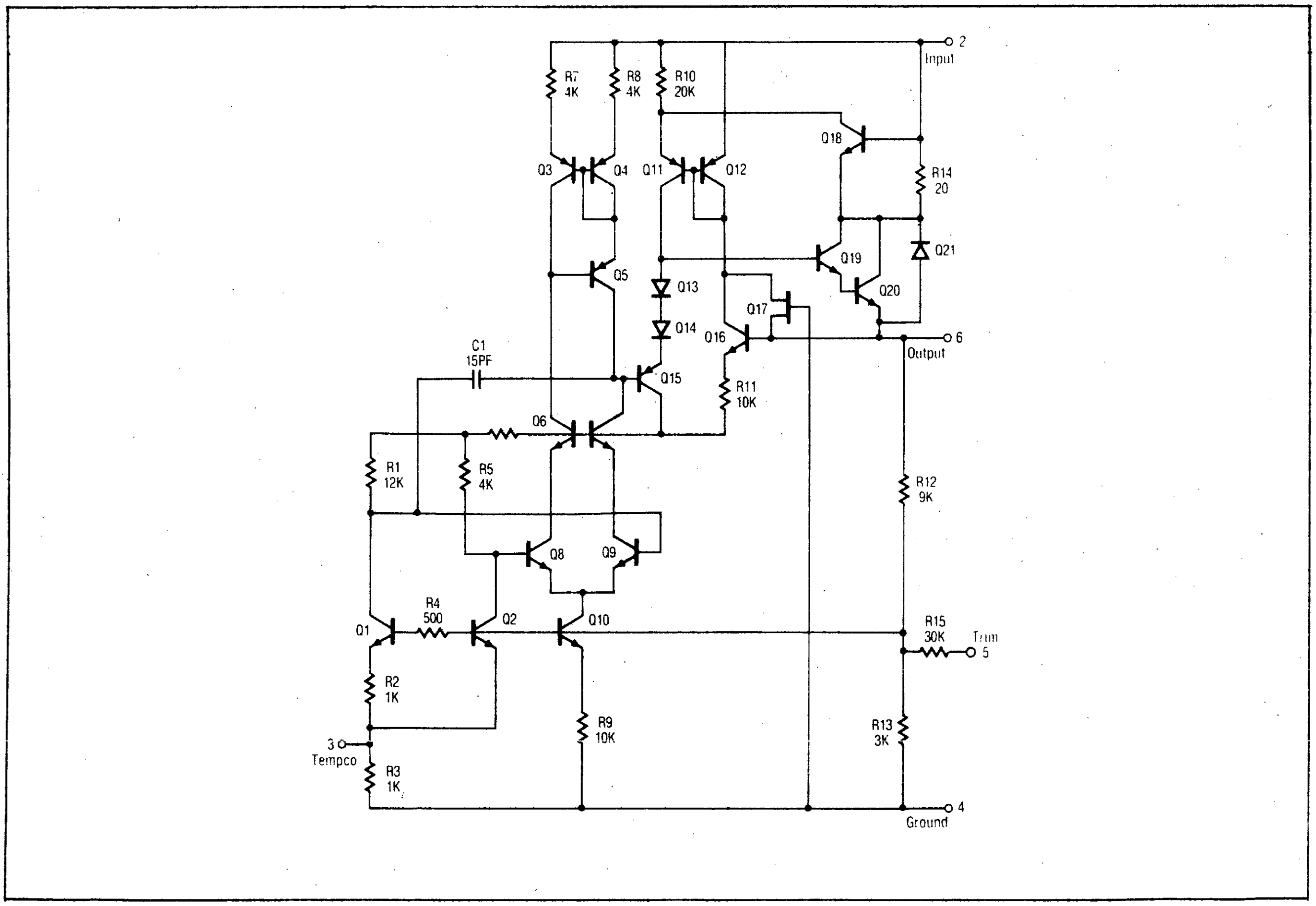
Features

- 5.0 Volt Output — ±0.3%
- Adjustable — ±3.0%
- Excellent Temperature Stability — 3.0ppm/°C
- Low Noise — $10\mu V_{p-p}$
- Wide Input Voltage Range — 7.0V to 40V
- No External Components
- Short Circuit Proof
- Low Power Consumption — 15mW

Description

The REF-02 Precision Voltage Reference contains a band-gap reference using thin-film resistors, a step-up amplifier, short circuit protection, and a zener-trim network. The REF-02's 5.0V output shows excellent stability for large changes of temperature, load current, and input voltage. An adjust pin is provided that can change the output voltage by at least 3% with little effect on temperature coefficient. A tempco pin also provides a voltage that varies linearly with temperature, typically from +470mV to +830mV over the military temperature range.

Simplified Schematic Diagram



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RAYTHEON

+2.5V Precision Voltage References

REF-03

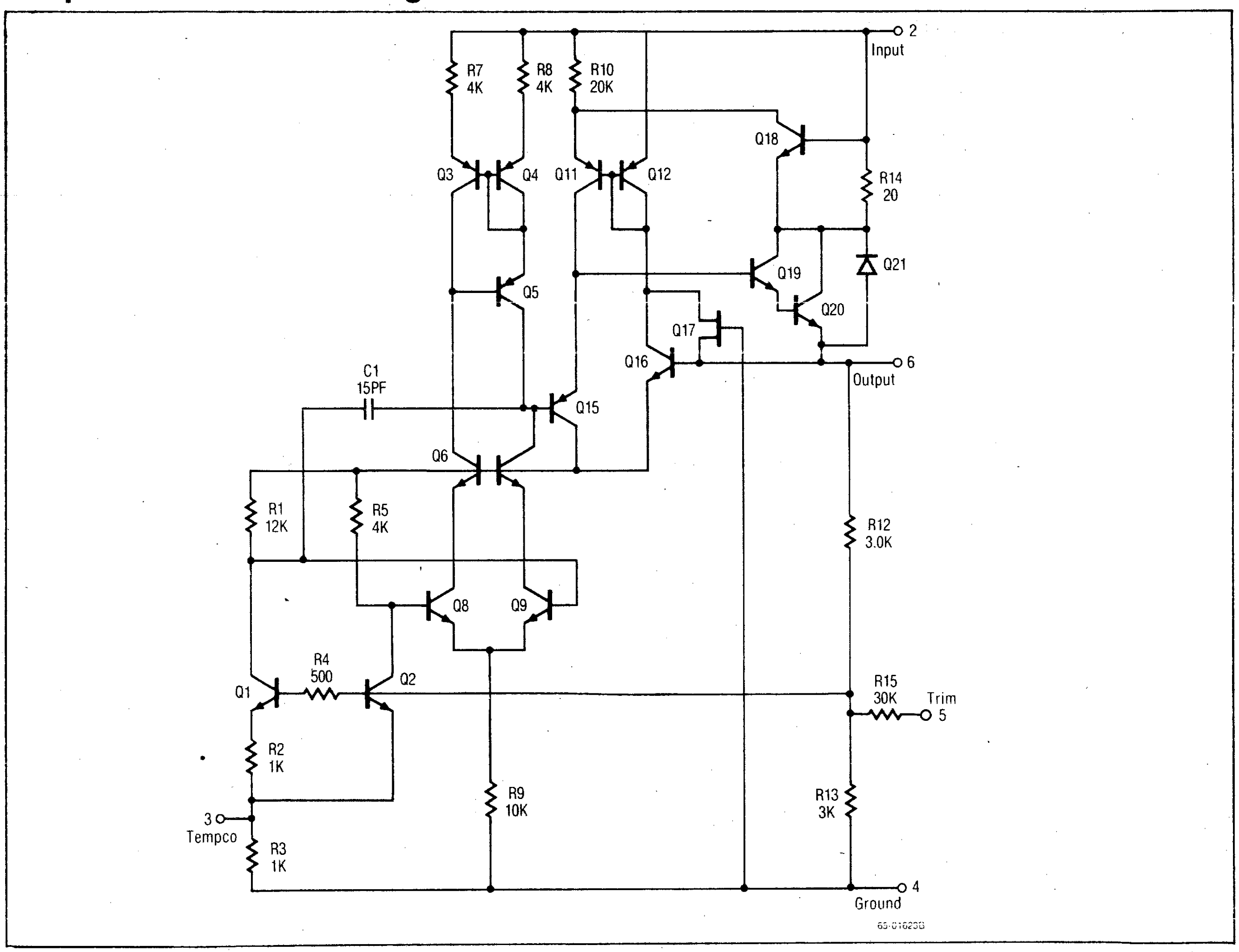
Features

- 2.5 Volt Output — ±0.3%
- Adjustable — ±3%
- Excellent Temperature Stability — 3.0ppm/°C
- Low Noise — $5.0\mu V_{p-p}$
- Wide Input Voltage Range — 4.5V to 40V
- No External Components
- Short Circuit Proof
- Low Power Consumption — 15mW

Description

The REF-03 Precision Voltage Reference contains a band-gap reference using thin-film resistors, a step-up amplifier, short circuit protection, and a zener-trim network. The REF-03's 2.5V output shows excellent stability for large changes of temperature, load current, and input voltage. An adjust pin is provided that can change the output voltage by at least 3.0% with little effect on temperature coefficient. A tempco pin also provides a voltage that varies linearly with temperature, typically from +470mV to +830mV over the military temperature range.

Simplified Schematic Diagram



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RAYTHEON

10-Bit High Speed Multiplying D/A Converter

DAC-10

Features

- Nonlinearity to 0.05% Max Over Temperature Range
- Low Full Scale Drift — 10ppm/°C
- Wide Range Multiplying Capability 1.0MHz bandwidth
- Wide Power Supply Range— +5.0V/-7.5V to ±18V
- Two Quadrant Multiplying
- High Output Compliance
- High Speed — 85nS

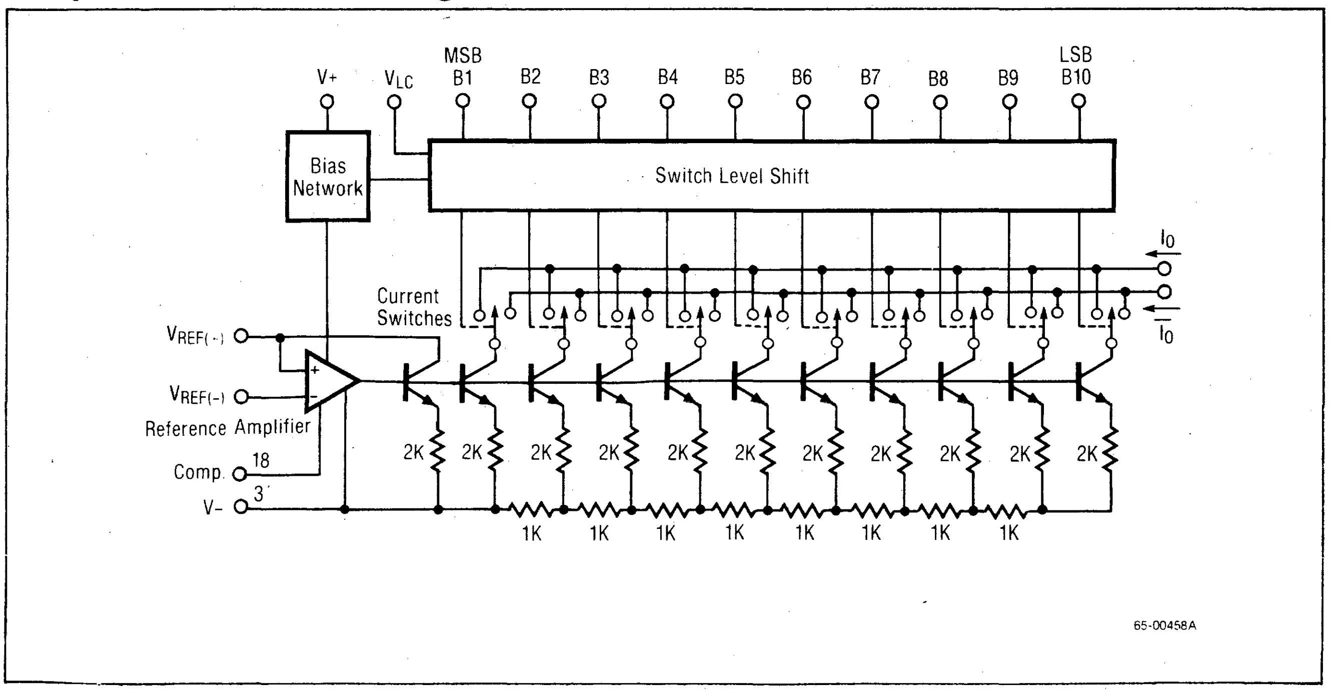
Applications

- A/D Converters
- Servo Controls
- Waveform Generators
- Programmable Power Supplies
- High Speed Modems

Description

The DAC-10 is a high speed, 10-bit, monolithic, multiplying Digital-to-Analog Converter. Settling times of 85nS are achieved with low power consumption and minimal output glitches. Full scale (10-bit) accuracy is achieved. The DAC-10 can be operated from almost any logic level input due to its adjustable (V_{LC}) threshold. Monotonicity is guaranteed to 10 bits and nonlinearities of ±0.05% are guaranteed over the full operating temperature range. Power consumption can be reduced to 85mW by lowering supply voltages to +5.0V to -7.5V. Operation at supply voltages up to ±18V does not appreciably affect device performance. Zener-Zap trimming is performed at wafer probe to optimize the converter's accuracy.

Simplified Schematic Diagram



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RAYTHEON

Micro-Power Switching Regulators

4191/2/3

Features

- High Efficiency — 80% Typical
- Low Quiescent Current — 135μA
- Adjustable Output — 2.5V to 30V
- Output Current — 150mA
- Internal Reference — 1.31V
- Remote Shutdown Capabilities

Description

Raytheon's micro-power switching regulators, 4191, 92 and 93, are the industry's first monolithic low power switching regulators available in a 8-lead mini-DIP, and designed specifically for battery operated instruments. They each contain a 1.3V temperature compensated bandgap reference, adjustable free running oscillator, voltage comparator, low battery detection circuitry and a 150mA switch transistor with all of the functions required to make a complete low power switching regulator.

These regulators can achieve up to 80% efficiency in most applications while being able to operate over a wide input supply voltage range, 2.4V to 24V, at an ultra low quiescent drain of 135μA.

These regulators have a free running oscillator which provides the drive circuitry for the on chip 150mA switch transistor. The 100Hz to 75kHz oscillator frequency is determined by an external capacitor on pin 2.

These universal regulators can be used as a building block in three basic applications: step-up, step-down, inverting.

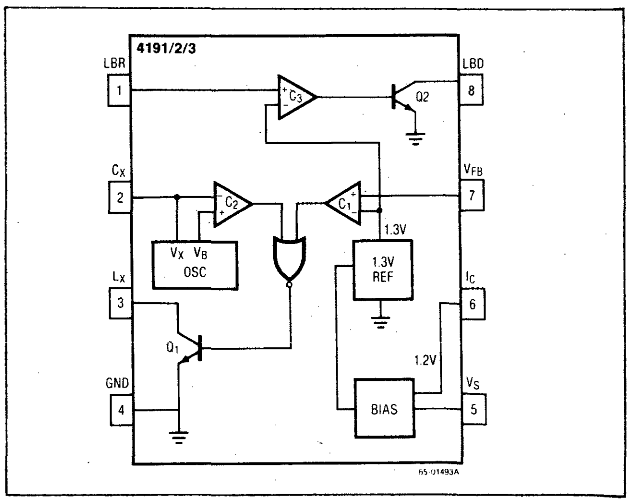
In their most popular configuration, step-up, these regulators can use fewer battery cells, making available more board space and lengthen battery life.

A practical example of these advantages would be an instrument designed to operate from a nominal 9 volt supply voltage. If this instrument were powered with just 7 components; a steering diode, an inductor, two resistors, a capacitor, a 4191, 92 or 93 and a 9 volt battery, it would receive a continuous 9 volts until the battery had decayed to a terminal voltage of 2.4 volts. If board space is at a premium, then the designer could remove the 9 volt source and replace it with a single 3 volt Ni-Cad battery without making any other adjustment(s) to the circuitry or affecting the overall operation of this instrument.

The open collector output transistor of these regulators provide the designer a method to have a "Low Battery Indicator" output current that can be used to signal a LCD whenever the battery voltage drops below a programmed level. This programmed level is determined by the designer with the selection of external resistors connected to pin 1.

The 4191, 92 and 93 offer the designer a mechanism to shut down this chip by connecting a zener diode in series with the I_C lead (pin 6). This will shut down the chip whenever the battery voltage drops below the predetermined level. In this application, the circuit can be designed to signal a LCD whenever the battery voltage has dropped to the first programmed level, then shut itself off when the battery has dropped to the second level.

Functional Block Diagram



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RAYTHEON Complete High-Speed 12-Bit Monolithic Digital-to-Analog Converter DAC-565

Features

- Nonlinearity 1/2 LSB —0.012%
- Differential Nonlinearity 13 bits — 0.012%
- Settles to 1/2 LSB in 200nS
- On Chip Bandgap Reference
- Linearity Guaranteed Over Temperature
- Low Power: 225mW Including Reference
- Direct Interface to All Major Logic Families

Description

The DAC-565 is a fast 12-bit digital-to-analog converter consisting of 12-bit precision, high-speed bipolar current steering switches, laser-trimmed thin film resistor network, stable bandgap reference, span and bipolar offset resistors to produce an accurate analog output current.

The high performance and flexibility of the DAC-565 was acheived through circuit design and layout, a thin film resistor process and interactive computer-controlled laser trimming. The DAC-565 settles to 1/2 LSB in 200nS, typical, with a maximum settling time of 500nS. Accuracy is specified at a maximum of 1/2 LSB for all grades.

This high speed and accuracy coupled with the inherent high output impedance make the DAC-565 the ideal DAC for high-speed display drivers, high speed control systems, and with the RC4805 high-speed latching comparator, analog-to-digital converters.

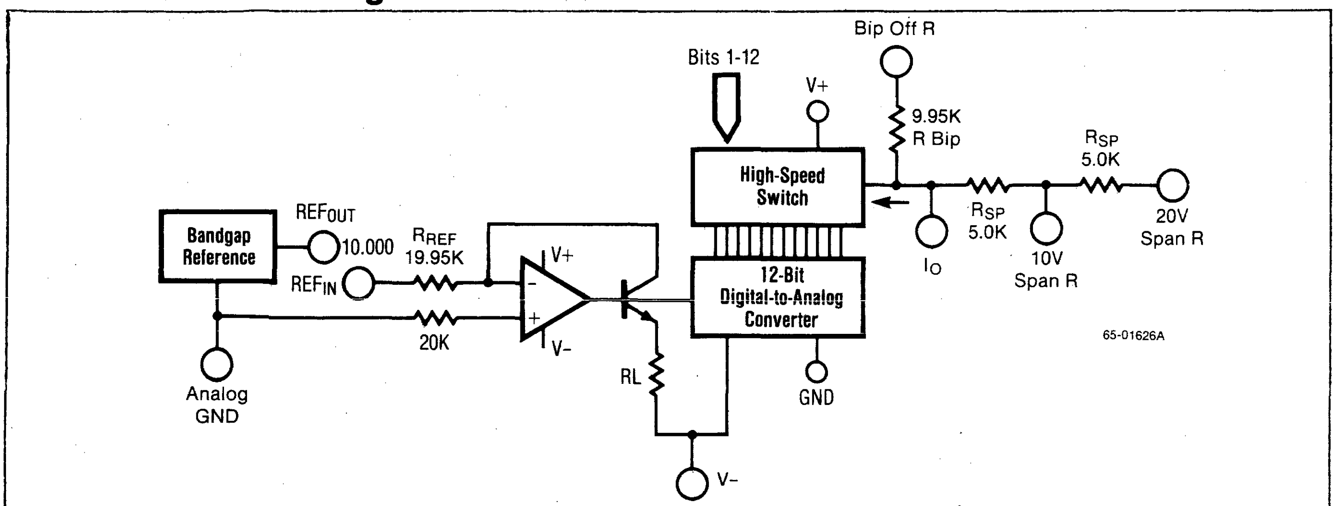
The bandgap reference is laser trimmed to optimize both temperature drift and absolute output voltage. The current sourcing capability of the DAC-565 reference (10mA typical) allows this reference to drive the DAC and also other peripheral circuit elements. Typical reference drift is better than 15ppm/°C (S and J grade).

The DAC-565 is available in 3 performance grades. The DAC-565J and DAC-565D grades are specified over 0°C to +70°C, while the DAC-565S grade is specified over the -55°C to +125°C temperature range.

Product Highlights

- The DAC-565 is a self-contained DAC and voltage reference with application resistors on a monolithic chip.
- The device incorporates interdigitizing which minimizes the effects of thin film sputtering, thermal, and diffusion gradients in the most critical portions of the design. Therefore, excellent linearity distributions are achieved prior to trimming, thus insuring optimal stability of the nonlinearity over temperature as well as stability versus time.
- The thin film resistors have a trim tab which is distant from the main body of the resistor. This resistor geometry insures near perfect nonlinearities after trim as well as minimum damage due to laser trimming.
- The internal reference is laser trimmed to 10 Volts with a ±1.0% maximum error. The reference voltage is available externally and can provide typically 10mA beyond that required for the reference and bipolar offset resistors.
  The DAC-565 contains SiCr thin film application resistors which can be used with either an external op amp to provide a precision voltage output DAC or as input resistors for a successive approximation A/D converter. The resistors are inherently matched and are laser trimmed to guarantee minimum full scale and bipolar offset errors.
- The DAC-565S grade guarantees linearity and monotonicity over the -55°C to +125°C range and is available fully processed to MIL-STD-883, Level B.

Functional Block Diagram



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RAYTHEON

12-Bit High Speed Multiplying D/A Converter

DAC-6012

Features

- Differential Nonlinearity — 0.012% (13 Bits)
- Guaranteed Monotonicity to 12 Bits Over Temperature
- Relative Accuracy — 0.05% All Grades
- Fast Settling Time — 250nS to ±0.5 LSB
- Full Scale Output Current — 4.0mA
- Complementary Current Outputs
- Output Compliance — -5.0V to +10V
- Full Scale Tempco — ±10ppm/°C
- Power Consumption — 230mW
- Direct Interface to All Major Logic Families
- Standard Processing without Resistor Trimming
- Low Cost

Description

The Raytheon DAC-6012 series of monolithic Multiplying Digital-to-Analog Converters guarantee differential nonlinearity to better than ±0.5 LSB (0.012%) for the 6012A and ±1.0 LSB (0.025%) for the 6012 over the full military and commercial temperature ranges. In addition to the excellent Differential Nonlinearity specifications, the 6012 series also include many features that previously were found in expensive hybrid modules or required full use of monolithic thin film laser or zener zap trimming techniques.

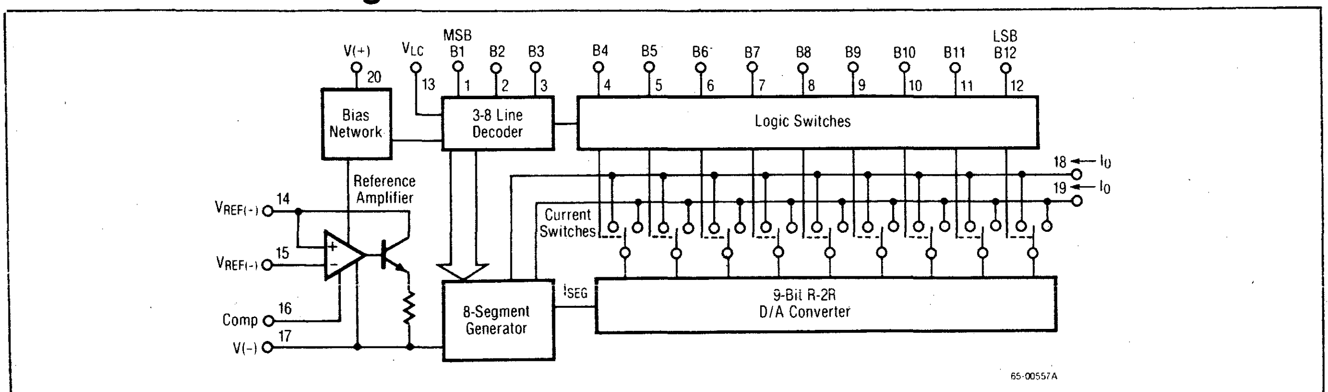
The Raytheon DAC-6012 incorporates a segmented design technique which reduces the requirement for high accuracy resistor ladder networks as an integral part of the DAC. The DAC-6012 design is structured with a 3-bit segment decoder, 5-bit master R-2R ladder DAC and 4-bit Slave DAC. This circuit configuration actually contains less ladder resistors than the traditional R-2R ladder approach as well as effectively improving the accuracy of the ladder resistors by a factor of 8.

The performance of the DAC-6012 is virtually independent of supply voltage variations due to the inherent nature of its design and processing. As an example, the DAC-6012 may be operated at any voltage from +4/-10V to ±18V with minimal effect on the full scale current, DNL, relative accuracy and settling time. The 5MΩ output impedance and -5.0V to +10V compliance range make the DAC-6012 ideal for high speed applications where output load resistors can be used in place of an output interface amplifier.

The complementary current outputs of the DAC-6012 are useful in symmetrical offset DAC applications and A/D converters requiring constant current loads to ensure significant reduction of switching transients.

In conjunction with the REF-01 and REF-02 voltage references, and the 4805 fast precision voltage comparator, the DAC-6012 can be used as the main building block in a wide variety of data conversion applications.

Functional Block Diagram



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LINEAR

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RAYTHEON

8-Bit High Speed Multiplying D/A Converter

DAC-08

Features

- Fast Settling Output Current — 85nS
- Full Scale Current Prematched to ±1.0 LSB
- Direct Interface to TTL, CMOS, ECL, HTL, PMOS
- Nonlinearity to ±0.1% Max. Over Temperature Range
- High Output Impedance and Compliance — -10V to +18V
- Differential Current Outputs
- Wide Range Multiplying Capability — 1.0MHz Bandwidth
- Low FS Current Drift — ±10ppm/°C
- Wide Power Supply Range — ±4.5V to ±18V
- Low Power Consumption — 33mW @ ±5.0V
- Low Cost

Description

The DAC-08 series of 8-bit monolithic multiplying Digital-to-Analog Converters provide very high speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85nS settling times with very low "glitch" and at low power consumption. Monotonic multiplying performance is attained over a wide 40 to 1 reference current range. Matching to within 1 LSB between reference and full scale currents eliminates the need for full scale trimming in most applications.

Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

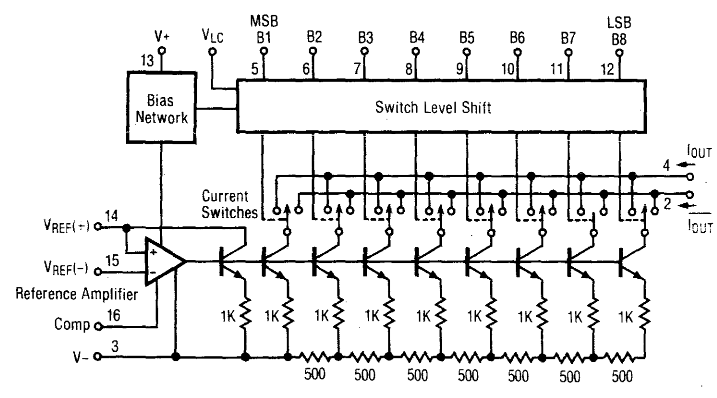
High voltage compliance dual complementary current outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. In many applications, the outputs can be directly converted to voltage without the need for an external op amp.

All DAC-08 series models guarantee full 8-bit monotonicity, and nonlinearities as tight as ±0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±4.5V to ±18V power supply range, with 33mW power consumption attainable at ±5.0V supplies.

The compact size and low power consumption make the DAC-08 attractive for portable and military/aerospace applications; devices processed to MIL-STD-883A, Level B are available.

DAC-08 applications include 8-bit, 1.0μS A/D converters, servo-motor and pen drivers, waveform generators, audio encoders and attenuators, analog meter drivers, programmable power supplies, CRT display drivers, high speed modems and other applications where low cost, high speed and complete input/output versatility are required.

Functional Block Diagram



RAYTHEON COMPANY • Semiconductor Division • 350 Ellis Street • Mountain View, CA 94039-7016
(415) 968-9211 TWX: 910-374-6484

High Performance Operational Amplifiers

Device	Descprition	Maximum Input Specifications			Typical Input Noise Specifications				Typ. Slew Rate (V/μS)	Typ. Unity Gain BW (MHz)	Max. Sply Volt. (±V)	Pins	Temp Range
		Offset Volt. (mV)	Offset Cur. (nA)	Bias Cur. (nA)	Volt. Density nV √Hz	Low Freq. Corner eN (Hz)	Cur. Density PA √Hz	Low Freq. Corner iN (Hz)					
OP-05	Single Instrumentation Grade	0.500	2.8	±3.0	10.0	10	0.14	50	0.17	0.5	22	8	M, C
OP-05A	Single Instrumentation Grade	0.150	2.0	±2.0	10.0	10	0.14	50	0.17	0.5	22	8	M, C
OP-05C	Single Instrumentation Grade	1.300	6.0	±7.0	10.2	10	0.15	50	0.17	0.5	22	8	M, C
OP-05E	Single Instrumentation Grade	0.500	3.8	±4.0	10.0	10	0.14	50	0.17	0.5	22	8	M, C
OP-07	Single Ultra Low Offset Voltage	0.075	2.8	±3.0	10.0	10	0.14	50	0.17	0.6	22	8	M
OP-07A	Single Ultra Low Offset Voltage	0.025	2.0	±2.0	10.0	10	0.14	50	0.17	0.6	22	8	M
OP-07C	Single Ultra Low Offset Voltage	0.150	6.0	±7.0	10.2	10	0.15	50	0.17	0.6	22	8	C
OP-07D	Single Ultra Low Offset Voltage	0.150	6.0	±12	10.3	10	0.15	50	0.17	0.6	22	8	C
OP-07E	Single Ultra Low Offset Voltage	0.075	3.8	±4.0	10.0	10	0.14	50	0.17	0.6	22	8	C
OP-27A	Single Ultra Low Noise	0.025	35	±40	3.0	3.0	0.4	140	2.8	8.0	22	8	M, C
OP-27B	Single Ultra Low Noise	0.060	50	±55	3.0	3.0	0.4	140	2.8	8.0	22	8	M, C
OP-27C	Single Ultra Low Noise	0.100	75	±80	3.2	3.0	0.4	140	2.8	8.0	22	8	M, C
OP-27E	Single Ultra Low Noise	0.025	35	±40	3.0	3.0	0.4	140	2.8	8.0	22	8	M, C
OP-27F	Single Ultra Low Noise	0.060	50	±55	3.0	3.0	0.4	140	2.8	8.0	22	8	M, C
OP-27G	Single Ultra Low Noise	0.100	75	±80	3.2	3.0	0.4	140	2.8	8.0	22	8	M, C
OP-37A*	Single High Slew Rate Low Noise	0.025	35	±40	3.0	3.0	0.4	140	11	63	22	8	M, C
OP-37B*	Single High Slew Rate Low Noise	0.060	50	±55	3.0	3.0	0.4	140	11	63	22	8	M, C
OP-37C*	Single High Slew Rate Low Noise	0.100	75	±80	3.2	3.0	0.4	140	11	63	22	8	M, C
OP-37E*	Single High Slew Rate Low Noise	0.025	35	±40	3.0	3.0	0.4	140	11	63	22	8	M, C
OP-37F*	Single High Slew Rate Low Noise	0.060	50	±55	3.0	3.0	0.4	140	11	63	22	8	M, C
OP-37G*	Single High Slew Rate Low Noise	0.100	75	±80	3.2	3.0	0.4	140	11	63	22	8	M, C
RC714	Single Precision	0.075	2.8	±3.0	9.6	3.0	0.12	140	0.17	0.5	22	8	C
RC714C	Single Precision	0.150	6.0	±7.0	9.8	3.0	0.13	140	0.17	0.5	22	8	C
RC714E	Single Precision	0.075	3.8	±4.0	9.6	3.0	0.12	140	0.17	0.5	22	8	C
RC714L	Single Precision	0.250	20	±30	9.8	3.0	0.13	140	0.17	0.5	22	8	C
RC3078	Single Micropower	4.5	32	170	19.0	100	1.0	200	1.5	0.1	15	8	M, C
RC3078A	Single Micropower	3.5	2.5	12	36.0	100	0.4	200	1.5	0.1	15	8	M, C
RC5534	Single High Performance Low Noise	4.0	300	1500	4.0	100	0.6	200	13.0	10.0	22	8	M, C
RC5534A	Single High Performance Low Noise	4.0	300	1500	3.5	100	0.4	200	13.0	10.0	22	8	M, C
RC2041	Dual High Performance Low Noise	3.0	200	500	5.0	20	0.4	200	3.0	7.0(4.0)	18	8	C
RC2043	Dual High Performance Low Noise	3.0	200	1000	5.0	20	0.4	200	6.0	14(8.0)	18	8	C
RC4560	Dual High Performance	6.0	200	500	10.0	20	0.5	200	4.0	10(7.0)	18	8	C
RC4562	Dual High Performance	6.0	200	500	6.0	20	0.2	200	7.0	15(8.0)	18	8	C
RC4558	Dual High Gain	6.0	200	500	10.0	20	0.5	200	1.0	2.5	18	8	M, C
RC4559	Dual High Performance	6.0	100	250	10.0	20	0.18	200	2(1.5)	4.0(3.0)	18	8	M, C
RC4739	Dual Low Noise	6.0	200	500	10.0	20	0.5	400	1.0	4.0	18	14	M, C
RC5532	Dual High Performance Low Noise	2.0	150	800	5.0	100	0.7	200	8.0	10.0	22	8	M, C
RC5532A	Dual High Performance Low Noise	2.0	150	800	5.0	100	0.7	200	8.0	10.0	22	8	M, C
RC4556	Dual High Performance	6.0	200	500	10.0	20	0.5	200	3.0	8.0(5.0)	18	8	C

Notes:

( ) denotes guaranteed specifications
M = Military/883B −55°C to +125°C
C = Commercial 0°C to +70°C
= Denotes preliminary data

RAYTHEON

Linear Integrated Circuits

The RCA line of linear integrated circuits (LIC's) covers a broad range of solid-state devices, including BiMOS, bipolar, CMOS, and MOS/FET types for a wide variety of applications in industrial, military, and consumer equipment. These circuits are available in a wide variety of package styles, including hermetic TO-5; dual-in-line plastic, ceramic, and frit-seal ceramic; and TO-220-style (Versa-V) plastic. RCA also offers high-reliability versions of a broad range of these standard circuits processed in accordance with MIL-STD-883 and MIL-M-38510.

BiMOS Circuits
RCA BiMOS op-amps and comparators utilizing both bipolar and p-channel MOS transistors on a common monolithic substrate establish new performance standards in virtually all op-amp categories: general-purpose, FET input, wideband (4 to 70 MHz), micropower (down to 1.5 μW), high-current (to 22 mA), and in comparator applications, particularly in those requiring the added convenience and flexibility of two single-supply comparators in one package with operation up to 44 volts.

Operational Amplifiers
RCA offers a broad line of operational amplifiers, including general-purpose types in single, dual, and quad configurations; types including mixed technologies (e.g., CMOS, PMOS and bipolar, called BiMOS); variable types often referred to as programmable op-amps; micropower; wide-band; high-voltage; high-current; and precision types.

Voltage Comparators
RCA's line of BiMOS and bipolar comparators includes single, dual, quad, and programmable types for a wide variety of applications in instrumentation, communications, and industrial equipment.

Data Conversion Circuits
This category includes A/D converters, 7-segment decoder/drivers, and display drivers.

Arrays
RCA's broad line of arrays includes transistor types (bipolar and CMOS), transistor amplifier types, transistor/diode types, and diode types in a wide variety of configurations: n-p-n, p-n-p, n-p-n/p-n-p, Darlington, superbeta, programmable unijunction transistor (PUT) and SCR.

Power Control Circuits
This category includes an automotive ignition switch, power amplifiers, programmable Schmitt triggers, solenoid and motor drivers, universal controller, voltage regulators and zero-voltage switches.

Differential Amplifiers
The RCA line of differential amplifiers includes a broad variety of general-purpose devices in which the basic signal-processing function is accomplished by a single differential-amplifier stage.

Special Function Circuits
These types include automotive circuits, broadband (video) amplifiers, four-quadrant multipliers, prescalers, single-chip detector alarm systems and a timercircuit.

TV/CATV Circuits
These circuits include AFT, chroma systems, horizontal and vertical deflection systems, sync/AGC circuits, luminance processors, multiplex decoders, PIX IF, remote control, sound IF, tuning and Videodisc circuits.

For a summary of available products refer to the Linear Integrated Circuits product guide CDL-820J for linear integrated circuits and to MOS Field-Effect Transistors catalog MOS-160D for MOS devices. For complete technical data refer to Linear Integrated Circuits DATABOOK SSD-240B.

LIC Operational Amplifiers

BiMOS Types

- **CA3193 BiMOS Precision Operational Amplifier**
- **CA3493 BiMOS Precision Operational Amplifier**

The CA3193 series and CA3493 series are ultra-stable, precision-instrumentation operational amplifiers that employ both PMOS and bipolar transistors on a single chip. They are internally phase-compensated and provide a gain-bandwidth product of 1.2 MHz. The CA3193 series are pin-compatible with the industry 741 series and many other IC op amps, and may be used as replacements for 741-series in most applications.

The CA3493 series are pin-compatible with many industry types such as 725, 108A, OP-5, OP-7, and LM714 where positive nulling is employed.

Features

- Low V_{IO}:
  75 μV max. (CA3493B)
  200 μV max. (CA3493A)
  500 μV max. (CA3493)
- Low $\Delta V_{IO}/\Delta T$:
  2 μV/°C max. (CA3493B)
  3 μV/°C max. (CA3493A)
  5 μV/°C max. (CA3493)
- Low I_{IO} and I_I
- Low $\Delta I_{IO}/\Delta T$:
  50 pA/°C max. (CA3493B)
  150 pA/°C max. (CA3493)
- Low $\Delta I_I/\Delta T$:
  0.5 nA/°C max. (CA3493B)
  3.7 nA/°C max. (CA3493)
- Extremely high gain:
  120 dB min. (CA3493B)
  110 dB min. (CA3493A)
  100 dB min. (CA3493)
- Low V_{IO} vs. time
- High CMRR and PSRR
- Internally compensated: 1.2-MHz gain-bandwidth product
- Low input noise: 0.1 Hz to 10 Hz
  Noise voltage: 0.36 μV_{p-p} typ.
  Noise current: 12 pA_{p-p} typ.

Applications

- Thermocouple preamplifiers
- Strain-gauge bridge amplifiers
- Summing amplifiers
- Differential amplifiers
- Bilateral current sources
- Log amplifiers
- Differential voltmeters
- Precision voltage references
- Active filters
- Buffers
- Integrators
- Sample-and-hold circuits
- Low frequency filters

- **CA3420 Low Supply Voltage, Low-Input Current BiMOS OP-AMP**
- **CA3440 Nanopower BiMOS OP AMP**

The CA3420, CA3420A and CA3420B BiMOS operational amplifiers feature gate-protected PMOS transistors in the input circuit to provide very high input impedance, very low input currents (less than 1 pA). The internal bootstrapping network features a unique guardbanding technique for reducing the doubling of leakage current for every 10° C increase in temperature. The CA3420 series operates at total supply voltages from 2 to 20 volts either single or dual supply.

Features

- 2 V Supply at 300 μA Supply Current
- 0.04 pA (typ) Input Current (Essentially Constant to 85°C)
- Rail-to-Rail Output Swing (Drive ±2 mA into 1 KΩ Load)
- Pin Compatible with 741 Op-Amp
- Low Cost 8-Lead Minidip, TO-5
- Output driving current 1.5 ma. min. (provided by non-linear current mirrors)

Applications

- pH Probe Amplifiers
- Picoammeters
- Electrometer (High Z) instruments
- Portable Equipment
- Inaccessible Field Equipment
- Battery Dependent Equipment (Medical and Military)
- Function generators
- Oscillators

The CA3440-series BiMOS OP AMP features gate-protected PMOS transistors in the input circuit to provide very high input impedance and very low input current (10 pA). These devices operate at total supply voltages from 5 to 15 volts and can be operated over the temperature range from -55 C to +125 C. Their virtues are programmability and very low standby power (300 nW).

Features

- 300-nW (typ.) standby power at $V^+ = 5V$
- Supply current, BW, slew rate programmable using external resistor
- 10-pA (typ.) input current
- 5.0 to 15-V supply (±2.5 to ±7.5V)/5-12 V single supply operation
- Output drives typical bipolar-type loads
- Low-cost 8-lead Mini-DIP, TO-5
- High $I_{out}/I_{standby}$ ratio at 900nW standby (can on demand sink 3.1 mA max (2 K load), source 3mA)
- Very low total standby currents (50 nA)
- Pin-compatible with 741 op amp

Recommended Applications

- Micropower Band-Gap Reference supply circuits
- Micropower Amplifier circuits
- Multimeters
- Audio amplifiers
- Solar-cell powered systems
- Voice-squelched amplifiers
- Battery and portable instruments
- Smoke detectors and security systems
- Biomedical comparators — buffers
- Active filters
- Multivibrators

LIC Operational Amplifiers

BiMOS Types

- **CA3260 Dual OP AMP**

The RCA CA3260 series are operational amplifiers that combine the advantages of both CMOS and bi-polar transistors on a monolithic chip. The CA3260 series are dual versions of the CA3160 series.

Features

- Dual version of the CA3160
- MOS/FET input stage provides:
  very high Z_I = 1.5 TΩ (1.5 × 10^{12}Ω) typ.
  very low II = 5 pA typ. at 15-V operation
  = 2 pA typ. at 5-V operation
- Common-mode input-voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail
- CMOS output stage permits signal swing to either (or both) supply rails
- Low V_{IO}: 2 mV max. (CA3260B)
  Wide BW: 4 MHz typ. (unity-gain crossover)
  High SR: 10 V/μs typ. (unity-gain follower)
  High output current (I_O): 20 mA typ.
- High A_{OL}: 320,000 (110 dB) typ.
- Internal phase compensation for unity gain
- Same pin-out as CA358, CA1458, CA1558

Applications

- Ground-referenced single-supply amplifiers
- Fast sample-hold amplifiers
- Long-duration timers/monostables
- Ideal interface with digital CMOS
- High-input-impedance wideband amplifiers
- Voltage followers (e.g., follower for single-supply D/A converter)
- Voltage regulators (permits control of output voltage down to zero volts)
- Wien-Bridge oscillators
- Voltage-controlled oscillators
- Photo-diode sensor amplifiers

- **CA3240 Dual-Unit Extended-Voltage-Range Op-Amp**
- **CA3140 Extended-Voltage-Range Op-Amp**

- very high input impedance: 1.5 TΩ typ.
- very low input current: 10 pA typ. at ±15 V
- low input offset voltage: as low as 2 mV max.
- wide common-mode input-voltage range: can be swung 0.5 V below negative rail
- output swing complements input common-mode range, permitting full utilization of low supply voltages (to 4 V) or to within 0.2 V when driving power transistors (no need for level-shifting circuits)
- PMOS input devices are protected by rugged bipolar diodes plus bipolar speed and high supply voltage.
- Operating capability: 4-44 V, single or dual supply

COMPARISON CHART

Symbol (TA = 25°C)	CA3240 Min.	CA3240 Typ.	CA3240 Max.	1458 Min.	1458 Typ.	1458 Max.	Units
R_I	30K	1500K	—	0.3	2	—	MΩ
I_I	—	10	50	—	80K	500K	pA
I_{IO}	—	0.5	30	—	20K	200K	pA
V_{IO}	—	5	15	—	2	6	mV
SR	—	9	—	—	0.5	—	V/μs
f_T	—	4.5	—	—	1	—	MHz
V_{ICR}	-15	-15.5 to +12.5	+11	-12	±13	+12	V
$V_{O\ p\text{-}p}$	-14	-14.4 to +13	+12	-10	±13	+10	V
A_{OL}	20K	—	—	20K	—	—	V/V

Features

- Internally compensated; needs no external components
- Wide bandwidth (4.5-MHz unity gain) makes possible low-cost video and audio circuits
- Fast settling time (1.4 μs typ. to 10 mV) for low-cost sample-and-hold and data-acquisition use
- Directly replaces industry types 741 (CA3140) and 1458 (CA3240) in most applications
- Characterized for ±15-V operation and for TTL supply systems down to 4 V
- High voltage-follower slew rate (9 V/μs)
- Strobable output stage
- Compared to BiFET devices, the CA3140 and CA3240 offer lower input currents, higher input resistance, improved offset current, and comparable offset voltage

Recommended Applications

- Ground-referenced single-supply amplifers in auto and portable instrumentation
- Long-duration timers/multivibrators (micro-seconds, minutes, hours)
- Interface in 5-V TTL systems and other low-supply-voltage systems
- All standard operational-amplifier applications
- Peak detectors
- Comparators
- Active filters
- Portable supplies

LIC Operational Amplifiers

BiMOS Types

- **CA3100 Wideband Op-Amp**
- **CA3160 Universal Op-Amp with Internal Compensation;**
- **CA3130 without Internal Compensation**

CA3160 Three technologies on a single chip;
CA3100 MOS/FET input stage, bipolar stage, and CMOS output stage

- CMOS output stage can swing output voltage to within 10 mV of either supply rail at very high values of load impedance

CA3130 PMOS and bipolar on a single chip

- Will handle both small and large signal inputs and still produce a true output virtually free of ringing and distortion

Symbol (TA = 25°C)	Min.	CA3100 ± 15 Volts Typ.	CA3100 ± 15 Volts Max.	CA3130/CA3160 ± 15 Volts Min.	CA3130/CA3160 ± 15 Volts Typ.	CA3130/CA3160 ± 15 Volts Max.	Units
R_I	—	—	—	30K	1500K	—	MΩ
I_I	—	0.7†	2†	—	5	50	pA
I_{IO}	—	0.05†	0.4†	—	0.5	30	pA
V_{IO}	—	1	5	—	6	15	mV
SR	50	70	—	—	10	—	V/μs
f_T	—	38	—	—	4	—	MHz
V_{ICR}	±12	+14 to −13	—	0	−0.5 to +12	+ 10	V
$V_{o\ p\text{-}p}$	−9	+11 to −11	+9	−0.01	−0.002 to +13.3	+12	V
A_{OL}	630	1.1K	—	—	50K	—	V/V

†microamperes

Features of CA3130, CA3160

- MOS/FET input features (See CA3140, CA3240)
- Wide bandwidth, typically 15 MHz for CA3130, 4 MHz for CA3160
- High slew rate: 10 V/μs typ. (unity-gain follower)
- High output current (I_o): 20 mA typ.
- High A_{OL}: 320,000 (110 dB) typ.

Features of CA3100

- High open-loop gain: 42 dB typ. at 1 MHz
- High unity-gain f_T: 38 MHz typ.
- Wide power bandwidth (V_o): 18 $V_{p\text{-}p}$ at 1.2 MHz
- High slew rate: 70 V/μs typ. (20-dB amplifier), 25 V/μs (unity-gain amplifier)
- Fast settling time: 0.6 μs typ.
- LM118, LM748, LM101 compatability

Recommended Applications

CA3130, CA3160

- High-input impedance comparators
- Ideal interface with digital CMOS
- Voltage followers
- Voltage regulators
- For other applications, see CA3140, CA3240

CA3100

- Video amplifiers
- Fast peak detectors
- Video pre-drivers
- Multivibrators
- Oscillators
- Meter driver amplifiers
- Oscillators

CA080, CA081, CA082, CA083, CA084 Series

BiMOS Replacements for Industry TL080 Series BiFET Types

The CA080 series offer lower input bias and offset currents, higher input impedances, and wider bandwidth than their BiFET counterparts and other pin-compatible op amps.

Features

- Very low input bias current (50 pA max.) and offset current (30 pA max.)
- Input impedance typically $10^{12}\Omega$
- Low input offset voltage (2mV typ.)
- Wide common-mode input voltage range
- Lower power consumption: 42mW (single amp. channel)
- High slew rate: 13v/us typ.
- Unity-gain bandwidth = 5 MHz (typ.)
- Wide output voltage swing: 25 volts
- Low distortion
- Short-circuit protection
- Noise voltage (1 kHz): 40 nV/$\sqrt{Hz}$
- Direct replacement for industry type TL080 series in most applications

Applications

- Inverters
- High-Q notch filters
- IC preamplifiers
- Unity-gain absolute value amplifiers
- Sample and hold amplifiers
- Active filters
- Low-current amplification circuits
- Data acquisition equipment
- AC voltmeters (front end)

Characteristics T_A=25°C	CA080 CA081 CA082 CA083 CA084	CA080A CA081A CA082A CA083A CA084A	CA080B CA081B CA082B CA083B CA084B	CA080 CA081 CA082	CA080A CA081A CA082A	Units
T_A Range	0-70	0-70	0-70	−55 to 125 °C		
V_{IO} (max.)	15	6	3	6	3	V
I_I (max.)	50	40	30	40	40	pA
I_{IO} (max.)	30	20	10	20	20	pA
I^+ (max.)	2.8*	2.8*	2.8*	2.8*	2.8*	mA
V_{ICR}(min.)	±10	±12	±12	±12	±12	V
A_{OL} (min.)	25K	50K	50K	50K	50K	V/V
f_T (typ.)	5	5	5	5	5	MHz
SR (typ.)	13	13	13	13	13	V/μs

*Per ampl CA3082, CA3083, CA3084

LIC Operational Amplifiers-OTAs

CA3280 Dual Variable OP AMP

The CA3280 series consists of two variable operational amplifiers that are designed to substantially reduce the initial input offset voltage and the offset-voltage variation with respect to changes in programming current. This design results in reduced "AGC thump", an objectional characteristic of many AGC systems. Interdigitation, or cross coupling of critical portions of the circuit reduces the amplifier dependence upon thermal and processing variables.

The CA3280 has all the generic characteristics of an operational voltage amplifier except that the forward transfer characteristic is best described by transconductance rather than voltage gain, and the output is current, not voltage. The magnitude of the output current is equal to the product of transconductance and the input voltage. This type of operational transconductance amplifier has gained wide acceptance as a gateable, gain-controlled building block for instrumentation and audio applications, such as linearization of transducer outputs, standardization of widely changing signals for data processing, multiplexing, instrumentation amplifiers operating from the nanopower range to high-current and high-speed comparators.

Features

- Low initial input-offset voltage: 500μV max. (CA3280A)
- Low Offset-voltage change versus I_{ABC}: <500 μV typ. for all types
- Low offset-voltage drift: 5 μV/C max. (CA3280A)
- Excellent matching of the two amplifiers for all characteristics
- Internal current-driven linearizing diodes reduce the external input current to an offset component
- Differential amplifier emitters brought out for use in emitter-coupled dual-differential amplifier applications
- Low noise: 8 nV/$\sqrt{Hz}$ @ 1 kHz typ.
- Low noise distortion: 0.4% THD typ.
- Two modes of gain control

Recommended Applications

- Voltage-controlled amplifiers
- Voltage-controlled filters
- Voltage-controlled oscillators
- Multipliers
- Demodulators Sample and hold
- Instrumentation amplifiers
- Function generators
- Triangle wave-to-sine wave converters
- Comparators
- Audio preamplifiers

Symbol (TA = 25°C)	Charactertics and Limits						Units
	CA3280			CA3280A			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
R_I	0.5	—	—	0.5	—	—	MΩ
I_B	—	3	8	—	3	8	μA
I_{IO}	—	0.3	0.7	—	0.3	0.7	μA
V_{IO}	—	0.7	3	—	0.25	0.5	mV
SR	—	125	—	—	125	—	V/μs
gm	—	16	22	—	16	22	mmho
V_{ICR} + / −	−13	—	13	−13	—	13	V
V_{OM} +	12	13.9	—	12.5	13.9	—	V
V_{OM} −	−12	−14.5	—	−13.5	−14.5	—	V
V_{ABC}	—	1.2	—	—	1.2	—	V

CA3060 Variable Op-Amp Array
CA3078 Micropower Op-Amp

CA3078: Low standby power assures operation from a single 1.5-V battery; a programmable input terminal permits tailoring the frequency response and slew rate without sacrificing power.

CA3060: 3 variable op-amps on one chip plus a zener bias regulator to control bias current or as a voltage-reference source for external circuits.

Symbol	Characteristics Limits, T_A = 25°C						Units
	CA3060 (ea. amplifier)			CA3078A			
	I_{ABC} = 100 μA			R_{SET}: 5.1 MΩ;I_Q: 20μA			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}	—	1	5	—	1.3	3.5	mV
I_{IO}	—	250	1000	—	0.5	2.5	μA
I_{IB}	—	2500	5000	—	7	12	nA
I_{OM}	150	240	—	—	±12	—	mA
V_{OM} +	12	13.6	—	5.1	5.3	—	V
V_{OM} −	12	14.7	—	5.1	5.3	—	V
V_{ABC}	—	0.66	—	—	—	—	V
g_{21}	30	102	—	—	—	—	mmho
CMRR	70	90	—	80	115	—	dB
V_{ICR}	+12 to −12	+13 to −14	—	−5 5	−5.5 to+5.8	—	V
SR	—	8	—	—	—	—	V/μs

CA3078 A_{OL}: 88 db min., 92 typ. dB

Features

CA3078

- Low standby power: as low as 700 nW
- Wide supply-voltage range: ±0.75 to ±15 V
- High peak output current: 6.5 mA min.
- Adjustable quiescent current
- Output short-circuit protection

CA3060

- Low power consumption: as low as 100μW/amplifier
- Independent biasing for each amplifier
- Programmable range of input characteristics
- Low input bias and input offset current
- No effect on device under output short-circuit conditions
- High foward trandsconductance

Recommended Applications

CA3078

- Portable electronics
- Medical electronics
- Instrumentation
- Telemetry

CA3060

- Active filters
- Gyrators
- Multiplexers
- Strobing and gating functions
- Sample-and-hold functions
- Mixers
- Comparators
- Modulators
- Multipliers

LIC Operational Amplifiers-OTAs

CA3094 Programmable Power Switch/Amplifier
CA3080 Programmable Op-Amp

- Input control permits user to vary voltage, power bandwidth, slew rate, input and output currents
- Devices can be programmed and/or signal-modulated for optimum gain, speed, bandwidth, power
- Outputs can "sink" or "source" currents
- Linear gain is adjustable over 3 decades of amplifier bias current I_{ABC}
- Standby power levels can be adjusted from below 10µW up to 30 mW

Symbol	Characterstics Limits, T_A = 25°C						Units
	CA3094			CA3080			
	I_{ABC} = 100 µA			I_{ABC} = 500µA			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}	—	0.4	5	—	0.4	5	mV
I_{IO}	—	0.02	0.2	—	0.12	0.6	µA
I_{IB}	—	200	500	—	2	5	µA
I_{OM}	—	—	—	350	500	650	µA
$+V_{OM}$	14.95	14.99	—	12	13.5	—	V
$-V_{OM}$	—	14.96	—	12	14.4	—	V
V_{ABC}	—	0.68	—	—	0.71	—	V
g_m	1.65	2.2	2.75	6.7	9.6	13	mmho
CMRR	70	110	—	80	110	—	dB
V_{ICR}	+12†	+13.8†		+12 to	+13.6	—	V
	-14‡	-4.5‡		-12	-14.6		
SR	500 (max. value) 0.7 (unity gain)			—	—	75	V/µs

† V^+ - 15V ‡ V^- = 15V

Features

CA3094

- Programmable: strobing, gating, squelching, agc capabilities
- Capable of delivering 3 W average or 10 W peak to external loads
- High current-handling capability: 100 mA avg., 300 mA peak
- Sensitivity controlled by varying bias current
- Power output of 0.6 W in high-power, single-ended class A amplifier (1.6 W dissipation)
- THD: 1.4% typ. (at 0.6 W class A)
- Designed for single or dual power supplies

CA3080

- Differential input, single-ended class A output
- I_{ABC} used for either gating or linear gain control
- Slew rate (unity gain, compensated): 50 V/µs
- Flexible supply voltage range: ±2 V to ±15 V
- Fully adjustable gain: 0 to $g_m R_L$ limit
- Tight g_m spread: 2:1 for CA3080, 1.6:1 for CA3094

Recommended Applications

CA3094

- Fire detection and instrusion alarm systems
- Portable GFI detectors • Function generators
- Temperature-measuring equipment
- Driver for complementary power transistors for audio use
- Battery-operated flashers • Power supplies

CA3080

- Communications equipment
- Function generators (1,000,000-to-1 sweep capability) • Peak detector instruments
- Battery-operated paging systems
- Audio-frequency synthesizers

LIC Voltage Comparators

Dual and Single Types

Symbol	Characteristics Limits: T_A = 25°C				Units
	Dual			Single	
	BiMOS CA3290,A,B			CA311	
	V+	Typ.	Max.	Max.	
V_{IO}	+5	7.5	20	—	mV
	±15	7.5	20	10	
I_{IB}	+5	3.5 pA	50 pA	—	nA
	±15	12	50 pA	250	
I_{IO}	+5	2 pA	30 pA	—	nA
	±15	7 pA	30 pA	50	
V_{ICR}	+5†	Typ. Value: V^+ -3.5 to V^- -1.5		—	V
	±15‡	Typ. Value: V^+ -3.4 to V^- -1.6		—	
I_{SINK}	+5	30	—	—	mA
V_{sat}	+5	0.12	0.4	—	V
T_R	±15 R	1.2	—	—	µS
	±15 F	200	—	200*	ns
CMRR	±15	44	562	—	µV/V
	+5	100	562	—	

†Min. value: V^+ -3.5 to V; ‡Min. value: V^+ -3.8 to V
R = Rising Edge F = Falling Edge *Typical
T_R = Response Time at R_L = 5.1 kΩ

Features

CA3290, CA3290A, CA3290B

- State-of-the-art design, first in the industry
- MOS/FET input/bipolar output BiMOS types
- Wide V_{ICR}, can be swung 1.5 V below the negative supply rail, permits single-supply operation
- Ultra-low input current (3.5 pA typ.), eliminates need for high-impedance buffer circuits
- Wide differential input voltage range (to ± 36 V), allows input circuits to operate at high V+
- No phase reversal of output signal when input transients go below ground
- Very low supply current drain (0.8 mA at +5 V)
- Low output saturation voltage (120 mV at 4 mA)
- 14-pin package to reduce stray capacitances between input and output circuits

CA311

- Directly interchangeable with National LM311 series and other 311 industry types

Recommended Applications

- High-source-impedance voltage comparators
- Long-time-delay circuits
- A/D converters
- Window detector circuits
- Zero-crossing detectors
- Positive and negative peak detectors

LIC Voltage Comparators

Quad and Programmable Types
Programmable Types with Memory

Symbol	Characteristics Limits: T_A = 25°C						Units
	CA3098			CA3099			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IO}(LR)	-15	-3	6	-8	-3	2	mV
V_{IO}(HR)	-10	±10	10	-5	±1	5	mV
V_{IO}(HR-LR)	—	3	20	—	3	10	mV
Temp. Coeff.	—	6.7	—	—	6.7	20	μV/°C
V_{CE}(sat)	—	0.72	1.2	—	0.72	1.2	V
I_T ON	500	710	800	600	710	800	μA
OFF	400	560	750	420	560	750	μA
I_{IB}	—	42	100	—	33	200	nA
$I_{OL(OFF)}$	—	—	10	—	—	10	μA
I_O	100	—	—	—	—	—	mA
t_d	—	600	—	—	600	—	ns
t_f	—	50	—	—	50	—	ns
t_r	—	500	—	—	500	—	ns
t_s	—	4.5	—	—	4.5	—	μs
V_{REF}	—	—	—	5.7	6	6.3	V
V_{REG}	—	—	—	6	7.2	8	V

Features

- Designed to control high-operating-current loads such as thyristors, lamps, relays, LED's
- Can be operated with single power supply (16 V max.) or dual power supply (± 8V)
- Directly control currents up to 150 mA
- Operate with microwatt standby power when current to be controlled is less than 30 mA
- Programmable operating current
- High sensor range: 100 ohms to 100 megohms
- Built-in hysteresis: 20 mV max. for CA3098, 10 mV max. for CA3099
- Programmable hysteresis: 20 mV to V^+ for CA3098, 10 mV to V^+ for CA3099
- Temperature-compensated reference voltage (CA3099)

Recommended Applications

- Signal reconditioning
- On-off motor switching
- Schmitt triggers, level detectors
- Time delays
- Overvoltage, overcurrent, overtemperature protection
- Battery-operated equipment

Quad Types

Sym-bol	Max. Characteristics Limits: T_A=25°C, V^+ =+5V				
	CA139	CA139,A	CA239,A	CA339,A	Units
V_{IO}	5	2	—	—	mV
I_{IO}	25	25	50	50	nA
I_{IB}	100	100	250	250	nA
V_{ICR}	V^+-1.5	V^+-1.5	—	—	V
I^+	2	2	—	—	mA
I_{OL}	0.1	0.1	—	—	nA
I_{OM}^-	16⁺	16⁺	—	—	mA

Features

- Direct replacements for industry types 139, 139A, 239, 239A, 339, 339A
- Low supply-current drain, suitable for battery operation
- Common-mode input-voltage range to ground

Recommended Applications

- Square-wave generators
- Pulse generators
- Time-delay generators
- High-voltage digital logic gates
- Multivibrators
- A/D converters
- MOS clock timers

Data Conversion Circuits

Display Drivers

- **CA3207 BiMOS Sequencer Driver**
- **CA3208 BiMOS Segment Latch-Driver**

The RCA CA3207 and CA3208 sequence-driver and segment latch-driver, respectively, are used in combination to drive vacuum fluorescent display devices of up to 14 characters of display. The CA3207 selects the digit or character to be displayed in sequence and the CA3208 turns on the required number of segments of the character selected.

Features

- Serial input, parallel output
- Total of 14 outputs
- CMOS and T^2L compatible inputs
- Low-power CMOS Logic-Bipolar high-voltage output BiMOS process
- Use with vacuum fluorescent display
- Will operate in an output voltage range of 35 V to 55 V

Sequencer Driver (CA3207E)

- Sequentially turns on 1 of 14 characters (or 2 of 28 when used with 2 CA3208E's)
- Signal dimming through Gates 1 or 2

Latch Driver (CA3208E)

- Drives any combination of 14 outputs selected by DATA input
- Two or more devices may be interconnected by means of the CE and $\overline{CE}$ inputs to drive more than 14 characters

CA3168 2-Digit BCD-to-7-Segment Decoder/Driver

The RCA CA3168 is a monolithic integrated circuit intended for 2-digit display such as "numbers" for TV and "CB" channel selection, and other 0-99 numerical or counting for consumer or industrial indicator applications.

Features

- Separate BCD inputs and segment outputs for each digit
- Input loading less than 15μA
- I^2L logic with buffered inputs and outputs
- Internal input overrange protection circuit
- 5-V supply operation
- Internal biasing circuits
- Output drive capability of 25 mA per segment
- Open collector outputs drive indicators directly

Data Conversion Circuits

A/D Converters

CA3300 CMOS Video Speed 6-Bit Flash A/D Converter
CA3308 CMOS Video Speed 8-Bit Flash A/D Converter

The RCA CA3300 and CA3308 are CMOS parallel (FLASH) A/D converters designed for applications demanding both low power consumption and high-speed digitization. They operate over a wide full-scale input-voltage range with maximum power consumption as low as 50 to 200 mW depending upon the clock frequency selected.

Features
- CMOS low power with speed
- Parallel conversion technique
- 15 MHz sampling rate (66-ns conversion time)
- ±½ LSB accuracy
- 2 units in parallel allow 30-MHz sampling rate

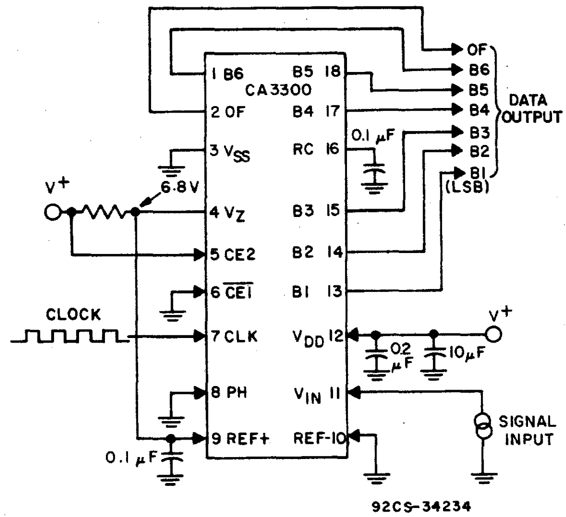
Recommended Applications
- The devices are especially suited for high-speed conversion applications where low power is also important
- High-speed A/D conversion
- Ultrasound signature analysis
- Transient signal analysis
- High-energy physics research
- High-speed oscilloscope storage/display
- General-purpose hybrid ACDs
- Optical character recognition
- Radar pulse analysis
- Motion signature analysis

Features *CA3300*
- 6-bit latched 3-state output with overflow bit
- Single supply voltage (3 to 10V)
- 2 units in series allow 7-bit output
- Internal VREF with ext VREF option

Applications
- TV video digitizing (industrial/security)

Features *CA3308*
- 8-bit latched 3-state output with overflow bit
- Single supply voltage (4 to 8 V)
- 2 units in series allow 9-bit output

Applications
- TV video digitizing (industrial/security/broadcast)
- μP data acquisition systems



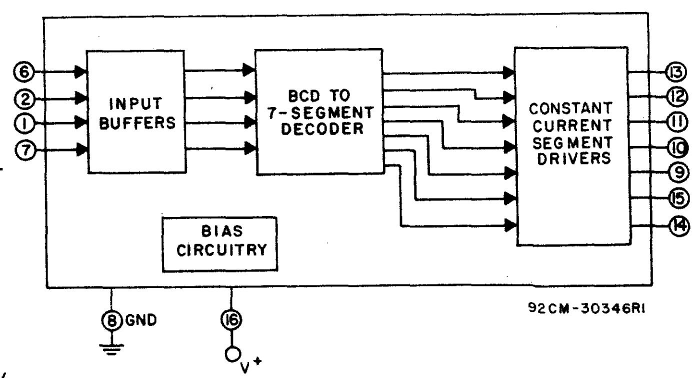
Typical CA3300 6-bit configuration 15-MHz sampling rate.

CA3161 BCD-to-Seven-Segment Decoder/Driver
CA3162 Converter for 3-Digit Digital Readout System

The CA3162E analog-to-digital converter is specially designed for use in low-cost digital readout systems. This circuit and a companion type, the CA3161E BCD-to-7-segment decoder/driver, can be used to implement a 2-chip, 3-digit readout system featuring simplicity of operation and a minimum of external parts. The CA3162E provides highly accurate conversions, exceptional temperature stability, and other features listed below.

Features *CA3162E*
- Dual-slope A/D conversion for excellent accuracy and noise rejection
- On-chip clock and ultra-stable bandgap reference; no additional IC's required
- Reads 99 mV below ground with single +5 V supply
- Choice of low-speed (4-Hz) or high-speed (96-Hz) conversion rate
- Overrange indication
- I²L technology
- Hold function inhibits conversion but maintains display

CA3161E
- TTL-compatible input logic levels
- 15-mA typ. constant-current output drive, eliminates need for current-limiting resistors
- Pin-compatible with industry standard decoders



CA3161 Block Diagram

Recommended Applications
- Medical equipment
- Welding controls
- Electronic scales
- Electronic games
- Temperature measuring instruments
- Power-supply meters
- Analog panel meters
- Auto Accessories
- Industrial Controls

LIC Amplifier, Transistor/Diode, and Diode Arrays

Features

- CA3093 has high I_C (100 mA max. each transistor) and temperature-compensation capability
- CA3097 has PUT with extremely long time constants, SCR with 150-mA forward current, complete isolation between elements
- CA3019 has excellent diode match, low leakage currents, low pedestal voltage when gating
- CA3039 has ultra-low capacitance diodes: 1 ns typ. reverse recovery time, C_D=0.65 pF typ., V_F matched within 5 mV
- CA3141 has $V_{BR(R)}$ of 30 V min., low I_R of 100 nA max., low C_D of 0.3 pF typ., V_F of each diode pair matched to within 0.55 mV at 1-mA I_F
- CA3048, CA3052 include internal dc feedback and bias to provide temperature-stabilized operation

Recommended Applications

- Lamp and relay drivers, differential amplifiers, temperature-compensated amplifiers
- Timers, light dimmers/motor controls, comparators, Schmitt triggers, constant-current sources
- Analog switches, balanced modulators, mixers, diode gates for chopper modulators
- Balanced modulators or demodulators, ring modulators, high-speed diode gates
- Current-ratio detectors, high-voltage diode gates, analog switches
- Low-level preamplifiers, mixers, tone generators, linear signal mixers

Amplifier Types				Transistor/Diode Types		Diode types		
Dual independent Differential	**4 AC Amplifiers**	**3 Variable Operation Amplifiers**	**Quad Operational Amplifier**	**3 n-p-n Transistors 2 Zener Diodes 1 Diode**	**1 n-p-n, 1 p-n-p/n-p-n pair, 1 Zener Diode, 1 PUT 1 SCR**	**1 Quad Plus 2**	**6 Ultra-Fast Low Capacitance**	**10 High-Voltage (5 Pairs)**
CA3026 CA3049# CA3102#	CA3048 CA3052	CA3060 CA3060A	CA124 CA224 CA324	CA3093	CA3097	CA3019	CA3039	CA3141
CA3054	2 Darlington Differential Amplifiers with Diode Bias String CA3050, CA3051							
#High Frequency								

LIC Transistor Arrays

Features

- CA3081, CA3082 directly drive 7-segment displays
- CA3127, CA3102, CA3049 are useful in low-power applications up to 500 MHz; low 1/f noise; f_T greater than 1 GHZ
- CA3227, CA3246 consist of five general-purpose silicon n-p-n transistors on a common monolithic substrate, f_T greater than 3GHz
- CA3600 (PMOS and NMOS devices) is specified and tested for linear circuit applications

Each transistor can conduct currents up to 10 mA.

High input resistance (100 GΩ typ.).

Recommended Applications

- Drivers for incandescent display devices, relay controls, thyristor firing
- VHF amplifiers, mixers, rf mixers/oscillators, doubly balanced modulators/demodulators
- Core-memory drivers, high-speed switching, high-current LED drivers, lamp drivers
- For complementary-symmetry circuits at supply voltages of 3 to 15 V and frequencies up to 5 MHz (untuned)
- High-input-impedance, general-purpose amplifiers, preamplifiers, differential amplifiers
- IF converter, IF amplifier, sense amplifiers, synthesizers, synchronous detectors, cascade amplifiers

High-Current		Bipolar Types (▲ High-Beta Types) High-Voltage				General-Purpose			CMOS Type
7 n-p-n Common Collector	CA3082	5 Independent-3 n-p-n 2 p-n-p	5 Independent n-p-n	Darlington-Connected Pair Plus 2 Independent n-p-n	Differentially Connected Pair Plus 3 Independent n-p-n	Darlington-Connected Pair Plus 2 Independent n-p-n	Differentially Connected Pair Plus 3 Independent n-p-n	5 Independent n-p-n	3 n-Channel and 3 p-Channel
7 n-p-n Common Emitter	CA3081								
5 Independent n-p-n	CA3083 CA3183 CA3183A	CA3096 CA3096A CA3096C	CA3183 CA3183A	CA3118 CA3118A	CA3146 CA3146A	CA3018 CA3018A	CA3045 CA3046 CA3086	CA3227 CA3246	CA3600
4 Isolated n-p-n	CA3138▲ CA3138A▲ CA1724 CA1725	High-Frequency CA3127				1 Darlington Pair, 1 Current Mirror Pair, 2 p-n-p, 1 Shared Diode CA3084			

LINEAR

RCA

LIC Power Control Circuits

Automotive Ignition Switch

• CA3165 Electronic Switching Circuit

The RCA CA3165 is a single-chip electronic switching circuit intended primarily for ignition applications. It includes an oscillator that is amplitude-modulated by the rotor teeth of a distributor, a detector that develops the positive-going modulation envelope, a Schmitt trigger that eliminates switching uncertainties.

Features

- Switching initiated by damping of internal oscillator
- Proximity sensing of rotational motion
- Repeatable timing of switching states
- Five outputs — two complementary pairs and one non-inverting output (CA3165E1)
- Two outputs — one complementary pair (CA3165E)

Solenoid & Motor Driver

• CA3169 Solenoid and Motor Driver

The RCA CA3169 is a monolithic integrated circuit capable of driving lamps and other devices that can be changed between two states (on or off). Transistors, SCRs, and triacs are some of the solid-state devices that can be controlled by the CA3169. The device also can control relays, solenoids (latching or non-latching), motors (DC-forward and reverse) and DC stepping motors.

Features

- Chip encapsulated in a 5-lead plastic TO-220-style package (VERSA-VI)
- Output short-circuit protection
- Thermal overload protection
- Solenoid inductive "kick" protection with internal-clamp diodes
- Output sink and source capacity of 600-mA minimum overtemperature
- Horizontal and vertical mounting packages available.
- Separate sink circuit and source circuit, each individually controlled
- Inputs can be driven by TTL logic levels and CMOS logic levels
- Low V_{CE}(sat)

Applications

- Latching solenoid driver (single and multiple)
- Non-latching solenoid driver
- Relay driver
- Lamp controller
- Lamp driver
- Motor controller (forward and reverse)
- Stepper motor controller
- On-off logic controllers (TTL logic)
- Intermediate power driver
- Triac, SCR, and transistor drivers

• CA3219 Quad-Power NAND Driver

The RCA CA3219 quad power NAND driver contains four NAND gate switches for interfacing low-level logic to inductive and resistive loads such as: relays, solenoids, AC and DC motors, heaters, incandescent displays, and vacuum fluorescent displays.

Features

- Driven outputs capable of switching 600 mA load currents without spurious changes in output state
- Inputs compatible with TTL or 5-volt CMOS logic
- Suitable for resistive or inductive loads

Universal Controller

• CA3228 Speed-Control System

The RCA CA3228 is a monolithic I^2L integrated circuit designed as an automotive speed-control system. The system monitors vehicle speed and compares it to a set reference speed. Any deviation in vehicle speed causes a servo mechanism to open or close the engine throttle as required to eliminate the speed error. The reference speed is set by the driver to hold the existing speed and stored in a 9-bit counter.

Features

- Low power dissipation
- I^2L control logic
- Power-ON reset
- On-chip oscillator for system time reference
- Single line command
- Amplitude encoded control signals
- Transient compensated input commands
- Controlled acceleration mode
- Internal redundant brake and low speed disable
- Braking disable

Voltage Regulators

Features *CA723, CA723C*

- Up to 150 mA output current
- Regulation in excess of 10 A with suitable pass transistors
- Input and output short-circuit protection
- Load and line regulation of 0.03%
- Adjustable output voltage of 2 V to 37 V
- Direct replacements for 723, 723C industry types

Features *CA3085, CA3085A, CA3085B*

- Up to 100 mA output current
- Regulation up to 12 mA without pass transistors, in excess of 100 mA with suitable pass transistors
- Load and line regulation of 0.025%
- Low noise • Frequency compensation
- Input and output short-circuit protection
- Temperature-compensated reference voltage
- Pin-compatible with LM100 series

Recommended Applications

- Series and shunt voltage regulators
- Current regulators • Floating regulators
- Temperature controllers
- High-current voltage regulators
- Dual-tracking regulation
- Combination positive and negative voltage regulators

Features *CA1524, CA2524, CA3524*

- Complete PWM power control Circuitry
- Separate outputs for Single-ended or push-pull operation
- Line and load regulation of 0.2% typ.
- Internal reference supply with 1% max. oscillator and reference voltage variation over full temperature range
- Standby current of less than 10 mA
- Frequency of operation beyond 100kHz
- Variable output dead time of 0.5 to 5 μs
- Low V_{CE}(sat) over the temperature range

Recommended Applications

- Positive and negative regulated supplies
- Dual-output regulators
- Flyback converters
- DC-DC transformer-coupled regulating converters
- Single-ended DC-DC converters
- Variable power supplies

LIC Power Control Circuits

Zero-Voltage Switches

Features

CA3058, CA3059, CA3079

- Operation at 24 V, 120 V, 208/230 V, 227 V at 50, 60, or 400 Hz
- Differential on-off sensing amplifier
- Zero-crossing detector • Triac gating circuit
- Low balanced input current: 1 μA max.
- Built-in protection circuit for open or shorted sensor
- Differential input
- Sensor range of 2 to 100 kilohoms

Recommended Applications

CA3058, CA3059, CA3079

- Relay control • Valve control • Lamp control
- Synchronous switching of flashing lights
- On-off motor switching
- Differential comparators with self-contained power supply for industrial applications
- Photosensitive controls
- Power one-shot controls

LIC Differential Amplifiers

Features

- Balanced differential-amplifier configuration with controlled constant-current source
- RF, if, and video frequency capability
- Balanced agc capability
- Operation from dc to 120 MHz
- CA3028B is controlled for input offset voltage, current, and input bias current, and is intended for "balance" requirements
- CA3005 and CA3006 are identical except for input offset voltage

Applications

- RF amplifiers • Oscillators
- Mixers • Limiters
- IF amplifiers • Product detectors
- Frequency generators • Pulse amplifiers
- Preamplifiers for low-level transducers
- DC, audio, and sense amplifiers

	T_A = 25°C; V^+ = 6V Unless Otherwise Specified						
Type	V_{IO} Max. mV	I_{IO} Max. μA	I_{IB} Max. μA	P_D Typ. mW	G_P# Typ. dB	NF# Typ. dB	CMR‡ Typ. dB
CA3005	5	1.4*	40	26	20	7.8	101
CA3006	1	1.4*	40	26	20	7.8	101
CA3028A	—	—	70	36	20†	7.2†	—
CA3028B	5	5	40	36	20†	7.2†	110
CA3053	—	—	—	50†	39★	—	—

*Typical #f 100 MHz ‡f 1.75 MHz †V^+ 9 V
★V^+ 9 V, f 10.7 MHz

LIC Special Function Circuits

Prescalers

CA3179E

The RCA-CA3179E is an integrated-circuit prescaler intended for use in communications and instrumentation systems, it performs division by 256 in the uhf mode and division by 64 in the vhf mode.

Features

- Broadband operation — DC to 1.25 GHz
- High sensitivity
- Standard T^2L or ECL power supply
- Dual mode operation — VHF/UHF (÷64/÷256)
- Complementary ECL outputs
- Independent VHF and UHF input terminals

CA3199E

The CA3199E is a bipolar integrated fixed-ratio (divide-by-four) counter which operates over the VHF/UHF frequency band (DC to 1.3 GHz). It accepts either single or double-ended ac-coupled input signals and provides complementary emitter follower outputs at sandard ECL logic levels.

Features

- Broadband operation — DC to 1.3 GHz
- High sensitivity
- Standard TTL or ECL power supply of 5V ± 0.5%
- Complementary ECL outputs

Applications *CA3179E, CA3199E*

- Digital frequency synthesizers for: VHF/UHF receivers, Satellite communications, instrumentation
- High-frequency divider for: UHF frequency counters, UHF timers, High-speed computers, Frequency standards, SHF second IF local-oscillator injection, PCM communications, Satellite communications, Radar ranging systems
- High-frequency up-converters

CA3211

The RCA-CA3211E is an integrated-circuit prescaler intended for use in TV frequency synthesis tuning systems over an input frequency range of 90 to 1000 MHz. It performs division by 256 in the UHF and VHF mode.

Features

- Divide by 256
- Input frequency to 1 GHz
- Dual input ports electrically selectable
- Input sensitivity
  $<$10 μW typical
  (Generator available power into a 50-Ω load)
- 5-V power supply
- Balanced output ports

LIC Special Function Circuits

Four Quadrant Multiplier

CA3091

Four-quadrant multiplier that provides an output voltage that is the product of two input (x and y) voltages

Features

- Accuracy of ±4% max.
- Internal bias regulator
- Linearity of 3% max.
- 3-dB bandwidth of 4.4 MHz
- Low-power operation capability: ±6 V, 4-mW drain
- Low power-supply sensitivity: 36 mV/V typ.
- Functions as a multiplier, divider, squarer, square-rooter, power-series approximator

Applications

- Ideal full-wave rectifiers
- Automatic level controllers
- Frequency discriminators
- RMS converters
- Voltage-controlled filters and oscillators

Single-Chip Detector Alarm Systems

CA3164E

The RCA CA3164 is a monolithic BiMOS integrated circuit designed to meet the stringent system requirements of a battery- or line-operated alarm circuit. When used with an ionization chamber and electromechanical or piezoelectric horn, it provides a one-chip approach to smoke detection.

Features

- Interfaces directly with high Z sensors — no external buffer FET required
- Low input current: 1 pA max.
- Gate-protected input terminals
- On-chip beep oscillator for low battery indication
- Self-contained low-battery-voltage detection circuit
  (a) Fixed or adjustable trip point available
  (b) Dynamic battery test when filter capacitor =2μF
- Chamber trigger voltage independent of battery supply voltage (less than 150 mV over temperature and supply variations)
- Reference source current available =5μA (typ.)
- Low standby battery current = 8 μA (typ.)
- Can be used with photoelectric sensors by using a minimum of external passive components in combination with the RCA-CA3078 micropower op-amp
- Multiple-unit interconnect terminal controls a common annunciator circuit
  (a) A fault to ground doesn't prevent local operation
  (b) The low battery alarm signal triggers only the local unit
- LED output indicates status of smoke-detector circuit
- Operates from 11 V (max.) supply (either battery or line)
- Battery reversal protection feature

Timer

CA555, CA555C Types

The RCA-CA555 and CA555C are highly stable timers for use in precision timing and oscillator applications. As timers, these monolithic integrated circuits are capable of producing accurate time delays for periods ranging from microseconds through hours.

Features

- Accurate timing from microseconds through hours
- Astable and monostable operation
- Adjustable duty cycle
- Output capable of sourcing or sinking up to 200 mA
- Output capable of driving TTL devices
- Normally ON and OFF outputs
- High-temperature stability — 0.005%/°C
- Directly interchangeable with SE555, NE555, MC1555, and MC1455

Applications

- Precision timing
- Sequential timing
- Time-delay generation
- Pulse generation
- Pulse-width and position modulation
- Pulse detector

TV/CATV Circuits

AFT	**HORIZONTAL/VERTICAL SYSTEMS**	**MULTIPLEX DECODERS**	**SOUND IF**	**TUNING**
CA3064	CA920A	CA758	CA1190	CA3140
CA3139	CA1391	CA1310A	CA1191	CA3152
CHROMA SYSTEMS	CA1394	CA3195	CA2111A	CA3163
CA1398	CA3154	**PIX IF**	CA2136A	CA3166
CA3070	CA3159	CA270	CA3011	CA3168
CA3071	CA3202	CA1352	CA3012	CA3199
CA3072	CA3210	CA3068	CA3013	CA3211
CA3121	CA3223***	CA3136	CA3014	**VIDEODISC CIRCUITS**
CA3126	**SYNC/AGC CIRCUITS**	CA3153	CA3042	CA2111A
CA3128**	CA3120	CA3191	CA3065	CA3215
CA3137	CA3142	CA3192	CA3134	CA3216
CA3145	**LUMINANCE PROCESSORS**	CA7607		CD3226A@
CA3151	CA3135	CA7611		
CA3158	CA3143			
CA3170	CA3144			
CA3172	CA3156			
CA3194**				
CA3201				
CA3217				
CA3221				

@CMOS types, *BiMOS types, **PAL types, ***625 line

12-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

Am6012

Preliminary

DESCRIPTION

The Am6012 12-Bit multiplying Digital-to-Analog converter provides high speed and 0.025% differential nonlinearity over its full commercial temperature range.

The D/A converter uses a 3-bit segment generator for the MSBs in conjunction with a 9-bit R-2R diffused resistor ladder to provide 12-bit resolution without costly trimming processes. This technique guarantees a very uniform step size (up to ± ½ LSB from the ideal), monotonicity to 12 bits and integral nonlinearity to 0.05% at its differential current outputs.

The dual complementary outputs of the Am6012 increase its versatility, and effectively double the peak-to-peak output swing. Digital inputs, in addition, can be configured to accept all popular logic families.

While the device requires a reference input of 1mA for a 4mA full scale current, operation is nearly independent of power supply voltage shifts. The power supply rejection ratio is ±0.001%FS/% ΔV. The devices will work from +5, −12V to ±18V rails, with as low as 230mW power consumption typical.

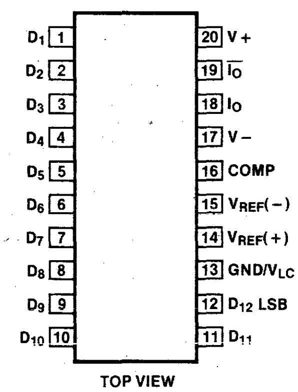
FEATURES

- **12-bit resolution**
- **Accurate to within ±0.025%**
- **Monotonic over temperature**
- **Fast settling time, 250ns typical**
- **Trimless design for low cost**
- **Differential current outputs**
- **High-speed multiplying capability**
- **Full scale current, 4mA (with 1mA reference)**
- **High output compliance voltage, −5 to +10V**
- **Low power consumption, 230mW**

APPLICATIONS

- **CRT displays, computer graphics**
- **Robotics, and machine tools**
- **Automatic test equipment**
- **Programmable power supplies**
- **CAD/CAM systems**
- **Data acquisition and control systems**
- **Analog-to-Digital converter systems**

PIN CONFIGURATION

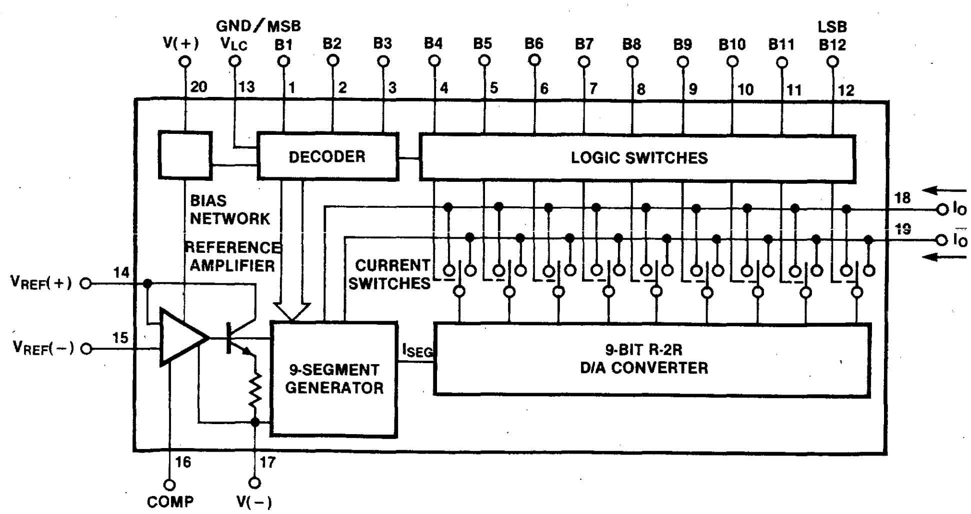


ORDER NUMBER
AM6012F

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	
Am6012F	0°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
Power Supply Voltage	±18V
Logic Inputs	−5V to +18V
Voltage Across Current Outputs	−8V to +12V
Reference Inputs V_{14}, V_{15}	V− to V+
Reference Input Differential Voltage (V_{14} to V_{15})	±18V
Reference Input Current (I_{14})	1.25mA

BLOCK DIAGRAM



8-BIT HIGH SPEED MULTIPLYING D/A CONVERTER

DAC-08 SERIES

FORMERLY: NE5007/5008-F,N
SE5008-F

DESCRIPTION

The DAC-08 series of 8-bit monolithic multiplying Digital-to-Analog Converters provide very high speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85ns settling times with very low glitch and at low power consumption. Monotonic multiplying performance is attained over a wide 20 to 1 reference current range. Matching to within 1 LSB between reference and full scale currents eliminates the need for full scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

Dual complementary outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. True high voltage compliance outputs allow direct output voltage conversion and eliminate output op amps in many applications.

All DAC-08 series models guarantee full 8-bit monotonicity and linearities as tight as 0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±4.5V to ±18V power supply range, with 33mW power consumption attainable at ±5V supplies.

The compact size and low power consumption make the DAC-08 attractive for portable and military/aerospace applications.

FEATURES

- **Fast settling output current—70ns**
- **Full scale current prematched to ±1 LSB**
- **Direct interface to TTL, CMOS, ECL, HTL, PMOS**
- **Relative accuracy to 0.1% maximum over temperature range**
- **High output compliance −10V to +18V**
- **True and complemented outputs**
- **Wide range multiplying capability**
- **Low FS current drift—±10ppm/°C**
- **Wide power supply range—±4.5V to ±18V**
- **Low power consumption—33mW at ±5V**

APPLICATIONS

- **8-bit, 1μs A-to-D converters**
- **Servo-motor and pen drivers**
- **Waveform generators**
- **Audio encoders and attenuators**
- **Analog meter drivers**
- **Programmable power supplies**
- **CRT display drivers**
- **High speed modems**
- **Other applications where low cost, high speed and complete input/output versatility are required**
- **Programmable gain and attentuation**
- **Analog-Digital Multiplication**
- **Stepping motor drive**

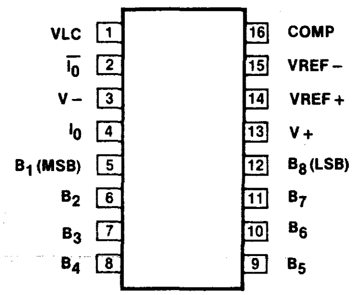
ORDERING INFORMATION

RELATIVE ACCURACY	0 to 70°C	−55 to 125°C
0.39% FS	DAC-08CN	
	DAC-08CF	
0.19% FS	DAC-08EN	
	DAC-08EF	DAC-08F
	DAC-08ED	
0.1% FS	DAC-08HF	DAC-08AF
	DAC-08HN	

$T_A = 25°C$ unless otherwise noted

PIN CONFIGURATION

F,N PACKAGE

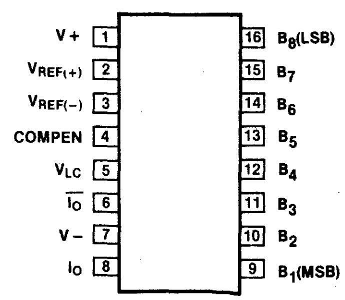


TOP VIEW

ORDER NUMBER

DAC-08AF	SE5009F
DAC-08F	SE5008F
DAC-08HF,N	NE5009F,N
DAC-08CF,N	NE5007F,N

D PACKAGE



TOP VIEW

ORDER NUMBER

DAC-08ED

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
T_A	Operating temperature range		°C
	DAC-08, DAC-08A	-55 to +125	
	DAC-08C, E, H	0 to +70	
t_{stg}	Storage temperature	-65 to +150	°C
P_D	Power dissipation	500	mW
	Lead soldering temperature (60sec)	300	°C
	V+ to V- supply	36	V
	Logic inputs	V- to V- plus 36V	
V_{LC}	Logic threshold control	V- to V+	
	Analog current outputs	See output current or output voltage performance curve	
V_{14}, V_{15}	Reference inputs	V- to V+	
V_{14} to V_{15}	Reference input differential voltage	±18	V
I_{14}	Reference input current	5.0	mA

8-BIT μP-COMPATIBLE D/A CONVERTER

NE/SE5019

DESCRIPTION

The NE5019 is a complete 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most micro-processors.

The chip also comprises a stable voltage reference (5V nominal) and a high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

FEATURES

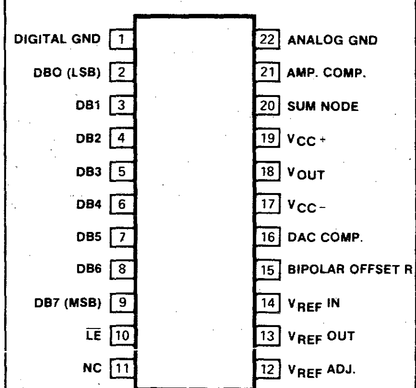
- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Output buffer amplifier**
- **Accurate to ± 1/4 LSB (.1%)**
- **Monotonic to 8 bits**
- **Amplifier and reference both short-circuit protected**
- **Compatible with 8085, 6800 and many other μP's**

APPLICATIONS

- **Precision 8-bit D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog-digital multiplication**

PIN CONFIGURATION

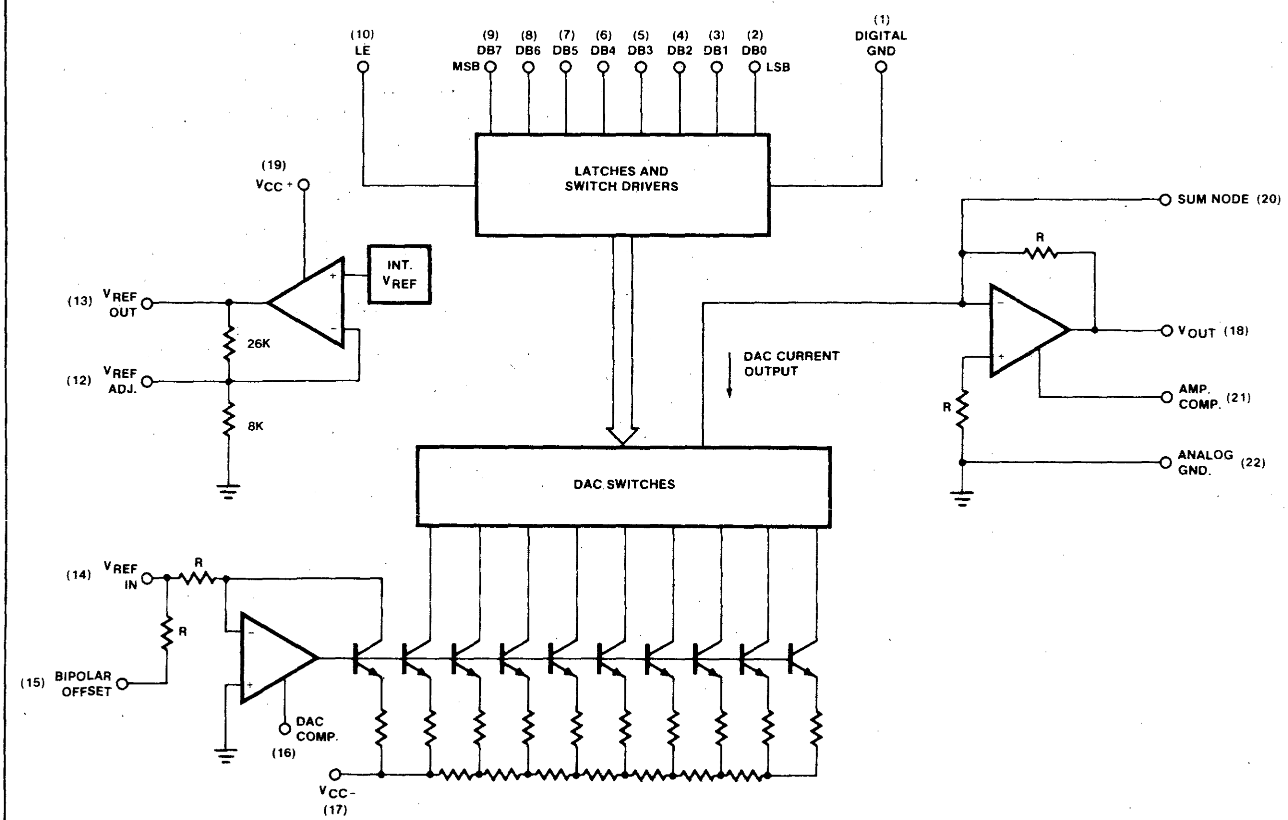
F,N PACKAGE



TOP VIEW

ORDER NUMBERS
NE5019F SE5019F
NE5019N

BLOCK DIAGRAM



All R values equal 5KΩ and are thermally matched.

Figure 1

10-BIT μP-COMPATIBLE D/A CONVERTER

NE5020

DESCRIPTION

The NE5020 is a microprocessor-compatible monolithic 10-bit digital to analog converter subsystem. This device offers 10-bit resolution and ±0.1% accuracy and monotonicity guaranteed over full operating temperature range.

Low loading latches, adjustable logic thresholds and addressing capability allow the NE5020 to directly interface with most microprocessor and logic controlled systems.

The NE5020 contains internal voltage reference, DAC switches and resistor ladder. Also, the input buffer and output summing amplifier are included. In addition, the matched application resistors for scaling either unipolar or bipolar output values are included on a single monolithic chip.

The result is a near minimum component count 10-bit resolution DAC system.

FEATURES

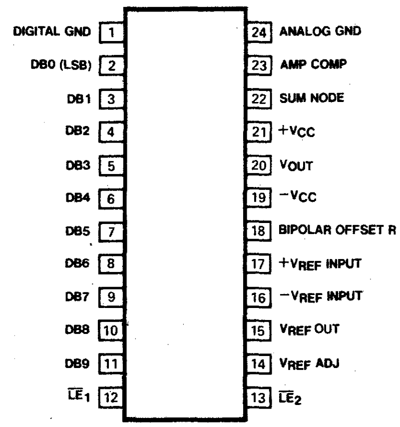
- **10-bit resolution**
- **Guaranteed monotonicity over operating range**
- **±0.1% relative accuracy**
- **Unipolar (0V to +10V) and Bipolar (±5V) output range**
- **Logic bus compatible**
- **5μsec settling time**

APPLICATIONS

- **Precision 10-bit D/A converters**
- **10-bit Analog to Digital converters**
- **Programmable power supplies**
- **Test equipment**
- **Measurement instruments**

PIN CONFIGURATION

F, N PACKAGE



ORDER NUMBERS
NE5020F
NE5020N

BLOCK DIAGRAM

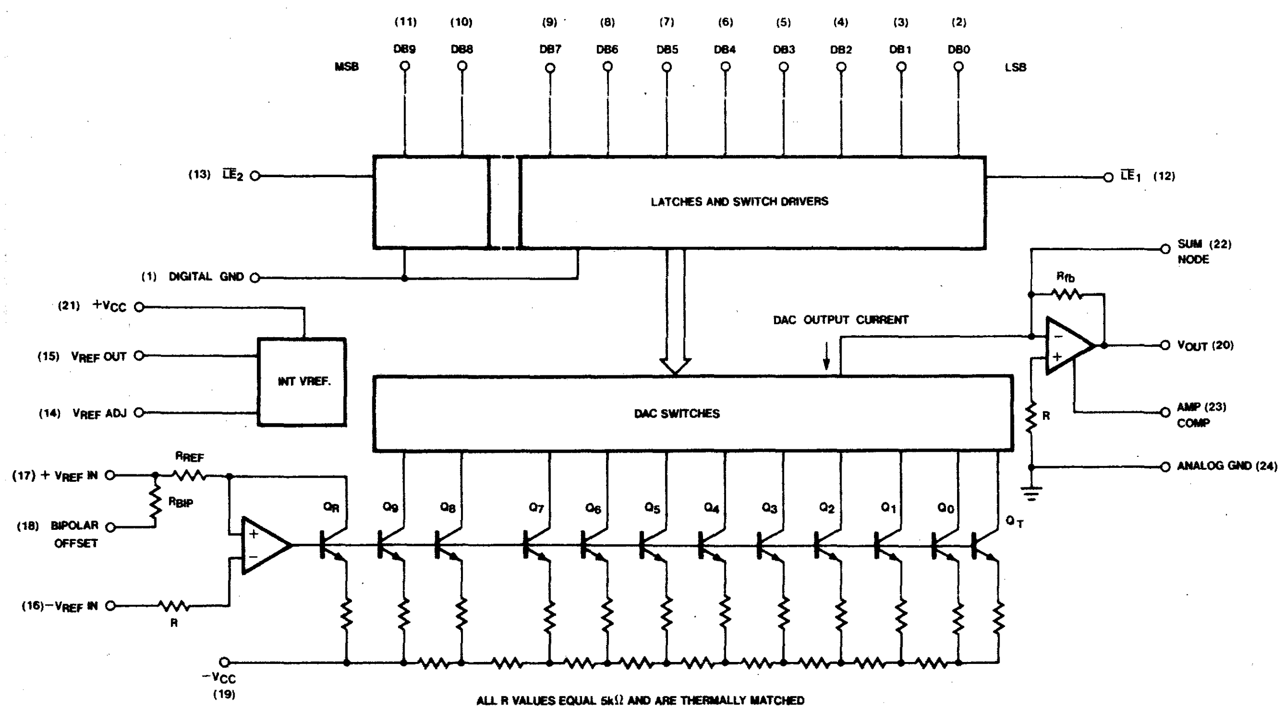


Figure 1

LINEAR

Signetics

8-BIT GENERAL PURPOSE A/D CONVERTER

NE5034

DESCRIPTION

The NE5034 is a high-speed microprocessor-compatible 8-bit Analog-to-Digital converter. It uses the successive approximation conversion technique, and includes the comparator, reference DAC, SAR, an internal clock and three-state buffers all on the same chip.

The converter can accommodate a wide analog input voltage range, bipolar or unipolar, selectable through external input resistors. An external capacitor controls the internal clock frequency, providing conversion times down to 17μs. Faster conversion times are possible using an external clock.

Microprocessor interfacing requirements are simple, allowing analog-to-digital conversion with a minimum of external components.

FEATURES

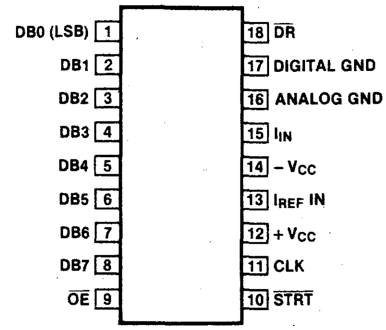
- **8-bit resolution and accuracy**
- **Accepts unipolar or bipolar inputs**
- **Three-state output buffers for easy microprocessor interface**
- **Choice of internal or external clocking**
- **Short conversion time, 17μs typical using internal clock**

APPLICATIONS

- **All microprocessor-based monitoring and control systems requiring analog signal inputs.**
- **Typical applications include: Automated process control, machine tools, robots, test and measurement instruments, environmental controls**
- **Other applications include: Ratiometric A/D conversion, very high resolution A/D conversion systems requiring high speed 8-bit building blocks**

PIN CONFIGURATION

F PACKAGE



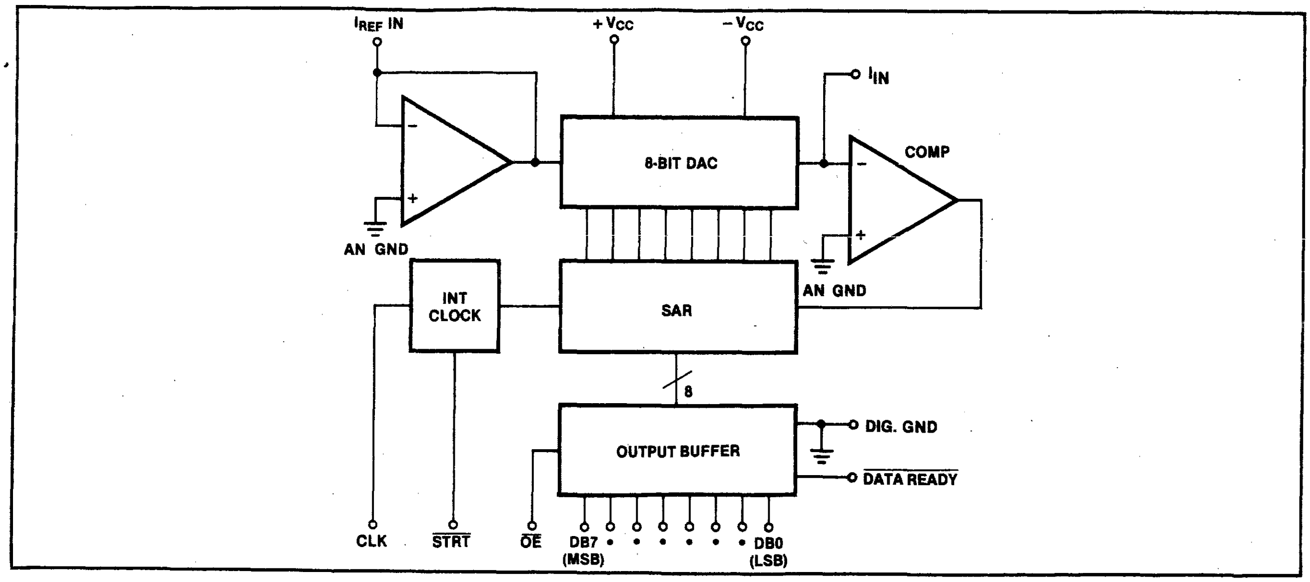
TOP VIEW

ORDER NUMBERS
NE5034F

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
$V_{CC}+$	Positive supply voltage	0 to +6	V
$V_{CC}-$	Negative supply voltage	0 to −15	V
I_{REF}	Reference current	1.5	mA
I_{IN}	Analog input current	5.0	mA
V_O	Data output voltage	6.0	V
Analog GND to Digital GND		1.0	V
V_L	Logic input voltage	−1 to $V_{CC}+$	V
P_D	Power dissipation		
	F package	1000	mW
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

BLOCK DIAGRAM



6-BIT A/D CONVERTER (PARALLEL OUTPUTS) NE5037

DESCRIPTION

The NE5037 is a low cost, complete successive approximation analog to digital (A/D) converter, fabricated in Bipolar/I^{2}L technology. With an external reference voltage, the NE5037 will accept input voltages between 0V and V_{REF}. An external $\overline{START}$ pulse of at least 300ns in duration will provide the 6-bit result of the conversion in parallel format. Full conversion with no missing codes occurs in 9μs.

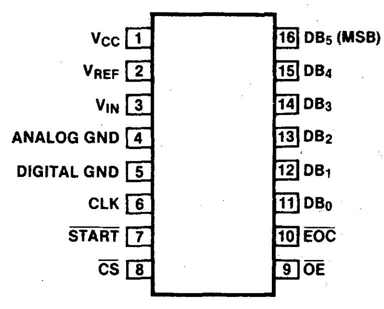
FEATURES

- **T^{2}L compatible inputs and outputs**
- **Three state output buffer**
- **Easy interface to CMOS μProcessors**
- **Fast conversion—9μs**
- **Guaranteed no missing codes over full temp range**
- **Single supply operation, +5V**
- **Positive true binary outputs**
- **High impedance analog inputs**

APPLICATIONS

- **Temperature control**
- **μP-based appliances**
- **Light level monitors**
- **Head position sensing**
- **Electronic toys**
- **Joystick interface**

PIN CONFIGURATION

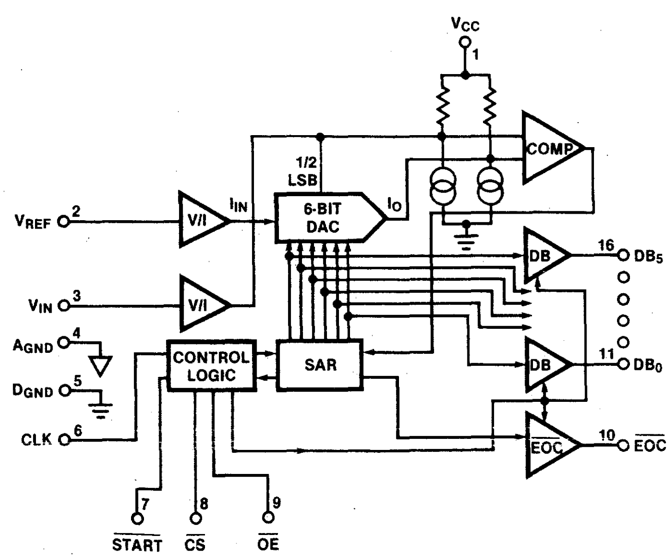


ORDER NUMBERS
NE5037F, NE5037N
NE5037D

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	7	V
V_{REF}	Reference voltage	7	V
$V_{IN\,(Analog)}$	Analog input voltage	7	V
$V_{IN\,(Digital)}$	Digital input voltage ($\overline{CS}$, $\overline{OE}$, $\overline{START}$, CLK)	7	V
D_{OUT}	Data outputs (DB0 to DB5)		
	Three-state mode	7	V
	Enabled mode (each output)	5	mA
$\overline{EOC}$	End of conversion	V_{CC}	
Δ_{GND}	Analog GND to digital GND	±1	V
T_A	Operating temperature range	0 to 70	°C
T_{STG}	Storage temperature range	−65 to 150	°C
t_{SOLD}	Lead soldering temperature (10 seconds)	300	°C
P_D	Power dissipation		
	F package	220	mW
	N package	220	mW

BLOCK DIAGRAM



8-BIT μP-COMPATIBLE D/A CONVERTER—CURRENT OUTPUT NE/SE5119

DESCRIPTION

The NE5119 is a high-speed 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most microprocessors.

The chip also comprises a stable voltage reference (5V nominal). The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output has high voltage compliance increasing versatility.

FEATURES

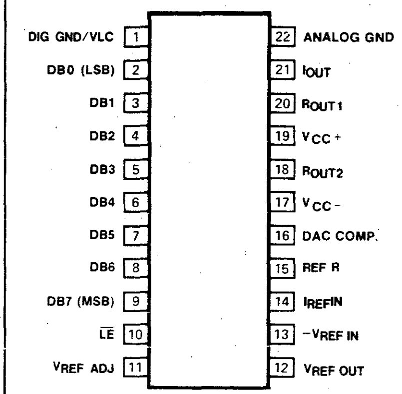
- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Fast settling output current—200ns**
- **Accurate to ± 1/4 LSB (.1%)**
- **Monotonic to 8 bits**
- **Reference short-circuit protected**
- **Compatible with 8086, 6800 and many other μP's**

APPLICATIONS

- **Precision 8-bit D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- ~~**Measuring instruments**~~
- **Analog-digital multiplication**
- **CRT display drivers**
- **High-speed modems**

PIN CONFIGURATION

F,N PACKAGE



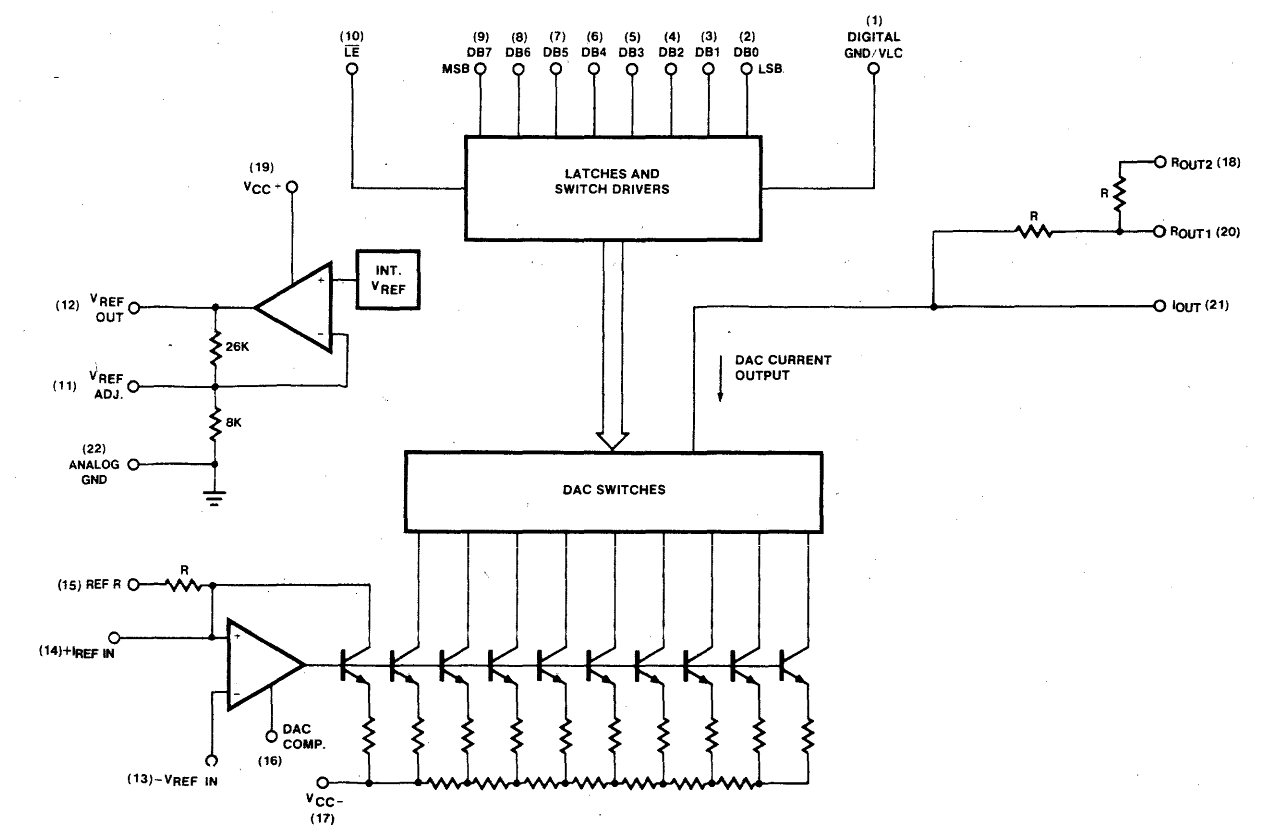
TOP VIEW

ORDER NUMBERS

NE5119F SE5119F

NE5119N

BLOCK DIAGRAM



All R values equal 5kΩ and are thermally matched.

Figure 1

DESCRIPTION

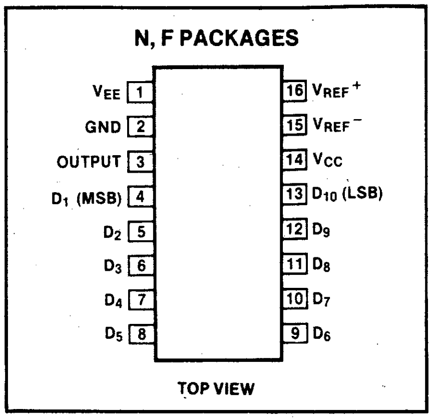
The NE5410/SE5410 are 10-Bit Multiplying Digital-to-Analog Converters pin-and-function compatible with the industry-standard MC3410, but with improved performance. These are capable of high-speed performance, and are used as general-purpose building blocks in cost-effective D/A systems.

The NE/SE5410 provides complete 10-bit accuracy and differential nonlinearity over temperature, and a wide compliance voltage range. Segmented current sources, in conjunction with an R/2R DAC provides the binary weighted currents. The output buffer amplifier and voltage reference have been omitted to allow greater speed, lower cost, and maximum user flexibility.

FEATURES

- **Pin-and-function compatible with MC3410**
- **10-bit resolution and accuracy (±0.05%)**
- **Guaranteed differential non-linearity over temperature**
- **Wide compliance voltage range— −2.5 to +2.5V**
- **Fast settling time—250ns typical**
- **Digital inputs are TTL and CMOS compatible**
- **High-speed multiplying input slew rate —20mA/μs**
- **Reference amplifier internally compensated**
- **Standard supply voltages +5V and −15V**

PIN CONFIGURATION



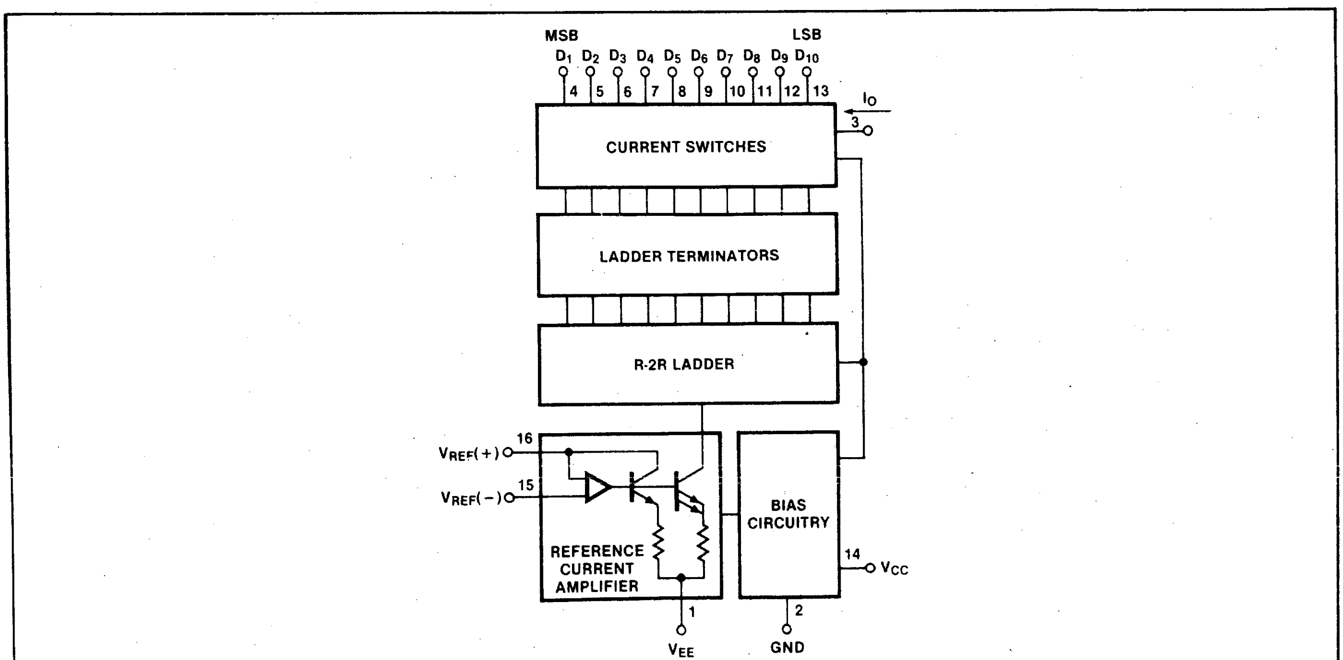
APPLICATIONS

- **Successive approximation A/D converters**
- **High-speed, automatic test equipment**
- **High-speed modems**
- **Waveform generators**
- **CRT displays**
- **Strip CHART and X-Y plotters**
- **Programmable power supplies**
- **Programmable gain and attenuation**

ABSOLUTE MAXIMUM RATINGS $T_A = +25°C$ unless otherwise noted

SYMBOL AND PARAMETER		RATING	UNIT
V_{CC}	Power Supply	+7.0	Vdc
V_{EE}		−18	Vdc
V_I	Digital Input Voltage	+15	Vdc
V_O	Applied Output Voltage	+4, −5.0	Vdc
$I_{REF(16)}$	Reference Current	2.5	mA
V_{REF}	Reference Amplifier Inputs	V_{CC}, V_{EE}	Vdc
$V_{REF(D)}$	Reference Amplifier Differential Inputs	0.7	Vdc
T_A	Operating Temperature Range		
	SE5410	−55 to +125	°C
	NE5410	0 to +70	°C
T_J	Junction Temperature		
	Ceramic Package	+175	°C
	Plastic Package	+150	°C

BLOCK DIAGRAM



SPATIAL, STEREO AND PSEUDO-STEREO SOUND CIRCUIT — TDA3810

Preliminary

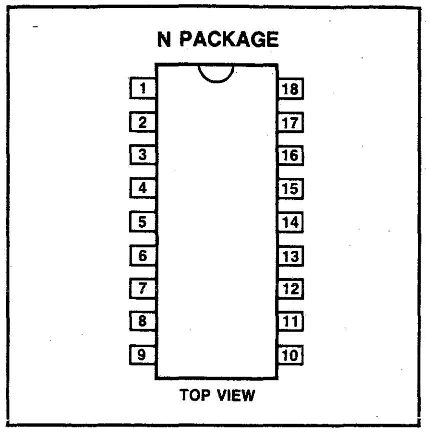
DESCRIPTION

The TDA3810 is an integrated circuit which can provide three switched functions for radio and television equipment: spatial sound from a stereo source; stereo sound from a stereo source; pseudo-stereo sound from a mono source.

FEATURES

- **Three switched functions:**
  - **spatial**
  - **stereo**
  - **pseudo-stereo**
- **Muting circuit prevents LED flickering**
- **LED driving outputs (pins 7 and 8)**
- **TTL compatible inputs for selecting operating mode**

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

SYMBOL AND PARAMETER		RATING	UNIT
V_{CC}	Supply voltage (pin 18)	17	V
I_{CC}	Supply current (pin 18)	12	mA
T_{STG}	Storage temperature range	−25 to +150	°C
T_A	Operating ambient temperature range	0 to +70	°C
Thermal Resistance			
$R_{th\ cr\text{-}a}$	From crystal to ambient	80	K/W

TRUTH TABLE

MODE	CONTROL INPUT STATE		LED SPATIAL	LED PSEUDO
	PIN 11	PIN 12	PIN 7	PIN 8
Mono pseudo-stereo	HIGH	LOW	Off	On
Spatial stereo	HIGH	HIGH	On	Off
Stereo	LOW	X	Off	Off

LOW = 0 to 0.8V (the less positive voltage)
HIGH = 2V to V_{CC} (the more positive voltage)
X = state is don't care

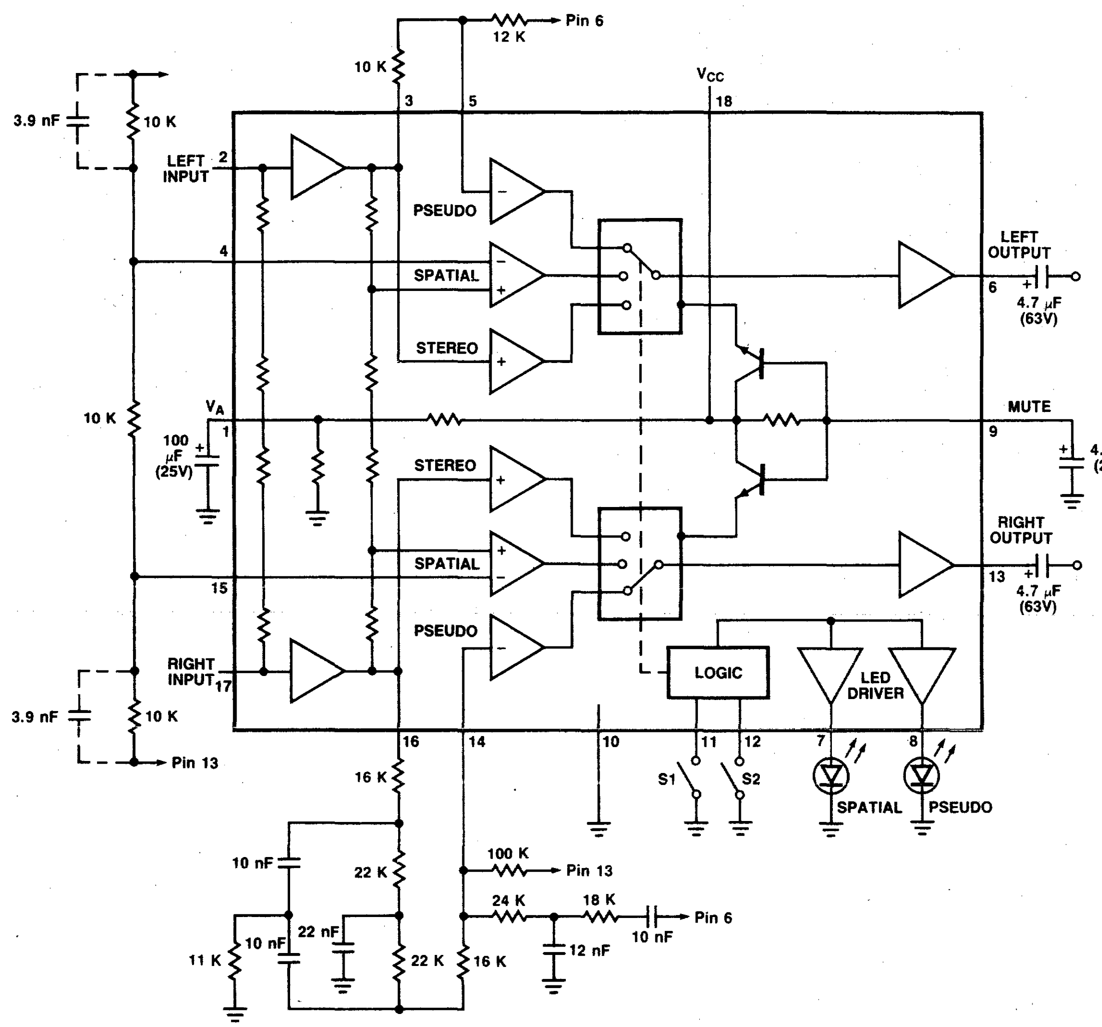
FUNCTIONAL PIN DESCRIPTION

PIN NO.	NAME AND FUNCTION
1	V_{REF}
2	Left channel input
3	Left channel stereo feedback
4	Left channel spatial feedback
5	Left channel pseudo feedback
6	Left channel output
7	Spatial indicator driver
8	Pseudo indicator driver
9	Mute
10	Ground
11	S1
12	S2
13	Right channel output
14	Right channel pseudo feedback
15	Right channel spatial feedback
16	Right channel stereo feedback
17	Right channel input
18	V_{DD}

SPATIAL, STEREO AND PSEUDO-STEREO SOUND CIRCUIT TDA3810

Preliminary

BLOCK DIAGRAM



SPATIAL, STEREO AND PSEUDO-STEREO SOUND CIRCUIT TDA3810

Preliminary

DC ELECTRICAL CHARACTERISTICS V_{CC} = 12V; T_A = 25°C; Test circuit Figure 1 stereo mode (pin 11 to ground) unless otherwise specified.

SYMBOL AND PARAMETER		TEST CONDITION	TDA3810			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage range	(Pin 18)	4.5		16.5	V
V_{CC}	Supply current			6	12	mA
V_S	Reference voltage		5.3	6	6.7	V
$V_{i(rms)}$	Input voltage	(Pin 2 or 17) THD = 0.2%	2			V
R_i	Input resistance	(Pin 2 or 17)	50	75		kΩ
G_v	Voltage gain V_o/V_i			0		dB
α	Channel separation (R/L)		60	70		dB
THD	Total harmonic distortion	f = 40 to 16000 Hz; $V_{o(rms)}$ = 1V		0.1		%
RR	Power supply ripple rejection			50		dB
$V_{n(rms)}$	Noise output voltage	(Unweighted) left and right output)		10		μV
Spatial mode (Pins 11 and 12 HIGH)						
α	Antiphase crosstalk			50		%
G_v	Voltage gain		1.4	2.4	3.4	dB

PSEUDO-STEREO MODE The quality and strength of the pseudo-stereo effect is determined by external filter components.

SYMBOL AND PARAMETER		TEST CONDITION	TDA3810			UNIT
			Min	Typ	Max	
Control inputs		(Pins 11 and 12)				
R_i	Input resistance		70	120		kΩ
$-I_i$	Switching current			35	100	μA
LED drivers (Pins 7 and 8)						
I_o	Output current for LED		10	12	15	mA
V_F	Forward voltage				6	V

DESCRIPTION

The NE570/571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expandor. Each channel has a full wave rectifier to detect the average value of the signal; a linerarized, temperature compensated variable gain cell; and an operational amplifier.

The NE570/571 is well suited for use in telephone subscriber and trunk carrier systems, communications systems and hi-fi audio systems.

FEATURES

- **Complete compressor and expandor in 1 IC**
- **Temperature compensated**
- **Greater than 110dB dynamic range**
- **Operates down to 6Vdc**
- **System levels adjustable with external components**
- **Distortion may be trimmed out**

CIRCUIT DESCRIPTION

The NE570/571 compandor building blocks, as shown in the block diagram, are a full wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at V_{REF}. The rectified current is averaged on an external filter capacitor tied to the C_{RECT} terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively coupled voltage inputs as shown in the following equation. Note that for capacitively coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than .1μA.

$$G \propto \frac{|V_{IN} - V_{REF}|\ \text{avg.}}{R_1}$$

or

$$G \propto \frac{|V_{IN}|\ \text{avg.}}{R_1}$$

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expandor or compressor application, this would lead to third harmonic distortion, so there is a tradeoff to be made between fast attack and decay times, and distortion. For step changes in amplitude, the change in gain with time is shown by this equation.

$$G(t) = (G_{initial} - G_{final})\ e^{-t/\tau} + G_{final};\ \tau = 10K \times C_{RECT}$$

The variable gain cell is a current in, current out device with the ratio I_{OUT}/I_{IN} controlled by the rectifier. I_{IN} is the current which flows from the ΔG input to an internal summing node biased at V_{REF}. The following equation applies for capacitively coupled inputs. The output current, I_{OUT}, is fed to the summing node of the op amp.

$$I_{IN} = \frac{V_{IN} - V_{REF}}{R_2} = \frac{V_{IN}}{R_2}$$

A compensation scheme built into the ΔG cell compensates for temperature, and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset voltages. The THD trim terminal provides a means for nulling the internal offsets for low distortion operation.

The operational amplifier (which is internally compensated) has the non-inverting input tied to V_{REF}, and the inverting input connected to the ΔG cell output as well as brought out externally. A resistor, R_3, is brought out from the summing node and allows compressor or expandor gain to be determined only by internal components.

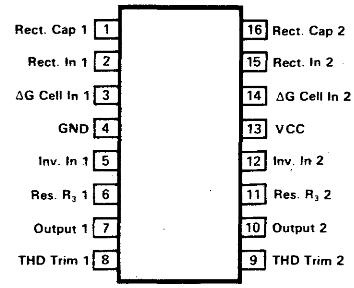
Note:
1. Supplied only in large SO (Small Outline) package.

APPLICATIONS

- **Telephone trunk compandor—570**
- **Telephone subscriber compandor—571**
- **High level limiter**
- **Low level expandor—noise gate**
- **Dynamic noise reduction systems**
- **Voltage controlled amplifier**
- **Dynamic filters**

PIN CONFIGURATION

D[1], F, N PACKAGE



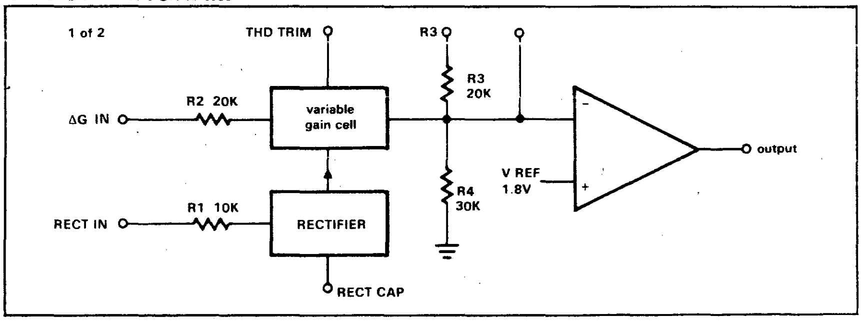
Order Part No.

NE570D[1]	NE570 F,N
NE571D[1]	NE571 F,N
SA571D[1]	SA571 F,N

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
	Positive supply		Vdc
	570	24	
	571	18	
T_A	Operating temperature range		
	NE	0 to 70	°C
	SA	-40 to +85	°C
P_D	Power dissipation	400	mW

BLOCK DIAGRAM



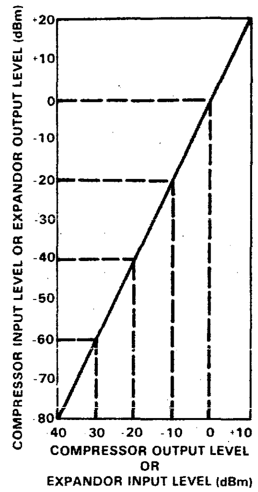
The output stage is capable of ±20mA output current. This allows a +13dBm (3.5V rms) output into a 300Ω load which, with a series resistor and proper transformer, can result in +13dBm with a 600Ω output impedance.

A band gap reference provides the reference voltage for all summing nodes, a regulated supply voltage for the rectifier and ΔG cell, and a bias current for the ΔG cell. The low tempco of this type of reference provides very stable biasing over a wide temperature range.

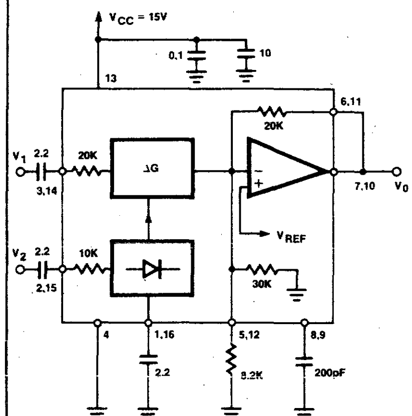
The typical performance characteristics illustration shows the basic input-output transfer curve for basic compressor or expandor circuits.

TYPICAL PERFORMANCE CHARACTERISTICS

BASIC INPUT-OUTPUT TRANSFER CURVE



TYPICAL TEST CIRCUIT



DC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 15V

PARAMETER	TEST CONDITIONS	NE570 Min	NE570 Typ	NE570 Max	NE/SA571[6] Min	NE/SA571[6] Typ	NE/SA571[6] Max	UNIT
V_{CC} Supply voltage		6		24	6		18	V
I_{CC} Supply current	No signal		3.2	4.0		3.2	4.8	mA
Output current capability		±20			±20			mA
Output slew rate			±.5			±.5		V/us
Gain cell distortion[2]	Untrimmed		.3	1.0		.5	2.0	%
	Trimmed		.05			.1		
Resistor tolerance			±5	±15		±5	±15	%
Internal reference voltage		1.7	1.8	1.9	1.65	1.8	1.95	V
Output dc shift[3]	Untrimmed		±20	±50		±30	±100	mV
Expandor output noise	No signal, 15Hz-20kHz[1]		20	45		20	60	μV
			-15					dBRNC
Unity gain level		-1	0	+1	-1.5	0	+1.5	dBm
Gain change[2,4]	-40°C < T < 70°C		±.1			±.1		dB
	0°C < T < 70°C		±.1	±.2		±.1	±.4	
Reference drift[4]	-40°C < T < 70°C		+2, -25	-10, -40		+2, -25	+20, -50	mV
	0°C < T < 70°C		±5	±10		±5	±20	
Resistor drift[4]	-40°C < T < 70°C		+8,-0					%
	0°C < T < 70°C		+1,-0					
Tracking error [5], input V_1 = OdBm	Rectifier input, V_2 =							dB
	+6dBm		±.2					
	-10dBm		+.2	-.2,+.4		+.2	-.2,+.5	
	-20dBm		+.2	-.3,+.6		+.2	-.4,+.7	
	-30dBm		+.2	-.5,+1		+.2	-1,+1.5	
	-40dBm		+.2,-.4			+.2,-.4		
Channel Separation		60				60		dB

NOTES
1. Input to V_1 and V_2 grounded.
2. Measured at OdBm,1kHz
3. Expandor ac input change from no signal to OdBm
4. Relative to value at T_A = 25°C
5. Relative to OdBm
6. Electrical characteristics for the SA571 only are specified over -40 to +85°C temperature range.

LINEAR

Signetics

PROGRAMMABLE ANALOG COMPANDOR

NE572

DESCRIPTION

The NE572 is a dual channel, high performance gain control circuit in which either channel may be used for dynamic range compression or expansion. Each channel has a full wave rectifier to detect the average value of input signal; a linearized, temperature compensated variable gain cell (ΔG) and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous compandors.

The NE572 is intended for noise reduction in high performance audio systems. It can also be used in a wide range of communication systems and video recording applications.

FEATURES

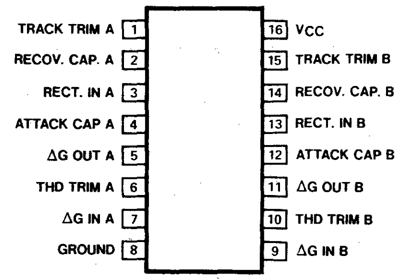
- **Independent control of attack and recovery time.**
- **Improved low frequency gain control ripple**
- **Complementary gain compression and expansion with external Op Amp**
- **Wide dynamic range—greater than 110dB**
- **Temperature compensated gain control**
- **Low distortion gain cell**
- **Low noise—6μV typical**
- **Wide supply voltage range—6V-22V**
- **System level adjustable with external components.**

APPLICATIONS

- **Dynamic noise reduction system**
- **Voltage control amplifier**
- **Stereo expandor**
- **Automatic level control**
- **High level limiter**
- **Low level noise gate**
- **State variable filter**

PIN CONFIGURATION

D[1], N PACKAGE



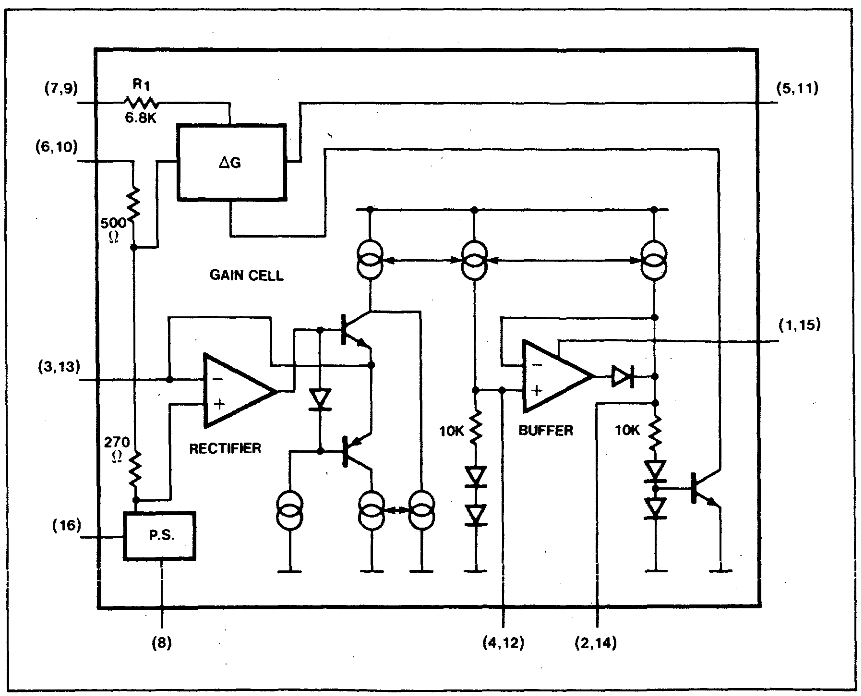
(Top view)

ORDER PART NO.
NE572N
NE572D

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	22	VDC
T_A	Operating temperature range	0 to 70	°C
P_D	Power dissipation	500	mW

BLOCK DIAGRAM



Note:
1. Supplied only in large SO (Small Outline) package.

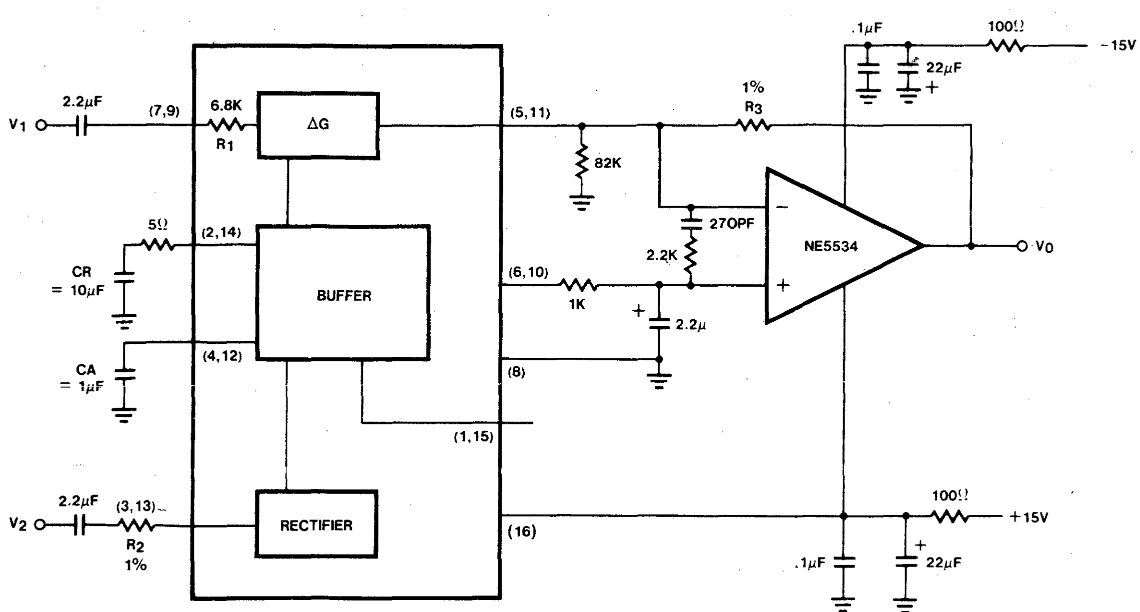
PROGRAMMABLE ANALOG COMPANDOR

NE572

ELECTRICAL CHARACTERISTICS Standard Test Conditions (unless otherwise noted) V_{CC} = 15V TA = 25°C Expandor mode (see test circuit) Input signals at unity gain level = 100mV RMS at 1KHz, $V_1 = V_2$, R_2 = 3.3K R_3 = 17.3K

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		6		22	V_{DC}
I_{CC}	Supply current	No Signal			6	mA
	Internal voltage reference		2.3	2.5	2.7	V_{DC}
THD THD THD	(untrimmed) (trimmed) (trimmed)	1kHz C_A = 1.0μF 1kHz C_R = 10μF 100Hz		.2 .05 .25	1.0	% % %
	No signal output noise	Input to V_1 and V_2 grounded (20-20kHz)		6	25	uV
	DC level shift (untrimmed)	Input change from no signal to 100mV RMS		±20	±50	MV
	Unity gain level		−1	0	+1	dB
	Large signal distortion	$V_1 = V_2$ = 400mV		0.7	3.0	%
	Tracking error measured relative to value at unity gain output	Rectifier input V_2 = +6dB −30dB		±.2 ±.5	 −1.5 +.8	dB
	Channel crosstalk	200mV RMS into channel A, measured output on channel B	60			dB
	Power supply rejection ratio	120Hz		70		dB

TEST CIRCUIT



HIGH SPEED DUAL DIFFERENTIAL COMPARATOR/SENSE AMP NE/SE521

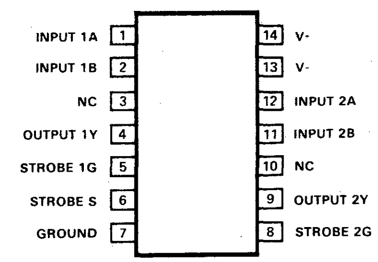
FEATURES

- 12ns maximum guaranteed propagation delay
- 20μA maximum input bias current
- TTL compatible strobes and outputs
- Large common mode input voltage range
- Operates from standard supply voltages
- Military qualifications pending

APPLICATIONS

- MOS memory sense amp
- A-to-D conversion
- High speed line receiver

PIN CONFIGURATION

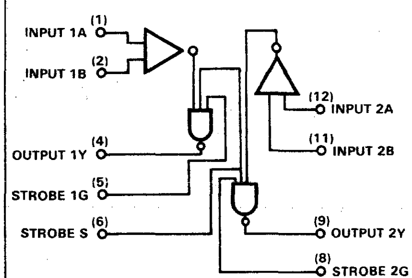


ORDER NUMBERS
NE521D,F,N SE521F

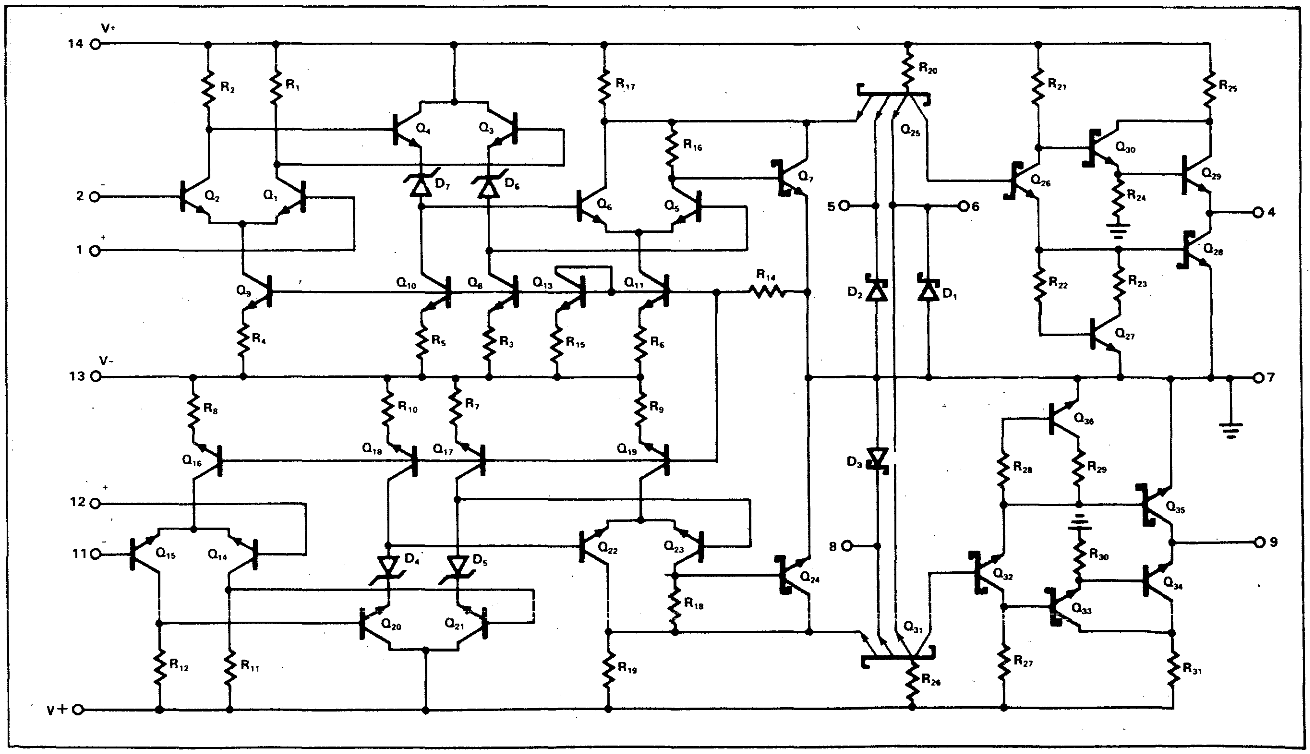
ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
	Supply voltage		V
V+	Positive	+7	
V-	Negative	-7	
V_{IDR}	Differential input voltage	±6	V
V_{IN}	Input voltage		V
	Common mode	±5	
	Strobe/gate	+5.25	
P_D	Power dissipation	600	mW
T_A	Operating temperature range		
	NE521	0 to 70	°C
	SE521	-55 to +125	
T_{stg}	Storage temperature range	-65 to +150	°C
	Lead temperature (solder, 60 sec)	+300	°C

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



VOLTAGE COMPARATOR

NE/SE527

DESCRIPTION

The SE/NE527 is a high speed analog voltage comparator which, in the first time mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed T2L gates with a precision linear amplifier on a single monolithic chip. The SE/NE527 is similar in design to the Signetics SE/NE529 voltage comparator except that it incorporates a "Emitter Follower" input stage for extremely low input currents. This opens the door to a whole new range of applications for analog voltage comparators.

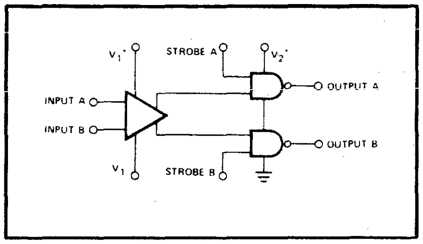
FEATURES

- **15ns propagation delay**
- **Complementary output gates**
- **TTL or ECL compatible outputs**
- **Wide common mode and differential voltage range**
- **Mil std 883A,B,C available**
- **Typical Gain of 5000**

APPLICATIONS

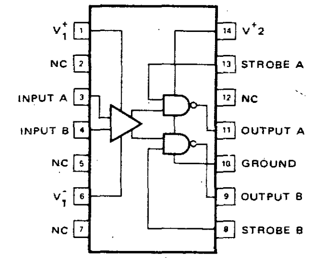
- **A/D conversion**
- **ECL to TTL interface**
- **TTL to ECL interface**
- **Memory sensing**
- **Optical data coupling**

BLOCK DIAGRAM



PIN CONFIGURATIONS

D,F,N PACKAGE

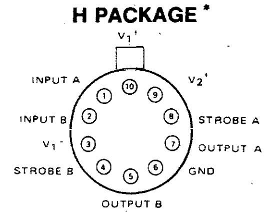


TOP VIEW

ORDER NUMBERS

NE527D,N,F SE527N,F

H PACKAGE *

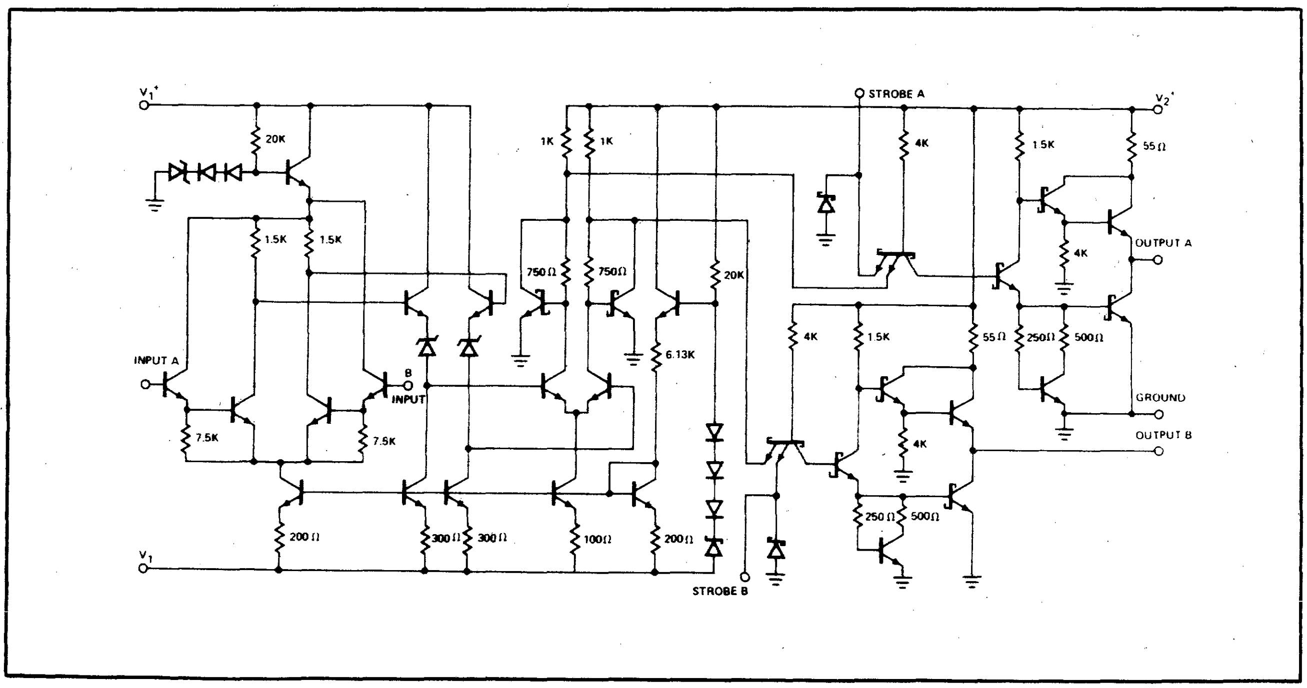


ORDER NUMBERS

NE/SE527H

*Metal cans (H) not recommended for new designs

EQUIVALENT SCHEMATIC



LINEAR

Signetics

VOLTAGE COMPARATOR

NE/SE529

DESCRIPTION

The SE/NE529 is a high speed analog voltage comparator which, for the first time mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed T²L gates with a precision linear amplifier on a single monolithic chip.

FEATURES

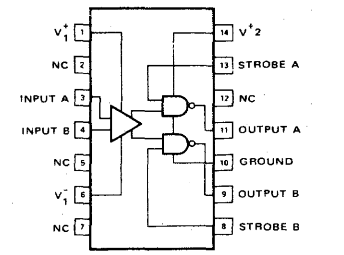
- **10ns propagation delay**
- **Complementary output gates**
- **TTL or ECL compatible outputs**
- **Wide common mode and differential voltage range**
- **Typical Gain 5000**

APPLICATIONS

- **A/D conversion**
- **ECL to TTL interface**
- **TTL to ECL interface**
- **Memory sensing**
- **Optical data coupling**
- **Mil std 883A,B,C available**

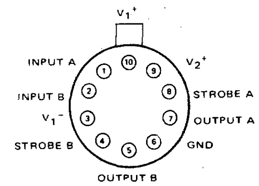
PIN CONFIGURATION

D,F,N PACKAGE



TOP VIEW
ORDER NUMBERS
NE/SE529F, NE529N,D

H PACKAGE*

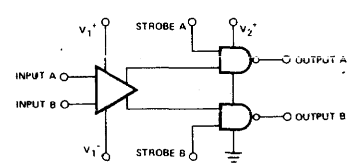


ORDER NUMBERS
NE/SE529H
*Metal cans (H) not recommended for new designs

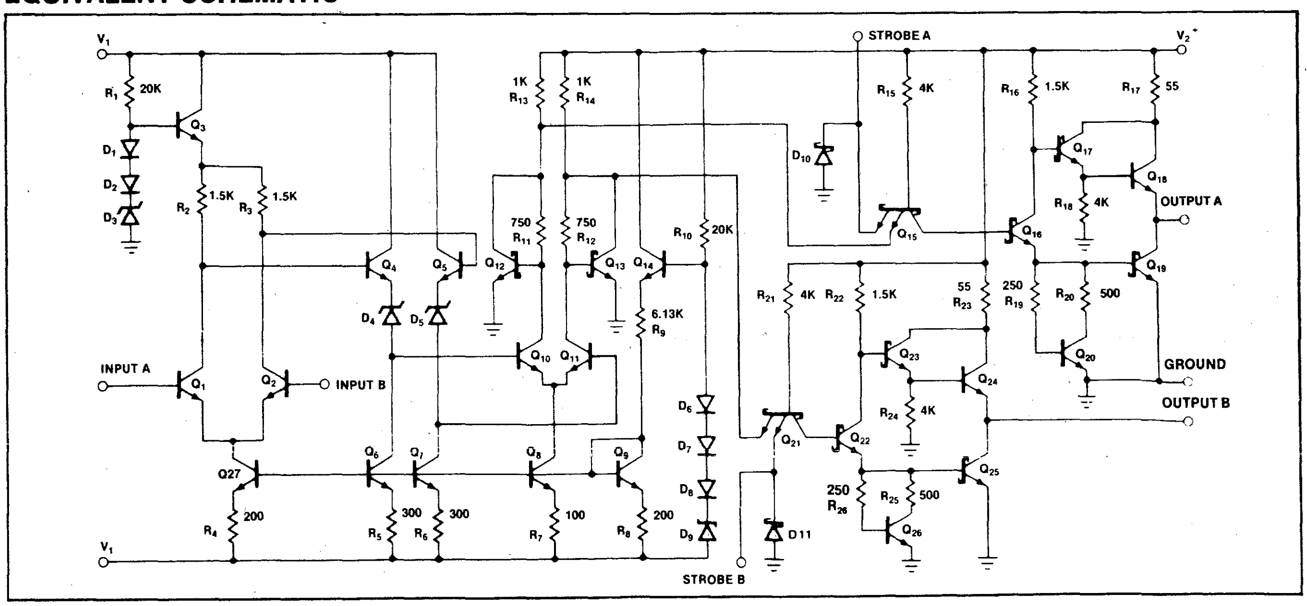
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage (V1+)	+15	V
Negative supply voltage (V1-)	-15	V
Gate supply voltage (V2+)	+7	V
Output voltage	+7	V
Differential input voltage	±5	V
Input common mode voltage	±6	V
Power dissipation	600	mW
Operating temperature range		
NE529	0 to +70	°C
SE529	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature		
(soldering, 60 sec)	+300	°C

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



VACUUM FLUORESCENT DISPLAY DRIVER

NE/SA594

DESCRIPTION

The NE/SA594 is a display driver interface for vacuum fluorescent displays. The device is comprised of 8 drivers and a bias network and is capable of driving the digits and/or segments of most vacuum fluorescent displays.

The inputs are designed to be compatible with TTL, DTL, NMOS, PMOS or CMOS output circuitry.

There is an active pull-down circuit on each output so that display ghosting is minimized and no external components are required for most fluorescent display applications.

FEATURES

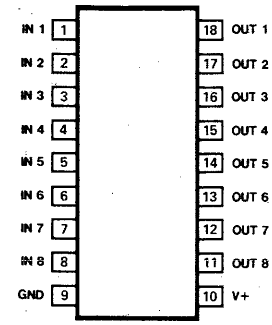
- **Digit and/or segment drivers**
- **Active output pull-down circuitry**
- **High output breakdown voltage**
- **Low supply voltage**
- **Input compatible with all logic outputs**

APPLICATIONS

- Digital clocks
- Dashboard displays
- Panel displays

PIN CONFIGURATION

N, F PACKAGE



TOP VIEW

ORDER NUMBERS
NE/SA594N NE/SA594F

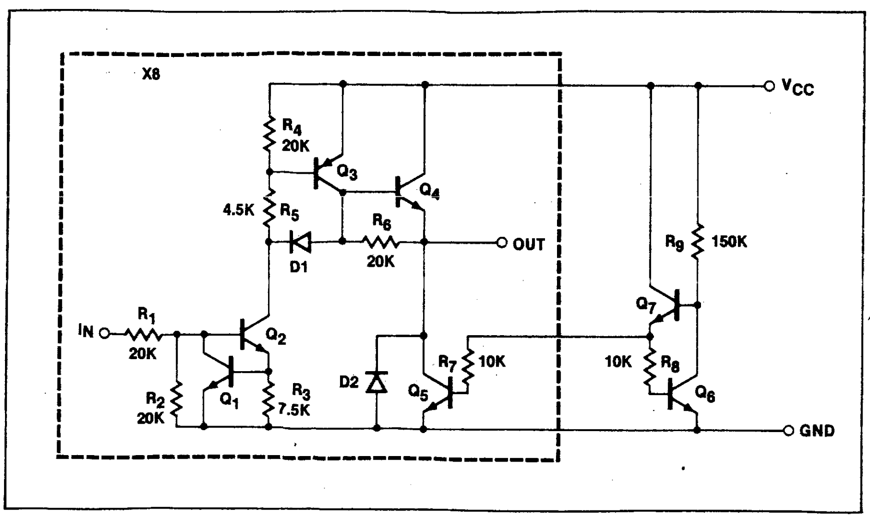
ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise noted)

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	45	V
V_{OUT}	Output voltage	V_{CC}	
V_{IN}	Input voltage	−0.3, +20	V
I_{OUT}	Output current		
	Each output	50	mA
	All outputs	200	mA
Pd	Power dissipation* (at 25°C)	800	mW
T_A	Operating temperature range		
	NE	0 to 70	°C
	SA	−40 to +85	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_J	Maximum junction temperature	− 165	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

NOTE

*Derate N (Plastic) Package above 38°C at 7.14 mW/°C.
Derate F (Ceramic) Package above 75°C at 10.8 mW/°C.

EQUIVALENT SCHEMATIC



ADDRESSABLE RELAY DRIVER

NE5090

DESCRIPTION

The NE/SE5090 addressable relay driver is a high current latched driver, similar in function to the 9934 address decoder. The device has 8 open collector Darlington power outputs, each capable of 150mA load current. The outputs are turned on or off by respectively loading a logic "1" or logic "0" into the device data input. The required output is defined by a 3 bit address. The device must be enabled by a $\overline{CE}$ input line which also serves the function of further address decoding. A common clear input, $\overline{CLR}$, turns all outputs off when a logic "0" is applied. The device is packaged in a 16 pin plastic or CERDIP package.

FEATURES

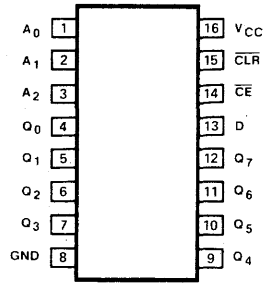
- **8 high current outputs**
- **Low-loading bus compatible inputs**
- **Power-on clear ensures safe operation**
- **Will operate in addressable or demultiplex mode**
- **Allows random (addressed) data entry**
- **Easily expandable**
- **Pin compatible with 9334**

APPLICATIONS

- **Relay driver**
- **Indicator lamp driver**
- **Triac trigger**
- **LED display digit driver**
- **Stepper motor driver**

PIN CONFIGURATION

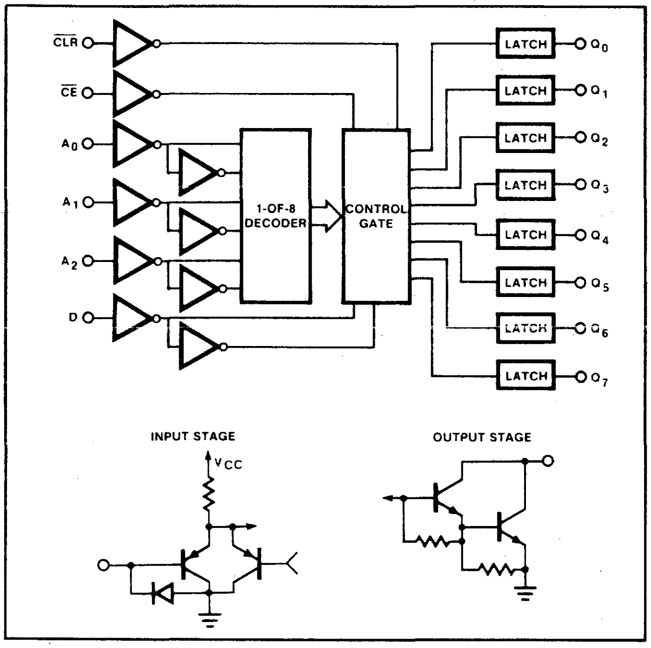
F, N PACKAGE



TOP VIEW

ORDER NUMBERS
NE5090N
NE5090F

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

$T_A = 25°C$ unless otherwise specified.

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7	V
V_{IN}	Input voltage	−0.5 to +15	V
V_{OUT}	Output voltage	0 to +30	V
I_{GND}	Ground current	500	mA
I_{OUT}	Output current Each output	200	mA
P_D	Power dissipation[1]	1	W
Ambient temperature range			°C
T_A	SE5090	−55 to +125	
T_A	NE5090	0 to +70	
T_J	Junction	150	
T_{STG}	Storage	−65 to +150	
T_{sold}	Lead soldering temperature (10 sec max)	300	°C

ADDRESSABLE PERIPHERAL DRIVERS

NE590/NE591

DESCRIPTION

The NE590/591 addressable peripheral drivers are high current latched drivers, similar in function to the 9334 address decoder. The device has 8 Darlington power outputs, each capable of 250mA load current. The outputs are turned on or off by respectively loading a logic high or logic low into the device data input. The required output is defined by a 3-bit address. The device must be enabled by a $\overline{CE}$ input line. A common clear input, $\overline{CLR}$, turns all outputs off when a logic low is applied.

The NE590 has 8 open collector Darlington outputs which sink current to ground. The device is packaged in a 16-pin molded or cerdip package.

The NE591 has 8 open emitter Darlington outputs which source current to an external load from a common collector line, V_S. This V_S line need not necessarily be the same as the 5 volt V_{CC} supply. The device is packaged in an 18-pin molded or cerdip package.

FEATURES

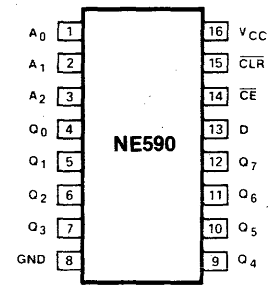
- **8 high current outputs**
- **Low-loading bus compatible inputs**
- **Power-on clear ensures safe operation**
- **NE590 will operate in addressable or demultiplex mode**
- **Allows random (addressed) data entry**
- **Easily expandable**
- **NE590 is pin compatible with 9334**

APPLICATIONS

- **Relay driver**
- **Indicator lamp driver**
- **Triac trigger**
- **LED display digit driver**
- **Stepper motor driver**

PIN CONFIGURATION

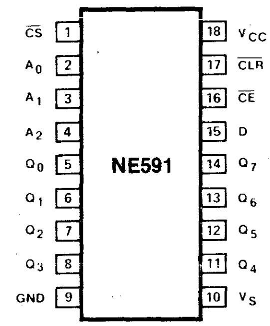
F,N PACKAGE



TOP VIEW

ORDER NUMBERS
NE590N,F

F,N PACKAGE



TOP VIEW

ORDER NUMBERS
NE591N,F

PIN DESIGNATION

590 PIN NO.	591 PIN NO.	SYMBOL	NAME & FUNCTION
1-3	2-4	A_0-A_2	A 3-bit binary address on these pins defines which of the 8 output latches is to receive the data.
4-7, 9-12	5-8, 11-14	Q_0-Q_7	The 8 device outputs. The NE590 has open collector Darlington outputs. The NE591 has open emitter follower outputs.
13	15	D	The data input. When the chip is enabled, this data bit is transferred to the defined output such that: "1" turns output switch "ON" "0" turns output switch "OFF" Thus in logic terms, the NE590 inverts data to the relevant output. The NE591 retains true data at the output.
14	16	$\overline{CE}$	The chip enable. When this input is low, the output latches will accept data. When $\overline{CE}$ goes high, all outputs will retain their existing state, regardless of address or data input conditions.
15	17	$\overline{CLR}$	The clear input. When $\overline{CLR}$ goes low all output switches are turned "OFF". On the NE590, a high data input will override the clear function on the addressed latch. On the NE591, $\overline{CLR}$ low will override any other condition.
—	1	$\overline{CS}$	The chip select input provides for an additional level of address decoding.
—	10	V_S	The V_S line provides the power to all 8 output devices. It is connected to the collectors of all 8 output transistors. This pin may be connected to the V_{CC} or another supply.

PROGRAMMABLE SEVEN CHANNEL RC ENCODER — NE5044

DESCRIPTION

The NE5044 is a programmable parallel input, serial output pulsewidth encoder. A multiplexed dual linear ramp technique is used to allow up to 7 inputs to be converted to a serial pulsewidth modulated signal with excellent linearity and minimal crosstalk. Fixed or variable frame rates can be used, externally controlled, for ease of demodulation. An onboard 5V regulator eliminates power supply sensitivities and provides up to 20mA current capability for driving external loads.

FEATURES

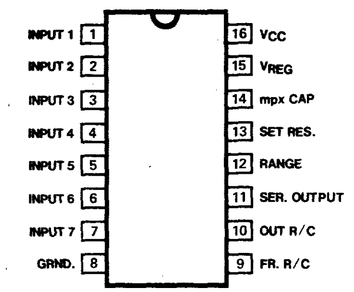
- **3 to 7 channels, externally selectable**
- **Constant current dual linear ramp for linearity better than .3%**
- **Internal voltage regulator for low drift**
- **Wide supply range 4.5 – 16V**
- **Fixed or variable frame rate set by external R-C**
- **External control for channel gain or range**
- **Versatile applications; exponential rates, mixing, dual rate, reversing etc.**
- **Compatible with all transmission mediums**

APPLICATIONS

- **Radio controlled aircraft, cars, boats, trains**
- **Industrial controllers**
- **Remote controlled entertainment systems**
- **Security systems**
- **Instrumentation recorders/controls**
- **Remote Analog/digital data transmission**
- **Automotive sensor systems**
- **Robotics**
- **Telemetry**

PIN CONFIGURATION

D,N PACKAGE



TOP VIEW

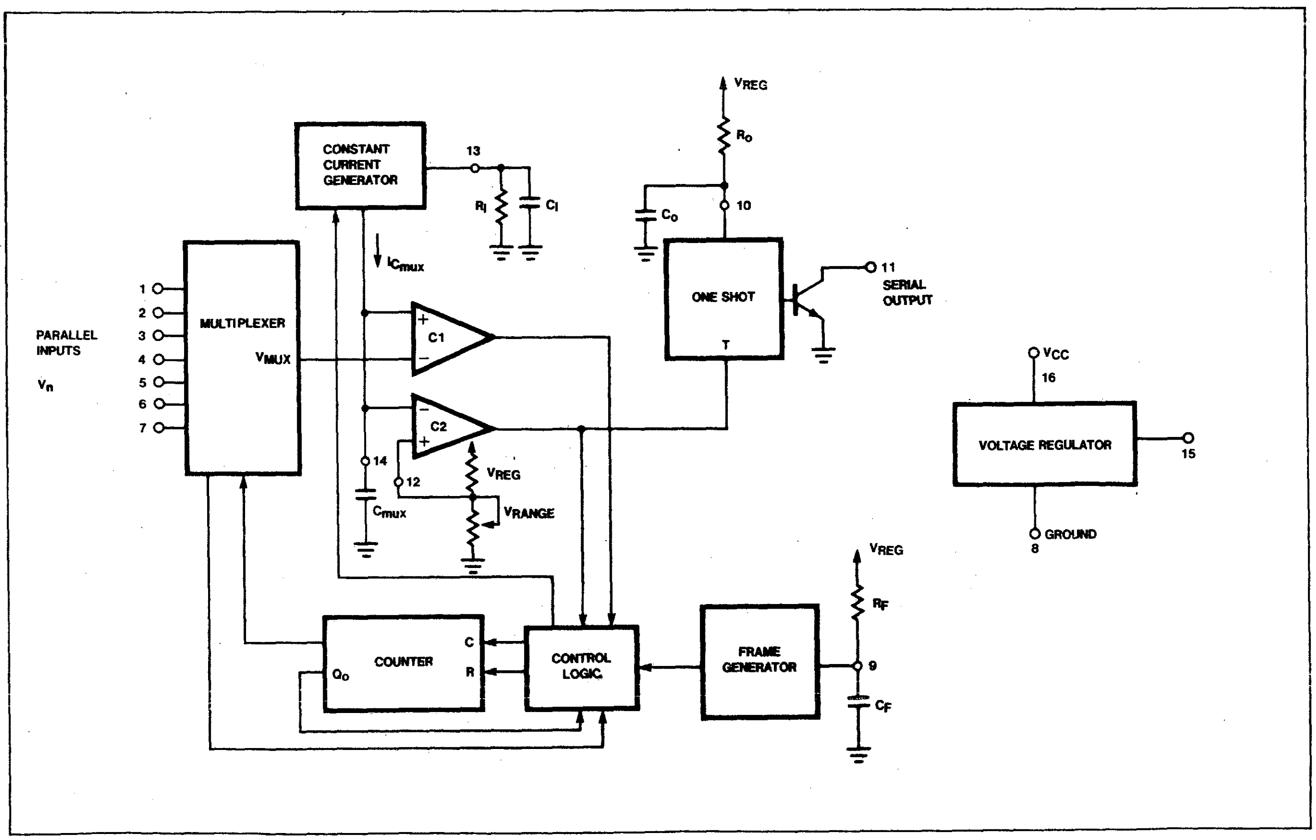
ORDER NUMBERS
NE5044D NE5044N

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
V_{CC}, Supply voltage	17	V
Regulator ouput current	−25	mA
Serial output peak current	30	mA
Constant current generator	−1	mA
Parallel inputs, range input	0-V_{REG}	V
One shot input, frame generator input	0-V_{REG}	V
Operating temperature	−20 to +75	°C
Storage temperature	−65 to +150	°C

NOTE
1. T_A = 25° unless otherwise stated.

BLOCK DIAGRAM



PROGRAMMABLE SEVEN CHANNEL RC ENCODER — NE5044

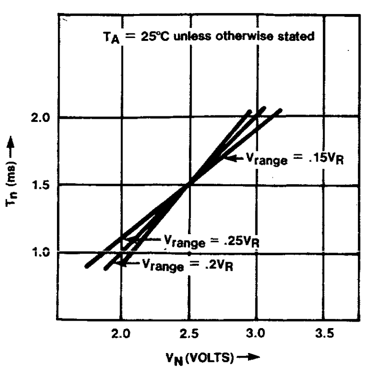
DC ELECTRICAL CHARACTERISTICS

Test conditions $T_A = 25°C$, $V_{CC} = 10V$ using Test Circuit A unless otherwise stated.

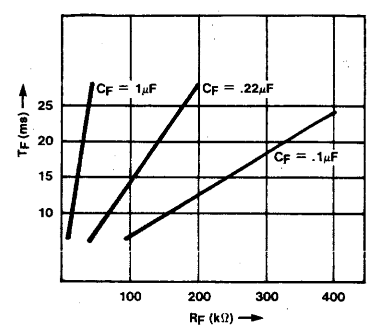
	PARAMETER	TEST CONDITIONS	NE 5044 Min	Typ	Max	UNIT
	POWER SUPPLY REQUIREMENTS (Note 1)					
	Power supply voltage range		4.5		16	V
	Power supply current	Excluding control pots and serial output currents		11	15	mA
	VOLTAGE REGULATOR					
V_{REG}	Output voltage		4.5	5.0	5.5	V
	Output current	$V_R \geq 4.5V$			−20	mA
	Line regulation	$7 \leq V_{CC} \leq 16$		.005	0.2	V/V
	MULTIPLEXER					
	Input current	$V_n = 2.5v$		±30	±200	nA
	Input voltage range	$V_n - V_{Range} \geq .75V$	1.5		5	V
	Crosstalk			±1	±5	μs
	OUTPUT PULSE					
T_n	Position	$R_I \bullet C_{mux} = 1.25ms$; $V_n = .5V_{REG}$; $V_{RANGE} = .2V_{REG}$	1350	1500	1650	μs
	Position linearity error			5		μs
	Position tempco	$0°C \leq T_A \leq 70°C$.		.15		μs/°C
	Position PSR	$6V \leq V_{CC} \leq 16V$		.5	1	μs/V
T_O	Width	$R_OC_O = 300\mu s$	240	285	330	μs
	Saturation voltage	$I_O = 25mA$		.6	1	V
I_{11}	Leakage current			.05	50	μA
	Range input voltage	$R_I = 50k\Omega$	.75			V
		$R_I = 25k\Omega$	1.00			V
	Frame time (Fixed)	$R_FC_F = 30ms$	17	20	23	ms
	Inhibit threshold				.4	V

NOTE
1. At supply voltages exceeding 12V, a current limiting resistor of 20 to 50Ω in series with V_{CC} is recommended.

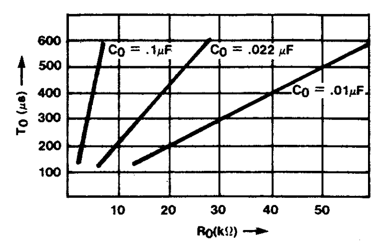
OUTPUT PULSE WIDTH (T_n) vs INPUT VOLTAGE (V_n)



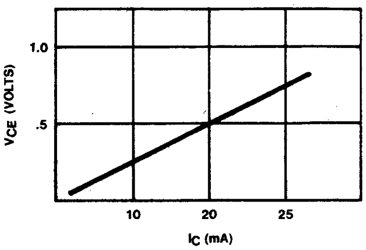
FRAME TIME (T_F) vs R_F



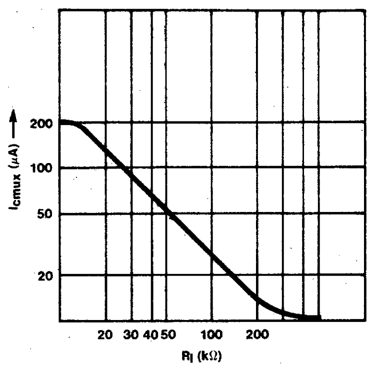
OUTPUT ONESHOT TIME (T_O) vs R_O



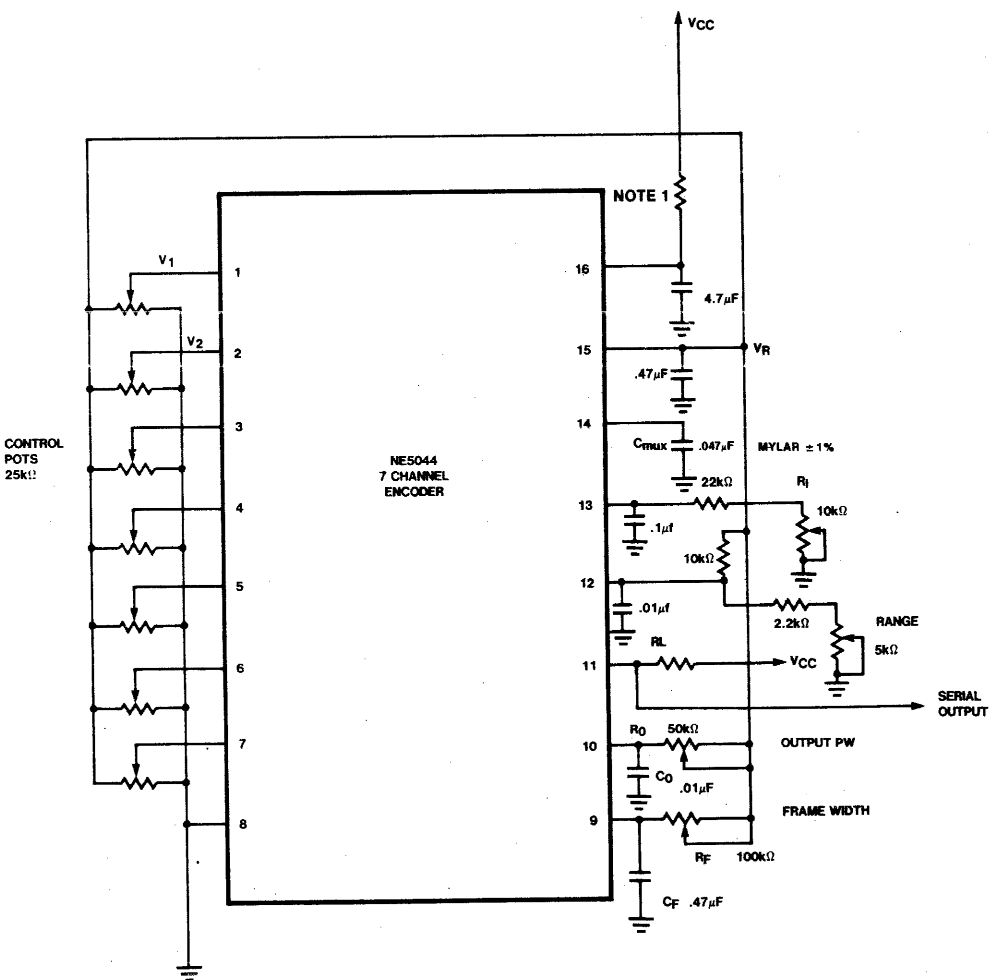
OUTPUT SATURATION VOLTAGE vs OUTPUT CURRENT



CONSTANT CURRENT vs R_I



TEST CIRCUIT



NOTE
1. At supply voltages exceeding 12V, a current limiting resistor of 20 to 50Ω in series with V_{CC} is recommended

SEVEN CHANNEL RC DECODER

NE5045

DESCRIPTION

The NE5045 is a serial input, parallel output, decoder intended for applications in pulse width or pulse position modulation systems. The serial input pulse, either positive or negative, is shaped and amplified before being fed to the counter/decoder. An integrating type sync. separator detects pulses greater than $T_W = R_S C_S$. The amplified input pulse triggers an internal one-shot (minimum pulse) which in turn clocks the counter-decoder, thereby enhancing system noise rejection. A missing pulse detector resets the decoder during the sync. pause. An internal voltage regulator supplies power for the radio receiver providing excellent isolation from the power supply as well as the decoder logic.

FEATURES

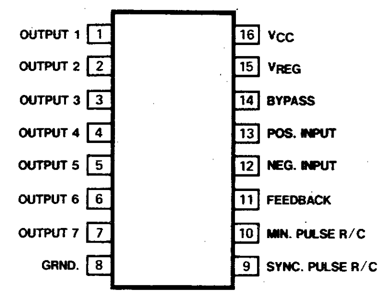
- **Decodes up to 7 channels**
- **High gain input amplifier**
- **Externally set sync. pause and minimum pulse**
- **Wide supply voltage range, 3.6V–8V.**
- **Positive or negative pulse inputs**
- **Noise and flutter rejection**
- **Outputs reset to zero without inputs**
- **Compatible with all transmission mediums**

APPLICATIONS

- **Radio controlled aircraft, cars, boats, trains**
- **Industrial controllers**
- **Remote controlled entertainment systems**
- **Security systems**
- **Instrumentation recorders/controls**
- **Remote Analog/digital data transmission**
- **Automotive sensor systems**
- **Robotics**
- **Telemetry**

PIN CONFIGURATION

D,N PACKAGE



TOP VIEW

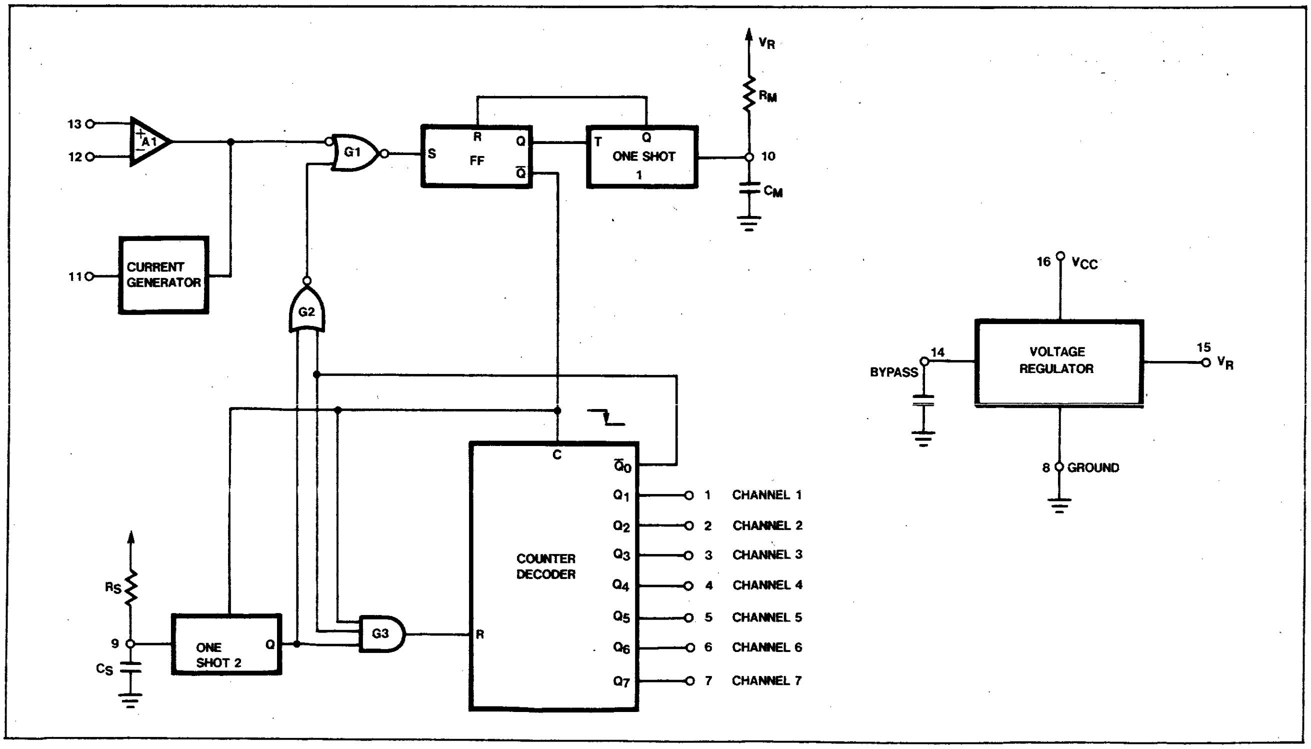
ORDER NUMBERS
NE5045N NE5045D

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
V_{CC}, Supply voltage	10	V
Regulator output current	−25	mA
Decoded output current	±5	mA
Pause input voltage	0 to V_R	V
Input amplifier voltage	0 to V_R	V
Operating temperature	−20 to +75	°C
Storage temperature	−65 to +150	°C

NOTE
1. T_A = 25°C unless otherwise stated

BLOCK DIAGRAM



SEVEN CHANNEL RC DECODER

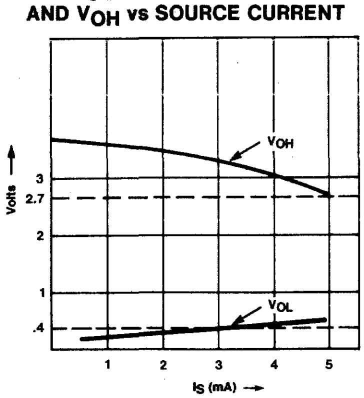
NE5045

DC ELECTRICAL CHARACTERISTICS

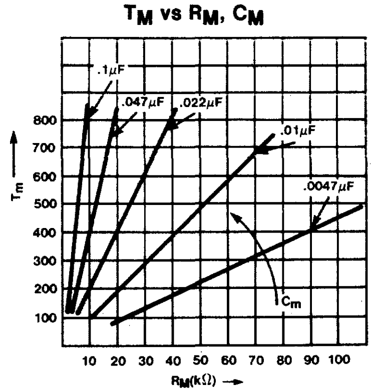
Standard conditions: (T_A = 25°C, V_{CC} = 5.0V unless otherwise stated), using Test Circuit #1

	PARAMETER	TEST CONDITIONS	NE5045 Min	NE5045 Typ	NE5045 Max	UNIT
	POWER SUPPLY REQUIREMENTS					
	Power supply voltage range	Test circuit #1	3.6		8.0	V
	Power supply current	Excluding input bias current		9.0	14.0	mA
	VOLTAGE REGULATOR					
	Output voltage		3.7	4.1	4.5	V
V_R	Output current	$V_R \geq 3.7V$			−15	mA
	Line regulation	V_{CC} = 6V to 8V		.01	.05	V/V
	Voltage drop	V_{CC} = 4V, I_R = −10mA			1.3	V
	INPUT AMPLIFIER					
	Input bias current			10	100	nA
	Input voltage range		2.0		4.0	V
	Open loop gain			60		dB
	Feedback current		100	200	400	μA
	Detection threshold	Test circuit #1, ΔV12 & 13		8	20	mV
T_S	Sync. pause time	$R_S C_S$ = 6.0ms	5.1	6.0	6.9	ms
T_M	Minimum pulse time	$R_m C_m$ = 500μs	405	475	545	μs
	OUTPUTS-ALL CHANNELS					
	V_{OL}	I_{SINK} = 1mA		.25	.5	V
	V_{OH}	I_{SOURCE} = 2mA	2.7			V

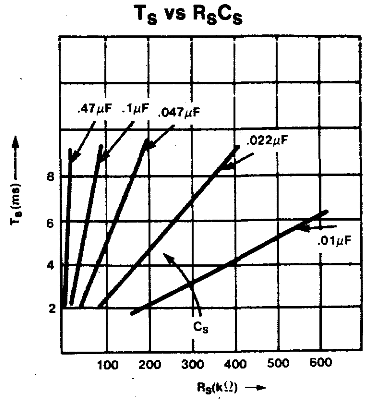
V_{OL} vs SINK CURRENT AND V_{OH} vs SOURCE CURRENT



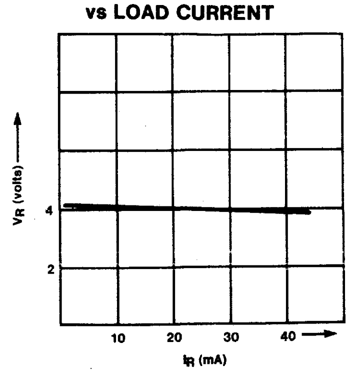
MINIMUM PULSE TIME, T_M vs R_M, C_M



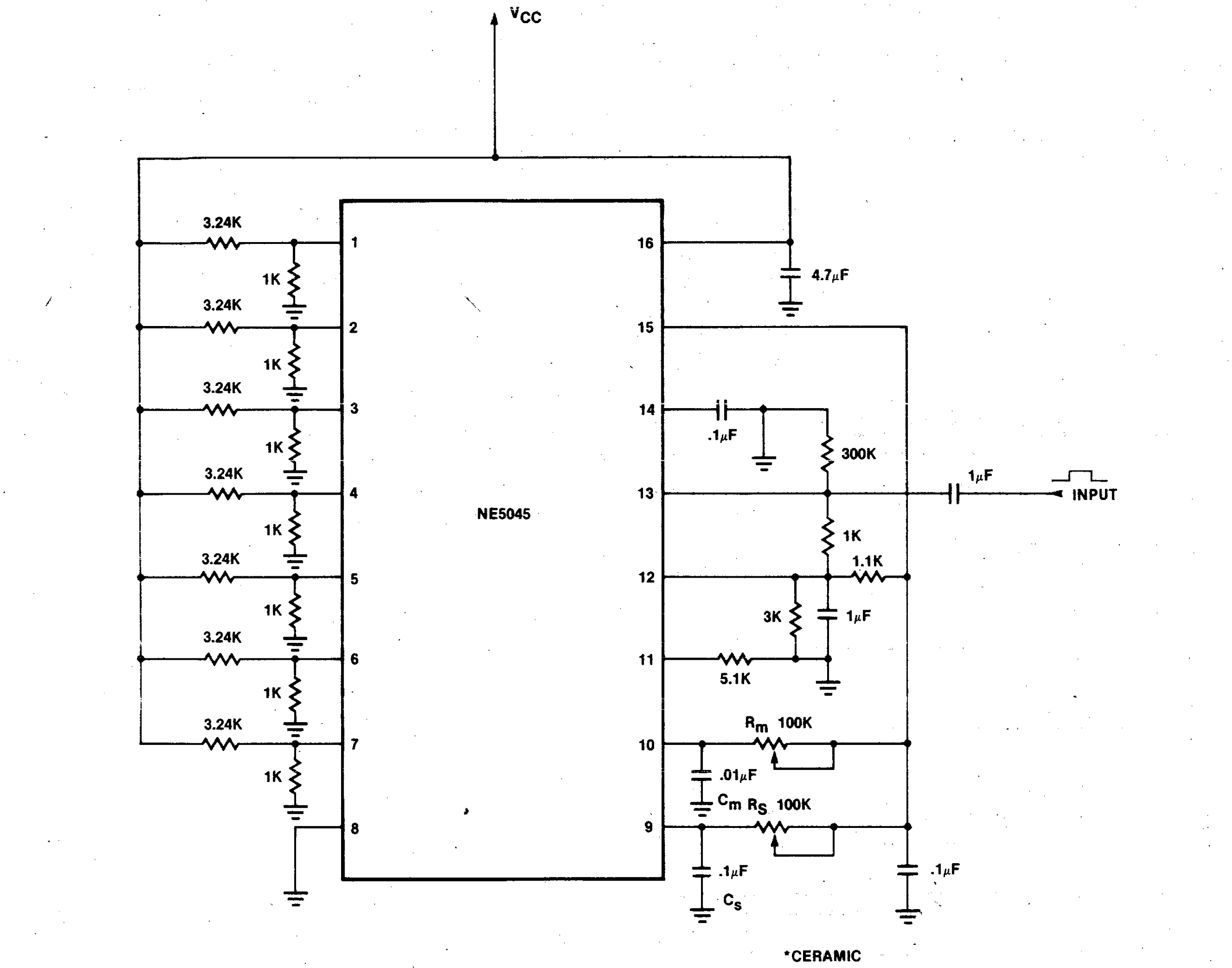
SYNC. PAUSETIME, T_S vs $R_S C_S$



REGULATOR VOLTAGE vs LOAD CURRENT



TEST CIRCUIT



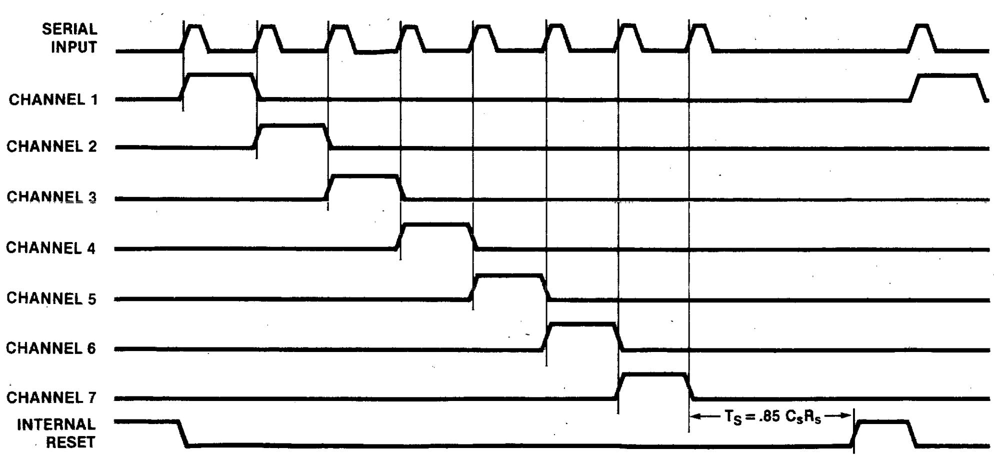


Figure 1. NE5045 Decoder Timing Diagram

SERVO AMPLIFIER

NE544

DESCRIPTION

The NE544 is a servo amplifier and pulse-width demodulator with internal motor drive transistors. It is designed for remote control applications in digital proportional systems but can be used in many other closed loop position control applications. It incorporates a linear one shot for improved positional accuracy and outputs for external pnp motor drive transistors.

FEATURES

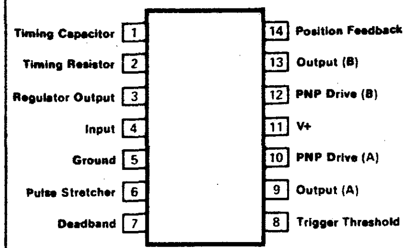
- **500mA load current capability**
- **Bidirectional bridge output with single power supply**
- **Low standby power drain**
- **Adjustable deadband and trigger thresholds**
- **High linearity, 0.5% maximum error**
- **Output drive for external PNP transistors (optional)**
- **Wide supply voltage range**

APPLICATIONS

- **Miniature position Servo**
- **Robotics**
- **Control devices**
- **Remote positioning**

PIN CONFIGURATIONS

N PACKAGE



TOP VIEW

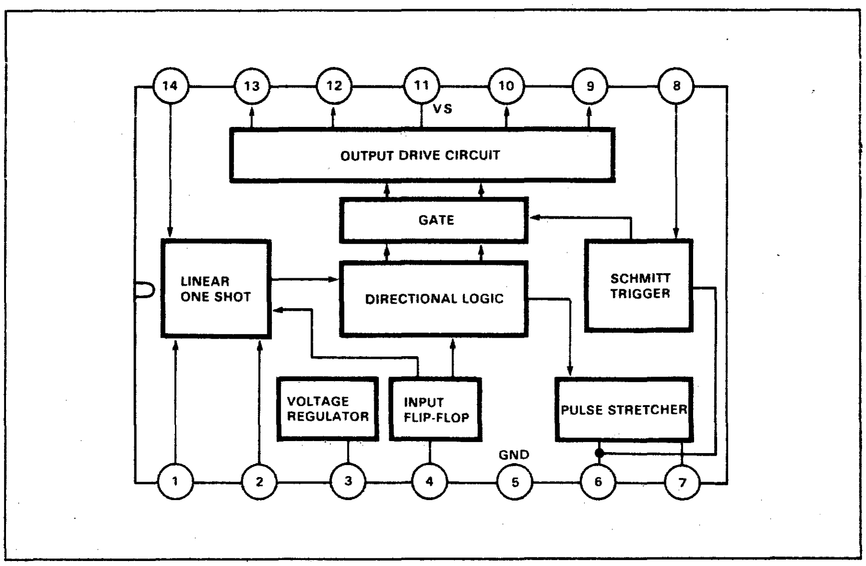
ORDER NUMBER
NE544N

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise specified.

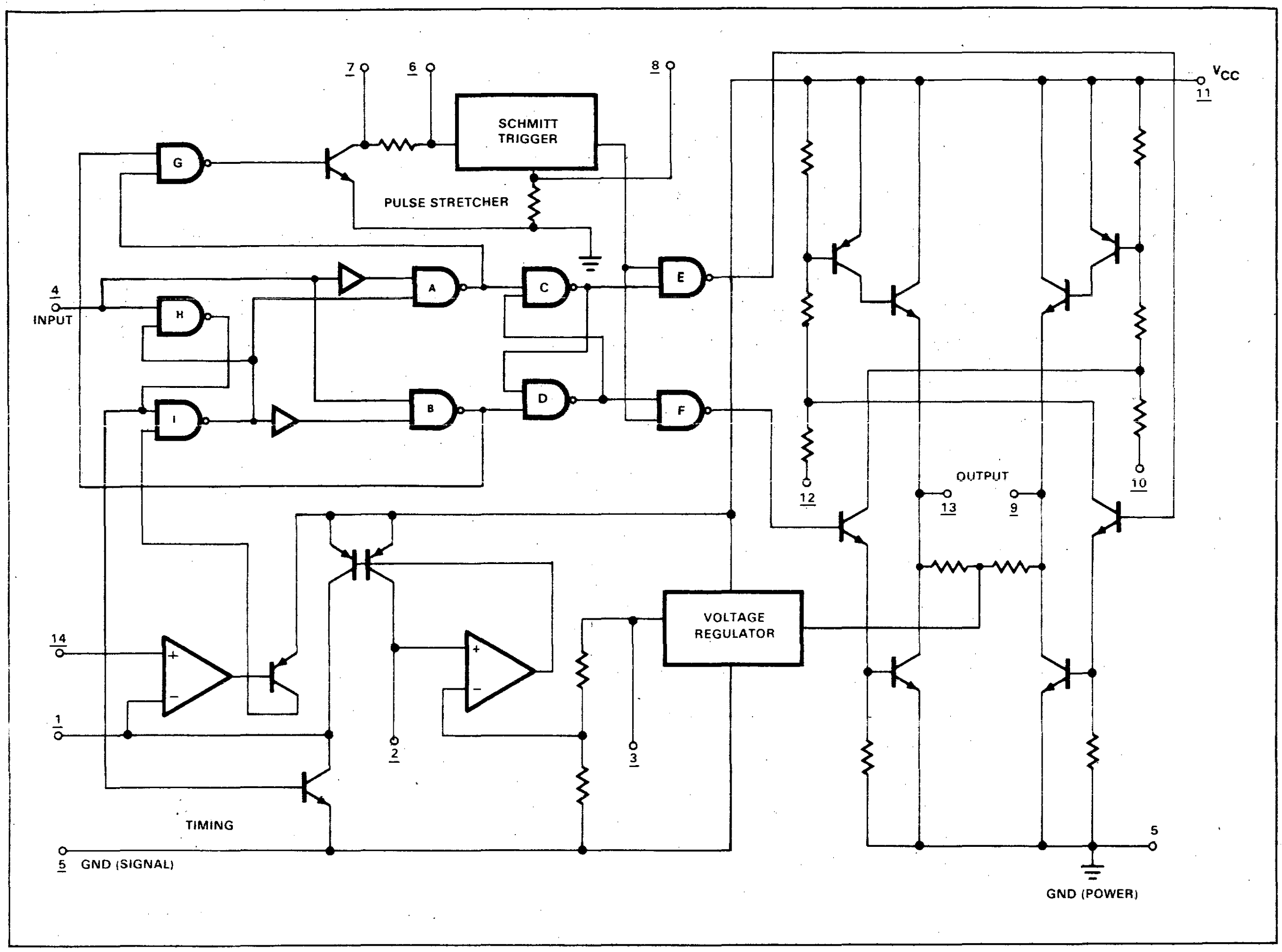
PARAMETER		RATING	UNIT
V+	Supply voltage	6.0	V
I_O	Output current	500	mA
T_A	Operating temperature	-20 to +75	°C
T_{stg}	Storage temperature	-65 to +150	°C

BLOCK DIAGRAM



SERVO AMPLIFIER NE544

EQUIVALENT CIRCUIT SCHEMATIC



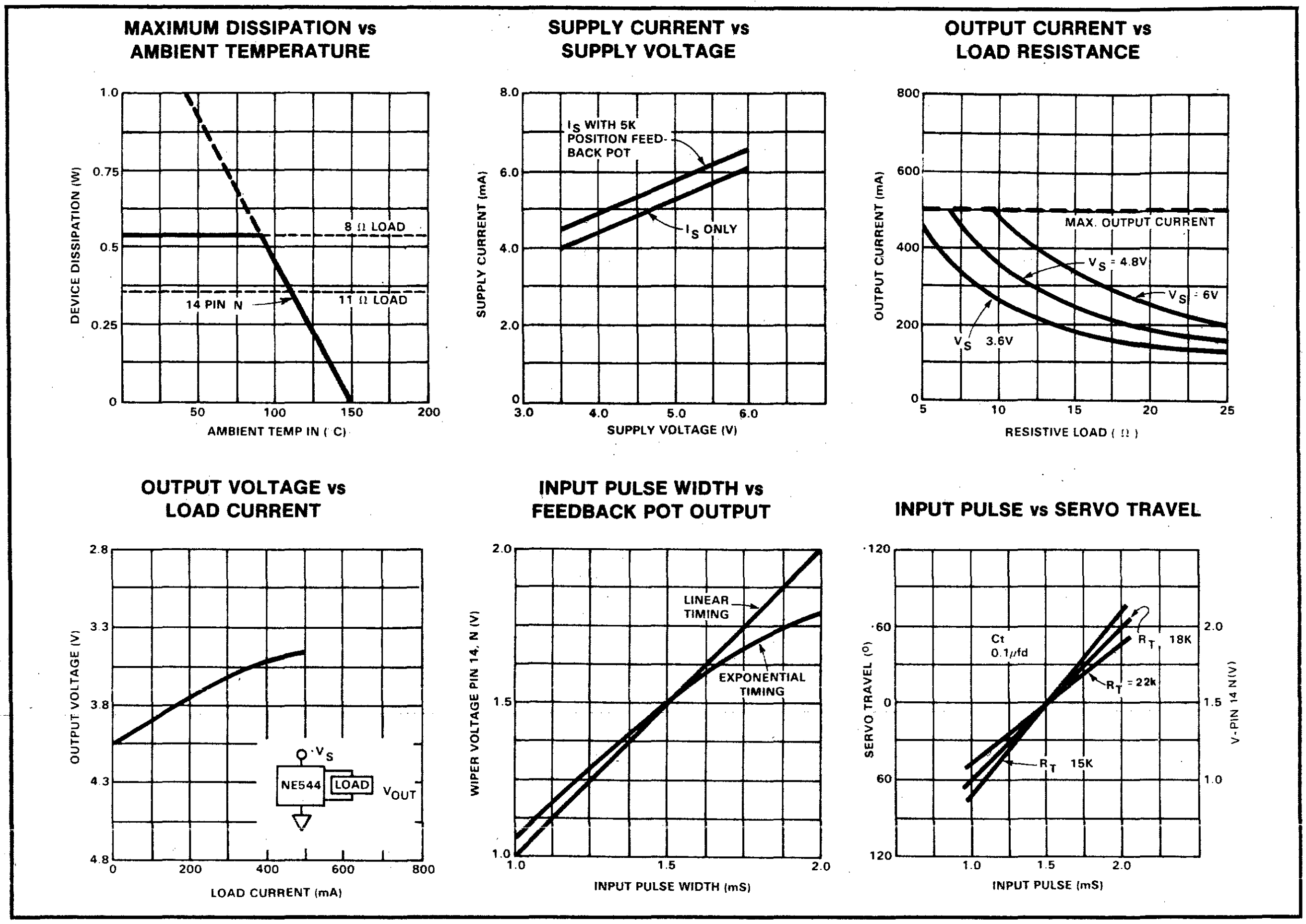
DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = 4.8V$ unless otherwise specified.

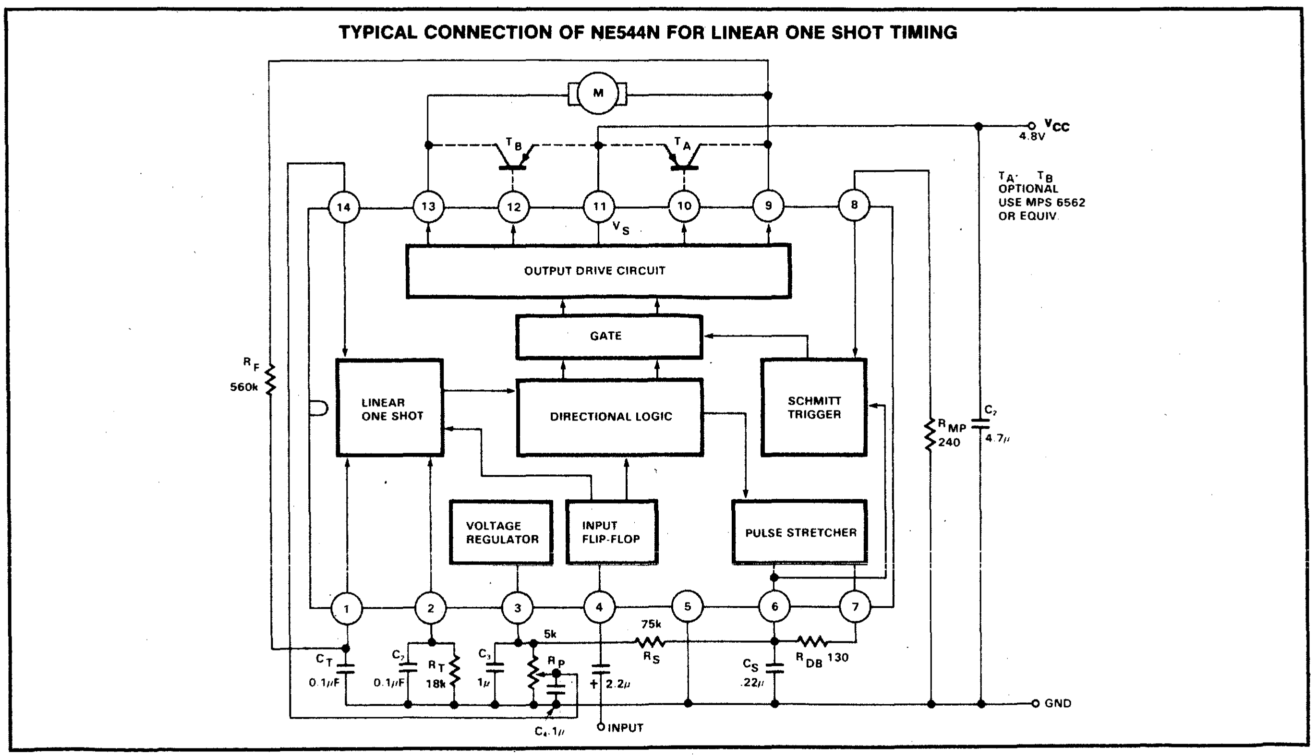
	PARAMETER		TEST CONDITIONS	LIMITS Min	Typ	Max	UNIT
V_{CC}	Supply voltage			3.2	4.8	6	V
I_{CC}	Supply current	Pin 11	Quiescent	4.2	5.5	10	mA
V_{TH}	Input threshold	Pin 4					V
	On				1.5		
	Off				1.4		
Z_{IN}	Input resistance	Pin 4			18		kΩ
	Output voltage						V
V_{OL}	Low		Pin 9 or 13, I_L = 400mA		0.3		
V_{OH}	High				3.9		
V_{REG}	Regulated voltage	Pin 3		2.1	2.5	2.9	V
ΔV_{REG}	Regulation	Pin 3	$3.9V \le V_{CC} \le 6V$		10		mV/V
	Minimum dead band	Pin 7	$R_{DB} = 0$		1		µs
	One shot temperature coefficient				.01		%/°C
	Standby output voltage		Pin 9 and 13		2.5		V
	PNP drive current		Pin 10 and 12		20		mA

SERVO AMPLIFIER

NE544

TYPICAL PERFORMANCE CHARACTERISTICS





LVDT SIGNAL CONDITIONER

NE5520

DESCRIPTION

The NE5520 is a signal conditioning circuit for use with Linear Variable Differential Transformers (LVDT). The chip includes a low distortion amplitude stable sine wave oscillator with programmable frequency to drive the primary of the LVDT; a synchronous demodulator to convert the LVDT output amplitude and phase to position information; and an output amp to provide gain and filtering.

FEATURES

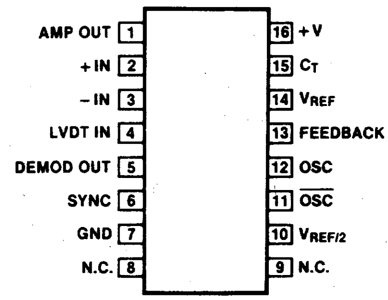
- Oscillator frequency: 1kHz to 20kHz
- Low distortion
- Capable of ratiometric operation
- Single supply operation 5V to 20V or dual supply ±2.5V to ±10V
- Low power consumption

APPLICATIONS

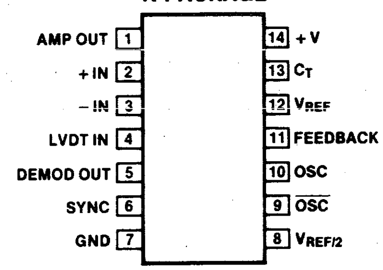
- LVDT signal conditioning
- RVDT signal conditioning

PIN CONFIGURATION

D[1], F PACKAGE



N PACKAGE

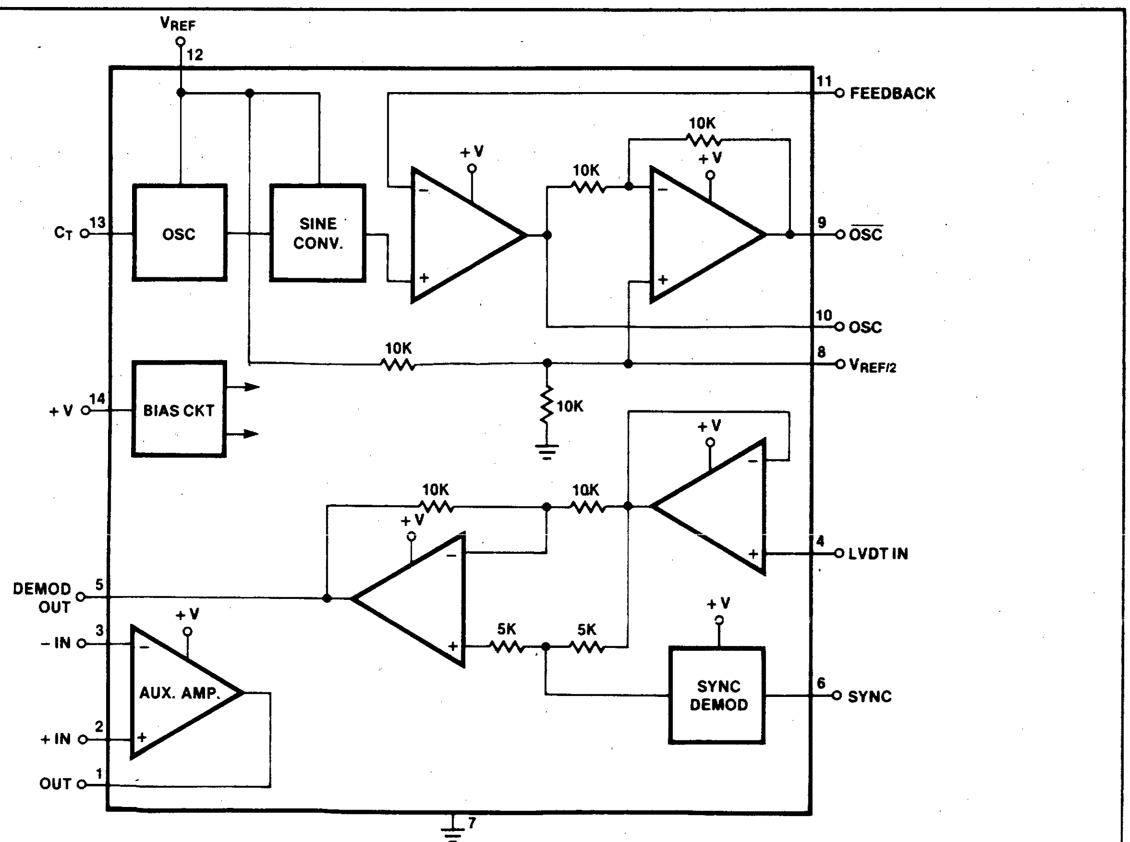


TOP VIEWS
ORDER NUMBERS
NE5520D[1]
NE5520F (16-Pin), NE5520N (14-Pin)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	+20	V
Split supply voltage	±10	V
Operating temperature range	0 to +70	°C
Storage temperature range	−65 to +165	°C
Power Dissipation (Note 1)	840	mW

BLOCK DIAGRAM



NOTES:
1. Supplied only in large SO (Small Outline) package. See package diagram.
2. Pin numbers are for N package.

OPERATIONAL TRANSCONDUCTANCE AMPLIFIERS LM13600/13600A

DESCRIPTION

The LM13600 series consists of two current controlled transconductance amplifiers each with differential inputs and a push pull output. The two amplifiers share common supplies but otherwise operate independently. Linearizing diodes are provided at the inputs to reduce distortion and allow higher input levels. The result is a 10 dB signal-to-noise improvement referenced to 0.5 percent THD. Controlled impedance buffers are provided which are specifically designed to complement the dynamic range of the amplifiers.

FEATURES

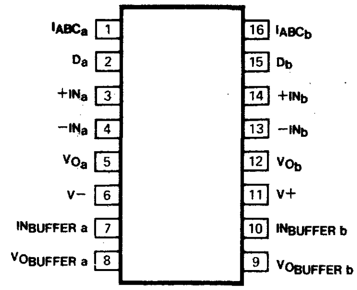
- **gm adjustable over 6 decades**
- **Excellent gm linearity**
- **Excellent matching between amplifiers**
- **Linearizing diodes**
- **Controlled impedance buffers**
- **High output signal to noise ratio**
- **Wide supply range ±2V to ±22V.**

APPLICATIONS

- **Current controlled amplifiers**
- **Current controlled impedances**
- **Current controlled filters**
- **Current controlled oscillators**
- **Multiplexers**
- **Timers**
- **Sample and hold circuits**

PIN DESCRIPTION

D,N PACKAGE



TOP VIEW

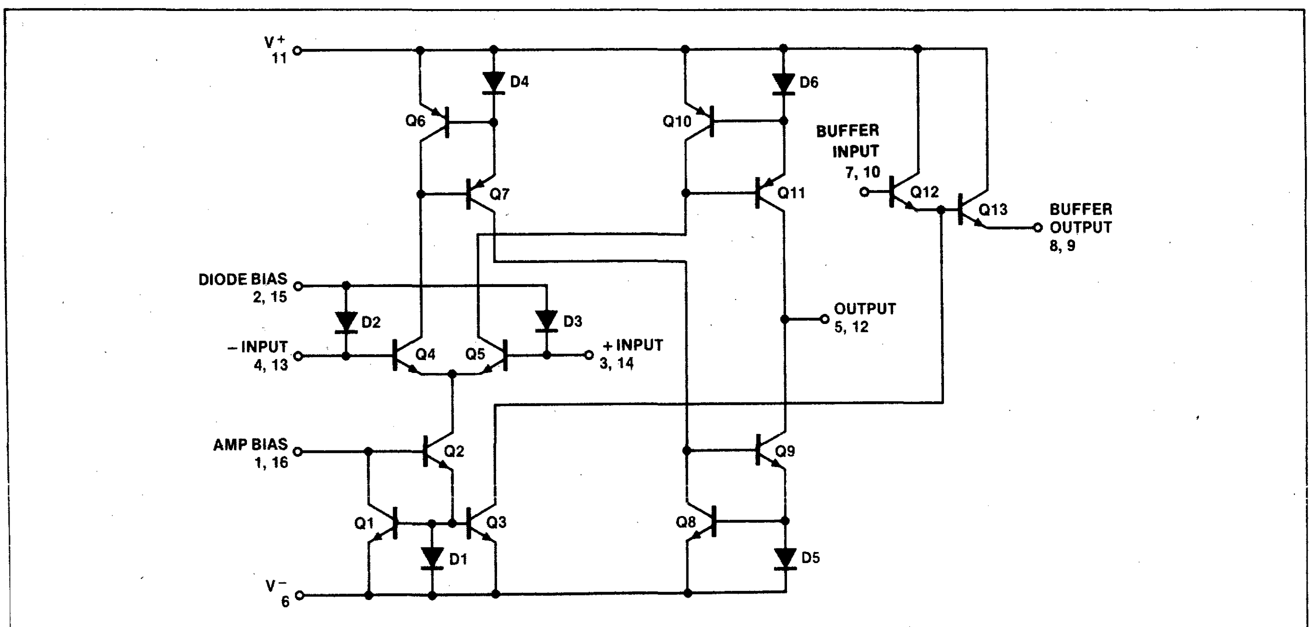
ORDER NUMBERS
LM13600N LM13600D
LM13600AN

NOTE
See Signetics NE5517 for typical circuit applications information.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage[1]		
LM13600	36 V_{DC} or ±18	V
LM13600A	44 V_{DC} or ±22	V
Power dissipation[2] T_A = 25°C		
LM13600N, LM13600AN	570	mW
Differential input voltage	±5	V
Diode bias current (I_D)	2	mA
Amplifier bias current (I_{ABC})	2	mA
Output short circuit duration	Indefinite	
Buffer output current[3]	20	mA
Operating temperature range		
LM13600N, LM13600AN	0°C to +70	°C
DC input voltage	$+V_S$ to $-V_S$	
Storage temperature range	−65°C to +150	°C
Lead temperature (Soldering, 10 Seconds)	300	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	LM13600			LM13600A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage (V_{OS})	 Over specified temperature range I_{ABC} 5μA		0.4 0.3	5 5		0.4 0.3	2 5 2	mV mV mV
$\Delta V_{OS}/\Delta T$	Over temperature		7			7		μV/°C
V_{OS} including diodes	Diode Bias Current (I_D) = 500 μA		0.5	5		0.5	2	mV
Input offset change	5 μA ≤ I_{ABC} ≤ 500 μA		0.1			0.1	3	mV
Input offset current			0.1	0.6		0.1	0.6	μA
$\Delta I_{OS}/\Delta T$	Over temperature		0.001			0.001		μA/°C
Input bias current	 Over temperature range		0.4 1	5 8		0.4 1	5 7	μA μA
$\Delta I_B/\Delta T$	Over temperature		0.01			0.01		μA/°C
Forward Transconductance (gm)	 Over temperature range	 6700 5400	 9600	 13000	 7700 4000	 9600	 12000	 μmho μmho
gm tracking			0.3			0.3		dB
Peak output current	RL = 0, I_{ABC} = 5μA RL = 0, I_{ABC} = 500 μA RL = 0, Over temp range	 350 300	5 500	 650	3 350 300	5 500	7 650	μA μA μA
Peak output voltage positive negative	 RL = ∞, 5 μA ≤ I_{ABC} ≤ 500 μA RL = ∞, 5 μA ≤ I_{ABC} ≤ 500 μA	 +12 −12	 +14.2 −14.4		 +12 −12	 +14.2 −14.4		 V V
Supply current	I_{ABC} = 500 μA, Both channels		2.6	4		2.6	4	mA
V_{OS} sensitivity positive negative	 $\Delta V_{OS}/\Delta$ V+ $\Delta V_{OS}/\Delta$ V−		 20 20	 150 150		 20 20	 150 150	 μV/V μV/V
CMRR		80	110		80	110		dB
Common mode range		±12	±13.5		±12	±13.5		V
Crosstalk	Referred to input[5] 20 Hz < f < 20 KHz		 100			 100		 dB
Diff. input current	I_{ABC} = 0, Input = ±4V		0.02	100		0.02	10	nA
Leakage current	I_{ABC} = 0 (Refer to test circuit)		0.2	100		0.2	5	nA
Input resistance		10	26		10	26		KΩ
Open loop bandwith			2			2		MHz
Slew rate	Unity gain compensated		50			50		V/μSec
Buff. input current	5		0.4	5		0.4	5	μA
Peak buffer output voltage	5	10			10			V

NOTES
1. For selections to a supply voltage above ±22V, contact factory.
2. For operating at high temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175° C/W which applies for the device soldered in a printed circuit board, operating in still air.
3. Buffer output current should be limited so as to not exceed package dissipation.
4. These specifications apply for V_S = ± 15V, T_A = 25°C, amplifier bias current (I_{ABC}) = 500μA, pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.
5. These specifications apply for V_{SS} = ± 15V, I_{ABC} = 500 μA, R_{OUT} = 5KΩ connected from the buffer output to $-V_S$ and the input of the buffer is connected to the transconductance amplifier output.

LINEAR

Signetics

DUAL HIGH PERFORMANCE OPERATIONAL AMPLIFIER — NE/SE5512

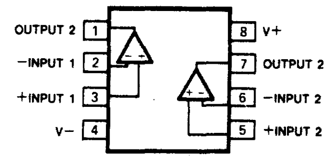
DESCRIPTION
The 5512 series of high performance operational amplifier provides very good input characteristics. These amplifiers feature low input bias and voltage characteristics such as a 108 op amp with improved CMRR and a high differential input voltage limit achieved through the use of a bias cancellation and PNP input circuits with collector to emitter clamping. The output characteristics are like those of a 741 op amp with improved slew rate and drive capability yet have low supply quiescent current.

APPLICATIONS
- AC amplifiers
- RC active filters
- Transducer amplifiers
- DC gain block
- Battery operation
- Instrumentation amplifiers

FEATURES
- **Low input bias < ±3nA**
- **Low input offset current < ±3nA**
- **Low input offset voltage < 1mV**
- **Low V_{OS} temperature drift 4μV/°C**
- **Low input bias temperature drift 30pA/°C**
- **Low input voltage noise 25nV/√Hz**
- **Low supply current 1.5mA/amp**
- **High slew rate 1.0V/μs**
- **High CMRR 100dB**
- **High input impedance 100MΩ**
- **High PSRR 110dB**
- **High differential input voltage limit**
- **No cross-over distortion**
- **Indefinite output short circuit protection**
- **Internally compensated for unity gain**

PIN CONFIGURATIONS

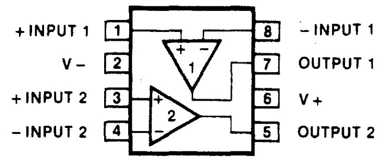
FE,N PACKAGE



TOP VIEW

ORDER NUMBERS
NE/SE5512FE NE/SE5512N

D PACKAGE



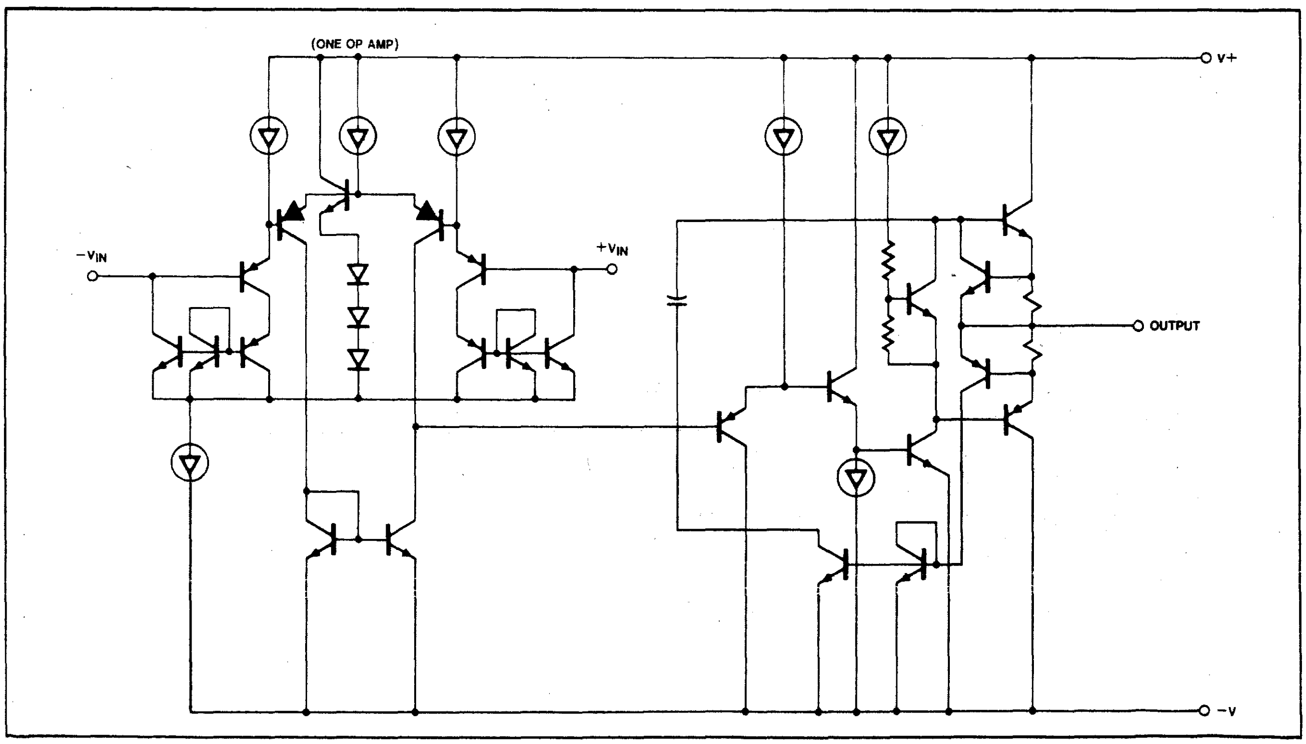
TOP VIEW

ORDER NUMBER
NE5512D

ABSOLUTE MAXIMUM RATINGS

	Parameter	Rating	Unit
V_{CC}	Supply Voltage	±16	V
V_D	Power dissipation	500	mW
T_A	Operating temperature range		
	NE5512	0 to 70	°C
	SE5512	−55 to +125	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead temperature soldering	300	°C

EQUIVALENT SCHEMATIC



DUAL HIGH PERFORMANCE OPERATIONAL AMPLIFIER — NE/SE5512

ELECTRICAL PERFORMANCE CHARACTERISTICS $V_{CC} = \pm 15V$, F.R. = −55°C to +125°C (SE), 0°C to +70°C (NE)

	PARAMETER	TEST CONDITIONS	SE5512			NE5512			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS} ΔV_{OS}	Input offset voltage	$R_S = 100\Omega$ $T_A = +25°C$ T_A = F.R. Over Temp.		0.7 1 4	2 3		1 1.5 5	5 6	mV μV/°C
I_{OS} ΔI_{OS}	Input offset current	$R_S = 100k\Omega$ $T_A = +25°C$ T_A = F.R. Over Temp.		3 4 30	10 20		6 8 40	20 30	nA pA/°C
I_B ΔI_B	Input bias current	$R_S = 100k\Omega$ T = +25°C T_A = F.R. Over Temp.		3 4 30	10 20		6 8 40	20 30	nA pA/°C
R_{IN}	Input resistance differential	$T_A = 25°C$		100			100		MΩ
V_{CM}	Input common mode range	$T_A = 25°C$ T_A = F.R.	±13.5 ±13	±13.7 ±13.2		±13.5 ±13	±13.7 ±13.2		V
CMRR	Input common-mode rejection ratio	$V_{CC} = \pm 15V$ $V_{IN} = \pm 13.5V$ (RM) $T_A = 25°C$ $V_{IN} = \pm 13V$ (F.R.) T_A = F.R.	70	100		70	100		dB
A_{VOL} GAIN	Large-signal voltage gain	$R_L = 2k\Omega$ $T_A = 25°C$ $V_O = \pm 10V$ T_A = F.R.	50 25	200		50 25	200		V/mV
S.R.	Slew rate	$T_A = 25°C$	0.6	1			1		V/μs
GBW	Small-signal unity gain bandwidth	$T_A = 25°C$		3			3		MHz
θ_M	Phase margin	$T_A = 25°C$		45			45		Degree
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$ $T_A = 25°C$ T_A = F.R.	±13 ±12.5	±13.5 ±13		±13 ±12.5	±13.5 ±13		V
V_{OUT}	Output voltage swing	$R_L = 600\Omega$* $T_A = 25°C$ T_A = F.R.	±10 ±7.5	±11.5 ±9		±10 ±8	±11.5 ±9		V
I_{CC}	Power supply current	R_L = Open $T_A = 25°C$ T_A = F.R.		3.4 3.6	5 5.5		3.4 3.6	5 5.5	mA
P_{SRR}	Power supply rejection ratio	$T_A = 25°C$ T_A = F.R.	80 80	110 100		80 80	110 100		dB
AA	Amplifier to amplifier coupling	f = 1kHz to 20kHz $T_A = 25°C$		−120			−120		dB
HD	Total harmonic distortion	f = 10kHz $T_A = 25°C$ $V_O = 7V_{RMS}$		0.01			0.01		%
V_{IN_N}	Input noise voltage	f = 1kHz $T_A = 25°C$		30			30		nV/$\sqrt{Hz}$
I_{IN_N}	Input noise current	f = 1kHz $T_A = 25°C$		.2			.2		pA/$\sqrt{Hz}$
I_{SC}	Short circuit	±15V $T_A = 25°C$		40			40		mA

NOTE
For operation at elevated temperature, N package must be derated based on a thermal resistance of 120°/W junction to ambient. Thermal resistance of the FE package is 125°/W.

QUAD HIGH PERFORMANCE OP AMP

NE/SE5514

DESCRIPTION

The NE/SE5514 family of Quad Operational Amplifiers sets new standards in Bipolar Quad Amplifier Performance. The amplifiers feature low input bias current and low offset voltages. Pin-out is identical to LM324/LM348 which facilitates direct product substitution for improved system performance. Output characteristics are similar to a μA741 with improved slew and drive capability.

FEATURES

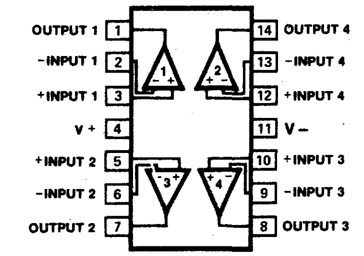
- **Low input bias current: $<\pm 3nA$**
- **Low input offset current: $<\pm 3nA$**
- **Low input offset voltage: $<1mV$**
- **Low supply current: 1.5mA/Amp**
- **1 V/μsec slew rate**
- **High input impedance: 100MΩ**
- **High common mode impedance: 10GΩ**
- **Internal compensation for unity gain**

APPLICATIONS

- **AC amplifiers**
- **RC active filters**
- **Transducer amplifiers**
- **DC gain block**
- **Instrumentation amplifier**

PIN CONFIGURATION

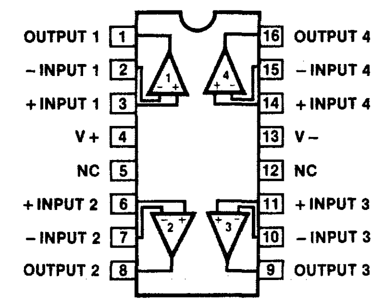
F,N PACKAGE



TOP VIEW

ORDER NUMBERS
NE5514F, N   SE5514F, N

D[1] PACKAGE



TOP VIEW

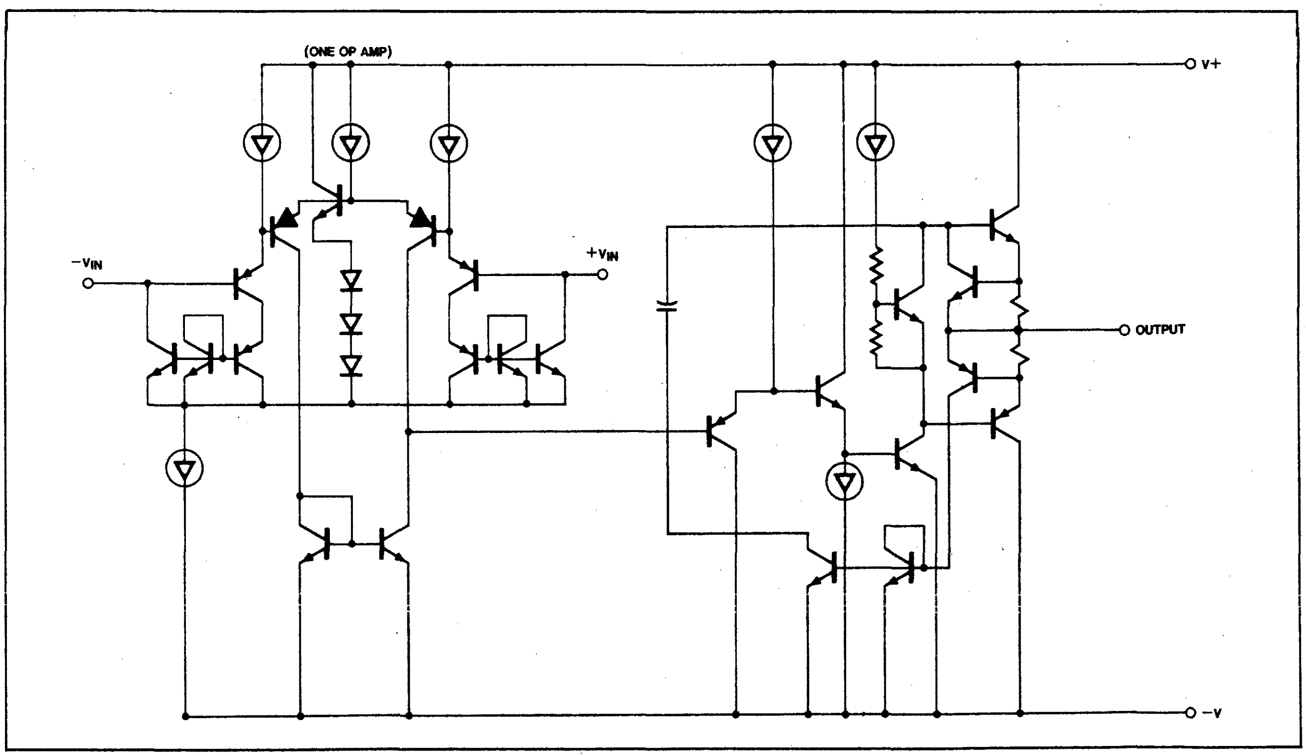
ORDER NUMBER
NE5514D[1]

NOTE:
1. Supplied only in large SO (Small Outline) package.

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	±16	V
V_{DIFF}	Differential input voltage	32	V
V_{IN}	Input voltage	0 to 32	V
	Output short to ground	Continuous	
T_S	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature	300	°C
T_A	Operating temperature range		
	NE5514	0 to 70	°C
	SE5514	−55 to +125	°C

EQUIVALENT SCHEMATIC



QUAD HIGH PERFORMANCE OP AMP

NE/SE5514

ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 15V$, F.R. = −55°C (SE) 0°C to 70°C (NE)

PARAMETER		TEST CONDITIONS	SE5514			NE5514			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS} ΔV_{OS}	Input offset voltage	$R_S = 100\Omega$, $T_A = +25°C$, T_A = F.R. Over temp.		0.7 1 4	2 3		1 1.5 5	5 6	mV μV/°C
I_{OS} ΔI_{OS}	Input offset current	$R_S = 100k\Omega$, $T_A = +25°C$, T_A = F.R. Over temp.		3 4 30	10 20		6 8 40	20 30	nA pA/°C
I_B ΔI_B	Input bias current	$R_S = 100k\Omega$, $T_A = +25°C$, T_A = F.R. Over temp.		3 4 30	10 20		6 8 40	20 30	nA pA/°C
R_{IN}	Input resistance differential	$T_A = 25°C$		100			100		MΩ
V_{CM}	Input common mode range	$T_A = 25°C$, T_A = F.R.	±13.5 ±13.5	±13.7 ±13.2		±13.5 ±13	±13.7 ±13.2		V
CMRR	Input common-mode rejection ratio	$V_{CC} = \pm 15V$, $V_{IN} = \pm 13.5V$ (RM), $T_A = 25°C$, $V_{IN} = \pm 13V$ (F.R.), T_A = F.R.	70	100		70	100		dB
AVOL GAIN	Large-signal voltage gain	$R_L = 2k\Omega$, $T_A = 25°C$ $V_C = \pm 10V$, T_A = F.R.	50 25	200		50 25			V/mV
S.R.	Slew rate	$T_A = 25°C$	0.6	1		0.6	1		V/μs
GBW	Small-signal unity gain bandwidth	$T_A = 25°C$		3			3		MHz
θ_M	Phase margin	$T_A = 25°C$		45			45		Degr
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$, $T_A = 25°C$, T_A = F.R.	±13 ±12.5	±13.5 ±13		±13 ±12.5	±13.5 ±13		V
V_{OUT}	Output voltage swing	$R_L = 600\Omega$*, $T_A = 25°C$, T_A = F.R.	±10 ±7.5	±11.5 ±9		±10 ±8	±11.5 ±9		V
I_{CC}	Power supply current	R_L = Open, $T_A = 25°C$, T_A = F.R.		6 7	10 12		6 7	10 12	mA
PSRR	Power supply rejection ratio	$T_A = 25°C$, T_A = F.R.	80 80	110 100		80 80	110 100		dB
AA	Amplifier to amplifier coupling	f = 1kHz to 20kHz, $T_A = 25°C$		−120			−120		dB
HD	Total harmonic distortion	f = 10kHz, $T_A = 25°C$, V_O = 7VRMS		0.01			0.01		%
V_{INN}	Input-noise voltage	f = 1kHz, $T_A = 25°C$		30			30		nV/√Hz
I_{SC}	Short Circuit	$T_A = 25°C$	10	40	60	10	40	60	mA

NOTE

*For operation at elevated temperature, N package must be derated based on a thermal resistance of 95°C/W junction to ambient.

DUAL OPERATIONAL TRANSCONDUCTANCE AMPLIFIER NE5517/5517A

DESCRIPTION

The NE5517 contains two current controlled transconductance amplifiers, each with a differential input and push-pull output. The NE5517 offers significant design and performance advantages over similar devices for all types of programmable gain applications. Constant impedance buffers are provided which effectively eliminate changes in output offset voltage as the amplifier bias current is varied. Circuit performance is enhanced through the use of linearizing diodes at the inputs which enable a 10 dB signal to noise improvement referenced to .5 percent THD. The NE5517 is suited for a wide variety of industrial and consumer applications and is recommended as the preferred circuit in the Dolby* HX (Headroom Extension) system.

FEATURES

- **Constant impedance buffers**
- **ΔV_{BE} of buffer is constant with amplifier I_{BIAS} change**
- **Pin compatible with LM13600**
- **Excellent matching between amplifiers**
- **Linearizing diodes**
- **High output signal-to-noise ratio**

APPLICATIONS

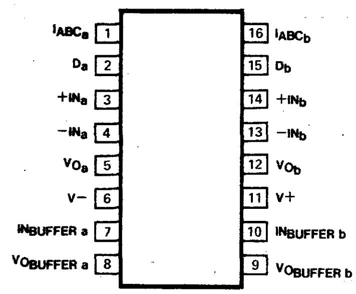
- **Multiplexers**
- **Timers**
- **Electronic music synthesizers**
- **Dolby* HX Systems**
- **Current-controlled amplifiers, filters**
- **Current-controlled oscillators, impedances**

NOTE

*Dolby is a registered trademark of Dolby Laboratories Inc., San Francisco, Calif.

PIN CONFIGURATION

D,N PACKAGE



TOP VIEW

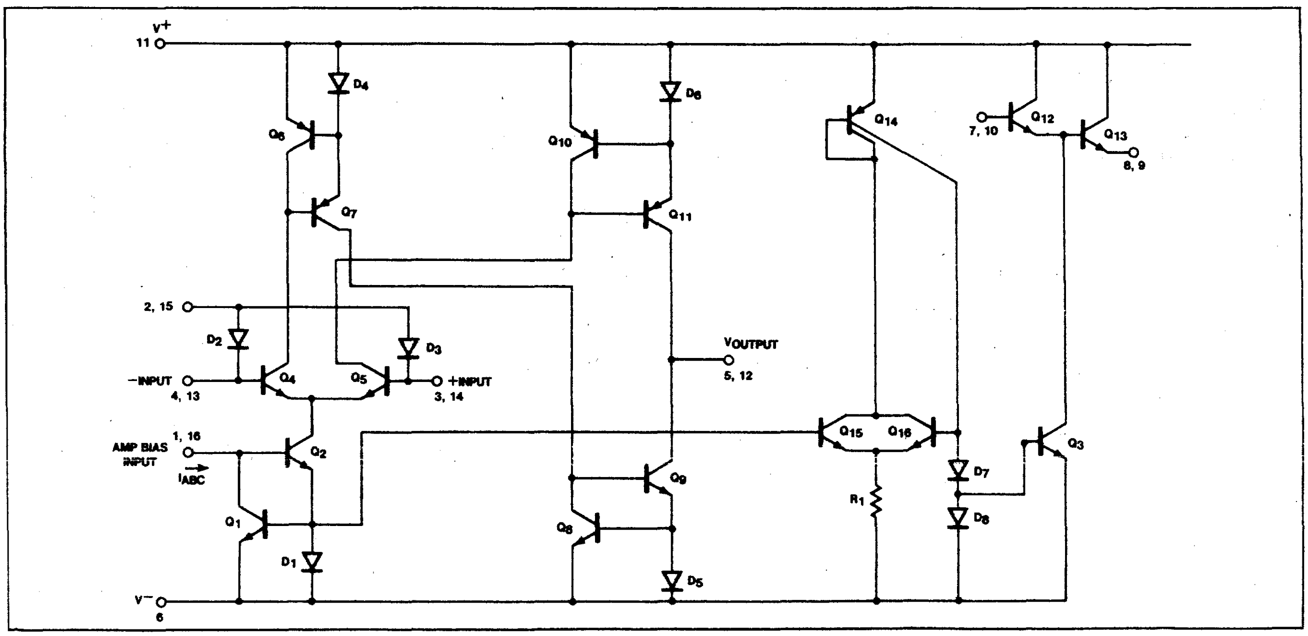
ORDER NUMBERS

NE5517N NE5517D NE5517AN

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply Voltage[1]		
NE5517	36 V_{DC} or ±18	V
NE5517A	44 V_{DC} or ±22	V
Power Dissipation[2] $T_A = 25°C$		
NE5517N, NE5517AN	570	mW
Differential Input Voltage	±5	V
Diode Bias Current (I_D)	2	mA
Amplifier Bias Current (I_{ABC})	2	mA
Output Short Circuit Duration	Indefinite	
Buffer Output Current[3]	20	mA
Operating Temperature Range		
NE5517N, NE5517AN	0°C to +70	°C
DC Input Voltage	$+V_S$ to $-V_S$	
Storage Temperature Range	−65°C to +150	°C
Lead Temperature (Soldering, 10 Seconds)	300	°C

CIRCUIT SCHEMATIC



DUAL OPERATIONAL TRANSCONDUCTANCE AMPLIFIER NE5517/5517A

ELECTRICAL CHARACTERISTICS[4]

PARAMETER	TEST CONDITIONS	NE5517 Min	NE5517 Typ	NE5517 Max	NE5517A Min	NE5517A Typ	NE5517A Max	UNIT
Input offset voltage (V_{OS})			0.4	5		0.4	2	mV
	Over temperature range						5	mV
	I_{ABC} 5μA		0.3	5		0.3	2	mV
$\Delta V_{OS}/\Delta T$	Avg. TC of input offset voltage		7			7		μV/°C
V_{OS} including diodes	Diode bias current (I_D) = 500μA		0.5	5		0.5	2	mV
Input offset change	5μA ≤ I_{ABC} ≤ 500μA		0.1			0.1	3	mV
Input offset current			0.1	0.6		0.1	0.6	μA
$\Delta I_{OS}/\Delta T$	Avg. TC of input offset current		0.001			0.001		μA/°C
Input bias current			0.4	5		0.4	5	μA
	Over temperature range		1	8		1	7	μA
$\Delta I_B/\Delta T$	Avg. TC of input current		0.01			0.01		μA/°C
Forward Transconductance (gm)		6700	9600	13000	7700	9600	12000	μmho
	Over temperature range	5400			4000			μmho
gm tracking			0.3			0.3		dB
Peak output current	RL = 0, I_{ABC} = 5μA		5		3	5	7	μA
	RL = 0, I_{ABC} = 500μA	350	500	650	350	500	650	μA
	RL = 0,	300			300			μA
Peak output voltage								
Positive	RL = ∞, 5μA ≤ I_{ABC} ≤ 500μA	+12	+14.2		+12	+14.2		V
Negative	RL = ∞, 5μA ≤ I_{ABC} ≤ 500μA	−12	−14.4		−12	−14.4		V
Supply current	I_{ABC} = 500μA, both channels		2.6	4		2.6	4	mA
V_{OS} sensitivity								
Positive	$\Delta V_{OS}/\Delta V+$		20	150		20	150	μV/V
Negative	$\Delta V_{OS}/\Delta V-$		20	150		20	150	μV/V
CMRR		80	110		80	110		dB
Common mode range		±12	±13.5		±12	±13.5		V
Crosstalk	Referred to input[5] 20Hz < f < 20kHz		100			100		dB
Diff. input current	I_{ABC} = 0, input = ±4V		0.02	100		0.02	10	nA
Leakage current	I_{ABC} = 0 (Refer to test circuit)		0.2	100		0.2	5	nA
Input resistance		10	26		10	26		KΩ
Open loop bandwidth			2			2		MHz
Slew rate	Unity gain compensated		50			50		V/μSec
Buff. input current	5		0.4	5		0.4	5	μA
Peak buffer output voltage	5	10			10			V
ΔV_{BE} of buffer	6 Refer to Buffer V_{BE} test circuit		0.5	5		0.5	5	mV

NOTES
1. For selections to a supply voltage above ±22V, contact factory.
2. For operating at high temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175° C/W which applies for the device soldered in a printed circuit board, operating in still air.
3. Buffer output current should be limited so as to not exceed package dissipation.
4. These specifications apply for V_S = ±15V, T_A = 25°C, amplifier bias current (I_{ABC}) = 500μA, pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.
5. These specifications apply for V_S = ±15V, I_{ABC} = 500μA, R_{OUT} = 5kΩ connected from the buffer output to $-V_S$ and the input of the buffer is connected to the transconductance amplifier output.
6. V_S = ±15, R_{OUT} = 5KΩ connected from Buffer output to $-V_S$ and 5μA ≤ I_{ABC} ≤ 500μA.

LINEAR

Signetics

INTERNALLY COMPENSATED DUAL LOW NOISE OP AMP — NE/SE5532/5532A

DESCRIPTION

The 5532 is a dual high-performance low noise operational amplifier. Compared to most of the standard operational amplifiers, such as the 1458, it shows better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

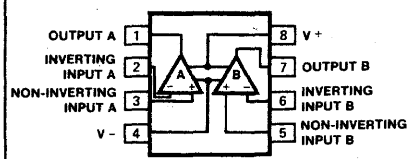
This makes the device especially suitable for application in high quality and professional audio equipment, instrumentation and control circuits, and telephone channel amplifiers. The op amp is internally compensated for gains equal to one. If very low noise is of prime importance, it is recommended that the 5532A version be used which has guaranteed noise voltage specifications.

FEATURES

- Small-signal bandwidth: 10MHz
- Output drive capability: 600Ω, 10V (rms)
- Input noise voltage: $5nV/\sqrt{Hz}$ (typical)
- DC voltage gain: 50000
- AC voltage gain: 2200 at 10kHz
- Power bandwidth: 140kHz
- Slew-rate: 9V/μs
- Large supply voltage range: ±3 to ±20V

PIN CONFIGURATION

FE,N PACKAGE



TOP VIEW

ORDER NUMBERS

NE5532FE, N — SE5532FE

NE5532AFE, N — SE5532AFE

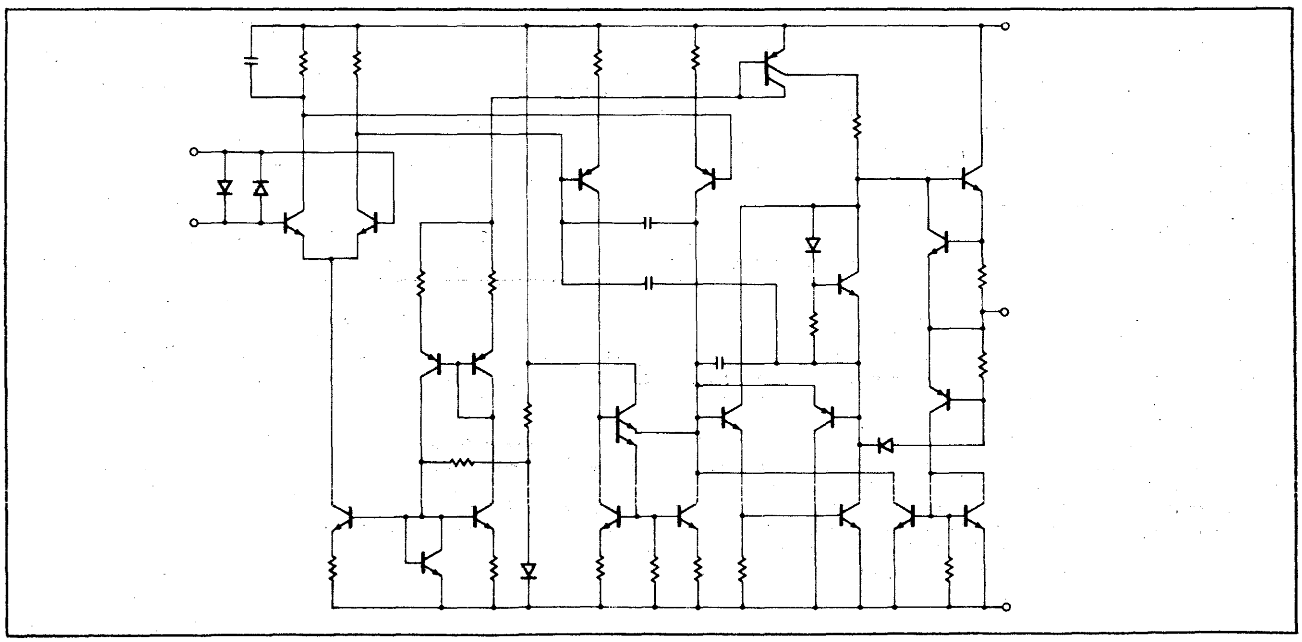
ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_S	Supply voltage	±22	V
V_{IN}	Input voltage	±V supply	V
V_{DIFF}	Differential input voltage[1]	±.5	V
T_A	Operating temperature range	0 to 70	°C
T_{STG}	Storage temperature	−65 to +150	°C
T_J	Junction temperature	150	°C
P_D	Power dissipation		
	5532FE	1000	mW
	Lead temperature (soldering, 10 sec)	300	°C

NOTES:

1. Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ± 10mA.
2. Thermal resistance of the FE package is 125°C/W.

EQUIVALENT SCHEMATIC (EACH AMPLIFIER)



INTERNALLY COMPENSATED DUAL LOW NOISE OP AMP NE/SE5532/5532A

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.[1,2]

PARAMETER		TEST CONDITIONS	SE5532/55232A			NE5532/5532A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage			0.5	2		0.5	4	mV
		Over temperature			3			5	mV
$\Delta V_{OS}/\Delta T$				5			5		μV/°C
I_{OS}	Offset current				100		10	150	nA
		Over temperature			200			200	nA
$\Delta I_{OS}/\Delta T$				200			200		pA/°C
I_B	Input current			200	400		200	800	nA
		Over temperature			700			1000	nA
$\Delta I_B/\Delta T$				5			5		mA/°C
I_{CC}	Supply current						8	16	mA
		Over temperature			13				mA
V_{CM}	Common mode input range		±12	±13		±12	±13		V
CMRR	Common mode rejection ratio		80	100		70	100		dB
PSRR	Power supply rejection ratio			10	50		10	100	μV/V
A_{VOL}	Large signal voltage gain	$R_L \geq 2k\Omega$, $V_0 = \pm 10V$	50			25	100		V/mV
		Over temperature	25			15			V/mV
		$R_L \geq 600\Omega$, $V_0 = \pm 10V$	40			15	50		V/mV
		Over temperature	20			10			V/mV
V_{OUT}	Output swing	$R_L \geq 600\Omega$				±12	±13		V
		Over temperature				±10	±12		V
		$R_L \geq 600\Omega$, $V_S = \pm 18V$	±15	±16		V			
		Over temperature				±12	±14		V
		$R_L \geq 2k\Omega$ over temp.	±12	±13		±10	±13		V
R_{IN}	Input resistance		30	300		30	300		kΩ
I_{SC}	Output short circuit current		10	38	60	10	38	60	mA

NOTES
1. For NE5532, NE5532A, $T_{Min} = 0°C$, $T_{Max} = 70°C$.
2. For SE5532/5532A, $T_{Min} = -55°C$, $T_{Max} = +125°C$.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	NE/SE5532/5532A			UNIT
			Min	Typ	Max	
R_{OUT}	Output resistance	$A_V = 30dB$ Closed loop $f = 10kHz$, $R_L = 600\Omega$		0.3		Ω
	Overshoot	Voltage follower $V_{IN} = 100mV$ p-p $C_L = 100pF$ $R_L = 600\Omega$		10		%
	Gain	$f = 10kHz$		2.2		V/mV
	Gain bandwidth product	$C_L = 100pF$ $R_L = 600\Omega$		10		MHz
	Slew rate			9		V/μs
	Power bandwidth	$V_{OUT} = \pm 10V$ $V_{OUT} = \pm 14V$, $R_L = 600\Omega$, $V_{CC} = \pm 18V$		140 100		kHz kHz

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	NE/SE5532			NE/SE5532A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input noise voltage	$f_o = 30Hz$		8			8	12	$nV/\sqrt{Hz}$
	$f_o = 1kHz$		5			5	6	$nV/\sqrt{Hz}$
Input noise current	$f_o = 30Hz$		2.7			2.7		$pA/\sqrt{Hz}$
	$f_o = 1kHz$		0.7			0.7		$pA/\sqrt{Hz}$
Channel separation	$f = 1kHz$, $RS = 5k\Omega$		110			110		dB

SINGLE AND DUAL LOW NOISE OP AMP NE5533/5533A / NE/SE5534/5534A

DESCRIPTION

The 5533/5534 are dual and single high-performance low noise operational amplifiers. Compared to other operational amplifiers, such as TL083, they show better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

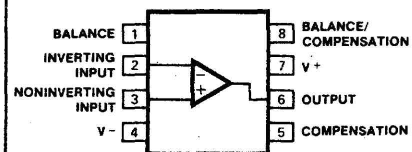
This makes the devices especially suitable for application in high quality and professional audio equipment, in instrumentation and control circuits and telephone channel amplifiers. The op amps are internally compensated for gain equal to, or higher than, three. The frequency response can be optimized with an external compensation capacitor for various applications (unity gain amplifier, capacitive load, slew-rate, low overshoot, etc.) If very low noise is of prime importance, it is recommended that the 5533A/5534A version be used which has guaranteed noise specifications.

FEATURES

- **Small-signal bandwidth: 10MHz**
- **Output drive capability: 600Ω, 10V (rms) at $V_S = \pm 18V$**
- **Input noise voltage: 4nV/$\sqrt{Hz}$**
- **DC voltage gain: 100000**
- **AC voltage gain: 6000 at 10kHz**
- **Power bandwidth: 200kHz**
- **Slew-rate: 13V/μs**
- **Large supply voltage range: ±3 to ±20V**

PIN CONFIGURATIONS

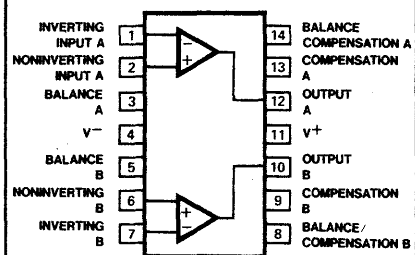
D,FE,N PACKAGE



TOP VIEW

ORDER NUMBERS
NE/SE5534N, FE NE/SE5534AN, FE
NE5534D

N PACKAGE



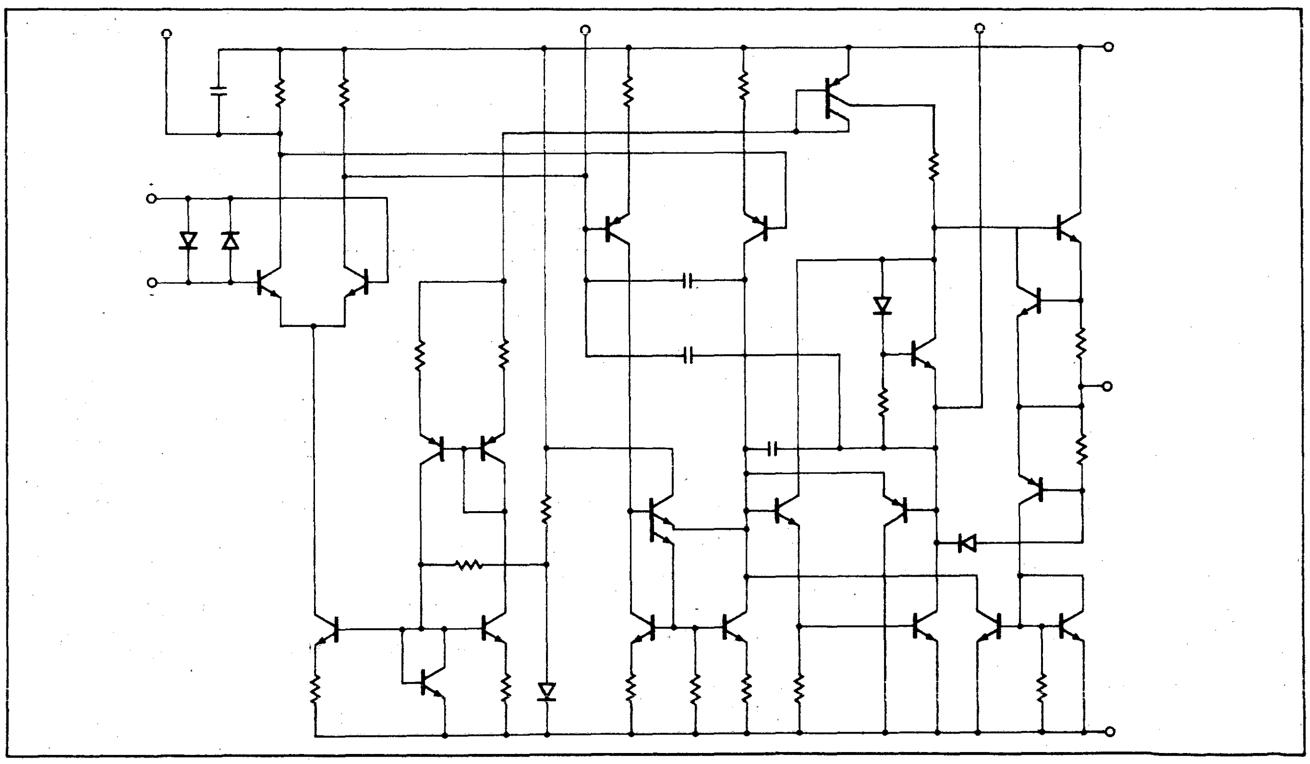
TOP VIEW

ORDER NUMBERS
NE5533N
NE5533AN

LINEAR

Signetics

EQUIVALENT SCHEMATIC



AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm15V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE5534/5534A			NE5533/5533A 5534/5534A			UNIT
		Min	Typ	Max	Min	Typ	Max	
R_{OUT} Output resistance	$A_V = 30dB$ closed loop $f = 10kHz$, $R_L = 600\Omega$, $C_C = 22pF$		0.3			0.3		Ω
Transient response T_R Rise time Overshoot	Voltage follower, $V_{IN} = 50mV$ $R_L = 600\Omega$, $C_C = 22pF$, $C_L = 100pF$		20 20			20 20		ns %
Transient response T_R Rise time Overshoot	$V_{IN} = 50mv$, $R_L = 600\Omega$ $C_C = 47pF$, $C_L = 500pF$		50 35			50 35		ns %
AC Gain	$f = 10kHz$, $C_C = 0$ $f = 10kHz$, $C_C = 22pF$		6 2.2			6 2.2		V/mV V/mV
Gain bandwidth product	$C_C = 22pF$, $C_L = 100pF$		10			10		mHz
Slew rate	$C_C = 0$ $C_C = 22pF$		13 6			13 6		V/μS V/μS
Power bandwidth	$V_{OUT} = \pm10V$, $C_C = 0$ $V_{OUT} = \pm10V$, $C_C = 22pF$ $V_{OUT} = \pm14V$, $R_L = 600\Omega$ $C_C = 22pF$, $V_{CC} = \pm18V$		200 95 70			200 95 70		kHz kHz kHz

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm15V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	5533/5534			5533A/5534A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input noise voltage	$f_o = 30Hz$ $f_o = 1kHz$		7 4			5.5 3.5	7 4.5	$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
Input noise current	$f_o = 30Hz$ $f_o = 1kHz$		2.5 0.6			1.5 0.4		$pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$
Broadband noise figure	$f = 10Hz - 20kHz$, $R_S = 5k\Omega$					0.9		dB
Channel separation	$f = 1kHz$, $R_S = 5k\Omega$		110			110		dB

LINEAR

Signetics

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_S	Supply voltage	± 22	V
V_{IN}	Input voltage	± V supply	V
V_{DIFF}	Differential input voltage[1]	± 0.5	V
T_A	Operating temperature range		
	SE5534/5534A	− 55 to + 125	°C
	NE5533/5533A/5534/5534A	0 to + 70	°C
T_{STG}	Storage temperature	− 65 to + 150	°C
T_J	Junction temperature	150	°C
P_D	Power dissipation at 25°C[2]		
	5533N, 5534N, 5534FE	800	mW
	Output short circuit duration[3]	indefinite	
	Lead temperature (soldering, 10 sec)	300	°C

NOTES

1. Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ±10mA.
2. For operation at elevated temperature, derate packages based on the following junction-to-ambient thermal resistances:
   8-pin ceramic (FE) 140°C/W
   14-pin ceramic (F) 110°C/W
   8-pin plastic (N) 162°C/W
   14-pin plastic (N) 150°C/W
3. Output may be shorted to ground at V_S = ±15V, T_A = 25°C. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.[1,2]

PARAMETER		TEST CONDITIONS	SE5534/5534A			NE5533/5533A 5534/5534A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage			0.5	2		0.5	4	mV
		Over temperature			3			5	mV
$\Delta V_{OS}/\Delta T$				5			5		μV/°C
I_{OS}	Offset current			10	200		20	300	nA
		Over temperature			500			400	nA
$\Delta I_{OS}/\Delta T$				200			200		pA/°C
I_B	Input current			400	800		500	1500	nA
		Over temperature			1500			2000	nA
$\Delta I_B/\Delta T$				5			5		nA/°C
I_{CC}	Supply current			4	6.5		4	8	mA
	Per op amp	Over temperature			9			10	mA
V_{CM}	Common mode input range		± 12	± 13		± 12	± 13		V
CMRR	Common mode rejection ratio		80	100		70	100		dB
PSRR	Power supply rejection ratio			10	50		10	100	μV/V
A_{VOL}	Large signal voltage gain	$R_L \geq 600\Omega$, $V_O = \pm 10V$	50	100		25	100		V/mV
		Over temperature	25			15			V/mV
V_{OUT}	Output swing	$R_L \geq 600\Omega$	± 12	± 13		± 12	± 13		V
	5534 only	Over temperature	± 10	± 12		± 10	± 12		V
		$R_L \geq 600\Omega$, $V_S = \pm 18V$	± 15	± 16		± 15	± 16		V
		$R_L \geq 2k\Omega$	± 13	± 13.5		± 13	± 13.5		V
		Over Temperature	± 12	± 12.5		± 12	± 12.5		V
R_{IN}	Input resistance		50	100		30	100		kΩ
I_{SC}	Output short circuit current			38			38		mA

NOTES

1. For NE5533/5533A/5534/5534A, $T_{MIN} = 0°C$, $T_{MAX} = 70°C$
2. For SE5534/5534A, $T_{MIN} = -55°C$, $T_{MAX} = +125°C$

LINEAR

Signetics

PHASE LOCKED LOOP

NE/SE564

DESCRIPTION

The NE564 is a versatile, high guaranteed frequency Phase Locked Loop designed for operation up to 50MHz. As shown in the block diagram, the NE564 consists of a VCO, limiter, phase comparator, and post detection processor.

APPLICATIONS

- High speed modems
- FSK receivers and transmitters
- Frequency synthesizers
- Signal generators
- Various satcom/TV systems

FEATURES

- Operation with single 5V supply
- TTL compatible inputs and outputs
- Guaranteed operation to 50MHz
- External loop gain control
- Reduced carrier feedthrough
- No elaborate filtering needed in FSK applications
- Can be used as a modulator
- Variable loop gain (Externally Controlled)

ABSOLUTE MAXIMUM RATINGS

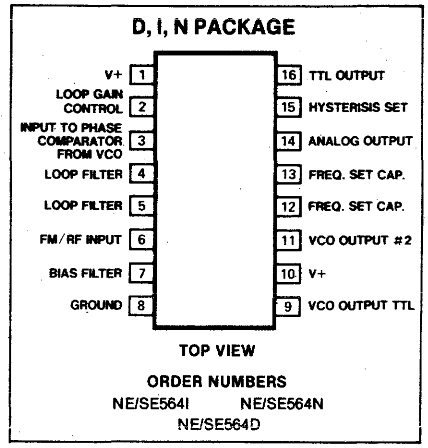
	PARAMETER		RATING	UNIT
V+	Supply voltage			V
	Pin 1		14	
	Pin 10		6	
P_D	Power dissipation		600	mW
T_A	Operating temperature	NE	0 to 70	°C
,	Operating temperature	SE	−55 to +125	
t_{stg}	Storage temperature		−65 to 150	°C

NOTE:
Operation above 5 volts will require heatsinking of the case.

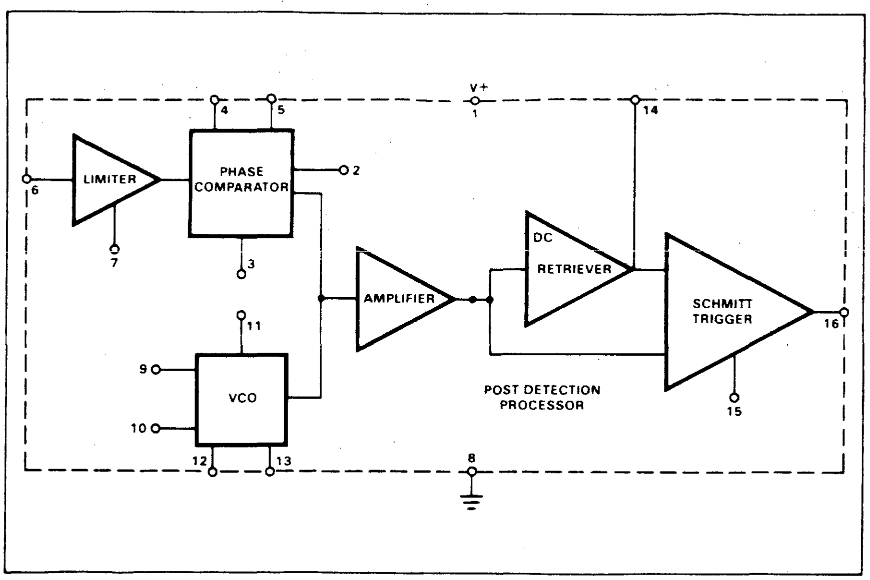
OUTLINE OF SETUP PROCEDURE

1. Determine operating frequency of the VCO−.
   If ÷ N in feedback loop, then $f_o = N \times f_{in}$.
2. Calculate value of the VCO frequency set capacitor:
   $$C_O \approx \frac{1}{2500\, f_o}$$
3. Set I_2 (current sinking into Pin 2) for ≅ 200µA. After operation is obtained, this value may be adjusted for best dynamic behavior.
4. Check VCO output frequency with digital counter at Pin 9 of device (loop open, VCO to ϕ det.). Adjust C_O trim or frequency adj. Pin 4-5 for exact center frequency if needed.
5. Close loop and inject input signal to Pin 6. Monitor Pin 3 and 6 with two channel scope. Lock should occur with $\Delta\phi_{3-6}$ equal to 90° (phase error).
6. If pulsed burst or ramp frequency is used for input signal, special loop filter design may be required in place of simple single capacitor filter on Pin 4 and 5. (See PLL application section in Analog Manual.)
7. The input signal to Pin 6 and the VCO feedback signal to Pin 3 must have a duty cycle of 50% for proper operation of the phase detector. Due to the nature of a balanced mixer if signals are not 50% in duty cycle, D.C. offsets will occur in the loop which tend to create an artificial or biased VCO offset.
8. For multiplier circuits where phase jitter is a problem, loop filter capacitors may be increased to a value of 10-50µF on Pin 4, 5. Also careful supply decoupling may be necessary. This includes the counter chain V_{CC} lines.

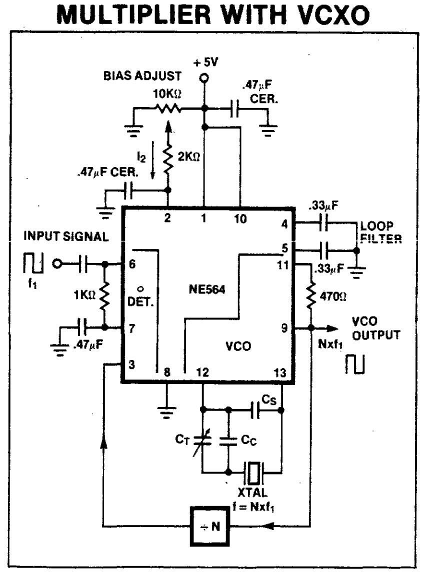
PIN CONFIGURATION



BLOCK DIAGRAM



NE564 PHASE LOCKED FREQUENCY MULTIPLIER WITH VCXO



PHASE LOCKED LOOP

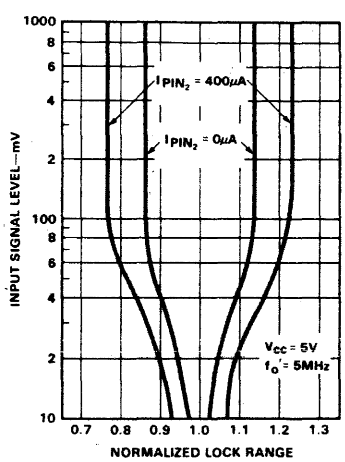
NE/SE564

ELECTRICAL CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$, $f_o = 5MHz$, $I_B = 400\mu A$ unless otherwise specified

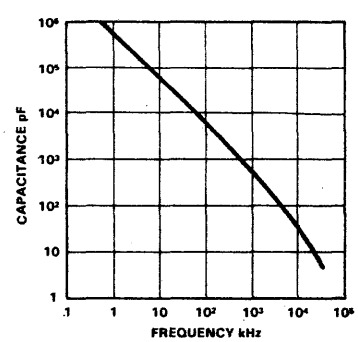
PARAMETER	TEST CONDITIONS	SE564			NE564			UNIT
		Min	Typ	Max	Min	Typ	Max	
Maximum VCO frequency	$C_1 = 0$	50	65		45	60		MHz
Lock range	Input ≥ 200mVrms $T_A = 25°C$	40	70		40	70		% of f_o
	$= 125°C$	20	30					
	$= -55°C$	50	80					
	$= 0°C$					70		
	$= 70°C$					40		
Capture range	Input ≥ 200mVrms, $R_2 = 27\Omega$	20	30		20	30		% of f_o
VCO frequency drift with temperature	$f_o = 5MHz$, $T_A = -55°C$ to $125°C$		400	1000				PPM/°C
	$= 0°C$ to $70°C$					400	1250	
	$f_o = 500KHz$, $T_A = -55°C$ to $125°C$		250	500				
	$= 0°C$ to $70°C$					400	850	
VCO free running frequency	$f_o = \frac{1}{25R_CC_1}$, $C_1 = 80pF$, $R_C = 100\Omega$ "Internal"	4	5	6	3.5	5	7	MHz
VCO frequency change with supply voltage	$V_{CC} = 4.5V$ to $5.5V$		3	8		3	8	% of f_o
Demodulated output voltage	Modulation frequency: 1KHz $f_o = 5MHz$, input deviation:							
	2%T = 25°C	16	28		16	28		mVrms
	1%T = 25°C	8	14		8	14		mVrms
	= 0°C					13		mVrms
	= −55°C	6	10					mVrms
	= 70°C					15		mVrms
	= 125°C	12	16					mVrms
Distortion	Deviation: 1% to 8%		1			1		%
Signal to noise ratio	Std. condition, 1% to 10% dev.		40			40		dB
AM rejection	Std. condition, 30% AM		35			35		dB
Demodulated Output at operating voltage	Modulation frequency: 1KHz $f_o = 5MHz$, input deviation: 1%							
	$V_{CC} = 4.5V$	7	12		7	12		mVrms
	$V_{CC} = 5.5V$	8	14		8	14		mVrms
Supply current	$V_{CC} = 5V$ I_1, I_{10}		45	60		45	60	mA
Output								
"1" output leakage current	$V_{OUT} = 5V$, Pin 16, 9		1	20		1	20	μA
"0" output voltage	$I_{OUT} = 2mA$, Pin 16, 9		0.3	0.6		0.3	0.6	V
	$I_{OUT} = 6mA$, Pin 16, 9		0.4	0.8		0.4	0.8	V

TYPICAL PERFORMANCE CHARACTERISTICS

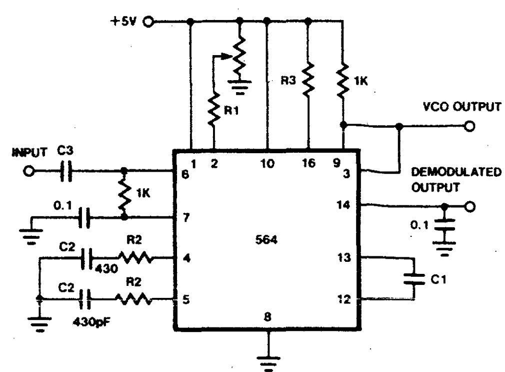
LOCK RANGE vs SIGNAL INPUT



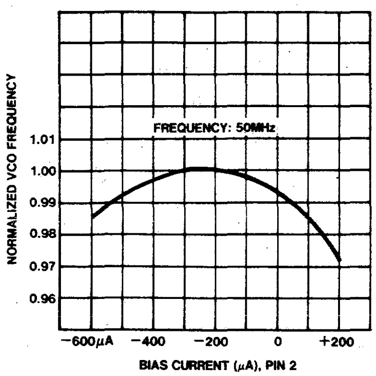
VCO CAPACITOR vs FREQUENCY



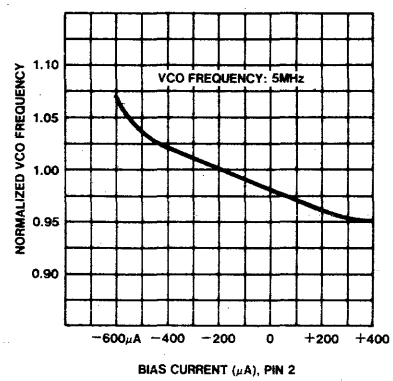
SE/NE 564 TEST CIRCUIT



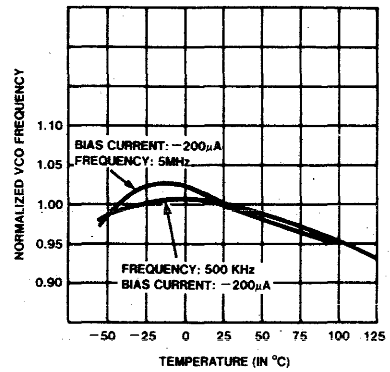
TYPICAL NORMALIZED VCO FREQUENCY AS A FUNCTION OF PIN 2 BIAS CURRENT



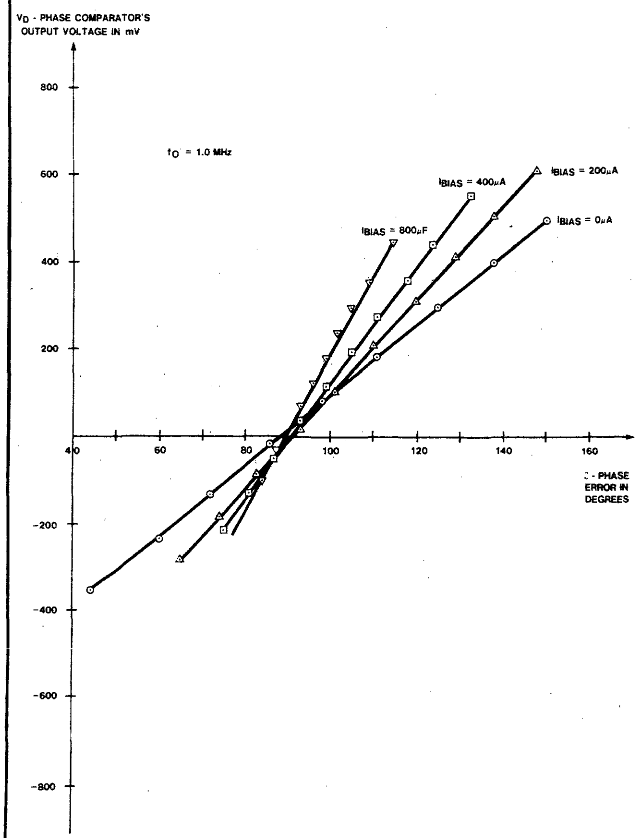
TYPICAL NORMALIZED VCO FREQUENCY AS A FUNCTION OF PIN 2 BIAS CURRENT



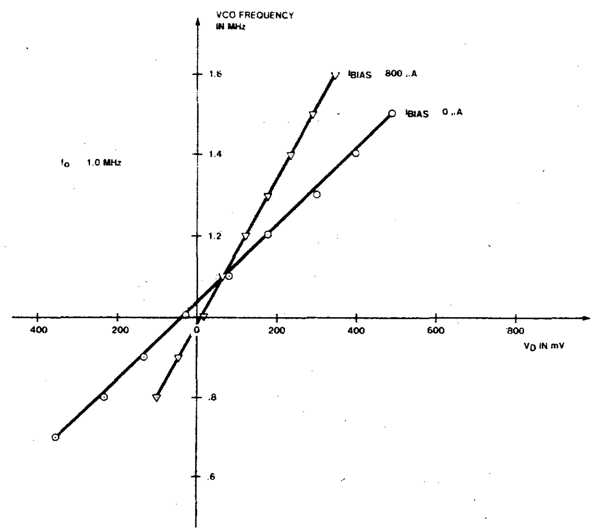
NORMALIZED VCO FREQUENCY AS A FUNCTION OF TEMPERATURE



VARIATION OF THE PHASE COMPARATOR'S OUTPUT VOLTAGE VERSUS PHASE ERROR AND BIAS CURRENT (K_D)



VCO OUTPUT FREQUENCY AS A FUNCTION OF INPUT VOLTAGE AND BIAS CURRENT (K_O)



SWITCHED-MODE POWER SUPPLY CONTROL CIRCUIT — NE/SE5560

DESCRIPTION

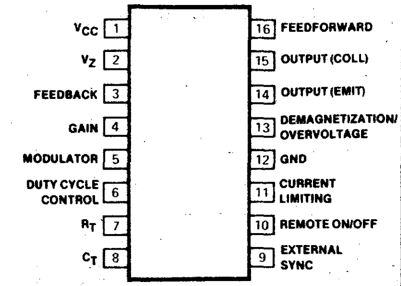
The NE/SE5560 is a control circuit for use in switched mode power supplies. This single monolithic chip incorporates all the control and housekeeping (protection) functions required in switched mode power supplies, including an internal temperature compensated reference source, internal Zener reference, sawtooth generator, pulse width modulator, output stage and various protection circuits.

FEATURES

- **Stabilized power supply**
- **Temperature compensated reference source**
- **Sawtooth generator**
- **Pulse width modulator**
- **Remote on/off switching**
- **Current limiting**
- **Low supply voltage protection**
- **Loop fault protection**
- **Demagnetization/overvoltage protection**
- **Maximum duty cycle clamp**
- **Feed forward control**
- **External synchronization**

PIN CONFIGURATION

D,F,N PACKAGE



TOP VIEW

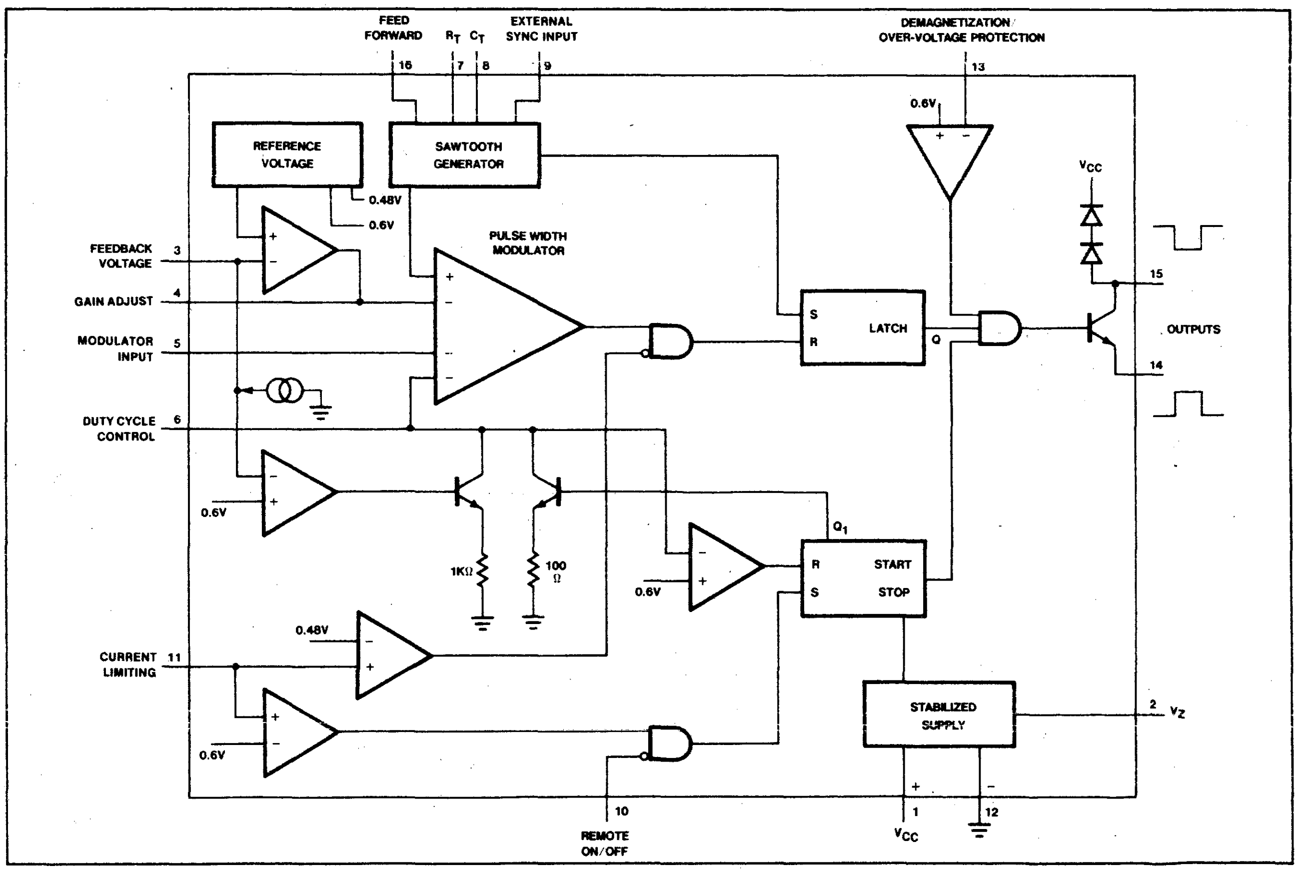
ORDER NUMBERS

NE5560N SE5560F
NE5560D SE5560N
NE5560F

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply		
Voltage sourced	+18	V
Current sourced	30	mA
Output transistor		
Output current	40	mA
Collector voltage (Pin 15)	+18	V
Max. emitter voltage (Pin 14)	+5	V
Operating temperature (ambient)		
SE5560	−55 to +125	°C
NE5560	0 to 70	°C
Storage temperature range	−65 to +150	°C

BLOCK DIAGRAM



SWITCHED-MODE POWER SUPPLY CONTROL CIRCUIT NE/SE5560

DC ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_{CC} = 12V$ unless otherwise specified)

PARAMETER	TEST CONDITIONS	SE5560			NE5560			UNIT
		Min	Typ	Max	Min	Typ	Max	
Reference Sections								
Internal reference voltage (V_{ref})	25°C	3.69	3.72	3.81	3.57	3.72	3.95	V
	Over temperature	3.65		3.85	3.53		4.00	V
Temperature coefficient of V_{ref}			-100			-100		ppm/°C
Internal Zener reference (V_Z)	$I_L = -7$ mA	7.8	8.4	9.0	7.8	8.4	9.0	V
Temperature coefficient of V_Z			200			-200		ppm/°C
Oscillator Section								
Frequency range	Over temperature	50		100k	50		100k	Hz
Initial accuracy oscillator	R = 5 kΩ		5			5		%
Duty cycle range	$f_o = 20$ kHz	0		98	0		98	%
Modulator								
Modulation input current	Voltage at Pin 5 = 2V Over temperature		0.2	20		0.2	20	μA
Housekeeping Function								
Pin 6, input current	at 2V Over temperature		0.2	20		0.2	20	μA
Pin 6, duty cycle limit control	(for 50% maximum duty cycle) 15 kHz to 50 kHz/ 41% of V_Z	40	50	60	40	50	60	% of duty cycle
Pin 1, low supply voltage protection thresholds		8	9.0	10.5	8	9.0	10.5	V
Pin 3, feedback loop protection trip threshold		400	600	720	400	600	720	mV
Pin 3, pull up current	at 2V Over temperature	-7	-15	-35	-7	-15	-35	μA
Pin 13, demagnetization/over voltage protection trip on threshold		470	600	720	470	600	720	mV
Pin 13, input current	at 0.25V 25°C		0.6	10		0.6	10	μA
	Over temperature			20			20	
Pin 16, feed forward duty cycle control	Voltage at Pin 16 = $2V_Z$	30	40	50	30	40	50	% original duty cycle
*Pin 16, feed forward input current	at 16V, $V_{CC} = 18V$ 25°C		0.2	5		0.2	5	μA
	Over temperature			10			10	μA
External Synchronization								
Pin 9 off		0		0.8	0		0.8	V
on		2		V_Z	2		V_Z	V
sink current	Voltage at Pin 9 = 0V, 25°C		-65	-100		-65	-125	μA
	Over temperature			-125			-125	μA
Remote								
Pin 10 off		0	0.8		0	0.8		V
on		2	V_Z		2	V_Z		V
sink current	at 0V 25°C		-85	-100		-85	-125	μA
	Over temperature			-125			-125	μA
Current Limiting								
Pin 11, I_{IN}	Voltage at Pin 11 = 250 mV, 25°C		-2	-10		-2	-10	μA
	Over temperature			-20			-20	μA
Single pulse inhibit delay	Inhibit delay time for 20% overdrive at 40 mA I_{OUT}		0.7	0.8		0.7	0.8	μs
Trip Levels: Shut down, slow start		0.560	0.600	0.700	0.560	0.600	0.700	V
Current limit		0.400	0.480	0.500	0.400	0.480	0.500	V
Error Amplifier								
Output voltage swing (V_{OH})		6.2		9.5	6.2		9.5	V
Output voltage swing (V_{OL})				0.7			0.7	V
Open loop gain		54	60		54	60		dB
Feedback resistor		10k			10k			Ω
Small signal bandwidth			3			3		MHz

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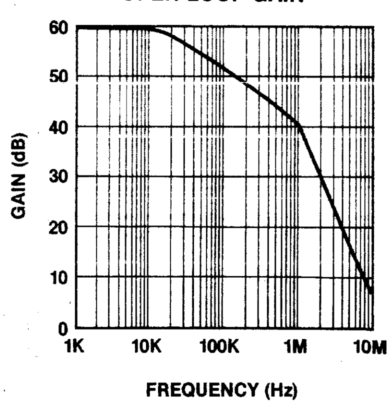
DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	TEST CONDITIONS	SE5560			NE5560			UNIT
		Min	Typ	Max	Min	Typ	Max	
Output Stage								
V_{CE}(SAT) $I_C = 40mA$				0.5			0.5	V
Output current (pin 15)		40			40			mA
Max emitter voltage (pin 14)		5	6		5	6		V
Supply Voltage/Current								
I_{CC}	$I_Z = 0$, voltage fed, $V_{CC} = 12V$, 25°C			10			10	mA
	Over temp.			15			15	mA
V_{CC}	$I_{CC} = 10mA$, current feed	20		23	19		24	V
V_{CC}	$I_{CC} = 30mA$, current feed	20		30	20		30	V

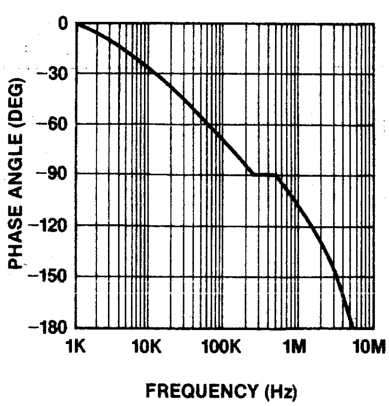
TYPICAL PERFORMANCE CHARACTERISTICS

ERROR AMPLIFIER

OPEN LOOP GAIN



OPEN LOOP PHASE

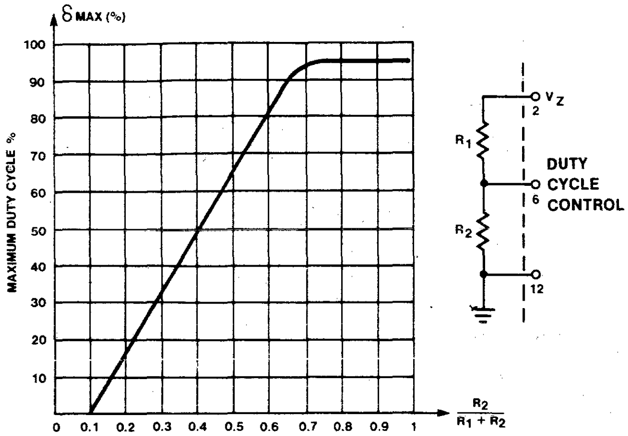


MAXIMUM PIN VOLTAGES

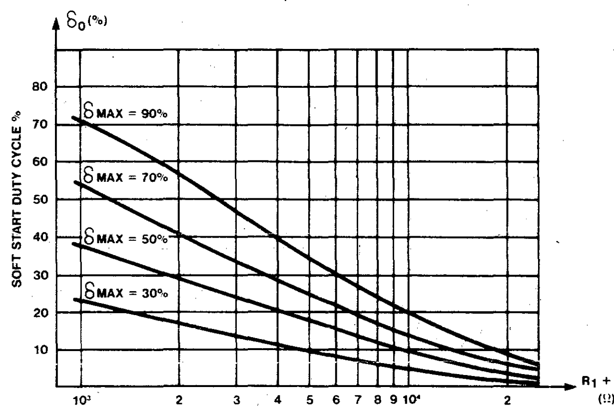
NE5560	
FUNCTION	**MAXIMUM VOLTAGE**
1. V_{CC}	+ 18 volts
2. V_Z	Do not force (28.4V)
3. Feedback	V_Z
4. Gain	
5. Modulator	V_Z
6. Duty Cycle Control	V_Z
7. R_T	Current force mode
8. C_T	
9. External Sync	V_Z
10. Remote On/Off	V_Z
11. Current Limiting	V_{CC}
12. GND	GND
13. Demagnetization/Overvoltage	V_{CC}
14. Output (Emit)	V_Z
15. Output (Collector)	V_{CC} + 2Vbe
16. Feed forward	V_{CC}

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

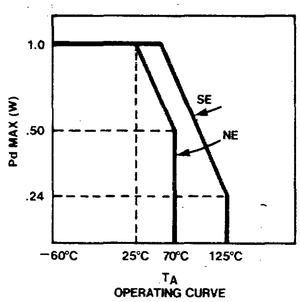
GRAPH FOR DETERMINING δ MAX



SOFT-START MIN DUTY CYCLE vs R1 + R2

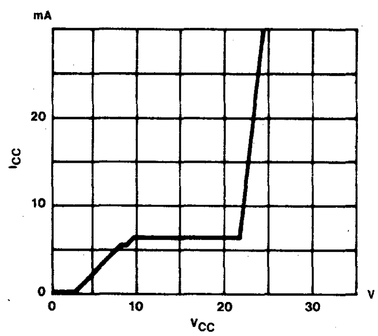


POWER DERATING CURVE

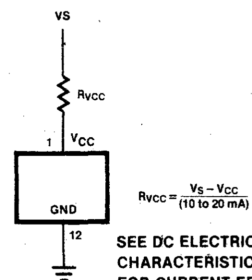


Pd = VCC ICC + (VCC − VZ)IZ
+ [(V15−V14)I15 X DUTY CYCLE]

NE5560 VOLTAGE/CURRENT FED SUPPLY CHARACTERISTICS



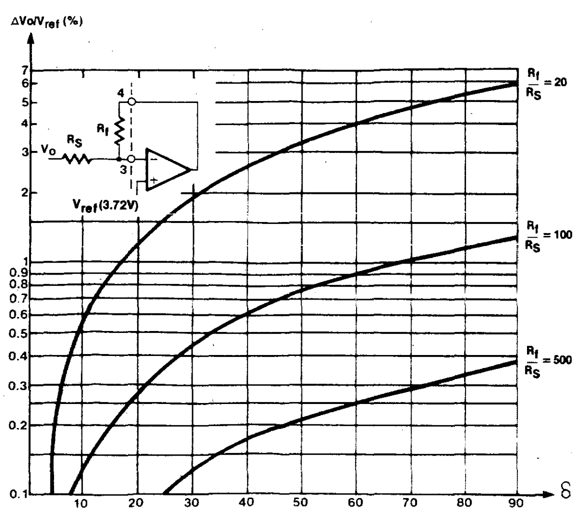
CURRENT FED DROPPING RESISTOR



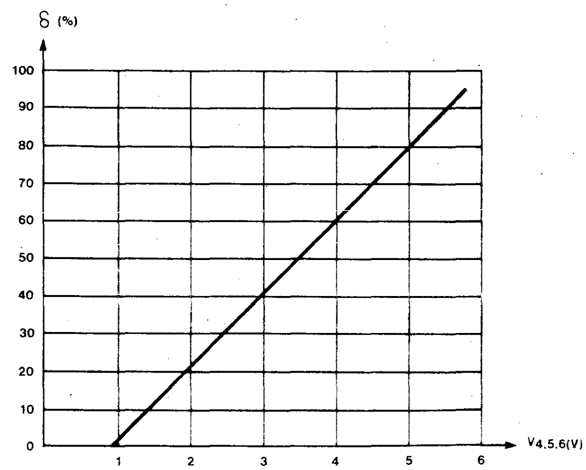
$R_{VCC} = \frac{V_S - V_{CC}}{(10 \text{ to } 20 \text{ mA})}$

SEE DC ELECTRICAL CHARACTERISTICS FOR CURRENT FEED V_{CC} RANGE.

REGULATION vs ERROR AMP CLOSED LOOP GAIN

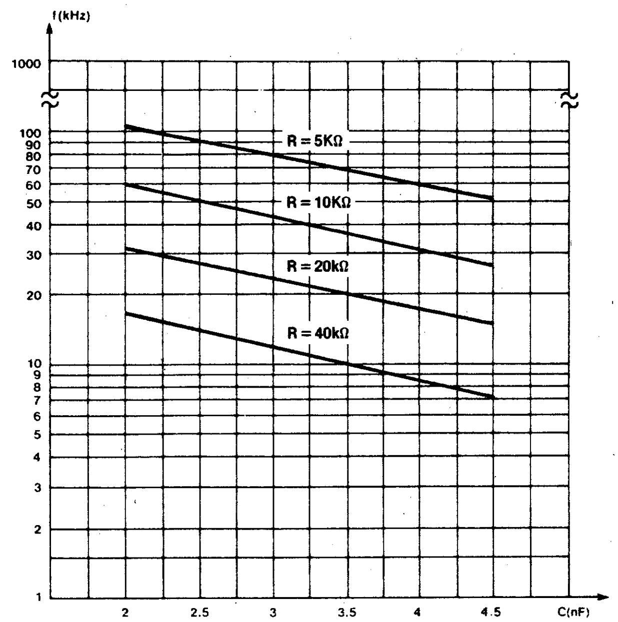


TRANSFER CURVE OF PULSE WIDTH MODULATOR DUTY CYCLE vs INPUT VOLTAGE

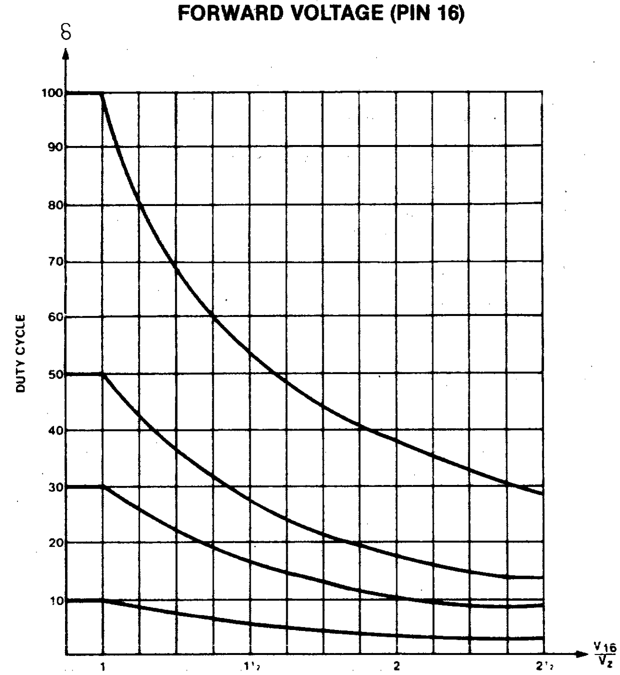


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

TYPICAL FREQUENCY PLOT vs R_T AND C_T



DUTY CYCLE SENSITIVITY TO FEED FORWARD VOLTAGE (PIN 16)



THEORY OF OPERATION

The following functions are incorporated:

- A temperature compensated reference source.
- An error amplifier with pin 3 as input. The output is connected to pin 4 so that the gain is adjustable with external resistors.
- A sawtooth generator with a TTL-compatible synchronization input (pins 7,8,9).
- A pulse-width modulator with a duty-cycle range from 0 to 95%.

(The PWM has two additional inputs:

Pin 6 can be used for a precise setting of δ max.

Pin 5 gives a direct access to the modulator, allowing for real constant current operation:)

- A gate at the output of the PWM provides a simple dynamic current limit.
- A latch that is set by the flyback of the sawtooth and reset by the output pulse of the above-mentioned gate prohibits double pulsing.
- Another latch functions as a start-stop circuit; it provides a fast switch-off and a slow start.
- A current protection circuit that operates via the start-stop circuit. This is a combined function with the current limit circuit, therefore pin 11 has two trip-on levels; the lower one for cycle-by-cycle current limiting, the upper one for current protection by means of switch-off and slow-start.
- A TTL-compatible remote on/off input at pin 10, also operating via the start-stop circuit.
- An inhibit input at pin 13. The output pulse can be inhibited immediately.
- An output gate that is commanded by the latches and the inhibit circuit.
- An output transistor of which both the collector (pin 15) and the emitter (pin 14) are externally available. This allows for normal or inverse output pulses.
- A power supply that can be either voltage or current driven (pins 1 and 12). The internally generated stabilized output voltage V_Z is connected to pin 2.
- A special function is the so-called feed-forward at pin 16. The amplitude of the sawtooth generator is modulated in such a way that the duty cycle becomes inversely proportional to the voltage on this pin: $\delta \sim 1/V16$
- Loop fault protection circuits assure that the duty-cycle is reduced to zero or a low value for open or short-circuited feedback loops.

Stabilized Power Supply (Pins 1, 2, 12)

The power supply of the NE5560 is of the well known series regulation type and provides a stablized output voltage of typically 8.5 volts.

This voltage V_Z is also present at pin 2 and can be used for precise setting of δ max. and to supply external circuitry. Its maximum current capability is 5mA.

The circuit can be fed directly from a DC voltage source between 10.5V and 18V or can be current driven via a limiting resistor. In the latter case, internal pinch-off resistors will limit the maximum supply voltage; typical 23V for 10mA and maximum 30V for 30mA.

The low supply voltage protection is active when V(1-12) is below 10.5V and inhibits the output pulse (no hysteresis).

When the supply voltage surpasses the 10.5V level, the IC starts delivering output pulses via the slow-start function.

The current consumption at 12V is less than 10mA, provided that no current is drawn from V_Z and R(7-12) ≥ 20kΩ.

SWITCHED MODE POWER SUPPLY CONTROLLER

NE/SE5561

DESCRIPTION

The NE5561/SE5561 is a control circuit for use in switched mode power supplies. It contains an internal temperature compensated supply, PWM, sawtooth oscillator, over-current sense latch, and output stage. The device is intended for low cost SMPS applications where extensive housekeeping functions are not required.

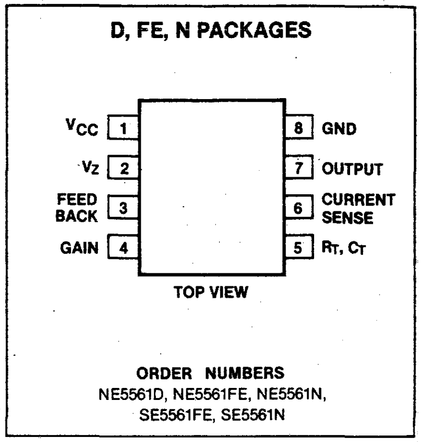
FEATURES

- **Micro-miniature (D) package**
- **Pulse-width modulator**
- **Current limiting (cycle by cycle)**
- **Sawtooth generator**
- **Stabilized power supply**
- **Double pulse protection**
- **Internal temperature compensated reference**

APPLICATIONS

- **Switch mode power supplies**
- **D/C motor controller inverter**
- **DC/DC converter**

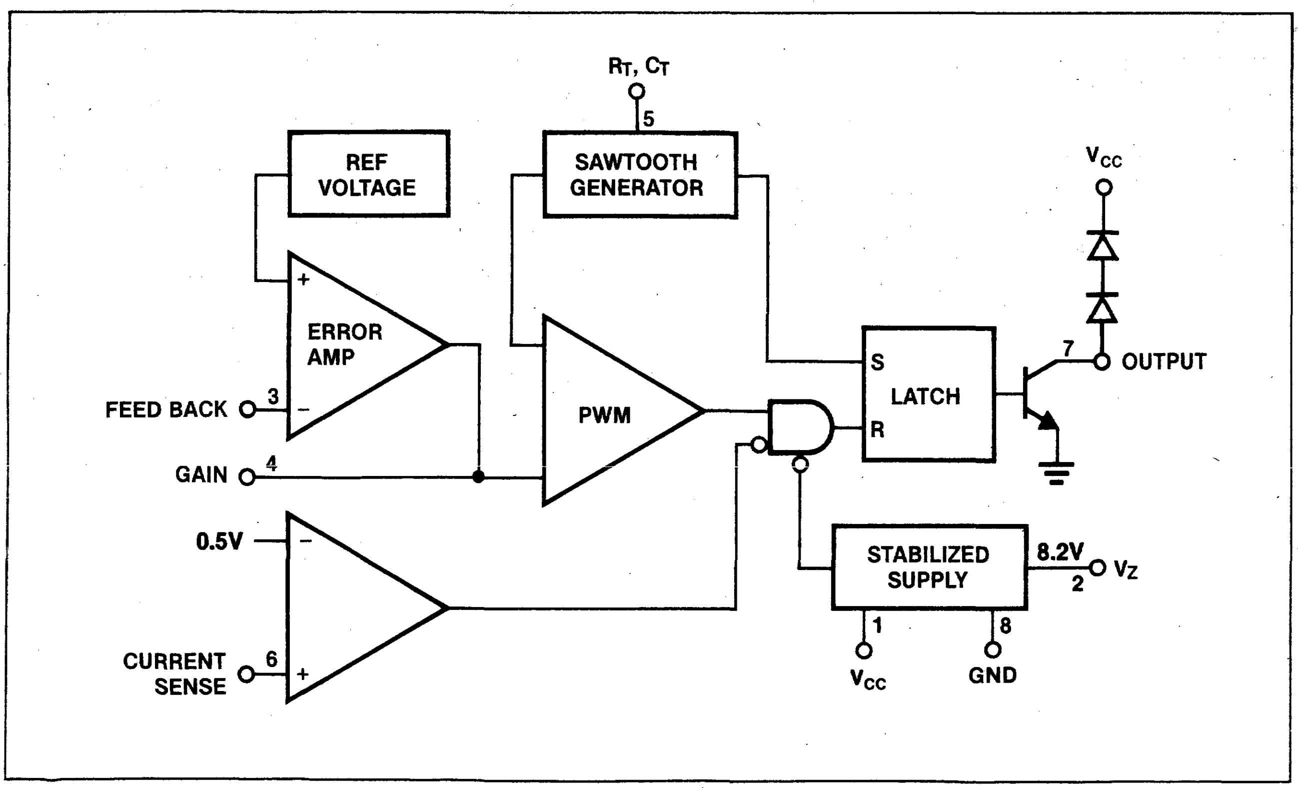
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage, V_{CC}	18	V
Output Current	40	mA
Output duty cycle	98	%
Max total power dissipation	0.75	W
Operating temperature range		
NE5561	0 to 70	°C
SE5561	−55 to +125	°C

BLOCK DIAGRAM



SWITCHED MODE POWER SUPPLY CONTROLLER

NE/SE5561

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 12V$, $T_A = 25°C$ unless otherwise specified.

SYMBOL AND PARAMETER	TEST CONDITIONS		SE5561 Min	SE5561 Typ	SE5561 Max	NE5561 Min	NE5561 Typ	NE5561 Max	UNIT
Reference Section									
V_{REF}, Internal ref voltage	$T_A = 25°C$		3.69	3.75	3.84	3.57	3.75	3.96	V
	Over temp.		3.65		3.88	3.55		3.98	V
V_Z, internal zener ref	$^*I_L = 7mA$		7.8	8.2	8.8	7.8	8.2	8.8	V
Temp coefficient of V_{REF}				± 100			± 100		ppm/°C
Temp coefficient of V_Z				± 200			± 200		ppm/°C
Oscillator Section									
Frequency range	Over temp.		50		100k	50		100k	Hz
Initial accuracy				12			12		%
Duty cycle range	$f_o = 20kHz$		0		98	0		98	%
Current Limiting (I_{IN})	Pin 6 = 250mV	$T_A = 25°C$		−2	−10		−2	−10	μA
		Over temp.			−20			−20	μA
Single pulse inhibit delay	Inhibit delay time for 20% overdrive at	$I_{OUT} = 20mA$		0.88	1.10		0.88	1.10	μs
		$I_{OUT} = 40mA$		0.7	0.8		0.7	0.8	μs
Current limit trip level			.400	.500	.600	.400	.500	.600	V
Error Amplifier									
Open loop gain				60			60		dB
Feedback resistor			10k			10k			Ω
Small signal bandwidth				3			3		MHz
Output voltage swing (V_{OH})			6.2			6.2			V
Output voltage swing (V_{OL})					0.7			0.7	V
Output Stage									
Output current	Over temp.		20			20			mA
V_{ce} Sat	$I_C = 20mA$, over temp.				0.4			0.4	V
Supply Voltage/Current									
I_{CC}	$I_Z = 0$, voltage fed	$T_A = 25°C$			10.0			10.0	mA
		Over temp.			13.0			13.0	mA
V_{CC}	$I_S = 10mA$, current fed		20.0	21.0	22.0	19.0	21.0	24.0	V

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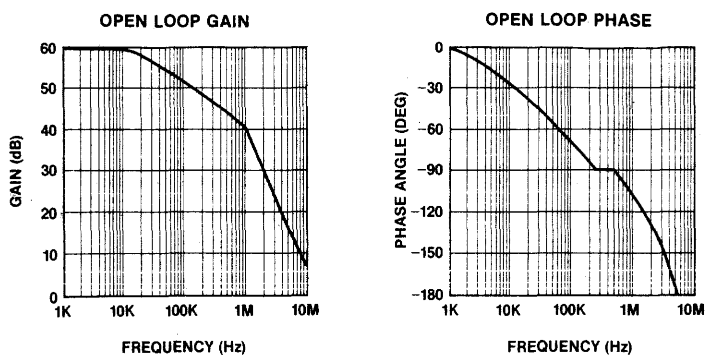
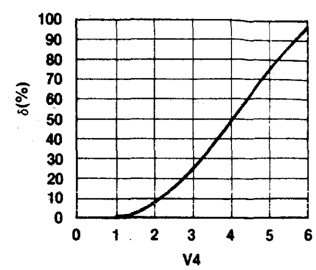
TYPICAL PERFORMANCE CHARACTERISTICS

ERROR AMPLIFIER

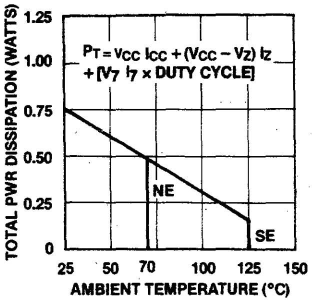


TRANSFER CURVE OF PULSE-WIDTH MODULATOR DUTY CYCLE VS INPUT VOLTAGE

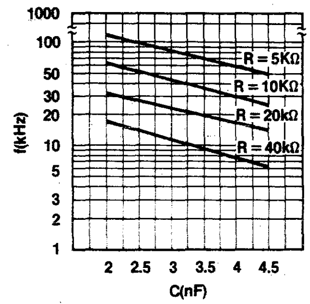


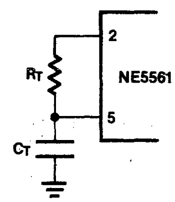
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

POWER DERATING CURVE

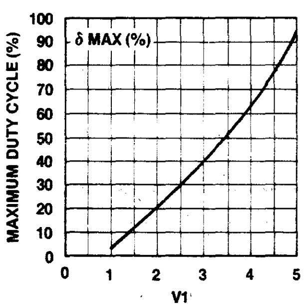


TYPICAL FREQUENCY PLOT VS R_T AND C_T

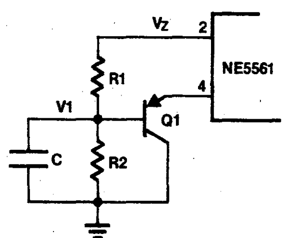




MAXIMUM DUTY CYCLE VS BASE VOLTAGE ON Q1

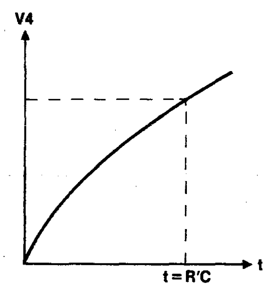


START-UP CIRCUIT



$$\delta_{max} = f\left[\frac{R2}{R1+R2}\; V_Z + V_{BE\,Q1}\right]$$

SLOW START VOLTAGE



NE5561 Start-Up

The start-up, or initial turn on, of this device requires some degree of external protective duty cycle limiting to prevent the duty cycle from initially going to the extreme maximum ($\delta > 90\%$). Either over-current limit or slow start circuitry must be employed to limit duty cycle to a safe value during start-up. Both may be used if desired.

To implement slow-start, the start-up circuit can be used. The divider R1 and R2 sets a voltage, buffered by Q1, such that the output of the error amplifier is clamped to a maximum output voltage, thereby limiting the maximum duty cycle. The addition of capacitor C will cause this voltage to ramp up slowly when power is applied, causing the duty cycle to ramp up simultaneously.

Over-current limit may be used also. To limit duty cycle in this mode, the switch current is monitored at pin 6 and the output of the 5561 is disabled on a cycle by cycle basis when current reaches the programmed limit. With current limit control of slow-start, the duty cycle is limited to that value just allowing maximum switch current to flow. (Approximately 0.50V measured at pin 6.)

APPLICATIONS

5V, 0.5A Buck Regulator Operates from 15V

The converter design shows how simple it is to derive a TTL supply from a system supply of 15V (see Figure 1). The NE5561 drives a 2N4920 PNP transistor directly to provide switching current to the inductor.

Overall line regulation is excellent and covers a range of 12V to 18V with minimal change (< 10 mV) in the output operating at full load.

As with all NE5561 circuits, the auxiliary slow start and δ_{max} circuit is required, as evidenced by Q1. The δ_{max} limit may be calculated by using the relationship (Figure 5a, b).

$$\frac{R2}{R1+R2}(8.2V) = V_{\delta(max)}.$$

The maximum duty cycle is then determined from the pulse-width modulator transfer graph, and R1, R2 are defined from the desired conditions.

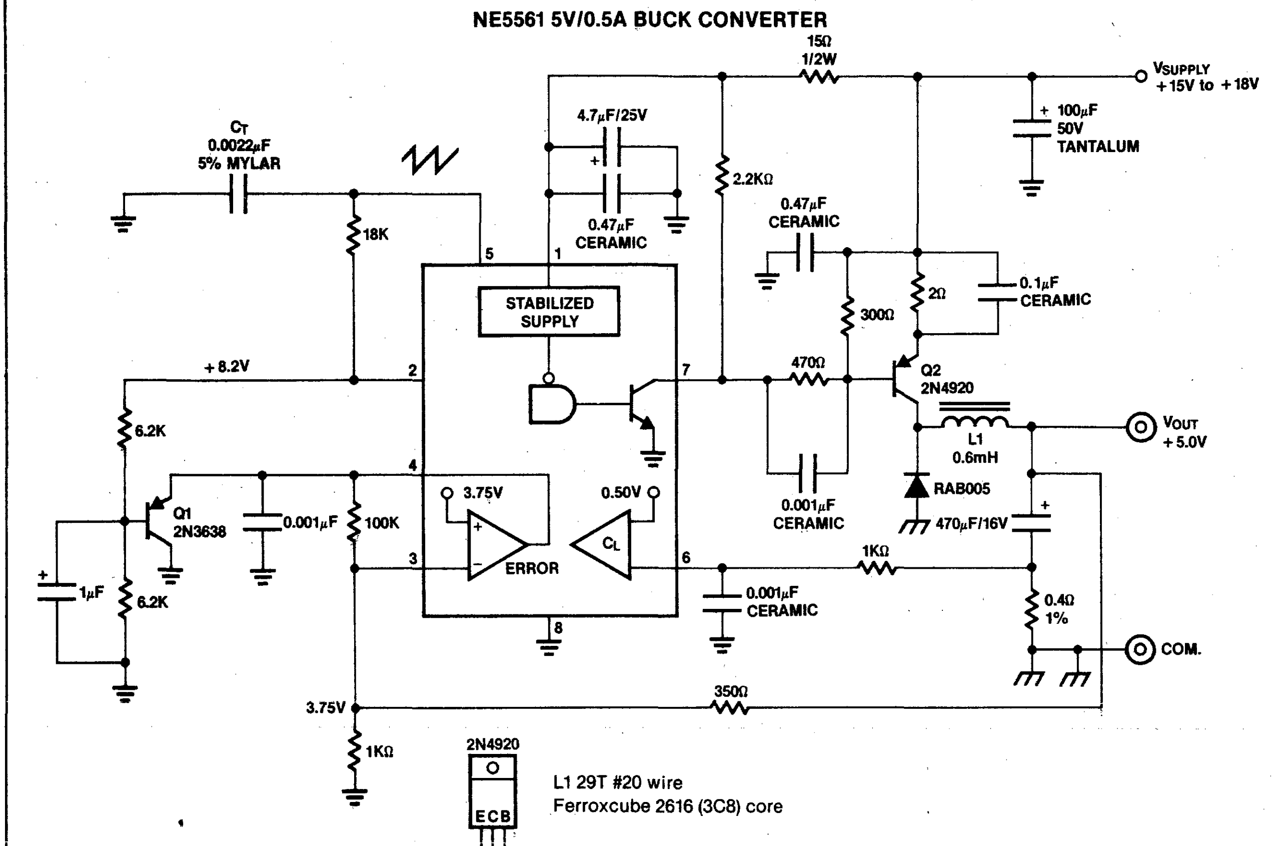


Figure 1

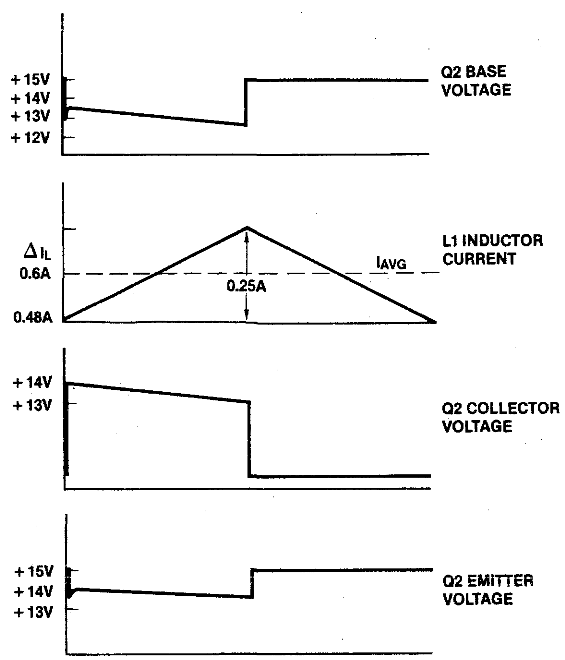


Figure 2

REGULATING PULSE WIDTH MODULATOR

SG3524

DESCRIPTION

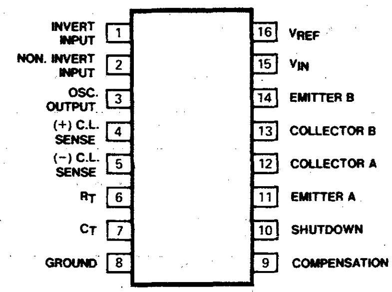
This monolithic integrated circuit contains all the control circuitry for a regulating power supply inverter or switching regulator. Included in a 16-pin dual-in-line package is the voltage reference, error-amplifier, oscillator, pulse width modulator, pulse steering flip-flop, dual alternating output switches and current limiting and shut-down circuitry. This device can be used for switching regulators of either polarity, transformer coupled DC to DC converters, transformerless voltage doublers and polarity converters, as well as other power control applications. The SG3524 is designed for commercial applications of 0°C to +70°C.

FEATURES

- **Complete PWM power control circuitry**
- **Single ended or push-pull outputs**
- **Line and load regulation of 0.2%**
- **1% maximum temperature variation**
- **Total supply current is less than 10mA**
- **Operation beyond 100kHz**

PIN CONFIGURATION

D,F,N PACKAGE

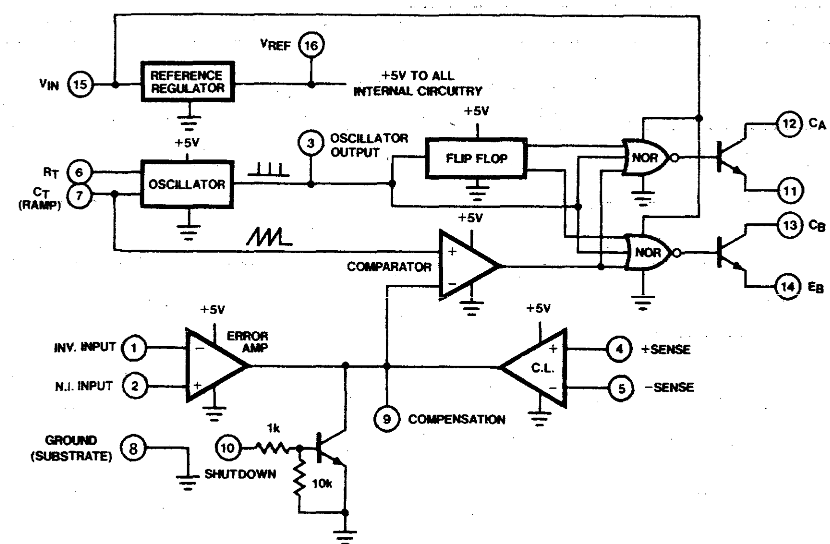


ORDER PART NUMBERS:
SG3524F, SG3524D,
SG3524N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Input voltage	40	V
Output current (each output)	100	mA
Reference output current	50	mA
Oscillator charging current	5	mA
Power dissipation		
Package limitation	1000	mW
Derate above 25°C	8	mW/°C
Operating temperature range	0 to +70	°C
Storage temperature range	−65 to +150	°C

BLOCK DIAGRAM



REGULATING PULSE WIDTH MODULATOR

SG3524

DC ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+70°C$, $V_{ON} = 20V$, and $f = 20kHz$ unless otherwise specified.)

PARAMETER	TEST CONDITIONS	SG3524			UNIT
		Min	Typ	Max	
Reference Section					
Output voltage		4.6	5.0	5.4	V
Line regulation	$V_{IN} = 8$ to 40V		10	30	mV
Load regulation	$I_L = 0$ to 20mA		20	50	mV
Ripple rejection	f = 120Hz, $T_A = 25°C$		66		dB
Short circuit current limit	$V_{REF} = 0$, $T_A = 25°C$		100		mA
Temperature stability	Over operating temperature range		0.3	1	%
Long term stability	$T_A = 25°C$		20		mV/kHr
Oscillator Section					
Maximum frequency	$C_T = .001$ mfd, $R_T = 2k\Omega$		300		kHz
Initial accuracy	R_T and C_T constant		5		%
Voltage stability	$V_{IN} = 8$ to 40V, $T_A = 25°C$			1	%
Temperature stability	Over operating temperature range			2	%
Output amplitude	Pin 3, $T_A = 25°C$		3.5		V_P
Output pulse width	$C_T = .01$ mfd, $T_A = 25°C$		0.5		μs
Error Amplifier Section					
Input offset voltage	$V_{CM} = 2.5V$		2	10	mV
Input bias current	$V_{CM} = 2.5V$		2	10	μA
Open loop voltage gain		68	80		dB
Common mode voltage	$T_A = 25°C$	1.8		3.4	V
Common mode rejection ratio	$T_A = 25°C$		70		dB
Small signal bandwidth	$A_V = 0dB$, $T_A = 25°C$		3		MHz
Output voltage	$T_A = 25°C$	0.5		3.8	V
Comparator Section					
Duty cycle	% each output "ON"	0		45	%
Input threshold	Zero duty cycle		1		V
Input threshold	Maximum duty cycle		3.5		V
Input bias current			1		μA
Current Limiting Section					
Sense voltage	Pin 9 = 2V with error amplifier set for maximum out, $T_A = 25°C$	180	200	220	mV
Sense voltage T.C.			0.2		mV/°C
Common mode voltage		−1		+1	V
Output Section (each output)					
Collector-emitter voltage (breakdown)		40			V
Collector-leakage current	$V_{CE} = 40V$		0.1	50	μA
Saturation voltage	$I_C = 50mA$		1	2	V
Emitter output voltage	$V_{IN} = 20V$	17	18		V
Rise time	$R_C = 2k\Omega$, $T_A = 25°C$		0.2		μs
Fall time	$R_C = 2k\Omega$, $T_A = 25°C$		0.1		μs
Total standby current (excluding oscillator charging current, error and current limit dividers, and with outputs open)	$V_{IN} = 40V$		8	10	mA

LINEAR

Signetics

FM RADIO CIRCUIT

TDA 7000

Preliminary

DESCRIPTION

The TDA7000 is a monolithic integrated circuit for mono FM portable radios where a minimum of peripheral components is important (small dimensions and low costs).

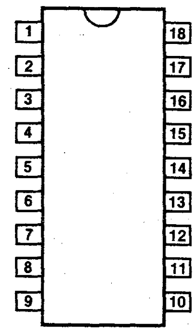
The IC has an FLL (Frequency-Locked-Loop) system with an intermediate frequency of 70 kHz. The I.F. selectivity is obtained by active RC filters. The only function which needs alignment is the resonant circuit for the oscillator, thus selecting the reception frequency. Spurious reception is avoided by means of a mute circuit, which also eliminates too-noisy input signals. Special precautions are taken to meet the radiation requirements.

FEATURES

- **R.F. input stage**
- **Mixer**
- **Local oscillator**
- **I.F. amplifier/limiter**
- **Phase demodulator**
- **Mute detector**
- **Mute switch**

PIN CONFIGURATION

N PACKAGE



TOP VIEW

ABSOLUTE MAXIMUM RATINGS

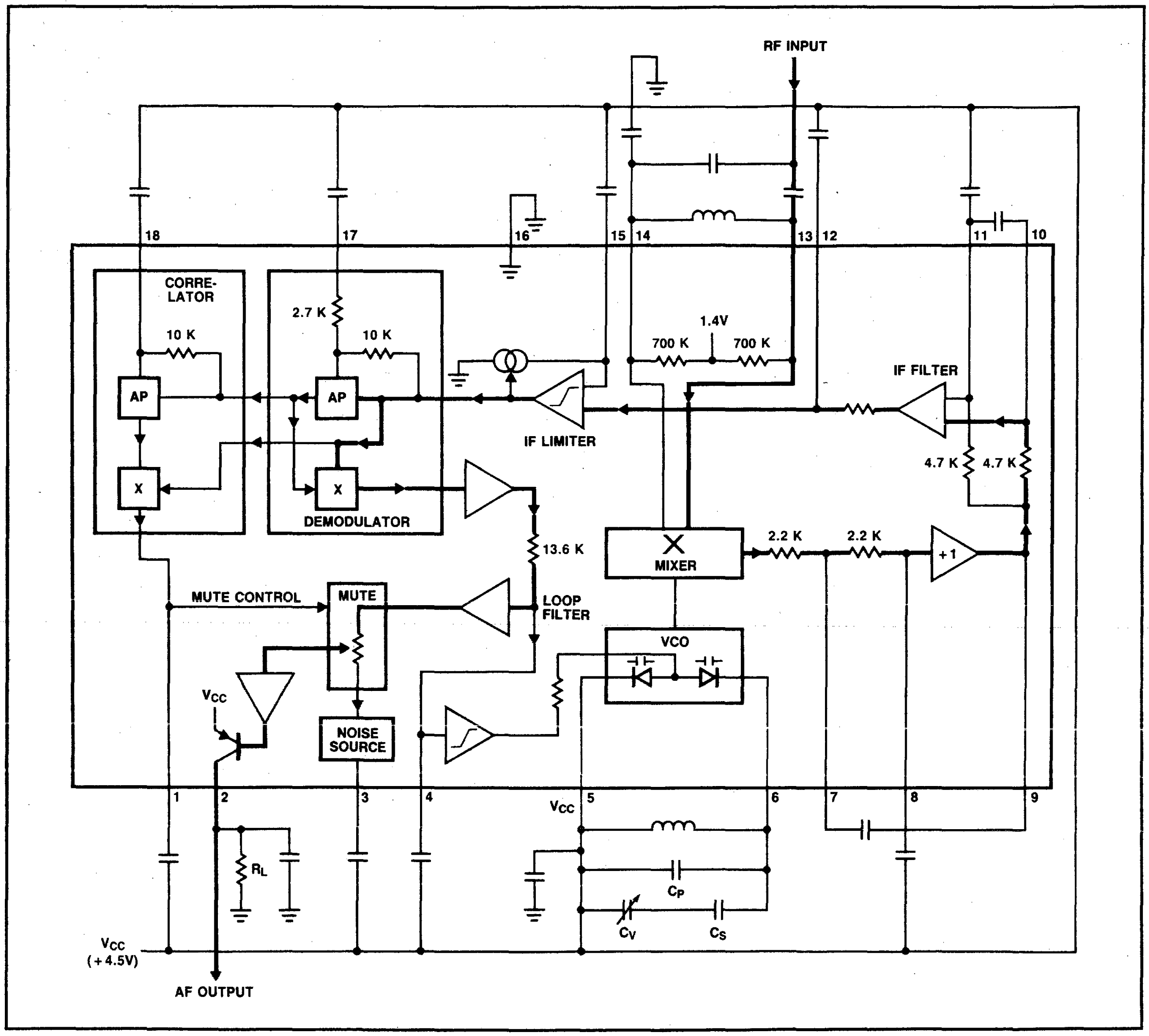
SYMBOL AND PARAMETER		RATING	UNIT
V_{CC}	Supply voltage (pin 5)	12	V
$V_{6\text{-}5}$	Oscillator voltage (pin 6)	V_{CC}−0.5 to V_{CC}+0.5	V
	Total power dissipation	See derating curve Figure 2	
T_{STG}	Storage temperature range	−55 to +150	°C
T_A	Operating ambient temperature range	0 to +60	°C

FUNCTIONAL PIN DESCRIPTION

PIN NO.	NAME AND FUNCTION
1	Muting capacitor
2	Audio frequency output
3	Noise source
4	Loud filter capacitor
5	Supply voltage
6	VCO
7	1st integrator capacitor (to pin 9)
8	2nd integrator capacitor
9	1st integrator capacitor (to pin 7)
10	IF filter capacitor
11	IF filter capacitor
12	IF limiter capacitor
13	RF input
14	Mixer
15	Current source capacitor
16	Ground
17	Demodulator capacitor
18	Correlator capacitor

Preliminary

BLOCK DIAGRAM



FM RADIO CIRCUIT

TDA 7000

Preliminary

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5V; T_A = 25°C: measured in Figure 3; unless otherwise specified

SYMBOL AND PARAMETER		TEST CONDITION	TDA7000			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage	(Pin 5)	2.7	4.5	10	V
I_{CC}	Supply current	V_{CC} = 4.5V		8		mA
I_6	Oscillator current	(Pin 6)		280		μA
$V_{14\text{-}16}$	Voltage	(Pin 14)		1.35		V
I_2	Output current	(Pin 2)		60		μA
$V_{2\text{-}16}$	Output voltage	(Pin 2) R_L = 22 kΩ		1.3		V

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5 V; T_A = 25°C; measured in Figure 3 (mute switch open, enabled); f_{rf} = 96 MHz (tuned to max. signal at 5 μV e.m.f.) modulated with Δf = ±22.5 kHz; f_m = 1 kHz; EMF = 0.2 mV (e.m.f. voltage at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified.

SYMBOL AND PARAMETER		TEST CONDITION	TDA7000			UNIT
			Min	Typ	Max	
EMF	Sensitivity (see Figure 2) (e.m.f. voltage)	−3 dB limiting; muting disabled		1.5		μV
		−3 dB muting		6		
		S/N = 26 dB		5.5		
EMF	Signal handling (e.m.f. voltage)	THD < 10%; Δf = ± 75 kHz		200		mV
S/N	Signal-to-noise ratio			60		dB
THD	Total harmonic distortion	Δf = ±22.5 kHz		0.7		%
		Δf = ±75 kHz		2.3		
AMS	AM suppression of output voltage	(ratio of the AM output signal referred to the FM output signal) FM signal: f_m = 1 kHz; Δf = ±75 kHz AM signal: f_m = 1 kHz; m = 80%		50		dB
RR	Ripple rejection	(ΔV_{CC} = 100 mV; f = 1 kHz)		10		dB
$V_{6\text{-}5(rms)}$	Oscillator voltage (r.m.s. value)	(Pin 6)		250		mV
Δf_{osc}	Variation of oscillator frequency	Supply voltage (ΔV_{CC} = 1V)		60		kHz/V
S_{+300}	Selectivity		45		dB	
S_{-300}			35		dB	
Δf_{rf}	A.F.C. range			±300		kHz
B	Audio bandwidth	ΔV_O = 3 dB measured with pre-emphasis (t = 50 μs)		10		kHz
$V_{O(rms)}$	A.F. output voltage (r.m.s. value)	R_L = 22 kΩ		75		mV
R_L	Load resistance	V_{CC} = 4.5V			22	kΩ
		V_{CC} = 9.0V			47	

NOTES:

1. The muting system can be disabled by feeding a current of about 20 μA into pin 1.
2. The interstation noise level can be decreased by choosing a low-value capacitor at pin 3. Silent tuning can be achieved by omitting this capacitor.

FM RADIO CIRCUIT

TDA7010T

Preliminary

DESCRIPTION

The TDA7010T is a monolithic integrated circuit for mono FM portable radios, where a minimum of peripheral components is important (small dimensions and low costs).

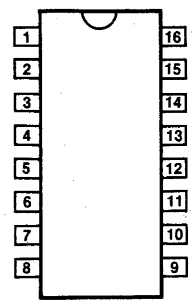
The IC has an FLL (Frequency-Locked-Loop) system with an intermediate frequency of 70 kHz. The I.F. selectivity is obtained by active RC filters. The only function which needs alignment is the resonant circuit for the oscillator, thus selecting the reception frequency. Spurious reception is avoided by means of a mute circuit, which also eliminates too noisy input signals. Special precautions are taken to meet the radiation requirements.

FEATURES

- **R.F. input stage**
- **Mixer**
- **Local oscillator**
- **I.F. amplifier/limiter**
- **Phase demodulator**
- **Mute detector**
- **Mute switch**

PIN CONFIGURATION

D PACKAGE



TOP VIEW

ABSOLUTE MAXIMUM RATINGS

SYMBOL AND PARAMETER		RATING	UNIT
V_{CC}	Supply voltage (pin 4)	12	V
$V_{6\text{-}5}$	Oscillator voltage (pin 5)	$V_{CC}-0.5$ to $V_{CC}+0.5$	V
	Total power dissipation	See derating curve Figure 2	
T_{STG}	Storage temperature range	−55 to +150	°C
T_A	Operating ambient temperature range	0 to +60	°C

FUNCTIONAL PIN DESCRIPTION

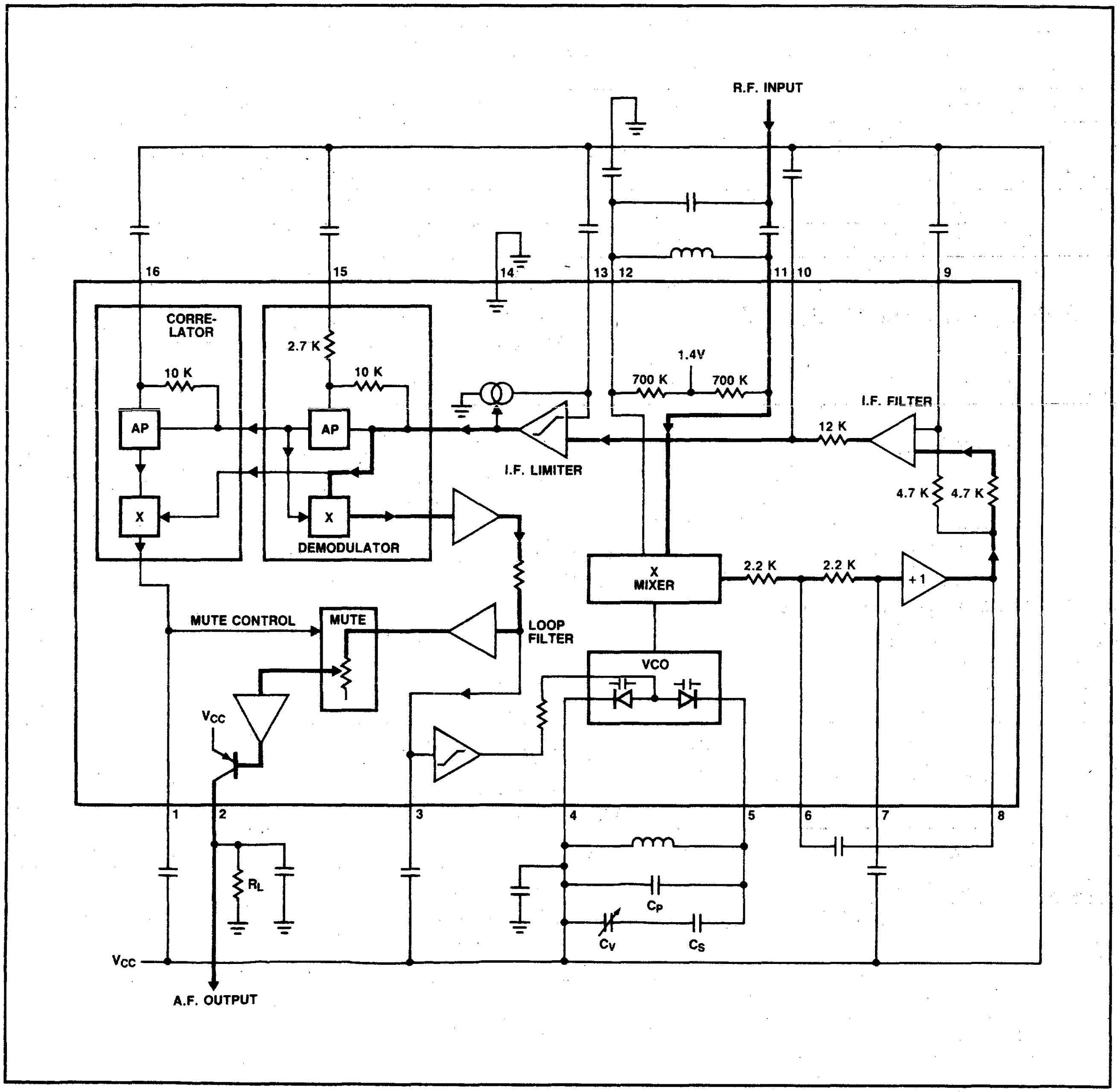
PIN NO.	NAME AND FUNCTION
1	Muting capacitor
2	Audio frequency output
3	Loop filter capacitor
4	Supply voltage
5	VCO
6	1st integrator capacitor (to pin 8)
7	2nd integrator capacitor
8	1st integrator capacitor (to pin 6)
9	IF filter capacitor
10	IF limiter capacitor
11	RF input
12	Mixer
13	Current source capacitor
14	Ground
15	Demodulator capacitor
16	Correlator capacitor

FM RADIO CIRCUIT

TDA7010T

Preliminary

BLOCK DIAGRAM



FM RADIO CIRCUIT

TDA7010T

Preliminary

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5V; T_A = 25°C: measured in Figure 3; unless otherwise specified.

SYMBOL AND PARAMETER		TEST CONDITION	TDA3810			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage	(Pin 4)	2.7	4.5	10	V
I_{CC}	Supply current	V_{CC} = 4.5V		8		mA
I_5	Oscillator Current	(Pin 5)		280		μA
V_{12-14}	Voltage	(Pin 12)		1.35		V
I_2	Output current	(Pin 2)		60		μA
V_{2-14}	Output voltage	(Pin 2) R_L = 22 kΩ		1.3		V

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5 V; T_A =25°C; measured in Figure 3 (mute switch open, enabled); f_{rf} = 96 MHz (tuned to max. signal at 5 μV e.m.f.) modulated with Δf = ±22.5 kHz; f_m = 1 kHz; EMF = 0.2 mV (e.m.f. voltage at a source impedance of 75 Ω); r.m.s. noise voltage measured unweighted (f = 300 Hz to 20 kHz); unless otherwise specified.

SYMBOL AND PARAMETER		TEST CONDITION	TDA7010T			UNIT
			Min	Typ	Max	
EMF	Sensitivity (see Figure 2) (e.m.f. voltage)	−3 dB limiting; muting disabled		1.5		μV
		−3 dB muting		6		
		S/N = 26 dB		5.5		
EMF	Signal handling (e.m.f. voltage)	THD < 10%; Δf = ± 75 kHz		200		mV
S/N	Signal-to-noise ratio			60		dB
THD	Total harmonic distortion	Δf = ±22.5 kHz Δf = ±75 kHz		0.7 2.3		% %
AMS	AM suppression of output voltage	(ratio of the AM output signal referred to the FM output signal) FM signal: f_m = 1 kHz; Δf = ±75 kHz AM signal: f_m = 1 kHz; m = 80%		50		dB
RR	Ripple rejection	(ΔV_{CC} = 100 mV; f = 1 kHz)		10		dB
$V_{5-4(rms)}$	Oscillator voltage (r.m.s. value)	(Pin 5)		250		mV
Δf_{osc}	Variation of oscillator frequency	Supply voltage (ΔV_{CC} = 1V)		60		kHz/V
S_{+300}	Selectivity		43			dB
S_{-300}			28			
Δf_{rf}	A.F.C. range			±300		kHz
B	Audio bandwidth	ΔV_O = 3 dB measured with pre-emphasis (t = 50 μs)		10		kHz
$V_{O(rms)}$	A.F. output voltage (r.m.s. value)	R_L = 22 kΩ		75		mV
R_L	Load resistance	V_{CC} = 4.5V			22	kΩ
		V_{CC} = 9.0V			47	

SAMPLE AND HOLD AMPLIFIER

NE/SE5537

DESCRIPTION

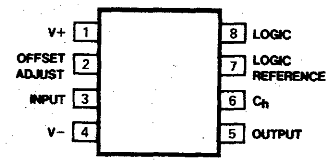
The NE5537 monolithic Sample and Hold amplifier combines the best features of ion implanted JFET's with bipolar devices to obtain high accuracy, fast acquisition time, and low droop rate. This device is pin compatible with the LF198, and features superior performance in droop rate and output drive capability. The circuit shown in Figure 1 contains two operational amplifiers which function as a unity gain amplifier in the Sample mode. The first amplifier has bipolar input transistors which gives the system a low offset voltage. The second amplifier has JFET input transistors to achieve low leakage current from the hold capacitor. A unique circuit design for leakage current cancellation using current mirrors gives the NE5537 a low droop rate at higher temperature. The output stage has the capability to drive a 2KΩ load. The logic input is compatible with TTL, PMOS or CMOS logic. The differential logic threshold is 1.4V with the Sample mode occurring when the logic input is high. It is available in 8-lead TO-5 and 8-pin plastic DIP packages.

FEATURES

- Operates from ±5V to ±18V supplies
- Hold leakage current 6pA @ T_j25°C
- Less than 10μs acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5mV typical hold step at C_h = 0.01μF
- Low input offset: 1MV (typical)
- 0.002% gain accuracy with R_L = 2kΩ
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth

PIN CONFIGURATION

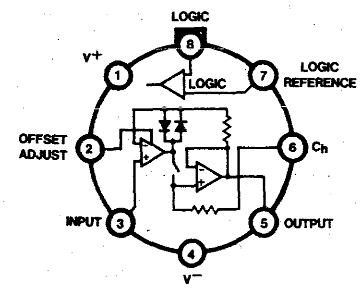
N PACKAGE



TOP VIEW

ORDER NUMBERS
NE/SE5537N

H PACKAGE
Metal Can Package



TOP VIEW

ORDER NUMBERS
NE/SE5537-H

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	±18	V
Power dissipation (package limitation)[1]	500	mW
Operating ambient temperature range		
SE5537	−55 to +125	°C
NE5537	0 to +70	°C
Storage temperature range	−65 to +150	°C
Input voltage	Equal to supply voltage	
Logic to logic reference differential voltage[2]	+7, −30	V
Output short circuit duration	Indefinite	
Hold capacitor short circuit duration	10	sec
Lead temperature (soldering, 10sec)	300	°C

NOTES
1. The maximum junction temperature of the SE5537 is 150°C and for the NE5537 is 100°C. When operating at elevated ambient temperature, the TO-5 and plastic DIP packages must be derated based on a thermal resistance (θja) of 150°C/W.
2. Although the differential voltage may not exceed the limits given, the common mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

BLOCK DIAGRAM

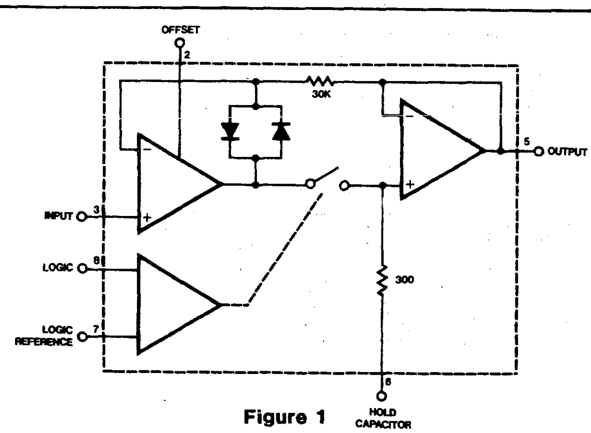


Figure 1

DESCRIPTION

The 558 Quad Timers are monolithic timing devices which can be used to produce four entirely independent timing functions. The 558 output sinks current. These highly stable, general purpose controllers can be used in a monostable mode to produce accurate time delays, from microseconds to hours. In the time delay mode of operation, the time is precisely controlled by one external resistor and one capacitor. A stable operation can be achieved by using two of the four timer sections.

The four timing sections in the 558 are edge triggered; therefore, when connected in tandem for sequential timing applications, no coupling capacitors are required. Output current capability of 100mA is provided in both devices.

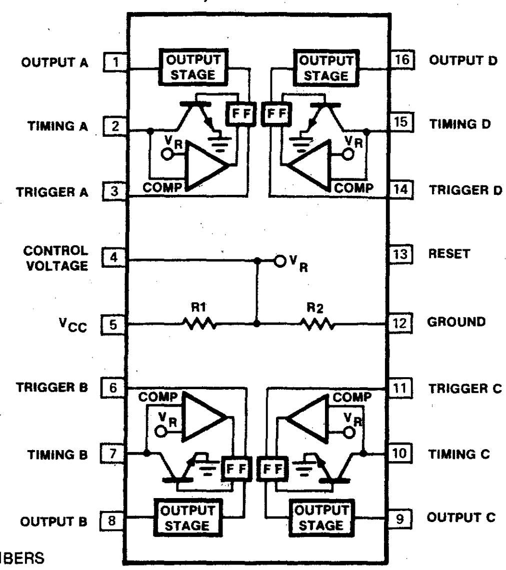
FEATURES

- **100mA output current per section**
- **Edge triggered (no coupling capacitor)**
- **Output independent of trigger conditions**
- **Wide supply voltage range 4.5V to 18V**
- **Timer intervals from microseconds to hours**
- **Time period equals RC**
- **Military qualifications pending**

APPLICATIONS

- **Sequential timing**
- **Time delay generation**
- **Precision timing**
- **Industrial controls**
- **Quad one-shot**

PIN CONFIGURATION



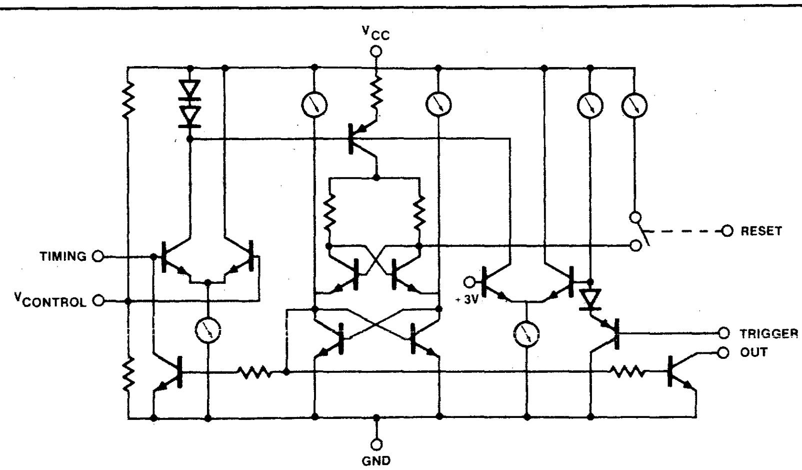
ORDER NUMBERS
NE/SA/SE558F NE/SA/SE558N

TOP VIEW

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
NE/SA558	+16	V
SE558	+18	V
Power dissipation	1.25	W
Operating temperature range		
NE558	0 to +70	°C
SA558	-40 to +85	°C
SE558	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	+300	°C

558 EQUIVALENT CIRCUIT



QUAD TIMER

NE/SA/SE558

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, V_{CC} = +5V to +15V unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE558			NE/SA558			UNIT
		Min	Typ	Max	Min	Typ	Max	
Supply voltage		4.5		18	4.5		16	V
Supply current	V_{CC} = Reset = 15V		16	32		16	36	mA
Timing accuracy (T = RC)	R = 2kΩ to 100kΩ C = 1μF							
Initial accuracy			± 1.0	3		± 2	5	%
Drift with temperature			30	100		30	150	ppm/°C
Drift with supply voltage			0.1	0.9		0.1	0.9	%/V
Trigger voltage[1]	V_{CC} = 15V	0.8		2.4	0.8		2.4	V
Trigger current	Trigger = 0V		5	30		5	100	μA
Reset voltage[2]		0.8		2.4	0.8		2.4	V
Reset current	Reset		50	300		50	500	μA
Threshold voltage			0.63			0.63		xV_{CC}
Threshold leakage			15			15		nA
Output voltage[3]	I_L = 10mA		0.1	0.2		0.1	0.4	V
	I_L = 100mA		0.7	1.5		1.0	2.0	V
Output leakage			10	500		10	500	nA
Propagation delay			1.0			1.0		μs
Risetime of output	I_L = 100mA		100			100		ns
Falltime of output	I_L = 100mA		100			100		ns

NOTES

1. The trigger functions only on the falling edge of the trigger pulse only after previously being high. After reset the trigger must be brought high and then low to implement triggering.
2. For reset below 0.8 volts, outputs set low and trigger inhibited. For reset above 2.4 volts, trigger enabled.
3. The 558 output structure is open collector which requires a pull up resistor to V_{CC} to sink current. The output is normally low sinking current.

LINEAR

Signetics

VOICE SYNTHESIZER

MEA8000

Preliminary

DESCRIPTION

The MEA8000 is a 24-pin N MOS integrated circuit for generating good quality speech from digital code with a programmable bit rate. The circuit is primarily intended for applications in microprocessor controlled systems, where the speech code is stored separately in a Read-Only Memory. An efficient, easy-to-use speech editing and encoding system with EPROM programming capability, has been specially developed.

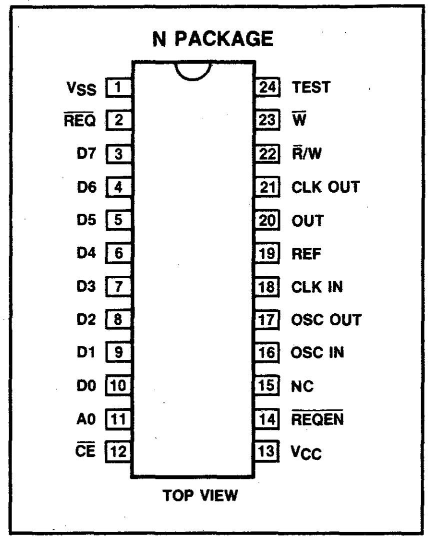
APPLICATIONS

- Telephony
- Automotive
- Computer response/prompt.
- Video games.
- General industrial.

FEATURES

- **Microprocessor interface cability including an 8-bit data bus, an enable and a read/write input control signals.**
- **32-bit data buffer holding speech frame codes.**
- **Digital filter of 8th order with 3 programmable formant frequencies, one fixed formant frequency, and 4 programmable formant bandwidths. 4 KHZ bandwidth.**
- **Programmable amplitudes.**
- **Programmable duration of each frame: 8, 16, 32, or 64 milliseconds.**
- **Low data rate: average 1000 bits/sec.**
- **Operates from standard EPROMs/ROMs.**
- **Minimal external audio filter requirement.**
- **Crystal controlled oscillator or external (TTL) clock.**
- **Single +5V power supply.**

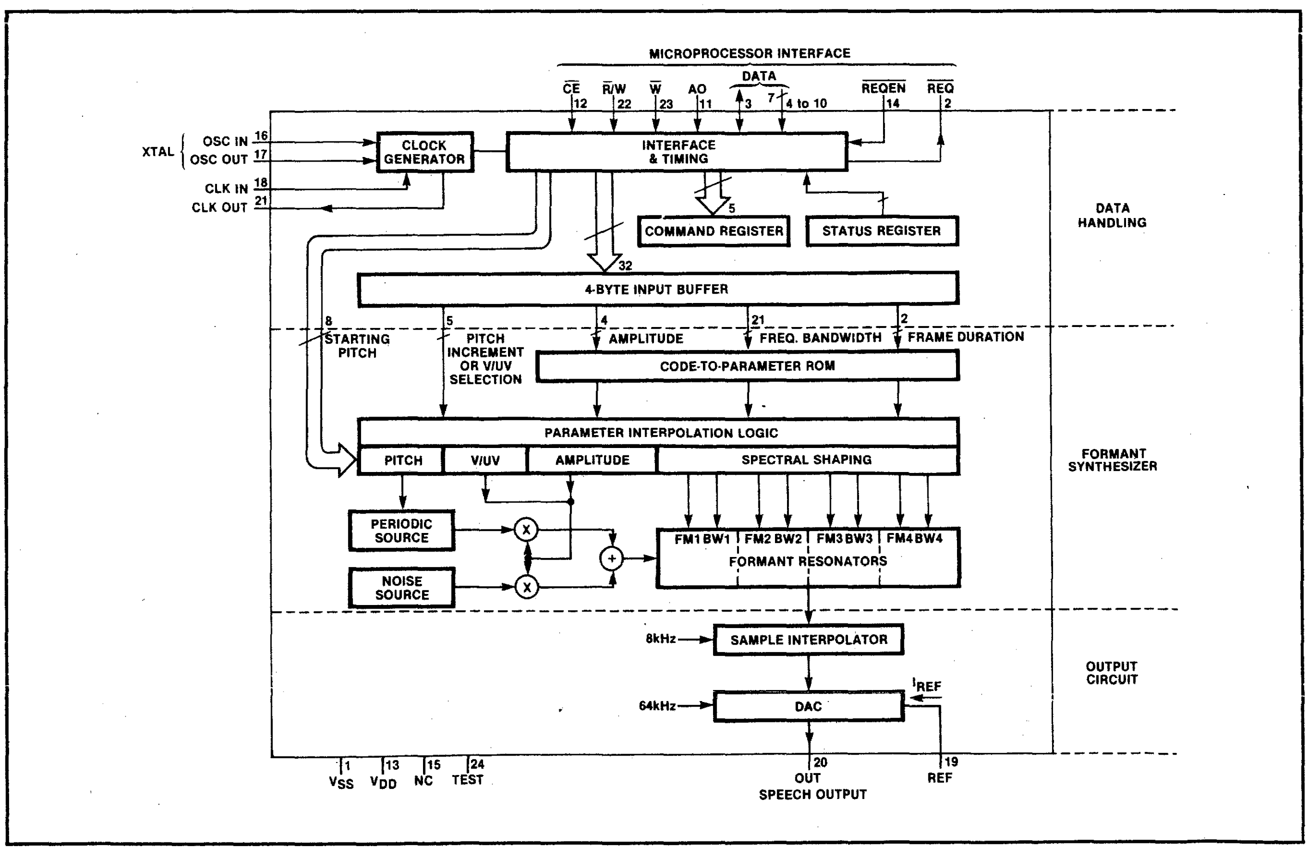
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATING

SYMBOL AND PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7	V
V_I	Voltage on any pin with respect to V_{SS}	−0.5 to +7	V
$V_{\overline{REQ}}$, V_{OUT}	Output voltage on pins 2 and 20	15	V
T_{STG}	Storage temperature range	−20 to +125	°C
T_A	Operating ambient temperature range	0 to +70	°C

BLOCK DIAGRAM

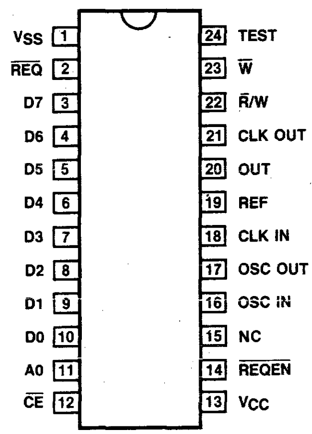


VOICE SYNTHESIZER

MEA8000

Preliminary

FUNCTIONAL PIN DESCRIPTION



PIN NO.	SYMBOL	NAME AND FUNCTION
		CONTROL
2	$\overline{REQ}$	**DATA REQUEST** output signal (open drain) which follows the inverse of the status REQ bit, but only if enabled by either the ROE bit in the command register or the external $\overline{REQEN}$ input pin.
3 to 10	D7 to D0	**Data bus** to which command or encoded speech parameters can be written. D7 is a bidirectional line through which the status bit can be read.
11	A0	**Data/control** input. Discriminates between speech code input buffer (A0 = '0') and command register (A0 = '1') during a 'write' operation.
12 22 23	$\overline{CE}$ $\overline{R}$/W $\overline{W}$	**Chip enable, Read/Write, Write** These control signals provides an easy interface to most microprocessors or microcomputers (see timing diagrams).
14	$\overline{REQEN}$	**Request enable** input. $\overline{REQEN}$ = '0' enables the status REQ bit to appear inverted on the $\overline{REQ}$ output, independent of the command register.
		TIMING
16 17	OSC IN OSC OUT	Connections for internal clock oscillator. Nominal crystal frequency is 3.84 MHz. OSC IN must be tied to ground if CLK IN is used.
18	CLK IN	**Clock input** for external clock, TTL compatible, 3.84 MHz. Must be tied to ground when not used.
21	CLK OUT	A buffered output of the internal clock cycle (= CLK IN divided by 3).
		OUTPUT
19	REF	**Reference Current** input pin for biasing the audio output level. This reference current can be derived from a resistor to the positive supply.
20	OUT	**Speech output.** This output is a 64 kHz pulse, modulated in both width and amplitude. It is configured as a current sink with a saturating voltage of about 3V.
		SUPPLY
1	V_{SS}	**Ground.**
13	V_{CC}	**Single supply voltage.** Nominally 5V, but battery operation is also possible.
15	NC	No connection.
24	TEST	Used for testing purposes. Changes other pin functions. Must be tied to ground for user operation.

Preliminary

DC ELECTRICAL CHARACTERISTICS T_A = 25°C: V_{CC} = 5V, unless otherwise stated. All voltages referenced to V_{SS}

SYMBOL AND PARAMETER		TEST CONDITION	MEA8000 Min	MEA8000 Typ	MEA8000 Max	UNIT
V_{CC}	Supply voltage (note 1)		4.5	5.0	5.5	V
I_{CC}	Supply current	(No audio load)		30	50	mA
	D0 to D7, A0, CE, W R/W REQEN, CLK IN:					
V_{IH}	Input HIGH voltage		2.0		V_{CC}	V
V_{IL}	Input LOW voltage		−0.5		0.8	V
I_{IR}	Input Leakage current (note 2)				10	μA
C_I	Input Capacitance				7	pF
	D7 (I/O), CLK OUT:					
V_{OH}	Output HIGH voltage	$-I_{OH}$ =−100 μA	2.4			V
V_{OL}	Output LOW voltage	I_{OL} = 1.6 mA			0.4	V
C_L	Output Load capacitance				50	pF
	REQ:					
V_{OH}	Output HIGH voltage	Open drain			13.2	V
V_{OL}	Output LOW voltage	I_{OL} = 1.6 mA			0.4	V
C_L	Output Load capacitance				50	pF
	Audio output					
I_{REF}	Reference current (note 8) - Pin 19				0.3	mA
I_{OUT}	Output current (peak) - Pin 20					
		I_{REF} = 0 mA		100		μA
		I_{REF} = 0.1 mA		1.7		mA
		I_{REF} = 0.3 mA		5		mA
V_{OUT}	V_{OUT} (pin 20) for linear operation (note 3)	I_{REF} = 0.1 mA	2.5		13.2	V
	Oscillator					
f_{XTAL}	Crystal frequency	Internal		3.84	4.00	MHz
f_{CLK}	Clock frequency	External		3.84	4.00	MHz

AC ELECTRICAL CHARACTERISTICS (note 4) (Figure 4 and 5)

SYMBOL AND PARAMETER		TEST CONDITION	MEA8000 Min	MEA8000 Typ	MEA8000 Max	UNIT
t_{WR}	Write enable pulse width.	Clock frequency = 3.84 MHz	200			ns
t_{AS}	Address set-up time.		30			ns
t_{AH}	Address hold time.		30			ns
t_{DS}	Data set-up time for write operation.		150			ns
t_{DH}	Data hold time for write operation.		30			ns
t_{RH}	Request hold time (note 5)				350	ns
t_{RN}	Request next (note 6)				3	μs
t_{RD}	Read enable time.		200			ns
t_{DD}	Data delay for read operation (note 7)				150	ns
t_{DF}	Data floating for read operation (note 7)				150	ns
t_{RV}	Request valid before a write operation.		0			ns
t_{ROE}	Request output enable response.				750	ns
t_{CS}	Control set-up time.				20	ns
t_{CH}	Control hold time.				20	ns

NOTES
1. The circuit will continue to operate from a supply of up to 6.5V, but without necessarily meeting the specification.
2. This is also valid for V_{CC} = 0V.
3. This permits connection of the output load to a supply higher than that supplying the synthesizer.
4. Timing reference level is 1.5V.
5. An external pull up resistor is required, as this is an open drain output. The time (t_{RH}) to reach 2.0V is specified at a load to 5V of 3.3 kΩ and 50 pF.
6. Between two data write operations of one speech frame.
7. Levels greater than 2.0V for a '1' or less than 0.8V for a '0' are reached with a load of one TTL input and 50 pF.
8. Typical voltage level at the REF pin is 2.5V.

VIDEO AMPLIFIER

NE/SE592

DESCRIPTION

The SE/NE592 is a monolithic, two stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers. Now available in an 8-pin version with fixed gain of 400 without external components and adjustable gain from 400 to 0 with one external resistor.

FEATURES

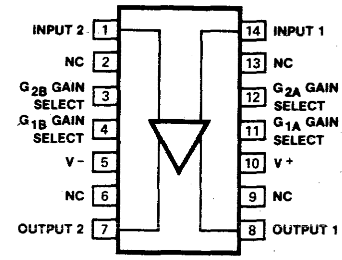
- **120MHz bandwidth**
- **Adjustable gains from 0 to 400**
- **Adjustable pass band**
- **No frequency compensation required**
- **Wave shaping with minimal external components**

APPLICATIONS

- **Floppy disk head amplifier**
- **Video amplifier**
- **Pulse amplifier in communications**
- **Magnetic memory**
- **Video recorder systems**

PIN CONFIGURATION

DH, FH, N14 PACKAGE

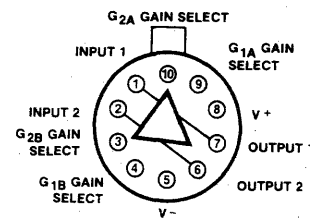


TOP VIEW

ORDER NUMBERS

NE592DH	NE592N14
NE592FH	SE592FH

H PACKAGE*



NOTE
Pin 5 connected to case.

ORDER NUMBERS

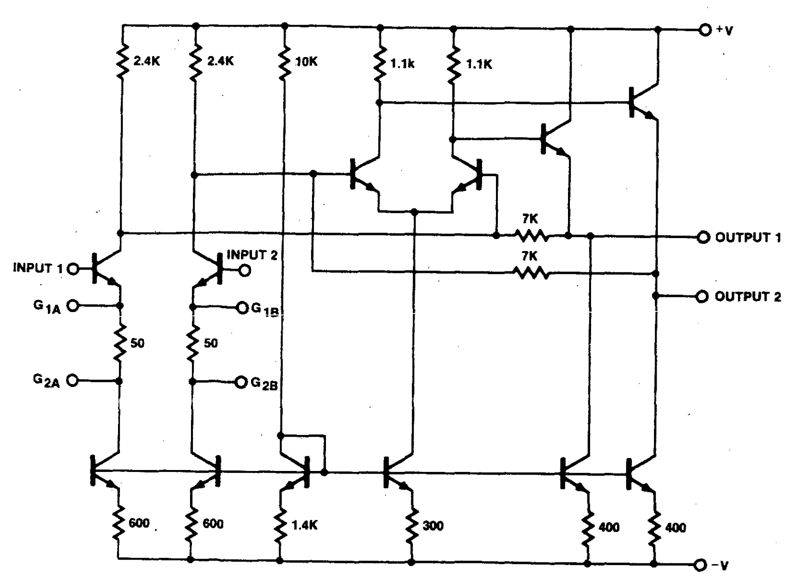
NE592H	SE592H

*Metal cans (H) not recommended for new designs.

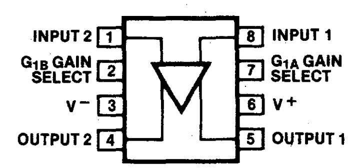
ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$ unless otherwise specified.

PARAMETER	RATING	UNIT
Supply voltage	±8	V
Differential input voltage	±5	V
Common mode		
Input voltage	±6	V
Output current	10	mA
Operating temperature range		
SE592	-55 to +125	°C
NE592	0 to +70	°C
Storage temperature range	-65 to +150	°C
Power dissipation	500	mW

EQUIVALENT CIRCUIT



DE, FE, N8 PACKAGE



TOP VIEW

ORDER NUMBERS

NE592DE	NE592N8
NE592FE	S592FE

DC ELECTRICAL CHARACTERISTICS $T_A = +25°C$, $V_{SS} = \pm 6V$, $V_{CM} = 0$ unless otherwise specified.

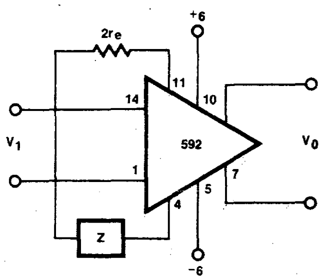
Recommended operating supply voltages $V_S = \pm 6.0V$.

PARAMETER	TEST CONDITIONS	NE592			SE592			UNITS
		Min	Typ	Max	Min	Typ	Max	
Differential voltage gain								
Gain 1[1]	$R_L = 2k\Omega$, $V_{OUT} = 3V$ p-p	250	400	600	300	400	500	V/V
Gain 2[2,4]		80	100	120	90	100	110	V/V
Bandwidth								
Gain 1[1]			40			40		MHz
Gain 2[2,4]			90			90		MHz
Rise time								
Gain 1[1]	$V_{OUT} = 1V$ p-p		10.5			10.5		ns
Gain 2[2,4]			4.5	12		4.5	10	ns
Propagation delay								
Gain 1[1]	$V_{OUT} = 1V$ p-p		7.5			7.5		ns
Gain 2[2,4]			6.0	10		6.0	10	ns
Input resistance								
Gain 1[1]			4.0			4.0		kΩ
Gain 2[2,4]		10	30		20	30		kΩ
Input capacitance[2]	Gain 2[4]		2.0			2.0		pF
Input offset current			0.4	5.0		0.4	3.0	μA
Input bias current			9.0	30		9.0	20	μA
Input noise voltage	BW 1kHz to 10MHz		12			12		μVrms
Input voltage range				±1.0			±1.0	V
Common mode rejection ratio								
Gain 2[4]	$V_{CM} \pm 1V$, $F < 100kHz$	60	86		60	86		dB
Gain 2[4]	$V_{CM} \pm 1V$, $F = 5MHz$		60			60		dB
Supply voltage rejection ratio								
Gain 2[4]	$\Delta V_S = \pm 0.5V$	50	70		50	70		dB
Output offset voltage								
Gain 1	$R_L = \infty$			1.5			1.5	V
Gain 2[4]	$R_L = \infty$			1.5			1.0	V
Gain 3[3]	$R_L = \infty$		0.35	0.75		0.35	0.75	V
Output common mode voltage	$R_L = \infty$	2.4	2.9	3.4	2.4	2.9	3.4	V
Output voltage swing differential	$R_L = 2K$	3.0	4.0		3.0	4.0		V
Output resistance			20			20		Ω
Power supply current	$R_L = \infty$		18	24		18	24	mA
THE FOLLOWING SPECS APPLY OVER TEMPERATURE		**0°C ≤ T_A ≤ 70°C**			**−55°C ≤ T_A ≤ 125°C**			
Differential voltage gain								
Gain 1[1]	$R_L = 2k\Omega$, $V_{OUT} = 3V$ p-p	250		600	200		600	V/V
Gain 2[2,4]		80		120	80		120	V/V
Input resistance								
Gain 2[2,4]		8.0			8.0			kΩ
Input offset current				6.0			5.0	μA
Input bias current				40			40	μA
Input voltage range		±1.0			±1.0			V
Common mode rejection ratio								
Gain 2[4]	$V_{CM} \pm 1V$, $F < 100kHz$	50			50			dB
Supply voltage rejection ratio								
Gain 2[4]	$\Delta V_S = \pm 0.5V$	50			50			dB
Output offset voltage								
Gain 1	$R_L = \infty$			1.5			1.5	V
Gain 2[4]	$R_L = \infty$			1.5			1.2	V
Gain 3[3]	$R_L = \infty$			1.0			1.0	V
Output voltage swing differential	$R_L = 2K$	2.8			2.5			V
Power supply current	$R_L = \infty$			27			27	mA

NOTES:
1. Gain select pins G_{1A} and G_{1B} connected together.
2. Gain select pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 14-pin version only.

TYPICAL APPLICATIONS

FILTER NETWORKS



$$\frac{V_0\,(s)}{V_1\,(s)} \cong \frac{1.4 \times 10^4}{Z(s) + 2r_e}$$

$$\cong \frac{1.4 \times 10^4}{Z(s) + 32}$$

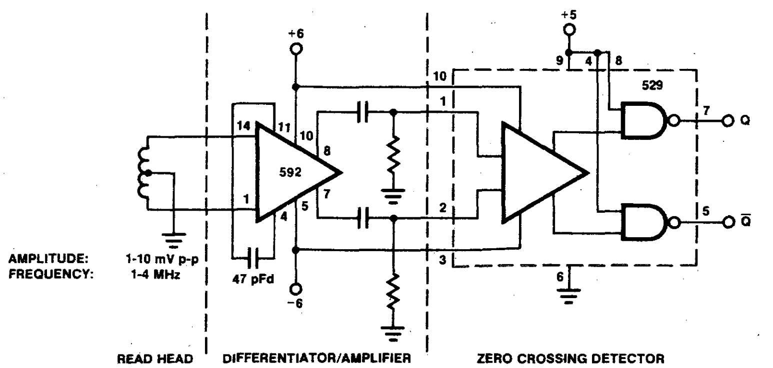
BASIC CONFIGURATION

Z NETWORK	FILTER TYPE	$\frac{V_0\,(s)}{V_1\,(s)}$ TRANSFER FUNCTION
R L (series)	LOW PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
R C (series)	HIGH PASS	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
R L C (series)	BAND PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/L\, s + 1/LC}\right]$
R in series with L ∥ C	BAND REJECT	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

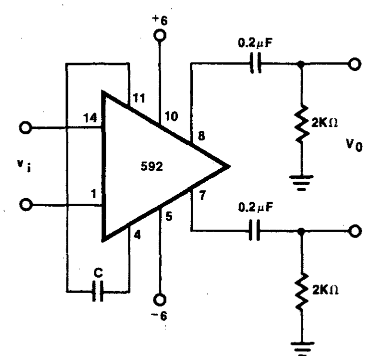
NOTE

In the networks above, the R value used is assumed to include $2r_e$, or approximately 32Ω.

DISC/TAPE PHASE MODULATED READBACK SYSTEMS



DIFFERENTIATION WITH HIGH COMMON MODE NOISE REJECTION



FOR FREQUENCY $F_1 << 1/2\,\pi\,(32)\,C$

$V_0 \cong 1.4 \times 10^4 C \frac{dV_i}{dT}$

ULTRA HIGH FREQUENCY OPERATIONAL AMPLIFIER

NE/SE5539

DESCRIPTION

The Signetics NE5539 is a very wide bandwidth, high slew rate, monolithic operational amplifier for use in video amplifiers, RF amplifiers, and extremely high slew rate amplifiers.

Emitter follower inputs provide a true differential high input impedance device. Proper external compensation will allow design operation over a wide range of closed loop gains, both inverting and non-inverting, to meet specific design requirements.

FEATURES

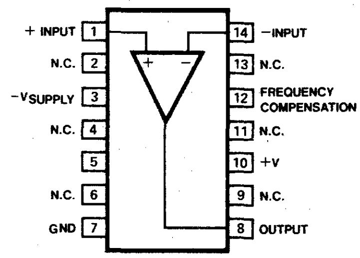
- **Gain bandwidth product: 1.2GHz at 17dB**
- **Slew rate: 600V/μsec**
- **Full power response: 48MHz**
- **A_{VOL}: 52dB typical**

APPLICATIONS

- **Fast pulse amplifiers**
- **RF oscillators**
- **Fast sample and hold**
- **High gain video amplifiers (BW > 20MHz)**

PIN CONFIGURATION

D,F,N PACKAGE



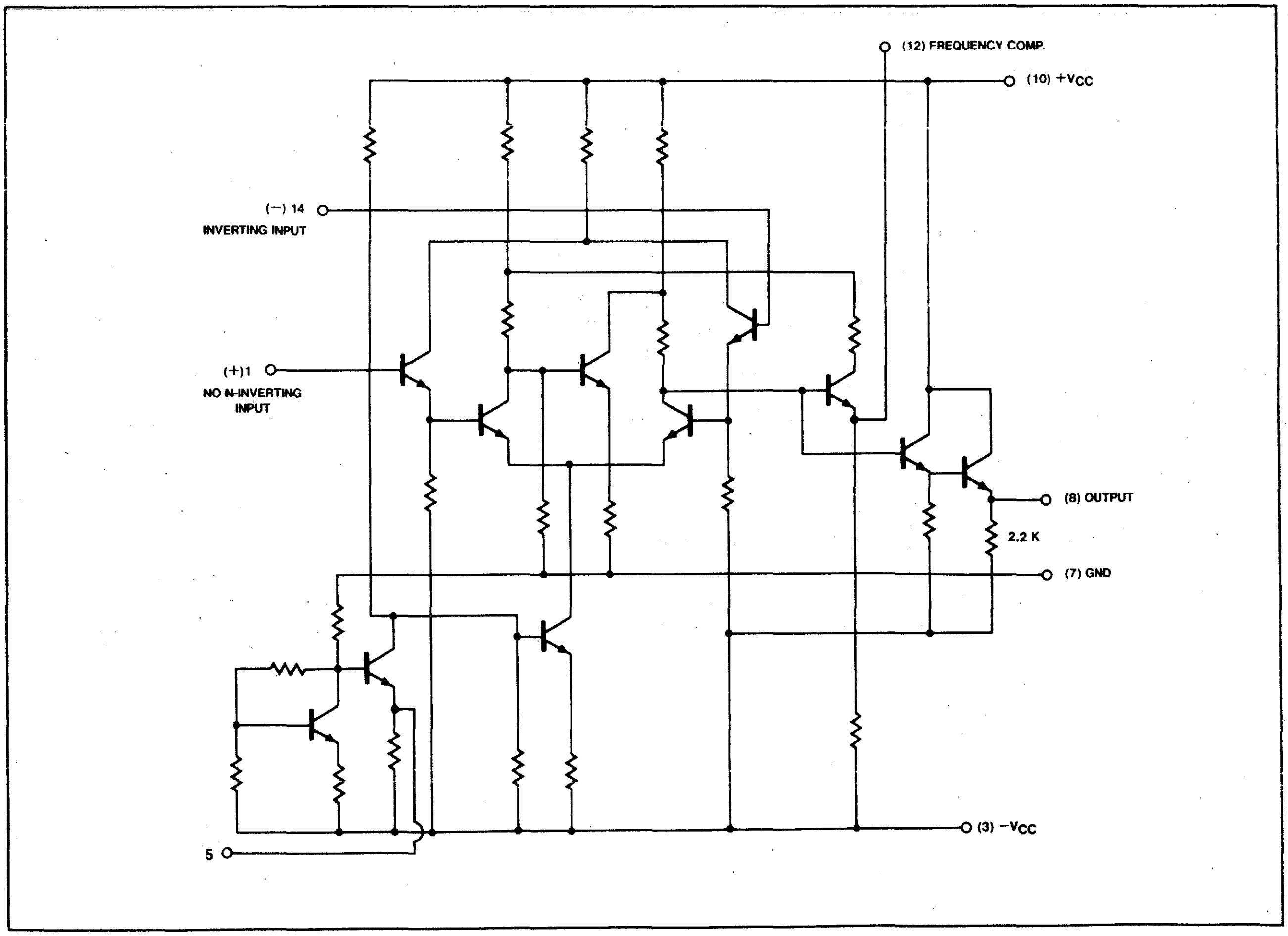
TOP VIEW

ORDER NUMBERS
NE/SE5539F NE/SE5539N
NE5539D

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	±12	V
P_D	Internal power dissipation	550	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_J	Max junction temperature	150	°C
T_A	Operating temperature range		
	NE	0 to 70	°C
	SE	−55 to +125	°C
	Lead temperature	300	°C

EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $T_A = 25°C$ unless otherwise specified

PARAMETER		TEST CONDITIONS		SE5539 Min	SE5539 Typ	SE5539 Max	NE5539 Min	NE5539 Typ	NE5539 Max	UNIT
V_{OS}	Input offset voltage	$V_O = 0V$, $R_S = 100\Omega$	Over temp		2	5				mV
			$T_A = 25°C$		2	3		2.5	5	
$\Delta V_{OS}/\Delta T$					5			5		μV/°C
I_{OS}	Input offset current		Over temp		.1	3				μA
			$T_A = 25°C$		.1	1			2	
$\Delta I_{OS}/\Delta T$					.5			.5		nA/°C
I_B	Input bias current		Over temp		6	25				μA
			$T_A = 25°C$		5	13		5	20	
$\Delta I_B/\Delta T$					10			10		nA/°C
CMRR	Common mode rejection ratio	$F = 1kHz$, $R_S = 100\Omega$, $V_{CM} \pm 1.7V$		70	80		70	80		dB
			Over temp	70	80					dB
R_{IN}	Input impedance				100			100		kΩ
R_{OUT}	Output impedance				10			10		Ω
V_{OUT}	Output voltage swing	$R_L = 150\Omega$ to GND and 470Ω to $-V_{CC}$	+Swing				+2.3	+2.7		V
			−Swing				−1.7	−2.2		
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$ to GND, Over temp	+Swing	+2.3	+3.0					V
			−Swing	−1.5	−2.1					
		$R_L = 2k\Omega$ to GND, $T_A = 25°C$	+Swing	+2.5	+3.1					V
			−Swing	−2.0	−2.7					
$I_{CC}+$	Positive supply current	$V_O = 0$, $R_1 = \infty$	Over temp		14	18				mA
			$T_A = 25°C$		14	17		14	18	
$I_{CC}-$	Negative supply current	$V_O = 0$, $R_1 = \infty$	Over temp		11	15				mA
			$T_A = 25°C$		11	14		11	15	
PSRR	Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$	Over temp		300	1000				μV/V
			$T_A = 25°C$					200	1000	
A_{VOL}	Large signal voltage gain	$V_O = +2.3V, -1.7V$ $R_L = 150\Omega$ to GND, 470Ω to $-V_{CC}$					47	52	57	dB
A_{VOL}	Large signal voltage gain	$V_O = +2.3V, -1.7V$ $R_L = 2K$ to GND								dB
			$T_A = 25°C$				47	52	57	
A_{VOL}	Large signal voltage gain	$V_O = +2.5V, -2.0V$ $R_L = 2k\Omega$ to GND	Over temp	46		60				dB
			$T_A = 25°C$	48	53	58				

NOTE

1. Differential input voltage should not exceed 0.25 volts to prevent excessive input bias current and common mode voltage 2.5 volts. These voltage limits may be exceeded if current limit is 10mA.

ULTRA HIGH FREQUENCY OPERATIONAL AMPLIFIER — NE/SE5539

AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $R_L = 150\Omega$ to GND & 470Ω to $-V_{CC}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE5539 Min	SE5539 Typ	SE5539 Max	NE5539 Min	NE5539 Typ	NE5539 Max	UNIT
Gain bandwidth product	$A_{CL} = 7$ $V_O = 0.1$ Vp-p		1200			1200		MHz
Small signal bandwidth	$A_{CL} = 2$ $R_L = 150\Omega$[1]		110			110		MHz
Settling time	$A_{CL} = 2$ $R_L = 150\Omega$[1]		15			15		nSec
Slew rate	$A_{CL} = 2$ $R_L = 150\Omega$[1]		600			600		V/μSec
Propagation delay	$A_{CL} = 2$ $R_L = 150\Omega$[1]		7			7		nSec
Full power response	$A_{CL} = 2$ $R_L = 150\Omega$[1]		48			48		MHz
Full power response	$A_V = 7$, $R_L = 150\Omega$		20			20		MHz
Wide band noise (RMS)	$B_W = 5MHz$, $R_S = 50\Omega$		4			4		nV/$\sqrt{Hz}$

NOTE 1: External compensation.

DC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 6V$, $T_A = 25°C$ unless otherwise specified

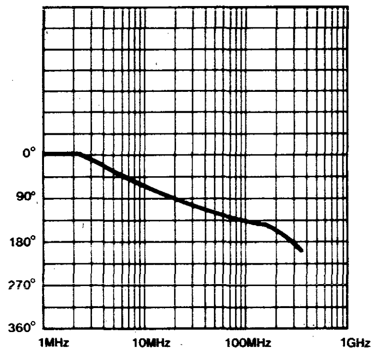
PARAMETERS		TEST CONDITIONS			SE5539 Min	SE5539 Typ	SE5539 Max	UNIT
V_{OS}	Input offset voltage			Over temp		2	5	mV
				$T_A = 25°C$		2	3	
I_{OS}	Input offset current			Over temp		.1	3	μA
				$T_A = 25°C$		.1	1	
I_B	Input bias current			Over temp		5	20	μA
				$T_A = 25°C$		4	10	
CMRR	Common mode rejection ratio	$V_{CM} = \pm 1.3V$, $R_S = 100\Omega$			70	85		dB
$I_{CC}+$	Positive supply current			Over temp		11	14	mA
				$T_A = 25°C$		11	13	
$I_{CC}-$	Negative supply current			Over temp		8	11	mA
				$T_A = 25°C$		8	10	
PSRR	Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$		Over temp		300	1000	μV/V
				$T_A = 25°C$				
V_{OUT}	Output voltage swing	$R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$	Over temp	+ Swing	+1.4	+2.0		V
				− Swing	−1.1	−1.7		
			$T_A = 25°C$	+ Swing	+1.5	+2.0		
				− Swing	−1.4	−1.8		

AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 6V$, $R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$ unless otherwise specified

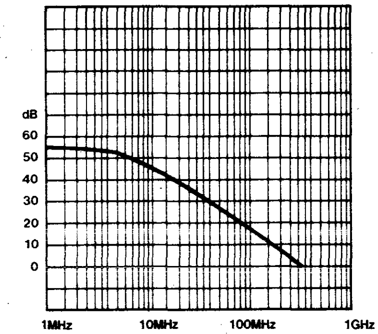
PARAMETER	TEST CONDITIONS	SE5539 Min	SE5539 Typ	SE5539 Max	UNIT
Gain bandwidth product	$A_{CL} = 7$		700		MHz
Small signal bandwidth	$A_{CL} = 2$[1]		120		MHz
Settling time	$A_{CL} = 2$[1]		23		ns
Slew rate	$A_{CL} = 2$[1]		330		V/μs
Propagation delay	$A_{CL} = 2$[1]		4.5		ns
Full power response	$A_{CL} = 2$[1]		20		MHz

NOTE 1: External compensation.

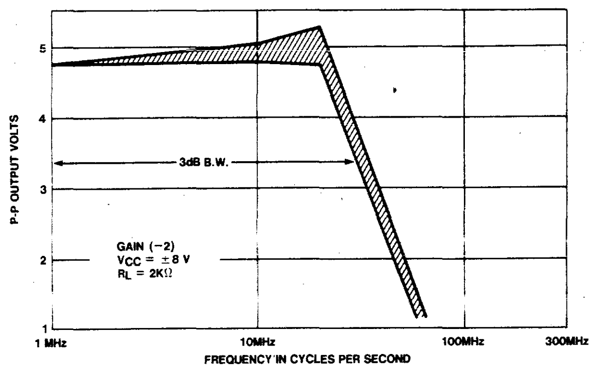
NE5539 OPEN LOOP PHASE



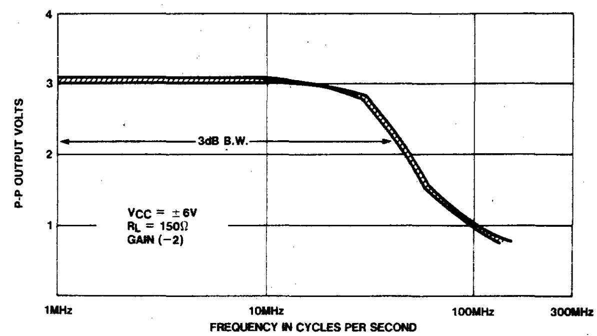
NE5539 OPEN LOOP GAIN



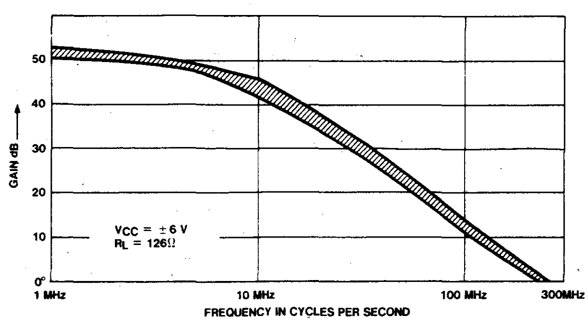
POWER BANDWIDTH (SE)



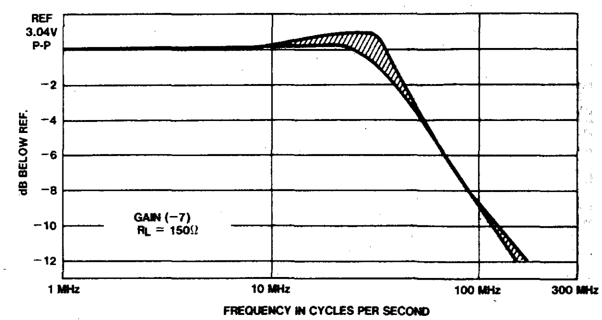
POWER BANDWIDTH (NE)



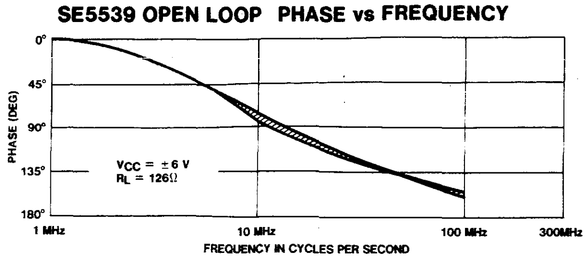
SE5539 OPEN LOOP GAIN vs FREQUENCY



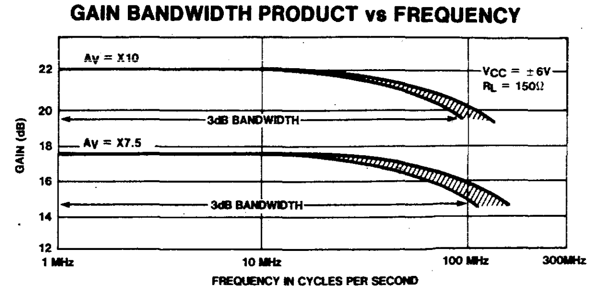
POWER BANDWIDTH



SE5539 OPEN LOOP PHASE vs FREQUENCY



GAIN BANDWIDTH PRODUCT vs FREQUENCY



NOTE

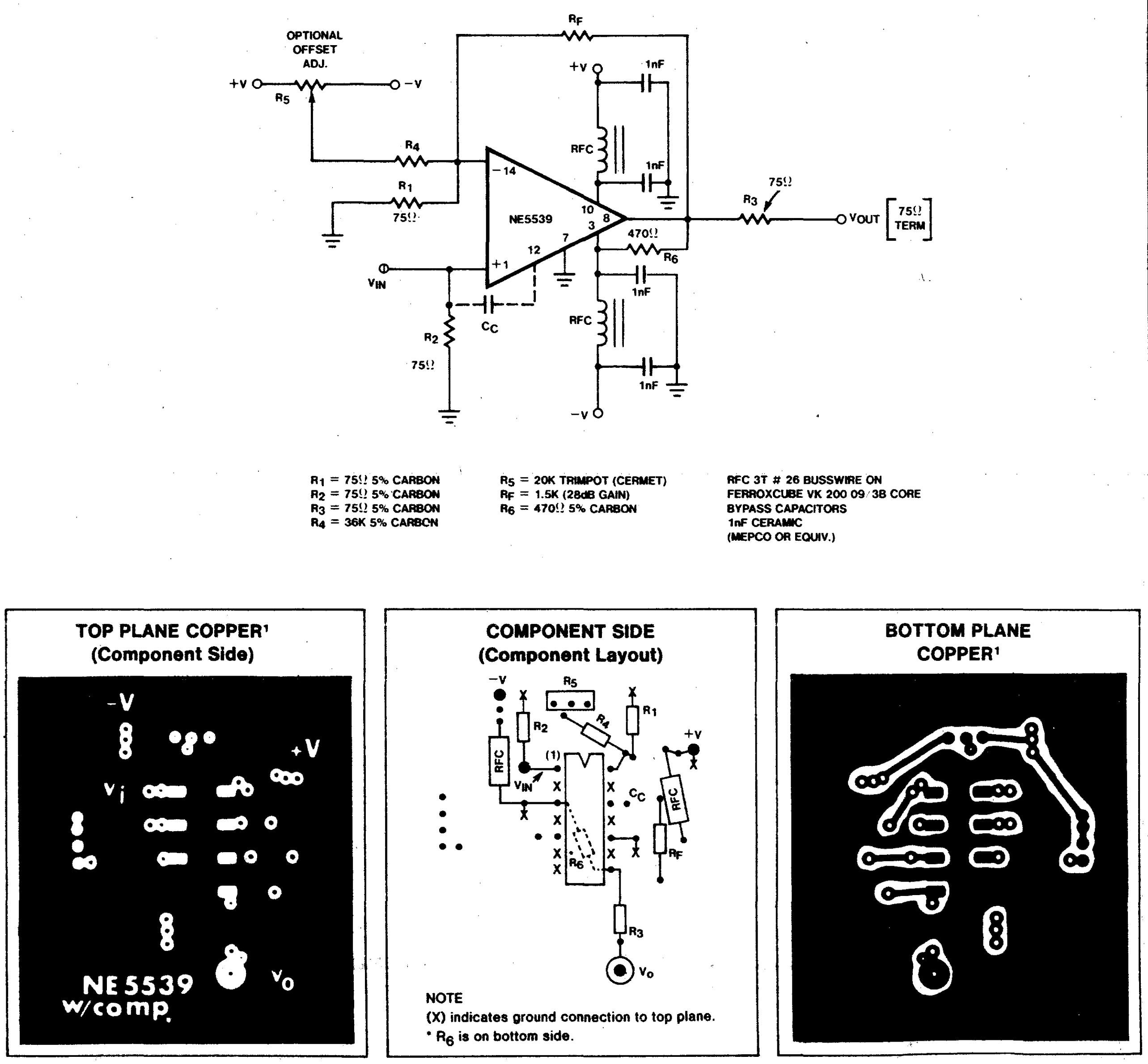
Indicates typical distribution $-55°C \leq T_A \leq 125°C$

LINEAR

Signetics

CIRCUIT LAYOUT CONSIDERATIONS

As may be expected for an ultra-high frequency, wide gain bandwidth amplifier, the physical circuit layout is extremely critical. Breadboarding is not recommended. A double-sided copper clad printed circuit board will result in more favorable system operation. An example utilizing a 28dB non-inverting amp is shown in Figure 1.



NOTE 1: Bond edges of top and bottom ground plane copper.

Figure 1. 28dB Non-Inverting Amp Sample P.C. Layout

VIDEO AMPLIFIER

NE5592

Preliminary

DESCRIPTION

The NE5592 is a dual monolithic, two stage, differential output, wideband video amplifier. It offers fixed gain of 400 without external components or adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers.

FEATURES

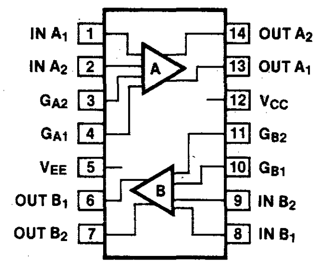
- **120MHz bandwidth**
- **Adjustable gains from 0 to 400**
- **Adjustable pass band**
- **No frequency compensation required**
- **Wave shaping with minimal external components**

APPLICATIONS

- **Floppy disk head amplifier**
- **Video amplifier**
- **Pulse amplifier in communications**
- **Magnetic memory**
- **Video recorder systems**

PIN CONFIGURATION

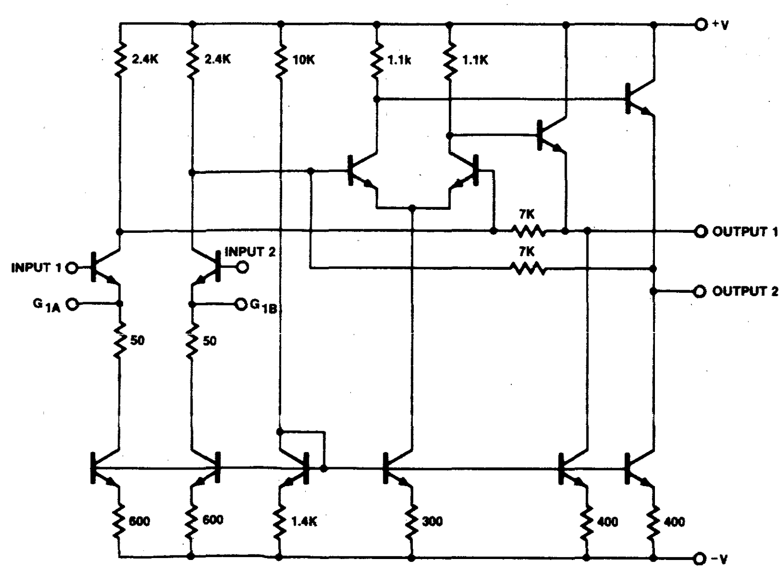
D, N PACKAGES



ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$ unless otherwise specified.

PARAMETER	RATING	UNIT
Supply voltage	±8	V
Differential input voltage	±5	V
Common mode		
Input voltage	±6	V
Output current	10	mA
Operating temperature range		
NE5592	0 to +70	°C
Storage temperature range	-65 to +150	°C
Power dissipation	500	mW

EQUIVALENT CIRCUIT



LINEAR

Signetics

VIDEO AMPLIFIER NE5592

Preliminary

DC ELECTRICAL CHARACTERISTICS

$T_A = +25°C$, $V_{SS} = \pm 6V$, $V_{CM} = 0$ unless otherwise specified.
Recommended operating supply voltage $V_S = \pm 6.0V$.

PARAMETER	TEST CONDITIONS	NE5592			UNITS
		Min	Typ	Max	
Differential voltage gain					
Gain 1[1]	$R_L = 2k\Omega$, $V_{OUT} = 3V$ p-p	250	400	600	V/V
Bandwidth					
Gain 1[1]			40		MHz
Rise Time					
Gain 1[1]	$V_{OUT} = 1V$ p-p		10.5		ns
Propagation delay					
Gain 1[1]	$V_{OUT} = 1V$ p-p		7.5		ns
Input resistance					
Gain 1[1]			4.0		kΩ
Input capacitance[1]			2.0		pF
Input offset current			0.4	5.0	μA
Input bias current			9.0	30	μA
Input noise voltage	BW 1kHz to 10MHz		12		μVrms
Input voltage range				±1.0	V
Common mode rejection ratio					
Gain 1[1]	$V_{CM} \pm 1V$, F < 100kHz	60	86		dB
Gain 1[1]	$V_{CM} \pm 1V$, F = 5MHz		60		dB
Supply voltage rejection ratio					
Gain 1[1]	$\Delta V_S = \pm 0.5V$	50	70		dB
Channel separation	$V_{OUT} = 3V_{PP}$; F = 100K (input referenced)		85		dB
Output offset voltage					
Gain 1[1]	$R_L = \infty$			1.5	V
Gain 2[2]	$R_L = \infty$		0.35	0.75	V
Output common mode voltage	$R_L = \infty$	2.4	2.9	3.4	V
Output differential voltage swing	$R_L = 2k$	3.0	4.0		V
Output resistance			20		Ω
Power supply current	$R_L = \infty$		18	24	mA
THE FOLLOWING SPECS APPLY OVER TEMPERATURE		**0°C ≤ T_A ≤ 70°C**			
Differential voltage gain					
Gain 1[1]	$R_L = 2k\Omega$, $V_{OUT} = 3V$ p-p	250		600	V/V
Input resistance					
Gain 1[1]					kΩ
Input offset current				6.0	μA
Input bias current				40	μA
Input voltage range		±1.0			V
Common mode rejection ratio					
Gain 1[1]	$V_{CM} \pm 1V$, F < 100kHz	50			dB
Supply voltage rejection ratio					
Gain 1[1]	$\Delta V_S = \pm 0.5V$	50			dB
Channel separation	$V_{OUT} = 3V_{PP}$; F = 100K (input referenced)		75		dB
Output offset voltage					
Gain 1	$R_L = \infty$			1.5	V
Gain 2[2]	$R_L = \infty$			1.0	V
Output differential voltage swing	$R_L = 2k$	2.8			V
Power supply current	$R_L = \infty$			27	mA

NOTES:
1. Gain select pins connected together.
2. All gain select pins open.

SSi Telecommunications Integrated Circuit Capabilities

Silicon Systems offers a broad line of standard telecommunications circuits aimed at providing cost-effective solutions for common customer application problems. At the heart of SSi's efforts in the communications market is its pioneering work with CMOS switched capacitor filters. Our early success with the DTMF receiver has enabled us to develop a family of chips utilizing the switched capacitor filter technology.

As a trendsetter in the field, Silicon Systems is leading the way towards a whole new era of VLSI circuits for telecommunications. Our broad selection of DTMF receivers demonstrates not only technological leadership in our own semiconductor field but also our capability to anticipate the growing needs of the fast-paced telecommunications marketplace.

PROCESSES
Silicon Systems offers circuits in junction-isolated, bipolar, single and double-layer metal. Plus, SSi has a CMOS capability that includes not only a metal-gate process but also a silicon-gate process that produces circuits packed with more functions in a smaller size for high-speed, low-power performance. These are the most popular and reliable processes in the two basic technologies, and SSI's advanced ultra-clean wafer fab produces higher yields than ordinary facilities.

PRODUCT QUALITY
Silicon Systems has made a major investment in product test and in-line quality control equipment. For example, a state-of-the-art LTX CP80 is used for functional and parametric testing of sophisticated analog, digital, and combination A/D circuits. In this way, SSi is dedicated to the delivery of complex VLSI circuits to meet the incoming quality level you require.

Here are a few completed circuits that demonstrate our broad telecommunications IC capability:

BIPOLAR

Integrated Circuit Function	Application
Audio System Receiver	Telephone Answering Machine
VHF/UHF Gain Mixer	Radio Receiver
Pulse Width Modulator	Switching Power Supply
Controller	Home Appliance
Digital Receiver	Remote Control
PCM Encoder/Decoder	Telecom System
Digital Correlator/ Integrator	Radio Telescope

MOS

Integrated Circuit Function	Application
DTMF Receiver	*Decodes Touch-Tone® Telephone Signals
300 Baud Modem	Data Transmission
1200/2400 Baud Receiver	FSK/PSK Modem
Error Corrector	Military Radio
Remote Transmitter	Telephone Answering Machine
Phoneme Based Speech Synthesizer	Text-to-Speech
Display Timing Generator	TV Sets
Video Processor	Infrared Video System
16 Channel Switching Matrix	Bank Communications System
Digital Loop Detector	Traffic Signal Control
Programmable Digital Receiver	Home Appliance Remote Control
Vocal Tract System	Speech Synthesis

LINEAR

Silicon Systems incorporated

SSI STANDARD PRODUCTS TELECOMMUNICATIONS CIRCUITS

Part Number	Circuit Type	Package
DTMF's Receivers/Filters		
SSI 201	12V, DTMF Receiver	22 DIP
SSI 202	5V, DTMF Receiver	18 DIP
SSI 203	5V, DTMF Receiver (w/early detect)	18 DIP
SSI 5601	5V/12V, Dial Tone Reject Filter	14 DIP
Modem		
SSI 180	1200 Baud FSK Modem	16 DIP
Speech Synthesizer		
SSI SC-01	VOTRAX SC-01 Compatible	22 DIP
SSI 263	VOTRAX SC-02 Compatible	24 DIP
Switched Capacitor Filter Array		
SCA-6 SCA-12	CMOS Semicustom SCF Array (6 filter sections) CMOS Semicustom SCF Array (12 filter sections)	8-28 DIP 24-40 DIP

Silicon Systems incorporated
14351 Myford Road, Tustin, California 92680 (714) 731-7110, TWX 910-595-2809

Don't miss the Sections on Semicustom ICs

Digital Gate Arrays, Standard Cells, and Linear Arrays Are All Covered

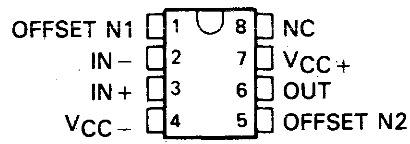
Vol. II, page 4425

TYPES TL291, TL292, TL294
HIGH-FREQUENCY OPERATIONAL AMPLIFIERS

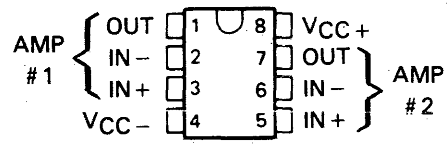
D2782, SEPTEMBER 1983

- **Small-Signal Unity-Gain Bandwidth . . . 20 MHz Typ**
- **Noninverting Slew Rate . . . 50 V/μs Typ (Unity-Gain Follower)**
- **Internal Frequency Compensation**
- **Full-Power Bandwidth at V_{OPP} = 20 V . . . 400 kHz Typ**
- **Open-Loop Gain at Full-Power Bandwidth, V_{OPP} = 20 V . . . 34 dB Typ**
- **Output Short-Circuit Protection**
- **TL291 Has Offset Null Capability**
- **Pinout is Same as Standard General Purpose Operational Amplifiers**

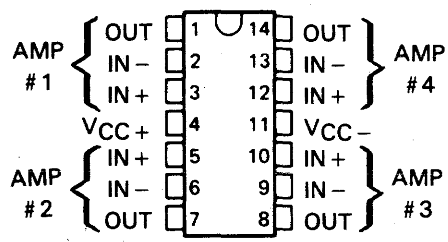
TL291
JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



TL292
JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



TL294
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC—No internal connection

description

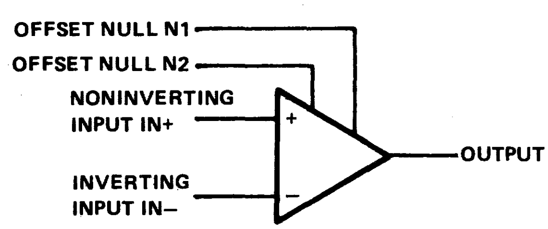
These devices are high-speed operational amplifiers designed for applications requiring wide bandwidth and a fast slew rate. These monolithic circuits incorporate new high-frequency P-N-P transistors that eliminate the need for large feed-forward capacitors required in previous moderately high-frequency designs to pass the signal around slow lateral P-N-P stages.

These operational amplifiers have a typical full-power bandwidth of 400 kilohertz for a 20-volt peak-to-peak output swing. because of the higher 20-megahertz unity-gain bandwidth, the typical open-loop gain at the 400-kilohertz full-power bandwidth is a very respectable 34 decibels.

The TL291 single-channel operational amplifier pinout includes offset nulling, which is easily accomplished by connecting a potentiometer across the offset null pins with the wiper connected to the V_{CC-} pin.

The TL291M, TL292M, and TL294M will be characterized for operation over the full military temperature range of −55°C to 125°C. The TL291C, TL292C, and TL294C will be characterized for operation from 0°C to 70°C.

symbol (each amplifier)



TI Sales Offices

ALABAMA: Huntsville, 500 Wynn Drive, Suite 514, Huntsville, AL 35805, (205) 837-7530.

ARIZONA: Phoenix, P.O. Box 35160, 8102 N. 23rd Ave., Suite A, Phoenix, AZ 85021, (602) 995-1007.

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INDIANA: Ft. Wayne, 2020 Inwood Dr., Ft. Wayne, IN 46805, (219) 424-5174; **Indianapolis,** 2346 S. Lynhurst, Suite J-400, Indianapolis, IN 46241, (317) 248-8555.

IOWA: Cedar Rapids, 373 Collins Rd. NE, Suite 200, Cedar Rapids, IA 52402, (319) 395-9550.

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MICHIGAN: Farmington Hills, 33737 W. 12 Mile Rd., Farmington Hills, MI 48018, (313) 553-1500.

MINNESOTA: Edina, 7625 Parklawn, Edina, MN 55435, (612) 830-1600.

MISSOURI: Kansas City, 8080 Ward Pkwy., Kansas City, MO 64114, (816) 523-2500; **St. Louis,** 11861 Westline Industrial Drive, St. Louis, MO 63141, (314) 569-7600.

NEW JERSEY: Clark, 292 Terminal Ave. West, Clark, NJ 07066, (201) 574-9800.

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IOWA: Arrow (319) 395-7230.

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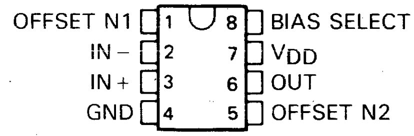
TYPES TLC251, TLC251A, TLC251B, TLC271, TLC271A, TLC271B
PROGRAMMABLE LOW-POWER LinCMOS™ OPERATIONAL AMPLIFIERS

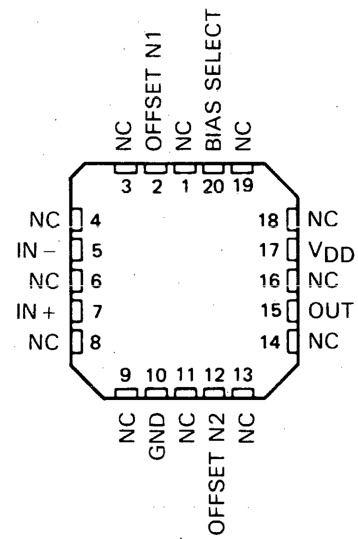
D2751, JULY 1983—REVISED OCTOBER 1983

- **Wide range of Supply Voltages:**
  1 V to 16 V (TLC251)
  4 V to 16 V (TLC271)
- **True Single-Supply Operation**
- **Common-Mode Input Voltage Includes the Negative Rail**
- **Low Noise . . . 30 nV/√Hz Typ at 1 kHz (High-Bias)**

D, JG, OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



FH OR FK PACKAGE
(TOP VIEW)

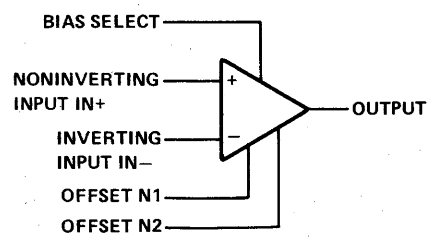


NC No internal connection

description

The TLC251 and TLC271 series are low-cost, low-power programmable operational amplifiers designed to operate with single or dual supplies. Unlike traditional metal-gate CMOS op amps, these devices utilize the Texas Instruments silicon gate LinCMOS™ process, giving them stable input offset voltages without sacrificing the advantages of metal-gate CMOS. This series of parts is available in selected grades of input offset voltage and can be nulled with one external potentiometer. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this family is ideally suited for battery-powered or energy-conserving applications. A bias-select pin can be used to program one of three ac performance and power-dissipation levels to suit the application. The TLC251 offers the same operation as the TLC271, but also features guaranteed operation down to a 1 V supply. Both devices are stable at unity gain.

symbol



TEMPERATURE RANGES AND PACKAGES

SERIES	TEMPERATURE RANGE	PACKAGES
TLC251C Types	0°C to 70°	JG, P, D
TLC271C Types	0°C to 70°C	JG, P, D
TLC271I Types	−40°C to 85°C	JG, P, D
TLC271M Types	−55°C to 125°C	JG, FH, FK

DEVICE FEATURES

PARAMETER	LOW BIAS	MEDIUM BIAS	HIGH BIAS
Supply current (Typ)	10 μA	150 μA	1000 μA
Slew rate (Typ)	0.04 V/μs	0.6 V/μs	4.5 V/μs
Input offset voltage (Max)			
. . . Standard types	10 mV	10 mV	10 mV
. . . A-suffix types	5 mV	5 mV	5 mV
. . . B-suffix types	2 mV	2 mV	2 mV
Offset voltage change (Typ)	0.1 μV/month† 0.7 μV/°C	0.1 μV/month† 2 μV/°C	0.1 μV/month† 5 μV/°C
Input bias current (Typ)	1 pA	1 pA	1 pA
Input offset current (Typ)	1 pA	1 pA	1 pA

†The long-term drift value applies after the first month.

LINEAR

Texas Instruments

ADVANCE INFORMATION

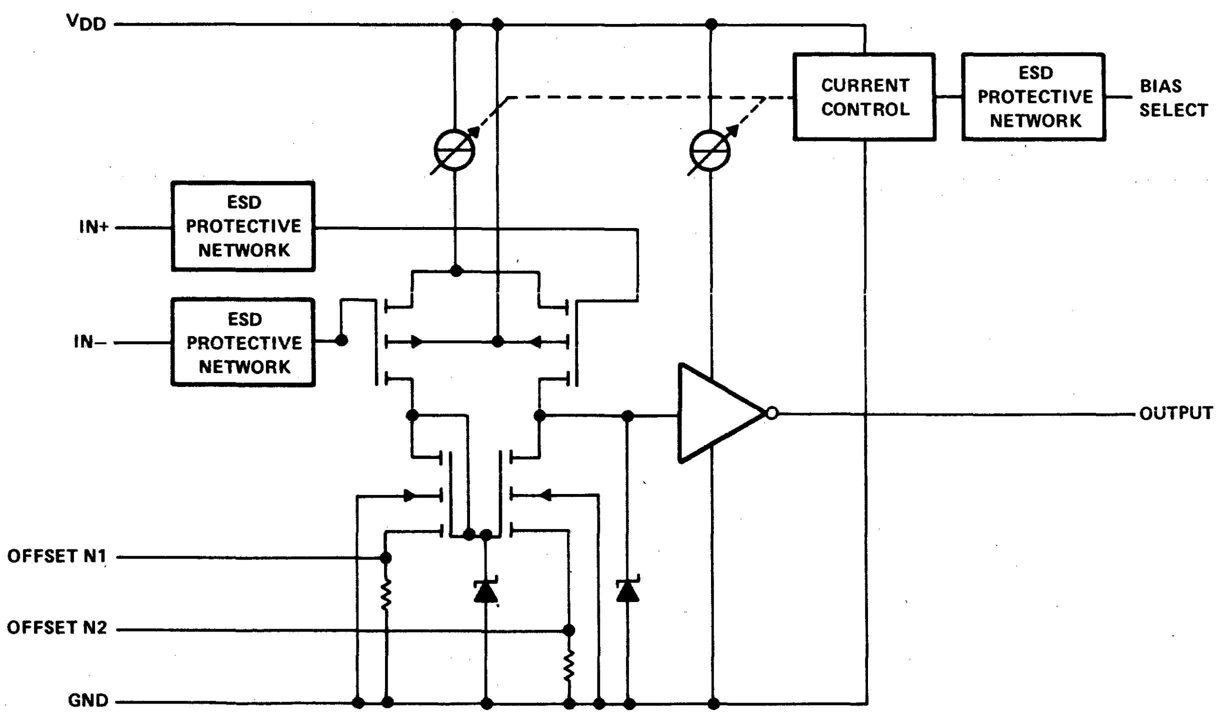
This document contains information on a new product. Specifications are subject to change without notice.

These devices have internal Electrostatic Discharge (ESD) protection circuits which will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883B Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

Because of the extremely high input impedance and low input bias and offset currents, applications for the TLC251 and TLC271 series include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS operational amplifiers without the power penalties of traditional bipolar devices. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC271. Remote and inaccessible equipment applications are possible using the low-voltage and low-power capabilities of the TLC251. In addition, by driving the bias-select input with a logic signal from a microprocessor, these operational amplifiers can have software-controlled performance and power consumption. The TLC251 is well suited to solve the difficult problems associated with single-battery and solar-cell-powered applications.

Devices having an "M" suffix are characterized for operation over the temperature range of −55°C to 125°C, those with an "I" suffix are characterized for operation from −40°C to 85°C, and those with a "C" suffix are characterized for operation from 0°C to 70°C.

schematic



LINEAR

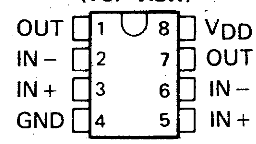
Texas Instruments

TYPES TLC252, TLC25L2, TLC25M2, TLC272, TLC27L2, TLC27M2
LinCMOS™ DUAL OPERATIONAL AMPLIFIERS

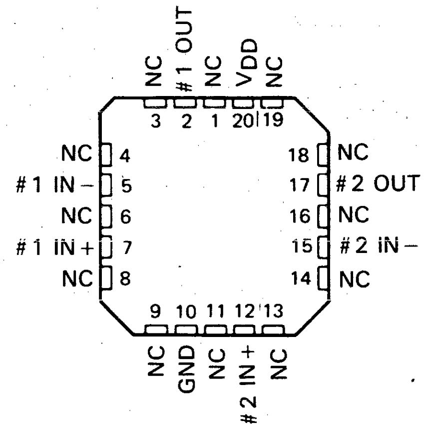
JUNE 1983—REVISED OCTOBER 1983

- **Wide range of Supply Voltages:**
  1 V to 16 V (TLC252 types)
  4 V to 16 V (TLC272 types)
- **True Single-Supply Operation**
- **Common-Mode Input Voltage Includes the Negative Rail**
- **Low Noise . . . 30 nV/√Hz Typ at f = 1 kHz (High-Bias Versions)**

D, JG, OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



FH OR FK PACKAGE
(TOP VIEW)

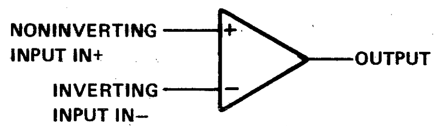


NC—No internal connection

description

The TLC252 and TLC272 series are low-cost, low-power dual operational amplifiers designed to operate with single or dual supplies. These devices utilize the Texas Instruments silicon gate LinCMOS™ process, giving them stable input offset voltages that are available in selected grades of 2, 5 or 10 mV maximum, very high input impedances, and extremely low input offset and bias currents. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this series is ideally suited for battery-powered or energy-conserving applications. The TLC252 types offer guaranteed operation down to a 1-V supply. All devices are unity-gain stable and have excellent noise characteristics.

symbol (each amplifier)



DEVICE FEATURES

PARAMETER	TLC25L2 TLC27L2 (LOW BIAS)	TLC25M2 TLC27M2 (MEDIUM BIAS)	TLC252 TLC272 (HIGH BIAS)
Supply current (Typ)	20 μA	300 μA	2000 μA
Slew rate (Typ)	0.04 V/μs	0.6 V/μs	4.5 V/μs
Input offset voltage (Max)			
. . . Standard types	10 mV	10 mV	10 mV
. . . A-suffix types	5 mV	5 mV	5 mV
. . . B-suffix types	2 mV	2 mV	2 mV
Offset voltage change (Typ)	0.1 μV/month† 0.7 μV/°C	0.1 μV/month† 2 μV/°C	0.1 μV/month† 5 μV/°C
Input bias current (Typ)	1 pA	1 pA	1 pA
Input offset current (Typ)	1 pA	1 pA	1 pA

†The offset voltage drift applies after the first month only.

TEMPERATURE RANGES AND PACKAGES

SERIES	TEMPERATURE RANGE	PACKAGES
TLC252C Types	0°C to 70°	JG, P, D
TLC272C Types	0°C to 70°C	JG, P, D
TLC272I Types	−40°C to 85°C	JG, P, D
TLC272M Types	−55°C to 125°C	JG, FH, FK

ADVANCE INFORMATION

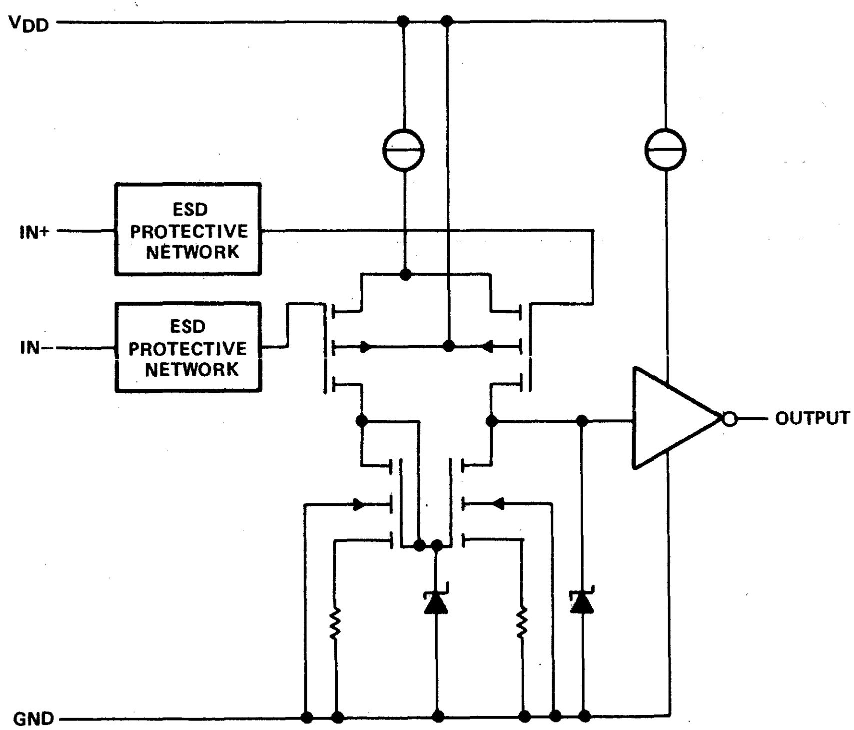
This document contains information on a new product. Specifications are subject to change without notice.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

These devices have internal Electrostatic Discharge (ESD) protection circuits which will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883B Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

Because of the extremely high input impedance and low input bias and offset currents, applications for the TLC252 and TLC272 series include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS™ operational amplifiers without the power penalties of traditional bipolar devices. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC252 and TLC272 series. Remote and inaccessible equipment applications are possible using the low-voltage and low-power capabilities of the TLC252. The TLC252 types are well suited to solve the difficult problems associated with single-battery and solar-cell-powered applications. This series includes devices that are characterized for commercial, industrial, and military temperature ranges and are available in 8-pin plastic and ceramic dual-in-line (DIP) packages, small outline (D) package, and chip carrier (FH, FK) packages.

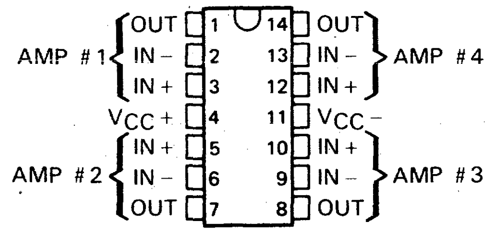
schematic (each amplifier)



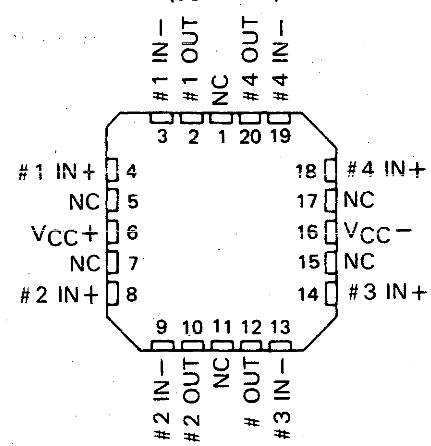
D2753, JUNE 1983—REVISED OCTOBER 1983

- **Wide range of Supply Voltages:**
  1 V to 16 V (TLC254 types)
  4 V to 16 V (TLC274 types)
- **True Single-Supply Operation**
- **Common-Mode Input Voltage Includes the Negative Rail**
- **Low Noise . . . 30 nV/√Hz Typ at f = 1 kHz (High-Bias Versions)**

D, J, OR N DUAL IN-LINE-PACKAGE
(TOP VIEW)



FH OR FK PACKAGE
(TOP VIEW)



NC—No internal connection

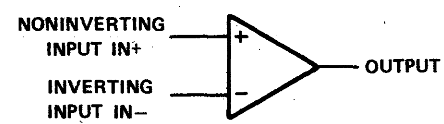
description

The TLC254 and TLC274 series are low-cost, low-power dual operational amplifiers designed to operate with single or dual supplies. These devices utilize the Texas Instruments silicon gate LinCMOS™ process, giving them stable input offset voltages that are available in selected grades of 2, 5 or 10 mV maximum, very high input impedances, and extremely low input offset and bias currents. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this series is ideally suited for battery-powered or energy-conserving applications. The TLC254 types offer guaranteed operation down to a 1-V supply. All devices are unity-gain stable and have excellent noise characteristics.

TEMPERATURE RANGES AND PACKAGES

DEVICE TYPES	TEMPERATURE RANGE	PACKAGES
TLC254C	0°C to 70°	J, N, D
TLC274C	0°C to 70°C	J, N, D
TLC274I	−40°C to 85°C	J, N, D
TLC274M	−55°C to 125°C	J, FH, FK

symbol (each amplifier)



DEVICE FEATURES

PARAMETER	TLC25L4 TLC27L4 (LOW BIAS)	TLC25M4 TLC27M4 (MEDIUM BIAS)	TLC254 TLC274 (HIGH BIAS)
Supply current (Typ)	40 μA	600 μA	4000 μA
Slew rate (Typ)	0.04 V/μs	0.6 V/μs	4.5 V/μs
Input offset voltage (Max)			
. . . Standard types	10 mV	10 mV	10 mV
. . . A-suffix types	5 mV	5 mV	5 mV
. . . B-suffix types	2 mV	2 mV	2 mV
Offset voltage change (Typ)	0.1 μV/month† 0.7 μV/°C	0.1 μV/month† 2 μV/°C	0.1 μV/month† 5 μV/°C
Input bias current (Typ)	1 pA	1 pA	1 pA
Input offset current (Typ)	1 pA	1 pA	1 pA

†The long-term drift value applies after the first month.

LINEAR

Texas Instruments

ADVANCE INFORMATION

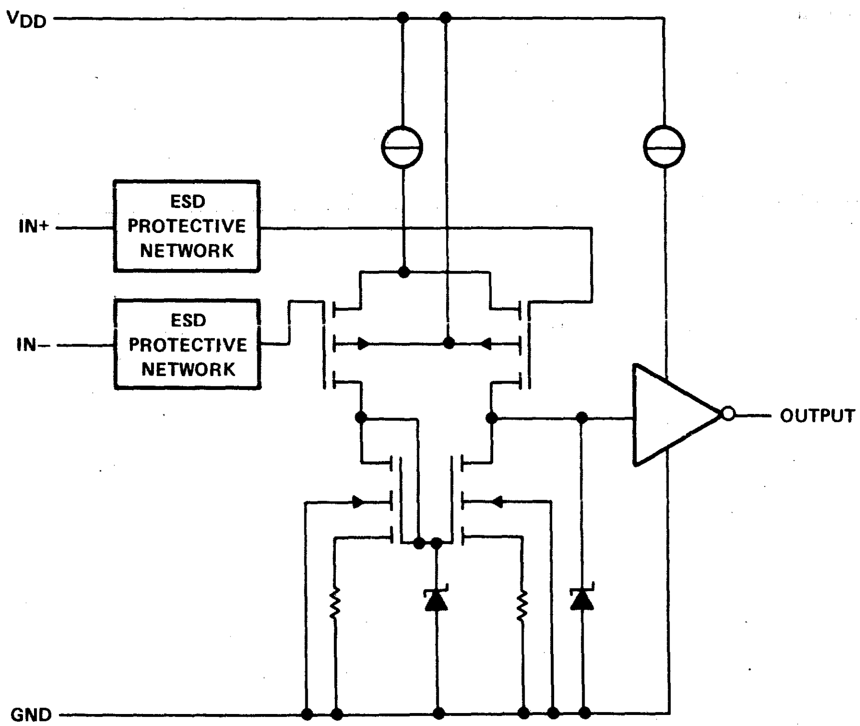
This document contains information on a new product. Specifications are subject to change without notice.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

These devices have internal Electrostatic Discharge (ESD) protection circuits which will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883B Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

Because of the extremely high input impedance and low input bias and offset currents, applications for the TLC254 and TLC274 series include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS™ operational amplifiers without the power penalties of traditional bipolar devices. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC254 and TLC274 series. Remote and inaccessible equipment applications are possible using the low-voltage and low-power capabilities of the TLC254. The TLC254 types are well suited to solve the difficult problems associated with single-battery and solar-cell-powered applications. This series includes devices that are characterized for commercial, industrial, and military temperature ranges and are available in 14-pin plastic and ceramic dual-in-line (DIP) packages, small outline (D) package, and chip carrier (FH, FK) packages.

schematic (each amplifier)

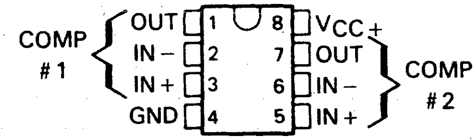


TYPES TLC372M, TLC372C
DUAL LinCMOS™ DIFFERENTIAL COMPARATORS

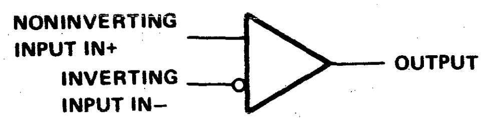
OCTOBER 1983

- **Single- or Dual-Supply Operation**
- **Wide Range of Supply Voltages 2 to 18 Volts**
- **Very Low Supply Current Drain 0.2 mA Typ**
- **Fast Response Time . . . 200 ns Typ for TTL-Level Input Step**
- **Built-In ESD Protection**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **Extremely Low Input Bias Current 1 pA Typ**
- **Ultra-Stable Low Input Offset Voltage**
- **Common-Mode Input Voltage Range Includes Ground**
- **Output Compatible with TTL, MOS, and CMOS**

**JG OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)**



symbol (each comparator)



description

This device is fabricated using LinCMOS™ technology and consists of two independent voltage comparators designed to operate from a single power supply. Operation from dual supplies is also possible so long as the difference between the two supplies is 2 to 18 volts. Each of these devices features extremely high input impedance (typically greater than 10^{12} ohms) allowing direct interfacing with high-impedance sources. The outputs are n-channel open-drain configurations, and can be connected to achieve positive-logic wired-AND relationships.

These devices have internal Electrostatic Discharge (ESD) protection circuits which will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883B Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

The TLC372M is characterized for operation over the full military temperature range of −55°C to 125°C. The TLC372C is characterized for operation from 0°C to 70°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TLC372M	TLC372C	UNIT
Supply voltage (see Note 1)		18	18	V
Differential input voltage (see Note 2)		±18	±18	V
Input voltage, V_I		18	18	V
Output voltage, V_O		18	18	V
Output current, I_O		20	20	mA
Duration of output short-circuit to ground (see Note 3)		unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 4)		900	900	mW
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
4. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2. In the J package, the TLC372C chips are glass-mounted; the TLC372M chips are alloy-mounted.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			TLC372M			TLC372C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$ min, See Note 5		25°C		2	10		2	10	mV
				Full range			12			12	
I_{IO}	Input offset current	See Note 5		25°C		1			1		pA
				Full range			10			0.3	nA
I_{IB}	Input bias current			25°C		1					pA
				Full range			20			0.6	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to $V_{CC}-1.5$			0 to $V_{CC}-1.5$			V
				Full range	0 to $V_{CC}-2$			0 to $V_{CC}-2$			
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, $R_L \geq$ 15 kΩ to V_{CC}		25°C		200			200		V/mV
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1		nA
			V_{OH} = 15 V	Full range			1			1	μA
V_{OL}	Low-level output voltage	V_{ID} = 1 V, I_{OL} = 4 mA		25°C		150	400		150	400	mV
				Full range			700			700	
I_{OL}	Low-level output current	V_{ID} = 1 V, V_{OL} = 1.5 V		25°C	6	16		6	16		mA
I_{CC}	Supply current (two comparators)	V_{ID} = −1 V, No load		25°C		0.2			0.2		mA

†All characteristics are measured with zero common-mode input voltage unless otherwise specified.

NOTE 5: The offset voltages and offset currents given are the maximum values required to drive the output up to 4 V or down to 400 mV with a pull-up resistor of 2.5 kΩ to V_{CC}. Thus, these parameters actually define an error band and take into account the worst-case effects of voltage gain and input impedance. Full range for T_A is −55°C to 125°C for TLC372M, 0°C to 70°C for TLC372C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF‡ See Note 6	100-mV input step with 5-mV overdrive		0.9		μs
		TTL-level input step		0.2		

‡C_L includes probe and jig capacitance.

NOTE 6: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

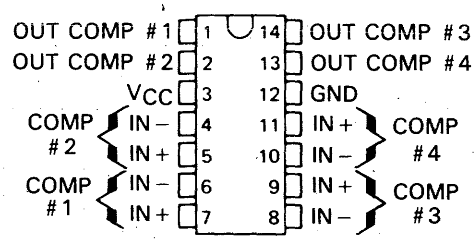
TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES TLC374M, TLC374C QUADRUPLE LinCMOS™ DIFFERENTIAL COMPARATORS

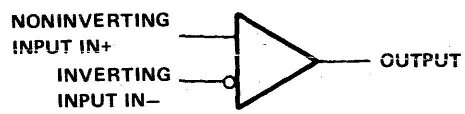
D2783, SEPTEMBER 1983

- Single- or Dual-Supply Operation
- Wide Range of Supply Voltages 2 to 18 volts
- Very Low Supply Current Drain 0.4 mA Typ
- Fast Response Time . . . 200 ns Typ for TTL-Level Input Step
- Built-In ESD Protection
- High Input Impedance . . . 10^{12} Ω Typ
- Extremely Low Input Bias Current 1 pA Typ
- Ultra-Stable Low Input Offset Voltage
- Common-Mode Input Voltage Range Includes Ground
- Output Compatible with TTL, MOS, and CMOS

TLC374M . . . J DUAL-IN-LINE PACKAGE
TLC374C . . . D, J, OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



symbol (each comparator)



description

This device is fabricated using LinCMOS™ technology and consists of four independent voltage comparators designed to operate from a single power supply. Operation from dual supplies is also possible so long as the difference between the two supplies is 2 to 18 volts. Each of these devices features extremely high input impedance (typically greater than 10^{12} ohms) allowing direct interfacing with high-impedance sources. The outputs are n-channel open-drain configurations, and can be connected to achieve positive-logic wired-AND relationships. The TLC374C is designed as a pin-compatible, functional replacement for the LM339, offering twice the speed while consuming typically one-half of the power.

These devices have internal Electrostatic Discharge (ESD) protection circuits which will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883B Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

The TLC374M is characterized for operation over the full military temperature range of −55°C to 125°C. The TLC374C is characterized for operation from 0°C to 70°C.

PRODUCT PREVIEW

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TLC374M	TLC374C	UNIT
Supply voltage (see Note 1)		18	18	V
Differential input voltage (see Note 2)		±18	±18	V
Input voltage, V_I		18	18	V
Output voltage, V_O		18	18	V
Output current, I_O		20	20	mA
Duration of output short-circuit to ground (see Note 3)		unlimited	unlimited	
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 4)		900	900	mW
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package		260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
4. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves, Section 2. In the J package, the TLC374C chips are glass-mounted; the TLC374M chips are alloy-mounted.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			TLC374M MIN	TLC374M TYP	TLC374M MAX	TLC374C MIN	TLC374C TYP	TLC374C MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$ min, See Note 5		25°C		2	10		2	10	mV
				Full range			12			12	mV
I_{IO}	Input offset current	See Note 5		25°C		1			1		pA
				Full range			10			0.3	nA
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			20			0.6	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to $V_{CC}-1.5$			0 to $V_{CC}-1.5$			V
				Full range	0 to $V_{CC}-2$			0 to $V_{CC}-2$			V
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, $R_L \geq 15$ kΩ to V_{CC}		25°C		200			200		V/mV
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1		nA
			V_{OH} = 15 V	Full range			1			1	μA
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 4 mA		25°C		150	400		150	400	mV
				Full range			700			700	mV
I_{OL}	Low-level output current	V_{ID} = −1 V, V_{OL} = 1.5 V		25°C	6	16		6	16		mA
I_{CC}	Supply current (four comparators)	V_{ID} = −1 V, No load		25°C		0.4	1		0.4	1	mA

†All characteristics are measured with zero common-mode input voltage unless otherwise specified.

NOTE 5: The offset voltages and offset currents given are the maximum values required to drive the output up to 4 V or down to 400 mV with a pull-up resistor of 2.5 kΩ to V_{CC}. Thus, these parameters actually define an error band and take into account the worst-case effects of voltage gain and input impedance. Full range for T_A is −55°C to 125°C for TLC374M, 0°C to 70°C for TLC374C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF‡, See Note 6	100-mV input step with 5-mV overdrive		0.9		μs
		TTL-level input step		0.2		μs

‡C_L includes probe and jig capacitance.

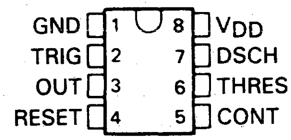
NOTE 6: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

TYPES TLC555M, TLC555C LinCMOS™ TIMERS

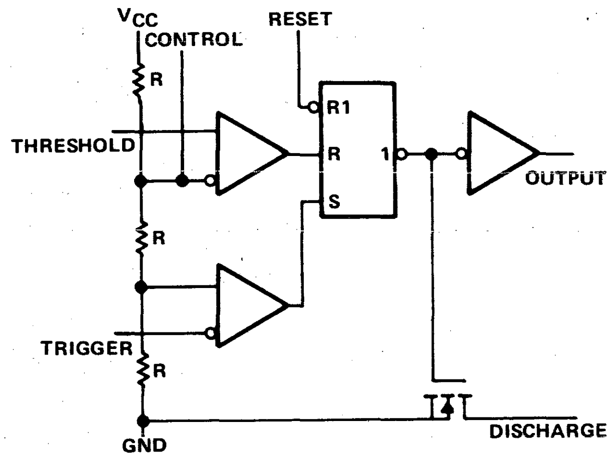
D2784, SEPTEMBER 1983

- Very Low Power Consumption . . . 1 mW Typ at V_{DD} = 5 V
- Capable of Very High-Speed Operation . . . Typically 2 MHz in Astable Mode
- Complementary CMOS output Capable of Swinging Rail-to-Rail
- High Output-Current Capability
  . . . Sink 100 mA Typ
  . . . Source 10 mA Typ
- Output Fully CMOS-, TTL-, and MOS-Compatible
- Low Supply Current Reduces Spikes During Output Transitions
- High Impedance Inputs . . . 10^{12} Ω Typ
- Single-Supply Operation from 2 to 18 volts
- Functionally Interchangeable with the Signetics NE555; has Same Pinout

TLC555M . . . JG PACKAGE
TLC555C . . . D, JG, or P PACKAGE
(TOP VIEW)



functional block diagram



Reset can override Trigger, which can override Threshold.

description

The TLC555 is a monolithic timing circuit fabricated using TI's LinCMOS™ process. Due to its high-impedance inputs (typically 10^{12} Ω), it is capable of producing accurate time delays and oscillations while using less expensive, smaller timing capacitors than the NE555. Like the NE555, the TLC555 achieves both monostable (using one resistor and one capacitor) and astable (using two resistors and one capacitor) operation. In addition, 50% duty cycle astable operation is possible using only a single resistor and one capacitor. The LinCMOS™ process allows the TLC555 to operate at frequencies up to 2 MHz and be fully compatible with CMOS, TTL, and MOS logic. It also provides very low power consumption (typically 1 mW at V_{DD} = 5 V) over a wide range of supply voltages ranging from 2 volts to 18 volts.

Like the NE555, the threshold and trigger levels are normally two-thirds and one-third respectively of V_{DD}. These levels can be altered by use of the control voltage terminal. When the trigger input falls below trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. When the reset input goes low, the flip-flop is reset and the output goes low. Whenever the output is low, a low impedance path is provided between the discharge terminal and ground.

While the complementary CMOS output is capable of sinking over 100 mA and sourcing over 10 mA, the TLC555 exhibits greatly reduced supply current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE555.

These devices have internal Electrostatic Discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883B Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

All unused inputs should be tied to an appropriate logic level to prevent false triggering.

The TLC555M is characterized for operation over the full military temperature range of −55 °C to 125 °C; the TLC555C is characterized for operation from 0 °C to 70 °C.

ADVANCE INFORMATION

This document contains information on a new product. Specifications are subject to change without notice.

FUNCTION TABLE

RESET	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	< 1/3 V_{DD}	Irrelevant	High	Off
High	> 1/3 V_{DD}	> 2/3 V_{DD}	Low	On
High	> 1/3 V_{DD}	< 2/3 V_{DD}	As previously established	

†Voltages levels shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Input voltage range (any input) . . . . . −0.3 V to 18 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 600 mW
Operating free-air temperature range: TLC555M . . . . . −55°C to 125°C
TLC555C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: D or P package . . . . . 300°
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Table. In the JG package, TLC555M chips are alloy-mounted and TLC555C chips are glass-mounted.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	OPERATING FACTOR	ABOVE T_A
D	600 mW	5.8 mW/°C	46°C
JG (Alloy-Mounted Chip)	600 mW	8.4 mW/°C	79°C
JG (Glass-Mounted Chip)	600 mW	6.6 mW/°C	59°C
P	600 mW	No derating necessary	

electrical characteristics at 25°C free-air temperature, V_{DD} = 5 V to 15 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Threshold voltage level as a percentage of supply voltage				66.7%		
Threshold current	V_{DD} = 5 V			10		pA
Trigger voltage level as a percentage of supply voltage				33.3%		
Trigger current	V_{DD} = 5 V			10		pA
Reset voltage level				0.7		V
Reset current	V_{DD} = 5 V			±10		pA
Control voltage (open-circuit) as a percentage of supply voltage				66.7%		
Low-level output voltage	V_{DD} = 15 V	I_{OL} = 10 mA		0.1		V
		I_{OL} = 50 mA		0.5		
		I_{OL} = 100 mA		1		
	V_{DD} = 5 V	I_{OL} = 5 mA		0.1		
		I_{OL} = 8 mA		0.16		
High-level output voltage	V_{DD} = 15 V	I_{OH} = −1 mA		14.8		V
		I_{OH} = −5 mA		14		
		I_{OH} = −10 mA		12.7		
	V_{DD} = 5 V	I_{OH} = −2 mA		4		
		I_{OH} = −1 mA		4.5		
Supply current	V_{DD} = 15 V			360		μA
	V_{DD} = 5 V			170		

operating characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Initial error of timing interval	V_{DD} = 5 V to 15 V, R_A = R_B = 1 kΩ to 100 kΩ, C_T = 0.1 μF, See Figure 1		1%		
Supply voltage sensitivity of timing interval			0.1		%/V
Output pulse rise time	V_{DD} = 5 V, R_L = 10 MΩ, C_L = 10 pF		20		ns
Output pulse fall time			20		
Maximum frequency in astable mode	R_A = 470 Ω, R_B = 200 Ω, C_T = 200 pF		2.1		MHz

TYPICAL APPLICATION DATA

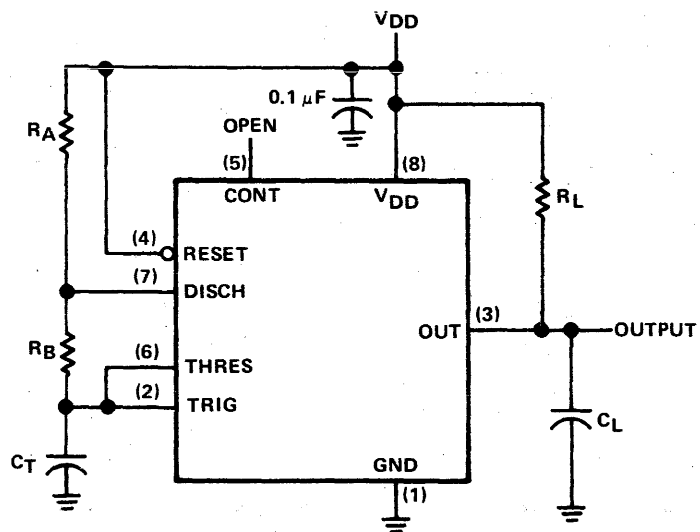


FIGURE 1—CIRCUIT FOR ASTABLE OPERATION

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TDC1018
Advance Information

D/A Converter
8 bit, 125 MSPS

The TRW TDC1018 is a 125 MegaSample Per Second (MSPS), 8-bit digital-to-analog converter, capable of directly driving a 75-ohm load. Most applications require no extra registering, buffering, or deglitching. Four special level controls make the device ideal for video applications. All data and control inputs are ECL compatible.

The TDC1018 is built with TRW's OMICRON-B™ 1-micron dual-layer metal bipolar process. On-chip data registers and precise matching of propagation delays make the TDC1018 inherently low-glitching. The TDC1018 offers high performance, low power consumption, and video compatibility in a 24 Lead DIP package.

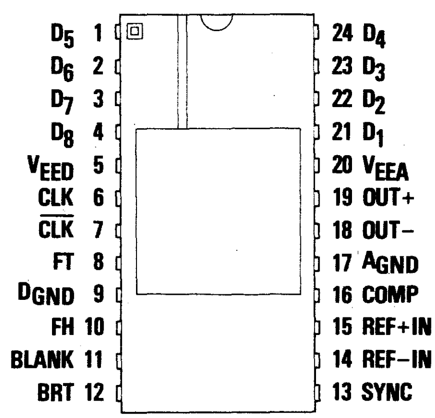
Features

- 125 MSPS Conversion Rate
- 8-Bit
- 1/2 LSB Linearity
- Differential Current Outputs
- Video Controls: Sync, Blank, Bright, Force High
- Low Glitch Energy
- ECL Compatible
- Power Dissipation < 800 mW
- Available In 24 Lead DIP Package
- Single −5.2V Power Supply

Applications

- RGB Graphics
- Digital Synthesizers
- Automated Test Equipment
- Raster Graphic Displays
- High-Resolution Video
- Digital Transmitters/Modulators

Pin Assignments



LSI Products Division
TRW Electronic Components Group
P.O. Box 2472
La Jolla, CA 92038

Phone: (619) 457-1000
Telex: 697-957
TWX: 910-335-1571

40G01211 Rev. B-6/83
Printed in the U.S.A.

TDC1048

Preliminary Information

TRW

Monolithic Video A/D Converter

8 bit, 20 MSPS

The TRW TDC1048 is a 20 MegaSample Per Second (MSPS) full-parallel (flash) analog-to-digital converter, capable of converting an analog signal with full-power frequency components up to 7 MHz into 8-bit digital words. A sample-and-hold circuit is not necessary. Low power consumption eases thermal considerations, and board space is minimized with a 28 Lead package. All digital inputs and outputs are TTL compatible.

The TDC1048 consists of 255 clocked latching comparators, combining logic, and an output buffer register. A single convert signal controls the conversion operation. The unit can be connected to give either true or inverted outputs in binary or offset two's complement coding.

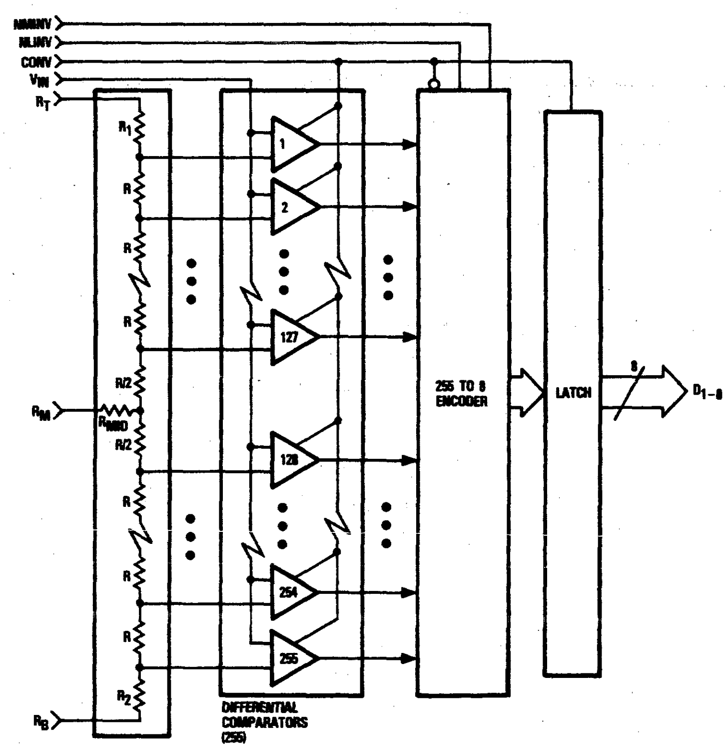
Features

- 8-Bit Resolution
- 20 MSPS Conversion Rate
- Low Power Consumption, 1.4W (Worst Case)
- Sample-And-Hold Circuit Not Required
- Differential Phase 1°
- Differential Gain 2%
- 1/2 LSB Linearity
- TTL Compatible
- Selectable Output Format
- Available In 28 Lead DIP, CERDIP, Or Contact Chip Carrier

Applications

- Low-Cost Video Digitizing
- Radar Data Conversion
- Data Acquisition
- Medical Imaging

Functional Block Diagram



LSI Products Division
TRW Electronic Components Group
P.O. Box 2472
La Jolla, CA 92038

Phone: (619) 457-1000
Telex: 697-957
TWX: 910-335-1571

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A/D Converters

All TRW A/D converters, except the TDC1001 and TDC1002, are fully parallel "flash" types, which accurately sample and convert high-frequency input signals without a track-and-hold circuit. Resolutions from 4 to 9 bits and speeds from 1 to 100 MSPS (MegaSamples Per Second) offer the best choice for most signal processing requirements. The parts are TTL compatible, except as noted below.

Product	Resolution (bits)	Conversion Rate* (MSPS)	Power Dissipation* (watts)	Package	Available	Extended Temperature Range Available	Notes
TDC1001	8	2.5	0.6	J8	Now	−20°C to 85°C	Successive approximation
TDC1002	8	1.0	0.6	J8	Now	−20°C to 85°C	Successive approximation
TDC1007	8	20	2.6	J1, C1, L1	Now	−30°C to 125°C	
				E1, P1	Now	no	Evaluation boards
TDC1014	6	25	1.0	J7, C3, B7	Now	−55°C to 125°C	
				E1, P1	Now	no	Evaluation boards
TDC1019	9	15	2.6	J1, C1, L1	Now	3Q83	ECL-compatible
				E1	Now	no	Evaluation board
TDC1021	4	25	0.3	J9	Now	−55°C to 125°C	
TDC1025	8	50	4.5	C1, L1	3Q83	3Q83	ECL-compatible
				E1	Now	no	Evaluation board
TDC1027	7	18	1.6	J7, B7	Now	4Q83	
TDC1029	6	100	1.6	J7	Now	3Q83	ECL-compatible
				E1	Now	no	Evaluation board

*Guaranteed, Worst Case, T_A = 0°C to 70°C.

D/A Converters

These D/A converters offer 75-ohm, 1V outputs to drive video filters or transmission lines directly. On-chip data registers and careful internal timing to matched current sources result in output glitches that are so small (less than 100 picovolt-seconds worst case) that no resampling circuit or deglitcher is necessary. The TDC1016 has 10 input data bits and is available in three integral linearity grades equivalent to 1/2 LSB error at 8, 9, and 10 bit resolution. The parts have dual-level input buffers which operate with TTL or ECL signals: In ECL mode, only a single −5V power supply is required. The TDC1016 in the J5 or C2 package can operate in a fully differential ECL mode, as well as single-ended ECL or TTL.

Product	Bits	Integral Linearity Error (%)	Conversion Rate * (MSPS)	Power Dissipation* (watts)	Package	Available	Extended Temperature Range Available	Notes
TDC1016	8**	0.20	20	0.7	J5, J7, C2, B7	Now	−55°C to 125°C	
	9**	0.10	20	0.7	J5, J7, C2, B7	Now	3Q83	
	10**	0.05	20	0.7	J5, J7, C2, B7	Now	3Q83	

* Guaranteed, Worst Case, T_A = 0°C to 70°C.

**The TDC1016 has 10 bit resolution, and is available in three linearity grades to meet 8, 9, and 10 bit system requirements.

TDC1025
Preliminary Information

Monolithic A/D Converter
8 Bit, 50 MSPS

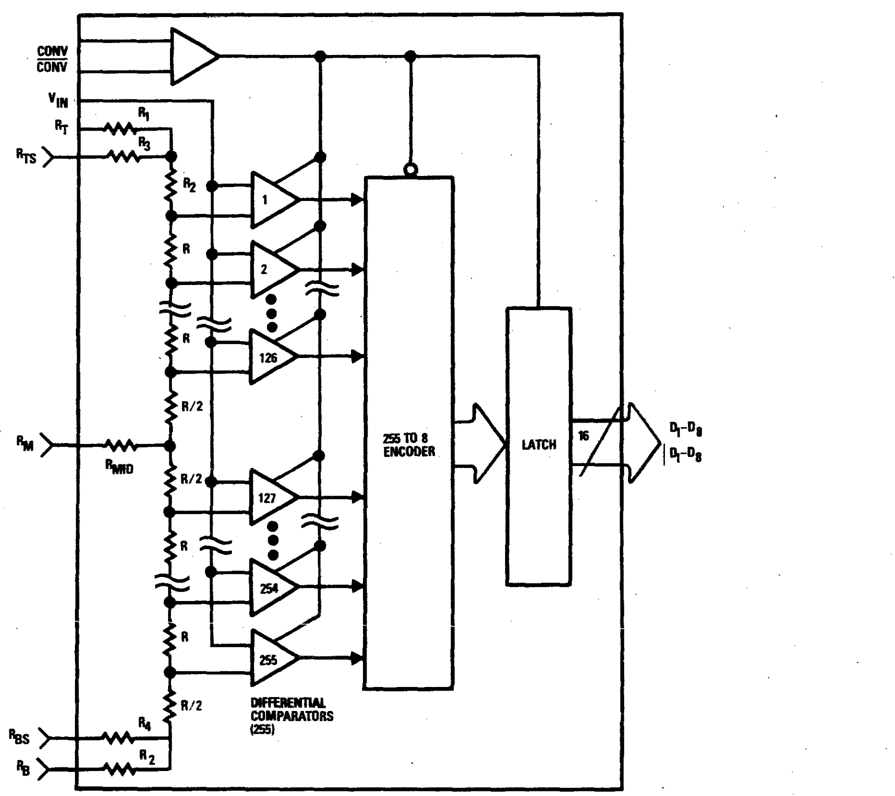
The TRW TDC1025 is a 50 MegaSample Per Second (MSPS) full-parallel (flash) analog-to-digital converter, capable of converting an analog signal with full-power frequency components up to 12 MHz into 8-bit digital words. A sample-and-hold circuit is not necessary. All digital inputs and outputs are ECL compatible.

The TDC1025 consists of 255 latching comparators, combining logic, and an output buffer register. A single convert signal controls the conversion operation. The digital outputs will interface with differential or single-ended ECL. The device requires a single −5.2V power supply.

Features
- 8-Bit Resolution
- 50 MSPS Conversion Rate
- Sample-and-Hold Circuit Not Required
- Differential or Single-Ended ECL Compatible
- Available in 68 Leaded Chip Carrier and 68 Contact Chip Carrier
- Advanced 1-micron (OMICRON-B™) Technology
- Complete Evaluation Board (TDC1025E1C) Available

Applications
- Medical Electronics
- Fluid Flow Analysis
- Seismic Analysis
- Radar/Sonar
- Transient Analysis
- High-Speed Image Processing

Functional Block Diagram



LSI Products Division
TRW Electronic Components Group
P.O. Box 2472
La Jolla, Ca. 92038

Phone: (619) 457-1000
Telex: 697-957
TWX: 910-335-1571

40G00817 Rev. A–6/82
Printed in the U.S.A.

TDC1027
Preliminary Information

Monolithic Video A/D Converter
7 Bit, 18 MSPS

The TRW TDC1027 is an 18 MegaSample Per Second (MSPS) full-parallel (flash) analog-to-digital converter, capable of converting an analog signal with full-power frequency components up to 5 MHz into 7-bit digital words. A sample-and-hold circuit is not necessary. All digital inputs and outputs are TTL compatible.

The TDC1027 consists of 127 latching comparators, combining logic, and an output buffer register. A single convert signal controls the conversion operation. The unit can be connected to give either true or inverted outputs in binary or offset two's complement coding.

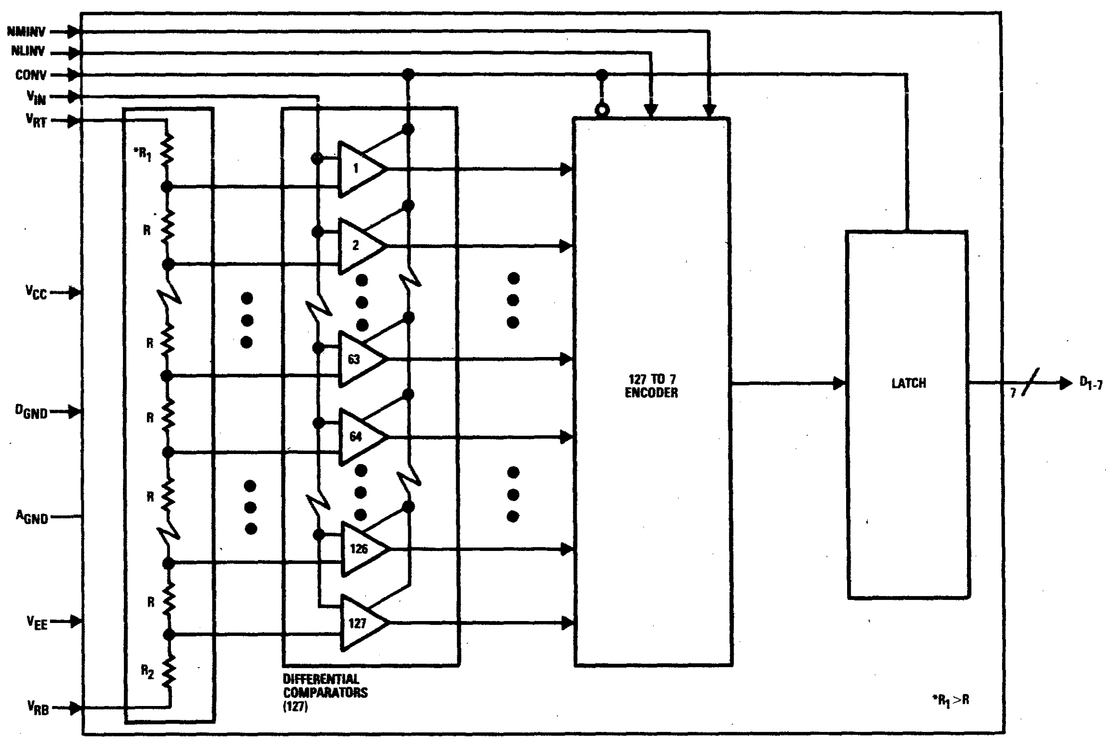
Features

- 7-Bit Resolution
- ½ LSB Linearity
- Sample-And-Hold Circuit Not Required
- TTL Compatible
- 18 MSPS Conversion Rate
- Selectable Output Format
- Available in 24 Lead DIP

Applications

- Low-Cost Video Digitizing
- Medical Imaging
- Data Acquisition
- TV Special Effects
- Video Simulators
- Radar Data Conversion

Functional Block Diagram



LSI Products Division
TRW Electronic Components Group
P.O. Box 2472
La Jolla, Ca. 92038

Phone: (619) 457-1000
Telex: 697-957
TWX: 910-335-1571

40G00283 Rev. C- 9/83
Printed in the U.S.A.

TDC1029
Preliminary Information

TRW

Monolithic A/D Converter
6 bit, 100 MSPS

The TRW TDC1029 is a 100 MegaSample Per Second (MSPS) full-parallel (flash) analog-to-digital converter, capable of converting an analog signal with full power frequency components up to 50 MHz into 6-bit digital words. A sample-and-hold circuit is not necessary. All digital inputs and outputs are ECL compatible.

The TDC1029 consists of 63 clocked latching comparators, combining logic, and an output buffer register. A single differential convert signal controls the conversion operation. The digital outputs are single-ended ECL with the exception of the MSB which is differential. Binary or offset two's complement output format is available.

Features

- 6-Bit Resolution
- 100 MSPS Conversion Rate
- 50 MHz Input Bandwidth
- Low Cost
- 1/2 LSB Linearity
- Sample-And-Hold Circuit Not Required
- 1V Input Range
- Aperture Error < 50 psec
- Binary Or Two's Complement Output Format
- Available In 24 Lead DIP

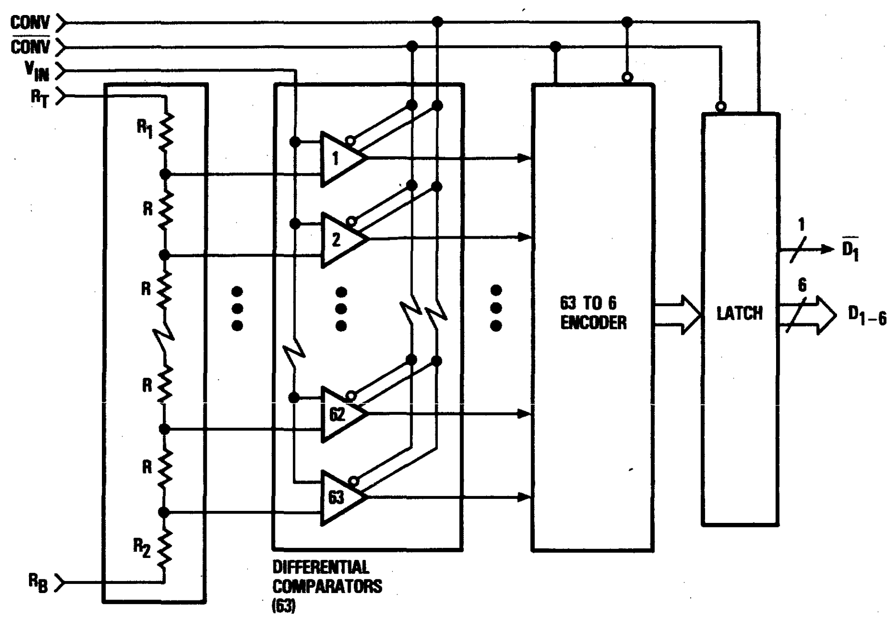
Applications

- Transient Digitizers
- Direct Digital Receivers
- Radar Data Conversion
- Data Acquisition
- Telecommunications
- Medical Imaging

LINEAR

TRW LSI Products

Functional Block Diagram



LSI Products Division
TRW Electronic Components Group
P.O. Box 2472
La Jolla, CA 92038

Phone: (619) 457-1000
Telex: 697-957
TWX: 910-335-1571

40G01198 Rev. B-6/83
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UNITRODE

TYPE	Voltage Reference ± 4%	Voltage Reference ± 1%	Soft Start	PWM Latch	Under-Voltage Lockout	Pulse-by-Pulse Current Limiting	Shutdown Terminal	Output Current	Feed Forward	Maximum Frequency Oscillator	Dual Uncommitted Outputs	Single-Ended Output	Totem Pole Outputs	Separate Oscillator Sync Terminal	Adjustable Deadtime Control	Latch Off or Continuous Retry Mode	Double Pulse Suppression	Low Current Start Up
Regulating PWMs UC1524 UC1524/883B	X						X	100mA		300kHz	X							
Advanced Regulating PWMs UC1524A UC1524A/883B		X		X	X	X	X	200mA		500kHz	X						X	
Advanced Regulating PWMs UC1525A UC1525A/883B		X	X	X	X		X	100mA 0.4A Pulse		500kHz			X	X	X			
Advanced Regulating PWMs UC1527A UC1527A/883B		X	X	X	X		X	100mA 0.4A Pulse		500kHz			X	X	X			
Advanced Regulating PWMs UC1526 UC1526/883B		X	X	X	X	X	X	100mA		400kHz			X	X	X		X	
Regulating PWMs UC493/UC494/UC495		X						200mA		300kHz	X				X		X	
Advanced Regulating PWMs UC493A/UC494A/UC495A* UC493AC/UC494AC/UC495AC*		X			X			200mA		300kHz	X				X		X	
Current Mode PWM Controllers UC1846 UC1846/883B		X	X	X	X	X	X	200mA	X	500kHz			X	X	X	X	X	
Current Mode PWM Controllers UC1847 UC1847/883B		X	X	X	X	X	X	200mA	X	500kHz			X	X	X	X	X	
Programmable Primary Side PWMs UC1840 UC1840/883B		X	X	X	X	X	X	200mA	X	500kHz		X			X	X	N/A	X
Programmable Primary Side PWMs UC1842 UC1842/883B		X		X	X	X		100mA 1A Pulse	X	500kHz		X			X		N/A	X

*Series available with 883B screening.

LINEAR

Unitrode

Power Supply Support Functions

UNITRODE

TYPE	DESCRIPTION	KEY FEATURES	PACKAGE
UC1543/2543/3543 UC1544/2544/3544	Power Supply Supervisory Circuit, Monitors and Controls Power Supply Output	• Over/Under-Voltage, and Current Sensing Circuits • Programmable Time Delays • SCR "Crowbar" Drive of 300mA • Optional Over-Voltage Latch • Internal 1% Accurate Reference • Remote Activation Capability • Uncommitted Comparator • Inputs for Low Voltage Sensing (UC1544 series only)	16 Pin DIL (1543 Series) 18 PIN DIL (1544 series)
UC1706/2706/3706	Dual High Current MOSFET Compatible Output Driver	• Dual, 1.5A, Totem Pole Outputs • Parallel or Push-Pull Operations • Single-Ended to Push-Pull Conversion • Internal Overlap Protection • Analog, Latched Shutdown • High-Speed, Power MOSFET Compatible • Thermal Shutdown Protection • 5 to 40V Operation • Low Quiescent Current	16 Pin DIL
UC1834/2834/3834	High Efficiency Linear Regulator, Low Input-Output Differential	• Minimum V_{IN}—V_{OUT} less than 0.5V at 5A Load with External Pass Device • Equally Usable for either Positive or Negative Regulator Design • Adjustable Low Threshold Current Sense Amplifier • Under- and Over-Voltage Fault Alert with Programmable Delay • Over-Voltage Fault Latch with 100mA Crowbar Drive Output	16 Pin DIL
UC1901/2901/3901	Isolated Feedback Generator Stable and Reliable Alternative to an Optical Coupler	• An Amplitude-Modulation System for Transformer Coupling an Isolated Feedback Error Signal • Internal 1% Reference and Error Amplifier • Loop Status Monitor • Low-Cost Alternative to Optical Couplers • Internal Carrier Oscillator Usable to 5MHz • Modulator Synchronizable to an External Clock	14 Pin DIL
UC1903/2903/3903	Quad Supply and Line Monitor Precision System	• Monitor Four Power Supply Output Voltage Levels • Both Over- and Under-Voltage Indicators • Internal Inverter for Negative Level Sense • Adjustable Fault Window • Additional Input for Early Line Fault Sense • On Chip, High-Current General Purpose OP-AMP	18 Pin DIL

Motor Control Circuits

TYPE	DESCRIPTION	KEY FEATURES	PACKAGE
UC1637/2637/3637	Switched Mode Controller for DC Motor Drive	• Single or Dual Supply Operation • ± 2.5V to ± 20V Input Supply Range • ± 5% Initial Oscillator Accuracy; ± 10% Over Temperature • Pulse-by-Pulse Current Limiting • Under-Voltage Lockout • Uncommitted PWM Comparators for Design Flexibility	18 Pin DIL
UC3717	Stepper Motor Drive Circuit	• Half-Step and Full-Step Mode • Bipolar Constant Current Motor Drive • Built-In Protection Diodes • Wide Range of Current Control 5-1000mA • Wide Voltage Range 10-45V • Designed for Unregulated Motor Supply Voltage • Thermal Overload Protection	16 Pin DIL

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UNITRODE

Three Terminal Voltage Regulators, Adjustable

TYPE	OUTPUT CURRENT (A)	POLARITY	REGULATED OUTPUT VOLTAGE (V)	PACKAGE
UC117K/LM117K UC217K/LM217K *UC317K/LM317K	1.5A	Pos.	Adjustable from 1.2V to 37V	TO-3 TO-3 TO-3
UC137K/LM137K UC237K/LM237K *UC337K/LM337K	1.5A	Neg.	Adjustable from −1.2V to −37V	TO-3 TO-3 TO-3
UC150K/LM150K UC250K/LM250K *UC350K/LM350K	3.0A	Pos.	Adjustable from 1.2V to 33V	TO-3 TO-3 TO-3

Three Terminal Voltage Regulators, Fixed, Positive

TYPE	OUTPUT CURRENT (A)	POLARITY	REGULATED OUTPUT VOLTAGE (V)			PACKAGE
UC7800AK/LM140AK SERIES *UC7800ACK/LM340AK SERIES	1.5A	Pos.	5V ± 1%	12V ± 1%	15V ± 1%	TO-3 TO-3
UC7800K/LM140K SERIES *UC7800CK/LM340K SERIES	1.5A	Pos.	5V ± 4%	12V ± 4%	15V ± 4%	TO-3 TO-3

LINEAR

Three Terminal Voltage Regulators, Fixed, Negative

TYPE	OUTPUT CURRENT (A)	POLARITY	REGULATED OUTPUT VOLTAGE (V)			PACKAGE
UC7900AK/LM120K SERIES *UC7900ACK SERIES	1.5A	Neg.	−5V ± 1%	−12V ± 1%	−15V ± 1%	TO-3 TO-3
UC7900K SERIES *UC7900CK/LM320K SERIES	1.5A	Neg.	−5V ± 4%	−12V ± 4%	−15V ± 4%	TO-3 TO-3

* Also available in TO-220 package.

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INTRODUCTION TO MEMORY

The Master Selection Guide provides sufficient information for making initial product selections. All devices that appear in this section, both in the initial selection guide and the data pages, are included in the indexes. These index listings lead to the page and line on that page where each device appears.

The Memory Section provides initial selection information and data on PROMs, RAMs, and ROMs as well as other memory devices. In these particular sections, the devices are characterized by organization (words and bits/word) and by access times. In order to assure that the access times are comparable, whenever possible the values have been shown in nanoseconds over the full rated temperature range for the devices (i.e., 0° to 70°C for commercial units and −55°C to 125°C for military units). The full temperature nanosecond value is marked "nsF." When this value isn't specified, the guaranteed nanosecond value at room temperature is listed followed by "nsR." In some cases a guaranteed value has not been established; then the typical value is shown followed by "ns*". "Typical" values are invariably much faster than the guaranteed ones so that such listings place these memories higher on the list than they otherwise would appear.

CATEGORY

Detailed Product Information provided by:

The manufacturers listed above have provided detailed information on their latest and most significant products.

EINFÜHRUNG SPEICHER

Der Master Selection Guide für Speicher enthält alle Informationen, die Sie für die Erstauswahl Ihres Produkts benötigen. Die Bauteile, die in diesem Abschnitt erscheinen, sowohl im Selection Guide als auch auf den Datenblättern, sind in allen Master Indexes enthalten. Diese Register verweisen auf die Seite und Zeile, auf der das entsprechende Bauelement vorkommt.

Der Speicherteil bestert aus einem Selection Guide und Daten über PROMs, RAMs und ROMs sowie andere Speicher-Bauteile. In diesen einzelnen Abschnitten sind die Bauteile nach Organisation (Worte und Bits/Wort) und nach Zugriffszeiten eingeteilt. Um sicherzustellen, daß die Zugriffszeiten verglichbar sind, wurden die Werte nach Möglichkeit in Nanosekunden für de vollen zugfelassenen Temperaturbereich (d.h. 0° bis 70°C für kommerzielle Bauteile und —55° bis 125°C für militärische Bauteile) angegeben. Der nsec-Wert für den vollen Temperaturbereich ist mit "nsF" bezeichnet. Wenn dieser Wert nicht genannt ist, so ist der garantierte nsec-Wert bei Raumtemperatur mit "nsR" angegeben. In einigen Fällen wurde ein garantierter Wert nicht festgelegt. Dann wird der typische Wert mit einem nachfolgenden "ns*" markiert. "Typische" Werte sind durchwegs schneller als garantierte, so daß solche Eintragungen die Speicher weiter oben in der Liste erscheinen lassen als dies sonst der Fall wäre.

INTRODUCTION AUX MEMOIRES

Le Guide Général de Sélection fournit suffisamment de renseignements pour permettre des sélections initiales de produits. Tous les apareils énumérés dans cette section, tant dans le Premier Guide de Sélection que dans les feuilles de données, sont inclus dans tous les index. Ces index vous procurent la possibilité de retrouver à quelle page et à quelle ligne tel ou tel appareil a été mentionné.

La Section "Mémoires" contient des données et des renseignements de sélection initiale sur les PROMs, les RAMs et les ROMs, ainsi que sur d'autres appareils mémoires. Dans ces sous-sections, les appareils sont distingués par définition (mots et bit/mot) et par temps d'acces. Afin d'être sûr que les temps d'accès soient comparables, chaque fois que cela a été possible, les valeurs ont été indiquées en nanosecondes pour toute la fourchette de température (exemple: 0° à 70° pour les produits industriels, et —55°C à 125°C pour les produits militaires). La valeur entière de température en nanosecondes est désignée par "nsf". Lorsque cette valeur n'est pas donnée, une valeur garantie à température ambiante, exprimée en nanosecondes, est suivie par "nsR". Dans certains cas aucune valeur garantie en nanosecondes n'a pu être établie, la valeur "typique" est alors traduite par "ns". Les valeurs "typiques" sont invariablement beaucoup plus rapides que celles dites "garanties", de sorte que ces mémoires "typiques" apparaissent plus haut sur la liste qu'elles ne le seraient sur d'autres.

INTRODUCCIÓN A MEMORIA

La Guía Maestra de Selección provee suficiente información para hacer selecciones iniciales del producto. Todas las componentes que aparecen en esta sección, ya sea en la guía de selección inicial o en las páginas de datos, están incluídas en todos los otros índices. Estas listas de índices los conduce a la página y linea de aquella página donde se encuentra cada componente.

La Sección de Memoria provee información para la selección inicial y datos de PROMs, RAMs, and ROMs así como otras piezas de memoria. En estas secciones en particular, las componentes se caracterizan por organización (palabras y bits/palabras) y por tiempo de acceso. Con objeto de asegurar que los tiempos de acceso son comparables, cuando es posible, los valores aparecen en nanosegundos sobre el intérvalo completo de temperature para las componentes (en otras palabras, 0° to 70°C para piezas de uso comercial y —55° a 125°C para piezas de uso militar). El valor del intérvalo completo de temperatura esta marcado "nsF". Cuando este valor no está especificado, el valor de nanosegundon está garantizado para temperatura ambiental y aparece seguido por "nsR". En algunos casos el valor no ha sido establecido; entonces el valor tipico aparece seguido por "ns*". Valores "típocos" son sin falta más rápido que los garantizados de tal manera que las listas ubica estas memorias antes que normalmente los mostraría.

メモリーへの案内

マスターセレクションガイドは選択に取りかかる充分な資料を揃えています。セレクションガイド，データ掲載ページにのっている製品は全てのインデックスに入っており，そのインデックスによりページ数，行数はすぐ見つけられます。

このセクションにはPROM，RAM，ROM他のメモリーのデーターが入っています。製品はその構成（ワード，ビット／ワード）とアクセスタイム毎に分類されています。アクセスタイムが同等であるかどうか確認する為可能な限り夫々の全温度範囲（一般0℃～70℃；ミリタリ－55℃～125℃）でのアクセスタイムをナノセカンドで表示しています。全温度範囲でのアクセスタイムは"nsF"と表示，規定されていないものすなわち室温での保証値は"nsR"となっています。保証値が決められていない場合は代表的値として"ns★"がついています。"Typical"値は通常保証値よりも速くつけられるのでリスト上では他に記載されているものより高い場所に記載されています。

MEMORY–Character Generators

Format	Number of Output Lines	Input Logic levels	Supply Voltage, V	Device	Source	
Character Generators						
5x7	1	TTL	5	DM76S128	† National	
				DM76S64	† National	
				DM8678	National	
				DM86S128	National	
				DM86S64	National	
	5	MOS	5	MM52116FDW	National	
		TTL	5	R03-2513	GI	
				5055	MMI	
				5155	MMI	
				6055	MMI	
				6155	MMI	
				MCM6670	**Motorola**	**(4048)**
				MCM6674	**Motorola**	**(4048)**
			−12,5	3258	Fairchild	
				32581	Fairchild	
				32582	Fairchild	
	7	TTL	5	6056	MMI	
				6061	MMI	
				6062	MMI	
				6156	MMI	
				6161	MMI	
				6162	MMI	
			−12,5	3257	Fairchild	
	35	TTL	5	**MSL9650**	**OKI**	**(4118)**
6x10	7	MOS	5	MCH-01	Motorola	
7x9	1	TTL	5	DM76S128	† National	
				DM76S64	† National	
				DM8678	National	
				DM86S128	National	
				DM86S64	National	
	7	MOS	5	MM52116FDX	National	
		TTL	5	5290	† MMI	
				5291	† MMI	
				6071	MMI	
				6072	MMI	
				6171	MMI	
				6172	MMI	
				6290	MMI	
				6291	MMI	
				MCM66700	**Motorola**	**(4048)**
				MCM66710	**Motorola**	**(4048)**
				MCM66714	**Motorola**	**(4048)**
				MCM66720	**Motorola**	**(4048)**
				MCM66730	**Motorola**	**(4048)**
				MCM66734	**Motorola**	**(4048)**
				MCM66740	**Motorola**	**(4048)**
				MCM66750	**Motorola**	**(4048)**
				MCM66751	Motorola	
				MCM66760	**Motorola**	**(4048)**
				MCM66770	**Motorola**	**(4048)**
				MCM66780	**Motorola**	**(4048)**
				MCM66790	**Motorola**	**(4048)**
			−12,5	3260	Fairchild	
7x11	1	TTL	5	CRT7004	SMC	
				CRT8002	SMC	
9x9	9	TTL	5	5292	† MMI	
				5293	† MMI	
				6292	MMI	
				6293	MMI	
10x9	10	TTL	5	**SCN2670**	**Signetics**	**(1677)**
14 Segments	14	TTL	5	**MSL9664**	**OKI**	**(4118)**
				MSL9665	**OKI**	**(4118)**
16 Segments	16	TTL	5	**MSL9662**	**OKI**	**(4118)**
				MSL9663	**OKI**	**(4118)**

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY–Code Converters

Code Conversion From To	Bits In	Bits Out	Process	Supply Voltage, V	Device	Source	
Code Converters							
BINARY-BCD	6	6	Bipolar	5	**SN54185A**	† TI	(988)
					SN74185A	TI	(988)
Degree-Sine					**5086**	† MMI	(819)
					5087	† MMI	(819)
					6086	MMI	(819)
					6087	MMI	(819)
EBCDIC-ASCII	12	8	Bipolar	5	DM8576AAA	National	
Multiple ASCII-SELECTRIC, EBCID, HOLLERITH			NMOS	±5	MCM68316	Motorola	
					MCM68A316E-81	**Motorola**	(4048)
Binary-BCD	9	7	Bipolar	5	**SN54S485**	† TI	(1043)
					SN74S485	TI	(1043)
BCD-BINARY	6	6	Bipolar	5	**SN54184**	† TI	(987)
					SN74184	TI	(987)
BCD-Binary	7	9	Bipolar	5	**SN54S484**	† TI	(1043)
					SN74S484	TI	(1043)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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Master Selection Guide

MEMORY

MEMORY–FIFOs, LIFOs

First-in First-out

Words	Bits/ Word	Data Rate MHz (max)	Supply Voltage, V	Device	Source	
16	4	8.0*	3-15	CD40105B	† RCA	(838)
				CD40105BE	RCA	(838)
		10.0	5	54F403	† Fairchild	(743)
				74F403	Fairchild	(743)
				N9403	Signetics	(1660)
		12.0	5	SN54LS222	† TI	(995)
				SN54LS224	† TI	(995)
				SN74LS222	TI	(995)
				SN74LS224	TI	(995)
		20.0	5	SN54LS227	† TI	(997)
				SN54LS228	† TI	(997)
				SN74LS227	TI	(997)
				SN74LS228	TI	(997)
	5	10.0	5	SN74S225	TI	(996)
24	4	2.5	5-16	MS618	† RTC	
32	8	0.5	−12,5	AM2812C	AMD	
				AM2812L	AMD	
				MJ2812	Plessey	
				MJ2814	† Plessey	
		1.0	−12,5	AM2812AC	AMD	
				AM2812AL	AMD	
	9	0.5	−12,5	AM2813C	AMD	
				AM2813L	AMD	
				MJ2813	Plessey	
		1.0	−12,5	AM2813AC	AMD	
				AM2813AL	AMD	
40	9	0.5	−12,5	FR1502-11	Western	
		1.0	−12,5	33512	Fairchild	
				3351M	† Fairchild	
				FR1502-10	Western	
		1.5	−12,5	3351-3	Fairchild	
		2.0	−12,5	33511	Fairchild	
64	4	0.7	−12,5	AM3341C	AMD	
				3341	Fairchild	
				3341M	† Fairchild	
		1.0	−12,5	AM2841C	AMD	
				AM2841M	† AMD	
				3341A	Fairchild	
				MJ2841	Plessey	
		1.2	−12,5	AM2841A	AMD	
		7.0	5	C57401	† MMI	(805)
		8.0	5	9423C	Fairchild	
				9423M	† Fairchild	
		10	5	DM77S401	† National	
				DM87S401	National	
		10.0	5	54F413	† Fairchild	(750)
				54F433	† Fairchild	(743)
				74F413	Fairchild	(750)
				74F433	Fairchild	(743)
				C57401A	† MMI	(805)
				C67401	MMI	(805)
		15	5	DM77S401A	† National	
				DM87S401A	National	
		15.0	5	C67401A	MMI	(805)
		16.7	5	C67401B	MMI	(805)
	5	7.0	5	C57402	† MMI	(805)
		10	5	DM77S402	† National	
				DM87S402	National	
		10.0	5	C57402A	† MMI	(805)
				C67402	MMI	(805)
		15	5	DM77S402A	National	
				DM87S402A	National	
		16.7	5	C67402B	MMI	(805)
	9	15.0	5	TDC1030	TRW-LSI	(1161)
132/128	9	0.65	5	WD1510-00	Western	
	-	1.0	5	WD1510-01	Western	
512	9	4.2	5	MK4501-20	Mostek	
		5.7	5	MK4501-15	Mostek	
		7.1	5	MK4501-12	Mostek	

Last-in First-out

Words	Bits/ Word	Data Rate MHz (max)	Supply Voltage, V	Device	Source
81	4	1.0	5	SR5018	SMC
132/128	9	1.0	5	WD1510-02	Western
133	4	1.0	5	SR5017	SMC

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–E² PROMs

E² PROMs

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source
16x16	—	E²	Serial	8	5	**COP494**	**National (4067)**
						NMC9306	**National (4067)**
		NVRAM	Serial	8	5	**X2444**	**Xicor (4265,4267)**
	160 nsF	E²	Serial	14	5	NCR52801	NCR
21x16	10 nsF	EA	Serial	8	−20,10	NCR7033	NCR
32x8	450 nsF	E²	TS	18	5	HNVM3300	† Hughes
32x16	1 μsF	EA	TS	28	−28,5	ER2051	GI
	2 μsF	EA	TS	28	−28,5	ER2051HR	† GI
	4 μsF	EA	TS	28	−29,5	NCR2051	NCR
						NC7051	Nitron
32x32	15 μsF	E²	Serial	14	5	MCM2802	Motorola
50x14	1000 nsF	EA			−30,5	ER1451	GI
64x4	10 μsF	EA	TS	18	6.5,−10,−33	MN1208	Panasonic
	300 nsF	NVRAM	TS	18	5	NCR52210	NCR
						X2210	**Xicor (4266)**
						X2210M	**Xicor (4266)**
	450 nsF	E²	TS	16	5	SY2801A	Synertek
64x8	4 μsF	EA	TS	22	−29,5	ER2055	GI
						NCR2055	NCR
						NC7055	Nitron
	300 nsF	NVRAM	TS	18	5	HNVM3500	† Hughes
64x16	450 nsF	E²	TS	16	5	**COP495**	**National (4068)**
						NMC9346	**National (4068)**
82x1	100 μsF	EA	TS	18	−30,5	ER0082	GI
100x14	2100 nsF	EA	Serial	14	−35	NCR1400	NCR
	3400 nsF	EA	Serial	14	−35	ER1400	GI
						NCR1400	NCR
100x50	3400 nsF	EA	Serial	14	30,5	ER1451	GI
128x4	300 nsF	NVRAM	TS	24	5	NCR52211	NCR
128x8	100 nsF	E²	TS	24	5	ER5901	GI
						ER5901HR	† GI
	300 nsF	NVRAM	TS	24	5	NCR52001	NCR
256x4	300 nsF	NVRAM	TS	18	5	NCR52212	NCR
						X2212	**Xicor (547,4266)**
						X2212DM	**† Xicor (547,4266)**
256x8	110 nsF	E²	TS	18	5	SY2802E	Synertek
	300 nsF	NVRAM	TS	24	5	NCR52002	NCR
512x8	200 nsF	NVRAM	TS	28	5	**2004-2**	**Intel (4023)**
	250 nsF	NVRAM	TS	28	5	**2004**	**Intel (4023)**
	300 nsF	E²	TS	24	5	**X2804A**	**Xicor (4267,4268)**
		NVRAM	TS	24	5	NCR52004	NCR
				28	5	**2004-3**	**Intel (4023)**
	450 nsF	E²	TS	24	5	**X2804A-45**	**Xicor (4267,4268)**
						X2804AM-45	**† Xicor (4267,4268)**
	650 nsF	E²	TS	24	5	HNVM3004	Hughes
	5000 nsF	EA	TS	22	−29,5	NCR2055	NCR
1024x8	650 nsF	E²	TS	24	5	HNVM3008	Hughes
						HNVM3108	† Hughes
						HNVM3708	Hughes
1024x1	300 nsF	NVRAM	TS	18	5	NCR52201	NCR
						X2201A	**Xicor (4266)**
						X2201ADM	**† Xicor (4266)**
1024x4	900 nsF	EA	TS	22	−30,−12,5	ER3400	GI
						NCR3400	NCR
						NC7451	Nitron
2048x4	1600 nsF	EA	TS	24	−24,−14,5	ER2810	GI
						ER2810HR	† GI
2048x8	200 nsF	E²	TS	24	5,21	**52B13-200**	**SEEQ (516,4133)**
						52B13H-200	**SEEQ (516,4133)**
				28	5	NMC9817-20	National
	250 nsF	E²	TS	24	5	XL2816A-250	EXEL
						2815	Intel
						2816	Intel
						2816A	Intel
						M2816A	† Intel
						NMC2816-25	National
						NMC2816E-25	National
						NMC9716-25	**National (4069)**
						5213-250	SEEQ
						5213H-250	SEEQ
						52B13H-250	**SEEQ (516,4133)**
						SY2816	Synertek
					5,21	**52B13-250**	**SEEQ (516,4133)**
				28	5	**2817**	**Intel (4024)**
						NMC9817-25	National
						MSM2816	OKI
	300 nsF	E²	TS	24	5	XLS2816A	EXEL
						HN48016	Hitachi
						M52B13H-300	**† SEEQ (516)**
						X2816A	**Xicor (547,4267,4268)**
						X2816AM	**† Xicor (547,4267,4268)**
					5,21	**M52B13-300**	**† SEEQ (516)**
	350 nsF	E²	TS	24	5	XLS2816A-350	EXEL
						2815-3	Intel
						2816-3	Intel
						2816A-3	Intel
						NMC2816-35	National
						NMC2816E-35	National
						NMC9716-35	**National (4069)**
						5213-350	SEEQ
						5213H-350	SEEQ
						M5213-350	† SEEQ
						X2816A-45	Xicor (4267,4268)
					5,21	**52B13-350**	**SEEQ (516,4133)**
						52B13H-350	**SEEQ (516,4133)**
				28	5	**2817-3**	**Intel (4024)**
						NMC9817-35	National
	450 nsF	E²	TS	24	5	2815-4	Intel
						2816-4	Intel
						2816A-4	Intel
						NMC2816-45	National
						NMC2816E-45	National
						NMC9716-45	**National (4069)**
						X2816A-35	Xicor (4267,4268)
				28	5	**2817-4**	**Intel (4024)**
						M2817	† Intel
4096x8	150 nsF	E²	TS	28	5	MCM2832	Motorola
	200 nsF	E²	TS	28	5	5223-200	SEEQ
						52B23-200	**SEEQ (4133)**
						52B23H-200	**SEEQ (4133)**
	250 nsF	E²	TS	28	5	M2732A-25	† Intel
						52B23-250	**SEEQ (4133)**
						52B23H-250	**SEEQ (4133)**
	300 nsF	E²	TS	28	5	**52B23-3**	**SEEQ (4133)**
						52B23-300	**SEEQ (4133)**
						52B23H-3	**SEEQ (4133)**
						52B23H-300	**SEEQ (4133)**
	450 nsF	E²	TS	28	5	M2732A-45	† Intel
						NCR52832	NCR

† Military Temperature Range (−55° to 125°C)

* Typical Value

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MEMORY-E² PROMs (Cont'd)

E² PROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source
8192x4	450 nsF	E²	TS	28	5	NCR52864	NCR
8192x8	200 nsF	E²	TS	28	5	XLS2864A-200	EXEL
						52B33-200	SEEQ (4133)
						52B33H-200	SEEQ (4133)
						TMM2764	Toshiba
	250 nsF	E²	TS	28	5	XLS2864A-250	EXEL
						M2764-25	Intel
						52B33-250	SEEQ (4133)
						52B33H-250	SEEQ (4133)
	300 nsF	E²	TS	28	5	XLS2864A-300	EXEL
						52B33-3	SEEQ (4133)
						52B33-300	SEEQ (4133)
						52B33H-3	SEEQ (4133)
						52B33H-300	SEEQ (4133)
	350 nsF	E²	TS	28	5	XLS2864A-350	EXEL
						X2864A	Xicor (4269)
	450 nsF	E²	TS	28	5	M2764-45	Intel
						NMH2864	† National
						NMH2864C	National

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

Master Selection Guide

MEMORY

MEMORY–PROMs

PROMs

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source
1Kx8	55 nsF	NMOS	TS	24	5	MB7132E-W	† Fujitsu
2Kx4	35 nsF	NMOS	TS	20	5	MB7128Y	Fujitsu
	55 nsF	CMOS	TS	20	5	MB7128E-W	† Fujitsu
2Kx8	55 nsF	NMOS	TS	24	5	MB7138E-W	† Fujitsu
4Kx4	35 nsF	NMOS	TS	20	5	MB7152-Y	Fujitsu
	55 nsF	NMOS	TS	20	5	MB7152E-W	† Fujitsu
8Kx8	70 nsF	NMOS	TS	24	5	MB7144E-W	† Fujitsu
16x4	25 nsF	TTL	TS	16	5	DM85S47A	National
	30 nsF	TTL	TS	16	5	DM75S07A	† National
	35 nsF	TTL	OC	16	5	DM85S06	National
			TS	16	5	DM85S07	National
	50 nsF	TTL	OC	16	5	DM75S06	† National
			TS	16	5	DM75S07	† National
32x8	15 nsF	TTL	OC	16	5	DM87S188	National
			TS	16	5	DM87S288	National
	20 nsF	TTL	OC	16	5	DM77S188	† National
			TS	16	5	DM77S288	† National
	20 nsR	ECL	OE	16	−5.2	SN10139	TI
	25 nsF	ECL	OE	16	−5.2	**MCM10139**	**Motorola** (4047)
		TTL	OC	16	5	AM27S18AC	AMD
						63S080	**MMI** (4026)
			TS	16	5	AM27S19AC	AMD
						63S081	**MMI** (4026)
	35 nsF	TTL	OC	16	5	AM27S18AM	† AMD
						53S080	† **MMI** (4026)
						DM74S188	**National** (4057)
			TS	16	5	AM27S19AM	† AMD
						53S081	† **MMI** (4026)
						DM74S288	**National** (4057)
	40 nsF	TTL	OC	16	5	AM27S18C	AMD
						TBP18SA30	TI
			TS	16	5	AM27S19C	AMD
						TBP18S030	**TI** (542,4237)
	45 nsF	TTL	OC	16	5	**DM54S188**	† **National** (4057)
			TS	16	5	**DM54S288**	† **National** (4057)
	50 nsF	TTL	OC	16	5	AM27LS18C	AMD
						AM27S18M	† AMD
						HM7602-5	**Harris** (3943)
						6330-1	MMI
						N82S23	Signetics
						TBP18SA030M	† **TI** (542,4237)
			TS	16	5	AM27LS19C	AMD
						AM27S19M	† AMD
						HM7603-5	**Harris** (3943)
						6331-1	MMI
						N82S123	Signetics
						TBP18S030M	† **TI** (542,4237)
	50 nsR	TTL	OC	16	5	SN54188A	† TI
						SN74188A	TI
	60 nsF	TTL	OC	16	5	**HM7602-2**	† **Harris** (3943)
						5330-1	† MMI
			TS	16	5	**HM7603-2**	† **Harris** (3943)
						5331-1	† MMI
	65 nsF	TTL	—	16	5	IM5610C	Intersil
			OC	16	5	IM5600C	Intersil
						S82S23	† **Signetics** (532)
			TS	16	5	AM27LS19M	† AMD
						S82S123	† **Signetics** (532)
	75 nsF	TTL	—	16	5	IM5610M	† Intersil
64x8	75 nsR	TTL	OC	24	5	SN74186	TI

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source
256x4	10 nsF	ECL	OE	16	−5.2	F10Z416A	Fairchild
	11 ns *	ECL	OE	16	−5.2	F10416C	Fairchild
	12 ns *	ECL	OE	16	−5.2	GXB1049	Siemens
	15 nsF	ECL	OE	16	−5.2	F100Z416	Fairchild
						F10Z416	Fairchild
	20 nsR	ECL	OE	16	−5.2	**10149**	**Signetics** (858)
	24 nsF	ECL	OE	16	−4.5	F100416C	Fairchild
	25 nsF	ECL	OE	16	−5.2	**MCM10149**	**Motorola** (4047)
	30 nsF	TTL	OC	16	5	AM27S20AC	AMD
			TS	16	5	AM27S21AC	AMD
	35 nsF	TTL	OC	16	5	**HM7610B-5**	**Harris** (3944)
			TS	16	5	**HM7611B-5**	**Harris** (3944)
	40 nsF	TTL	OC	16	5	AM27S20AM	† AMD
						HM7620B-5	**Harris** (3945)
			TS	16	5	AM27S21AM	† AMD
						HM7621B-5	**Harris** (3945)
	45 nsF	TTL	OC	16	5	AM27S20C	AMD
						HM7610A-5	**Harris** (3944)
						63S140	**MMI** (4026)
			TS	16	5	AM27S21C	AMD
						HM7611A-5	**Harris** (3944)
						63S141	**MMI** (4026)
						29613A	† **Raytheon** (4131)
						29613A	Raytheon
	50 nsF	TTL	OC	16	5	**HM7610B-2**	† **Harris** (3944)
						DM74S387	**National** (4057)
						N82S126	Signetics
			TS	16	5	**HM7611B-2**	† **Harris** (3944)
						DM74S287	**National** (4057)
						N82S129	Signetics
	55 nsF	TTL	OC	16	5	**HM7620B-1**	† **Harris** (3945)
						53S140	† **MMI** (4026)
						6300-1	MMI
						63LS140	MMI
			TS	16	5	**HM7621B-2**	† **Harris** (3945)
						53S141	† **MMI** (4026)
						6301-1	MMI
						63LS141	MMI
						TBP24S10	**TI** (542,4238)
	60 nsF	TTL	OC	16	5	AM27S20M	† AMD
						AM29760AM	AMD
						HM7610-5	**Harris** (3944)
						DM54S387	† **National** (4057)
						29613A	† Raytheon
						29613A	Raytheon
			TS	16	5	AM27S21M	† AMD
						HM7611-5	**Harris** (3944)
						DM54S287	† **National** (4057)
	65 nsF	TTL	OC	16	5	**HM7610A-2**	† **Harris** (3944)
						TBP24SA10	**TI** (542,4238)
						TBP24SA10M	† **TI** (542,4238)
			TS	16	5	**HM7611A-2**	† **Harris** (3944)
						TBP24S10M	† **TI** (542,4238)
	70 nsF	TTL	OC	16	5	IM5603C	Intersil
						S82S126	† **Signetics** (532)
			TS	16	5	IM5623C	Intersil
						S82S129	† **Signetics** (532)
	75 nsF	TTL	OC	16	5	**HM7610-2**	† **Harris** (3944)
						5300-1	† MMI
						53LS140	† MMI
						TBP247A10M	† TI
			TS	16	5	**HM7611-2**	† **Harris** (3944)
						5301-1	† MMI
						53LS141	† MMI
	80 nsF	TTL	OC	16	5	IM5603M	† Intersil
						IM5623M	† Intersil

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY–PROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source
PROMs (Cont'd)							
256x8	1 µs*	Erasable	TS	24	5	CDP18042CD	RCA
	1 µsF	Erasable	TS	24	−9,5	AM1702A	AMD
						AM1702AL	AMD
	1.5 µsF	Erasable	TS	24	−9,5	AM1702A-6	AMD
	2.3 µsF	Erasable	TS	24	−9,5	MM8702A-4	National
	35 nsF	NMOS	OC	20	5	MB7117H	Fujitsu
			TS	20	5	MB7118H	Fujitsu
	45 nsF	NMOS	OC	20	5	MB7117E	Fujitsu
			TS	20	5	MB7118E	Fujitsu
	60 nsF	TTL	TS	20	5	**DM74LS471**	**National** (4057)
	70 nsF	TTL	OC	20	5	6308-1	MMI
						TBP28LA22	**TI** (4240)
				24	5	6335-1	† MMI
			TS	20	5	6309-1	MMI
						DM54LS471	† **National** (4057)
						TBP28L22	**TI** (542,4240)
				24	5	6336-1	MMI
	80 nsF	TTL	OC	20	5	5308-1	† MMI
						TBP28LA22M	† **TI** (4240)
			TS	20	5	5309-1	† MMI
						TBP28L22M	† **TI** (542,4240)
	550 nsF	Erasable	TS	24	−9,5	AM1702A-1	AMD
						AM1702AL-1	AMD
	650 nsF	Erasable	TS	24	−9,5	AM1702A-2	AMD
						AM1702AL-2	AMD
512x4	30 nsF	TTL	OC	16	5	AM27S12AC	AMD
			TS	16	5	AM27S13AC	AMD
	40 nsF	TTL	OC	16	5	AM27S12AM	† AMD
			TS	16	5	AM27S13AM	† AMD
						29611A	**Raytheon** (4131)
	45 nsF	TTL	OC	16	5	**63S240**	**MMI** (4026)
			TS	16	5	**63S241**	**MMI** (4026)
	50 nsF	TTL	OC	16	5	AM27S12C	AMD
						HM7620A-5	**Harris** (3945)
						N82S130	Signetics
			TS	16	5	AM27S13C	AMD
						HM7621A-5	**Harris** (3945)
						MCM7621A	**Motorola** (4047)
						N82S131	Signetics
				24	5	**MCM7641A**	**Motorola** (4047)
	55 nsF	TTL	OC	16	5	**53S240**	† **MMI** (4026)
						DM74S570	**National** (4057)
						DM74S570A	**National** (4057)
			TS	16	5	**53S241**	† **MMI** (4026)
						DM74S571	**National** (4057)
						DM74S571A	**National** (4057)
						DM74S571B	**National** (4057)
						29611	† **Raytheon** (4131)
						29611	Raytheon
	60 nsF	TTL	OC	16	5	AM27S12M	† AMD
						6305-1	MMI
						63LS240	MMI
			TS	16	5	AM27S13M	† AMD
						6306-1	MMI
						63LS241	MMI
						29613C	**Raytheon** (4131)
	65 nsF	TTL	OC	16	5	**DM54S570**	† **National** (4057)
						DM54S570A	† **National** (4057)
			TS	16	5	**DM54S571**	† **National** (4057)
						DM54S571A	† **National** (4057)
						DM54S571B	† **National** (4057)
	70 nsF	TTL	OC	16	5	**HM7620-5**	**Harris** (3945)
						HM7620A-2	† **Harris** (3945)
						S82S130	† **Signetics** (532)

(Continued)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source
512x4	70 nsF	TTL					(Cont'd)
			TS	16	5	**HM7621-5**	**Harris** (3945)
						HM7621A-2	† **Harris** (3945)
						MCM7621	**Motorola** (4047)
						29611	† Raytheon
						29611	Raytheon
						S82S131	† **Signetics** (532)
	75 nsF	TTL	OC	16	5	5305-1	† MMI
						53LS240	† MMI
			TS	16	5	5306-1	† MMI
						53LS241	† MMI
						29613M	† **Raytheon** (4131)
	80 nsF	TTL	—	16	5	IM5624C	Intersil
			OC	16	5	IM5604C	Intersil
	85 nsF	TTL	OC	16	5	**HM7620-2**	† **Harris** (3945)
			TS	16	5	**HM7621-2**	† **Harris** (3945)
	90 nsF	TTL	—	16	5	IM5624M	† Intersil
			OC	16	5	IM5604M	† Intersil
512x8	20 ns*	Reg	TS	24	5	TBP28R45	TI
	20 nsF	Reg	TS	24	5	AM27S25AC	AMD
	25 nsF	Reg	TS	24	5	AM27S25AM	† AMD
	27 nsF	Reg	TS	22	5	AM27S27C	AMD
				24	5	AM27S25C	AMD
	30 nsF	Reg	TS	22	5	AM27S27M	† AMD
				24	5	AM27S25M	† AMD
	35 ns*	TTL	TS	20	5	TBP28P42	TI
				24	5	TBP28P45	TI
						TBP28S45	TI
	35 nsF	TTL	OC	20	5	AM27S28AC	AMD
						MB7123H	Fujitsu
				24	5	AM27S30AC	AMD
			Reg	24	5	**DM87SR25**	**National** (4057)
						DM87SR474	**National** (4057)
						DM87SR476	**National** (4057)
			TS	20	5	AM27S29AC	AMD
						MB7124H	Fujitsu
				24	5	AM27S31AC	AMD
	40 nsF	TTL	Reg	24	5	**DM77SR25**	† **National** (4057)
						DM77SR476	† **National** (4057)
	45 nsF	TTL	OC	20	5	AM27S28AM	† AMD
						MB7123E	Fujitsu
						DM74S473A	**National** (4057)
				24	5	AM27S30AM	† AMD
						HM7640A-5	**Harris** (3946)
						DM74S475A	**National** (4057)
			TS	20	5	AM27S29AM	† AMD
						MB7124E	Fujitsu
						HM7649A-5	**Harris** (3947)
						DM74S472A	**National** (4057)
						DM74S472B	National
						N82S147A	**Signetics** (4174)
				24	5	AM27S31AM	† AMD
						HM7641A-5	**Harris** (3946)
						DM74S474A	**National** (4057)
	50 nsF	TTL	TS	20	5	**MCM7649A**	**Motorola** (4047)
	55 nsF	TTL	OC	20	5	AM27S28C	AMD
				24	5	AM27S30C	AMD
			TS	20	5	AM27S29C	AMD
						6349-2	MMI
				24	5	AM27S31C	AMD
						HM7649A-2	† **Harris** (3947)
						6341-2	MMI
	60 ns*	TTL	TS	20	5	**TBP28L42**	**TI** (542,4241)
				24	5	TBP28L45	TI
	60 nsF	TTL	OC	20	5	**DM54S473A**	† **National** (4057)
						DM74S473	**National** (4057)

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

Master Selection Guide

MEMORY

MEMORY-PROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source
PROMs							**(Cont'd)**
512x8	60 nsF	TTL	OC				(Cont'd)
				24	5	**HM7640A-2**	**† Harris (3946)**
						DM54S475A	**† National (4057)**
			TS	20	5	**HM7649-5**	**Harris (3947)**
						DM54S472	**† National (4057)**
						DM54S472A	**† National (4057)**
						DM54S472B	**† National (4057)**
						DM54S474A	**† National (4057)**
						DM54S474B	**† National (4057)**
						DM74S472	**National (4057)**
						TBP28S42	**TI (542,4244)**
				24	5	AM27S15C	AMD
						HM7641A-2	**† Harris (3946)**
						N82S115	Signetics
						N82S141	Signetics
						TBP28S46	**TI (542,543,4245)**
	65 nsF	TTL	OC	20	5	AM27S28M	† AMD
						DM54S473	**† National (4057)**
						TBP28SA42	**TI (4245)**
				24	5	**DM54S475**	**† National (4057)**
						DM74S475	**National (4057)**
						TBP28SA46	**TI (4245)**
			TS	20	5	AM27S29M	† AMD
				24	5	AM27S31M	† AMD
						DM74S474	**National (4057)**
	70 nsF	TTL	OC	20	5	6348-1	MMI
				24	5	AM27S30M	† AMD
						HM7640-5	**Harris (3946)**
						6340-1	MMI
			TS	20	5	6349-1	MMI
						MCM7649	**Motorola (4047)**
						29623	**Raytheon (4131)**
						TBP28S42M	† TI
						TBP28S42M	TI
				24	5	**HM7641-5**	**Harris (3946)**
						5341-2	† MMI
						6341-1	MMI
						MCM7641	**Motorola (4047)**
						DM54S474	**† National (4057)**
						TBP28S46M	**† TI (542,543,4245)**
	80 nsF	TTL	OC	20	5	5348-1	† MMI
				24	5	5340-1	† MMI
			TS	20	5	**HM7649-2**	**Harris (3947)**
						5349-1	† MMI
				24	5	5341-1	† MMI
	85 nsF	TTL	OC	20	5	**TBP28SA42M**	**† TI (4245)**
				24	5	**HM7640-2**	**† Harris (3946)**
						TBP28SA46M	**† TI (4245)**
			TS	20	5	**TBP28S42M**	**† TI (542,4244)**
						TBP28S42M	TI
				24	5	**HM7641-2**	**† Harris (3946)**
	90 nsF	TTL	OC	24	5	5340-2	† MMI
			TS	24	5	AM27S15M	† AMD
						S82S115	**† Signetics (532)**
						S82S141	**† Signetics (532)**
	200 nsF	CMOS	TS	24	5	**HM6641-2**	**† Harris (3969)**
						HM6641-8	**† Harris (3969)**
						HM6641-9	**Harris (3969)**
	300 nsF	CMOS Erasable					
			TS	24	10	IM6654A	Intersil
		TTL	TS	5		**X2804**	**Xicor (4267,4268)**
							(Continued)
512x8							(Cont'd)
	450 nsF	CMOS Erasable					
			TS	24	5	IM6654-1	Intersil
	550 nsF	CMOS Erasable					
			TS	24	5	IM6654	Intersil
	600 nsF	CMOS Erasable					
			TS	24	5	IM6654M	† Intersil
	35 nsF	TTL	TS	20	5	**DM74S472B**	**National (4057)**
	40 nsF	TTL	Reg	24	5	**DM77SR474**	**† National (4057)**
1024x4	—	Reg	TS	24	5	**AM27S65**	**AMD (3902)**
	30 ns *	TTL	OC	18	5	**DM54S572A**	**† National (4057)**
						DM54S573A	**† National (4057)**
	35 nsF	TTL	OC	18	5	AM27S32AC	AMD
						AM27S33AC	AMD
						MB7121H	Fujitsu
			TS	18	5	AM27S33AC	AMD
						MB7122H	Fujitsu
						63S441A	**MMI (4026)**
						DM74S573B	**National (4057)**
						N82S137B	**Signetics (4172)**
	35 nsR	TTL	OC	18	5	**TBP24SA41**	**TI (4239)**
						TBP24SA41M	**† TI (4239)**
			TS	18	5	**TBP24S41**	**TI (542,4239)**
						TBP24S41M	**† TI (542,4239)**
	40 nsF	TTL	OC	18	5	93452C	Fairchild
			TS	18	5	93453C	Fairchild
	45 nsF	TTL	OC	18	5	AM27S32AM	† AMD
						MB7121E	Fujitsu
						HM7642B-5	**Harris (3948)**
						DM74S572A	**National (4057)**
			TS	18	5	AM27S33AM	† AMD
						MB7122E	Fujitsu
						HM7643B-5	**Harris (3948)**
						63S441	**MMI (4026)**
						DM74S573A	**National (4057)**
				24	5	**DM87S181A**	**National (4057)**
	50 nsF	Reg	TS	18	5	**63RA441**	**MMI (4030)**
		TTL	OC	18	5	**HM7642A-5**	**Harris (3948)**
			TS	18	5	**HM7643A-5**	**Harris (3948)**
						53S441A	**† MMI (4026)**
						MCM7643A	**Motorola (4047)**
						DM54S573B	**† National (4057)**
	55 nsF	TTL	OC	18	5	AM27S32C	AMD
						93452M	† Fairchild
						HM7642B-2	**† Harris (3948)**
						HN25044	Hitachi
			TS	18	5	AM27S33C	AMD
						93453M	† Fairchild
						HM7643B-2	**† Harris (3948)**
						HN25045	Hitachi
						53S441	**† MMI (4026)**
						6353-2	MMI
	60 nsF	Reg	TS	18	5	**53RA441**	**† MMI (4030)**
		TTL	OC	18	5	**HM7642-2**	**† Harris (3948)**
						HM7642-5	**Harris (3948)**
						6350-1	MMI
						6352-1	MMI
						DM74S572	**National (4057)**
			TS	18	5	HM7643-2	† Harris
						HM7643-5	**Harris (3948)**
						6351-1	MMI
						6353-1	MMI
						DM74S573	**National (4057)**
						N82S137	**Signetics (4172)**
	65 nsF	TTL	OC	18	5	AM27S32M	† AMD
			TS	18	5	AM27S33M	† AMD
				24	5	**DM77S181A**	**† National (4057)**
							(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY–PROMs (Cont'd)

PROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source
1024x4 (Cont'd)							
	70 nsF	TTL	OC	18	5	HM7642A-2	† Harris (3948)
			TS	18	5	HM7643A-2	† Harris (3948)
						MCM7643	Motorola (4047)
						S82S137A	† Signetics (532)
	75 nsF	TTL	OC	18	5	5350-1	† MMI
						5352-1	† MMI
						DM54S572	† National (4057)
			TS	18	5	5351-1	† MMI
						5353-1	† MMI
						DM54S573	† National (4057)
	80 nsF	TTL	TS	18	5	S82S137	† Signetics (532)
	85 nsF	TTL	TS	18	5	HM7643-2	† Harris (3948)
	550 nsF	CMOS Erasable	TS	24	5	IM6653-1	Intersil
	600 nsF	CMOS Erasable	TS	24	5	IM6653M	† Intersil
1024x8	—	TTL	TS	24	5	AM27PS181	AMD
						AM27PS281	AMD
						AM27S35AC	AMD (3901)
						AM27S35AM	† AMD (3901)
						AM27S35C	AMD (3901)
						AM27S35M	† AMD (3901)
						AM27S37A	AMD (3901)
	20 ns*	Reg	TS	24	5	TBP28R85	TI
	35 ns*	TTL	TS	24	5	TBP28P85	TI
						TBP28S85	TI (4246)
	35 nsF	TTL	OC	24	5	AM27S180AC	AMD (3905)
						AM27S280AC	AMD (3905)
						AM27S37	AMD (3901)
						93Z450A	Fairchild
						MB71324	Fujitsu
			TS	24	5	AM27S181AC	AMD (3905)
						AM27S281AC	AMD (3905)
						93Z451A	Fairchild
						MB7132Y	Fujitsu
	40 nsF	Reg	TS	24	5	63RS881	MMI
						DM77SR181	† National (4057)
						DM87SR181	National (4057)
	45 nsF	TTL	OC	24	5	93Z450	Fairchild
						MB7131H	Fujitsu
			TS	24	5	93Z451	Fairchild
						MB7132H	Fujitsu
						N82S181B	Signetics (4176)
	50 nsF	TTL	OC	24	5	AM27S180AM	† AMD (3905)
						AM27S280AM	† AMD (3905)
			TS	24	5	AM27S181AM	† AMD (3905)
						AM27S281AM	† AMD (3905)
						HM7681A-5	Harris (3949)
						HN25089S	Hitachi
						82HS181	Intel
						MCM7681A	Motorola (4047)
	55 nsF	TTL	OC	24	5	MB7131E	Fujitsu
						DM87S180	National (4057)
						DM87S280	National (4057)
			TS	24	5	MB7132E	Fujitsu
						82S181	Intel
						53RS881	MMI (4032)
						6381-2	MMI
						DM87S281	National (4057)
						N82S181A	Signetics (4176)
	60 nsF	TTL	OC	24	5	AM27S180C	AMD (3905)
						AM27S280C	AMD (3905)
						93460M	† Fairchild
						SN74S2708	TI

(Continued)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source
1024x8	60 nsF	TTL	OC	24	5	(Cont'd)	
						TBP28S86-60	TI (542,543,4246)
						TBP28SA86-60	TI (4247)
			TS	24	5	AM27S181C	AMD (3905)
						AM27S281C	AMD (3905)
						HM7681A-2	† Harris (3949)
						29631A	† Raytheon (4131)
						29631A	Raytheon
						29633A	† Raytheon (4131)
						29633A	Raytheon
						N82S183	Signetics
	65 ns*	TTL	TS	24	5	TBP28L85	TI
	70 nsF	TTL	OC	24	5	6380-2	MMI
						N82S180	Signetics
			TS	24	5	HM7681-5	Harris (3949)
						5381-2	† MMI
						MCM7681	Motorola (4047)
						DM87S181	National (4057)
						29633A	† Raytheon
						29633A	Raytheon
						N82S181	Signetics
	75 nsF	TTL	OC	24	5	DM77S180	† National (4057)
						DM77S280	† National (4057)
						TBP28SA86M	† TI (4247)
			TS	24	5	DM77S181	† National (4057)
						DM77S281	† National (4057)
						TBP24S86M	† TI
						TBP28S2708	† TI (4248)
	80 ns*	TTL	TS	24	5	TBP28L86	TI (542,543,4242)
						TBP28L86M	† TI (542,543,4242)
	80 nsF	TTL	OC	24	5	AM27S180M	† AMD (3905)
						AM27S280M	† AMD (3905)
			TS	24	5	AM27S181M	† AMD (3905)
						AM27S281M	† AMD (3905)
						S82S181A	† Signetics (532,4176)
	90 nsF	TTL	OC	24	5	5380-2	† MMI
						6380-1	MMI
						S82S180	† Signetics
			TS	24	5	HM7681-2	† Harris (3949)
						6381-1	MMI
						S82S181	† Signetics (532)
						S82S183	† Signetics
						S82S2708	† Signetics (532)
	95 nsF	TTL	TS	24	5	29633C	Raytheon (4131)
	100 nsF	TTL	OC	24	5	HN25088	Hitachi
						HN25089	† Hitachi
			TS	24	5	DM87LS181	National (4057)
	120 nsF	TTL	TS	24	5	DM77LS181	† National (4057)
						N82LS181	Signetics
	125 nsF	TTL	OC	24	5	5380-1	† MMI
			TS	24	5	5381-1	† MMI
	175 nsF	TTL	TS	24	5	S82LS181	† Signetics
	300 nsF	Erasable	TS	24	±5,12	MCM27A08	Motorola
						MCM68A708	Motorola
	350 nsF	Erasable	TS	24	±5,12	AM2708-13	AMD
						F2708-1	Fairchild
						TMS2708-35	TI (543,4234)
	450 nsF	CMOS Erasable	TS	24	5	IM6658	Intel
						IM6658M	† Intel
		Erasable	TS	24	5	MM2758	National
					±5,12	AM2708	AMD
						AM9708	† AMD
						F2708	Fairchild
						F68708	Fairchild
						MCM2708	Motorola

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–PROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Page
PROMs								**(Cont'd)**
1024x8	450 nsF	Erasable	TS	24	±5,12			(Cont'd)
						MCM68708	Motorola	
						INS8708	National	
						TMS2708-45	**TI**	**(543,4234)**
						TMS27L08-45	**TI**	**(543,4234)**
2048x4	—	Reg	TS	24	5	**AM27S75**	**AMD**	**(3902)**
		TTL	TS	20	5	TBP28R165	TI	
	35 nsF	TTL	OC	18	5	AM27S184AC	AMD	
						MB7127Y	Fujitsu	
			TS	18	5	AM27S185AC	AMD	
						MB7128Y	Fujitsu	
						63S841A	**MMI**	**(4026)**
						DM87S185B	**National**	**(4057)**
	45 ns *	TTL	OC	18	5	SN54S455	† TI	
						SN74S455	TI	
						TBP24SA81	**TI**	**(4240)**
						TBP24SA81M	**† TI**	**(4240)**
			TS	18	5	**TBP24S81**	**TI**	**(542,4239)**
						TBP24S81M	**† TI**	**(542,4239)**
	45 nsF	TTL	OC	18	5	AM27S184AM†	AMD	
						MB7127H	Fujitsu	
			TS	18	5	AM27S185AM†	AMD	
						MB7128H	Fujitsu	
						DM87S185A	**National**	**(4057)**
						N82S185B	**Signetics**	**(4178)**
	50 nsF	TTL	OC	18	5	AM27S184C	AMD	
			TS	18	5	AM27S185C	AMD	
						HM7685A-5	**Harris**	**(3950)**
						53S841A	**† MMI**	**(4026)**
						63S841	**MMI**	**(4026)**
						DM77S185B	**† National**	**(4057)**
						N82S185A	**Signetics**	**(4178)**
	55 nsF	TTL	OC	18	5	AM27S184M	† AMD	
						DM87S184	**National**	**(4057)**
			TS	18	5	AM27S185M	† AMD	
						MB7128E	Fujitsu	
						MB7128E-W	† Fujitsu	
						53S841	**† MMI**	**(4026)**
						6389-2	MMI	
						DM87S185	**National**	**(4057)**
	60 nsF	TTL	TS	18	5	AM27LS185C	AMD	
						AM27PS185C	AMD	
						HM7685A-2	**† Harris**	**(3950)**
						DM77S185A	**† National**	**(4057)**
						29651A	**Raytheon**	**(4131)**
						29653A	**Raytheon**	**(4131)**
				24	5	**N82S191A**	**Signetics**	**(4180)**
	65 nsF	TTL	OC	18	5	AM27LS184M†	AMD	
			TS	18	5	AM27LS185M†	AMD	
						AM27PS185M†	AMD	
	70 nsF	TTL	OC	18	5	6388-1	MMI	
						DM77S184	**† National**	**(4057)**
			TS	18	5	**HM7685-5**	**Harris**	**(3950)**
						5389-2	† MMI	
						6389-1	MMI	
						MCM7685	**Motorola**	**(4047)**
						DM77S185	**† National**	**(4057)**
						29651C	**Raytheon**	**(4131)**
	75 nsF	TTL	TS	18	5	**29653C**	**Raytheon**	**(4131)**
	80 nsF	TTL	TS	18	5	**S82S185A**	**Signetics**	**(532,4178)**
				24	5	**S82S191A**	**† Signetics**	**(532,4180)**
	90 nsF	TTL	TS	18	5	**HM7685-2**	**† Harris**	**(3950)**
						29651M	**† Raytheon**	**(4131)**
								(Continued)
2048x4								(Cont'd)
	95 nsF	TTL	TS	18	5	**29653M**	**† Raytheon**	**(4131)**
	100 nsF	TTL	OC	18	5	5388-1	† MMI	
			TS	18	5	5389-1	† MMI	
						N82S185	Signetics	
	115 nsF	TTL	TS	18	5	**S82S185**	**† Signetics**	**(532)**
	450 nsF	CMOS Erasable	TS	24	5	IM6657	Intersil	
						IM6657M	† Intersil	
2048x8	—	TTL	TS	24	5	**AM27S45**	**AMD**	**(3904)**
						AM27S45A	**AMD**	**(3904)**
						AM27S47	**AMD**	**(3904)**
						AM27S47A	**AMD**	**(3904)**
	20 ns *	Reg	TS	24	5	TBP28R166	† TI	
	35 ns *	TTL	OC	24	5	TBP28SA166	TI	
			TS	24	5	TBP28P166	† TI	
						TBP28S166	**TI**	**(4247)**
	35 nsF	Reg	TS	24	5	**63RA1681A**	**MMI**	**(4035)**
						63RS1681A	**MMI**	**(4038)**
						MCM27S45	Motorola	
						MCM27S47	Motorola	
		TTL	OC	24	5	AM27S190AC	AMD	
						AM27S290AC	AMD	
			TS	24	5	AM27S191A	AMD	
						AM27S291A	AMD	
						MB7138YZ	Fujitsu	
						3636B-1	Intel	
						63S1681A	**MMI**	**(4026)**
						MCM27S191	Motorola	
						MCM27S291	Motorola	
						DM87S191B	**National**	**(4057)**
						DM87S291B	**National**	**(4057)**
	40 nsF	Reg	TS	24	5	**53RA1681A**	**† MMI**	**(4035)**
						53RS1681A	**† MMI**	**(4038)**
						63RA1681	**MMI**	**(4035)**
						63RS1681	**MMI**	**(4038)**
	45 nsF	Reg	TS	24	5	**53RA1681**	**† MMI**	**(4035)**
						53RS1681	**† MMI**	**(4038)**
		TTL	OC	24	5	932510C	Fairchild	
						93Z510C	Fairchild	
						MB7137H	Fujitsu	
			TS	24	5	932511C	Fairchild	
						93Z511C	Fairchild	
						MB7138H	Fujitsu	
						3636B-2	Intel	
						DM87S191A	**National**	**(4057)**
						DM87S291A	**National**	**(4057)**
	50 nsF	TTL	OC	24	5	AM27S190C	AMD	
						AM27S290AM†	AMD	
						AM27S290C	AMD	
						HN24084S	Hitachi	
						HN25084S	Hitachi	
						TBP28SA86A-50	**TI**	**(4247)**
			TS	24	5	AM27PS191C	AMD	
						AM27PS291C	AMD	
						AM27S191	AMD	
						AM27S191AM†	AMD	
						AM27S291	AMD	
						AM27S291AM†	AMD	
						HM76161A-5	**Harris**	**(3951)**
						HN25085S	Hitachi	
						3636B	Intel	
						82HS191	Intel	
						53S1681A	**† MMI**	**(4026)**
						63S1681	**MMI**	**(4026)**
						MCM76161A	**Motorola**	**(4047)**
						DM77S191B	**† National**	**(4057)**
						DM77S291B	**† National**	**(4057)**
								(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

Master Selection Guide

MEMORY

MEMORY–PROMs (Cont'd)

Organi-zation	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
PROMs							**(Cont'd)**	
2048x8	50 nsF	TTL	TS	24	5		(Cont'd)	
						29681A	**† Raytheon (4131)**	
						29681A	Raytheon	
						29683A	**† Raytheon (4131)**	
						29683A	Raytheon	
	55 nsF	TTL	OC	24	5	93Z510M	† Fairchild	5
						MB7137E	† Fujitsu	
			TS	18	5	**MCM7685A**	**Motorola (4047)**	
				24	5	93Z511M	† Fairchild	
						MB7138E	Fujitsu	
						MB7138E-W	† Fujitsu	10
	60 nsF	TTL	OC	18	5	HN25084	Hitachi	
				24	5	HN25168S	Hitachi	
			TS	18	5	HN25085	Hitachi	
				24	5	**HM76161-5**	**Harris (3951)**	
						HN25169S	Hitachi	15
						DM77S191A	**† National (4057)**	
						DM77S291A	**† National (4057)**	
	65 nsF	TTL	OC	24	5	AM27S190M	† AMD	
						DM87S190	**National (4057)**	
						DM87S290	**National (4057)**	20
			TS	24	5	AM27PS191M	† AMD	
						AM27PS291AM	† AMD	
						AM27S291M	† AMD	
						53S1681	**† MMI (4026)**	
						DM87S191	**National (4057)**	25
						DM87S291	**National (4057)**	
	70 nsF	TTL	TS	24	5	82S191	Intel	
						MCM76161	**Motorola (4047)**	
						29681A	† Raytheon	
						29681A	Raytheon	30
						29683A	† Raytheon	
						29683A	Raytheon	
	75 ns *	TTL	TS	24	5	**TBP28L166**	**TI (4243)**	
	80 nsF	TTL	OC	24	5	**DM77S190**	**† National (4057)**	
						DM77S290	**† National (4057)**	35
			TS	24	5	**HM76161-2**	**† Harris (3951)**	
						DM77S191	**† National (4057)**	
						DM77S291	**† National (4057)**	
						29681	**Raytheon (4131)**	
						N82S191	Signetics	40
	85 nsF	TTL	TS	24	5	**29683**	**Raytheon (4131)**	
	100 nsF	TTL	TS	24	5	**S82S191**	**† Signetics (532)**	
	120 nsF	CMOS	TS	24	5	**HM6616-8**	**† Harris (3969)**	
	300 nsF	Erasable	TS	24	5	AM9716	AMD	
						MK2716-5	Mostek	45
					±5,12	TMS27A16	Motorola	
		NMOS	TS	24	±5,12	**TMS2716-30**	**TI (4233)**	
		TTL	TS	5		**X2816**	**Xicor (547,4267,4268)**	
	350 nsF	Electrically Erasable	TS	24	5	**X2816A-35**	**Xicor (547,4267,4268)**	
						X2816AM-35	**† Xicor (547,4267,4268)**	50
		Erasable	TS	24	5	AM2716-1	AMD	
						F2716-1	Fairchild	
						2716-1	Intel	
						MK2716-6	Mostek	
						MCM2716-35	Motorola	55
						MCM27L16-35	Motorola	
						MM2716-1	National	
						NMC6716-1	National	
						SY2716-1	Synertek	
						TMM323-1	Toshiba	60
							(Continued)	
2048x8							(Cont'd)	
	390 nsF	Erasable	TS	24	5	AM2716-2	AMD	
						HN462716-2	Hitachi	
						2716-2	Intel	
						MK2716-7	Mostek	
						MM2716-2	National	65
						NMC6716-2	National	
						SY2716-2	Synertek	
	450 nsF	Electrically Erasable	TS	24	5	**X2816A-45**	**Xicor (547,4267,4268)**	
						X2816AM-45	**† Xicor (547,4267,4268)**	
		Erasable	TS	24	5	AM2716	AMD	70
						AM2716M	† AMD	
						F2716	Fairchild	
						F68716	Fairchild	
						HN462716	Hitachi	
						2716	Intel	75
						M2716	Intel	
						M5L2716	Mitsubishi	
						MK2716-8	Mostek	
						MM2716	National	
						NMC2716E	National	80
						NMC27C16-45	National	
						μPD2716	NEC	
						SY2716	Synertek	
					±5,12	**TMS2716-45**	**TI (4233)**	
	490 nsF	Erasable	TS	24	5	2716-5	Intel	85
	550 nsF	Erasable	TS	24	5	NMC27C16-55	National	
	650 nsF	Erasable	TS	24	5	2716-6	Intel	
						MK2716-12	Mostek	
4096x4	—	Reg	TS	24	5	**AM27S85**	**AMD (3902)**	
	35 nsF	TTL	OC	20	5	**AM27S40A**	**AMD (3907)**	90
			TS	20	5	**AM27S41A**	**AMD (3907)**	
						63S1641A	**MMI (4026)**	
						MCM76165	**Motorola (4047)**	
						DM87S195B	National	
						N82HS195	Signetics	95
	40 nsF	Reg	TS	24	5	**63D1641**	**MMI (4041)**	
	45 nsF	Reg	TS	24	5	**53D1641**	**† MMI (4041)**	
		TTL	TS	20	5	DM87S195A	National	
				24	5	MB7134H	Fujitsu	
						MB7152E	Fujitsu	100
	50 nsF	TTL	OC	20	5	**AM27S40**	**AMD (3907)**	
						AM27S40AM	**† AMD (3907)**	
			TS	20	5	AM27PS41	AMD	
						AM27S41	**AMD (3907)**	
						AM27S41AM	**† AMD (3907)**	105
						53S1641A	**† MMI (4026)**	
						63S1641	**MMI (4026)**	
						DM77S195B	**† National (4057)**	
						S82HS195	† Signetics	
	55 nsF	TTL	TS	24	5	MB7134E	Fujitsu	110
						MB7152H	Fujitsu	
	60 nsF	TTL	TS	20	5	**HM76165-5**	**Harris (3952)**	
						DM77S195A	**† National (4057,4057)**	
	65 nsF	TTL	OC	20	5	**AM27S40M**	**† AMD (3907)**	
			TS	20	5	**AM27S41M**	**† AMD (3907)**	115
						53S1641	**† MMI (4026)**	
	80 nsF	TTL	TS	20	5	**HM76165-2**	**† Harris (3952)**	
4096x8	40 nsF	TTL	TS	24	5	**AM27S43A**	**AMD (3908)**	
						3632-1	Intel	
						82HS321	Intel	120
	50 nsF	TTL	TS	24	5	**AM27S43**	**AMD (3908)**	
						3632	Intel	
						82S321	Intel	
							(Continued)	

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–PROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	
PROMs								**(Cont'd)**
4096x8	50 nsF	TTL	TS	24	5			(Cont'd)
						M3632	† Intel	
						M3632	Intel	
	55 nsF	TTL	OC	24	5	MB7141H	Fujitsu	
			TS	24	5	MB7142H	Fujitsu	
						DM87S321	**National**	**(4057)**
						DM87S421	**National**	**(4057)**
	65 nsF	TTL	OC	24	5	MB7141E	Fujitsu	
			TS	24	5	MB7142E	Fujitsu	
						HM76321-5	**Harris**	**(3953)**
						DM77S321	**† National**	**(4057)**
						DM77S421	**† National**	**(4057)**
				28	5	MB7142E-W	† Fujitsu	
	70 nsF	TTL	TS	24	5	**29671A**	**† Raytheon**	**(4131)**
						29671A	Raytheon	
	80 nsF	TTL	TS	24	5	**29671**	**† Raytheon**	**(4131)**
						29671	Raytheon	
						29671A	† Raytheon	
						29671A	Raytheon	
						N82S321	Signetics	
	85 nsF	TTL	TS	24	5	**HM76321-2**	**† Harris**	**(3953)**
						29673	**† Raytheon**	**(4131)**
						29673	Raytheon	
	100 nsF	TTL	TS	24	5	29671	† Raytheon	
						29671	Raytheon	
	105 nsF	TTL	TS	24	5	29673	† Raytheon	
						29673	Raytheon	
	150 nsF	Erasable	TS	24	5	**AM2732A-1**	**AMD**	**(3926)**
						AM2732A-15	**AMD**	**(3926)**
	200 nsF	Erasable	TS	24	5	**AM2732A-2**	**AMD**	**(3926)**
						AM2732A-20	**AMD**	**(3926)**
						MBM2732A-20	Fujitsu	
						HN482732A-20	Hitachi	
						2732A-2	Intel	
						2732A-20	Intel	
	250 nsF	Erasable	TS	24	5	**AM2732A**	**AMD**	**(3926)**
						AM2732A-25	**† AMD**	**(3926)**
						AM2732A-25	AMD	
						MBM2732A-25	Fujitsu	
						HN482732A-25	Hitachi	
						2732A	Intel	
						2732A-25	Intel	
						TMM2732-2	Toshiba	
	300 nsF	Erasable	TS	24	5	**AM2732A-3**	**AMD**	**(3926)**
						AM2732A-30	**AMD**	**(3926)**
						MBM2732A-30	Fujitsu	
						MBM2732A-30X	Fujitsu	
						HN472632A-30	Hitachi	
						HN482732A-30	Hitachi	
						2732A-3	Intel	
						2732A-30	Intel	
		NMOS	TS	24	5	R09433C	GI	
	350 nsF	Erasable	TS	24	5	NMC27C32-35	National	
		NMOS	TS	24	5	M58735	Mitsubishi	
	450 nsF	Erasable	TS	24	5	**AM2732A-4**	**AMD**	**(3926)**
						AM2732A-45	**† AMD**	**(3926)**
						AM2732A-45	AMD	
						F2732	Fairchild	
						HN462532	Hitachi	
						HN462732	Hitachi	
						2732A-4	Intel	
						M5L2732	Mitsubishi	
						NMC27C32-45	National	
						μPD2732	NEC	
						TMM2732	Toshiba	
		NMOS	TS	24	5	R094132	GI	
								(Continued)
4096x8								(Cont'd)
	550 nsF	Erasable	TS	24	5	NMC27C32-55	National	
8192x8	45 nsF	TTL	OC	24	5	93Z564	Fairchild	
			TS	24	5	93Z565	Fairchild	
	55 nsF	TTL	OC	24	5	MB7143H	Fujitsu	
			TS	24	5	MB7144H	Fujitsu	
	85 nsF	TTL	TS	24	5	**HM76641-5**	**Harris**	**(3954)**
	100 nsF	TTL	TS	24	5	**HM76641-2**	**† Harris**	**(3954)**
	175 nsF	CMOS	TS	28	5	**HM6664-2**	**† Harris**	**(3969)**
						HM6664-8	**† Harris**	**(3969)**
						HM6664-9	**Harris**	**(3969)**
	200 nsF	CMOS, Erasable	TS	28	5	**HN27C64-20**	**Hitachi**	**(3974)**
		Erasable	TS	28	5	**AM2764-20**	**AMD**	**(3928)**
						MBM2764-20	Fujitsu	
						HN26C64-20	Hitachi	
						2764-2	Intel	
						5133-2	**SEEQ**	**(513,4137)**
						5133-200	**SEEQ**	**(513,4137)**
						TMM2764-2	Toshiba	
	250 nsF	CMOS, Erasable	TS	28	5	MBM27C64-25	Fujitsu	
						HN27C64-25	**Hitachi**	**(3974)**
		Erasable	TS	28	5	**AM2764-25**	**AMD**	**(3928)**
						2764	Fairchild	
						MBM2764-25	Fujitsu	
						HN482764-3	Hitachi	
						2764	Intel	
						2764-25	Intel	
						5133-250	**SEEQ**	**(513,4137)**
						M5133-250	**† SEEQ**	**(513)**
	300 nsF	CMOS, Erasable	TS	28	5	MBM27C64-30	Fujitsu	
						MBM27C64-30W	† Fujitsu	
						HN27C64-30	**Hitachi**	**(3974)**
		Erasable	TS	28	5	**AM2764-30**	**AMD**	**(3928)**
						MBM2764-30	Fujitsu	
						MBM2764-30X	Fujitsu	
						2764-3	Intel	
						2764-30	Intel	
						5133-3	**SEEQ**	**(513,4137)**
						5133-300	**SEEQ**	**(513,4137)**
	350 nsF	Erasable	TS	24	5	**MCM68766-35**	**Motorola**	**(4047)**
				28	5	**TMS2564-35**	**TI**	**(543,4229)**
	400 nsF	Erasable	TS	28	5	**5133-4**	**SEEQ**	**(513,4137)**
	450 nsF	Erasable	TS	24	5	**MCM68764**	**Motorola**	**(4047)**
						MCM68766	**Motorola**	**(4047)**
				28	5	**AM2764-45**	**AMD**	**(3928)**
						HN482764-4	Hitachi	
						2764-4	Intel	
						2764-45	Intel	
						M5L2764	Mitsubishi	
						MSM2764A	**OKI**	**(4118)**
						5133-450	**SEEQ**	**(513,4137)**
						M5133-450	**† SEEQ**	**(513)**
						TMS2564-45	**TI**	**(543,4229)**
	500 nsF	Erasable	TS	28	5	**TMS2564-50**	**TI**	**(543,4229)**
16384x8	150 nsF	Erasable	TS	28	5	**AM27128-1**	**AMD**	**(3929)**
						AM27128-15	**AMD**	**(3929)**
	200 nsF	Erasable	TS	28	5	**AM27128-2**	**AMD**	**(3929)**
						AM27128-20	**† AMD**	**(3929)**
						AM27128-20	AMD	
						M27128	† Intel	
						5143-2	**SEEQ**	**(513)**
						5143-200	**SEEQ**	**(513)**
	250 nsF	Erasable	OE	28	5	**HN4827128-25**	**Hitachi**	**(3975)**
			TS	28	5	**AM27128**	**AMD**	**(3929)**
								(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY–PROMs (Cont'd)

PROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	
16384x8	250 nsF	Erasable	TS	28	5			(Cont'd)
						AM27128-25	† **AMD**	**(3929)**
						AM27128-25	AMD	
						MBM27128-25	Fujitsu	
						HN4827128-25	Hitachi	
						27128-25	Intel	
						5143-250	**SEEQ**	**(513)**
						M5143-250	† **SEEQ**	**(513)**
	300 nsF	Erasable	OE	28	5	**HN4827128-30**	**Hitachi**	**(3975)**
						27128-30	Intel	
			TS	28	5	**AM27128-3**	**AMD**	**(3929)**
						AM27128-30	**AMD**	**(3929)**
						MBM27128-30	Fujitsu	
						HN4827128-30	Hitachi	
						27128-3	Intel	
						5143-3	**SEEQ**	**(513)**
						5143-300	**SEEQ**	**(513)**
		NMOS	TS	28	5	MBM27128-30W	† Fujitsu	
	450 nsF	Erasable	OE	28	5	**HN4827128-45**	**Hitachi**	**(3975)**
						27128-45	Intel	
						M27128-45	† Intel	
			TS	28	5	**AM27128-4**	**AMD**	**(3929)**
						AM27128-45	† **AMD**	**(3929)**
						AM27128-45	AMD	
						HN4827128-45	Hitachi	
						27128-4	Intel	
						5143-4	**SEEQ**	**(513)**
						5143-450	**SEEQ**	**(513)**
						M5143-450	† **SEEQ**	**(513)**
32768x8	170 nsF	Erasable	TS	28	5	**AM27256-1**	**AMD**	**(3930)**
	200 nsF	CMOS	TS	28	5	MBM27C256-20	Fujitsu	
		Erasable	TS	28	5	**AM27256-2**	**AMD**	**(3930)**
						AM27256-20	**AMD**	**(3930)**
		NMOS	TS	28	5	RO9256D	GI	
	250 nsF	CMOS	TS	28	5	MBM27C256-25	Fujitsu	
		Erasable	TS	28	5	**AM27256**	**AMD**	**(3930)**
						AM27256-25	**AMD**	**(3930)**
						27256	**Intel**	**(4025)**
		NMOS	TS	28	5	RO9256DS	GI	
	300 nsF	CMOS	TS	28	5	MBM27C256-30	Fujitsu	
		Erasable	TS	28	5	**AM27256-3**	**AMD**	**(3930)**
						AM27256-30	**AMD**	**(3930)**
	350 nsF	NMOS	TS	28	5	RO9256CS	GI	
	450 nsF	Erasable	TS	28	5	**AM27256-4**	**AMD**	**(3930)**
						AM27256-45	**AMD**	**(3930)**
		NMOS	TS	28	5	RO9256B	GI	

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

Master Selection Guide

MEMORY

MEMORY-RAMs

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source
Bubble							
Note: Bubble Memory Support Circuits (controllers, function drivers, coil drivers, sense amplifiers), see Interface, Memory and Peripheral Drivers; Interface—Sense Amplifiers; Linear-Other Devices (Volume II).							
1 Megabit (2048x512)				20		7110	Intel
						BPK70	**Intel** (4022)
1 Megabit (4096x256x1)				20		**BPK72**	**Intel** (4021)
						MBM2011A	Motorola
4 Megabit (512x8192)				20		7114	Intel
74032-Bits Serial	370 ms	NMOS	—	18		**FBM31DB**	**FujitsuA** (3940)
83354-Bits Serial	4.5 ms	NMOS	—	18		**FBM32DA**	**FujitsuA** (3940)
262144 (1024x256)						MBM2256	Motorola
273745-Bits Serial	6.0 ms		—	20		**FBM43DA**	**FujitsuA** (3941)
283026-Bits Serial	8.5 ms	NMOS	—	16		**FBM42DA**	**FujitsuA** (3941)
296128-Bits Serial	370 ms	Card				FBC304M1A	FujitsuA
324024-Bits Serial	4.5 ms	Card	—			FBC304D2A	FujitsuA
CCD							
32768-Bits (4096x8x1)			TS	16	±5,12	F232	Fairchild
65535-Bits (4096x16x1)			TS	16	±5,12	F264	Fairchild
Dynamic							
2048x8	50 nsF	NMOS	OC	24	5	μPB409	NEC
			TS	24	5	μPB429	NEC
4096x1	120 nsF	NMOS	TS	16	±5,12	IM7027-1	Intersil
						MK4027-1	Mostek
						MCM4027A-1	Motorola
	135 nsF	NMOS	TS	22	±5,15	μPD411-4	NEC
	150 nsF	NMOS	TS	16	±5,12	MK4027-2	Intersil
						ITT4027-2	ITT
						MK4027-2	Mostek
						MCM4027A-2	Motorola
						M4027-2	SGS
				22	±5,12	μPD411-3	NEC
	200 nsF	NMOS	TS	16	±5,12	IM7027-3	Intersil
						MK4027-3	Intersil
						ITT4027-3	ITT
						MK4027-3	Mostek
						MKB4027-83	Mostek
						MCM4027A-3	Motorola
						M4027-3	SGS
				22	±5,12	μPD411-2	NEC
						μPD411A-2	NEC
	250 nsF	NMOS	TS	16	±5,12	IM7027-4	Intersil
						MK4027-4	Intersil
						ITT4027-4	ITT
						MK4027-4	Mostek
						MKB4027-84	Mostek
						MCM4027A-4	Motorola
						M4027-4	SGS
				22	±5,12	μPD411-1	NEC
						μPD411A-1	NEC
	300 nsF	NMOS	TS	22	±5,12	μPD411	NEC
						μPD411A	NEC
	350 nsF	NMOS	TS	16	±5,12	ITT4027-6	ITT
8192x8	120 nsF	NMOS	TS	28	5	**IMS2630-12**	**Inmos** (3980)
	150 nsF	NMOS	TS	28	5	**IMS2630-15**	**Inmos** (3980)
	200 nsF	NMOS	TS	28	5	**IMS2630-20**	**Inmos** (3980)
	250 nsF	NMOS	TS	28	5	2186-25	Intel
	300 nsF	NMOS	TS	28	5	2186-30	Intel
						2187A-30	Intel
						2187A-35	Intel
	350 nsF	NMOS	TS	28	5	2186-35	Intel
						2187A-25	Intel
16384x1	55 nsF	NMOS	TS	20	5	M5M2167-55	Mitsubishi
	70 nsF	NMOS	TS	20	5	M5M2167-70	Mitsubishi
	100 nsF	NMOS	TS	16	5	MB8117-10	Fujitsu
						MB8118-10	Fujitsu
						HM8416A-3	Hitachi
						MK4516-10	Mostek
						MCM4517-10	**Motorola** (4046,4049)
						μPD2118-3	NEC
				18	5	**IMS2620-10**	**Inmos** (3979)
	120 nsF	NMOS	TS	16	5	MB8117-12	Fujitsu
						MB8118-12	Fujitsu
						HM8416A-4	Hitachi
						2118-4	Intel
						M2118-4	† Intel
						MK4516-12	Mostek
						MCM4517-12	**Motorola** (4046,4049)
						MCM6665C-12	**Motorola** (4046)
					±5,12	HM4716A-1	Hitachi
						MM5290-1	National
						μPD-2118-2	NEC
						μPD416-5	**NEC** (4073)
				18	5	**IMS2620-12**	**Inmos** (3979)
	150 nsF	NMOS	TS	16	5	HM4816A-7	Hitachi
						M2118-7	† Intel
						MK4516-15	Mostek
						MCM4517-15	**Motorola** (4046,4049)
						MCM6665C-15	**Motorola** (4046)
					±5,12	F4116-2	Fairchild
						HM4716A-2	Hitachi
						ITT4116-2	ITT
						M5K4116-2	Mitsubishi
						MK4116-2	Mostek
						MKB4116-82	† Mostek
						MCM4116B-15	**Motorola** (4046)
						MM5290-2	National
						μPD2118	NEC
						μPD416-3	**NEC** (4073)
						M4116	SGS
						HYB4116-P2	Siemens
						TMS4116-15	TI
						TMM416-2	Toshiba
				18	5	**IMS2620-15**	**Inmos** (3979)
	200 nsF	NMOS	TS	16	±5	**MCM4517-20**	**Motorola** (4046,4049)
					±5,12	**AM9016E**	**AMD** (3918)
						F4116-3	Fairchild
						HM4716A-3	Hitachi
						ITT4116-3	ITT
						M5K4116-3	Mitsubishi
						MK4116-3	Mostek
						MKB4116-83	† Mostek
						MCM4116B-20	**Motorola** (4046)
						MCM6665C-20	**Motorola** (4046)
						MM5290-3	National
						μPD416-2	**NEC** (4073)
						HYB4116-3	Siemens
						HYB4116-P3	Siemens

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

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MEMORY

MEMORY-RAMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	
Dynamic								**(Cont'd)**
16384x1	200 nsF	NMOS	TS	16	±5,12			(Cont'd)
						TMS4116-20	TI	
						TMM416-3	Toshiba	
	235 nsF	NMOS	TS	16	5	MKB4516-80 †	Mostek	
	250 nsF	NMOS	TS	16	±5,12	AM9016D	AMD	(3918)
						F4116-4	Fairchild	
						HM4716A-4	Hitachi	
						ITT4116-4	ITT	
						MK4116-4	Mostek	
						MKB4116-84 †	Mostek	
						MCM4116B-25	Motorola	(4046)
						MM5290-4	National	
						μPD416-1	NEC	(4073)
						HYB4116-4	Siemens	
						TMS4116-25	TI	
						TMM416-4	Toshiba	
	270 nsF	NMOS	TS	16	5	MKB4516-81 †	Mostek	
	300 nsF	NMOS	TS	16	±5,12	AM9016C	AMD	(3918)
						MCM4116B-30	Motorola	(4046)
						μPD416	NEC	(4073)
	320 nsF	NMOS	TS	16	5	MKB4516-82 †	Mostek	
16384x4	100 nsF	NMOS	TS	18	5	MB81416-10	Fujitsu	
	120 nsF	NMOS	TS	18	5	MB81416-12	Fujitsu	
	150 nsF	NMOS	TS	18	5	MB81416-15	Fujitsu	
						SMJ4416-15 †	TI	(4220)
						TMS4416-15	TI	(4220)
	200 nsF	NMOS	TS	18	5	SMJ4416-20 †	TI	(4220)
						TMS4416-20	TI	(4220)
	250 nsF	NMOS	TS	18	5	TMS4416-25	TI	(4220)
32768x1	200 nsF	NMOS	TS	18	±5,12	MK4332D-3	Mostek	
						MKM4332-83 †	Mostek	
	250 nsF	NMOS	TS	18	±5,12	MKM4332-84 †	Mostek	
64536x1	150 nsF	NMOS	TS	16	5	MB8264A-15W†	Fujitsu	
	200 nsF	NMOS	TS	16	5	MB8264A-20W†	Fujitsu	
65536x1	55 nsF	NMOS	TS	16	5	MB8281	Fujitsu	
	100 nsF	NMOS	TS	16	5	F4164	Fairchild	
						MB8264A-10	Fujitsu	
						MB8265A-10	Fujitsu	
						MB8266A-10	Fujitsu	
						IMS2600-10	Inmos	(3979)
						μPD4164-2	NEC	(4077)
	120 nsF	NMOS	TS	16	5	F4164-12	Fairchild	
						F64K-12	Fairchild	
						MB8264A-12	Fujitsu	
						MB8265A-12	Fujitsu	
						MB8266A-12	Fujitsu	
						HM4864-1	Hitachi	
						HM4864A-12	Hitachi	
						HM4865A-12	Hitachi	
						IMS2600-12	Inmos	(3979)
						MT4265-12A	MicronTech	
						MCM6665A-12	Motorola	(4046)
						MCM6665B-12	Motorola	(4046)
						NMC4164-12	National	
						μPD4164-12	NEC	(4077)
						MSM3764-12	OKI	(4118)
						SMJ4164-12 †	TI	(4219)
						TMS4164-12	TI	(543,4219)
						TMM4164-2	Toshiba	
	150 nsF	NMOS	TS	16	5	F4164-15	Fairchild	
						F64K-15	Fairchild	
						MB8264-15	Fujitsu	
						MB8264A-15	Fujitsu	
						MB8265-15	Fujitsu	
						MB8265A-15	Fujitsu	
						MB8266A-15	Fujitsu	
								(Continued)
65536x1	150 nsF	NMOS	TS	16	5			(Cont'd)
						HM4864-2	Hitachi	
						HM4864A-15	Hitachi	
						HM4865A-15	Hitachi	
						IMS2600-15	Inmos	(3979)
						2164A-15	Intel	
						MT4264-15A	MicronTech	
						M5K4164-15	Mitsubishi	
						MK4564-15	Mostek	
						MKB4564-82 †	Mostek	
						MCM6664A-15	Motorola	(4046)
						MCM6665A-15	Motorola	(4046)
						MCM6665B-15	Motorola	(4046)
						NMC4164-15	National	
						μPD4164-15	NEC	(4077)
						μPD4164-3	NEC	(4077)
						MSM3764-15	OKI	(4118)
						MN4164-15	Panasonic	(4120)
						HYB4164-2	Siemens	
						SMJ4164-15 †	TI	(4219)
						TMS4164-15	TI	(543,4219)
						TMM4164-3	Toshiba	
				20	5	TMS4161	TI	(4214)
	200 nsF	NMOS	TS	16	5	F4164-20	Fairchild	
						F64K-20	Fairchild	
						MB8264-20	Fujitsu	
						MB8265-20	Fujitsu	
						HM4864-3	Hitachi	
						HM4864A-20	Hitachi	
						HM4865A-20	Hitachi	
						2164A-20	Intel	
						M2164A-20 †	Intel	
						MT4264-20A	MicronTech	
						M5K4164-20	Mitsubishi	
						MK4564-20	Mostek	
						MKB4564-83 †	Mostek	
						MCM6664A-20	Motorola	(4046)
						MCM6665A-20	Motorola	(4046)
						MCM6665B-20	Motorola	(4046)
						NMC4164-20	National	
						μPD4164-0	NEC	(4077)
						μPD4164-20	NEC	(4077)
						MSM3764-20	OKI	(4118)
						MN4164-20	Panasonic	(4120)
						HYB4164-3	Siemens	
						SMJ4164-20 †	TI	(4219)
						TMS4164-20	TI	(543,4219)
						TMM4164-4	Toshiba	
	250 nsF	NMOS	TS	16	5	MK4564-25	Mostek	
						MKB4564-84 †	Mostek	
						μPD4164-1	NEC	(4077)
						TMS4164-25	TI	(543,4219)
65536x4	100 nsF	NMOS	TS	18	5	TMS4464-10	TI	(4213)
	120 nsF	NMOS	TS	18	5	TMS4464-12	TI	(4213)
	150 nsF	NMOS	TS	18	5	TMS4464-15	TI	(4213)
	200 nsF	NMOS	TS	18	5	TMS4464-20	TI	(4213)
65536x9	200 nsF	Mod	TS	30	5	HS2649	National	(4071)
131072x1								
	150 nsF	NMOS	TS	18	5	MK4528-15	Mostek	
	200 nsF	NMOS	TS	18	5	MK4528-20	Mostek	
						MKM4528D-83†	Mostek	
	250 nsF	NMOS	TS	18	5	MK4528-25	Mostek	
						MKM4528D-84†	Mostek	
262144x1								
	100 nsF	NMOS	TS	16	5	MB81256-10	Fujitsu	
						MB81257-10	Fujitsu	
						MCM6256-10	Motorola	(4051)
						TMS4256-10	TI	(4212)
						TMS4257-10	TI	(4212)
								(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–RAMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Page	Line
Dynamic								**(Cont'd)**	
262144x1								(Cont'd)	
	120 nsF	NMOS	TS	16	5	MB81256-12	Fujitsu		
						MB81257-12	Fujitsu		
						HM50256-12	**Hitachi**	**(3970)**	
						HM50257-12	**Hitachi**	**(3971)**	
						MCM6256-20	**Motorola**	**(4051)**	5
						TMS4256-12	**TI**	**(4212)**	
						TMS4257-12	**TI**	**(4212)**	
						TMM41256-12	Toshiba		
	150 nsF	NMOS	TS	16	5	MB81256-15	Fujitsu		
						MB81257-15	Fujitsu		10
						HM50256-15	**Hitachi**	**(3970)**	
						HM50257-15	**Hitachi**	**(3971)**	
						TMS4256-15	**TI**	**(4212)**	
						TMS4257-15	**TI**	**(4212)**	
						TMM41256-15	Toshiba		15
	200 nsF	NMOS	TS	16	5	**HM50256-20**	**Hitachi**	**(3970)**	
						HM50257-20	**Hitachi**	**(3971)**	
						MCM6256-20	Motorola		
						TMS4256-20	**TI**	**(4212)**	
						TMS4257-20	**TI**	**(4212)**	20
Static									
4x4	1 µsR	CMOS	—	24	4.5-15	MC14580BA	† Motorola		
	1.5 µsR	CMOS	—	24	3-15	MC14580BC	Motorola		
	40 nsR	TTL	OC	16	5	54170	† Fairchild		
						54LS170	† Fairchild		
						74170	Fairchild		25
						74LS170	Fairchild		
						ZN54170	† Fairchild		
						ZN74170	Ferranti		
						HM74LS170	Hitachi		
						SN74LS170	Motorola		30
						DM54170	† National		
						DM54LS170	† National		
						DM74170	National		
						DM74LS170	National		
						74LS170	SGS		35
						54LS170	† Signetics		
						74LS170	Signetics		
						SN54170	**† TI**	**(981)**	
						SN54LS170	**† TI**	**(981)**	
						SN74170	**TI**	**(981)**	40
						SN74LS170	**TI**	**(981)**	
			TS	16	5	54LS670	† Fairchild		
						74LS670	Fairchild		
						HD74LS670	Hitachi		
						M74LS670	Mitel		45
						SN54LS670	† Motorola		
						SN74LS670	Motorola		
						DM54LS670	† National		
						DM74LS670	National		
						74LS670	SGS		50
						54LS670	**† Signetics**	**(530)**	
						74LS670	Signetics		
						SN54LS670	**† TI**	**(1080)**	
						SN74LS670	**TI**	**(1080)**	
4x8	1 µsR	CMOS	—	24	3-15	CD4039A	† RCA		55
						CM4036A	† Solitron		
						CM4039A	† Solitron		
					5	CD4036A	† RCA		
8x2	12 nsF	ECL	OE	18	−5.2	**10155**	**Signetics**	**(858)**	
	15 nsF	ECL	—	24	−5.2	**MCM10143**	**Motorola**	**(4046)**	60
	50 nsR	TTL	TS	24	5	74S172	Signetics		
						SN74172	**TI**	**(982)**	
16x1	20 nsR	TTL	OC	14	5	**SN7481A**	**TI**	**(948)**	
				16	5	**SN7484A**	**TI**	**(949)**	
								(Continued)	

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Page	Line
16x1								(Cont'd)	
	35 nsR	TTL	OC	14	5	MC4004	Motorola		65
						MC4005	Motorola		
						MC4304	† Motorola		
						MC4305	† Motorola		
16x12	40 ns *	TTL	OC	20	5	SN54LS313	† TI		
16x4	5 nsF	ECL	OE	16	−4.5	F100402	Fairchild		70
	6 nsF	ECL	OE	16	−5.2	**MC10H145**	**Motorola**	**(821)**	
	7 nsF	ECL	OE	24	−4.5	F100145	Fairchild		
						100145	**Signetics**	**(858)**	
	9 nsF	ECL	OE	16	−5.2	F10145A	Fairchild		
						F10545A	† Fairchild		75
	10 ns *	ECL	OE	16	−5.2	HD10145	Hitachi		
	15 nsF	ECL	OE	16	−5.2	**MCM10145**	**Motorola**	**(4046)**	
	15 nsR	ECL	OE	16	−5.2	10145	Signetics		
	18 nsF	ECL	OE	16	−5.2	MCM10545	† Motorola		
	20 nsF	TTL	TS	18	5	9410C	Fairchild		80
	25 nsF	TTL	OC	16	5	AM27S02AC	AMD		
						AM27S06AC	AMD		
						AM27S06C	AMD		
			TS	16	5	AM27S03AC	AMD		
						AM27S07AC	AMD		85
						AM27S07C	AMD		
						DM74S189A	National		
	30 nsF	TTL	OC	16	5	AM27S02AM	† AMD		
						AM27S06AM	† AMD		
						AM27S06M	† AMD		90
			TS	16	5	AM27S03AM	† AMD		
						AM27S07AM	† AMD		
						AM27S07M	† AMD		
						DM54S189A	National		
	35 nsF	TTL	OC	16	5	AM27S02C	AMD		95
						AM3101-1C	AMD		
						AM3101AC	AMD		
						SN7489-1	AMD		
						SN74S289	AMD		
						74S289	Fairchild		100
						HD74S289	Hitachi		
						DM74S289	National		
						µPB2289	NEC		
						N3101A	Signetics		
						SN74S289A	**TI**	**(1012)**	105
			TS	16	5	AM27S03C	AMD		
						SN74S189	AMD		
						74S189	Fairchild		
						HD74S189	Hitachi		
						DM74S189	National		110
						74S189	Signetics		
						SN74S189A	**TI**	**(988)**	
	40 nsF	TTL	TS	18	5	DM85S68	National		
	45 ns *	TTL	OC	16	5	74LS289	Fairchild		
			TS	16	5	74LS189	Fairchild		115
	45 nsF	TTL	OC	16	5	AM27S02M	† AMD		
			TS	16	5	AM27S03M	† AMD		
	50 nsF	TTL	OC	16	5	AM3101-1M	† AMD		
						AM3101AM	† AMD		
						SN5489-1	† AMD		120
						SN54S289	† AMD		
						SN7489	AMD		
						54S289	† Fairchild		
						DM54S289	† National		
						N82S25	Signetics		125
						S3101A	† Signetics		
						SN54S289A	**† TI**	**(1012)**	
				28	5	IDM29705C	National		
			TS	16	5	SN54S189	† AMD		
								(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

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MEMORY

MEMORY-RAMs (Cont'd)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source
16x4	50 nsF	TTL	TS	16	5		(Cont'd)
						54S189	† Fairchild
						DM54S189	† National
						DM8599	National
						54S189	**† Signetics (532)**
						SN54S189A	**† TI (988)**
				28	5	IDM2970C	National
	53 nsF	TTL	TS	28	5	**AM29705C**	**AMD (1425)**
						F29705M	† National
						IDM29705	† National
	55 ns *	TTL	OC	16	5	54LS289	† Fairchild
						54LS89	† Fairchild
			TS	16	5	54LS189	† Fairchild
	55 nsF	TTL	OC	16	5	AM27LS02C	AMD
						AM27LS06C	AMD
				28	5	IDM29704M	† National
			TS	16	5	AM27LS03C	AMD
						AM27LS07C	AMD
	58 nsF	TTL	TS	28	5	**AM29705M**	**† AMD (1425)**
	60 nsF	TTL	OC	16	5	AM27LS06M	† AMD
						AM3101	AMD
						AM5489	† AMD
						DM8589	National
						μPB2089	NEC
						S82S25	† Signetics
						SN54LS289A	**† TI (1012)**
						SN54LS319A	**† TI (1017)**
						SN74LS289A	**TI (1012)**
						SN74LS319A	**TI (1017)**
			TS	16	5	AM27LS07M	† AMD
						SN54LS189A	**† TI (988)**
						SN54LS219A	**† TI (994)**
						SN74LS189A	**TI (988)**
						SN74LS219A	**TI (994)**
	60 nsR	TTL	OC	16	5	HD7489	Hitachi
						SN7489	**TI (951)**
	70 nsF	TTL	OC	16	5	AM27LS02C	AMD
			TS	16		AM27LS03C	AMD
						DM7599	† National
	80 nsF	TTL	OC	16	5	DM7589	† National
	85 nsF	TTL	OC	16	5	AM27LS02M	† AMD
			TS	16	5	AM27LS03M	† AMD
	110 nsR	TTL	OC	16	5	AM31L01C	AMD
						AM31L01M	† AMD
	120 nsR	CMOS	TS	18	4.5-12.5	F4710BC	Fairchild
						F4710BM	† Fairchild
	650 nsR	CMOS	TS	16	5	MM74C89	National
						CD40114B	† RCA
						CD4011BE	**RCA (837)**
16x9	40 ns *	TTL	OC	20	5	SN54LS311	† TI
						SN54LS312	† TI
						SN74LS311	TI
						SN74LS312	TI
			TS	20	5	SN54LS211	† TI
						SN54LS212	† TI
						SN74LS211	TI
						SN74LS212	TI
16x12	40 ns *	TTL	TS	20	5	SN54LS213	† TI
						SN74LS213	TI
32x2	50 nsF	TTL	OC	16	5	N82S21	Signetics
32x8	40 ns *	TTL	OC	20	5	SN54LS318	† TI
						SN74LS318	TI
			TS	20	5	SN54LS218	† TI
						SN74LS218	TI

(Continued)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source
32x8							(Cont'd)
	300 ns *	CMOS	TS	18	10	HCMP1824	Hughes
						HMMP1824	† Hughes
						CDP1824	**† RCA (1594)**
	600 ns *	CMOS	TS	18	5	**CDP1824C**	**† RCA (1594)**
					10	HCMP1824C	Hughes
						HMMP1824C	† Hughes
64x1	1.05 μsR	CMOS	TS	24	5-15	MCM14552A	† Motorola
	2.1 μsR	CMOS	TS	24	5-15	HD14552B	Hitachi
						MCM14552C	Motorola
	10 nsR	ECL	OE	16	−5.2	SN10142	TI
	12 nsF	ECL	OE	16	−5.2	μPB10142	NEC
	15 nsF	ECL	OE	16	−5.2	HD10148	Hitachi
						MCM10148	**Motorola (4046)**
						μPB10148	NEC
	15 nsR	ECL	OE	16	−5.2	SN10140	TI
						SN10148	TI
	270 nsR	CMOS	—	14	3-18	MCM14505A	† Motorola
						HEF4505	**† Signetics (864)**
	350 nsR	CMOS	—	14	4.5-16	HD14505B	Hitachi
						MCM14505C	Motorola
64x4	6 ns *	ECL	OE	24	−5.2	GXB100473	Siemens
	40 ns *	TTL	OC	16	5	SN54LS316	† TI
						SN54LS317	† TI
						SN74LS316	TI
						SN74LS317	TI
			TS	16	5	SN54LS216	† TI
						SN54LS217	† TI
						SN74LS216	TI
						SN74LS217	TI
	2000 ns *	CMOS	TS	16	5	MN1203	Panasonic
64x8	800 nsF	CMOS	TS	22	5	**CDP1826C**	**RCA (1594)**
64x9	35 nsF	TTL	OC	28	5	93419A	Fairchild
						N82S09	Signetics
						N82S19	Signetics
	45 nsF	TTL	OC	28	5	93419C	Fairchild
						MBM93419	Fujitsu
	60 nsF	TTL	OC	28	5	93419M	† Fairchild
						S82S19	**† Signetics (532)**
	80 nsF	TTL	OC	28	5	**S82S09**	**† Signetics (532)**
64x12	150 nsF	CMOS	TS	18	3-11	IM6512AI	Intersil
						IM6512AM	† Intersil
	460 nsF	CMOS	TS	18	3-7	IM6512I	Intersil
						IM6512M	† Intersil
	600 nsF	CMOS	TS	18	3-7	IM6512C	Intersil
128x1	12 nsR	ECL	OE	16	−5.2	**MCM10147**	**Motorola (4046)**
						GXB10147A	Siemens
	15 nsR	ECL	OE	16	−5.2	HD10147	Hitachi
						SN10147	TI
128x8	—	CMOS	—	8	5	PCD8571	Signetics
	250 ns *	NMOS	TS	24	5	S68B10	AMI
						F68B10	Fairchild
						MCM68B10	**Motorola (4046)**
	250 nsF	CMOS	TS	24	10	**CDP1823**	**RCA (1594)**
		NMOS	TS	24	5	EF68B10	Thomson-CSF
	350 nsF	NMOS	TS	24	5	S6810-1	AMI
	360 nsF	NMOS	TS	24	5	S68A10	AMI
						F68A10	Fairchild
						HM468A10	Hitachi
						MCM68A10	**Motorola (4046)**
						EF68A10	Thomson-CSF
	450 nsF	CMOS	TS	24	5	**CDP1823C**	**RCA (1594)**
		NMOS	TS	24	5	S6810	AMI
						F6810	**Fairchild (1461)**
						HM46810	Hitachi

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–RAMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source
Static							**(Cont'd)**
128x8	450 nsF	NMOS	TS	24	5		(Cont'd)
						MCM6810	**Motorola (1505,4046)**
						EF6810	Thomson-CSF
256x1	1.4 µsR	CMOS	—	16	3-15	MCM14537A	† Motorola
	2 µsR	CMOS	—	16	3-15	HD14537B	† Hitachi
						MCM14537C	† Motorola
	8 nsF	ECL	OE	16	−5.2	HM10414-1	Hitachi
	10 nsF	ECL	OE	16	−5.2	F100414C	Fairchild
						F10414C	Fairchild
						HM10414	Hitachi
						DM10414A	National
	15 nsF	ECL	OE	16	−5.2	F10414M	† Fairchild
						MCM10152	**Motorola (4046)**
	25 nsF	ECL	OE	16	−5.2	µPB10144	NEC
	26 nsF	ECL	OE	16	−5.2	**MCM10144**	**Motorola (4046)**
						MCM10544	† Motorola
						DM10414	National
	30 nsF	ECL	OE	16	−5.2	F10410C	Fairchild
	35 nsF	TTL	TS	16	5	AM27LS00AC	AMD
	35 nsR	ECL	OE	16	−5.2	SN10144	TI
	40 nsF	TTL	OC	16	5	74LS301	Signetics
						N82LS17	**Signetics (4160)**
			TS	16	5	**N82LS16**	**Signetics (4160)**
	45 nsF	TTL	OC	16	5	AM27LS01AC	AMD
						AM27LS01AM	† AMD
						AM29720C	AMD
						HM2504-1	Hitachi
			TS	16	5	AM27LS00AM	† AMD
						AM27LS00C	AMD
						AM29721C	AMD
	50 nsF	TTL	OC	16	5	µPB2206	NEC
						N82S17	Signetics
			TS	16	5	DM74S200	National
						µPB2200	NEC
						N82S16	Signetics
	55 nsF	TTL	OC	16	5	AM27LS01M	† AMD
						AM29720M	† AMD
						HM2504	† Hitachi
			TS	16	5	AM27LS00M	† AMD
						AM29721M	† AMD
	60 nsF	TTL	OC	16	5	DM74S206	National
						S82LS17	**† Signetics (4160)**
			TS	16	5	**S82LS16**	**† Signetics (4160)**
	65 nsF	TTL	OC	16	5	**SN74S301**	**† TI (1016)**
			TS	16	5	µPB2202	NEC
						SN74S201	**TI (993)**
	70 nsF	TTL	OC	16	5	54LS301	† Signetics
						54S301	**† Signetics (532)**
						S82S17	† Signetics
			TS	16	5	**S82S16**	**† Signetics (532)**
	80 nsF	TTL	OC	16	5	AM27LS01LC	AMD
			TS	16	5	AM27LS00LC	AMD
	95 nsF	TTL	OC	16	5	AM27LS01LM	† AMD
			TS	16	5	AM27LS00LM	† AMD
	100 nsF	TTL	TS	16	5	93L421M	† Fairchild
	200 ns *	CMOS	TS	16	3-15	F4720AC	Fairchild
					4.5-12.5	F4720C	Fairchild
						F4720M	† Fairchild
	345 nsF	CMOS	TS	16	10	CD40061A	† RCA
	400 nsR	CMOS	TS	16	3-15	MM54C200	† National
						MM74C200	National
							(Continued)
256x1							(Cont'd)
	850 nsF	CMOS	TS	16	5	CD40061	RCA
	900 nsF	PMOS	—	16	−12.5	MK4007	Mostek
						MK4007-4	Mostek
256x4	3 µsF	CMOS	TS	22	3	ITT5101S	ITT
	6 nsF	ECL	OE	24	−5.2	HM10422-6	Hitachi
	7 nsF	ECL	OE	24	−4.5	MBM100422A-7	Fujitsu
					−5.2	MBM10422A-7	Fujitsu
						HM10422-7	Hitachi
	10 nsF	ECL	—	24	−5.2	MBM10422	Fujitsu
			OE	24	−4.5	F100422	Fairchild
						F100422C	Fairchild
						100422B	Signetics
					−5.2	F10422	Fairchild
						F10422C	Fairchild
						DM10422A	National
						10422B	Signetics
	12 nsF	ECL	OE	22	−5.2	MB7072E	Fujitsu
				24	−4.5	HM100422	Hitachi
					−5.2	HM10422	Hitachi
	15 nsF	ECL	OE	22	−5.2	MB7072N	Fujitsu
				24	−4.5	DM100422	National
						100422	Signetics
						100422A	Signetics
					−5.2	MBM10422N	Fujitsu
						DM10422	National
						10422A	Signetics
	20 nsF	ECL	—	24	−5.2	10422	Signetics
	25 nsF	NMOS	TS	24	5	**AM9122-25**	**AMD (3916)**
	30 nsF	ECL	OE	24	−5.2	93422AM	† Fairchild
						93L422AC	Fairchild
	30 nsF*	TTL	TS	22	5	MCM93L422	Motorola
	35 nsF	NMOS	TS	24	5	**AM9122-35**	**AMD (3916)**
						AM9122-35M	**† AMD (3916)**
						AM91L22-35	**AMD (3916)**
		TTL	OC	22	5	AM93412AC	AMD
			TS	22	5	AM93422AC	AMD
						MCM93L422	**Motorola (4046)**
	40 nsF	TTL	OC	22	5	AM93412	AMD
			TS	16	5	SN74S207	TI
				20	5	SN74S208	TI
				22	5	AM93422	AMD
						93422C	Fairchild
						MCM93422	**Motorola (4046)**
	45 nsF	NMOS	TS	24	5	**AM91L22-45**	**AMD (3916)**
						AM91L22-45M	**† AMD (3916)**
		TTL	OC	22	5	AM93412AM	† AMD
						AM93L412AC	AMD
			TS	22	5	AM93422AM	† AMD
						AM93L422AC	AMD
	55 nsF	TTL	OC	22	5	AM93L412AM	† AMD
			TS	22	5	AM93L422AM	† AMD
	60 nsF	NMOS	TS	24	5	**AM91L22-60**	**AMD (3916)**
		TTL	OC	22	5	AM93412M	† AMD
						AM93L412	AMD
			TS	22	5	AM93422M	† AMD
						AM93L422	AMD
						93422M	† Fairchild
						93L422C	Fairchild
	75 nsF	TTL	OC	22	5	AM93L412M	† AMD
			TS	22	5	AM93L422M	† AMD
						93L422AM	Fairchild
						93L422M	† Fairchild
	175 nsF	NMOS	TS	16	5	SY21H12	Synertek
				18	5	SY21H11	Synertek
				22	5	SY21H01	Synertek
							(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

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MEMORY

MEMORY-RAMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
Static							**(Cont'd)**	
256x4							(Cont'd)	
	200 nsF	NMOS	TS	16	5	SY21H12-2	Synertek	
				18	5	SY21H11-2	Synertek	
				22	5	SY21H01-2	Synertek	
	220 nsF	CMOS	TS	18	5	**HM6561B-2**	**† Harris (3965)**	
						HM6561B-8	**† Harris (3965)**	5
						HM6561B-9	**Harris (3965)**	
						IM65X61-1	Intel	
						IM65X61-1	Intersil	
						IM65X61-1M	† Intersil	
				22	5	**HM6551B-2**	**† Harris (3965)**	10
						HM6551B-8	**† Harris (3965)**	
						HM6551B-9	**Harris (3965)**	
						IM65X51-1	Intersil	
						IM65X51-1M	† Intersil	
	235 nsF	CMOS	TS	18	10	IM65X61A	Intersil	15
						IM65X61AM	† Intersil	
				22	10	IM65X51A	Intersil	
						IM65X51AM	† Intersil	
	240 nsF	CMOS	TS	22	5	**HS6551RH**	**† Harris (4689)**	
	250 nsF	CMOS	TS	22	5	**MWS5101EL2**	**RCA (1594)**	20
						SCM5101-1B	SSS	
					10	**CDP1822**	**RCA (1594)**	
						TCC-244	RCA	
		NMOS	TS	16	5	AM9101D	AMD	
						AM9111D	AMD	25
						AM9112D	AMD	
						SY2112A-2	**Synertek (4210)**	
				18	5			
						µPD2111AL-2	NEC	
						SY2111A-2	**Synertek (4210)**	
				22	5	**SY2101A-2**	**Synertek (4210)**	30
	300 nsF	CMOS	TS	18	5	**HM6561-2**	**† Harris (3965)**	
						HM6561-8	**† Harris (3965)**	
						HM6561-9	**Harris (3965)**	
						IM65X61	Intersil	
						IM65X61M	† Intersil	35
				22	5	**HM6551-2**	**† Harris (3965)**	
						HM6551-8	**† Harris (3965)**	
						HM6551-9	**Harris (3965)**	
						IM65X51	Intersil	
						IM65X51M	† Intersil	40
						LH-5101S	Sharp	
		NMOS	TS	16	5	AM9101C	AMD	
						AM9101CM	† AMD	
						AM9111C	AMD	
						AM9111CM	† AMD	45
						AM9112C	AMD	
						AM9112CM	† AMD	
						AM91L01C	AMD	
						AM91L01CM	† AMD	
						AM91L111C	AMD	50
						AM91L11CM	† AMD	
						AM91L12C	AMD	
						AM91L12CM	† AMD	
	350 nsF	CMOS	TS	18	5	**HM6561-5**	**Harris (3965)**	
						IM65X61C	Intersil	55
				22	5	**HM6551-5**	**Harris (3965)**	
						IM65X51C	Intersil	
						MWS5101DL3	**† RCA (1594)**	
						MWS5101EL3	**RCA (1594)**	
						SCM5101-1A	SSS	60
		NMOS	TS	16	5	**SY2112A**	**Synertek (4210)**	
				18	5	**SY2111A**	**Synertek (4210)**	
				22	5	**SY2101A**	**Synertek (4210)**	
							(Continued)	

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
256x4							(Cont'd)	
	400 nsF	CMOS	TS	22	5	HMMP1822C	† Hughes	
						CDP1822C	**† RCA (1594)**	65
		NMOS	TS	16	5	AM9101B	AMD	
						AM9101BM	† AMD	
						AM9111B	AMD	
						AM9111BM	† AMD	
						AM9112B	AMD	70
						AM9112BM	† AMD	
						AM91L01B	AMD	
						AM91L01BM	† AMD	
						AM91L11B	AMD	
						AM91L11BM	† AMD	75
						AM91L12B	AMD	
						AM91L12BM	† AMD	
	450 nsF	CMOS	TS	22	5	S5101L-1	AMI	
						S5101L1	AMI	
						S6501L1	AMI	80
						HM435101-1	Hitachi	
						M5L5101L-1	Mitsubishi	
						MCM51L01-45	Motorola	
						µPD5101L-1	NEC	
						SCM5101-1	SSS	85
						TC5501	Toshiba	
		NMOS	TS	16	5	**SY2112A-4**	**Synertek (4210)**	
				18	5	**SY2111A-4**	**Synertek (4210)**	
				22	5	**SY2101A-4**	**Synertek (4210)**	
	500 nsF	NMOS	TS	16	5	AM9112A	AMD	90
						AM9112AM	† AMD	
						AM91L12A	AMD	
						AM91L12AM	† AMD	
						SY2112-1	**Synertek (4210)**	
				18	5	AM9101A	AMD	95
						AM9101AM	AMD	
						AM9111A	AMD	
						AM9111AM	AMD	
						AM91L01A	AMD	
						AM91L01AM	AMD	100
						AM91L111AM	AMD	
						AM91L11A	AMD	
						SY2111-1	**Synertek (4210)**	
				22	5	**SY2101-1**	**Synertek (4210)**	
	650 nsF	CMOS	TS	22	5	S5101L	AMI	105
						S5101L-3	AMI	
						S5101L3	AMI	
						S6501L	AMI	
						S6501L-3	AMI	
						MCM5101-65	Motorola	110
						MCM51L01-65	Motorola	
						µPD5101L	NEC	
						SCM5101-3	SSS	
						TC5501-1	Toshiba	
	800 nsF	CMOS	TS	22	5	S5101-8	AMI	115
						S5101L8	AMI	
						S6501-8	AMI	
						S6501L-8	AMI	
						MCM5101-80	Motorola	
						MN5101	Panasonic	120
						LH-5101W	Sharp	
						883/5101-4	† SSS	
	950 nsF	NMOS	TS	18	5	M120	SGS	
256x8	40 nsF	TTL	TS	22	5	**N8X350**	**Signetics (1627,1652)**	
						S8X350	**† Signetics (527,532,1627,1652)**	125
256x9	35 nsF	TTL	TS	22	5	**N82S212A**	**Signetics (4162)**	
	45 nsF	TTL	TS	22	5	93479	Fairchild	
	60 nsF	TTL	TS	24	5	N82S210	Signetics	
							(Continued)	

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–RAMs (Cont'd)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	
256x9								(Cont'd)
	70 nsF	TTL	TS	22	5	**S82S212**	**† Signetics**	**(532)**
	90 nsF	TTL	TS	24	5	S82S210	† Signetics	
512x4	1.2 μsF	CMOS	TS	24	5	LH-5102	Sharp	
512x9	45 nsF	NMOS	TS	24	5	TM52150-4	TI	
	55 nsF	NMOS	TS	24	5	**TMS2150-5**	**TI**	**(4222)**
	70 nsF	NMOS	TS	24	5	**TMS2150-7**	**TI**	**(4222)**
	90 nsF	NMOS	TS	24	5	**TMS2150-9**	**TI**	**(4222)**
1024x1	8 nsF	ECL	OE	16	−5.2	HM2112-1	Hitachi	
	10 ns*	ECL	OE	16	−5.2	AM10415	AMD	
	10 nsF	ECL	OE	16	−4.5	100415B	Signetics	
					−5.2	F10415C	Fairchild	
						10415B	Signetics	
				24	−4.5	F100415C	Fairchild	
					−5.2	**MCM10146A**	**Motorola**	**(4046)**
			OE	16	−5.2	HM2112	Hitachi	
	15 nsF	ECL	OE	16	−4.5	**AM100415A**	**AMD**	**(3910)**
						100415A	Signetics	
					−5.2	**AM10415SA**	**† AMD**	**(3909)**
						MCM10415	**Motorola**	**(4047)**
	20 nsF	ECL	OE	16	−4.5	HM100415	Hitachi	
						100415	Signetics	
					−5.2	**AM10415A**	**† AMD**	**(3909)**
						AM10415SA	† AMD	
						F10415AC	Fairchild	
						MBM10415AH	Fujitsu	
						HM2110-2	Hitachi	
						MCM10415A	**† Motorola**	**(4047)**
						DM10415A	National	
						10415A	Signetics	
		NMOS	TS	16	5	2125H-1	Intel	
	25 nsF	ECL	OE	16	−5.2	AM10415A	† AMD	
						HM2110-1	Hitachi	
						GXB10415	Siemens	
		NMOS	OC	16	5	2115H-2	Intel	
			TS	16	5	2125H-2	Intel	
	29 nsF	ECL	OE	16	−5.2	**MCM10146**	**Motorola**	**(4046)**
	30 nsF	NMOS	OC	16	5	2115H-3	Intel	
			TS	16	5	2125H-3	Intel	
		TTL	OC	16	5	AM93415AC	AMD	
						AM93425AC	AMD	
						93415AC	Fairchild	
			TS	16	5	93425AC	Fairchild	
	35 nsF	ECL	OE	16	−5.2	**AM10415**	**AMD**	**(3909)**
						F10415	Fairchild	
						HM2110	Hitachi	
						DM10415	National	
		NMOS	OC	16	5	2115H-4	Intel	
			TS	16	5	2125H-4	Intel	
		TTL	OC	16	5	HM2510-2	Hitachi	
	40 nsF	ECL	OE	16	−5.2	**AM10415M**	**† AMD**	**(3909)**
						MCM10546	† Motorola	
		TTL	OC	16	5	AM93415AM	† AMD	
			TS	16	5	AM93425AM	† AMD	
	45 nsF	NMOS	OC	16	5	2115A	Intel	
						2115AL	Intel	
						MCM2115A-45	Motorola	
						MCM21L15A-45	Motorola	
			TS	16	5	2125A	Intel	
						2125AL	Intel	
						MCM2125A-45	Motorola	
						MCM21L25A-45	Motorola	
		TTL	OC	16	5	AM93415C	AMD	
								(Continued)
1024x1	45 nsF	TTL	OC	16	5			(Cont'd)
						93415C	Fairchild	
						HM2510-1	Hitachi	
						MCM93415C	**Motorola**	**(4046)**
			TS	16	5	AM93425C	AMD	
						93425C	Fairchild	
						HM2511-1	Hitachi	
						MCM93425	**Motorola**	**(4046)**
	50 nsF	TTL	OC	16	5	μPB2205	NEC	
						SN74S314A	TI	
			TS	16	5	93425AM	† Fairchild	
						SN74S214A	TI	
	55 nsF	NMOS	OC	16	5	MCM2115A-55	Motorola	
			TS	16	5	MCM2125A-55	Motorola	
	60 nsF	TTL	OC	16	5	AM93L415C	AMD	
						93415M	† Fairchild	
						93L415	Fairchild	
						93L415C	Fairchild	
						MCM93415M	**† Motorola**	**(4046)**
			TS	16	5	93425M	† Fairchild	
						93L425C	Fairchild	
	65 nsF	TTL	OC	16	5	AM93415M	† AMD	
			TS	16	5	AM93425M	† AMD	
	70 ns *	TTL	OC	16	5	SN74LS315	TI	
			TS	16	5	SN74LS215	TI	
	70 nsF	NMOS	OC	16	5	2115A-2	Intel	
						2115AL-2	Intel	
						MCM2115A-70	Motorola	
						MCM21L15A-70	Motorola	
			TS	16	5	2125A-2	Intel	
						2125AL-2	Intel	
						MCM2125A-70	Motorola	
						MCM21L25A-70	Motorola	
				18	5	HM2148	Hitachi	
		TTL	OC	16	5	AM93L415M	† AMD	
						93L415M	Fairchild	
						HM2510	Hitachi	
						SN74S314	TI	
			TS	16	5	AM93L425M	† AMD	
						93L425M	† Fairchild	
						HM2511	Hitachi	
						SN74S214	TI	
	95 nsF	TTL	OC	16	5	SN74LS314	TI	
			TS	16	5	SN74LS214	TI	
	125 nsF	CMOS	TS	16	4.5-10.5	IM65X08A-1	† Intersil	
						IM65X08A-1I	Intersil	
					10	**CDP1821**	**† RCA**	**(1594)**
				18	4.5-10.5	IM65X18A-1	Intersil	
						IM65X18A-1M	† Intersil	
	130 nsF	CMOS	TS	16	5	NMC85008B-9	National	
	180 nsF	CMOS	TS	16	5	**HM6508B-2**	**† Harris**	**(3965)**
						HM6508B-8	**† Harris**	**(3965)**
						HM6508B-9	**Harris**	**(3965)**
						IM5X08-1	Intersil	
						IM65X08-1M	† Intersil	
				18	5	**HM6518B-2**	**† Harris**	**(3965)**
						HM6518B-8	**† Harris**	**(3965)**
						HM6518B-9	**Harris**	**(3965)**
						IM65X18-1	Intersil	
						IM65X18-1M	† Intersil	
	200 nsF	CMOS	TS	16	4.5-10.5	IM65X08A	Intersil	
						IM65X08AM	† Intersil	
				18	4.5-10.5	IM65X18A	Intersil	
						IM65X18AM	† Intersil	
	250 nsF	CMOS	TS	16	5	**HM6508-2**	**† Harris**	**(3965)**
								(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY-RAMs (Cont'd)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source
256x4 (Cont'd)							
	200 nsF	NMOS	TS	16	5	SY21H12-2	Synertek
				18	5	SY21H11-2	Synertek
				22	5	SY21H01-2	Synertek
	220 nsF	CMOS	TS	18	5	**HM6561B-2**	† **Harris** (3965)
						HM6561B-8	† **Harris** (3965)
						HM6561B-9	**Harris** (3965)
						IM65X61-1	Intel
						IM65X61-1	Intersil
						IM65X61-1M	† Intersil
				22	5	**HM6551B-2**	† **Harris** (3965)
						HM6551B-8	† **Harris** (3965)
						HM6551B-9	**Harris** (3965)
						IM65X51-1	Intersil
						IM65X51-1M	† Intersil
	235 nsF	CMOS	TS	18	10	IM65X61A	Intersil
						IM65X61AM	† Intersil
				22	10	IM65X51A	Intersil
						IM65X51AM	† Intersil
	240 nsF	CMOS	TS	22	5	**HS6551RH**	† **Harris** (4689)
	250 nsF	CMOS	TS	22	5	**MWS5101EL2**	**RCA** (1594)
						SCM5101-1B	SSS
					10	**CDP1822**	**RCA** (1594)
						TCC-244	RCA
		NMOS	TS	16	5	AM9101D	AMD
						AM9111D	AMD
						AM9112D	AMD
						SY2112A-2	**Synertek** (4210)
				18	5		
						µPD2111AL-2	NEC
						SY2111A-2	**Synertek** (4210)
				22	5	**SY2101A-2**	**Synertek** (4210)
	300 nsF	CMOS	TS	18	5	**HM6561-2**	† **Harris** (3965)
						HM6561-8	† **Harris** (3965)
						HM6561-9	**Harris** (3965)
						IM65X61	Intersil
						IM65X61M	† Intersil
				22	5	**HM6551-2**	† **Harris** (3965)
						HM6551-8	† **Harris** (3965)
						HM6551-9	**Harris** (3965)
						IM65X51	Intersil
						IM65X51M	† Intersil
						LH-5101S	Sharp
		NMOS	TS	16	5	AM9101C	AMD
						AM9101CM	† AMD
						AM9111C	AMD
						AM9111CM	† AMD
						AM9112C	AMD
						AM9112CM	† AMD
						AM91L01C	AMD
						AM91L01CM	† AMD
						AM91L111C	AMD
						AM91L11CM	† AMD
						AM91L12C	AMD
						AM91L12CM	† AMD
	350 nsF	CMOS	TS	18	5	**HM6561-5**	**Harris** (3965)
						IM65X61C	Intersil
				22	5	**HM6551-5**	**Harris** (3965)
						IM65X51C	Intersil
						MWS5101DL3	† **RCA** (1594)
						MWS5101EL3	**RCA** (1594)
						SCM5101-1A	SSS
		NMOS	TS	16	5	**SY2112A**	**Synertek** (4210)
				18	5	**SY2111A**	**Synertek** (4210)
				22	5	**SY2101A**	**Synertek** (4210)

(Continued)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source
256x4 (Cont'd)							
	400 nsF	CMOS	TS	22	5	HMMP1822C	† Hughes
						CDP1822C	† **RCA** (1594)
		NMOS	TS	16	5	AM9101B	AMD
						AM9101BM	† AMD
						AM9111B	AMD
						AM9111BM	† AMD
						AM9112B	AMD
						AM9112BM	† AMD
						AM91L01B	AMD
						AM91L01BM	† AMD
						AM91L11B	AMD
						AM91L11BM	† AMD
						AM91L12B	AMD
						AM91L12BM	† AMD
	450 nsF	CMOS	TS	22	5	S5101L-1	AMI
						S5101L1	AMI
						S6501L1	AMI
						HM435101-1	Hitachi
						M5L5101L-1	Mitsubishi
						MCM51L01-45	Motorola
						µPD5101L-1	NEC
						SCM5101-1	SSS
						TC5501	Toshiba
		NMOS	TS	16	5	**SY2112A-4**	**Synertek** (4210)
				18	5	**SY2111A-4**	**Synertek** (4210)
				22	5	**SY2101A-4**	**Synertek** (4210)
	500 nsF	NMOS	TS	16	5	AM9112A	AMD
						AM9112AM	† AMD
						AM91L12A	AMD
						AM91L12AM	† AMD
						SY2112-1	**Synertek** (4210)
				18	5	AM9101A	AMD
						AM9101AM	AMD
						AM9111A	AMD
						AM9111AM	AMD
						AM91L01A	AMD
						AM91L01AM	AMD
						AM91L111AM	AMD
						AM91L11A	AMD
						SY2111-1	**Synertek** (4210)
				22	5	**SY2101-1**	**Synertek** (4210)
	650 nsF	CMOS	TS	22	5	S5101L	AMI
						S5101L-3	AMI
						S5101L3	AMI
						S6501L	AMI
						S6501L-3	AMI
						MCM5101-65	Motorola
						MCM51L01-65	Motorola
						µPD5101L	NEC
						SCM5101-3	SSS
						TC5501-1	Toshiba
	800 nsF	CMOS	TS	22	5	S5101-8	AMI
						S5101L8	AMI
						S6501-8	AMI
						S6501L-8	AMI
						MCM5101-80	Motorola
						MN5101	Panasonic
						LH-5101W	Sharp
						883/5101-4	† SSS
	950 nsF	NMOS	TS	18	5	M120	SGS
256x8	40 nsF	TTL	TS	22	5	**N8X350**	**Signetics** (1627,1652)
						S8X350	† **Signetics** (527,532,1627,1652)
256x9	35 nsF	TTL	TS	22	5	**N82S212A**	**Signetics** (4162)
	45 nsF	TTL	TS	22	5	93479	Fairchild
	60 nsF	TTL	TS	24	5	N82S210	Signetics

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

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MEMORY

MEMORY-RAMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
Static							**(Cont'd)**	
256x9							(Cont'd)	
	70 nsF	TTL	TS	22	5	**S82S212**	**† Signetics (532)**	
	90 nsF	TTL	TS	24	5	S82S210	† Signetics	
512x4	1.2 μsF	CMOS	TS	24	5	LH-5102	Sharp	
512x9	45 nsF	NMOS	TS	24	5	TM52150-4	TI	
	55 nsF	NMOS	TS	24	5	**TMS2150-5**	**TI (4222)**	5
	70 nsF	NMOS	TS	24	5	**TMS2150-7**	**TI (4222)**	
	90 nsF	NMOS	TS	24	5	**TMS2150-9**	**TI (4222)**	
1024x1	8 nsF	ECL	OE	16	−5.2	HM2112-1	Hitachi	
	10 ns*	ECL	OE	16	−5.2	AM10415	AMD	
	10 nsF	ECL	OE	16	−4.5	100415B	Signetics	10
					−5.2	F10415C	Fairchild	
						10415B	Signetics	
				24	−4.5	F100415C	Fairchild	
					−5.2	**MCM10146A**	**Motorola (4046)**	
			OE	16	−5.2	HM2112	Hitachi	15
	15 nsF	ECL	OE	16	−4.5	**AM100415A**	**AMD (3910)**	
						100415A	Signetics	
					−5.2	**AM10415SA**	**† AMD (3909)**	
						MCM10415	**Motorola (4047)**	
	20 nsF	ECL	OE	16	−4.5	HM100415	Hitachi	20
						100415	Signetics	
					−5.2	**AM10415A**	**† AMD (3909)**	
						AM10415SA	† AMD	
						F10415AC	Fairchild	
						MBM10415AH	Fujitsu	25
						HM2110-2	Hitachi	
						MCM10415A	**† Motorola (4047)**	
						DM10415A	National	
						10415A	Signetics	
		NMOS	TS	16	5	2125H-1	Intel	30
	25 nsF	ECL	OE	16	−5.2	AM10415A	† AMD	
						HM2110-1	Hitachi	
						GXB10415	Siemens	
		NMOS	OC	16	5	2115H-2	Intel	
			TS	16	5	2125H-2	Intel	35
	29 nsF	ECL	OE	16	−5.2	**MCM10146**	**Motorola (4046)**	
	30 nsF	NMOS	OC	16	5	2115H-3	Intel	
			TS	16	5	2125H-3	Intel	
		TTL	OC	16	5	AM93415AC	AMD	
						AM93425AC	AMD	40
						93415AC	Fairchild	
			TS	16	5	93425AC	Fairchild	
	35 nsF	ECL	OE	16	−5.2	**AM10415**	**AMD (3909)**	
						F10415	Fairchild	
						HM2110	Hitachi	45
						DM10415	National	
		NMOS	OC	16	5	2115H-4	Intel	
			TS	16	5	2125H-4	Intel	
		TTL	OC	16	5	HM2510-2	Hitachi	
	40 nsF	ECL	OE	16	−5.2	**AM10415M**	**† AMD (3909)**	50
						MCM10546	† Motorola	
		TTL	OC	16	5	AM93415AM	† AMD	
			TS	16	5	AM93425AM	† AMD	
	45 nsF	NMOS	OC	16	5	2115A	Intel	
						2115AL	Intel	55
						MCM2115A-45	Motorola	
						MCM21L15A-45	Motorola	
			TS	16	5	2125A	Intel	
						2125AL	Intel	
						MCM2125A-45	Motorola	60
						MCM21L25A-45	Motorola	
		TTL	OC	16	5	AM93415C	AMD	
							(Continued)	
1024x1	45 nsF	TTL	OC	16	5		(Cont'd)	
						93415C	Fairchild	
						HM2510-1	Hitachi	
						MCM93415C	**Motorola (4046)**	65
			TS	16	5	AM93425C	AMD	
						93425C	Fairchild	
						HM2511-1	Hitachi	
						MCM93425	**Motorola (4046)**	
	50 nsF	TTL	OC	16	5	μPB2205	NEC	70
						SN74S314A	TI	
			TS	16	5	93425AM	† Fairchild	
						SN74S214A	TI	
	55 nsF	NMOS	OC	16	5	MCM2115A-55	Motorola	
			TS	16	5	MCM2125A-55	Motorola	75
	60 nsF	TTL	OC	16	5	AM93L415C	AMD	
						93415M	† Fairchild	
						93L415	Fairchild	
						93L415C	Fairchild	
						MCM93415M	**† Motorola (4046)**	80
			TS	16	5	93425M	† Fairchild	
						93L425C	Fairchild	
	65 nsF	TTL	OC	16	5	AM93415M	† AMD	
			TS	16	5	AM93425M	† AMD	
	70 ns *	TTL	OC	16	5	SN74LS315	TI	85
			TS	16	5	SN74LS215	TI	
	70 nsF	NMOS	OC	16	5	2115A-2	Intel	
						2115AL-2	Intel	
						MCM2115A-70	Motorola	
						MCM21L15A-70	Motorola	90
			TS	16	5	2125A-2	Intel	
						2125AL-2	Intel	
						MCM2125A-70	Motorola	
						MCM21L25A-70	Motorola	
				18	5	HM2148	Hitachi	95
		TTL	OC	16	5	AM93L415M	† AMD	
						93L415M	Fairchild	
						HM2510	Hitachi	
						SN74S314	TI	
			TS	16	5	AM93L425M	† AMD	100
						93L425M	† Fairchild	
						HM2511	Hitachi	
						SN74S214	TI	
	95 nsF	TTL	OC	16	5	SN74LS314	TI	
			TS	16	5	SN74LS214	TI	105
	125 nsF	CMOS	TS	16	4.5-10.5	IM65X08A-1	† Intersil	
						IM65X08A-1I	Intersil	
					10	**CDP1821**	**† RCA (1594)**	
				18	4.5-10.5	IM65X18A-1	Intersil	
						IM65X18A-1M	† Intersil	110
	130 nsF	CMOS	TS	16	5	NMC85008B-9	National	
	180 nsF	CMOS	TS	16	5	**HM6508B-2**	**† Harris (3965)**	
						HM6508B-8	**† Harris (3965)**	
						HM6508B-9	**Harris (3965)**	
						IM5X08-1	Intersil	115
						IM65X08-1M	† Intersil	
				18	5	**HM6518B-2**	**† Harris (3965)**	
						HM6518B-8	**† Harris (3965)**	
						HM6518B-9	**Harris (3965)**	
						IM65X18-1	Intersil	120
						IM65X18-1M	† Intersil	
	200 nsF	CMOS	TS	16	4.5-10.5	IM65X08A	Intersil	
						IM65X08AM	† Intersil	
				18	4.5-10.5	IM65X18A	Intersil	
						IM65X18AM	† Intersil	125
	250 nsF	CMOS	TS	16	5	**HM6508-2**	**† Harris (3965)**	
							(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY–RAMs (Cont'd)

Static (Cont'd)

Organi-zation	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	
1024x1	250 nsF	CMOS	TS	16	5			(Cont'd)
						HM6508-8	**† Harris**	**(3965)**
						HM6508-9	**Harris**	**(3965)**
						IM65X08	Intersil	
						IM65X08M	† Intersil	
						MCM6508-25	Motorola	
						CDP1821C	**RCA**	**(1594)**
				18	5	**HM6518-2**	**† Harris**	**(3965)**
						HM6518-8	**† Harris**	**(3965)**
						HM6518-9	**Harris**	**(3965)**
						IM65X18C	Intersil	
						IM65X18M	† Intersil	
						MCM6518-25	Motorola	
				48	5	HM92560-2	† Harris	
		NMOS	TS	16	5	2102H	Fairchild	
						2102HM	† Fairchild	
						2102LH	Fairchild	
						2102LHM	† Fairchild	
						21L02H	Fairchild	
						µPD2102AL-2	NEC	
						M2102A-2	SGS	
						M2102AL-2	SGS	
	260 nsF	CMOS	TS	16	5	**HS6508RH**	**† Harris**	**(4675)**
	300 nsF	CMOS	TS	16	5	S6508-1	AMI	
						HM6508-5	**Harris**	**(3965)**
						IM65X08C	Intersil	
						MCM6508-30	Motorola	
				18	5	**HM6518-5**	**Harris**	**(3965)**
						MCM6518-30	Motorola	
	350 nsF	CMOS	TS	16	4-11	S6508A	AMI	
		NMOS	TS	16	5	2102F	Fairchild	
						2102FM	† Fairchild	
						2102LF	Fairchild	
						2102LFM	† Fairchild	
						21L02F	Fairchild	
						M2102A	SGS	
						M2102AL	SGS	
	370 nsF	CMOS	TS	16	5	TC5508	Toshiba	
	400 nsF	NMOS	TS	16	5	MCM6508-40	Motorola	
	450 nsF	CMOS	TS	16	5	TC5508-4	Toshiba	
		NMOS	TS	16	5	21021	Fairchild	
						21021M	† Fairchild	
						2102L1	Fairchild	
						2102L1M	† Fairchild	
						21L021	Fairchild	
						µPD2102AL-4	NEC	
						M2102A-4	SGS	
						M2102AL-4	SGS	
	460 nsF	CMOS	TS	16	5	S6508	AMI	
				18	5	MCM6518-46	Motorola	
	550 nsF	CMOS	TS	16	5	TC5508-1	Toshiba	
	650 nsF	NMOS	TS	16	5	21022	Fairchild	
						21022M	† Fairchild	
						2102L2	Fairchild	
						2102L2M	† Fairchild	
						21L022	Fairchild	
						M2102A-6	SGS	
1024x4	10 nsF	ECL		24	−4.5	MBM100474A-10	Fujitsu	
					−5.2	MBM10474A-10	Fujitsu	
	15 nsF	ECL	OE	24	−4.5	**AM100474A**	**AMD**	**(3912)**
						MBM100474-15	Fujitsu	
						HD100474-1	Hitachi	
					−5.2	**AM10474AC**	**AMD**	**(3911)**
								(Continued)
1024x4	15 nsF	ECL	OE	24	−5.2			(Cont'd)
						MBM10474-15	Fujitsu	
						MCM10474A	**Motorola**	**(4047)**
						DM10474A	National	
	20 nsF	ECL	OE	24	−4.5	MBM100474-20	Fujitsu	
					−5.2	**AM10474AM**	**† AMD**	**(3911)**
	25 nsF	CMOS	TS	18	5	C42148-25	Cypress	
		ECL	OE	24	−4.5	**AM100474**	**AMD**	**(3912)**
						HD100474	Hitachi	
					−5.2	**AM10474C**	**AMD**	**(3911)**
						MCM10474	**Motorola**	**(4047)**
						DM10474	National	
						GXB100474	Siemens	
		NMOS	TS	24	5	**AM9150-25**	**AMD**	**(3921)**
	30 nsF	ECL	OE	24	−4.5	F100474	Fairchild	
					−5.2	**AM10474M**	**† AMD**	**(3911)**
						F10474C	Fairchild	
	35 nsF	CMOS	TS	18	5	C42148-35	Cypress	
						HM6148-35	Hitachi	
		NMOS	TS	18	5	AM2148-35	AMD	
						AM2149-35	AMD	
						µPD2149-2	**NEC**	**(4083)**
				24	5	**AM9150-35**	**AMD**	**(3921)**
						AM9150-35M	**† AMD**	**(3921)**
	45 nsF	CMOS	TS	18	5	C42148-45	Cypress	
						HM6148-45	Hitachi	
		NMOS	TS	18	5	AM2148-45	AMD	
						AM2148-45M	† AMD	
						AM2149-45	AMD	
						AM2149-45M	† AMD	
						AM21L48-45	AMD	
						AM21L49-45	AMD	
						2148H-2	Intel	
						2149H-2	Intel	
						µPD2149-1	**NEC**	**(4083)**
						SY2148H-2	**Synertek**	**(4210)**
						SY2149H-2	**Synertek**	**(4210)**
				24	5	**AM9150-45**	**AMD**	**(3921)**
						AM9150-45M	**† AMD**	**(3921)**
		TTL	TS	18	5	93475	Fairchild	
	55 nsF	CMOS	TS	18	5	C42148-55	Cypress	
						HM6148-55	Hitachi	
		MNOS	TS	18	5	HM2148-3	Hitachi	
		NMOS	TS	18	5	AM2148-55M	† AMD	
						AM2148-55	AMD	
						AM2148-55M	† AMD	
						AM2149-55	AMD	
						AM2149-55M	† AMD	
						AM21L48-55	AMD	
						AM21L49-55	AMD	
						2148H-3	Intel	
						2148HL-3	Intel	
						2149H-3	Intel	
						NMC2148-3	National	
						µPD2149	**NEC**	**(4083)**
						SY2148H-3	**Synertek**	**(4210)**
						SY2148HL-3	**Synertek**	**(4210)**
						SY2149H-3	**Synertek**	**(4210)**
						SY2149HL-3	**Synertek**	**(4210)**
						SYM2148H-3	**† Synertek**	**(535)**
						SYM2149H-3	**† Synertek**	**(535)**
	70 nsF	CMOS	TS	18	5	HM6148	Hitachi	
						HM6148L	Hitachi	
		NMOS	TS	18	5	AM2148-70	AMD	
						AM2148-70M	† AMD	
						AM2149-70	AMD	
						AM2149-70M	† AMD	
						AM21L48-70	AMD	
								(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

Master Selection Guide

MEMORY

MEMORY–RAMs (Cont'd)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	
1024x4	70 nsF	NMOS	TS	18	5			(Cont'd)
						AM21L49-70	AMD	
						2148H	Intel	
						2148HL	Intel	
						2149H	Intel	
						2149HL	Intel	
						M2148H	† Intel	
						NMC2148	National	
						NMC2148H	National	
						NMC2148L	National	
						SY2148H	**Synertek**	**(4210)**
						SY2148HL	**Synertek**	**(4210)**
						SY2149H	**Synertek**	**(4210)**
						SY2149HL	**Synertek**	**(4210)**
						SYM2148H	**† Synertek**	**(535)**
						SYM2149H	**† Synertek**	**(535)**
	85 nsF	CMOS	TS	18	5	HM6148-6	Hitachi	
		NMOS	TS	18	5	**SYM2148H-6**	**† Synertek**	**(535)**
						SYM2149H-6	**† Synertek**	**(535)**
	100 nsF	CMOS	TS	18	5	MD21SC14-10	Mitel	
						SCM21C14-1	SSS	
		NMOS	TS	18	5	2114AL-1	Intel	
						SY2114AL-1	**Synertek**	**(4210)**
	120 nsF	CMOS	TS	18	5	**HM6514S-2**	**† Harris**	**(3966)**
						HM6514S-8	**† Harris**	**(3966)**
						HM6514S-9	**Harris**	**(3966)**
						SCM21C14-2	SSS	
		NMOS	TS	18	5	2114AL-2	Intel	
						SY2114AL-2	**Synertek**	**(4210)**
	150 nsF	CMOS	TS	18	5	MD21SC14-15	Mitel	
						SCM21C14-3	SSS	
		NMOS	TS	18	5	HM472114A-1	Hitachi	
						2114AL-3	Intel	
						M2114AL-3	† Intel	
						MM2114-15	National	
						NMC2114A-3	National	
						NMC2114A-3L	National	
						SY2114AL-3	**Synertek**	**(4210)**
						SYM2114A-3	**† Synertek**	**(535)**
						TMS2114-15	TI	
						TMS2114L-15	TI	
	170 nsF	CMOS	TS	18	5	IM6514C	Intersil	
						IM6514M	† Intersil	
	200 nsF	CMOS	TS	18	5	**HM6514B-9**	**Harris**	**(3966)**
						HS6514RH	**† Harris**	**(4682)**
						μPD444-3	NEC	
						μPD444/6514-3	NEC	
						MSM5114-2	**OKI**	**(4118)**
						MWS5114-3	**† RCA**	**(1594)**
						SCM21C14-4	SSS	
						TC5514A-2	Toshiba	
						TC5514AL-2	Toshiba	
		NMOS	TS	18	5	AM9114E	AMD	
						AM9114EM	† AMD	
						AM91L14E	AMD	
						AM91L14EM	† AMD	
						2114-2	Fairchild	
						2114L-2	Fairchild	
						HM472114A-2	Hitachi	
						2114AL-4	Intel	
						M2114A-4	† Intel	
						M2114AL-4	† Intel	
						M5L2114L-2	Mitsubishi	
						MCM2114-20	**Motorola**	**(4046)**
						MCM21L14-20	**Motorola**	**(4046)**
						MM2114-2	National	
						MM2114-2L	National	
								(Continued)
1024x4	200 nsF	NMOS	TS	18	5			(Cont'd)
						NMC2114A-4	National	
						NMC2114A-4L	National	
						SY2114-2	**Synertek**	**(4210)**
						SY2114A-4	**Synertek**	**(4210)**
						SY2114AL-4	**Synertek**	**(4210)**
						SY2114L-2	**Synertek**	**(4210)**
						SY2114LV-2	**Synertek**	**(4210)**
						SYM2114A-4	**† Synertek**	**(535)**
						TMS2114-20	TI	
						TMS2114L-20	TI	
						TMM314A-1	Toshiba	
						TMM314AL-1	Toshiba	
				20	5	SY2142-2	Synertek	
						SY2142L-2	Synertek	
				22	5	AM9130E	AMD	
	220 nsF	CMOS	TS	18	5	**HM6514B-2**	**† Harris**	**(3966)**
						HM6514B-8	**† Harris**	**(3966)**
	250 nsF	CMOS	TS	18	5	MP2114C	MicroPwr	
						MP6514	MicroPwr	
						MD21SC14-25	Mitel	
						μPD444/6514-2	NEC	
						MWS5114-2	**† RCA**	**(1594)**
						SRM2114	S MOS	
						SRM6514	S MOS	
		NMOS	TS	18	5	M2114A-5	† Intel	
						MCM2114-25	**Motorola**	**(4046)**
						MCM21L14-25	**Motorola**	**(4046)**
						NMC2114A-5	National	
						SY2114A-5	**Synertek**	**(4210)**
						SYM2114A-5	**† Synertek**	**(535)**
						TMS2114-25	TI	
						TMS2114L-25	TI	
				22	5	AM9130D	AMD	
	300 nsF	CMOS	TS	18	5	S6514	AMI	
						HM6514-2	**† Harris**	**(3966)**
						HM6514-9	**Harris**	**(3966)**
						HM6514C-9	**Harris**	**(3966)**
						HM4334-3	Hitachi	
						NMC6514-2	† National	
						NMC6514-9	National	
						μPD444/6514-1	NEC	
						CMM5114/1RZ	RCA	
						MWS5114-1	**† RCA**	**(1594)**
						TC5514A-3	Toshiba	
						TC5514AL-3	Toshiba	
		NMOS	TS	18	5	AM9114C	AMD	
						AM9114CM	† AMD	
						AM9124C	AMD	
						AM9124CM	† AMD	
						AM91L14C	AMD	
						AM91L14CM	† AMD	
						AM91L24C	AMD	
						AM91L24CM	† AMD	
						2114-3	Fairchild	
						2114-3M	† Fairchild	
						2114L-3	Fairchild	
						HM472114-3	Hitachi	
						M5L2114L-3	Mitsubishi	
						MCM2114-30	**Motorola**	**(4046)**
						MCM21L14-30	**Motorola**	**(4046)**
						MM2114-3	National	
						MM2114-3L	National	
						SY2114-3	**Synertek**	**(4210)**
						SY2114L-3	**Synertek**	**(4210)**
						SYM2114-3	**† Synertek**	**(535)**
				20	5	SY2142-3	Synertek	
						SY2142L-3	Synertek	
								(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

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MEMORY

MEMORY-RAMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source
Static							**(Cont'd)**
1024x4	300 nsF	NMOS	TS				(Cont'd)
				22	5	AM9130C	AMD
						AM9130CM	† AMD
						AM91L30C	AMD
						AM91L30CM	† AMD
	350 nsF	CMOS	TS	18	5	**HM6514-5**	**Harris (3966)**
						NMC6514-5	National
	400 nsF	NMOS	TS	22	5	AM9130B	AMD
						AM9130BM	† AMD
						AM91L30B	AMD
						AM91L30BM	† AMD
	450 nsF	CMOS	TS	18	5	HM4334-4	Hitachi
						M58981-45	Mitsubishi
						μPD444/6514	NEC
				20	5	μPD445L	NEC
						TC5514	Toshiba
		NMOS	TS	18	5	AM9114B	AMD
						AM9114BM	† AMD
						AM9124B	AMD
						AM9124BM	† AMD
						AM91L14B	AMD
						AM91L14BM	† AMD
						AM91L24B	AMD
						AM91L24BM	† AMD
						2114	Fairchild
						2114L	Fairchild
						2114M	† Fairchild
						HM472114-4	Hitachi
						M5L2114L	Mitsubishi
						MCM2114-45	**Motorola (4046)**
						MCM21L14-45	**Motorola (4046)**
						MM2114	National
						MM2114L	National
						EA2114L	NEC
						μPD2114L	NEC
						SY2114	**Synertek (4210)**
						SY2114L	**Synertek (4210)**
						SYM2114	**† Synertek (535)**
						TMS2114-45	TI
						TMS2114L-45	TI
						TMM314A	Toshiba
						TMM314AL	Toshiba
				20	5	SY2142	Synertek
						SY2142L	Synertek
	500 nsF	NMOS	TS	22	5	AM9130A	AMD
						AM9130AM	† AMD
						AM91L30A	AMD
						AM91L30AM	† AMD
	550 nsF	CMOS	TS	20	5	TC5047A-1	Toshiba
	650 nsF	CMOS	TS	20	5	μPD445L-1	NEC
						TC5514-1	Toshiba
	800 nsF	CMOS	TS	20	5	TC5047A-2	Toshiba
						TC5514-2	Toshiba
	1000 nsF						
		CMOS	TS	18	1-1.7	MP2114CLP1	MicroPwr
						MP6514LP1	MicroPwr
					3-5	MP2114CLP3	MicroPwr
1024x8	55 nsF	NMOS	TS	24	5	MK4801A-55	Mostek
	70 nsF	NMOS	TS	24	5	MK4801A-70	Mostek
						MKB4801A-870	† Mostek
	90 nsF	NMOS	TS	24	5	MK4801A-90	Mostek
						MKB4801A-890	† Mostek
						SY2158A-1	**Synertek (4210)**
						SY2158B-1	**Synertek (4210)**
						SY2158L-1	**Synertek (4210)**
						SY2159A-1	**Synertek (4210)**
							(Continued)
1024x8	90 nsF	NMOS	TS	24	5		(Cont'd)
						SY2159B-1	**Synertek (4210)**
						SY2159L-1	**Synertek (4210)**
	100 nsF	Dual Port					
			—	48	5	SY21D1	Synertek
		NMOS	—	48	5	SYM21D1	† Synertek
			TS	48	5	**SY2130**	**Synertek (4210)**
						SY2131	**Synertek (4210)**
	120 nsF	NMOS	TS	24	5	MK4118A-1	Mostek
						MKB4801A-81	† Mostek
						SY2158A-2	**Synertek (4210)**
						SY2158B-2	**Synertek (4210)**
						SY2158L-2	**Synertek (4210)**
						SY2159A-2	**Synertek (4210)**
						SY2159B-2	**Synertek (4210)**
						SY2159L-2	**Synertek (4210)**
	150 nsF	NMOS	TS	22	5	μPD421-5	NEC
				24	5	MK4118A-2	Mostek
						SY2158A-3	**Synertek (4210)**
						SY2158B-3	**Synertek (4210)**
						SY2158B-4	**Synertek (4210)**
						SY2158L-3	**Synertek (4210)**
						SY2159A-3	**Synertek (4210)**
						SY2159B-3	**Synertek (4210)**
						SY2159L-3	**Synertek (4210)**
	200 nsF	NMOS	TS	22	5	μPD421-3	NEC
				24	5	MK4118A-3	Mostek
						SY2158A-4	**Synertek (4210)**
						SY2158L-4	**Synertek (4210)**
						SY2159A-4	**Synertek (4210)**
						SY2159B-4	**Synertek (4210)**
						SY2159L-4	**Synertek (4210)**
	250 nsF	NMOS	TS	22	5	μPD421-2	NEC
				24	5	MK4118A-4	Mostek
	300 nsF	NMOS	TS	22	5	μPD421-1	NEC
						R8104-3	Rockwell
	400 nsF	NMOS	TS	22	5	R8114-3	Rockwell
	450 nsF	NMOS	TS	22	5	μPD421	NEC
2048x1	300 nsF	CMOS	TS	18	5	NMC6503-9	† National
	350 nsF	CMOS	TS	18	5	NMC6503-5	National
2048x8	45 nsF	NMOS	TS	24	5	**MCM2016H-45**	**Motorola (4046,4052)**
	55 nsF	CMOS	TS	24	5	**HM65162S-5**	**Harris (3966)**
						HM65162S-9	**Harris (3966)**
						HM65172S-5	**Harris (3967)**
						HM65172S-9	**Harris (3967)**
		NMOS	TS	24	5	**MCM2016H-55**	**Motorola (4046,4052)**
	70 nsF	CMOS	TS	24	5	**HM65162B-2**	**† Harris (3966)**
						HM65162B-5	**Harris (3966)**
						HM65162B-8	**† Harris (3966)**
						HM65162B-9	**Harris (3966)**
						HM65172B-2	**† Harris (3967)**
						HM65172B-5	**Harris (3967)**
						HM65172B-8	**† Harris (3967)**
						HM65172B-9	**Harris (3967)**
						IDT6116S70	**IDT (3982)**
						MP6116S-1	MicroPwr
						MP6117S-1	MicroPwr
						MP6118S-1	MicroPwr
						NC6116	Nitron
		NMOS	TS	24	5	**AM9128-70**	**AMD (3917)**
						MCM2016H-70	**Motorola (4046,4052)**
	90 nsF	CMOS	TS	24	5	**HM65162-2**	**† Harris (3966)**
						HM65162-5	**Harris (3966)**
						HM65162-8	**† Harris (3966)**
						HM65162-9	**Harris (3966)**
						HM65162C-9	**Harris (3966)**
							(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

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MEMORY

MEMORY–RAMs (Cont'd)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	
2048x8	90 nsF	CMOS	TS	24	5			(Cont'd)
						HM65172-2	† **Harris**	**(3967)**
						HM65172-5	**Harris**	**(3967)**
						HM65172-8	† **Harris**	**(3967)**
						HM65172-9	**Harris**	**(3967)**
						HM65172C-9	**Harris**	**(3967)**
						IDT6116L90	† **IDT**	**(3982)**
						IDT6116L90	IDT	
						IDT6116S90	† **IDT**	**(3982)**
						IDT6116S90	IDT	
	100 nsF	CMOS	TS	24	5	HM6116-10	Hitachi	
		NMOS	TS	24	5	**AM9128-10**	**AMD**	**(3917)**
						F3528-10	Fairchild	
						F3528L-10	Fairchild	
						MB8128-10	Fujitsu	
						SY2128-1	**Synertek**	**(4210)**
						SY2128L-1	**Synertek**	**(4210)**
						SY2129-1	**Synertek**	**(4210)**
						SY2129L-1	**Synertek**	**(4210)**
	120 nsF	CMOS	TS	24	5	MB8416A-12	Fujitsu	
						MB8416A-12L	Fujitsu	
						HM65162C-2	† **Harris**	**(3966)**
						HM65162C-8	† **Harris**	**(3966)**
						HM65168-2	† **Harris**	**(3966)**
						HM65168-8	† **Harris**	**(3966)**
						HM65168-9	**Harris**	**(3966)**
						HM65172C-2	† **Harris**	**(3967)**
						HM65172C-8	† **Harris**	**(3967)**
						HM6116-2	Hitachi	
						HM6116L-2	Hitachi	
						IDT6116L120	† **IDT**	**(3982)**
						IDT6116L120	IDT	
						IDT6116S120	† **IDT**	**(3982)**
						IDT6116S120	IDT	
						MP6116S-12	MicroPwr	
						MP6117S-12	MicroPwr	
						MP6118S-12	MicroPwr	
						MCM6116-12	**Motorola**	**(4046)**
						MCM61L16-12	Motorola	
						SCM6116-2	SSS	
						TMS4016-12	TI	
		NMOS	TS	24	5	**AM9128-12M**	† **AMD**	**(3917)**
						F3528-12	Fairchild	
						F3528L-12	Fairchild	
						MKB4802-81	† Mostek	
						SY2128-2	**Synertek**	**(4210)**
						SY2128L-2	**Synertek**	**(4210)**
						SY2129-2	**Synertek**	**(4210)**
						SY2129L-2	**Synertek**	**(4210)**
	150 nsF	CMOS	TS	24	5	S6516	AMI	
						MB8416A-15	Fujitsu	
						MB8416A-15L	Fujitsu	
						HM6116-15	Hitachi	
						HM6116-3	Hitachi	
						HM6117-3	Hitachi	
						IDT6116L150	† **IDT**	**(3982)**
						IDT6116L150	IDT	
						IDT6116S150	† **IDT**	**(3982)**
						IDT6116S150	IDT	
						MP6116S-15	MicroPwr	
						MP6117S-15	MicroPwr	
						MP6118S-15	MicroPwr	
						MKB6116-82	† Mostek	
						MKB6116L-82	† Mostek	
						MCM6116-15	**Motorola**	**(4046)**
						MCM61L16-15	Motorola	
						μPD446-3	**NEC**	**(4090)**
						μPD449-3	**NEC**	**(4093)**
								(Continued)
2048x8	150 nsF	CMOS	TS	24	5			(Cont'd)
						CDM6116A-3	**RCA**	**(1594)**
						SCM6116-3	SSS	
		NMOS	TS	24	5	**AM9128**	**AMD**	**(3917)**
						AM9128-15M	† **AMD**	**(3917)**
						F3528-15	Fairchild	
						F3528L-15	Fairchild	
						MB8128-15	Fujitsu	
						M58275-15	Mitsubishi	
						NMC2116-15	National	
						NMC2116-15L	National	
						μPD4016-3	**NEC**	**(4088)**
						SY2128-3	**Synertek**	**(4210)**
						SY2128L-3	**Synertek**	**(4210)**
						SY2129-3	**Synertek**	**(4210)**
						SY2129L-3	**Synertek**	**(4210)**
						SYM2128-3	† **Synertek**	**(535)**
						SYM2129-3	† **Synertek**	**(535)**
						TMS4016-15	TI	
						TMM2016	Toshiba	
	200 nsF	CMOS	TS	24	5	MB8416	Fujitsu	
						MB8417	Fujitsu	
						MB8418	Fujitsu	
						HM6516-2	† **Harris**	**(3966)**
						HM6516-5	**Harris**	**(3966)**
						HM6516-8	† **Harris**	**(3966)**
						HM6516-9	**Harris**	**(3966)**
						HM6116-20	Hitachi	
						HM6116-4	Hitachi	
						HM6116L-4	Hitachi	
						HM6117-4	Hitachi	
						MP6116-20	MicroPwr	
						MP6117-20	MicroPwr	
						MP6118-20	MicroPwr	
						MP8416-20	MicroPwr	
						MP8417-20	MicroPwr	
						MP8418-20	MicroPwr	
						MKB6116-83	† Mostek	
						MKB6116L-83	† Mostek	
						MCM6116-20	**Motorola**	**(4046)**
						MCM61L16-20	Motorola	
						μPD446-2	**NEC**	**(4090)**
						μPD449-2	**NEC**	**(4093)**
						MSM5128	**OKI**	**(4118)**
						CDM6116-2	**RCA**	**(1594)**
						CDM6117-2	**RCA**	**(1594)**
						CDM6118-2	**RCA**	**(1594)**
						SRM2016C20	SMOS	
						SRM2017C20	SMOS	
						SRM2018C20	SMOS	
						SCM6116-4	SSS	
						TC5516A-2	Toshiba	
						TC5516AL-2	Toshiba	
		NMOS	TS	24	5	**AM9128-20**	**AMD**	**(3917)**
						AM9128-20M	† **AMD**	**(3917)**
						F3528-20	Fairchild	
						F3528L-20	Fairchild	
						M58725	Mitsubishi	
						MCM2016-20	**Motorola**	**(4046,4052)**
						NMC2116-20L	National	
						NMC2116-25L	National	
						μPD4016-2	**NEC**	**(4088)**
						SY2128-4	**Synertek**	**(4210)**
						SY2128L-4	**Synertek**	**(4210)**
						SY2129-4	**Synertek**	**(4210)**
						SY2129L-4	**Synertek**	**(4210)**
						SYM2128-4	† **Synertek**	**(535)**
						SYM2129-4	† **Synertek**	**(535)**
						TMS4016-20	TI	
						TMM2016-2	Toshiba	
								(Continued)

† Military Temperature Range (−55° to 125°C)   * Typical Value

Bold face indicates additional data is provided on the page noted.

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MEMORY

MEMORY-RAMs (Cont'd)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source
2048x8							(Cont'd)
	250 nsF	CMOS	TS	24	5	MB8416-25W †	Fujitsu
						MP6116-25	MicroPwr
						MP6117-25	MicroPwr
						MP6118-25	MicroPwr
						MP8416-25	MicroPwr
						MP8417-25	MicroPwr
						MP8418-25	MicroPwr
						MKB6116-84 †	Mostek
						MKB6116L-84 †	Mostek
						μPD446-1	**NEC (4090)**
						μPD449-1	**NEC (4093)**
						CDM6116-1	**RCA (1594)**
						CDM6116A-9	**RCA (1594)**
						CDM6117-1	**RCA (1594)**
						CDM6118-1	**RCA (1594)**
						SRM2016C25	S MOS
						SRM2017C25	S MOS
						SRM2018C25	S MOS
						TC5516A	Toshiba
						TC5517A	Toshiba
						TC5517A-2	Toshiba
						TC5518B-2	Toshiba
		NMOS	TS	24	5	NMC2116-25	National
						μPD4016-1	**NEC (4088)**
						TMS4016-25	TI
	350 nsF	NMOS	TS	24	5	F3528-35	Fairchild
	450 nsF	CMOS	TS	24	5	**μPD446**	**NEC (4090)**
						μPD449	**NEC (4093)**
4096x1	10 nsF	ECL	OE	18	−5.2	MBM100470A-10	Fujitsu
						MBM10470A-10	Fujitsu
				20	−5.2	HM2142	Hitachi
	15 nsF	ECL	OE	16	−5.2	HM10470-1	Hitachi
						MCM10470A	**Motorola (4047)**
				18	−4.5	**AM100470SA**	**AMD (3914)**
						HM100470-1	Hitachi
					−5.2	**AM10470SAC**	**AMD (3913)**
						MBM10470A-15	Fujitsu
						DM10470A	National
	20 nsF	ECL	OE	18	−4.5	MBM100470	Fujitsu
					−5.2	**AM10470SAM** †	**AMD (3913)**
						MBM10470A-20	Fujitsu
	25 nsF	ECL	OE	18	−4.5	**AM100470A**	**AMD (3914)**
						F100470A	Fairchild
						HM100470	Hitachi
						100470A	Signetics
					−5.2	**AM10470AC**	**AMD (3913)**
						F10470A	Fairchild
						HM10470	Hitachi
						MCM10470	**Motorola (4047)**
						DM10470	National
						~~DM10470L~~	~~National~~
						10470A	Signetics
		NMOS	TS	18	5	μPD2147A-25	NEC
	30 nsF	ECL	OE	18	−5.2	**AM10470AM** †	**AMD (3913)**
	35 nsF	CMOS	TS	18	5	HM6147H-35	Hitachi
		ECL	OE	18	−4.5	**AM100470**	**AMD (3914)**
						F100470	Fairchild
						100470	Signetics
					−5.2	**AM10470C**	**AMD (3913)**
						F10470	Fairchild
						10470	Signetics
		NMOS	TS	18	5	AM2147-35	AMD
							(Continued)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source
4096x1	35 nsF	NMOS	TS	18	5		(Cont'd)
						2147H-1	Intel
						μPD2147A-35	NEC
						SY2147H-1	**Synertek (4210)**
	40 nsF	ECL	OE	18	−4.5	**AM10470M** †	**AMD (3913)**
	45 nsF	CMOS	TS	18	5	HM6147-45	Hitachi
		NMOS	TS	18	5	AM2147-45	AMD
						AM2147-45M †	AMD
						AM21L47-45	AMD
						HM4847-2	Hitachi
						2147H-2	Intel
						M2147H-2 †	Intel
						MM2148H-2	National
						μPD2147A-45	NEC
						SY2147H-2	**Synertek (4210)**
						SYM2147H-2 †	**Synertek (535)**
	55 nsF	CMOS	TS	18	5	HM6147-3	Hitachi
						HM6147-55	Hitachi
						MCM6147-55	**Motorola (4046)**
						~~MCM61L47-55~~	~~Motorola~~
		NMOS	TS	18	5	AM2147-55	AMD
						AM2147-55M †	AMD
						AM21L47-55	AMD
						HM4847-3	Hitachi
						2147-3	Intel
						2147A-3	Intel
						2147AL-3	Intel
						2147H-3	Intel
						2147HL-3	Intel
						M2147H-3 †	Intel
						ITT2147-55	ITT
						MCM2147-55	Motorola
						MM2147-3	National
						MM2148H-3	National
						MM2148H-3L	National
						NMC2147H-3	National
						NMC2147H-4	National
						μPD2147-3	NEC
						SY2147-3	**Synertek (4210)**
						SY2147H-3	**Synertek (4210)**
						SY2147HL-3	**Synertek (4210)**
						SYM2147-3 †	**Synertek (535)**
						SYM2147-6 †	**Synertek (535)**
						SYM2147H-3	**Synertek (535)**
						TMM315-1	Toshiba
						UM2147-1	Universal
	70 nsF	CMOS	TS	18	5	HM6147	Hitachi
						HM6147L	Hitachi
						MCM6147-70	**Motorola (4046)**
						MCM61L47-70	Motorola
		NMOS	TS	18	5	AM2147-70	AMD
						AM2147-70M †	AMD
						AM21L47-70	AMD
						HM4847	Hitachi
						2147A	Intel
						2147AL	Intel
						2147H	Intel
						2147HL	Intel
						M2147H †	Intel
						2147	Intersil
						ITT2147-70	ITT
						MCM2147-70	Motorola
						MM2147	National
						MM2147L	National
						MM2148H	National
						MM2148H-L	National
						μPD2147-2	NEC
						SY2147H	**Synertek (4210)**
							(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY-RAMs (Cont'd)

Organi-zation	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	
Static						**(Cont'd)**		
4096x1	70 nsF	NMOS	TS	18	5			(Cont'd)
						SY2147HL	**Synertek**	**(4210)**
						SYM2147	**† Synertek**	**(535)**
	85 nsF	CMOS	TS	18	5	TMM315	Toshiba	
		NMOS	TS	18	5	HM6147-6	Hitachi	
						MCM2147-85	Motorola	
						MM2147M	† National	
						SY2147-6	**Synertek**	**(4210)**
4096x1	90 nsF	NMOS	TS	18	5	ITT2147-90	ITT	
	100 nsF	NMOS	TS	18	5	MCM2147-100	Motorola	
						µPD2147	NEC	
	120 nsF	CMOS	TS	18	5	**HM6504S-2**	**† Harris**	**(3966)**
						HM6504S-8	**† Harris**	**(3966)**
						HM6504S-9	**Harris**	**(3966)**
		NMOS	TS	18	5	AM21L41-12	AMD	
						2141-2	Intel	
						NMC2141-2	National	
						TMS4044-12	TI	
						TMS40L44-12	TI	
	150 nsF	NMOS	TS	18	5	AM21L41-15	AMD	
						2141-3	Intel	
						2141L-3	Intel	
						NMC2141-3	National	
	180 nsF	CMOS	TS	18	5	**HS6504RH**	**† Harris**	**(4668)**
	200 nsF	CMOS	TS	18	5	**HM6504B-8**	**† Harris**	**(3966)**
						HM6504B-9	**Harris**	**(3966)**
						IM6504C	Intersil	
						IM6504M	† Intersil	
						TC5504A-2	Toshiba	
		NMOS	TS	18	5	AM21L41-20	AMD	
						AM9044E	AMD	
						AM9244E	AMD	
						2141-4	Intel	
						2141L-4	Intel	
						IM7141-2	Intersil	
						IM7141-2M	† Intersil	
						IM7141L-2	Intersil	
						M5T4044-20	Mitsubishi	
						MK4104-3	Mostek	
						MK4104-33	Mostek	
						MCM6641-20	Motorola	
						MCM66L41-20	Motorola	
						µPD4104-2	NEC	
						TMS4044-20	TI	
						TMS40L44-20	TI	
				22	5	AM9140E	AMD	
	220 nsF	CMOS	TS	18	5	**HM6504B-2**	**† Harris**	**(3966)**
	250 nsF	CMOS	TS	18	5	MP6504	MicroPwr	
						SRM6504	S MOS	
		NMOS	TS	18	5	AM21L41-25	AMD	
						AM9044D	AMD	
						AM9044DM	† AMD	
						AM90L44D	AMD	
						AM9244D	AMD	
						AM9244DM	† AMD	
						AM92L44D	AMD	
						2141-5	Intel	
						2141L-5	Intel	
						MK4104-34	Mostek	
						MK4104-4	Mostek	
						MKB4104-84	† Mostek	
						MCM6641-25	Motorola	
						MCM66L41-25	Motorola	
						MM5257-25	National	
						MM5257-25L	National	
						µPD4104-1	NEC	
								(Continued)
4096x1	250 nsF	NMOS	TS	18	5			(Cont'd)
						TMS4044-25	TI	
						TMS40L44-25	TI	
				22	5	AM9140D	AMD	
	300 nsF	CMOS	TS	18	5	**HM6504-2**	**† Harris**	**(3966)**
						HM6504-8	**† Harris**	**(3966)**
						HM6504-9	**Harris**	**(3966)**
						HM6504C-9	**Harris**	**(3966)**
						NMC6404-9	National	
						NMC6504-2	† National	
						NMC6504-9	National	
						CMM5104/1RZ	RCA	
						TC5504A-3	Toshiba	
		NMOS	TS	18	5	AM4044C	AMD	
						AM4244C	AMD	
						AM9044CM	† AMD	
						AM90L44C	AMD	
						AM90L44CM	† AMD	
						AM9244CM	† AMD	
						AM92L44C	AMD	
						AM92L44CM	† AMD	
						IM7141-3	Intersil	
						IM7141-3M	† Intersil	
						IM7141L-3	Intersil	
						M5T4044-30	Mitsubishi	
						MK4104-35	Mostek	
						MK4104-5	Mostek	
						MKB4104-85	† Mostek	
						MCM6641-30	Motorola	
						MCM66L41-30	Motorola	
						MM5257-3	National	
						MM5257-3L	National	
						µPD4104	NEC	
				22	5	AM9140C	AMD	
						AM9140CM	† AMD	
						AM91L40C	AMD	
						AM91L40CM	† AMD	
	320 nsF	CMOS	TS	18	5	S6504	AMI	
	350 nsF	CMOS	TS	18	5	**HM6504-5**	**Harris**	**(3966)**
						NMC6504-5	National	
		NMOS	TS	18	5	MK4104-6	Mostek	
						MKB4104-86	† Mostek	
	400 nsF	NMOS	TS	22	5	AM9140B	AMD	
						AM9140BM	† AMD	
						AM91L40B	AMD	
						AM91L40BM	† AMD	
	450 nsF	CMOS	TS	18	5	HM4315	Hitachi	
		NMOS	TS	18	5	AM9044B	AMD	
						AM9044BM	† AMD	
						AM90L44B	AMD	
						AM90L44BM	† AMD	
						AM9244B	AMD	
						AM9244BM	† AMD	
						AM92L44B	AMD	
						AM92L44BM	† AMD	
						IM7141	Intersil	
						IM7141L	Intersil	
						IM7141M	† Intersil	
						MCM6641-45	Motorola	
						MCM66L41-45	Motorola	
						MM5257	National	
						MM5257L	National	
						TMS4044-45	TI	
						TMS40L44-45	TI	
	500 nsF	NMOS	TS	22	5	AM9140A	AMD	
						AM9140AM	† AMD	
						AM91L40A	AMD	
						AM91L40AM	† AMD	
								(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY–RAMs (Cont'd)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source
4096x1							(Cont'd)
	550 nsF	CMOS	TS	18	5	TC5504-1	Toshiba
	800 nsF	CMOS	TS	18	5	TC5504-2	Toshiba
	1000 nsF	CMOS	TS	18	1-1.7	MP6504LP1	MicroPwr
4096x4	40 nsF	NMOS	TS	20	5	IMS1421-40	Inmos (3978)
	45 nsF	CMOS	TS	20	5	HM6168-45	Hitachi (3972)
						HM6168H-45	Hitachi (3972)
						IDT6168L45	† IDT (3993)
						IDT6168L45	IDT
						IDT6168S45	† IDT (3993)
						IDT6168S45	IDT
				24	5	IDT71681L45	† IDT (3993)
						IDT71681L45	IDT
						IDT71681S45	† IDT (3993)
						IDT71681S45	IDT
						IDT71682L45	IDT (3993)
						IDT71682S45	IDT (3993)
		NMOS	TS	20	5	AM2168-45	AMD (3920)
						AM2169-45	AMD (3920)
						MB8168-45	Fujitsu
						IMS1420-45	Inmos (501,3978)
	50 nsF	NMOS	TS	20	5	IMS1421-50	Inmos (3978)
	55 nsF	CMOS	TS	20	5	HM6168-55	Hitachi (3972)
						HM6168H-55	Hitachi (3972)
						IDT6168L55	† IDT (3993)
						IDT6168L55	IDT
						IDT6168S55	† IDT (3993)
						IDT6168S55	IDT
				24	5	IDT71681L55	† IDT (3993)
						IDT71681L55	IDT
						IDT71681S55	† IDT (3993)
						IDT71681S55	IDT
						IDT71682L55	† IDT
						IDT71682L55	IDT
						IDT71682S55	† IDT (3993)
						IDT71682S55	IDT
		NMOS	TS	20	5	AM2168-55	AMD (3920)
						AM2168-55M	† AMD (3920)
						AM2169-55	AMD (3920)
						AM2169-55M	† AMD (3920)
						IMS1420-55	Inmos (501,3978)
						IMS1420-55M	† Inmos (501,3978)
						SY2168-3	Synertek (4210)
						SY2169-3	Synertek (4210)
	70 nsF	CMOS	TS	20	5	HM6168-70	Hitachi (3972)
						HM6168H-70	Hitachi (3972)
						IDT6168L70	† IDT (3993)
						IDT6168L70	IDT
						IDT6168S70	† IDT (3993)
						IDT6168S70	IDT
				24	5	IDT71681L70	† IDT (3993)
						IDT71681L70	IDT
						IDT71681S70	† IDT (3993)
						IDT71681S70	IDT
						IDT71682L70	† IDT (3993)
						IDT71682L70	IDT
						IDT71682S70	† IDT (3993)
						IDT71682S70	IDT
		NMOS	TS	20	5	AM2168-70	AMD (3920)
						AM2168-70M	† AMD (3920)
						AM2169-70	AMD (3920)
						AM2169-70M	† AMD (3920)
						MB8168-70	Fujitsu
						MB8168-70W	† Fujitsu
						IMS1420-70L	Inmos (501,3978)
						IMS1420-70M	† Inmos (501,3978)
							(Continued)
4096x4	70 nsF	NMOS	TS	20	5		(Cont'd)
						IMS1420L	Inmos (501,3978)
						SY2168	Synertek (4210)
						SY2169	Synertek (4210)
						SYM2168	† Synertek (535)
						SYM2169	† Synertek (535)
	85 nsF	CMOS	TS	20	5	IDT6168L85	† IDT (3993)
						IDT6168L85	IDT
						IDT6168S85	† IDT (3993)
						IDT6168S85	IDT
				24	5	IDT71681L85	† IDT (3993)
						IDT71681L85	IDT
						IDT71681S85	† IDT (3993)
						IDT71681S85	IDT
						IDT71682L85	† IDT (3993)
						IDT71682L85	IDT
						IDT71682S85	† IDT (3993)
						IDT71682S85	IDT
		NMOS	TS	20	5	MBM8168-85W	† Fujitsu
	100 nsF	CMOS	TS	20	5	IDT6168L100	† IDT (3993)
						IDT6168L100	IDT
						IDT6168S100	IDT (3993)
				24	5	IDT71681L100	† IDT (3993)
						IDT71681L100	IDT
						IDT71681S100	† IDT (3993)
						IDT71681S100	IDT
						IDT71682L100	† IDT (3993)
						IDT71682L100	IDT
						IDT71682S100	† IDT (3993)
						IDT71682S100	IDT
		NMOS	TS	20	5	IMS1420-10L	Inmos (501,3978)
4096x8	200 nsF	NMOS	—	28	5	8148	Intel
8192x8	85 nsF	CMOS	TS	28	5	IDT7M864-85	IDT (4000)
						IDT8M864-85	IDT (4000)
	100 nsF	CMOS	TS	28	5	HM6264-10	Hitachi (3973)
						TC5564	Toshiba
						TC5564L	Toshiba
						TC5565	Toshiba
						TC5565L	Toshiba
	120 nsF	CMOS	TS	28	5	HM6264-12	Hitachi (3973)
						IDT7M864-120	IDT (4000)
						IDT7M864-120C	† IDT (4000)
						IDT8M864-120	IDT (4000)
						IDT8M864-120C	† IDT (4000)
	150 nsF	CMOS	TS	28	5	HM65642	† Harris
						HM6264-15	Hitachi (3973)
						IDT7M864-150	IDT (4000)
						IDT7M864-150C	† IDT (4000)
						IDT8M864-150	IDT (4000)
						IDT8M864-150C	† IDT (4000)
						TC5564-1	Toshiba
						TC5564L-1	Toshiba
						TC5565-1	Toshiba
		NMOS	TS	28	5	NMC4864	National
	200 nsF	CMOS	TS	28	5	IDT7M864-200	IDT (4000)
						IDT7M864-200C	† IDT (4000)
						IDT8M864-200	IDT (4000)
						IDT8M864-200C	† IDT (4000)
	250 nsF	NMOS	TS	28	5	2186-25	Intel
	260 nsF*	CMOS	TS	40	5	HS6564RH	† Harris (4696)
	300 nsF	NMOS	TS	28	5	2186-30	Intel
						2187A-30	Intel
	350 nsF	NMOS	TS	28	5	2186-35	Intel
						2187-35	Intel
						2187A-25	Intel
							(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY-RAMs (Cont'd)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	
8192x8 (Cont'd)								
	400 nsF	CMOS Module	TS	40	5	**HM5-6564-2**	† **Harris**	**(3968)**
						HM5-6564-9	**Harris**	**(3968)**
	450 nsF	CMOS Module	TS	40	5	**HM5-6564-5**	**Harris**	**(3968)**
16384x1	15 nsF	ECL		20	−4.5	MB81256-10	Fujitsu	
						MBM100480-15	Fujitsu	
					−5.2	MBM10480-15	Fujitsu	
	25 nsF	ECL	OE	20	−4.5	MBM100480	Fujitsu	
						HM100480	Hitachi	
					−5.2	MBM10480	Fujitsu	
						HM10480	Hitachi	
	35 nsF	ECL	OE	20	−4.5	F100480	Fairchild	
					−5.2	F10480	Fairchild	
		NMOS	TS	20	5	**AM2167-35**	**AMD**	**(3915)**
						IMS1400-35	**Inmos**	**(3977)**
						MCM2167H-35	**Motorola**	**(4046,4053)**
	45 nsF	CMOS	TS	20	5	HM6167-45	Hitachi	
						IDT6167L45	**IDT**	**(3988)**
						IDT6167S45	**IDT**	**(3988)**
		NMOS	TS	20	5	**AM2167-45**	**AMD**	**(3915)**
						AM2167-45M	† **AMD**	**(3915)**
						MB8167A-45	Fujitsu	
						IMS1400-45	**Inmos**	**(3977)**
						ITT2167-45	ITT	
						MCM2167H-45	**Motorola**	**(4046,4053)**
	55 nsF	CMOS	TS	20	5	HM6167-55	Hitachi	
						IDT6167L55	**IDT**	**(3988)**
				22	5	**IDT7M464-55**	**IDT**	**(3988)**
				24	5	**IDT6167S55**	† **IDT**	**(3988)**
						IDT6167S55	IDT	
		NMOS	TS	20	5	**AM2167-55**	**AMD**	**(3915)**
						AM2167-55M	† **AMD**	**(3915)**
						MB8167A-55	Fujitsu	
						IMS1400-55	**Inmos**	**(3977)**
						IMS1400-55M	† **Inmos**	**(501)**
						ITT2167-55	ITT	
						μPD2167	**NEC**	**(4086)**
						μPD2167-3	**NEC**	**(4086)**
						SY2167-3	**Synertek**	**(4210)**
	65 nsF	CMOS	TS	22	5	**IDT7M464-65**	**IDT**	**(4004)**
						IDT7M464-65C	† **IDT**	**(4004)**
	70 nsF	CMOS	TS	20	5	HM6167	Hitachi	
						IDT6167L70	**IDT**	**(3988)**
						IDT6167S70	**IDT**	**(3988)**
		NMOS	TS	20	5	**AM2167-70**	**AMD**	**(3915)**
						AM2167-70M	† **AMD**	**(3915)**
						MB8167A-70	Fujitsu	
						MB8167A-70W	Fujitsu	
						IMS1400-70L	**Inmos**	**(501)**
						IMS1400-70M	† **Inmos**	**(3977)**
						IMS1400L	**Inmos**	**(3977)**
						ITT2167-70	ITT	
						μPD2167-2	**NEC**	**(4086)**
						SY2167	**Synertek**	**(4210)**
						SYM2167	† **Synertek**	**(535)**
	85 nsF	CMOS	TS	20	5	HM6167-6	Hitachi	
						HM6167L-6	Hitachi	
						IDT6167L85	† **IDT**	**(3988)**
						IDT6167L85	IDT	
						IDT6167S85	† **IDT**	**(3988)**
						IDT6167S85	IDT	
16384x1	85 nsF	CMOS	TS					(Cont'd)
				22	5	**IDT7M464-85**	**IDT**	**(4004)**
						IDT7M464-85C	† **IDT**	**(4004)**
		NMOS	TS	20	5	MBM8167A-85W	† Fujitsu	
	100 nsF	CMOS	TS	20	5	HM6167-8	Hitachi	
						HM6167L-8	Hitachi	
						IDT6167S100	**IDT**	**(3988)**
				22	5	**IDT7M464-100C**	† **IDT**	**(4004)**
				24	5	**IDT6167L100**	† **IDT**	**(3988)**
						IDT6167L100	IDT	
		NMOS	TS	20	5	**IMS1400-10L**	**Inmos**	**(3977)**
	150 nsF	NMOS	TS	16	±5,12	**AM9016F**	**AMD**	**(3918)**
16384x4	350 nsF	CMOS	TS	40	5	**HM5-6564-2**	† Harris	(3968)
						HM5-6564-9	Harris	(3968)
	450 nsF	CMOS	TS	40	5	HM5-6564-5	Harris	
16384x16	150 nsF	CMOS	TS	48	5	**HM92560-8**	† **Harris**	(3968)
		CMOS Module	TS	48	5	**HM92560-2**	† **Harris**	(3968)
						HM92560-9	**Harris**	(3968)
	250 nsF	CMOS Module	TS	48	5	**HM92560-5**	**Harris**	(3968)
						HM92570-2	† **Harris**	(3968)
						HM92570-8	† **Harris**	(3968)
						HM92570-9	**Harris**	(3968)
	270 nsF	CMOS	TS	48	5	HM92560-2	† Harris	(3968)
						HM92560-8	† Harris	(3968)
						HM92560-9	Harris	(3968)
						HM92570-2	† Harris	(3988)
						HM92570-8	† Harris	(3968)
						HM92570-9	Harris	(3968)
	300 nsF	CMOS Module	TS	48	5	**HM92570-5**	† **Harris**	(3968)
32768x8	150 nsF	CMOS	TS	48	5	HM92560-8	† Harris	(3968)
						HM92560-9	Harris	(3968)
						HM92570-2	† Harris	(3968)
	250 nsF	CMOS	TS	48	5	HM92560-5	Harris	(3968)
						HM92570-8	† Harris	(3968)
						HM92570-9	Harris	(3968)
	270 nsF	CMOS	TS	48	5	HM92560-2	† Harris	(3968)
						HM92560-8	† Harris	(3968)
						HM92560-9	Harris	(3968)
						HM92570-2	† Harris	(3968)
						HM92570-8	† Harris	(3968)
						HM92570-9	Harris	(3968)
	300 nsF	CMOS	TS	48	5	HM92570-5	† Harris	
65536x1	70 nsF	CMOS	TS	22	5	**IDT7M164-70**	**IDT**	**(4008)**
	100 nsF	CMOS	TS	22	5	**IDT7M164-100**	**IDT**	**(4008)**
						IDT7M164-100C	† **IDT**	**(4008)**
		NMOS	TS	16	5	**AM9064-10**	**AMD**	**(3919)**
	120 nsF	CMOS	TS	22	5	**IDT7M164-120**	**IDT**	**(4008)**
						IDT7M164-120C	† **IDT**	**(4008)**
		NMOS	TS	16	5	**AM9064-12**	**AMD**	**(3919)**
	150 nsF	CMOS	TS	22	5	**IDT7M164-150**	**IDT**	**(4008)**
						IDT7M164-150C	† **IDT**	**(4008)**
		NMOS	TS	16	5	**AM9064-15**	† **AMD**	**(3919)**
						ITT4164-15	ITT	
	200 nsF	NMOS	TS	16	5	ITT4164-20	ITT	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY-ROMs

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source
32x8	45 nsR	TTL	OC	16	5	SN7488A	TI
256x4	1.8 μsR	CMOS	—	16	3-15	HD14524B	Hitachi
						MCM14524A	† **Motorola** (4048)
						MCM14524C	**Motorola** (4048)
	60 nsF	TTL	OC	16	5	SN74187	TI
256x8	70 nsF	TTL	OC	20	5	SN74S271	TI
			TS	20	5	SN74S371	TI
512x4	70 nsF	TTL	OC	16	5	SN74S270	TI
			TS	16	5	SN74S370	TI
512x8	70 nsF	NMOS	TS	24	5	82HM141C	Intersil
	90 nsF	NMOS	TS	24	5	82HM141M	† Intersil
	500 nsF	CMOS	TS	24	10	HCMP1831	Hughes
						HCMP1832	Hughes
						HMMP1831	† Hughes
						HMMP1832	† Hughes
						CDP1831	† **RCA** (1593)
						CDP1832	† **RCA** (1593)
	700 nsF	PMOS	TS	24	−12,5	3514	Fairchild
	1000 nsF	CMOS	TS	24	5	HCMP1831C	Hughes
						HCMP1832C	Hughes
						HMMP1831C	† Hughes
						HMMP1832C	† Hughes
						CDP1831C	† **RCA** (1593)
						CDP1832C	† **RCA** (1593)
1024x4	60 nsF	HMOS	TS	24	5	82HM137C	Intersil
	80 nsF	HMOS	TS	24	5	82HM137M	† Intersil
1024x8	35 nsF	NMOS	TS	24	5	**SY3308R**	**Synertek** (4211)
	45 nsF	TTL	TS	22	5	MB7130E	Fujitsu
						MB7130H	Fujitsu
	55 nsF	TTL	OC	24	5	6280-2	MMI
			TS	24	5	6281-2	MMI
	70 nsF	HMOS	TS	24	5	82HM181C	Intersil
		NMOS	TS	24	5	**SY3308**	**Synertek** (4211)
	75 nsF	TTL	OC	24	5	5280-2	† MMI
			TS	24	5	5281-2	† MMI
	80 nsF	TTL	OC	24	5	6280-1	MMI
						6282-1	MMI
			TS	24	5	6281-1	MMI
						6283-1	MMI
	90 nsF	HMOS	TS	24	5	82HM181M	† Intersil
		TTL	OC	24	5	DM75S29	† National
			TS	24	5	DM75S28	† National
	175 nsF	TTL	OC	24	5	5280-1	† MMI
						5282-1	† MMI
			TS	24	5	5281-1	† MMI
						5283-1	† MMI
	250 nsF	NMOS	TS	24	5	F68B308	Fairchild
						MCM68B308	Motorola
						MCM68B30A	Motorola
	350 ns *	CMOS	TS	24	10	HCMP1833	Hughes
						HCMP1834	Hughes
						HMMP1833	† Hughes
						HMMP1834	† Hughes
						CDP1833	† **RCA** (1593)
						CDP1834	† **RCA** (1593)
	350 nsF	NMOS	TS	24	5	MCM68A30A	Motorola
						μPD2308A-35	**NEC** (4096)
						SMJ2708-35	† **TI** (4234)
						TMS2708-35	TI
					±5,12	MCM68A308	Motorola
						MCM68A308P7	Motorola
	450 nsF	NMOS	TS	24	5	**μPD2308A-45**	**NEC** (4096)

(Continued)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source
1024x8	450 nsF	NMOS	TS	24	5		(Cont'd)
						SMJ2708-45	† **TI** (4234)
						SMJ27L08-45	† **TI** (4234)
						TMS2708-45	TI
						TMS27L08-45	TI
					±5,12	AM8308	AMD
						μPD2308A	**NEC** (4096)
	500 nsF	NMOS	TS	24	5	HN46830	Hitachi
	850 ns *	CMOS	TS	24	5	**CDP1833C**	† **RCA** (1593)
						CDP1834C	† **RCA** (1593)
		NMOS	TS	24	5	HCMP1833C	Hughes
						HCMP1834C	Hughes
						HMMP1833C	† Hughes
						HMMP1834C	† Hughes
1024x9	100 nsF	TTL	OC	24	5	6260-1	MMI
			TS	24	5	6261-1	MMI
	150 nsF	TTL	OC	24	5	5260-1	† MMI
			TS	24	5	5261-1	† MMI
1024x10	100 nsF	TTL	OC	24	5	6255-1	MMI
			TS	24	5	6256-1	MMI
	150 nsF	TTL	OC	24	5	5255-1	† MMI
			TS	24	5	5256-1	† MMI
1024x12	200 nsR	CMOS	TS	18	10	IM6312AI	Intersil
	220 nsR	CMOS	TS	18	5	IM6312AM	† Intersil
	510 nsF	CMOS	TS	18	5	IM6312-1I	Intersil
	560 nsF	CMOS	TS	18	5	IM6312-1M	† Intersil
	640 nsF	CMOS	TS	18	5	IM6312I	Intersil
						IM6312M	† Intersil
1152x9	125 nsF	TTL	OC	24	5	6290	MMI
						6291	MMI
2048x4	60 nsF	NMOS	TS	24	5	72HM185C	Intersil
						82HM185M	† Intersil
2048x8	—	NMOS	—	16	5	SPR-16	GI
	35 nsF	NMOS	—	24	5	**SY3316R**	**Synertek** (4211)
	45 nsF	TTL	TS	22	5	MB7136H	Fujitsu
	55 nsF	TTL	TS	22	5	MB7136E	Fujitsu
				24	5	MB7138E-W	† Fujitsu
	80 nsF	NMOS	TS	24	5	82HM191C	Intersil
						SYM3316	† MMI
						SYM3316A	MMI
						SY2316A	**Synertek** (4211)
						SY3316	**Synertek** (4211)
						SY3316A	**Synertek** (4211)
	100 nsF	NMOS	TS	24	5	82HM191M	† Intersil
						SYM3316	† **Synertek** (535)
						SYM3316A	† **Synertek** (535)
	110 nsF	NMOS	TS	24	5	S68116	AMI
		TTL	OC	24	5	6275-1	MMI
			TS	24	5	6276-1	MMI
	120 nsF	TTL	OC	24	5	5275-1	† MMI
			TS	24	5	5276-1	† MMI
	150 ns *	I²L	OC/TTL				
				24	5	SBP9818C	TI
						SBP9818M	† TI
	200 nsF	NMOS	TS	24	5	**SY2316B-2**	**Synertek** (4211)
	250 nsF	CMOS	TS	24	5	23SC16A	Supertex
		NMOS	TS	24	5	**F35316-25**	**Fairchild** (1464)
						2616A-25	Signetics
	300 nsF	CMOS	TS	24	5	MD23SC16	Mitel
						CDP1835C	† **RCA** (1593)
		HMOS	TS	24	5	IM7332C	Intersil
		NMOS	TS	24	5	**F35316-30**	**Fairchild** (1464)
						G2316B-3	GTEMicro
						2616-30	Signetics
						SY2316B-3	**Synertek** (4211)

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–ROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Page
2048x8								(Cont'd)
	350 ns *	CMOS	TS	24	5	IM6316I	Intersil	
						IM6316M	† Intersil	
		I²L	OC/TTL	24	5	SBP8316C	TI	
						SBP8316M	† TI	
	350 nsF	CMOS	TS	24	5	23MC16A	† Supertex	
						23SC16A-3	Supertex	
		NMOS	TS	24	5	AM8316EC	AMD	
						AM9218C	AMD	
						F3516-35	Fairchild	
						F68316	**Fairchild**	**(1464)**
						R03-9316C	GI	
						MK34000-3	Mostek	
						MCM68A316A	**Motorola**	**(4048)**
						MCM68A316E	**Motorola**	**(4048)**
						MCM68A316EP91	Motorola	
						µPD2316E-35	**NEC**	**(4098)**
						µPD2316E-5	**NEC**	**(4098)**
						2616-35	Signetics	
						SMJ2516-35	**† TI**	**(4232)**
						TMS2516-35	**TI**	**(543,4232)**
	430 nsF	CMOS	—	18	5	**MCM65516-43**	**Motorola**	**(4048)**
	450 nsF	NMOS	TS	24	5	AM8316EB	AMD	
						AM9217BC	AMD	
						AM9217BM	† AMD	
						AM9218BC	AMD	
						AM9218BM	† AMD	
						S68A316	AMI	
						S68B316	AMI	
						F3516-45	Fairchild	
						R03-9316B	GI	
						G2316B-4	GTEMicro	
						MK34000-84	† Mostek	
						MM52116	National	
						µPD2316E	**NEC**	**(4098)**
						µPD2316E-45	**NEC**	**(4098)**
						R2316B	Rockwell	
						R2316E	Rockwell	
						M2316	SGS	
						2616-45	Signetics	
						SY2316B	**Synertek**	**(4211)**
						SMJ2516-45	**† TI**	**(4232)**
						TMS2516-45	**TI**	**(543,4232)**
						TMM331A	Toshiba	
						TMM334	Toshiba	
						TSU2316E	Toshiba	
	550 nsF	CMOS	—	18	5	**MCM65516-55**	**Motorola**	**(4048)**
			TS	18	4.5-5.5	**CDP65516**	**RCA**	**(1593)**
				24	5	CM1600	Supertex	
		NMOS	TS	24	5	AM9217AC	AMD	
						AM9217AM	† AMD	
	800 nsF	CMOS	TS	24	5	CM1600-2	Supertex	
						MM1600	† Supertex	
2048x10	500 nsF	NMOS	TS	40	5	R03-9502	GI	
4096x4	45 nsF	TTL	TS	20	5	MB7134H	Fujitsu	
	55 nsF	TTL	TS	20	5	MB7134E	Fujitsu	
4096x8	65 nsF	TTL	TS	24	5	MB7142E-W	† Fujitsu	
	115 nsF	NMOS	TS	24	5	S68132	AMI	
	150 nsF	CMOS	TS	24	5	SCM23C32-3	SSS	
						SCM23C33-3	SSS	
	200 nsF	CMOS	TS	24	5	SCM23C32-4	SSS	
						SCM23C33-4	SSS	
		NMOS	TS	24	5	R09432D	GI	
						R09433D	GI	
						2332-20	Signetics	
						2632A-20	Signetics	
								(Continued)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Page
4096x8	200 nsF	NMOS	TS	24	5			(Cont'd)
						SY2332-2	**Synertek**	**(4211)**
						SY2333-2	**Synertek**	**(4211)**
						SYM2332-3	**† Synertek**	**(535)**
						SYM2333-3	**† Synertek**	**(535)**
	250 nsF	CMOS	TS	24	5	23SC32A	Supertex	
						23SC33A	Supertex	
		NMOS	TS	24	5	2332-25	Signetics	
						2632A-25	Signetics	
						UM2333-25	Universal	
	300 nsF	CMOS	TS	24	5	883/23C32M	† SSS	
						883/23C33M	† SSS	
						SCM23C32	SSS	
						SCM23C32M	† SSS	
						SCM23C33	SSS	
						SCM23C33M	† SSS	
		NMOS	TS	24	5	AM9232C	AMD	
						AM9233C	AMD	
						F3532-30	**Fairchild**	**(1465)**
						F3533-30	**Fairchild**	**(1465)**
						IM7332	Intersil	
						µPD2332A-30	**NEC**	**(4100)**
						µPD2332B-30	**NEC**	**(4100)**
						R2332-3	Rockwell	
						2332-30	Signetics	
						2632A-30	Signetics	
						2632AE-30	† Signetics	
						SY2332-3	**Synertek**	**(4211)**
						SY2333-3	**Synertek**	**(4211)**
						SMJ2532-30	**† TI**	**(4231)**
						TMS2532-30	**TI**	**(543,4231)**
						TMS2732A-30	**TI**	**(4230)**
						TMS4732-30	**TI**	**(4226)**
						VT2332A	**VTI**	**(4249)**
						VT2333A	**VTI**	**(4249)**
	350 nsF	CMOS	TS	24	4-6.5	**CDM5332**	**RCA**	**(1593)**
						CDM5333	**RCA**	**(1593)**
					5	23MC32A	† Supertex	
						23MC33A	† Supertex	
						23SC32A-3	Supertex	
						23SC33A-3	Supertex	
		NMOS	TS	24	5	**S2333**	**AMI**	**(3932)**
						S68A332	AMI	
						F3532-35	**Fairchild**	**(1465)**
						F3533-35	**Fairchild**	**(1465)**
						F68A332	Fairchild	
						G2332-3	GTEMicro	
						MCM68A332	**Motorola**	**(4048)**
						MCM68A332P2	Motorola	
						µPD2332A-1	**NEC**	**(4100)**
						µPD2332A-35	**NEC**	**(4100)**
						µPD2332B-1	**NEC**	**(4100)**
						IPD2332B-35	**NEC**	**(4100)**
						2632A-35	Signetics	
						2632AM-35	† Signetics	
						SMJ2532-35	**† TI**	**(4231)**
						TMS2532-35	**TI**	**(543,4231)**
						TMS2732A-35	**TI**	**(4230)**
						TMS4732-35	**TI**	**(4226)**
						TMM2332	Toshiba	
	450 nsF	CMOS	TS	24	5	TC5332	Toshiba	
						TC5333	Toshiba	
						TC5334	Toshiba	
						TC5335	Toshiba	
		NMOS	TS	24	5	AM9232BC	AMD	
								(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY–ROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source
4096x8	450 nsF	NMOS	TS	24	5		(Cont'd)
						AM9232BM	† AMD
						AM9233BC	AMD
						AM9233BM	† AMD
						S68332	AMI
						F3532-45	Fairchild (1465)
						F3533-45	Fairchild (1465)
						R09433C	GI
						R09432B	GI
						R09433B	GI
						G2332-4	GTEMicro
						MM52132	National
						μPD2332	NEC (4100)
						μPD2332A	NEC (4100)
						μPD2332A-45	NEC (4100)
						μPD2332B	NEC (4100)
						μPD2332B-45	NEC (4100)
						R2332	Rockwell
						2332-45	Signetics
						2632A-45	Signetics
						2632AM-45	† Signetics
						ROM4732	SMC
						SY2332	Synertek (4211)
						SY2333	Synertek (4211)
						SYM2332	† Synertek (535)
						SYM2333	† Synertek (535)
						SMJ2532-45	† TI (4231)
						TMS2532-45	TI (543,4231)
						TMS2732A-45	TI (4230)
						TMS4732	TI (4226)
						TMS4732-45	TI (4226)
						TMM333	Toshiba
						TSU333-2	Toshiba
						VT2332	VTI (4249)
						VT2333	VTI (4249)
	500 nsF	NMOS	TS	24	5	F68332	Fairchild (1465)
	500 μsF	CMOS	TS	24	4-6.5	CDP1837C	RCA (1593)
	800 nsF	CMOS	TS	24	5	CM3200-2	Supertex
						MM3200	† Supertex
	1500 nsF	CMOS	TS	24	5	CM3200-3	Supertex
4096x10	300 nsF	NMOS	TS	28	5	S9508A	AMI
						R09508	GI
	350 nsF	NMOS	TS	28	5	AM9240-35	AMD
8000x8	350 nsF	NMOS	TS	28	5	TMS2564-35	TI (4229)
	450 nsF	NMOS	TS	28	5	SMJ2564-45	† TI (4229)
						TMS2564-45	TI (4229)
8192x4x2	450 nsF	NMOS	TS	24	5	2364B	SGS
						26S64	SGS
						M2362	SGS
8192x8	120 nsF	NMOS	TS	24	5	S68164	AMI
	150 nsF	CMOS	TS	24	5	SCM23C64-3	SSS
	200 nsF	CMOS	TS	24	5	SCM23C64-4	SSS
		NMOS	TS	24	5	AM9265-20	AMD (3923)
						R09464AD	GI
						R09464D	GI
						MCM68364	Motorola (4048,4054)
						R2364A2	Rockwell
						2664-20	Signetics (4198)
						2664A-20	Signetics
						TMM2366	Toshiba
				28	5	AM9264-20	AMD (3922)
						XLS2366	EXEL
						R09864AD	GI
						R09864D	GI
							(Continued)
8192x8	200 nsF	NMOS	TS	28	5		(Cont'd)
						μPD2364E	NEC (4102,4104)
						IPD2364E-20	NEC (4102)
						R2364B2	Rockwell
						2364-20	Signetics (4196)
						SY6365	Synertek (4211)
						TMS2764H-20	TI (4228)
						TMM2365	Toshiba
						VT2365B	VTI (4251)
						VT2366B	VTI (4251)
	250 nsF	CMOS	TS	24	4-6	CDM5364	RCA (1593)
					5	MP2364-25	MicroPwr
						MP2365-25	MicroPwr
						TC5364	Toshiba
						TC5365	Toshiba
						TC5366	Toshiba
						VT23C64	VTI
				28	4-6	CDM5365	RCA
		NMOS	TS	24	5	AM9264D	AMD (3922)
						S68B364	AMI (3933)
						F3564-25	Fairchild (1465)
						MK36000-4	Mostek
						MKB36000-83	† Mostek
						MKB37000-84	† Mostek
						MCM68364-25	Motorola (4048,4054)
						MCM68365-25	Motorola (4048,4054)
						MCM68366-25	Motorola (4048,4054)
						MCM68B364	Motorola
						R2364A25	Rockwell
						M36000	SGS
						2664-25	Signetics
						2664A-25	Signetics
						ROM36000	SMC
						SY2364A	Synertek (4211)
						VT2364B	VTI (4250)
				28	5	AM9265D	AMD (3923)
						S2364B	AMI (3934)
						F3565-25	Fairchild (1465)
						MK37000-4	Mostek
						MK37000-5	Mostek
						MCM68369-25	Motorola (4055)
						MCM68370-25	Motorola (4055)
						IPD2364E-25	NEC (4102)
						R2364B25	Rockwell
						2364-25	Signetics
						TMS2764H-25	TI (4228)
						TMM2364	Toshiba
		TTL	TS	24	5	F3566-25	Fairchild (1466)
				28	5	F3568-25	Fairchild (1466)
						F3569-25	Fairchild (1466)
						F3570-25	Fairchild (1467)
	300 ns *	NMOS	TS	28	5	2364-30	Signetics
	300 nsF	CMOS	TS	24	5	HCMP23C64C	Hughes
						883/23C64M	† SSS
						SCM23C64M	† SSS
						SCM23C65	SSS
						23SC65	Supertex
						23SC65A	Supertex
				28	5	G5364-3	GTEMicro
						G5365-3	GTEMicro
						SCM23C64	SSS
						23SC64	Supertex
						23SC64A	Supertex
		NMOS	TS	24	5	AM9264C	AMD (3922)
							(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

Master Selection Guide

MEMORY

MEMORY-ROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
8192x8	300 nsF	NMOS	TS	24	5		(Cont'd)	
						S4264	AMI	
						XLS2364	EXEL	
						R09464AC	GI	
						R09464C	GI	
						2364-3	GTEMicro	5
						MK36000-5	Mostek	
						MKB36000-84	† Mostek	
						MKB37000-85	† Mostek	
						MCM68364-30	**Motorola** **(4048,4054)**	
						µPD2364-30	**NEC** **(4102)**	10
						R2364A3	Rockwell	
						2664A-30	Signetics	
						2664AE-30	† Signetics	
						SY2364-3	**Synertek** **(4211)**	
						SY2364A-3	**Synertek** **(4211)**	15
						SYM2364-3	**† Synertek** **(535)**	
						SYM2364A-3	**† Synertek** **(535)**	
						TMS4764-30	**TI** **(4225)**	
						VT2364A	**VTI** **(4250)**	
				28	5	**AM9265C**	**AMD** **(3923)**	20
						XLS2365	EXEL	
						R09864AC	GI	
						R09864C	GI	
						R2364B3	Rockwell	
						SY2365-3	**Synertek** **(4211)**	25
						SY2365A-3	**Synertek** **(4211)**	
						SYM2365-3	**† Synertek** **(535)**	
						SYM2365A-3	**† Synertek** **(535)**	
						TMS2764H-30	**TI** **(4228)**	
						VT2365A	**VTI** **(4251)**	30
						VT2366A	**VTI** **(4251)**	
	350 nsF	CMOS	TS	24	5	HN61365	Hitachi	
						HN61366	Hitachi	
						MP2364-35	MicroPwr	
						MP2365-35	MicroPwr	35
						SMM2364	SMOS	
				28	5	HN61364	Hitachi	
						SMM2365	SMOS	
		NMOS	TS	24	5	**S68A364**	**AMI** **(3933)**	
						F3564-35	**Fairchild** **(1465)**	40
						F3565-35	**Fairchild** **(1465)**	
						2364-4	GTEMicro	
						IM7364C	Intersil	
						MCM68365-35	**Motorola** **(4048,4054)**	
						MCM68366-35	**Motorola** **(4048,4054)**	45
						MCM68A364	Motorola	
						MCM68A364P3	Motorola	
						µPD2364-35	**NEC** **(4102)**	
						TMS4764-35	**TI** **(4225)**	
				28	5	**S2364A**	**AMI** **(3934)**	50
						MCM68369-35	**Motorola** **(4055)**	
						MCM68370-35	**Motorola** **(4055)**	
						2364-35	Signetics	
						2664AM-35	† Signetics	
		TTL	TS	24	5	**F3566-35**	**Fairchild** **(1466)**	55
				28	5	**F3568-35**	**Fairchild** **(1466)**	
						F3569-35	**Fairchild** **(1466)**	
						F3570-35	**Fairchild** **(1467)**	
	400 nsF	CMOS	TS	24	5	23MC65	Supertex	
						23MC65A	Supertex	60
						23SC65-3	Supertex	
						23SC65A-3	Supertex	
				28	5	23MC64	† Supertex	
						23MC64A	† Supertex	
						23SC64-3	Supertex	65
						23SC64A-3	Supertex	
							(Continued)	
8192x8							(Cont'd)	
	450 nsF	CMOS	TS	24	5	MP2364-45	MicroPwr	
						MP2364C	MicroPwr	
						MP2365-45	MicroPwr	
				28	5	G5364-4	GTEMicro	70
						G5365-4	GTEMicro	
		NMOS	TS	24	5	**AM9264B**	**AMD** **(3922)**	
						XLS2364-450	EXEL	
						R09464AB	GI	
						R09464B	GI	75
						MCM68367-45	**Motorola** **(4054)**	
						MCM68368-45	**Motorola** **(4054)**	
						MM52164	National	
						2664A-45	Signetics	
						2664AM-45	† Signetics	80
						SY2364	**Synertek** **(4211)**	
						SYM2364	**† Synertek** **(535)**	
						SYM2364A	**† Synertek** **(535)**	
						TMS4764	**TI** **(4225)**	
						TMS4764-45	**TI** **(4225)**	85
						VT2364	**VTI** **(4250)**	
				28	5	**AM9265B**	**AMD** **(3923)**	
						XLS2365-450	EXEL	
						XLS2366-450	EXEL	
						R09864AB	GI	90
						R09864B	GI	
						µPD2364-45	**NEC** **(4102)**	
						2364-45	Signetics	
						SY2365	**Synertek** **(4211)**	
						SY2365A	**Synertek** **(4211)**	95
						SYM2365	**† Synertek** **(535)**	
						SYM2365A	**† Synertek** **(535)**	
						TMS2764H-45	**TI** **(4228)**	
						VT2365	**VTI** **(4251)**	
						VT2366	**VTI** **(4251)**	100
	1000 nsF	CMOS	TS	24	1.5	MP2364LP1	MicroPwr	
						MP2365LP1	MicroPwr	
	1500 nsF	CMOS	TS	28	5	CM6400	Supertex	
	2000 nsF	CMOS	TS	28	5	CM6400-3	Supertex	
						CM6400A-3	Supertex	105
						MM6400	† Supertex	
						MM6400A	† Supertex	
8192x10	—	NMOS	TS	24	5	MCM68380	Motorola	
	350 nsF	NMOS	TS	28	5	AM9280-35	AMD	
12288x10	300 nsF	NMOS	TS	28	5	VT23121	VTI	110
16384x8	—	NMOS	TS	28	5	SPR-128	GI	
	6 µs	NMOS	TS	24	5	S3630B	AMI	
	150 nsF	NMOS	TS	28	5	**MCM63128-15**	**Motorola** **(4048,4055,4056)**	
						MCM63128-20	**Motorola** **(4048,4055,4056)**	
	200 nsF	NMOS	TS	28	5	R09128D	GI	115
						AM92128-20	**AMD** **(3924)**	
						23128-20	**Signetics** **(4200)**	
						SY23128-2	**Synertek** **(4211)**	
						SY23128A-2	**Synertek** **(4211)**	
						SY23130-2	**Synertek** **(4211)**	120
						SY23130A-2	**Synertek** **(4211)**	
						TMS27128-20	**TI** **(4227)**	
						TMM23128	Toshiba	
						TMM27128-20	Toshiba	
						VT23128A	**VTI** **(4252)**	125
						VT23129A	**VTI** **(4252)**	
	250 nsF	CMOS	TS	28	5	HN613128	Hitachi	
							(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY–ROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	
16384x8	250 nsF	CMOS	TS	28	5			(Cont'd)
						MP23128-25	MicroPwr	
						CDM53128	**RCA**	(1593)
						SCM23C128	SSS	
		NMOS	TS	28	5	**AM92128-25**	**AMD**	(3924)
						AM92128D	**AMD**	(3924)
						S23128B	**AMI**	(3935)
						μPD23128	**NEC**	(4106)
						23128-25	**Signetics**	(4202)
						TMS27128-25	**TI**	(4227)
						TMS47128-25	**TI**	(4224)
						TMM27128-25	Toshiba	
						VT23128	**VTI**	(4252)
						VT23129	**VTI**	(4252)
	300 nsF	NMOS	—	28	5	R09160	GI	
			TS	28	5	**AM92128-30**	**AMD**	(3924)
						AM92128C	**AMD**	(3924)
						R09128C	GI	
						23128-30	**Signetics**	(4202)
						SY23128-3	**†Synertek**	(4211)
						SY23128A-3	**†Synertek**	(4211)
						SY23130-3	**†Synertek**	(4211)
						SY23130A-3	**†Synertek**	(4211)
						SYM23128-3	**†Synertek**	(535)
						SYM23128A-3	**†Synertek**	(535)
						TMS27128-30	**TI**	(4227)
	350 nsF	NMOS	TS	28	5	**S23128A**	**AMI**	(3935)
						S3630A	AMI	
						TMS47128-35	**TI**	(4224)
	450 nsF	NMOS	TS	28	5	**AM92128-45**	**†AMD**	(3924)
						AM92128B	**AMD**	(3924)
						R09128B	GI	
						32128-45	Signetics	
						SY23128A	**†Synertek**	(4211)
						SY23130	**†Synertek**	(4211)
						SY23130A	**†Synertek**	(4211)
						SYM23128	**†Synertek**	(535)
						SYM23128A	**†Synertek**	(535)
						TMS27128-45	**TI**	(4227)
						TMS47128-45	**TI**	(4224)
						VT23128B	**VTI**	(4252)
						VT23129B	**VTI**	(4252)
	2000 nsF	CMOS	TS	28	5	CM1310	Supertex	
	5000 nsF	CMOS	TS	52	5	**μPD73128**	**NEC**	(4114)
	6500 nsF	CMOS	TS	28	5	HN43128	Hitachi	
32768x4	6500 nsF	CMOS	TS	28	5	HN43128	Hitachi	
32768x8	150 nsF	CMOS	TS	28	5	TMM23256	Toshiba	
		NMOS	TS	28	5	**S23256C**	**AMI**	(3936)
						MCM63256-15	**Motorola**	(4048,4055,4056)
	200 nsF	NMOS	TS	28	5	**AM92256-20**	**AMD**	(3925)
						XLS23256-200	EXEL	
						XLS23257-200	EXEL	
						XLS23258-200	EXEL	
						MK38000-20	Mostek	
						MCM63256-20	**Motorola**	(4048,4055,4056)
						23256A-20	Signetics	
						SY23256-2	**Synertek**	(4211)
						SY23256A-2	**Synertek**	(4211)
	250 nsF	CMOS	TS	28	4-6	**CDM53256**	**RCA**	(1593)
					5	XLS23C256	EXEL	
						MB83256	Fujitsu	
						HN613256	Hitachi	
						MP2325-25	MicroPwr	
								(Continued)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	
32768x8	250 nsF	CMOS	TS	28	5			(Cont'd)
						MP2326-25	MicroPwr	
						SCM23C256	SSS	
		NMOS	TS	28	5	**S23256B**	**AMI**	(3936)
						MK38000-25	Mostek	
						MKB38000-84†	Mostek	
						MCM65256	Motorola	
						MCM65256-25	Motorola	
						μPD23256	**NEC**	(4108)
						23256A-25	Signetics	
						TMS47256-25	**TI**	(4223)
						VT23256	**VTI**	(4253)
						VT23257	**VTI**	(4253)
	300 nsF	NMOS	TS	28	5	**AM92256-30**	**AMD**	(3925)
						XLS23256-300	EXEL	
						XLS23257-300	EXEL	
						XLS23258-300	EXEL	
						MKB38000-85†	Mostek	
						23256A-30	Signetics	
						SY23256-3	**Synertek**	(4211)
						SY23256A-3	**Synertek**	(4211)
						SYM23256-3	**†Synertek**	(535)
						SYM23256A-3	**†Synertek**	(535)
	350 nsF	NMOS	TS	28	5	23256A-35	Signetics	
						TMS47256-35	**TI**	(4223)
	450 nsF	CMOS	TS	28	5	MP2325-45	MicroPwr	
						MP2326-45	MicroPwr	
						2325	S MOS	
						SMM2326	S MOS	
		NMOS	TS	28	5	**AM92256-45**	**†AMD**	(3925)
						XLS23256-450	EXEL	
						XLS23257-450	EXEL	
						XLS23258-450	EXEL	
						23256A-45	Signetics	
						SY23256A	**Synertek**	(4211)
						SYM23256A	**†Synertek**	(535)
						TMS47256-45	**TI**	(4223)
	850 nsF	CMOS	TS	28	5	MP2325-85	MicroPwr	
						MP2326-85	MicroPwr	
	3500 nsF	CMOS	TS	28	5	HN61256	Hitachi	
65536x4	3500 nsF	CMOS	TS	28	5	HN61256	Hitachi	
131072x8	—	CMOS	TS	40	5	μPD738000	NEC	
	300 nsF	NMOS	TS	28	5	**μPD231000-30**	**NEC**	(4110)
	350 nsF	CMOS	TS	28	5	HN62301	Hitachi	
		NMOS	TS	28	5	**μPD231000-35**	**NEC**	(4110)
	5000 nsF	CMOS	TS	28	5	**μPD23C128**	**NEC**	(4112)
				52	5	**μPD731000**	**NEC**	(4116)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

Master Selection Guide

MEMORY

MEMORY–Shift Registers

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage, V	Device	Source	
Dynamic								
100	2	SS	PMOS	2.0 M	±5	AM1406	† AMD	
						AM1407	† AMD	
						AM1506	AMD	
						AM1507	AMD	
256	4	SS	PMOS	5.0 M	±5	AM1402AC	AMD	
						AM1402AM	† AMD	
				10.0 M	±5	AM2802C	AMD	
						AM2802M	† AMD	
455	2	SS	CCD	20.0 M	17	CCD321	Fairchild	
512	1	SS	PMOS	2.0 M	±5	AM1405A	AMD	
				3.0 M	±5	AM2805M	† AMD	
						AM2807M	† AMD	
				4.0 M	±5	AM2805C	AMD	
						AM2807C	AMD	
	2	SS	PMOS	5.0 M	±5	AM1403AC	AMD	
						AM1403AM	† AMD	
				10.0 M	±5	AM2803C	AMD	
						AM2803M	† AMD	
1024	1	SS	PMOS	3.0 M	±5	AM2806M	† AMD	
						AM2808M	† AMD	
				4.0 M	±5	AM2806C	AMD	
						AM2808C	AMD	
				5.0 M	±5	AM1404AC	AMD	
						AM1404AM	† AMD	
				10.0 M	±5	AM2804C	AMD	
						AM2804M	† AMD	
	2	SS	NMOS	1.0 M	5	AM2401	AMD	
				2.0 M	5	AM9401C	AMD	
						AM9401M	† AMD	
			PMOS	2.0 M	− 12,5	MM4025	† AMD	
						MM4026	† AMD	
				5.0 M	− 10.5,5	AM2825M	† AMD	
						AM2826M	† AMD	
				6.0 M	− 10.5,5	AM2825C	AMD	
						AM2826C	AMD	
2048	1	SS	PMOS	2.0 M	− 12,5	MM4027	† AMD	
				4.0 M	− 10.5,5	AM2827M	† AMD	
				6.0 M	− 10.5,5	AM2827C	AMD	
4096	4	PP	CCD	5.0 M	±5,12	CCD460	Fairchild	
65536	1	SS	CCD	25 M	±5,12	F464	Fairchild	
Static								
1-134	4	SS	NMOS	1 M	5	SR5015	SMC	
4	1	PP	Bipolar					
				3 M	5	SN74L95	TI	
						SN74L99	TI	
					12	375A/C	TeledyneS	
					15	375B/M	TeledyneS	
				6 M	5	DM54L95	† National	
						DM74L95	National	
				15 M	5	93L00C	Fairchild	
						93L00M	† Fairchild	
						MC8300	Motorola	
						MC9300	† Motorola	
						N8271	**Signetics**	**(876)**
						S8270	† Signetics	
						S8271	† Signetics	
				20 M	5	MC7270	Motorola	
						MC7271	Motorola	
						MC8270	Motorola	
						MC8271	Motorola	
						RC8270	Raytheon	
						RC8271	Raytheon	

(Continued)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage, V	Device	Source	
4	1	PP	Bipolar					
				20 M	5	(Cont'd)		
						RM8270	† Raytheon	
						RM8271	† Raytheon	
				25 M	5	54178	† Fairchild	
						54179	† Fairchild	
						54194	† Fairchild	
						5495	† Fairchild	
						74178	Fairchild	
						74179	Fairchild	
						74194	Fairchild	
						7495	Fairchild	
						ZN5495A	† Ferranti	
						ZN7495A	Ferranti	
						HD74194	Hitachi	
						HD7495A	Hitachi	
						HD74LS194A	Hitachi	
						MC74194	Motorola	
						DM54194	† National	
						DM5495	† National	
						DM74194	National	
						DM7495	National	
						54194	**† Signetics**	**(861)**
						5495A	**† Signetics**	**(860)**
						74194	**Signetics**	**(861)**
						7495A	**Signetics**	**(860)**
						74LS95B	Signetics	
						SN54178	**† TI**	**(984)**
						SN54179	**† TI**	**(985)**
						SN54194	**TI**	**(990)**
						SN5495A	**† TI**	**(954)**
						SN54L95	**TI**	**(954)**
						SN54L99	**† TI**	**(955)**
						SN54LS194A	**† TI**	**(990)**
						SN54LS95B	**† TI**	**(954)**
						SN74178	**TI**	**(984)**
						SN74179	**TI**	**(985)**
						SN74194	**TI**	**(990)**
						SN7495A	**TI**	**(954)**
						SN74LS194A	**TI**	**(990)**
						SN74LS95B	**TI**	**(954)**
				30 M	5	54195	† Fairchild	
						54LS194A	Fairchild	
						54LS195A	† Fairchild	
						54LS295A	† Fairchild	
						54LS395	† Fairchild	
						54LS95B	† Fairchild	
						74195	Fairchild	
						74LS194A	Fairchild	
						74LS195A	Fairchild	
						74LS295A	Fairchild	
						74LS395	Fairchild	
						74LS95B	Fairchild	
						9300C	Fairchild	
						9300M	† Fairchild	
						HD74195	Hitachi	
						HD74LS195A	Hitachi	
						MC74195	Motorola	
						SN54LS194A	† Motorola	
						SN54LS195A	† Motorola	
						SN54LS295A	† Motorola	
						SN54LS395	† Motorola	
						SN54LS95B	† Motorola	
						SN74LS194A	Motorola	
						SN74LS195A	Motorola	
						SN74LS295A	Motorola	
						SN74LS395	Motorola	
						SN74LS95B	Motorola	
						DM54195	† National	
						DM74195	National	

(Continued)

† Military Temperature Range (− 55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY–Shift Registers (Cont'd)

Static (Cont'd)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage, V	Device	Source
4	1	PP	Bipolar	30 M	5		(Cont'd)
						DM8300	National
						DM9300	† National
						T54LS395	† SGS
						T74LS395	SGS
						54LS195A	† Signetics (530)
						74195	Signetics (861)
						74LS195A	Signetics
						SN54195	† TI (991)
						SN54LS195A	† TI (991)
						SN54LS295B	† TI (1014)
						SN54LS395A	† TI (1031)
						SN74195	TI (991)
						SN74LS195A	TI (991)
						SN74LS295B	TI (1014)
						SN74LS395A	TI (1031)
				31 M	5	MC7495A	Motorola
				35 M	5	MC4012	Motorola
						MC4312	† Motorola
				70 M	5	54S194	† Fairchild
						74S194	Fairchild
						93S00C	Fairchild
						93S00M	† Fairchild
						74S194	Signetics
						74S195	Signetics
						SN54S194	† TI (990)
						SN54S195	† TI (991)
						SN74S194	TI (990)
						SN74S195	TI (991)
				140 M	−5.2	95H00C	Fairchild
				150 M	−5.2	F10000C	Fairchild
						MC10141	Motorola
						MC10541	† Motorola
						10141	Signetics (858)
				250 M	−5.2	F10141	Fairchild
			CMOS	2 M	3-15	F40194BM	† Fairchild
						F40195BM	† Fairchild
						F4035BM	† Fairchild
						HD14035B	Hitachi
						MC14035BC	Motorola
						CD4035BC	National
						MM54C195	† National
						CD4035BE	RCA (838)
						883/4035B	† SSS
						SCL4035B	SSS
						CM4035AE	Solitron
				3 M	3-15	F40194BC	Fairchild
						F40195BC	Fairchild
						F4035BC	Fairchild
						MC14035BA	† Motorola
						CD4035BM	† National
						MM74C195	National
						CD4035B	† RCA (838)
						CM4035A	† Solitron
				4.5 M	3-15	MC14194BA	† Motorola
				6.5 M	3-15	MM54C95	† National
						MM74C95	National
		PS	Bipolar	10 M	5	5494	† Fairchild
						7494	Fairchild
						ZN5494	† Ferranti
						ZN7494	Ferranti
						MC7494	Motorola
						5494	Signetics (860)
						7494	Signetics (860)

(Continued)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage, V	Device	Source
4	1	PS	Bipolar	10 M	5		(Cont'd)
						SN5494	† TI (953)
						SN7494	TI (953)
		SP		325 M	−5.2	MC1694	† Motorola
		SS		0.5 M	15	MC686	Motorola
	2	SP	CMOS	1 M	5	CM4015AE	Solitron
				1.5 M	5	CM4015A	† Solitron
				2.5 M	3-15	F4015BC	Fairchild
						HD14015B	Hitachi
						MC14015BC	Motorola
						CD4015A	National
						CD4015BE	RCA (838)
				3 M	3-15	F4015BM	† Fairchild
						CD4015B	† RCA (838)
						883/4015B	† SSS
						SCL4015B	SSS
					3-18	MC14015BA	† Motorola
5	1	PP	Bipolar	10 M	5	5496	† Fairchild
						7496	Fairchild
						ZN5496	† Ferranti
						ZN7496	Ferranti
						HD7496	Hitachi
						MC7496	Motorola
						DM5496	† National
						DM7496	National
						5496	† Signetics (528,860)
						54LS96	Signetics (529)
						7496	Signetics (860)
						74LS96	Signetics
						SN5496	† TI (954)
						SN7496	TI (954)
				25	5	SN54LS96	† TI (954)
						SN74LS96	TI (954)
	4	SS	CMOS	1.5 M	5	CM4006AD	† Solitron
				2 M	3-15	F4006BC	Fairchild
						CD4006BE	RCA (838)
						CM4006A	† Solitron
						CM4006AE	Solitron
				2.5 M	3-15	F4006M	† Fairchild
						CD4006A	National
				3 M	3-15	883/4006B	† SSS
						SCL4006B	SSS
				4 M	5-15	MC14006BC	Motorola
				7 M	5-15	MC14006BA	† Motorola
8	1	PP	Bipolar	15 M	5	DM7546	† National
						DM8546	National
				25 M	5	54198	† Fairchild
						54199	† Fairchild
						74198	Fairchild
						74199	Fairchild
						HD74198	Hitachi
						HD74199	Hitachi
						DM54198	† National
						DM54199	† National
						DM74198	National
						DM74199	National
						74199	Signetics (861)
						SN54198	† TI (992)
						SN54199	† TI (993)
						SN74198	TI (992)
						SN74199	† TI (993)
				35 M	5	AM25LS23C	AMD (1427)

(Continued)

† Military Temperature Range (−55° to 125°C)
* Typical Values

SS = Serial In, Serial Out

PP = Parallel In, Parallel Out

MEMORY–Shift Registers (Cont'd)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage, V	Device	Source	
Static								**(Cont'd)**
8	1	PP	Bipolar					
				35 M	5			(Cont'd)
						AM25LS23M	**† AMD**	**(1427)**
						SN54LS323	† AMD	
						SN74LS323	AMD	
						54LS299	† Fairchild	
						54LS323	† Fairchild	
						74LS299	Fairchild	
						74LS323	Fairchild	
						SN54LS299	**† TI**	**(1016)**
						SN54LS323	**† TI**	**(1018)**
						SN64LS299	TI	
						SN74LS323	**TI**	**(1018)**
				50 M	5	**SN54S299**	**† TI**	**(1016)**
						SN74S299	**TI**	**(1016)**
			CMOS	2.5 M	3-15	SCL4034B	SSS	
					3-18	MC14034BC	Motorola	
					5	CM4034AE	Solitron	
				3 M	3-15	CD4034BC	National	
						CD4034BM	National	
						CD4034B	**† RCA**	**(838,840)**
						883/4034B	† SSS	
						TC4034B	Toshiba	
					3-18	HD14034B	Hitachi	
						MC14034BA	Motorola	
					5	CM4034A	† Solitron	
		PS	Bipolar					
				14 M	5	DM7590	† National	
						DM8590	National	
				20 M	5	54165	† Fairchild	
						74165	Fairchild	
						MC74165	Motorola	
						DM54165	† National	
						DM74165	National	
						54165	**† Signetics**	**(861)**
						74165	**Signetics**	**(861)**
						SN54165	**† TI**	**(979)**
						SN74165	**TI**	**(979)**
				25 M	5	54166	† Fairchild	
						54LS165	† Fairchild	
						74166	Fairchild	
						74LS165	Fairchild	
						HD74166	Hitachi	
						SN54LS165	† Motorola	
						SN74LS165	Motorola	
						DM54166	† National	
						DM74166	National	
						54166	**† Signetics**	**(861)**
						74166	**Signetics**	**(861)**
						SN54166	**† TI**	**(979)**
						SN54LS165	**† TI**	**(979)**
						SN54LS166	**† TI**	**(979)**
						SN74166	**TI**	**(979)**
						SN74LS165	**TI**	**(979)**
						SN74LS166	**TI**	**(979)**
			CMOS	1 M	3-15	F4014BC	Fairchild	
						F4021BC	Fairchild	
				2.5 M	3-15	HD14021B	Hitachi	
						MC14021BC	Motorola	
						CD4014A	National	
						CD4021A	National	
						CD4014BE	**RCA**	**(838)**
						CD4021BE	**RCA**	**(838)**
						SCL4014B	SSS	
						SCL4021B	SSS	
						CM4018AE	Solitron	
						CM4021AE	Solitron	
								(Continued)
8	1	PS	CMOS					(Cont'd)
				3 M	3-15	F4014BM	† Fairchild	
						F4021BM	† Fairchild	
						MC14014BA	† Motorola	
						MC14021BA	† Motorola	
						CD4014B	**† RCA**	**(838)**
						CD4021B	**† RCA**	**(838)**
						883/4014B	† SSS	
						883/4021B	† SSS	
						CM4014A	† Solitron	
						CM4021A	† Solitron	
				5 M	3-15	MM54C165	† National	
						MM74C165	National	
		SP	Bipolar					
				6 M	5	DM54L164A	† National	
						DM74L164A	National	
				12 M	5	SN54L164	† TI	
						SN74L164	TI	
				25 M	5	54164	† Fairchild	
						54LS164	† Fairchild	
						74164	Fairchild	
						74LS164	Fairchild	
						ZN54164	† Ferranti	
						ZN74164	Ferranti	
						HD74164	Hitachi	
						HD74LS164	Hitachi	
						SN54LS164	† Motorola	
						SN74LS164	Motorola	
						DM54164	† National	
						DM54LS164	† National	
						DM74164	National	
						DM74LS164	National	
						DM7570	† National	
						DM8570	National	
						54164	**† Signetics**	**(528,861)**
						54LS164	**† Signetics**	**(529)**
						74164	**Signetics**	**(861)**
						74LS164	Signetics	
						SN54164	**† TI**	**(979)**
						SN54LS164	**† TI**	**(979)**
						SN74164	**TI**	**(979)**
						SN74LS164	**TI**	**(979)**
						TD3503	Toshiba	
				350 M	−5.2	F10041	Fairchild	
			CMOS	5.5 M	3-15	MM54C164	† National	
						MM74C164	National	
		SS	Bipolar					
				3 M	5	**SN54L91**	**† TI**	**(952)**
						SN74L91	TI	
				4 M	5	DM54L91	† National	
						DM74L91	National	
				10 M	5	5491	† Fairchild	
						7491	Fairchild	
						ZN5491A	† Ferranti	
						ZN7491	Ferranti	
						MC5491A	† Motorola	
						MC7491A	Motorola	
						SN5491A	† National	
						SN7491A	National	
						5491	**† Signetics**	**(860)**
						7491	**Signetics**	**(860)**
						SN5491A	**† TI**	**(952)**
						SN54LS91	**† TI**	**(952)**
						SN7491A	**TI**	**(952)**
						SN74LS91	**TI**	**(952)**
			CMOS	2.5 M	3-15	MC14094BA	† Motorola	
						MC14094BC	Motorola	
						CD4094B	**† RCA**	**(838)**
								(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY-Shift Registers (Cont'd)

Bits Per Register	No. of Reg.	Oper-ation	Process	Frequency (Hz - Spec)	Supply Voltage, V	Device	Source
Static							**(Cont'd)**
8	1	SS	CMOS	2.5 M	3-15		(Cont'd)
						CD4094BE	**RCA (838)**
						883/4094B	† SSS
						SCL4094B	SSS
						TC4094B	Toshiba
	2	SS	Bipolar				
				10 M	5	93L28C	Fairchild
						93L28M	† Fairchild
						MC8328	Motorola
						MC9328	† Motorola
				15 M	5	RC8277	Raytheon
						RM8277	† Raytheon
						N8277	Signetics
				20 M	5	9328C	Fairchild
						9328M	† Fairchild
10	1	PP	Bipolar				
				25 M	5	RC8274	Raytheon
						RM8274	† Raytheon
						S8274	† Signetics
		SP	Bipolar				
				25 M	5	RC8273	Raytheon
						RM8273	† Raytheon
						N8273	**Signetics (876)**
						S8273	† Signetics
16	1	S/SP	Bipolar				
				20M	5	54F673	Fairchild
						54F674	Fairchild
						54F675	Fairchild
						54F676	**Fairchild (763)**
						74F673	Fairchild
						74F674	Fairchild
						74F675	Fairchild
						74F676	**Fairchild (763)**
						74F673	**Signetics (880)**
						74F674	**Signetics (880)**
						74F675	**Signetics (880)**
						74F676	**Signetics (880)**
		SP	NMOS	3.0M	5	**TSC9403**	**TeledyneS (3101)**
						TSC9404	**TeledyneS (3101)**
16-128	1	SS	CMOS	1.5 M	3-15	MC14562BC	Motorola
				3 M	3-15	MC14562BA	† Motorola
30	1	SS	CMOS	1 M	3-15	MD4330B	Mitel
32	6	SS	PMOS	1 M	− 12,5	3348	Fairchild
						3349	Fairchild
64	1	SS	CMOS	1 M	3-15	F4031BC	Fairchild
						CD4031BE	**RCA (838)**
				2 M	3-15	F4031BM	† Fairchild
						CD4031B	**† RCA (838)**
				2.7 M	3-15	F4557BM	† Fairchild
					3-16	MC1455BC	Motorola
				4 M	3-15	CD4031BC	National
						CD4031BM	† National
				5 M	3-15	F4557BC	Fairchild
					3-18	MC14557BA	† Motorola
				10 M	3-16	MS612	RTC
	2	SS	CMOS	4 M	3-15	MC14517BC	Motorola
						CD4517BE	**† RCA (838)**
						SCL4517B	SSS
				5 M	3-15	MC14517BA	† Motorola
						CD4517BE	† RCA
						883/4517B	† SSS
			TTL	30 M	5	TDC1005	† TRW-LSI
						TDC1005	TRW-LSI
	4	SS	CMOS	4 M	4.5-12.5	F4731BC	Fairchild
						F4731BM	† Fairchild
							(Continued)

Bits Per Register	No. of Reg.	Oper-ation	Process	Frequency (Hz - Spec)	Supply Voltage, V	Device	Source
64	4	SS					(Cont'd)
			PMOS	1.5 M	− 12,5	3342	Fairchild
80	4	SS	NMOS	1 M	5	SR5015-80	SMC
				3 M	5	M142	SGS
						M142A	SGS
			PMOS	1.5 M	− 12,5	AM3347	AMD
						3347	Fairchild
				2 M	− 12,5	3357-2	Fairchild
				2.5 M	− 12,5	AM2847M	† AMD
						F2847LM	† Fairchild
						F2847M	† Fairchild
				3 M	− 12,5	AM2847C	AMD
						F2847	Fairchild
						F2847L	Fairchild
				4 M	− 12,5	3357-1	Fairchild
						F3357M	† Fairchild
81	4	SS	NMOS	1 M	5	SR5015-81	SMC
						SR5018	SMC
96	4	SS	PMOS	2.5 M	− 12,5	AM2896M	† AMD
				3 M	− 12,5	AM2896C	AMD
128	1	SS	CMOS	5 M	12	MS625	RTC
	2	SS	PMOS	1 M	− 12,5	MK1002	AMD
				2 M	− 12,5	AM2809M	† AMD
						AM2810C	AMD
						AM2810M	† AMD
						TMS3114	AMD
				2.5 M	− 12,5	AM2809C	AMD
						AM2814C	AMD
						AM2814M	† AMD
	4	SS	PMOS	2.5 M	− 12,5	AM2855	AMD
						AM4055	† AMD
						AM5055	AMD
133	4	SS	NMOS	1 M	5	SR5015-133	SMC
						SR5017	SMC
256	1	SS	TTL	30 M	5	TDC1006	† TRW-LSI
						TDC1006	TRW-LSI
	2	SS	PMOS	2.5 M	− 12,5	AM2856	AMD
						AM4056	† AMD
						AM5056	AMD
512	1	SS	PMOS	2.5 M	− 12,5	AM2857C	AMD
						AM4057	† AMD
						AM5057	AMD
1024	1	SS	PMOS	1.5 M	− 12,5	AM2533	AMD
				2 M	− 12,5	AM2833C	AMD
						AM2833M	† AMD
92304	1	SS	Bubble				
				0.1 M	—	TIB0203S	TI
290560	1	SS	Bubble		—	H4701B	Hitachi

† Military Temperature Range (−55° to 125°C)
* Typical Values

SS = Serial In, Serial Out

PP = Parallel In, Parallel Out

Last Page This Section. Next Page 3901

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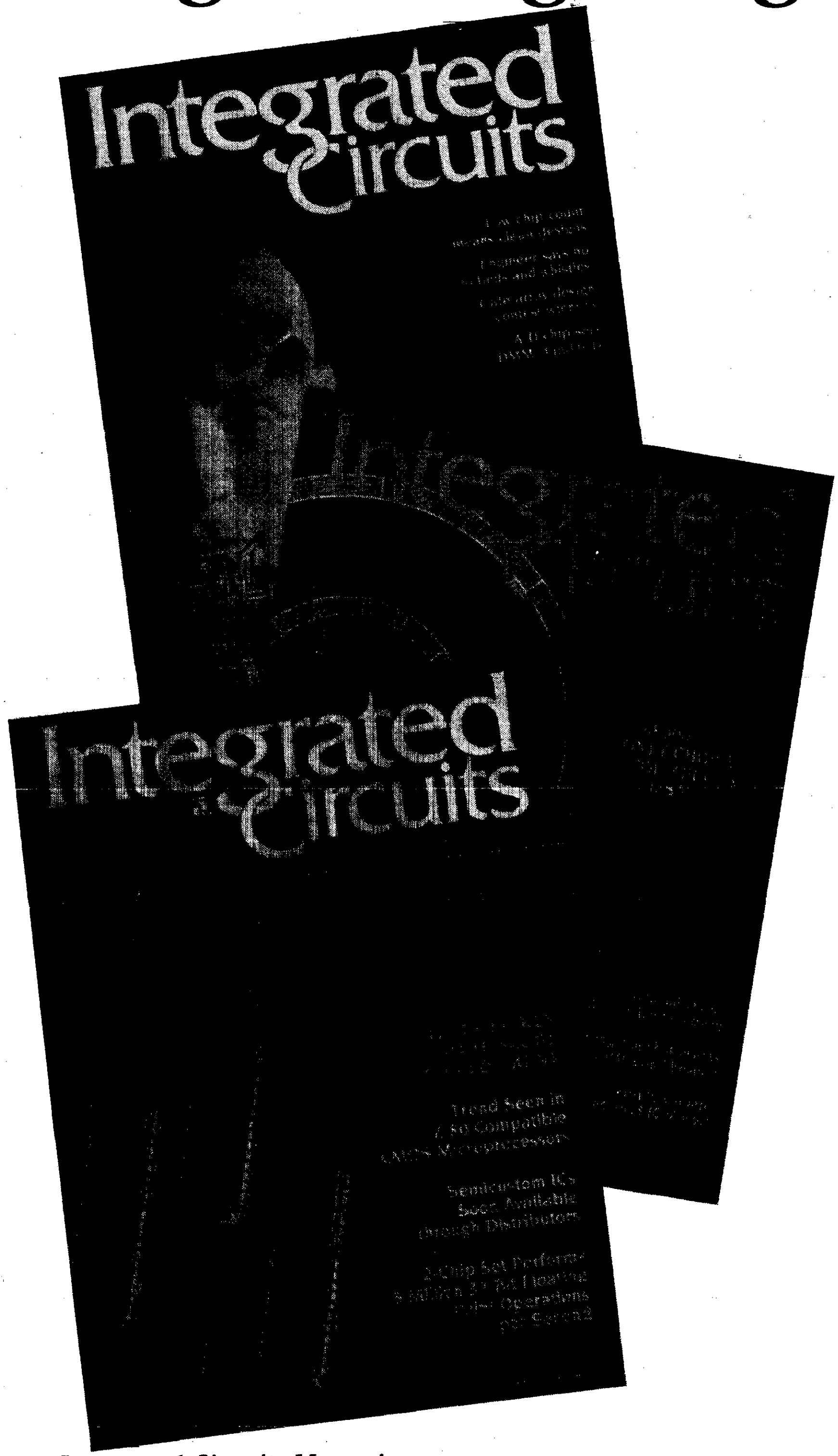

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Advanced Micro Devices

Bipolar Memories
Am27S35A/35/37A/37

DISTINCTIVE CHARACTERISTICS

- Member of AMD's Generic Family of 8-bit wide registered PROMs
- On-chip edge-triggered registers – ideal for pipelined microprogrammed systems
- Versatile synchronous and asynchronous enables for simplified word expansion
- Versatile programmable register INITIALIZE either asynchronous (Am27S35A/35) or synchronous (Am27S37A/37)
- Slim, 24-pin, 300-mil lateral center package occupies approximately 1/3 the board space required by standard discrete PROM and register
- Consumes approximately 1/2 the power of separate PROM/register combination for improved system reliability
- Fast standard version – 40ns max setup and 25ns max clock-to-output allows system speed improvements
- "A" version offers improved AC performance in critical paths (35ns max setup and 20ns max clock-to-output)
- Platinum-Silicide fuses guarantee high reliability, fast programming, and exceptionally high programming yields (typ>98%)
- AC performance is factory tested utilizing programmed test words and columns

GENERIC SERIES CHARACTERISTICS

The Am27S35A/35 and Am27S37A/37 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

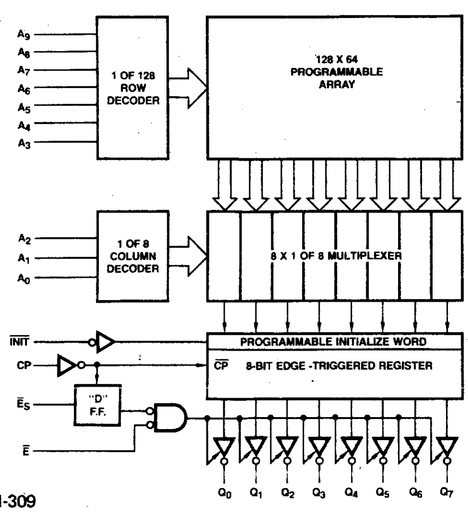
All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming equipment) these products can be rapidly programmed to any customized pattern. Extra test words are preprogrammed during manufacturing to insure extremely high field programming yields and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large nonconductive gaps that ensure long-term reliability. Extensive operating testing has shown that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage-compensated bias network to provide excellent parametric performance over the full military power supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

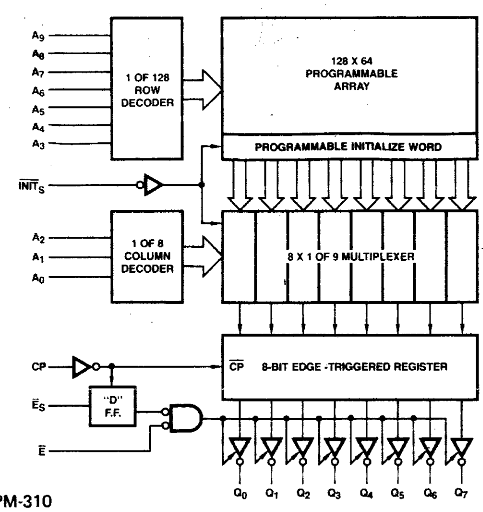
BLOCK DIAGRAMS

Am27S35



BPM-309

Am27S37



BPM-310

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Bipolar Memories
Am27S65/75/85

SERIAL SHADOW REGISTER (SSR) DIAGNOSTICS CAPABILITIES

- Serial access to output register to allow input of diagnostic control information
- Serial access of output register allows observation of register data
- Eliminates the need for diagnostics code internal to the PROM, allowing increased applications code density
- Simplified diagnostics increases system reliability
- Separate diagnostic register allows real time "snap shot" of machine state

DISTINCTIVE CHARACTERISTICS

- Highest density fastest performance PROM organization
- On-chip edge-triggered registers – ideal for pipelined microprogrammed systems
- On-chip diagnostic shift register for serial observability and controllability of the output register
- Fast standard version: 30ns max setup and 15ns max clock-to-output allows system speed improvements
- "A" version offers improved AC performance in critical paths (25ns max setup and 12ns max clock-to-output)
- User-programmable synchronous and asynchronous Enables
- User-programmable for synchronous or asynchronous Initialize
- Increased drive capability, 24mA I_{OL}
- THINDIP, 24-pin, 300-mil lateral center package increases overall board density
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ >98%)
- AC performance is factory tested utilizing programmed test rows and columns

GENERIC SERIES CHARACTERISTICS

The Am27S65, Am27S75, and Am27S85 are members of an advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW which can be selectively programmed to a logic HIGH by applying appropriate programming voltages to the circuit.

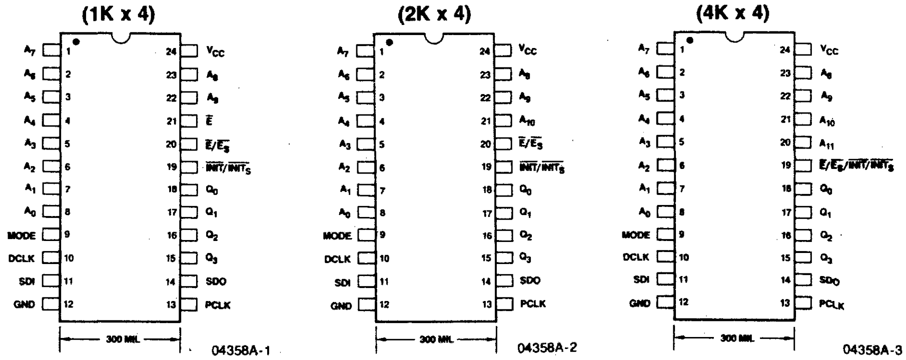
All parts are fabricated with AMD's fast-programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming algorithms (and common programming equipment), these products can be rapidly programmed to any customized pattern. Extra test words are preprogrammed during manufacturing to insure extremely high field programming yields and produce excellent AC and DC parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large nonconductive gaps that ensure very stable long-term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths, which are regulated by a built-in temperature- and voltage-compensated bias network to provide excellent parametric performance over the full military power supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

4-WIDE REGISTERED PROMs WITH SSR DIAGNOSTICS CONNECTION DIAGRAMS

Am27S65 (1K x 4) **Am27S75 (2K x 4)** **Am27S85 (4K x 4)**



Note: Pin 1 is marked for orientation.

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MEMORY

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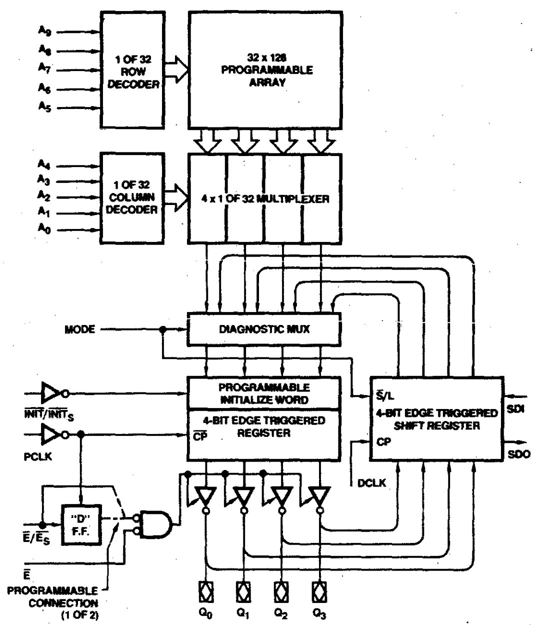
Bipolar Memories
Am27S65/75/85

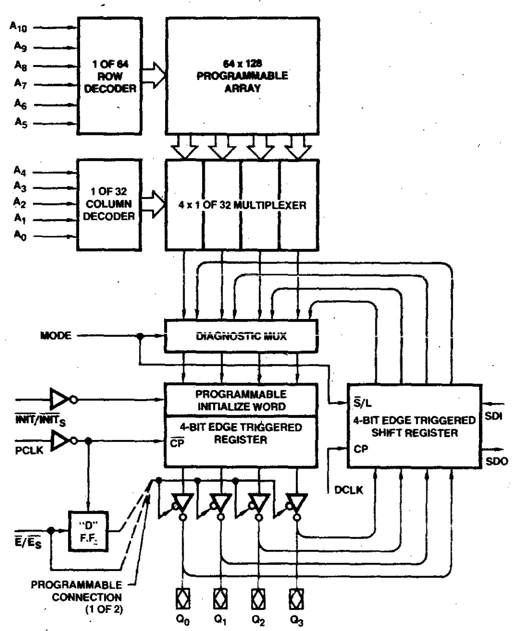
BLOCK DIAGRAMS

Am27S65
(1K x 4)



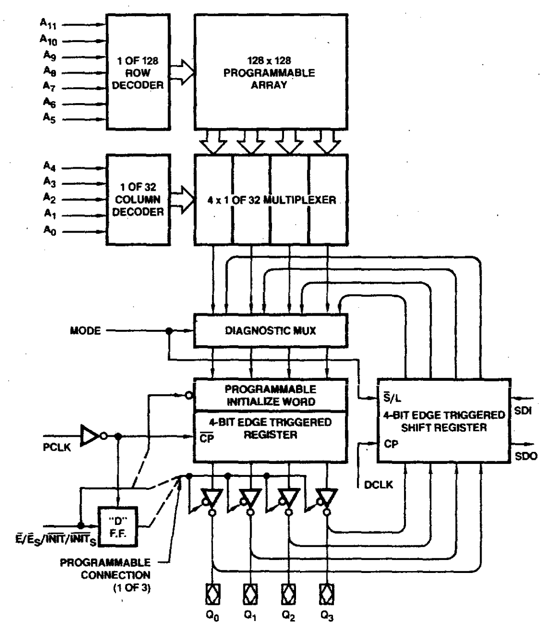
04358A-4

Am27S75
(2K x 4)



04358A-5

Am27S85
(4K x 4)



04358A-6

Advanced Micro Devices

Bipolar Memories
Am27S45A/45/47A/47

DISTINCTIVE CHARACTERISTICS

- Member of AMD's Generic Family of 8-bit wide registered PROMs
- On-chip edge-triggered registers – ideal for pipelined microprogrammed systems
- User programmable for synchronous or asynchronous enable for simplified word expansion
- Versatile programmable register INITIALIZE either asynchronous (Am27S45A/45) or synchronous (Am27S47A/47)
- Slim, 24-pin, 300-mil lateral center package occupies approximately 1/3 the board space required by standard discrete PROM and register
- Consumes approximately 1/2 the power of separate PROM/register combination for improved system reliability
- Fast standard version – 45ns max setup and 25ns max clock-to-output allows system speed improvements
- "A" version offers improved AC performance in critical paths (40ns max setup and 20ns max clock-to-output)
- Platinum-Silicide fuses guarantee high reliability, fast programming, and exceptionally high programming yields (typ>98%)
- AC performance is factory tested utilizing programmed test words and columns

GENERIC SERIES CHARACTERISTICS

The Am27S45A/45 and Am27S47A/47 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW which can be selectively programmed to a logic HIGH by applying appropriate programming voltages to the circuit.

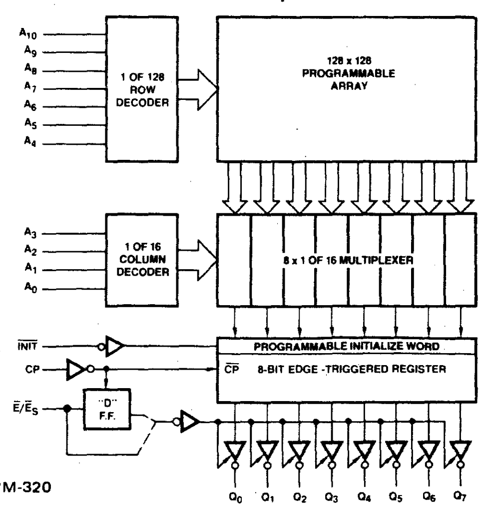
All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming algorithms (and common programming equipment) these products can be rapidly programmed to any customized pattern. Extra test words are preprogrammed during manufacturing to insure extremely high field programming yields and produce excellent AC and DC parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large nonconductive gaps that ensure very stable long-term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths, which are regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over the full military power supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

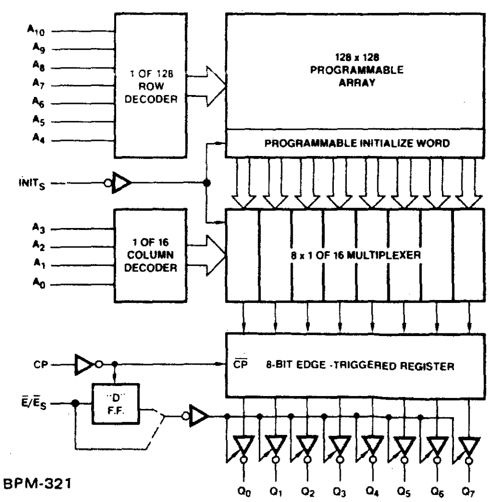
BLOCK DIAGRAMS

Am27S45A/45



BPM-320

Am27S47A/47



BPM-321

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MEMORY

Advanced Micro Devices

Bipolar Memories
Am27S180A/181A/280A/281A/180/181/280/281

DISTINCTIVE CHARACTERISTICS

Part Number	Package Width	Other Features
Am27S180A	24-Pin, Plug in Replacement for Industry Standard 600-mil Configuration No Board Changes Required	Ultra fast – 35ns max
Am27S181A		
Am27S180		Fast – 60ns max
Am27S181		
Am27S280A	New Space-Saving 24-Pin, THINDIP, 300-mil Configuration Increases Overall Board Density	Ultra fast – 35ns max
Am27S281A		
Am27S280		Fast – 60ns max
Am27S281		

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Bipolar Memories
Am27S180A/181A/280A/281A/180/181/280/281

DISTINCTIVE CHARACTERISTICS

- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- AC performance is factory tested utilizing programmed test words and columns
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Members of Generic PROM series utilizing standard programming algorithm

GENERIC SERIES CHARACTERISTICS

These 8K PROMs are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming equipment) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long-term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

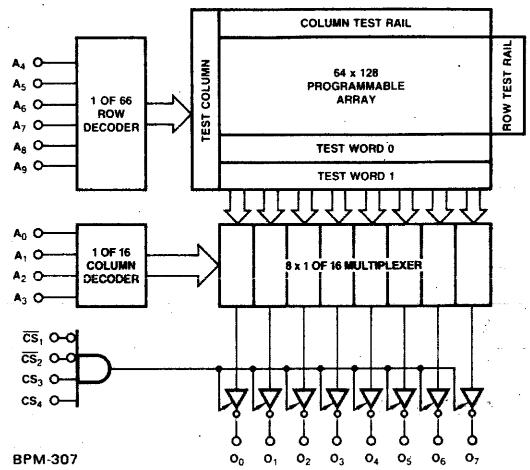
Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths.

These PROMs are manufactured using Advanced Micro Devices' selective oxidation process, IMOX. This advanced process combined with a merged fuse array permits an increase in density and a decrease in internal capacitance resulting in the fastest possible PROMs.

FUNCTIONAL DESCRIPTION

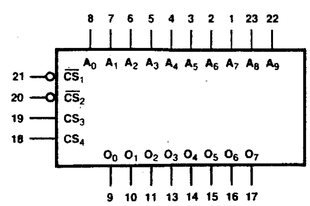
These 8K PROMs are high speed electrically programmable Schottky read only memories. Organized in the industry standard 1024 x 8 configuration, they are available in both open collector (Am27S180A/180 and Am27S280A/280) and three-state (Am27S181A/181 and Am27S281/281) output versions. After programming, stored information is read on outputs O_0-O_7 by applying unique binary addresses to A_0-A_9 and holding $\overline{CS}_1$ and $\overline{CS}_2$ LOW and CS_3 and CS_4 HIGH. All other valid input conditions on $\overline{CS}_1$, $\overline{CS}_2$, CS_3 and CS_4 place O_0-O_7 into the OFF or high impedance state.

BLOCK DIAGRAM



BPM-307

LOGIC DIAGRAM

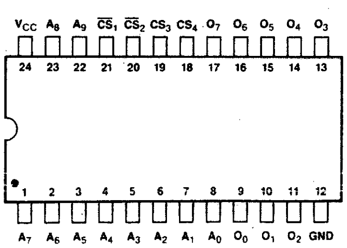


BPM-099

V_{CC} = Pin 24
GND = Pin 12

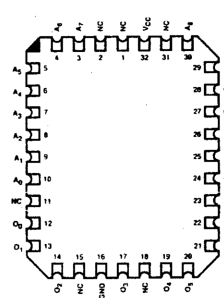
CONNECTION DIAGRAMS – Top Views

DIP



BPM-100

Chip-Pak™



BPM-279

Note: Pin 1 is marked for orientation.

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Advanced Micro Devices

MEMORY

Advanced Micro Devices

Bipolar Memories
Am27S40A/41A/40/41

DISTINCTIVE CHARACTERISTICS

- Ultra fast access time "A" version (35ns max) – Fast access time Standard version (50ns max) – allow tremendous system speed improvements
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- AC performance is factory tested utilizing programmed test words and columns
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Member of generic PROM series utilizing standard programming algorithm

GENERIC SERIES CHARACTERISTICS

These 16K PROMs are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long-term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

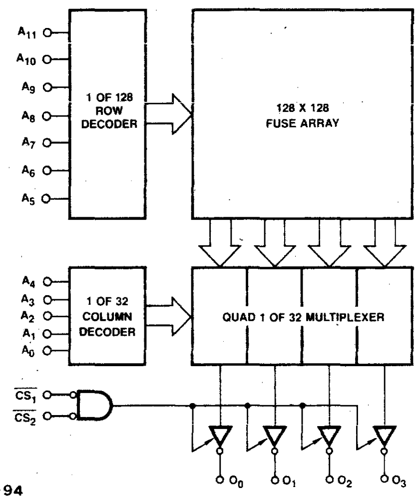
Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths.

These PROMs are manufactured using Advanced Micro Devices' selective oxidation process, IMOX™. This advanced process combined with a merged fuse array permits an increase in density and a decrease in internal capacitance resulting in the fastest possible PROMs.

FUNCTIONAL DESCRIPTION

The Am27S40A, Am27S41A, Am27S40, and Am27S41 are high speed electrically programmable Schottky read only memories. Organized in 4096 x 4 configuration, they are available in both open collector (Am27S40A and Am27S40) and three-state (Am27S41A and Am27S41) output versions. After programming, stored information is read on outputs O_0-O_3 by applying unique binary addresses to A_0-A_{11} and holding the chip select inputs, $\overline{CS}_1$ and $\overline{CS}_2$, LOW. If either chip select input goes to a logic HIGH, O_0-O_3 go to the OFF or HIGH impedance state.

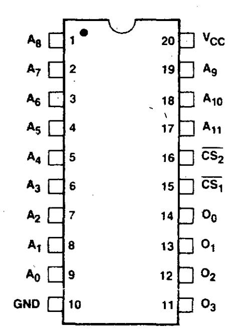
BLOCK DIAGRAM



BPM-194

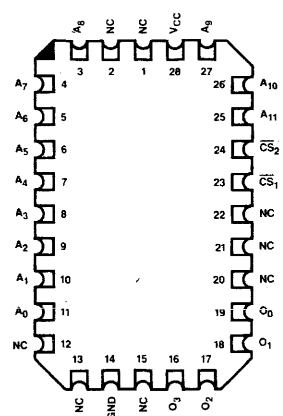
CONNECTION DIAGRAMS – Top Views

DIP



BPM-195

Chip-Pak™



BPM-196

Note: Pin 1 is marked for orientation.

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Advanced Micro Devices

Bipolar Memories
Am27S43A/43

DISTINCTIVE CHARACTERISTICS

- Ultra fast access time "A" version (40ns max) – Fast access time Standard version (55ns max) – allow tremendous system speed improvements
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- AC performance is factory tested utilizing programmed test words and columns
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Member of generic PROM series utilizing standard programming algorithm

GENERIC SERIES CHARACTERISTICS

These 32K PROMs are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long-term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

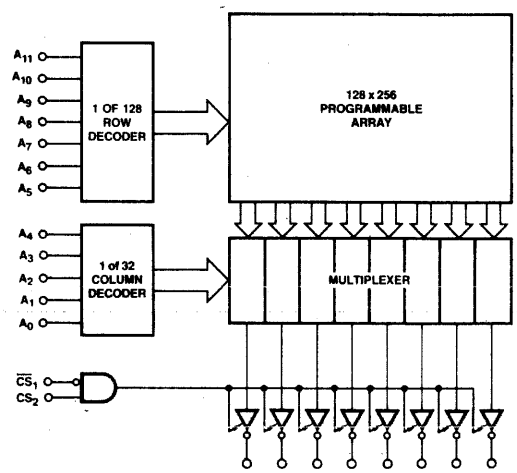
Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths.

These PROMs are manufactured using Advanced Micro Devices' selective oxidation process, IMOX™. This advanced process combined with a merged fuse array permits an increase in density and a decrease in internal capacitance resulting in the fastest possible PROMs.

FUNCTIONAL DESCRIPTION

The Am27S43A and Am27S43 are high speed electrically programmable Schottky read only memories. Organized in 4096 x 8 configuration, they are available in three-state (Am27S43A and Am27S43) output versions. After programming, stored information is read on outputs O_0-O_7 by applying unique binary addresses to A_0-A_{11} and holding the chip select inputs, $\overline{CS}_1$, LOW and CS_2, HIGH. If $\overline{CS}_1$ goes to logic HIGH or CS_2 goes to a logic LOW, O_0-O_7 go to the OFF or HIGH impedance state.

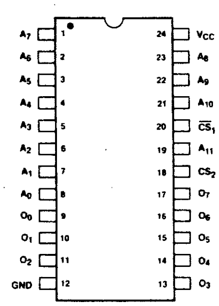
BLOCK DIAGRAM



BPM-265

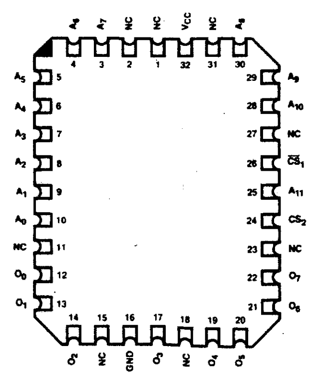
CONNECTION DIAGRAMS – Top Views

DIP



BPM-266

Chip-Pak™
L-32-2



BPM-267

Note: Pin 1 is marked for orientation.

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Advanced Micro Devices

Bipolar Memories
Am10415SA/415A/415

DISTINCTIVE CHARACTERISTICS

- Fast access time (10ns typ.) – improves system cycle speeds
- Fully compatible with standard voltage compensated 10K series ECL – no board changes required
- Internally voltage compensated providing flat AC performance
- Outputs preconditioned during write cycle eliminating write recovery glitch
- Emitter follower outputs – easy wire-ORing
- Power dissipation decreases with increasing temperature

FUNCTIONAL DESCRIPTION

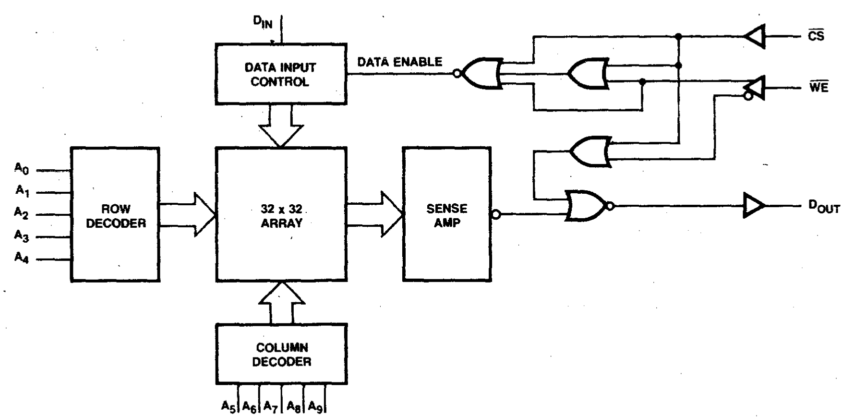
The Am10415SA, Am10415A and Am10415 are fully decoded 1024-bit ECL RAMs organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, A_0 through A_9. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and an unterminated OR tieable emitter follower output.

An active LOW write line ($\overline{WE}$) controls the write/read operation of the memory. When the chip select and write lines are LOW, the data input (D_{IN}) is written into the addressed memory word simultaneously preconditioning the output so true data is present when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch".

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the noninverting output (D_{OUT}).

During the writing operation or when the chip select line is HIGH the output of the memory goes to a LOW state.

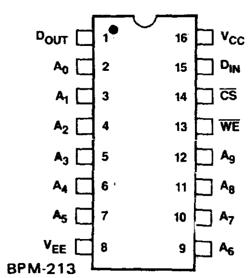
BLOCK DIAGRAM



BPM-212

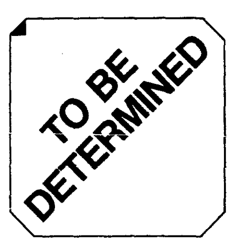
CONNECTION DIAGRAMS – Top Views

DIP



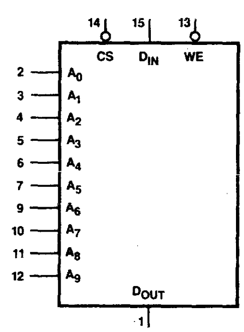
BPM-213

Chip-Pak™



Note: Pin 1 is marked for orientation.
The flatpackage version has the same pinout as the dual in-line package.

LOGIC SYMBOL



BPM-214

V_{CC} = Pin 16
V_{EE} = Pin 8

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Advanced Micro Devices

MEMORY

Advanced Micro Devices

Bipolar Memories
Am100415A/415

DISTINCTIVE CHARACTERISTICS

- Fast access time (10ns typ) – improves system cycle speeds
- Fully compatible with 100K series ECL logic – no board changes required
- Enhanced output voltage level compensation providing 6X (improvement in) V_{OL} and V_{OH} stability over supply and temperature ranges
- Internally voltage and temperature compensated providing flat AC performance
- Outputs preconditioned during write cycle eliminating write recovery glitch
- Emitter follower outputs – easy wire-ORing
- Power dissipation decreases with increasing temperature

FUNCTIONAL DESCRIPTION

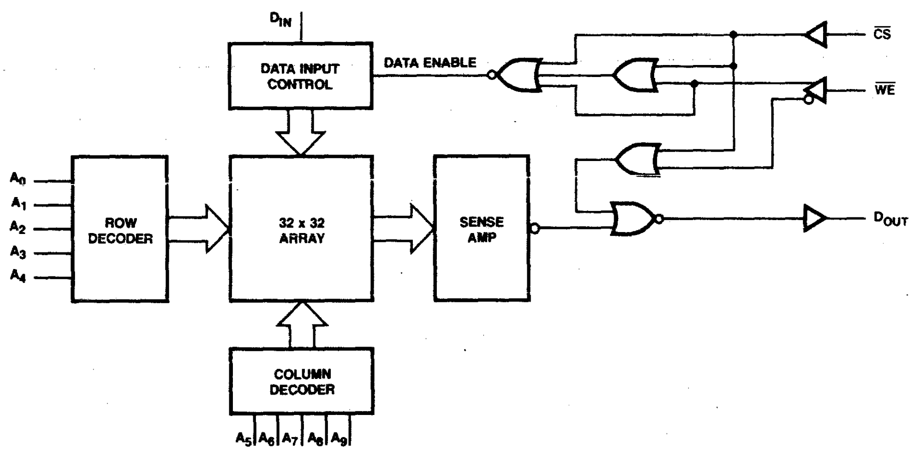
The Am100415A and Am100415 are fully decoded 1024-bit ECL RAMs organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, A_0 through A_9. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and an unterminated OR tieable emitter follower output.

An active LOW write line ($\overline{WE}$) controls the write/read operation of the memory. When the chip select and write lines are LOW, the data input (D_{IN}) is written into the addressed memory word simultaneously preconditioning the output so true data is present when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch".

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the noninverting output (D_{OUT}).

During the writing operation or when the chip select line is HIGH the output of the memory goes to a LOW state.

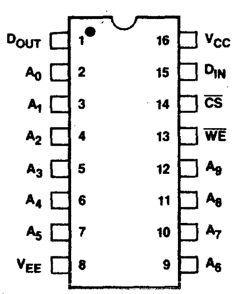
LOGIC BLOCK DIAGRAM



BPM-186

CONNECTION DIAGRAM – Top Views

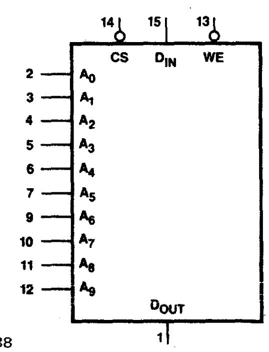
DIP



Chip-Pak™

BPM-187 Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 16
V_{EE} = Pin 8

BPM-188

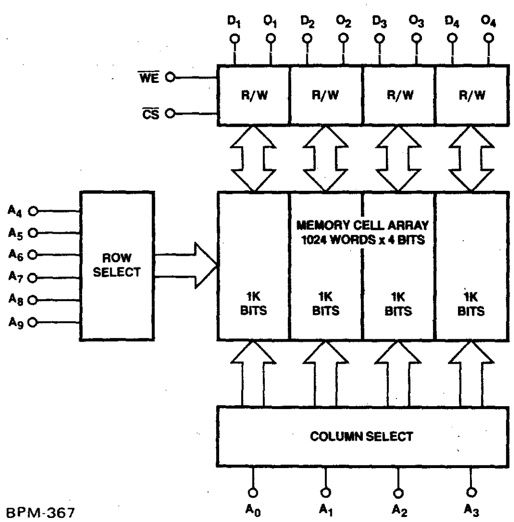
Advanced Micro Devices

Bipolar Memories
Am10474SA/474A/474

DISTINCTIVE CHARACTERISTICS

- Fast access time (12ns typ) – improves system cycle speeds
- Fully compatible with standard voltage compensated 10K series ECL – no board changes required
- Internally voltage and temperature compensated providing flat AC performance
- Emitter follower outputs – easy wire-ORing
- Power dissipation decreases with increasing temperature

LOGIC BLOCK DIAGRAM



BPM-367

FUNCTIONAL DESCRIPTION

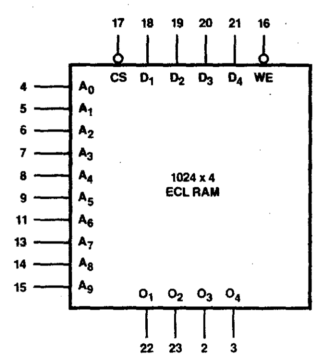
The Am10474SA, Am10474A and Am10474 are fully decoded 4096-bit ECL RAMs organized 1024 words by 4 bits. Word selection is achieved by means of a 10-bit address, A_0 through A_9. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and an unterminated OR tieable emitter follower output.

An active LOW write line ($\overline{WE}$) controls the write/read operation of the memory. When the chip select and write lines are LOW, the data input (D_1-D_4) are written into the addressed memory words.

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the noninverting outputs D_1-D_4.

During the writing operation or when the chip select line is HIGH the output of the memory goes to a LOW state.

LOGIC SYMBOL

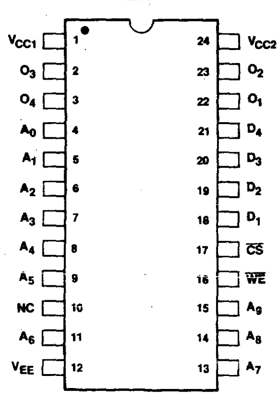


V_{CC2} = Pin 24
V_{EE} = Pin 12

BPM-368

CONNECTION DIAGRAMS – Top Views

DIP



Chip-Pak™

Note: Pin 1 is marked for orientation.

BPM-369

This document contains information on a product under development at Advanced Micro Devices, Inc. The information is intended to help you to evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.

Advanced Micro Devices

Bipolar Memories
Am100474SA/474A/474

DISTINCTIVE CHARACTERISTICS

- Fast access time (12ns typ) – improves system cycle speeds
- Fully compatible with 100K series ECL logic – no board changes required
- Enhanced output voltage level compensation providing 6X (improvement in) V_{OL} and V_{OH} stability over supply and temperature ranges
- Internally voltage and temperature compensated providing flat AC performance
- Emitter follower outputs – easy wire-ORing
- Power dissipation decreases with increasing temperature

FUNCTIONAL DESCRIPTION

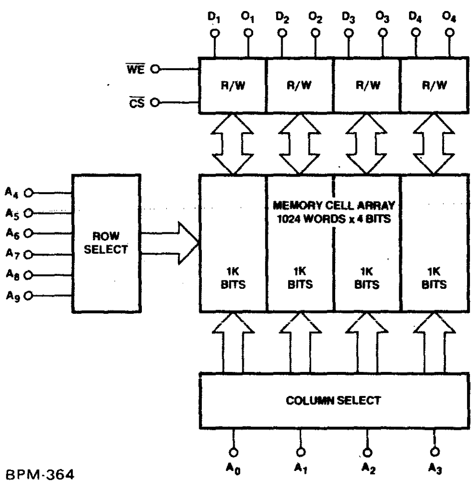
The Am100474SA, Am100474A and Am100474 are fully decoded 4096-bit ECL RAMs organized 1024 words by 4 bits. Word selection is achieved by means of a 10-bit address, A_0 through A_9. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and unterminated OR tieable emitter follower outputs.

An active LOW write line ($\overline{WE}$) controls the write/read operation of the memory. When the chip select and write lines are LOW, the data inputs (D_1-D_4) are written into the addressed memory words.

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed words is read out on the noninverting outputs O_1-O_4.

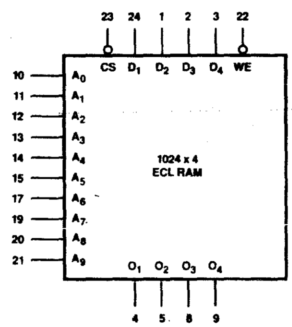
During the writing operation or when the chip select line is HIGH the output of the memory goes to a LOW state.

LOGIC BLOCK DIAGRAM



BPM-364

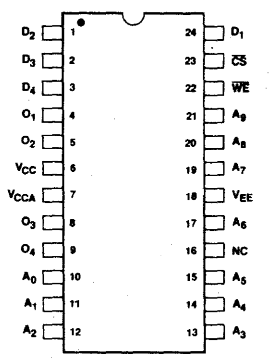
LOGIC SYMBOL



BPM-365

CONNECTION DIAGRAMS – Top Views

DIP



Chip-Pak™

Note: Pin 1 is marked for orientation.

BPM-366

This document contains information on a product under development at Advanced Micro Devices, Inc. The information is intended to help you to evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.

Advanced Micro Devices

Bipolar Memories
Am10470SA/470A/470

DISTINCTIVE CHARACTERISTICS

- Fast access time (12ns typ) – improves system cycle speeds
- Fully compatible with standard voltage compensated 10K series ECL – no board changes required
- Internally voltage compensated providing flat AC performance
- Outputs preconditioned during write cycle eliminating write recovery glitch
- Emitter follower outputs – easy wire-ORing
- Power dissipation decreases with increasing temperature

FUNCTIONAL DESCRIPTION

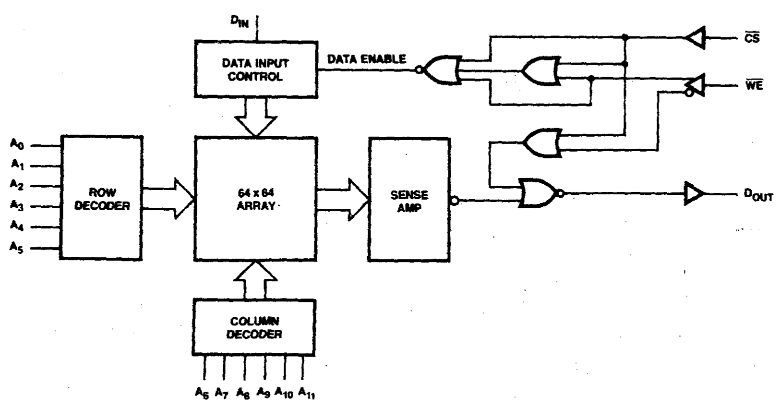
The Am10470SA, Am10470A and Am10470 are fully decoded 4096-bit ECL RAMs organized 4096 words by one bit. Bit selection is achieved by means of a 12-bit address, A_0 through A_{11}. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and an unterminated OR tieable emitter follower output.

An active LOW write line ($\overline{WE}$) controls the write/read operation of the memory. When the chip select and write lines are LOW, the data input (D_{IN}) is written into the addressed memory word simultaneously preconditioning the output so true data is present when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the 'write recovery glitch.'

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the noninverting output (D_{OUT}).

During the writing operation or when the chip select line is HIGH the output of the memory goes to a LOW state.

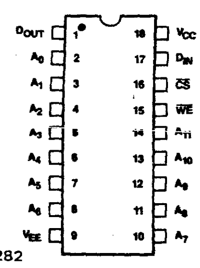
BLOCK DIAGRAM



BPM-299

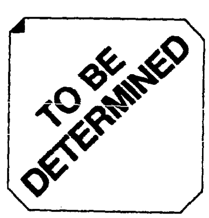
CONNECTION DIAGRAMS – Top Views

DIP



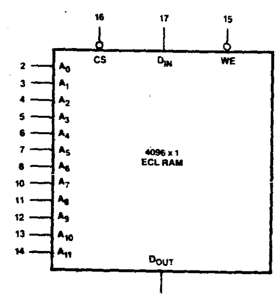
BPM-282

Chip-Pak™



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



BPM-283

V_{CC} = Pin 18
V_{EE} = Pin 9

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Advanced Micro Devices

Bipolar Memories
Am100470SA/470A/470

DISTINCTIVE CHARACTERISTICS

- Fast access time (12ns typ) – improves system cycle speeds
- Fully compatible with 100K series ECL logic – no board changes required
- Enhanced output voltage level compensation providing 6X (improvement in) V_{OL} and V_{OH} stability over supply and temperature ranges
- Internally voltage and temperature compensated providing flat AC performance
- Outputs preconditioned during write cycle eliminating write recovery glitch
- Emitter follower outputs – easy wire-ORing
- Power dissipation decreases with increasing temperature

FUNCTIONAL DESCRIPTION

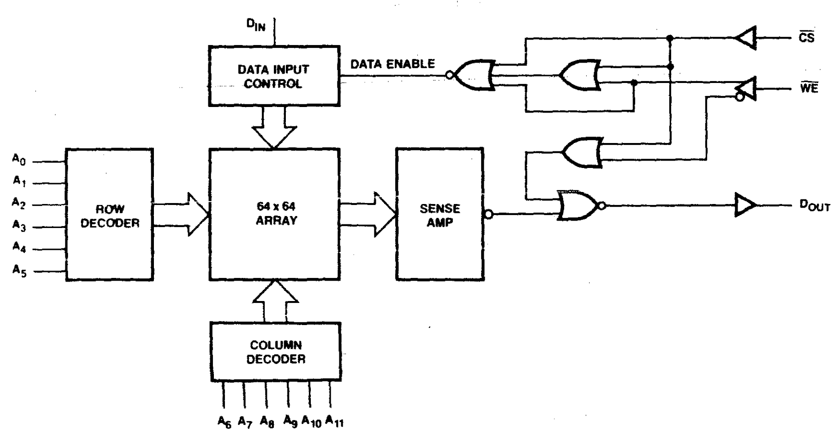
The Am100470SA, Am100470A and Am100470 are fully decoded 4096-bit ECL RAMs organized 4096 words by one bit. Bit selection is achieved by means of a 12-bit address, A_0 through A_{11}. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and an unterminated OR tieable emitter follower output.

An active LOW write line ($\overline{WE}$) controls the write/read operation of the memory. When the chip select and write lines are LOW, the data input (D_{IN}) is written into the addressed memory word simultaneously preconditioning the output so true data is present when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the 'write recovery glitch.'

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the noninverting output (D_{OUT}).

During the writing operation or when the chip select line is HIGH the output of the memory goes to a LOW state.

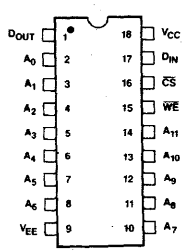
LOGIC BLOCK DIAGRAM



BPM-281

CONNECTION DIAGRAM – Top Views

DIP

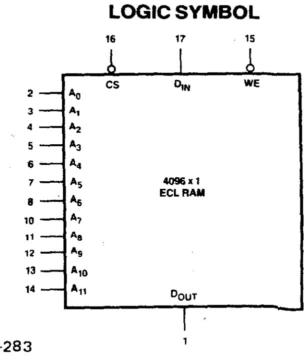


BPM-282

Chip-Pak™

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



BPM-283

V_{CC} = Pin 18
V_{EE} = Pin 9

Advanced Micro Devices

Bipolar Memories
Am10470SA/470A/470

DISTINCTIVE CHARACTERISTICS

- Fast access time (12ns typ) – improves system cycle speeds
- Fully compatible with standard voltage compensated 10K series ECL – no board changes required
- Internally voltage compensated providing flat AC performance
- Outputs preconditioned during write cycle eliminating write recovery glitch
- Emitter follower outputs – easy wire-ORing
- Power dissipation decreases with increasing temperature

FUNCTIONAL DESCRIPTION

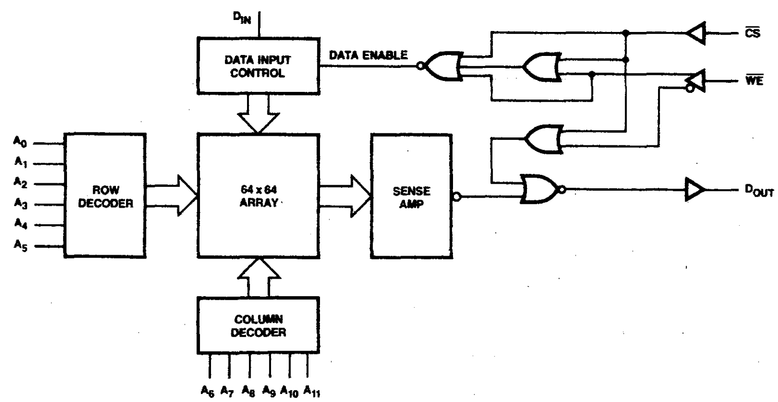
The Am10470SA, Am10470A and Am10470 are fully decoded 4096-bit ECL RAMs organized 4096 words by one bit. Bit selection is achieved by means of a 12-bit address, A_0 through A_{11}. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and an unterminated OR tieable emitter follower output.

An active LOW write line ($\overline{WE}$) controls the write/read operation of the memory. When the chip select and write lines are LOW, the data input (D_{IN}) is written into the addressed memory word simultaneously preconditioning the output so true data is present when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the 'write recovery glitch.'

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the noninverting output (D_{OUT}).

During the writing operation or when the chip select line is HIGH the output of the memory goes to a LOW state.

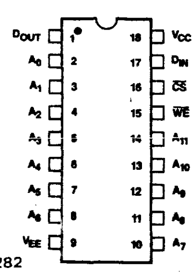
BLOCK DIAGRAM



BPM-299

CONNECTION DIAGRAMS – Top Views

DIP

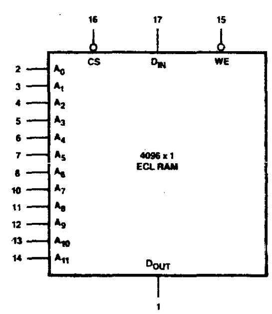


BPM-282

Chip-Pak™

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



BPM-283

V_{CC} = Pin 18
V_{EE} = Pin 9

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Advanced Micro Devices

Bipolar Memories
Am100470SA/470A/470

DISTINCTIVE CHARACTERISTICS

- Fast access time (12ns typ) – improves system cycle speeds
- Fully compatible with 100K series ECL logic – no board changes required
- Enhanced output voltage level compensation providing 6X (improvement in) V_{OL} and V_{OH} stability over supply and temperature ranges
- Internally voltage and temperature compensated providing flat AC performance
- Outputs preconditioned during write cycle eliminating write recovery glitch
- Emitter follower outputs – easy wire-ORing
- Power dissipation decreases with increasing temperature

FUNCTIONAL DESCRIPTION

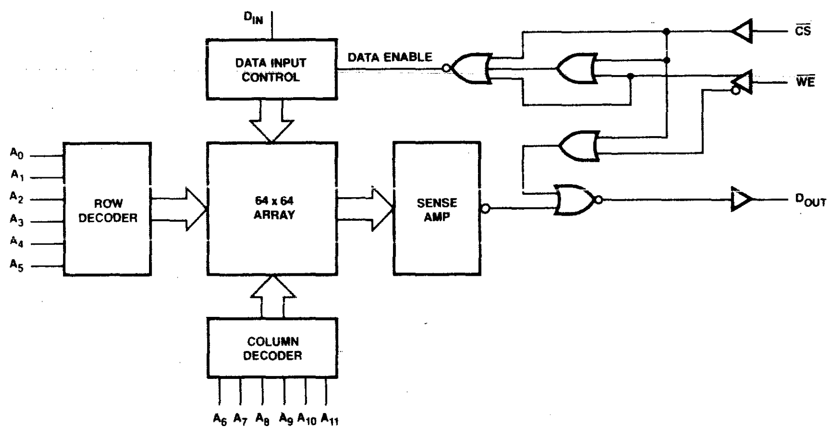
The Am100470SA, Am100470A and Am100470 are fully decoded 4096-bit ECL RAMs organized 4096 words by one bit. Bit selection is achieved by means of a 12-bit address, A_0 through A_{11}. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and an unterminated OR tieable emitter follower output.

An active LOW write line ($\overline{WE}$) controls the write/read operation of the memory. When the chip select and write lines are LOW, the data input (D_{IN}) is written into the addressed memory word simultaneously preconditioning the output so true data is present when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the 'write recovery glitch.'

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the noninverting output (D_{OUT}).

During the writing operation or when the chip select line is HIGH the output of the memory goes to a LOW state.

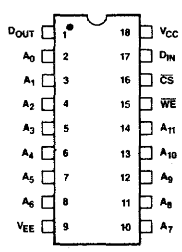
LOGIC BLOCK DIAGRAM



BPM-281

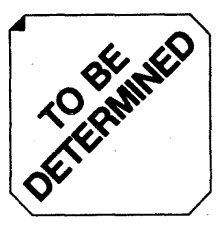
CONNECTION DIAGRAM – Top Views

DIP



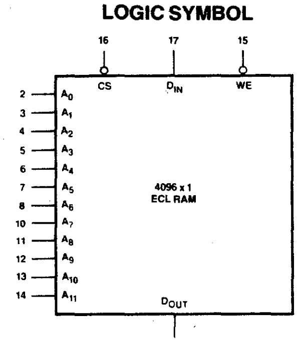
BPM-282

Chip-Pak™



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



BPM-283

V_{CC} = Pin 18
V_{EE} = Pin 9

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Advanced Micro Devices

MOS Memories
Am2167

DISTINCTIVE CHARACTERISTICS

- High speed – access times as fast as 35ns maximum
- 16K x 1 organization
- Single +5 volt power supply
- Fully static storage and interface circuitry
- No clocks or timing signals required
- Automatic power down when deselected
- Low power dissipation
  - Am2167: 660mW active, 110mW power down
- Standard 20-pin, .300 inch dual in-line package
- High output drive
  - Up to seven standard TTL loads or six Schottky TTL loads
- TTL compatible interface levels
- No power-on current surge

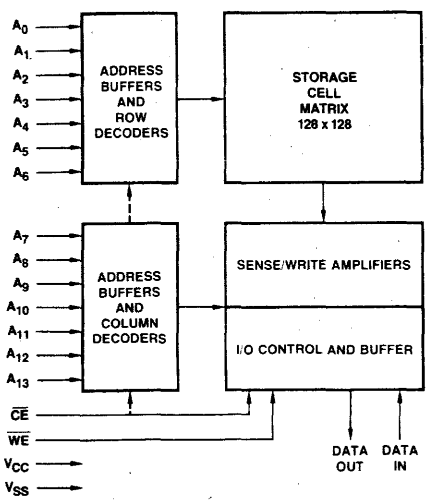
GENERAL DESCRIPTION

The Am2167 is a high performance, 16,384-bit, static, read/write, random access memory. It is organized as 16,384 words by one bit per word. All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive up to six standard Schottky TTL loads or up to seven standard TTL loads.

Only a single +5 volt power supply is required. When deselected ($\overline{CE} \geq V_{IH}$), the Am2167 automatically enters a power-down mode which reduces power dissipation by 80%.

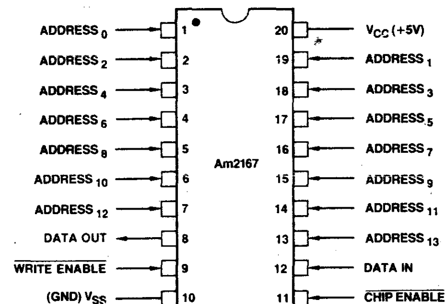
Data In and Data Out use separate pins and are the same polarity allowing them to be connected together for operation in a common data bus environment. Data Out is a three-state output allowing similar devices to be wire-OR'd together.

BLOCK DIAGRAM



03211B-1

CONNECTION DIAGRAM – Top View
D-20-1, P-20-1



03211B-2

Note: Pin 1 is marked for orientation.

PRODUCT SELECTIONS

	Am2167-35	Am2167-45	Am2167-55	Am2167-70
Maximum Access Time (ns)	35	45	55	70
Maximum Active Current (mA)	120	120 (160 mil)	120 (160 mil)	120 (160 mil)
Maximum Standby Current (mA)	20	20 (30 mil)	20 (30 mil)	20 (30 mil)
Full Military Operating Range Version	No	Yes	Yes	Yes

ORDERING INFORMATION

Am2167-35 Order Code	Am2167-45 Order Code	Am2167-55 Order Code	Am2167-70 Order Code	Package Type	Operating Range
Am2167-35PC	Am2167-45PC	Am2167-55PC	Am2167-70PC	P-20-1	COM'L
Am2167-35DC	Am2167-45DC	Am2167-55DC	Am2167-70DC	D-20-1	COM'L
–	Am2167-45DM	Am2167-55DM	Am2167-70DM	D-20-1	MIL
–	Am2167-45DMB	Am2167-55DMB	Am2167-70DMB	D-20-1	MIL

Notes: 1. P = Molded DIP, D = Hermetic DIP. Number following letter is number of leads.
2. See Operating Range table.

Advanced Micro Devices

MOS Memories
Am9122/L22

DISTINCTIVE CHARACTERISTICS

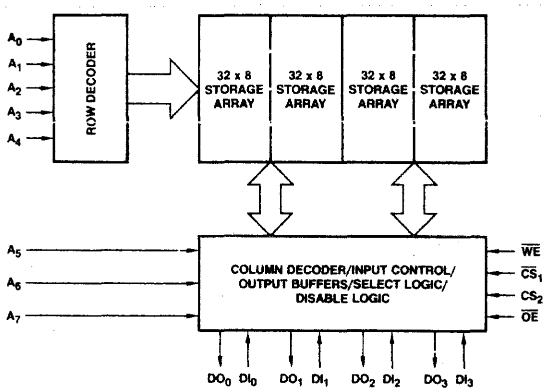
- High performance replacement for 93422/93L422
- 256 x 4 organization for small memory systems
- Fast access times – down to 25ns (Commercial)
  – down to 35ns (Military)
- Low operating power dissipation
  – Standard power: 660mW (Commercial)
    745mW (Military)
  – Low power: 248/440mW (Commercial)
    495mW (Military)
- Single 5 volt power supply – ±10% tolerance both commercial and military
- Guaranteed 0.1% AQL

FUNCTIONAL DESCRIPTION

The Am9122/Am91L22 series is a MOS pin-for-pin and functional replacement for the 93422/93L422 bipolar memories. These devices are high-performance, low-power, 1024-bit, static, read/write random access memories. They offer a wide range of access times including versions as fast as 25ns. Each memory is implemented as 256 words by 4 bits per word. This organization permits efficient design of small memory systems and allows finer resolution of incremental memory depth.

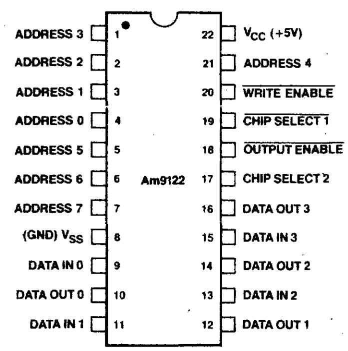
The Am9122/91L22 employs an output enable and two chip enable inputs to give the user better data control. High noise immunity, high output drive (4 TTL loads) and TTL logic voltage levels allow easy conversion from bipolar to MOS. 10% power supply tolerances give better margins in the memory system. As with all AMD MOS RAMs, the Am9122/91L22 is guaranteed to 0.1% AQL.

Am9122 BLOCK DIAGRAM



RAM-019

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation. RAM-020

SELECTION GUIDE

		Am9122-25	Am9122-35	Am91L22-35	Am91L22-45	Am91L22-60
Maximum Access Time (ns)		25	35	35	45	60
Maximum Operating Current (mA)	0 to 70°C	120	120	80	80	45
	–55 to 125°C	N/A	135	N/A	90	N/A

Advanced Micro Devices

MEMORY

Advanced Micro Devices

MOS Memories
Am9128

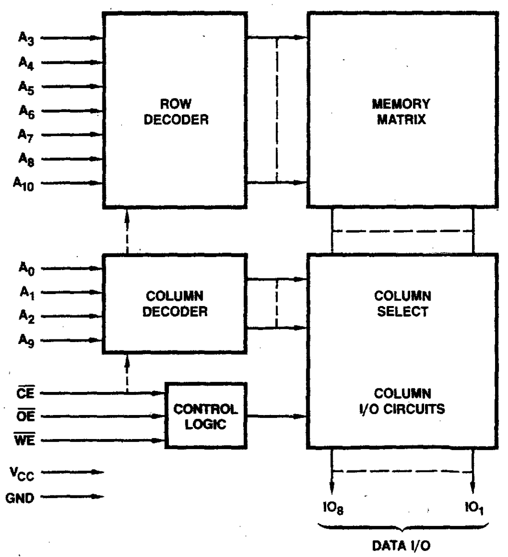
DISTINCTIVE CHARACTERISTICS

- 2,048 x 8-bit organization
- Logic voltage levels compatible with TTL
- Three-state output buffers-common I/O
- Fully static; no clocks or refresh required
- Single +5V power supply ±10% tolerance
- I_{CC} max as low as 100mA
- t_{AA}/t_{ACS} as low as 70ns
- Power down mode (I_{SB} as low as 15mA)
- Commercial and full military temperature ranges

GENERAL DESCRIPTION

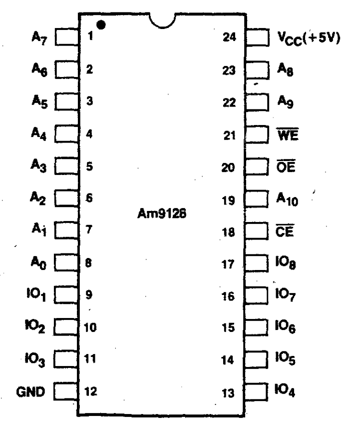
The Am9128 is a 16,384-bit static Random Access Read-write Memory organized as 2048 words of 8 bits. It uses fully static circuitry, requiring no clocks or refresh to operate. Directly TTL-compatible inputs and outputs and operation from a single +5V supply simplify system designs. Common data I/O pins using three-state outputs are provided. The Am9128 is available in an industry-standard 24-pin DIP package with 0.6-inch pin row spacing. The Am9128 uses the JEDEC standard pinout for byte-wide memories (compatible to 16K EPROM's).

BLOCK DIAGRAM



02050B-1

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

02050B-2

PRODUCT SELECTOR GUIDE

		Am9128-70	Am9128-90	Am9128-10	Am9128-12	Am9128-15	Am9128-20
Maximum Access Time (ns)		70	90	100	120	150	200
0 to 70°C	I_{CC} Max (mA)	140	N/A	120	N/A	100	140
	I_{SB} Max (mA)	30	N/A	15	N/A	15	30
−55 to 125°C	I_{CC} Max (mA)	N/A	180	N/A	150	150	150
	I_{SB} Max (mA)	N/A	30	N/A	30	30	30

Advanced Micro Devices

MOS Memories
Am9016

DISTINCTIVE CHARACTERISTICS

- High density 16K x 1 organization
- Replacement for MK4116
- Low maximum power dissipation – 462mW active, 20mW standby
- High-speed operation – 150ns access, 320ns cycle (COM'L)
  200ns access, 375ns cycle (MIL)
- ±10% tolerance on standard +12, +5, −5 voltages
- TTL compatible interface signals
- Three-state output
- RAS only, RMW and Page mode clocking options
- 128 cycle refreshing
- Unlatched data output
- Standard 16-pin, .3 inch wide dual-in-line package
- JEDEC standard 18-pin, Chip-Pak™ leadless chip carrier
- Double poly N-channel silicon gate MOS technology
- Extended ambient operating temperature (−55 to +85°C) available

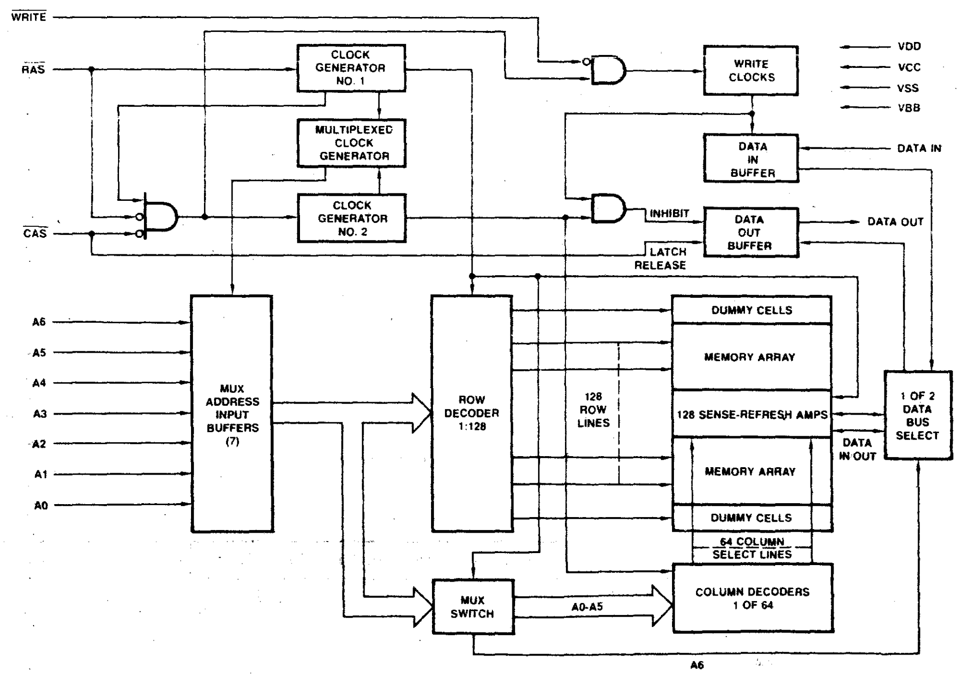
GENERAL DESCRIPTION

The Am9016 is a high-speed, 16K-bit, dynamic, read/write random access memory. It is organized as 16,384 words by 1 bit per word and is packaged in a standard 16-pin DIP or 18-pin leadless chip carrier. The basic memory element is a single transistor cell that stores charge on a small capacitor. This mechanism requires periodic refreshing of the memory cells to maintain stored information.

All input signals, including the two clocks, are TTL compatible. The Row Address Strobe (RAS) loads the row address and the Column Address Strobe (CAS) loads the column address. The row and column address signals share seven input lines. Active cycles are initiated when RAS goes low, and standby mode is entered when RAS goes high. In addition to normal read and write cycles, other types of operations are available to improve versatility, performance and power dissipation.

The 3-state output buffer turns on when the column access time has elapsed and turns off after CAS goes high. Input and output data are the same polarity.

BLOCK DIAGRAM



MOS-190

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Advanced Micro Devices

MOS Memories
Am9064

DISTINCTIVE CHARACTERISTICS

- High speed $\overline{RAS}$ access of 100 and 120ns
- Fast cycle time of 190 and 220ns
- Single +5V ± 10% power supply
- Temperature and power supply compensated on-chip substrate-bias generator
- Low power 22mW standby
  - 330mW active – 220ns cycle time
  - 385mW active – 190ns cycle time
- Read, Write, Read-Modify-Write, Page-Mode and RAS-Only refresh capability
- Early write common I/O capability
- $\overline{CAS}$ controlled three-state output
- 128 refresh cycles in 2ms
- Double poly NMOS silicon gate technology

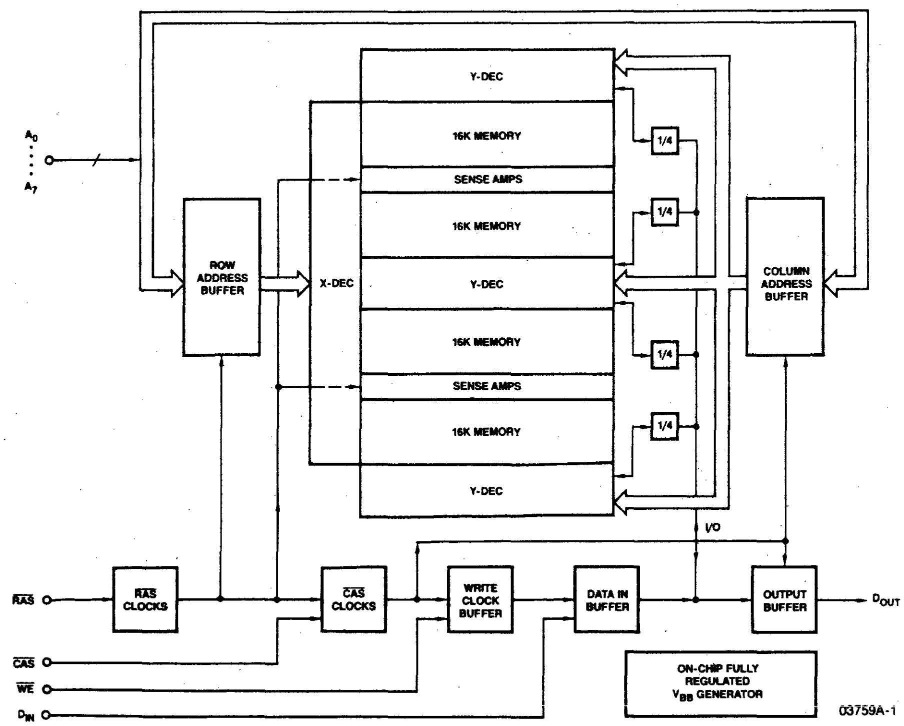
GENERAL DESCRIPTION

The Am9064 is a high speed, high-performance dynamic RAM, organized 65,536 x 1 and manufactured using advanced NMOS silicon-gate technology. The design is optimized for both high speed and low power dissipation, and only a single +5V supply is needed because the on-chip substrate-bias generator (compensated for temperature and supply variations) provides the necessary back bias.

The Am9064 features multiplexed addressing, and all input signals, including clocks, are TTL-compatible; input and output signals are the same polarity, and the three-state output buffer is $\overline{CAS}$ controlled. The Hi-C single-transistor memory cell is used to enhance signal margin and reduce the α-particle-induced soft-error rate.

Refresh is achieved by performing $\overline{RAS}$-only cycles or normal read/write cycles on 128 address combinations of ($A_0 - A_6$) within a 2ms period.

BLOCK DIAGRAM



ORDERING INFORMATION

Package Type	$\overline{RAS}$ Access Time		
	100ns	120ns	150ns
Plastic	Am9064-10PC	Am9064-12PC	Am9064-15PC
Cerdip	Am9064-10DC	Am9064-12DC	Am9064-15DC

Advanced Micro Devices

MOS Memories
Am2168/69

DISTINCTIVE CHARACTERISTICS

- High speed – access times as fast as 45ns maximum
- 4K x 4 organization
- Single +5 volt power supply
- Fully static storage and interface circuitry
- No clocks or timing signals required
- Automatic power down when deselected
- Power dissipation
  - Am2168: 660mW active; 165mW power down
    Am2169: 660mW
- Standard 20-pin, .300 inch dual-in-line package
- High output drive
  - Up to seven standard TTL loads or six Schottky TTL loads
- TTL compatible interface levels
- IMOS processing

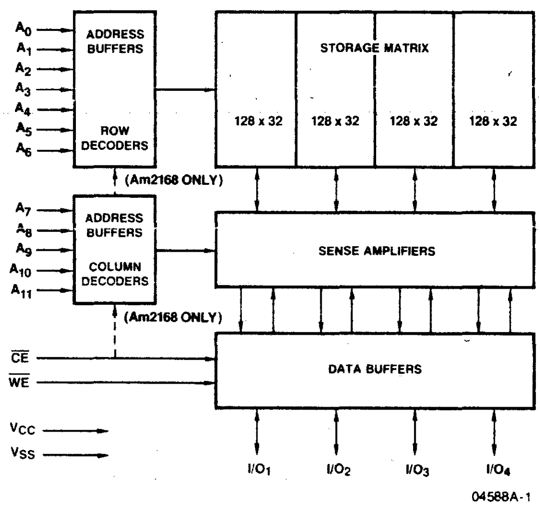
GENERAL DESCRIPTION

The Am2168 and Am2169 are high performance, static, N-Channel, read/write, random access memories organized as 4096 words of 4 bits. Operation is from a single 5V supply, and all input/output levels are identical to standard TTL specifications. The Am2168 and Am2169 are the same except that the Am2168 offers an automatic $\overline{CE}$ power down feature.

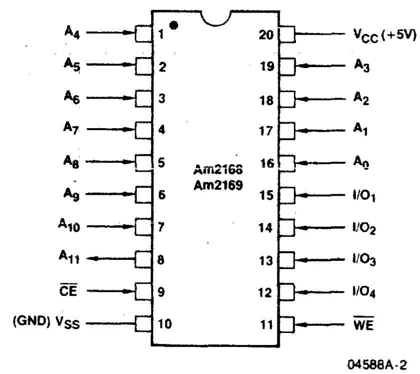
The Am2168 remains in a low-power standby mode as long as $\overline{CE}$ remains high, thus reducing its power requirements. The Am2168 power decreases from 660mW to 165mW in the standby mode. The $\overline{CE}$ input does not affect the power dissipation of the Am2169.

Data readout is not destructive and has the same polarity as data input. $\overline{CE}$ provides for easy selection of an individual device when the outputs are OR-tied.

BLOCK DIAGRAM



CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

PRODUCT SELECTIONS

		Am2168-45	Am2169-45	Am2168-55	Am2169-55	Am2168-70	Am2169-70
Maximum Access Time (ns)		45	45	55	55	70	70
0 to 70°C	I_{CC} (mA)	120	120	120	120	120	120
	I_{SB}* (mA)	30	N/A	30	N/A	30	N/A
−55 to +125°C	I_{CC} (mA)	N/A	N/A	160	160	160	160
	I_{SB}* (mA)	N/A	N/A	30	30	30	30

*Am2168 only

Advanced Micro Devices

MEMORY

Advanced Micro Devices

MOS Memories
Am9150

DISTINCTIVE CHARACTERISTICS

- 1024 x 4 organization
- High speed – 25ns max access time
- Separate data inputs and outputs
- Memory reset function
- High density SLIM 24-pin 300-MIL package
- Three-state output buffers
- Single +5V power supply ±10%

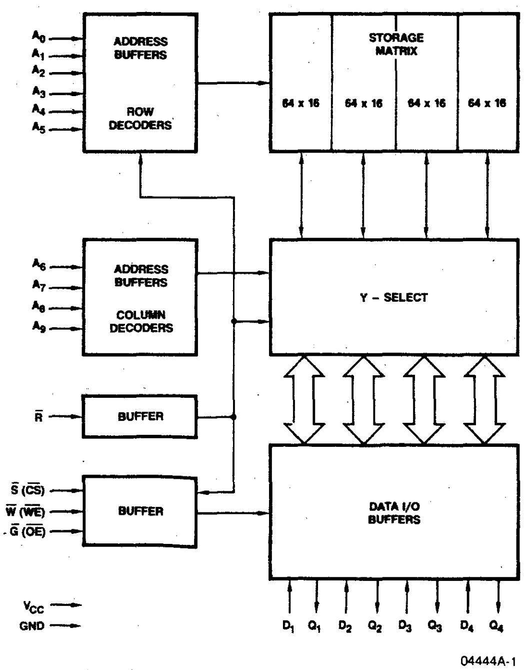
GENERAL DESCRIPTION

The Am9150 is a high-performance, static, n-channel, read/write, random access memory organized as 1024 x 4. It features single 5V supply operation, TTL-compatible input and output levels, and separate input and output pins for improved system performance and ease of use.

The Am9150 also incorporates a reset feature which will reset the entire contents of the memory to a logical LOW in two cycle times by controlling $\overline{R}$ ($\overline{RESET}$) and $\overline{S}$ ($\overline{CS}$).

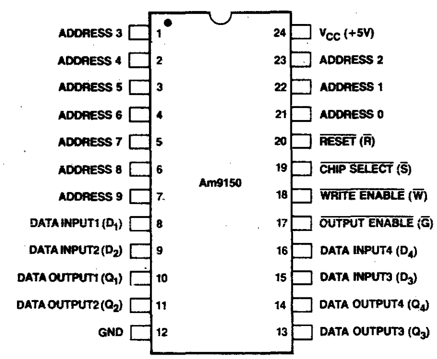
The Am9150 has four control signals, $\overline{R}$, $\overline{S}$, $\overline{W}$ and $\overline{G}$. The $\overline{S}$ input controls read, write and reset operations of the device and provides for easy selection of an individual device when the outputs are tied together. The $\overline{W}$ ($\overline{WE}$) input controls the normal read and write operations, and the $\overline{G}$ ($\overline{OE}$) controls the state of the outputs.

BLOCK DIAGRAM



04444A-1

CONNECTION DIAGRAM
Top View



04444A-2

Note: Pin 1 is marked for orientation.

FUNCTION TABLE

Inputs				Outputs	Mode
$\overline{S}$	$\overline{W}$	$\overline{G}$	$\overline{R}$		
H	X	X	X	High Z	Not Selected
L	H	X	L	High Z	Reset
L	L	X	H	High Z	Write
L	H	L	H	$Q_1 - Q_4$	Read
L	X	H	H	High Z	Output Disable

PRODUCT SELECTIONS

		Am9150-25	Am9150-35	Am9150-45
Maximum Access Time (ns)		25	35	45
I_{CC} Max (mA)	0 to +70°C	180	180	180
	−55 to +125°C	N/A	180	180

MOS Memories
Am9264

DISTINCTIVE CHARACTERISTICS

- Enhanced manufacturability with post-metal programming
- Access time – 250ns (max)
- Single +5V ±10% power supply
- Fully static operation
- Completely TTL compatible
- Standard 24 pin DIP
- Pin compatible with 16K/32K/64K EPROMs/ROMs
- Military version (−55 to +125°C) – Available – 450ns (max) access time

FUNCTIONAL DESCRIPTION

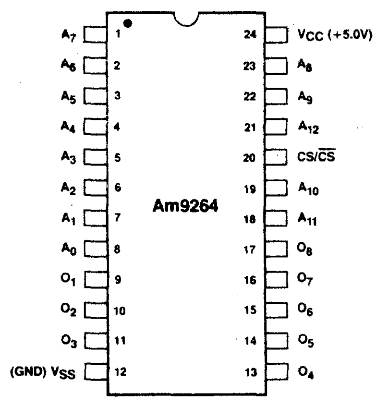
The Am9264 high performance read only memory is organized 8192 words by 8 bits with access times of less than 250ns. This organization simplifies the design of small memory systems and permits incremental memory sizes of 8192 words. The fast access times provided allow the ROM to service high performance microcomputer applications without stalling the processor.

The programmable chip select input signal is provided to control the output buffers. Chip Select Polarity may be provided by the customer thus allowing the addressing of 2 memory chips without external gating. The outputs of the unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am9264 devices and other three state components.

This memory is fully static and requires no clock signals of any kind. A selected chip will output data from a location specified by the address present on the address input lines. Input and output levels are compatible with TTL specifications.

The ability to program customer code at the last step of fabrication (Post Metal Programming Technique) will result in faster turn around time for new or old patterns. This technique will allow us to test wafers before committing customer patterns to categorize speed and power dissipation requirements.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

ROM-010

ORDERING INFORMATION

Package Type	Ambient Temperature Specifications	Access Time		
		450ns	300ns	250ns
Molded	0°C ≤ T_A ≤ +70°C	AM9264BPC	AM9264CPC	AM9264DPC
Cerdip	0°C ≤ T_A ≤ +70°C	AM9264BCC	AM9264CCC	AM9264DCC
Ceramic Side-Brazed	0°C ≤ T_A ≤ +70°C	AM9264BDC	AM9264CDC	AM9264DDC
	−55°C ≤ T_A ≤ +125°C	AM9264BDM		

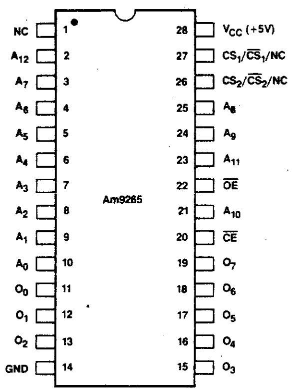
Advanced Micro Devices

MOS Memories
Am9265

DISTINCTIVE CHARACTERISTICS

- Enhanced manufacturability with post metal programming
- Access time – 250ns (max)
- Fully static operation
- Single +5V ± 10% power supply
- Automatic power down feature controlled by separate $\overline{CE}$ pin.
  - 80mA max operating current
  - 20mA max standby current
- Separate $\overline{OE}$ pin for tri-state output control
- Two programmable chip selects with no-connect option
- Pin compatible with 28 pin 64K and higher density ROMs/EPROMs
- Completly TTL compatible
- Standard 28 pin DIP
- Military version (−55 to +125°C) – Available with 450ns (max) access time

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation ROM-001

OPERATING RANGE

Part Number	Ambient Temperature	V_{CC}	V_{SS}
Am9265DC/PC/CC	$0°C \leq T_A \leq +70°C$	+5.0V ±10%	0V
Am9265DM	$-55°C \leq T_A \leq +125°C$	+5.0V ±10%	0V

FUNCTIONAL DESCRIPTION

The Am9265 high performance read only memory is organized 8192 words by 8 bits with access times of less than 250ns. This organization simplifies the design of small memory systems and permits incremental memory sizes of 8192 words. The fast access times provided allow the ROM to service high performance microcomputer applications without stalling the processor.

Two programmable chip select inputs are provided to control the output buffers. Chip select polarity may be specified by the customer thus allowing the addressing of 4 memory chips without external gating. The outputs of the unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am9265 devices and other three state components. No-connect option on chip selects can be provided if desired by the customer.

This memory is fully static and requires no clock signals of any kind. A selected chip will output data from a location specified by the address present on the address input lines. Input and output levels are compatible with TTL specifications. A separate $\overline{OE}$, output enable pin, controls outputs providing greater system flexibility and eliminating bus contention.

The Am9265 features an automatic stand-by mode. When deselected by $\overline{CE}$, the maximum supply current is reduced from 80mA to 20mA, a 75% reduction.

The ability to program customer code at the last step of fabrication (Post Metal Programming Technique) results in faster turn around time for new or old patterns. This technique also allows testing of wafers to categorize speed and power dissipation before committing customer patterns.

ORDERING INFORMATION

Package Type	Ambient Temperature Specifications	Access Time 450ns	300ns	250ns
Molded	$0°C \leq T_A \leq +70°C$	AM9265BPC	AM9265CPC	AM9265DPC
Cerdip	$0°C \leq T_A \leq +70°C$	AM9265BCC	AM9265CCC	AM9265DCC
Ceramic Side-Brazed	$0°C \leq T_A \leq +70°C$	AM9265BDC	AM9265CDC	AM9265DDC
	$-55°C \leq T_A \leq +125°C$	AM9265BDM		

Advanced Micro Devices

MOS Memories
Am92128

DISTINCTIVE CHARACTERISTICS

- Enhanced manufacturability with post metal programming
- Access time – 250ns (max)
- Fully static operation
- Single +5V ± 10% power supply
- Automatic power down feature controlled by separate $\overline{CE}$ pin
  80mA max operating current
  25mA max standby current
- Separate $\overline{OE}$ pin for three-state output control
- Programmable chip select with no-connect option
- Pin compatible with 28-pin and high density ROMs/EPROMs
- TTL compatible
- Standard 28-pin DIP
- Military version (–55 to +125°C) – Available with 450ns (max) access time

FUNCTIONAL DESCRIPTION

The Am92128 high performance read only memory is organized 16,384 words by 8 bits and has access times of less than 250ns. This organization simplifies the design of memory systems and permits incremental memory sizes of 16,384 bytes. The fast access times provided allow the ROM to service high performance microcomputer applications without inserting wait states.

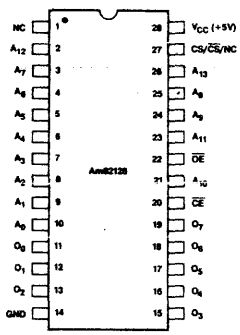
One programmable chip select input is provided to control the output buffers. Chip select polarity may be specified by the customer thus allowing the addressing of 2 memory chips without external gating. The outputs of the unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am92128 devices and other three-state components. No-connect option on chip select can be provided if desired by the customer.

This memory is fully static and requires no clock signals of any kind. A selected chip will output data from a location specified by the address present on the address input lines. Input and output levels are compatible with TTL specifications. A separate $\overline{OE}$, output enable pin, controls outputs providing greater system flexibility and eliminating bus contention.

The Am92128 features an automatic stand-by mode. When deselected by $\overline{CE}$, the maximum supply current is reduced from 80mA to 25mA, a 70% reduction.

The ability to program customer code at the last step of fabrication (Post Metal Programming Technique) results in faster turn around time for new or old patterns. This technique also allows testing of wafers to categorize speed and power dissipation before committing customer patterns.

CONNECTION DIAGRAM
Top View



ROM-008

Note: Pin 1 is marked for orientation.

PIN NAMES

$A_0 - A_{13}$	Address	$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable	V_{CC}	+5V
NC	No Connection	GND	Ground
CS/$\overline{CS}$	Chip Select	$O_0 - O_7$	Data Outputs

TRUTH TABLE

$\overline{CS}$ or CS		$\overline{CE}$	$\overline{OE}$	Mode	Outputs	Power
H	L	L	X	Deselected	High-Z	Active
H	L	H	X	Deselected	High-Z	Standby
L	H	L	H	Inhibit	High-Z	Active
L	H	H	X	Deselected	High-Z	Standby
L	H	L	L	Read	D_{OUT}	Active

H = HIGH (≥ 2.0V)
L = LOW (≤ 0.8V)
X = Don't Care

OPERATING RANGE

Part Number	Ambient Temperature	V_{CC}	V_{SS}
Am92128 X PC/CC	0°C ≤ T_A ≤ +70°C	+5.0V ±10%	0V
Am92128BDM	–55°C ≤ T_A ≤ +125°C	+5.0V ±10%	0V

ORDERING INFORMATION

Package Type	Ambient Temperature Specifications	Access Time		
		450ns	300ns	250ns
Molded	0°C ≤ T_A ≤ +70°C	Am92128BPC	Am92128CPC	Am92128DPC
Cerdip	0°C ≤ T_A ≤ +70°C	Am92128BCC	Am92128CCC	Am92128DCC
Side-Brazed	+55°C ≤ T_A ≤ +125°C	Am92128BDM		

Advanced Micro Devices

MOS Memories
Am92256

DISTINCTIVE CHARACTERISTICS

- Enhanced manufacturability with post metal programming
- Access time – 250ns (max)
- Fully static operation
- Single +5V ± 10% power supply
- Automatic power down feature controlled by separate $\overline{CE}$ pin
  - 120mA max operating current
  - 30mA max standby current
- Separate $\overline{OE}$ pin for three-state output control
- Pin compatible with 28-pin high density ROMs/EPROMs
- TTL compatible
- Standard 28-pin DIP

FUNCTIONAL DESCRIPTION

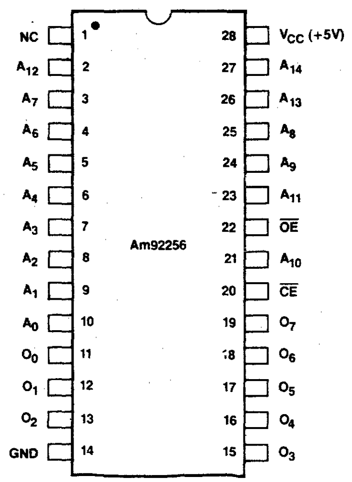
The Am92256 high performance read only memory is organized 32,768 words by 8 bits and has access times of less than 250ns. This organization simplifies the design of memory systems and permits incremental memory sizes of 32,768 bytes. The fast access times provided allow the ROM to service high performance microcomputer applications without inserting wait states.

The Am92256 features an automatic stand-by mode. When deselected by $\overline{CE}$, the maximum supply current is reduced from 120mA to 30mA, a 75% reduction. The outputs of the deselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am92256 devices and other three-state components.

This memory is fully static and requires no clock signals of any kind. A selected chip will output data from a location specified by the address present on the address input lines. Input and output levels are compatible with TTL specifications. A separate $\overline{OE}$, output enable pin, controls outputs providing greater system flexibility and eliminating bus contention.

The ability to program customer code at the last step of fabrication (Post Metal Programming Technique) results in faster turn around time for new or old patterns. This technique also allows testing of wafers to categorize speed and power dissipation before committing customer patterns.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation. ROM-005

PIN NAMES

A_0–A_{14}	Address	$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable	V_{CC}	+5V
NC	No Connection	GND	Ground
		O_0–O_7	Data Outputs

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	Mode	Outputs	Power
H	X	Deselect	High-Z	Standby
L	H	Inhibit	High-Z	Active
L	L	Read	D_{OUT}	Active

H = HIGH (≥ 2.0V)
L = LOW (≤ 0.8V)
X = Don't Care

OPERATING RANGE

Part Number	Ambient Temperature	V_{CC}	V_{SS}
Am92256PC/CC	0°C ≤ T_A ≤ +70°C	+5.0V ±10%	0V

ORDERING INFORMATION

Package Type	Ambient Temperature Specifications	Access Time 450ns	300ns	250ns
Molded	0°C ≤ T_A ≤ +70°C	Am92256BPC	Am92256CPC	Am92256DPC
Cerdip	0°C ≤ T_A ≤ +70°C	Am92256BCC	Am92256CCC	Am92256DCC

Advanced Micro Devices

MOS Memories
Am2732

DISTINCTIVE CHARACTERISTICS

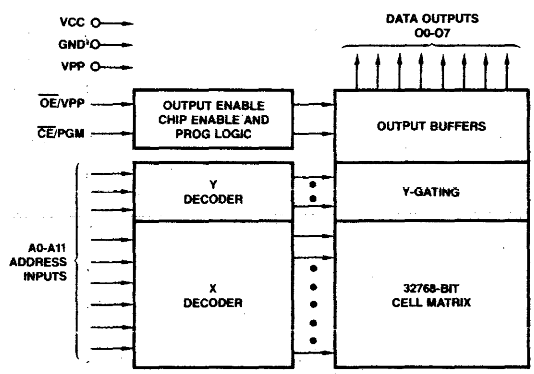
- 0.3% AQL guaranteed
- Direct replacement for Intel 2732
- Pin compatible with Am9233 – 32K ROM
- Single +5V power supply
- Fast access time – 350ns and 450ns
- Low power dissipation
  –787mW active
  –157mW standby
- Fully static operation – no clocks
- Three-state outputs
- TTL compatible inputs/outputs

GENERAL DESCRIPTION

The Am2732 is a 32768-bit ultraviolet erasable and programmable read-only memory. It is organized as 4096 words by 8 bits per word, operates from a single +5V supply, has a static standby mode, and features fast single address location programming.

Because the Am2732 operates from a single +5V supply, it is ideal for use in microprocessor systems. All programming signals are TTL levels, requiring a single pulse. For programming outside of the system, existing EPROM programmers may be used. Locations may be programmed singly, in blocks, or at random. Total programming time for all bits is 200 seconds.

BLOCK DIAGRAM



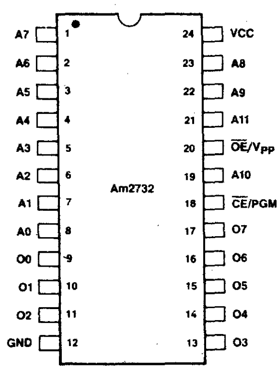
MOS-490

MODE SELECTION

Pins / Mode	CE/PGM (18)	OE/VPP (20)	VCC (24)	Outputs (9-11, 13-17)
Read	VIL	VIL	+5	DOUT
Standby	VIH	Don't Care	+5	High Z
Program	VIL	VPP	+5	DIN
Program Verify	VIL	VIL	+5	DOUT
Program Inhibit	VIH	VPP	+5	High Z

CONNECTION DIAGRAMS – Top Views

DIP

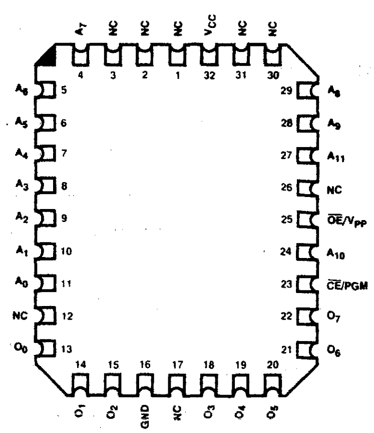


MOS-491

Pin 1 is marked for orientation.

A_0-A_{11}: Addresses
O_0-O_7: Outputs
CE/PGM: Chip Enable/Program
OE/VPP: Output Enable

Chip-Pak™
L-32-2



MOS-671

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

Advanced Micro Devices

MOS Memories
Am2732A

DISTINCTIVE CHARACTERISTICS

- Fast access times – 200ns, 250ns, 300ns, 450ns
- New low-cost plastic package for applications not requiring reprogramming
- Low power dissipation
  – 525mW active, 130mW standby
- ±10% V_{CC} supply tolerance available
- Three-state outputs
- 24-pin JEDEC approved 2732 pin-out
- Pin compatible with Am9233 – 32K-bit ROM
- Separate chip enable and output enable

GENERAL DESCRIPTION

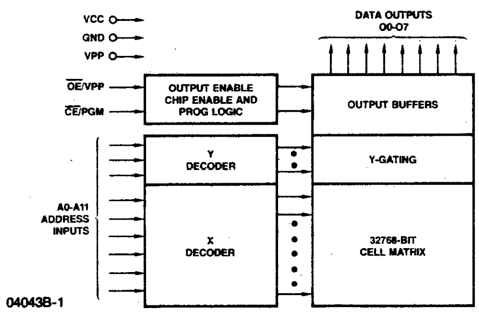
The Am2732A is a 32768-bit UV-light erasable and electrically programmable read-only memory, organized as 4096 words by 8-bits. The standard Am2732A offers an access time of 250ns, allowing operation with high-speed microprocessors without any WAIT state.

To eliminate bus contention in a multiple-bus microprocessor system, Am2732A offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks or at random.

The part is available in an economical plastic package for applications which do not require reprogramming.

BLOCK DIAGRAM



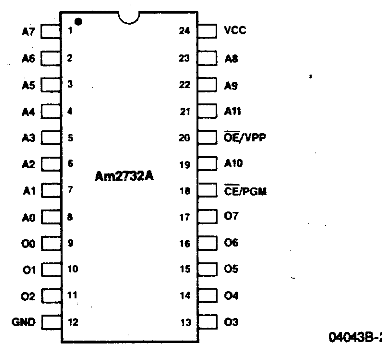
MODE SELECTION

Mode \ Pins	$\overline{CE}$/PGM (18)	$\overline{OE}$/VPP (20)	VCC (24)	Outputs (9-11, 13-17)
Read	VIL	VIL	+5	DOUT
Standby	VIH	X	+5	High Z
Program	VIL	VPP	+5	DIN
Program Verify	VIL	VIL	+5	DOUT
Program Inhibit	VIH	VPP	+5	High Z

X can be either V_{IL} or V_{IH}

Figure 1.

CONNECTION DIAGRAM – Top View
D-24-4



04043B-2

Pin 1 is marked for orientation.

A0-A11: Addresses
O0-O7: Outputs
$\overline{CE}$/PGM: Chip Enable/Program
$\overline{OE}$/VPP: Output Enable/VPP Supply

Figure 2.

ORDERING INFORMATION

Order Number[1]	t_{ACC} (ns)	t_{CE} (ns)	t_{OE} (ns)	V_{CC}	Temperature Range
AM2732APC	250	250	100	5V ±5%	C
AM2732A-2DX	200	200	70	5V ±5%	C, I, L
AM2732A-20DX	200	200	70	5V ±10%	C, I, L, M
AM2732A-DX	250	250	100	5V ±5%	C, I, L
AM2732A-25DX	250	250	100	5V ±10%	C, I, L, M
AM2732A-3DX	300	300	150	5V ±5%	C, I, L
AM2732A-30DX	300	300	150	5V ±10%	C, I, L
AM2732A-4DX	450	450	150	5V ±5%	C, I, L
AM2732A-45DX	450	450	150	5V ±10%	C, I, L, M

Note 1: X = C (0 to 70°C), X = I (–40 to +85°C), X = L (–55 to +100°C), X = M (–55 to +125°C).

Advanced Micro Devices

MOS Memories
Am2764

DISTINCTIVE CHARACTERISTICS

- Fast access time – 200ns, 250ns, and 300ns
- New low-cost plastic package for applications not requiring reprogramming
- Low power dissipation
  – 525mW active, 105mW standby
- ±10% power supply tolerance available
- 28-pin JEDEC approved 2764 pinout
- Pin compatible with Am9265 – 64K ROM
- Choice of 4 temperature ranges in ceramic package
- Fast programming time

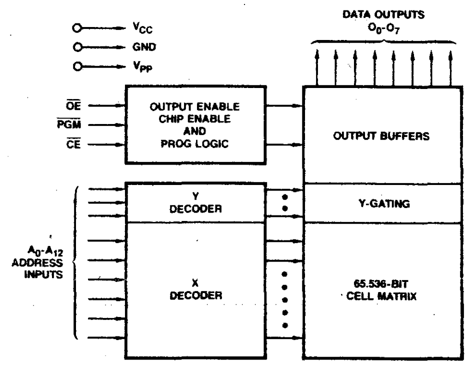
GENERAL DESCRIPTION

The Am2764 is a 65536-bit ultraviolet erasable and programmable read-only memory. It is organized as 8192 words by 8 bits per word, operates from a single +5V supply, has a static standby mode, and features fast single address location programming.

Because the Am2764 operates from a single +5V supply, it is ideal for use in microprocessor systems. All programming signals are TTL levels, requiring a single pulse. For programming outside of the system, existing EPROM programmers may be used. Locations may be programmed singly, in blocks, or at random.

The part ia available in an economical plastic package for applications which do not require reprogramming.

BLOCK DIAGRAM



01942D-1

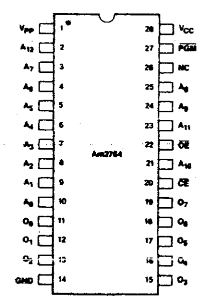
MODE SELECTION

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	X	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	High Z

X can be either V_{IL} or V_{IH}

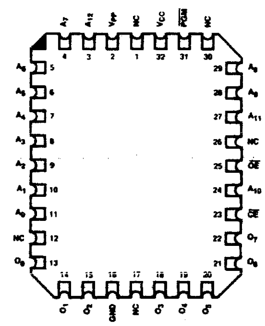
CONNECTION DIAGRAMS – Top Views

D-28-1
P-28-1



01942D-2

L-32-2



01942D-3

Pin 1 is marked for orientation.

A_0-A_{12}:	Addresses	$\overline{OE}$:	Output Enable
O_0-O_7:	Outputs	$\overline{PGM}$:	Program
$\overline{CE}$:	Chip Enable	NC:	No Connect

ORDERING INFORMATION

Order Number[1]	t_{ACC} (ns)	t_{CE}(ns)	t_{OE}(ns)	V_{CC}	Temperature Range
AM2764-2DX AM2764-2LX	200	200	75	5V ± 5%	C, I
AM2764-20DX AM2764-20LX	200	200	75	5V ± 10%	C, I
AM2764DX AM2764LX	250	250	100	5V ± 5%	C, I, L
AM2764-25DX AM2764-25LX	250	250	100	5V ± 10%	C, I, L, M
AM2764-3DX AM2764-3LX	300	300	120	5V ± 5%	C, I, L
AM2764-30DX AM2764-30LX	300	300	120	5V ± 10%	C, I, L
AM2764-4DX AM2764-4LX	450	450	150	5V ± 5%	C, I, L
AM2764-45DX AM2764-45LX	450	450	150	5V ± 10%	C, I, L, M
AM2764PC	250	250	100	5V ±5%	C

Note: 1. X = C (0 to +70°C), X = I (−40 to +85°C), X = L (−55 to 100°C), X = M (−55 to +125°C,.

Advanced Micro Devices

MOS Memories
Am27128

DISTINCTIVE CHARACTERISTICS

- Fast access time – 150ns, 200ns, 250ns, 300ns, 450ns
- Low power consumption
  - 525mW active
  - 130mW stand-by
- Single 5V power supply
- ±10% V_{CC} supply tolerance available
- Fully static operation – no clocks
- Separate chip enable and output enable controls
- TTL compatible inputs/outputs
- 28-pin JEDEC approved 27128 pin-out
- Pin compatible to Am2764 EPROM and Am92128-128K ROM
- Fast programming time (3 min typical)

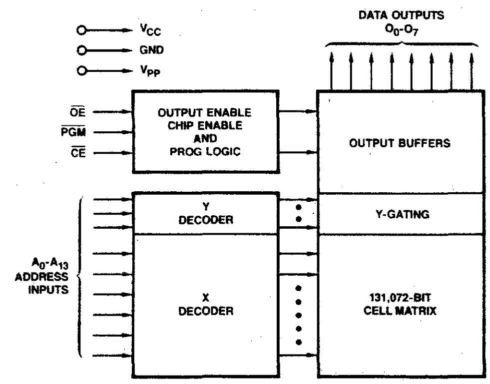
GENERAL DESCRIPTION

The Am27128 is a 131,072-bit UV-light erasable and electrically programmable read-only memory. It is organized as 16384 words by 8-bits per word. The standard Am27128 offers access time of 250ns, allowing operation with high-speed microprocessors without any WAIT state.

To eliminate bus contention in a multiple-bus microprocessor system, the Am27128 offers separate output enable ($\overline{OE}$) and chip enable ($\overline{CE}$) controls.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks or at random. To reduce programming time, the Am27128 may be programmed using 1ms pulses. Typically, Am27128 can be programmed in three minutes. See Flow Chart on page 6 for details.

BLOCK DIAGRAM



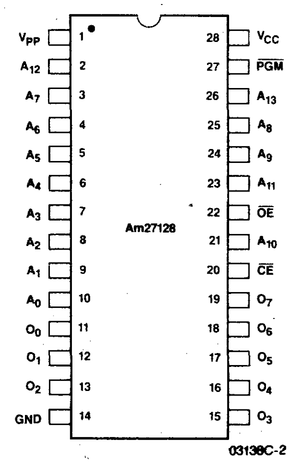
MODE SELECTION

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	High Z

X can be either V_{IL} or V_{IH}

Figure 1.

CONNECTION DIAGRAM – Top View



Note: Pin 1 is marked for orientation.

A_0-A_{13}:	Addresses	$\overline{OE}$:	Output Enable
O_0-O_7:	Outputs	$\overline{PGM}$:	Program
$\overline{CE}$:	Chip Enable		

Figure 2.

ORDERING INFORMATION

Order[1] Number	t_{ACC} (ns)	t_{CE} (ns)	t_{OE} (ns)	V_{CC}	Temperature Range
AM27128-1DX	150	150	75	5V ± 5%	C, I
AM27128-15DX	150	150	75	5V ± 10%	C, I
AM27128-2DX	200	200	75	5V ± 5%	C, I, L
AM27128-20DX	200	200	75	5V ± 10%	C, I, L, M
AM27128DX	250	250	100	5V ± 5%	C, I, L
AM27128-25DX	250	250	100	5V ± 10%	C, I, L, M
AM27128-3DX	300	300	120	5V ± 5%	C, I, L
AM27128-30DX	300	300	120	5V ± 10%	C, I, L
AM27128-4DX	450	450	150	5V ± 5%	C, I, L
AM27128-45DX	450	450	150	5V ± 10%	C, I, L, M

Note: 1. X = C (0 to +70°C), X = I (−40 to +85°C), X = L (−55 to +100°C), X = M (−55 to +125°C).

Advanced Micro Devices

MOS Memories
Am27256

DISTINCTIVE CHARACTERISTICS

- Fast access time – 170ns, 200ns, 250ns, 300ns, 450ns
- Programming voltage: 12.5V
- Low power consumption
  - 525mW active
  - 130mW stand-by
- Single 5V power supply
- ±10% V_{CC} supply tolerance available
- Fully static operation – no clocks
- Separate chip enable and output enable controls
- TTL compatible inputs/outputs
- 28-pin JEDEC approved Am27256 pin-out
- Pin compatible to Am2764 EPROM, Am27128 EPROM and Am92256 – 256K ROM
- Fast progamming time (5 min typical)
- Auto select mode for automated programming

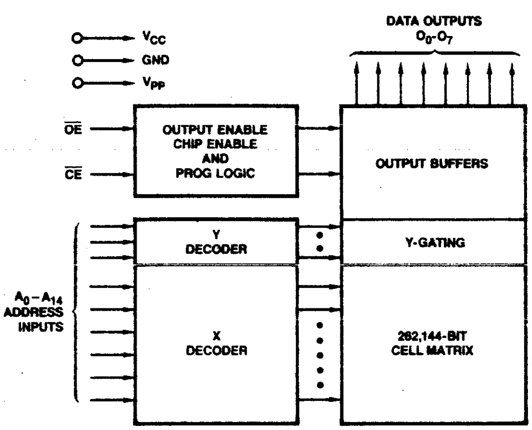
GENERAL DESCRIPTION

The Am27256 is a 262,144 bit UV-light erasable and electrically programmable read-only memory. It is organized as 32,768 words by 8-bits per word. The standard Am27256 offers access time of 250ns, allowing operation with high-speed microprocessors without any WAIT state.

To eliminate bus contention on a multiple-bus microprocessor system, the Am27256 offers separate output enable ($\overline{OE}$) and chip enable ($\overline{CE}$) controls.

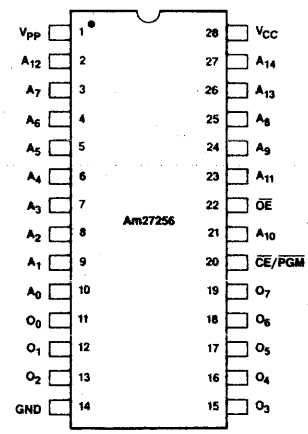
All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks or at random. To reduce programming time, the Am27256 may be programmed using 1ms pulses. Typically, the Am27256 can be programmed in five minutes.

BLOCK DIAGRAM



040698-1

CONNECTION DIAGRAM – Top View



Note: Pin 1 is marked for orientation. 040698-2

$A_0 - A_{14}$: Addresses — $\overline{OE}$: Output Enable

$O_0 - O_7$: Outputs — $\overline{CE}/\overline{PGM}$: Chip Enable/Program

Figure 2.

Figure 1. Mode Select

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A_9 (24)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	X	V_{CC}	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	V_{CC}	High Z
Stand By	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High Z
Auto Select	V_{IL}	V_{IL}	V_H	V_{CC}	V_{CC}	Code

Note: X can be either V_{IL} or V_{IH}
V_H = 12.0V ±0.5V

ORDERING INFORMATION

Order Number	t_{ACC} (ns)	t_{CE} (ns)	t_{OE} (ns)	V_{CC}
Am27256-1DC	170	170	75	5V ±5%
Am27256-2DC	200	200	75	5V ±5%
Am27256-20DC	200	200	75	5V ±10%
Am27256DC	250	250	100	5V ±5%
Am27256-25DC	250	250	100	5V ±10%
Am27256-3DC	300	300	120	5V ±5%
Am27256-30DC	300	300	120	5V ±10%
Am27256-4DC	450	450	150	5V ±5%
Am27256-45DC	450	450	150	5V ±10%

ABBREVIATIONS OF COMPANY NAMES

Action Ins	Action Instruments
AD	Analog Devices
ADT	Advanced Digital Technology
Advent	Advent Products, Inc.
Alphatron	Alphatron
AMA	American Automation
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
Amperex	Amperex Electronic Corp.
Analogic	Analogic
Analog Sys	Analog Systems
APC	Applied Micro Circuits
Apex	Apex Microtechnology
APM	Applied Microsystems Corp.
Appl Sys	Applied Systems Corp.
APT	Applied Microtechnology
Aptek	Aptek Microsystems
Array Tech	Array Technology
AWI	AWI Electronics
Barvon	Barvon Research
Bedford	Bedford Computer Systems Inc.
Burr-Brown	Burr-Brown
CAE	Computer Aided Engineering
Cal Devices	California Devices
Cermetek	Cermetek
CGRS	CGRS Microtech Inc.
Cherry	Cherry Semiconductor
CIC	Custom Integrated Circuits
CirTech	Circuit Technology
Citel	Citel
Comlinear	Comlinear Corporation
CMA	Custom MOS Arrays
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Comdial	Comdial Semiconductor
Comp Auto	Computer Automation
Compas	Compas Microsystems
Cont Logic	Control Logic Inc.
Control Sys	Control Systems Microsystems Div.
CreMicro	Creative Micro Systems
Cromemco	Cromemco, Inc.
Cubit	Cubit Inc.
Curtis	Curtis Electro Devices, Inc.
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Cybersys	Cybersystems
Cybertek	Cybertek Inc.
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Data Trans	Data Translation
Datel	Datel
Datricon	Datricon Corporation
DDC	Data Devices Corporation
DEC	Digital Equipment Corporation
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Digelec	Digelec Corp.
Digitek	Digitek, Inc.
Dionics	Dionics Inc.
Dist Comp	Distributed Computer Systems
Divers Tech	Diversified Technology
E-HI	E-H International, Inc.
EDI	Electronic Designs Inc.
Elind	Elind Elettronica Industriale
EMM-SESCO	EEM-SESCO
Emulogic	Emulogic Inc.
ETI Micro	ETI Micro
Exar	Exar Integrated Systems
Exel	Exel Microelectronics
Fairchild	Fairchild
Ferranti	Ferranti Electric
Force	Force Computers
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Fujitsu	Fujitsu Microelectronics, Inc.
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GTE Micro	GTE Microcircuits
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HP	Hewlett-Packard
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HyComp	HyComp
ICC	International Cybernetics
IDT	Integrated Device Technology
IMI	International Microcircuits, Inc.
IMP	International Microelectronic Products
IMS	Industrial MicroSystems Inc.
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S MOS	S MOS Systems
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SSS	Solid State Scientific
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AMI

A Subsidiary of Gould Inc.

S2333

32,768 BIT (4096x8) STATIC NMOS ROM

Features

- ☐ Fast Access Time: 350ns Maximum
- ☐ Fully Static Operation
- ☐ Single +5V ±5% Power Supply
- ☐ Directly TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Two Programmable Chip Selects
- ☐ EPROM Pin Compatible (2732)
- ☐ Extended Temperature Range Available

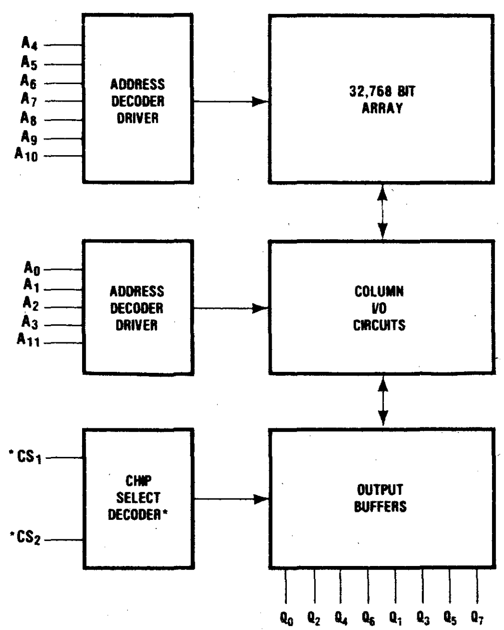
General Description

The AMI S2333 is a 32,768 bit static mask programmable NMOS ROM organized as 4096 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and has a single +5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S2333 is pin compatible with UV EPROMs making system development much easier and more cost effective. The fully static S2333 requires no clocks for operation. The two chip selects are mask programmable with the active level for each being specified by the user.

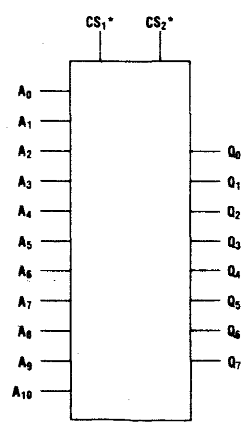
The S2333 is fabricated using AMI's N-Channel MOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

Block Diagram

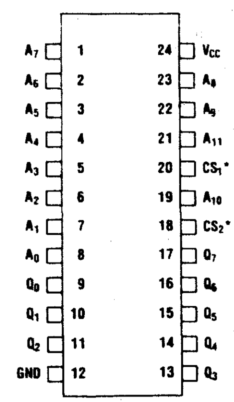


*PROGRAMMABLE CHIP SELECTS
MAY BE SPECIFIED AS ACTIVE LOW ($\overline{CS}$) OR ACTIVE HIGH (CS) OR NO CONNECT (NC)

Logic Symbol



Pin Configuration



Pin Names

A_0—A_{11}	Address Inputs
Q_0—Q_7	Data Outputs
CS_1—CS_2	Chip Select Inputs
V_{CC}	+5V Power Supply

AMI®

A Subsidiary of Gould Inc.

65,536 BIT (8192x8) STATIC NMOS ROM

Features

- ☐ Fast Access Time: S68A364-350ns Maximum
  S58B364-250ns Maximum
- ☐ Low Standby Power: 85mW Maximum
- ☐ Late Mask Programmable
- ☐ Fully Static Operation
- ☐ Single +5V ±10% Power Supply
- ☐ Directly TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Programmable Chip Enable

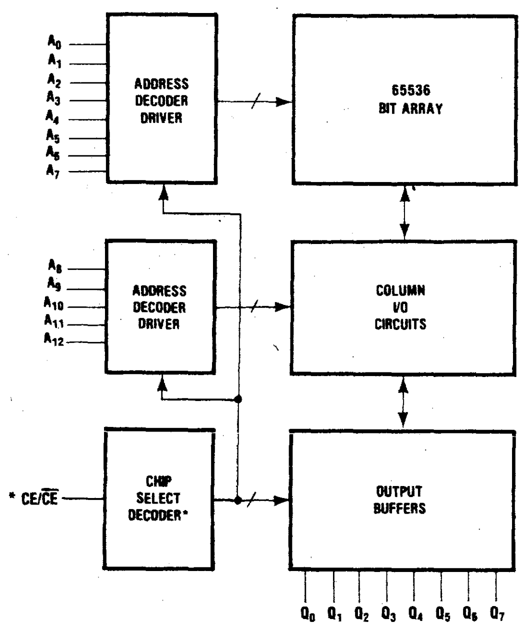
General Description

The AMI S68364 family are 65,536 bit static mask programmable NMOS ROMs organized as 8192 words by 8 bits. The devices are fully TTL compatible on all inputs and outputs and have a single +5V power supply. The three-state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The devices are fully static, requiring no clocks for operation. The chip enable is mask programmable, the active level being specified by the user. When not enabled, power supply current is reduced to a maximum of 15mA.

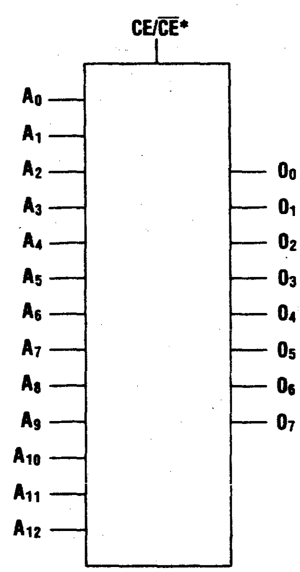
The S68364 family of devices are fabricated using AMI's NMOS ROM technology. This permits the mask programmable ROMs.

Block Diagram

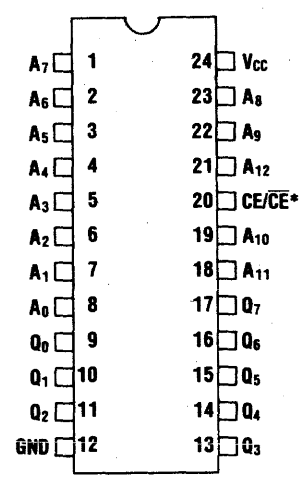


*USER DEFINED MASK PROGRAMMABLE CHIP ENABLE—MAY BE DEFINED AS ACTIVE HIGH, ACTIVE LOW, OR NO CONNECT.

Logic Symbol



Pin Configuration



Pin Names

A_0—A_{12}	Address Inputs
Q_0—Q_7	Data Outputs
CE/$\overline{CE}$	Programmable Chip Enable
V_{CC}	+5V Power Supply

American Microsystems, Inc.

MEMORY

65,536 BIT (8192x8) STATIC NMOS ROM

Features

- ☐ Fast Access Time: S2364A 350ns Maximum
  S2364B 250ns Maximum
- ☐ Low Standby Power: 85mW Maximum
- ☐ Fully Static Operation
- ☐ Single +5V ±10% Power Supply
- ☐ Directly TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Three Programmable Chip Enables/Selects
- ☐ EPROM Pin Compatible (2764)
- ☐ Late Mask Programmable

General Description

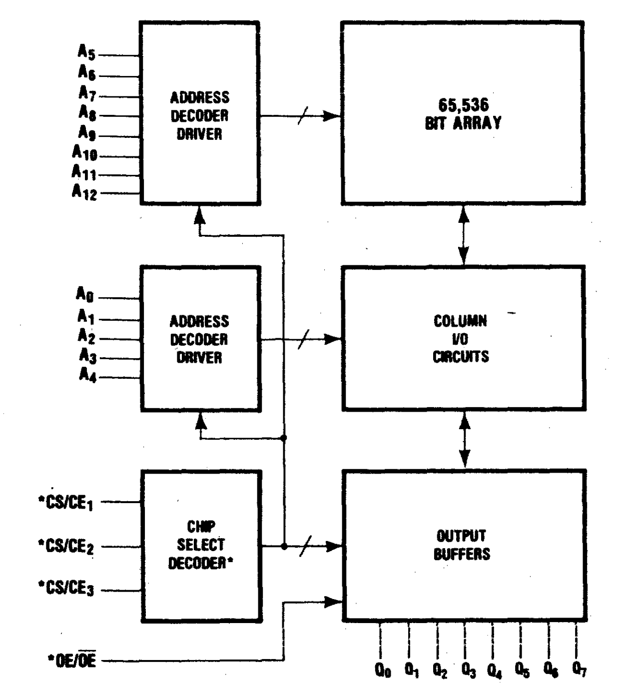
The AMI S2364 is a 65,536 bit static mask programmable NMOS ROM organized as 8192 words by 8 bits.

The device is fully TTL compatible on all inputs and outputs and has a single +5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S2364 is pin compatible with the 2764 UV EPROM making system development much easier and more cost effective. It is fully static, requiring no clocks for operation. The three chip enables are mask programmable; the active level for each being specified by the user. When not enabled, power supply current is reduced to a 10mA maximum.

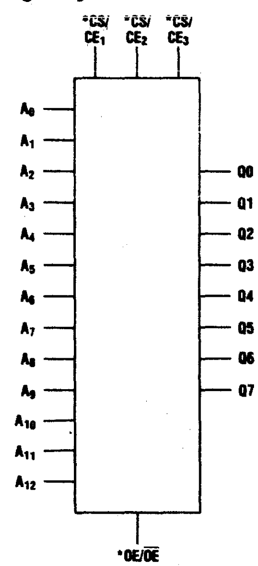
The S2364 is fabricated using AMI's N-Channel MOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

Block Diagram

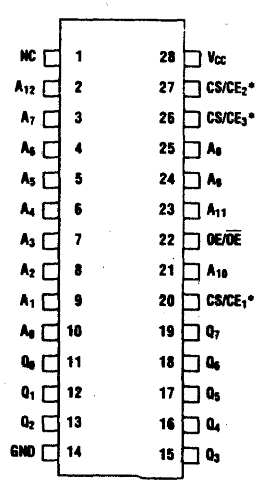


*CONTROL FUNCTION AND ACTIVE LEVEL IS USER DEFINED

Logic Symbol



Pin Configuration



Pin Names

A_0—A_{12}	Address Inputs
Q_0—Q_7	Data Outputs
CS/CE_1-CS/CE_3	Chip Selects/Enables
OE/$\overline{OE}$	Output Enable
V_{CC};GND;NC	5V;Ground;No Connect

AMI®

A Subsidiary of Gould Inc.

S23128A/S23128B

131,072 BIT (16384x8) STATIC NMOS ROM

Features

- ☐ Fast Access Time: S23128A-350ns Maximum
  S23128B-250ns Maximum
- ☐ Low Standby Power: 110mW Max.
- ☐ Fully Static Operation
- ☐ Single +5V ± 10% Power Supply
- ☐ Directly TTL Compatible Outputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Two Programmable Chip Enables/Selects
- ☐ EPROM Pin Compatible (27128)
- ☐ Late Mask Programmable
- ☐ Programmable Output/Chip Enable

General Description

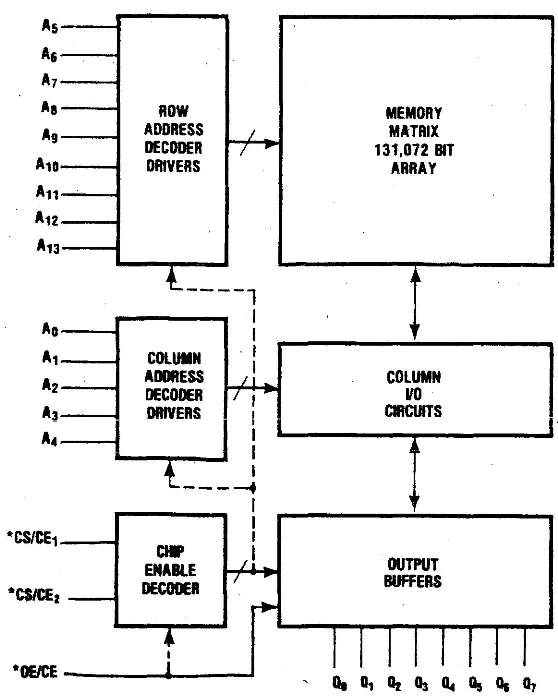
The AMI S23128 is a 131,072 bit static mask programmable NMOS ROM organized as 16,384 words by 8 bits.

The device is fully TTL compatible on all inputs and outputs and has a single +5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S23128 is pin compatible with the 27128 EPROM making system development easier and more cost effective. The fully static S23128 requires no clocks for operation. The three control pins are mask programmable with the active level and function being specified by the user. The pins can also be programmed as no connections. If CE functions are selected, automatic powerdown is available. The power supply current is reduced to 12mA when the chip is disabled.

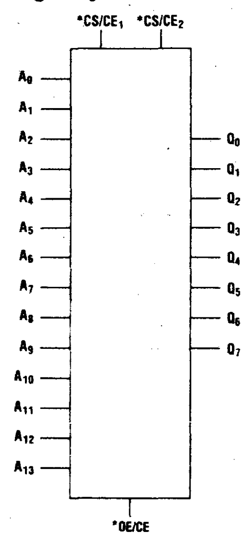
The S23128 is fabricated using AMI's NMOS technology. This permits the manufacture of high density, high performance ROMs.

Block Diagram

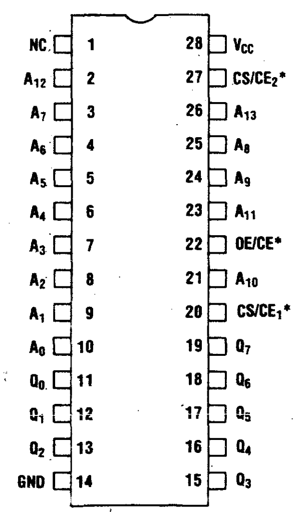


* THE USER DECIDES BETWEEN A CS OR CE FUNCTION AND THEN DEFINES THE ACTIVE LEVEL FOR CS/CE AND OE/CE.

Logic Symbol



Pin Configuration



Pin Names

A_0-A_{13}	Address Inputs
Q_0-Q_7	Data Outputs
CS/CE_1-CS/CE_2	Chip Selects/Enables
OE/CE	Output Enable/Chip Enable
V_{CC};GND;NC	5V;Ground; No Connect

American Microsystems, Inc.

MEMORY

262,144 BIT (32,768x8) STATIC NMOS ROM

Features

- ☐ Fast Access Time:
  - S23256B: 250ns Maximum
  - S23256C: 150ns Maximum
- ☐ Low Power Dissipation
  - Active Current: 40mA Maximum
  - Standby Current: 10mA Maximum
- ☐ Fully Static Operation
- ☐ Two User-Defined and Programmable Control Lines: CE/CS, OE/CE
- ☐ EPROM Pin Compatible
- ☐ Late Mask Programmable
- ☐ Three-State TTL Compatible Outputs

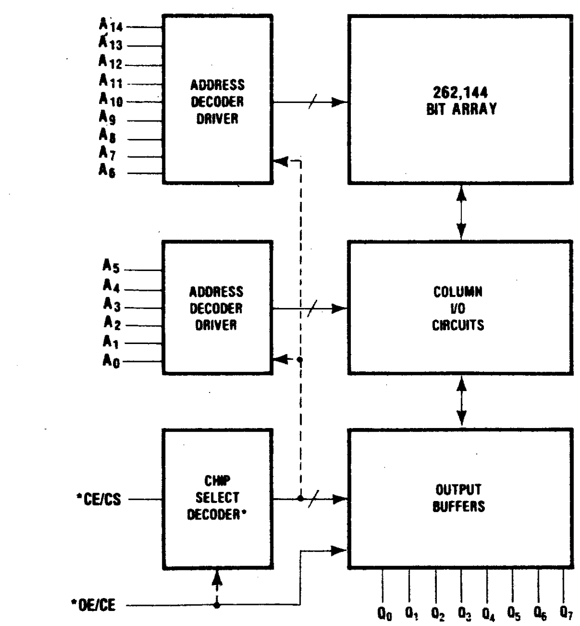
General Description

The AMI S23256 is a 262,144 bit static mask programmable NMOS ROM organized as 32,768 words by 8 bits. The devices are fully TTL compatible on all inputs and outputs and operate from a single +5V ±10% power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S23256 is pin compatible with the 27128 UV EPROM making system development much easier and more cost effective. It is fully static, requiring no clocks for operation.

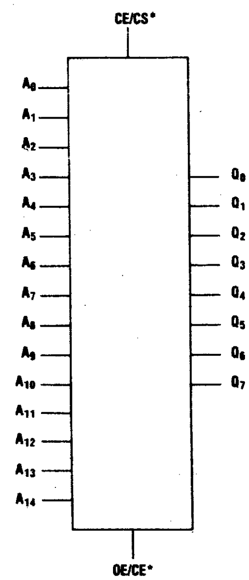
The S23256 is fabricated using AMI's N-Channel MOS ROM technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

Block Diagram

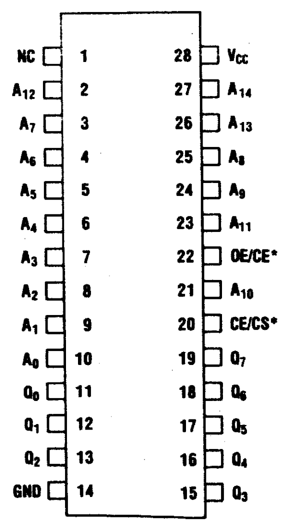


*THE USER DECIDES BETWEEN A CE OR CS AND OE OR CE FUNCTION AND THEN DEFINES THE ACTIVE LEVEL

Logic Symbol



Pin Configuration



Pin Names

$A_0 - A_{14}$	Address Inputs
$Q_0 - Q_7$	Data Outputs
CE/CS	Chip Enable/Chip Select
OE/CE	Output/Chip Enable
V_{CC};GND;NC	5V;Ground;No Connect

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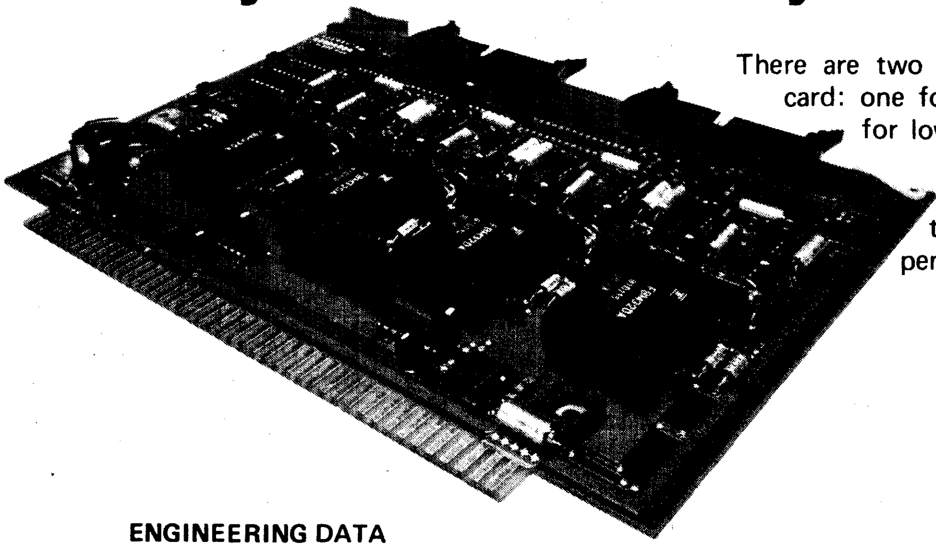
32K byte Bubble Memory Card

FUJITSU



There are two kinds of Fujitsu bubble memory card: one for high-speed file memory and one for low-speed file memory.

Both can be connected to the 8-bit micro-processor buss and the capacity is easily increased depending on a system.

ENGINEERING DATA

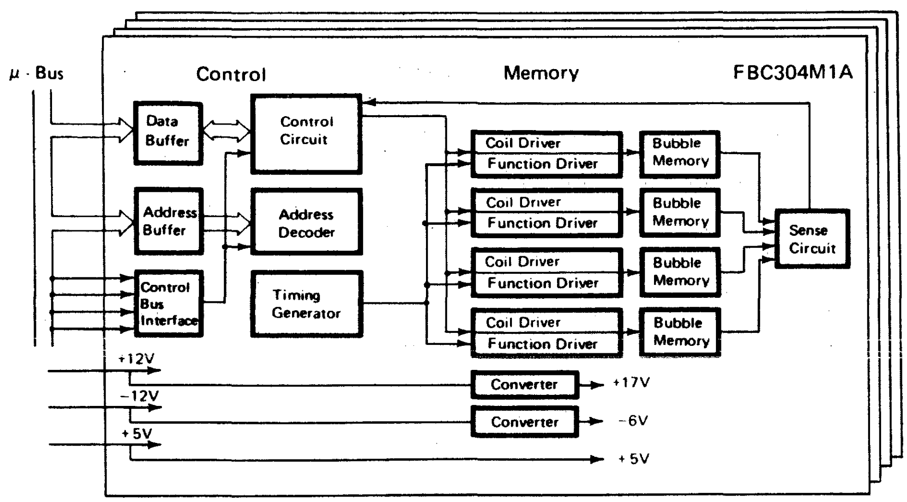
	FBC304M1A	FBC304D2A
Devices	FBM31DB	FBM32DA
Number of Devices	4	4
Organization	Serial loop	Major/Minor loop
Capacity	296,128 bits	324,024 bits
Average Access Time	370 ms	4.5 ms
Drive Frequency	100KHz	100KHz
Data Rate	100K bits/sec.	200K bits/sec.
Interface	TTL Compatible	TTL Compatible
Power Consumption Operating Stand-by	 9 W 6 W	 11 W 2.5 W
Power Requirement *	+12 V (± 5 %) 0.3A Max. −12 V (± 5 %) 0.2A Max. + 5 V (± 5 %) 1.6A Max.	+12 V (± 5 %) 1.0A Max. −12 V (± 5 %) 0.2A Max. + 5 V (± 5 %) 0.7A Max.
Temperature Range Operating Non-volatile Storage	 0°C to +50°C −40°C to +85°C	 0°C to +50°C −40°C to +85°C
Card Dimension	230 x 160 mm²	230 x 160 mm²

* Sequencial power-on and power-off are unnecessary.

Fijutsu 32K byte Bubble Memory Card

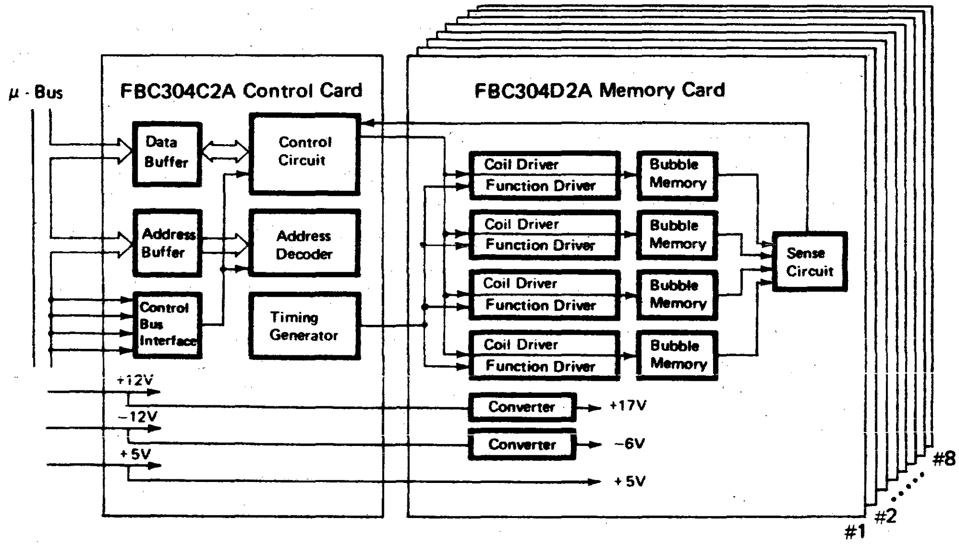
FBC304M1A is a 32K byte bubble memory card containing four 74K bit serial loop organized Bubble Memory Devices FBM31DB.

The timing and control circuits, in addition to coil drivers, function drivers, sense amplifier, etc., are also mounted on the same card, which can be directly connected to the 8-bit micro-processor as a low-speed data file and program memory.



Fujitsu America, Inc., 918 Sherwood Drive, Lake Bluff, Illinois 60044

FBC304D2A is a 32K byte high-speed bubble memory card with a TTL interface, containing four 83K bit major/minor loop organized Bubble Memory Devices FBM32DA with peripheral circuits. As a high-speed random access file memory this card can be connected to the 8 bit microprocessor buss via a control card FBC304C2A and the number of cards can be increased up to 256K bytes (8 cards), according to a system scale.

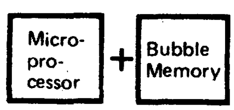


EXPECTED BUBBLE MEMORY APPLICATIONS

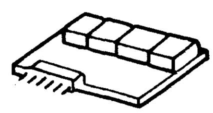
System Memory Capacity (Byte)	10K	100K	1M	10M
Chip Capacity (bit)	64K ~ 100K	256K ~ 1M	> 1 M	

Bubble Memory Products

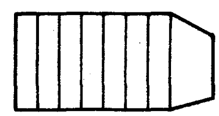
Program Memory



Mini-File Memory

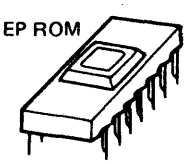


File Memory

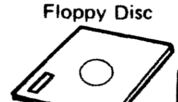


Competing Technology (Application Area)

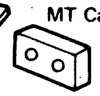
EP ROM



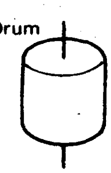
Floppy Disc



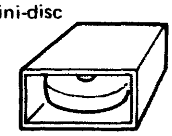
MT Cassette



Drum



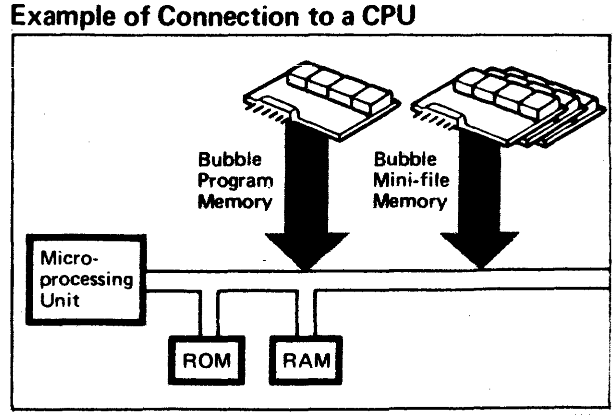
Mini-disc



Applications

- File memory for micro-computer and mini-computer
- Replacement for disc, drum and tape devices
- Program loaders for testing equipment and numerical control systems

Example of Connection to a CPU



Fujitsu America

MEMORY

Fujitsu America, Inc., 918 Sherwood Drive, Lake Bluff, Illinois 60044

64K bit Bubble Memory Device

FUJITSU

FBM31DB and FBM32DA are 18-pin DIP packages that contain a 64K bit serial loop chip and a 64K bit major/minor loop chip, respectively, orthogonal coils for rotating magnetic field, and a magnet for biasing which makes the bubbles stable to keep data.

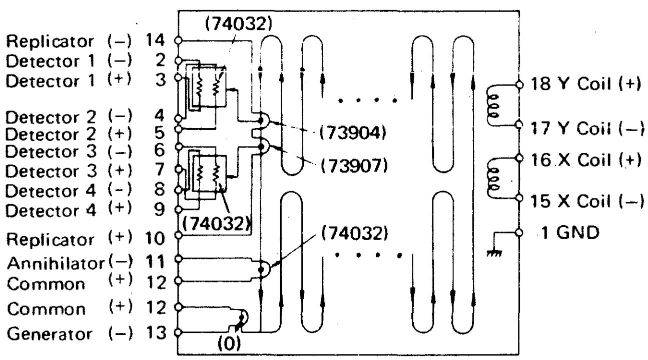
These bubble memory devices serve as the heart of the Fujitsu bubble memory card mounted on a printed circuit board.

ENGINEERING DATA

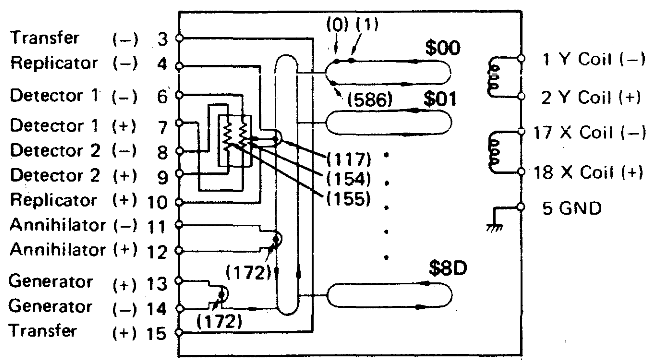
	FBM31DB	FBM32DA
Capacity:	74,032 bits	83,354 bits (total) 81,006 bits (effective)
Organization:	Serial loop	Major/Minor loop
Drive Frequency:	100KHz	100KHz
Transfer Rate:	100K bits/sec.	50K bits/sec.
Average Access Time:	370 ms	4.5 ms
Power Consumption:	500 mW	500 mW
Temperature Range Operating: Non-volatile Storage:	 0°C to + 55°C −40°C to + 85°C	 0°C to + 55°C −40°C to + 85°C
External Magnetic Field Operating: Non-Volatile Storage:	 50 Oe Max. 100 Oe Max.	 50 Oe Max. 100 Oe Max.
Physical Structure:	18 pin DIP	18 pin DIP
Dimensions:	27.94 x 31 x 10 mm^3	27.94 x 31 x 10 mm^3
Weight	30 g	30 g

CIRCUIT DIAGRAM

- FBM31DB **(Serial loop)**



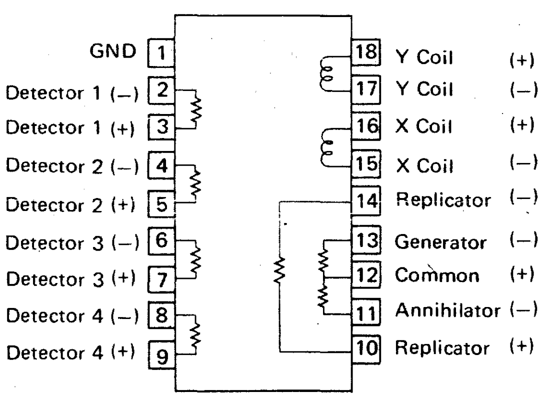
- FBM32DA **(Major/Minor loop)**



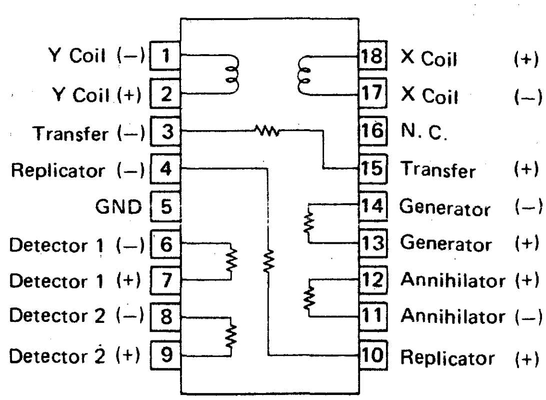
* Loop numbers (00 through 8D) are designated by hexadecimal code.

PIN ASSIGNMENT

- FBM31DB **(Serial loop)**



- FBM32DA **(Major/Minor loop)**



Fujitsu America, Inc., 918 Sherwood Drive, Lake Bluff, Illinois 60044

256K bit Bubble Memory Device

FUJITSU

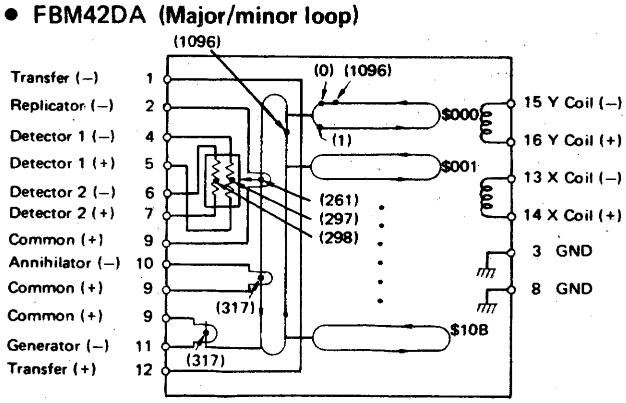
The FBM42DA is a major/minor bubble memory device in a 16 DIP package containing a 256K bit chip; the FBM43DA is a block replicator transfer bubble memory device in a 20 pin DIP package containing a 256K bit chip. Both devices are mountable on a printed circuit board and have orthogonal coils for rotating magnetic field. They also incorporate magnets for biasing, thereby providing the bubbles with stability to retain data.

ENGINEERING DATA

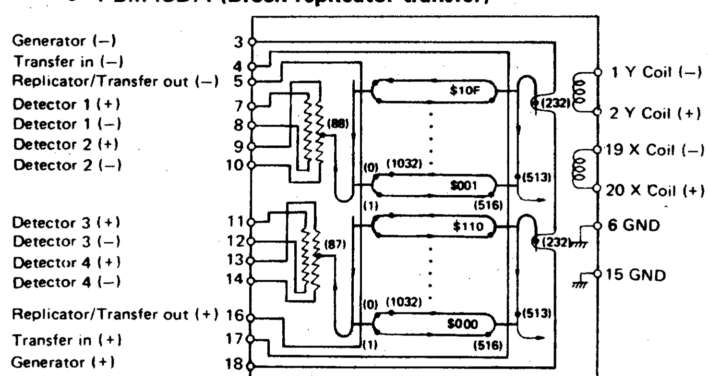
	FBM42DA	FBM43DA
Capacity	283,026 bits (effective) 1,097 bits X 258 loops	273,745 bits (effective) 1,033 bits X 265 loops
Organization	Major/minor loop	Major/minor loop (Block replicator transfer system)
Drive Frequency	100KHz	100KHz
Transfer Rate	50K bits/sec	100K bits/sec
Average Access Time	8.5 ms	6.0 ms
Power Consumption	670 mW	670 mW
Temperature Range Operating Non-volatile Storage	 0°C to +55°C −40°C to +85°C	 0°C to +55°C −40°C to +85°C
External Magnetic field	50 Oe Max.	50 Oe Max.
Physical Structure	16 pin DIP	20 pin DIP
Dimensions	27.94 x 31 x 11 mm^3	27.94 x 31 x 11 mm^3
Weight	30 g	30 g

CIRCUIT DIAGRAM

- FBM42DA (Major/minor loop)

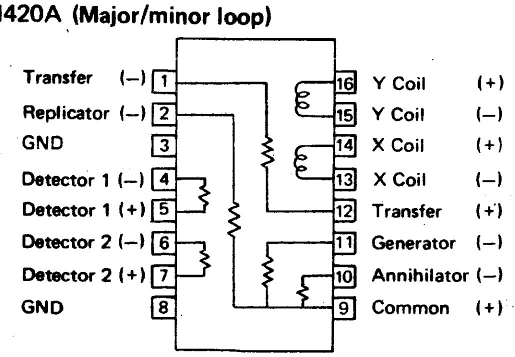


- FBM43DA (Block replicator transfer)

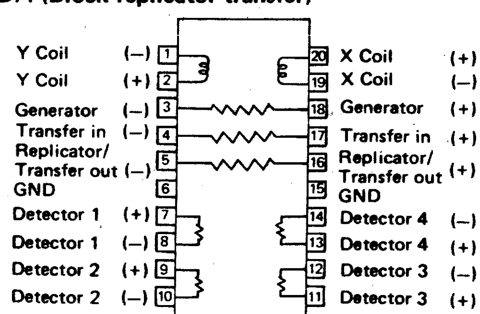


PIN ASSIGNMENT

- FBM420A (Major/minor loop)



- FBM43DA (Block replicator transfer)



*The $ mark prefixed hexadecimal codes in the circuit diagrams indicate minor loop numbers.

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HARRIS

HM-7602/03

32 x 8 PROM

HM-7602 — Open Collector Outputs
HM-7603 — "Three State" Outputs

Description

The HM-7602/03 is a fully decoded high speed Schottky TTL 256/Bit Field Programmable ROM in a 32 word by 8 bit/word format with open collector (HM-7602) or "Three State" (HM-7603) outputs. These PROMs are available in a 16 pin D.I.P. (ceramic or power plastic).

All bits are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any one bit position.

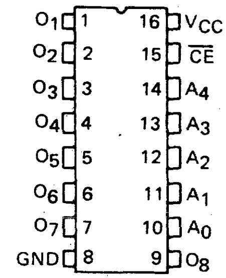
Nickel-chromium fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7602/03 contains test rows which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows are blown prior to shipment.

There is one chip enable input on the HM-7602/03. $\overline{CE}$ low enables the chip.

Pinout

TOP VIEW – DIP



PIN NAMES

$A_0 - A_4$	Address Inputs
$O_1 - O_8$	Data Outputs
$\overline{CE}$	Chip Enable Input

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7602/03-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7602/03-2/-8 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -250	µA µA	V_{IH} = VCC Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	VCC = VCC Min VCC = VCC Max.
V_{OH} V_{OL}	Output Voltage "1" "0"	2.4* –	3.2* 0.35	– 0.45	V V	I_{OH} = -2.0mA, VCC = VCC Min. I_{OL} = +16mA, VCC = VCC Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+100 -100	µA µA	V_{OH}, VCC = VCC Max. V_{OL} = 0.3V, VCC = VCC Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	VCC = VCC Max., V_{OUT} = 0.0V One Output Only for a Max. of 1 Second.
I_{CC}	Power Supply Current	–	90	130	mA	VCC = VCC Max. All Inputs Grounded

NOTE: Positive current defined as into device terminals
* "Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

Typical measurements are at T_A = +25°C, V_{CC} = +5V

		HM-7602/03-5 5V ±5% 0°C to +75°C		HM-7602/03-2/-8 5V ±10% -55°C to +125°C		
SYMBOL	PARAMETER	TYPICAL	MAXIMUM*	TYPICAL	MAXIMUM*	UNITS
T_{AA}	Address Access Time	30	50	–	60	ns
T_{EA}	Chip Enable Access Time	20	35	–	50	ns

*A.C. limits guaranteed for worst case N^2 sequencing with maximum test frequency of 5MHz.

Harris Semiconductor

MEMORY

HARRIS

HM-7610/11

HIGH SPEED 256 x 4 PROM

HM-7610 - Open Collector Outputs
HM-7611 - "Three State" Outputs

Description

The HM-7610/11 are fully decoded high speed Schottky TTL 1024 bit Field Programmable ROM's in a 256 word by 4 bit/word format with open collector (HM-7610) or "three state" (HM-7611) outputs. The PROMs are available in 16 pin D.I.P. (ceramic or power plastic).

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

The HM-7610/11 contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

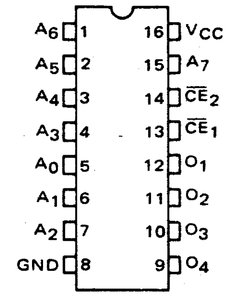
This PROM is intended for use in state of the art high speed logic systems.

Nickel-chromium fuse technology is used on these and all other Harris Bipolar PROMs.

There are two chip enable inputs on the HM-7610/11 where $\overline{CE}_1$ and $\overline{CE}_2$ low enables the chip.

Pinouts

TOP VIEW—DIP



PIN NAMES

$A_0 - A_7$ Address Inputs
$O_1 - O_4$ Data Outputs
$\overline{CE}_1, \overline{CE}_2$ Chip Enable Inputs

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7610/11-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7610/11-2/-8 (V_{CC} = 5.0V ±10%, T_A = –55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– –	+40 -100	μA μA	V_{IH} = VCC Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	VCC = VCC Min. VCC = VCC Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4* –	3.2* 0.35	– 0.50	V V	I_{OH} = -2.0mA, VCC = VCC Min. I_{OL} = +16mA, VCC = VCC Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40*	μA μA	VOH, VCC = VCC Max. VOL = 0.3V, VCC = VCC Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current *	-15*	–	-100*	mA	V_{CC} = V_{CC} Max. V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	90	110	mA	VCC = VCC Max. All Inputs Grounded

NOTE: Positive current defined as into device terminals.
* "Three-State" only.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

Typical Measurements are at T_A = 25°C, V_{CC} = +5V

		HM-7610/11-5 5V ±5% 0°C to +75°C						HM-7610/11-2/-8 5V ±10% –55°C to +125°C						
		"B"		"A"		STD		"B"		"A"		STD		
SYMBOL	PARAMETER	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	UNITS
T_{AA}	Address Access Time	25	35	35	45	40	60	–	50	–	65	–	75	ns
T_{EA}	Chip Enable Access Time	–	25	–	25	–	25	–	30	–	30	–	30	ns
T_{DA}	Chip Disable Access Time	–	25	–	25	–	25	–	30	–	30	–	30	

A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

HARRIS

HM-7620/21

HIGH SPEED 512 x 4 PROM

HM-7620- Open Collector Outputs
HM-7621 - "Three State" Outputs

Description

The HM-7620/21 are fully decoded high speed Schottky TTL 2048 bit Field Programmable ROM's in a 512 word by 4 bit/word format with open collector (HM-7620) or "three state" (HM-7621) outputs. These PROMs are available in 16 pin D.I.P. (ceramic or power plastic).

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

The HM-7620/21 contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A. C. performance. The fuses in these test rows and columns are blown prior to shipment.

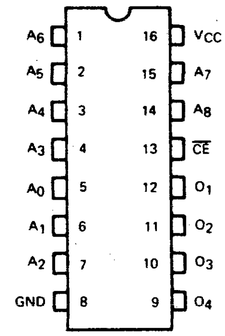
This PROM is intended for use in state of the art high speed logic systems.

Nickel-chromium fuse technology is used on these and all other Harris Bipolar PROMs.

There is a single chip enable input on the HM-7620/21 where $\overline{CE}$ low enables the chip.

Pinout

TOP VIEW - DIP



PIN NAMES

$A_0 - A_8$	Address Inputs
$\overline{CE}$	Chip Enable Input
$O_1 - O_4$	Data Outputs

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7620/21-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7620/21-2/-8 (V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/enable "1" Input Current "0"	– –	– –	+40 -100	μA μA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	– –	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4* –	3.2* 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40 *	μA μA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15 *	–	-100*	mA	V_{CC} = V_{CC} Max. V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	90	120	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

NOTE: Positive current defined as into device terminals.
* "Three-State" only.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

Typical Measurements are at T_A = 25°C, V_{CC} = +5V

		HM-7620/21 - 5 5V ±5% 0°C to +75°C						HM-7620/21-2/8 5V ±10% −55°C to +125°C						
		"B"		"A"		STD		"B"		"A"		STD		
SYMBOL	PARAMETER	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	UNITS
T_{AA}	Address Access Time	30	40	40	50	50	70	–	55	–	70	–	85	ns
T_{EA}	Chip Enable Access Time	–	25	–	25	–	25	–	30	–	30	–	30	ns
T_{DA}	Chip Disable Access Time	–	25	–	25	–	25	–	30	–	30	–	30	ns

A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

HARRIS

HM-7640/41

HIGH SPEED 512 x 8 PROM

HM-7640 - Open Collector Outputs
HM-7641 - "Three State" Outputs

Description

The HM-7640/41 are fully decoded high speed Schottky TTL 4096 bit Field Programmable ROMs in a 512 word by 8 bit/word format with open collector (HM-7640) or "three-state" (HM-7641) outputs. These PROMs are available in a 24 pin DIP (ceramic or power plastic).

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

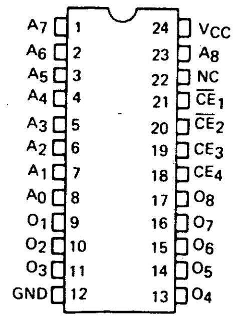
Nickel-chromium fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7640/41 contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There are four chip enable inputs on the HM-7640/41 where $\overline{CE_1}$ and $\overline{CE_2}$ low and CE_3 and CE_4 high enables the chip.

Pinouts

TOP VIEW – DIP



PIN NAMES

A_0 - A_8	Address Inputs
O_1 - O_8	Data Outputs
$\overline{CE_1}$, $\overline{CE_2}$, CE_3, CE_4	Chip Enable Inputs

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7640/41-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7640/41-2/-8 (V_{CC} - 5.0V ±10%, T_A = −55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– –	−40 -100	μA μA	V_{IH} = VCC Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	– –	– 0.8	V V	VCC = VCC Min. VCC = VCC Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4* –	3.2* 0.35	– 0.50/0.45	V V	I_{OH} = -2.0mA, VCC = VCC Min. I_{OL} = +16mA, VCC = VCC Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40 *	μA μA	VOH, VCC = VCC Max. VOL = 0.3V, VCC = VCC Max.
VCL	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
IOS	Output Short Circuit Current	-15*	–	-100*	mA	VCC = VCC Max. V_{OUT} = 0.0V One Output at a Time for Max. of 1 Second
ICC	Power Supply Current	–	125	170	mA	VCC = VCC Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
* "Three-State" only.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

Typical Measurements are at T_A = 25°C, V_{CC} = +5V

		HM-7640/41-5 5V ±5% 0°C to +75°C				HM-7640/41-2/-8 5V ±10% −55°C to +125°C				
		"A"		STD		"A"		STD		
SYMBOL	PARAMETER	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	UNITS
T_{AA}	Address Access Time	35	45	50	70	–	60	–	85	ns
T_{EA}	Chip Enable Access Time	–	35	–	40	–	45	–	50	ns
T_{DA}	Chip Disable Access Time	–	35	–	40	–	45	–	50	ns

A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

Harris Semiconductor

MEMORY

HARRIS

HM-7649

HIGH SPEED 512 x 8 PROM

Description

The HM-7649 is a fully decoded high speed Schottky TTL 4096 bit Field Programmable ROM in a 512 word by 8 bit/word format with "Three State" outputs. This PROM is available in a 20 pin D.I.P. (ceramic or power plastic).

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

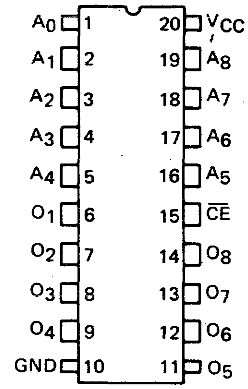
Nickel Chromium fuse technology is used on this and all other Harris Bipolar PROMs.

The pinout is identical to the 74S473 PROM.

The HM-7649 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametic and A. C. performance. The fuses in these test rows and columns are blown prior to shipment.

There is a chip enable input on the HM-7649 where $\overline{CE}$ low enables the device.

Pinout



TOP VIEW - D.I.P.

PIN NAMES

A_0-A_8	Address Inputs
O_1-O_8	Data Outputs
$\overline{CE}$	Chip Enable Input

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7649-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7649-2/8 (V_{CC} - 5.0V ±10%, T_A = −55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– –	+25 -100/-250	μA μA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	– –	– 0.80	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4 –	3.2 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40	μA μA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-20	–	-100	mA	V_{CC}=V_{CC} Max. V_{OUT}=0.0V, One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	120	170	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

NOTE: Multiple entries refer to parameter values for "A"/STD. Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

Typical Measurements are at T_A = 25°C, V_{CC} = +5V

		HM-7649-5 5V ±5% 0°C to +75°C				HM-7649-2/-8 5V ±10% -55°C to +125°C				
		"A"		STD		"A"		STD		
SYMBOL	PARAMETER	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	UNITS
T_{AA}	Address Access Time	35	45	40	60	–	60	–	80	ns
T_{EA}	Chip Enable Access Time	–	35	–	40	–	45	–	50	ns
T_{DA}	Chip Disable Access Time	–	35	–	40	–	45	–	50	ns

A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

HM-7642/43

HIGH SPEED 1K x 4 PROM

HM-7642 - Open Collector Outputs
HM-7643 - "Three State" Outputs

Description

The HM-7642/43 are fully decoded high speed Schottky TTL 4096 bit Field Programmable ROMs in a 1K word by 4 bit/word format with open collector (HM-7642) or "three state" (HM-7643) outputs. These PROM's are available in an 18 pin DIP (ceramic or power plastic).

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

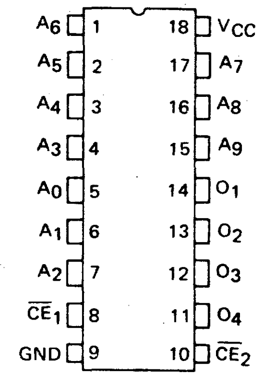
Nickel-chromium fuse technology is used on these and all other Harris Bipolar PROMs.

The HM-7642/43 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There are two chip enable inputs on the HM-7642/43. $\overline{CE}_1$ and $\overline{CE}_2$ low enables the chip.

Pinout

TOP VIEW—DIP



PIN NAMES

A_0 - A_9	ADDRESS INPUTS
O_1 - O_4	DATA OUTPUTS
$\overline{CE}_1$, $\overline{CE}_2$	CHIP ENABLE INPUTS

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7642/43-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7642/43-2/-8 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical Measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– –	-40 -100	μA μA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	– –	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4* –	3.2* 0.35	– 0.50/0.50/0.45	V V	I_{OH} = -2.0mA, V_{CC} = VCC Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40*	μA μA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{CC} = V_{CC} Max. V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	100	140	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
* "Three-State" only.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

Typical Measurements are at T_A = 25°C, V_{CC} = +5V

		HM-7642/43-5 5V ±5% 0°C to +75°C						HM-7642/43-2/-8 5V ±10% –55°C to +125°C						
		"B"		"A"		STD		"B"		"A"		STD		
SYMBOL	PARAMETER	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	UNITS
T_{AA}	Address Access Time	35	45	40	50	45	60	–	55	–	70	–	85	ns
T_{EA}	Chip Enable Access Time	–	25	–	25	–	25	–	30	–	30	–	30	ns
T_{DA}	Chip Disable Access Time	–	25	–	25	–	25	–	30	–	30	–	30	ns

A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

HARRIS

HM-7681

HIGH SPEED 1K x 8 PROM

Description

The HM-7681 is a fully decoded high speed Schottky TTL 8192 bit Field Programmable ROM in a 1K word by 8 bit/word format with "Three State" outputs. This PROM is available in a 24 pin D.I.P. (ceramic or power plastic).

All bits are manufactured storing a logic "1" (Positive Logic) and can be selectively programmed for a logical "0" in any one bit position.

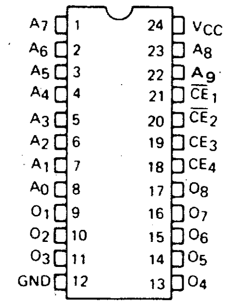
Nickel-chromium fuse technology is used on this and all other HARRIS Bipolar PROMs.

The HM-7681 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There are four chip enable inputs on the HM-7681. $\overline{CE}_1$, $\overline{CE}_2$ low, and CE_3, CE_4 high enables the chip.

Pinouts

TOP VIEW – DIP



PIN NAMES

A_0 - A_9	Address Inputs
O_1 - O_8	Data Outputs
$\overline{CE}_1$, $\overline{CE}_2$, CE_3, CE_4	Chip Enable Inputs

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7681-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7681-2/8 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/enable "1" Input Current "0"	– –	– –	+40 -100/-250	μA μA	V_{IH} = VCC Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	– –	– 0.8	V V	VCC = VCC Min. VCC = VCC Max.
VOH VOL	Output "1" Voltage "0"	2.4 –	3.2 0.35	– 0.50	V V	IOH = -2.0mA, VCC = VCC Min. IOL = +16mA, VCC = VCC Min.
IOHE IOLE	Output Disable "1" Current "0"	– –	– –	+40 -40	μA μA	VOH, VCC = VCC Max. VOL = 0.3V, VCC = VCC Max.
VCL	Input Clamp Voltage	–	–	-1.2	V	IIN = -18mA
IOS	Output Short Circuit Current	-15	–	-100	mA	VCC = VCC Max., VOUT = 0.0V One Output Only for a Max. of 1 Second
ICC	Power Supply Current	–	130	170	mA	VCC = VCC Max. All Inputs Grounded

NOTE: Multiple entries refer to parameter values for "A"/STD. Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

Typical Measurements are at T_A=25°C, V_{CC}=+5V

		HM-7681-5 5V ±5% 0°C to +75°C				HM-7681-2/8 5V ±10% −55°C to +125°C				
		"A"		STD		"A"		STD		
SYMBOL	PARAMETER	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	UNITS
T_{AA}	Address Access Time	40	50	50	70	–	60	–	90	ns
T_{EA}	Chip Enable Access Time	–	35	–	40	–	40	–	50	ns
T_{DA}	Chip Disable Access Time	–	35	–	40	–	40	–	50	ns

A.C. Limits guaranteed for worst case N^2 sequencing with maximum test frequency of 5MHz.

Harris Semiconductor

MEMORY

HARRIS

HM-7685

HIGH SPEED 2K x 4 PROM

Description

The HM-7685 is a fully decoded high speed Schottky TTL 8192- bit Field Programmable ROM in a 2K word by a 4 bit/word format with "Three State" outputs. This PROM is available in an 18 pin DIP (ceramic or power plastic).

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

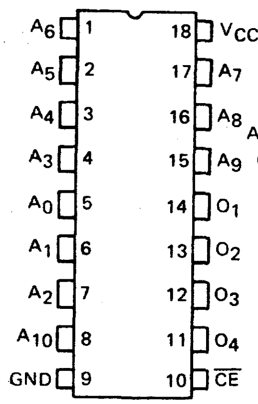
Nickel-chromium fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7685 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A. C. performance. The fuses in these test rows and columns are blown prior to shipment.

There is a chip enable on the HM-7685. $\overline{CE}$ low enables the chip.

Pinouts

TOP VIEW - DIP



PIN NAMES

$A_0 - A_{10}$	Address Inputs
$O_1 - O_4$	Data Outputs
$\overline{CE}$	Chip Enable Input

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7685-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7685-2/-8 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– –	+40 -100/-250	μA μA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	– –	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4 –	3.2 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40	μA μA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	–	-100	mA	V_{CC}=V_{CC} Max. V_{OUT}=0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	120	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Multiple entries refer to parameter values of "A"/STD. Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

Typical Measurements are at T_A=25°C, V_{CC}=+5V

		HM-7685-5 5V ±5% 0°C to +75°C				HM-7685-2/-8 5V ±10% -55°C to +125°C				
		"A"		STD		"A"		STD		
SYMBOL	PARAMETER	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	UNITS
T_{AA}	Address Access Time	40	50	50	70	–	60	–	90	ns
T_{EA}	Chip Enable Access Time	–	30	–	40	–	35	–	50	ns
T_{DA}	Chip Disable Access Time	–	30	–	40	–	35	–	50	ns

A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

HARRIS

HM-76161

HIGH SPEED 2K x 8 PROM

Description

The HM-76161 is a fully decoded high speed Schottky TTL 16,384 bit Field Programmable ROM in a 2K word by 8 bit/word format with "Three State" outputs. This PROM is available in a 24 pin DIP (ceramic or power plastic).

All bits are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any bit position.

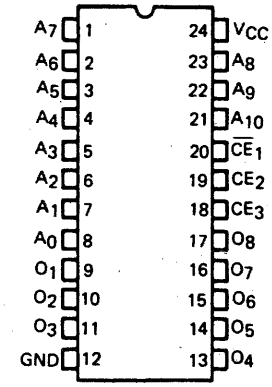
The nickel-chromium fuse technology used is the same as all other Harris Bipolar PROMs and the JAN approved MIL-M-38510 PROMs.

The HM-76161 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There are three chip enable inputs on the HM-76161. $\overline{CE}_1$ low, CE_2 high, and CE_3 high enables the device.

Pinout

TOP VIEW - D I P



PIN NAMES

$A_0 - A_{10}$	Address Inputs
$O_1 - O_8$	Data Outputs
$\overline{CE}_1, CE_2, CE_3$	Chip Enable Inputs

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-76161-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-76161-2/-8 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical Measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+40	μA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	–	-100	μA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	–	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	–	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4	3.2	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.50	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+40	μA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-40	μA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	–	-100	mA	V_{CC} = V_{CC} Max. V_{OUT} = 0.0V One Output at a Time for Max. of 1 Second
I_{CC}	Power Supply Current	–	130	180	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

Typical Measurements are at T_A=25°C, V_{CC}=+5V

		HM-76161-5 5V ±5% 0°C to +75°C				HM-76161-2/-8 5V ±10% -55°C to +125°C		
		"A"		STD		STD		
SYMBOL	PARAMETER	TYP	MAX	TYP	MAX	TYP	MAX	UNITS
T_{AA}	Address Access Time	40	50	45	60	–	80	ns
T_{EA}	Chip Enable Access Time	–	40	–	40	–	50	ns
T_{DA}	Chip Disable Access Time	–	40	–	40	–	50	ns

A.C. limits guaranteed for worst case N^2 sequencing with maximum test frequency of 5MHz

HARRIS

HM-76165

4K x 4 PROM

Description

The HM-76165 PROM is a fully decoded Schottky TTL 16,384 bit field programmable ROM in a 4K word by 4 bit/word format with "Three State" outputs. This PROM is available in a 20 pin 0.300 inch wide DIP.

All bits are manufactured storing a logical "1" and can be selectively programmed for a logical "0" in any bit position.

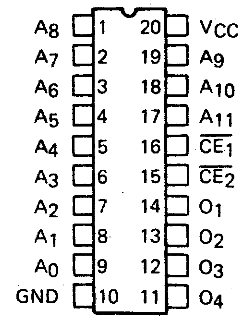
MIL-M-38510 qualified NiCr technology is used on the HM-76165 and all other HARRIS bipolar PROMs.

The HM-76165 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

The HM-76165 utilizes two chip enables where $\overline{CE_1}$ low and $\overline{CE_2}$ low enables the device.

Pinout

TOP VIEW – DIP



PIN NAMES

$A_0 - A_{11}$	Address Inputs
$O_1 - O_4$	Data Outputs
$\overline{CE_1}, \overline{CE_2}$	Chip Enable Inputs

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-76165-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-76165-2/-8 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical Measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+40	µA	V_{IH} = VCC Max.
I_{IL}	Input Current "0"	–	-50.0	-100	µA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	VCC = VCC Min.
V_{IL}	Voltage "0"	–	1.5	0.80	V	VCC = VCC Max.
VOH	Output "1"	2.4	3.2	–	V	IOH = -2.0mA, VCC = VCC Min.
VOL	Voltage "0"	–	0.35	0.50	V	IOL = +16mA, VCC = VCC Min.
IOHE(1)	Output Disable "1"	–	–	+40	µA	VOH, VCC = VCC Max.
IOLE	Current "0"	–	–	-40	µA	VOL = 0.3V, VCC = VCC Max.
VCL	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
IOS	Output Short Circuit Current	-15	–	-100	mA	VOUT = 0.0V, One Output at a Time for a Max. of 1 Second
ICC	Power Supply Current	–	120	170	mA	VCC = VCC Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
(1) I_{OHE} = +60µA for -2 and -8.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

Typical Measurements are at T_A = +125°C, V_{CC} = +5V

SYMBOL	PARAMETER	HM-76165-5 5V ±5% 0°C to +75°C TYPICAL	HM-76165-5 MAXIMUM	HM-76165-2/-8 5V ±10% -55°C to +125°C TYPICAL	HM-76165-2/-8 MAXIMUM	UNITS
T_{AA}	Address Access Time	45	60	50	80	ns
T_{EA}	Chip Enable Access Time	25	35	30	40	ns
T_{DA}	Chip Disable Access Time	25	35	30	40	ns

A.C. limits guaranteed for worst case N^2 sequencing with maximum test frequency of 5MHz.

HARRIS

HM-76321

4K x 8 PROM

Description

The HM-76321 is a fully decoded Schottky TTL 32,768 bit field programmable ROM in a 4K word by 8 bit/word format with "Three State" outputs. This PROM is available in a 24 pin DIP.

All bits are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any bit position.

MIL-M-38510 qualified NiCr technology is used on the HM-76321 and all other HARRIS Bipolar PROMs.

The HM-76321 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

The HM-76321 utilizes two chip enable controls, where $\overline{CE_1}$ low and CE_2 high enables the device.

Pinout

TOP VIEW – DIP

Signal	Pin	Pin	Signal
A_7	1	24	V_{CC}
A_6	2	23	A_8
A_5	3	22	A_9
A_4	4	21	A_{10}
A_3	5	20	$\overline{CE_1}$
A_2	6	19	A_{11}
A_1	7	18	CE_2
A_0	8	17	O_8
O_1	9	16	O_7
O_2	10	15	O_6
O_3	11	14	O_5
GND	12	13	O_4

PIN NAMES

A_0 - A_{11}	Address Inputs
O_1 - O_8	Data Outputs
$\overline{CE_1}$, CE_2	Chip Enable Inputs

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-76321-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-76321-2/-8 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical Measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -100	μA μA	V_{IH} = VCC Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = VCC Min. V_{CC} = VCC Max.
VOH VOL	Output "1" Voltage "0"	2.4 –	3.2 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = VCC Min. I_{OL} = +16mA, V_{CC} = VCC Min.
IOHE(1) IOLE	Output Disable "1" Current "0"	– –	– –	+40 -40	μA μA	VOH, V_{CC} = VCC Max. VOL = 0.3V, V_{CC} = VCC Max.
VCL	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
IOS	Output Short Circuit Current	-15	–	-100	mA	VOUT = 0.0V, One Output at a Time for a Max. of 1 Second
ICC	Power Supply Current	–	–	190	mA	V_{CC} = VCC Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
(1) I_{OHE} = +100μA for -2 and -8.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

Typical measurements are at T_A = +25°C, V_{CC} = +5V

		HM-76321-5 5V ±5% 0°C to +75°C		HM-76321-2/-8 5V ±10% -55°C to +125°C		
SYMBOL	PARAMETER	TYPICAL	MAXIMUM	TYPICAL	MAXIMUM	UNITS
T_{AA}	Address Access Time	45	65	–	85	ns
T_{EA}	Chip Enable Access Time	25	35	–	40	ns
T_{DA}	Chip Disable Access Time	25	35	–	40	ns

A.C. limits guaranteed for worst case N^2 sequencing with maximum test frequency of 5MHz.

HM-76641

8K x 8 PROM

Description

The HM-76641 is a fully decoded Schottky TTL 65,536 bit field programmable ROM in an 8K word by 8 bit/word format with "Three State" outputs. This PROM is available in a 24 pin DIP.

All bits are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any bit position.

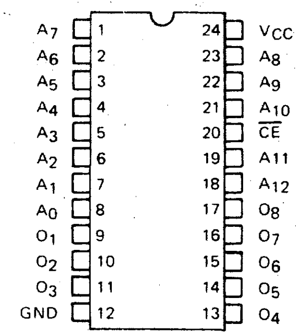
MIL-M-38510 qualified NiCr technology is used on the HM-76641 and all other HARRIS bipolar PROMs.

The HM-76641 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

The HM-76641 utilizes a single chip enable, $\overline{CE}$, which when low enables the device.

Pinout

TOP VIEW – DIP



PIN NAMES

A_0 - A_{12} Address Inputs
O_1 - O_8 Data Outputs
$\overline{CE}$ Chip Enable Inputs

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-76641-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-76641-2/-8 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical Measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+40	μA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	-50.0	-100	μA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4	3.2	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.50	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}(1)	Output Disable "1"	–	–	+40	μA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-40	μA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	–	-100	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	–	190	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
(1) I_{OHE} = +100μA for -2 and -8.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

Typical Measurements are at T_A = +25°C, V_{CC} = +5V

		HM-76641-5 5V ±5% 0°C to +75°C		HM-76641-2/-8 5V ±10% -55°C to +125°C		
SYMBOL	PARAMETER	TYPICAL	MAXIMUM	TYPICAL	MAXIMUM	UNITS
T_{AA}	Address Access Time	50	85	–	100	ns
T_{EA}	Chip Enable Access Time	30	40	–	45	ns
T_{DA}	Chip Disable Access Time	30	40	–	45	ns

A.C. limits guaranteed for worst case N^2 sequencing with maximum test frequency of 5MHz.

PROGRAMMING THE HM-76XXX PROMS

The HM-76XXX PROMs are manufactured with all bits storing a logical "1" (output high). Any desired bit can be programmed to a logical "0" (output low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in the table, or use any of the commercially available programmers which can meet these specifications.

PROGRAMMING SPECIFICATIONS

SYMBOL	PARAMETER	MINIMUM	RECOMMENDED OR TYPICAL	MAXIMUM	UNITS
V_{IH} V_{IL}	Address Input Voltage (1)	2.4 0.0	5.0 0.4	5.0 0.5	V V
V_{PH} (2) V_{PL} (3)	Programming/Verify Voltage to V_{CC}	12.0 4.5	12.0 4.5	12.5 5.5	V V
I_{ILP}	Programming Input Low Current at V_{PH}	—	-300	-600	μA
tr tf	Programming (V_{CC}) Voltage Rise and Fall Time	1.0 1.0	1.0 1.0	10 0 10.0	μs μs
td	Programming Delay	10	10	100.	μs
tp	Programming Pulse Width (4)	90	100	110	μs
P.D.C.	Programming Duty Cycle	—	50	90	%
VOPE VOPD	Output Voltage – Enable (5) Output Voltage – Disable (6)	10.5 4.5	10.5 5.0	11.0 5.5	V V
T_a	Ambient Temperature	—	25	75	°C

During programming the chip must be disabled for proper operation.

NOTES:
1. No inputs should be left open for V_{IH}.
2. V_{PH} source must be capable of supplying one ampere.
3. It is recommended that dual verification be made at V_{PL} min and V_{PL} max.
4. Note step 10 in programming procedure.
5. V_{OPE} source must be capable of supplying 10mA minimum.
6. Disable condition will be met with output open circuit.

PROGRAMMING PROCEDURE

1. Address the PROM with the binary address of the word to be programmed. Address inputs are TTL compatible. An open circuit should not be used to address the PROM.
2. Bring the $\overline{CE}_X$ input(s) high and the CE_X input(s) low to disable the device. The disabling of the device during programming is an essential step in correctly programming all HARRIS PROMs. The chip enables are TTL compatible. An open circuit should not used to disable the device.
3. Disable the programming circuitry by applying a voltage of V_{OPD} to the outputs of the PROM. Any output may be left open to achieve the disable.
4. Raise V_{CC} to V_{PH} with rise time less than or equal to t_r.
5. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact, which generates an output high. Programming a fuse will cause the output to go low.
6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.
7. Lower V_{CC} to 4.5 volts following a delay of t_d from last programming enable pulse applied to an output.
8. Enable the PROM for verification by applying V_{IL} to $\overline{CE}_X$ and V_{IH} to CE_X.
9. Repeat verification (step 8) at V_{CC} = 5.5 volts.
10. If any bit does not verify as programmed, repeat steps 2 through 9 until the bit has received a total of 1ms of programming time. Bits which do not program within 1ms are programming rejects. No further at empt to program these parts should be made.
11. Repeat steps 1 through 10 for all other bits to be programmed in the PROM.
12. Programming rejects returned to the factory must be accompanied by data giving address, desired data, and actual output data of the location in which a programming failure has occurred.

TYPICAL PROGRAMMING CIRCUIT

The circuit and timing diagrams shown in Figures 1 and 2 will establish the proper programming conditions for the output enable pulses. This allows the use of standard TTL parts for all logic inputs to the PROM. Note the gate which senses the output must withstand inputs up to 11.0 volts during programming.

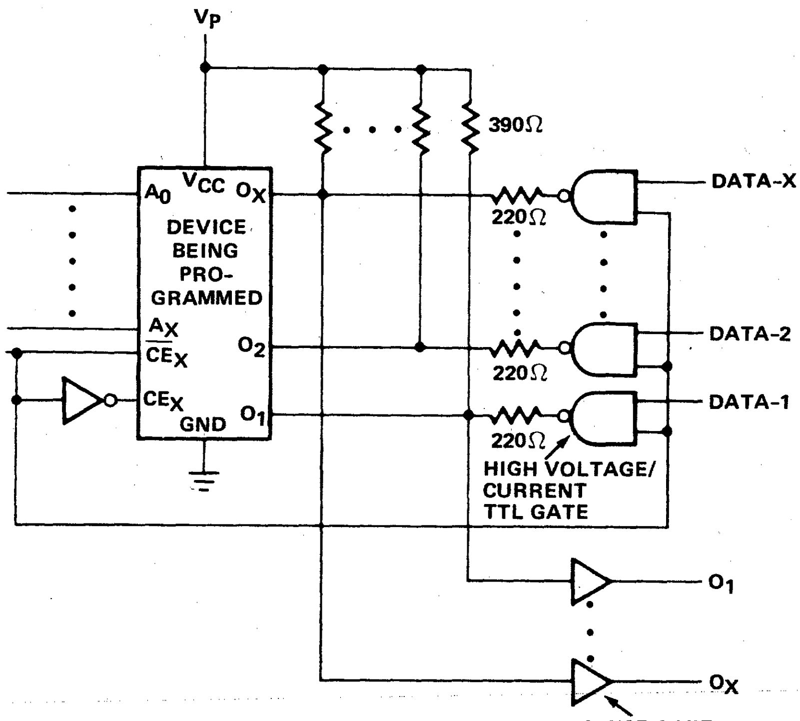


FIGURE 1

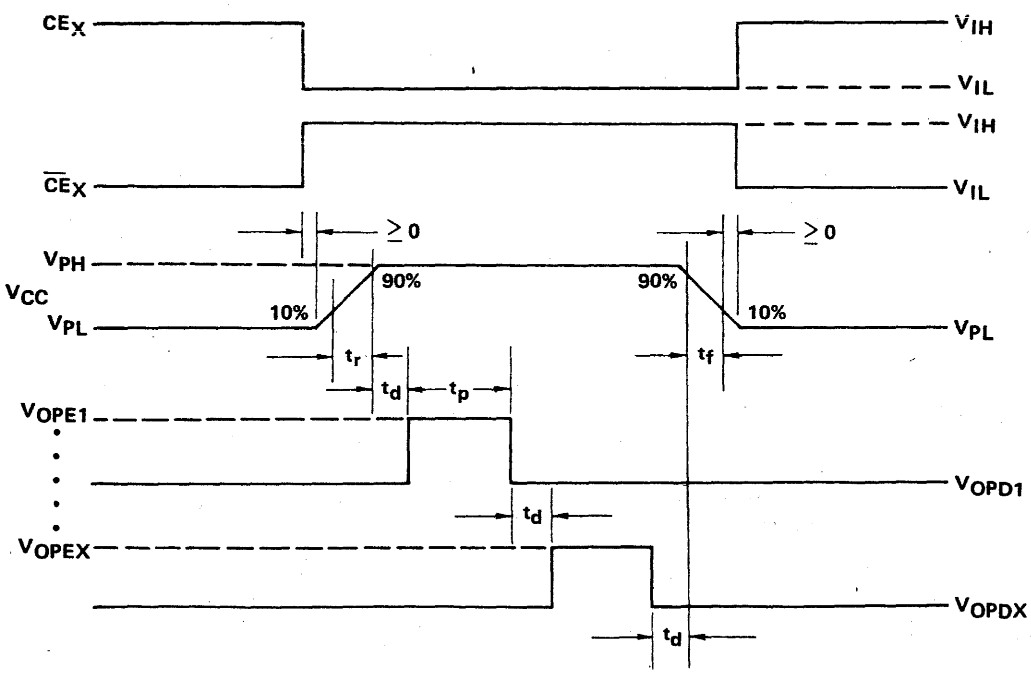


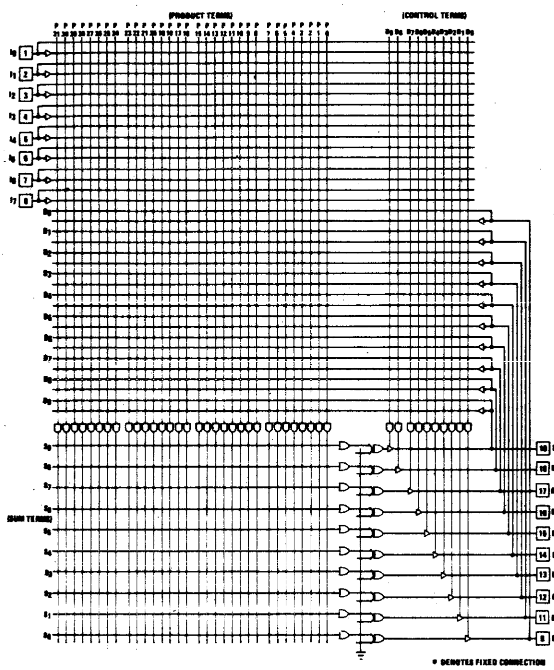
FIGURE 2

Waveforms Applied to the Device Pins During Programming

HPL-77153/82S153

HPL™ Harris Programmable Logic

Functional Diagram



D. C. ELECTRICAL CHARACTERISTICS (Operating)

HPL-77153/82S153-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HPL-77153/82S153-2/-8 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS	
I_{IH}	Input Current	"1"	–	+40	µA	V_{IH} = V_{CC} MAX	V_{CC} = V_{CC} MAX
I_{IL}	Dedicated Input	"0"	–	-100	µA	V_{IL} = 0.4V	
I_{BZH}	Input Current	"1"	–	+40	µA	V_{BH} = V_{CC} MAX	V_{CC} = V_{CC} MAX
I_{BZL}	Bidirectional Pin Current Hi-Z State	"0"	–	-100	µA	V_{BL} = 0.4V	
V_{IH}	Input Threshold	"1"	2.0	–	V	V_{CC} = V_{CC} MAX	
V_{IL}	Voltage	"0"	–	0.8	V	V_{CC} = V_{CC} MIN	
V_{OH}	High-Level Output Voltage		2.4	–	V	V_{CC} = V_{CC} MIN, V_{IL} = 0.8V, V_{IH} = 2.0V	I_{OH} = -2.0mA
V_{OL}	Low-Level Output Voltage		–	0.5	V		I_{OL} = +16mA
V_{CL}	Input Clamp Voltage		–	-1.2	V	I_{IN} = -18mA, V_{CC} = 0V	
I_{OS}	Output Short Circuit Current	C	-20	-70	mA	V_{CC} = 5.0V, V_{OUT} = 0V	
		M	-15	-85	mA	One output for MAX of One Sec.	
I_{CC}	Power Supply Current	C	–	155	mA	V_{CC} = V_{CC} MAX	
		M	–	165	mA		

C = Commercial (-5) M = Military (-2/-8)

A. C. SWITCHING CHARACTERISTICS (Operating)

SYMBOL			HPL-77153/82S153-5 5V ± 5% 0°C to +75°C		HPL-77153/82S153-2/-8 5V ± 10% -55°C to +125°C		
JEDEC STANDARD	OLD SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
TDVQH1	T_{PD}	Propagation Delay-Input or I/O to Active High Output	–	40	–	55	ns
TDVQL1	T_{PD}	Propagation Delay-Input or I/O to Active Low Output	–	40	–	55	ns
TDVQH2	T_{OE}	Enable Access Time to Active High Output	–	35	–	45	ns
TDVQL2	T_{OE}	Enable Access Time to Active Low Output	–	35	–	45	ns
TDVQZ1	T_{OD}	Disable Access Time from Active High Output	–	30	–	45	ns
TDVQZ2	T_{OD}	Disable Access Time from Active Low Output	–	30	–	45	ns

NOTE: Maximum test frequency is 5MHz with a 50% duty cycle.

Description

The HPL-77153/82S153 is a programmable logic device designed to be cost effective and space saving replacement for discrete logic designs. This device is a two-level logic element, consisting of 32 product terms (AND) and 10 sum terms (OR) with fusible links for programming I/O polarity and direction.

All product terms can be linked to 8 inputs (I) and 10 bidirectional I/O lines (B) allowing variable I/O configurations using the 10 direction control gates (D), ranging from 17 inputs and 1 output to 8 inputs and 10 outputs.

On chip T/C buffers allow either True (I,B) and/or Complement ($\overline{I},\overline{B}$) signals to be linked to any of the product terms, the outputs of which may be used as inputs to any or all of the sum terms. The output polarity of the sum terms is individually programmable by means of a fuse link controlled EX-OR gate to allow implemention of Sum Of Products (SOP) or Inverted Sum Of Products (ISOP) expressions.

The HPL-77153/82S153 is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Nickel-chromium fuse technology is used on these and all other HARRIS HPL-77XXX programmable logic devices. The HPL-77153/82S153 is available in 20 pin slimline DIP packages with a pinout identical to the 82S153.

The HPL-77153/82S153 contains unique test circuitry developed by HARRIS which is enabled at the time of manufacture to allow complete AC and DC testing.

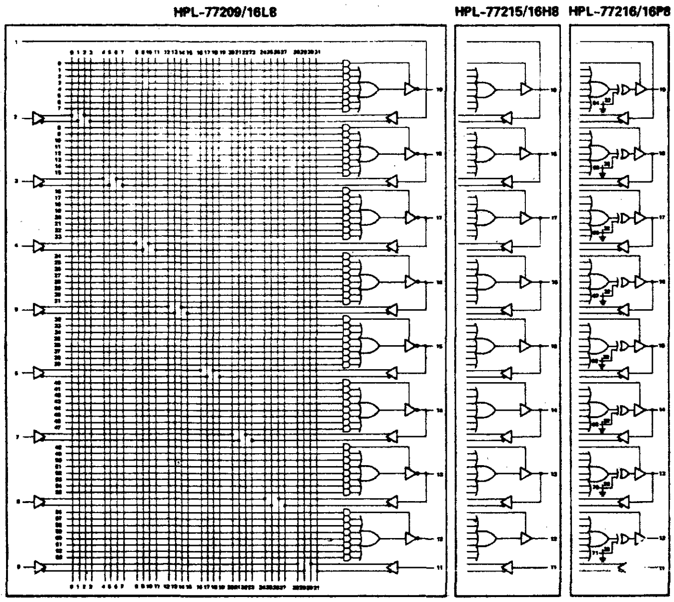
HARRIS

HPL-77215/16H8
HPL-77216/16P8
HPL-77209/16L8

HPL™ Harris Programmable Logic

Functional Diagram

HPL-77209/16L8 HPL-77215/16H8 HPL-77216/16P8



D.C. ELECTRICAL CHARACTERISTICS (Operating)

HPL-77215/216/209 −5 (V_{CC} = 5.0V±5%, T_A = 0°C to +75°C)
HPL-77215/216/209 −2/−8 (V_{CC} = 5.0V±10%, T_A = −55°C to +125°C)

SYMBOL	PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS	
I_{IH}	Input Current	"1"	—	+25	μA	V_{IH} = Vcc MAX	Vcc = Vcc MAX
I_{IL}	Dedicated Input	"0"	—	−100	μA	V_{IL} = 0.4 V	
I_{FZH}	Output Current	"1"	—	+40	μA	V_{FH} = Vcc MAX	Vcc = Vcc MAX
I_{FZL}	Hi-Z State	"0"	—	−40	μA	V_{FL} = 0.4V	
I_{BZH}	Bidirectional Pin Current	"1"	—	+40	μA	V_{BH} = Vcc MAX	Vcc = Vcc MAX
I_{BZL}	Hi-Z State	"0"	—	−100	μA	V_{BL} = 0.4V	
V_{IH}	Input Threshold (1)	"1"	2.0	—	V	Vcc = Vcc MAX	
V_{IL}	Voltage	"0"	—	0.8	V	Vcc = Vcc MIN	
V_{OH}	High-Level Output Voltage (2)		2.4	—	V	Vcc = Vcc MIN	I_{OH} = −2.0mA (M) I_{OH} = −3.2mA (C)
V_{OL}	Low-Level Output Voltage (2)		—	0.5	V	V_{IL} = 0.8V V_{IH} = 2.0V	I_{OL} = +16mA (M) I_{OL} = +24mA (C) (3)
V_{CL}	Input Clamp Voltage (1)		—	−1.2	V	I_{IN} = −18mA, Vcc = OV	
I_{OS}	Output Short Circuit Current (2)		−30	−130	mA	Vcc = 5.0V, V_{OUT} = OV One Output for MAX of One Sec.	
I_{CC}	Power Supply Current		—	155 (C)	mA	Vcc = Vcc MAX	
			—	165 (M)	mA		

C = Commercial (−5) M = Military (−2/−8)
(1) These specifications apply to both Input (I) and Bidirectional (B) pins.
(2) These specifications apply to both Output (F) and Bidirectional (B) pins.
(3) One output at a time, otherwise 16mA.

A. C. SWITCHING CHARACTERISTICS (Operating)

SYMBOL			HPL-77215−5 HPL-77216−5 HPL-77209−5 5V±5% 0°C to +75°C		HPL-77215−2/−8 HPL-77216−2/−8 HPL-77209−2/−8 5V±10% −55°C to +125°C		
JEDEC STANDARD	OLD SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
TDVQH1	T_{PD}	Propagation Delay – Input or I/O to Active High Output	—	35	—	45	ns
TDVQL1	T_{PD}	Propagation Delay – Input or I/O to Active Low Output	—	35	—	45	ns
TDVQH2	T_{PZX}	Enable Access Time to Active High Output (1)	TDVQZ1	35	TDVQZ1	45	ns
TDVQL2	T_{PZX}	Enable Access Time to Active Low Output (1)	TDVQZ2	35	TDVQZ2	45	ns
TDVQZ1	T_{PXZ}	Disable Access Time from Active High Output	—	30	—	35	ns
TDVQZ2	T_{PXZ}	Disable Access Time from Active Low Output	—	30	—	35	ns

(1) Enable Access Time is guaranteed greater than Disable Access Time to avoid device contention.
NOTE: Maximum test frequency is 5MHz with a 50% duty cycle.

Description

The HPL-77215/216/209 are programmable logic devices designed to be cost effective and space saving replacements for discrete logic designs. These devices are two-level logic elements consisting of 7 product terms (AND) summed (OR) together to generate each of the 8 outputs. An eighth product term associated with each output can drive it to a high impedance state allowing 6 (B0-B5) of the 8 outputs to be used as inputs, either permanently or dynamically.

The HPL-77209 is functionally identical to the industry standard 16L8, and implements logic expressions of the Inverted Sum Of Products (ISOP) form.

The HPL-77215 is a similar device to the 16L8 but does not include the associated output inversion. It implements logic expressions of the Sum Of Products (SOP) form.

The HPL-77216 is a more flexible device, it includes 8 EX-OR gates in each output path, controlled by 8 extra fuses, allowing the polarity of each output to be user configured. This device can implement a combination of SOP and ISOP expressions.

The HPL-77215/216/209 are field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Nickel-chromium fuse technology is used on these and all other HARRIS HPL-77XXX programmable logic devices. The HPL-77215/216/209 are available in 20 pin slimline DIP packages with pinouts identical to the 16L8.

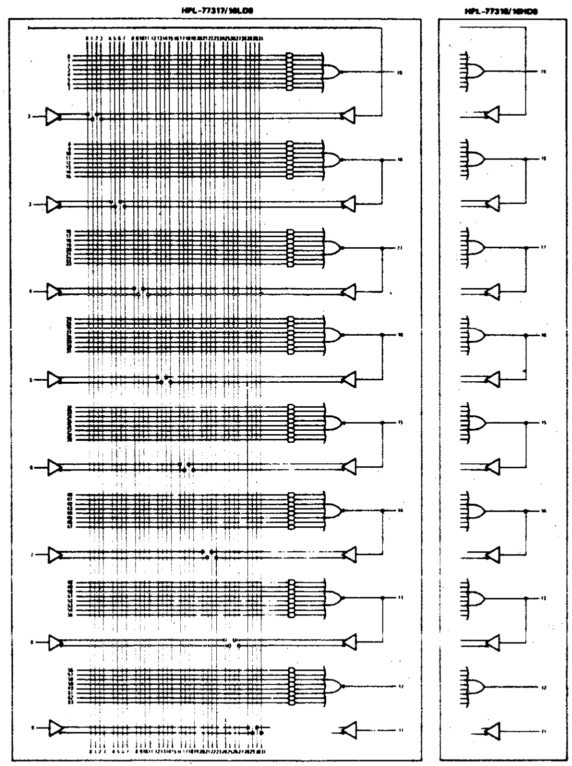
The HPL-77215/216/209 contain unique test circuitry developed by HARRIS which is enabled at the time of manufacture to allow complete AC and DC testing.

HARRIS

HPL-77317/16LD8
HPL-77318/16HD8

HPL™ Harris Programmable Logic

Functional Diagram



D.C. ELECTRICAL CHARACTERISTICS (Operating)

HPL-77317/318 -5 (Vcc = 5.0V+5%, T_A = 0°C to +75°C)
HPL-77317/318 -2/-8 (Vcc = 5.0V+10%, T_A = -55°c to +125°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS	
I_{IH} I_{IL}	Input Current "1" Dedicated Input "0"	— —	-25 100	μA μA	V_{IH} Vcc MAX V_{IL} 0.4 V Vcc Vcc MAX	
V_{IH}	Input Threshold Voltage "1"	2.0	—	V	Vcc Vcc MAX	
V_{IL}	Input Threshold Voltage "0"	—	0.8	V	Vcc Vcc MIN	
V_{OH}	High-Level Output Voltage	2.4	—	V	Vcc Vcc MIN	I_{OH} -2.0mA (M) I_{OH} -3.2mA (C)
V_{OL}	Low-Level Output Voltage	—	0.5	V	V_{IL} 0.8V V_{IH} = 2.0V	I_{OL} = +16mA (M) I_{OL} = +24mA (C) (1)
V_{CL}	Input Clamp Voltage (1)	—	-1.2	V	I_{IN} = -18mA, Vcc = OV	
I_{OS}	Output Short Circuit Current	-30	-130	mA	Vcc = 5.0V, V_{OUT} = OV One Output for MAX of One Sec.	
I_{CC}	Power Supply Current	— —	155 (C) 165 (M)	mA mA	Vcc = Vcc MAX	

C = Commercial (-5) M = Military (-2/-8)

(1) One output at a time, otherwise 16mA.

A. C. SWITCHING CHARACTERISTICS (Operating)

SYMBOL			HPL-77317-5 HPL-77318-5 5V ± 5% 0°C to +75°C		HPL-77317-2/-8 HPL-77318-2/-8 5V ± 10% -55°C to +125°C		
JEDEC STANDARD	OLD SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
TDVQH	TPD	Propagation Delay – Input to Active High Output	—	35	—	45	ns
TDVQL	TPD	Propagation Delay – Input to Active Low Output	—	35	—	45	ns

NOTE: Maximum test frequency is 5MHz with a 50% duty cycle.

Description

The HPL-77317/318 are programmable logic devices designed to be cost effective and space saving replacements for discrete logic designs. These devices are two-level logic elements consisting of 8 product terms (AND) summed (OR) together to generate each of the 8 outputs. To achieve 8 product terms per output, the ability to force the outputs to a high impedance state has not been included. All eight outputs are permanently active.

The HPL-77317 is similar to the industry standard 16L8, and implements logic expressions of the Inverted Sum Of Products (ISOP) form.

The HPL-77318 is a similar device to the HPL-77317, but does not include the associated output inversion. It implements logic expressions of the Sum Of Products (SOP) form.

Six of the 8 outputs feature feedback into the fuse matrix, allowing output functions to be utilized for other output functions.

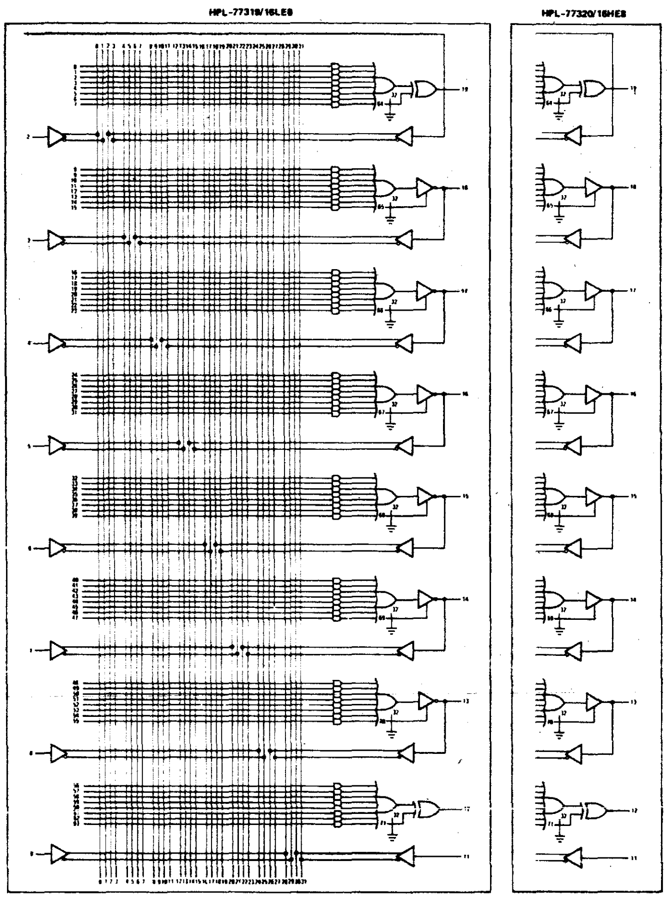
The HPL-77317/318 are field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Nickel-chromium fuse technology is used on these and all other HARRIS HPL-77XXX programmable logic devices. The HPL-77317/318 are available in 20 pin slimline DIP packages with pinouts similar to the 16L8.

The HPL-77317/318 contain unique test circuitry developed by HARRIS, which is enabled at the time of manufacture to allow complete AC, DC and functional testing.

HPL-77319/16LE8
HPL-77320/16HE8
HPL™ Harris Programmable Logic

Functional Diagram



D.C. ELECTRICAL CHARACTERISTICS (Operating)

HPL-77319/320-5 (V_{CC} = 5.0V±5%, T_A = 0°C to +75°C)
HPL-77319/320 -2/-8 (V_{CC} = 5.0V±10%, T_A = −55°C to +125°C)

SYMBOL	PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS	
I_{IH}	Input Current	"1"	—	+25	μA	V_{IH} = Vcc MAX	Vcc = Vcc MAX
I_{IL}	Dedicated Input	"0"	—	−100	μA	V_{IL} = 0.4 V	
I_{BZH}	Bidirectional Pin Current	"1"	—	+40	μA	V_{BH} = Vcc MAX	Vcc = Vcc MAX
I_{BZL}	Hi-Z State	"0"	—	−100	μA	V_{BL} = 0.4V	
V_{IH}	Input Threshold (1)	"1"	2.0	—	V	Vcc = Vcc MAX	
V_{IL}	Voltage	"0"	—	0.8	V	Vcc = Vcc MIN	
V_{OH}	High-Level Output Voltage (2)		2.4	—	V	Vcc = Vcc MIN	I_{OH} = −2.0mA (M) I_{OH} = −3.2mA (C)
V_{OL}	Low-Level Output Voltage (2)		—	0.5	V	V_{IL} = 0.8V V_{IH} = 2.0V	I_{OL} = +16mA (M) I_{OL} = +24mA (C) (3)
V_{CL}	Input Clamp Voltage (1)		—	−1.2	V	I_{IN} = −18mA, Vcc = 0V	
I_{OS}	Output Short Circuit Current (2)		−30	−130	mA	Vcc = 5.0V, V_{OUT} = 0V One Output for MAX of One Sec.	
I_{CC}	Power Supply Current		—	155 (C)	mA	Vcc = Vcc MAX	
			—	165 (M)	mA		

C = Commercial (−5) M – Military (−2/−8)
(1) These specifications apply to both Input (I) and Bidirectional (B) pins.
(2) These specifications apply to both Output (F) and Bidirectional (B) pins.
(3) One output at a time, otherwise 16mA.

A. C. SWITCHING CHARACTERISTICS (Operating)

SYMBOL			HPL-77319-5 HPL-77320-5 5V±5% 0°C to +75°C		HPL-77319-2/-8 HPL-77320-2/-8 5V±10% −55°C to +125°C		
JEDEC STANDARD	OLD SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
TDVQH	T_{PD}	Propagation Delay – Input or I/O to Active High Output	—	35	—	45	ns
TDVQL	T_{PD}	Propagation Delay – Input or I/O to Active Low Output	—	35	—	45	ns

NOTE: Maximum test frequency is 5MHz with a 50% duty cycle.

Description

The HPL-77319/320 are programmable logic devices designed to be cost effective and space saving replacements for discrete logic designs. These devices are two-level logic elements consisting of 8 product terms (AND) summed (OR) together to generate each of the 8 outputs. An extra fuse associated with each bi-directional pin can drive it to a high impedance state allowing 6 (B0-B5) of the 8 outputs to be used as inputs.

An extra fuse associated with each output pin can be used to control output polarity which is active high on an unprogrammed part.

The HPL-77319 is similar to the industry standard 16L8, and implements logic expressions of the Inverted Sum of Products (ISOP) form.

The HPL-77320 is a similar device to the HPL-77319 but does not include the associated output inversion. It implements logic expressions of the Sum of Products (SOP) form.

The HPL-77319/320 are field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Nickel-chromium fuse technology is used on these and all other HARRIS HPL-77XXX programmable logic devices. The HPL-77319/320 are available in 20 pin slimline DIP packages with pinouts identical to 16L8.

The HPL-77319/320 contain unique test circuitry developed by HARRIS which is enabled at the time of manufacture to allow complete AC, DC and functional testing.

PROGRAMMING HARRIS PROGRAMMABLE LOGIC (HPL)

Following is the programming procedure which is used for the HPL-77XXX devices. These devices are manufactured with all fuses intact. Any desired fuse can be programmed by following the simple procedure shown on the following page. One may build a programmer to satisfy the specifications described in the table, or use any of the commercially available programmers which meet these specifications.

PROGRAMMING SPECIFICATIONS

TABLE 1

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNITS
V_{CCP}	V_{CC} Supply During Programming[1]	I_{CCP} = 550 mA min	8.25	8.5	8.75	V
I_{CCP}	I_{CC} Limit During Programming	V_{CCP} = +8.50V±0.25V	550	—	1000	mA
V_{IH}	Input Voltage (High)		2.4	—	5.5	V
V_{IL}	Input Voltage (Low)		0.0	—	0.8	V
I_{IHP}	Input Current (High) During Prog.	V_{IH} = +5.5V	—	—	50	μA
I_{ILP}	Input Current (Low) During Prog.	V_{IL} = 0V	—	—	−500	μA
V_{OPF}	Forced Output Voltage[2]	I_{OPF} = 300mA±25mA Transient or Steady State	16.0	16.5	18.0	V
I_{OPF}	Forced Output Current	V_{OPF} = 17.5V±0.5V	275	300	325	mA
PW_V	Verify Pulse Width		1	5	50	μS
PW_P	Programming Pulse Width		90	100	110	μS
T_D	Pulse Sequence Delay		1	5	50	μS
t_{r2}	Forced Output Voltage Rise Time	10% to 90%	4	14	40	μS
t_{r1}	V_{CC} Supply Rise Time	10% to 90%	2	7	20	μS
t_{f2}	Forced Output Voltage Fall Time	90% to 10%	2	7	20	μS
t_{f1}	V_{CC} Supply Fall Time	90% to 10%	1	4	10	μS
T_{PP}	Programming Period		100	160	350	μS
F_L	Fusing Attempts per Link		—	1	2	Cycle
V_S	Verify Threshold[3]		1.4	1.5	1.6	V

NOTES:

1. Bypass V_{CC} to GND with a 0.01 μF capacitor to reduce voltage spikes. The V_{CC} power supply must be capable of handling 1 Ampere maximum.
2. Care should be taken to ensure that the voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the device output voltage for a programmed link. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.

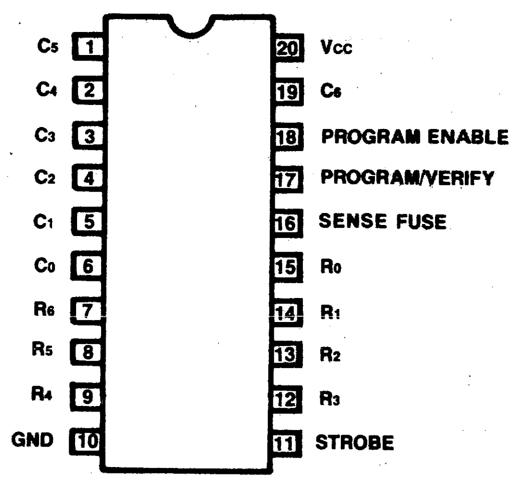


Figure 1
EDIT MODE PINOUT
HPL-77XXX

*NOTE: While programming HPL-77XXX devices, no pins should be left floating. Pin 16 (SENSE FUSE) appears as an open collector output during programming. It should be tied to VCC through a 10K ohm resistor. It is recommended that all unused row and column address pins be tied to GND. Consult individual HPL data sheets for information pertaining to selection of fuses.

HPL PROGRAMMING PROCEDURE & WAVEFORMS

PROGRAMMING PROCEDURE

1. Set-Up:
   a. During programming, no pins should be left floating. Pin 16 should be terminated with a 10k ohm resistor to V_{CC}.
   b. Set GND (Pin 10) to OV.
2. Select the EDIT Mode:
   a. Apply OV to Pin 20.
   b. Apply V_{IL} to Pin 18.
   c. Apply V_{IH} to Pin 11.
   d. Apply V_{IL} to Pin 17.
3. Select the Fuse to be Programmed:
   a. Wait T_D and select a ROW by specifying the appropriate binary ROW address according to Table 2.
   b. Select a COLUMN by specifying the appropriate binary COLUMN address according to Table 3.
4. Program the Fuse:
   a. Wait T_D and raise Pin 20 to V_{CCP}.
   b. Wait T_D and raise Pin 17 to V_{IH}.
   c. Wait T_D and raise Pin 18 to V_{OPF}.
   d. Wait T_D and pulse Pin 11 to V_{IL} for a duration of PWp.
   e. Return Pin 11 to V_{IH}.
   f. Wait T_D and lower Pin 18 to V_{IL}.
   g. Wait T_D and lower Pin 17 to V_{IL}.
5. Verify Programmed Fuse:
   a. Wait T_D and lower Pin 11 to V_{IL}.
   b. At the end of PW_V, monitor Pin 16 for a level of Vs.
   c. Return Pin 11 to V_{IH}.
   d. Wait T_D and lower Pin 20 to OV.
   e. If Pin 16 has indicated a V_{OL}, return to step 4 and repeat so that the fuse receives a maximum of two (2) fusing attempts.
6. Repeat Steps 3 Through 5 for All Fuses to be Blown.

PROGRAMMING WAVEFORMS

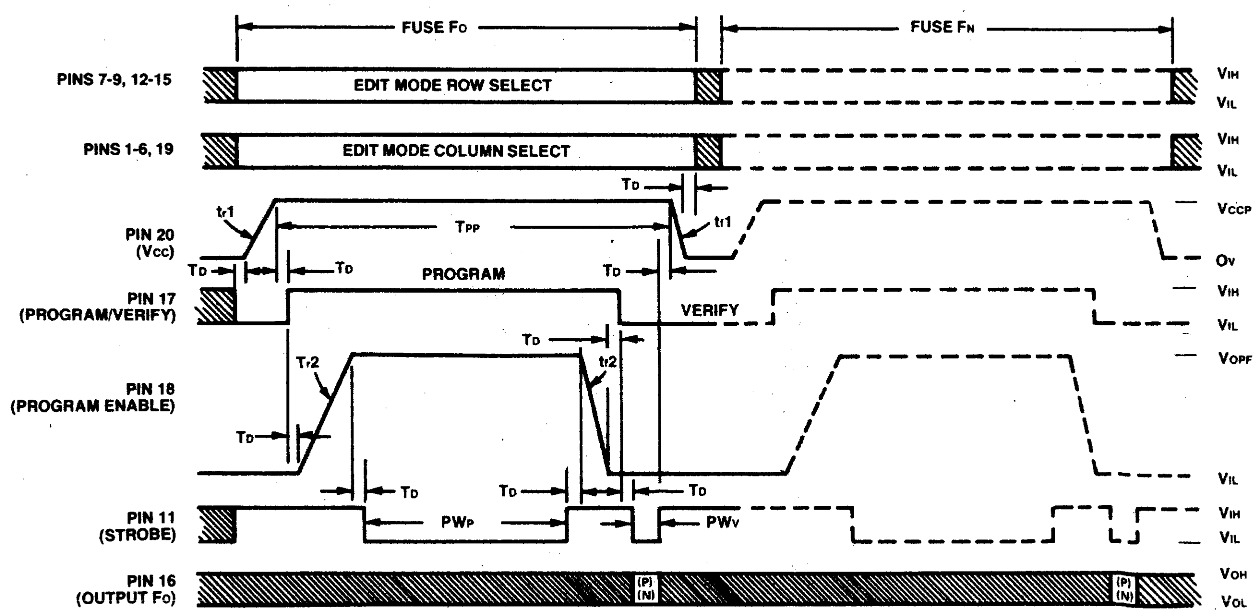


Figure 2

HARRIS

HPL-77061

Product Preview HPL™ Harris Programmable Logic

The HPL-77061 is a proprietary device designed by Harris Semiconductor. It is a 24 pin device with 12 input pins, 6 bi-directional pins, and 4 output pins. The architecture consists of a programmable AND array, followed by a fixed OR array, followed by a programmable INVERTER. This configuration generates a device that implements logic expressions in either SUM OF PRODUCTS (SOP) or INVERTED SUM OF PRODUCTS (ISOP) form. Two fuses associated with each output and bi-directional pin allow their three state buffers to be configured as permanently active, permanently inactive, or under the control of a common CHIP SELECT(CS) signal. When under the control of the CS signal, they may be configured to be active when CS is high and inactive when low, or active when CS is low and inactive when high.

The HPL-77061 is intended to be used as an address decoder in 8, 16 or 32 bit microprocessor systems, and is known as a FIELD PROGRAMMABLE ADDRESS DECODER (FPAD). When used as an address decoder, it is possible to contiguously concatenate the address spaces of large and small system components. This allows more efficient use to be made of available memory space, as well as making the memory decoder design easier. The HPL-77061 may also be used to replace several TTL packages in many random logic designs. In both the above applications, a significant reduction in board space, power consumption, package count, and an increase in reliability may be realized. The HPL-77061 incorporates Harris designed test circuitry which allows complete parametric and logical testing of unprogrammed devices at the time of manufacture. The benefits for the user of this exhaustive testing are very high POST PROGRAMMING FUNCTIONAL YIELD (95% guaranteed; 97% typically) and pretested AC and DC parametrics.

The HPL-77061 uses the standard HPL programming algorithm which is also used for all Harris Programmable Logic parts. Special test fuses are included in the HPL-77061. These are selectively programmed during post manufacturing testing. This allows all the programming circuitry to be tested for correct operation.

The Harris policy is to ship pretested devices, removing the test burden from the small user and assuring the large user the highest possible quality.

• PROPAGATION DELAY	25ns MAX COMMERCIAL
• SUPPLY CURRENT	140mA MAX COMMERCIAL
• PACKAGE	24 PIN SLIMLINE (POWER PLASTIC & CERAMIC)
• TEMPERATURE OPTIONS	COMMERCIAL, MILITARY & 883B
• AC/DC SPECS	PRETESTED
• FUNCTIONALITY	PRETESTED
• PROGRAMMING	GENERIC
• TTL COMPATIBLE	

HPL is a trademark of Harris Corporation

CMOS/NMOS RAMs - Cross Reference

Description	HARRIS	AMI	Fujitsu	Hitachi	IDT	Intersil	Micro Power Systems	Mitsubishi
1K CMOS RAMs	HM-6508 (1K × 1) 16-pin synch	6508	8401			6508	6508	
	HM-6518 (1K × 1) 18-pin synch	6518				6518	6518	
	HM-6551 (256 × 4) 22-pin synch					6551		
	HM-6561 (256 × 4) 18-pin synch					6561		
4K CMOS RAMs	HM-6504 (4K × 1) 18-pin synch	6504	8404	4315 6147		6504	6504	
	HM-6514 (1K × 4) 18-pin synch	6514	8414	4334 6148		6514	6514	58981
16K CMOS RAMs	HM-6516 (2K × 8) 24-pin synch	6516						
	HM-65162 (2K × 8) 24-pin asynch		8416	6116	6116			5117
	HM-65172 (2K × 8) 24-pin asynch		8418	6177				5116

Description	HARRIS	Motorola	National	NEC	OKI	RCA	Toshiba	NMOS Memories (Generic)
1K CMOS RAMs	HM-6508 (1K × 1) 16-pin synch	6508	6508 74C929	443		6508 1821	5508	2125 4015
	HM-6518 (1K × 1) 18-pin synch	6518	6518 74C930					
	HM-6551 (256 × 4) 22-pin synch		6551 74C920			1822	5101	2101
	HM-6561 (256 × 4) 18-pin synch							2111
4K CMOS RAMs	HM-6504 (4K × 1) 18-pin synch	6504	6504		5104		5504	2141/47 315D 4104 4404
	HM-6514 (1K × 4) 18-pin synch	6514	6514	444	5114 5115	5114	5114	2114 2148/49 4045 314A
16K CMOS RAMs	HM-6516 (2K × 8) 24-pin synch		6516					
	HM-65162 (2K × 1) 24-pin asynch	65116	6116	446	5128	6116	5517	2116 2016 4016 4802 2128 8128 58725
	HM-65172 (2K × 8) 24-pin asynch			449			5516	

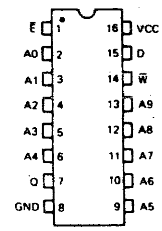
Harris Semiconductor

MEMORY

1024 × 1 — 1K Synchronous

Part Number	Access Time	Power Supply Current: Operating	Power Supply Current: Standby	Replaces Pin for Pin
HM-6508B	180 ns	4 mA/MHz	10 μA	National 74C929 Intersil 6508
HM-6508	250 ns	4 mA/MHz	10 μA	AMI 56508

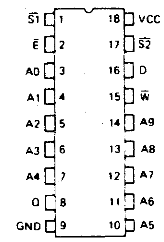
Pinout



1024 × 1 — 1K Synchronous

Part Number	Access Time	Power Supply Current: Operating	Power Supply Current: Standby	Replaces Pin for Pin
HM-6518B	180 ns	4 mA/MHz	10 μA	National 74C930 Intersil 6518
HM-6518	250 ns	4 mA/MHz	10 μA	

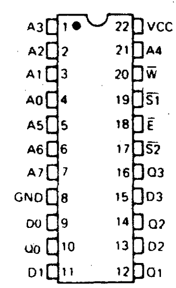
Pinout



256 × 4 — 1K Synchronous

Part Number	Access Time	Power Supply Current: Operating	Power Supply Current: Standby	Replaces Pin for Pin
HM-6551B	220 ns	4 mA/MHz	10 μA	Intersil 6551
HM-6551	300 ns	4 mA/MHz	10 μA	

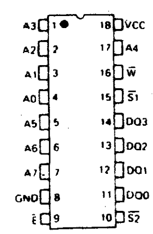
Pinout



256 × 4 — 1K Synchronous

Part Number	Access Time	Power Supply Current: Operating	Power Supply Current: Standby	Replaces Pin for Pin
HM-6561B	220 ns	4 mA/MHz	10 μA	Intersil 6561
HM-6561	300 ns	4 mA/MHz	10 μA	

Pinout

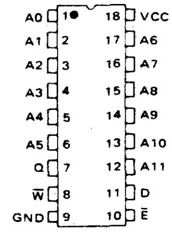


CMOS STATIC RAMs 4K & 16K

4096 × 1 — 4K Synchronous

Part Number	Access Time	Power Supply Current: Operating	Power Supply Current: Standby	Replaces Pin for Pin
HM-6504S	120 ns	7 mA/MHz	25 μA	Fujitsu 8404
HM-6504B	200 ns	7 mA/MHz	25 μA	Oki 5104
HM-6504	300 ns	7 mA/MHz	25 μA	National 6504

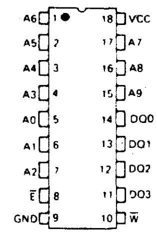
Pinout



1024 × 4 — 4K Synchronous

Part Number	Access Time	Power Supply Current: Operating	Power Supply Current: Standby	Replaces Pin for Pin
HM-6514S	120 ns	7 mA/MHz	25 μA	Fujitsu 6514 Hitachi 4334
HM-6514B	200 ns	7 mA/MHz	25 μA	NEC 444 RCA 5114
HM-6514	300 ns	7 mA/MHz	25 μA	Toshiba 5514 National 6514

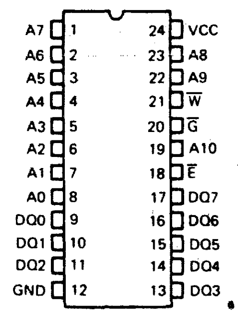
Pinout



2048 × 8 — 16K Synchronous

Part Number	Access Time	Power Supply Current: Operating	Power Supply Current: Standby	Similar To
HM-6516B	120 ns	10 mA/MHz	50 μA	Hitachi 6116 Toshiba 5517
HM-6516	200 ns	10 mA/MHz	50 μA	National 6516

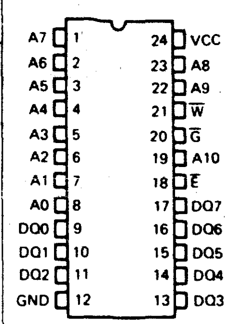
Pinout



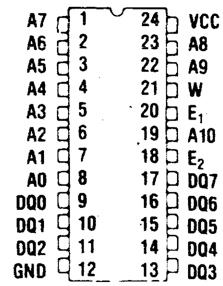
2048 × 8 — 16K Asynchronous

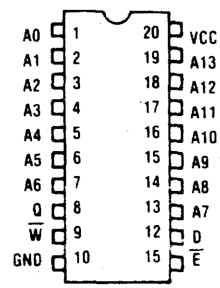
Part Number	Access Time	Power Supply Current: Operating	Power Supply Current: Standby	Replaces Pin for Pin
HM-65162S HM-65162B	55 ns 70 ns	70 mA 70 mA	100 μA 50 μA	Fujitsu 8416 Hitachi 6116 NEC 446
HM-65162	90 ns	70 mA	100 μA	Toshiba 5517 National 6116
HM-65162C	90 ns (Ind) 120 ns (Mil)	70 mA	1 mA	IDT 6116

Pinout



CMOS STATIC RAMs 16K

2048 × 8 — 16K Asynchronous					Pinout
Part Number	Access Time	Power Supply Current		Replaces Pin for Pin	
		Operating	Standby		
HM-65172S	55 ns	70 mA	100 μA	Fujitsu 8418 Hitachi 6117 Toshiba 5516 NEC 449	
HM-65172B	70 ns	70 mA	50 μA		
HM-65172	90 ns	70 mA	100 μA		
HM-65172C	90 ns (Ind)	70 mA	1 mA		
	120 ns (Mil)	70 mA	1 mA		

16384 × 1 — 16K Asynchronous					Pinout
Part Number	Access Time	Power Supply Current		Replaces Pin for Pin	
COMING SOON		Operating	Standby		
HM-65262B	55 ns	60 mA	50 μA	Hitachi 6167 IDT 6167	
HM-65262	70 ns	60 mA	50 μA		

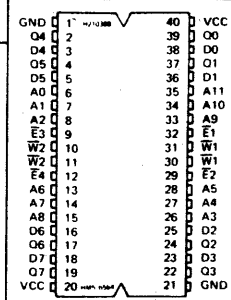
HARRIS

CMOS STATIC RAM MODULES 64K & 256K

LCC RAM Module — 16384 × 4/8192 × — 64K Synchronous

Part Number	Access Time	Power Supply Current		Replaces Pin for Pin
		Operating	Standby	
HM5-6564	350 ns	56/28 mA	800 µA	—
HM5-6564-5	450 ns	60/30 mA	4.0 µA	—

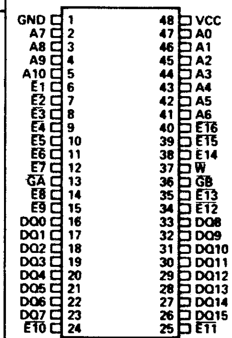
Pinout



LCC RAM Module - 16384 × 16/32768 × 8 — 256K Synchronous

Part Number	Access Time	Power Supply Current		Replaces Pin for Pin
		Operating	Standby	
HM-92560	150 ns	30/15 mA	50 µA	—
HM-92560-5	250 ns	35/20 mA	3.5 mA	—

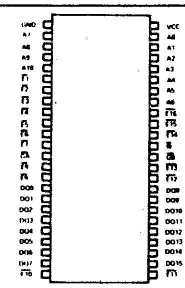
Pinout



LCC Unbuffered RAM Module - 16384 × 16/32768 × 8 — 256K Asynchronous

Part Number	Access Time	Power Supply Current		Replaces Pin for Pin
		Operating	Standby	
COMING SOON HM-92562	90 ns	75 mA	500 µA	—

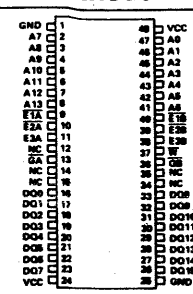
Pinout



LCC Buffered RAM Module - 16384 × 16/32768 × 8 — 256K Synchronous

Part Number	Access Time	Power Supply Current		Replaces Pin for Pin
		Operating	Standby	
HM-92570	250 ns 300 ns	30/15 mA 35/20 mA 35/20 mA	600 µA 3.5 mA	—

Pinout



Harris Semiconductor

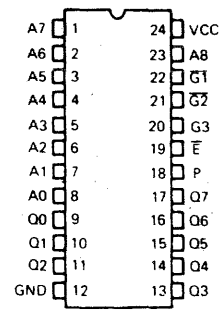
MEMORY

CMOS PROMs 4K, 16K & 64K

512 × 8 — 4K Synchronous

Part Number	Memory Element	Access Time	Power Supply Current: Operating	Power Supply Current: Standby	Replaces Pin for Pin
HM-6641	Fuse	250 ns	10 mA/MHz	100 μA	Bipolar 7641 Signetics 82S141

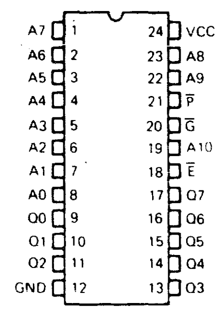
Pinout



2048 × 8 — 16K Synchronous

Part Number	Memory Element	Access Time	Power Supply Current: Operating	Power Supply Current: Standby	Replaces Pin for Pin
HM-6616B	Fuse	90 ns	15 mA/MHz	100 μA	NMOS 2716 National 27C16 National 6716 Intersil 6716
HM-6616	Fuse	120 ns	15 mAMHz	100 μA	

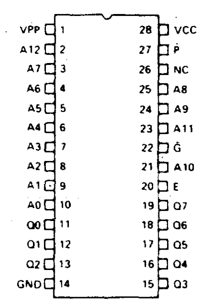
Pinout



8192 × 8 — 64K Asynchronous

Part Number	Memory Element	Access Time	Power Supply Current: Operating	Power Supply Current: Standby	Replaces Pin for Pin
COMING SOON HM-6664	Fuse	175 ns	10 mA/MHz	100 μA	NMOS 2764 Fujitsu 27C64

Pinout

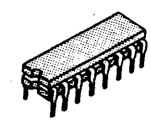


HM50256-12, HM50256-15 — Preliminary
HM50256-20

262144-word × 1-bit Dynamic Random Access Memory

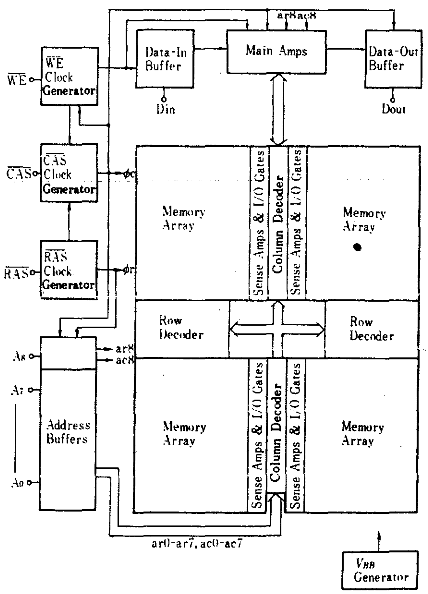
■FEATURES

- Industry Standard 16-Pin DIP
- Single 5V (±10%)
- On chip substrate bias generator
- Low Power: 350mW active, 23mW standby
- High speed: Access Time 120ns/150ns/200ns(max.)
- Common I/O capability using early write operation
- Page mode capability
- TTL compatible
- 256 refresh cycles.....(4 ms)
- 3 variation of refresh . . . $\overline{RAS}$ only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh
  Hidden refresh

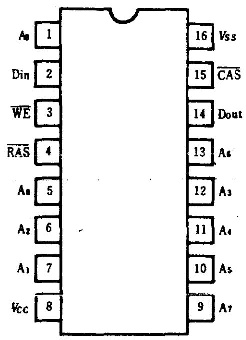


(DG-16B)

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

A_0~A_8	Address Inputs
$\overline{CAS}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
A_0~A_7	Refresh Address Inputs

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachis Sales Dept, regarding specifications.

■ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . −1V to +7V
Operating temperature, Ta (Ambient) . . . . 0°C to +70°C
Storage temperature . . . . −65°C to +150°C
Power dissipation 1W
Short circuit output current 50mA

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	min	typ	max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

Note) 1. All voltages referenced to V_{SS}

HITACHI

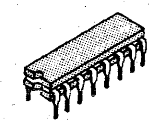
HM50257-12, HM50257-15, HM50257-20

Preliminary

262144-word × 1-bit Dynamic Random Access Memory

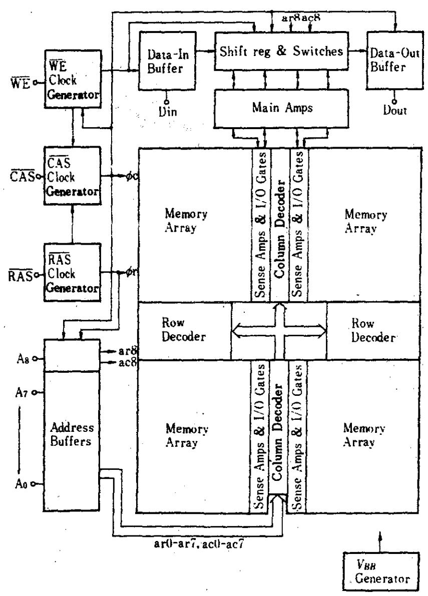
■ FEATURES

- Industry standard 16-pin DIP
- Single 5V (±10%)
- On chip substrate bias generator
- Low Power: 350mW active, 20mW standby
- High speed: Access Time 120ns/150ns/200ns (max.)
- Common I/O capability using early write operation
- Nibble mode capability
- Indifinite Dout hold using $\overline{CAS}$ control
- TTL compatible
- 256 refresh cycles ..... (4ms)
- 3 Variations of refresh; $\overline{RAS}$ only refresh, $\overline{CAS}$ befor $\overline{RAS}$ refresh, Hidden refresh

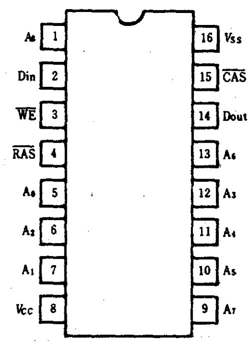


(DG-16B)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

$A_0 \sim A_8$	Address Inputs
$\overline{CAS}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
$A_0 \sim A_7$	Refresh Address Inputs

■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS}	-1V to +7V
Operating temperature, Ta (Ambient)	0°C to +70°C
Storage temperature	-65°C to +150°C
Power dissipation	1W
Short circuit output current	50mA

■ RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	min	typ	max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

Note 1) All voltages referenced to V_{SS}.

Note)
The specifications of this device are subject to change without notice.
Please contact your nearest Hitachis Sales Dept, regarding specifications.

HITACHI

Hitachi America

MEMORY

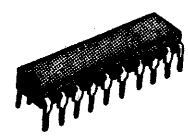
HM6168H-45, HM6168H-55, HM6168H-70, HM6168HP-45, HM6168HP-55, HM6168HP-70 — Preliminary

4096-word × 4-bit High Speed Static CMOS RAM

■FEATURES

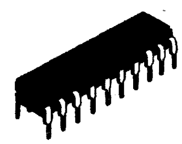
- High Speed: Fast Access Time 45/55/70 ns (max.)
- Single +5V Supply and High Density 20 Pin Package
- Low Power Standby and Low Power Operation;
  100μW typ. (Standby), 250mW typ. (Operation)
- Completely Static Memory
  No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible — All Inputs and Outputs

HM6168H-45/55/70



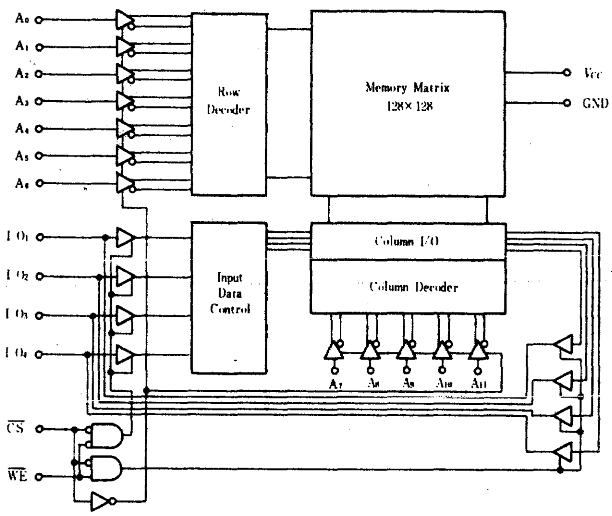
(DG-20)

HM6168HP-45/55/70

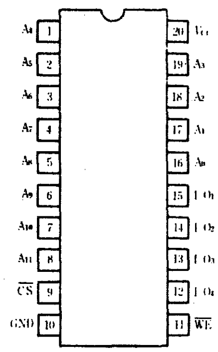


(DP-20)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_{IN}	−3.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (Ceramic)	T_{stg}	−65 to +150	°C
Storage Temperature (Plastic)	T_{stg}	−55 to +125	°C
Temperature under Bias	T_{bias}	−10 to +85	°C

* Pulse Width 20ns, DC= −0.5V

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachis Sales Dept. regarding specifications.

HITACHI

Hitachi America

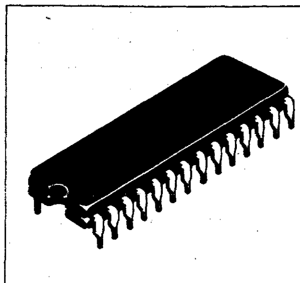
MEMORY

HM6264P-10, HM6264P-12, HM6264P-15

8192-word x 8-bit High Speed Static CMOS RAM

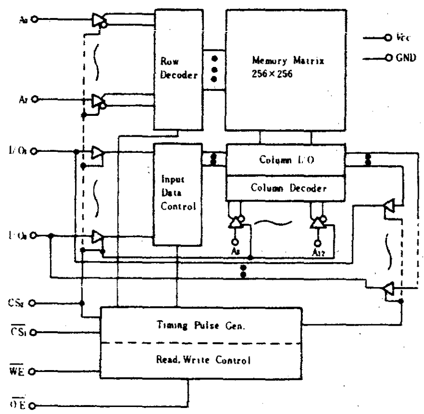
■ FEATURES

- Fast access Time — 100ns/120ns/150ns (max.)
- Low Power Standby — Standby: 0.1mW (typ.)
  Low Power Operation — Operating: 200mW (typ.)
- Single +5V Supply
- Completely Static Memory..... No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three State Output
- Directly TTL Compatible: All Input and Output
- Standard 28pin Package Configuration
- Pin Out Compatible with 64K EPROM HN482764

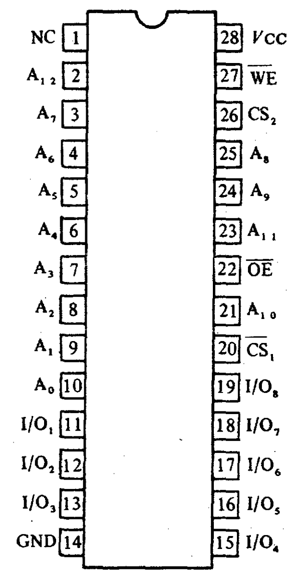


(DP-28)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage *	V_T	−0.5 ** to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature (Under Bias)	T_{bias}	−10 to +85	°C

* With respect to GND. ** Pulse width 50ns: −3.0V

■ TRUTH TABLE

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB}, I_{SB1}	
X	X	L	X		High Z	I_{SB}, I_{SB2}	
H	L	H	H	Output Disabled	High Z	I_{CC}, I_{CC1}	
H	L	H	L	Read	Dout	I_{CC}, I_{CC1}	
L	L	H	H	Write	Din	I_{CC}, I_{CC1}	Write Cycle (1)
L	L	H	L		Din	I_{CC}, I_{CC1}	Write Cycle (2)

× : Don't care.

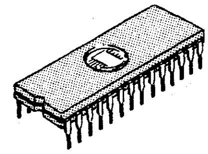
HITACHI

HN27C64G-20
HN27C64G-25, HN27C64G-30

8192-word X 8-bit UV Erasable and Programmable Read Only Memory

The HN27C64G is a 8192 word by 8-bit erasable and electrically programmable ROM. This device is packaged in a 28 pin dual-in-line package with transparent lid. The transparent lid on the package allows the memory content to be erased with ultraviolet light.

HN27C64G-20,
HN27C64G-25, HN27C64G-30

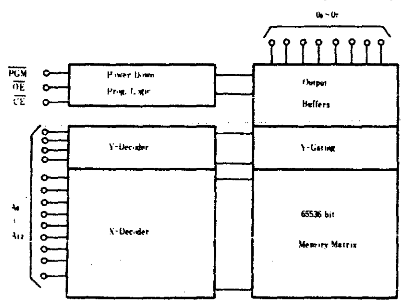


(DG-28)

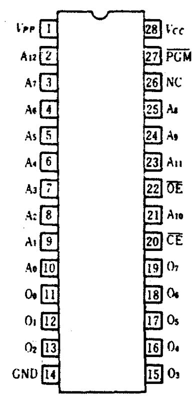
■ FEATURES

- Single Power Supply .... +5V ± 5%
- Simple Programming .... Program Voltage: +21V D.C. Program with one 50ms Pulse
- Static .... No clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Mode.
- Access Time .... HN27C64G-20 200ns Max.
  HN27C64G-25 250ns Max.
  HN27C64G-30 300ns Max.
- High Performance Programming Available
- Low Power Dissipation .... 40mW/MHz (Active Mode)
  525μW Max. (Stand-by Mode)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ MODE SELECTION

Mode \ Pins	CE (20)	OE (22)	PGM (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11~13, 15~19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Dout
Stand-by	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	X	V_{IL}	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Dout
Program Inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	High Z

X : don't care

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +125	°C
All Input and Output Voltage*	V_{in}, V_{out}	-0.6 to +7.0	V
V_{PP} Voltage	V_{PP}	-0.6 to +25	V
V_{CC} Voltage*	V_{CC}	-0.6 to +7.0	V

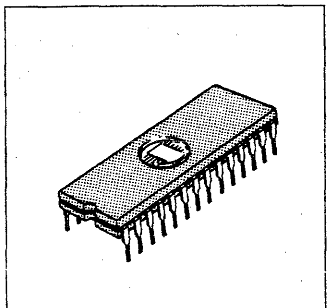
* : with respect to GND

HITACHI

HN4827128G-25, HN4827128G-30, HN4827128G-45

16384-Word x 8-bit UV Erasable and Programmable Read Only Memory

The HN4827128 is a 16384 word by 8 bit erasable and electrically programmable ROM. This device is packaged in a dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can then be written into the device.

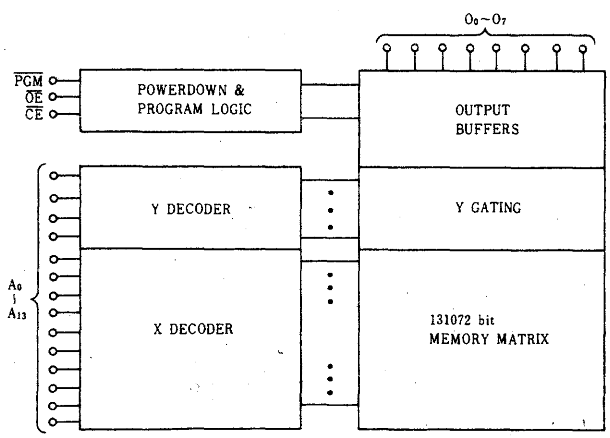


(DG-28)

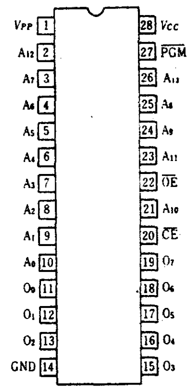
■FEATURES

- Single Power Supply . . . . +5V ± 5%
- Simple Programming . . . . Program Voltage: +21V DC
  Program with One 50ms Pulse
- Static . . . . No Clocks Required
  Inputs and Outputs TTL Compatible During Both Read and Program Mode.
- Access Time 250ns/300ns/450ns
- Absolute Max. Rating of Vpp Pin 26.5V
- Low Stand-by Current 35mA
- High Performance Programming Available
- Compatible with INTEL 27128

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■MODE SELECTION

MODE \ Pins	CE (20)	OE (22)	PGM (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11~13, 15~19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Dout
Stand by	V_{IH}	×	×	V_{CC}	V_{CC}	High Z
Program	V_{IL}	×	V_{IL}	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Dout
Program Inhibit	V_{IH}	×	×	V_{PP}	V_{CC}	High Z

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

HITACHI

Don't Miss the IC Updates

These quarterly updates keep your IC Master current the year 'round.

Look for them in Integrated Circuits Magazine

inmos

High Performance 16Kx1 Static RAM

IMS1400

FEATURES

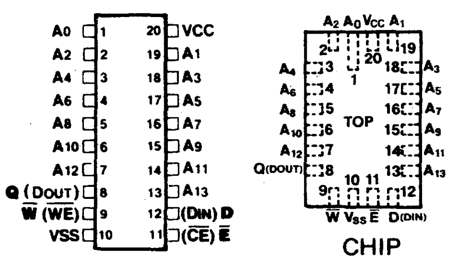
- 35, 45 and 55ns Chip Enable access
- Maximum active power 660mW
- Maximum standby power 110mW
- Single 5 volt ± 10% supply
- $\overline{E}$ ($\overline{CE}$) power down function
- TTL compatible inputs and output
- Fully static—no clocks for timing
- Three-state output

IMS1400L

FEATURES

- 70 and 100ns Chip Enable access
- Maximum active power 495mW
- Maximum standby power 83mW
- Single 5V ± 10% Supply
- $\overline{E}$ power down function
- TTL compatible inputs and output
- Fully static - no clocks for timing
- Three-state output

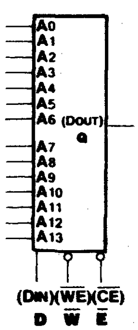
PIN CONFIGURATION



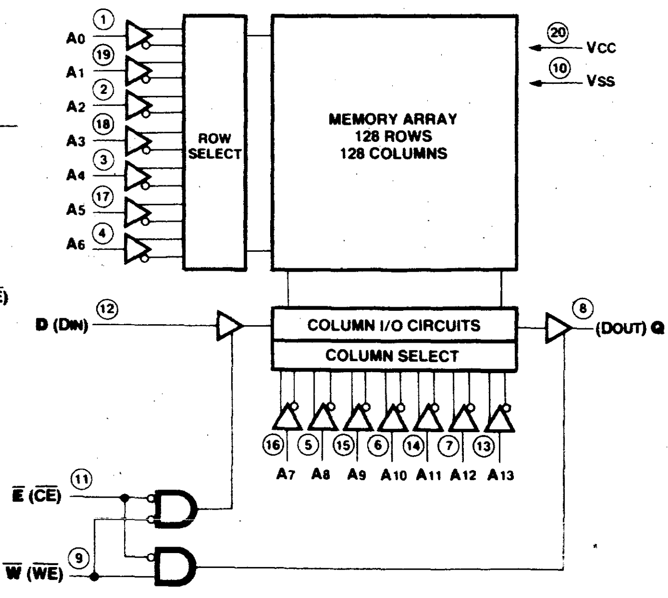
DIP

CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A0 - A13 ADDRESS INPUTS	VCC POWER (+5V)
W (WE) WRITE ENABLE	VSS GROUND
E (CE) CHIP ENABLE	
D (DIN) DATA INPUT	
Q (DOUT) DATA OUTPUT	

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High Performance 4Kx4 Static RAM

inmos

IMS1420
IMS1421

IMS1420L

FEATURES

- 4K x 4 Bit Organization
- 40nsec and 50nsec Address Access Times
- 605mW Maximum Power Dissipation
- Fully TTL Compatible
- Common Data Inputs & Outputs
- 20-pin, 300-mil DIP
- Single +5V ± 10% Operation

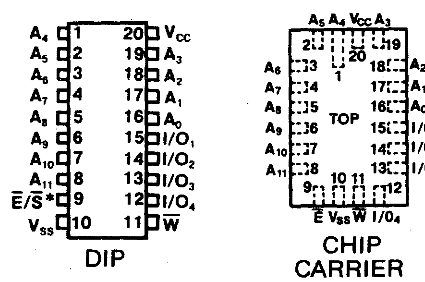
IMS1420
- 45nsec and 55nsec Chip Enable Access Times
- Power Down Function
- 165mW Maximum Standby Power

IMS1421
- High Speed Chip Select Function
- 30nsec and 40nsec Chip Select Access Times

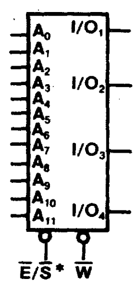
FEATURES

- 4K x 4 Bit Organization
- 70 and 100ns Chip Enable Access Times
- 65 and 95ns Address Access Times
- 495mW Maximum Power Dissipation
- 83mW Maximum Standby Power
- Fully TTL Compatible
- Common Data Inputs & Outputs
- 20-pin, 300-mil Plastic DIP
- Single +5V ± 10% Operation
- Power Down Function

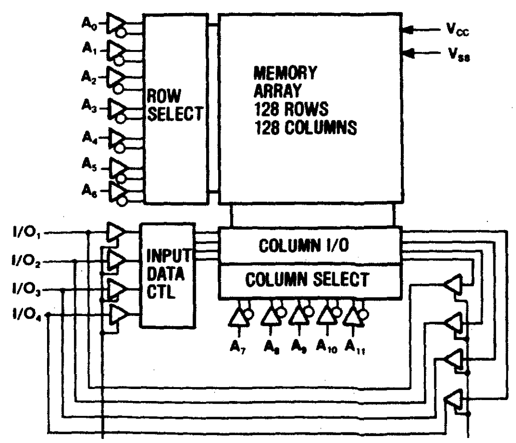
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_{11}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
W̄	WRITE ENABLE	V_{SS}	GROUND
Ē*	CHIP ENABLE		
S̄*	CHIP SELECT		
I/O	DATA IN/OUT		

*Ē IMS1420 ONLY
S̄ IMS1421 ONLY

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High Performance 64K Dynamic RAM

inmos

IMS2600 64Kx1 | IMS2620 16Kx4

IMS2600 64Kx1

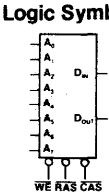
FEATURES

- High Speed, $\overline{RAS}$ Access of 100, 120 and 150ns
- Cycle Times of 160, 190 and 230ns
- Low Power:
  22mW Standby
  303mW Active (350ns Cycle Time)
  413mW Active (190ns Cycle Time)
- Single +5V ± 10% Power Supply
- On-Chip refresh using $\overline{CAS}$-before-$\overline{RAS}$, Pin 1 left as N/C for 256K expansion
- Indefinite D_{OUT} Hold Under $\overline{CAS}$ Control
- Industry Standard 16 Pin Configuration
- Nibble-Mode Capability (High Speed 4 Bit Serial Mode)
- 4ms/256 Cycle Refresh
- All Inputs and Output TTL Compatible
- Read, Write, Read-Modify-Write Capability both on Single Bit and in Nibble Mode Operation
- $\overline{RAS}$-Only Refresh Capability
- Common I/O Capability using "Early-Write"

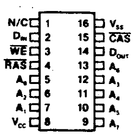
Pin Names

A_0-A_7	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{RAS}$	ROW ADDRESS STROBE
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{WE}$	WRITE ENABLE
V_{CC}	+5 VOLT SUPPLY INPUT
V_{SS}	GROUND

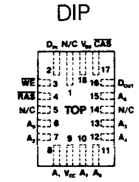
Logic Symbol



Pin Configuration

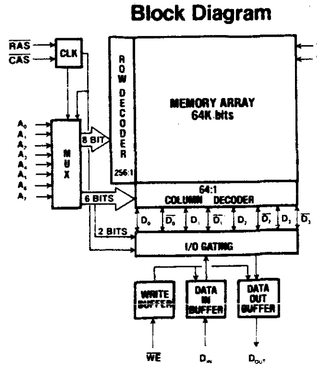


DIP



Chip Carrier

Block Diagram



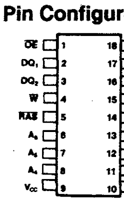
IMS2620 16Kx4

*No Page Mode Operation

FEATURES

- 16K x 4 Organization
- High Speed, $\overline{RAS}$ Access of 100, 120 and 150ns
- Cycle Times of 160, 190, and 240ns
- Low Power:
  28mW Standby
  495mW Active (160ns Cycle Time)
  330mW Active (350ns Cycle Time)
- Common I/O
- Single +5V ± 10% Power Supply
- On-Chip Refresh Assist using $\overline{CAS}$-before-$\overline{RAS}$
- Multiplexed Addresses 8 Row, 6 Column
- 18-Pin Package—JEDEC Standard Pinout
- All Inputs and Outputs TTL Compatible
- Output Enable ($\overline{OE}$) Control for Greater Timing Flexibility
- 4ms/256 Cycle Refresh
- Read, Write and Read-Modify-Write Capability
- 25 MBit Data Rate

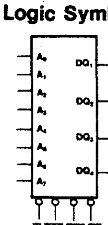
Pin Configuration



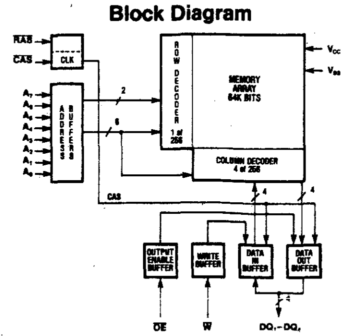
Pin Names

A_0 - A_7	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{RAS}$	ROW ADDRESS STROBE
DQ_1 - DQ_4	DATA IN/DATA OUT
$\overline{OE}$	OUTPUT ENABLE
$\overline{W}$	WRITE ENABLE
V_{CC}	+5V SUPPLY
V_{SS}	GROUND

Logic Symbol



Block Diagram



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IMS2630

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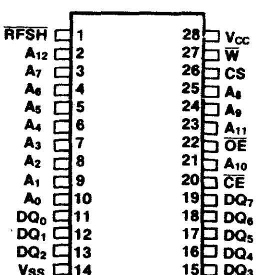
High Performance 8Kx8 Dynamic RAM

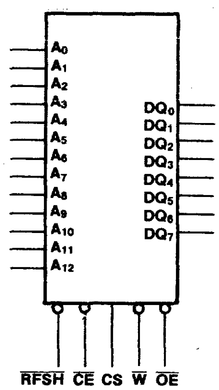
FEATURES
- 8Kx8 Byte-Wide Organization
- High Speed Chip Enable Access of 120, 150 and 200ns
- 28-Pin Package—JEDEC Standard Pinout
- 256 Cycle/4ms Refresh
- On-Chip Refresh Counter
- Hidden Refresh Using Pin 1 Refresh
- Single +5V ± 10% Supply
- Latched Chip Select and Address
- High Speed Output Enable Control
- Low Power
  - 42mW Standby
  - 358mW Max @ 190ns cycle
  - 275mW Max @ 240ns cycle
  - 220mW Max @ 310ns cycle

TYPICAL APPLICATIONS
- Cost-Effective Alternative to 8Kx8 SRAMs
- Easily Interfaced with Microprocessors
- Buffer Memory
- Controllers
- Terminals
- Printers
- Displays
- Personal Computers
- Games
- Instrumentation

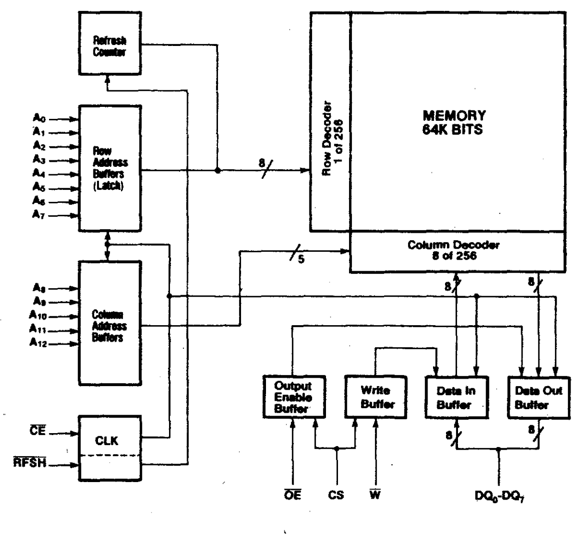
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_{12}	ADDRESS INPUTS		
CE	CHIP ENABLE	DQ_0-DQ_7	DATA IN/DATA OUT
CS	CHIP SELECT	V_{CC}	+5V SUPPLY
W	WRITE ENABLE	V_{SS}	GROUND
OE	OUTPUT ENABLE	RFSH	REFRESH ENABLE

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IMS3630

8Kx8 EEPROM

inmos

FEATURES

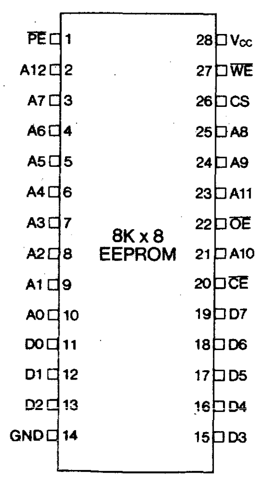
- High Speed, Chip Enable Access of 200ns
- +5 Volt Only Operation For All Modes
- Advanced Nitrox Process
- Row Or Full Array Erase Mode
- Single Byte Or Multiple Byte Modification
- Row Programming—Provides Up To 64 Times Faster Programming
- Latched Addresses and Data
- Latched Program/Erase Allows Processor To Perform Other Functions During Non-Volatile Modification
- Clocked Operation Provides Low Standby Power
- Industry Standard 28 Pin Dual-In-Line Pinout

TYPICAL APPLICATIONS

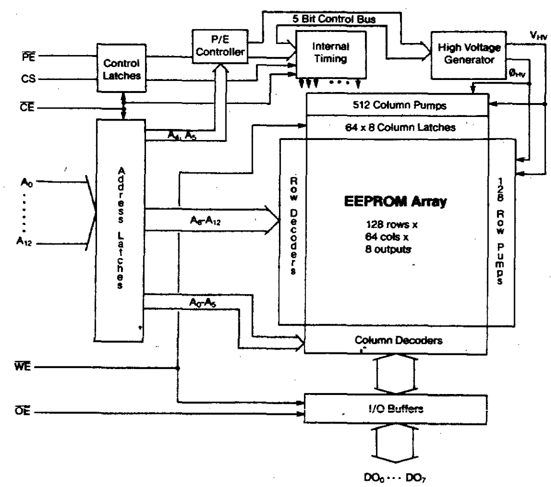
- Computer Systems
- Point of Sale Terminals
- Communication Systems
- Process Controllers
- Telemetry Systems
- Control Systems
- Instrumentation

The IMS3630 has been optimized for in-system operation. All modes of operation, including Chip Erase, are executed with a single +5 volt supply and standard TTL signal levels. Furthermore, all programming and erasing operations are controlled by using a simple sequence of initiate and terminate cycles. This eliminates the need to hold control signals, addresses, or data during the extended intervals required for programming or erasing.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



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CMOS STATIC RAMS 16K (2K x 8 BIT)

IDT6116S IDT6116L

MILITARY / INDUSTRIAL / COMMERCIAL TEMPERATURE RANGES

FEATURES:

- High-speed (equal access and cycle time)
  - —MILITARY/INDUSTRIAL
    IDT6116S 90/120/150 ns (max.)
    IDT6116L 90/120/150 ns (max.)
  - —COMMERCIAL
    IDT6116S 70/90/120 ns (max.)
    IDT6116L 90/120/150 ns (max.)
- Low power consumption
  - IDT6116S: Active: 180 mW (Typ.), Standby: 100 μW (Typ.)
  - IDT6116L: Active: 160 mW (Typ.), Standby: 20 μW (Typ.)
- Battery backup operation — 2V data retention voltage
- Produced with advanced CEMOS™ I high-performance technology
- CEMOS™ I process virtually eliminates alpha particle soft-error rates (with no organic die coatings)
- Single 5V (±10%) power supply
- Input and output directly TTL compatible
- Three-state output
- Static operation: no clocks or refresh required
- Standard 24-pin dual-in-line ceramic sidebrazed package or 28-pin and 32-pin LCC
- Pin compatible with standard 16K static RAM and EPROM
- Standard product 100% screened to MIL-STD-883, Class C
- Military product available 100% screened to Class B

DESCRIPTION:

The IDT6116 is a 16,384-bit high-speed static RAM organized as 2K x 8. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS™ I. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective alternative to bipolar and fast NMOS memories.

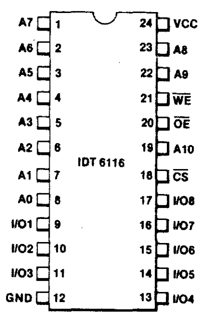
Access times as fast as 70ns are available with maximum power consumption of only 550mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby power mode as long as $\overline{CS}$ remains high. In the standby mode, the low power device consumes less than 20μW typically. This capability provides significant system level power and cooling savings. Both versions also offer a battery backup data retention capability where the circuit typically consumes only 1 μW to 4 μW operating off of a 2V battery.

All inputs and outputs of the IDT6116 are TTL compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation, providing equal access and cycle times for ease of use.

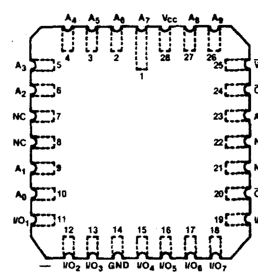
The IDT6116 is packaged in either a 24-pin, 600 mil or 300 mil DIP, 32-pin and 28-pin leadless chip carriers, or 24-pin flatpack, providing high board-level packing densities.

The IDT6116 Military RAM is 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

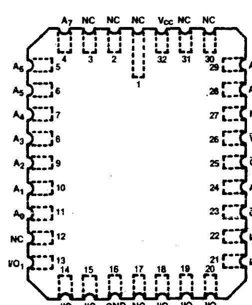
PIN CONFIGURATIONS



24 PIN SIDEBRAZE TOP VIEW

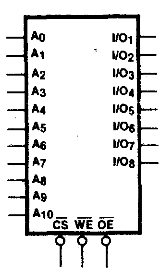


28 PIN LCC TOP VIEW



32 PIN LCC TOP VIEW

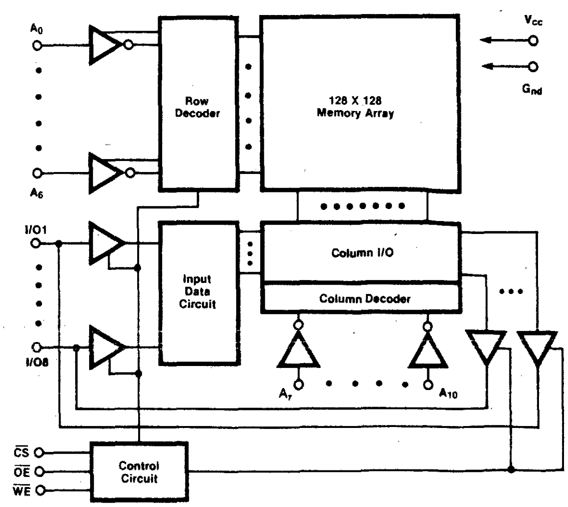
LOGIC SYMBOL



PIN NAMES

A_0-A_{10}	ADDRESS	$\overline{WE}$	WRITE ENABLE
I/O_1-I/O_8	DATA INPUT/OUTPUT	$\overline{OE}$	OUTPUT ENABLE
$\overline{CS}$	CHIP SELECT	GND	GROUND
V_{CC}	POWER		

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS[1]

TEMPERATURE RANGE		−55°C to +125°C	−40°C to +85°	0°C to +70°C	
SYMBOL	PARAMETER	RATING			UNIT
V_{TERM}	Voltage on any Pin with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	−0.5 to +7.0	V
T_A	Operating Temperature	−55 to +125	−40 to +85	0 to +70	°C
T_{BIAS}	Temperature Under Bias	−65 to +135	−55 to +125	−10 to +85	°C
T_{STG}	Storage Temperature	−65 to +150	−65 to +150	−55 to +125	°C
P_T	Power Dissipation	1.0	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	50	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	−1.0*	—	+0.8	V
C_L	Output Load	—	—	100	pF
TTL	Output Load	—	—	1	—

MILITARY (T_A = −55°C to +125°C)
INDUSTRIAL (T_A = −40°C to +85°C)
COMMERCIAL (T_A = 0°C to +70°C)

* V_{IL} min. = −3.5V for pulse widths less than 30 ns and duty cycles less than 50%.

IDT6116S DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V ±10%, T_A= −55°C to +125°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT6116S90/120 MIN.	TYP.[1]	MAX.	IDT6116S150 MIN.	TYP.[1]	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}	—	—	10	—	—	10	μA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = GND to V_{CC}	—	—	10	—	—	10	μA
I_{CC}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	—	40	100	—	35	90	mA
I_{CC1}	Operating Power Supply Current	V_{IH} = 3.5V, V_{IL} = 0.6V $I_{I/O}$ = 0mA	—	35	—	—	30	—	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100%	—	40	100	—	35	90	mA
I_{SB}	Standby Power Current	$\overline{CS}$ = V_{IH}	—	5	25	—	5	25	mA
I_{SB1}	Standby Power Current	$\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V	—	0.02	10	—	0.02	10	mA
V_{OL}	Output Low Voltage	I_{OL} = 3.5mA[2]	—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −1.0mA	2.4	—	—	2.4	—	—	V

1. V_{CC} = 5V, T_A = 25°C
2. I_{OL} = 2.1mA for IDT6116S150

IDT6116L DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = −55°C to +125°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT6116L90/120 MIN.	TYP.[1]	MAX.	IDT6116L150 MIN.	TYP.[1]	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}	—	—	5	—	—	5	μA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = GND to V_{CC}	—	—	5	—	—	5	μA
I_{CC}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	—	40/35	100/90	—	30	80	mA
I_{CC1}	Operating Power Supply Current	V_{IH} = 3.5V, V_{IL} = 0.6V $I_{I/O}$ = 0mA	—	35/30	—	—	30	—	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100%	—	40/35	100/90	—	30	80	mA
I_{SB}	Standby Power Current	$\overline{CS}$ = V_{IH}	—	5	20	—	5	15	mA
I_{SB1}	Standby Power Current	$\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V	—	4	900	—	4	900	μA
V_{OL}	Output Low Voltage	I_{OL} = 3.5mA[2]	—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −1.0mA	2.4	—	—	2.4	—	—	V

1. V_{CC} = 5V, T_A = 25°C
2. I_{OL} = 2.1mA for IDT6116L150

Integrated Device Technology, Memory

Integrated Device Technology, Inc. 3236 Scott Blvd., Santa Clara, CA 95051
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IDT6116S DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V ±10%, T_A=−40°C to +85°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT6116S90/120 MIN.	TYP.(1)	MAX.	IDT6116S150 MIN.	TYP.(1)	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC}=5.5V, V_{IN}=GND to V_{CC}	—	—	10	—	—	10	μA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ $V_{I/O}$=GND to V_{CC}	—	—	10	—	—	10	μA
I_{CC}	Operating Power Supply Current	$\overline{CS}=V_{IL}$, $I_{I/O}$=0mA	—	40	90	—	35	80	mA
I_{CC1}	Operating Power Supply Current	V_{IH}=3.5V, V_{IL}=0.6V $I_{I/O}$=0mA	—	35	—	—	30	—	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle=100%	—	40	90	—	35	80	mA
I_{SB}	Standby Power Current	$\overline{CS}=V_{IH}$	—	5	20	—	5	20	mA
I_{SB1}	Standby Power Current	$\overline{CS} \geq V_{CC}-0.2V$, $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$	—	20	2000	—	20	2000	μA
V_{OL}	Output Low Voltage	I_{OL}=4mA(2)	—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH}=−1.0mA	2.4	—	—	2.4	—	—	V

1. V_{CC}=5V, T_A=25°C
2. I_{OL}=2.1mA for IDT6116S150

IDT6116L DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V ±10%, T_A=−40°C to +85°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT6116L90/120 MIN.	TYP.(1)	MAX.	IDT6116L150 MIN.	TYP.(1)	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC}=5.5V, V_{IN}=GND to V_{CC}	—	—	2	—	—	2	μA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ $V_{I/O}$=GND to V_{CC}	—	—	2	—	—	2	μA
I_{CC}	Operating Power Supply Current	$\overline{CS}=V_{IL}$, $I_{I/O}$=0mA	—	40/35	90/80	—	30	70	mA
I_{CC1}	Operating Power Supply Current	V_{IH}=3.5V, V_{IL}=0.6V $I_{I/O}$=0mA	—	35/30	—	—	30	—	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle=100%	—	40/35	90/80	—	30	70	mA
I_{SB}	Standby Power Current	$\overline{CS}=V_{IH}$	—	5	20/15	—	4	12	mA
I_{SB1}	Standby Power Current	$\overline{CS} \geq V_{CC}-0.2V$, $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$	—	4	200	—	4	200	μA
V_{OL}	Output Low Voltage	I_{OL}=4mA(2)	—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH}=−1.0mA	2.4	—	—	2.4	—	—	V

1. V_{CC}=5V, T_A=25°C
2. I_{OL}=2.1mA for IDT6116L150

IDT6116S DC CHARACTERISTICS (V_{CC} = 5V ±10%, Gnd = 0V, T_A = 0°C to +70°C)

SYMBOL	ITEM	TEST CONDITIONS	IDT6116S 70 MIN.	TYP.(1)	MAX.	IDT6116S 90/120 MIN.	TYP.*	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}	—	—	10	—	—	10	μA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = GND to V_{CC}	—	—	10	—	—	10	μA
I_{CC}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	—	50	100	—	40	80	mA
I_{CC1}	Operating Power Supply Current	V_{IH} = 3.5V, V_{IL} = 0.6V $I_{I/O}$ = 0mA	—	40	—	—	35	—	mA
I_{CC2}	Average Operating Current	Min. Cycle Duty = 100%	—	50	100	—	40	80	mA
I_{SB}	Standby Power Current	$\overline{CS}$ = V_{IH}	—	5	15	—	5	15	mA
I_{SB1}	Standby Power Current	$\overline{CS} \geq V_{CC}-0.2V$, $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$	—	20	2000	—	20	2000	μA
V_{OL}	Output Voltage	I_{OL} = 4mA	—	—	0.4	—	—	0.4	V
V_{OH}	Output Voltage	I_{OH} = −1.0mA	2.4	—	—	2.4	—	—	V

1. V_{CC} = 5V, T_A = 25°C

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IDT6116L DC CHARACTERISTICS (V_{CC} = 5V ±10%, Gnd = 0V, T_A = 0°C to +70°C)

SYMBOL	ITEM	TEST CONDITIONS	IDT6116L 90 MIN.	TYP.[1]	MAX.	IDT6116L 120/150 MIN.	TYP.[1]	MAX.	UNIT
$\lvert I_{LI}\rvert$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}	—	—	2	—	—	2	μA
$\lvert I_{LO}\rvert$	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = GND to V_{CC}	—	—	2	—	—	2	μA
I_{CC}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	—	40	80	—	35/30	70/60	mA
I_{CC1}		V_{IH} = 3.5V, V_{IL} = 0.6V $I_{I/O}$ = 0mA	—	35	—	—	30	—	mA
I_{CC2}	Average Operating Current	Min. Cycle Duty = 100%	—	40	80	—	35/30	70/60	mA
I_{SB}	Standby Power Current	$\overline{CS}$ = V_{IH}	—	5	15	—	4	12	mA
I_{SB1}		$\overline{CS} \geq V_{CC}$ −0.2V, $V_{IN} \geq V_{CC}$ −0.2V or $V_{IN} \leq$ 0.2V	—	4	100	—	4	100	μA
V_{OL}	Output Voltage	I_{OL} = 4mA[2]	—	—	0.4	—	—	0.4	V
V_{OH}		I_{OH} = −1.0mA	2.4	—	—	2.4	—	—	V

1. V_{CC} = 5V, T_A = 25°C 2. I_{OL} = 2.1mA for IDT6116L 150

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = −55°C to +125°C/−40°C to +85°C/0°C to +70°C)[1]

SYMBOL	PARAMETER	IDT616S70[2] MIN.	MAX.	IDT6116S90 IDT6116L90 MIN.	MAX.	IDT6116S120 IDT6116L120 MIN.	MAX.	IDT6116S150 IDS6116L150 MIN.	MAX.	UNIT
READ CYCLE										
t_{RC}	Read Access Time	70	—	90	—	120	—	150	—	ns
t_{AA}	Address Access Time	—	70	—	90	—	120	—	150	ns
t_{ACS}	Chip Select Access Time	—	70	—	90	—	120	—	150	ns
t_{CLZ}	Chip Selection to Output in Low Z	5	—	0/0/5	—	5/5/10	—	10/15[3]	—	ns
t_{OE}	Output Enable to Output Valid	—	50	—	65	—	80	—	100	ns
t_{OLZ}	Output Enable to Output in Low Z	5	—	0/0/5	—	5/5/10	—	10/15[3]	—	ns
t_{CHZ}	Chip Deselection to Output in High Z	0	35	0	40	0	40	0	50	ns
t_{OHZ}	Output Disable to Output in High Z	0	35	0	40	0	40	0	50	ns
t_{OH}	Output Hold from Address Change	5	—	0/0/5	—	5/5/10	—	10/15[3]	—	na
WRITE CYCLE										
t_{WC}	Write Cycle Time	70	—	90	—	120	—	150	—	ns
t_{CW}	Chip Selection to End of Write	40	—	55	—	70	—	90	—	ns
t_{AW}	Address Valid to End of Write	65	—	80	—	105	—	120	—	ns
t_{AS}	Address Setup Time	15	—	15	—	20	—	20	—	ns
t_{WP}	Write Pulse Width	40	—	55	—	70	—	90	—	ns
t_{WR}	Write Recovery Time	5	—	10/5/5	—	10/5/5	—	10	—	ns
t_{OHZ}	Output Disable to Output in High Z	0	35	0	40	0	40	0	50	ns
t_{WHZ}	Write to Output in High Z	0	40	0	50	0	50	0	60	ns
t_{DW}	Data to Write Time Overlap	30	—	30	—	35	—	40	—	ns
t_{DH}	Data Hold from Write Time	5	—	10/10/5	—	10/10/5	—	10	—	ns
t_{OW}	Output Active from End of Write	0	—	0	—	0/5/5	—	5/10[4]	—	ns

1. Parameters listing three limits apply in this Temp. Range order: Military/Industrial/Commercial. All other limits apply to all three Temp. Ranges.
2. IDT6116S70 available in Commercial 0°C to 70°C only.
3. 10ns applies over −55°C to +125°C and −40°C to +85°C; 15ns applies over 0°C to +70°C.
4. t_{OW} = 5ns over −55°C to +125°C; t_{OW} = 10ns over −40°C to +85°C and 0°C to +70°C.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	1 TTL Gate and C_L=100pF (including scope and jig)

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TRUTH TABLE

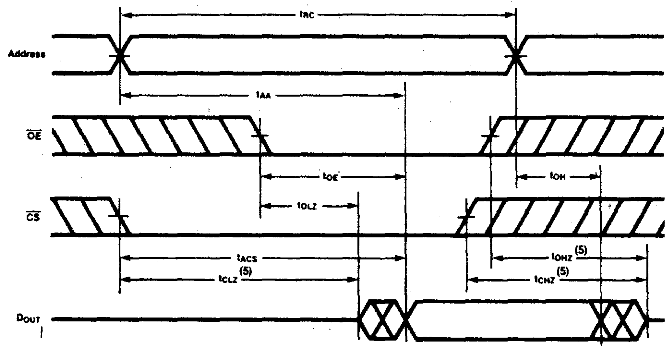
MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O OPERATION
Standby	H	X	X	High Z
Read	L	L	H	D_{OUT}
Read	L	H	H	High Z
Write	L	X	L	D_{IN}

CAPACITANCE(1) ($T_A = 25°C$, f = 1.0 MHz)

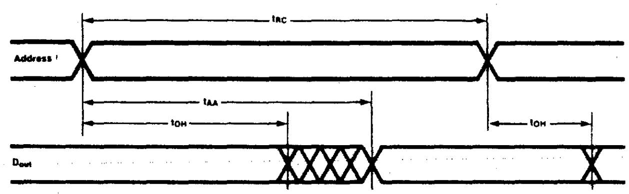
SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O} = 0V$	8	pF

1. This parameter is sampled and not 100% tested.

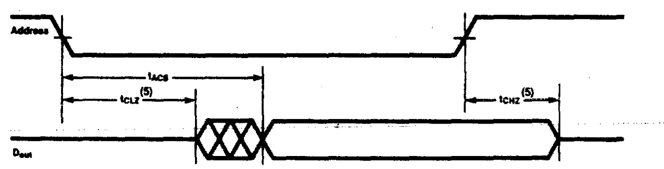
TIMING WAVEFORMS OF READ CYCLE NO. 1(1)



READ CYCLE 2(1,2,4)

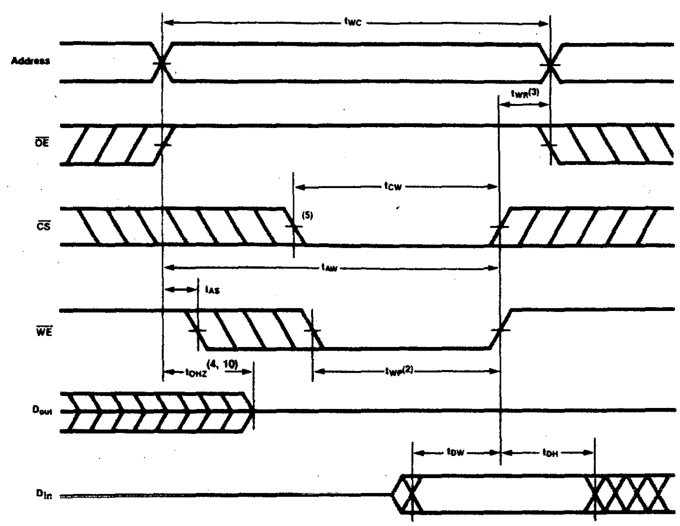


READ CYCLE 3(1,3,4)



NOTES: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORMS OF WRITE CYCLE 1(1)



NOTE: See footnotes on next page.

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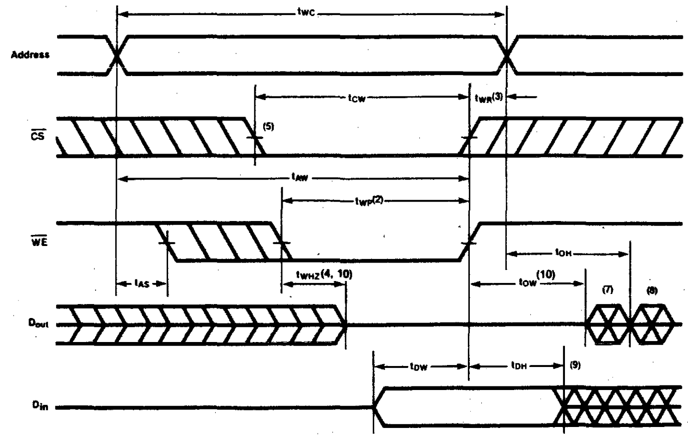
TIMING WAVEFORM OF WRITE CYCLE 2[1,6]



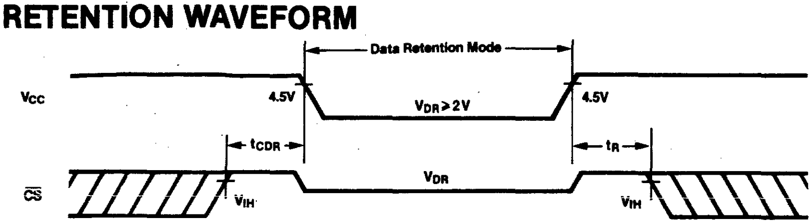
NOTES: 1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{CE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

DATA RETENTION CHARACTERISTICS
($T_A = -55°C$ to $+125°C/-40°C$ to $+85°C/0°C$ to $70°C$)

SYMBOL	PARAMETER	TEST CONDITIONS		IDT6116L MIN.	TYP.[1]	MAX.	IDT6116S MIN.	TYP.[1]	MAX.	UNIT
V_{DR}	V_{CC} for Retention Data			2.0	—	—	2.0	—	—	V
I_{CCDR}	Data Retention Current	$V_{CC} = 2.0V$, $\overline{CS} \geq V_{CC} - 0.2V$	COM'L	—	0.5	20	—	2	400	μA
		$V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	IND	—	0.5	40	—	2	600	μA
			MIL	—	0.5	300	—	2	1000	μA
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	0	—	—	ns
t_R	Operation Recovery Time			t_{RC}(2)	—	—	t_{RC}(2)	—	—	ns

1. $V_{CC} = 2V$, $T_A = +25°C$
2. t_{RC} = Read Cycle Time

LOW V_{CC} DATA RETENTION WAVEFORM



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Integrated Device Technology, Inc. reserves the right to make changes to the specifications in this data sheet in order to improve design or performance and to supply the best possible product.

CMOS STATIC RAMS 16K (16K×1 BIT)

IDT6167S IDT6167L

Integrated Device Technology, Inc

MILITARY / INDUSTRIAL / COMMERCIAL TEMPERATURE RANGES

FEATURES:

- High-speed (equal access and cycle time)
  - —MILITARY/INDUSTRIAL
    IDT6167S 55/70/85/100ns (max.)
    IDT6167L 55/70/85/100ns (max.)
  - —COMMERCIAL
    IDT6167S 45/55/70/85ns (max.)
    IDT6167L 45/55/70/85ns (max.)
- Low power consumption

IDT6167S	IDT6167L
Active: 150mW (typ.)	Active: 125mW (typ.)
Standby: 100μW (typ.)	Standby: 10μW (typ.)

- Battery backup operation — 2V data retention voltage (IDT6167L only)
- High-density 20-pin dual-in-line package and 20-pin leadless chip carriers
- Produced with advanced CEMOS™ I high-performance technology
- CEMOS™ I process virtually eliminates alpha particle soft-error rates (with no organic die coatings)
- Separate data input and output
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Pin-compatible with standard 16K×1 static RAMs
- Standard product 100% screened to MIL-STD-883 Class C
- Military product available 100% screened to Class B

DESCRIPTION:

The IDT6167 is a 16,384-bit high-speed static RAM organized as 16K×1. It is fabricated using IDT's high-performance, high-reliability technology — CEMOS™ I. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories.

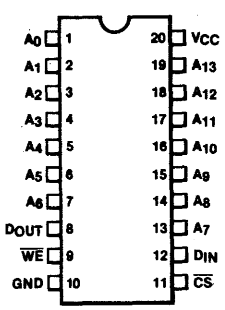
Access times as fast as 45ns are available with maximum power consumption of only 330mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{CS}$ remains high. In the standby mode, the device consumes less than 100μW, typically. This capability provides significant system-level power and cooling savings. The low power, (L), version also offers a battery backup data retention capability where the circuit typically consumes only 1μW operating off of a 2V battery.

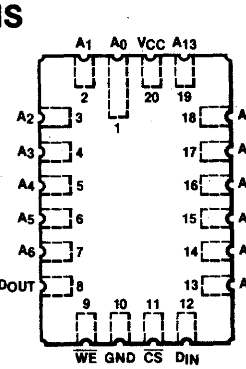
All inputs and the output of the IDT6167 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

The IDT6167 is packaged in either a space-saving 20-pin, 300 mil DIP, a 20-pin leadless chip carrier, or 20-pin flatpack providing high board-level packing densities.

The IDT6167 Military RAM is 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

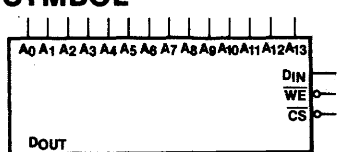
PIN CONFIGURATIONS



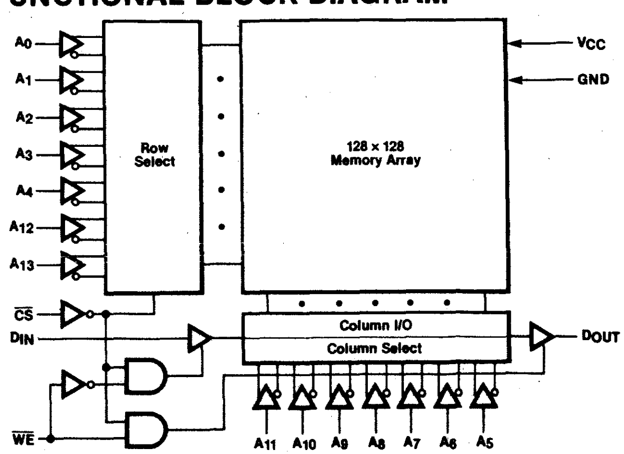


LCC Top View

LOGIC SYMBOL



FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_0–A_{13}	ADDRESS INPUTS	D_{IN}	DATA IN
$\overline{CS}$	CHIP SELECT	D_{OUT}	DATA OUT
$\overline{WE}$	WRITE ENABLE	GND	GROUND
V_{CC}	POWER		

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MEMORY

ABSOLUTE MAXIMUM RATINGS[1]

TEMPERATURE RANGE		−55°C to +125°	−40°C to +85°C	0°C to +70°C	
SYMBOL	RATING	VALUE			UNIT
V_{TERM}	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	−0.5 to +7.0	V
T_A	Operating Temperature	−55 to +125	−40 to +85	0 to +70	°C
T_{BIAS}	Temperature Under Bias	−65 to +135	−55 to +125	−10 to +85	°C
T_{STG}	Storage Temperature	−65 to +150	−65 to +150	−55 to +125	°C
P_T	Power Dissipation	1.0	1.0	1.0	W
I_{OUT}	DC Output Current	20	20	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS
(T_A = −55°C to +125°C/−40°C to +85°C/0°C to +70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	−0.5*	—	0.8	V

* V_{IL} min. = −3.5V for pulse widths less than 30ns and duty cycles less than 50%.

MILITARY (T_A = −55°C to +125°C)

INDUSTRIAL (T_A = −40°C to +85°C)

COMMERCIAL (T_A = 0°C to +70°C)

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = −55°C to +125°C/−40°C to +85°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT6167S MIN.	IDT6167S TYP.[1]	IDT6167S MAX.	IDT6167L MIN.	IDT6167L TYP.[1]	IDT6167L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	—	10	—	—	5/2	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	—	10	—	—	5/2	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Output Open	—	30	60	—	25	50	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100%	—	30	60	—	25	50	mA
I_{SB}	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$	—	5	20	—	5	20	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS} \geq V_{CC}$ −0.2V $V_{IN} \geq V_{CC}$ −0.2V or ≤ 0.2V	—	20	10,000/ 2000	—	2	900/ 150	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA	—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4mA	2.4	—	—	2.4	—	—	V

1. V_{CC} = 5V, T_A = 25°C

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0 to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT6167S MIN.	IDT6167S TYP.[1]	IDT6167S MAX.	IDT6167L MIN.	IDT6167L TYP.[1]	IDT6167L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	—	2	—	—	2	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	—	2	—	—	2	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Output Open	—	30	60	—	25	50	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100%	—	30	60	—	25	50	mA
I_{SB}	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$	—	5	20	—	5	20	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS} \geq V_{CC}$ −0.2V $V_{IN} \geq V_{CC}$ −0.2V or ≤ 0.2V	—	20	2000	—	2	50	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA	—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4mA	2.4	—	—	2.4	—	—	V

1. V_{CC} = 5V, T_A = 25°C

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D Out	Active
Write	L	L	High Z	Active

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

SYMBOL	ITEM	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	6	pF

NOTE: This parameter is sampled and not 100% tested.

Integrated Device Technology MEMORY

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = −55°C to +125°C/−40°C to +85°C unless otherwise noted.)

SYMBOL		PARAMETER	IDT6167S55 IDT6167L55 MIN.	MAX.	IDT6167S70 IDT6167L70 MIN.	MAX.	IDT6167S85 IDT6167L85 MIN.	MAX.	IDT6167S100 IDT6167L100 MIN.	MAX.	UNIT
READ CYCLE											
t_{RC}	(TAVAV)	Read Cycle Time	55	—	70	—	85	—	100	—	ns
t_{AA}	(TAVQV)	Address Access Time	—	55	—	70	—	85	—	100	ns
t_{ACS}	(TELQV)	Chip Select Access Time	—	55	—	70	—	85	—	100	ns
t_{OH}	(TAXQX)	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{LZ}	(TELQX)	Chip Selection to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{HZ}	(TEHQZ)	Chip Deselection to Output in High Z	0	40	0	40	0	50	0	50	ns
t_{PU}	(TELICCH)	Chip Selection to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}	(TEHICCL)	Chip Deselection to Power Down Time	—	55	—	70	—	85	—	100	ns
WRITE CYCLE											
t_{WC}	(TAVAV)	Write Cycle Time	55	—	70	—	85	—	100	—	ns
t_{CW}	(TELWH)	Chip Selection to End of Write	45	—	55	—	65	—	80	—	ns
t_{AW}	(TAVWH)	Address Valid to End of Write	45	—	55	—	65	—	80	—	ns
t_{AS}	(TAVWL)	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{WP}	(TWLWH)	Write Pulse Width	35	—	40	—	45	—	55	—	ns
t_{WR}	(TWHAX)	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	(TDVWH)	Data Valid to End of Write	25	—	30	—	35	—	40	—	ns
t_{DH}	(TWHDX)	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{WZ}	(TWLQZ)	Write Enable to Output in High Z	0	40	0	40	0	50	0	50	ns
t_{OW}	(TWHQX)	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C) unless otherwise noted.)

SYMBOL		PARAMETER	IDT6167S45 IDT6167L45 MIN.	MAX.	IDT6167S55 IDT6167L55 MIN.	MAX.	IDT6167S70 IDT6167L70 MIN.	MAX.	IDT6167S85 IDT6167L85 MIN.	MAX.	UNIT
READ CYCLE											
t_{RC}	(TAVAV)	Read Cycle Time	45	—	55	—	70	—	85	—	ns
t_{AA}	(TAVQV)	Address Access Time	—	45	—	55	—	70	—	85	ns
t_{ACS}	(TELQV)	Chip Select Access Time	—	45	—	55	—	70	—	85	ns
t_{OH}	(TAXQX)	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{LZ}	(TELQX)	Chip Selection to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{HZ}	(TEHQZ)	Chip Deselection to Output in High Z	0	30	0	30	0	30	0	40	ns
t_{PU}	(TELICCH)	Chip Selection to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}	(TEHICCL)	Chip Deselection to Power Down Time	—	35	—	35	—	35	—	40	ns
WRITE CYCLE											
t_{WC}	(TAVAV)	Write Cycle Time	45	—	55	—	70	—	85	—	ns
t_{CW}	(TELWH)	Chip Selection to End of Write	40	—	45	—	55	—	65	—	ns
t_{AW}	(TAVWH)	Address Valid to End of Write	40	—	45	—	55	—	65	—	ns
t_{AS}	(TAVWL)	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{WP}	(TWLWH)	Write Pulse Width	30	—	35	—	40	—	45	—	ns
t_{WR}	(TWHAX)	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	(TDVWH)	Data Valid to End of Write	25	—	25	—	30	—	35	—	ns
t_{DH}	(TWHDX)	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{WZ}	(TWLQZ)	Write Enable to Output in High Z	0	30	0	30	0	30	0	40	ns
t_{OW}	(TWHQX)	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

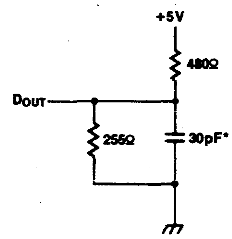


Figure 1. Output Load

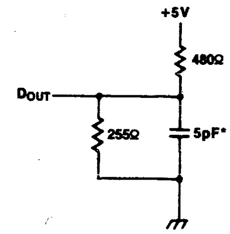
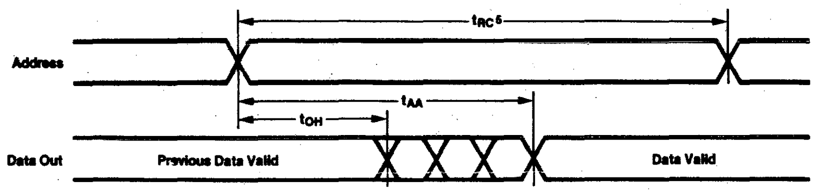


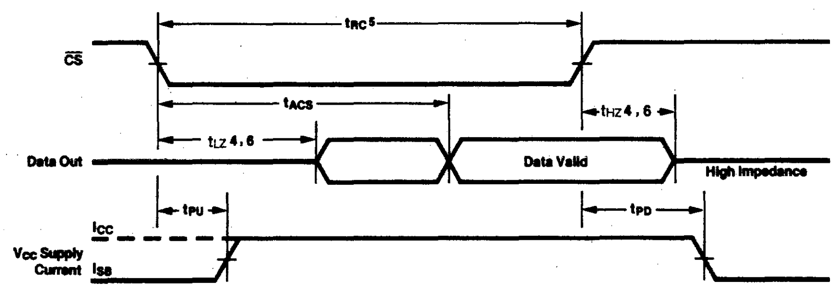
Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

***Including scope and jig.**

TIMING WAVEFORM OF READ CYCLE NO. 1[1,2]

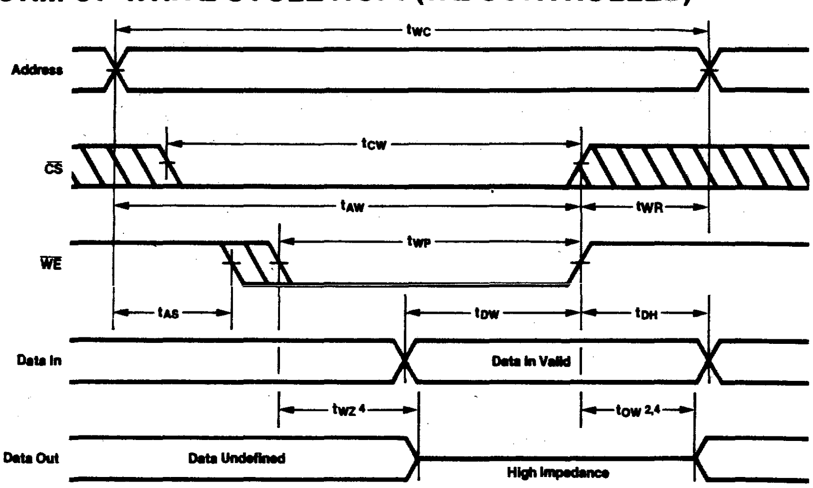


TIMING WAVEFORM OF READ CYCLE NO. 2[1,3]



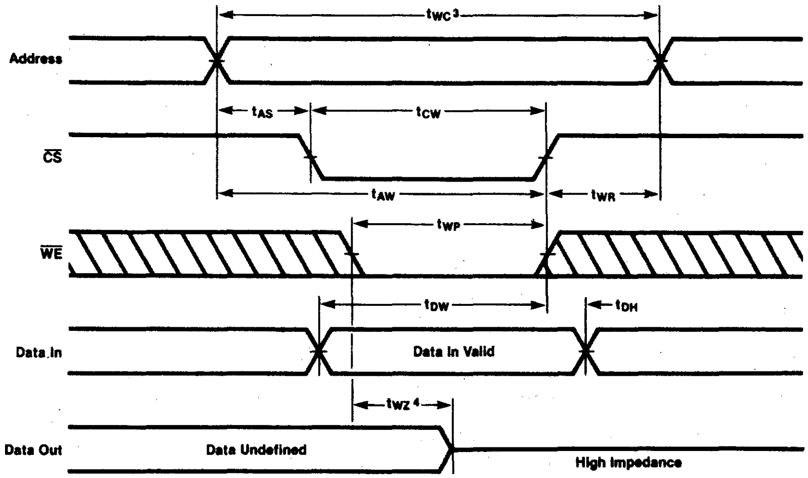
NOTES: 1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2. This parameter is sampled, not 100% tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. For any given speed grade, operating voltage and temperature, t_{HZ} will be less than or equal to t_{LZ}.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[1]



NOTES: 1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)[1]



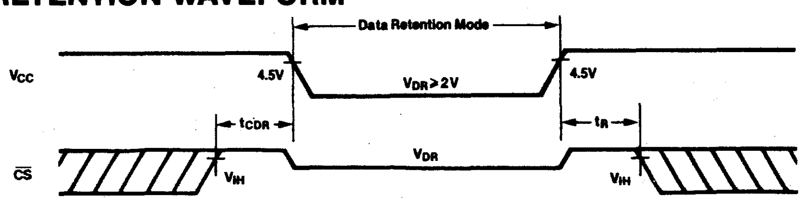
NOTES: 1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.

LOW V_{CC} DATA RETENTION CHARACTERISTICS FOR L VERSION ONLY (T_A = −55°C to +125°C/−40°C to +85°C/0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.[1]	MAX.	UNIT
V_{DR}	V_{CC} for Data Retention			2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC}$ −0.2V $V_{IN} \geq V_{CC}$ −0.2V or $\leq$ 0.2V	COM'L	— —	0.5[2] 1.0[3]	20[2] 30[2]	μA
			IND	—	0.5[2] 1.0[3]	40[2] 60[3]	
			MIL	— —	0.5[2] 1.0[3]	300[2] 450[3]	
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	ns
t_R	Operation Recovery Time			t_{RC}[4]	—	—	ns

NOTES: 1. T_A = 25°C
2. at V_{CC} = 2V
3. at V_{CC} = 3V
4. t_{RC} = Read Cycle Time

LOW V_{CC} DATA RETENTION WAVEFORM



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Integrated Device Technology, Inc

CMOS STATIC RAMS
16K (4K x 4 BIT)

IDT6168S/L
IDT71681S/L
IDT71682S/L

MILITARY / INDUSTRIAL / COMMERCIAL TEMPERATURE RANGES

FEATURES:

- High-speed (equal access and cycle time)
  IDT6168S/IDT6168L 45 (com'l)/55/70/85/100 ns (max.)
  IDT71681S/IDT71681L 45 (com'l)/55/70/85/100 ns (max.)
  IDT71682S/IDT71682L 45 (com'l)/55/70/85/100 ns (max.)
- Low power consumption
  — IDT6168S/IDT71681S/IDT71682S
  Active: 225 mW (typ.)
  Standby: 100 μW (typ.)
  — IDT6168L/IDT71681L/IDT71682L
  Active: 225 mW (typ.)
  Standby: 10 μW (typ.)
- Bidirectional data input and output (IDT6168 only)
- Separate data inputs and outputs (IDT71681 and IDT71682 only)
- Outputs in high impedance in WRITE mode (IDT71682 only)
- Battery backup operation — 2V data retention voltage (L versions only)
- Produced with advanced CEMOS™ I high-performance technology
- CEMOS I process virtually eliminates alpha particle soft-error rates (with no organic die coatings)
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Standard product 100% screened to MIL-STD-883 Class C
- Military product available 100% screened to Class B

DESCRIPTION:

The IDT6168, IDT71681 and IDT71682 are 16,384-bit high-speed static RAMs organized as 4K x 4. They are fabricated using IDT's high-performance, high-reliability technology — CEMOS™ I. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories.

The IDT71681 and IDT71682 are manufactured with separate data inputs and outputs. This feature allows for improved system architectures. The external latches of a bidirectional bus system are not needed, improving both board density and system power levels. The absence of bus contention allows a streamlined approach, enhancing system speeds. Also, they fit readily into a pipeline structure.

Access times as fast as 45 ns are available with maximum power consumption of only 495 mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{CS}$ remains high. In the standby mode, the device consumes less than 100 μW, typically. This capability provides significant system-level power and cooling savings. The low power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 1 μW operating off a 2V battery.

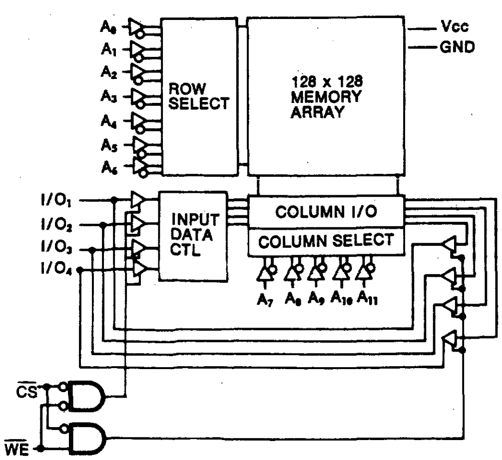
All inputs and outputs of the IDT6168, IDT71681 and IDT71682 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

The IDT6168 is packaged in either a space-saving 20-pin, 300 mil DIP, a 20-pin leadless chip carrier or a 20-pin flatpack and the IDT71681 and IDT71682 in a 24-pin, 300 mil DIP or a 28-pin leadless chip carrier, providing high board-level packing densities.

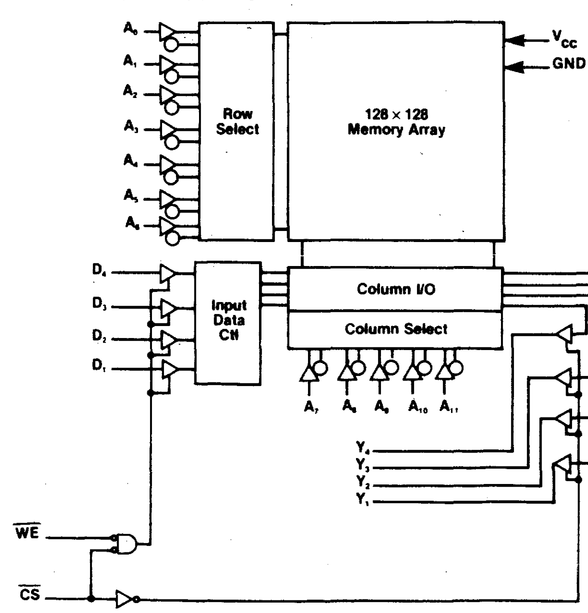
The Military RAMs are 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAMS

IDT6168



IDT71681



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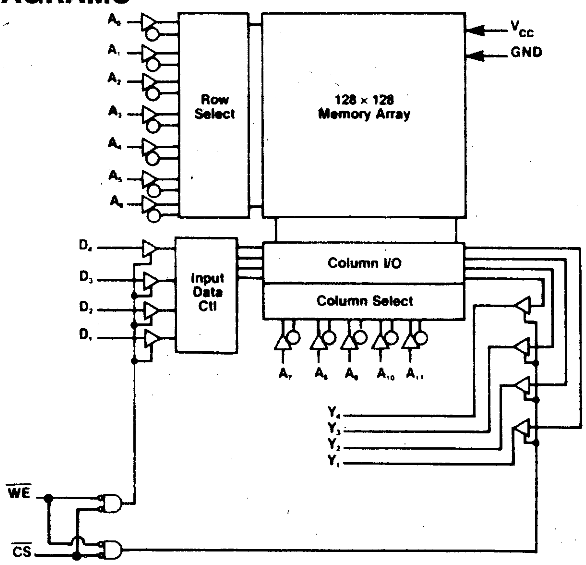
Integrated Device Technology

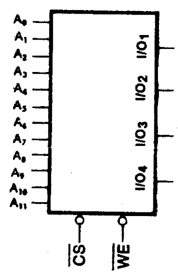
MEMORY

FUNCTIONAL BLOCK DIAGRAMS

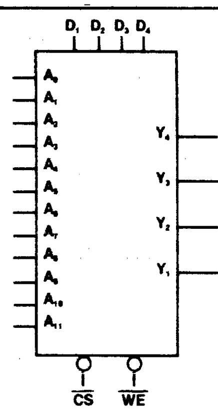
IDT71682



LOGIC SYMBOLS

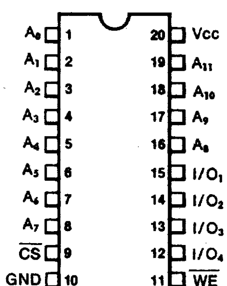


(IDT6168)

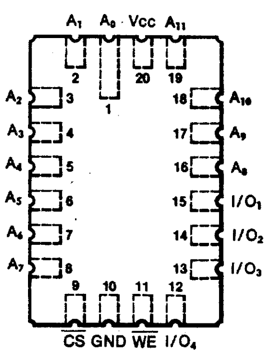


(IDT71681 & IDT71682)

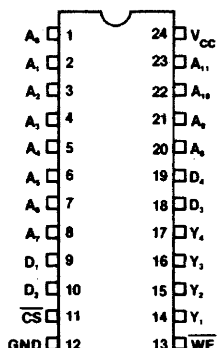
PIN CONFIGURATIONS



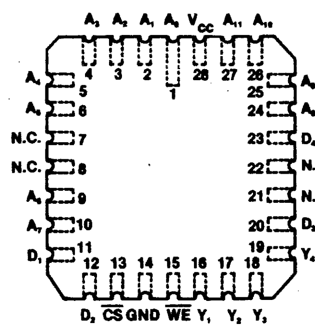
DIP
Top View
(IDT6168)



LCC
Top View
(IDT6168)



DIP
Top View
(IDT71681
IDT71682)



LCC
Top View
(IDT71681
IDT71682)

PIN NAMES

(IDT6168)

A_0-A_{11}	ADDRESS INPUTS	I/O_1-I/O_4	DATA INPUT/OUTPUT
$\overline{CS}$	CHIP SELECT	Vcc	POWER
$\overline{WE}$	WRITE ENABLE	GND	GROUND

(IDT71681 & IDT71682)

A_0-A_{11}	ADDRESS INPUTS	D_1-D_4	DATA IN
$\overline{CS}$	CHIP SELECT	Y_1-Y_4	DATA OUT
$\overline{WE}$	WRITE ENABLE	GND	GROUND
V_{CC}	POWER		

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ABSOLUTE MAXIMUM RATINGS[1]

TEMPERATURE RANGE		−55°C to +125°C	−40°C to +85°	0°C to +70°C	
SYMBOL	PARAMETER	RATING			UNIT
V_{TERM}	Voltage on any Pin with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	−0.5 to +7.0	V
T_A	Operating Temperature	−55 to +125	−40 to +85	0 to +70	°C
T_{BIAS}	Temperature Under Bias	−65 to +135	−55 to +125	−10 to +85	°C
T_{STG}	Storage Temperature	−65 to +150	−65 to +150	−55 to +125	°C
P_T	Power Dissipation	1.0	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	50	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	−1.0*	—	+0.8	V

MILITARY (T_A = −55°C to +125°C)
INDUSTRIAL (T_A = −40°C to +85°C)
COMMERCIAL (T_A = 0°C to +70°C)

* V_{IL} min. = −3.5V for pulse widths less than 30 ns and duty cycles less than 50%.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = −55°C to +125°C/−40°C to +85°C/0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT6168S/71681S MIN.	TYP.[1]	MAX.	IDT6168L/71681L MIN.	TYP.[1]	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	—	10/10/2	—	—	5/2/2	μA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	—	10/10/2	—	—	5/2/2	μA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Output Open	—	45	90	—	45	90	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100%	—	45	90	—	45	90	mA
I_{SB}	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$	—	5	20	—	5	20	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS} \geq V_{CC}$ − 0.2V $V_{IN} \geq V_{CC}$ − 0.2V or ≤ 0.2V	—	20	10,000/ 2000/2000	—	2	900/ 150/50	μA
V_{OL}	Output Low Voltage	I_{OL} = 8mA	—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4mA	2.4	—	—	2.4	—	—	V

1. V_{CC} = 5V, T_A = 25°C

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D Out	Active
Write	L	L	High Z	Active

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

SYMBOL	ITEM	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: This parameter is sampled and not 100% tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

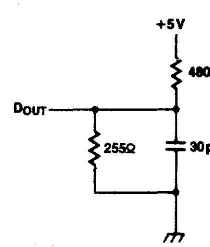

Figure 1. Output Load

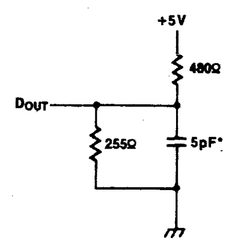

Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

***Including scope and jig.**

AC CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = −55°C to +125°C/−40°C to +85°C/0°C to +70°C unless otherwise noted.)[1]

SYMBOL	PARAMETER	IDT6168S45[2] IDT6168L45 MIN.	MAX.	IDT6168S55 IDT6168L55 MIN.	MAX.	IDT6168S70 IDT6168L70 MIN.	MAX.	IDT6168S85 IDT6168L85 MIN.	MAX.	IDT6168S100[3] IDT6168L100 MIN.	MAX.	UNIT
READ CYCLE												
t_{RC} (TAVAV)	Read Cycle Time	45	—	55	—	70	—	85	—	100	—	ns
t_{AA} (TAVQV)	Address Access Time	—	45	—	55	—	70	—	85	—	100	ns
t_{ACS} (TELQV)	Chip Select Access Time	—	45	—	55	—	70	—	85	—	100	ns
t_{OH} (TAXQX)	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t_{LZ} (TELQX)	Chip Selection to Output in Low Z	20	—	20	—	20	—	20	—	20	—	ns
t_{HZ} (TEHQZ)	Chip Deselection to Output in High Z	—	20	—	25	—	30/30/25	—	40/40/25	—	50	ns
t_{PU} (TELICCH)	Chip Selection to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD} (TEHICCL)	Chip Deselection to Power Down Time	—	40	—	55/55/50	—	70/70/60	—	85/85/70	—	100	ns
t_{RCS}	Read Command Set-Up Time	−5	—	−5	—	−5	—	−5	—	−5	—	ns
t_{RCH}	Read Command Hold Time	−5	—	−5	—	−5	—	−5	—	−5	—	ns
WRITE CYCLE												
t_{WC} (TAVAV)	Write Cycle Time	40	—	50	—	60	—	75	—	90	—	ns
t_{CW} (TELWH)	Chip Selection to End of Write	35	—	50/50/45	—	60/60/55	—	75/75/65	—	90	—	ns
t_{AW} (TAVWH)	Address Valid to End of Write	35	—	50/50/45	—	60/60/55	—	75/75/65	—	90	—	ns
t_{AS} (TAVWL)	Address Setup Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP} (TWLWH)	Write Pulse Width	35	—	50/50/45	—	60/60/55	—	75/75/70	—	90	—	ns
t_{WR} (TWHAX)	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{DW} (TDVWH)	Data Valid to End of Write	15	—	25/25/20	—	30/30/25	—	35/35/30	—	40	—	ns
t_{DH} (TWHDX)	Data Hold Time	3	—	5/5/3	—	5/5/3	—	5/5/3	—	5	—	ns
t_{WZ} (TWLQZ)	Write Enable to Output in High Z	—	20	—	25	—	30	—	40	—	50	ns
t_{OW} (TWHQX)	Output Active from End of Write	10	40	0/0/10	40/40/50	0/0/10	50/50/60	0/0/10	60/60/70	0	70	ns

AC CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = −55°C to +125°C/−40°C to +85°C/0°C to +70°C unless otherwise noted.)[1]

SYMBOL	PARAMETER	IDT7168145[2] IDT7168245 MIN.	MAX.	IDT7168155 IDT7168255 MIN.	MAX.	IDT7168170 IDT7168270 MIN.	MAX.	IDT7168185 IDT7168285 MIN.	MAX.	IDT71681100[3] IDT71682100 MIN.	MAX.	UNIT
READ CYCLE												
t_{RC} (TAVAV)	Read Cycle Time	45	—	55	—	70	—	85	—	100	—	ns
t_{AA} (TAVQV)	Address Access Time	—	45	—	55	—	70	—	85	—	100	ns
t_{ACS} (TELQV)	Chip Select Access Time	—	45	—	55	—	70	—	85	—	100	ns
t_{OH} (TAXQX)	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t_{LZ} (TELQX)	Chip Selection to Output in Low Z	20	—	20	—	20	—	20	—	20	—	ns
t_{HZ} (TEHQZ)	Chip Deselection to Output in High Z	—	20	—	25	—	30	—	40	—	50	ns
t_{PU} (TELICCH)	Chip Selection to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD} (TEHICCL)	Chip Deselection to Power Down Time	—	40	—	55/55/50	—	70/70/60	—	85/85/70	—	100	ns
t_{RCS}	Read Command Set-Up Time	−5	—	−5	—	−5	—	−5	—	−5	—	ns
t_{RCH}	Read Command Hold Time	−5	—	−5	—	−5	—	−5	—	−5	—	ns
WRITE CYCLE												
t_{WC} (TAVAV)	Write Cycle Time	40	—	45/45/50	—	55/55/60	—	65/65/70	—	80	—	ns
t_{CW} (TELWH)	Chip Selection to End of Write	35	—	45	—	55	—	65	—	80	—	ns
t_{AW} (TAVWH)	Address Valid to End of Write	35	—	45	—	55	—	65	—	80	—	ns
t_{AS} (TAVWL)	Address Setup Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP} (TWLWH)	Write Pulse Width	30	—	35	—	40	—	45	—	55	—	ns
t_{WR} (TWHAX)	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{DW} (TDVWH)	Data Valid to End of Write	15	—	25/25/20	—	30/30/25	—	35/35/30	—	40	—	ns
t_{DH} (TWHDX)	Data Hold Time	3	—	5/5/3	—	5/5/3	—	5/5/3	—	5	—	ns
t_{LY} (TDVQV)	Data Valid to Output Valid (71681 only)	—	35	—	35/35/40	—	40/40/45	—	45/45/50	—	50	ns
t_{WY} (TWLQV)	Write Enable to Output Valid (71681 only)	—	35	—	35/35/40	—	40/40/45	—	45/45/50	—	50	ns
t_{WZ} (TWLQZ)	Write Enable to Output in High Z (71682 only)	—	—	—	25	—	30	—	40	—	50	ns
t_{OW} (TWHQX)	Output Active from End of Write (71682 only)	—	—	0	40	0	50	0	60	0	70	ns

(1) Parameters listing three limits apply in this Temp. Range order: Military/Industrial/Commercial. All other limits apply to all three Temp. Ranges.
(2) Available in Commercial 0°C to +70°C only.
(3) Available in Military −55°C to +125°C and Industrial −40°C to +85°C only.

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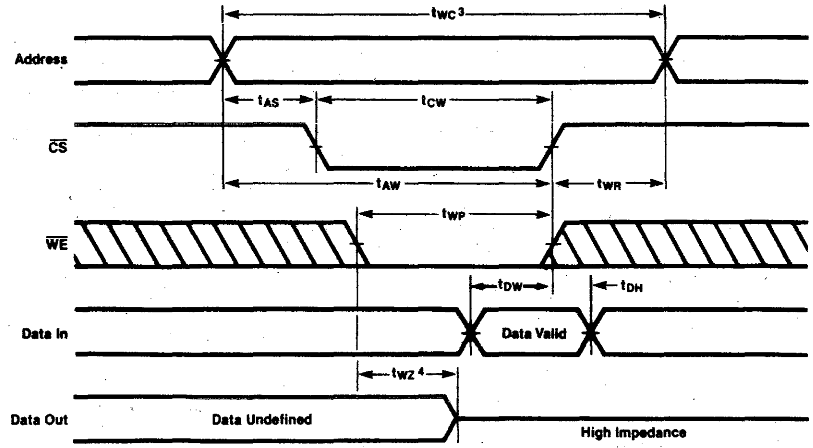
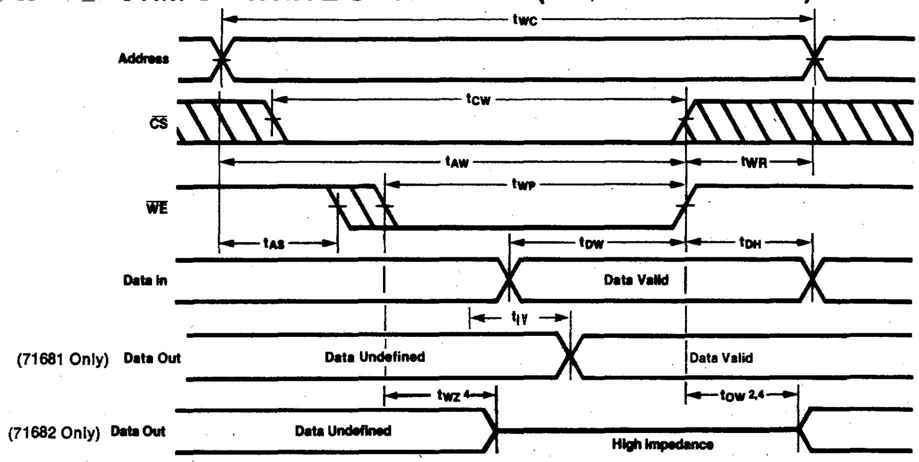
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)[1] For IDT6168

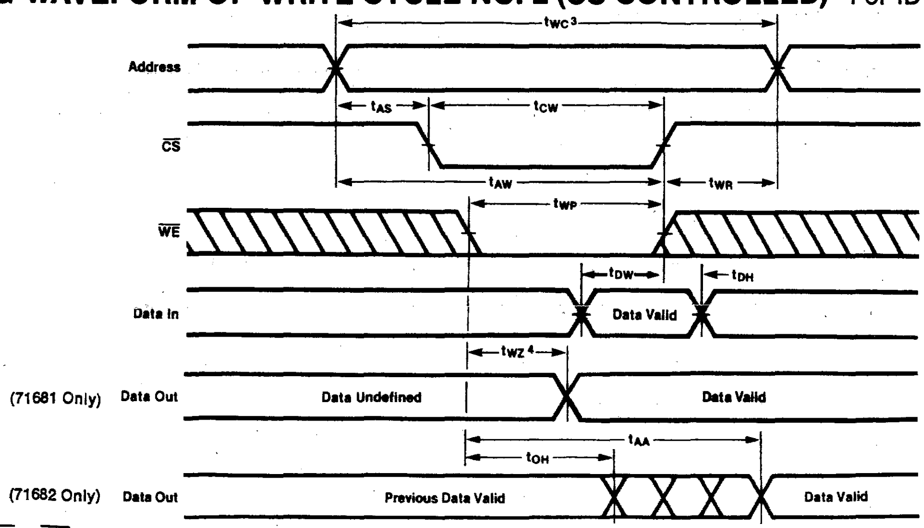


NOTES: 1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[1] For IDT71681 and IDT71682



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)[1] For IDT71681 and IDT71682



NOTES: 1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.

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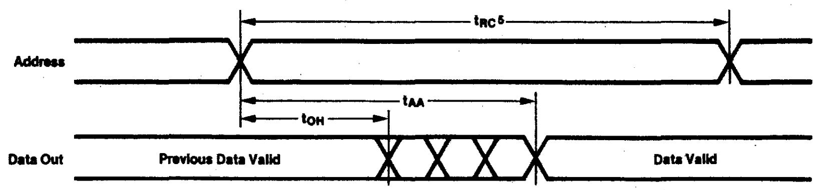
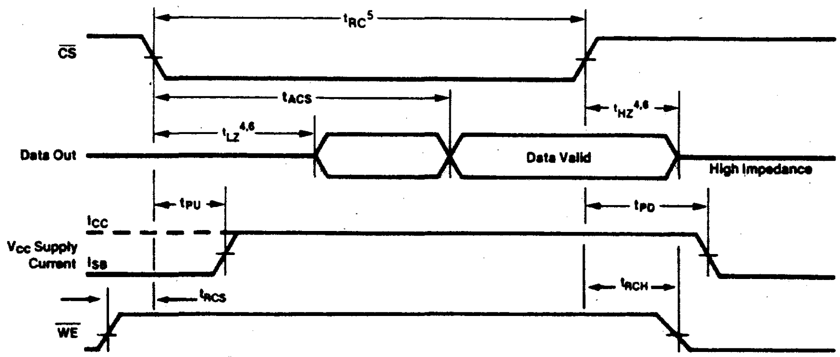
TIMING WAVEFORM OF READ CYCLE NO. 1[1,2] For IDT6168 and IDT71681 and IDT71682

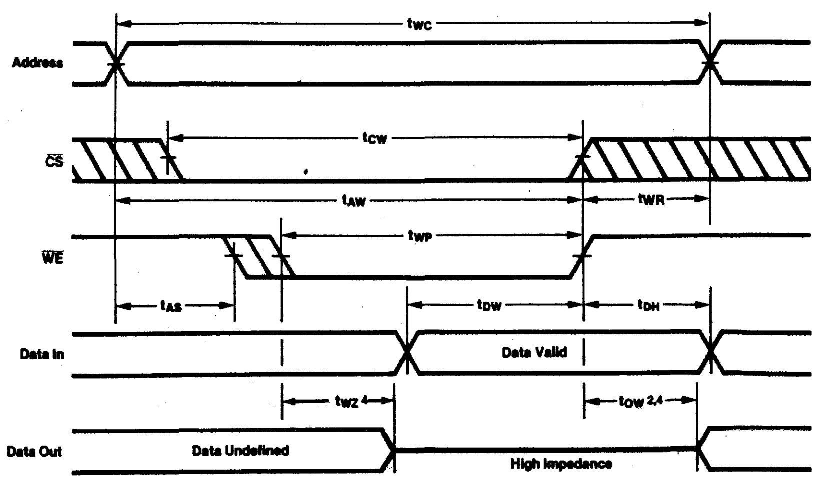


TIMING WAVEFORM OF READ CYCLE NO. 2[1,3] For IDT6168 and IDT71681 and IDT71682



NOTES:
1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2. This parameter is sampled, not 100% tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. For any given speed grade, operating voltage and temperature, t_{HZ} will be less than or equal to t_{LZ}.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[1] For IDT6168



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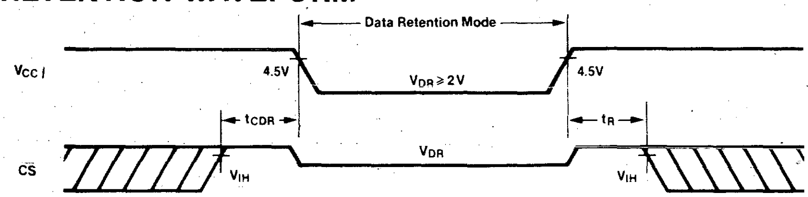
LOW V_{CC} DATA RETENTION CHARACTERISTICS ($T_A = -55°C$ to $+125°C$/ $-40°C$ to $+85°C$/$0°C$ to $+70°C$)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.[1]	MAX.	UNIT
V_{DR}	V_{CC} for Data Retention			2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC} -0.2V$ $V_{IN} \geq V_{CC} -0.2V$ or $\leq 0.2V$	COM'L	— —	0.5(2) 1.0(3)	20(2) 30(2)	μA
			IND	—	0.5(2) 1.0(3)	40(2) 60(3)	
			MIL	— —	0.5(2) 1.0(3)	300(2) 450(3)	
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	ns
t_R	Operation Recovery Time			t_{RC}(4)	—	—	ns

NOTES: 1. $T_A = 25°C$
2. at $V_{CC} = 2V$
3. at $V_{CC} = 3V$
4. t_{RC} = Read Cycle Time

LOW V_{CC} DATA RETENTION WAVEFORM



Integrated Device Technology

MEMORY

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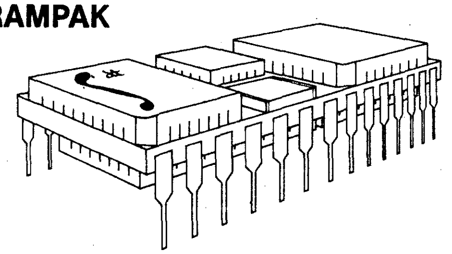
Integrated Device Technology, Inc

64K (8K x 8) CMOS STATIC RAMPAK

IDT7M864 IDT8M864

MILITARY / COMMERCIAL TEMPERATURE RANGES

64K RAMPAK



FEATURES:

- 8,192 x 8 static RAM module complete with decoder and decoupling capacitor
- High-speed 85 (commercial only)/120/150/200ns (equal access and cycle times)
- Low power consumption; 300 mW typ.
- Two pinout options (64K EPROM & 64K static RAM)
- Utilizes IDT6116s — high performance 16K RAMs produced with advanced CEMOS™ I technology
- CEMOS I process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (± 10%) power supply
- Input and output directly TTL-compatible
- Static operation: no clock or refresh required
- Standard military components 100% screened to MIL-STD-883 Class C
- Military components available 100% screened to Class B

DESCRIPTION:

The IDT7M864/IDT8M864 are 64K (8,192 x 8 bit) high speed static RAMs constructed on a ceramic substrate using 4 IDT6116 (2,048 x 8) static RAMs in leadless chip carriers. Functional equivalence to a monolithic 64K static RAM is achieved by utilization of an on-board decoder circuit that interprets the higher order addresses A_{11} and A_{12} to select one of the four 2Kx8 RAMs. Extremely fast speeds can be achieved with this technique due to use of the IDT6116 fabricated in IDT's high performance, high-reliability technology - CEMOS I. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 16K static RAMs available.

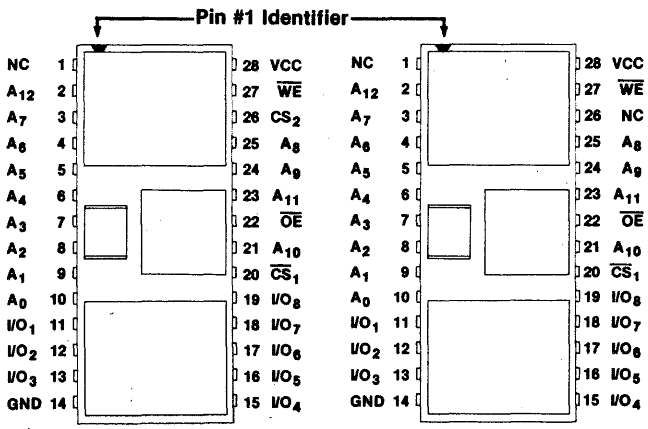
The IDT7M864/IDT8M864 are available with access times as fast as 85ns for commercial and 120ns for military temperature ranges, with maximum power consumption of only 825mW. The circuit also offers a reduced power standby mode. When $\overline{CS}_1$ goes high, and/or CS_2 (7M864) goes low, the circuit will automatically go to, and remain in, a standby mode as long as these conditions are held. In the standby mode, the module consumes less than 275mW. Substantially lower power levels can be achieved in the ISB_1 mode (less than 25mW max.) and 2V data retention mode (less than 3mW max.) - see "DC Characteristics" and "Data Retention Characteristics" for details.

Pinout of the IDT8M864 is equivalent to the 64K EPROMs (no connect on pin 26), ideal for applications requiring easy microcode changes during prototyping. The IDT7M864's pinout is compatible with monolithic 64K static RAMs (CS_2 on pin 26).

All inputs and outputs of the IDT7M864/IDT8M864 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Full asyncronous circuitry is used, requiring no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

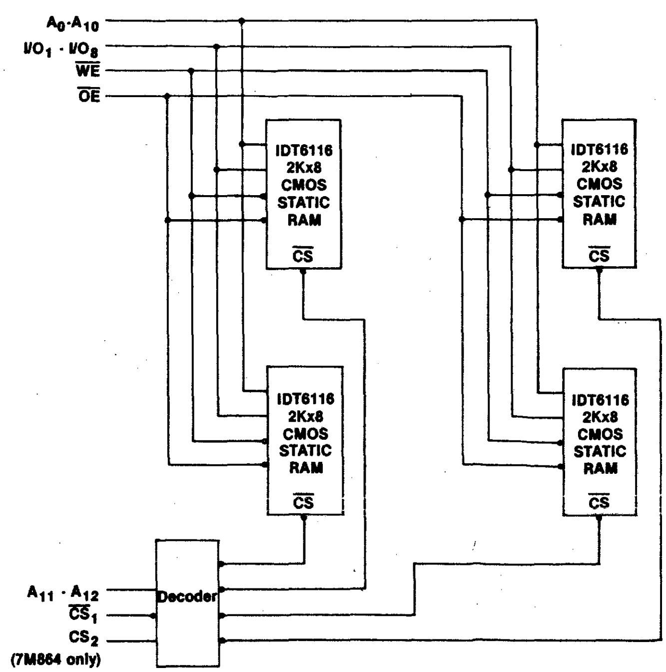
All IDT military module components are 100% processed to the test methods of MIL-STD-883, Method 5004, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS



7M864 8M864

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_0-A_{12}	ADDRESS	$\overline{WE}$	WRITE ENABLE
I/O_1-I/O_8	DATA INPUT/OUTPUT	$\overline{OE}$	OUTPUT ENABLE
$\overline{CS}_1$, CS_2	CHIP SELECT	GND	GROUND
V_{CC}	POWER		

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TRUTH TABLE

MODE	$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	I/O OPERATION
Standby	H	X	X	X	High Z
Standby	X	L	X	X	High Z
Read	L	H	L	H	D_{OUT}
Read	L	H	H	H	High Z
Write	L	H	X	L	D_{IN}

RECOMMENDED DC OPERATING CONDITIONS

(T_A = −55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	−0.5 *	—	.65	V
C_L	Output Load	—	—	100	pF
TTL	Output Load	—	—	1	—

* V_{IL} min. = −3.5V for pulse widths less than 30 ns and duty cycles less than 50%.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = −55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7M864/8M864 MIN.	TYP.[1]	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	—	15	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{OE}$ or $\overline{CS_1}$ ≥ V_{IH}, or CS_2 ≤ V_{IL}, V_{OUT} = 0V to V_{CC}	—	—	15	µA
I_{CC}	Operating Power Supply Current	$\overline{CS_1}$ ≤ V_{IL}, CS_2 ≥ V_{IH}, Output Open	—	65	150	mA
I_{CC1}	Dynamic Operating Current	Min. Duty Cycle = 100%	—	65	150	mA
I_{SB}	Standby Power Supply Current	$\overline{CS_1}$ ≥ V_{IH}, or CS_2 ≤ V_{IL}	—	20	50	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS_1}$ ≥ V_{CC} − 0.2V, and/or CS_2 ≤ 0.2V V_{IN} ≥ V_{CC} − 0.2V or ≤ 0.2V	—	15	1200	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −1mA	2.4	—	—	V

1. V_{CC} = 5V, T_A = 25°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−10 to +85	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	4.0	4.0	W
I_{OUT}	DC Output Current	50	50	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	10ns
Input and Output Timing Reference Levels	1.5V
Output Load	1 TTL Gate and C_L = 100pF (including scope and jig)

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

SYMBOL	ITEM	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	22	pF

NOTE: This parameter is sampled and not 100% tested.

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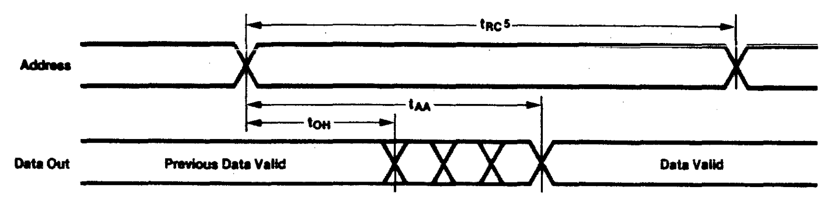
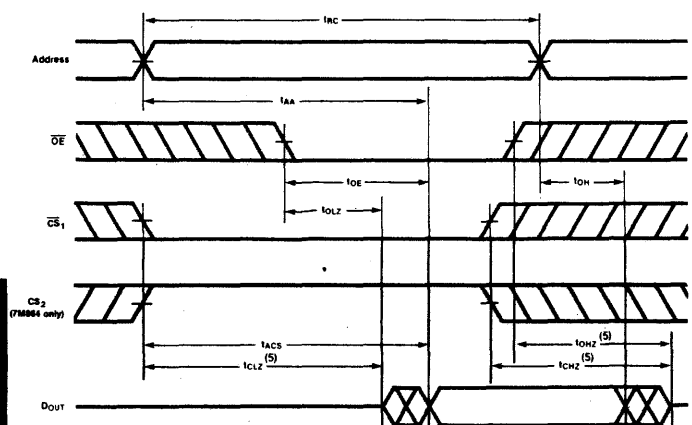
AC ELECTRICAL CHARACTERISTICS (V_{CC}=5V ± 10%, T_A= −55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	7M/8M864L85 COMMERCIAL ONLY MIN.	MAX.	7M/8M864L120 MIN.	MAX.	7M/8M864L150 MIN.	MAX.	7M/8M864L200 MIN.	MAX.	UNIT
READ CYCLE										
t_{RC}	Read Cycle Time	85	—	120	—	150	—	200	—	ns
t_{AA}	Address Access Time	—	85	—	120	—	150	—	200	ns
t_{ACS}	Chip Select Access Time	—	85	—	120	—	150	—	200	ns
t_{CLZ}	Chip Selection to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	65	—	65	—	80	—	100	ns
t_{OLZ}	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	ns
t_{CHZ}	Chip Deselection to Output in High Z	—	55	—	70	—	70	—	80	ns
t_{OHZ}	Output Disable to Output in High Z	—	40	—	40	—	40	—	50	ns
t_{OH}	Output Hold from Address Change	0	—	0	—	0	—	0	—	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	85	—	120	—	150	—	200	—	ns
t_{CW}	Chip Selection to End of Write	65	—	80	—	100	—	120	—	ns
t_{AW}	Address Valid to End of Write	70	—	85	—	100	—	120	—	ns
t_{AS}	Address Setup Time	15	—	15	—	20	—	20	—	ns
t_{WP}	Write Pulse Width	55	—	55	—	70	—	90	—	ns
t_{WR}	Write Recovery Time	10	—	10	—	10	—	10	—	ns
t_{OHZ}	Output Disable to Output in High Z	—	40	—	40	—	40	—	50	ns
t_{WHZ}	Write to Output in High Z	0	50	0	50	0	60	0	60	ns
t_{DW}	Data to Write Time Overlap	30	—	30	—	35	—	40	—	ns
t_{DH}	Data Hold from Write Time	10	—	10	—	10	—	10	—	ns
t_{OW}	Output Active from End of Write	0	—	0	—	0	—	5	—	ns

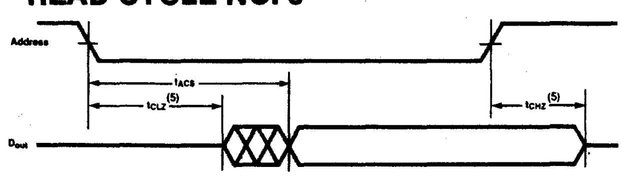
TIMING WAVEFORM OF READ CYCLE NO. 1[1,2]



TIMING WAVEFORM OF READ CYCLE NO. 2[1,3]

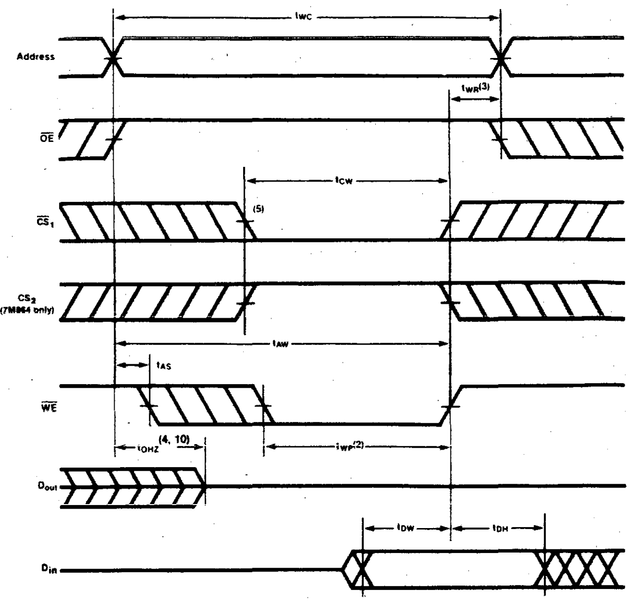


TIMING WAVEFORM OF READ CYCLE NO. 3[1,3,4]

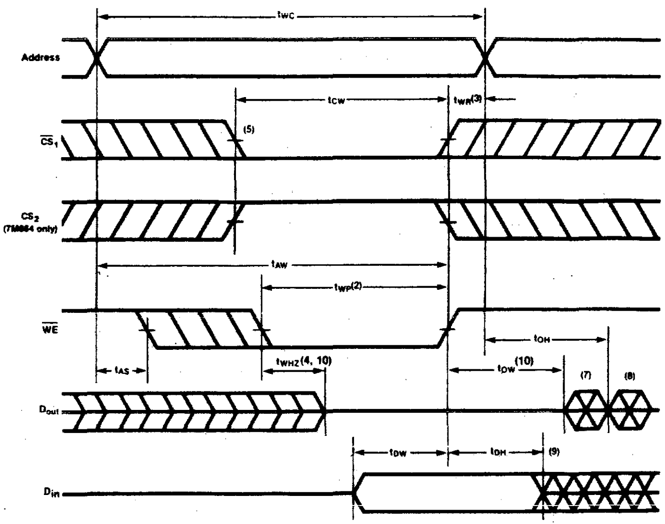


NOTES: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}_1$ = V_{IL}, CS_2 = V_{IH} (7M864 only).
3. Address valid prior to or coincident with $\overline{CS}_1$ transition low, CS_2 transition high (7M864 only).
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE 1(1)



TIMING WAVEFORM OF WRITE CYCLE 2(1,6)



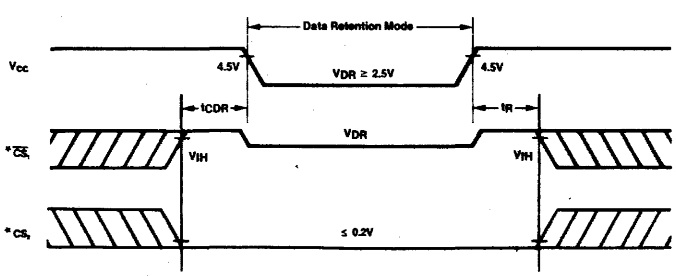
NOTES: 1. $\overline{WE}$ is high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}_1$, or high CS_2 (7M864 only) and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}_1$ or $\overline{WE}$ going high or CS_2 going low to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}_1$ low transition or CS_2 high transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS}_1$ is low or CS_2 is high during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_A = −55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.(1)	MAX COMM.	MAX. MIL.	UNIT
V_{DR}	V_{CC} for Data Retention		2.5	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS}_1 \geq V_{CC} - 0.2V$, $CS_2 \leq 0.2V$	— —	2.0(2) 4.0(3)	80(2) 120(3)	850(2) 1000(3)	μA
t_{CDR}	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	0	—	—	—	ns
t_R	Operation Recovery Time		t_{RC}(4)	—	—	—	ns

NOTES: 1. $T_A = 25°C$ 3. at $V_{CC} = 3V$
2. at $V_{CC} = 2.5V$ 4. t_{RC} = Read Cycle Time

LOW V_{CC} DATA RETENTION WAVEFORM



*Low V_{CC} data retention achieved by the indicated $\overline{CS}_1$ waveform or CS_2 waveform.

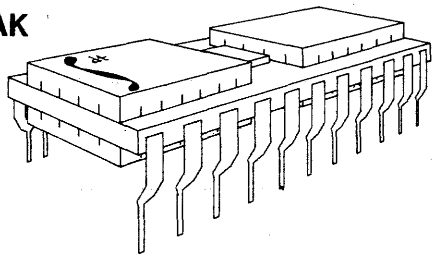
Integrated Device Technology, Inc.

64K (16K x 4) CMOS STATIC RAMPAK

IDT7M464

MILITARY / COMMERCIAL TEMPERATURE RANGES

64K RAMPAK



FEATURES:

- 65,536x1 bit static RAM module complete with decoder and decoupling capacitor
- High-speed 70 (commercial only)/100/120/150ns (equal access and cycle times)
- Low power consumption; 250mW typically
- Offered in a 22 pin, 300 mil center sidebraze DIP
- Pin compatible with proposed monolithics
- Utilizes IDT6167s — high performance 16K RAMs produced with advanced CEMOS™I technology
- CEMOS I process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (± 10%) power supply
- Input and output directly TTL-compatible
- Static operation: no clock or refresh required
- Standard military components 100% screened to MIL-STD-883 Class C
- Military components available 100% screened to Class B

DESCRIPTION:

The IDT7M464 is a 64K (16,384 x 4 bit) high speed CMOS static RAM constructed on a ceramic substrate using 4 IDT6167 (16,384 x 1 bit) CMOS static RAMs in leadless chip carriers. Functional equivalence to proposed monolithic 16Kx4 static RAMS is achieved by utilization of tungsten traces within the substrate to connect the four 16K RAMs in a 16Kx4 configuration. Extremely fast speeds can be achieved with this technique due to use of the IDT6167 fabricated in IDT's high-performance, high-reliability technology — CEMOS™I. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 16K static RAMs available.

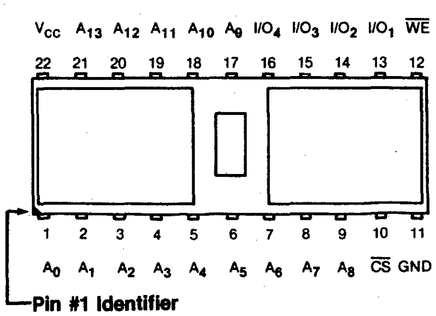
The IDT7M464 is available with access times as fast as 55ns for commercial and 65ns for military temperature ranges, with maximum power consumption of only 1.1 watt. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{CS}$ remains high, consuming only 300mW maximum. Substantially lower power levels can be achieved in the I_{SB1} mode (less than 6mW max.) and 2V data retention mode (less than 2mW max.) - see "DC Characteristics" and "Data Retention Characteristics" for details.

The IDT7M464 is offered in a space saving 22-pin, 300 mil pin center package, providing equivalent pinout to the proposed monolithic 16Kx4 static RAMs.

All inputs and outputs of the IDT7M464 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Full asyncronous circuitry is used, requiring no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

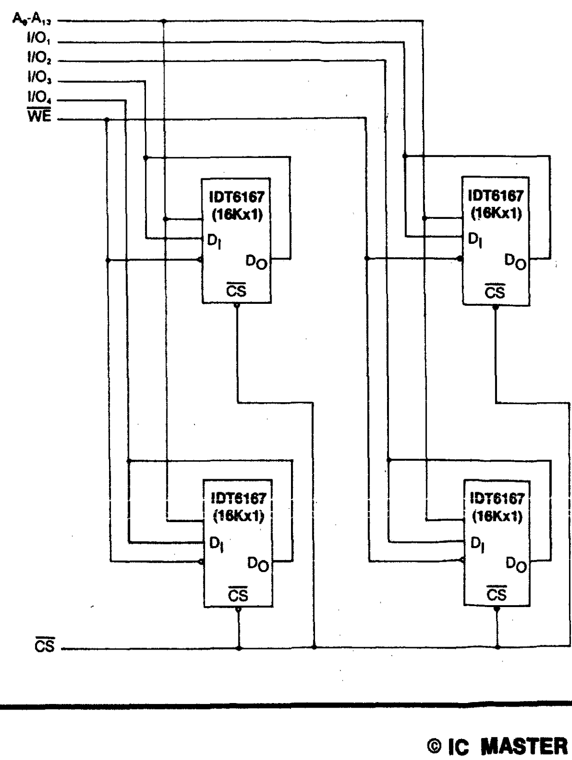
All IDT military module components are 100% processed to the test methods of MIL-STD-883, Method 5004, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



7M464
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_0–A_{13}	ADDRESS	$\overline{WE}$	WRITE ENABLE
I/O_1–I/O_4	DATA INPUT/OUTPUT	V_{CC}	POWER
$\overline{CS}$	CHIP SELECT	GND	GROUND

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TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D Out	Active
Write	L	L	High Z	Active

RECOMMENDED DC OPERATING CONDITIONS

($T_A = -55°C$ to $+125°C$ and $0°C$ to $+70°C$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	−0.5 *	—	+0.8	V

* V_{IL} min. = −3.5V for pulse widths less than 30 ns and duty cycles less than 50%.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, $T_A = -55°C$ to $+125°C$ and $0°C$ to $+70°C$)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7M164 MIN.	TYP.[1]	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	$V_{CC} = 5.5V$, $V_{IN} = 0V$ to V_{CC}	—	—	15	μA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS} = V_{IH}$, $V_{OUT} = 0V$ to V_{CC}	—	—	15	μA
I_{CC1}	Operating Power Supply Current	$\overline{CS} = V_{IL}$, Output Open	—	100	195	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100%	—	100	195	mA
I_{SB}	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$	—	20	55	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	—	8	1000[2]	μA
V_{OL}	Output Low Voltage	$I_{OL} = 8mA$	—	—	0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -4mA$	2.4	—	—	V

1. $V_{CC} = 5V$, $T_A = 25°C$
2. I_{SB1} max at commercial temperature = 0.2mA

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−10 to +85	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	4.0	4.0	W
I_{OUT}	DC Output Current	50	50	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE ($T_A = 25°C$, f = 1.0MHz)

SYMBOL	ITEM	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0V$	20	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	22	pF

NOTE: This parameter is sampled and not 100% tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

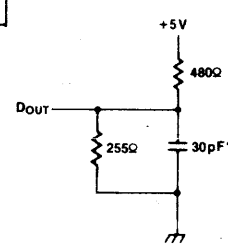

Figure 1. Output Load

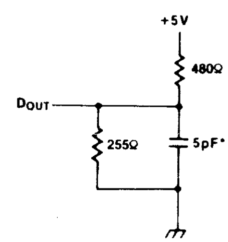

Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

*Including scope and jig.

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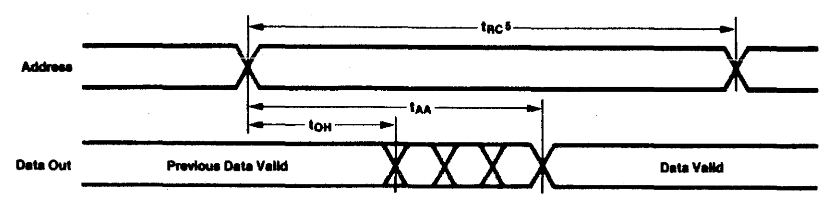
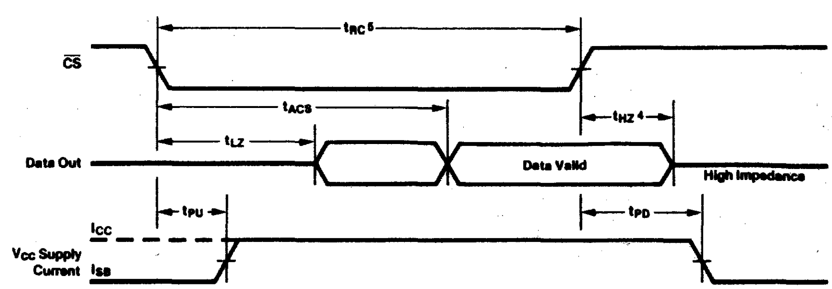
AC ELECTRICAL CHARACTERISTICS (V_{CC}=5V ± 10%, T_A= −55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	7M464S55 COMMERCIAL ONLY MIN.	MAX.	7M464S65 MIN.	MAX.	7M464S85 MIN.	MAX.	7M464S100 MILITARY ONLY MIN.	MAX.	UNIT
READ CYCLE										
t_{RC}	Read Cycle Time	55	—	65	—	85	—	100	—	ns
t_{AA}	Address Access Time	—	55	—	65	—	85	—	100	ns
t_{ACS}	Chip Select Access Time	—	55	—	65	—	85	—	100	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{LZ}	Chip Selection to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{HZ}	Chip Deselection to Output in High Z	0	40	0	40	0	50	0	50	ns
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Deselection to Power Down Time	—	55	—	65	—	85	—	100	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	55	—	65	—	85	—	100	—	ns
t_{CW}	Chip Selection to End of Write	45	—	55	—	65	—	80	—	ns
t_{AW}	Address Valid to End of Write	45	—	55	—	65	—	80	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	35	—	40	—	45	—	55	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	25	—	30	—	35	—	40	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High Z	0	40	0	40	0	50	0	50	ns
t_{OW}	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

TIMING WAVEFORM OF READ CYCLE NO. 1[1,2]



TIMING WAVEFORM OF READ CYCLE NO. 2[1,3]



NOTES: 1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2. This parameter is sampled, not 100% tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

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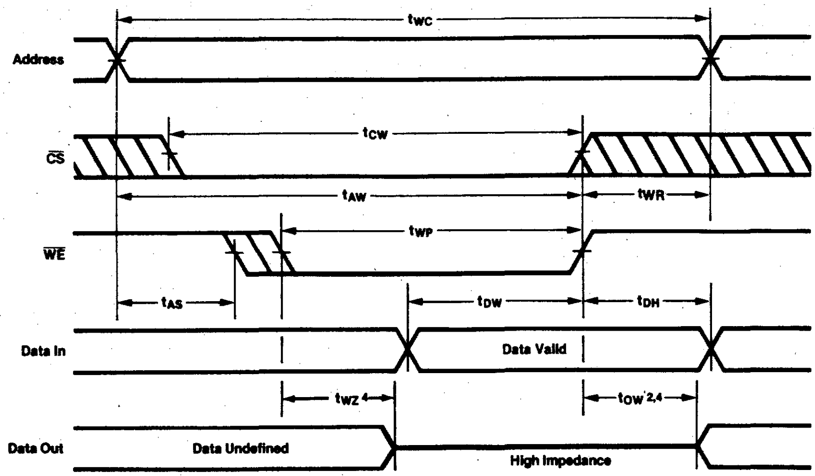
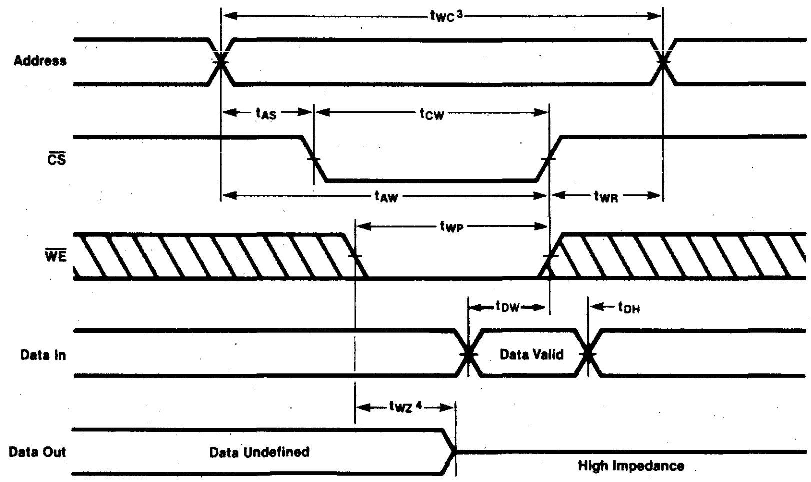
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[1]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)[1]



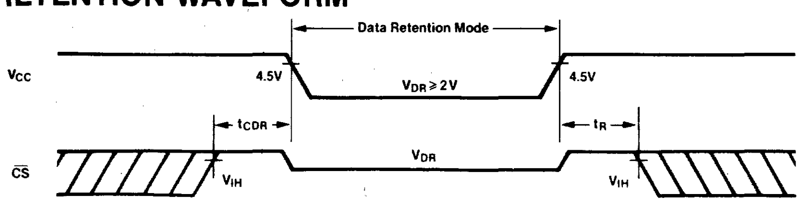
NOTES: 1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.

LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_A = −55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.[1]	MAX COMM.	MAX. MIL.	UNIT
V_{DR}	V_{CC} for Data Retention		2.0	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC}$ −0.2V $V_{IN} \geq V_{CC}$ −0.2V or ≤ 0.2V	— —	2.0[2] 4.0[3]	80[2] 120[3]	850[2] 1000[3]	μA
t_{CDR}	Chip Deselect to Data Retention Time		15	—	—	—	ns
t_R	Operation Recovery Time		t_{RC}[4]	—	—	—	ns

NOTES: 1. T_A = 25°C 3. at V_{CC} = 3V
2. at V_{CC} = 2V 4. t_{RC} = Read Cycle Time

LOW V_{CC} DATA RETENTION WAVEFORM

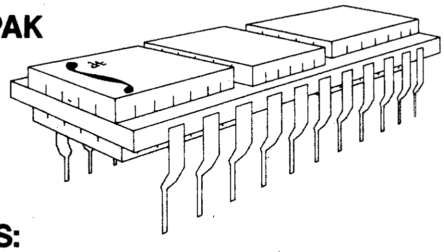


Integrated Device Technology, Inc

64K (64K × 1) CMOS STATIC RAMPAK

IDT7M164
PRELIMINARY

64K RAMPAK



FEATURES:

- 65,536 bit CMOS static RAM module with decoupling capacitor
- High-speed: 55/65/85ns max. commercial
  65/85/100ns max. military
- Low power consumption: 1.1W max.
- Pinout identical to proposed monolithic 64Kx1 static RAMs
- Utilizes IDT6167s — high performance 16K RAMs produced with advanced CEMOS™I technology
- CEMOS I process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (± 10%) power supply
- Input and output directly TTL-compatible
- Static operation: no clock or refresh required
- Standard military components 100% screened to MIL-STD-883 Class C
- Military components available 100% screened to Class B

DESCRIPTION:

The IDT7M164 is a 64K (65,536x1 bit) high speed static RAM constructed on a ceramic substrate using 4 IDT6167 (16Kx1) static RAMs in leadless chip carriers. Functional equivalence to proposed monolithic 64Kx1 static RAMs is achieved by utilization of an on-board decoder circuit that interprets the higher order addresses A_{14} and A_{15} to select one of the four 16Kx1 RAMs. Extremely fast speeds can be achieved with this technique due to use of the IDT6167 fabricated in IDT's high performance, high-reliability technology — CEMOS™I. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 16K static RAMs available.

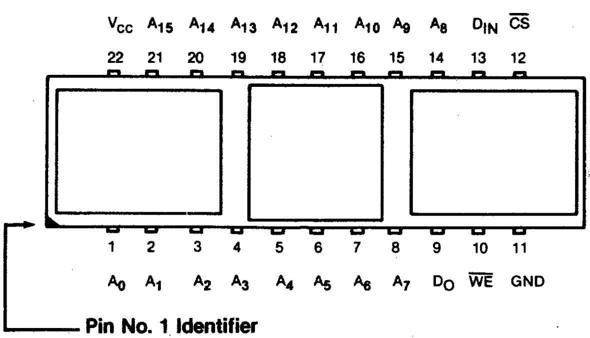
The IDT7M164 is available with access times as fast as 70ns for commercial and 100ns for military temperature ranges, with maximum power consumption of only 660mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby mode as long as this condition is held. In the standby mode, the module typically consumes less than 100 mW. Substantially lower power levels can be achieved in the ISB_1 mode (less than 50 μW typ.) and 2V data retention mode (less than 4 μW typ.) - see "DC Characteristics" and "Data Retention Characteristics" for details.

The IDT7M164 is offered in a space saving 22-pin, 300 mil pin center package, providing equivalent pinout to the proposed monolithic 64Kx1 static RAMs.

All inputs and outputs of the IDT7M164 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Full asyncronous circuitry is used, requiring no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

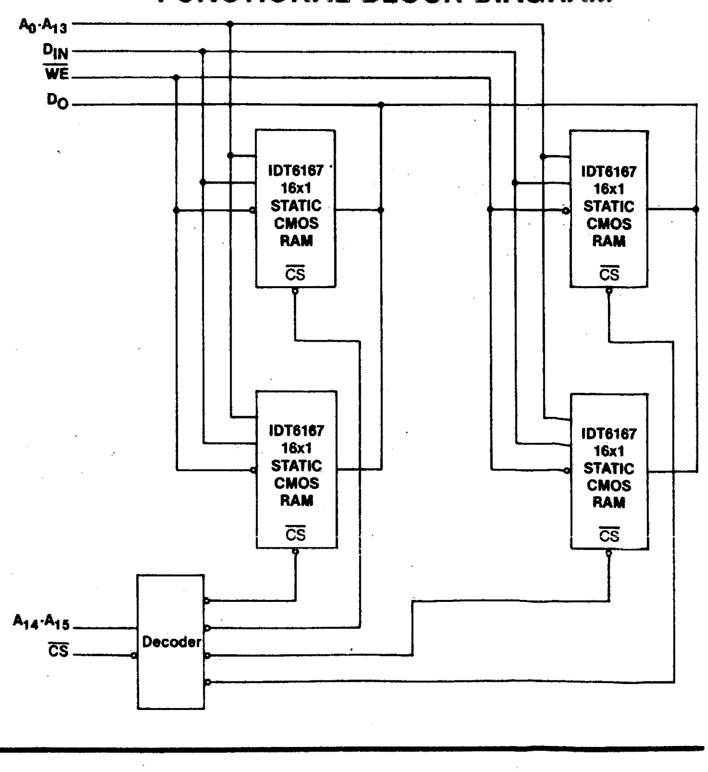
All IDT military module components are 100% processed to the test methods of MIL-STD-883, Method 5004, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



IDT7M164
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_0-A_{15}	ADDRESS	$\overline{WE}$	WRITE ENABLE
D_{IN}	DATA INPUT	D_O	DATA OUTPUT
$\overline{CS}$	CHIP SELECT	GND	GROUND
V_{CC}	POWER		

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D Out	Active
Write	L	L	High Z	Active

RECOMMENDED DC OPERATING CONDITIONS
(T_A = −55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	−0.5 *	—	+0.8	V

* V_{IL} min. = −3.5V for pulse widths less than 30 ns and duty cycles less than 50%.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = −55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7M164 MIN.	TYP.(1)	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	—	20	μA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS} = V_{IH}$, V_{OUT} = 0V to V_{CC}	—	—	20	μA
I_{CC1}	Operating Power Supply Current	$\overline{CS} = V_{IL}$, Output Open	—	50	120	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100%	—	50	120	mA
I_{SB}	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$	—	20	80	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS} \geq V_{CC}$ − 0.2V $V_{IN} \geq V_{CC}$ − 0.2V or ≤ 0.2V	—	0.008	3.5(2)	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4mA	2.4	—	—	V

1. V_{CC} = 5V, T_A = 25°C
2. I_{SB1} max at commercial temperature = 0.2mA

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−10 to +85	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	4.0	4.0	W
I_{OUT}	DC Output Current	50	50	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

SYMBOL	ITEM	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	22	pF

NOTE: This parameter is sampled and not 100% tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

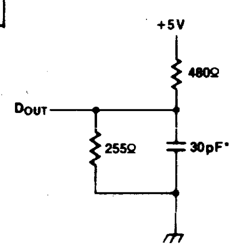


Figure 1. Output Load

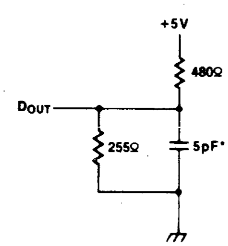


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

*Including scope and jig.

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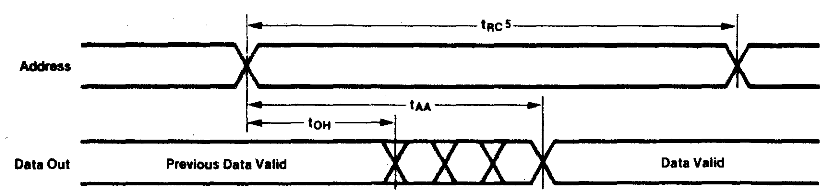
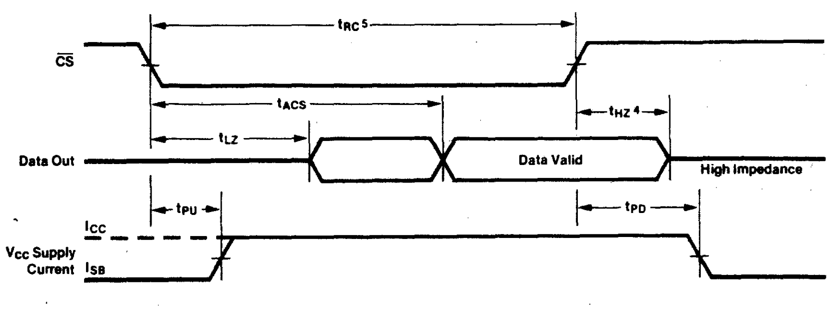
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = −55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	COMMERCIAL ONLY MIN.	COMMERCIAL ONLY MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT
READ CYCLE										
t_{RC}	Read Cycle Time	70	—	100	—	120	—	150	—	ns
t_{AA}	Address Access Time	—	70	—	100	—	120	—	150	ns
t_{ACS}	Chip Select Access Time	—	70	—	100	—	120	—	150	ns
t_{OH}	Output Hold from Address Change	10	—	10	—	10	—	10	—	ns
t_{LZ}	Chip Selection to Output in Low Z	20	—	35	—	40	—	55	—	ns
t_{HZ}	Chip Deselection to Output in High Z	15	55	30	70	35	80	50	100	ns
t_{PU}	Chip Selection to Power Up Time	15	—	30	—	35	—	50	—	ns
t_{PD}	Chip Deselection to Power Down Time	—	70	—	100	—	120	—	150	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	70	—	100	—	120	—	150	—	ns
t_{CW}	Chip Selection to End of Write	65	—	80	—	100	—	120	—	ns
t_{AW}	Address Valid to End of Write	65	—	80	—	100	—	120	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	40	—	45	—	50	—	60	—	ns
t_{WRW}	Write Recovery Time $\overline{WE}$ Controlled	0	—	0	—	0	—	0	—	ns
t_{WRC}	Write Recovery Time $\overline{CS}$ Controlled	25	—	25	—	30	—	35	—	ns
t_{DW}	Data Valid to End of Write	30	—	30	—	35	—	40	—	ns
t_{DHW}	Data Hold Time $\overline{WE}$ Controlled	0	—	0	—	0	—	0	—	ns
t_{DHC}	Data Hold Time $\overline{CS}$ Controlled	25	—	25	—	30	—	35	—	ns
t_{WZ}	Write Enable to Ouput in High Z	0	40	0	40	0	50	0	50	ns
t_{OW}	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

TIMING WAVEFORM OF READ CYCLE NO. 1[1,2]

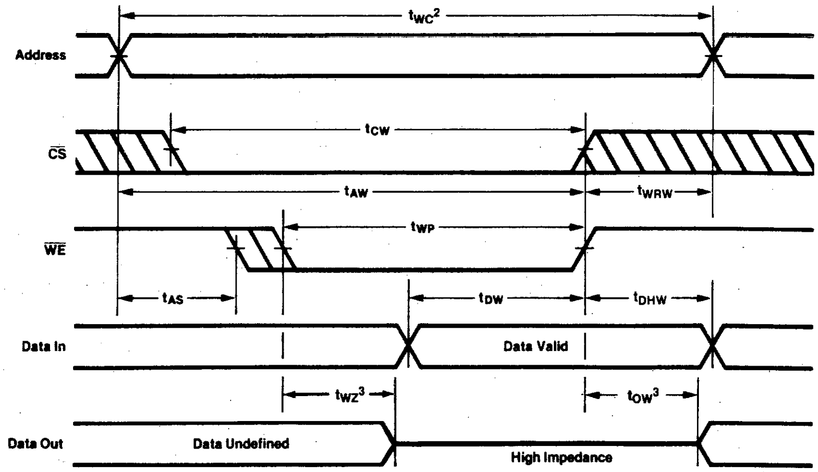


TIMING WAVEFORM OF READ CYCLE NO. 2[1,3]

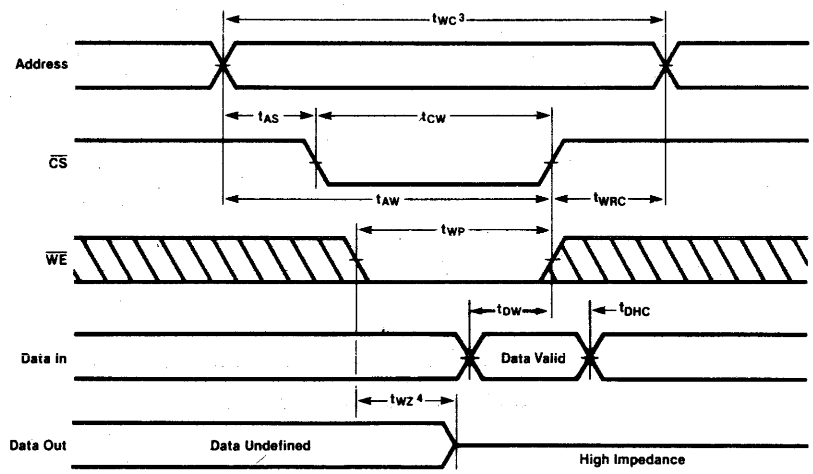


NOTES:
1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2. This parameter is sampled, not 100% tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[1]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)[1]



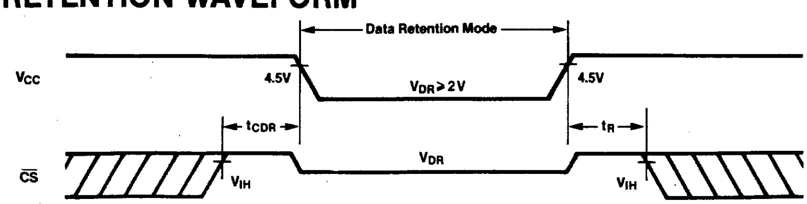
NOTES: 1. $\overline{WE}$ must be high during address transitions.
2. All write cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±100mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.

LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_A = −55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.(1)	MAX COMM.	MAX. MIL.	UNIT
V_{DR}	V_{CC} for Data Retention		2.0	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC}$ −0.2V $V_{IN} \geq V_{CC}$ −0.2V or ≤ 0.2V	— —	2.0(2) 4.0(3)	60(2) 90(3)	800(2) 1200(3)	μA
t_{CDR}	Chip Deselect to Data Retention Time		0	—	—	—	ns
t_R	Operation Recovery Time		t_{RC}(4)	—	—	—	ns

NOTES: 1. T_A = 25°C 3. at V_{CC} = 3V
2. at V_{CC} = 2V 4. t_{RC} = Read Cycle Time

LOW V_{CC} DATA RETENTION WAVEFORM



Integrated Device Technology

MEMORY

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Integrated Device Technology, Inc.

16x16 BIT PARALLEL CMOS MULTIPLIER

IDT7216 IDT7217

MILITARY / COMMERCIAL TEMPERATURE RANGES

FEATURES:

- 16x16 parallel multiplier with double precision product
- High-speed 75ns maximum clock to multiply time
- Produced with advanced CEMOS™I high-performance technology
- Low power consumption - 150mW typical, less than 1/10th the power of compatible bipolar parts
- IDT7216 is pin and functionally compatible with TRW MPY-16HJ and AMD AM29516
- IDT7217 requires only single clock with register enables making it pin and functionally compatible with AMD AM29517
- Configured for easy array expansion
- User controlled option for transparent output register mode
- Round control for rounding the MSP
- Single 5V power supply
- Input and output directly TTL-compatible
- Three-state output
- Available in DIP, LCC or Flat-Pak
- Standard product 100% screened to MIL-STD-883 Class C
- Military product available 100% screened to Class B

DESCRIPTION:

The IDT7216/IDT7217 are high speed, low power 16x16 multipliers, ideal for fast, real time digital signal processing applications. Utilization of a modified Booths algorithm and IDT's high-performance, high reliability technology - CEMOS I, has achieved speeds comparable to bipolar (75ns max.) at 1/10th the power consumption.

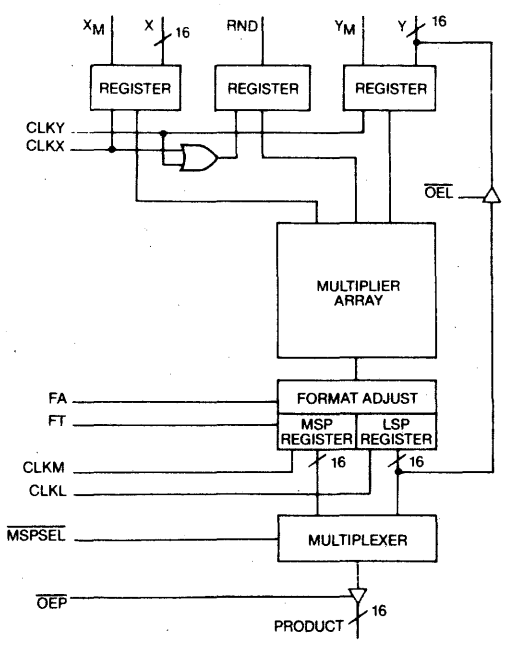
The IDT7216/IDT7217 are ideal for applications requiring high speed multiplications such as fast Fourier transform analysis, digital filtering, graphic display systems, speech synthesis and recognition, and in any system requirement where multiplication speeds of a mini/micro computer are inadequate.

All input registers, as well as LSP and MSP output registers, use the same positive edge triggered D type flip-flop. In the IDT7216, there are independent clocks (CLKX, CLKY, CLKM, CLKL) associated with each of these registers. The IDT7217 has only a single clock input (CLK) and three register enables. $\overline{\text{ENX}}$ and $\overline{\text{ENY}}$ control the two input registers, while $\overline{\text{ENP}}$ controls the entire product.

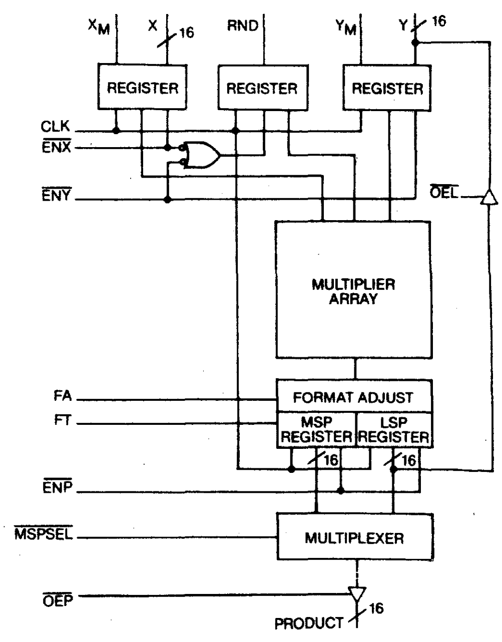
The IDT7216/7217 offer additional flexability with the FA control and $\overline{\text{MSPSEL}}$ functions. The FA control formats the output for 2's complement by shifting the MSP up one bit and then repeating the sign bit in the MSP of the LSP. The $\overline{\text{MSPSEL}}$ low selects the MSP to be available at the product output port, while a high selects the LSP to be available. Keeping this pin low will ensure total compatibility with the TRW MPY-16HJ.

The IDT7216/IDT7217 Multipliers are 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making them ideally suited to applications demanding the highest level of performance and reliability.

LOGIC DIAGRAMS



IDT7216



IDT7217

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ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	−55 to +125	°C
T_{BIAS}	Temperature Under Bias	−10 to +85	−65 to +135	°C
T_{STG}	Storage Temperature	−55 to +125	−65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 5%, T_A = 0°C to +70°C and V_{CC} = 5V ±10%, T_A = −55°C to +125°C)

SYMBOL	PARAMETER	TEST CONDITIONS	T_A = 0°C to 70°C MIN	TYP[1]	MAX	T_A = −55°C to +125°C MIN	TYP[1]	MAX	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max, V_{IN} = 0 to V_{CC}	—	—	2	—	—	10	μA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0 to V_{CC}	—	—	2	—	—	10	μA
I_{CC}	Operating Power Supply Current	Output Open	—	30	60	—	30	80	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$ or $\leq V_{IL}$	—	10	30	—	10	30	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geqslant V_{CC}$ − .2V or $\leqslant$ .2V	—	0.1	1.0	—	0.1	1.0	mA
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = −0.4mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0mA	—	—	0.5	—	—	0.5	V

(1) V_{CC} = 5V, T_A = 25°C.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	MIN	TYP	MAX	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	—	V
V_{IL}	Input Low Voltage	—	—	0.8	V

TEST LOADS

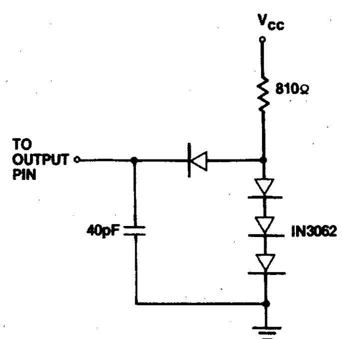

Figure 1. A.C. Output Test Load

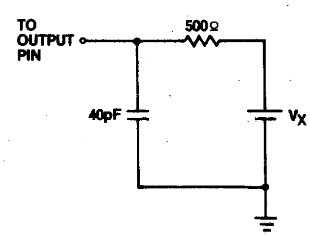

Figure 2. Output Three State Delay Load

V_X = 0V or 2.6V

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

SYMBOL	ITEM	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE: This parameter is sampled and not 100% tested.

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AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 5%, T_A = 0°C to +70°C) COMMERCIAL

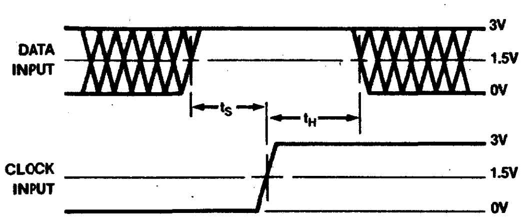
SYMBOL	PARAMETER	IDT7216-75 IDT7217-75 MIN.	MAX.	IDT7216-90 IDT7217-90 MIN.	MAX.	IDT7216-140 IDT7217-140 MIN.	MAX.	UNIT	TEST LOAD FIG.
t_{MUC}	Unclocked Multiply Time	—	110	—	125	—	180	ns	1
t_{MC}	Clocked Multiply Time	—	75	—	90	—	140	ns	1
t_S	X, Y, RND Setup Time	25	—	25	—	25	—	ns	1
t_H	X, Y, RND Hold Time	0	—	0	—	0	—	ns	1
t_{PWH}	Clock Pulse Width High	20	—	20	—	25	—	ns	1
t_{PWL}	Clock Pulse Width Low	20	—	20	—	25	—	ns	1
t_{PDSEL}	$\overline{MSPSEL}$ to Product Out	—	35	—	35	—	40	ns	1
t_{PDP}	Output Clock to P	—	35	—	35	—	40	ns	1
t_{PDY}	Output Clock to Y	—	35	—	35	—	40	ns	1
t_{ENA}	3 state enable time (Note 2)	—	35	—	35	—	40	ns	2
t_{DIS}	3 state disable time (Note 2)	—	30	—	30	—	40	ns	2
t_S	Clock Enable Setup Time (IDT7217 only)	25	—	25	—	25	—	ns	1
t_H	Clock Enable Hold Time (IDT7217 only)	0	—	0	—	0	—	ns	1
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML (see Note 1) (IDT7216 only)	0	—	0	—	0	—	ns	1

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = −55°C to +125°C) MILITARY

SYMBOL	PARAMETER	IDT7216-90 IDT7217-90 MIN.	MAX.	IDT7216-120 IDT7217-120 MIN.	MAX.	IDT7216-185 IDT7217-185 MIN.	MAX.	UNIT	TEST LOAD FIG.
t_{MUC}	Unclocked Multiply Time	—	130	—	160	—	230	ns	1
t_{MCS}	Clocked Multiply Time	—	90	—	120	—	185	ns	1
t_S	X, Y, RND Setup Time	30	—	30	—	30	—	ns	1
t_H	X, Y, RND Hold Time	0	—	0	—	0	—	ns	1
t_{PWH}	Clock Pulse Width High	30	—	30	—	30	—	ns	1
t_{PWL}	Clock Pulse Width Low	30	—	30	—	30	—	ns	1
t_{PDSEL}	$\overline{MSPSEL}$ to Product Out	—	40	—	40	—	45	ns	1
t_{PDP}	Output Clock to P	—	40	—	40	—	45	ns	1
t_{PDY}	Output Clock to Y	—	40	—	40	—	45	ns	1
t_{ENA}	3 state enable time (Note 2)	—	40	—	40	—	45	ns	2
t_{DIS}	3 state disable time (Note 2)	—	40	—	40	—	45	ns	2
t_S	Clock Enable Setup Time (IDT7217 only)	30	—	30	—	30	—	ns	1
t_H	Clock Enable Hold Time (IDT7217 only)	0	—	0	—	0	—	ns	1
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML (see Note 1) (IDT7216 only)	0	—	0	—	0	—	ns	1

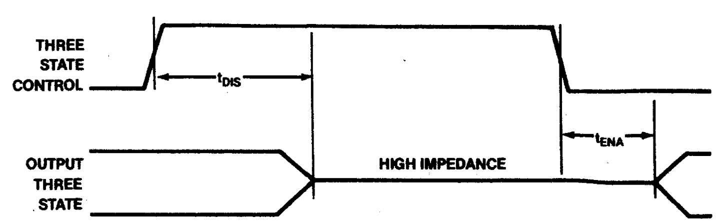
Note 1. To ensure that the correct product is entered in the output registers, new data may not be entered into the input registers before the output registers have been clocked.
2. Transition is measured ±500mV from steady state voltage with loading specified in Fig. 2

SET-UP AND HOLD TIME

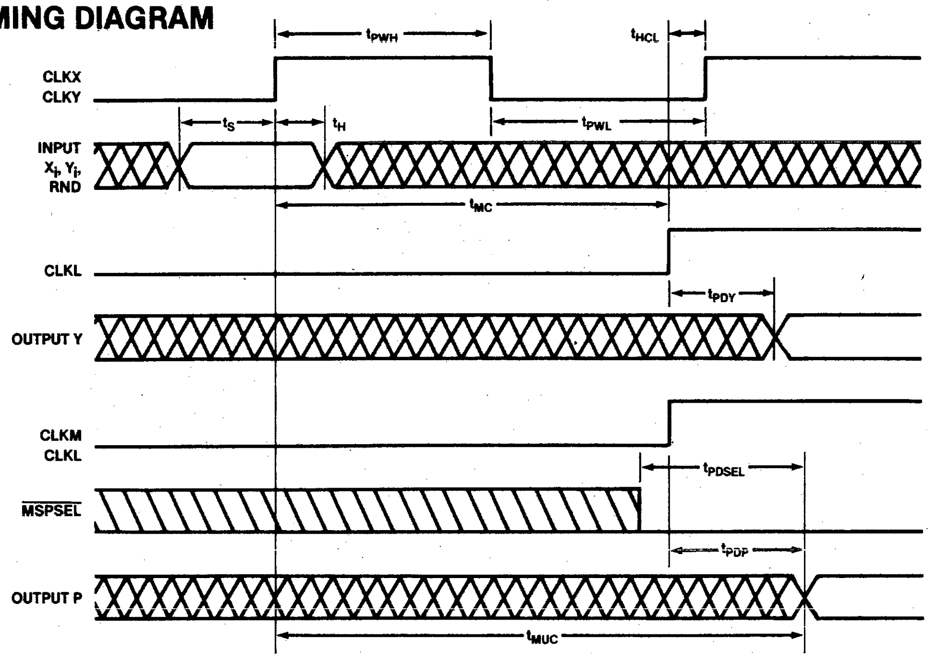


NOTES: Diagram shown for HIGH data only. Output transition may be opposite sense.

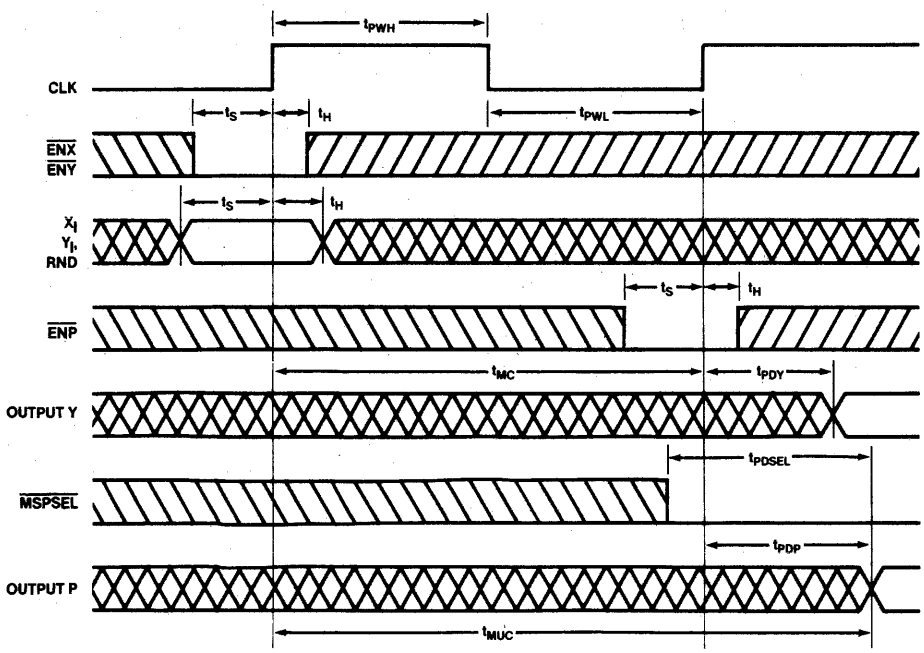
THREE STATE CONTROL TIMING DIAGRAM



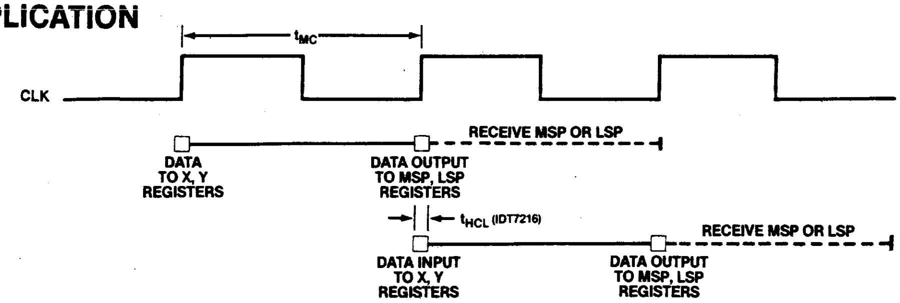
IDT7216 TIMING DIAGRAM



IDT7217 TIMING DIAGRAM



SIMPLIFIED TIMING DIAGRAM TYPICAL APPLICATION



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MEMORY

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DEFINITION OF TERMS

X_{15}-X_0	Multiplicand Data inputs.
Y_{15}-Y_0	Multiplier Data inputs.
X_M, Y_M (TCX, TCY)*	Mode control inputs for each data word; LOW for unsigned data and HIGH for two's complement data.
FA (RS)*	Format adjust control selects either a full 32-bit product (HIGH) or a left shifted 31-bit product with the sign bit replicated in the LSP (LOW). This control is normally high, except for certain fractional two's complement applications. (See Multiplier output formats table).
FT	Feedthrough control (HIGH) makes both MSP and LSP registers transparent.
$\overline{MSPSEL}$	Selects either MSP (LOW) or LSP (HIGH) to be available at the product output port.
RND	Round control for the rounding of the MSP.
$\overline{OEP}$ (TRIM)*	Three-state enable for product output port.
$\overline{OEL}$ (TRIL)*	Three-state enable for routing LSP through Y input/output port.
IDT7216 ONLY	
CLKX	Register Clock, X_{15}-X_0, X_M, RND
CLKY	Register Clock, Y_{15}-Y_0, Y_M, RND
CLKM	MSP Register Clock
CLKL	LSP Register Clock
IDT7217 ONLY	
CLK	Clock, All Registers
$\overline{ENX}$	Register Enable, X_{15}-X_0, X_M, RND
$\overline{ENY}$	Register Enable, Y_{15}-Y_0, Y_M, RND
$\overline{ENP}$	Register Enable, MSP, LSP

* TRW MPY 16HJ pin designation

16x16 BIT MULTIPLIER CONNECTION DIAGRAMS

PIN#	7216 DIP	7217 DIP	7216 FP	7217 FP	7216 LCC	7217 LCC
1	X_4	X_4	P_{15} P_{31}	P_{15} P_{31}	$+V_{CC}$	$+V_{CC}$
2	X_3	X_3	P_{14} P_{30}	P_{14} P_{30}	GND	GND
3	X_2	X_2	P_{13} P_{29}	P_{13} P_{29}	GND	GND
4	X_1	X_1	P_{12} P_{28}	P_{12} P_{28}	$\overline{MSPSEL}$	$\overline{MSPSEL}$
5	X_0	X_0	P_{11} P_{27}	P_{11} P_{27}	FT	FT
6	$\overline{OEL}$	$\overline{OEL}$	P_{10} P_{26}	P_{10} P_{26}	FA	FA
7	CLKL	CLK	P_9 P_{25}	P_9 P_{25}	$\overline{OEP}$	$\overline{OEP}$
8	CLKY	$\overline{ENY}$	P_8 P_{24}	P_8 P_{24}	CLKM	$\overline{ENP}$
9	P_0 Y_0	P_0 Y_0	P_7 P_{23}	P_7 P_{23}	N/C	N/C
10	P_1 Y_1	P_1 Y_1	P_6 P_{22}	P_6 P_{22}	P_{15} P_{31}	P_{15} P_{31}
11	P_2 Y_2	P_2 Y_2	P_5 P_{21}	P_5 P_{21}	P_{14} P_{30}	P_{14} P_{30}
12	P_3 Y_3	P_3 Y_3	P_4 P_{20}	P_4 P_{20}	P_{13} P_{29}	P_{13} P_{29}
13	P_4 Y_4	P_4 Y_4	P_3 P_{19}	P_3 P_{19}	P_{12} P_{28}	P_{12} P_{28}
14	P_5 Y_5	P_5 Y_5	P_2 P_{18}	P_2 P_{18}	P_{11} P_{27}	P_{11} P_{27}
15	P_6 Y_6	P_6 Y_6	P_1 P_{17}	P_1 P_{17}	P_{10} P_{26}	P_{10} P_{26}
16	P_7 Y_7	P_7 Y_7	P_0 P_{16}	P_0 P_{16}	P_9 P_{25}	P_9 P_{25}
17	P_8 Y_8	P_8 Y_8	P_{15} Y_{15}	P_{15} Y_{15}	P_8 P_{24}	P_8 P_{24}
18	P_9 Y_9	P_9 Y_9	P_{14} Y_{14}	P_{14} Y_{14}	P_7 P_{23}	P_7 P_{23}
19	P_{10} Y_{10}	P_{10} Y_{10}	P_{13} Y_{13}	P_{13} Y_{13}	P_6 P_{22}	P_6 P_{22}
20	P_{11} Y_{11}	P_{11} Y_{11}	P_{12} Y_{12}	P_{12} Y_{12}	P_5 P_{21}	P_5 P_{21}
21	P_{12} Y_{12}	P_{12} Y_{12}	P_{11} Y_{11}	P_{11} Y_{11}	P_4 P_{20}	P_4 P_{20}
22	P_{13} Y_{13}	P_{13} Y_{13}	P_{10} Y_{10}	P_{10} Y_{10}	P_3 P_{19}	P_3 P_{19}
23	P_{14} Y_{14}	P_{14} Y_{14}	P_9 Y_9	P_9 Y_9	P_2 P_{18}	P_2 P_{18}
24	P_{15} Y_{15}	P_{15} Y_{15}	P_8 Y_8	P_8 Y_8	P_1 P_{17}	P_1 P_{17}
25	P_0 P_{16}	P_0 P_{16}	P_7 Y_7	P_7 Y_7	P_0 P_{16}	P_0 P_{16}
26	P_1 P_{17}	P_1 P_{17}	P_6 Y_6	P_6 Y_6	N/C	N/C
27	P_2 P_{18}	P_2 P_{18}	P_5 Y_5	P_5 Y_5	P_{15} Y_{15}	P_{15} Y_{15}
28	P_3 P_{19}	P_3 P_{19}	P_4 Y_4	P_4 Y_4	P_{14} Y_{14}	P_{14} Y_{14}
29	P_4 P_{20}	P_4 P_{20}	P_3 Y_3	P_3 Y_3	P_{13} Y_{13}	P_{13} Y_{13}
30	P_5 P_{21}	P_5 P_{21}	P_2 Y_2	P_2 Y_2	P_{12} Y_{12}	P_{12} Y_{12}
31	P_6 P_{22}	P_6 P_{22}	P_1 Y_1	P_1 Y_1	P_{11} Y_{11}	P_{11} Y_{11}
32	P_7 P_{23}	P_7 P_{23}	P_0 Y_0	P_0 Y_0	P_{10} Y_{10}	P_{10} Y_{10}
33	P_8 P_{24}	P_8 P_{24}	CLKY	$\overline{ENY}$	P_9 Y_9	P_9 Y_9
34	P_9 P_{25}	P_9 P_{25}	CLKL	CLK	P_8 Y_8	P_8 Y_8
35	P_{10} P_{26}	P_{10} P_{26}	$\overline{OEL}$	$\overline{OEL}$	P_7 Y_7	P_7 Y_7
36	P_{11} P_{27}	P_{11} P_{27}	X_0	X_0	P_6 Y_6	P_6 Y_6
37	P_{12} P_{28}	P_{12} P_{28}	X_1	X_1	P_5 Y_5	P_5 Y_5
38	P_{13} P_{29}	P_{13} P_{29}	X_2	X_2	P_4 Y_4	P_4 Y_4
39	P_{14} P_{30}	P_{14} P_{30}	X_3	X_3	P_3 Y_3	P_3 Y_3
40	P_{15} P_{31}	P_{15} P_{31}	X_4	X_4	P_2 Y_2	P_2 Y_2
41	CLKM	$\overline{ENP}$	X_5	X_5	P_1 Y_1	P_1 Y_1
42	$\overline{OEP}$	$\overline{OEP}$	X_6	X_6	P_0 Y_0	P_0 Y_0
43	FA	FA	X_7	X_7	N/C	N/C
44	FT	FT	X_8	X_8	CLKY	$\overline{ENY}$
45	$\overline{MSPSEL}$	$\overline{MSPSEL}$	X_9	X_9	CLKL	CLK
46	GND	GND	X_{10}	X_{10}	$\overline{OEL}$	$\overline{OEL}$
47	GND	GND	X_{11}	X_{11}	X_0	X_0
48	$+V_{CC}$	$+V_{CC}$	X_{12}	X_{12}	X_1	X_1
49	$+V_{CC}$	$+V_{CC}$	X_{13}	X_{13}	X_2	X_2
50	Y_M	Y_M	X_{14}	X_{14}	X_3	X_3
51	X_M	X_M	X_{15}	X_{15}	X_4	X_4
52	RND	RND	CLKX	$\overline{ENX}$	X_5	X_5
53	CLKX	$\overline{ENX}$	RND	RND	X_6	X_6
54	X_{15}	X_{15}	X_M	X_M	X_7	X_7
55	X_{14}	X_{14}	Y_M	Y_M	X_8	X_8
56	X_{13}	X_{13}	$+V_{CC}$	$+V_{CC}$	X_9	X_9
57	X_{12}	X_{12}	$+V_{CC}$	$+V_{CC}$	X_{10}	X_{10}
58	X_{11}	X_{11}	GND	GND	X_{11}	X_{11}
59	X_{10}	X_{10}	GND	GND	X_{12}	X_{12}
60	X_9	X_9	$\overline{MSPSEL}$	$\overline{MSPSEL}$	N/C	N/C
61	X_8	X_8	FT	FT	X_{13}	X_{13}
62	X_7	X_7	FA	FA	X_{14}	X_{14}
63	X_6	X_6	$\overline{OEP}$	$\overline{OEP}$	X_{15}	X_{15}
64	X_5	X_5	CLKM	$\overline{ENP}$	CLKX	$\overline{ENX}$
65	—	—	—	—	RND	RND
66	—	—	—	—	X_M	X_M
67	—	—	—	—	Y_M	Y_M
68	—	—	—	—	$+V_{CC}$	$+V_{CC}$

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IDT MILITARY PROCESSING TO MIL-STD-883

Maintaining the highest standards of quality in our memory products is the basis of IDT's standard manufacturing systems and procedures. IDT products begin with stringent design rules derived for use in high reliability programs. This is followed by a dedicated commitment to reliable workmanship as well as rigid controls throughout wafer fab, device assembly and electrical test, all of which are designed to produce products that are inherently reliable.

All monolithic memory products, including commercial grade, are manufactured and screened to the demanding requirements of MIL-STD-883, Method 5004, Class C. Documentation, design, processing and assembly workmanship guidelines for these monolithic components are patterned after MIL-M-38510 specifications.

For customer applications requiring higher levels of reliability screening, we supply full military range monolithic components completely screened to the Class B criteria of Method 5004. This includes 100% 160-hour burn-in at $T_A = +125°C$ (or equivalent) per Method 1015 followed by 100% temperature testing of all DC and AC parameters and DC functional characteristics over the full −55°C to +125°C temperature range.

In the case of module assemblies, additional screening of the fully assembled RAMPAKs is performed per Figure 3 to assure package integrity and mechanical reliability. Finally, 100% electrical tests are performed.

Samples of the monolithic product which have been processed to Method 5004 100% screening requirements are submitted to the Quality Conformance inspection requirements of MIL-STD-883. These Quality Conformance inspections, as shown in Figure 2, are performed to the criteria of Method 5005, Group A (electrical), Group B (mechanical), Group C (chip integrity), and Group D (package environmental integrity).

For special customer specifications or quality requirements beyond Class B levels of MIL-STD-883 — such as SEM analysis, X-ray, or other screening flows to meet specific needs — contact your local IDT sales office.

MONOLITHIC COMPONENT SCREENING PROCEDURES

PER MIL-STD-883, METHOD 5004, CLASS B

SCREEN	TEST METHOD	LEVEL
Visual and Mechanical		
Internal Visual	2010 Condition B	100%
High-Temperature Storage	1008, Condition C	100%
Temperature Cycle	1010, Condition C	100%
Constant Acceleration	2001	100%
Hermeticity, Fine and Gross	1014	100%
Burn-In		
Pre-Burn-In Electrical	Per Applicable Device Specification	100%
Burn-In	1015, 160 Hrs. @ +125°C or Equivalent	100%
Final Electrical Tests		
Static (DC)	a. At 25°C and Power Supply Extremes	100%
	b. At Temperature and Power Supply Extremes	100%
Functional	a. At 25°C and Power Supply Extremes	100%
	b. At Temperature and Power Supply Extremes (IDT imposed)	100%
Switching (AC) or Dynamic	a. At 25°C and Power Supply Extremes	100%
	b. At Temperature and Power Supply Extremes (IDT imposed)	100%
External Visual	2009	100%

Figure 1

QUALITY CONFORMANCE TESTING

PER MIL-STD-883, METHOD 5005, CLASS B

SCREEN	TEST METHOD	LEVEL
Quality Conformance Sample Tests	Group A (Electrical Tests)	Sample
	Group B (Mechanical Tests)	Sample
	Group C (Chip Integrity Tests)	Sample
	Group D (Package Integrity Tests)	Sample

Figure 2

FULLY ASSEMBLED MODULE SCREENING

PER MIL-STD-883, METHOD 5004, CLASS B

SCREEN	TEST METHOD	LEVEL
Temperature Cycle	1010 Condition C	100%
Hermeticity Fine and Gross	1014	100%
Final Electrical Tests		
Static (DC)	a. At 25°C and Power Supply Extremes	100%
	b. At Temperature and Power Supply Extremes	100%
Functional	a. At 25°C and Power Supply Extremes	100%
	b. At Temperature and Power Supply Extremes (IDT exposed)	100%
Switching (AC) or Dynamic	a. At 25°C and Power Supply Extremes	100%
	b. At Temperature and Power Supply Extremes (IDT exposed)	100%
External Visual	2009	100%

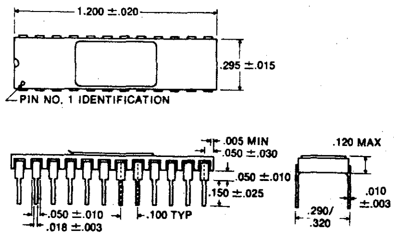
Figure 3

For special customer specifications or quality requirements beyond Class B levels of MIL-STD-883, such as SEM analysis, X-ray, or other screening flows to meet specific needs, contact your local IDT sales office.

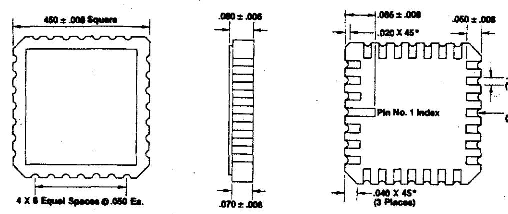
Integrated Device Technology MEMORY

CMOS PRODUCTS PACKAGE DIAGRAMS
IDT6116/IDT71681/IDT71682

24-LEAD THINDIP SIDEBRAZE

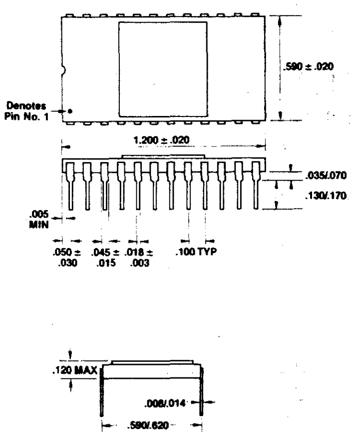


28 PIN LCC

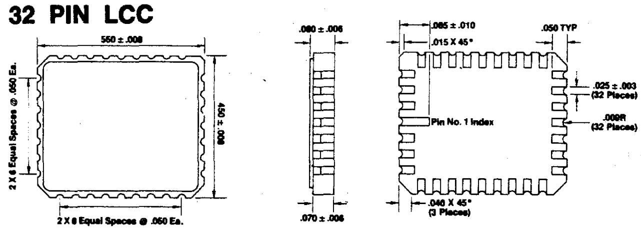


IDT6116

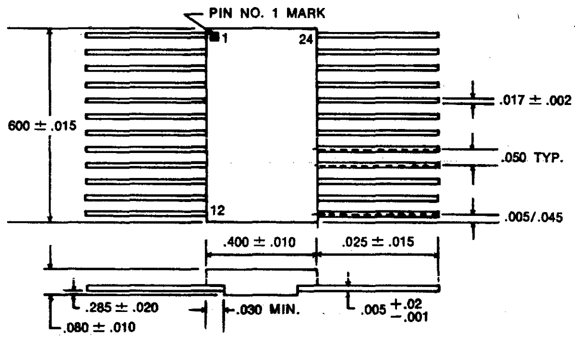
24-LEAD SIDEBRAZE



32 PIN LCC

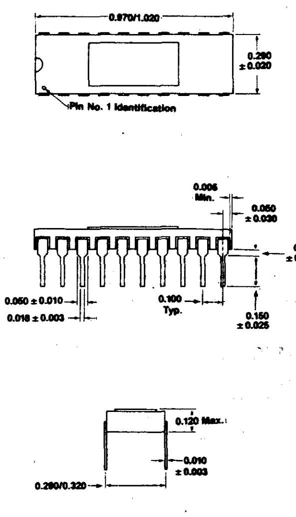


24-LEAD FLATPACK

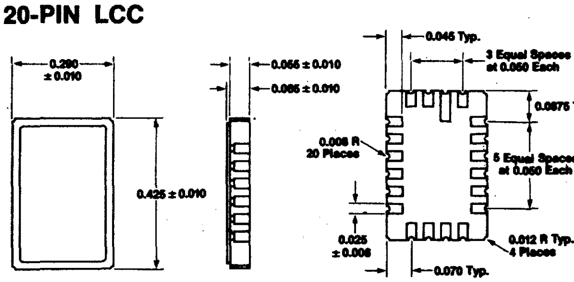


IDT6167/IDT6168

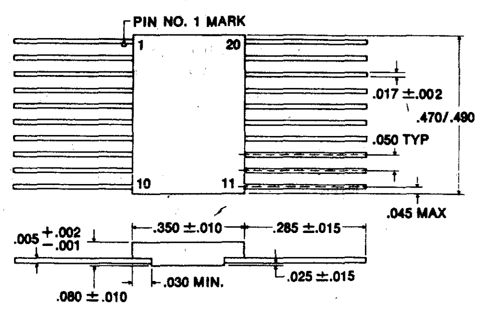
20-LEAD SIDEBRAZE



20-PIN LCC



20-LEAD FLATPACK



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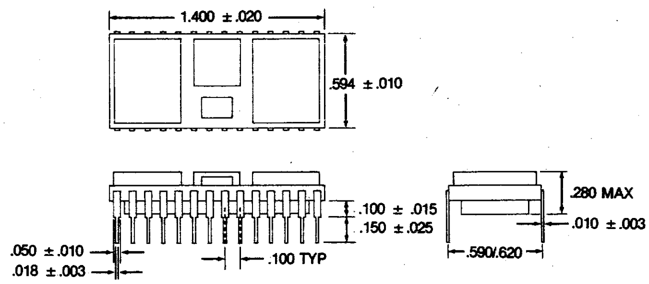
CMOS PRODUCTS PACKAGE DIAGRAMS

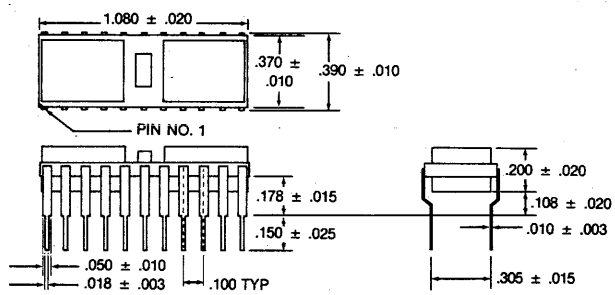
IDT7M/8M864

28-LEAD SIDEBRAZE



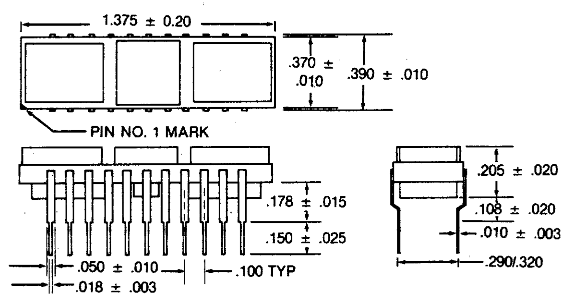
IDT7M464 (BENT LEADS)

22-LEAD SIDEBRAZE



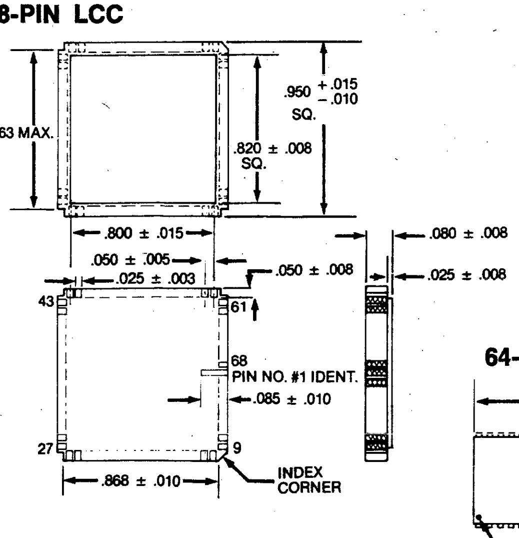
IDT7M164

22-LEAD SIDEBRAZE

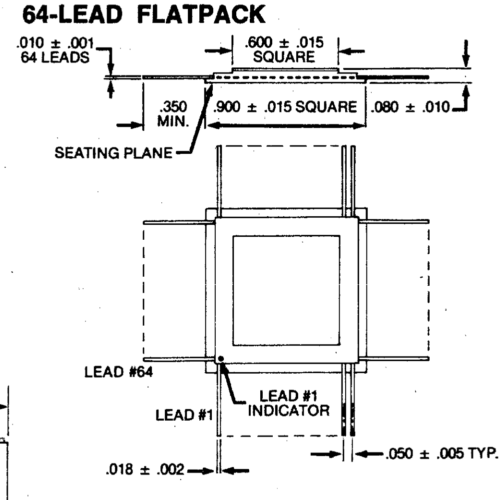


IDT7216/7217

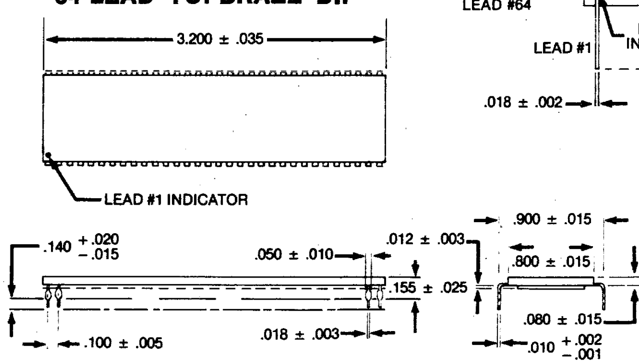
68-PIN LCC



64-LEAD FLATPACK



64-LEAD TOPBRAZE DIP



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intel

PRELIMINARY

BPK 72A
1MBIT BUBBLE MEMORY PROTOTYPE KIT

Device	Case Operating Temperature
BPK 72A-1	0 To 75°C
BPK 72A-4	10°C To 55°C
BPK 72A-5	– 20°C To 85°C

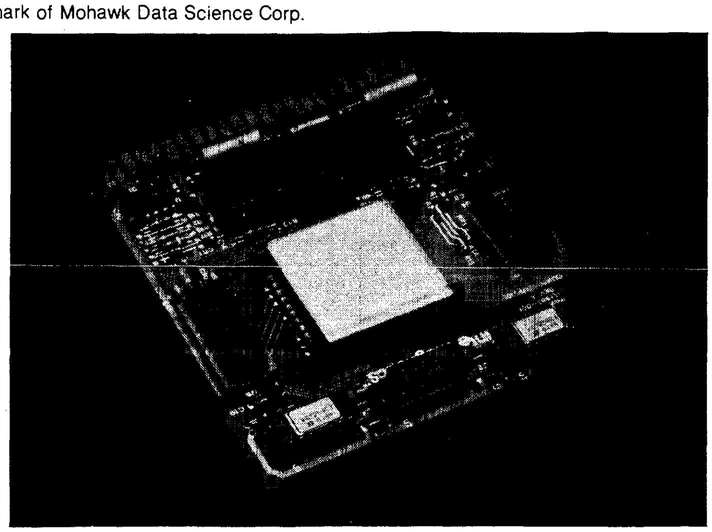
- **Assembled and Tested 1MBit Bubble Memory Prototype Kit on 4" x 4" PC Board**
- **Complete with Powerfail Data Protection and Clock Circuitry**
- **Built-in Error Detection/Correction**
- **Interfaces with Intel 8080/85/86/88 186/286 and Other Microprocessors**
- **Software Driver for Bubble Memory Kit Diskette for Intel MDS* System**
- **1Mbit, Non-Volatile, Read-Write, Solid-State Memory in Leaded Dense Package**
- **Average Random Access Time of 48ms**
- **Maximum Data Rate of 100K bit/sec**
- **Operates from +5V and +12V Power Supplies**
- **Complete Documentation and Interfacing Information Included**

The BPK 72A prototype kit is a completely assembled and tested 1Mbit bubble memory evaluation tool. It is ideal for the design engineer that wants the opportunity to fast evaluate how a bubble memory solution improves and adds value to an end-product by providing a compact solid-state memory that also reliably keeps the data at any powerdown.

Application information on microprocessor interfacing is included in the kit. A Bubble Memory Kit software driver is also included on a diskette for the Intel MDS* System.

For production purposes, the bubble memory and the support circuit components can be ordered as the BPK 70A Subsystem. The 7220, controlling up to eight BPK 70A's, is ordered separately.

*MDS is a registered trademark of Mohawk Data Science Corp.



OCTOBER 1983
ORDER NO. 210804-002

BPK 70A
1MBIT BUBBLE MEMORY SUBSYSTEMS

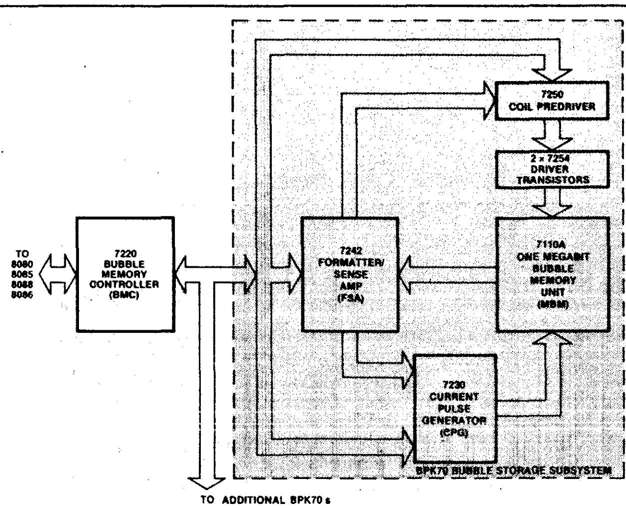
Device	Case Operating Temperature
BPK 70A-1	0 To 75°C
BPK 70A-4	10°C To 55°C
BPK 70A-5	– 20°C To 85°C

- **1 Mbit (128K Bytes) Non-Volatile, Solid-State, Read/Write Bubble Memory Subsystem**
- **Interfaces to Host Microprocessor Via Additional Bubble Memory Controller**
- **Maximum Data Rate of 100K Bit/Sec with One Subsystem**
- **Maximum Data Rate of 800K Bit/Sec with Eight Subsystems in Parallel**
- **Contains Bubble Memory and ICs for Production with 1Mbit Bubble Memory**
- **Modularity Provides Expansion Up to Eight Subsystems Per Controller**
- **Average Random Access Time of 48ms**
- **Bubble Memory in 20-Pin, Dual-In-Line Leaded Package**

A BPK 70A Bubble Storage Subsystem is a modular building block consisting of one 1Mbit Magnetic Bubble Memory and five support ICs (Shown in the figure below). The MBM is in a leaded package requiring no socket. These are the basic components to build a non-volatile, solid-state, read-write memory system utilizing 1Mbit bubble memory.

An additional 1Mbit Bubble Memory Controller (BMC) 7220 provides the interface between the host microprocessor and the Bubble Memory Subsystem and provides all the timing and control signals to the Subsystem. The user interface of the BMC is compatible with microprocessor bus systems for 8080, 8085, 8086, 8088, 80186, 80286 and other standard microprocessors. The BMC is a software driven device utilizing 16 convenient commands. The design engineer's primary responsibility is the interfacing to the BMC. This interfacing is comparable to the one of a disk drive controller.

The modular Intel Subsystem provides a path for density expansion. One BMC can interface up to eight BPK 70A subsystems. Thus a 1Mbit (128K byte) system can be expanded up to 8Mbit (1M byte) by using additional subsystems.



CONFIGURATION OF ONE BPK 70 BUBBLE STORAGE SUBSYSTEM WITH THE 7220 CONTROLLER

OCTOBER 1983
ORDER NO. 210356-003

ADVANCE INFORMATION

2004
4K (512 x 8) NON-VOLATILE RANDOM ACCESS MEMORY

- **5 Volt Only Operation**
- **Fast Static RAM Read/Write Cycles**
  2004-2, 200ns Max.
  2004, 250ns Max.
  2004-3, 300ns Max.
- **Single Line STORE & RECALL**
- **10ms Self-Timed STORE Cycles for 2004-2 and 2004 (20ms for 2004-3)**
- **Automatic Recall on Power Up**
- **Write Protect Circuit to Preserve Data On Power-Up and Power-Down**
- **Lower Power Standby Mode**
- **10-Year Data Retention for each STORE**
- **Minimum 10,000 Non-Volatile STORE Cycle Endurance**
- **Unlimited Endurance for Read, Write, and RECALL Cycles**
- **HMOS*-E FLOTOX Cell Design**
- **Conforms to JEDEC Byte-Wide Universal Site**

The Intel 2004 Non-Volatile Random Access Memory (NVRAM) is a 4K device with 512 × 8 architecture. It provides the real-time read/write functions of a static RAM together with the reliable non-volatile storage capability of an E^2PROM array to preserve its memory contents when power is removed.

Internally, the 2004 NVRAM consists of a high speed static RAM array backed up, bit-for-bit, by an E^2PROM array for non-volatile storage. The transfer of memory data between the static RAM and the E^2PROM array occurs in parallel for fast storage and recall as well as minimal system support.

Two functions are provided to transfer data between the volatile RAM and its non-volatile E^2PROM counterpart. The STORE function transfers RAM data into the E^2PROM while the RECALL function fetches E^2PROM data and places it in the RAM array. Both functions are controlled by a single $\overline{NE}$ signal which can easily be activated with traditional circuitry in memory mapped space, through an I/O port, or from the output of a power-fail detector.

The RAM operating characteristics of the 2004 NVRAM provides high speed microprocessor performance with unlimited endurance. In the non-volatile storage mode, data retention is specified at over 10 years for each STORE operation. Over 10,000 STORE operations can be performed reliably.

The 2004 NVRAM is furnished in a 28-pin byte wide package with its address, data and control lines configured according to the standard JEDEC universal 28-pin site.

*HMOS is patent process of Intel Corporation.

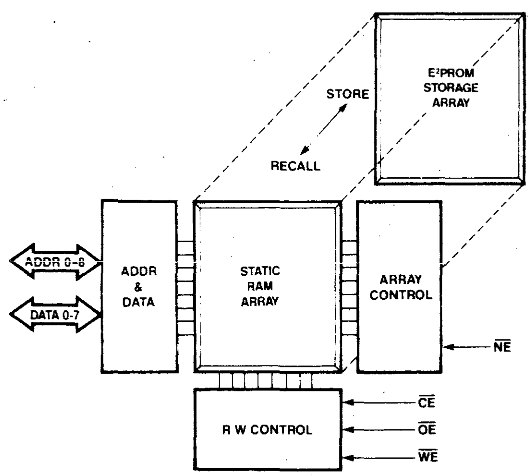


Figure 1. 2004 Functional Diagram

2004 PIN NAMES

A_0-A_8	ADDRESSES
I/O	DATA INPUT/OUTPUTS
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE (READ)
$\overline{NE}$	NON-VOLATILE ENABLE (STORE/RECALL CONTROL)
$\overline{WE}$	WRITE ENABLE
N. C.	NO CONNECT

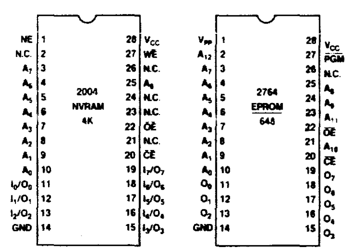


Figure 2. 2004 Pin Configuration

AUGUST 1983
ORDER NUMBER: 230665-003

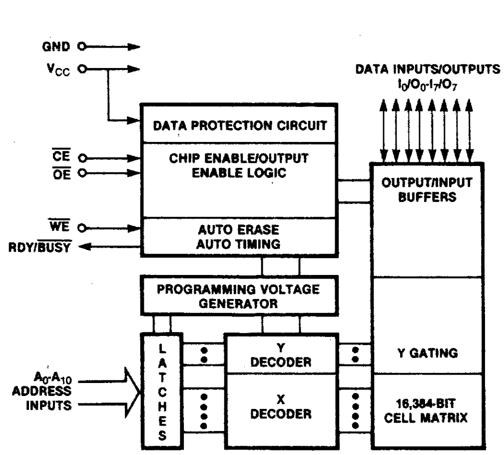
Intel
MEMORY

2817A
16K (2K x 8) ELECTRICALLY ERASABLE PROM

- **5 Volt Only Operation**
- **On-Chip Latches for Direct Microprocessor Interface**
- **Automatic Byte-Erase-before-Write**
- **Self Timed Byte Write**
- **Fast Read Access Time:**
  - —2817A-1 200ns max
  - —2817A-2 200ns max
  - —2817A 250ns max
  - —2817A-3 350ns max
  - —2817A-4 450ns max
- **Write Protect Circuit to Preserve Data on Power Up and Power Down**
- **10,000 Erase/Write Cycles per Byte**
- **Reliable Intel HMOS*-E FLOTOX Cell Design Technology**
- **READY/$\overline{BUSY}$ Line for End-of-Write Signal**
- **10 Year Data Retention For Each Write**

The Intel 2817A is a 16,384 bit Electrically Erasable Programmable Read Only Memory. Like the Intel 2816A it has completely Non-Volatile Data Storage. In addition, it offers a high degree of integrated functionality which enables in-circuit byte writes to be performed with minimal hardware and software overhead. The Intel 2817A is a product of Intel's advanced E^2PROM technology and uses the powerful HMOS*-E process for reliable, non-volatile data storage.

*HMOS is a patented process of Intel Corporation.



PIN NAMES

A_0-A_{10}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	DATA OUTPUTS
I_0-I_7	DATA INPUTS
RDY/$\overline{BUSY}$	DEVICE READY/BUSY
N.C.	NO CONNECT
$\overline{WE}$	WRITE ENABLE

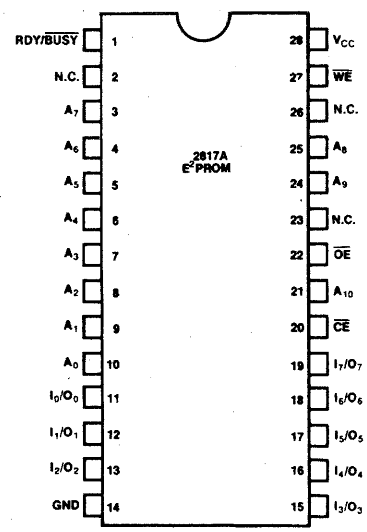


Figure 1. 2817A Functional Block Diagram

Figure 2. 2817A Pin Configuration

OCTOBER 1983
ORDER NO. 230641-002

intel

PRELIMINARY

27256
256K (32K x 8) UV ERASABLE PROM

- **Software Carrier Capability**
- **250 ns Maximum Access Time**
- **Two-Line Control**
- **int$_e$ligent Identifier™ Mode —Automated Programming Operations**
- **TTL Compatible**
- **Industry Standard Pinout . . . JEDEC Approved**
- **Low Power —100 mA max. Active — 40 mA max. Standby**
- **int$_e$ligent Programming™ Algorithm —Fastest EPROM Programming**

The Intel 27256 is a 5V only, 262,144-bit ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM). Organized as 32K words by 8 bits, individual bytes are accessed in under 250ns. This is compatible with high performance microprocessors, such as the Intel 8MHz iAPX 186, allowing full speed operation without the addition of performance-degrading WAIT states. The 27256 is also directly compatible with Intel's 8051 family of microcontrollers.

The 27256 enables implementation of new, advanced systems with firmware intensive architectures. The combination of the 27256's high density, cost effective EPROM storage, and new advanced microprocessors having megabit addressing capability provides designers with opportunities to engineer user-friendly, high reliability, high-performance systems.

The 27256's large storage capability of 32K bytes enables it to function as a high density software carrier. Entire operating systems, diagnostics, high-level language programs and specialized application software can reside in a 27256 EPROM directly on a system's memory bus. This permits immediate microprocessor access and execution of software and eliminates the need for time consuming disk accesses and downloads.

Several advanced features have been designed into the 27256 that allow for fast and reliable programming —the int$_e$ligent identifier™ mode and the int$_e$ligent Programming™ Algorithm. Programming equipment that takes advantage of these innovations will electronically identify the 27256 and then rapidly program it using an efficient programming method.

Two-line control and JEDEC-approved, 28-pin packaging are standard features of all Intel high-density EPROMs. This assures easy microprocessor interfacing and minimum design efforts when upgrading, adding, or choosing between nonvolatile memory alternatives.

The 27256 is manufactured using Intel's advanced HMOS*II-E technology.

*HMOS is a patented process of Intel Corporation.

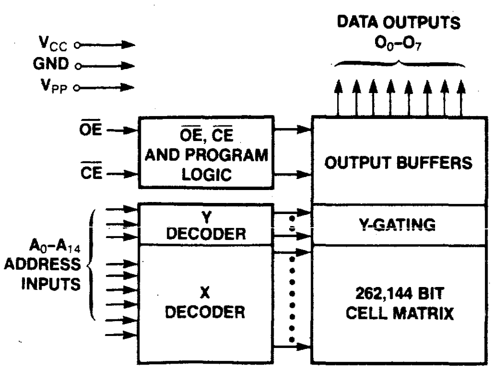
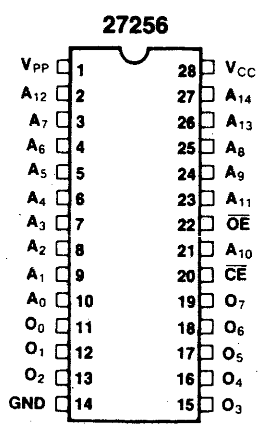


Figure 1. Block Diagram



PIN NAMES

A_0–A_{14}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0–O_7	OUTPUTS

Figure 2. Pin Configuration

Intel

MEMORY

JUNE 1983
ORDER NUMBER: 210827-004

High Performance Ti-W PROM Family

53/63SXXX   53/63SXXXA

Features/Benefit

- From 256 Bit to 32768 Bit of memory
- Reliable Titanium-Tungsten fuses (Ti-W)
- Low voltage programming
- Highest speed Schottky PROM family available
- Pin compatible with standard Schottky PROMs
- PNP inputs for low input current
- Compatible pin configurations for upward expansion

Applications

- Microprogram control store
- microprocessor program store
- Look up table
- Character generator
- Random logic
- Code converter

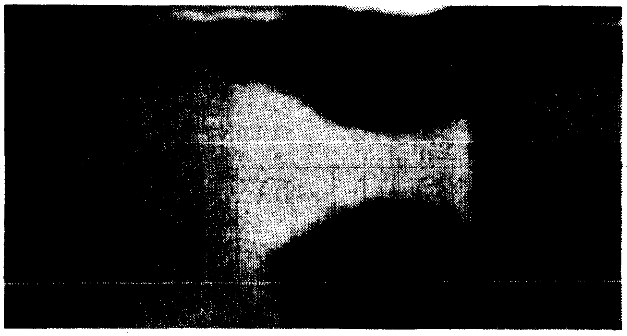
Description

The family features common electrical parameters and programming algorithm, low input current PNP inputs, full Schottky clamping and three-state and open collector outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on chip circuitry and extra fuses provide preprogramming testing which assure high programming yields and high reliability.

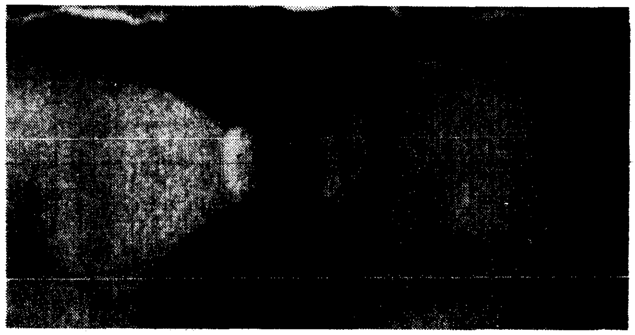
The 63 series is specified for operation over the commercial temperature and voltage range. the 53 series is specified for the military ranges.

New Programming Technique:

Our new HIGH Performance PROMs use an elevated voltage at V_{CC} instead of using a separate programming pin (one of the enables) as in the Standard Performance PROMs using nichrome fuses. Changes in the internal circuitry were made to optimize speed and accordingly the unblown fuse represents a LOW at the output. When a fuse is programmed it reflects a high at the output.



Unblown Fuse



Blown Fuse

High Performance PROM Selection Guide

MEMORY			PACKAGE		DEVICE TYPE	
SIZE	ORGANIZATION		PINS	TYPE	0°C to + 75°C	- 55°C to + 125°C
¼K	32 x 8	OC TS	16, (20)	N,J,F,W (L)	63S080 63S081	53S080 53 S081
1K	256 x 4	OC TS	16, (20)	N,J,F,W (L)	63S140 63S141	53S140 53S141
2K	512 x 4	OC TS	16, (20)	N,J,F,W (L)	63S240 63S241	53S240 53S241
4K	1024 x 4	TS	18, (20)	N,J,F, (L)	63S441 63S441A	53S441 53S441A
8K	2048 x 4	TS	18, (28)	N,J,F, (L)	63S841 63S841A	53S841 53S841A
16K	4096 x 4	TS	20	N, J, F	63S1641 63S1641A	53S1641 53S1641A
	2048 x 8	TS	24, (28)	J,JS,F, (L)	63S1681 63S1681A	53S1681 53S1681A
32K	4096 x 8	TS	24, (28)	*J (L)	63S3281 63S3281A	53S3281 53S3281A

* Flat-pack contact the factory   ( ) = Military Product

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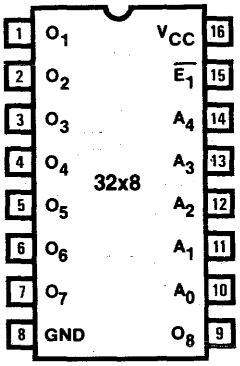
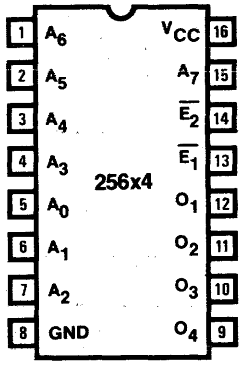
Pin Configurations

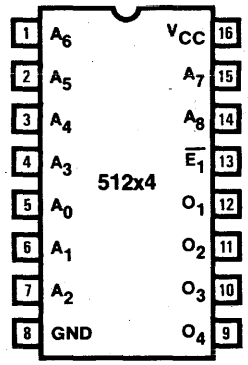
53/63S080
53/63S081



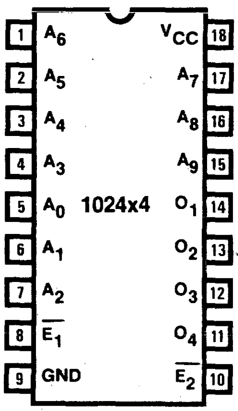
53/63S140
53/63S141



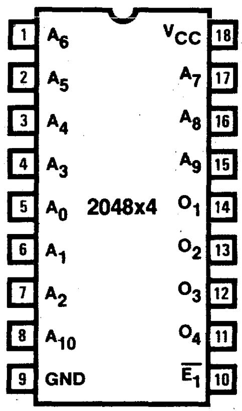
53/63S240
53/63S241



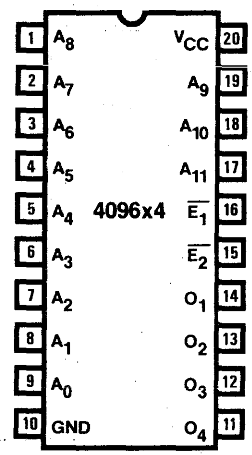
53/63S441
53/63S441A



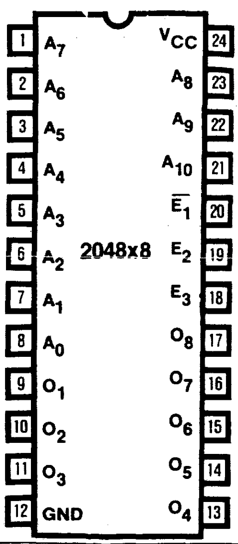
53/63S841
53/63S841A



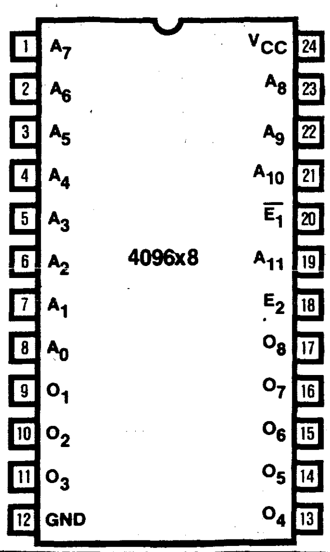
53/63S1641
53/63S1641A



53/63S1681
53/63S1681A



53/63S3281
53/63S3281A



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Absolute Maximum Ratings

Supply voltage V_{CC} .... −0.5V to 7V
Input voltage .... −1.5V to 7V
Off-state output voltage .... −0.5V to 5.5V
Storage temperature range .... −65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA				−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V				−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 16mA	MIL			0.5	V
				COM except S1681, S3281			0.45	
				COM S1681, S3281			0.5	
V_{OH}	High-level output voltage *	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL I_{OH} = −2mA		2.4			V
			COM I_{OH} = −3.2mA					
I_{OZL}	Off-state output current *	V_{CC} = MAX	V_O = 0.4V				−40	μA
I_{OZH}			V_O = 2.4V				40	μA
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4V				40	μA
			V_O = 5.5V				100	
I_{OS}	Output short-circuit current **	V_{CC} = 5V	V_O = 0V		−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX All inputs grounded. All outputs open.	S080, S081			90	125	mA
			S140, S141			80	130	
			S240, S241			90	130	
			S441, S441A			95	140	
			S841, S841A			110	150	
			S1641, S1641A			130	175	
			S1681, S1681A			135	185	
			S3281, S3281A			150	190	

* Three-state only.
** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

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Monolithic Memories

Switching Characteristics

Over Commercial Operating Conditions

DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME MAX	t_{EA} AND t_{ER} (ns) ENABLE ACCES AND RECOVERY TIME MAX
63S080, 63S081	25	20
63S140, 63S141	45	25
63S240, 63S241	45	25
63S441	45	25
63S441A	35	25
63S841	50	25
63S841A	35	25
63S1641	50	25
63S1641A	35	25
63S1681	50	30
63S1681A	35	30
63S3281	50	30
63S3281A	40	30

Over Military Operating Conditions

DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME MAX	t_{EA} AND t_{ER} (ns) ENABLE ACCES AND RECOVERY TIME MAX
53S080, 53S081	35	30
53S140, 53S141	55	30
53S240, 53S241	55	30
53S441	55	30
53S441A	50	30
53S841	55	30
53S841A	50	30
53S1641	65	30
53S1641A	50	30
53S1681	60	35
53S1681A	50	35
53S3281	60	35
53S3281A	50	35

High Performance Registered 1024x4 PROM
53/63RA441

Features/Benefits

- Edge triggered "D" registers
- Advanced Schottky processing
- 4-bit-wide in 18 pin for high board density
- Lower system package counts
- Lower system power
- Faster cycle times
- 16mA I_{OL} output drive capability

Applications

- Pipelined microprogramming
- State sequencers
- Next address generation
- Mapping PROM

Description

A family of registered PROMs offers new savings for designers of pipelined microprogrammable systems. The wide instruction register which holds the micro-instruction during execution, is now incorporated into the PROM chip.

Ordering Information

MEMORY		PACKAGE		DEVICE TYPE	
SIZE	ORGANIZATION	PINS	TYPE	MIL	COM
4K	1024x4	18	J, N	53RA441	63RA441

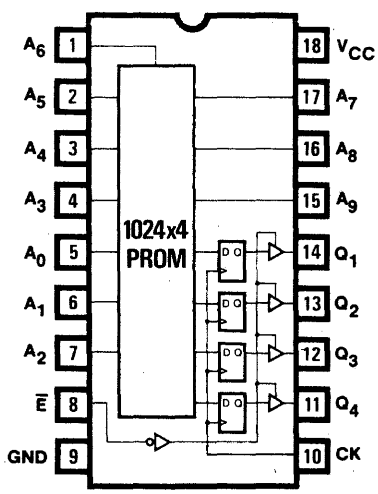
Edge Triggered Register

The PROM output is loaded into a 4-bit register on the rising edge of the clock. The use of the term "register" is to be distinguished from the term "latch," in that a register contains master slave flip-flops and the latch contains gated flip-flops. The advantages of using a register are that system timing is simplified, and faster micro cycle times can be obtained.

The output of the register is buffered by three-state drivers which are compatible with the new low-power Schottky three-state bus standard.

Pin Configuration

53/63RA441



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Monolithic Memories MMI

Monolithic Memories

MEMORY

Absolute Maximum Ratings

Supply voltage, V_{CC} 7V
Input voltage 7V
Off-state output voltage 5.5V
Storage temperature .... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
t_{su}	Address set-up time	60	30		50	30		
t_h	Address hold time	0	−10		0	−10		
t_w	Clock pulse width	25	8		20	8		
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA				−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V				−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC}				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 16mA				0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OH} = −2mA COM I_{OH} = −3.2mA		2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.5V				−40	μA
I_{OZH}	Off-state output current	V_{CC} = MAX	V_O = 2.4V				40	μA
I_{OS}	Output short-circuit current*	V_{CC} = 5V	V_O = 0V		−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX	All inputs grounded All outputs open	MIL		120	175	mA
				COM		120	165	mA

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

†Typicals at 5.0V V_{CC} and 25°C T_A

Switching Characteristics

Over Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{pd}	Clock to output access time		20	35		20	30	ns
t_{ER}/t_{EA}	Enable to output access and recovery time		19	35		19	30	ns

Monolithic Memories

MEMORY

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Monolithic Memories

High Performance 1024x8 Registered PROM

53/63RS881 53/63RS881A

Features/Benefits

- Edge triggered "D" registers
- Synchronous and Asynchronous enables
- Versatile 1:16 initialization words
- 8-bit-wide in 24 pin SKINNYDIP® for high board density
- Simplifies system timing
- Faster cycle times
- 16mA I_{OL} output drive capability
- Reliable titanium-tungsten fuses (Ti-W)

Applications

- Microprogram control store
- State sequencers
- Next address generation
- Mapping PROM

Description

The 53/63RS881 and 53/63RS881A are 1Kx8 PROMs with on chip "D" type registers, versatile output enable control through synchronous and asynchronous enable inputs, and flexible start up sequencing through programmable initialization.

Data is transferred into the output registers on the rising edge of the clock. Provided that the asynchronous ($\overline{E}$) and synchronous ($\overline{E_S}$) enables are low, the data will appear at the outputs. Prior to the positive clock edge, register data are not affected by changes in addressing or synchronous enable inputs.

Memory expansion and data control is made flexible with synchronous and asynchronous enable inputs. Outputs may be set to the high impedance state at any time by setting $\overline{E}$ to a high or if $\overline{E_S}$ is high when the rising clock edge occurs. When V_{CC} power is first applied the synchronous enable flip-flop will be in the set condition causing the outputs to be in the high impedance state.

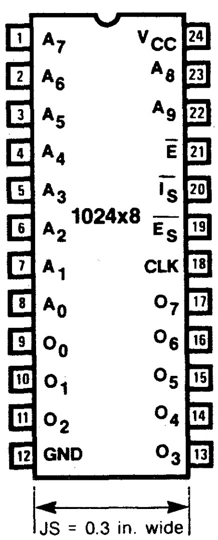
The flexible initialization feature allows start up and time out sequencing with 1:16 programmable words to be loaded into the output registers. With the synchronous INITIALIZE ($\overline{I_S}$) pin low, one of the 16 column words (A_3-A_0) will be set in the output registers independent of the row addresses (A_9-A_4). The unprogrammed state of $\overline{I_S}$ words are low, presenting a CLEAR with $\overline{I_S}$ pin low. With all $\overline{I_S}$ column words (A_3-A_0) programmed to the same pattern, the $\overline{I_S}$ function will be independent of both row and column addressing and may be used as a single pin control. With all $\overline{I_S}$ words programmed high a PRESET function is performed.

Ordering Information

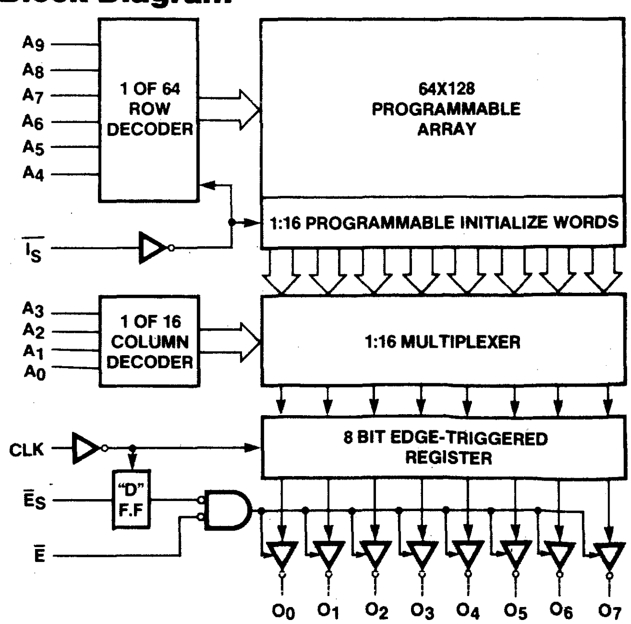
MEMORY		PACKAGE		DEVICE TYPE	
SIZE	PERFORMANCE	PINS	TYPE	MIL	COM
8K	Standard	24	JS, F	53RS881	63RS881
	Enhanced	28	L	53RS881A	63RS881A

* Flat-pack — contact the factory

Pin Configuration



Block Diagram



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Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 to 7V	12V
Input voltage	-1.5 to 7V	7V
Off-state output voltage	-0.5V to 5.5V	12V
Storage temperature	-65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER	TYP	MILITARY 53RS881A MIN	MILITARY 53RS881A MAX	MILITARY 53RS881 MIN	MILITARY 53RS881 MAX	COMMERCIAL 63RS881A MIN	COMMERCIAL 63RS881A MAX	COMMERCIAL 63RS881 MIN	COMMERCIAL 63RS881 MAX	UNIT
t_w	Width of clock (high or low)	10	20		20		20		20		ns
$t_{s(A)}$	Setup time from address to clock	25	40		45		30		35		ns
$t_{s(\overline{E_S})}$	Setup time from $\overline{E_S}$ to clock	8	15		15		15		15		ns
$t_{s(\overline{I_S})}$	Setup time from $\overline{I_S}$ to clock	20	30		35		25		30		ns
$t_{h(A)}$	Hold time address to clock	-5	0		0		0		0		ns
$t_{h(\overline{E_S})}$	Hold time ($\overline{E_S}$)	-3	5		5		5		5		ns
$t_{h(\overline{I_S})}$	Hold time ($\overline{I_S}$)	-5	0		0		0		0		ns
V_{CC}	Supply voltage	5	4.5	5.5	4.5	5.5	4.75	5.25	4.75	5.25	V
T_A	Operating free-air temperature	25	-55	125	-55	125	0	75	0	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18mA			-1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V			-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC}MAX			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 16mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL I_{OH} = -2mA; COM I_{OH} = -3.2mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4V			-40	μA
I_{OZH}	Off-state output current	V_{CC} = MAX	V_O = 2.4V			40	μA
I_{OS}	Output short-circuit current*	V_{CC} = MAX	V_O = 0V	-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX	All inputs TTL; all outputs open.		130	180	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
† Typicals at 5.0V, V_{CC} and 25°C TA.

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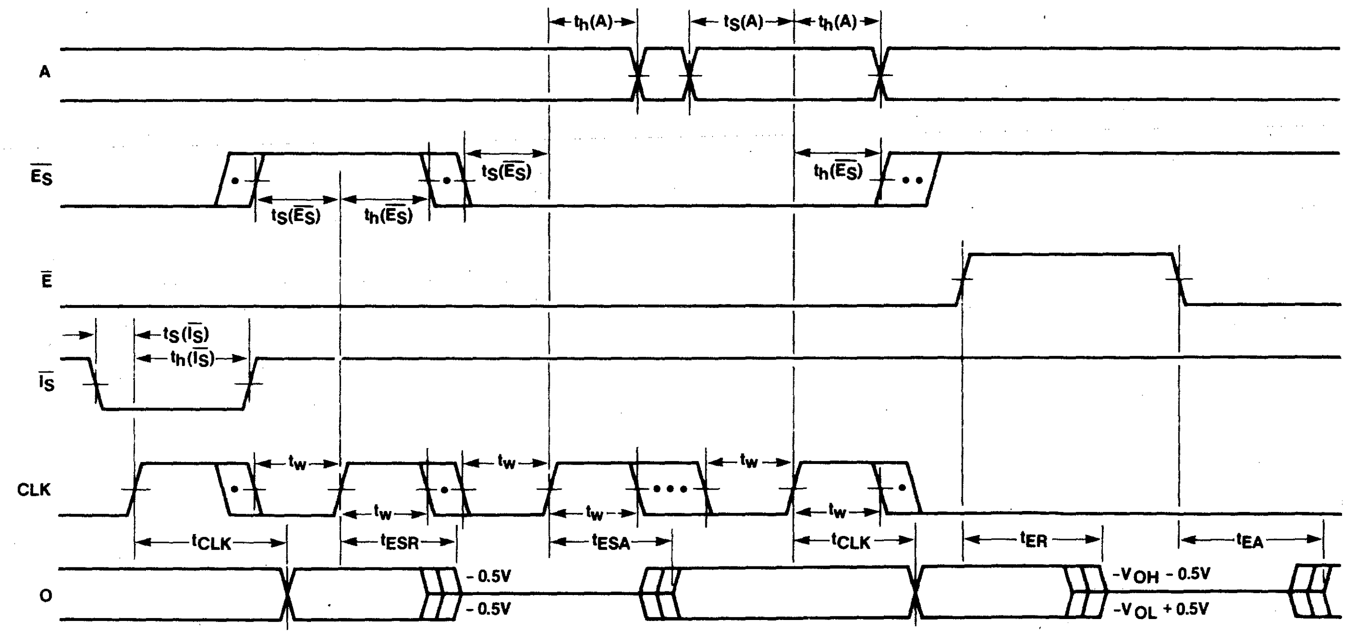
Switching Characteristics Over Operating Conditions and using Standard Test Load

SYMBOL	PARAMETER	TYP	MILITARY				COMMERCIAL				UNIT
			53RS881A		53RS881		63RS881A		63RS881		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CLK}	Clock to output Delay	10		20		25		15		20	ns
t_{ESA}	Clock to output access time ($\overline{E}_S$)	18		30		35		25		30	ns
t_{ESR}	Clock to output recovery time ($\overline{E}_S$)	17		30		35		25		30	ns
t_{EA}	Enable to output access time ($\overline{E}$)	18		30		35		25		30	ns
t_{ER}	Disable to output recovery time ($\overline{E}$)	17		30		35		25		30	ns

Definition of Waveforms



NOTES: 1. Input pulse amplitude 0V to 3.0V.

2. Input rise and fall times 2-5ns from 1.0V to 2.0V.

3. Input access measured at the 1.5V level.

4. t_{AA} is tested with switch S_1 closed. C_L = 30pF and measured at 1.5V output level.

5. t_{EA} and t_{ESA} are measured at the 1.5V output level with C_L = 30pF. S_1 is open for high impedance to "1" test and closed for high impedance to "0" test.

t_{ER} and t_{ESA} are measured C_L = 5pF. S_1 is open for "1" to high impedance test, measured at V_{OH} -0.5V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} +0.5V output level.

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2048x8 Registered Prom with Asynchronous Enable

53/63RA1681 53/63RA1681A

Features/Benefits

- Asynchronous output enable
- Edge-triggered "D" registers
- Versatile 1:16 user programmable initialization words
- 8-bit-wide in 24 pin SKINNYDIP® for high board density
- Simplifies system timing
- Faster cycle times
- 16mA I_{OL} output drive capability
- Reliable titanium-tungsten fuses (Ti-W)

Applications

- Microprogram control store
- State sequencers
- Next address generation
- Mapping PROM

Description

The 53/63RS1681 and 53/63RS1681A are 2 K x 8 PROMs with on chip "D" type registers. Output enable control through an asynchronous enable input and flexible start up sequencing through programmable initialization words.

Ordering Information

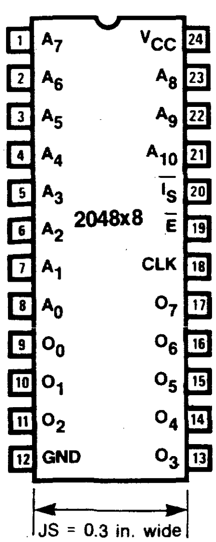
MEMORY		PACKAGE		DEVICE TYPE	
SIZE	PERFORMANCE	PINS	TYPE	MIL	COM
16K	Standard	24	JS	53RA1681	63RA1681
	Enhanced			53RA1681A	63RA1681A

Data is transferred into the output registers on the rising edge of the clock. Provided that the asynchronous ($\overline{E}$) enable is LOW, the data will appear at the outputs. Prior to the positive clock edge, register data are not affected by changes in addressing.

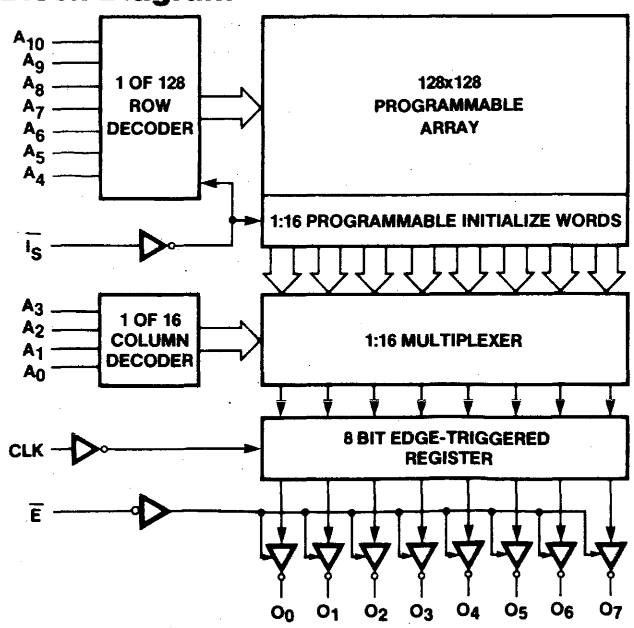
Memory expansion and data control is made flexible with asynchronous enable input. Outputs may be set to the high impedance state at any time by setting $\overline{E}$ to a HIGH.

The flexible initialization feature allows start up and time out sequencing with 1:16 programmable words to be loaded into the output registers. With the synchronous INITIALIZE ($\overline{I_S}$) pin LOW, one of the 16 column words (A_3-A_0) will be set in the output registers independent of the row addresses (A_{10}-A_4). With all $\overline{I_S}$ column words (A_3-A_0) programmed to the same pattern, the $\overline{I_S}$ function will be independent of both row and column addressing and may be used as a single pin control. With all $\overline{I_S}$ words programmed HIGH a PRESET function is performed. The unprogrammed state of $\overline{I_S}$ words are LOW, presenting a CLEAR with $\overline{I_S}$ pin LOW.

Pin Configuration



Block Diagram



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Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5 to 7V	12V
Input voltage	-1.5 to 7V	7V
Off-state output voltage	-0.5V to 5.5V	12V
Storage temperature	-65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER	TYP†	MILITARY 53RA1681A MIN	MILITARY 53RA1681A MAX	MILITARY 53RA1681 MIN	MILITARY 53RA1681 MAX	COMMERCIAL 63RA1681A MIN	COMMERCIAL 63RA1681A MAX	COMMERCIAL 63RA1681 MIN	COMMERCIAL 63RA1681 MAX	UNIT
t_W	Width of clock (high or low)	10	20		20		20		20		ns
$t_{s(A)}$	Setup time from address to clock	28	40		45		35		40		ns
$t_{s(\overline{I_S})}$	Setup time from $\overline{I_S}$ to clock	20	30		35		25		30		ns
$t_{h(A)}$	Hold time address to clock	-5	0		0		0		0		ns
$t_{h(\overline{I_S})}$	Hold time ($\overline{I_S}$)	-5	0		0		0		0		ns
V_{CC}	Supply voltage	5	4.5	5.5	4.5	5.5	4.75	5.25	4.75	5.25	V
T_A	Operating free-air temperature	25	-55	125	-55	125	0	75	0	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2.0			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18mA			-1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V			-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC}MAX			40	µA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 16mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL I_{OH} = -2mA; COM I_{OH} = -3.2mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4V			-40	µA
I_{OZH}	Off-state output current	V_{CC} = MAX	V_O = 2.4V			40	µA
I_{OS}	Output short-circuit current*	V_{CC} = 5.0V	V_O = 0V	-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX	All inputs TTL; all outputs open.		140	185	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

† Typical at 5.0 V V_{CC} and 25° C T_A.

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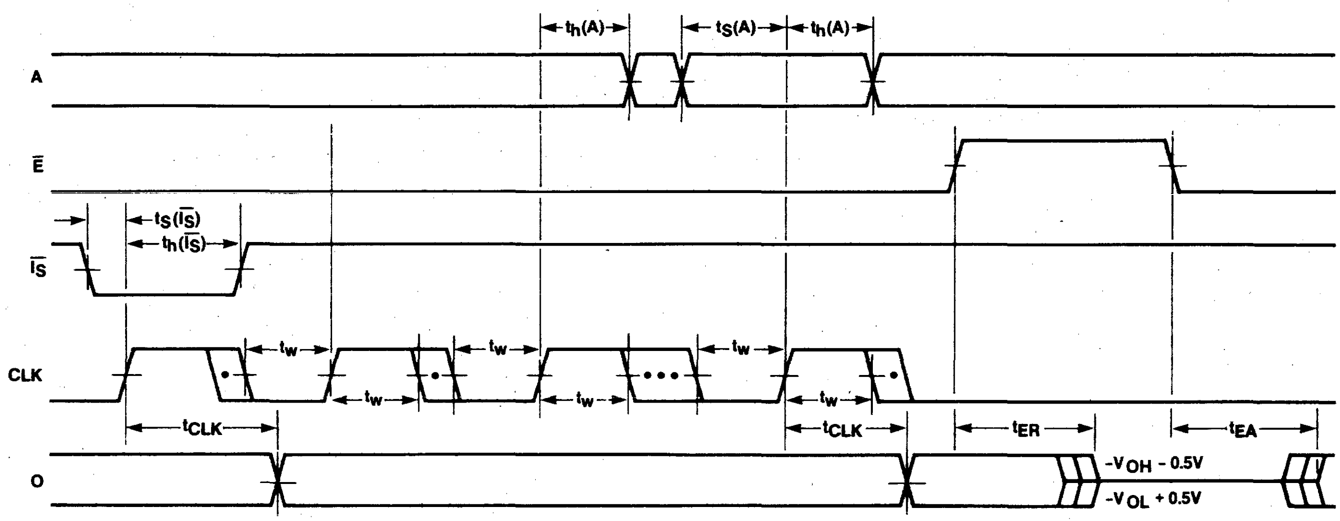
MEMORY

Switching Characteristics Over Operating Conditions and using Standard Test Load

SYMBOL	PARAMETER	TYP†	MILITARY				COMMERCIAL				UNIT
			53RA1681A		53RA1681		63RA1681A		63RA1681		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CLK}	Clock to output Delay	10		20		25		15		20	ns
t_{EA}	Enable to output access time ($\overline{E}$)	15		30		35		25		30	ns
t_{ER}	Disable to output recovery time ($\overline{E}$)	15		30		35		25		30	ns

† Typical at 5.0 V V_{CC} and 25°C T_A.

Definition of Waveforms



NOTES: 1. Input pulse amplitude 0V to 3.0V.

2. Input rise and fall times 2-5ns from 1.0V to 2.0V.

3. Input access measured at the 1.5V level.

4. Switch S_1 is closed, C_L = 30pF and outputs measured at 1.5V level for all tests except t_{EA} and t_{ER}.

5. t_{EA} is measured at the 1.5V output level with C_L = 30 pF. S_1 is open for high impedance to "1" test and closed for high impedance to "0" test.

t_{ER} is tested with C_L = 5pF. S_1 is open for "1" to high impedance test, measured at V_{OH} -0.5V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} +0.5V output level.

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MEMORY

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2048x8 Registered Prom with Synchronous Enable

53/63RS1681 53/63RS1681A

Features/Benefits

- Synchronous output enable
- Edge-triggered "D" registers
- Versatile 1:16 user programmable initialization words
- 8-bit-wide in 24 pin SKINNYDIP® for high board density
- Simplifies system timing
- Faster cycle times
- 16mA I_{OL} output drive capability
- Reliable titanium-tungsten fuses (Ti-W)

Applications

- Microprogram control store
- State sequencers
- Next address generation
- Mapping PROM

Description

The 53/63RS1681 and 53/63RS1681A are 2 K x 8 PROMs with on chip "D" type registers, versatile output enable control through synchronous enable input and flexible start up sequencing through programmable initialization words.

Data is transferred into the output registers on the rising edge of the clock. Provided that the synchronous ($\overline{E}_S$) enable is LOW, the data will appear at the outputs. Prior to the positive clock edge, register data are not affected by changes in addressing or synchronous enable inputs.

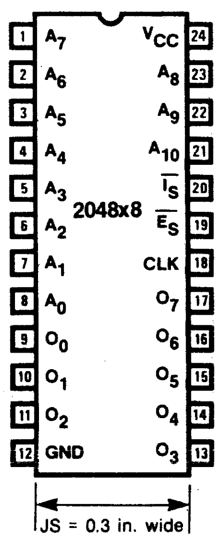
Memory expansion and data control is made flexible with the synchronous enable input. Outputs may be set to the high impedance state by setting $\overline{E}_S$ HIGH before the rising clock edge occurs. When V_{CC} power is first applied the synchronous enable flip-flop will be in the set condition causing the outputs to be in the high impedance state.

The flexible initialization feature allows start up and time out sequencing with 1:16 programmable words to be loaded into the output registers. With the synchronous INITIALIZE ($\overline{I}_S$) pin LOW, one of the 16 column words (A_3-A_0) will be set in the output registers independent of the row addresses (A_{10}-A_4). With all $\overline{I}_S$ column words (A_3-A_0) programmed to the same pattern, the $\overline{I}_S$ function will be independent of both row and column addressing and may be used as a single pin control. With all $\overline{I}_S$ words programmed HIGH a PRESET function is performed. The unprogrammed state of $\overline{I}_S$ words are LOW, presenting a CLEAR with $\overline{I}_S$ pin LOW.

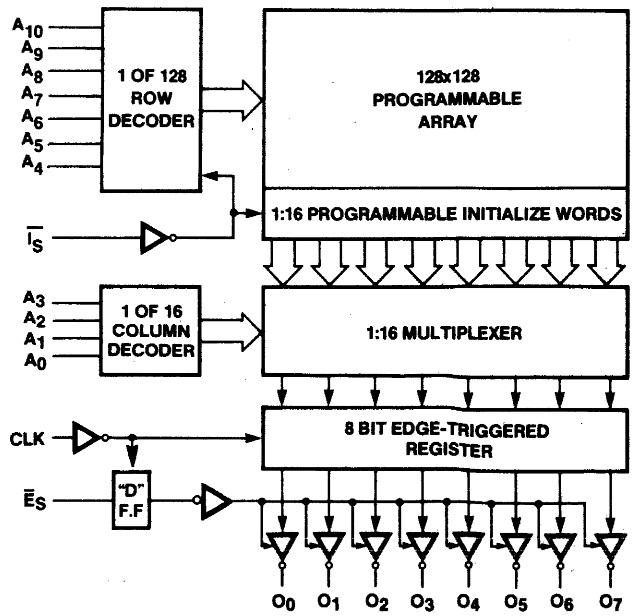
Ordering Information

MEMORY		PACKAGE		DEVICE TYPE	
SIZE	PERFORMANCE	PINS	TYPE	MIL	COM
16K	Standard	24	JS	53RS1681	63RS1681
	Enhanced			53RS1681A	63RS1681A

Pin Configuration



Block Diagram



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Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	−0.5 to 7V	12V
Input voltage	−1.5 to 7V	7V
Off-state output voltage	−0.5V to 5.5V	12V
Storage temperature	−65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER	TYP†	MILITARY				COMMERCIAL				UNIT
			53RS1681A		53RS1681		63RS1681A		63RS1681		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Width of clock (high or low)	10	20		20		20		20		ns
$t_{s(A)}$	Setup time from address to clock	28	40		45		35		40		ns
$t_{s(\overline{E_S})}$	Setup time from $\overline{E_S}$ to clock	7	15		15		15		15		ns
$t_{s(\overline{I_S})}$	Setup time from $\overline{I_S}$ to clock	20	30		35		25		30		ns
$t_{h(A)}$	Hold time address to clock	−5	0		0		0		0		ns
$t_{h(\overline{E_S})}$	Hold time ($\overline{E_S}$)	−3	5		5		5		5		ns
$t_{h(\overline{I_S})}$	Hold time ($\overline{I_S}$)	−5	0		0		0		0		ns
V_{CC}	Supply voltage	5	4.5	5.5	4.5	5.5	4.75	5.25	4.75	5.25	V
T_A	Operating free-air temperature	25	−55	125	−55	125	0	75	0	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2.0			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V			−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC}			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 16mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OH} = −2mA COM I_{OH} = −3.2mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4V			−40	μA
I_{OZH}	Off-state output current	V_{CC} = MAX	V_O = 2.4V			40	μA
I_{OS}	Output short-circuit current*	V_{CC} = 5V	V_O = 0V	−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX	All inputs TTL; all outputs open.		140	185	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
† Typical at 5.0 V V_{CC} and 25°C T_A

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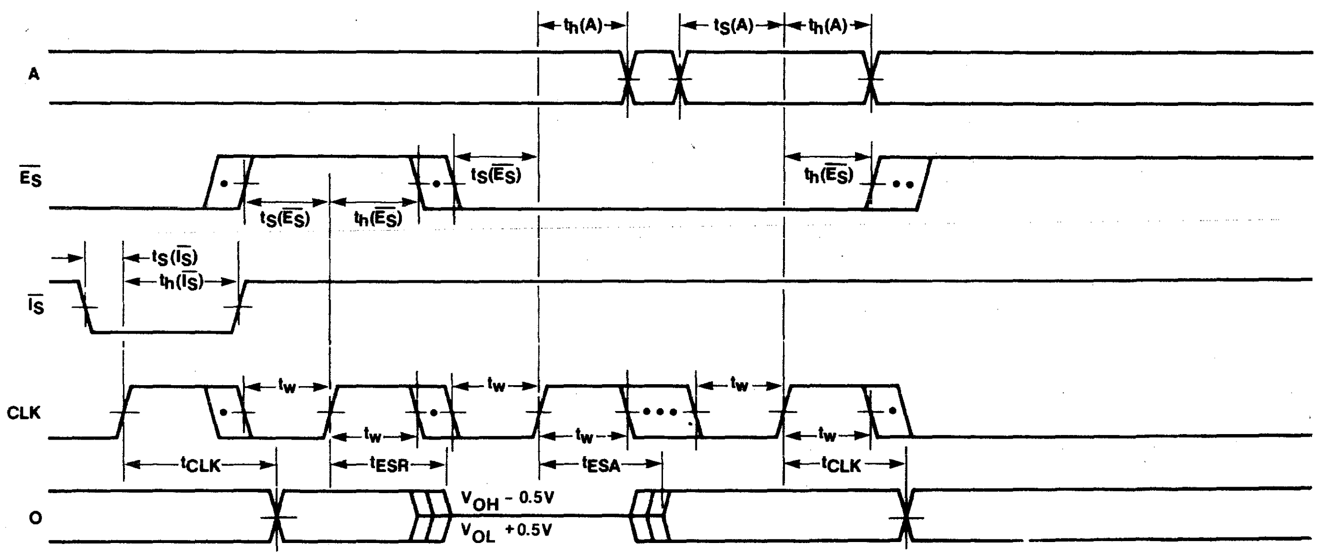
Switching Characteristics Over Operating Conditions and using Standard Test Load

SYMBOL	PARAMETER	TYP†	MILITARY				COMMERCIAL				UNIT
			53RS1681A		53RS1681		63RS1681A		63RS1681		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CLK}	Clock to output Delay	10		20		25		15		20	ns
t_{ESA}	Clock to output access time ($\overline{E}_S$)	15		30		35		25		30	ns
t_{ESR}	Clock to output recovery time ($\overline{E}_S$)	15		30		35		25		30	ns

† Typical at 5.0 V V_{CC} and 25°C T_A.

Definition of Waveforms



NOTES: 1. Input pulse amplitude 0V to 3.0V.

2. Input rise and fall times 2-5ns from 1.0V to 2.0V.

3. Input access measured at the 1.5V level.

4. Switch S_1 is closed, C_L = 30pF and outputs measured at 1.5V level for all tests except t_{ESA} and t_{ESR}.

5. t_{ESA} is measured at the 1.5V output level with C_L = 30pF. S_1 is open for high impedance to "1" test and closed for high impedance to "0" test.

t_{ESR} is tested with C_L = 5pF. S_1 is open for "1" to high impedance test, measured at V_{OH}-0.5V output level; S_1 is closed for "0" to high impedance test measured at V_{OL}+0.5V output level.

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4096x4 Diagnostic Registered PROM with Asynchronous Enable

53D1641 63D1641

Patent Pend.

Features/Benefits

- **Asynchronous output enable**
- **Provides system diagnostic testing for system controllability and observability**
- **Shadow register eliminates shifting hazards**
- **Edge-triggered "D" registers simplifies system timing**
- **Casadable for wide control words used in microprogramming**
- **24-pin SKINNYDIP® saves space**
- **24 mA output drive capability**
- **Replaces embedded diagnostic code**

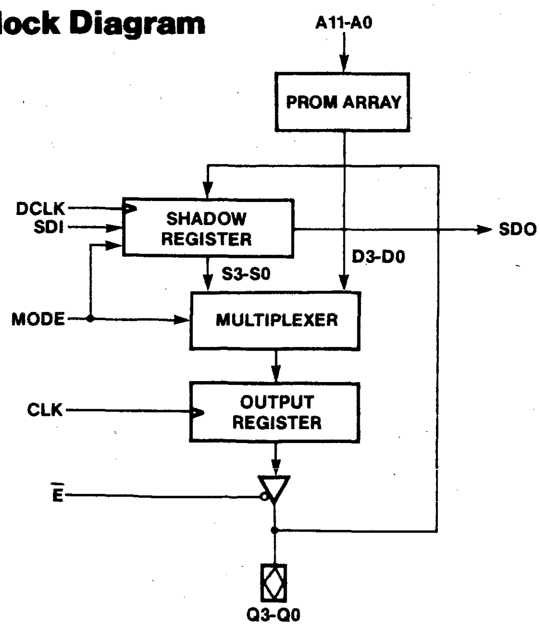
Applications

- **Microprogram control store with built-in system diagnostic testing**
- **Serial character generator**
- **Serial code converter**
- **Parallel in/serial out memory**
- **Cost-effective board testing**

Description

The 53/63D1641 is a 4Kx4 PROM with registered three-state outputs and a shadow register for diagnostic capabilities.

Block Diagram



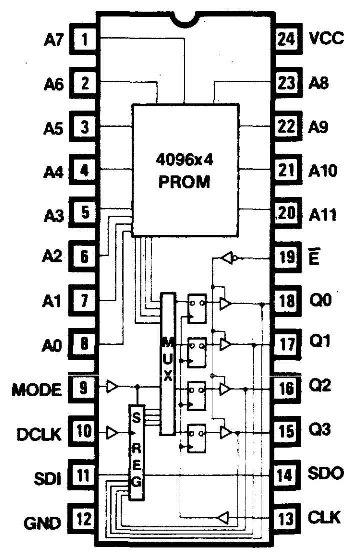
SKINNYDIP® is a registered trademark of Monolithic Memories.

Ordering Information

MEMORY		TEMP.	PACKAGE		PART NO.
SIZE	ORG.		PINS	TYPE	
16K	4096x4	MIL	24	JS	53D1641
		COM			63D1641

Shadow register diagnostics allow observation and control of the system without introducing intermediate illegal states. The output register, which can receive parallel data from either the PROM array or the shadow register, is loaded on the rising edge of CLK. The shadow register, which can receive parallel data from the output register or serial data from SDI, is loaded on the rising edge of DCLK. When the output drivers are disabled, the shadow register receives its parallel data from the output bus. During diagnostics, data loaded into the output register from the PROM array can be parallel-loaded into the shadow register and serially shifted out through SDO, allowing observation of the system. Similarly, diagnostic data can be serially shifted into the shadow register through SDI, and parallel-loaded into the output register, allowing control and test scanning to be imposed on the system. Since the output register and the shadow register are loaded by different input signals, they can be operated independent of one another. In addition, diagnostic PROMs can be cascaded to construct wide control words used in microprogramming.

Logic Symbol



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Function Table

INPUTS				OUTPUTS			OPERATION
MODE	SDI	CLK	DCLK	Q_3-Q_0	S_3-S_0	SDO	
L	X	↑	*	Qn ← PROM	HOLD	S_3	Load output register from PROM array
L	X	*	↑	HOLD	$S_n \leftarrow S_{n-1}$ $S_0 \leftarrow$ SDI	S_3	Shift shadow register data
L	X	↑	↑	Qn ← PROM	$S_n \leftarrow S_{n-1}$ $S_0 \leftarrow$ SDI	S_3	Load output register from PROM array while shifting shadow register data
H	X	↑	*	$Q_n \leftarrow S_n$	HOLD	SDI	Load output register from shadow register
H	L	*	↑	HOLD	$S_n \leftarrow Q_n$	SDI	Load shadow register from output bus
H	H	*	↑	HOLD	HOLD	SDI	No operation†

* Clock must be steady or falling.
† Reserved operation for SN54/74S818 8-Bit Diagnostic Register.

Definition of Signals

MODE The MODE pin controls the output register multiplexer and the shadow register. When MODE is LOW, the output register receives data from the PROM array and the shadow register is configured as a shift register with SDI as its input. When MODE is HIGH, the output register receives data from the shadow register. The shadow register is controlled by SDI as well as MODE. With MODE HIGH and SDI LOW, the shadow register receives parallel data from the output bus. With MODE and SDI both HIGH, the shadow register holds its present data.

SDI The Serial Data In pin is the input to the least significant bit of the shadow register when operating in the shift mode. SDI is also a control input to the shadow register when it is not in the shift mode.

SDO The Serial Data Out pin is the output from the most significant bit of the shadow register when operating in the shift mode. When the shadow register is not in the shift mode, SDO displays the logic level present at SDI, decreasing serial shift time for cascaded diagnostic PROMs.

CLK The clock pin loads the output register on the rising edge of CLK.

DCLK The diagnostic clock pin loads or shifts the shadow register on the rising edge of DCLK.

Q_3-Q_0 Q_n represents the data outputs of the output register. During a shadow register load with outputs enabled these pins are the internal data inputs to the shadow register. With the outputs three-stated these pins are external data inputs to the shadow register.

S_3-S_0 S_n represents the internal shadow register outputs.

A_{11}-A_0 A_n represents the address inputs to the PROM array.

$\overline{E}$ The Output Enable pin operates independent of CLK. When $\overline{E}$ is LOW the outputs are enabled. When $\overline{E}$ is HIGH, the outputs are in the high impedance state.

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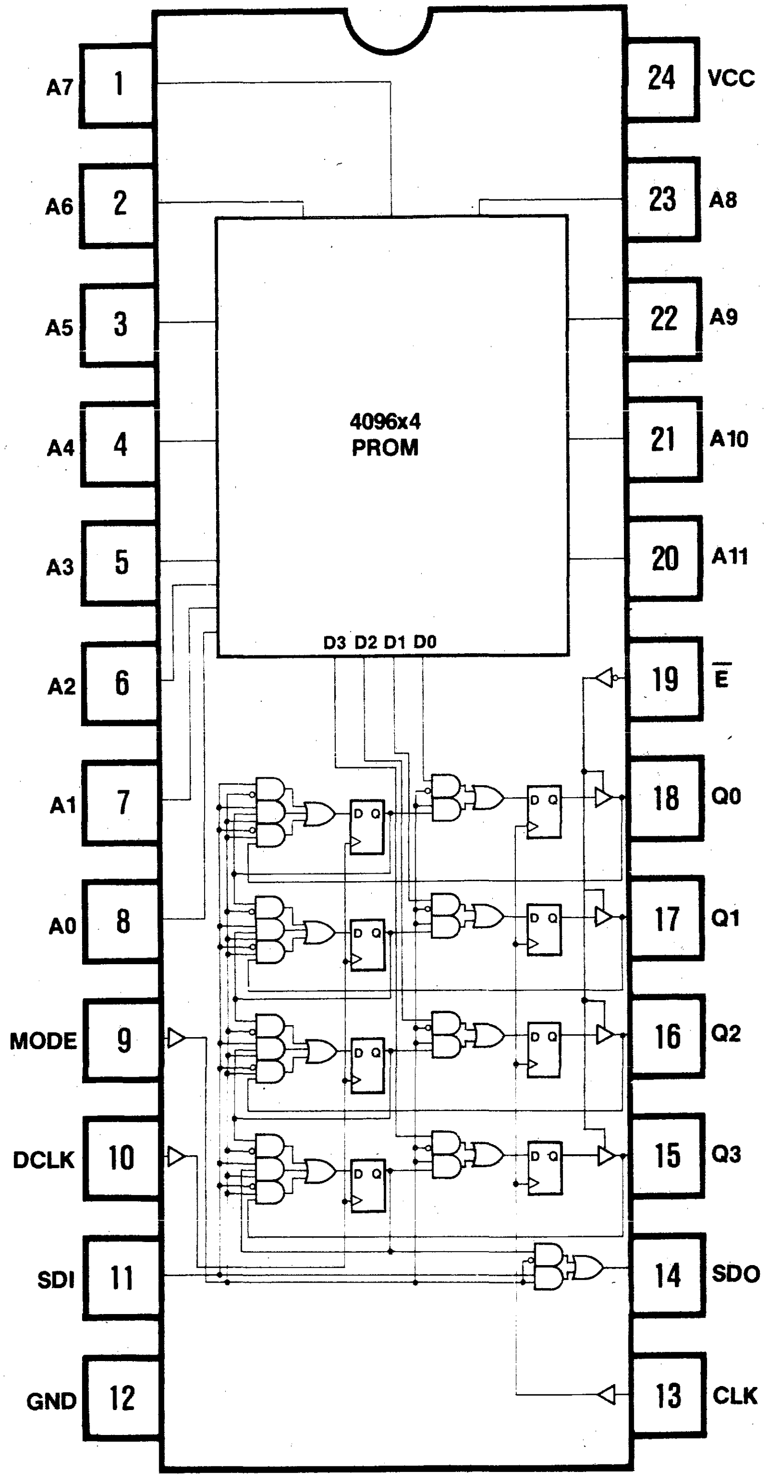
Monolithic Memories

Logic Diagram

4096x4 Diagnostic PROM with Asynchronous Enable



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Monolithic Memories

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	-0.5V to 7V	12V
Input voltage	-1.5V to 7V	7V
Input current	-30mA to +5mA	
Off-state output voltage	-0.5V to 5.5V	12V
Storage temperature	-65°C to +150°C	

Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free air temperature	-55	25	125	0	25	75	°C
t_w	Width of CLK (HIGH or LOW)	25	10		20	10		ns
t_{su}	Set up time from address to CLK	45	25		40	25		ns
t_h	Hold time for CLK	0	-15		0	-15		ns
t_{wd}	Width of DCLK (HIGH or LOW)	45	15		40	15		ns
t_{sud}	Set up time from control inputs (SDI, MODE) to CLK, DCLK	50	20		45	20		ns
t_{hd}	Hold time for DCLK	0	-5		0	-5		ns

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18mA			-1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V			-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	$V_I = V_{CC}$			40	uA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OL} = 16mA COM I_{OL} = 24mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OH} = -2mA COM I_{OH} = -3.2mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4V			-100	uA
I_{OZH}			V_O = 2.4V			40	uA
I_{OS}	Output short-circuit current*	V_{CC} = MAX	V_O = 0V	-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX, All inputs TTL; All outputs open			140	190	mA

† Typical at 5.0V V_{CC} and 25°C T_A.

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Monolithic Memories

MEMORY

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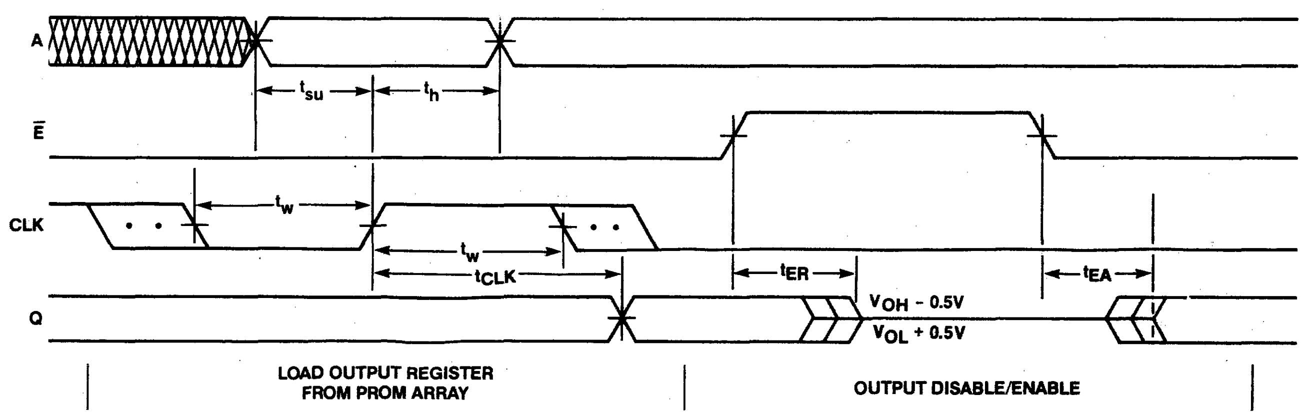
Monolithic Memories

Switching Characteristics Over Operating Conditions and Using Standard Test Load

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP†	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
t_{CLK}	CLK to output		11	25		11	20	ns
t_{ER}	Disable time		16	30		16	25	ns
t_{EA}	Enable time		16	30		16	25	ns
f_{MAXD}	Maximum diagnostic clock frequency	7	18		10	18		MHz
t_{DS}	DCLK to SDO delay (MODE = LOW)		17	35		17	30	ns
t_{SS}	SDI to SDO delay (MODE = HIGH)		16	30		16	25	ns
t_{MS}	MODE to SDO delay		14	30		14	25	ns

† Typical at 5.0V V_{CC} and 25°C T_A.

Definition of Waveforms



NORMAL PROM OPERATION (MODE = LOW)

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Monolithic Memories

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Memory Selector Guide

Motorola has developed a very broad range of reliable MOS and bipolar memories for virtually any digital data processing system application. And for those whose requirements go beyond individual components, Motorola also supplies Memory Systems and Micromodules.

New Motorola memories are being introduced continually. **This selector guide lists all those available as of November 1983.** For later releases, additional technical information or pricing, contact your nearest authorized Motorola distributor or Motorola sales office.

RAMs

MOS DYNAMIC RAMs

Organization	Part Number	Access Time (ns Max)	Power Supplies	No. of Pins
16384 × 1	MCM4116BP15	150	+12, ±5 V	16
16384 × 1	MCM4116BP20	200	+12, ±5 V	16
16384 × 1	MCM4116BP25	250	+12, ±5 V	16
16384 × 1	MCM4517P10	100	+5 V	16
16384 × 1	MCM4517P12	120	+5 V	16
16384 × 1	MCM4517P15	150	+5 V	16
16384 × 1	MCM4517P20	200	+5 V	16
65536 × 1	MCM6664AP15[1]	150	+5 V	16
65536 × 1	MCM6664AP20[1]	200	+5 V	16
65536 × 1	MCM6665AP15	150	+5 V	16
65536 × 1	MCM6665AP20	200	+5 V	16
65536 × 1	MCM6664BP15[1]*	150	+5 V	16
65536 × 1	MCM6664BP20[1]*	200	+5 V	16
65536 × 1	MCM6665BP15*	150	+5 V	16
65536 × 1	MCM6665BP20*	200	+5 V	16

CMOS STATIC RAMs (+5 Volts)

Organization	Part Number	Access Time (ns max)	No. of Pins
2048 × 8	MCM6116P12	120	24
2048 × 8	MCM6116P15	150	24
2048 × 8	MCM6116P20	200	24
4096 × 1	MCM6147P55	55	18
4096 × 1	MCM6147P70	70	18

Operating temperature ranges:
MOS — 0°C to 70°C
ECL — 0°C to 75°C
TTL — Military −55°C to +125°C, Commercial 0°C to 75°C

*To be introduced.
(Not all speed selections shown)

[1]Motorola's innovative pin #1 refresh

[2]300 mil package

MOS STATIC RAMs (+5 Volts)

Organization	Part Number	Access Time (ns max)	No. of Pins
128 × 8	MCM6810	450	24
128 × 8	MCM68A10	360	24
128 × 8	MCM68B10	250	24
1024 × 4	MCM2114P20	200	18
1024 × 4	MCM2114P25	250	18
1024 × 4	MCM2114P30	300	18
1024 × 4	MCM2114P45	450	18
1024 × 4	MCM21L14P20	200	18
1024 × 4	MCM21L14P25	250	18
1024 × 4	MCM21L14P30	300	18
1024 × 4	MCM21L14P45	450	18
2048 × 8	MCM2016HP45	45	24
2048 × 8	MCM2016HN45	45	24[2]
2048 × 8	MCM2016HY45	45	24[2]
2048 × 8	MCM2016HP55	55	24
2048 × 8	MCM2016HN55	55	24[2]
2048 × 8	MCM2016HY55	55	24[2]
2048 × 8	MCM2016HP70	70	24
2048 × 8	MCM2016HN70	70	24[2]
2048 × 8	MCM2016HY70	70	24[2]
16384 × 1	MCM2167HP35	35	20
16384 × 1	MCM2167HL35	35	20
16384 × 1	MCM2167HZ35	35	20
16384 × 1	MCM2167HP45	45	20
16384 × 1	MCM2167HL45	45	20
16384 × 1	MCM2167HZ45	45	20
16384 × 1	MCM2167HP70	70	20
16384 × 1	MCM2167HL70	70	20
16384 × 1	MCM2167HZ70	70	20

TTL RAMs

Organization	Part Number	Access Time (ns max)	Output	No. of Pins
1024 × 1	MCM93415	45	O.C.	16
1024 × 1	MCM93425	45	3-State	16
256 × 4	MCM93L422	60	3-State	22
256 × 4	MCM93L422A	45	3-State	22
256 × 4	MCM93422	45	3-State	22
256 × 4	MCM93422A	35	3-State	22

RAMs (continued)

ECL 10K, 10KH RAMs

Organization	Part Number	Access Time (ns max)	No. of Output	Pins
8×2	MCM10143	15.3	O.E.	24
16×4	MC10H145	6	O.E.	16
16×4	MCM10145	15	O.E.	16
64×1	MCM10148	15	O.E.	16
128×1	MCM10147	15	O.E.	16
256×1	MCM10144	26	O.E.	16
256×1	MCM10152	15	O.E.	16
1024×1	MCM10146	29	O.E.	16
1024×1	MCM10415-20	20	O.E.	16
1024×1	MCM10415-15	15	O.E.	16
1024×1	MCM10415-10	10	O.E.	16
256×4	MCM10422-15	15	O.E.	24
256×4	MCM10422-10	10	O.E.	24
4096×1	MCM10470-25	25	O.E.	18
4096×1	MCM10470-15	15	O.E.	18
1024×4	MCM10474-25	25	O.E.	24
1024×4	MCM10474-15	15	O.E.	24
16384×1	MCM10480-20*	20	O.E.	20
4096×4	MCM10484-20*	20	O.E.	28

ECL 100K RAMs

1024×1	MCM100415-10*	10	O.E.	16
256×4	MCM100422-10*	10	O.E.	24
4096×1	MCM100470-15*	15	O.E.	18
1024×4	MCM100474-15*	15	O.E.	24
16384×1	MCM100480-20*	20	O.E.	20
4096×4	MCM100484-20*	20	O.E.	28

EPROMs

MOS EPROMs

Organization	Part Number	Access Time (ns max)	Power Supplies	No. of Pins
8192×8	MCM68764C	450	+5 V	24
8192×8	MCM68766C	450	+5 V	24
8192×8	MCM68766C35	350	+5 V	24

Operating temperature ranges:
MOS – 0°C to 70°C
ECL – 0°C to 75°C
TTL – Military −55°C to +125°C, Commercial 0°C to 75°C

*To be introduced.
(Not all speed selections shown)

PROMs

ECL PROMs

Organization	Part Number	Access Time (ns max)	No. of Pins
32×8	MCM10139	20	16
256×4	MCM10149	25	16
256×4	MCM10149A*	15	16

TTL PROMs (3-State Outputs)

Organization	Part Number	Access Time (ns max)	No. of Pins
32×8	MCM27S19*	25	16
512×4	MCM7621	70	16
512×4	MCM7621A	60	16
512×8	MCM7641	70	24
512×8	MCM7641A	60	24
512×8	MCM7649	60	20
512×8	MCM7649A	45	20
512×8	MCM27S29*	35	20
512×8	MCM27S31*	35	24
512×8	MCM27S25*	See Note 3	24
512×8	MCM27S27*	See Note 3	22
1024×4	MCM7643	70	18
1024×4	MCM7643A	50	18
1024×8	MCM7681	70	24
1024×8	MCM7681A	50	24
1024×8	MCM27S181*	35	24[4]
1024×8	MCM27S281*	35	24[2]
1024×8	MCM27S35[5]*	See Note 3	24
1024×8	MCM27S37[6]*	See Note 3	24
2048×4	MCM7685	70	18
2048×4	MCM7685A	55	18
2048×8	MCM76161	70	24
2048×8	MCM76161A	50	24
2048×8	MCM27S191	35	24[4]
2048×8	MCM27S291	35	24[2]
2048×8	MCM27S45[5]	See Note 3	24
2048×8	MCM27S47[6]	See Note 3	24
4096×4	MCM76165	35	20

[2] 300 mil package

[3] Registered Outputs – 20 ns max clock to output
35 ns max address to clock setup time

[4] 600 mil package

[5] Asynchronous register

[6] Synchronous register

Motorola Semiconductor

MEMORY

MOTOROLA *Semiconductor Products Inc.*

ROMs

MOS STATIC ROMs (+5 Volts)

Character Generators[7]

Organization	Part Number	Access Time (ns max)	No. of Pins
128×(7×5)	MCM6670P	350	18
128×(7×5)	MCM6674P	350	18
128×(9×7)	MCM66700P	350	24
128×(9×7)	MCM66710P	350	24
128×(9×7)	MCM66714P	350	24
128×(9×7)	MCM66720P	350	24
128×(9×7)	MCM66730P	350	24
128×(9×7)	MCM66734P	350	24
128×(9×7)	MCM66740P	350	24
128×(9×7)	MCM66750P	350	24
128×(9×7)	MCM66760P	350	24
128×(9×7)	MCM66770P	350	24
128×(9×7)	MCM66780P	350	24
128×(9×7)	MCM66790P	350	24

MOS Binary ROMs (+5 Volts)

Organization	Part Number	Access Time (ns max)	No. of Pins
2048×8	MCM68A316EP	350	24
2048×8	MCM68A316EP91[8]	350	24
4096×8	MCM68A332P	350	24
4096×8	MCM68A332P2[3]	350	24
8192×8	MCM68364P35	350	24
8192×8	MCM68364P35-3[8]	350	24
8192×8	MCM68364P25	250	24
8192×8	MCM68364P20	200	24
8192×8	MCM68365P25	250	24
8192×8	MCM68365P35	350	24
8192×8	MCM68366P25	250	24
8192×8	MCM68366P35	350	24
16384×8	MCM63128P15	150	28
16384×8	MCM63128P20	200	28
32768×8	MCM63256P15	150	28
32768×8	MCM63256P20	200	28

CMOS ROMs (+5 Volts)

Organization	Part Number	Access Time (ns max)	No. of Pins
256×4	MCM14524	1200	16
2048×8	MCM65516P43	430	18
2048×8	MCM65516P43M[8]	430	18
2048×8	MCM65516P55	550	18

Operating temperature ranges:
- MOS — 0°C to 70°C
- ECL — 0°C to 75°C
- TTL — Military −55°C to +125°C, Commercial 0°C to 75°C

*To be introduced.
(Not all speed selections shown)

[7]Character generators include shifted and unshifted characters, ASCII alphanumeric control, math, Japanese British, German, European and French symbols.

[8]Standard Patterns for MOS ROMs:
- MCM68A316EP91 — Universal Code Converter and Character Generator
- MCM68A332P2 — Sine/Cosine Look-Up Table
- MCM68364P35-3 — Log/Antilog Look-Up Table
- MCM65516P43M — MC146805 Monitor Program

Motorola Semiconductor

MEMORY

MOTOROLA Semiconductor Products Inc.

MOTOROLA

SEMICONDUCTORS

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MCM4517

Advance Information

16,384-BIT DYNAMIC RAM

The MCM4517 is a 16,384-bit, high-speed, dynamic Random-Access Memory. Organized as 16,384 one-bit words and fabricated using HMOS high-performance, N-channel, silicon-gate technology. This new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

By multiplexing row- and column-address inputs, the MCM4517 requires only seven address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by $\overline{CAS}$ allowing for greater system flexibility.

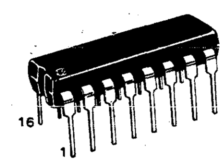
All inputs and outputs, including clocks, are fully TTL compatible. The MCM4517 incorporates a one-transistor cell design and dynamic storage techniques.

- Organized as 16,384 Words of 1 Bit
- Single +5 Volt Operation
- Fast 100 ns Operation
- Low Power Dissipation:
  170 mW Maximum (Active)
  14 mW Maximum (Standby)
- Maximum Access Time
  MCM4517-10 — 100 ns
  MCM4517-12 — 120 ns
  MCM4517-15 — 150 ns
  MCM4517-20 — 200 ns
- Three-State Data Output
- Internal Latches for Address and Data Input
- Early-Write Common I/O Output Capability
- 64K Compatible 128-cycle, 2 ms Refresh
- $\overline{RAS}$-only Refresh Mode
- $\overline{CAS}$ Controlled Output
- Upward Pin Compatibility from the 16K RAM (MCM4116) to the 64K RAM (MCM6664)
- Allows Undershoot V_{IL} min = −2 V
- Hidden $\overline{RAS}$ Only Refresh Capability

MOS

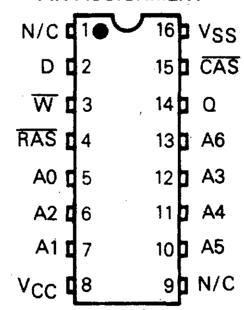
(N-CHANNEL, SILICON-GATE)

16,384-BIT DYNAMIC RAM



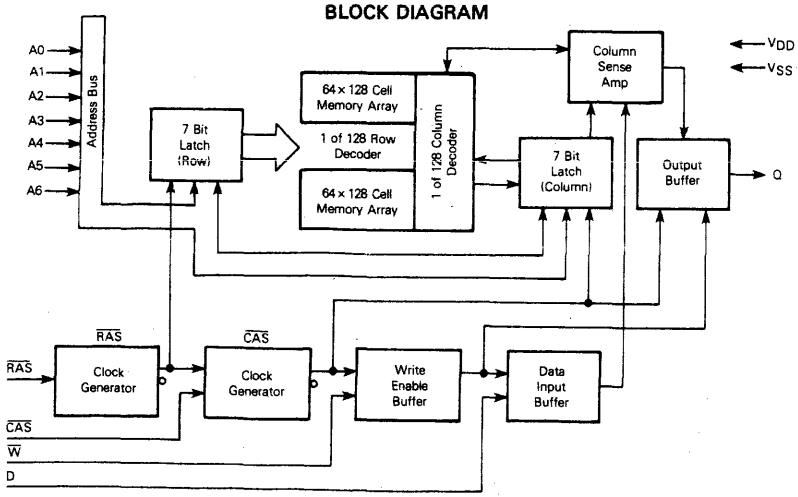
P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



PIN NAMES	
A0-A6	Address Input
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

 ADI-836-R2

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MCM6665B

Advance Information

64K BIT DYNAMIC RAM

The MCM6665B is a 65,536-bit, high-speed, dynamic Random-Access Memory. It is organized as 65,536 one-bit words and fabricated using HMOS high-performance N-channel silicon-gate technology, and is a yield enhanced version of our popular MCM6664A, featuring a smaller die size and redundancy.

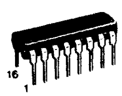
By multiplexing row- and column-address inputs, the MCM6665B requires only eight address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by CAS allowing for greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM6665B incorporates a one-transistor cell design and dynamic storage techniques.

- Organized as 65,536 Words of 1 Bit
- Single 5 V Operation (± 10%)
- Maximum Access Time
  MCM6665B-15 = 150 ns
  MCM6665-20 = 200 ns
- Low Power Dissipation
  302.5 mW Maximum (Active) MCM6665B-15)
  22 nW Maximum (Standby)
- Three-State Data Output
- Internal Latches for Address and Data Input
- Early-Write Common I/O Capability
- 16K Compatible 128-Cycle, 2 ms Refresh
- $\overline{RAS}$-only Refresh Mode
- $\overline{CAS}$ Controlled Output
- Upward Pin Compatible from the 16K RAM (MCM4116, MCM4517)
- Fast Page Mode Cycle Time

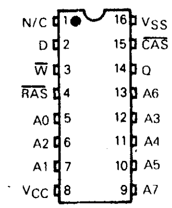
MOS
(N-CHANNEL, SILICON-GATE)

65,536-BIT DYNAMIC RANDOM ACCESS MEMORY



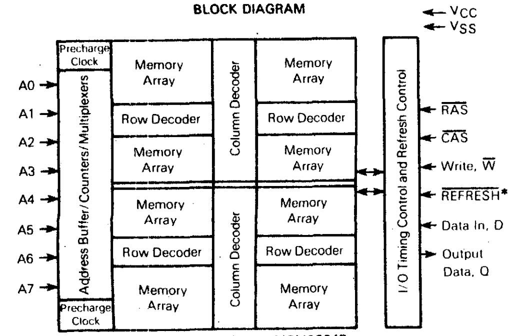
P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



PIN NAMES	
A0-A7	Address Input
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
VCC	Power (+5 V)
VSS	Ground

BLOCK DIAGRAM



*Refresh Function Available on MCM6664B

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

 ADI-981-R1

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MCM6665C

Product Preview

64K BIT DYNAMIC RAM

The MCM6665C is a 65,536-bit, high-speed, dynamic Random-Access Memory. Organized as 65,536 one-bit words and fabricated using HMOS high-performance N-channel silicon-gate technology, this new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

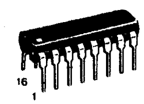
By multiplexing row- and column-address inputs, the MCM6665C requires only eight address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by $\overline{CAS}$, allowing for greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM6665C incorporates a one-transistor cell design and dynamic storage techniques.

- Organized as 65,536 Words of 1 Bit
- Single + V Operation (± 10%)
- Full Power Supply Range Capabilities
- Maximum Access Time
  MCM6665C-12 = 120 ns
  MCM6665C-15 = 150 ns
  MCM6665C-20 = 200 ns
- Low Power Dissipation
- Three-State Data Output
- Internal Latches for Address and Data Input
- Early-Write Common I/O Capability
- 16K Compatible 128-Cycle, 2 ms Refresh
- $\overline{RAS}$-only Refresh Mode
- CAS Controlled Ouput
- Upward Pin Compatible from the 16K RAM (MC4116, MCM4517)
- Fast Page Mode Cycle Time
- Redundancy Added

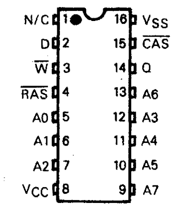
MOS
(N-CHANNEL, SILICON-GATE)

65, 536-BIT DYNAMIC RANDOM ACCESS MEMORY



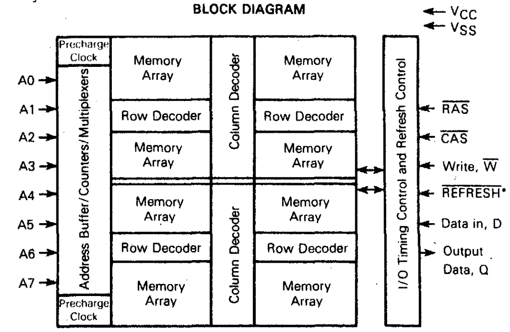
P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



PIN NAMES	
A0-A7	Address Input
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
VCC	Power (+5 V)
VSS	Ground

BLOCK DIAGRAM



*Refresh Function Available on MCM6664C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltages to this high-impedance circuit.

This document contains information on a new product. Specifications and herein are subject to change without notice.

 AD1-999

MOTOROLA

SEMICONDUCTORS

3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MCM6256

Product Preview

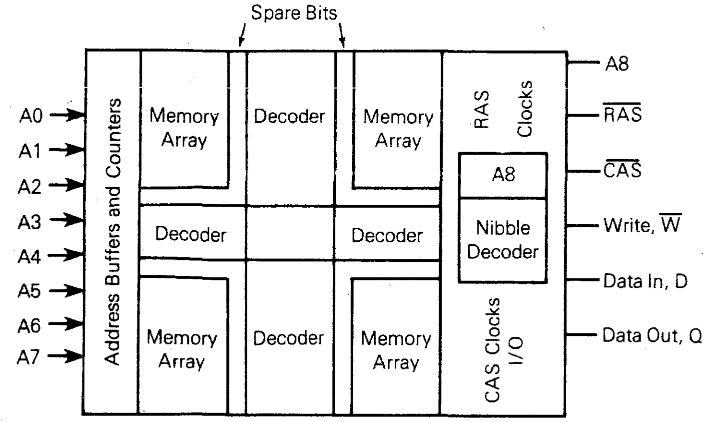
256K-BIT DYNAMIC RAM

The MCM6256 is a 262,144 bit, high-speed, dynamic Random Access Memory. Organized as 262,144 one-bit words and fabricated using Motorola's high-performance silicon-gate MOS (HMOS) technology, this new single +5 volt supply dynamic RAM combines high performance with low cost and improved reliability. The MCM6256 has the capability of using laser fuse redundancy and is manufactured using advanced direct-step on wafer photolithographic equipment.

By multiplexing row and column address inputs, the MCM6256 requires only nine address lines and permits packaging in standard 16-pin 300 mil wide dual-in-line packages. Complete address decoding is done on-chip with address latches incorporated. Data out (Q) is controlled by $\overline{CAS}$ allowing greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM6256 incorporates a one transistor cell design and dynamic storage techniques. In addition to the $\overline{RAS}$-only refresh mode, a $\overline{CAS}$ before $\overline{RAS}$ automatic refresh is available. Another special feature of the MCM6256 is nibble mode, allowing the user to serially access 4 bits of data at a high data rate. Nibble mode address is controlled by the addresses on pin 1 (A8 row and A8 column).

- Organized as 262,144 Words of 1 Bit
- Single +5 Volt Operation (±10%)
- Maximum Access Time:
  MCM6256-10 = 100 ns
  MCM6256-12 = 120 ns
  MCM6256-15 = 150 ns
- Low Power Dissipation:
  70 mA maximum (Active) MCM6256-10
  4 mA maximum (Standby)
- Three-State Data Output
- Early-Write Common I/O Capability
- 256 Cycle, 4 ms Refresh
- $\overline{RAS}$-Only Refresh Mode
- Automatic ($\overline{CAS}$ before $\overline{RAS}$) Refresh Mode
- Fast Nibble Mode on Read and Write Cycles
  20 ns Access Time
  40 ns Cycle Time

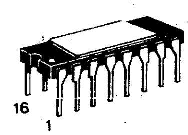


This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MOS

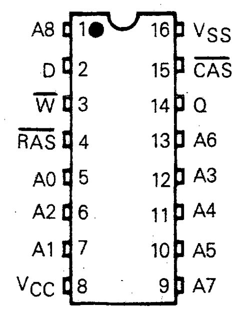
(N-CHANNEL, SILICON-GATE)

262,144 BIT DYNAMIC RANDOM ACCESS MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 690

PIN ASSIGNMENT



PIN NAMES	
A0-A8	Address Input
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

MOTOROLA SEMICONDUCTORS

3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MCM2016H

Advance Information

MOS

(N-CHANNEL, SILICON-GATE)

2,048 × 8 BIT STATIC RANDOM ACCESS MEMORY

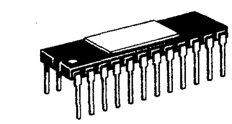
FAST 16K BIT STATIC RAM

The MCM2016H is a 16,384-bit Static Random Access Memory organized as 2048 words by 8 bits, fabricated using Motorola's High-performance silicon-gate MOS (HMOS) technology. It uses an innovative design approach which combines the ease-of-use features of fully static operation (no external clocks or timing strobes required) with the reduced standby power dissipation associated with clocked memories. To the user this means low standby power dissipation without the need for address setup and hold times, nor reduced data rates due to cycle times that are no longer than access times. Perfect for cache and sub-100 ns buffer memory systems, this high speed static RAM is intended for applications that demand superior performance and reliability.

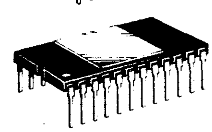
Chip Enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. In less than a cycle time after chip enable ($\overline{E}$) goes high, the part automatically reduces its power requirements and remains in this low-power standby mode as long as the chip enable ($\overline{E}$) remains high. This feature provides significant system-level power savings.

The MCM2016H is in a 24-pin dual-in-line 600 mil wide package with the industry standard JEDEC approved pinout and is pinout compatible with the industry standard 16K EPROM/ROM. A 24 pin dual-in-line 300 mil wide package will also be available.

- Single +5 Volt Operation (±10%)
- Fully Static: No Clock or Timing Strobe Required
- Fast Access Time: MCM2016H-45 — 45 ns (max)
  MCM2016H-55 — 55 ns (max)
  MCM2016H-70 — 70 ns (max)
- Power Dissipation: 120 mA Maximum (Active)
  20 mA Maximum (Standby)
- Three-State Output



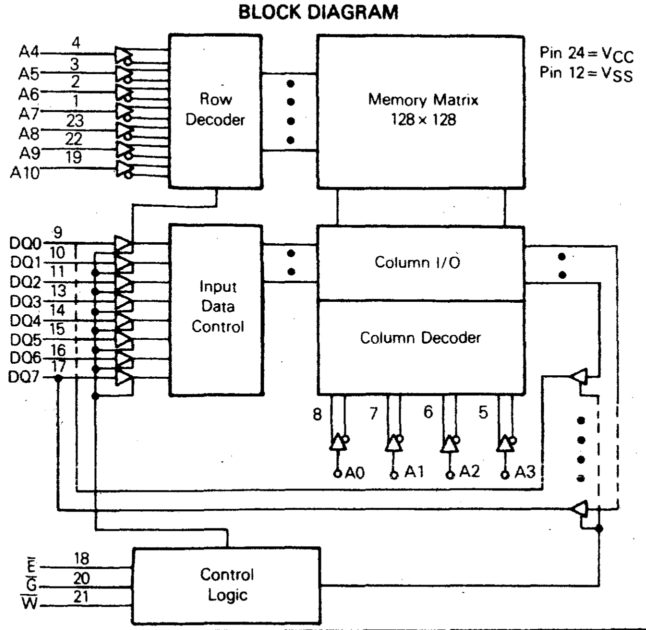
Y SUFFIX
CERAMIC PACKAGE
CASE 716-08



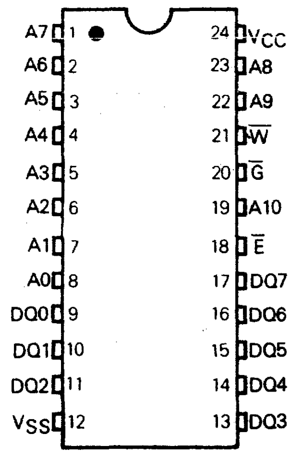
L SUFFIX
CERAMIC PACKAGE
CASE 716-06

P SUFFIX PLASTIC PACKAGE ALSO AVAILABLE — CASE 709

BLOCK DIAGRAM



PIN ASSIGNMENTS



PIN NAMES	
A0-A10	Address Input
DQ0-DQ7	Data Input/Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
V_{CC}	Power (+5 V)
V_{SS}	Ground

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ADI-951-R1

MOTOROLA
SEMICONDUCTORS
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MCM2167H

Advance Information

FAST 16K BIT STATIC RAM

The MCM2167H is a 16,384-bit Static Random Access Memory organized as 16,384 words by 1 bit, fabricated using Motorola's High-performance silicon-gate MOS (HMOS) technology. It uses an innovative design approach which combines the ease-of-use features of fully static operation (no external clocks or timing strobes required) with the reduced standby power dissipation associated with clocked memories. To the user this means low standby power dissipation without the need for address setup and hold times, nor reduced data rates due to cycle times that are no longer than access times. Perfect for cache and sub-100 ns buffer memory systems, this high speed static RAM is intended for applications demanding superior performance and reliability.

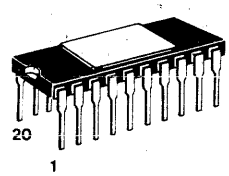
Chip Enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. In less than a cycle time after Chip Enable ($\overline{E}$) goes high, the part automatically reduces its power requirements and remains in this low-power standby mode as long as the Chip Enable ($\overline{E}$) remains high. This feature provides significant system-level power savings.

The MCM2167H is in a 20 pin dual-in-line package with the industry standard pinout. It is TTL compatible in all respects. The data out has the same polarity as the input data. A data input and a separate three-state output provide flexibility and allow easy OR-ties.

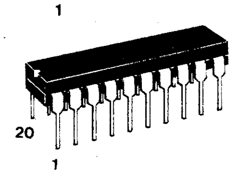
- Single +5 V Operation (± 10%)
- Fully Static Memory — No Clock or Timing Strobe Required
- Fast Access Time: MCM2167H-35 — 35 ns Max.
  MCM2167H-45 — 45 ns Max.
- Power Dissipation: 120 mA Maximum (Active)
  20 mA Maximum (Standby)
- Low Power Also Available: MCM21L67H
- Automatic Power Down

MOS
(N-CHANNEL, SILICON-GATE)

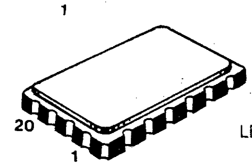
16,384-BIT STATIC RANDOM ACCESS MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 729

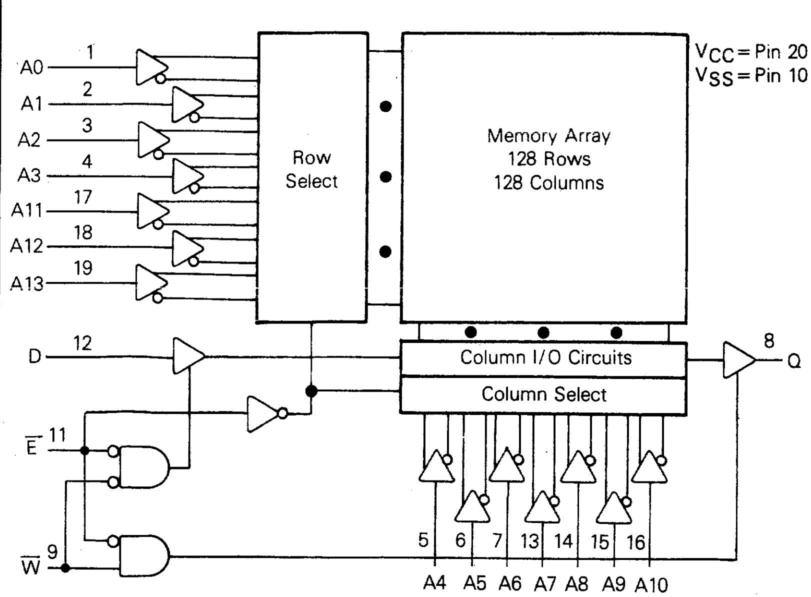


P SUFFIX
PLASTIC PACKAGE
CASE 738

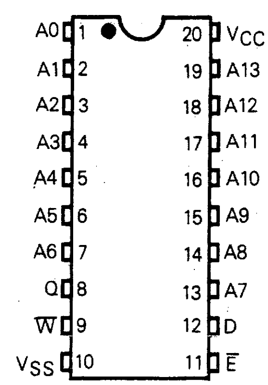


Z SUFFIX
LEADLESS CHIP CARRIER
CASE 756B

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES	
A0-A13	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D	Data Input
Q	Data Output
V_{CC}	Power (+5 V)
V_{SS}	Ground

 ADI-980

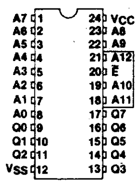
MOTOROLA
SEMICONDUCTORS

3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

Nonvolatile Memories

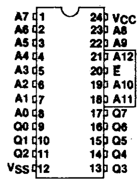
24 PIN-COMPATIBLE 64K ROM FAMILY

MCM68364



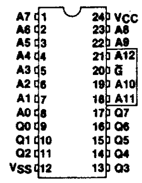
- EDGE ACTIVATED
- POWER DOWN
- ADDRESS LATCH

MCM68365



- FULLY STATIC
- POWER DOWN
- $t_{ACC} = t_{CYCLE}$

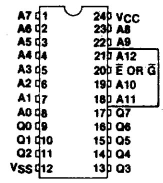
MCM68366



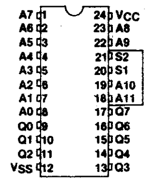
- FULLY STATIC
- OUTPUT ENABLE
- FAST ACCESS

24 PIN-COMPATIBLE 64K ROM FAMILY (CONTINUED)

MCM68364/5/6

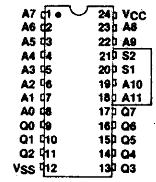


MCM68367



- FULLY STATIC
- PAGE MODE

MCM68368



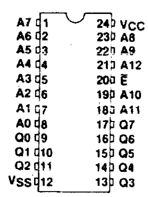
- FULLY STATIC
- BANK SELECT

MCM68365

CHARACTERISTICS

- 8192 × 8 MASK PROGRAMMABLE ROM
- SINGLE +5 VOLT 10% SUPPLY
- PIN COMPATIBLE WITH 8K, 16K, AND 32K ROMs
- FULLY STATIC OPERATION
- AUTOMATIC POWER DOWN
- LOW POWER DISSIPATION
  225 mW ACTIVE (TYPICAL)
  30 mW STANDBY (TYPICAL)
- MAXIMUM ACCESS TIMEs:
  68365C30 — 300 ns
  68365C35 — 350 ns

PINOUT

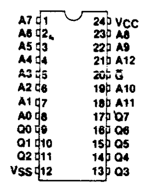


MCM68366

CHARACTERISTICS

- 8192 × 8 MASK PROGRAMMABLE ROM
- SINGLE +5 VOLT 10% SUPPLY
- INDUSTRY STANDARD 24 PIN PACKAGE
- FULLY STATIC OPERATION (NO CLOCKS OR STROBES)
- FAST 150 ns ACCESS TIME FROM OUTPUT ENABLE
- LOW POWER DISSIPATION
  225 mW ACTIVE (TYPICAL)
- FULLY TTL COMPATIBLE
- MASK PROGRAMMABLE OUTPUT ENABLE
- PIN COMPATIBLE WITH MCM68766 (64K EPROM)

PINOUT

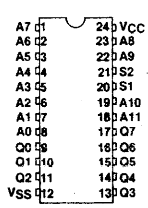


MCM68367

CHARACTERISTICS

- 8K × 8 HMOS MASK PROGRAMMABLE ROM
- PAGE MODE — ACCESS TOP HALF OR BOTTOM HALF OF THE 4K BYTES
- APPEARS TO OUTSIDE WORLD AS 4K × 8 STANDARD ROM
- FULLY STATIC OPERATION (NO CLOCKS)
- SUPPLY CURRENT
  100 mA ACTIVE (MAX)
- MAXIMUM ACCESS TIME — 450 ns
- PROGRAM LAYER LATE IN PROCESS

PINOUT

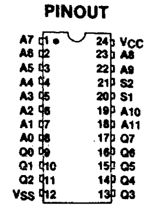


MCM68368

CHARACTERISTICS

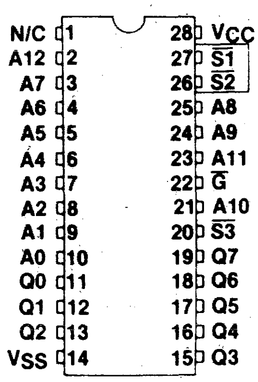
- 8K × 8 HMOS MASK PROGRAMMABLE ROM
- MEMORY IS DIVIDED INTO EIGHT 1K × 8 BYTES WHICH ARE SELECTED BY INDIRECT ADDRESSING
- APPEARS TO OUTSIDE WORLD AS 4K × 8 ROM STANDARD PACKAGE
- FULLY STATIC OPERATION (NO CLOCKS)
- SUPPLY CURRENT
  125 mA ACTIVE (MAX)
- MAX ACCESS TIME — 450 ns
- PROGRAM LAYER LATE IN PROCESS

PINOUT



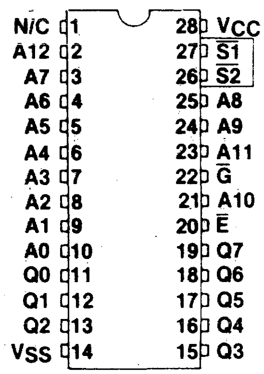
28 PIN-COMPATIBLE ROM FAMILY

MCM68369



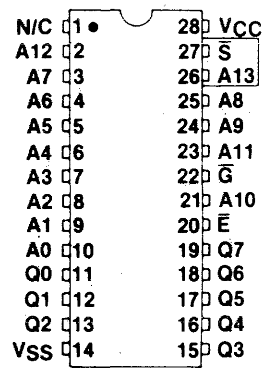
- 64K (8K × 8)

MCM68370



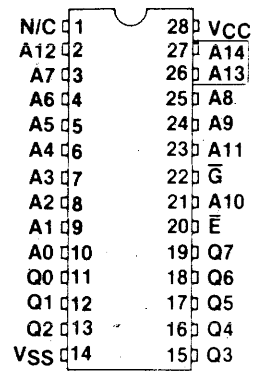
- 64K (8K × 8)

MCM63128



- 128K (16K × 8)

MCM63256



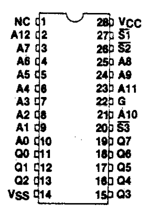
- 256K (32K × 8)

MCM68369

CHARACTERISTICS

- 8K × 8 NMOS MASK PROGRAMMABLE ROM
- INDUSTRY STANDARD 28 PIN PACKAGE
- FULLY STATIC OPERATION (NO CLOCKS OR STROBES)
- SUPPLY CURRENT
  100 mA ACTIVE (MAXIMUM)
- MAXIMUM ACCESS TIME — 350 ns
- MASK PROGRAMMABLE CHIP SELECTS AND OUTPUT ENABLE
- PROGRAM LAYER LATE IN PROCESS

PINOUT

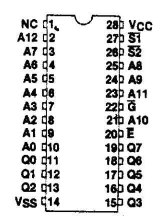


MCM68370

CHARACTERISTICS

- 8K × 8 NMOS MASK PROGRAMMABLE ROM
- INDUSTRY STANDARD 28 PIN PACKAGE
- FULLY STATIC OPERATION (NO CLOCKS OR STROBES)
- SUPPLY CURRENT
  100 mA ACTIVE (MAXIMUM)
  15 mA STANDBY (MAXIMUM)
- MAXIMUM ACCESS TIME — 350 ns
- MASK PROGRAMMABLE CHIP ENABLE, OUTPUT ENABLE, AND CHIP SELECTS
- PROGRAM LAYER LATE IN PROCESS

PINOUT

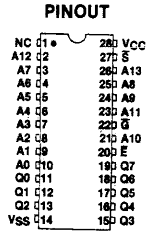


MCM63128

CHARACTERISTICS

- 16K × 8 HMOS MASK PROGRAMMABLE ROM
- INDUSTRY STANDARD 28 PIN PACKAGE
- FULLY STATIC OPERATION (NO CLOCKS OR STROBES)
- SUPPLY CURRENT
  100 mA ACTIVE (MAXIMUM)
  15 mA STANDBY (MAXIMUM)
- MAXIMUM ACCESS TIME — 200 ns
- MASK PROGRAMMABLE CHIP AND OUTPUT ENABLES
- PROGRAM LAYER LATE IN PROCESS
- THE FUNCTIONS $\overline{E}$ AND $\overline{S}$ ON PINS 20 AND 27 CAN BE INTERCHANGED AT USER OPTION
- $\overline{G}$ CAN BE ORed OR ANDed WITH $\overline{S}$ OR $\overline{E}$ AT USER OPTION

PINOUT

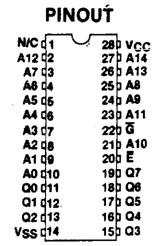


MCM63256

CHARACTERISTICS

- 32,768x8 HMOS MASK PROGRAMMABLE ROM
- INDUSTRY STANDARD 28 PIN PACKAGE
- FULLY STATIC OPERATION (NO CLOCKS OR STROBES)
- SUPPLY CURRENT
  100 mA ACTIVE (MAXIMUM)
  15 mA STANDBY (MAXIMUM)
- MAXIMUM ACCESS TIME — 150 ns
- MASK PROGRAMMABLE CHIP AND OUTPUT ENABLES
- ADDRESS (A14) IS USER SELECTABLE FOR EITHER PIN 27 OR PIN 1
- PROGRAM LAYER LATE IN PROCESS

PINOUT



MOTOROLA *Semiconductor Products Inc.*

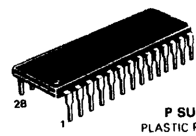
MOTOROLA
SEMICONDUCTORS
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MCM63128

Advance Information

HMOS
(N-CHANNEL, SILICON GATE)

16,384 × 8 BIT READ ONLY MEMORY



128K BIT READ ONLY MEMORY

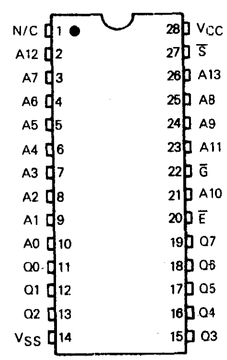
The MCM63128 is a MOS mask programmable, byte-oriented, Read-Only Memory (ROM). The MCM63128 is organized as 16×8 and is fabricated using Motorola's high performance N-channel silicon gate technology (HMOS). This device is designed to provide maximum circuit density and reliability with the highest possible performance. It remains fully compatible with TTL inputs and outputs while maintaining low power dissipation and wide operating margins. The MCM63128 also contains circuitry for current surge suppression which maintains the chip in an internal deselect mode until V_{CC} approaches 2.5 volts, at which time the chip is internally selected.

There are numerous logical nor or NAND combinations between Chip Enable ($\overline{E}$), Chip Select ($\overline{S}$), and Output Enable ($\overline{G}$) that tri state the device. This feature is selected by the user and placed into effect with the mask programming. The active level of the Chip Enable ($\overline{E}$), Chip Select ($\overline{S}$), and the Output Enable ($\overline{G}$), along with the memory contents, are defined by the user.

The Chip Enable input cotntrols the automatic power down feature which deselects the outputs and reduces the power consumption.

- Single + 5 Volt (±10%) Supply
- Fully Static Periphery — No Clocking Required on Chip Enable
- Power Dissipation
  100 mA Active (Maximum) (Unloaded)
  15 mA Standby (Maximum)
- Program Layer Late in Process for Quick Turnaround Time
- 150 ns — MCM63128P15
  200 ns — MCM63128P20
- Maximum Access from Address and Chip Enable
  60 ns — MCM63128P15
  80 ns — MCM63128P20
- Active Level for Chip Enable and Output Enable are User Selectable
- 28-Pin JEDEC Standard Package and Pinout

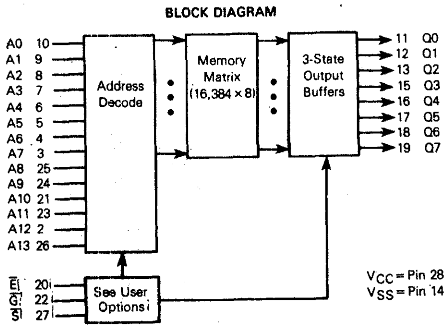
PIN ASSIGNMENT



PIN NAMES

A0-A13	Address
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{S}$	Chip Select
Q0-Q7	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

BLOCK DIAGRAM



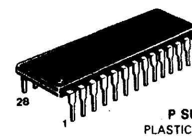
MOTOROLA
SEMICONDUCTORS
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MCM63256

Advance Information

HMOS
(N-CHANNEL, SILICON GATE)

32,768 × 8 BIT READ ONLY MEMORY



256K BIT READ ONLY MEMORY

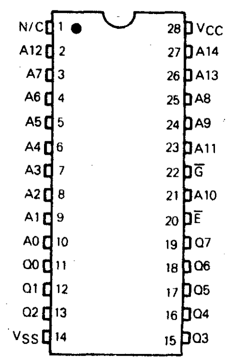
The MCM63256 is a MOS mask programmable byte-oriented, Read-Only Memory (ROM). The MCM63256 is organized as 32K×8 and is fabricated using Motorola's high performance N-channel silicon gate technology (HMOS). This device is designed to provide maximum circuit density and reliability with the highest possible performance. It remains fully compatible with TTL inputs and outputs while maintaining low power dissipation and wide operating margins. The MCM63256 also contains circuitry for current surge suppression which maintains the chip in an internal deselect mode until V_{CC} approachs 2.5 volts, at which time the chip is internally selected.

The active level of the Chip Enable and the Output Enable, along with the memory contents, are defined by the user. The user can also define the pinout assignment for address (A14) to either pin 27 or pin 1.

The Chip Enable input controls the automatic power down feature which deselects the outputs and reduces the power consumption.

- Single + 5 Volt (±10%) Supply
- Fully Static Periphery — No Clocking Required on Chip Enable
- Power Dissipation
  100 mA Active (Maximum) (Unloaded)
  15 mA Standby (Maximum)
- Program Layer Late in Process for Quick Turnaround Time
- Maximum Access from Address and Chip Enable
  150 ns—MCM63256P15
  200 ns—MCM63256P20
- Maximum Access from Output Enable
  60 ns—MCM63256P15
  80 ns—MCM63256P20
- Address (A14) is User Selectable for Either Pin 27 or Pin 1
- Active Level for Chip Enable and Output Enable are User Selectable
- 28-Pin JEDEC Standard Package and Pinout

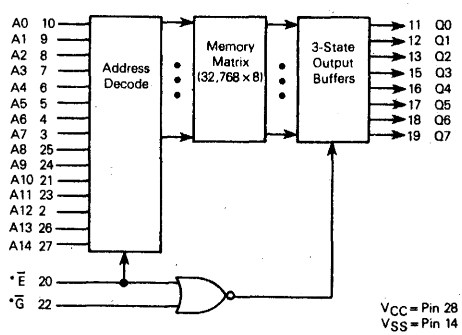
PIN ASSIGNMENT



PIN NAMES

A0-A14	Address
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
Q0-Q7	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

BLOCK DIAGRAM



*Active level defined by the user.

ADI-989

Introduction

GENERAL

This generic Schottky PROM family by National Semiconductor makes available to the industry one of the widest selections in sizes and organizations. Four-bit wide PROMs are provided with 256 to 4096 words in pin compatible 16 and 18 pin dual-in-line packages. The 8-bit wide devices range from 32 to 4096 words in a variety of packages. Being 'generic,' all PROMs share a common programming algorithm.

TITANIUM-TUNGSTEN FUSES

National's new Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti:W) fuse links designed to program efficiently with only 10.5 Volts applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metalization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5 Volts, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti:W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti:W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

National Semiconductor

Bipolar PROM Selection Guide

Size (Bits)	Organization		DIP (Pins)	Part Number	TAA (Max) in nS	TEA (Max) in nS	ICC (Max) in mA	Temperature Celsius
256	32 x 8	OC	16	DM54S188	45	30	110	−55 to +125
	32 x 8	OC	16	DM74S188	35	20	110	0 to +70
	32 x 8	TS	16	DM54S288	45	30	110	−55 to +125
	32 x 8	TS	16	DM74S288	35	20	110	0 to +70
1024	256 x 4	OC	16	DM54S387	60	30	130	−55 to +125
	256 x 4	OC	16	DM74S387	50	25	130	0 to +70
	256 x 4	TS	16	DM54S287	60	30	130	−55 to +125
	256 x 4	TS	16	DM74S287	50	25	130	0 to +70
2048	512 x 4	OC	16	DM54S570	65	35	130	−55 to +125
	512 x 4	OC	16	DM74S570	55	30	130	0 to +70
	512 x 4	TS	16	DM54S571	65	35	130	−55 to +125
	512 x 4	TS	16	DM74S571	55	30	130	0 to +70
	512 x 4	OC	16	DM54S570A	60	35	130	−55 to +125
	512 x 4	OC	16	DM74S570A	45	25	130	0 to +70
	512 x 4	TS	16	DM54S571A	60	35	130	−55 to +125
	512 x 4	TS	16	DM74S571A	45	25	130	0 to +70
	512 x 4	TS	16	DM54S571B	50	35	130	−55 to +125
	512 x 4	TS	16	DM74S571B	35	25	130	0 to +70
	256 x 8	TS	20	DM54LS471	70	35	100	−55 to +125
	256 x 8	TS	20	DM74LS471	60	30	100	0 to +70
4096	512 x 8	OC	20	DM54S473	75	35	155	−55 to +125
	512 x 8	OC	20	DM74S473	60	30	155	0 to +70
	512 x 8	TS	20	DM54S472	75	35	155	−55 to +125
	512 x 8	TS	20	DM74S472	60	30	155	0 to +70
	512 x 8	OC	20	DM54S473A	60	35	155	−55 to +125
	512 x 8	OC	20	DM74S473A	45	25	155	0 to +70
	512 x 8	TS	20	DM54S472A	60	35	155	−55 to +125
	512 x 8	TS	20	DM74S472A	45	25	155	0 to +70
	512 x 8	TS	20	DM54S472B	50	35	155	−55 to +125
	512 x 8	TS	20	DM74S472B	35	25	155	0 to +70
	512 x 8	OC	24	DM54S475	75	40	170	−55 to +125
	512 x 8	OC	24	DM74S475	65	35	170	0 to +70
	512 x 8	TS	24	DM54S474	75	40	170	−55 to +125
	512 x 8	TS	24	DM74S474	65	35	170	0 to +70
	512 x 8	OC	24	DM54S475A	60	35	170	−55 to +125
	512 x 8	OC	24	DM74S475A	45	25	170	0 to +70
	512 x 8	TS	24	DM54S474A	60	35	170	−55 to +125
	512 x 8	TS	24	DM74S474A	45	25	170	0 to +70
	512 x 8	TS	24	DM54S474B	50	35	170	−55 to +125
	512 x 8	TS	24	DM74S474B	35	25	170	0 to +70
	512 x 8	REG	24*	DM77SR474	40**	30	185	−55 to +125
	512 x 8	REG	24*	DM87SR474	35**	25	185	0 to +70
	512 x 8	REG	24*	DM77SR476	40**	30	185	−55 to +125
	512 x 8	REG	24*	DM77SR25	40**	30	185	−55 to +125
	512 x 8	REG	24*	DM87SR476	35**	25	185	0 to +70
	512 x 8	REG	24*	DM87SR25	35**	25	185	0 to +70
	1024 x 4	OC	18	DM54S572	75	45	140	−55 to +125
	1024 x 4	OC	18	DM74S572	60	35	140	0 to +70
	1024 x 4	TS	18	DM54S573	75	45	140	−55 to +125
	1024 x 4	TS	18	DM74S573	60	35	140	0 to +70
	1024 x 4	OC	18	DM54S572A	60	35	140	−55 to +125
	1024 x 4	OC	18	DM74S572A	45	25	140	0 to +70
	1024 x 4	TS	18	DM54S573A	60	35	140	−55 to +125
	1024 x 4	TS	18	DM74S573A	45	25	140	0 to +70
	1024 x 4	TS	18	DM54S573B	50	35	140	−55 to +125
	1024 x 4	TS	18	DM74S573B	35	25	140	0 to +70

* – 24 Pin Narrow Dual Inline Package

** – Set up Time

National Semiconductor

Bipolar PROM Selection Guide

National Semiconductor

Size (Bits)	Organization		DIP (Pins)	Part Number	TAA (Max) in nS	TEA (Max) in nS	ICC (Max) in mA	Temperature Celsius
8192	1024 x 8	OC	24	DM77S180	75	35	170	−55 to +125
	1024 x 8	TS	24*	DM77S280	75	35	170	−55 to +125
	1024 x 8	OC	24	DM87S180	55	30	170	0 to +70
	1024 x 8	TS	24*	DM87S280	55	30	170	0 to +70
	1024 x 8	OC	24	DM77S181	75	35	170	−55 to +125
	1024 x 8	TS	24*	DM77S281	75	35	170	−55 to +70
	1024 x 8	OC	24	DM87S181	55	30	170	0 to +70
	1024 x 8	TS	24*	DM87S281	55	30	170	0 to +70
	1024 x 8	TS	24	DM77LS181	175	70	100	−55 to +125
	1024 x 8	TS	24	DM87LS181	120	50	100	0 to +70
	1024 x 8	TS	24	DM77S181A	65	35	170	−55 to +125
	1024 x 8	TS	24	DM87S181A	45	30	170	0 to +70
	1024 x 8	REG.	24*	DM77SR181	50**	30	175	−55 to +125
	1024 x 8	REG.	24*	DM87SR181	40**	25	175	0 to +70
	2048 x 4	OC	18	DM77S184	75	35	140	−55 to +125
	2048 x 4	OC	18	DM87S184	55	30	140	0 to +70
	2048 x 4	TS	18	DM77S185	75	35	140	−55 to +125
	2048 x 4	TS	18	DM87S185	55	30	140	0 to +70
	2048 x 4	TS	18	DM77S185A	60	30	140	−55 to +125
	2048 x 4	TS	18	DM87S185A	45	25	140	0 to +70
	2048 x 4	TS	18	DM77S185B	50	30	140	−55 to +125
	2048 x 4	TS	18	DM87S185B	35	25	140	0 to +70
16384	2048 x 8	OC	24	DM77S190	80	40	175	−55 to +125
	2048 x 8	TS	24*	DM77S290	80	40	175	−55 to +125
	2048 x 8	OC	24	DM87S190	65	30	175	0 to +70
	2048 x 8	TS	24*	DM87S290	65	30	175	0 to +70
	2048 x 8	OC	24	DM77S191	80	40	175	−55 to +125
	2048 x 8	TS	24*	DM77S291	80	40	175	−55 to +125
	2048 x 8	OC	24	DM87S191	65	30	175	0 to +70
	2048 x 8	TS	24*	DM87S291	65	30	175	0 to +70
	2048 x 8	TS	24	DM77S191A	60	35	175	−55 to +125
	2048 x 8	TS	24	DM87S191A	45	30	175	0 to +70
	2048 x 8	TS	24	DM77S191B	50	30	175	−55 to +125
	2048 x 8	TS	24	DM87S191B	35	25	175	0 to +70
	4096 x 4	TS	20	DM77S195A	60	30	170	−55 to +125
	4096 x 4	TS	20	DM87S195A	45	25	170	0 to +70
	4096 x 4	TS	20	DM77S195B	50	30	170	−55 to +125
	4096 x 4	TS	20	DM87S195B	35	25	170	0 to +70
32768	4096 x 8	TS	24	DM77S321	65	35	185	−55 to +125
	4096 x 8	TS	24	DM87S321	55	30	185	0 to +70
	4096 x 8	TS	24*	DM77S421	65	35	185	−55 to +125
	4096 x 8	TS	24*	DM87S421	55	30	185	0 to +70

Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2)	-0.5 to +7.0V
Input Voltage (Note 2)	-1.2 to +5.5V
Output Voltage (Note 2)	-0.5 to +5.5V
Storage Temperature	-65 to +150C
Lead Temperature (10 seconds)	300C

* – 24 Pin Narrow Dual Inline Package
** – Set up Time

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

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MEMORY

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	DM77S321/421			DM87S321/421			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{IL}	Input Load Current	V_{CC} = Max., V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max., V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max., V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min., I_{OL} = 12mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25°C, 1MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max., All Outputs Open		135	185		135	185	mA
	TRI-STATE Parameters								
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max. (Note 4)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max., V_O = 0.45 to 2.4V Chip Disabled	−50		+50	−50		+50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0mA	2.4	3.2					V
		I_{OH} = −6.5mA				2.4	3.2		V

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Symbol	Parameter	JEDEC Symbol	DM77S321/421			DM87S321/421			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
T_{AA}	Address Access Time	TAVQV		40	65		40	55	ns
T_{EA}	Enable Access Time	TEVQV		20	35		20	30	ns
T_{ER}	Enable Recovery Time	TEXQX		20	35		20	30	ns
T_{ZX}	Output Enable Time	TEVQX		20	35		20	30	ns
T_{XZ}	Output Disable Time	TEXQZ		20	35		20	30	ns

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Symbol	Parameter	JEDEC Symbol	DM77S321A/421A			DM87S321A/421A			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
T_{AA}	Address Access Time	TAVQV		35			35		ns
T_{EA}	Enable Access Time	TEVQV		20			20		ns
T_{ER}	Enable Recovery Time	TEXQX		20			20		ns
T_{ZX}	Output Enable Time	TEVQX		20			20		ns
T_{XZ}	Output Disable Time	TEXQZ		20			20		ns

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.
Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Non-Registered PROM Programming Procedure

National Schottky PROMs are shipped from the factory with all fuses intact. As a result, the outputs will be low (logical "0") for all addresses. To generate high (logical "1") levels at the outputs, the device must be programmed. Information regarding commercially available programming equipment may be obtained from National. If it is desired to build your own programmer, the following conditions must be observed:

1. Programming should be attempted only at ambient temperatures between 15 and 30 degrees Celsius.

2. Address and enable inputs must be driven with TTL logic levels during programming and verification.

3. Programming will occur at the selected address when V_{CC} is at 10.5 volts, and at the selected bit location when the output pin, representing that bit, is at 10.5 volts, and the device is subsequently enabled. To achieve these conditions in the appropriate sequence, the following procedure must be followed:

   a) Select the desired word by applying high or low levels to the appropriate address inputs. Disable the device by applying a high level to one or more "active low" chip enable inputs.

   b) Increase V_{CC} from nominal to 10.5 volts (plus or minus 0.5V) with a slew rate between 1.0 and 10.0V/μs. Since V_{CC} is the source of the current required to program the fuse as well as the I_{CC} for the device at the programming voltage, it must be capable of supplying 750mA at 11.0 volts.

   c) Select the output where a logical high is desired by raising that output voltage to 10.5 volts (plus or minus 0.5V). Limit the slew rate from 1.0 to 10.0V/μs. This voltage change may occur simultaneously with the increase in V_{CC}, but must not precede it. It is critical that only one output at a time be programmed since the internal circuits can only supply programming current to one bit at a time. Outputs not being programmed must be left open or connected to a high impedance source of 20kΩ minimum (Remember that the outputs of the device are disabled at this time).

   d) Enable the device by taking the chip enable(s) to a low level. This is done with a pulse of 10μs. The 10μs duration refers to the time that the circuit (device) is enabled. Normal input levels are used and rise and fall times are not critical.

   e) Verify that the bit has been programmed by first removing the programming voltage from the output and then reducing V_{CC} to 4.0 volts (plus or minus 0.2V). Verification at a V_{CC} level of 4.0 volts will guarantee proper output states over the V_{CC} and temperature range of the programmed part. The device must be enabled to sense the state of the outputs. During verification, the loading of the output must be within specified I_{OL} and I_{OH} limits. Steps b, c, and d must be repeated up to 10 times or until verification that the bit has been programmed.

   f) Following verification, apply five additional programming pulses to the bit being programmed. The programming procedure is now complete for the selected bit.

   g) Repeat steps a through f for each bit to be programmed to a high level. If the procedure is performed on an automatic programmer, the duty cycle of V_{CC} at the programming voltage must be limited to a maximum of 25%. This is necessary to minimize device junction temperatures. After all selected bits are programmed, the entire contents of the memory should be verified.

Note: Since only an enabled device is programmed, it is possible to program these parts at the board level if all programming parameters are complied with.

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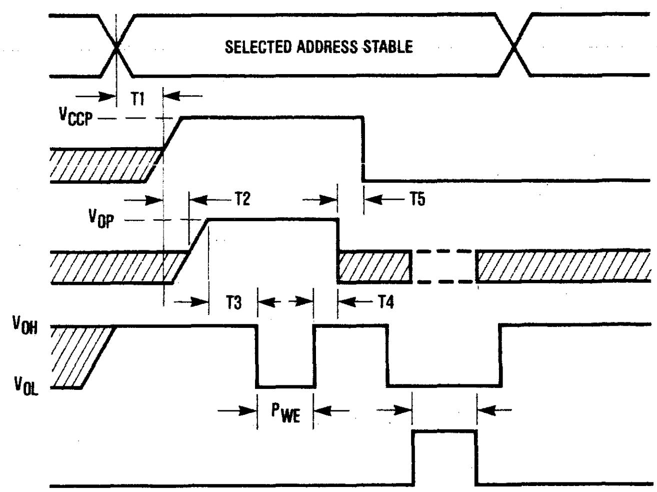
Programming Parameters Do not test or you may program the device

Sym	Parameters	Conditions	Min	Recommended Value	Max	Units
V_{CCP}	Required V_{CC} for Programming		10.0	10.5	11.0	V
I_{CCP}	I_{CC} During Programming	$V_{CC} = 11V$			750	mA
V_{OP}	Required Output Voltage for Programming		10.0	10.5	11.0	V
I_{OP}	Output Current while Programming	$V_{OUT} = 11V$			20	mA
I_{RR}	Rate of Voltage Change of V_{CC} or Output		1.0		10.0	V/μs
P_{WE}	Programming Pulse Width (Enabled)		9	10	11	μs
V_{CCV}	Required V_{CC} for Verification		3.8	4.0	4.2	V
M_{DC}	Maximum Duty Cycle for V_{CC} at V_{CCP}			25	25	%

Programming Waveforms Non-Registered PROM

T1 = 100ns min.
T2 = 5μs min. T2 may be > 0 if V_{CCP} rises at the same rate or faster than (V_{OP})
T3 = 100ns min.
T4 = 100ns min.
T5 = 100ns min.

P_{WE} is repeated for 5 additional pulses after verification of V_{OH} indicates a bit has been programmed.



National Semiconductor

Registered PROM Programming Procedure

National Schottky PROMs are shipped from the factory with all fuses intact. As a result, the outputs will be low (logical '0') for all addresses. To generate high (logical '1') levels at the outputs, the device must be programmed. Information regarding commercially available programming equipment may be obtained from National. If it is desired to build your own programmer, the following conditions must be observed.

1. Programming should be attempted only at ambient temperatures between 15°C and 30°C.
2. Address and Enable inputs must be driven with TTL logic levels during programming and verification.
3. Programming will occur at the selected address when V_{CC} is at 10.5V, and at the selected bit location when the output pin, representing that bit, is at 10.5V, and the device is subsequently enabled. To achieve these conditions in the appropriate sequence, the following procedure must be followed:
   a) Select the desired word by applying high or low levels to the appropriate address inputs. Disable the device by applying a high level to asynchronous chip Enable input $\overline{G}$. $\overline{GS}$ is held low during the entire programming time.
   b) Increase V_{CC} from nominal to 10.5V (±0.5V) with a slew rate between 1.0 and 10V/μs. Since V_{CC} is the source of the current required to program the fuse as well as the I_{CC} for the device at the programming voltage, it must be capable of supplying 750mA at 11V.
   c) Select the output where a logical high is desired by raising that output voltage to 10.5V (±0.5V). Limit the slew rate from 1.0 to 10V/μs. This voltage change may occur simultaneously with the increase in V_{CC}, but must not precede it. It is critical that only one output at a time be programmed since the internal circuits can only supply programming current to one bit at a time. Outputs not being programmed must be left open or connected to a high impedance source of 20kΩ minimum. (Remember that the outputs of the device are disabled at this time.)
   d) Enable the device by taking the chip enable ($\overline{G}$) to a low level. This is done with a pulse of 10μs. The 10μs duration refers to the time that the circuit (device) is enabled. Normal input levels are used and rise and fall times are not critical.
   e) Verify that the bit has been programmed by first removing the programming voltage from the output and then reducing V_{CC} to 4.0V (±0.2V). Verification at a V_{CC} level of 4.0V will guarantee proper output states over the V_{CC} and temperature range of the programmed part. Each data verification must be preceded by a positive going (low to high) clock edge to load the data from the array into the output register. The device must be enabled to sense the state of the outputs. During verification, the loading of the output must be within specified I_{OL} and I_{OH} limits. Steps b, c, and d must be repeated up to 10 times or until verification that the bit has been programmed.
   f) The initialize word is programmed by setting $\overline{INIT}$ input to a logic low and programming the initialize word output by output in the same manner as any other address. This can be accomplished by inverting the A9 address input from the PROM programmer and applying it to the $\overline{INIT}$ input. Using this method, the initialize word will program at address 512.
   g) Following verification, apply five additional programming pulses to the bit being programmed. The programming procedure is now complete for the selected bit.
   h) Repeat steps a through f for each bit to be programmed to a high level. If the procedure is performed on an automatic programmer, the duty cycle of V_{CC} at the programming voltage must be limited to a maximum of 25%. This is necessary to minimize device junction temperatures. After all selected bits are programmed, the entire contents of the memory should be verified.

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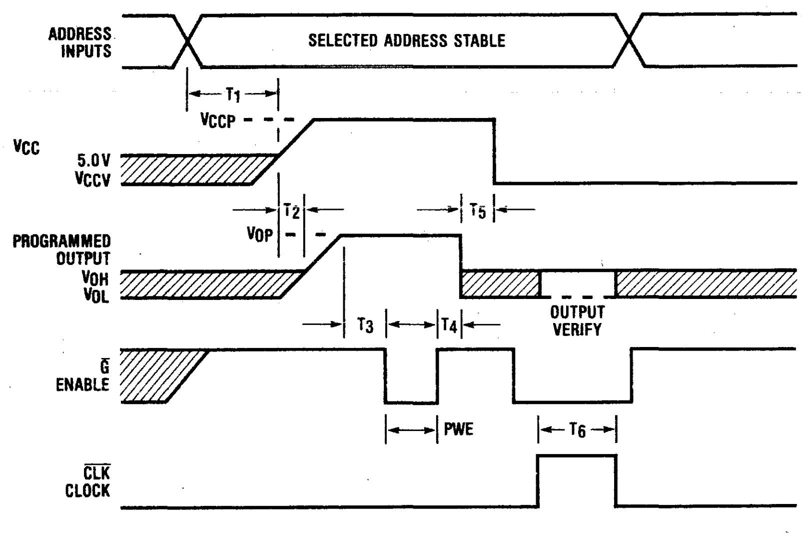
Programming Parameters Do not test or you may program the device

Sym	Parameters	Conditions	Min	Recommended Value	Max	Units
V_{CCP}	Required V_{CC} for Programming		10.0	10.5	11.0	V
I_{CCP}	I_{CC} During Programming	$V_{CC} = 11V$			750	mA
V_{OP}	Required Output Voltage for Programming		10.0	10.5	11.0	V
I_{OP}	Output Current while Programming	$V_{OUT} = 11V$			20	mA
I_{RR}	Rate of Voltage Change of V_{CC} or Output		1.0		10.0	V/μs
P_{WE}	Programming Pulse Width (Enabled)		9	10	11	μs
V_{CCV}	Required V_{CC} for Verification		3.8	4.0	4.2	V
M_{DC}	Maximum Duty Cycle for V_{CC} at V_{CCP}			25	25	%

Programming Waveforms Registered PROM



$T_1 = 100ns$ MIN.
$T_2 = 5\mu s$ MIN. (T_2 MAY BE > 0 IF V_{CCP} RISES AT THE SAME RATE OR FASTER THAN V_{OP}.)
$T_3 = 100ns$ MIN.
$T_4 = 100ns$ MIN.
$T_5 = 100ns$ MIN.
$T_6 = 50ns$ MIN.

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Standard Test Load

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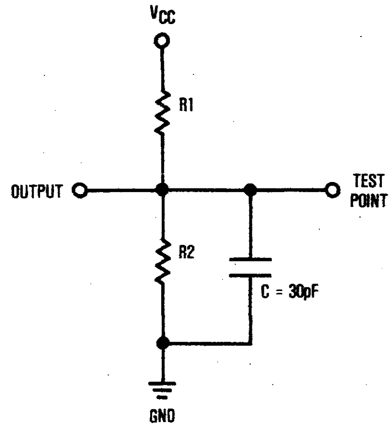
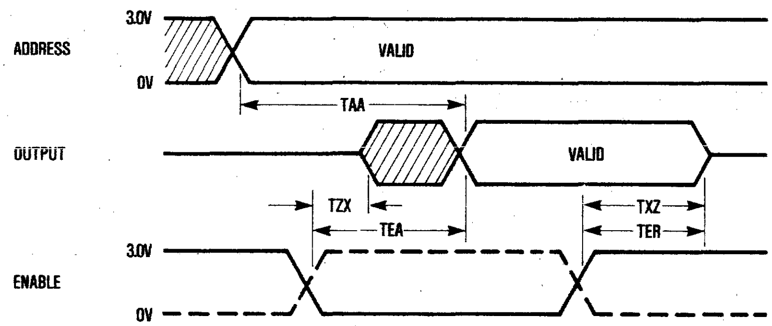
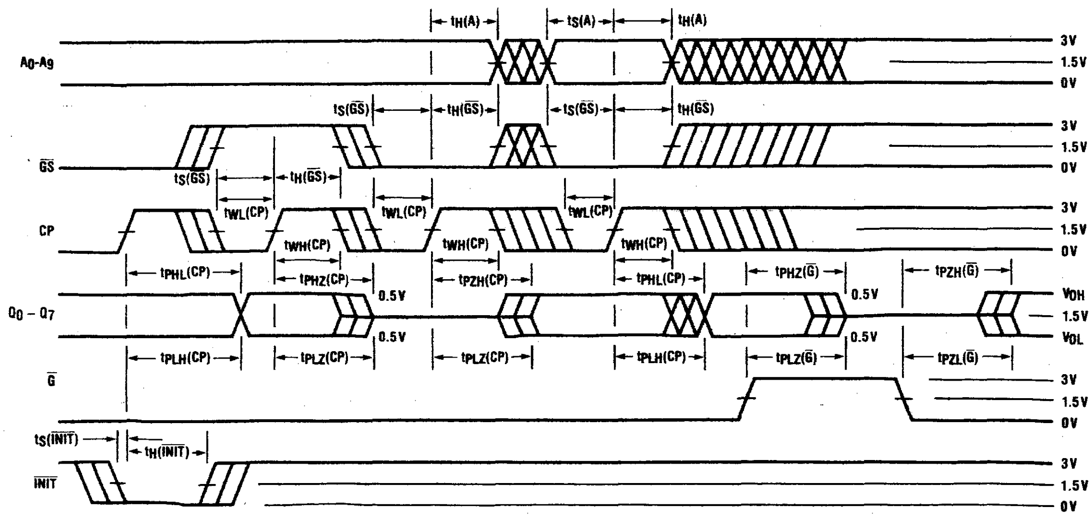


- Device input waveform characteristics are; Repetition rate = 1MHz
  Source impedance = 50Ω
  Rise and Fall times = 2.5ns max.
  (1.0 to 2.0 volt levels)
- TAA is measured with stable enable inputs.
- TEA and TER are measured from the 1.5 volt level on inputs and outputs with all address and enable inputs stable at applicable levels.
- For I_{OL} = 16mA, R1 = 300Ω and R2 = 600Ω for I_{OL} = 12mA, R1 = 400Ω and R2 = 800Ω.
- "C" includes scope and jig capacitance.

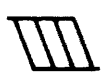
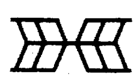
Switching Time Waveforms Non-Registered PROM



Switching Waveforms Registered PROM



Key To Timing Diagram

WAVEFORM	INPUTS	OUTPUTS	WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY		DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L		DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H			

Approved Programmers for NSC PROMs

MANUFACTURER	SYSTEM #
DATA I/O	5/17/19/29A
PRO-LOG	M910, M980
KONTRON	MPP80S
STAG	PPX
AIM	RP400
DIGELEC	UP803
STARPLEX™	

Quality Enhancement Programs For Bipolar Memory

A+ PROGRAM*			B+ PROGRAM		
Test	**Condition**	**Guaranteed LOT AQL 5**	**Test**	**Condition**	**Guaranteed LOT AQL 5**
D.C. Parametric And Functionality	25°C	0.05	D.C. Parametric And Functionality	25°C	0.05
	Each Temperature Extreme	0.05		Each Temperature Extreme	0.05
A.C. Parametric	25°C	0.4	A.C. Parametric	25°C	0.4
Mechanical	Critical	0.01	Mechanical	Critical	0.01
	Major	0.28		Major	0.28
Seal Tests Hermetic	Fine Leak (5×10^{-8})	0.4	Seal Tests Hermetic	Fine Leak (5×10^{-8})	0.4
	Gross	0.4		Gross	0.4

*Includes 160 hours of burn-in at 125°C.

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February 1983

NMC9306/COP494 256-Bit Serial Electrically Erasable Programmable Memory

General Description

The NMC9306/COP494 is a 256-bit non-volatile sequential access memory fabricated using advanced floating gate N-channel E^{2}PROM technology. It is a peripheral memory designed for data storage and/or timing and is accessed via the simple MICROWIRE™ serial interface. The device contains 256 bits of read/write memory divided into 16 registers of 16 bits each. Each register can be serially read or written by a COP400 series controller. Written information is stored in a floating gate cell with at least 10 years data retention and can be updated by an erase-write cycle. The NMC9306/COP494 has been designed to meet applications requiring up to 1×10^4 erase/write cycles per register. A power down mode reduces power consumption by 70 percent.

Features

- Low cost
- Single supply operation (5V ± 10%)
- TTL compatible
- 16 × 16 serial read/write memory
- MICROWIRE compatible serial I/O
- Compatible with COP400 processors
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology

Block and Connection Diagrams

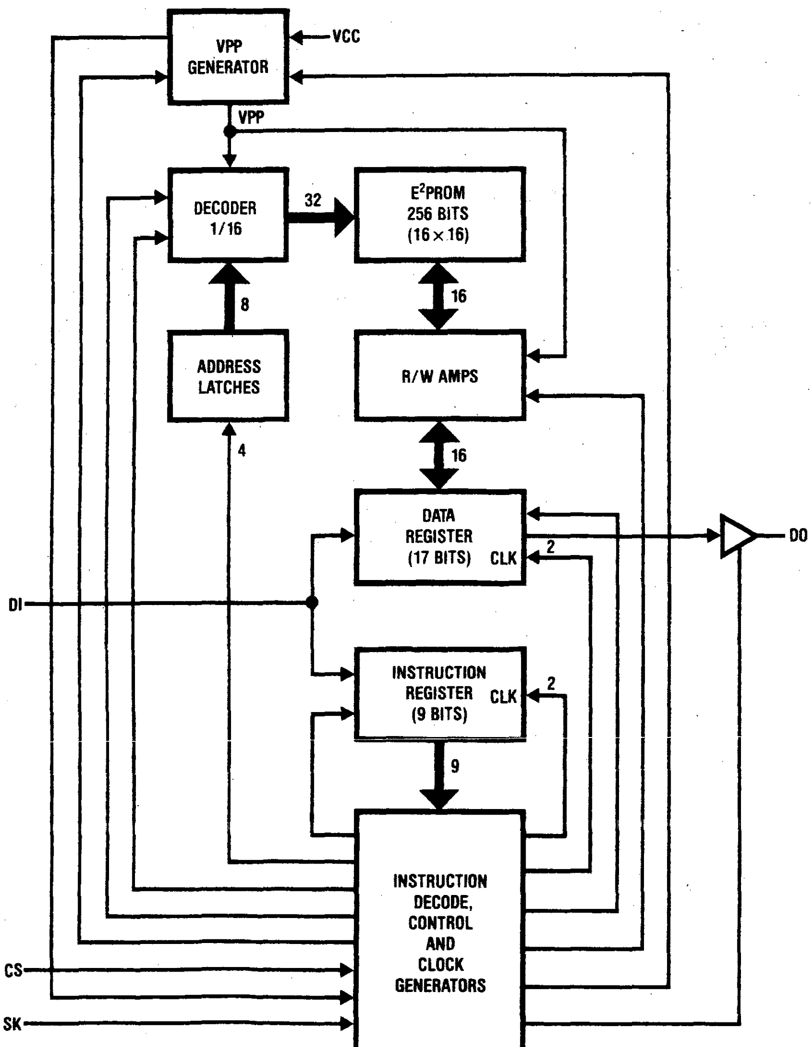

FIGURE 1

Dual-In-Line Package

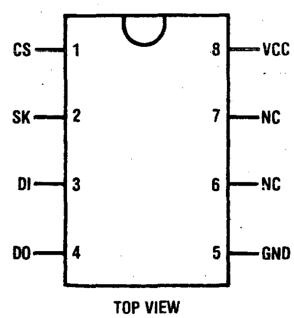

FIGURE 2

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
VCC	Power Supply
GND	Ground

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October 1983

NMC9346/COP495 1024-Bit Serial Electrically Erasable Programmable Memory (5V Only)

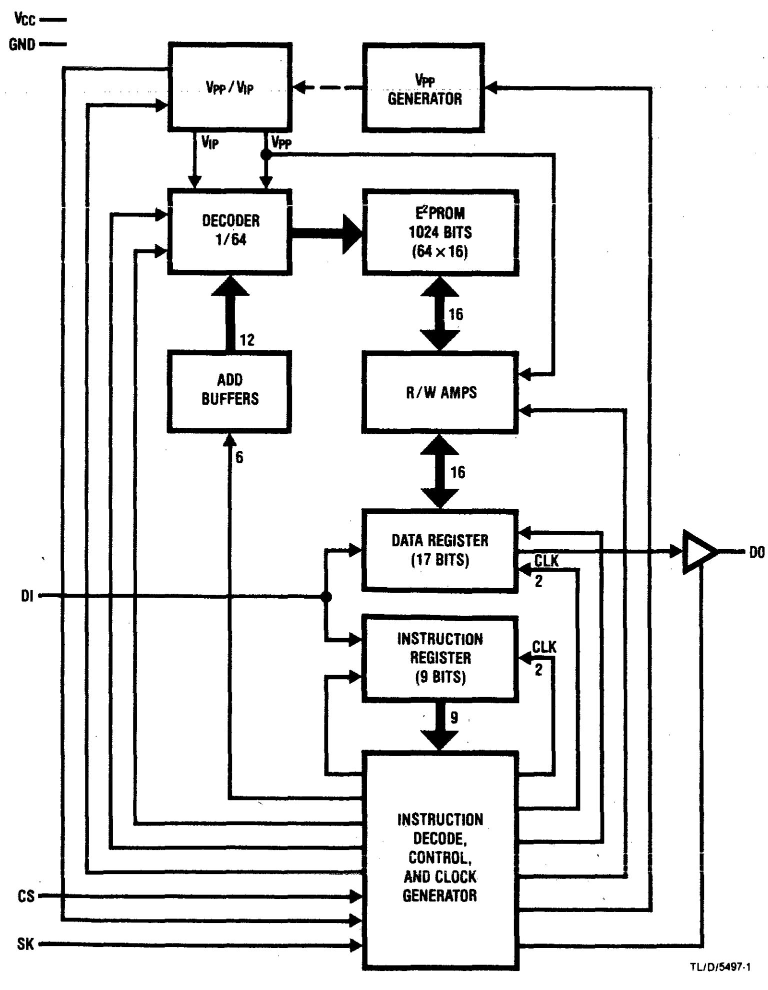
General Description

The NMC9346/COP495 is a 1024-bit non-volatile, sequential E^2PROM, fabricated using advanced N-channel E^2PROM technology. It is an external memory with the 1024 bits of read/write memory divided into 64 registers of 16 bits each. Each register can be serially read or written by a COP400 controller, or a standard microprocessor. Written information is stored in a floating gate cell until updated by an erase and write cycle. The NMC9346/COP495 has been designed for applications requiring up to 10^4 erase/write cycles per register. A power-down mode is provided by CS to reduce power consumption by 75 percent.

Features

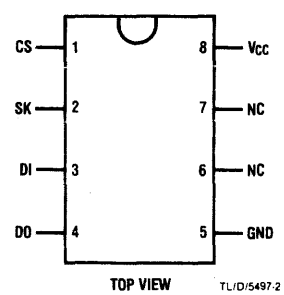
- Low cost
- Single supply read/write/erase operations (5V ± 10%)
- TTL compatible
- 64 × 16 serial read/write memory
- MICROWIRE™ compatible serial I/O
- Simple interfacing
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology
- Self-timed programming cycle
- Device status signal during programming

Block Diagram Serial E^2PROM



Connection Diagram

Dual-In-Line Package



Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground
NC	Not Connected

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National Semiconductor

February 1983

NMC9716 16k (2k × 8) Electrically Erasable PROM

Max Access/Current	NMC9716-25	NMC9716-35	NMC9716-45
Max Access Time (ns)	250	350	450
Max Active Current (mA)	110	110	110
Max Standby Current (mA)	50	50	50

General Description

The NMC9716 is a 16,384-bit electrically erasable and programmable read-only memory (E^2PROM) fabricated using National's high speed, low power, N-channel double silicon gate technology. The electrical erase/write capability of the NMC9716 makes it ideal for a wide variety of applications requiring in-system, non-volatile erase and write.

The NMC9716 is pin and functionally compatible with the NMC2816 E^2PROM, with the added system feature of erasing/writing with a 5V TTL pulse on chip enable ($\overline{CE}$), while the VPP is held at 21V. The erase/write cycle is very similar to the industry standard 2716 EPROM programming cycle.

The device operates from a 5V power supply in the read mode and, with its very fast read access speed, is compatible with high performance microprocessors.

The NMC9716 is deselected when $\overline{CE}$ input is high and is automatically placed in the standby mode. This mode provides a 52% reduction in power with no increase in access time. The NMC9716 also has an output enable control to eliminate bus contention in a system environment.

The NMC9716 can be easily erased and reprogrammed in a byte-by-byte mode and the entire memory array can be erased with a single programming pulse in the chip erase mode. Byte erase is identical to byte write, with all inputs at logic one (TTL high).

Features

- Erase/write with a 5V TTL pulse or a 21V pulse
- Pin and functionally compatible with the NMC2816
- No rise time restriction on erase/write pulse
- 2048 × 8 organization
- Conforms to JEDEC byte-wide family standard
- Microprocessor compatible architecture
- Single byte erase/write capability
- 10 ms byte erase/write time
- 10 ms chip erase mode
- Low power dissipation
  610 mW max (active power ICC + IPP)
  295 mW max (standby power ICC + IPP)

Block and Connection Diagrams

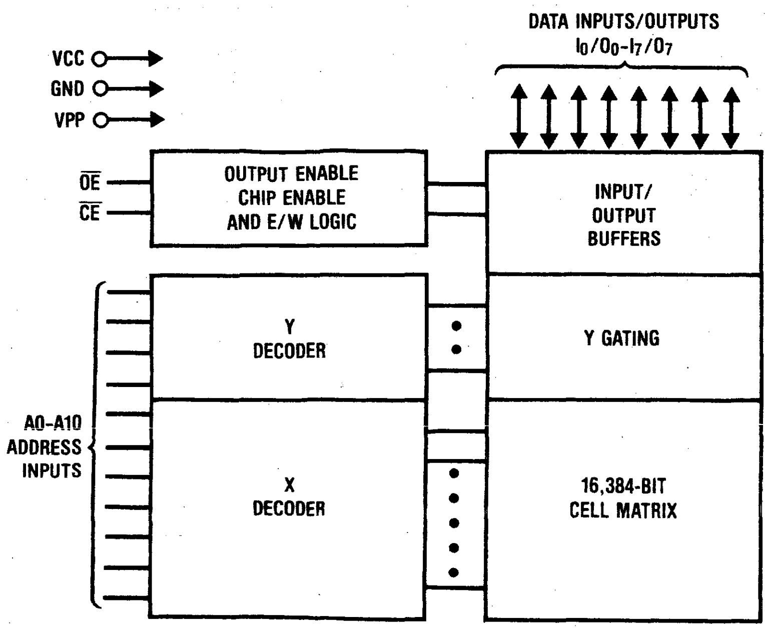
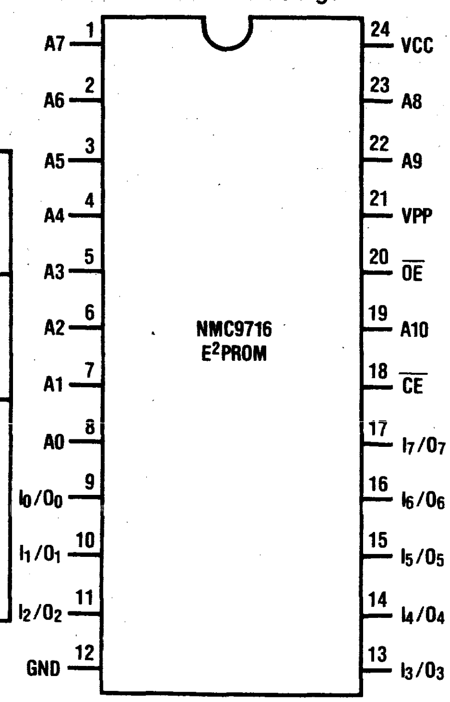


FIGURE 1

Dual-In-Line Package



TOP VIEW
FIGURE 2

Pin Names

A0–A10	Addresses	O_0–O_7	Data Outputs
$\overline{CE}$	Chip Enable	I_0–I_7	Data Inputs
$\overline{OE}$	Output Enable	VPP	Program Voltage

IM-B25M23/Printed in U.S.A.

National Semiconductor

PRELIMINARY
June 1983

NMC9817 16,384-Bit (2k × 8) E²PROM

General Description

The NMC9817 is a fast 5V-only E²PROM which offers many desired application features, making it ideally suited for efficiency and ease in system design. The added features on the NMC9817 include: 5V-only operation provided by an on-chip V_{PP} generation during erase-write; address and data latches to reduce part count and to free the microprocessor while the chip is busy during erase-write; 'ready' line indicator to indicate status of chip to the microprocessor and automatic erase before byte-write. It can meet applications requiring up to 10^4 write cycles per byte. The NMC9817 is a product of National's advanced E²PROM stepper technology and uses the powerful XMOS™ process for reliable, non-volatile data storage.

The NMC9817 sharply minimizes the interfacing hardware logic and firmware required to perform data writes. The device has complete self-timing which leaves the processor free to perform other tasks until the NMC9817 signals 'ready'. With an automatic erase before write, the user benefits by saving an erase command contributing to efficient usage of system processing time. On-chip address and data latching further enhances system performance.

The NMC9817's very fast read access times make it compatible with high performance microprocessor applications. It uses the proven two line control architecture which eliminates bus contention in a system environment. Combining these features with the NMC9817's 'ready' signal makes the device an extremely powerful, yet simple to use, E² memory.

The density, and level of integrated control, make the NMC9817 suitable for users requiring no hardware overhead, high system performance, minimal board space and design ease. Designing with and using the NMC9817 is extremely cost effective as the required high voltage and interfacing hardware required for other E²PROM devices has been eliminated by 5V-only operation and on-chip latches. See *Figures 1, 2, and 3* for the NMC9817 block diagram, pinout, and simple interface requirements.

Features

- Single 5V supply (eliminates an external 21V V_{PP})
- Self-timed byte-write with auto erase
- No external capacitor or pulse shaping circuits
- On-chip address and data latches
- Two line output control
- TRI-STATE® outputs
- RDY pin indicator
- Fast byte-writing
  - Write cycle (2 ms typical)
  - E/W cycle (4 ms typical)
- Very fast access times
  - NMC9817-20—200 ns
  - NMC9817-25—250 ns
  - NMC9817-35—350 ns
- Direct microprocessor interface capability
- No support components needed
- Reliable E²PROM XMOS stepper technology

Block and Connection Diagrams

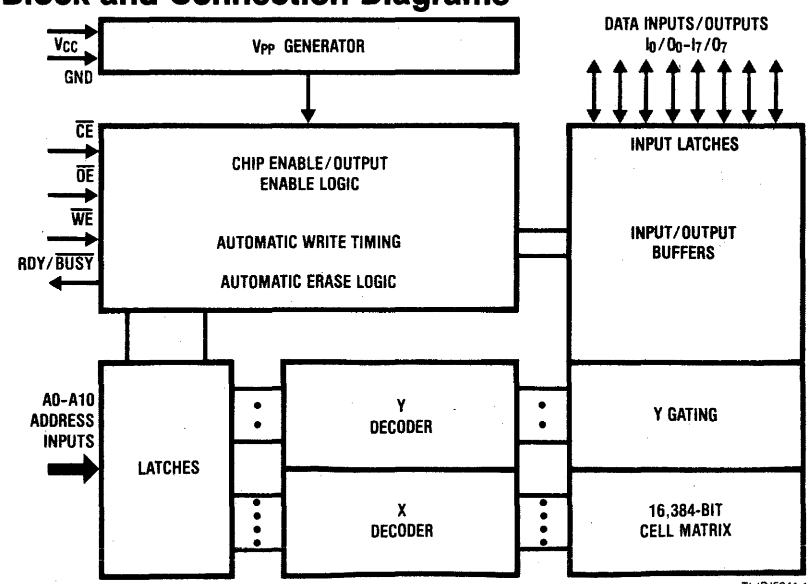
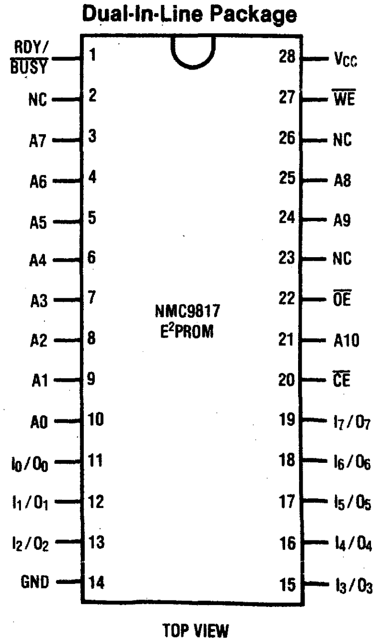


FIGURE 1

Dual-In-Line Package



TL/D/5041-2

FIGURE 2

Pin Names

A0–A10	Addresses	I_0–I_7	Data Inputs
$\overline{CE}$	Chip Enable	RDY/$\overline{BUSY}$	Device Ready/Busy
$\overline{OE}$	Output Enable	NC	No Connect
O_0–O_7	Data Outputs		

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National Semiconductor

PRELIMINARY
September 1983

HS2649 65,536 x 9 Bit Dynamic Random-Access Memory Module

General Description

The HS2649 is a high speed high density 589,824 bit, dynamic random-access memory organized into 65,536 words of 9 bits each (8 bit data plus parity). Single +5 volt power supply operation with internal decoupling capacitors allows for very compact layout of large memory systems.

The HS2649 is in a 30 pin single-in-line package (SIP) which uses a minimum of board space. This SIP package features ceramic construction, high strength, and good thermal conductivity.

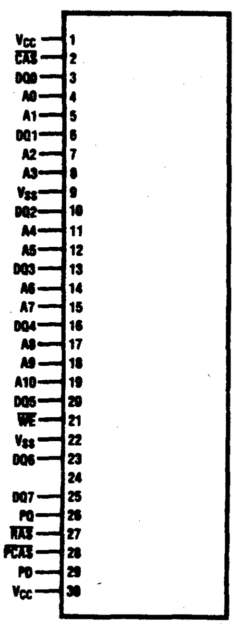
Applications

- Mainframe memory
- Buffer memory
- Peripheral storage
- Transportable computers

Features

- 65536×9 Bit Dynamic Ram
- SIP package
- 200 ns access time
- 335 ns cycle time
- Single +5 volt supply ±10%
- Common I/O except parity bit
- All inputs TTL compatible
- 256 refresh cycles/4 ms
- Power 2.8W active max, 180 mW standby max.

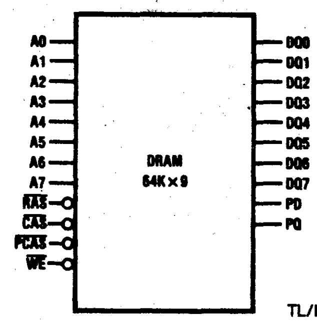
Connection Diagram*



TL/K/5478-2

*A8, 9 & 10 are designated for reference for future products, and are no connections on this part.

Logic Symbol



TL/K/5478-1

Pin Designations

A0 thru A7	Address Inputs
DQ0 thru DQ7	Data Inputs/Outputs
PD	Parity Input
PQ	Parity Output
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{PCAS}$	Parity Column Address Strobe
$\overline{WE}$	Write Enable
V_{CC}	+5 Volt Supply
V_{SS}	Ground

Don't miss the Sections on Semicustom ICs

Digital Gate Arrays, Standard Cells, and Linear Arrays Are All Covered

Vol. II, page 4425

NEC
NEC Electronics

μPD416-2/-3/-5
16384 x 1-BIT DYNAMIC MOS RANDOM ACCESS MEMORY

DESCRIPTION

The NEC μPD416 is a 16384 words by 1 bit Dynamic MOS RAM. It is designed for memory applications where very low cost and large bit storage are important design objectives.

The μPD416 is fabricated using a double-poly-layer N channel silicon gate process which affords high storage cell density and high performance. The use of dynamic circuitry throughout, including the sense amplifiers, assures minimal power dissipation.

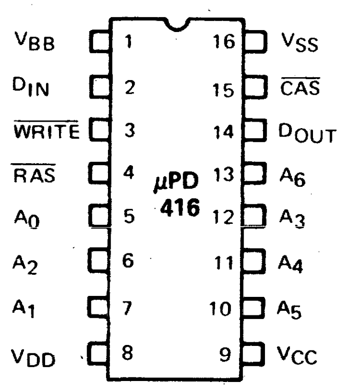
Multiplexed address inputs permit the μPD416 to be packaged in the standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is available in either ceramic or plastic. Noncritical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

FEATURES

- 16384 Words x 1 Bit Organization
- High Memory Density – 16 Pin Ceramic and Plastic Packages
- Multiplexed Address Inputs
- Standard Power Supplies +12V, −5V, +5V
- Low Power Dissipation; 462 mW Active (MAX), 20 mW Standby (MAX)
- Output Data Controlled by $\overline{CAS}$ and Unlatched at End of Cycle
- Read-Modify-Write, $\overline{RAS}$-only Refresh, and Page Mode Capability
- All Inputs TTL Compatible, and Low Capacitance
- 128 Refresh Cycles
- 5 Performance Ranges:

	ACCESS TIME	R/W CYCLE	RMW CYCLE
μPD416-2	200 ns	375 ns	375 ns
μPD416-3	150 ns	320 ns	320 ns
μPD416-5	120 ns	320 ns	320 ns

PIN CONFIGURATION



A_0-A_6	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write
V_{BB}	Power (-5V)
V_{CC}	Power (+5V)
V_{DD}	Power (+12V)
V_{SS}	Ground

Rev/4

DC CHARACTERISTICS

T_a = 0°C to +70°C①, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = 5V ± 10%, V_{SS} = 0V

PARAMETER		SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Supply Voltage		V_{DD}	10.8	12.0	13.2	V	②
Supply Voltage		V_{CC}	4.5	5.0	5.5	V	② ③
Supply Voltage		V_{SS}	0	0	0	V	②
Supply Voltage		V_{BB}	-4.5	-5.0	-5.5	V	②
Input High (Logic 1) Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$		V_{IHC}	2.7		7.0	V	②
Input High (Logic 1) Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$ $\overline{WRITE}$		V_{IH}	2.4		7.0	V	②
Input Low (Logic 0) Voltage, all inputs		V_{IL}	1.0		0.8	V	②
Operating V_{DD} Current		I_{DD1}			35	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} Min. ④
Standby V_{DD} Current		I_{DD2}			1.5	mA	$\overline{RAS}$ V_{IHC}, D_{OUT} High Impedance
Refresh V_{DD} Current	All Speeds except μPD416-5	I_{DD3}			25	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ V_{IHC}; t_{RC} 375 ns ④
	μPD416-5	I_{DD3}			27	mA	
Page Mode V_{DD} Current		I_{DD4}			27	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} 225 ns ④
Operating V_{CC} Current		I_{CC1}				μA	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} 375 ns ⑤
Standby V_{CC} Current		I_{CC2}	10		10	μA	$\overline{RAS}$ V_{IHC}; D_{OUT} High Impedance
Refresh V_{CC} Current		I_{CC3}	10		10	μA	$\overline{RAS}$ cycling, $\overline{CAS}$ V_{IHC}, t_{RC} 375 ns
Page Mode V_{CC} Current		I_{CC4}				μA	$\overline{RAS}$ V_{IL}, $\overline{CAS}$ cycling, t_{PC} 225 ns ⑤
Operating V_{BB} Current		I_{BB1}			200	μA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} 375 ns
Standby V_{BB} Current		I_{BB2}			100	μA	$\overline{RAS}$ V_{IHC}, D_{OUT} High Impedance
Refresh V_{BB} Current		I_{BB3}			200	μA	$\overline{RAS}$ cycling, $\overline{CAS}$ V_{IHC}, t_{RC} 375 ns
Page Mode V_{BB} Current		I_{BB4}			200	μA	$\overline{RAS}$ V_{IL}, $\overline{CAS}$ cycling; t_{PC} 225 ns
Input Leakage (any input)		$I_{I(L)}$	-10		10	μA	V_{BB} = 5V, 0V V_{IN} ≤ +7V, all other pins not under test = 0V
Output Leakage		$I_{O(L)}$	-10		10	μA	D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ +5.5V
Output High Voltage (Logic 1)		V_{OH}	2.4			V	I_{OUT} = 5 mA ③
Output Low Voltage (Logic 0)		V_{OL}			0.4	V	I_{OUT} = 4.2 mA

Notes: ① T_a is specified here for operation at frequencies to t_{RC} ≥ t_{RC} (min). Operation at higher cycle rates with reduced ambient temperatures and high power dissipation is permissible, however, provided AC operating parameters are met. See Figure 1 for derating curve.

② All voltages referenced to V_{SS}.

③ Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.

④ I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate. See Figures 2, 3 and 4 for I_{DD} limits at other cycle rates.

⑤ I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to data out. At all other times I_{CC} consists of leakage currents only.

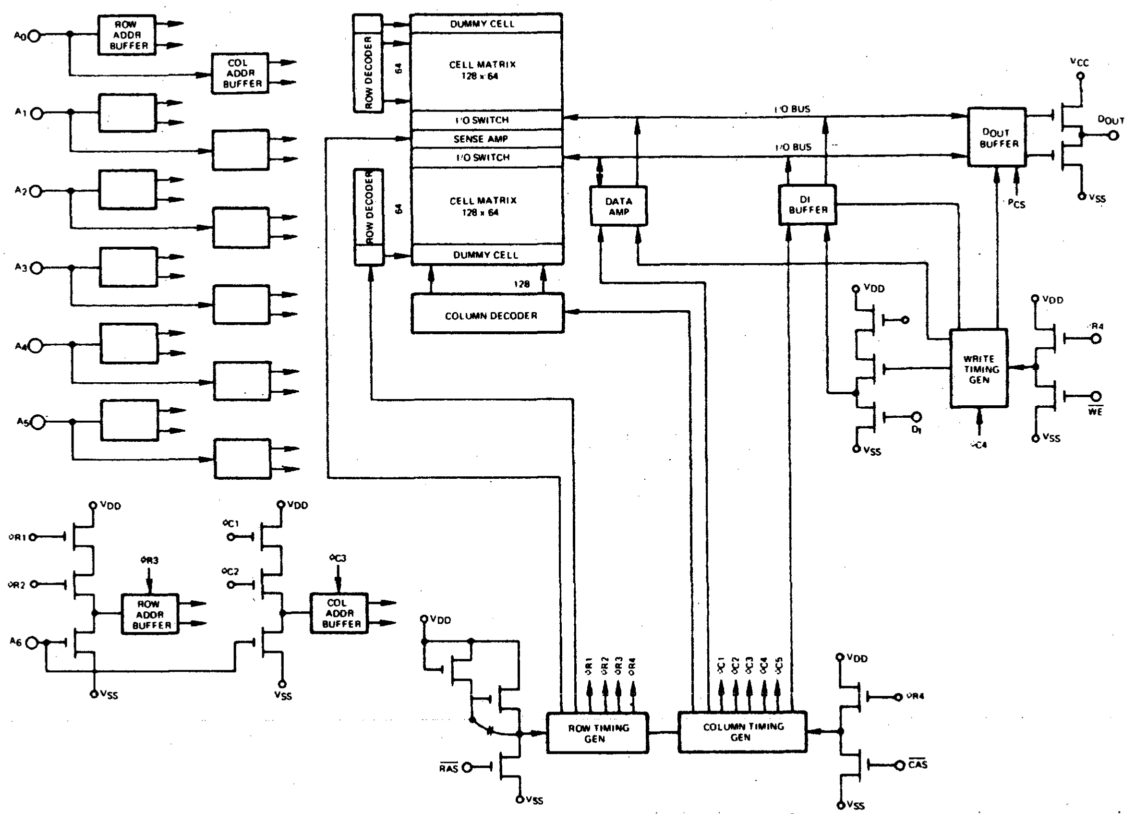
AC CHARACTERISTICS

T_a = 0°C to +70°C, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS μPD416-2 MIN		μPD416-3 MIN		μPD416-5 MIN		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
Random read or write cycle time	t_{RC}	375		320		320		ns	③
Read-write cycle time	t_{RWC}	375		375		320		ns	③
Page mode cycle time	t_{PC}	225		170		160		ns	
Access time from $\overline{RAS}$	t_{RAC}		200		150		120	ns	④ ⑥
Access time from $\overline{CAS}$	t_{CAC}		135		100		80	ns	⑤ ⑥
Output buffer turn-off delay	t_{OFF}	0	50	0	40	0	35	ns	⑦
Transition time (rise and fall)	t_T	3	50	3	35	3	35	ns	②
$\overline{RAS}$ precharge time	t_{RP}	120		100		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	200	32,000	150	32,000	120	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	135		100		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	135	10,000	100	10,000	80	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	65	20	50	15	40	ns	⑧
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	-20		-20		0		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	25		20		15		ns	
Column address set-up time	t_{ASC}	-10		-10		10		ns	
Column address hold time	t_{CAH}	55		45		40		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	120		95		80		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time	t_{RCH}	0		0		0		ns	
Write command hold time	t_{WCH}	55		45		40		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	120		95		80		ns	
Write command pulse width	t_{WP}	55		45		40		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	70		50		50		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	70		50		50		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	⑨
Data-in hold time	t_{DH}	55		45		40		ns	⑨
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	120		95		80		ns	
CAS precharge time (for page mode cycle only)	t_{CP}	80		60		60		ns	
Refresh period	t_{REF}		2		2		2	ms	
$\overline{WRITE}$ command set-up time	t_{WCS}	20		20		0		ns	⑩
$\overline{CAS}$ to $\overline{WRITE}$ delay	t_{CWD}	95		70		80		ns	⑩
$\overline{RAS}$ to $\overline{WRITE}$ delay	t_{RWD}	160		120		120		ns	⑩

Notes:
① AC measurements assume t_T = 5 ns.
② V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}
③ The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_a ≤ 70°C) is assured.
④ Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.
⑤ Assumes that $t_{RCD} \geq t_{RCD}$ (max).
⑥ Measured with a load equivalent to 2 TTL loads and 100 pF.
⑦ t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
⑧ Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}
⑨ These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
⑩ t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) ≥ t_{RWD} (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +150°C
All Output Voltages ①	−0.5 to +20 Volts
All Input Voltages ①	−0.5 to +20 Volts
Supply Voltages V_{DD}, V_{CC}, V_{SS} ①	−0.5 to +20 Volts
Supply Voltages V_{DD}, V_{CC} ②	−1.0 to +15 Volts
Short Circuit Output Current	50 mA
Power Dissipation	1 Watt

Notes: ① Relative to V_{BB}
② Relative to V_{SS}
$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAPACITANCE

$T_a = 0°C$ to $70°C$, $V_{DD} = +12V \pm 10\%$, $V_{BB} = -5V \pm 10\%$, $V_{CC} = +5V \pm 10\%$, $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance (A_0-A_6), D_{IN}	C_{I1}		4	5	pF	
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}		8	10	pF	
Output Capacitance (D_{OUT})	C_O		5	7	pF	

μPD4164-12/-15/-20 65,536 x 1-BIT DYNAMIC RANDOM ACCESS MEMORY

DESCRIPTION

The NEC μPD4164 is a 65,536 words by 1 bit Dynamic N-Channel MOS RAM designed to operate from a single +5V power supply. The negative-voltage substrate bias is internally generated — its operation is both automatic and transparent.

The μPD4164 utilizes a three-poly N-channel silicon gate process which provides high storage cell density, high performance and high reliability.

The μPD4164 uses a single transistor dynamic storage cell and advanced dynamic circuitry throughout, including the 512 sense amplifiers, which assures that power dissipation is minimized. Refresh characteristics have been chosen to maximize yield (low cost to user) while maintaining compatibility between Dynamic RAM generations.

The μPD4164 three-state output is controlled by $\overline{\text{CAS}}$, independent of $\overline{\text{RAS}}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{\text{CAS}}$ low. The data out pin is returned to the high impedance state by returning $\overline{\text{CAS}}$ to a high state. The μPD4164 hidden refresh feature allows $\overline{\text{CAS}}$ to be held low to maintain output data while $\overline{\text{RAS}}$ is used to execute $\overline{\text{RAS}}$ only refresh cycles.

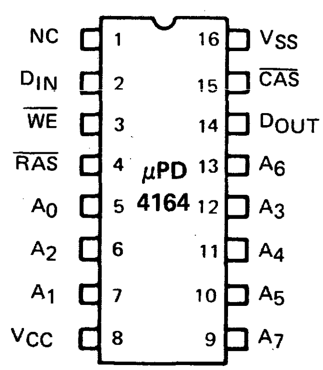
Refreshing is accomplished by performing $\overline{\text{RAS}}$ only refresh cycles, hidden refresh cycles, or normal read or write cycles on the 128 address combinations of A_0 through A_6 during a 2 ms period.

Multiplexed address inputs permit the μPD4164 to be packaged in the standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is compatible with widely available automated handling equipment.

FEATURES

- High Memory Density
- Multiplexed Address Inputs
- Single +5V Supply
- On Chip Substrate Bias Generator
- Access Time: μPD4164-20 — 200 ns
  μPD4164-15 — 150 ns
  μPD4164-12 — 120 ns
- Read, Write Cycle Time: μPD4164-20 — 335 ns
  μPD4164-15 — 270 ns
  μPD4164-12 — 260 ns
- Low Power Dissipation: 250 mW (Active); 28 mW (Standby)
- Non-Latched Output is Three-State, TTL Compatible
- Read, Write, Read-Write; Read-Modify-Write, RAS Only Refresh, and Page Mode Capability
- All Inputs TTL Compatible, and Low Input Capacitance
- 128 Refresh Cycles (A_0-A_6 Pins for Refresh Address)
- CAS Controlled Output Allows Hidden Refresh
- Available in Both Ceramic and Plastic 16 Pin Packages

PIN CONFIGURATION



PIN NAMES

A_0-A_7	Address Inputs
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
NC	No Connection

Rev/2

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . 0°C to +70°C
Storage Temperature (Ceramic Package) . . . . −55°C to +150°C
(Plastic Package) . . . . −55°C to +125°C
Supply Voltages On Any Pin Except V_{CC} . . . . −1 to +7 Volts ①
Supply Voltage V_{CC} . . . . −0.5 to +7 Volts ①
Short Circuit Output Current . . . . 50 mA
Power Dissipation . . . . 1 Watt

Note: ① Relative to V_{SS}

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = 0° to 70°C ① ; V_{CC} = +5V ± 10%; V_{SS} = 0V

PARAMETER	SYMBOL		LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Supply Voltage	V_{CC}		4.5	5.0	5.5	V	All Voltages Referenced to V_{SS}
	V_{SS}		0	0	0	V	
High Level Input Voltage, ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	V_{IHC}		2.4		5.5	V	
High Level Input Voltage, All Inputs Except $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	V_{IH}		2.4		5.5	V	
Low Level Input Voltage, All Inputs	V_{IL}		-2.0		0.8	V	
Operating Current Average Power Supply Operating Current $\overline{RAS}$, $\overline{CAS}$ Cycling; $t_{RC} = t_{RC}$ (Min.)	I_{CC1}	μPD4164-20			45	mA	②
		μPD4164-15			50		
		μPD4164-12			55		
Standby Current Power Supply Standby Current ($\overline{RAS} = V_{IHC}$, D_{OUT} = Hi-Impedance)	I_{CC2}				5.0	mA	
Refresh Current Average Power Supply Current, Refresh Mode; $\overline{RAS}$ Cycling, $\overline{CAS} = V_{IHC}$, $t_{RC} = t_{RC}$ (Min.)	I_{CC3}	μPD4164-20			35	mA	②
		μPD4164-15			40		
		μPD4164-12			45		
Page Mode Current Average Power Supply Current, Page Mode Operation $\overline{RAS} = V_{IL}$; $\overline{CAS}$ Cycling $t_{PC} = t_{PC}$ (Min.)	I_{CC4}	μPD4164-20			35	mA	②
		μPD4164-15			40		
		μPD4164-12			45		
Input Leakage Current Any Input V_{IN} = 0 to +5.5 Volts, All Other Pins Not Under Test = 0V	$I_{I(L)}$		−10		10	μA	
Output Leakage Current D_{OUT} is Disabled, V_{OUT} = 0 to +5.5 Volts	$I_{O(L)}$		−10		10	μA	
Output Levels High Level Output Voltage (I_{OUT} = 5 mA)	V_{OH}		2.4		V_{CC}	V	
Low Level Output Voltage (I_{OUT} = 4.2 mA)	V_{OL}		0		0.4	V	

Notes: ① T_a is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and high power dissipation is permissible, however, provided AC operating parameters are met.
② I_{CC1}, I_{CC3} and I_{CC4} depend on output loading and cycle rates. Specified rates are obtained with the output open.

AC CHARACTERISTICS

$T_a = 0°$ to $+70°C$ ①; $V_{CC} = +5V \pm 10\%$; $V_{SS} = 0V$ ③ ④

PARAMETER	SYMBOL	LIMITS μPD4164-20 MIN	LIMITS μPD4164-20 MAX	LIMITS μPD4164-15 MIN	LIMITS μPD4164-15 MAX	LIMITS μPD4164-12 MIN	LIMITS μPD4164-12 MAX	UNIT	TEST CONDITIONS
Random Read or Write Cycle Time	t_{RC}	330		260		230		ns	⑤
Read Write Cycle Time	t_{RWC}	345		280		255		ns	⑤
Page Mode Cycle Time	t_{PC}	190		145		130		ns	
Access Time from $\overline{RAS}$	t_{RAC}		200		150		120	ns	⑥ ⑧
Access Time from $\overline{CAS}$	t_{CAC}		100		75		60	ns	⑦ ⑧
Output Buffer Turn-Off Delay	t_{OFF}	0	50	0	40	0	35	ns	⑨
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	35	ns	④
$\overline{RAS}$ Precharge Time	t_{RP}	120		100		90		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	200	10,000	150	10,000	120	10,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	100		75		60		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	100	10,000	75	10,000	60	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	200		150		120		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	30	100	25	75	25	60	ns	⑩
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	0		0		0		ns	
$\overline{CAS}$ Precharge Time	t_{CPN}	30		25		25		ns	
$\overline{CAS}$ Precharge Time (For Page Mode Cycle Only)	t_{CP}	80		60		60		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	0		0		0		ns	
Row Address Set-Up Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	20		15		15		ns	
Column Address Set-Up Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	30		25		20		ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	130		100		80		ns	
Read Command Set-Up Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	25		20		20		ns	⑬
Read Command Hold Time	t_{RCH}	0		0		0		ns	⑬
Write Command Hold Time	t_{WCH}	55		45		35		ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	120		95		95		ns	
Write Command Pulse Width	t_{WP}	55		45		35		ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	55		45		40		ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	55		45		40		ns	
Data-In Set-Up Time	t_{DS}	0		0		0		ns	⑪
Data-In Hold Time	t_{DH}	55		45		35		ns	⑪
Data-In Hold Time Referenced to $\overline{RAS}$	t_{DHR}	155		120		95		ns	
Refresh Period	t_{REF}		2		2		2	ms	
WRITE Command Set-Up Time	t_{WCS}	10		−10		−10		ns	⑫
$\overline{CAS}$ to $\overline{WRITE}$ Delay	t_{CWD}	55		45		40		ns	⑫
$\overline{RAS}$ to WRITE Delay	t_{RWD}	130		120		100		ns	⑫

Notes:
① T_a is specified here for operation at frequencies to $t_{RC} > t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met.
② An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
③ AC measurements assume $t_T = 5$ ns.
④ V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
⑤ The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle times at which proper operation over the full temperature range ($0°C < T_a < 70°C$) is assured.
⑥ Assumes that $t_{RCS} \leq t_{RCD}$ (max). If t_{RCS} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.
⑦ Assumes that $t_{RCD} > t_{RCD}$ (max).
⑧ Measured with a load equivalent to 2 TTL loads and 100 pF.
⑨ t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
⑩ Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
⑪ These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
⑫ t_{WCS}, t_{CWD} and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} > t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} > t_{CWD}$ (min) and $t_{RWD} > t_{RWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell. If neither of the above conditions are met the condition of the data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
⑬ Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

μPD2147A HIGH-SPEED 4096 x 1-BIT STATIC RAM

Description

The μPD2147A is a 4096-bit static Random Access Memory organized as 4096 words by 1 bit, using a scaled MOS technology. It uses a uniquely innovative design approach which provides the ease-of-use features associated with non-clocked static memories and the reduced standby power dissipation associated with clocked static memories. To the user this means low standby power dissipation without the need for clocks, address setup and hold times, nor reduced data rates due to cycle times that are longer than access times.

$\overline{CS}$ controls the power-down feature. In less than a cycle time after $\overline{CS}$ goes high — deselecting the μPD2147A — the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ remains high. This device feature results in system power savings as great as 85% in larger systems, where the majority of devices are deselected.

The μPD2147A is placed in an 18-pin cerdip package configured with the industry standard 2147 pinout. It is directly TTL compatible in all respects: input, output, and a single +5V supply. The data is read out nondestructively and has the same polarity as the input data. A data input and a separate three-state output are used.

Features

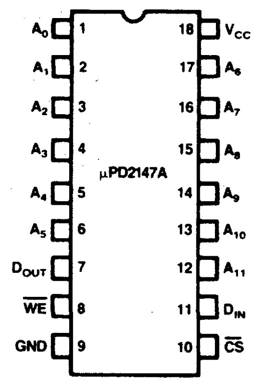
- Pinout, Function, and Power Compatible to Industry Standard 2147
- Scaled MOS Technology
- Completely Static Memory — No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Single +5V Supply
- Direct Performance Upgrade for 2147
- Automatic Power-Down
- High Density 18-Pin Package
- Directly TTL Compatible — All Input and Output
- Separate Data Input and Output
- Three-State Output

	Max Access Time	Supply Current	
		Active	Standby
μPD2147A-25	25 ns	160 mA	20 mA
μPD2147A-35	35 ns	160 mA	20 mA
μPD2147A-45	45 ns	160 mA	20 mA

Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	Output	Power
H	X	Not Selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	D_{OUT}	Active

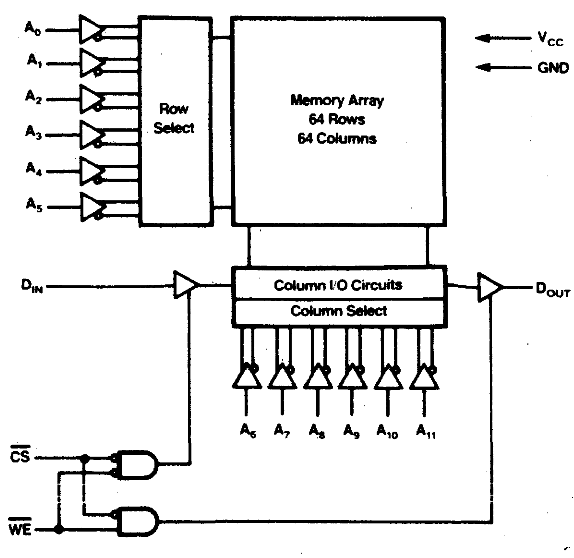
Pin Configuration



Pin Identification

Pin		Function
No.	Symbol	
1-6, 17-12	A_0-A_{11}	Address Inputs
7	D_{OUT}	Data Output
8	$\overline{WE}$	Write Enable
9	GND	Ground
10	$\overline{CS}$	Chip Select
11	D_{IN}	Data Input
18	V_{CC}	Power (+5V)

Block Diagram



Absolute Maximum Ratings*

$T_a = 25°C$	
Operating Temperature	−10°C to +85°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin	−3.5V to +7V ①
DC Output Current	20mA
Power Dissipation	1.2 W

Note: ① with respect to ground

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and Operating Characteristics

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$①

Parameter	Symbol	Limits Min	Typ②	Max	Unit	Test Conditions
Input Load Current (All Input Pins)	I_{LI}		0.01	10	μA	V_{CC} = Max, V_{IN} = GND to V_{CC}
Output Leakage Current	I_{LO}		0.01	10	μA	$\overline{CS} = V_{IH}$, V_{CC} = Max, V_{OUT} = GND to V_{CC}
Operating Current	I_{CC}		120	150	mA	$T_a = 25°C$ V_{CC} = Max, $\overline{CS} = V_{IL}$,
				160	mA	$T_a = 0°C$ Output Open
Standby Current	I_{SB}		12	20	mA	V_{CC} = Min to Max, $\overline{CS} = V_{IH}$
Peak Power-On Current	I_{PO} ③		25	50	mA	V_{CC} = GND to V_{CC} = Min, $\overline{CS}$ = Lower to V_{CC} or V_{IH} Min
Input Low Voltage	V_{IL}	−3.0		0.8	V	
Input High Voltage	V_{IH}	2.0		6.0	V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −4.0 mA
Output Short Circuit Current	I_{OS}			±130	mA	V_{OUT} = GND to V_{CC}

Notes: ① The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.
② Typical limits are V_{CC} = 5V, T_a = 25°C and specified loading.
③ A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected; otherwise, power-on current approaches I_{CC} active.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 1

Capacitance

$T_a = 25°C$; f = 1.0 MHz①

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{IN}			5	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}			6	pF	V_{OUT} = 0V

Note: ① This parameter is sampled and not 100% tested.

Figure 1 — Output Load

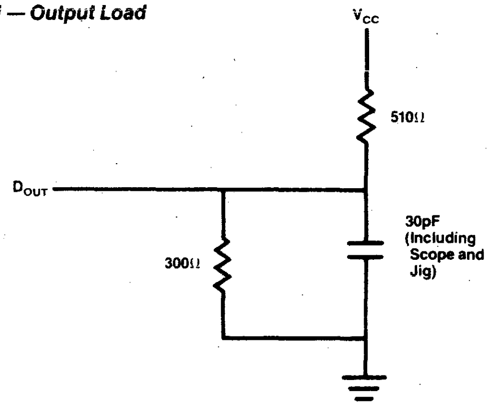
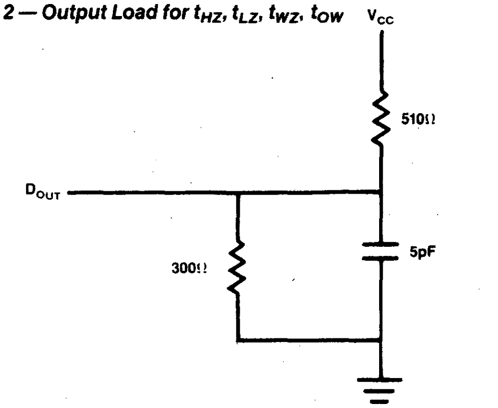


Figure 2 — Output Load for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}



NEC Electronics

MEMORY

AC Characteristics

Read Cycle

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%, unless otherwise noted.

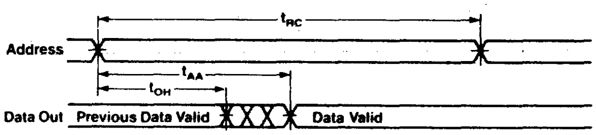
Parameter	Symbol	Limits μPD2147A-25 Min	Limits μPD2147A-25 Max	Limits μPD2147A-35 Min	Limits μPD2147A-35 Max	Limits μPD2147A-45 Min	Limits μPD2147A-45 Max	Unit	Test Conditions
Read Cycle Time	t_{RC} ①	25		35		45		ns	
Address Access Time	t_{AA}		25		35		45	ns	
Chip Select Access Time	t_{ACS}		25		35		45	ns	
Output Hold From Address Change	t_{OH}	5		5		5		ns	
Chip Select to Output in Low Z	t_{LZ} ②	5		5		5		ns	③
Chip Deselection to Output in High Z	t_{HZ} ②	0	20	0	30	0	30	ns	④
Chip Selection to Power-Up Time	t_{PU}	0		0		0		ns	
Chip Selection to Power-Down Time	t_{PD}		20		20		20	ns	

Write Cycle

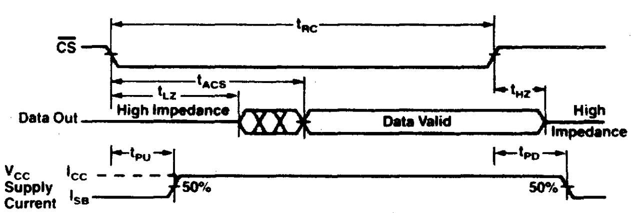
Parameter	Symbol	Limits μPD2147A-25 Min	Limits μPD2147A-25 Max	Limits μPD2147A-35 Min	Limits μPD2147A-35 Max	Limits μPD2147A-45 Min	Limits μPD2147A-45 Max	Unit	Test Conditions
Write Cycle Time②	t_{WC}	25		35		45		ns	
Chip Selection to End of Write	t_{CW}	25		35		45		ns	
Address Valid to End of Write	t_{AW}	25		35		45		ns	
Address Setup Time	t_{AS}	0		0		0		ns	
Write Pulse Width	t_{WP}	20		20		25		ns	
Write Recovery Time	t_{WR}	0		0		0		ns	
Data Valid to End of Write	t_{DW}	20		20		25		ns	
Data Hold Time	t_{DH}	10		10		10		ns	
Write Enabled to Output in High Z	t_{WZ}	0	15	0	20	0	25	ns	③
Output Active From End of Write	t_{OW}	0		0		0		ns	④

Timing Waveforms

Read Cycle No. 1 ⑤⑥

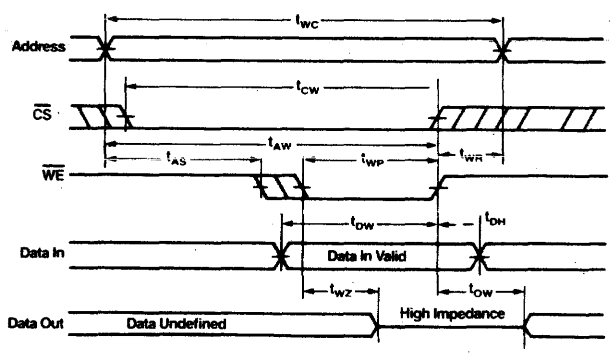


Read Cycle No. 2 ⑤⑦

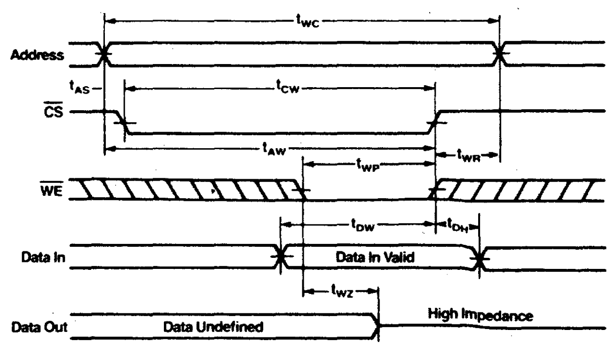


Notes:
1. All Read Cycle timings are referenced from the last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min, both for a given device and from device to device.
3. Transition is measured · 200mV from steady state voltage with specified loading in Figure 2.
4. Transition is measured at V_{OL} · 200mV and V_{OH} 200mV with specified loading in Figure 2.
5. $\overline{WE}$ is high for Read Cycles.
6. Device is continuously selected, $\overline{CS}$ V_{IL}.
7. Addresses valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle No. 1 ($\overline{WE}$ Controlled) ⑤



Write Cycle No. 2 ($\overline{CS}$ Controlled) ⑤



Notes:
1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured at V_{OL} · 200mV and V_{OH} 200mV with specified loading in Figure 2.
4. Transition is measured · 200mV from steady state voltage with specified loading in Figure 2.
5. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.

NEC Electronics

MEMORY

4096 (1024x4) BIT STATIC RAM

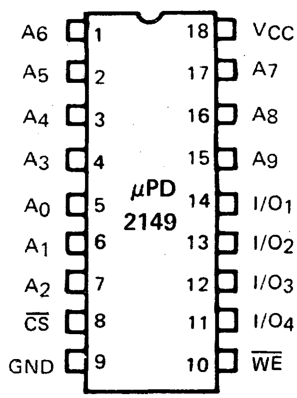
DESCRIPTION

The μPD2149 is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits. Using a scaled NMOS technology, it incorporates an innovative design approach which provides the ease-of-use features associated with non-clocked static memories.

The μPD2149 is encapsulated in an 18-pin ceramic package configured with the industry standard pinout. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. The data is read out non-destructively and has the same polarity as the input data.

FEATURES

- Completely Static Memory — No Clock or Timing Strobe Required
- Equal Access and Cycle Times, Faster Chip Select Access
- Single +5V Supply
- High Density 18-Pin Package
- Directly TTL Compatible — All Inputs and Outputs
- Common Input and Output
- Three-State Output
- Access Time: 35-55 ns MAX (From Address)
  15-25 ns MAX (From Chip Select)
- Power Dissipation: 180 mA MAX



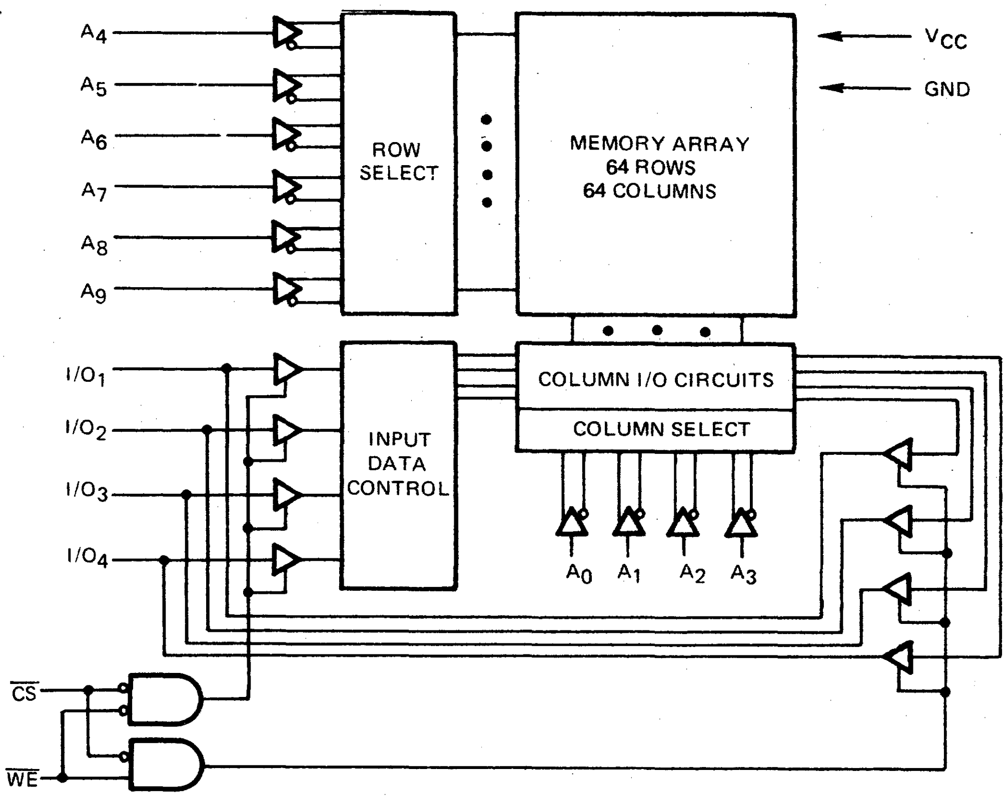
PIN NAMES

A_0-A_9	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O_1-I/O_4	Data Input/Output
V_{CC}	Power (+5V)
GND	Ground

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	I/O
H	X	Not Selected	High Z
L	L	Write	D_{IN}
L	H	Read	D_{OUT}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . -10°C to +85°C
Storage Temperature . . . . -65°C to +150°C
Voltage on Any Pin . . . . -1.5V to +7V ①
DC Output Current . . . . 20 mA
Power Dissipation 1.2W

Note: ① with respect to ground

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%, unless otherwise noted.

PARAMETER	SYMBOL	MIN	MAX	UNIT	TEST CONDITIONS
Input Leakage Current	I_{LI}		+10	μA	V_{IN} = GND to V_{CC}
Ouput Leakage Current	I_{LO}		+50	μA	CS = V_{IH} V_{OUT} = GND to 4.5V
Power Supply Current	I_{CC}		180	MA	V_{IN} = V_{CC}, I/O = open
Input Low Voltage	V_{IL}		0.8	V	
Input High Voltage	V_{IH}	2.1	V_{CC}	V	
Output Low Voltage	V_{OL}		0.4	V	I_{OL} = 8 MA
Output High Voltage	V_{OH}	2.4		V	I_{OH} = -4 MA
Output Short Circuit Current	I_{OS}		±200	MA	V_{OUT} = GND to V_{CC}

Note: The operating temperature range is guaranteed with transverse air flow exceeding 400 feet per minute.

CAPACITANCE

$T_a = 25°C$; f = 1.0 MHz ①

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			5	pF	$V_{IN} = 0V$
Output Capacitance	C_{OUT}			7	pF	$V_{OUT} = 0V$

Note: ① This parameter is sampled and not 100% tested.

AC TEST CONDITIONS

Input Pulse Levels . . . . Gnd to 3.0V
Input Rise and Fall Times . . . . 5 ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . See Figure 1

AC CHARACTERISTICS READ CYCLE ①

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$, unless otherwise noted.

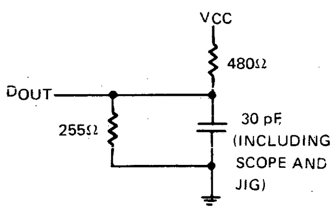


Figure 1

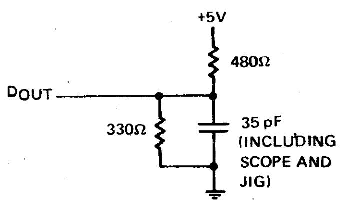


Figure 2

PARAMETER	SYMBOL	2149-2 MIN	2149-2 MAX	2149-1 MIN	2149-1 MAX	2149 MIN	2149 MAX	UNIT	TEST CONDITIONS
Read Cycle Time	T_{RC}	35		45		55		ns	
Access Time	T_A		35		45		55	ns	
Chip Selection to Output Valid	T_{CO}		15		20		25	ns	
Chip Selection to Output Active	T_{CX}	5		5		5		ns	
Output 3-State From Deselection	T_{OTD}		10		15		20	ns	②
Output Hold From Address Change	T_{OH}	5		5		5		ns	

Notes: ① $\overline{WE}$ is high for read cycle.
② Transition is measured ±500 MV from steady state with load of Figure 2. This parameter is sampled and not 100% tested.

AC CHARACTERISTICS WRITE CYCLE

PARAMETER	SYMBOL	μPD2149-2 MIN	μPD2149-2 MAX	μPD2149-1 MIN	μPD2149-1 MAX	μPD2149 MIN	μPD2149 MAX	UNIT	TEST CONDITIONS
Write Cycle Time	t_{WC}	35		45		55		ns	
Chip Selection to End of Write	t_{CW}	30		40		50		ns	
Address Valid to End of Write	t_{AW}	30		40		50		ns	
Address Setup Time	t_{AS}	0		0		0		ns	
Write Pulse Width	t_{WP}	30		35		40		ns	
Write Recovery Time	t_{WR}	5		5		5		ns	
Data Valid to End of Write	t_{DW}	20		20		20		ns	
Data Hold Time	t_{DH}	5		5		5		ns	
Write Enabled to Output in High Z	t_{WZ}	0	10	0	15	0	20	ns	①
Output Active from End of Write	t_{OW}	0		0		0		ns	②

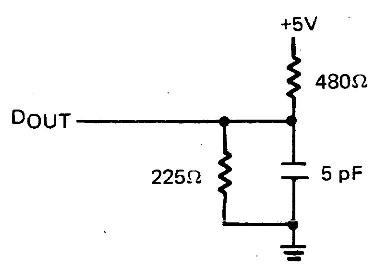


Figure 3

Notes: ① WE or CS must be high during all address transitions.
② Transition is measured ±500 MV from steady state with load of Figure 3. This parameter is sampled and not 100% tested.

μPD2167-2/-3
16,384 x 1-BIT STATIC RAM

Description

The μPD2167 is a 16,384-word by 1-bit static MOS RAM. Using a scaled-NMOS technology, its design provides the easy-to-use features associated with non-clocked static memories.

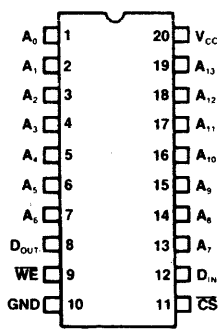
The μPD2167 has a three-state output and offers a standby mode that features an 83% savings in power consumption. The μPD2167 requires a single +5 volt supply and is fully TTL-compatible. It features equal access and cycle times and, because of its fully static operation, it requires no external clocks or timing strobes. It is packaged in a standard 20-pin, 300 mil DIP.

Features

- ☐ 16384 x 1 organization
- ☐ Fully static memory — no clock or timing strobe required
- ☐ Equal access and cycle times
- ☐ Single +5v supply
- ☐ Automatic power-down
- ☐ Standard 20-pin DIP, 300 mil
- ☐ All inputs and output directly TTL-compatible
- ☐ Separate data input and output
- ☐ Three-state output
- ☐ Power dissipation: 180 mA max (active)
  30 mA max (standby)

	Access time	R/W Cycle time
μPD2167-3	55ns	55ns
μPD2167-2	70ns	70ns

Pin Configuration

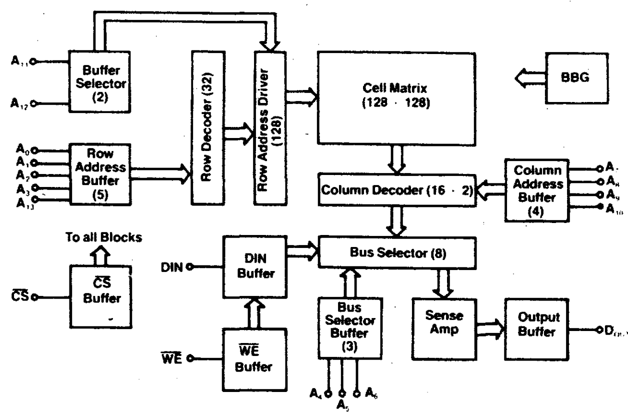


Pin Names

A_0-A_{13}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	Power (+5v)
V_{SS}	Ground

Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	Output	Power
H	X	not selected	High Z	Standby
L	L	write	High Z	Active
L	H	read	D_{OUT}	Active



Absolute Maximum Ratings*

T_a=25°C	
Temperature under bias	−10°C to +85°C
Storage temperature	−65°C to +150°C
Voltage on any pin with respect to ground	−3.5v to +7v
D.C. output current	20mA
Power dissipation	1.2w

*Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance
T_a=25°C, f=1.0 MHz

Parameter	Symbol	Max.	Unit	Conditions
Input Capacitance	C_{IN}	5	pF	V_{IN}=OV
Output Capacitance	C_{OUT}	6	pF	V_{OUT}=OV

This parameter is sampled and not 100% tested.

DC Characteristics

$T_a = 0°C$ to $+70°C$, $V_{CC} = +5v \pm 10\%$

Parameter	Sym	Min	Typ	Max	Unit	Test Conditions
Input load current all input pins	I_{LI}			10	μA	V_{CC} = max, V_{IN} = GND to V_{CC}
Output leakage current	I_{LO}		0.1	50	μA	$\overline{CS} = V_{IH}$, V_{CC} = max, V_{OUT} = GND to V_{CC}
Operating current	I_{CC}			170	mA	$T_A = 25°C$ (V_{CC} = max, $\overline{CS} = V_{IL}$, output open)
				180	mA	$T_A = 0°C$ (V_{CC} = max, $\overline{CS} = V_{IL}$, output open)
Standby current	I_{SB}			30	mA	V_{CC} = min to max, $\overline{CS} = V_{IH}$
Peak Power-On current	I_{PO}①		35	70	mA	V_{CC} = GND to V_{CC} min. $\overline{CS}$ = Lower of V_{CC} or V_{IH} min.
Input low voltage	V_{IL}	−3.0		0.8	V	
Input high voltage	V_{IH}	2.0		6.0	V	
Output low voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4			V	I_{OH} = −4 mA
Output short circuit current	I_{OS1}		−150		mA	V_{OUT} = GND
Output short circuit current	I_{OS2}		150		mA	$V_{OUT} = V_{CC}$

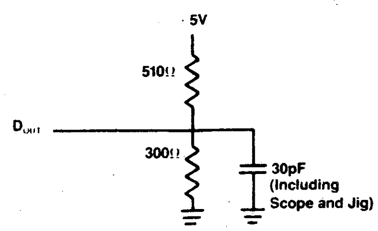


Figure 1 – Output Load

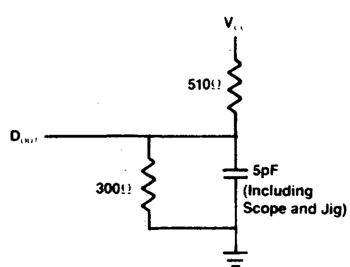


Figure 2 – Output Load for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}

AC Characteristics

$T_a = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$

Parameter	Symbol	μPD2167-3 min	μPD2167-3 typ	μPD2167-3 max	μPD2167-2 min	μPD2167-2 typ	μPD2167-2 max	Unit	Notes
Read Cycle									
Read cycle time	t_{RC}	55			70			ns	
Address access time	t_{AA}			55			70	ns	①
Chip select access time	t_{ACS}			55			70	ns	②
Output hold from address change	t_{OH}	5			5			ns	
Chip select to output in low Z	t_{LZ}	10			10			ns	
Chip deselect to output in high Z	t_{HZ}	0		40	0		40	ns	
Chip select to power up time	t_{PU}	0			0			ns	
Chip deselect to power down time	t_{PD}		30			30		ns	
Write Cycle									
Write cycle time	t_{WC}	55			70			ns	
Chip select to end of write	t_{CW}	45			55			ns	
Address valid to end of write	t_{AW}	45			55			ns	
Address setup time	t_{AS}	0			0			ns	
Write pulse	t_{WP}	35			40			ns	
Write recovery time	t_{WR}	10			15			ns	
Data valid to end of write	t_{DW}	25			30			ns	
Data hold time	t_{DH}	10			10			ns	
Write enabled to output in high Z	t_{WZ}	0		30	0		35	ns	
Output active from end of write	t_{OW}	0			0			ns	

Notes:
① $\overline{CS}$ valid prior to or coincident with address transition
② Address valid prior to or coincident with $\overline{CS}$ transition low

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μPD4016-1/-2/-3
2048 x 8-BIT STATIC RAM

Description

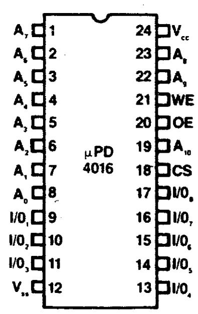
The μPD4016 is a 16384-bit static Random Access Memory device organized as 2048 words by 8 bits. Using a scaled NMOS technology, its design provides the ease-of-use features associated with nonclocked static memories. The μPD4016 has a three-state output and offers a standby mode with an attendant 75% to 90% savings in power consumption. It features equal access and cycle times and provides an output enable function that eliminates the need for external bus buffers. The μPD4016 is packaged in 600 mil and 300 mil 24-pin dual-in-line packages and is plug-compatible with 2716 EPROMS.

Features

- □ Scaled NMOS technology
- □ Completely static memory: no clock, no refresh
- □ Equal access and cycle times
- □ Single +5V supply
- □ Automatic power-down
- □ All inputs and outputs directly TTL-compatible
- □ Common I/O capability
- □ OE eliminates need for external bus buffers
- □ Three-state outputs
- □ Plug-compatible with 2716 EPROMS
- □ Standby current 15mA standard, selectable to 5mA
- □ Available in 600 mil and 300 mil DIP (Skinnydip)

	Access Time	R/W Cycle	I_{cc} (max)
μPD4016-1	250 ns	250 ns	60 mA
μPD4016-2	200 ns	200 ns	60 mA
μPD4016-3	150 ns	150 ns	60 mA

Pin Configuration



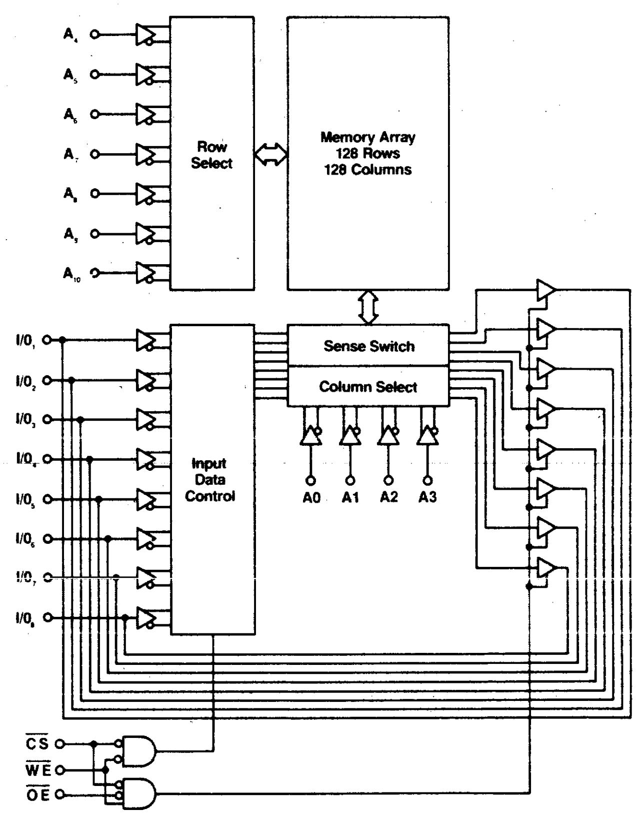
Pin Identification

Pin No.	Pin Symbol	Function
1-8, 19, 22, 23	A_7-A_0, A_{10}, A_9, A_8	Address Inputs
9-11, 13-17	I/O_1 - I/O_8	Data Input/Output
12	V_{SS}	Ground
18	CS	Chip Select
20	OE	Output Enable
21	WE	Write Enable
24	V_{CC}	Power (+5V)

Truth Table

CS	OE	WE	Mode	I/O	Power
H	X	X	Not Selected	High-Z	Standby
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
L	L	L	Write	D_{IN}	Active

Block Diagram



Absolute Maximum Ratings*

T_a = 25°C

Temperature Under Bias	−10°C to +85°C
Storage Temperature	−65°C to +150°C (4016D)
	−55°C to +125°C (4016C)
Voltage on Any Pin with Respect to Ground	−0.5V to +7V
DC Output Current	20mA
Power Dissipation	1W

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Rev/3

Capacitance
T_a = 25°C; f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{IN}			5	pF	V_{IN} = 0V
I/O Capacitance	$C_{I/O}$			7	pF	$V_{I/O}$ = 0V

This parameter is sampled and not 100% tested.

DC Characteristics
T_a = 0°C to 70°C, V_{CC} 5V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Leakage Current	I_{LI}			10	μA	VCC = Max. VIN = GND to VCC
Output Leakage Current	I_{LO}			10	μA	VCC = Max. CS = VIH VOUT = GND to VCC
Operating Current	I_{CC}			60	mA	VCC = Max. CS = VIL Outputs Open
Standby Current ①	I_{SB}			15	mA	VCC = Min. to Max. CS = VIH
Input Low Voltage	V_{IL}	−0.3		0.8	V	
Input High Voltage	V_{IH}	2.0		6.0	V	
Output Low Voltage	V_{OL}			0.4	V	IOL = 4mA
Output High Voltage	V_{OH}	2.4			V	IOH = 1mA
Output Short Circuit Current	I_{OS}	TBD		TBD	mA	VOUT = GND to VCC

Notes: ①5mA max available (contact regional office).

AC Test Conditions

Input Pulse Levels	0.8V to 2.2V
Input Rise and Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V

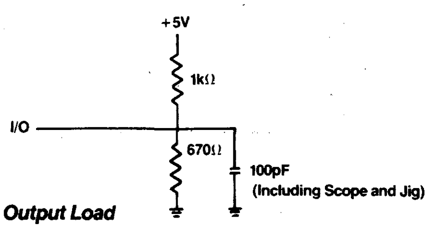


Figure 1 – Output Load

AC Characteristics
Read Cycle
T_a = 0°C to 70°C, V_{CC} = 5V ± 10%

Parameter	Symbol	μPD4016-3 Min	μPD4016-3 Max	μPD4016-2 Min	μPD4016-2 Max	μPD4016-1 Min	μPD4016-1 Max	Unit	Test Conditions
Read Cycle Time	t_{RC}	150		200		250		ns	①
Address Access Time	t_{AA}		150		200		250	ns	
Chip Select Access Time	t_{ACS}		150		200		250	ns	②
Output Hold from Address Change	t_{OH}	10		10		10		ns	
Chip Selection to Output in Low Z	t_{LZ}	10		10		10		ns	③④
Chip Deselection to Output in High Z	t_{HZ}		50		60		80	ns	③④
Output Enable to Output Valid	t_{OE}		70		90		110	ns	
Output Enable to Output in Low Z	t_{OLZ}	10		10		10		ns	③④
Output Disable to Output in High Z	t_{OHZ}		50		60		80	ns	③④
Chip Selection to Power up Time	t_{PU}	0		0		0		ns	④
Chip Deselection to Power down Time	t_{PD}		70		90		110	ns	④

Write Cycle
T_a = 0°C to 70°C, V_{CC} = 5V ± 10%

Parameter	Symbol	μPD4016-3 Min	μPD4016-3 Max	μPD4016-2 Min	μPD4016-2 Max	μPD4016-1 Min	μPD4016-1 Max	Unit	Test Conditions
Write Cycle Time	t_{WC}	150		200		250		ns	
Chip Selection to End of Write	t_{CW}	120		160		200		ns	
Address Valid to End of Write	t_{AW}	90		120		150		ns	
Address Setup Time	t_{AS}	0		0		0		ns	
Write Pulse Width	t_{WP}	80		100		130		ns	⑤
Write Recovery Time	t_{WR}	10		10		10		ns	
Data Valid to End of Write	t_{DW}	50		60		80		ns	
Data Hold Time	t_{DH}	0		0		0		ns	
Write Enabled to Output in High-Z	t_{WZ}		50		60		80	ns	⑥⑦
Output Active from End of Write	t_{OW}	10		10		10		ns	⑥⑦

Notes:
① All Read Cycle timings are referenced from the last valid address to the first transitioning address.
② Address valid prior to or coincident with $\overline{CS}$ transition low.
③ Transition is measured ± 200mV from steady state voltage with specified load of Figure 1.
④ This parameter is sampled and not 100% tested.
⑤ If CS and OE are both low before write enabled, $t_{WP} = t_{WZ} + t_{DW}$.
⑥ Transition is measured ± 200mV from steady state voltage with specified loading in Figure 2.
⑦ This parameter is sampled and not 100% tested.

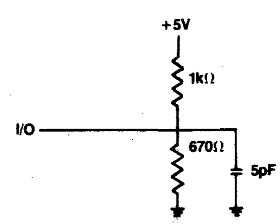


Figure 2 – Transition Load

NEC Electronics

MEMORY

μPD446/-1/-2/-3
2048 x 8-BIT STATIC CMOS RAM

DESCRIPTION

The μPD446 is a high speed, low power, 2048 word by 8 bit static CMOS RAM fabricated using an advanced silicon gate CMOS technology. A unique circuitry technique makes the μPD446 a very low operating power device which requires no clock or refreshing to operate. Minimum standby power current is drawn by this device when $\overline{CS}$ equals V_{CC} independently of the other input levels.

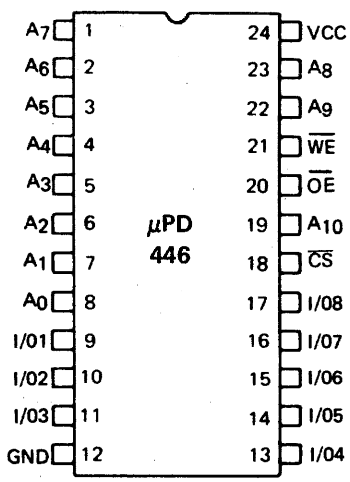
Data retention is guaranteed at a power supply voltage as low as 2V.

The μPD446 is packaged in a standard 24-pin dual-in-line package and is plug-in compatible with 16K EPROMs. The μPD446 is also available in the 24-pin mini-flat (SOP) package.

FEATURES

- Single +5V Supply
- Fully Static Operation – No Clock or Refreshing required
- TTL Compatible – All Inputs and Outputs
- Common I/O Using Three-State Output
- $\overline{OE}$ Eliminates Need for External Bus Buffers
- Max Access/Min Cycle Times Down to 150 ns
- Low power Dissipation, 18 mA Max Active/10 μA Max Standby/ 10 μA Max Data Retention
- Data Retention Voltage – 2V Min
- Standard 24-Pin Plastic, DIP, and Mini-flat (SOP) Packages
- Plug-in Compatible with 16K EPROMs
- Operating Temperature Range – –40°C to +85°C
- For operation at less than 4.5V power supply, contact the NEC Sales Office

PIN CONFIGURATION



PIN NAMES

A_0-A_{10}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select
I/O1-I/O8	Data Input/Output
V_{CC}	Power (+5V)
GND	Ground

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O	ICC
H	X	X	NOT SELECTED	HZ	STANDBY
L	H	H	NOT SELECTED	HZ	ACTIVE
L	L	H	READ	D_{OUT}	ACTIVE
L	X	L	WRITE	D_{IN}	ACTIVE

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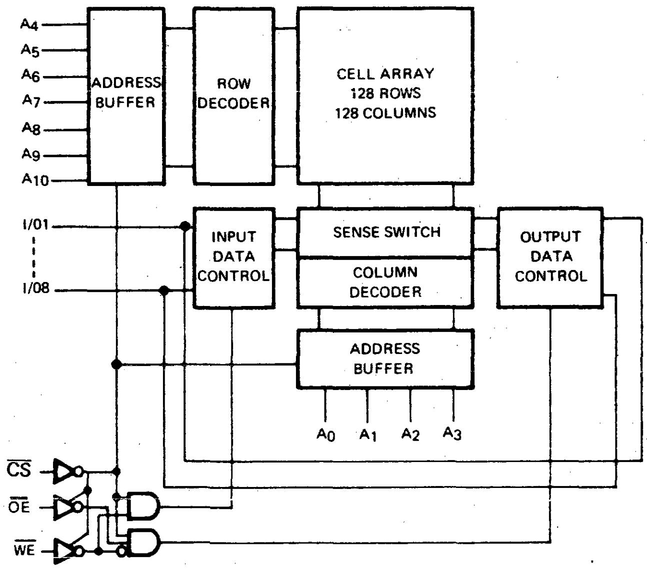
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Supply Voltage 7.0V
Input or Output Voltage Supplied . . . . -0.3 to $V_{CC} + 0.3$V
Storage Temperature Range . . . . $-55°C$ to $125°C$
Operating Temperature Range . . . . $-40°C$ to $+85°C$

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = -40°C$ to $+85°C$, $V_{CC} = 5.0V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	CONDITIONS
Input High Voltage	V_{IH}	2.2		V_{CC} +0.3	V	
Input Low Voltage	V_{IL}	−0.3		0.8	V	
Input Leakage Current	I_{LI}	−1.0		1.0	μA	$V_{IN} = 0 \sim V_{CC}$
I/O Leakage Current	I_{LO}	−1.0		1.0	μA	$V_{CS} = V_{IH}$ $V_{I/O} = 0 \sim V_{CC}$
Operating Supply Current	I_{CCA_1}		①	①	mA	$V_{CS} = V_{IL}$ $I_{I/O} = 0$ MIN TCYCLE
	I_{CCA_2}		5	10	mA	$V_{CS} = V_{IL}$ $I_{I/O} = 0$ DC CURRENT
	I_{CCA_3}		30	100	μA	$V_{CS} = 0.2V$ $I_{I/O} = 0$ $V_{IN} = V_{CC} -0.2$ OR 0.2V
Standby Current	I_{CCS}			10	μA	$V_{CS} = V_{CC} -0.2$ $V_{IN} = 0 \sim V_{CC}$
Output High Voltage	V_{OH}	2.4			V	$I_{OH} = -1.0$ mA
Output Low Voltage	V_{OL}			0.4	V	$I_{OL} = 2.0$ mA

NOTE: ① μPD446: 12 mA TYP, 18 mA MAX
μPD446-1: 18 mA TYP, 26 mA MAX
μPD446-2: 20 mA TYP, 30 mA MAX
μPD446-3: 25 mA TYP, 38 mA MAX

CAPACITANCE

T_a = 25°C, f = 1.0 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		6	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$		8	pF	$V_{I/O}$ = 0V

AC CHARACTERISTICS

READ CYCLE

V_{CC} = 5.0V ± 10%, T_a = −40°C to +85°C

PARAMETER	SYMBOL	μPD446-3 MIN	μPD446-3 MAX	μPD446-2 MIN	μPD446-2 MAX	μPD446-1 MIN	μPD446-1 MAX	μPD446 MIN	μPD446 MAX	UNIT
Read Cycle Time	t_{RC}	150		200		250		450		ns
Address Access Time	t_{AA}		150		200		250		450	ns
Chip Select Access Time	t_{ACS}		150		200		250		450	ns
Output Enable to Output Valid	t_{OE}		75		100		120		150	ns
Output Hold from Address Change	t_{OH}	15		15		15		15		ns
Chip Enable to Output in LZ	t_{CLZ}	10		10		10		10		ns
Output Enable to Output in LZ	t_{OLZ}	5		5		5		5		ns
Chip Disable to Output in HZ	t_{CHZ}		50		60		80		100	ns
Output Disable to Output in HZ	t_{OHZ}		50		60		80		100	ns

WRITE CYCLE

V_{CC} = 5.0V ± 10%, T_a = −40°C to +85°C

PARAMETER	SYMBOL	μPD446-3 MIN	μPD446-3 MAX	μPD446-2 MIN	μPD446-2 MAX	μPD446-1 MIN	μPD446-1 MAX	μPD446 MIN	μPD446 MAX	UNIT
Write Cycle Time	t_{WC}	150		200		250		450		ns
Chip Enable to End of Write	t_{CW}	120		150		180		210		ns
Address Valid to End of Write	t_{AW}	120		150		180		210		ns
Address Setup Time	t_{AS}	0		0		0		0		ns
Write Pulsewidth	t_{WP}	90		120		150		180		ns
Write Recovery Time	t_{WR}	0		0		0		0		ns
Data Valid to End of Write	t_{DW}	50		60		80		100		ns
Data Hold Time	t_{DH}	0		0		0		0		ns
Write Enable to Output in HZ	t_{WHZ}		50		60		80		100	ns
Output Active from End of Write	t_{OW}	10		10		10		10		ns

LOW V_{CC} DATA RETENTION

T_a = −40°C to +85°C

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
VCC for Data Retention	V_{CCDR}	$V_{IN} = 0 \sim V_{CC}$, $V_{\overline{CS}} = V_{CC}$	2.0			V
Data Retention Current	I_{CCDR}	V_{CC} = 3.0V, $V_{IN} = 0 \sim V_{CC}$ $V_{\overline{CS}} = V_{CC}$		0.01	10	μA
Chip Deselection to Data Retention Time	t_{CDR}		0			ns
Operation Recovery Time	t_R		t_{RC}			ns

2048 × 8-BIT STATIC CMOS RAM

DESCRIPTION

The μPD449 is a high speed, low power, 2048 word by 8-bit static CMOS RAM fabricated using an advanced silicon gate CMOS technology. A unique circuitry technique makes the μPD449 a very low operating power device which requires no clock or refreshing to operate.

Since the device has two chip enable inputs, it is suited for battery backup applications. Minimum standby power current is drawn by this device when $\overline{CE}1$ or $\overline{CE}2$ equals V_{CC} independently of the other input levels.

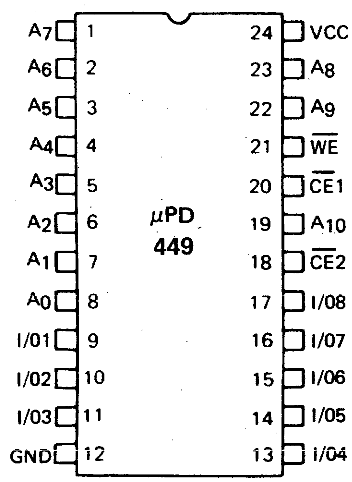
Data Retention is guaranteed at a power supply voltage as low as 2V.

The μPD449 is packaged in a standard 24-pin dual-in-line package and is plug-in compatible with 16K EPROMs. The μPD449 is also available in the 24-pin mini-flat (SOP) package.

FEATURES

- Single +5V Supply
- Fully Static Operation — No Clock or Refreshing required
- TTL Compatible — All Inputs and Outputs
- Common Data Input and Output Using Three-State Output
- Two Chip Enable Inputs eliminates need for External Bus Buffers
- Max Access/Min Cycle Times Down to 150 ns
- Low Power Dissipation; 18 mA Max Active/10 μA Max Standby/ 10 μA Max Data Retention
- Data Retention Voltage — 2V Min
- Standard 24-Pin Plastic, DIP and Mini-flat (SOP) Packages
- Plug-in Compatible with 16K EPROMs
- Operating Temperature Range −40°C to +85°C
- For operation at less than 4.5V power supply, contact the NEC Sales Office

PIN CONFIGURATION



PIN NAMES

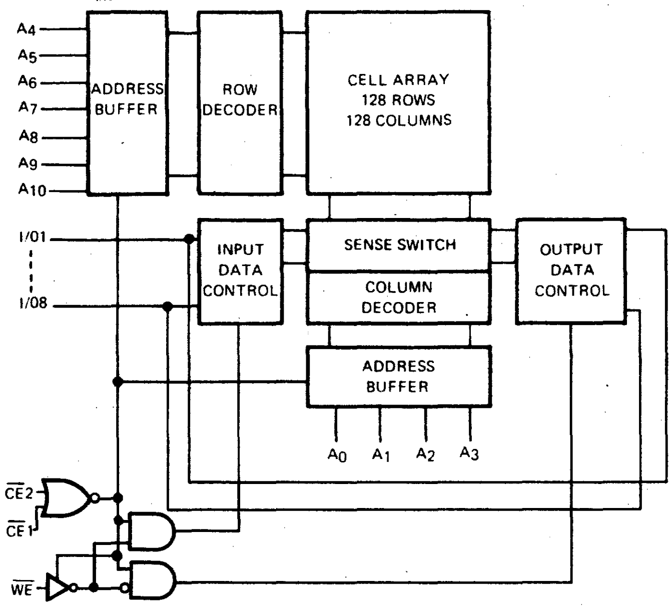
A_0-A_{10}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CE}1$-$\overline{CE}2$	Chip Enable Inputs
I/O1-I/O8	Data Input/Output
V_{CC}	Power (+5V)
GND	Ground

TRUTH TABLE

$\overline{CE}1$	$\overline{CE}2$	$\overline{WE}$	MODE	I/O	ICC
X	H	X	NOT SELECTED	HZ	STANDBY
H	X	X	NOT SELECTED	HZ	STANDBY
L	L	L	WRITE	D_{IN}	ACTIVE
L	L	H	READ	D_{OUT}	ACTIVE

Rev/1

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Supply Voltage 7.0V
Input or Output Voltage Supplied . . . . -0.3 to $V_{CC} + 0.3V$
Storage Temperature Range . . . . $-55°C$ to $125°C$
Operating Temperature Range . . . . $-40°C$ to $+85°C$

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$V_{CC} = 5V \pm 10\%$, T_a $-40°C$ to $+85°C$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	2.2		V_{CC} +0.3	V	
Input Low Voltage	V_{IL}	-0.3		0.8	V	
Input Leakage Current	I_{LI}	-1.0		1.0	μA	$V_{IN} = 0 \sim V_{CC}$
I/O Leakage Current	I_{LO}	1.0		1.0	μA	$V_{\overline{CE}1}$ or $V_{\overline{CE}2} = V_{IH}$ or $V_{WE} = V_{IL}$ $V_{I/O} = 0 \sim V_{CC}$
Operating Supply Current	I_{CCA1}		①	①	mA	$V_{\overline{CE}1}$ and $V_{\overline{CE}2} = V_{IL}$ $I_{I/O} = 0$ MIN TCYCLE
	I_{CCA2}		5	10	mA	$V_{\overline{CE}1}$ and $V_{\overline{CE}2} = V_{IL}$ $I_{I/O} = 0$ DC CURRENT
	I_{CCA3}		30	10	μA	$V_{\overline{CE}1}$ and $V_{\overline{CE}2} = 0.2V$ $V_{IN} = V_{CC}$ 0.2V or 0.2V $I_{I/O} = 0$
Standby Current	I_{CCS}			10	μA	$V_{\overline{CE}1}$ or $V_{\overline{CE}2} = V_{CC}$ -0.2V $V_{IN} = 0 \sim V_{CC}$
Output High Voltage	V_{OH}	2.4			V	$I_{OH} = -1.0$ mA
Output Low Voltage	V_{OL}			0.4	V	$I_{OL} = 2.0$ mA

NOTE: ① μPD449: 12 mA TYP, 18 mA MAX
μPD449-1: 18 mA TYP, 26 mA MAX
μPD449-2: 20 mA TYP, 30 mA MAX
μPD449-3: 25 mA TYP, 38 mA MAX

MEMORY

CAPACITANCE

$T_a = 25°C$, f = 1.0 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		6	pF	$V_{IN} = 0V$
Input/Output Capacitance	$C_{I/O}$		8	pF	$V_{I/O} = 0V$

AC CHARACTERISTICS

READ CYCLE

$V_{CC} = 5.0V \pm 10\%$, $T_a = -40°C$ to $+85°C$

PARAMETER	SYMBOL	μPD449-3 MIN	μPD449-3 MAX	μPD449-2 MIN	μPD449-2 MAX	μPD449-1 MIN	μPD449-1 MAX	μPD449 MIN	μPD449 MAX	UNIT
Read Cycle Time	t_{RC}	150		200		250		450		ns
Access Time	t_A		150		200		250		450	ns
Chip Enable ($\overline{CE}$1) to Output Valid	t_{CO1}		150		200		250		450	ns
Chip Enable ($\overline{CE}$2) to Output Valid	t_{CO2}		150		200		250		450	ns
Output Hold from Address Change	t_{OH}	15		15		15		15		ns
Chip Enable ($\overline{CE}$1) to Output in LZ	t_{LZ1}	5		5		5		5		ns
Chip Enable ($\overline{CE}$2) to Output in LZ	t_{LZ2}	5		5		5		5		ns
Chip Enable ($\overline{CE}$1) to Output in HZ	t_{HZ1}		50		60		80		100	ns
Chip Enable ($\overline{CE}$2) to Output in HZ	t_{HZ2}		50		60		80		100	ns

WRITE CYCLE

$V_{CC} = 5.0V \pm 10\%$, $T_a = -40°C$ to $+85°C$

PARAMETER	SYMBOL	μPD449-3 MIN	μPD449-3 MAX	μPD449-2 MIN	μPD449-2 MAX	μPD449-1 MIN	μPD449-1 MAX	μPD449 MIN	μPD449 MAX	UNIT
Write Cycle Time	t_{WC}	150		200		250		450		ns
Chip Enable ($\overline{CE}$1) to End of Write	t_{CW1}	120		150		180		210		ns
Chip Enable ($\overline{CE}$2) to End of Write	t_{CW2}	120		150		180		210		ns
Address Setup Time	t_{AW}	0		0		0		0		ns
Write Pulsewidth	t_{WP}	90		120		150		180		ns
Write Recovery Time	t_{WR}	0		0		0		0		ns
Write Enable to Output in HZ	t_{WZ}		50		60		80		100	ns
Output Active from End of Write	t_{OW}	10		10		10		10		ns
Data Valid to End of Write	t_{DW}	50		60		80		100		ns
Data Hold Time	t_{DH}	0		0		0		0		ns

LOW V_{CC} DATA RETENTION

$T_a = -40°C$ to $+85°C$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC} for Data Retention	V_{CCDR}	$V_{IN} = 0 \sim V_{CC}$, $V_{\overline{CE}1}$ or $V_{\overline{CE}2} = V_{CC}$	2.0			V
Data Retention Current	I_{CCDR}	$V_{CC} = 3.0V$, $V_{IN} = 0 \sim V_{CC}$ $V_{\overline{CE}1}$ or $V_{\overline{CE}2} = V_{CC}$		0.01	10	μA
Chip Disable to Data Retention Time	t_{CDR}		0			ns
Operation Recovery Time	t_R		t_{RC}			ns

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μPD2308A
NMOS READ ONLY MEMORY
1,024 WORDS, 8 BITS/WORD

FEATURES:

- **Two Fast Access Times:**
  —450nsec
  —350nsec
- **All Inputs TTL Compatible**
- **All Outputs Drive 2 TTL Load Directly**
- **Single +5 Volt Supply with ± 10% Tolerance**
- **Three-State Outputs for Direct Bus Compatibility**
- **Pin Compatible to 2708 EPROM**
- **Fully Static Operation**
- **All Inputs Protected Against Static Charge**
- **100% Burned-In**

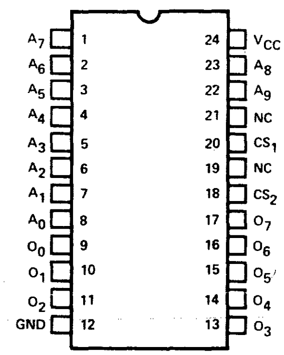
GENERAL DESCRIPTION:

The μPD2308A is a 8,192 bit Read Only Memory, utilizing MOS N-Channel silicon gate technology. The device is completely static in operation and is organized as 1024 words by 8 bits and operates from a single +5 volt power supply. All inputs and outputs are fully TTL compatible. It has two programmable chip selects, and Pins 21 and 19 have no connection (NC) to allow full plug-in compatibility with 2708 EPROMs. Programming of the device is done through a custom mask during fabrication.

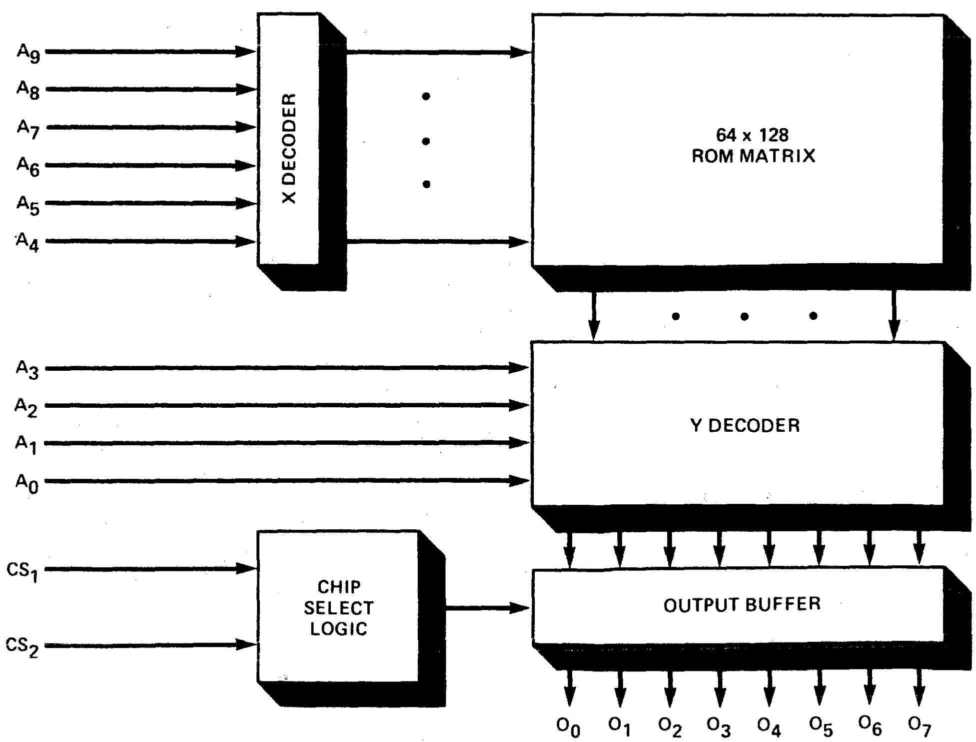
ORDERING INFORMATION

PART NUMBER INDUSTRIAL	ACCESS TIME	PACKAGE
μPD 2308A-45PC	450nsec	Molded DIP
μPD 2308A-35PC	350nsec	Molded DIP

PIN CONFIGURATION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply Voltage	−0.5 to +7	V
V_I	Input Voltage	−0.5 to +7	V
V_O	Output Voltage	−0.5 to +7	V
T_{opt}	Operating Temperature	−0 to +70	°C
T_{stg}	Storage Temperature	−65 to +125	°C

Stresses more severe than those listed here may cause permanent damage to the device. This is a stress rating only, and operation of the device at any condition above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS (T_a = 0° to +70°C, V_{CC} = +5 ± 10%)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input "Low" Voltage		−0.5		0.8	V
V_{IH}	Input "High" Voltage		2.0		V_{CC} + 1	V
I_{IL}	Input Load Current	V_{IN} = 0 to +5.50V			10	μA
V_{OL}	Output "Low" Voltage	I_{OL} = +3.2mA			0.40	V
V_{OH}	Output "High" Voltage	I_{OH} = −200μA	2.4			V
I_{LO}	Output Leakage Current	Chip Disabled V_{OUT} = +0.4V to V_{CC}			10	μA
I_{CC}	Power Supply Current	All inputs +5.50V Outputs Unloaded		60	90	mA

A.C. CHARACTERISTICS (T_a = 0° to +70°C, V_{CC} = +5 ± 10%)

		μPD2308A-35		μPD2308A-45		
Symbol	Parameter	Min.	Max.	Min.	Max.	Units
t_{ACC}	Access Time		350		450	nsec
t_{CO}	Output Enable Time		150		150	nsec
t_{DF}	Output Disable Time		100		100	nsec
t_{OH}	Output Hold Delay	20		20		nsec
C_I	Input Capacitance		7		7	pf
C_O	Output Capacitance		10		10	pf

A.C. TEST CONDITIONS

Input rise and fall times (t_r, t_f) = 20 nsec
Timing Measurement Reference Levels:
  Input and output high levels (V_{IH}, V_{OH}) = 2.0 Volts
  Input and output low levels (V_{IL}, V_{OL}) = 0.8 Volts
Output load = 1 series 74 TTL + 100 pf

CUSTOM PROGRAMMING INSTRUCTIONS

BIT PATTERN SUBMITTAL OPTIONS:

The customer's unique bit pattern can be submitted in a convenient method that is easy for the ROM customer, and readily verifiable for accuracy. The bit pattern can be delivered to NEC contained within:

1. One programmed 2708 EPROM

BIT PATTERN VERIFICATION:

For customer verification of the submitted bit patterns, several alternatives are also available. The following is found to be most expeditious.

CUSTOM PATTERN SUBMITTED VIA:	VERIFICATION ROUTINE
1. One programmed 2708 EPROM	Customer sends NEC one additional erased 2708. NEC programs the spare 2708 with the data from the programmed 2708, and returns to customer for verification.

NEC Electronics

MEMORY

μPD2316E
NMOS READ ONLY MEMORY
2,048 WORDS, 8 BITS/WORD

FEATURES:

- **Two Fast Access Times:**
  —450nsec
  —350nsec
- **All Inputs TTL Compatible**
- **Single +5 V ± 10% Supply**
- **Three-State Outputs for Direct Bus Compatibility**
- **Pin Compatible to 2708 and 2716 EPROMs**
- **Fully Static Operation**
- **Inputs Static Charge Protected**
- **100% Burned-In**

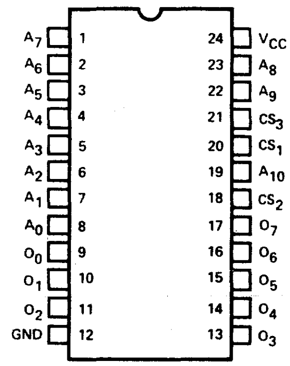
GENERAL DESCRIPTION:

The μPD2316E is a 16,384 bit Read Only Memory utilizing MOS N-Channel silicon gate technology. The device is completely static in operation and is organized as 2048 words by 8 bits and operates from a single +5 volt power supply. All inputs and outputs are fully TTL compatible. It has three programmable chip select inputs and three state outputs that allow memory expansion to 16,384 words by 8 bits without the use of external logic. Programming of the device is accomplished by a custom mask during fabrication. Pinout is compatible with 2708 and 2716 EPROMs.

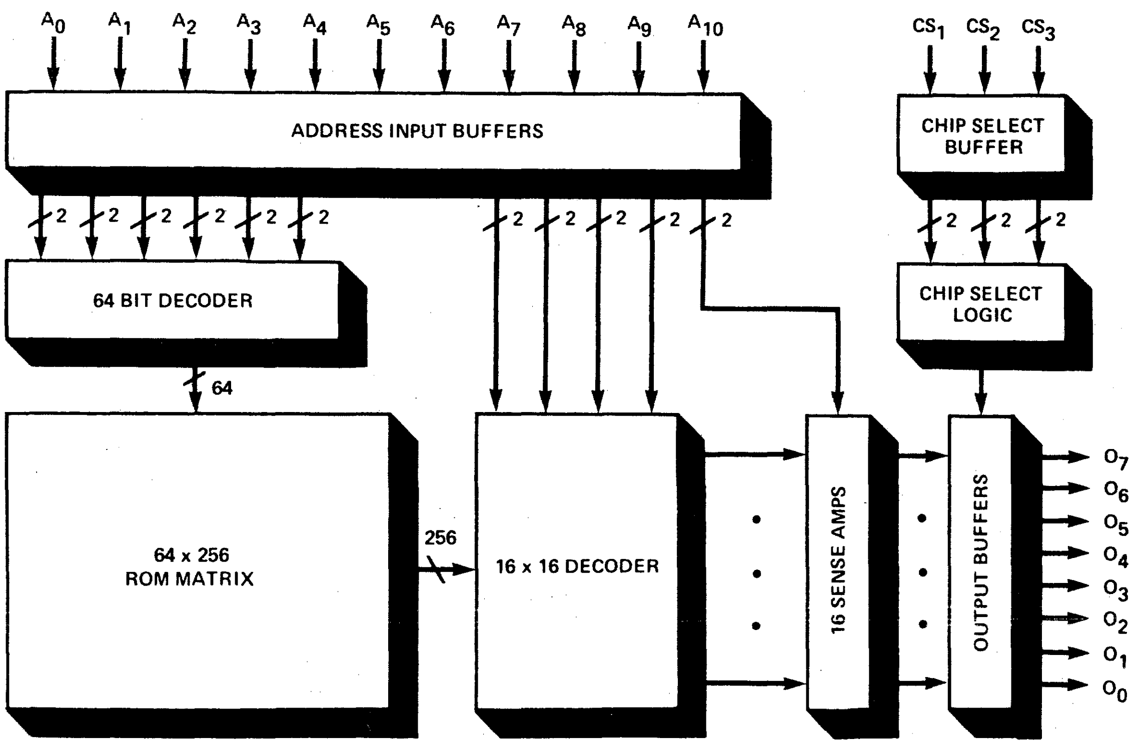
ORDERING INFORMATION

PART NUMBER INDUSTRIAL	ACCESS TIME	PACKAGE
μPD 2316E-45PC	450nsec	Molded DIP
μPD 2316E-35PC	350nsec	Molded DIP

PIN CONFIGURATION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply Voltage	−0.5 to +7	V
V_I	Input Voltage	−0.5 to +7	V
V_O	Output Voltage	−0.5 to +7	V
T_{opt}	Operating Temperature	−0 to +70	°C
T_{stg}	Storage Temperature	−65 to +125	°C

Stresses more severe than those listed here may cause permanent damage to the device. This is a stress rating only, and operation of the device at any condition above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS (T_a = 0°C to +70°C, V_{CC} = +5±10%)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input "Low" Voltage		−0.5		0.8	V
V_{IH}	Input "High" Voltage		2.0		V_{CC} + 1	V
I_{IL}	Input Load Current	V_{IN} = 0 to +5.50V			10	μA
V_{OL}	Output "Low" Voltage	I_{OL} = +3.2mA			0.40	V
V_{OH}	Output "High" Voltage	I_{OH} = −200μA	2.4			V
I_{LO}	Output Leakage Current	Chip Disabled, V_{OUT} = +0.4V to V_{CC}			10	μA
I_{CC}	Power Supply Current	All inputs +5.50V, Outputs Unloaded		60	90	mA

A.C. CHARACTERISTICS (T_a = 0°C to +70°C, V_{CC} = +5±10%)

		μPD2316E-35		μPD2316E-45		
Symbol	Parameter	Min.	Max.	Min.	Max.	Units
t_{ACC}	Access Time		350		450	nsec
t_{CO}	Output Enable Time		150		150	nsec
t_{DF}	Output Disable Time		100		100	nsec
t_{OH}	Output Hold Delay	20		20		nsec
C_I	Input Capacitance		7		7	pf
C_O	Output Capacitance		10		10	pf

A.C. TEST CONDITIONS

Input rise and fall times (t_r, t_f) = 20 nsec
Timing Measurement Reference Levels:
Input and output high levels (V_{IH}, V_{OH}) = 2.0 Volts
Input and output low levels (V_{IL}, V_{OL}) = 0.8 Volts
Output load = 1 series 74 TTL + 100 pf

CUSTOM PROGRAMMING INSTRUCTIONS

BIT PATTERN SUBMITTAL OPTIONS:

The customer's unique bit pattern can be submitted in several convenient methods that are easy for the ROM customer, and readily verifiable for accuracy. The bit pattern can be delivered to NEC contained within:

1. One programmed 2716 EPROM
2. Two programmed 2708 EPROMs

BIT PATTERN VERIFICATION:

For customer verification of the submitted bit patterns, several alternatives are also available. The following are those found to be most expeditious.

CUSTOM PATTERN SUBMITTED VIA:	VERIFICATION ROUTINE
1. One programmed 2716 EPROM	Customer sends NEC one additional erased 2716. NEC programs the spare 2716 with the data extracted from the programmed 2716, and returns to the customer for verification.
2. Two programmed 2708's EPROMs	Customer sends NEC two additional erased 2708's. NEC programs the spare 2708's with the pattern data extracted from the programmed 2708's and returns to the customer for verification.

μPD2332 NMOS READ ONLY MEMORY 4096 WORDS, 8 BITS/WORD

FEATURES:

- **Three Fast Access Times**
  -450nsec
  -350nsec
  -300nsec
- **All Inputs TTL Compatible**
- **Outputs Drive 2 TTL Loads Directly**
- **Single +5V ± 10% Supply**
- **Two Programmable Chip Selects**
- **Both JEDEC Pinouts Available**

	PIN 18	PIN 21
μPD2332A	A11	CS2
μPD2332B	CS2	A11

- **Pin Compatible to 2716 and 2732 EPROMS**
- **Fully Static Operation**
- **All Inputs Protected Against Static Charge**
- **100% Burned-In**

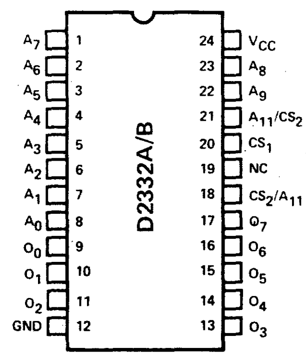
ORDERING INFORMATION

PART NUMBER	PIN 18	PIN 21	ACCESS TIME	PACKAGE
μPD 2332A-45PC	A11	CS2	450ns	Molded DIP
μPD 2332A-35PC	A11	CS2	350ns	Molded DIP
μPD 2332A-30PC	A11	CS2	300ns	Molded DIP
μPD 2332B-45PC	CS2	A11	450ns	Molded DIP
μPD 2332B-35PC	CS2	A11	350ns	Molded DIP
μPD 2332B-30PC	CS2	A11	300ns	Molded DIP

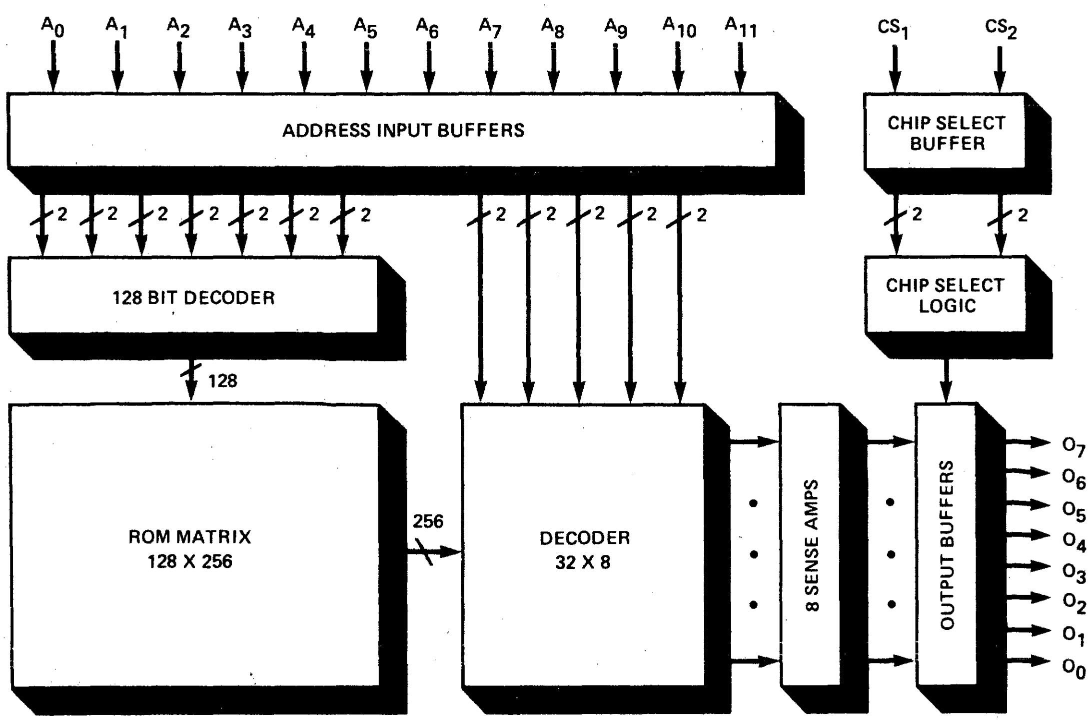
GENERAL DESCRIPTION:

The μPD2332A/B is a 32,768 bit fully static Read Only Memory utilizing MOS N-Channel silicon gate ion implanted technology. It is organized 4096 words by 8 bits and operates from a single +5V ± 10% power supply. All inputs are TTL compatible. It has two programmable chip selects and three-state outputs for direct bus compatibility. It is unique in that both JEDEC standard pin configurations are available.

PIN CONFIGURATION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply Voltage	−0.5 to +7	V
V_I	Input Voltage	−0.5 to +7	V
V_O	Output Voltage	−0.5 to +7	V
T_{opt}	Operating Temperature	−0 to +70	°C
T_{stg}	Storage Temperature	−65 to +125	°C

Stresses more severe than those listed here may cause permanent damage to the device. This is a stress rating only, and operation of the device at any condition above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS (T_a = 0° to +70°C, V_{CC} = +5 ± 10%)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input "Low" Voltage		−0.5		0.8	V
V_{IH}	Input "High" Voltage		2.0		V_{CC} +1	V
I_{IL}	Input Load Current	V_{IN} = 0 to 5.5V			10	μA
V_{OL}	Output "Low" Voltage	I_{OL} = +3.2mA			0.40	V
V_{OH}	Output "High" Voltage	I_{OH} = −200μA	2.4			V
I_{LO}	Output Leakage Current	Chip Disabled V_{OUT} = +0.4V to V_{CC}			10	μA
I_{CC}	Power Supply Current	All inputs +5.5V Output Unloaded		60	90	mA

A.C. CHARACTERISTICS (T_a = 0° to +70°C, V_{CC} = +5 ± 10%)

		μPD2332A/B-30		μPD2332A/B-35		μPD2332A/B-45		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{ACC}	Access Time		300		350		450	nsec
t_{CO}	Output Enable Time		150		150		150	nsec
t_{DF}	Output Disable Time		100		100		100	nsec
t_{OH}	Output Hold Delay	20		20		20		nsec
C_I	Input Capacitance		7		7		7	pf
C_O	Output Capacitance		10		10		10	pf

A.C. TEST CONDITIONS

Input rise and fall times (t_r, t_f) = 20 nsec
Timing Measurement Reference Levels:
Input and output high levels (V_{IH}, V_{OH}) = 2.0 Volts
Input and output low levels (V_{IL}, V_{OL}) = 0.8 Volts
Output load = 1 series 74 TTL + 100 pf

CUSTOM PROGRAMMING INSTRUCTIONS

BIT PATTERN SUBMITTAL OPTIONS:

The customer's unique bit pattern can be submitted in several convenient methods that are easy for the ROM customer, and readily verifiable for accuracy. The bit pattern can be delivered to NEC contained within:

1. One programmed 2732 EPROM
2. Two programmed 2716 EPROMs

BIT PATTERN VERIFICATIONS:

For customer verification of the submitted bit patterns, several alternatives are also available. The following are those found to be most expeditious.

CUSTOM PATTERN SUBMITTED VIA:	VERIFICATION ROUTINE
1. One programmed 2732 EPROM	Customer sends NEC one additional erased 2732. NEC programs the spare 2732 with the data from the programmed 2732, and returns to customer for verification.
2. Two programmed 2716 EPROMs	Customer sends NEC two additional erased 2716's. NEC programs the spare 2716's with the data from the programmed EPROMs and returns to customer for verification.

NEC Electronics

MEMORY

NEC
NEC Electronics

μPD2364
NMOS READ ONLY MEMORY
8192 WORDS, 8 BITS/WORD

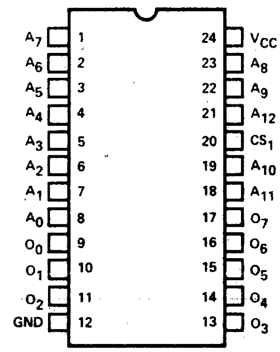
FEATURES:

- **Three Fast Access Times**
  -450nsec
  -350nsec
  -300nsec
- **All Inputs and Outputs TTL Compatible**
- **Single +5V ± 10% Power Supply**
- **One Programmable Chip Select**
- **Three-State Outputs for Direct Bus Compatibility**
- **Pin Compatible to 2716, 2732, and 2564 EPROMS**
- **Fully Static Operation**
- **All Inputs Protected Against Static Charge**
- **100% Burned-In**

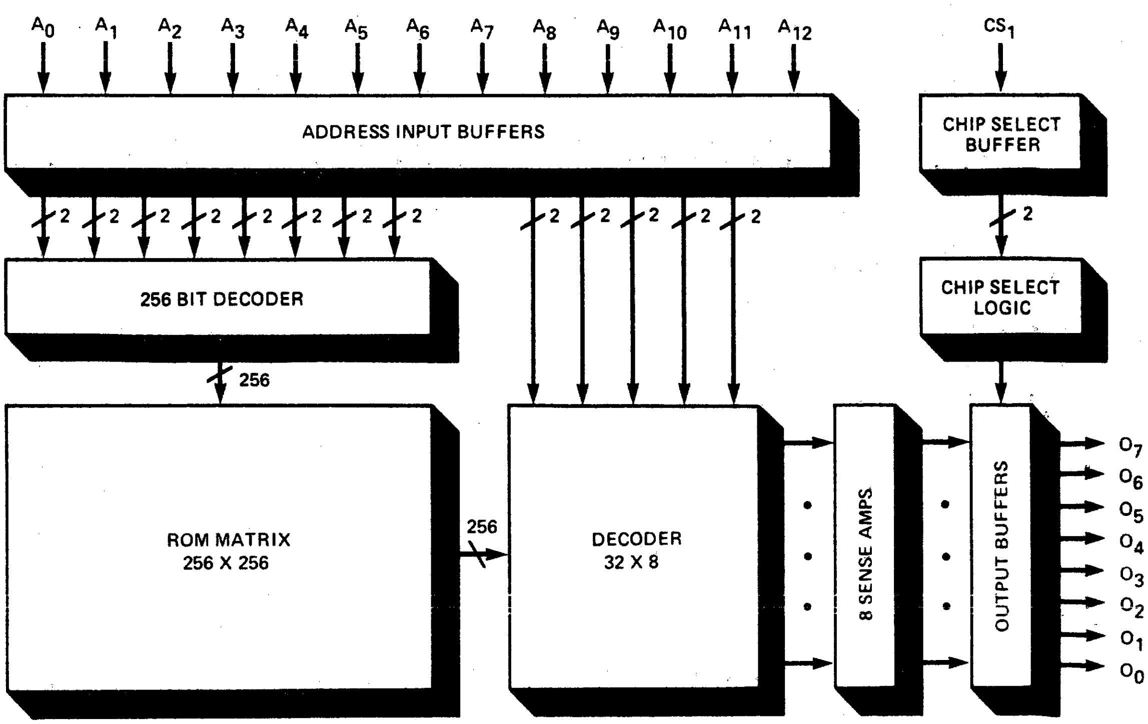
GENERAL DESCRIPTION:

The μPD2364 is a 65,536 bit Read Only Memory utilizing MOS N-Channel silicon gate technology. The device is completely static in operation, organized as 8192 words by 8 bits and operates from a single +5V power supply. All inputs and outputs are fully TTL compatible. It has one programmable chip select input and three-state outputs that allow memory expansion to 16,384 words by 8 bits without the use of external logic. Programming of the device is accomplished by a custom mask during fabrication. Pinout is compatible with 2716, 2732, and 2564 EPROMs.

PIN CONFIGURATION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply Voltage	−0.5 to +7	V
V_I	Input Voltage	−0.5 to +7	V
V_O	Output Voltage	−0.5 to +7	V
T_{opt}	Operating Temperature	−0 to +70	°C
T_{stg}	Storage Temperature	−65 to +125	°C

Stresses more severe than those listed here may cause permanent damage to the device. This is a stress rating only, and operation of the device at any condition above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS (T_a = 0° to +70°C, V_{CC} = +5 ± 10%)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input "Low" Voltage		−0.5		0.8	V
V_{IH}	Input "High" Voltage		2.0		V_{CC} + 1	V
I_{IL}	Input Load Current	V_{IN} = 0 to 5.5V			10	μA
V_{OL}	Output "Low" Voltage	I_{OL} = +2.1mA			0.4	V
V_{OH}	Output "High" Voltage	I_{OH} = −400μA	2.4			V
I_{LO}	Output Leakage Current	Chip Disabled V_{OUT} = +0.4V to V_{CC}			10	μA
I_{CC}	Power Supply Current	All inputs +5.5V Output Disabled		80	140	mA

A.C. CHARACTERISTICS (T_a = 0° to +70°C, V_{CC} = +5 ± 10%)

		μPD2364-30		μPD2364-35		μPD2364-45		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{ACC}	Access Time		300		350		450	nsec
t_{CO}	Output Enable Time		120		150		150	nsec
t_{DF}	Output Disable Time		120		150		150	nsec
t_{OH}	Output Hold Delay	20		20		20		nsec
C_I	Input Capacitance		10		10		10	pf
C_O	Output Capacitance		15		15		15	pf

A.C. TEST CONDITIONS

Input rise and fall times (t_r, t_f) = 20 nsec
Timing Measurement Reference Levels:
Input and output high levels (V_{IH}, V_{OH}) = 2.0 Volts
Input and output low levels (V_{IL}, V_{OL}) = 0.8 Volts
Output load = 1 series 74 TTL + 100 pf

CUSTOM PROGRAMMING INSTRUCTIONS

BIT PATTERN SUBMITTAL OPTIONS:

The customer's unique bit pattern can be submitted in several convenient methods that are easy for the ROM customer, and readily verifiable for accuracy. The bit pattern can be delivered to NEC contained within:

1. One programmed 2764 EPROM
2. Two programmed 2732 EPROMs

BIT PATTERN VERIFICATIONS:

For customer verification of the submitted bit patterns, several alternatives are also available. The following are those found to be most expeditious.

CUSTOM PATTERN SUBMITTED VIA:	VERIFICATION ROUTINE
1. One programmed 2764 EPROM	Customer sends NEC one additional erased 2764. NEC programs the spare 2764 with the data from the programmed 2764, and returns to customer for verification.
2. Two programmed 2732 EPROMs	Customer sends NEC two additional erased 2732's. NEC programs the spare 2732's with the data from the programmed EPROMs and returns to customer for verification.

μPD2364E
NMOS READ ONLY MEMORY
8192 WORDS, 8 BITS/WORD

FEATURES:

- **Two Fast Access Times:**
  -250nsec—μPD2364E-25
  -200nsec—μPD2364E-20
- **All Inputs and Outputs are fully TTL Compatible**
- **Three-State Output for Direct Bus Compatibility**
- **Single +5V ± 5% Power Supply**
- **Three Programmable Chip Selects**
- **All Inputs Protected Against Static Charge**
- **100% Burned-In**

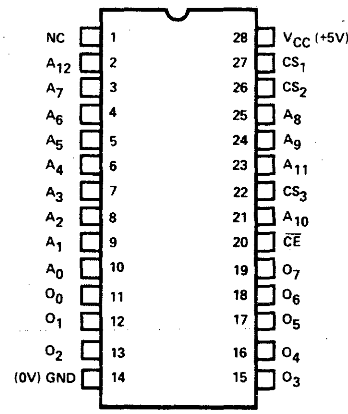
GENERAL DESCRIPTION:

The μPD2364E-20/2364E-25 is a 65,536 bit Read Only utilizing NMOS silicon gate technology. The device is static in operation, organized as 8192 words by 8 bits and operates from a single +5 Volt power supply. The device has three-state outputs and all inputs and outputs are fully TTL compatible. The chip select pins are mask programmable and can be specified by selecting "1", "0" and "Don't Care" Data. Pinout is compatible with 2764 EPROMs.

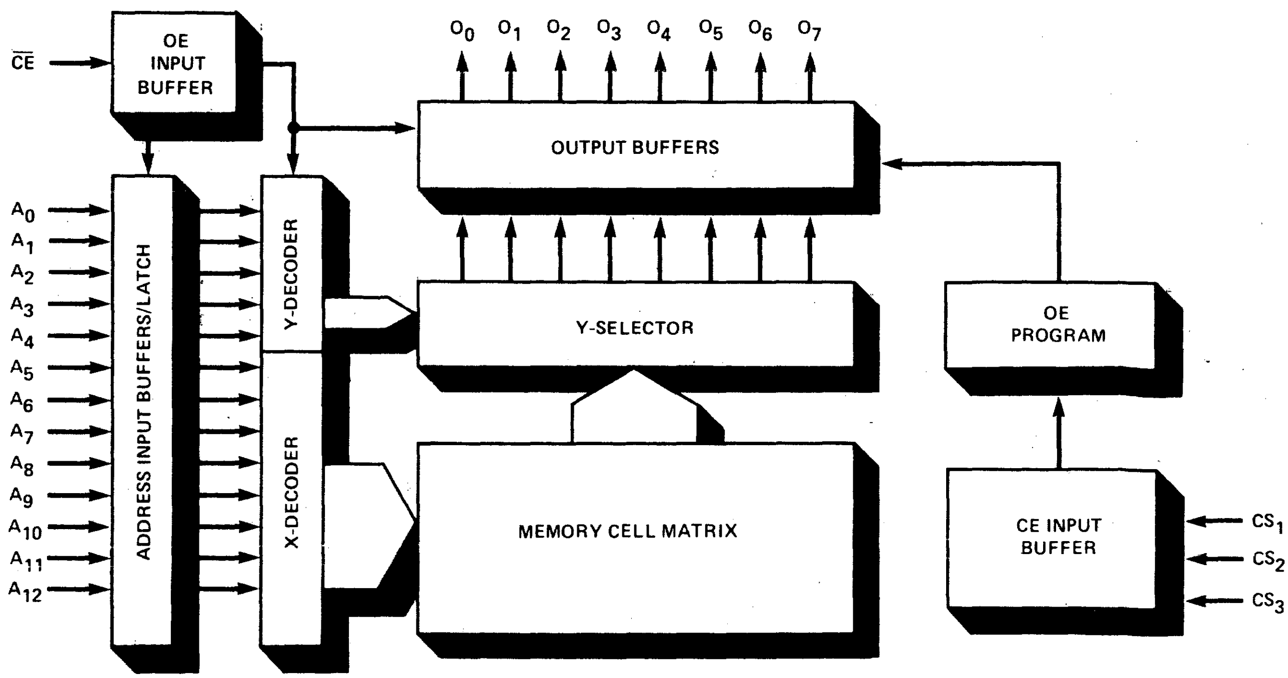
ORDERING INFORMATION

PART NUMBER	ACCESS TIME	PACKAGE
μPD 2364E-25PC	250nsec	Molded 28-PIN DIP
μPD 2364E-20PC	200nsec	Molded 28-PIN DIP

PIN CONFIGURATION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply Voltage	−0.5 to +7	V
V_I	Input Voltage	−0.5 to +7	V
V_O	Output Voltage	−0.5 to +7	V
T_{opt}	Operating Temperature	−0 to +70	°C
T_{stg}	Storage Temperature	−65 to +125	°C

Stresses more severe than those listed here may cause permanent damage to the device. This is a stress rating only, and operation of the device at any condition above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS (T_a = 0° to +70°C, V_{CC} = +5 ± 5%)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IH}	Input "High" Voltage		+2.1		V_{CC} +1.0	V
V_{IL}	Input "Low" Voltage		−0.5		+0.7	V
V_{OH}	Output "High" Voltage	I_{OH} = −400μA	+2.4			V
V_{OL}	Output "Low" Voltage	I_{OL} = +2.1mA			+0.4	V
I_{LIH}	Input Leakage Current High	$V_I = V_{CC}$			+10	μA
I_{LIL}	Input Leakage Current Low	V_I = Ov			−10	μA
I_{LOH}	Output Leakage Current High	$V_O = V_{CC}$, Chip Deselected			+10	μA
I_{LOL}	Output Leakage Current Low	V_O = Ov, Chip Deselected			−10	μA
I_{CC1}	Supply Voltage	CE = V_{IL}		45	85	mA
I_{CC2}	Supply Voltage	CE = V_{IH}, Standby Mode		12	20	mA

A.C. CHARACTERISTICS (T_a = 0° to +70°C, V_{CC} = +5 ± 5%)

			D2364E-25			D2364E-20			
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
t_{ACC}	Access Time	Input Voltage tr, tf = 20ns Timing Reference Levels: Input = 0.8V & 2.0V Output = 0.8V & 2.0V Load 1 TTL + 100 pF			250			200	ns
t_{CE}	Chip Enable Access Time				250			200	ns
t_{OE}	OE_1 to OE_3 Output On Time		10		110	10		100	ns
t_{OH}	Output Hold Time		0			0			ns
t_{DF}	Output Disable Time		0		100	0		90	ns
C_I	Input Capacitance	f = 1MHz			10			10	pF
C_O	Output Capacitance	f = 1MHz			15			15	pF

CUSTOM PROGRAMMING INSTRUCTIONS

BIT PATTERN SUBMITTAL OPTIONS:

The customer's unique bit pattern can be submitted in several convenient methods that are easy for the ROM customer, and readily verifiable for accuracy. The bit pattern can be delivered to NEC contained within:

1. One programmed 2764 EPROM
2. Two programmed 2732 EPROMs

BIT PATTERN VERIFICATIONS:

For customer verification of the submitted bit patterns, several alternatives are also available. The following are those found to be most expeditious.

CUSTOM PATTERN SUBMITTED VIA:	VERIFICATION ROUTINE
1. One programmed 2764 EPROM	Customer sends NEC one additional erased 2764. NEC programs the spare 2764 with the data from the programmed 2764, and returns to customer for verification.
2. Two programmed 2732 EPROMs	Customer sends NEC two additional erased 2732's. NEC programs the spare 2732's with the data from the programmed EPROMs and returns to customer for verification.

NEC Electronics

MEMORY

NEC
NEC Electronics

μPD23128
NMOS READ ONLY MEMORY
16,384 WORDS, 8 BITS/WORD

FEATURES:

- **Fast Access Time: 250nsec Max.**
- **All Inputs and Outputs are TTL Compatible**
- **Single +5 Volt ± 10% Supply**
- **Three-State Outputs for Direct Bus Compatibility**
- **Edge Enabled Operation**
- **Programmable Chip Select for Memory Expansion**
- **Low-Power Standby Mode**
- **All Inputs Protected Against Static Charge**
- **100% Burned-In**

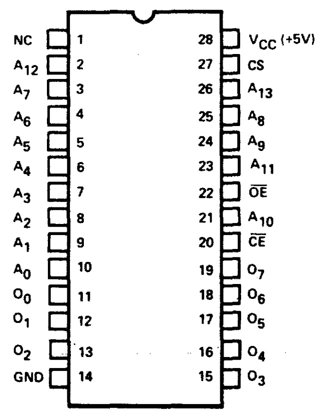
GENERAL DESCRIPTION:

The μPD23128 is a 131,072 bit edge enabled Read Only Memory, utilizing MOS N-Channel silicon gate, ion implanted technology. The device is organized 16,384 words by 8 bits and operates from a single +5 volt supply. All inputs and outputs are fully TTL compatible and the device has one programmable chip select, with three-state outputs that allow memory expansion without the use of external logic. Programming of the device is accomplished during the fabrication process. Pinout is compatible with 27128 EPROMs.

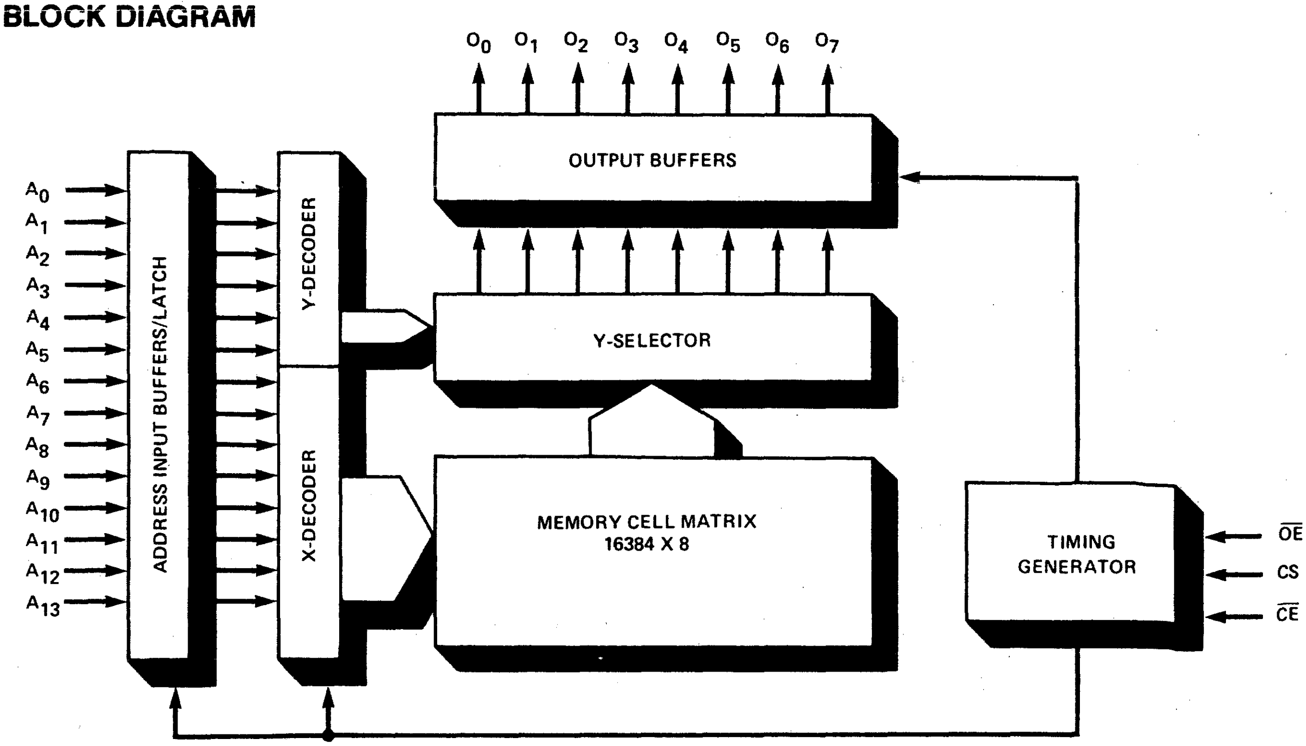
ORDERING INFORMATION

PART NUMBER	ACCESS TIME	PACKAGE
μPD 23128-25PC	250nsec	Plastic DIP

PIN CONFIGURATION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply Voltage	−0.5 to +7	V
V_I	Input Voltage	−0.5 to +7	V
V_O	Output Voltage	−0.5 to +7	V
T_{opt}	Operating Temperature	−0 to +70	°C
T_{stg}	Storage Temperature	−65 to +125	°C

Stresses more severe than those listed here may cause permanent damage to the device. This is a stress rating only, and operation of the device at any condition above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS ($T_a = 0°C$ to $+70°C$, $V_{CC} = +5 \pm 10\%$)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IH}	Input "High" Voltage		+2.0		V_{CC} +1.0	V
V_{IL}	Input "Low" Voltage		−0.5		+0.8	V
V_{OH}	Output "High" Voltage	$I_{OH} = -400\mu A$	+2.4			V
V_{OL}	Output "Low" Voltage	$I_{OL} = +3.2mA$			+0.4	V
I_{LIH}	Input Leakage Current	$V_I = V_{CC}$			+10	μA
I_{LIL}	Input Leakage Current	$V_I = 0_V$			−10	μA
I_{LOH}	Output Leakage Current	$V_O = V_{CC}$, Chip Deselected			+10	μA
I_{LOL}	Output Leakage Current	$V_O = 0_V$, Chip Deselected			−10	μA
I_{CC1}	Power Supply Current	$t_{CYC} = 350ns$		+25	+40	mA
I_{CC2}	Power Supply Current	Standby Mode		+7	+15	mA

A.C. CHARACTERISTICS ($T_a = 0°C$ to $+70°C$, $V_{CC} = +5 \pm 10\%$)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
t_{CYC}	Cycle Time	Output Load = 1TTL + 100pF Input Voltage t_r, t_f = 20 ns Timing Reference Levels: Input Voltage = 0.8V & 2.0V Output Voltage = 0.8V & 2.0V	350			ns
t_{AS}	Address Setup Time		0			ns
t_{AH}	Address Hold Time		60			ns
t_{CE}	Chip Enable Access Time				250	ns
t_{OE}	Output Enable Access Time				120	ns
t_{ACC}	Access Time(1)				250	ns
t_{DF}	Output Disable Time		0		70	ns
t_{CC}	Chip Enable Off Time		50			ns
C_I	Input Capacitance	f = 1MHz			10	pF
C_O	Output Capacitance	f = 1MHz			15	pF

CUSTOM PROGRAMMING INSTRUCTIONS

BIT PATTERN SUBMITTAL OPTIONS:

The customer's unique bit pattern can be submitted in several convenient methods that are easy for the ROM customer, and readily verifiable for accuracy. The bit pattern can be delivered to NEC contained within:

1. One programmed 27128 EPROM
2. Two programmed 2764 EPROMs
2. Four programmed 2732 EPROMs

BIT PATTERN VERIFICATIONS:

For customer verification of the submitted bit patterns, several alternatives are also available. The following are those found to be most expeditious.

CUSTOM PATTERN SUBMITTED VIA:	VERIFICATION ROUTINE
1. One programmed 27128 EPROM	Customer sends NEC one additional erased 27128. NEC programs the spare 27128 with the data from the programmed 27128, and returns to customer for verification.
2. Two programmed 2764 EPROMs	Customer sends NEC two additional erased 2764's. NEC programs the spare 2764's with the data from the programmed 2764's and returns to the customer for verification.
3. Four programmed 2732 EPROMs	Customer sends NEC four additional erased 2732's. NEC programs the spare 2732's with the data from the programmed 2732's and returns to the customer for verification.

μPD23256
NMOS READ ONLY MEMORY
32,768 WORDS, 8 BITS/WORD

FEATURES:

- **Fast Access: 250nsec Max.**
- **All Inputs and Outputs are TTL Compatible**
- **Single +5 Volt ± 10% Supply**
- **Three-State Outputs for Direct Bus Compatibility**
- **Edge Enabled Operation**
- **Low-Power Standby Mode**
- **One Programmable Chip Select for Memory Expansion**
- **All Inputs Protected Against Static Charge**
- **100% Burned-In**

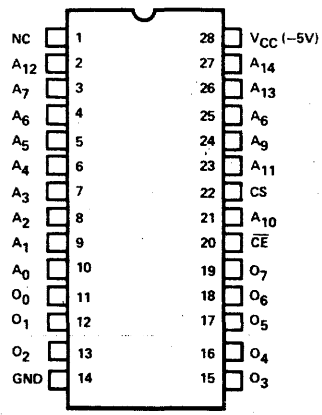
GENERAL DESCRIPTION:

The μPD23256 is a 262,144 bit edge enabled Read Only Memory, utilizing MOS N-Channel silicon gate, ion implanted technology. The device is organized 32,768 words by 8-bits and operates from a single +5 Volt supply. All inputs and outputs are fully TTL compatible with one programmable chip select, and the device has three-state outputs that allow memory expansion without the use of external logic. Programming of the device is accomplished during the fabrication process and the pinout is compatible with 27128 EPROMs.

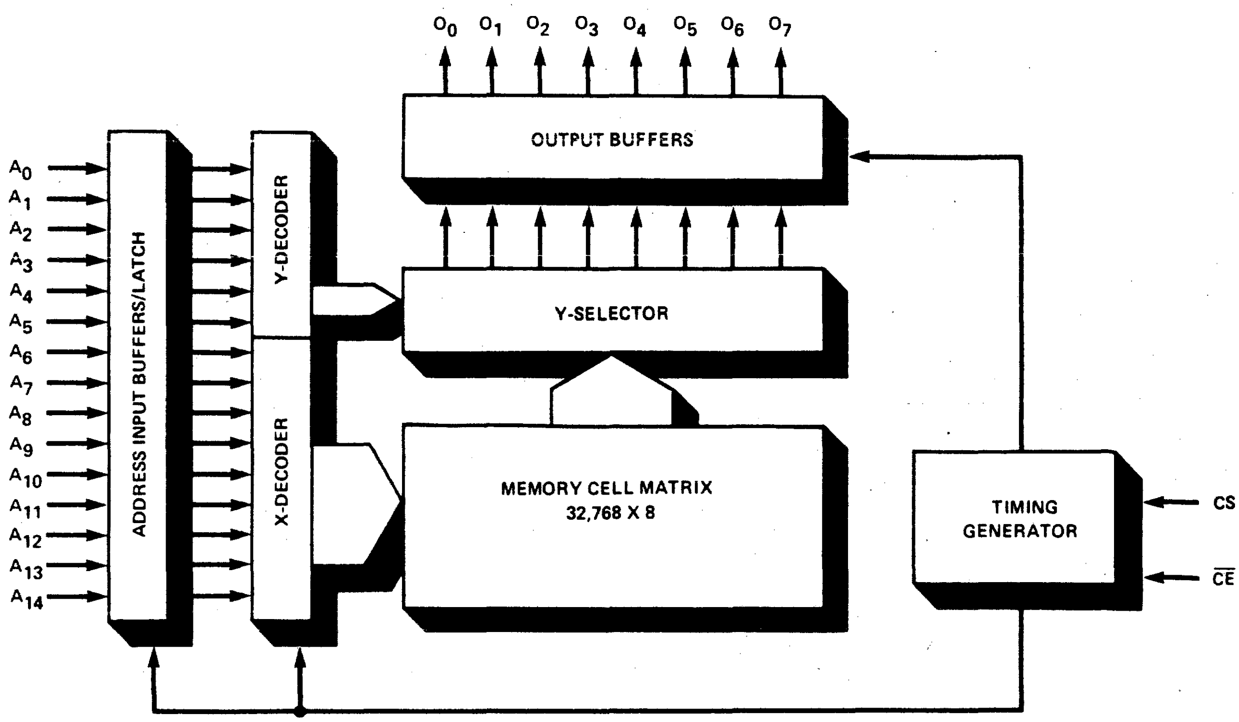
ORDERING INFORMATION

PART NUMBER	ACCESS TIME	PACKAGE
μPD 23256-25PC	250nsec	Plastic DIP

PIN CONFIGURATION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply Voltage	−0.5 to +7	V
V_I	Input Voltage	−0.5 to +7	V
V_O	Output Voltage	−0.5 to +7	V
T_{opt}	Operating Temperature	−0 to +70	°C
T_{stg}	Storage Temperature	−65 to +125	°C

Stresses more severe than those listed here may cause permanent damage to the device. This is a stress rating only, and operation of the device at any condition above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS (T_a = 0° C to +70° C, V_{CC} = +5 ± 10%)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IH}	Input "High" Voltage		+2.0		V_{CC} +1.0	V
V_{IL}	Input "Low" Voltage		−0.5		+0.8	V
V_{OH}	Output "High" Voltage	I_{OH} = −400μA	+2.4			V
V_{OL}	Output "Low" Voltage	I_{OH} = +3.2mA			+0.4	V
I_{LIH}	Input Leakage Current High	V_I = V_{CC}			+10	μA
I_{LIL}	Input Leakage Current Low	V_I = O_V			−10	μA
I_{LOH}	Output Leakage Current High	V_O = V_{CC}, Chip Deselected			+10	μA
I_{LOL}	Output Leakage Current Low	V_O = O_V, Chip Deselected			−10	μA
I_{CC1}	Power Supply Current	t_{CYC} = 350ns		+25	+40	mA
I_{CC2}	Power Supply Current	Standby Mode		+8	+15	mA

A.C. CHARACTERISTICS (T_a = 0° C to +70° C, V_{CC} = +5 ± 10%)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
t_{CYC}	Cycle Time	Input Rise/Fall Times: 20ns Timing Reference Levels: Input Voltage = 0.8V & 2.0V Output Voltage = 0.8V & 2.0V Output Load = 1 TTL + 100pF	350			ns
t_{AS}	Address Setup Time		0			ns
t_{AH}	Address Hold Time		60			ns
t_{ACC}	Access Time(1)				250	ns
t_{CE}	Chip Enable Access Time				250	ns
t_{OE}	Output Enable Access Time				120	ns
t_{DF}	Output Disable Time		0		70	ns
t_{CC}	Chip Enable Off Time		50			ns
C_I	Input Capacitance	f = 1MHz			10	pF
C_O	Output Capacitance	f = 1MHz			15	pF

CUSTOM PROGRAMMING INSTRUCTIONS

BIT PATTERN SUBMITTAL OPTIONS:

The customer's unique bit pattern can be submitted in several convenient methods that are easy for the ROM customer, and readily verifiable for accuracy. The bit pattern can be delivered to NEC contained within:

1. Two programmed 27128 EPROMs
2. Four programmed 2764 EPROMs

BIT PATTERN VERIFICATIONS:

For customer verification of the submitted bit patterns, several alternatives are also available. The following are those found to be most expeditious.

CUSTOM PATTERN SUBMITTED VIA:	VERIFICATION ROUTINE
1. Two programmed 27128 EPROMs	Customer sends NEC two additional erased 27128's. NEC programs the spare 27128's with the data from the programmed 27128's, and returns to the customer for verification.
2. Four programmed 2764 EPROMs	Customer sends NEC four additional erased 2764's. NEC programs the spare 2764's with the data from the programmed 2764's, and returns to the customer for verification.

μPD231000 NMOS READ ONLY MEMORY 131,072 WORDS, 8 BITS/WORD

FEATURES:

- **Two Fast Access Times:**
  —350nsec-μPD231000-35
  —300nsec-μPD231000-30
- **All Inputs and Outputs are Fully TTL Compatible**
- **Single +5 Volt Power Supply**
- **Three-State Outputs for Direct Bus Compatibility**
- **Edge Enabled Operation**
- **Low Power Standby Mode**
- **All Inputs Protected Against Static Charge**
- **100% Burned-In**

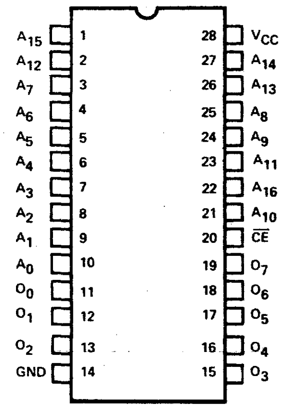
GENERAL DESCRIPTION:

The μPD231000 is a 1,048,576 bit Read Only Memory, utilizing NMOS silicon gate technology. The device is edge enabled, organized as 131,072 words by 8 bits and operates from a single +5 Volt power supply. All inputs and outputs are fully TTL compatible. The device has three state outputs for direct bus interface. The device has a low-power stand-by mode and is available in two speed versions (300 and 350nsec). Programming of the device is accomplished by a custom mask during the fabrication process.

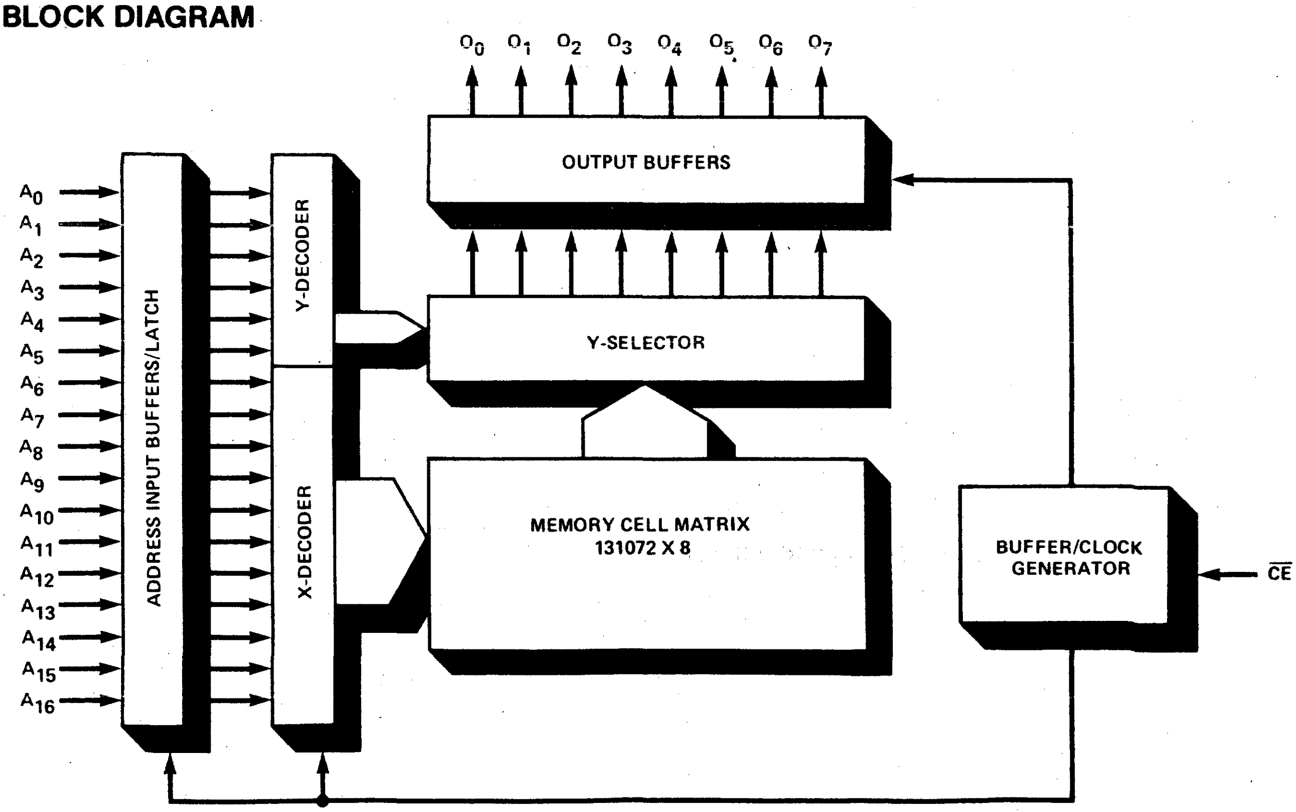
ORDERING INFORMATION

PART NUMBER	ACCESS TIME	PACKAGE
μPD 231000-35PC	350nsec	Plastic DIP
μPD 231000-30PC	300nsec	Plastic DIP

PIN CONFIGURATION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply Voltage	−0.5 to +7	V
V_I	Input Voltage	−0.5 to +7	V
V_O	Output Voltage	−0.5 to +7	V
T_{opt}	Operating Temperature	−0 to +70	°C
T_{stg}	Storage Temperature	−65 to +125	°C

Stresses more severe than those listed here may cause permanent damage to the device. This is a stress rating only, and operation of the device at any condition above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS (T_a = 0° to +70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IH}	Input "High" Voltage		+2.0		V_{CC} +1.0	V
V_{IL}	Input "Low" Voltage		−0.5		+0.8	V
V_{OH}	Output "High" Voltage	I = −400μA	+2.4			V
V_{OL}	Output "Low" Voltage	I = +3.2mA			+0.4	V
I_{LIH}	Input Leakage Current High	V = V_{CC}			+10	μA
I_{LIL}	Input Leakage Current Low	V = O_V			−10	μA
I_{LOH}	Output Leakage Current High	V = V_{CC}, Chip Deselected			+10	μA
I_{LOL}	Output Leakage Current Low	V = 0V, Chip Deselected			−10	μA
I_{CC1}	Power Supply Current	Operating Mode (Average) t_{CYC} = 450ns		35	50	mA
I_{CC2}	Power Supply Current	Standby Mode		8	15	mA

A.C. CHARACTERISTICS (T_a = 0°C to +70°C, V_{CC} = +5V ± 10%)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
t_{CYC}	Cycle Time	Input Voltage t_r, t_f = 20 ns Timing Reference Levels: Input Voltage = 0.8V & 2.0V Output Voltage = 0.8V & 2.0V Output Load = 1TTL + 100pF	450			ns
t_{AS}	Address Setup Time		0			ns
t_{AH}	Address Hold Time		100			ns
t_{ACC}	Access Time				350	ns
t_{CE}	Chip Enable Access Time				350	ns
t_{CC}	Chip Enable Off Time		70			ns
C_I	Input Capacitance	f = 1MHz			10	pF
C_O	Output Capacitance	f = 1MHz			15	pF

CUSTOM PROGRAMMING INSTRUCTIONS

BIT PATTERN SUBMITTAL OPTIONS:

The customer's unique bit pattern can be submitted in a convenient method that is easy for the ROM customer, and readily verifiable for accuracy. The bit pattern can be delivered to NEC contained within:

1. Eight programmed 27128 EPROMs

BIT PATTERN VERIFICATIONS:

For customer verification of the submitted bit patterns, several alternatives are also available. The following are those found to be most expeditious.

CUSTOM PATTERN SUBMITTED VIA:	VERIFICATION ROUTINE
1. Eight programmed 27128 EPROMs	Customer sends NEC eight additional erased 27128's. NEC programs the spare 27128's with the data from the programmed 27128's, and returns to the customer for verification.

μPD23C128
CMOS READ ONLY MEMORY
16,384 WORDS, 8 BITS/WORD

FEATURES:

- 16,384 Words by 8 Bits
- Access Time: 5μsec V_{CC} = 5V ± 10%
- Low Power Consumption—CMOS Technology
- One Mask Programmable Chip Select
- Three State Output for Direct Bus Interface
- Built for Direct Interface with 8048/8048 μproc.
- Single Power Supply (3.5-5.5V)
- 100% Burned-In

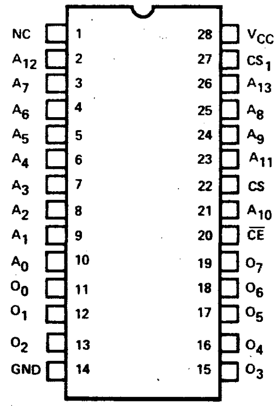
ORDERING INFORMATION

PART NUMBER	ACCESS TIME	PACKAGE
μPD 23C128PC	5μsec	28 Pin Molded DIP

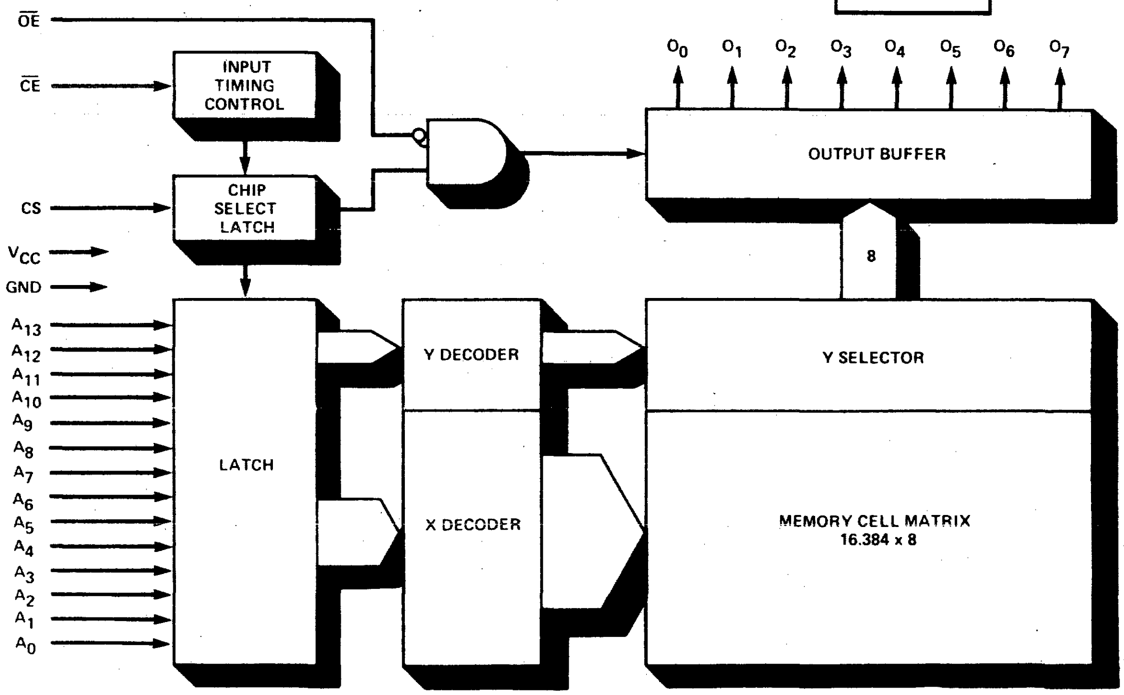
GENERAL DESCRIPTION:

The μPD23C128 is a 131,072 bit Read Only Memory utilizing low power CMOS technology. The device is mask programmable and is organized 16,384 words, by 8 bits/word and operates from a single 3.5-5.5 volt supply. The device has one mask programmable chip select input for simple memory expansion and has three-state output for direct bus interface.

PIN CONFIGURATION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply Voltage	-0.3 ~ +7	V
V_I	Input Voltage	-0.3 ~ V_{CC} +0.3	V
V_O	Output Voltage	-0.3 ~ V_{CC} +0.3	V
T_{opt}	Operating Temperature	-10 ~ +70	°C
T_{stg}	Storage Temperature	-40 ~ +125	°C

Stresses more severe than those listed here may cause permanent damage to the device. This is a stress rating only, and operation of the device at any condition above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS ($T_a = 0°$ to $+70°C$)

Symbol	Parameter	Test Condition	$V_{CC} = 5V \pm 10\%$ Min.	Typ.	Max.	V_{CC} = 3.5 to 5.5V Min.	Typ.	Max.	Unit
V_{IH}	Input "High" Voltage		$0.7V_{CC}$		V_{CC}	$0.7V_{CC}$		V_{CC}	V
V_{IL}	Input "Low" Voltage				0.7			0.5	V
V_{OH}	Output "High" Voltage	$I_{OH} = -1.0mA$	2.4						V
		$I_{OH} = -0.5mA$	3.5						V
		$I_{OH} = -200\mu A$				3.0			V
V_{OL}	Output "Low" Voltage	$I_{OL} = 1.0mA$			0.45				V
		$I_{OL} = 200\mu A$						0.5	V
I_{LIH}	Input Leakage Current High	$V_I = V_{CC}$			1.0			1.0	μA
I_{LIL}	Input Leakage Current Low	$V_I = 0V$			−1.0			−1.0	μA
I_{LOH}	Output Leakage Current High	$V_O = V_{CC}$			1.0			1.0	μA
I_{LOL}	Output Leakage Current Low	$V_O = 0V$			−1.0			−1.0	μA
I_{CC1}	Supply Current			1	4		1	4	mA
I_{CC2}		Chip		0.1	0.4		0.1	0.4	mA
I_{CC3}		Deselect *1			2			2	μA

*1 = No transition on input signals

A.C. CHARACTERISTICS ($T_a = 0°$ to $+70°C$)

Symbol	Parameter	Condition	$V_C = 5V \pm 10\%$ Min.	Typ.	Max.	V_{CC} = 3.5 to 5.5V Min.	Typ.	Max.	Unit
t_{CYC}	Cycle Time	$C_L = 50$ pF	5.5			11.0			μs
t_{AS}	Address Setup Time		0			0			μs
t_{AH}	Address Hold Time		1.0			2.0			μs
t_{ACC}	Access Time				5.0			10.0	μs
t_{CE}	Chip Enable Access Time				0.75			1.5	μs
t_{DF}	Output Disable Time				0.5			1.0	μs
t_{CO}	Chip Enable Off Time		0.5			1.0			μs

Symbol	Parameter	Test Condition	Limits Min.	Typ.	Max.	Unit
C_I	Input Capacitance	V = 0V, f = 1MHz			15	pF
C_O	Output Capacitance	$T_a = 25°C$			15	pF

CUSTOM PROGRAMMING INSTRUCTIONS

BIT PATTERN SUBMITTAL OPTIONS:

The customer's unique bit pattern can be submitted in several convenient methods that are easy for the ROM customer, and readily verifiable for accuracy. The bit pattern can be delivered to NEC contained within:

1. One programmed 27128 EPROM
2. Two programmed 2764 EPROMs
3. Four programmed 2732 EPROMs

BIT PATTERN VERIFICATION:

For customer verification of the submitted bit patterns, several alternatives are also available. The following are those found to be most expeditious.

CUSTOM PATTERN SUBMITTED VIA:	VERIFICATION ROUTINE
1. One programmed 27128 EPROM	Customer sends NEC one additional erased 27128. NEC programs the spare 27128 with the data from the programmed 27212 and returns to customer for verification.
2. Two programmed 2764 EPROMs	Customer sends NEC two additional erased 2764's. NEC programs the spare 2764's with the data from the programmed 2764's and returns to the customer for verification.
3. Four programmed 2732 EPROMs	Customer sends NEC four additional erased 2732's. NEC programs the spare 2732's with the data from the programmed 2732's and returns to the customer for verification.

μPD73128G CMOS READ ONLY MEMORY 16,384 WORDS, 8 BITS/WORD

FEATURES:

- **16,384 Words by 8 Bits**
- **Access Time: 5μsec VCC " 5V ± 10%**
- **Low Power Consumption—CMOS Technology**
- **Four Mask Programmable Chip Selects**
- **Three State Output for Direct Bus Interface**
- **Built for Direct Interface with 8048/8748 μproc.**
- **Single Power Supply (3.5-5.5V)**
- **52 Pin Plastic Flat Package**

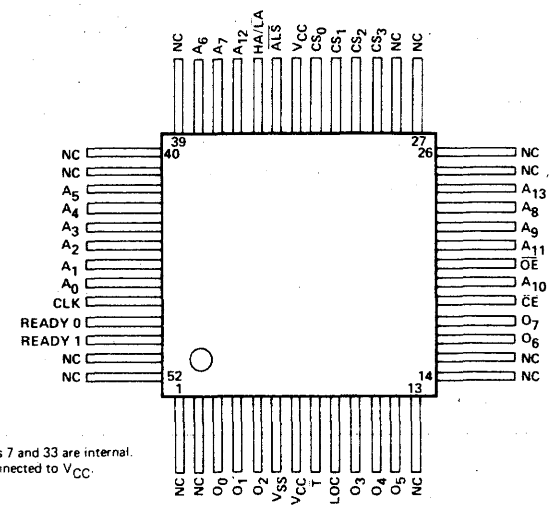
ORDERING INFORMATION

PART NUMBER	ACCESS TIME	PACKAGE
μPD 73128G	5μsec	52 Pin Plastic Flat Package

GENERAL DESCRIPTION:

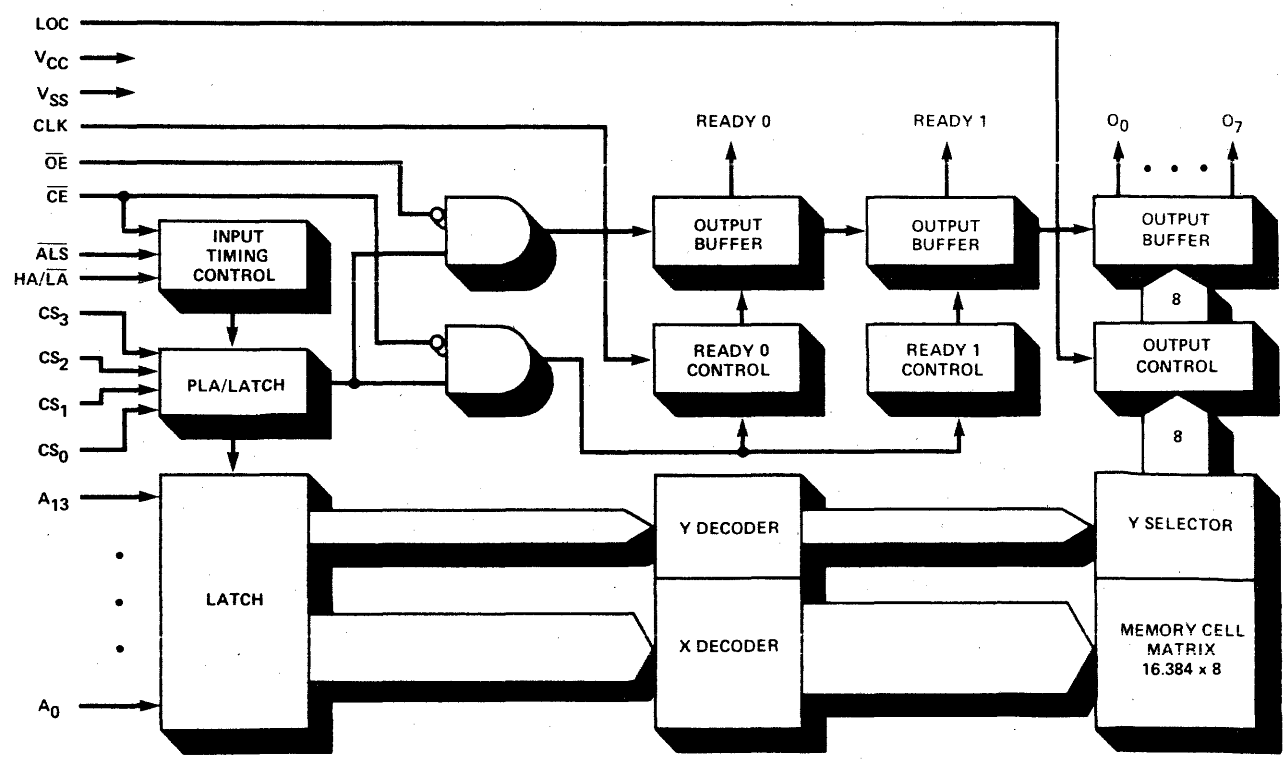
The μPD73128G is a 131,072 bit Read Only Memory utilizing low power CMOS technology. The device is mask programmable and is organized 16,384 words, by 8 bits/word and operates from a single 3.5-5.5 volt supply. The device has four mask programmable chip select inputs for simple memory expansion and has three-state output for direct bus interface.

PIN CONFIGURATION (TOP VIEW)



NOTE: Pins 7 and 33 are internal. Connected to V_{CC}.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply Voltage	−0.3 ~ +7	V
V_I	Input Voltage	−0.3 ~ V_{CC} +0.3	V
V_O	Output Voltage	−0.3 ~ V_{CC} +0.3	V
T_{opt}	Operating Temperature	−10 ~ +70	°C
T_{stg}	Storage Temperature	−40 ~ +125	°C

Stresses more severe than those listed here may cause permanent damage to the device. This is a stress rating only, and operation of the device at any condition above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS (T_a = 0° ~ +70°C)

Symbol	Parameter	Test Condition	V_{CC} = 5V ± 10%			V_{CC} = 2.5 ~ 6.0V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IH}	Input "High" Voltage		0.7V_{CC}		V_{CC}	0.7V_{CC}		V_{CC}	V
V_{IL}	Input "Low" Voltage				0.8			0.4	V
V_{OH}	Output "High" Voltage	I_{OH} = −1.0mA	2.4						V
		I_{OH} = −0.5mA	3.5						V
		I_{OH} = −200μA				2.0			V
V_{OL}	Output "Low" Voltage	I_{OL} = 1.0mA			0.45				V
		I_{OL} = 200μA						0.5	V
I_{LIH}	Input Leakage Current High	V_I = V_{CC}			1.0			1.0	μA
I_{LIL}	Input Leakage Current Low	V_I = 0V			−1.0			−1.0	μA
I_{LOH}	Output Leakage Current High	V_O = V_{CC}			1.0			1.0	μA
I_{LOL}	Output Leakage Current Low	V_O = 0V			−1.0			−1.0	μA
I_{CC1}	Supply Current	Chip Deselected		4	10		4	12	mA
I_{CC2}					10			10	μA

A.C. CHARACTERISTICS (T_a = 0° ~ +70°C)

Symbol	Parameter	Condition	V_{CC} = 5V ± 10%			V_{CC} = 2.5 ~ 6.0V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{C1}	CE Cycle Time		*1			*1			μs
t_{C2}			*2			*2			μs
t_{AS}	Address Setup Time		0.5			1			μs
t_{AH}	Address Hold Time		0.5			1			μs
t_{AC}	Access Time				3			6	μs
t_{HS}	ALS, HA/LA Setup Time		0.75			1.5			μs
t_{HH}	ALS, HA/LA Hold Time	C_L = 50pF	0.75			1.5			μs
t_{OE}	Data Output Delay Time (from OE)				0.75			1.5	μs
t_{ON1}	READY Output Delay Time (from CE)				0.75			1.5	μs
t_{ON2}	READY Output Delay Time (from OE)				0.75			1.5	μs
t_{RD}	READY Enable to Output Delay Time (from CE)				5			10	μs
t_{OF1}	Output Float Delay Time (from CE)				0.5			1	μs
t_{OF2}	Output Float Delay Time (from OE)				0.5			1	μs
t_p	CE Precharge Time		1			2			μs

Symbol	Parameter	Test Condition	Limits Min.	Limits Typ.	Limits Max.	Unit
C_I	Input Capacitance	V_I = 0V, f = 1MHz			15	pF
C_O	Output Capacitance	V_O = 0V, f = 1MHz			15	pF

*1 = $t_{C1} = t_p + t_{AC}$
*2 = $t_{C2} = t_{C1} + t_p + t_{HH} + t_{HS}$
Additional Application Information Is Available.

NEC
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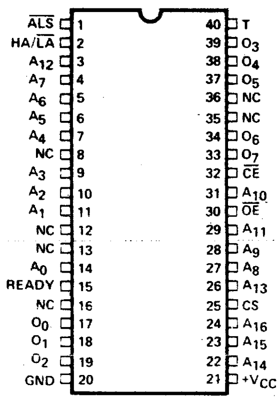
μPD731000 CMOS READ ONLY MEMORY 131,072 WORDS, 8 BITS/WORD

FEATURES:

- One Megabit Programmable Data Capacity
- 131,072 Words by 8 Bits
- Access Time: 3μsec V_{CC} = 5V ± 10%
- Low Power Consumption—CMOS Technology
- Two Mask Programmable Chip Selects
- Three State Output for Direct Bus Interface
- Built for Direct Interface with 8048/8748 μprocessor
- Single Power Supply (3.5-5.5V)
- 52 Pin Plastic Flat Package/40 Pin DIP

ORDERING INFORMATION

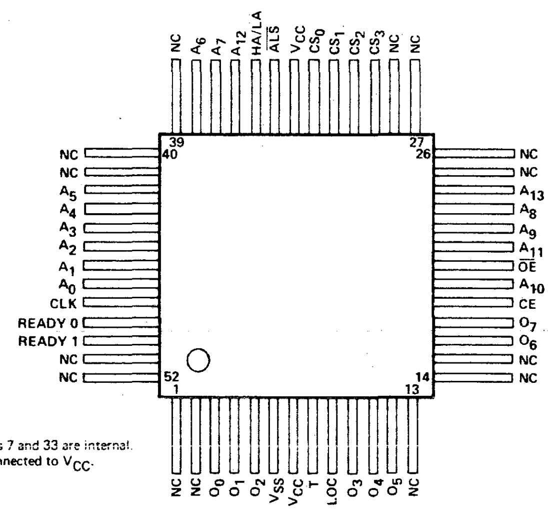
PART NUMBER	ACCESS TIME	PACKAGE
μPD 731000G	5μsec	52 Pin Plastic Flat Package
μPD 738000PC		40 Pin Plastic DIP



GENERAL DESCRIPTION:

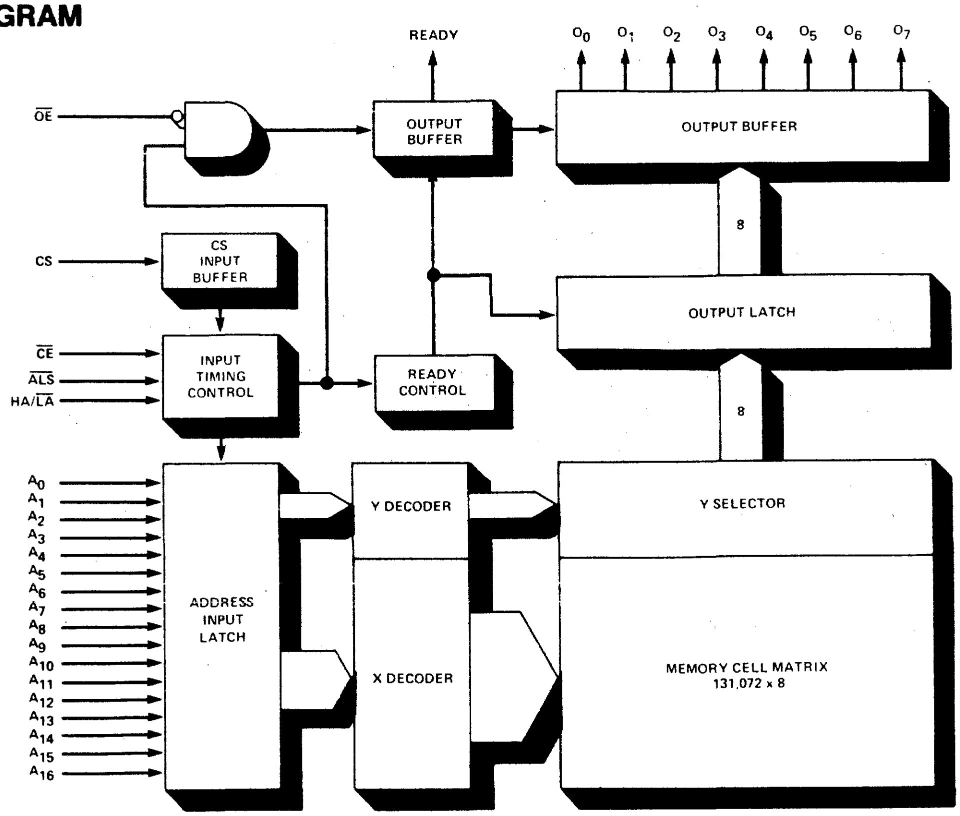
The μPD731000 is a 131,072 bit Read Only Memory utilizing low power CMOS technology. The device is mask programmable and is organized 16,384 words, by 8 bits/word and operates from a single 3.5-5.5 volt supply. The device has one mask programmable chip select inputs for simple memory expansion and has three-state outputs for direct bus interface.

PIN CONFIGURATION (TOP VIEW)



NOTE: Pins 7 and 33 are internal. Connected to V_{CC}.

BLOCK DIAGRAM



NEC Electronics

MEMORY

ABSOLUTE MAXIMUM RATINGS ($T_a = 25°C$)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply Voltage	−0.5 to +7	V
V_I	Input Voltage	−0.5 to +7	V
V_O	Output Voltage	−0.5 to +7	V
T_{opt}	Operating Temperature	−0 to +70	°C
T_{stg}	Storage Temperature	−65 to +125	°C

Stresses more severe than those listed here may cause permanent damage to the device. This is a stress rating only, and operation of the device at any condition above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS ($T_a = 0° \sim +70°C$, $V_{SS} = 0V$)

Symbol	Parameter	Test Condition	$V_{CC} = 5V \pm 10\%$ Min.	Typ.	Max.	$V_{CC} = 2.7 \sim 5.5V$ Min.	Typ.	Max.	Unit
V_{IH}	Input "High" Voltage		$0.7V_{CC}$		V_{CC}	$0.7V_{CC}$		V_{CC}	V
V_{IL}	Input "Low" Voltage				0.8			0.4	V
V_{OH}	Output "High" Voltage	$I_{OH} = -1.0mA$	3.5						V
									V
		$I_{OH} = -200\mu A$				2.0			V
V_{OL}	Output "Low" Voltage	$I_{OL} = 1.0mA$			0.4				V
		$I_{OL} = 200\mu A$						0.5	V
I_{LIH}	Input Leakage Current High	$V_I = V_{CC}$			1.0			1.0	μA
I_{LIL}	Input Leakage Current Low	$V_I = 0V$			−1.0			−1.0	μA
I_{LOH}	Output Leakage Current High	$V_O = V_{CC}$			1.0			1.0	μA
I_{LOL}	Output Leakage Current Low	$V_O = 0V$			−1.0			−1.0	μA
I_{CC1}	Supply Current			5	10		5	12	mA
I_{CC2}		*1 *2		0.1	10		0.1	10	μA
I_{CC3}		*1			10			10	μA

Symbol	Parameter	Test Condition	Limits Min.	Typ.	Max.	Unit
C_I	Input Capacitance	$V_I = 0V$, f = 1MHz			15	pF
C_O	Output Capacitance	$V_O = 0V$, f = 1MHz			15	pF

*1 = Chip is deselected
*2 = Input signal is not changed

A.C. CHARACTERISTICS ($T_a = 0° \sim +70°C$, $V_{SS} = 0V$)

Symbol	Parameter	Condition	$V_{CC} = 5V \pm 10\%$ Min.	Typ.	Max.	$V_{CC} = 2.5 \sim 6.0V$ Min.	Typ.	Max.	Unit
t_{C1}	CE Cycle Time	$C_L = 50pF$	*3			*3			μs
t_{C2}			*4			*4			μs
t_{AS}	Address Setup Time		0.5			1			μs
t_{AH}	Address Hold Time		0.5			1			μs
t_{ACC}	Access Time				3			6	μs
t_{HS}	ALS, HA/LA Setup Time		0.75			1.5			μs
t_{HH}	ALS, HA/LA Hold Time		0.75			1.5			μs
t_{CSS}	CS Setup Time		1			2			μs
t_{OE}	Output Enable Access Time				0.75			1.5	μs
t_{ON1}	READY Output Delay Time (from CE)				0.75			1.5	μs
t_{ON2}	READY Output Delay Time (from OE)				0.75			1.5	μs
t_{RD}	READY Enable to Output Delay Time (from CE)				5			10	μs
t_{OF1}	Output Float Delay Time (from CE)				0.5			1	μs
t_{OF2}	Output Float Delay Time (from OE)				0.5			1	μs
t_p	CE Precharge Time		1			2			μs

*3 = $t_{C1} = t_p + t_{AC}$
*4 = $t_{C2} = t_{C1} + t_p + t_{HH} + t_{HS}$
Additional application information is available.

NEC Electronics

MEMORY

Call on OKI Semiconductor

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PART NUMBER		DESCRIPTION

CMOS MICROPROCESSOR

MSM80C85A	RS	8 BIT CMOS MICROPROCESSOR
MSM80C85A	GSK	8 BIT CMOS MICROPROCESSOR
MSM80C86	RS	16 BIT CMOS MICROPROCESSOR
MSM80C86-2	RS	16 BIT CMOS MICROPROCESSOR
MSM80C87	RS	CMOS NUM. DATA PROC.
MSM80C88	RS	8 BIT CMOS MICROPROCESSOR
MSM80C88-2	RS	8 BIT CMOS MICROPROCESSOR
MSM80C188	RS	8 BIT CMOS MICROPROCESSOR

NMOS MICROPROCESSOR

MSM8085A	RS	8 BIT NMOS MICROPROCESSOR

CMOS MICROCOMPUTERS

MSM5840H	RS	4 BIT CMOS MCU—NO ROM
MSM5840H-XX	RS	4 BIT CMOS MCU—W/ROM
MSM5840H-XX	GS	4 BIT CMOS MCU—W/ROM
MSM5842-XX	RS	4 BIT CMOS MCU—W/ROM
MSM5842-XX	GSK	4 BIT CMOS MCU—W/ROM
MSM58421-XX	GSK	4 BIT CMOS MCU-LCD—W/ROM
MSM58422-XX	GSK	4 BIT CMOS MCU-VF—W/ROM
MSM5845-XX	RS	4 BIT CMOS MCU—W/ROM
MSM80C35	RS	ROMLESS CMOS 80C48
MSM80C39	RS	ROMLESS CMOS 80C49
MSM80C48-XX	RS	CMOS 8048 8 BIT UC
MSM80C48-XX	GSK	CMOS 8048 8 BIT UC
MSM80C49-XX	RS	CMOS 8049 8 BIT UC
MSM80C49-XX	GSK	CMOS 8049 8 BIT UC

MCU/MPU DEVELOPMENT PACKAGES

EASE-40-I		SERIES 40 DEV PKG—ISIS
EASE-40-C		SERIES 40 DEV PKG—CP/M
EASE-49-I		SERIES 80 DEV PKG—ISIS
EASE-49-C		SERIES 80 DEV PKG—CP/M
MPB-202		SERIES 40 DEV BOARD
MPB-203		SERIES 40 DEV BOARD
MPB-421-LCD		SERIES 40 DEV BOARD
MPB-422-VF		SERIES 40 DEV BOARD
MPB-802		SERIES 80 DEV BOARD

PERIPHERAL CIRCUITS

MSM3914A-34	RS	NMOS 16X8 KYBD ENCDR
MSM5204A	RS	8 BIT CMOS A/D CONVT
MSM5204-1	KIT	5204/450 KHZ RESONATOR
MSM5832	RS	CMOS REAL TIME CLOCK
MSM58321	RS	CMOS REAL TIME CLOCK
MSM6203	RS	ARITHMETIC CIRCUIT
MSM80C58	RS	CMOS ARITHMETIC CKT
MSM8155	RS	NMOS 256X8 RAM/I-O TIMR
MSM81C55	RS	CMOS 256X8 RAM/I-O/TIMR
MSM82C12	RS	CMOS 8 BIT I/O PORT
MSM82C43	RS	CMOS 8 BIT I/O PORT EXPDR
MSM82C51A	RS	CMOS USART
MSM82C53-5	RS	CMOS PROG. INTVR TIMER
MSM82C55A-5	RS	CMOS PROG. PERIP INTFCE
MSM8255	RS	256X8 RAM/I-O/TIMER
MSM82C57-5	RS	CMOS DMA CONTROLLER
MSM82C59A-2	RS	CMOS INTERRUPT CONTROLLER
MSM82C84A	RS	CMOS CLOCK GEN DEV
MSM82C88	RS	CMOS BUS CNTL
MSM83C55-XX	RS	CMOS 16K ROM, I/O
MSM83C55-2	RS	CMOS 16K ROM + I/O

PART NUMBER		DESCRIPTION	

DYNAMIC RAM

MSM3732L-15	RS	32KX1	NMOS DRAM
MSM3732H-15	RS	32KX1	NMOS DRAM
MSM3732L-20	RS	32KX1	NMOS DRAM
MSM3732H-20	RS	32KX1	NMOS DRAM
MSM3764-12	RS	64KX1	NMOS DRAM
MSM3764-15	RS	64KX1	NMOS DRAM
MSM3764-20	RS	64KX1	NMOS DRAM
MSM41256	RS	256KX1	NMOS DRAM
MSM37256	AS	256KX1	NMOS DRAM
MSM41257	RS	256KX1	NMOS DRAM

STATIC RAM

MSM5114-2	RS	1KX4	CMOS STATIC RAM
MSM5128-12	RS	2KX8	CMOS STATIC RAM
MSM5128-15	RS	2KX8	CMOS STATIC RAM
MSM5128-15	GSK	2KX8	CMOS STATIC RAM
MSM5128-20	RS	2KX8	CMOS STATIC RAM
MSM5128-20	GSK	2KX8	CMOS STATIC RAM
MSM5165	RS	8KX8	CMOS STATIC RAM

EPROM

MSM2764	AS	8KX8	NMOS EPROM
MSM27C64	AS	8KX8	CMOS EPROM

ROM

MSM38256	RS	32KX8	NMOS MASK ROM
MSM3864	RS	8KX8	NMOS MASK ROM

CMOS VOICE SYNTHESIZERS

MSM5205	RS	SPEECH SYNTHESIZER, ADPCM
MSM5205-2	KIT	5205/ALP-2 FILT/RESONTR
MSM5205-3	KIT	5025/ALP-3 FILT/RESONTR
MSM5205-4	KIT	5205/ALP-4 FILT/RESONTR
MSM5218	RS	SPEECH ANALY/SYNTHESIS, ADPCM
MSM5218-2	KIT	5218/ALP-2 FILT/RESONTR
MSM5218-2-2	KIT	5218/TWO ALP-2 FIL/RES 1
MSM5218-3	KIT	5218/ALP-3 FILT/RESONTR
MSM5218-3-3	KIT	5218/TWO ALP-3 FIL/RES 1
MSM218-4	KIT	5218/ALP-4 FILT/RESONTR
MSM5218-4-4	KIT	5218/TWO ALP-4 FIL/RES 1
MSM5204A	RS	8 BIT CMOS A/D CONVERTER
MSM5248	RS	SPEECH SYNTH, 48K BIT ROM, ADPCM
MSM6202	GSK	SPEECH SYNTH, 144K BIT ROM, ADPCM
MSM6212	RS	SPEECH SYNTH, 288K BIT ROM, ADPCM
MSM6243	GSK	SPEECH SYNTH, 192K BIT ROM, ADPCM
MSM6912	AS	AUDIO FILTER
SAS-1		SPEECH DEV SYSTEM
SAS-2		SPEECH DEV SYSTEM
ALP-2		LOW PASS FILTER 2KHz
ALP-3		LOW PASS FILTER 3KHz
ALP-4		LOW PASS FILTER 4KHz

TELECOMMUNICATIONS

MSA104	RS	LOGARITHMIC AMPLIFIER
MSA105	AS	LOGARITHMIC AMPLIFIER
MSM5249	RS	CMOS PULSE DIALER
MSM6910	AS	CMOS CODEC/FILT COMBO
MSM6912	AS	PCM CHANNEL FILTER
MSM6912	RS	PCM CHANNEL AUDIO FILT
MSM6917	AS	U-255 CODEC CIRCUIT
MSM3953	AS	1200B CCITT MODEM
MSM6926	RS	300B CCITT MODEM
MSM6927	RS	1200B CCITT MODEM
MSM6946	RS	300B BELL MODEM
MSM6947	RS	1200B BELL MODEM

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high-technology products in high-volume supply.

PART NUMBER		DESCRIPTION
DISPLAY DRIVERS & CHARACTER GENERATORS		
MSL912	RS	OCTAL +30V DISP DRVR
MSL915	RS	OCTAL −60V DISP DRVR
MSL915	DICE	OCTAL −60V DISP DRVR
MSL917	RS	OCTAL −60V DISP DRVR
MSL966	RS	LED DIGIT DRIVER
MSM5219	GSK	CMOS 48 BIT LCD DRIVER
MSM5219	DICE	CMOS 48 BIT LCD DRIVER
MSM5238	GSK	32 ROW LCD D/MATRIX DR
MSM5526	RS	RF COUNTER/DISP DRIVER
MSM58282	RS	4D LED DISPLAY DRIVER
MSM58283	RS	4D VF DISPLAY DRIVER
MSM58292	GS	5D LCD DISPLAY DRIVER
MSM58293	GS	5D VF DISPLAY DRIVER
MSM58371	RS	12 BIT S/R W/LED DRV
MSM5838	GS	LCD DOT ROW DRIVER
MSM5839	GS	LCD DOT COL DRIVER
MSM9353	RS	LCD 8 DOT LEVEL METER
MSM9356	GSK	LCD 32 DOT LEVEL METER
MSM9356	DICE	LCD 32 DOT LEVEL METER
MSL9510	RS	8D SCAN VF DISP DRVR
MSL9511	RS	8D SCAN VF DISP DRVR
MSL9650-01	AS	35 DOT CHAR GEN + ROM
MSL9662-01	RS	16 SEG AN CHAR GEN
MSL9663-01	RS	16 SEG AN CHAR GEN
MSL9664-01	RS	14 SEG AN CHAR GEN
MSL9665-01	RS	14 SEG AN CHAR GEN

PART NUMBER		DESCRIPTION
TIMEKEEPING		
MSM5509	RS	6D LED DIGITAL CLOCK
MSM5523	RS	LED CLK, RF CNTR, 4.5 DIG
MSM5524	RS	4½ DIG VF CLOCK
MSM5525	RS	3½ DIG VF RF CNTR
MSM5528	RS	3½ DIG VF CAR CLOCK
MSM5529	RS	4D MUX VF AUTO CLOCK
MSM5550	RS	4D VF ALARM CLK CKT
MSM5557	GSK	MUX LCD ALARM CLOCK
MSM5557	DICE	MUX LCD ALARM CLOCK
MSM5558	RS	VF DIGITAL CLOCK
MSM5803	GSK	LCD ALARM CLOCK
MISCELLANEOUS CIRCUITS		
MSL2312	RS	DIV 10/100 PRESCALER
MSM5232	RS	8 CHANNEL TONE GEN
MSM5814	RS	MOTOR CONTROLLER
MSM5816	RS	MOTOR CONTROL PLL
MSM5819	RS	MOTOR CONTROL PLL
MSL9362	RS	4 CH PROP R/C XMTR
MSL9363	RS	4 CH PROP R/C RCVR

PACKAGING RS: PLASTIC GS: PLASTIC FLAT PACK
AS: CERAMIC GSK: BENT LEAD FLAT PACK

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1333 Lawrence Expressway, Suite 401, Santa Clara, CA 95051

Tel: 408/984-4842
WATS: 800/542-8617
TWX: 910/338-0508
FAX: 408/984-4879
Cable: OKI SNTA

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OKI Semiconductor, Inc.
2102 Business Center Drive, Suite 212
Irvine, California 92715
Tel: 714/752-1843 TWX: 910/595-1747

South Central
OKI Semiconductor, Inc.
16990 Dallas Parkway, Suite 151
Dallas, Texas 75248
Tel: 214/248-8801

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OKI Semiconductor, Inc.
65 Williams Street, Suite 120
Wellesley, Massachusetts 02181
Tel: 617/431-7944 TWX: 710/383-6812

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6100 Green Valley Drive, Suite 160
Bloomington, Minnesota 55438
Tel: 612/835-0837 TWX: 910/576-2998

Southeast
OKI Semiconductor, Inc.
440 Lakeside Drive
Horsham, Pennsylvania 19044
Tel: 215/674-9511 TWX: 510/665-6550

MAJOR ACCOUNTS
OKI Semiconductor, Inc.
205 South Avenue, Suite 100
Poughkeepsie, New York 12601
Tel: 914/473-8044 TLX: 0291516

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OKI
SEMICONDUCTOR

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One Panasonic Way, Secaucus, N.J. 07094 • Tel: (201) 348-5269 • TWX: 710-992-8920

MN4164, N MOS 65K Bit Dynamic Ram

Description

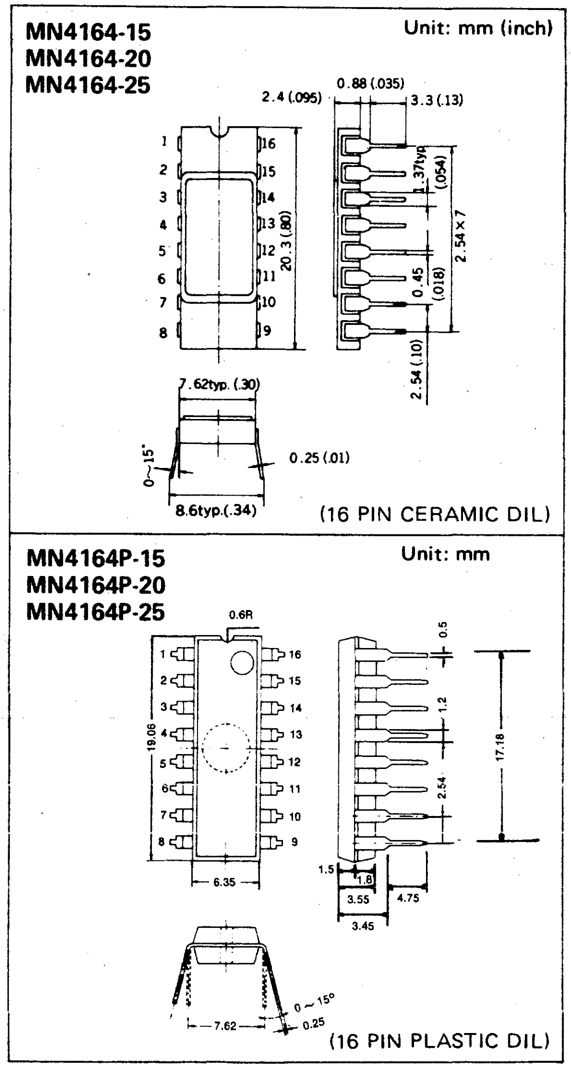
System oriented features include: operation from a single +5V ±10% tolerance power supply, direct TTL interfacing capability, on-chip addresses and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system.

The RAM module also incorporates several flexible operating modes: "Read," "Write," "Read-Modify-Write" cycles, "Page-Mode" operation and "RAS-Only" refresh. Proper control of the clock inputs (RAS, CAS and WRITE) allows common I/O capability, two dimensional chip selection, and extended page boundaries (for operating in page mode).

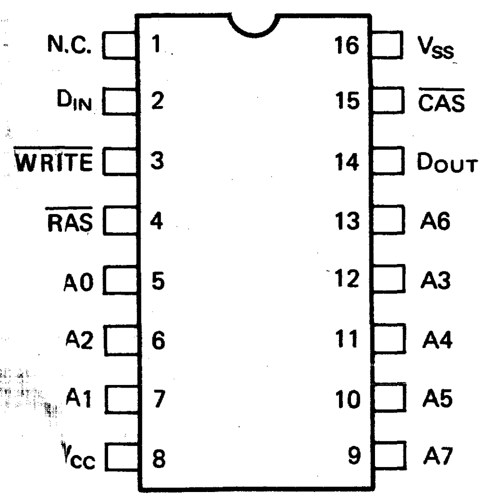
Features

- 65,536 x 1 RAM, 16-pin package
- Row access time:
  150 ns Max. (MN4164-15/MN4164P-15)
  200 ns Max. (MN4164-20/MN4164P-20)
  250 ns Max. (MN4164-25/MN4164P-25)
- Cycle time:
  270 ns Max. (MN4164-15/MN4164P-15)
  330 ns Max. (MN4164-20/MN4164P-20)
  410 ns Max. (MN4164-25/MN4164P-25)
- Low power dissipation:
  275 mW Max. (active)
  27.5 mW Max. (standby)
- Single 5V supply, ±10% tolerance
- 128 refresh cycles/2ms

MN4164 Block Diagram



Pin Assignment (Top View)



Pin Names	Function
$A_0 \sim A_7$	Address Inputs
RAS	Row Address Strobe
CAS	Column Address Strobe
WRITE	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	Power (+5V)
V_{SS}	Ground (0V)

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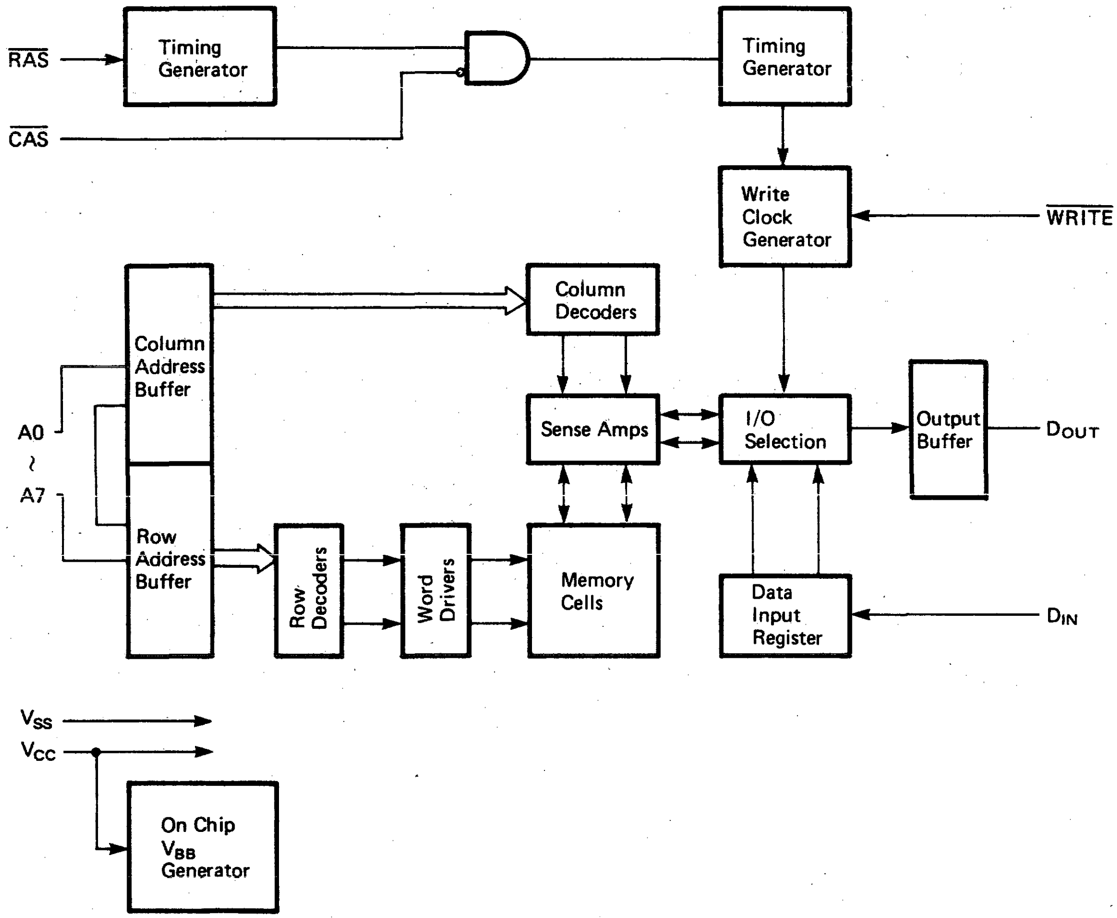

Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Voltage on any Pin relative to V_{SS}	V_{IN}, V_{OUT}	−1.0 to +7.0	V
Voltage on V_{CC} Supply relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Operating Temperature	T_{OP}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Current	I_{OS}	50	mA

Note: Exceeding Absolute Maximum Ratings may cause permanent device damage. Functional operating of the device is not implied outside the operating conditions. Exposure to absolute maximum ratings for extended periods of time may impact device reliability.

Recommended Operating Conditions (Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.2	—	V_{CC} +1.0V	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	—	—	10	pF
Output Capacitance	C_{OUT}	—	—	12	pF

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MN4164, N MOS 65K Bit Dynamic Ram

DC Characteristics (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Operating Current: Average power supply current (RAS, CAS cycling; t_{RC} = min)	I_{CC1}	—	—	50	mA	1)
Standby Current: Power supply current (RAS = CAS = V_{IH})	I_{CC2}	—	—	5	mA	
Refresh Current: Average supply current (RAS cycling, CAS = V_{IH}; t_{RC} = min)	I_{CC3}	—	—	40	mA	1)
Page Mode Current: Average power supply current (RAS = V_{IL}, CAS cycling; t_{PC} = min)	I_{CC4}	—	—	40	mA	1)
Input Leakage Current: Input leakage current, any input ($0V \leqq V_{IN} \leqq 5.5V$, all other pins not under test = 0V)	I_{LI}	−10	0.1	10	μA	
Output Leakage Current: (Data out is disable, $0V \leqq V_{OUT} \leqq 5.5V$)	I_{LO}	−10	0.1	10	μA	
Output Level: Output low voltage (I_{OL} = 4.2 mA)	V_{OL}	—	—	0.4	V	
Output Level: Output high voltage (I_{OH} = −5 mA)	V_{OH}	2.4	—	—	V	

Note: 1) I_{CC1}, I_{CC3}, I_{CC4} depend on cycle rate and output loading. Specifications are for maximum cycle rate and no load. Supply current may be scaled according to the following equation:

$$I(t_{RC}) = \frac{t_{RC}\ min \times I(t_{RC}\ min) + (t_{RC} - t_{RC}\ min) \times I_{CC2}}{t_{RC}}$$

AC Characteristics[1), 2)] (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Unit	MN4164-15 MN4164P-15		MN4164-20 MN4164P-20		MN4164-25 MN4164P-25		Notes
			Min	Max	Min	Max	Min	Max	
Refresh period	t_{REF}	ms	—	2	—	2	—	2	
Random read or write cycle time	t_{RC}	ns	270	—	330	—	410	—	
Read-write cycle time	t_{RWC}	ns	310	—	375	—	515	—	
Page mode cycle time	t_{PC}	ns	170	—	225	—	275	—	
Access time from RAS	t_{RAC}	ns	—	150	—	200	—	250	4), 6), 8)
Access time from CAS	t_{CAC}	ns	—	100	—	135	—	165	5), 6), 8)
Output buffer turn-off delay	t_{OFF}	ns	0	40	0	50	0	60	7)
Transition time	t_T	ns	3	50	3	50	3	50	3)
RAS precharge time	t_{RP}	ns	100	—	120	—	150	—	
RAS pulse width	t_{RAS}	ns	150	10,000	200	10,000	250	10,000	
RAS hold time	t_{RSH}	ns	100	—	135	—	165	—	
CAS precharge time	t_{CP}	ns	50	—	80	—	100	—	
CAS pulse width	t_{CAS}	ns	100	10,000	135	10,000	165	10,000	
CAS hold time	t_{CSH}	ns	150	—	200	—	250	—	
RAS to CAS delay time	t_{RCD}	ns	25	50	25	65	40	85	8)
CAS to RAS precharge time	t_{CRP}	ns	−20	—	−20	—	−20	—	
Row Address set-up time	t_{ASR}	ns	0	—	0	—	0	—	
Row Address hold time	t_{RAH}	ns	20	—	20	—	35	—	
Column Address set-up time	t_{ASC}	ns	−5	—	−5	—	−5	—	
Column Address hold time	t_{CAH}	ns	45	—	55	—	75	—	
Column Address hold time referenced to RAS	t_{AR}	ns	95	—	120	—	160	—	
Read command setup time	t_{RCS}	ns	0	—	0	—	0	—	
Read command hold time	t_{RCH}	ns	0	—	0	—	0	—	
Write command set-up time	t_{WCS}	ns	−20	—	−20	—	−20	—	10)
Write command hold time	t_{WCH}	ns	45	—	55	—	75	—	
Write command hold time referenced to RAS	t_{WCR}	ns	95	—	120	—	160	—	
Write command pulse width	t_{WP}	ns	45	—	55	—	75	—	
Write command to RAS lead time	t_{RWL}	ns	60	—	80	—	100	—	
Write command to CAS lead time	t_{CWL}	ns	60	—	80	—	100	—	
Data-in set-up time	t_{DS}	ns	0	—	0	—	0	—	9)
Data-in hold time	t_{DH}	ns	45	—	55	—	75	—	9)
Data-in hold time referenced to RAS	t_{DHR}	ns	95	—	120	—	160	—	
CAS to WRITE delay	t_{CWD}	ns	80	—	95	—	125	—	10)
RAS to WRITE delay	t_{RWD}	ns	130	—	160	—	200	—	10)
Read command hold time referenced to RAS	t_{RRH}	ns	20	—	25	—	35	—	

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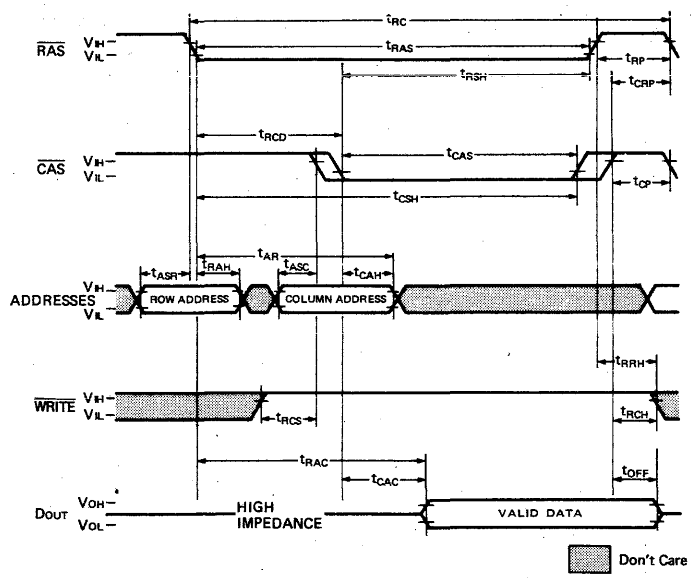
MN4164, N MOS 65K Bit Dynamic Ram

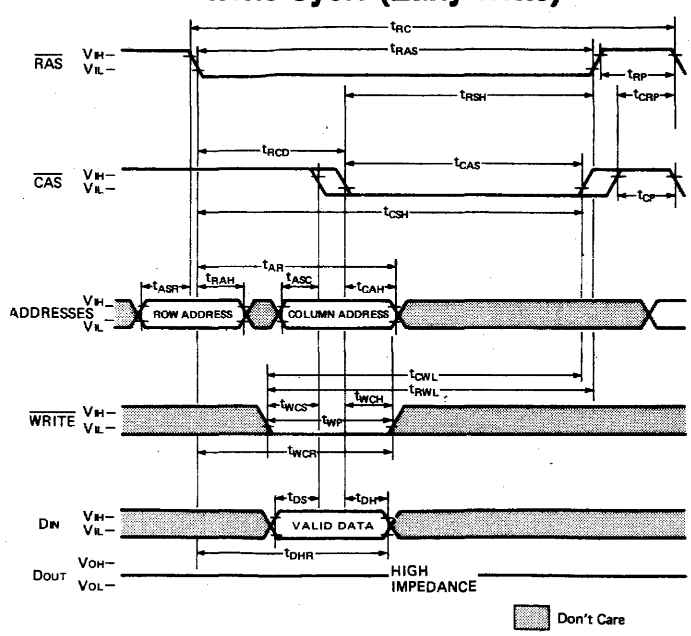
Note:

1) Several cycles are required after power up or prolonged periods of RAS inactivity (2 ms) before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
2) AC measurements assume $t_T = 5.0$ ns.
3) V_{IH} and V_{IL} are reference levels for measuring signal timings and transition times.
4) Assumes that $t_{RCD} \leqq t_{RCD}$ (Max).
5) Assumes that $t_{RCD} \geqq t_{RCD}$ (Max).
6) Measure with load equivalent to 2 TTL loads and 100 pF.
7) t_{OFF} defines the time at which the output enters high impedance state. It is not referenced to levels of V_{IH} and V_{IL}.
8) Operation within the t_{RCD} (Max) limit ensures that t_{RAC} (Max) can be met. t_{RCD} is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} limit, then row access time is $t_{RCD} + t_{CAC}$.
9) These parameters are referenced to leading edge of CAS (Early-Write) or WRITE (Delayed-Write or Read-Modify-Write) whichever occurs last.
10) t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included under AC Characteristics as electrical characteristics only. If $t_{WCS} \leqq t_{WCS}$ (Min), the cycle is an Early-Write cycle and the data out pins will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geqq t_{CWD}$ (Min) and $t_{RWD} \geqq t_{RWD}$ (Min), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

Read Cycle

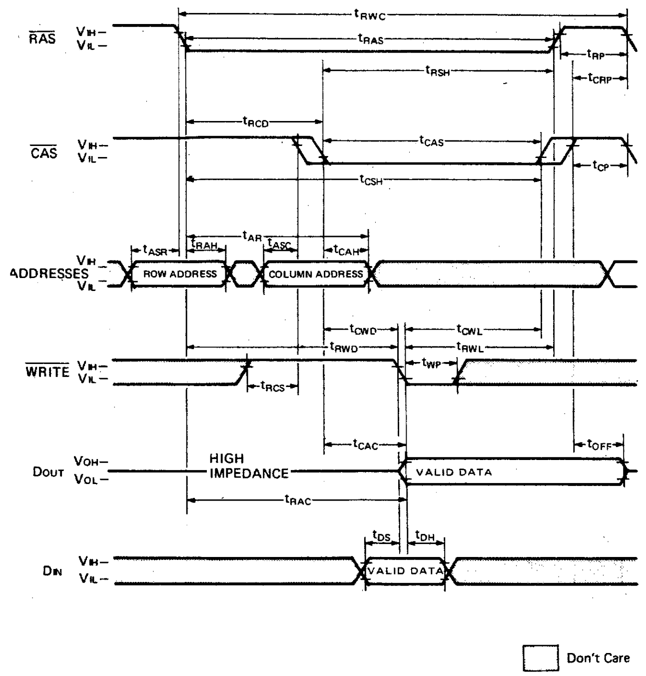


Write Cycle (Early Write)

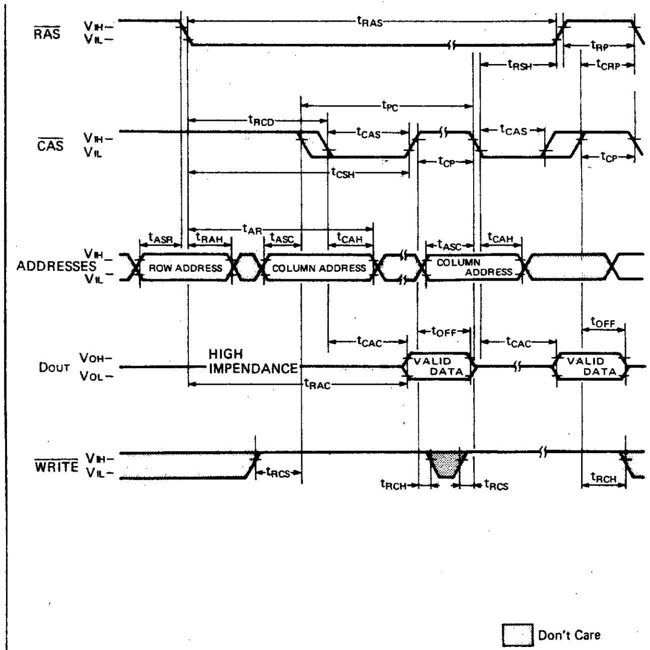


MN4164, N MOS 65K Bit Dynamic Ram

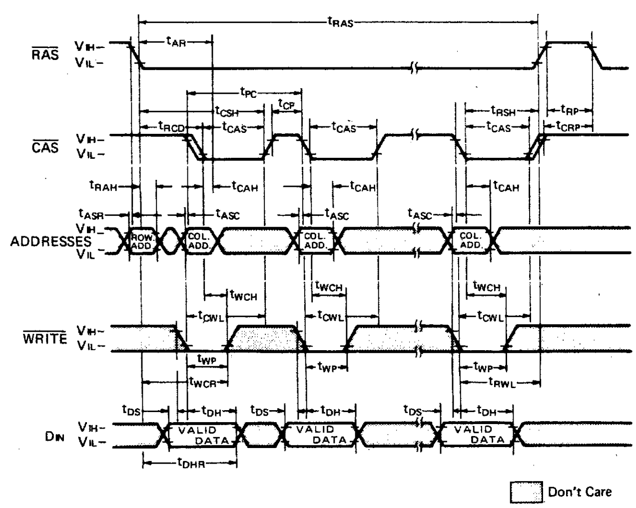
Read-Write/Read-Modify-Write Cycle



Page Mode Read Cycle

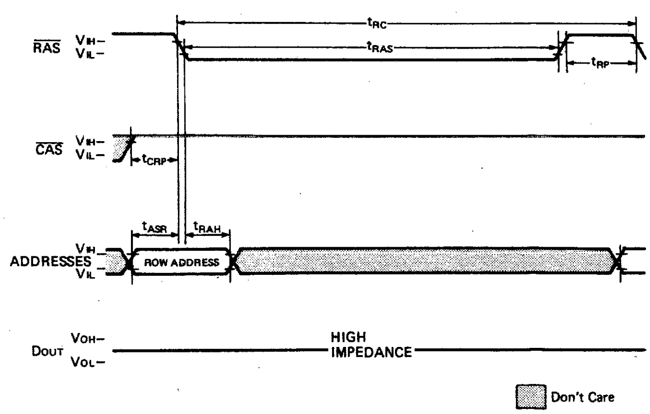


Page Mode Write Cycle



"RAS Only" Refresh Cycle

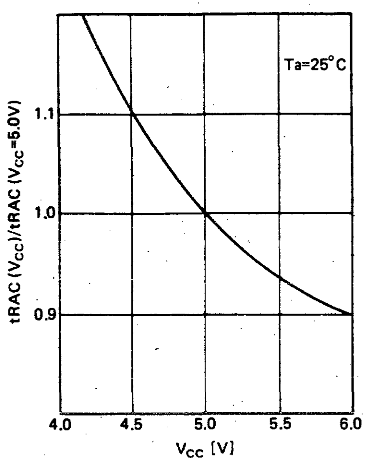
Note: $\overline{WRITE}$ = Don't Care



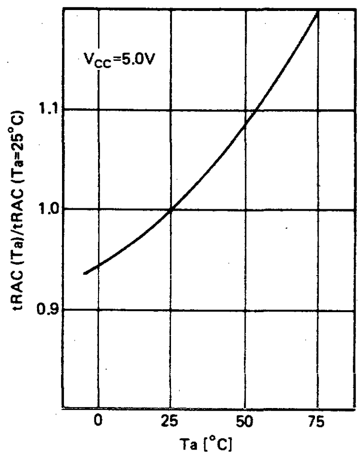
MN4164, N MOS 65K Bit Dynamic Ram

Typical Characteristics Curves

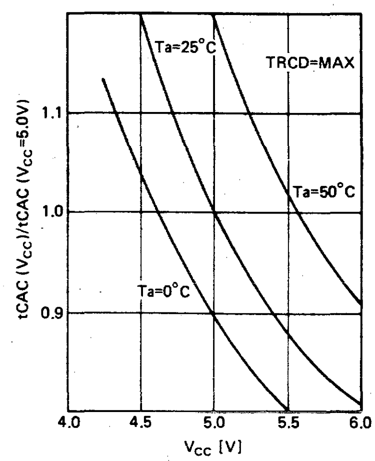
Access time from $\overline{RAS}$ (Relative value) v.s. V_{CC}



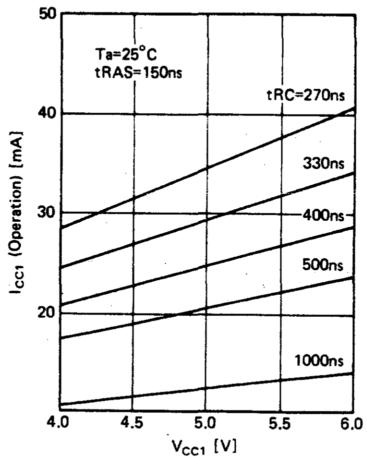
Access time from $\overline{RAS}$ (Relative value) v.s. Ta



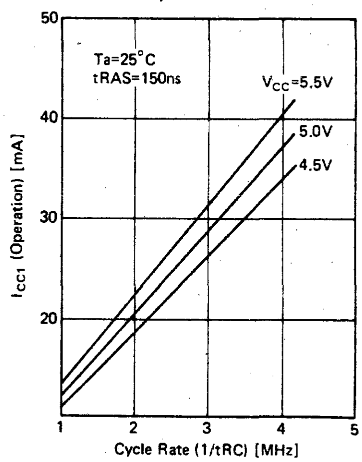
Access time from $\overline{CAS}$ (Relative value) v.s. V_{CC}



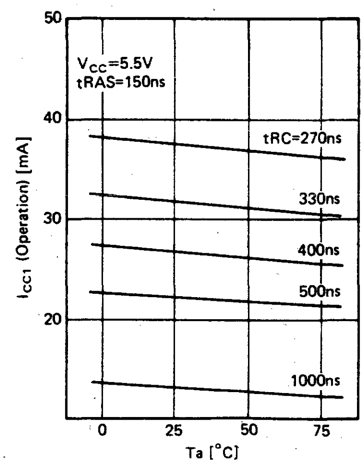
I_{CC1} (tRAS: Constant) v.s. V_{CC}



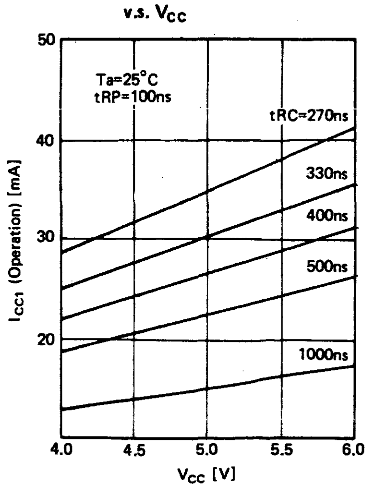
I_{CC1} (tRAS: Constant) v.s. Cycle Rate



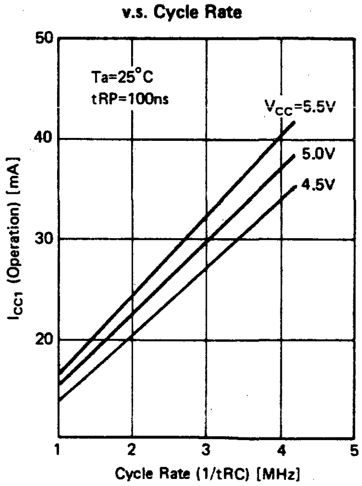
I_{CC1} (tRAS: Constant) v.s. Ta



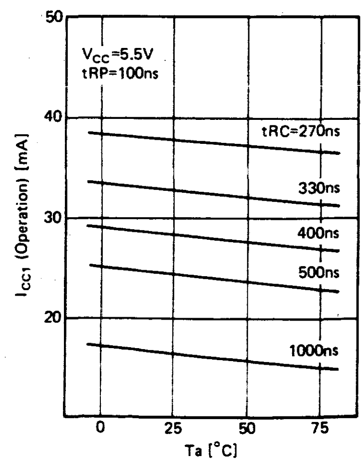
I_{CC1} (tRP: Constant) v.s. V_{CC}



I_{CC1} (tRP: Constant) v.s. Cycle Rate



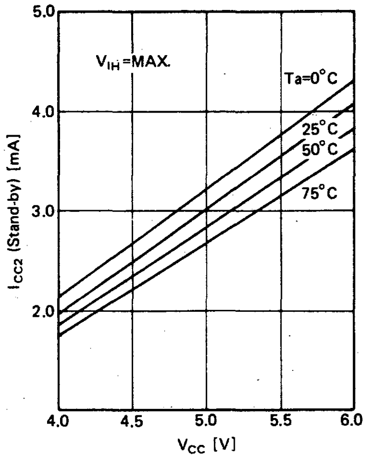
I_{CC1} (tRP: Constant) v.s. Ta



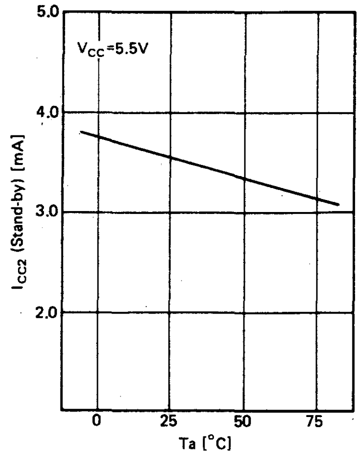
MN4164, N MOS 65K Bit Dynamic Ram

Typical Characteristics Curves (Continued)

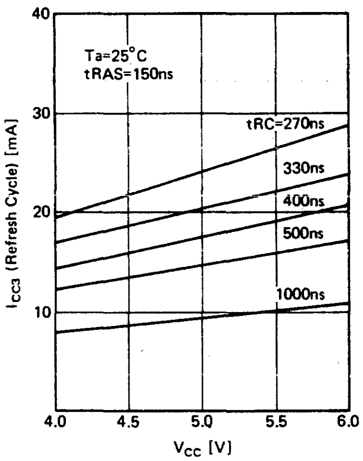
I_{CC2} vs. V_{CC}



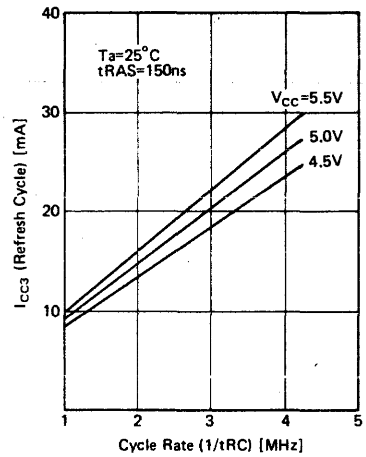
I_{CC2} v.s. Ta



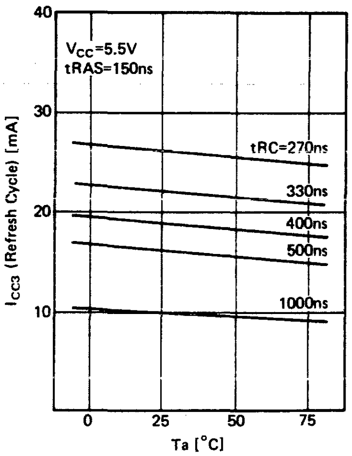
I_{CC3} (tRAS: Constant) v.s. V_{CC}



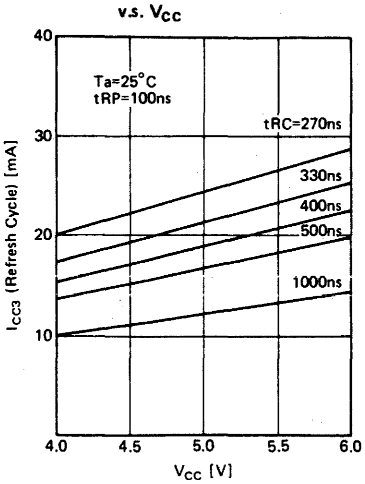
I_{CC3} (tRAS: Constant) v.s. Cycle Rate



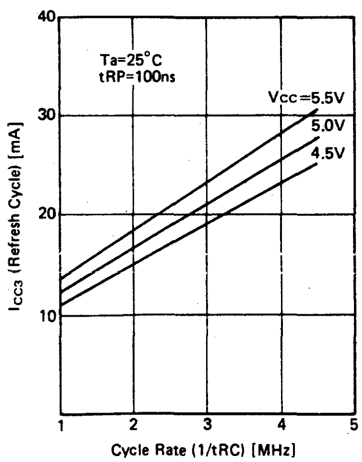
I_{CC3} (tRAS: Constant) v.s. Ta



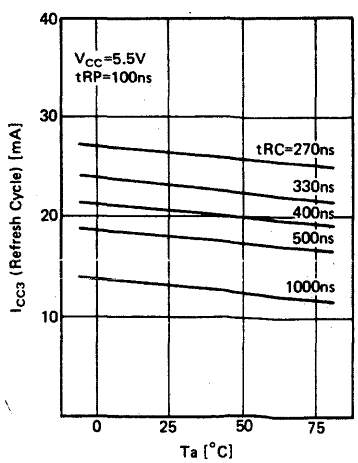
I_{CC3} (tRP: Constant) v.s. V_{CC}



I_{CC3} (tRP: Constant) v.s. Cycle Rate



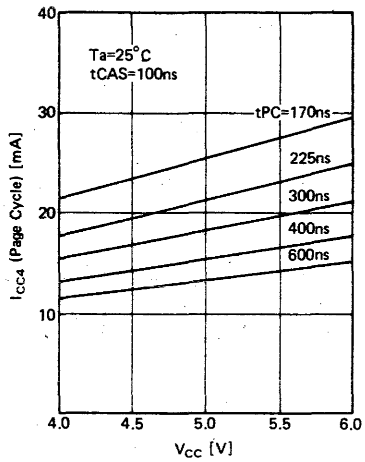
I_{CC3} (tRP: Constant) v.s. Ta



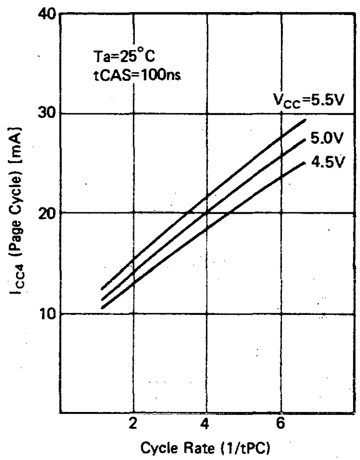
MN4164, N MOS 65K Bit Dynamic Ram

Typical Characteristics Curves (Continued)

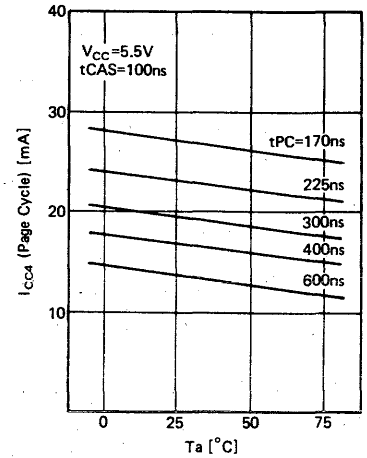
I_{CC4} (tCAS: Constant)
v.s. V_{CC}



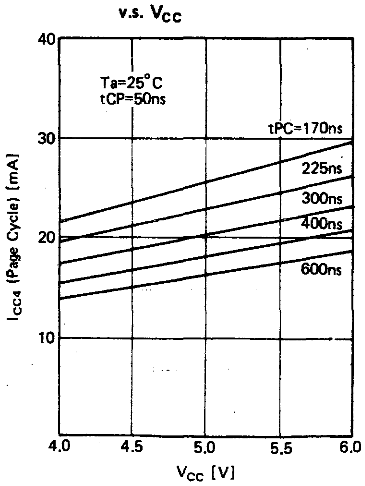
I_{CC4} (tCAS: Constant)
v.s. Cycle Rate



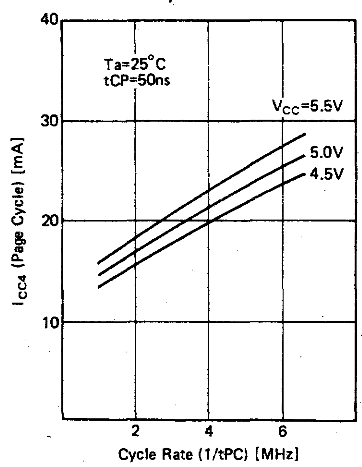
I_{CC4} (tCAS: Constant)
v.s. Ta



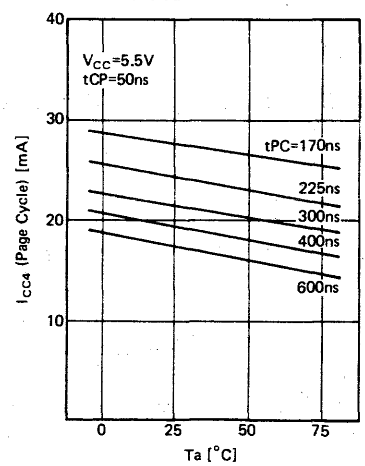
I_{CC4} (tCP: Constant)
v.s. V_{CC}



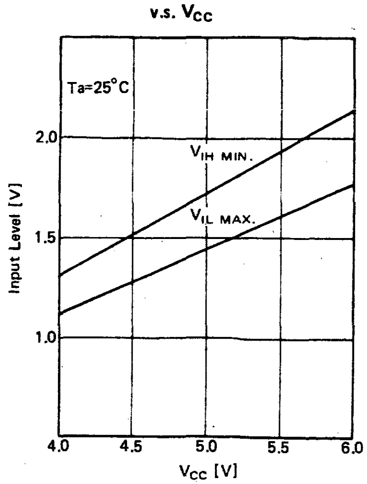
I_{CC4} (tCP: Constant)
v.s. Cycle Rate



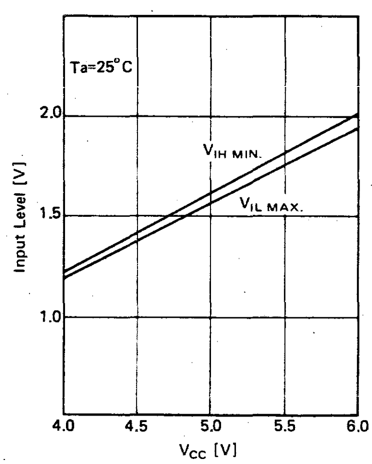
I_{CC4} (tCP: Constant)
v.s. Ta



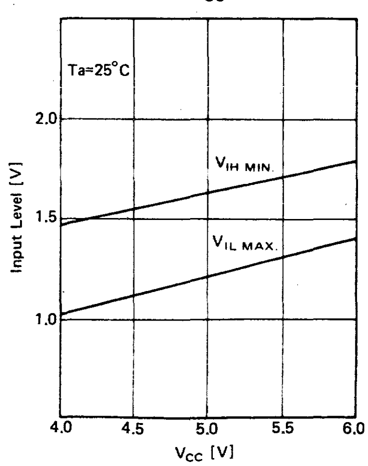
Address Input
v.s. V_{CC}



Data Input
v.s. V_{CC}



Clock Input
v.s. V_{CC}



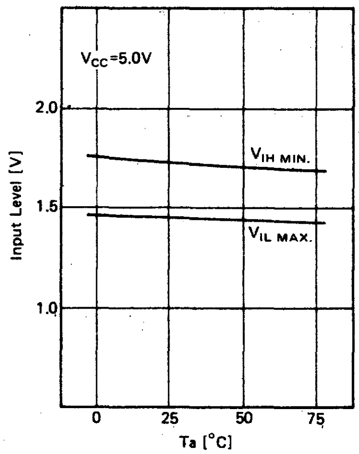
Panasonic

MEMORY

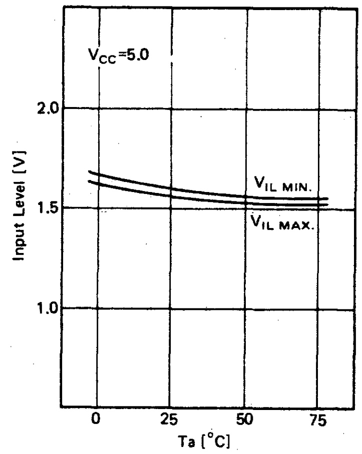
MN4164, N MOS 65K Bit Dynamic Ram

Typical Characteristics Curves (Continued)

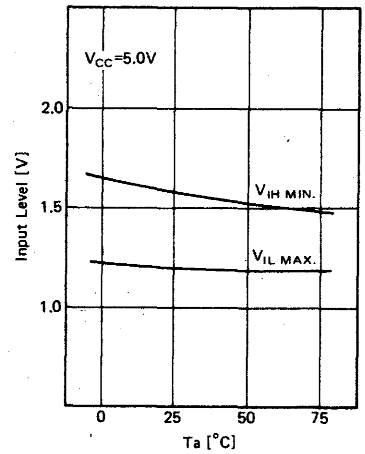
Address Input v.s. Ta



Data Input v.s. Ta



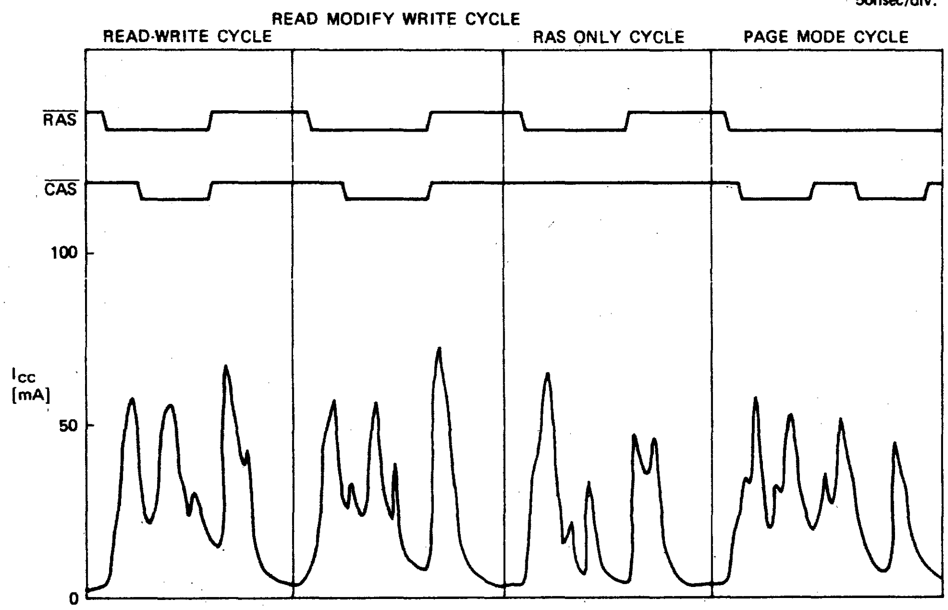
Clock Input v.s. Ta



Typical Supply Current Wave Forms

TYPICAL SUPPLY CURRENT WAVE FORMS

Ta=25°C
50nsec/div.



Panasonic® **PANASONIC INDUSTRIAL COMPANY**
Division of Matsushita Electric Corporation of America / Electronic Components Division
One Panasonic Way, Secaucus, N.J. 07094 • Tel: (201) 348-5269 • TWX: 710-992-8920

MN4164, N MOS 65K Bit Dynamic Ram

Functional Description

Address Input

The 16 address bits required to decode 1 of the 65,536-cell locations within the RAM module are multiplexed onto the 8 address inputs and latched into the on-chip address latches by externally applying two negative going TTL level clocks. The first clock, Row Address Strobe (RAS), latches the 8 row addresses bits into the chip. The second clock, the Column Address Strobe (CAS), subsequently latches the 8 column address bits into the chip. ($A_0 \sim A_7$ are row and column address input.) Each of these signals, RAS and CAS, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the CAS clock sequence are inhibited until the occurrence of a delayed signal derived from the RAS clock chain. This "gated CAS" feature allows the CAS clock to be externally activated as soon as the Row Address Hold Time (t_{RAH}) has been satisfied and the address inputs have been changed from row address to column address information.

Note that CAS can be activated at any time after t_{RAH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing specifications result from the internal gating of CAS; they are t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if CAS is applied to the RAM module at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time from CAS (t_{CAC}) rather than from RAS (t_{RAC}), and access time from RAS will be increased by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

Data Input/Output

Data is retrieved from memory in a read cycle by maintaining WRITE in the inactive or high state throughout the portion of the memory cycle in which CAS is active (low). Data read from the selected cell will be available at the output within the specified access time.

Data to be written into a selected cell is latched into an on chip register by a combination of WRITE and CAS while RAS is active. The later of the signals (WRITE or CAS) to make its negative transition is the strobe for the Data in register. This permits several options in the write cycle timing. In a write cycle, if the WRITE input is brought low (active) prior to CAS, the D_{IN} is strobed by CAS and the set up and hold times are referenced to CAS.

If the input data is not available at CAS time or if it is desired that the cycle be a Read-Modify-Write cycle, the WRITE signal will be delayed until after CAS has made its negative transition. In this delayed write cycle, the data input set up and hold times are referenced to the negative edge of WRITE rather than CAS. (To illustrate this feature, D_{IN} is referenced to WRITE in the timing diagrams depicting the "Read-Modify-Write" cycle while the "WRITE" and "Page-Mode-Write" cycle diagrams show D_{IN} referenced to CAS.)

Data Output

The normal condition of the data output (D_{OUT}) of the RAM module is a high impedance state. That is to say, any time CAS is at a high level, the D_{OUT} pin will be floating. The only time the outputs will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until CAS is taken back to the inactive (high) conditions.

If the memory cycle in progress is "Read" or "Read-Modify-Write" cycle, then the data output will go from the high impedance state to the active condition and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. Once having gone active the output will remain valid until CAS is taken to the precharge state, whether or not RAS goes into precharge.

If the cycle in progress is a "Write" cycle (Write active before CAS goes active), then the output pins will maintain the high impedance throughout the entire cycle.

Note that with this type of output configuration, the user is given full control of the D_{OUT} pin simply by controlling the placement of WRITE command during write operations, and the pulse width of CAS during read operations. Note also that even though data is not latched at the output, data can remain valid from access time until the beginning of a subsequent cycle without paying any penalty in overall memory cycle time (stretching cycle). This type of output operation results in some very significant system implications.

Common I/O

If all write operations are handled in the "Write" cycle mode (WRITE active before CAS goes active), then D_{IN} can be connected directly to D_{OUT} respectively for common I/O data bus.

RAS and CAS Chip Selection

Only those devices which receive both RAS and CAS signals will execute a read or write cycle. Since D_{OUT} is not latched, CAS is not required to turn off the outputs of unselected memory device in a matrix. This means that both CAS and/or RAS can be decoded for chip selection. If a common CAS scheme is used where RAS is decoded for module selection, then total memory power can be conserved. If both RAS and CAS are decoded, then a two dimensional (X, Y) chip select array can be realized.

Page Mode

The "Page-Mode" feature of the RAM allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing row address into the chip and maintaining the RAS signal at a logic 0 throughout all successive memory cycle in which the row address is common. This "Page-Mode" of operation will not dissipate the power associated with the negative going edge of RAS. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

The successive memory operations in "Page-Mode" may be any sequence of read, write, or read-modify-write operations.

The page boundary of a single RAM module is limited to the 256 column locations determined by all combinations of the 8 column address bits. However, in system applications which utilize more than 65,536 data words (more than one 64K memory block), the page boundary can be extended by using CAS rather than RAS as the chip select signal. RAS is applied to all devices to latch the row address into each device and then CAS is decoded and serves as a page cycle select signal. Only those devices which receive both RAS and CAS signals will execute a read or write cycle.

Refresh

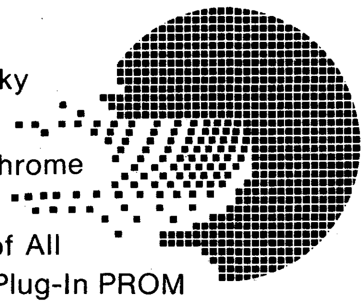
Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses within each 2 ms time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "RAS-Only" cycles. RAS-Only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

RAYTHEON

Field Programmable Read-Only Memories

29000 Series

Features



- Low Power Schottky Technology
- Highly Reliable Nichrome Fuses
- SPROM Versions of All Configurations as Plug-In PROM Replacements
- Typical SPROM "OFF" Power is 25% of Standard Power.
- SPROMs Feature Guaranteed Access Times and Full V_{CC} Tolerance Under Power-Switched Conditions.
- All Devices Use Same Programming Techniques (Generic)
- All Devices Available in both Commercial (0°C to 75°C) and Military (-55°C to +125°C) Versions.
- Packages Available
  - Flat
  - 0.3 Wide DIP
  - 0.6 Wide DIP
  - 28 Pin LCC

Absolute Maximum Ratings

(Above which the useful life may be impaired).

Junction Temperature	-65°C to +175°C
Storage Temperature	-65°C to +150°C
Temperature Under Bias	-55°C to +125°C
Supply Voltage to Ground Potential (Continuous)	-0.5V to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	-0.5V to $+V_{CC}$ Max
DC Input Voltage (Address Inputs)	-0.5V to +5.5V
DC Voltage Applied to Outputs During Programming	26V
Output Current into Outputs During Programming	250mA
DC Input Voltage (Chip Select Input-Pin)	-0.5V to +33V
DC Input Current	-30mA to +5.0mA

Ordering Information

2 9 6 1 1 A D M B

Bipolar PROM Family — 296

Memory Size
1 = 512 x 4 (2K)
2 = 512 x 8 (4K)
3 = 1024 x 8 (8K)
4 = 4096 x 4 (16K)
5 = 2048 x 4 (8K)
7 = 4096 x 8 (32K)
8 = 2048 x 8 (16K)

Product
1 = PROM
3 = SPROM

AC Performance
None = Standard
A = Select

Package Type
D Ceramic Dual-in-Line
F Ceramic Flat pack
L Leadless Chip Carrier
S Ceramic "Slim-DIP"

Temperature Range
M Military -55°C to +125°C
C Commercial 0°C to +75°C

Hi-Rel Screening
B MIL-STD-883, Level B
S MIL-STD-883, Level S

RAYTHEON COMPANY • Semiconductor Division • 350 Ellis Street • Mountain View, CA 94039-7016
(415) 968-9211 • TWX: 910-374-6484

Common Electrical Characteristics Over Operating Range (unless otherwise noted)

Parameter	Description	Test Conditions	Min	Typ[1]	Max	Units
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}	2.4	3.6		V
V_{OL}[3]	Output Low Voltage	V_{CC} = Min I_{OL} = 8.0mA V_{IN} = V_{IH} or V_{IL} I_{OL} = 16mA		0.30 0.35	0.4 0.5	V
V_{IH}	Input High Level	Guaranteed Input Logical High Voltage for All Inputs	2.0		5.5	V
V_{IL}	Input Low Level	Guaranteed Input Logical Low Voltage for All Inputs	0.0		0.8	V
I_{IL}	Input Low Current	V_{CC} = Max, V_{IN} = 0.4V		−10	−250	μA
I_{IH}	Input High Current	V_{CC} = Max, V_{IN} = 2.7V			10	μA
		V_{CC} = Max, V_{IN} = 5.5V			0.1	mA
I_{SC}	Output Short Circuit Current	V_{CC} = Max, V_{OUT} = 0.2V (Note 2)	−12	−35	−85	mA
V_I	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18mA			−1.5	V
I_{CEX}	Output Leakage Current	V_{CC} = Max V_O = 4.5V Chip Disabled V_O = 0.45V			+100 −100	μA

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = +25°C.
2. Not more than one output should be selected at a time. Duration of the short circuit should not be more than one second.
3. This characteristic cannot be tested prior to programming; it is guaranteed by factory testing.

SPROM Characteristics

Part Number	Density	Lead Count	I_{CC} (mA) Disable	I_{CC} (mA) Enable	T_{AA} (nS)[1] Mil	T_{AA} (nS)[1] Com	T_{EA} (nS)[1] Mil	T_{EA} (nS)[1] Com	T_{ER} (nS)[1] Mil	T_{ER} (nS)[1] Com
29633	1024 x 8	24	45	170	90	70	115	75	40	30
29633A	1024 x 8	24	45	170	70	50	70	50	40	30
29653	2048 x 4	18	45	170	90	75	95	80	45	35
29653A	2048 x 4	18	45	170	75	65	80	70	45	35
29673	4096 x 8	24	55	195	105	85	95	125	50	45
29683	2048 x 8	24	50	180	105	85	105	85	50	45
29683A	2048 x8	24	50	180	70	50	80	65	45	35

PROM Characteristics

Part Number	Density	Lead Count	I_{CC} (mA)	T_{AA} (nS)[1] Mil	T_{AA} (nS)[1] Com	T_{EA} (nS)[1] Mil	T_{EA} (nS)[1] Com	T_{ER} (nS)[1] Mil	T_{ER} (nS)[1] Com
29671	4096 x 8	24	195	100	80	50	40	45	40
29671A	4096 x 8	24	195	80		45		35	
29681	2048 x 8	24	180	100	80	50	40	45	40
29681A	2048 x 8	24	180	70	50	45	35	35	30

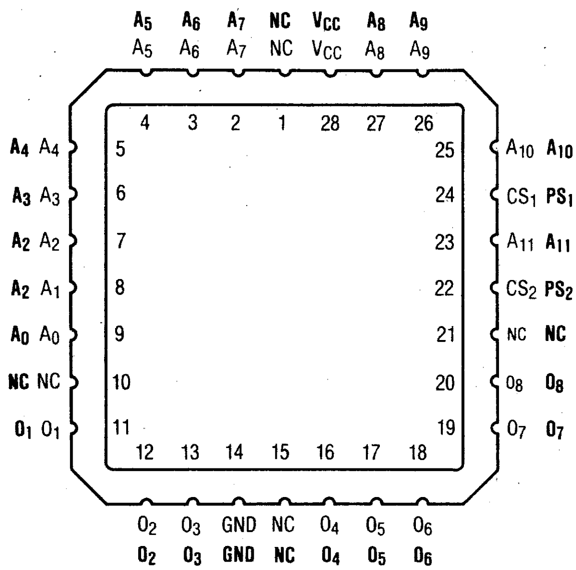
Note: Test Conditions — C_L = 30pF, R_L = 300Ω to V_{CC} and 600Ω to GND (16mA Load). 300Ω resistor opened for t_{EA} and t_{ER} measurements between HIGH and OFF states.

RAYTHEON

Pin Out Information

29671/A
29673/A

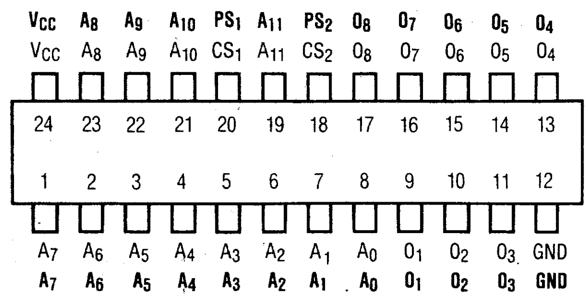
Leadless Chip Carrier (28 Pin)



Pin 24 is also the programming pin (pp).

29671/A
29673/A

Dual-in-Line and Flat Packages

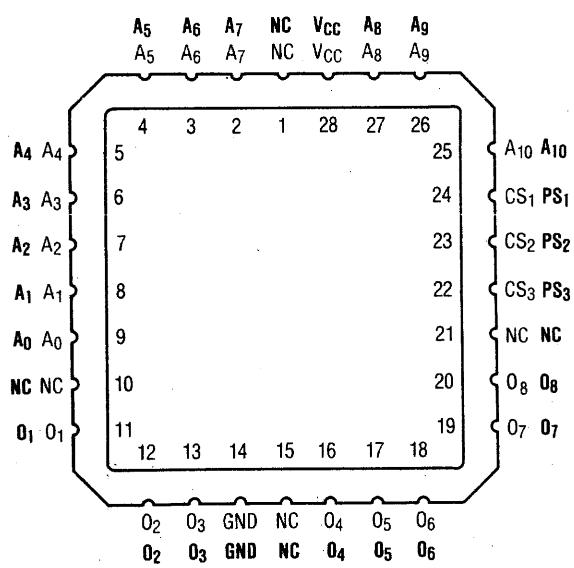


Pin 20 is also the programming pin (pp).

65-01624A

29681/A
29683/A

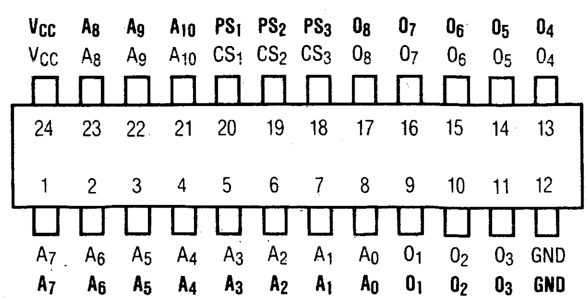
Leadless Chip Carrier (28 Pin)



Pin 24 is also the programming pin (pp).

29681/A
29683/A

Dual-in-Line and Flat Packages



Pin 20 is also the programming pin (pp).

65-01625A

Raytheon

MEMORY

RAYTHEON

seeq

52B13/52B23/52B33
52B13H/52B23H/52B33H
Electrically Erasable ROM

PRELIMINARY DATA SHEET

March 1983

Features

- **Input Latches**
- **Single 5V Supply**
- **Specified over V_{CC} ±10% Range**
- **TTL Byte Erase/Byte Write/Chip Clear**
- **1 ms or 10 ms Byte Erase/Byte Write**
- **10,000 Erase/Write Cycles per Byte**
- **Silicon Signature™ and DiTrace™**
- **Fast Read Access Time — 250 ns**
- **JEDEC Approved Byte Wide Memory Pinout**

Description

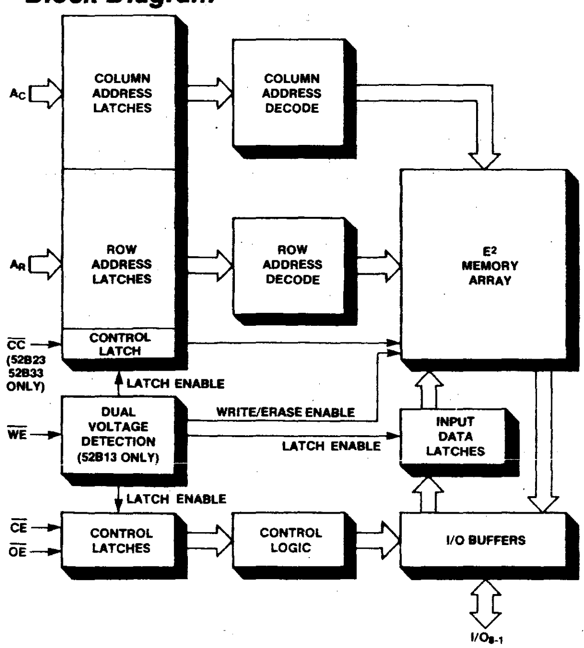
SEEQ's family of 5 volt, electrically erasable read only memories, E²ROMs, include three densities. The 52B13 and 52B13H are 2048 x 8 bit, the 52B23 and 52B23H are 4096 x 8 bit, and the 52B33 and 52B33H are 8192 x 8 bit E²ROM. Each device operates on 5 volt TTL levels in the read, write and erase modes. In addition, high voltage (14-22 volts) may be used with the 52B13 for erase and write. All devices have a chip clear mode in which the entire memory is erased in a single erase cycle. The 52B13 performs chip clear with a high voltage signal while the other devices in the family require only a TTL level signal on $\overline{OE}$. The erasure time for both chip clear and byte erase is under 10 ms for all device types. Where faster erase/write times are required, the "H" product may be used to achieve erase or write in under 1 ms.

Data, addresses, $\overline{CE}$, $\overline{CC}$ and $\overline{OE}$ are latched on the leading edge of $\overline{WE}$. The system controller needs only to maintain the $\overline{WE}$ signal during the erase/write cycle after the latches are activated. Once written, which requires under 10 ms, there is no limit to the number of times that the data may be read. Each byte may be erased and written at least 10,000 times.

This family of E²ROMs include Silicon Signature™ and DiTrace™, SEEQ's on-chip traceability feature. This feature provides the ability to trace the history of any packaged device back to the wafer level. Silicon Signature™ contains device revisions and programming information. The process lot numbers and data is written into DiTrace™.

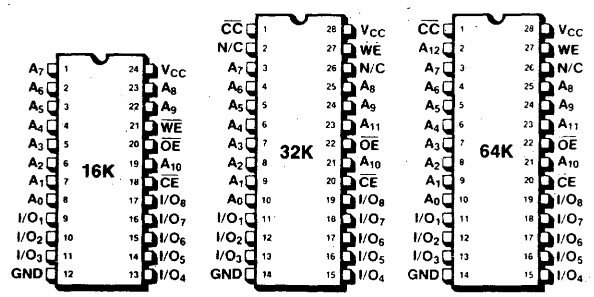
The members of SEEQ's family of latched E²ROMs are each available in the military (-55°C to +125°C) and the extended (-40°C to +85°C) temperature ranges.

Block Diagram



Pin Configurations

52B13/52B13H　52B23/52B23H　52B33/52B33H



Pin Names

Ac	ADDRESSES — COLUMN (LOWER ORDER BITS)
AR	ADDRESSES — ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O	DATA INPUT (WRITE OR ERASE), DATA OUTPUT (READ)
$\overline{CC}$	CHIP CLEAR
N/C	NO CONNECT

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Absolute Maximum Stress Ratings*

Temperature
Storage .... -65° C to + 100° C
Under Bias .... -10° C to +80° C
All Inputs or Outputs with
Respect to Ground .... +6V to -0.3V
52B13 Only
$\overline{WE}$ During Writing/Erasing
with Respect to Ground ...... +22.5V to -0.3V
Duration of $\overline{WE}$ Supply at
22V During W/E Inhibit .... 24 Hours

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions (All Operating Modes — Reference Table 1)

	52BXX-3	52BXX-200/-250/-350
V_{CC} Supply Voltage	5V ± 5%	5V ± 10%
Temperature Range	0 to 70° C	0 to 70° C

D.C. Operating Characteristics During Read or Write/Erase

(Over the Operating V_{CC} and Temperature Range)

Symbol	Parameter	Min.	Nom.[1]	Max.	Unit	Test Conditions
I_{IN}	Input Leakage Current			10	μA	$V_{IN} = V_{CC}$ Max.
I_O	Output Leakage Current			10	μA	$V_{OUT} = V_{CC}$ Max.
I_{WE}	Write Enable Leakage Read Mode			10	μA	$\overline{WE} = V_{IH}$
	TTL W/E Mode			10	μA	$\overline{WE} = V_{IL}$
	High Voltage W/E Mode[2]			1.5	mA	$\overline{WE}$ = 22V, $\overline{CE} = V_{IL}$
	High Voltage W/E Inhibit Mode[2]			1.5	mA	$\overline{WE}$ = 22V, $\overline{CE} = V_{IH}$
	Chip Erase — TTL Mode			10	μA	$\overline{WE} = V_{IL}$
	Chip Erase — High Voltage Mode[2]			1.5	mA	$\overline{WE}$ = 22V
I_{CC1}	V_{CC} Standby Current 52B13/H		15	30	mA	$\overline{CE} = V_{IH}$
	52B23/H, 52B33/H		18	40	mA	
I_{CC2}	V_{CC} Active Current 52B13/H		50	80	mA	$\overline{CE} = \overline{OE} = V_{IL}$
	52B23/H, 52B33/H		60	110	mA	
V_{IL} (D.C.)	Input Low Voltage (D.C.)	-0.1		0.8	V	
V_{IL} (A.C.)	Input Low Voltage (A.C.)	-0.4			V	Time = 10 ns
V_{IH}	Input High Voltage	2		V_{CC} + 1	V	
V_{WE}	$\overline{WE}$ Read Voltage	2		V_{CC} + 1	V	
	$\overline{WE}$ Write/Erase Voltage TTL Mode	-0.1		0.8	V	
	High Voltage Mode[2]	14		22	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400 μA
V_{OE}	$\overline{OE}$ Chip Erase Voltage	14		22	V	I_{OE} = 10 μA

Notes:
1. Nominal values are for T_A = 25° C and V_{CC} = 5.0V.
2. Applies to 52B13 only.

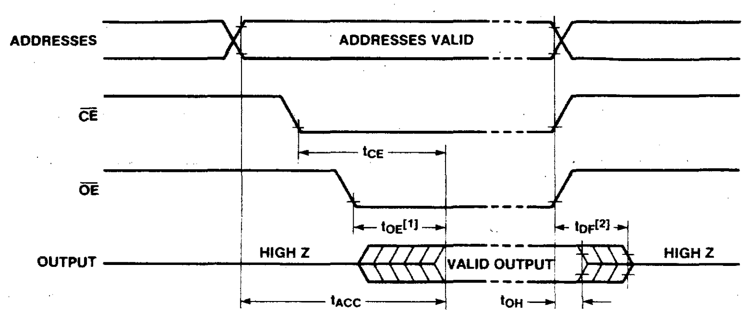
A.C. Operating Characteristics During Read (Over Operating V_{CC} and Temperature Range)

Symbol	Parameter	Device Number Extension	52BXX/52BXXH Min.	Nom.	Max.	Units	Conditions
t_{ACC}	Address to Data Valid	-200			200	ns	$\overline{CE} = \overline{OE} = V_{IL}$
		-250			250	ns	
		-350/-3			350	ns	
t_{CE}	Chip Enable to Data Valid	-200			200	ns	$\overline{OE} = V_{IL}$
		-250			250	ns	
		-350/-3			350	ns	
t_{OE}[1]	Output Enable to Data Valid	-200	10		80	ns	$\overline{CE} = V_{IL}$
		-250	10		90	ns	
		-350/-3	10		100	ns	
t_{DF}[2]	Output Enable to High Impedance	-200	0		60	ns	$\overline{CE} = V_{IL}$
		-250	0		70	ns	
		-350/-3	0		80	ns	
t_{OH}	Output Hold				0	ns	$\overline{CE} = \overline{OE} = V_{IL}$
C_{IN}/ C_{OUT}[3]	Input/Output Capacitance				10	pF	$V_{IN}=0/V_{OUT}=0$, $T_A = 25°C$

A.C. Operating Characteristics During Write/Erase (Over Operating V_{CC} and Temperature Range)

Symbol	Parameter		Min.	Max.	Units
Q[4]	Maximum Endurance		10,000		Cycles/Byte
t_S	$\overline{CC}$, $\overline{CE}$, $\overline{OE}$ or A_N Setup to $\overline{WE}$		50		ns
t_{DS}	Data Setup to $\overline{WE}$		0		ns
t_H[5]	$\overline{WE}$ to $\overline{CE}$, $\overline{OE}$, $\overline{CC}$, A_N or Data Change		50		ns
t_{WP}	Write Enable, $\overline{WE}$, Pulse Width	Chip Clear — All Devices	9		ms
		Byte Modes — 52BXX	9		ms
		Byte Modes — 52BXXH	1		ms
t_{WR}[6]	$\overline{WE}$ to Mode Change		50		ns

READ TIMING



Notes:
1. $\overline{OE}$ may be delayed up to t_{ACC} — t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
3. This parameter is periodically sampled.
4. Maximum endurance, Q, is the number of write and erase cycles/byte.
5. After t_H, hold time, from $\overline{WE}$, the inputs $\overline{CE}$, $\overline{OE}$, $\overline{CC}$, Address and Data are latched and are "Don't Cares" until t_{WR}, Write Recovery Time, after the trailing edge of $\overline{WE}$.
6. The Write Recovery Time, t_{WR}, is the time after the trailing edge of $\overline{WE}$ that the latches are open and able to accept the next mode set-up conditions. Reference Table 1 (page 2) for mode control conditions.

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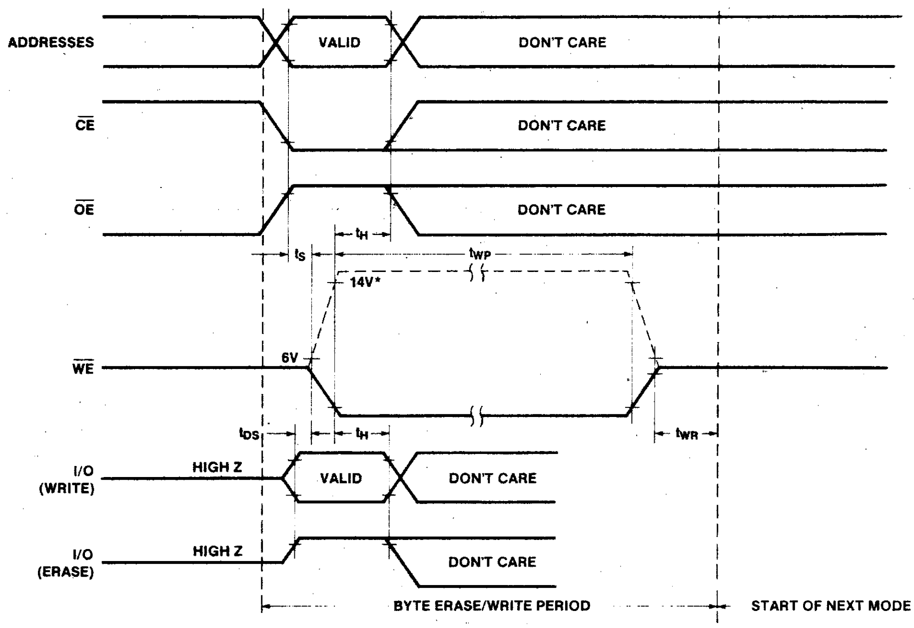
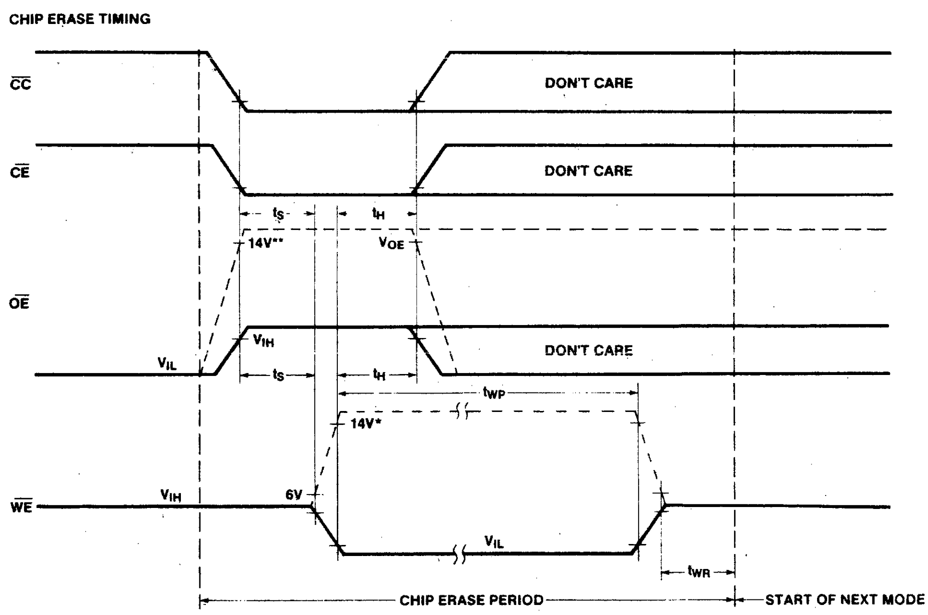
SEEQ Technology

MEMORY

BYTE ERASE OR BYTE WRITE TIMING



CHIP ERASE TIMING



ADDRESS AND I/O PINS ARE "DON'T CARE".

*IN THE BYTE ERASE/WRITE OR CHIP ERASE MODE, $\overline{WE}$ FOR THE 52B13 MAY BE EITHER A HIGH OR TTL VOLTAGE. $\overline{WE}$ FOR THE 52XXH IS TTL ONLY.

**IN THE CHIP ERASE MODE, $\overline{OE}$ IS A HIGH VOLTAGE FOR THE 52B13/52B13H ONLY.

seeq

5133/5143
64K/128K UV EPROM

PRODUCT DESCRIPTION

September 1983

Features

- **200 ns Access Times at 0 to 70° C**
- **Programmed Using Intelligent Algorithm**
  - **— Typically 5 ms/byte Programming Time**
  - **— 2 Minutes for 5143 (27128)**
  - **— 1 Minute for 5133 (2764)**
- **JEDEC Approved Bytewide Pin Configuration**
  - **— 5133 8K x 8 Organization**
  - **— 5143 16K x 8 Organization**
- **Low Power Dissipation**
  - **— 100 mA Active Current**
  - **— 30 mA Standby Current**
- **Extended Temperature Range Available**
- **Silicon Signature™**

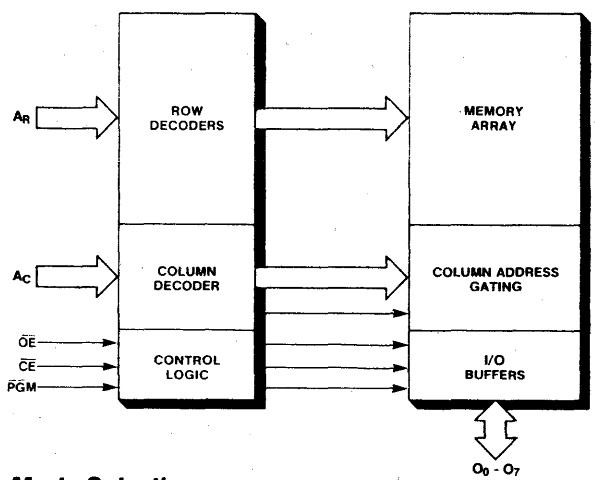
Description

SEEQ's 5133 and 5143 are ultraviolet light erasable EPROMs which are organized 8K x 8 and 16K x 8 respectively. They are pin for pin compatible to 64K and 128K EPROMs, such as the 2764 and 27128 respectively, in all operational/programming modes. Both devices have access times as fast as 200 ns over the 0 to 70° C temperature and V_{CC} tolerance range. The access time is achieved without sacrificing power since the maximum active and standby currents are 100 mA and 30 mA respectively. The 200 ns allows higher system efficiency by eliminating the need for wait states in today's 8- or 16-bit microcomputers.

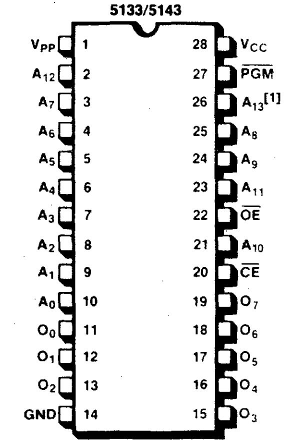
Initially, and after erasure, all bits are in the "1" state. Data is programmed by applying 21 V to V_{PP} and a TTL "0" to pin 27 (program pin). The 5133 and 5143 may be programmed with an intelligent algorithm

(continued on page 2)

Block Diagram



Pin Configuration



NOTE 1: PIN 26 IS A NO CONNECT ON THE 5133.

Mode Selection

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	High Z
Silicon Signature™	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}

For Silicon Signature™: A_0–A_3 are toggled. A_4 = V_{IL}. A_9 = 12V. all other addresses are at any TTL level.

Pin Names

A_C	ADDRESSES — COLUMN (LSB)
A_R	ADDRESSES — ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0 - O_7	OUTPUTS
$\overline{PGM}$	PROGRAM

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that is now available on commercial programmers. The programming time is typically 5 ms/byte or 2 minutes for all 16K bytes of the 5143. The 5133 requires only half of this time, about a minute for 8K bytes. This faster time improves manufacturing throughput time by hours over conventional 50 ms algorithms. Commercial programmers (e.g. Data I/O, Pro-log, Digelec, Kontron, and Stag) have implemented this fast algorithm for SEEQ's EPROMs. If desired, the 5143 and the 5133 may be programmed using the conventional 50 ms programming specification of older generation EPROMs.

Incorporated on the 5143 and 5133 is Silicon Signature™. Silicon Signature contains encoded data which identifies SEEQ as the EPROM manufacturer, the product's fab location, and programming information. This data is encoded in ROM to prevent erasure by ultraviolet light.

Absolute Maximum Stress Ratings

Temperature
- Storage .... -65° C to +150° C
- Under Bias .... -10° C to +80° C

All Inputs or Outputs with
- Respect to Ground .... +7V to -0.6V

V_{PP} During Programming with
- Respect to Ground .... +22V to -0.6V

Voltage on A_9 with
- Respect to Ground .... +15.5V to -0.6V

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions (51XX = 5133 and 5143)

	51XX-200, 51XX-250 51XX-300, 51XX-450	51XX-2, 51XX-3, 51XX-4
V_{CC} Supply Voltage(1)	5 V ± 10%	5 V ± 5%
Temperature Range (Read Mode)	0 to 70° C	0 to 70° C
V_{PP} During Programming	21 ± 0.5 V	21 ± 0.5 V

DC Operating Characteristics During Read or Programming

Symbol	Parameter		Limits Min.	Limits Max.	Unit	Test Conditions
I_{IN}	Input Leakage Current			10	μA	$V_{IN} = V_{CC}$ Max.
I_O	Output Leakage Current			10	μA	$V_{OUT} = V_{CC}$ Max.
I_{PP} 2	V_{PP} Current	Read Mode		5	mA	$V_{PP} = V_{CC}$ Max.
		Prog. Mode		30	mA	$V_{PP} = 21.5V$
I_{CC1} 2	V_{CC} Standby Current			30	mA	$\overline{CE} = V_{IH}$
I_{CC2} 2	V_{CC} Active Current			100	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V_{IL}	Input Low Voltage		-0.1	0.8	V	
V_{IH}	Input High Voltage		2	$V_{CC} + 1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage		2.4		V	$I_{OH} = -400$ μA

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

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MEMORY

AC Operating Characteristics During Read

Symbol	Parameter	Limits (nsec)								Test Conditions
		51XX-2 51XX-200		51XX-250		51XX-3 51XX-300		51XX-4 51XX-450		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
T_{ACC}	Address to Data Valid		200		250		300		450	$\overline{CE} = \overline{OE} = V_{IL}$
T_{CE}	Chip Enable to Data Valid		200		250		300		450	$\overline{OE} = V_{IL}$
T_{OE}	Output Enable to Data Valid		75		100		120		150	$\overline{CE} = V_{IL}$
T_{DF}	Output Enable to Output Float	0	60	0	60	0	105	0	130	$\overline{CE} = V_{IL}$
T_{OH}	Output Hold from Chip Enable, Addresses, or Output Enable whichever occurred first	0		0		0		0		$\overline{CE} = \overline{OE} = V_{IL}$

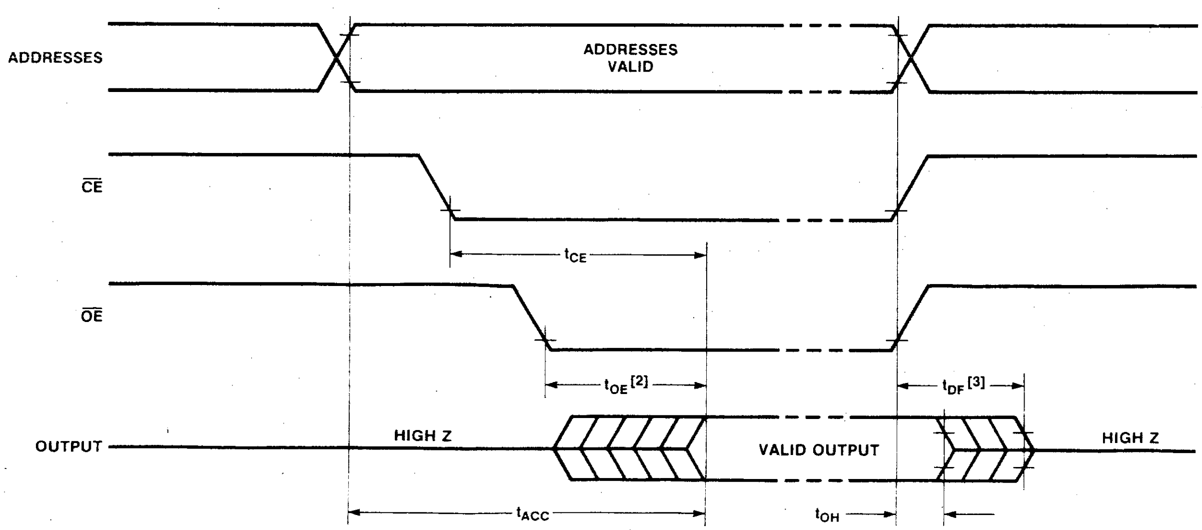
Capacitance[1]

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

A.C. Test Conditions

Output Load: 1 TTL gate and $C_L = 100$ pF
Input Rise and Fall Times: ≤ 20ns
Input Pulse Levels: 0.45V to 2.4V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A.C. Waveforms



NOTES:
1. THIS PARAMETER IS SAMPLED AND IS NOT 100% TESTED.
2. $\overline{OE}$ MAY BE DELAYED UP TO $t_{ACC} - t_{OE}$ AFTER THE FALLING EDGE OF $\overline{CE}$ WITHOUT IMPACT ON t_{ACC}.
3. t_{DF} IS SPECIFIED FROM $\overline{OE}$ OR $\overline{CE}$, WHICHEVER OCCURS FIRST.

Signetics

BIPOLAR MEMORY Products

Integrated Fuse Logic (IFL)

20 Pin: 82S151
82S153/82S153A(T.S.)
82S159(T.S.)

24 Pin: 82S167(T.S.)

28 Pin: 82S100(T.S.)/82S101(O.C.)
82S102(O.C.)/82S103(T.S.)
82S105A(T.S.)

RAMs

256-BIT: 82LS16(T.S)/82LS17(O.C.)

2034-BIT: 82S212A(T.S.)

PROMs

256-BIT: 82S23A(O.C.)/82S123A(T.S.)

1024-BIT: 82S126A(O.C.)/82S129A(T.S.)

2048-BIT: 82S130A(O.C.)/82S131A(T.S.)
82LS135(T.S.)

4096-BIT: 82S137A/82S137B(T.S.)
82S147A(T.S.)

8192-BIT: 82S181A/82S181B(T.S.)
82S185A/82S185B(T.S.)

16,384-BIT: 82S191A(T.S.)
82HS195(T.S.)

32,768-BIT: 82HS321(T.S.)

signetics
a subsidiary of U.S. Philips Corporation
Signetics Corporation
811 E. Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088-3409
Telephone 408/739-7700

SELECTION GUIDE

Device	Org	Output CKT 1	Output Logic 2	Access Time 3	Temp 4	Pkg 5	Pins	Max Icc
FPLAs								
82S100	16x48x8	TS	—	50	M,C	F,N	28	170
82S101	16x48x8	OC	—	50	M,C	F,N	28	170
82S152	18x32x10	OC	I/O	40	M,C	F,N	20	155
82S152A*	18x32x10	OC	I/O	30	M,C	F,N	20	155
82S153	18x32x10	TS	I/O	40	M,C	F,N	20	155
82S153A*	18x32x10	TS	I/O	30	M,C	F,N	20	155
82S161*	12x48x8	TS	—	50	M,C	F,N	24	170
82S173*	20x24x11	TS	I/O	25	M,C	F,N	24	170
FPGAs								
82S151*	18x12	TS	I/O	20	M,C	F,N	20	155
82S103	16x9	TS	—	35	M,C	F,N	28	170
FPLSs								
82S105	16x48x8	TS	R	60	M,C	F,N	28	180
82S105A	16x48x8	TS	R	50	M,C	F,N	28	180
82S155*	16x32x12	TS	I/O,R	65	M,C	F,N	20	155
82S157*	16x32x12	TS	I/O,R	65	M,C	F,N	20	155
82S159	16x32x12	TS	I/O,R	65	M,C	F,N	20	155
82S167	14x48x6	TS	R	65	C	F3,N3	24	160
PROMs								
82S23	32x8	OC	—	50	M,C	F,N	16	77
82S23A*	32x8	OC	—	25	M,C	F,N	16	100
82S123	32x8	TS	—	50	M,C	F,N	16	77
82S123A*	32x8	TS	—	25	M,C	F,N	16	100
82S126	256x4	OC	—	50	M,C	F,N	16	120
82S126A*	256x4	OC	—	35	M,C	F,N	16	120
82S129	256x4	TS	—	50	M,C	F,N	16	120
82S129A*	256x4	TS	—	35	M,C	F,N	16	120
10149	256x4	OE	—	20	C	F	16	150
100149	256x4	OE	—	20	C	F	16	150
82S130	512x4	OC	—	50	M,C	F,N	16	140
82S130A*	512x4	OC	—	35	M,C	F,N	16	140
82S131	512x4	TS	—	50	M,C	F,N	16	140
82S131A*	512x4	TS	—	35	M,C	F,N	16	140
82LS135	256x8	TS	—	100	M,C	F,N	20	100
82S135*	256x8	TS	—	45	M,C	F,N	20	155
82S115	512x8	TS	L	60	M,C	F,N	24	175
82S141	512x8	TS	—	60	M,C	F,N	24	175
82S137	1024x4	TS	—	60	M,C	F,N	18	140
82S137A	1024x4	TS	—	45	M,C	F,N	18	140
82S137B	1024x4	TS	—	35	C	F,N	18	140
82S147	512x8	TS	—	60	M,C	F,N	20	155
82S147A	512x8	TS	—	45	M,C	F,N	20	155
82LS181	1024x8	TS	—	150	M,C	F,N	24	80
82S180	1024x8	OC	—	70	M,C	F,N	24	175
82S181	1024x8	TS	—	70	M,C	F,N	24	175
82S181A	1024x8	TS	—	50	M,C	F,N	24	175
82S181B	1024x8	TS	—	45	C	F,N	24	175
82S183	1024x8	TS	L	60	M,C	F,N	24	175
82S2708	1024x8	TS	—	90	M	F,R,G	24	185
82S185	2048x4	TS	—	100	M,C	F,N	18	120
82S185A	2048x4	TS	—	50	M,C	F,N	18	155
82S185B	2048x4	TS	—	45	C	F,N	18	155
82S191	2048x8	TS	—	80	M,C	F,N	24	175
82S191A	2048x8	TS	—	55	M,C	F,N	24	175
82S191B*	2048x8	TS	—	45	M,C	F,N	24	175
82HS195*	4096x4	TS	—	30	M,C	F,N	20	155
82S321*	4096x8	TS	—	70	M,C	F,N	24	175
82HS321*	4096x8	TS	—	40	M,C	F,N	24	175
82HS641*	8192x8	TS	—	45	M,C	F,N	24	175

SELECTION GUIDE

Device	Org	Output CKT 1	Output Logic 2	Access Time 3	Temp 4	Pkg 5	Pins	Max Icc
CAMs								
10155	8x2	OE	—	13	C	F,N	18	140
RAMs								
3101A	16x4	OC	B	35	C	F,N	16	105
54/74S189	16x4	TS	B	35	M,C	F,N	16	110
82S21	32x2	OC	T	50	C	F,N	16	130
82S16	256x1	TS	T	50	M,C	F,N	16	115
82S17	256x1	OC	T	50	M,C	F,N	16	115
74S301	256x1	OC	B	50	M,C	F,N	16	115
82LS16	256x1	TS	T	40	M,C	F,N	16	70
82LS17	256x1	OC	T	40	M,C	F,N	16	70
74LS301	256x1	OC	B	40	M,C	F,N	16	70
82S09	64x9	OC	T	45	M,C	F,N	28	190
82S09A	64x9	OC	T	35	C	F,N	28	190
82S19	64x9	OC	B	35	M,C	F,N	28	190
82S210	256x9	TS	B	60	M,C	F,N	24	185
82S212	256x9	TS	B	45	M,C	F,N	22	185
82S212A	256x9	TS	B	35	C	F,N	22	185
8X350	256x8	TS	B	N/A	M,C	F,N	22	185

NOTES:

1 Output circuit
- OE = Open Emitter
- OC = Open Collector
- TS = 3 State

2 Output logic
- T = Transparentinput data appears on output during Write
- B = Blankedoutput is blanked during Write
- R = Register
- I/O = Input/Output option
- L = Latch

3 Commercial (0°C to +75°C) except (82S2708)

4 Temperature range
- C = Commercial (0°C to +75°C)
- M = Military (−55°C to +125°C)
- A = Automotive (−40°C to +85°C)

5 Packages:
- F = Hermetic Cerdip Dual In Line
- N = Plastic Dual In Line
- R = Ceramic Flat Pack (Military only)
- G = Ceramic Square Leadless Chip Carrier (Military only)

*Under development

FIELD PROGRAMMABLE GATE ARRAY (18×15×12) — 82S151

INTEGRATED FUSE LOGIC
SERIES 20

DESCRIPTION

The 82S151 is a single level logic element, consisting of 12 AND gates with fusible link connections for programming I/O polarity, I/O direction and output enable control.

All gates are linked to 6 inputs (I) and 12 bidirectional I/O lines (B). These yield variable I/O gate configurations via 3 direction control gates (D), ranging from 18 inputs to 12 outputs.

On chip T/C buffers couple either True (I, B) or Complement ($\overline{I}$, $\overline{B}$) input polarities to each AND gate. The polarity of all gate outputs is individually programmable through a set of EX-OR gates for implementing AND/NAND logic functions. Alternately, if desired, OR/NOR logic functions can also be realized by programming for each gate the complement of its inputs and output (DeMorgan's Theorem).

The 82S151 is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

This device is available in a 20-pin slimline package. For the commercial temperature range (0°C to +75°C) specify N82S151 N or F. For the military temperature range (−55°C to +125°C) specify S82S151 F only.

FEATURES

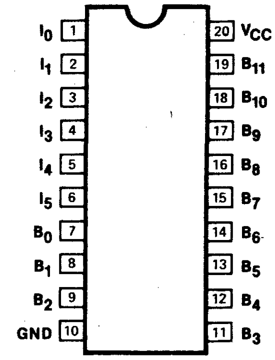
- **Field Programmable (Ni-Cr link)**
- **6 inputs**
- **15 Product Terms:**
  - **12 Logic Terms**
  - **3 Control Terms**
- **12 bidirectional I/O lines**
- **Active high or low outputs**
- **Programmable output enable**
- **Power dissipation: 650mW (typ)**
- **I/O propagation delay: 25ns (max)**
- **Input loading**
  - **N82S151: −100μA (max)**
  - **S82S151: −150μA (max)**
- **Output: three-state**
- **TTL compatible**

APPLICATIONS

- **Random gating functions**
- **Address decoding**
- **Code detectors**
- **Memory mapped I/O**
- **Fault monitors**
- **I/O port decoders**

PIN CONFIGURATION

F,N PACKAGES



F = Cerdip
N = Plastic

LOGIC FUNCTIONS

Typical Output Functions:

Active-High

$X = A \cdot \overline{B} \cdot C \cdot \ldots\ldots$

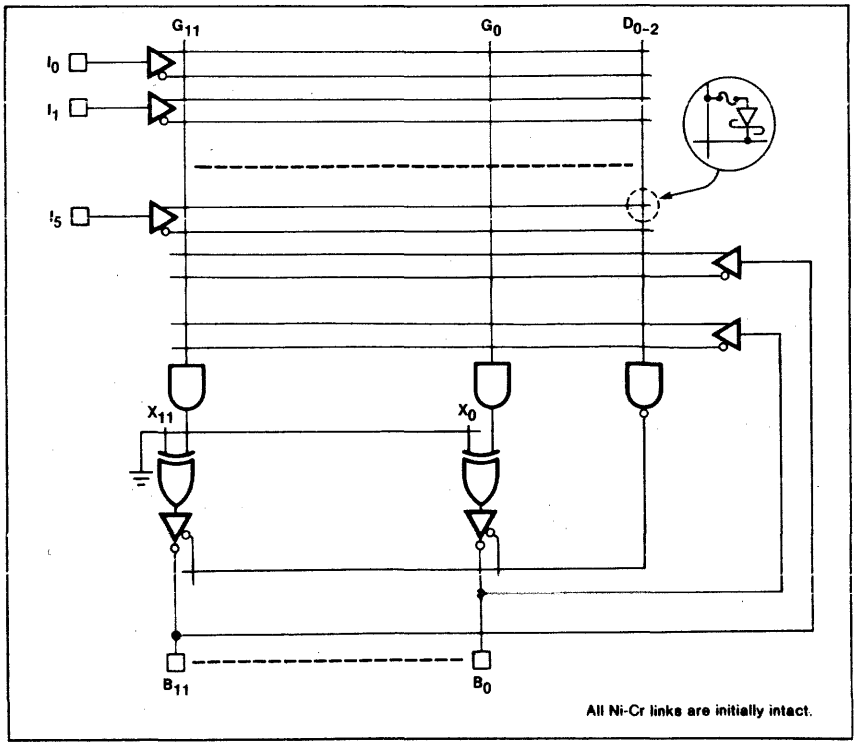
Active-Low

$\overline{X} = \overline{A \cdot \overline{B} \cdot C \cdot \ldots\ldots}$

$\overline{X} = \overline{A} + B + \overline{C} + \ldots\ldots$

NOTES:
1. For each of the 12 outputs, either function X (active-high) or $\overline{X}$ (active-low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. X, A, B, C, etc. are user defined connections to fixed inputs (I) and bidirectional pins (B).

FUNCTIONAL DIAGRAM



FIELD PROGRAMMABLE GATE ARRAY (18×15×12)

82S151

INTEGRATED FUSE LOGIC
SERIES 20

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING[1] Min	Max	UNIT
V_{CC}	Supply voltage		+7	Vdc
V_{IN}	Input voltage		+5.5	Vdc
V_{OUT}	Output voltage		+5.5	Vdc
I_{IN}	Input currents	−30	+30	mA
I_{OUT}	Output currents		+100	mA
	Temperature range			C°
T_A	Operating			
	N82S151	0	+75	
	S82S151	−55	+125	
T_{STG}	Storage	−65	+150	

THERMAL RATINGS

TEMPERATURE	Military	Commercial
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

DC ELECTRICAL CHACTERISTICS

N82S151: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82S151: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER		TEST CONDITION	N82S151 Min	N82S151 Typ[2]	N82S151 Max	S82151 Min	S82151 Typ[2]	S82151 Max	UNIT
	Input voltage[3]								V
V_{IL}	Low	V_{CC} = Min			.80			.80	
V_{IH}	High	V_{CC} = Max	2.0			2.0			
V_{IC}	Clamp[3,4]	V_{CC} = Min, I in = −12mA		−.8	−1.2		−.8	−1.2	
	Output voltage[3]	V_{CC} = Min							V
V_{OL}	Low	I_{OL} = 10mA			.5				
V_{OL}	Low	I_{OL} = 8mA						.5	
V_{OH}	High	I_{OH} = −2mA	2.4			2.4			
	Input Current	V_{CC} = Max							µA
I_{IL}	Low	V_{IN} = 0.45V			−100			−150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output Current	V_{CC} = max							
$I_{O(OFF)}$	Hi-Z state[7]	V_{OUT} = 5.5V			80			110	µA
		V_{OUT} = .45V			−140			−210	
I_{OS}	Short circuit[4,5]	V_{OUT} = 0V	−15		−70	−15		−85	mA
I_{CC}	V_{CC} supply current	V_{CC} = max		130	155		130	155	mA
	Capacitance	V_{CC} = 5V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_B	I/O	V_B = 2.0V		15			15		

AC ELECTRICAL CHACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1K\Omega$
N82S151: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82S151: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER		TO	FROM	TEST CONDITIONS	N82S151 Min	N82S151 Typ[2]	N82S151 Max	S82S151 Min	S82S151 Typ[2]	S82S151 Max	UNIT
T_{PD}	Progagation delay	Output ±	Input ±	C_L = 30pF		20	25		20		ns
T_{OE}	Output enable	Output−	Input ±			20	25		20		ns
T_{OD}	Output disable[6]	Output+	Input ±	C_L = 5pF		20	25		20		ns

NOTES
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device of these or any other condition above those indicated in the operation of the device specifications is not implied.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Duration of short circuit should not exceed 1 second.
6. Measured at $V_T = V_{OL} + 0.5V$.
7. I_O (OFF) at V_{OUT} = 0.45V includes I_{IL} max value and at V_{OUT} = 5.5V includes I_{IH} max value.

FIELD PROGRAMMABLE LOGIC ARRAY (18×42×10) 82S153/82S153A (T.S.)

INTEGRATED FUSE LOGIC
SERIES 20

DESCRIPTION

The 82S153 and 82S153A are two-level logic elements, consisting of 32 AND gates and 10 OR gates with fusible link connections for programming I/O polarity and direction.

All AND gates are linked to 8 inputs (I) and 10 bidirectional I/O lines (B). These yield variable I/O gate configurations via 10 direction control gates (D), ranging from 18 inputs to 10 outputs.

On chip T/C buffers couple either True (I, B) or Complement ($\overline{I}$, $\overline{B}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Their output polarity, in turn, is individually programmable through a set of EX-OR gates for implementing AND/OR or AND/NOR logic functions.

The 82S153 and the 82S153A are field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Both devices are available in a 20-pin slim line package. For the commercial temperature range (0°C to +75°C) specify N82S153 N or F and N82S153A N or F. For the military temperature range (−55°C to +125°C) specify S82S153 F only and S82S153A F only.

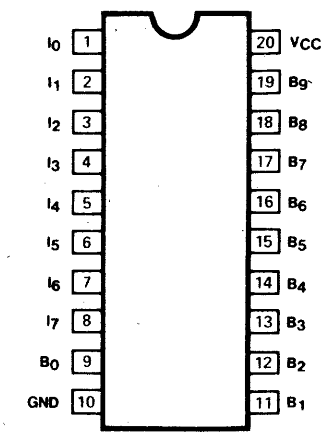
FEATURES

- **Field Programmable (Ni-Cr links)**
- **8 inputs**
- **32 AND gates**
- **10 OR gates**
- **10 bidirectional I/O lines**
- **Active high or low outputs**
- **42 Product Terms:**
  - **32 Logic Terms**
  - **10 Control Terms**
- **I/O propagation delay:**
  - **N82S153: 40ns (max)**
  - **N82S153A: 30ns (max)**
  - **S82S153: 60ns (max)**
  - **S82S153A: 45ns (max)**
- **Input loading**
  - **N82S153: −100μA (max)**
  - **S82S153: −150μA (max)**
- **Power dissipation:**
  - **650mW (typ)**
- **Output: three-state**
- **TTL compatible**

APPLICATIONS

- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping**
- **Multiplexing**

PIN CONFIGURATION



F = Cerdip
N = Plastic

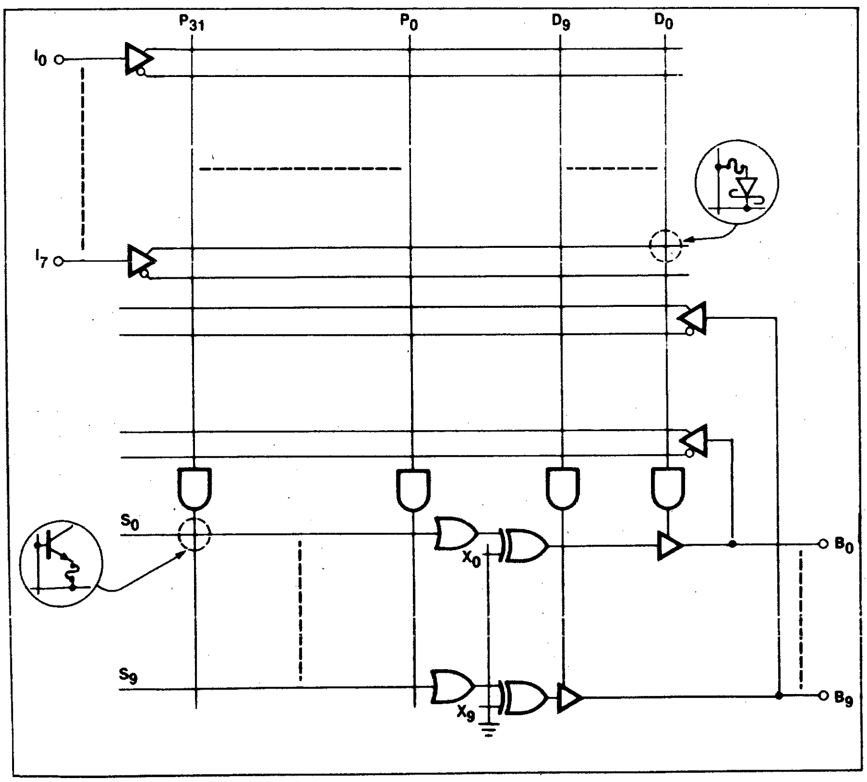
LOGIC FUNCTION

Typical product term:
$Pn = A \cdot \overline{B} \cdot C \cdot D \cdot \ldots\ldots$
Typical logic function:
At Output Polarity = H
$Z = P0 + P1 + P2 \ldots.$

At Output Polarity = L
$\overline{Z} = \overline{P0 + P1 + P2 + \ldots.}$
$Z = \overline{P0} \cdot \overline{P1} \cdot \overline{P2} \ldots.$

NOTES:
1. For each of the 10 outputs, either function Z (active-high) or $\overline{Z}$ (active-low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. Z, A, B, C, etc. are user defined connections to fixed inputs (I) and bidirectional pins (B).

FUNCTIONAL DIAGRAM



FIELD PROGRAMMABLE LOGIC ARRAY (18×42×10) 82S153/82S153A (T.S.)

INTEGRATED FUSE LOGIC
SERIES 20

ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING Min	RATING Max	UNIT
V_{CC}	Supply voltage		+7	Vdc
V_{IN}	Input voltage		+5.5	Vdc
V_{OUT}	Output voltage		+5.5	Vdc
I_{IN}	Input currents	−30	+30	mA
I_{OUT}	Output currents		+100	mA
	Temperature range			C°
T_A	Operating			
	N82S153/153A	0	+75	
	S82S153/153A	−55	+125	
T_{STG}	Storage	−65	+150	

THERMAL RATINGS

TEMPERATURE	Military	Commercial
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

DC ELECTRICAL CHARACTERISTICS

N82S153, N82S153A: $0°C \le T_A \le +75°C$, $4.75 \le V_{CC} \le 5.25V$
S82S153, S82S153A: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

	PARAMETER	TEST CONDITION	N82S153 Min	N82S153 Typ[2]	N82S153 Max	S82S153 Min	S82S153 Typ[2]	S82S153 Max	UNIT
	Input voltage[3]								V
V_{IL}	Low	V_{CC} = min			.85			.80	
V_{IH}	High	V_{CC} = max	2.0			2.0			
V_{IC}	Clamp[3,4]	V_{CC} = min, Iin = −12mA		−.8	−1.2		−.8	−1.2	
	Output voltage	V_{CC} = min							V
V_{OL}	Low[3,5]	I_{OL} = 15mA			.5				
V_{OL}	Low[3,5]	I_{OL} = 12mA						.5	
V_{OH}	High[3,6]	I_{OH} = −2mA	2.4			2.4			
	Input current	V_{CC} = max							μA
I_{IL}	Low	V_{IN} = 0.45V			−100			−150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current	V_{CC} = max							
$I_{O(OFF)}$	Hi-Z state[10]	V_{OUT} = 5.5V			80			110	μA
		V_{OUT} = .45V			−140			−210	
I_{OS}	Short circuit[4, 6, 7]	V_{OUT} = 0V	−15		−70	−15		−85	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = max		130	155		130	165	mA
	Capacitance	V_{CC} = 5V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_B	I/O	V_B = 2.0V		15			15		

AC ELECTRICAL CHACTERISTICS

$R_A = 470\Omega$, $R_2 = 1K\Omega$
N82S153, N82S153A: $0°C \le T_A \le +75°C$, $4.75 \le V_{CC} \le 5.25V$
S82S153, S82S153A: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

	PARAMETER	TO	FROM	TEST CONDITIONS	N82S153 Min	N82S153 Typ	N82S153 Max	S82S153 Min	S82S153 Typ	S82S153 Max	UNIT
T_{PD}	Progagation delay	Output ±	Input ±	C_L = 30pF		30	40		30	55	ns
T_{OE}	Output enable	Output−	Input ±			25	35		25	45	
T_{OD}	Output disable[9]	Output+	Input ±	C_L = 5pF		25	35		25	45	ns

	PARAMETER	TO	FROM	TEST CONDITIONS	N82S153A Min	N82S153A Typ	N82S153A Max	S82S153A Min	S82S153A Typ	S82S153A Max	UNIT
T_{PD}	Progagation delay	Output ±	Input ±	C_L = 30pF		20	30		20	45	ns
T_{OE}	Output enable	Output−	Input ±			20	30		20	40	
T_{OD}	Output disable[9]	Output+	Input ±	C_L = 5pF		20	30		20	40	ns

INTEGRATED FUSE LOGIC
SERIES 20

DESCRIPTION

The 82S159 is a three state output registered logic element combining AND/OR gate arrays with clocked J/K flip-flops, dynamically convertible to D-type via a "foldback" inverting buffer and control gate F_C. It features 8 registered I/O outputs (F), in conjunction with bidirectional I/O lines (B). These yield variable I/O gate and register configurations via control gates (D, L) ranging from 16 inputs to 12 outputs.

The AND/OR arrays consist of 32 logic AND gates, 13 control AND gates, and 21 OR gates with fusible link connections for programming I/O polarity and direction. All AND gates are linked to 4 inputs (I), bidirectional I/O lines (B), internal flip-flop outputs (Q), and Complement Array output ($\overline{C}$). The Complement Array consists of a NOR gate optionally linked to all AND gates for generating and propagating complementary AND terms.

On chip I/C buffers couple either True (I, B, Q) or Complement ($\overline{I}$, $\overline{B}$, $\overline{Q}$, $\overline{C}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. One group of OR gates drives bidirectional I/O lines (B), whose output polarity is individually programmable through a set of EX-OR gates for implementing AND-OR or AND-NOR logic functions. Another group drives the J-K inputs of all flip-flops, as well as asynchronous Preset and Reset lines (P, R), (except the 82S158/159, where AND functions are provided).

All flip-flops are positive edge trigger and can be used as input, output, or I/O (for interfacing with a bidirectional data bus) in conjunction with load control gates (L), steering inputs (I), (B), (Q) and programmable output select lines (E).

The 82S159 is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

The 82S159 is available in a 20-pin, slim line package. For the commercial temperature range (0°C to +75°C) specify N82S159N or F. For the military range (−55°C to +125°C) specify S82S159F only.

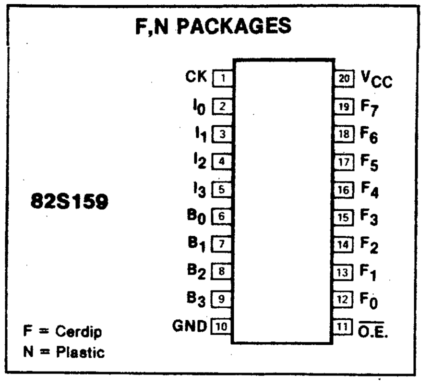
FEATURES

- Field programmable (Ni-Cr link)
- 4 dedicated inputs
- 13 control gates
- 32 AND gates
- 21 OR gates
- 45 product terms:
  32 logic terms
  13 control terms
- 4 bidirectional I/O lines
- 8 bidirectional registers
- J/K, T, or D-type flip-flops
- Asynchronous Preset/Reset
- Complement Array
- Active high or low outputs
- Programmable $\overline{O.E.}$ control
- Positive edge trigger clock
- Power-on reset on all flip-flops (F_n = "1")
- Clock frequency: N82S159: 15 MHz (max)
  S82S159: MHz (max)
- Input loading: N82S159: −100μA (max)
  S82S159: −150μA (max)
- Power dissipation: 650mW (typ)
- TTL Compatible

APPLICATIONS

- Random sequential logic
- Synchronous up/down counters
- Shift registers
- Bidirectional data buffers
- Timing function generators
- System controllers/synchronizers
- Priority encoder/registers

PIN CONFIGURATION



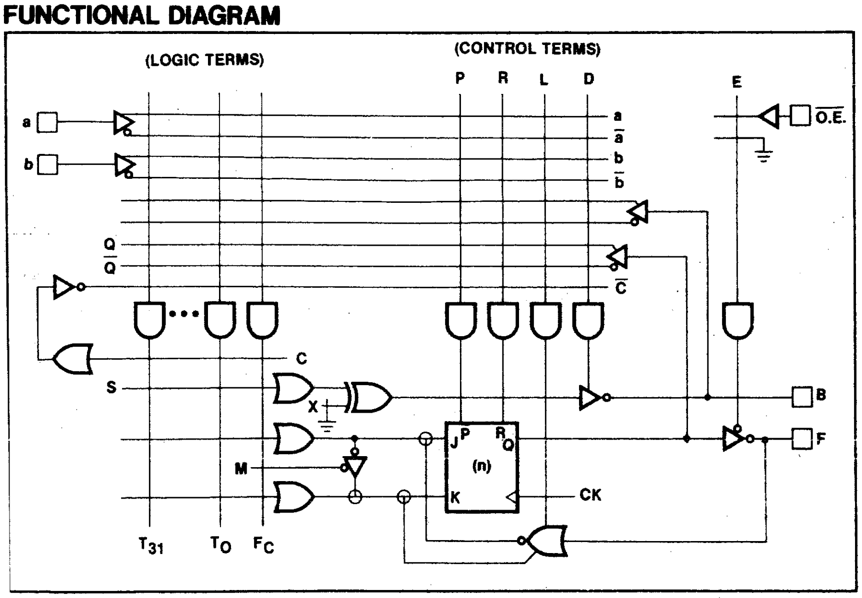
FLIP-FLOP TRUTH TABLE

V_{CC}	$\overline{O.E.}$	L	CK	P	R	J	K	Q	F
	H								H/HI-Z
↑	L	X	X	L	X	X	X	L	H
+5	L	X	X	H	L	X	X	H	L
	L	X	X	L	H	X	X	L	H
	L	L	↑	L	L	L	L	Q	$\overline{Q}$
	L	L	↑	L	L	L	H	L	H
	L	L	↑	L	L	H	L	H	L
	L	L	↑	L	L	H	H	$\overline{Q}$	Q
	H	H	↑	L	L	L	H	L	H*
	H	H	↑	L	L	H	L	H	L*
	+10V	X	↑	X	X	L	H	L	H**
	+10V	X	↑	X	X	H	L	H	L**

NOTES

1. Positive Logic:
   $J/K = T_0 + T_1 + T_2 \ldots\ldots\ldots T_{47}$
   $T_n = \overline{C} \bullet (I_0 \bullet I_1 \bullet I_2 \ldots) \bullet (Q_0 \bullet Q_1 \ldots) \bullet (B_0 \bullet B_1 \bullet \ldots)$
2. ↑ denotes transition from Low to High level.
3. X = Don't Care
4. * = Forced at F_n pin for loading J/K flip-flop in I/O mode. L must be enabled, and other active T_n disabled via steering input(s) I, B, or Q.
5. At P = R = H, Q = H. The final state of Q depends on which is released first.
6. ** = Forced at F_n pin to load J/K flip-flop independent of program code (Diagnostic mode).

FUNCTIONAL DIAGRAM



FIELD PROGRAMMABLE LOGIC SEQUENCER (16×45×12)

82S159 (T.S.)

INTEGRATED FUSE LOGIC
SERIES 20

ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING Min	RATING Max	UNIT
V_{CC}	Supply voltage		+7	Vdc
V_{IN}	Input voltage		+5.5	Vdc
V_{OUT}	Output voltage		+5.5	Vdc
I_{IN}	Input currents	−30	+30	mA
I_{OUT}	Output currents		+100	mA
	Temperature range			°C
T_A	Operating			
	N82S159	0	+75	
	S82S159	−55	+125	
T_{STG}	Storage	−65	+150	

THERMAL RATINGS

TEMPERATURE	MILITARY	COMMERCIAL
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

DC ELECTRICAL CHARACTERISTICS

N82S159: $0° \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S159: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

	PARAMETER	TEST CONDITIONS	N82S159 Min	N82S159 Typ[2]	N82S159 Max	S82S159 Min	S82S159 Typ[2]	S82S159 Max	UNIT
	Input voltage[3]								V
V_{IH}	High	V_{CC} = Max	2			2			
V_{IL}	Low	V_{CC} = Min			0.80			0.8	
V_{IC}	Clamp	V_{CC} = Min, I_{IN} = −12mA		−0.8	−1.2		−0.8	−1.2	
	Output voltage[3]	V_{CC} = Min							V
V_{OH}	High (82S155/7/9)	I_{OH} = −2mA	2.4			2.4			
V_{OL}	Low	I_{OL} = 10mA		0.35	0.5				
V_{OL}	Low	I_{OL} = 10mA					0.35	0.5	
	Input current	V_{CC} = Max							μA
I_{IH}	High	V_{IN} = 5.5V		<1	40		<1	50	
I_{IL}	Low	V_{IN} = 0.45V		−10	−100		−10	−150	
I_{IL}	Low (CK input)	V_{IN} = 0.45V		−50	−250		−50	−350	
	Output current	V_{CC} = Max							
$I_{O(OFF)}$	Hi-Z state[8]	V_{OUT} = 5.5V		1	80		1	110	μA
		V_{OUT} = 0.45V		−1	−140		−1	−210	
I_{OS}	Short circuit[4,6]	V_{OUT} = 0V	−15		−70	−15		−85	mA
I_{CC}	V_{CC} supply current[7]	V_{CC} = Max		150	190		150	190	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_{OUT}	Output	V_{OUT} = 2.0V		15			15		

NOTES
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device of these or any other condition above those indicated in the operation of the device specifications is not implied.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured with V_{IH} applied to $\overline{O.E.}$
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with the $\overline{O.E.}$ input grounded, all other inputs at 4.5V and the outputs open.
8. I_O (OFF) at V_{OUT} = 0.45V includes I_{IL} max value and at V_{OUT} = 5.5V includes I_{IH} max value.

Signetics

MEMORY

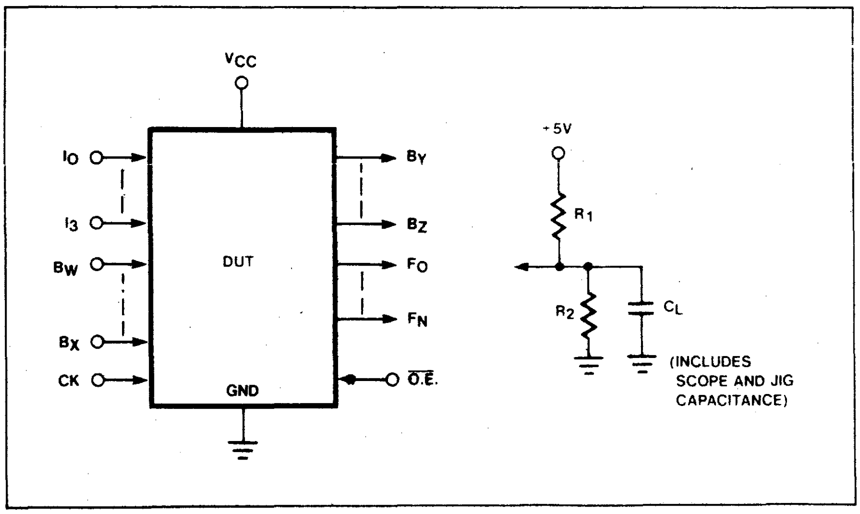
AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$

N82S159: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82S159: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

	PARAMETER	TO	FROM	TEST CONDITIONS	N82S159 Min[5]	N82S159 Typ[1]	N82S159 Max	S82S159 Min	S82S159 Typ[1]	S82S159 Max	UNIT
	Pulse width										ns
T_{CKH}	Clock[2] high	CK−	CK+		25	20			20		
T_{CKL}	Clock low	CK+	CK−		30	20			20		
T_{CKP}	Period	CK+	CK+		70	50			50		
T_{PRH}	Preset/Reset pulse	(I,B)+	(I,B)−		40	30			20		
	Set up time										ns
T_{IS1}	Input	CK+	(I,B)±		40	30			30		
T_{IS2}	Input (through F_n)	CK+	F±	C_L = 30pF	—	10			5		
T_{IS3}	Input (through Complement array)[4]	CK+	(I,B)±		65	40			40		
	Hold time										ns
T_{IH1}	Input	CK+	(I,B)±			−10	0		−10		
T_{IH2}		CK+	F±			0	—		−5		
	Propagation delay										ns
T_{CKO}	Clock	F±	CK+			25	30		25		
T_{OE1}	Output enable	F−	$\overline{O.E.}$−			20	30		20		
T_{OD1}	Output disable[3]	F+	$\overline{O.E.}$+	C_L = 5pF		20	55		20		
T_{PD}	Output	B±	(I,B)±	C_L = 30pF		40	50		35		
T_{OE2}	Output enable	B±	(I,B)+			35	55		35		
T_{OD2}	Output disable[3]	B+	(I,B)−	C_L = 5pF		35	35		35		
T_{PRO}	Preset/Reset	F±	(I,B)+	C_L = 30pF		50	55		50		
T_{PPR}	Power-on preset	F−	V_{CC}+			0	10		0		

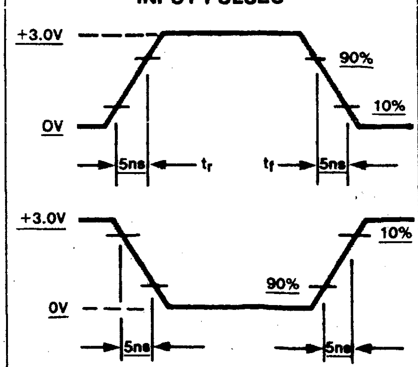
NOTE
1. All typical values are at V_{CC} = 5V, T_A = 25°C.
2. To prevent spurious clocking, clock rise time (10%-90%) ≤ 10ns.
3. Measured at $V_T = V_{OL}$ + 0.5 V.
4. When using the Complement Array T_{CKP} = 75ns (min).
5. Limits are guaranteed with 12 product terms maximum connected to each sum term line.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM

INPUT PULSES



Measurements: All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

FIELD PROGRAMMABLE LOGIC SEQUENCER (14×48×6) 82S167 (T.S.)

INTEGRATED FUSE LOGIC
SERIES 24

DESCRIPTION

The 82S167 is a bipolar, programmable state machine of the Mealy type. It contains logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip state and output registers. These consist respectively of 8 Q_p, and 4 Q_f edge-triggered, clocked S/R flip-flops, with an asynchronous preset option.

All flip-flops are unconditionally preset to "1" during power turn-on.

The AND array combines 14 external inputs, $I_{0\text{-}13}$, with 8 internal inputs, $P_{0\text{-}7}$, fed back from the State register to form up to 48 transition terms (AND terms). In addition, bit-0 and bit-1 of the internal state register are brought off-chip to allow extending the output register to 6 bits, if so desired.

All transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the low to high transition of the Clock pulse.

Both True and Complement transition terms can be generated by optional use of the internal variable (C) from the complement array. Also, if desired, the Preset input can be converted to output-enable function, as an additional user programmable option.

The device is available in the commercial temperature range. For the commercial temperature range (0°C to +75°C) specify N82S167F or N.

FEATURES

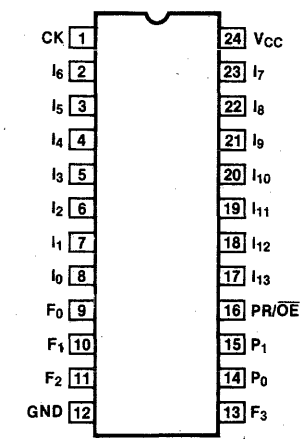
- Field programmable (Ni-Cr link)
- 14 True/Complement buffered inputs
- 48 programmable AND gates
- 25 programmable OR gates
- 8-bit state register
- 2-bit shared state/output register
- 4-bit output register
- Transition complement array
- Programmable asynchronous preset/output enable
- Positive edge-trigger clock
- Power-on preset to logic "1" of all registers
- Automatic logic "HOLD" state via S/R flip-flops
- On-chip test array
- $f_{(max)}$: 13.9MHz (82S167)
- Power: 650mW (typ)
- TTL compatible
- Tri-state outputs
- Single +5V supply
- 300 mil wide 24-pin DIP

APPLICATIONS

- Interface protocols
- Sequence detectors
- Peripheral controllers
- Timing generators
- Sequential circuits
- Elevator controllers
- Security locking systems
- Counters
- Shift registers

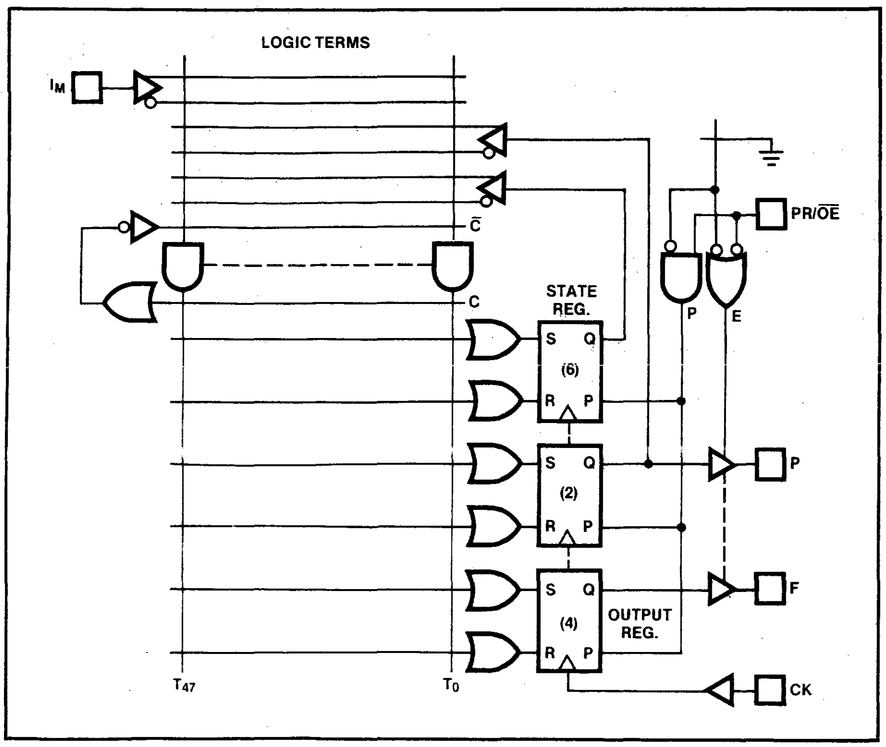
PIN CONFIGURATION

F, N PACKAGE*



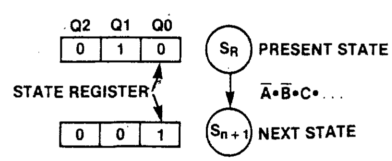
*F = Cerdip
N = Plastic

LOGIC DIAGRAM



LOGIC FUNCTION

Typical State Transition:



SET Q_0: $S_0 = (\bar{Q}_2 \cdot Q_1 \cdot \bar{Q}_0) \cdot \bar{A} \cdot \bar{B} \cdot C \ldots$
$R_0 = 0$

RESET Q_1: $S_1 = 0$
$R_1 = (\bar{Q}_2 \cdot Q_1 \cdot \bar{Q}_0) \cdot \bar{A} \cdot \bar{B} \cdot C \ldots$

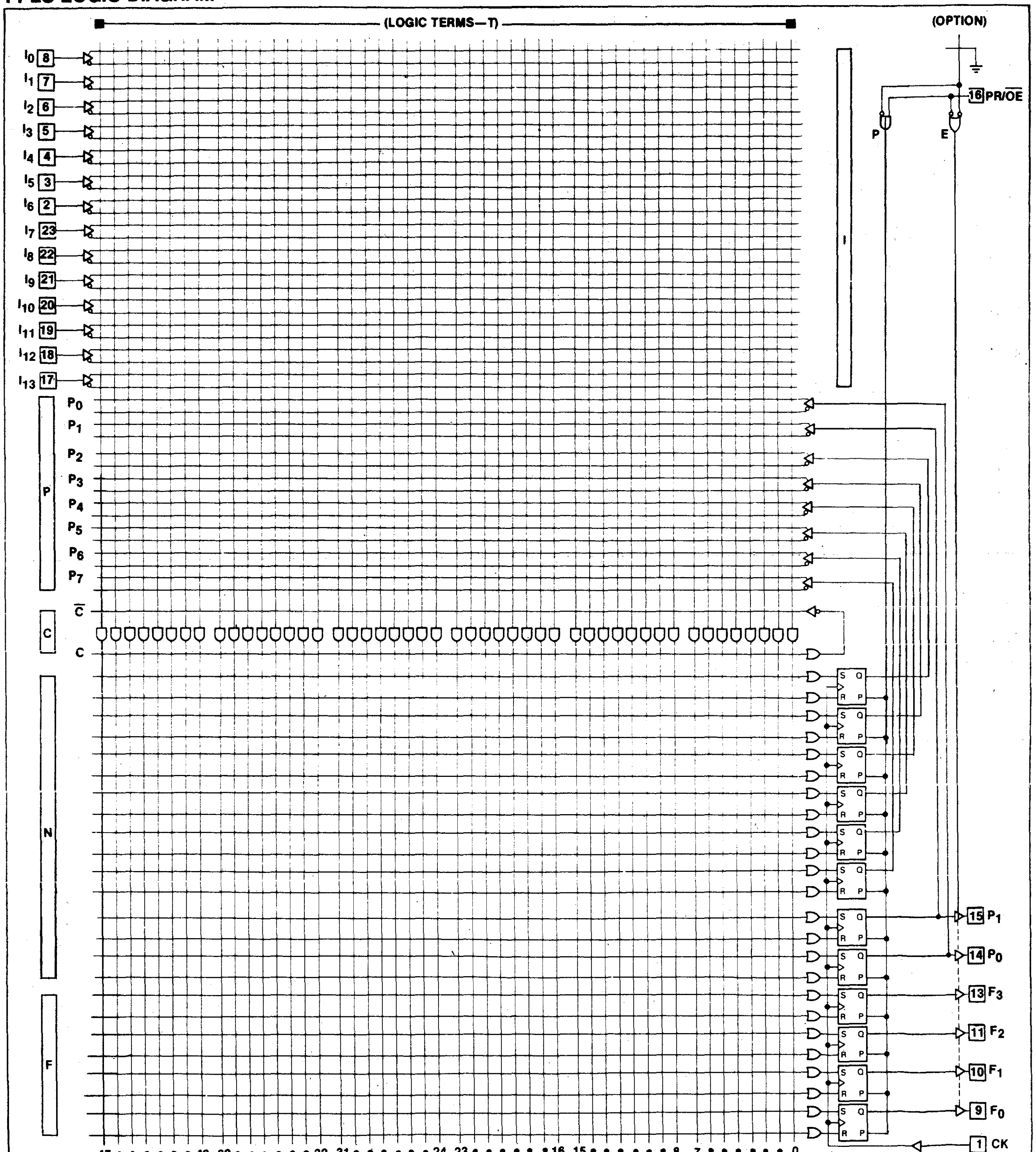
HOLD Q_2: $S_2 = 0$
$R_2 = 0$

FIELD PROGRAMMABLE LOGIC SEQUENCER (14×48×6)

82S167 (T.S.)

INTEGRATED FUSE LOGIC
SERIES 24

FPLS LOGIC DIAGRAM



NOTES

1. All AND gate inputs with a blown link float to a logic "1".
2. All OR gate inputs with a blown link float to a logic "0".

FIELD PROGRAMMABLE LOGIC ARRAY (16×48×8) 82S100 (T.S.)/82S101 (O.C.)

INTEGRATED FUSE LOGIC
SERIES 28

DESCRIPTION

The 82S100 (tri-state) and 82S101 (open collector) are Bipolar, Fuse-Link Programmable Logic Arrays (FPLA). Each device utilizes the standard AND/OR/Invert architecture to directly implement custom sum of product logic equations.

Each device consists of 16 dedicated inputs and 8 dedicated outputs. Each output is capable of being actively controlled by any or all of the 48 product terms. The true, complement, or don't care condition of each of the 16 inputs ANDed together comprise one P-term. All 48 P-terms are then ORed to each output. The user must then only select which P-terms will activate an output by disconnecting terms which do not affect the output. In addition each output can be fused as active-high(H) or active-low(L).

The 82S100 and 82S101 are fully TTL compatible, and include chip-enable control for expansion of input variables, and output inhibit. They feature either open collector or tri-state outputs for ease of expansion of product terms and application in bus-organized systems.

Both devices are available in commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S100/101, F or N, and for the military temperature range (−55°C to +125°C specify S82S100/101, F, G or R.

FEATURES

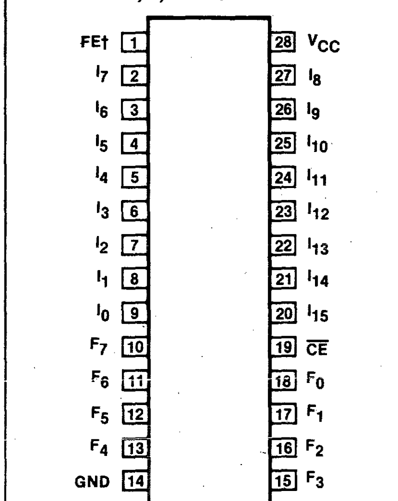
- **Field programmable (Ni-Cr link)**
- **Input variables: 16**
- **Output functions: 8**
- **Product terms: 48**
- **Address access time:**
  - **S82S100/101 — 80ns max**
  - **N82S100/101 — 50ns max**
- **Power dissipation: 600mW typ**
- **Input loading:**
  - **S82S100/101: −150μA max**
  - **N82S100/101: −100μA max**
- **Chip enable input**
- **Output option:**
  - **82S100: Tri-state**
  - **82S101: Open collector**
- **Output disable function:**
  - **Tri-state — Hi-Z**
  - **Open collector — Hi**
- **Separate I/O architecture**

APPLICATIONS

- **CRT display systems**
- **Random logic**
- **Code conversion**
- **Peripheral controllers**
- **Function generators**
- **Look-up and decision tables**
- **Microprogramming**
- **Address mapping**
- **Character generators**
- **Data security encoders**
- **Fault detectors**
- **Frequency synthesizers**
- **16 bit-to-8 bit bus interface**
- **Random logic replacement**

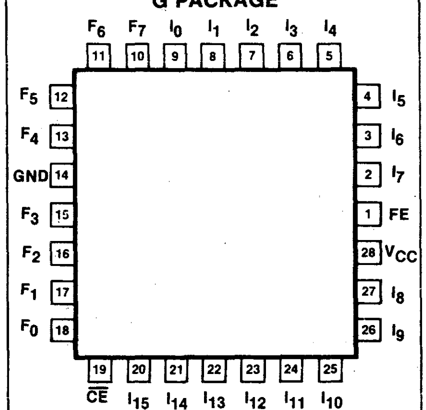
PIN CONFIGURATION

F,N,R PACKAGE*



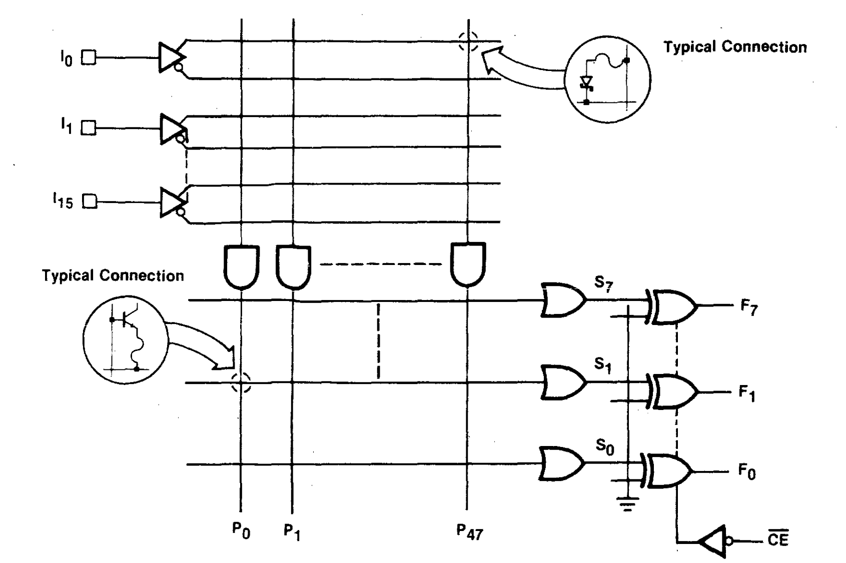
*F = Cerdip N = Plastic R = Flat Pack
†Open or grounded during normal operation.

G PACKAGE



G = Leadless

LOGIC DIAGRAM



Fusible Ni-Cr links are initially intact at all array cross-points.

FIELD PROGRAMMABLE LOGIC ARRAY (16×48×8) 82S100 (T.S.)/82S101 (O.C.)

INTEGRATED FUSE LOGIC
SERIES 28

ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING Min	RATING Max	UNIT
V_{CC}	Supply voltage		+7	Vdc
V_{IN}	Input voltage		+5.5	Vdc
V_{OUT}	Output voltage		+5.5	Vdc
I_{IN}	Input currents	−30	+30	mA
I_{OUT}	Output currents		+100	mA
	Temperature range			°C
T_A	Operating			
	N82S100/101	0	+75	
	S82S100/101	−55	+125	
T_{STG}	Storage	−65	+150	

THERMAL RATINGS

TEMPERATURE	MILITARY	COMMERCIAL
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

DC ELECTRICAL CHARACTERISTICS

N82S100/101: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S100/101: −55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

	PARAMETER	TEST CONDITIONS	N82S100/101 Min	N82S100/101 Typ[2]	N82S100/101 Max	S82S100/101 Min	S82S100/101 Typ[2]	S82S100/101 Max	UNIT
	Input voltage[3]								V
V_{IH}	High	V_{CC} = Max	2			2			
V_{IL}	Low	V_{CC} = Min			0.8			0.8	
V_{IC}	Clamp[3,4]	V_{CC} = Min, I_{IN} = −12mA		−0.8	−1.2		−0.8	−1.2	
	Output voltage	V_{CC} = Min							V
V_{OH}	High (82S100)[3,5]	I_{OH} = −2mA	2.4			2.4			
V_{OL}	Low[3,6]	I_{OL} = 9.6mA		0.35	0.45		0.35	0.50	
	Input current								μA
I_{IH}	High	V_{IN} = 5.5V		<1	25		<1	50	
I_{IL}	Low	V_{IN} = 0.45V		−10	−100		−10	−150	
	Output current	$\overline{CE}$ = High, V_{CC} = Max							
I_{OLK}	Leakage[7]	V_{OUT} = 5.5V		1	40		1	60	μA
$I_{O(OFF)}$	Hi-Z state (82S100)[7]	V_{OUT} = 5.5V		1	40		1	60	μA
		V_{OUT} = 0.45V		−1	−40		−1	−60	
I_{OS}	Short circuit (82S100)[4,8]	$\overline{CE}$ = Low, V_{OUT} = 0V	−15		−70	−15		−85	mA
I_{CC}	V_{CC} supply current[9]	V_{CC} = Max		120	170		120	180	mA
	Capacitance[7]	$\overline{CE}$ = High, V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_{OUT}	Output	V_{OUT} = 2.0V		17			17		

AC ELECTRICAL CHARACTERISTICS

R_1 = 470Ω, R_2 = 1kΩ, C_L = 30pF
N82S100/101: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S100/101: −55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

	PARAMETER	TO	FROM	N82S100/101 Min	N82S100/101 Typ[2]	N82S100/101 Max	S82S100/101 Min	S82S100/101 Typ[2]	S82S100/101 Max	UNIT
	Propagation delay									ns
T_{IA}	Input	Output	Input		35	50		35	80	
T_{CE}	Chip enable	Output	Chip enable		15	30		15	50	
	Disable time									ns
T_{CD}	Chip disable	Output	Chip enable		15	30		15	50	

NOTES:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and only functional operation of the device at these or any other conditions above those indicated in the operation of the device specifications is not implied.
2. All voltages are at V_{CC} = 5V, T_A = 25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic high stored.
6. Measured with a programmed logic condition for which the output test is at a low logic level. Output sink current is applied through a resistor to V_{CC}.
7. Measured with V_{IH} applied to $\overline{CE}$.
8. Duration of short circuit should not exceed 1 second.
9. I_{CC} is measured with the chip enable input grounded, all other inputs at 4.5V and the outputs open.

FIELD PROGRAMMABLE GATE ARRAY (16×9×9) 82S102 (O.C.)/82S103 (T.S.)

INTEGRATED FUSE LOGIC
SERIES 28

DESCRIPTION

The 82S102 and 82S103 are Bipolar, fuse programmable, gate arrays. The device consists of 9 AND/NAND Gates which share 16 common inputs. The type of gate is selected by programming the output as active-high(H) or active-low(L). Each of the 16 inputs I_0–I_{15} can be programmed to provide the True (H), Complement (L), or Don't Care (—) state to each of the 9 AND/NAND gates. OR/NOR logic functions can also be implemented by complementing the inputs and outputs via on-chip inverting buffers.

Both devices are field-programmable, which means that custom patterns are immediately available.

The 82S102 and 82S103 include chip-enable control for output strobing and inhibit. They feature either open collector or tri-state outputs for ease of expansion of input variables and application in bus-organized systems.

Both devices are available in the commercial and military temperature ranges. For the commercial range (0°C to +75°C) specify N82S102/103, F or N, and for the military range (−55°C to +125°C) specify S82S102/103, F, G, and R.

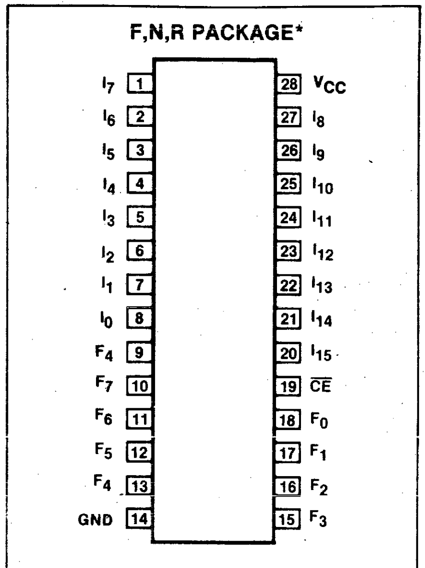
FEATURES

- **Field programmable (Ni-Cr link)**
- **16 input variables**
- **9 output functions**
- **Chip enable input**
- **I/O propagation delay:**
  - **N82S102/103: 35ns max**
  - **S82S102/103: 50ns max**
- **Power dissipation: 600mW typ**
- **Input loading:**
  - **N82S102/103: −100μA max**
  - **S82S102/103: −150μA max**
- **Output options:**
  - **82S102: Open collector**
  - **82S103: Tri-state**
- **Output disable function:**
  - **82S102: Hi**
  - **82S103: Hi-Z**
- **Fully TTL compatible**

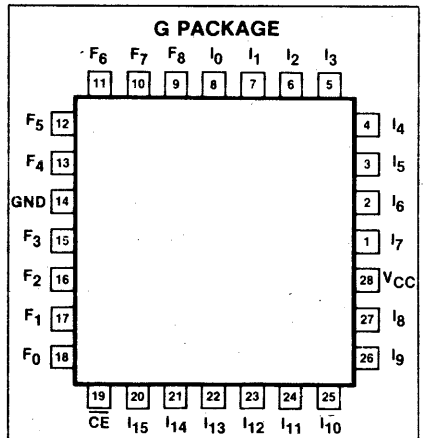
APPLICATIONS

- **Random logic**
- **Address decoders**
- **Code detectors**
- **Peripheral selectors**
- **Fault monitors**
- **Machine state decoders**

PIN CONFIGURATION

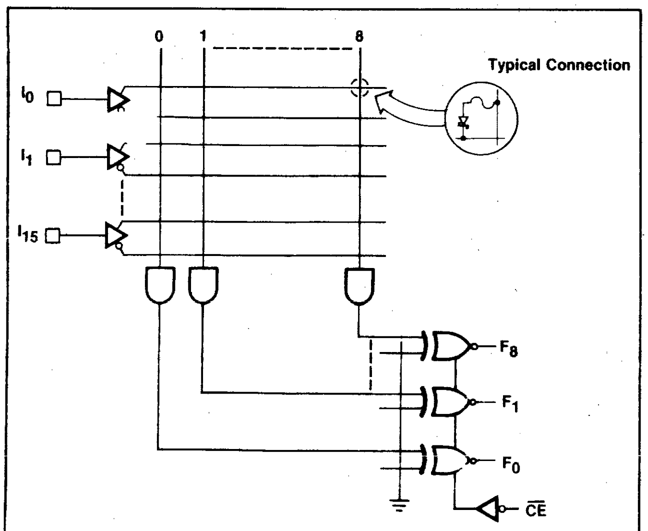


*F = Cerdip N = Plastic R = Flat Pack



G = Leadless

LOGIC DIAGRAM



Fusible Ni-Cr links are initially intact at all array cross-points.

FIELD PROGRAMMABLE GATE ARRAY (16×9×9) 82S102 (O.C.)/82S103 (T.S.)

INTEGRATED FUSE LOGIC
SERIES 28

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S102)	+5.5	
V_O	Off-state (82S103)	+5.5	
I_{IN}	Input current	±30	mA
I_{OUT}	Output current	+100	mA
	Temperature range		°C
T_A	Operating		
	N82S102/103	0 to +75	
	S82S102/103	−55 to +125	
T_{STG}	Storage	−65 to +150	

THERMAL RATINGS

TEMPERATURE	MILITARY	COMMERCIAL
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

DC ELECTRICAL CHARACTERISTICS

N82S102/103: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82S102/103: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER[1]		TEST CONDITIONS	N82S102/103			S82S102/103			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low[1]	V_{CC} = Min			0.8			0.8	
V_{IH}	High[1]	V_{CC} = Max	2.0			2.0			
V_{IC}	Clamp[1,3]	V_{CC} = Min, I_{IN} = −12mA		−0.8	−1.2		−0.8	−1.2	
	Output voltage	V_{CC} = Min							V
V_{OL}	Low[1,4]	I_{OL} = 9.6mA		0.35	0.45		0.35	0.50	
V_{OH}	High (82S103)[1,5]	I_{OH} = −2mA	2.4			2.4			
	Input current								µA
I_{IL}	Low	V_{IN} = 0.45V		−10	−100		−10	−150	
I_{IH}	High	V_{IN} = 5.5V		<1	25		<1	50	
	Output current	V_{CC} = Max							
I_{OLK}	Leakage (82S102)[6]	V_{OUT} = 5.5V		1	40		1	60	µA
$I_{O(OFF)}$	Hi-Z state (82S103)[6]	V_{OUT} = 5.5V		1	40		1	60	µA
		V_{OUT} = 0.45V		−1	−40		−1	−60	
I_{OS}	Short circuit (82S103)[3,7]	V_{OUT} = 0V	−15		−70	−15		−85	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = Max		120	170		120	180	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_{OUT}	Output[6]	V_{OUT} = 2.0V		15			15		

AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
N82S102/103: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82S102/103: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER		TO	FROM	N82S102/103			S82S102/103			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
	Progagation delay									ns
T_{IA}	Input	Output	Input		20	35		20	55	
T_{CE}	Chip enable	Output	Chip enable		15	30		15	45	
	Disable time									ns
T_{CD}	Chip disable	Output	Chip enable		15	30		15	45	

NOTES

1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Test each output one at a time.
4. Measured with a programmed logic condition for which the output under test is at a low logic level. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic high at the output.
6. Measured with V_{IH} applied to $\overline{CE}$.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with the chip enable input grounded, all other inputs at 4.5V and the outputs open.

INTEGRATED FUSE LOGIC
SERIES 28

DESCRIPTION

The 82S105A is a bipolar programmable state machine of the Mealy type. It contains logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip State and Output registers. These consist respectively of 6 Q_P, and 8 Q_F edge triggered, clocked S/R flip-flops, with an asynchronous Preset option. All flip-flops are unconditionally preset to "1" during power turn on.

The AND array combines 16 external inputs $I_{0\text{-}15}$ with 6 internal inputs $P_{0\text{-}5}$ fed back from the State register to form up to 48 Transition terms (AND terms). All Transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the Low to High transition of the Clock pulse. Both True and Complement Transition terms can be generated by optional use of the internal input variable (C) from the Complement array. Also, if desired, the Preset input can be converted to Output-Enable function, as an additional user programmable option.

The device is available in commercial temperature range. For the commercial temperature range (0°C to +75°) specify N82S105A, F or N.

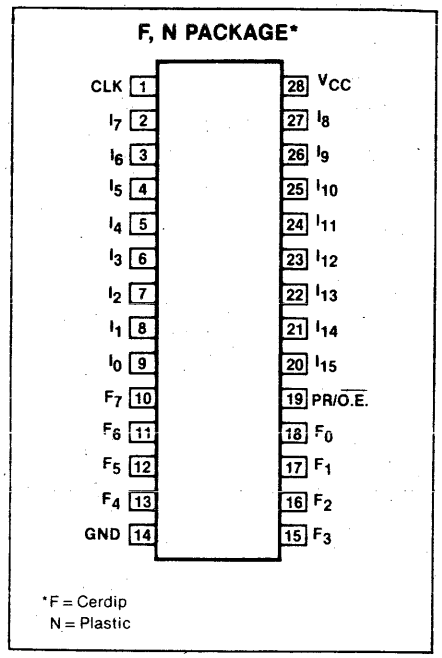
FEATURES

- **Field programmable (Ni-Cr link)**
- **16 input variables**
- **8 output functions**
- **48 transition terms**
- **6-bit state register**
- **8-bit output register**
- **Transition complement array**
- **Positive edge trigger clock**
- **Programmable asynchronous preset or output enable**
- **Power-on preset to all "1" of internal registers**
- **f(max) = 20MHz**
- **650mW power dissipation (typical)**
- **TTL compatible**
- **Single +5V supply**
- **Open collector and tri-state versions**
- **TRI-STATE outputs**

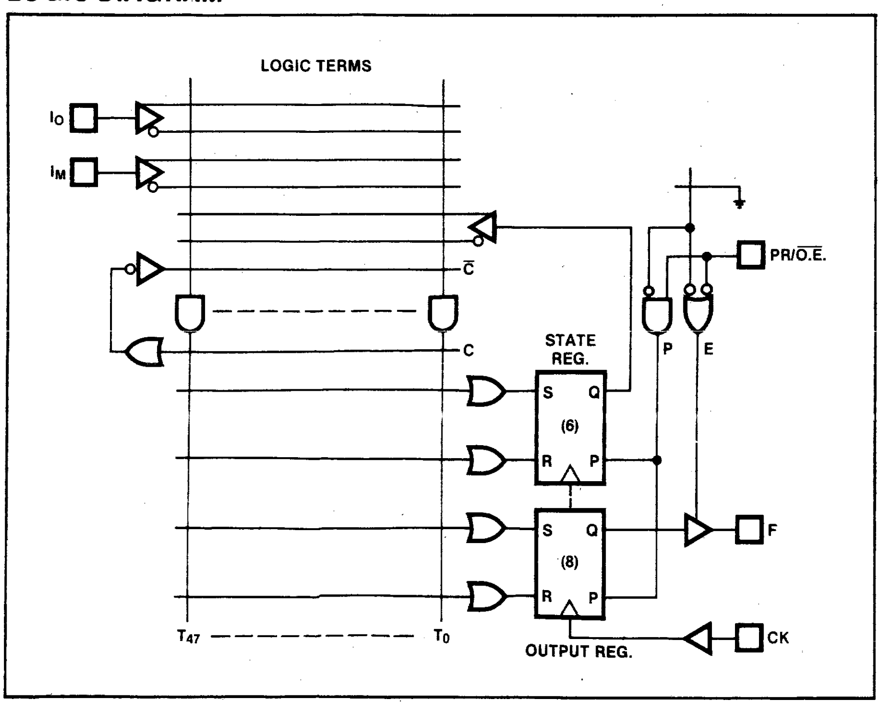
APPLICATIONS

- **Interface protocols**
- **Sequence detectors**
- **Peripheral controllers**
- **Timing generators**
- **Sequential circuits**
- **Elevator controllers**
- **Security locking systems**
- **Counters**
- **Shift registers**

PIN CONFIGURATION

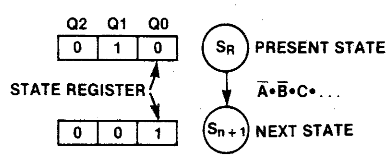


LOGIC DIAGRAM



LOGIC FUNCTION

Typical State Transition:



SET Q_0: $S_0 = (\bar{Q}_2 \cdot Q_1 \cdot \bar{Q}_0) \cdot \bar{A} \cdot \bar{B} \cdot C \ldots$
$R_0 = 0$

RESET Q_1: $S_1 = 0$
$R_1 = (\bar{Q}_2 \cdot Q_1 \cdot \bar{Q}_0) \cdot \bar{A} \cdot \bar{B} \cdot C \ldots$

HOLD Q_2: $S_2 = 0$
$R_2 = 0$

FIELD PROGRAMMABLE LOGIC SEQUENCER (16×48×8)

82S105A (T.S.)

INTEGRATED FUSE LOGIC
SERIES 28

ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING Min	RATING Max	UNIT
V_{CC}	Supply voltage		+7	Vdc
V_{IN}	Input voltage		+5.5	Vdc
V_{OUT}	Output voltage		+5.5	Vdc
I_{IN}	Input currents	−30	+30	mA
I_{OUT}	Output currents		+100	mA
	Temperature range			°C
T_A	Operating	0	+75	
T_{STG}	Storage	−65	+150	
T_{SDO}	Simultaneous Terms/OR[10]		4	

THERMAL RATINGS

TEMPERATURE	MILITARY	COMMERCIAL
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

	PARAMETER	TEST CONDITIONS	N82S105A Min	N82S105A Typ[2]	N82S105A Max	UNIT
	Input voltage[3]					V
V_{IH}	High	V_{CC} = Max	2			
V_{IL}	Low	V_{CC} = Min			0.8	
V_{IC}	Clamp[4]	V_{CC} = Min, I_{IN} = −12mA		−0.8	−1.2	
	Output voltage[3]	V_{CC} = Min				V
V_{OH}	High[5]	I_{OH} = −2mA	2.4			
V_{OL}	Low[6]	I_{OL} = 9.6mA		0.35	0.45	
	Input current					μA
I_{IH}	High	V_{IN} = 5.5V		<1	25	
I_{IL}	Low	V_{IN} = 0.45V		−10	−100	
I_{IL}	Low (CK input)	V_{IN} = 0.45V		−50	−250	
	Output current	V_{CC} = Max				
$I_{O(OFF)}$	Hi-Z state[7]	V_{OUT} = 5.5V		1	40	μA
		V_{OUT} = 0.45V		−1	−40	
I_{OS}	Short circuit[4,8]	V_{OUT} = 0V	−20		−70	mA
I_{CC}	V_{CC} supply current[9]	V_{CC} = Max		120	180	mA
	Capacitance[7]	V_{CC} = 5.0V				pF
C_{IN}	Input	V_{IN} = 2.0V		8		
C_{OUT}	Output	V_{OUT} = 2.0V		10		

NOTES
1. Stresses above those listed under "Absolute Maximum Ratings" may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured with V_{IL} applied to $\overline{O.E.}$ and a logic high stored, or with V_{IH} applied to PR.
6. Measured with a programmed logic condition for which the output is at a low logic level, and V_{IL} applied to PR/$\overline{O.E.}$. Output sink current is supplied through a resistor to V_{CC}.
7. Measured with V_{IH} applied to PR/$\overline{O.E.}$.
8. Duration of short circuit should not exceed 1 second.
9. I_{CC} is measured with the PR/$\overline{O.E.}$ input grounded, all other inputs at 4.5V and the outputs open.
10. See OR DRIVE limitations on page 9.

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$ $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

	PARAMETERS	TO	FROM	N82S105A			UNIT
				Min	Typ[1]	Max	
	Pulse width						ns
T_{CKH}	Clock high[2]	CK−	CK+	25	15		
T_{CKL}	Clock low	CK+	CK−	25	15		
T_{CKP1} B	Period (w/o c-array)	CK+	CK+	50	40		
T_{CKP2} B	Period (w/c-array)	CK+	CK+	80	50		
T_{PRH}	Preset pulse	PR+	PR−	25	15		
	Set-up time[3]						ns
T_{IS1} A	Input	CK+	Input ±	40			
T_{IS1} B	Input	CK+	Input ±	30			
T_{IS2} A	Input (through Complement array)	CK+	Input ±	70			
T_{IS2} B	Input (through Complement array)	CK+	Input ±	60			
T_{VS}	Power-on preset	CK−	V_{CC} +	0	−10		
T_{PRS}	Preset	CK−	PRS−	0	−10		
	Hold time						ns
T_{IH}	Input	Input ±	CK+	5	−10		
	Propagation delay						ns
T_{CKO}	Clock	Output ±	CK+		15	20	
T_{OE}	Output enable	Output −	$\overline{O.E.}$ −		20	30	
T_{OD}	Output disable	Output +	$\overline{O.E.}$ +		20	30	
T_{PR}	Preset	Output +	PR+		18	30	
T_{PPR}	Power-on preset	Output +	V_{CC} +		0	10	
	Frequency of operation						MHz
f_{MAX} B	w/o c-array					20	
f_{MAX} B	w/c-array					12.5	

NOTES:
1. All typical values are at $V_{CC} \pm 5V$, $T_A = 25°C$.
2. To prevent spurious clocking, clock rise time (10%-90%) ≤ 30ns.
3. See "Speed vs. OR Loading" on page 9.

Signetics

MEMORY

256-BIT BIPOLAR RAM (256×1) 82LS16 (T.S.)/82LS17 (O.C.)

DESCRIPTION

The 82LS16 and 82LS17 are Read/Write memory arrays which feature either open collector or 3-state output options for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and PNP input transistors which reduce input loading.

During Write operation, the logical state of the output of both devices follows the complement of the data input being written. This feature allows faster execution of Write/Read cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following a Write cycle.

Both devices have fast Read access and Write cycle times, as well as low power requirements and thus are ideally suited in high-speed memory applications such as cache, buffers, scratch pads, writable control stores, where power limitations are of major concern.

Both devices are available in the commercial temperature range (0°C to +75°C) and the military temperature range (−55°C to +125°C). They are specified as: N82LS16F or N or N82LS17F or N for the commercial temperature range, and S82LS16F, G, or W or S82LS17F, G, or W for the military temperature range. Military products are available as fully processed to Mil-Std 883 Level B or Level C; specify either 883B or 883C.

See page 4-9 for Truth Table, Timing Diagrams, Test Circuit and Waveform.

FEATURES

- **Address access time:**
  N82LS16/17: 40ns max
  S82LS16/17: 60ns max
- **Write cycle time:**
  N82LS16/17: 40ns max
  S82LS16/17: 65ns max
- **Power dissipation: 0.98mW/bit typ**
- **Input loading:**
  N82LS16/17: −100μA max
  S82LS16/17: −250μA max
- **Output follows complement of data input during Write**
- **On-chip address decoding**
- **Output option:**
  82LS16 3-state
  82LS17 Open collector
- **Schottky clamped**
- **TTL compatible**

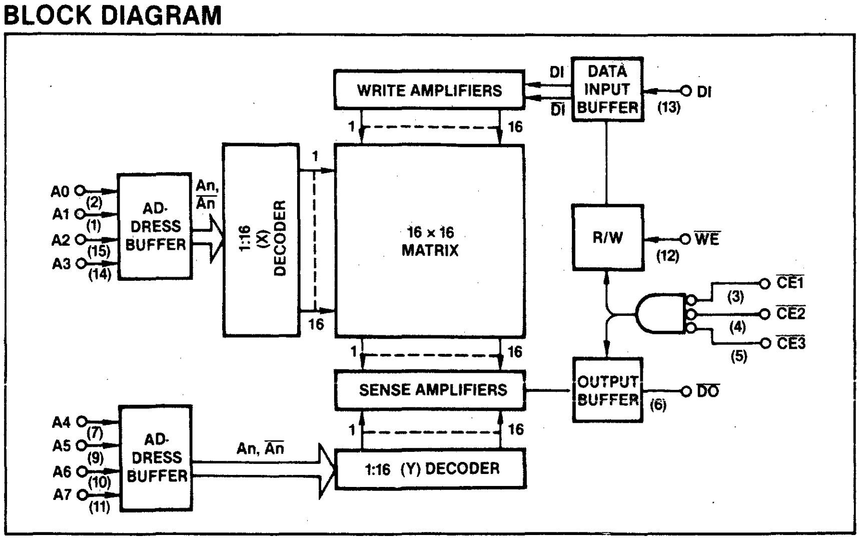
APPLICATIONS

- **Buffer memory**
- **Writable control store**
- **Memory mapping**
- **Push down stack**
- **Scratch pad**

ABSOLUTE MAXIMUM RATINGS

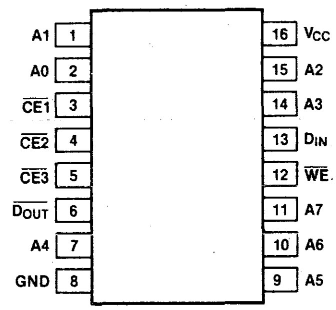
	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OUT}	High (open collector)	+5.5	
	Temperature Range		
T_A	Operating		°C
	N grade	0 to +70	
	S grade	−55 to +125	
T_{STG}	Storage	−65 to +150	°C

BLOCK DIAGRAM



PIN CONFIGURATIONS

F, N, W PACKAGE

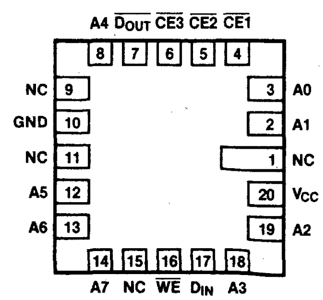


TOP VIEW

Order Numbers:
N82LS16F or N82LS16N
N82LS17F or N82LS17N
S82LS16F or S82LS16W
S82LS17F or S82LS17W

F = Cerdip
N = Plastic
W = Flat Pak

G PACKAGE



TOP VIEW

Order Numbers:
S82LS16G or S82LS17G

G = Leadless

DC ELECTRICAL CHARACTERISTICS

N82LS16/17: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82LS16/17: −55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

	PARAMETER	TEST CONDITIONS	N82LS16/17			S82LS16/17			UNIT
			Min	Typ[1]	Max	Min	Typ[1]	Max	
	Input voltage[2]								V
V_{IH}	High	V_{CC} = max	2.0			2.0			
V_{IL}	Low	V_{CC} = min			0.8			0.8	
V_{IC}	Clamp[3]	V_{CC} = min, I_{IN} = −12mA		−1.0	−1.5		−1.0	−1.5	
	Output voltage[2]	V_{CC} = min							V
V_{OH}	High (82LS16)[4]	I_{OH} = −3.2mA	2.6			2.4			
V_{OL}	Low[5]	I_{OL} = 16mA		0.35	0.45		0.35	0.5	
	Input current[3]	V_{CC} = max							μA
I_{IH}	High	V_{IN} = 5.5V		1	25		1	25	
I_{IL}	Low	V_{IN} = 0.45V		−10	−100		−10	−250	
	Output current								μA
I_{OLK}	Leakage (82LS17)[5]	V_{OUT} = 5.5V		1	40		1	40	
I_{OZ}	Hi-Z state (82LS16)[6]	V_{OUT} = 5.5V		1	40		1	50	
		V_{OUT} = 0.45V		−1	−40		−1	−50	
I_{OS}	Short circuit (82LS16)[7]	V_{CC} = max, V_O = 0V	−15		−70	−15		−70	
I_{CC}	V_{CC} supply current[8]	V_{CC} = max		50	70		50	100	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

R1 = 270Ω, R2 = 600Ω, C_L = 30pF
N82LS16/17: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82LS16/17: −55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

	PARAMETER	TO	FROM	N82LS16/17			S82LS16/17			UNIT
				Min	Typ[1]	Max	Min	Typ[1]	Max	
	Access time									ns
T_{AA}	Address	Output	Address		30	40		30	70	
T_{CE}	Chip enable	Output	Chip enable		15	25		15	40	
T_{CD}	Disable time	Output	Chip enable		15	25		15	40	ns
T_{WD}	Valid time	Output	Write enable		30	40		30	55	ns
	Setup and hold time									ns
T_{WSA}	Setup time	Write enable	Address	0	−5		10	−5		
T_{WHA}	Hold time	Write enable	Address	0	−5		10	−5		
T_{WSD}	Setup time	Write enable	Data in	25	15		40	15		
T_{WHD}	Hold time	Write enable	Data in	0	−5		10	−5		
T_{WSC}	Setup time	Write enable	$\overline{CE}$	0	−5		10	−5		
T_{WHC}	Hold time	Write enable	$\overline{CE}$	0	−5		10	−5		
	Pulse width									ns
T_{WP}	Write enable[9]			25	15		40	15		

NOTES

1. All typical values are at V_{CC} = 5V, T_A + 25°C.
2. All voltage values are with respect to network ground terminal.
3. Test each input one at a time.
4. Measured with a logic low stored and V_{IL} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
5. Measured with a logic high stored. Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IH} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
7. Duration of the short-circuit should not exceed 1 second.
8. I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
9. Minimum required to guarantee a Write into the slowest bit.

2304-BIT BIPOLAR RAM (256×9) 82S212A (T.S.)

DESCRIPTION

The organization of the 82S212A allows byte wide storage of data, including parity. Where parity is not required, the ninth bit can be used as a tag for each word stored. The 82S212A is ideal for scratch-pad, push-down stacks, buffer memories, and other internal memory applications in which space and performance requirements dictate a wide data path in favor of word depth.

The 82S212A data inputs and outputs are common (common I/O) with separate output disable (OD) line that allows ease of read/write operations using a common bus.

The 82S212A is available in the commercial temperature range. For the commercial temperature range (0°C to 75°C) specify N82S212AF or N.

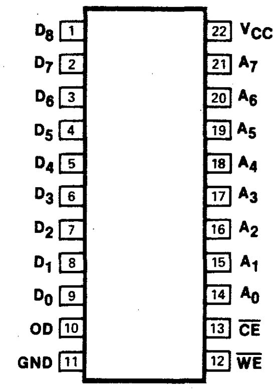
FEATURES

- **Address access time:**
  N82S212A: 35ns max
- **Power dissipation: 0.3mW/bit**
- **Tri-state outputs**
- **Schottky clamped TTL**

APPLICATIONS

- **Cache memory**
- **Buffer storage**
- **Writable control store**

PIN CONFIGURATION



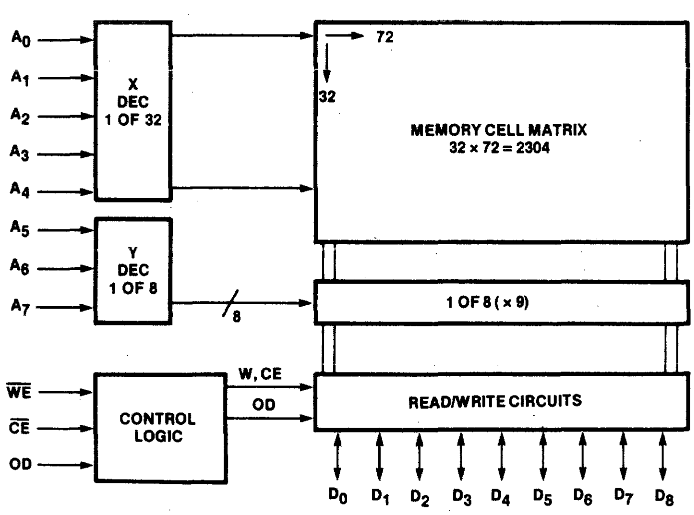
*F = Cerdip
N = Plastic

TRUTH TABLE

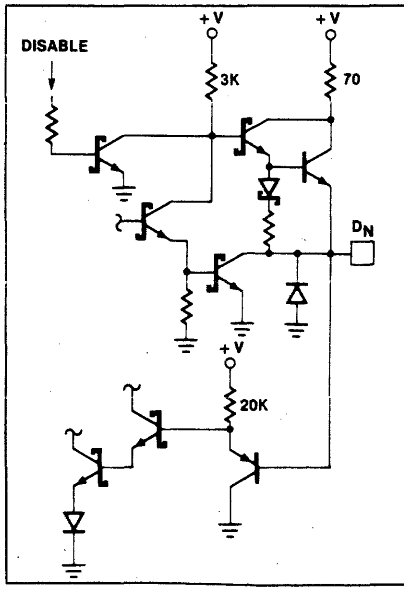
MODE	$\overline{WE}$	$\overline{CE}$	OD	D_N IN/OUT
Disable output	X	X	1	High Z
Disable R/W	X	1	X	High Z
Write	0	0	1	Data in
Read	1	0	0	Data out

X = Don't care

BLOCK DIAGRAM



TYPICAL I/O STRUCTURE



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
V_O	Off-state output voltage	+5.5	Vdc
	Temperature range		°C
T_A	Operating	0 to +75	
T_{STG}	Storage	−65 to +150	

DC ELECTRICAL CHARACTERISTICS[1] N82S212A: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER		TEST CONDITIONS	N82S212A Min	Typ	Max	UNIT
	Input voltage					V
V_{IL}	Low	V_{CC} = Min			0.8	
V_{IH}	High	V_{CC} = Max	2.0			
V_{IC}	Clamp[2]	V_{CC} = Min, I_{IN} = −12mA			−1.5	
	Output voltage					V
V_{OL}	Low[3]	V_{CC} = Min, I_{OL} = 8.0mA			0.5	
V_{OH}	High	I_{OH} = −2mA	2.4			
	Input current					μA
I_{IL}	Low	V_{IN} = 0.45V			−100	
I_{IH}	High	V_{IN} = 5.5V			25	
	Output current					
I_{OZ}	Hi-Z state	$\overline{CE}$ = High or OD = High, V_{OUT} = 5.5V			40	μA
		$\overline{CE}$ = High or OD = High, V_{OUT} = 0.5V			−100	
I_{OS}	Short circuit[4, 5]	$\overline{CE}$ = OD = Low, V_{OUT} = 0V	−15		−70	mA
I_{CC}	V_{CC} supply current	V_{CC} = Max		135	185	mA
	Capacitance	V_{CC} = 5.0V				pF
C_{IN}	Input	V_{IN} = 2.0V		5		
C_{OUT}	Output	V_{OUT} = 2.0V		8		

AC ELECTRICAL CHARACTERISTICS[1] R_1 = 470Ω, R_2 = 1kΩ, C_L = 30pF

N82S212A: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER		TO	FROM	N82S212A Min	Typ[3]	Max	UNIT
	Access time						ns
T_{AA}	Address	Output	Address			35	
	Enable time						ns
T_{OE}	Output	Output	OD			25	
T_{CE}	Output	Output	Chip enable			25	
	Disable time						ns
T_{OD}[6]	Output	Output	OD			25	
T_{CD}[6]	Output	Output	Chip enable			25	
	Pulse width						ns
T_{WP}	Write			25			
T_{WSC}	Setup time	Write	Chip enable	5			
T_{WHC}	Hold time	Chip enable	Write	5			
T_{WSD}	Setup time	Write	Data	25			
T_{WHD}	Hold Time	Data	Write	5			
T_{WSA}	Setup time	Write	Address	5			
T_{WHA}	Hold time	Address	Write	5			
T_{SO}	Setup time (from disabled state)	Chip enable	OD	50			
T_{HO}	Hold time	OD	Chip enable	50			

NOTES
1. The operating embient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2 minute warmup.
2. All voltages are with respect to network ground terminal.
3. All typical values are at V_{CC} = 5V, T_A = 25°C.
4. Measured on one pin at a time.
5. Duration of I_{OS} test should not exceed one second.
6. Measured at a delta of 0.5V from Logic Level with R_1 = 750Ω, R_2 = 750Ω and C_L = 5pF.

Signetics

MEMORY

256-BIT BIPOLAR PROM (32×8) 82S23A (O.C.)/82S123A (T.S.)

DESCRIPTION

The 82S23A and 82S123A are field programmable, which means that customer patterns are immediately available by following the fusing procedure given in this data manual. The 82S23A and 82S123A devices are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 1 chip enable input for memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S23A and 82S123A devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S23A/123A, N or F, and for the military temperature range (−55°C to +125°C) specify S82S23A/123A, F or W.

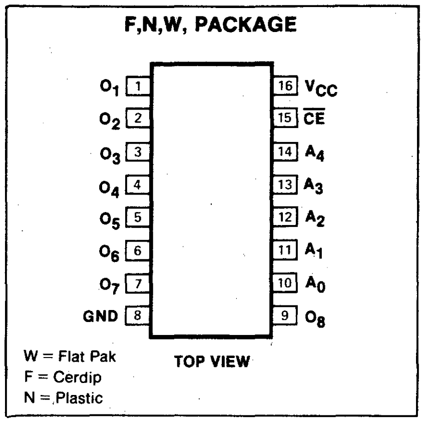
FEATURES

- **Address access time:**
  - **N82S23A/123A: 25ns max**
  - **S82S23A/123A: 35ns max**
- **Power dissipation: 1.3mW/bit typ**
- **Input loading:**
  - **N82S23A/123A: −100μA max**
  - **S82S23A/123A: −150μA max**
- **On-chip address decoding**
- **Output options:**
  - **82S23A: Open collector**
  - **82S123A: Tri-state**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

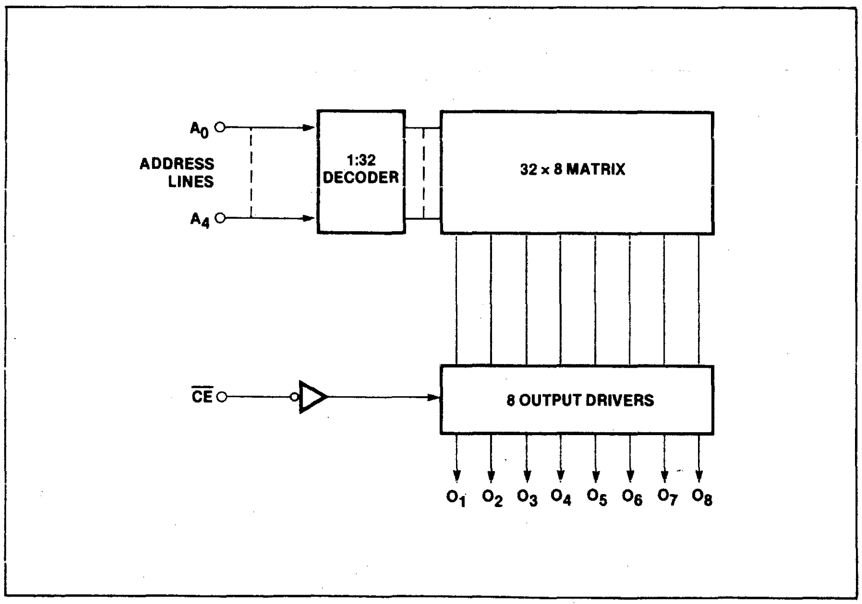
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Format conversion**
- **Hardwired algorithms**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S23)	+5.5	
V_O	Off-state (82S123)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S23A/123A	0 to +75	
	S82S23A/123A	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S23A/123A: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S23A/123A: −55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

	PARAMETER	TEST CONDITIONS[1,2]	N82S23A/123A			S82S23A/123A			UNIT
			Min	Typ[5]	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low				0.8			0.8	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = −12mA			-1.2			-1.2	
	Output voltage	$\overline{CE}$= Low							V
V_{OL}	Low	I_{OUT} = 16mA			0.45			0.5	
V_{OH}	High	I_{OUT} = -2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			50			50	
	Output current								
I_{OLK}	Leakage (82S23A)	$\overline{CE}$ = High, V_{OUT} = 5.5V			40			50	μA
I_{OZ}	Hi-Z state (82S123A)	$\overline{CE}$ = High, V_{OUT} = 5.5V			40			50	μA
		$\overline{CE}$ = High, V_{OUT} = 0.5V			-40			-50	
I_{OS}	Short circuit (82S123A)[3]	$\overline{CE}$ = Low, V_{OUT} = 0V, High stored	−15		-90	-20		-100	mA
I_{CC}	V_{CC} supply current	V_{CC} = Max			96			110	mA
	Capacitance	$\overline{CE}$ = High, V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

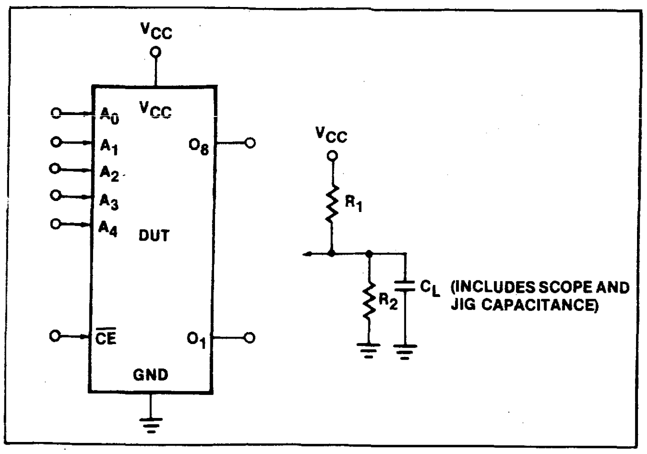
AC ELECTRICAL CHARACTERISTICS

R_1 = 270Ω, R_2 = 600Ω, C_L = 30pF
N82S23A/123A: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S23A/123A: −55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

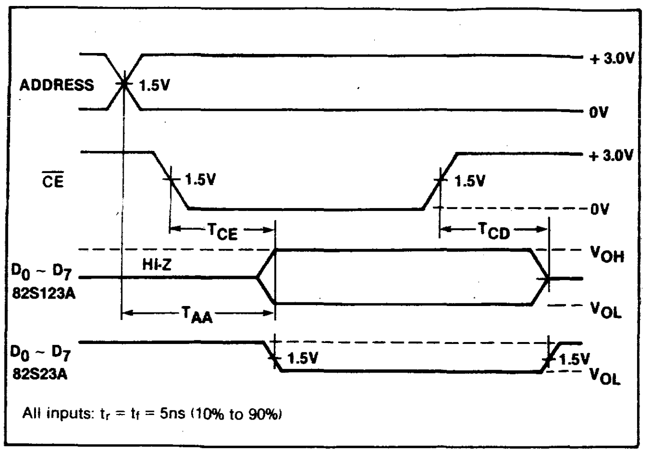
	PARAMETER	TO	FROM	N82S23A/123A			S82S23A/123A			UNIT
				Min	Typ[5]	Max	Min	Typ	Max	
	Access time									ns
T_{AA}[4]		Output	Address		20	25			35	
T_{CE}		Output	Chip enable			18			22	
	Disable time									ns
T_{CD}		Output	Chip disable			18			22	

NOTES
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μsec.
5. Typical values are at V_{CC} = 5V, T_A = 25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



1024-BIT BIPOLAR PROM (256×4)

82S126A (O.C.)/82S129A (T.S.)

DESCRIPTION

The 82S126A and 82S129A are field programmable, which means that customer patterns are immediately available by following the fusing procedure given in this data manual. The 82S126A and 82S129A devices are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 2 chip enable input for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S126A and 82S129A devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S126A/129A, F or N, and for the military temperature range (−55°C to +125°C) specify S82S126A/129A, F or R.

FEATURES

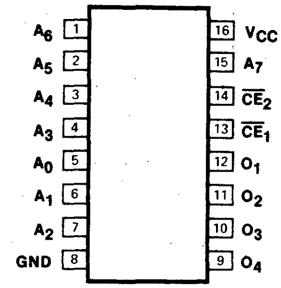
- **Address access time:**
  - **N82S126A: 30ns max**
  - **N82S129A: 27ns max**
  - **S82S126A/129A: 35ns max**
- **Power dissipation: 0.5mW/bit typ**
- **Input loading:**
  - **N82S126A/129A: −100μA max**
  - **S82S126A/129A: −150μA max**
- **On-chip address decoding**
- **Output options:**
  - **82S126A: Open collector**
  - **82S129A: Tri-state**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION

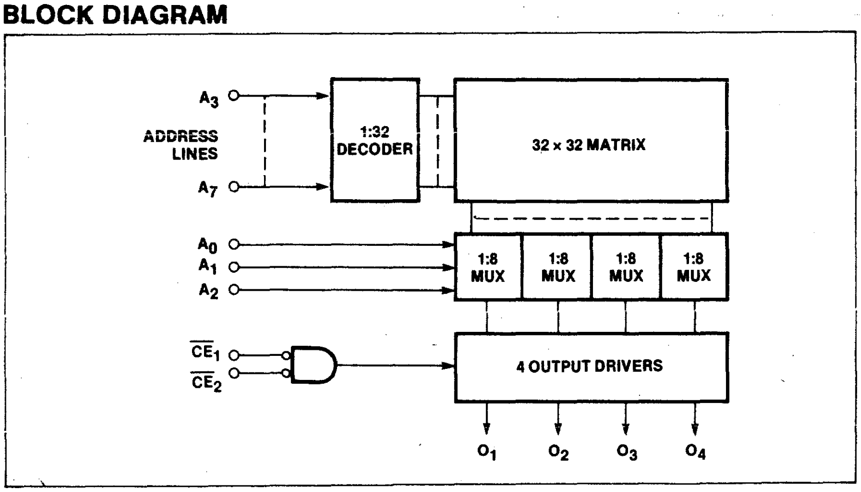
F,N,R PACKAGE*



*F = Cerdip
N = Plastic
R = Flat Pak

TOP VIEW

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S126)	+5.5	
V_O	Off-state (82S129)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S126A/129A	0 to +75	
	S82S126A/129A	-55 to +125	
T_{STG}	Storage	-65 to +150	

1024-BIT BIPOLAR PROM (256×4) 82S126A (O.C.)/82S129A (T.S.)

DC ELECTRICAL CHARACTERISTICS

N82S126A/129A: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S126A/129A: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1, 2]	N82S126A/129A			S82S126A/129A			UNIT
			Min	Typ[5]	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low				0.8			0.8	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	$I_{IN} = -12mA$			-1.2			-1.2	
	Output voltage	$\overline{CE}_{1,2}$ = Low							V
V_{OL}	Low	I_{OUT} = 16mA			0.45			0.5	
V_{OH}	High (82S129)	I_{OUT} = -2.0mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								
I_{OLK}	Leakage (82S126A)	$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_{OUT} = 5.5V			40			60	μA
I_{OZ}	Hi-Z state (82S129A)	$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_{OUT} = 5.5V			40			60	μA
		$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_{OUT} = 0.5V			-40			-60	
I_{OS}	Short circuit (82S129A)[3]	$\overline{CE}_{1,2}$ = Low, V_{OUT} = 0V, Stored high	-15		-70	-15		-85	mA
I_{CC}	V_{CC} supply current	V_{CC} = Max			120			125	mA
	Capacitance	CE_1 or CE_2 = High V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

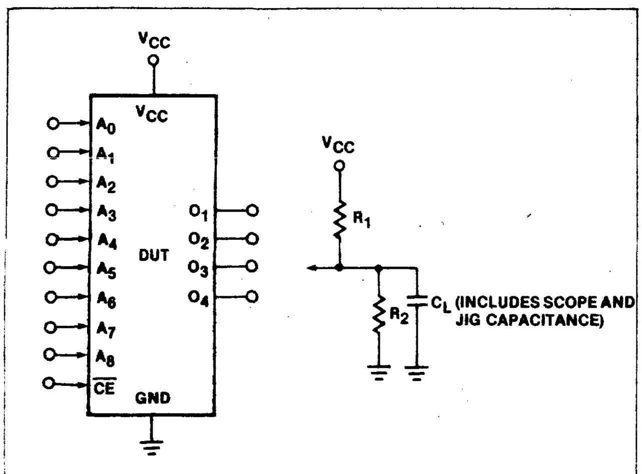
AC ELECTRICAL CHARACTERISTICS

$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$
N82S126A/129A: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S126A/129A: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

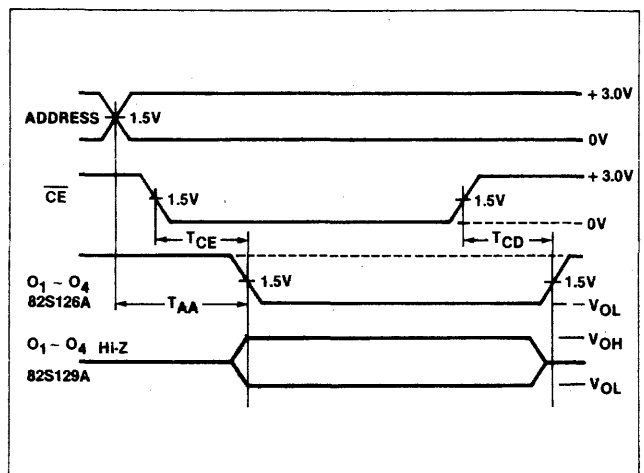
PARAMETER		TO	FROM	N82S129A			N82S126A			S82S126A 82S129A			UNIT
				Min	Typ[5]	Max	Min	Typ[5]	Max	Min	Typ	Max	
T_{AA}	Address access[4]	Output	Address		17	27		17	30			35	ns
T_{CE}	Enable access	Output	Chip enable		10	20		10	20			20	ns
T_{CD}	Output disable	Output	Chip enable		6	15		6	15			15	ns

NOTES
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μsec.
5. Typical values are at V_{CC} = 5V, T_A = 25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



2048-BIT BIPOLAR PROM (512×4)

82S130A (O.C.)/82S131A (T.S.)

DESCRIPTION

The 82S130A and 82S131A are field programmable, which means that customer patterns are immediately available by following the fusing procedure given in this data manual. The standard 82S130A and 82S131A are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 1 chip enable input for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S130A and 82S131A devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S130A/131A, F or N, and for the military temperature range (−55°C to +125°C) specify S82S130A/131A, F or R.

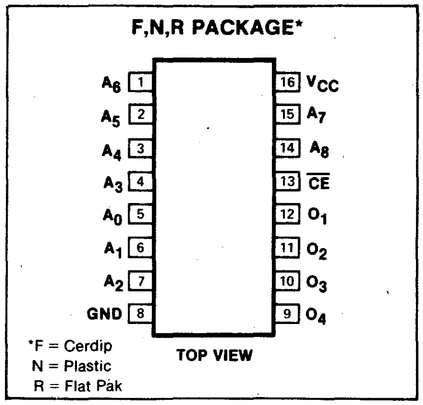
FEATURES

- **Address access time:**
  - **N82S130A: 33ns max**
  - **N82S131A: 30ns max**
  - **S82S130A/131A: 35ns max**
- **Power dissipation: 0.3mW/bit typ**
- **Input loading:**
  - **N82S130A/131A: −100μA max**
  - **S82S130A/131A: −150μA max**
- **On-chip address decoding**
- **Output options:**
  - **82S130A: Open collector**
  - **82S131A: Tri-state**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

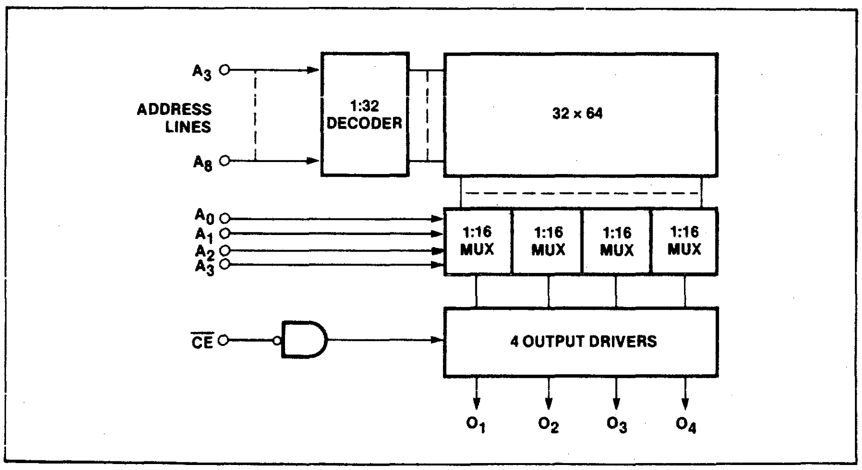
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S130)	+5.5	
V_O	Off-state (82S131)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S130A/131A	0 to +75	
	S82S130A/131A	-55 to +125	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S130A/131A: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S130A/131A: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1, 2]	N82S130A/131A			S82S130A/131A			UNIT
			Min	Typ[5]	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low				0.8			0.8	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	$I_{IN} = -12mA$			-1.2			-1.2	
	Output voltage	$\overline{CE}$ = Low							V
V_{OL}	Low	$I_{OUT} = 16mA$			0.45			0.5	
V_{OH}	High (82S131)	$I_{OUT} = -2mA$	2.4			2.4			
	Input current								μA
I_{IL}	Low	$V_{IN} = 0.45V$			-100			-150	
I_{IH}	High	$V_{IN} = 5.5V$			40			50	
	Output current								
I_{OLK}	Leakage (82S130A)	$\overline{CE}$ = high, $V_{OUT} = 5.5V$			40			60	μA
I_{OZ}	Hi-Z state (82S131A)	$\overline{CE}$ = high, $V_{OUT} = 5.5V$			40			60	μA
		$\overline{CE}$ = high, $V_{OUT} = 0.5V$			-40			-60	
I_{OS}	Short circuit (82S131A)[3]	$\overline{CE}$ = Low, $V_{OUT} = 0V$, Stored high	−15		-70	-15		-85	mA
I_{CC}	V_{CC} supply current	V_{CC} = Max			140			140	mA
	Capacitance	$\overline{CE}$ = High, $V_{CC} = 5.0V$							pF
C_{IN}	Input	$V_{IN} = 2.0V$		5			5		
C_{OUT}	Output	$V_{OUT} = 2.0V$		8			8		

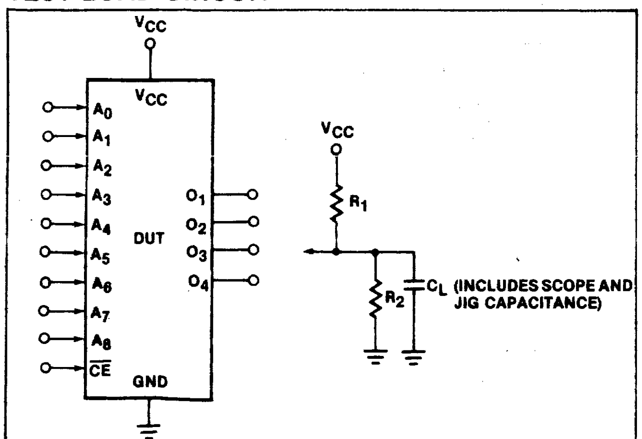
AC ELECTRICAL CHARACTERISTICS

$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$
N82S130A/131A: $0° \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S130A/131A: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TO	FROM	N82S131A			N82S130A			S82S130A N82S131A			UNIT
				Min	Typ[5]	Max	Min	Typ[5]	Max	Min	Typ	Max	
T_{AA}	Address access[4]	Output	Address		18	30		18	33			35	ns
T_{CE}	Enable access	Output	Chip enable		10	20		10	20			20	ns
T_{CD}	Output disable	Output	Chip enable		6	15		6	15			15	ns

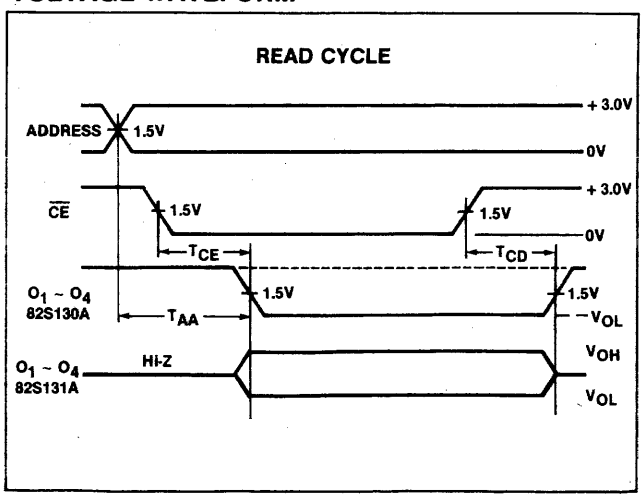
NOTES
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μsec.
5. Typical values are at $V_{CC} = 5V$, $T_A = 25°C$.

TEST LOAD CIRCUIT



All inputs: tr = tf = 5ns (10% to 90%)

VOLTAGE WAVEFORM



Signetics

MEMORY

2048-BIT BIPOLAR PROM (256×8) 82LS135 (T.S.)

DESCRIPTION

The 82LS135 is field-programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The standard devices are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

The 82LS135 includes on-chip decoding and two chip enable inputs for ease of memory expansion, and features tri-state outputs for optimization of word expansion in bused organizations.

The 82LS135 device is available in the commercial temperature range (0°C to 75°C), and is specified as N82LS135F or N.

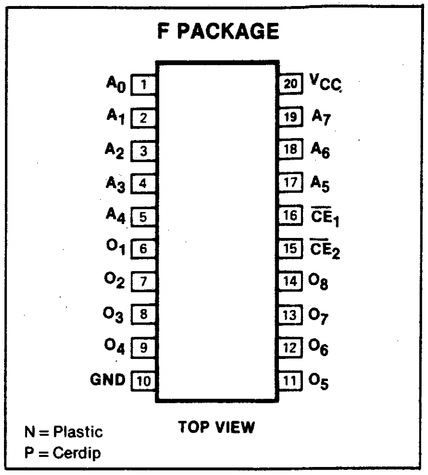
FEATURES

- **Address access time: 100ns max.**
- **Power dissipation: 200μW/bit typ**
- **Input loading: -100μA max**
- **Two chip enable inputs**
- **On chip address decoding**
- **No separate fusing pins**
- **Fully TTL compatible**

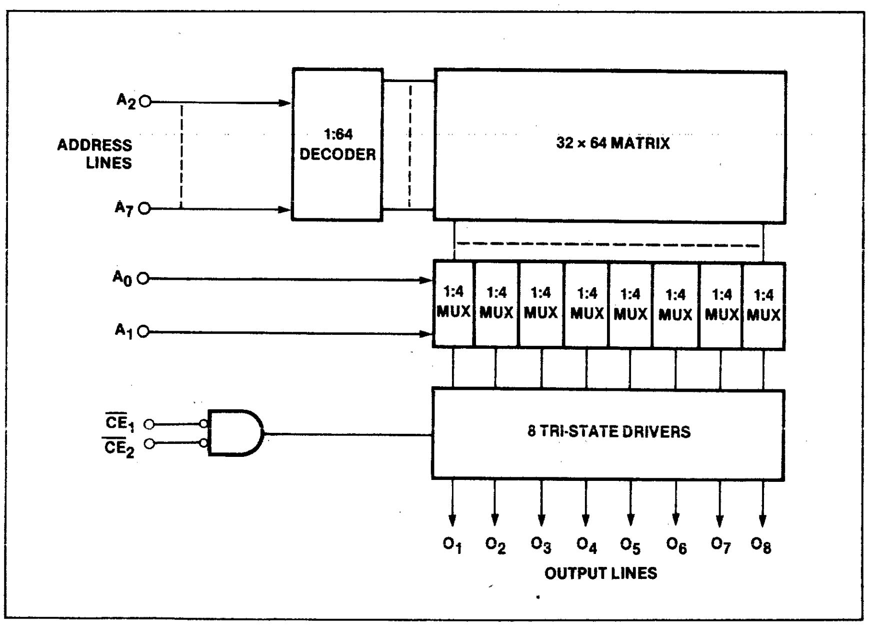
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_O	Off-state	+5.5	Vdc
	Temperature range		°C
T_A	Operating	−40 to +85	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

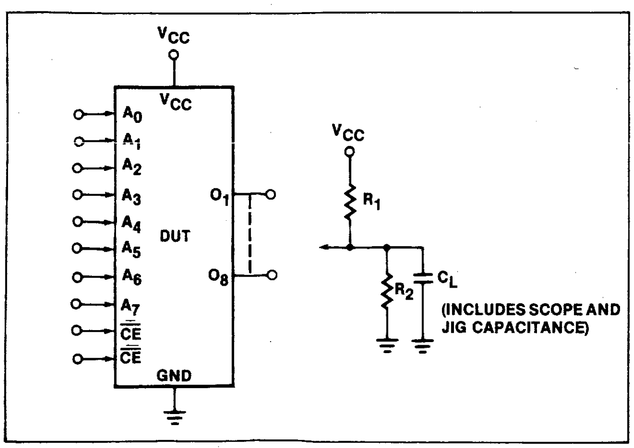
PARAMETER		TEST CONDITIONS[1,2]	LIMITS Min	Typ[5]	Max	UNIT
	Input voltage					V
V_{IL}	Low				.80	
V_{IH}	High		2.0			
V_{IC}	Clamp	$I_{IN} = -12mA$			-1.2	
	Output voltage					V
V_{OL}	Low	$I_{OUT} = 16mA$			.50	
V_{OH}	High	$\overline{CE}_1$, $\overline{CE}_2$ = Low, $I_{OUT} = -2mA$, High stored	2.4			
	Input current					µA
I_{IL}	Low	$V_{IN} = 0.45V$			-100	
I_{IH}	High	$V_{IN} = 5.5V$			40	
	Output current					
I_{OLK}	Leakage	$\overline{CE}_1$, $\overline{CE}_2$ = High, $V_{OUT} = 5.5V$			40	µA
I_{OZ}	Hi-Z state	$\overline{CE}_1$, $\overline{CE}_2$ = High, $V_{OUT} = 0.5V$			-40	µA
		$\overline{CE}_1$, $\overline{CE}_2$ = High, $V_{OUT} = 5.5V$			40	
I_{OS}	Short circuit[3]	$V_{OUT} = 0V$	−15		−75	mA
I_{CC}	V_{CC} supply current	V_{CC} = Max		80	100	mA
	Capacitance	$V_{CC} = 5.0V$ $\overline{CE}$ = High				pF
C_{IN}	Input	$V_{IN} = 2.0V$		5		
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		

AC ELECTRICAL CHARACTERISTICS $R_1 = 10 k\Omega$, $R_2 = 20 k\Omega$, $C_L = 90 pF$, $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

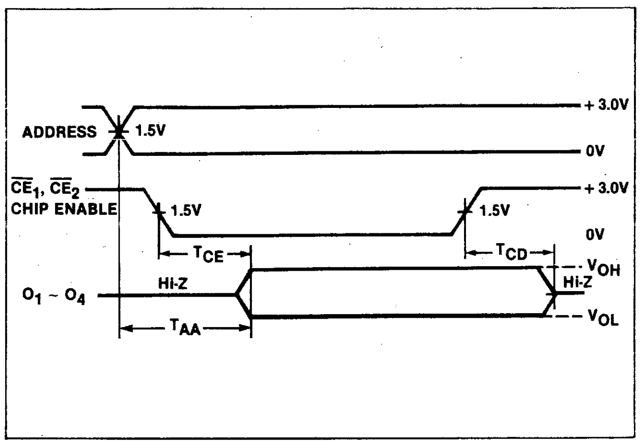
PARAMETER		TO	FROM	LIMITS Min	Typ[5]	Max	UNIT
	Access time						ns
T_{AA}[4]		Output	Address		70	100	
T_{CE}		Output	Chip enable		30	50	
T_{CD}	Disable time	Output	Chip disable		30	50	ns

NOTES
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1µsec.
5. Typical values are at $V_{CC} = 5V$, $T_A = 25°C$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



Signetics

MEMORY

4096-BIT BIPOLAR PROM (1024×4)

82S137A/82S137B (T.S.)

DESCRIPTION

The 82S137 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The 82S137 is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 2 chip enable inputs for ease of memory expansion. They feature tri-state outputs for optimization of word expansion in bused organizations.

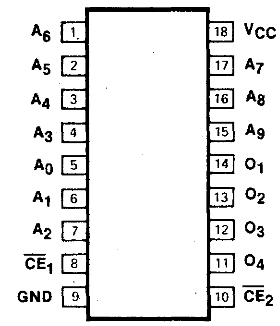
The 82S137 device is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S137AF or N, or N82S137BF or N, and for the military temperature range (−55°C to +125°C) specify S82S137AF or R.

FEATURES

- **Address access time:**
  - **N82S137A: 45ns max**
  - **N82S137B: 35ns max**
  - **S82S137A: 70ns max**
- **Power dissipation: 13mW/bit typ**
- **Input loading:**
  - **N82S137: −100μA max**
  - **S82S137: −150μA max**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

PIN CONFIGURATION

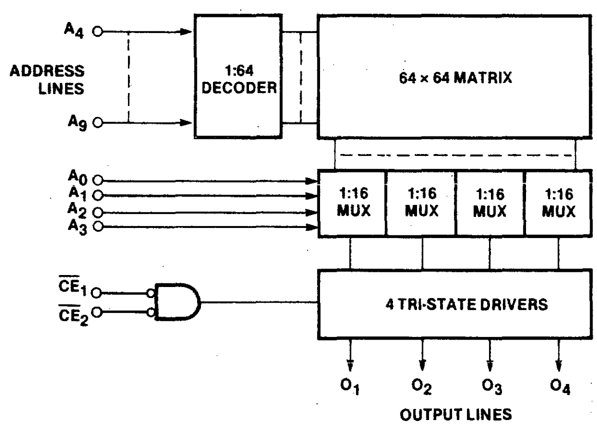
F,N,R PACKAGE*



TOP VIEW

*F = Cerdip
N = Plastic
R = Flat Pak

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_O	Off-state	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S137	0 to +75	
	S82S137	−55 to +125	
T_{STG}	Storage	−65 to +150	

4096-BIT BIPOLAR PROM (1024×4) — 82S137A/82S137B (T.S.)

DC ELECTRICAL CHARACTERISTICS

N82S137A/N82S137B: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S137A: −55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TEST CONDITIONS[1,2]	N82S137A/N82S137B			S82S137A			UNIT
			Min	Typ[5]	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low				0.8			0.8	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = −12mA		−0.8	−1.2			−1.2	
	Output voltage	$\overline{CE}_{1,2}$ = Low							V
V_{OL}	Low	I_{OUT} = 16mA			0.45			0.5	
V_{OH}	High	I_{OUT} = −2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			−100			−150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								
I_{OZ}	Hi-Z state	$\overline{CE}_{1,2}$ = High, V_{OUT} = 0.5V			40			60	μA
		$\overline{CE}_{1,2}$ = High, V_{OUT} = 5.5V			−40			−60	μA
I_{OS}	Short circuit[3]	$\overline{CE}_{1,2}$ = Low, V_{OUT} = 0V, Stored High	−15		−70	−15		−85	mA
I_{CC}	V_{CC} supply current	V_{CC} = Max		85	140			150	mA
	Capacitance	$\overline{CE}_{1,2}$ = High, V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

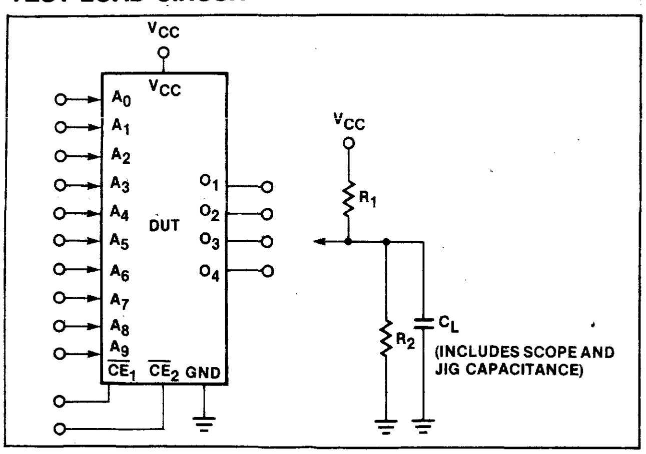
AC ELECTRICAL CHARACTERISTICS

R_1 = 270Ω, R_2 = 600Ω, C_L = 30pF
N82S137A/N82S137B: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S137A: −55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

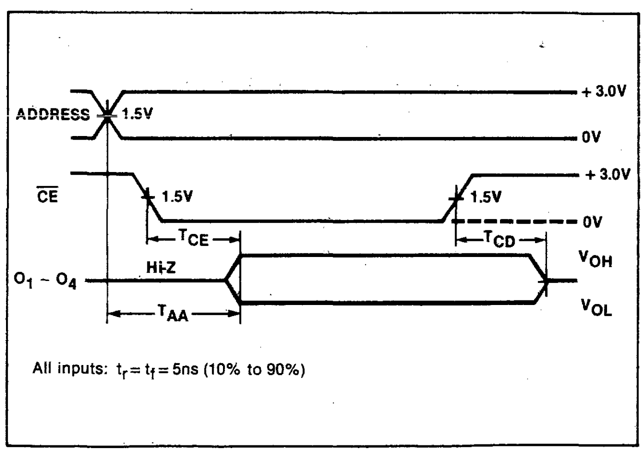
PARAMETER		TO	FROM	N82S137A			N82S137B			S82S137A			UNIT
				Min	Typ[5]	Max	Min	Typ	Max	Min	Typ	Max	
T_{AA}[4]	Access time	Output	Address		35	45		30	35			70	ns
T_{CE}		Output	Chip enable		15	30			25			40	ns
T_{CD}	Disable time	Output	Chip disable		15	30			25			40	ns

NOTES
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μsec.
5. Typical values are at V_{CC} = 5V, T_A = 25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



4096-BIT BIPOLAR PROM (512×8)

82S147A (T.S.)

DESCRIPTION

The 82S147A is field-programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The standard devices are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

The 82S147A includes on-chip decoding and one chip enable input for ease of memory expansion, and features tri-state outputs for optimization of word expansion in bused organizations.

The 82S147A device is available in the commercial temperature range (0°C to +75°C), and is specified as N82S147A, F or N.

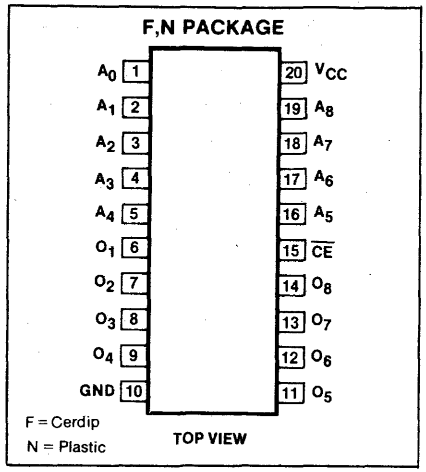
FEATURES

- **Address access time: 45ns max**
- **Power dissipation: 853mW max**
- **Input loading: −100µA max**
- **One chip enable input**
- **On chip address decoding**
- **No separate fusing pins**
- **Fully TTL compatible**

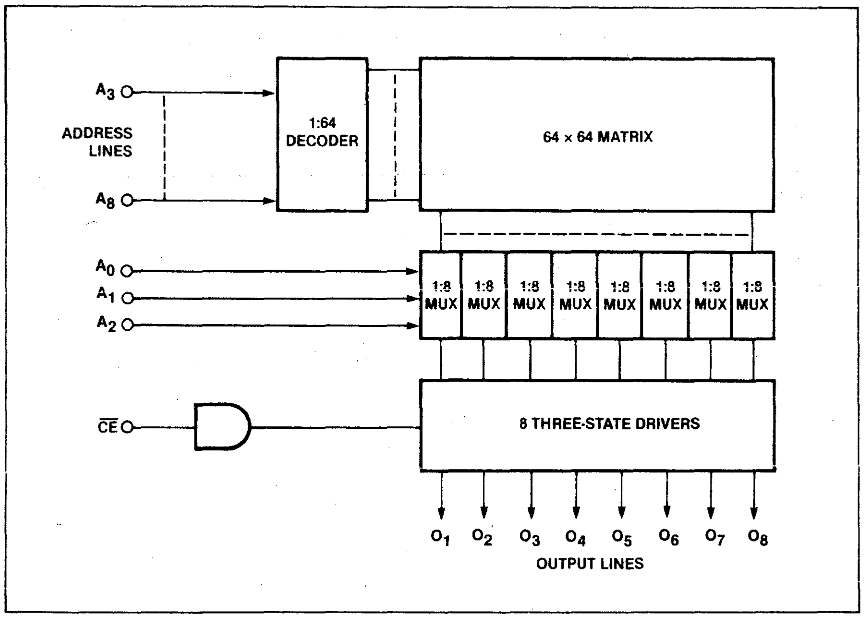
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_O	Off-state	+5.5	Vdc
	Temperature range		°C
T_A	Operating	0 to +75	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS

N82S147A: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S147: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITION[1, 2]	N82S147A			S82S147A			UNIT
			Min	Typ[5]	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low				0.8			0.8	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	$I_{IN} = -12mA$		−0.8	−1.2			−1.2	
	Output voltage	$\overline{CE}$ = Low							V
V_{OL}	Low	$I_{OUT} = 9.6mA$			0.45			0.5	
V_{OH}	High	$I_{OUT} = -2mA$	2.4			2.4			
	Input current								μA
I_{IL}	Low	$V_{IN} = 0.45V$			−100			−150	
I_{IH}	High	$V_{IN} = 5.5V$			40			50	
	Output current								
I_{OZ}	Hi-Z state	$\overline{CE}$ = High, $V_{OUT} = 5.5V$			40			−60	μA
		$\overline{CE}$ = High, $V_{OUT} = 0.5V$			−40			60	μA
I_{OS}	Short circuit[3]	$\overline{CE}$ = Low, $V_{OUT} = 0V$	−15		−70	−15		−85	mA
I_{CC}	V_{CC} supply current	V_{CC} = Max		125	155			165	mA
	Capacitance	$\overline{CE}$ = High, $V_{CC} = 5.0V$							pF
C_{IN}	Input	$V_{IN} = 2.0V$		5			5		
C_{OUT}	Output	$V_{OUT} = 2.0V$		8			8		

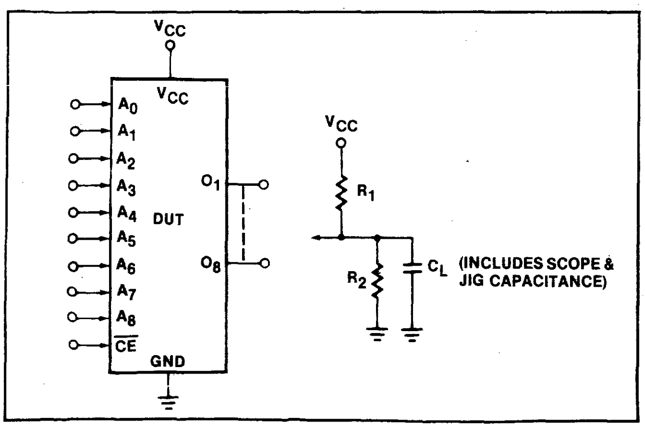
AC ELECTRICAL CHARACTERISTICS

$R1 = 470\Omega$, $R2 = 1k\Omega$, $C_L = 30pF$
N82S147A: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S147A: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

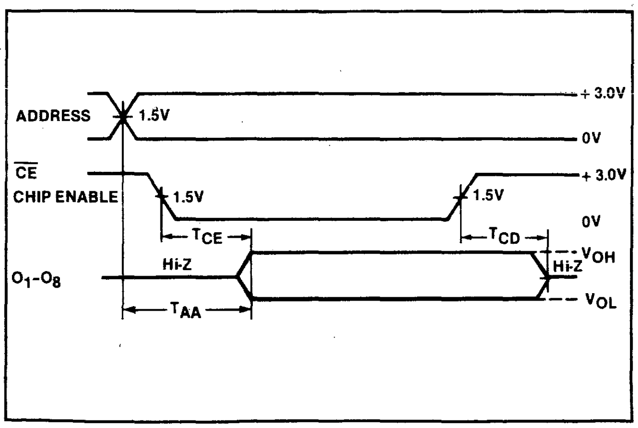
PARAMETER		TO	FROM	N82S147A			S82S147A			UNIT
				Min	Typ[5]	Max	Min	Typ	Max	
	Access time									ns
T_{AA}[4]		Output	Address		45	45			60	
T_{CE}		Output	Chip enable		20	30			35	
	Disable time									ns
T_{CD}		Output	Chip disable		20	30			35	

NOTES
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μsec.
5. Typical values are at $V_{CC} = 5V$, $T_A = 25°C$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



8192-BIT BIPOLAR PROM (1024×8)

82S181A/82S181B (T.S.)

DESCRIPTION

The 82S181 is field-programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The 82S181 is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

This device includes on-chip decoding and 4 chip enable inputs for ease of memory expansion. It features 2 tri-state outputs for optimization of word expansion in bused organizations.

The 82S181 is available in both the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S181AF or N or N82S181BF or N, and for the military temperature range (−55°C to +125°C) specify S82S181A, R, F, G.

FEATURES

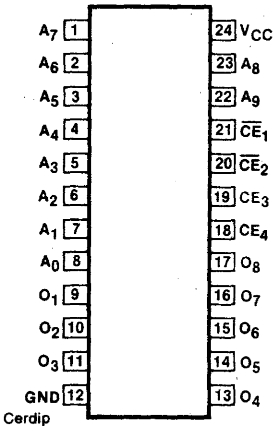
- **Address access time:**
  N82S181A: 55ns max
  N82S181B: 45ns max
  S82S181A: 80ns max
- **Power dissipation: 76μW/bit typ**
- **Input loading:**
  N82S181: −100μA max
  S82S181: −150μA max
- **On-chip address decoding**
- **Output:**
  82S181: tri-state
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION

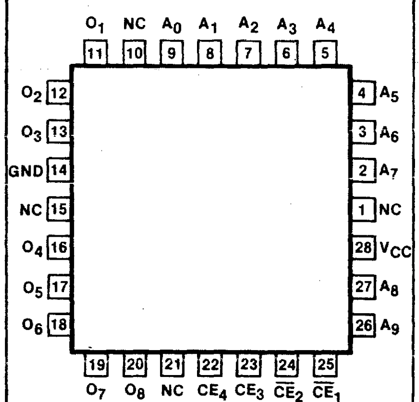
F,N,R PACKAGE*



*F = Cerdip
N = Plastic
R = Flat Pak

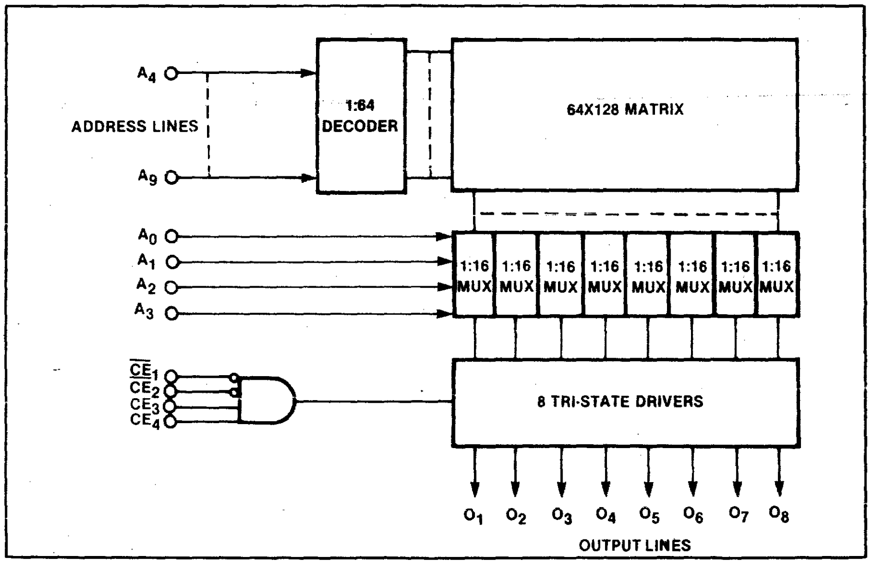
TOP VIEW

G PACKAGE



G = Leadless

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
V_O	Output voltage Off-state	 +5.5	Vdc
T_A	Temperature range Operating N82S181 S82S181	 0 to +75 -55 to +125	°C
T_{STG}	Storage	-65 to +150	

8192-BIT BIPOLAR PROM (1024×8)

82S181A/82S181B (T.S.)

DC ELECTRICAL CHARACTERISTICS

N82S181A/N82S181B: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S181A: −55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TEST CONDITIONS[1,2]	N82S181A/N82S181B			S82S181A			UNIT
			Min	Typ[5]	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low				0.8			0.8	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = −12mA		-0.8	-1.2			-1.2	
	Output voltage	$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High							V
V_{OL}	Low	I_{OUT} = 9.6mA			0.45			0.5	
V_{OH}	High	I_{OUT} = -2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								
I_{OZ}	Hi-Z state	$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, V_{OUT} = 5.5V			40			60	μA
		$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, V_{OUT} = 0.5V			-40			− 60	μA
I_{OS}	Short circuit[3]	$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High, V_{OUT} = 0V High Stored	− 15		-70	-15		-85	mA
I_{CC}	V_{CC} supply current	V_{CC} = Max		125	175			185	mA
	Capacitance	$\overline{CE}_{1,2}$ = High, V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

R_1 = 470Ω, R_2 = 1kΩ, C_L = 30pF
N82S181A/N82S181B: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S181A: −55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TO	FROM	N82S181A			N82S181B			S82S181A			UNIT
				Min	Typ[5]	Max	Min	Typ	Max	Min	Typ	Max	
T_{AA}[4]	Access time	Output	Address		45	55			45			80	ns
T_{CE}		Output	Chip enable		20	35			30			45	
T_{CD}	Disable time	Output	Chip disable		20	35			30			45	ns

NOTES

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μsec.
5. Typical values are at V_{CC} = 5V, T_A = 25°C.

8192-BIT BIPOLAR PROM (2048X4)

82S185A/82S185B (T.S.)

DESCRIPTION

The 82S185 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The standard 82S185 is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

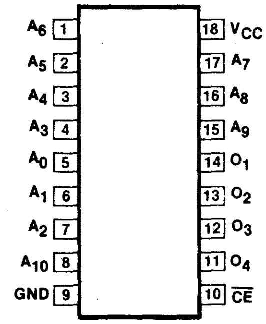
This device includes on-chip decoding and 1 chip enable input for memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations.

The 82S185 device is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S185A, F, N or N82S185B, F, or N, and for the military temperature range (−55°C to +125°C) specify S82S185A, F or R.

FEATURES

- **Low power dissipation: 70μW/bit typ**
- **Address access time:**
  - **N82S185A: 50ns max**
  - **N82S185B: 45ns max**
  - **S82S185A: 80ns max**
- **Input loading:**
  - **N82S185: −100μA max**
  - **S82S185: −150μA max**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

F,N,R PACKAGE



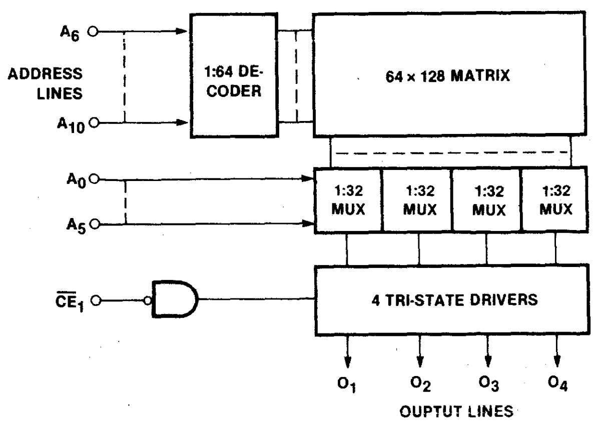
TOP VIEW

F = Cerdip
N = Plastic R = Flat Pak

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_O	Off-state	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S185	0 to +75	
	S82S185	-55 to +125	
T_{STG}	Storage	-65 to +150	

BLOCK DIAGRAM



8192-BIT BIPOLAR PROM (2048X4)

82S185A/82S185B (T.S.)

DC ELECTRICAL CHARACTERISTICS

N82S185A/N82S185B: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82S185A: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER		TEST CONDITIONS[1,2]	N82S185A/B			S82S185A			UNIT
			Min	Typ[5]	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low				0.8			0.8	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	$I_{IN} = -12mA$		-0.8	-1.2			-1.2	
	Output voltage	$\overline{CE}$ = Low							V
V_{OL}	Low	$I_{OUT} = 16mA$			0.45			0.5	
V_{OH}	High	$I_{OUT} = -2mA$	2.4			2.4			
	Input current								µA
I_{IL}	Low	$V_{IN} = 0.45V$			-100			-150	
I_{IH}	High	$V_{IN} = 5.5V$			40			50	
	Output current								
I_{OZ}	Hi-Z state	$\overline{CE}$ = High, $V_{OUT} = 0.5V$			-40			-60	µA
		$\overline{CE}$ = High, $V_{OUT} = 5.5V$			40			60	
I_{OS}	Short circuit[3]	$\overline{CE}$ = Low, $V_{OUT} = 0V$ High Stored	-15		-70	15		-85	mA
I_{CC}	V_{CC} supply current	V_{CC} = Max		110	155			160	mA
	Capacitance	$\overline{CE}$ = High, $V_{CC} = 5.0V$							pF
C_{IN}	Input	$V_{IN} = 2.0V$		5			5		
C_{OUT}	Output	$V_{OUT} = 2.0V$		8			8		

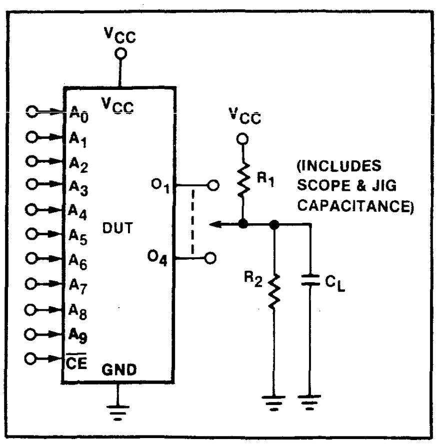
AC ELECTRICAL CHARACTERISTICS

$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$
N82S185A/N82S185B: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82S185A: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

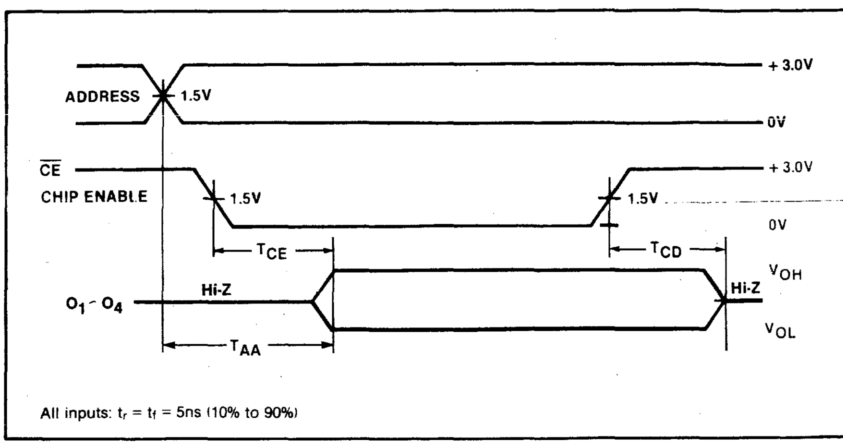
PARAMETER	TO	FROM	N82S185A			N82S185B			S82S185A			UNIT
			Min	Typ[5]	Max	Min	Typ	Max	Min	Typ	Max	
Access time												ns
T_{AA}[4]	Output	Address		40	50			45			80	
T_{CE}	Output	Chip enable		20	30			25			40	
Disable time												ns
TCD	Output	Chip disable		20	30			25			40	

NOTES
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1µsec.
5. Typical values are at $V_{CC} = 5V$, $T_A = 25°C$

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



Signetics

MEMORY

DESCRIPTION

The 82S191 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The 82S191 is supplied with all outputs at a logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

This device includes on-chip decoding and 3 chip enable inputs for ease of memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations.

The 82S191 device is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S191A, F or N, and for the military temperature range (−55°C to +125°C) specify S82S191A, F, R or G.

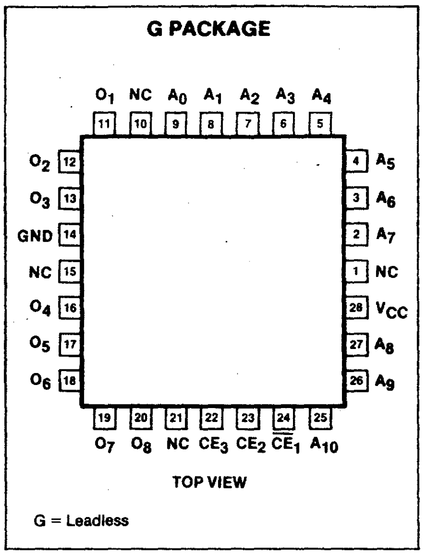
FEATURES

- **Address access time:**
  - **N82S191A: 55ns max**
  - **S82S181A: 70ns max**
- **Power dissipation: 40μW/bit typ**
- **Input loading:**
  - **N82S191A: −100μA max**
  - **S82S191A: −150μA max**
- **3 chip enable inputs**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

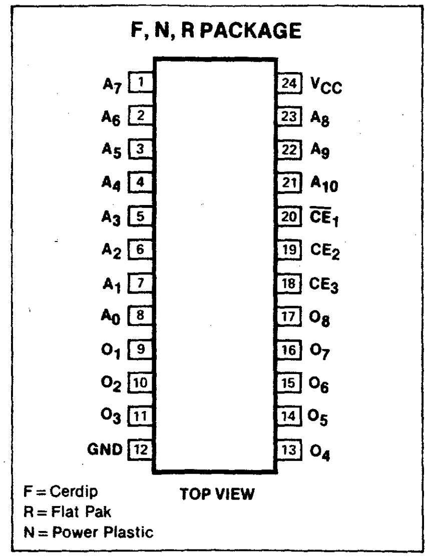
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS

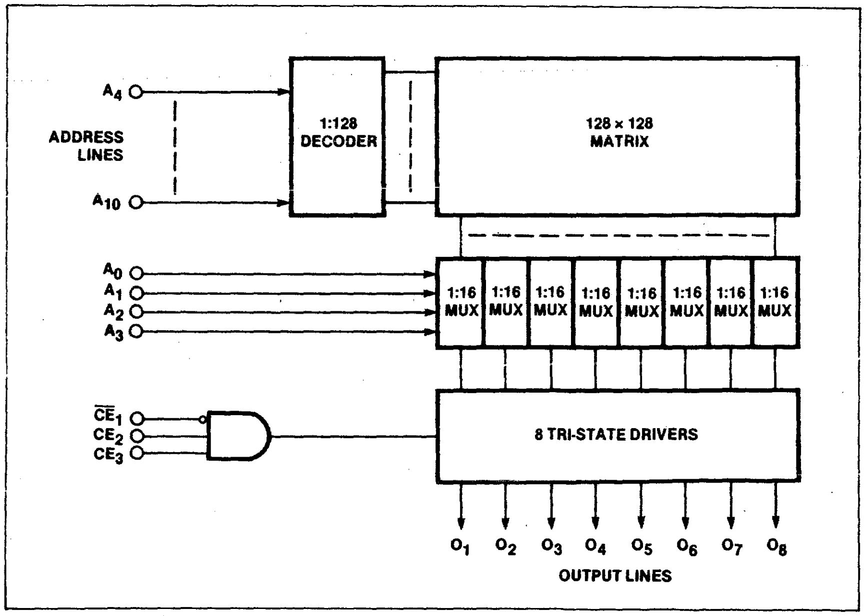


G = Leadless



F = Cerdip
R = Flat Pak
N = Power Plastic

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_O	Off-state	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S191	0 to +75	
	S82S191	-55 to +125	
T_{STG}	Storage	-65 to +150	

16,384-BIT BIPOLAR PROM (2048×8)

82S191A (T.S.)

DC ELECTRICAL CHARACTERISTICS

N82S191A: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S191A: −55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TEST CONDITIONS[1,2]	N82S191A			S82S191A			UNIT
			Min	Typ[5]	Max	Min	Typ[5]	Max	
	Input voltage								V
V_{IL}	Low				0.8			0.8	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = −12mA		-0.8	-1.2			-1.2	
	Output voltage	$\overline{CE}_1$ = Low, $CE_{2,3}$ = High							V
V_{OL}	Low	I_{OUT} = 9.6mA		•	0.45			0.5	
V_{OH}	High	I_{OUT} = -2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								μA
I_{OZ}	Hi-Z state	$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, V_{OUT} = 0.5			-40			-60	
		$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, V_{OUT} = 5.5			40			60	
I_{OS}	Short circuit[3]	$\overline{CE}_1$ = Low, $CE_{2,3}$ = High, V_{OUT} = 0V	−15		-70	-15		-85	mA
I_{CC}	V_{CC} supply current	V_{CC} = Max		130	175			185	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

R_1 = 470Ω, R_2 = 1kΩ, C_L = 30pF
N82S191A: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S191A: −55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TO	FROM	N82S191A			S82S191A			UNIT
				Min	Typ[5]	Max	Min	Typ	Max	
	Access time									ns
T_{AA}[4]		Output	Address		40	55			70	
T_{CE}		Output	Chip enable		20	30			35	
	Disable time									ns
T_{CD}		Output	Chip disable		20	30			35	

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μsec.
5. Typical values are at V_{CC} = 5V, T_A = 25°C.

16,384-BIT BIPOLAR PROM (4096×4)

82HS195(T.S.)

Advance Information

DESCRIPTION

The 82HS195 is field programmable, which means that custom patterns are immediately available by following the Generic II fusing procedure. The standard 82HS195 is supplied with all outputs at logical high. Outputs are programmed to a logic low level at any specified address by fusing a programmable matrix.

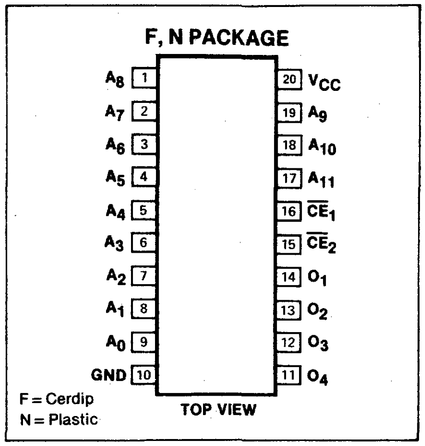
This device includes on-chip decoding and 2 chip enable inputs for memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations.

The 82HS195 device is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S195, F or N, and for the military temperature range (−55°C to +125°C) specify S82S195, F.

FEATURES

- **Low power dissipation: 35μW/bit typ**
- **Address access time:**
  - **N82HS195: 30ns max**
  - **S82HS195: 40 ns max**
- **Input loading:**
  - **N82HS195: −100μA max**
  - **S82HS195: −150μA max**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are high level**
- **Fully TTL compatible**

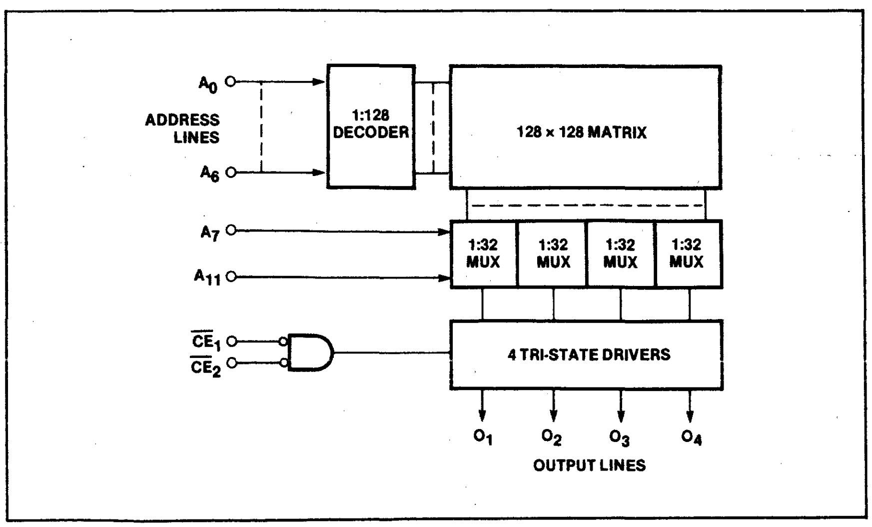
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_O	Off-state	+5.5	
	Temperature range		°C
T_A	Operating		
	N82HS195	0 to +75	
	S82HS195	-55 to +125	
T_{STG}	Storage	-65 to +150	

BLOCK DIAGRAM



Signetics

MEMORY

16,384-BIT BIPOLAR PROM (4096×4)

82HS195(T.S.)

Advance Information

DC ELECTRICAL CHARACTERISTICS

N82HS195: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82HS195: −55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TEST CONDITIONS[1,2]	N82HS195			S82HS195			UNIT
			Min	Typ[5]	Max	Min	Typ	Max	
	Input voltage[1]								V
V_{IL}	Low				0.8			0.8	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = −12mA		-0.8	-1.2			-1.2	
	Output voltage[1]	$\overline{CE}_1$ & $\overline{CE}_2$ = Low							V
V_{OL}	Low	I_{OUT} = 16mA			0.45			0.5	
V_{OH}	High	I_{OUT} = −2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								
I_{OZ}	Hi-Z state	$\overline{CE}_1$ & $\overline{CE}_2$ = High, V_{OUT} = 0.5V			-40			-60	μA
		$\overline{CE}_1$ & $\overline{CE}_2$ = High, V_{OUT} = 5.5V			40			60	
I_{OS}	Short circuit[3]	$\overline{CE}_1$ & $\overline{CE}_2$ = Low, V_{OUT} = 0V High Stored	−15		-70	-15		-85	mA
I_{CC}	V_{CC} supply current	V_{CC} = Max		110	155			165	mA
	Capacitance	$\overline{CE}_1$ & $\overline{CE}_2$ = High, V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

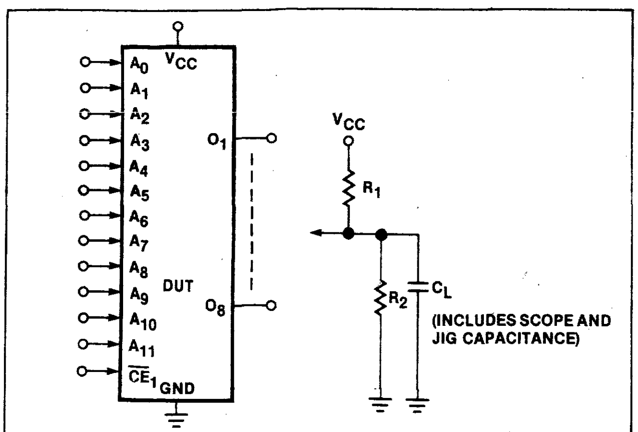
R_1 = 270Ω, R_2 = 600Ω, C_L = 30pF
N82HS195: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82HS195: −55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TO	FROM	N82HS195			S82HS195			UNIT
				Min	Typ[5]	Max	Min	Typ	Max	
	Access time									ns
T_{AA}[4]		Output	Address		25	30			40	
T_{CE}		Output	Chip enable		20	20			25	
	Disable time									ns
TCD		Output	Chip disable		20	20			25	

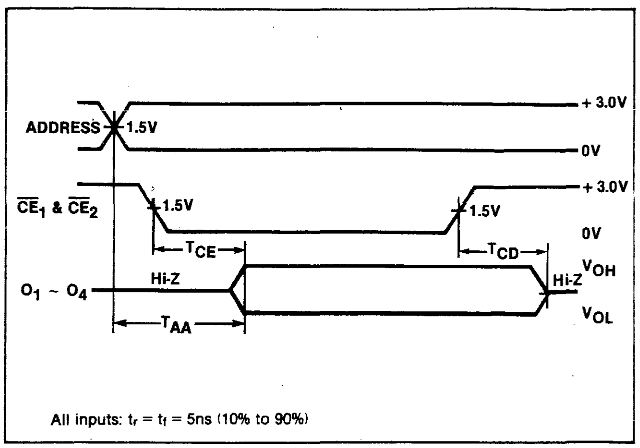
NOTES

1. All voltage values are with respect to network ground terminal.
2. Positive current is defined as into the terminal referenced.
3. Duration of the short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μsec.
5. All typical values are at V_{CC} = 5V, T_A = 25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



Signetics

MEMORY

32,768-BIT BIPOLAR PROM (4096×8) 82HS321(T.S.)

Preliminary

DESCRIPTION

The 82HS321 is field programmable, which means that custom patterns are immediately available by following the Generic II fusing procedure. The 82HS321 is supplied with all outputs at a logical high. Outputs are programmed to a logic low level at any specified address by fusing a programmable matrix.

This device includes on-chip decoding and 2 chip enable inputs for ease of memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations.

The 82HS321 device is available in the commercial and military ranges. For the commercial temperature range (0°C to +75°C) specify N82HS321, F, N, and for the military temperature range (−55°C to +125°C) specify S82HS321, F, R or G.

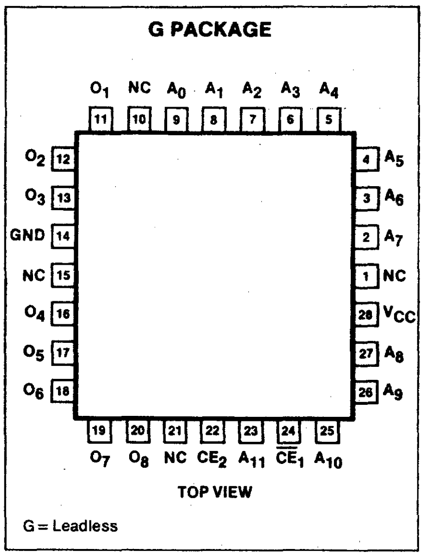
FEATURES

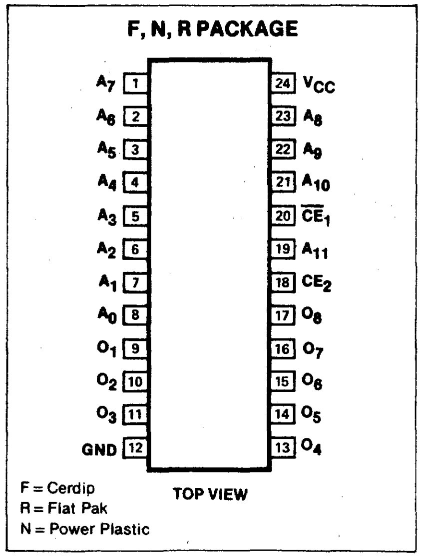
- Address access time:
  - N82HS321: 45ns max
  - S82HS321: 60ns max
- Power dissipation: 20μW/bit typ
- Input loading:
  - N82HS321: −100μA max
  - S82HS321: −150μA max
- 2 chip enable inputs
- On-chip address decoding
- No separate fusing pins
- Unprogrammed outputs are high level
- Fully TTL compatible

APPLICATIONS

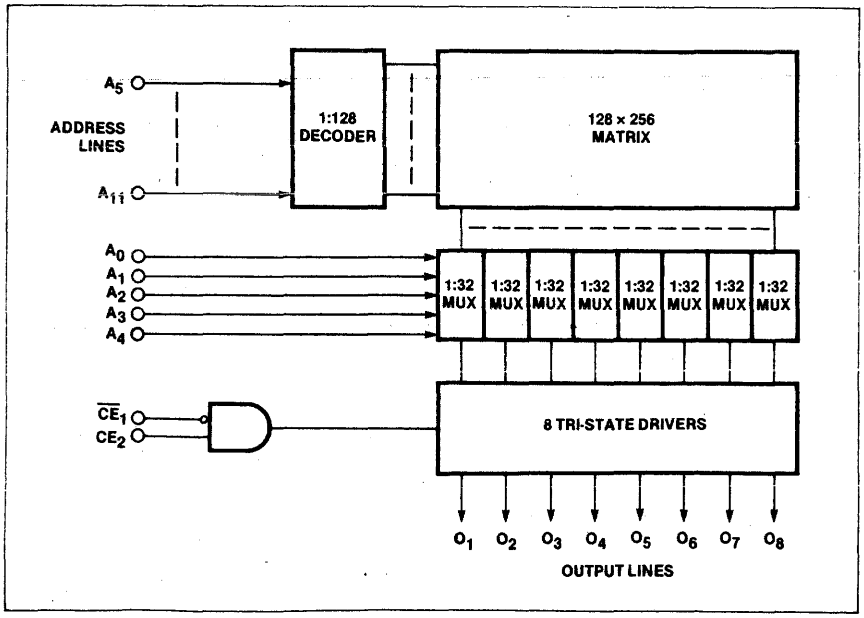
- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATIONS





BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_O	Off-state	+5.5	
	Temperature range		°C
T_A	Operating		
	N82HS321	0 to +75	
	S82HS321	-55 to +125	
T_{STG}	Storage	-65 to +150	

32,768-BIT BIPOLAR PROM (4096×8)

82HS321(T.S.)

Preliminary

DC ELECTRICAL CHARACTERISTICS

N82S321: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S321: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TEST CONDITIONS[1, 2]	N82S321			S82S321			UNIT
			Min	Typ[5]	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low				0.8			0.8	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = – 12mA		-0.8	-1.2			-1.2	
	Output voltage	$\overline{CE}_1$ = Low, CE_2 = High							V
V_{OL}	Low	I_{OUT} = 9.6mA			0.45			0.5	
V_{OH}	High	I_{OUT} = -2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								μA
I_{OZ}	Hi-Z state	$\overline{CE}_1$ = High, CE_2 = Low, V_{OUT} = 0.5			-40			-60	
		$\overline{CE}_1$ = High, CE_2 = Low, V_{OUT} = 5.5			40			60	
I_{OS}	Short circuit[3]	$\overline{CE}_1$ = Low, CE_2 = High, V_{OUT} = 0V	-15		-70	-15		-85	mA
I_{CC}	V_{CC} supply current	V_{CC} = Max		130	175			185	mA
	Capacitance	$\overline{CE}_1$ = High, CE_2 = Low, V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

R_1 = 470Ω, R_2 = 1kΩ, C_L = 30pF
N82S321: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S82S321: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TO	FROM	N82S321			S82S321			UNIT
				Min	Typ[5]	Max	Min	Typ	Max	
	Access time									ns
T_{AA}[4]		Output	Address			35			60	
T_{CE}		Output	Chip enable			25			30	
	Disable time									ns
T_{CD}		Output	Chip disable			25			30	

NOTES
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μsec.
5. Typical values are at V_{CC} = 5V, T_A = 25°C.

Signetics

MOS MEMORY Products

EPROMs

27C64
27C128
27128

ROMs

2364-15/20
2664-15/20
26S64-30/45
23128-15/20
23128-25/30/45
23256A-20/25/30/45

signetics
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Signetics Corporation
811 E. Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088-3409
Telephone 408/739-7700

65,536-BIT CMOS EPROM (8192×8) — 27C64

Advance Information

DESCRIPTION

The Signetics 27C64 EPROM is a static complementary MOS (CMOS) 5V only, 65,536-bit electrically programmable and ultraviolet light erasable read only memory, organized as 8192 words by 8 bits.

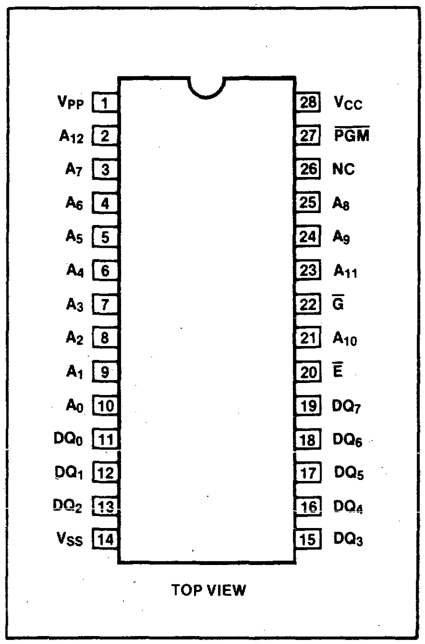
The 27C64 has a separate Output Enable control ($\overline{G}$) from the Chip Enable Control ($\overline{E}$), in order to eliminate bus contention in multiple bus systems.

The 27C64 typically consumes only 5μW power either in standby mode ($\overline{E} = V_{CC}$) or in quiescent active mode ($\overline{E} = V_{SS}$ pausing on one address location with $V_{IN} = V_{CC}$ or V_{SS}).

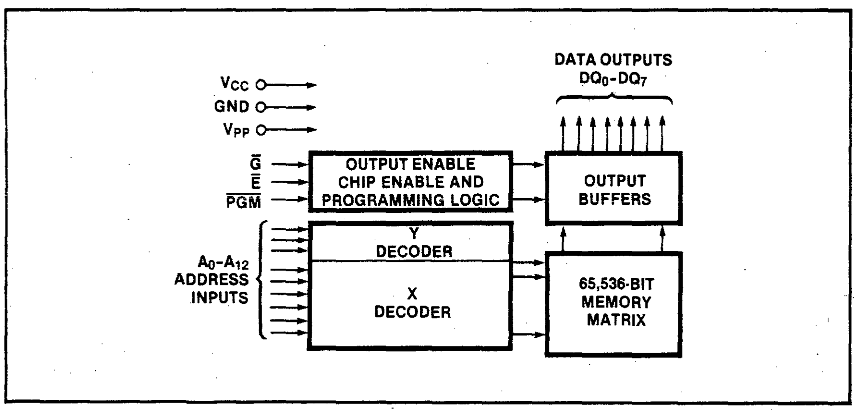
FEATURES

- **Low CMOS power consumption — 5μW typ. (standby or quiescent active) 25mW typ. (active)**
- **200ns access time**
- **TTL compatible**
- **Single +5V power supply**
- **Industry standard pinout**
- **Three-state outputs**
- **Two line controls**
- **Fast programming**

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

A_0-A_{12}	ADDRESSES
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ_0-DQ_7	Data Inputs/ Outputs
$\overline{PGM}$	Program Enable
N.C.	No Connect

ABSOLUTE MAXIMUM RATINGS (Note 1)

PARAMETER	RATING	UNIT
Temperature Range		
Storage	−65 to +125	°C
Bias	−10 to +80	
Operating Mode	0 to 70	
Program Mode	25 ±5	
Applied Voltage with Respect to Ground Potential		
Input	−0.5 to +7	V
Output	−0.5 to +7	
Supply Voltage with Respect to Ground Potential	−0.5 to +6	V
	−0.5 to +22	

NOTE
1. Stresses beyond the limits listed under "Absolute Maximum Ratings" may cause damage to the device. These are stress ratings only. Functional operation at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.

Signetics

MEMORY

Advance Information

DC ELECTRICAL CHARACTERISTICS DURING READ (Note 2) $T_A = 0°$ to $+70°C$, $V_{CC} = 5.0V \pm 10\%$, unless otherwise specified, $V_{PP} = V_{CC}$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
V_{IL}	Input Voltage Low		−0.1		0.8	V
V_{IH}	Input Voltage High		2.0		$V_{CC}+1$	V
V_{OL}	Output Voltage Low	$I_{OL} = 3.2mA$	—		0.45	V
V_{OH}	Output Voltage High	$I_{OH} = -400\mu A$	2.4		V_{CC}	V
I_{LI}	Input Load Current	$V_{IN} = 5.5V$ or $0.45V$	—		10	μA
I_{LO}	Output Leakage	$V_{OUT} = 5.5V$ or $0.45V$, $\overline{E} = V_{CC}$	—		10	μA
I_{CCS1}	V_{CC} Standby Current	$\overline{E} = V_{CC}$	—	1	100	μA
I_{CCS2}	V_{CC} Standby Current	$\overline{E} = V_{IH}$	—		1	mA
I_{CCQ1}	V_{CC} Active Current (Quiescent)	$\overline{E} = \overline{G} = V_{SS}$ All Addresses at either V_{SS} or V_{CC}	—	1	100	μA
I_{CCQ2}	V_{CC} Active Current (Quiescent)	$\overline{E} = \overline{G} = V_{IL}$ All Addresses at either V_{IL} or V_{IH}		1.3	15	mA
I_{CCA1}	V_{CC} Active Current (Operating)	$\overline{E} = \overline{G} = V_{SS}$ All addresses changing between V_{SS} and V_{CC}	—	5	25	mA
I_{CCA2}	V_{CC} Active Current (Operating)	$\overline{E} = \overline{G} = V_{IL}$ All addresses changing between V_{IL} and V_{IH}		20	30	mA
C_{IN}	Input Capacitance (Note 3)	$V_{IN} = 0V$, $f = 1MHz$		4	6	pF
C_{OUT}	Output Capacitance (Note 4)	$V_{OUT} = 0V$, $f = 1MHz$		8	12	pF

NOTES
2. Typical values are for $T_A = 25°C$ and nominal power supply voltages.
3. Typical values are for $T_A = 25°C$ and nominal power supplies.
4. These parameters are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS DURING READ (Note 5) $T_A = 0°$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise specified, $V_{PP} = V_{CC}$

STANDARD SYMBOL	COMMON SYMBOL	PARAMETER	TEST CONDITIONS (Note 5)	27C64-20 Min	27C64-20 Max	27C64-25 Min	27C64-25 Max	27C64-30 Min	27C64-30 Max	UNIT
t_{AVQV}	t_{ACC}	Address Access Time	$\overline{E} = \overline{G} = V_{IL}$		200		250		300	ns
t_{ELQV}	t_{CE}	Chip Select Delay	$\overline{G} = V_{IL}$		200		250		300	ns
t_{GLQV}	t_{OE}	Output Enable Delay	$\overline{E} = V_{IL}$ (Note 6)	10	70	10	100	10	150	ns
t_{EHQZ}	t_{DF}	Chip Deselect Delay (Note 7)	$\overline{E} = V_{IL}$ t_{DF} is measured at $V_{OL} = 0.8$ to tri-state (High-Z) transition	0	60	0	90	0	130	ns
t_{AXQZ}	t_{OH}	Previous Output Data Holding Time	From Addresses, $\overline{E}$ or $\overline{G}$ whichever occurred first $\overline{E} = \overline{G} = V_{IL}$	0		0		0		ns

NOTES
5. AC TEST CONDITIONS:
Output load 2 TTL gates and $C_L = 100pF$
Input rise and fall times: ≤20ns
Input pulse levels: 0.8V to 2.2V
Timing measurement reference levels:
Inputs 1.5V
Outputs 0.6V and 2.2V

6. G may be delayed up to $t_{AVQV} - t_{GLQV}$ after the falling edge of $\overline{E}$ without impact on t_{AVQV}.
7. t_{EHQX} is specified from $\overline{G}$ or $\overline{E}$, whichever occurs first.

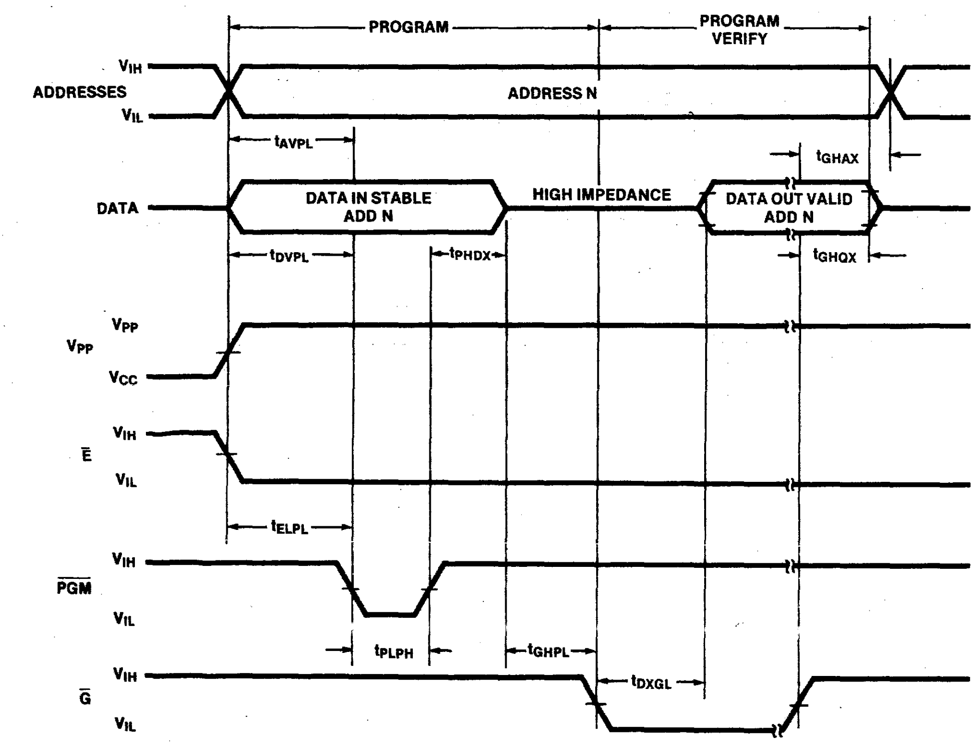
Advance Information

AC ELECTRICAL CHARACTERISTICS DURING PROGRAMMING (Note 10) $T_A = 25 \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$

STANDARD SYMBOL	COMMON SYMBOL	PARAMETER	TEST CONDITIONS(Note 2)	LIMITS Min	Typ	Max	UNIT
t_{AVPL}	t_{AS}	Address Set-up Time		2			μS
t_{DVPL}	t_{DS}	Data Set-up Time		2			μS
t_{PHDX}	t_{DH}	Data Hold Time		2			μS
t_{VHPL}	t_{VPPS}	V_{PP} Set-up Time		2			μS
t_{ELPL}	t_{CES}	$\overline{CE}$ Set-up Time		2			μS
t_{PLPH}	t_{PW}	$\overline{PGM}$ Pulse Width During Programming		25	50	55	mS
t_{GHPL}	t_{OES}	$\overline{OE}$ Set-up Time		2			μS
t_{GHQZ}	t_{DF}	Chip Deselect Delay (Note 9)	$\overline{CE} = V_{IL}$	0		130	ns
t_{PHAX}	t_{AH}	Address Hold Time					μS

Note:
9. t_{GHQX} is specified from $\overline{G}$ or $\overline{E}$, whichever occurs first.
10. The input reference level is 1V for V_{IL} and 2V for V_{IH}.

TIMING DIAGRAM DURING PROGRAMMING

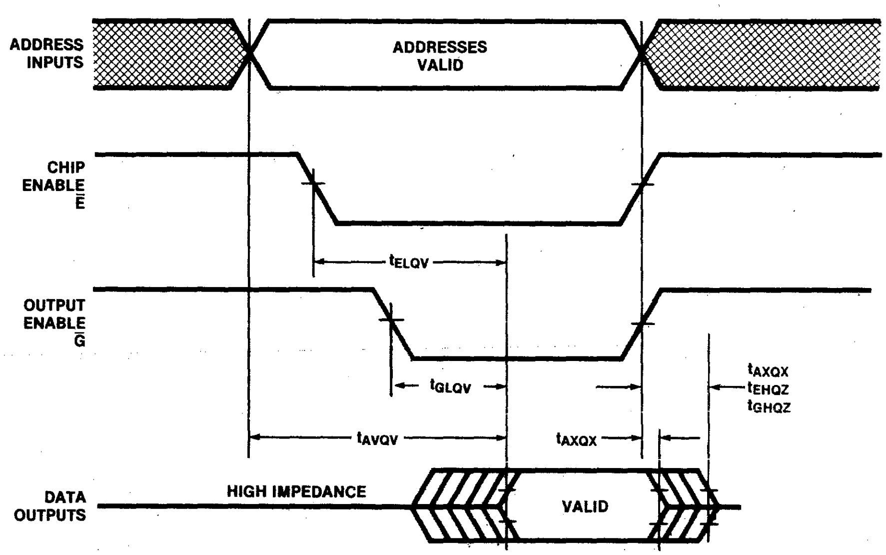


Advance Information

MODE SELECTION

MODE/PINS	$\overline{E}$ (20)	$\overline{G}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	DQ_0-DQ_7 (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	DQ_{OUT}
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	DQ_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	DQ_{OUT}
Program Inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	High Z
X can be either V_{OL} or V_{OH}.						

TIMING DIAGRAM DURING READ



DC ELECTRICAL CHARACTERISTICS DURING PROGRAMMING (Note 8) $T_A = 25 \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input Voltage — Low		−0.1		0.8	V
V_{IH}	Input Voltage — High		2.0		$V_{CC}+1$	
V_{OL}	Output Voltage During Verify — Low	$I_{OL} = 3.2mA$			0.45	V
V_{OH}	Output Voltage During Verify — High	$I_{OH} = 400\mu A$	2.4			
I_{LI}	Input Load Current	$V_{IN} = 5.25V$ or V_{IL}			10	μA
I_{CCA3}	V_{CC} Supply Current — Active			20	30	mA
I_{PP2}	V_{PP} Supply Current During Programming Pulse	$\overline{E} = \overline{PGM} = V_{IL}$, $V_{PP} = 21.5V$, DQ_0-$DQ_7 = V_{IL}$			30	mA

Note:
8. V_{CC} must be applied before and removed after V_{PP}. V_{PP} should never exceed 21.5V (including transients). If $\overline{PGM} = V_{IL}$, V_{PP} should not be switched.

131,072-BIT CMOS EPROM (16,384×8) 27C128

Preview

DESCRIPTION

The Signetics 27C128 EPROM is a static complementary MOS (CMOS) 5V only, 131,072-bit electrically programmable and ultraviolet light erasable read only memory, organized as words by bits.

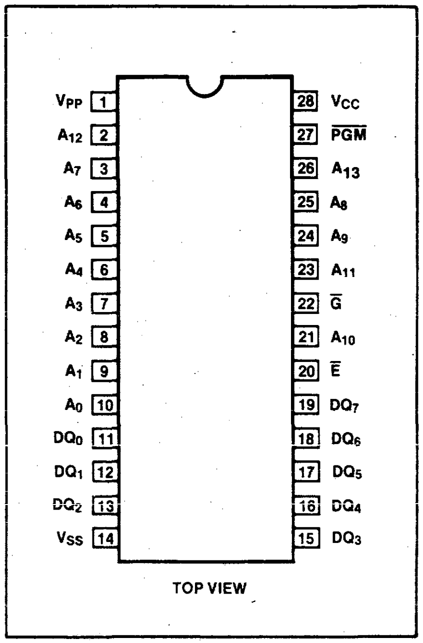
The 27C128 has a separate Output Enable control ($\overline{G}$) from the Chip Enable Control ($\overline{E}$), in order to eliminate bus contention in multiple bus systems.

The 27C128 typically consumes only 5μW power either in standby mode ($\overline{E} = V_{CC}$) or in quiescent active mode ($\overline{E} = V_{SS}$ pausing on one address location with $V_{IN} = V_{CC}$ or V_{SS}).

FEATURES

- **Low CMOS power consumption — 5μW typ. (standby or quiescent active) 25mW typ. (active)**
- **250ns access time**
- **TTL compatible**
- **Single +5V power supply ±10%**
- **Industry standard pinout**
- **Three-state outputs**
- **Two line controls**
- **Fast programming**

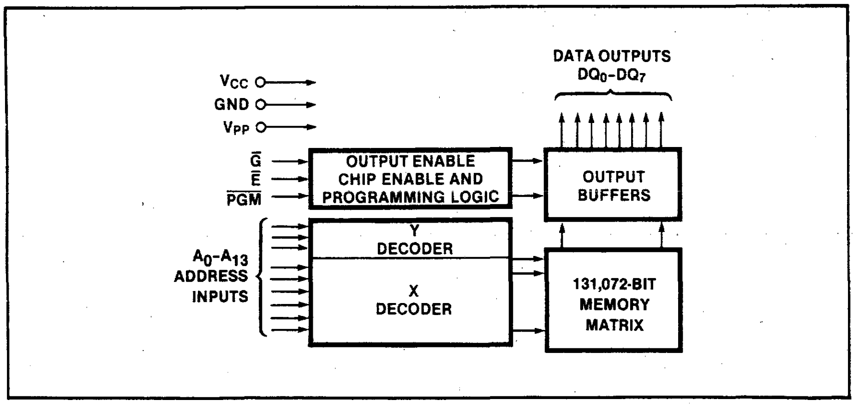
PIN CONFIGURATION



PIN NAMES

A_0-A_{13}	ADDRESSES
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ_0-DQ_7	Data Inputs/ Outputs
$\overline{PGM}$	Program Enable

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

PARAMETER	RATING	UNIT
Temperature Range		
Storage	−65 to +125	°C
Bias	−10 to +80	
Operating Mode	0 to 70	
Program Mode	25 ±5	
Applied Voltage with Respect to Ground Potential		
Input	−0.5 to +7	V
Output	−0.5 to +7	
Supply Voltage with Respect to Ground Potential	−0.5 to +6	V
	−0.5 to +22	

NOTE

1. Stresses beyond the limits listed under "Absolute Maximum Ratings" may cause damage to the device. These are stress ratings only. Functional operation at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.

131,072-BIT CMOS EPROM (16,384×8) 27C128

Preview

DC ELECTRICAL CHARACTERISTICS DURING READ (Note 2) $T_A = 0°$ to $+70°C$, $V_{CC} = 5.0V \pm 10\%$, unless otherwise specified, $V_{PP} = V_{CC}$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS Min	Typ	Max	UNIT
V_{IL}	Input Voltage Low		−0.1		0.8	V
V_{IH}	Input Voltage High		2.0		$V_{CC}+1$	V
V_{OL}	Output Voltage Low	$I_{OL} = 3.2mA$	—		0.45	V
V_{OH}	Output Voltage High	$I_{OH} = -400\mu A$	2.4		V_{CC}	V
I_{LI}	Input Load Current	$V_{IN} = 5.5V$ or 0.45V	—		10	μA
I_{LO}	Output Leakage	$V_{OUT} = 5.5V$ or 0.45V, $\overline{E} = V_{CC}$	—		10	μA
I_{CCS1}	V_{CC} Standby Current	$\overline{E} = V_{CC}$	—	1	100	μA
I_{CCS2}	V_{CC} Standby Current	$\overline{E} = V_{IH}$	—		1	mA
I_{CCQ1}	V_{CC} Active Current (Quiescent)	$\overline{E} = \overline{G} = V_{SS}$ All Addresses at either V_{SS} or V_{CC}	—	1	100	μA
I_{CCQ2}	V_{CC} Active Current (Quiescent)	$\overline{E} = \overline{G} = V_{IL}$ All Addresses at either V_{IL} or V_{IH}		1.3	15	mA
I_{CCA1}	V_{CC} Active Current (Operating)	$\overline{E} = \overline{G} = V_{SS}$ All addresses changing between V_{SS} and V_{CC}	—	5	25	mA
I_{CCA2}	V_{CC} Active Current (Operating)	$\overline{E} = \overline{G} = V_{IL}$ All addresses changing between V_{IL} and V_{IH}		20	30	mA
C_{IN}	Input Capacitance (Note 3)	$V_{IN} = 0V$, f = 1MHz		4	6	pF
C_{OUT}	Output Capacitance (Note 4)	$V_{OUT} = 0V$, f = 1MHz		8	12	pF

NOTES
2. Typical values are for $T_A = 25°C$ and nominal power supply voltages.
3. Typical values are for $T_A = 25°C$ and nominal power supplies.
4. These parameters are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS DURING READ (Note 5) $T_A = 0°$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise specified, $V_{PP} = V_{CC}$

STANDARD SYMBOL	COMMON SYMBOL	PARAMETER	TEST CONDITIONS (Note 5)	LIMITS 27C128-20 Min	27C128-20 Max	27C128-25 Min	27C128-25 Max	27C128-30 Min	27C128-30 Max	UNIT
t_{AVQV}	t_{ACC}	Address Access Time	$\overline{E} = \overline{G} = V_{IL}$		200		250		300	ns
t_{ELQV}	t_{CE}	Chip Select Delay	$\overline{G} = V_{IL}$		200		250		300	ns
t_{GLQV}	t_{OE}	Output Enable Delay	$\overline{E} = V_{IL}$ (Note 6)	10	70	10	100	10	150	ns
t_{EHQZ}	t_{DF}	Chip Deselect Delay (Note 7)	$\overline{E} = V_{IL}$; t_{DF} is measured at $V_{OL} = 0.8$ to tri-state (High-Z) transition	0	60	0	90	0	130	ns
t_{AXQZ}	t_{OH}	Previous Output Data Holding Time	From Addresses, $\overline{E}$ or $\overline{G}$ whichever occurred first $\overline{E} = \overline{G} = V_{IL}$	0		0		0		ns

NOTES
5. AC TEST CONDITIONS:
Output load 2 TTL gates and $C_L = 100pF$
Input rise and fall times: ≤20ns
Input pulse levels: 0.8V to 2.2V
Timing measurement reference levels:
Inputs 1.5V
Outputs 0.6V and 2.2V

6. G may be delayed up to $t_{AVQV} - t_{GLQV}$ after the falling edge of $\overline{E}$ without impact on t_{AVQV}.
7. Specified from $\overline{G}$ or $\overline{E}$, whichever occurs first.

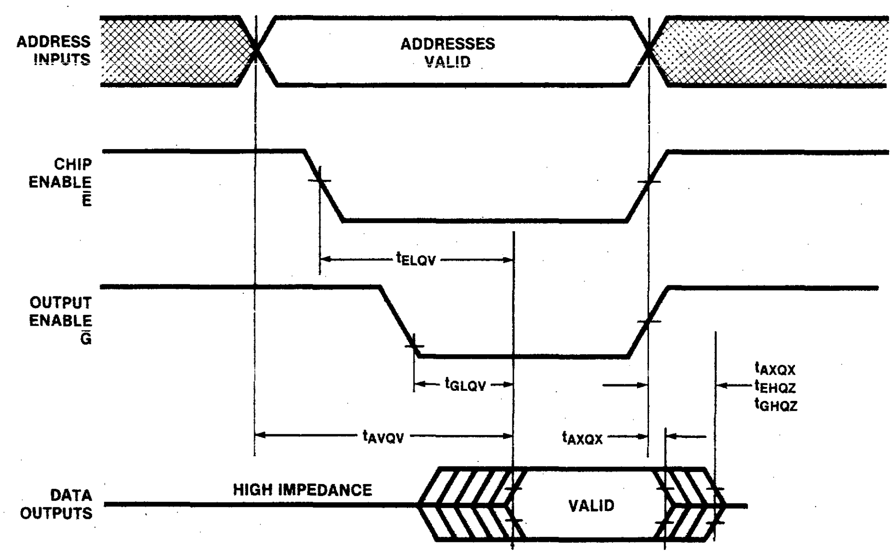
Preview

MODE SELECTION

MODE/PINS	$\overline{E}$ (20)	$\overline{G}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	DQ_0-DQ_7 (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	DQ_{OUT}
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	DQ_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	DQ_{OUT}
Program Inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	High Z

X can be either V_{OL} or V_{OH}.

TIMING DIAGRAM DURING READ



DC ELECTRICAL CHARACTERISTICS DURING PROGRAMMING (Note 8) $T_A = 25 \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input Voltage — Low		−0.1		0.8	V
V_{IH}	Input Voltage — High		2.0		$V_{CC}+1$	
V_{OL}	Output Voltage During Verify — Low	$I_{OL} = 3.2mA$			0.45	V
V_{OH}	Output Voltage During Verify — High	$I_{OH} = 400\mu A$	2.4			
I_{LI}	Input Load Current	$V_{IN} = 5.25V$ or V_{IL}			10	μA
I_{CCA3}	V_{CC} Supply Current — Active			20	30	mA
I_{PP2}	V_{PP} Supply Current During Programming Pulse	$\overline{E} = \overline{PGM} = V_{IL}$ $V_{PP} = 21.5V$, DQ_0-$DQ_7 = V_{IL}$			30	mA

NOTE

8. V_{CC} must be applied before and removed after V_{PP}. V_{PP} should never exceed 21.5V (including transients). If $\overline{PGM} = V_{IL}$, V_{PP} should not be switched.

131,072-BIT NMOS EPROM (16,384×8) 27128

Preview

DESCRIPTION

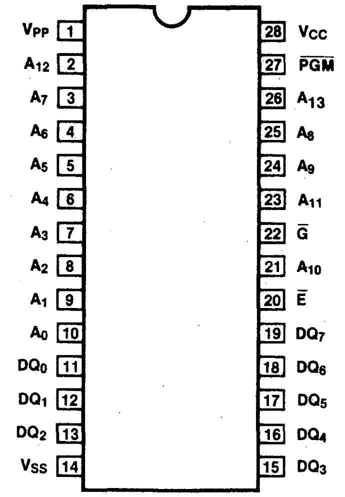
The Signetics 27128 EPROM is an NMOS, 5V only, 131,072-bit electrically programmable and ultraviolet light erasable read only memory, organized as 16,384 words by 8 bits. The 27128 has a separate Output Enable control ($\overline{G}$) from the Chip Enable control ($\overline{E}$), in order to eliminate bus contention in multiple bus systems.

The 27128 has a standby mode to reduce the power dissipation with no increase in access time. The maximum active current is 100mA while the standby current is 40mA from the power supply. This mode is initiated by placing a TTL-high signal on the $\overline{E}$ input.

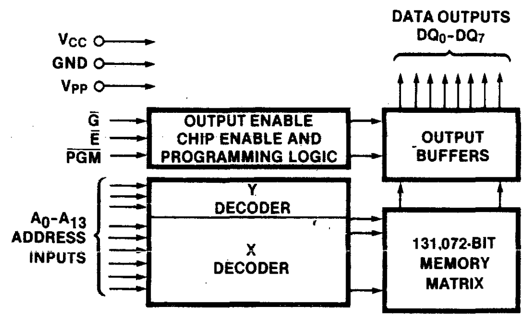
FEATURES

- **250ns access time**
- **TTL compatible**
- **Single +5V power supply ±10%**
- **Industry standard pinout**
- **Power down mode with 30mA maximum power supply current**
- **Three-state outputs**
- **Two line controls**

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

A_0-A_{13}	ADDRESSES
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ_0-DQ_7	Data Inputs/ Outputs
$\overline{PGM}$	Program Enable

DC ELECTRICAL CHARACTERISTICS DURING READ (Note 1) $T_A = 0°$ to $+70°C$, $V_{CC} = 5.0V \pm 10\%$, unless otherwise specified, $V_{PP} = V_{CC}$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input Voltage — Low		−0.1		0.8	V
V_{IH}	Input Voltage — High		2.0		$V_{CC}+1$	
V_{OL}	Output Voltage — Low	$I_{OL} = 3.2mA$			0.45	V
V_{OH}	Output Voltage — High	$I_{OH} = -400\mu A$	2.4		V_{CC}	
I_{LI}	Input Load Current	$V_{IN} = 5.5V$ or $0.45V$			10	μA
I_{LO}	Output Leakage	$V_{OUT} = 5.5V$ or $0.45V$, $\overline{E} = V_{IH}$			10	μA
I_{CC1}	V_{CC} Supply Current — Standby	$\overline{E} = V_{IH}$		15	30	mA
I_{CC2}	V_{CC} Supply Current — Active	$\overline{E} = \overline{G} = V_{IL}$		50	100	mA
I_{PP1}	V_{PP} Supply Current — Read Mode	$V_{PP} = 5.25V$			5	mA

NOTE
1. Typical values are for $T_A = 25°C$ and nominal power supply voltages.

131,072-BIT NMOS EPROM (16,384×8) 27128

Preview

AC ELECTRICAL CHARACTERISTICS DURING READ (Note 2) $T_A = 0°$ to $+70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise specified, $V_{PP} = V_{CC}$

STANDARD SYMBOL	COMMON SYMBOL	PARAMETER	TEST CONDITIONS (Note 2)	LIMITS 27128-20 Min	Max	27128-25 Min	Max	27128-30 Min	Max	UNIT
t_{AVQV}	t_{ACC}	Address Access Time	$\overline{E} = \overline{G} = V_{IL}$		200		250		300	ns
t_{ELQV}	t_{CE}	Chip Select Delay	$\overline{G} = V_{IL}$		200		250		300	ns
t_{GLQV}	t_{OE}	Output Enable Delay	$\overline{E} = V_{IL}$ (Note 3)	10	70	10	100	10	150	ns
t_{EHQX} t_{GHQX}	t_{DF}	Chip Deselect Delay (Note 4)	$\overline{E} = V_{IL}$ t_{DF} is measured at $V_{OL} = 0.5$ to tri-state (High-Z) transition	0	60	0	90	0	130	ns
t_{AXQX}	t_{OH}	Previous Output Data Holding Time	From Addresses, $\overline{E}$ or $\overline{G}$ whichever occurred first $\overline{E} = \overline{G} = V_{IL}$	0		0		0		ns

NOTES
2. AC TEST CONDITIONS:
Output load 2 TTL gates and $C_L = 100pF$
Input rise and fall times: $\leq 20ns$
Input pulse levels: 0.8V to 2.2V
Timing measurement reference levels:
Inputs 1.5V
Outputs 0.6V and 2.2V
3. G may be delayed up to $t_{AVQV} - t_{GLQV}$ after $\overline{E}$ without impact on t_{AVQV}.
4. t_{EHQX} is specified from $\overline{G}$ or $\overline{E}$, whichever occurs first.

DC ELECTRICAL CHARACTERISTICS DURING PROGRAMMING (Note 5) $T_A = 25 \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS Min	Typ	Max	UNIT
V_{IL}	Input Voltage — Low		−0.1		0.8	V
V_{IH}	Input Voltage — High		2.0		$V_{CC}+1$	
V_{OL}	Output Voltage During Verify — Low	$I_{OL} = 3.2mA$			0.45	V
V_{OH}	Output Voltage During Verify — High	$I_{OH} = 400\mu A$	2.4			
I_{LI}	Input Load Current	$V_{IN} = 5.25V$ or V_{IL}			10	µA
I_{CC2}	V_{CC} Supply Current — Active				100	mA
I_{PP2}	V_{PP} Supply Current During Programming Pulse	$\overline{E} = \overline{PGM} = V_{IL}$ $V_{PP} = 21.5V$, DQ_0-$DQ_7 = V_{IL}$			30	mA

NOTE
5. V_{CC} must be applied before and removed after V_{PP}. V_{PP} should never exceed 21.5V (including transients). If $\overline{PGM} = V_{IL}$, V_{PP} should not be switched.

AC ELECTRICAL CHARACTERISTICS DURING PROGRAMMING (Note 7) $T_A = 25 \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 21V \pm 0.5V$

STANDARD SYMBOL	COMMON SYMBOL	PARAMETER	TEST CONDITIONS (Note 2)	LIMITS Min	Typ	Max	UNIT
t_{AVPL}	t_{AS}	Address Set-up Time		2			µS
t_{DVPL}	t_{DS}	Data Set-up Time		2			µS
t_{PHDX}	t_{DH}	Data Hold Time		2			µS
t_{VHPL}	t_{VPPS}	V_{PP} Set-up Time		2			µS
t_{ELPL}	t_{CES}	$\overline{E}$ Set-up Time		2			µS
t_{PLPH}	t_{PW}	$\overline{PGM}$ Pulse Width During Programming		45	50	55	mS
t_{GHPL}	t_{OES}	$\overline{G}$ Set-up Time		2			µS
t_{GHQX} t_{EHQZ}	t_{DF}	Chip Deselect Delay (Note 6)	$\overline{E} = V_{IL}$	0		130	ns
t_{PHAX}	t_{AH}	Address Hold Time			0		ns

NOTES
6. t_{GHQX} is specified from $\overline{G}$ or $\overline{E}$, whichever occurs first.
7. The input reference level is 1V for V_{IL} and 2V for V_{IH}.

65,536-BIT STATIC MOS ROM (8192×8)

2364-15/20

DESCRIPTION

This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

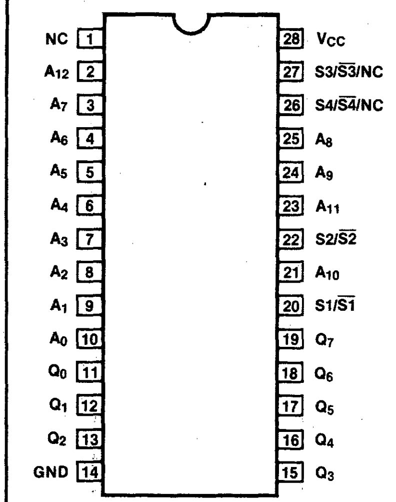
The four Chip Select inputs are programmable. Active-high or active-low level Chip Select input can can be defined by the designer and the desired chip select logic level is fixed during the masking process. The programmable Chip Select input, as well as OR-tie compatibility on the outputs, facilitates easy memory expansion.

The 2364 Read-Only Memory is fabricated with n-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits.

FEATURES

- **Fast access time**
- **Industry standard pinout — JEDEC approved**
- **Completely TTL compatible**
- **One +5V ±10% power supply**
- **Low power dissipation**
- **Three-state output — OR-tie capability**
- **Four programmable Chip Select inputs for easy memory expansion or no connection option**
- **Inputs protected — all inputs have protection against static charge**
- **2764 EPROM compatible**

PIN CONFIGURATION



TOP VIEW

PACKAGE AVAILABILITY

See Ordering Information

ABSOLUTE MAXIMUM RATINGS (Note 1)

PARAMETER	RATING	UNIT
Operating Temperature 2364-XX	0 to +70	°C
2364E-XX	−40 to +85	°C
Storage Temperature	−65 to +150	°C
Voltage on Any Pin Relative to Ground	−2 to +7	V
Power Dissipation	1	Watt
Electrostatic Discharge Rating Relative to Ground (Note 2)	±2000	V

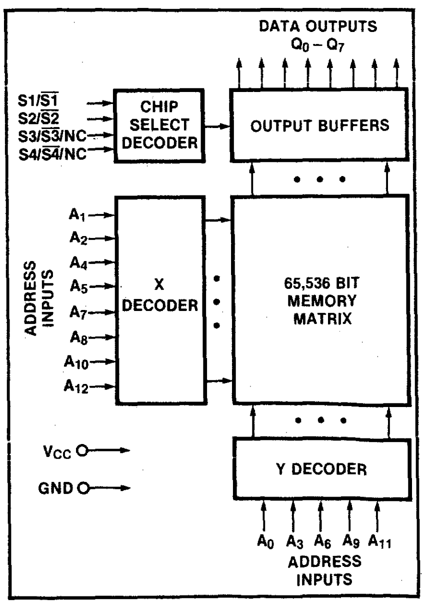
NOTES

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these any any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Test condition. Discharge 100pF through 1500 ohms, MIL-STD 883, method 3015.1.

PIN NAMES

A_0–A_{12}	Address Inputs
S1–S4	Chip Selects
Q_0–Q_7	Data Outputs
V_{CC}	Power
GND	Ground
NC	Not Connected

BLOCK DIAGRAM



ORDERING INFORMATION

TEMPERATURE RANGE	PACKAGE TYPE	ORDER NUMBER BY ACCESS TIME	
		150ns	200ns
0°C to +70°C	Plastic	2364-15N	2364-20N
0°C to +70°C	Cerdip	2364-15F	2364-20F
0°C to +70°C	Ceramic	2364-15I	2364-20I
−40°C to +85°C	Plastic	2364E-15N	2364E-20N
−40°C to +85°C	Cerdip	2364E-15F	2364E-20F
−40°C to +85°C	Ceramic	2364E-15I	2364E-20I

DC ELECTRICAL CHARACTERISTICS $V_{CC}=5.0V \pm 10\%$

PARAMETER	TEST CONDITIONS	2364E-15		2364E-20		2364-15		2364-20		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
Input voltage V_{IL} Low (Note 3) V_{IH} High		 −2.0 2.0	 0.8 V_{CC}	 −2.0 2.0	 0.8 V_{CC}	 −2.0 2.0	 0.8 V_{CC}	 −2.0 2.0	 0.8 V_{CC}	V
Output voltage V_{OL} Low V_{OH} High	 $I_{OL}=3.2mA$ $I_{OH}=-400\mu A$	 2.4	 0.4 V_{CC}	 2.4	 0.4 V_{CC}	 2.4	 0.4 V_{CC}	 2.4	 0.4 V_{CC}	V
I_{LI} Input load current	$0V \le V_{IN} \le 5.5V$		1		1		1		1	μA
I_{LO} Output leakage	Chip deselected. $V_{OUT}=+0.4V$ to V_{CC}		5		5		5		5	μA
I_{CC} Supply current	Chip deselected. $V_{CC}=5.5V$, $V_{IN}=V_{CC}$		120		110		110		90	mA
Capacitance (Note 4) C_{IN} Input C_{OUT} Output	$T_A=25°C$, f = 1MHz, all pins except pin under test tied to ground		 7 10		 7 10		 7 10		 7 10	pF

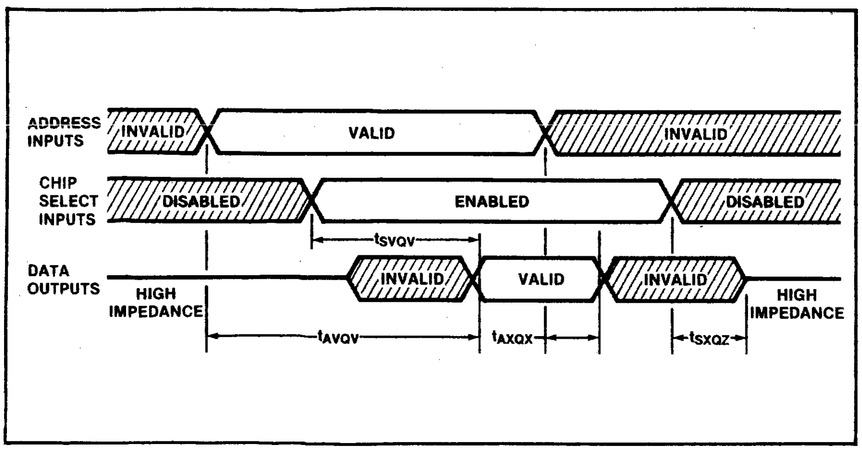
NOTES
3. Input levels that swing more negative than −2.0V may alter AC electrical characteristics.
4. This parameter is periodically sampled and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS $V_{CC}=5.0V \pm 10\%$

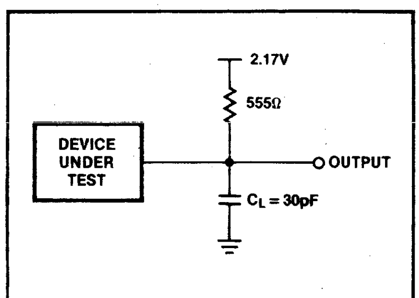
PARAMETER		-15		-20		UNIT
		Min	Max	Min	Max	
t_{AVQV}	Address access time		150		200	ns
t_{SVQV} (Note 5)	Chip select delay		100		100	ns
t_{SXQZ} (Note 6)	Chip deselect delay		75		100	ns
t_{AXQX}	Previous data valid after address change delay	0		0		ns

NOTES
5. t_{SVQV} is at value indicated, provided the valid address leads the chip select by (t_{AVQV}-t_{SVQV}) ns or more.
6. t_{SXQZ} is measured at $V_{OL}=0.5V$ on the "0" to High-Z state transition, with AC test load connected to the output.

TIMING DIAGRAM



AC TEST LOAD



Input transition time ≤5ns
Input signal levels: 0.4V to 2.4V
Timing reference levels:
Input = 1.5V
Output = 0.6V and 2.2V

65,536-BIT STATIC MOS ROM (8192×8)

2664A-15/20

DESCRIPTION

This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

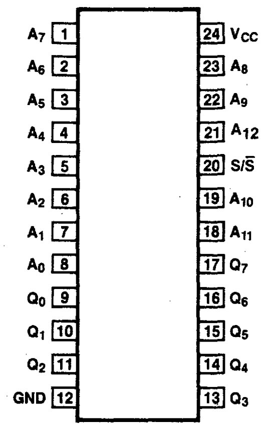
The Chip Select input is programmable. Active-high or active-low level Chip Select input can be defined by the designer and the desired chip select logic level is fixed during the masking process. The programmable Chip Select input, as well as OR-tie compatibility on the outputs, facilitates easy memory expansion.

The 2664A Read-Only Memory is fabricated with n-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits.

FEATURES

- **Fast access time**
- **Low power dissipation**
- **Industry standard pinout — JEDEC approved**
- **Completely TTL compatible**
- **One +5V ±10% power supply**
- **Three-state output — OR-tie capability**
- **One programmable chip select input for easy memory expansion or no connection option**
- **Inputs protected — all inputs have protection against static charge**
- **2764 EPROM compatible**

PIN CONFIGURATION



TOP VIEW

PACKAGE AVAILABILITY

See Ordering Information

ABSOLUTE MAXIMUM RATINGS (Note 1)

PARAMETER	RATING	UNIT
Operating Temperature 2664A-XX	0 to +70	°C
2664AE-XX	−40 to +85	°C
Storage Temperature	−65 to +150	°C
Voltage on Any Pin Relative to Ground	−2 to +7	V
Power Dissipation	1	Watt
Electrostatic Discharge Rating Relative to Ground (Note 2)	±2000	V

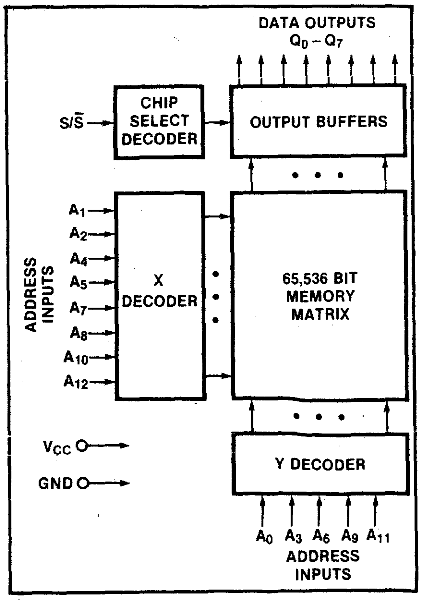
NOTES

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these any any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Test condition. Discharge 100pF through 1500 ohms, MIL-STD 883, method 3015.1.

PIN NAMES

A_0-A_{12}	Address Inputs
S	Chip Select
Q_0-Q_7	Data Outputs
V_{CC}	Power
GND	Ground

BLOCK DIAGRAM



ORDERING INFORMATION

TEMPERATURE RANGE	PACKAGE TYPE	ORDER NUMBER BY ACCESS TIME	
		150ns	200ns
0°C to +70°C	Plastic	2664A-15N	2664A-20N
−40°C to +85°C	Plastic	2664AE-15N	2664AE-20N
−40°C to +85°C	Cerdip	2664AE-15F	2664AE-20F
−40°C to +85°C	Ceramic	2664AE-15I	2664AE-20I

65,536-BIT STATIC MOS ROM (8192×8) — 2664A-15/20

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 5.0V \pm 10\%$

PARAMETER		TEST CONDITIONS	2664AE-15		2664AE-20		2664A-15		2664A-20		UNIT
			Min	Max	Min	Max	Min	Max	Min	Max	
	Input voltage										V
V_{IL}	Low (Note 3)		−2.0	0.8	−2.0	0.8	−2.0	0.8	−2.0	0.8	
V_{IH}	High		2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	
	Output voltage										V
V_{OL}	Low	$I_{OL} = 3.2mA$		0.4		0.4		0.4		0.4	
V_{OH}	High	$I_{OH} = -400\mu A$	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	
I_{LI}	Input load current	$0V \leq V_{IN} \leq 5.5V$		1		1		1		1	μA
I_{LO}	Output leakage	Chip deselected. $V_{OUT} = +0.4V$ to V_{CC}		5		5		5		5	μA
I_{CC}	Supply current	Chip deselected. $V_{CC} = 5.5V$, $V_{IN} = V_{CC}$		120		110		110		90	mA
	Capacitance (Note 4)										pF
C_{IN}	Input	$T_A = 25°C$, f = 1MHz, all pins except		7		7		7		7	
C_{OUT}	Output	pin under test tied to ground		10		10		10		10	

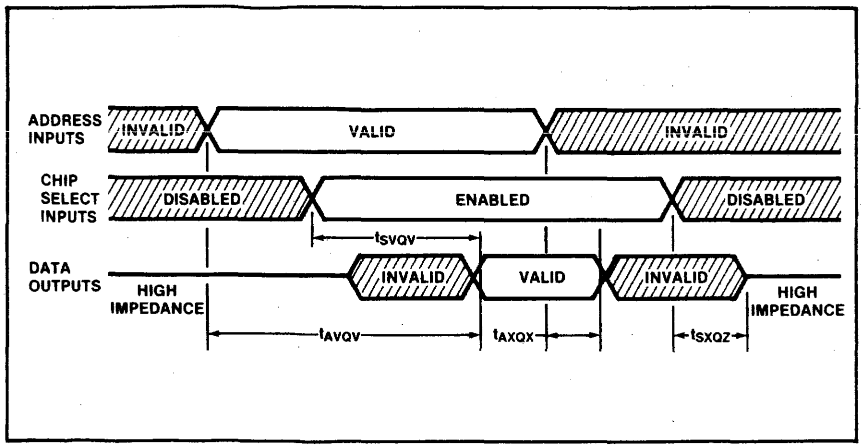
NOTES
3. Input levels that swing more negative than −2.0V may alter AC electrical characteristics.
4. This parameter is periodically sampled and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 5.0V \pm 10\%$

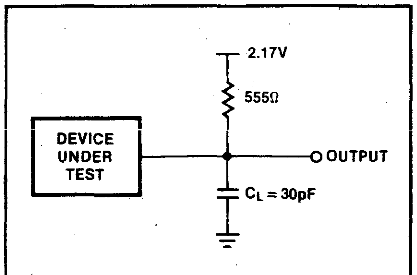
PARAMETER		-15		-20		UNIT
		Min	Max	Min	Max	
t_{AVQV}	Address access time		150		200	ns
t_{SVQV} (Note 5)	Chip select delay		100		100	ns
t_{SXQZ} (Note 6)	Chip deselect delay		75		100	ns
t_{AXQX}	Previous data valid after address change delay	0		0		ns

NOTES
5. t_{SVQV} is at value indicated, provided the valid address leads the chip select by (t_{AVQV}-t_{SVQV}) ns or more.
6. t_{SXQZ} is measured at $V_{OL} = 0.5V$ on the "0" to High-Z state transition, with AC test load connected to the output.

TIMING DIAGRAM



AC TEST LOAD



Input transition time ≤5ns
Input signal levels: 0.4V to 2.4V
Timing reference levels:
Input = 1.5V
Output = 0.6V and 2.2V

signetics

131,072-BIT STATIC MOS ROM (16,384×8) 23128-15/20

DESCRIPTION

This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

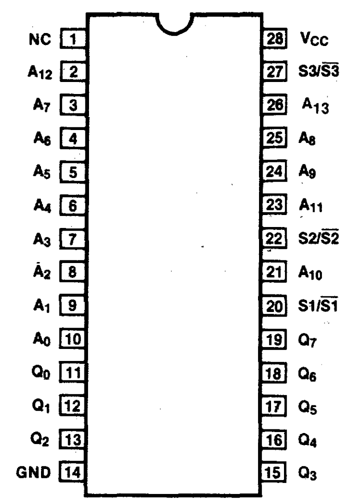
The three Chip Select inputs are programmable. Active-high or active-low level Chip Select input can can be defined by the designer and the desired chip select logic level is fixed during the masking process. The programmable Chip Select input, as well as OR-tie compatibility on the outputs, facilitates easy memory expansion.

The 23128 Read-Only Memory is fabricated with n-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits.

FEATURES

- **Fast access time**
- **Industry standard pinout — JEDEC approved**
- **Completely TTL compatible**
- **One +5V ±10% power supply**
- **Low power dissipation**
- **Three-state output — OR-tie capability**
- **Four programmable Chip Select inputs for easy memory expansion or no connection option**
- **Inputs protected — all inputs have protection against static charge**
- **27128 EPROM compatible**

PIN CONFIGURATION



TOP VIEW
PACKAGE AVAILABILITY
See Ordering Information

ABSOLUTE MAXIMUM RATINGS (Note 1)

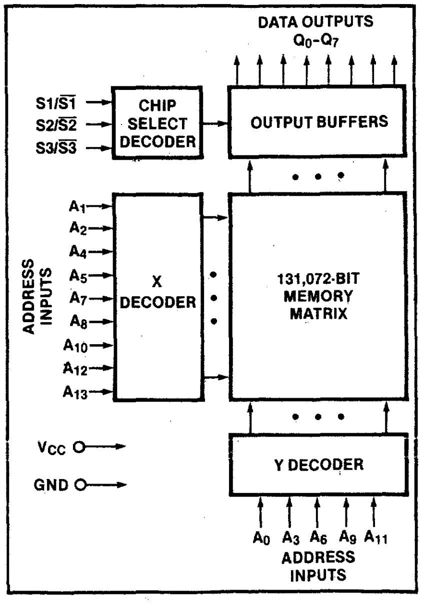
PARAMETER	RATING	UNIT
Operating Temperature 23128-XX	0 to +70	°C
23128E-XX	−40 to +85	°C
Storage Temperature	−65 to +150	°C
Voltage on Any Pin Relative to Ground	−2 to +7	V
Power Dissipation	1	Watt
Electrostatic Discharge Rating Relative to Ground (Note 2)	±2000	V

NOTES
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these any any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Test condition. Discharge 100pF through 1500 ohms, MIL-STD 883, method 3015.1.

PIN NAMES

A_0-A_{13}	Address Inputs
S1-S3	Chip Selects
Q_0-Q_7	Data Outputs
V_{CC}	Power
GND	Ground

BLOCK DIAGRAM



ORDERING INFORMATION

TEMPERATURE RANGE	PACKAGE TYPE	ORDER NUMBER BY ACCESS TIME	
		150ns*	200ns
0°C to +70°C	Plastic	23128-15N	23128-20N
0°C to +70°C	Ceramic	23128-15I	23128-20I
−40°C to +85°C	Plastic	23128E-15N	23128E-20N
−40°C to +85°C	Ceramic	23128E-15I	23128E-20I

*Preliminary

Signetics

MEMORY

131,072-BIT STATIC MOS ROM (16,384×8) — 23128-15/20

DC ELECTRICAL CHARACTERISTICS $V_{CC}=5.0V \pm 10\%$

PARAMETER		TEST CONDITIONS	23128E-15*		23128E-20		23128-15*		23128-20		UNIT
			Min	Max	Min	Max	Min	Max	Min	Max	
	Input voltage										V
V_{IL}	Low (Note 3)		–2.0	0.8	–2.0	0.8	–2.0	0.8	–2.0	0.8	
V_{IH}	High		2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	
	Output voltage										V
V_{OL}	Low	$I_{OL}=3.2mA$		0.4		0.4		0.4		0.4	
V_{OH}	High	$I_{OH}=-400\mu A$	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	
I_{LI}	Input load current	$0V \le V_{IN} \le 5.5V$		1		1		1		1	μA
I_{LO}	Output leakage	Chip deselected. $V_{OUT}=+0.4V$ to V_{CC}		5		5		5		5	μA
I_{CC}	Supply current	Chip deselected. $V_{CC}=5.5V$, $V_{IN}=V_{CC}$		120		120		110		100	mA
	Capacitance (Note 4)										pF
C_{IN}	Input	$T_A=25°C$, f = 1MHz, all pins except		7		7		7		7	
C_{OUT}	Output	pin under test tied to ground		10		10		10		10	

NOTES
3. Input levels that swing more negative than –2.0V may alter AC electrical characteristics.
4. This parameter is periodically sampled and is not 100% tested.

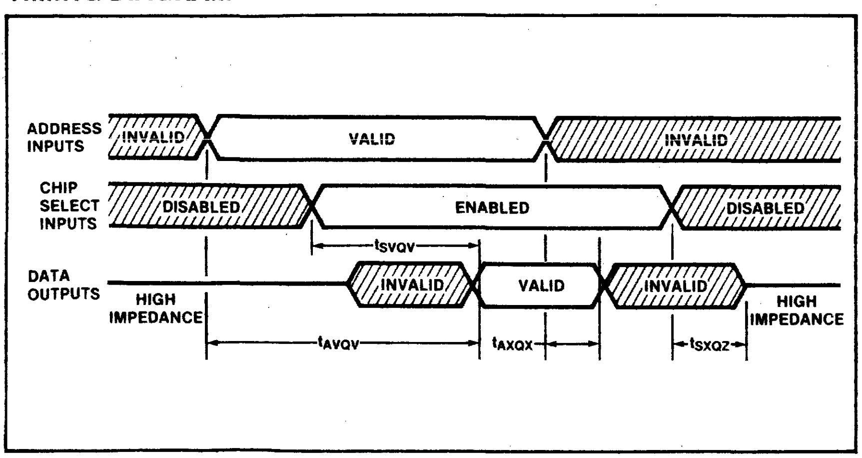
AC ELECTRICAL CHARACTERISTICS $V_{CC}=5.0V \pm 10\%$

PARAMETER		-15*		-20		UNIT
		Min	Max	Min	Max	
t_{AVQV}	Address access time		150		200	ns
t_{SVQV} (Note 5)	Chip select delay		100		100	ns
t_{SXQZ} (Note 6)	Chip deselect delay		75		100	ns
t_{AXQX}	Previous data valid after address change delay	0		0		ns

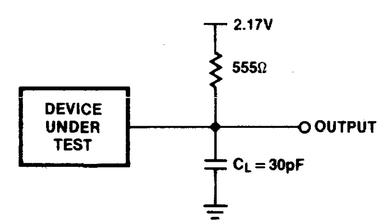
NOTES
5. t_{SVQV} is at value indicated, provided the valid address leads the chip select by (t_{AVQV}-t_{SVQV}) ns or more.
6. t_{SXQZ} is measured at $V_{OL}=0.5V$ on the "0" to High-Z state transition, with AC test load connected to the output.

*Preliminary

TIMING DIAGRAM



AC TEST LOAD



Input transition time ≤5ns
Input signal levels: 0.4V to 2.4V
~~Timing reference levels:~~
Input = 1.5V
Output = 0.6V and 2.2V

131,072-BIT STATIC MOS ROM (16,384×8) 23128/23128E/23128M

DESCRIPTION

This ROM is designed for memory applications where high performance, large bit storage, simple interfacing and wide operating temperature range are important design objectives.

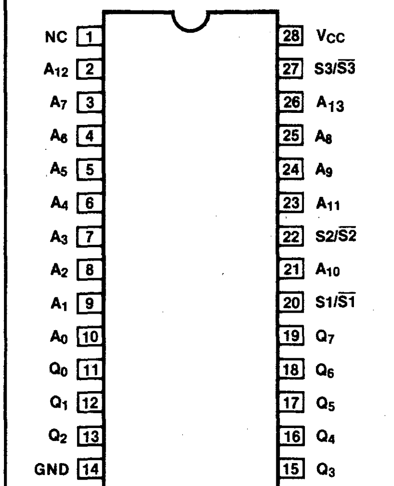
The Chip Select inputs are programmable. Active-high or active-low level Chip Select input can be defined by the designer and the desired chip select logic level is fixed during the masking process. The programmable Chip Select input, as well as OR-tie compatibility on the outputs, facilitates easy memory expansion.

The 23128 Read-Only Memory is fabricated with n-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits.

FEATURES

- **Fast access time**
  - **— 250ns max. 23128-25**
  - **— 300ns max. 23128M**
- **Industry standard pinout — JEDEC approved**
- **Completely TTL compatible**
- **Single +5V ±10% power supply**
- **Low power dissipation**
- **Three-state output — OR-tie capability**
- **Three programmable Chip Select inputs for easy memory expansion**
- **Inputs protected — all inputs have protection against static charge**
- **27128 compatible**

PIN CONFIGURATION



TOP VIEW

PACKAGE AVAILABILITY
See Ordering Information

ABSOLUTE MAXIMUM RATINGS (Note 1)

PARAMETER		RATING	UNIT
Operating Temperature	23128-XX	0 to +70	°C
	23128E-XX	−40 to +85	°C
	23128M-XX	−55 to +125	°C
Storage Temperature		−65 to +150	°C
Voltage on Any Pin Relative to Ground		−2 to +7	V
Power Dissipation		1	Watt
Electrostatic Discharge Rating Relative to Ground (Note 2)		±2000	V

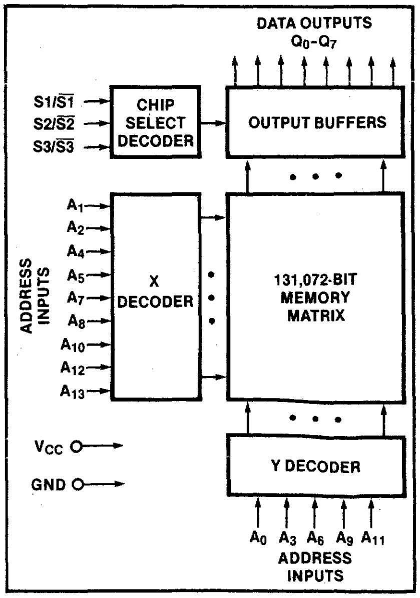
NOTES

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Test condition: Discharge 100pF through 1500ohm, MIL-STD-883, method 3015.1.

PIN NAMES

A_0-A_{13}	Address Inputs
S1-S3	Chip Selects
Q_0-Q_7	Data Outputs
V_{CC}	Power
GND	Ground

BLOCK DIAGRAM



ORDERING INFORMATION

TEMPERATURE RANGE	PACKAGE TYPE	ORDER NUMBER BY ACCESS TIME		
		250ns	300ns	450ns
0°C to +70°C	Plastic	23128-25N	23128-30N	23128-45N
0°C to +70°C	Ceramic	23128-25I	23128-30I	23128-45I
−40°C to +85°C	Plastic	23128E-25N	23128E-30N	23128E-45N
−40°C to +85°C	Ceramic	23128E-25I	23128E-30I	23128E-45I
−55°C to +125°C (Note 3)	Ceramic	23128M-25	23128M-30I	23128M-45I

NOTE

3. Also available processed to MIL-STD-883, Method 5004, Class B.

DC ELECTRICAL CHARACTERISTICS $V_{CC}=5.0V \pm 10\%$

PARAMETER		TEST CONDITIONS	23128E/M		23128-25		23128-30/45		UNIT
			Min	Max	Min	Max	Min	Max	
	Input voltage								V
V_{IL}	Low (Note 4)		−2.0	0.8	−2.0	0.8	−2.0	0.8	
V_{IH}	High		2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	
	Output voltage								V
V_{OL}	Low	$I_{OL}=3.2mA$		0.4		0.4		0.4	
V_{OH}	High	$I_{OH}=-400\mu A$	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	
I_{LI}	Input load current	$0V \leq V_{IN} \leq 5.5V$		1		1		1	μA
I_{LO}	Output leakage	Chip deselected. $V_{OUT}=+0.4V$ to V_{CC}		5		5		5	μA
I_{CC}	Supply current	Chip deselected. $V_{CC}=5.5V$, $V_{IN}=V_{CC}$		120		100		90	mA
	Capacitance (Note 5)								pF
C_{IN}	Input	$T_A=25°C$, f=1MHz, all pins except		7		7		7	
C_{OUT}	Output	pin under test tied to ground		10		10		10	

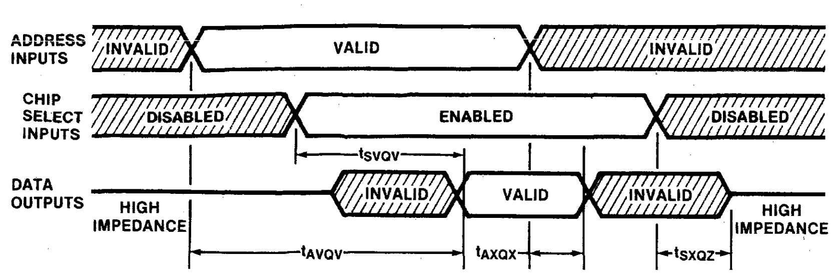
NOTES
4. Input levels that swing more negative than −2.0V may alter AC electrical characteristics.
5. This parameter is periodically sampled and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS $V_{CC}=5.0V \pm 10\%$

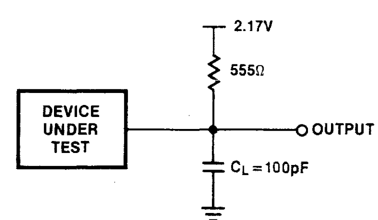
PARAMETER		-25		-30		-45		UNIT
		Min	Max	Min	Max	Min	Max	
t_{AVQV}	Address access time		250		300		450	ns
t_{SVQV} (Note 6)	Chip select delay		120		150		150	ns
t_{SXQZ} (Note 7)	Chip deselect delay		100		100		100	ns
t_{AXQX}	Previous data valid after address change delay	0		0		0		ns

NOTES
6. t_{SVQV} is at value indicated, provided the valid address leads the chip select by (t_{AVQV}-t_{SVQV}) ns or more.
7. t_{SXQZ} is measured at $V_{OL}=0.5V$ on the "0" to High-Z state transition, with AC TEST LOAD as shown below.

TIMING DIAGRAM



AC TEST LOAD



Input transition time ≤5ns
Input signal levels: 0.8V to 2V
Timing reference levels: Input = 1.5V
Output = 0.6V and 2.2V

Signetics

MEMORY

262,144-BIT STATIC MOS ROM (32,768×8) — 23256A

Preliminary

DESCRIPTION

The 23256A is a 262,144-bit read-only memory organized as 32,768 words by 8 bits. The pinout conforms to JEDEC standards for byte-wide memories.

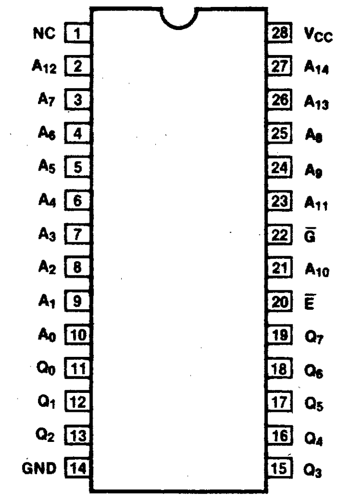
The 23256A is a fully static device; it goes into low power, standby mode when pin 20 ($\overline{E}$), is held high. Either $\overline{G}$ or $\overline{E}$ may be used for output control to eliminate bus contention.

The 23256A is fabricated using high performance n-channel silicon gate MOS technology.

FEATURES

- **Completely TTL compatible, 2 TTL loads**
- **Single +5V ±10% power supply**
- **Three-state outputs**
- **Fast access time — 200ns**
- **Fully static**
- **Low standby power**
- **JEDEC approved byte-wide pinout**
- **Inputs and outputs protected against static charge**

PIN CONFIGURATION



TOP VIEW

PACKAGE AVAILABILITY
See Ordering Information

ABSOLUTE MAXIMUM RATINGS (Note 1)

PARAMETER	RATING	UNIT
Operating Temperature	0 to +70	°C
Storage Temperature	−65 to +150	°C
Voltage on Any Pin Relative to Ground	−2 to +7	V
Power Dissipation	1	Watt
Electrostatic Discharge Rating Relative to Ground (Note 2)	±2000	V

NOTES
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Test condition. Discharge 100pF through 1500 ohms, MIL-STD 883, method 3015.1.

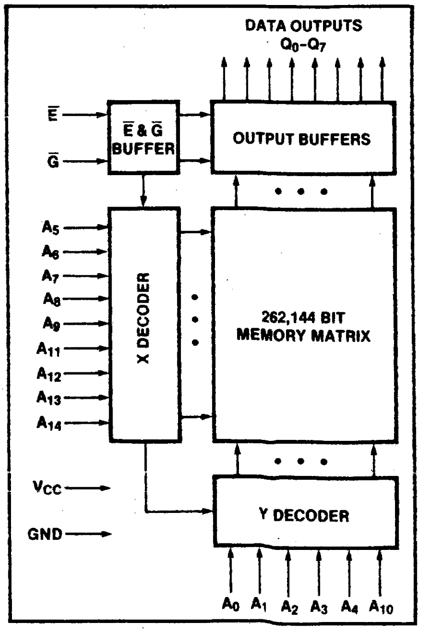
PIN NAMES

A_0-A_{14}	Address Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
Q_0-Q_7	Data Outputs
V_{CC}	Power
GND	Ground
NC	Not Connected

ORDERING INFORMATION

TEMPERATURE RANGE	PACKAGE TYPE	ORDER NUMBER BY ACCESS TIME			
		200ns	250ns	300ns	450ns
0°C to +70°C	Plastic	23256A-20N	23256A-25N	23256A-30N	23256A-45N

BLOCK DIAGRAM



262,144-BIT STATIC MOS ROM (32,768 × 8) 23256A

Preliminary

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 5.0V \pm 10\%$

PARAMETER	TEST CONDITIONS	Min	Max	UNIT
Input voltage V_{IL} Low (Note 3) V_{IH} High		−2.0 2.0	0.8 V_{CC}	V V
Output voltage V_{OL} Low V_{OH} High	$I_{OL} = 3.2mA$ $I_{OH} = -400\mu A$	 2.4	0.4 V_{CC}	V V
I_{LI} Input load current	$0V \leq V_{IN} \leq 5.5V$		1	μA
I_{LO} Output leakage			5	μA
Supply current I_{CC} Active I_{CCZ} Standby	Output unloaded $\overline{E} = V_{IH}$		90 10	mA mA
Capacitance (Note 4) C_{IN} Input C_{OUT} Output	$T_A = 25°C$, f = 1MHz All pins except pin under test tied to ground		7 12	pF pF

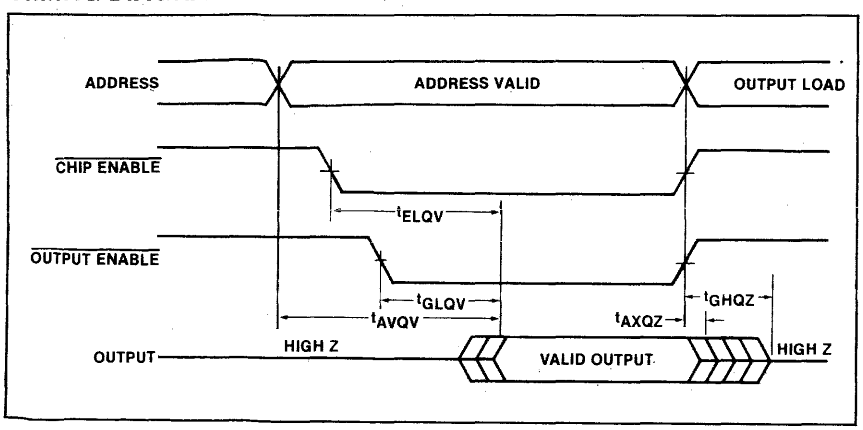
NOTES
3. Input levels that swing more negative than −2.0V may alter AC electrical characteristics.
4. This parameter is periodically sampled and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 5.0V \pm 10\%$

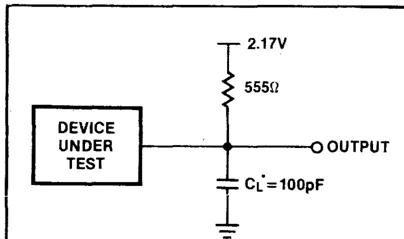
PARAMETER		-20		-25		-30		-45		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{AVQV}	Address access time		200		250		300		450	ns
t_{ELQV}	Chip enable to output delay		200		250		300		450	ns
t_{GLQV}	Output enable to output valid delay (Note 5)		100		120		150		180	ns
t_{EHQZ} t_{GHQZ}	Chip disable delay (Note 6)		100		100		120		150	ns
t_{AXQZ}	Previous data valid after address change delay	0		0		0		0		ns

NOTES
5. t_{ELQV} is at value indicated provided the valid address leads output enable by $(t_{AVQV} - t_{GLQV})$ ns.
6. t_{EHQZ} and t_{GHQZ} are measured at $V_{OL} = 0.5V$ on the "0" to High-Z state transition with load as shown below connected to output.

TIMING DIAGRAM



AC TEST LOAD



Input transition time ≤5ns
Input signal levels: 0.4V to 2.4V
Timing reference levels:
Input = 1.5V
Output = 0.6V and 2.2V
*for 23256A-20 C_L = 30pF.

65,536-BIT STATIC MOS ROM (TWO 4096×8 BANKS) — 26S64-30/45

DESCRIPTION

The 26S64 is a mask-programmable, 8192 words by 8 bits Read-Only Memory, partitioned into two banks of 4096 words by 8 bits. Each half can be accessed by a 12-bit address, A_0 through A_{11}, and switching from one bank to the other is effected by a pair of bank-select addresses, FF8 and FF9. The address FF8 accesses the bank containing locations 0000 through 0FFF, and FF9 accesses the bank containing locations 1000 through 1FFF. The bank-select locations, 1FF8 and 0FF9, must be programmed with a no-operation (NOP) instruction.

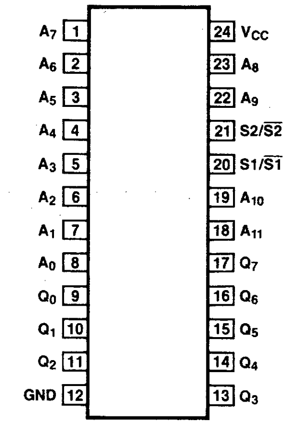
The 26S64 has two user-programmable chip selects, along with three-state outputs, allowing easy memory expansion. It is suitable for applications where 12 address lines must be used to access 8192 words of memory, the 13th address bit is internally generated and latched, in response to bank select address FF8 or FF9.

The 26S64 is manufactured with n-channel silicon gate MOS technology, and all inputs and outputs are TTL compatible.

FEATURES

- **Fast access time**
- **Organized as two 4K × 8 banks**
- **Access 8K bytes with 4K system address capability**
- **Industry standard pinout**
- **Low power dissipation**
- **TTL compatible inputs and outputs**
- **Single +5V ±10% power supply**
- **Three-state outputs — OR-tie capability**
- **Electrostatic discharge protection**

PIN CONFIGURATION



TOP VIEW

PACKAGE AVAILABILITY

See Ordering Information

ABSOLUTE MAXIMUM RATINGS (Note 1)

PARAMETER	RATING	UNIT
Operating Temperature	0 to +70	°C
Storage Temperature	−65 to +150	°C
Voltage on Any Pin Relative to Ground	−2 to +7	V
Power Dissipation	1	Watt
Electrostatic Discharge Rating Relative to Ground (Note 2)	±2000	V

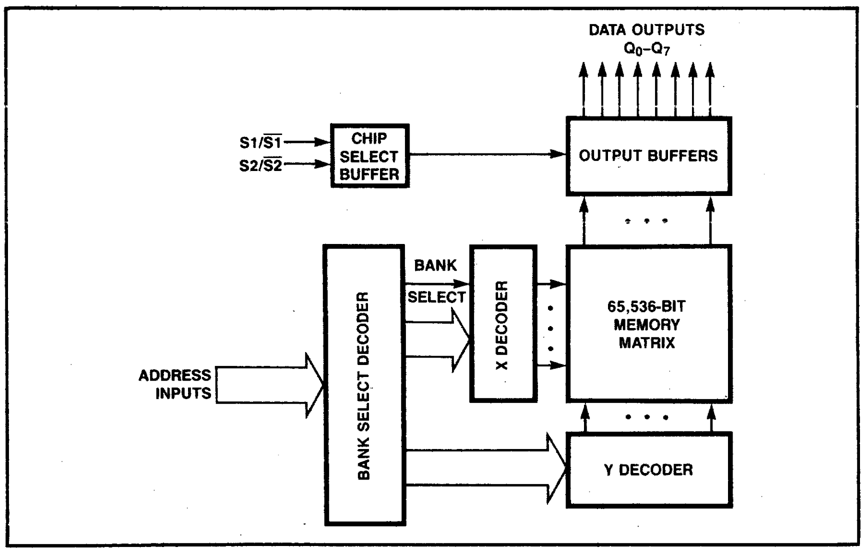
NOTES

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these any any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Test condition. Discharge 100pF through 1500 ohms, MIL-STD 883, method 3015.1.

PIN NAMES

A_0–A_{11}	Address inputs
Q_0–Q_7	Data outputs
S1/S2	Chip selects
V_{CC}/GND	Power/ground

BLOCK DIAGRAM



ORDERING INFORMATION

TEMPERATURE RANGE	PACKAGE TYPE	ORDER NUMBER BY ACCESS TIME	
		300ns	450ns
0°C to +70°C	Plastic	26S64-30N	26S64-45N
0°C to +70°C	Cerdip	26S64-30F	26S64-45F

65,536-BIT STATIC MOS ROM (TWO 4096×8 BANKS) 26S64-30/45

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 5.0V \pm 10\%$

PARAMETER		TEST CONDITIONS	26S64 Min	26S64 Max	UNIT
	Input voltage				V
V_{IL}	Low (Note 3)		−2.0	0.8	
V_{IH}	High		2.0	V_{CC}	
	Output voltage				V
V_{OL}	Low	$I_{OL} = 1.6mA$		0.4	
V_{OH}	High	$I_{OH} = -100\mu A$	2.4	V_{CC}	
I_{LI}	Input load current	$0V \le V_{IN} \le 5.5V$			μA
I_{LO}	Output leakage	Chip deselected. $V_{OUT} = +0.4V$ to V_{CC}		5	μA
I_{CC}	Supply current	Chip deselected. $V_{CC} = 5.5V$, $V_{IN} = V_{CC}$		100	mA
	Capacitance (Note 4)				pF
C_{IN}	Input	$T_A = 25°C$, f = 1MHz, all pins except pin under test tied to ground		7	
C_{OUT}	Output			10	

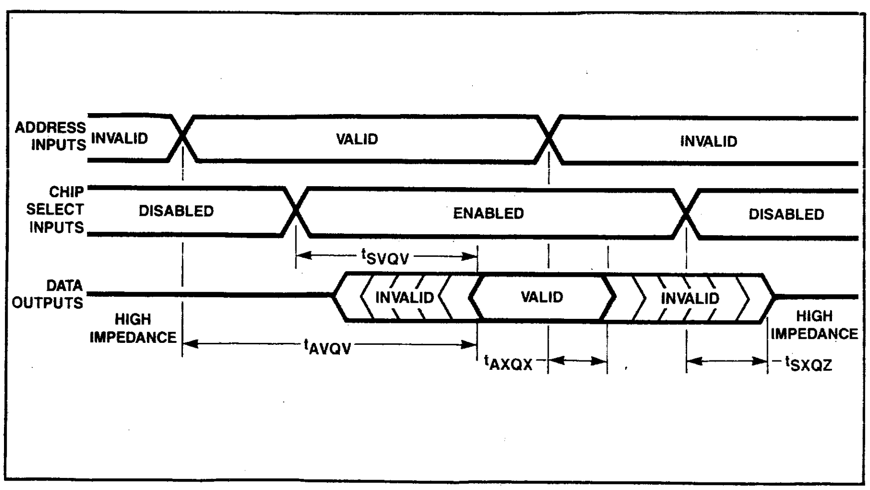
NOTES
3. Input levels that swing more negative than −2.0V may alter AC electrical characteristics.
4. This parameter is periodically sampled and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 5.0V \pm 10\%$

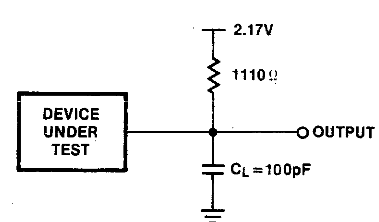
PARAMETER		26S64-30 Min	26S64-30 Max	26S64-45 Min	26S64-45 Max	UNIT
t_{AVQV}	Address access time (Note 5)		300		450	ns
t_{SVQV}	Chip select delay (Note 6)		120		150	ns
t_{SXQZ}	Chip deselect delay (Note 7)		100		100	ns
t_{AXQX}	Previous data valid after address change delay	0		0		ns

NOTES
5. Following a change of banks, at least two times t_{AVQV} must elapse before a valid access may be exercised.
6. t_{SVQV} is at value indicated, provided the valid address leads the chip select by (t_{AVQV}-t_{SVQV}) ns or more.
7. t_{SXQZ} is measured at $V_{OL} = 0.5V$ on the "0" to High-Z state transition, with AC test load connected to the output.
8. Bank select can be effected only while chip is selected, and bank switch address is held valid for at least 100ns.
9. At power-up the 26S64 may come up in either bank; proper initialization is required.

TIMING DIAGRAM



AC TEST LOAD



Input transition time ≤ 5ns
Input signal levels: 0.8V to 2V
Timing reference levels: Input = 1.5V
Output = 0.6V and 2.2V

Rotating Memory Integrated Circuit Capabilities

Silicon Systems is a semiconductor company dedicated primarily to the design and production of "application specific" integrated circuits. SSi sometimes works closely with a group of equipment manufacturers to develop an IC. Often these IC's become the "standard products" of the industry. Such is the case with Silicon Systems' family of read/write IC's for the rotating memory market.

SSi's first read/write Winchester IC developed in 1976

In 1976 Silicon Systems developed its first read/write monolithic bipolar integrated circuit for the IBM 3350 Winchester disk drive PCM (plug-compatible memory) market. Called the SSi 104, it integrated all of the required read, write, control, and data protection functions on one chip. Assembled in a flat pack, the device could be mounted directly on the head-arm assembly. The SSi 104 soon became the industry standard.

A broad line of Rotating Memory IC's

SSi now has several varieties of read/write products including the SSi 115 with 2, 4, or 5 channels, the SSi 117 with 4 to 6 channels, and the SSi 501 with 8 channels. For thin-film-head applications, SSi has the 4-channel SSi 114. SSi also has servo preamps including the SSi 101 for ferrite-head drives and the SSi 116 for thin-film-head drives. SSi has defined a floppy-disk read/write IC, the soon-to-be released SSi 570.

IC's for streamers, tape drives, and controllers, too

If you don't see the product you need, it may be on our standard product list soon. We serve the disk drive market more completely than anyone else with our standard line of circuits, and we have also developed a score of custom IC's of various designs and functions for the rotating memory market: IC's for spindle control, data paths, IC's for data separation and controllers too. So, if the exact circuit you need isn't already in our line — we have the technology and experience to make a custom chip for you.

SSI PRODUCT SELECTOR GUIDE DISK DRIVE CIRCUITS

Part No.	Circuit Function	No. of Channels	Power Supplies	Logic Type	Data Write/Read	Write Current Source	Write Unsafe Indicator	Write Read Gain	Special Feature
FERRITE									
SSI 101	Servo Preamp	N/A	8.3V 10V	—	—	—	—	77 to 110	Min BW 10 MHz
SSI 104	Read/Write Amp	4	+6V −4V	ECL	Bi-Directional Differential	External	Low for Write Unsafe	28 to 43	
SSI104L	Read/Write Amp	4	+6V −4V	ECL	Bi-Directional Differential	External	Low for Write Unsafe	28 to 43	Low Noise (1.7nV/$\sqrt{Hz}$)
SSI 108	Read/Write Amp	4	+6V −4V	ECL	Bi-Directional Differential	External	Low for Write Unsafe	28 to 43	24 pin DIP opt 104
SSI 115	Read/Write Amp	2,4,5	±5V	TTL	Bi-Directional Differential	External	Low for Write Unsafe	26 to 52	Write Current Diverter in Read Mode
SSI 117	Read/Write Amp	4,6	+5V +12V	TTL	TTL Write Diff. Read	On-Chip	Low for Write Safe	80 to 120	"OEM" supplies
SSI 122	Read/Write Amp	4	+6V −4V	ECL	Bi-Directional Differential	External	Low for Write Unsafe	28 to 43	22 pin DIP opt 104
SSI 501	Read/Write Amp	8	+5V +12V	TTL	TTL Write Diff. Read	On-Chip	Low for Write Safe	80 to 120	"OEM" supplies
THIN-FILM									
SSI 114	Read/Write Amp	4	±5V	TTL	Diff. Write Diff. Read	On-Chip	Low for Write Safe	75 to 120	Sep. Read/Write Bus, Write Safe Verify output
SSI 116	Servo Preamp	N/A	8.3V	—	—	—	—	200 to 310	Min BW 20 MHz
TAPE DRIVE									
SSI 8500	CRC Character Generator	—	—	—	—	—	—	—	—
SSI 8502	LRC Character Generator	—	—	—	—	—	—	—	—
SSI 8520	Queue/Deskew Register	—	—	—	—	—	—	—	—
FLOPPY READ/WRITE									
SSI 570	Read/Write System	2	+5V +12V	TTL	—	On-Chip	—	—	—

Note: On-Chip Write Current Sources are programmed with an External Resistor.

Silicon Systems® incorporated
14351 Myford Road, Tustin, California 92680 (714) 731-7110, TWX 910-595-2809

ABBREVIATIONS OF COMPANY NAMES

Action Ins	Action Instruments
AD	Analog Devices
ADT	Advanced Digital Technology
Advent	Advent Products, Inc.
Alphatron	Alphatron
AMA	American Automation
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
Amperex	Amperex Electronic Corp.
Analogic	Analogic
Analog Sys	Analog Systems
APC	Applied Micro Circuits
Apex	Apex Microtechnology
APM	Applied Microsystems Corp.
Appl Sys	Applied Systems Corp.
APT	Applied Microtechnology
Aptek	Aptek Microsystems
Array Tech	Array Technology
AWI	AWI Electronics
Barvon	Barvon Research
Bedford	Bedford Computer Systems Inc.
Burr-Brown	Burr-Brown
CAE	Computer Aided Engineering
Cal Devices	California Devices
Cermetek	Cermetek
CGRS	CGRS Microtech Inc.
Cherry	Cherry Semiconductor
CIC	Custom Integrated Circuits
CirTech	Circuit Technology
Citel	Citel
Comlinear	Comlinear Corporation
CMA	Custom MOS Arrays
Comark	Comark Corp.
Comdial	Comdial Semiconductor
Comp Auto	Computer Automation
Compas	Compas Microsystems
Cont Logic	Control Logic Inc.
Control Sys	Control Systems Microsystems Div.
CreMicro	Creative Micro Systems
Cromemco	Cromemco, Inc.
Cubit	Cubit Inc.
Curtis	Curtis Electro Devices, Inc.
Cybernetic	Cybernetic Micro Systems
Cybersys	Cybersystems
Cybertek	Cybertek Inc.
Data General	Data General
Data I/O	Data I/O
Data Trans	Data Translation
Datel	Datel
Datricon	Datricon Corporation
DDC	Data Devices Corporation
DEC	Digital Equipment Corporation
Die-Tech	Die-Tech
Digelec	Digelec Corp.
Digitek	Digitek, Inc.
Dionics	Dionics Inc.
Dist Comp	Distributed Computer Systems
Divers Tech	Diversified Technology
E-HI	E-H International, Inc.
EDI	Electronic Designs Inc.
Elind	Elind Elettronica Industriale
EMM-SESCO	EEM-SESCO
Emulogic	Emulogic Inc.
ETI Micro	ETI Micro
Exar	Exar Integrated Systems
Exel	Exel Microelectronics
Fairchild	Fairchild
Ferranti	Ferranti Electric
Force	Force Computers
Fujitsu A	Fujitsu America
Fujitsu	Fujitsu Microelectronics, Inc.
GI	General Instrument
GTE Micro	GTE Microcircuits
Harris	Harris Semiconductor
Heurikon	Heurikon Corp.
Hilevel	Hilevel Technology, Inc.
Hitachi	Hitachi America, Ltd.
Holt	Holt Inc.
HP	Hewlett-Packard
Hughes	Hughes Aircraft, Solid State Products
Hybrid Sys	Hybrid Systems
HyComp	HyComp
ICC	International Cybernetics
IDT	Integrated Device Technology
IMI	International Microcircuits, Inc.
IMP	International Microelectronic Products
IMS	Industrial MicroSystems Inc.
Infosphere	Infosphere
Inmos	Inmos
IntCirEng	Integrated Circuit Engineering
IntCirSys	Integrated Circuit Systems
IntCompSys	Integrated Computer Systems
Int Tech	Integrated Technology Corp.
Intech	Intech Microcircuits Div.
Intel	Intel
Interdesign	Interdesign
Intersil	Intersil
Intronics	Intronics
ITT	ITT Semiconductors
Kinetic Sys	Kinetic Systems
Kontron	Kontron Electronics
Lambda	Lambda Semiconductor
Linear Tech	Linear Technology
LSI Comp	LSI Computer Systems
LSI Logic	LSI Logic Corporation
Master Logic	Master Logic Corporation
Matrix	Matrix Corp.
Matrox	Matrox Electronic Systems
Maxim	Maxim Integrated Products
MCC	Micro-Computer Control
MCE	MCE Electronics
Micrel	Micrel
Micro Innov	Micro Innovators
Micropac	Micropac Industries
Micro Net	Micro Networks
Micro Pwr	Micro Power Systems
Micro Sci	Micro Sciences Corp.
Micro Tech	Microcircuits Technology
Micro-Link	Micro-Link Corporation
Micron	Micron Technology
MilerTron	MilerTronics
Miller	Miller Technology
Mitel	Mitel Semiconductor
Mitsubishi	Mitsubishi Electronics
MMI	Monolithic Memories, Inc.
Mostek	Monolithic Systems Corp.
Motorola	Mostek
MRC	Motorola Semiconductor
Murray	MRC Systems
Monosil	Murray Consulting
National	National Semiconductor
NCM	NCM Corp.
NCR	NCR Corp., Microelectronics Division
NEC	NEC Electronics
Nitron	Nitron
OAE	Oliver Advanced Engineering
Octagon	Octagon Systems Corp.
OEI	Optical Electronics Inc.
Ohio Sci	Ohio Scientic
OKI	OKI Semiconductor
Omnibyte	Omnibyte Corp.
Onset	Onset Computer Corp.
Panasonic	Panasonic
Pico Design	Pico Design
Polycore	Polycore Electronics
Plessey	Plessey Semiconductors
PMI	Precision Monilithics, Inc.
PragDes	Pragmatic Design Inc.
Pro-Log	Pro-Log Corp.
Quay	Quay Corp.
Raytheon	Raytheon Semiconductor
RCA	RCA Solid State Division
RCI Data	RCI Data
RELMS	Relational Memory Systems
Reticon	Reticon
RIFA	RIFA
Rockwell	Rockwell, Microelectronic Devices
RTC	Riehl Time Corporation
Sanyo	Sanyo
SBE	SBE, Inc.
SEEQ	SEEQ Technology, Inc.
SPI	Semi Processes Inc.
Siemens	Siemens
Si-Fab	Si-Fab
Signetics	Signetics
SGS	SGS Semiconductor
Sharp	Sharp
Silicon G	Silicon General
Siliconix	Siliconix
Silicon Sys	Silicon Systems Inc.
Siltronics	Siltronics
SMC	Standard Microsystems Corp.
S MOS	S MOS Systems
Solarise	Solarise Enterprises
Solitron	Solitron Devices
Sprague	Sprague Electric Company
SSM	Solid State Micro Technology for Music
SSS	Solid State Scientific
Stag	Stag Microsystems
STC	Storage Technology Corp.
STD	STD Microsystems
Struc Des	Structured Design Inc.
Stynetic	Stynetic Systems
Sunrise	Sunrise Electronics
Sunshine	Sunshine Semiconductor
Supertex	Supertex Inc.
Symtek	Symtek Corp.
Synertek	Synertek
Sys Innov	Systems Innovations
Tau Zero	Tau Zero Inc.
Technitrol	Technitrol
Tektronix	Tektronix
Teledyne C	Teledyne Crystalonics
Teledyne P	Teledyne Philbrick
Teledyne S	Teledyne Semiconductor
Telefunken	Telefunken
Telmos	Telmos
Teltone	Teltone Corporation
TI	Texas Instruments
Third Domain	Third Domain
Thomson-CSF	Thomson-CSF Components Corp.
Toshiba	Toshiba America
Trans-Data	Trans-Data
TRW	TRW LSI Products
Unitrode	Unitrode
Universal	Universal Semiconductor, Inc.
Varix	Varix Corp.
VLSI Design	VLSI Design Associates
VTI	VLSI Technology, Inc.
Votrax	Votrax
Weitek	Weitek Corporation
Western	Western Digital
Wintek	Wintek Corp.
Xicor	Xicor, Inc.
Xycom	Xycom
Zendex	Zendex Corp.
Zilog	Zilog
ZyMOS	ZyMOS Corporation
Zytrex	Zytrex Corp.

RAM Selection Guide

Commercial $T_A = 0°C$ to $70°C$)

Part Number	Organization	Access Time (ns)	Maximum Current (mA) Operating	Maximum Current (mA) Standby	Power Supply (Volts)	Number of Pins	Package Type (Note 1)
SY2101-1	256 x 4	500	70	--	+5	22	C, P
SY2101A	256 x 4	350	55	--	+5	22	C, P
SY2101A-2	256 x 4	250	55	--	+5	22	C, P
SY2101A-4	256 x 4	450	55	--	+5	22	C, P
SY2111-1	256 x 4	500	70	--	+5	18	C, D, P
SY2111A	256 x 4	350	55	--	+5	18	C, D, P
SY2111A-2	256 x 4	250	55	--	+5	18	C, D, P
SY2111A-4	256 x 4	450	55	--	+5	18	C, D, P
SY2112-1	256 x 4	500	70	--	+5	16	C, D, P
SY2112A	256 x 4	350	55	--	+5	16	C, D, P
SY2112A-2	256 x 4	250	55	--	+5	16	C, D, P
SY2112A-4	256 x 4	450	55	--	+5	16	C, D, P
SY2114AL-1	1024 x 4	100	40	--	+5	18	C, D, P
SY2114AL-2	1024 x 4	120	40	--	+5	18	C, D, P
SY2114AL-3	1024 x 4	150	40	--	+5	18	C, D, P
SY2114AL-4	1024 x 4	200	40	--	+5	18	C, D, P
SY2114A-4	1024 x 4	200	70	--	+5	18	C, D, P
SY2114A-5	1024 x 4	250	70	--	+5	18	C, D, P
SY2148H	1024 x 4	70	150	30	+5	18	C, D, P
SY2148H-2	1024 x 4	45	150	30	+5	18	C, D, P
SY2148H-3	1024 x 4	55	150	30	+5	18	C, D, P
SY2148HL	1024 x 4	70	125	20	+5	18	C, D, P
SY2148HL-3	1024 x 4	55	125	20	+5	18	C, D, P
SY2149H	1024 x 4	70	150	--	+5	18	C, D, P
SY2149H-2	1024 x 4	45	150	--	+5	18	C, D, P
SY2149H-3	1024 x 4	55	150	--	+5	18	C, D, P
SY2149HL	1024 x 4	70	125	--	+5	18	C, D, P
SY2149HL-3	1024 x 4	55	125	--	+5	18	C, D, P
SY2147H-2	4096 x 1	45	180	30	+5	18	C, D, P
SY2147H-3	4096 x 1	55	180	30	+5	18	C, D, P
SY2147H	4096 x 1	70	160	20	+5	18	C, D, P
SY2147HL-3	4096 x 1	55	125	15	+5	18	C, D, P
SY2147HL	4096 x 1	70	140	10	+5	18	C, D, P
SY2158-2	1024 x 8	120	100	30	+5	24	P
SY2158-3	1024 x 8	150	100	30	+5	24	P
SY2158-4	1024 x 8	200	100	30	+5	24	P
SY2159-2	1024 x 8	120	100	--	+5	24	P
SY2159-3	1024 x 8	150	100	--	+5	24	P
SY2159-4	1024 x 8	200	100	--	+5	24	P
SY2128-1	2048 x 8	100	100	20	+5	24	K, C, D, P
SY2128-2	2048 x 8	120	100	20	+5	24	K, C, D, P
SY2128-3	2048 x 8	150	100	20	+5	24	K, C, D, P
SY2128-4	2048 x 8	200	100	20	+5	24	K, C, D, P
SY2128L-1	2048 x 8	100	80	15	+5	24	K, C, D, P
SY2128L-2	2048 x 8	120	80	15	+5	24	K, C, D, P
SY2128L-3	2048 x 8	150	80	15	+5	24	K, C, D, P
SY2128L-4	2048 x 8	200	80	15	+5	24	K, C, D, P
SY2129-1	2048 x 8	100	100	--	+5	24	K, C, D, P
SY2129-2	2048 x 8	120	100	--	+5	24	K, C, D, P
SY2129-3	2048 x 8	150	100	--	+5	24	K, C, D, P
SY2129-4	2048 x 8	200	100	--	+5	24	K, C, D, P
SY2129L-1	2048 x 8	100	80	--	+5	24	K, C, D, P
SY2129L-2	2048 x 8	120	80	--	+5	24	K, C, D, P
SY2129L-3	2048 x 8	150	80	--	+5	24	K, C, D, P
SY2129L-4	2048 x 8	200	80	--	+5	24	K, C, D, P
SY2168 [2]	4096 x 4	70	120	30	+5	20	C, D, P
SY2168-3 [2]	4096 x 4	55	120	30	+5	20	C, D, P
SY2169 [2]	4096 x 4	70	120	--	+5	20	C, D, P
SY2169-3 [2]	4096 x 4	55	120	--	+5	20	C, D, P
SY2167 [2]	16,384 x 1	70	120	30	+5	20	C, D, P
SY2167-3 [2]	16,384 x 1	55	120	30	+5	20	C, D, P
SY2130 [2]	1024 x 8	100	170	40	+5	48	C, D, P
SY2131 [2]	1024 x 8	100	170	—	+5	48	C, P

NOTES: 1. C = Ceramic, D = Cerdip, P = Plastic, K = Leadless Chip Carrier.
2. Preliminary Information (new product).

ROM Selection Guide

Commercial: T_A = 0° C to +70° C

Part Number	Organization	Access Time (ns) Max.	Maximum Current (mA)		Power Supply (Volts)	Number of Pins	Package Type (Note 1)	Compatible EPROM/PROM
			Operating	Standby				
SY3308	1024 x 8	70	120	—	+5	24	C, D, P, K	82S181
SY3308R	1024 x 8	35[3]	130	—	+5	24	C, D, P, K	27S35
SY2316B	2048 x 8	450	98	—	+5	24	C, D, P	2716
SY2316B-2	2048 x 8	200	98	—	+5	24	C, D, P	2716
SY2316B-3	2048 x 8	300	98	—	+5	24	C, D, P	2716
SY3316	2048 x 8	80	120	—	+5	24	C, D, P, K	82S191
SY3316A	2048 x 8	80	120	20	+5	24	C, D, P, K	82S191
SY3316R	2048 x 8	35[3]	130	—	+5	24	C, D, P, K	27S45
SY2332	4096 x 8	450	100	—	+5	24	C, D, P	TMS2532
SY2332-2	4096 x 8	200	100	—	+5	24	C, D, P	TMS2532
SY2332-3	4096 x 8	300	100	—	+5	24	C, D, P	TMS2532
SY2333	4096 x 8	450	100	—	+5	24	C, D, P	2732/A
SY2333-2	4096 x 8	200	100	—	+5	24	C, D, P	2732/A
SY2333-3	4096 x 8	300	100	—	+5	24	C, D, P	2732/A
SY2364	8192 x 8	450	100	—	+5	24	C, D, P	TMS2564
SY2364-2	8192 x 8	200	100	—	+5	24	C, D, P	TMS2564
SY2364-3	8192 x 8	300	100	—	+5	24	C, D, P	TMS2564
SY2364A	8192 x 8	450	100	12	+5	24	C, D, P	TMS2564
SY2364A-2	8192 x 8	200	100	12	+5	24	C, D, P	TMS2564
SY2364A-3	8192 x 8	300	100	12	+5	24	C, D, P	TMS2564
SY2365	8192 x 8	450	100	—	+5	28	C, D, P	2764
SY2365-2	8192 x 8	200	100	—	+5	28	C, D, P	2764
SY2365-3	8192 x 8	300	100	—	+5	28	C, D, P	2764
SY2365A	8192 x 8	450	100	12	+5	28	C, D, P	2764
SY2365A-2	8192 x 8	200	100	12	+5	28	C, D, P	2764
SY2365A-3	8192 x 8	300	100	12	+5	28	C, D, P	2764
SY23128-2	16,384 x 8	200	100	—	+5	28	C, D, P	27128
SY23128-3	16,384 x 8	300	100	—	+5	28	C, D, P	27128
SY23128	16,384 x 8	450	100	—	+5	28	C, D, P	27128
SY23128A-2	16,384 x 8	200	100	10	+5	28	C, D, P	27128
SY23128A-3	16,384 x 8	300	100	10	+5	28	C, D, P	27128
SY23128A	16,384 x 8	450	100	10	+5	28	C, D, P	27128
SY23130	16,384 x 8	450	100	—	+5	28	C, D, P	—
SY23130-2	16,384 x 8	200	100	—	+5	28	C, D, P	—
SY23130-3	16,384 x 8	300	100	—	+5	28	C, D, P	—
SY23130A	16,384 x 8	450	100	10	+5	28	C, D, P	—
SY23130A-2	16,384 x 8	200	100	10	+5	28	C, D, P	—
SY23130A-3	16,384 x 8	300	100	10	+5	28	C, D, P	—
SY23256-2	32,768 x 8	200	100	—	+5	28	C, D, P	27256
SY23256-3	32,768 x 8	300	100	—	+5	28	C, D, P	27256
SY23256	32,768 x 8	450	100	—	+5	28	C, D, P	27256
SY23256A-2	32,768 x 8	200	100	10	+5	28	C, D, P	27256
SY23256A-3	32,768 x 8	300	100	10	+5	28	C, D, P	27256
SY23256A	32,768 x 8	450	100	10	+5	28	C, D, P	27256
SY6364[2]	8192 x 8	200	70	1mA/10μA[4]	+5	24	C, D, P	
SY6365[2]	8192 x 8	200	70	1mA/10μA[4]	+5	28	C, D, P	

NOTES:
1. C = Ceramic, D = Cerdip, P = Plastic, K = Leadless Chip Carrier.
2. Preliminary information.
3. Effective Access Time (t_{CPA}).
4. $\overline{CE}$ @ 2V/$\overline{CE}$ @ V_{CC}.

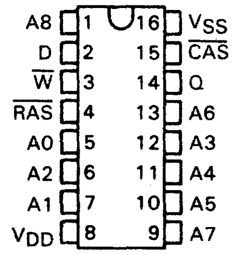
TMS4256, TMS4257
262,144-BIT DYNAMIC RANDOM-ACCESS MEMORIES

MAY 1983

- 262,144 X 1 Organization
- Single +5-V Supply (10% Tolerance)
- JEDEC Standardized Pin Out
- Upward Pin Compatible with TMS4164 (64K Dynamic RAM)
- Performance Ranges:

DEVICE	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TMS4256-10 TMS4257-10	100 ns	50 ns	200 ns
TMS4256-12 TMS4257-12	120 ns	60 ns	230 ns
TMS4256-15 TMS4257-15	150 ns	75 ns	260 ns
TMS4256-20 TMS4257-20	200 ns	100 ns	330 ns

TMS4256, TMS4257 . . . JL OR NL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{\text{CAS}}$	Column Address Strobe
D	Data-In
Q	Data-Out
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{W}}$	Write Enable
V_{DD}	+5-V Supply
V_{SS}	Ground

- Long Refresh Period . . . 4 ms (MAX)
- Low Refresh Overhead Time . . . As Low As 1.3% of Total Refresh Period
- On-Chip Substrate Bias Generator
- All Inputs, Outputs, and Clocks Fully TTL Compatible
- 3-State Unlatched Output
- Common I/O Capability with "Early Write" Feature
- Page ('4256) or Nibble-Mode ('4257) Options for Faster Access Operation
- Low Power Dissipation:
  Operating . . . 200 mW (TYP)
  Standby . . . 16.5 mW (TYP)
- $\overline{\text{RAS}}$ Only Refresh Mode
- Hidden Refresh Mode

description

The '4256 and '4257 are high-speed, 262,144-bit dynamic random-access memories, organized as 262,144 words of one bit each. They employ state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon gate technology for very high performance combined with low cost and improved reliability.

These devices feature maximum $\overline{\text{RAS}}$ access times of 100 ns, 120 ns, 150 ns, or 200 ns. Typical power dissipation is 200 mW operating and 16.5 mW standby.

New SMOS technology permits operation from a single +5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{DD} peaks are 150 mA typical, and a −1-V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address and data-in lines are latched on chip to simplify system design. Data-out is unlatched to allow greater system flexibility.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

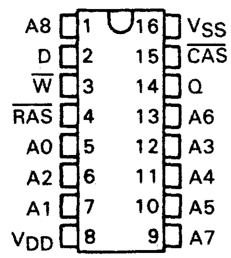
TMS4256, TMS4257
262,144-BIT DYNAMIC RANDOM-ACCESS MEMORIES

MAY 1983

- 262,144 X 1 Organization
- Single +5-V Supply (10% Tolerance)
- JEDEC Standardized Pin Out
- Upward Pin Compatible with TMS4164 (64K Dynamic RAM)
- Performance Ranges:

DEVICE	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TMS4256-10 TMS4257-10	100 ns	50 ns	200 ns
TMS4256-12 TMS4257-12	120 ns	60 ns	230 ns
TMS4256-15 TMS4257-15	150 ns	75 ns	260 ns
TMS4256-20 TMS4257-20	200 ns	100 ns	330 ns

TMS4256, TMS4257 . . . JL OR NL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column Address Strobe
D	Data-In
Q	Data-Out
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Write Enable
V_{DD}	+5-V Supply
V_{SS}	Ground

- Long Refresh Period . . . 4 ms (MAX)
- Low Refresh Overhead Time . . . As Low As 1.3% of Total Refresh Period
- On-Chip Substrate Bias Generator
- All Inputs, Outputs, and Clocks Fully TTL Compatible
- 3-State Unlatched Output
- Common I/O Capability with "Early Write" Feature
- Page ('4256) or Nibble-Mode ('4257) Options for Faster Access Operation
- Low Power Dissipation:
  Operating . . . 200 mW (TYP)
  Standby . . . 16.5 mW (TYP)
- $\overline{RAS}$ Only Refresh Mode
- Hidden Refresh Mode

description

The '4256 and '4257 are high-speed, 262,144-bit dynamic random-access memories, organized as 262,144 words of one bit each. They employ state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon gate technology for very high performance combined with low cost and improved reliability.

These devices feature maximum $\overline{RAS}$ access times of 100 ns, 120 ns, 150 ns, or 200 ns. Typical power dissipation is 200 mW operating and 16.5 mW standby.

New SMOS technology permits operation from a single +5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{DD} peaks are 150 mA typical, and a −1-V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address and data-in lines are latched on chip to simplify system design. Data-out is unlatched to allow greater system flexibility.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

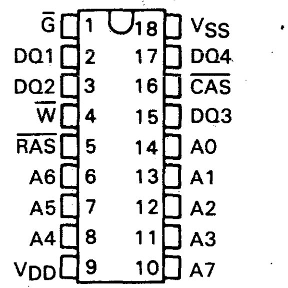
TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

- **65,536 X 4 Organization**
- **Single +5-V Supply (10% Tolerance)**
- **JEDEC Standardized Pin-Out**
- **Pin-Out Identical to TMS4416 (16K X 4 Dynamic RAM)**
- **Performance Ranges:**

DEVICE	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
TMS4464-10	100 ns	60 ns	200 ns	275 ns
TMS4464-12	120 ns	70 ns	230 ns	320 ns
TMS4464-15	150 ns	85 ns	260 ns	365 ns
TMS4464-20	200 ns	120 ns	330 ns	460 ns

- **Long Refresh Period . . . 4 ms (MAX)**
- **Low Refresh Overhead Time . . . As Low As 1.3% of Total Refresh Period**
- **On-Chip Substrate Bias Generator**
- **All Inputs, Outputs, and Clocks Fully TTL Compatible**
- **3-State Unlatched Output**
- **Early Write or $\overline{G}$ to Control Output Buffer Impedance**
- **Page-Mode Operation for Faster Access**
- **Low Power Dissipation:**
  - **Operating . . . 350 mW (TYP)**
  - **Standby . . . 16.5 mW (TYP)**
- **$\overline{RAS}$ Only Refresh Mode**
- **Hidden Refresh Mode**

TMS4464 . . . JL OR NL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column Address Strobe
DQ1-DQ4	Data-In/Data-Out
$\overline{G}$	Output Enable
$\overline{RAS}$	Row Address Strobe
V_{DD}	+5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TMS4464 is a high-speed, 262,144-bit dynamic random-access memory, organized as 65,536 words of four bits each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon gate technology for very high performance combined with low cost and improved reliability.

This device features maximum $\overline{RAS}$ access times of 100 ns, 120 ns, 150 ns, or 200 ns. Typical power dissipation is 350 mW operating and 16.5 mW standby.

New SMOS technology permits operation from a single +5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{DD} peaks are 150 mA typical, and a −1-V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address and data-in lines are latched on chip to simplify system design. Data-out is unlatched to allow greater system flexibility.

The TMS4464 is offered in an 18-pin dual-in-line ceramic or plastic package and is guaranteed for operation from 0°C to 70°C. These packages are designed for insertion in mounting-hole rows on 300-mil (7,62 mm) centers.

Texas Instruments

MEMORY

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

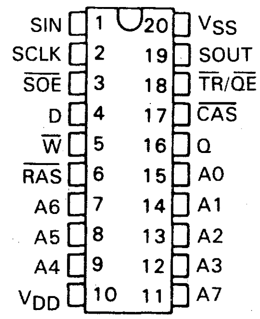
TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TMS4161
65,536-BIT MULTIPORT MEMORY

JULY 1983

- Dual Accessability – One Port Sequential Access, One Port Random Access
- Four Cascaded 64-Bit Serial Shift Registers for Sequential Access Applications
- Shift Register Loaded Once Every 64, 128, 192, or 256 Shift Cycles as Desired by User
- Fast Serial Port . . . 25 MHz Shift Rate
- $\overline{TR}/\overline{QE}$ as Output Enable Allows Direct Connection of D, Q and Address Lines to Simplify System Design
- Random Access Port Looks Exactly Like a TMS4164
- Separate Serial In and Serial Out to Allow Simultaneous Shift In and Out
- 65,536 × 1 Organization
- Maximum Access Time from $\overline{RAS}$ Less Than 150 ns
- Minimum Cycle Time (Read or Write) Less Than 260 ns
- Long Refresh Period . . . 4 Milliseconds
- Low Refresh Overhead Time . . . As Low As 1.6% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Outputs for Both Random and Serial Access
- Common I/O Capability with "Early Write" Feature
- Page-Mode Operation for Faster Access
- Low Power Dissipation
  - Operating . . . 200 mW (Typical)
  - Standby . . . 35 mW (Typical)
- New SMOS (Scaled-MOS) N-Channel Technology
- $\overline{SOE}$ Simplifies Multiplexing of Video Data Streams

TMS4161 . . . NL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column Address Strobe
D	Random Access Data-In
Q	Random Access Data-Out
$\overline{RAS}$	Row Address Strobe
SCLK	Serial Data Clock
SIN	Serial Data-In
$\overline{SOE}$	Serial Output Enable
SOUT	Serial Data-Out
$\overline{TR}/\overline{QE}$	Register Transfer/Q Output Enable
$\overline{W}$	Write Enable
V_{DD}	+5-V Supply
V_{SS}	Ground

description

The TMS4161 is a high-speed, dual-access 65,536-bit dynamic random-access memory. The random-access port makes the memory look like it is organized as 65,536 words of one bit each like the TMS4164. The sequential access port is interfaced to an internal 256-bit dynamic shift register organized as four 64-bit shift registers which makes the memory look like it is organized as up to 256 words of up to 256 bits each which are accessed serially. One,

PRODUCT PREVIEW

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TEXAS INSTRUMENTS
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two, three, or four 64-bit shift registers can be sequentially read out depending on a two-bit code applied to the two most significant column address inputs. The TMS4161 employs state-of-the-art SMOS (Scaled-MOS) N-channel double level polysilicon gate technology for very high performance combined with low cost and improved reliability.

The TMS4161 features full asynchronous dual access capability except when transferring data between the shift register and the memory array.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power. Note that the transfer of a row of data from the memory array to the shift register also refreshes that row.

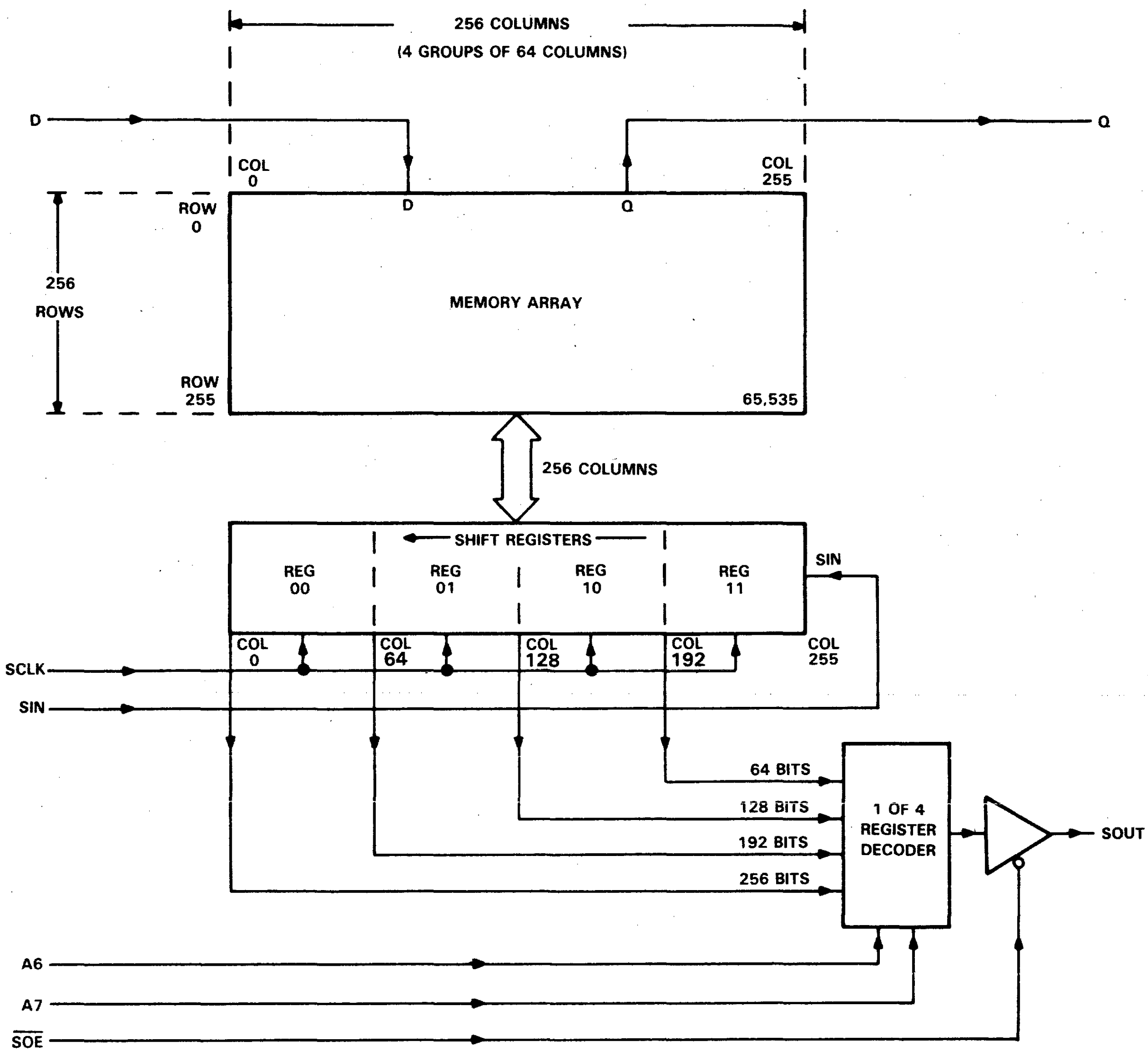
All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data-in are latched on chip to simplify system design. Data-out is unlatched to allow greater system flexibility.

The TMS4161 is offered in a 20-pin dual-in-line-plastic package and is guaranteed for operation from 0°C to 70°C. Packages are designed for insertion in mounting-hole rows on 300-mil (7.62 mm) centers.

random access address space to sequential address space mapping

The TMS4161 is designed with each row divided into four, 64-column sections. The first column section to be shifted out is selected by the two most significant column address bits. If the two bits represent binary 00, then one to four registers can be shifted out in order. If the two bits represent binary 01, then only 1 to 3 (the most significant) registers can be shifted out in order. If the two bits represent 10, then one to two of the most significant registers can be shifted out in order. Finally, if the two bits represent 11 only the most significant register can be shifted out. All registers are shifted out with the least significant bit (bit 0) first and the most significant bit (bit 63) last. Note that if the two column address bits equal 00 during the last register transfer cycle ($\overline{TR}/\overline{QE}$ equal to 0) a total of 256 bits can be sequentially read out.

functional block diagram



random access operation

TR/QE

The TR/QE pin has two functions. First, it selects either register transfer or random-access operation as RAS falls, and second, if this is a random-access operation, it functions as an output enable after CAS falls.

To use the TMS4161 in the random-access mode, TR/QE must be high as RAS falls. Holding TR/QE high disconnects the 256 elements of the shift registers from the corresponding 256 bit lines of the memory array. If data is to be shifted, the shift registers must be disconnected from the bit lines. Holding TR/QE low enables the 256 switches that connect the shift registers to the bit lines and indicates that a transfer will occur between the shift registers and one of the memory rows.

Once CAS has been pulled low, TR/QE controls when the data will appear at the Q output (if this is a read cycle). Whenever TR/QE is held high, the Q output will be in the high-impedance state. This feature removes the possibility of an overlap between data on the address lines and data appearing on the Q output making it possible to connect the address lines to the Q and D lines (Use of this organization prohibits the use of the early write cycle.).

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data-out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data-in (D)

Data is written during a write or read-modify-write cycle. The falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data-out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan-out of two Series 74 TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state as long as $\overline{CAS}$ or $\overline{TR}/\overline{QE}$ is held high. Data will not appear on the output until after both $\overline{CAS}$ and $\overline{TR}/\overline{QE}$ have been brought low. In a read cycle, the guaranteed maximum output enable access time is valid only if t_{CQE} is greater than t_{CQE} MAX, and t_{RLCL} is greater than t_{RLCL} MAX. Likewise, $t_{a(C)}$ MAX is valid only if t_{RLCL} is greater than t_{RLCL} MAX. Once the output is valid, it will remain valid while $\overline{CAS}$ and $\overline{TR}/\overline{QE}$ are both low; $\overline{CAS}$ or $\overline{TR}/\overline{QE}$ going high will return the output to a high-impedance state. In an early write cycle, the output is always in a high-impedance state. In a delayed write or read-modify-write cycle, the output will follow the sequence for the read cycle. In a register transfer cycle, the output will always be in a high-impedance state.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$ only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power. Note that the shift registers are also dynamic storage elements and that the data held in the registers will be lost unless SCLK goes high to shift the data one bit position or else the data is reloaded from the memory array. See specifications for maximum register data retention times.

page-mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on a single RAM, the row address and $\overline{RAS}$ are applied to multiple 64K RAMs. $\overline{CAS}$ is then decoded to select the proper RAM.

sequential access operation

$\overline{\mathrm{TR}}/\overline{\mathrm{QE}}$

Memory operations involving parallel use of the shift register are first indicated by bringing $\overline{\mathrm{TR}}/\overline{\mathrm{QE}}$ low before $\overline{\mathrm{RAS}}$ falls low. This enables the switches connecting the 256 elements of the shift register to the 256 bit lines of the memory array. The $\overline{\mathrm{W}}$ line determines whether the data will be transferred from or to the shift registers.

write enable ($\overline{\mathrm{W}}$)

In the sequential access mode, $\overline{\mathrm{W}}$ determines whether a transfer will occur from the shift registers to the memory array, or from the memory array to the shift registers. To transfer from the shift registers to the memory array, $\overline{\mathrm{W}}$ is held low as $\overline{\mathrm{RAS}}$ falls, and, to transfer from the memory array to the shift registers, $\overline{\mathrm{W}}$ is held high as $\overline{\mathrm{RAS}}$ falls. Thus, reads and writes are always with respect to the memory array. The write setup and hold times are referenced to the falling edge of $\overline{\mathrm{RAS}}$ for this mode of operation.

row address (A0 through A7)

Eight address bits are required to select one of the 256 possible rows involved in the transfer of data to or from the shift registers. The A0-A7, $\overline{\mathrm{W}}$, and the $\overline{\mathrm{TR}}/\overline{\mathrm{QE}}$ line are latched on the falling edge of $\overline{\mathrm{RAS}}$.

register column address (A7, A6)

To select one of the four shift registers (transfer from memory to register only), the appropriate 2-bit column address (A7, A6) must be valid when $\overline{\mathrm{CAS}}$ falls. However, the $\overline{\mathrm{CAS}}$ and register address signals need not be supplied every cycle, only when it is desired to change or select a new register.

SCLK

Data is shifted in and out on the rising edge of SCLK. This makes it possible to view the shift registers as though it were made of 256 rising edge D flip-flops connected D to Q. The TMS4161 is designed to work with a wide range duty cycle clock to simplify system design. Note that data will appear at the SOUT pin not only on the rising edge of SCLK but also after an access time of $t_{a(RSO)}$ from $\overline{\mathrm{RAS}}$ high during a parallel load of the shift registers.

SIN and SOUT

Data is shifted in through the SIN pin and is shifted out through the SOUT pin. The TMS4161 is designed such that it requires 0 ns hold time on SIN as SCLK rises. SOUT is guaranteed not to change for at least 8 ns after SLCK rises. These features make it possible to easily connect TMS4161s together, to allow SOUT to be connected to SIN, and to give external circuitry a full SLCK cycle time to allow manipulation of the serial data. To guarantee proper serial clock sequence after power up, a transfer cycle must be initiated before serial data is applied at SIN.

$\overline{\mathrm{SOE}}$

The serial output enable pin controls the impedance of the serial output allowing multiplexing of more than one bank of TMS4161 memories into the same external video circuitry. When $\overline{\mathrm{SOE}}$ is at a low logic level, SOUT will be enabled and the proper data read out. When $\overline{\mathrm{SOE}}$ is at a high logic level, SOUT will be disabled and be in the high-impedance state.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage on any pin except V_{DD} and data out (see Note 1)	−1.5 V to 10 V
Voltage on V_{DD} supply and data out with respect to V_{SS}	−1 V to 6 V
Short circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range	0 °C to 70 °C
Storage temperature range	−65 °C to 150 °C

† Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TMS4164, SMJ4164
65,536-BIT DYNAMIC RANDOM-ACCESS MEMORY

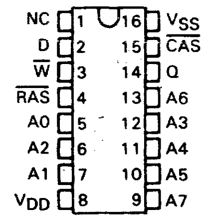
JULY 1980 – REVISED OCTOBER 1983

- 65,536 X 1 Organization
- Single +5-V Supply (10% Tolerance)
- JEDEC Standardized Pin-Out in Dual-In-Line Packages
- Upward Pin Compatible with TMS4116 (16K Dynamic RAM)
- First Military Version of 64K DRAM
- Available Temperature Ranges:
  - M . . . −55°C to 125°C
  - S . . . −55°C to 100°C
  - E . . . −40°C to 85°C
  - L . . . 0°C to 70°C
- Long Refresh Period . . . 4 milliseconds
- Low Refresh Overhead Time . . . As Low As 1.8% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Output
- Common I/O Capability with "Early Write" Feature
- Page-Mode Operation for Faster Access
- Low Power Dissipation
  - Operating . . . 125 mW (TYP)
  - Standby . . . 17.5 mW (TYP)
- Performance Ranges:

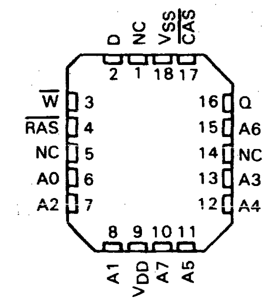
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
'4164-12	120 ns	70 ns	230 ns	260 ns
'4164-15	150 ns	85 ns	260 ns	285 ns
'4164-20	200 ns	135 ns	330 ns	345 ns

- New SMOS (Scaled-MOS) N-Channel Technology

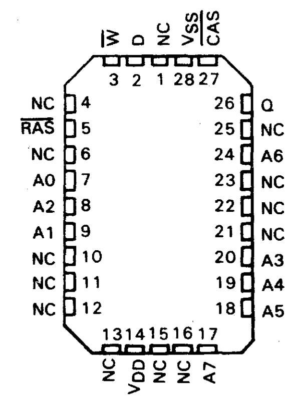
TMS4164 . . . JDL OR NL PACKAGE
SMJ4164 . . . JD PACKAGE
(TOP VIEW)



TMS4164 . . . FPL PACKAGE
SMJ4164 . . . FG PACKAGE
(TOP VIEW)



SMJ4164 . . . FE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column Address Strobe
D	Data-In
NC	No-Connection
Q	Data-Out
$\overline{RAS}$	Row Address Strobe
V_{DD}	+5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The '4164 is a high-speed, 65,536-bit, dynamic random-access memory, organized as 65,536 words of one bit each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon gate technology for very high performance combined with low cost and improved reliability.

ADVANCE INFORMATION
MILITARY PRODUCTS (SMJ) ONLY
This document contains information on a new product. Specifications are subject to change without notice.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TMS4416, SMJ4416
16,384-WORD BY 4-BIT DYNAMIC RAM

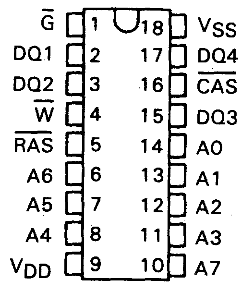
AUGUST 1980 – REVISED SEPTEMBER 1983

- 16,384 X 4 Organization
- Single +5-V Supply (10% Tolerance)
- Performance Ranges:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
'4416-15	150 ns	80 ns	260 ns	360 ns
'4416-20	200 ns	120 ns	330 ns	440 ns

- Available Temperature Ranges*:
  - S . . . −55°C to 100°C
  - E . . . −40°C to 85°C
  - L . . . 0°C to 70°C
- Long Refresh Period . . . 4 milliseconds
- Low Refresh Overhead Time . . . As Low As 1.7% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Outputs
- Early Write or $\overline{\text{G}}$ to Control Output Buffer Impedance
- Page-Mode Operation for Faster Access
- Low Power Dissipation
  - Operating . . . 130 mW (TYP)
  - Standby . . . 17.5 mW (TYP)
- New SMOS (Scaled-MOS) N-Channel Technology

TMS4416 . . . NL PACKAGE
SMJ4416 . . . JD PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{\text{CAS}}$	Column Address Strobe
DQ1-DQ4	Data In/Data Out
$\overline{\text{G}}$	Output Enable
$\overline{\text{RAS}}$	Row Address Strobe
V_{DD}	+5-V Supply
V_{SS}	Ground
$\overline{\text{W}}$	Write Enable

description

The '4416 is a high-speed, 65,536-bit, dynamic, random-access memory, organized as 16,384 words of 4 bits each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon gate technology for very high performance combined with low cost and improved reliability.

The '4416 features $\overline{\text{RAS}}$ access times to 150 ns maximum. Power dissipation is 130 mW typical operating, 17.5 mW typical standby.

New SMOS technology permits operation from a single +5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{DD} peaks have been reduced to 60 mA typical, and a −1-V input voltage undershoot can be tolerated, minimizing system noise considerations. Input clamp diodes are used to ease system design.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{\text{RAS}}$ in order to retain data. $\overline{\text{CAS}}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 54/74 TTL. All address lines and data-in are latched on chip to simplify system design. Data-out is unlatched to allow greater system flexibility.

* M temperature range (−55°C to 125°C) to be available in future.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TMS4500A DYNAMIC RAM CONTROLLER

JANUARY 1982 – REVISED APRIL 1983

- Controls Operation of 8K/16K/32K/64K Dynamic RAMs
- Creates Static RAM Appearance
- One Package Contains Address Multiplexer, Refresh Control, and Timing Control
- Directly Addresses and Drives Up to 256K Bytes of Memory Without External Drivers
- Operates from Microprocessor Clock
  - No Crystals, Delay Lines, or RC Networks
  - Eliminates Arbitration Delays
- Refresh May Be Internally or Externally Initiated
- Versatile
  - Strap-Selected Refresh Rate
  - Synchronous, Predictable Refresh
  - Selection of Distributed, Transparent, and Cycle-Steal Refresh Modes
  - Interfaces Easily to Popular Microprocessors
- Strap-Selected Wait State Generation for Microprocessor/Memory Speed Matching
- Ability to Synchronize or Interleave Controller with the Microprocessor System (Including Multiple Controllers)
- Three-State Outputs Allow Multiport Memory Configuration
- Performance Ranges of 150 ns/200 ns/250 ns

TMS4500A . . . NL PACKAGE
(TOP VIEW)

Signal	Pin	Pin	Signal
CLK	1	40	VCC
RDY	2	39	$\overline{\text{REFREQ}}$
REN1	3	38	TWST
$\overline{\text{CS}}$	4	37	FS0
ALE	5	36	FS1
$\overline{\text{RAS0}}$	6	35	RA7
$\overline{\text{RAS1}}$	7	34	CA7
$\overline{\text{ACR}}$	8	33	MA7
$\overline{\text{ACW}}$	9	32	MA6
$\overline{\text{CAS}}$	10	31	CA6
RA0	11	30	RA6
CA0	12	29	RA5
MA0	13	28	CA5
MA1	14	27	MA5
CA1	15	26	RA4
RA1	16	25	CA4
RA2	17	24	MA4
CA2	18	23	RA3
MA2	19	22	CA3
GND	20	21	MA3

description

The TMS4500A is a monolithic DRAM system controller designed to provide address multiplexing, timing, control and refresh/access arbitration functions to simplify the interface of dynamic RAMs to microprocessor systems.

The controller contains a 16-bit multiplexer that generates the address lines for the memory device from the 16 system address bits and provides the strobe signals required by the memory to decode the address. An 8-bit refresh counter generates the 256-row addresses required for refresh.

A refresh timer is provided that generates the necessary timing to refresh the dynamic memories and assure data retention.

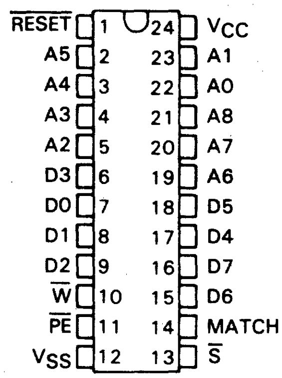
The TMS4500A also contains refresh/access arbitration circuitry to resolve conflicts between memory access requests and memory refresh cycles. The TMS4500A is offered in a 40-pin, 600-mil dual-in-line plastic package and is guaranteed for operation from 0°C to 70°C.

TMS2150
CACHE ADDRESS COMPARATOR

MARCH 1982 – REVISED SEPTEMBER 1983

- Fast Address to Match Valid Delay – Two Speed Ranges: 45 ns, 55 ns
- 512 X 9 Internal RAM
- 300-Mil 24-Pin Ceramic Side Brazed Package
- Max Power Dissipation: 660 mW
- On-Chip Parity Generation and Checking
- Parity Error Output/Force Parity Error Input
- On-Chip Address/Data Comparator
- Asynchronous, Single-Cycle Reset
- Easily Expandable
- Fully Static, TTL Compatible
- Reliable SMOS (Scaled NMOS) Technology

TMS2150 . . . JDL PACKAGE
(TOP VIEW)



description

The 8-bit-slice cache address comparator consists of a high-speed 512 X 9 static RAM array, parity generator, and parity checker, and 9-bit high-speed comparator. It is fabricated using N-channel silicon gate technology for high speed and simple interface with MOS and bipolar TTL circuits. The cache address comparator is easily cascadable for wider tag addresses or deeper tag memories. Significant reductions in cache memory component count, board area, and power dissipation can be achieved with this device.

When $\overline{\text{S}}$ is low and $\overline{\text{W}}$ is high, the cache address comparator compares the contents of the memory location addressed by A0-A8 with the data on D0-D7 plus generated parity. An equality is indicated by a high level on the MATCH output. A low-level output from $\overline{\text{PE}}$ signifies a parity error in the internal RAM data. $\overline{\text{PE}}$ is an N-channel open-drain output for easy OR-tieing. During a write cycle ($\overline{\text{S}}$ and $\overline{\text{W}}$ low), data on D0-D7 plus generated even parity are written in the 9-bit memory location addressed by A0-A8. Also during write, a parity error may be forced by holding $\overline{\text{PE}}$ low.

A $\overline{\text{RESET}}$ input is provided for initialization. When $\overline{\text{RESET}}$ goes low, all 512 X 9 RAM locations will be cleared and the MATCH output will be forced high.

The cache address comparator operates from a single +5 V supply and is offered in a 24-pin 300-mil side brazed package. The device is fully TTL compatible and is guaranteed to operate from 0°C to 70°C.

MATCH OUTPUT DESCRIPTION

MATCH = V_{OH} if: [A0-A8] = D0-D7 + parity,
or: $\overline{\text{RESET}} = V_{IL}$,
or: $\overline{\text{S}} = V_{IH}$,
or: $\overline{\text{W}} = V_{IL}$

MATCH = V_{OL} if: [A0-A8] $\neq$ D0-D7 + parity,
with $\overline{\text{RESET}} = V_{IH}$,
$\overline{\text{S}} = V_{IL}$, and $\overline{\text{W}} = V_{IH}$

FUNCTION TABLE

OUTPUT		FUNCTION
MATCH	$\overline{\text{PE}}$	DESCRIPTION
L	L	Parity Error
L	H	Not Equal
H	L	Undefined Error
H	H	Equal

Where $\overline{\text{S}} = V_{IL}$, $\overline{\text{W}} = V_{IH}$, $\overline{\text{RESET}} = V_{IH}$

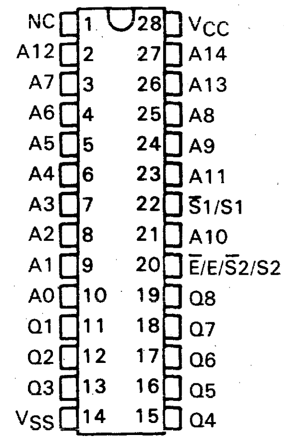
TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

- **32,768 X 8 Organization**
- **Fully Static (No clocks, No Refresh)**
- **All Inputs and Outputs TTL Compatible**
- **Single 5-V Power Supply**
- **Optional Power Down or Chip Select**
- **64K Bank Select Option**
- **Maximum Access Time from Address or Power Down:**

TMS47256-25	250 ns
TMS47256-35	350 ns
TMS47256-45	450 ns

- **Worst Case Active Power Dissipation . . . 330 mW**
- **Worst Case Standby Power Dissipation . . . 66 mW**

TMS47256 . . . JL OR NL PACKAGE†
STANDARD ROM
(TOP VIEW)



† The package for the bank select ROM is shown on page 2.

PIN NOMENCLATURE STANDARD ROM	
A0-A14	Addresses
$\overline{E}$/E/$\overline{S}$2/S2	Chip Enable/Power Down or Chip Select
NC	No Connection
Q1-Q8	Data Out
$\overline{S}$1/S1	Chip Select
V_{CC}	+5-V Supply
V_{SS}	Ground

description

The TMS47256 is a 262,144-bit read-only memory organized as 32,768 words of 8-bit length. This makes the TMS47256 ideal for microprocessor based systems. The device is fabricated using N-channel silicon-gate technology for high speed and simple interface with bipolar circuits.

There are two versions of the TMS47256: the standard ROM with options on chip selects and power down, and the bank select ROM with similar options. The operation section of this data sheet describes both versions.

The TMS47256 is fully compatible with Series 74, 74S, or 74LS TTL. The data outputs are three-state for OR-tieing multiple devices on a common bus. Pins 20 and 22 are mask-programmable, providing additional system flexibility. The data is always available, it is not dependent on external clocking of pins 20 and 22.

The TMS47256 is designed for high-density fixed-memory applications such as logic function generation and microprogramming. It is pin compatible with TI's full line of ROMs and EPROMs.

This ROM is supplied in 28-pin dual-in-line plastic (NL suffix) or ceramic (JL suffix) packages designed for insertion in mounting-hole rows on 600 mil centers. The device is designed for operation from 0°C to 70°C.

operation, standard ROM

address (A0-A14)

The address-valid interval determines the device cycle time. The 15-bit positive-logic address is decoded on-chip to select one of 32,768 words of 8-bit length in the memory array. A0 is the least-significant bit and A14 the most-significant bit of the word address.

chip select ($\overline{S}$1 or S1)

Pin 22 can be programmed during mask fabrication to be active with either a high- or low-level input. When the signal

PRODUCT PREVIEW

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TEXAS INSTRUMENTS
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TMS47128
16,384-WORD BY 8-BIT READ-ONLY MEMORY

JUNE 1983

- 16,384 X 8 Organization
- Fully Static (No Clocks, No Refresh)
- All Inputs and Outputs TTL Compatible
- Single 5-V Power Supply
- Optional Power Down or Chip Select
- 64K Bank Select Option
- Maximum Access Time from Address or Power Down:

TMS47128-25	250 ns
TMS47128-35	350 ns
TMS47128-45	450 ns

- Worst Case Active Power Dissipation . . . 330 mW
- Worst Case Standby Power Dissipation . . . 66 mW

TMS47128 . . . JL OR NL PACKAGE†
STANDARD ROM
(TOP VIEW)

Signal	Pin	Pin	Signal
NC	1	28	V_{CC}
A12	2	27	$\overline{S}$2/S2
A7	3	26	A13
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	$\overline{S}$1/S1
A2	8	21	A10
A1	9	20	$\overline{E}$/E/$\overline{S}$3/S3
A0	10	19	Q8
Q1	11	18	Q7
Q2	12	17	Q6
Q3	13	16	Q5
V_{SS}	14	15	Q4

† The package for the bank select ROM is shown on page 2.

description

The TMS47128 is a 131,072-bit read-only memory organized as 16,384 words of 8-bit length. This makes the TMS47128 ideal for microprocessor based systems. The device is fabricated using N-channel silicon-gate technology for high speed and simple interface with bipolar circuits.

There are two versions of the TMS47128: the standard ROM with options on chip selects and power down, and the bank select ROM with similar options. The operation section of this data sheet describes both versions

PIN NOMENCLATURE STANDARD ROM	
A0-A13	Addresses
$\overline{E}$/E/$\overline{S}$3/S3	Chip Enable/Power Down or Chip Select
NC	No Connection
Q1-Q8	Data Out
$\overline{S}$1/S1, $\overline{S}$2/S2	Chip Selects
V_{CC}	+5-V Supply
V_{SS}	Ground

The TMS47128 is fully compatible with Series 74, 74S, or 74LS TTL. The data outputs are three-state for OR-tieing multiple devices on a common bus. Pins 20, 22, and 27 are mask-programmable, providing additional system flexibility. The data is always available, it is not dependent on external clocking of pins 20, 22, or 27.

The TMS47128 is designed for high-density fixed-memory applications such as logic function generation and microprogramming. It is pin compatible with TI's full line of ROMs and EPROMs.

This ROM is supplied in 28-pin dual-in-line plastic (NL suffix) or ceramic (JL suffix) packages designed for insertion in mounting-hole rows on 600 mil centers. The device is designed for operation from 0°C to 70°C.

operation, standard ROM

address (A0-A13)

The address-valid interval determines the device cycle time. The 14-bit positive-logic address is decoded on-chip to select one of 16,384 words of 8-bit length in the memory array. A0 is the least-significant bit and A13 the most-significant bit of the word address.

chip select ($\overline{S}$1 or S1 and $\overline{S}$2 or S2)

Pins 22 and 27 can be programmed during mask fabrication to be active with either a high- or a low-level input. When

Texas Instruments

MEMORY

PRODUCT PREVIEW

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TEXAS INSTRUMENTS
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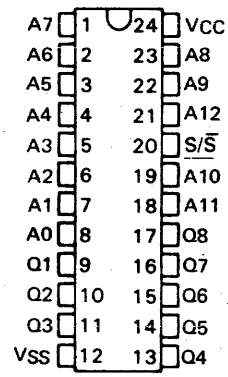
TMS4764
8192-WORD BY 8-BIT READ-ONLY MEMORY

JUNE 1981 – REVISED JULY 1983

- 8192 X 8 Organization
- Fully Static (No Clocks, No Refresh)
- All Inputs and Outputs TTL Compatible
- Single 5-V Power Supply
- Maximum Access Time From Address:
  TMS4764-30 300 ns
  TMS4764-35 350 ns
  TMS4764-45 450 ns
- Typical Active Power Dissipation
  . . . 275 mW

TMS4764 . . . JL OR NL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0 – A12	Addresses
Q1 – Q8	Data Out
S/S̄	Chip Select
V_{CC}	+5-V Supply
V_{SS}	Ground

description

The TMS4764 is a 65,536-bit read-only memory organized as 8192 words of 8-bit length. This makes the TMS4764 ideal for microprocessor based systems. The device is fabricated using N-channel silicon-gate technology for high speed and simple interface with bipolar circuits.

All inputs can be driven directly by Series 74 TTL circuits without the use of any internal pull-up resistor. Each output can drive two Series 74 or 74S loads without external resistors. The data outputs are three-state for OR-tieing multiple devices on a common bus. Pin 20 is programmable, providing additional system flexibility. The data is always available, it is not dependent on external clocking of pin 20.

The TMS4764 is designed for high-density fixed-memory applications such as logic function generation and microprogramming. It is pin compatible with TI's full line of ROMs and EPROMs.

This ROM is supplied in 24-pin dual-in-line-plastic (NL suffix) or ceramic (JL suffix) packages designed for insertion in mounting-hole rows on 600-mil centers or chip on board. The device is designed for operation from 0°C to 70°C.

operation

address (A0 – A12)

The address-valid interval determines the device cycle time. The 13-bit positive-logic address is decoded on-chip to select one of 8192 words of 8-bit length in the memory array. A0 is the least-significant bit and A12 the most-significant bit of the word address.

chip select (S or S̄)

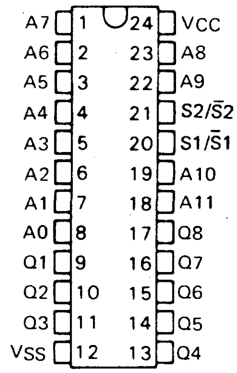
Pin 20 can be programmed during mask fabrication to be active with either a high- or a low-level input. When the signal is active, all eight outputs are enabled and the eight-bit addressed word can be read. When the signal is not active, all eight outputs are in a high-impedance state.

TMS4732
4096-WORD BY 8-BIT READ-ONLY MEMORY

MAY 1977 – REVISED JULY 1983

- **4096 X 8 Organization**
- **All Inputs and Outputs TTL Compatible**
- **Fully Static (No Clocks, No Refresh)**
- **Single 5-V Power Supply**
- **Maximum Access Time From Address:**
  TMS4732-30 300 ns
  TMS4732-35 350 ns
  TMS4732-45 450 ns
- **Typical Power Dissipation . . . 275 mW**
- **3-State Outputs for OR-Ties**
- **Pin-Compatible with TMS2532 EPROM**
- **Two Output Enable Controls for Chip Select Flexibility**

TMS4732 . . . JL OR NL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0 – A11	Addresses
Q1 – Q8	Data Out
S1/$\overline{S}$1, S2/$\overline{S}$2	Chip Selects
V_{CC}	+5-V Supply
V_{SS}	Ground

description

The TMS4732 is a 32,768-bit read-only memory organized as 4096 words of 8-bit length. This makes the TMS4732 ideal for microprocessor based systems. The device is fabricated using N-channel silicon-gate technology for high speed and simple interface with bipolar circuits.

All inputs can be driven directly by Series 74 TTL circuits without the use of any internal pull-up resistor. Each output can drive one Series 74 or 74S load without external resistors. The data outputs are three-state for OR-tieing multiple devices on a common bus. Two chip-select controls allow data to be read. These controls are programmable, providing additional system decode flexibility. The data is always available, it is not dependent on external clocking of the control pins.

The TMS4732 is designed for high-density fixed-memory applications such as logic function generation and microprogramming. The part is pin compatible with the TMS2532 4096 × 8 EPROM, which aids in prototyping and code verification.

This ROM is supplied in 24-pin dual-in-line-plastic (NL suffix) or ceramic (JL suffix) packages designed for insertion in mounting-hole rows on 600-mil centers or chip on board. The device is designed for operation from 0°C to 70°C.

operation

address (A0 – A11)

The address-valid interval determines the device cycle time. The 12-bit positive-logic address is decoded on-chip to select one of 4096 words of 8-bit length in the memory array. A0 is the least-significant bit and A11 the most-significant bit of the word address.

chip select/output enable (pins 20 and 21)

Each of these pins can be programmed during mask fabrication to be active with either a high- or a low-level input. When both signals are active, all eight outputs are enabled and the eight-bit addressed word can be read. When either signal is not active, all eight outputs are in a high-impedance state.

TMS27128
131,072-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

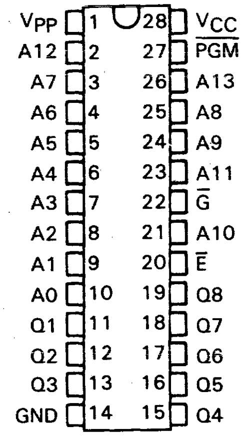
OCTOBER 1983

- 16,384 X 8 Organization
- Single +5-V Power Supply
- Pin Compatible with TMS2764 EPROM
- All Inputs Are TTL Compatible
- Max Access/Min Cycle Time:

TMS27128-20	200 ns
TMS27128-25	250 ns
TMS27128-30	300 ns
TMS27128-45	450 ns

- Low Power Dissipation
  – 500 mW (Typical)
- JEDEC Approved Pinout

TMS27128 . . . JL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A13	Addresses
$\overline{E}$	Chip Enable/Power Down
$\overline{G}$	Output Enable
GND	Ground
$\overline{PGM}$	Program
Q1-Q8	Outputs
V_{CC}	+5-V Power Supply
V_{PP}	+21-V Power Supply

description

The TMS27128 is an ultraviolet light-erasable, electrically programmable read-only memory. It has 131,072 bits organized as 16,384 words of 8-bit length. The TMS27128 only requires a single 5-volt power supply with a tolerance of ±5%. The TMS27128-20 provides an access time of 200 ns, which is compatible with high-speed microprocessors.

The TMS27128 provides dual output control lines: Output Enable ($\overline{G}$) and Chip Enable/Power Down ($\overline{E}$). This feature allows the $\overline{G}$ control line to eliminate bus contention in multibus microprocessor systems. The TMS27128 has a standby mode that reduces the maximum power dissipation from 750 mW to 225 mW when the device is placed on standby.

This EPROM is supplied in a 28-pin dual-in-line ceramic package (JL suffix). It is pin compatible with the TMS2764 EPROM and is designed for operation from 0°C to 70°C.

operation

The five modes of operation for the TMS27128 are listed in the following table.

FUNCTION (PINS)	MODE				
	Read	Power Down (Standby)	Program	Program Verification	Inhibit Programming
$\overline{PGM}$ (27)	V_{IH}	X	V_{IL}	V_{IH}	X
V_{PP} (1)	5 V	5 V	21 V	21 V	21 V
V_{CC} (28)	V_{CC}	V_{CC}	5 V	5 V	5 V
$\overline{E}$ (20)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}
$\overline{G}$ 22	V_{IL}	X	V_{IH}	V_{IL}	X
Q1-Q8 (11 to 13, 15 to 19)	Q	HI-Z	D	Q	HI-Z

X = V_{IL} or V_{IH}

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TMS2764H
65,536-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

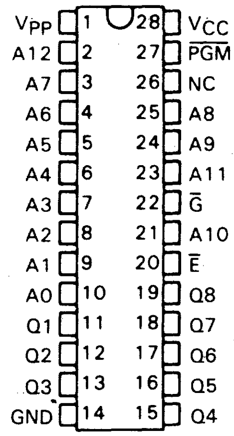
JULY 1983

- **Organization . . . 8192 X 8**
- **Single +5-V Power Supply**
- **Pin Compatible with TMS2732A EPROM**
- **All Inputs and Outputs are TTL Compatible**
- **Performance Ranges:**

	MAX ACCESS/ MIN CYCLE TIME	VOLTAGE TOLERANCE
TMS2764H-20	200 ns	±5%
TMS2764H-25	250 ns	±5%
TMS2764H-30	300 ns	±10%
TMS2764H-45	450 ns	±10%

- **Low Active Current . . . 100 mA (Max)**
- **JEDEC Approved Pinout**
- **21-V Power Supply Required for Programming**
- **Fast Programming Algorithm Compatible**
- **N-Channel Silicon-Gate Technology**
- **8-Bit Output for Use in Microprocessor-Based Systems**
- **Static Operation (No Clocks, No Refresh)**

TMS2764H . . . JL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A12	Addresses
$\overline{E}$	Chip Enable
NC	No Connection
$\overline{G}$	Output Enable
Q1-Q8	Outputs
$\overline{PGM}$	Program

description

The TMS2764H is an ultraviolet light-eraseable, electrically programmable read-only memory. It has 65,536 bits organized as 8,192 words of 8-bit length. The TMS2764H-20 only requires a single 5-volt power supply with a tolerance of ±5%, and has a maximum access time of 200 ns. This access time is compatible with high-performance microprocessors.

The TMS2764H provides two output control lines: Output Enable ($\overline{G}$) and Chip Enable ($\overline{E}$). This feature allows the $\overline{G}$ control line to eliminate bus contention in multibus microprocessor systems. The TMS2764H has a power-down mode that reduces maximum active current from 100 mA to 35 mA when the device is placed on standby.

This EPROM is supplied in a 28-pin, 600-mil dual-in-line ceramic package and is designed for operation from 0 °C to 70 °C.

PRODUCT PREVIEW

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TEXAS INSTRUMENTS
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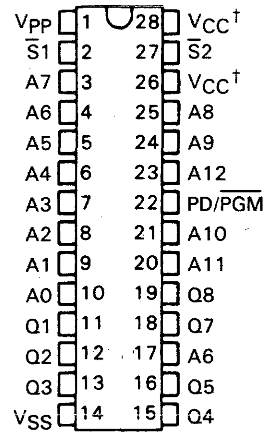
TMS2564, SMJ2564
65,536-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORIES

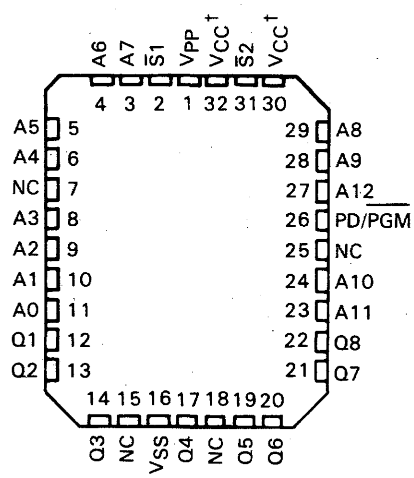
MAY 1981 – REVISED SEPTEMBER 1983

- Organization . . . 8K X 8
- Single +5-V Power Supply
- Pin Compatible with Existing ROMs and EPROMs (8K, 16K, 32K, and 64K)
- All Input/Outputs Fully TTL Compatible
- Static Operation (No Clocks, No Refresh)
- Max Access/Min Cycle Time:
  - TMS2564-35 . . . 350 ns
  - TMS2564-45 . . . 450 ns
  - SMJ2564-45 . . . 450 ns
- 8-Bit Output for Use in Microprocessor-Based Systems
- N-Channel Silicon-Gate Technology
- 3-State Output Buffers
- Guaranteed DC Noise Immunity with Standard TTL Loads
- No Pull-Up Resistors Required
- Low Power Dissipation:
  - Active . . . 400 mW Typical
  - Standby . . . 75 mW Typical
- Available in Full Military Temperature Range Version (SMJ2564)

TMS2564 . . . JL OR JDL PACKAGE
SMJ2564 . . . J PACKAGE
(TOP VIEW)



SMJ2564 . . . FE PACKAGE
(TOP VIEW)



†Connected internally, V_{CC} need be supplied to only one of these two pins.

PIN NOMENCLATURE	
A(N)	Address Inputs
NC	No Connection
PD/$\overline{PGM}$	Power Down/Program
Q(N)	Input/Output
$\overline{S}$(N)	Chip Selects
V_{CC}	+5-V Power Supply
V_{PP}	+25-V Power Supply
V_{SS}	0-V Ground

description

The '2564 is a 65,536-bit ultraviolet-light-erasable, electrically-programmable read-only memory. This device is fabricated using N-channel silicon-gate technology for high-speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54/74 TTL circuits without the use of external resistors. The data outputs are three-state for connecting multiple devices to a common bus.

The TMS2564 is offered in a dual-in-line ceramic package (JL or JDL suffix) rated for operation from 0°C to 70°C. The SMJ2564 is offered in a 28-pin dual-in-line ceramic package (J) and a leadless ceramic chip carrier (FE), rated for operation from −55°C to 125°C. The J package is designed for insertion in mounting-hole rows on 600-mil (15,2 mm) centers, whereas the FE package is intended for surface mounting on solder pads on 0.050-inch (1,27 mm) centers. The FE package offers a three-layer rectangular chip carrier with dimensions 0.450×0.550×0.100 (11,43×13,97×2,54 mm).

ADVANCE INFORMATION
MILITARY PRODUCTS (SMJ) ONLY
This document contains information on a new product. Specifications are subject to change without notice.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

32,768-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

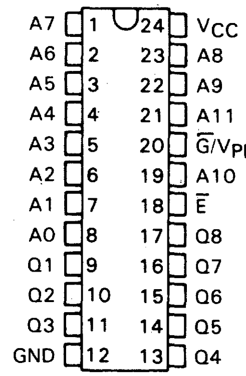
AUGUST 1983

- **Organization . . . 4096 X 8**
- **Single +5-V Power Supply**
- **All Inputs and Outputs Are TTL Compatible**
- **Performance Ranges:**

	ACCESS TIME (MAX)	CYCLE TIME (MIN)
TMS2732A-30	300 ns	300 ns
TMS2732A-35	350 ns	350 ns
TMS2732A-45	450 ns	450 ns

- **Low Standby Power Dissipation . . . 158 mW (Maximum)**
- **JEDEC Approved Pinout . . . Industry Standard**
- **21-V Power Supply Required for Programming**
- **N-Channel Silicon-Gate Technology**
- **8-Bit Output for Use in Microprocessor Based Systems**
- **Static Operation (No Clocks, No Refresh)**

TMS2732A . . . JL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0 – A11	Addresses
$\overline{E}$	Chip Enable
$\overline{G}/V_{PP}$	Output Enable/+21 V
Q1 – Q8	Outputs
V_{CC}	+5-V Power Supply

description

The TMS2732A is an ultraviolet light-erasable, electrically programmable read-only memory. It has 32,768 bits organized as 4,096 words of 8-bit length. The TMS2732A only requires a single 5-volt power supply with a tolerance of ±5%.

The TMS2732A provides two output control lines: Output Enable ($\overline{G}$) and Chip Enable ($\overline{E}$). This feature allows the $\overline{G}$ control line to eliminate bus contention in multibus microprocessor systems. The TMS2732A has a power-down mode that reduces maximum power dissipation from 657 mW to 158 mW when the device is placed on standby.

This EPROM is supplied in a 24-pin dual-in-line ceramic package and is designed for operation from 0°C to 70°C.

operation

The six modes of operation for the TMS2732A are listed in the following table.

FUNCTION (PINS)	MODE					
	Read	Deselect	Power Down (Standby)	Program	Program Verification	Inhibit Programming
$\overline{E}$ (18)	V_{IL}	Don't Care	V_{IH}	V_{IL}	V_{IL}	V_{IH}
$\overline{G}/V_{PP}$ (20)	V_{IL}	V_{IH}	Don't Care	21 V	V_{IL}	21 V
V_{CC} (24)	5 V	5 V	5 V	5 V	5 V	5 V
Q1-Q8 (9 to 11, 13 to 17)	Q	HI-Z	HI-Z	D	Q	HI-Z

PRODUCT PREVIEW

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TMS2532, SMJ2532
32,768-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORIES

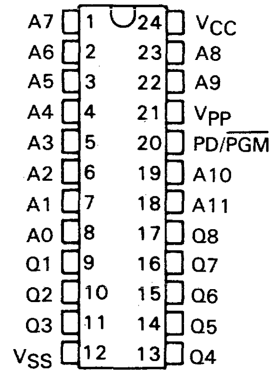
DECEMBER 1979 – REVISED SEPTEMBER 1983

- Organization . . . 4096 X 8
- Single +5-V Power Supply
- Pin Compatible with Existing ROMs and EPROMs (8K, 16K, 32K, and 64K)
- JEDEC Standard Pinout
- All Inputs/Outputs Fully TTL Compatible
- Static Operation (No Clocks, No Refresh)
- Max Access/Min Cycle Time:

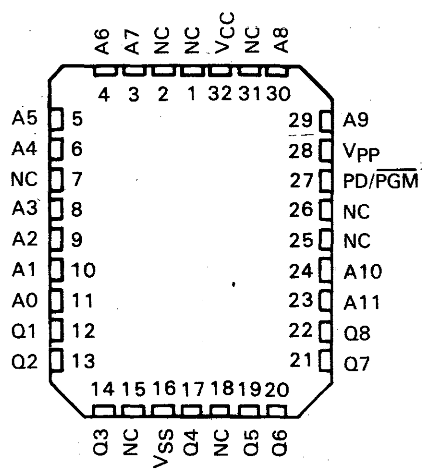
'2532-30	300 ns
'2532-35	350 ns
'2532-45	450 ns

- 8-Bit Output for Use in Microprocessor-Based Systems
- N-Channel Silicon-Gate Technology
- 3-State Output Buffers
- Low Power Dissipation:
  - Active . . . 400 mW Typical
  - Standby . . . 50 mW Standby
- Guaranteed DC Noise Immunity with Standard TTL Loads
- No Pull-Up Resistors Required
- Available in Full Military Temperature Range Version (SMJ2532)

TMS2532 . . . JL PACKAGE
SMJ2532 . . . J PACKAGE
(TOP VIEW)



SMJ2532 . . . FE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A(N)	Address Inputs
NC	No Internal Connection
PD/$\overline{PGM}$	Power Down/Program
Q(N)	Data Outputs
V_{CC}	+5-V Power Supply
V_{PP}	+25-V Supply
V_{SS}	0-V Ground

description

The '2532 series are 32,768-bit, ultraviolet-light-erasable, electrically-programmable read-only memories. These devices are fabricated using N-channel silicon-gate technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54/74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 54/74 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The TMS2532 series are plug-in compatible with the TMS4732 32K ROM.

The TMS2532's are offered in a dual-in-line ceramic package (JL suffix), rated for operation from 0 °C to 70 °C. The SMJ' devices are offered in a 24-pin dual-in-line ceramic package (J) and in a 32-pad leadless ceramic chip carrier (FE). The J package is designed for insertion in mounting-hole rows on 600-mil (15,2 mm) centers, whereas the FE package is intended for surface mounting on solder pads on 0.050-inch (1,27 mm) centers. The FE package offers a three-layer rectangular chip carrier with dimensions 0.450 × 0.550 × 0.100 (11,43 × 13,97 × 2,54 mm).

TMS2516, SMJ2516
16,384-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORIES

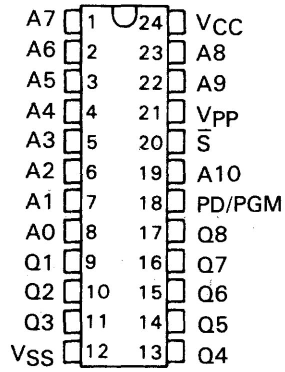
DECEMBER 1979 – REVISED AUGUST 1983

- **Organization . . . 2048 X 8**
- **Single +5-V Power Supply**
- **Pin Compatible with Existing ROMs and EPROMs (16K, 32K, and 64K)**
- **JEDEC Standard Pinout**
- **All Inputs/Outputs Fully TTL Compatible**
- **Static Operation (No Clocks, No Refresh)**
- **Max Access/Min Cycle Time:**

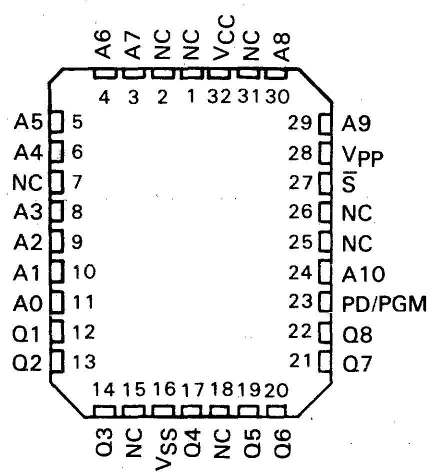
  '2516-35 350 ns
  '2516-45 450 ns
- **8-Bit Output for Use in Microprocessor-Based Systems**
- **N-Channel Silicon-Gate Technology**
- **3-State Output Buffers**
- **40% Lower Power**

  Active 285 mW Typical
  Standby 50 mW Typical
- **Guaranteed DC Noise Immunity with Standard TTL Loads**
- **No Pull-Up Resistors Required**
- **Available in Full Military Temperature Range Version (SMJ2516)**

TMS2516 . . . JL PACKAGE
SMJ2516 . . . J PACKAGE
(TOP VIEW)



SMJ2516 . . . FE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A(N)	Address Inputs
NC	No Internal Connection
PD/PGM	Power Down/Program
Q(N)	Data Outputs
$\overline{S}$	Chip Select
V_{CC}	+5-V Power Supply
V_{PP}	+25-V Power Supply
V_{SS}	0-V Ground

description

The '2516 series are 16,384-bit, ultraviolet-light erasable, electrically-programmable read-only memories. These devices are fabricated using N-channel silicon-gate technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54/74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 54/74 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The '2516 is plug-in compatible with the '4016 16K static RAM.

TEXAS INSTRUMENTS
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TMS2716
2048-WORD BY 8-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORIES

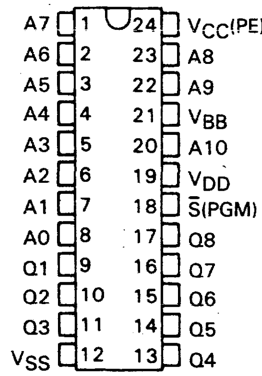
DECEMBER 1979 – REVISED OCTOBER 1983

- 2048 X 8 Organization
- All Inputs and Outputs Fully TTL Compatible
- Static Operation (No Clocks, No Refresh)
- Performance Ranges:

	ACCESS TIME (MAX)	CYCLE TIME (MIN)
TMS2716-30	300 ns	300 ns
TMS2716-45	450 ns	450 ns

- 3-State Outputs for OR-Ties
- N-Channel Silicon-Gate Technology
- 8-Bit Output for Use in Microprocessor-Based Systems
- Low Power . . . 315 mW (Typical)

TMS2716 . . . JL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A10	Addresses
Q1-Q8	Data Out
S̄(PGM)	Chip Select (Program)
V_{BB}	−5-V Supply
V_{CC}(PE)	+5-V Supply (Program Enable)
V_{DD}	+12-V Supply
V_{SS}	0 V Ground

description

The TMS2716 is an ultra-violet light-erasable, electrically programmable read-only memory. It has 16,384 bits organized as 2048 words of 8-bit length. The device is fabricated using N-channel silicon-gate technology for high-speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 circuits without the use of external pull-up resistors and each output can drive one Series 74 or 74LS TTL circuit without external resistors. The TMS2716 guarantees 250 mV dc noise immunity in the low state. Data outputs are three-state for OR-tying multiple devices on a common bus. The TMS2716 is plug-in compatible with the TMS2708 and the TMS27L08. Pin compatible mask programmed ROMs are available for large volume requirements.

This EPROM is designed for high-density fixed-memory applications where fast turn arounds and/or program changes are required. It is supplied in a 24-pin dual-in-line cerpak (JL suffix) package designed for insertion in mounting-hole rows on 600-mil (15,2 mm) centers. It is designed for operation from 0°C to 70°C.

operation (read mode)

address (A0-A10)

The address-valid interval determines the device cycle time. The 11-bit positive-logic address is decoded on-chip to select one of 2048 words of 8-bit length in the memory array. A0 is the least-significant bit and A10 most-significant bit of the word address.

chip select, program [S̄ (PGM)]

When the chip select is low, all eight outputs are enabled and the eight-bit addressed word can be read. When the chip select is high, all eight outputs are in a high-impedance state.

program

In the program mode, the chip select feature does not function as pin 18 inputs only the program pulse. The program mode is selected by the V_{CC}(PE) pin. Either 0 V or +12 V on this pin will cause the TMS2716 to assume program cycle.

data out (Q1-Q8)

The chip must be selected before the eight-bit output word can be read. Data will remain valid until the address is changed or the chip is deselected. When deselected, the three-state outputs are in a high-impedance state. The outputs will drive TTL circuits without external components.

DECEMBER 1979 – REVISED AUGUST 1983

- 1024 X 8 Organization
- All Inputs and Outputs Fully TTL Compatible
- Static Operation (No Clocks, No Refresh)
- Max Access/Min Cycle Time

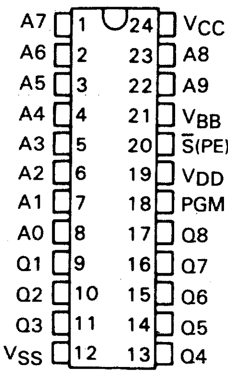
'2708-35	350 ns
'2708-45	450 ns
'27L08-45	450 ns

- 3-State Outputs for OR-Ties
- N-Channel Silicon-Gate Technology
- 8-Bit Output for Use in Microprocessor-Based Systems
- Power Dissipation

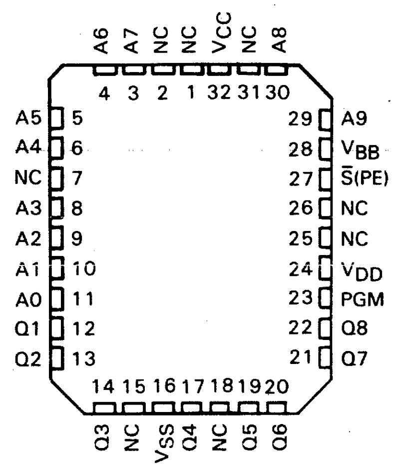
'27L08	580 mW Max Active
'2708	800 mW Max Active

- 10% Power Supply Tolerance (TMS27L08-45 and all SMJ' versions)
- Plug-Compatible Pin-Outs Allowing Interchangeability/Upgrade to 16K With Minimum Board Change
- Available in Full Military Temperature Range Versions (SMJ2708)

TMS2708 . . . JL PACKAGE
SMJ2708 . . . J PACKAGE
(TOP VIEW)



SMJ2708 . . . FE PACKAGE
(TOP VIEW)



NC – No Connection

description

The '2708-35, '2708-45, and '27L08-45 are ultraviolet light-erasable, electrically programmable read-only memories. They have 8,192 bits organized as 1024 words of 8-bit length. The devices are fabricated using N-channel silicon-gate technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54/74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 54/74 or 54LS/74LS TTL circuit without external resistors. The '27L08 guarantees 200 mV dc noise immunity in the high state and 250 mV in the low state. The data outputs for the '2708-35, '2708-45, and '27L08-45 are three-state for OR-tying multiple devices on a common bus.

PIN NOMENCLATURE	
A0-A7	Address Inputs
NC	No Connection
PGM	Program
Q1-Q8	Data Out
S̄(PE)	Chip Select/Program Enable
V_{BB}	−5-V Power Supply
V_{CC}	+5-V Power Supply
V_{DD}	+12-V Power Supply
V_{SS}	0-V Ground

Bipolar Programmable Read-Only Memories Product Guide

High-Performance
Schottky PROMs
Low-Power PROMs

TEXAS INSTRUMENTS

NUMERICAL INDEX
HIGH–PERFORMANCE SCHOTTKY PROMS

DEVICE	FUNCTION	AVAILABILITY
TBP18S030	32 X 8 PROM's	NOW
TBP18SA030		NOW
TBP24S10	256 X 4 PROM's	NOW
TBP24SA10		NOW
TBP24S41	1024 X 4 PROM's	NOW
TBP24SA41		NOW
TBP24S81	2048 X 4 PROM's	NOW
TBP24S81-55		NOW
TBP24SA81		NOW
TBP24SA81-55		NOW
TBP28L22	256 X 8 Low-Power PROM's	NOW
TBP28LA22		NOW
TBP28L42	512 X 8 Low-Power PROM's	NOW
TBP28L46		NOW
TBP28L86A	1024 X 8 Low-Power PROM's	▲
TBP28L166	2048 X 8 Low-Power PROM's	NOW
TBP28S42	512 X 8 PROM's	NOW
TBP28SA42		NOW
TBP28S46		NOW
TBP28SA46		NOW
TBP28S86A	1024 X 8 PROM's	NOW
TBP28S86A-50		NOW
TBP28SA86A		NOW
TBP28SA86A-50		NOW
TBP28S165	2048 X 8 PROM's	▲
TBP28S166		NOW
TBP28S2708A	1024 X 8 PROM's	NOW

▲ Planned for future announcement. Contact TI field sales office or authorized TI distributor for status.

Texas Instruments

MEMORY

TEXAS INSTRUMENTS
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TBP14S10 ('S287) This product is no longer in production, it is replaced by TBP24S10.

TBP14SA10 ('S387) This product is no longer in production, it is replaced by TBP24SA10.

TBP18S22 ('S471) This product is no longer in production, it is replaced by TBP28L22.

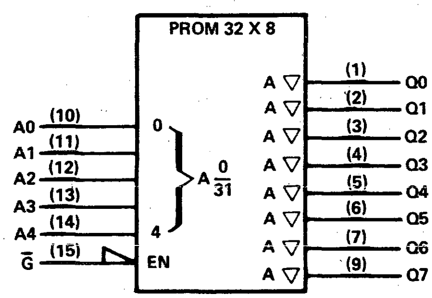
TBP18SA22 ('S470) This product is no longer in production, it is replaced by TBP28LA22.

TBP18S030 ('S288)

PROGRAMMABLE READ-ONLY MEMORIES

- 32 X 8
- Three-state outputs
- Typical address access time . . . 25 ns
- Typical power . . . 400 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	Q0	9	Q7
2	Q1	10	A0
3	Q2	11	A1
4	Q3	12	A2
5	Q4	13	A3
6	Q5	14	A4
7	Q6	15	$\overline{G}$
8	GND	16	V_{CC}

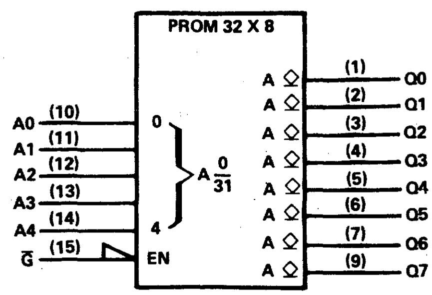
For chip carrier options and information, contact the factory.

TBP18SA030 ('S188)

PROGRAMMABLE READ-ONLY MEMORIES

- 32 X 8
- Open-collector outputs
- Typical address access time . . . 25 ns
- Typical power . . . 400 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	Q0	9	Q7
2	Q1	10	A0
3	Q2	11	A1
4	Q3	12	A2
5	Q4	13	A3
6	Q5	14	A4
7	Q6	15	$\overline{G}$
8	GND	16	V_{CC}

For chip carrier options and information, contact the factory.

TBP18S42 ('S472) This product is no longer in production, it is replaced by TBP28S42.

TBP18SA42 ('S473) This product is no longer in production, it is replaced by TBP28SA42.

TBP18S46 ('S474) This product is no longer in production, it is replaced by TBP28S46.

TBP18SA46 ('S475) This product is no longer in production, it is replaced by TBP28SA46.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
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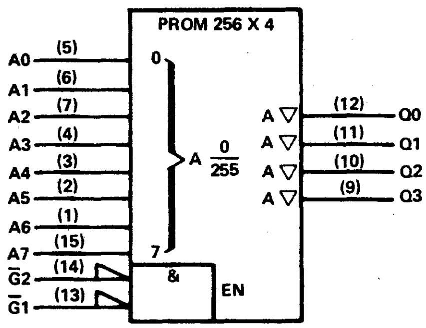
TBP24S10

PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 4
- Three-state outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 375 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A6	9 Q3
2 A5	10 Q2
3 A4	11 Q1
4 A3	12 Q0
5 A0	13 G1
6 A1	14 G2
7 A2	15 A7
8 GND	16 V_{CC}

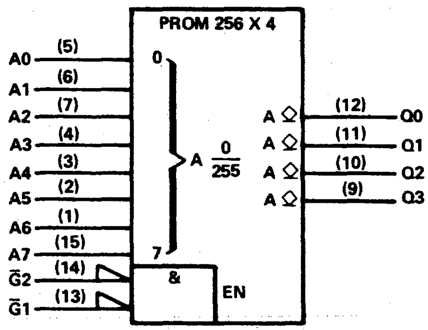
For chip carrier options and information, contact the factory.

TBP24SA10

PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 4
- Open-collector outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 375 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A6	9 Q3
2 A5	10 Q2
3 A4	11 Q1
4 A3	12 Q0
5 A0	13 G1
6 A1	14 G2
7 A2	15 A7
8 GND	16 V_{CC}

For chip carrier options and information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

For additional information on other Texas Instruments Military products, refer to the Military section.

TEXAS INSTRUMENTS
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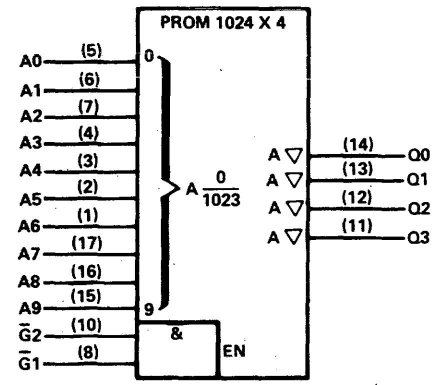
TBP24S41 ('S476)

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 4
- Three-state outputs
- Typical address access time . . . 40 ns
- Typical select time . . . 20 ns
- Typical power . . . 475 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A6	10 G̅2
2 A5	11 Q3
3 A4	12 Q2
4 A3	13 Q1
5 A0	14 Q0
6 A1	15 A9
7 A2	16 A8
8 G̅1	17 A7
9 GND	18 V_{CC}

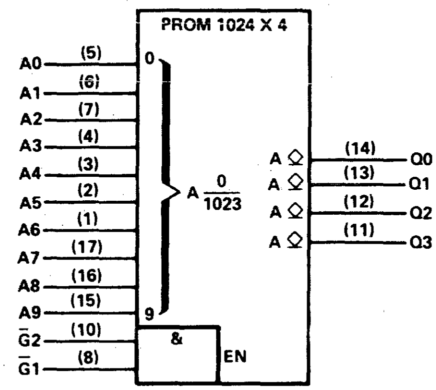
For chip carrier options and information, contact the factory.

TBP24SA41 ('S477)

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 4
- Open-collector outputs
- Typical address access time . . . 40 ns
- Typical select time . . . 20 ns
- Typical power . . . 475 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A6	10 G̅2
2 A5	11 Q3
3 A4	12 Q2
4 A3	13 Q1
5 A0	14 Q0
6 A1	15 A9
7 A2	16 A8
8 G̅1	17 A7
9 GND	18 V_{CC}

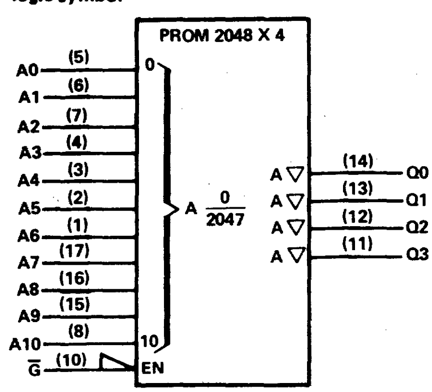
For chip carrier options and information, contact the factory.

TBP24S81 ('S454)
TBP24S81-55

PROGRAMMABLE READ-ONLY MEMORIES

- 2048 X 4
- Three-state outputs
- Typical address access time . . . 45 ns
- TBP24S81-55 maximum address access time . . . 55 ns
- Typical select time . . . 20 ns
- Typical power . . . 625 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A6	10 G̅
2 A5	11 Q3
3 A4	12 Q2
4 A3	13 Q1
5 A0	14 Q0
6 A1	15 A9
7 A2	16 A8
8 A10	17 A7
9 GND	18 V_{CC}

For chip carrier options and information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

For additional information on other Texas Instruments Military products, refer to the Military section.

TEXAS INSTRUMENTS
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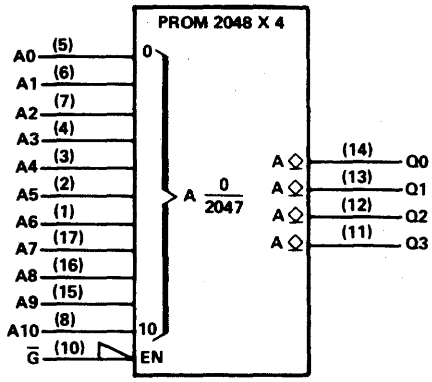
TBP24SA81 ('S455)
TBP24SA81-55

PROGRAMMABLE READ-ONLY MEMORIES

- 2048 X 4
- Open-collector outputs
- Typical address access time . . . 45 ns
- TBP24SA81-55 maximum address access time . . . 55 ns
- Typical select time . . . 20 ns
- Typical power . . . 625 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A6	10 $\overline{G}$
2 A5	11 Q3
3 A4	12 Q2
4 A3	13 Q1
5 A0	14 Q0
6 A1	15 A9
7 A2	16 A8
8 A10	17 A7
9 GND	18 V_{CC}

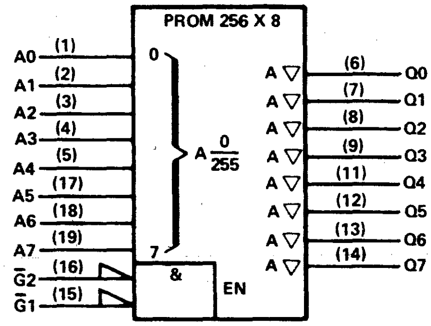
For chip carrier options and information, contact the factory.

TBP28L22

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 8
- Three-state outputs
- Typical address access time . . . 45 ns
- Typical select time . . . 20 ns
- Typical power . . . 375 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A0	11 Q4
2 A1	12 Q5
3 A2	13 Q6
4 A3	14 Q7
5 A4	15 $\overline{G}$1
6 Q0	16 $\overline{G}$2
7 Q1	17 A5
8 Q2	18 A6
9 Q3	19 A7
10 GND	20 V_{CC}

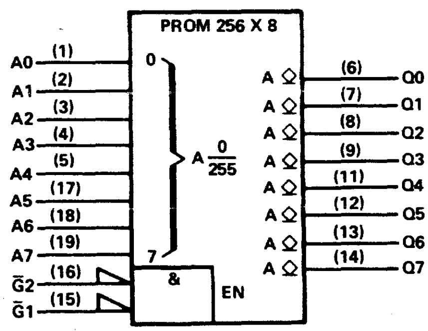
For chip carrier options and information, contact the factory.

TBP28LA22

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 8
- Open-collector outputs
- Typical address access time . . . 45 ns
- Typical select time . . . 20 ns
- Typical power . . . 375 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A0	11 Q4
2 A1	12 Q5
3 A2	13 Q6
4 A3	14 Q7
5 A4	15 $\overline{G}$1
6 Q0	16 $\overline{G}$2
7 Q1	17 A5
8 Q2	18 A6
9 Q3	19 A7
10 GND	20 V_{CC}

For chip carrier options and information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
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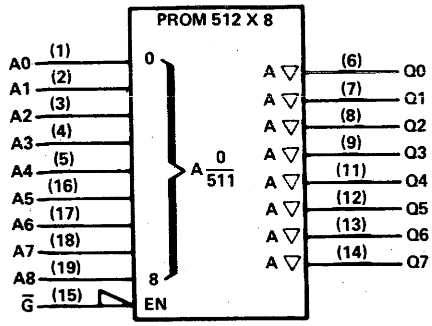
TBP28L42

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Typical address access time . . . 55 ns
- Typical select time . . . 25 ns
- Typical power . . . 275 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	A0	11	Q4
2	A1	12	Q5
3	A2	13	Q6
4	A3	14	Q7
5	A4	15	G̅
6	Q0	16	A5
7	Q1	17	A6
8	Q2	18	A7
9	Q3	19	A8
10	GND	20	V_{CC}

For chip carrier options and information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc – no internal connection.

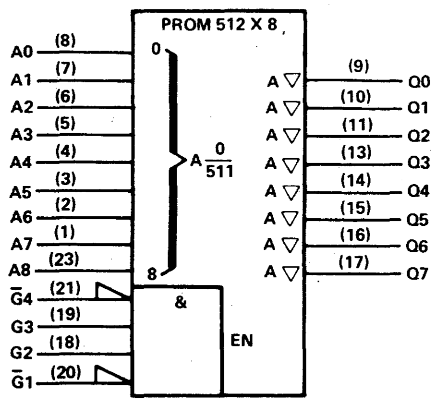
TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TBP28L45
TBP28L46

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Typical address access time . . . 55 ns
- Typical select time . . . 25 ns
- Typical power . . . 275 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 G̅1
9 Q0	21 G̅4
10 Q1	22 nc
11 Q2	23 A8
12 GND	24 V_{CC}

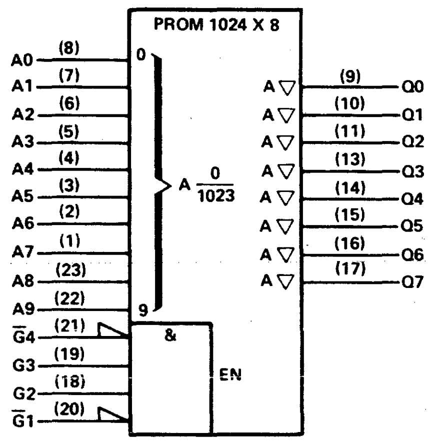
For chip carrier options and information, contact the factory.

TBP28L85A
TBP28L86A

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Three-state outputs
- Typical address access time . . . 65 ns
- Typical select time . . . 30 ns
- Typical power . . . 275 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 G̅1
9 Q0	21 G̅4
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

TBP28L86 ('LS478) **This product is no longer in production, it is replaced by TBP28L86A.**

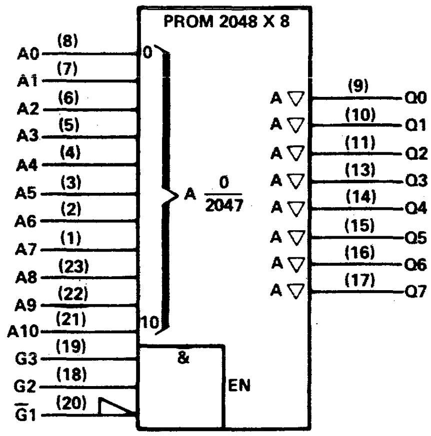
† Pin numbers shown on logic symbols are for J and N packages only.
nc – no internal connection.

TBP28L166

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 2048 X 8
- Three-state outputs
- Typical address access time ... 65 ns
- Typical select time ... 30 ns
- Typical power ... 350 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	A7	13	Q3
2	A6	14	Q4
3	A5	15	Q5
4	A4	16	Q6
5	A3	17	Q7
6	A2	18	G2
7	A1	19	G3
8	A0	20	$\overline{G1}$
9	Q0	21	A10
10	Q1	22	A9
11	Q2	23	A8
12	GND	24	V_{CC}

For chip carrier options and information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.

nc — no internal connection.

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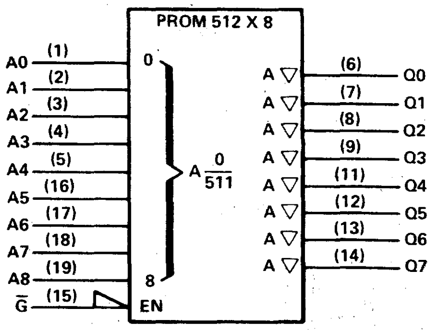
TBP28S42

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Typical address access time ... 35 ns
- Typical select time ... 20 ns
- Typical power ... 500 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A0	11 Q4
2 A1	12 Q5
3 A2	13 Q6
4 A3	14 Q7
5 A4	15 G̅
6 Q0	16 A5
7 Q1	17 A6
8 Q2	18 A7
9 Q3	19 A8
10 GND	20 V_{CC}

For chip carrier options and information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
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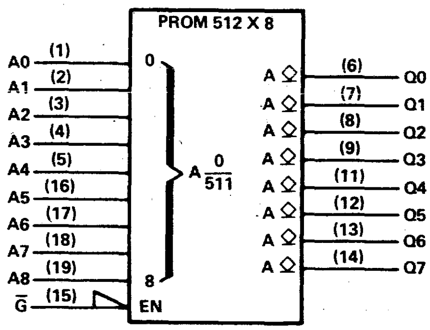
TBP28SA42

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Open-collector outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 500 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	A0	11	Q4
2	A1	12	Q5
3	A2	13	Q6
4	A3	14	Q7
5	A4	15	$\overline{G}$
6	Q0	16	A5
7	Q1	17	A6
8	Q2	18	A7
9	Q3	19	A8
10	GND	20	V_{CC}

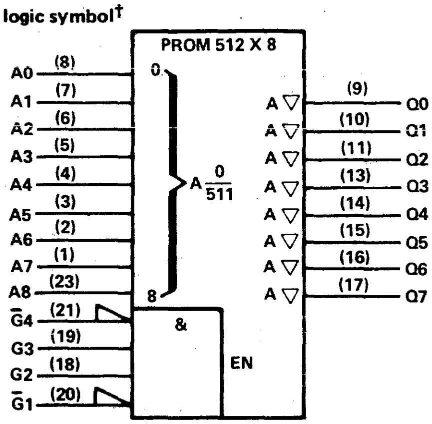
For chip carrier options and information, contact the factory.

TBP28S45
TBP28S46

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 500 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	A7	13	Q3
2	A6	14	Q4
3	A5	15	Q5
4	A4	16	Q6
5	A3	17	Q7
6	A2	18	G2
7	A1	19	G3
8	A0	20	$\overline{G1}$
9	Q0	21	$\overline{G4}$
10	Q1	22	nc
11	Q2	23	A8
12	GND	24	V_{CC}

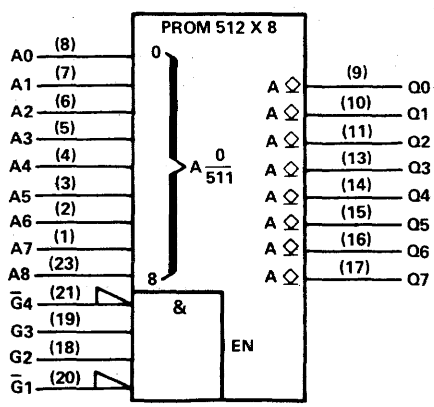
For chip carrier options and information, contact the factory.

TBP28SA45
TBP28SA46

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Open-collector outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 500 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	A7	13	Q3
2	A6	14	Q4
3	A5	15	Q5
4	A4	16	Q6
5	A3	17	Q7
6	A2	18	G2
7	A1	19	G3
8	A0	20	$\overline{G1}$
9	Q0	21	$\overline{G4}$
10	Q1	22	nc
11	Q2	23	A8
12	GND	24	V_{CC}

For chip carrier options and information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
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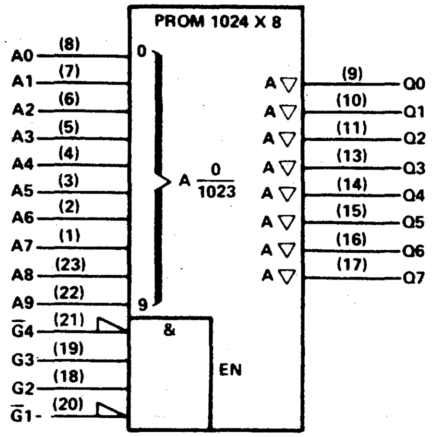
TBP28S85A
TBP28S85A-50

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Three-state outputs
- Typical address access time . . . 35 ns
- TBP28S85A-50 maximum address access time . . . 50 ns
- Typical select time . . . 20 ns
- Typical power . . . 550 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	A7	13	Q3
2	A6	14	Q4
3	A5	15	Q5
4	A4	16	Q6
5	A3	17	Q7
6	A2	18	G2
7	A1	19	G3
8	A0	20	$\overline{G1}$
9	Q0	21	$\overline{G4}$
10	Q1	22	A9
11	Q2	23	A8
12	GND	24	V_{CC}

For chip carrier options and information, contact the factory.

TBP28S86 ('S478)
TBP28S86-60

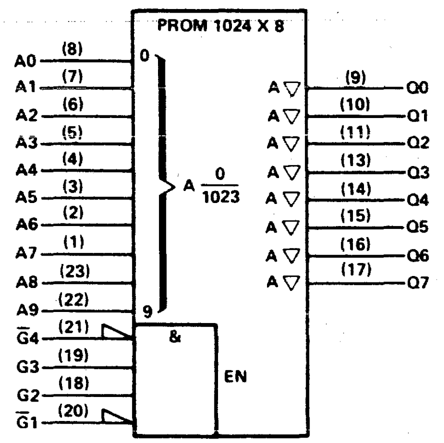
These products are no longer in production. They are replaced by TBP28S86A and TBP28S86A-50.

TBP28S86A
TBP28S86A-50

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Three-state outputs
- Typical address access time . . . 35 ns
- TBP28S86A-50 maximum address access time . . . 50 ns
- Typical select time . . . 20 ns
- Typical power . . . 550 mw

logic symbol†



pin assignments

J, N PACKAGES			
1	A7	13	Q3
2	A6	14	Q4
3	A5	15	Q5
4	A4	16	Q6
5	A3	17	Q7
6	A2	18	G2
7	A1	19	G3
8	A0	20	$\overline{G1}$
9	Q0	21	$\overline{G4}$
10	Q1	22	A9
11	Q2	23	A8
12	GND	24	V_{CC}

For chip carrier options and information, contact the factory.

TBP28SA86 ('S479)
TBP28SA86-60

These products are no longer in production. They are replaced by TBP28SA86A and TBP28SA86A-50.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TEXAS INSTRUMENTS
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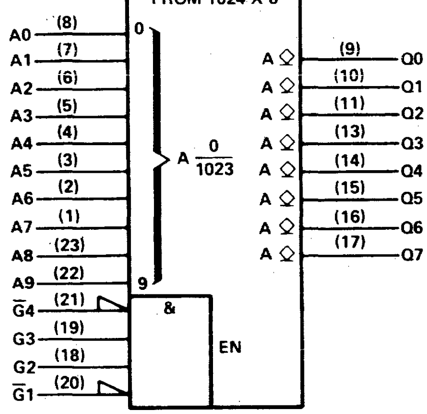
TBP28SA86A
TBP28SA86A-50

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Open-collector outputs
- Typical address access time . . . 35 ns
- TBP28SA86A-50 maximum address access time . . . 50 ns
- Typical select time . . . 20 ns
- Typical power . . . 550 mW

logic symbol†



pin assignments

J, N PACKAGES			
1	A7	13	Q3
2	A6	14	Q4
3	A5	15	Q5
4	A4	16	Q6
5	A3	17	Q7
6	A2	18	G2
7	A1	19	G3
8	A0	20	G̅1
9	Q0	21	G̅4
10	Q1	22	A9
11	Q2	23	A8
12	GND	24	V_{CC}

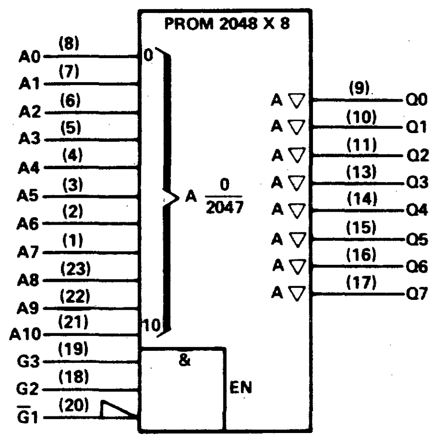
For chip carrier options and information, contact the factory.

TBP28S165
TBP28S166

PROGRAMMABLE READ-ONLY MEMORIES

- 2048 X 8
- Three-state outputs
- Typical select time . . . 15 ns

logic symbol†



pin assignments

J, N PACKAGES			
1	A7	13	Q3
2	A6	14	Q4
3	A5	15	Q5
4	A4	16	Q6
5	A3	17	Q7
6	A2	18	G2
7	A1	19	G3
8	A0	20	G̅1
9	Q0	21	A10
10	Q1	22	A9
11	Q2	23	A8
12	GND	24	V_{CC}

For chip carrier options and information, contact the factory.

TYPE	PACKAGE ROW SPACING	TYPICAL ADDRESS ACCESS TIME	GUARANTEED MAXIMUM ACCESS TIME	TYPICAL POWER DISSIPATION
TBP28S165	7.62 mm (0.300 in.)	25 ns		550 mW
TBP28S166	15,24 mm (0.600 in.)	35 ns		650 mW

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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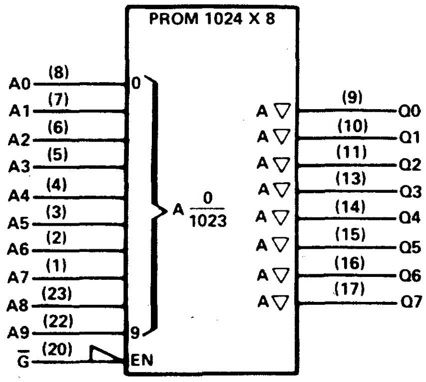
TBP28S2708 ('S2708) This product is no longer in production, it is replaced by TBP28S2708A.

TBP28S2708A

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Three-state outputs
- Typical select time . . . 20 ns
- Typical address access time . . . 35 ns
- Typical power dissipation . . . 550 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 nc
7 A1	19 nc
8 A0	20 G̅
9 Q0	21 nc
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier opions and information, contact the factory.

TIM8228 is the same as SN74S428

TIM8238 is the same as SN74S438

TIM9905 is the same as SN74LS251

TIM9906 is the same as SN74LS259

TIM9907 is the same as SN74148

TIM9908 is the same as SN74LS348

† Pin numbers shown on logic symbols are for J and N packages only.
nc – no internal connection.

TEXAS INSTRUMENTS
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VT2332/33

4096 x 8 STATIC READ ONLY MEMORY

FEATURES

- 4096 x 8-bit organization
- Single +5 V supply
- Access Time—250 ns (max)
- Totally static operation
- Completely TTL compatible
- VT2332 pin compatible with 2532
- VT2333 pin compatible with 2732
- 3-State Outputs for wired-OR expansion
- Two programmable Chip Selects
- 2708/2716/2532/2732 EPROMs accepted as program data inputs

DESCRIPTION

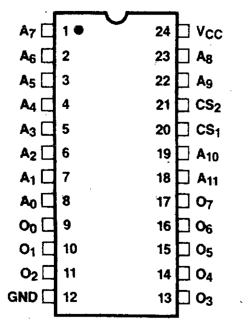
The VT2332/3 high-performance Read Only Memory is organized 4096 words by eight bits with access times of less than 250 ns. This ROM is designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. This device offers TTL input and output levels with a minimum of 0.4 V noise immunity in conjunction with a +5 V power supply.

The VT2332/3 operates totally asynchronously. No clock input is required. The two programmable Chip Selects allow up to four 32K ROMs to be wired-OR without external decoding. Both devices offer 3-state output buffers for memory expansion.

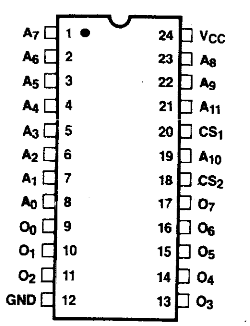
Designed to replace either the 2732 or 2532 32K EPROMs, the VT2332/3 can eliminate the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

PIN CONFIGURATIONS

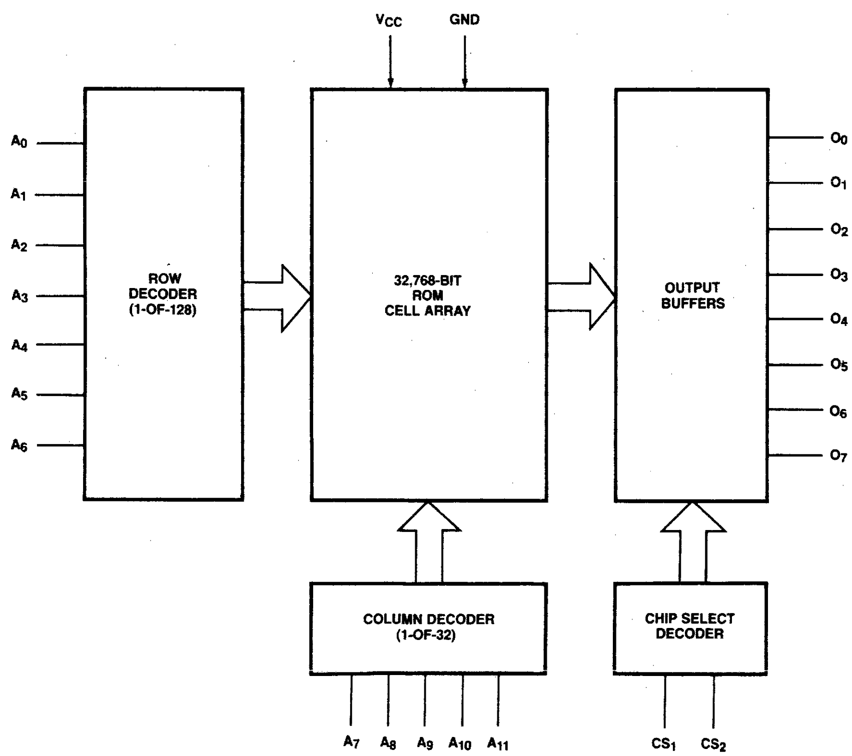
VT2332



VT2333



BLOCK DIAGRAM



VLSI Technology

MEMORY

VT2364

8192 x 8 STATIC READ ONLY MEMORY

FEATURES

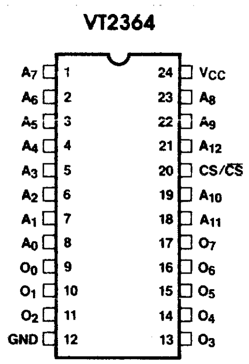
- 2732 EPROM pin compatible
- 8192 x 8-bit organization
- Single +5 V supply
- Access time—250 ns max
- Totally static operation
- Completely TTL compatible
- Operating Power: 45 mA (max)
- 24-Pin JEDEC approved pin-out
- Programmable Chip Select
- 3-state outputs for wired-OR expansion
- EPROMS accepted as program data input

DESCRIPTION

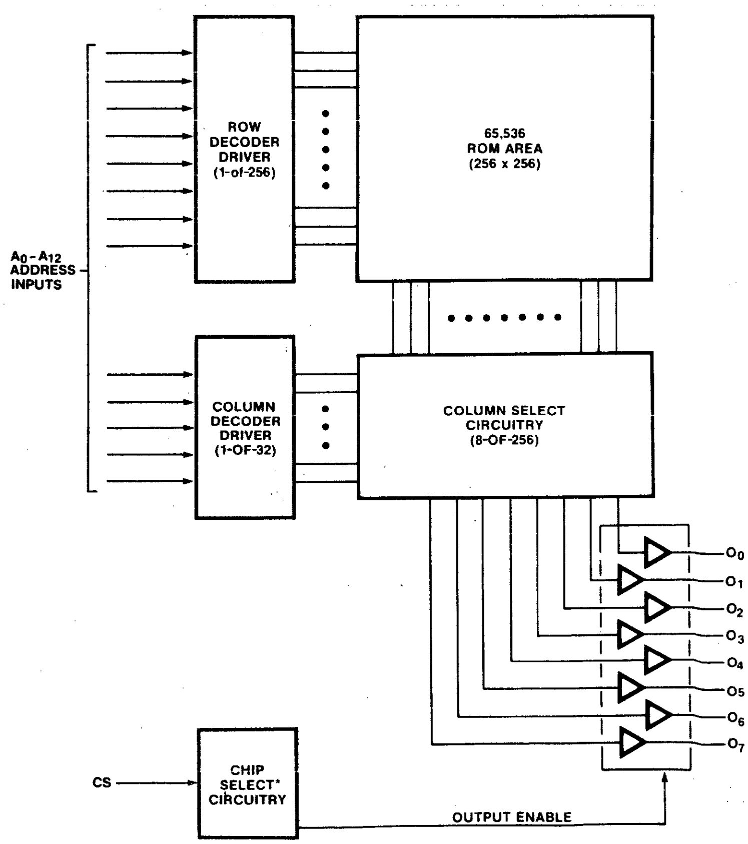
The VT2364 high-performance Read Only Memory is organized as 8,192 words by eight bits with an access time of 250 ns. The ROM is designed to be compatible with all microprocessors and similar applications where high-performance large-bit storage and simple interfacing are important design considerations. It conforms to the JEDEC approved pinouts for 24-pin 64K ROMs.

The VT2364 offers very simple operation with no power down. The programmable Chip Select allows two 64K ROMs to be Wired-OR without external decoding. It is pin compatible with the 2732 EPROM thus eliminating the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMS.

PIN CONFIGURATIONS



BLOCK DIAGRAM



*CHIP SELECT (CS) IS PROGRAMMABLE ACTIVE LOW OR ACTIVE HIGH.

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VT 2365/66

8,192 x 8 STATIC READ ONLY MEMORY

FEATURES

- 2764/2564 EPROM pin compatible
- 8,192 x 8-bit organization
- Single +5 V supply
- Access time—200 ns (max)
- Totally static operation
- Completely TTL compatible
- Power
  Operating: 45 mA (max)
  Standby: 10 mA (max)
- 28-Pin JEDEC approved pinout
- Automatic power down ($\overline{CE}$)
- Output Enable function ($\overline{OE}$)
- Programmable Chip Select
- 3-state outputs for wired-OR expansion
- EPROMs accepted as program data input

DESCRIPTION

The VT2365/66 high-performance Read Only Memory is organized 8,192 words by eight bits with an access time of 200 ns. The ROM is designed to be compatible with all microprocessors and similar applications where high-performance large-bit storage and simple interfacing are important design considerations. It conforms to the JEDEC approved pinout for 28-pin 64K ROMs.

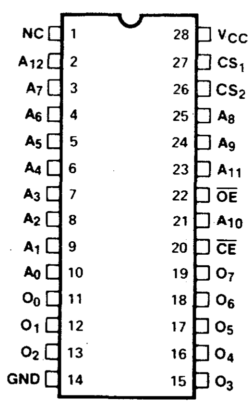
The VT2365/66 offers an automatic power down feature with power down controlled by the Chip Enable. ($\overline{CE}$) input. When $\overline{CE}$ goes HIGH, the device will automatically power down and remain in a low-power standby mode as long as $\overline{CE}$ remains HIGH.

This unique feature provides system level power savings of as much as 90%. The programmable Chip Selects allow up to four 64K ROMs to be wired-OR without external decoding. An additional feature of the VT2365 is the Output Enable ($\overline{OE}$) function which eliminates bus contention in multiple-bus microprocessor systems.

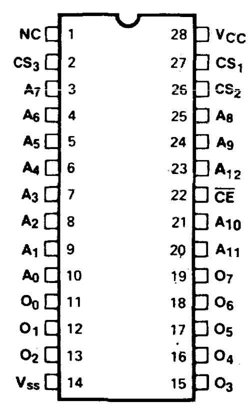
The VT2365 is pin compatible with the 2764 EPROM and the VT2366 is pin compatible with the 2564 EPROM, thus eliminating the need to redesign printed circuit boards for volume mask programmable ROMs after prototyping with EPROMs.

PIN CONFIGURATIONS

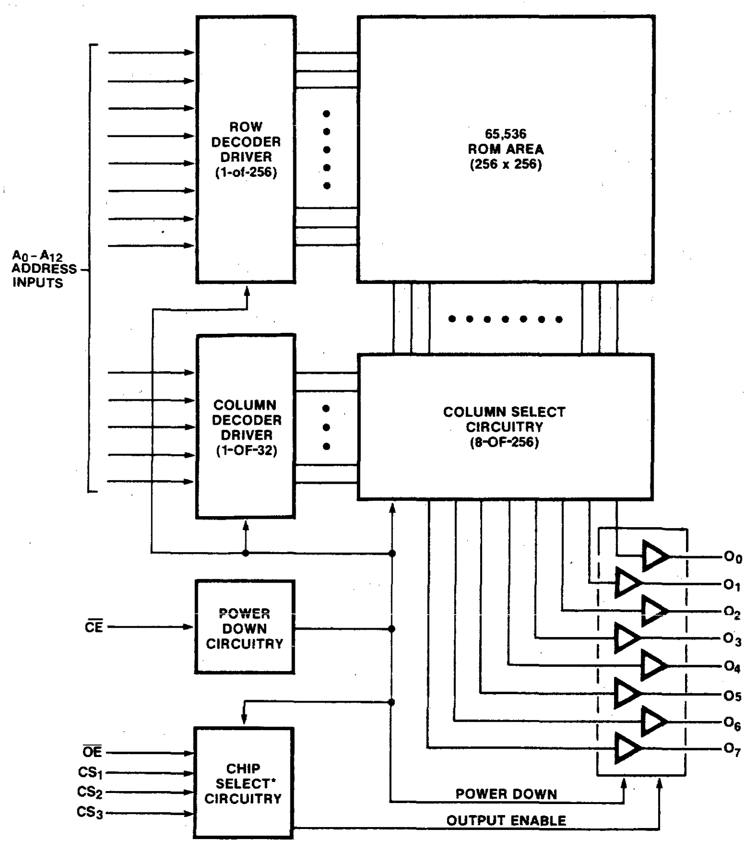
VT2365



VT2366



BLOCK DIAGRAM



*CHIP SELECT (CS) IS PROGRAMMABLE ACTIVE LOW OR ACTIVE HIGH.

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VT23128/29

16,384 x 8 STATIC READ ONLY MEMORY

FEATURES

- 16,384 x 8-bit organization
- Single +5 V supply
- Access time 170 ns max
- Totally static operation
- Completely TTL compatible
- Operating power 45 mA max
- Standby power 10 mA max
- Automatic power down (C̅E̅)
- Output enable function (O̅E̅)
- Programmable Chip Select
- 3-state outputs for wired-OR expansion
- 28-pin JEDEC approved pinouts
- VT23128 pin compatible with the 2764 EPROM
- VT23129 pin compatible with the 2564 EPROM
- EPROMs accepted as program data input

DESCRIPTION

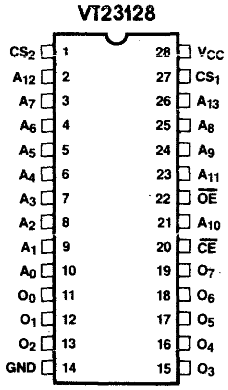
The VT23128/29 high-performance Read Only Memory is organized 16,384 words by eight bits with an access time of 170 ns. It is designed to be compatible with all microprocessors and similar applications where high-performance large-bit storage and simple interfacing are important design considerations.

The VT23128/29 offers automatic power down with power down controlled by the Chip Enable (C̅E̅) input. When C̅E̅ goes HIGH, the device will automatically power down and remain in a low-power standby mode as long as C̅E̅ remains HIGH. This unique feature provides system level power savings of as much as 90%. The VT23128 also has an Output Enable (O̅E̅) function to eliminate bus contention in multiple-bus microprocessor systems. The programmable Chip Select allows up to eight 128K ROMs to be wired-OR without external decoding.

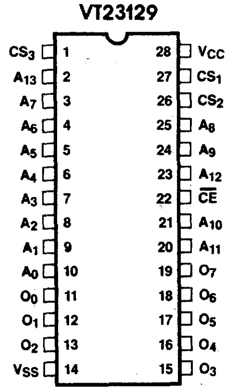
The VT23128 is pin compatible with the 2764 EPROM and the VT23129 is pin compatible with the 2564 EPROM, thus eliminating the need to redesign printed circuit boards for volume mask programmable ROMs after prototyping with EPROMS.

PIN CONFIGURATION

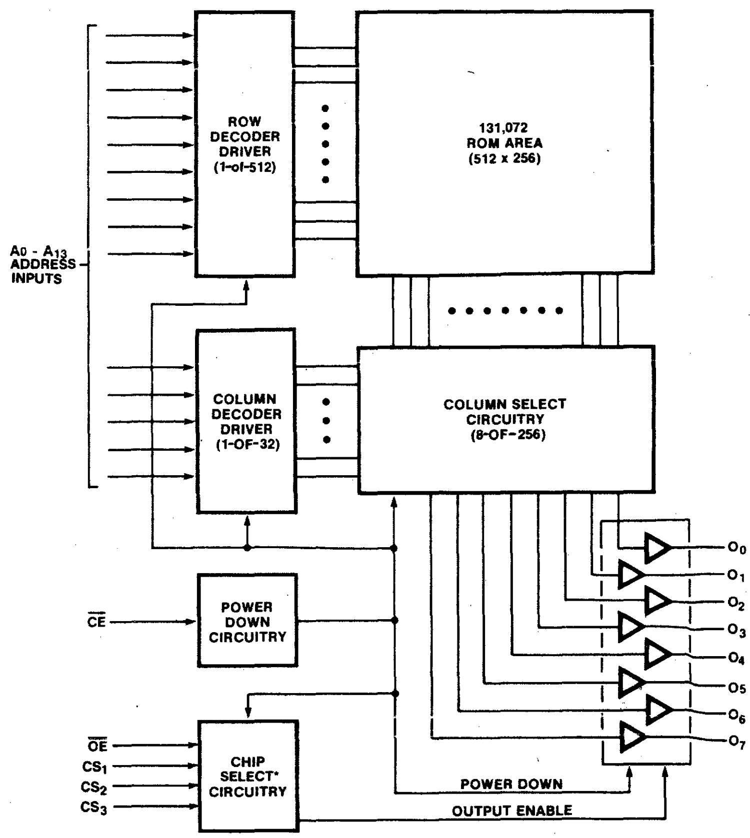
VT23128



VT23129



BLOCK DIAGRAM



*CHIP SELECT (CS) IS PROGRAMMABLE ACTIVE LOW, ACTIVE HIGH, OR DON'T CARE

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VT23256/57 PRELIMINARY

32,768 x 8 STATIC READ ONLY MEMORY

FEATURES

- 32,768 x 8-bit organization
- Single +5 V supply
- Access time 200 ns max
- Totally static operation
- Completely TTL compatible
- Operating power 60 mA max
- Standby power 10 mA max
- Automatic power down ($\overline{CE}$)
- Output Enable function ($\overline{OE}$)
- Programmable Chip Select
- 3-state outputs for wired-OR expansion
- 28-pin JEDEC approved pinouts
- VT23256 pin compatible with the 2764 EPROM
- VT23257 pin compatible with the 2564 EPROM
- EPROMs accepted as program data input

DESCRIPTION

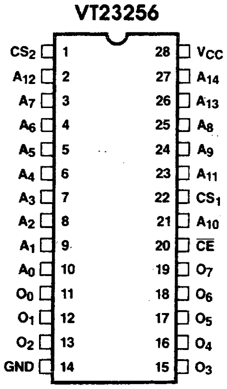
The VT23256/57 high-performance Read Only Memory is organized words by eight bits with an access time of 200 ns. It is designed to be compatible with all microprocessors and similar applications where high-performance large-bit storage and simple interfacing are important design considerations.

The VT23256/57 offers automatic power down with power down controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes HIGH, the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$ remains HIGH. This unique feature provides system level power savings of as much as 90%. The VT23256/57 also has an Output Enable ($\overline{OE}$) function to eliminate bus contention in multiple-bus microprocessor systems. The programmable Chip Select allows up to four 256K ROMs to be wired-OR without external decoding.

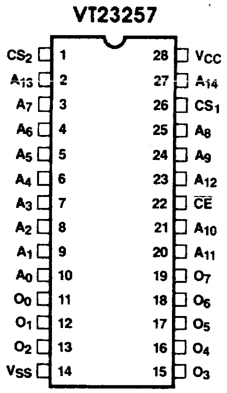
The VT23256 is pin compatible with the 2764 EPROM and the VT23257 is pin compatible with the 2564 EPROM, thus eliminating the need to redesign printed circuit boards for volume mask programmable ROMs after prototyping with EPROMS.

PIN CONFIGURATION

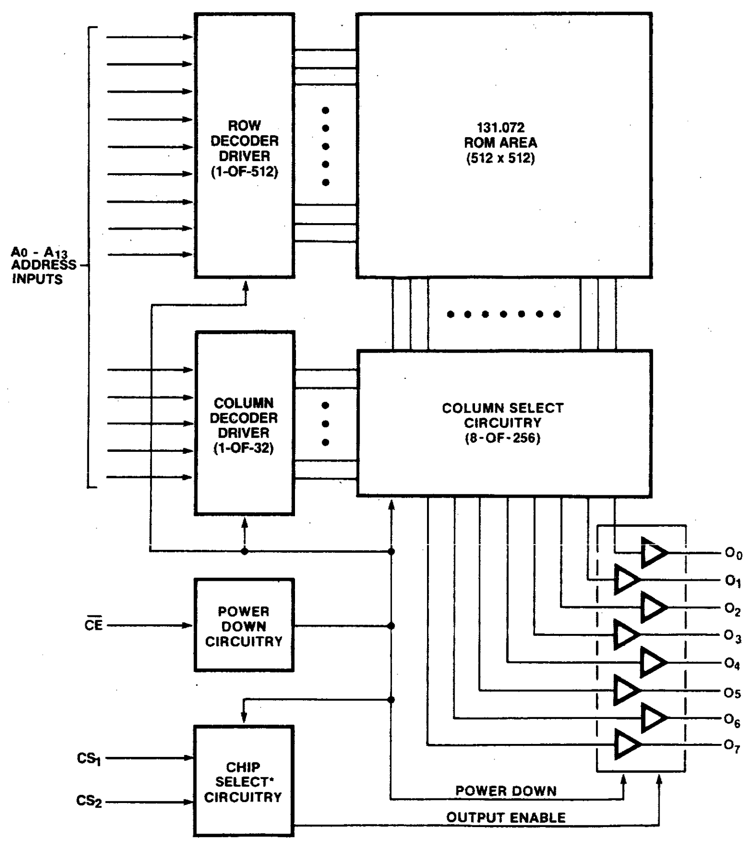
VT23256



VT23257



BLOCK DIAGRAM



*CHIP SELECT (CS) IS PROGRAMMABLE ACTIVE LOW OR ACTIVE HIGH.

VLSI Technology

MEMORY

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VL4500A

DYNAMIC RAM CONTROLLER

FEATURES

- Controls operation of 8K/16K/32K/64K dynamic RAMs
- Creates static RAM appearance
- One package contains address multiplexer, refresh control and timing control
- Directly addresses and drives up to 256K bytes of memory without external drivers
- Operates from microprocessor clock
  - No crystals, delay lines, or RC networks
  - Eliminates arbitration delays
- Refresh may be internally or externally initiated
- Versatile
  - Strap-selected refresh rate
  - Synchronous, predictable refresh
  - Selection of distributed, transparent, and cycle-steal refresh modes
  - Interfaces easily to popular microprocessors
- Strap-selected wait state generation for microprocessor/memory speed matching
- Ability to synchronize or interleave controller with the microprocessor system (including multiple controllers)
- Three-state outputs allow multiport memory configuration
- Performance ranges of 150 ns/200 ns/250 ns
- Compatible with TI TMS 4500A

DESCRIPTION

The VL4500A is a monolithic DRAM system controller designed to provide address multiplexing, timing, control and refresh/access arbitration functions to simplify the interface of dynamic RAMs to microprocessor systems.

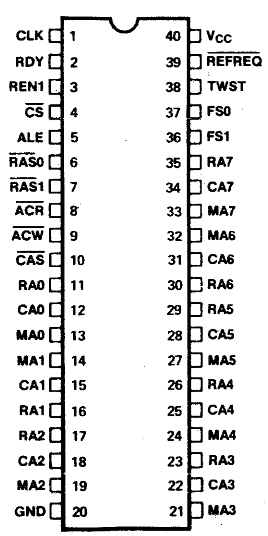
The controller contains a 16-bit multiplexer that generates the address lines for the memory device from the 16 system address bits and provides the strobe signals required by the memory to decode the address. An 8-bit refresh counter generates the 256-row addresses required to refresh.

A refresh timer is provided that generates the necessary timing to refresh the dynamic memories and assure data retention.

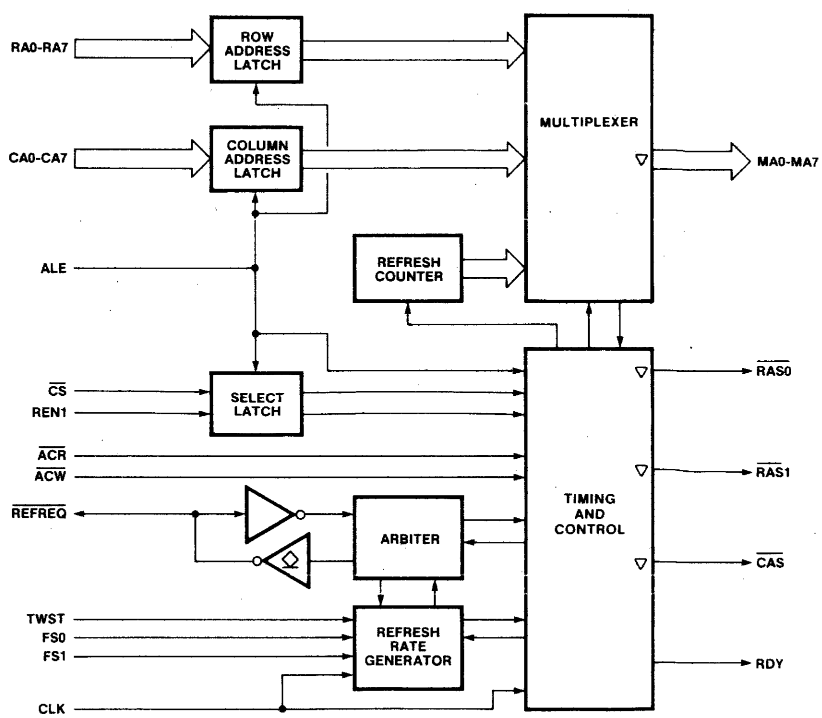
The VL4500A also contains refresh/access arbitration circuitry to resolve conflicts between memory access requests and memory refresh cycles. The VL4500A is offered in a 40-pin, 600-mil dual in-line plastic package and is guaranteed for operation from 0°C to 70°C.

PIN CONFIGURATION

(Top View)



BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Operating Ambient Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Supply Voltage Range, V_{CC}[1]	−1.5 to 7 V
Input Voltage Range (any input)[1]	−1.5 to 7 V
Continuous Power Dissipation	1.2 W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS: T_A = 0°C to +70°C

Symbol	Parameter	Min	Nom	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH} (except $\overline{\text{REFREQ}}$)	High-Level Input Voltage	2.0		6.0	V
V_{IH} ($\overline{\text{REFREQ}}$)	High-Level Input Voltage	2.4		6.0	V
V_{IL} (except $\overline{\text{REFREQ}}$)	Low-Level Input Voltage	−1.0[2]		0.8	V
V_{IL} ($\overline{\text{REFREQ}}$)	Low-Level Input Voltage	−1.0[2]		1.2	V

DC CHARACTERISTICS: T_A = 0°C to +70°C, V_{CC} = 5 V ± 10%

Symbol	Parameter		Test Conditions		Min	Typ[3]	Max	Unit
V_{OH}	High-Level Output Voltage	MA0-MA7, RDY	I_{OH} = −1 mA	V_{CC} = 4.5 V	2.4			V
		$\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$, $\overline{\text{CAS}}$			2.7			
		$\overline{\text{REFREQ}}$	I_{OH} = 100 μA	V_{CC} = 4.5 V	2.4			
V_{OL}	Low-Level Output Voltage		I_{OL} = 4 mA	V_{CC} = 4.5 V			0.4	V
I_{IH}	High-Level Input Current	$\overline{\text{REFREQ}}$	V_I = 5.5 V				100	μA
		All others					10	
I_{IL}	Low-Level Input Current	$\overline{\text{REFREQ}}$	V_I = 0 V				−1.25	mA
		All others					−10	μA
I_{OZ}	Off-State Output Current		V_O = 0 to 4.5 V	V_{CC} = 5.5 V			±50	μA
I_{CC}	Operating Supply Current		T_A = 0°C	V_{CC} = 5.5 V		100	140	mA
C_I	Input Capacitance		V_I = 0 V	f = 1 MHz		5		pF
C_O	Output Capacitance		V_O = 0 V	f = 1 MHz		6		pF

Notes:

1. Voltage values are with respect to the ground terminal.
2. The algebraic convention, where the more negative limit is designated as minimum, is used in this data sheet for logic voltage levels only.
3. All typical values are at V_{CC} = 5 V, T_A = 25°C except where otherwise noted.

AC CHARACTERISTICS: $T_A = 0°C$ to $+70°C$, $V_{CC} = 5\ V \pm 10\%$

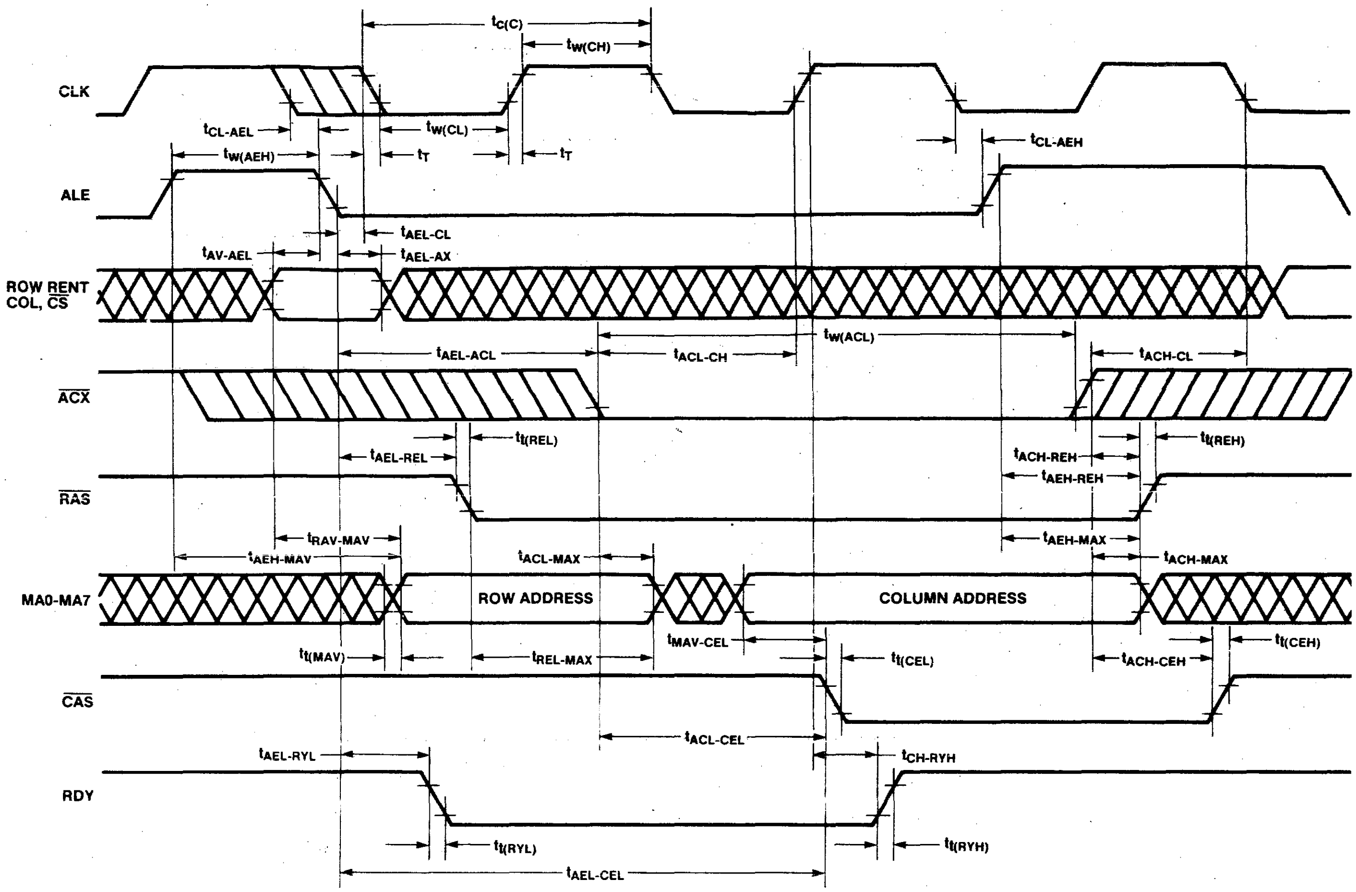
Symbol	Parameter	VL4500A-15PC Min	VL4500A-15PC Max	VL4500A-20PC Min	VL4500A-20PC Max	VL4500A-25PC Min	VL4500A-25PC Max	Unit
$t_{C(C)}$	CLK Cycle Time	100		100		140		
$t_{W(CH)}$	CLK High Pulse Width	20		20		20		
$t_{W(CL)}$	CLK Low Pulse Width	35		35		35		
t_t	Transition Time, All Inputs		50		50		50	
$t_{AEL\text{-}CL}$	Time Delay, ALE Low to CLK Starting Low(1)	10		10		15		
$t_{CL\text{-}AEL}$	Time Delay, CLK Low to ALE Starting Low(1)	10		10		15		
$t_{CL\text{-}AEH}$	Time Delay, CLK Low to ALE Starting High(2)	15		20		20		
$t_{W(AEH)}$	Pulse Width ALE High	50		60		60		ns
$t_{AV\text{-}AEL}$	Time Delay, Address, REN1, $\overline{CS}$ Valid to ALE Low	5		10		15		
$t_{AEL\text{-}AX}$	Time Delay, ALE Low to Address Not Valid	10		10		10		
$t_{AEL\text{-}ACL}$	Time Delay, ALE Low to $\overline{ACX}$ Low(3, 4, 5, 6)	$t_{h(RA)} + 30$		$t_{h(RA)} + 40$		$t_{h(RA)} + 50$		
$t_{ACH\text{-}CL}$	Time Delay, $\overline{ACX}$ High to CLK Low(3, 7)	20		20		20		
$t_{ACL\text{-}CH}$	Time Delay, $\overline{ACX}$ Low to CLK Starting High (to remove RDY)	30		30		30		
$t_{RQL\text{-}CL}$	Time Delay, $\overline{REFREQ}$ Low to CLK Starting Low(8)	20		20		20		
$t_{W(RQL)}$	Pulse Width, $\overline{REFREQ}$ Low	20		20		20		

Notes:

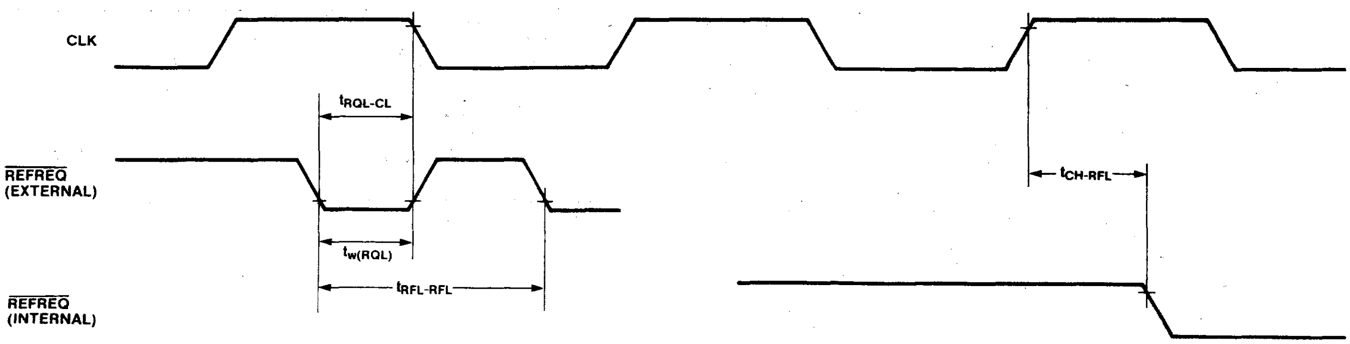
1. Coincidence of the trailing edge of CLK and the trailing edge of ALE should be avoided, as the refresh/access occurs on the trailing CLK edge. A trailing edge of CLK should occur during the interval from $\overline{ACX}$ high to ALE low.
2. If ALE rises before $\overline{ACX}$ and a refresh request is present, the falling edge of CLK after $t_{CL\text{-}AEH}$ will output the refresh address to MA0-MA7 and initiate a refresh cycle.
3. These specifications relate to system timing and do not directly reflect device performance.
4. On the access grant cycle following refresh, the occurrence of $\overline{CAS}$ low depends on the relative occurrence of ALE low to $\overline{ACX}$ low. If $\overline{ACX}$ occurs prior to or coincident with ALE then $\overline{CAS}$ is timed from the CLK high transition that causes RAS low. If $\overline{ACX}$ occurs 20 ns or more after ALE then $\overline{CAS}$ is timed from the CLK low transition following the CLK high transition causing RAS low.
5. For maximum speed access (internal delays on both access and access grant cycles), $\overline{ACX}$ should occur prior to or coincident with ALE.
6. $t_{h(RA)}$ is the dynamic memory row address hold time. $\overline{ACX}$ should follow ALE by $t_{AEL\text{-}CEL}$ in systems where the required $t_{h(RA)}$ is greater than $t_{REL\text{-}MAX}$ minimum.
7. Minimum of 20 ns is specified to ensure arbitration will occur on falling CLK edge. $t_{ACH\text{-}CL}$ also affects precharge time such that the minimum $t_{ACH\text{-}CL}$ should be equal or greater than: $t_{W(RH)}\text{-}t_{W(CL)}$ + 30 ns (for cycle where $\overline{ACX}$ high occurs prior to ALE high) where $t_{W(RH)}$ is the DRAM $\overline{RAS}$ precharge time.
8. This parameter is necessary only if refresh arbitration is to occur on this low-going CLK edge (in systems where refresh is synchronized to external events).

TIMING DIAGRAMS

ACCESS CYCLE TIMING



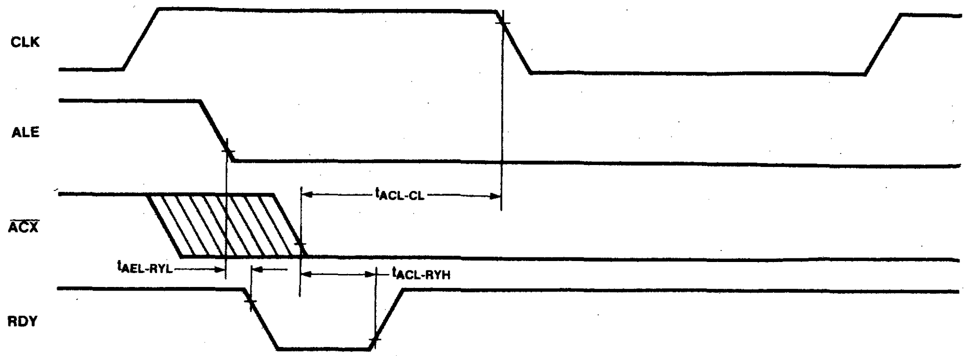
REFRESH REQUEST TIMING



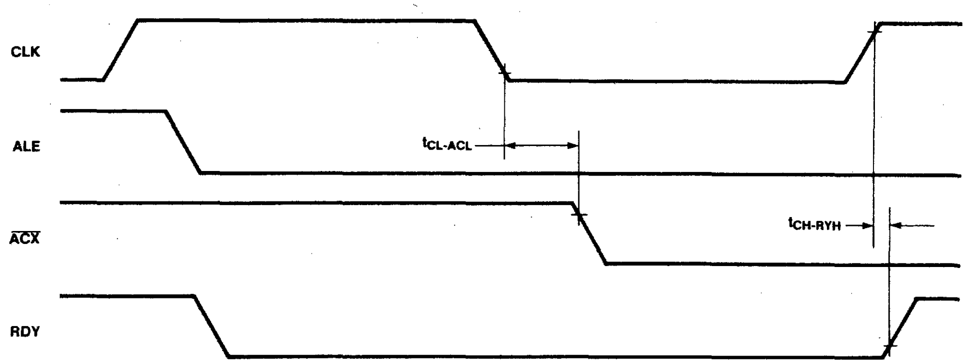
VLSI Technology

MEMORY

READY (RDY) SIGNAL TIMING (WAIT STATE OPERATION, TWST = 1)



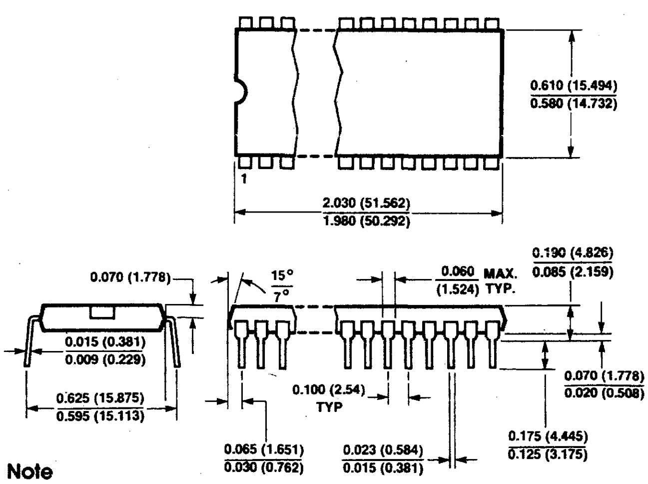
RDY starting high is timed from $\overline{ACX}$ low ($t_{ACL\text{-}RYH}$) for the condition $\overline{ACX}$ going low while CLK high.



RDY starting high is timed from CLK high ($t_{CH\text{-}RYH}$) for the condition $\overline{ACX}$ going low while CLK low.

PACKAGE DIAGRAM

40-LEAD PLASTIC DUAL IN-LINE (P—DIP) PACKAGE



Note

1. All metric dimensions are in parenthesis ().

ORDERING INFORMATION

VL4500A-15PC (TMS4500AN-15)	150 ns	Plastic, commercial, 0 – 70°C
VL4500A-20PC (TMS4500AN-20)	200 ns	Plastic, commercial, 0 – 70°C
VL4500A-25PC (TMS4500AN-25)	250 ns	Plastic, commercial, 0 – 70°C

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NEW PRODUCT BULLETIN

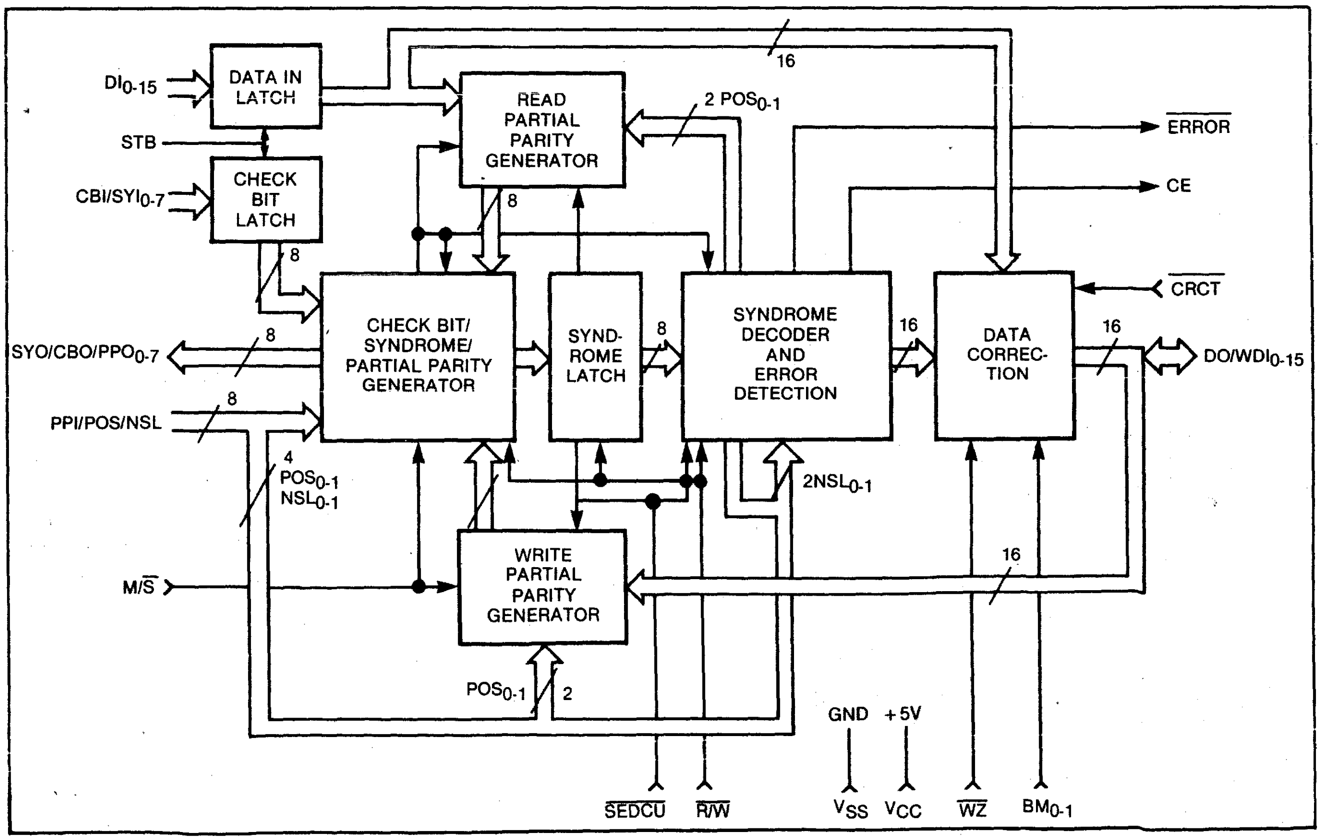
Error Detection and Correction Unit WD8206

FEATURES

- DETECTS AND CORRECTS ALL SINGLE BIT ERRORS
- DETECTS ALL DOUBLE BIT AND MOST MULTIPLE BIT ERRORS
- 52 NS MAXIMUM FOR DETECTION; 67 NS MAXIMUM FOR CORRECTION (16 BIT SYSTEM)
- EXPANDABLE TO HANDLE 80 BIT MEMORIES
- SYNDROME OUTPUTS FOR ERROR LOGGING
- SEPARATE INPUT AND OUTPUT BUSSES — NO TIMING STROBES REQUIRED
- SUPPORTS READS WITH AND WITHOUT CORRECTION, WRITES, PARTIAL (BYTE) WRITES, AND READ-MODIFY-WRITES
- NMOS TECHNOLOGY FOR LOW POWER
- COMPATIBLE WITH INTEL 8206 DEVICE
- 68 PIN LEADLESS JEDEC PACKAGE
- SINGLE +5V SUPPLY

DESCRIPTION

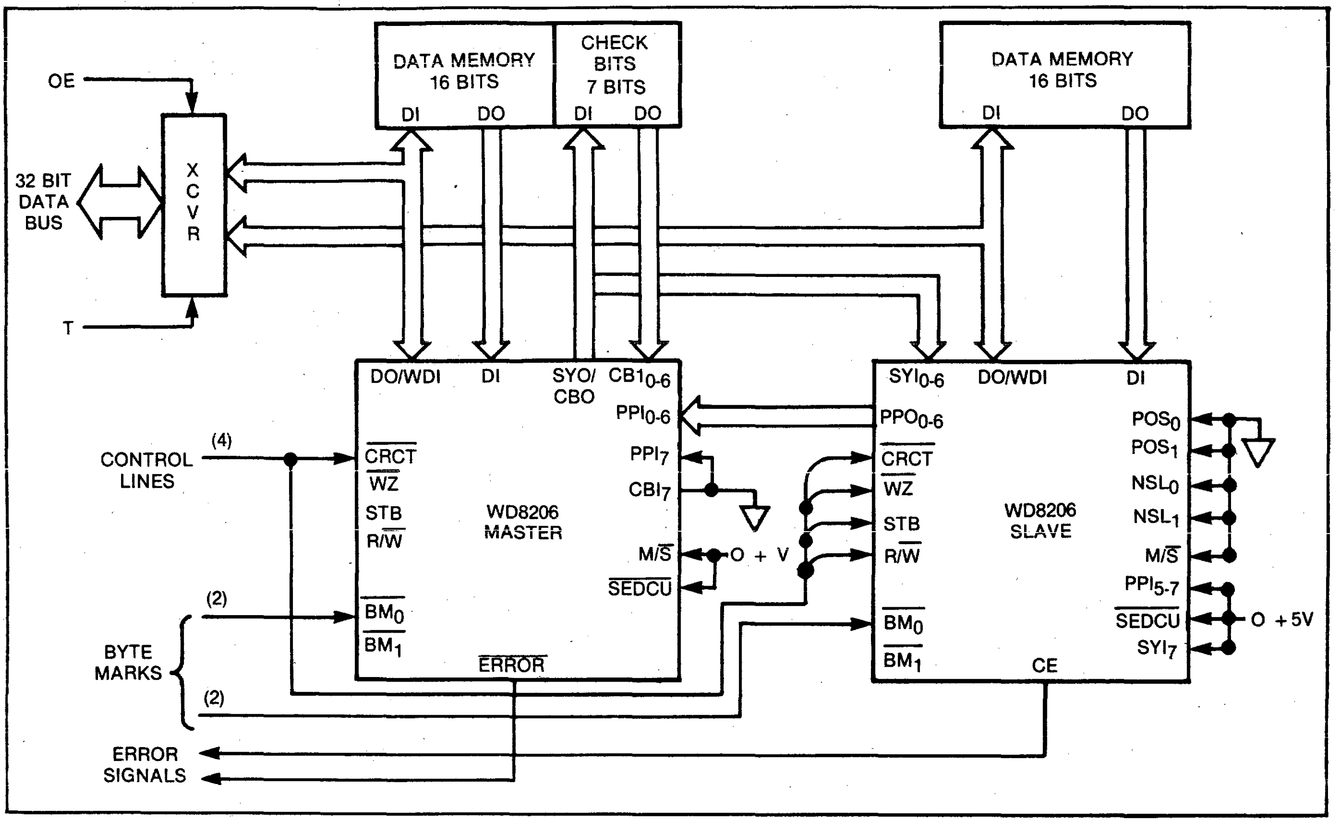
The NMOS 8206 Error Detection and Correction Unit is a high-speed device that provides error detection and correction for memory systems (static and dynamic) requiring high reliability and performance. Each WD8206 handles 8 or 16 data bits and up to 8 check bits. WD8206's can be cascaded to provide correction and detection for up to 80 bits of data. Other WD8206 features include the ability to handle byte writes, memory initialization, and error logging.



WD8206 BLOCK DIAGRAM

PROPOSED APPLICATIONS

The WD8206 interface to a typical 32 bit memory system is illustrated below. For larger systems, the partial parity bits from slaves two to four must be XOR'ed externally, which calls for one level of XOR gating for three WD8206's and two levels for four or five WD8206's.



SIMPLIFIED SYSTEM DIAGRAM

WESTERN DIGITAL
C O R P O R A T I O N

2445 McCABE WAY
IRVINE, CALIFORNIA 92714

(714) 863-0102, TWX 910-595-1139

NEW PRODUCT BULLETIN

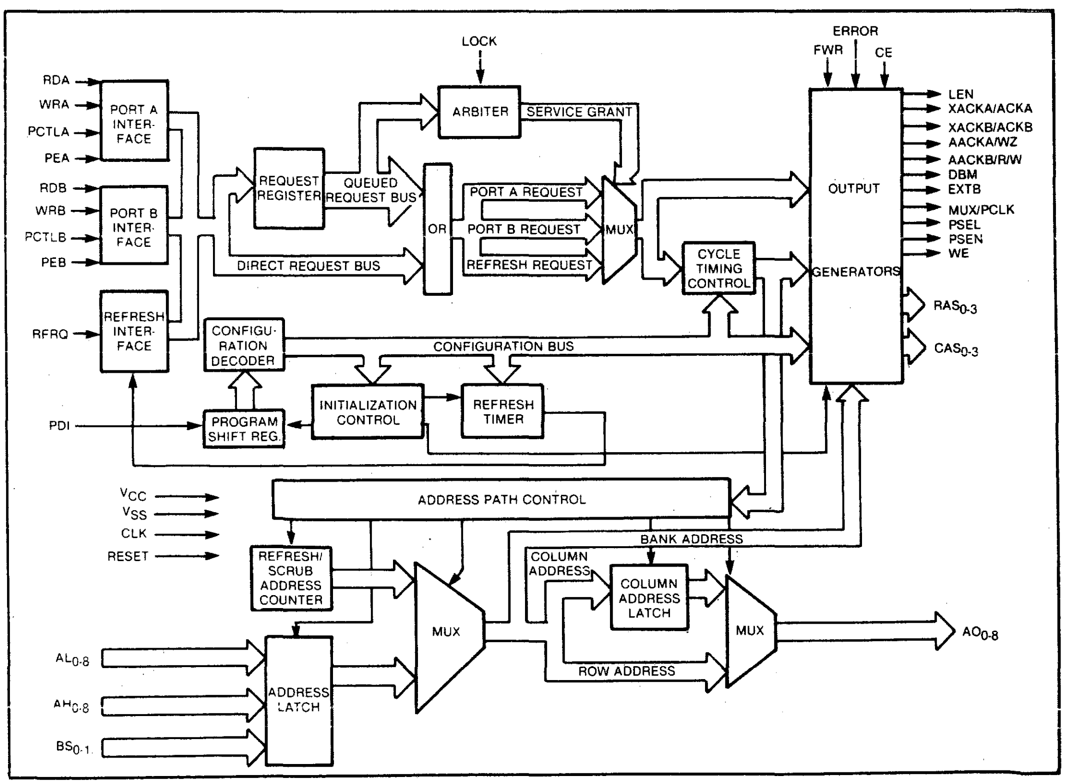
Advanced Dynamic RAM Controller WD8207

FEATURES

- PROVIDES ALL SIGNALS NECESSARY TO CONTROL 16K, 64K AND 256K DYNAMIC RAMS
- DIRECTLY ADDRESSES AND DRIVES UP TO 2 MEGABYTES WITHOUT EXTERNAL DRIVERS
- SUPPORTS SINGLE AND DUAL-PORT CONFIGURATIONS
- AUTOMATIC RAM INITIALIZATION IN ALL MODES
- FIVE PROGRAMMABLE REFRESH MODES
- TRANSPARENT MEMORY SCRUBBING IN ECC MODE
- DATA TRANSFER ACKNOWLEDGE SIGNALS FOR EACH PORT
- PROVIDES SIGNALS TO DIRECTLY CONTROL THE WD8206 ERROR DETECTION AND CORRECTION UNIT
- SUPPORTS SYNCHRONOUS OR ASYNCHRONOUS OPERATION ON EITHER PORT
- SINGLE +5V SUPPLY

DESCRIPTION

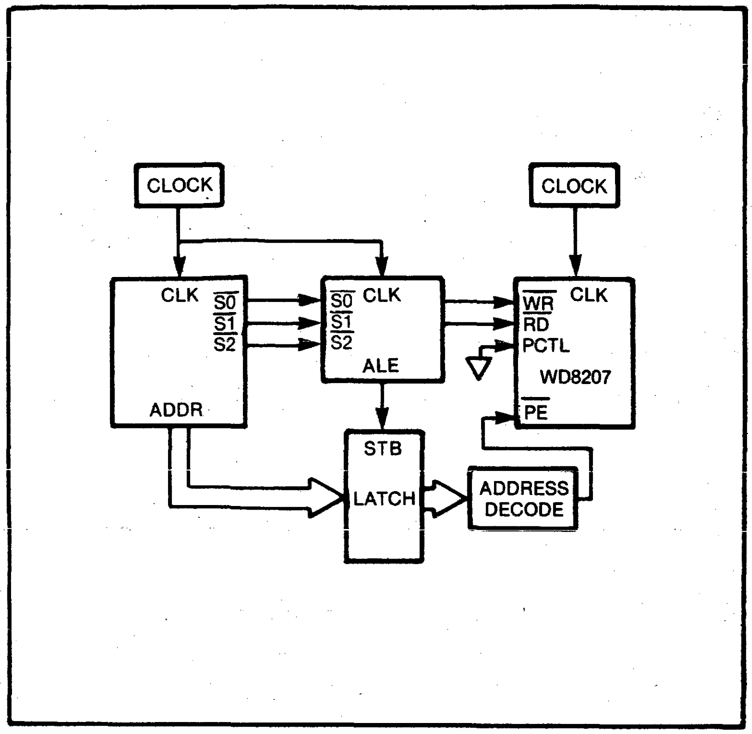
The WD8207 is a 68-pin leadless JEDEC type A hermetic chip carrier. The WD8207 Advanced Dynamic RAM Controller (ADRC) is a high-performance, systems-oriented, Dynamic RAM controller that is designed to easily interface 16K, 64K and 256K Dynamic RAMs microprocessor Systems. A dual-port interface allows two different busses to independently access memory. When configured with a WD8206 Error Detection and Correction Unit the WD8207 supplies the necessary logic for designing large error-corrected memory arrays. This combination provides automatic memory initialization and transparent memory error scrubbing.



WD8207 BLOCK DIAGRAM

PROPOSED APPLICATIONS

The ADRC supports several microprocessor interface options including synchronous and asynchronous connection.



SIMPLIFIED SYSTEM DIAGRAM

WESTERN DIGITAL CORPORATION
2445 McCABE WAY
IRVINE, CALIFORNIA 92714
(714) 863-0102, TWX 910-595-1139

PRELIMINARY DATA SHEET

X2444 / X2444I — 256 Bit Serial Nonvolatile Static RAM

16x16 Bit Serial NOVRAM*

- **Ideal for use with Single Chip Microcomputers**
  - **Static Timing 1 MHz Operation**
  - **Minimum I/O Interface**
  - **Serial Port Compatible (COPS™, 8051)**
  - **Minimum Support Circuits**
- **Software and Hardware Control of Nonvolatile Functions**
  - **Maximum Store Protection**
- **TTL Compatible**
- **16x16 Organization**
- **X2444 Emulator Available—X2444E**
- **Reliable N-Channel Floating Gate Technology**
- **Single 5V Supply**
- **Low Power Dissipation**
  - **Active Current: 15mA Typ.**
  - **Store Current: 8mA Typ.**
  - **Standby Current: 6mA Typ.**
  - **Sleep Current: 5mA Typ.**
- **8-Pin Mini-Dip**
  - **Low Cost**
  - **Compact**

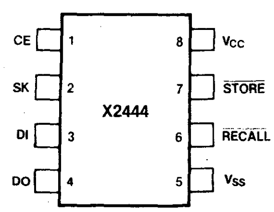
The X2444 is a 256-bit Xicor NOVRAM memory fabricated in Xicor's proven NMOS technology. The device is organized as 16 words of 16 bits each. Serial access allows the use of a cost-effective 8-pin package, making the X2444 ideal for cost sensitive and compact design applications. Each bit of the static RAM is overlayed with a bit of nonvolatile electrically erasable PROM (E^2PROM). Data can be transferred back and forth between the two memories either by instructions sent from the processor over the serial interface, or by toggling the external $\overline{STORE}$ and $\overline{RECALL}$ inputs. Nonvolatile data is retained in the E^2PROM, while independent data can be accessed and updated in the RAM.

High voltage pulses and supplies are not required. A single 5V supply is the only power source needed, and all signals are TTL compatible.

The X2444 offers many modes of operation in order to minimize the power consumption of the chip. The chip is placed in the STANDBY mode whenever it is deselected, and is placed in the SLEEP mode whenever the sleep instruction is executed. The chip will automatically return active from STANDBY when selected by CE, and will exit the SLEEP mode when the next RECALL operation is performed, either by the RCL instruction or by taking the $\overline{RECALL}$ input low.

PIN CONFIGURATION

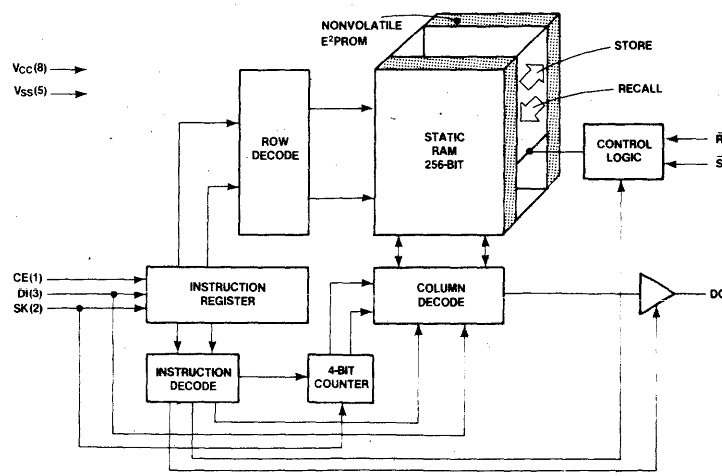
8-PIN DIP .300″



PIN NAMES

CE	CHIP ENABLE
SK	SERIAL CLOCK
DI	SERIAL DATA IN
DO	SERIAL DATA OUT
$\overline{RECALL}$	RECALL
$\overline{STORE}$	STORE
V_{CC}	+5V
V_{SS}	GROUND

FUNCTIONAL DIAGRAM X2444 (16x16)



*NOVRAM is Xicor's nonvolatile static random access memory device.
COPS™ is a trademark of National Semiconductor, Inc.

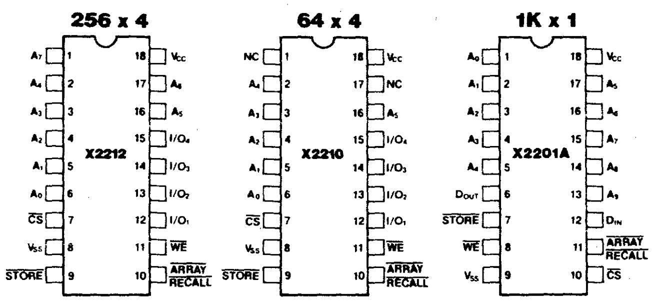
Characteristics Subject to Change Without Notice
June 1983, Stock No. 200-019

Xicor NOVRAM* Memories
Nonvolatile Static RAMS

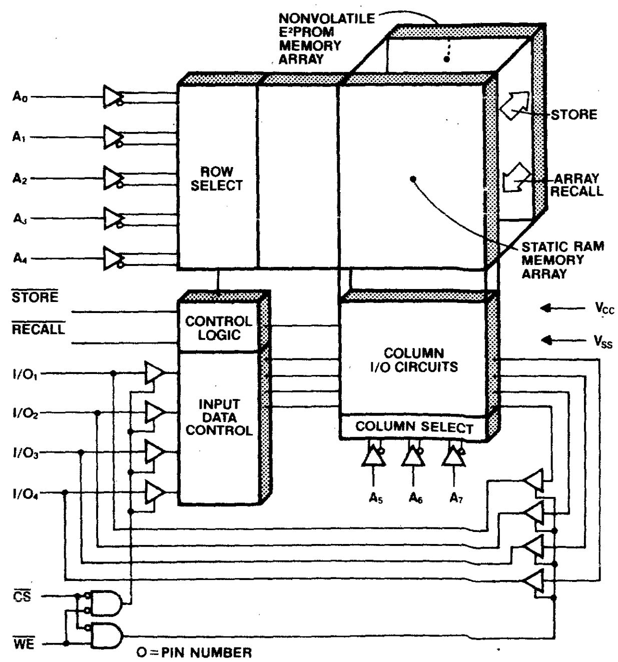
5V-Programmable	X2212	256 x 4 Bit Nonvolatile Static RAM
10% Power Supply Margin	X2210	64 x 4 Bit Nonvolatile Static RAM
V_{CC} = 5V ±10%	X2201A	1024 x 1 Bit Nonvolatile Static RAM

- **NONVOLATILE STATIC RAM:** The **X2201A, X2210,** and **X2212** are organized as conventional static RAMs overlaid bit-for-bit with a nonvolatile Electrically Erasable PROM (E^2PROM). Nonvolatile data can be stored in the E^2PROM and at the same time independent data can be accessed in the RAM memory. At any time, data can be transferred back-and-forth between the RAM and E^2PROM by simple store and array recall signals.
- **5V ONLY:** High-voltage pulses or supplies are never required. A single 5V supply is the *only power source* ever required for any function.
- **EASE-OF-USE:** Unprecedented simplicity, all inputs and outputs are directly TTL compatible. Fully static timing. Three-state output. 18-pin package.
- **PERFORMANCE:** RAM cycle time is less than 300ns. During the lifetime of the device, data can be recalled from the E^2PROM an unlimited number of times.
- **POWER-FAILURE PROTECTION:** One simple TTL signal saves the entire RAM database. A snapshot nonvolatile copy of all RAM data is internally stored safely without power and can be recalled to the RAM when power returns. No battery backup required.
- **ORGANIZED FOR MICROCOMPUTER SYSTEMS:** The common data input and output is organized four bits wide on the X2210 and X2212. The X2201A is organized conveniently by one for larger memory applications.
- **Xicor's** products are fabricated with reliable n-channel floating gate MOS technology. For systems where RAM nonvolatility or *in-the-circuit* ROM changes by TTL signals are important, the **Xicor X2201A, X2210,** or **X2212** is the ideal choice.

PIN CONFIGURATIONS



FUNCTIONAL DIAGRAM



PIN NAMES

A_0—A_9	ADDRESS INPUTS
$I/O_1 - I/O_4$	DATA INPUT/OUTPUT
$\overline{WE}$	WRITE ENABLE
$\overline{CS}$	CHIP SELECT
$\overline{ARRAY\ RECALL}$	ARRAY RECALL
$\overline{STORE}$	STORE
V_{CC}	+5V
V_{SS}	GROUND
NC	NO CONNECT

July 1983 Stock No. 200-024

*NOVRAM is Xicor's nonvolatile static RAM device

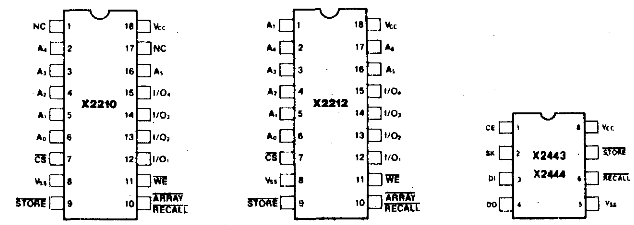
XICOR, Inc., 851 Buckeye Court, Milpitas, California 95035 (408) 946-6920 TWX 910-379-0033

XICOR ORDERING INFORMATION

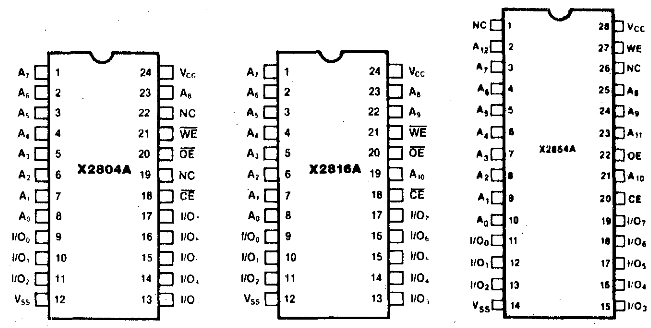
Device Type	Part #	Organization	Package	Temp. Range	Processing	Access Time
NOVRAM	X2444P	16×16*	Plastic	0° to + 70°C	Standard	N/A
	X2444PI	16×16*	Plastic	−40° to + 85°C	Standard	N/A
	X2443P	16×16*	Plastic	0° to + 70°C	Standard	N/A
	X2443PI	16×16*	Plastic	−40° to + 85°C	Standard	N/A
	X2210D	64×4	Cerdip	0° to + 70°C	Standard	300ns
	X2210DI	64×4	Cerdip	−40° to + 85°C	Standard	300ns
	X2210DM	64×4	Cerdip	−55° to + 125°C	Standard	300ns
	X2210DMB	64×4	Cerdip	−55° to + 125°C	883B	300ns
	X2212D	256×4	Cerdip	0° to + 70°C	Standard	300ns
	X2212DI	256×4	Cerdip	−40° to + 85°C	Standard	300ns
	X2212DM	256×4	Cerdip	−55° to + 125°C	Standard	300ns
	X2212DMB	256×4	Cerdip	−55° to + 125°C	883B	300ns
					* Serial Interface	
E²PROM	X2804AD	512×8	Cerdip	0° to + 70°C	Standard	300ns
	X2804AD-35	512×8	Cerdip	0° to + 70°C	Standard	350ns
	X2804AD-45	512×8	Cerdip	0° to + 70°C	Standard	450ns
	X2804ADI-35	512×8	Cerdip	−40° to + 85°C	Standard	350ns
	X2804ADI-45	512×8	Cerdip	−40° to + 85°C	Standard	450ns
	X2804ADM-35	512×8	Cerdip	−55° to + 125°C	Standard	350ns
	X2804ADM-45	512×8	Cerdip	−55° to + 125°C	Standard	450ns
	X2804ADMB-35	512×8	Cerdip	−55° to + 125°C	883B	350ns
	X2804ADMB-45	512×8	Cerdip	−55° to + 125°C	883B	450ns
	X2816AD	2K×8	Cerdip	0° to + 70°C	Standard	300ns
	X2816AD-35	2K×8	Cerdip	0° to + 70°C	Standard	350ns
	X2816AD-45	2K×8	Cerdip	0° to + 70°C	Standard	450ns
	X2816ADI-35	2K×8	Cerdip	−40° to + 85°C	Standard	350ns
	X2816ADI-45	2K×8	Cerdip	−40° to + 85°C	Standard	450ns
	X2816ADM-35	2K×8	Cerdip	−55° to + 125°C	Standard	350ns
	X2816ADM-45	2K×8	Cerdip	−55° to + 125°C	Standard	450ns
	X2816ADMB-35	2K×8	Cerdip	−55° to + 125°C	883B	350ns
	X2816ADMB-45	2K×8	Cerdip	−55° to + 125°C	883B	450ns
	X2816AE	2K×8	LCC	0° to + 70°C	Standard	300ns
	X2816AE-35	2K×8	LCC	0° to + 70°C	Standard	350ns
	X2816AE-45	2K×8	LCC	0° to + 70°C	Standard	450ns
	X2816AEI-35	2K×8	LCC	−40° to + 85°C	Standard	350ns
	X2816AEI-45	2K×8	LCC	−40° to + 85°C	Standard	450ns
	X2816AEM-35	2K×8	LCC	−55° to + 125°C	Standard	350ns
	X2816AEM-45	2K×8	LCC	−55° to + 125°C	Standard	450ns
	X2816AEMB-35	2K×8	LCC	−55° to + 125°C	883B	350ns
	X2816AEMB-45	2K×8	LCC	−55° to + 125°C	883B	450ns
	X2864AD	8K×8	Cerdip	0° to + 70°C	Standard	300ns
	X2864AD-35	8K×8	Cerdip	0° to + 70°C	Standard	350ns
	X2864AD-45	8K×8	Cerdip	0° to + 70°C	Standard	450ns

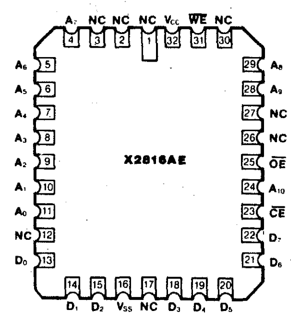
PIN CONFIGURATIONS

NOVRAM



E²PROM





PRELIMINARY DATA SHEET
Characteristics Subject to Change
Without Notice.

X2816A 2K x 8 Bit Electrically Erasable PROM
X2804A 512 x 8 Bit Electrically Erasable PROM

5 Volt Programmable E²PROMs

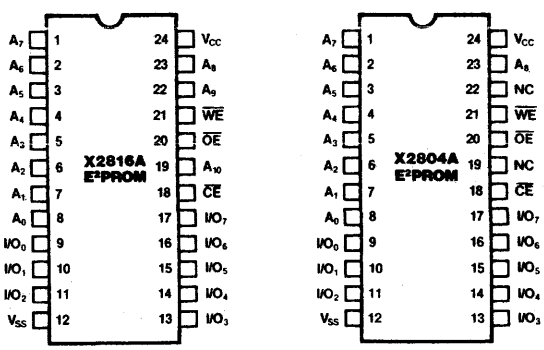
- **Simple Byte Write Operation**
  - **No High Voltages Necessary**
  - **Single TTL level $\overline{WE}$ Signal Modifies Data**
  - **Internally Latched Addresses and Data**
  - **Automatic Write Time-out**
  - **Noise Protected $\overline{WE}$ Pin**
- **Conforms to JEDEC Byte-wide Standard**
- **Reliable N-Channel Floating Gate MOS Technology**
- **Single 5-Volt Supply**
- **Byte Write Time: 10ms Max.**
- **Fast Access Time: 300ns Max.**
- **Low Power Dissipation**
  - **Active Current X2816A: 110mA Max.**
    X2804A: 80mA Max.
  - **Standby Current: 50mA Max.**

The Xicor X2816A (16,384 bits) and X2804A (4,096 bits) are electrically erasable programmable read-only memories (E²PROMs) with unprecedented ease-of-use features. Xicor E²PROM data can be modified using simple TTL level signals and a single 5-volt power supply. In addition, Xicor E²PROMs are operationally and pin compatible with existing 2K x 8 byte-programmable E²PROMs which require an additional high voltage power supply for programming. (See *optional* high voltage programming compatible mode.) Writing data in Xicor E²PROMs is analogous to writing data in a static RAM. A 200ns TTL low level signal to the $\overline{WE}$ pin initiates a byte write operation which is automatically timed out in a maximum of 10ms. Since addresses and data are internally latched, Xicor E²PROMs free the system for other tasks during the 10ms period, such as programming other Xicor E²PROMs. In addition to byte modification capability, a 10ms total chip erase feature is provided.

Xicor E²PROMs use a 2-line control architecture, $\overline{CE}$ and $\overline{OE}$, to eliminate bus contention in a system environment. A power down mode is featured. In the standby mode, power consumption is reduced by 55% without increasing access time. The standby mode is achieved by applying a $\overline{CE}$ high signal.

The X2816A and X2804A are fabricated with the same reliable n-channel floating gate MOS technology used in Xicor's popular 5-Volt programmable NOVRAM memories.

PIN CONFIGURATIONS 24 PIN DIP.600"



PIN NAMES

A_0-A_{10}	ADDRESS INPUTS
I/O_0-I/O_7	DATA INPUTS/OUTPUTS
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
V_{CC}	+5V
V_{SS}	GROUND
NC	NO CONNECT

MODE SELECTION

Standard Xicor 5V-Programmable Mode

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O	POWER
H	X	X	Standby	High Z	Standby
L	L	H	Read	D_{OUT}	Active
L	H	L	Byte Write	D_{IN}	Active
L	H	H	Read and Write Inhibit	High Z	Active

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Preliminary Information Sheet
May 1983, Stock No. 200-012

XICOR, Inc., 851 Buckeye Court, Milpitas, California 95035 (408) 946-6920 TWX 910-379-0033

ADVANCED INFORMATION

64K X2864A 8K x 8 Bit Electrically Erasable PROM

5 Volt E^2PROM

FEATURES

- **Simple Byte and Page Write**
  - — Single TTL Level $\overline{WE}$ Signal
  - — Latched Address and Data
  - — Automatic Internal Erase
  - — Automatic Write Timing
  - — Automatic Page Write
  - — $\overline{DATA}$ Polling Verification
  - — Optional Chip Erase
- **Enhanced Write Protection**
- **Single 5 Volt Supply**
- **Byte or Page Write: 5 ms Typical**
  - — Effective 300 μsec/Byte Write
  - — Chip Rewrite—2.6 sec
- **Fast Access Time: 350 ns**
- **Power: 110 mA—Active Current**
  50 mA—Standby Current
- **JEDEC Approved Byte-Wide Pinout**

DESCRIPTION

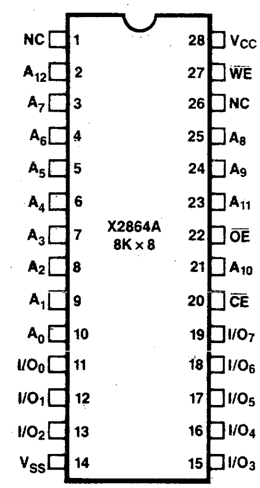
The Xicor X2864A is an electrically erasable programmable read-only-memory (E^2PROM) with unprecedented ease-of-use features. Xicor E^2PROMs can be modified using simple TTL level signals and a single 5 volt power supply. In addition, the X2864A is operationally and pin compatible with existing 8K x 8 EPROMs which require high voltage programming and ultraviolet exposure erasing. Writing data in Xicor E^2PROMs is analogous to writing data in a static RAM. A 200 ns TTL low level signal to the $\overline{WE}$ pin initiates a byte write operation which is automatically timed out in 5 ms. Since addresses and data are internally latched, Xicor E^2PROMs free the system for other tasks during the 5 ms period, such as programming other Xicor E^2PROMs.

A 16-Byte Page Write allows data to be written at an effective rate of 300 μsec/byte or 2.6 seconds to rewrite the entire chip. An optional chip erase feature is also included.

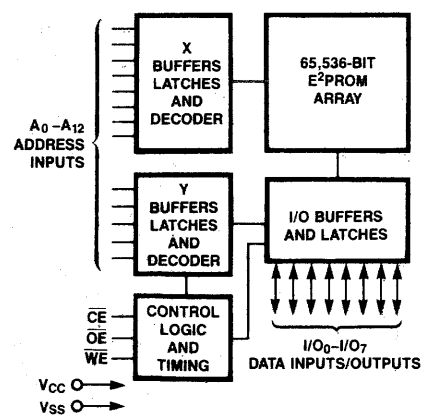
The X2864A also features $\overline{DATA}$ Polling, which enables the E^2PROM to signal the processor that a write operation is complete without requiring the use of any external hardware.

The X2864A is fabricated with the same reliable N-Channel floating gate MOS technology used in the popular 5 volt programmable Xicor NOVRAMs.

PIN CONFIGURATION



FUNCTIONAL DIAGRAM



MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—
L	V_{OE}	L	Chip Erase	D_{IN} = H	Active

Xicor

MEMORY

Characteristics subject to change without notice.

Last Page This Section. Next Page 4349

INTRODUCTION TO PROM PROGRAMMERS

This section describes instruments used to enter assembly language code into programmable devices such as PROMs, EPROMs, EEPROMs, EAROMs, PALs, PLAs and MPUs. Equipment listed includes programmers designed for system development, production and field-service applications. Manufacturers are sequenced alphabetically, and each system is characterized by pertinent selection factors. These parameters include programmed device types, type of display, personality modules, edit functions, programming checks, self-test features and types of interface ports.

Some manufacturers assign different model numbers to units having capabilities beyond those listed for the model designated at the top of the Master Selection Guide. In these cases the units are covered under "Comments".

Detailed Product Information provided by:

The manufacturers listed above have provided detailed information on their latest and most significant products.

PROM PROGRAMMERS

Application	Capabilities	Programmed Devices	Display	Maximum PROM Array (bits)	Personality Modules	Maximum Gang Capacity (Sockets)	Edit Functions
Development	Program, copy, compare, read	EPROM	CRT, LED	16Kx8	Not Required		Insert, delete
Production	Copy	EPROM, EEPROM	LED	32Kx8	Software based	16	
Development, production, field service	Program, copy, compare, read, erase	EPROM	LED	32Kx8	Not required, software-based	1	Insert, move, delete, nibble swap, memory map
Production	Program, copy, compare	Bipolar PROM	Lamps	4Kx8	Dedicated	1	
Development, field service, Production	Program, copy, compare, read, erase	NMOS, CMOS, MPU, EEPROM, EPROM	7-Segment LED(4)	23Kx8 expandable	Software programmable	1	Via Host System
Development, field service	Program, read	Bipolar PROM	Lamps, digit switch	4Kx8	Dedicated		
Development, production, field service	Program, copy, compare, read, test	FPLA: Signetics 82S100, 82S101, 82S106, 82S107	LED		Dedicated		Insert, delete
Development, field service, production	Program, copy, compare, read	Bipolar PROM (8 x 32)	LED	32x8			Insert, delete
Development	Program, copy, compare, read, test	Seeq 72720 (T.I. 7000 with EEPROM)	User terminal	up to 8Kx8		1	Line editing or any word processor on host computer
Development	Program, copy, compare, read, test, erase	EPROM, EEPROM	CRT	32Kx8	Dedicated		
Development, Incoming Test	Program, copy, compare, read, test	8748, 8749	User terminal	1Kx8 8748, 2Kx8 8749		1	Line editing or any word processor on host computer
Development, incoming test	Program, copy, compare, read, test	8751, 8752	User terminal	2Kx8 8751, 4Kx8 8752		1	Line editing or any word processor on host computer
Development	Program, copy, compare, read	EPROM, EEPROM, MPU	LED	8Kx8	Dedicated (Universal NMOS and Intel single-chip microcomputers)	1	Insert, delete, write, fill
Development, field service	Program, copy (load), compare (verify), read, test, erase	Bipolar (fuse-link and vertical-fuse) PROM, CMOS, PROM, EPROM, EEPROM, EAROM, MPU	16-character fluorescent	256Kx8	24-pin skinny-wide and 40-pin MPU socket adapters; no modules required	1	Insert, move, delete, nibble swap, memory map, split, shuffle, clear, complement, fill RAM
Development, field service	Program, copy (load), compare (verify), read, test, erase	CMOS, PROM, EPROM, EEPROM, EAROM, MPU	16-character fluorescent	256Kx8		1	Insert, move, delete, nibble swap, memory map, split, shuffle, clear, complement, fill RAM

PROM PROGRAMMERS

Programming Checks	Self-Test	Prompting	Buffer Memory	I/O Interface	Comments	Model	Source
Blank, verify		Audible		RS232 Serial, selectable baud rate	Operates with Z80/8080 CP/M. Utility software supplied to partition long object or HEX files into required EPROM length and split 16-bit files into upper/lower 8-bit files.	UP8	Advent
Blank, checksum, illegal bit, verify	Keyboard, display, switches	Visual/ audible				CopyROM3716	Citel
Blank, checksum, illegal bit, verify	Keyboard, display, switches, buffer, memory	Visual/ audible	8Kx8 expandable	Parallel TTL, RS232 serial		System37	Citel
Illegal bit, Vcc sensitivity		Visual				PD2000S	Curtis
Blank, checksum, illegal bit, verify, on current	Status of programming levels	Visual/ audible	64	RS232 serial selectable Baud rates 110-9600	Programs 4K 3-supply through 25gK 1-5 supply and beyond. Stand-alone duplicator or complete remote control by host computer.	PD5000E	Curtis
Vcc sensitivity		Visual				PM3000S	Curtis
Verify		Visual				PR-100A	Curtis
Blank, checksum, illegal bit, verify	Diagnostic & calibration	Visual/ Audible	32 bytes	RS5332 110-9600 Baud	Handles Signetics, TI, NSC, Harris, AMD, MMI, Intersil.	PR5200B	Curtis
Checksum verify bytes		Visual	User system	300, 1200, 2400 baud RS 232 link to host computer	IBM PC cross assemblers with downloader available. Programmer board connects to any RS-232 port and utilizes user computer terminal and power supply.	CYP-7000	Cybernetic
Blank, checksum, verify		Visual/ Audible	16Kx8	RS232 Serial, Selectable Baud Rate		CYP275	Cybernetic
Checksum verify bytes		Visual	User system	300, 1200, 2400 baud RS 232 link to host computer	IBM PC cross assemblers with downloader available. Programmer board connects to any RS-232 port and utilizes user computer terminal and power supply.	CYP8048/9	Cybernetic
Checksum verify bytes		Visual	User system	300, 1200, 2400 baud RS 232 link to host computer	IBM PC cross assemblers with downloader available. Programmer board connects to any RS-232 port and utilizes user computer terminal and power supply.	CYP8051	Cybernetic
Blank, checksum, illegal bit, verify	Keyboard, display, switches, buffer memory, automatic power-up, program ROM, status of programming electronics	Visual	2kx8	RS232 serial, selectable baud rate (110-9600 baud)		20B Universal NMOS Memory Programmer	Data I/O
Blank, checksum, illegal bit, verify, overcurrent check, backward device, 2-pass verify with variable	Keyboard, display, switches, buffer memory, automatic power-up, program ROM, status readout of programming electronics	Visual	32Kx8	RS232 serial, current loop, selectable baud rate (50-19,200)	Portable programming system; includes UV erasing lamp and removable lid for storing accessory.	22A Personal Programmer	Data I/O
Blank, checksum, illegal bit, verify, overcurrent check, backward device, 2-pass verify with variable Vcc	Keyboard, display, switches, buffer memory, automatic power-up, program ROM, status of programming electronics	Visual	32Kx8	RS232 serial, current loop, selectable baud rate (50-19,200)	Portable MOS-only programming system; includes UV erasing lamp and removable lid for accessory storage.	22B Personal Programmer	Data I/O

Bold face indicates additional data is provided on the page noted.

PROM PROGRAMMERS

Application	Capabilities	Programmed Devices	Display	Maximum PROM Array (bits)	Personality Modules	Maximum Gang Capacity (Sockets)	Edit Functions
Development, field service	Program, copy (load), compare (verify), read, test	Bipolar PROM, CMOS, PROM, EPROM, EEPROM, EAROM, PAL, PLA, MPU, FPGA, FPLA, FPRP, FPLS, prog. I/O port, PMUX	16-character fluorescent	256Kx8 (UniPak2)	Software selectable Paks (UniPAK 2, MOSPak, LogicPak, Gang Pak, Handler UniPak)	8	Insert, move (block), delete, nibble swap, memory map, split, shuffle, clear, complement, fill RAM
Production	Program, copy (load), compare (verify), read, test, EEPROM cycling test, electronic device identification	MOS and CMOS PROM, EPROM, EEPROM, intelligent algorithms for EPROMs	16 character fluorescent	16Kx8, expandable	Software selectable	20	Complement RAM, fill RAM, 16-bit mode
Development, production	Program, Set program, copy (load), compare (verify), read, test, EEPROM cycling test, electronic device identification	MOS and CMOS, EPROM, EEPROM, intelligent algorithms for EPROMs	16 character fluorescent	16Kx8	Software selectable	20	Insert, delete, I/O offset, begin RAM, fill RAM, complement RAM, 16-bit mode
Development, production, field service	Program, copy, compare, read, test, stimulate	CMOS, PROM, EPROM, EEPROM	LED Hexadecimal	32Kx8	Dedicated, generic		Insert, move, search, split/shuffle, memory map
Production, field service	Program, copy, compare, read, test	CMOS, PROM, EPROM	LED	4Kx8	Gang, generic gang	16	
Production, field service	Program, copy, compare, read, test, erase	CMOS, PROM, EPROM, EEPROM	LED	16Kx8	Gang, generic gang	10	
Development, production, field service	Program, copy, compare, read, test, erase	Bipolar PROM, CMOS, PROM, EPROM, EEPROM, EAROM, IFL, PAL, PLA, MPU	CRT	63Kx8	Generic		Insert, move, delete, nibble swap, memory map, complement, byte, split, shuffle, search
Development, production	Program, copy, compare, read, test, erase	Bipolar PROM, CMOS, PROM, EPROM, EAROM, PAL, PMUX, MPU	LED, hexadecimal	50Kx8 (add field 64Kx8BMS)	Dedicated, generic		Move, nibble swap, memory map, complement
Development, production, field service	Program, copy, compare, read	Bipolar PROM, EPROM, MPU	LED	16Kx8	Dedicated, generic, gang	8	Insert, delete, nibble swap
Development, field service	Program, copy, compare, read, test, erase	CMOS, PROM, EPROM, EEPROM, EAROM	LED	32Kx8	Dedicated		Insert, move, delete, memory map
Development, field service	Program, copy, compare, read, test, erase, modify	Bipolar PROM, CMOS, PROM EEPROM			Not required		Move, compare, replace
Development, field service	Program, copy, compare, read, test, erase	Bipolar PROM, CMOS PROM, EPROM, EEPROM, EAROM, PAL	LED	32Kx8	Generic & software programmable		Insert, move, delete, nibble swap, memory map, search

PROM PROGRAMMERS

Programming Checks	Self-Test	Prompting	Buffer Memory	I/O Interface	Comments	Model	Source	Line
Blank, checksum, illegal bit, verify, overcurrent, backward device, 2-pass verify with variable Vcc	Keyboard, display, switches, buffer memory, automatic power-up, program ROM, status of programming electronics	Visual/ audible	16Kx8 (standard), 64Kx8, (optional)	RS232 serial, current loop, selectable baud rate (50-19,200 baud)	Edit in hexadecimal, octal or binary. English-language prompts, menus and error messages. Remote control and 26 development-system format translators are standard.	29A Universal Programmer	Data I/0	1
Blank, checksum, illegal bit, verify, overcurrent, backward device, mislocated device	Keyboard, display, switches, buffer memory, automatic power-up, program ROM, status of programming electronics	Visual/ audible	32Kx8	RS232 serial, selectable baud rate (110-9600 baud)	Remote control and 26 data translation formats are standard. M120A controls 200A Data Contriol Unit for program storage.	M120A Gang Programmer	Data I/0	
Blank, checksum, illegal bit, verify, overcurrent, backward device, miclocated device, variable Vcc on verification	Keyboard, display, switches, buffer memory, automatic power-up, program ROM, status of programming electronics	Visual/ audible	128Kx8, 256Kx8	RS232 serial (2), selectable baud rate (110-9600 baud)	Can segment programs and load each segment into different PROMs simultaneously. Remote control and 26 data translation formats are standard. M121A controls 200A Data Control Unit for program.	M121A Gang Programmer	Data I/0	
Blank, illegal bit, checksum, verify	Automatic with power-up	Visual/ audible	8Kx8 expanded to 32Kx8 data retention with power off	RS232 serial port, selectable baud rate to 19.2K	Interfacing formats: Intel Hex; Motorola exorciser; ACSII-Hex Space; ACSII-BNPF & manual format. EPROM/EEPROM simulation capability	EP-804	Digelec	
Blank, verify		Visual/ audible	4Kx8	RS232 serial, current loop, selectable baud rate	Can program two different patterns simultaneously.	GP-16 Gang Programmer	Digelec	5
Blank, checksum, illegal bit, verify, parametric test	Device Selection vs Pin Out	Visual/ audible				GP-810 Gang Programmer	Digelec	
Blank, checksum, illegal bit, verify, continuity, parametric check	Buffer memory, program voltages	Visual/ audible	64Kx8, espandable to 512Kx8 battery backup	Parallel TTL, RS232 serial, current loop, selectable baud rate	No calibration required. Software/Menu driven machine.	UP-803	Digelec	
Blank, verify, continuity, window check		Visual/ audible	4Kx8, 8Kx8, expandable, battery backup	Parallel TTL, RS232 serial, current loop, selectable baud rate	12 interfacing formats; 4 data entry keyboard formats	UPP-801	Digelec	
Blank, checksum, illegal bit, verify	Display, buffer memory	Visual/ audible	16Kx8	RS232 serial, current loop, selectable baud rate, 110 to 9600 baud	Unit is equipped with three fast programmable power supplies (100ns/V) for programming voltages	RP400-S	Elind	
Blank, checksum, illegal bit, verify	Buffer memory	Visual/ audible	64Kx8	RS232 seial, +TTL serial	The RP600 is a dedicated EPROM Programmer, the selection is made by software. The unit is particularly suited for field service. The unit can program all EPROMs available at the moment.	RP600	Elind	10
Verify						H3000	Hughes	
Blank, checksum, illegal bit, verify	Keyboard, display, buffer memory module	Visual	32Kx8	RS232 serial, current loop, selectable baud rate	PROM Emulation Module option allows user to test and debug programs before committing to PROMs.	IM1010 Universal Programmer	IMS	

Bold face indicates additional data is provided on the page noted.

PROM PROGRAMMERS

Application	Capabilities	Programmed Devices	Display	Maximum PROM Array (bits)	Personality Modules	Maximum Gang Capacity (Sockets)	Edit Functions
Production, development	Program, copy, compare, read, test, erase	EPROM, EEROM, CMOS, EPROM	LED	16Kx8, 32Kx8	Software programmable	16	Move, delete, memory map, I/O offset, fill RAM
Development, production	Program, copy, compare, read, erase (E2 only)	Bipolar PROM, EPROM, EEPROM, MPU	LED	32Kx8bits	Generic, gang, generic gang	8	Move*, nibble swap* n byte swap*, memory map*, enter
Development, production	Program, copy, compare, read, test, erase	Bipolar PROM, CMOS PROM, EPROM, EEPROM, EAROM, PAL, PLA, MPU, EPLA, FDRP, EPGA, FPLS, PMUX	Fluorescent	32Kx8	Dedicated, generic, gang, generic gang	8	Set, insert, move, delete, nibble swap, memory map, fill, invert, 16-bit split/shuffle, logical AND/OR/XOR, string search
Development, production, field service	Program, copy, compare, read, test, erase	Bipolar PROM, CMOS PROM, EPROM, EEPROM, EAROM, PAL, PLA, FPLA, FPRP, FPGA, FPLS, PMUX	LED	32Kx8	Dedicated, generic, gang, generic gang	8	Insert, move, delete, nibble swap, memory map, fill, invert
Development, production, field service	Program, copy, compare, read, test, erase	Bipolar PROM, CMOS PROM, EPROM, EEPROM, EAROM, PAL, PLA, MPU, FPLA, FPLS, PMUX	LED	32Kx8	Dedicated, generic, gang, generic gang	8	Set, insert, move, delete, nibble swap, memory map, fill, invert
Development, production, field service	Program, copy, verify, read, test, erase, help, odd/even	Bipolar PROM, CMOS PROM, EPROM, EEPROM, EAROM, PLA	CRT via terminal	8Kx8	Dedicated	1	Insert, move, delete, save, memory map, change
Development, production, field service	Program, copy, compare, read, test, erase	Bipolar PROM, CMOS PROM, EPROM, EEPROM, EAROM, PAL, PLA, MPU, All programmable devices	CRT Interfaces with Remote printer		None—(completely software based)!!	1	Insert, move, delete, nibble swap, memory map, on screen cursor-controlled editing
Production	Program, copy, compare, read, test	EPROM	LED	32Kx8	Generic gang	16 (32 with satellite)	None allowed
Production	Program, copy, compare, read, test, erase, dc parameters	EPROM, EEPROM, EAROM	LED, ASCII	256Kx8	Generic gang	18 (36 with satellite)	None allowed
Production	Program, copy, compare, read, test, erase, dc parameters	EPROM, EEPROM, EAROM	LED, ASCII	256Kx8	Generic gang	20 (40 with satellite)	None allowed
Development, production	Program, copy, compare, read	EPROM	LED	2764	Dedicated	1	Insert, move
Development, production, field service	Copy, compare	Bipolar PROM, CMOS PROM, EPROM, EEPROM, PLA	LED	64Kx8	Dedicated, generic, gang, generic gang	8	Insert, move, delete, nibble swap, memory map
Development, production, field service	Program, copy, compare, read	Bipolar PROM, CMOS PROM, EPROM, EEPROM	LED	64Kx16	Dedicated, generic, gang, generic gang	8	Insert, move, delete, nibble swap, memory map

PROM PROGRAMMERS

Programming Checks	Self-Test	Prompting	Buffer Memory	I/O Interface	Comments	Model	Source	Line
Blank, checksum, illegal bit, verify, misaligned or upside-down device, broken or bent pin, overcurrent	Keyboard, display, switches, buffer memory, automatic power reset, calibration, programming electronics	Visual/ audible	64Kx9 standard; 128Kx9, 256Kx9 and 512Kx9	RS232 serial, selectable baud rate	Simultaneous set programming ability, electrically isolated programming sockets. Computer control software automates EPROM programming, intelligent Fast algorithms supported.	IM3016 Multi-Master Programmer	IMS	1
Blank, checksum, illegal bit, verify, reverse socket detection	Buffer memory, motherboard, power supply, module	Visual/ audible*	16Kx8, expandable to 32K; virtual buffer*	RS232 serial, automatic baud rate selection	*iUPS software package feature. Host software driver also provides file manipulation, file mapping, held file, screen editing, data manipulation and other features.	UP-200/201	Intel	
Blank, checksum, illegal bit, verify at high and low Vcc limits	Keyboard, display, switches, buffer, firmware integrity	Visual/ audible	8Kx8, expandable to 32Kx8	Parallel TTL, RS232 serial, current loop, selectable baud rate (50 to 38400 baud), IEEE-488	Build-in uv EPROM eraser with keyboard programmable timer. Remote controllable via RA232 and IEEE-488 ports. Error-tolerant communications protocol for long distance telephone transfers. Compatible with MPP-80S modules.	EPP-80	Kontron	
Blank, checksum, illegal bit, verify at high and low Vcc limits	Keyboard, display switches, buffer memory	Visual/ audible	4Kx8, 8Kx8, 16Kx8, 32Kx8 plus mass storage	RS232 serial, selectable baud rate	Build-in uv source, IC handler interface. MPP 80SAM has acoustic coupler and modem.	MPP-80	Kontron	
Blank, checksum, illegal bit, verify at high and low Vcc limits	Keyboard, display switches, buffer memory, firmware integrity	Visual/ audible	8Kx8, expandable to 32Kx8	RS232 serial, current loop, selectable baud rate (50 to 38400 baud)	Build-in uv EPROM eraser. IC handler interface. Remote controllable via RS232 port from terminal or host computer. MPP-80SAM has build-in acoustic coupler, modem and error-tolerant communications protocol.	MPP80S	Kontron	5
Blank, illegal bit, verify		Visual/ audible	8Kx8, expandable	Proprietary		MG8PPS	Motorola	
Blank, checksum, illegal bit, verify, matrix test	Keyboard, buffer memory, leakage test on socket	Visual/ audible menu-driven	64Kx8 Std, expandable to 256Kx8	Dual RS-232	Five versions available, depending on programming capabilities needed. Fully expanded, Datatap uses 40 separate high-voltage drivers with a library of over 1000 programmable devices, programmed from one universal socket!!	Datatap®	Oliver	
Blank, illegal bit, verify, matrix test*	Keyboard, switches, leakage test on socket matrix	Visual/ audible			*Matrix test checks both data and address lines for ESD (electrostatic discharge) damage. Data lines are checked for min. sink and source current capability during both blank and verify tests. 100-240 Vac operation.	UPP-2700	Oliver	
Blank, checksum, illegal bit, verify, Vcc level tests, matrix test	Keyboard, switches, leakage test on socket matrix	Visual/ audible, including voice option	2 ports for label printer and voice enunciator	UL-Listed, short circuit protection, power-fail restart capability		**UPP-28000-ZIF**	**Oliver (4401)**	
Blank, checksum, illegal bit, verify, Vcc level tests, matrix test	Keyboard, switches, leakage test on socket matrix	Visual/ audible, including voice option		2 ports for label printer and voice enunciator		**UPP-28000 Scoop**	**Oliver (4401)**	10
Blank, illegal bit, verify		Visual	None	RS232 serial, selectable baud rate		Gangbuster	Onset	
Blank, verify, at high and low Vcc limits, checksum	Keyboard, display, switches, buffer memory	Visual/ audible	8Kx8, 16Kx8, expandable, battery backup CMOS	Parallel TTL, RS232 serial, selectable baud rate	Two year warranty. Separate master and copy sockets on personality modules (can duplicate directly from master to copy socket). Fixed Vpp power supplies do not require adjustment.	M910AControl Unit	Pro-Log	
Blank, checksum, illegal bit, verify at high and low Vcc limits	Keyboard, display, switches, buffer memory	Visual/ audible	8Kx8, 16Kx8, expandable, battery backup CMOS	Parallel TTL, RS232 serial, selectable baud rate	Two year warranty. Separate master and copy sockets on personality modules (can duplicate directly from master to copy socket). Fixed Vpp power supplies do not require adjustment.	M980Control Unit	Pro-Log	

Bold face indicates additional data is provided on the page noted.

PROM PROGRAMMERS

Master Selection Guide

PROM PROGRAMMERS

Application	Capabilities	Programmed Devices	Display	Maximum PROM Array (bits)	Personality Modules	Maximum Gang Capacity (Sockets)	Edit Functions
Development, production, field service	Program, copy, compare, read, test, erase	Bipolar PROM, CMOS PROM, EPROM, EEPROM, PAL, MPU	LED	64Kx16	Dedicated, generic, gang, generic gang	8	Insert, move, delete, nibble swap, memory map, split/interweave (4 and 8 bit), invert
Development, production, field service	Program, copy, compare, read, test	PAL	KED	2K	Dedicated	1	Insert, move, delete, memory map
Development, production	Program, copy, compare, read, test	PAL					Insert, delete, memory map
Production	Program, copy, compare, read, test for device programmability, erase EEPROM, device software	Bipolar PROM, CMOS PROM, EPROM, EEPROM, PAL, FLPA, MPU	14 character alphanumeric LED	256K bits	Slave for FPLA, PAL AIM devices and gang EPROM programming	24 using 2 gang slaves	Peek, poke, move, insert, clear DATA RAM to state, odd/even byte separate/swap, list, find, checksum and selected range programming
Production	Gang program, copy, compare, read, test for device programmibility, EPROMS, EEPROMS and MPU's and erase EEPROMS. Devices software selected.	CMOS PROM, EPROM, EEPROM, MPU, PAL, FPLA	14 character alphanumeric LED	256K bits	Slave for FPLA, PAL AIM devices and gang EPROM programming	36 using 2 gang slaves	Peek, poke, move, insert, clear DATA RAM to state, odd/even byte separate/swap, list, find, checksum and selected range programming
Production	Gang program, copy, compare, read, test for device programmability.	8748, 8748H, 8749H, 8741, 8755A, 8751	LED	256K bits	Slave for FPLA, PAL AIM devices and gang EPROM programming	24 using 2 gang slaves	Peek, poke, move, insert, clear DATA RAM to state, odd/even byte separate/swap, list, find, checksum and selected range programming
Development, field service	Program, copy, compare, read, test, erase EEPROM and simulate. Devices software selected	EPROM, EEPROM, Intel and Motorola MPU's	8-character LED	128K bits			Peek, poke, move, clear DATA RAM to state, odd/even byte separate/swap list, checksum and selected range programming
Development, production	Read, program, load from disk, verify, verify Blk, store to disk, program chip set	EPROM, bipolar PROM, CMOS, MPU, EEPROM, EAROM, PAL, PLA, FPGA, FPLA, FPLS, PMUX, FPRP, prog I/O port	80 characters x 24 line CRT	64Kx8		9 (40 pin)	Change, move, fill, complement, word order/-size, memory map
Development, field engineering	Read, program, load from disk, verify, verify Blk, store to disk, erase	EPROM, bipolar PROM, CMOS, MPU, EEPROM, EAROM, PAL, PLA, FPGA, FPLA, FPLS, PMUX, FPRP, prog I/O port	80 characters x 24 line CRT	64Kx8		1	Change, move, fill, complement, word order/-size, memory map

PROM PROGRAMMERS

Programming Checks	Self-Test	Prompting	Buffer Memory	I/O Interface	Comments	Model	Source		Line
Blank, checksum, illegal bit, verify, backward PROM, shorted address line, overload (Vcc and Vpp)	Keyboard, diaplsy, switches, buffer memory, programmable algorithms	Visual/ audible	8Kx8, 16Kx8, expandable, battery backup, CMOS	Parallel TTL, RS232 serial, selectable baud rate, TTY		System90	Pro-Log		1
Blank, verify, function test, continuity	Display, switches, buffer memory	Visual	2Kx8	RS232 serial, selectable baud rate	PALs are designed simulated programmed and functionally tested on the PAL BURNER. PAL design specifications may be down loaded from another computer or stored in the on-board storage media. Programs all MMI, AMD, TI, and NATIONAL 20 and 24 pin PALs	**SD1000**	**StrucDes**	**(4402)**	
Illegal bit, verify			2Kx8	RS232 Serial, selectable baud rate		SIMPALINK	StrucDes		
Blank, programmability checksum, illegal bit, verify	Keyboard, display, switches, DATA RAM, automatic voltage and timing recalibration before and during programming	English word, audible	16Kx8 expandable to 64Kx8	Dual independent RS232 serial ports selectable formats parity, baud rates 110-19.2K, terminal and computer control	Z-2000 has same features as Z-1000 except memory is 64Kx8 and has interfaces for 8 inch dual disc drives and IEEE488.	**Z1000/Z2000**	**Sunrise**	**(4403)**	
Blank, programmability checksum, illegal bit, verify	Keyboard, display, switches, DATA RAM, automatic voltage and timing recalibration before and during programming	English word, audible	16Kx8 expandable to 64Kx8	Dual independent RS232 serial ports selectable formats parity, baud rates 110-19.2K, terminal and computer control	Z-2400 has same features as Z-1200 except memory is 64Kx9 and has 8 inch dual disc drives and IEEE-488 included.	**Z1200&Z2400 Gang Programmers**	**Sunrise**	**(4403)**	5
Blank, programmability checksum, illegal bit, verify	Keyboard, display, switches, DATA RAM, automatic voltage and timing recalibration before and during programming	English word, audible	16Kx8 expandable to 64Kx8	Dual independent RS232 serial ports selectable formats parity, baud rates 110-19.2K, terminal and computer control, 8-bit parallel port	Z-2448 has same features as Z-1248 except memory is 64Kx8 and it has 8-inch dual disc drives and IEEE-488 included.	**Z1248**	**Sunrise**	**(4403)**	
Blank, checksum, illegal bit, verify	Keyboard, DATA RAM, simulator, programming sockets, display	Visual/ audio	8Kx8 expandable to 16Kx8 battery operated	RS232 serial, selectable formats, parity, baud rates 110-19.2K, terminal and computer control with selectable communications	PROM data display simultaneous with RAM data. ZAP48 has same features as plus programming of Intel's 8748, 8749, 850, 8741, 8755A and 8751MPU's. ZAP68 has same features as ZAP80 plus programming of Motorola's 68701 and 68705 MPU's.	**ZAP80/ZAP48/ ZAP68**	**Sunrise**	**(4403)**	
Verify blank, verify programmable block check, verify overcurrent, backward, wrong chip type, threshold voltage margins, mislocated device	Registers, memory, drivers, power usage, auto-calibration to .1% on current and voltage	Visual LED's, visual CRT	Virtual paged to disk—no limit	RS232 serial, selectable baud rate (110-9600) Parallel printer port	New chips are supported through software distribution on diskette. Statistics gathering gives printout of programming activity and yield. Automatic labeling support standard. Single button repeat programming.	PG1140-X	Varix		
Verify blank, verify programmable block check, verify overcurrent, backward, wrong chip type, threshold voltage margins, mislocated device	Registers, memory, drivers, power usage, auto-calibration to .1% on current and voltage	Visual LED's, visual CRT	Virtual paged to disk—no limit	RS232 serial, selectable baud rate (110-9600) Parallel printer port	New chips are supported through software distribution on diskette. Customer may write software to program or test his own proprietary chips.	SP0300-X	Varix		

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Last Page This Section. Next Page 4401

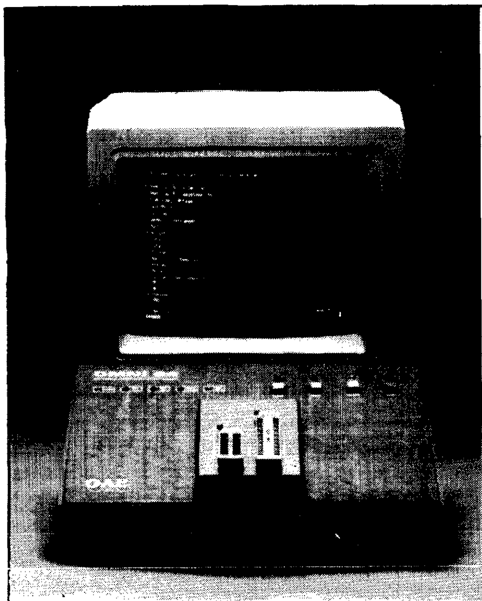
Don't miss the Sections on Semicustom ICs

Digital Gate Arrays, Standard Cells, and Linear Arrays Are All Covered

Vol. II, page 4425

Oliver Advanced Engineering, Inc.

NEW



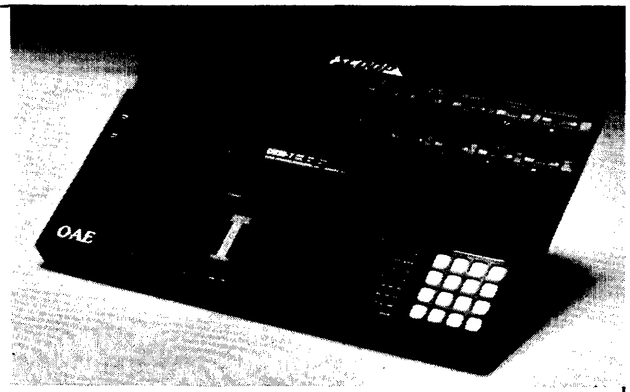
OMNI 64™
SOFTWARE CONFIGURED PROGRAMMER

- Practically every programmable device in production can be programmed on two universal sockets, including EPROMs, EEPROMs, bipolar PROMs, single chip microprocessors, PALs, FPLAs, FPLSs, FPGAs, and even diode arrays.
- No more personality modules, HEX keypads or cryptic one-line displays. The OMNI 64 has replaced them with programmable pin drivers, a large firmware data base and a cursor controlled full screen display format.
- Any 24×80 CRT with clear screen and addressable cursor will provide over 50 pre-formatted user interactive screens.
- 65,536 bytes of DATA RAM standard, 262,144 bytes optional.
- The OMNI 64 comes in five upgradable levels. No need to pay for programming hardware that you are not going to use.
- ATE version available. Combines DC and AC parametric testing with the extensive OMNI 64 programming data base.

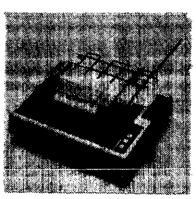
Patents pending.

Specifications are subject to change without notice.

NEW MODEL 28000 SCOOP
EPROM & E²PROM TESTER-DUPLICATOR



- OAE's exclusive SCOOP design allows all PROMs to be scooped from their sockets and into a tube in one operation!
- 20 Sockets for high throughput and lower labor costs.
- Full alpha-numeric display produces easy to understand operator prompts.
- TESTS and PROGRAMS both 24 & 28 pin NMOS, HMOS, and CMOS 5v single supply EPROMs and E²PROMs.
- Fourteen new tests check for shorts, opens, excessive leakage, and static damage on both data and address lines.



- Two stage Matrix Test™ locates defective or incorrectly inserted devices in Stage I. Static damaged or tri-stated parts are detected in Stage II.
- Sink and source current tests are performed every time a device is read.
- Label Printer produces professional custom labels for each device. Diagnostic error labels are automatically printed for marginal or defective EPROMs.
- 18 Zero Insertion Force Socket version also available.

For more information call the OAE HOTLINE (213) 240-0080

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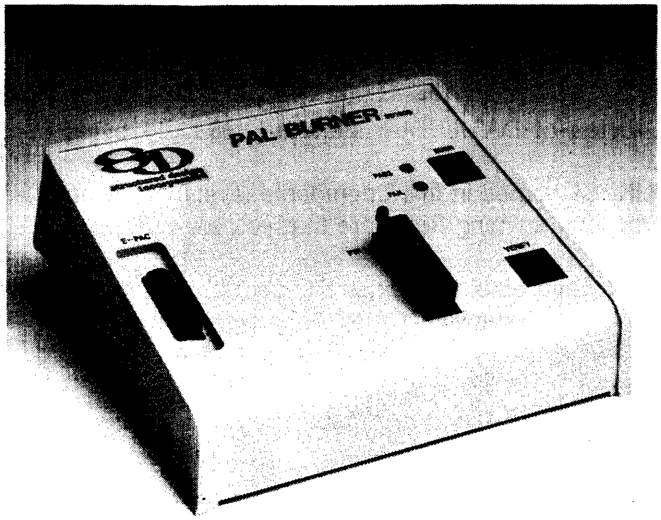
3B}IC/MST.AD 10/83

SIMPLIFIED METHODOLOGY

Structured Design Provides the Complete PAL® Development System

PAL BURNER

At Structured Design we believe in methods — *complete step-by-step methods* that free your creativity to design hardware that's practical, marketable and tested.



Simplify, Simplify, Simplify

Like all methods that work, ours includes all you need to do your job. The SD1000 PAL Burner is the most complete programmer available today, working without costly add-on equipment or awkward switching of modules.

New PAL Burner Offers Cost-Effective Design Power

PAL Burner combines power with simplicity. It's simple enough that your non-technical staff can easily use it; yet, it's powerful enough to capture and store complex designs. Since PAL Burner includes a structured, menu-driven, user-friendly PAL assembler that prompts you through each step, you virtually eliminate syntax errors saving many design hours and dollars.

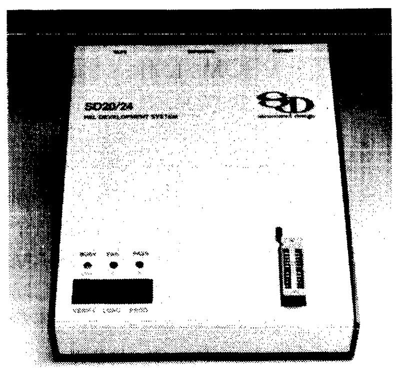
Compatible. Reliable. Easy-to-Use.

PAL Burner offers other benefits: programs all current PALs (Monolithic Memories, Texas Instruments, National Semiconductor, Advanced Micro Devices), built-in PALASM simulator and portability. Weighing only two pounds, PAL Burner is easy to pack in your briefcase to capture after-hours design inspirations.

In addition, PAL Burner is upward compatible. We can meet new firmware and software developments almost as they're introduced.

SD1000 PAL Burner

- **Assembles Boolean equations through new menu-driven PALASM**
- **Programs 20-pin and 24-pin PALs**
- **Programs MMI, National, TI, and AMD PALs**
- **Stores PAL design specification in E-PAC**
- **Verifies logic through Function Test**
- **Verifies Boolean equations through SIMULATE function**
- **Scores Function Test with Stuck-High/Stuck-Low FAULT Grading**
- **Verifies socket connection through Continuity Test**
- **Blows security fuse**



Also available is our original PAL Programmer, the SD 20/24 PAL Development System.

Call us first for a simple method — you won't need to call anyone else!

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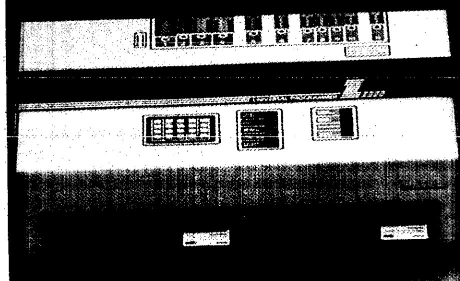
AMERICA'S BEST PROM PROGRAMMERS

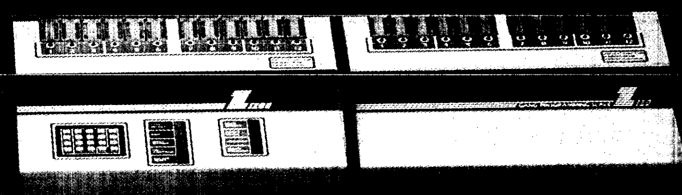
Two series of high tech instruments for EPROM/PROM/PAL/MPU programming.

Z SERIES programming units give you two independent RS-232 ports, 16 character alphanumeric displays, up to 128K x 8 of static RAM, full RAM editors, and prompted device selection. You can slave expand our universal or gang programmers for even greater production throughput of EPROMs, EEPROMs or Intel MPUs. These smart Z80A based units even calibrate themselves to save you time and ensure the best production lot yield.

For development applications or high volume programming, you can choose units with integral dual 8 inch DS/DD disk drives and CP/M* operating system.

ZAP SERIES of EPROM/MPU programmers are portable, easy to use and nicad battery operated. These compact, superbly engineered instruments give you many of the features of larger units plus PROM simulation. Use ZAP programmers for your engineering, low volume production and field service applications.



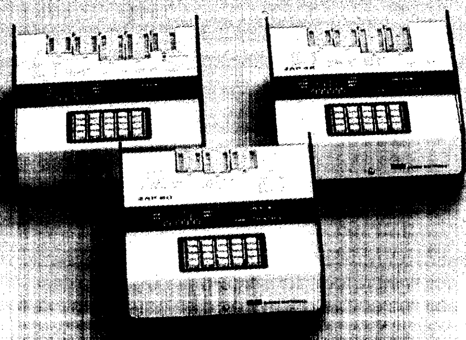


Z-2000B Disk Based Programmer

The Z-2000B universal programmer has all the features of the Z-1000B plus built-in dual 8 inch disk drives. Up to 2 megabytes of disk storage, 64K x 8 static RAM, CP/M* operating system, cross assemblers, two RS-232 ports and optional IEEE 488 interface makes this our premier programmer.

Z-1200/Z[illegible]

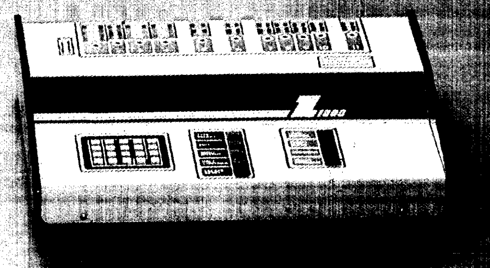
Z-1200s are design[illegible] EEPROMs simultaneously [illegible] You can add Z-120 gang [illegible] multiply your throughput and [illegible] gram Intel's 87XX family of microcom[illegible] Z-1248 programmer or Z-148 slave.



Zap Series EPROM/EEPROM/MPU Programmers

The ZAP SERIES of portable, battery operated programmers are designed for your development and field service needs.

These handy units program EPROMs and EEPROMs thru 27128, Intel and Motorola MPUs, use fast algorithms and have built-in PROM simulators. They also feature keystroke device selection, 16K x 8 DATA RAM, a sophisticated editor, 110 to 19.2K baud RS-232 ports and terminal control.



Z-1000/1000B Universal Programmers

The Z-1000 and 1000B program your EPROMs, bipolar PROMs, PALs, FPLAs and Intel microcomputers. Prompted device selection, fast algorithms and easily upgraded software let you program almost any device available now or in the future. These units are slave expandable for EPROM and MPU gang programming.

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INTRODUCTION TO CUSTOM/SEMICUSTOM CIRCUITS

This section describes services and products of companies supplying digital, linear and combined ditigal/linear custom circuits. Listed alphabetically in the Master Selection Guide, the companies are characterized by descriptions of design services, production facilities, process technologies and testing capability. Options for user contribution to custom-circuit projects are outlined by listing the vendor's preferred level of user input which can range anywhere from system concept to a known good device.

Semicustom Gate Arrays, Linear and Linear/Digital Arrays, Standard Cells, and Programmable Logic are covered in detail appropriate for locating devices or suppliers. In the semicustom area, performance parameters are circuit dependent and definitions are not standardized; therefore some are more useful in comparisons within a manufacturer's line than in comparisons between manufacturers. Frequently the manufacturer's data provides additional capability information that will assist in source selection.

Detailed Product Information provided by:

The manufacturers listed above have provided detailed information on their latest and most significant products.

EINFÜHRUNG KUNDEN-SPEZIFISCHE ICs

Deiser neue Abschnitt beschreibt Dienstleistungen und produkte von Herstellern, die digitale, lineare und kombinierte digital/lineare kundenspezifische Schaltkreise anbieten. Die Firmen werden in alphabetischer Reihenfolge genannt und anhand ihrer Fähigkeit zum Schaltkreis- Entwurf, ihrer Produktionsanlagen, Prozeβtechniken und Testmöglichkeiten beschrieben. Die verschiedenen Möglichkeiten des Anwenders im Hinblick auf dessen Angaben sind durch eine Auflistung der vom Hersteller gewünschten technischen Details erläutert. Diese können von einer Gundkonzeption bis zu einem bekannten, funktionierenden Bauelement reichen.

Die enthaltenen halb-spezifischen (semicustom) Bauteile beschränken sich auf Gatter- und Zellen-Arrays, die durch die letzte Maske zum kundenspezifischen Schaltkreis werden. Feldprogrammierbare Bauteile sind in diesem Abschnitt nicht enthalten. PALs werden unter Speichern (Memory) aufgeführt und PLAs finden sich sowohl im Memory- als auch im Digitalteil.

INTRODUCTION AUX CIRCUITS FAITS SUR COMMANDE

Nouvelle cette année, cette Section décrit les services et produits fournis par des sociétés fabriquant sur mesure des circuits digitaux, linéaires, digitaux/linéaires. Le Guide Général de Sélection offre sur plusieurs pages un tableau indiquant par fabricant les services offerts, les équipements disponibles, les systèmes technologiques, et les procédés de test utilisés. Les possibilités de collaboration entre le fabricant et le client sont également indiquées dans ce même tableau.

Les produits partiellement faits sur mesure ont été limités aux "portes" et "cellules de mémoire" qui sont individualisées par un procédé final d'interconnexion. Les appareils programmables à l'extérieur ne sont pas considérés dans cette Section. Le PALs sont étudiés dans la Section "Mémoires", et les PLAs se trouvent dans les Sections "Mémoires" et "Systèmes Digitaux".

INTRODUCCIÓN A LOS CIRCUITOS POR PEDIDO

Esta sección, nueva para este año, describe servicios y productos de compañías que ofrecen circuitos por pedido, sea digital, lineal y digital/lineal combinado. Apareciendo en orden alfabético el la Guía Maestra de Selección, las compañías se caracterizan por descripciones de servicio de deseño, taller de producción, technologia de processos y capacidad de distintas pruebas. Opciones de contribución por el operador en los proyectos de circuitos por pedido, están delineados en la lista de nivel de asistencia del operador preferido por el fabricante que abarca de concepto de sistema a pieza comprobada buena.

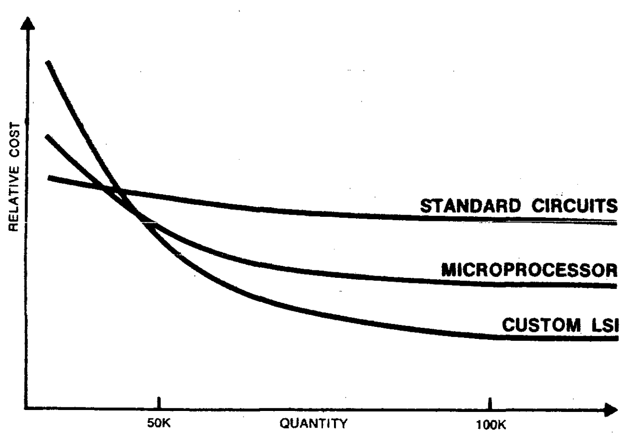
Componentes a pedido limitado están restringidos a redes de puertas y celdas electrónicas que son "a pedido" en el proceso final de interconección. Componentes programables en el campo no están incluidas en esta sección. Los PALs aparecen en las lista la sección de Memoria y los PLAs se encuentran en ambas secciones bajo Memoria y Digital.

カストムサーキットへの案内

本年新たに加わったこのセクションにはディジタル，リニア，双方兼ねたカストム回路を供給するメーカーのサーヴィスと製品を掲載しています。メーカー名はＡＢＣ順にマスターセレクションガイドにのっていますが，そのメーカー毎に，デザイン，製造設備，プロセス技術，テスト能力を示してあります。カストムサーキットに関するメーカー側のカストマー参加希望はシステムの概念から良く知られている製品の良品迄概略を記載しています。

セミカストム製品は最終の配線接続によりカストム化されるゲートアレイ，セルアレイに限定しています。フィールドプログラマブル製品はこのセクションにはのせていません。ＰＡＬはメモリーセクションに，ＰＬＡはメモリー，ディジタルセクションにあります。

Options for Going Custom



Standard circuits are recommended for production volumes below 1000 units. Intermediate-volume applications may benefit best from customizing through software, such as with microprocessors. Custom chips have the lowest cost at high-volume production. Source: National Semiconductor

For many applications, standard integrated circuits may be inappropriate from the standpoints of cost, size, power consumption or reliability. Moreover, unique features demanded by proprietary products often require entirely new circuit configurations. As a result, customized ICs are assuming an increasingly important role in system design.

Custom IC suppliers report that the chief benefits enjoyed by nearly all custom-circuit users are low-cost parts and cost savings resulting from reduced printed-circuit board space, parts handling, inventory, testing requirements and system maintenance. Obtaining these benefits requires careful consideration of the many options provided by both custom ICs and other approaches which ultimately effect economics.

For example, in addition to standard and custom parts, options for implementing new system designs include semicustom ICs, microcomputers, custom microcomputers, a mixture of microcomputers and custom ICs, or a mixture of all of these. The system development strategy used depends largely upon marketing objectives and may require staged system development, first with standard ICs, then with semicustom ICs and, finally, full custom units. Or, the strategy may dictate developing standard or semicustom prototype systems with concurrent verification of a full custom design.

Another option is to alter a standard microprocessor and other standard circuits, rather than using a full custom design. Customizing standard products can reduce the design costs, turnaround time and risks of a full custom design. In some cases, semicustom or custom circuits can replace microprocessors which have been used in dedicated, mostly controller-type applications. Or, a custom circuit may be a direct integration of several standard ICs, such as op-amps, comparators and resistor networks.

All approaches require up-front decisions involving design, prototype and production turnaround times, volume/cost trade-offs, alternate sourcing, circuit configuration and process technologies, and the user/supplier interface. The most critical factor, however, is cost.

The cost of a nonstandard IC includes expenses for design and tooling, wafer and chip processing, packaging and testing.

Design and Tooling: Until recently, IC users had just two options for implementing new designs: standard parts and full custom circuits. When standard parts were inadequate, a user had to commit to great production volumes to amortize high development costs. Additionally, development times often extended well over a year, and chances of initial success were relatively slim. However, custom suppliers have minimized these drawbacks by devising new customizing techniques to the extent that few custom circuits now are developed entirely from scratch.

Full Custom: In this approach the circuit designer draws from a collection of time-tested circuit modules and components to customize a chip. These elements of known performance are located on the chip with the assistance of CAD equipment to form optimized interconnect patterns, thereby minimizing chip area and thus cost. Full custom design gives the most efficient use of silicon chip area. Although design turnaround time has been longer than other options, advanced CAD techniques are closing the gap.

Semicustom: This approach produces custom circuits by interconnecting repetetive patterns of preprocessed circuit elements on a chip called a *masterslice*. Because a masterslice is processed just short of the final interconnect pattern, the same part is mass-produced for use by all customers, with customizing occuring at the final interconnect stage.

Gate arays are masterslices containing repetitive patterns of transistors connected as logic gates. *Device arrays* are patterns uncommitted transistors and resistors. The next level of customization uses an array of unconnected transistors and resistors called *cells*. Each cell can be interconnected internally to provide a specific logic function, and each cell on the chip interconnected into a customized system. The repertoire of allowable cell functions is called the *cell library*.

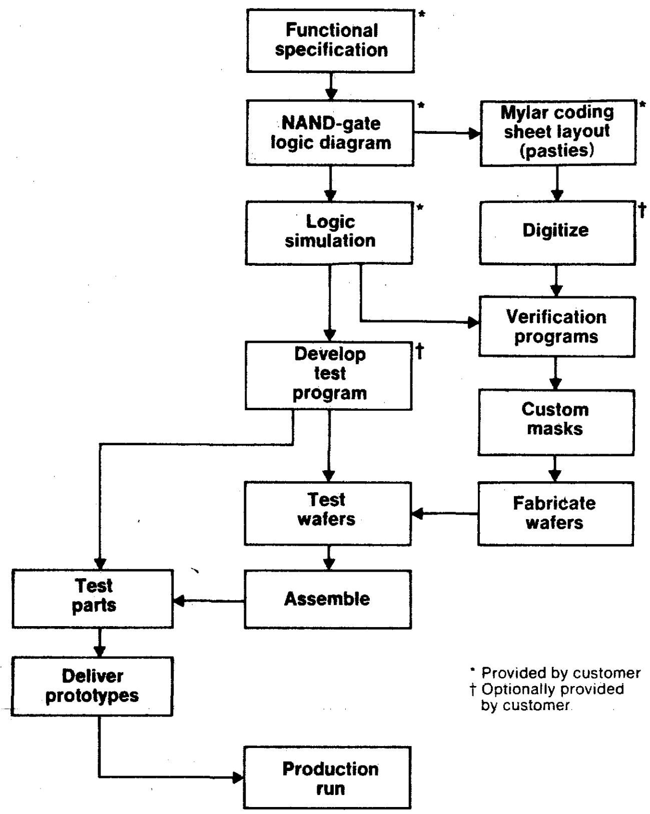
Interconnect design for masterslices can be manual or computer-aided. In all cases, the masterslice approach minimizes design turnaround time. Complex custom-cell library circuits can be obtained in about 18 weeks or less in prototype form; prototypes from gate arrays typically are available in about nine weeks.

One major disadvantage of masterslice circuits has been low circuit density. Circuit and device arrays require channels and alleys for routing interconnects. And because a single pattern must accommodate many different system designs, considerable interconnect routing space can be left unused after the chip is designed. Conversely, in a full custom design, unused space can be minimized. Consequently, a masterslice can be three times larger than an equivalent full-custom chip costing 20% to 60% less.

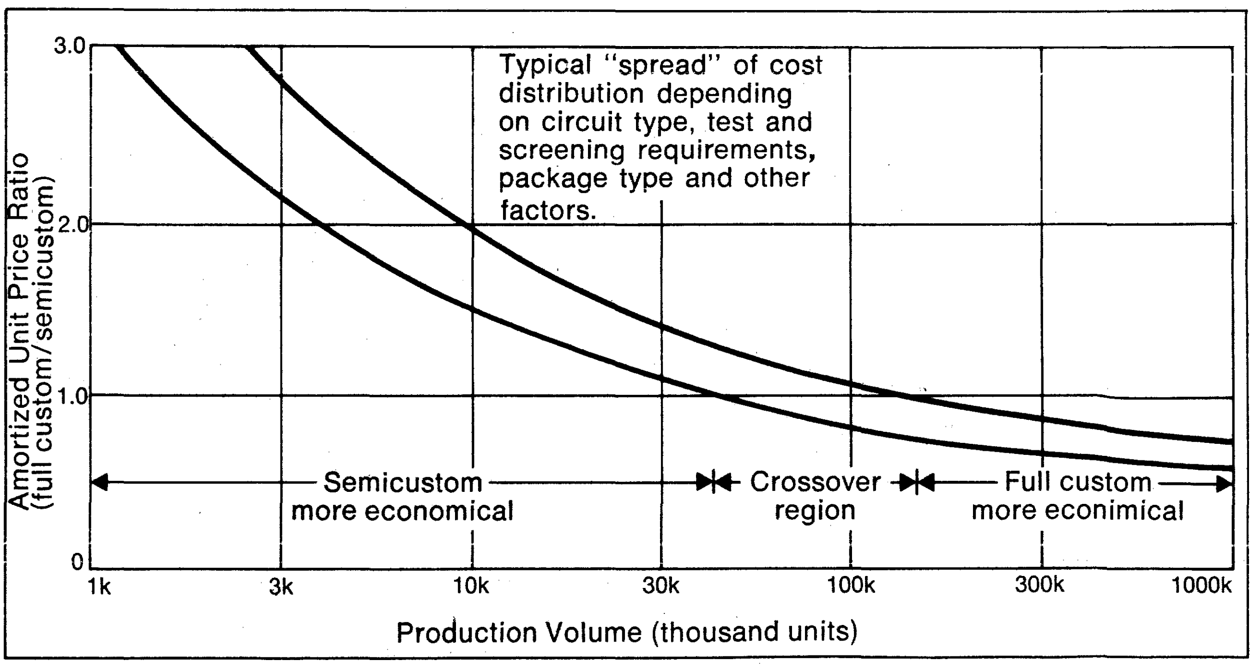
But masterslice manufacturers are increasing circuit densities to bring unit cost closer to that of full-custom circuits purchased in high volume. Circuits with two and three layers of interconnects are being developed to allow more efficient use of chip area. Triple interconnect-level masterslices are already used in a recent generation of IBM computers. So while full-custom designers are reducing design turnaround time, masterslice proponents are reducing unit cost.

Production: IC houses that process custom circuits basically sell a production service, not a design service. Most are concerned first with recovering design costs and then making profit on the volume production of parts. The general rule of thumb calls for total production volume representing at least ten times the supplier's design cost.

Some firms may accept a smaller production volume if engineering costs can be lowered. The customer may satisfy this requirement by using a design specialty firm or the in-house



Developing a custom IC is a multistage process. The degree of user involvement varies between companies. This diagram outlines the development of a custom chip designed from a cell library. Source: Signetics



Production volume influences the choice between full-custom and semicustom parts. However, other considerations (such as design turnaround time) may be overriding factors. Source: Exar engineering staff. Specialty firms provide services such as design, mask-making, assembly and testing. In many cases a design house controls the evolution of an IC through tooling, fabrication and final delivery.

Selecting a fabrication process based solely on chip cost is not entirely straightforward. For any given process, all wafers cost about the same regardless of circuit complexity. The cost of a chip is determined chiefly by yield, which tends to decrease with chip-area increase. Thus, chip cost varies directly with chip area.

Cost comparison between processes is more complex. Older processes do not necessarily produce higher yields than newer process techniques. And although processes involving more fabrication steps tend to have higher production cost per wafer, a more complex process may also allow circuit designs that produce smaller chips. Similarly, wafers fabricated by newer processes that involve expensive production equipment are usually costly. But, improved processes, although expensive, can produce high yields which tend to lower the die cost. The process must therefore be chosen to get the lowest chip cost consistent with meeting performance requirements.

Packaging: A standard package can cost from a few cents to several dollars. In many custom designs, package cost can be the largest part of unit cost, especially if a custom package is required.

Testing: This cost can be a large portion of the total unit cost. So care must be taken to design the chip for minimum testing requirements. Testing costs depend on the type of test equipment used and the amount of time required to test. Ideally the simplest and most widely available equipment should be used.

Testing cost can range from $50 per hour to several hundred dollars per hour. The manner in which tests are specified can vary test time per part from a few seconds to a minute. It is not economically feasible to test many complex digital circuits for every possible combination of inputs and outputs. And unless complex random logic is designed with testing in mind, it may not be possible to test the final product adequately.

Testing should be considered early in the design phase to minimize cost. Usually it is possible to select a process technology or circuit configuration that eliminates the need for some parametric tests. If timing requirements are critical, for example, using one of the faster process technologies or circuit configurations can eliminate testing speed parameters. Similarly, using a superior process for linear circuits could eliminate the need to test for offset voltages in op-amps.

Terminology

Assembly: Process of mounting a chip into a package and connecting the chip terminal pads to package terminals.

CAD: Computer-aided design. CAD includes computerized equipment that performs circuit simulation, logic simulation, automatic circuit and logic drawing, topological digitizing, topology construction on a CRT terminal, design rule checking and test generation.

Cell: Circuit performing a digital or linear function that is repeatedly used to design an LSI/VLSI chip.

Cell library: Collection of predesigned cell functions stored in a CAD data base. Custom LSI/VLSI devices can be designed by choosing appropriate cells from the library and locating them on a chip to minimize interconnects and maximize performance. The cells are computer characterized for performance much like SSI and MSI ICs with data sheets for each cell.

Custom circuit: In general, a component whose manufacture is under the exclusive control of a customer. The term can refer to full-custom, customized-standard or semicustom parts. In semicustom parts most of the mask layers are common to many customers, and only the final interconnect patterns are special. A customized part is a modification of a standard part to the requirements of a customer. Full-custom parts normally are fabricated from masks configured for the customer.

Design rules: Collection of rules that define minimum dimensions of device topological structures. Design rules also express process-parameter design limits such as gain factor, threshold level, oxide thickness and capacitance.

Die: Rectangular piece of semiconductor material into which electrical circuits have been fabricated. Also called a chip. Plural is dice.

Digitized data base: Recorded digital data representing a topological drawing of an SSI, MSI, LSI or VLSI device. The data include locations and dimensions of rectangles that make up individual circuit elements and interconnects.

Feature size: Dimensions of rectangles, lines and spacings in in an IC topological design.

Gate: Basic digital-logic element producing a binary output depending on the logic state of various inputs.

Gate array: Regular pattern of circuit components on a chip, connected to form regular patterns of gates. The gates are not interconnected until the customer specifies the chip function.

Gate equivalent: Basic unit of measure for digital circuit complexity based on the number of elementary logic gates needed to provide the same circuit function.

LSI: Large-scale integration. Device design integrating from 100 up to thousands of gate equivalents on a chip.

Macrocell array: Regular pattern of grouped, unconnected circuit components. Macrocells are formed into standard logic elements by interconnecting the components to provide specific circuit functions. Interconnects between the cells are specified to perform a specific chip function. The formation of the cell functions and cell interconnects are unique to the customer.

MSI: Medium-scale integration. Device design integrating from 10 to 100 gate equivalents on a chip.

Masterslice: In general, a partially processed chip containing circuit elements for customizing through final metal interconnect patterns. Can refer to gate, device or cell arrays.

Pastie: Scaled decal (usually transparent) representing both function and dimensions of an IC building block such as a gate, flip-flop or I/O buffer. Pasties are a commonly used tool for designing LSI/VLSI chips from a cell library. Each cell type has pastie equivalents.

SSI: Small-scale integration. ICs containing fewer than ten logic-gate equivalents.

Silicon gate: MOS design in which the gate is made of silicon instead of metal. Silicon-gate MOS is faster and more dense than metal-gate MOS.

VLSI: Very-large-scale integration. Device design integrating thousands of gate equivalents on a chip.

Cost: Intense activity in both gate arrays and associated development tools should make the gate-array concept extremely cost competitive with other design approaches. Typical costs for the development of a gate array and a full-custom IC are shown in the accompanying tables.

New gate arrays are currently in widespread development by IC manufacturers; CMOS products with up to 8,000 gates and emitter-coupled-logic (ECL) devices with 100-picosecond gate delays have already been developed. Although most of the attention has been concentrated on CMOS, many bipolar technologies are not being neglected.

Gate arrays are available in a number of bipolar technologies including ECL, Schottky TTL, integrated injection logic, integrated Schottky logic (ISL), and Schottky transistor logic (STL). Gate delays for these devices can be as low as 0.8 nanoseconds. Gate array chips are also available in NMOS and combination CMOS/NMOS versions.

Availability of computer-aided-design (CAD) tools and software support are helping both semicustom and custom products gain acceptance. In some cases, IC suppliers permit customers to use the supplier's in-house CAD facilities. Training courses, running three to five days, are also being offered by many IC manufacturers.

Custom IC cost factors.

Before Process Assembly
- Orders: Issues & Tracking
- Specific Documentation
- Orders: Issues & Tracking
- Purchase Prices
- Cost of Capital
- Inventory: Storage Space/Handling
- Incoming Inspection
- PC Board Space
- Power Consumption

After PC Assembly
- Test: Board
- Failure Diagnostic
- Test Active/Passive Components
- Repair
- Re-Test
- Re-Inventory

Typical costs for the development of a 1000-gate array.

	min.	max.
1. Tooling Development		
A) Circuit Conversion	$500	$1500
B) Layout	$2.5K	$5K
C) Digitization, PG Tape, Masks, 20 prototype units in ceramic DIP, bench tested	$9K	$13K
2. Preproduction		
A) Test Program Development	$4K	$8K
B) Test hardware		
Personality Board	$1K	$2K
Probe Card	$100	$200
Special Supplies, Signal Generator	*	*
Burn-In Board	$500	$2500
Other	*	*
C) Production Qualification Units (Optional)		
Burned-In, Temperature Tested 100 units	3K	$6K
883B Environmental Screening	Extra	
TOTAL	$18K	$40K
* Depends on application		

Typical development costs for a full-custom integrated circuit.

			min.	max.
1. Tooling Development				
A) Circuit to LSI Conversion				
B) Layout				
C) Digitization, PG Tape, Masks			$20K	$200K
2. Engineering Evaluations: 5 wafers				
Working Plates		Per Plate	$50	$100
Bipolar:	1-Layer Metal	4-6 weeks	$3K	$6K
	2-Layer Metal	6-8 weeks	$5K	$10K
	Pt Schottky Diodes	- week extra		
CMOS:	1 Poly, 1 Metal	6-8 weeks	$3K	$5K
	Same, 4 Micron	6-8 weeks	$4K	$6K
May need several iterations, usually 2 to 4				
3. Prototypes				
A) Establish Waferbank				
30-45 Wafers from Several Runs			$10K	$30K
B) First Look Samples 100 Untested Dice Packaged in Ceramic Sidebraze			$600	$1500
C) Test Program Development			$5K	$30K
D) Test Hardware				
Personality Board			$1K	$2K
Probe Card			$100	$200
Special Supplies, Signal Generators			*	*
Burn-In Board			$500	$2500
Other			*	*
E) Production Qualification Units (if desired)				
Burned-In, Temperature Tested 100 Units			$3K	$6K
883B Environmental Screening			Extra	
TOTAL			$40K	$280K
* Depends on application				

Comparison. The relative ranking of risk factors for alternative design approaches is shown at the right. These ratings will vary depending on the selected suppliers for custom, cell library, gate array or non-LSI devices. Therefore, this chart should be used only as a guide. In the case of linear designs, risks are greater than for digital counterparts. Unless the various circuit blocks assembled from a cell library are compatible with each other from the standpoint of processing, the overall performance of the chip can be less than expected. For instance, the breakdown voltage, beta, sheet resistance, implant dosage, and epi thickness requirements, to say nothing of the starting material, may be mutually exclusive. Also, NPN and PNP transistor configurations cannot both be optimized for performance as is possible with discrete devices.

Comparisons of advantages of various design approaches. A rating of 1 indicates best. (Numbers in parenthesis apply to linear designs.)

	Full Custom	Cell Library	Gate Array	Non-LSI
Design Costs	4(3)	3(4)	2	1
Design Time	4(3)	2(4)	3(2)	1
Mask Costs	4	4	2	1
Redesign Flexibility	4	3	2	1
Test Program Costs	3	3	2	1
Circuit Purchase Price	1	2	3	4
System Power Required	1	2	2	4
Reliability	1	2	2	4
PC Board & Costs	1	2	2	4
Production Labor	1	2	2	4
Security	1	3	2	4
Added Features/ Board	1	3	3	4

CUSTOM CONSIDERATIONS

Benefits provided by custom, related to cost factors, are described in the following paragraphs:

Specification Documentation: Since a single custom IC can replace as many as 100 MSI circuits (plus assorted external active and passive components, such as decoupling capacitors, diodes, and transistors), paperwork needed is greatly reduced.

Purchasing: The purchasing function is not a "free" activity in any company. It costs money to issue purchase orders, and to track them through various delivery dates and procedures with phone calls and computer time. The lower parts count significantly reduce this paper load.

Purchase Price: Depending on the complexity of the chip, the price for a custom device can be lower, at, or above that of all the components to be replaced. It is important to count all of the passive peripheral components involved, such as sockets, resistors, capacitors, inductors, and perhaps even connector pins to the outside.

Cost of Capital: This cost varies with prevailing interest rate. If a company has to borrow development money, usually at about three or four percent over prime rate, then this interest is also an expense incurred by the project. But even if cash is available, there still may be an opportunity cost. This is the income that could have been earned if the cash had been used on short-term projects (such as buying more inventory — provided the sales to turn the inventory over exists).

Inventory: Once the material is in the plant, it has to be handled (including counting, sorting, and paperwork), and stored. Usually, storage space is predefined, and, since it already exists, it is not considered to be an additional expense. However, one has to remember that real estate value on a per-footage basis is substantial and that other departments might make a more cost effective use of any space available. Hence, an additional cost is incurred for each additional component that has to be stored and accounted for. Also, components may become obsolete before the inventory is used up. Custom ICs contribute to decreasing inventory expenses.

Incoming Inspection: Unless pre-aged and pre-screened components are bought to prevent early failures (infant mortality), it is advantageous to inspect active components as they come in. Again, a reduction in the number and variety of devices to be tested adds to profits.

Printed Circuit Board Space: Fewer components mean less space needed to mount them, less auxiliary components, less artwork for interconnect lines, fewer holes to be drilled, and less insertion time and effort — as well as a smaller board.

Power Consumption: The power consumption of the entire system is usually dramatically reduced, making savings possible with lowered power supply and cooling requirements.

CUSTOM/SEMICUSTOM

Manufacturer	Advanced Micro Devices	Alphatron	American Microsystems, Inc.
FOR DETAILED DATA SEE:	(Page 4600)		(Page 4614)
Customized Standard Circuits			Digital, Linear, Combined Digital/Linear
Gate Array	Programmable Array Logic		3μ and 5μ silicon-gate CMOS
Chip Density Range (equiv. gates)	200 to 800	Up to 4400 2-input gates	300 to 1200 2-input gates (5μ) 500 to 5000 2-input gates (3μ)
Cell Library		CMOS	Yes
Design Kit Available	Yes	Yes	Yes
Full Custom Circuits Digital		Silicon- or metal-gate PMOS, NMOS, CMOS	Silicon- or metal-gate PMOS, NMOS, CMOS with high-voltage output capability.
Linear		Silicon- or metal-gate PMOS, NMOS, CMOS	Silicon-gate NMOS, CMOS, filter, amplifier to rf
Combined Digital/Linear		Silicon- or metal-gate PMOS, NMOS, CMOS	Silicon-gate NMOS, CMOS, 14-bit resolution, VHF-rf
Provide Design Assistance	Yes	Yes	Yes - class instruction
Acceptable Customer Input (in order of preference)		Alphamap layout logic diagram functional description block diagram.	Logic diagram, functional specification, data-base tape, PG tape, masks, COT.
Design Aids	AMPALASM-20 software for Boolean equation generation. AMPLPL software provides similar capability for advanced products.	Logic simulation, breadboard assistance, design rule checks, decals.	Complete CAD assistance for logic circuit simulation design rule checks, breadboard assistance.
Production	In-house	Wafer production procured from outside foundries. Testing done in-house.	Masks, fabrication and assembly in-house.
Preferred Delivered Product	Ceramic and plastic DIPs, leadless chip carriers, dice; all available in commercial and military.	Any upon request	DIP, chip carriers, die-on-board packages, wafers, die to commercial or military specifications.
Test Program Generation		Yes	Yes, CAD supported
Production Test	100% dc, ac and functional testing. Burn-in, thermal shock, environmental, MIL.	Functional, parametric, burn-in, thermal shock, environmental, MIL.	Functional, parametric, burn-in, thermal shock, environmental, MIL.
Electrical Test Systems Available	Xincom, Accutest	In-house designed, customer-supplied, or outside service.	Sentry, Teradyne, Xincom, LTX, General Radio.
Comments	Commercial programmers available Software output JEDEC PLDTF. Most complex programmable logic parts available.	Multiple sourcing. Cell library and design rule handbook.	Complete custom capability including design, instruction, CAD and process licensing and technology sales. CAD also available through timesharing and at Design Centers.

CUSTOM/SEMICUSTOM (cont)

Manufacturer FOR DETAILED DATA SEE:	Applied Micro Circuits	AWI	Barvon Research (Page 4626)
Customized Standard Circuits		Linear, Digital, Combined Digital/Linear	Digital Combined Digital/Linear
Gate Array	ECL	Bipolar, CMDS, silicon-gate MOS, hybrids	2-5μ silicon-gate CMOS, Bi-CMOS (Bipolar and CMOS)
Chip Density Range (equiv. gates)	250 to 1500 gates	10 to 10,000	100 to 10,000 2-input gates
Cell Library	ECL	Over 2600 type	CMOS, Bi-CMOS
Design Kit Available	Yes	Yes	Yes
Full Custom Circuits Digital	ECL	Yes	Silicon-gate CMOS, HCMOS, HMOS, Bi-CMOS
Linear		All processes	Silicon-gate CMOS, HCMOS, Bi-CMOS
Combined Digital/Linear		All processes	Silicon-gate CMOS, HCMOS, Bi-CMOS
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Functional specification, logic diagram, test vectors, PG Tape, Tegas Tape.	Functional schematic, circuit diagram	Logic diagram, circuit diagram, breadboard, functional specification, test vectors, COT, known good device.
Design Aids	Logic simulation, design rule checks.	Users manual	Circuit simulation, logic simulation, schematic entry, test program generation, design rule checks, breadboard assistance.
Production	In-house, procured	In-house robotics and automation	In-house, procured
Preferred Delivered Product	Packaged dice	Printed card mounted, packaged units	Packaged devices, others available
Test Program Generation		No	Yes
Production Test	Functional, parametric, burn-in, thermal shock environmental.	Functional	Functional, parametric, burn-in, thermal shock, environmental, MIL.
Electrical Test Systems Available		Customer supplied	Sentry, Teradyne
Comments			Complete custom capability including design, instruction, CAD and technology licensing. Standard cell library available.

CUSTOM/SEMICUSTOM (cont)

Manufacturer FOR DETAILED DATA SEE:	California Devices	Cherry Semiconductor	Circuit Technology Inc.
Customized Standard Circuits	Digital	Digital, Linear, Combined Digital/Linear	Digital
Gate Array	Silicon- or metal-gate CMOS	I^2L, LSI^2L, ECL and other bipolar	Silicon gate CMOS
Chip Density Range (equiv. gates)	50 to 1780 2-input gates	64 to 150 gates/mm^2	560 to 1440 — 5 micron single metal 1120 to 3876 — 4 micron double metal
Cell Library	Silicon- or metal-gate CMOS	I^2L, LSI^2L, ECL and other bipolar	CMOS and LSTTL
Design Kit Available	Yes	Yes	Yes plus CAD
Full Custom Circuits Digital		I^2L, LSI^2L, ECL and other bipolar	Silicon gate CMOS
Linear	Bipolar linear arrays	I^2L, LSI^2L, ECL and other bipolar	
Combined Digital/Linear		I^2L, LSI^2L, ECL and other bipolar	
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Logic diagram with test vectors and PG tape; circuit diagram with data-base tape and composite drawing; breadboard.	Customer-owned tooling; circuit diagram; logic diagram; breadboard.	Logic diagram and test vectors. Customer-owned tooling. Functional specification.
Design Aids	Logic and circuit simulation; breadboard assistance; design rule checks.	Logic simulation; breadboard assistance; design rule checks.	Logis simulation, auto layout, rules checks, network comparison checks.
Production	In-house and procured	In-house	In-house plus second sourcing availability.
Preferred Delivered Product	Scribed dice, packaged dice, substrate-mounted device.	Packaged dice; flip chips	All options available
Test Program Generation	Yes	Yes	Yes
Production Test	Functional, parametric, burn-in, thermal shock, environmental, MIL.	All except military	Full capability including full MIL, class S and geothermal (200°C).
Electrical Test Systems Available	Sentry VII, Sentry Series 20	Teradyne 1259, A310, A311	Fairchild series 10
Comments	Si-gate isolated oxide CMOS has TTL/LSTTL interfacing capability, high-speed performance.	Dice can be solder-bump flip chips with nitride passivation; packaged dice can be delivered from COT for full custom.	No limit on package variety. In-house multichip hybrid capability.

CUSTOM/SEMICUSTOM (cont)

Manufacturer FOR DETAILED DATA SEE:	Circuit Technology Inc.	Citel (Page 4628)	Comlinear Corp.
Customized Standard Circuits	Digital	Digital	Yes
Gate Array	CMOS on Sapphire	3μ silicon-gate CMOS	
Chip Density Range (equiv. gates)	1120 to 3876-4 micron double metal	200 to 1200	
Cell Library	CMOS and LSTTL	Yes	
Design Kit Available	Yes plus CAD		
Full Custom Circuits Digital	CMOS on Sapphire	Silicon or metal-gate CMOS, silicon-gate NMOS, bipolar	
Linear		Bipolar	Bipolar-FET
Combined Digital/Linear		CMOS	
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Logic diagram and test vectors. Customer-owned tooling. Functional specification.	Logic diagram, circuit diagram, functional specification, bread-board, data-base tapes, PG tapes, mask sets, customer-owned tooling.	Functional specification
Design Aids	Logic simulation, auto layout, rules checks, network comparison checks.	Logic simulation, design-rule checks, net-list verification.	Computer simulation
Production	In-house	In-house	In-house or procured
Preferred Delivered Product	All options available	Packaged units; will supply wafers or dice.	Packaged circuit, printed card mounted units.
Test Program Generation	Yes	Yes	Yes
Production Test	Full capability including full MIL and class S.	Functional, parametric	Functional, burn-in, thermal shock, linear, MIL
Electrical Test Systems Available	Fairchild series 10	Sentry VII	Complete time domain and frequency domain testing from dc to 18 GHz.
Comments	No limit on package variety. In-house multichip hybrid capability.	Complete custom capability	Specialties include amplifiers with extremely wide bandwidth and fast settling time, fast sample-hold and A to D conversion products.

CUSTOM/SEMICUSTOM (cont)

Manufacturer FOR DETAILED DATA SEE:	Custom Integrated Circuits	Custom MOS Arrays (Page 4630)	Exar Integrated Systems (Page 3386)
Customized Standard Circuits	Digital, Linear, Combined Digital/Linear	CMOS	Digital, Linear, Combined Digital/Linear
Gate Array	I²L, Linear Master Slice, design on other companies' gate arrays		Metal-gate CMOS; I²L Si-gate CMOS
Chip Density Range (equiv. gates)	50 to 8000 (5-input gates)	448 to 1568 (2 inputs)	100 to 1250
Cell Library	I²L	Yes	Metal-gate CMOS; I²L Si-gate CMOS
Design Kit Available			Yes
Full Custom Circuits Digital	I²L, CMOS, TTL and other bipolar devices		Metal-gate CMOS; I²L Si-gate CMOS
Linear	Bipolar, CMOS		No
Combined Digital/Linear	I²L/Linear, TTL/Linear, CMOS/Linear		I²L, other bipolar
Provide Design Assistance	Yes		Yes
Acceptable Customer Input (in order of preference)	No preference		Complete layout, breadboard, circuit diagram, logic diagram, functional diagram.
Design Aids	Logic simulation, circuit simulation, design rule checks, breadboarding, complete Calma layout system, in-house CAD software, engineering assistance.		Logic simulation; breadboard assistance; design rule checks.
Production	Procured		In-house
Preferred Delivered Product	No preference		Probed wafers, scribed dice, packaged dice.
Test Program Generation	Yes		Yes
Production Test	All		Functional, parametric, environmental, burn-in
Electrical Test Systems Available	HP, MCC		Sentry; Fairchild 5000, Teradyne J273, A311; Amdahl
Comments	Total IC development from concept through product delivery. Any subset of the development cycle (design, layout, etc.)		

CUSTOM/SEMICUSTOM (cont)

Manufacturer	Fairchild	Ferranti	Fujitsu
FOR DETAILED DATA SEE:	(Page 4634)		(Page 4637)
Customized Standard Circuits	Digital	Linear, Digital, Combined Linear/Digital	Digital
Gate Array	Bipolar ECL	Collector Diffusion Isolation	Silicon-gate CMOS, LSTTL
Chip Density Range (equiv. gates)	20 to 1000 3-Input NAND	200 to 10,000 Gates/chip	200 to 8000 2-Input NAND
Cell Library		Collector Diffusion Isolation	Silicon-gate CMOS, LSTTL
Design Kit Available		Yes	Yes
Full Custom Circuits Digital		Collector Diffusion Isolation	Silicon-gate CMOS, LSTTL
Linear		Collector Diffusion Isolation	Silicon-gate CMOS, LSTTL
Combined Digital/Linear		Collector Diffusion Isolation	
Provide Design Assistance		Yes	Yes
Acceptable Customer Input (in order of preference)		Pattern-generator tape, composite drawing when done on Ferranti's supplied design station; functional specification, logic diagram, circuit diagram, breadboard, test vectors.	Logic data and test timing data (Fujitsu format).
Design Aids	Logic simulation, breadboard assistance, design rule checks.	Logic simulation, breadboard assistance, design rule checks, full design capability.	Logic simulation, design rule checks; complete CAD system.
Production	In-house	In-house	In-house
Preferred Delivered Product		Packaged dice	Substrate mounted dice
Test Program Generation		Yes	Automatic
Production Test		Functional, parametric, burn-in, thermal shock, environmental, MIL, linear.	Functional, ac and dc parametric.
Electrical Test Systems Available	FARCAD	LTX, Teradyne, Custom	In-house
Comments	Remote access to FARCAD via telephone link	Semi-custom from off-the-shelf selection of a range of standard wafers.	Dual-layer metal; CAD system verifies design; auto placement and routing from customer's inputs.

CUSTOM/SEMICUSTOM (cont)

Manufacturer FOR DETAILED DATA SEE:	General Instrument	GTE Microcircuits	Harris Semiconductor (Page 4644)
Customized Standard Circuits			Digital, Linear, Combined Digital/Linear
Gate Array	Silicon-gate CMOS	ISO-CMOS	Silicon-gate CMOS, TTL-AS, TTL-ALS
Chip Density Range (equiv. gates)	560 to 2014	504 — 2500	Up to 10,000 (CMOS) Up to 2,500 (TTL-AS) 120, 312 and 918, (TTL-ALS) (Rad Hard)
Cell Library	Silicon-gate CMOS	ISO-CMOS	Silicon-gate CMOS, TTL-AS
Design Kit Available	Yes	Yes	Yes
Full Custom Circuits Digital	No	ISO-CMOS	Metal-gate CMOS and MOS; silicon-gate PMOS, LSTTL; ALSTTL; STTL; I²L.
Linear	No	ISO-CMOS	Bipolar (dielectric isolation) CMOS/bipolar (metal-gate/bipolar) and silicon.
Combined Digital/Linear	No	ISO-CMOS	Silicon-gate CMOS; bipolar
Provide Design Assistance	No	Yes	Yes
Acceptable Customer Input (in order of preference)	No	Calma tapes, PG tapes, masks	System specification, Logic diagram, JG, CALMA or Mebes Data Base.
Design Aids	No	Design rule checks, Logic simulation	Proven Cell Library MACROS, Logic Simulation, Layout Programs and Test Grading.
Production	No	In-house	In-house
Preferred Delivered Product	No	Packaged die, probed wafers, mapped wafers	Wafer, packaged dice, scribed dice, and packaged devices.
Test Program Generation	No	Yes	Yes
Production Test	No	Functional, parametric, burn-in	Up to and included equivalent Class "S" military flow. Also in-house total dose testing.
Electrical Test Systems Available	No	Sentry LTX, H.P., Mega, XINCOM	Sentry
Comments			Also offer low voltage CMOS. Radiation hardening for most process technologies. Also provides silicon foundry.

Master Selection Guide

CUSTOM/SEMICUSTOM

CUSTOM/SEMICUSTOM (cont)

Manufacturer FOR DETAILED DATA SEE:	Holt, Inc. (Page 4745)	Integrated Circuit Systems	Integrated Technology Corporation
Customized Standard Circuits	Linear, Digital, Combined Linear/Digital	Digital, Linear, Combined Digital/Linear	
Gate Array	Metal gate CMOS, linear bipolar	CMOS	
Chip Density Range (equiv. gates)	80 to 1098		
Cell Library	Metal gate CMOS	All MOS processes	
Design Kit Available	No		
Full Custom Circuits Digital	Silicon gate, metal gate CMOS	CMOS/SOS; CMOS, DMOS, NMOS, SI or Metal Gate; Double level metal; Double level poly.	Silicon- or metal-gate MOS; TTL, STTL, LSTTL, I²L, ECL, other bipoar
Linear	Bipolar	CMOS	Silicon- or metal-gate CMOS; bipolar
Combined Digital/Linear	Metal gate CMOS and bipolar	CMOS	Silicon- or metal-gate CMOS; bipolar
Provide Design Assistance	Yes	Yes	
Acceptable Customer Input (in order of preference)	Any	No minimum required	
Design Aids	Logic simulation, breadboard assistance, DRC.	DRC and ERC on VAX 11/780, Calma GDS II, sticks software, production test, systems.	Logic simulation; breadboard assistance; design rule checks; transient analysis.
Production	Procured	Small to medium quantity	Procured
Preferred Delivered Product	Packaged die, scribed die	Packaged parts	Mapped wafers; probed wafers; packaged dice; PC-mounted packaged units; design tooling; complete systems.
Test Program Generation	Yes	Yes	Yes
Production Test	Functional, parametric, burn-in, thermal shock, environmental, MIL, Linear SEM.	Yes	Functional; parametric
Electrical Test Systems Available	IT-200	Megatest	Siemens
Comments		Services: design, layout, chip/PCB artwork, test generation, product engineering, test and production.	Services: design, tooling for custom ICs; service industry used for photomasks, wafer fab, assembly, some testing. System design and production with custom IC's.

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CUSTOM/SEMICUSTOM

CUSTOM/SEMICUSTOM (cont)

Manufacturer FOR DETAILED DATA SEE:	Interdesign (Page 4747)	International Microcircuits (Page 4748)	International Microelectronic Products (Page 4749)
Customized Standard Circuits	Digital, Linear, Combined Digital/Linear	Digital	Digital, Combined Linear/Digital
Gate Array	CDI RTL and CML, metal-gate, CMOS, silicon-gate CMOS; bipolar	Silicon- or metal-gate CMOS	No
Chip Density Range (equiv. gates)	See comments	75 to 7500	200 to 10,000
Cell Library	Yes	Yes	Silicon-gate CMOS
Design Kit Available	Yes	Yes	Yes
Full Custom Circuits Digital	Silicon-gate CMOS; metal-gate CMOS; CDI bipolar; Linear bipolar; Linear CMOS.		Silicon-gate NMOS and CMOS
Linear	Bipolar		
Combined Digital/Linear	All linear functions		Silicon-gate NMOS and CMOS
Provide Design Assistance	Yes		Yes
Acceptable Customer Input (in order of preference)	Pencil-connected layout; logic diagram; specification; PG tapes; circuit diagram and breadboard (for linear bipolar).		Functional specification, logic diagram, circuit diagram, breadboard, test vectors, customer-owned tooling (pattern-generator tape, composite drawing), known good device.
Design Aids	Logic/circuit computer simulation; breadboard parts; layout sheets; functional overlays; evaluation parts.		Logic simulation, breadboard assistance, design rule checks, engineering assistance.
Production	Metallized wafers procured; other functions in-house.	In-house and procured	In-house
Preferred Delivered Product	Packaged dice, bare dice, probed wafers.	Scribed dice; packaged dice	Mapped wafers, probed wafers, scribed dice, packaged dice, or special packages.
Test Program Generation	Yes	Yes	Yes
Production Test	Functional; parametric; burn-in; MIL 883B; environmental.	Functional, parametric, burn-in, thermal shock, environmental, MIL.	Functional, parametric, burn-in
Electrical Test Systems Available	Teradyne J325; LTX CP/TS70; LOMAC LM325; Fairchild 5000; LTX DX90, Pragmatic Inspector 100.	GenRad, Sentry	Sentry 20, Kiethley
Comments	CDI RTL; 255 logic cells; CDI CML 450-2000 gates; metal-gate CMOS: 140-800 gates. Silicon-gate CMOS 150-2000 gates. Linear bipolar 100-150 components.		

CUSTOM/SEMICUSTOM (cont)

Manufacturer FOR DETAILED DATA SEE:	Intersil (Page 4751)	LSI Computer Systems (Page 4761)	LSI Logic (Page 4762)
Customized Standard Circuits	Digital, Linear/Digital		Digital
Gate Array	Silicon-gate CMOS, 2μ and 4μ		Silicon-gate CMOS, HCMOS and ECL
Chip Density Range (equiv. gates)	To 15,000		300 to 10,000
Cell Library	Yes		7400/4000 CMOS and HCMOS, ECL: 10K-SSI/MSI functions
Design Kit Available	Yes		Yes
Full Custom Circuits Digital	CMOS	Metal-gate PMOS, CMOS; Silicon-gate NMOS; Silicon-gate CMOS.	Implemented in gate array format Silicon gate oxide isolated CMOS/HCMOS; oxide isolated bipolar ECL.
Linear	CMOS	Metal-gate PMOS, CMOS; Silicon-gate CMOS	
Combined Digital/Linear	CMOS	Metal-gate PMOS, CMOS; Silicon-gate CMOS	
Provide Design Assistance	Yes	Yes	
Acceptable Customer Input (in order of preference)	Schematic, logic diagram, test vectors.	Logic diagram; customer-owned tooling (pattern-generation tape, composite drawing); circuit diagram; breadboard; functional specification.	Logic diagram to PG tape — Many input formats possible depending on customer interface required.
Design Aids	CAD assistance, training, manuals.	Design rule checks, computer-aided transient analysis, Applicon 760.	LSI design system (LDS), including design entry, circuit simulation, logic simulation, PG and test tape generation via remote terminal or factory based.
Production	In-house	Procured	In-house
Preferred Delivered Product	Packaged dice	Packaged dice, dice	Packaged dice
Test Program Generation	Yes	Yes	Yes
Production Test	Functional, parametric, burn-in, thermal shock, environmental, MIL.	Functional, parametric, burn-in; thermal shock, environmental; MIL.	Functional parametric to MIL 883B.
Electrical Test Systems Available	Sentry, Teradyne, Xincom, Tektronix	Macrodata 107 and customized equipment.	Industry standard tester
Comments	Specialize in linear and data-acquisition signal-conditioning circuits.	Multiple-sourced production	Multiple sourced

CUSTOM/SEMICUSTOM (cont)

Manufacturer FOR DETAILED DATA SEE:	Master Logic	MCE Semiconductor	Micrel Inc. (Page 4765)
Customized Standard Circuits	Digital	Linear, Digital, Combined Linear/Digital, Bipolar, CMOS	
Gate Array	Silicon- or metal-gate CMOS	CMOS, ECL, Dielectric Isolation, I²L, Linear	
Chip Density Range (equiv. gates)	50 to 1500, silicon-gate 50 to 600, metal-gate	50 to 10,000 gates	
Cell Library	Yes	Yes	
Design Kit Available	Yes	Yes	
Full Custom Circuits Digital	Silicon- or metal-gate CMOS	CMOS, TTL, LSTTL, I²L, ECL, Linear	PMOS, CMOS, NMOS silicon or metal-gate, isoplanar type processing.
Linear	No	Up to 75 Volt	Bipolar, CMOS
Combined Digital/Linear	Yes	Up to 20 Volt	
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Any	MCE will interface with customer anywhere in design sequence. UniDES; software.	Customer owned tooling, PG Tape, Data base tape.
Design Aids	Design Manual, CAD with VIA Systems, "Gates" design package.	Logic simulation; breadboard assistance; design rule checks; UNIDES.	Design rule checks
Production	Procured	In-house manufacturing; 4" Wafer Fab	In-house wafer fabrication; 3- and 4-inch lines procurred asembly.
Preferred Delivered Product	Any	Mapped wafers; probed wafers; scribed dice; substrate-mounted dice; packaged dice; custom packaging.	Packaged tested die, probed wafers, mapped wafers.
Test Program Generation	Yes	Yes	Yes
Production Test	In-house	Functional; parametric	Functional, parametric, burn-in, MIL STD 883.
Electrical Test Systems Available	Pragmatic designs	Teradyn J273 and A300 with laser trim; Pragmatic Inspector 200 (72 pin digital IC); Kiethley 300.	Sentry VII, Series 20
Comments	Multiple sourced	Functional arrays available CMOS MGA and SGA series; also linear function cells.	

CUSTOM/SEMICUSTOM (cont)

Manufacturer FOR DETAILED DATA SEE:	Microcircuits Technology, Inc.	Micro Innovators	Micro Power Systems (Page 4766)
Customized Standard Circuits	Digital, Linear, Digital/Linear	Digital	
Gate Array	Linear bipolar, metal gate NMOS, CMOS; silicon gate CMOS		
Chip Density Range (equiv. gates)	250 to 6000 gates	50 to 250 mil²	
Cell Library	Silicon gate or metal gate NMOS, CMOS, linear bipolar		Poly-gate CMOS, bipolar LSI, thin film on silicon
Design Kit Available	No	No	No
Full Custom Circuits Digital	Silicon gate CMOS, Metal Gate CMOS	Silicon- or metal-gate PMOS, NMOS, CMOS, other MOS	Low-voltage, poly-gate CMOS
Linear	Bipolar, CMOS	Silicon- or metal-gate PMOS, NMOS, CMOS, other MOS	High-gain/low current analog bipolar; thin-film resistor
Combined Digital/Linear	CMOS and bipolar	Silicon- or metal-gate PMOS, NMOS, CMOS, other MOS	Bipolar and CMOS
Provide Design Assistance	Yes		Yes
Acceptable Customer Input (in order of preference)	Logic diagram, breadboard, block diagram, functional specifications.	Functional specification; logic diagram; circuit diagram; breadboard; test vectors; customer-owned tooling.	Circuit/logic diagram; breadboard; functional specifications; customer-owned tooling.
Design Aids	Calma CAD, logic simulation, circuit simulation.	Logic simulation; breadboard assistance; design rule checks.	Breadboard assistance; cooperative design from logic/circuit diagrams.
Production	In-house, procured	In-house	In-house
Preferred Delivered Product	Packaged units	Probed wafers; packaged dice	Custom packaging; all standard configurations except mapped wafers.
Test Program Generation	Yes	Yes	Yes
Production Test	Functional, parametric, burn-in, environmental, MIL, linear	Functional; parametric; burn-in	All
Electrical Test Systems Available	Fairchild Sentry	Sentry, Teradyne, Comparator	Fairchild, Datatron, Macrodata, custom.
Comments	MOS: 3 and 5 micron channel lengths.	Tooling can be used by at least two MOS wafer manufacturers to ensure alternate sourcing.	

CUSTOM/SEMICUSTOM (Cont)

Manufacturer FOR DETAILED DATA SEE:	Micro-Sciences	Mitel Semiconductor (Page 3048)	Monolithic Memories Inc. (Page 4768)
Customized Standard Circuits	Digital	Digital	
Gate Array	CMOS	Silicon-gate CMOS	Field Programmable Logic — PAL and mask — programmed version — HAL.
Chip Density Range (equiv. gates)	300 to 6000	500 — 6000 gates	100 to 350 gates
Cell Library	CMOS, NMOS	Silicon-gate CMOS	
Design Kit Available	No	Yes	Yes
Full Custom Circuits Digital	Silicon- or metal-gate PMOS, NMOS, CMOS	Silicon-gate CMOS	
Linear		Silicon-gate CMOS, double poly	
Combined Digital/Linear		Silicon-gate CMOS, double poly	
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Logic diagram; circuit diagram; functional specification; breadboard; customer-owned tooling; known good device.	Functional specification, logic diagram, circuit diagram, customer-owned tooling.	PALs — not required, field programmable. HALs — logic equations, 25-50 "seed" vectors for test generation software.
Design Aids	Logic simulation; breadboard assistance.	Logic simulation, design rule checks.	PALASM software for simulation, fault grading, fuse pattern generation, (mask design input for HALs).
Production	Procured	In-house	In-house
Preferred Delivered Product	Packaged dice	Mapped wafers, probed wafers, scribed dice, packaged dice.	DIPs, LLCs, flat paks
Test Program Generation	Yes	Yes	Yes
Production Test	Functional; parametric; burn-in	Functional, parametric, burn-in, thermal shock, environmental, MIL linear.	Functional, parametric, burn-in, thermal shock, environmental, MIL.
Electrical Test Systems Available		Sentry VII, LTX-DS80	In-house designed
Comments	Chip debugging with portable micro prober on customer's premises.		Several commercial programmers available.

CUSTOM/SEMICUSTOM (Cont)

Manufacturer FOR DETAILED DATA SEE:	Monosil (Citel) (Page 4628)	Motorola (Page 4796)	Murray Consulting
Customized Standard Circuits	Digital	Digital	Linear, Digital, Combined Linear/Digital
Gate Array	3μ silicon-gate CMOS CMOS	MCA 600 ECL/1200 ECL; MCA 500 ALS/1300 ALS	CMOS
Chip Density Range (equiv. gates)	200 to 3200	652/1192; 533/1280	1 to 100
Cell Library	Yes	120 functions; 80 functions	BiMOS
Design Kit Available		Manuals	No
Full Custom Circuits Digital	Silicon- or metal-gate CMOS, silicon-gate NMOS, bipolar	NMOS, CMOS, ECL	Silicon-gate CMOS; TTL
Linear	Bipolar	No	
Combined Digital/Linear	CMOS	No	Silicon-gate CMOS; bipolar
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Logic diagram; circuit diagram; functional specification; breadboard, data-base tapes, PG tapes, mask sets, customer-owned tooling.	CAD interface, logic simulation, circuit documentation.	Breadboard; circuit diagram; functional specification.
Design Aids	Logic simulation, design rule checks, net-list verification.	Computer aided design package	Design rule checks
Production	In-house	High volume capability	In-house, procured
Preferred Delivered Product	Packaged units; will supply wafers or dice.	Choice of packages	Packaged dice; PC-mounted packaged units.
Test Program Generation	Yes	Yes	No
Production Test	Functional, parametric	100% AC and DC and functional	Functional
Electrical Test Systems Available	Sentry VII	Fairchild Sentry VIII and Series 21	
Comments	Complete custom capability	ECL 10K compatible, ECL 10 KH compatible, TTL-LS compatible, remote dseign centers.	Develop photo-integrated circuits: CMOS, MOS, bipolar, BiMOS.

CUSTOM/SEMICUSTOM (Cont)

Manufacturer	NEC Electronics	NCM Corporation	Nitron
FOR DETAILED DATA SEE:	(Page 4799)		
Customized Standard Circuits	Digital, Linear, Combined Digital/Linear	Linear, digital, combination	Digital
Gate Array	CMOS, ECL, TTL-LS	CMOS (si-gate, metal-gate) bipolar	Metal-gate CMOS
Chip Density Range (equiv. gates)	To 11,000	1000 (max.)	50 to 600
Cell Library	Yes	YES	Macro library of common functions (overlays)
Design Kit Available	Yes	No	Yes
Full Custom Circuits Digital		CMOS (si-gate, metal-gate) bipolar	Metal-gate PMOS, CMOS
Linear		CMOS (si-gate, metal-gate) bipolar	Metal-gate PMOS, CMOS
Combined Digital/Linear		CMOS (si-gate, metal-gate); bipolar	Metal-gate PMOS, CMOS
Provide Design Assistance		Yes	Yes
Acceptable Customer Input (in order of preference)		Functional specs, logic diagram, circuit diagram, breadboard, test vectors, customer-owned tooling, known good devices.	Customer-owned tooling with debugged test program; logic diagram, electrical specification with test vectors.
Design Aids		Logic simulation, breadboarding, design rule check, cell library.	All available
Production		Procured	In-house
Preferred Delivered Product		Packaged-units, dice, probed wafers, pc assemblies.	Packaged dice
Test Program Generation		Yes	Yes
Production Test		Functional, parametric, burn-in, thermal cycle.	All commercial and full military
Electrical Test Systems Available		In-house built. μc – controlled test systems.	Sentry
Comments			

CUSTOM/SEMICUSTOM (Cont)

Manufacturer FOR DETAILED DATA SEE:	National	Pico Design	Plessey Semiconductors (Page 4815)
Customized Standard Circuits	Digital	No	Digital, Linear, Combined Digital/Linear
Gate Array	Silicon-gate CMOS	No	Bipolar, ECL and CMOS
Chip Density Range (equiv. gates)	To 2400	10,000	ECL to 1200, CMOS to 10440
Cell Library	Yes	Yes	Yes
Design Kit Available	Yes	No	Yes
Full Custom Circuits Digital	Metal-gate PMOS, metal-or Silicon-gate NMOS, high voltage metal-gate CMOS, low voltage metal- and silicon-gate CMOS, metal double poly silicon-gate CMOS, dual layer XMOS, oxide isolated and Schottky devices, I^2L.	Silicon- or metal-gate PMOS, NMOS, CMOS, other MOS.	PMOS, NMOS, CMOS; I^2L, ECL
Linear	Same as above	No	Bipolar, CMOS
Combined Digital/Linear	Same as above	No	I^2L, ECL Bipolar, CMOS
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Any	Logic diagram, circuit schematic, breadboard, functional specification.	Logic diagram, breadboard, customer-owned tooling, data base tape.
Design Aids	Computer aided circuit analysis, logic and systems simulation, digitizing cell plotting and editing, design rule check, pattern generation, photolithography.	Logic and circuit simulation; design rule checks; CALMA GDS II.	Design rule check, testability analyzer, fault analyzer, auto-placement, auto-router, logic simulator.
Production	In-house	Procured	
Preferred Delivered Product	Packaged dice	All except PC-mounted packaged units.	Packaged tested dice, scribed dice, probed wafers, mapped wafers.
Test Program Generation	Yes	Yes	Yes
Production Test	All except linear	Functional; parametric	Functional, parametric, burn-in, MIL-STD-883.
Electrical Test Systems Available	Century VI and VII, Sentinel, Teradyne, Megatest.	Fairchild, Sentry VII and Series 20	Teradyne J274, Fairchild, Sentry special in-house.
Comments			

CUSTOM/SEMICUSTOM (Cont)

Manufacturer FOR DETAILED DATA SEE:	Polycore Electronics Inc.	Precision Monolithics, Inc.	Raytheon (Page 4822)
Customized Standard Circuits		Linear	Linear, Digital
Gate Array		From customer-owned tooling	Bipolar digital ISL
Chip Density Range (equiv. gates)			800 to 2400
Cell Library		Standard parts available in chip form	Yes, TTL
Design Kit Available		Kit parts	Yes
Full Custom Circuits Digital	CMOS metal-gate	TTL, LSTTL, ISL, I^2L, ECL, ISO/CMOS-SiGate	Consult factory (bipolar)
Linear	Bipolar	20, 40, 60V supply voltage	Bipolar
Combined Digital/Linear	Power Interface/Driver Circuits	I^2L, ECL, TTL, LSTTL	Consult factory (bipolar)
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Schematics, Performance specs.	Customer-owned tooling (pattern-generator-tape, composite drawing), known good device.	TEGAS net list, circuit schematics, data base program.
Design Aids	Breadboard simulation	Kit parts	Evaluation devices, design source manual, factory tutorial.
Production	In-house wafer fabrication procurred assembly	In-house 3″, 4″ lines	Yes
Preferred Delivered Product	Packaged units, dice	Mapped wafers, probed wafers, packaged units.	
Test Program Generation	Yes	Yes	Yes
Production Test	Functional, parametric, burn-in; thermal shock, environmental, MIL.	Functional, parametric, burn-in, thermal shock, environmental, MIL, linear.	Yes
Electrical Test Systems Available	MCT 200	LTX, F-5000	Sentry 7, Sentry Series 21
Comments	Also provide silicon foundry service in linear, I^2L and CMOS metal gate.	Ion implantation; dual layer metallization; nitride passivation; thin film resistors; MIL 35810 qualified.	

CUSTOM/SEMICUSTOM (cont)

Manufacturer	RCA	Semi Processes, Inc.	Si Fab
FOR DETAILED DATA SEE:	(Page 4824)	(Page 4826)	(Page 4827)
Customized Standard Circuits	Digital	Digital	Digital
Gate Array	Silicon-gate, metal-gate CMOS	Silicon-gate CMOS	Silicon- and metal-gate
Chip Density Range (equiv. gates)	168 to 840	48 to 1400	
Cell Library	CMOS	Yes	Yes
Design Kit Available	No	Yes	
Full Custom Circuits Digital	Silicon-gate, metal-gate CMOS		CMOS
Linear			CMOS
Combined Digital/Linear			CMOS
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Logic diagram, circuit diagram, breadboard test vectors, customer-owned tooling (pattern-generator tape, composite drawing), known good device.	Logic diagram; circuit diagram; test vectors; custom-owned tooling; breadboard; functional specification.	
Design Aids	Logic simulation; breadboard assistance; design rule checks.	Design rule checks, logic simulation, circuit simulation	
Production	In-house	In-house	In-house
Preferred Delivered Product	Probed wafers, scribed dice, packaged dice.	As requested	
Test Program Generation	Yes	Yes	
Production Test	Functional, parametric, burn-in	Functional; parametric; burn-in, ac	
Electrical Test Systems Available	Teradyne; Century 7; J273, J193, J283, J325; LTX; Tester; MTS 77.	Sentry, Genrad, Pragmatic	
Comments		Breadboard assistance using SPI's proprietary 74HC low power CMOS logic IC's.	

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CUSTOM/SEMICUSTOM

CUSTOM/SEMICUSTOM (cont)

Manufacturer FOR DETAILED DATA SEE:	Signetics (Page 4829)	Signetics (Page 4829)	Silicon Systems (Page 4872)
Customized Standard Circuits	Digital	Digital	
Gate Array	Silicon-gate CMOS	ECL 100K and 10 K compatibility (0.5 ns)	
Chip Density Range (equiv. gates)	330 to 1100 1250 to 5000 (mid '84)	500-800	
Cell Library	Silicon-gate CMOS, TTL and LSTTL	Macrocell Library	
Design Kit Available	Yes	Yes	
Full Custom Circuits Digital	No*		Silicon- or metal-gate PMOS, NMOS, CMOS, bipolar, TTL, STL, SRTL, LSTTL, ECL, I²L
Linear	No		Silicon- or metal-gate PMOS, NMOS, CMOS, bipolar
Combined Digital/Linear	TBD		Silicon- or metal-gate CMOS, bipolar, TTL, SRTL, I²L, STL
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Logic diagram, timing diagram, and simulation output; CAD output.	Calma tapes plus simulation results; Mylar symbolic representation plus simulation results.	Functional specification, logic diagram, circuit diagram, breadboard, test vectors.
Design Aids	Schematic capture, complete simulation, auto place, auto route, auto test generation.	Logic simulation, CAD design rule checks, layout to simulation check, test generation, design manual, training sessions.	Breadboards, logic and circuit simulation, design-rule checks, test-program development.
Production	In-house	In-house	Procured and in-house
Preferred Delivered Product	Packaged units	Packaged units	Packaged units and tested dice
Test Program Generation	Yes	Yes	Yes
Production Test	Functional, parametric, burn-in	Functional, parametric and ac	Automatic testers for analog and digital devices.
Electrical Test Systems Available	Sentry VII, VIII, and 21	Tektronix (25 MHz)	
Comments	* Standard cells from 200 to 2000 gates.		

CUSTOM/SEMICUSTOM (cont)

Manufacturer FOR DETAILED DATA SEE:	Siltronics	Solid State Scientific	Sprague Electric Co.
Customized Standard Circuits			Linear
Gate Array			
Chip Density Range (equiv. gates)			
Cell Library			
Design Kit Available			No
Full Custom Circuits Digital	TTL, STTL, LSTTL, I^2L, ECL, other bipolar	Silicon-gate CMOS, NMOS metal-gate CMOS	
Linear	TTL, STTL, LSTTL, I^2L, ECL, other bipolar	Silicon-gate CMOS, NMOS	
Combined Digital/Linear	TTL, STTL, LSTTL, I^2L, ECL, other bipolar	Silicon-gate NMOS, CMOS	
Provide Design Assistance		Yes	
Acceptable Customer Input (in order of preference)		Minimum of functional diagram; breadboard; pattern generator tape or database tape.	Composite drawing
Design Aids	Breadboard assistance; design-rule checks.	Logic simulator assistance, breadboard assistance, design rule checks.	
Production	Breadboard wafers; in-house assembly.	In-house	In-house
Preferred Delivered Product	Fully tested assembled package.	No preference	Wafers, dice, packaged devices
Test Program Generation	Yes	Yes	
Production Test	Customized to suit	Full screening available including burn-in and full environmental screening.	
Electrical Test Systems Available	J259-style equipment; custom testers.	Sentry VII, Sentinal, Teradyne	
Comments	Specialize in mixed analog/ digital bipolar. Die sizes to 40,000 mil².	Capabilities include: design, layout, CAP, mask shop, wafer fabrication assembly, and test.	ULN-2350C and ULN-2351C basic unmetallized circuit.

CUSTOM/SEMICUSTOM (cont)

Manufacturer FOR DETAILED DATA SEE:	Standard Microsystems	Sunshine Semiconductor	Supertex
Customized Standard Circuits	Digital, Combined Digital/Linear	Digital, Combined Linear/Digital	Linear, Digital
Gate Array			Silicon- or metal-gate CMOS
Chip Density Range (equiv. gates)			50 to 2000
Cell Library	Silicon-gate NMOS, CMOS	Si-gate CMOS	
Design Kit Available	No		No
Full Custom Circuits Digital	Metal-gate PMOS; silicon-gate NMOS, CMOS	Silicon-gate CMOS, metal-gate CMOS, nonvolatile CMOS	Silicon- or metal-gate CMOS
Linear			Silicon- or metal-gate CMOS
Combined Digital/Linear	Silicon-gate NMOS, CMOS	Metal Gate CMOS	Silicon- or metal-gate CMOS
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Functional specification, logic diagram, Calma database tape, other.	Product description, block diagram with specifications, logic diagram.	Breadboard with functional specification and logic diagram; customer-owned tooling.
Design Aids	Logic simulation; breadboard design rule checks, electrical rule checks, transient analysis	Breadboard, circuit and logic simulation, DRC, graphics, NCC	Logic simulation; breadboard assistance.
Production	In-house	Procured	In-house
Preferred Delivered Product	Packaged devices preferred. All others available.	Packaged dice, bare dice, design and layout	Probed wafers; inspected dice; packaged dice.
Test Program Generation	Yes	Yes	Yes
Production Test	Full testing and screening, including burn-in.	Procured	Functional; parametric; burn-in; environmental.
Electrical Test Systems Available	Megatest Q8000; SMC; dedicated testers, Fairchild, Sentry and Sentinal.		Teradyne J193; GenRad 2225
Comments	Specialize in digital MOS/LSI and VLSI; will also customize by modifying MOS/LSI standard parts. Second sources available.	Services include product and specification finalization, logic and circuit design, layout, test definition.	

CUSTOM/SEMICUSTOM (cont)

Manufacturer FOR DETAILED DATA SEE:	Synertek (Page 4873)	Telmos (Page 4877)	Telmos (Page 4877)
Customized Standard Circuits		Digital	Digital/Linear
Gate Array		Silicon-gate and metal-gate CMOS	Silicon-gate analog/digital Silicon-gate high voltage
Chip Density Range (equiv. gates)		50 to 1260 gates	
Cell Library		Silicon-gate and metal-gate CMOS digital	100 to 1200 gates
Design Kit Available	Yes		Yes
Full Custom Circuits Digital	Silicon-gate CMOS, NMOS	Custom designs are preferred	
Linear	Same as above		
Combined Digital/Linear	Same as above	Silicon-gate analog/digital	Silicon-gate analog/digital
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Functional specification, customer owned tooling, logic diagram, circuit diagram, breadboard.	Schematic I/O requirements, functional spec. breadboard, test vectors, customer owned tooling, known good device.	Schematic I/O requirements, functional specs, breadboard test vectors, customer owned tooling, known good device.
Design Aids	Logic simulation breadboard assistance, continuity check, design rule check.	Aspec, Spice IIG — transient analysis logic, Tegas IV — logic simulation, Sentry VII — test.	Aspec, Spice 11G, transient analysis logic; Tegas IV, logic simulation.
Production	In-house	In-house wafer fab facility	In-house wafer fabrication
Preferred Delivered Product	Packaged dice, scribed dice	Wafer, dual in line packages, chip carriers.	Wafer, dual-in-line packages, chip carriers.
Test Program Generation	Yes	Yes	Yes
Production Test	All	Functional, parametric burn-in thermal shock, environmental.	Functional, parametric burn-in thermal shock, environmetal
Electrical Test Systems Available	Century, Xincom		Sentry VII
Comments	Customer interface ranges from "black box" specification to COT. Company will work with customer engineers to develop in-house capability for designing future COT.		

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CUSTOM/SEMICUSTOM

CUSTOM/SEMICUSTOM (cont)

Manufacturer FOR DETAILED DATA SEE:	Texas Instruments (Page 4878)	TLSI, Inc.	Torric Corporation
Customized Standard Circuits	Digital		Linear, Digital, Combined Digital/Linear
Gate Array	LPS, silicon-gate CMOS, STL	Silicon-gate CMOS	Silicon or metal-gate CMOS, Linear Bipolar, Digital ECL
Chip Density Range (equiv. gates)	540 to 4000	300 + 2500	300 — 2500
Cell Library	Software functions — bipolar CMOS MACROS	Si-gate CMOS, NMOS	Silicon-gate CMOS
Design Kit Available	Yes	No	Yes
Full Custom Circuits Digital	LPS, STL, I²L, CMOS, NMOS	CMOS, NMOS, PMOS	Silicon- or metal-gate PMOS, NMOS, CMOS, TTL, STTL, I²L
Linear	Yes	CMOS, NMOS, PMOS	Silicon- or metal-gate CMOS; TTL, STTL
Combined Digital/Linear	Yes	CMOS, NMOS, PMOS	Silicon- or metal-gate CMOS; TTL, STTL
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Logic diagram, PG tape, HDL/TDL design input, functional specification.	Specification, logic diagram schematic, breadboard COT	Functional specification; logic diagram; circuit diagram; breadboard; known good device; customer owned tooling; test vectors.
Design Aids	Simulation, testability analysis, test grading, load checker. Texas Instruments logic array design utility — TILADS.	Custom cell library, logic simulation, CAD, CAE, Design Rule checks.	Logic simulation; breadboard assistance; design rule checks; graphics CAD.
Production	In-house	Procured	Procured
Preferred Delivered Product	Packaged devices	Package die, dice	Packaged dice, printed-card-mounted packaged units.
Test Program Generation	Yes	Yes	Yes
Production Test	Functional, parametric, burn-in, MIL.	Functional, parametric, burn-in, linear	No
Electrical Test Systems Available	Sentry 20, in-house	LTX, HP, Gen Rad, dedicated Multiple production sources;	
Comments		no minimum production requirements.	

CUSTOM/SEMICUSTOM (cont)

Manufacturer FOR DETAILED DATA SEE:	Trans-Data	Universal Semiconductor (Page 4930)	VLSI Design Associates
Customized Standard Circuits		Digital	Digital/Analog
Gate Array		Silicon-gate ISO-CMOS	
Chip Density Range (equiv. gates)		180 to 2400	
Cell Library		Silicon-gate ISO-CMOS	Silicon-gate CMOS, Digital and Analog
Design Kit Available		Yes	No
Full Custom Circuits Digital	Silicon-gate NMOS and CMOS	Silicon-gate ISO-CMOS	Silicon-gate CMOS and NMOS; logic and memory; nonvolatile memory.
Linear	Silicon-gate — CMOS	Same as above	Silicon-gate CMOS and NMOS; CCD; Switched capacitor filters.
Combined Digital/Linear	Silicon-gate — CMOS	Same as above	
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Functional specs, logic diagram, circuit diagram, known good device, customer tooling.	Logic reconfigured at GATE/FF Level. Logic diagram, PG tapes, masks.	Logic diagram, circuit diagram, functional specification, breadboard.
Design Aids		Logic simulation, breadboard assistance, design rule checks. Auto test generation; auto place/route; logic to layout verification.	In-house: Calma GDS II and VAX11/780.
Production	Procured	In-house	Procured
Preferred Delivered Product	Packaged dice (prototype quantities), probed wafers.	Package parts, dice probed wafers.	As requested
Test Program Generation	Yes	Yes	Yes
Production Test		Functional, parametric, burn-in, thermal shock, environmental, MIL.	Functional, parametric
Electrical Test Systems Available	Functional, Parametric, Burn-in, Thermal Shock, environmental MIL.	Micro Manipulator, Sentry II, VI, VII, Sentry System 20, pragmatic functional tester. Fairchild Series 10.	
Comments	Provide assistance to customers who will utilize gate arrays manufactured by others.	With smaller random logic circuits, prefer to start with a gate array and convert to full custom when manufacturing volumes justify the conversion.	Independent design center; multiple sources, design aids.

CUSTOM/SEMICUSTOM (cont)

Manufacturer FOR DETAILED DATA SEE:	VLSI Technology (Page 4931)	Western Digital	ZyMOS
Customized Standard Circuits		Digital	Digital, combined digital/linear
Gate Array		Up to 1000 gates, Silicon-gate NMOS	Up to 2500 gates, metal-gate CMOS 3000 gates, silicon-gate CMOS 4000 gates, NMOS.
Chip Density Range (equiv. gates)			Metal-gate CMOS, silicon-gate CMOS, NMOS
Cell Library		Yes	Yes
Design Kit Available	NMOS, HMOS, CMOS		Metal-gate CMOS, silicon-gate CMOS, NMOS
Full Custom Circuits Digital			
Linear	NMOS, CMOS		CMOS
Combined Digital/Linear	NMOS, CMOS		CMOS
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Functional specification logic diagram, breadboard, customer-owned tooling, data base tape, PG tape, mask.	Functional specification logic system	Logic input through ZyP CAD system, logic diagram, functional specification, customer-owned tooling.
Design Aids	PRISM VLSI design system, including high-level design language, circuit extraction logic and circuit simulation, design rule checks, plotting, STIX.	Logic simulation, design rule checks, test program development.	Circuit simulation, logic simulation, test program generation, artwork generation all linked to common data base, design rule checks, breadboard assistance.
Production	In-house	In-house	In-house
Preferred Delivered Product	Packaged dice preferred. Any on request.	Packaged units and tested dice	Packaged dice preferred, any on request
Test Program Generation	Yes	Yes	Yes
Production Test	Functional, parametric, burn-in, thermal shock, environmental, MIL.	Functional, burn-in	Functional, parametric
Electrical Test Systems Available	Sentry 20/120, Accutest		Sentry, VII, Lomac
Comments	Multiple sourcing compatibility, foundry services, training and CAD aids to support User-Designed VLSI and Mead-Designed VLSI.	Uncommitted logic arrays, 20 pin DIP, 130 prefabricated logic elements or 28/40 pin DIP, 400 prefabricated logic elements.	ZyP CAD system — logic level design at customer's facility, CMOS and NMOS silicon level simulation.

CUSTOM/SEMICUSTOM-Gate Arrays

Internal Gate Delay ns (max)	Toggle Frequency MHz	Type	No. Equiv. 2-Input Gates	Input/Output Cells: Input Only	Output Only	Uncommitted	Input/Output Compatibility: CMOS	TTL-LS	TTL	ECL	Supply Voltage V	Comments	Device	Source
Gate Arrays														
—	15		1200			80	x	x	x		4 to 10		H1084	† Hughes
0.5	300	ECL	2800		(68)	120				x	−4.5	Macrocell array	**MCA2500ECL**	**Motorola (4796)**
					(68)	120				x	−4.5	Macrocell array	MCA2500ECL	National
		ECL-ALS	1456	Dir.	49	99		x	x	x	−4.5	1280-bit RAM on-chip	MCA1500M	National
	450	ECL	638	30		28		x	x	x	−4.5 to -5.2		**ACE600**	**Signetics (4858)**
			878	42		32		x	x	x	−4.5 to -5.2		**ACE900**	**Signetics (4858)**
			1000			96		x	x	x	−4.5 to -5.2	320-bit RAM on-chip	**ACE1320M**	**Signetics (4860)**
			1414			96		x	x	x	−4.5 to -5.2		**ACE1400**	**Signetics (4860)**
			2204			128		x	x	x	−4.5 to -5.2		**ACE2200**	**Signetics (4860)**
	500	ECL	20			21				x	−4.5 to -5.7	20 equiv. 3-input gates	**FGE0020**	**Fairchild (4634)**
	1000	ECL	500			72		x	x	x	−4.2 to -5.7 or 5	500 equiv. 3-input gates	**FGE0500**	**Fairchild (4634)**
			1000			86		x	x	x	−4.2 to -5.7 or 5	1000 equiv. 3-input gates	FGE1000	Fairchild
			2000			126		x	x	x	−4.2 to -5.7 or 5	2000 equiv. 3-input gates	**FGE2000**	**Fairchild (4634)**
0.55	400	ECL	75			24				x	−5.2		SCD1000	Plessey
		ECL	300	36		20				x	−5.2		SCD2000H	Plessey
		ECL	600			54				x	−5.2		**SCD4000**	**Plessey (4815)**
0.75	700	ECL	300	28		28				x	−4.5		**µPB6301**	**NEC (4799)**
1.05	500	ECL	1200	40		48				x	−4.5		**µPB6310**	**NEC (4799)**
			2000	60		48				x	−4.5		**µPB6320**	**NEC (4799)**
1.2	85	TTL-AS	1500			88		x	x		5, 2		**HGA-B01500**	**Harris (4741)**
			3000			120		x	x		5, 2		**HGA-B02500**	**Harris (4741)**
	160	ECL	625		(18)	60				x	−5.2	Macrocell array	MCA600	AMD
					(18)	60				x	−5.2	Macrocell array	**LCA600**	**LSILogic (4762)**
					(18)	60				x	−5.2	Macrocell array	**MCA600ECL**	**Motorola (4796)**
					(18)	60				x	−5.2	Macrocell array	MCA600ECL	National
			1192		(26)	60				x	−5.2	Macrocell array	MCA1200	AMD
					(26)	60				x	−5.2	Macrocell array	**LCA1200**	**LSILogic (4762)**
					(26)	60				x	−5.2	Macrocell array	**MCA1200ECL**	**Motorola (4796)**
					(26)	60				x	−5.2	Macrocell array	MCA1200ECL	National
	200	ECL	250	8		26			x	x	−5.2/5	Mixed TTL/ECL outputs	Q720	† AppMicroCir
			500	28		28			x	x	−5.2/5	Mixed TTL/ECL outputs	Q710	† AppMicroCir
			1000	38		38			x	x	−5.2/5	Mixed TTL/ECL outputs	Q700	† AppMicroCir
			1500	46		38			x	x	−5.2/5	Mixed TTL/ECL outputs	Q750	† AppMicroCir
1.4	160	ECL	2800			120		x	x		5	Macrocell array	**MCA2800ALS**	**Motorola (4797)**
						120		x	x		5	Macrocell array	MCA2800ALS	National
1.5	75	TTL-AS	1500			88		x	x		5, 2		HGABA01500	† Harris
	85	TTL-AS	3000			120		x	x		5, 2		HGABA03000	† Harris
	200	ECL	250	8		26			x	x	−5.2/5	Mixed TTL/ECL outputs	Q720	† AppMicroCir
			500	28		28			x	x	−5.2/5	Mixed TTL/ECL outputs	Q710	† AppMicroCir
			1000	38		38			x	x	−5.2/5	Mixed TTL/ECL outputs	Q700	† AppMicroCir
			1500	46		38			x	x	−5.2/5	Mixed TTL/ECL outputs	Q750	† AppMicroCir
	250	ECL	300	36		20				x	−5.2		SCD2000M	Plessey
1.5 *	200	TTL-LS	2000			112		x	x		5, 2.3	2108 equiv. 3-input gates	**B2000**	**Fujitsu (4638)**
1.6	50	CMOS	1500			76	x	x	x		3 to 10		BC210	† Barvon
			2500			108	x	x	x		3 to 10		BC225	† Barvon
1.8	40	CMOS	968			54	x	x	x		3 to 6		**LL7090**	**† LSILogic (4762)**
			1430			68	x	x	x		3 to 6		**LL7140**	**† LSILogic (4762)**
			2224			86	x	x	x		3 to 6		**LL7220**	**† LSILogic (4762)**
			3268			110	x	x	x		3 to 6		**LL7320**	**† LSILogic (4762)**
			4368			122	x	x	x		3 to 6		**LL7430**	**† LSILogic (4762)**
			6425			160	x	x	x		3 to 6		**LL7640**	**† LSILogic (4762)**

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

CUSTOM/SEMICUSTOM–Gate Arrays (Cont'd)

Internal Gate Delay ns (max)	Toggle Frequency MHz	Type	No. Equiv. 2-Input Gates	Input/Output Cells: Input Only	Output Only	Un-committed	Input/Output Compatibility: CMOS	TTL-LS	TTL	ECL	Supply Voltage V	Comments	Device	Source	
Gate Arrays															**(Cont'd)**
1.8	40	CMOS													(Cont'd)
			8456			180	x	x	x		3 to 6		**LL7840**	**† LSILogic**	**(4762)**
			10013			180	x	x	x		3 to 6		**LL71000**	**† LSILogic**	**(4762)**
	45	CMOS	500			40	x	x	x		2 to 9		IGD10500	† Intersil	
			1000			68	x	x	x		2 to 9		IGD11000	† Intersil	
			1500			84	x	x	x		2 to 9		IGD11500	† Intersil	
			2600			100	x	x	x		2 to 9		IGD12600	† Intersil	
			4500			140	x	x	x		2 to 9		IGD14500	† Intersil	
			6000			180	x	x	x		2 to 9		IGD16000	† Intersil	
1.9 *	—	TTL-LS	360			48		x	x		5	360 equiv. 3-input gates	**B350**	**Fujitsu**	**(4637)**
			1120			88		x	x		5	1120 equiv. 3-input gates	**B1100**	**Fujitsu**	**(4637)**
2.0	50	CMOS	2500	39		84	x	x			5		**FGC2400**	**† Fairchild**	**(4634)**
			3925	31		90	x	x			5		**FGC4000**	**† Fairchild**	**(4634)**
			6006	41		120	x	x			5		**FGC6000**	**† Fairchild**	**(4634)**
2.1	110	CMOS	1260	17		42	x	x	x		4 to 6		SCX6212	National	
			2385	55		56	x	x	x		4 to 6		SCX6224	National	
			2430	12		76	x	x	x		4 to 6		SCX6225	National	
			4860	53		54	x	x	x		4 to 6		SCX6248	National	
			6260	66		88	x	x	x		4 to 6		SCX6260	National	
2.2	160	TTL-AS	1280	(88)	(44)	88		x		x	5, 2	Mixed TTL/ECL compatible	TAT010	† TI	
				(88)	(44)	88				x	−5.2		TAT010	† TI	
			2420	(120)	(60)	120		x		x	5, 2	Mixed TTL/ECL compatible	TAT020	† TI	
				(120)	(60)	120				x	−5.2		TAT020	† TI	
2.2 *	—	TTL-LS	500			62		x	x		5	512 equiv. 3-input gates	**B500**	**Fujitsu**	**(4637)**
2.4	50	CMOS	360			36	x	x	x		3 to 6		IS03A	† Siliconix	
						36	x	x	x		3 to 6		**IS03A**	**† Universal**	**(4930)**
			540			48	x	x	x		3 to 6		IS03B	† Siliconix	
						48	x	x	x		3 to 6		**IS03B**	**† Universal**	**(4930)**
			720			54	x	x	x		3 to 6		IS03C	† Siliconix	
						54	x	x	x		3 to 6		**IS03C**	**† Universal**	**(4930)**
			960			62	x	x	x		3 to 6		IS03D	† Siliconix	
						62	x	x	x		3 to 6		**IS03D**	**† Universal**	**(4930)**
			1200			68	x	x	x		3 to 6		IS03E	† Siliconix	
						68	x	x	x		3 to 6		**IS03E**	**† Universal**	**(4930)**
			1500			70	x	x	x		3 to 6		IS03F	† Siliconix	
						70	x	x	x		3 to 6		**IS03F**	**† Universal**	**(4930)**
			1800			82	x	x	x		3 to 6		IS03G	† Siliconix	
						82	x	x	x		3 to 6		**IS03G**	**† Universal**	**(4930)**
			2400			82	x	x	x		3 to 6		IS03H	† Siliconix	
						82	x	x	x		3 to 6		**IS03H**	**† Universal**	**(4930)**
2.5	200	ECL	300	36		20				x	−5.2		SCD2000L	† Plessey	
3.0	—	STL	560			61		x	x				**STL700**	**† TI**	**(538)**
	25	CMOS	228			28	x	x	x		4 to 6		**MA0200**	**† Citel**	**(4628)**
						28	x	x	x		4 to 6		MA0200	Matra	
			380			36	x	x	x		4 to 6		**MA0400**	**† Citel**	**(4628)**
						36	x	x	x		4 to 6		MA0400	Matra	
			754			50	x	x	x		4 to 6		**MA0800**	**† Citel**	**(4628)**
						50	x	x	x		4 to 6		MA0800	Matra	
			1020			52	x	x	x		2.5 to 5.5		**GA1000**	**† AMI**	**(4619)**
			1139			62	x	x	x		4 to 6		**MA1200**	**† Citel**	**(4628)**
						62	x	x	x		4 to 6		MA1200	Matra	
			1260	1		75	x	x	x		3 to 7		HCS12000	† CalDevices	
			1500			64	x	x	x		2.5 to 5.5		**GA1500**	**† AMI**	**(4619)**
			1782	1		89	x	x	x		3 to 7		HCS17800	† CalDevices	
			2025			74	x	x	x		2.5 to 5.5		**GA2000**	**† AMI**	**(4619)**
			2508			84	x	x	x		2.5 to 5.5		**GA2500**	**† AMI**	**(4619)**
															(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

Master Selection Guide

CUSTOM/SEMICUSTOM

CUSTOM/SEMICUSTOM-Gate Arrays (Cont'd)

Internal Gate Delay ns (max)	Toggle Frequency MHz	Type	No. Equiv. 2-Input Gates	Input/Output Cells: Input Only	Output Only	Uncommitted	Input/Output Compatibility: CMOS	TTL-LS	TTL	ECL	Supply Voltage V	Comments	Device	Source
Gate Arrays														**(Cont'd)**
3.0														(Cont'd)
	30	CMOS	1000			62	x	x	x		2.5 to 5.5		**GA1000D**	**† AMI (4619,4619)**
			2070			84	x	x	x		2.5 to 5.5		**GA2000D**	**† AMI (4619,4619)**
			3080			102	x	x	x		2.5 to 5.5		**GA3000D**	**† AMI (4619)**
			4012			120	x	x	x		2.5 to 5.5		**GA4000D**	**† AMI (4619)**
			4995			134	x	x	x		2.5 to 5.5		**GA5000D**	**† AMI (4619)**
	35	CMOS	400			40	x	x	x		3 to 8		SGA04	† MicroTech
			600			48	x	x	x		3 to 8		SGA06	† MicroTech
			1000			58	x	x	x		3 to 8		SGA10	† MicroTech
			1500			72	x	x	x		3 to 8		SGA15	† MicroTech
			2000			82	x	x	x		3 to 8		SGA20	† MicroTech
			3000			110	x	x	x		3 to 8		SGA30	† MicroTech
			4000			120	x	x	x		3 to 8		SGA40	† MicroTech
			5000			138	x	x	x		3 to 8		SGA50	† MicroTech
			6000			168	x	x	x		3 to 8		SGA60	† MicroTech
	50	ECL	533	26	27			x	x		5	Macrocell array	**MCA500ALS**	**Motorola (4797)**
				26	27			x	x		5	Macrocell array	MCA400ALS	National
			1280	40	40			x	x		5	Macrocell array	**MCA1300ALS**	**Motorola (4797)**
				40	40			x	x		5	Macrocell array	MCA1300ALS	National
	85	CMOS	648			56	x	x	x		5		**HGA-C00600**	**† Harris (4740)**
			1296			80	x	x	x		5		**HGA-C01200**	**† Harris (4740)**
			2520			102	x	x	x		5		**HGA-C02500**	**† Harris (4740)**
	100	CMOS	6000			120	x	x	x		3 to 7		CLA4000	Plessey
	125	TTL	1000			76		x	x		5,2.5		**FGT0750**	**Fairchild (4634)**
	130	ECL	300	36		20				x	−5.2		SCD2000L	† Plessey
3.2	55	ISL	836			48		x	x		5,1.8	Gate delay 2.3 ns max with active pull-up	**CGA8L48**	**† Raytheon (508,4822)**
			1196			60		x	x		5,1.8	Gate delay 2.3 ns max with active pull-up	**CGA12L60**	**† Raytheon (508,4822)**
			1620			68		x	x		5,1.8	Gate delay 2.3 ns max with active pull-up	**CGA16L68**	**† Raytheon (508,4822)**
			1984			76		x	x		5,1.8	Gate delay 2.3 ns max with active pull-up	**CGA20L76**	**† Raytheon (508,4822)**
			2376			84		x	x		5,1.8	Gate delay 2.3 ns max with active pull-up	**CGA24L84**	**† Raytheon (508,4822)**
3.5	20	CMOS	500			44	x	x	x		4 to 6		50500B	GTEMicro
			1000			54	x	x	x		4 to 6		51000B	GTEMicro
			1500			68	x	x	x		4 to 6		51500B	GTEMicro
			2000			78	x	x	x		4 to 6		52000B	GTEMicro
	50	CMOS	150			32	x	x	x		3 to 7		AT-HSD-150	† ArrayTech
			250	18	12	32	x	x	x		3 to 7		AT-HSD-250	† ArrayTech
			350			36	x	x	x		3 to 7		AT-HSD-350	† ArrayTech
			550			48	x	x	x		3 to 7		AT-HSD-550	† ArrayTech
			750			54	x	x	x		3 to 7		AT-HSD-750	† ArrayTech
			1000			62	x	x	x		3 to 7		AT-HSD-1000	† ArrayTech
			1200			68	x	x	x		3 to 7		AT-HSD-1200	† ArrayTech
			1500			76	x	x	x		3 to 7		AT-HSD-1500	† ArrayTech
			1800			82	x	x	x		3 to 7		AT-HSD-1800	† ArrayTech
		ISL	836			48		x	x		5,1.8	Gate delay 2.3 ns max with active pull-up	CGA8L48	† Raytheon
			1196			60		x	x		5,1.8	Gate delay 2.3 ns max with active pull-up	CGA12L60	† Raytheon
			1620			68		x	x		5,1.8	Gate delay 2.3 ns max with active pull-up	CGA16L68	† Raytheon

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

CUSTOM/SEMICUSTOM–Gate Arrays (Cont'd)

Internal Gate Delay ns (max)	Toggle Frequency MHz	Type	No. Equiv. 2-Input Gates	Input/Output Cells: Input Only	Output Only	Uncommitted	Input/Output Compatibility: CMOS	TTL-LS	TTL	ECL	Supply Voltage V	Comments	Device	Source
Gate Arrays													**(Cont'd)**	
														(Cont'd)
3.5	50	ISL	1984			76		x	x		5,1.8	Gate delay 2.3 ns max with active pull-up	CGA20L76	† Raytheon
			2376			84		x	x		5,1.8	Gate delay 2.3 ns max with active pull-up	CGA24L84	† Raytheon
	66	CMOS	648			37	x	x	x		4 to 6		SCX6306	National
			1260	17		42	x	x	x		4 to 6		SCX6312	National
			2385	55		56	x	x	x		4 to 6		SCX6324	National
			2430	12		76	x	x	x		4 to 6		SCX6325	National
			4860	54		54	x	x			4 to 6		SCX6348	National
			6090	66		88	x	x			4 to 6		SCX6360	National
	75	CMOS	648			56	x	x	x		5		**HGA-C00600**	**† Harris (4740)**
			1296			80	x	x	x		5		**HGA-C01200**	**† Harris (4740)**
			2520			102	x	x	x		5		**HGA-C02500**	**† Harris (4740)**
	80	STL	540	(76)	(38)	76		x			5, 2		**TAT004**	**† TI (538,4894)**
			1008	(104)	(52)	104		x			5, 2		**TAT008**	**† TI (538,4894)**
3.5*	25	CMOS	300	1		37	x		x	x		3 to 7	HCS3100	† CalDevices
			400	1		43	x		x	x		3 to 7	HCS4100	† CalDevices
			500			46	x	x	x		2.5 to 5.5		**GA500**	**† AMI (4619)**
			540	1		49	x	x	x		3 to 7		HCS5400	† CalDevices
			770	1		59	x	x	x		3 to 7		HCS7700	† CalDevices
			1000	1		67	x	x	x		3 to 7		HCS10000	† CalDevices
3.6	100	TTL-LS	1000	66		52		x	x		5		µPB6110	NEC
3.8	75	CMOS	8000			160		x	x		5		**C8000VH**	**Fujitsu (4640)**
4.0	12	CMOS	330			38	x	x	x		2 to 6		**SCC0335H**	**Signetics (4866)**
			448			26	x	x	x		2 to 6		**SCC0455H**	**Signetics (4866)**
			704			38	x	x	x		3 to 15		**SCC0705H**	**Signetics (4866)**
			1106			66	x	x	x		2 to 6		**SCC1105H**	**Signetics (4866)**
	15	CMOS	500			50	x	x	x		5		HD61J	Hitachi
			1000			68	x	x	x		5		HD61K	Hitachi
			1600			68	x	x	x		5		HD61L	Hitachi
			2500			104	x	x	x		5	Optional 256-bit RAM	HIT	Hitachi
	20	CMOS	504			38	x	x	x		0.5 to 7		Interchip 50	† IntMicCir
			960			48	x	x	x		0.5 to 7		Interchip 100	† IntMicCir
			1444			62	x	x	x		0.5 to 7		Interchip 150	† IntMicCir
			2000	(76)	(76)		x	x	x		3 to 6.5		MA4200	† Mitel
	25	ISL	1192			36		x	x		5, 1.5		**8A1200**	**† Signetics (4834)**
						60		x	x		5, 1.5		**8A1260**	**† Signetics (527,4844)**
			1472			42		x	x		5, 1.5		**8A1542**	**† Signetics (527,4848)**
			1620			64		x	x		5, 1.5		**8A1664**	**† Signetics (527,4852)**
			1740			64		x	x		5, 1.5		**8A1864**	**† Signetics (527,4853)**
			2088			76		x	x		5, 1.5		**8A2176**	**† Signetics (527,4854)**
	35	CMOS	4104			118	x	x	x		5		µPD65040	NEC
			6528			134	x	x	x		5		µPD65060	NEC
			11250			172	x	x	x		5		µPD65100	NEC
	38	CMOS	135			32	x	x	x		3 to 10		**G70090**	**† IntMicCir (4747)**
			300			40	x	x	x		3 to 10		**G70200**	**† IntMicCir (4747)**
			375			40	x	x	x		3 to 10		**G70250**	**† IntMicCir (4747)**
			540			52	x	x	x		3 to 10		**G70360**	**† IntMicCir (4747)**
			735			58	x	x	x		3 to 10		**G70490**	**† IntMicCir (4747)**
			960			68	x	x	x		3 to 10		**G70640**	**† IntMicCir (4747)**
			1215			76	x	x	x		3 to 10		**G70810**	**† IntMicCir (4747)**
			1500			84	x	x	x		3 to 10		**G71000**	**† IntMicCir (4747)**
														(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

Master Selection Guide

CUSTOM/SEMICUSTOM

CUSTOM/SEMICUSTOM–Gate Arrays (Cont'd)

Internal Gate Delay ns (max)	Toggle Frequency MHz	Type	No. Equiv. 2-Input Gates	Input/Output Cells: Input Only	Output Only	Uncommitted	Input/Output Compatibility: CMOS	TTL-LS	TTL	ECL	Supply Voltage V	Comments	Device	Source
Gate Arrays														**(Cont'd)**
4.0	38	CMOS												(Cont'd)
			1740			64	x	x	x		3 to 10		**G91160**	**† IntlMicCir (4747)**
			2160			100	x	x	x		3 to 10		**G71440**	**† IntlMicCir (4747)**
			2646			84	x	x	x		3 to 10		**G91764**	**† IntlMicCir (4747)**
			2940			116	x	x	x		3 to 10		**G71960**	**† IntlMicCir (4747)**
			3360			68	x	x	x		3 to 10		**G92240**	**† IntlMicCir (4747)**
			4185			84	x	x	x		3 to 10		G92780	† IntlMicCir (4747)
			5250			106	x	x	x		3 to 10		**G93500**	**† IntlMicCir (4747)**
			7650			100	x	x	x		3 to 10		**G95100**	**† IntlMicCir (4747)**
4.2	38	CMOS	500	3		40	x	x	x		3 to 10		**BC405**	**† Barvon (4626)**
			1000	3		65	x	x	x		3 to 10		**BC410**	**† Barvon (4626)**
			1500	3		75	x	x	x		3 to 10		**BC415**	**† Barvon (4626)**
			2000	3		90	x	x	x		3 to 10		**BC420**	**† Barvon (4626)**
	55	CMOS	440			54		x	x		5		**C440H**	**Fujitsu (4639)**
			770			46		x	x		3 to 10		**C770H**	**Fujitsu (4639)**
			1275			64		x	x		5		**C1275H**	**Fujitsu (4639)**
			2000			72		x	x		5		**C2000H**	**Fujitsu (4639)**
			3900			72		x	x		5		**C3900H**	**Fujitsu (4639,4640)**
	100	CMOS	1000			76	x	x	x		5, 2		CT0750	† Fairchild
4.4	30	CMOS	360			36	x	x	x		3 to 14		IS05A	† Siliconix
						36	x	x	x		3 to 14		**IS05A**	**† Universal (4930)**
			540			48	x	x	x		3 to 14		IS05B	† Siliconix
						48	x	x	x		3 to 14		**IS05B**	**† Universal (4930)**
			720			54	x	x	x		3 to 14		IS05C	† Siliconix
						54	x	x	x		3 to 14		**IS05C**	**† Universal (4930)**
			960			62	x	x	x		3 to 14		IS05D	† Siliconix
						62	x	x	x		3 to 14		**IS05D**	**† Universal (4930)**
			1200			68	x	x	x		3 to 14		IS05E	† Siliconix
						68	x	x	x		3 to 14		**IS05E**	**† Universal (4930)**
			1500			70	x	x	x		3 to 14		IS05F	† Siliconix
						70	x	x	x		3 to 14		**IS05F**	**† Universal (4930)**
			1800			82	x	x	x		3 to 14		IS05G	† Siliconix
						82	x	x	x		3 to 14		**IS05G**	**† Universal (4930)**
			2400			82	x	x	x		3 to 14		IS05H	† Siliconix
						82	x	x	x		3 to 14		**IS05H**	**† Universal (4930)**
	80	CML	500			38	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA5RA	† Ferranti
						38	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA5RA	† Interdesign
			900			48	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA9RA	† Ferranti
						48	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA9RA	† Interdesign
			1200			52	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA12RA	† Ferranti
						52	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA12RA	† Interdesign
			1600			62	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA16RA	† Ferranti
						62	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA16RA	† Interdesign
			1800			64	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA18RA	† Ferranti
						64	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA18RA	† Interdesign
			2000			72	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA20RA	† Ferranti
						72	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA20RA	† Interdesign
			2400			80	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA24RA	† Ferranti
						80	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA24RA	† Interdesign
			3000			82	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA30RA	† Ferranti
						82	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA30RA	† Interdesign
			4000			118	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA40RA	† Ferranti
						118	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA40RA	† Interdesign

† Military Temperature Range (−55° to 125°C)

* Typical Value

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CUSTOM/SEMICUSTOM-Gate Arrays (Cont'd)

Internal Gate Delay ns (max)	Toggle Frequency MHz	Type	No. Equiv. 2-Input Gates	Input/Output Cells: Input Only	Output Only	Uncommitted	Input/Output Compatibility: CMOS	TTL-LS	TTL	ECL	Supply Voltage V	Comments	Device	Source
Gate Arrays														**(Cont'd)**
4.5	25	CMOS	48		14	16	x	x	x		3 to 7		**SP7000**	**†SPI (4826)**
			80		16	20	x	x	x		2 to 7		**SP7001**	**†SPI (4826)**
			150		16	24	x	x	x		2 to 7		**SP7002**	**†SPI (4826)**
			300		22	44	x	x	x		2 to 7		**SP7003**	**†SPI (4826)**
					34	44	x	x	x		2 to 7		**SP7004**	**†SPI (4826)**
			544		30	56	x	x	x		2 to 7		**SP7005**	**†SPI (4826)**
			1000		40	76	x	x	x		2 to 7		**SP7010**	**†SPI (4826)**
					72	84	x	x	x		3 to 7		**SP7210**	**SPI (4826)**
	30	CMOS	400			40	x	x	x		5		**CMA2004**	**†CMA (4630)**
			800			60	x	x	x		5		**CMA2008**	**†CMA (4630)**
			1100			68	x	x	x		5		**CMA2011**	**†CMA (4630)**
			1500			80	x	x	x		5		**CMA2015**	**†CMA (4630)**
			2400			110	x	x	x		5		**CMA2024**	**†CMA (4630)**
	70	TTL-LS	256	6		32		x	x		5	256 equiv. 3-input gates	**μPB6101**	**NEC (4804)**
			598	12		52		x	x			598 equiv. 3-input gates	**μPB6102**	**NEC (4804)**
	80	CML	500			38	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA5RA	† Ferranti
						38	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA5RA	† Interdesign
			900			48	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA9RA	† Ferranti
						48	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA9RA	† Interdesign
			1200			52	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA12RA	† Ferranti
						52	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA12RA	† Interdesign
			1600			62	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA16RA	† Ferranti
						62	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA16RA	† Interdesign
			1800			64	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA18RA	† Ferranti
						64	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA18RA	† Interdesign
			2000			72	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA20RA	† Ferranti
						72	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA20RA	† Interdesign
			2400			80	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA24RA	† Ferranti
						80	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA24RA	† Interdesign
			3000			82	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA30RA	† Ferranti
						82	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA30RA	† Interdesign
			4000			118	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA40RA	† Ferranti
						118	x	x	x	x	3.5 to 5.5	300 μW/gate	ULA40RA	† Interdesign
4.6	15	CMOS	504	(38)	(38)		x	x	x		3 to 6.5		MA5050	† Mitel
			960	(48)	(48)		x	x	x		3 to 6.5		MA5100	† Mitel
			1444	(62)	(62)		x	x	x		3 to 6.5		MA5150	† Mitel
5.0	20	CMOS	252			38	x	x	x		3 to 10		SG250	† MicroTech
			300		16	34	x	x	x		5 to 10. to 200	16 push-pull outputs, ± 15 mA, 200 V.	TMG5002	Telmos
			405			40	x	x	x		3 to 10		SG400	† MicroTech
			605			48	x	x	x		3 to 10		SG600	† MicroTech
			798			54	x	x	x		3 to 10		SG800	† MicroTech
			1012			58	x	x	x		3 to 10		SG1000	† MicroTech
			1250			66	x	x	x		3 to 10		SG1250	† MicroTech
			1510			72	x	x	x		3 to 10		SG1500	† MicroTech
			1980			82	x	x	x		3 to 10		SG2000	† MicroTech
	25	CMOS	880			66	x	x	x		3 to 6		**LL5080**	**†LSILogic (4762)**
			1404			84	x	x	x		3 to 6		**LL5140**	**†LSILogic (4762)**
			2224			106	x	x	x		3 to 6		**LL5220**	**†LSILogic (4762)**
			3192			130	x	x	x		3 to 6		**LL5320**	**†LSILogic (4762)**
			4202			148	x	x	x		3 to 6		**LL5420**	**†LSILogic (4762)**
			6000			172	x	x	x		3 to 6		**LL5600**	**†LSILogic (4762)**
		TTL-LS	320			28		x			5		**TAL002**	**TI (4887)**
			500			42		x			5		**TAL004**	**TI (4887)**

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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CUSTOM/SEMICUSTOM–Gate Arrays (Cont'd)

Internal Gate Delay ns (max)	Toggle Frequency MHz	Type	No. Equiv. 2-Input Gates	Input/Output Cells: Input Only	Output Only	Uncommitted	Input/Output Compatibility: CMOS	TTL-LS	TTL	ECL	Supply Voltage V	Comments	Device	Source
Gate Arrays														**(Cont'd)**
5.0	25													(Cont'd)
		CMOS	840			40	x	x	x		3 to 7		**CLA2100**	† **Plessey (4819)**
		CMOS	1440			52	x	x	x		3 to 7		**CLA2300**	† **Plessey (4819)**
		CMOS	2400			64	x	x	x		3 to 7		**CLA2500**	† **Plessey (4819)**
	30	CMOS	150			32	x	x	x		3 to 14		AT-D-150	† ArrayTech
			250	18	12	32	x	x	x		3 to 14		AT-D-250	† ArrayTech
			350			36	x	x	x		3 to 14		AT-D-350	† ArrayTech
			550			48	x	x	x		3 to 14		AT-D-550	† ArrayTech
			750			54	x	x	x		3 to 14		AT-D-750	† ArrayTech
			1000			62	x	x	x		3 to 14		AT-D-1000	† ArrayTech
			1200			68	x	x	x		3 to 14		AT-D-1200	† ArrayTech
			1500			76	x	x	x		3 to 14		AT-D-1500	† ArrayTech
			1800			82	x	x	x		3 to 14		AT-D-1800	† ArrayTech
	33	CMOS	500	3		40	x	x	x		3 to 10		BC405	† Barvon
			1000	3		65	x	x	x		3 to 10		BC410	† Barvon
			1500	3		75	x	x	x		3 to 10		BC415	† Barvon
			2000	3		90	x	x	x		3 to 10		BC420	† Barvon
	40	CMOS	725			58	x				5		**PA40650**	† **RCA (4824)**
			953			70	x				5		**PA40850**	† **RCA (4824)**
			1133			78	x				5		**PA41000**	† **RCA (4824)**
			1313			86	x				5		**PA41200**	† **RCA (4824)**
	50	CMOS	600			38	x	x	x		5		7CL	† STC
			648	2		35	x	x	x		3 to 6		HCA6306	† Motorola
			725			58	x				4 to 10		**PA60650**	† **RCA (4824)**
			1200	17		42	x	x	x		3 to 6		HCA6312	† Motorola
			1313			86	x				4 to 10		**PA61200**	† **RCA (4824)**
			1440			64	x	x	x		5		7CM	† STC
			1920			96	x	x	x		5		7CK	† STC
			2295	55		56	x	x	x		3 to 6		HCA6324	† Motorola
			4200			80	x	x	x		3 to 7		**CLA3000**	† **Plessey (4819)**
			4860	53		54	x	x	x		3 to 6		HCA6348	† Motorola
5.0 *	15	CMOS	504			38	x	x	x		3 to 6.5		50500A	GTEMicro
			960			48	x	x	x		3 to 6.5		51000A	GTEMicro
			1440			62	x	x	x		3 to 6.5		51500A	GTEMicro
6 *	25	CMOS	1200			64	x	x	x		5		TAC020	TI
6.0	12	CMOS	408			34	x	x	x		3 to 9		**IGC10408**	† **Intersil (4751)**
			756			44	x	x	x		3 to 9		**IGC10756**	† **Intersil (4751)**
			1500			62	x	x	x		3 to 9		**IGC11500**	† **Intersil (4751)**
			2001			70	x	x	x		3 to 9		**IGC12001**	† **Intersil (4751)**
	15	CMOS	324			30	x	x	x		3 to 6		LAD3	† GI
			560			38	x	x	x		3 to 6		LA05	† GI
			960			50	x	x	x		3 to 6		LA10	† GI
			1440			62	x	x	x		3 to 6		LA15	† GI
			2014			74	x	x	x		3 to 6		LA20	† GI
	20	ISL	1192			36		x	x		5, 1.5		8A1200	† Signetics
						60		x	x		5, 1.5		8A1260	† Signetics
			1472			42		x	x		5, 1.5		8A1542	† Signetics
			1620			64		x	x		5, 1.5		8A1664	† Signetics
			1740			64		x	x		5, 1.5		8A1864	† Signetics
			2088			76		x	x		5, 1.5		8A2176	† Signetics
	25	CMOS	427	2		34	x	x	x		5		**μPD65003**	**NEC (4809)**
			500	3		40	x	x	x		3 to 10		**BC505**	† **Barvon (4626)**
			858			48	x	x	x		5		**μPD65002**	**NEC (4809)**
			1000	3		65	x	x	x		3 to 10		**BC510**	**Barvon (4626)**
			1368			62	x	x	x		5		**μPD65010**	**NEC (4809)**
			1500	3		75	x	x	x		3 to 10		**BC515**	† **Barvon (4626)**

(Continued)

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CUSTOM/SEMICUSTOM–Gate Arrays (Cont'd)

Internal Gate Delay ns (max)	Toggle Frequency MHz	Type	No. Equiv. 2-Input Gates	Input/Output Cells: Input Only	Output Only	Uncommitted	Input/Output Compatibility: CMOS	TTL-LS	TTL	ECL	Supply Voltage V	Comments	Device	Source
Gate Arrays														**(Cont'd)**
6.0	25	CMOS	2000	3		90	x	x	x		3 to 10		**BC520**	(Cont'd) **† Barvon (4626)**
			2112			78	x	x	x		5		**μPD65020**	**NEC (4809)**
6.5 *	—	CMOS	200			26		x	x		5	208 equiv. 3-input gates	**B200**	**Fujitsu (4637)**
6.7	50	CMOS	640			38	x	x	x		5		MKA300	† Mostek
			2048			92	x	x	x		5		MKA102A	† Mostek
			3680			130	x	x	x		5		MKA1840	† Mostek
			5376			138	x	x	x		5		MKA2688	† Mostek
7.0	10	CMOS	1250			80	x	x	x		5		XRCSD	† Exar
7.2	27	CMOS	500	3		40	x	x	x		3 to 10		BC505	† Barvon
			1000	3		65	x	x	x		3 to 10		BC520	† Barvon
			1500	3		75	x	x	x		3 to 10		BC515	† Barvon
			2000	3		90	x	x	x		3 to 10		BC520	† Barvon
8.0	10	NMOS	370	2	16				x		5	Logic array	WD1820	Western
			1760	3		35			x		5	Logic array with PLA	WD1828/40	Western
	20	CMOS	168			20	x				3 to 12		**MA10150**	**† RCA (4824)**
			182			20	x				4 to 10		**MA60150**	**† RCA (4824)**
			276			24	x				3 to 12		**MA16250**	**† RCA (4824)**
			300			24	x						**MA60250**	**† RCA (4824)**
			317			30	x				5		**PA20254**	**† RCA (4824)**
			400			48	x				3 to 12		**MA10350**	**† RCA (4824)**
			452			32	x				4 to 10		**MA60400**	**† RCA (4824)**
			517			46	x				5		**PA20450**	**† RCA (4824)**
			576			64	x				3 to 12		**MA10500**	**† RCA (4824)**
			632			32	x				4 to 10		**MA60550**	**† RCA (4824)**
			725			58	x				5		**PA30650**	**† RCA (4824)**
			848			32	x				4 to 10		**MA60800**	**† RCA (4824)**
			953			70	x				5		**PA20850**	**† RCA (4824)**
			1313			78	x				5		**PA21000**	**† RCA (4824)**
	33	CMOS	300			38	x	x	x		1 to 12		TM4030	† Telmos
			338		8	37	x	x	x		5 to 10, to 300	40 dedicated flip-flops, 8 300V transistors	TM5001	† Telmos
			400			44	x	x	x		1 to 12		TM4040	† Telmos
			540			50	x	x	x		1 to 12		TM4054	† Telmos
			770			60	x	x	x		1 to 12		TM4077	† Telmos
			1000			68	x	x	x		1 to 12		TM4100	† Telmos
			1260			76	x	x	x		1 to 12		TM4126	† Telmos
	40	CMOS	150			29	x	x	x		2 to 7		MPE	Interdesign
			510			54	x	x	x		2 to 7		**MPA**	**† Interdesign (4746)**
			1000			73	x	x	x		2 to 7		**MPB**	**† Interdesign (4746)**
			1500			89	x	x	x		2 to 7		**MPC**	**† Interdesign (4746)**
			2000			122	x	x	x		2 to 7		**MPD**	**† Interdesign (4746,4747)**
8.4	35	CMOS	770			46	x	x	x		5		C770	Fujitsu
			1275			64	x	x	x		5		C1275	Fujitsu
			2000			72	x	x	x		5		C2000	Fujitsu
			3900			72	x	x	x		5		**C3900**	**Fujitsu (4640)**
9.0	15	CMOS	272			32	x	x	x		3 to 6		**LL3020**	**† LSILogic (4762)**
			342			36	x	x	x		3 to 6		**LL3030**	**† LSILogic (4762)**
			420			40	x	x	x		3 to 6		**LL3040**	**† LSILogic (4762)**
			600			48	x	x	x		3 to 6		**LL3060**	**† LSILogic (4762)**
			812			56	x	x	x		3 to 6		**LL3080**	**† LSILogic (4762)**
			1056			64	x	x	x		3 to 6		**LL3110**	**† LSILogic (4762)**
			1332			72	x	x	x		3 to 6		**LL3130**	**† LSILogic (4762)**
			1722			82	x	x	x		3 to 6		**LL3170**	**† LSILogic (4762)**
			2162			92	x	x	x		3 to 6		**LL3210**	**† LSILogic (4762)**
			2550			100	x	x	x		3 to 6		**LL3250**	**† LSILogic (4762)**

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

CUSTOM/SEMICUSTOM–Gate Arrays (Cont'd)

Internal Gate Delay ns (max)	Toggle Frequency MHz	Type	No. Equiv. 2-Input Gates	Input/Output Cells: Input Only	Output Only	Uncommitted	Input/Output Compatibility: CMOS	TTL-LS	TTL	ECL	Supply Voltage V	Comments	Device	Source
Gate Arrays														**(Cont'd)**
10	8	CMOS	153			30	x	x	x		1.5 to 18	4 dedicated flip-flops	**HI3600**	**† Holt (4745)**
			384			44	x	x	x		1.5 to 18	16 dedicated flip-flops	**HI3900**	**† Holt (4745)**
			490			48	x	x	x		1.5 to 18	32 dedicated flip-flops	**HI3100**	**† Holt (4745)**
			1020			68	x	x	x		1.5 to 18	60 dedicated flip-flops	**HI3300**	**† Holt (4745)**
	10	CMOS	300	1		37	x	x	x		2.7 to 12		**UA-1**	**† AMI (4619)**
			400	1		43	x	x	x		2.7 to 12		**UA-2**	**† AMI (4619)**
			540	1		49	x	x	x		2.7 to 12		**UA-3**	**† AMI (4619)**
			770	1		59	x	x	x		2.7 to 12		**UA-4**	**† AMI (4619)**
			1000	1		67	x	x	x		2.7 to 12		**UA-5**	**† AMI (4619)**
			1260	1		75	x	x	x		2.7 to 12		**UA-6**	**† AMI (4619)**
	15	CMOS	560			38	x	x	x		3 to 8		MA8505	† CirTech
			960			50	x	x	x		3 to 8		MA8510	† CirTech
			1440			62	x	x	x		3 to 8		MA8515	† CirTech
			2014			74	x	x	x		3 to 8		MA8520	† CirTech
10.0	20	CMOS	560			38	x	x	x		3 to 7		**CLA1000**	**† Plessey (4819)**
		CMOS	964			50	x	x	x		3 to 7		**CLA1200**	**† Plessey (4819)**
		CMOS	1400			62	x	x	x		3 to 7		**CLA1500**	**† Plessey (4819)**
12	6	CMOS	300	1		37	x	x	x		3 to 10		**LC3100**	**† LSILogic (4762)**
			400	1		43	x	x	x		3 to 10		**LC4100**	**† LSILogic (4762)**
			540	1		49	x	x	x		3 to 10		**LC5400**	**† LSILogic (4762)**
			770	1		59	x	x	x		3 to 10		**LC7700**	**† LSILogic (4762)**
			1000	1		67	x	x	x		3 to 10		**LC10000**	**† LSILogic (4762)**
			1260	1		75	x	x	x		3 to 10		**LC12600**	**† LSILogic (4762)**
	20	CML	2000			64	x	x	x	x	3.5 to 5.5	250 μW/gate	ULA9C	† Ferranti
						64	x	x	x	x	3.5 to 5.5	250 μW/gate	ULA9C	† Interdesign
			2400			68	x	x	x	x	3.5 to 5.5	250 μW/gate	ULA12C	† Ferranti
						68	x	x	x	x	3.5 to 5.5	250 μW/gate	ULA12C	† Interdesign
12.7	20	CML	500			38	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA5RB	† Ferranti
						38	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA5RB	† Interdesign
			900			48	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA9RB	† Ferranti
						48	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA9RB	† Interdesign
			1200			52	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA12RB	† Ferranti
						52	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA12RB	† Interdesign
			1600			62	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA16RB	† Ferranti
						62	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA16RB	† Interdesign
			1800			64	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA18RB	† Ferranti
						64	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA18RB	† Interdesign
			2000			72	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA20RB	† Ferranti
						72	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA20RB	† Interdesign
			2400			80	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA24RB	† Ferranti
						80	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA24RB	† Interdesign
			3000			82	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA30RB	† Ferranti
						82	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA30RB	† Interdesign
			4000			118	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA40RB	† Ferranti
						118	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA40RB	† Interdesign
13	5	CMOS	50			22	x	x	x		3 to 15		TM3050	† Telmos
			112			32	x	x	x		3 to 15		TM3100	† Telmos
			162			38	x	x	x		3 to 15		TH3150	† Telmos
			216			44	x	x	x		3 to 15		TM3200	† Telmos
			224			53	x	x	x		3 to 15	32 dedicated flip-flops	TM3350	† Telmos
			272			69	x	x	x		3 to 15	72 dedicated flip-flops	TM3600	† Telmos
			464			69	x	x	x		3 to 15	24 dedicated flip-flops	TM3500	† Telmos
13.6	20	CML	500			38	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA5RB	† Ferranti
						38	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA5RB	† Interdesign
			900			48	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA9RB	† Ferranti
						48	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA9RB	† Interdesign

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† Military Temperature Range (−55° to 125°C)

* Typical Value

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CUSTOM/SEMICUSTOM–Gate Arrays (Cont'd)

Internal Gate Delay ns (max)	Toggle Frequency MHz	Type	No. Equiv. 2-Input Gates	Input/Output Cells: Input Only	Output Only	Uncommitted	Input/Output Compatibility: CMOS	TTL-LS	TTL	ECL	Supply Voltage V	Comments	Device	Source
Gate Arrays														**(Cont'd)**
13.6	20	CML	1200			52	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA12RB	† Ferranti
						52	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA12RB	† Interdesign
			1600			62	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA16RB	† Ferranti
						62	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA16RB	† Interdesign
			1800			64	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA18RB	† Ferranti
						64	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA18RB	† Interdesign
			2000			72	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA20RB	† Ferranti
						72	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA20RB	† Interdesign
			2400			80	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA24RB	† Ferranti
						80	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA24RB	† Interdesign
			3000			82	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA30RB	† Ferranti
						82	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA30RB	† Interdesign
			4000			118	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA40RB	† Ferranti
						118	x	x	x	x	3.5 to 5.5	100 μW/gate	ULA40RB	† Interdesign
14	20	CML	450			39	x	x	x	x	3.5 to 5.5	250 μW/gate	ULA2C	† Ferranti
						39	x	x	x	x	3.5 to 5.5	250 μW/gate	ULA2C	† Interdesign
			900			48	x	x	x	x	3.5 to 5.5	250 μW/gate	ULA5C	† Ferranti
						48	x	x	x	x	3.5 to 5.5	250 μW/gate	ULA5C	† Interdesign
15		I²L	1120			96	x	x	x				**SBP96700**	**† TI (538)**
			2120			140	x	x	x				**SBP96600**	**† TI (538)**
	2	CMOS	80			28	x	x	x		3 to 15		606	† MicroTech
			160			38	x	x	x		3 to 15		616	† MicroTech
			320			48	x	x	x		3 to 15		626	† MicroTech
			480			62	x	x	x		3 to 15		636	† MicroTech
			1000			72	x	x	x		3 to 15		646	† MicroTech
		NMOS	120			28			x		5 to 7	12 dedicated flip-flops	707	† MicroTech
			240			40			x		5 to 7	24 dedicated flip-flops	717	† MicroTech
			400			50			x		5 to 7	40 dedicated flip-flops	727	† MicroTech
			560			51			x		5 to 7	50 dedicated flip-flops	737	† MicroTech
	20	CML	454			39	x	x	x	x	3.5 to 5.5	250 μW/gate	ULA2C	† Ferranti
						39	x	x	x	x	3.5 to 5.5	250 μW/gate	ULA2C	† Interdesign
			900			48	x	x	x	x	3.5 to 5.5	250 μW/gate	ULA5C	† Ferranti
						48	x	x	x	x	3.5 to 5.5	250 μW/gate	ULA5C	† Interdesign
			2000			64	x	x	x	x	3.5 to 5.5	250 μW/gate	ULA9C	† Ferranti
						64	x	x	x	x	3.5 to 5.5	250 μW/gate	ULA9C	† Interdesign
			2400			68	x	x	x	x	3.5 to 5.5	250 μW/gate	ULA12C	† Ferranti
						68	x	x	x	x	3.5 to 5.5	250 μW/gate	ULA12C	† Interdesign
16	6 *	CMOS	330			38	x	x	x		3 to 15		**SCC0330M**	**Signetics (4862)**
			448			26	x	x	x		3 to 15		**SCC0450M**	**Signetics (4862)**
			704			38	x	x	x		3 to 15		**SCC0700M**	**Signetics (4862)**
			1106			66	x	x	x		3 to 15		**SCC1100M**	**Signetics (4862)**
	10	CMOS	168			20	x				1.1 to 20		MA30150	† RCA
			276			24	x						MA30250	† RCA
17	9	CMOS	140			29	x	x	x		3 to 15		**MCA**	**† Interdesign (4746)**
			200			34	x	x	x		3 to 15		**MCB**	**† Interdesign (4746)**
			270			40	x	x	x		3 to 15		**MCC**	**† Interdesign (4746)**
			340			40	x	x	x		3 to 15	28 dedicated flip-flops	**MCE**	**† Interdesign (4746)**
			440			46	x	x	x		3 to 15	32 dedicated flip-flops	**MCD**	**† Interdesign (4746)**
			630			50	x	x	x		3 to 15		**MCF**	**† Interdesign (4746)**
			880			58	x	x	x		3 to 15		**MCG**	**† Interdesign (4746)**
18	3	CMOS	100			32	x	x			0.5 to 18		Interchip A	† Intech
			150			38	x	x			0.5 to 18		Interchip B	† Intech
			215			44	x	x			0.5 to 18		Interchip C	† Intech
			224			53	x	x			0.5 to 18	32 dedicated flip-flops	Interchip D	† Intech
			368			64	x	x			0.5 to 18	72 dedicated flip-flops	Interchip F	† Intech

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† Military Temperature Range (−55° to 125°C)

* Typical Value

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CUSTOM/SEMICUSTOM–Gate Arrays (Cont'd)

Internal Gate Delay ns (max)	Toggle Frequency MHz	Type	No. Equiv. 2-Input Gates	Input/Output Cells: Input Only	Output Only	Uncommitted	Input/Output Compatibility: CMOS	TTL-LS	TTL	ECL	Supply Voltage V	Comments	Device	Source
Gate Arrays														**(Cont'd)**
18	3	CMOS	464			64	x	x			0.5 to 18	24 dedicated flip-flops	Interchip E	† Intech
21	2.5	CMOS	112			29	x	x	x		3 to 12		XRCMA	† Exar
			162			34	x	x	x		3 to 12		XRCMB	† Exar
			216			40	x	x	x		3 to 12		XRCMC	† Exar
			544			46	x	x	x		3 to 12		XRCMD	† Exar
25	8	CMOS	100	11		18	x	x	x		3 to 18		CDI1000	† CalDevices
			200	12		26	x	x	x		3 to 18		CDI2000	† CalDevices
			315	14		32	x	x	x		3 to 18		CDI3000	† CalDevices
			420	14		38	x	x	x		3 to 18		CDI4000	† CalDevices
			600	18		44	x	x	x		3 to 18		CDI6000	† CalDevices
			880	16		54	x	x	x		3 to 18		CDI8800	† CalDevices
	12	CMOS	220	8	10		x	x	x		1 to 18		MGA220	† MCE
			225	8	10		x	x	x		1 to 18		MGA255	† MCE
30	10	I²L	11400			62			x	x	1 to 6	Programmable speed/power, 7600 equiv. 5-input gates	GAC-8000	† CIC
42	10	CML	500			38	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA5RC	† Ferranti
						38	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA5RC	† Interdesign
			900			48	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA9RC	† Ferranti
						48	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA9RC	† Interdesign
			1200			52	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA12RC	† Ferranti
						52	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA12RC	† Interdesign
			1600			62	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA16RC	† Ferranti
						62	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA16RC	† Interdesign
			1800			64	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA18RC	† Ferranti
						64	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA18RC	† Interdesign
			2000			72	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA20RC	† Ferranti
						72	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA20RC	† Interdesign
			2400			80	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA24RC	† Ferranti
						80	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA24RC	† Interdesign
			3000			82	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA30RC	† Ferranti
						82	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA30RC	† Interdesign
			4000			118	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA40RC	† Ferranti
						118	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA40RC	† Interdesign
45	5	CML	450			39	x	x	x	x	3.5 to 5.5	70 μW/gate	ULA2N	† Ferranti
						39	x	x	x	x	3.5 to 5.5	70 μW/gate	ULA2N	† Interdesign
			900			48	x	x	x	x	3.5 to 5.5	70 μW/gate	ULA5N	† Ferranti
						48	x	x	x	x	3.5 to 5.5	70 μW/gate	ULA5N	† Interdesign
			2000			64	x	x	x	x	3.5 to 5.5	40 μW/gate	ULA9N	† Ferranti
						64	x	x	x	x	3.5 to 5.5	40 μW/gate	ULA9N	† Interdesign
			2400			68	x	x	x	x	3.5 to 5.5	40 μW/gate	ULA12N	† Ferranti
						68	x	x	x	x	3.5 to 5.5	40 μW/gate	ULA12N	† Interdesign
	10	CML	500			38	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA5RC	† Ferranti
						38	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA5RC	† Interdesign
			900			48	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA9RC	† Ferranti
						48	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA9RC	† Interdesign
			1200			52	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA12RC	† Ferranti
						52	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA12RC	† Interdesign
			1600			62	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA16RC	† Ferranti
						62	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA16RC	† Interdesign
			1800			64	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA18RC	† Ferranti
						64	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA18RC	† Interdesign
			2000			72	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA20RC	† Ferranti
						72	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA20RC	† Interdesign
			2400			80	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA24RC	† Ferranti
						80	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA24RC	† Interdesign

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† Military Temperature Range (−55° to 125°C)

* Typical Value

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CUSTOM/SEMICUSTOM-Gate Arrays (Cont'd)

Internal Gate Delay ns (max)	Toggle Frequency MHz	Type	No. Equiv. 2-Input Gates	Input/Output Cells: Input Only	Output Only	Uncommitted	Input/Output Compatibility: CMOS	TTL-LS	TTL	ECL	Supply Voltage V	Comments	Device	Source
Gate Arrays														**(Cont'd)**
45	10	CML												(Cont'd)
			3000			82	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA30RC	† Ferranti
						82	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA30RC	† Interdesign
			4000			118	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA40RC	† Ferranti
						118	x	x	x	x	3.5 to 5.5	30 μW/gate	ULA40RC	† Interdesign
48	5	CML	450			39	x	x	x	x	3.5 to 5.5	70 μW/gate	ULA2N	† Ferranti
						39	x	x	x	x	3.5 to 5.5	70 μW/gate	ULA2N	† Interdesign
			900			48	x	x	x	x	3.5 to 5.5	70 μW/gate	ULA5N	† Ferranti
						48	x	x	x	x	3.5 to 5.5	70 μW/gate	ULA5N	† Interdesign
			2000			64	x	x	x	x	3.5 to 5.5	40 μW/gate	ULA9N	† Ferranti
						64	x	x	x	x	3.5 to 5.5	40 μW/gate	ULA9N	† Interdesign
			2400			68	x	x	x	x	3.5 to 5.5	40 μW/gate	ULA12N	† Ferranti
						68	x	x	x	x	3.5 to 5.5	40 μW/gate	ULA12N	† Interdesign
50	2	CMOS	75			23	x	x	x		2 to 15		G4060	† IntlMicCir
			140			29	x	x	x		2 to 15		G4112	† IntlMicCir
			200			35	x	x	x		2 to 15		**G4160**	**† IntlMicCir (4747)**
			256			18	x	x	x		0.1 to 100 μA	Programmable speed/power	D15C	† MCE
			275			38	x	x	x		2 to 15		**G4220**	**† IntlMicCir (4747)**
			288			28	x	x	x		0.1 to 100 μA	Programmable speed/power	D15A	† MCE
			330			41	x	x	x		2 to 15		**G4264**	**† IntlMicCir (4747)**
			390			43	x	x	x		2 to 15		**G4312**	**† IntlMicCir (4747)**
			455			47	x	x	x		2 to 15		**G4364**	**† IntlMicCir (4747)**
			520			40	x	x	x		0.1 to 100 μA	Programmable speed/power	D15B	† MCE
			525			49	x	x	x		2 to 15		**G4420**	**† IntlMicCir (4747)**
			600			53	x	x	x		2 to 15		**G4480**	**† IntlMicCir (4747)**
			864			21	x	x	x		0.1 to 100 μA	Programmable speed/power	D15D	† MCE
		I^2L	192			24	x	x	x	x	1 to 12	Programmable speed/power	1200	Cherry
						24	x	x	x		1.5 to 7	Programmable speed/power	**XR200**	**† Exar (3386)**
			288			28	x	x	x	x	1 to 12	Programmable speed/power	1300	Cherry
						28	x	x	x		1.5 to 7	Programmable speed/power	**XR300**	**† Exar (3386)**
			520			40	x	x	x		1.5 to 7	Programmable speed/power	**XR500**	**† Exar (3386)**
140	5	CML	500			38	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA5RD	† Ferranti
						38	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA5RD	† Interdesign
			900			48	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA9RD	† Ferranti
						48	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA9RD	† Interdesign
			1200			52	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA12RD	† Ferranti
						52	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA12RD	† Interdesign
			1600			62	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA16RD	† Ferranti
						62	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA16RD	† Interdesign
			1800			64	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA18RD	† Ferranti
						64	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA18RD	† Interdesign
			2000			72	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA20RD	† Ferranti
						72	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA20RD	† Interdesign
			2400			80	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA24RD	† Ferranti
						80	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA24RD	† Interdesign
			3000			82	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA30RD	† Ferranti
						82	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA30RD	† Interdesign
			4000			118	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA40RD	† Ferranti
						118	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA40RD	† Interdesign
220	5	CML	500			38	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA5RD	† Ferranti
						38	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA5RD	† Interdesign
			900			48	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA9RD	† Ferranti
						48	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA9RD	† Interdesign
			1200			52	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA12RD	† Ferranti
						52	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA12RD	† Interdesign

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

Master Selection Guide

CUSTOM/SEMICUSTOM

CUSTOM/SEMICUSTOM–Gate Arrays (Cont'd)

Internal Gate Delay ns (max)	Toggle Fre-quency MHz	Type	No. Equiv. 2-Input Gates	Input/Output Cells: Input Only	Input/Output Cells: Output Only	Input/Output Cells: Un-com-mitted	Input/Output Compatibility: CMOS	Input/Output Compatibility: TTL-LS	Input/Output Compatibility: TTL	Input/Output Compatibility: ECL	Supply Voltage V	Comments	Device	Source
Gate Arrays														**(Cont'd)**
220	5	CML												(Cont'd)
			1600			62	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA16RD	† Ferranti
						62	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA16RD	† Interdesign
			1800			64	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA18RD	† Ferranti
						64	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA18RD	† Interdesign
			2000			72	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA20RD	† Ferranti
						72	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA20RD	† Interdesign
			2400			80	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA24RD	† Ferranti
						80	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA24RD	† Interdesign
			3000			82	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA30RD	† Ferranti
						82	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA30RD	† Interdesign
			4000			118	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA40RD	† Ferranti
						118	x	x	x	x	3.5 to 5.5	12 μW/gate	ULA40RD	† Interdesign
8000	0.1	CML	510			40	x	x	x	x	3.5 to 5.5	0.4 μW/gate	ULA2M	† Ferranti
						40	x	x	x	x	3.5 to 5.5	0.4 μW/gate	ULA2M	† Interdesign
10500	0.1	CML	510			40	x	x	x	x	3.5 to 5.5	0.4 μW/gate	ULA2M	† Ferranti
						40	x	x	x	x	3.5 to 5.5	0.4 μW/gate	ULA2M	† Interdesign

† Military Temperature Range (−55° to 125°C)

* Typical Value

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CUSTOM/SEMICUSTOM–Linear & Linear/Digital Arrays

Manufacturer / Technology	Total Bonding Pads	Linear: Dedicated Op Amps, A/D, etc.	Linear: Total Other Lin. Components	Digital: Equiv. 2-Input Gates	Digital: Gate Delay ns @ V	Uncommited Transistors: NPN	Uncommited Transistors: PNP	Number Capacitors	Supply Voltage, V	Comments	Device	Source
Linear & Linear/Digital Arrays												
Array Technology CMOS	42	6		200	5	500	500	12	12	8-bit DAC, 4 op amps, 2 comparators	AT-LD-04	ArrayTech
	70	12		400	5	1000	1000	24	12	8-bit DAC, 8 op amps, 4 comparators	AT-LD-08	ArrayTech
Barvon Research Bi-CMOS		1	2292	400	7	104	76		15/6	4 to 16 decades, combination bipolar and CMOS	**BC3G02**	**Barvon (4626)**
	58	—	585	250	7	92	52		15/6	Combination bipolar and CMOS	**BC3G01**	**Barvon (4626)**
California Devices BIP	14		110			22	8		20		CLIC-C	CalDevices
	16		209			50	16		20		CLIC-D	CalDevices
			260			59	15		20		CLIC-A	CalDevices
	18		168			38	12		20		CLIC-I	CalDevices
			207			48	15		20		CLIC-E	CalDevices
			460			96	36		20		CLIC-F	CalDevices
	20		370			72	22		20		CLIC-H	CalDevices
	24		300			69	12		20		CLIC-B	CalDevices
			310			60	18		20		CLIC-G	CalDevices
			398			80	22		20		CLIC-L	CalDevices
Cherry Semiconductor BIP	16		333			60	25		20	Flip-chip	CS2800	Cherry
	18		187			48	15		20		CS2000E	Cherry
			325			60	18		20		CS2500G	Cherry
	22		299			61	24		20	Photosensor on-chip	CS3500	Cherry
			479			88	36		20		CS3200L	Cherry
	24		437			96	36		20		CS3000F	Cherry
	25		695			123	52		20		CS3600	Cherry
	28		801			153	56		20		CS4000	Cherry
I²L	40		300	256					12	69 NPN/PNP transistors, ion implant resistors	CML1400	Cherry
			300	256					12	69 NPN/PNP transistors, 18 input/output cells	CS1400	Cherry
Custom Integrated Circuits BIP	10		38			25	8	33	20	1 cell, often used in multiples, PNPs have 4 collectors	MSA-1	CIC
	38		124			84	40	124	20	1 cell can be used in multiples	MSB-1	CIC
	50		800			561	164	725	20	15 cells	MSA-15	CIC
	56		148			168	80	148	20	2 cells	MSB-2	CIC
Exar BIP	14		110			23	8		20		**XR-C100**	**Exar (3386)**
	16		209			50	16		36		**XR-D100**	**Exar (3386)**
			260			60	18		20		**XR-A100**	**Exar (3386)**
			300			69	12		20		**XR-B100**	**Exar (3386)**
	18		200			48	15		20		**XR-E100**	**Exar (3386)**
			230			34	16		75	High voltage array	XR-X100	Exar
			260			38	12		20		**XR-J100**	**Exar (3386)**
			309			58	18		20		**XR-G100**	**Exar (3386)**
			401			75	22		20		**XR-H100**	**Exar (3386)**
	24		251			80	26		20		**XR-L100**	**Exar (3386)**
			472			93	36		20		**XR-F100**	**Exar (3386)**
	28		539			128	52	8	36	8 JFETs, ion implant resistors	**XR-V100**	**Exar (3386)**
			812			148	56		20		**XR-M100**	**Exar (3386)**
	40		901			208	68		36	8 JFETs, ion implant resistors	**XR-W100**	**Exar (3386)**
I²L	40		401	256		45	12		12	6 or 12V process	**XR400**	**Exar (3386)**
Ferranti Electric CML/RTL	25		908	100		407		2	5.5	Precision reference, shaping capacitors, 100 mA transistors, 1V operation	ULA1G	Ferranti
	28		1080	150		384			5.5	1V operation	ULA1L	Ferranti

(Continued)

[1] Delay conditions: 2-Input NAND driving 2 NANDs (FO = 2), 5V supply, 70°C, worst-case processing.

Master Selection Guide

CUSTOM/SEMICUSTOM

CUSTOM/SEMICUSTOM–Linear & Linear/Digital Arrays (Cont'd)

Manufacturer Technology	Total Bonding Pads	Linear: Dedicated Op Amps, A/D, etc.	Linear: Total Other Lin. Components	Digital: Equiv. 2-Input Gates	Digital: Gate Delay ns @ V	Uncommited Transistors NPN	Uncommited Transistors PNP	Number Capacitors	Supply Voltage, V	Comments	Device	Source
Linear & Linear/Digital Arrays												**(Cont'd)**
Ferranti Electric												(Cont'd)
CML/RTL	28		1390	160		647		2	5.5	Precision reference, shaping capacitors, 100 mA transistors, 1V operation	ULA2G	Ferranti
	30		1327	280		676			5.5	1V operation	ULA1U	Ferranti
	40		1920	340		715			5.5	1V operation	ULA2L	Ferranti
			2377	510		1280			5.5	1V operation	ULA2U	Ferranti
			2781	580		1589			5.5	1V operation	ULA3U	Ferranti
	48		4304	730		1644			5.5	1V operation	ULA5L	Ferranti
Holt												
CMOS	52	46		36				105	15	8-bit DAC, 11 op amps, 1 comparator, 22 flip-flops, 4 switched-capacitor filters	**HI3700**	**Holt (4745)**
Integrated Circuits												
BIP	14					22	8		20		IMC-20C	IntCirSys
	16					59	18		20		IMC-20A	IntCirSys
						50	16		40		IMC-400	IntCirSys
						62	13		40		IMC-40B	IntCirSys
	18					48	0		20		IMC-20E	IntCirSys
						60	0		20		IMC-20G	IntCirSys
						72	22		20		IMC-20H	IntCirSys
						38	0		20		IMC-20J	IntCirSys
	20					60	28		40		IMC-20B	IntCirSys
	24					96	0		20		IMC-20F	IntCirSys
						69	12		20		IMC-20L	IntCirSys
						80	0		20		IMC-40A	IntCirSys
						96	14		20		IMC	IntCirSys
Interdesign												
BIP	14		110			22	8		20		**MOC**	**Interdesign (4746)**
	16		194			50	16		36		**MOD**	**Interdesign (4746)**
			260			59	18		20		**MOA**	**Interdesign (4746)**
	18		170			38	12		20		**MOJ**	**Interdesign (4746)**
			187			48	15		20		**MOE**	**Interdesign (4746)**
			314			56	22		20		**MOQ**	**Interdesign (4746)**
			382			72	22		20		**MOH**	**Interdesign (4746)**
	20		310			60	18		20		**MOG**	**Interdesign (4746)**
	24		300			69	12		20		**MOB**	**Interdesign (4746)**
			416			80	26		20		**MOL**	**Interdesign (4746)**
			437			96	36		20		**MOF**	**Interdesign (4746)**
			571			72	57		20		**MOP**	**Interdesign (4746)**
	28		812			141	56		20		**MOM**	**Interdesign (4746)**
	40		1072			182	70		20		**MON**	**Interdesign (4746)**
CDI	40		2000	265		715			5.5		**MUA**	**Interdesign (4746)**
			2000	265		715			5.5		**MUB**	**Interdesign (4746)**
			2000	265		715			5.5		**MUC**	**Interdesign (4746)**
CMOS	42		930	199		414	398	84	15	16 dedicated flip-flops, switched capacitor array	**MLA**	**Interdesign (4746)**
MCE Semiconductor												
BIP	14					16	18	2	20	Power array	MCEP20A	MCE
			109			22	8		20		MCEA20C	MCE
			109			62	8		20		MCEA20CS	MCE
	16		194			100	16		40		MCEA40D	MCE
			194			50	16		40		MCEA40DS	MCE
			245			60	28		40		MCEA40AS	MCE
			259			59	18		20		MCEA20A	MCE
			259			59	18		20		MCEA20AS	MCE
	18		170			38	12		20		MCEA20J	MCE

(Continued)

† Military Temperature Range (−55° to 125°C)   * Typical Value

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CUSTOM/SEMICUSTOM–Linear & Linear/Digital Arrays (Cont'd)

Manufacturer / Technology	Total Bonding Pads	Linear: Dedicated Op Amps, A/D, etc.	Linear: Total Other Lin. Components	Digital: Equiv. 2-Input Gates	Digital: Gate Delay ns @ V	Uncommited Transistors: NPN	Uncommited Transistors: PNP	Number Capacitors	Supply Voltage, V	Comments	Device	Source
Linear & Linear/Digital Arrays												**(Cont'd)**
MCE Semiconductor												(Cont'd)
BIP	18		170			38	12		20		MCEA20JS	MCE
			187			48	15		20		MCEA20E	MCE
			187			48	15		20		MCEA20ES	MCE
			308			60	18		20		MCEA20G	MCE
			308			60	18		20		MCEA20GS	MCE
			382			72	22		20		MCEA20H	MCE
			382			74	22		20		MCEA20HS	MCE
	20		—			27	12		40	5 op amps, power array	MCEP40A	MCE
			218			62	10		40		MCEA40BS	MCE
	24		301			69	12		20		MCEA20B	MCE
			301			69	12		20		MCEA20BS	MCE
			416			80	26		20		MCEA20L	MCE
			416			80	26		20		MCEA20LS	MCE
			437			96	36		20		MCEA20F	MCE
			437			96	36		20		MCEA20FS	MCE
			464			96	36		20		MCEA20WS	MCE
	28					149	56		20		MCEA20M	MCE
			812			149	56		20		MCEA20MS	MCE
CMOS	18	2						2	8	2 op amps, dedicated logic	MGA255	† MCE
		2						2	12	2 op amps, dedicated logic	MGA255	† MCE
		2				8 @ 15			2	18	MGA255	† MCE
Plessey Semiconductor												
BIP	24		278			81	28		24		BAA1000	Plessey
			572			159	58		24		BAA2000	Plessey
Reticon												
NMOS	60	31						2500	± 11	14 filter sections, 3 extra op amps, 20 state cells, min. package size 25 pins, switched capacitor filter array	R5626	Reticon
Silicon Systems Inc.												
CMOS	28	24						396	15	12 op amps, 210 switches, 4 buffers, 8 flip-flops, switched capacitor filter array	**SCA-6**	**SiliconSys (3685,4872)**
	54	46						720	12	24 op amps, 456 switches, 6 buffers, 16 flip-flops, switched capacitor filter array	**SCA-12**	**SiliconSys (3685,4872)**
STC Microtechnology												
BIP	18		274			64	10		15	Ft=1.5 GHz	MSIV-1	STC
	26		548			128	20		15	Ft=1.5 GHz	MSIV-2	STC
	34		871			258	32	2	15		MSII	STC
	40		1056			256	40		15	Ft=1.5 GHz	MSIV-4	STC
Telmos												
CMOS	36			290	5			54	10	16 dedicated flip-flops, 8 op amps, 36 switches	**TM6005**	**Telmos (4877)**
	42			530	5			80	10	32 dedicated flip-flops, 16 op amps, 32 switches	**TM6001**	**Telmos (4877)**
	46			320	5			452	10	37 op amps, 100 switches	**TM6003**	**Telmos (4877)**
	55			740	5			232	10	40 dedicated flip-flops, 16 op amps, 100 switches	**TM6002**	**Telmos (4877)**
	62			800	5			244	10	32 dedicated flip-flops, 22 op amps, 104 switches	**TM6004**	**Telmos (4877)**

[1] Delay conditions: 2-Input NAND driving 2 NANDs (FO = 2), 5V supply, 70°C, worst-case processing.

CUSTOM/SEMICUSTOM–Standard Cells

Manufacturer Device Process Technology	Geometry (μm)	Interconnections Metal	Interconnections Poly	Delay 2-Input NAND Gate* (ns)	Cell Library Includes A/D	D/A	Op Amp	Core μP	RAM	ROM	PLA	Supply Voltage, V	Comments	Library or Process Name	Source
Standard Cells															
Alphatron CMOS, Si-Gate	3	1	1				x		x	x		3 to 6		ALPHAMAP	† Alphatron
	4	1	1				x		x	x		3 to 6	74LS MSI speeds	ALPHAMAP	† Alphatron
American Microsystems CMOS, Si-Gate	3	1	1	2.5								3 to 10		**CMOS Library**	**† AMI (4624)**
		2	1	2				x				3 to 10		**CMOS Library**	**† AMI (4624)**
	5	1	0	7				x				3 to 15		**CMOS Library**	**† AMI (4624)**
NMOS, Si-Gate	4	1	0	7								5		**NMOS Library**	**† AMI (4624)**
Array Technology CMOS, Si-Gate	3	1	1	4		x	x	x	x	x		±5		CMOS Library	† ArrayTech
NMOS, Si-Gate	4	1	1	6				x	x	x		3 to 7		NMOS Library	† ArrayTech
Barvon CMOS, Si-Gate	3	2		1.8	x	x	x	x	x	x	x	3 to 10	Core μP, 1Q84	**BHC Library**	**Barvon (4626)**
HMOS	3	2											Avail. 1Q84	**BHN Library**	**Barvon (4626)**
Circuit Technology CMOS, Si-Gate	4	1	1	5			x					3 to 10	200°C operation	CELLMOS	† CirTech
	5	1	1	6			x					3 to 15	200°C operation	CELLMOS	† CirTech
CMOS, SOS	3	1	1	3			x					3 to 10		CELLMOS	† CirTech
	4	1	1	4			x					4 to 12		CELLMOS	† CirTech
	5	1	1	5			x					4 to 16		CELLMOS	† CirTech
CMOS, Si-Gate 3	2					x		x	x			Avail. 1984		CMOS	Mostek
			1.8	x	x	x	x	x	x	x	3 to 10	Core μP, 1Q84		**BHC Library**	**Barvon (4626)**
Custom MOS Arrays CMOS, Metal-Gate	5	1			x	x	x		x	x	x	1.1 to 10	Low voltage and current	CMA1000 Series	CMA
CMOS, Si-Gate	3	1	1	3	x	x	x		x	x	x	2 to 7		CMOS Library	CMA
Fairchild Bipolar	3	2											Avail. 1H84	I³L	Fairchild
CMOS, Si-Gate	2	2	1										Avail. 1H84	CMOS Library	Fairchild
Fujitsu Microelectronics CMOS, Si-Gate	2.8	2	0	3.5					x	x		5		CMOS Library	Fujitsu
GTE Microcircuits CMOS, Si-Gate	3	2	2		x	x	x	x	x	x	x	5	Avail. 1Q84	ISO-CMOS Library	GTEMicro
	4	1	2	4.2				x	x	x	x	5		ISO-CMOS Library	GTEMicro
	5	1	2	5.2								5		ISO-CMOS Library	GTEMicro

† Military Temperature Range (−55° to 125°C)

* Typical Value

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CUSTOM/SEMICUSTOM–Standard Cells (Cont'd)

Manufacturer Device Process Technology	Geometry (µm)	Interconnections Metal	Interconnections Poly	Delay 2-Input NAND Gate¹ (ns)	A/D	D/A	Op Amp	Core µP	RAM	ROM	PLA	Supply Voltage, V	Comments	Library or Process Name	Source
Standard Cells															**(Cont'd)**
Harris Semiconductor CMOS, Si-Gate	3	1	1	3.8								1.5 to 7		**SAJI-IV**	**† Harris (4744)**
Hughes Aircraft CMOS, Si-Gate	2.5											4 to 10		HCMOS Library	† Hughes
Integrated Circuit Systems CMOS, Metal-Gate	7.5	1		30					x			5 to 18		CMOS Library	† IntCirSys
CMOS, Si-Gate	3	1	1	4					x			5		CMOS Library	† IntCirSys
	5	1	1	10					x			5 to 10		CMOS Library	† IntCirSys
NMOS, Metal-Gate	4.5	1		20				x	x	x	x	5 to 10		NMOS Library	† IntCirSys
	5	1	1	20					x	x	x	5 to 10		NMOS Library	† IntCirSys
Intel CMOS, Si-Gate	2	1	1	1.0				x	x	x	x	5	Currently in Beta sites	CHMOS-1 Library	Intel
Intersil CMOS, Si-Gate	3	2	1	<2								2 to 10	Avail. 1984	CMOS Library	Intersil
Int'l Microcircuits CMOS, Si-Gate	3	2	1	2	x	x	x		x	x	x	3.5 to 8		**CMOS Library**	**IntlMicCir (4747)**
Int'l Microelectronic Prod CMOS, Si-Gate	3	2		2.5	x	x	x		x	x	x	5		**Impel Library**	**† IMP (4749)**
	5	1	1									3 to 12		**Impel library**	**† IMP (4749)**
	3		2		x	x	x		x	x	x	5		**Impel library**	**† IMP (4749)**
Master Logic CMOS, Metal-Gate	4	1		15	x	x	x					2 to 7		MALV Series	† MasterLogic
CMOS, Si-Gate	4	1		3	x	x						2 to 7		MASG Series	† MasterLogic
MCE Semiconductor Bipolar, J. I.	5	1	1	12.5	x	x	x					to 75	Library includes some 75V devices	UniCELL	† MCE
CMOS, Metal-Gate	5	1		10			x					1 to 18		UniCELL MGA	† MCE
CMOS, Si-Gate	3.5	1	1	4.5			x					3 to 6		ULA Series	† MCE
Microcircuit Technology NMOS, Si-Gate	3	1	1						x	x	x	5		NMOS Library	MicroTech
CMOS, Si-Gate	3	1	1						x	x	x	3 to 7		CMOS Library	MicroTech
Mostek CMOS, Si-Gate	3	2					x		x	x			Avail. 1984	CMOS Library	Mostek

¹ Delay conditions: 2-Input NAND driving 2 NANDs (FO = 2), 5V supply, 70°C, worst-case processing.

CUSTOM/SEMICUSTOM–Standard Cells (Cont'd)

Manufacturer Device Process Technology	Geometry (µm)	Interconnections Metal	Poly	Delay 2-Input NAND Gate* (ns)	Cell Library Includes A/D	D/A	Op Amp	Core µP	RAM	ROM	PLA	Supply Voltage, V	Comments	Library or Process Name	Source	
Standard Cells																**(Cont'd)**
NCM Corp CMOS, Metal-Gate	7.5	1	0	20			x		x	x	x	1.5 to 15		2000 Series	† NCM	
CMOS, Si-Gate	5	1	1	8.5			x		x	x	x	1.5 to 15		4000 Series	† NCM	
NCR Corp CMOS, Si-Gate	3	1	1	4					x	x	x	3 to 6		CMOS-2 Library	NCR	
NMOS, Si-Gate	4	1	1	6					x	x	x	5		VLSI-1	NCR	
Nitron CMOS, Metal-Gate	5	1		20	x	x	x				x	5 to 15		Nitrochip	† Nitron	
CMOS, Si-Gate	5	1		5	x	x	x				x	3 to 10		Nitrochip	† Nitron	
Plessey Semiconductor CMOS, Si-Gate	2.5	2		1.4	x	x	x	x	x	x	x	3 to 7		**CMOS**	**Plessey**	**(4821)**
	5	1	1	6	x	x	x					3 to 7		CMOS	Plessey	
NMOS	5	1		20								5		CMOS	Plessey	
RCA Solid State CMOS, Si-Gate	3	1	1	5			x					3 to 7		**PsCMOS-2**	**RCA**	**(4824)**
	5	1	1	10			x					3 to 7		**PsCMOS-1**	**RCA**	**(4824)**
	7	1	1	20			x					3 to 12		**PsCMOS-C2L**	**RCA**	**(4824)**
CMOS, SOS	3	1	1	4			x					3 to 12		**SOS-2 Library**	**RCA**	**(4824)**
	5	1	1	8			x					3 to 12		**SOS-1 Library**	**RCA**	**(4824)**
SGS-ATES Bipolar, MTL²V	6	2		25		x	x		x	x		2 to 10		Zodiac	SGS	
Signetics Bipolar	5	2		3.5								5	Medium power	**EPL-1**	**† Signetics**	**(4855)**
		2		5								5	Low power	**EPL-2**	**† Signetics**	**(4855)**
		2		6								5		**ISL**	**† Signetics**	**(4855)**
CMOS, Si-Gate	3	2	1	8								2 to 6	High Speed	INTER	Signetics	
	4	1	1	8								3 to 15	Medium Speed	INTER	Signetics	
Silicon Systems CMOS, Si-Gate	3	2	1	3	x	x	x	x	x	x	x	5		CMOS Library	SiliconSys	
Siliconix CMOS, Si-Gate	3	2	2	3		x	x		x	x		3 to 6	Avail. 4Q83	ISO-3 Library	Siliconix	
	5	2	2	5.5		x	x		x	x		3 to 14		ISO-5 Library	Siliconix	
Synertek CMOS, Si-Gate	3	1	1	8				x	x	x		3 to 6		**HCMOS Library**	**† Synertek**	**(4874)**
Texas Instruments CMOS, Si-Gate	3	1	1	4								5	Avail. 4Q83	**CMOS Library**	**TI**	**(4882)**
VLSI Technology CMOS, Si-Gate	3	2	1	5				x	x	x	x	5	Configurable cells	**CMOS Library**	**VTI**	**(4931)**
HMOS	3	1	1	4				x	x	x	x	5	Configurable cells	**HMOS Library**	**VTI**	**(4931)**

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

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CUSTOM/SEMICUSTOM

CUSTOM/SEMICUSTOM–Standard Cells (Cont'd)

Manufacturer Device Process Technology	Geometry (µm)	Interconnections Metal	Interconnections Poly	Delay 2-Input NAND Gate[1] (ns)	Cell Library Includes A/D	D/A	Op Amp	Core µP	RAM	ROM	PLA	Supply Voltage, V	Comments	Library or Process Name	Source	Line
Standard Cells																**(Cont'd)**
ZyMOS CMOS, Metal-Gate	6	1	1	12.2								1.1 to 6		Zy20000	† ZyMOS	
CMOS, Si-Gate	3	1	1	1.6				x	x	x	x	1.1 to 5.5		Zy50000	† ZyMOS	
	5	1	1	5.8	x	x	x	x	x	x	x	1.1 to 5.5		Zy40000	† ZyMOS	

[1] Delay conditions: 2-Input NAND driving 2 NANDs (FO = 2), 5V supply, 70°C, worst-case processing.

CUSTOM/SEMICUSTOM–Programmable Logic

Programmable Logic

Organization	Propagation Time	Output	Supply Voltage, V	Device	Source
Field Programmable Array Logic	—	TS	5	SN54PL20L8 †	TI (4903,4914)
				SN54PL20R4 †	TI (4903,4914)
				SN54PL20R6 †	TI (4904,4914)
				SN54PL20R8 †	TI (4904,4914)
				SN54PLR19L8 †	TI (4906,4922)
				SN54PLR19R4 †	TI (4906,4922)
				SN54PLR19R6 †	TI (4907,4922)
				SN54PLR19R8 †	TI (353,4907,4922)
				SN54PLT19L8 †	TI (353,4908,4926)
				SN54PLT19R4 †	TI (353,4908,4926)
				SN54PLT19R6 †	TI
				SN54PLT19R8 †	TI (353,4909,4926)
				SN74PL20L8	TI (4903,4914)
				SN74PL20R4	TI (4903,4914)
				SN74PL20R6	TI (4904,4914)
				SN74PL20R8	TI (4904,4914)
				SN74PLR19L8	TI (4906,4922)
				SN74PLR19R4	TI (4906,4922)
				SN74PLR19R6	TI (353,4907,4922)
				SN74PLR19R8	TI (353,4907,4922)
				SN74PLT19L8	TI (353,4908,4926)
				SN74PLT19R4	TI (353,4908,4926)
				SN74PLT19R6	TI (353,4909,4926)
				SN74PLT19R8	TI (353,4909,4926)
	25 nsF	TS	5	AMPAL16H8AC	AMD (4600)
				AMPAL16HD8AC	AMD (4600)
				AMPAL16L8AC	AMD (4600)
				AMPAL16LD8AC	AMD (4600)
				AMPAL16R4AC	AMD (4600)
				AMPAL16R6AC	AMD (4600)
				AMPAL16R8AC	AMD (4600)
				AMPAL22V10A	AMD (4600)
				PAL16L8AC	MMI (4768)
				PAL16R4AC	MMI (4768)
				PAL16R6AC	MMI (4768)
				PAL16R8AC	MMI (4768)
				PAL20L8AC	MMI (4768)
				PAL20R4AC	MMI (4768)
				PAL20R6AC	MMI (4768)
				PAL20R8AC	MMI (4768)
				DMPAL10H8AC	National
				DMPAL10L8AC	National
				DMPAL12H6AC	National
				DMPAL12L6AC	National
				DMPAL14H4AC	National
				DMPAL16C1AC	National
				DMPAL16H2AC	National
				DMPAL16L2AC	National
				DMPAL16L8AC	National
				DMPAL16R4AC	National
				DMPAL16R6AC	National
				DMPAL16R8AC	National
				DMPL14L4AC	National
				SN74ALS16R4-1	TI
				SN74PL16L8-1	TI (4901,4910)
				SN74PL16R4-1	TI (4901,4910)
				SN74PL16R6-1	TI (4902,4910)
				SN74PL16R8-1	TI (4902,4910)
	30 nsF	TS	5	AMPAL16H8AM †	AMD (4600)
				(Continued)	
Field Programmable Array Logic	30 nsF	TS	5	(Cont'd)	
				AMPAL16HD8AM †	AMD (4600)
				AMPAL16L8AM †	AMD (4600)
				AMPAL16LD8AM †	AMD (4600)
				AMPAL16R4AM †	AMD (4600)
				AMPAL16R6AM †	AMD (4600)
				AMPAL16R8AM †	AMD (4600)
				PAL16L8AM †	MMI (4768)
				PAL16R4AM †	MMI (4768)
				PAL16R6AM †	MMI (4768)
				PAL16R8AM †	MMI (4768)
				PAL20L8AM †	MMI (4768)
				PAL20R4AM †	MMI (4768)
				PAL20R6AM †	MMI (4768)
				PAL20R8AM †	MMI (4768)
				DMPAL10H8AM †	National
				DMPAL10L8AM †	National
				DMPAL12H6AM †	National
				DMPAL12L6AM †	National
				DMPAL14H4AM †	National
				DMPAL14L4AM †	National
				DMPAL16C1AM †	National
				DMPAL16H2AM †	National
				DMPAL16L2AM †	National
				DMPAL16L8AM †	National
				DMPAL16R4AM †	National
				DMPAL16R6AM †	National
				DMPAL16R8AM †	National
				SN54ALS16R4-1 †	TI
				SN54PL16L8-1 †	TI (4901,4910)
				SN54PL16R4-1 †	TI (4901,4910)
				SN54PL16R6-1 †	TI (4902,4910)
				SN54PL16R8-1 †	TI (4902,4910)
	35 nsF	TS	5	AMPAL16H8C	AMD (4600)
				AMPAL16H8LC	AMD (4600)
				AMPAL16HD8C	AMD (4600)
				AMPAL16HD8LC	AMD (4600)
				AMPAL16L8C	AMD (4600)
				AMPAL16L8LC	AMD (4600)
				AMPAL16LD8C	AMD (4600)
				AMPAL16LD8LC	AMD (4600)
				AMPAL16R4C	AMD (4600)
				AMPAL16R4LC	AMD (4600)
				AMPAL16R6C	AMD (4600)
				AMPAL16R6LC	AMD (4600)
				AMPAL16R8C	AMD (4600)
				AMPAL16R8LC	AMD (4600)
				AMPAL22V10	AMD (4600)
				HPL77209-5	Harris (3958)
				HPL77209/16L8-5	Harris (3958)
				HPL77215/16H8-5	Harris (3958)
				HPL77216/16P8-5	Harris (3958)
				HPL77317/16LD8-5	Harris (3959)
				HPL77318/16HD8-5	Harris (3959)
				HPL77319-5	Harris (3960)
				(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

Master Selection Guide

CUSTOM/SEMICUSTOM

CUSTOM/SEMICUSTOM–Programmable Logic (Cont'd)

Programmable Logic (Cont'd)

Organization	Propagation Time	Output	Supply Voltage, V	Device	Source	
Field Programmable Array Logic	35 nsF	TS	5			(Cont'd)
				HPL77320-5	Harris	(3960)
				PAL10H8C	MMI	(4768)
				PAL10L8C	MMI	(4768)
				PAL12H6C	MMI	(4768)
				PAL12L6C	MMI	(4768)
				PAL14H4C	MMI	(4768)
				PAL14L4C	MMI	(4768)
				PAL16H2C	MMI	(4768)
				PAL16L2C	MMI	(4768)
				PAL16L8A-2C	MMI	(4768)
				PAL16L8C	MMI	(4768)
				PAL16R4A-2C	MMI	(4768)
				PAL16R4C	MMI	(4768)
				PAL16R6A-2C	MMI	(4768)
				PAL16R6C	MMI	(4768)
				PAL16R8A-2C	MMI	(4768)
				PAL16R8C	MMI	(4768)
				DMPAL10H8C	National	
				DMPAL10L8C	National	
				DMPAL12H6C	National	
				DMPAL12L6C	National	
				DMPAL14H4C	National	
				DMPAL14L4C	National	
				DMPAL16C1C	National	
				DMPAL16H2C	National	
				DMPAL16L2C	National	
				DMPAL16L8C	National	
				DMPAL16R4C	National	
				DMPAL16R6C	National	
				DMPAL16R8C	National	
	40 nsF	TS	5	AMPAL16H8LM	† AMD	(4600)
				AMPAL16H8M	† AMD	(4600)
				AMPAL16HD8LM	† AMD	(4600)
				AMPAL16HD8M	† AMD	(4600)
				AMPAL16L8LM	† AMD	(4600)
				AMPAL16L8M	† AMD	(4600)
				AMPAL16LD8LM	† AMD	(4600)
				AMPAL16LDM	† AMD	
				AMPAL16R4LM	† AMD	(4600)
				AMPAL16R4M	† AMD	(4600)
				AMPAL16R6LM	† AMD	(4600)
				AMPAL16R6M	† AMD	(4600)
				AMPAL16R8LM	† AMD	(4600)
				AMPAL16R8M	† AMD	(4600)
				PAL12L10C	MMI	(4768)
				PAL12L10M	† MMI	(4768)
				PAL14L8C	MMI	(4768)
				PAL14L8M	† MMI	(4768)
				PAL16A4C	MMI	(4768)
				PAL16C1C	MMI	(4768)
				PAL16L6C	MMI	(4768)
				PAL16L6M	† MMI	(4768)
				PAL16X4C	MMI	(4768)
				PAL18L4C	MMI	(4768)
				PAL18L4M	† MMI	(4768)
				PAL20C1C	MMI	(4768)
				PAL20C1M	† MMI	(4768)
				PAL20L2C	MMI	(4768)
				PAL20L2M	† MMI	(4768)
				DMPAL12L10C	National	
				DMPAL12L10M†	National	
				DMPAL14L8C	National	
				DMPAL14L8M†	National	
				DMPAL16L6C	National	
				DMPAL16L6M†	National	
				DMPAL18L4C	National	
				DMPAL18L4M†	National	
				DMPAL20C1C	National	
Field Programmable Array Logic	40 nsF	TS	5			(Cont'd)
				DMPAL20C1M†	National	
				DMPAL20L2C	National	
				DMPAL20L2M†	National	
	45 nsF	TS	5	HPL77209-2	† Harris	(3958)
				HPL77209/16L8-2	† Harris	(3958)
				HPL77215/16H8-2	† Harris	(3958)
				HPL77216/16P8-2	† Harris	(3958)
				HPL77317-2	† Harris	(3959)
				HPL77318-2	† Harris	(3959)
				HPL77319-2	† Harris	(3960)
				PAL10H8M	† MMI	(4768)
				PAL10L8M	† MMI	(4768)
				PAL12H6M	† MMI	(4768)
				PAL12L6M	† MMI	(4768)
				PAL14H4M	† MMI	(4768)
				PAL14L4M	† MMI	(4768)
				PAL16A4M	† MMI	(4768)
				PAL16C1M	† MMI	(4768)
				PAL16H2M	† MMI	(4768)
				PAL16L2M	† MMI	(4768)
				PAL16L8M	† MMI	(4768)
				PAL16R4M	† MMI	(4768)
				PAL16R6M	† MMI	(4768)
				PAL16R8M	† MMI	(4768)
				PAL16X4M	† MMI	(4768)
				DMPAL10H8M†	National	
				DMPAL10L8M†	National	
				DMPAL12H6M†	National	
				DMPAL12L6M†	National	
				DMPAL14H4M†	National	
				DMPAL14L4M†	National	
				DMPAL16C1M†	National	
				DMPAL16H2M†	National	
				DMPAL16L2M†	National	
				DMPAL16L8M†	National	
				DMPAL16R4M†	National	
				DMPAL16R6M†	National	
				DMPAL16R8M†	National	
	50 nsF	TS	5	PAL16L8-2C	MMI	(4768)
				PAL16L8A-2M	† MMI	(4768)
				PAL16R4-2C	MMI	(4768)
				PAL16R4A-2M	† MMI	(4768)
				PAL16R6-2C	MMI	(4768)
				PAL16R6A-2M	† MMI	(4768)
				PAL16R8-2C	MMI	(4768)
				PAL16R8A-2M	† MMI	(4768)
				PAL20L10M	† MMI	(4768)
				PAL20X10M	† MMI	(4768)
				PAL20X4M	† MMI	(4768)
				PAL20X8M	† MMI	(4768)
				DMPAL209X4C	National	
				DMPAL20L10C	National	
				DMPAL20X10C	National	
				DMPAL20X8C	National	
	55 nsF	TS	5	PAL16L8A-4C	MMI	(4768)
				PAL16R4A-4C	MMI	(4768)
				PAL16R6A-4C	MMI	(4768)
				PAL16R8A-4C	MMI	(4768)
	60 nsF	TS	5	PAL10H3-2C	MMI	
				PAL10L8-2C	MMI	(4768)
				PAL12H6-2C	MMI	(4768)
				PAL12L6-2C	MMI	(4768)
				PAL14H4-2C	MMI	(4768)
				PAL14L4-2C	MMI	(4768)
				PAL16C1-2C	MMI	(4768)
				PAL16H2-2C	MMI	(4768)

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

CUSTOM/SEMICUSTOM–Programmable Logic (Cont'd)

Programmable Logic (Cont'd)

Organization	Propagation Time	Output	Supply Voltage, V	Device	Source
Field Programmable Array Logic					
	60 nsF	TS	5		(Cont'd)
				PAL16L2-2C	**MMI (4768)**
				PAL20L10C	**MMI (4768)**
				PAL20X10C	**MMI (4768)**
				PAL20X4C	**MMI (4768)**
				PAL20X8C	**MMI (4768)**
				DMPAL20L10M	National
				DMPAL20X10M	National
				DMPAL20X4M	National
				DMPAL20X8M	National
	65 nsF	TS	5	**PAL16L8-2M**	**† MMI (4768)**
				PAL16R4-2M	**† MMI (4768)**
				PAL16R6-2M	**† MMI (4768)**
				PAL16R8-2M	**† MMI (4768)**
	75 nsF	TS	5	**PAL16L8A-4M**	**† MMI (4768)**
				PAL16R4A-4M	**† MMI (4768)**
				PAL16R6A-4M	**† MMI (4768)**
				PAL16R8A-4M	**† MMI (4768)**
	80 nsF	TS	5	PAL10H-2M	† MMI
				PAL10L8-2M	**† MMI (4768)**
				PAL12H6-2M	**† MMI (4768)**
				PAL12L6-2M	**† MMI (4768)**
				PAL14H4-2M	**† MMI (4768)**
				PAL14L4-2M	**† MMI (4768)**
				PAL16C1-2M	**† MMI (4768)**
				PAL16H2-2M	**† MMI (4768)**
				PAL16L2-2M	**† MMI (4768)**
				PAL16L8-4C	**MMI (4768)**
				PAL16R4-4C	**MMI (4768)**
				PAL16R6-4C	**MMI (4768)**
				PAL16R8-4C	**MMI (4768)**
	100 nsF	TS	5	**PAL16L8-4M**	**† MMI (4768)**
				PAL16R4-4M	**† MMI (4768)**
				PAL16R6-4M	**† MMI (4768)**
				PAL16R8-4M	**† MMI (4768)**
Field Programmable Array Logic, CMOS					
	90 nsF	TS	5	HPL16LC8-2	† Harris
				HPL16LC8-9	† Harris
				HPL16RC4-2	† Harris
				HPL16RC4-9	† Harris
				HPL16RC6-2	† Harris
				HPL16RC6-9	† Harris
				HPL16RC8-2	† Harris
				HPL16RC8-9	† Harris
Field Programmable Gate Array, 16 Inputs, 9 AND/NAND Gates, 9 Outputs					
	35 nsF	OC	5	**N82S102**	**Signetics (4155)**
		TS	5	**N82S103**	**Signetics (4155)**
	55 nsF	OC	5	**S82S102**	**† Signetics (532,4155)**
		TS	5	**S82S103**	**† Signetics (532,4155)**
Field Programmable Gate Array, 6 Inputs, 12 AND Gates, 12 I/O Lines					
	20 ns*	OC	5	**S82S150**	**† Signetics (532)**
		TS	5	**S82S151**	**† Signetics (532,4144)**
	25 nsF	OC	5	N82S150	Signetics
		TS	5	**N82S151**	**Signetics (4144)**
Field Programmable Identity Comparator, 12-Bit					
	—	—	5	**SN54ALS528**	**† TI (1046)**
				SN74ALS528	**TI (1046)**
Field Programmable Identity Comparator, 16-Bit					
	—	—	5	**SN54ALS526**	**† TI (1045)**
				SN74ALS526	**TI (1045)**
Field Programmable Identity Comparator, 8-Bit and 4-Bit Comparator					
	—	—	5	**SN54ALS527**	**† TI (1045)**
				SN74ALS527	**TI (1045)**
Field Programmable Logic Array, 14 Inputs, 32 Product Terms, Six Sum Terms					
	10 ns *	OC	5	**SN54PL840**	**† TI (4905,4918)**
				SN74PL840	**TI (4905,4918)**
		TS	5	**SN54PL839**	**† TI (4905,4918)**
				SN74PL839	**TI (4905,4918)**
Field Programmable Logic Array, 16 Inputs, 48 Product Terms, 8 Outputs					
	50 nsF	OC	5	MC82S101C	Motorola
				N82S101	**Signetics (4153)**
		TS	5	MC82S100C	Motorola
				N82S100	**Signetics (4153)**
	80 nsF	OC	5	MC82S101M	† Motorola
				S82S101	**† Signetics (532,4153)**
		TS	5	MC82S100M	† Motorola
				S82S100	**† Signetics (532,4153)**
Field Programmable Logic Array, 24 Inputs, 72 Product Terms, 16 Outputs					
	200 nsF	TS	5	μPB450	NEC
Field Programmable Logic Array, 48 Product Terms, 14 Inputs	100 nsF	OC	5	IM5200	Intersil
Field Programmable Logic Array, 8 Inputs, 32 AND Gates, 10 OR Gates, 10 I/O Lines					
	30 nsF	OC	5	N82S152A	Signetics
		TS	5	**N82S153A**	**Signetics (4146,4146)**
	40 nsF	OC	5	N82S152	Signetics
		TS	5	**HPL77153-5**	**Harris (3957)**
				N82S153	**Signetics (4146)**
	45 nsF	OC	5	S82S152A	† Signetics
		TS	5	**S82S153A**	**† Signetics (532,4146,4146)**
	55 nsF	OC	5	S82S152	† Signetics
		TS	5	**HPL77153-2**	**† Harris (3957)**
				S82S153	**† Signetics (532,4146)**
Field Programmable Logic Element (PROM), 1024x4					
	35 nsF	TS	5	**63S441A**	**MMI (4026)**
	50 nsF	TS	5	**53S441A**	**† MMI (4026)**
Field Programmable Logic Element (PROM), 2048x4					
	35 nsF	TS	5	**63S841A**	**MMI (4026)**
	50 nsF	TS	5	**53S841A**	**† MMI (4026)**
Field Programmable Logic Element (PROM), 32x8					
	25 nsF	TS	5	**63S080**	**MMI (4026)**
				63S081	**MMI (4026)**
	35 nsF	OC	5	**53S080**	**† MMI (4026)**
		TS	5	**53S081**	**† MMI (4026)**
Field Programmable Logic Element (PROM), 4096x4					
	35 nsF	TS	5	**63S1641A**	**MMI (4026)**
	50 nsF	TS	5	**53S1641A**	**† MMI (4026)**
Field Programmable Logic Sequencer, 12 Inputs, 32 Product Terms, 6 Outputs					
	45 nsF *	OC	5	SN54PL335	† TI
				SN74PL335	TI
		TS	5	SN54PL333	† TI
				SN74PL333	TI
Field Programmable Logic Sequencer, 12 Inputs, 50 Product Terms, 6 Outputs					
	35 ns *	—	5	SN74S331	TI
		TS	5	SN74S330	TI

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

Master Selection Guide

CUSTOM/SEMICUSTOM

CUSTOM/SEMICUSTOM–Programmable Logic (Cont'd)

Organization	Propagation Time	Output	Supply Voltage, V	Device	Source
Programmable Logic (Cont'd)					
Field Programmable Logic Sequencer, 16 Inputs, 48 Transition Terms, 8 Outputs					
	60 nsF	OC	5	N82S104A	Signetics
				S82S104A	**† Signetics (532)**
		TS	5	**N82S105A**	**Signetics (4157)**
				S82S105A	**† Signetics (532,4157)**
	90 nsF	OC	5	N82S104	Signetics
				S82S104	**† Signetics (532)**
		TS	5	N82S105	Signetics
				S82S105	**† Signetics (532)**
Field Programmable Logic Sequencer, 4 Inputs, 32 AND Gates, 21 OR Gates, 4 I/O Lines					
	35 ns *	OC	5	**S82S158**	**† Signetics (532)**
		TS	5	**S82S159**	**† Signetics (532,4148)**
	40 nsF	OC	5	N82S158	Signetics
		TS	5	~~**N82S159**~~	~~Signetics (4148)~~
Field Programmable Logic Sequencer, 4 Inputs, 32 AND Gates, 21 OR Gates, 6 I/O Lines					
	35 ns *	OC	5	**S82S156**	**† Signetics (532)**
		TS	5	**S82S157**	**† Signetics (532)**
	40 nsF	OC	5	N82S156	Signetics
		TS	5	N82S157	Signetics
Field Programmable Logic Sequencer, 4 Inputs, 32 AND Gates, 21 OR Gates, 8 I/O Lines					
	35 ns *	OC	5	**S82S154**	**† Signetics (532)**
		TS	5	**S82S155**	**† Signetics (532)**
	40 nsF	OC	5	N82S154	Signetics
		TS	5	N82S155	Signetics
Field Programmable Multiplexer, (10 inputs, four 10x8 programmable arrays, four 8:1 addressable multiplexers, four outputs)					
	55 nsF	TS	5	29693C	Raytheon
	75 nsF	TS	5	29693M	† Raytheon
Hard Array Logic					
	25 nsF	TS	5	**HAL16L8AC**	**MMI (4776,4784,4786)**
				HAL16R4AC	**MMI (4776,4784,4786)**
				HAL16R6AC	**MMI (4776,4784,4786)**
				HAL16R8AC	**MMI (4776,4784,4786)**
				HAL20L8AC	**MMI (4776,4787)**
				HAL20R4AC	**MMI (4776,4787)**
				HAL20R6AC	**MMI (4776,4787)**
				HAL20R8AC	**MMI (4776,4787)**
	30 nsF	TS	5	**HAL20L8AM**	**† MMI (4776)**
				HAL20R4AM	**† MMI (4776)**
				HAL20R6AM	**† MMI (4776)**
				HAL20R8AM	**† MMI (4776)**
	35 nsF	TS	5	C-HAL16L8	MMI
				C-HAL16R4	MMI
				C-HAL16R6	MMI
				C-HAL16R8	MMI
				HAL10H8C	**MMI (4776,4782)**
				HAL10L8C	**MMI (4776,4782)**
				HAL12H6C	**MMI (4776,4782)**
				HAL12L6C	**MMI (4776,4782)**
				HAL14H4C	**MMI (4776,4782)**
				HAL14L4C	**MMI (4776,4782)**
				HAL16H2C	**MMI (4776,4782)**
				HAL16L2C	**MMI (4776,4782)**
				HAL16L8C	**MMI (4776,4784)**
				HAL16R4C	**MMI (4776,4784)**
				HAL16R6C	**MMI (4776,4784)**
				HAL16R8C	**MMI (4776,4784)**

(Continued)

Organization	Propagation Time	Output	Supply Voltage, V	Device	Source
Hard Array Logic					(Cont'd)
	35 nsF	TS	5	**SP810H8**	**SPI (4826)**
				SP810L8	**SPI (4826)**
				SP812H6	**SPI (4826)**
				SP812L6	**SPI (4826)**
				SP814H4	**SPI (4826)**
				SP814L4	**SPI (4826)**
				SP816H2	**SPI (4826)**
				SP816L2	**SPI (4826)**
				SP816L8	**SPI (4826)**
				SP816R4	**SPI (4826)**
				SP816R6	**SPI (4826)**
				SP816R8	**SPI (4826)**
				FCT20x4	**Si-Fab (4827)**
				HCT10H8	**Si-Fab (4827)**
				HCT10L8	**Si-Fab (4827)**
				HCT12L10	**Si-Fab (4827)**
				HCT12L8	**Si-Fab (4827)**
				HCT14H4	**Si-Fab (4827)**
				HCT14L4	**Si-Fab (4827)**
				HCT14L8	**Si-Fab (4827)**
				~~**HCT16A4**~~	~~**Si-Fab (4827)**~~
				HCT16C1	**Si-Fab (4827)**
				HCT16H2	**Si-Fab (4827)**
				HCT16L2	**Si-Fab (4827)**
				HCT16L6	**Si-Fab (4827)**
				HCT16L8	**Si-Fab (4827)**
				HCT16R4	**Si-Fab (4827)**
				HCT16R6	**Si-Fab (4827)**
				HCT16R8	**Si-Fab (4827)**
				HCT16X4	**Si-Fab (4827)**
				HCT18L4	**Si-Fab (4827)**
				HCT20C1	**Si-Fab (4827)**
				HCT20L10	**Si-Fab (4827)**
				HCT20L2	**Si-Fab (4827)**
				HCT20x10	**Si-Fab (4827)**
				HCT20x8	**Si-Fab (4827)**
				ZX-CAL10H8	Zytrex
				ZX-CAL10L8	Zytrex
				ZX-CAL12H6	Zytrex
				ZX-CAL12L6	Zytrex
				ZX-CAL14H4	Zytrex
				ZX-CAL14L4	Zytrex
				ZX-CAL16H2	Zytrex
				ZX-CAL16L2	Zytrex
				ZX-CAL16L8	Zytrex
				ZX-CAL16R4	Zytrex
				ZX-CAL16R6	Zytrex
				ZX-CAL16R8	Zytrex
	40 nsF	TS	5	**HAL12L10C**	**MMI (4776,4783)**
				HAL14L8C	**MMI (4776,4783)**
				HAL16A4C	**MMI (4776,4784)**
				HAL16C1C	**MMI (4776,4782)**
				HAL16L6C	**MMI (4776,4783)**
				HAL16X4C	**MMI (4776,4784)**
				HAL18L4C	**MMI (4776,4783)**
				HAL20C1C	**MMI (4776,4783)**
				HAL20L2C	**MMI (4776,4783)**
				SP816C1	**SPI (4826)**
	45 nsF	TS	5	**HAL10H8M**	**† MMI (4776,4782)**
				HAL10L8M	**† MMI (4776,4782)**
				HAL12H6M	**† MMI (4776,4782)**
				HAL12L10M	**† MMI (4776,4783)**
				HAL12L6M	**† MMI (4776,4782)**
				HAL14H4M	**† MMI (4776,4782)**
				HAL14L4M	**† MMI (4776,4782)**
				HAL16A4M	**† MMI (4776,4784)**
				HAL16C1M	**† MMI (4776,4782)**
				HAL16H2M	**† MMI (4776,4782)**
				HAL16L2M	**† MMI (4776,4782)**

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

CUSTOM/SEMICUSTOM–Programmable Logic (Cont'd)

Programmable Logic (Cont'd)

Organization	Propagation Time	Output	Supply Voltage, V	Device	Source
Hard Array Logic					
	45 nsF	TS	5		(Cont'd)
				HAL16L6M	† **MMI** (4776,4783)
				HAL16L8M	† **MMI** (4776,4784)
				HAL16R4M	† **MMI** (4776,4784)
				HAL16R6M	† **MMI** (4776,4784)
				HAL16R8M	† **MMI** (4776,4784)
				HAL16X4M	† **MMI** (4776,4784)
				HAL18L4M	† **MMI** (4776,4783)
				HAL20L2M	† **MMI** (4776,4783)
				HAL24L8M	† MMI
	50 nsF	TS	5	**HAL16L8-2C**	**MMI** (4776,4784,4789)
				HAL16R4-2C	**MMI** (4776,4784,4789)
				HAL16R6-2C	**MMI** (4776,4784,4789)
				HAL16R8-2C	**MMI** (4776,4784,4789)
				HAL20L10C	**MMI** (4776,4785)
				HAL20X10C	**MMI** (4776,4785)
				HAL20X4C	**MMI** (4776,4785)
				HAL20X8C	**MMI** (4776,4785)
	60 nsF	TS	5	**HAL10H8-2C**	**MMI** (4776,4782,4788)
				HAL10L8-2C	**MMI** (4776,4782,4788)
				HAL12H6-2C	**MMI** (4776,4782,4788)
				HAL12L6-2C	**MMI** (4776,4782,4788)
				HAL14H4-2C	**MMI** (4776,4782,4788)
				HAL14L4-2C	**MMI** (4776,4782,4788)
				HAL16C1-2C	**MMI** (4776,4782,4788)
				HAL16H2-2C	**MMI** (4776,4782)
				HAL16L2-2C	**MMI** (4776,4782,4788)
				HAL20C1M	† **MMI** (4776,4783)
				HAL20L10M	† **MMI** (4776,4785)
				HAL20X10M	† **MMI** (4776,4785)
				HAL20X4M	† **MMI** (4776,4785)
				HAL20X8M	† **MMI** (4776,4785)
	75 nsF	TS	5	**HAL16L8-4C**	**MMI** (4776,4784,4790)
				HAL16R4-4C	**MMI** (4776,4784,4790)
				HAL16R6-4C	**MMI** (4776,4784,4790)
				HAL16R8-4C	**MMI** (4776,4784,4790)
Programmed at Factory, 14 Inputs, 96 Product Terms					
	150 nsF	—	5	DM7575	† National
				DM7576	† National
				DM8575	National
				DM8576	National

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

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ABBREVIATIONS OF COMPANY NAMES

Action Ins	Action Instruments
AD	Analog Devices
ADT	Advanced Digital Technology
Advent	Advent Products, Inc.
Alphatron	Alphatron
AMA	American Automation
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
Amperex	Amperex Electronic Corp.
Analogic	Analogic
Analog Sys	Analog Systems
APC	Applied Micro Circuits
Apex	Apex Microtechnology
APM	Applied Microsystems Corp.
Appl Sys	Applied Systems Corp.
APT	Applied Microtechnology
Aptek	Aptek Microsystems
Array Tech	Array Technology
AWI	AWI Electronics
Barvon	Barvon Research
Bedford	Bedford Computer Systems Inc.
Burr-Brown	Burr-Brown
CAE	Computer Aided Engineering
Cal Devices	California Devices
Cermetek	Cermetek
CGRS	CGRS Microtech Inc.
Cherry	Cherry Semiconductor
CIC	Custom Integrated Circuits
CirTech	Circuit Technology
Citel	Citel
Comlinear	Comlinear Corporation
CMA	Custom MOS Arrays
Comark	Comark Corp.
Comdial	Comdial Semiconductor
Comp Auto	Computer Automation
Compas	Compas Microsystems
Cont Logic	Control Logic Inc.
Control Sys	Control Systems Microsystems Div.
CreMicro	Creative Micro Systems
Cromemco	Cromemco, Inc.
Cubit	Cubit Inc.
Curtis	Curtis Electro Devices, Inc.
Cybernetic	Cybernetic Micro Systems
Cybersys	Cybersystems
Cybertek	Cybertek Inc.
Data General	Data General
Data I/O	Data I/O
Data Trans	Data Translation
Datel	Datel
Datricon	Datricon Corporation
DDC	Data Devices Corporation
DEC	Digital Equipment Corporation
Die-Tech	Die-Tech
Digelec	Digelec Corp.
Digitek	Digitek, Inc.
Dionics	Dionics Inc.
Dist Comp	Distributed Computer Systems
Divers Tech	Diversified Technology
E-HI	E-H International, Inc.
EDI	Electronic Designs Inc.
Elind	Elind Elettronica Industriale
EMM-SESCO	EEM-SESCO
Emulogic	Emulogic Inc.
ETI Micro	ETI Micro
Exar	Exar Integrated Systems
Exel	Exel Microelectronics
Fairchild	Fairchild
Ferranti	Ferranti Electric
Force	Force Computers
Fujitsu A	Fujitsu America
Fujitsu	Fujitsu Microelectronics, Inc.
GI	General Instrument
GTE Micro	GTE Microcircuits
Harris	Harris Semiconductor
Heurikon	Heurikon Corp.
Hilevel	Hilevel Technology, Inc.
Hitachi	Hitachi America, Ltd.
Holt	Holt Inc.
HP	Hewlett-Packard
Hughes	Hughes Aircraft, Solid State Products
Hybrid Sys	Hybrid Systems
HyComp	HyComp
ICC	International Cybernetics
~~**IDT**~~	~~Integrated Device Technology~~
IMI	International Microcircuits, Inc.
IMP	International Microelectronic Products
IMS	Industrial MicroSystems Inc.
Infosphere	Infosphere
Inmos	Inmos
IntCirEng	Integrated Circuit Engineering
IntCirSys	Integrated Circuit Systems
IntCompSys	Integrated Computer Systems
Int Tech	Integrated Technology Corp.
Intech	Intech Microcircuits Div.
Intel	Intel
Interdesign	Interdesign
Intersil	Intersil
Intronics	Intronics
ITT	ITT Semiconductors
Kinetic Sys	Kinetic Systems
Kontron	Kontron Electronics
Lambda	Lambda Semiconductor
Linear Tech	Linear Technology
LSI Comp	LSI Computer Systems
LSI Logic	LSI Logic Corporation
Master Logic	Master Logic Corporation
Matrix	Matrix Corp.
Matrox	Matrox Electronic Systems
Maxim	Maxim Integrated Products
MCC	Micro-Computer Control
MCE	MCE Electronics
Micrel	Micrel
Micro Innov	Micro Innovators
Micropac	Micropac Industries
Micro Net	Micro Networks
Micro Pwr	Micro Power Systems
Micro Sci	Micro Sciences Corp.
Micro Tech	Microcircuits Technology
Micro-Link	Micro-Link Corporation
~~**Micron**~~	~~Micron Technology~~
MilerTron	MilerTronics
Miller	Miller Technology
Mitel	Mitel Semiconductor
Mitsubishi	Mitsubishi Electronics
MMI	Monolithic Memories, Inc.
Mostek	Monolithic Systems Corp.
Motorola	Mostek
MRC	Motorola Semiconductor
Murray	MRC Systems
Monosil	Murray Consulting
National	National Semiconductor
NCM	NCM Corp.
NCR	NCR Corp., Microelectronics Division
NEC	NEC Electronics
Nitron	Nitron
OAE	Oliver Advanced Engineering
Octagon	Octagon Systems Corp.
OEI	Optical Electronics Inc.
Ohio Sci	Ohio Scientic
OKI	OKI Semiconductor
Omnibyte	Omnibyte Corp.
Onset	Onset Computer Corp.
Panasonic	Panasonic
Pico Design	Pico Design
Polycore	Polycore Electronics
Plessey	Plessey Semiconductors
PMI	Precision Monilithics, Inc.
PragDes	Pragmatic Design Inc.
Pro-Log	Pro-Log Corp.
Quay	Quay Corp.
Raytheon	Raytheon Semiconductor
RCA	RCA Solid State Division
RCI Data	RCI Data
RELMS	Relational Memory Systems
Reticon	Reticon
RIFA	RIFA
Rockwell	Rockwell, Microelectronic Devices
RTC	Riehl Time Corporation
Sanyo	Sanyo
SBE	SBE, Inc.
SEEQ	SEEQ Technology, Inc.
SPI	Semi Processes Inc.
Siemens	Siemens
Si-Fab	Si-Fab
Signetics	Signetics
SGS	SGS Semiconductor
Sharp	Sharp
Silicon G	Silicon General
Siliconix	Siliconix
Silicon Sys	Silicon Systems Inc.
Siltronics	Siltronics
SMC	Standard Microsystems Corp.
S MOS	S MOS Systems
Solarise	Solarise Enterprises
Solitron	Solitron Devices
Sprague	Sprague Electric Company
SSM	Solid State Micro Technology for Music
SSS	Solid State Scientific
Stag	Stag Microsystems
STC	Storage Technology Corp.
STD	STD Microsystems
Struc Des	Structured Design Inc.
Stynetic	Stynetic Systems
Sunrise	Sunrise Electronics
Sunshine	Sunshine Semiconductor
Supertex	Supertex Inc.
Symtek	Symtek Corp.
Synertek	Synertek
Sys Innov	Systems Innovations
Tau Zero	Tau Zero Inc.
Technitrol	Technitrol
Tektronix	Tektronix
Teledyne C	Teledyne Crystalonics
Teledyne P	Teledyne Philbrick
Teledyne S	Teledyne Semiconductor
Telefunken	Telefunken
Telmos	Telmos
Teltone	Teltone Corporation
TI	Texas Instruments
Third Domain	Third Domain
Thomson-CSF	Thomson-CSF Components Corp.
Toshiba	Toshiba America
Trans-Data	Trans-Data
TRW	TRW LSI Products
Unitrode	Unitrode
Universal	Universal Semiconductor, Inc.
Varix	Varix Corp.
VLSI Design	VLSI Design Associates
VTI	VLSI Technology, Inc.
Votrax	Votrax
Weitek	Weitek Corporation
Western	Western Digital
Wintek	Wintek Corp.
Xicor	Xicor, Inc.
Xycom	Xycom
Zendex	Zendex Corp.
Zilog	Zilog
ZyMOS	ZyMOS Corporation
Zytrex	Zytrex Corp.

Advanced Micro Devices

BIPOLAR LSI AND SUPPORT PRODUCTS
20-Pin IMOX™ Programmable Array Logic Elements

Features of PALs

- User customizable, high performance logic building blocks
- Custom logic patterns may be generated in minutes with PROM type programmers
- Easy to use software design aids available (PALASM*)
- Improves performance and reduces board area and cost of existing TTL SSI/MSI designs
- Aids creation of new system architectures through interactive design techniques
- Security fuse prevents copying of logic by competitors
- Slim 20 and 24-pin DIP packages

Advantages of AMD PALs

- IMOX™ oxide isolated technology insures industry's fastest (12ns typ) "A" versions and fastest half-power (24ns typ) "L" versions
- Platinum-silicide fuses and added test words insure programming yields > 98%
- Functional yield after programming > 99%
- Reliability assured through more than 40 billion fuse hours of life testing with no failures
- Full AC and DC parameter testing at the factory through on-board testing circuitry
- Power-up reset simplifies state machine design
- Industry leading quality guarantees

AMD PAL Speed/Power Families

Family	t_{pd} ns (Max)	t_s(1) ns (Max)	t_{co}(1) ns (Max)	I_{CC}(2) mA (Max)	I_{OL} mA (Min)
High Speed, "A"	25	20	15	155	24
Standard	35	30	25	155	24
Half Power, "L"	35	30	25	80	24

(1) Sequential functions.
(2) Combinatorial functions.

AMD PAL FUNCTIONS

Part Number	Array Inputs	Logic	OE	Outputs	Package Pins
16R8	Eight Dedicated Eight Feedback	Eight 8-Wide AND-OR	Dedicated	Registered Inverting	20
16R6	Eight Dedicated Six Feedback Two Bidirectional	Six 8-Wide AND-OR	Dedicated	Registered Inverting	20
		Two 7-Wide AND-OR-INVERT	Programmable	Bidirectional	
16R4	Eight Dedicated Four Feedback Four Bidirectional	Four 8-Wide AND-OR	Dedicated	Registered Inverting	20
		Four 7-Wide AND-OR-INVERT	Programmable	Bidirectional	
16L8	Ten Dedicated Six Bidirectional	Eight 7-Wide AND-OR-INVERT	Programmable	Six Bidirectional Two Dedicated	20
16H8	Ten Dedicated Six Bidirectional	Eight 7-Wide AND-OR	Programmable	Six Bidirectional Two Dedicated	20
16LD8	Ten Dedicated Six Bidirectional	Eight 8-Wide AND-OR-INVERT	–	Dedicated	20
16HD8	Ten Dedicated Six Bidirectional	Eight 8-Wide AND-OR	–	Dedicated	20
22V10	Twelve Dedicated Ten Bidirectional/ Feedback	Ten 12 (Average)-Wide AND-OR/ AND-OR-INVERT	Programmable	Ten Bidirectional/Registered Programmable Polarity	24

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*PALASM is a registered trademark of Monolithic Memories, Inc.

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BIPOLAR LSI AND SUPPORT PRODUCTS
20-Pin IMOX™ Programmable Array Logic Elements

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 20 to Pin 10) Continuous	−0.5 to +7V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to $+V_{CC}$ max
DC Voltage Applied to Outputs During Programming	21V
Output Current Into Outputs During Programming (Max Duration of 1 sec)	200mA
DC Input Voltage	−0.5 to +5.5V
DC Input Current	−30 to +5mA

OPERATING RANGE

Parameters	Description	Commercial Min	Commercial Max	Military Min	Military Max	Units
V_{CC}	Supply Voltage	4.75	5.25	4.50	5.50	V
T_A	Operating Free Air Temperature	0	75	−55		°C
T_C	Operating Case Temperature				125	°C

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions			Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2mA	COM'L	2.4	3.5		Volts
			I_{OH} = −2mA	MIL				
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	COM'L			0.50	Volts
			I_{OL} = 12mA	MIL				
V_{IH} (Note 2)	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL} (Note 2)	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.40V				−20	−250	μA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V					25	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.5V (Note 3)			−30	−60	−90	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX	16L8, 16H8, 16HD8, 16LD8 16L8A, 16H8A, 16HD8A, 16LD8A			110	155	mA
			16R8, 16R6, 16R4 16R8A, 16R6A, 16R4A			120	180	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−0.9	−1.2	Volts
I_{OZH}	Output Leakage Current (Note 4)	V_{CC} = MAX, V_{IL} = 0.8V V_{IH} = 2.0V	V_O = 2.7V				100	μA
I_{OZL}			V_O = 0.4V				−100	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @f = 1MHz (Note 5)				6		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @f = 1MHz (Note 5)				9		

Notes:
1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. I/O pin leakage is the worst case of I_{OZX} or I_{IX} (where X = H or L).
5. These parameters are not 100% tested, but are periodically sampled.

BIPOLAR LSI AND SUPPORT PRODUCTS
20-Pin IMOX™ Programmable Array Logic Elements

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless otherwise noted)
HIGH SPEED

Parameters	Description	Test Conditions	Typ (Note 1)	COM'L Min	COM'L Max	MIL Min	MIL Max	Units
t_{PD}	Input or Feedback to Non-Registered Output 16L8A, 16R6A, 16R4A, 16LD8A, 16H8A, 16HD8A	COM'L $R_1 = 200$ $R_2 = 390$; MIL $R_1 = 390$ $R_2 = 750$	12		25		30	ns
t_{EA}	Input to Output Enable 16L8A, 16R6A, 16R4A, 16H8A		12		25		30	ns
t_{ER}	Input to Output Disable 16L8A, 16R6A, 16R4A, 16H8A		12		25		30	ns
t_{PZX}	Pin 11 to Output Enable 16R8A, 16R6A, 16R4A		8		20		25	ns
t_{PXZ}	Pin 11 to Output Disable 16R8A, 16R6A, 16R4A		8		20		25	ns
t_{CO}	Clock to Output 16R8A, 16R6A, 16R4A		8		15		20	ns
t_s	Input or Feedback Setup Time 16R8A, 16R6A, 16R4A		10	20		25		ns
t_H	Hold Time 16R8A, 16R6A, 16R4A		−10	0		0		ns
t_P	Clock Period			35		45		ns
t_W	Clock Width			15		20		ns
f_{MAX}	Maximum Frequency				28.5		22	MHz

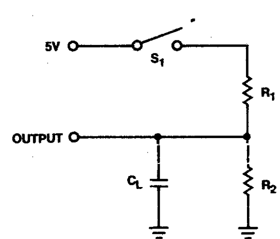
Notes: 1. Typical limits are at $V_{CC} = 5.0V$ and $T_A = 25°C$.
2. t_{PD} is tested with switch S_1 closed and $C_L = 50pF$.
3. For three-state outputs, output enable times are tested with $C_L = 50pF$ to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with $C_L = 5pF$. HIGH to high impedance tests are made to an output voltage of $V_{OH} - 0.5V$ with S_1 open; LOW to high impedance tests are made to the $V_{OL} + 0.5V$ level with S_1 closed.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless otherwise noted)
STANDARD SPEED

Parameters	Description	Test Conditions	Typ (Note 1)	COM'L Min	COM'L Max	MIL Min	MIL Max	Units
t_{PD}	Input or Feedback to Non-Registered Output 16L8, 16R6, 16R4, 16LD8, 16H8, 16HD8	COM'L $R_1 = 200$ $R_2 = 390$; MIL $R_1 = 390$ $R_2 = 750$	17		35		40	ns
t_{EA}	Input to Output Enable 16L8, 16R6, 16R4, 16H8		17		35		40	ns
t_{ER}	Input to Output Disable 16L8, 16R6, 16R4, 16H8		17		35		40	ns
t_{PZX}	Pin 11 to Output Enable 16R8, 16R6, 16R4		12		25		25	ns
t_{PXZ}	Pin 11 to Output Disable 16R8, 16R6, 16R4		12		25		25	ns
t_{CO}	Clock to Output 16R8, 16R6, 16R4		12		25		25	ns
t_s	Input or Feedback Setup Time 16R8, 16R6, 16R4		15	30		35		ns
t_H	Hold Time 16R8, 16R6, 16R4		−10	0		0		ns
t_P	Clock Period			55		60		ns
t_W	Clock Width			20		25		ns
f_{MAX}	Maximum Frequency				18		16.5	MHz

Notes: 1. Typical limits are at $V_{CC} = 5.0V$ and $T_A = 25°C$.
2. t_{PD} is tested with switch S_1 closed and $C_L = 50pF$.
3. For three-state outputs, output enable times are tested with $C_L = 50pF$ to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with $C_L = 5pF$. HIGH to high impedance tests are made to an output voltage of $V_{OH} - 0.5V$ with S_1 open; LOW to high impedance tests are made to the $V_{OL} + 0.5V$ level with S_1 closed.

AC TEST LOAD



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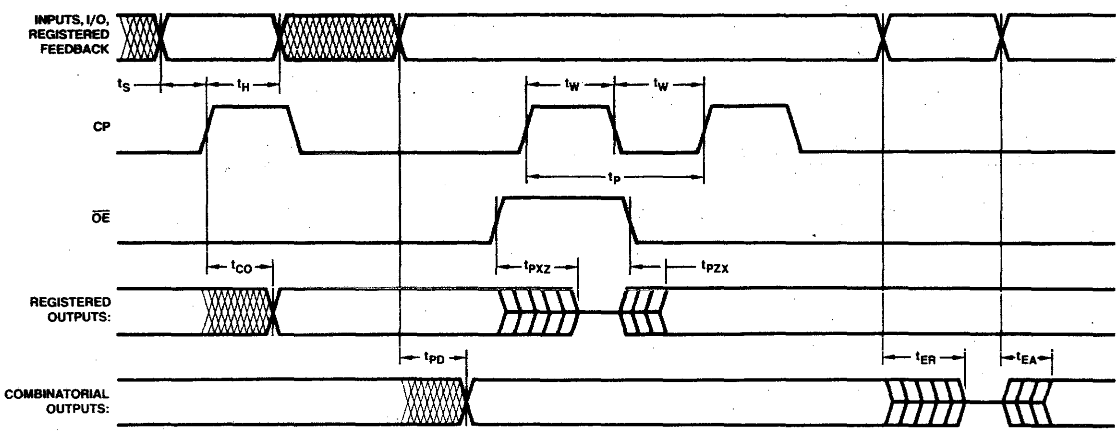
BIPOLAR LSI AND SUPPORT PRODUCTS
20-Pin IMOX™ Programmable Array Logic Elements

SWITCHING WAVEFORMS



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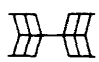
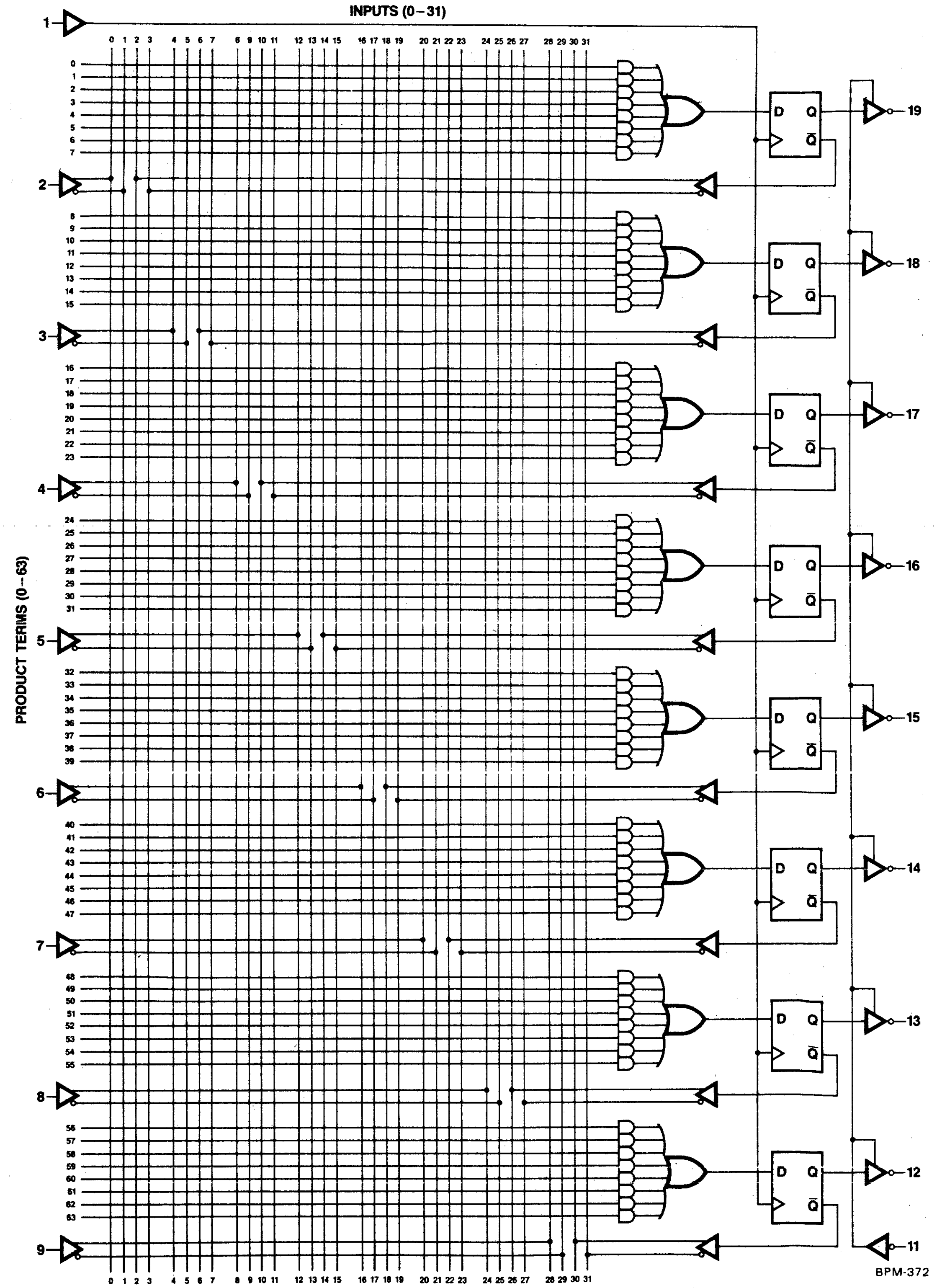
KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

BIPOLAR LSI AND SUPPORT PRODUCTS
20-Pin IMOX™ Programmable Array Logic Elements

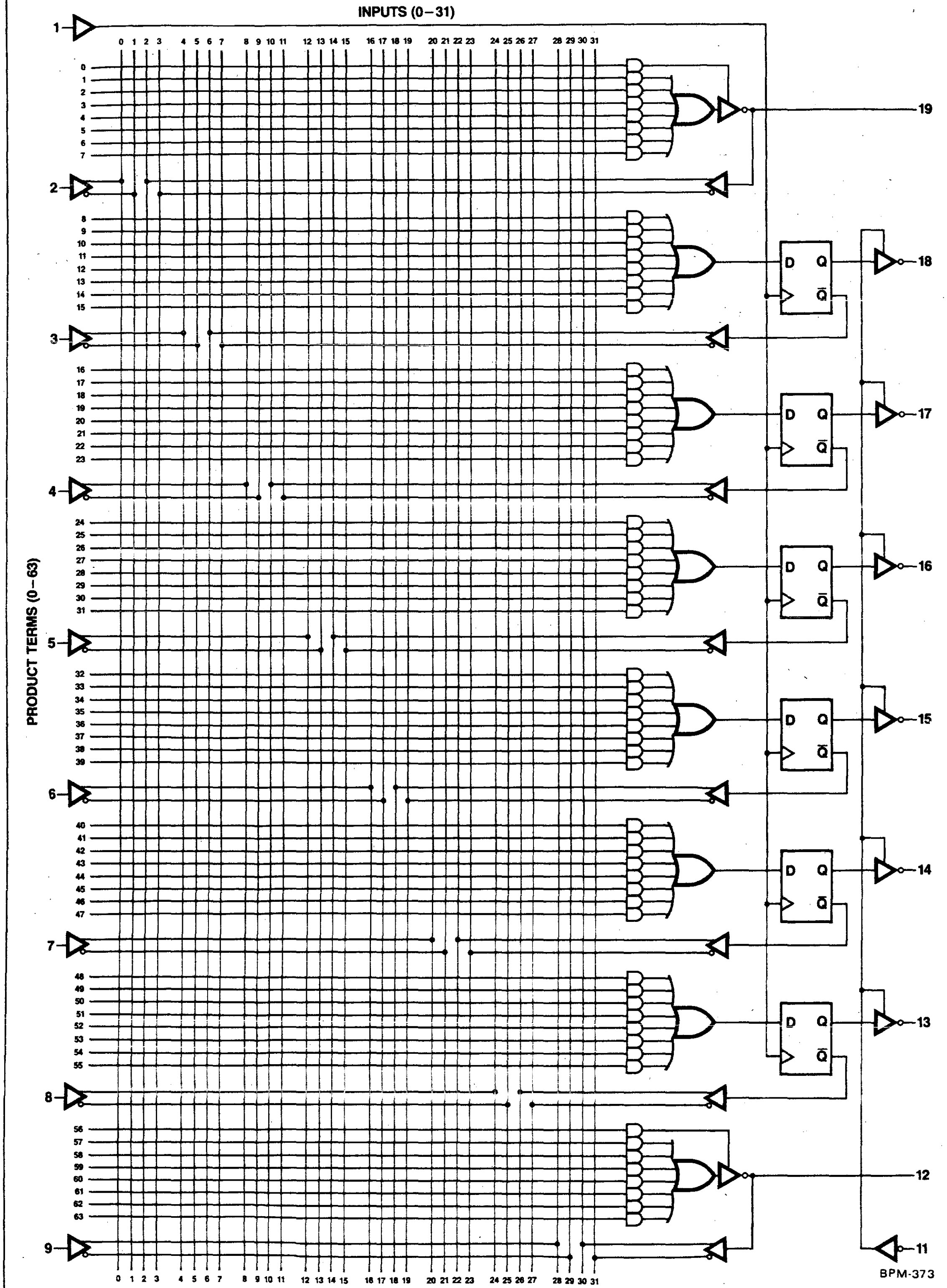
LOGIC DIAGRAM AmPAL16R8/AmPAL16R8A



Advanced Micro Devices

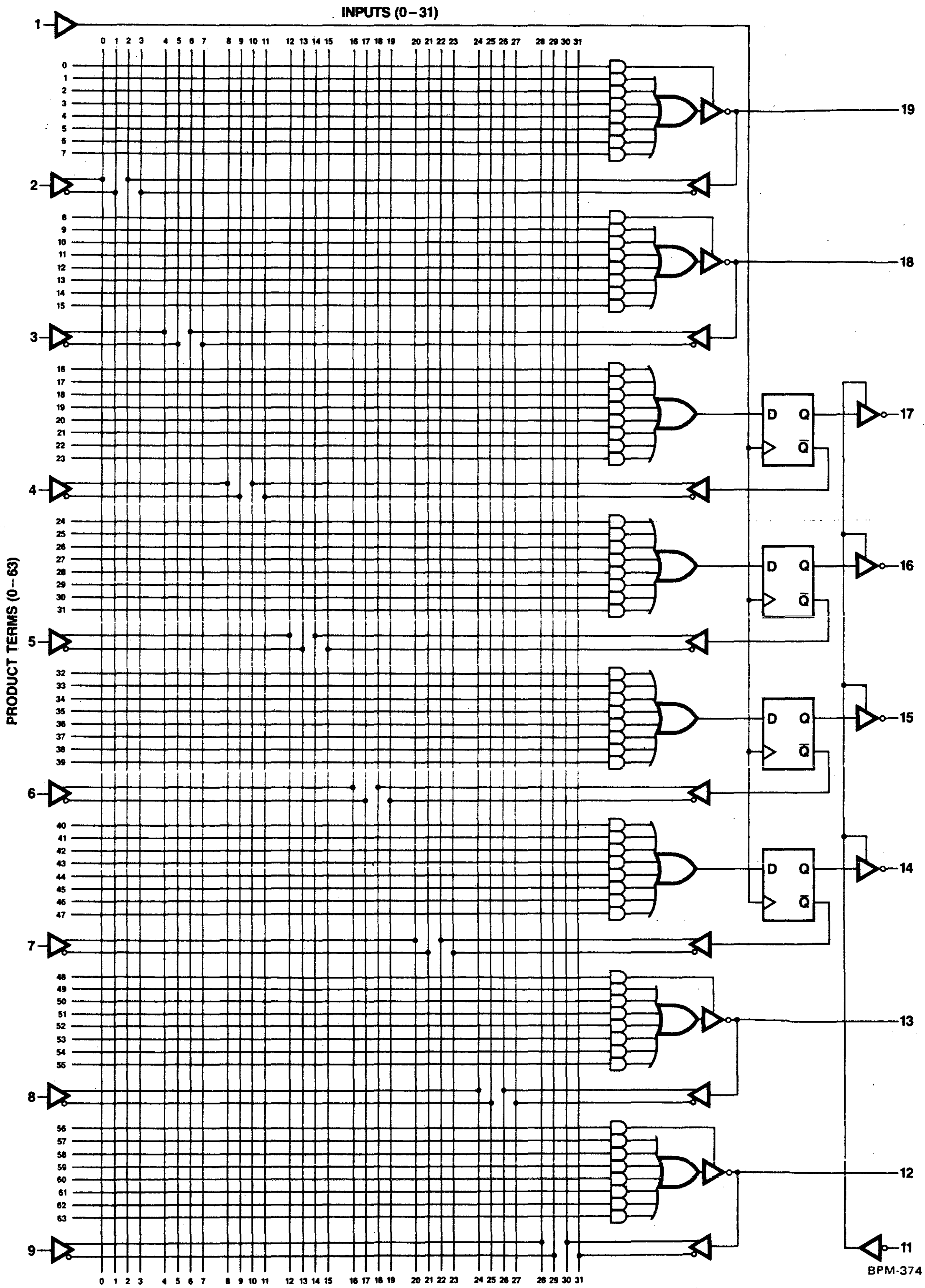
BIPOLAR LSI AND SUPPORT PRODUCTS
20-Pin IMOX™ Programmable Array Logic Elements

LOGIC DIAGRAM AmPAL16R6/AmPAL16R6A



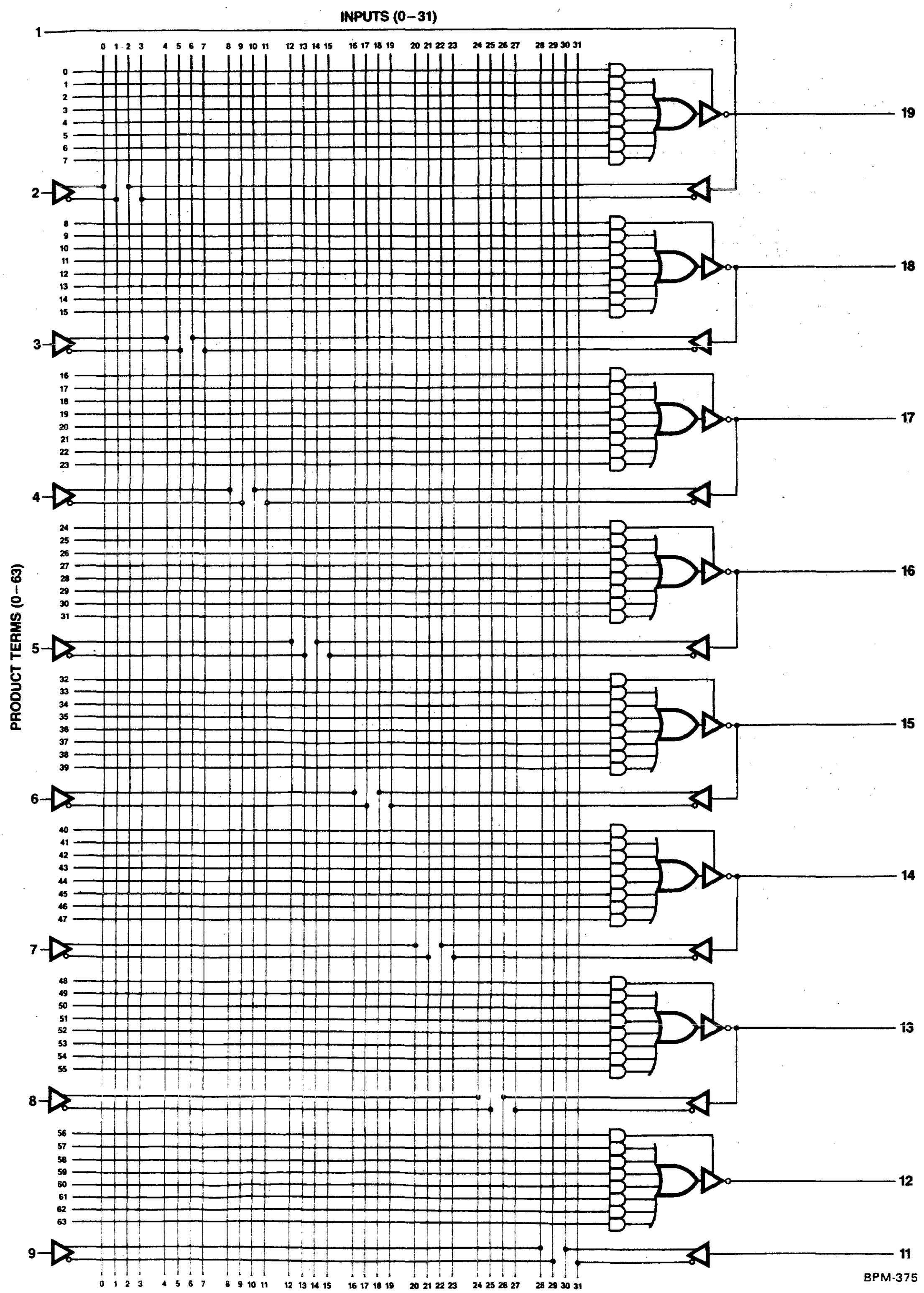
BIPOLAR LSI AND SUPPORT PRODUCTS
20-Pin IMOX™ Programmable Array Logic Elements

LOGIC DIAGRAM AmPAL16R4/AmPAL16R4A

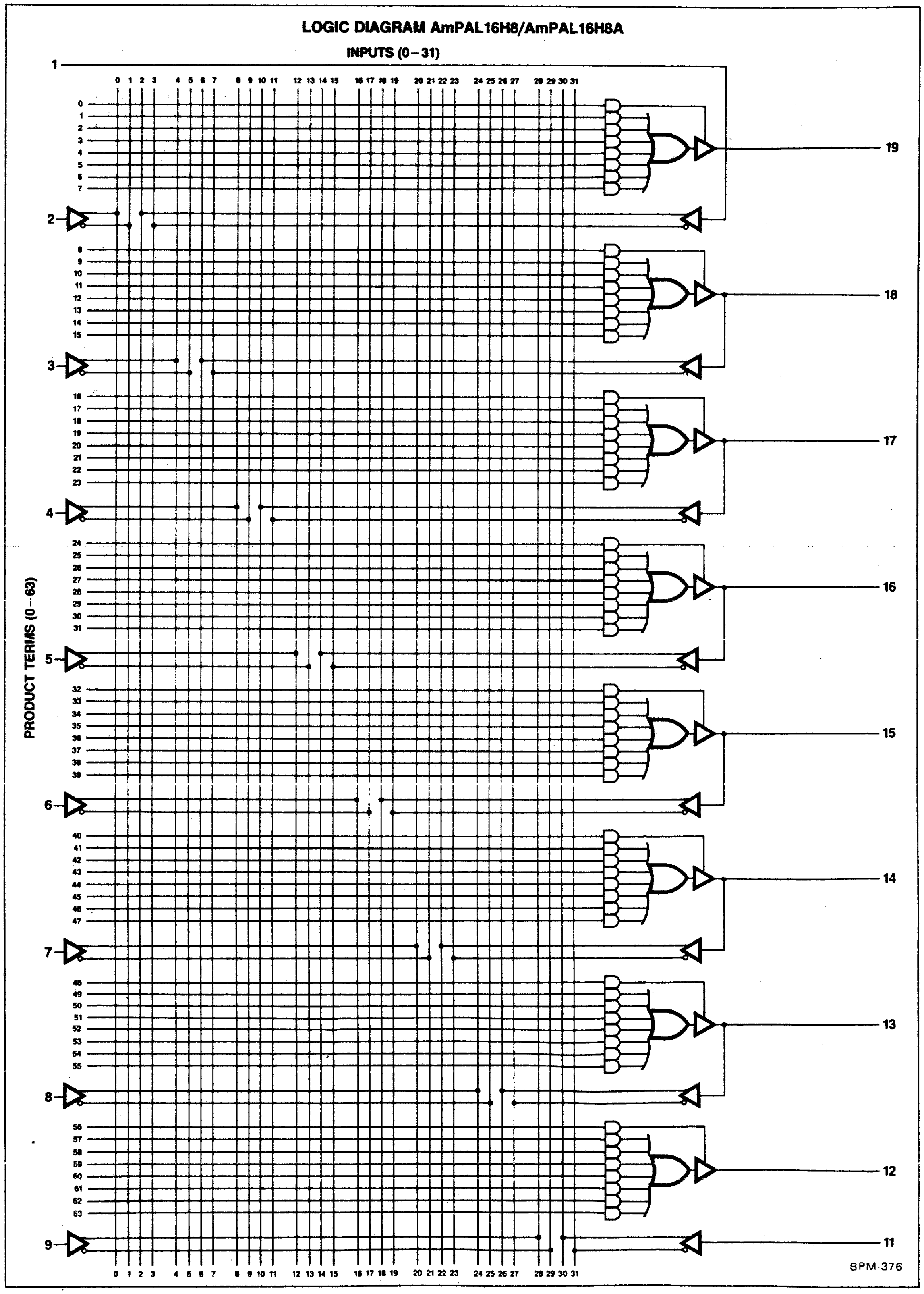


BIPOLAR LSI AND SUPPORT PRODUCTS
20-Pin IMOX™ Programmable Array Logic Elements

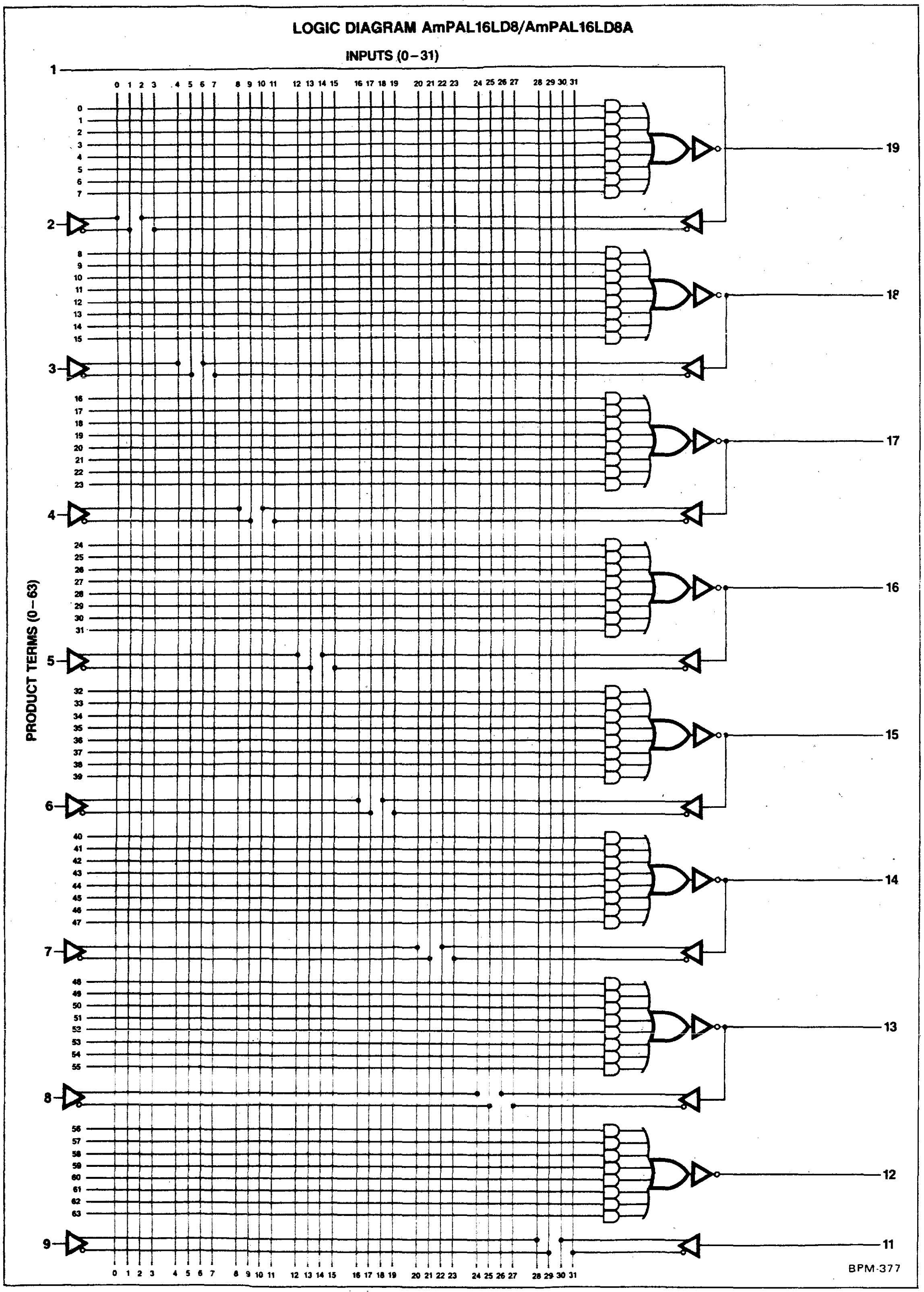
LOGIC DIAGRAM AmPAL16L8/AmPAL16L8A



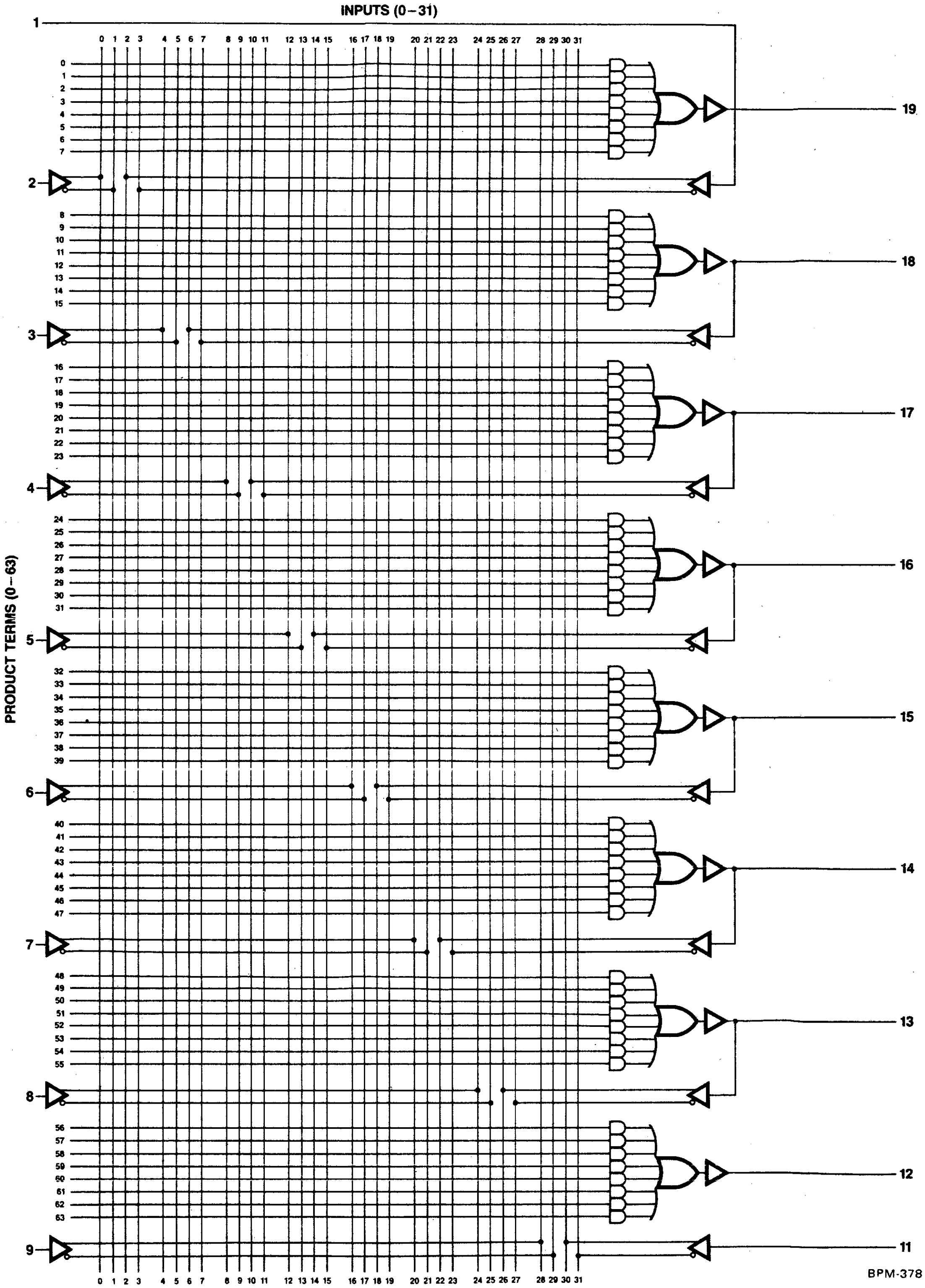
BIPOLAR LSI AND SUPPORT PRODUCTS
20-Pin IMOX™ Programmable Array Logic Elements



BIPOLAR LSI AND SUPPORT PRODUCTS
20-Pin IMOX™ Programmable Array Logic Elements



LOGIC DIAGRAM AmPAL16HD8/AmPAL16HD8A



BIPOLAR LSI AND SUPPORT PRODUCTS
20-Pin IMOX™ Programmable Array Logic Elements

PROGRAMMING

Each AMD PAL fuse is programmed with a simple sequence of voltages applied to two control pins (1 and 11) and a programming voltage pulse applied to the output under programming. Addressing of the 2048 element fuse array is accomplished with normal TTL levels on eight input pins (five select the input line number and three select the product term number). V_{CC} is maintained at a normal level throughout the programming and verify cycle – no extra high levels are required.

The necessary sequence of levels for programming any fuse is shown in the Programming Timing Diagram. The address of each fuse in terms of Input Line Number and Product Term Line Number is defined by the Fuse Address Tables 1 and 2. Current, voltage and timing requirements for each pin are specified in the Programming Parameter Table below.

The 16L8, 16R8, 16R6, 16R4, 16H8, 16LD8 and 16HD8 use identical programming conditions and sequences.

After all programming has been completed, the entire array should be reverified at V_{CCL} and again at V_{CCH}. Reverification can be accomplished by reading all eight outputs in parallel rather than one at a time. The array fuse verification cycle checks that the correct array fuses have been blown and can be sensed by the outputs.

AMD PALs have been designed with many internal test features that are used to assure high programming yield and correct logical operation for a correctly programmed part.

An additional fuse is provided on each AMD PAL circuit to prevent unauthorized copying of AMD PAL fuse patterns when design security is desired. Blowing the security fuse blocks entry to the fuse pattern verify mode.

To blow the security fuse:
1. Power up part to V_{CCP}
2. Raise Pin 5 to V_{HH}.
3. Pulse Pin 11 from ground to V_{OP} for a 50μsec duration.
4. Perform a normal end-of-programming verify cycle at V_{CCL} and V_{CCH}. All fuse locations should be sensed as blown if the security fuse has been successfully blown.

Note that parts with the security fuse blown may not be returned as programming rejects.

AMD PALs normally have high programming yields (>98%). Programming yield losses are frequently due to poor socket contact, equipment out of calibration or improperly used.

PROGRAMMING PARAMETERS T_A = 25°C

Parameters	Description		Min	Typ	Max	Units
V_{HH}	Control Pin Extra High Level	Pin 1 @ 10–40mA	10	11	12	Volts
		Pin 11 @ 10–40mA	10	11	12	
V_{OP}	Program Voltage Pins 12–19 @ 15–200mA		18	20	22	Volts
V_{IHP}	Input High Level During Programming and Verify		2.4	5	5.5	Volts
V_{ILP}	Input Low Level During Programming and Verify		0.0	0.3	0.5	Volts
V_{CCP}	V_{CC} During Programming @ I_{CC} = 50–200mA		5	5.2	5.5	Volts
V_{CCL}	V_{CC} During First Pass Verification @ I_{CC} = 50–200mA		4.1	4.3	4.5	Volts
V_{CCH}	V_{CC} During Second Pass Verification @ I_{CC} = 50–200mA		5.4	5.7	6.0	Volts
V_{Blown}	Successful Blown Fuse Sense Level @ Output	16L8, 16R8, 16R6, 16R4, 16LD8 16L8A, 16R8A, 16R6A, 16R4A, 16LD8A		0.3	0.5	Volts
		16H8, 16HD8, 16H8A, 16HD8A	2.4	3		
dV_{OP}/dt	Rate of Output Voltage Change		20		250	V/μsec
dV_{11}/dt	Rate of Fusing Enable Voltage Change (Pin 11 Rising Edge)		100		1000	V/μsec
t_P	Fusing Time First Attempt		40	50	100	μsec
	Subsequent Attempts		4	5	10	msec
t_D	Delays Between Various Level Changes		100	200	1000	ns
t_V	Period During which Output is Sensed for V_{Blown} Level				500	ns
V_{ONP}	Pull-Up Voltage On Outputs Not Being Programmed		V_{CCP} – 0.3	V_{CCP}	V_{CCP} + 0.3	Volts
R	Pull-Up Resistor On Outputs Not Being Programmed		1.9	2	2.1	KΩ

AMD PAL PROGRAMMING EQUIPMENT INFORMATION

Source and Location	Data I/O 10525 Willows Rd. N.E. Redmond, WA 98052	Kontron Electronics, Inc. 630 Price Avenue Redwood City, CA 94063	Stag Microsystems 528-5 Weddel Drive Sunnyvale, CA 94086
Programmer Model(s)	Model-100, 29, 19 or 17	Model-MPP-80S or EPP80	Model-PPX
AMD PAL Personality Module	Logicpak 950-1942-001	MOD-33	PPM2200
Socket Adapter	715-1947-003	SA37	Am202S

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BIPOLAR LSI AND SUPPORT PRODUCTS
20-Pin IMOX™ Programmable Array Logic Elements

PROGRAMMING WAVEFORMS

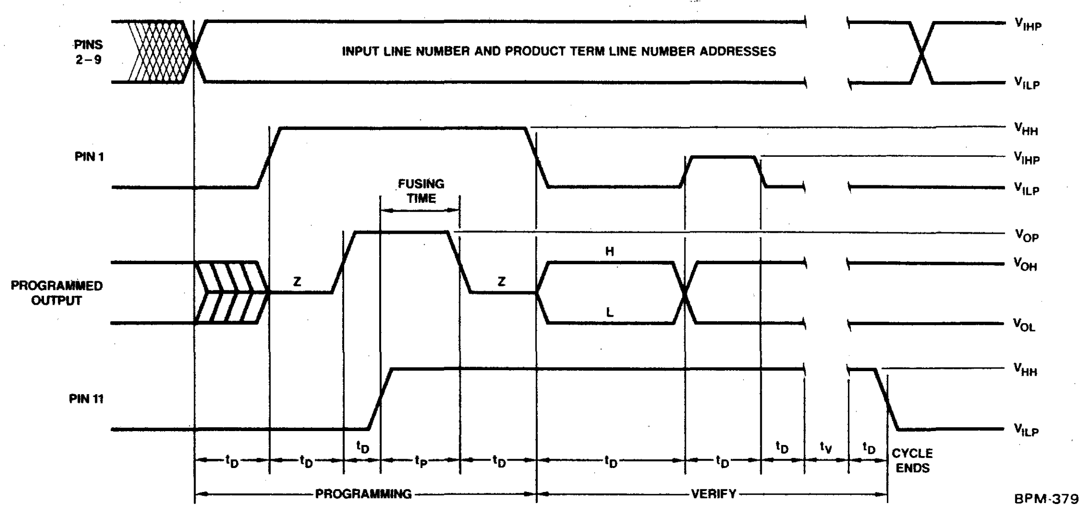

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TABLE 1. INPUT ADDRESSING

Input Line Number	Input Line Number Address Pin States 9	8	7	6	5
0	L	L	L	L	L
1	L	L	L	L	H
2	L	L	L	H	L
3	L	L	L	H	H
4	L	L	H	L	L
5	L	L	H	L	H
6	L	L	H	H	L
7	L	L	H	H	H
8	L	H	L	L	L
9	L	H	L	L	H
10	L	H	L	H	L
11	L	H	L	H	H
12	L	H	H	L	L
13	L	H	H	L	H
14	L	H	H	H	L
15	L	H	H	H	H
16	H	L	L	L	L
17	H	L	L	L	H
18	H	L	L	H	L
19	H	L	L	H	H
20	H	L	H	L	L
21	H	L	H	L	H
22	H	L	H	H	L
23	H	L	H	H	H
24	H	H	L	L	L
25	H	H	L	L	H
26	H	H	L	H	L
27	H	H	L	H	H
28	H	H	H	L	L
29	H	H	H	L	H
30	H	H	H	H	L
31	H	H	H	H	H

L = V_{ILP}
H = V_{IHP}

SIMPLIFIED PROGRAMMING DIAGRAM

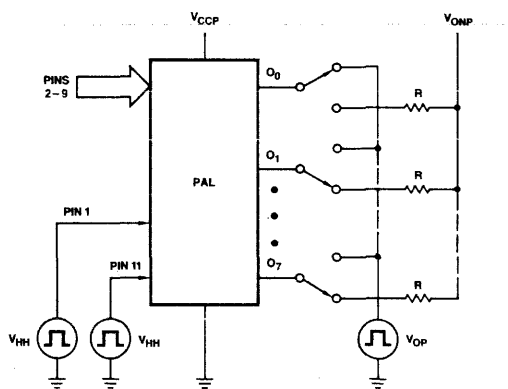

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TABLE 2. PRODUCT TERM ADDRESSING

Product Term Line Number								Product Term Select Address Pin 4	3	2
0	8	16	24	32	40	48	56	L	L	L
1	9	17	25	33	41	49	57	L	L	H
2	10	18	26	34	42	50	58	L	H	L
3	11	19	27	35	43	51	59	L	H	H
4	12	20	28	36	44	52	60	H	L	L
5	13	21	29	37	45	53	61	H	L	H
6	14	22	30	38	46	54	62	H	H	L
7	15	23	31	39	47	55	63	H	H	H
Pin 19	Pin 18	Pin 17	Pin 16	Pin 15	Pin 14	Pin 13	Pin 12			
Programming Access and Verify Pin										

L = V_{ILP}
H = V_{IHP}

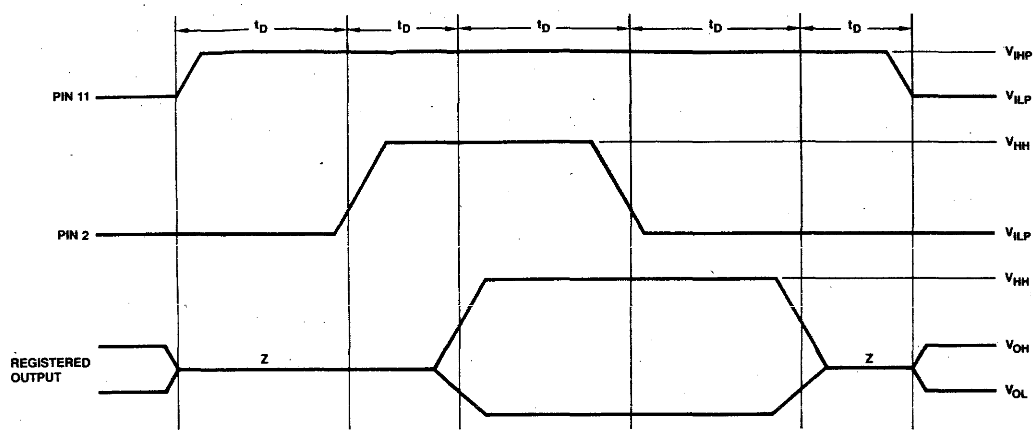
Advanced Micro Devices

BIPOLAR LSI AND SUPPORT PRODUCTS
20-Pin IMOX™ Programmable Array Logic Elements

PRELOAD OF REGISTERED OUTPUTS

AMD PAL registered outputs are designed with extra circuitry to allow loading each register asynchronously to either a HIGH or LOW state. This feature simplifies testing since any initial state for the registers can be set to optimize test sequencing.

The pin levels and timing necessary to perform the PRELOAD function are detailed below:



Level forced on registered output pin during preload cycle	Output state at the output pin after cycle
V_{HH}	HIGH
0V to V_{CCH} or OPEN	LOW

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ORDERING INFORMATION

AmPAL XXXXX X X X X

Basic Device
16R8
16R6
16R4
16L8
16H8
16LD8
16HD8

Speed Selection
= Standard
A = High Speed

Screening
C = 883C Basic Flow
B = 883B (Burn-in)

Temperature Range
C = Commercial
M = Military

Package
P = Molded DIP (Commercial Only)
D = Hermetic DIP
L = Chip-Pak™*

*Chip-Paks are rated at maximum case temperature only.

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

Spectrum of Custom Solutions

No other company can match AMI's track record in developing state-of-the-art custom VLSI products. With more than 2000 custom devices designed and manufactured since 1966, AMI has more experience than any other integrated circuit company in building a wide variety of custom microcircuits.

AMI not only has the experience, but the design engineering organization and the advanced production and testing facilities to produce the highest quality MOS/VLSI circuits. And because AMI also offers standard memory, microprocessor, telecommunication and consumer products and the widest variety of custom VLSI processes in the industry, we're able to be objective in helping customers determine their most cost effective approach.

The Advantages of Custom Circuits

Since a single custom MOS/VLSI chip can replace expensive electromechanical devices, discrete logic components, or less efficient general purpose LSI circuits, it offers a number of benefits not available with standard logic.

Custom circuits save money. Grouping functions onto a single chip lowers production and inventory costs dramatically. That reduces your product manufacturing costs as well.

Custom circuits are more reliable. Putting a complete system on a chip trims component count, improving both product reliability and production yields. Rework, repair and replacements are minimized.

Custom circuits reduce space and power requirements. Fewer components means both space and power requirements are reduced.

Custom circuits offer superior performance. Since the circuit is designed to your requirements, features and functions can be incorporated which are not available in general purpose chips. Special tailoring reduces test requirements as well.

Custom circuits offer proprietary protection. Being tailored exactly to your requirements, a custom circuit cannot be easily duplicated. This can help put you ahead — and keep you ahead — of your competition.

The Spectrum of Solutions

The decision to use a custom circuit depends on your system design requirements — such things as complexity, features, size and power limitations. But no longer is your custom decision limited by low volume or short development time — not when you come to AMI.

AMI has a full spectrum of custom solutions to assure you get that solution which meets your system performance and time-to-market requirements at the lowest possible cost.

AMI's spectrum of solutions bridges the total span of volume, timing and interface needs of our customers. From semi-custom designs, to full custom design — somewhere on the spectrum, your development time and volume requirements can be met. For customers who already have their designs, AMI can provide custom fabrication for the customer's tooling. We will even teach custom design if that's what our customers need. And we can even go a step further and license the technology for a customer to set up his own fabrication capability. No other company offers such a spectrum of solutions. And no other company has more experience at helping you pick the best solution for your needs.

Semi-Custom Gate Arrays

AMI offers both gate arrays and standard cell design methods for semi-custom circuit development.

Gate arrays are the best solution for circuits of moderate complexity in low-to-medium volume applications or where the shortest possible development time is required. AMI offers both gate arrays and standard cell design methods for semi-custom circuit development.

AMI CMOS semi-custom gate arrays are standard logic layouts of everything except the final metal interconnect pattern. Since only the final pattern needs to be developed to customize your circuits, both development time spans and development costs are dramatically reduced. Because wafers containing arrays are preprocessed and inventoried, production lead times are short. Gate arrays are especially attractive for applications requiring circuit volumes from 1,000 to 50,000 units per year.

For more details on AMI's gate arrays, refer to the "Semi-Custom" section.

Standard Cell Custom

Standard cells are custom circuits which are designed from computer stored modular cells. The computer assembles the cells into a collection of functional blocks to form a custom circuit. Since standard cells utilize predesigned cells, development time is reduced dramatically and development costs are cut 30 to 50 percent over conventional custom design. Circuit size is likely to be slightly larger than a conventional custom circuit, so they are most appropriate where rapid development is more important than minimal size. Standard cells are cost effective in volume levels beginning around 10,000 circuits.

For more details on AMI standard cells refer to the "Semi-Custom" section.

Optimized Custom Design

Where end product volume is high — beyond 50,000 units per year — or where special requirements for lowest power, minimal space or highest performance exist, the solution is likely to be conventional custom design. By optimizing circuit elements and layout for a specific part, die size is substantially smaller than using semi-custom design methods. In high volume applications, a smaller die size results in lower unit cost to the customer.

Spectrum of Custom Solutions

In addition, custom designs allow you to combine logic elements, memory, and analog circuits in a single device. This design flexibility is not available in gate arrays and only available to a limited extent in standard cells.

Instrumental in the design of custom circuits is our Symbolic Interactive Design System (SIDS). The design is done primarily with SIDS where a layout designer works with symbols directly at a large screen alphanumeric color CRT. After the SIDS circuit design has been completed and verified, the symbols are converted to polygons and a 10X reticle tape is prepared.

SIDS uses on-line, real-time design rule checking capability to isolate design rule errors in the layout. This allows immediate correction which greatly reduces the development span time.

Also a nodal trace function permits a designer to trace and highlight a given electrical node. In this way, the designer can manually insure that the node is connected as specified in the master logic description.

Full background real-time design rule checking on windows, cells, and chips is supported, as is full background continuity checking against the master logic description. This eliminates the delay from digitizing and batch processed computer checking of circuits for accuracy.

With SIDS, error correction, circuit modification and area relocations take only minutes. That significantly reduces design cycle time and development costs.

Computer-aided hand-drawn layouts are used to reduce extremely complex circuits to the absolute smallest size. Development time and costs are higher, but in certain cases, size or complexity requirements may require the hand-drawn approach.

Customer Owned Tooling

In many cases AMI customers design their own circuits, either through an internal design center, a design house, or another vendor. In these cases, AMI can provide custom circuit fabrication from customer owned tooling. In conjunction with a silicon foundry service, AMI's Customer Owned Tooling (COT) group can offer the customer design support in the form of design rules, standard cells, a three phase development program, test program generation and general technical support. In the event of design problems, AMI's COT group utilizes the design expertise of the custom or semi-custom group for technical assistance.

Once the circuit is designed, the customer has the option of transferring the circuit tooling to AMI in PG tape, data base tape or working plate form. Close cooperation between the customer and AMI's COT Group during an established three phase prototype development program simplifies circuit debug and reduces risk of design error.

Drawing on AMI's extensive manufacturing ability, COT offers a wide range of process variations, package types, and test capabilities. Unlike most of AMI's competition in the silicon foundry market, AMI has internal photolithography (mask making) and assembly capability. This internal capability avoids the high costs and quality risks of subcontracting two very important steps in custom IC manufacturing.

Once the prototype development program is completed, AMI can ship as few as five to as many as thousands of wafers per week to the customer. AMI can ship tested die, fully tested packaged devices and devices meeting military 883-B standards.

AMI's Customer Owned Tooling group is the only vendor in the silicon foundry market that offers design support, full service manufacturing capability, flexibility and experience.

Joint Development Ventures

Through a Joint Development Team (JDV) we can teach a customer to design his own MOS/VLSI circuits. The JDV is a combination of technically skilled people from the partner company and AMI who function as a design group concentrating on the customer's products alone. The JDV partner brings his system design staff and AMI brings the MOS/VLSI staff and its design technology. The partner becomes part of an in-house AMI design group. The end result is a design capability for the partner company for circuits that AMI will fabricate.

If the customer wants to go beyond designing his own circuits to operating his own manufacturing/pilot line, AMI will license the necessary technology in those situations where a long-term business relationship can be established between the partner company and AMI.

AMI Provides Leading CAD Technology

At almost all levels of the spectrum, computer-aided design (CAD) software and hardware aids are employed to assure correctness of design each step of the way and to shorten design spans reducing customer risk and lowering design cost. Highly efficient programs have been implemented to assist in logic design and simulation, layout planning, switched capacitor analysis routines and symbolic interactive design layout, to name just a few.

Hardware design aids include:

- On-site Burroughs 7760 computer with multiprocessing capability.
- Computer terminals built around a Prime computer and engineering design facilities which tie into the on-site 7760 and time-sharing services.
- Computervision interactive graphics system which provide on-line generation and editing of composite drawings; includes drafting surfaces and CRT displays.
- Calma graphics system for both production digitizing and on-line changes.
- Calma GDS-11 high speed electrostatic plotter.

Spectrum of Custom Solutions

• High speed, high resolution Electromask 9-track pattern generator.

Software design aids include:

Logic Design

• **Register Transfer Language (RTL) Simulation** — Provides a system behavior description to define instruction sets, optimize data paths, control hardware algorithm design and establish register designs.

• **Glide** — Permits user to design layout, simulate, generate patterns and develop test programs for logic arrays.

• **Path Analysis Program (PATH)** — Permits gross logic checks to be made before design, and final logic checks from the ultimate design.

• **Logic Simulator (SIMAD)** — (SIMulator with Assignable Delays) simulates logic network behavior for design verification and propagation delays.

• **Programmable Logic Array Design Aids (PLAID)** — Uses state tables and Boolean equations to generate the optimum physical structure for random logic designs.

• **Block Oriented Logic Translator (BOLT))** — A logic description compiler that generates a common data base used by SIDS, SIMAD, LPA, continuity check, PATH and CIPAR.

• **Design Rule Checking (DRC)**

• **Trace and Continuity Checking**

Circuit Design

• **Circuit Simulator (ASPEC)** — Analyzes DC operation, DC transfer functions, time domain or transients and frequency domain or small signal AC characteristics.

• **Pole Zero Analysis (PZSLIC)** — Program analyzes the frequency domain of linear integrated circuits.

• **Switched Capacitor Analysis Routine (SCAR)** — Analyzes switched capacitor filter designs for telecommunications and other analog circuits.

• **Data Analysis Program (DAP)** — Analyzes data from circuit fabrication to maintain the parameters of circuit designs.

Mask Design

• **Layout Planning Aid (LPA)** — Lays out the chip plan and interconnection between functional blocks of an integrated circuit.

• **Symbolic Interactive Design System (SIDS)** — Permits a layout designer to work directly with a computer to lay out and check a circuit on a CRT screen, dramatically shortening layout time requirements.

• **Circuit Interactive Place and Route (CIPAR)** — Automatically creates error-free mask designs in extremely short time spans.

Test Generation

AMI utilizes numerous software programs to generate test programs for integrated circuits. All serve to reduce the time needed to develop test programs to meet customer specifications.

Digital and Analog Combinations

AMI is a leading innovator in combining digital and analog functions on a single chip. We can combine any of the functions below into an optimum circuit configuration to meet your needs. Unique combinations of these functions are already used in many applications in the communications, consumer, and industrial marketplace.

DIGITAL	ANALOG
PLA	OP AMP
ALU	Oscillator
Inverter	Comparator
RAM and ROM	Voltage Reference
Shift Register	A/D and D/A Converters
Interface Driver	Switched Capacitor Filters
Automatic Power Down	Programmable Power Down
	Phase Locked Loops

State of the Art Packaging

AMI's packaging capability spans a broad spectrum, beginning with plastic, ceramic and CERDIP and going on to chip carriers, die bonding to PC boards and, most recently, mini-flat packs. As well as being a leader in plastic packaging for the high volume, low cost consumer industry, AMI's high reliability plastic packages and chip carriers are accepted under the stringent requirements in the Telecom and Automotive industries. As many industry segments move toward space-saving packages, AMI remains in the forefront in packaging using chip carriers. AMI now is developing a family of mini-flat packs which are a plastic alternative to a chip carrier.

AMI Delivers Quality

AMI quality controls for in-process wafer inspection and final assembly and test are the best in the industry. Our care in fabrication, assembly and test mean that you get products that meet your specifications for reliability. Because over 70 percent of our total production is custom, we perform many checks routinely that would only be done on special orders and at additional cost by other manufacturers. In fact, our own in-house standards are tougher than most of our customers require. Most importantly, AMI is committed to making sure that everything we do is done right, every time we do it.

The Industry's Highest Standard

AMI has consistently pursued product excellence and has reached for higher quality levels in finished products shipped. Circuits are inspected to 0.04% AQL or your specifications, whichever is more stringent.

Spectrum of Custom Solutions

This 0.04% AQL can put you in a superior competitive position. Your incoming test and assembly costs come down since there is less reworking on the line. And your customers receive a more reliable product.

Quality Checks

Among the routine quality controls exercised over every product at AMI are:

- Full logic design checks against system specifications
- Circuit simulation to verify performance against objectives
- Working plates check on automatic checkers
- Automated mask fabrication checks
- In-process wafer fabrication checks
- Wafer sort tests
- 100% optical inspection at dicing
- 100% die attach checking
- 100% lead bonding inspection prior to package sealing
- Seal checks, fine and gross leak tests
- Final digital and analog tests
- Customer specified environmental tests

Meticulous in-process checks are performed on design and workmanship at every step, to ensure a full manufacturable device. In manufacture, lot process and yield data are captured and examined as a matter of routine.

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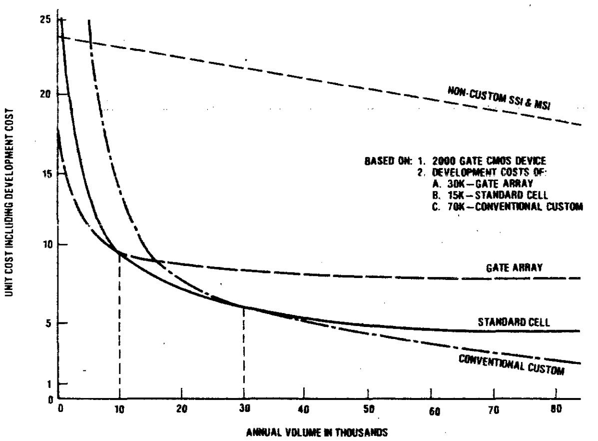
Semi-Custom Capabilities

Overview

As the semiconductor industry has marched into the new era of VLSI, a new market has appeared—fast turn custom or, as it is now called, semi-custom. AMI, a leader in custom MOS since 1966, is also a leader in this new semi-custom market. AMI has introduced CAD software and hardware tools to allow customers to design, simulate, and layout circuits using AMI gate array and standard cell families. Figure 1 shows the economic tradeoffs between gate array, standard cell, and full custom, all of which are offered by AMI.

Figure 1. Cost vs. Volume Alternatives



Gate Arrays

The simplest semi-custom ICs are gate arrays. As the name implies, a gate array consists of uncommitted component matrices of transistors (usually P- and N-type for CMOS) that allow user-defined interconnections through a single or double layer of metal. Since arrays employ fixed component locations and geometries, AMI can process the wafers up to the metallization stage and inventory the wafers for future customization. Thus gate arrays look like late mask programmable ROMs and benefit from this large-volume production because they appear to be a standard product. Thus AMI can offer them at an economical price and with fast prototyping and production turn on spans.

Standard Cells

The second semi-custom product group is standard cells.

Standard cells employ fully customized process/mask sets and must pass through all process steps before a user-specified circuit is completed. To design such chips, AMI customers use precharacterized functional cells from our cell libraries. Placing and routing the cells is done on AMI computers using specially developed software. Standard cell designs usually result in smaller chips since only the component structures required for the user-specified circuit are included, thus chips designed with cells are less expensive than gate array designed chips.

The key to success in this new market is flexibility. Flexibility to the user entails: low risk circuit implementation, short development span, lower development cost, lower piece part cost (over TTL implementations), easy to change or modify, enhanced product features, etc. For the manufacturer, flexibility means: ease of manufacture, economies of scale, and easy interface with customers. One last point: AMI offers the user the opportunity to migrate at a low cost, from a gate array to a standard cell (or possibly full custom) to further enhance his/her product. By using analog cells, significant advances in chip function integration are at the user's disposal.

In addition, AMI offers a wide selection of packages to meet specific user needs. AMI offers the CAD tools needed to work in the new market. AMI also offers the training required to move customers quickly and easily into this new technology.

2-Micron Products

AMI is developing 2-micron CMOS technology to support the next generation of semi-custom products, in both gate arrays and standard cells. These products will offer size and performance improvements of up to 50% from their 3-micron counterparts.

Introduction of the first 2-micron gate array family is planned for second quarter 1984 and is expected to offer capabilities of greater than 8000 gates.

For detailed information on Gate Arrays and Standard Cells consult the following seven pages.

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Gate Arrays

Features

- Arrays of Uncommitted CMOS Transistors Programmed by Metal Layer Interconnect to Implement Arbitrary Digital Logic Functions
- Multiple Developmental Interfaces: AMI or Customer Designed
- Three Array Families—5-Micron Single Metal CMOS, 3-Micron Single Metal CMOS, and 3-Micron Double Metal Versions
- Multiple Array Configurations—From 300 to 1260 Gates for 5-Micron Devices, and 500 to 5000 Gates for 3-Micron Devices
- Quick Turn Prototypes and Short Production Turn-On Time
- Economical Semi-Custom Approach for Low-to-Medium Production Volume Requirements
- Advanced Oxide-Isolated Silicon Gate CMOS Technology
- High Performance—2 to 3ns Typical Gate Delay for 3-Micron Devices
- Broad Power Supply Range—3V to 12V (± 10%)
- TTL or CMOS Compatible I/O
- Up to 134 I/O Connections
- Numerous Package Options
- Full Military Temperature Range (– 55°C to 125°C) and MIL-STD-883 Class B Screening Available

General Description

AMI's gate array products consist of arrays of CMOS devices whose interconnections are initially unspecified. By "programming" interconnect at the metal layer mask level, virtually arbitrary configurations of digital logic can be realized in an LSI implementation.

AMI gate array designs are based on topological cells—i.e., groups of uncommitted silicon-gate N-Channel and P-Channel transistors—that are placed at regular intervals along the X and Y axes of the chip with intervening polysilicon underpasses. Pads, input protection circuitry, and uncommitted output drivers are placed around the periphery.

Compared to SSI/MSI logic implementations, AMI's gate array approach offers lower system cost and, in addition, all the benefits of CMOS LSI. The lower system cost is due to significant reductions in component count, board area and power consumption. Product reliability, a strong function of component count, is thereby greatly enhanced. And compared to fully custom LSI circuits, the gate array offers several advantages: low development cost; shorter development time; shorter production turn-on time; and low unit costs for small to moderate production volumes.

AMI's CMOS gate arrays are offered in three families: the 5-micron UA series, the 3-micron single metal GA series, and the 3-micron double metal GA-D series. The 5-micron UA series has been in production since 1980 and well over one hundred circuits have been produced in that technology. The 3-micron GA and GA-D series are the high-speed high-density devices fabricated in AMI's state-of-the-art 3-micron CMOS processes.

Table 1. 5-Micron Gate Array Family

Circuit	Equivalent Two-Input Gates	Pads	LS Output Drivers	TTL Output Drivers
UA-1	300	40	17	20
UA-2	400	46	23	20
UA-3	540	52	25	24
UA-4	770	62	31	28
UA-5	1000	70	35	32
UA-6	1260	78	39	36

5-Micron Gate Array Family

The family of 5-micron CMOS products is offered in six configurations, summarized in Table I, with circuit complexities equivalent to 300, 400, 540, 770, 1000, and 1260 two-input gates, respectively. All pads can be individually configured as inputs, outputs, or I/O's. Input switching characteristics can be programmed for either CMOS or TTL compatibility. LS buffer output drivers will support CMOS levels of two low power schottky TTL loads. TTL buffer outputs will also provide CMOS levels and are capable of driving up to six LS TTL loads. All output drivers can be programmed for tri-state or open drain (open collector) operation as required.

The CMOS technology used for these products is AMI's state-of-the-art 5-micron, oxide-isolated, silicon gate CMOS process. This process offers all the conventional advantages of CMOS—i.e., very low power consumption, broad power supply voltage range (3V to 12V ± 10%), and high noise immunity—as well as dense circuits with high performance. Gate propagation delays are in the five to ten ns range for 5 volt operation at room temperature. AMI gate array products can be supplied in versions intended for operation over the standard commercial temperature range (0°C to + 70°C), the industrial range (– 40°C to + 85°C), or the full military range (– 55°C to + 125°C). MIL-STD-883 Class B screening, including internal visual inspection and high temperature burn-in, is offered. Similarly, customer-specified high reliability screening is available for commercial and industrial applications.

D.C. characteristics for the 5-micron gate array family are summarized in Table 2.

Table 2

Logic Element	2-Input Gate Equivalent
2-Input NOR	1
2-Input NAND	1
3-Input NOR	1.5
3-Input NAND	1.5
INVERTER	.5
D FLIP-FLOP W/RESET	5
D FLIP-FLOP W/SET-RESET	6
J-K FLIP-FLOP	8
CLOCKED LATCH	2.5
EXCLUSIVE OR	2.5
SCHMITT TRIGGER	2
4-BIT BCD CNTR W/RESET	27
TRANSMISSION GATE	.5

The current AMI array family, 300 gates to 1260 gates, is run in a 3-12V CMOS process (internally coded as CVA process). AMI is currently optimizing this array family for 3V to 5V operation (internally coded as CVH process). This new family, called UA-300 through UA-1260, is to be functionally identical to the existing UA-1 through UA-6. All design tools are interchangeable.

Customers who require 3V to 5V operation will be able to use the CVH family now. This optimized process will result in a 25-50% performance enhancement for 5V gate array designs. Customers who require operating voltages greater than 5V will continue to use the UA-1 to UA-6 CVA family.

In conjunction with these arrays, AMI has developed a set of "functional overlays." These are basic logic element building blocks—e.g. two input and larger gates of various types, flip-flops, and so forth—from which complete logic designs can be developed. Each functional overlay corresponds to a metal interconnect pattern that is superimposed on a set of uncommitted transistors (and polysilicon underpasses) in the array to implement the logic element. Typical functional overlay logic elements and the number of two-input gate equivalents they utilize are shown in Table 3.

Currently over 75 functional cells exist for this family.

3-Micron Gate Array Family

As part of AMI's long range semi-custom strategy in MOS/VLSI, AMI will continue to introduce new gate array products. These new products will offer performance and cost advantages not currently realizable. In conjunction with these new array products, AMI has introduced computer-aided design tools to automate the entire gate array design process.

The newest gate array family is the high-performance GA and GA-D series which is based on AMI's 3-micron CMOS silicon gate process technology. With a 3-micron drawn geometry, it is equivalent to a 2-micron effective channel length which is the state-of-the-art.

The AMI GA and GA-D series are designed for 5V operation over military temperature range (−55 to 125°C). Besides high speed (2 to 3ns typical delay) and high density (up to 5K gates), it features total I/O flexibility in that each I/O pad can be one of any 13 options.

The single metal version provides up to 2500 gates and the double metal GA-D version 5000 gates. See Table 3 for configurations.

Table 3. 3-Micron Gate Array Family

Process	Product No.	Gates	Pads
Single Metal	GA-2500	2500	84
	GA-2000	2025	74
	GA-1500	1500	64
	GA-1000	1020	52
	GA-500	540	40
Double Metal	GA-5000D	4995	134
	GA-4000D	4012	120
	GA-3000D	3080	102
	GA-2000D	2016	84
	GA-1000D	1024	64

In conjunction with these new array products, AMI will have a complete powerful set of design automation software to allow users complete design flexibility. Using a terminal tied to a central AMI owned or customer owned minicomputer or mainframe, the user will have access to a complete set of design automation software tools including:

- Schematic digitization and capture
- Logic simulation
- Circuit simulation
- Test vector generation
- Interactive or autoplace and route
- Auto continuity checking

These tools will allow the user to partially or fully automate the design task for maximum flexibility.

Customer Interfaces

Unlike other gate-array vendors, AMI offers all the services required to develop and fabricate a semi-custom circuit. In-house capabilities include circuit and logic simulation, mask making, full wafer fabrication, assembly, and test.

Gate Arrays

Gate array developments are supported in two basic ways:

1) **The AMI-Tooled Interface** is available to customers with little or no experience in semi-custom circuit development, or to experienced users with limited in-house capabilities. In these cases AMI requires a logic diagram or breadboard schematic of the circuit to be integrated, along with D.C. and A.C. specifications, and functional patterns in I/O format.

At the end of the development phase, the customer receives 25 fully tested prototypes, assembled in ceramic packages, which have been subjected to our stringent Q.A. screening requirements.

2) The **Customer-Tooled Interface** is more applicable to customers with multiple circuit development requirements and suitable in-house design capabilities. For these customers AMI will supply the necessary software tools which have been written in FORTRAN and PASCAL languages so they will be compatible not only with PRIME computers, as is presently the case, but also with VAX and IBM minis. The user in turn provides AMI with either a database tape in CALMA format, or an ELECTROMASK or DAVID MANN compatible pattern generator tape, along with test requirements. A debugged SENTRY program is preferred. AMI will then fabricate and test 25 prototypes which should be representative of the production units.

Software Support

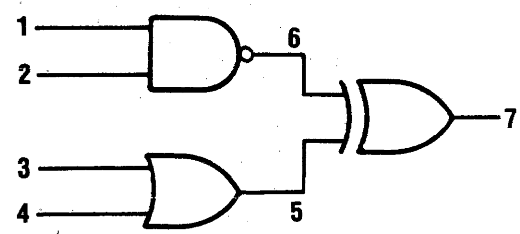
AMI CAD Technology (ACT™) is the most advanced integrated software package for CMOS/VLSI design available in the industry. It uses a common database for logic simulation, mask layout and test program generation. By operating from a common database, a gate array design can be converted into a standard cell or a fully crafted custom circuit with minimal risks.

The heart of the system is BOLT™ (Block Oriented Logic Translator) which is at the same time a hardware description language and a compiler. It allows the system designer to describe the logic network in a hierarchical fashion due to an unlimited macro nesting capability.

The common data base is created in a very simple fashion, consistent with the way that logic files are created in most timeshared logic simulators. Figure 2 shows a simple logic network and the corresponding BOLT™ file which allows programmability of rise and fall times for all gates.

GLIDE™ is the graphics editor on Prime used for interactive design of the single metal families of arrays. TRACE™ is a module that checks the layout database for continuity, and COMPARE™ verifies that the layout matches the BOLT™ logic file.

Figure 2.




```
6 ° NAND   1  2 (TDR = XX, TDF = XX);
5 ° OR     3  4 (TDR = XX, TDF = XX);
7 ° EXOR   5  6 (TDR = XX, TDF = XX);
```

GAPAR™ is the software module that allows automatic placement and routing of the double metal family of arrays. It is designed to complete at least 98% of the wiring connections on a 100% utilized array, based on a 90% confidence level using Donath-Heller-Milkhail two-dimensional model. The GAPAR™ system also offers interactive routing tools which can be used to complement the auto router when overflow conditions exist or to manually route critical delay paths.

CAPACITANCE™ calculates the actual capacitive load of the active gates from the layout database. The capacitance parameters are different for poly and metal interconnections, and for aluminum over diffusions or field oxide. In conjunction with DELAY™, it allows to accurately predict the dynamic behavior of the actual integrated circuit before it is fabricated.

TESTGEN™ is used to generate efficiently compressed functional test patterns based on the results of logic simulations from SIMAD™. This pattern compression minimizes the use of local memory on Sentry testers.

TESTPRO™ operates on Prime, allowing off-line generation of D.C. parametric tests in Factor language used in Fairchild test systems. Its output is merged with the compressed functional patterns from TESTGEN™, and the result is a full dynamic test program that can be tailored for use in any Sentry tester.

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Gate Arrays

Packages

Pinout or lead count varies with die size and array complexity. The arrays are offered in standard plastic and ceramic dual-in-line packages with pin counts ranging from 16 to 64, JEDEC-Standard leadless and leaded chip carriers, miniflat packs to 84 pins, and pin grid arrays to 144 pins. AMI gate array products are also available in wafer or unpackaged die form.

5-Micron Gate Array Series

DC Characteristics—TTL Interface Specified @ $V_{DD} = +5V \pm 10\%$; $V_{SS} = 0$; Temperature = −55°C to +125°C

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	2.0		V_{DD}	V
V_{IL}	Input Low Voltage	0.0		0.8	V
V_{OH}	Output High Voltage (LS Buffer $I_{OH} = -700\mu A$) (T Buffer $I_{OH} = -1.5mA$)	2.7 2.4			V V
V_{OL}	Output Low Voltage (T Buffer $V_{OL} = 2.4mA$) (LS Buffer $I_{OL} = 0.8mA$)			0.4 0.4	V V
I_{OZ}	3-State Output Leakage $V_O = 0$ or V_{DD}	−10	1	10	µA

DC Characteristics—CMOS Interface

Sym.	Parameter	V_{DD}	Limits: *T Low Min	*T Low Max	25°C Min	25°C Typ	25°C Max	*T High Min	*T High Max	Units	Condition
I_{DD}	Quiescent Device Current	5V 10V		0.1 0.2		.001 .002	0.1 0.2		1 2	µA/gate µA/gate	$V_{IN} = 0$ or V_{DD}
V_{OL}	Low Level Output Voltage			0.05			0.05		0.05	V	$I_O = 1\mu A$
V_{OH}	High Level Output Voltage	5V 10V	4.95 9.95		4.95 9.95			4.95 9.95		V V	$I_O = -1\mu A$
V_{IL}	Input Low Voltage	5V 10V	0.0 0.0	1.5 3.0	0.0 0.0		1.5 3.0	0.0 0.0	1.5 3.0	V V	
V_{IH}	Input High Voltage	5V 10V	3.5 7.0	5.0 10.0	3.5 7.0		5.0 10.0	3.5 7.0	5.0 10.0	V V	
I_{OL}	Output Low (Sink) Current T Buffer LS Buffer	5V 10V 5V 10V	3.2 6.0 1.0 1.8		3.2 6.0 1.0 1.8	4.8 9.0 1.6 3.1		2.4 4.0 0.8 1.0		mA mA mA mA	$V_O = 0.4V$ $V_O = 0.5V$ $V_O = 0.4V$ $V_O = 0.5V$
I_{OH}	Output High (Source) Current T Buffer LS Buffer	5V 10V 5V 10V		−600 −1120 −300 −560			−600 −1120 −300 −560		−500 −940 −250 −470	µA µA µA µA	$V_O = 4.6V$ $V_O = 9.5V$ $V_O = 4.6V$ $V_O = 9.5V$
I_{IN}	Input Leakage Current			1			1		1	µA	$V_{IN} = 0$ or V_{DD}
I_{OZ}	3 State Output Leakage Current			±1			±1		±10	µA	$V_O = 0$ or V_{DD}
C_I	Input Capacitance					5				pF	Any Input

*Military temperature range is −55°C to +125°C
Industrial temperature range is −40°C to +85°C
Commercial temperature range is 0°C to +70°C

Gate Arrays

Absolute Maximum Ratings

Supply Voltage, V_{DD}	$-.5V$ to $+7V$
Input Voltage, V_{IN}	$-.5V$ to $V_{DD}+.5V$
D.C. Input Current, I_I	$\pm 10mA$
Storage Temperature, T_{STG}	$-65°$ to $+150°C$

3-Micron Gate Array Series

D.C. Electrical Characteristics: $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_A = -55°$ to $+125°C$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{DD}	Quiescent Supply Current		10	50	μA	$V_I = V_{DD}$ or V_{SS}
V_{OL}	Low Level Output Voltage			.05	V	$I_{OL} = 1\mu A$
				.4	V	$I_{OL} = 3.2mA$
V_{OH}	High Level Output Voltage	4.95			V	$I_{OH} = -1\mu A$
		2.40			V	$I_{OH} = -5mA$
V_{IL}	Low Level Input Voltage	−.5		.8	V	TTL Interface
		−.5		1.5	V	CMOS Interface
V_{IM}	High Level Input Voltage	2.0		$V_{DD}+.5$	V	TTL Interface
		3.5		$V_{DD}+.5$	V	CMOS Interface
I_{IN}	Input Leakage Current			1	μA	$V_{IN} = V_{DD}$
I_{OZ}	High Impedance Output Leakage Current	−10	.001	10	μA	$V_{OH} = V_{DD}$ or V_{SS}
C_{IN}	Input Capacitance		5		pF	Any Input

Table 4. Propagation Delay Characteristics for AMI Gate Arrays
A.C. Characteristics: $T_A = 25°C$, $V_{DD} = 4.5V$, F.O. = 2

Function		Gate Delays			Units
		5μ	3μ S.M.	3μ D.M.	
INVERTER	L-H	6.0	4.5	3.4	ns
	H-L	5.3	1.3	1.0	ns
2INPUT NAND	L-H	9.0	5.8	4.4	ns
	H-L	9.0	1.8	1.4	ns
2INPUT NOR	L-H	12.0	8.4	6.3	ns
	H-L	8.2	1.5	1.1	ns
D-TYPE F/F					
MAX FREQUENCY		15	36	45	MHz
TTL INPUT BUFFER		18	7	5	ns
OUTPUT BUFFER					
DELAY ($C_L = 30pF$)		20	9	6.7	ns

NOTE: BASED ON WORST CASE PROCESS PARAMETERS. FOR TYPICAL DATA, DIVIDE GATE DELAYS BY 1.8.

Standard Cells

AMI's Standard Cells

Program Description

The cells in the Standard Cell Program are basic logic elements such as gates, flip-flops, register counter bits and I/O devices. Each cell has been previously designed and analyzed for performance. Complex digital functions can be rapidly implemented by interconnecting the various cells. Most cells have a series 4000 CMOS equivalent and a 74LS TTL equivalent for ease of breadboarding.

The cells are initially designed on an interactive color graphics terminal — AMI's SIDS (symbolic interactive design) system. The cell library is maintained within the SIDS data base. If other CAD (Computer-Aided Design) systems are used internally by a customer, the cell library can be digitized onto these systems.

Using the SIDS system, new cells or modifications of existing cells can be generated and added to the cell library rapidly, without any hand layout. Similarly, non-cell functions such as analog elements or memory arrays, RAM or ROM, can be designed using SIDS and merged with standard cells.

This ability to add special features efficiently makes AMI's standard cell program far more flexible than other manufacturer's cell development systems.

Table 5. Standard Cell Offerings

Part No.	Process Technology		Availability
XXXX-001	5μ CMOS	Single Metal	NOW
XXXX-001	4μ NMOS	Single Metal	NOW
XXXX-001	3μ CMOS	Single Metal	NOW
XXXX-001	3μ CMOS	Double Metal	NOW
XXXX-001	2μ CMOS	Double Metal	2Q'84

Performance

AMI's standard cell circuits can be successfully used in digital circuits with operating speeds up to 10MHz for NMOS (or CMOS at 10V V_{CC}) up to 40MHz for CMOS (5V V_{CC}). It should be emphasized that if only a small portion of the circuit requires faster performance, this portion can be "customized" either by creating special cells or by designing circuitry outside of the cell structure. AMI will review customer logic without obligation to determine if a cell design is feasible.

Features

The high speed, high performance 3-micron cell families are also available. These cells are designed in AMI's 3-micron single and double layer metal process. They have been characterized for 3-5V operation and over the full military temperature range. As in 4000 series CMOS, power for static operation is near zero.

3-Micron Single Metal Standard Cells

- State-of-the Art CMOS Technology
- 3-Micron Single Metal Cell as Basic Building Block
- Same Macros and Performance for Cells and Arrays

3-Micron Double Metal Standard Cells

- Automatic Placement and Routing
- Cells are Designed to Exceed the Performance of 3-Micron DLM Gate Arrays
- Fixed Cell Height/Variable Width
- Characterized at 25°C, 70°C, and 125°C with $V_{DD} = 4.5V$

NMOS Cells

This family is AMI's most complete cell family with over 135 cells in 4 speed/power combinations. V_{DD} and V_{SS} connections are metal lines running horizontally across the cell. Two other metal lines, usually used for clock signals, also run across the cell. Typical and worst case inverter delays are 5.5ns and 10.0ns, respectively.

The NMOS cells are implemented using a 4-micron silicon gate process and can be used over the full military temperature range (−55°C to 125°C). Operating voltage is 5V ± 10%. The NMOS cells have been designed with three power/speed options. The fastest cells also have the highest power consumption and use the most area. Therefore, the fast cells should be used only where circuit performance requires high speed. Most circuits are optimized by using a combination of low power, standard and high speed cells.

CMOS Cells

The CMOS cells are designed using a 5-micron silicon gate oxide-isolated process and using 3-micron single and double layer metal process. These processes are well suited for analog circuitry and some analog cells will be added to the digital cells. The 5-micron CMOS cells are characterized for 3V to 12V operation over the full military temperature range (−55°C to 125°C). CMOS cells are generally used where low power battery operation or backup are required.

AMI Standard Development

The circuit user provides a completed logic diagram and a circuit specification. AMI performs all other design activity including MOS logic design, circuit design, layout, mask generation and fabrication of wafers. This development option is recommended for most users desiring to build a single LSI device and for multiple circuit users who do not wish to become directly involved in the MOS circuit development.

Developing Your Standard Cell Design

AMI offers three basic options for developing a standard cell custom circuit. All of these apply to the Development Flow Diagram of Table 7.

Table 7. Gate Array/Standard Cell Development Flow

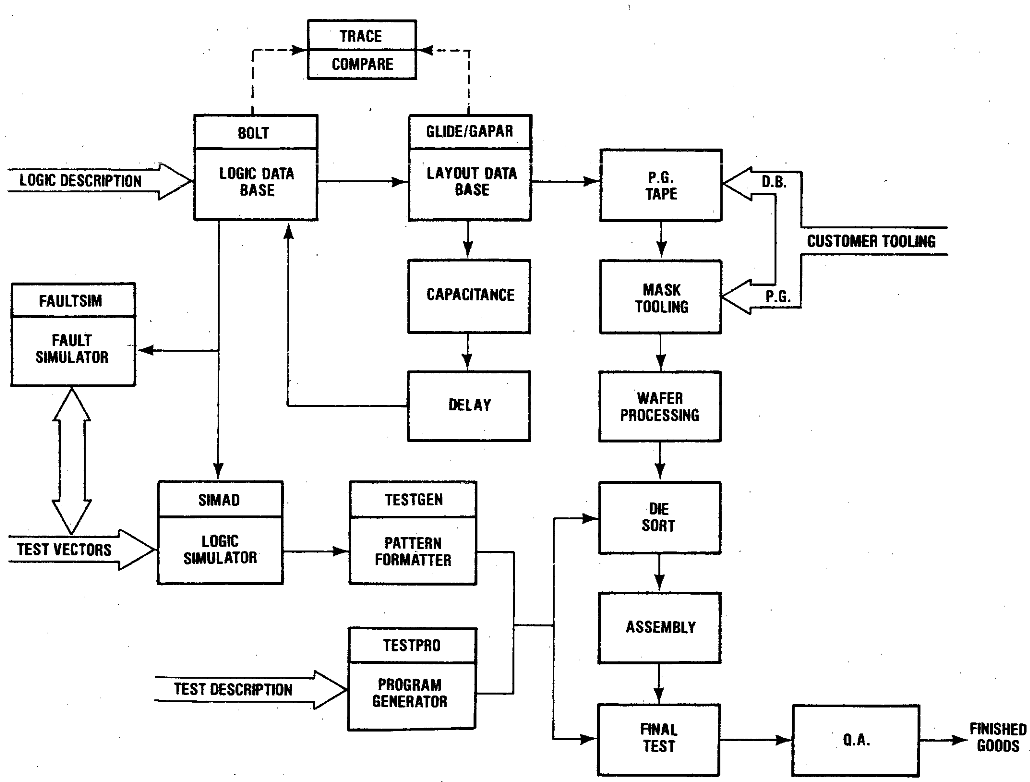

Table 8. AMI Standard Cell
3-Micron Single Metal Interface

	Logic Diagram Input		Net List Input	
No. of Gates	Cost	Max. Span	Cost	Max. Span
500	$19.7K	9 Weeks	$15.7K	7 Weeks
1000	$22.8K	11 Weeks	$16.8K	9 Weeks
2000	$31.3K	13 Weeks	$21.3K	11 Weeks

We're the last people you need to call

Look around; compare price, compare yield, compare turnaround time . . . then call BRI. We welcome your toughest VLSI design problem. Gate arrays, standard cell, PLS/PAL, Bi-CMOS, you name it. We've got a fully computerized design solution and a fabrication technique that will give you what you need, when you need it, at the right price. Volume is no obstacle.

BRI has combined a fully computerized and world-wide-accessible VLSI design system with high-volume, high-yield fabrication facilities to provide our clients with products offering both reduced die size and superior electrical characteristics. From initial design through final component assembly, or at any step in the process, BRI can bring an imaginative and cost-effective solution to your VLSI requirements. We don't have to be the first people you call but, when it comes to a final decision, we're determined to be the last.

for Semi-Custom I.C.s

Standard Cell

BRI's computer aided VLSI design features an extensive cell library which includes 7400 series, ROM/RAM and analog functions. This allows customized circuit design at lower cost and in less time. The 2 micron HCMOS dual layer metal process technology and advanced design techniques provide both increased circuit performance and reduced die size.

Gate Array

The 2 micron HCMOS dual layer metal process technology is supported by a fully automated design system to provide a family of gate arrays with 1.6 ns maximum propagation delay. All BRI gate array products are specifically designed for quick turn-around, high performance and low cost.

Analog/Digital Gate Array

Fabricated with the Bi-CMOS process technology, these arrays offer analog functions with true bipolar characteristics and low power CMOS ditigal functions in one cost-effective device. This allows the customer to maximize system integration while protecting his prioriet ary design.

PAL/PLS

These 2 micron HCMOS mask programmable products provide bipolar speed and CMOS power dissipation for greater reliability and lower cost. They are pin compatible with Signetics PLS and MMI PAL series.

For full facts on these and other BRI custom and semi-custom products, give us a call.

BRI

BARVON RESEARCH, INC.

2680 N. First St., Suite 210 • San Jose, CA 95134
Telephone: (408) 262-8368 • TELEX: 17-1627 • TWX: 910-379-0029

MA Series High Speed CMOS Gate Arrays 3μ Silicon Gate CMOS

Preliminary

Benefits

- ☐ Integrate HCMOS or standard TTL functions easily
- ☐ Reduce component count
- ☐ Reduce power dissipation and consumption
- ☐ Introduce new products quickly
- ☐ Improve system reliability
- ☐ Protect innovative designs longer

Features

- ☐ Typical propagation delay (t_p) <2.0 nsec
- ☐ Circuit/package flexibility
- ☐ Quiescent current: 0.01μA/gate
- ☐ Dedicated VLSI CAD system with complete software support
- ☐ Library of pre-designed macro cells
- ☐ Input protection on all pads
- ☐ Rapid design cycle—from 6 to 12 weeks depending on array size

General Description

The MA series of gate arrays is produced on Citel's 3μ silicon gate CMOS process, a state-of-the-art technology featuring oxide isolation, isoplanar structures and shallow functions for high speed and high density. As a fully licensed second source for both design and complete fabrication of Matra Harris gate arrays, Citel offers an extensive library of fully characterized macro cells which enables a rapid, yet reliable, logic implementation of any cell on any array.

Gate array design activity is performed on the Gatemark VLSI design system which includes such capabilities as schematic or net list entry, logic simulation, interactive layout, automatic place and route and a layout/net list check.

In addition to design and wafer fabrication, Citel offers a wide range of package options and a complete S-VII test capability for both wafer sort and final test. The I/O pad-to-gate ratio permits wide flexibility in package selection (e.g., the MA0400 fits a standard 20-pin DIP yet also provides 40 pads for those with high I/O needs). The MA Series currently includes four arrays ranging from 200 to 1200 gates. Additional semi-custom arrays and a complete library of standard cells for full custom CMOS design are in development.

Citel

CUSTOM/SEMICUSTOM

Citel 3μ CMOS Gate Array Family (MA Series)

Part No.	Gate Count	Pad Count	Packages: Plastic DIP	Packages: Ceramic	Packages: LCC	Cells Available
MA0200	228 & 28 I/O	32	8-28 pins	14-28 pins	14-28 pins	AND/OR/INV — 14 NAND/NOR/AND-OR-INV/EXOR — 19 Latches — 5 JK/D/RS Flip Flops — 17 MSI Functions — 10 (Counters, Adders, Registers) I/O Cells — 10 Misc. Functions — 7
MA0400	380 & 36 I/O	40	8-40 pins	18-40 pins	28-40 pins	
MA0800	754 & 50 I/O	54	22-40 pins	22-48 pins	32-64 pins	
MA1200	1139 & 62 I/O	66	24-40 pins	24-64 pins	40-64 pins	

CITEL

3060 Raymond Street ☐ Santa Clara, CA 95050
(408) 727-6562 TWX: 910-338-0540

Absolute Maximum Ratings

Supply Voltage .... -0.5 to +7.0V
Input/Output Voltage .... -0.3 to V_{DD} + 0.3V
Storage Temperature .... -65°C to +150°C

DC Electrical Characteristics (V_{DD} = 5V ±10%; -55°C to +125°C)

Parameter	Symbol	Min.	Typ	Max	Units	Conditions
Low-level Input Voltage (TTL)	V_{IL}	—	—	0.8	V	Input Buffer Cells
Low-level Input Voltage (CMOS)	V_{IL}	—	—	1.5	V	V_O = 4.5V; I_O = 0
High-level Input Voltage TTL	V_{IH}	2.2	—	—	V	Input Buffer Cells
High-level Input Voltage CMOS	V_{IH}	3.5	—	—	V	V_O = 0.5V; I_O = 0
Low-level Output Voltage	V_{OL}	—	0.2	0.4	V	I_{OL} = 3.2 mA
High-level Output Voltage	V_{OH}	3.9	—	—	V	I_{OH} = −100μA
Input Leakage Current	I_{IL}	-1	0.01	+1	μA	V_{IN} = 0V or V_{DD}
Standby Supply Current	I_{DD}	—	0.01	—	μA/Gate	

AC Electrical Characteristics (V_{DD} = 5V; Fan-out = 2 gates; T_{PD} = ½ (T_R + T_F)

Parameter	Typ (25°C)	Max (0° to 70°C)	Max (-55° to 125°C)	Units
Propogation Delay (t_p)				
Inverter	1.3	3.0	4.0	nsec
4-Input NAND	1.9	4.6	6.0	nsec
4-Input NOR	4.0	10.0	11.0	nsec
Input Buffer	2.2	7.0	9.0	nsec
Output Buffer (50pF)	13.0	20.0	25.0	nsec
Dynamic Supply Current	5.0 (max)	—	—	μA/MHz/Gate

Citel's capabilities also include full-custom MOS and bipolar integrated circuits and Universal Programmers. Complete information available upon request.

CITEL
3060 Raymond Street □ Santa Clara, CA 95050
(408) 727-6562 TWX: 910-338-0540

CUSTOM MOS ARRAYS, INC. 211 Topaz Street Milpitas, CA 95035 (408) 946-9111 TWX 910-338-2304

CMA Silicon Gate HCMOS Gate Arrays
CMA 2000 Series

GENERAL

The CMA 2000 Series of gate arrays from Custom MOS Arrays (CMA) are a high-performance family of gate arrays, with complexity ranging from 400 to 2400 gates and pin count ranging from 40 to 110 pins.

The CMA 2000 Series uses 3-micron technology with single-level metal and programmable via holes for interconnects, and offers Schottky TTL speeds and CMOS power consumption.

FEATURES

- 400–2400 Gate Complexity
- Up to 110 Input/Output (I/O) Pins
- Schottky TTL Speeds
- Reliable and Proven 3-micron HCMOS Technology
- Fully Characterized to Military Temperature Range
- Hermetic and Plastic Packaging
- Supports 7400/4000 SSI/MSI Functions
- Full TTL/CMOS Interface Compatibility
- Ultra-Low Leakage and Standby Currents
- Proprietary Latch-Up (SCR) Resistant Design
- Proprietary Static Protection Circuits
- Hermetic Packaged Parts are Processed to MIL-STD-883, Class C

PRODUCT DESCRIPTION

The CMA 2000 Series of gate arrays are manufactured using proven oxide-isolated HCMOS technology. Single-level metal interconnect enables CMA to obtain higher yields and hence lower production cost.

The gate arrays are organized as arrays of cells, and individual N and P channel transistors are configured into a variety of logic elements called macrocells. CMA's current macrocell library is detailed in Appendix 1.

A variety of Input/Output (I/O) configurations is available:

- All I/O pads are configurable as inputs, outputs or bi-directional tri-states.
- All I/O pads can have active pull-ups or pull-downs.
- Any input may make use of TTL input shifters for TTL requirements.
- All I/O pads can drive multi-TTL loads and may be paralleled for increased drive.

The CMA 2000 Series of gate arrays are ideal in applications where speed, space and power are at a premium.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3~7	V
V_I	Input voltage	With respect to GND	−0.3~7	V
T_{opg}	Operating ambient temperature (Military)		−55~+125	°C
T_{opg}	Operating ambient temperature (Commercial)		0~70	°C
T_{stg}	Storage temperature (Hermetic)		−65~150	°C
T_{stg}	Storage temperature (Plastic)		−40~125	°C

PRODUCT OUTLINE

Array Number	Complexity	Max. I/O Pads	Technology	Gate Speed*
CMA 2004	400	40	3-micron	4.5 ns
CMA 2008	800	60	3-micron	4.5 ns
CMA 2011	1100	68	3-micron	4.5 ns
CMA 2015	1500	80	3-micron	4.5 ns
CMA 2024	2400	110	3-micron	4.5 ns

***Notes on Gate Speed:** 1. Two-input NAND gate, fanout = 3 with 3 mm interconnect. 2. $T_A = 70°C$, $V_{DD} = 5V \pm 10\%$. 3. $T_{pd} = ½ \cdot (T_{pLH} + T_{pHL})$.

PROPAGATION DELAYS

In CMOS technology the propagation delay is a function of:

- Fanout
- Interconnect Routing
- Supply Voltage
- Temperature
- Processing
- Input Slew Rate/Polarity

CMA's CAD system takes all of these variables into account (except Input Slew Rate/Polarity) during simulation.

After the design netlist has been entered into CMA's CAD system the worst-case delay of each cell is automatically determined, taking into account the affects of fanout and estimated interconnect capacitance.

After interconnect routing is completed, the actual interconnect loading is calculated automatically from the database and automatically inputted into the simulator and final design verification is completed.

The effects of supply voltage and temperature are illustrated in Figures 1 and 2 below. A rule of thumb for processing variation is 35% to give worst-case delay figures.

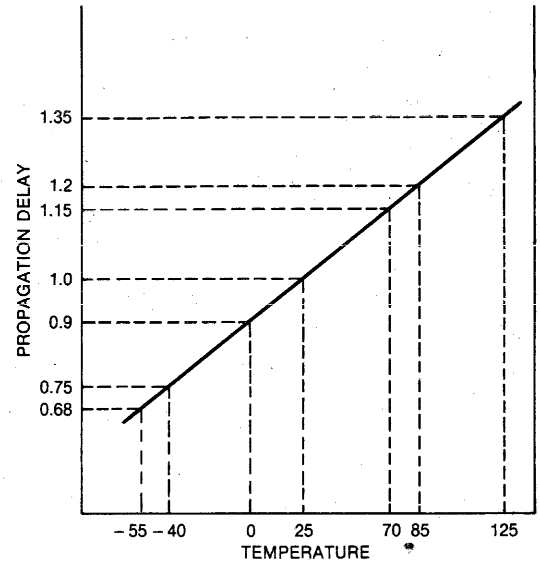

Figure 1. CMOS Delay vs. Temperature

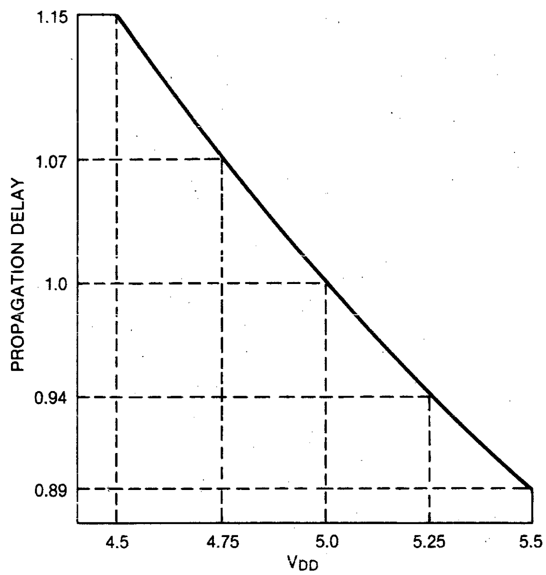

Figure 2. CMOS Delay vs. Supply Voltage

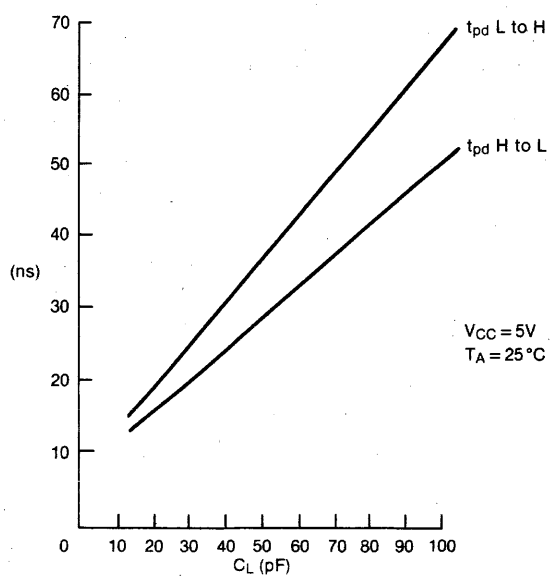

Figure 3. CMOS Driver Delay vs. Output Loading

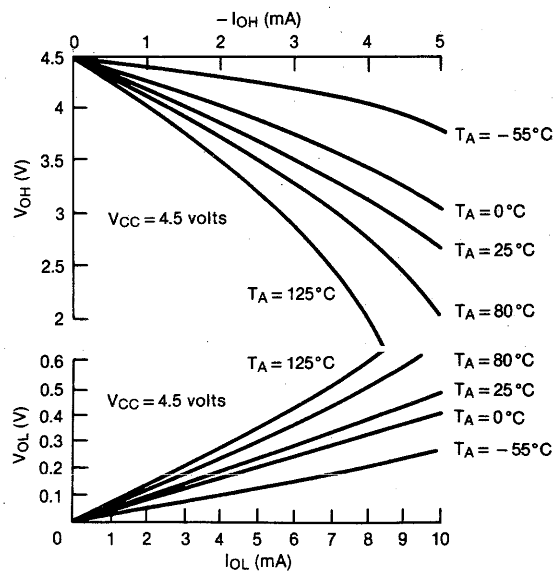

Figure 4. Output Current Drive

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DC CHARACTERISTICS ($T_A = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$)

Symbol	Parameter	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
V_{IH}	High-level input voltage		2.0		V_{CC}	V
V_{IL}	Low-level input voltage		−0.3		0.8	V
V_{OH}	High-level output voltage	$I_{OH} = +1$ mA	2.4			V
V_{OL}	Low-level output voltage	$I_{OL} = 4$ mA			0.4	V
I_{IL}	Input current	$V_I = 0 \sim 5.5V$			±10	μA

POWER CONSUMPTION

In CMOS, power dissipation is a function of three elements:

- Charging and discharging circuit nodes, usually 90% total power.
- Overlap currents when P and N transistors switch, usually 10% power.
- Leakage (DC power). This is negligible, a few microwatts.

Charging and discharging circuit nodes and the associated power consumption may be calculated using the equation $P = CV^2f$, where C is node capacitance, V is supply voltage, and f the operative frequency. The following example illustrates a typical power supply calculation.

Parameter	Gate Array CMA 2004	Gate Array CMA 2024
No. of Gates	400	2400
Percent Utilization (80%)	320	1920
No. of Switching Nodes (15%)	48	288
No. of Outputs Utilized	20	80
Output Load Capacitance	45 pF	45 pF
No. of Outputs Switching (20%)	4	16
Supply Voltage	5V	5V
Core Dissipation per MHz	0.6 mW	3.6 mW
Output Dissipation per MHz	4.5 mW	18 mW
At 10 MHz Clock Speed	51 mW	216 mW
At 30 MHz Clock Speed	153 mW	648 mW

Note: Overlap power is taken into account by increasing the nodal capacitance in the above calculation.

PRODUCT OPTIONS

The CMA 2000 Series are offered in a variety of operating temperature ranges and packages.

- Military Operating Range: −55°C to +125°C
- Industrial Temperature Range: −40°C to +85°C
- Commercial Temperature Range: 0°C to +70°C
- MIL-STD-883 Levels B and C Screening
- Most commercial packages are available as well as unpackaged die.

EQUIVALENT GATE COMPLEXITY

One of the first tasks in converting your logic functions into a gate array is to estimate its logic complexity. CMA defines gate count in terms of 2-input NAND gate equivalents.

Tables 1 and 2 list the approximate equivalent CMOS 2-input NAND gate count of most of the popular 7400 and 4000 Series SSI/MSI functions.

GATE ARRAY DEVELOPMENT SYSTEM CMA 2000 SERIES

The CMA CAD system is configured to allow generation of error-free designs. The desired logic functions are entered into the system and logical and timing verification is completed via CMA's simulator. The simulated input patterns and corresponding outputs are checked for completeness and other tests added until the final test patterns are completed. The flow diagram below illustrates the design cycle.

CMA's CAD team is currently working on a personal gate array development system for customer design verification. If you are interested in more details of the personal CMA 2000 Series, contact our applications department.

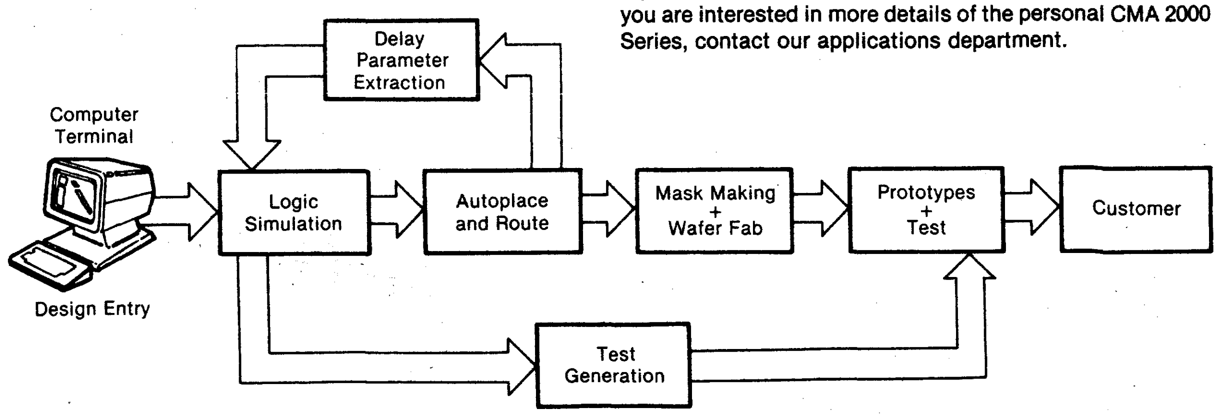

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Table 1. 7400 Equivalent Gate Count

Part No.	Gate Equivalent	Part No.	Gate Equivalent	Part No.	Gate Equivalent	Part No.	Gate Equivalent
7400	4	7470	16	74152	24	74253	40
7401	4	7471	15	74153	27	74257	36
7402	4	7472	14	74154	33	74258	34
7403	4	7473	20	74155	21	74259	48
7404	4	7474	15	74156	21	74260	6
7405	3	7475	14	74157	22	74261	58
7406	3	7476	20	74158	23	74265	7
7407	6	7477	14	74159	18	74266	10
7408	6	7478	20	74160	68	74273	50
7409	6	7480	17	74161	68	74274	70
7410	6	7481	80	74162	68	74275	70
7411	8	7482	27	74163	68	74276	40
7412	6	7483	57	74164	43	74278	34
7413	14	7484	80	74165	85	74279	10
7414	30	7485	73	74166	62	74280	24
7415	8	7486	12	74167	52	74281	170
7416	3	7487	19	74168	80	74283	59
7417	6	7489	320	74169	80	74284	58
7420	6	7490	40	74170	116	74285	58
7421	5	7491	43	74172	205	74289	280
7422	4	7492	41	74173	56	74290	48
7423	6	7493	41	74174	37	74293	45
7425	6	7494	42	74175	25	74295	57
7426	4	7495	42	74176	42	74298	32
7427	6	7496	44	74177	41	74299	188
7428	4	7497	120	74178	56	74323	188
7430	6	7498	33	74179	56	74348	64
7432	4	7499	46	74180	20	74351	124
7433	4	74100	18	74181	100	74352	26
7437	4	74102	14	74182	30	74353	39
7438	4	74103	20	74183	16	74362	44
7440	4	74106	20	74184	100	74363	28
7442	29	74107	20	74185	100	74364	48
7443	29	74108	20	74190	80	74365	37
7444	29	74109	21	74191	76	74366	40
7445	29	74110	14	74192	62	74367	37
7446	45	74111	20	74193	58	74368	40
7447	45	74116	26	74194	70	74373	58
7448	45	74120	15	74195	46	74374	74
7449	45	74135	24	74196	42	74375	16
7450	6	74136	12	74197	41	74376	40
7451	5	74138	23	74198	92	74377	48
7452	8	74139	20	74199	85	74378	34
7453	7	74141	16	74225	450	74379	24
7454	7	74142	90	74226	116	74381	150
7455	6	74143	45	74245	83	74386	12
7460	6	74144	98	74246	51	74390	86
7461	6	74145	24	74247	51	74393	80
7462	9	74147	35	74248	51	74395	50
7464	8	74148	35	74249	51	74398	22
7465	8	74150	60	74251	37	74399	22
		74151	24			74670	144

Table 2. 4000B Equivalent Gate Count

Part No.	Gate Equivalent	Part No.	Gate Equivalent	Part No.	Gate Equivalent	Part No.	Gate Equivalent
4000	5	4038	74	4153	32	4515	69
4001	4	4040	74	4155	22	4516	66
4002	4	4041	4	4157	24	4518	26
4006	108	4042	12	4158	24	4519	28
4007	2	4043	20	4160	64	4520	54
4008	32	4044	20	4162	64	4521	123
4009	5	4051	6	4163	64	4522	44
4010	5	4068	4	4164	51	4526	47
4011	4	4069	3	4166	84	4530	16
4012	4	4070	12	4174	38	4531	36
4013	10	4071	6	4175	25	4532	39
4014	43	4072	4	4192	60	4534	190
4015	62	4073	8	4193	56	4539	24
4017	45	4074	14	4273	50	4554	40
4018	52	4075	8	4373	58	4555	22
4019	12	4076	41	4374	74	4556	22
4020	40	4077	12	4375	14	4558	65
4021	43	4078	4	4386	12	4560	78
4022	35	4081	4	4501	6	4580	187
4024	44	4082	4	4504	33	4581	100
4026	65	4089	84	4505	271	4582	31
4027	20	4093	32	4506	1[illegible]	4583	23
4028	22	4094	86	4508	24	4584	30
4029	68	4099	64	4510	94	4585	35
4030	12	4106	30	4511	136	4597	103
4032	68	4107	18	4512	31	4598	74
4034	110	4138	20	4514	69	4599	42
4035	48	4139	10				

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Gate Array Products

Sept 1983

Gate Array Division

Fairchild's high performance gate arrays feature a wide range of gate counts and offer minimal circuit delays. The FGT0750 and the FGE1000 and FGC6000 series complement the FAST™, F100K ECL and HCMOS logic families respectively, allowing for easy integration of standard SSI/MSI functions into a unique LSI chip. Designs for all arrays are implemented using pre-defined SSI/MSI functions (macros). Fairchild's complete Computer-Aided Design System, FAIRCAD™, reduces development time and assures first time success.

Product	Gate Equiv.	Technology	I/O Levels	Typical Internal Gate Delay (ns)	Typical Buffer Delay		P_D Typ (W)†	I/O	Packaging	Available
					Input (ns)	Ouptut (ns)				
FGE0020	20	ECL	100K ECL	0.35	N/A	0.55	0.5	21	24 F/P	Now
FGE0500	500	ECL	100K/10K ECL	0.3-1.5	N/A	0.55	1.5-4.0	72	84-Pin CC 84-Pin Grid	Now
FGE2000	2000	ECL	100K/10K ECL	0.3-1.5	N/A	0.55	4.0-9.0	126	132-Pin CC 132-Pin Grid	Now
FGT0750	1000	FAST	TTL	1.8	1.8	3.0	1.0	76	68-, 84-Pin CC 68-, 84-Pin Grid	Now
FGC0500	540	2μ CMOS	TTL/ CMOS	1.5	2.0	6.0		40	28, 48 DIP 44 F/P	4Q '83
FGC1200	1242	2μ CMOS	TTL/ CMOS	1.5	2.0	6.0		73	40, 68 DIP 68, 84 PGA 68, 84 LCC	3Q '84
FGC2400	2625	2μ CMOS	TTL/ CMOS	1.5	2.0	6.0		109	84, 120 PGA 68, 84 LCC 84 LDCC 64 DIP	1Q '84
FGC4000	4020	2μ CMOS	TTL/ CMOS	1.5	2.0	6.0		133	120, 144 PGA 144 LDCC 64 DIP	3Q '84
FGC6000	6000	2μ CMOS	TTL/ CMOS	1.5	2.0	6.0		161	172 PGA 172 LDCC 64 DIP	2Q '84

†For the CMOS arrays, maximum power dissipation = 20 μW/switching gate/MHz.

For further information on product availability, CAD training and design schedules write to: Gate Array Marketing, 1801 McCarthy Blvd., Milpitas, CA 95035, or call (408) 942-2672.

Fairchild

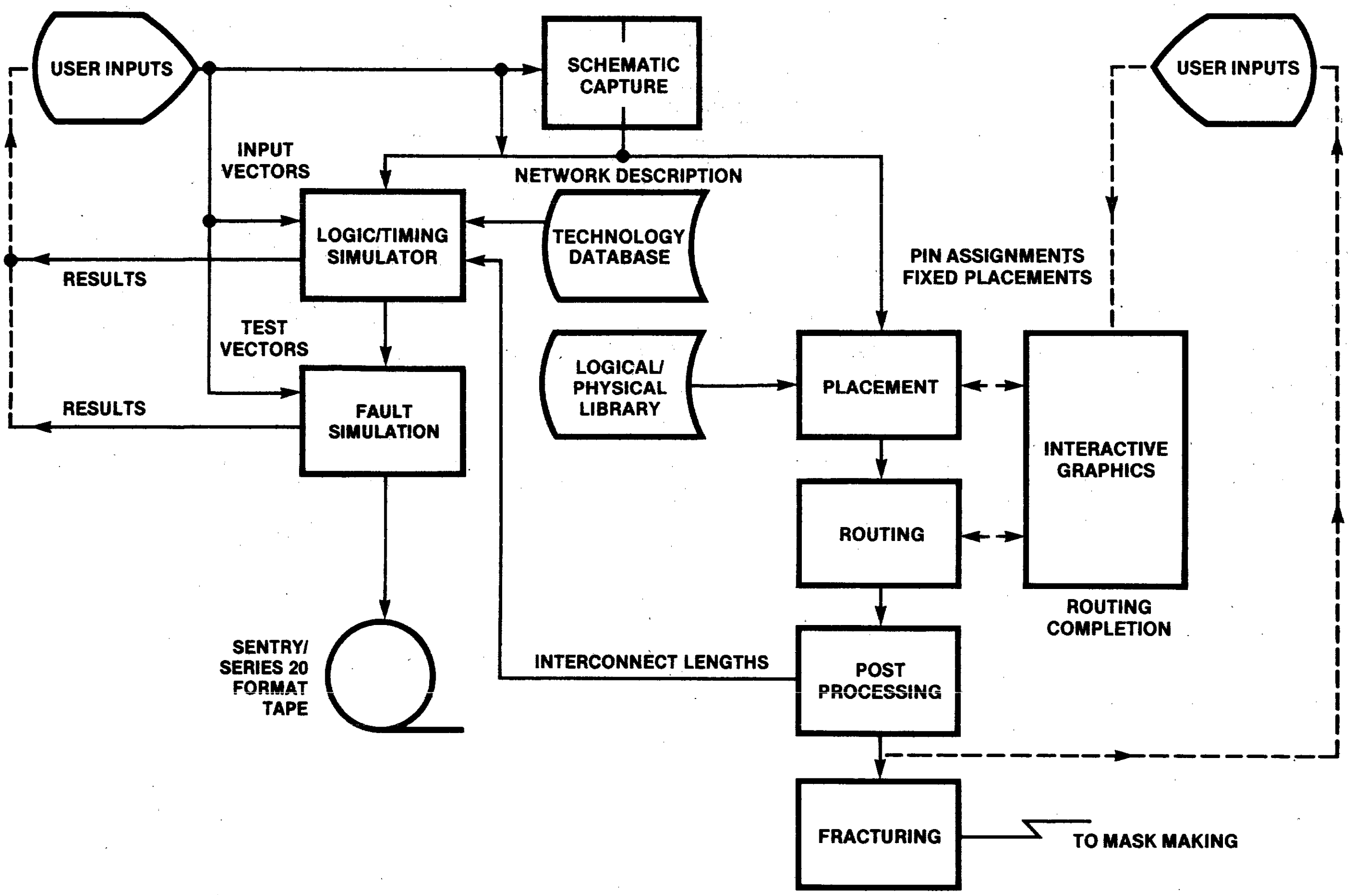
CUSTOM/SEMICUSTOM

Fairchild Camera and Instrument Corporation, Gate Array Division
1801 McCarthy Blvd. Milpitas, California 95035
(408) 942-2672 TWX 910 338 2275

FAIRCAD Computer-Aided Design System
A user friendly computer-aided design system is employed in all phases of the design cycle to assure fast turnaround times. Major functions performed by the FAIRCAD system include schematic capture, logic and timing simulation, test vector grading, automatic placement and routing and design rules checking. The user's logic description is input either interactively using a graphics workstation or entered in netlist form. Fairchild's FAIRLOGS™ simulator is used to verify array logic and timing. A fault simulator grades the effectiveness of a user-supplied test vector sequence. Placement and routing can be highly interactive processes, allowing the user to assign pins and pre-place critical path functions. Automatic routing eliminates tedious manual steps, thereby reducing routing design time from weeks to minutes. Upon routing completion, the circuit is resimulated using actual macro interconnect delays as a final verification of functionality and system performance. Design-rules checking insures that process-imposed geometry constraints are not violated.

The FAIRCAD system uses a multiple CPU configuration to insure high system availability. Remote access via telephone link is available and additional design centers are being planned worldwide. The FAIRCAD system is product and technology transparent, allowing new gate arrays and technologies to be easily integrated into the system.

FAIRCAD System



ABBREVIATIONS OF COMPANY NAMES

Action Ins	Action Instruments
AD	Analog Devices
ADT	Advanced Digital Technology
Advent	Advent Products, Inc.
Alphatron	Alphatron
AMA	American Automation
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
Amperex	Amperex Electronic Corp.
Analogic	Analogic
Analog Sys	Analog Systems
APC	Applied Micro Circuits
Apex	Apex Microtechnology
APM	Applied Microsystems Corp.
Appl Sys	Applied Systems Corp.
APT	Applied Microtechnology
Aptek	Aptek Microsystems
Array Tech	Array Technology
AWI	AWI Electronics
Barvon	Barvon Research
Bedford	Bedford Computer Systems Inc.
Burr-Brown	Burr-Brown
CAE	Computer Aided Engineering
Cal Devices	California Devices
Cermetek	Cermetek
CGRS	CGRS Microtech Inc.
Cherry	Cherry Semiconductor
CIC	Custom Integrated Circuits
CirTech	Circuit Technology
Citel	Citel
Comlinear	Comlinear Corporation
CMA	Custom MOS Arrays
Comark	Comark Corp.
Comdial	Comdial Semiconductor
Comp Auto	Computer Automation
Compas	Compas Microsystems
Cont Logic	Control Logic Inc.
Control Sys	Control Systems Microsystems Div.
CreMicro	Creative Micro Systems
Cromemco	Cromemco, Inc.
Cubit	Cubit Inc.
Curtis	Curtis Electro Devices, Inc.
Cybernetic	Cybernetic Micro Systems
Cybersys	Cybersystems
Cybertek	Cybertek Inc.
Data General	Data General
Data I/O	Data I/O
Data Trans	Data Translation
Datel	Datel
Datricon	Datricon Corporation
DDC	Data Devices Corporation
DEC	Digital Equipment Corporation
Die-Tech	Die-Tech
Digelec	Digelec Corp.
Digitek	Digitek, Inc.
Dionics	Dionics Inc.
Dist Comp	Distributed Computer Systems
Divers Tech	Diversified Technology
E-HI	E-H International, Inc.
EDI	Electronic Designs Inc.
Elind	Elind Elettronica Industriale
EMM-SESCO	EEM-SESCO
Emulogic	Emulogic Inc.
ETI Micro	ETI Micro
Exar	Exar Integrated Systems
Exel	Exel Microelectronics
Fairchild	Fairchild
Ferranti	Ferranti Electric
Force	Force Computers
Fujitsu A	Fujitsu America
Fujitsu	Fujitsu Microelectronics, Inc.
GI	General Instrument
GTE Micro	GTE Microcircuits
Harris	Harris Semiconductor
Heurikon	Heurikon Corp.
Hilevel	Hilevel Technology, Inc.
Hitachi	Hitachi America, Ltd.
Holt	Holt Inc.
HP	Hewlett-Packard
Hughes	Hughes Aircraft, Solid State Products
Hybrid Sys	Hybrid Systems
HyComp	HyComp
ICC	International Cybernetics
IDT	Integrated Device Technology
IMI	International Microcircuits, Inc.
IMP	International Microelectronic Products
IMS	Industrial MicroSystems Inc.
Infosphere	Infosphere
Inmos	Inmos
IntCirEng	Integrated Circuit Engineering
IntCirSys	Integrated Circuit Systems
IntCompSys	Integrated Computer Systems
Int Tech	Integrated Technology Corp.
Intech	Intech Microcircuits Div.
Intel	Intel
Interdesign	Interdesign
Intersil	Intersil
Intronics	Intronics
ITT	ITT Semiconductors
Kinetic Sys	Kinetic Systems
Kontron	Kontron Electronics
Lambda	Lambda Semiconductor
Linear Tech	Linear Technology
LSI Comp	LSI Computer Systems
LSI Logic	LSI Logic Corporation
Master Logic	Master Logic Corporation
Matrix	Matrix Corp.
Matrox	Matrox Electronic Systems
Maxim	Maxim Integrated Products
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MCE	MCE Electronics
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Micro Innov	Micro Innovators
Micropac	Micropac Industries
Micro Net	Micro Networks
Micro Pwr	Micro Power Systems
Micro Sci	Micro Sciences Corp.
Micro Tech	Microcircuits Technology
Micro-Link	Micro-Link Corporation
Micron	Micron Technology
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MRC	Motorola Semiconductor
Murray	MRC Systems
Monosil	Murray Consulting
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NEC	NEC Electronics
Nitron	Nitron
OAE	Oliver Advanced Engineering
Octagon	Octagon Systems Corp.
OEI	Optical Electronics Inc.
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OKI	OKI Semiconductor
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S MOS	S MOS Systems
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Western	Western Digital
Wintek	Wintek Corp.
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Xycom	Xycom
Zendex	Zendex Corp.
Zilog	Zilog
ZyMOS	ZyMOS Corporation
Zytrex	Zytrex Corp.

TTL Gate Arrays

FUJITSU

B240, B350, B600, B1100, B2000

General Information

Fujitsu Microelectronics, Inc. offers a full line of low power, high speed bipolar gate arrays. All are fabricated using low power Schottky TTL technology with TTL-compatible inputs and outputs, and use NAND-type logic. The Fujitsu bipolar gate array family has two layer metallization for gate interconnect, automatic interconnect routing for guaranteed 90 percent cell utilization and proven device reliability. They all feature over 54 predesigned, hardwired logic cells, and over 50 predesigned 74 series MSI (softwired) macros. All Fujitsu bipolar gate arrays can accept user defined macros as well. To assure the success of your design, Fujitsu's gate arrays feature DC parametric and DC functional testing as well as AC parametric testing.

The Fujitsu TTL Gate Array Family

Device Name	B240	B350	B600	B1100
Device Numbering	MB111K Series	MB112K Series	MB113K Series	MB114K Series
Technology	LSTTL	LSTTL	LSTTL	LSTTL
Internal Cells	240 3-Input NAND	360 3-input NAND	616 3-Input NAND	1120 3-Input NAND
Cell Speed	1.9ns @ 0.8mW	1.9ns @ 0.8mW	1.9ns @ 0.8mW	1.9ns @ 0.8mW
Peripheral Buffers	40 40 Input Total 32 Output	48 28 Input Total 38 Output	64 64 Input Total 51 Output	88 88 Input Total 70 Output
Packaging	14, 16, 18, 20, 22, 24, 28, 40, 42-pin DIP	22, 24, 28, 40, 42, 48, 64-pin DIP 64-pin RIT (square PGA)	24, 28, 40, 42 48, 64-pin DIP 64, 88-pin RIT (square PGA)	64, 88, 107-pin RIT (square PGA)
Interface	Logic Diagram or FLDL (Net List) and FTDL (Formatted Test Data)	Logic Diagram or FLDL (Net List) and FTDL (Formatted Test Data)	Logic Diagram or FLDL (Net List) and FTDL (Formatted Test Data)	Logic Diagram or FLDL (Net List) and FTDL (Formatted Test Data)
Macro Library	Same as B2000 description	Same as B2000 description	Same as B2000 description	Same as B2000 description
Turnaround Time	10 weeks after validation	10 weeks after validation	10 weeks after validation	10-weeks after validation
Price	Call Your FMI Sales Office	Call Your FMI Sales Office	Call Your FMI Sales Office	Call Your FMI Sales Office

The Fujitsu TTL Gate Array Family, Continued

Device Name	B2000
Device Numbering	MB17K Series
Technology	Low Power Schottky TTL
Internal Cells	2108-3 input NAND
Cell Speed	1.5 ns typical
Peripheral Buffers	112 Input, Output or I/O 72 connected outputs maximum
Packaging	135-pin RIT (square)
Interface	FLDL (Net List) and FTDL (formatted test data)
Macro Library	54 predesigned hardwired logic cells; over 50 predesigned 74 Series MSI (softwired) macros; user defined macros allowed
Turnaround Time	16 weeks after validation
Price	Call your FMI Sales Office

DC and AC Characteristics

	B240	B350
DC Specifications	$V_{IH}=2.0V$ Min. $V_{IL}=0.8V$ Max. $I_{IH}=20\mu A@2.4V$ $I_{IL}=-200\mu A@0.5V$ $V_{OH}=2.4V$ Min. $V_{OL}=0.5V$ Max. $@I_{OL}$ 10mA $I_{O5}=-15$ to $-100mA$ $I_{OZ}=\pm100\mu A$	$V_{IH}=2.0V$ Min. $V_{IL}=0.8V$ Max. $I_{IH}=20\mu A@2.4V$ $I_{IL}=-200\mu A@0.5V$ $V_{OH}=2.4V$ Min. $V_{OL}=0.5V$ Max. $@I_{OL}$ 10mA $I_{O5}=-15$ to $-100mA$ $I_{OZ}=\pm100\mu A$
AC Specifications	Input Buffer 2.9ns, 1.15mW Output Buffer 4.5ns ($C_L=15pF$) 6.5ns ($C_L=50pF$) 4.9 mW	Input Buffer 2.9ns, 1.15mW Output Buffer 4.5ns ($C_L=15pF$) 6.5ns ($C_L=50pF$) 4.9 mW

	B600	B1100	B2000
DC Specifications	$V_{IH}=2.0V$ Min. $V_{IL}=0.8V$ Max. $I_{IH}=20\mu A@2.4V$ $I_{IL}=-200\mu A@0.5V$ $V_{OL}=0.5V$ Max. $@I_{OL}$ 10mA $V_{OH}=2.4$ Min. $I_{O5}=-15$ to $-100mA$ $I_{OZ}=\pm100\mu A$	$V_{IH}=2.0V$ Min. $V_{IL}=0.8V$ Max. $I_{IH}=20\mu A@2.4V$ $I_{IL}=-200\mu A@0.5V$ $V_{OH}=2.4V$ Min. $V_{OL}=0.5V$ Max. $@I_{OL}$ 10mA $I_{O5}=-15$ to $-100mA$ $I_{OZ}=\pm100\mu A$	Input $V_{IH}=2.0V$ Min. Input $V_{IL}=0.8V$ Max. Input $I_{IH}=20\mu A$. Max. Input $I_{IL}=-200\mu A$. Max. Output $V_{OL}=0.5V$ @ 8mA Output $V_{OH}=2.4V$ @ $-2.6mA$ Output $I_{OZ}=\pm100\mu A$ Output $I_{OS}=-10$ to $-90mA$
AC Specifications	Input Buffer 2.9ns, 1.15mW Output Buffer 4.5ns ($C_L=15pF$) 6.5ns ($C_L=50pF$) 4.9 mW	Input Buffer 2.9ns, 1.15mW Output Buffer 4.5ns ($C_L=15pF$) 6.5ns ($C_L=50pF$) 4.9 mW	Input Buffer 3.5ns typ. (NAND) Output Buffer 3.5ns typ.(NAND)

CMOS Gate Arrays

FUJITSU

C440, C770, C1275 C2000, C2600, C3900, C8000

General Information

Fujitsu offers a full line of very highly integrated, low power high speed gate arrays which are fabricated with silicon gate CMOS technology. Fujitsu also guarantees 90 percent cell utilization for fully automatic placement and routing.

The Fujitsu CMOS Gate Array family offers more than 100 macro elements and contains gate arrays ranging in size from 400 basic cells to 8000 basic cells (2-input NAND equivalents).

All use Fujitsu's sophisticated computer-aided design system, which fullly automates both the design layout and fabrication. The designs are implemented on-chip by interconnecting basic cells and I/O cells using a double layer metallization process.

To assure the success of your design, Fujitsu's gate arrays feature DC parametric and DC functional testing as well as AC parametric testing.

The Fujitsu CMOS Gate Array Family, H Series

Device Name	C440H	C770H	C1275H	C2000H	C3900H
Device Numbering	MB64HK Series	MB62HK Series	MB63HK Series	MB60HK Series	MB61HK Series
Internal Cells	440-2 Input	770-2 Input	1275-2 Input	2000-2 Input	3900-2 Input
Cell Speed	4.0nS	4.0nS	4.0nS	4.0nS	4.0nS
Peripheral Buffer	54 Inputs or Outputs	74 Inputs or Outputs	80 Inputs or Outputs	68 Inputs or Outputs	68 Inputs or Outputs
Packaging	16, 18, 20, 22, 24, 28, 40, 42-pin DIP 64-pin RIT (square PGA)	24, 28, 40, 42, 48, 64-pin DIP 64-pin RIT (square PGA)	28, 40, 42, 48 64-pin DIP 64-pin RIT (square PGA)	40, 42, 48-pin DIP 64, 88-pin RIT (square PGA)	64, 68-pin RIT (square PGA)
Interface	Logic Diagrams or FLDL (Net List) and FTDL (Formatted Test Data	Logic Diagrams or FLDL (Net List) and FTDL (Formatted Test Data	Logic Diagrams or FLDL (Net List) and FTDL (Formatted Test Data	Logic Diagrams or FLDL (Net List) and FTDL (Formatted Test Data	Logic Diagrams or FLDL (Net List) and FTDL (Formatted Test Data
Turnaround Time	14-weeks after validation	14-weeks after validation	14-weeks after validation	14-weeks after validation	14-weeks after validation
Price	Call Your FMI Sales Office	Call Your FMI Sales Office	Call Your FMI Sales Office	Call Your FMI Sales Office	Call Your FMI Sales Office

The Fujitsu CMOS Gate Array Family, VH Series

Device Name	C2600VH	C3900VH	C8000VH
Device Numbering	MB60VHK Series	MB61VHK Series	MB66VHK Series
Internal Cells	2600 2-Input NAND	3900 2-Input NAND	8000 2-Input NAND
Cell Speed	2.5ns	2.5ns	2.5ns
Peripheral Buffers	106 Input/Output	127 Input/Output	160 Input/Output
Packaging	28, 40, 42, 48, 64-pin DIP 48, 64, 80-pin Flatpack 64, 88, 135-pin RIT (square PGA) 48, 64-pin LCC	40, 42, 48, 64-pin DIP 64, 88, 135-pin RIT (sqaure PGA) 48, 64-pin LCC 48, 64, 80-pin Flatpack	64, 135, 179-pin RIT (square PGA)

DC Electrical Characteristics
(All CMOS Arrays)

Parameter	Min	Typ	Max	Unit
Supply Voltage (V_{DD})	4.25	5.0	5.25	V
Input High Voltage (V_{IH})	2.0	—	—	V
Input Low Voltage (V_{IL})	V_{SS}	—	0.8	V
Input High Voltage at $I_{OH} = -0.4mA$	4.2	—	V_{DD}	V
Output Low Voltage at $I_{OH} = 20mA$	V_{SS}	—	0.4	V

Packaging, About Fujitsu Microelectronics, Inc.

Package Information

Fujitsu has a wide variety of standard device packaging available for your gate array design as shown below. If you have packaging requirements that are not on this table (Flat Pack, LCC), a Fujitsu applications engineer will be happy to discuss your needs.

Packaging Options

	B240	B350	B600	B1100	B2000	C440H	C770H	C1275H	C2000H	C3900H	C2600VH	C3900VH	C8000VH
DIP-14	■												
DIP-16	● ■					● ■							
DIP-18	● ■					● ■							
DIP-20	● ■					● ■							
DIP-22	● ■	● ■				● ■							
DIP-24	● ■	● ■	● ■			● ■	● ■						
DIP-28	● ■	● ■	● ■			● ■	● ■	● ■			■		
DIP-40	● ■	● ■	● ■			● ■	● ■	● ■	●		● ■	●	
DIP-42	● ■	● ■	● ■			■	● ■	● ■	●		● ■	●	
DIP-48		●	●				●	●	●		●	●	
DIP-64							■	■					
SDIP-64		■	■								■	■	
FPT-48											■	■	
FPT-64											■	■	
FPT-80											■	■	
RIT-64		●	●	●		●	●	●	●	●	●	●	●
RIT-88			●	●					●	●	●	●	
RIT-107*				●									
RIT-135					●						●	●	●
RIT-179													●

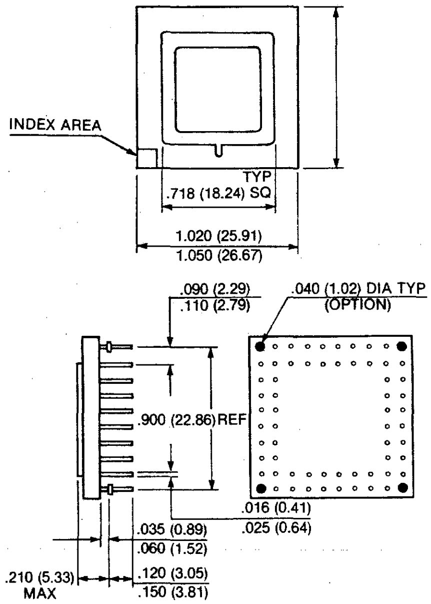
* RIT-107 is under development.

● Ceramic
■ Plastic

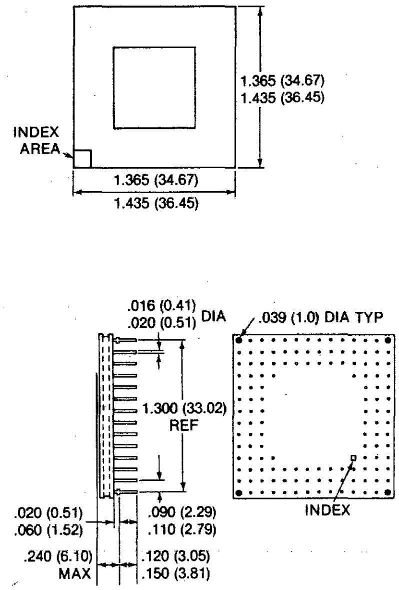
(RIT) Pin Square Package Dimensions

Dimension in inches (millimeters)

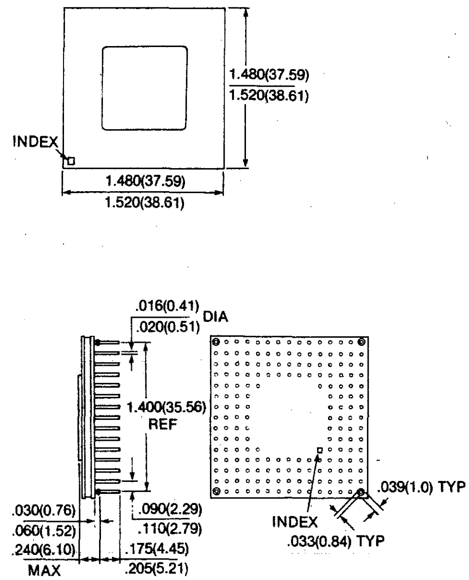
64-Pin Square Ceramic Package



135-Pin Square Ceramic Package



179-Pin Square Ceramic Package



About Fujitsu Microelectronics, Inc.

Fujitsu Microelectronics, Inc.—A U.S. Organization
Fujitsu Microelectronics, Inc. (FMI)is a U.S. subsidiary of Fujitsu Limited of Tokyo. A California Corporation, FMI is responsible for the marketing and sales of all semiconductor products in North, Central and South America.

Fujitsu Limited manufactures and markets advanced data processing and telecommunications systems, semiconductors and electronic components on a world wide scale. Fujitsu limited is ranked as Japan's number one computer manufacturer with scales in the $2 billion range.

A Leader in Large Scale Logic
Since 1974, Fujitsu Microelectronics has executed over 3,000 gate array designs. Gate arrays from Fujitsu give your designs a significant performance edge. In 1982, we introduced our CMOS device with 8,000 gates and 2.5 ns delay times. Our leadership Schottky TTL gate arrays is the first with 2,000 gates and 0.95 ns delays. Our leadership ECL arrays, with 400-picosecond delays are the fastest production arrays in the world.

Fujitsu's logic products offer leading edge technology, a complete selection of both bipolar and si-gate CMOS devices; and experience that can serve you through the coming generations of logic products.

About Fujitsu Microelectronics. Inc.
Fujitsu Microelectronics has completed a new assembly and test facility in order to better service our North American customers. The 66,000-square-foot facility is located in Kearny Mesa Industrial Park near downtown San Diego. The building was dedicated in June 1981 and is now fully operational.

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HARRIS

HS-3182

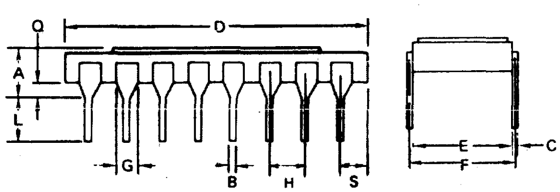
ARINC 429 Bus Interface Line Driver Circuit

Features

- INPUTS T^2L AND CMOS COMPATIBLE
- ADJUSTABLE RISE AND FALL TIMES VIA 2 EXTERNAL CAPACITORS
- PROGRAMMABLE OUTPUT DIFFERENTIAL RANGE VIA VOLTAGE REFERENCE INPUT (V_{REF})
- POWER STROBE INPUT PERMITS LOW QUIESCENT POWER OF < 20mW
- OUTPUTS ARE INHIBITED (0 VOLTS) IF DATA (A) AND DATA (B) INPUTS ARE BOTH IN THE "LOGIC ONE" STATE
- CAN OPERATE UP TO A 100 KILOBITS DATA RATE
- OUTPUT SHORT CIRCUIT PROOF AND CONTAINS OVERVOLTAGE PROTECTION
- DATA "A" AND DATA "B" SIGNALS ARE "AND'D" WITH CLOCK AND SYNC SIGNALS
- FULL MILITARY TEMPERATURE RANGE

Package

16 LEAD BRAZED DIP



LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H	DIM. L	DIM. Q	DIM. S
16	— / .200	.014 / .023	.008 / .015	— / .840	.220 / .310	.290 / .320	.030 / .070	.100 / BSC	.125 / .200	.015 / .060	— / .060

MIN. / MAX. NOTE: DIMENSIONS IN INCHES

Description

The HS-3182 ARINC 429 bus interface driver circuit is a monolithic dielectrically isolated bipolar differential line driver designed to meet the specifications of ARINC 429. This device is intended to be used with a companion chip, HS-3282 CMOS ARINC bus interface circuit, which provides the data formatting and processor interface function.

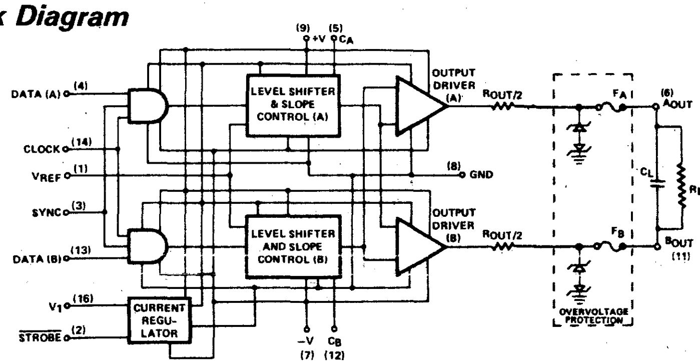
All logic inputs are T^2L and CMOS compatible. In addition to the DATA(A) and DATA(B) inputs there are also inputs for a CLOCK and SYNC signal which are AND'D with the DATA inputs. This feature was added to enhance system performance and to allow the HS-3182 to be used with devices other than the HS-3282. Also adding to system performance is the $\overline{\text{STROBE}}$ input. To minimize power consumption the $\overline{\text{STROBE}}$ input can be asserted to place the chip in the power-down mode where it draws substantially less current. Four power supplies are required: $+V = +15V \pm 10\%$, $-V = -15V \pm 10\%$, $V_1 = 5V \pm 5\%$ and V_{REF}. V_{REF} is used to program the output voltage swing, such that V_{OUT} (DIFF) $= \pm 2V_{REF}$. Typically, $V_{REF} = V_1 = 5V \pm 5\%$.

The driver output impedance is $75\Omega \pm 20\%$ at 25°C. Output rise and fall times are programmed through the use of two external capacitors, C_A and C_B. To meet the requirements for rise and fall times as specified in ARINC 429, $C_A = C_B = 75pF$ for the high speed operation (100 KBPS) and 500 pF for the low speed operation (12-14.5 KBPS). The outputs are protected against overvoltage and short circuit as shown in the Block Diagram. This device is designed to operate with a case temperature range of −55°C to +125°C.

Truth Table

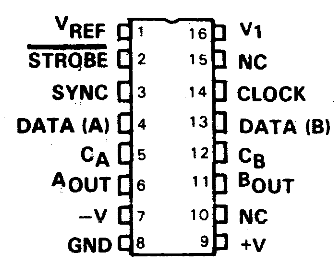
$\overline{\text{STROBE}}$	SYNC	CLOCK	DATA (A)	DATA (B)	A_{OUT}	B_{OUT}	COMMENTS
H	X	X	X	X	HI-Z	HI-Z	Power-Down State
L	X	L	X	X	OV	OV	NULL
L	L	X	X	X	OV	OV	NULL
L	H	H	L	L	OV	OV	NULL
L	H	H	L	H	$-V_{REF}$	$+V_{REF}$	LOW
L	H	H	H	L	$+V_{REF}$	$-V_{REF}$	HIGH
L	H	H	H	H	OV	OV	NULL

Block Diagram



Pinout

TOP VIEW



ABSOLUTE MAXIMUM RATINGS

Voltage Between +V and −V terminals	40V
V_1	7V
V_{REF}	6V
Logic Input Voltage	(Gnd − 0.3V) to (V_1 +0.3V)
Output Short Circuit Duration	See Note 1
Output Overvoltage Protection	See Note 3

OPERATING RANGE

Operating Voltage:	
+V	+15V ± 10%
−V	−15V ± 10%
V1	5V ± 5%
V_{REF} (for ARINC 429)	5V ± 5%
V_{REF} (applications other than ARINC)	0V to 6V
Operating Case Temperature	−55°C to +125°C
Storage Temperature	−65°C to +150°C

ELECTRICAL CHARACTERISTICS

$+V = +15V \pm 10\%$, $-V = -15V \pm 10\%$, $V_1 = V_{REF} = 5V \pm 5\%$
Case Temperature: −55°C to +125°C

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	TEST CONDITION
I_{CCPD} (+V)	Supply Current +V (Power Down)	−475	+10	475	μA	STROBE = H
I_{CCPD} (−V)	Supply Current −V (Power Down)	−475	+10	475	μA	STROBE = H
I_{CCOP} (+V)	Supply Current +V (Operating)		11	16	mA	No Load (0-100 kBps)
I_{CCOP} (−V)	Supply Current −V (Operating)		−10	−16	mA	No Load (0-100 kBps)
I_{CCOP} (V_1)	Supply Current V_1 (Operating)		600	975	μA	No Load (0-100 kBps)
I_{CCOP} (V_{REF})	Supply Current V_{REF} (Operating)	−1.0	−0.4	−0.15	mA	No Load (0-100 kBps)
V_{IH}	Logic "1" Input Voltage	2.0			V	
V_{IL}	Logic "0" Input Voltage			0.6	V	
V_{OH}	Output Voltage High (Output to ground)	V_{REF} (−250 mV)	V_{REF}	V_{REF} (+250mV)		No Load (0-100 kBps)
V_{OL}	Output Voltage Low (Output to ground)	$-V_{REF}$ (−250mV)	$-V_{REF}$	$-V_{REF}$ (+250mV)		No Load (0-100 kBps)
V_{NULL}	Output Voltage Null	−250	0	+250	mV	No Load (0-100 kBps)
I_{IL}	Input Current (Input Low)		−1	−20	μA	
I_{IH}	Input Current (Input High)		1	10	μA	
I_{OHSC}	Output Short Circuit Current (Output High)	−80	−100		mA	Short to GND
I_{OLSC}	Output Short Circuit Current (Output Low)	80	100		mA	Short to GND
C_{IN}	Input Capacitance			15	pF	
I_{SC} (+V)	Supply Current +V (Short Circuit)			150	mA	Short to GND
I_{SC} (−V)	Supply Current −V (Short Circuit)			−150	mA	Short to GND

NOTES:

① Heat sink may be required for 100KBPS @ +125°C and outout short circuit @ +125°C.
Thermal Characteristics: $T_{CASE} = T_{(Junction)} - \Theta_{(Junction - Case)} P_{(Dissipation)}$.

Where: $T_{(Junction\ Max)} = +175°C$
$\Theta_{(Junction-Case)} = 19.6°C/W$
$\Theta_{(Junction-Ambient)} = 86.5°C/W$

② Full Load for ARINC 429: $R_L = 400\Omega$ and $C_L = 30{,}000pF$ in parallel between A_{OUT} and B_{OUT}. (See Block Diagram).

③ Output Overvoltage Protection: The fuses used for output overvoltage protection may be blown by a fault at each output of greater than ±6.5V relative to GND.

POWER SPECIFICATIONS

NOMINAL POWER @25°C, +V = 15V, −V = −15V, $V_1 = V_{REF} = 5V$

DATA RATE (KBPS)	LOAD	+V	−V	V_1	CHIP POWER	POWER DISSIPATION IN LOAD
0−100	No Load	11 mA	−10 mA	600 μA	325 mW	0
12.5−14	Full Load*	24 mA	−24 mA	600 μA	660 mW	60 mW
100	Full Load*	46 mA	−46 mA	600 μA	1 watt	325 mW

*See Note (2) above.

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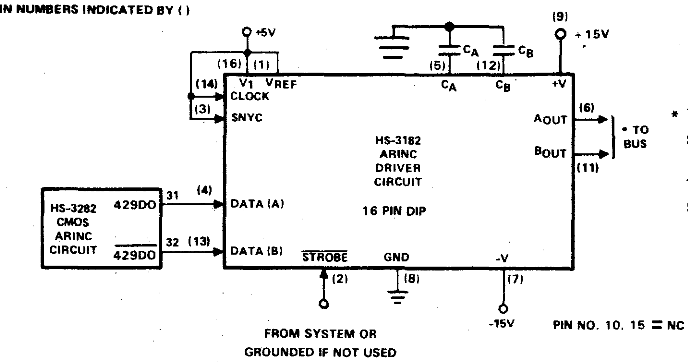
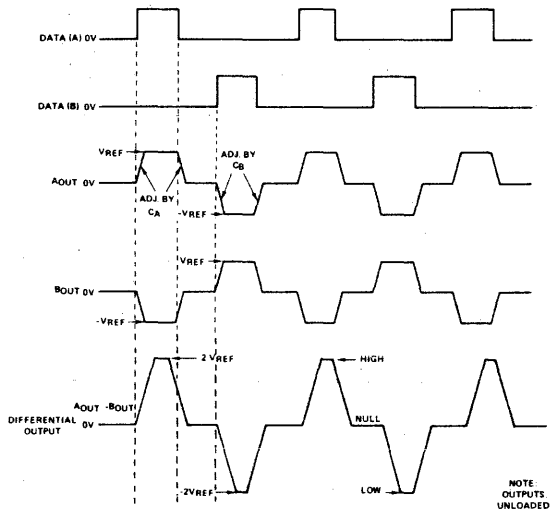
Typical Application

PIN NUMBERS INDICATED BY ( )



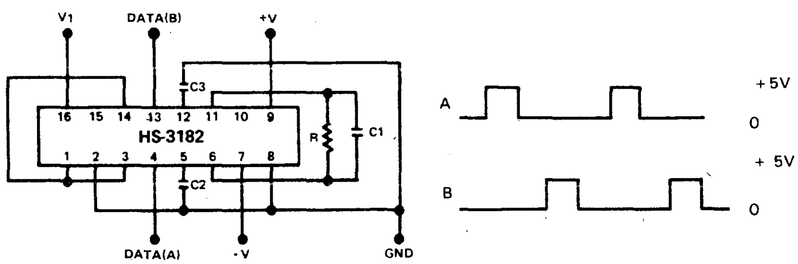
* The rise and fall time of the outputs are set to ARINC specified values by C_A and C_B. Typical $C_A = C_B$ = 75pF for high speed and 500pF for low speed operation. The output HI and low levels are set to ARINC specifications by V_{REF}.

Driver Waveforms



When the Data (A) input is in the Logic One state and the Data (B) input is in the Logic Zero state, A Out is equal to V_{REF} and B Out is equal to $-V_{REF}$ this constitutes the Output High state. Data (A) and Data (B) both in the Logic Zero state causes both A Out and B Out to be equal to 0V which designates the output Null state. Data (A) in the Logic Zero state and Data (B) in the Logic One state cause A Out to be equal to $-V_{REF}$ and B Out to be equal to V_{REF} which is the Output Low state. Both A Out and B Outputs are high impedance when the transmitter is disabled via the power strobe input.

Burn-In Schematic



R = 400Ω, ¼ watt.
C1 = 0.03μF
C2 = C3 = 500 pF, NPO.
+V = +15V ± 10%.
−V = −15V ± 10%.
V_1 = +5V ± 10%.

A 0.01 F decoupling capicitor is required on each of the three supply lines (+V, −V, and V_1) at every 3rd Burn-in socket.

Ambient Temp. Max = +125°C
Package = 16 Lead Brazed Dip
Pulse Conditions =
A & B = 6.25KHz, 25% on & 75% off duty cycle.
B is delayed one-half cycle and in sync with A.

HARRIS SEMICONDUCTOR PRODUCT FLOW
MIL-STD-883, METHOD 5004 CLASS B

100% SCREENING PROCEDURE

	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1010 Cond. C
4	Constant Acceleration	2001 Cond. E; Y1 plane
5	Seal: (A) Fine (B) Gross	1014 Cond. A or B 1014 Cond. C2
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. @ 125°C (or equivalent) (Burn-In circuits enclosed)
8	Final Electrical 100% go-no-go	Tested at Worst Case Operating Conditions
9	External Visual	2009 Sample Inspection

Note:

Traceability: All devices are assigned date code identification that provides traceability back to the inspection lot.

Branding: All devices are branded with the part number and EIA date code.

Aged Products: Product that has been held for more than 24 months will be reinspected prior to shipment to group A inspection requirements.

Additional Requirements: Sample Group A electrical tests are performed on a lot acceptance basis.

UNITED STATES

EASTERN REGION

2600 Virginia Avenue
Suite 800
Washington, DC 20037
(202) 342-3900
TWX: 710-822-9301

Five Old Concord Road
Burlington, MA 01803
(617) 273-1020
TWX: 710-332-1074

106 Seventh Street
Garden City, NY 11530
(516) 747-6776

WESTERN REGION

1503 South Coast Drive
Suite 320
Costa Mesa, CA 92626
(714) 957-6557
TWX: 910-595-1533

625 Ellis, Suite 300
Mt. View, CA 94043
(415) 964-6443
TWX: 910-379-6431

MIDWEST REGION

2850 Metro Dr., Suite 703
Minneapolis, MN 55420
(612) 854-3224
TWX: 910-576-3418

HOME OFFICE

P.O. Box 883
Melbourne, FL 32901
(305) 724-7045
TWX: 510-959-6259

EUROPEAN

Harris Systems Ltd.
Semiconductor Programs Division
P.O. Box 27
145 Farnham Road
Slough SL1 4XD
United Kingdom
Tel: 34666
TWX: 848174

HARRIS

CUSTOM INTEGRATED CIRCUITS DIVISION

HARRIS

HS-3282

CMOS ARINC Bus Interface Circuit

Description

The Harris HS-3282 is a high performance CMOS bus interface circuit that is intended to meet the requirements of ARINC Specification 429, and similar encoded, time multiplexed serial data protocols. The ARINC 429 bus interface circuit consists of two (2) receivers and a transmitter operating independently as shown in Figure 1. The two receivers operate at a frequency that is ten (10) times the receiver data rate, which can be the same or different from the transmitter data rate. Although the two receivers operate at the same frequency, they are functionally independent and each receives serial data asynchronously. The transmitter section of the ARINC bus interface circuit consists mainly of a First-In First-Out (FIFO) memory and timing circuit. The FIFO memory is used to hold eight (8) ARINC data words for transmission serially. The timing circuit is used to correctly separate each ARINC word as required by ARINC Specification 429.

Even though ARINC Specification 429 specifies a 32-bit word, including parity, the HS-3282 can be programmed to also operate with a word length of 25 bits. The incoming receiver data word parity is checked, and a parity status is stored in the receiver latch and is outputted on Pin BD08 during the 1st word. [A logic "0" indicates that an odd number of logic "1"s were received and stored; a logic "1" indicates that an even number of logic "1"s were received and stored]. In the transmitter the parity generator will generate either odd or even parity depending upon the status of PARCK control signal. A logic "0" on BD12 will cause odd parity to be generated and inputted to the output data stream. Conversely, a logic "1" on BD12 will result in the generation of even parity that will be inputted to the output data stream.

More versatility is provided in both the transmitter and receiver by the addition of an external TTL clock input allowing the bus interface circuit to operate at data rates from 0 to 0.1 megabits. The TTL external clock must be ten (10) times the data rate to insure no data ambiguity.

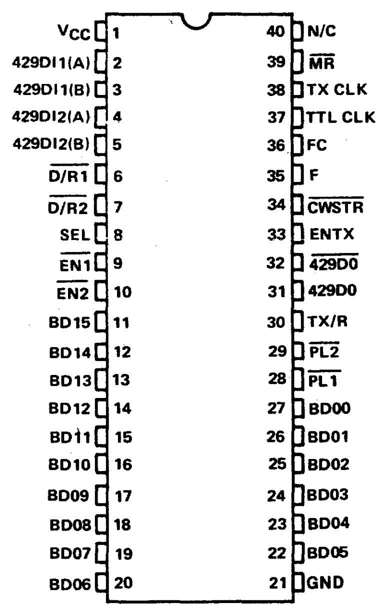
The ARINC bus interface circuit is fully guaranteed to support the data rates of ARINC specification 429 over both the voltage (± 5%) and full military temperature range. It interfaces with TTL, CMOS or NMOS support circuitry, and uses the standard 5-volt V_{CC} supply.

Features

- ARINC SPECIFICATION 429 COMPATIBLE
- DATA RATES OF 100 KILOBITS OR 12.5 KILOBITS
- SEPARATE RECEIVER AND TRANSMITTER SECTION
- DUAL AND INDEPENDENT RECEIVERS, CONNECTING DIRECTLY TO ARINC BUS
- SERIAL TO PARALLEL RECEIVER DATA CONVERSION
- PARALLEL TO SERIAL TRANSMITTER DATA CONVERSION
- WORD LENGTHS OF 25 OR 32 BITS
- PARITY STATUS OF RECEIVED DATA
- GENERATE PARITY OF TRANSMITTER DATA
- AUTOMATIC WORD GAP TIMER
- SINGLE 5-VOLT SUPPLY
- LOW POWER DISSIPATION
- FULL MILITARY TEMPERATURE RANGE

Pinout

TOP VIEW



ABSOLUTE MAXIMUM RATINGS

Voltage at any Pin (Except 2, 3, 4, & 5)	$-0.3V$ to V_{CC} $+0.3V$
Voltage at Pins 2, 3, 4, & 5	$-29V$ to $+29V$
Maximum V_{CC}	7.0V
Operating Temperature Range	−55°C to +125°C
Storage Temperature	−65°C to +150°C

CAUTION: To prevent permanent damage to this device, care should be exercised to insure that the absolute maximum ratings for supply voltages, temperature and voltage or current at any pin is not exceeded during both static and dynamic operation.

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ± 5% TA = Operating Temperature Range

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
	ARINC INPUTS					
V_{IH}	Logic "1" Input Voltage	6.7	10	13	V	Pin 2-3, 4-5
V_{IL}	Logic "0" Input Voltage	−6.7	−10	−13	V	Pin 2-3, 4-5
V_{IN}	Null Input Voltage	−2.5	0	+2.5	V	
V_{CH}	Common Mode V			±5	V	
I_{IH}	Input Leakage	75	135	200	μA	$V_{IN} = V_{CC}$
I_{IL}	Input Leakage	−200	−325	−450	μA	$V_{IN} = 0$
R_I	Differential Input Impedance	6			KΩ	
R_H	Input Impedance to V_{CC}	12			KΩ	
R_G	Input Impedance to GND	12			KΩ	
C_I	Differential Input Capacitance*			20	pF	
C_H	Input Capacitance to V_{CC}*			20	pF	
C_G	Input Capacitance to GND*			20	pF	
	BI-DIR. INPUTS					
V_{IH}	Logic "1" Input Voltage	2.1			V	
V_{IL}	Logic "0" Input Voltage			0.7	V	
I_I	Input Leakage	−1.5		−1.5	μA	$0<V_{IN}<V_{CC}$
	ALL OTHER INPUTS					
V_{IH}	Logic "1" Input Voltage	3.5			V	
V_{IL}	Logic "0" Input Voltage			0.7	V	
I_{IH}	Input Leakage (Except Pin 36)			10	μA	$V_{IN} = V_{CC}$
	Input Leakage (Pin 36)			50	μA	$V_{IN} = V_{CC}$
I_{IL}	Input Leakage			−10	μA	$V_{IN} = 0$
C_I	Input Capacitance*			15	pF	
	OUTPUTS (Including Bi-directional Outputs)					
V_{OH}	Logic "1" Output	2.7			V	$I_{OH} = -1.5mA$
V_{OL}	Logic "O" Output			0.4	V	$I_{OL} = 1.8mA$
C_O	Output Capacitance*			15	pF	
I_{CC_1}	Supply Current Stand-by			20.0	mA	$V_{CC} = 5.5$, $V_{IN} = 0$
I_{CC_2}	Supply Current Operation			20.0	mA	

*Guaranteed but not tested.

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ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	DATA RATE = 100 KBFS MIN	DATA RATE = 100 KBFS MAX	DATA RATE = 12.5 KBFS MIN	DATA RATE = 12.5 KBFS MAX	UNITS	TEST CONDITIONS
F_C[1]	Clock Frequency		1		1	MHz	≈50% Duty Cycle
F_D	Data Rate		100		12.5	KHz	
T_{LHC}	TTL Clock Rise Time		10		10	ns	
T_{HLC}	TTL Clock Fall Time		10		10	ns	
T_{MR}	Master Reset Pulse Width	200		200		ns	
	RECEIVER TIMING						
$T_{D/R}$[2]	Receiver Device Ready Time From 32nd Data Bit		16		128	μs	
$T_{D/REN}$	Device Ready to Enable Time	0		0		ns	
T_{EN}	Data Enable Pulse Width	200		200		ns	
T_{ENEN}	Data Enable to Data Enable Time	50		50		ns	
$T_{END/R}$	Data Enable to Device Ready Reset Time		200		200	ns	
T_{ENDATA}	Output Data Valid to Enable Time		200		200	ns	
T_{ENSEL}	Data Enable to Data Select Time	20		20		ns	
T_{SELEN}	Data Select to Data Enable Time	20		20		ns	
T_{DATAEN}	Output Data Disable Time		30		30	ns	
	CONTROL WORD TIMING						
T_{CWSTR}	Control Word Register Strobe Pulse Width	130		130		ns	
T_{CWSET}	Control Word Setup Time	130		130		ns	
T_{CWHLD}	Control Word Hold Time	0		0		ns	
	TRANSMITTER FIFO WRITE TIMING						
T_{PL}	Parallel Load Pulse Width	200		200		ns	
T_{PL12}	Parallel Load 1 to Parallel Load 2 Delay	0		0		ns	
$T_{TX/R}$	Transmitter Ready Delay Time		840		840	ns	
T_{DWSET}	Data Word Setup Time	110		110		ns	
T_{DWHLD}	Data Word Hold Time	0		0		ns	
	TRANSMITTER OUTPUT TIMING						
T_{ENDAT}	Enable Transmit to Output Data Valid Time		25		200	μs	
T_{BIT}	Output Data BIT Time	4.95	5.05	39.6	40.4	μs	
T_{NUL}	Output Data Nul Time	4.95	5.05	39.6	40.4	μs	
$T_{DTX/R}$	Data Transmission Word to TX/R Set Time		50		50	ns	
$T_{ENTX/R}$	Enable Transmit Turn Off Time	0		0		ns	
T_{GAP}	Data Word Gap Time	39.6	40.4	316.8	323.2	μs	
	REPEATER OPERATION TIMING						
T_{ENPL}	Data Enable to Parallel Load Delay Time	0		0		ns	
T_{PLEN}	Data Enable Hold For Parallel Load Time	0		0		ns	
$T_{TX/REN}$	Enable Transmit Delay Time	0		0		ns	

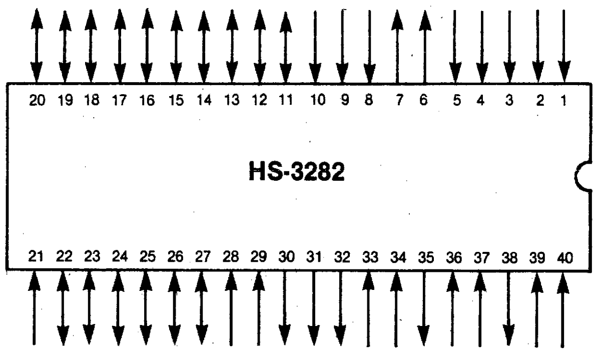
1. 60-40 Duty Cycle Acceptable 2. Same Delay For 25 bit Word Format

Pin Assignments

PIN	SYMBOL	SECTION	DESCRIPTION
1	V_{CC}	Receiver/ Transmitter	Supply pin. 5 volts ± 5%.
2	429 DI1 (A)	Receiver	ARINC 429 data input to Receiver 1.
3	429 DI1 (B)	Receiver	ARINC 429 data input to Receiver 1.
4	429 DI2 (A)	Receiver	ARINC 429 data input to Receiver 2.
5	429 DI2 (B)	Receiver	ARINC 429 data input to Receiver 2.
6	$\overline{D/R1}$	Receiver	Device ready flag output from Receiver 1 indicating a valid data word is ready to be fetched.
7	$\overline{D/R2}$	Receiver	Device ready flag output from Receiver 2 indicating a valid data word is ready to be fetched.
8	SEL	Receiver	Bus Data Selector - input signal to select one of two 16-bit words from either Receiver 1 or 2.
9	$\overline{EN1}$	Receiver	Input signal to enable data from Receiver 1 onto the data bus.
10	$\overline{EN2}$	Receiver	Input signal to enable data from Receiver 2 onto the data bus.
11	BD15	Receiver/ Transmitter	Bi-directional data bus for fetching data from either of the Receivers, or for loading data into the Transmitter memory or control word register. See Control Word Table for description of Control Word bits.
12	BD14	Receiver/ Transmitter	See pin 11.

PIN	SYMBOL	SECTION	DESCRIPTION
13	BD13	Receiver/ Transmitter	See pin 11.
14	BD12	Receiver/ Transmitter	See pin 11.
15	BD11	Receiver/ Transmitter	See pin 11.
16	BD10	Receiver/ Transmitter	See pin 11.
17	BD09	Receiver/ Transmitter	See pin 11.
18	BD08	Receiver/ Transmitter	See pin 11.
19	BD07	Receiver/ Transmitter	See pin 11.
20	BD06	Receiver/ Transmitter	See pin 11.
21	GND	Receiver/ Transmitter	Circuit ground.
22	BD05	Receiver/ Transmitter	See pin 11.
23	BD04	Receiver/ Transmitter	See pin 11. Control Word function not applicable.
24	BD03	Receiver/ Transmitter	See pin 11. Control Word function not applicable.
25	BD02	Receiver/ Transmitter	See pin 11. Control Word function not applicable.
26	BD01	Receiver/ Transmitter	See pin 11. Control Word function not applicable.
27	BD00	Receiver/ Transmitter	See pin 11. Control Word function not applicable.
28	$\overline{PL1}$	Transmitter	Parallel load input signal loading the first 16-Bit word into the Transmitter memory.

Pinout



PIN	SYMBOL	SECTION	DESCRIPTION
29	$\overline{PL2}$	Transmitter	Parallel load input signal loading the second 16-Bit word into the Transmitter memory and initiates data transfer into the memory stack.
30	TX/R	Transmitter	Transmitter flag output to indicate the memory is empty.
31	429D0	Transmitter	Data output from Transmitter.
32	$\overline{429D0}$	Transmitter	Data output from Transmitter.
33	ENTX	Transmitter	Transmitter Enable Input signal to initiate data transmission from FIFO memory.
34	$\overline{CWSTR}$	Receiver/ Transmitter	Control word input strobe signal to latch the control word from the data bus into the control word register.
35	NC	Receiver/ Transmitter	This pin should be left open.

PIN	SYMBOL	SECTION	DESCRIPTION
36	NC	Receiver/ Transmitter	No connect. This pin may be left open or tied low but never tied high.
37	TTLCLK	Receiver/ Transmitter	External clock input. May be either ten (10) or eighty (80) times the data rate. If using both ARINC data rates it must be ten (10) times the highest data rate. (Typically 1 MHz). If using crystal oscillator, this pin may be left open or tied high but never tied low.
38	TXCLK	Transmitter	Transmitter Clock output. Delivers a clock frequency equal to the transmitter data rate.
39	$\overline{MR}$	Receiver/ Transmitter	Master Reset. Active low pulse used to reset FIFO, bit counters, gap timmer, word count signal, TX/R and various other flags and controls. Usually only used on Power-Up or System Reset.
40	—	—	No connection.

The HS-3282 is designed to support ARINC Specification 429 and other serial data protocols that use a similar format by collecting the receiving, transmitting, synchronizing, timing and parity functions on a single, low power LSI circuit. It goes beyond the ARINC requirements of providing for either odd or even parity, and giving the user a choice of either 25 or 32 bit word lengths. The receiver and transmitter sections operate independently of each other. The serial-to-parallel conversion required of the receiver and the parallel-to-serial conversion requirements of the transmitter have been incorporated into the bus interface circuit.

Provisions have been made through the addition of an external TTL clock input to provide data rate flexibility. This requires an external TTL clock that is 10 times the data rate.

To obtain the flexibility discussed above, a number of external control signals are required. To reduce the pin count requirements, an internal control word register is used. The control word is latched from the data bus into the register by the Control Word Strobe (CWSTR) signal going to a logic "0". Eleven (11) control functions are used, and along with the bus data (BD) line are listed below:

CONTROL WORD

PIN NAME	SYMBOL	FUNCTION
BD05	SLFTST	Connects the self test signal from the transmitter directly to the receiver shift registers, bypassing the input receivers. Receiver 1 receives Data true and Receiver 2 receives Data not. Note that the transmitter output remains active. (Logic "0" on SLFTST Enables Self Test).
BD06	SDENB1	Signal to activate the Source Destination (SD) Decoder for Receiver 1. (Logic "1" activates SD Decoder).
BD07	X1	If SDENB1 = "1" then this bit is compared with ARINC Data Bit #9. If Y1 also matches (see Y1), the word will be accepted by the Receiver 1. If SDENB1 = "0" this bit becomes a don't care.
BD08	Y1	If SDENB1 = "1" then this bit is compared with ARINC Data Bit #10. If X1 also matches (see X1), the word will be accepted by the Receiver 1. If SDENB1 = "0" this bit becomes a don't care.
BD09	SDENB2	Signal to activate the Source Destination (SD) Decoder for Receiver 2. (Logic "1" activates SD Decoder).
BD10	X2	If SDENB2 = "1" then this bit is compared with ARINC Data Bit #9. If Y2 also matches (see Y2), the word will be accepted by the Receiver 2. If SDENB2 = "0" this bit becomes a don't care.
BD11	Y2	If SDENB2 = "1" then this bit is compared with ARINC Data Bit #10. If X2 also matches (see X2), the word will be accepted by the Receiver 2. If SDENB2 = "0" this bit becomes a don't care.
BD12	PARCK	Signal used to invert the transmitter parity bit for test of parity circuits. Logic "0" selects normal odd parity. Logic "1" selects even parity.
BD13	TXSEL	Selects high or low Transmitter data rate. If TXSEL = "0" then transmitter data rate is equal to the clock rate divided by ten (10). If TXSEL = "1" then transmitter data rate is equal to the clock rate divided by eighty (80).
BD14	RCVSEL	Selects high or low Receiver data rate. If RCVSEL = "0" then the received date rate should be equal to the clock rate divided by ten (10). If RCVSEL = "1" then the received data rate should be equal to the clock rate divided by eighty (80).
BD15	WLSEL	Selects word length. If WLSEL = "0" a 32-bit word format will be selected. If WLSEL = "1" a 25-bit word format will be selected.

ARINC 429 DATA FORMAT as input to the Receiver and output from the Transmitter is as follows:

TABLE 1 - ARINC 429 DATA FORMAT

ARINC BIT #	FUNCTIONS
1 - 8	Label
9 - 10	SDI or Data
11	LSB
12 - 27	Data
28	MSB
29	Sign
30, 31	SSM
32	Parity

This format is shuffled when seen on the sixteen bi-directional input/outputs. The format shown below is used from the receivers and input to the transmitter:

TABLE 2 - WORD 1 FORMAT

BIDIRECTIONAL BIT #	FUNCTION	ARINC BIT #
15, 14		13, 12
13	LSB	11
12, 11	SDI or Data	10, 9
10, 9	SSM Status	31, 30
8	Parity	32
7 - 00	Label	1 - 8

TABLE 3 - WORD 2 FORMAT

BIDIRECTIONAL BIT #	FUNCTION	ARINC BIT #
15	Sign	29
14	MSB	28
13 - 00	Data	27 - 14

If the receiver input data word string is broken before the entire data word is received, the receiver will reset and ignore the partially received data word.

If the transmitter is used to transmit consecutive data words, each word will be separated by a four (4) bit "null" state (both positive and negative outputs will maintain a zero (0) volt level).

RECEIVER OPERATION

Since the two receivers are functionally identical, only one will be discussed in detail, and the block diagram will be used for reference in this discussion. The receiver consists of the following circuits:

- The Line Receiver functions as a voltage level translator. It transforms the 10 volt differential line voltage, ARINC 429 format, into 5 volt internal logic level.
- The output of the Line Receiver is one of two inputs to the Self-Test Data Selector (SEL). The other input to the Data Selector is the Self-Test Signal from the Transmitter section.
- The incoming data, either Self-Test or ARINC 429, is double sampled by the Word Gap Timer to generate a Data Clock. The Receiver sample frequency (RCVCLK), 1 MHz, or 125 KHz, is generated by the Receiver/Transmitter Timing Circuit. This sampling frequency is ten times the Data Rate to ensure no data ambiguity.
- The derived data clock then shifts the data down a 32-bit long Data Shift Register (Data S/R1). The Data Word Length is selectable for either 25-Bits or 32-Bits long by the Control Signal (WLSEL). As soon as the data word is completely received, an internal signal (WDCNT1) is generated by the Word Gap Timer Circuit.
- The Source/Destination (S/D) Decoder compares the user set code (X and Y) with Bits 9 and 10 of the Data Word. If the two codes are matched, a positive signal is generated to enable the WDCNT1 signal to latch in the received data. Otherwise, the data word is ignored and no latching action takes place. The S/D Decoder can be Enabled and Disabled by the control signal S/D ENB. If the data word is latched, an indicator flag ($\overline{\text{D/R1}}$) is set. This indicates a valid data word is ready to be fetched by the user.
- The parity of the incoming word is checked and the status (i.e., logic "0" for odd parity and logic "1" for even parity) stored in the receiver latch and outputted on BD08 during the Word No. 1.
- Assuming the user desires to access the data, he first sets the Data Select Line (SEL) to a Logic "0" level and pulses the Enable ($\overline{\text{EN1}}$) line. This action causes the Data Selector (SEL1) to select the first-data word, which contains the label field and Enable it onto the Data Bus. To obtain the second data word, the user sets the SEL line to a Logic "1" level and pulse the Enable ($\overline{\text{EN1}}$) line again. The Enable pulse duration is matched to the user circuit requirement needed to latch in the Data Word from the Data Bus. The second Enable pulse is also used to reset the Device Ready ($\overline{\text{D/R1}}$) flip-flop. This completes a receiving cycle.

TRANSMITTER OPERATION

The Transmitter section consists of an 8-word deep by 31-Bit long FIFO Memory, Parity Generator, Transmitter Word Gap Timing Circuit and Driver Circuit.

- The FIFO Memory is organized in such a way that data loaded in the input register is automatically transferred to the output register for Serial Data Transmission. This eliminates a large amount of data managing time since the data need not be clocked from the input register to the output register. The FIFO input register is made up of two sets of 16 D-type flip-flops, which are clocked by the two parallel load signals ($\overline{\text{PL1}}$ and $\overline{\text{PL2}}$). The data from the Data Bus is clocked into the D-type flip-flop on the positive going edge of the $\overline{\text{PL}}$ signals. If the FIFO memory is initially empty, or the stack is not full, the data will be automatically transferred down the Memory Stack and into the output register or to the last empty FIFO storage register. If the

Transmitter Enable signal (ENTX) is not active, a Logic "0", the data remains at the output register. The FIFO Memory has storage locations to hold eight 31-Bit words. If the memory is full and new data is again strobed with $\overline{PL}$, the old data at the input register is written over by the new data. Data will remain in the Memory until ENTX goes to a Logic "1". This activates the FIFO Clock and data is shifted out serially to the Transmitter Driver.

- The Output Register of the FIFO is designed such that it can shift out a word of 25-Bits long or 32-Bits long. This word length is again controlled by the WLSEL bit. The TX Word Gap Timer Circuit also automatically inserts a gap equivalent to 4-Bit Times between each word. This gives a minimum requirement of 29-Bit time or 36-Bit time for each word transmission. Assuming the signal, ENTX, remains at a Logic "1", a transfer to stack signal is generated to transfer the data down the Memory Stack one position. This action is continued until the last word is shifted out of the FIFO memory. At this time a Transmitter Ready (TX/R) flag is generated to signal the user that the Transmitter is ready to receive eight more data words.
- A Bit Counter is used to detect the last Bit shifted out of the FIFO memory and replaces it with the Parity Bit generated by the Parity Generator. The Parity Generator has a control signal, Parity Check (PARCK), which establishes whether odd or even parity is inserted into the output data word. PARCK set to a logic "0" will result in odd parity and when set to a logic "1" will result in even parity.

SAMPLE INTERFACE TECHNIQUE

From Figure 1, one can see that the Data Bus is time shared between the Receiver and the Transmitter. Therefore, bus controlling must be synchronously shared between the Receiver and the Transmitter. Figure 2 shows the typical interface timing control of the ARINC Chip for Receiving function and for Transmitting function. Timing sequence for loading the Transmitter FIFO Memory is shown in Timing Interval A. A Transmitter Ready (TX/R) Flag signals the user that the Transmitter Memory is empty. The user then Enables the Transmitter Data, a 16-Bit word, on the Data Bus and strobes the Transmitter with a Parallel Load ($\overline{PL1}$) Signal. The second part of the 32-Bit word is similarly loaded into the Transmitter with $\overline{PL2}$, which also initiates data transfer to stack. This is continuous until the Memory is full, which is eight 31-Bit words. The user must keep track of the number of words loaded into the Memory to ensure no data is written over by other data. During the time the user is loading the Transmitter, he does not have to service the Receiver, even if the Receiver flags the user with the signal $\overline{D/R1}$ that a valid received word is ready to be fetched. This is shown by the Timing Interval B. If the user decides to obtain the received data before the Transmitter is completely loaded, he sets the two parallel load signals ($\overline{PL1}$ and $\overline{PL2}$) at a Logic "1" state, and strobe $\overline{EN1}$ while the signal SEL is at a Logic "0" state. After the negative edge of $\overline{EN1}$, the first 16-Bit segment of the received word becomes valid on the Data Bus. At the positive edge of $\overline{EN1}$, the user should toggle the signal SEL to ready the Receiver for the second 16-Bit word. Strobing the Receiver with $\overline{EN1}$, the second time, enables the second 16-Bit word and resets the Receiver Ready Flag $\overline{D/R1}$. The user should now reset the signal SEL to a Logic "0" state to ready the Receiver for another Read Cycle. During the time period that the user is fetching the received words, he can load the transmitter. This is done by interlacing the $\overline{PL}$ signals with the $\overline{EN}$ signals as shown in the Timing Interval B. Servicing the Receiver 2 is similar and is illustrated by Timing Interval C. Timing Interval D shows the rest of the Transmitter loading sequence and the beginning of the transmission by switching the signal TX Enable to a Logic "1" state. Timing Interval E is the time it takes to transmit all data from the FIFO Memory, either 288 Bit times or 232 Bit times.

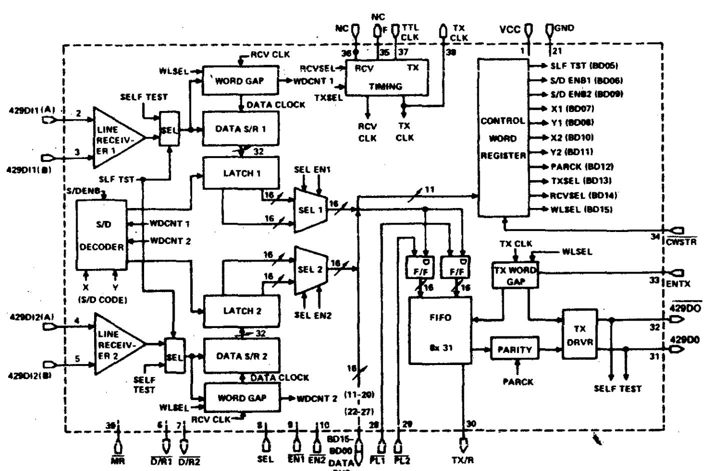


FIGURE 1. SINGLE CHIP ARINC 429 INTERFACE FUNCTIONAL BLOCK DIAGRAM.

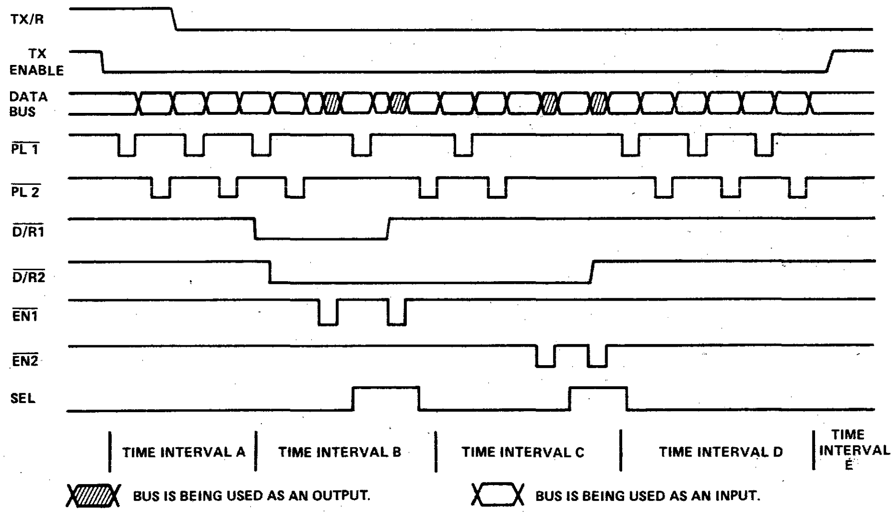


FIGURE 2. TYPICAL INTERFACE TIMING SEQUENCE

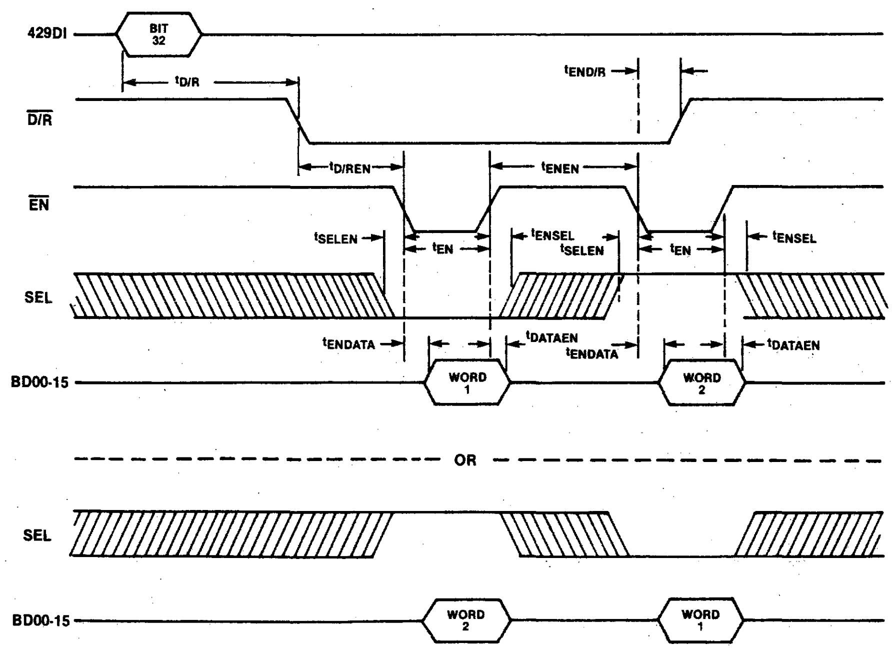


FIGURE 3 RECEIVER TIMING

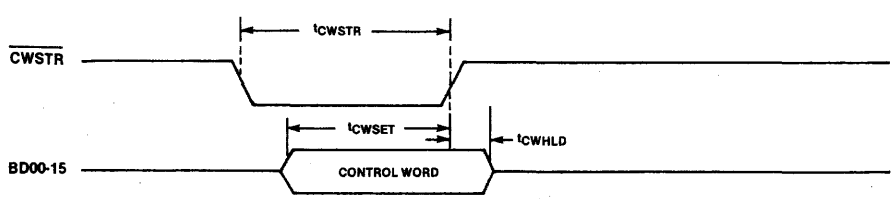


FIGURE 4 CONTROL WORD TIMING

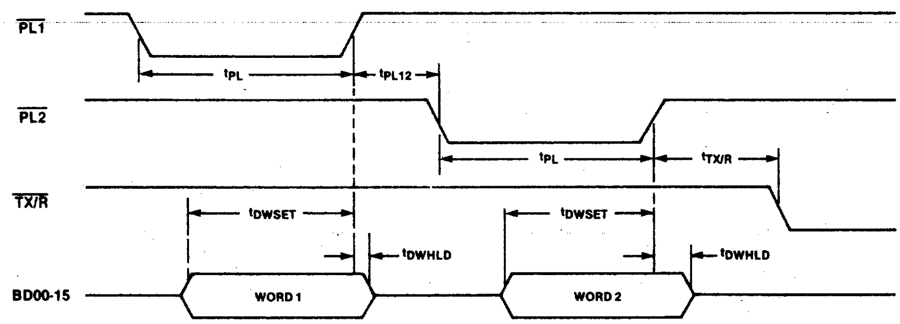


FIGURE 5 TRANSMITTER FIFO WRITE TIMING

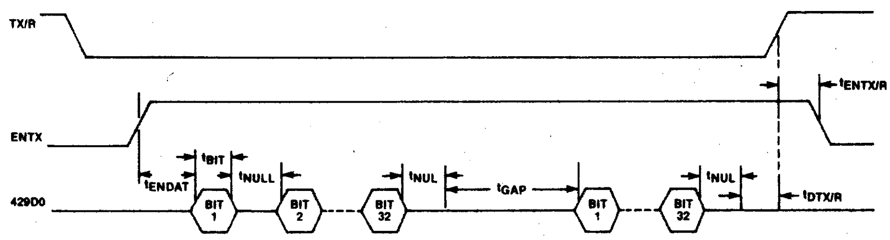


FIGURE 6 TRANSMITTER OUTPUT TIMING

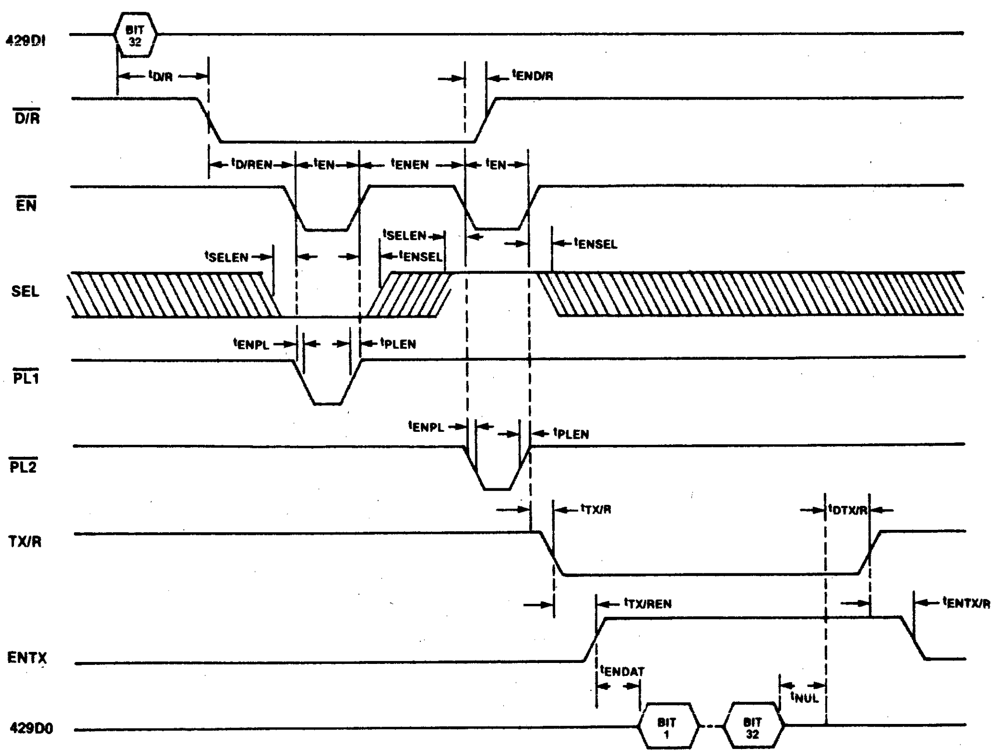
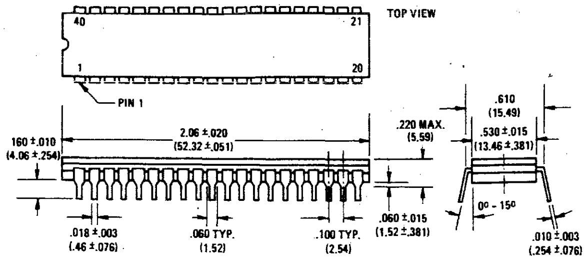


FIGURE 7 REPEATER OPERATION TIMING

Packaging

40-PIN CER-DIP



Ordering Information

HS 1-3282-8

- HS — HARRIS CUSTOM INTERGRATED CIRCUITS DIVISION
- 1 — PACKAGE CODE
  - 1: Ceramic
- 3282 — DEVICE NUMBER
- 8 — TEMPERATURE:
  - 8: Mil. Std. 883B
  - 5: 0°C to +70°C

1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ±.010 (±0.25mm) unless otherwise shown.

Test Product Flow

HARRIS SEMICONDUCTOR PRODUCT FLOW
MIL-STD-883, METHOD 5004 CLASS B
100% SCREENING PROCEDURE

	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1010 Cond. C
4	Constant Acceleration	2001 Cond. E; Y1 plane
5	Seal: A Fine B Gross	1014 Cond. A or B 1014 Cond. C2
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. @ 125°C (or equivalent) (Burn-In circuits enclosed)
8	Final Electrical 100% go-no-go	Tested at Worst Case Operating Conditions
9	External Visual	2009 Sample Inspection

Notes:
- Traceability. All devices are assigned date code identification that provides traceability back to the inspection lot.
- Branding. All devices are branded with the part number and EIA date code.
- Aged Products: Product that has been held for more than 24 months will be reinspected prior to shipment to group A inspection requirements.
- Additional Requirements: Sample Group A electrical tests are performed on a lot acceptance basis.

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P.O. Box 883
Melbourne, FL 32901
(305) 724-7045
TWX: 510-959-6259

EUROPEAN

Harris Systems Ltd.
Semiconductor Programs Division
P.O. Box 27
145 Farnham Road
Slough SL1 4XD
United Kingdom
Tel: 34666
TWX: 848174

HARRIS

CUSTOM INTEGRATED CIRCUITS DIVISION

HARRIS

HS-3819

Preliminary

Video Character Generator

Features

- OPERATION (DOT CLOCK) FROM 1.0 TO 27 MHz
- DESIGNED TO INTERFACE WITH INTEL 8275 PROGRAMMABLE CRT CONTROLLER
- DIRECTLY DECODES (FROM ON-CHIP ROM);
  - ASCII 96 CHARACTER SET
  - 32 PSEUDO-GRAPHIC CHARACTERS
  - 10 OVERLAY PATTERNS
- EXPANDABLE CHARACTER TABLE
- 9 X 12 DOT MATRIX WITH DESCENDER CAPABILITY
- HANDLES VIDEO MODIFIERS;
  - BLANK
  - VIDEO SUPPRESS
  - REVERSE VIDEO
  - LIGHT ENABLE

Description

The HS-3819 is a CMOS/LSI Video Character Generator designed to help interface an Intel 8275 Programmable CRT Controller to a video monitor. The character generator must be supplied with a clock frequency of between 1 and 27 MHz which will be used as the dot clock. This signal is then divided by nine to form the character clock output needed by the CRT Controller. The HS-3819 then converts character data into a video output signal, through use of an internal (ROM) character table. Stored in this ROM are the standard 96 ASCII characters, 32 pseudo-graphic characters and 10 overlay patterns used to modify characters. Additional characters, if needed, can easily be decoded from an external memory field.

Pinout

Signal	Pin	Pin	Signal
$\overline{WR}$	1	40	V_{CC}
$\overline{CS}$	2	39	$\overline{GRAPHE}$
A0	3	38	$\overline{E8}$
S1	4	37	$\overline{E7}$
S2	5	36	$\overline{E6}$
S3	6	35	$\overline{E5}$
LC3	7	34	$\overline{E4}$
LC2	8	33	$\overline{E3}$
LC1	9	32	$\overline{E2}$
LC0	10	31	$\overline{E1}$
EXEN	11	30	$\overline{E0}$
ROMDIS	12	29	DOTCLK
CC6	13	28	$\overline{RESET}$
CC5	14	27	CCLK
CC4	15	26	VSP
CC3	16	25	LTEN
CC2	17	24	RVV
CC1	18	23	$\overline{BLK}$
CC0	19	22	VID2
GND	20	21	VID1

LC0-3 – LINE COUNT
CC0-6 – CHARACTER CODE
ROMDIS – ROM DISABLE
LTEN – LIGHT ENABLE
RVV – REVERSE VIDEO
VSP – VIDEO SUPPRESS
$\overline{BLK}$ – BLANK
S1-3 – SPECIAL FUNCTION
EXEN – EXPANSION ENABLE
$\overline{E0\text{-}8}$ – EXPANSION INPUTS
$\overline{GRAPHE}$ – GRAPHICS ENABLE
$\overline{WR}$ – WRITE
$\overline{CS}$ – CHIP SELECT
A0 – ADDRESS 0
VID1-2 – VIDEO OUTPUTS
$\overline{RESET}$ – RESET
DOTCLK – DOT CLOCK
CCLK – CHARACTER CLOCK

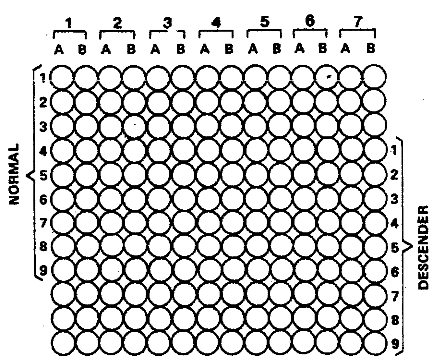
Standard Character Set

	0	1	2	3	4	5	6	7
0	NULL	£	SP	0	@	P	`	p
1	FM	DUP *	!	1	A	Q	a	q
2	¦	¬	"	2	B	R	b	r
3	▶	[illegible]	#	3	C	S	c	s
4	■	[illegible]	$	4	D	T	d	t
5	?	o—	%	5	E	U	e	u
6	▭	[illegible]	&	6	F	V	f	v
7	▬	⊟	'	7	G	W	g	w
8	[illegible]	‾	(	8	H	X	h	x
9	[illegible]	[illegible]	)	9	I	Y	i	y
A	╳	Z	*	:	J	Z	j	z
B	∧	—	+	;	K	[	k	{
C	←	⇧	,	<	L	\	l	|
D	→	⇩	–	=	M	]	m	}
E	[illegible]	A	.	>	N	∧	n	~
F	[illegible]	B	/	?	O	_	o	¢

Overlay Patterns

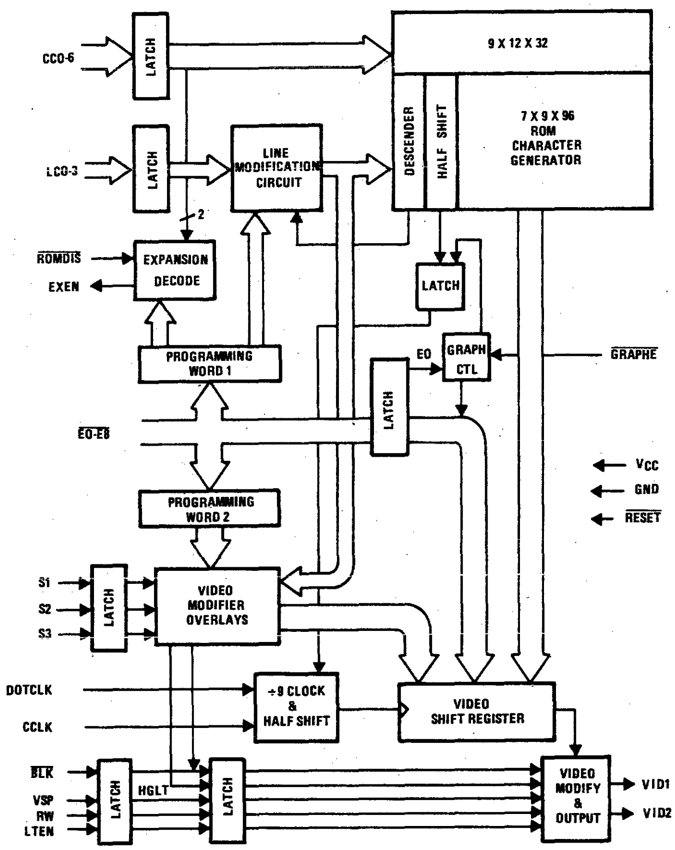
CRISS CROSS	╳	#	CROSS HATCH
UNDERLINE	_	—	HORIZONTAL STRIKE THROUGH
CRISS CROSS	╳		
DIAGONAL STRIKE	/		
DIAGONAL STRIKE	/		
DIAGONAL STRIKE	/		
DASHED UNDERLINE	...		
DASHED UNDERLINE	...		
DASHED UNDERLINE	...		
OPEN BOX	▯		
OPEN BOX	▯		
UNDERDOT	.		
UNDERDOT	.		
REVERSE DIAGONAL	\		
REVERSE DIAGONAL	\		
DOUBLE UNDERLINE	=		

Dot Matrix

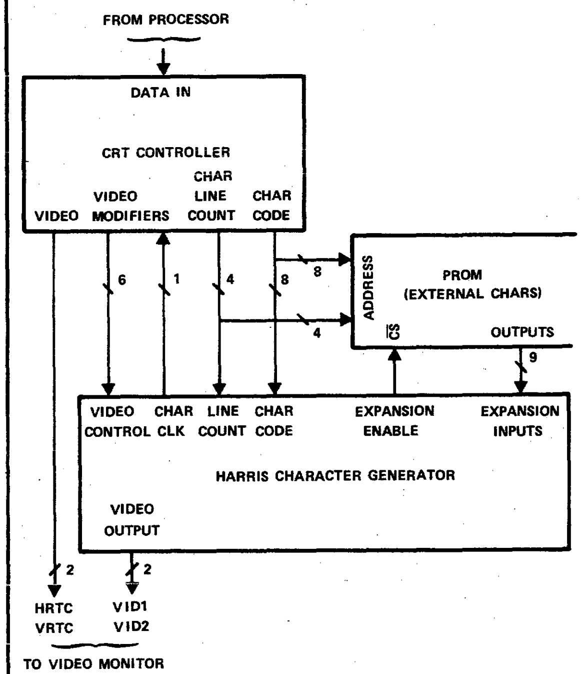


NOTES:
1. EACH ROW MAY HAVE DOTS IN SET A OR SET B ONLY.
2. EACH CHARACTER MAY HAVE DOTS IN NORMAL SET OR DESCENDER SET ONLY.

HS-3819 Block Diagram



System Application



Sales Offices

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EASTERN REGION

2600 Virginia Avenue
Suite 800
Washington, DC 20037
(202) 342-3900
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TWX: 910-576-3418

HOME OFFICE

P.O. Box 883
Melbourne, FL 32901
(305) 724-7045
TWX: 510-959-6259

EUROPEAN

Harris Systems Ltd.
Semiconductor Programs Division
P.O. Box 27
145 Farnham Road
Slough SL1 4XD
United Kingdom
Tel: 34666
TWX: 848174

HARRIS

SEMICONDUCTOR CUSTOM INTEGRATED CIRCUITS DIVISION

HARRIS

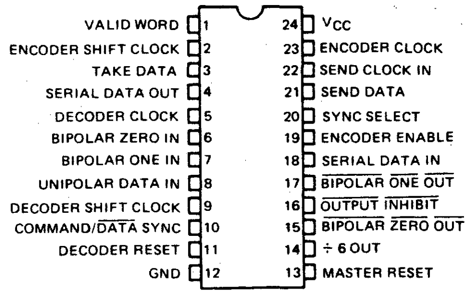
HS-15530RH

Radiation Resistant CMOS Manchester Encoder-Decoder

Features

- SUPPORT OF MIL-STD-1553
- 1.0 MEGABIT/SEC DATA RATE
- SYNC IDENTIFICATION AND LOCK-IN
- CLOCK RECOVERY
- MANCHESTER II ENCODE, DECODE
- SEPARATE ENCODE AND DECODE
- LOW OPERATING POWER: 50mW AT 5 VOLTS
- FULL MILITARY TEMPERATURE RANGE
- FUNCTIONAL TOTAL DOSE . . . 1×10^4 RAD(Si)
- LATCH-UP FREE TO . . . . 5×10^{11} RAD (Si)/sec

Pinout



Description

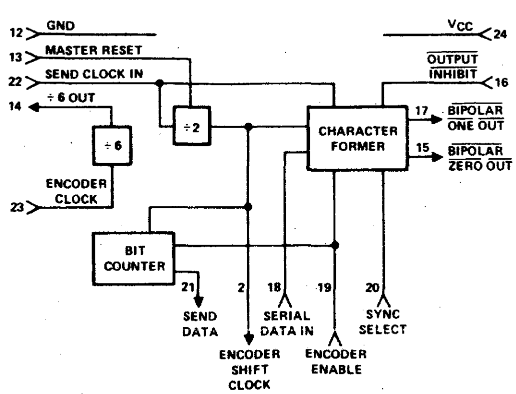
The Harris HS-15530RH is a high performance, radiation resistant, CMOS device intended to service the requirements of MIL-STD-1553 and similar Manchester II encoded, time division multiplexed serial data protocals. This LSI chip is divided into two sections, an Encoder and a Decoder. These sections operate completely independent of each other, except for the Master Reset function.

This circuit provides many of the requirements of MIL-STD-1553. The Encoder produces the sync pulse and the parity bit as well as the encoding of the data bits. The Decoder recognizes the sync pulse and identifies it as well as decoding the data bits and checking parity.

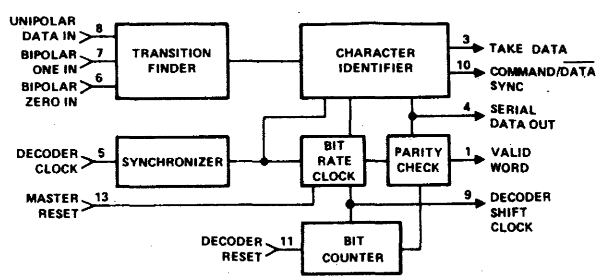
This integrated circuit is fully guaranteed to support the 1MHz data rate of MIL- STD-1553 over both temperature and voltage while residing in a radiation environment. It interfaces with CMOS, TTL or N channel support circuitry, and uses a standard 5 volt supply.

Block Diagrams

ENCODER



DECODER



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} + 0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	–55°C to +125°C

ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±5% T_A = Operating Temperature Range

D.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
V_{IHC}	Logical "1" Input Voltage (Clock)	V_{CC} -0.5			V	
V_{ILC}	Logical "0" Input Voltage (Clock)			GND +0.5	V	
I_{IL}	Input Leakage	-1.0		+1.0	μA	0V ≤ V_{IN} ≤ V_{CC}
V_{OH}	Logical "1" Output Voltage	2.4			V	I_{OH} = -3mA
V_{OL}	Logical "0" Output Voltage			0.4	V	I_{OL} = 1.8mA
I_{CCSB}	Supply Current Standby		0.5	2	mA	V_{IN} = V_{CC} = 5.25V Outputs Open
I_{CCOP}	Supply Current Operating*		8.0	10.0	mA	V_{CC} = 5.25V, f = 1MHz
C_{IN}	Input Capacitance*		5.0	7.0	pF	
C_O	Output Capacitance*		8.0	10.0	pF	

*Guaranteed and sampled but not 100% tested.

ENCODER TIMING V_{CC} = 5.0V ±5% T_A = Operating Temperature Range

A.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
F_{EC}	Encoder Clock Frequency			13	MHz	C_L = 50pF
F_{ESC}	Send Clock Frequency			2.16	MHz	
T_{ECR}	Encoder Clock Rise Time			8	ns	
T_{ECF}	Encoder Clock Fall Time			8	ns	
F_{ED}	Data Rate			1.08	MHz	
T_{MR}	Master Reset Pulse Width	150			ns	
T_{E1}	Shift Clock Delay			125	ns	
T_{E2}	Serial Data Setup	75			ns	
T_{E3}	Serial Data Hold	75			ns	
T_{E4}	Enable Setup	90			ns	
T_{E5}	Enable Pulse Width	80			ns	
T_{E6}	Sync Setup	55			ns	
T_{E7}	Sync Pulse Width	150			ns	
T_{E8}	Send Data Delay	–10		50	ns	
T_{E9}	Bipolar Output Delay			130	ns	

DECODER TIMING V_{CC} = 5.0V ±5% T_A = Operating Temperature Range

A.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
F_{DC}	Decoder Clock Frequency			13	MHz	C_L = 50pF
T_{DCR}	Decoder Clock Rise Time			8	ns	
T_{DCF}	Decoder Clock Fall Time			8	ns	
F_{DD}	Data Rate			1.08	MHz	
T_{DR}	Decoder Reset Pulse Width	150			ns	
T_{DRS}	Decoder Reset Setup Time	75			ns	
T_{MR}	Master Reset Pulse Width	150			ns	
T_{D1}	Bipolar Data Pulse Width	T_{DC} +10			ns	①
T_{D2}	Sync Transition Span		18T_{DC}		ns	①
T_{D3}	One Zero Overlap			T_{DC} -10	ns	①
T_{D4}	Short Data Transition Span		6T_{DC}		ns	①
T_{D5}	Long Data Transition Span		12T_{DC}		ns	①
T_{D6}	Sync Delay (ON)		40	110	ns	
T_{D7}	Take Data Delay (ON)		50	110	ns	
T_{D8}	Serial Data Out Delay		80	80	ns	
T_{D9}	Sync Delay (OFF)		90	110	ns	
T_{D10}	Take Data Delay (OFF)		110	110	ns	
T_{D11}	Valid Word Delay		90	110	ns	

NOTE ① : 15T_{DC} +10 = [15 (Decoder Clock Period)] +10ns T_{DC} = Decoder Clock Period = $\frac{1}{F_{DC}}$

These parameters are guaranteed but not 100% tested.

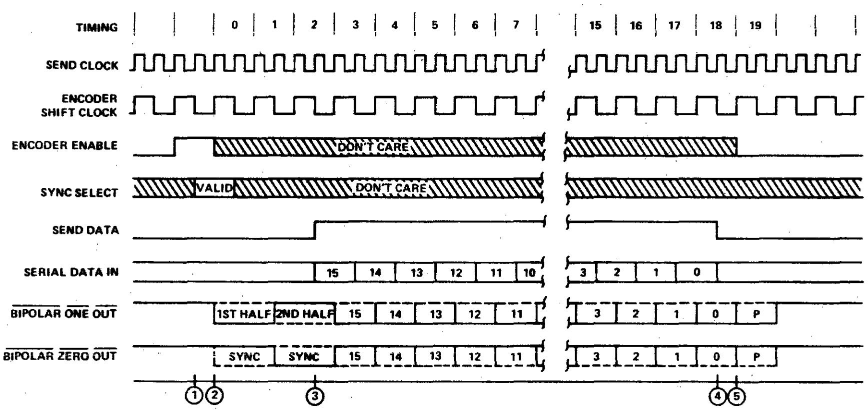
PIN	SECTION	NAME	DESCRIPTION
1	Decoder	VALID WORD	Output high indicates receipt of a valid word.
2	Encoder	ENCODER SHIFT CLOCK	Output for shifting data into the Encoder. This clock shifts data on a low-to-high transition.
3	Decoder	TAKE DATA	Output is high during receipt of data after identification of a sync pulse.
4	Decoder	SERIAL DATA OUT	Delivers received data in correct NRZ format.
5	Decoder	DECODER CLOCK	Input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the Decoder.
6	Decoder	BIPOLAR ZERO IN	A high input should be applied when the bus is in its negative state. This pin must be held high when the Unipolar input is used.
7	Decoder	BIPOLAR ONE IN	A high input should be applied when the bus is in its positive state, this pin must be held low when the Unipolar input is used.
8	Decoder	UNIPOLAR DATA IN	With pin 6 high and pin 7 low, this pin enters unipolar data into the transition finder circuit. If not used this input must be held low.
9	Decoder	DECODER SHIFT CLOCK	Output which delivers a frequency (Decoder Clock ÷ 12), synchronized by the recovered serial data stream.
10	Decoder	COMMAND SYNC	Output of a high from this pin occurs during output of decoded data which was preceded by a Command (or Status) synchronizing character. A low output indicates a Data synchronizing character.
11	Decoder	DECODER RESET	A high input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word.
12	Both	GROUND	Ground supply pin.
13	Both	MASTER RESET	A high on this pin clears 2:1 counters in both the Encoder and Decoder.
14	Encoder	÷ 6 OUT	Output from 6:1 divider which is driven by the ENCODER CLOCK.
15	Encoder	$\overline{\text{BIPOLAR}}$ $\overline{\text{ZERO}}$ $\overline{\text{OUT}}$	An active low output designed to drive the zero or negative sense of a bipolar line driver.
16	Encoder	$\overline{\text{OUTPUT}}$ $\overline{\text{INHIBIT}}$	A low on this input forces pin 15 and pin 17 high, the inactive states.
17	Encoder	$\overline{\text{BIPOLAR}}$ $\overline{\text{ONE}}$ $\overline{\text{OUT}}$	An active low output designed to drive the one or positive sense of a bipolar line driver.
18	Encoder	SERIAL DATA IN	Accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK.
19	Encoder	ENCODER ENABLE	A high on this input initiates the encode cycle. (Subject to the preceding cycle being complete.)
20	Encoder	SYNC SELECT	Actuates command sync for an input high and data sync for an input low.
21	Encoder	SEND DATA	Is an active high output which enables the external source of serial data.
22	Encoder	SEND CLOCK IN	Clock input at a frequency equal to the data rate X2.
23	Encoder	ENCODER CLOCK.	Input to the 6:1 divider.
24	Both	VCC	Positive supply pin.

Encoder Operation

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SEND CLOCK input. An auxillary divide by six counter is provided on chip which can be utilized to produce the SEND CLOCK by dividing the DECODER CLOCK.

The Encoder's cycle begins when ENCODER ENABLE is high during a falling edge of ENCODER SHIFT CLOCK ①. This cycle lasts for one word length or twenty ENCODER SHIFT CLOCK periods. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high at SYNC SELECT input actuates a command sync or a low will produce a data sync for that word ② . When the Encoder is ready to accept data, the SEND DATA output will go high and remain high for sixteen ENCODER SHIFT CLOCK periods ③ . During these sixteen periods the data should be clocked into the SERIAL DATA input with every low-to-high transition of the ENCODER SHIFT CLOCK ③ – ④ . After the sync and the Manchester II coded data are transmitted through the $\overline{\text{BIPOLAR ONE}}$ and $\overline{\text{BIPOLAR ZERO}}$ outputs, the Encoder adds on an additional bit which is the parity for that word ⑤ . At any time a low on $\overline{\text{OUTPUT INHIBIT}}$ input will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To abort the Encoder transmission a positive pulse must be applied at MASTER RESET. Anytime after or during this pulse, a low to high transition on SEND CLOCK clears the internal counters and initializes the Encoder for a new word.



Decoder Operation

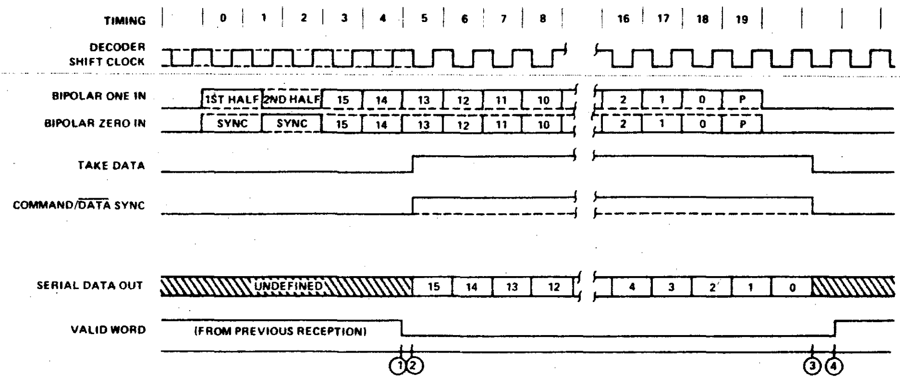
The Decoder requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. The Manchester II coded data can be presented to the Decoder in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in Military Spec 1553. The UNIPOLAR DATA input can only accept non-inverted Manchester II coded data. (e.g. from $\overline{\text{BIPOLAR ZERO OUT}}$ of an Encoder.)

The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized ①, the type of sync is indicated on COMMAND/$\overline{\text{DATA}}$ SYNC output. If the sync character was a command sync, this output will go high ② and remain high for sixteen DECODER SHIFT CLOCK periods ③ , otherwise it will remain low. The TAKE DATA output will go high and remain high ② – ③ while the Decoder is transmitting the decoded data through SERIAL DATA OUT. The decoded data available at SERIAL DATA OUT is in a NRZ format. The DECODER SHIFT CLOCK is provided so that the decoded bits can get shifted into an external register on every low-to-high transition of this clock ② – ③ .

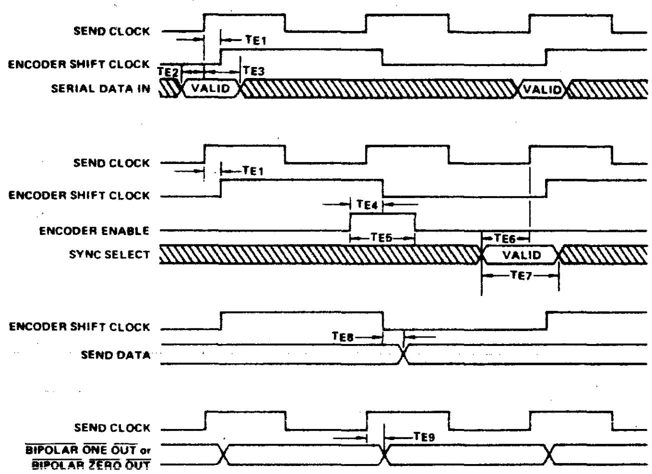
After all sixteen decoded bits have been transmitted ③ the data is checked for odd parity. A high on VALID WORD output ④ indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence.

At any time in the above sequence a high input on DECODER RESET during a low-to-high transition of DECODER SHIFT CLOCK will abort transmission and initialize the Decoder to start looking for a new sync character.

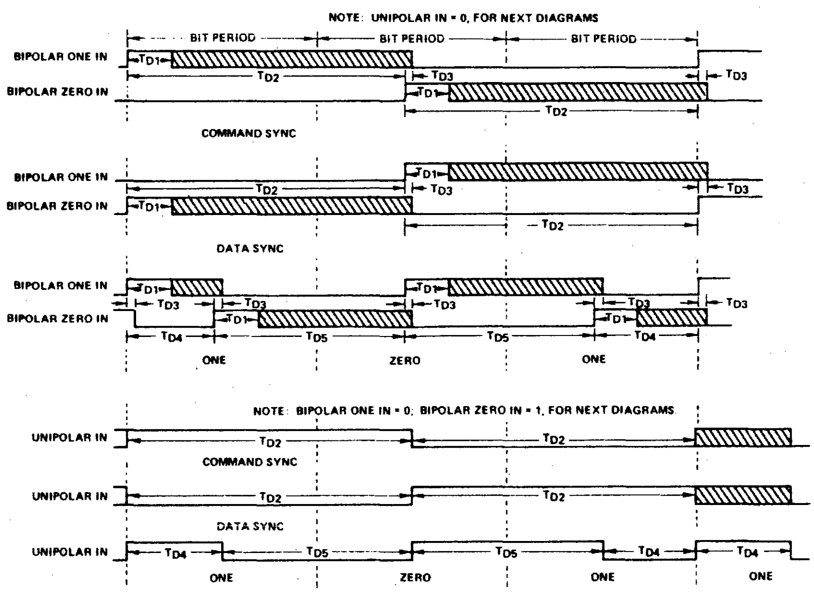
Decoder Operation (continued)



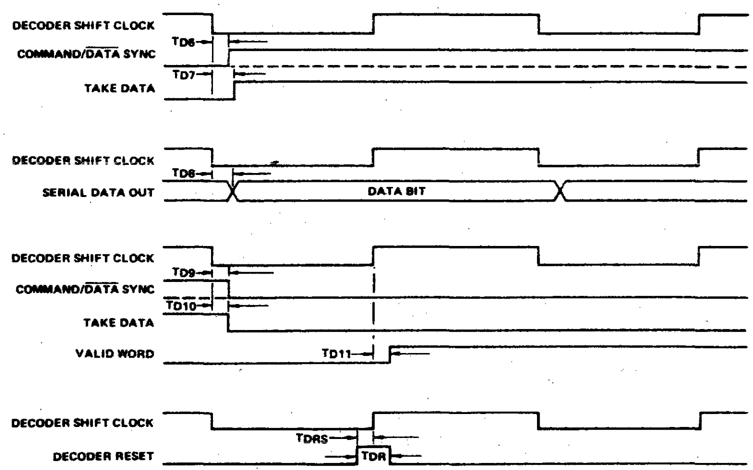
Encoder Timing



Decoder Timing

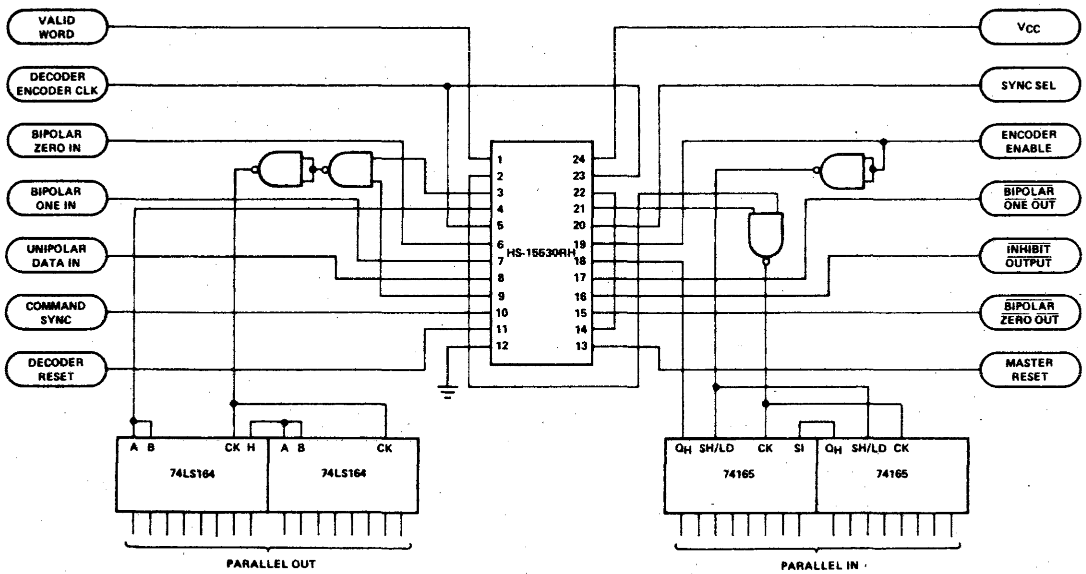


Decoder Timing (continued)

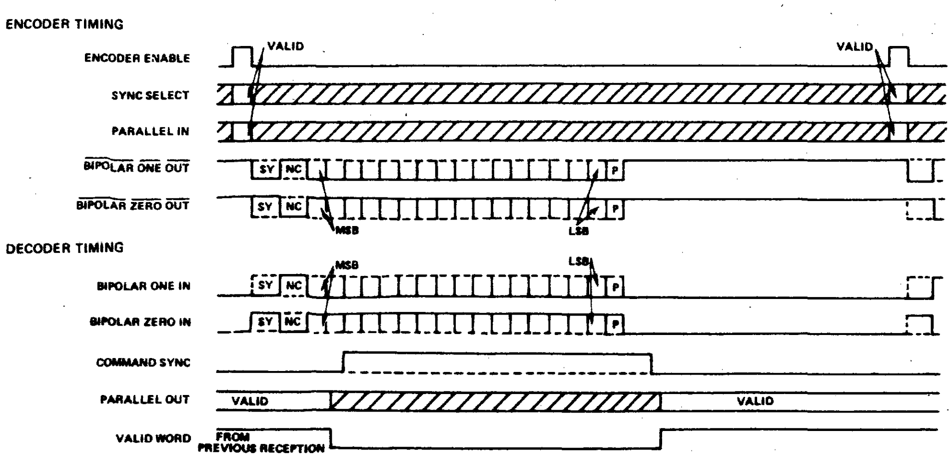


Applications

How to Make Our MTU Look Like a Manchester Encoded UART



Typical Timing Diagrams for a Manchester Encoded UART



The 1553 standard defines a time division multiplexed data bus for application within aircraft. The bus is defined to be bipolar, and encoded in a Manchester II format, so no DC component appears on the bus. This allows transformer coupling and excellent isolation among systems and their environment.

The HS-15530RH supports the full bipolar configuration, assuming a bus driver configuration similar to that in Figure 1. Bipolar inputs from the bus, like Figure 2, are also accommodated.

The signaling format in MIL-STD-1553 is specified on the assumption that the network of 32 or fewer terminals are controlled by a central control unit by means of Command Words, and Data. Terminals respond with Status Words, and Data. Each word is preceded by a synchronizing pulse, and followed by parity bit, occupying a total of 20 μsec. The word formats are shown in Figure 4. The special abbreviations are as follows:

- P — Parity, which is defined to be odd, taken across all 17 bits.
- R/T — Receive on logical zero, transmit on ONE.
- ME — Message Error if logical 1.
- TF — Terminal Flag, if set, calls for controller to request self-test data.

The paragraphs above are intended only to suggest the content of MIL-STD-1553, and do not completely describe its bus requirements, timing or protocols.

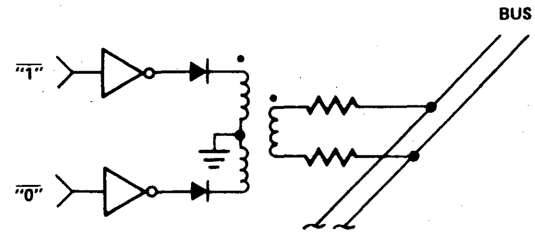


FIGURE 1 – Simplified MIL-STD-1553 Driver

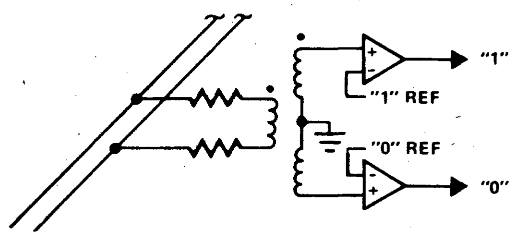


FIGURE 2 – Simplified MIL-STD-1553 Receiver

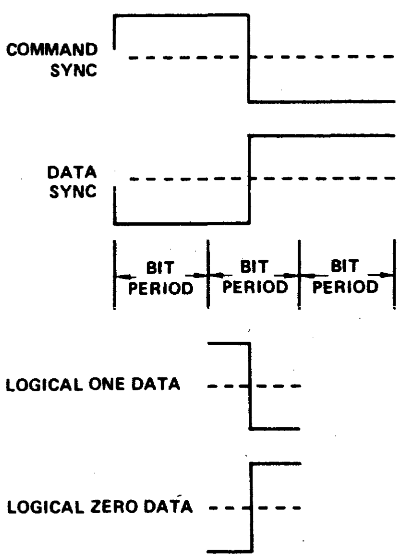


FIGURE 3 – MIL-STD-1553 Character Formats

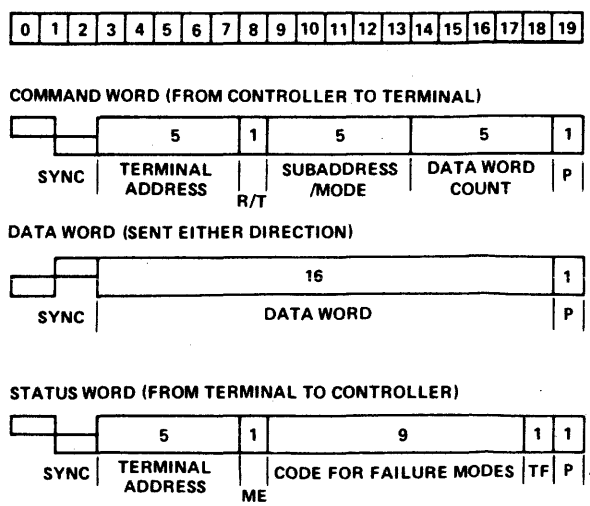


FIGURE 4 – MIL-STD-1553 Word Formats

NOTE: This page is a summary of MIL-STD-1553 and is not intended to describe the operation of the HS-15530RH

Radiation Screening Procedure

(1) Two (2) probed good samples per wafer will be selected from ≥20% of the wafers in a run. (All wafers in a "run" will have been processed together through all high temperature processing steps and through metallization.)

(2) The sample die shall be assembled and tested for functionality.

(3) The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^4 Rad(Si +10% from a Gamma Cell 220 Cobalt 60 source or equivalent. The samples shall be biased at 5 volts with all inputs high. The dose rate shall be between 50 rads/sec and 200 rads/sec.

(4) I_{CCSB} at V_{CC} = 5 volts will be measured and recorded for each device within one hour (±15 minutes) after irradiation. The lot will be accepted only if the average of these measure values is ≤5mA.

Radiation Effects

The HS--15530RH is processed with the same mask set as is used for HARRIS' equivalent commercial part. Latchup free operation, achieved by the use of special starting material and improved total dose hardness, is obtained with special high temperature processing cycles. These process techniques can, in principal, be applied to any standard HARRIS CMOS product.

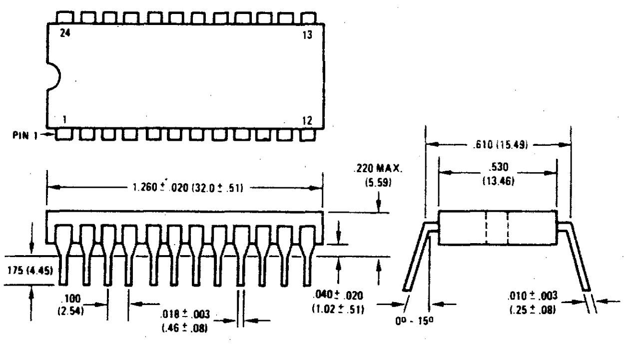
The primary failure mode under exposure to ionizing radiation is an increase in static leakage current (I_{CCSB}). Functional failure due to the increased leakage currents will typically occur for dose levels in excess of 5 x 10^4 RAD-Si. AC and DC parameters other than ICC will change less than 10% for total dose levels under 5 x 10^4 RAD-Si. The excess leakage currents will anneal at room temperature and are typically reduced by a factor of 3-10 within 24 hours after irradiation.

On a production basis, HARRIS is able to perform screens only for a total dose hardness. Transident radiation tests, however, have shown the following results:

Latchup free doses ≥5 x 10^{11} rads/sec. Upset (loss of stored data) typically ≥ 10^8 rads/sec.

Package

24 LEAD DIP



1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ±.010 (±0.25mm) unless otherwise shown.

Ordering Information

HS 1 -15530RH - 2

HARRIS — HS

PACKAGE — 1 — Cerdip

DEVICE NUMBER — 15530RH

TEMPERATURE: 2 — -55°C to +125°C

Sales Offices

UNITED STATES

EASTERN REGION

2600 Virginia Avenue
Suite 800
Washington, DC 20037
(202) 342-3900
TWX: 710-822-9301

Five Old Concord Road
Burlington, MA 01803
(617) 273-1020
TWX: 710-332-1074

106 Seventh Street
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Costa Mesa, CA 92626
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(415) 964-6443
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2850 Metro Dr., Suite 703
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(612) 854-3224
TWX: 910-576-3418

HOME OFFICE

P.O. Box 883
Melbourne, FL 32901
(305) 724-7045
TWX: 510-959-6259

EUROPEAN

Harris Systems Ltd.
Semiconductor Programs Division
P.O. Box 27
145 Farnham Road
Slough SL1 4XD
United Kingdom
Tel: 34666
TWX: 848174

HARRIS

CUSTOM INTEGRATED CIRCUITS DIVISION

HARRIS

HS-6504RH

4096 x 1 CMOS RAM

Preliminary

Features

- LOW POWER STANDBY . . . . 100 μW MAX.
- LOW POWER OPERATION . . . . 25mW/MHz MAX.
- EXTREMELY LOW SPEED POWER PRODUCT
- FUNCTIONAL TOTAL DOSE . . . . 1 x 10^5 RAD Si
- DATA UPSET . . . . $>10^8$ RAD Si/SEC
- LATCH - UP FREE TO . . . . $>5 \times 10^{11}$ RAD Si/SEC
- TTL COMPATIBLE INPUT/OUTPUT
- THREE - STATE OUTPUT
- STANDARD JEDEC PINOUT
- FAST ACCESS TIME . . . . 200nsec TYP
- MILITARY TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON CHIP ADDRESS REGISTER

Description

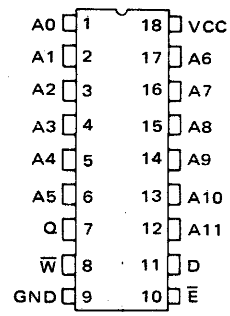
The HS–6504RH is a 4096 x 1 static CMOS RAM fabricated using the Harris Custom Integrated Circuits Division radiation hardened self-aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

On-chip latches are provided for addresses, data input and data output allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance for use in expanded memory arrays.

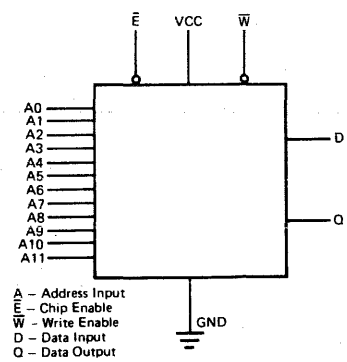
The HS–6504RH is a fully static RAM and may be maintained in any state for an indefinite period of time.

Pinout

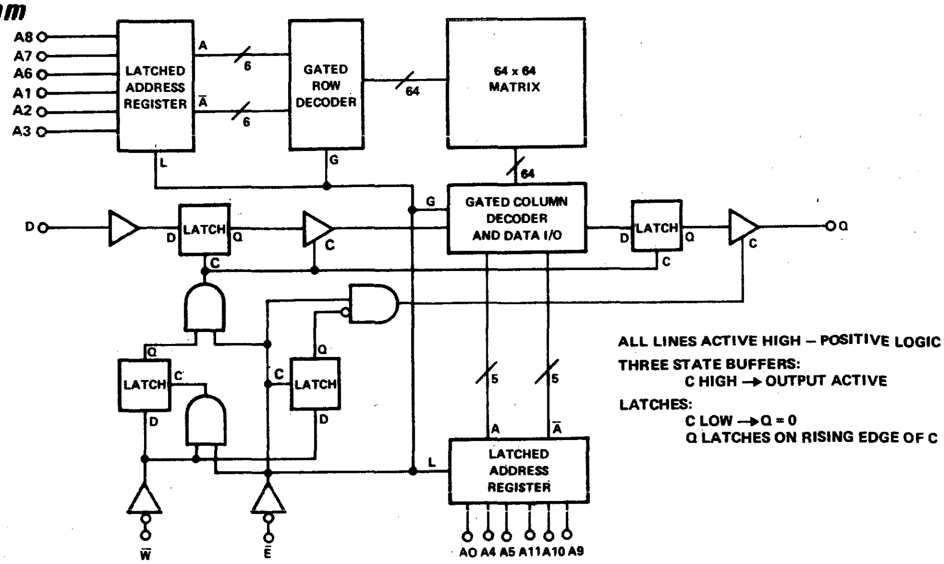
TOP VIEW



Logic Symbol



Functional Diagram



Information on this device is preliminary. Data is subject to change unless otherwise specifically agreed. No obligations are assumed for notice of change or future manufacture of this device.

CAUTION: These devices are sensitive to electrostatic discharge.

Symbols and Abbreviations

This data sheet utilizes a new set of specification nomenclature. This new format is an IEEE and JEDEC supported standard for semiconductor memories. It is intended to clarify the symbols, abbreviations and definitions, and to make all memory data sheets consistent. We believe that, once acclimated, you will find this standardized format easy to read and use.

ELECTRICAL PARAMETER ABBREVIATIONS

All abbreviations use upper case letters with no subscripts. The initial symbol is one of these four characters:

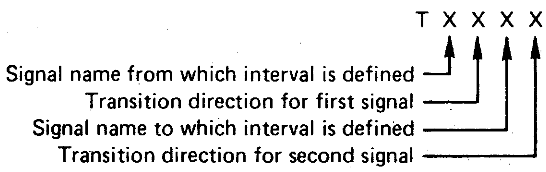
V (Voltage)
I (Current)
P (Power)
C (Capacitance)

The second letter specifies input (I) or output (O), and the third letter indicates the high (H), low (L) or off (Z) state of the pin during measurements. Examples:

VIL — Input Low Voltage
IOZ — Output Leakage Current

TIMING PARAMETER ABBREVIATIONS

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:



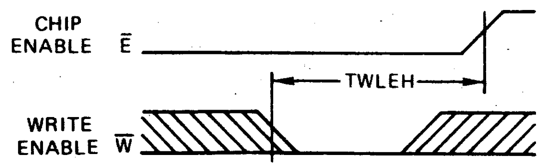
Signal Definitions:

A = Address
D = Data In
Q = Data Out
W = Write Enable
E = Chip Enable
S = Chip Select
G = Output Enable

Transition Definitions:

H = Transition to High
L = Transition to Low
V = Transition to Valid
X = Transition to Invalid or Don't Care
Z = Transition to Off (High Impedance)

EXAMPLE:

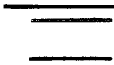
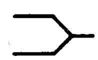


The example shows Write pulse setup time defined as TWLEH-Time from Write enable Low to chip Enable High.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set-up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	—	HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS

Supply Voltage - (VCC - GND)	-0.3V to +7.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage	4.5V to 5.5V
Operating Temperature	-55°C to +125°C

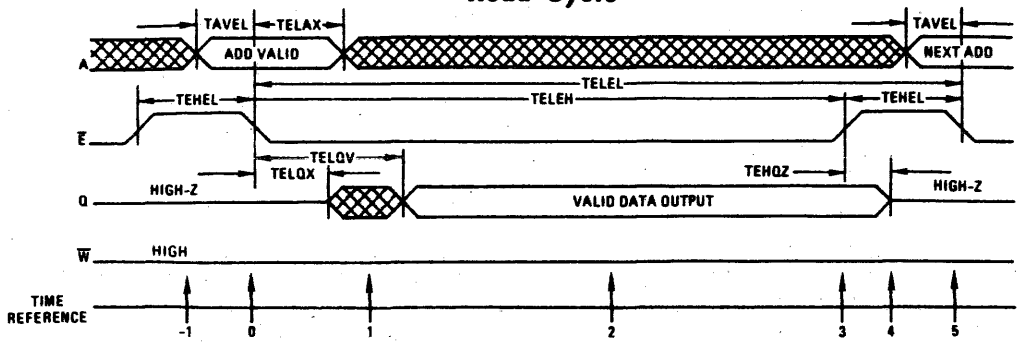
CAUTION: To prevent permanent damage to this device, care should be exercised to insure that the absolute maximum ratings for supply voltages, temperature and voltage or current at any pin is not exceeded during both static and dynamic operation.

ELECTRICAL CHARACTERISTICS ⑤

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE		TEMP = 25°C ① VCC = 5.0V TYPICAL		UNITS	TEST CONDITIONS
			MIN	MAX	PRE RAD	POST RAD		
D.C.	ICCSB	Standby Supply Current		100	5	5	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		7	4.5		mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Current		50	3	3	μA	IO = 0, VCC = 3.0 VI = VCC or GND
	VCCDR	Data Retention Voltage		3	2.6	1.8	V	
	II	Input Leakage Current	−1	+1	0	0	uA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	−10	+10	±0.5	±0.5	μA	GND ≤ VI ≤ VCC
	VIL	Input Low Voltage	−0.3	0.8	1.5	1.3	V	
	VIH	Input High Voltage All inputs except Ē R/W̄	VCC −2.0	VCC +0.3	2.7	2.3	V	
	VIH	Input High Voltage for Ē R/W̄	VCC −1.5	VCC +0.3	2.9	1.9	V	
	VOL	Output Low Voltage		0.4	0.2	0.15	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.6	4.0	V	IO = −1.0mA
	CI	Input Capacitance ③		8.0	5.0	5.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance ③		10.0	6.0	6.0	pF	f = 1MHz VI = VCC or GND
A.C.	TELQV	Chip Enable Access Time		300	150	180	ns	④
	TAVQV	Address Access Time		320	140	180	ns	④
	TELQX	Chip Enable Output Enable Time		100	50	60	ns	④
	TEHQZ	Chip Enable Output Disable Time		100	50	60	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		150	180	ns	④
	TEHEL	Chip Enable Pulse Positive Width	120		40	80	ns	④
	TAVEL	Address Setup Time	20		−10	0	ns	④
	TELAX	Address Hold Time	50		30	35	ns	④
	TWLWH	Write Enable Pulse Width	80		20	30	ns	④
	TWLEH	Write Enable Pulse Setup Time	200		140	140	ns	④
	TWLEL	Early Write Pulse Setup Time	0		−15	−10	ns	④
	TWHEL	Write Enable Read Mode Setup Time	0		−15	−10	ns	④
	TELWH	Early Write Pulse Hold Time	80		40	50	ns	④
	TDVWL	Data Setup Time	0		−15	−10	ns	④
	TDVEL	Early Write Data Setup Time	0		−15	−10	ns	④
	TWLDX	Data Hold Time	80		50	60	ns	④
	TELDX	Early Write Data Hold Time	80		50	60	ns	④
	TELWL	Early Write Output Hi-Z Time	0		−10	−10	ns	④
	TQVWL	Data Valid to Write Time	0		0	0	ns	④
	TELEL	Read or Write Cycle Time	420		190	260	ns	④

NOTES:
1. All devices guaranteed at worst case limits. Room temp., 5 volt data provided for information and not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Post Rad Data @ TD = 1 x10^5.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC test Conditions: Inputs: TRISE = TFALL ≤ 20nsec; Outputs: 1TTL Load and 50 pF. All timing measurements at 1/2 VCC.
5. Pre-Radiation and Post-Radiation limits.

Read Cycle

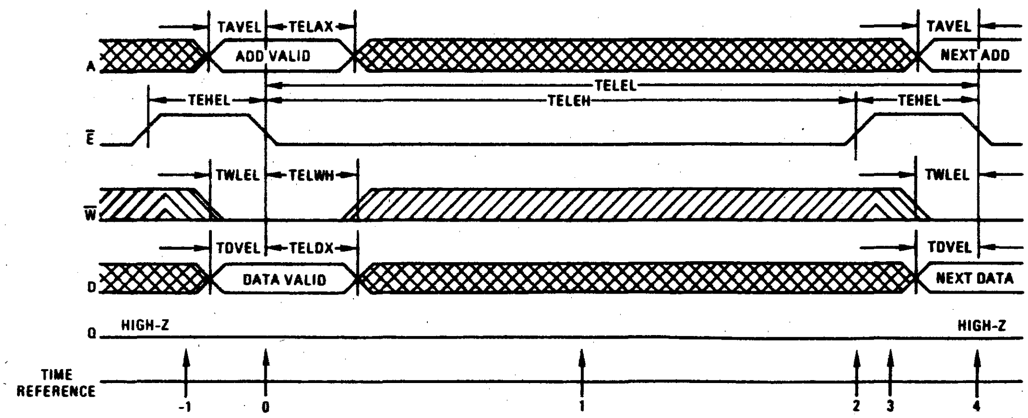


TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	OUTPUT Q	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	OUTPUT ENABLED
2	L	H	X	V	OUTPUT VALID
3	↗	H	X	V	READ ACCOMPLISHED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of Ē (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until during time (T = 2). W̄ must remain high until after time (T = 2). After the output data has been read, Ē may return high (T = 3). This will disable the output buffer and ready the RAM for the next memory cycle (T = 4).

Early Write Cycle

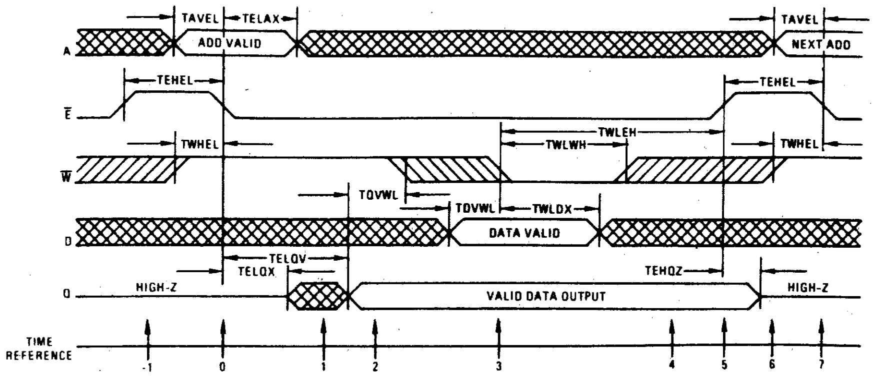


TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	L	V	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	X	X	X	Z	WRITE IN PROGRESS INTERNALLY
2	↗	X	X	X	Z	WRITE COMPLETED
3	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
4	↘	L	V	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The early write cycle is the only cycle where the output is guaranteed not to become active. On the falling edge of Ē (T = 0), the addresses, the write signal, and the data input are latched in on chip registers. The logic value of W̄ at the time Ē falls determines the state of the output buffer for that cycle. Since W̄ is low when Ē falls, the output buffer is latched into the high impedance state and will remain in that state until Ē returns high (T = 2). For this cycle, the data input is latched by Ē going low; therefore data set up and hold times should be referenced to Ē. When Ē (T = 2) returns to the high state the output buffer disables and all signals are unlatched. The device is now ready for the next cycle.

Read Modify Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	⤥	H	V	X	Z	CYCLE BEGINS, ADDRESS ARE LATCHED
1	L	H	X	X	X	OUTPUT ENABLED
2	L	H	X	X	V	OUTPUT VALID, READ AND MODIFY TIME
3	L	⤥	X	V	V	WRITE BEGINS, DATA IS LATCHED
4	L	X	X	X	V	WRITE IN PROGRESS INTERNALLY
5	⤤	X	X	X	V	WRITE COMPLETED
6	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
7	⤥	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The read modify write cycle begins as all other cycles on the falling edge of Ē (T= 0). The W̄ line should be high at (T = 0) in order to latch the output buffers in the active state. During (T = 1) the output will be active but not valid until (T = 2). On the falling edge of the W̄ (T = 3) the data present at the output and input are latched. The W̄ signal also latches itself on its low going edge. All input signals excluding Ē have been latched and have no further effect on the RAM. The rising edge of Ē (T = 5) completes the write portion of the cycle and unlatches all inputs and output. The output goes to a high impedance and the RAM is ready for the next cycle.

NOTES: In the above descriptions the numbers in parenthesis (T = n) refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

Radiation Screening Procedure

(1) Two (2) probed good samples per wafer will be selected from ≥ 20% of the wafers in a run. (All wafers in a "run" will have been processed together through all high temperature processing steps and through metallization.)

(2) The sample die shall be assembled and tested to the production test program for proper operation.

(3) The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^5 Rad Si (± 10%) from a Gamma Cell 220 Cobalt 60 source or equivalent. The samples shall be biased at 5 volts with all inputs high. The dose rate shall be between 50 rads/sec and 200 rads/sec.

(4) The samples will be tested to the data sheet limits within one hour (±15 minutes) after irradiation. The lot will be accepted only if all units, exclusive of non-radiation failures, meet the data sheet limits.

Radiation Effects

The HS-6504RH is an RH memory designed to survive in a radiation environment and to meet the electrical characteristics and be pin compatible to the Harris equivalent commercial part. Latchup free operation, achieved by the use of special starting material and improved total dose hardness, is obtained with special high temperature processing cycles. These process techniques can, in principle, be applied to any standard HARRIS CMOS product.

On a production basis, HARRIS only performs screens for total dose hardness to a level of 1 x 10^5 rad-Si. Transient radiation tests, however, have shown the following results:

Latchup free to doses ≥ 5 x 10^{11} rads/sec.
Upset (loss of stored data) typically ≥ 10^8 rads/sec.

Test Product Flow

HARRIS SEMICONDUCTOR PRODUCT FLOW
MIL-STD-883, METHOD 5004 CLASS B

100% SCREENING PROCEDURE

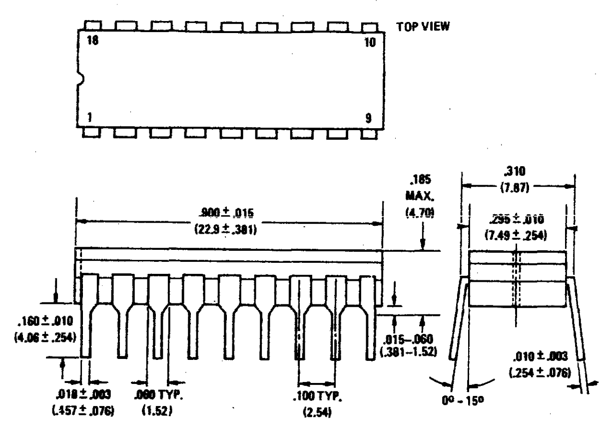
	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1010 Cond. C
4	Constant Acceleration	2001 Cond. E; Y1 plane
5	Seal: A Fine B Gross	1014 Cond. A or B 1014 Cond. C2
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. @ 125°C (or equivalent) (Burn-In circuits enclosed)
8	Final Electrical 100% go-no-go	Tested at Worst Case Operating Conditions
9	External Visual	2009 Sample Inspection

Notes:

- Traceability: All devices are assigned date code identification that provides traceability back to the inspection lot.
- Branding: All devices are branded with the part number and EIA date code.
- Aged Products: Product that has been held for more than 24 months will be reinspected prior to shipment to group A inspection requirements.
- Additional Requirements: Sample Group A electrical tests are performed on a lot acceptance basis.

Packaging

18 LEAD CERAMIC DIP



1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ± .010 (± 0.25mm) unless otherwise shown.

Ordering Information

Example: **HS 1 - 6504RH**

- HS — HARRIS CUSTOM INTEGRATED CIRCUITS DIVISION
- 1 — PACKAGE
- 6504RH — DEVICE

PACKAGE

FLAT PACK	9-
CERDIP	1-

NOTICE: Harris Semiconductor's products are sold by description only. Harris Semiconductor reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders.

Sales Offices

UNITED STATES

EASTERN REGION

2600 Virginia Avenue
Suite 800
Washington, DC 20037
(202) 342-3900
TWX: 710-822-9301

Five Old Concord Road
Burlington, MA 01803
(617) 273-1020
TWX: 710-332-1074

106 Seventh Street
Garden City, NY 11530
(516) 747-6776

WESTERN REGION

1503 South Coast Drive
Suite 320
Costa Mesa, CA 92626
(714) 957-6557
TWX: 910-595-1533

625 Ellis, Suite 300
Mt. View, CA 94043
(415) 964-6443
TWX: 910-379-6431

MIDWEST REGION

2850 Metro Dr., Suite 703
Minneapolis, MN 55420
(612) 854-3224
TWX: 910-576-3418

HOME OFFICE

P.O. Box 883
Melbourne, FL 32901
(305) 724-7045
TWX: 510-959-6259

EUROPEAN

Harris Systems Ltd.
Semiconductor Programs Division
P.O. Box 27
145 Farnham Road
Slough SL1 4XD
United Kingdom
Tel: 34666
TWX: 848174

HARRIS

CUSTOM INTEGRATED CIRCUITS DIVISION

HARRIS

HS-6508RH

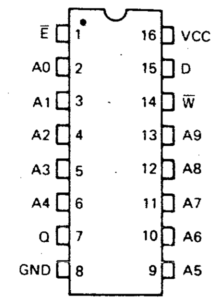
1024 x 1 CMOS RAM

Features

- FUNCTIONAL TOTAL DOSE . . . . 2 x 10^4 RAD Si
- LATCH-UP FREE TO . . . . 5.0 x 10^{11} RAD Si/sec
- LOW STANDBY POWER . . . . 550 μW MAX
- LOW OPERATING POWER . . . . 25mW/MHz MAX
- FAST ACCESS TIME . . . . 300nsec MAX
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE – 2 TTL LOADS
- HIGH NOISE IMMUNITY
- ON-CHIP ADDRESS REGISTER
- MILITARY TEMPERATURE RANGE
- THREE-STATE OUTPUTS
- 16 PIN PACKAGE FOR HIGH DENSITY

Pinout

TOP VIEW



A – Address Input D – Data Input
Ē – Chip Enable Q – Data Output
W̄ – Write Enable

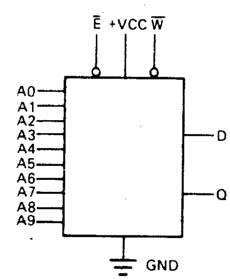
Description

The HS-6508RH is a 1024 by 1 static CMOS RAM fabricated using the HARRIS Programs Division radiation hardened self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

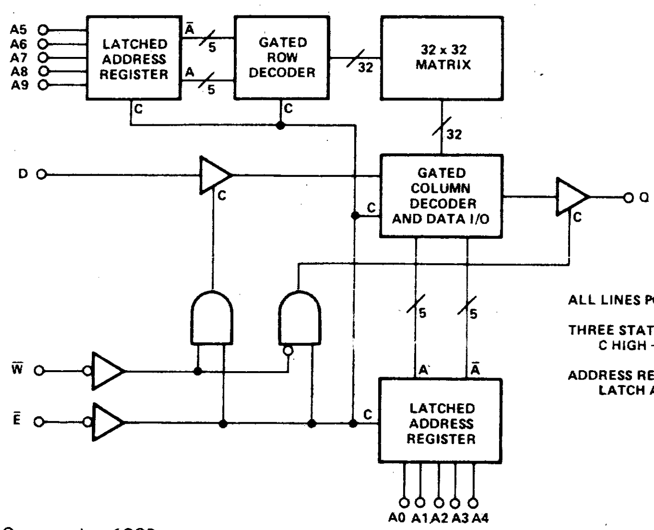
On-chip latches are provided for addresses allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HS-6508RH is a fully static RAM and may be maintained in any state for an indefinite period of time.

Logic Symbol



Functional Diagram



ALL LINES POSITIVE LOGIC – ACTIVE HIGH

THREE STATE BUFFERS:
C HIGH → OUTPUT ACTIVE

ADDRESS REGISTER AND DECODERS:
LATCH AND GATE ON RISING EDGE OF C

Symbols and Abbreviations

This data sheet utilizes a new set of specification nomenclature. This new format is an IEEE and JEDEC supported standard for semiconductor memories. It is intended to clarify the symbols, abbreviations and definitions, and to make all memory data sheets consistent. We believe that, once acclimated, you will find this standardized format easy to read and use.

ELECTRICAL PARAMETER ABBREVIATIONS

All abbreviations use upper case letters with no subscripts. The initial symbol is one of these four characters:

V (Voltage)
I (Current)
P (Power)
C (Capacitance)

The second letter specifies input (I) or output (O), and the third letter indicates the high (H), low (L) or off (Z) state of the pin during measurements. Examples:

VIL — Input Low Voltage
IOZ — Output Leakage Current

TIMING PARAMETER ABBREVIATIONS

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:

T X X X X

- Signal name from which interval is defined (first X)
- Transition direction for first signal (second X)
- Signal name to which interval is defined (third X)
- Transition direction for second signal (fourth X)

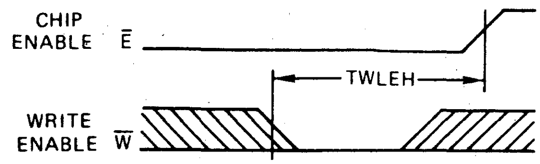
Signal Definitions:

A = Address
D = Data In
Q = Data Out
W = Write Enable
E = Chip Enable
S = Chip Select
G = Output Enable

Transition Definitions:

H = Transition to High
L = Transition to Low
V = Transition to Valid
X = Transition to Invalid or Don't Care
Z = Transition to Off (High Impedance)

EXAMPLE:

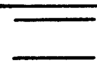
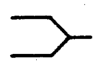


The example shows Write pulse setup time defined as TWLEH-Time from Write enable Low to chip Enable High.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set-up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	—	HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -VCC	7.0V	Operating Supply Voltage -VCC	4.5V to 5.5V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V		
Storage Temperature	-65°C to +150°C	Operating Temperature	-55°C to +125°C

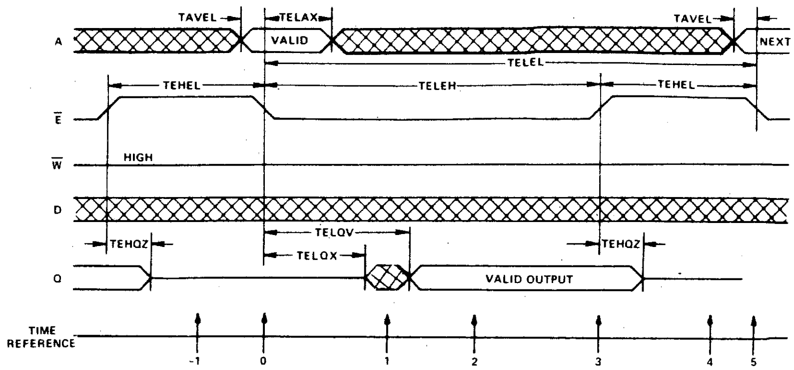
CAUTION: To prevent permanent damage to this device, care should be exercised to insure that the absolute maximum ratings for supply voltages, temperature and voltage or current at any pin is not exceeded during both static and dynamic operation.

ELECTRICAL CHARACTERISTICS ⑤

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100		10	100	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3		1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5		5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 3.2mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -3mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300		160	250	ns	④
	TAVQV	Address Access Time		310		160	260	ns	④
	TELQX	Chip Enable Output Enable Time		200		60	170	ns	④
	TWLQZ	Write Enable Output Disable Time		200		60	170	ns	④
	TEHQZ	Chip Enable Output Disable Time		200		60	170	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		250	160		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		130	90		ns	④
	TAVEL	Address Setup Time	10		10	0		ns	④
	TELAX	Address Hold Time	70		50	40		ns	④
	TDVWH	Data Setup Time	130		100	80		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	160		130	100		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	160		130	100		ns	④
	TWLWH	Write Enable Pulse Width	160		130	100		ns	④
	TELEL	Read or Write Cycle Time	450		380	250		ns	④

NOTES:
1. All devices guaranteed at worst case limits. Room temp., 5 volt data provided for information and not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.
5. Pre-Radiation characteristics. See Radiation effects section for Post-Radiation characteristics.

Read Cycle

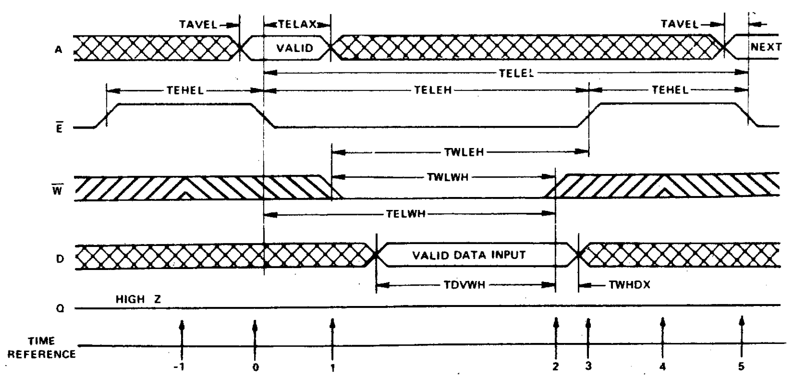


TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUTS Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↓	H	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	X	OUTPUT ENABLED
2	L	H	X	X	V	OUTPUT VALID
3	↑	H	X	X	V	READ ACCOMPLISHED
4	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↓	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

In the HS-6508RH Read Cycle, the address information is latched into the on-chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the data output becomes enabled; however, the data is not valid until during time (T = 2). $\overline{W}$ must remain high for the read cycle. After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the chip and force the output buffer to a high impedance state. After the required $\overline{E}$ high time (TEHEL) the RAM is ready for the next memory cycle (T = 4).

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUTS Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↓	X	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	↓	X	X	Z	WRITE PERIOD BEGINS
2	L	↑	X	V	Z	DATA IS WRITTEN
3	↑	H	X	X	Z	WRITE COMPLETED
4	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↓	X	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The write cycle is initiated by the falling edge of $\overline{E}$ which latches the address information into the on-chip registers. The write portion of the cycle is defined as both $\overline{E}$ and $\overline{W}$ being low simultaneously. $\overline{W}$ may go low anytime during the cycle provided that the write enable pulse setup time (TWLEH) is met. The write portion of the cycle is terminated by the first rising edge of either $\overline{E}$ or $\overline{W}$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the rising edge of $\overline{E}$. By positioning the $\overline{W}$ pulse at different times within the $\overline{E}$ low time (TELEH), various types of write cycles may be performed.

If the $\overline{E}$ low time (TELEH) is greater than the $\overline{W}$ pulse (TWLWH) plus an output enable time (TELQX), a combination read write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH). The data input and data output pins may be tied together for use with a common I/O data bus structure. When using the RAM in this method allow a minimum of one output disable time (TWLQZ) after $\overline{W}$ goes low before applying input data to the bus. This will insure that the output buffers are not active.

Radiation Screening Procedure

(1) Two (2) probed good samples per wafer will be selected from $\geq$20% of the wafers in a run. (All wafers in a "run" will have been processed together through all high temperature processing steps and through metallization.)

(2) The sample die shall be assembled and tested for functionality.

(3) The sample devices shall be subjected to a Total Dose Radiation level of 2 x 10^4 Rad Si($\pm$10%) from a Gamma Cell 220 Cobalt 60 source or equivalent. The samples shall be biased at 5 volts with all inputs high. The dose rate shall be between 50 rads/sec and 200 rads/sec.

(4) I_{CCSB} at V_{CC} = 5 volts will be measured and recorded for each device within one hour ($\pm$15 minutes) after irradiation. The lot will be accepted only if the average of these measured values is $\leq$10mA.

Radiation Effects

The HS-6508RH is a radiation hardened memory processed with the same mask set as is used for HARRIS' equivalent commercial part. Latchup free operation, achieved by the use of special starting material and improved total dose hardness, is obtained with special high temperature processing cycles. These process techniques can, in principal, be applied to any standard HARRIS CMOS product.

The primary failure mode under exposure to ionizing radiation is an increase in static leakage current (ICCSB). Functional failure due to the increased leakage currents will typically occur for dose levels in excess of 5 x 10^4 RAD-SI. AC and DC parameters other than ICC will change less than 10% for total dose levels under 5 x 10^4 RAD-SI. The excess leakage currents will anneal at room temperature and are typically reduced by a factor of 3-10 within 24 hours after irradiation.

On a production basis, HARRIS is able to perform screens only for total dose hardness. Transient radiation tests, however, have shown the following results:

Latchup free to doses $\geq$ 5 x 10^{11} rads/sec.
Upset (loss of stored data) typically $\geq 10^8$ rads/sec.

HARRIS SEMICONDUCTOR PRODUCT FLOW
MIL-M-38510/MIL-STD-883, METHOD 5004 CLASS B

100% SCREENING PROCEDURE

	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1010 Cond. C
4	Constant Acceleration	2001 Cond. E; Y1 plane
5	Seal: (A) Fine (B) Gross	1014 Cond. A or B 1014 Cond. C2
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. @ 125°C (or equivalent) (Burn-In circuits enclosed)
8	Final Electrical 100% go-no-go	Tested at Worst Case Operating Conditions
9	External Visual	2009 Sample Inspection

Note:

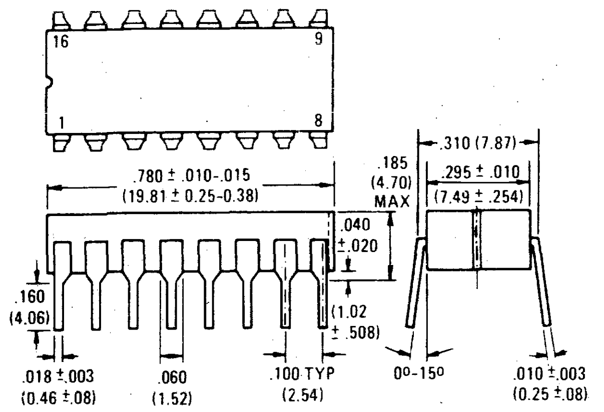
Traceability: All devices are assigned date code identification that provides traceability back to the inspection lot.

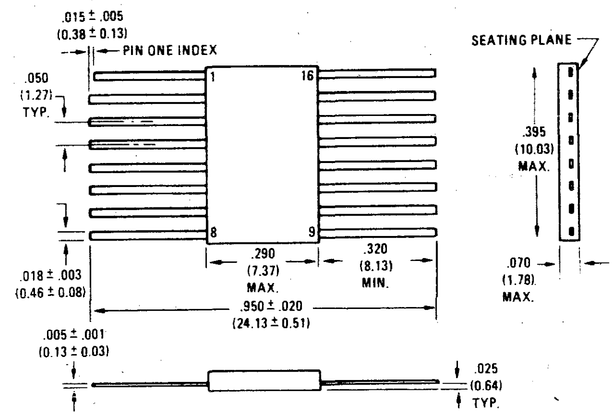
Branding: All devices are branded with the part number and EIA date code.

Aged Products: Product that has been held for more than 24 months will be reinspected prior to shipment to group A inspection requirements.

Additional Requirements: Sample Group A electrical tests are performed on a lot acceptance basis.

Packaging





1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ±.010 (± 0.25mm) unless otherwise shown.

Ordering Information

Example: HS 1 - 6508 RH

HARRIS PROGRAMS DIVISION (HS)
PACKAGE (1)
DEVICE (6508)
VERSION (RH)

PACKAGE

FLAT PACK	9-
CERDIP	1-

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HARRIS

HS-6514RH

1024 x 4 CMOS RAM

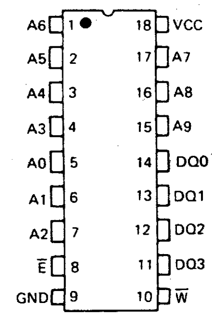
Preliminary

Features

- LOW POWER STANDBY — 100μW MAX.
- LOW POWER OPERATION — 25mW/MHz MAX.
- FUNCTIONAL TOTAL DOSE — 1×10^5 RAD Si
- DATA UPSET — $>10^8$ RADS Si/sec
- LATCH - UP FREE TO — $>5 \times 10^{11}$ RAD Si/sec
- TTL COMPATIBLE INPUT/OUTPUT
- COMMON DATA IN/OUT
- THREE - STATE OUTPUTS
- STANDARD JEDEC PINOUT
- FAST ACCESS TIME — 200 nsec TYP.
- MILITARY TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON - CHIP ADDRESS REGISTER

Pinout

TOP VIEW



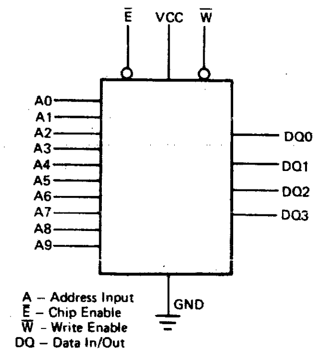
Description

The HS–6514RH is a 1024 x 4 static CMOS RAM fabricated using the Harris Custom Integrated Circuits Division radiation hardened self-aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

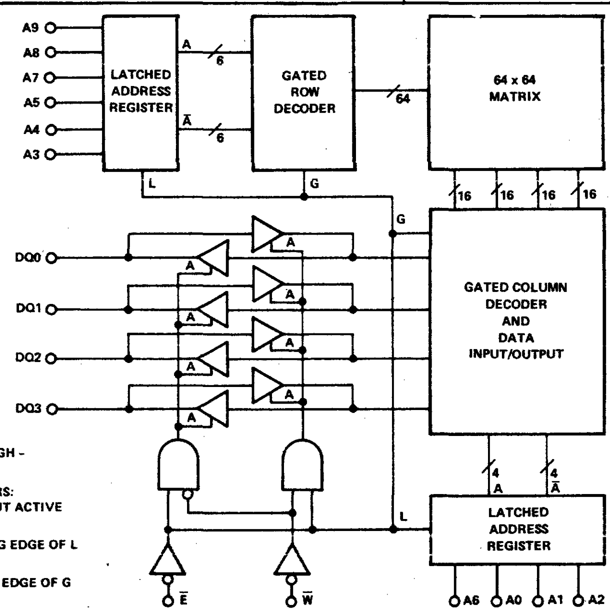
On-chip latches are provided for the addresses allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory systems.

The HS–6514RH is a fully static RAM and may be maintained in any state for an indefinite period of time.

Logic Symbol



Functional Diagram



Information on this device is preliminary. Data is subject to change unless otherwise specifically agreed. No obligations are assumed for notice of change or future manufacture of this device.

CAUTION: **These devices are sensitive to electrostatic discharge.**

Symbols and Abbreviations

This data sheet utilizes a new set of specification nomenclature. This new format is an IEEE and JEDEC supported standard for semiconductor memories. It is intended to clarify the symbols, abbreviations and definitions, and to make all memory data sheets consistent. We believe that, once acclimated, you will find this standardized format easy to read and use.

ELECTRICAL PARAMETER ABBREVIATIONS

All abbreviations use upper case letters with no subscripts. The initial symbol is one of these four characters:

V (Voltage)
I (Current)
P (Power)
C (Capacitance)

The second letter specifies input (I) or output (O), and the third letter indicates the high (H), low (L) or off (Z) state of the pin during measurements. Examples:

VIL — Input Low Voltage
IOZ — Output Leakage Current

TIMING PARAMETER ABBREVIATIONS

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:

T X X X X

Signal name from which interval is defined
Transition direction for first signal
Signal name to which interval is defined
Transition direction for second signal

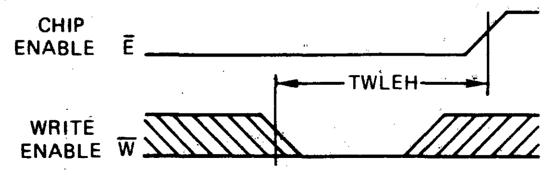
Signal Definitions:

A = Address
D = Data In
Q = Data Out
W = Write Enable
E = Chip Enable
S = Chip Select
G = Output Enable

Transition Definitions:

H = Transition to High
L = Transition to Low
V = Transition to Valid
X = Transition to Invalid or Don't Care
Z = Transition to Off (High Impedance)

EXAMPLE:

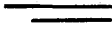
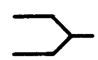


The example shows Write pulse setup time defined as TWLEH-Time from Write enable Low to chip Enable High.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set-up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	—	HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS

Supply Voltage – (VCC -GND)	-0.3V to +7.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC + 0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage	4.5V to 5.5V
Operating Temperature	–55°C to +125°C

CAUTION: To prevent permanent damage to this device, care should be exercised to insure that the absolute maximum ratings for supply voltages, temperature and voltage or current at any pin is not exceeded during both static and dynamic operation.

ELECTRICAL CHARACTERISTICS ⑤

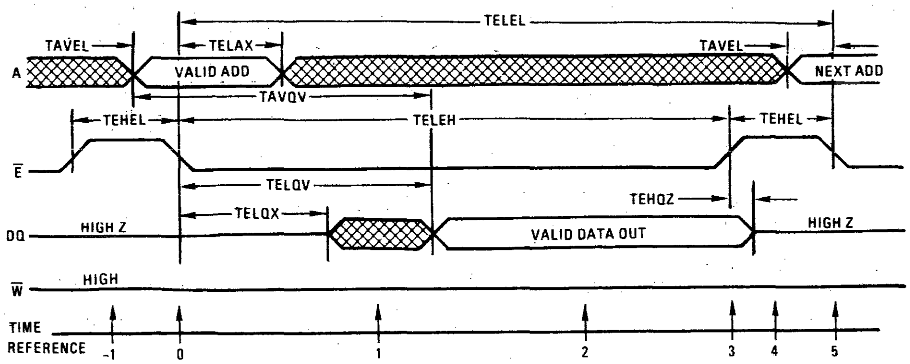
	SYMBOL	PARAMETER	TEMP. & VCC= OPERATING RANGE MIN	MAX	TEMP = 25°C ① VCC = 5.0V TYPICAL PRE RAD	POST RAD	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		250	6	6	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		7	4.5		mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retenetion Current		50	4	4	μA	IO=0 VI=VCC or GND VCC=3.0V
	VCCDR	Data Retention Voltage		3.0	2.6	1.8	V	
	II	Input Leakage Current	–1	+1	0	0	μA	GND≤VI≤VCC
	IIOZ	Input/Output Leakage Current	–10	+10	±0.5	±0.5	μA	GND≤VIO≤VCC
	VIL	Input Low Voltage	–0.3	0.8	1.5	1.3	V	
	VIH	Input High Voltage	VCC –2.0	VCC +0.3	2.7	2.3	V	
	VOL	Output Low Voltage		0.40	0.2	0.15	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.7	4.1	V	IO = –1.0mA
	CI	Input Capacitance ③		8.0	5.0	5.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10.0	6.0	6.0	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300	170	200	ns	④
	TAVQV	Address Access Time		320	170	200	ns	④
	TELQX	Chip Enable Output Enable Time		100	40	50	ns	④
	TWLQZ	Write Enable Output Disable Time	20	100	40	50	ns	④
	TEHQZ	Chip Enable Output Disable Time		100	40	50	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		170	200	ns	④
	TEHEL	Chip Enable Pulse Positive Width	120		40	80	ns	④
	TAVEL	Address Setup Time	20		–10	0	ns	④
	TELAX	Address Hold Time	100		50	60	ns	④
	TWLWH	Write Enable Pulse Width	300		150	150	ns	④
	TWLEH	Write Enable Pulse Setup Time	300		150	150	ns	④
	TELWH	Write Enable Pulse Hold Time	300		150	150	ns	④
	TDVWH	Data Setup Time	200		100	120	ns	④
	TWHDZ	Data Hold Time	30		10	15	ns	④
	TWLDV	Write Data Delay Time	100		50	60	ns	④
	TWLEL	Early Output High-Z Time	0		–20	–15	ns	④
	TEHWH	Late Output High-Z Time	0		–20	–15	ns	④
	TELEL	Read or Write Cycle Time	420		210	280	ns	④

NOTES:
1. All devices guaranteed at worst case limits. Room temp., 5 volt data provided for information and not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Post Rad data at TD = 1 X 10^5.
3. Capacitance sampled and guaranteed – not 100% rested.
4. AC test Conditions: Inputs: TRISE = TFALL≤ 20nsec; Outputs: 1 TTL Load and 50pF. All timing measurements at 1/2 VCC.
5. Pre-Radiation and Post-Radiation limits.

Harris Semiconductor

CUSTOM/SEMICUSTOM

Read Cycle



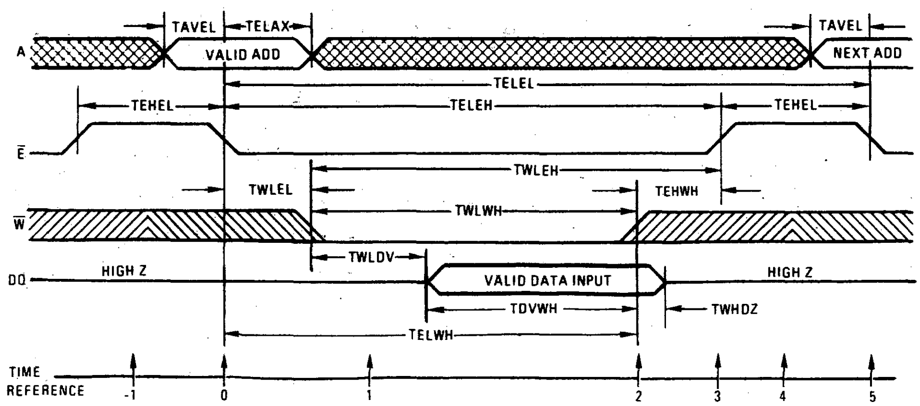
TRUTH TABLE

TIME REFERENCE	INPUTS E	W	A	DATA I/O DQ	FUNCTION
1	H	X	X	Z	MEMORY DISABLED
0	⌐_	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	OUTPUT ENABLED
2	L	H	X	V	OUTPUT VALID
3	_/	H	X	V	READ ACCOMPLISHED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	⌐_	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time the addresses may change state without affecting device operation. During time (T = 1) the outputs become enabled but data is not valid until time (T = 2).

$\overline{W}$ must remain high throughout the read cycle. After the data has been read $\overline{E}$ may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4). The memory is now ready for the next cycle.

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS E	W	A	DQ	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	⌐_	X	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	X	Z	WRITE PERIOD BEGINS
2	L	_/	X	V	DATA IN IS WRITTEN
3	_/	H	X	Z	WRITE COMPLETED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	⌐_	X	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The write cycle is initiated by the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on chip registers. There are two basic types of write cycles, which differ in the control of the common data-in/data-out bus.

Case 1: $\overline{E}$ falls before $\overline{W}$ falls

The output buffers may become enabled (reading) if $\overline{E}$ falls before $\overline{W}$ falls. $\overline{W}$ is used to disable (three-state) the outputs so input data can be applied. TWLDV must be met to allow the $\overline{W}$ signal time to disable the outputs before applying input data. Also, at the end of the cycle the outputs may become active if $\overline{W}$ rises before E. The RAM outputs will disable (three-state) after E rises (TEHQZ). In this type of write cycle TWLEL and TEHWH may be ignored.

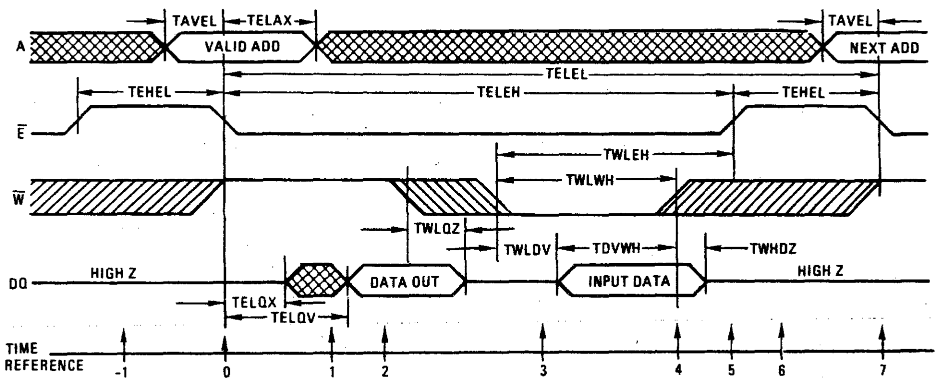
Case 2: $\overline{E}$ falls equal to or after $\overline{W}$ falls, and $\overline{E}$ rises before or equal to $\overline{W}$ rises.

This $\overline{E}$ and $\overline{W}$ control timing will guarantee that the data outputs will stay disabled throughout the cycle, thus simplifying the data input timing. TWLEL and TEHWH must be met but TWLDV becomes meaningless and can be ignored. In this cycle TDVWH and TWHDZ become TDVEH and TEHDZ. In other words, reference data setup and hold times to the $\overline{E}$ rising edge.

	IF	OBSERVE	IGNORE
Case 1	$\overline{E}$ falls before $\overline{W}$	TWLDV	TWLEL
Case 2	$\overline{E}$ falls after $\overline{W}$ & $\overline{E}$ rises before $\overline{W}$	TWLEL TEHWH	TWLDV TWHDV

If a series of consecutive write cycles are to be performed, $\overline{W}$ may be held low until all desired locations have been written (an extension of Case 2).

Read Modify Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	DATA I/O DQ	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↓	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	READ MODE, OUTPUT ENABLED
2	L	H	X	V	READ MODE, OUTPUT VALID
3	L	L	X	Z	WRITE MODE, OUTPUT HIGH Z
4	L	↑	X	V	WRITE MODE, DATA IS WRITTEN
5	↑	H	X	Z	WRITE COMPLETED
6	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
7	↓	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

If the pulse width of $\overline{W}$ is relatively short in relation to that of $\overline{E}$ a combination read-write cycle may be performed. If $\overline{W}$ remains high for the first part of the cycle, the outputs will become active during time (T = 1). Data out will be valid during time (T = 2). After the data is read, $\overline{W}$ can go low. After minumum TWLWH, $\overline{W}$ may return high. The information just written may now be read or $\overline{E}$ may return high, disabling the output buffers and preparing the device for the next cycle. Any number or sequence of read-write operations may be performed while $\overline{E}$ is low providing all timing requirements are met.

NOTES:

In the above descriptions the numbers in parenthesis (T = n) refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

Radiation Screening Procedure

(1) Two (2) probed good samples per wafer will be selected from ≥ 20% of the wafers in a run. (All wafers in a "run" will have been processed together through all high temperature processing steps and through metallization.)

(2) The sample die shall be assembled and tested to the production test program for proper operation.

(3) The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^5 Rad Si (± 10%) from a Gamma Cell 220 Cobalt 60 source or equivalent. The samples shall be biased at 5 volts with all inputs high. The dose rate shall be between 50 rads/sec and 200 rads/sec.

(4) The samples will be tested to the data sheet limits within one hour (±15 minutes) after irradiation. The lot will be accepted only if all units, exclusive of non-radiation failures, meet the data sheet limits.

Radiation Effects

The HS-6514RH is an RH memory designed to survive in a radiation environment and to meet the electrical characteristics and be pin compatible to the Harris equivalent commercial part. Latchup free operation, achieved by the use of special starting material and improved total dose hardness, is obtained with special high temperature processing cycles. These process techniques can, in principle, be applied to any standard HARRIS CMOS product.

On a production basis, HARRIS only performs screens for total dose hardness to a level of 1 x 10^5 rad-Si. Transient radiation tests, however, have shown the following results:

Latchup free to doses ≥ 5 x 10^{11} rads/sec.
Upset (loss of stored data) typically ≥ 10^8 rads/sec.

Test Product Flow

HARRIS SEMICONDUCTOR PRODUCT FLOW
MIL-STD-883, METHOD 5004 CLASS B

100% SCREENING PROCEDURE

	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1010 Cond. C
4	Constant Acceleration	2001 Cond. E; Y1 plane
5	Seal: A Fine B Gross	1014 Cond. A or B 1014 Cond. C2
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. @ 125°C (or equivalent) (Burn-In circuits enclosed)
8	Final Electrical 100% go-no-go	Tested at Worst Case Operating Conditions
9	External Visual	2009 Sample Inspection

Notes:

Traceability: All devices are assigned date code identification that provides traceability back to the inspection lot.

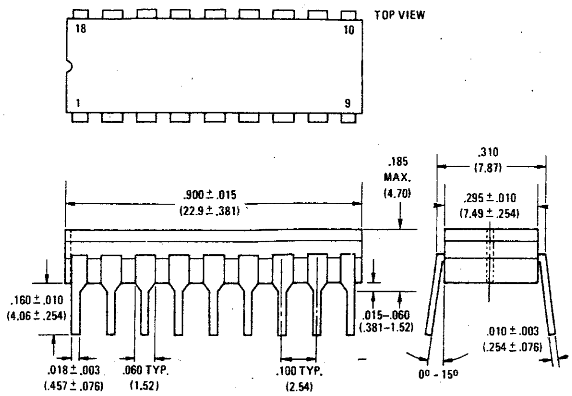
Branding: All devices are branded with the part number and EIA date code.

Aged Products: Product that has been held for more than 24 months will be reinspected prior to shipment to group A inspection requirements.

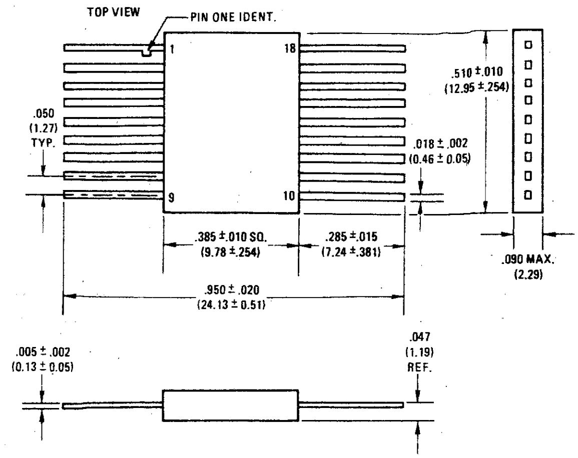
Additional Requirements: Sample Group A electrical tests are performed on a lot acceptance basis.

Packaging

18 LEAD CERAMIC DIP



18 LEAD CERPACK



1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ±.010 (± 0.25mm) unless otherwise shown.

Ordering Information

Example: HS 1 - 6514RH

- HS — HARRIS CUSTOM INTEGRATED CIRCUITS DIVISION
- 1 — PACKAGE
- 6514 — DEVICE
- RH — VERSION

PACKAGE

FLAT PACK	9-
CERDIP	1-

NOTICE: Harris Semiconductor's products are sold by description only. Harris Semiconductor reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly the reader is cautioned to verify that data sheets are current before placing orders.

Sales Offices

UNITED STATES

EASTERN REGION

2600 Virginia Avenue
Suite 800
Washington, DC 20037
(202) 342-3900
TWX: 710-822-9301

Five Old Concord Road
Burlington, MA 01803
(617) 273-1020
TWX: 710-332-1074

106 Seventh Street
Garden City, NY 11530
(516) 747-6776

WESTERN REGION

1503 South Coast Drive
Suite 320
Costa Mesa, CA 92626
(714) 957-6557
TWX: 910-595-1533

625 Ellis, Suite 300
Mt. View, CA 94043
(415) 964-6443
TWX: 910-379-6431

MIDWEST REGION

2850 Metro Dr., Suite 703
Minneapolis, MN 55420
(612) 854-3224
TWX: 910-576-3418

HOME OFFICE

P.O. Box 883
Melbourne, FL 32901
(305) 724-7045
TWX: 510-959-6259

EUROPEAN

Harris Systems Ltd.
Semiconductor Programs Division
P.O. Box 27
145 Farnham Road
Slough SL1 4XD
United Kingdom
Tel: 34666
TWX: 848174

HARRIS

CUSTOM INTEGRATED CIRCUITS DIVISION

HARRIS

HS-6551RH

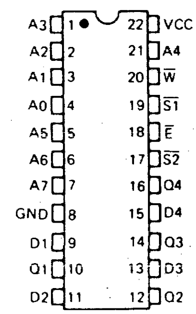
256 x 4 CMOS RAM

Features

• FUNCTIONAL TOTAL DOSE	2 x 10^4 RAD Si
• LATCH-UP FREE TO	5.0 x 10^{11} RAD Si/sec
• LOW STANDBY POWER	550µW MAX
• LOW OPERATING POWER	25mW/MHz MAX
• FAST ACCESS TIME	300ns MAX
• TTL COMPATIBLE IN/OUT	
• HIGH OUTPUT DRIVE - 1TTL LOAD	
• HIGH NOISE IMMUNITY	
• ON CHIP ADDRESS REGISTER	
• MILITARY TEMPERATURE RANGE	
• THREE-STATE OUTPUTS	
• 22 PIN PACKAGE FOR HIGH DENSITY	

Pinout

TOP VIEW



A – Address Input
Ē – Chip Enable
S̄ – Chip Select
W̄ – Write Enable
D – Data Input
Q – Data Output

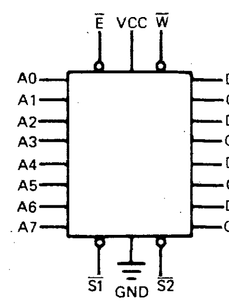
Description

The HS-6551RH is a 256 by 4 static CMOS RAM fabricated using the Harris Programs Division radiation hardened self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

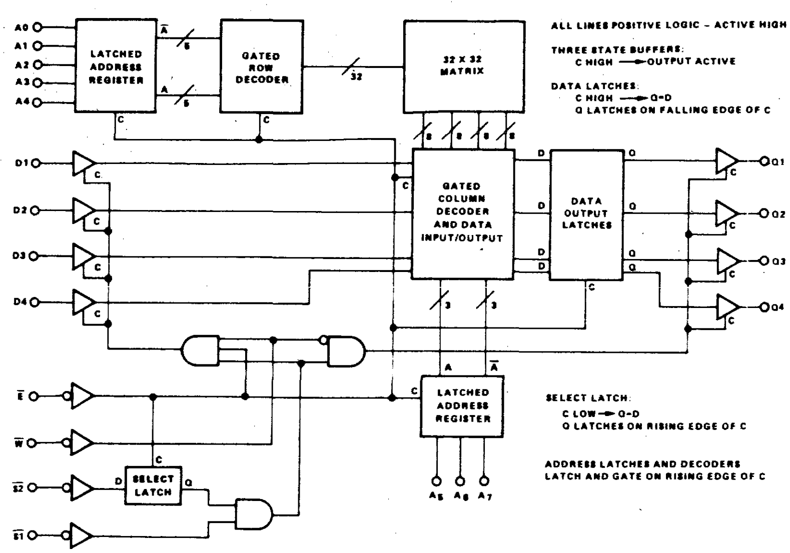
On-chip latches are provided for addresses, allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HS-6551RH is a fully static RAM and may be maintained in any state for an indefinite period of time.

Logic Symbol



Functional Diagram



Symbols and Abbreviations

This data sheet utilizes a new set of specification nomenclature. This new format is an IEEE and JEDEC supported standard for semiconductor memories. It is intended to clarify the symbols, abbreviations and definitions, and to make all memory data sheets consistent. We believe that, once acclimated, you will find this standardized format easy to read and use.

ELECTRICAL PARAMETER ABBREVIATIONS

All abbreviations use upper case letters with no subscripts. The initial symbol is one of these four characters:

V (Voltage)
I (Current)
P (Power)
C (Capacitance)

The second letter specifies input (I) or output (O), and the third letter indicates the high (H), low (L) or off (Z) state of the pin during measurements. Examples:

VIL — Input Low Voltage
IOZ — Output Leakage Current

TIMING PARAMETER ABBREVIATIONS

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:

T X X X X

Signal name from which interval is defined
Transition direction for first signal
Signal name to which interval is defined
Transition direction for second signal

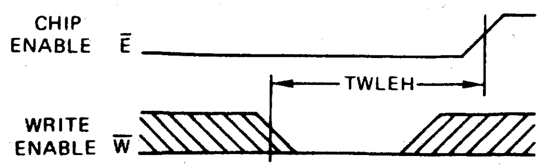
Signal Definitions:

A = Address
D = Data In
Q = Data Out
W = Write Enable
E = Chip Enable
S = Chip Select
G = Output Enable

Transition Definitions:

H = Transition to High
L = Transition to Low
V = Transition to Valid
X = Transition to Invalid or Don't Care
Z = Transition to Off (High Impedance)

EXAMPLE:

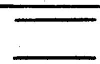
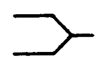


The example shows Write pulse setup time defined as TWLEH-Time from Write enable Low to chip Enable High.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set-up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	—	HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS

Supply Voltage -VCC	+7V
Applied Input or Output Voltage	GND -0.3V VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC	4.5V to 5.5V
Operating Temperature	-55°C to +125°C

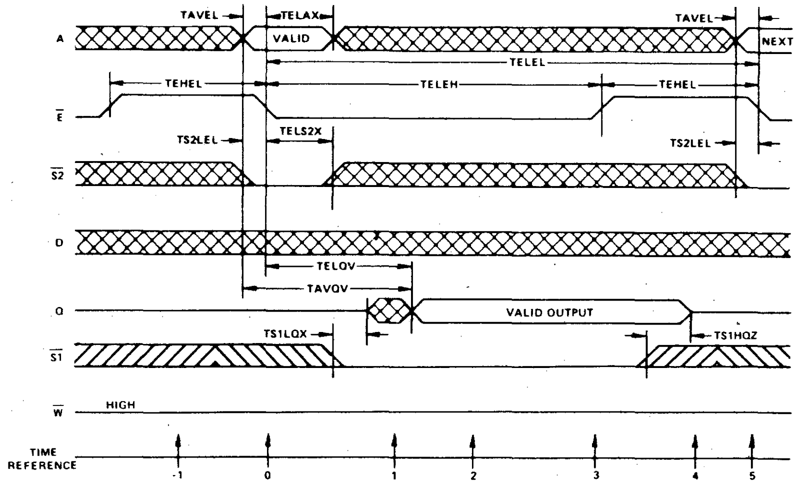
CAUTION: To prevent permanent damage to this device, care should be exercised to insure that the absolute maximum ratings for supply voltages, temperature and voltage or current at any pin is not exceeded during both static and dynamic operation.

ELECTRICAL CHARACTERISTICS ⑤

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100		10	100	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3		1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5		5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 2.0mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -1.0mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VI = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300		160	240	ns	④
	TAVQV	Address Access Time		300		150	240	ns	④
	TS1LQX	Chip Select 1 Output Enable Time		150		60	120	ns	④
	TWLQZ	Write Enable Output Disable Time		150		60	120	ns	④
	TS1HQZ	Chip Select 1 Output Disable Time		150		60	120	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		240	160		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		70	50		ns	④
	TAVEL	Address Setup Time	15		0	-10		ns	④
	TS2LEL	Chip Select 2 Setup Time	15		0	-10		ns	④
	TELAX	Address Hold Time	70		50	40		ns	④
	TELS2X	Chip Select 2 Hold Time	70		50	40		ns	④
	TDVWH	Data Setup Time	150		120	100		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLS1H	Chip Select 1 Write Pulse Setup Time	180		150	120		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	180		150	120		ns	④
	TS1LWH	Chip Select 1 Write Pulse Hold Time	180		150	120		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	180		150	120		ns	④
	TWLWH	Write Enable Pulse Width	180		150	120		ns	④
	TELEL	Read or Write Cycle Time	450		270	170		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC Test Conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – 1 TTL load and 50pF. All timing measurements at 1/2 VCC.
5. Pre-radiation characteristics, see radiation effects for Post-Radiation characteristics.

Read Cycle



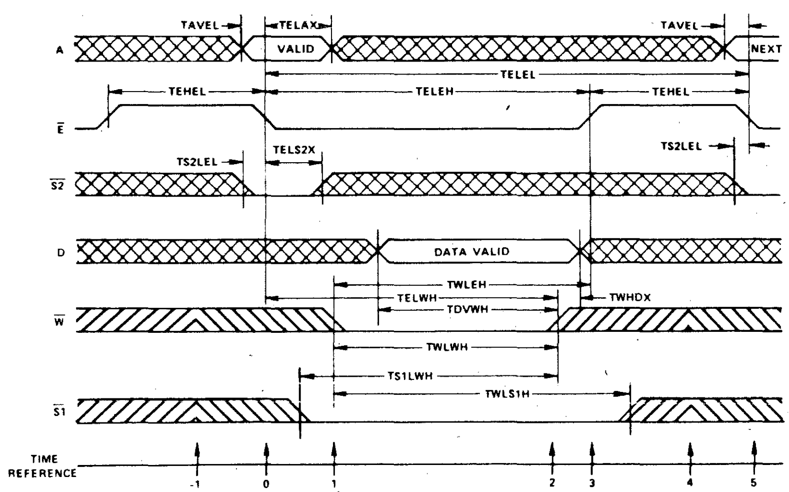
TRUTH TABLE

TIME REFERENCE	INPUTS E	S̅1	S̅2	W̅	A	D	OUTPUTS Q	FUNCTION
-1	H	H	X	X	X	X	Z	MEMORY DISABLED
0	↘	X	L	H	V	X	Z	ADDRESSES AND S̅2 ARE LATCHED, CYCLE BEGINS
1	L	L	X	H	X	X	X	OUTPUT ENABLED BUT UNDEFINED
2	L	L	X	H	X	X	V	DATA OUTPUT VALID
3	↗	L	X	H	X	X	V	OUTPUTS LATCHES, VALID DATA
4	H	H	X	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	L	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The HS-6551RH Read Cycle is initiated by the falling edge of E̅. This signal latches the input address word and S̅2 into on-chip registers providing that minimum setup and hold times are met. After the required hold time, these inputs may change state without affecting device operation. S̅2 acts as a higher order address and simplifies decoding. For the output to be read, E̅, S̅1 must be low and W̅ must be high. S̅2 must have been latched low on the falling edge of E̅. The output data will be valid at access time (TELQV).

The HS-6551RH has output data latches that are controlled by E̅. On the rising edge of E̅ the present data is latched and remains in that state until E̅ falls. Either or both S̅1 or S̅2 may be used to force the output buffers into a high impedance state.

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS						OUTPUTS	FUNCTION
	E	S1	S2	W	A	D	Q	
-1	H	H	X	X	X	X	Z	MEMORY DISABLED
0	↓	X	L	X	V	X	Z	CYCLE BEGINS, ADDRESSES AND $\overline{S2}$ ARE LATCHED
1	L	L	X	↓	X	X	Z	WRITE PERIOD BEGINS
2	L	L	X	↑	X	V	Z	DATA IN IS WRITTEN
3	↑	X	X	H	X	X	Z	WRITE IS COMPLETED
4	H	H	X	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↓	X	L	X	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

In the Write Cycle the falling edge of $\overline{E}$ latches the addresses and $\overline{S2}$ into on-chip registers. $\overline{S2}$ must be latched in the low state to enable the device. The write portion of the cycle is defined as $\overline{E}$, $\overline{W}$, $\overline{S1}$ being low and $\overline{S2}$ being latched low simultaneously. The $\overline{W}$ line may go low at any time during the cycle providing that the write pulse setup times (TWLEH and TWLS1H) are met. The write portion of the cycle is terminated on the first rising edge of either $\overline{E}$, $\overline{W}$, or $\overline{S1}$.

If a series of consecutive write cycles are to be executed, the $\overline{W}$ line may be held low until all desired locations have been written. If this method is used, data setup and hold times must be referenced to the first rising edge of $\overline{E}$ or $\overline{S1}$. By positioning the write pulse at different times within the $\overline{E}$ and $\overline{S1}$ low time (TELEH) various types of write cycles may be performed. If the $\overline{S1}$ low time (TS1LS1H) is greater than the $\overline{W}$ pulse plus an output enable time (TS1LQX), a combination read-write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

The HS-6551RH may be used on a common I/O bus structure by tying the input and output pins together. The multiplexing is accomplished internally by the $\overline{W}$ line. In the write cycle, when $\overline{W}$ goes low, the output buffers are forced to a high impedance state. One output disable time delay (TWLQZ) must be allowed before applying input data to the bus.

Radiation Screening Procedure

(1) Two (2) probed good samples per wafer will be selected from $\geq$20% of the wafers in a run. (All wafers in a "run" will have been processed together through all high temperature processing steps and through metallization.)

(2) The sample die shall be assembled and tested for functionality.

(3) The sample devices shall be subjected to a Total Dose Radiation level of 2 x 10^4 Rad Si (+10%) from a Gamma Cell 220 Cobalt 60 source or equivalent. The samples shall be biased at 5 volts with all inputs high. The dose rate shall be between 50 rads/sec and 200 rads/sec.

(4) I_{CCSB} at V_{CC} = 5 volts will be measured and recorded for each device within one hour ($\pm$15 minutes) after irradiation. The lot will be accepted only if the average of these measured values is $\leq$10mA.

Radiation Effects

The HS-6551RH is a radiation hardened memory processed with the same mask set as is used for HARRIS' equivalent commercial part. Latchup free operation is achieved by the use of special starting material and improved total dose hardness is obtained with special high temperature processing cycles. These process techniques can, in principal, be applied to any standard HARRIS CMOS product.

The primary failure mode under exposure to ionizing radiation is an increase in static leakage current (ICCSB). Functional failure due to the increased leakage currents will typically occur for dose levels in excess of 5 x 10^4 RAD-Si. AC and DC parameters other than ICC will change less than 10% for total dose levels under 5 x 10^4 RAD-Si. The excess leakage currents will anneal at room temperature and are typically reduced by a factor of 3-10 within 24 hours after irradiation.

On a production basis, HARRIS is able to perform screens only for total dose hardness. Transient radiation tests, however, have shown the following results:

Latchup free to doses $\geq$ 5 x 10^{11} rads/sec.
Upset (loss of stored data) typically $\geq$ 10^8 rads/sec.

HARRIS SEMICONDUCTOR PRODUCT FLOW
MIL-M-38510/MIL-STD-883, METHOD 5004 CLASS B

100% SCREENING PROCEDURE

	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1010 Cond. C
4	Constant Acceleration	2001 Cond. E; Y1 plane
5	Seal: Ⓐ Fine Ⓑ Gross	1014 Cond. A or B 1014 Cond. C2
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. @ 125°C (or equivalent)
8	Final Electrical 100% go-no-go	Tested at Worst Case Operating Conditions
9	External Visual	2009 Sample Inspection

Note:

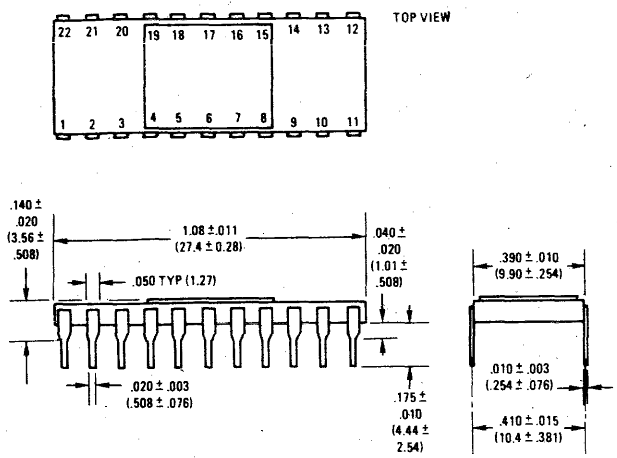
Traceability: All devices are assigned date code identification that provides traceability back to the inspection lot.

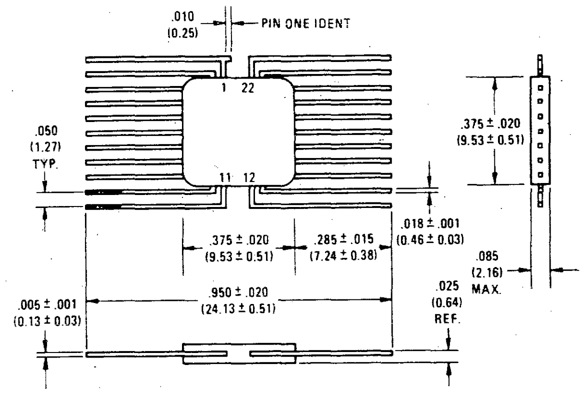
Branding: All devices are branded with the part number and EIA date code.

Aged Products: Product that has been held for more than 24 months will be reinspected prior to shipment to group A inspection requirements.

Additional Requirements: Sample Group A electrical tests are performed on a lot acceptance basis.

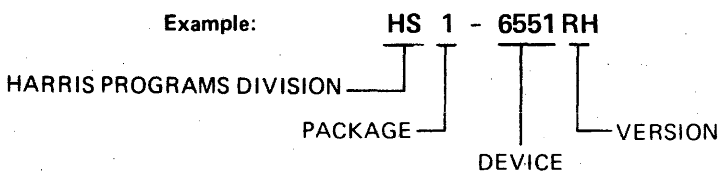
Packaging





1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ± .010 (± 0.25mm) unless otherwise shown.

Ordering Information



PACKAGE

FLAT PACK	9-
CERDIP	1-

NOTICE: Harris Semiconductor's products are sold by description only. Harris Semiconductor reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders.

HARRIS

HS-6564RH

Radiation Resistant

8K x 8, 16K x 4 CMOS RAM

Preliminary

Features

- LOW POWER STANDBY — 500µW MAX
- LOW POWER OPERATION — 180mW/MHz MAX
- DATA RETENTION — 3.0 V MIN
- TTL COMPATIBLE IN/OUT
- THREE STATE OUTPUTS
- FAST ACCESS TIME — 250 nsec TYP.
- MILITARY TEMPERATURE RANGE — -55°C TO +125°C
- ON CHIP ADDRESS REGISTERS
- ORGANIZABLE 8K×8 OR 16K×4
- 40 PIN DIP PINOUT 2.000″ × 0.900″
- FUNCTIONAL TOTAL DOSE — 1×10^5 RAD Si
- DATA UPSET — $>10^8$ RAD Si/SEC
- LATCH-UP FREE TO — $>5\times10^{11}$ RAD Si/SEC

Description

The HS-6564RH is a radiation resistant 64K bit, synchronous CMOS RAM. It consists of 16 HS-6504RH 4K×1 radiation resistant CMOS RAMs, in leadless carriers, mounted on a ceramic substrate. The HS-6564RH is configured as an extra wide, standard length 40 pin DIP. The memory appears to the system as an array of 16 4K×1 static RAMs. The array is organized as two 8K by 4 blocks of RAM sharing only the address bus. The data inputs, data outputs, chip enables and write enables are separate for each block of RAM. This allows the user to organize the HS-6564RH RAM as either an 8K by 8 or a 16K by 4 array.

This 64K memory provides a unique blend of low power CMOS semiconductor technology and advanced packaging techniques. The HS-6564RH is intended for use in radiation environments where a large amount of RAM is needed, and where power consumption and board space are prime concerns. On-chip latches are provided for addresses, data input and data output allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance for use in expanded memory arrays. The guaranteed low voltage data retention characteristics allow easy implementation of non-volatile read/write memory by using very small batteries mounted directly on the memory circuit board.

Pinout

TOP VIEW

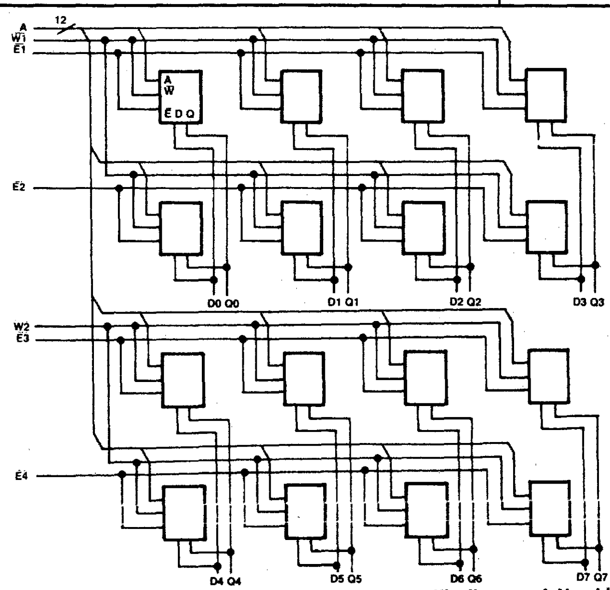
Signal	Pin	Pin	Signal
*GND	1	40	VCC*
Q4	2	39	Q0
D4	3	38	D0
Q5	4	37	Q1
D5	5	36	D1
A0	6	35	A6
A1	7	34	A7
A4	8	33	A8
$\overline{E}3$	9	32	$\overline{E}1$
*$\overline{W}2$	10	31	$\overline{W}1$
$\overline{W}2$	11	30	$\overline{W}1$*
$\overline{E}4$	12	29	$\overline{E}2$
A11	13	28	A3
A10	14	27	A2
A9	15	26	A5
D6	16	25	D2
Q6	17	24	Q2
D7	18	23	D3
Q7	19	22	Q3
*VCC	20	21	GND*

***NOTES:**

Pins 20 and 40 (VCC) are internally connected. Similarly pins 1 and 21 (Ground) are connected. The user is advised to connect all four VCC pins and Ground pins to his board busses. This will improve power distribution across the array and will enhance decoupling.

Pin 10 is internally connected to pin 11, and pin 30 is connected to pin 31. For those users wishing to preserve board compatibility with possible future RAM arrays, we recommend connections to the write lines be made at pins 11 and 31, leaving pins 10 and 30 free for future expansion.

Functional Diagram



Information on this device is preliminary. Data is subject to change unless otherwise specifically agreed. No obligations are assumed for notice of change or future manufacture of this device.

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

Harris Semiconductor

CUSTOM/SEMICUSTOM

Symbols and Abbreviations

This data sheet utilizes a new set of specification nomenclature. This new format is an IEEE and JEDEC supported standard for semiconductor memories. It is intended to clarify the symbols, abbreviations and definitions, and to make all memory data sheets consistent. We believe that, once acclimated, you will find this standardized format easy to read and use.

ELECTRICAL PARAMETER ABBREVIATIONS

All abbreviations use upper case letters with no subscripts. The initial symbol is one of these four characters:

V (Voltage)
I (Current)
P (Power)
C (Capacitance)

The second letter specifies input (I) or output (O), and the third letter indicates the high (H), low (L) or off (Z) state of the pin during measurements. Examples:

VIL – Input Low Voltage
IOZ – Output Leakage Current

TIMING PARAMETER ABBREVIATIONS

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:

T X X X X
Signal name from which interval is defined (1st X)
Transition direction for first signal (2nd X)
Signal name to which interval is defined (3rd X)
Transition direction for second signal (4th X)

Signal Definitions:

A = Address
D = Data In
Q = Data Out
W = Write Enable
E = Chip Enable
S = Chip Select
G = Output Enable

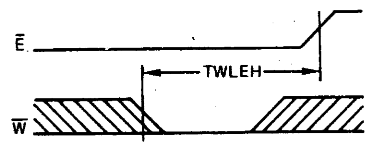
Transition Definitions:

H = Transition to High
L = Transition to Low
V = Transition to Valid
X = Transition to Invalid or Don't Care
Z = Transition to Off (High Impedance)

EXAMPLE:

CHIP ENABLE

WRITE ENABLE

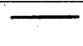
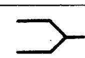


The example shows Write pulse setup time defined as TWLEH-Time from Write enable Low to chip Enable High.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set-up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	—	HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage – (VCC – GND)	−0.3V to +7.0V
Input or Output Voltage Applied	(GND −0.3V) to (VCC +0.3V)
Storage Temperature	−65°C to +150°C

OPERATING RANGE

Operating Supply Voltage	+4.5 to +5.5V
Operating Temperature	−55°C to +125°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS ④

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	TYPICAL TEMP. = 25°C ① VCC = 5.0V PRE RAD	POST RAD	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		800	80	80	μA	IO = 0 VI = VCC or GND
	ICCOP1	Operating Supply Current (8K × 8) ②		56	36		mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCOP2	Operating Supply Current (16K × 4) ②		28	18		mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		600	48	48	μA	IO = 0, VCC = 3.0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	3.0		2.6	1.8	V	
	IIA	Address Input Leakage	−20	+20			μA	GND≤VI≤VCC
	IID1	Data Input Leakage (8K × 8)	−3	+3			μA	GND≤VI≤VCC
	IID2	Data Input Leakage (16K × 4)	−5	+5			μA	GND≤VI≤VCC
	IIE1	Enable Input Leakage (8K × 8)	−10	+10			μA	GND≤VI≤VCC
	IIE2	Enable Input Leakage (16K × 4)	−5	+5			μA	GND≤VI≤VCC
	IIW	Write Enable Input Leakage (Each)	−10	+10			μA	GND≤VI≤VCC
	IOZ1	Output Leakage (8K × 8)	−20	+20	±4	±4	μA	GND≤VO≤VCC
	IOZ2	Output Leakage (16K × 4)	−40	+40	±8	±8	μA	GND≤VO≤VCC
	VIL	Input Low Voltage	−0.3	0.8	1.5	1.3	V	
	VIH1	Input High Level (Except $\overline{E}$ and $\overline{W}$)	VCC −1.5	VCC +0.3	2.7	2.5	V	
	VIH2	Input High Level ($\overline{E}$ and $\overline{W}$)	VCC −1.0	VCC +0.3	2.9	2.1	V	
	VOL	Output Low Voltage		0.4	0.2	0.15	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.6	4.0	V	IO = −1.0mA
	CIA	Address Input Capacitance ③		200			pF	f = 1MHz, VI = VCC or GND
	CID1	Data Input Capacitance (8K × 8) ③		50			pF	f = 1MHz, VI = VCC or GND
	CID2	Data Input Capacitance (16K × 4) ③		100			pF	f = 1MHz, VI = VCC or GND
	CIE1	Enable Input Capacitance (8K × 8) ③		160			pF	f = 1MHz, VI = VCC or GND
	CIE2	Enable Input Capacitance (16K × 4) ③		80			pF	f = 1MHz, VI = VCC or GND
	CIW	Write Enable Input Capacitance (Each) ③		100			pF	f = 1MHz, VI = VCC or GND
	CO1	Output Capacitance (8K × 8) ③		50			pF	f = 1MHz, VO = VCC or GND
	CO2	Output Capacitance (16K × 4) ③		100			pF	f = 1MHz, VO = VCC or GND

NOTES:

① Each individual RAM in the leadless carrier is fully tested at worst case limits of temperature and voltage. The complete assembled HS-6564RH array is tested at room temperature only. The worst case parameters are guaranteed over the specified temperature and voltage ranges. Room temperature, 5 volt data is provided for information purposes and is not guaranteed.

② Operating supply current is proportional to operating frequency. ICCOP is specified at an operating frequency of 1MHz, indicating repetive accessing at a 1μs rate. Operation at slower rates will decrease ICCOP proportionally.

③ Capacitance sampled and guaranteed – not 100% tested.

④ Pre Radiation and Post Radiation limits.

ELECTRICAL CHARACTERISTICS

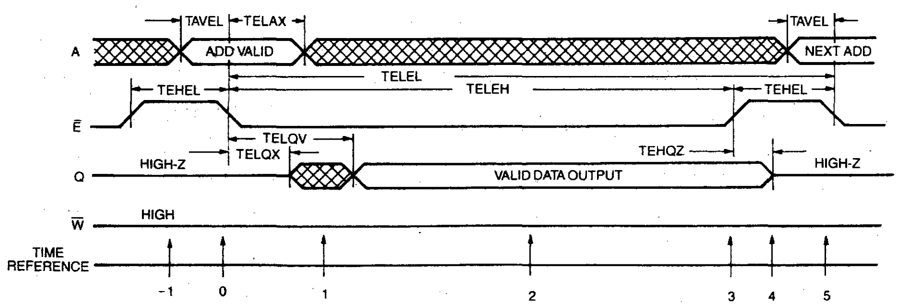
	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	TYPICAL TEMP. = 25°C VCC = 5.0V PRE RAD	POST RAD	UNITS	TEST CONDITIONS
A.C.	TELQV	Chip Enable Access		350	200	230	ns	(5)
	TAVQV	Address Access (TAVQV=TELQV+TAVEL)		400	220	260	ns	
	TELQX	Output Enable	20	120	70	80	ns	
	TEHQZ	Output Disable		130	80	90	ns	
	TELEL	Read or Write Cycle	480		250	320	ns	
	TELEH	Chip Enable Low	350		200	230	ns	
	TEHEL	Chip Enable High	130		50	90	ns	
	TAVEL	Address Setup	50		20	30	ns	
	TELAX	Address Hold	50		30	35	ns	
	TWLWH	Write Enable Low	150		90	100	ns	
	TWLEH	Write Enable Setup	250		190	190	ns	
	TWLEL	Early Write Setup (Write Mode)	10		−5	0	ns	
	TWHEL	Write Enable Read Setup	10		−5	0	ns	
	TELWX	Early Write Hold (Write Mode)	100				ns	
	TDVWL	Data Setup	10		−5	20	ns	
	TDVEL	Early Write Data Setup	10		−5	20	ns	
	TWLDX	Data Hold	100		70	80	ns	
	TELDX	Early Write Data Hold	100		70	80	ns	
	TQVWL	Data Valid to Write (Read-Modify-Write)	0		0	0	ns	(5)

NOTES:

(5) AC Test Conditions:

Inputs – Trise = Tfall ≤ 20ns.
Outputs – CLOAD = 100pF.
Timing measured at 1.5V reference level.

Read Cycle

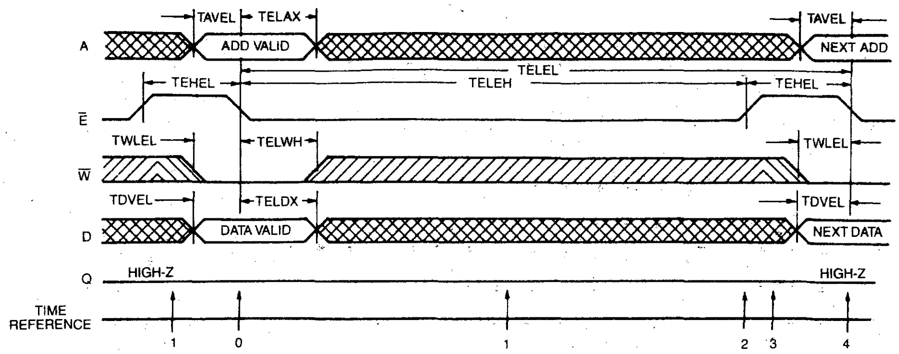


TRUTH TABLE

TIME REFERENCE	INPUTS E	W	A	OUTPUT Q	FUNCTION
−1	H	X	X	Z	MEMORY DISABLED
0	↓	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	OUTPUT ENABLED
2	L	H	X	V	OUTPUT VALID
3	↑	H	X	V	READ ACCOMPLISHED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS −1)
5	↓	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of E (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until during time (T = 2). W must remain high until after time (T = 2). After the output data has been read, E may return high (T = 3). This will disable the output buffer and ready the RAM for the next memory cycle (T = 4).

Early Write Cycle

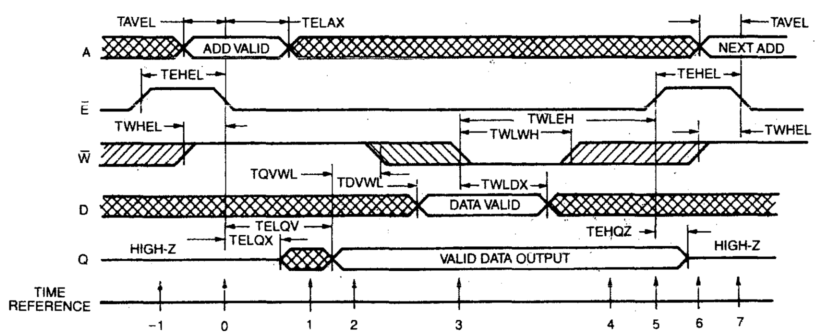


TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	D	OUTPUT Q	FUNCTION
−1	H	X	X	X	Z	MEMORY DISABLED
0	↘	L	V	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	X	X	X	Z	WRITE IN PROGRESS INTERNALLY
2	↗	X	X	X	Z	WRITE COMPLETED
3	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS −1)
4	↘	L	V	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The early write cycle is the only cycle where the output is guaranteed not to become active. On the falling edge of Ē (T = 0), the addresses, the write signal, and the data input are latched in on chip registers. The logic value of W̄ at the time Ē falls determines the state of the output buffer for that cycle. Since W̄ is low when Ē falls, the output buffer is latched into the high impedance state and will remain in that state until Ē returns high (T = 2). For this cycle, the data input is latched by Ē going low; therefore data set up and hold times should be referenced to Ē. When Ē (T = 2) returns to the high state, the output buffer disables and all signals are unlatched. The device is now ready for the next cycle.

Read Modify Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	D	OUTPUT Q	FUNCTION
−1	H	X	X	X	Z	MEMORY DISABLED
0	↘	H	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	X	OUTPUT ENABLED
2	L	H	X	X	V	OUTPUT VALID, READ AND MODIFY TIME
3	L	↘	X	V	V	WRITE BEGINS, DATA IS LATCHED
4	L	X	X	X	V	WRITE IN PROGRESS INTERNALLY
5	↗	X	X	X	V	WRITE COMPLETED
6	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS −1)
7	↘	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The read modify write cycle begins as all other cycles on the falling edge of Ē (T = 0). The W̄ line should be high at (T = 0) in order to latch the output buffers in the active state. During (T = 1) the output will be active but not valid until (T = 2). On the falling edge of the W̄ (T = 3) the data present at the output and input are latched. The W̄ signal also latches itself on its low going edge. All input signals excluding Ē have been latched and have no further effect on the RAM. The rising edge of Ē (T = 5) completes the write portion of the cycle and unlatches all inputs and output. The output goes to a high impedance and the RAM is ready for the next cycle.

NOTES: In the above descriptions the numbers in parenthesis (T = n) refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

Board Size Tradeoffs

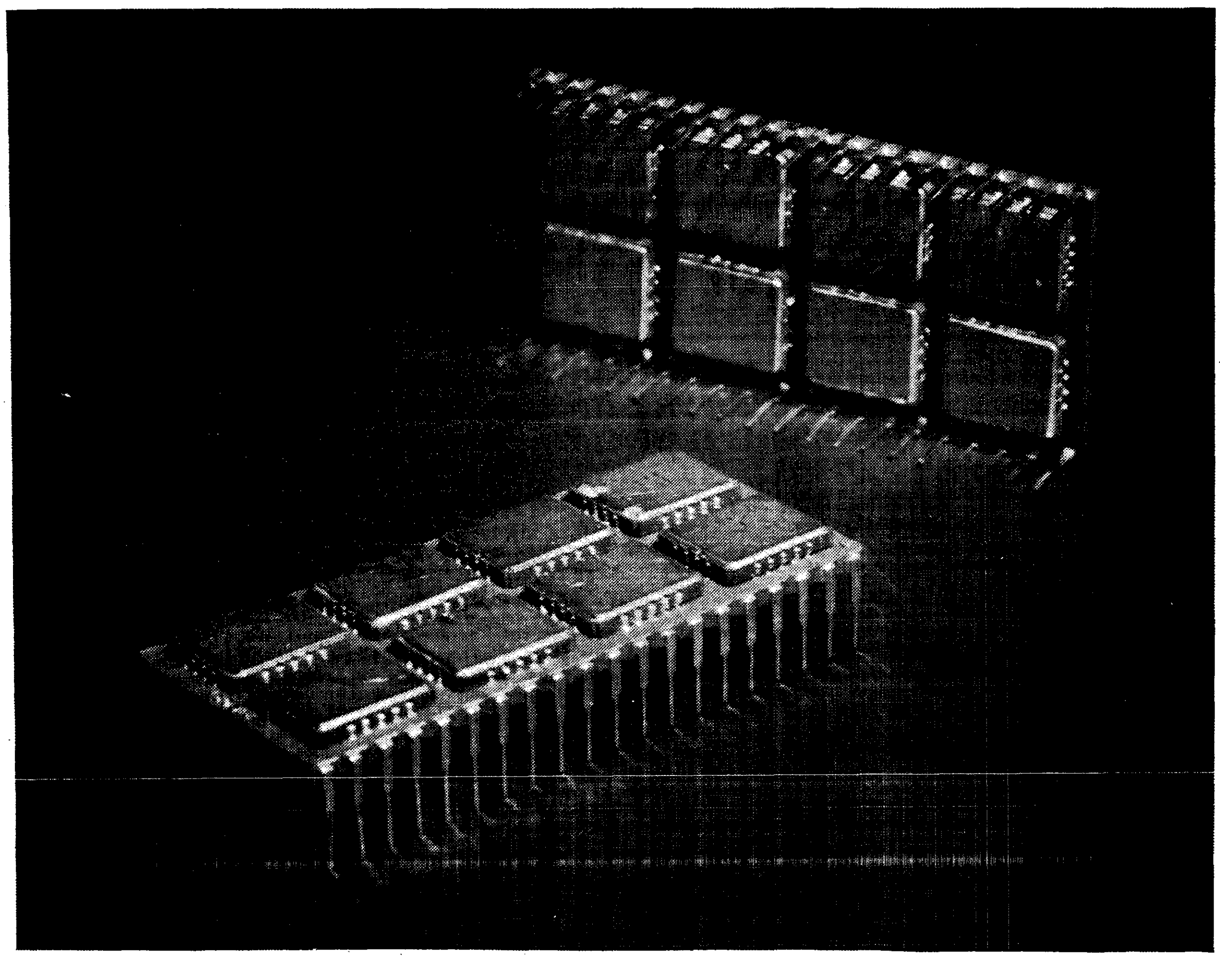
Printed circuit board real estate is a costly commodity. Actual board costs depend on layout tolerances, density, complexity, number of layers, choice of board material, and other factors.

The following table compares board space for 16 standard DIP 4K RAMs to the HS-6564RH RAM array. Both fine line, close tolerance layout and standard "easy" layout board sizes are shown in the comparison.

64K ARRAY OF 16 4K RAMs ON A PC BOARD V.S. THE HS-6564RH

PACKAGE	CIRCUIT SUBSTRATE	SIZE
18 Pin DIP	Standard Two Sided PCB	12 to 15 sq. in.
18 Pin DIP	Fine Line or Multilayer PCB	9 to 11 sq. in.
18 Pin Leadless Carrier	Multilayer Alumina Substrate	3 to 5 sq. in.
HS-6564RH	Two Sided Mounting Multilayer Alumina Substrate	2 sq. in.

The cost of semiconductor circuits decline with time. If actual costs were included, they would be out of date in a very short time. We urge you to contact your local Harris office or sales representative for accurate pricing allowing cost tradeoff analysis. In your cost analysis, also consider the advantages of a lighter, smaller overall package for your system. Consider how much more valuable your system will be when the memory array size is decreased to about 1/6 of normal size.



HS-6564RH – 64K BIT CMOS RAM

To Organize 8K × 8:
Connect: $\overline{E}1$ with $\overline{E}3$ (Pin
$\overline{E}2$ with $\overline{E}4$ (Pin
$\overline{W}1$ with $\overline{W}2$ (Pin

Concerns for Proper Operation of Chip

The transition between blocks of RAM requ
the chip enables as if there were only two, E
between chip enables must be treated with
high at least one chip enable high time (TEH
devices whose outputs are tied common e

Printed Circuit Board Mounting:

The leadless chip carrier packages used in
to VCC or GND. The designer should be aw
pressed completely down against the surfa
help prevent the leadless carriers from tou

HARRIS CMOS RAMs are designe
guaranteed over temperature. The fo

1. Chip Enable ($\overline{E}$) must be he
2. All other inputs should be h
3. Inputs which are to be held h
up and power down transitio
4. The RAM can begin operat

VCC

$\overline{E}$

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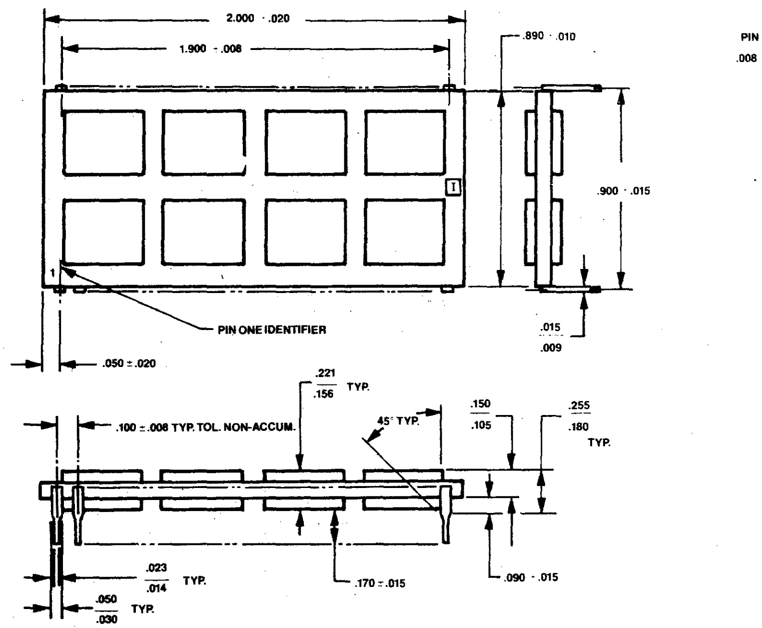

NOTES:

1. ALL E
BE G
MIN.
2. FLAT
3. DIE A
CONI

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NOTICE: Harris Semiconductor's products are sold by description only. Harris Semiconduc and/or specifications at any time without notice. Accordingly the reader is cautioned to veri

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EASTERN REGION

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Suite 800
Washington, DC 20037
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CUSTOM INTEGRATED CIRCUITS I

Board Size Tradeoffs

Printed circuit board real estate is a costly commodity. Actual board costs depend on layout tolerances, density, complexity, number of layers, choice of board material, and other factors.

The following table compares board space for 16 standard DIP 4K RAMs to the HS-6564RH RAM array. Both fine line, close tolerance layout and standard "easy" layout board sizes are shown in the comparison.

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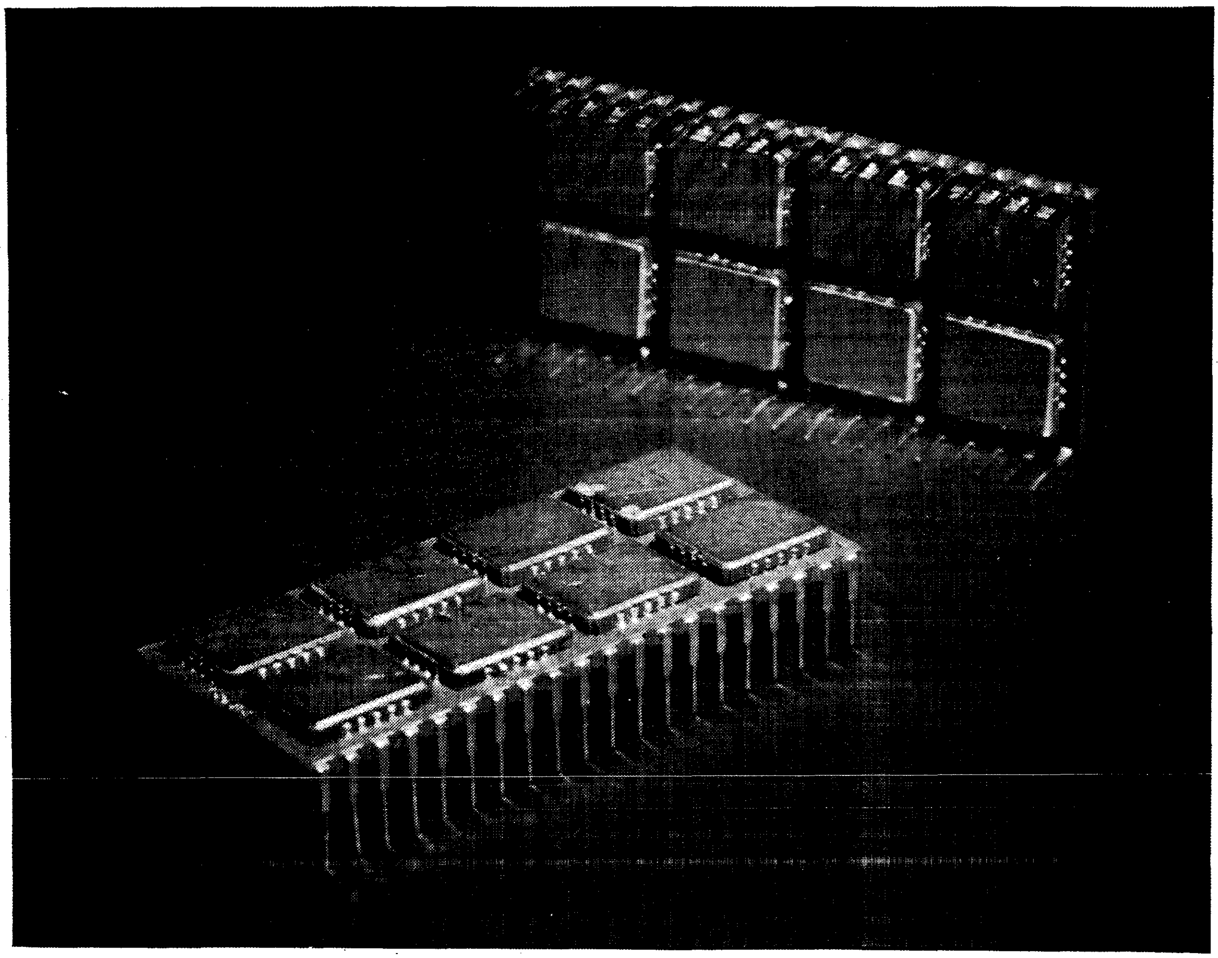
The cost of semiconductor circuits decline with time. If actual costs were included, they would be out of date in a very short time. We urge you to contact your local Harris office or sales representative for accurate pricing allowing cost tradeoff analysis. In your cost analysis, also consider the advantages of a lighter, smaller overall package for your system. Consider how much more valuable your system will be when the memory array size is decreased to about 1/6 of normal size.



HS-6564RH – 64K BIT CMOS RAM

Organization Guide

To Organize 8K × 8:		To Organize 16K × 4:	
Connect: $\overline{E}$1 with $\overline{E}$3	(Pins 9 + 32)	Connect: Q0 with Q4	(Pins 2 + 39)
$\overline{E}$2 with $\overline{E}$4	(Pins 12 + 29)	D0 with D4	(Pins 3 + 38)
$\overline{W}$1 with $\overline{W}$2	(Pins 11 + 31)	Q1 with Q5	(Pins 4 + 37)
		D1 with D5	(Pins 5 + 36)
		D2 with D6	(Pins 16 + 25)
		Q2 with Q6	(Pins 17 + 24)
		D3 with D7	(Pins 18 + 23)
		Q3 with Q7	(Pins 19 + 22)
		Optional $\overline{W}$1 may be common with $\overline{W}$2	(Pins 11 + 31)

Concerns for Proper Operation of Chip Enables:

The transition between blocks of RAM requires a change in the chip enable being used. When operating in the 8K × 8 mode, use the chip enables as if there were only two, $\overline{E}$1 and $\overline{E}$2. In the 16K × 4 mode, all chip enables must be treated separately. Transitions between chip enables must be treated with the same timing constraints that apply to any one chip enable. All chip enables must be high at least one chip enable high time (TEHEL) before any chip enable can fall. More than one chip enable low simultaneously, for devices whose outputs are tied common either internally or externally, is an illegal input condition and must be avoided.

Printed Circuit Board Mounting:

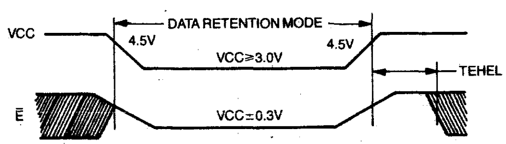
The leadless chip carrier packages used in the HS-6564RH have conductive lids. These lids are electrically floating, not connected to VCC or GND. The designer should be aware of the possibility that the carriers on the bottom side could short conductors below if pressed completely down against the surface of the circuit board. The pins on the package are designed with a standoff feature to help prevent the leadless carriers from touching the circuit board surface.

Low Voltage Data Retention

HARRIS CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC + 0.3V to VCC − 0.3V.
2. All other inputs should be held either high (at CMOS VCC) or at ground to minimize ICCDR.
3. Inputs which are to be held high (e.g. $\overline{E}$) must be kept between VCC + 0.3V and 70% of VCC during the power up and power down transitions.
4. The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING



Radiation Screening Procedure

(1) Two (2) probed good samples per wafer will be selected from ≥ 20% of the wafers in a run. (All wafers in a "run" will have been processed together through all high temperature processing steps and through metal-lization.)

(2) The sample die shall be assembled and tested for functionality.

(3) The sample devices shall be subjected to a Total Dose Radiation level of 1×10^5 Rad Si (± 10%) from a Gamma Cell 220 Cobalt 60 source or equivalent. The samples shall be biased at 5 volts with all inputs high. The dose rate shall be between 50 rads/sec and 200 rads/sec.

(4) The samples will be tested to the data sheet limits within one hour (± 15 minutes) after irradiation. The lot will be accepted only if all units, exclusive of non-radiation failures, meet the data sheet limits.

Radiation Effects

The HS-6564RH is a radiation resistant memory module designed to survive in a radiation environment and to meet the electrical characteristics and be pin compatible to the Harris equivalent commercial part. Latchup free operation, achieved by the use of special starting material and improved total dose hardness, is obtained with special high temperature processing cycles. These process techniques can, in principle, be applied to any standard HARRIS CMOS product.

On a production basis, HARRIS only performs screens for total dose hardness to a level of 1×10^5 rad-Si. Transient radiation tests, however, have shown the following results:

Latchup free to doses $\geq 5 \times 10^{11}$ rads/sec.
Upset (loss of stored data) typically $\geq 10^8$ rads/sec.

Test Product Flow

HARRIS SEMICONDUCTOR PRODUCT FLOW
MIL-STD-883, METHOD 5004 CLASS B

100% SCREENING PROCEDURE*

	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1010 Cond. C
4	Constant Acceleration	2001 Cond. E; Y1 plane
5	Seal: Fine Gross	1014 Cond. A or B 1014 Cond. C2
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. @ 125°C (or equivalent)
8	Final Electrical 100% go-no-go	Tested at Worst Case Operating Conditions
9	External Visual	2009 Sample Inspection

*** ALL SCREENING IS PERFORMED AT LEADLESS CARRIER LEVEL EXCEPT FINAL ELECTRICAL**

NOTE:

Traceability: All devices are assigned date code identification that provides traceability back to the inspection lot.

Branding: All devices are branded with the part number and EIA date code.

Aged Products: Product that has been held for more than 24 months will be reinspected prior to shipment to group A inspection requirements.

Additional Requirements: Sample Group A electrical tests are performed on a lot acceptance basis.

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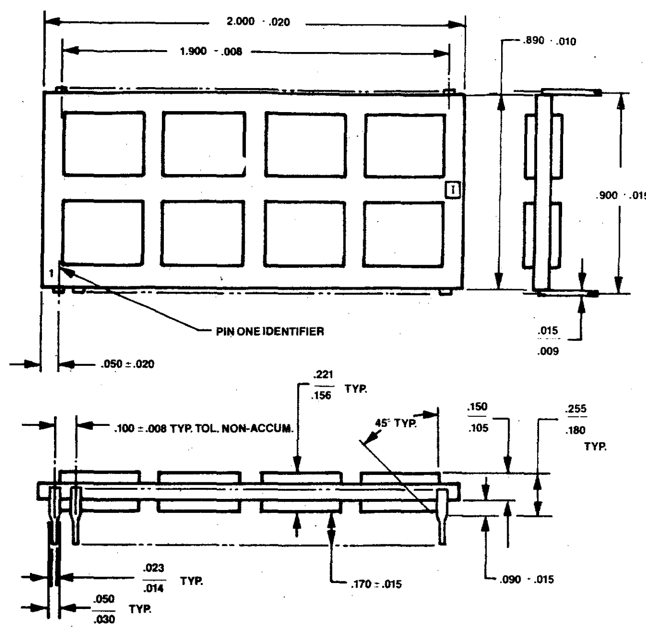
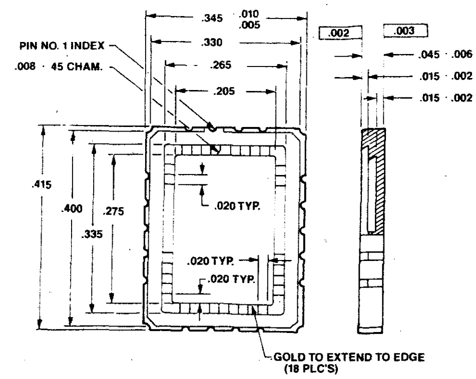
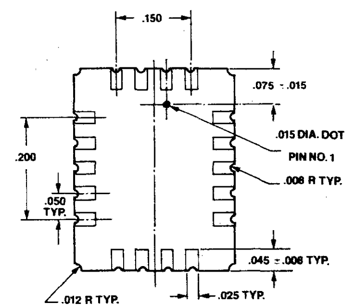
Packaging







NOTES:
1. ALL EXPOSED METALLIZED AREAS SHALL BE GOLD PLATED 50 MICRO INCHES MIN. THICKNESS OVER NICKEL PLATE.
2. FLATNESS PERTAINS TO METALLIZED PADS ONLY.
3. DIE ATTACH PAD TO BE ELECTRICALLY CONNECTED TO PIN NO. 18.

Sales Offices

UNITED STATES

EASTERN REGION

2600 Virginia Avenue
Suite 800
Washington, DC 20037
(202) 342-3900
TWX: 710-822-9301

Five Old Concord Road
Burlington, MA 01803
(617) 273-1020
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TWX: 910-576-3418

HOME OFFICE

P.O. Box 883
Melbourne, FL 32901
(305) 724-7045
TWX: 510-959-6259

EUROPEAN

Harris Systems Ltd.
Semiconductor Programs Division
P.O. Box 27
145 Farnham Road
Slough SL1 4XD
United Kingdom
Tel: 34666
TWX: 848174

HARRIS

CUSTOM INTEGRATED CIRCUITS DIVISION

HS-3516RH

High Slew Rate, Wideband, Radiation Resistant, Operational Amplifier

HARRIS

Preliminary

Features

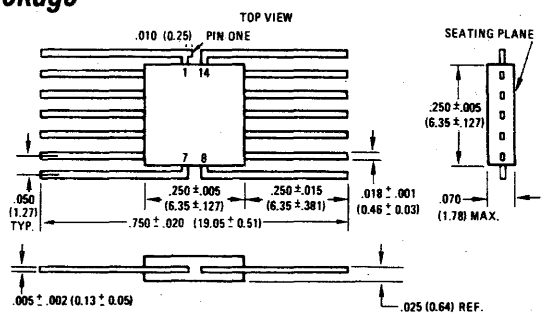
- HIGH SLEW RATE . . . . >±22V/µs
- FAST SETTLING TIME 450ns
- WIDE POWER BANDWIDTH. 12MHz
- LOW OFFSET VOLTAGE. . . . . ±5mV
- LOW POWER SUPPLY CURRENT 6.5mA
- SHORT CIRCUIT PROTECTION
- RADIATION ENVIRONMENT
  - NEUTRON FLUENCE (ϕ) 5×10^{12} n/cm^2 (E≥10KeV)
  - GAMMA RATE ($\dot{\gamma}$) . . . . . 1×10^9 RADs Si/s
  - GAMMA DOSE (γ) . . . . . . 1×10^6 RADs Si

Description

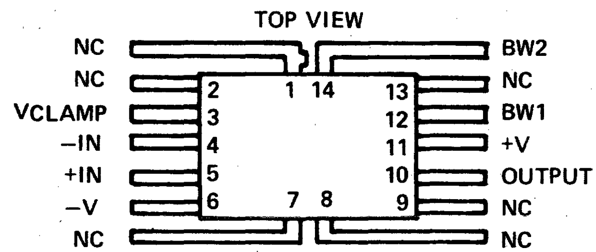
The HS-3516RH is a monolithic, high slew rate, wideband, radiation resistant, operational amplifier. It provides a bandwidth (unity gain stable) of greater than 10MHz and a slew rate in excess of 22V/µsec. Optional frequency compensation adjustment is provided. The HS-3516RH has an internal unity gain frequency compensation capacitor which is internally connected. A clamp node feature enables the user to clamp the output voltage via pin 3 which can source or sink up to 3mA for high frequency clamped switching purposes.

This device is designed to operate from −55°C to +125°C and in strategic-level radiation environments.

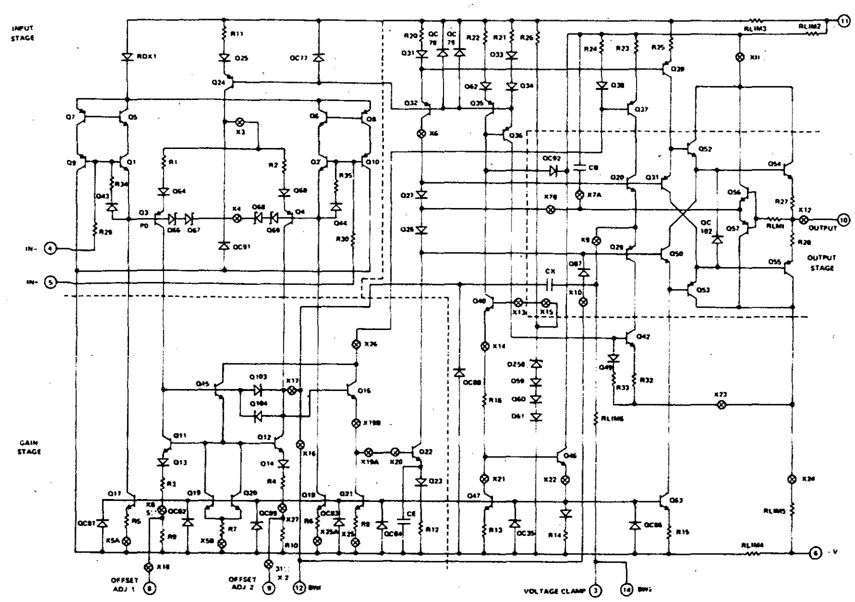
Package



Pinout



Schematic



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ABSOLUTE MAXIMUM RATINGS

Voltage Between +V and −V terminals	40V	Internal Power Dissipation	625mW
Differential Input Voltage	±15V	Storage Temperature Range	−65°C to +175°C
Output Short Circuit Duration	Indefinite	Operating Temperature Range	−55°C to +125°C

CAUTION: To prevent permanent damage to this device, care should be exercised to insure that the absolute maximum ratings for supply voltages, temperature and voltage or current at any pin is not exceeded during both static and dynamic operation.

ELECTRICAL CHARACTERISTICS +V = 15V, −V = −15V, T_A = −55°C to +125°C

PARAMETER	TEMP	MIN	TYP	MAX	UNITS
Offset Voltage	25°C 125°C −55°C		1 2 3	3 5 6	mV mV mV
Input Bias Current	25°C 125°C −55°C		35 50	100 100 200	nA nA nA
Input Offset Current	25°C 125°C −55°C		30	100 150 250	nA nA nA
Input Resistance	25°C		>100		MΩ
Large Signal Voltage Gain[1]	25°C Full	90 90			dB dB
Common Mode Rejection Ratio[2]	25°C Full	80 80	115 90		dB dB
Supply Current	25°C 125°C −55°C		5.0	6.5 6.5 8.7	mA mA mA
Power Supply Rejection Ratio[3]	25°C Full	80 80			dB dB
Output Voltage Swing	25°C 125°C −55°C 	+12.5 −11.0 +12.5 −11.0 +12.0 −11.0	+13.0 −12.0 +13.0 −12.0		V V V V V V
Output Short Circuit Current	25°C 125°C −55°C		27	45 45 60	mA mA mA
Gain Bandwidth Product	25°C Full		12.0 10.0		MHz MHz
Slew Rate[3, 5]	25°C	22	25		V/µs
Rise Time[4]	25°C		30	35	ns
Overshoot[4]	25°C		15	35	%
Overdrive Recovery Time	25°C		2	5	µs
Settling Time[4]	25°C Full		180	450 450	ns ns
Output Clamp Voltage	25°C			0.4	V
Input Clamp (+) Icn− Current (pin 3)	25°C 125°C −55°C	−1.0 −1.0 −0.8		−3.3 −3.3 −3.5	mA mA mA
Input Clamp (−) Icn+ Current (pin 3)	25°C 125°C −55°C	+0.5 +0.5 +0.3		+3.0 +3.0 +3.2	mA mA mA

NOTES:

1. $V_o = \pm10V$, $R_L = 2K$
2. $V_{cm} = \pm10V$, $R_L = 2K$
3. $\Delta V = \pm5.0V$
4. $A_V = +1$, $V_{IN} = 1V$, $R_L = 2K$, $C_L = 100pf$
5. $C_{BW} = 0$, $V_o = \pm10V$, $R_L = 2K$, $C_L = 100pf$

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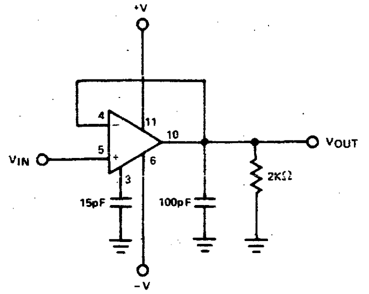
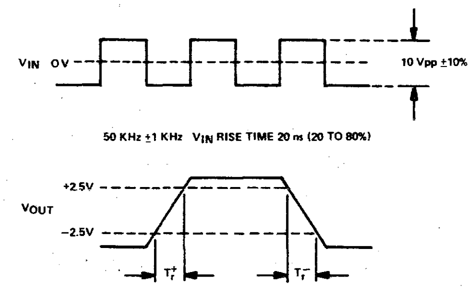
SLEW RATE CIRCUIT



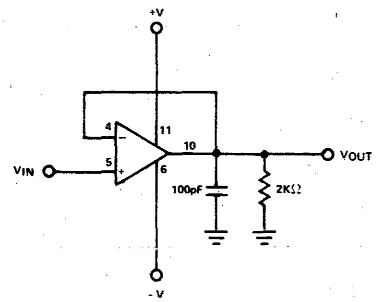
1. SLEW RATE = $\frac{5}{T_r^+ \ (\mu s)}$ V/μs

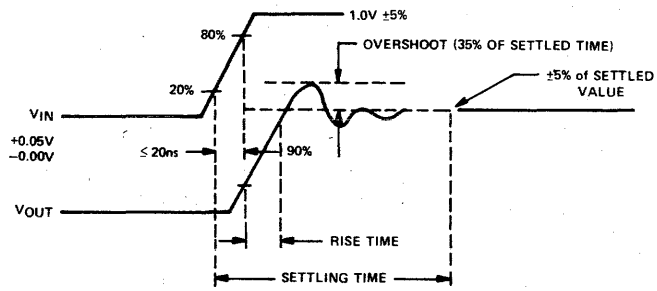
   OR — $\frac{5}{T_r^- \ (\mu s)}$ V/μs

2. INPUT BIAS CURRENT OF NON-INVERTING INPUT MAY INCREASE IF V_{IN} APPLIED BEFORE + V AND −V.

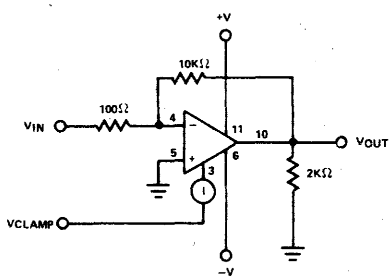


RISE TIME/SETTLING TIME CIRCUIT





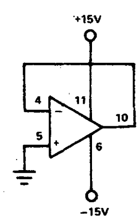
VOLTAGE CLAMP CIRCUIT



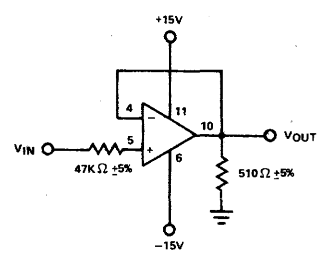
1. V_{IN} = +1.0 VDC
2. V_{CLAMP} = −3.0 VDC
3. MEASURE V_{OUT}; V_{OUT} SHALL BE WITHIN ±0.4VDC OF V_{CLAMP}.
4. REPEAT STEPS 1, 2, 3 USING BOTH VOLTAGES OF OPPOSITE POLARITY.
5. REPEAT STEPS 1 THRU 4 USING A VALUE OF 6 VDC IN STEP 2.
6. I =

	MIN	MAX
6. I =	− 1.0mA	− 3.3mA
	+ 0.5mA	+ 3.0mA

IRRADIATION CIRCUIT



BURN-IN CIRCUIT



V_{IN} = 50 KHz SQUARE WAVE 50% DUTY CYCLE −4.0V TO +4.0V

Radiation Screening Procedure

(1) Two (2) probed good samples per wafer will be selected from ≥ 20% of the wafers in a run. (All wafers in a "run" will have been processed together through all high temperature processing steps and through metallization.)

(2) The sample die shall be assembled and tested for functionality.

(3) The sample devices shall be subjected to a Total Dose Radiation level of 1×10^6 Rad (Si) ±10% from a gamma cell 220 cobalt 60 source or equivalent. The devices will be powered in the configuration illustrated with VSUPPLY = ±15V. The dose rate shall be between 50 rads/sec and 200 rads/sec.

(4) AVOL, VIO, and IBIAS, with VSUPPLY = ±15V, will be measured and recorded for each device within one hour after irradiation. The lot will be accepted only if the sample, exclusive of non-radiation failures, meets the limits of AVOL ≥ 80dB, VIO ≤ ±5.0mV and IBIAS ≤ ±400nA at room temperature.

Radiation Effects

(1) Total Dose

Little or no effect will be observed at 1×10^5 Rad (Si). IBIAS, IIO, and AVOL starts to degrade between 1×10^5 and 1×10^6 Rad (Si).

(2) Dose Rate

Devices are constructed in DI and consequently are latchup free.

(3) Neutron Fluence

Performance degradation is insignificant at 5×10^{12}n/cm^2.

Test Product Flow

HARRIS SEMICONDUCTOR PRODUCT FLOW
MIL-STD-883, METHOD 5004 CLASS B

100% SCREENING PROCEDURE

	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1010 Cond. C
4	Constant Acceleration	2001 Cond. E; Y1 plane
5	Seal: A Fine B Gross	1014 Cond. A or B 1014 Cond. C2
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. @ 125°C (or equivalent) (Burn-In circuits enclosed)
8	Final Electrical 100% go-no-go	Tested at Worst Case Operating Conditions
9	External Visual	2009 Sample Inspection

Note:

Traceability: All devices are assigned date code identification that provides traceability back to the inspection lot.

Branding: All devices are branded with the part number and EIA date code.

Aged Products: Product that has been held for more than 24 months will be reinspected prior to shipment to group A inspection requirements.

Additional Requirements: Sample Group A electrical tests are performed on a lot acceptance basis.

Sales Offices

EASTERN REGION

2600 Virginia Avenue
Suite 800
Washington, DC 20037
(202) 342-3900
TWX: 710-822-9301

Five Old Concord Road
Burlington, MA 01803
(617) 273-1020
TWX: 710-332-1074

106 Seventh Street
Garden City, NY 11530
(516) 747-6776

WESTERN REGION

1503 South Coast Drive
Suite 320
Costa Mesa, CA 92626
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TWX: 910-595-1533

625 Ellis, Suite 300
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MIDWEST REGION

2850 Metro Dr., Suite 703
Minneapolis, MN 55420
(612) 854-3224
TWX: 910-576-3418

HOME OFFICE

P.O. Box 883
Melbourne, FL 32901
(305) 724-7045
TWX: 510-959-6259

EUROPEAN

Harris Systems Ltd.
Semiconductor Programs Division
P.O. Box 27
145 Farnham Road
Slough SL1 4XD
United Kingdom
Tel: 34666
TWX: 848174

CUSTOM INTEGRATED CIRCUITS DIVISION

HARRIS

HARRIS

HS-3530RH

Low Power-Radiation Resistant Programmable Operational Amplifier

Features

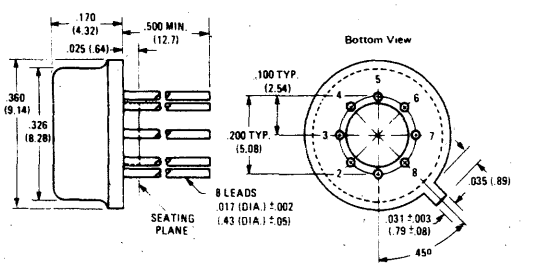
- WIDE RANGE AC PROGRAMMING
  - SLEW RATE 06 TO3V/μs
  - GAIN X BANDWIDTH . . . . 100KHz TO 5.0MHz
- WIDE RANGE DC PROGRAMMING
  - POWER SUPPLY RANGE . . . . $\pm$1.5V TO $\pm$18V
  - SUPPLY CURRENT . . . . 10μA TO 1.2mA
- SHORT CIRCUIT PROTECTION
- RADIATION ENVIRONMENT
  - NEUTRON FLUENCE(ϕ) . 5 x 10^{12} n/cm^2 (E $\geq$ 10KeV)
  - GAMMA RATE($\dot{\gamma}$) . . . . 1 x 10^9 RADS (Si)/s
  - GAMMA DOSE(γ) . . . . 1 x 10^6 RADS (Si)

Description

The HS-3530 is a Low Power Operational Amplifier which is an internally compensated monolithic device offering a wide range of performance specifications. Parameters such as power dissipation, slew rate, bandwidth, noise and input DC parameters are programmed by selecting an external resistor or current source. Supply voltages as low as $\pm$3 volts may be used with little degradation of AC performance. The HS-3530 has been specifically designed to meet exposure to radiation environments. Operation from $-55°C$ to $+125°C$ is guaranteed.

A major advantage of the HS-3530 is that operating characteristics remain virtually constant over a wide supply range (+3V to +15V), allowing the amplifier to offer maximum performance in almost any system, including battery operated equipment. A primary application for this device is in active filtering and conditioning for a wide variety of signals that differ in frequency and amplitude. Also, by modulating the set current, it can be used for designs such as current controlled oscillators/modulators, sample and hold circuits and variable active filters.

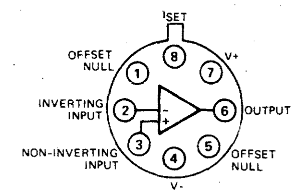
Package



1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions $\pm$ .010 ($\pm$0.25mm) unless otherwise shown.

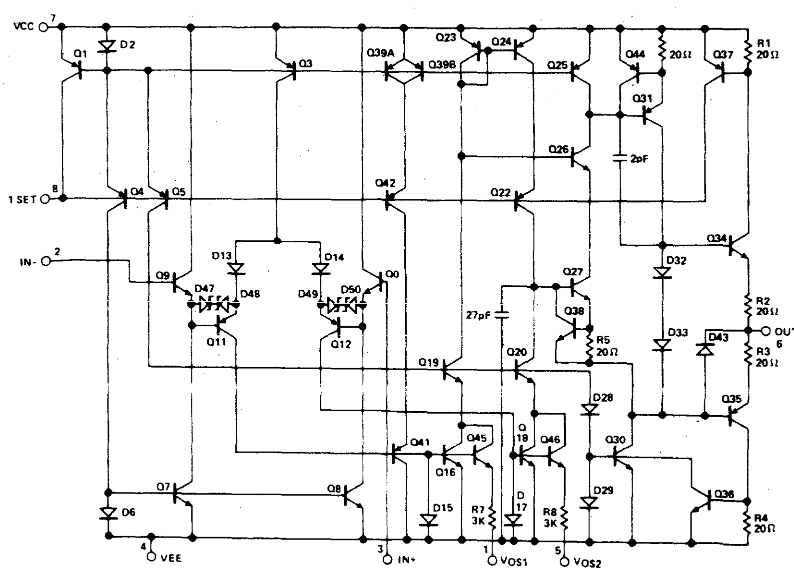
Pinout

TOP VIEW



NOTE: Case tied to V-

Schematic



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ABSOLUTE MAXIMUM RATINGS

Voltage between V+ and V- terminals	40V
Differential Input Voltage	± 20V
Input Voltage (Note 1)	± 15V
I_{SET} (current at I_{SET})	500μA
V_{SET} (voltage to ground at I_{SET})	(V+ -2.0V)<V_{SET}<V+
Output Short Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C

NOTE:
① For supply voltage less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

PRE-RADIATION ELECTRICAL CHARACTERISTICS

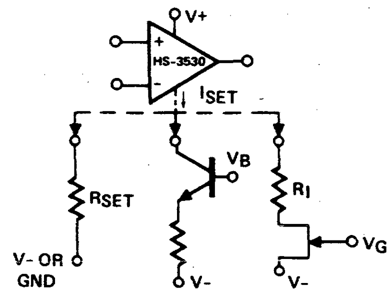
V_{SUPPLY} = ±15V		I_{SET} = 1.5μA (R_L = 75KΩ)			I_{SET} = 15μA (R_L = 5KΩ)			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Offset Voltage	25°C		1	3		1	3	mV
	Full			5			5	mV
Input Bias Current	25°C		1.2			10	20	nA
	Full		2.5			22	40	nA
Input Offset Current	25°C		0.3			2	5	nA
	Full						10	nA
Input Resistance	25°C		>100		50	>100		MΩ
Large Signal Voltage Gain[1]	25°C	65K	115K		80K	130K		V/V
	Full	25K	60K		50K	70K		V/V
Common Mode Rejection Ratio[2]	25°C	80	115		80	115		dB
	Full				80	110		dB
Supply Current	25°C		13	15		125	150	μA
	Full		14	15		130	160	μA
Power Supply Rejection Ratio[3]	25°C	80	130		80	130		dB
	Full				80	120		dB
Output Voltage Swing[2]	25°C	±12.5	±14.2		±12.5	±14.2		V
	Full	±10.5	±14.0		±10.5	±14.0		V
Output Current	25°C		±.5			±5		mA
	Full		±.4			±4		mA
Output Short-Circuit Current	25°C		2			14		mA
Gain-Bandwidth Product	25°C		85			850		kHz
	Full		65			640		kHz
Slew Rate[5]	25°C		.05			.55		V/μS
Rise Time[4]	25°C		7.5			.7		μS
Overshoot[4]	25°C		5			10		%
Overdrive Recovery Time	25°C					2		μS

V_{SUPPLY} = ±3V		I_{SET} = 1.5μA (R_L = 75KΩ)			I_{SET} = 15μA (R_L = 5KΩ)			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Large Signal Voltage Gain[1]	25°C	25K	60K		25K	75K		V/V
	Full	15K	40K		25K	50K		V/V
Common Mode Rejection Ratio[2]	25°C	80	100		80	95		dB
	Full	80	90					dB
Supply Current	25°C		12	15		115	150	μA
	Full			15			160	μA
Power Supply Rejection Ratio[3]	25°C	80	105		80	105		dB
	Full	80	100					dB
Output Voltage Swing[1]	25°C	±2.0			±2.0			V
	Full	±2.0			±2.0			V
Gain-Bandwidth Product	25°C		72			730		kHz
	Full		60			600		kHz
Slew Rate[5]	25°C		04			.4		V/μS
Offset Voltage	25°C		1	3		1	3	mV
	Full			5			5	

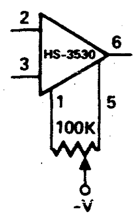
NOTES:

1.	$V_{SUPPLY} = \pm3.0V$ / $V_O = \pm1.0V$	$V_{SUPPLY} = \pm15.0V$ / $V_O = \pm10.0V$	$I_{SET} = 1.5\mu A$ / $R_L = 75K$	$I_{SET} = 15\mu A$ / $R_L = 5K$ +25°C +125°C, $R_L = 75K$ -55°C
2.	$V_{CM} = \pm1.5V$	$V_{CM} = \pm5.0V$		
3.	$V = \pm1.5V$	$\Delta V = \pm5.0V$		
4.	← $A_V = +1$, $V_{IN} = 400mV$, $R_L = 5K$, $C_L = 100pF$ →			
5.	$V_O = \pm2.0V$	$V_O = \pm10.0V$	$R_L = 20K$	$R_L = 5K$ +25°C +125°C, $R_L = 75K$ -55°C

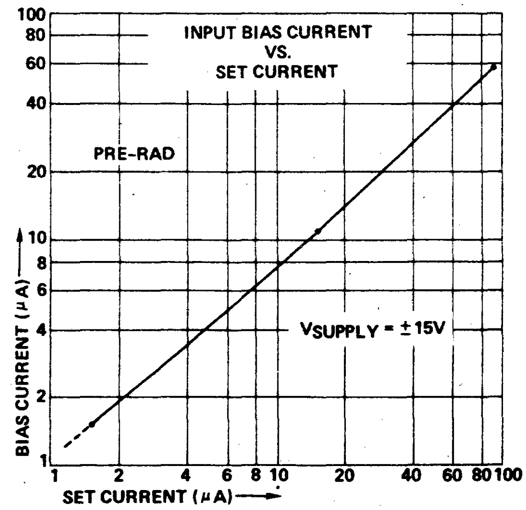
Typical Biasing Circuits

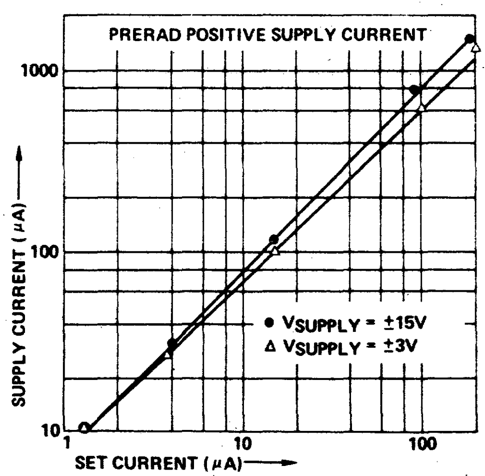


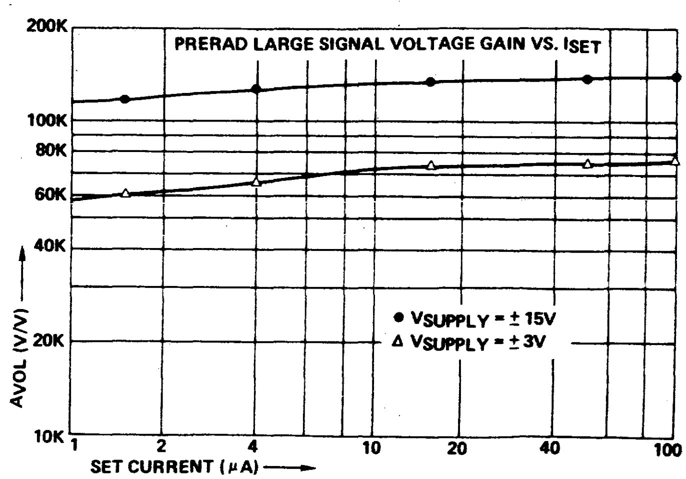
SUGGESTED OFFSET NULL



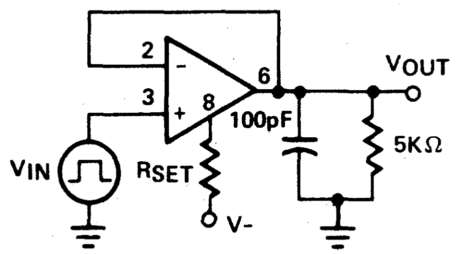
Typical Performance Curves

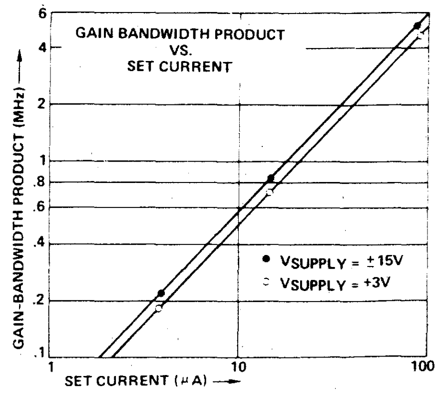




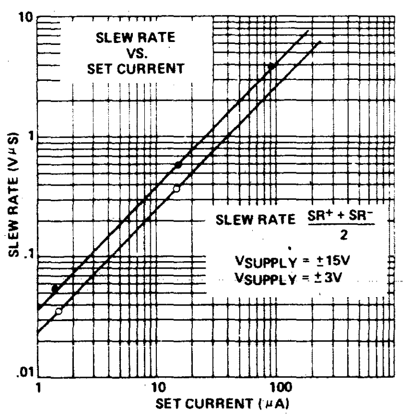


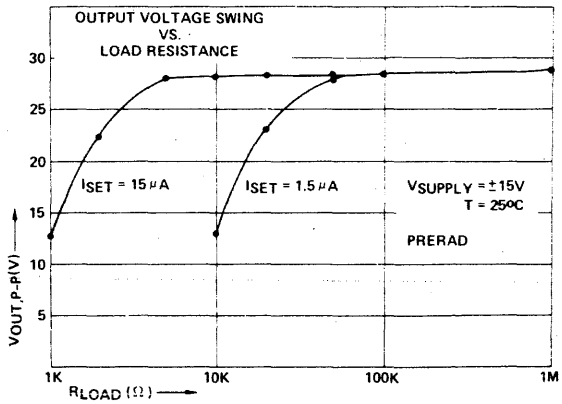
Transient Response/Slew Rate Circuit

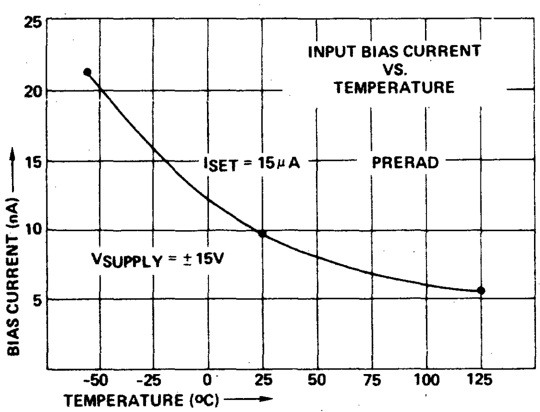


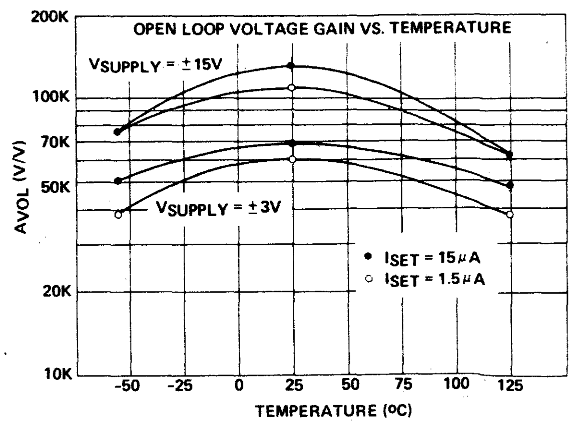


Typical Performance Curves









Radiation Screening Procedure

(1) Two (2) probed good samples per wafer will be selected from ≥20% of the wafers in a run. (All wafers in a "run" will have been processed together through all high temperature processing steps and through metallization.)

(2) The sample die shall be assembled and tested for functionality.

(3) The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^6 Rad (Si) ±10% from a Gamma Cell 220 Cobalt 60 source or equivalent. The devices will be powered in a voltage follower configuration, with I_{SET} = 15 μA and V_{SUPPLY} = ±15V. The dose rate shall be between 50 rads/sec and 200 rads/sec.

(4) A_{VOL} and V_{IO}, with I_{SET}= 15 μA, V_{SUPPLY} = +15V and R_L = 25K, will be measured and recorded for each device within one hour after irradiation. The lot will be accepted only if the sample, exclusive on non-radiation failures, meets the limits of $A_{VOL} \geq$ 20K V/V and $V_{IO} \leq$ 3.5 mV at room temperature.

Radiation Effects

(1) Total Dose:
Very little degradation of any of the parameters will be seen up to γ= 10^4 Rad (Si). Moderate degradation of open loop gain, bias current, and offset current begins at greater than 10^5 and less than 10^6 Rad (Si).

(2) Dose Rate:
During transient ionizing radiation at a level of 1 x 10^9 rad (Si)/s, the peak level of supply current will be about 150 to 200 mA. After about 0.1 to 0.5 μS this current drops about 10%. Maximum recovery time will be about 6 to 8 μS.

(3) Neutron Fluence:
Large signal voltage gain degrades rapidly for low supply voltages and low set currents. For V_{SUPPLY} = +15V and I_{SET} > 10 μA, large signal voltage gain degrades by only about 50%. Input bias current doubles for ϕ= 5 x 10^{12}n/cm^2.

Test Product Flow

HARRIS SEMICONDUCTOR PRODUCT FLOW
MIL - STD - 883, METHOD 5004 CLASS B
100% SCREENING PROCEDURE

	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1010 Cond. C
4	Constant Acceleration	2001 Cond. E; Y1 plane
5	Seal: A Fine B Gross	1014 Cond. A or B 1014 Cond. C2
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. 125°C (or equivalent)
8	Final Electrical 100% go-no-go	Tested at Worst Case Operation Conditions
9	External Visual	2009 Sample Inspection

Note:

Traceability:	All devices are assigned date code identification that provides traceability back to the inspection lot.
Branding:	All devices are branded with the part number and E1A date code.
Aged Products:	Product that has been held for more than 24 months will be reinspected prior to shipment to group A inspection requirements.
Additional Requirements:	Sample Group A electrical tests are performed on a lot acceptance basis.

HARRIS

Preliminary

HS-3546RH

Radiation Resistant High Performance Operational Amplifier

Features

- LOW OFFSET VOLTAGE 0.3mV
- HIGH SLEW RATE ±4V/µs
- WIDE BANDWIDTH 8MHz
- LOW DRIFT 2µV/°C
- FAST SETTLING (0.01%, 10V STEP) 4.2µs
- LOW POWER CONSUMPTION 35mW
- SUPPLY RANGE ±5V TO ±20V
- RADIATION ENVIRONMENT
  - NEUTRON FLUENCE (ϕ) . 5×10^{12} n/cm² (E ≥ 10KeV)
  - GAMMA RATE ($\dot{\gamma}$) . . . . 1×10^{9} RADS (Si)/s
  - GAMMA DOSE (γ) . . . . 1×10^{6} RADS (Si)

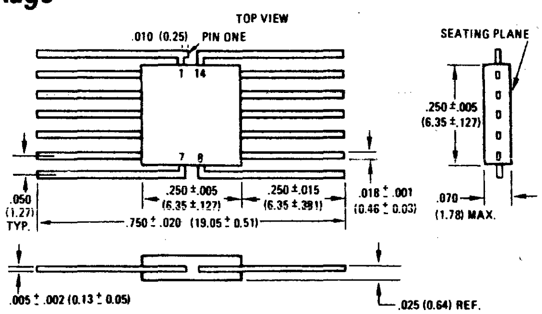
Description

The HS-3546RH is a radiation resistant, high performance dielectrically isolated monolithic operational amplifier with superior specifications. This amplifier offers excellent dynamic performance coupled with low values for offset voltage and drift, input noise voltage and power consumption.

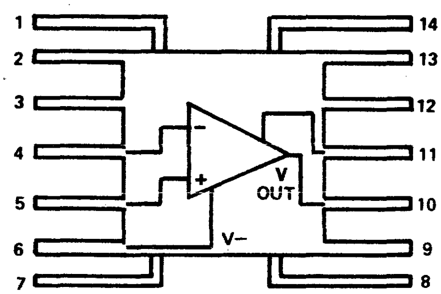
A wide range of applications can be achieved by using the features made available by the HS-3546RH. With wide bandwidth (8MHz), low power (35mW) and internal compensation, these devices are ideally suited for precision active filter designs. For audio applications these amplifiers offer low noise (8nV/√Hz) and excellent full power bandwidth (60 KHz). The HS-3546RH is particularly useful in designs requiring low offset voltage (0.3mV) and drift (2µV/°C), such as instrumentation and signal conditioning circuits. The high slew rate (4V/µs) and fast settling time (4.2 µs to 0.01%, 10V step) makes this amplifier a useful component in fast, accurate data acquisition systems.

The HS-3546RH has been specifically designed to meet exposure to radiation environments. It is available in a 14 Pin Ceramic Flatpack package and is guaranteed operational from -55°C to +125°C.

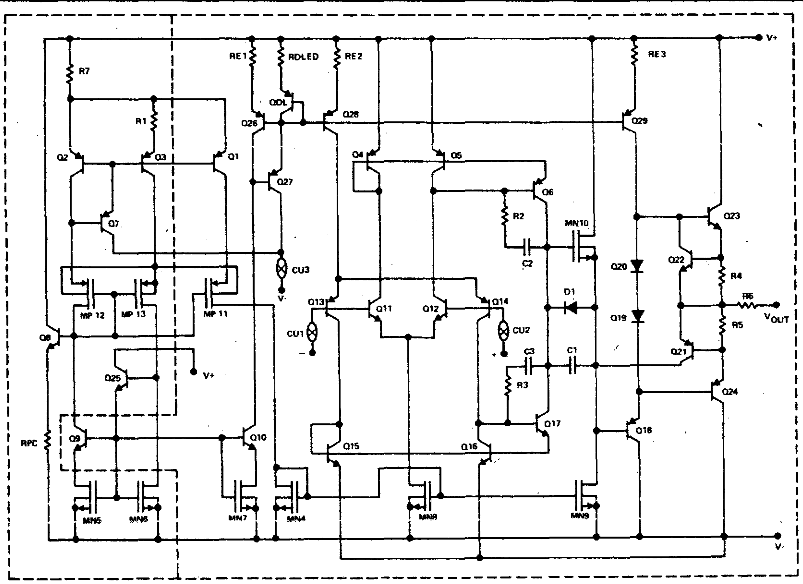
Package



Pinout



Schematic



ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless Otherwise Stated	
Voltage Between V+ and V- Terminals	40.0V
Differential Input Voltage	±7V
Input Voltage (Note 2)	±15.0V
Output Short Circuit Duration (Note 3)	Indefinite
Power Dissipation (Note 4)	880mW
Operating Temperature Range	$-55°C \leq T_A \leq +125°C$
Storage Temperature Range	$-65°C \leq T_A \leq +150°C$

CAUTION: To prevent permanent damage to this device, care should be exercised to insure that the absolute maximum ratings for supply voltages, temperature and voltage or current at any pin is not exceeded during both static and dymanic operation.

ELECTRICAL CHARACTERISTICS V+ = 15V, V– = –15V T_A = –55°C to +125°C

PARAMETER	TEMP	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
* Offset Voltage	+25°C		0.3	2.5	mV
	Full			3.0	mV
Av. Offset Voltage Drift	Full		2		μV/°C
* Bias Current	+25°C		130	200	nA
	Full			325	nA
* Offset Current	+25°C		30	75	nA
	Full			125	nA
Common Mode Range	Full	±12			V
Input Noise Voltage (f = 1kHz)	+25°C		8		$nV/\sqrt{Hz}$
Input Resistance			500		kΩ
TRANSFER CHARACTERISTICS					
* Large Signal Voltage Gain (Note 5)	Full	50K	150K		V/V
* Common Mode Rejection Ratio (Note 8)	Full	86			dB
Small Signal Bandwidth	+25°C		8		MHz
OUTPUT CHARACTERISTICS					
* Output Voltage Swing (R_L = 10K)	Full	±12	±13		V
(R_L = 2K)	Full	±10	±12		V
Full Power Bandwidth (Note 5)	+25°C		60		kHz
Output Current (Note 6)	Full	±18	±25		mA
Output Resistance	+25°C		200		Ω
TRANSIENT RESPONSE (Note 7)					
Rise Time	+25°C		50	150	ns
Overshoot	+25°C		30	45	%
Slew Rate	+25°C	±1	±4		V/μs
Settling Time (Note 9)			4.2		μs
POWER SUPPLY CHARACTERISTICS					
* Supply Current	+25°C		4.6	5.5	mA
* Power Supply Rejection Ratio (Note 8)	Full	86			dB

*100% tested

Harris Semiconductor

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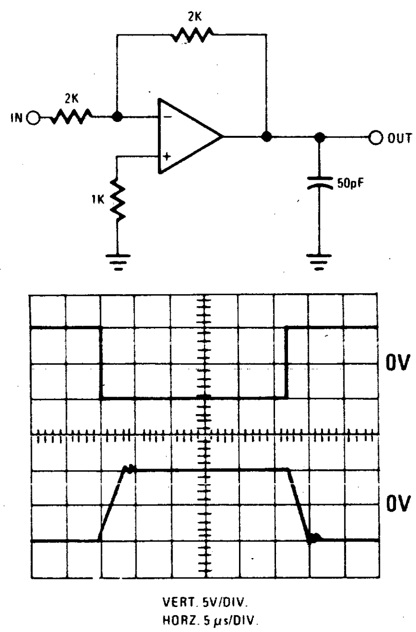
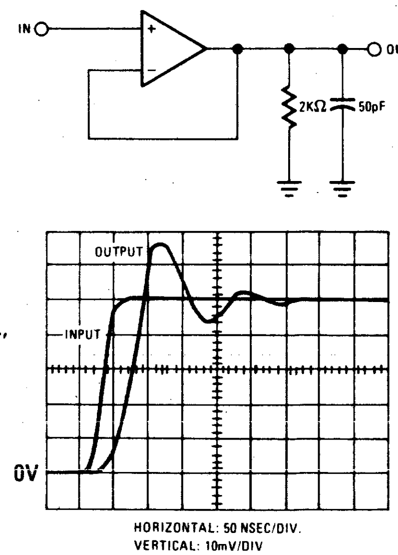
NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Any one amplifier may be shorted to ground indefinitely.
4. Derate 5.8mW/°C above T_A = +25°C.
5. V_{OUT} = ±10V; R_L = 2K ohms.
6. Output current is measured with V_{OUT} = ±5 volts.
7. For transient response test circuits and measurement conditions refer to Test Circuits section of the data sheet.
8. ΔV = ±5.0 volts.
9. Settling time is measured to 0.1% of final value for a 10 volt input step, A_V = -1.

Test Circuits

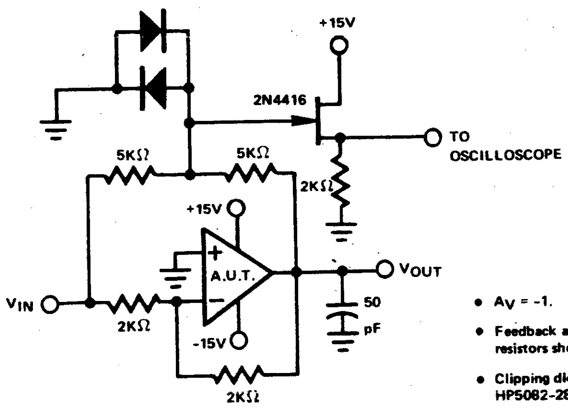


LARGE SIGNAL RESPONSE CIRCUIT (Volts: 5V/Div., Time: 5µs/Div.)



SMALL SIGNAL RESPONSE CIRCUIT (Volts: 10mV/Div., Time: 50ns/Div.)

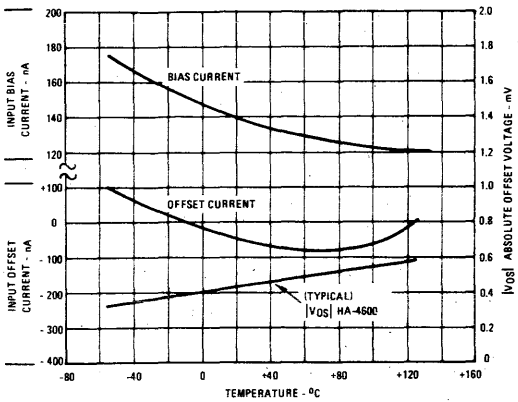
SETTLING TIME CIRCUIT



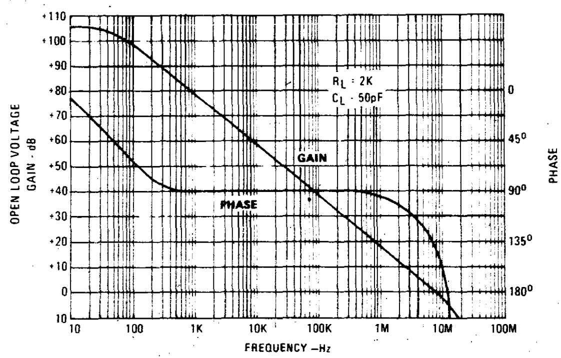
- A_V = -1.
- Feedback and summing resistors should be 0.1%.
- Clipping diodes are optional. HP5082-2810 recommended.

V+ = +15V, V- = -15V, T_A = +25°C Unless Otherwise Stated.

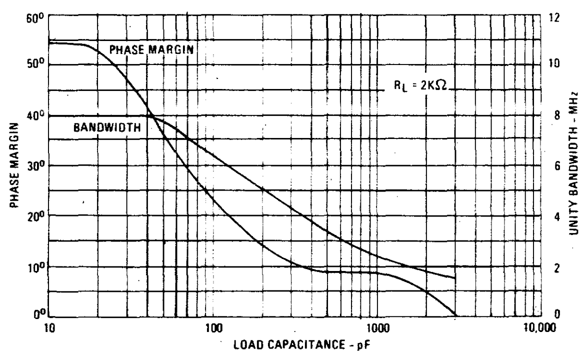
OFFSET VOLTAGE INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE



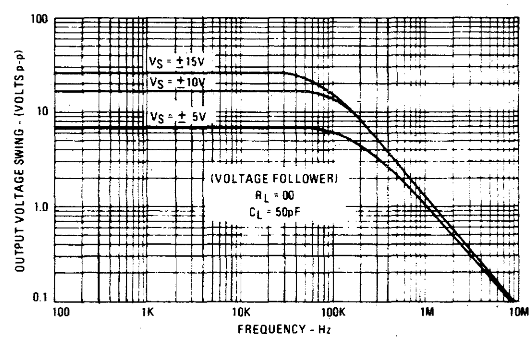
OPEN LOOP FREQUENCY RESPONSE



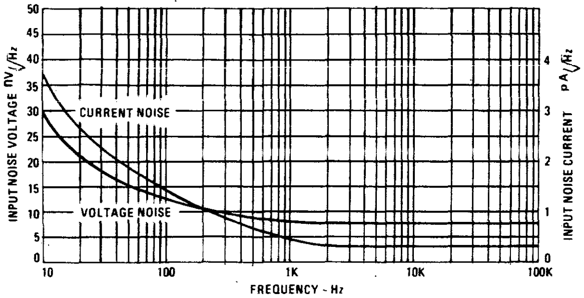
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN VS. LOAD CAPACITANCE



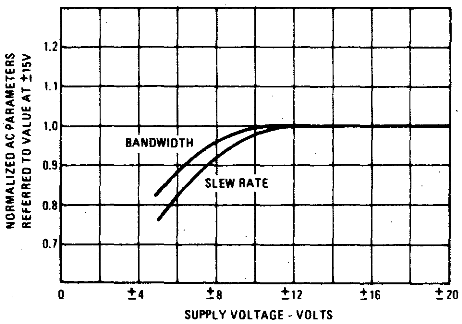
OUTPUT VOLTAGE SWING VS. FREQUENCY AND SUPPLY VOLTAGE



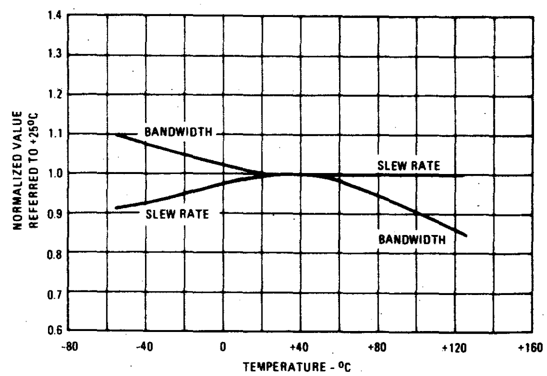
INPUT NOISE VS. FREQUENCY



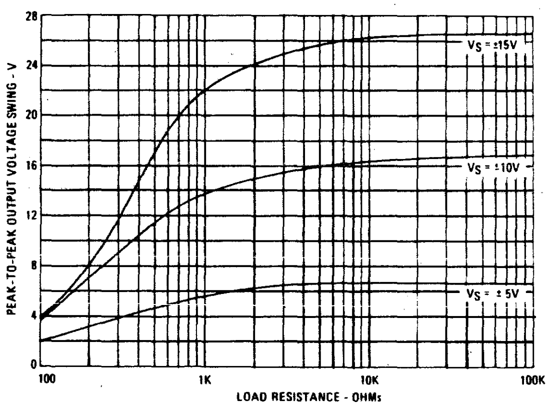
NORMALIZED AC PARAMETERS
VS. SUPPLY VOLTAGE



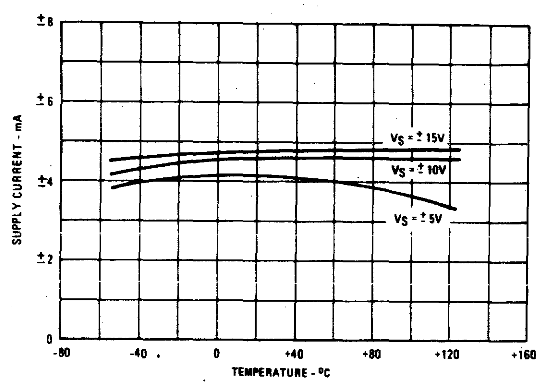
NORMALIZED AC PARAMETERS
VS. TEMPERATURE



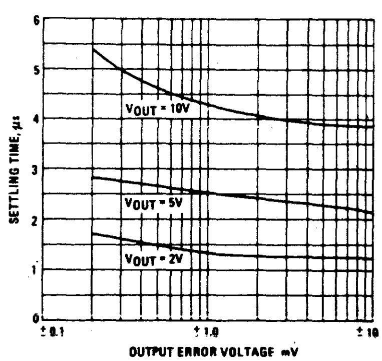
MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD
RESISTANCE AND SUPPLY VOLTAGE



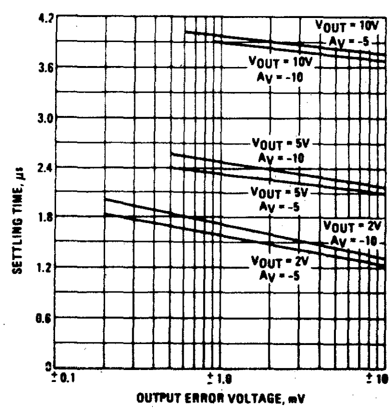
POWER SUPPLY CURRENT VS. TEMPERATURE
AND SUPPLY VOLTAGE



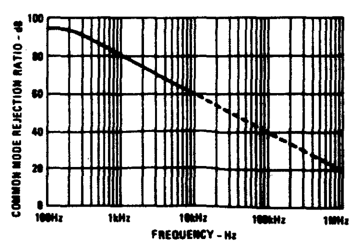
SETTLING TIME VS. OUTPUT
AMPLITUDE (A_V = -1)



SETTLING TIME VS. OUTPUT AMPLITUDE
AND SIGNAL GAIN (A_V = -5 AND A_V = -10)



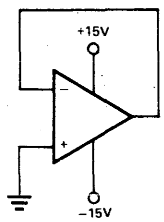
COMMON MODE REJECTION
RATIO VS. FREQUENCY



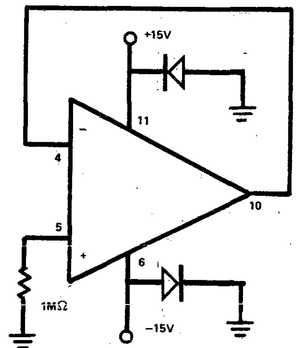
1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with .01 μ F ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

2. In high frequency applications where large value feedback resistors are used, a small capacitor (3pF) may be needed in parallel with the feedback resistor to neutralize the pole introduced by input capacitance.

Irradiation Circuit



Burn-in Circuit



NOTES:
T_A = +125°C
D = IN4002 OR EQUIVALENT

Radiation Screening Procedure

(1) Two (2) probed good samples per wafer will be selected from $\geq$20% of the wafers in a run (All wafers in a "run" will have been processed together through all high temperature processing steps and through metallization.)

(2) The sample die shall be assembled and tested for functionality.

(3) The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^5 Rad (Si) ±10% from a gamma cell 220 cobalt 60 source or equivalent. The devices will be powered in the configuration illustrated with V_{SUPPLY} = ±15V. The dose rate shall be between 50 rads/sec and 200 rads/sec.

(4) A_{VOL}, V_{IO}, AND I_{BIAS}, with V_{SUPPLY} = ±15V, will be measured and recorded for each device within one hour after irradiation. The lot will be accepted only if the sample, exclusive of non-radiation failures, meets the limits of $A_{VOL} \geq$ 50K, $V_{IO} \leq$ ±2.5mV and $I_{BIAS} \leq$ 1.0 μA at room temperature.

Radiation Effects

(1) Total Dose
Little or no effect will be observed at 1 x 10^4 Rad (Si). I_{BIAS}, I_{IO} and A_{VOL} starts to degrade between 1 x 10^4 and 1 x 10^5 Rad (Si).

(2) Dose Rate
Devices are constructed in DI and consequently are latchup free.

Test Product Flow

HARRIS SEMICONDUCTOR PRODUCT FLOW
MIL-STD-883, METHOD 5004 CLASS B

100% SCREENING PROCEDURE

	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1010 Cond. C
4	Constant Acceleration	2001 Cond. E; Y1 plane
5	Seal: A Fine B Gross	1014 Cond. A or B 1014 Cond. C2
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. @ 125°C (or equivalent) (Burn-In circuits enclosed)
8	Final Electrical 100% go-no-go	Tested at Worst Case Operating Conditions
9	External Visual	2009 Sample Inspection

Notes:

- Traceability: All devices are assigned date code identification that provides traceability back to the inspection lot.
- Branding: All devices are branded with the part number and EIA date code.
- Aged Products: Product that has been held for more than 24 months will be reinspected prior to shipment to group A inspection requirements.
- Additional Requirements: Sample Group A electrical tests are performed on a lot acceptance basis.

Ordering Information

HS 9 3546RH

- HS — HARRIS
- 9 — PACKAGE: 9 – Cerpack
- 3546RH — DEVICE NUMBER

Sales Offices

UNITED STATES

EASTERN REGION

2600 Virginia Avenue
Suite 800
Washington, DC 20037
(202) 342-3900
TWX: 710-822-9301

Five Old Concord Road
Burlington, MA 01803
(617) 273-1020
TWX: 710-332-1074

106 Seventh Street
Garden City, NY 11530
(516) 747-6776

WESTERN REGION

1503 South Coast Drive
Suite 320
Costa Mesa, CA 92626
(714) 957-6557
TWX: 910-595-1533

625 Ellis, Suite 300
Mt. View, CA 94043
(415) 964-6443
TWX: 910-379-6431

MIDWEST REGION

2850 Metro Dr., Suite 703
Minneapolis, MN 55420
(612) 854-3224
TWX: 910-576-3418

HOME OFFICE

P.O. Box 883
Melbourne, FL 32901
(305) 724-7045
TWX: 510-959-6259

EUROPEAN

Harris Systems Ltd.
Semiconductor Programs Division
P.O. Box 27
145 Farnham Road
Slough SL1 4XD
United Kingdom
Tel: 34666
TWX: 848174

HARRIS

CUSTOM INTEGRATED CIRCUITS DIVISION

HARRIS

Preliminary

HS-4602RH

Radiation Resistant High Performance Quad Operational Amplifier

Features

- LOW OFFSET VOLTAGE 0.3mV
- HIGH SLEW RATE ±4V/μs
- WIDE BANDWIDTH 8MHz
- LOW DRIFT 2μV/°C
- FAST SETTLING (0.01%, 10V STEP) 4.2μs
- LOW POWER CONSUMPTION 35mW/AMP
- SUPPLY RANGE ±5V TO ±20V
- RADIATION ENVIRONMENT
  - NEUTRON FLUENCE (ϕ) . 5×10^{12} n/cm^2 (E $\geq$ 10KeV)
  - GAMMA RATE ($\dot{\gamma}$) . . . . 1×10^9 RADS (Si)/s
  - GAMMA DOSE (γ) . . . . 1×10^6 RADS (Si)

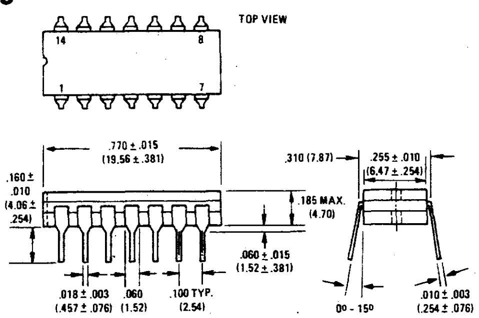
Description

The HS-4602RH is a radiation resistant, high performance dielectrically isolated monolithic quad operational amplifier with superior specifications not previously available in a quad amplifier. This amplifier offers excellent dynamic performance coupled with low values for offset voltage and drift, input noise voltage and power consumption.

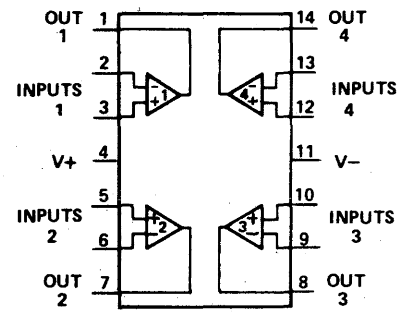
A wide range of applications can be achieved by using the features made available by the HS-4602RH. With wide bandwidth (8MHz), low power (35mW/amp), and internal compensation, these devices are ideally suited for precision active filter designs. For audio applications these amplifiers offer low noise (8nV/$\sqrt{\text{Hz}}$) and excellent full power band-width (60KHz). The HS-4602RH is particularly useful in designs requiring low offset voltage (0.3mV) and drift (2μV/°C), such as instrumentation and signal conditioning circuits. The high slew rate (4V/μs) and fast settling time (4.2μs to 0.01%, 10V step) makes this amplifier a useful component in fast, accurate data acquisition systems.

The HS-4602RH has been specifically designed to meet exposure to radiation environments. It is available in a 14 pin dual-in-line package and is guaranteed operational from −55°C to +125°C.

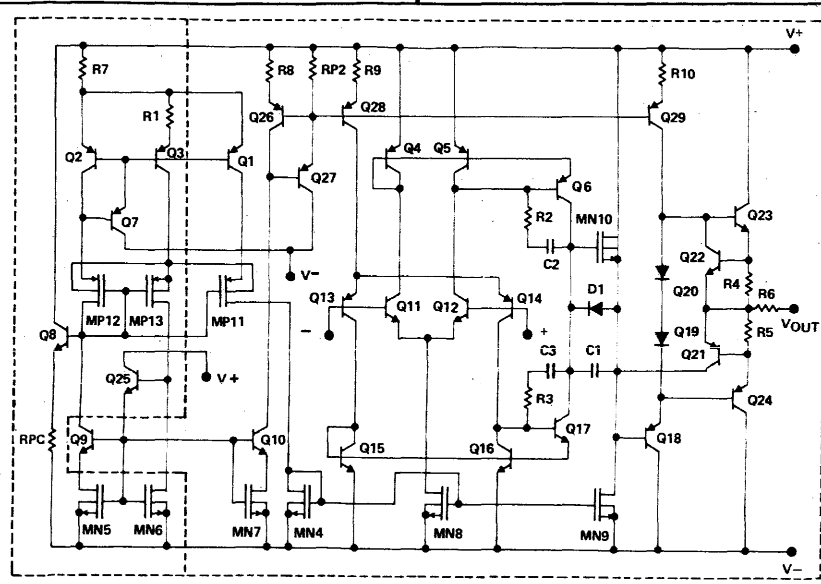
Package



Pinout



Schematic



(ONE FOURTH ONLY HS-4602-RH)

ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V- Terminals	40.0V
Differential Input Voltage	±7V
Input Voltage (Note 2)	±15.0V
Output Short Circuit Duration (Note 3)	Indefinite
Power Dissipation (Note 4)	880mW
Operating Temperature Range	$-55°C \leq T_A \leq +125°C$
Storage Temperature Range	$-65°C \leq T_A \leq +150°C$

CAUTION: To prevent permanent damage to this device, care should be exercised to insure that the absolute maximum ratings for supply voltages, temperature and voltage or current at any pin is not exceeded during both static and dymanic operation.

ELECTRICAL CHARACTERISTICS V+ = 15V, V− = −15V T_A = −55°C to +125°C

PARAMETER	TEMP	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
* Offset Voltage	+25°C		0.3	2.5	mV
	Full			3.0	mV
Av. Offset Voltage Drift	Full		2		μV/°C
* Bias Current	+25°C		130	200	nA
	Full			325	nA
* Offset Current	+25°C		30	75	nA
	Full			125	nA
Common Mode Range	Full	±12			V
Input Noise Voltage (f = 1kHz)	+25°C		8		$nV/\sqrt{Hz}$
Input Resistance			500		kΩ
TRANSFER CHARACTERISTICS					
* Large Signal Voltage Gain (Note 5)	Full	50K	150K		V/V
* Common Mode Rejection Ratio (Note 9)	Full	86			dB
Channel Separation (Note 6)	+25°C		-108		dB
Small Signal Bandwidth	+25°C		8		MHz
OUTPUT CHARACTERISTICS					
* Output Voltage Swing (R_L = 10K)	Full	±12	±13		V
(R_L = 2K)	Full	±10	±12		V
Full Power Bandwidth (Note 5)	+25°C		60		kHz
Output Current (Note 7)	Full	±10	±15		mA
Output Resistance	+25°C		200		Ω
TRANSIENT RESPONSE (Note 8)					
Rise Time	+25°C		50	150	ns
Overshoot	+25°C		30	45	%
Slew Rate	+25°C	±1	±4		V/μs
Settling Time (Note 10)			4.2		μs
POWER SUPPLY CHARACTERISTICS					
* Supply Current	+25°C		4.6	5.5	mA
* Power Supply Rejection Ratio (Note 9)	Full	86			dB

*100% tested

Harris Semiconductor

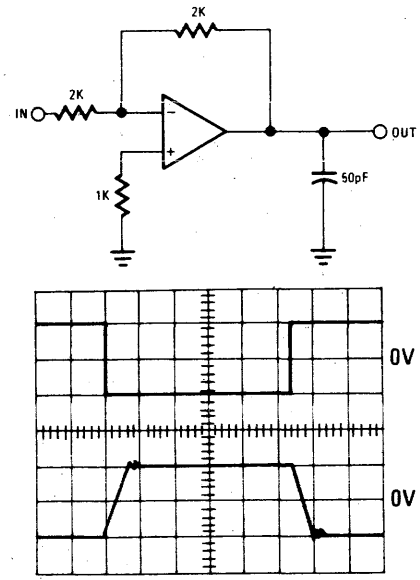
CUSTOM/SEMICUSTOM

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Any one amplifier may be shorted to ground indefinitely.
4. Derate 5.8mW/°C above T_A = +25°C.
5. V_{OUT} = ±10V; R_L = 2K ohms.
6. Channel separation value is referred to the input of the amplifier. Input test conditions are: f = 10kHz; V_{IN} = 200mV peak-to-peak; R_S = 1K ohms. (Refer to Channel Separation vs. Frequency Curve for test circuits.)
7. Output current is measured with V_{OUT} = ±5 volts.
8. For transient response test circuits and measurement conditions refer to Test Circuits section of the data sheet.
9. ΔV = ±5.0 volts.
10. Settling time is measured to 0.1% of final value for a 10 volt input step, A_V = -1.

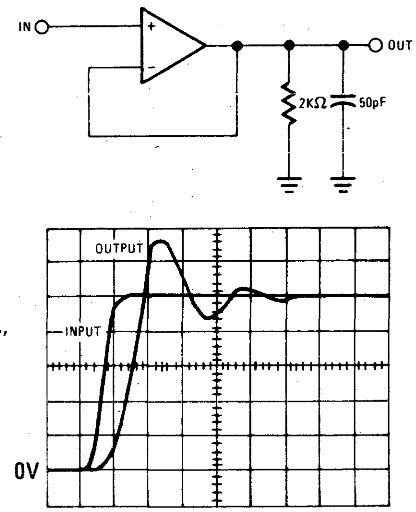
Test Circuits

LARGE SIGNAL RESPONSE CIRCUIT
(Volts: 5V/Div., Time: 5μs/Div.)



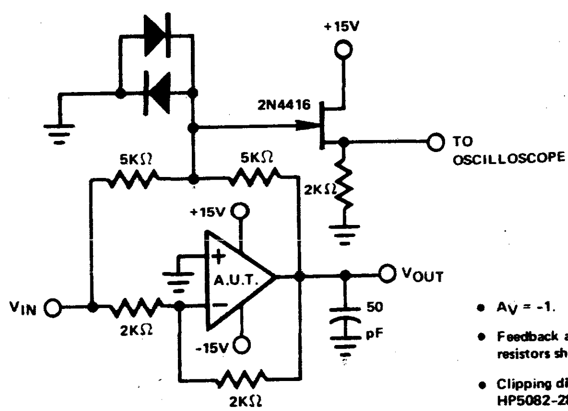
VERT. 5V/DIV.
HORZ. 5 μs/DIV.

SMALL SIGNAL RESPONSE CIRCUIT
(Volts: 10mV/Div., Time: 50ns/Div.)



HORIZONTAL: 50 NSEC/DIV.
VERTICAL: 10mV/DIV

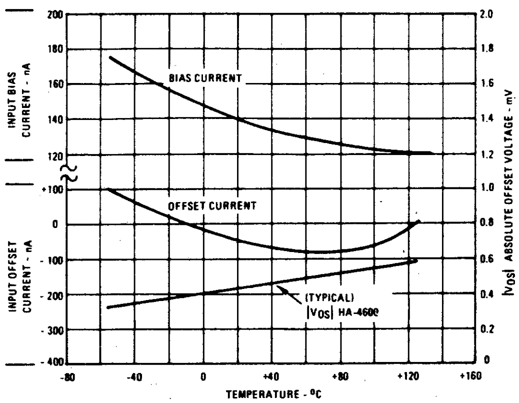
SETTLING TIME CIRCUIT



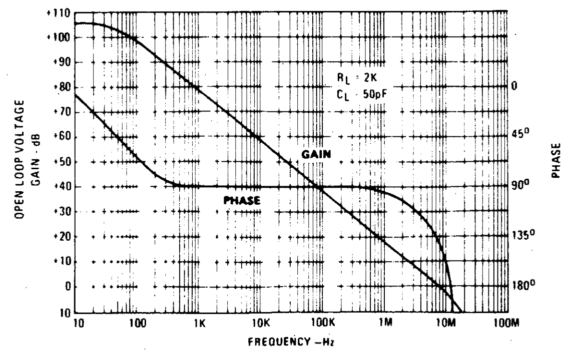
- A_V = -1.
- Feedback and summing resistors should be 0.1%.
- Clipping diodes are optional. HP5082-2810 recommended.

V+ = +15V, V- = -15V, T_A = +25°C Unless Otherwise Stated.

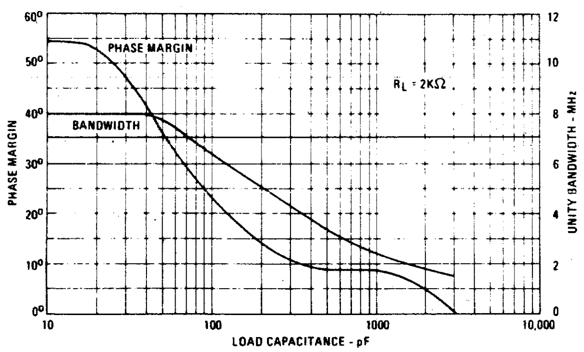
OFFSET VOLTAGE INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE



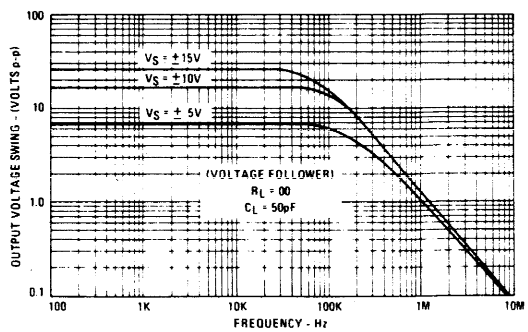
OPEN LOOP FREQUENCY RESPONSE



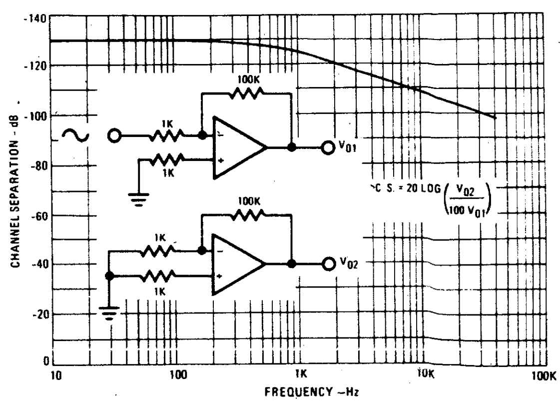
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN VS. LOAD CAPACITANCE



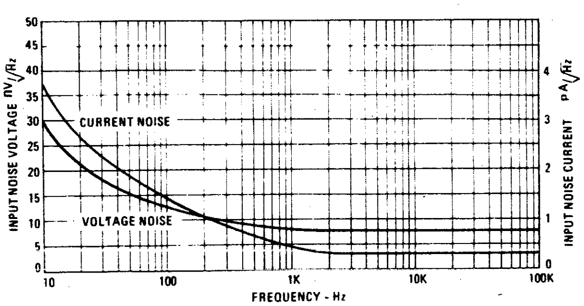
OUTPUT VOLTAGE SWING VS. FREQUENCY AND SUPPLY VOLTAGE



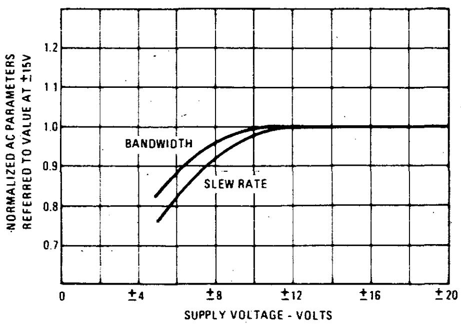
CHANNEL SEPARATION VS. FREQUENCY



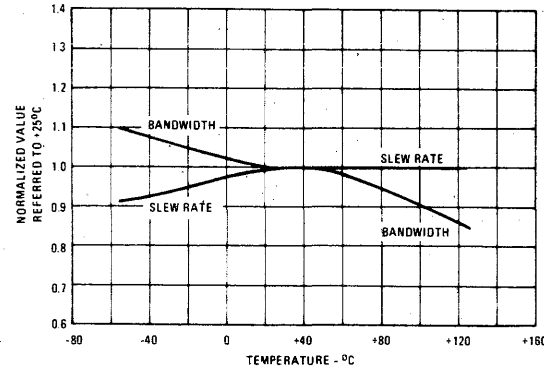
INPUT NOISE VS. FREQUENCY



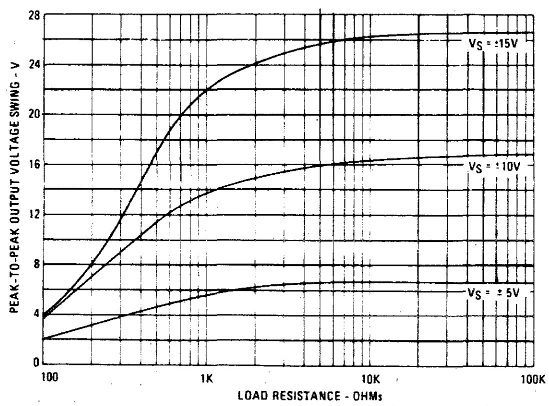
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE



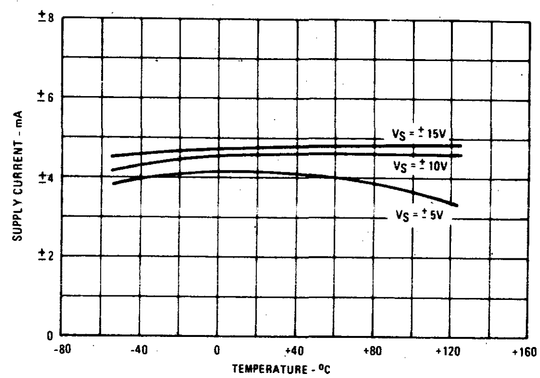
NORMALIZED AC PARAMETERS VS. TEMPERATURE



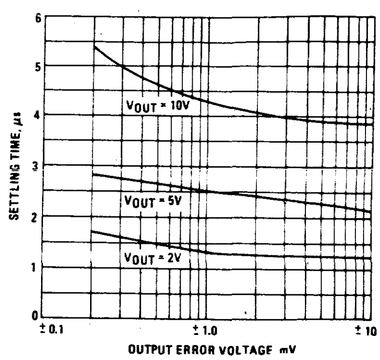
MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE AND SUPPLY VOLTAGE



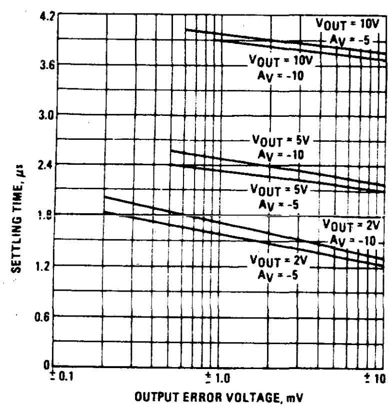
POWER SUPPLY CURRENT VS. TEMPERATURE AND SUPPLY VOLTAGE



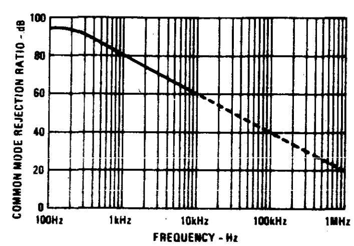
SETTLING TIME VS. OUTPUT AMPLITUDE (A_V = -1)



SETTLING TIME VS. OUTPUT AMPLITUDE AND SIGNAL GAIN (A_V = -5 AND A_V = -10)



COMMON MODE REJECTION RATIO VS. FREQUENCY



Harris Semiconductor

CUSTOM/SEMICUSTOM

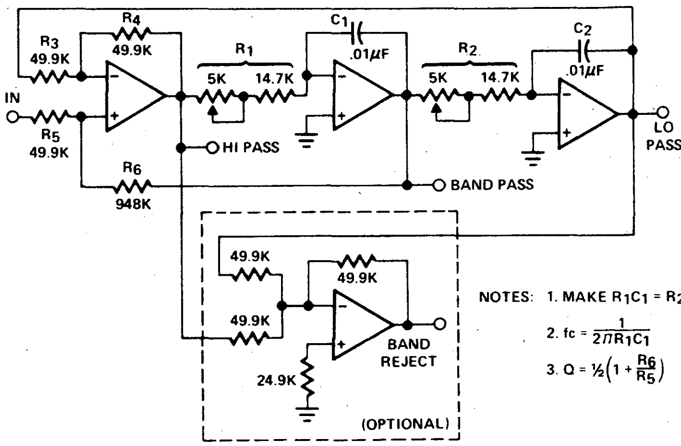
1. <u>POWER SUPPLY DECOUPLING:</u> Although not absolutely necessary, it is recommended that all power supply lines be decoupled with .01 μ F ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

2. <u>UNUSED OP AMPS:</u> Unused op amp sections should be connected in a non-inverting follower configuration with the (+) input tied to ground in order to insure optimum performance of devices being used.

3. In high frequency applications where large value feedback resistors are used, a small capacitor (3pF) may be needed in parallel with the feedback resistor to neutralize the pole introduced by input capacitance.

Applications

2ND ORDER STATE VARIABLE FILTER (1kHz, Q = 10)



NOTES: 1. MAKE $R_1C_1 = R_2C_2$

2. $f_c = \frac{1}{2\pi R_1 C_1}$

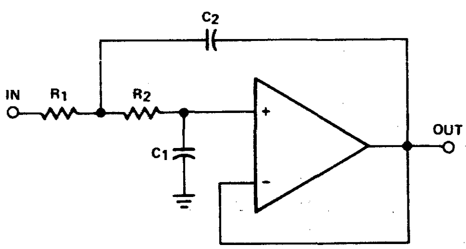
3. $Q = \frac{1}{2}\left(1 + \frac{R_6}{R_5}\right)$

The state variable filter is relatively insensitive to component changes (changes can be adjusted out with potentiometers) and also has low sensitivity to amplifier bandwidths. (Amplifier gain bandwidth product should be $\gg Q \times f_C$).

This filter finds wide application because multiple filtering functions are available simultaneously (High pass, Lo pass, Band pass, Band reject). In this circuit the various RC products are matched with pot adjustments allowing for non-interactive adjustment of Q and f_C. This allows capacitors (C_1, C_2) with loose tolerances to be used. To tune for f_C, apply a sine wave at f_C to the input, adjust R_1 for equal amplitudes at the Hi pass and Band pass terminals (they will be phased 90^o apart) then adjust R_2 for equal amplitudes at the Band pass and Lo pass terminals.

The state variable filter is often used as building blocks in multiple pole Butterworth of Chebyshev filters. Many references contain normalized tables indicating settings for Q and f_C of each pole-pair section.

SALLEN AND KEY 2ND ORDER LO PASS FILTER



NOTES:

1. Make $R_1 = R_2$

2. $f_c = \frac{1}{2\pi R_1 \sqrt{C_1 C_2}}$

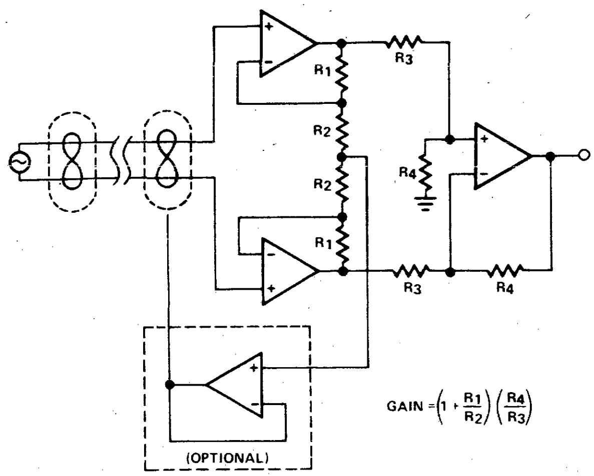
3. $Q = \frac{1}{2}\sqrt{\frac{C_2}{C_1}}$

The advantage of using the Sallen and Key filter is simplicity, but in any application this must be weighed against the state-variable type filter for accuracy, practicality, and cost. Amplifier bandwidth limitations are much more apparent at moderate frequencies and Q values with this filter design. (For accuracy, amplifier gain-bandwidth product should be $\gg f_C \times Q^2$). The wide bandwidth of the HS-4602RH is particularly advantageous in this design even at audio frequencies.

In this filter all component values affect both Q and f_C. Precision, temperature stable resistors and capacitors must be used.

For economy, this filter could be used in the low Q stages of multiple-pole filter design, while the state variable type is used in the more critical stages.

INSTRUMENTATION AMPLIFIER

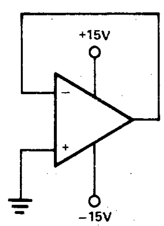


Instrumentation amplifiers (differential amplifiers) are specifically designed to extract and amplify small differential signals from much larger common mode voltages.

To serve as building blocks in instrumentation amplifiers, op amps must have very low offset voltage drift, high gain and wide bandwidth. The HS-4602RH is ideally suited for this application, delivering superior input and speed characteristics.

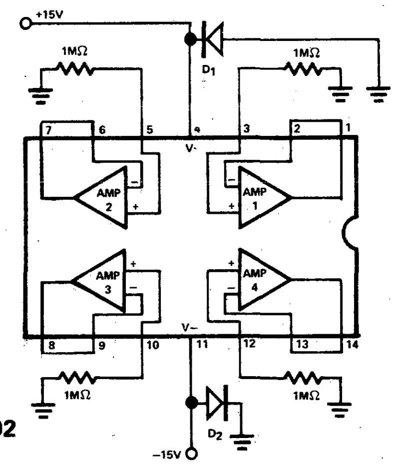
The optional circuitry makes use of the fourth amplifier section as a shield driver which enhances the AC common mode rejection by nullifying the effects of capacitance-to-ground mismatch between input conductors.

Irradiation Circuit



(1/4 OF HS-4602RH DEPICTED)

Burn-in Circuit



NOTES:
T_A = +125°C
D_1, D_2 = IN4002

Radiation Screening Procedure

(1) Two (2) probed good samples per wafer will be selected from ≥20% of the wafers in a run (All wafers in a "run" will have been processed together through all high temperature processing steps and through metallization.)

(2) The sample die shall be assembled and tested for functionality.

(3) The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^5 Rad (Si) ±10% from a gamma cell 220 cobalt 60 source or equivalent. The devices will be powered in the configuration illustrated with V_{SUPPLY} = ±15V. The dose rate shall be between 50 rads/sec and 200 rads/sec.

(4) A_{VOL}, V_{IO}, AND I_{BIAS}, with V_{SUPPLY} = ±15V, will be measured and recorded for each device within one hour after irradiation. The lot will be accepted only if the sample, exclusive of non-radiation failures, meets the limits of $A_{VOL} \geq$ 50K, $V_{IO} \leq$ ±2.5mV and $I_{BIAS} \leq$ 1.0 µA at room temperature.

Radiation Effects

(1) Total Dose
Little or no effect will be observed at 1 x 10^4 Rad (Si). I_{BIAS}, I_{IO} and A_{VOL} starts to degrade between 1 x 10^4 and 1 x 10^5 Rad (Si).

(2) Dose Rate
Devices are constructed in DI and consequently are latchup free.

Test Product Flow

HARRIS SEMICONDUCTOR PRODUCT FLOW
MIL-STD-883, METHOD 5004 CLASS B

100% SCREENING PROCEDURE

	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1010 Cond. C
4	Constant Acceleration	2001 Cond. E; Y1 plane
5	Seal: A Fine B Gross	1014 Cond. A or B 1014 Cond. C2
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. @ 125°C (or equivalent) (Burn-In circuits enclosed)
8	Final Electrical 100% go-no-go	Tested at Worst Case Operating Conditions
9	External Visual	2009 Sample Inspection

Notes:

Traceability: All devices are assigned date code identification that provides traceability back to the inspection lot.

Branding: All devices are branded with the part number and EIA date code.

Aged Products: Product that has been held for more than 24 months will be reinspected prior to shipment to group A inspection requirements.

Additional Requirements: Sample Group A electrical tests are performed on a lot acceptance basis.

Ordering Information

HS 1 4602RH

- HS — HARRIS
- 1 — PACKAGE: 1 — Cerdip
- 4602RH — DEVICE NUMBER

Sales Offices

UNITED STATES

EASTERN REGION

2600 Virginia Avenue
Suite 800
Washington, DC 20037
(202) 342-3900
TWX: 710-822-9301

Five Old Concord Road
Burlington, MA 01803
(617) 273-1020
TWX: 710-332-1074

106 Seventh Street
Garden City, NY 11530
(516) 747-6776

WESTERN REGION

1503 South Coast Drive
Suite 320
Costa Mesa, CA 92626
(714) 957-6557
TWX: 910-595-1533

625 Ellis, Suite 300
Mt. View, CA 94043
(415) 964-6443
TWX: 910-379-6431

MIDWEST REGION

2850 Metro Dr., Suite 703
Minneapolis, MN 55420
(612) 854-3224
TWX: 910-576-3418

HOME OFFICE

P.O. Box 883
Melbourne, FL 32901
(305) 724-7045
TWX: 510-959-6259

EUROPEAN

Harris Systems Ltd.
Semiconductor Programs Division
P.O. Box 27
145 Farnham Road
Slough SL1 4XD
United Kingdom
Tel: 34666
TWX: 848174

HARRIS

CUSTOM INTEGRATED CIRCUITS DIVISION

HARRIS

Preliminary

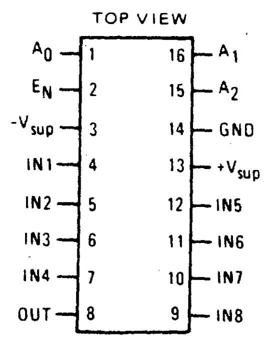
HS-508ARH

Radiation Resistant 8 Channel CMOS Analog Multiplexer With Overvoltage Protection

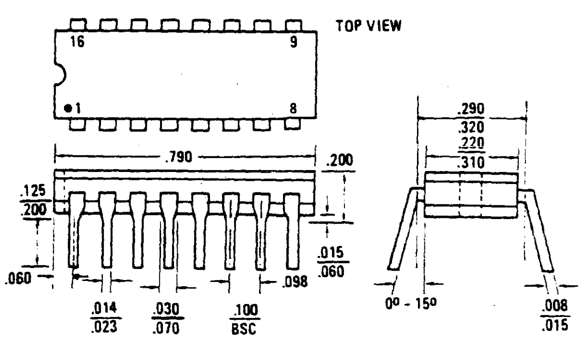
Features

- ANALOG/DIGITAL OVERVOLTAGE PROTECTION
- FAIL SAFE WITH POWER LOSS (NO LATCHUP)
- BREAK-BEFORE-MAKE SWITCHING
- DTL/TTL AND CMOS COMPATIBLE
- ANALOG SIGNAL RANGE ±15V
- ACCESS TIME (TYP.) 500ns
- SUPPLY CURRENT AT 1MHz ADDRESS TOGGLE (TYP.) 4mA
- STANDBY POWER (TYP.) 7.5mW
- RADIATION ENVIRONMENT
  - NEUTRON FLUENCE (ϕ) 1×10^9 n/cm^2 (E $\geqslant$ 10KeV)
  - GAMMA RATE ($\dot{\gamma}$) . . . . 1×10^8 RADs(Si)/s
  - GAMMA DOSE (γ) . . . . 1×10^5 RADs(Si)

Pinout



Package

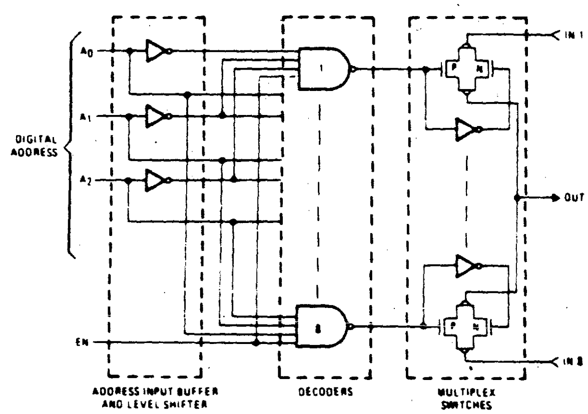


Description

The HS-508ARH is a dielectrically isolated, radiation resistant, CMOS analog multiplexer incorporating an important feature; it withstands analog input voltages much greater than the supplies. This is essential in any system where the analog inputs originate outside the equipment. They can withstand a continuous input up to 10 volts greater than either supply, which eliminates the possibility of damage when supplies are off, but input signals are present. Equally important, it can withstand brief input transient spikes of several hundred volts; which otherwise would require complex external protection networks. Necessarily, ON resistance is somewhat higher than similar unprotected devices, but very low leakage current combine to produce low errors. Reference Application Notes 520 and 521, available from the Analog Products Division of Harris, for further information on the 508A multiplexer in general.

The HS-508ARH has been specifically designed to meet exposure to radiation environments. Operation from −55°C to +125°C is guaranteed.

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge.

ABSOLUTE MAXIMUM RATINGS

Voltage between Supply Pins	40V	Total Power Dissipation*	725 mW
V+ to Ground	20V	Operating Temperature	-55°C to +125°C
V_{EN}, V_A, Digital Input Overvoltage:			
V_A	V_{Supply}(+) +4V V_{Supply}(-) -4V	Storage Temperature	-65°C to +150°C
Analog Input Overvoltage:			
V_S	V_{Supply}(+) +20V V_{Supply}(-) -20V		

*Derate 8mW/°C above t_A = 75°C

ELECTRICAL CHARACTERISTICS (Unless Otherwise Specified)

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics section.

PARAMETER	TEMP	-55°C to +125°C MIN	TYP	MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS					
*V_S, Analog Signal Range	Full	-15		+15	V
*R_{ON}, On Resistance (Note 1)	+25°C		1.2	1.5	KΩ
	Full		1.5	1.8	KΩ
*$I_{S(OFF)}$, Off Input Leakage Current	+25°C		0.03		nA
	Full			±50	nA
*$I_{D(OFF)}$, Off Output Leakage Current	+25°C		1.0		nA
	Full			±250	nA
*$I_{D(OFF)}$ with Input Overvoltage Applied (Note 2)	+25°C		4.0		nA
	Full			2.0	µA
*$I_{D(ON)}$, On Channel Leakage Current	+25°C		0.1		nA
	Full			±250	nA
DIGITAL INPUT CHARACTERISTICS					
V_{AL}, Input Low Threshold (Note 6)	Full			0.8	V
V_{AH}, Input High Threshold (Note 6)	Full	4.0			V
*I_A, Input Leakage Current (High or Low)	Full			1.0	µA
SWITCHING CHARACTERISTICS					
t_A, Access Time	+25°C		0.5	1.0	µs
t_{OPEN}, Break - Before Make Delay	+25°C		80		ns
$t_{ON(EN)}$, Enable Delay (ON)	+25°C		300		ns
$t_{OFF(EN)}$, Enable Delay (OFF)	+25°C		300		ns
Settling Time (0.1%)	+25°C		1.2		µs
(0.025%)	+25°C		3.5		µs
"OFF Isolation" (Note 3)	+25°C		65		dB
$C_{S(OFF)}$, Channel Input Capacitance	+25°C		5		pF
$C_{D(OFF)}$, Channel Output Capacitance	+25°C		25		pF
C_A, Digital Input Capacitance	+25°C		5		pF
$C_{DS(OFF)}$, Input to Output Capacitance	+25°C		0.1		pF
POWER REQUIREMENTS					
P_D, Power Dissipation	Full		7.5		mW
*I+, Current (Note 4)	Full		0.5	2.0	mA
*I-, Current (Note 4)	Full		0.02	1.0	mA
*I+, Standby (Note 5)	Full		0.5	2.0	mA
*I-, Standby (Note 5)	Full		0.02	1.0	mA

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = -100µA
2. Analog Overvoltage = ±33V
3. V_{EN} = 0.8V, R_L = 1K, C_L = 7pF, V_S = 3V RMS, f = 500KHz
4. V_{EN} = +4.0V
5. V_{EN} = 0.8V
6. To drive from DTL/TTL Circuits, 1KΩ pull-up resistors to +5.0V supply are recommended

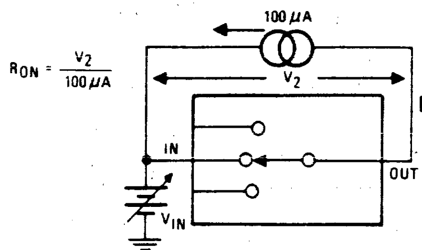
100% Tested for Dash 8 at +25°C and +125°C Only.

Truth Table

A_2	A_1	A_0	E_N	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

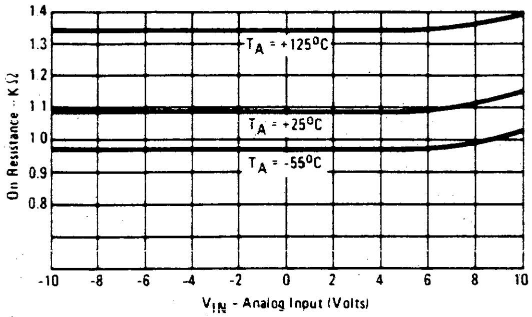
UNLESS OTHERWISE SPECIFIED: $T_A = 25^oC$, $V_{SUPPLY} = +15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$

TEST CIRCUIT NO. 1

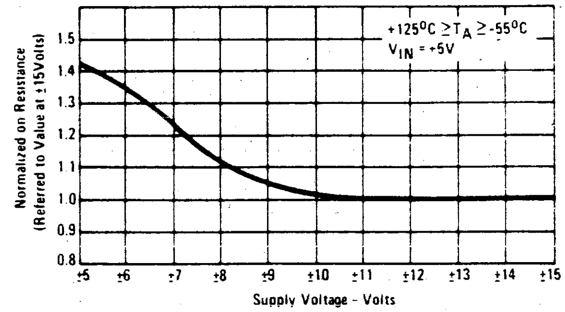


ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

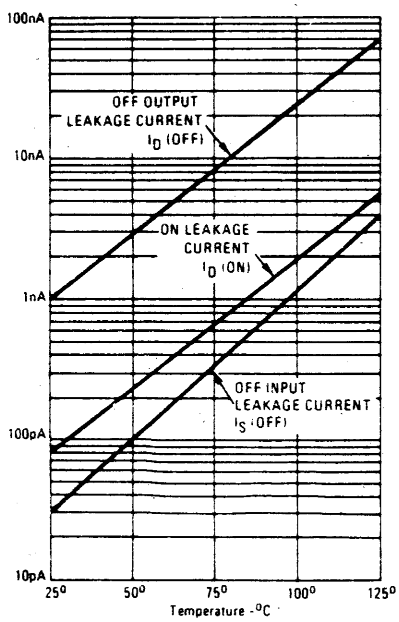
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE

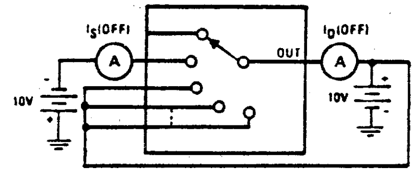


LEAKAGE CURRENT vs. TEMPERATURE



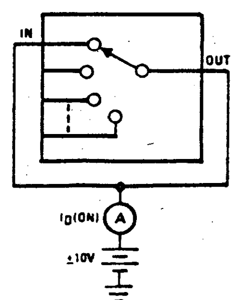
TEST CIRCUIT NO. 2

OFF LEAKAGE CURRENT vs. TEMPERATURE

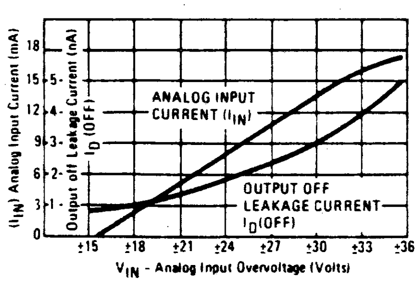


ON LEAKAGE CURRENT vs. TEMPERATURE

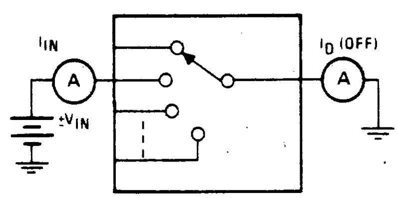
TEST CIRCUIT NO. 3



ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



TEST CIRCUIT NO. 4



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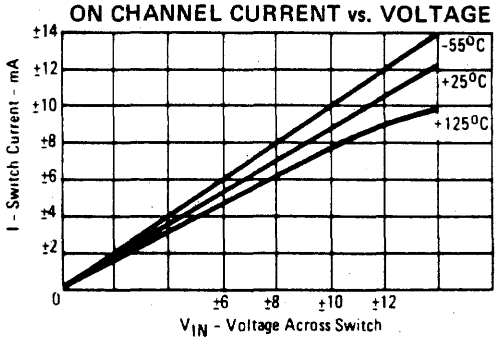
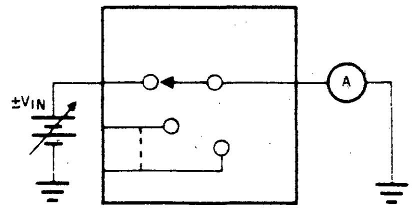
ON CHANNEL CURRENT vs. VOLTAGE



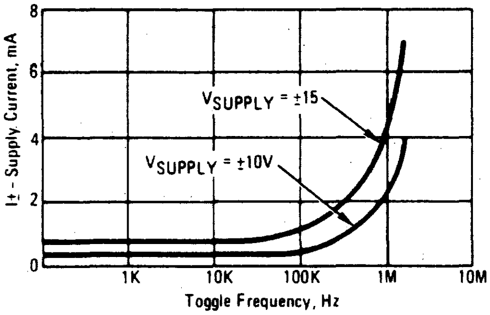
TEST CIRCUIT NO. 5

ON CHANNEL CURRENT vs. VOLTAGE

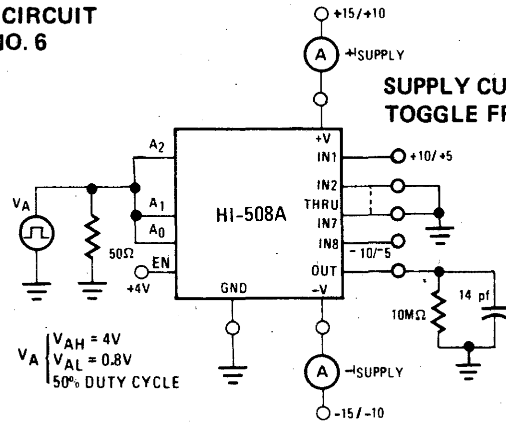


TEST CIRCUIT NO. 6

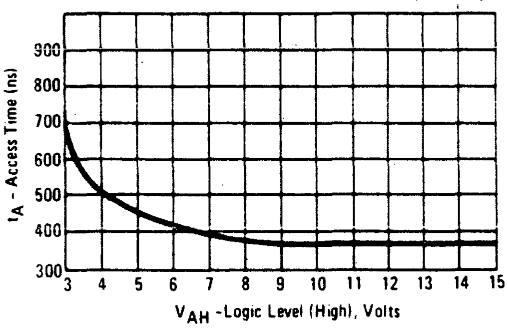
SUPPLY CURRENT vs. TOGGLE FREQUENCY



SUPPLY CURRENT vs. TOGGLE FREQUENCY

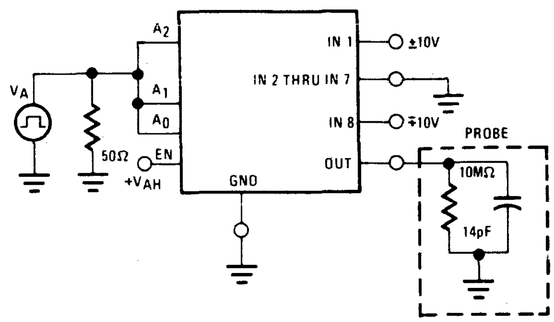


ACCESS TIME vs. LOGIC LEVEL (HIGH)

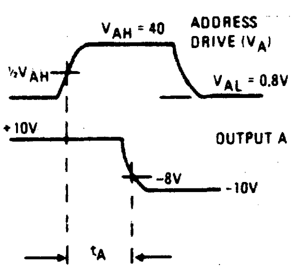


TEST CIRCUIT NO. 7

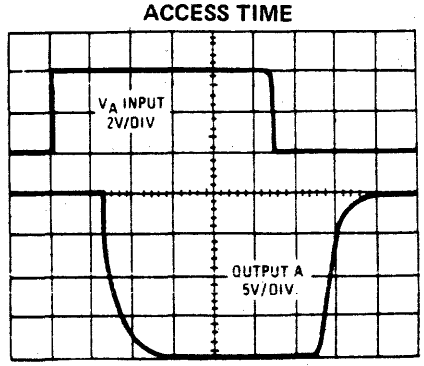
ACCESS TIME vs. LOGIC LEVEL (HIGH)



Switching Waveforms



ACCESS TIME



200ns/Div.

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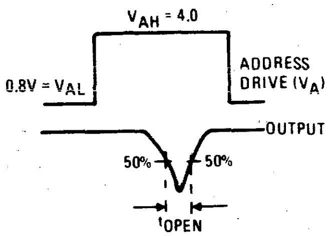
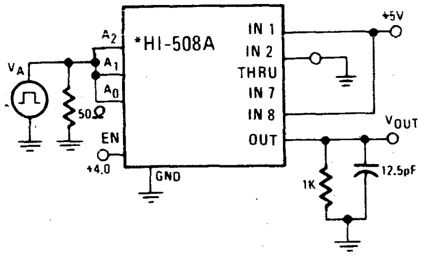
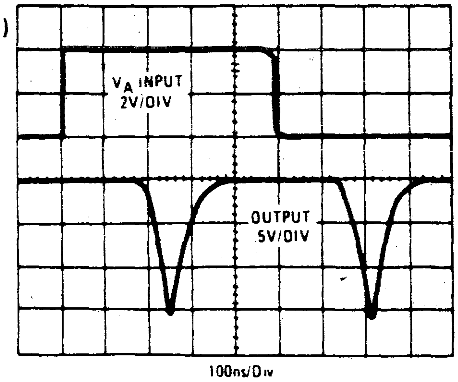
TEST CIRCUIT
NO. 8
BREAK BEFORE MAKE DELAY (t_{OPEN})

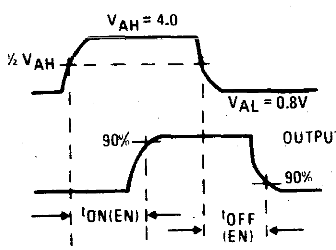


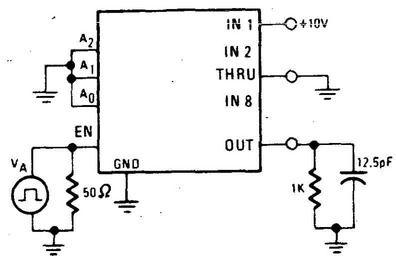


BREAK BEFORE MAKE DELAY (t_{OPEN})

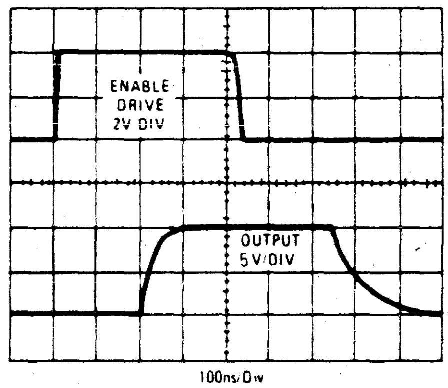


TEST CIRCUIT
NO. 9
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



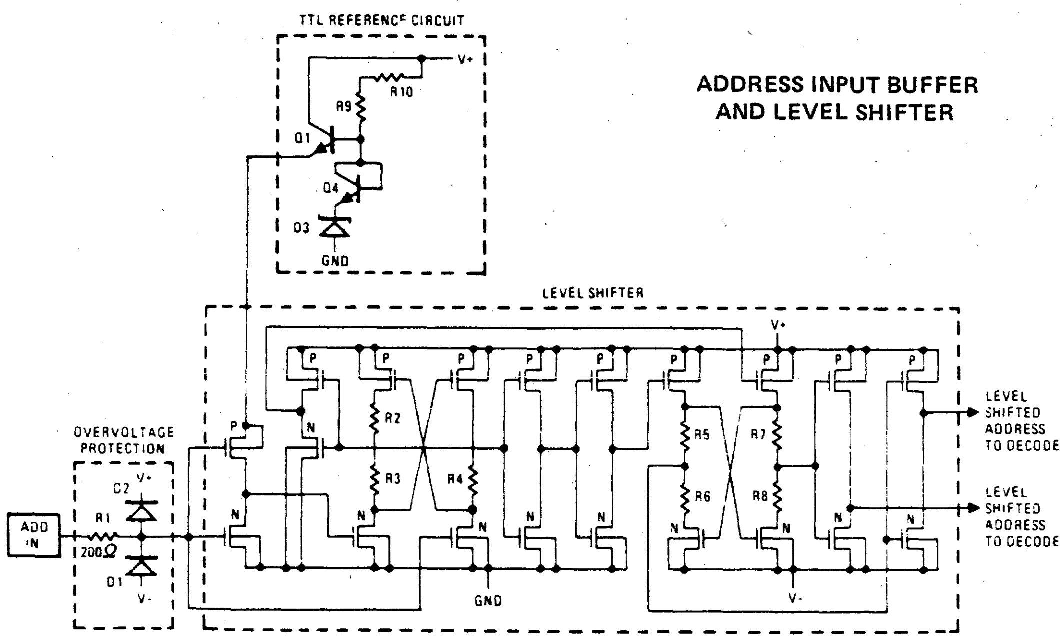


ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)

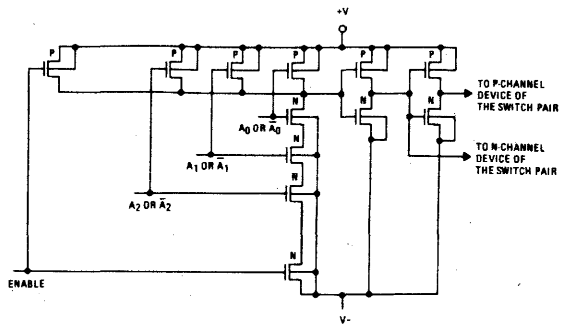


Schematic Diagrams

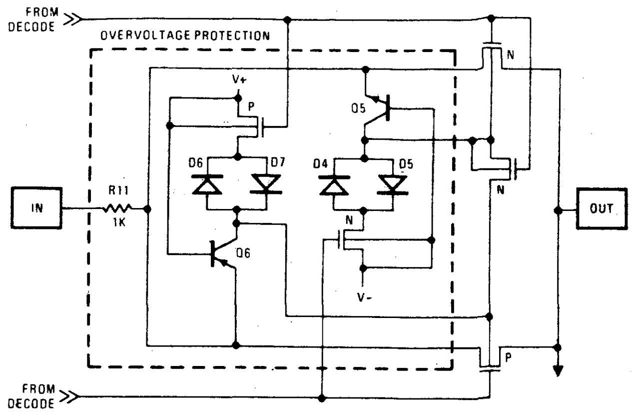
ADDRESS INPUT BUFFER AND LEVEL SHIFTER



ADDRESS DECODER



MULTIPLEX SWITCH



Radiation Screening Procedure

(1) Two (2) probed good samples per wafer will be selected from ≥20% of the wafers in a run. (All wafers in a "run" will have been processed together through all high temperature processing steps and through metallization.)

(2) The sample die shall be assembled and tested for functionality.

(3) The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^5 Rad (Si) ±10% from a Gamma Cell 220 Cobalt 60 source or equivalent. The devices will be powered in the configuration illustrated with V_{SUPPLY} = ±15V. The dose rate shall be between 50 rads/sec and 200 rads/sec.

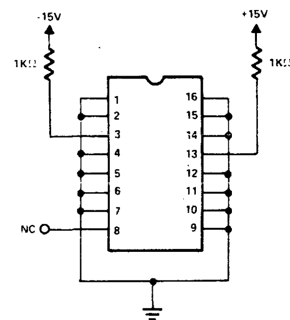
(4) On Current Leakage $I_{D(ON)}$ with V_{SUPPLY} = ±15V will be measured and recorded for each device within one hour after irradiation. The lot will be accepted only if the sample meets the limit of $I_{D(ON)} \leq 1\mu A$ when tested at 25°C.

Radiation Effects

(1) TOTAL DOSE:
Very little degradation of any of the parameters will be seen up to $\gamma = 1 \times 10^5$ Rad (Si).

(2) DOSE RATE:
The HS508A RH is manufactured in DI, consequently, it is latch up free.

Irradiation Bias Circuit



Sales Offices

UNITED STATES

EASTERN REGION

2600 Virginia Avenue
Suite 800
Washington, DC 20037
(202) 342-3900
TWX: 710-822-9301

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Burlington, MA 01803
(617) 273-1020
TWX: 710-332-1074

106 Seventh Street
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(516) 747-6776

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TWX: 910-576-3418

HOME OFFICE

P.O. Box 883
Melbourne, FL 32901
(305) 724-7045
TWX: 510-959-6259

EUROPEAN

Harris Systems Ltd.
Semiconductor Programs Divisior
P.O. Box 27
145 Farnham Road
Slough SL1 4XD
United Kingdom
Tel: 34666
TWX: 848174

HARRIS

CUSTOM INTEGRATED CIRCUITS DIVISION

HS-1840RH

HARRIS

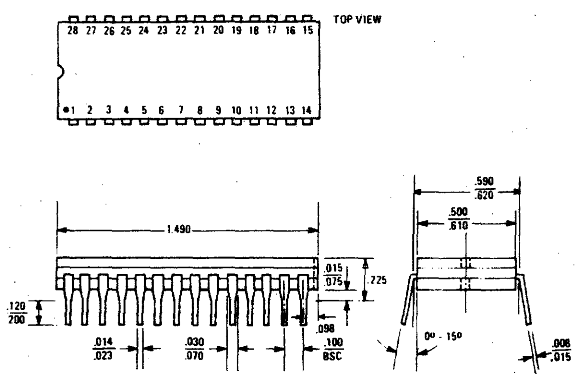
Preliminary

Radiation Resistant 16 Channel CMOS Analog Multiplexer with High-Z Analog Input Protection

Features

- HIGH ANALOG INPUT IMPEDANCE DURING POWER LOSS (OPEN) — 500MΩ
- LOW POWER CONSUMPTION (STANDBY) — 600μW
- ACCESS TIME — 500ns
- EXCELLENT IN HI-REL REDUNDANT SYSTEMS
- BREAK-BEFORE-MAKE SWITCHING
- NO LATCH-UP
- RADIATION ENVIRONMENT
  - NEUTRON FLUENCE (ϕ) . 1×10^9 n/cm^2(E $\geq$ 10KeV)
  - GAMMA RATE ($\dot{\gamma}$) . . . . 1×10^8 RADs (Si)/s
  - GAMMA DOSE (γ) . . . . 2×10^5 RADs(Si)

Package



Pinout

TOP VIEW

Pin	Function	Pin	Function
1	$+V_{SUPPLY}$	28	OUT
2	NC	27	$-V_{SUPPLY}$
3	NC	26	IN 8
4	IN 16	25	IN 7
5	IN 15	24	IN 6
6	IN 14	23	IN 5
7	IN 13	22	IN 4
8	IN 12	21	IN 3
9	IN 11	20	IN 2
10	IN 10	19	IN 1
11	IN 9	18	$\overline{ENABLE}$
12	GND	17	ADDRESS A_0
13	$(+5V_{SUPPLY})$ V_{REF}	16	ADDRESS A_1
14	ADDRESS A_3	15	ADDRESS A_2

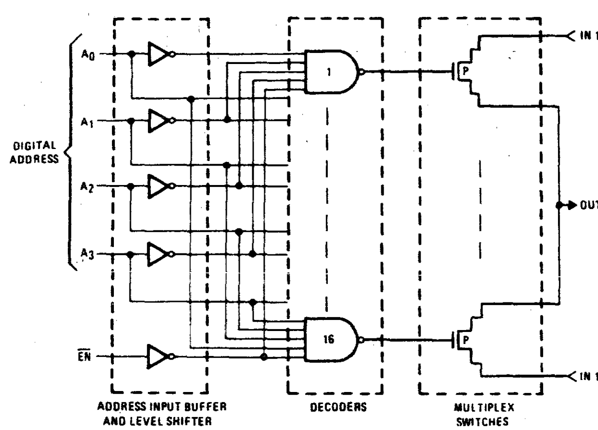
CAUTION: These devices are sensitive to electronic discharge.

Description

The HS-1840RH is a radiation resistant, monolithic 16 channel multiplexer constructed with the Harris Linear Dielectric Isolation CMOS process. It is designed to provide a high input impedance to the analog source if device power fails (open) or the analog signal voltage inadvertently exceeds the supply rails during powered operation. Excellent for use in redundant applications, since the secondary device can be operated in a standby unpowered mode affording no additional power drain. But more significantly, a very high impedance exists between the active and inactive devices preventing any interaction. One of sixteen channel selection is controlled by a 4-bit binary address plus an Enable-Inhibit input which conveniently controls the ON/OFF operation of several multiplexers in a system. All digital inputs have electrostatic discharge protection.

The HS-1840RH has been specifically designed to meet exposure to radiation environments. It is available in a 28 pin dual-in-line package and is guaranteed operational from −55°C to +125°C.

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 1 and 27 — +40V
V_{REF} to Ground — +20V
V_{EN}, V_A, Digital Input Overvoltage:
V_A: V_{REF} +4V; Ground −4V
Analog Input Overvoltage:
V_S: V_{Supply} (+) +20V; V_{Supply} (-) −20V

Total Power Dissipation* — 1200mW
Operating Temperature — -55°C to +125°C
Storage Temperature — -65°C to +150°C

*Derate 8mW/°C above T_A = +25°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified:
Supplies = +15V, -15V: V_{REF}(Pin 13) = +5V; V_{AH}(Logic Level High) = 4.0V; V_{AL}(Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics section.

PARAMETER	TEMP.	-55°C to +125°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS					
*V_S, Analog Signal Range	Full	-5		+15	V
*R_{ON}, On Resistance (Note 1) V_{IN} = +15V	Full		0.5	1.0	KΩ
V_{IN} = -5V	Full		2.5	5.0	KΩ
*I_S(OFF), Off Input Leakage Current	+25°C		0.03		nA
	Full			±100	nA
*I_S(OFF), with Power Off (Note 8)	Full			±100	nA
*I_D(OFF), Off Output Leakage Current	+25°C		1.0		nA
	Full			±1000	nA
* I_D(OFF), or I_S(OFF) with Input Overvoltage Applied (Note 2)	+25°C		50		nA
	Full			±1000	nA
*I_D(ON), On Channel Leakage Current	+25°C		1.0		nA
	Full			±1000	nA
DIGITAL INPUT CHARACTERISTICS					
V_{AL}, Input Low Threshold — TTL Drive (Note 7)	Full			0.8	V
V_{AH}, Input High Threshold — TTL Drive (Note 7)	Full	4.0			V
V_{AL} — MOS Drive (Note 3)	+25°C			0.8	V
V_{AH} — MOS Drive (Note 3)	+25°C	6.0			V
*I_A, Input Leakage Current (High or Low)	Full			1.0	μA
SWITCHING CHARACTERISTICS					
t_A, Access Time	+25°C		500	1000	ns
t_{OPEN}, Break-Before-Make Delay	+25°C	20	80		ns
t_{ON}(EN), Enable Delay (ON)	+25°C		300	1000	ns
t_{OFF}(EN), Enable Delay (OFF)	+25°C		300	1000	ns
Settling Time (0.1%)	+25°C		1.2		μs
(0.025%)	+25°C		4.1		μs
"Off Isolation" (Note 4)	+25°C		65		dB
C_S(OFF), Channel Input Capacitance	+25°C		5		pF
C_D(OFF), Channel Output Capacitance	+25°C		50		pF
C_A, Digital Input Capacitance	+25°C		5		pF
C_{DS}(OFF), Input to Output Capacitance	+25°C		0.15		pF
POWER REQUIREMENTS					
P_D, Power Dissipation (Note 5)	+25°C		0.6	15.0	mW
(Note 6)	+25°C		0.6	15.0	mW
*I+, Current Pin 1 (Note 5)	Full		0.02	0.5	mA
*I-, Current Pin 27 (Note 5)	Full		0.02	0.5	mA
*I+, Standby (Note 6)	Full		0.02	0.5	mA
*I-, Standby (Note 6)	Full		0.02	0.5	mA

Truth Table

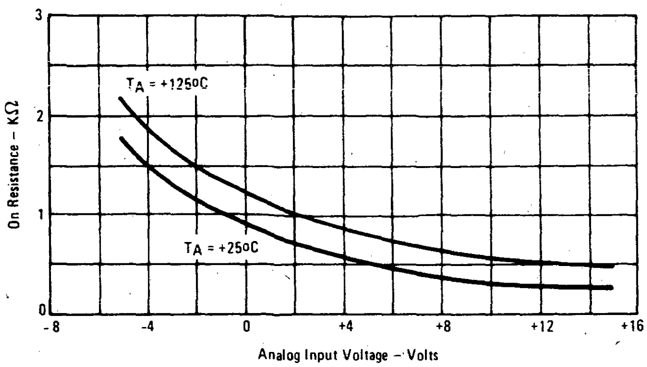
A_3	A_2	A_1	A_0	$\overline{EN}$	"ON" CHANNEL
X	X	X	X	H	NONE
L	L	L	L	L	1
L	L	L	H	L	2
L	L	H	L	L	3
L	L	H	H	L	4
L	H	L	L	L	5
L	H	L	H	L	6
L	H	H	L	L	7
L	H	H	H	L	8
H	L	L	L	L	9
H	L	L	H	L	10
H	L	H	L	L	11
H	L	H	H	L	12
H	H	L	L	L	13
H	H	L	H	L	14
H	H	H	L	L	15
H	H	H	H	L	16

NOTES:

1. I_{OUT} = 1mA
2. Analog Overvoltage = ±20V
3. V_{REF} = +10V
4. V_{EN} = 4.0V, R_L = 1K, C_L = 7pF, V_S = 3VRMS, f = 500kHz
5. V_{EN} = 0.8V
6. V_{EN} = 4.0V
7. To drive from DTL/TTL circuits 1K pull-up resistors to +5.0V supply are recommended
8. All supplies (V+, V−, +5V) and digital inputs (A_0, A_1, A_2, A_3, EN) opened. Analog input ±10V.

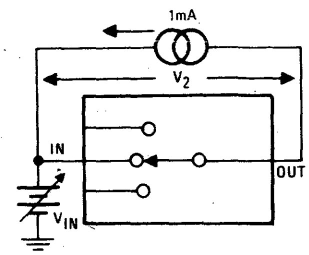
Unless Otherwise Specified: $T_A = 25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$ and $V_{REF} = 5V$.

ON RESISTANCE VS. ANALOG INPUT VOLTAGE

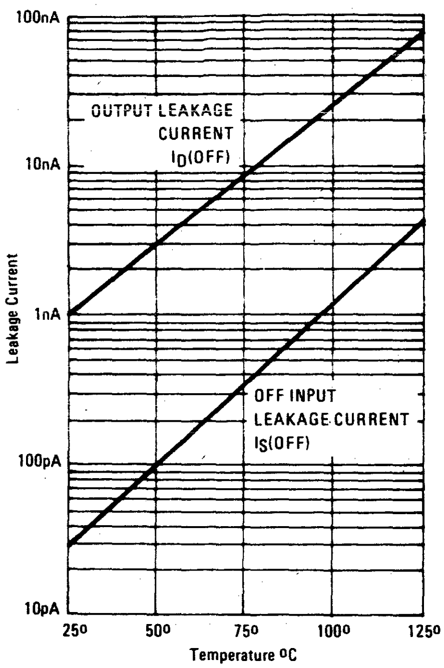


ON RESISTANCE vs INPUT SIGNAL LEVEL

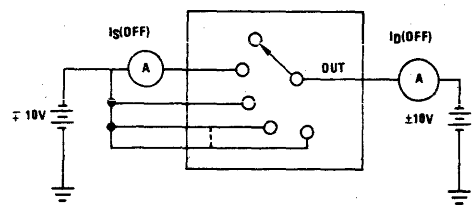
$$R_{ON} = \frac{V_2}{1mA}$$



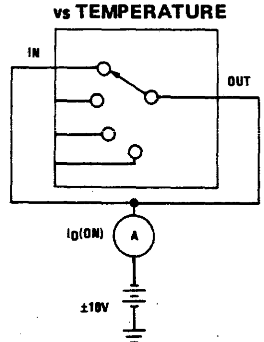
LEAKAGE CURRENT VS. TEMPERATURE



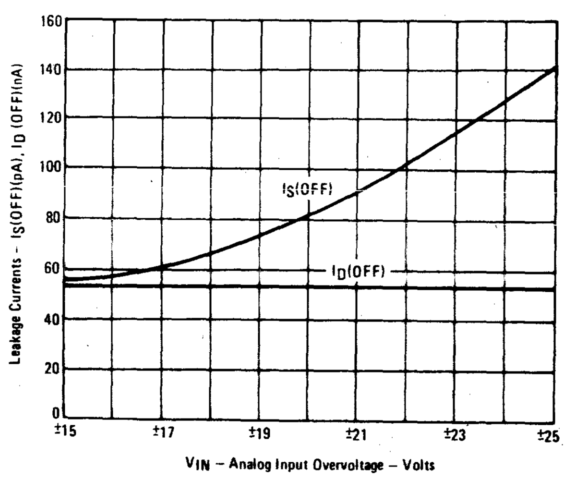
OFF LEAKAGE CURRENT vs TEMPERATURE



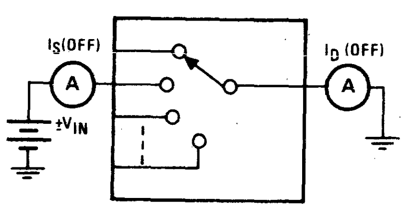
ON LEAKAGE CURRENT vs TEMPERATURE



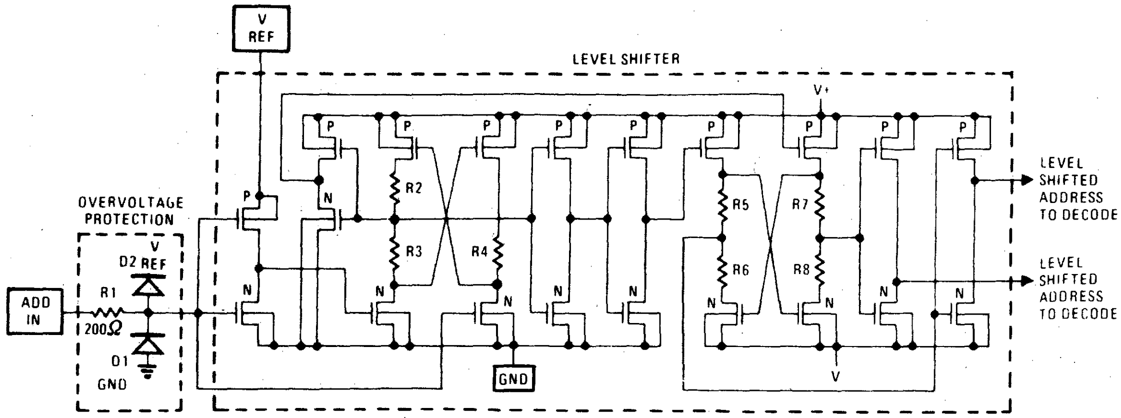
ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



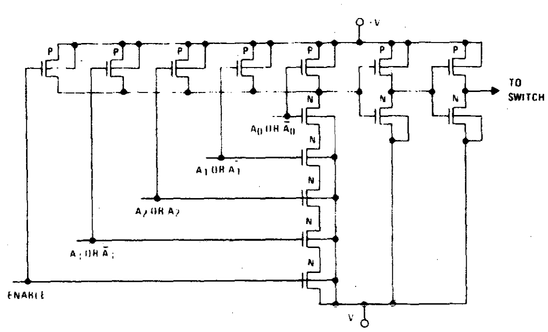
ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



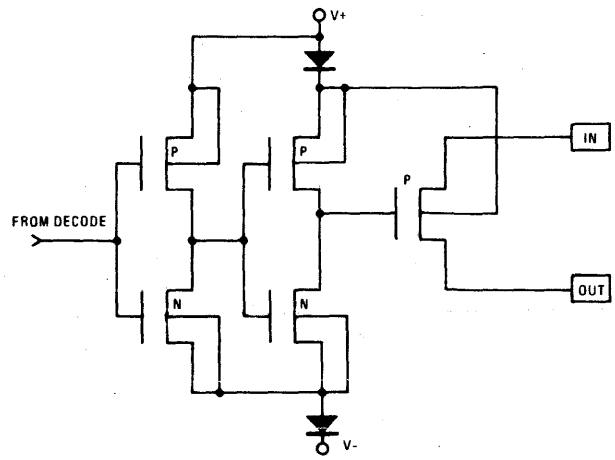
ADDRESS AND ENABLE INPUT BUFFER AND LEVER SHIFTER



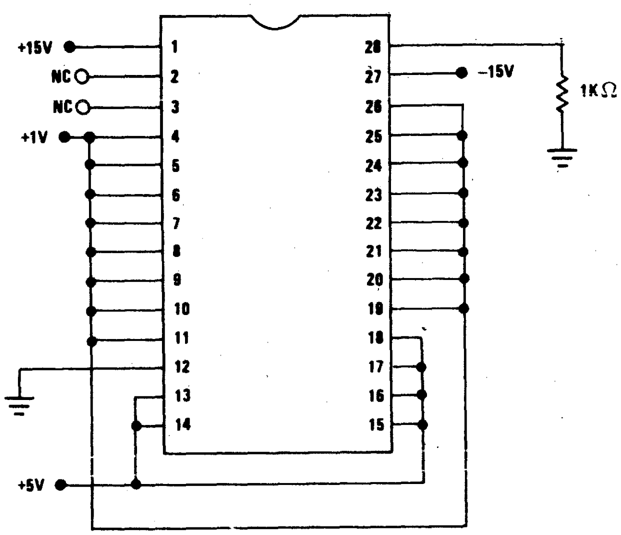
ADDRESS DECODER



MULTIPLEXER SWITCH



HS1840RH IRRADIATION CONFIGURATION



Radiation Screening Procedure

(1) Two (2) probed good die per wafer will be selected from $\geq$20% of the wafers in a run. (All wafers in a "run" will have been processed together through all high temperature processing steps and through metallization.)

(2) The sample die shall be assembled and tested for functionality.

(3) The sample devices shall be subjected to a Total Dose Radiation level of 2×10^5 Rad (Si) ± 10% from a Gamma Cell 220 Cobalt 60 source or equivalent. The devices will be powered in the configuration illustrated with V_{SUPPLY} = ±15V. The dose rate shall be between 50 rads/sec and 200 rads/sec.

(4) On Current Leakage $I_{D(ON)}$ with V_{SUPPLY} = ±15V will be measured and recorded for each device within one hour after irradiation. The lot will be accepted only if the sample meets the limit of $I_{D(ON)} \leq 1\ \mu A$ when tested at 25°C.

Radiation Effects

(1) TOTAL DOSE:
Very little degradation of any of the parameters will be seen up to $\gamma = 2 \times 10^5$ Rad (Si).

(2) DOSE RATE:
The HS-1840RH is manufactured in DI, consequently, it is latch up free.

Product Test Flow

HARRIS SEMICONDUCTOR PRODUCT FLOW
MIL-STD-883, METHOD 5004 CLASS B

100% SCREENING PROCEDURE

	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1010 Cond. C
4	Constant Acceleration	2001 Cond. E; Y1 plane
5	Seal: A Fine B Gross	1014 Cond. A or B 1014 Cond. C2
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. 125°C (or equivalent)
8	Final Electrical 100% go-no-go	Tested at Worst Case Operating Conditions
9	External Visual	2009 Sample Inspection

Note:

Traceability: All devices are assigned date code identification that provides traceability back to the inspection lot.

Branding: All devices are branded with the part number and EIA date code.

Aged Products: Product that has been held for more than 24 months will be reinspected prior to shipment to group A inspection requirements.

Additional Requirements: Sample Group A electrical tests are performed on a lot acceptance basis.

HARRIS

HGA-C00600
HGA-C01200
HGA-C02500

CMOS Gate Array

Features

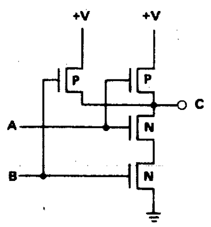
- 3 MICRON CMOS TECHNOLOGY
- 600, 1200, AND 2500 GATE ARRAYS
- 3ns TYPICAL GATE DELAY
- 50 MHz TOGGLE FREQUENCY
- 74LS- SSI, MSI LIBRARY IMPLEMENTED
- ADVANCED CAD TELEDESIGN™ SOFTWARE SUPPORT
- COMPATIBLE WITH DIAL-A-CHIP℠ DESIGN AUTOMATION SYSTEM
- INDIVIDUALLY PROGRAMMABLE I/O BUFFERS
- BI-DIRECTIONAL AND THREE STATE I/O
- TTL AND CMOS COMPATIBILITY
- COMMERCIAL TEMPERATURE RANGE
- MILITARY TEMPERATURE RANGE
- MULTIPLE PACKAGE OPTIONS

CMOS Gate Array Family

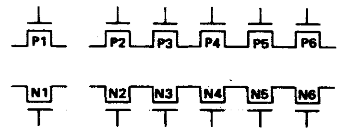
PART NO.	TRAN-SISTOR	GATE EQUIV.	DIE SIZE (MILS)	I/O PINS	ROWS/ CELLS
HGA-C00600	2592	648	198 X 165	54	6 X 36
HGA-C01200	5184	1296	257 X 198	78	12 X 36
HGA-C02500	10,080	2520	272 X 287	100	14 X 60

* One gate equivalent is equal to one 2-input nand.

TWO-INPUT NAND
1 GATE EQUIVALENT



BASIC CELL



Description

Harris Custom Integrated Circuits Division offers a complete family of custom and semicustom logic. The HGA-C00600, HGA-C01200 and HGA-C02500 are three CMOS gate arrays manufactured using the HARRIS state-of-the-art SAJI IV process. This local oxidation process offers 3 m channel lengths and 2 minimum features. Typical propagation gate delay is 3ns with 50MHz toggle frequencies possible. Personalization is accomplished by patterning two levels of interconnection on three mask layers: polysilicon, contacts and metal.

The entire process is fully supported by advanced CAD Teledesign™* software. With the HARRIS Dial-A-Chip℠** design automation system a customer chooses the amount of his participation in the design and development of his circuit. Using the HARRIS Teledesign™ timeshare system, logic description, simulation, and artwork editing can all be performed by the customer in his own office via a digital data communications link or if he so chooses, he may use the Customer Design Center in Melbourne.

The HARRIS system minimizes the amount of design and logic coding by offering a library of 74LS equivalent SSI and MSI function designs. There is no need to implement large MSI functions with primative gates. Each function has a complete data sheet specifying propagation delays and A. C. parameters. A final software program verifies that the original logic description matches the finished artwork.

Each input-output buffer can be individually specified to be input, output, three-state, or bi-directional. CMOS or TTL compatiblity can also be specified. The large number of I/O buffers keeps the input/output to gate ratio high insuring that the design is not pin limited.

Transition from gate arrays to standard cell circuits is very simple. The same logic description files are used as input to the Dial-A-Chip℠ software. Both utilize the same SSI, MSI 74LS library.

*Trademark of Harris Corporation
**Servicemark of Harris Corporation

HARRIS

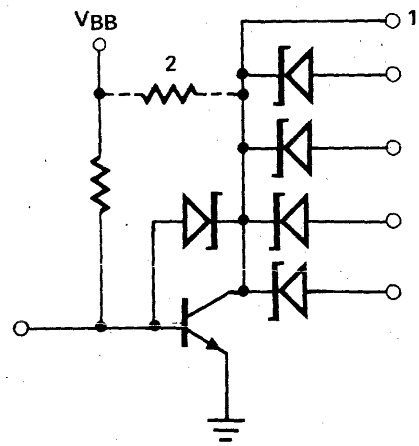
Advance

HGA-B01500
HGA-B02500

ASTL Gate Array

Features

- 3 MICRON TECHNOLOGY
- 1500, AND 2500 GATE ARRAYS
- 1.0ns TYPICAL GATE DELAY
- 150MHz TOGGLE FREQUENCY
- 74LS-SSI, MSI LIBRARY
- ADVANCED CAD TELEDESIGN™ SOFTWARE SUPPORT
- COMPATIBLE WITH DIAL-A-CHIP℠ DESIGN AUTOMATION SYSTEM
- INDIVIDUALLY PROGRAMMABLE I/O BUFFERS
- BI-DIRECTIONAL AND THREE STATE I/O
- TTL COMPATIBILITY
- COMMERCIAL TEMPERATURE RANGE
- MILITARY TEMPERATURE RANGE
- MULTIPLE PACKAGE OPTIONS
- 265 MICROWATTS PER GATE TYPICAL



Notes: 1. Ohmic contact for Common Base connections.
2. Collector Resistor Option for high Fan-Out. Refer to appropriate HBAXXX Data Sheets.

Harris Semiconductor

CUSTOM/SEMICUSTOM

Description

Harris Custom Integrated Circuits Division offers a complete family of custom and semi-custom logic. The HGA-B01500 and HGA-B02500 are ASTL gate arrays manufactured using the HARRIS state of the art advanced schottky transistor logic process. The process offers 10μm metal pitch and 3μm minimum features. Typical propagation gate delay is 1.0ns with 150MHz toggle frequencies possible. Personalization is accomplished by patterning two levels of aluminum interconnection on four mask layers.

The entire process is fully supported by advanced CAD Teledesign™* software. With the HARRIS Dial-A-Chip℠** design automation system a customer chooses the amount of his participation in the design and development of his circuit. Using the HARRIS Teledesign ™ software, logic description, simulation, and artwork editing can all be performed by the customer in his own office via a digital data communications link or if he so chooses, he may use the Customer Design Center in Melbourne.

The HARRIS system minimizes the amount of design and logic coding by offering a library of 74LS equivalent SSI and MSI function designs. There is no need to design large MSI functions with primitive gates. Each function has a complete data sheet specifying propagation delays and A.C. parameters. A final software program verifies that the original logic description matches the finished artwork.

Each input-output buffer can be individually specified to be input, output, three-state, or bi-directional. The large number of I/O buffers keeps the gate to input/output ratio low insuring that the design is not pin limited.

Transition from gate arrays to a standard cell design is very simple. The same logic description files are used as input to the Teledesign™ software. Both utilize the same SSI, MSI 74LS library, functions.

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Semicustom Capabilities

HCA SSI/MSI LIBRARY

For use with HARRIS CMOS Gate Array
and Standard Cell Family

HCA000XB	DUAL 2 INPUT NAND
HCA000IB	DUAL 2 INPUT NAND WITH INVERTER
HCA002XB	DUAL 2 INPUT NOR
HCA002IB	DUAL 2 INPUT NOR WITH INVERTER
HCA004XB	TRIPLE INVERTER
HCA007XB	HIGH FANOUT BUFFER (5 pF DRIVE)
HCA008XB	2 INPUT AND
HCA010XB	3 INPUT NAND
HCA011XB	3 INPUT AND
HCA020XB	4 INPUT NAND
HCA021XB	4 INPUT AND
HCA027XB	3 INPUT NOR
HCA029XB	6 INPUT NAND
HCA030XB	8 INPUT NAND
HCA032XB	2 INPUT OR
HCA051XB	4 INPUT AND-OR-INVERT GATE
HCA073XB	JK FLIP FLOP WITH RESET
HCA074RB	D FLIP FLOP WITH RESET
HCA074SB	D FLIP FLOP WITH SET
HCA074XB	D FLIP FLOP WITH SET AND RESET
HCAN74RB	D FLIP FLOP WITH RESET—NEGATIVE EDGE TRIGGERED
HCAN74SB	D FLIP FLOP WITH SET—NEGATIVE EDGE TRIGGERED
HCAN74XB	D FLIP FLOP WITH SET AND RESET—NEGATIVE EDGE TRIGGERED
HCA075XB	QUAD D TYPE LATCH WITH INDIVIDUAL RESETS
HCA083SB	BCD FULL ADDER
HCA085XB	4-BIT MAGNITUDE COMPARATOR
HCA086XB	2 INPUT EXCLUSIVE OR
HCA138XB	3 TO 8 LINE DECODER
HCA139XB	2 TO 4 LINE DECODER
HCA152XB	8 TO 1 DATA SELECTOR
HCA157XB	QUAD 2 TO 1 DATA SELECTOR
HCA161XB	4-BIT SYNCHRONOUS BINARY COUNTER WITH ASYNCHRONOUS RESET
HCA163XB	4-BIT SYNCHRONOUS BINARY COUNTER WITH SYNCHRONOUS RESET
HCA164XB	8-BIT PARALLEL OUTPUT SHIFT REGISTER
HCA165XB	8-BIT PARALLEL LOAD SHIFT REGISTER
HCA173XB	4-BIT D REGISTER WITH THREE STATE OUTPUTS
HCA175XB	QUAD D FLIP FLOP WITH RESET
HCA180XB	9-BIT PARITY GENERATOR
HCA192XB	4-BIT SYNCHRONOUS UP DOWN DECADE COUNTER
HCA193XB	4-BIT SYNCHRONOUS UP DOWN BINARY COUNTER
HCA194XB	4-BIT SYNCHRONOUS LOAD BI-DIRECTIONAL SHIFT REGISTER
HCA225XB	EXPANDABLE 4 WORD BY 1 BIT FIFO
HCA240XB	OCTAL INVERTING THREE STATE BUFFER
HCA244XB	OCTAL NON-INVERTING THREE STATE BUFFER
HCA257XB	QUAD 2 TO 1 LINE DATA SELECTOR
HCA273XB	OCTAL D FLIP FLOP WITH COMMON CLOCK
HCA283XB	4-BIT BINARY FULL ADDER WITH FAST CARRY
HCA352XB	DUAL 4 TO 1 LINE DATA SELECTOR
HCA377XB	OCTAL D FLIP FLOP WITH ENABLE
HCA393XB	4-BIT BINARY RIPPLE COUNTER
HCA645XB	OCTAL BUS TRANSCEIVER
HCA1000B	15:1 RATIO PULL UP RESISTOR WITH ENABLE

Semicustom Capabilities

HCA SSI/MSI LIBRARY

For use with HARRIS CMOS Gate Array
and Standard Cell Family

GATE ARRAY I/O BUFFERS

HCA900XB	CMOS INPUT BUFFER
HCA901XB	CMOS INPUT BUFFER WITH 18K PULL UP RESISTOR
HCA910XB	TTL INPUT BUFFER
HCA911XB	TTL INPUT BUFFER WITH 18K PULL UP RESISTOR
HCA950XB	3.2 MA OUTPUT BUFFER
HCA951XB	3.2 MA OUTPUT BUFFER—OPEN DRAIN P-CHANNEL
HCA952XB	3.2 MA OUTPUT BUFFER—OPEN DRAIN N-CHANNEL
HCA960XB	3.2 MA OUTPUT BUFFER—THREE STATE
HCA970XB	3.2 MA BI-DIRECTIONAL BUFFER—CMOS INPUT
HCA971XB	3.2 MA BI-DIRECTIONAL BUFFER—CMOS INPUT WITH 18K PULL UP
HCA980XB	3.2 MA BI-DIRECTIONAL BUFFER—TTL INPUT
HCA981XB	3.2 MA BI-DIRECTIONAL BUFFER—TTL INPUT WITH 18K PULL UP RESISTOR
HCAVSSXB	PLACEABLE VSS I/O PAD
HCAVIA	VIA CELL

STANDARD CELL I/O BUFFERS

HCC900XB	CMOS INPUT BUFFER
HCC901XB	CMOS INPUT BUFFER WITH 18K PULL UP
HCC905XB	CMOS INPUT BUFFER—INVERTING
HCC906XB	CMOS INPUT BUFFER—INVERTING WITH PULL UP
HCC908XB	SCHMITT TRIGGER INPUT BUFFER
HCC910XB	TTL INPUT BUFFER
HCC911XB	TTL INPUT BUFFER WITH 18K PULL UP
HCC915XB	TTL INPUT BUFFER WITH 18K PULL UP INVERTING
HCC950XB	3.2 MA OUTPUT BUFFER
HCC951XB	3.2 MA OUTPUT BUFFER WITH OPEN DRAIN P-CHANNEL
HCC952XB	3.2 MA OUTPUT BUFFER WITH OPEN DRAIN N-CHANNEL
HCC955XB	8.0 MA OUTPUT BUFFER
HCC960XB	3.2 MA OUTPUT BUFFER THREE STATE
HCC965XB	8.0 MA OUTPUT BUFFER THREE STATE
HCC970XB	3.2 MA BI-DIRECTIONAL WITH CMOS INPUT
HCC971XB	3.2 MA BI-DIRECTIONAL CMOS INPUT AND 18K PULL UP
HCC975XB	8.0 MA BI-DIRECTIONAL WITH CMOS INPUT
HCC976XB	8.0 MA BI-DIRECTIONAL CMOS INPUT AND 18K PULL UP
HCC980XB	3.2 MA BI-DIRECTIONAL TTL INPUT
HCC981XB	3.2 MA BI-DIRECTIONAL TLL INPUT AND 18K PULL UP
HCC985XB	8.0 MA BI-DIRECTIONAL TTL INPUT
HCC986XB	8.0 MA BI-DIRECTIONAL TTL INPUT AND 18K PULL UP
HCC990XB	UNBUFFERED INPUT WITH STATIC PROTECTION
HCCVDDYB	VDD SUPPLY PAD
HCCVSSYB	VSS SUPPLY PAD

HARRIS

HSC-CXXXXX

Standard Cell

Features

- 3 MICRON CMOS TECHNOLOGY
- VARIABLE DIE SIZE
- 3ns TYPICAL GATE DELAY
- 50MHz TOGGLE FREQUENCY
- 74LS-SSI, MSI LIBRARY IMPLEMENTED
- ADVANCED CAD TELEDESIGN™* SOFTWARE SUPPORT
- VARIABLE DIE SIZE
- INDIVIDUALLY PROGRAMMABLE I/O BUFFERS
- COMPATIBLE WITH DIAL-A—CHIP℠** DESIGN AUTOMATION SYSTEM
- BI-DIRECTIONAL AND THREE STATE I/O
- TTL AND CMOS COMPATIBILITY
- COMMERCIAL TEMPERATURE RANGE
- MILITARY TEMPERATURE RANGE
- MULTIPLE PACKAGE OPTIONS

Description

Harris Custom Integrated Circuits Division offers a complete family of custom and semicustom products. The HARRIS Standard Cell product is a very cost effective alternative to gate arrays or full custom. The standard cell circuit is manufactured using the HARRIS state-of-the-art SAJI IV local oxidation process. The process offers 3 μm channel lengths with typical gate delays of 3ns and toggle frequencies of 50MHz. Each input-output buffer can be individually programmed as input, output, three-state or bi-directional. CMOS and TTL compatibility can be specified. The same SSI MSI 74LS functions used to design the gate array are used for the standard cell circuits.

The logic description and simulator functions are identical for both standard cell circuits and gate arrays. However, the standard cell circuit dimensions can change dynamically for each individual circuit. Where the gate array is a fixed number of gates and fixed chip size, the standard cell uses only enough silicon to fully implement the desired logic function. Typically a standard cell chip is 30% smaller than a fully utilized gate array offering a cost savings benefit to those customers with medium to high volumes.

The standard cell chip does require a complete set of masks rather than the three required by the gate array. The standard cell circuit is fully supported by the HARRIS Teledesign™ software and the HARRIS Dial-A-Chip℠ timeshare service. This allows the customer to perform as much of the design and development as he desires from his own office with a data terminal.

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LINEAR MONOCHIPS

Designation	Technology	Size-Mils	Components	Voltage	Pads	Integration Fee
MOA	Bipolar	71 x 81	260	20V max	16 max	$3700
MOB	"	81 x 81	300	20V max	24 max	$3700
MOC	"	51 x 56	110	20V max	14 max	$2800
MOD	"	80 x 80	194	36V max	16 max	$3700
MOE	"	70 x 70	187	20V max	18 max	$3100
MOF	"	91 x 110	437	20V max	24 max	$4500
MOG	"	75 x 78	310	20V max	18 max	$3400
MOH	"	77 x 88	382	20V max	18 max	$3400
MOJ	"	61 x 65	170	20V max	18 max	$2800
MOL	"	81 x 100	416	20V max	24 max	$3900
MOM	"	101 x 151	812	20V max	28 max	$7000
MON	"	123 x 157	1070	20V max	40 max	$9000
MOP	"	90 x 121	623	20V max	24 max	$5000
MOQ	"	73 x 76	304	20V max	18 max	$3400
MLA	CMOS	136 x 185	1695	3 to 15V	42 max	$8500

DIGITAL MONOCHIPS

Designation	Technology	Size-Mils	Logic Cells	Gates	Gate Delay	Gate Power	Voltage	Pads	Integration Fee
MUA	Bipolar	131 x 131	225	450	25ns	2.0mW	*1 to 1.5V	40 max	$6500
MUB	"	"	"	"	200ns	0.2mW	"	"	"
MUC	"	"	"	"	10ns	2.5mW	"	"	"
MSA	"	157 x 157	"	"	8ns	1mW	5V max	"	$7000
MSB	"	200 x 186	440	880	"	"	"	52 max	$10000
MSC	"	191 x 205	990	1980	"	"	"	64 max	$15000
MCA	CMOS	112 x 124	112	140	13ns	<5μW**	3 to 15V	32 max	$5500
MCB	"	136 x 136	162	200	"	"	"	38 max	$5500
MCC	"	136 x 174	216	270	"	"	"	44 max	$6500
MCD	"	174 x 174	224	440	"	"	"	52 max	$7000
MCE	"	136 x 174	160	340	"	"	"	44 max	$6500
MCF	"	195 x 197	504	630	"	"	"	60 max	$8000
MCG	"	219 x 216	640	800	"	"	"	68 max	$9000
MPA	Si-CMOS	135 x 156	408	510	3.5ns	.14mW***	7V max	60 max	$7000
MPB	"	166 x 207	800	1000	"	"	"	78 max	$11000
MPC	"	196 x 239	1200	1500	"	"	"	95 max	$13000
MPD	"	234 x 251	1600	2000	"	"	"	109 max	$15000
MPE	"	90 x 112	120	150	"	"	"	36 max	$5500

*1 volt requires close work with Interdesign. **Frequency dependent, gate power at low frequency.
***Bipolar power at max frequency, CMOS at max frequency.

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Intersil

The IGC10000 Series CMOS Gate Arrays

FEATURES

- **Complexity from 408 to 1500 Equivalent 2-input Gates**
- **Mature Silicon Gate CMOS Technology**
  - **—Low development cost**
  - **—3.3 to 9V nominal power supply range ±10%**
  - **—Full CMOS temperature range: −55°C to +125°C**
  - **—Resistance to latch-up and electrostatic discharge**
- **Extensive Macro Cell Library**
  - **—Numerous combinational and sequential macros**
  - **—Facilitates 7400 and 4000-based designs**
  - **—TTL or CMOS compatible I/O**
  - **—Analog capability**
- **Fully Integrated CAD Software Support**
  - **—Highly efficient auto-routing capability**
  - **—Layout fully verified against input logic**
  - **—Accurate post-layout simulation with calculated RC delays**
  - **—Automatic test code conversion**

GENERAL DESCRIPTION

An IGC10000 Gate Array is a matrix of identical cells, each containing 3 uncommitted N-P transistor pairs. Large numbers of identical arrays are prefabricated and stockpiled. A particular circuit is constructed from a prefabricated array by specifying the interconnections among the transistors within and between cells on the final metal layer. Because all except the final metal layer are prefabricated, the cost advantages of mass production can be realized even for low-volume applications. In addition, prefabrication provides a saving in both design and manufacturing time; in some cases customers can receive prototype chips in as few as 6 weeks after initiation of the project.

In most cases IGC10000 gate arrays are processed with one mask step (a customized metal mask along with a standardized contact mask). For some analog applications or where more routing flexibility is needed, users have the option of programming the contact mask in addition to the metal mask.

THE IGC10000 FAMILY OF GATE ARRAYS

Figure 1 shows a structural representation of an IGC10000 Gate Array. Each rectangle in the body of the matrix represents an array cell; the rectangles

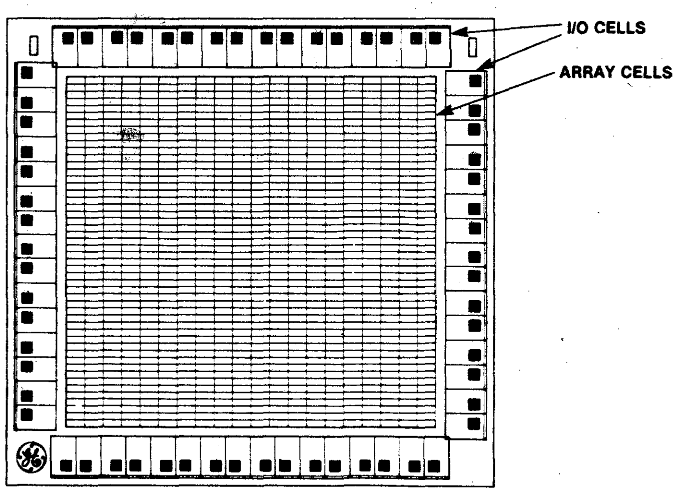

Figure 1. Gate Array Configuration

along each of the four sides of the chip represent I/O cells. Table 1 lists the members of the IGC10000 Gate Array family with their capacities and cell counts.

Table 1. The IGC10000 Gate Array Family

Part No.	Equivalent 2-Input Gates	Number of Array Cells	Bonding Pads and I/O Cells
IGC10408	408	272	34
IGC10756	756	504	44
IGC11500	1500	1000	62

TECHNOLOGY

IGC10000 gate arrays are fabricated using Intersil's high performance selectively oxidized 4-micron silicon gate CMOS process with single-layer metal interconnect. Wafers are processed using state-of-the-art processing technology with these features:

- Positive photoresist
- 1-1 scanning projection lithography
- Polysilicon, nitride and silicon dioxide plasma etching
- Ion implantation for source/drain doping and threshold adjustment
- Sputter metal deposition
- Industry standard oxidation and diffusion techniques
- Nitride and polysilicon Low Pressure Chemical Vapor Deposition (LPCVD)

ARRAY CELLS

An array cell, shown in topographical form in Figure 2, consists of three complementary transistor pairs and five strips of polysilicon (called crossunder strips) for making horizontal interconnections among array cells. Power (V_{DD}) and ground (V_{SS}) buses run vertically as shown. Metal strips (not shown) on top of the crossunder strips make the vertical interconnections within the array. The top and bottom polysilicon strips (called feed-throughs) are used for feeding horizontal connections through the array cell beneath the power and ground buses.

Figure 3 shows the circuit diagram for the array cell. Small hollow circles represent possible connection points; V_{SS} and V_{DD} metal strips are shown as dotted lines.

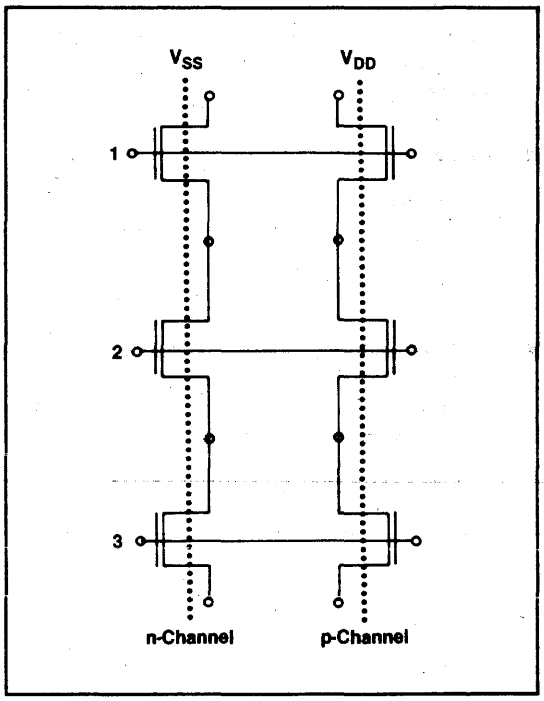

Figure 3. Schematic Diagram of the Array Cell

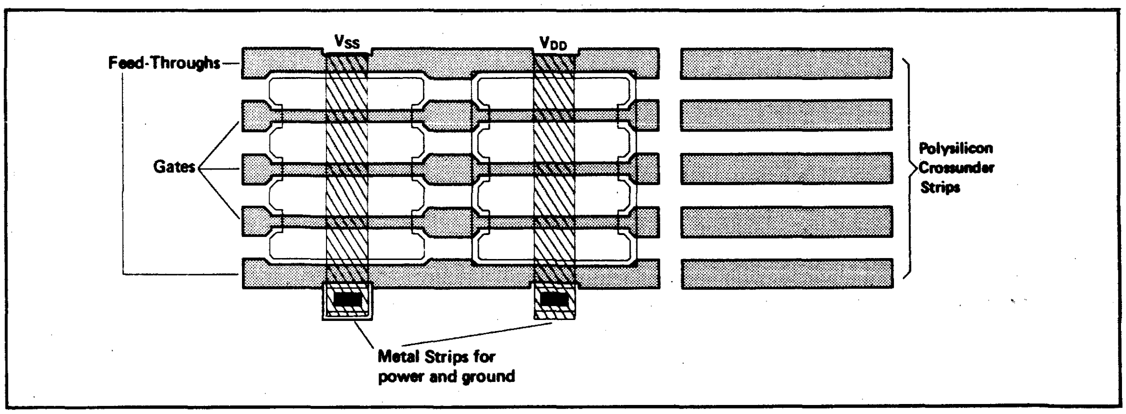

Figure 2. Topography of the Array Cell

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I/O CELLS

I/O cells are used to interface the array with external circuitry. Each I/O cell consists of an array of transistors of varying sizes, and allows construction of normal digital I/O interface circuits as well as analog circuitry of simple to moderate complexity.

I/O cells have these features:

- Protection against electrostatic discharge (ESD)
- Logic level translation (CMOS-to-TTL and TTL-to-CMOS)
- Bonding pad for connecting the cell to its corresponding package pin
- Ratioed transistors for analog implementation

The output drive capability of a single output buffer is one TTL load. Applications that require additional drive capability can be handled by using multiple I/O cells in parallel. (In a typical application, not all available I/O cells are needed for external connections; unused cells will thus usually be available to provide added drive capability where needed.)

MACROS

A macro is a physical implementation of a functional block and is realized by interconnections among transistors in one or more array cells. For example, the NOR function is constructed by connecting two p-channel transistors in series to V_{DD} and two n-channel transistors in parallel to V_{SS}, as shown in the topographical and schematic diagrams, Figures 4 and 5.

Designers implement their circuits by selecting and interconnecting the macros in the Macro Library, listed in Table 2.

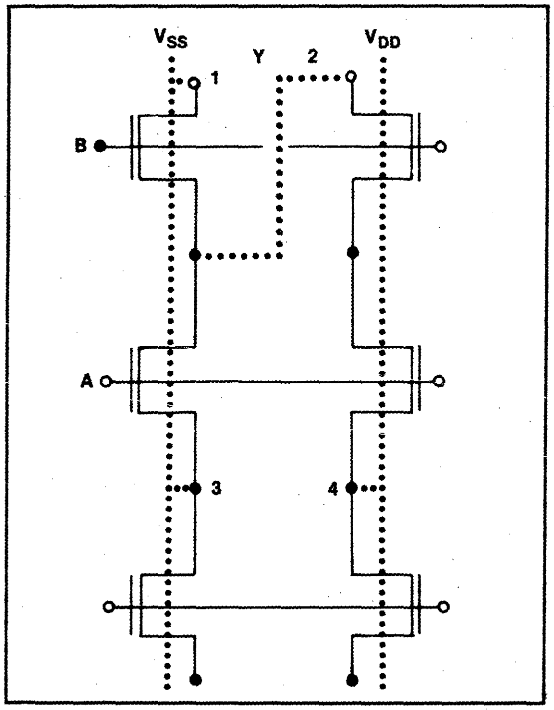

Figure 5. Schematic Diagram for the 2-Input NOR

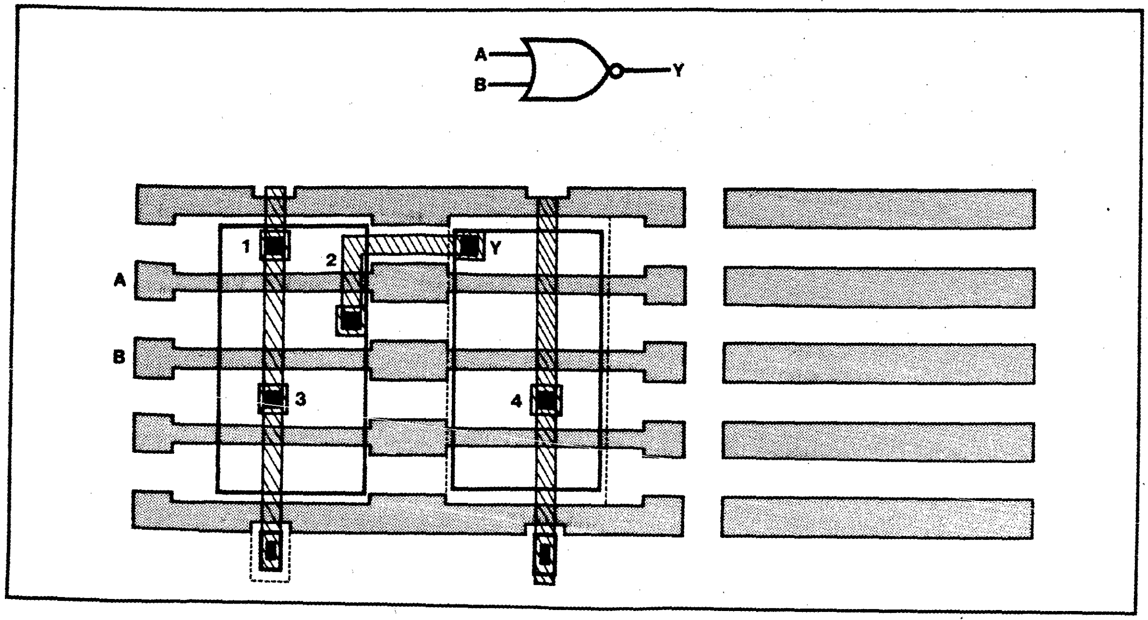

Figure 4. Interconnect Pattern for the 2-Input NOR

Table 2. IGC10000 MACRO Library

IGC10000 Combinational Macros	
Type	**Description**
NOR/NAND	2-input NAND 3-input NAND 4-input NAND 2-input NOR 3-input NOR 4-input NOR
XOR/XNOR	2-input XOR 2-input XNOR
Adder	One-bit full adder
Buffers and Inverters	1X inverter 2X inverter 3X inverter 4X inverter
Multifunction	2-1 AND-OR invert 2-2-2 AND-OR invert 3-2 AND-OR invert 2-1 OR-AND invert
Multiplexer	2 to 1 multiplexer
Schmitt Trigger	Schmitt Trigger
Transmission Gate	Buffered transmission gate Unbuffered transmission gate
Tristate Control	Tristate control

IGC10000 Sequential Macros		**Set**	**Reset**	**Jam Load**
D Flip-Flops	D flip-flop with reset	—	Yes	—
	D flip-flop with set	Yes	—	—
	D flip-flop with set and reset	Yes	Yes	—
	Divide by 2 flip-flop w/jam load and reset	—	Yes	Yes
	Divide by 2 flip-flop w/reset	—	Yes	—
	D flip-flop w/jam load and reset	—	Yes	Yes
	D flip-flop shift register with reset	—	[illegible]	[illegible]
JK Flip-Flops	JK flip-flop with reset	[illegible]	[illegible]	[illegible]
	JK flip-flop with [illegible]	[illegible]	[illegible]	[illegible]
T Flip-Flops	[illegible]	[illegible]	[illegible]	[illegible]
	[illegible]	[illegible]	Yes	—
	[illegible]	—	Yes	Yes
	[illegible]	—	Yes	—
	[illegible] counter w/jam load and reset	—	Yes	Yes
	Up/down counter with reset	—	Yes	—
	Up/down counter w/jam load and reset	—	Yes	Yes

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I/O CELLS

I/O cells are used to interface the array with external circuitry. Each I/O cell consists of an array of transistors of varying sizes, and allows construction of normal digital I/O interface circuits as well as analog circuitry of simple to moderate complexity.

I/O cells have these features:

- Protection against electrostatic discharge (ESD)
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- Bonding pad for connecting the cell to its corresponding package pin
- Ratioed transistors for analog implementation

The output drive capability of a single output buffer is one TTL load. Applications that require additional drive capability can be handled by using multiple I/O cells in parallel. (In a typical application, not all available I/O cells are needed for external connections; unused cells will thus usually be available to provide added drive capability where needed.)

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A macro is a physical implementation of a functional block and is realized by interconnections among transistors in one or more array cells. For example, the NOR function is constructed by connecting two p-channel transistors in series to V_{DD} and two n-channel transistors in parallel to V_{SS}, as shown in the topographical and schematic diagrams, Figures 4 and 5.

Designers implement their circuits by selecting and interconnecting the macros in the Macro Library, listed in Table 2.

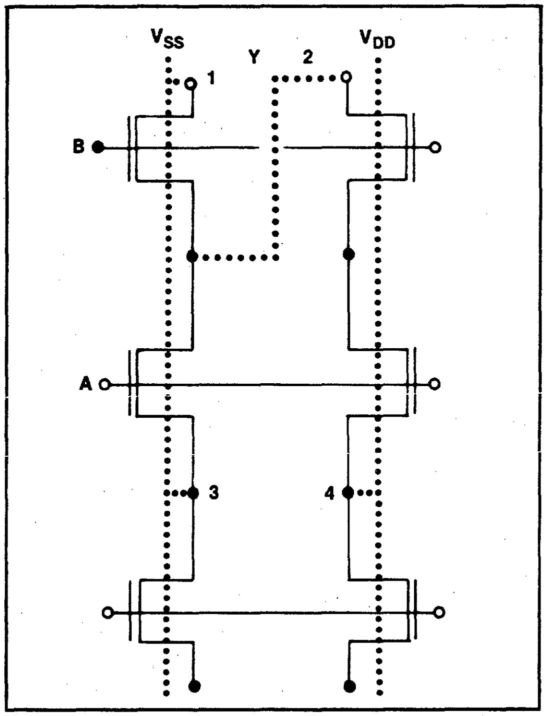

Figure 5. Schematic Diagram for the 2-Input NOR

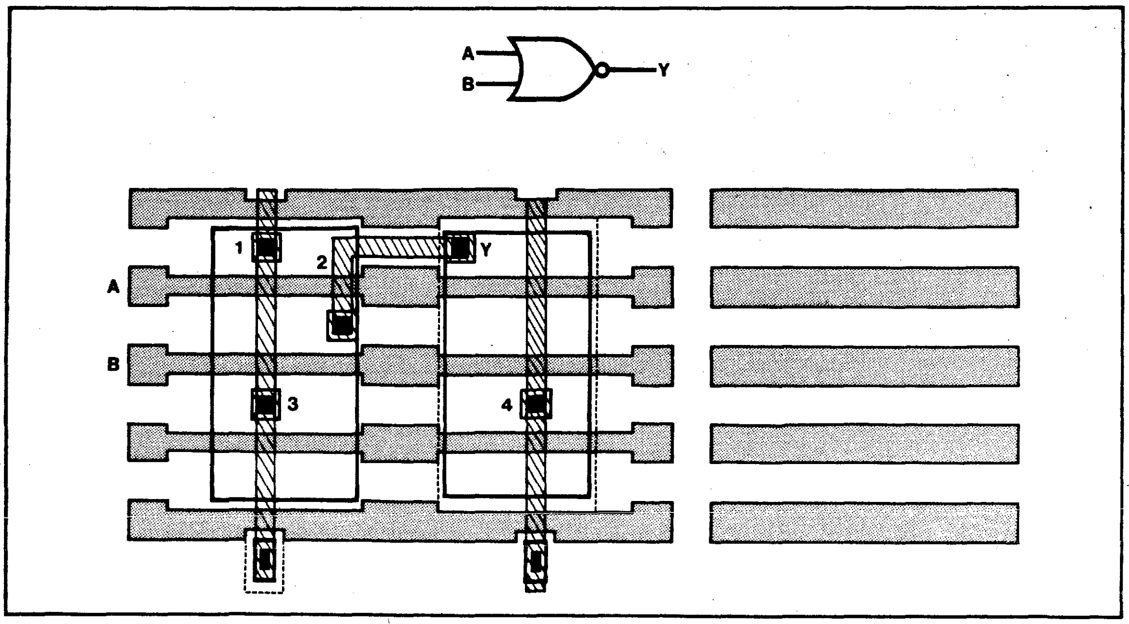

Figure 4. Interconnect Pattern for the 2-Input NOR

Table 2. IGC10000 MACRO Library

IGC10000 Combinational Macros

Type	Description
NOR/NAND	2-input NAND
	3-input NAND
	4-input NAND
	2-input NOR
	3-input NOR
	4-input NOR
XOR/XNOR	2-input XOR
	2-input XNOR
Adder	One-bit full adder
Buffers and Inverters	1X inverter
	2X inverter
	3X inverter
	4X inverter
Multifunction	2-1 AND-OR invert
	2-2-2 AND-OR invert
	3-2 AND-OR invert
	2-1 OR-AND invert
Multiplexer	2 to 1 multiplexer
Schmitt Trigger	Schmitt Trigger
Transmission Gate	Buffered transmission gate
	Unbuffered transmission gate
Tristate Control	Tristate control

IGC10000 Sequential Macros		Set	Reset	Jam Load
D Flip-Flops	D flip-flop with reset	—	Yes	—
	D flip-flop with set	Yes	—	—
	D flip-flop with set and reset	Yes	Yes	—
	Divide by 2 flip-flop w/jam load and reset	—	Yes	Yes
	Divide by 2 flip-flop w/reset	—	Yes	—
	D flip-flop w/jam load and reset	—	Yes	Yes
	D flip-flop shift register with reset	—	Yes	—
JK Flip-Flops	JK flip-flop with reset	—	Yes	—
	JK flip-flop with set	Yes	—	—
T Flip-Flops	T flip-flop with reset	—	Yes	—
Latches	D latch	—	—	—
	D latch w/single input control	—	—	—
	D latch with reset	—	Yes	—
	D latch w/reset and single input control	—	Yes	—
	D latch w/transmission gate on output	—	—	—
Counters	Down counter with reset	—	Yes	—
	Down counter w/jam load and reset	—	Yes	Yes
	Up counter with reset	—	Yes	—
	Up counter w/jam load and reset	—	Yes	Yes
	Up/down counter with reset	—	Yes	—
	Up/down counter w/jam load and reset	—	Yes	Yes

Table 2. IGC10000 MACRO Library (continued)

IGC10000 Digital I/O Cell Macros	
Type	**Description**
Bidirectional	Tristate output/unbuffered input Tristate output/inverting TTL input buffer
Feedthrough	Input feedthrough
Internal Buffer	Inverting internal buffer Internal tristate buffer
Input Buffer	Non-inverting TTL input buffer Non-inverting CMOS input buffer with pull-up options
Output Buffer	Open drain output buffer Non-inverting TTL output buffer Inverting TTL output buffer Tristate output buffer Symmetrical drive output buffer

IGC10000 Analog I/O Cell Macros

The list below represents a sample of custom macros developed for specific analog applications. Consult your Intersil Representative for suitability to your design.

- Analog Transmission Gate
- Auto Null Comparator
- Comparator
- Compensated Op Amp
- Crystal Oscillator
- Current Multiplier
- Current Reference
- Op Amp
- Power-on Reset
- RC Oscillator
- Schmitt Trigger

COMPUTER AIDED DESIGN SOFTWARE TOOLS

The IGC10000 family is supported by a proprietary computer aided design (CAD) system developed at the General Electric Microelectronics Center. The system provides CAD tools for logic simulation, accurate prediction of circuit speed performance, automated design of interconnect circuitry, electrical and design rule checking, post-layout simulation using RC delays extracted from the layout, and automatic conversion of simulation test pattern files into tester format.

The CAD tools are integrated under a supervisory program called the CADEXEC (for CAD Executive) that runs on a Digital Equipment Corporation VAX computer. Once the user has entered the circuit's interconnect information into the computer, this information is converted into a common database accessed by all other parts of the software through the CADEXEC.

Logic Simulation: Users have access to the TEGAS logic simulator. For pre-layout logic (functional) verification, customers may perform TEGAS simulation using our Unit Delay Macro Library database; for design verification (pre-layout timing analysis), calculated delays based on fanout are used in conjunction with Best, Typical, and Worst Case libraries, whose parameters are described in Table 3.

Table 3. Best, Typical, and Worst Case Parameters

Parameter	Best	Typical	Worst
Voltage (V)	5.5	5.0	4.5
Temperature (°C)	0	27	70
Process	Best	Typical	Worst

Routing: The SILICA layout system uses a proprietary automatic router developed at the General Electric Microelectronics Center. The SILICA router has consistently performed with higher completion rate and lower CPU time than other commercially available routers; in addition, the router improves the overall performance of the circuit by selecting paths that produce the smallest delay. Like many routers, the SILICA router has a Critical Net feature that minimizes polysilicon and total net length by routing the critical net first. Unique to the SILICA router is the Super Critical Net feature, which prohibits the use of polysilicon gates in a specified net.

Electrical and Design Rule Checking: SILICA DRC (Design Rule Checker) performs electrical and design rule checking in minutes instead of hours and extracts geometric data from the layout for input into the RC delay extraction software.

Manual editing: In rare instances manual layout editing may be done on one of our CALMA workstations. CALMA output is fed into SILICA DRC for convenient verification of electrical integrity.

Post-layout simulation: A specialized circuit simulator has been developed at the General Electric Microelectronics Center to compute the delays of the RC-interconnect nets from the topology of the network after performing layout. The RC Delay extraction software uses a full transient analysis for each net; delays are based on resistance as well as capacitance of the interconnection nets. The software calculates delays as a function both of load switching voltage and driver output impedance and handles loops, bidirectional drivers, and multiple drivers on the net.

After the RC delay information is extracted, the CADEXEC system inserts the delays into the network database for post-layout TEGAS simulation and critical path analysis, thus providing an additional opportunity for refining the layout prior to PG tape generation.

Tester Tape Generation: Test program conversion software automatically translates the customer's final TEGAS simulation output file into a test vector pattern file to be used in testing the finished device.

PACKAGING

Five types of packages are available for the IGC10000 gate arrays. Dual inline packages are available in plastic (Plastic DIP), ceramic (CerDIP) and multilayer ceramic (Side Brazed DIP); leadless chip carriers and pin grid arrays are provided in multilayer ceramic. Table 4 presents recommended package types for each pin count and array size.

Table 4. Recommended Package Types

Number of Pins	Plastic DIP	CerDIP	Side Brazed DIP	Leadless Chip Carrier	Pin Grid Array
8	408		408		
14	408	408	408		
16	408	408	408		
18	408	408	408		
20		408	408		
24	408	408	408		
	756	756	756		
	1500	1500	1500		
28	408	408	408		
	756	756	756		
	1500	1500	1500		
40	408	408	408		
	756	756	756		
	1500	1500	1500		
44				756	
				1500	
48			756		
			1500		
52				1500	
68				1500	1500

DEVELOPMENT

An overview of the gate array development process is shown in the flow chart of Figure 6. During Phase 1 (Design Translation), most of the responsibility lies with the customer; during Phase 3 (Fabrication), with Intersil. In Phase 2 (Design Implementation), most of the activities are performed by Intersil, but require customer interaction and approval. Figure 6 delineates the responsibilities of the customer and of Intersil. For more information, contact either your local Intersil representative, or Semicustom Marketing at the General Electric Microelectronics Center, Research Triangle Park, NC, telephone 919-549-3607.

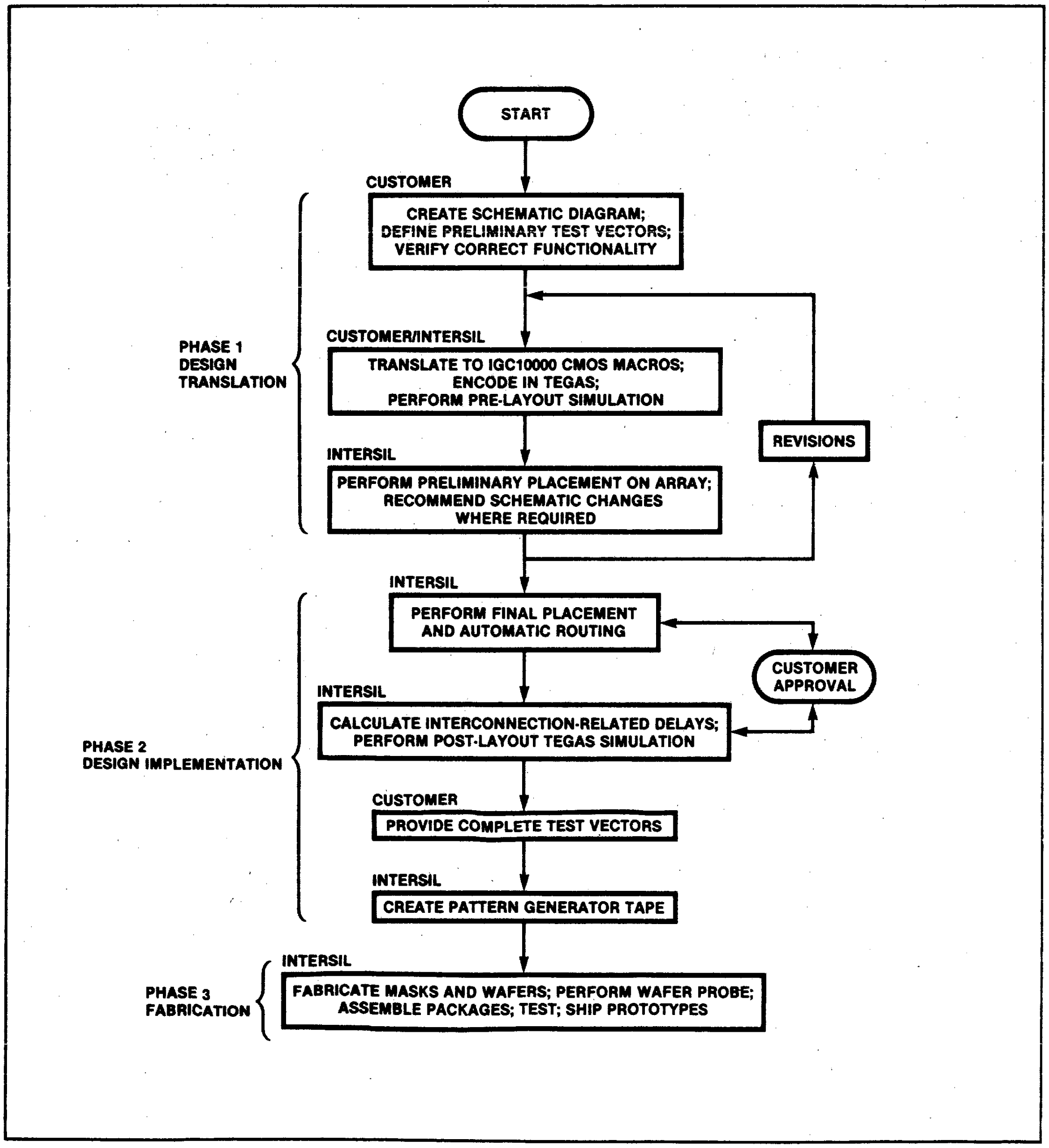

Figure 6. Simplified Flowchart for Gate Array Development

OPERATING CHARACTERISTICS[1]

Absolute Maximum Ratings[2] (Referenced to V_{SS})

Parameter	Symbol	Limits	Units
DC Supply Voltage	V_{DD}	−0.5 to +10.0	V
Input Voltage	V_I	−0.5 to V_{DD} + 0.5	V
DC Input Current	I_I	±10	mA
Operating Ambient Temperature Range	T_A	−55 to +125	°C
Storage Temperature Range (Ceramic)	T_{STG}	−65 to +150	°C
Storage Temperature Range (Plastic)	T_{STG}	−40 to +125	°C

NOTE 1: Stress ratings only. Functional operation of the device at these or any conditions beyond those indicated as Recommended Operating Conditions is not implied.
NOTE 2: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Limits	Units
DC Supply Voltage	V_{DD}	3.3±0.3V to 9.0±0.9V	V
Typical Operating Frequency	f_{CK}	8.0	MHz
Operating Ambient Temperature Range[1]	T_A	−55 to +125	°C

NOTE 1: IGC10000 gate array macros are currently characterized between 0 and 70°C.

AC CHARACTERISTICS

Specified for nominal processing = 5V, 27°C.
Calculated for a fanout of 1.

	Parameter	Typical Delay (ns)
Array Cell Macros		
2-input NAND	D to Output	6
2-input NOR	D to Output	6
4-input NAND	D to Output	8
4-input NOR	D to Output	18
1X inverter	D to Output	5
4X inverter	D to Output	4
2-1 AND-OR invert	D to Output	9
D flip-flop with reset	CK to Output	9
Schmitt trigger	Input to Output	18
Up counter with reset	CK to Output	11
I/O Cell Macros		
Input feedthrough	Pad to Output	1
Non-inverting Input Buffer	Pad to Output	9
Non-inverting Output Buffer	D to Pad	10 (15 pF) 19 (50 pF)

DC CHARACTERISTICS

V_{DD} = 5V ± 10%

Symbol	Parameter	Condition	Limits[1] 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	70°C Min.	70°C Max.	Units
I_{DD}[2]	Quiescent Device Current	$V_I = V_{DD}$ or V_{SS}				0.3			100	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| \leq 1\mu A$		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| \leq 1\mu A$	V_{DD} − 0.05		V_{DD} − 0.05			V_{DD} − 0.05		V
V_{IL}	Low Level Input Voltage	CMOS I/O Macro		1.5			1.5		1.5	V
V_{IH}	High Level Input Voltage	CMOS I/O Macro	3.5		3.5			3.5		V
V_{IL}	Low Level Input Voltage	TTL I/O Macro		0.8			0.8		0.8	V
V_{IH}	High Level Input Voltage	TTL I/O Macro	2.0		2.0			2.0		V
I_{OL}[3]	Output Low[4] (Sink Current)	$V_O = 0.4V$	1.8		1.8	3.6		1.6		mA
		$V_O = 2.5V$	3.8		3.8	7.6		3.4		mA
I_{OH}[3]	Output High (Source Current)	$V_O = 4.6V$	0.3		0.3	0.6		0.25		mA
		$V_O = 2.5V$	1.8		1.8	3.6		1.6		mA
I_{IN}	Input Leakage Current	V_{IN} = 0 or V_{DD}		± 0.1		± .001	± 0.1		± 1.0	μA
I_{OZ}	Tristate Output Leakage Current	V_O = 0 or V_{DD}		± 1.0		± .001	± 1.0		± 10	μA
C_{IN}	Input Capacitance	Any Input				5.0				pF

NOTES:

1. IGC10000 gate arrays are designed to perform under conditions up to 125°C. Limits reflect temperature range at which the macro library is characterized.
2. Any internal oscillators disabled.
3. Results depend on specific output macro used.
4. There may be limitations on maximum current when many outputs are simultaneously low.

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CUSTOM/SEMICUSTOM

ABBREVIATIONS OF COMPANY NAMES

Action Ins	Action Instruments
AD	Analog Devices
ADT	Advanced Digital Technology
Advent	Advent Products, Inc.
Alphatron	Alphatron
AMA	American Automation
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
Amperex	Amperex Electronic Corp.
Analogic	Analogic
Analog Sys	Analog Systems
APC	Applied Micro Circuits
Apex	Apex Microtechnology
APM	Applied Microsystems Corp.
Appl Sys	Applied Systems Corp.
APT	Applied Microtechnology
Aptek	Aptek Microsystems
Array Tech	Array Technology
AWI	AWI Electronics
Barvon	Barvon Research
Bedford	Bedford Computer Systems Inc.
Burr-Brown	Burr-Brown
CAE	Computer Aided Engineering
Cal Devices	California Devices
Cermetek	Cermetek
CGRS	CGRS Microtech Inc.
Cherry	Cherry Semiconductor
CIC	Custom Integrated Circuits
CirTech	Circuit Technology
Citel	Citel
Comlinear	Comlinear Corporation
CMA	Custom MOS Arrays
Comark	Comark Corp.
Comdial	Comdial Semiconductor
Comp Auto	Computer Automation
Compas	Compas Microsystems
Cont Logic	Control Logic Inc.
Control Sys	Control Systems Microsystems Div.
CreMicro	Creative Micro Systems
Cromemco	Cromemco, Inc.
Cubit	Cubit Inc.
Curtis	Curtis Electro Devices, Inc.
Cybernetic	Cybernetic Micro Systems
Cybersys	Cybersystems
Cybertek	Cybertek Inc.
Data General	Data General
Data I/O	Data I/O
Data Trans	Data Translation
Datel	Datel
Datricon	Datricon Corporation
DDC	Data Devices Corporation
DEC	Digital Equipment Corporation
Die-Tech	Die-Tech
Digelec	Digelec Corp.
Digitek	Digitek, Inc.
Dionics	Dionics Inc.
Dist Comp	Distributed Computer Systems
Divers Tech	Diversified Technology
E-HI	E-H International, Inc.
EDI	Electronic Designs Inc.
Elind	Elind Elettronica Industriale
EMM-SESCO	EEM-SESCO
Emulogic	Emulogic Inc.
ETI Micro	ETI Micro
Exar	Exar Integrated Systems
Exel	Exel Microelectronics
Fairchild	Fairchild
Ferranti	Ferranti Electric
Force	Force Computers
Fujitsu A	Fujitsu America
Fujitsu	Fujitsu Microelectronics, Inc.

GI	General Instrument
GTE Micro	GTE Microcircuits
Harris	Harris Semiconductor
Heurikon	Heurikon Corp.
Hilevel	Hilevel Technology, Inc.
Hitachi	Hitachi America, Ltd.
Holt	Holt Inc.
HP	Hewlett-Packard
Hughes	Hughes Aircraft, Solid State Products
Hybrid Sys	Hybrid Systems
HyComp	HyComp
ICC	International Cybernetics
IDT	Integrated Device Technology
IMI	International Microcircuits, Inc.
IMP	International Microelectronic Products
IMS	Industrial MicroSystems Inc.
Infosphere	Infosphere
Inmos	Inmos
IntCirEng	Integrated Circuit Engineering
IntCirSys	Integrated Circuit Systems
IntCompSys	Integrated Computer Systems
Int Tech	Integrated Technology Corp.
Intech	Intech Microcircuits Div.
Intel	Intel
Interdesign	Interdesign
Intersil	Intersil
Intronics	Intronics
ITT	ITT Semiconductors
Kinetic Sys	Kinetic Systems
Kontron	Kontron Electronics
Lambda	Lambda Semiconductor
Linear Tech	Linear Technology
LSI Comp	LSI Computer Systems
LSI Logic	LSI Logic Corporation
Master Logic	Master Logic Corporation
Matrix	Matrix Corp.
Matrox	Matrox Electronic Systems
Maxim	Maxim Integrated Products
MCC	Micro-Computer Control
MCE	MCE Electronics
Micrel	Micrel
Micro Innov	Micro Innovators
Micropac	Micropac Industries
Micro Net	Micro Networks
Micro Pwr	Micro Power Systems
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Mitel	Mitel Semiconductor
Mitsubishi	Mitsubishi Electronics
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Mostek	Monolithic Systems Corp.
Motorola	Mostek
MRC	Motorola Semiconductor
Murray	MRC Systems
Monosil	Murray Consulting
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NCM	NCM Corp.
NCR	NCR Corp., Microelectronics Division
NEC	NEC Electronics
Nitron	Nitron

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OEI	Optical Electronics Inc.
Ohio Sci	Ohio Scientic
OKI	OKI Semiconductor
Omnibyte	Omnibyte Corp.
Onset	Onset Computer Corp.
Panasonic	Panasonic
Pico Design	Pico Design
Polycore	Polycore Electronics
Plessey	Plessey Semiconductors
PMI	Precision Monilithics, Inc.
PragDes	Pragmatic Design Inc.
Pro-Log	Pro-Log Corp.
Quay	Quay Corp.
Raytheon	Raytheon Semiconductor
RCA	RCA Solid State Division
RCI Data	RCI Data
RELMS	Relational Memory Systems
Reticon	Reticon
RIFA	RIFA
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SBE	SBE, Inc.
SEEQ	SEEQ Technology, Inc.
SPI	Semi Processes Inc.
Siemens	Siemens
Si-Fab	Si-Fab
Signetics	Signetics
SGS	SGS Semiconductor
Sharp	Sharp
Silicon G	Silicon General
Siliconix	Siliconix
Silicon Sys	Silicon Systems Inc.
Siltronics	Siltronics
SMC	Standard Microsystems Corp.
S MOS	S MOS Systems
Solarise	Solarise Enterprises
Solitron	Solitron Devices
Sprague	Sprague Electric Company
SSM	Solid State Micro Technology for Music
SSS	Solid State Scientific
Stag	Stag Microsystems
STC	Storage Technology Corp.
STD	STD Microsystems
Struc Des	Structured Design Inc.
Stynetic	Stynetic Systems
Sunrise	Sunrise Electronics
Sunshine	Sunshine Semiconductor
Supertex	Supertex Inc.
Symtek	Symtek Corp.
Synertek	Synertek
Sys Innov	Systems Innovations
Tau Zero	Tau Zero Inc.
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WHEN PICKING A CUSTOM LSI MANUFACTURER, THE FIRST THING TO LOOK AT IS HOW GOOD THEY ARE. THE SECOND IS WHERE THEY'RE LOCATED.

If you're even thinking about a custom circuit, you're aware of the benefits it will give you: it will, over the long run, cost less to produce than any form of semi-custom; by incorporating the maximum number of functions, it will give you the most savings in board space, shipping, inventory control, inspection, manufacturing operations, and reliability. A properly designed custom chip will greatly increase your product's versatility, and give you an enormous marketing advantage.

But how can you be sure you'll actually get all these benefits?

1 ARE THEY CUSTOM SPECIALISTS?

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2 ARE THEY EASY TO WORK WITH?

The second way to make sure you get the most out of your custom chip is to work very closely with the manufacturer's engineers. The more active the interplay between you (or your engineers) and the manufacturer's designers, the more your chip will do for you (and, we might add, the faster the design will be completed).

And it's a lot easier to work closely with somebody when you can step in your car and be at his place in an hour or so. Or vice versa.

Well, if you're anywhere within 50 miles of New York, we — LSI Computer Systems, Inc. — are just such an easy drive away. We're right smack in the middle of Long Island.

Of course, being "easy to work with" is not solely a function of geographical location. It's also a function of accessibility, and *that's* largely a function of size. Many of our customers who have also worked with big LSI manufacturers tell us that our engineers are far more accessible than the big outfits' engineers are. We'd like to be big someday, too, but accessible is one thing we'll always be. It's one of the things that made us as big as we are.

Call Ron Colino. He's our VP/Marketing, and he can tell you a lot more reasons why you should come with us if you're thinking of custom. He can also tell you a lot of reasons why you *should* be thinking of custom if you're not.

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Please see IC Master, DIGITAL SECTION, page 803 for our line of Standard micro-circuits.

LSI LOGIC CORPORATION

LL3000 Series
Silicon-Gate HCMOS Logic Arrays

Preliminary

Features

- Silicon-gate 3.5-micron (drawn) HCMOS technology
- Single-layer metal interconnection
- HTTL and LSTTL speeds—5 ns through a 2-input NAND gate and interconnection, T_A = 25 degrees C, fanout = 2, V_{DD} = 5V
- Optimal block structure of 2N and 2P transistors
- Complexities ranging from 272 to 2550 blocks
- Pin counts ranging up to 104
- Fully supported by LDS™ (LSI Design System)
- Extensive macrocell and macrofunction libraries
- All non-power pads configurable as inputs, outputs or bidirectional
- TTL/CMOS I/O compatibility
- Configurable output drive up to 4.8mA
- All inputs and outputs protected from over-voltage and latch-up
- Full Military capability
- Ceramic and plastic packages
- LL3110Q evaluation device available

LSI Logic

CUSTOM/SEMICUSTOM

LSI LOGIC CORPORATION

LL5000 Series
Silicon-Gate HCMOS Logic Arrays

Features

- Silicon-gate 3-micron (drawn) HCMOS technology
- Schottky TTL speeds - 2.5ns through 2-input NAND gate and interconnection, T_A = 25°C, fanout = 2, V_{DD} = 5V
- Optimal block structure of 2N and 2P transistors
- Complexities ranging from 880 to 6000 blocks
- Pin counts ranging up to 180
- Fully supported by LDS™ (LSI Design System)
- Extensive macrocell and macrofunction libraries
- All non-power pads configurable as inputs, outputs or bidirectional
- TTL/CMOS I/O compatibility
- Configurable output drive up to 6.0mA
- All inputs and outputs protected from over-voltage and latch-up
- Full military capability
- Ceramic and plastic packages
- Alternately-sourced
- LL5220Q evaluation device available

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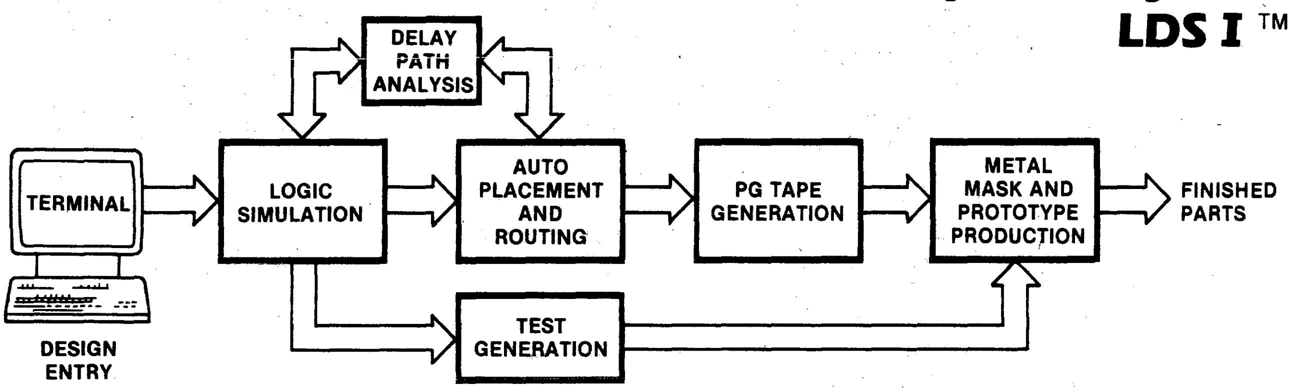
LL7000 Series Silicon-Gate HCMOS Logic Arrays

Advance Information

Features

- Silicon-gate 2.0-micron (drawn) HCMOS technology
- Faster than Schottky TTL speeds - 1.4ns through 2-input NAND gate and interconnection, $T_A = 25°C$, fanout = 2, $V_{DD} = 5V$
- Optimal block structure of 2N and 2P transistors
- Complexities ranging from 968 to 10,013 blocks
- Pin counts ranging up to 180
- Fully supported by LDS™ (LSI Design System)
- Extensive macrocell and macrofunction libraries
- All non-power pads configurable as inputs, outputs or bidirectional
- TTL/CMOS I/O compatibility
- Configurable output drive up to 6.0mA
- All inputs and outputs protected from over-voltage and latch-up
- Full military capability
- Ceramic and plastic packages
- Alternately-sourced
- LL7220Q evaluation device available

LSI Development System LDS I ™



Development Support and Interface

The LDS I™ (LSI Development System I) is used for logic simulation, design verification, test pattern generation, layout and mask design. The system may be accessed using a variety of remote terminals, including the Tektronix 4014 and 4112 vector-display terminals. The desired logic function may be entered alpha numerically or schematically into the system and the design electronically breadboarded using the LDS I™ logic simulator. The simulated input patterns may be checked for completeness, and other tests added (automatically if desired) until the final test pattern is completed. The personality masks may then be designed remotely by the customer using the LDS I™ interactive/automatic placement and routing program. Alternately, LSI LOGIC CORPORATION will complete the metal mask design. For more details see the LDS I™ Product Description available from LSI LOGIC CORPORATION.

For new designs, the LDS I™ Development System may be used to verify the design, generate test patterns and (optionally) design the metal masks. Four possible interfaces to LDS I™ are offered.

1. Use the complete LSI LOGIC CORPORATION system in Milpitas, California.
2. Install a remote terminal in your facility connected to LSI LOGIC CORPORATION mainframe. The Tektronix 4014 and 4112 are both supported, with the 4112 providing significantly higher performance. In either case a Tektronix 4662 11-inch×17-inch plotter may be used for graphics hard copy.
3. Install a turnkey LDS I™ system in your facility.
4. LSI Logic can specify design rules and provide macro layouts so that a customer's own CAD system may be used.

The following material is required by LSI LOGIC CORPORATION to alternate source an existing CDI-HC or AMI-UA array part.

- Calma data base or PG tape of the metal mask
- Sentry test tape
- AC test specifications
- Package and marking specifications
- Bonding diagram
- Four devices meeting all required specifications

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SY2827	MIC2827	2048 Dynamic Shift Register
SY2825	MIC2825	Dual 1024 Bit Dynamic Shift Register
SY1404	MIC1404	1024 Bit Dynamic Shift Register

* Call Micrel if you need help in Device Sourcing.

WAFER PROCESSING

Technology: PMOS, CMOS, NMOS Silicon or Metal Gate, Bipolar Linear. Minimum feature size is 4 micron and Isoplaner type processing is available for Silicon Gate MOS. Epi thickness 6-12 micron with Arsenic/antimony buried layer. 3 or 4 inch wafers.

Clean Room: 5000 ft^2 of class 100 clean room.

Engineering Run: 25 wafer starts with 10 guaranteed to meet your Process parameters. Delivery is 5 weeks with plates.

Production Run: 25 wafer minimum with no minimum annual volume. 10,000 wafer starts per month capacity. Delivery is 4 weeks, expedited to 10 days.

Customer Supplies: Tooling, design criteria and test software. We'll honor non-disclosure agreements.

Ion Implant: Varian DF4U/Veeco 2100

WAFER/PACKAGED IC TESTING:

Wafer Test: Map and test to process parameters.

Packaged IC Test: Mil STD 883 B Group A, using high/low temperature handlers.

Wafer Probing/Packaged IC: 3 Sentry VIIs or Series 20 VLSI Testers with handlers.

SEM Analysis: Mil STD 883B using ISI 5 x 30, 5-30KEV.

Screening: Mil STD 883B class B or customer requirement.

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GATE ARRAY MYTHS vs.

MYTHS .... VS............ REAL CUSTOM

MYTH 1 — User Friendly
"My logic diagram will always work when put in a gate array. A myth!"

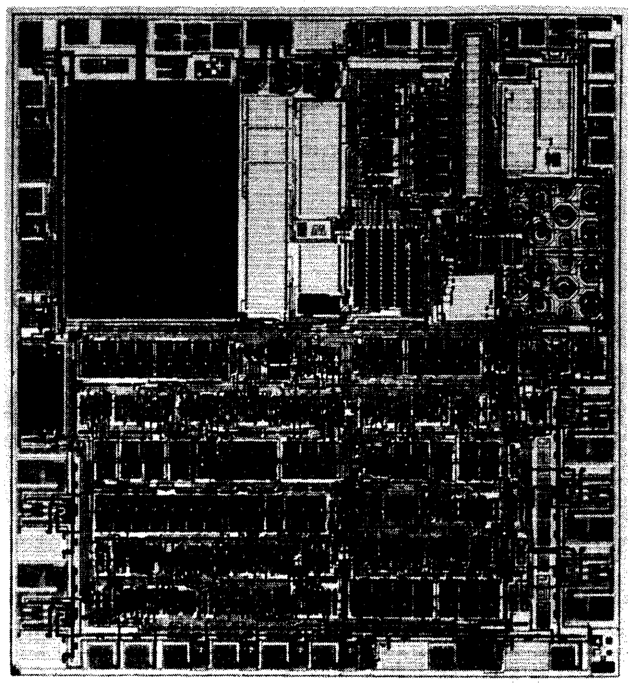
MYTH 2 — No System Timing Problems
"Circuit will never have any race conditions. A myth!"

MYTH 3 — Development Times Are Never Extended
"Chip will always work the first time, and never use more than one mask. A myth!"

MYTH 4 — No Customer Risk
"Development cost is low. A myth!" (Actually you pay double if chip doesn't work the first time.)

MYTH 5 — Testing Is Simple
"A myth!" (Actually testing is more difficult than the design.)

MYTH 6 — You're Never Switched from Gate Array to Full Custom
"The biggest myth of all."



*MPS Real Custom Chip (*HALLMOS circuit)*

Micro Power Systems

CUSTOM/SEMICUSTOM

MYTH ∞
"Quick. Take your logic diagram to any gate array company and in a few days/weeks — and almost like magic — tested production parts will appear, at a very low price. Now you can beat out your competitors."

FACTS
At Micro Power Systems, prospects are taken through the *Gate Array vs. Real Custom* analysis. Facts not myths determine the next step: (1) MPS' Real Custom, (2) MPS' Full Custom, or (3) other's gate arrays.

REAL CUSTOM
When you work in the real world of today — you need MPS' Real Custom to achieve your design and marketing goals. Over 65% of Micro Power's prospects fall into the Real Custom category. Here MPS uses an advanced, low-cost standard cell approach (over 2000 cells) for 80% of the design and 20% new design to optimize the interconnects and provide system enhancements. Quick turn-around and lower production costs are achieved by a proprietary interconnect system that provides a fast layout technique and optimizes silicon utilization.

FULL CUSTOM
Another 10% of our prospects take advantage of MPS' full custom. This is a 9 to 12-month joint effort where advanced circuit design, system definitions, and custom processing provide a quantum jump over the competition.

* *HALLMOS is a major breakthrough technology that combines precision linear bipolar, high accuracy thin film resistors, and high density CMOS all on the same monolithic integrated circuit. This process has a big potential in systems that utilize both analog and digital functions.*

MICRO POWER SYSTEMS'

REAL CUSTOM

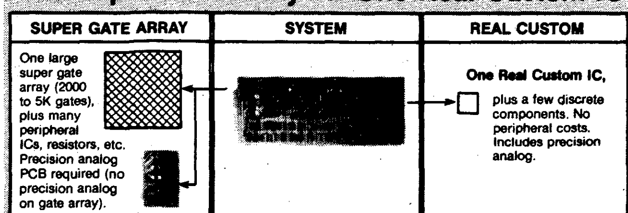
GATE ARRAYS

About 20 to 25% of our prospects require less than 500 parts per month. These prospects need a gate array company. We suggest they look for solid companies with their own foundries, testing, engineering support, and with realistic pricing and scheduling.

1 REAL CUSTOM vs. 1 GATE ARRAY

Compare MPS' Real Custom against one super gate array (see chart). Even comparing one super gate array shows major advantages for the Real Custom IC. Not only do you have significant parts and testing advantages — you can't use any precision analog in the super gate array. Is there a big difference between gate array and Real Custom delivery schedules? No! First, the gate array companies don't quote on a complete schedule. They use the time from when your circuit design is accepted (i.e., after you change your circuit to meet their technology limitations). Second, they quote to the most optimistic delivery date of the first prototype. You should prepare a realistic schedule with all the required events (yours and the vendors) from concept to delivery of production quantities. Then compare it to a Real Custom schedule and you'll find that they provide very little time savings, if any.

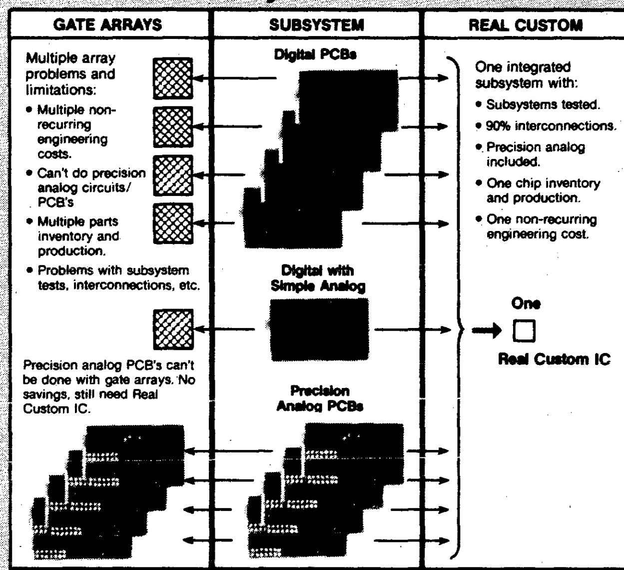
One Super Gate Array vs. One Real Custom IC



1 REAL CUSTOM vs. MULTIPLE ARRAYS

Look at the significant difference between using multiple gate arrays and one Real Custom IC in a digital/analog subsystem (see chart). Don't forget to add in your multiple gate array costs and costs for system definition, interconnection, and testing. With arrays, extensive interconnections remain at the system/board level and system testing becomes very difficult. Implementation of precision analog circuits are not even considered practical on arrays. Real Custom has inherently lower system development costs and lower production costs over solutions requiring multiple gate arrays.

Standard Gate Arrays vs. One Real Custom IC



CUSTOM CHIPS DELIVERED IN 1971

MPS has delivered full custom and Real Custom for over 13 years. We have advanced processes and design capabilities immediately available. For example, we routinely combine low noise bipolar transistors, CMOS logic, and thin film resistors on the same monolithic circuit. All these advanced technologies are currently in volume production.

RUN-AROUND

If you're in management and your personnel have been giving you the run-around about why your gate array project has gone through several redesigns and why the schedule has slipped — you'd better check out what the new projected production costs (piece price) are going to be. It may no longer fit into your marketing plan.

MYTH PERSISTS

We can't stop the gate array myth, but if you're serious about your company's future and being second best is not acceptable, then send for our *MPS Real Custom Plan*, or call Bob Sabo (ext. 210). A gate array shakeout is happening now. Do you want to deal in myths or facts?

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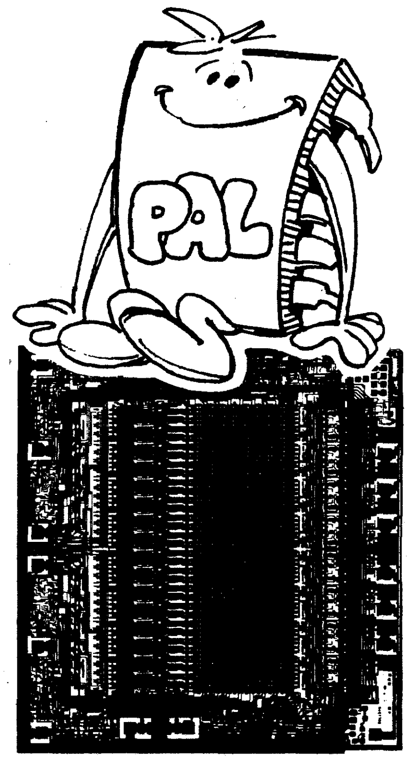
Micro Power Systems is the Leader in Refractory Gate MOS Technology



The PAL® Concept

Monolithic Memories' family of PAL devices gives designers a powerful tool with unique capabilities for use in new and existing logic designs. The PAL saves time and money by solving many of the system partitioning and interface problems brought about by increases in semiconductor device technology.

Rapid advances in large scale integration technology have led to larger and larger standard logic functions; single I.C.s now perform functions that formerly required complete circuit cards. While LSI offers many advantages, advances have been made at the expense of device flexibility. Most LSI devices still require large numbers of SSI/MSI devices for interfacing with user systems. Designers are still forced to turn to random logic for many applications.

The designer is confronted with another problem when a low to medium complexity product is designed. Often the function is well defined and could derive significant benefits from fabrication as an integrated circuit. However, the design cycle for a custom circuit is long and the costs can be very high. This makes the risk significant enough to deter most users. The technology to support maximum flexibility combined with fast turn around on custom logic has simply not been available. Monolithic Memories offers the programmable solution.

The PAL family offers a fresh approach to using fuse programmable logic. PAL circuits are a conceptually unified group of devices which combine programmable flexibility with high speed and an extensive selection of interface options. PAL devices can lower inventory, cut design cycles and provide high complexity with maximum flexibility. These features, combined with lower package count and high reliability, truly make the PAL a circuit designer's best friend.

PAL® is a registered trademark of Monolithic Memories.

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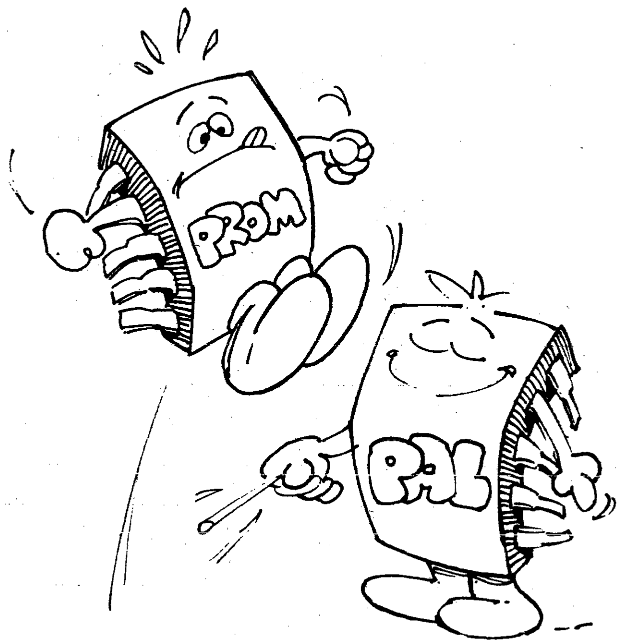
Monolithic Memories MMI

The PAL—Teaching Old PROMs New Tricks



MMI developed the modern PROM and introduced many of the architectures and techniques now regarded as industry standards. As the world's largest PROM manufacturer, MMI has the proven technology and high volume production capability required to manufacture and support the PAL.

The PAL is an extension of the fusible link technology pioneered by Monolithic Memories for use in bi-polar PROMs. The fusible link PROM first gave the digital systems designer the power to "write on silicon." In a few seconds he was able to transform a blank PROM from a general purpose device into one containing a custom algorithm, microprogram, or Boolean transfer function. This opened up new horizons for the use of PROMs in computer control stores, character generators, data storage tables and many other applications. The wide acceptance of this technology is clearly demonstrated by today's multi-million dollar PROM market.

The key to the PROM's success is that it allows the designer to quickly and easily customize the chip to fit his unique requirements. The PAL extends this programmable flexibility by utilizing proven fusible link technology to implement logic functions. Using PAL circuits the designer can quickly and effectively implement custom logic varying in complexity from random gates to complex arithmetic functions.

ANDs and ORs

The PAL implements the familiar sum of products logic by using a programmable AND array whose output terms feed a fixed OR array. Since the sum of products form can express any Boolean transfer function, the PAL circuit uses are only limited by the number of terms available in the AND - OR arrays. PAL devices come in different sizes to allow for effective logic optimization.

Figure 1 shows the basic PAL structure for a two input, one output logic segment. The general logic equation for this segment is

$$\text{Output} = (I_1+\bar{f}_1)(\bar{I}_1+\bar{f}_2)(I_2+\bar{f}_3)(\bar{I}_2+\bar{f}_4) + (I_1+\bar{f}_5)(\bar{I}_1+\bar{f}_6)(I_2+\bar{f}_7)\ (\bar{I}_2+\bar{f}_8)$$

where the "f" terms represent the state of the fusible links in the PAL AND array. An unblown link represents a logic 1. Thus,

fuse blown, f = 0

fuse intact, f = 1

An unprogrammed PAL has all fuses intact.

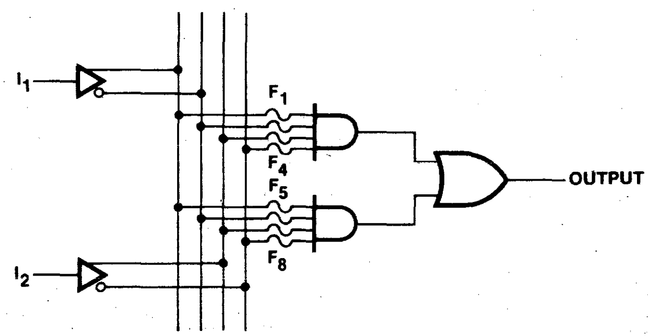


Figure 1

PAL Notation

Logic equations, while convenient for small functions, rapidly become cumbersome in large systems. To reduce possible confusion, complex logic networks are generally defined by logic diagrams and truth tables. Figure 2 shows the logic convention adopted to keep PAL logic easy to understand and use. In the figure, an "x" represents an intact fuse used to perform the logic AND function. (Note: the input terms on the common line with the x's are not connected together.) The logic symbology shown in Figure 2 has been informally adopted by integrated circuit manufacturers because it clearly establishes a one-to-one correspondence between the chip layout and the logic diagram. It also allows the logic diagram and truth table to be combined into a compact and easy to read form, thereby serving as a convenient shorthand for PAL circuits. The two input - one output example from Figure 1 redrawn using the new logic convention is shown in Figure 3.

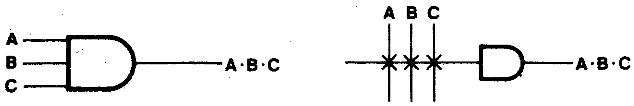


Figure 2

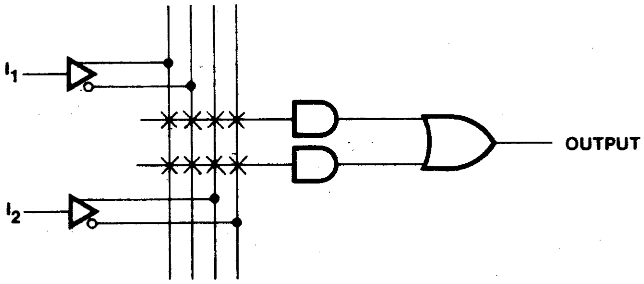


Figure 3

As a simple PAL example, consider the implementation of the transfer function:

Output = $I_1\bar{I}_2 + \bar{I}_1 I_2$

The normal combinatorial logic diagram for this function is shown in figure 4, with the PAL logic equivalent shown in figure 5.

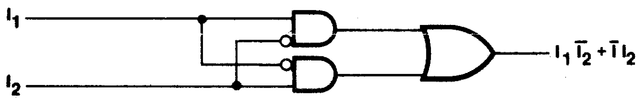


Figure 4

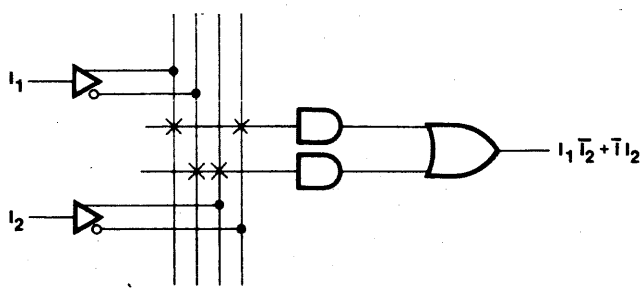


Figure 5

Using this logic convention it is now possible to compare the PAL structure to the structure of the more familiar PROM and PLA. The basic logic structure of a PROM consists of a fixed AND array whose outputs feed a programmable OR array (figure 6). PROMs are low-cost, easy to program, and available in a variety of sizes and organizations. They are most commonly used to store computer programs and data. In these applications the fixed input is a computer memory address; the output is the contents of that memory location.

PROM
16 Words X4 Bits

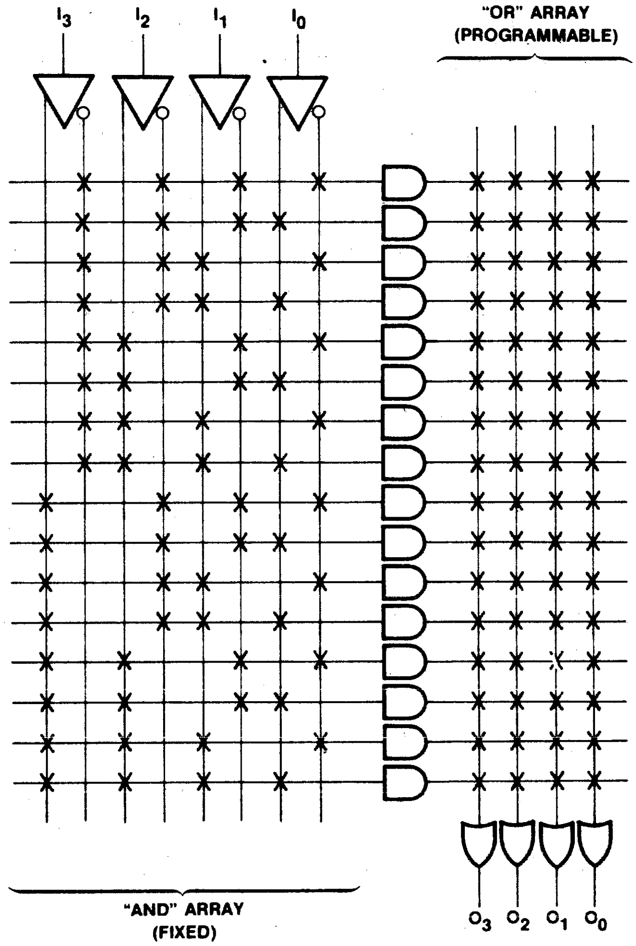


Figure 6

The basic logic structure of the PLA consists of a programmable AND array whose outputs feed a programmable OR array (Figure 7). Since the designer has complete control over all inputs and outputs, the PLA provides the ultimate flexibility for implementing logic functions. They are used in a wide variety of applications. However, this generality makes PLAs expensive, quite formidable to understand, and costly to program (they require special programmers).

The basic logic structure of the PAL, as mentioned earlier, consists of a programmable AND array whose outputs feed a fixed OR array (Figure 8). The PAL combines much of the flexibility of the PLA with the low cost and easy programmability of the PROM. Table 1 summarizes the characteristics of the PROM, PLA, and PAL logic families.

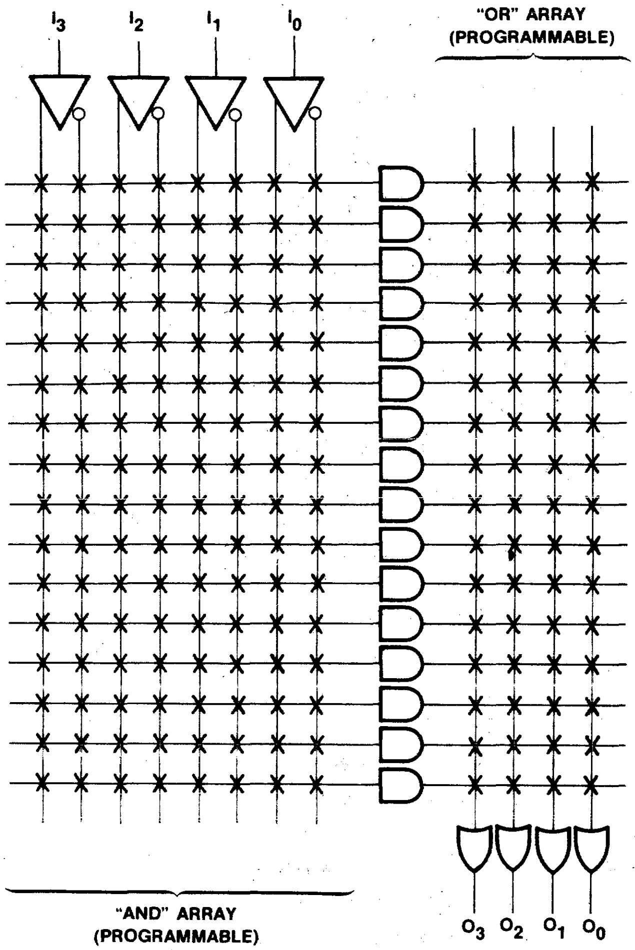


Figure 7

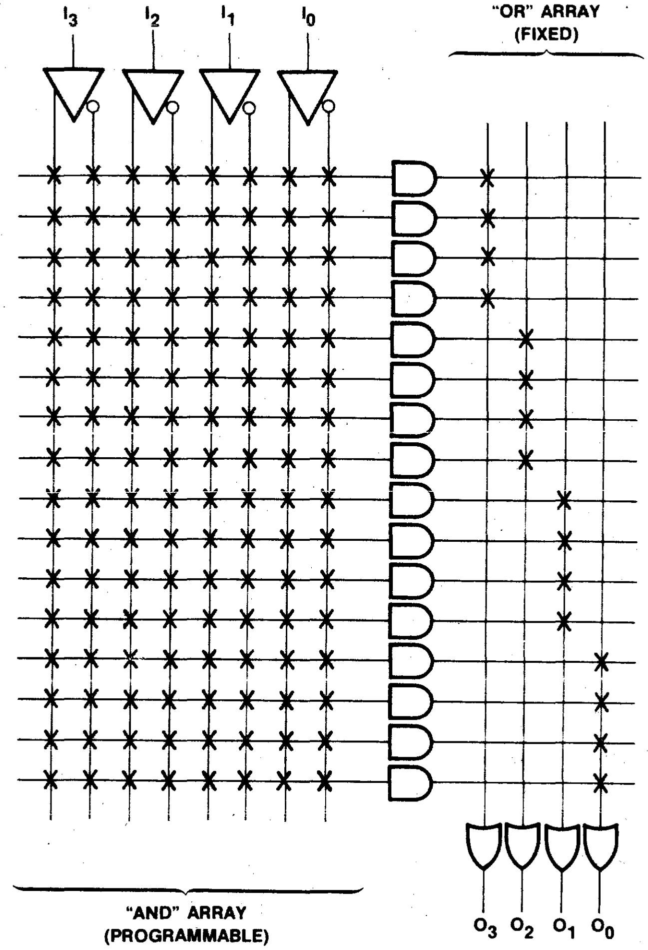


Figure 8

	AND	OR	OUTPUT OPTIONS
PROM	Fixed	Prog	TS, OC
FPLA	Prog	Prog	TS, OC, Fusible Polarity
FPGA	Prog	None	TS, OC, Fusible Polarity
FPLS	Prog	Prog	TS, Registered Feedback, I/O
PAL	Prog	Fixed	TS, Registered Feedback, I/O

Table 1

PAL Input/Output/Function/Performance Chart

PART NO.	INPUT	OUTPUT	PROGRAMMABLE I/O'S	FEEDBACK REGISTER	OUTPUT POLARITY	FUNCTIONS	PERFORMANCE STD	A	-2	-4
10H8	10	8			AND-OR	AND-OR Gate Array	X		X	
12H6	12	6			AND-OR	AND-OR Gate Array	X		X	
14H4	14	4			AND-OR	AND-OR Gate Array	X		X	
16H2	16	2			AND-OR	AND-OR Gate Array	X		X	
16C1	16	2			BOTH[1]	AND-OR Gate Array	X		X	
20C1	20	2			BOTH[1]	AND-OR Gate Array	X			
10L8	10	8			AND-NOR	AND-OR Invert Gate Array	X		X	
12L6	12	6			AND-NOR	AND-OR Invert Gate Array	X		X	
14L4	14	4			AND-NOR	AND-OR Invert Gate Array	X		X	
16L2	16	2			AND-NOR	AND-OR Invert Gate Array	X		X	
12L10	12	10			AND-NOR	AND-OR Invert Gate Array	X			
14L8	14	8			AND-NOR	AND-OR Invert Gate Array	X			
16L6	16	6			AND-NOR	AND-OR Invert Gate Array	X			
18L4	18	4			AND-NOR	AND-OR Invert Gate Array	X			
20L2	20	2			AND-NOR	AND-OR Invert Gate Array	X			
16L8	10	2	6		AND-NOR	AND-OR Invert Gate Array	X	X	X	X
20L8	14	2	6		AND-NOR	AND-OR Invert Gate Array		X		
20L10	12	2	8		AND-NOR	AND-OR Invert Gate Array	X			
16R8	8	8		8	AND-NOR	AND-OR Invert Gate Array w/Reg's	X	X	X	X
16R6	8	6	2	6	AND-NOR	AND-OR Invert Array w/Reg's	X	X	X	X
16R4	8	4	4	4	AND-NOR	AND-OR Invert Array w/Reg's	X	X	X	X
20R8	12	8		8	AND-NOR	AND-OR Invert w/Reg's		X		
20R6	12	6	2	6	AND-NOR	AND-OR Invert w/Reg's		X		
20R4	12	4	4	4	AND-NOR	AND-OR Invert w/Reg's		X		
20X10	10	10		10	AND-NOR	AND-OR-XOR Invert w/Reg's	X			
20X8	10	8	2	8	AND-NOR	AND-OR-XOR Invert w/Reg's	X			
20X4	10	4	6	4	AND-NOR	AND-OR-XOR Invert w/Reg's	X			
16X4	8	4	4	4	AND-NOR	AND-OR-XOR Invert w/Reg's	X			
16A4	8	4	4	4	AND-NOR	AND-CARRY-OR-XOR Invert w/Reg's	X			

Table 2

[1] Simultaneous AND-OR and AND-NOR outputs

PAL Circuits For Every Task

The members of the PAL family and their characteristics are summarized in Table 2. They are designed to cover the spectrum of logic functions at reduced cost and lower package count. This allows the designer to select the PAL that best fits his application. PAL units come in the following basic configurations:

Gate Arrays

PAL gate arrays are available in sizes from 12x10 (12 input terms, 10 output terms) to 20x2, with both active high and active low output configurations available (figure 9). This wide variety of input/output formats allows the PAL to replace many different sized blocks of combinatorial logic with single packages.

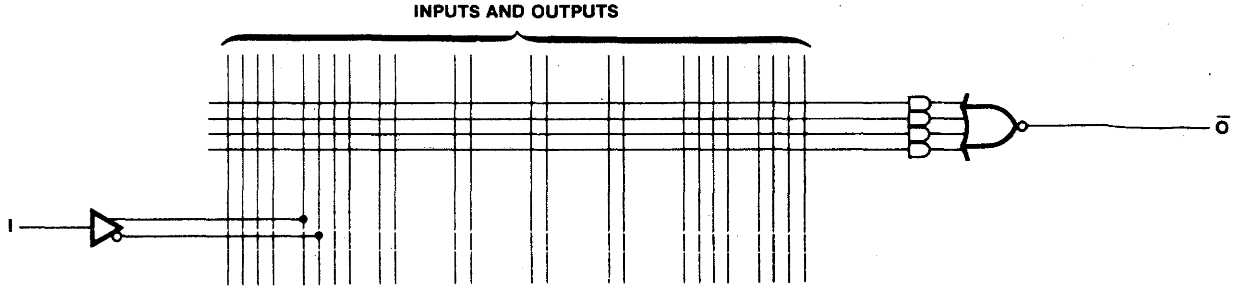


Figure 9

Programmable I/O

A feature of the high-end members of the PAL family is programmable input/output. This allows the product terms to directly control the outputs of the PAL (Figure 10). One product term is used to enable the three-state buffer, which in turn gates the summation term to the output pin. The output is also fed back into the PAL array as an input. Thus the PAL drives the I/O pin when the three-state gate is enabled; the I/O pin is an input to the PAL array when the three-state gate is disabled. This feature can be used to allocate available pins for I/O functions or to provide bi-directional output pins for operations such as shifting and rotating serial data.

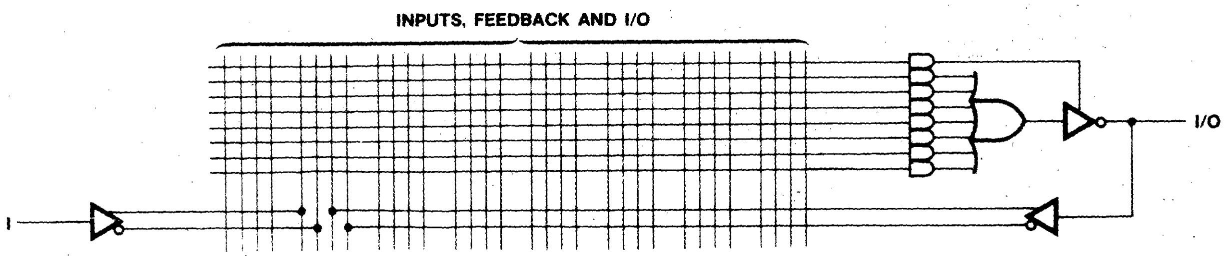


Figure 10

Registered Outputs with Feedback

Another feature of the high end members of the PAL family is registered data outputs with registered feedback. Each product term is stored into a D-type output flip-flop on the rising edge of the system clock (Figure 11). The Q output of the flip-flop can then be gated to the output pin by enabling the active low three-state buffer.

In addition to being available for transmission, the Q output is fed back into the PAL array as an input term. This feedback allows the PAL to "remember" the previous state, and it can alter its function based upon that state. This allows the designer to configure the PAL as a state sequencer which can be programmed to execute such elementary functions as count up, count down, skip, shift, and branch. These functions can be executed by the registered PAL at rates of up to 25 MHz.

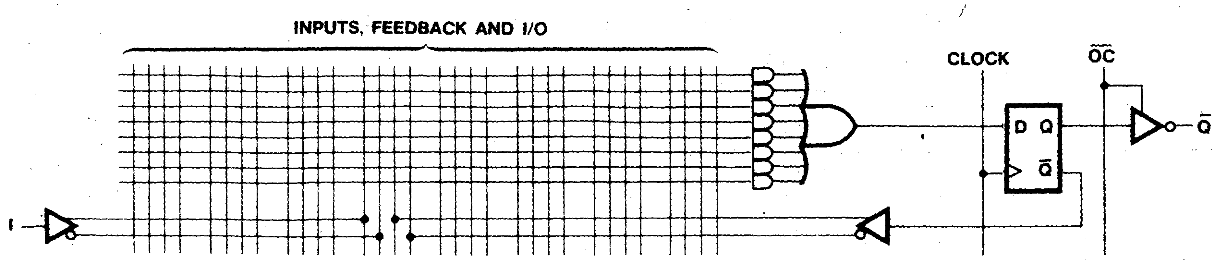


Figure 11

XOR PALs

These PAL devices feature an exclusive OR function. The sum of products is segmented into two sums which are then exclusive ORed (XOR) at the input of the D-type flip-flop (Figure 12). All of the features of the Registered PALs are included in the XOR PAL unit. The XOR function provides an easy implementation of the HOLD operation used in counters and other state sequencers.

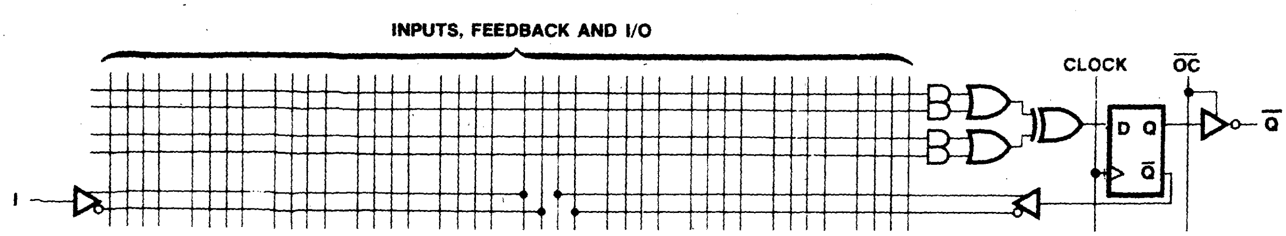


Figure 12

Arithmetic Gated Feedback

The arithmetic functions (add, subtract, greater than, and less than) are implemented by addition of gated feedback to the features of the XOR PAL device. The XOR at the input of the D-type flip-flop allows carrys from previous operations to be XORed with two variable sums generated by the PAL array. The flip-flop Q output is fed back to be gated with input terms A (Figure 13). This gated feedback provides any one of the possible Boolean combinations which are mapped in the Ka naugh map (Figure 15). Figure 14 shows how the PAL array ca be programmed to perform these 16 operations. These feature provide for versatile operations on two variables and facilitat the parallel generation of carrys necessary for fast arithmetic operations.

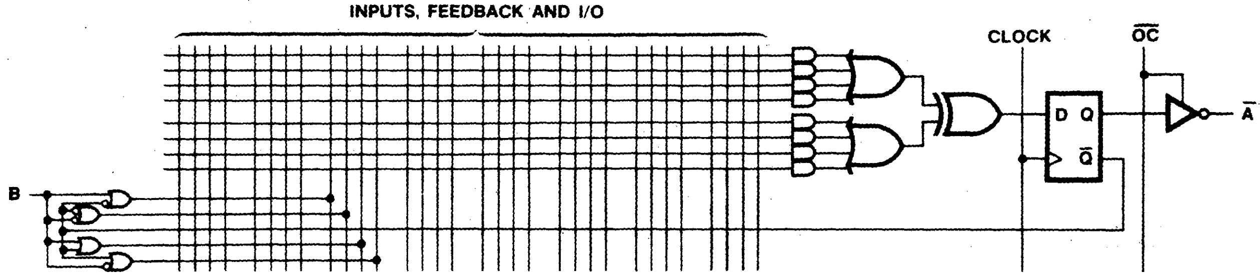


Figure 13

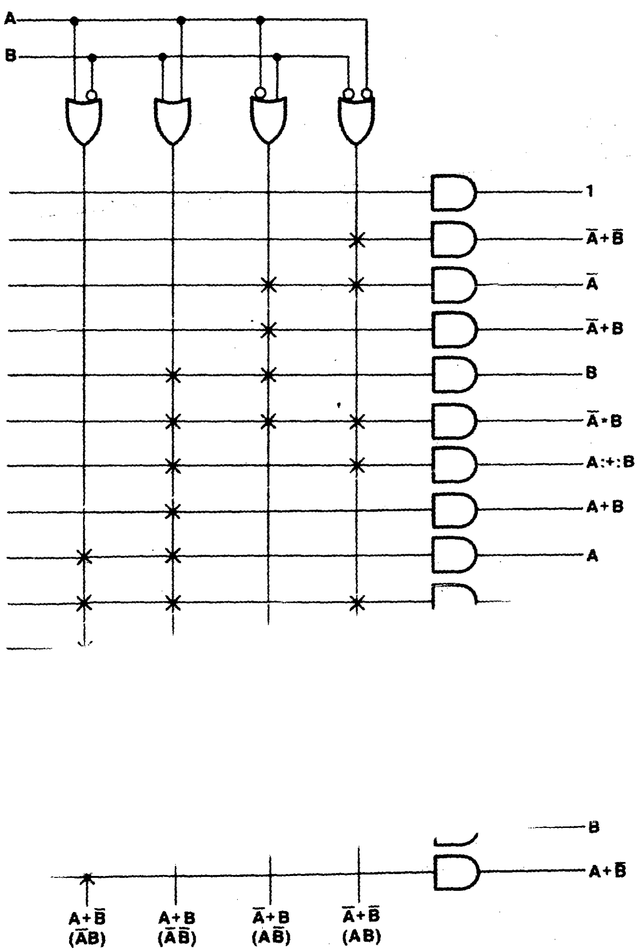


Figure 14

$(\overline{A}+B),(\overline{A}+\overline{B})$ / $(A+\overline{B}),(A+B)$

	--	-x	xx	x-
--	1	$\overline{A}+\overline{B}$	$\overline{A}$	$\overline{A}+B$
-x	A+B	A:+:B	$\overline{A}\cdot B$	B
xx	A	$A\cdot\overline{B}$	0	A · B

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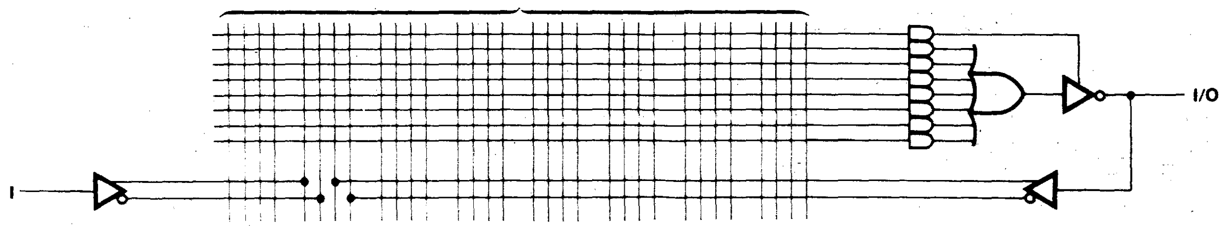

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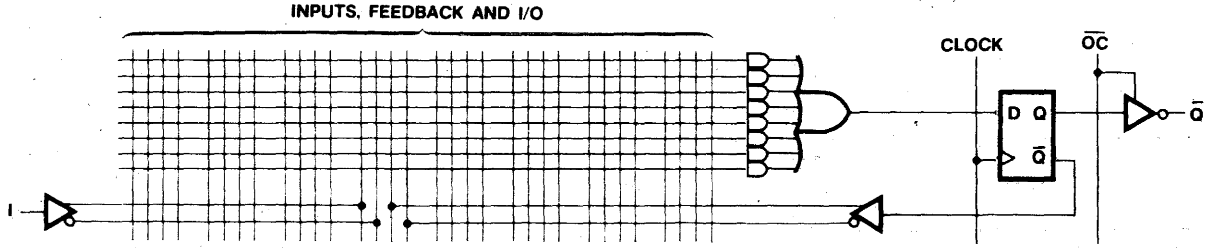

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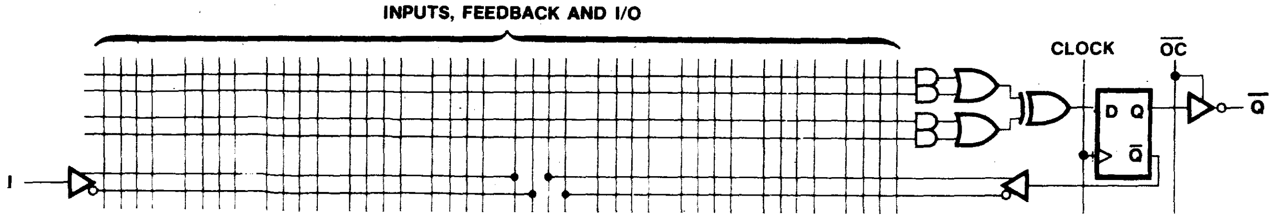

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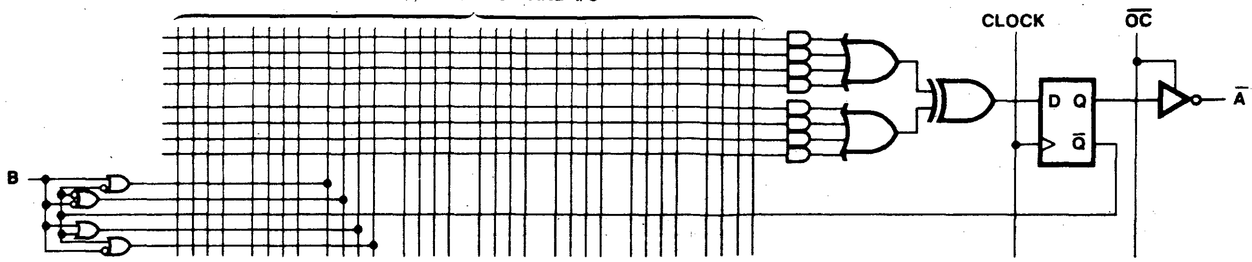

Figure 13

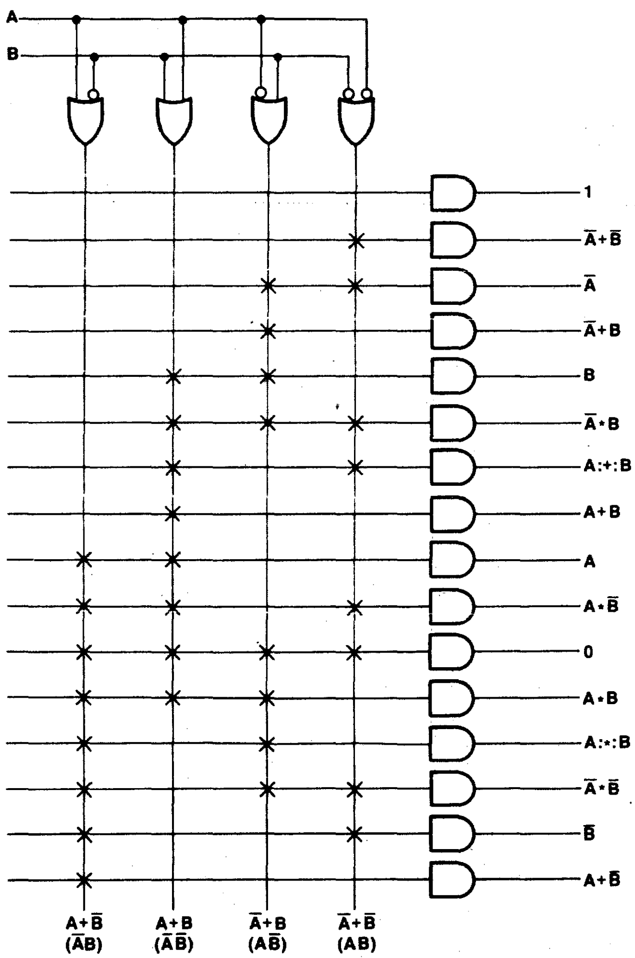

Figure 14

$(\bar{A}+B),(\bar{A}+\bar{B})$ / $(A+\bar{B}),(A+B)$	--	-x	xx	x-
--	1	$\bar{A}+\bar{B}$	$\bar{A}$	$\bar{A}+B$
-x	A+B	A:+:B	$\bar{A} \cdot B$	B
xx	A	$A \cdot \bar{B}$	0	$A \cdot B$
x-	$A+\bar{B}$	$\bar{B}$	$\bar{A} \cdot \bar{B}$	A:•:B

Figure 15

It should now be clear that the PAL family can replace most Small-Scale Integrated Logic (SSI) logic in use today, thereby lowering product cost and giving the designer even greater flexibility in implementing logic functions.

PAL Programming

PAL devices can be programmed in most standard PROM programmers with the addition of a PAL personality card. The PAL appears to the programmer as a PROM. During programming half of the PAL outputs are selected for programming while the other outputs and the inputs are used for addressing. The outputs are then switched to program the other locations. Verification uses the same procedure with the programming lines held in a low state.

PALASM (PAL Assembler)

PALASM is the software used to define, simulate, build, and test PAL units. PALASM accepts the PAL Design Specification as an input file. It verifies the design against an optional function table and generates the fuse plot which is used to program the PAL devices. PALASM is available upon request for many computers and is documented in the PAL Design Concepts section.

HAL (Hard Array Logic)

The HAL family is the mask programmed version of a PAL. The HAL is to a PAL just as a ROM is to a PROM. A standard wafer is fabricated to the 6th mask. Then a custom metal mask is used to fabricate Aluminum links for a HAL instead of the programmable Ti-W fuse array used in a PAL.

The HAL is a cost-effective solution for large quantities and is unique in that it is a gate array with a programmable prototype.

HMSI (HAL Medium Scale Integration)

The HMSI family is derived from the PAL using HAL technology. These devices perform predetermined functions which are not available in the existing TTL family. Because they are produced in volume, the user receives the benefit of volume pricing. HMSI PAL designs are given in the Applications section with their industry standard 74LS part number in line 2 of the PAL Design Specification.

PMSI (PAL Medium Scale Integration)

The PMSI family is derived in a similar fashion to HMSI except this product is produced entirely from a PAL circuit. A HAL circuit mask is not generated and an industry standard 74LS part number is not assigned unless sales warrant it.

PAL Technology

PAL circuits are manufactured using the proven TTL Schottky bipolar Ti-W fuse process to make fusible-link PROMs. An NPN emitter follower array forms the programmable AND array. PNP inputs provide high-impedance inputs (0.25 mA max) to the array. All outputs are standard TTL drivers with internal active pull-up transistors. Typical PAL propagation delay time is 25 ns, and all PALs are packaged in space saving 20-pin and 24-pin SKINNYDIP® packages.

PAL Data Security

The circuitry used for programming and logic verification can be used at any time to determine the logic pattern stored in the PAL array. For security, the PAL has a "last fuse" which can be blown to disable the verification logic. This provides a significant deterrent to potential copiers, and it can be used to effectively protect proprietary designs.

2175 Mission College Boulevard, Santa Clara, CA 95050 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374
Monolithic Memories

PAL®-Programmable Array Logic
HAL®-Hard Array Logic

Features/Benefits

- **Reduces SSI/MSI chip count greater than 5 to 1**
- **Saves space with SKINNYDIP® packages**
- **Reduces IC inventories substantially**
- **Expedites and simplifies prototyping and board layout**
- **PALASM™ silicon compiler provides auto routing and test vectors**
- **Security fuse reduces possibility of copying by competitors**

Description

The PAL family utilizes an advanced Schottky TTL process and the Bipolar PROM fusible link technology to provide user programmable logic for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.

The HAL family utilizes standard Low-Power Schottky TTL process and automated mask pattern generation directly from logic equations to provide a semi-custom gate array for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.

There are four different speed/power families offered. Choose from either the standard, high speed, half power, or quarter power family to maximize design performance.

The PAL/HAL lets the systems engineer "design his own chip" by blowing fusible links to configure AND and OR gates to perform his desired logic function. Complex interconnections which previously required time-consuming layout are thus "lifted" from PC board etch and placed on silicon where they can be easily modified during prototype check-out or production.

The PAL transfer function is the familiar sum of products. Like the PROM, the PAL has a single array of fusible links. Unlike the PROM, the PAL is a programmable AND array driving a fixed OR array (the PROM is a fixed AND array driving a programmable OR array).

The HAL transfer function is the familiar sum of products. Like the ROM, the HAL has a single array of selectable gates. Unlike the ROM, the HAL is a selectable AND array driving a fixed OR array (the ROM is a fixed AND array driving a selectable OR array).

In addition the PAL/HAL provides these options:

- **Variable input/output pin ratio**
- **Programmable three-state outputs**
- **Registers with feedback**
- **Arithmetic capability**
- **Exclusive-OR gates**

PAL®, (Programmable Array Logic), PALASM®, HAL®, and SKINNYDIP® are registered trademarks and PMSI, and HMSI are trademarks of Monolithic Memories Inc.

Unused inputs are tied directly to V_{CC} or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state. Registers consist of D type flip-flops which are loaded on the low-to-high transition of the clock. PAL/HAL Logic Diagrams are shown with all fuses blown, enabling the designer to use the diagrams as coding sheets.

The entire PAL family is programmed using inexpensive conventional PROM programmers with appropriate personality and socket adapter cards. Once the PAL is programmed and verified, two additional fuses may be blown to defeat verification. This feature gives the user a proprietary circuit which is very difficult to copy.

To design a HAL, the user first programs and debugs a PAL using PALASM and the "PAL DESIGN SPECIFICATION" standard format. This specification is submitted to Monolithic Memories where it is computer processed and assigned a bit pattern number, e.g., P01234.

Monolithic Memories will provide a PAL sample for customer qualification. The user then submits a purchase order for a HAL of the specified bit pattern number, e.g., HAL18L4 P01234. See Ordering Information below.

Ordering Information

PAL 16 L8 -2 M J 883B P01234

- PAL = PROGRAMMABLE FAMILY
HAL = HARD ARRAY FAMILY
- NUMBER OF ARRAY INPUTS
- OUTPUT TYPE
  - H = ACTIVE HIGH
  - L = ACTIVE LOW
  - C = COMPLEMENTARY
  - R = REGISTERED
  - X = EXCLUSIVE-OR REGISTERED
  - A = ARITHMETIC REGISTERED
- NUMBER OF OUTPUTS
- SPEED/POWER
  - A = HIGH SPEED
  - -2 = 1/2 POWER
  - -4 = 1/4 POWER
  - A-2 = HIGH SPEED AND 1/2 POWER
  - A-4 = HIGH SPEED AND 1/4 POWER
- TEMPERATURE RANGE
  - C = 0C TO +75C
  - M = -55C TO +125C
(CASE TEMPERATURE)
- PACKAGE
  - N = PLASTIC DIP, 20 PIN
  - J = CERAMIC DIP, 20 PIN
  - F = FLAT PACK
  - L = LEADLESS CHIP CARRIER
  - NS = MOLDED SKINNYDIP, 24 PIN
  - JS = CERAMIC SKINNYDIP, 24 PIN
- OPTIONAL HI-REL PROCESSING
  - 883B = MIL-STD-883, METHOD 5004 & 5005 LEVEL B
  - 883C = MIL-STD-883, METHOD 5004 & 5005 LEVEL C
  - B = MIL-STD-883, METHOD 5004 EQUIVALENT
  - C = MIL-STD-883, METHOD 5004 EQUIVALENT
- BIT PATTERN NUMBER

Monolithic Memories
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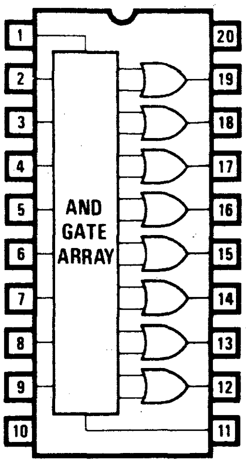
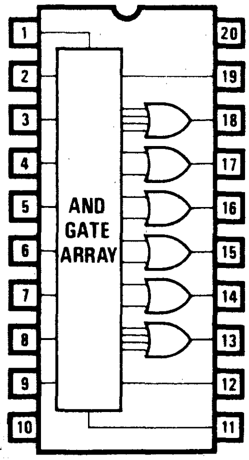
GENERIC LOGIC	PINS	PACKAGE	DESCRIPTION	PART NUMBER			
				STANDARD	HIGH SPEED	1/2 POWER	1/4 POWER
10H8	20	N, J, F, L	Octal 10 Input And-Or Gate Array	PAL10H8 HAL10H8		PAL10H8-2 HAL10H8-2	
12H6	20	N, J, F, L	Hex 12 Input And-Or Gate Array	PAL12H6 HAL12H6		PAL12H6-2 HAL12H6-2	
14H4	20	N, J, F, L	Quad 14 Input And-Or Gate Array	PAL14H4 HAL14H4		PAL14H4-2 HAL14H4-2	
16H2	20	N, J, F, L	Dual 16 Input And-Or Gate Array	PAL16H2 HAL16H2		PAL16H2-2 HAL16H2-2	
16C1	20	N, J, F, L	16 Input And-Or/And-Or-Invert Gate Array	PAL16C1 HAL16C1		PAL16C1-2 PAL16C1-2	
10L8	20	N, J, F, L	Octal 10 Input And-Or-Invert Gate Array	PAL10L8 HAL10L8		PAL10L8-2 HAL10L8-2	
12L6	20	N, J, F, L	Hex 12 Input And-Or-Invert Gate Array	PAL12L6 HAL12L6		PAL12L6-2 HAL12L6-2	
14L4	20	N, J, F, L	Quad 14 Input And-Or-Invert Gate Array	PAL14L4 HAL14L4		PAL14L4-2 HAL14L4-2	
16L2	20	N, J, F, L	Dual 16 Input And-Or-Invert Gate Array	PAL16L2 HAL16L2		PAL16L2-2 HAL16L2-2	
16L8	20	N, J, F, L	Octal 16 Input And-Or-Invert Gate Array	PAL16L8 * HAL16L8	PAL16L8A HAL16L8A	PAL16L8A-2 HAL16L8A-2	PAL16L8A-4 HAL16L8A-4
16R8	20	N, J, F, L	Octal 16 Input Registered And-Or Gate Array	PAL16R8 * HAL16R8	PAL16R8A HAL16R8A	PAL16R8A-2 HAL16R8A-2	PAL16R8A-4 HAL16R8A-4
16R6	20	N, J, F, L	Hex 16 Input Registered And-Or Gate Array	PAL16R6 * HAL16R6	PAL16R6A HAL16R6A	PAL16R6A-2 HAL16R6A-2	PAL16R6A-4 HAL16R6A-4
16R4	20	N, J, F, L	Quad 16 Input Registered And-Or Gate Array	PAL16R4 * HAL16R4	PAL16R4A HAL16R4A	PAL16R4A-2 HAL16R4A-2	PAL16R4A-4 HAL16R4A-4
16X4	20	N, J, F, L	Quad 16 Input Registered And-Or-Xor Gate Array	PAL16X4 HAL16X4			
16A4	20	N, J, F, L	Quad 16 Input Registered And-Carry-Or-Xor Gate Array	PAL16A4 HAL16A4			
12L10	24 (28)	NS,JS,F (L)	Deca 12 Input And-Or-Invert Gate Array	PAL12L10 HAL12L10			
14L8	24 (28)	NS,JS,F (L)	Octal 14 Input And-Or-Invert Gate Array	PAL14L8 HAL14L8			
16L6	24 (28)	NS,JS,F (L)	Hex 16 Input And-Or-Invert Gate Array	PAL16L6 HAL16L6			
18L4	24 (28)	NS,JS,F (L)	Quad 18 Input And-Or-Invert Gate Array	PAL18L4 HAL18L4			
20L2	24 (28)	NS,JS,F (L)	Dual 20 Input And-Or-Invert Gate Array	PAL20L2 HAL20L2			
20C1	24 (28)	NS,JS,F (L)	20 Input And-Or/And-Or Invert Gate Array	PAL20C1 HAL20C1			
20L10	24 (28)	NS,JS,F (L)	Deca 20 Input And-Or-Invert Gate Array	PAL20L10 HAL20L10			
20X10	24 (28)	NS,JS,F (L)	Deca 20 Input Registered And-Or-Xor Gate Array	PAL20X10 HAL20X10			
20X8	24 (28)	NS,JS,F (L)	Octal 20 Input Registered And-Or-Xor Gate Array	PAL20X8 HAL20X8			
20X4	24 (28)	NS,JS,F (L)	Quad 20 Input Registered And-Or-Xor Gate Array	PAL20X4 HAL20X4			
20L8	24 (28)	NS,JS,F (L)	Octal 20 Input And-Or-Invert Gate Array		PAL20L8A HAL20L8A		
20R8	24 (28)	NS,JS,F (L)	Octal 20 Input Registered And-Or Gate Array		PAL20R8A HAL20R8A		
20R6	24 (28)	NS,JS,F (L)	Hex 20 Input Registered And-Or Gate Array		PAL20R6A HAL20R6A		
20R4	24 (28)	NS,JS,F (L)	Quad 20 Input Registered And-Or Gate Array		PAL20R4A HAL20R4A		

* HAL available in "W" package. ( ) = Military Product Standard.

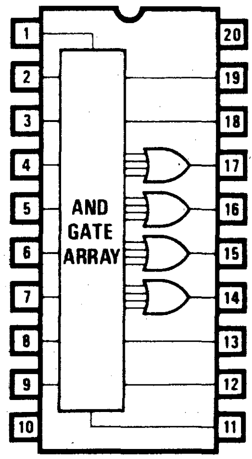
10H8



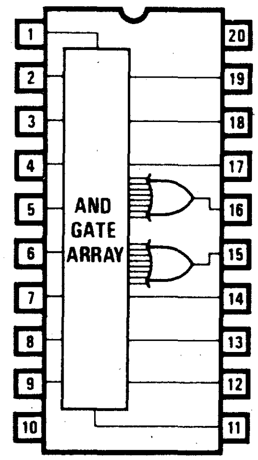
12H6



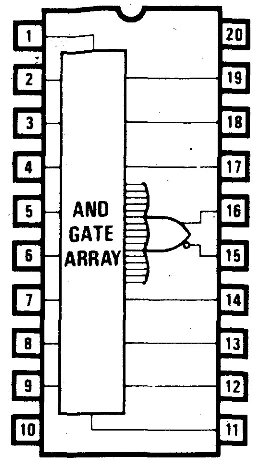
14H4



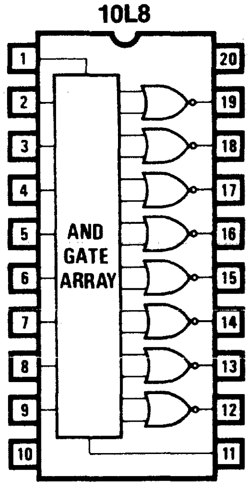
16H2



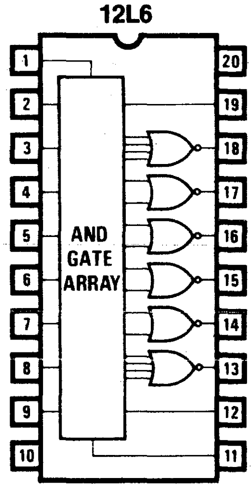
16C1



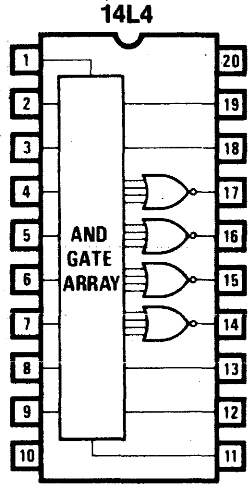
10L8



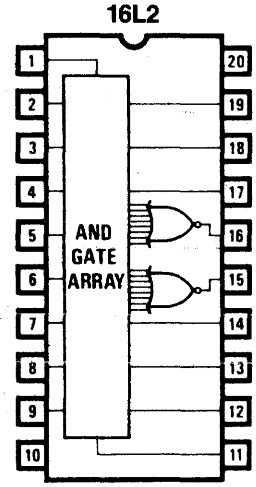
12L6



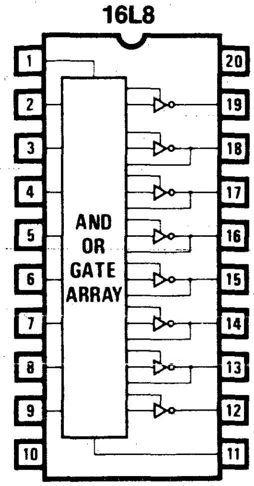
14L4



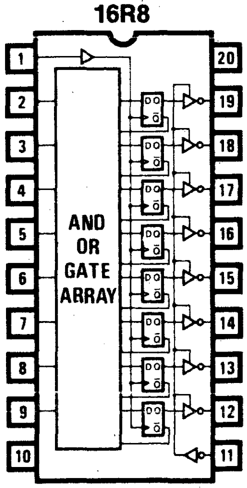
16L2



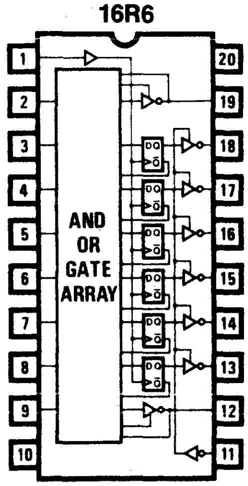
16L8



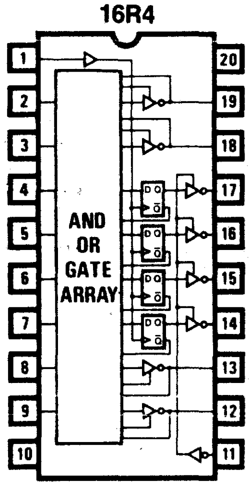
16R8



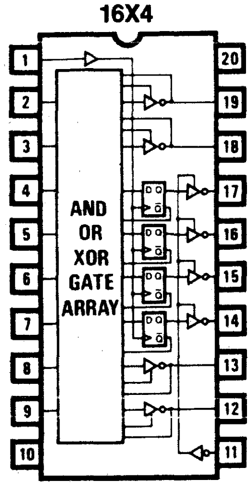
16R6



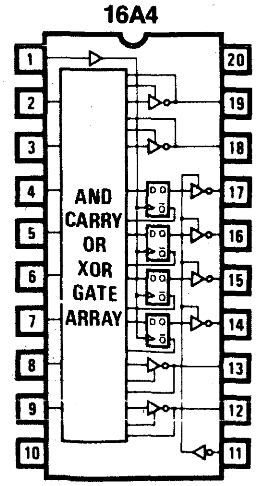
16R4



16X4



16A4



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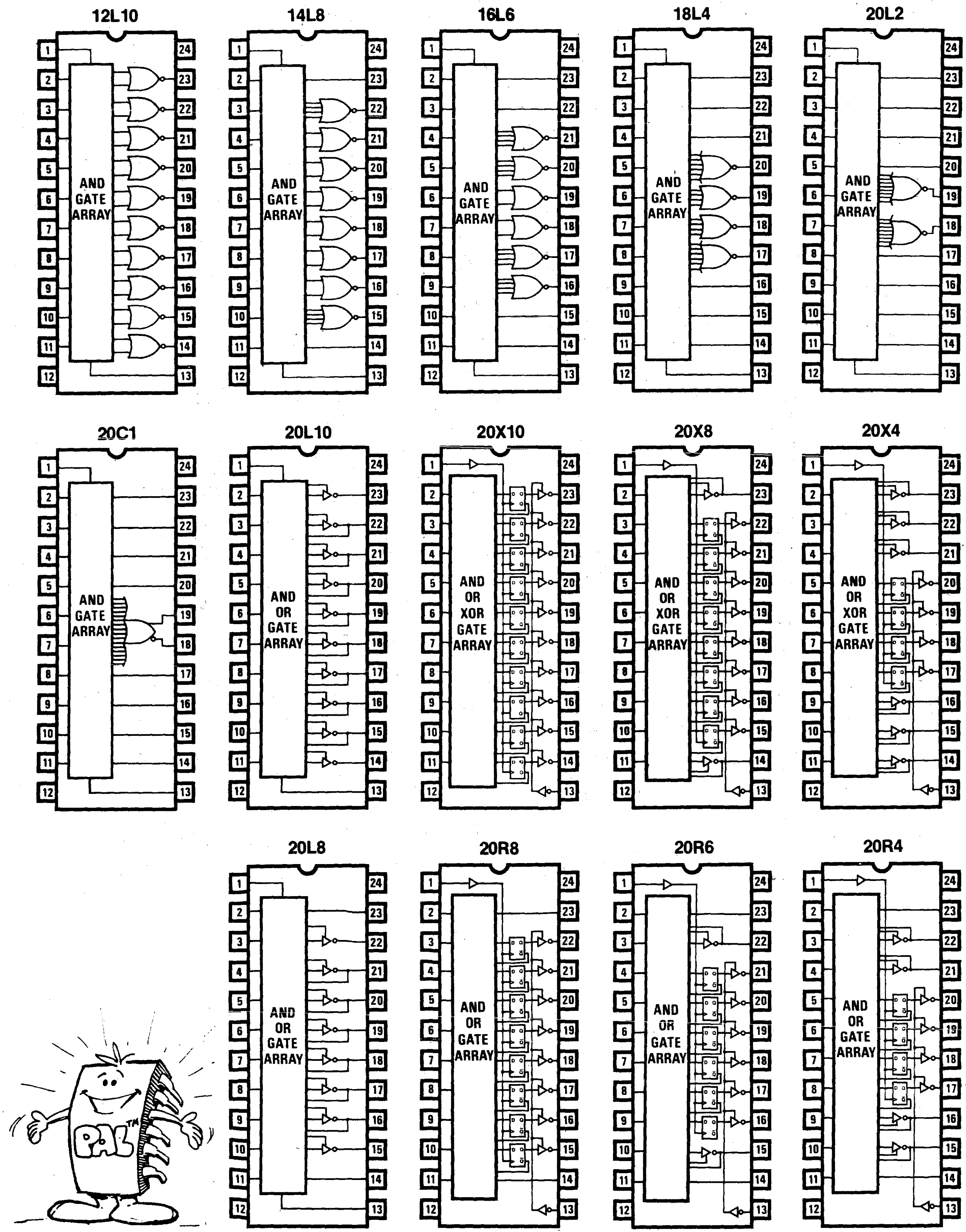

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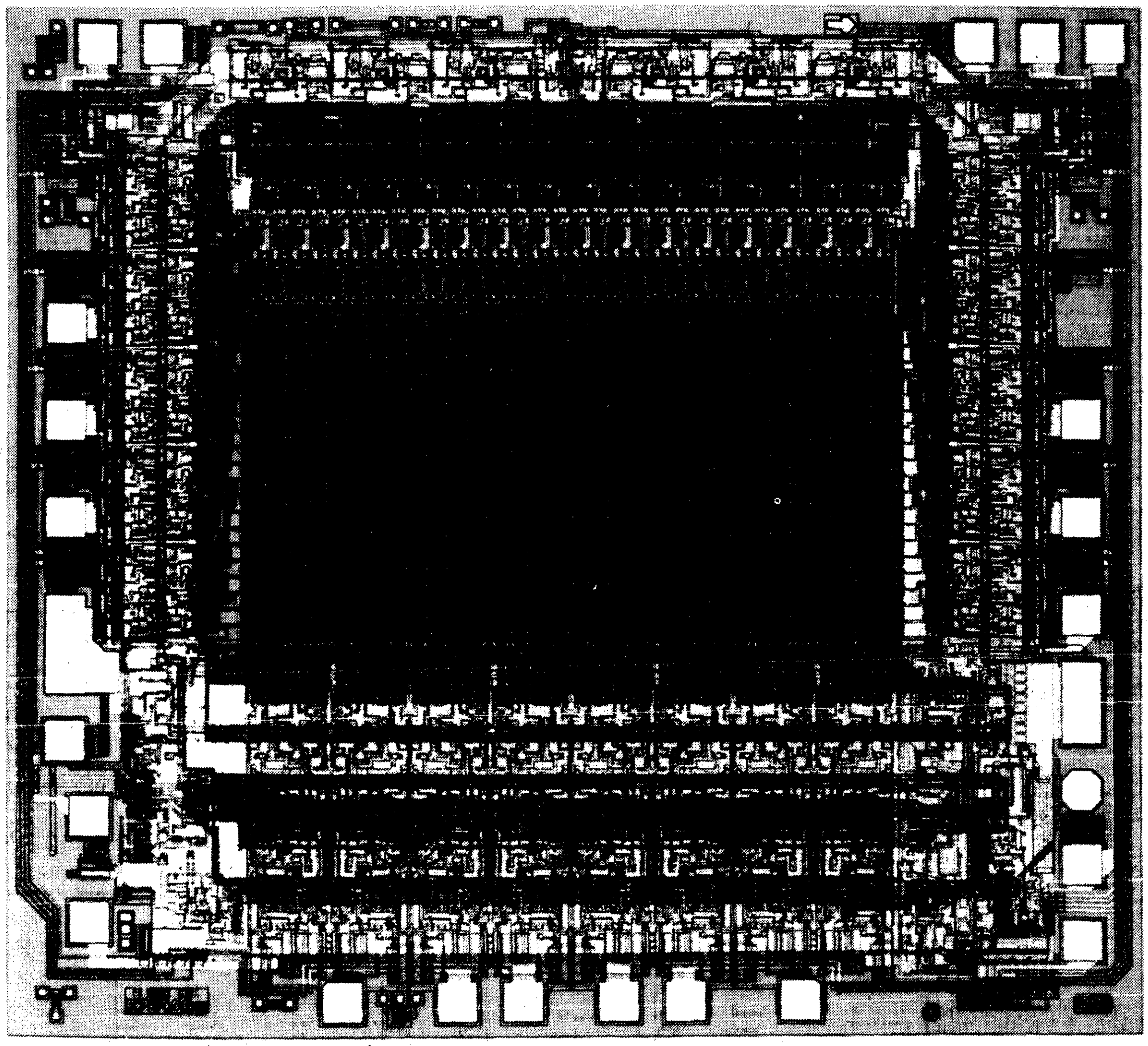
Monolithic Memories



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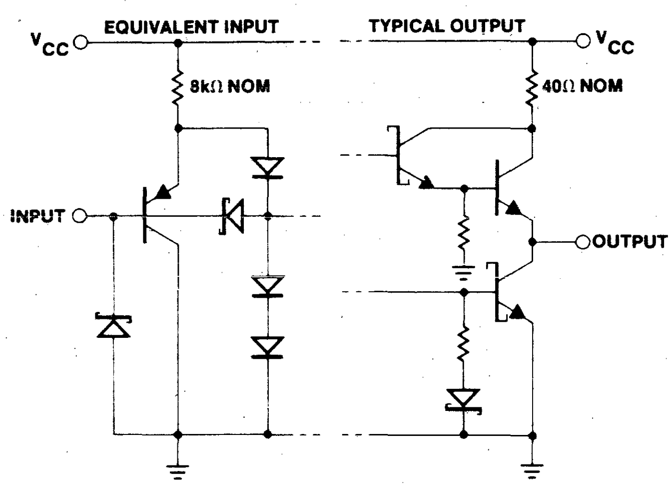
Monolithic Memories MMI

Absolute Maximum Ratings

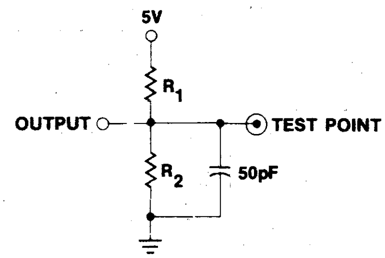
	Operating	Programming
Supply Voltage, V_{CC}	-0.5 to 7.0V	-0.5 to 12.0V
Input Voltage	-1.5 to 5.5V	-1.0 to 22V ⊕
Off-state output Voltage	5.5V	12.0V
Storage temperature		-65° to +150°C

⊕ Pins 1 and 11 may be raised to 20V

Schematic of Inputs and Outputs



Test Load



Other loads may be used.

Typical notes for all the following specifications

Notes: Apply to electrical and switching characteristics

† I/O pin leakage is the worst case of I_{OZX} or I_{IX} e.g., I_{IL} and I_{OZH}.

* These are absolute voltages with respect to the ground pin on the device and includes all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

* * Only one output shorted at a time.

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Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	–55			0		75	°C
T_C	Operating case temperature			125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = –18mA			–0.8	–1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX	V_I = 0.4V			–0.02	–0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL	I_{OL} = 8mA		0.3	0.5	V
			COM	I_{OL} = 8mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL	I_{OH} = –2mA	2.4	2.8		V
			COM	I_{OH} = –3.2mA				
I_{OS}	Output short-circuit current**	V_{CC} = 5V		V_O = 0V	–30	–70	–130	mA
I_{CC}	Supply current	V_{CC} = MAX				55	90	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feed-back to output	Except 16C1	R1 = 560Ω R2 = 1.1kΩ		25	45		25	35	ns
		16C1			25	45		25	40	

Monolithic Memories

CUSTOM/SEMICUSTOM

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Monolithic Memories MMI

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	–55			0		75	°C
T_C	Operating case temperature			125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = –18mA		-0.8	–1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX		V_I = 0.4V		-0.02	–0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL	I_{OL} = 8mA		0.3	0.5	V
			COM	I_{OL} = 8mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL	I_{OH} = –2mA	2.4	2.8		V
			COM	I_{OH} = –3.2mA				
I_{OS}	Output short-circuit current **	V_{CC} = 5V		V_O = 0V	–30	-70	–130	mA
I_{CC}	Supply current	V_{CC} = MAX				60	100	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output	R1 = 560Ω R2 = 1.1kΩ		25	45		25	40	ns

Monolithic Memories

CUSTOM/SEMICUSTOM

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	25	10		25	10		ns
		High	25	10		25	10		
t_{su}	Set up time from input or feedback to clock	16R8 16R6 16R4	45	25		35	25		ns
		16X4 16A4	55	30		45	30		
t_h	Hold time		0	−15		0	−15		ns
T_A	Operating free-air temperature		−55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = −18mA		−0.8	−1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX		V_I = 0.4V		−0.02	−0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL	I_{OL} = 12mA		0.3	0.5	V
			COM	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL	I_{OH} = −2mA	2.4	2.8		V
			COM	I_{OH} = −3.2mA				
I_{OZL}	Off-state output current †	V_{CC} = MAX		V_O = 0.4V			−100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current**	V_{CC} = 5V		V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX	16R4 16R6 16R8 16L8			120	180	mA
			16X4			160	225	
			16A4			170	240	

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feed-back to output	16R6 16R4 16L8	$R_1 = 200\Omega$, $R_2 = 390\Omega$		25	45		25	35	ns
		16X4 16A4			30	45		30	40	ns
t_{CLK}	Clock to output or feedback				15	25		15	25	ns
t_{PZX}	Pin 11 to output enable except 16L8				15	25		15	25	ns
t_{PXZ}	Pin 11 to output disable except 16L8				15	25		15	25	ns
t_{PZX}	Input to output enable	16R6 16R4 16L8			25	45		25	35	ns
		16X4 16A4			30	45		30	40	ns
t_{PXZ}	Input to output disable	16R6 16R4 16L8			25	45		25	35	ns
		16X4 16A4			30	45		30	40	ns
f_{MAX}	Maximum frequency	16R8 16R6 16R4		14	25		16	25		MHz
		16X4 16A4		12	22		14	22		

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Monolithic Memories MMI

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	40	20		35	20		ns
		High	30	10		25	10		ns
t_{su}	Set up time from input or feedback to clock		60	38		50	38		ns
t_h	Hold time		0	-15		0	-15		ns
T_A	Operating free-air temperature		-55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage				0.8	V
V_{IH}*	High-level input voltage		2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN, I_I = –18mA		-0.8	-1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX, V_I = 0.4V		-0.02	-0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX, V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX, V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN; MIL I_{OL} = 12mA; COM I_{OL} = 24mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN; MIL I_{OH} = –2mA; COM I_{OH} = –3.2mA	2.4	2.8		V
I_{OZL}	Off-state output current †	V_{CC} = MAX, V_O = 0.4V			-100	μA
I_{OZH}	Off-state output current †	V_{CC} = MAX, V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current **	V_{CC} = 5V, V_O = 0V	-30	-70	-130	mA
I_{CC}	Supply current	V_{CC} = MAX, 20X10, 20X8, 20X4		120	180	mA
I_{CC}	Supply current	V_{CC} = MAX, 20L10		90	165	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feed-back to output	R_1 = 200Ω, R_2 = 390Ω		35	60		35	50	ns
t_{CLK}	Clock to output or feedback			20	35		20	30	ns
$t_{PXZ/ZX}$	Pin 13 to output disable/enable except 20L10			20	45		20	35	ns
t_{PZX}	Input to output enable except 20X10			35	55		35	45	ns
t_{PXZ}	Input to output disable except 20X10			35	55		35	45	ns
f_{MAX}	Maximum frequency		10.5	16		12.5	16		MHz

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	20	10		15	10		ns
		High	20	10		15	10		ns
t_{su}	Set up time from input or feedback to clock	16R8A 16R6A 16R4A	30	15		25†	15		ns
t_h	Hold time		0	-10		0	-10		ns
T_A	Operating free-air temperature		-55			0		75	°C
T_C	Operating case temperature				125				°C

†Can select 20ns upon customer request.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = −18mA		−0.8	−1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX		V_I = 0.4V		−0.02	−0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL	I_{OL} = 12mA		0.3	0.5	V
			COM	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL	I_{OH} = −2mA	2.4	2.8		V
			COM	I_{OH} = −3.2mA				
I_{OZL}	Off-state output current †	V_{CC} = MAX		V_O = 0.4V			+100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current **	V_{CC} = 5V		V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX				120	180	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feed-back to output	16R6A 16R4A 16L8A	$R_1 = 200\Omega$, $R_2 = 390\Omega$		15	30		15	25	ns
t_{CLK}	Clock to output or feedback				10	20		10	15	ns
t_{PZX}	Pin 11 to output enable except 16L8A				10	25		10	20	ns
t_{PXZ}	Pin 11 to output disable except 16L8A				11	25		11	20	ns
t_{PZX}	Input to output enable	16R6A 16R4A 16L8A			10	30		10	25	ns
t_{PXZ}	Input to output disable	16R6A 16R4A 16L8A			13	30		13	25	ns
f_{MAX}	Maximum frequency	16R8A 16R6A 16R4A		20	40		28.5	40		MHz

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Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	20	7		15	7		ns
		High	20	7		15	7		ns
t_{su}	Set up time from input or feedback to clock	20R8A 20R6A 20R4A	30	15		25	15		ns
t_h	Hold time		0	−10		0	−10		ns
T_A	Operating free-air temperature		−55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = −18mA		−0.8	−1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX		V_I = 0.4V		−0.02	−0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL	I_{OL} = 12mA		0.3	0.5	V
			COM	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL	I_{OH} = −2mA	2.4	2.8		V
			COM	I_{OH} = −3.2mA				
I_{OZL}	Off-state output current †	V_{CC} = MAX		V_O = 0.4V			−100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current **	V_{CC} = 5V		V_O = 0V	−30	−90	−130	mA
I_{CC}	Supply current	V_{CC} = MAX				160	210	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feed-back to output	20R6A 20R4A 20L8A	$R_1 = 200\Omega$ $R_2 = 390\Omega$		15	30		15	25	ns
t_{CLK}	Clock to output or feedback				10	20		10	15	ns
t_{PZX}	Pin 13 to output enable except 20L8A				10	25		10	20	ns
t_{PXZ}	Pin 13 to output disable except 20L8A				11	25		11	20	ns
t_{PZX}	Input to output enable	20R6A 20R4A 20L8A			10	30		10	25	ns
t_{PXZ}	Input to output disable	20R6A 20R4A 20L8A			13	30		13	25	ns
f_{MAX}	Maximum frequency	20R8A 20R6A 20R4A		20	40		28.5	40		MHz

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Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	–55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage					0.8	V
V_{IH}*	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = –18mA		–0.8	–1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX	V_I = 0.4V		–0.02	–0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX	V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL I_{OL} = 4mA COM I_{OL} = 4mA		0.3	0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL I_{OH} = –1mA COM I_{OH} = –1mA	2.4	2.8		V
I_{OS}	Output short-circuit current**	V_{CC} = 5V	V_O = 0V	–30	–70	–130	mA
I_{CC}	Supply current	V_{CC} = MAX			30	45	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output	R1 = 1.12kΩ R2 = 2.2kΩ		45	80		45	60	ns

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	25	10		25	10		ns
		High	25	10		25	10		ns
t_{su}	Set up time from input or feedback to clock	16R6A-2 16R4A-2 16R8A-2	50	25		35	25		ns
t_h	Hold time		0	-15		0	-15		ns
T_A	Operating free-air temperature		-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = −18mA		-0.8	-1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX		V_I = 0.4V		-0.02	-0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL	I_{OL} = 12mA		0.3	0.5	V
			COM	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL	I_{OH} = -2mA	2.4	2.8		V
			COM	I_{OH} = -3.2mA				
I_{OZL}	Off-state output current †	V_{CC} = MAX		V_O = 0.4V			-100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current **	V_{CC} = 5V		V_O = 0V	-30	-70	-130	mA
I_{CC}	Supply current	V_{CC} = MAX				60	90	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feed-back to output	16L8A-2 16R6A-2 16R4A-2	R_1 = 200Ω R_2 = 390Ω		25	50		25	35	ns
t_{CLK}	Clock to output or feedback				15	25		15	25	ns
$t_{PXZ/ZX}$	Pin 11 to output disable/enable except 16L8A-2				15	25		15	25	ns
t_{PZX}	Input to output enable	16L8A-2 16R6A-2 16R4A-2			25	45		25	35	ns
t_{PXZ}	Input to output disable	16R8A-2 16R6A-2 16R4A-2			25	45		25	35	ns
f_{MAX}	Maximum frequency	16R8A-2 16R6A-2 16R4A-2		14	25		16	25		MHz

Operating Conditions

SYMBOL	PARAMETER			MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	16R8A-4 16R6A-4 16R4A-4	Low	40	20		30	20		ns
			High	40	20		30	20		
t_{su}	Set up time from input or feedback to clock	16R8A-4 16R6A-4 16R4A-4		90	45		60	45		ns
t_h	Hold time			0	-15		0	-15		ns
T_A	Operating free-air temperature			-55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = -18mA		-0.8	-1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX		V_I = 0.4V		-0.02	-0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	MIL	I_{OL} = 4mA		0.3	0.5	V
			COM	I_{OL} = 8mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	MIL	I_{OH} = -1mA	2.4	2.8		V
			COM	I_{OH} = -1 mA				
I_{OZL}	Output short-circuit current**	V_{CC} = MAX		V_O = 0.4V			-100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current	V_{CC} = 5V		V_O = 0V	-30	-70	-130	mA
I_{CC}	Supply current	V_{CC} = MAX		16R4A-4 16R6A-4 16R8A-4 16L8A-4		30	50	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feed-back to output	16R6A-4 16R4A-4 16L8A-4	R_1 = 800Ω R_2 = 1.56kΩ		35	75		35	55	ns
t_{CLK}	Clock to output or feedback				20	45		20	35	ns
$t_{PXZ/ZX}$	Pin 11 to output disable/enable—except 16L8A-4				15	40		15	30	ns
t_{PZX}	Input to output enable	16R6A-4 16R4A-4 16L8A-4			30	65		30	50	ns
t_{PXZ}	Input to output disable	16R6A-4 16R4A-4 16L8A-4			30	65		30	50	ns
f_{MAX}	Maximum frequency	16R8A-4 16R6A-4 16R4A-4		8	18		11	18		MHz

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Monolithic Memories MMI

Programming/Verifying Procedure

NOTES: For programming purposes many PAL pins have double functions.

For The PAL 20:

As long as Pin 1 is at HH, Pin 11 is at ground, and Pin 12 is either at HH or Z (as defined in Table 1) — Pins 16, 17, 18, and 19 are outputs. The other pin functions are: I0 (Pin 2) through I7 (Pin 9) plus Pin 12 address the proper row; A0 (Pin 15), A1 (Pin 14), and A2 (Pin 13) address the proper product lines.

When Pin 11 is at HH, Pin 1 is at ground and Pin 19 is either at HH or Z — Pins 12, 13, 14, and 15 are outputs. The other pin functions are: I0 (Pin 2) through I7 (Pin 9) plus Pin 19 address the proper row; A0 (now Pin 18), A1 (now Pin 17), and A2 (now Pin 16) address the proper product lines.

For The PAL 24:

As long as Pin 1 is at HH, Pin 13 is at ground and Pin 14 is either at HH or Z (as defined in Table 1) — Pins 19, 20, 21, 22, and 23 are outputs. The other pin functions are: I0 (Pin 2) through I9 (Pin 11) plus Pin 14 address the proper row; A0 (Pin 15), A1 (Pin 16), and A2 (Pin 17) address the proper product lines.

As long as Pin 13 is at HH, Pin 1 is at ground, and Pin 23 is either at HH or Z (as defined in Table 1) — Pins 14, 15, 16, 17, and 18 are outputs. The other pin functions are: I0 (Pin 2) through I9 (Pin 11) plus Pin 23 address the proper row; A0 (Pin 22), A1 (Pin 21), and A2 (Pin 20) address the proper product lines.

For The PAL 24A:

As long as Pin 1 is at HH, Pin 13 is at ground, and Pin 14 is either at HH or Z (as defined in Table 1) — Pins 19, 20, 21, and 22 are outputs. The other pin functions are: I0 (Pin 2) through I9 (Pin 11) plus Pin 14 address the proper row; A0 (Pin 15), A1 (Pin 16), and A2 (Pin 17) address the proper product lines.

As long as Pin 13 is at HH, Pin 1 is at ground, and Pin 23 is either at HH or Z (as defined in Table 1) — pins 15, 16, 17, and 18 are outputs. The other Pin functions are: I0 (Pin 2) through I9 (Pin 11) plus Pin 23 address the proper row; A0 (Pin 22), A1 (Pin 21), and A2 (Pin 20) address the proper product lines.

Pre-Verification

5.1.1 Raise V_{CC} to 5.0 volts.

5.1.2 Raise Output Disable pin, OD, to VIHH.

5.1.3 Select an input line by specifying Inputs and L/R as shown in Table 1 or Table 2.

5.1.4 Select a product line by specifying A0, A1, and A2 one-of-eight select as shown in Table 3, Table 4 or Table 5.

5.1.5 Pulse the CLOCK pin and verify (with CLOCK at VIL) that the output pin, O, is in the state corresponding to an unblown fuse.

— For verified unblown condition, continue procedure from 5.1.3 through 5.1.5.

— For verified blown condition, stop procedure and reject part.

Programming Algorithm

5.2.1 Raise Output Disable pin, OD, to VIHH

5.2.2 Programming pass. For all fuses to be blown:

5.2.2.1 Lower CLOCK pin to ground.

5.2.2.2 Select an input line by specifying Inputs and L/R as shown in Table 1 or Table 2.

5.2.2.3 Select a product line by specifying A0, A1, and A2 one-of-eight select as shown in Table 3, Table 4 or Table 5.

5.2.2.4 Raise V_{CC} to VIHH.

5.2.2.5 Program the fuse by pulsing the output pins of the selected product group -one at a time- to VIHH (as shown in the Programming Waveforms, Section 5.5).

5.2.2.6 Lower V_{CC} to 5.0 volts.

5.2.2.7 Repeat this procedure from 5.2.2.2 until pattern is complete.

5.2.3 First verification pass. For all fuse locations:

5.2.3.1 Select an input line by specifying Inputs and L/R as shown in Table 1 or Table 2.

5.2.3.2 Select a product line by specifying A0, A1, and A2 one-of-eight select as shown in Table 3, Table 4 or Table 5.

5.2.3.3 Pulse the CLOCK pin and verify (with CLOCK at VIL) that the output pin, O, is in the correct state.

— For verified output state, continue procedure

— For overblow condition, stop procedure and reject part.

— For underblow condition, reexecute steps 5.2.2.4 through 5.2.2.6 and 5.2.2.3. If successful, continue procedure. After three attempts to blow fuse without success, reject part but continue procedure.

5.2.3.4 Repeat this procedure from 5.2.3.1 until the entire array is exercised.

5.2.4 High Voltage Verify. For all fuse locations:

5.2.4.1 Raise V_{CC} to 5.5 volts.

5.2.4.2 Select an input line by specifying Inputs and L/R as shown in Table 1 or Table 2.

5.2.4.3 Select a product line by specifying A0, A1, and A2 one-of-eight select as shown in Table 3, Table 4 or Table 5.

5.2.4.4 Pulse the CLOCK pin and verify (with CLOCK at VIL) that the output pin, O, is in the correct state.

— For verified output state, continue procedure

— For invalid output state, stop procedure and reject part.

5.2.4.5 Repeat this procedure from 5.2.4.1 until the entire array is exercised.

5.2.5 Low Voltage Verify. For all fuse locations:

5.2.5.1 Lower V_{CC} to 4.5 volts.

5.2.5.2 Select an input line by specifying Inputs and L/R as shown in Table 1 or Table 2.

5.2.5.3 Select a product line by specifying A0, A1, and A2, one-of-eight select as shown in Table 3, Table 4 or Table 5.

5.2.5.4 Pulse the CLOCK pin and verify (with CLOCK at VIL) that the output pin, O, is in the correct state.
- For verified output state, continue procedure.
- For invalid output state, continue procedure and reject part.

Programming the Security Fuses

5.3.1 Verify per Section 5.2.4 and 5.2.5.

5.3.2 Raise V_{CC} to 6 volts.

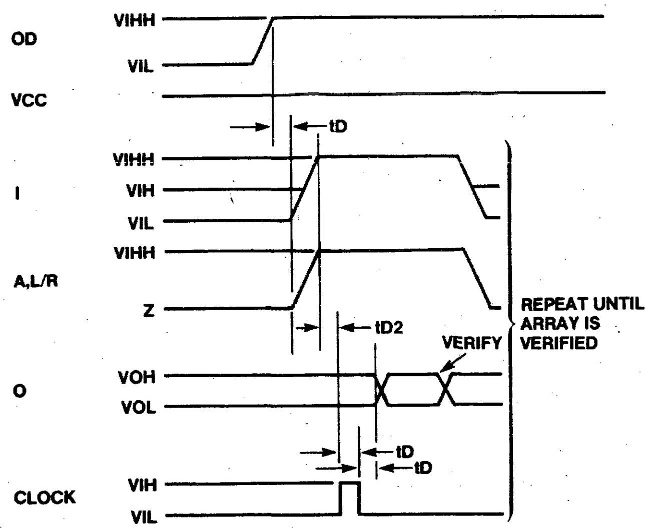
5.3.3 For PAL 20:
- Program the first fuse by pulsing Pin 1 to VP. (From 1 to 5 pulses is acceptable.)
- Program the second fuse by pulsing Pin 11 to VP. (From 1 to 5 pulses is acceptable.)

5.3.4 For PAL 24 and PAL 24A:
- Program the first fuse by pulsing Pin 1 to VP. (From 1 to 5 pulses is acceptable.)
- Program the second fuse by pulsing Pin 13 to VP. (From 1 to 5 pulses is acceptable.)

5.3.5 Verify per Section 5.2.4 and 5.2.5:
- A device is "secure" if either half fails to verify.

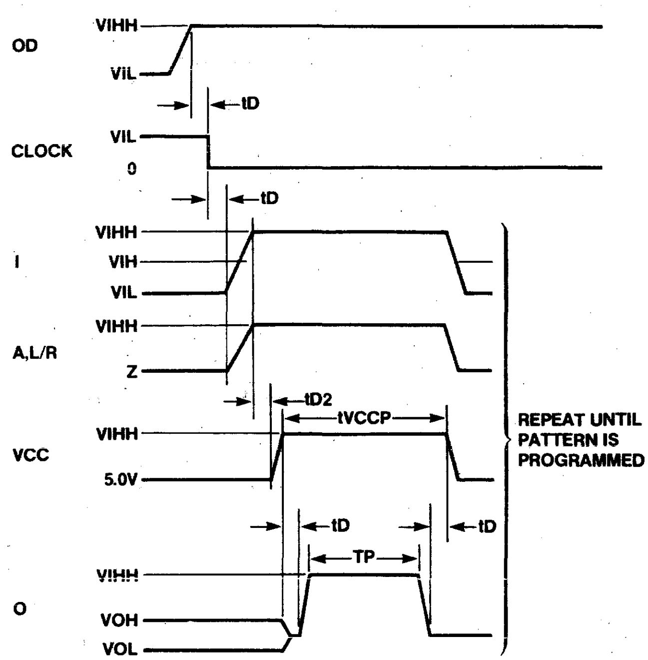
5.4 Programming Parameters

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNIT
V_{IHH}	Program-level input voltage		11.5	11.75	12	V
I_{IHH}	Program-level input current	Output Program Pulse			50	mA
		OD, L/R			50	mA
		All other inputs			10	mA
I_{CCH}	Program Supply Current				900	mA
t_{VCCP}	Pulse Width of V_{CC} @ V_{IHH}				60	µS
T_P	Program Pulse Width		10	20	50	µS
t_D	Delay Time		100			ns
t_{D2}	Delay Time after L/R Pin		10			µS
	V_{CCP} Duty Cycle				20	%
V_P	Security Fuse Programming Voltage		18	18.5	19	V
I_P	Security Fuse Programming Supply Current				400	mA
T_{PP}	Security Fuse Programming Pulse Width		10	40	70	µS
	Security Fuse Programming Duty Cycle				50	%
t_{RP}	Rise time of output programming and address pulses		1	1.5	10	V/µS
t_{RP}	Rise Time of security fuse programming pulses		1	1.5	10	V/µS
V_{CCPP}	V_{CC} value during security fuse programming		5.75	6.0	6.25	V
	V_{CC} value for first verify		4.75	5.0	5.25	V
	V_{CC} value for High V_{CC} verify		5.4	5.5	5.6	V
	V_{CC} value for Low V_{CC} verify		4.4	4.5	4.6	V

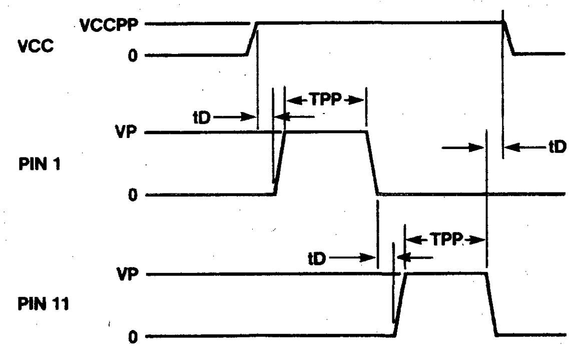


NOTE: VCC (Low Voltage Verify) = 4.5 volts
VCC (High Voltage Verify) = 5.5 volts
VCC (First Verify) = 5.0 volts
A Delay (tD2) must always precede the Positive Clock Transition. (e.g see section 5.2.3.3 for underblow condition)

5.5 ARRAY PROGRAMMING



5.6 SECURITY FUSE PROGRAMMING



Programmer/Development Systems

VENDOR	PAL 20s (ALL)	PAL 24s (STD)	PAL 24s (FAST)
Data I/O	— LogicPak (Rev-010) — 1427 Card Set	LogicPak (Rev-010)	— LogicPak (Rev-010)
Structured Design	— SD 20/24 — PAL Burner*	— SD 20/24 — PAL Burner*	— SD 20/24 — PAL Burner*
STAG	— PM202 (Rev 3) — PM2200*	— PM202 (Rev 3) — PM2200*	— PM202 (Rev) — PM2200*
DIGELEC	— UP803 (FAM51) or (FAM52)	— UP803 (FAM51) or (FAM52)	— UP803 (FAM51) or (FAM52)
PROLOG	— M980 PM9068		
KONTRON	— MPP80S MOD 21		

*Means that this version is being qualified.

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Programming Pin Configurations

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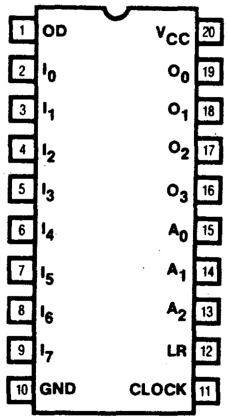
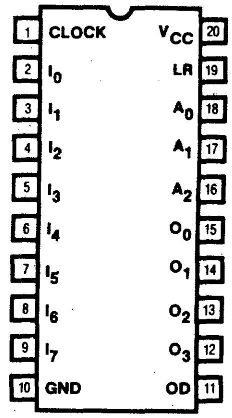


PRODUCTS 32 THRU 63



Voltage Legend

L = Low-level input voltage, V_{IL}
H = High-level input voltage, V_{IH}
HH = High-level program voltage, V_{IHH}
Z = High impedance (e.g., 10kΩ to 5.0V)

INPUT LINE NUMBER	PIN IDENTIFICATION								
	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	L/R
0	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	H	HH	HH	HH	HH	HH	HH	HH
28	L	HH	HH	HH	HH	HH	HH	HH	Z
29	H	HH	HH	HH	HH	HH	HH	HH	Z
30	L	HH	HH	HH	HH	HH	HH	HH	HH
31	H	HH	HH	HH	HH	HH	HH	HH	HH

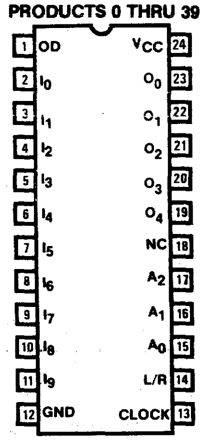
Table 1 Input Line Select

PRODUCT LINE NUMBER	PIN IDENTIFICATION						
	O_3	O_2	O_1	O_0	A_2	A_1	A_0
0, 32	Z	Z	Z	HH	Z	Z	Z
1, 33	Z	Z	Z	HH	Z	Z	HH
2, 34	Z	Z	Z	HH	Z	HH	Z
3, 35	Z	Z	Z	HH	Z	HH	HH
4, 36	Z	Z	Z	HH	HH	Z	Z
5, 37	Z	Z	Z	HH	HH	Z	HH
6, 38	Z	Z	Z	HH	HH	HH	Z
7, 39	Z	Z	Z	HH	HH	HH	HH
8, 40	Z	Z	HH	Z	Z	Z	Z
9, 41	Z	Z	HH	Z	Z	Z	HH
10, 42	Z	Z	HH	Z	Z	HH	Z
11, 43	Z	Z	HH	Z	Z	HH	HH
12, 44	Z	Z	HH	Z	HH	Z	Z
13, 45	Z	Z	HH	Z	HH	Z	HH
14, 46	Z	Z	HH	Z	HH	HH	Z
15, 47	Z	Z	HH	Z	HH	HH	HH
16, 48	Z	HH	Z	Z	Z	Z	Z
17, 49	Z	HH	Z	Z	Z	Z	HH
18, 50	Z	HH	Z	Z	Z	HH	Z
19, 51	Z	HH	Z	Z	Z	HH	HH
20, 52	Z	HH	Z	Z	HH	Z	Z
21, 53	Z	HH	Z	Z	HH	Z	HH
22, 54	Z	HH	Z	Z	HH	HH	Z
23, 55	Z	HH	Z	Z	HH	HH	HH
24, 56	HH	Z	Z	Z	Z	Z	Z
25, 57	HH	Z	Z	Z	Z	Z	HH
26, 58	HH	Z	Z	Z	Z	HH	Z
27, 59	HH	Z	Z	Z	Z	HH	HH
28, 60	HH	Z	Z	Z	HH	Z	Z
29, 61	HH	Z	Z	Z	HH	Z	HH
30, 62	HH	Z	Z	Z	HH	HH	Z
31, 63	HH	Z	Z	Z	HH	HH	HH

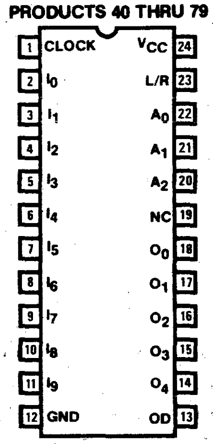
Table 2 Product Line Select

Programming Pin Configurations

PRODUCTS 0 THRU 39



PRODUCTS 40 THRU 79



Voltage Legend

L = Low-level input voltage, V_{IL}
H = High-level input voltage, V_{IH}
HH = High-level program voltage, V_{IHH}
Z = High impedance (e.g. 10K Ω to 5.0V)

INPUT LINE NUMBER	PIN IDENTIFICATION										
	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	L/R
0	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	HH
28	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	Z
29	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	Z
30	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	HH
31	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	HH
32	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	Z
33	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	Z
34	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	HH
35	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	HH
36	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
37	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
38	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH
39	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH

Table 1 Input Line Select

PRODUCT LINE NUMBER	PIN IDENTIFICATION							
	O_4	O_3	O_2	O_1	O_0	A_2	A_1	A_0
0, 40	Z	Z	Z	Z	HH	Z	Z	Z
1, 41	Z	Z	Z	Z	HH	Z	Z	HH
2, 42	Z	Z	Z	Z	HH	Z	HH	Z
3, 43	Z	Z	Z	Z	HH	Z	HH	HH
4, 44	Z	Z	Z	Z	HH	HH	Z	Z
5, 45	Z	Z	Z	Z	HH	HH	Z	HH
6, 46	Z	Z	Z	Z	HH	HH	HH	Z
7, 47	Z	Z	Z	Z	HH	HH	HH	HH
8, 48	Z	Z	Z	HH	Z	Z	Z	Z
9, 49	Z	Z	Z	HH	Z	Z	Z	HH
10, 50	Z	Z	Z	HH	Z	Z	HH	Z
11, 51	Z	Z	Z	HH	Z	Z	HH	HH
12, 52	Z	Z	Z	HH	Z	HH	Z	Z
13, 53	Z	Z	Z	HH	Z	HH	Z	HH
14, 54	Z	Z	Z	HH	Z	HH	HH	Z
15, 55	Z	Z	Z	HH	Z	HH	HH	HH
16, 56	Z	Z	HH	Z	Z	Z	Z	Z
17, 57	Z	Z	HH	Z	Z	Z	Z	HH
18, 58	Z	Z	HH	Z	Z	Z	HH	Z
19, 59	Z	Z	HH	Z	Z	Z	HH	HH
20, 60	Z	Z	HH	Z	Z	HH	Z	Z
21, 61	Z	Z	HH	Z	Z	HH	Z	HH
22, 62	Z	Z	HH	Z	Z	HH	HH	Z
23, 63	Z	Z	HH	Z	Z	HH	HH	HH
24, 64	Z	HH	Z	Z	Z	Z	Z	Z
25, 65	Z	HH	Z	Z	Z	Z	Z	HH
26, 66	Z	HH	Z	Z	Z	Z	HH	Z
27, 67	Z	HH	Z	Z	Z	Z	HH	HH
28, 68	Z	HH	Z	Z	Z	HH	Z	Z
29, 69	Z	HH	Z	Z	Z	HH	Z	HH
30, 70	Z	HH	Z	Z	Z	HH	HH	Z
31, 71	Z	HH	Z	Z	Z	HH	HH	HH
32, 72	HH	Z	Z	Z	Z	Z	Z	Z
33, 73	HH	Z	Z	Z	Z	Z	Z	HH
34, 74	HH	Z	Z	Z	Z	Z	HH	Z
35, 75	HH	Z	Z	Z	Z	Z	HH	HH
36, 76	HH	Z	Z	Z	Z	HH	Z	Z
37, 77	HH	Z	Z	Z	Z	HH	Z	HH
38, 78	HH	Z	Z	Z	Z	HH	HH	Z
39, 79	HH	Z	Z	Z	Z	HH	HH	HH

Table 2 Product Line Select

2175 Mission College Boulevard, Santa Clara, CA 95050 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374
Monolithic Memories

MOTOROLA

FOR CUSTOM LSI/VLSI BIPOLAR CIRCUITS

High Performance ALS-TTL-Compatible Macrocell Arrays

MCA500ALS MCA1300ALS MCA2800ALS

In addition to standard logic lines, Motorola also offers a variety of TTL-compatible Macrocell Arrays. These products provide a means for developing economical custom LSI/VLSI logic circuits. Performance is achieved by the combination of an advanced MOSAIC I (Motorola Oxide-Isolated Self-Aligned Implanted Circuit) oxide isolated bipolar integrated circuit process and a series gated emitter-coupled logic (ECL) macrocell circuit technology. Input and output circuits provide level translation to and from the internal array logic for standard TTL/MOS interface.

Each cell within the arrays contains a number of unconnected transistors and resistors. Stored within a computer are the specifications to automatically interconnect these elements forming SSI/MSI logic cells (rather than simple gates) called macrocells. These macrocells take the form of standard logic blocks such as dual type D flip-flops, dual full adders, quad latches and many other pre-defined "library" functions. Presently, the macrocell library for the ALS-TTL arrays contains more than 80 logic functions.

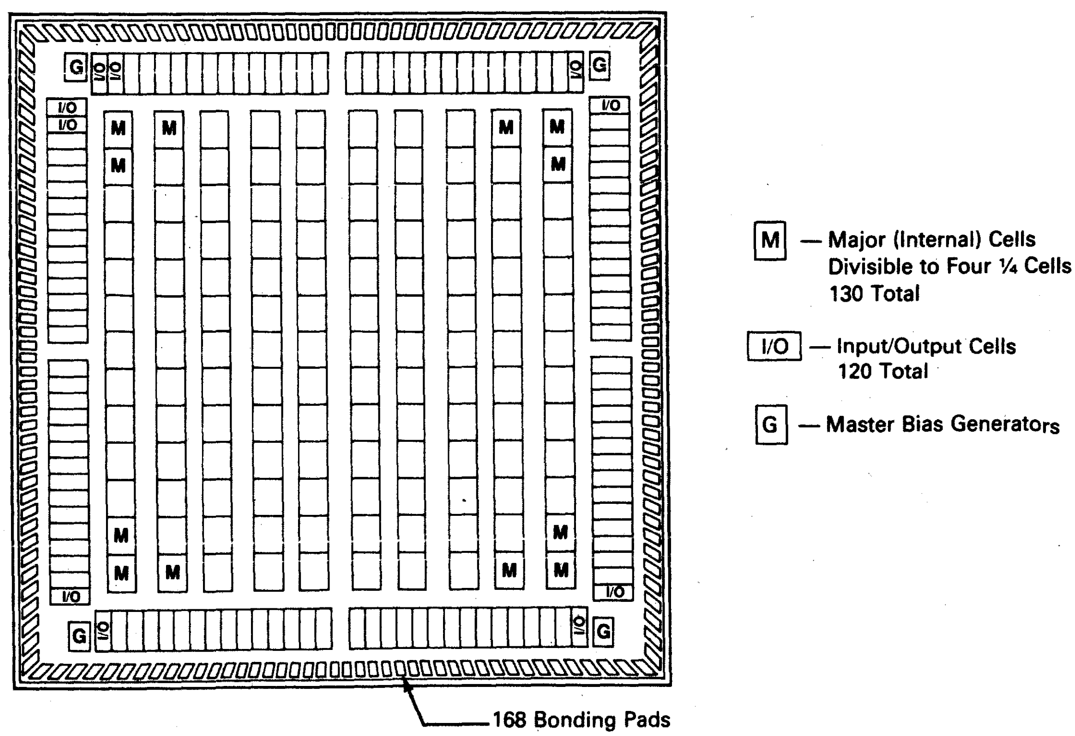
Generating an LSI/VLSI design is simply a matter of selecting the appropriate macrocells and describing the proper interconnection network to implement the design. Motorola's CAD (Computer-Aided-Design) interface provides automatic placement and routing of the cells (intraconnection of the cell itself is automatically accomplished when placed), full logic and fault-testing capabilities, AC delay simulations, generation of test tapes and custom metallization to complete the IC processing sequence.

The ability to stockpile fully diffused wafers provides a very fast turnaround time (the time from customer notification of a completed design to delivery of finished parts) of currently nine weeks.

ALS-TTL MCA Selection Chart

	MCA 500ALS	MCA 1300ALS	MCA 2800ALS	MCA 2400ETL
Configuration				
Max Gate Equivalent	533	1280	2720	2958
Major Macrocells	24	60	30	130
I/O Ports	57	76	120	120
Input/Interface Cells	26	40	120 I/O	70TTL I/O
Output Marcocells	24	40		72ECL
Performance				
Max Gate Delay (M Cell)	4.0 ns	3.0 ns	1.1 ns	1.1 ns
Max Toggle Frequency	80 MHz	80 MHz	125 MHz	125 MHz
Maximum Power Dissipation	1.0 W	1.4 W	2.5 W	4.0 W
Packages				
Dual-In-Line	28, 40, 48	40, 48	—	
Chip Carrier, Pin Grid Array	68	68, 84	84,149PG	149PG
Temperature Range	0–70°C	0–70°C	0–70°C	0–70°C
Supply Voltage	5.0 V ±5%	5.0 V ±5%	5.0 V ±5%	+5.0, −5.2 V
Availability	Now	Now	Now	4Q83

MCA2800ALS MACROCELL ARRAY LAYOUT



MOTOROLA

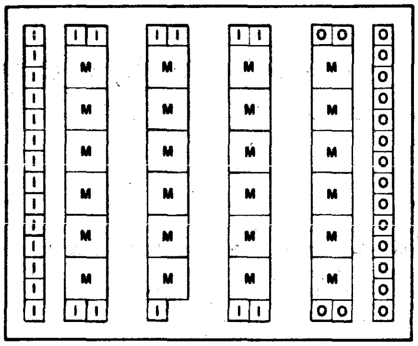
MECL 10,000 Macrocell Array Family

The Macrocell Array Concept combines a pre-diffused array of components with computer-aided design techniques to offer system designers a rapid, cost-effective means for implementing semi-custom, high-speed digital logic systems with VLSI circuitry.

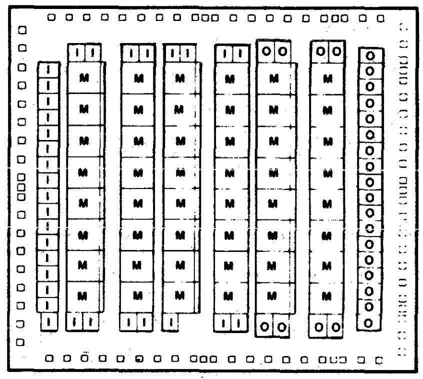
Compared with equivalent systems developed with discrete logic (separately packed SSI/MSI logic functions) the high packing density of the Macrocell array chip offers up to 100-to-1 reduction in system component count, with a power dissipation improvement (reduction) of as much as 12 to 1.

Compared with the conventional approach to custom LSI circuits, the Macrocell approach offers a tremendous reduction in delivery time. With a stockpile of fully diffused wafers, turnaround time (from the time the customer gives the go-ahead signal for generating masks until he receives finished parts) is seven weeks.

MECL Macrocell Array family members presently consist of the MCA1200ECL (68 Pin) Array, the MCA600ECL (28, 40 and 68 Pin) Array, and the MCA2500ECL (149 Pin) Array.



THE MCA600ECL
Total of 67 cell locations—24 Major, 25 Interface and 18 Output cell locations.



THE MCA1200ECL
Total of 106 cell locations—48 Major, 32 Interface and 26 Output cell locations.

Parameter	MCA2500ECL	MCA1200ECL	MCA600ECL
Maximum Equivalent Gates	2472	1192	652
Major Macrocells	110	48	24
Interface/Input Macrocells	—	32	25
Output Macrocells	68	26	18
Maximum Gate Delay	0.5 ns	1.2 ns	1.2 ns
Power Dissipation	6.0 Watts	4 Watts	2.5 Watts
Package	149 Pin Grid Array	68 Leadless 72 Pin Grid	28,40 DIL 68 Leadless
Temperature Range	0–70°C	0–70°C	0–70°C
I/O Interface	10K/10KH/100K	MECL 10K/10KH	MECL 10K/10KH
Design Interface	CAD	CAD	CAD

M10900 Family

The M10900 family is a series of very high performance bipolar LSI products designed off the MECL Macrocell Array offering. While the Macrocell Array is normally used for custom circuits which require option development time and costs, the M10900 family is a standard product ordered like any other MECL 10K circuit.

Device	Description	Comments
MC10900Z	8-Bit ALU with Parity Slice	17.8 ns Max Addition of 2 8-Bit Words. Introduced
MC10901Z	8 x 8-Bit Array Multiplier	Expandable to 32 x 32. 24.3 ns Max Delay for 8 x 8 Multiply. Introduced
MC10902Z	8-Bit Binary/BCD ALU Slice	Expandable to 32-Bits. 17.9 ns Max Add Delay. Introduced
MC10904Z	8-Bit Micro Code Sequencer Slice	Expandable to 24-Bits. 14.0 ns Max Clock to Output.
MC10905Z	Error Detect and Correct Circuit	16-Bit Check and Correct with 1 Chip. Expandable to 64-Bits. 16-Bit Check and Correct in 19.7 ns Max.

NEC
NEC Electronics

μPB6300 SERIES HIGH SPEED ECL GATE ARRAYS

Description

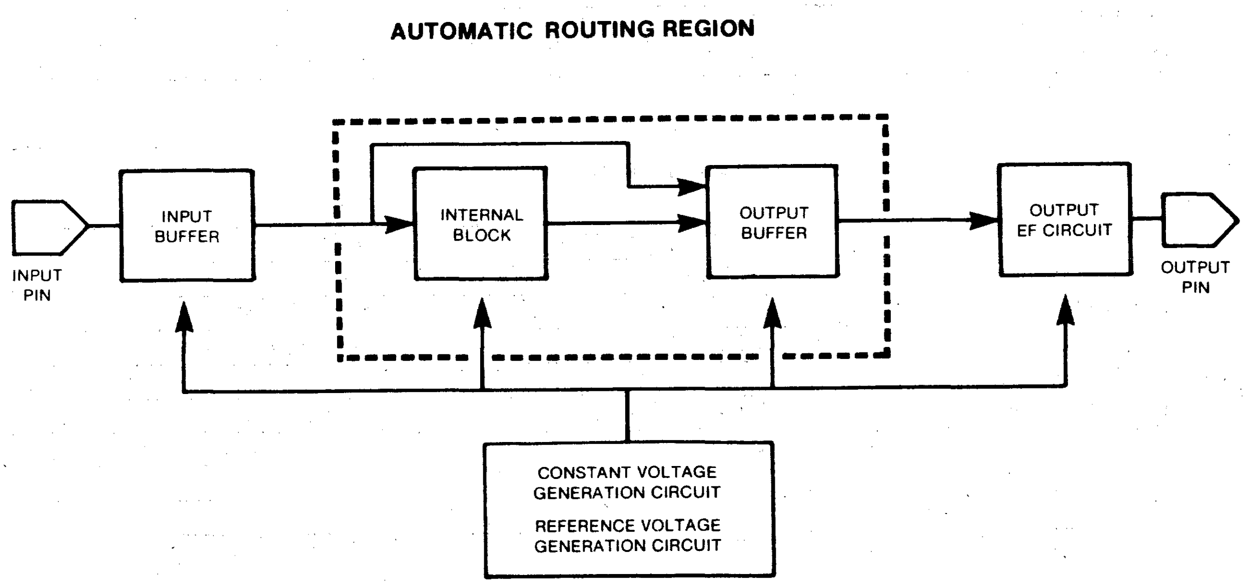
The μPB6300 series consists of three high speed ECL gate arrays manufactured using advanced bipolar technology. The μPB6301, μPB6310, and μPB6320 have 300, 1200, and 2000 equivalent gates, respectively. Specific LSI designs are built by interconnecting cells (2.5 gates) by means of advanced CAD tools such as logic simulation, automatic placement and routing, delay simulation, and test program generation. Customers can use the GE MARK III® time sharing system through their own terminals for logic simulation.

Customers can choose from a wide range of package types. The μPB6300 gate arrays are available in 72 = to 132 = pin grid arrays (PGA) packages and a 68-pin leadless dip carrier (LCC) package.

Features

- ☐ High speed: ☒ 0.5ns/gate (fan-in (=) fan-out (=) 2.5, L = 2.0mm)
- ☐ ECL 100K compatible
- ☐ Shallow junction dielectric isolation
- ☐ 68 available macros in function block library
- ☐ Fully supported by advanced CAD with direct customer access
- ☐ Quick Turn Around Time ☒ available 8~10 weeks after logic validation

CONSTITUTION



BLOCK	CONSTITUTION	FUNCTION	BLOCK HEADING
Input, Output Pin		ECL -100 K level interface	—
Input Buffer	EF output, CML internal	Level shift ECL - 100 K to CML	M
Internal Block	EF Output, CML internal	Shown in block library	C, J, V
Output Buffer	ECL -100 K Basic Circuit (W/O output EF)	level shift CML to ECL - 100 K (With simple logic function)	G
Output Special Circuit	only EF for Output	For ECL -100 k level output	B
Constant Voltage Generation Reference Voltage Generation	Constant voltage Generation Circuit with Temperature compensation	1) C.S. constant current control 2) Generation of reference voltage	—

NEC Electronics

CUSTOM/SEMICUSTOM

μPB6301 SPECIFICATION

ITEM		SPECIFICATION		COMMENT
Part Number		μPB6301		
Integration (Gate)		~ 300		1 cell = 2.25 gate
Input Output Interface		ECL - 100 K		output: 50 Ω to -2 V
Power Supply Voltage		V_{EE} = -4.5 V ± 10%		max = -5.7 V
Ambient Temperature		Ta = Q ~ +70°C		4 m/sec air cooling
t_{pd}/P_o	Internal Gate	0.5 nS/5.4 mW		F/I = F/O = 2.5, L = 2 mm
	Input Buffer	0.5 nS/5.4 mW		
	Output Buffer	0.8 nS/22.5 mW		
Power Dissipation		3.1 W (typ)		Ta, V_{EE} = Typical
		4.6 W (max)		Ta, V_{EE} = Worst
Package		72 PIP	68 LCC	Θ = 5.6°C/W,
Pin Count (Max.)	Input	56	56	0 = 10°C/W, 1m/sec.
	Output	28	28	Input + Output ≤ 56
	Power Supply	8	8	
Cell Count	Internal cell	16 × 8 = 128		
	Peripheral	14 × 2 = 28		
Assembly Method		Wire bonding		
Number of Macros		68		
Circuit Form		EF Output, CML Internal		with wired logic

μPB6310 SPECIFICATION

ITEM		SPECIFICATION			COMMENT
Part Number		μPB6310			
Integration (Gate)		~ 1200			1 cell = 2.25 gate
Input Output		ECL - 100 K			outputs: 50 Ω to -2 V
Power Supply Voltage		V_{EE} = -4.5 V ± 10%			max = -5.7 V
Ambient Temperature		Ta = O ~ +70°C			4 m/sec air cooling
t_{pd}/P_o	Internal	0.7 nS/1.9 mW			F/I = F/o = 2.5, L = 3 mm
	Input Buffer	0.6 nS/1.9 mW			
	Output Buffer	1.0 nS/22.5 mW			
Power Dissipation		3.7 W (typ)			Ta, V_{EE} = Typical
		5.6 W (max)			Ta, V_{EE} = Worst
Package		72 PIP	132 PIP	68 LCC	Θ = 5.6°C/W,
Pin Count (Max.)	Input	64	88	60	Input + Output ≤
	Output	32	48	32	Package Pin - Power Pin
	Power Supply	8	16	8	
Cell Count	Internal	32 × 16 = 512			
	Peripheral	24 × 2 = 48			
Assembly Method		Wire bonding			
Number of Macros		50			
Circuit Form		EF Output, CML Internal			with wired logic

μPB6320 SPECIFICATION

ITEM		SPECIFICATION	COMMENT
Part Number		μPB6320	
Integration (Gate)		~ 2000	1 cell = 2.25 gate
Input Output Interface		ECL - 100 K	output: 50 Ω to -2.0 V
Power Supply Voltage		V_{EE} = -4.5 V ± 10%	max = -5.7 V
Ambient Temperature		Ta = O ~ +70°C	4 m/sec air cooling
t_{pd}/P_o	Internal Gate	0.7 nS/1.9 mW	
	Input Buffer	0.6 nS/1.9 mW	
	Output Buffer	1.0 nS/22.5 mW	
Power Dissipation		6.1 W (typ)	Ta, V_{EE} = Typical
		9.5 W (max)	Ta, V_{EE} = Worst
Package		72 PIP 132 PIP 68 LCC	Θ = 5.6°C/W,
Pin Count (Max.)	Input	56 108 56	Used Input + Used Output ≤ Max Input
	Output	28 48 28	
	Power Supply	16 24 16	
Cell Count	Internal cell	32 × 26 = 832	
	Peripheral	24 × 2 = 48	
Assembly Method		Wire bonding	
Number of Macros		50	
Circuit Form		EF Output, CML Internal	with wired logic

μPB6301, μPB6310, μPB6320

Function Block Library List

INPUT BUFFER

Block Name	Function	6301 Typical Power (mW)	6301 Cell Count	6310/6320 Typical Power (mW)	6310/6320 Cell Count
M201	1-IN-AND	11.5	1	3.7	1
M210	1-IN-NAND	11.5	1	3.7	1
M211	1-IN-AND (low power)	8.6	1	1.9	1
M212	1-IN-NAND (low power)	8.6	1	1.9	1

INTERNAL BLOCK

Block Name	Function	6301 Typical Power (mW)	6301 Cell Count	6310/6320 Typical Power (mW)	6310/6320 Cell Count
JWI	2-IN-WIRED-AND	-5.9	0	-1.8	0
JWI3	3-IN-WIRED-AND	-13.2	0	-2.7	0
JWI4	4-IN-WIRED-AND	-17.7	0	-5.6	0
V001	CLAMP-VOLTAGE-GENERATOR	35.8	1	9.8	1
C027	1-IN 2-OUTPUT AND/NAND	29.2	1	9.1	1
C028	2-IN 2-OUTPUT AND/NAND	29.2	1	9.1	1
C029	3-IN 2-OUTPUT AND/NAND	29.2	1	9.1	1
C030	4-IN 2-OUTPUT AND/NAND	29.2	1	9.1	1
C031	5-IN 2-OUTPUT AND/NAND	29.2	1	9.1	1
C004	DUAL 1-IN-AND/NAND	34.6	1	11.0	1
C005 E102	DUAL 2-IN-AND/NAND	34.6	1	11.0	1
C032	1-IN 3-OUTPUT AND 1-OUTPUT NAND BUFFER	29.2	1	9.1	1
C033	1-IN 1-OUTPUT AND 3-OUTPUT NAND BUFFER	29.2	1	9.1	1
C034	2-IN 3-OUTPUT AND 1-OUTPUT NAND BUFFER	29.2	1	9.1	1
C035	2-IN 1-OUTPUT AND 3-OUTPUT NAND BUFFER	29.2	1	9.1	1
C036	3-IN 3-OUTPUT AND 1-OUTPUT NAND BUFFER	29.2	1	9.1	1
C037	3-IN 1-OUTPUT AND 3-OUTPUT NAND BUFFER	29.2	1	9.1	1
C038	1-IN-AND-SIN-BUFFER	16.7	3	—	—
C039	1-IN-NAND-DELAY-BUFFER	28.1	4	—	—
C040	DUAL-1-IN-DELAY-BUFFER	16.7	1	—	—
C041	2-WIDE 2 · 2-IN-AND-OR	34.6	1	—	—
C042	3-WIDE 3 · 2 · 2-IN-AND-OR	63.7	3	—	—
C043	4-WIDE 3 · 3 · 3 · 3-IN-AND-OR	81.0	3	—	—
C044	2-WIDE 3 · 3-IN-AND-OR	46.4	2	—	—
C045	2-WIDE 1 · 1-IN-AND-OR	34.6	1	11.0	1
C046	2-WIDE 1 · 1-IN-AND-OR	34.6	1	11.0	1
C047	2-WIDE 1 · 2-IN-AND-OR	34.6	1	11.0	1
C048	3-WIDE 1 · 2 · 3-IN-AND-OR	45.9	2	14.7	2
C049	4-WIDE 1 · 2 · 3 · 4-IN-AND-OR	57.2	3	18.4	3
C050	5-WIDE 1 · 2 · 3 · 4 · 4-IN-AND-OR	68.6	3	—	—
C051	2-WIDE 2 · 2-IN-AND-OR	28.6	1	9.2	1
C052	2-WIDE 2 · 2-IN-AND-OR	46.4	2	14.6	2
C053	2-WIDE 3 · 3-IN-AND-OR	46.4	2	24.2	2
C054	2-WIDE 4 · 4-IN-AND-OR	46.4	2	24.2	2
C055	3-WIDE 2 · 2 · 2-IN-AND-OR	63.7	3	33.3	3
C056	3-WIDE 3 · 3 · 3-IN-AND-OR	45.9	2	24.2	2
C057	4-WIDE 2 · 2 · 2 · 2-IN-AND-OR	51.3	2	27.1	2
C058	4-WIDE 2 · 2 · 2 · 2-IN-AND-OR	39.4	2	13.0	2
C059	1 · 1-IN-EOR	34.6	1	11.0	1
C060	1 · 1-IN-ENOR	34.6	1	11.0	1
C061	2 · 1-IN-AND-EOR	22.7	1	—	—
C062	2 · 1-IN-AND-EOR	22.7	1	—	—
C063	2 · 1-IN-AND-EOR	34.6	2	11.0	1

C064	1 · 1 · 1-IN-EOR	79.9	3	25.7	3
C065	1 · 1 · 1-IN-ENOR	79.9	3	25.7	3
C066	2 · 1-IN-AND-EOR	34.6	2	11.0	1
C067	1 · 2 · 2 · 2 · 2-IN-EXOR	—	—	13.1	3
C116	1 · 2 · 2-IN-AND-DFF	105.0	5	27.8	5
C117	2 · 3 · 3 · 2-IN-AND-DFF	110.4	5	—	—
C118	1 · 2 · 2-IN-AND-DFF	96.7	4	—	—
C119	2 · 3 · 3 · 2-IN-AND-DFF	107.5	5	—	—
C137 E131	MASTER-SLAVE-DFF	34.6	3	11.0	3

OUTPUT BUFFER

Block Name	Function	6301 Typical Power (mW)	6301 Cell Count	6310/6320 Typical Power (mW)	6310/6320 Cell Count
G017	1-IN-AND	31.5	1	31.5	1
GA00	1-IN-NAND	31.5	1	31.5	1
GA01	2-IN-AND	36.0	1	36.0	1
GA02	2-IN-NAND	36.0	1	36.0	1
GA03	3-IN-AND	40.5	1	—	—
GA04	3-IN-NAND	40.5	1	—	—
GA05	4-IN-AND	45.0	1	—	—
GA06	4-IN-NAND	45.0	1	—	—
GA07	1-IN-AND/NAND	31.5	2	31.5	2
GA08	2-IN-AND/NAND	36.0	2	36.0	2
G006	3-IN-AND/NAND	40.5	2	—	—

OUTPUT E.F. CIRCUIT

Block Name	Function	6301 Typical Power (mW)	6301 Cell Count	6310/6320 Typical Power (mW)	6310/6320 Cell Count
B230	OUTPUT LEVEL TRANSRATOR	18.2	—	18.2	—

NEC Electronics

CUSTOM/SEMICUSTOM

μPB6101/μPB6102/μPB6103 BIPOLAR GATE ARRAYS

Description

The μPB6101/6102/6103 are high-speed, low-power TTL compatible gate arrays using an advanced NEC bipolar technology. They consist of an uncommitted configurable logic array and TTL compatible input/output (I/O) buffers.

NEC's comprehensive CAD support system and master slice system significantly reduce the time and expense normally associated with semi-custom devices.

Normal turnaround time, after logic validation, is only 8~10 weeks. Advanced CAD tools, such as: logic simulation, automatic placement and routing, delay simulation, and test program generation are used to insure accurate error-free designs of all NEC gate arrays.

Features

- ☐ Choice of three (3) Array Sizes
- ☐ High Speed 2.5nS/gate
- ☐ Low Power 1.4 mW/gate
- ☐ Comprehensive CAD for Rapid, Error-Free Designs
- ☐ Remote CAD Access on the GE Mark III Time Share Network Using Customer Terminal for Logic Simulation
- ☐ Four Output Buffer Types Available (Totem Pole, Open Collector, Three-State, Bidirectional)
- ☐ Package Options Dual-in-Line packages, Flat-Packages, Pin-Grid Arrays
- ☐ 8~10 Week Delivery After Logic Simulation

Packaging

The package type (dual-in-line, flat package, or pin-gride array) is generally determined by the customer, while the number of pins is a function (sum) of the utilized I/O and power pins. The μPB610X Series can be packaged in a 16-pin DIP (μPB6101) (minimum) through 72-pin (μPB6103) (maximum) PGA

The Series consists of three (3) devices:

Part Number	Gates	Output Buffers	Input Buffers
μPB6101	256	32	38
μPB6102	598	52	64
μPB6103	918	69	69

Package Pin Counts

Part	Package Pins	
Number	Minimum	Maximum
μPB6101	**16**	**40**
μPB102	**20**	**72**
μPB6103	**20**	**72**

ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{CC}	+7.0	V
Input Voltage	V_I	−0.5 to +7.0	V
Output Voltage	V_O	−0.5 to +5.5	V

RECOMMENDED OPERATING CONDITION

ITEM	SYMBOL	CONDITION	UNIT
Power Supply	V_{CC}	5 ± 10 %	V
Operating Temperature	T_{OP}	0 to 85	°C
"H" Level Output Current	I_{OH}	100 MAX.	μA
"L" Level Output Current	I_{OL}	12 MAX.	mA

ELECTRICAL CHARACTERISTICS

D.C. CHARACTERISTICS (T_a=25 °C)

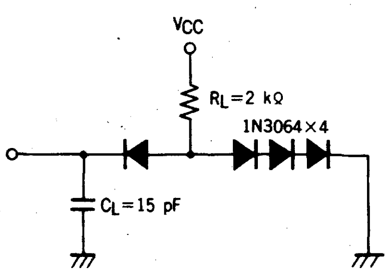
ITEM	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Low Level Input Voltage	V_{IL}				0.8	V
High Level Input Voltage	V_{IH}		2.0			V
Input Clamp Voltage	V_{IC}	V_{CC}=4.5 V, I_{IL}=−18 mA	−1.5			V
Low Level Output Voltage	V_{OL}	V_{CC}=4.5 V, I_{OL}=12 mA		0.3	0.5	V
High Level Output Voltage	V_{OH}	V_{CC}=4.5 V, I_{OH}=1 mA Note 1	2.5	3.0		V
Short Circuit Output Current	I_{OS}	V_{CC}=5.5 V, V_O=0 V	−100		−25	mA
Low Level Input Current	I_{IL}	V_{CC}=5.5 V, V_I= 0.4 V	−200			μA
High Level Input Current	I_{IH}	V_{CC}=5.5 V, V_I=2.7 V			20	μA
High Level Output Current	I_{OH}	V_{CC}=5 V, V_O=5.5 V			100	μA
Off State Output Current	I_{OZ}	V_{CC}=4.5 V, V_O=0.4 V/2.4 V (3 State Output)	−20		20	μA
Off State Output Current	I_{OZ}	(Bidirectional)	−200		40	μA

Note 1: Does not apply to Open-Collector Outputs

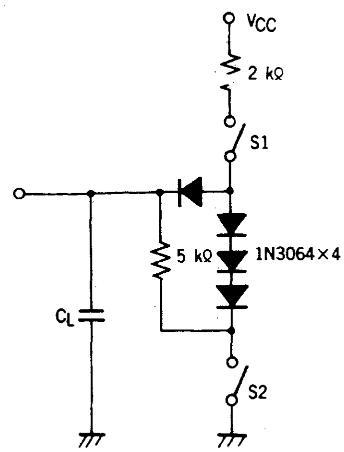
A.C. CHARACTERISTICS (T_a= 25 °C)

ITEM	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Delay Time/Gate	t_{PHL}	F/O=1 l=2 mm	1.0	1.8	2.7	ns
	t_{PLH}		1.4	2.5	3.7	ns
Delay Time/Input Buffer	t_{PHL}	F/O=1 l=2 mm	1.0	1.8	2.7	ns
	t_{PLH}		1.3	2.3	3.5	ns
Delay Time/Output Buffer	t_{PHL}	C_L=15 pF	2.8	4.7	7.1	ns
	t_{PLH}	C_L=15 pF	3.2	5.4	8.1	ns

OUTPUT LOAD CONDITION



i) for ordinary output



ii) for Three state output

EXAMPLE OF POWER DISSIPATION

ITEM	SYMBOL	POWER DISSIPATION	UNIT
Internal Gate	F010	1.4	mW
Input Buffer	M001	1.9	mW
Output Buffer (Totem-Pole)	B001	2.4	mW
Output Buffer (Open Collector)	B002	2.4	mW
Output Buffer (Three State)	B003	2.5	mW
Output Buffer (Bidirectional)	B004	4.4	mW
Output Buffer (Bidirectional D.C.)	B007	4.4	mW

NEC Electronics

CUSTOM/SEMICUSTOM

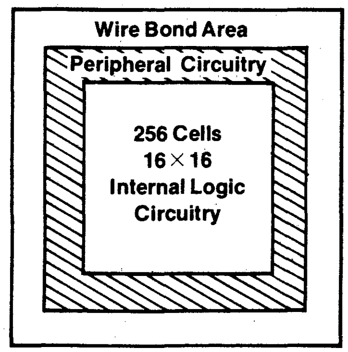
Chip Architecture

The arrays are divided into three basic areas. The I/O buffers are placed uniformly on the periphery of each device so that there are an equal number on each die edge. At each signal pad location, the pin function can be one of several possible I/O function configurations.

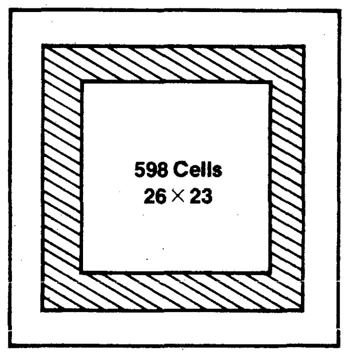
The area between the cells and the bonding pads contains all of the peripheral circuitry which convert from I/O levels to the internal logic, and a voltage generating for the internal power supply.

The center of the die contains rows of continuous gates separated by horizontal routing channels. The density of the array is a factor of the total cell count (row × line). Each cell is made up of two transistors and four resistors.

μPB6101



μPB6102



μPB6103

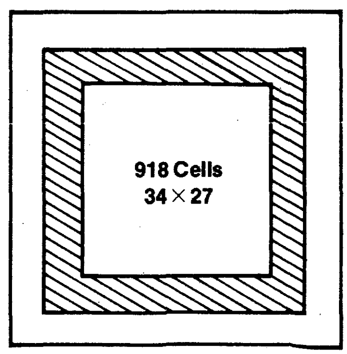


Fig. 1 Function block library list

BLOCK NAME	FUNCTION	CELL NO.	P_D (mW)
F004	INVERTER	1	1.4
F000	2-INPUT NAND	1	1.4
F010	3-INPUT NAND	1	1.4
C020	6-INPUT NAND	2	1.4
C030	9-INPUT NAND	3	1.4
F011	3-INPUT AND	2	2.3
C021	6-INPUT AND	2	2.3
C51A	2-WIDE 3-INPUT AND OR INVERTER	2	2.8
C054	4-WIDE 3-INPUT AND OR INVERTER	4	5.6
F086	EXCLUSIVE OR	6	8.4
F074	D-F/F	6	8.4
C109	J-K F/F	7	9.8
C075	D-LATCH	4	5.6
CC10	3-STATE CONTROL	1	1.4
M001	INPUT BUFFER	–	1.9
B001	OUTPUT BUFFER (TOTEM-POLE)	–	2.4
B002	OUTPUT BUFFER (OPEN COLLECTOR)	–	2.4
B003	OUTPUT BUFFER (3-STATE)	–	2.5
B004	OUTPUT BUFFER (BIDIRECTIONAL)	–	4.4
B007	OUTPUT BUFFER (BIDIRECTIONA) (OPEN COLLECTOR)	–	4.4
V000	0 LEVEL GENERATOR	1	1.4
JWI	WIRED AND	–	–
C005	DELAY GATE	4	3.7
CS10	OUTPUT LEVEL SHIFT	1	2.5

DEVELOPMENT PROCEDURE

Chart 1 illustrates the development step of both customer and NEC. The following two types of interfaces are available for customers.

1) CAD interface (Interface A) ..... most common method.

In this method the customer will begin at the logic design stage and proceed through to the logic simulation stage. NEC will then carry on from automatic placement and routing through sample delivery to final shipment of product.

The major benefit of this method is that the customer can perform the logic simulation on their own premises by using the NEC CAD facilities through the GE MARK III time share system, thus reducing the time needed for design.

Document

(1) contact and non-disclosure agreement
(2) circuit drawing based on NEC's functional block
(3) interconnection data file (LOGINC)
(4) test data pattern file (LOGPAT)
(5) Pin-assignment (if required)
(6) Critical path assignment (if required)

2) Circuit drawing interface (interface B)

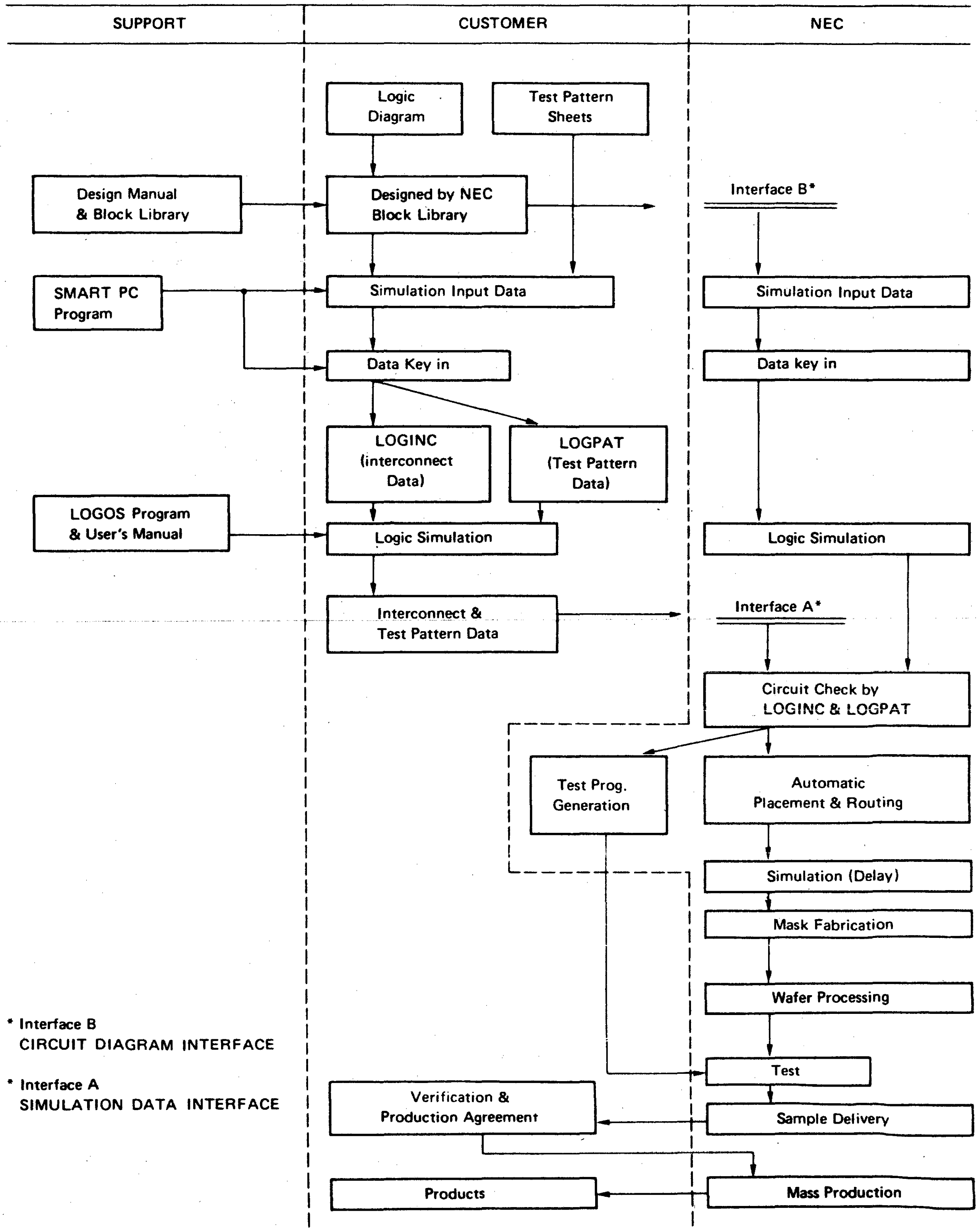
(1) logic drawing . . . . Here the customer will prepare the logic drawing according to the block library shown in Fig. 1 and the design manual.
(a typical example is shown in Fig. 2)

(2) test pattern sheet. . . . . The test pattern sheet also needs to be prepared
(a typical example is shown in Fig. 3)

The remaining stages from logic simulation to shipment are performed by NEC. Design rule check and logic simulation results are reported to the customers.

NEC will furnish evaluation samples within 10 weeks of logic validation.

Flow Chart of Development and Interface



* Interface B
CIRCUIT DIAGRAM INTERFACE

* Interface A
SIMULATION DATA INTERFACE

μPD65000 SERIES ADVANCE SILICON CMOS CMOS GATE ARRAYS

Description

The μPD 65000 Series is a family of low power, high-speed gate arrays manufactured using advanced Silicon gate CMOS technology. The series consists of from 427 to 11,250 gate devices that are available in a variety of package types.

The semi-custom approach of using Gate Arrays offers a unique and effective method of manufacturing I.C.'s with greatly reduced cost and development time. NEC makes this possible by stocking wafers which are completely fabricated except for the final step of interconnection of components to make up the required circuit configuration. This enables a designer the freedom of interconnecting the uncommitted components to achieve his unique circuit configuration.

The semi-custom approach is intended for customers seeking cost effective alternatives. By using Gate Arrays, customers can reduce component count and board size so that they can be more competitive in the markets which they serve. NEC's Gate Array program allows a customized I.C. to be developed with a short turn around time and at a small fraction of the cost of a full custom development program.

An advanced Computer-Aided Design (CAD) system is provided by NEC to achieve high quality, low cost and fast semi-custom I.C. development. Two kinds of interface are available for the customer. Interface "A" requires the customer to do the logic simulation either at one of the NEC's design centers or at his own facility through a terminal linked to G.E. Mark III time-sharing system. Interface "B" only requires the customer to provide the logic diagram and timing chart and NEC will do the rest.

So, contact us now and let NEC's Gate Array help you to succeed in your business.

Part Number	Number of Gates	Configuration	Input Buffers	Output Buffers
3-Micron Geometry				
μPD65002	858	66 × 13	50	50
μPD65003	427	61 × 7	38	36
μPD65010	1368	76 × 18	64	64
μPD65020	2112	96 × 22	80	80
2-Micron Geometry				
μPD65040	4104	152 × 27	120	116
μPD65060	6528	192 × 34	148	138
μPD65100	11,250	250 × 45	196	176

Notes:
1. A gate consists of 2 P-ch and 2 N-ch transistors.

Features

Features	3-micron	2-micron
☐ High Speed	3ns/gate	2ns/gate
☐ Low Power	30μW/gate	20μW/gate

- ☐ Comprehensive CAD for rapid, error-free designs
- ☐ Remote CAD access on the GE Mark III time share network using customer terminal for logic simulation.
- ☐ Four output buffer types available (normal, open drain, three state, bidirectional).
- ☐ Quick turnaround time (10~12 weeks)
- ☐ Fully supported by advanced CAD
- ☐ 20K gate automatic placement and routing capability
- ☐ Logic simulation
- ☐ Test program generation
- ☐ Delay simulation

ABSOLUTE MAXIMUM RATINGS

($T_A = 25°C$)

ITEM	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{DD}	-0.5 ~ 7	V
Input Voltage	V_I	-0.5 ~ V_{DD} + 0.5	V
Output Current	I_O	10	mA
Operating Temperature	T_{OPT}	-40 ~ +85	°C
Storage Temperature	T_{STG}	-65 ~ +150	°C

Chip Structure

The LSI chip consists of two areas; an internal cell area and a peripheral area.

Input/Output Buffer

All I/O buffers can be configured as input, schmit trigger input, normal output, open drain output, three state output or bidirectional.

All I/O buffers are fully CMOS/TTL compatible.

All assigned outputs are capable of driving 8 LS-TTL loads. Additional driving capability can be obtained by connecting output buffers in parallel.

Internal Cell

One cell has 2 p-channel transistors and 2 n-channel transistors, which are arranged in an array surrounded by routing channels

One cell can be used as 2 input NAND gate so the number of cells is equal to the number of gates.

Function Block

LSI logic function can be realized using the internal cell area. SSI/MSI logic functions are configured in units of circuit assemblage called "block" or "macro" which can be placed in any location of the internal cell area. NEC has over 140 kinds of macro's. This enables flexible LSI design and reduces design TAT.

Package Availability

Plastic and ceramic DIP packages range from 40 pins to 64 pins, flat packages from 64 pins to 100 pins, and Pin Gride Arrays (PGA) packages from 72 pins to 208 pins.

A customer can select a specific package type according to design and I/O pin requirement.

RECOMMENDED OPERATING CONDITION

(T_A = 25° C)

ITEM	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply Voltage	V_{DD}	CMOS Level	4.5	5	5.5	V
Input Voltage	V_I		0		V_{DD}	V
Low Level Input Voltage	V_{IL}	CMOS Level	0		0.3 V_{DD}	V
High Level Input Voltage	V_{IH}	CMOS Level	0.7 V_{DD}		V_{DD}	V
Low Level Input Voltage	V_{IL}	TTL Level*	0		0.8	V
High Level Input Voltage	V_{IH}	TTL Level*	2.0		V_{DD}	V
Input Rise, Fall Time	T_{RT}		0		10	μS

*T_A = 0 ~ 70° C, V_{DD} = 5 V ±5%

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5 V ± 10%. T_A = -40 ~ +85° C)

ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Static Current	I_L	$V_I = V_{DD}$ OR GND		0.1	200	μA
Dynamic Current	I_{DD}	1 mHz/cell		4		μ A
Input Current	I_L	$V_I = V_{DD}$ OR GND		10^{-5}	10	μA
Low Level Output Current	I_{OL}	V_{OL} = 0.4 V	3.2	6		mA
High Level Output Current	I_{OH}	V_{OH} = V_{DD} -0.4 V	1	2		mA
Low Level Output Voltage	V_{OL}	I_O = 0			0.1	V
High Level Output Voltage	V_{OH}	I_O = 0	V_{DD} -0.1			V

AC CHARACTERISTICS

(V_{DD} = 5 V ±10%. T_A = -40 ~85° C)

ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Max Operating Frequency	F_{MAX}		20	50		MHz
Delay Time*	T_{PD}	GATE		2		ns
	T_{PD}	I/0 Buffer		12**		ns
Output Rise Time	T_R	C_L = 15 pF		10		ns
Output Fall Time	T_F	C_L = 15 pF		7		ns

*With fan out of 3 and 3 mm wiring.
**With 15pF

NEC
NEC Electronics

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- ☐ Logic simulation
- ☐ Test program generation
- ☐ Delay simulation

ABSOLUTE MAXIMUM RATINGS

(T_A = 25° C)

ITEM	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{DD}	-0.5 ~ 7	V
Input Voltage	V_I	-0.5 ~ V_{DD} + 0.5	V
Output Current	I_O	10	mA
Operating Temperature	T_{OPT}	-40 ~ +85	°C
Storage Temperature	T_{STG}	-65 ~ +150	°C

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A customer can select a specific package type according to design and I/O pin requirement.

RECOMMENDED OPERATING CONDITION

(T_A = 25° C)

ITEM	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply Voltage	V_{DD}	CMOS Level	4.5	5	5.5	V
Input Voltage	V_I		0		V_{DD}	V
Low Level Input Voltage	V_{IL}	CMOS Level	0		0.3 V_{DD}	V
High Level Input Voltage	V_{IH}	CMOS Level	0.7 V_{DD}		V_{DD}	V
Low Level Input Voltage	V_{IL}	TTL Level*	0		0.8	V
High Level Input Voltage	V_{IH}	TTL Level*	2.0		V_{DD}	V
Input Rise, Fall Time	T_{RT}		0		10	μS

*T_A = 0 ~ 70°C, V_{DD} = 5 V ±5%

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5 V ± 10%. T_A = -40 ~ +85° C)

ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Static Current	I_L	$V_I = V_{DD}$ OR GND		0.1	200	μA
Dynamic Current	I_{DD}	1 mHz/cell		4		μ A
Input Current	I_L	$V_I = V_{DD}$ OR GND		10^{-5}	10	μA
Low Level Output Current	I_{OL}	V_{OL} = 0.4 V	3.2	6		mA
High Level Output Current	I_{OH}	V_{OH} = V_{DD} -0.4 V	1	2		mA
Low Level Output Voltage	V_{OL}	I_O = 0			0.1	V
High Level Output Voltage	V_{OH}	I_O = 0	V_{DD} -0.1			V

AC CHARACTERISTICS

(V_{DD} = 5 V ±10%. T_A = -40 ~85° C)

ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Max Operating Frequency	F_{MAX}		20	50		MHz
Delay Time*	T_{PD}	GATE		2		ns
	T_{PD}	I/0 Buffer		12**		ns
Output Rise Time	T_R	C_L = 15 pF		10		ns
Output Fall Time	T_F	C_L = 15 pF		7		ns

*With fan out of 3 and 3 mm wiring.
**With 15pF

Chart 1. Flowchart of Development and Interface

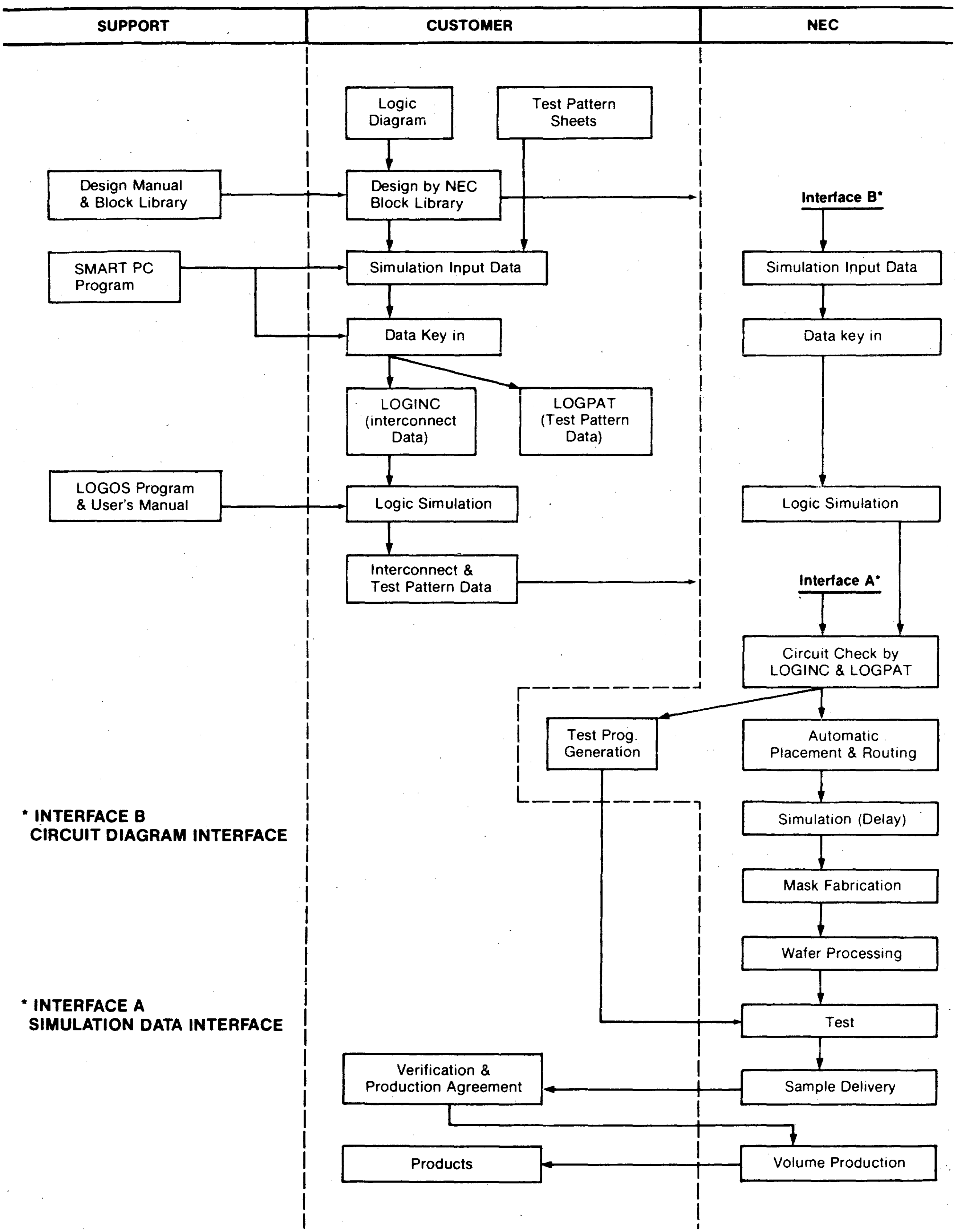


Figure 1. μD65002, μPD65010, μPD65020 Block List

INTERFACE BLOCK

Block Type	Function
FI01	Input Buffer (CMOS Level)
FI02	Input Buffer (TTL Level)
FO01	Output Buffer (Normal)
EXT1	Output Buffer (Nch Open Drain)
EXT2	Output Buffer (Pch Open Drain)
B003	I/0 Buffer (3 state CMOS Level)
B004	I/0 Buffer (3 state TTL Level)

FUNCTION BLOCK

	Block Type	Function	Cells
IN-VERTER	F101	1-Input (F.O. = 5)	1
	F102	1-Input (F.O. = 10)	1
	F103	1-Input (F.O. = 15)	2
	F104	1-Input (F.O. = 20)	2
BUFFER	F111	1-Input (F.O. = 5)	1
	F112	1-Input (F.O. = 10)	2
	F113	I-Input (F.O. = 15)	2
	F114	1-Input (F.O. = 20)	3
NOR	F202	2-Input NOR Gate	1
	F203	3-Input NOR Gate	2
	F204	4-Input NOR Gate	2
OR	F212	2-Input OR Gate	2
	F213	3-Input OR Gate	2
	F214	4-Input OR Gate	3
NAND	F302	2-Input NAND Gate	1
	F303	3-Input NAND Gate	2
	F304	4-Input NAND Gate	2
	F305	5-Input NAND Gate	3
	F306	6-Input NAND Gate	3
AND	F312	2-Input AND Gate	2
	F313	3-Input AND Gate	2
	F314	4-Input AND Gate	3
AND-NOR	F421	2 + 1 Input AND-NOR Gate	2
	F422	2 + 2 Input AND-NOR Gate	2
	F423	3 + 1 Input AND-NOR Gate	2
	F424	2 AND, 2-NOR	2
OR-NAND	F431	2 + 1 OR-NAND Gate	2
	F432	2 + 2 OR-NAND Gate	2

FUNCTION BLOCK

	Block Type	Function	Cells
	F433	3 + 1 OR-NAND Gate	2
	F434	2 OR, 2 NAND	2
DRIVER	F501	Clock Driver	1
	F502	Clock Driver (Dual)	2
	F503	Clock Driver (Parallel)	3
	F504	Clock Driver (Pala-Dual)	4
	F505	OSC Control	2
	F531*	3-State Buffer (EN)	3
	F532*	3-State Buffer (EN)	3
EX-OR	F511	2-Input Exclusive OR Gate	3
EX-NOR	F512	2-Input Exclusive NOR Gate	3
LATCH	F601	D-Latch	3
	F602	D-Latch with Reset	4
	F603	D-Latch with Reset	4
	F604*	D-Latch C	3
	F605*	D-Latch C with Reset	4
FLIP-FLOP	F611	D-Type	5
	F612	D-Type with Reset	7
	F613	D-Type with Set	7
	F614	D-Type with Set-Reset	7
	F615*	D-Type with Reset	7
	F616*	D-Type with Set	7
	F617*	D-Type with Set-Reset	7
	F631*	D-Type C	5
	F635*	D-Type C with Reset	7
	F636*	D-Type C with Set	7
	F637*	D-Type C with Set-Reset	7
	F641*	D-Type (Buffered Out)	6
	F642*	D-Type (Buffered Out) with Reset	6
	F643*	D-Type (Buffered Out) with Set	8
	F644*	D-Type (Buffered Out) with Set-Reset	8
	F645*	D-Type (Buffered Out) with Reset	8
	F646*	D-Type (Buffered Out) with Set	8
	F647*	D-Type (Buffered Out) with Set-Reset	8
	F661*	D-Type (Buffered Out) with C	8

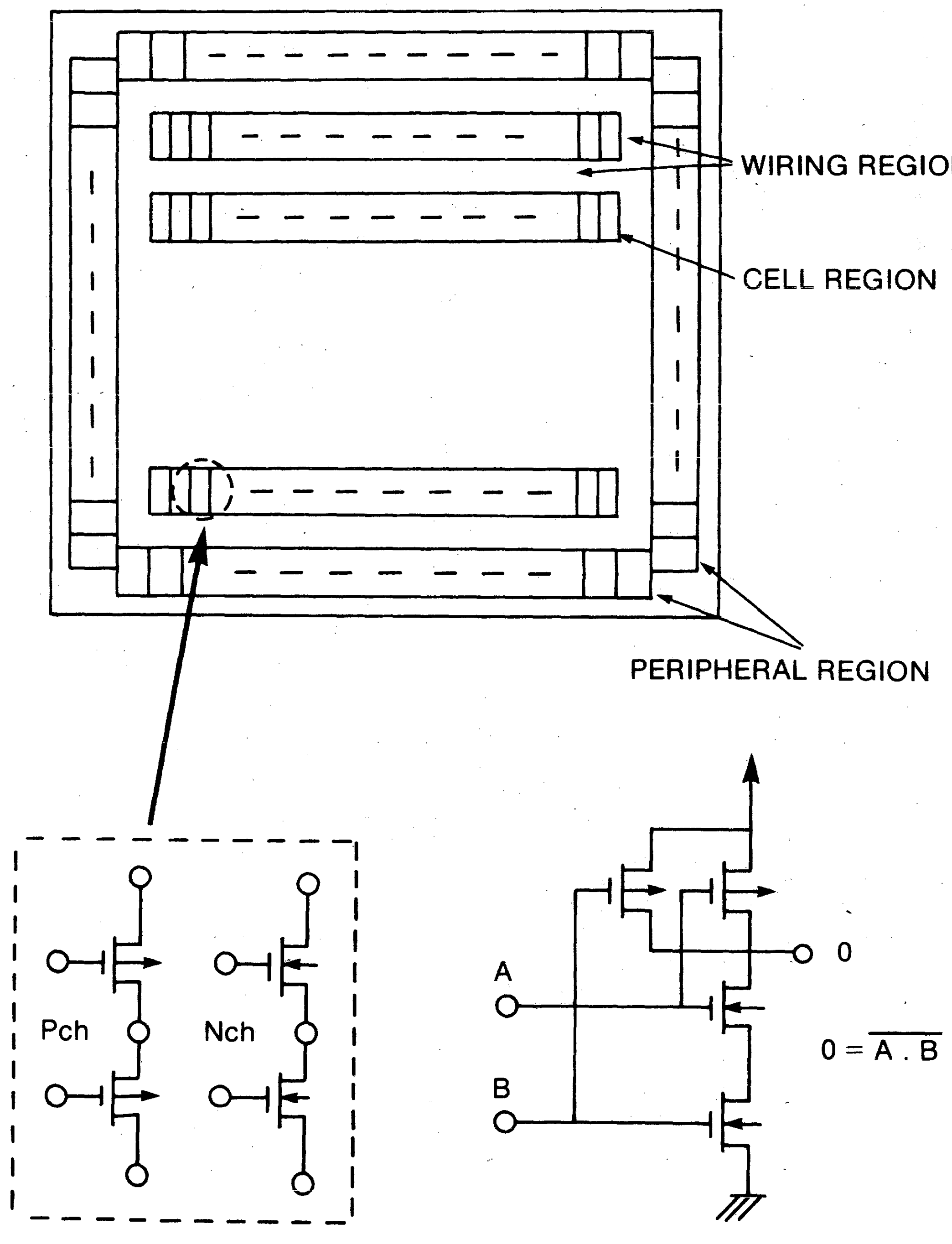
(*Under Designing)

FUNCTION BLOCK

	Block Type	Function	Cells
	F665*	D-Type (Buffered Out) with Reset	8
	F666*	D-Type (Buffered Out) with Set	8
	F667*	D-Type (Buffered Out) with Set-Reset	8
	F691	Serial/Parallel Shift Registre	5
	F712	Toggle with Reset	7
	F713	Toggle with Set	7
	F714	Toggle with Set-Reset	7
	F715*	Toggle with Reset	7
	F716*	Toggle with Set	7
	F717*	Toggle with Set-Reset	7
FLIP-FLOP	F735*	Toggle (T) with Reset	7
	F736*	Toggle (T) with Set	7
	F737*	Toggle (T) with Set-Reset	7
	F742*	Toggle (Buffered Out) with Reset	8
	F743*	Toggle (Buffered Out) with Set	8
	F744*	Toggle (Buffered Out) with Set-Reset	8
	F745*	Toggle (Buffered Out) with Reset	8
	F746*	Toggle (Buffered Out) with Set	8
	F747*	Toggle (Buffered Out) with Set-Reset	8
	F766*	Toggle (Buffered Out) (T) with Set	8
	F767*	Toggle (Buffered Out) (T) w/Set-Reset	8
	F771*	J-K F/F	9
	F772*	J-K F/F with Reset	11
	F773*	J-K F/F with Set	11
	F774*	J-K F/F with Set-Reset	11
	F775*	J-K F/F with Reset	11
	F776*	J-K F/F with Set	11
	F777*	J-K F/F with Set-Reset	11
	F781*	J-K F/F C	9
	F785*	J-K F/F C with Reset	11
	F786*	J-K F/F C with Set	11
	F787*	J-K F/F C with Set-Reset	11

(* Under Designing)

Chip Layout of CMOS Gate Array



CELL CONFIGURATION
(1 CELL)

EXAMPLE OF
GATE CONFIGURATION
(2-IN NAND GATE)

PLESSEY
Solid State

ADVANCE INFORMATION

SCD4000 600 Gate ECL Array

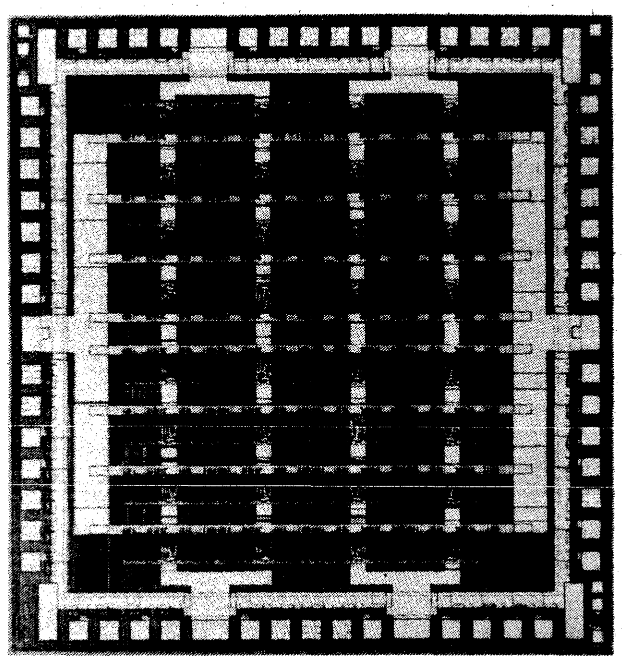
General Description

The Plessey SCD4000 is part of a family of semi-custom gate arrays using emitter coupled logic (ECL) circuits fabricated on a high performance bipolar process to give very fast switching speeds. ECL technology offers the fastest possible gate arrays. SCD4000 achieves basic gate delays of 400ps and D-type flip-flop clock rates of 400MHz typical. The array can be used as an economical replacement for several ECL 10K and 100K standard SSI and MSI parts even at low volumes. The design procedure consists of customising two metallisation layers which are then applied to pre-processed slices held in stock to manufacture quickly a new circuit or follow-on order from the customer.

Features

- Approx. 600 logic gate complexity.
- Compound (OR-AND-OR) gate delays typically 500ps.
- Basic gate delays typically 400ps.
- Series gated (or stacked) ECL logic uses reduced internal voltage swings (500mV).
- ECL 10K compatibility.
- Fully automated design procedure.
- Extensive library of standard cells.
- Two layer metallisation allows up to 100 per cent utilisation.
- 56 input/output pins, 10 power connection pins.
- Maximum power dissipation typically 3.5 watts (100 per cent utilisation).

Figure 1 **SCD4000 Chip Photograph**

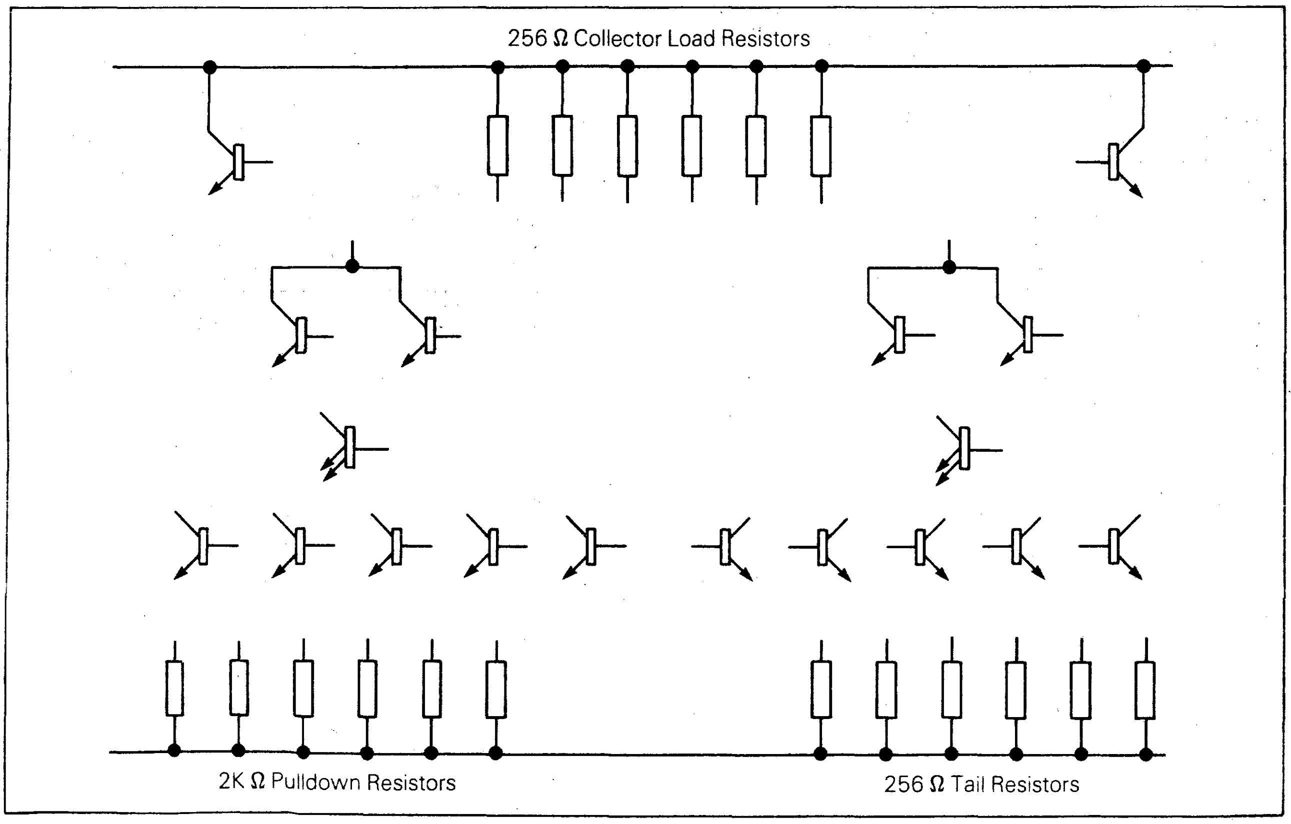


(chip size 170 × 170 mil)

Plessey Semiconductors

CUSTOM/SEMICUSTOM

Figure 2 **SCD4000 Cell Components**



Array Organisation

The array is configured into 8 × 8 cells each of which contains 20 transistors and 18 resistors as shown in figure 2. Each pair of cells shares a common voltage bias which provides all the reference levels required for internal ECL circuits and also for interfacing ECL 10K logic levels. Three of the reference levels are used for series gating. This enables complex functions to be implemented with a single cell.

The cell components have no predefined interconnect pattern. Consequently logic functions can be implemented using any required component configuration. Furthermore, additional logic is available by using the wired-AND and wired-OR functions. The result of using these powerful techniques is a 64 cell array which provides a conservative 600 logic gate complexity. (In fact, were the array to be implemented with high efficiency functions such as parity gates, a gate count of 960 would be achieved even before using the wired function).

The array has 64 edge pads of which 10 are reserved for power connections. The remaining 54 edge pads are freely available for either input or output functions as each pad site contains high current output transistors and input interface components.

Power Dissipation

Clearly power dissipation is dependent both upon the complexity and implementation of a given design. A completely full array will have a power dissipation of about 3.5 watts. The use of series gated logic greatly reduces the power necessary to perform a logical function as complex functions (e.g. 4 to 1 multiplexer) can be implemented on a single current source.

Cell Library Coding

The contents of the cell library are shown in Table 1. Each cell may contain more than one logic element and each element may have a number of options. For each cell there is a functional description showing logic levels, truth table and other circuit elements such as level shifters. A particular code is required to define the function of a specific element used within a cell. The format is as follows.

GE WW X Y Z

Where
- GE is the library cell.
- WW defines the cell.
- X selects gate or circuit element.
- Y defines variant option.
- Z input reference level.

SCD4000 Design Procedure

SCD4000 is supported by a fully automated software package including CLASSIC (an event driven logic simulator) and SCARP (an autoroute program) together with comprehensive electrical and rule violation checks. The flow diagram in figure 3 indicates the typical design procedure.

The design route outlined here will enable customers to successfully produce an ECL gate array in typically 10-16 weeks. The customer does not need to acquire specialised integrated circuit knowledge to be able to design devices. A number of customer/Plessey interfaces are possible during the course of a given design, ranging from simple logic specification at one extreme to magnetic tape (containing all the information necessary to drive the maskmaking pattern generator) at the other.

Figure 3 **Typical Design Flow Chart**

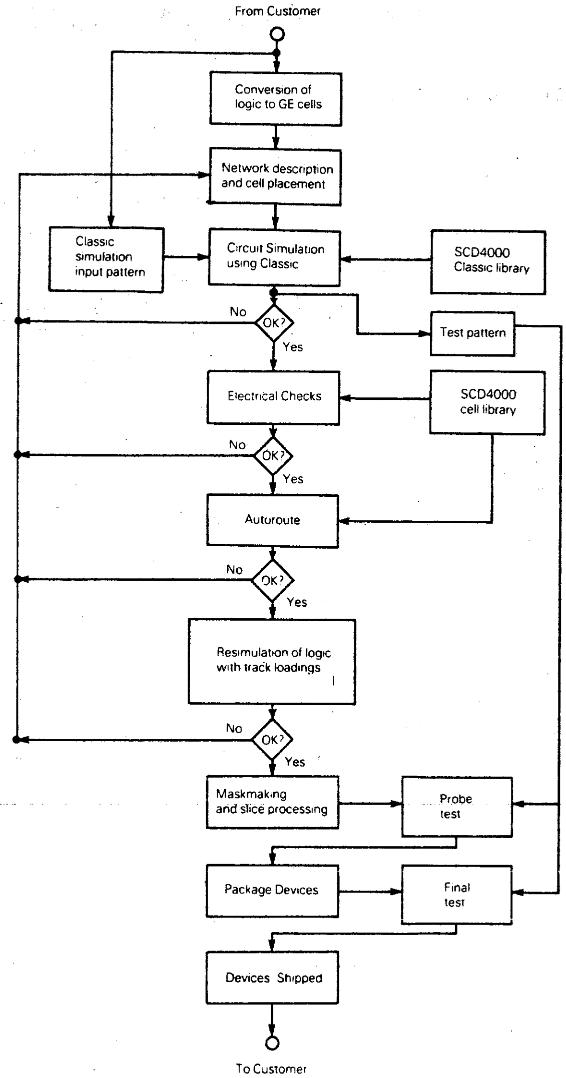


Table 1 GE Cell Library

Cell Name	Logic Function	Input/Output Buffer Compatible Input	Output
GEAA	3 input buffer gate + 2 input OR	Yes	Yes
GEAB	Triple 2 input OR/NOR	Yes	Yes
GEAC	Dual 5 input OR/NOR	Yes	Yes
GEAN	Hex 1 input buffer (true and inverse)	Yes	Yes
GEAP	Quad 1 input buffer (true and inverse)	Yes	Yes
GEAT	Triple 3 input OR/NOR	Yes	Yes
GEBC	Dual comparator	No	No
GECA	Dual 2 input OR/3 input OR-AND	Yes	No
GECB	Dual 2 input OR/2 input OR-AND	No	Yes
GECC	4 input OR/3 input/3 input OR-AND	Yes	No
GEDF	2 to 4 decoder with force high	Yes	No
GEEB	Dual Equivalence/Not Equivalence	No	Yes
GEFA	Full Adder	No	No
GEMA	4 to 1 multiplexer inverter	No	No
GEMB	Dual multiplexer (true and inverse)	No	Yes
GEMF	Dual multiplexer with force high or low	No	No
GEPA	4 input parity	No	No
GESA	Dual D-latch + inverter	No	No
GESB	Dual D-latch (true and inverse)	No	No
GETF	3 to 1 multiplexer with force high or low	No	No
GETV	2 to 1 multiplexer master-slave latch	No	No

For further information please contact: *The I.C. Marketing Manager*

ADVANCE INFORMATION
Design release fourth quarter, 1983
Production release second quarter, 1984

2.5 MICRON CMOS GATE ARRAYS

This range of CMOS Gate Arrays adds an increased maximum size and speed capability to Plesseys exisiting Five and Four micron geometry products. They use the same well proven proprietary Plessey CAD system ensuring trouble free designs.

	CLA5100	CLA5200	CLA5300	CLA5400	CLA5500	CLA5600	CLA5700	CLA5800	CLA5900
Technology	Silicon Gate	Silicon Gate	Silicon Gate	Silicon Gate	Silicon Gate	Silicon Gate	Silicon Gate	Silicon Gate	Silicon Gate
Process Geometry (μm)	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5
User-defined metal interconnection levels	2	2	2	2	2	2	2	2	2
Bonding Pads									
Uncommitted	36	48	64	80	96	112	128	144	160
Power	4	8	8	8	16	16	16	16	16
-Total	40	56	72	88	112	128	144	160	176
No. of equivalent 2 input NAND gates	640	1232	2016	3060	4404	5984	7104	8856	10,440
Typical gate utilization %	87	87	87	87	87	87	87	87	87
Gate delay (typ) (nS) Inverter F.0.1	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9
3 I/P NAND F.0.3	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8	2.8
System clock (MHz)	25	25	25	25	25	25	25	25	25
Toggle Freq.	50	50	50	50	50	50	50	50	50
Power consumption per gate (average)	1μW/MHz	1μW/MHz	1μW/MHz	1μW/MHz	1μW/MHz	1μW/MHz	1μW/MHz	1μW/MHz	1μW/MH
Power supply range (V)	3 to 7	3 to 7	3 to 7	3 to 7	3 to 7	3 to 7	3 to 7	3 to 7	3 to 7
Ambient operating Temperature (°C)	-55 to +125	-55 to +125	-55 to +125	-55 to +125	-55 to +125	-55 to +125	-55 to +125	-55 to +125	-55 to +125
I/O Compatibility A=CMOS B=TTL, C=LSTTL	ABC	ABC	ABC	ABC	ABC	ABC	ABC	ABC	ABC
Die size (mils)	111x111	138x138	166x166	194x194	235x235	269x268	291x291	319x324	346x346
Automatic Placement	YES	YES	YES	YES	YES	YES	YES	YES	YES
Automatic Routing	YES	YES	YES	YES	YES	YES	YES	YES	YES
Masks needed for customization	3	3	3	3	3	3	3	3	3

AVAILABILITY

Plessey is now accepting designs for prototyping with full production capacity available second quarter 1984.

PLESSEY
Solid State
A Division of Plessey Trading Corporation
3 Whatney, Irvine, California 92714
Telephone (714) 951-5212 TWX 910-595-1930
Telex: 701464 ANSBCK PLESSEY

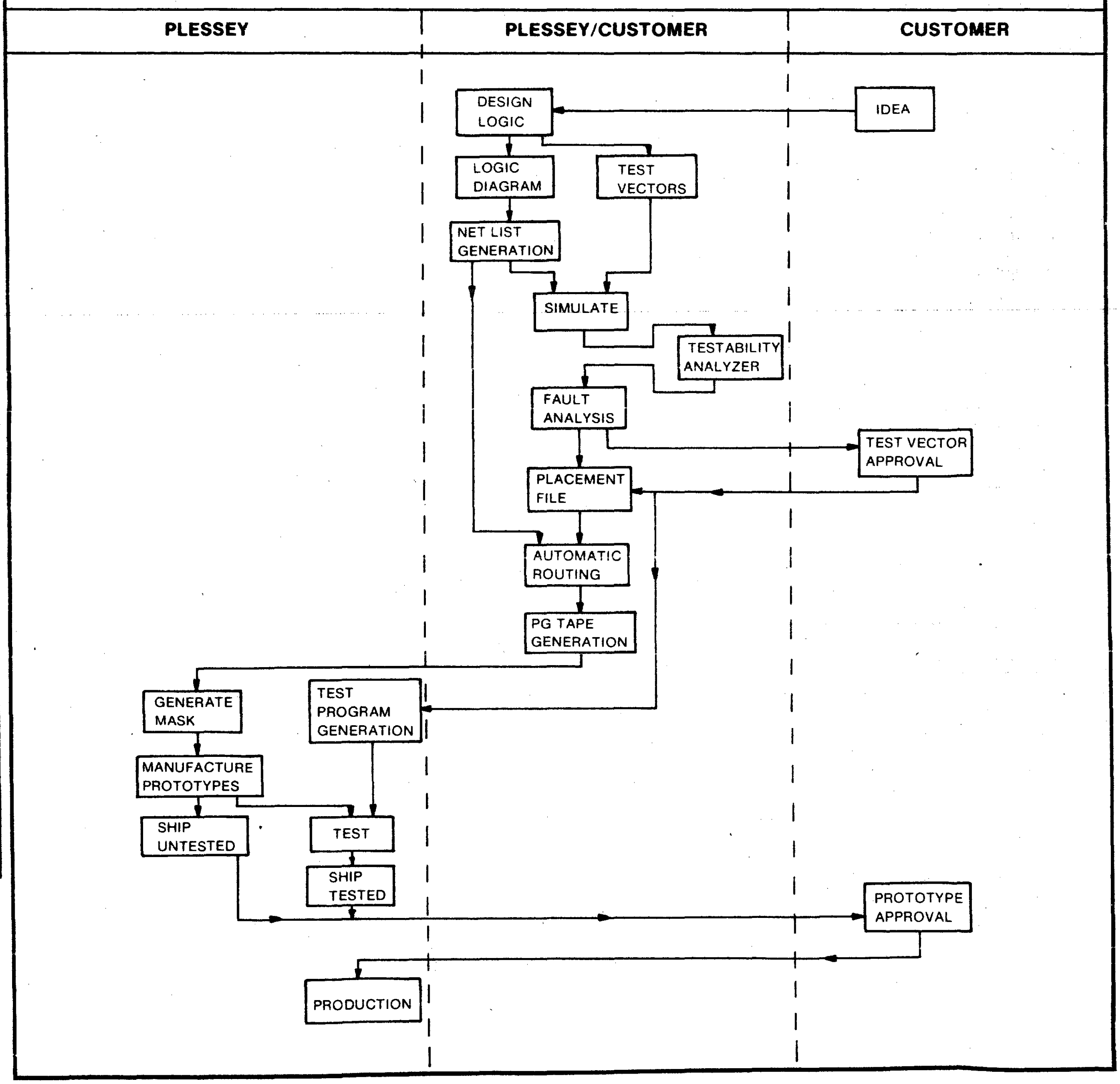
Semi-Custom Design

Plessey offers high density cell-based and *Gate Array Semi-Custom* devices fabricated on the best Bipolar, CMOS and NMOS technologies currently available. A full custom design and custom processing facility is also available.

The selection of the best approach for a particular problem depends upon a number of factors such as circuit size, development time and cost, and unit production cost amongst others.

Plessey will be pleased to assist in the selection of an optimal solution on receipt of complete information.

PLESSEY SEMICONDUCTORS
CMOS GATE ARRAYS
DESIGN RESPONSIBILITIES



CMOS LSI Gate Arrays

This series of *CMOS Gate Arrays* offer a quick and convenient method of producing low cost and high density customized integrated circuits.

This family of devices features very low power consumption using the latest silicon gate CMOS technology.

Two customizing layers of metallization give maximum design flexibility, speed and efficient use of chip area.

A sophisticated CAD system facilitates design and makes fully functional parts first time a certainty.

	CLA1000	CLA1200	CLA1500	CLA2100	CLA2300	CLA2500	CLA3700
TECHNOLOGY	SILICON GATE	SILICON GATE	SILICON GATE	SILICON GATE	SILICON GATE	SILICON GATE	SILICON GATE
PROCESS GEOMETRY (μm)	5	5	5	5	5	5	4
User-defined Metal Interconnection Levels	1①	1①	1①	2	2	2	2
Bonding Pads - Uncommitted - Power - Total	38 2 40	50 2 52	62 2 64	40 4 44	52 4 56	64 4 68	80 4 84
No. of Equivalent 2-input NAND gates	560	960	1440	840	1440	2400	4200
Typical Gate Utilization	70	70	70	87	87	87	87
Gate Delays - Typical (ns) Maximum	6 9	6 9	6 9	4 6	4 6	4 6	3 5
Toggle Frequency (MHz)	20	20	20	30	30	30	50
Power Dissipation @ gate	12μW/MHz	12μW/MHz	12μW/MHz	10μW/MHz	10μW/MHz	10μW/MHz	8μW/MHz
Typical Array Power Dissipation (mW)	30.6	52.4	78.6	47.5	81.5	135.7	190.0
Power Supply Range (V)	3 to 7	3 to 7	3 to 7	3 to 7	3 to 7	3 to 7	3 to 7
Ambient Operating Temperature (°C)	-55 to 125	-55 to 125	-55 to 125	-55 to 125	-55 to 125	-55 to 125	-55 to 125
I/O Compatibility A=CMOS,B=TTL,C=LSTTL	A,B,C	A,B,C	A,B,C	A,B,C	A,B,C	A,B,C	A,B,C
Die Size (mils)	191 x 131	211 x 177	223 x 233	196 x 132	243 x 156	243 x 230	233 x 244
Density (gates/mm2	60	60	60	100	100	100	120
Automatic Placement	NO	NO	NO	YES②	YES②	YES②	YES②
Automatic Routing	NO	NO	NO	YES	YES	YES	YES
Masks Needed for Customization	1	1	1	3	3	3	3

① Plessey performs layout

② Auto-placement to be implemented 3Q83

PLESSEY
Solid State
A Division of Plessey Trading Corporation
3 Whatney, Irvine, California 92714
Telephone (714) 951-5212 TWX 910-595-1930
Telex: 701464 ANSBCK PLESSEY

ADVANCE INFORMATION
Design Release fourth 1/4 83
Production Release 2nd 1/4 84

Plessey Semiconductors

CUSTOM/SEMICUSTOM

CMOS MICROCELL MV2000 Series
2.5 MICRON DOUBLE LAYER METAL

Introduction

Microcell is a powerful blend of more conventional standard cell, distributed gates, and generated logic approaches to LSI circuit design. It uses Plessey's well established CMOS process and versatile double layer metal interconnect. Very high circuit speeds are possible with the 2 1/2 micron geometry used.

This approach allows circuit costs to approach those of full custom ICs without the time and cost penalties normally associated wtih full custom.

Design Process

The design process is arranged to allow the fullest possible checking to ensure first time success. The Microcell approach itself reduces the amount of checking to be done as all standard cells are proven and, hence, only the interconnections require checking in the simulation. Design is done using the same comprehensive and versatile CAD system developed over many years for Plessey's existing range of microcell and gate array products.

Specification 25°C

Gate delay (typ) (output falling) 2 input NAND FO 1 2 input NAND FO 3	 0.8nS 1.2nS
Maximum system clock	25MHz
Maximum toggle frequency	50MHz
Power consumption/gate (average)	1 W/MHz
Power supply	3 to 7v (5V preferred)
Operating temperature	-55 to +125°C
I/O Compatibility	CMOS, TTL, LSTTL
Store Temperature	-65 to +150°C

Packaging

Standard packages are as follows:

24, 28, 40, 48 pin DII 68, 84 pin LCC, 68, 84, 108, 132 PGA

Supply of devices in other packages is subject to negotiation. Below 24 pins standard DIL packages are standard.

Cell Library

CTINV1	Small Inverter
CTINV4	Large Inverter
CTNAND2	Two Input Nand Gate
TNAND3	Three input Nand Gate
CTNAND4	Four Input Nand Gate
CTNOR2	Two Input Nor Gate
CTNOR3	Three Input Nor Gate
CTNOR4	Four Input Nor Gate
CTAOI	And Or Inverter Cell
CTOAI	Or And Inverter Cell
CT2ANOR	Two Input And Nor Gate
CT2ONAND	Two Input Or Nand Gate
CT4ANOR	Four Input And Nor Gate
CT4ONAND	Four Input Or Nand Gate
CT42ANOR	Four and Two Input And Nor Cells
CT42ONAN	4 + 2 Input Or Nand Gate
CTEXOR	Two Input Exclusive Or
CTEXNOR	Two Input Exclusive Nor
CTHADD	Half Adder
CTFADD	Full Adder
CTCK1	Small Clock Generator
CTCK2	Medium Clock Generator
CTCK3	Large Clock Generator
CTDL	Latch
CTDLRS	Latch with Set and Reset
CTMSD	Master-slave D-type
CTMSDRS	Master-slave D-type with Set and Reset
CTSR	Shift Register Cell
CTSRRS	Shift Register Cell with Set and Reset
CTTRA	Line Driver
CT2TRA	Two into One Multiplexer
CTPAD	Pad cell used for supply connection etc.
CTIP	Input Pad
CTIPBN	Normal TTL Input Buffer
CTIPBL	Large TTL Input Buffer
CTPRO	I/P Protection Cell
CTRH+	High Value pull up +V
CTRH−	High Value pull down -V
CTRL+	Low Value pull up +V
CTRL−	Low Value pull down -V
CTSCHMIT	Schmitt Trigger
CTOPD	Output Pad
CTOPL	Large Output Driver
CTOPQ	Quad Output Driver
CTOPTRD	Output Pad with separate P and N devices
CTOPTRL	Large Tristate Driver
CTOPTRQ	Quad Tristate Output Driver
CTTRID	Tristate Driver
CTFILL1	Filler cell for spacing Inverter and similar height cells
CTFILL2	Filler cell for spacing CTEXOR and similar height cells
CTFILL3	Filler cell for spacing CTFADD and similar height cells
CTCKF	Clock Filler Cell
CTCKDS	Clock Filler Cell
CTCKFIL1	Clock Filler Cell
CTCKFIL2	Clock Filler Cell
CTSRFIL	Filler Cell for CTSR and CTSRRS

Other cells including PLA, ROM, RAM and a Microprocessor will be introduced in due course.

Qualification

Parts are normally supplied to Plessey's stringent commercial release standards. Screening to MIL883B and equivalent standards is available on request at additional cost.

Eliminate Gate

With Raytheon's Full Service Approach to Advanced Bipolar ISL Configurable Gate Array Problem Solving.

Your reason for considering semicustom gate arrays is for the time and cost effective superior product solutions they provide. Raytheon achieves those goals for you, recognizing and avoiding the many potentially risk inducing pitfalls that could affect your objectives.

Employing service intensive customer applications support and proven automated design techniques, Raytheon strives for error-free gate array implementation the first time.

Experience

Raytheon was among the very first to design and manufacture gate arrays. Our long standing dedication to hard-to-do, high-performance, high-reliability design and production requirements carries over to all aspects of our gate array programs.

We began with a 60-gate device in 1974, followed by a 300-gate device in 1978 and a bipolar ISL 1620-gate density array in 1981. Over 70 circuit designs have been successfully developed, and are now in volume production. We now have five members of our ISL CGA family, ranging from 800 to 2400-gates.

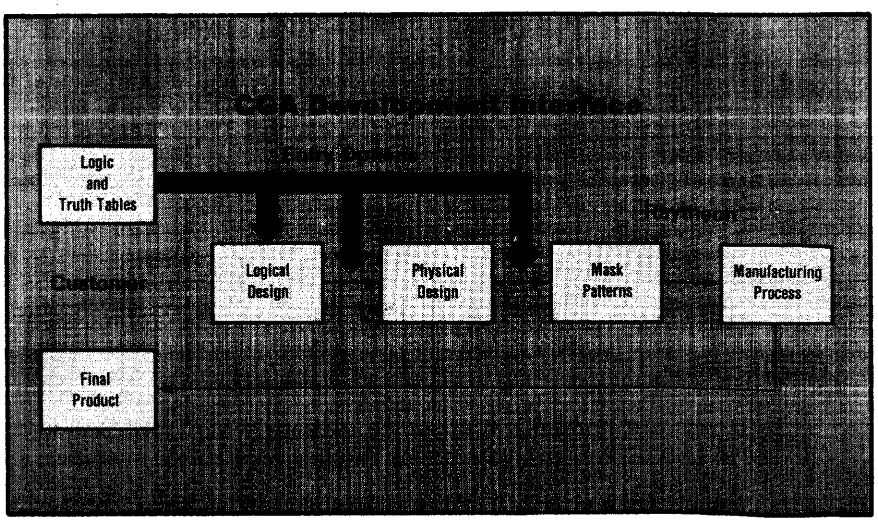
Personalized Development Support

Raytheon's cost effective approach to semicustom circuit implementation makes it fast and easy to develop your prototypes. Working parts can be in your system within 8 weeks.

Raytheon can start with your logic diagram and truth tables or divide the design tasks with you to optimize cost, minimize the turnaround time, and ensure design control.

Regardless of the design entry point that you choose, the Raytheon design engineering team will work closely with your designers to help assure optimum product performance, cost-effective partitioning, accurate logic translation, and required testability.

A comprehensive design source manual and an intensive 3-day tutorial are available to those customers who will be performaing the circuit design portions of development.



Array Anxiety

Design Automation

Raytheon's CAD facility offers a comprehensive assortment of analysis and design software, in a **common data base** environment, to quickly produce error-free prototype devices:

- Schematic Capture
- Logic Simulation
- Fault Grading
- Auto-Placement and Routing (Auto-Layout)
- Performance Verification

Performance Characteristics

Raytheon ISL CGAs are all designed for radiation tolerance and to operate over the -55° C to +125° C temperature range. Full MIL-STD-883, Class B or S processing, program management, and other custom or special requirments can be satisfied.

Bipolar ISL Technology

Raytheon's highly manufacturable 3 micron bipolar ISL process produces high density, superior performance, and efficient power consumption on all configurable gate arrays.

Interdensity compatibility exists between all arrays. Topological uniformity permits universal macrofunction and I/O designs.

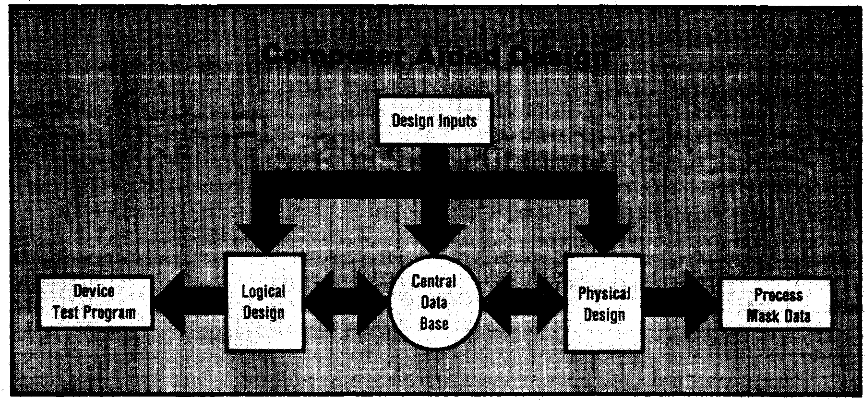
All Raytheon CGA's are fully TTL compatible. You can choose the desired function from a list of 35 I/O configurations and situate it at any signal pad location.

Package Options

Everything will be done to put your array in the package you need. Choose from ceramic DIPs, leadless chip carriers, flatpaks, pin grid arrays, or name the custom package you require.

Dedicated Service

Raytheon's high level of applications support begins before an order is received. Call us today. Let's examine your needs, and explore a thoroughly analyzed and properly executed configurable gate array development. Raytheon means service and dedication.



	Part Numbers				
	CGA8L48	CGA12L60	CGA16L68	CGA20L76	CGA24L84
Number of Array ISL Gates	836	1196	1620	1984	2376
Number of I/Os	48	60	68	76	84
Standard Speed (nS)	2.3	2.3	2.3	2.3	2.3
Enhanced Speed (nS)*	1.8	1.8	1.8	1.8	1.8
Power /Gate (μW)	350	350	350	350	350
Operating Power Supply (V_{CC}/V_{BB})	5/1.8	5/1.8	5/1.8	5/1.8	5/1.8

*A Raytheon proprietary feature that is available on all ISL gates.

The following MSI functions are a partial listing of those available in our **Macrofunction Library** for convenient implementation of customer circuit design.

Function	5400/7400 Series No.*
D-Type Flip-Flop with Clear and Preset	74
Two Input Exclusive-OR Gate	86
J-K Type Flip-Flop	109
3-to-8 Line Decoder	138
8-to-3 Line Priority Encoder	148
1-of-8 Data Selectors/Multiplexers with Strobed Outputs	151
4-to-1 Data Selector/Multiplexer	153
4-to-16 Line Decoder/Demultiplexer	154
Sychronous Decade Counter	162A
4-Bit Bidirectional Universal Shift Register	194
S-R Latch	279
9-Bit Odd/Even Parity Generator/Checker	280
4-Bit Binary Full Adder with Fast Carry	283
8-Bit Universal Shift/Storage Register	299
Octal Transparent Latches	373
Octal D-Type Edge-Triggered Flip-Flops	374
4-Bit ALU	381

*The ISL logic format functions are pin polarity and function equivalents of the corresponding 5400/7400 LS Series functions.

Raytheon reserves the right to change the circuitry and other data at any time without notice.

RAYTHEON

Raytheon Company, Semiconductor Division
350 Ellis Street, Mountain View, CA 94043
(415) 966-7716

Custom and Semicustom LSI

RCA Semicustom LSI Capabilities

Automated GAs

Features

- Easy to Design and Change
- Fast Turnaround • CMOS Performance
- Wafer Stockpiling • CAD Compatible
- Library of Logic Macros

As gate counts and design complexities increase, manual layout of GAs becomes costly and time consuming. Therefore, RCA has developed automated placement and routing techniques.

The Automated GA System requires only one unique metal mask level. Artwork for this level is generated automatically from RCA's extensive library of logic cells.

The metal mask describes the required logic functions on the array and then defines a unique interconnect pattern. Artwork for the mask is generated automatically from RCA's extensive library of logic macros (predefined logic structures or cells).

Automated GA software has proved to be very effective, providing 100% connectivity and gate utilization up to 98% for complex random logic applications.

PaCMOS (Programmable Automated Cell CMOS) Standard Cells

PaCMOS is an RCA computer-automated design approach to LSI. It is based on a group of circuit building blocks, called standard cells, that can be automatically chosen, placed, and interconnected by a computer program.

RCA has a large and expanding library of previously designed, verified, and life-tested standard cells — available in C^2L (closed-geometry silicon-gate CMOS-bulk), bulk CMOS (5μ and 3μ), and silicon-gate CMOS on sapphire substrate.

As a design aid in selecting appropriate cells, a standard cell notebook is available. In it, all of the logic cells are fully characterized and documented in the form of data sheets.

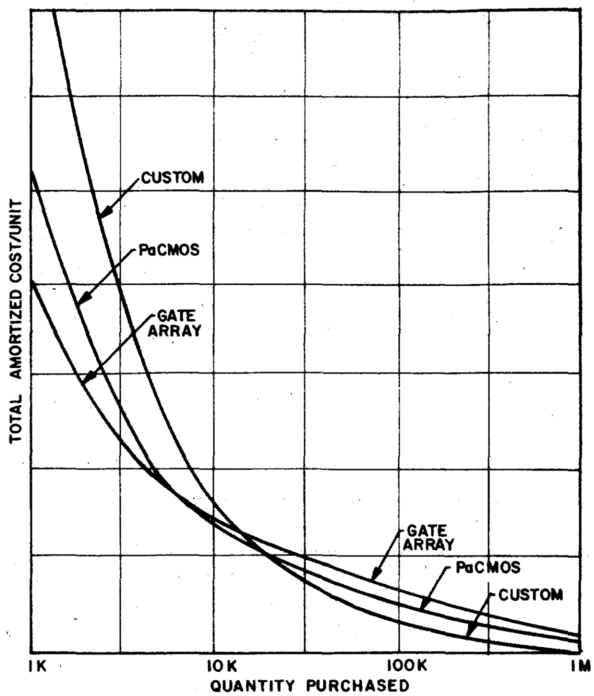
It provides the name and function of the cell, the circuit and logic configuration, the Boolean equation, the truth table, and the dynamic performance data.

By using the standard cell notebook, the designer can match his particular circuit configuration with the available standard cells and generate an input net list.

In addition to the standard cells, PaCMOS can also accommodate subchip options. Regular structures such as RAMs, ROMs, PLAs, PROMS, EPROMs, and register stacks, which have been remotely designed by conventional handcrafted techniques, can be automatically connected while the remainder of the host chip is computer generated.

PaCMOS VERSUS GA

A PaCMOS semicustom LSI offers attractive tradeoffs between development time, die size, and cost for many IC designs. Although its development time is slightly longer than a gate array, its die size is smaller. And in volume production PaCMOS can provide significant cost advances over GA designs.



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Design Automated Tools

MIMIC

A powerful software simulation program, called MIMIC, allows designers of GAs, as well as other RCA semicustom and custom LSI devices, to model the logical operation of digital circuits before device fabrication. Through the program, designers can discover logical flaws, race, hazard, or spike conditions, and timing and critical path uncertainties.

CRITIC (Computer Recognition of Illegal Technology in Integrated Circuits)

Another software tool available in the design of GAs, as well as other RCA semicustom and custom LSI devices, is the CRITIC program. CRITIC checks mask artwork by describing the mask as a series of polygons in terms of the vertices that define them. The program then automatically searches for and reports on minimum tolerance violations (width, spacing, and enclosure) and illegal topology relations (overlap, abut, cross, contain, and disjoint).

AFTER

The AFTER program (Automatic Functional Test Encoding Routine) aids the IC designer in generating functional test patterns required for the testing of digital IC's on Automatic Test Equipment (ATE). Input/output truth tables, representing these tests, can be created by the designer using the MIMIC logic simulation program by specifying the IC's inputs to MIMIC; its outputs are calculated by MIMIC. ATEs currently supported are the Fairchild Sentry/Sentinel/Series 20, the Teradyne J283, and the Datatron test systems.

CONCERT

(CONnectivity CERTification) is a layout analysis program which aids the verification of the logical and electrical correctness of the mask artwork produced by the APAR automatic layout programs. The layout generated by RCA's APAR programs (MP2D and GA) consists of standard cell placements and wire interconnects.

Custom and Semicustom LSI

Features

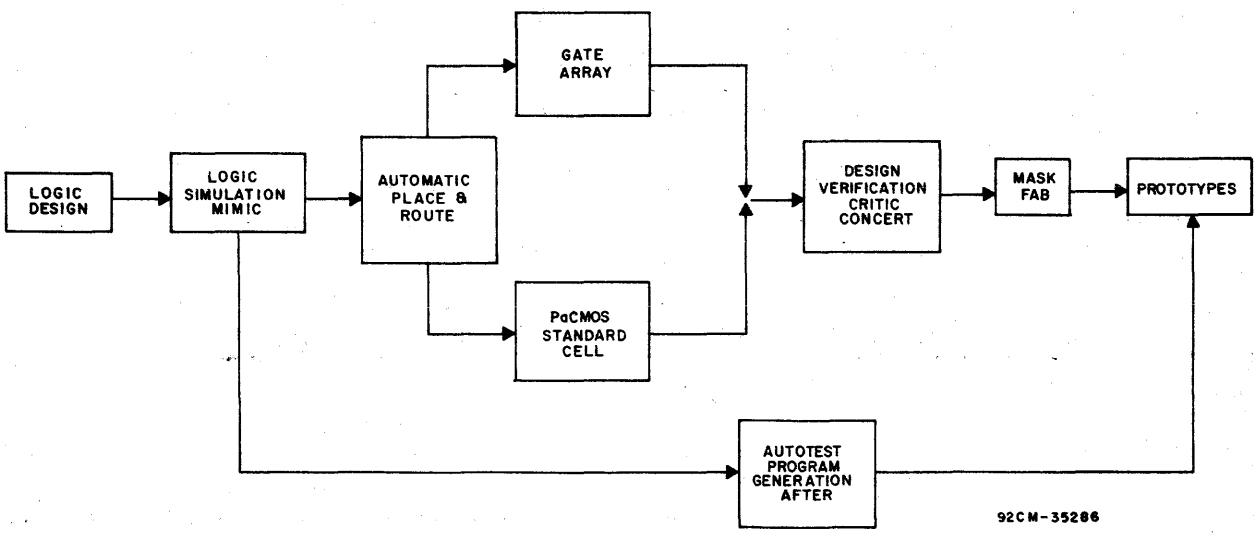
- Full Range of Cost-Effective Design Capabilities
  Gate Arrays — automatically placed and routed
  CMOS I (5μ) — CMOS II (3μ)
  PaCMOS — standard cells
  Full Custom LSI
- Fully Suported Design Automation
  MIMIC — logic simulation
  CRITIC — design rule vertification
  AFTER — test program generation
  CONCERT — connectivity check
- Long Experience
  More than 15 years of custom/semicustom service to demanding customers.

Comparison of Custom/Semicustom LSI Options*

	Semicustom		Full Custom
	Gate Array	PaCMOS Std. Cell	
Development Cost	0.2	0.3	1
Development Time	0.17	0.23	1
Risk (1st time success)	1	1.05	2
Final Die Size	1.5-2.0	1.1-1.4	1
Production Die Cost	3-4	1.5-2.0	1
Efficiency of Chip Utilization	0.8	1	1

*All comparisons normalized to a full custom basis assuming a 1000 gate complexity function.

RCA Design Automation System



RCA presently offers a variety of Gate Arrays classified according to:

Gate complexity: 250 to 6000 gates

RCA offers 17 Automated Universal Arrays (AUAs). The interconnect mask patterns for AUAs are generated solely by user-accessible software via the techniques of design automation (DA). AUAs are classified according to:

Process technology:
CMOS I — 5μ silicon gate
CMOS II — 3μ silicon gate
CMOS/SOS — 4μ silicon on sapphire
CMOS II — Double level metal — 3μ silicon gate

RCA presently offers a variety of PaCMOS cell libraries as follows:

Gate complexity: User defined

Process technology:
CMOS silicon gate (C^2L)
CMOS silicon on sapphire (CMOS/SOS)
CMOS I — 5μ bulk CMOS
CMOS II — 3μ bulk CMOS

RCA will soon offer additional APAR cell libraries. They are classified by:

Process technology:
CMOS/SOS — 2μ
CMOS II — Double level metal

All of the above will be offered in plastic, ceramic, side-brazed ceramic, and leadless and leaded chip carrier packages.

SP7000 SERIES CMOS GATE ARRAYS

FEATURES

- Utilizes SPI's Selective Oxidation, Silicon-Gate CMOS Process.
- High Speed 3.5nS Gate Delay
- Low Cost
- Operates Over 3 to 7 Volt Supply Range
- Prototypes 8-10 Weeks
- TTL/CMOS Compatible Inputs

SP7000 SERIES SPECIFICATIONS

Part Number	Number of Gates	Number of Pads	Number of Output Drivers	Die Size	Typical Output Current I_{OL}@$V_{OL}=0.4V$	Typical Output Current I_{OL}@$V_{OH}=4.2V$
SP7000	48	16	14	76 x 73	6mA	6mA
SP7001	80	20	16	86 x 93	10mA	8mA
SP7002	147	24	16	103 x 107	12mA	8mA
SP7003	300	40	22	118 x 104	6mA	1.5mA
SP7004	300	40	36	127 x 158	10mA	8mA
SP7005	544	56	32	132 x 150	6mA	1.5mA
SP7010	1000	76	40	185 x 185	6mA	1.5mA
SP7210	1200	84	72	186 x 251	6mA	4mA

Note: Some device specifications can be altered to meet customer requirements.

SPI's gate array in HCMOS will provide the key to reducing board space, lowering power requirements and improving cost effectiveness.

Whatever your gate array needs, SPI can tailor an interface program to match them. If you have a specific circuit you would like to implement in HCMOS, SPI will be glad to review your application and provide a detailed quotation on cost, delivery and technical parameters.

CHLA CMOS LOGIC ARRAY FAMILY

FEATURES

- Utilizes SPI's Selective Oxidation Silicon Gate
- CMOS Process
- Low static power dissipation — 1.0 μW
- High speed
- 3 to 6 volt power supply range
- Full TTL interface compatibility
- High noise immunity
- Low cost semi-custom

DESCRIPTION

The CHLA is a logic array with uncommitted logic cells driving output structures that may be configured as normal output buffers, 3-state buffers, or as D type edge triggered latches. To design with these devices the designer needs only to supply the necessary logic equations. Depending on the logic equations up to 64 product terms may be implemented. Since all logic gates are CMOS the static power supply current is independent of the number of product terms and is less than 2.0 μA.

Part Number	Description Inputs	Outputs	I/O
SP810H8	10	8	
SP812H6	12	6	
SP814H4	14	4	
SP818H2	16	2	
SP816C1	16	2	
SP810L8	10	8	
SP812L6	12	6	
SP814L4	14	4	
SP816L2	16	2	
SP816L8	10	8	6*
SP816R8	8	8	8**
SP816R6	8	6	8**
SP816R4	8	4	8**

* = 3-State
** = Latched 3-State

C-MOS HARD ARRAY LOGIC
SI-HAL SERIES 20 & 24

DESCRIPTION

The Si-HAL family provides a rapid economical way of customizing several SSI or MSI integrated circuits into one device. Si-HALs can be used to replace bipolar PALs and HALs or they can be developed from a unique logic schematic. Unlike bipolar HALs, C-MOS Si-HALs are not limited to fixed logic functions. You have a totally uncommited logic format to work with in developing your semi-custom circuit. You may choose from a wide range of logic functions including, but not limited to, AND, NOR, OR, NAND gates and various flip flops.

All of the Monolithic Memories HAL Series 20 & 24 can be pin for pin replaced with a Si-HAL Series 20 & 24.

The C-MOS Si-HAL family features an advanced silicon-gate process which gives all the advantages of C-MOS, and still is a direct replacement for many bipolar PALs and HALs.

Si-Fab ii is a unique process, which goes beyond the performance characteristics of conventional silicon-gate C-MOS. It has the same low power characteristics, but in addition demonstrates improved speed. On-chip gate delays are comparable to silicon-gate (1-3ns), but the data entry speeds are improved 50-75%. This speed enhancement is made possible through our unique Si-Fab II output drivers. Also, output drive is improved to handle up to 20 LSTTL loads.

HAL DEVELOPMENT

The following procedures can be followed in developing a Si-HAL semi-custom circuit.

1. Purchase a bipolar PAL and debug it to your circuit requirement.
2. Send Si-Fab two of your PAL circuits with either
   a. copy of circuit logic equations
   or
   b. a schematic drawing (checked for revisions and accuracy)

NOTE: If you are not interested in developing a circuit using a PAL first, a Si-HAL can be directly developed from your circuit schematic diagram.

Call Si-Fab with any questions you may have regarding Si-HALs or semi-custom circuit development

MAIN BENEFITS

- **Semi-custom solution to random logic**
- **Direct C-MOS replacement of bipolar HALs and PALs**
- **Easy, economical implementation from logic schematics**
- **Si-Fab II C-MOS provides low power, high speeds, high output drive**
- **Variety of packages available**

PART NO.	DESCRIPTION
Si-HAL 10H8	Octal 10input And-Or Gate Array
Si-HAL 12H6	Hex 12input And-Or Gate Array
Si-HAL 14H4	Quad 14input And-Or Gate Array
Si-HAL 16H2	Dual 16input And-Or Gate Array
Si-HAL 16C1	16input And-Or/And-Or-Invert Gate Array
Si-HAL 10L8	Octal 10input And-Or-Invert Gate Array
Si-HAL 12L6	Hex 12input And-Or-Invert Gate Array
Si-HAL 14L4	Quad 14input And-Or-Invert Gate Array
Si-HAL 16L2	Dual 16input And-Or-Invert Gate Array
Si-HAL 16L8	Octal 16input And-Or-Invert Gate Array
Si-HAL 16R8	Octal 16input Registered And-Or Gate Array
Si-HAL 16R6	Hex 16input Registered And-Or Gate Array
Si-HAL 16R4	Quad 16input Registered And-Or Gate Array
Si-HAL 16X4	Quad 16input Registered And-Or-Xor Gate Array
Si-HAL 16A4	Quad 16input Reg And-Carry-Or-Xor Gate

PACKAGING

Si-HALs can be shipped in chip or package form. A variety of packages are available. Request of quote for your package requirements.

Series 20 has 20 lead maximum.
Series 24 has 24 lead maximum.

PRICING

Prices will vary depending on circuit complexity, quantity, and package required. A one time development charge will be assessed on all orders, but this will be partially rebated on production orders according to quantity on all orders exceeding 1000 pieces.

Price List available on request.

Si-Fab
Si-Fab Corporation • 27 Janis Way • Scotts Valley, CA 95066 • (408)438-6800

ABBREVIATIONS OF COMPANY NAMES

Action Ins	Action Instruments
AD	Analog Devices
ADT	Advanced Digital Technology
Advent	Advent Products, Inc.
Alphatron	Alphatron
AMA	American Automation
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
Amperex	Amperex Electronic Corp.
Analogic	Analogic
Analog Sys	Analog Systems
APC	Applied Micro Circuits
Apex	Apex Microtechnology
APM	Applied Microsystems Corp.
Appl Sys	Applied Systems Corp.
APT	Applied Microtechnology
Aptek	Aptek Microsystems
Array Tech	Array Technology
AWI	AWI Electronics
Barvon	Barvon Research
Bedford	Bedford Computer Systems Inc.
Burr-Brown	Burr-Brown
CAE	Computer Aided Engineering
Cal Devices	California Devices
Cermetek	Cermetek
CGRS	CGRS Microtech Inc.
Cherry	Cherry Semiconductor
CIC	Custom Integrated Circuits
CirTech	Circuit Technology
Citel	Citel
Comlinear	Comlinear Corporation
CMA	Custom MOS Arrays
Comark	Comark Corp.
Comdial	Comdial Semiconductor
Comp Auto	Computer Automation
Compas	Compas Microsystems
Cont Logic	Control Logic Inc.
Control Sys	Control Systems Microsystems Div.
CreMicro	Creative Micro Systems
Cromemco	Cromemco, Inc.
Cubit	Cubit Inc.
Curtis	Curtis Electro Devices, Inc.
Cybernetic	Cybernetic Micro Systems
Cybersys	Cybersystems
Cybertek	Cybertek Inc.
Data General	Data General
Data I/O	Data I/O
Data Trans	Data Translation
Datel	Datel
Datricon	Datricon Corporation
DDC	Data Devices Corporation
DEC	Digital Equipment Corporation
Die-Tech	Die-Tech
Digelec	Digelec Corp.
Digitek	Digitek, Inc.
Dionics	Dionics Inc.
Dist Comp	Distributed Computer Systems
Divers Tech	Diversified Technology
E-HI	E-H International, Inc.
EDI	Electronic Designs Inc.
Elind	Elind Elettronica Industriale
EMM-SESCO	EEM-SESCO
Emulogic	Emulogic Inc.
ETI Micro	ETI Micro
Exar	Exar Integrated Systems
Exel	Exel Microelectronics
Fairchild	Fairchild
Ferranti	Ferranti Electric
Force	Force Computers
Fujitsu A	Fujitsu America
Fujitsu	Fujitsu Microelectronics, Inc.
GI	General Instrument
GTE Micro	GTE Microcircuits
Harris	Harris Semiconductor
Heurikon	Heurikon Corp.
Hilevel	Hilevel Technology, Inc.
Hitachi	Hitachi America, Ltd.
Holt	Holt Inc.
HP	Hewlett-Packard
Hughes	Hughes Aircraft, Solid State Products
Hybrid Sys	Hybrid Systems
HyComp	HyComp
ICC	International Cybernetics
IDT	Integrated Device Technology
IMI	International Microcircuits, Inc.
IMP	International Microelectronic Products
IMS	Industrial MicroSystems Inc.
Infosphere	Infosphere
Inmos	Inmos
IntCirEng	Integrated Circuit Engineering
IntCirSys	Integrated Circuit Systems
IntCompSys	Integrated Computer Systems
Int Tech	Integrated Technology Corp.
Intech	Intech Microcircuits Div.
Intel	Intel
Interdesign	Interdesign
Intersil	Intersil
Intronics	Intronics
ITT	ITT Semiconductors
Kinetic Sys	Kinetic Systems
Kontron	Kontron Electronics
Lambda	Lambda Semiconductor
Linear Tech	Linear Technology
LSI Comp	LSI Computer Systems
LSI Logic	LSI Logic Corporation
Master Logic	Master Logic Corporation
Matrix	Matrix Corp.
Matrox	Matrox Electronic Systems
Maxim	Maxim Integrated Products
MCC	Micro-Computer Control
MCE	MCE Electronics
Micrel	Micrel
Micro Innov	Micro Innovators
Micropac	Micropac Industries
Micro Net	Micro Networks
Micro Pwr	Micro Power Systems
Micro Sci	Micro Sciences Corp.
Micro Tech	Microcircuits Technology
Micro-Link	Micro-Link Corporation
Micron	Micron Technology
MilerTron	MilerTronics
Miller	Miller Technology
Mitel	Mitel Semiconductor
Mitsubishi	Mitsubishi Electronics
MMI	Monolithic Memories, Inc.
Mostek	Monolithic Systems Corp.
Motorola	Mostek
MRC	Motorola Semiconductor
Murray	MRC Systems
Monosil	Murray Consulting
National	National Semiconductor
NCM	NCM Corp.
NCR	NCR Corp., Microelectronics Division
NEC	NEC Electronics
Nitron	Nitron
OAE	Oliver Advanced Engineering
Octagon	Octagon Systems Corp.
OEI	Optical Electronics Inc.
Ohio Sci	Ohio Scientic
OKI	OKI Semiconductor
Omnibyte	Omnibyte Corp.
Onset	Onset Computer Corp.
Panasonic	Panasonic
Pico Design	Pico Design
Polycore	Polycore Electronics
Plessey	Plessey Semiconductors
PMI	Precision Monilithics, Inc.
PragDes	Pragmatic Design Inc.
Pro-Log	Pro-Log Corp.
Quay	Quay Corp.
Raytheon	Raytheon Semiconductor
RCA	RCA Solid State Division
RCI Data	RCI Data
RELMS	Relational Memory Systems
Reticon	Reticon
RIFA	RIFA
Rockwell	Rockwell, Microelectronic Devices
RTC	Riehl Time Corporation
Sanyo	Sanyo
SBE	SBE, Inc.
SEEQ	SEEQ Technology, Inc.
SPI	Semi Processes Inc.
Siemens	Siemens
Si-Fab	Si-Fab
Signetics	Signetics
SGS	SGS Semiconductor
Sharp	Sharp
Silicon G	Silicon General
Siliconix	Siliconix
Silicon Sys	Silicon Systems Inc.
Siltronics	Siltronics
SMC	Standard Microsystems Corp.
S MOS	S MOS Systems
Solarise	Solarise Enterprises
Solitron	Solitron Devices
Sprague	Sprague Electric Company
SSM	Solid State Micro Technology for Music
SSS	Solid State Scientific
Stag	Stag Microsystems
STC	Storage Technology Corp.
STD	STD Microsystems
Struc Des	Structured Design Inc.
Stynetic	Stynetic Systems
Sunrise	Sunrise Electronics
Sunshine	Sunshine Semiconductor
Supertex	Supertex Inc.
Symtek	Symtek Corp.
Synertek	Synertek
Sys Innov	Systems Innovations
Tau Zero	Tau Zero Inc.
Technitrol	Technitrol
Tektronix	Tektronix
Teledyne C	Teledyne Crystalonics
Teledyne P	Teledyne Philbrick
Teledyne S	Teledyne Semiconductor
Telefunken	Telefunken
Telmos	Telmos
Teltone	Teltone Corporation
TI	Texas Instruments
Third Domain	Third Domain
Thomson-CSF	Thomson-CSF Components Corp.
Toshiba	Toshiba America
Trans-Data	Trans-Data
TRW	TRW-LSI Products
Unitrode	Unitrode
Universal	Universal Semiconductor, Inc.
Varix	Varix Corp.
VLSI Design	VLSI Design Associates
VTI	VLSI Technology, Inc.
Votrax	Votrax
Weitek	Weitek Corporation
Western	Western Digital
Wintek	Wintek Corp.
Xicor	Xicor, Inc.
Xycom	Xycom
Zendex	Zendex Corp.
Zilog	Zilog
ZyMOS	ZyMOS Corporation
Zytrex	Zytrex Corp.

Signetics

BIPOLAR LSI
Gate Array/Semi-Custom Products

SEMI-CUSTOM SERVICE	8A1664
FLEXX™ ARRAY	8A1864
8A1200	8A2176
CG1001	CCL
8A1260	ACE0600/0900
8A1542	ACE 1320/1400/2200

SCC 0330-M, SCC 0450-M, SCC 0700-M, SCC 1100-M
SCC 0335-H, SCC 0455-H, SCC 0705-H, SCC 1105-H
SCC 1250-SH, SCC 2500-SH, SCC 5000-SH

signetics
a subsidiary of U.S. Philips Corporation
Signetics Corporation
811 E. Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088-3409
Telephone 408/739-7700

THE COMPLETE SEMICUSTOM SOLUTION

To meet your semicustom needs Signetics has developed a comprehensive semicustom service that offers one-stop shopping with state-of-the-art technology. This service gives you a choice of silicon systems ranging from CMOS to T²L and ECL, the widest range of semicustom products in the industry, with performance capable of meeting all your semicustom logic needs. All are supported with complete in-house capability for processing and fabrication, will full service CAD, which simplifies your design task and guarantees first-pass success for your semicustom program.

STATE-OF-THE-ART CAD

Signetics' CAD system encompasses the complete semicustom design process, from schematic input through auto place and route, design rule checking and test generation. This fully automated procedure speeds design and makes your job easy and guarantees that your semicustom chip is developed without error and on schedule. With Signetics' CAD you are using the most up-to-date semicustom design system available.

SCHEMATIC INPUT — FAST AND EASY

In designing a semicustom chip the first step is to enter your circuit into the computer. The most advanced method of circuit entry is Signetics schematic input system. This system only requires you to enter your schematic by use of a keyboard and mouse, which is fast and easy. The computer then automatically converts your schematic to a net list which is used for simulation and auto place and route.

For circuit entry Signetics gives you a choice of two schematic input systems, one with software originally developed by Future Net and one by Mentor. The Future Net system operates on a low cost IBM Personal Computer which you can use in your own shop or in a Signetics' sales office. The Mentor schematic input system operates on an Apollo computer which is available in one of Signetics' design centers. With either input system you will find the schematic entry step fast and easy.

COMPUTER SIMULATION — EASY AND SURE

Once your schematic has been entered, the next and final step is to simulate the logic using our TEGAS 5 Program. To do this you enter your test vectors then submit the job from your IBM PC to Signetics' computer via telephone link. If you are using one of our design centers the simulation can be performed on-site with the Apollo computer. Upon completion of simulation the computer returns to you the resulting output vectors to allow you to check your design. Computer simulation ensures that your circuit is functioning properly before Signetics manufactures your semicustom chip.

WHAT SIGNETICS DOES — MORE CAD

After completion of simulation your job is finished. Signetics takes over and completes the manufacture of your semicustom device, which involves the use of additional Signetics CAD. The effects of wire delay, if any, are compensated using our WIDGET program. Using your net list which was produced by the schematic input system, Signetics performs a comprehensive design rule check, then routes the chip automatically. Using your test vectors Signetics automatically produces a test tape for final testing using our SENGEN program. The routed chip is then masked and processed using our advanced semiconductor methodology.

In performing Signetics part of the task, a key step is auto place and route, and Signetics has placed a high emphasis on developing these programs. The MEDS program automatically routes at the gate level and is used for gate arrays and creation of macros. The CALMP program is used for more advanced structures, such as Signetics FLEXX™ Array. CALMP assembles macros and gates with automatically variable routing space for optimal packing of the chip. These and other similar programs allow Signetics to offer comprehensive use of auto-routing in all our semicustom products.

FULL IN-HOUSE CAPABILITY

As a full capability semiconductor supplier and in semicustom since 1975, Signetics has all the in-house support necessary for producing your semicustom chip. In addition to a full service CAD facility, Signetics has complete masking, wafer fabrication and processing, including military processing, for Source Control Drawing or MIL STD 883B parts production. This full capability ensures availability of parts and that your semicustom device will be processed according to your needs and on schedule.

A FULL CHOICE OF SILICON

With Signetics you can implement your semicustom requirement with silicon that is advanced in technology and architecture. In technology you have a choice of three levels of CMOS and five kinds of bipolar arrays with gate speed ranging from 8 nsec to 0.5 nsec and various output drive levels. In architecture these products are structured as gate arrays, masterslice, composite cell, and FLEXX™ arrays, with up to 5000 gates and 128 I/Os. These devices have been configured to encompass the complete range of semicustom applications to allow Signetics to meet your own specific needs.

CMOS GATE ARRAYS

Signetics CMOS gate arrays are oxide-isolated, silicon gate devices built on an epi substrate which virtually eliminates latch-up. Input/Output is compatible with CMOS or LSTTL logic. These are highly advanced CMOS gate arrays with a full selection of technology and architecture.

M-Series CMOS Gate Arrays Single layer metal, 330 to 1100 gates, up to 68 I/Os, with 8 nsec gate delay typical for a 2 output gate with 5V V_{DD}.

H-Series CMOS Gate Arrays Single layer metal, 330 to 1100 gates, up to 68 I/Os, with 4 nsec gate delay typical for a 2 output gate with 5V V_{DD}.

SH-Series CMOS Gate Arrays Dual layer metal, 1250 to 5000 gates, up to 128 I/Os, with 2 nsec gate delay typical for a 2 output gate with 5V V_{DD}.

BIPOLAR SEMICUSTOM DEVICES

Signetics bipolar semicustom devices are available with both junction isolation and oxide isolation, for T^2L and ECL applications. They are designed for high speed and high output drive.

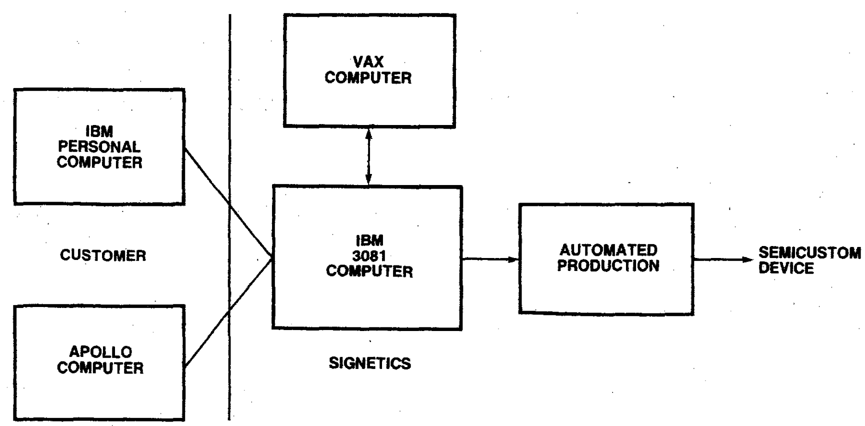
8AXXXX Series ISL Gate Arrays Dual layer metal junction isolated Integrated Schottky Logic for T^2L applications, 1200 to 2100 gates, up to 76 I/Os, with 4 nsec gate speed typical. Full military criteria.

Composite Cell Logic Three standard cell dual-layer metal libraries ranging from 3.5 nsec to 5 nsec typical gate delay. Up to 1000 actual gates, I/Os limited by package. Up to 80 mA output drive for T^2L applications. Full military criteria.

8HXXXX Series ISL Gate Arrays Dual layer metal, oxide isolated Integrated Schottky Logic for T^2L applications, 1600 to 3200 gates, up to 120 I/Os, with 1.5 nsec gate speed typical. Full military criteria.

FLEXX™ Array User-created or standard cells, dual-layer metal, variable routing space for optimal chip size, up to 2000 gates, I/Os limited by package. Oxide-isolated Integrated Schottky Logic for T^2L applications, 1.5 nsec gate delay typical. Full military criteria.

ACE Masterslice Array Oxide isolated CML for ECL 10 K, ECL 100 K and T^2L applications, 600 to 2200 gates, optional RAM on chip, up to 128 I/Os, 0.5 nsec gate delay, air cooled.



Signetics Computer Aided Design Facility used for design of semicustom devices. Provides remote access for schematic input and simulation. Signetics completes the design with design rule checking, automatic place and route, and automatic test tape generation before producing the semicustom device.

FEATURES

- 1.5 nsec typical gate delay
- Up to 2000 actual gates
- I/Os limited by package
- 250uW per gate
- Up to 48 mA output drive
- TTL Compatible
- Full CAD support
- Automatic schematic input
- Circuit simulation
- Automatic place and route
- Automatic macro generation
- Hard and soft macros
- Variable die size
- Plastic and ceramic chip carriers
- Standard DIPs

BENEFITS

- Fast, easy design
- Efficient use of silicon
- Proprietary LSI device
- High speed
- Replaces up to 100 SSI/MSI parts
- Reduces PCB area
- Saves manufacturing costs
- Reduces size, weight and power
- Improves system reliability

PRODUCT DESCRIPTION

The FLEXX™ array represents a major advance in semicustom technology which combines a new concept in architecture with the most advanced CAD available. With it you can create your proprietary semicustom LSI device quickly and easily, much like gate array or standard cell methodology, but with silicon utilization as efficient as standard LSI products designed by traditional handpacking methods. As a result of its superior design and silicon utilization efficiency the FLEXX™ Array is being used by Signetics to develop standard LSI products. The FLEXX™ Array is now available to Signetics customers as a semicustom development tool.

FLEXX™ Array Architecture

As shown in the figure, the FLEXX™ Array is composed of macros, which are rectangular assemblies of gates, with additional random gates included as required. The macros are variable in length and width for optimum routing efficiency, and the routing channel width is variable to accommodate only those traces required to route the chip. No unused gates are included. As a result of this architecture, the FLEXX™ Array is much more efficient in silicon utilization than a gate array or standard cell array, which means that the end device will have a smaller die and therefore a lower cost.

Multi-Level Software

To assembly the FLEXX™ Array Signetics uses multi-level automatic place and route software. The first level automatically generates the macros; it establishes the macro width and interconnects the gates within the macro. The second level places and interconnects the macros as well as individual gates; it varies the spacing between macros to accommodate the required interconnecting traces. This process is fully automatic and can be done quickly which speeds the development of your FLEXX™ Array.

Fully Automatic Design

To design a FLEXX™ Array the user enters the schematic and test vectors with a remote terminal then reviews the computer simulation of the circuit. In this procedure the user has the choice of using established ("hard") macros from Signetics computer library, modifying these macros or creating new ("soft") macros as required. Once the simulation is completed, Signetics takes over and routes the chip and procedures prototypes within ten weeks.

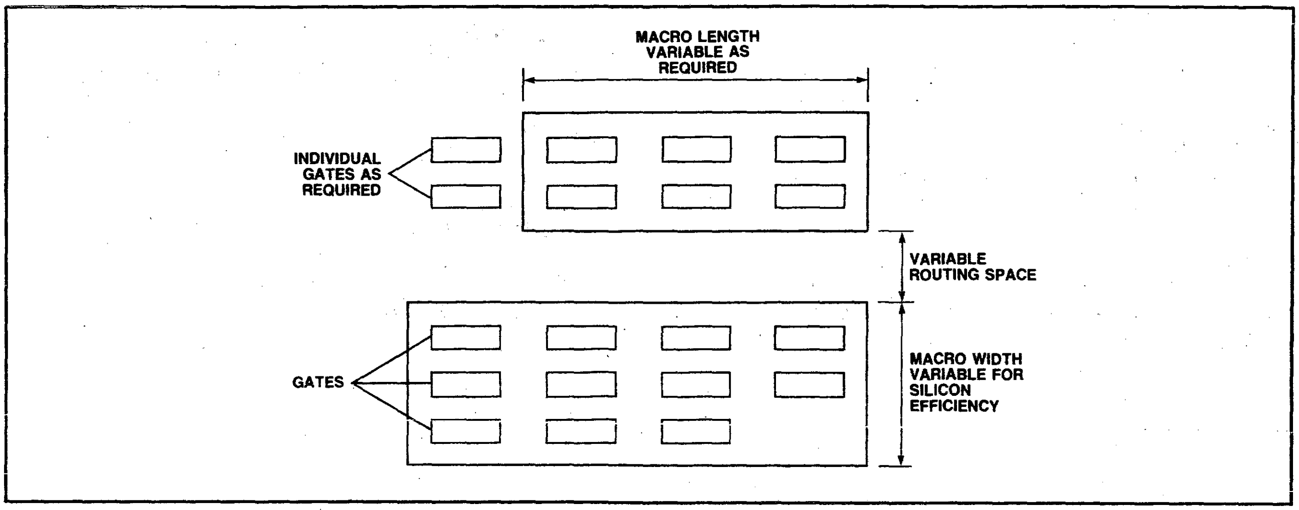
Silicon Technology — Performance

The FLEXX™ Array is a methodology for assembling a logic design on silicon; it is therefore largely independent of the particular silicon technology and can be used with CMOS and varieties of bipolar technology.

The first technology used to implement the FLEXX™ Array is oxide isolated ISL or Integrated Schottky Logic. ISL provides a superior speed power product with the speed of LSTTL at one-tenth the power. With oxide isolation, both the speed-power product and the gate delay of ISL are reduced by a factor of three, giving the FLEXX™ Array speed approaching ECL and power efficiency that allows large scale integration in a plastic package without special cooling.

With oxide-isolated ISL the gate used in the FLEXX™ Array has a typical delay time of 1.5 nsec. Output buffers are capable of driving up to 48 mA. The number of actual gates which can be placed on the FLEXX™ Array is limited to about 2000 by thermal constraints. The number of I/Os is limited only by package pin-out. Available packages currently include standard plastic and ceramic DIPs and a variety of chip carriers.

FLEXX™ ARRAY ARCHITECTURE



ISL GATE ARRAY

8A1200

PRODUCT DESCRIPTION

The 8A1200 Gate Array (Figure 1) is an uncommitted array of ISL gates (Figure 2), Schottky buffers (Figure 3) and LSTTL-compatible I/O cells (Figure 4). Thus, up to 1200 gates can be custom interconnected to provide the advantages of both Large Scale Integration (LSI) and proprietary design. The 8A1200 array is based on a technological subset of LSI called ISL (Integrated Schottky Logic). ISL combines the best features of low-power Schottky and I^2L Bipolar technologies.

Designing with the 8A1200 is easy and fast, requiring no more than conventional logic design, logic simulation, and custom coding of metal interconnections among preprocessed logic gates on the array—refer to Table 1 for a comparison of ISL and 74LS logic functions. The design techniques and the implementation processes are analogous to the design of a Printed Circuit Board.

Logic functions are defined by the user and are implemented by interconnecting 1144 ISL NAND gates, using two layers of metal routing. Fifty-two Schottky buffers are provided to drive multi-load internal clock or enable signals. For external interface, up to 36 LSTTL I/O buffers can be specified. As shown in Figure 4, each I/O can be configured to implement any one of 11 different functions: inputs, input/output, totem-pole, open collector, and three-state.

FEATURES

- **Customer programmable LSI**
- **1144 ISL (NAND) gates**
- **Two-layer metal interconnection**
- **52 Schottky buffers**
- **36 I/O buffers**
- **LSTTL compatible**
- **Standard PNP inputs**
- **8mA output current sink**
- **−55°C to +125°C ambient temperature**
- **4ns gate speed (typical)**
- **Speed-power product—0.7 picojoules**
- **22, 28, 40, or 44-pin package**

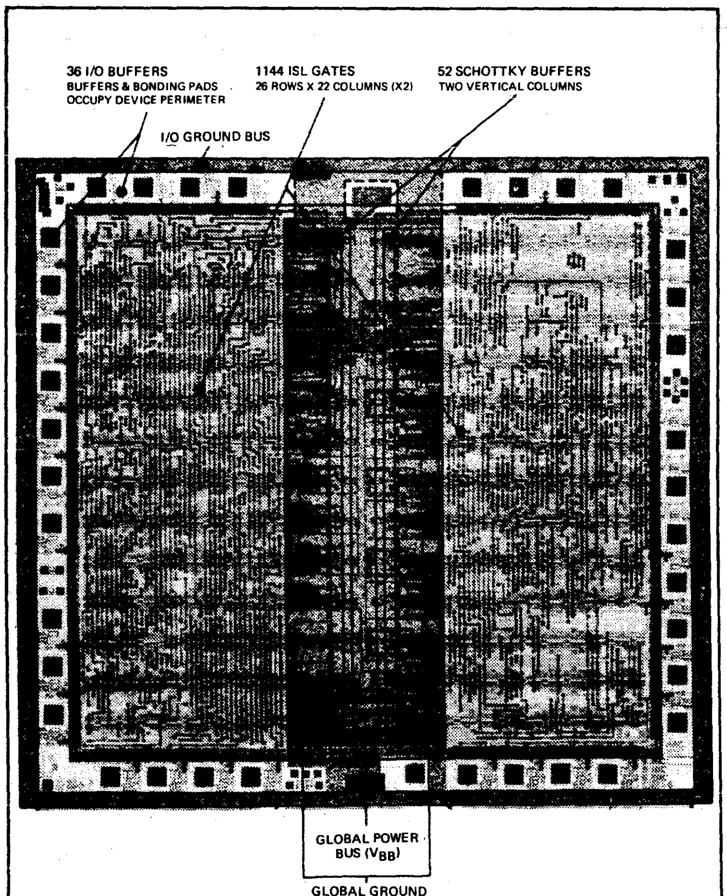


Figure 1. Internal Configuration of 8A1200 ISL Gate Array

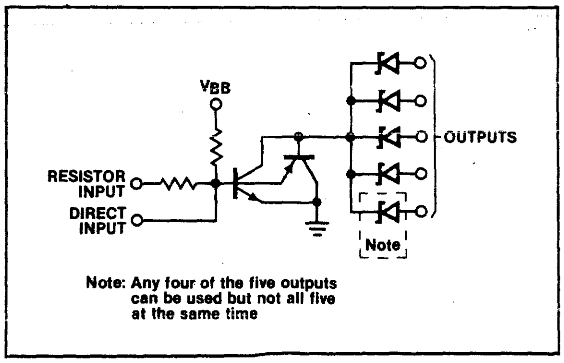


Figure 2. ISL Gate—Schematic Diagram

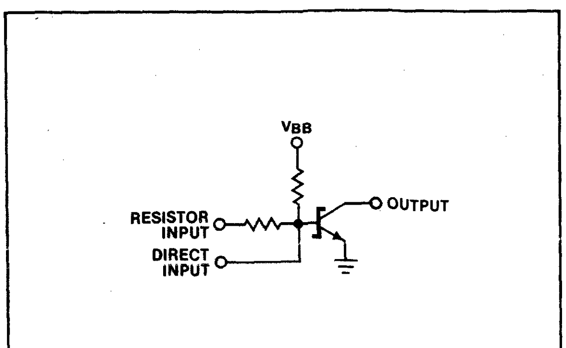
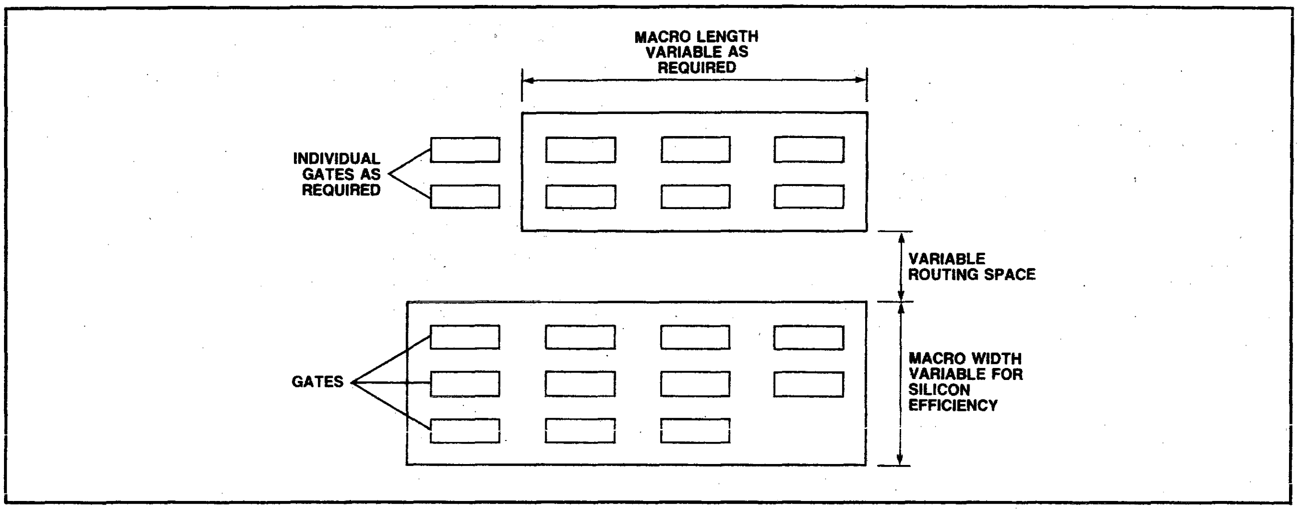


Figure 3. Schottky Buffer—Schematic Diagram

FLEXX™ ARRAY ARCHITECTURE



ISL GATE ARRAY

8A1200

PRODUCT DESCRIPTION

The 8A1200 Gate Array (Figure 1) is an uncommitted array of ISL gates (Figure 2), Schottky buffers (Figure 3) and LSTTL-compatible I/O cells (Figure 4). Thus, up to 1200 gates can be custom interconnected to provide the advantages of both Large Scale Integration (LSI) and proprietary design. The 8A1200 array is based on a technological subset of LSI called ISL (Integrated Schottky Logic). ISL combines the best features of low-power Schottky and I^2L Bipolar technologies.

Designing with the 8A1200 is easy and fast, requiring no more than conventional logic design, logic simulation, and custom coding of metal interconnections among preprocessed logic gates on the array—refer to Table 1 for a comparison of ISL and 74LS logic functions. The design techniques and the implementation processes are analogous to the design of a Printed Circuit Board.

Logic functions are defined by the user and are implemented by interconnecting 1144 ISL NAND gates, using two layers of metal routing. Fifty-two Schottky buffers are provided to drive multi-load internal clock or enable signals. For external interface, up to 36 LSTTL I/O buffers can be specified. As shown in Figure 4, each I/O can be configured to implement any one of 11 different functions: inputs, input/output, totem-pole, open collector, and three-state.

FEATURES

- **Customer programmable LSI**
- **1144 ISL (NAND) gates**
- **Two-layer metal interconnection**
- **52 Schottky buffers**
- **36 I/O buffers**
- **LSTTL compatible**
- **Standard PNP inputs**
- **8mA output current sink**
- **−55°C to +125°C ambient temperature**
- **4ns gate speed (typical)**
- **Speed-power product—0.7 picojoules**
- **22, 28, 40, or 44-pin package**

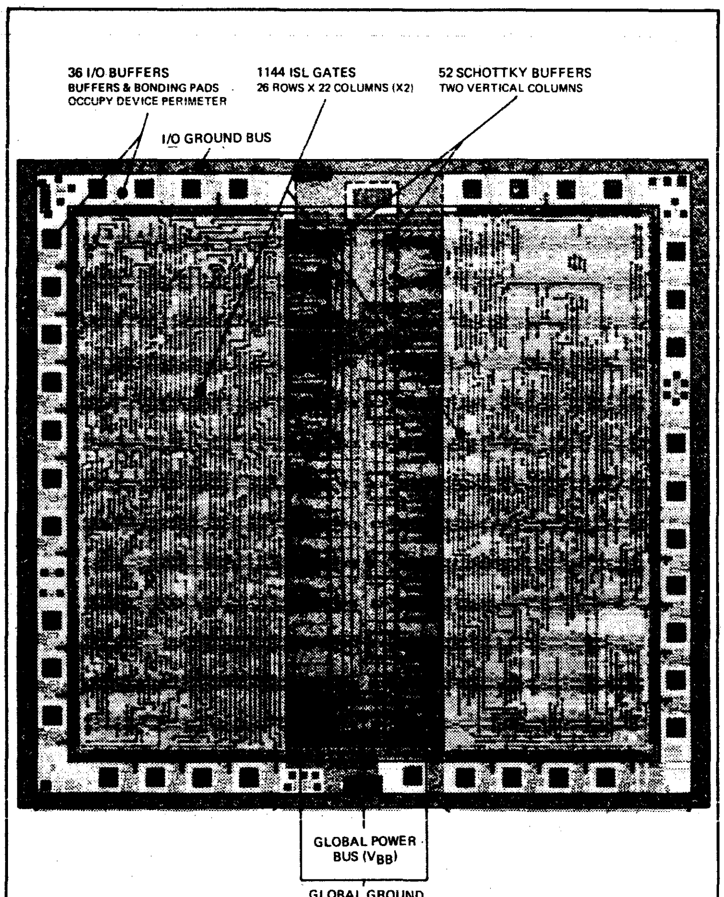


Figure 1. Internal Configuration of 8A1200 ISL Gate Array

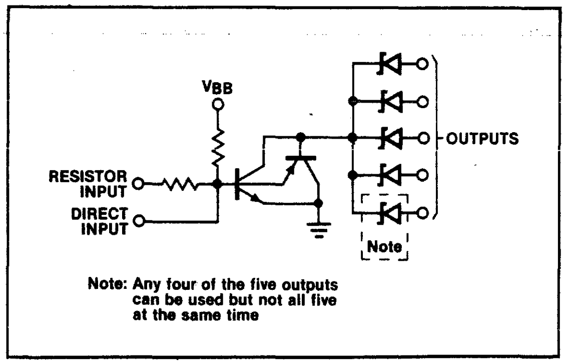


Figure 2. ISL Gate—Schematic Diagram

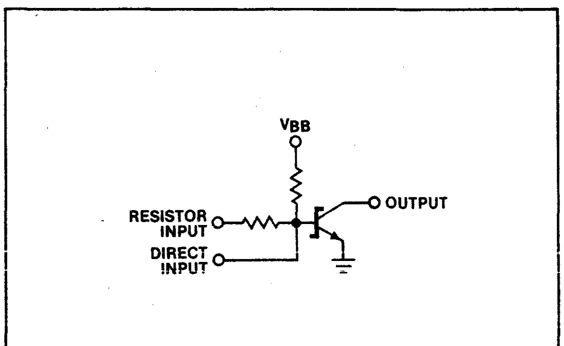


Figure 3. Schottky Buffer—Schematic Diagram

Table 1. Comparison of ISL with 74LS Functions

LOGIC FUNCTION	PARAMETERS[3]	ISL[1]	74LS	LOGIC FUNCTION	PARAMETERS[3]	ISL[1]	74LS
NAND (7400)	Power (in mW)	0.30	2.00	D FLIP-FLOP (7474)	Power (in mW)	1.50	20.00
	T_{ON} (in ns)	2.00	15.00	C→$\overline{Q}$	T_{ON} (in ns)	28.00	40.00
	T_{OFF} (in ns)	10.00	15.00		T_{OFF} (in ns)	28.00	40.00
AND (7408)	Power (in mW)	0	11.00	D LATCH (7475)	Power (in mW)	1.20	30.00
	T_{ON} (in ns)	0	20.00	DATA→$\overline{Q}$	T_{ON} (in ns)	5.00	17.00
	T_{OFF} (in ns)	2[2]	15.00		T_{OFF} (in ns)	12.00	17.00
EXCLUSIVE OR (7486)	Power (in mW)	1.20	12.50	4-INPUT MUX (74153)	Power (in mW)	1.50	25.00
	T_{ON} (in ns)	18.00	22.00	DATA→$\overline{Q}$	T_{ON} (in ns)	7.00	26.00
	T_{OFF} (in ns)	24.00	30.00		T_{OFF} (in ns)	16.00	26.00
EXCLUSIVE NOR (74266)	Power (in mW)	0.90	18.00				
	T_{ON} (in ns)	15.00	30.00				
	T_{OFF} (in ns)	16.00	30.00				

Notes:
1. Power and delay times are given for 150°C MAX.
2. T_{OFF} is 2ns for each input; T_{OFF} can be reduced to 0ns with a pullup cell which uses 0.3 mW.
3. LS power dissipation is based on $V_{CC} \times I_{MAX}$.

AC AND DC ELECTRICAL CHARACTERISTICS

Conditions:

Commercial—
V_{CC} = 5.0V (± 5%)
V_{BB} = 1.5V (± 10%)
T_A[1] = 0°C to 70°C

Military—
V_{CC} = 5.0V (± 10%)
V_{BB} = 1.5V (± 10%)
T_A[1] = −55°C to 125°C

ABSOLUTE MAXIMUM RATINGS

PARAMETER	DESCRIPTION	RATING	UNIT
V_{CC}	Supply voltage	+7.0	V
V_{BB}	ISL gate supply voltage	+7.0	V
E_{IN}	Input voltage, continuous	−0.5 to +5.5	V
I_{IN}	Input current, continuous	−30 to +1.0	mA
V_O	Voltage applied to open-collector output in off-state	−0.5 to +7.0	V
T_A	Ambient temperature, operating	−55 to +125	°C
T_{STG}	Storage temperature	−65 to +150	°C

PARAMETER		TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
ISL GATE (Internal)									
I_{BB}/G	Power supply current per gate				190			190	μA
ILF	Input load factor				1			1	Unit load
FO	Fanout				4			4	Unit load
t_{pdAV}	Average gate propagation delay $t_{pdAV} = \frac{t_{pdLH} + t_{pdHL}}{2}$	Fan-in = one (1) ISL gate or Schottky buffer; Fan-out = one (1) ISL gate or Schottky buffer		4	6		4	6	ns
t_{pdHL}2	High-to-low propagation delay	Delay is inferred from circuit simulation		1	2		1	2	ns
t_{pdLH}2	Low-to-high propagation delay			7	10		7	10	ns
SCHOTTKY BUFFER (Internal)									
I_{BB}/G	Power supply current per gate				190			190	μA
ILF	Input load factor				1			1	Unit load
FO	Fanout				10			10	Unit load
t_{pdAV}	Average gate propagation delay $t_{pdAV} = \frac{t_{pdLH} + t_{pdHL}}{2}$	Fan-in = one (1) ISL gate or Schottky buffer; Fan-out = one (1) ISL gate or Schottky buffer		4	6		4	6	ns
t_{pdHL}2	High-to-low propagation delay	Delay is inferred from circuit simulation.		1	2		1	2	ns
t_{pdLH}2	Low-to-high propagation delay			7	10		7	10	ns

	PARAMETER	TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
[illegible]									
I_{CC}	IOCD power supply current	From array = high			1.38			1.50	mA
	IOD power supply current	V_{IN} = 3V, from array = high			2.53			2.75	mA
ILF	Input load factor					3			Unit load
FO	Fanout								
	To T.S. (I/O only)	(drives 3-state inputs only)				16		16	Inputs
	To Array (I/O only)	(drives internal gates)				10		10	Unit loads
t_{pdAV}	Average propagation delay	Fan in = one (1) ISL gate or Schottky buffer			10	14	10	14	ns
	$t_{pdAV} = \frac{t_{pdLH} + t_{pdHL}}{2}$	Fan out = one (1) from 3-state input of an output buffer							
INPUT BUFFERS: INB, EOCD, TEOC [illegible]									
I_{CC}	TOC, supply current	V_{IN} = 3V, from Array = L			1.76			1.90	mA
	INB, EOCD, supply current	V_{IN} = 3V			1.15			1.25	mA
	IOD, supply current	V_{IN} = 3V, from Array = H			2.53			2.75	mA
	TEOC, supply current	V_{IN} = 3V, from TS = H, from Array = L			3.11			3.35	mA
	TTS, supply current	From Array = L, from TS = H V_{IN} = 3V			3.11			3.35	mA
V_{TH}	Input threshold voltage		0.80		2.0	0.80		2.0	V
V_{CD}	Input clamp diode voltage	I_{IN} = − 18mA			− 1.5			− 1.5	V
I_{IL}	Input low current	V_{IN} = 0.4V			− 20			− 20	μA
I_{IH}	Input high current	V_{IN} = 2.7V			20			20	μA
I_I	Max input high current	V_{IN} = 5.5V, V_{CC} = Max			100			100	μA
FO	INB & IOD "to array" outputs				10			10	Unit load
	EOCD & IOD "to 3-state" outputs				16			16	Inputs
t_{pdLH}	Propagation delay, low-to-high F.O. = one (1) ISL load	See Figure 5a		5	8		5	8	ns
t_{pdHL}	Propagation delay, high-to-low F.O. = one (1) ISL load			2	4		2	4	ns
t_{pdLH}	Propagation delay, low-to-high F.O. = ten (10) ISL loads			3	4		3	4	ns
t_{pdHL}	Propagation delay, high-to-low F.O. = ten (10) ISL loads			4	5		4	5	ns
OUTPUT BUFFER: AP (Active Pullup)									
I_{CC}	Power supply current	From array = high			1.38			1.50	mA
ILF	Input load factor		3			3			Unit loads
V_{OL}	Output low voltage	I_{OL} = 8mA			500				mV
		I_{OL} = 4mA						400	mV
V_{OH}	Output high voltage	I_{OH} = − 400μA	2.7			2.5			V
I_{OS}	Output short circuit current	V_{OUT} = 0V	− 15		− 100	− 15		− 100	mA
t_{pdLH}	Propagation delay, low to high output	See Figure 5b		4	8		4	8	ns
t_{pdHL}	Propagation delay, high to low output			4	8		4	8	ns

	PARAMETER	TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
OPEN COLLECTOR OUTPUT BUFFERS: OC, TOC (from array), EOC, TEOC (from array)									Preliminary
I_{CC}	OC power supply current	From array = high			1.38			1.50	mA
	TOC power supply current	From array = low			1.76			1.90	mA
	EOC power supply current	From array = low, from T.S. = high			1.96			2.10	mA
	TEOC power supply current	From array = low, from T.S. = high			3.11			3.35	mA
ILF	Input load factor "from array"		3			3			Unit load
	Input load factor "from T.S."		3			3			Unit load
V_{OL}	Output low voltage	I_{OL} = 8mA comm			500				mV
		I_{OL} = 4mA						400	mV
I_{OH}	Output high current	V_{OUT} = 5.5V			20			20	μA
t_{pdLH}	Propagation delay low to high output	See Figure 5c		9	TBD		9	TBD	ns
t_{pdHL}	Propagation delay high to low output			8	TBD		8	TBD	ns
THREE-STATE OUTPUT BUFFERS: TS, TTS (from array)									
I_{CC}	TS power supply current	From T.S. = high From array = low			1.96			2.10	mA
	TTS power supply current	From array = low V_{IN} = 3V, from T.S. = high			3.11			3.35	mA
ILF	Input load factor, either input		3			3			Unit load
V_{OL}	Output low voltage	I_{OL} = 8mA			500				mV
		I_{OL} = 4mA						400	mV
V_{OH}	Output high voltage	I_{OH} = – 400μA	2.7			2.5			V
I_{OS}	Output short circuit current	V_{OUT} = 0V	– 15		– 100	– 15		– 100	mA
I_{OZL}	Three-state off current, output low	V_{OUT} = 0.4V			– 20			– 20	μA
I_{OZH}	Three-state off current, output high	V_{OUT} = 2.4V			20			20	μA
t_{pdLH}	Propagation delay, low to high output	See Figure 5d		4	9		4	9	ns
t_{pdHL}	Propagation delay, high to low output			6	10		6	10	ns
t_{pdZL}	Propagation delay, HI Z to low output			11	14		11	14	ns
t_{pdZH}	Propagation delay, HI Z to high output			10	13		10	13	ns
t_{pdLZ}	Propagation delay, low to HI Z output			6	12		6	12	ns
t_{pdHZ}	Propagation delay, high to HI Z output			7	7		7	7	ns

Notes:
1. Maximum power dissipation limit of circuit is determined by package selection.
2. Guaranteed value is t_{pdAV}.
3. For all input parameters on TEOC and TTS, the "from Three-State" input should be high.

8A1200 EVALUATION CIRCUIT

CG1001

PRODUCT DESCRIPTION

The 8A1200/CG1001 Evaluation Circuit is a committed array of ISL gates, Schottky buffers, and LSTTL I/O cells, providing the user with several logic functions that can be easily and economically implemented by the use of semi-custom LSI. Basically, the CG1001 provides a demonstration vehicle for characterizing design functions of the 8A1200 ISL Gate Array; the demonstration part contains logic functions that are representative of, and can be compared with, those of standard 7400-series parts.

Also, the CG1001 contains several test configurations that can be used in evaluating circuit performance under various logical, topological, and environmental conditions. A block diagram of the Gate Array Evaluation Circuit is shown in Figure 2 and logic representations of each discrete function are shown in Figures 3 through 6.

FEATURES

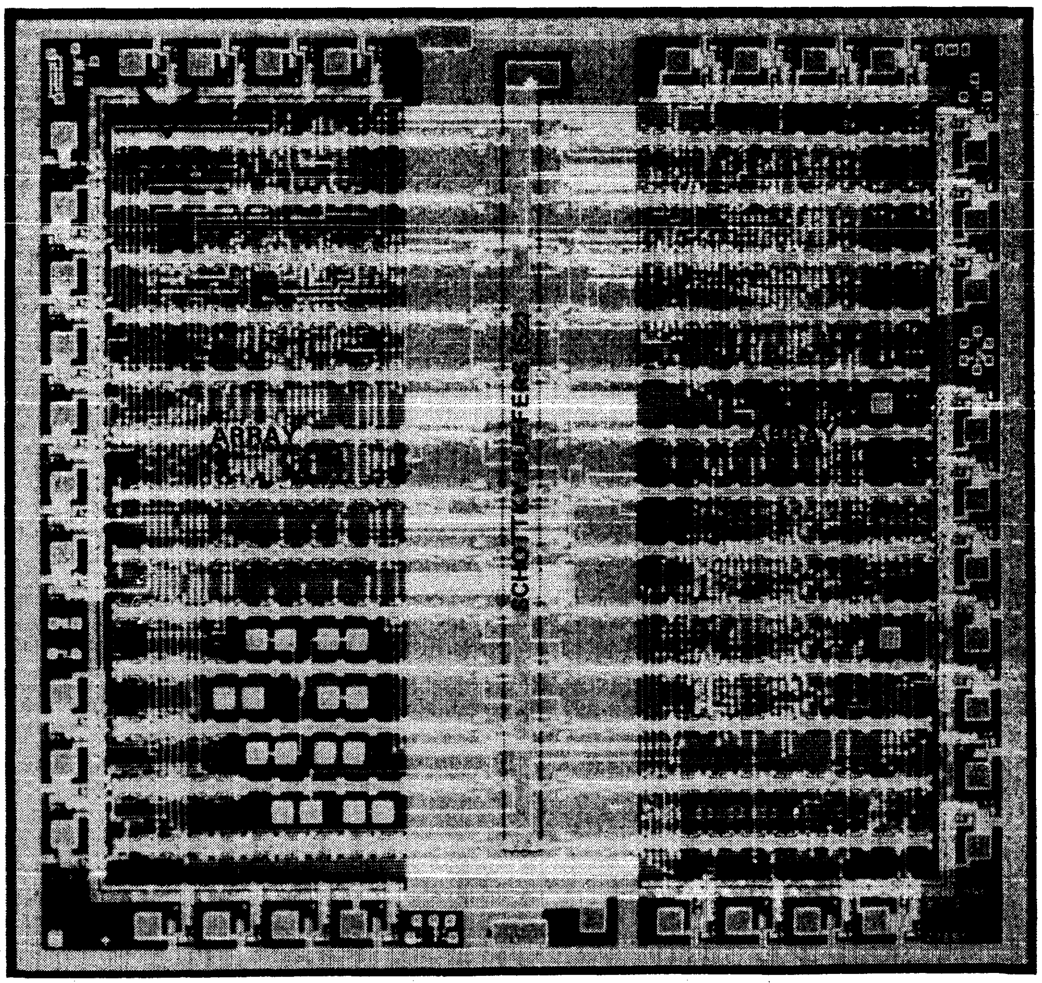
REPRESENTATIVE LOGIC FUNCTIONS:

- 8 to 1 Multiplexer (Figure 3)—similar to 74152.
- 4-Bit Adder (Figure 4)—similar to 7483.
- 4-Bit Universal Shift Register (Figure 5)—similar to 74194

SPECIAL TEST CIRCUITS

- D-flip flop wired as a toggle flip flop
- Demonstration of fanout effects on ISL gates
- Test of fanin and pattern sensitivity effects on ISL gates
- Ring oscillators which show the basic gate delays of ISL gates and Schottky buffers under various layout and logical conditions

8A1200/CG1001 EVALUATION CIRCUIT



8A1200 EVALUATION CIRCUIT

CG1001

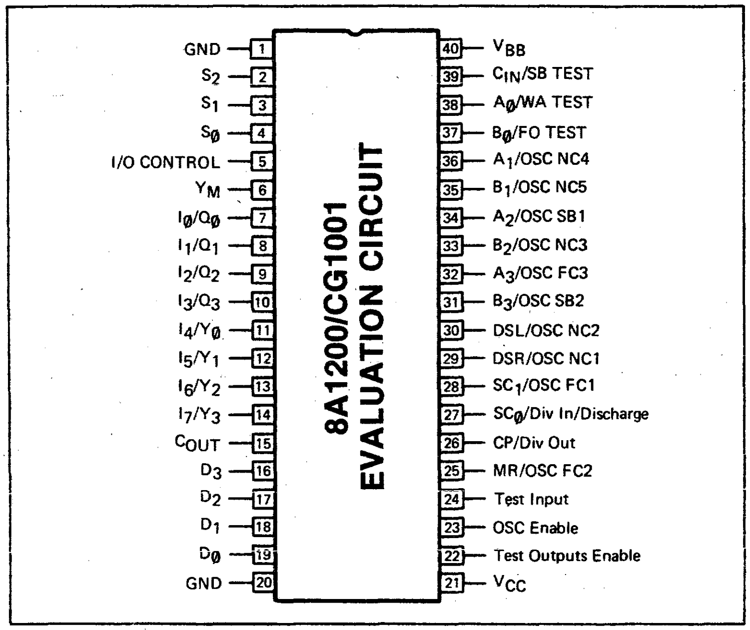


Figure 1. Package Configuration and Pin Designators of 8A1200/CG1001 Evaluation Circuit

DC ELECTRICAL CHARACTERISTICS

PARAMETER	DESCRIPTION	TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Supply current at V_{CC}	Pins 5 and 22 = L (OUTPUT ENABLES)		56	87		59	93	mA
I_{BB}	Supply current at V_{BB}			62	85		62	93	mA

Note. All other DC CHARACTERISTICS are specific to the I/O cells and can be found in the Data Sheet pertaining to the 8A1200 ISL Gate Array.

AC ELECTRICAL CHARACTERISTICS

PARAMETERS (Note 1)	REFERENCES FROM	REFERENCES TO	TEST CONDITIONS	LIMITS (COMMERCIAL) MIN	LIMITS (COMMERCIAL) TYP	LIMITS (COMMERCIAL) MAX	LIMITS (MILITARY MIN	LIMITS (MILITARY TYP	LIMITS (MILITARY MAX	UNITS
Propagation delay of 8-to-1 Multiplexer:										
t_{pdHL}	PINS 7-14	PIN 6	See test setup		40					ns
t_{pdLH}	PINS 7-14	PIN 6	below		55					ns

TEST SETUP FOR 8-TO-1 MULTIPLEXER

PIN 8 = L (INPUT)
PIN 22 = L (TEST OUTPUTS OFF)
PIN 23 = L (OSC OFF)

FUNCTION →	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	Y_M
PIN NO. →	2	3	4	7	8	9	10	11	12	13	14	6
STATES →	L	L	L	In	L	L	L	L	L	L	L	Out
	L	L	H	L	In	L	L	L	L	L	L	Out
	L	H	L	L	L	In	L	L	L	L	L	Out
	L	H	H	L	L	L	In	L	L	L	L	Out
	H	L	L	L	L	L	L	In	L	L	L	Out
	H	L	H	L	L	L	L	L	In	L	L	Out
	H	H	L	L	L	L	L	L	L	In	L	Out
	H	H	H	L	L	L	L	L	L	L	In	Out

PARAMETERS (Note 1)	REFERENCES FROM	REFERENCES TO	TEST CONDITIONS	LIMITS (COMMERCIAL) MIN	LIMITS (COMMERCIAL) TYP	LIMITS (COMMERCIAL) MAX	LIMITS (MILITARY) MIN	LIMITS (MILITARY) TYP	LIMITS (MILITARY) MAX	UNITS
Propagation delay of 4-Bit Adder:										
t_{pdHL}	PIN 39	PIN 15			41					ns
t_{pdLH}			See test setup		40					ns
t_{pdHL}	PIN 39	PIN 11	below		42					ns
t_{pdLH}					35					ns
t_{pdHL}	PIN 32	PIN 15			40					ns
t_{pdLH}					35					ns

TEST SETUP FOR 4-BIT ADDER

PIN 8 = H (OUTPUT)
PIN 22 = L (TEST OUTPUTS OFF)
PIN 23 = L (OSC OFF)

FUNCTION →	B_3	A_3	B_2	A_2	B_1	A_1	B_0	A_0	C_{IN}	Y_3	Y_2	Y_1	Y_0	C_{OUT}
PIN NO. →	31	32	33	34	35	36	37	38	39	14	13	12	11	15
STATES	L	H	L	H	L	H	L	H	In	X	X	X	X	Out
	L	L	L	L	L	L	L	L	In	X	X	X	Out	X
	H	In	L	H	L	H	L	H	L	X	X	X	X	Out

Signetics

CUSTOM/SEMICUSTOM

8A1200 EVALUATION CIRCUIT

CG1001

AC ELECTRICAL CHARACTERISTICS (cont'd)

PARAMETERS (Note 1)	REFERENCES FROM	REFERENCES TO	TEST CONDITIONS	LIMITS (COMMERCIAL) MIN	LIMITS (COMMERCIAL) TYP	LIMITS (COMMERCIAL) MAX	LIMITS (MILITARY) MIN	LIMITS (MILITARY) TYP	LIMITS (MILITARY) MAX	UNITS
Propagation delay of Fan-In/Fan-Out tests:										
t_{pdHL}	PIN 24	PIN 37	See test setup		37					ns
t_{pdLH}			"r" below		36					ns
t_{pdHL}			See test setups		38					ns
t_{pdLH}			"s" and "t" below		35					ns
t_{pdHL}			See test setups		37					ns
t_{pdLH}			"v" and "w" below		33					ns
t_{pdHL}	PIN 24	PIN 38	See test setup		744					ns
t_{pdLH}			"p" below		737					ns
t_{pdHL}			See test setup		39					ns
t_{pdLH}			"r" below		40					ns
t_{pdHL}			See test setups		40					ns
t_{pdLH}			"s" "t", and "u' below		40					ns
t_{pdHL}			See test setups		51					ns
t_{pdLH}			"v", "w", and "x" below		40					ns
t_{pdHL}	PIN 24	PIN 39	See test setup		35					ns
t_{pdLH}			"r" below		35					ns
t_{pdHL}			See test setup		34					ns
t_{pdLH}			"s" below		36					ns
t_{pdHL}			See test setup		28					ns
t_{pdLH}			"v" below		38					ns

TEST SETUPS FOR FAN-IN/FAN-OUT TESTS (See DELAY COMPARISONS)

PIN 5 = L (INPUT)
PIN 22 = H (TEST OUTPUTS ON)
PIN 23 = L (OSC OFF)

TEST SETUP	SELECTOR S_1 PIN 3	SELECTOR S_0 PIN 4	DISCHARGE (NOTE 2) PIN 27	LOAD PIN 2	TEST INPUT PIN 24	FAN-OUT TEST PIN 37	Wired-AND TEST PIN 38	SCHOTTKY BUFFER TEST PIN 39
p	L	L	L	L	In	–	Out	–
r	L	H	L	L	In	Out	Out	Out
s	H	L	L	L	In	Out	Out	Out
t	H	L	‾_/‾	H	In	Out	Out	–
u	H	L	‾_/‾	L	In	–	Out	–
v	H	H	L	L	In	Out	Out	Out
w	H	H	‾_/‾	H	In	Out	Out	–
x	H	H	‾_/‾	L	In	–	Out	–

Signetics

CUSTOM/SEMICUSTOM

8A1200 EVALUATION CIRCUIT

CG1001

AC ELECTRICAL CHARACTERISTICS (cont'd)

PARAMETERS (Note 1)	REFERENCES		TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
	FROM	TO		MIN	TYP	MAX	MIN	TYP	MAX	
Propagation delay of 4-Bit Shift Register:			See test setup							
t_{pdHL}	PIN 26	PINS 7,8	below		34					ns
t_{pdLH}					34					ns
t_{pdHL}	PIN 26	PIN 9			37					ns
t_{pdLH}					34					ns
t_{pdHL}	PIN 26	PIN 10			33					ns
t_{pdLH}					33					ns
t_{pdHL}	PIN 25	PINS 7-10			33					ns

TEST SETUP FOR 4-BIT SHIFT REGISTER [illegible]

FUNCTION (NOTES 3, 4, & 5) →	CP	$\overline{MR}$	$SC_\emptyset$	SC_1	D_{ST}	D_{SL}	$D_\emptyset$	D_1	D_2	D_3	$Q_\emptyset$	Q_1	Q_2	Q_3
PIN NO. →	26	25	27	28	29	30	19	18	17	16	7	8	9	10
STATES →	In(↑)	H	H	H	X	X	D_{IN}	X	X	X	Out	X	X	X
	In(↑)	H	H	H	X	X	X	X	D_{IN}	X	X	X	Out	X
	In(↑)	H	H	H	X	X	X	X	X	D_{IN}	X	X	X	Out
	X	In	X	X	X	X	X	X	X	X	Out	Out	Out	Out

8A1200 EVALUATION CIRCUIT

CG1001

AC ELECTRICAL CHARACTERISTICS (cont'd)

PARAMETERS (Note 1)	REFERENCES		TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
	FROM	TO		MIN	TYP	MAX	MIN	TYP	MAX	
Propagation delay for Divider:										
t_{pdHL}	PIN 27	PIN 26	See test setup below		44					ns
t_{pdLH}					39					ns
Period of Ring Oscillator:										
tosc	–	PIN 25	See test setup below		108					ns
tosc	–	PIN 28			109					ns
tosc	–	PIN 29			107					ns
tosc	–	PIN 30			106					ns
tosc	–	PIN 31			101					ns
tosc	–	PIN 32			107					ns
tosc	–	PIN 33			86					ns
tosc	–	PIN 34			91					ns
tosc	–	PIN 35			147					ns
tosc	–	PIN 36			82					ns

TEST SETUP FOR DIVIDER/RING OSCILLATORS

PIN 23 = L (OSC OFF)

PIN 5 = L (INPUT)
PIN 22 = H (TEST OUTPUTS ON)
PIN 23 = H (OSC ON)

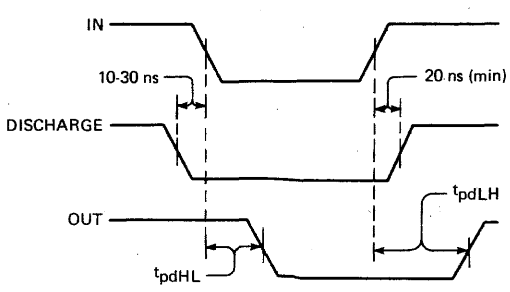
DIV IN PIN 27	DIV OUT PIN 26	OSC FC2 PIN 25	OSC FC1 PIN 28	OSC NC1 PIN 29	OSC NC2 PIN 30	OSC SB2 PIN 31	OSC FC3 PIN 32	OSC NC3 PIN 33	OSC SB1 PIN 34	OSC NC5 PIN 35	OSC NC4 PIN 36
In(↑)	Out	Oscillator Calculations: The ten 11-gate rings oscillate with a period (t_{osc}) equal to 22 gate delays. Average gate delay (t_{avg} = half pair delay) can be calculated as follows:									

$$t_{avg} = \frac{t_{osc}}{22} = \frac{t_{pdLH} + t_{pdHL}}{2}$$

Notes:

1. Measure t_{pdLH} and t_{pdHL} from "In" to "Out" for each path.
2. Discharge input (pin 27) must meet both MIN and MAX times for setup and hold– see WAVEFORM 1.
3. For Q_0 and Q_1 outputs (pins 7 and 8), propagation delay is representative of the delay through an input buffer, a three-state output buffer with a fan-in of 1, and a standard ISL "D" flip-flop.
4. For the Q_2 output (pin 9), the propagation delay will differ from that of Q_0 and Q_1 by the Δ time delay caused by the additional fan-in of 4 on the three-state output buffer.
5. For the Q_3 output (pin 10), the propagation delay will differ from that of Q_0 and Q_1 by the Δ time delay caused by the additional fan-in of 2 on the three-state output buffer.

WAVEFORM 1: Discharge Input Timing



DELAY COMPARISONS

Wired-AND Test (Pin 38)

COMPARISON (Note 1)	DESCRIPTION
(r) – (s)	Effect of Δ fan-in of 4 on ISL gate delay, load capacitors precharged
(r) – (u)	Effect of Δ fan-in of 4 on ISL gate delay, load capacitors discharged
(s) – (v)	Effect of Δ fan-in of 5 on ISL gate delay, load capacitors precharged
(u) – (x)	Effect of Δ fan-in of 5 on ISL gate delay, load capacitors discharged
(r) – (v)	Effect of Δ fan-in of 9 on ISL gate delay, load capacitors precharged
(r) – (x)	Effect of Δ fan-in of 9 on ISL gate delay, load capacitors discharged
(t) – (u)	Effect of dummy loads, fan-in = 5
(w) – (x)	Effect of dummy loads, fan-in = 10
(s) – (u)	Effect of worst case pattern sensitivity, fan-in = 5
(v) – (x)	Effect of worst case pattern sensitivity, fan-in = 10
(p)	Delay of 142 ISL gates + input buffer + T.S. output buffer

Signetics

CUSTOM/SEMICUSTOM

ISL GATE ARRAY

8A1260

PRODUCT DESCRIPTION

The 8A1260 Gate Array (Figure 1) is an uncommitted array of ISL gates (Figure 2), Schottky buffers (Figure 3) and LSTTL-compatible I/O cells (Figure 4). Thus, up to 1200 gates can be custom interconnected to provide the advantages of both Large Scale Integration (LSI) and proprietary design. The 8A1260 array is based on a technological subset of LSI called ISL (Integrated Schottky Logic). ISL combines the features of Schottky and the density of I²L Bipolar technologies.

Designing with the 8A1260 is easy and fast, requiring no more than conventional logic design, logic simulation, and custom coding of metal interconnections among preprocessed logic gates on the array. Refer to Table 1 for a comparison of ISL and 74LS logic functions. The design techniques and the implementation processes are analogous to the design of a Printed Circuit Board.

Logic functions are defined by the user and are implemented by interconnecting 1144 ISL NAND gates, using two layers of metal routing. Fifty-two Schottky buffers are provided to drive multi-load internal clock or enable signals. For external interface, up to 60 LSTTL I/O buffers can be specified. Each I/O can be configured as 1-of-4 input buffers, 1-of-4 output buffers, or as a combination of one input buffer and one output buffer for a transceiver.

FEATURES

- **Customer programmable LSI**
- **1144 ISL (NAND) gates**
- **Two-layer metal interconnection**
- **52 Schottky buffers**
- **60 I/O buffers**
- **LSTTL compatible**
- **Standard PNP inputs**
- **8mA output current sink**
- **−55°C to +125°C ambient temperature**
- **4ns gate speed (typical)**
- **Speed-power product—0.7 picojoules**
  68 pin package

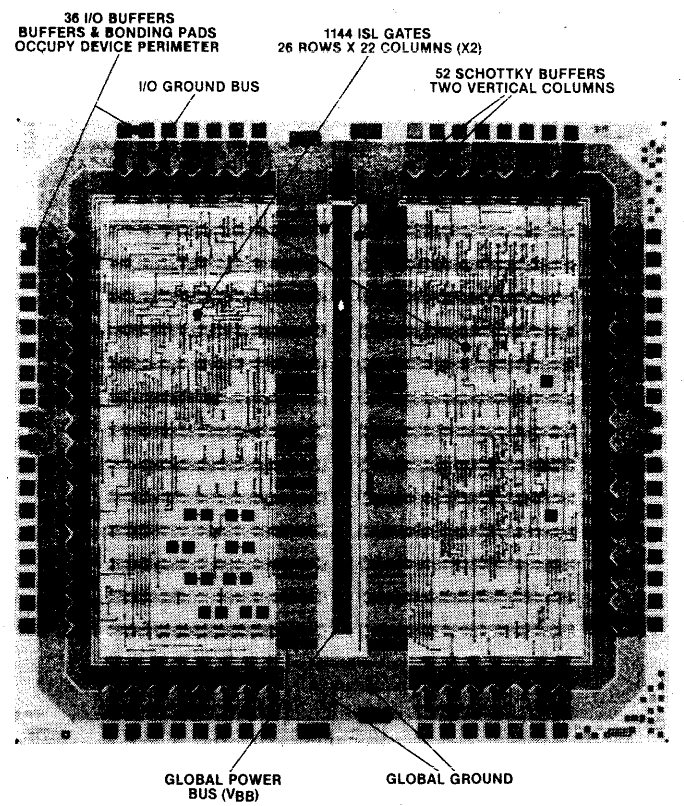


Figure 1. Internal Configuration of 8A1260

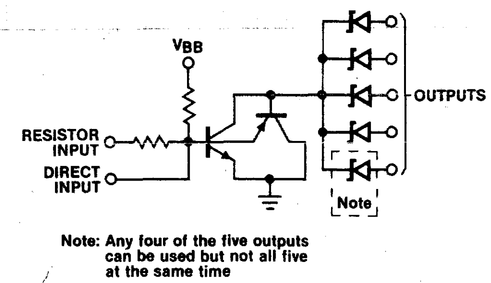


Figure 2. ISL Gate—Schematic Diagram

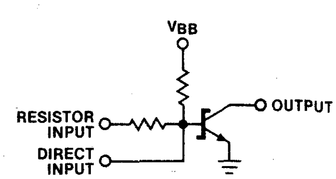


Figure 3. Schottky Buffer—Schematic Diagram

AC AND DC ELECTRICAL CHARACTERISTICS

Conditions:

Commercial—	Military—
V_{CC} = 5.0V (± 5%)	V_{CC} = 5.0V (± 10%)
V_{BB} = 1.5V (± 10%)	V_{BB} = 1.5V (± 10%)
T_A = 0°C to 70°C	T_A = −55°C to 125°C

ABSOLUTE MAXIMUM RATINGS

PARAMETER	DESCRIPTION	RATING	UNIT	PARAMETER	DESCRIPTION	RATING	UNIT
V_{CC}	Supply voltage	+7.0	V	V_O	Voltage applied to open-collector output in off-state	−0.5 to +7.0	V
V_{BB}	ISL gate supply voltage	+7.0	V				
E_{IN}	Input voltage, continuous	−0.5 to +5.5	V	T_A	Ambient temperature, operating	−55 to +125	°C
I_{IN}	Input current, continuous	−30 to +1.0	mA	T_{STG}	Storage temperature	−65 to +150	°C

PARAMETER		TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
ISL GATE (Internal)									
I_{BB}/G	Power supply current per gate				190			190	μA
ILF	Input load factor				1			1	Unit load
FO	Fan-out				4			4	Unit load
t_{pdAV}	Average gate propagation delay $t_{pdAV} = \frac{t_{pdLH} + t_{pdHL}}{2}$	Fan-in = one (1) ISL gate or Schottky buffer; Fan-out = one (1) ISL gate or Schottky buffer		4	6		4	6	ns
t_{pdHL}	High-to-low propagation delay	Delay is inferred from circuit simulation		1	2		1	2	ns
t_{pdLH}	Low-to-high propagation delay			7	10		7	10	ns

ISL GATE ARRAY

8A1260

PARAMETER		TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SCHOTTKY BUFFER (Internal)									
I_{BB}/G	Power supply current per gate				190			190	μA
ILF	Input load factor				1			1	Unit load
FO	Fan-out				10			10	Unit load
t_{pdAV}	Average gate propagation delay $t_{pdAV} = \frac{t_{pdLH} + t_{pdHL}}{2}$	Fan-in = one (1) ISL gate or Schottky buffer Fan-out = one (1) ISL gate or Schottky buffer		4	6		4	6	ns
t_{pdHL}	High-to-low propagation delay	Delay is inferred from circuit simulation		1	2		1	2	ns
t_{pdLH}	Low-to-high propagation delay			7	10		7	10	ns
INPUT BUFFERS: IN, IN7, IO, and IOT									
I_{CC}	Power supply current	V_{IN} = 3V(IN from Array = H)			1.30			1.40	mA
VTH	Input threshold voltage		0.80		2.0	0.80		2.0	V
VCD	Input clamp diode voltage	$I_{IN} = -18mA$			– 1.5			–1.5	V
I_{IL}	Input low current	$V_{IN} = 0.4V$			– 20			–20	μA
I_{IH}	Input high current	$V_{IN} = 2.7V$			20			20	μA
I_I	Max input high current	$V_{IN} = 5.5V$, V_{CC} = Max			100			100	μA
FO	INB & IOD "to array" outputs				10			10	Unit load
	EOCD & IOD "to three-state" outputs				16			16	Unit load
t_{pdLH}	Propagation delay, low-to-high F.O. = one (1) ISL load	(See Fig. 5a)		5	8		5	8	ns
t_{pdHL}	Propagation delay, high-to-low F.O. = one (1) ISL load			2	4		2	4	ns
t_{pdLH}	Propagation delay, low-to-high F.O. = ten (10) ISL loads			3	4		3	4	ns
t_{pdHL}	Propagation delay, high-to-low F.O. = ten (10) ISL loads			4	5		4	5	ns
OUTPUT BUFFER: AP (Active Pullup)									
I_{CC}	Power supply current	From array = high			1.38			1.50	mA
ILF	Input load factor		3			3			Unit loads
V_{OL}	Output low voltage	$I_{OL} = 8mA$ $I_{OL} = 4mA$			500			 400	mV mV
V_{OH}	Output high voltage	$I_{OH} = -400\mu A$	2.7			2.5			V
I_{OS}	Output short circut current	V_{OUT} = OV	– 15		– 100	–15		–100	mA

PARAMETER		TEST CONDITIONS	LIMITS (COMMERCIAL) MIN	TYP	MAX	LIMITS (MILITARY) MIN	TYP	MAX	UNITS
OUTPUT BUFFER: AP (Active Pullup) (continued)									
t_{pdLH}	Propagation delay, low-to-high output			4	8		4	8	ns
t_{pdHL}	Propagation delay, high-to-low output	(See Fig. 5b)		4	8		4	8	ns
OPEN COLLECTOR, OUTPUT BUFFERS: OC AND EOC [illegible]									
I_{CC}	OC power supply current	From array = high			1.38			1.50	mA
	EOC power supply current	From array = low, From T.S. = high			1.98			2.10	mA
ILF	Input load factor "from array"		3			3			Unit load
	Input load factor "from T.S."		3			3			Unit load
VOL	Output low voltage	I_{OL} = 8mA			500				mV
		I_{OL} = 4mA						400	mV
IOH	Output high current	V_{OUT} = 5.5V			20			20	μA
t_{pdLH}	Propagation delay, low-to-high output			9	TBD		9	TBD	ns
t_{pdHL}	Propagation delay, high-to-low output	(See Fig. 5c)		8	TBD		8	TBD	ns
THREE-STATE OUTPUT BUFFERS: TS [illegible]									
I_{CC}	TS power supply current	From T.S. = high, From array = low			1.98			2.10	mA
ILF	Input load factor, either input		3			3			Unit load
V_{OL}	Output low voltage	I_{OL} = 8mA			500				mV
		I_{OL} = 4mA						400	mV
V_{OH}	Output high voltage	I_{OH} = −400μA	2.7			2.5			V
I_{OS}	Output short circuit current	V_{OUT} = OV	− 15		− 100	−15		−100	mA
I_{OLZ}	Three-state off current, output low	V_{OUT} = 0.4V			− 20			−20	μA
I_{OHZ}	Three-state off current,	V_{OUT} = 2.4V			20			20	μA
t_{pdLH}	Propagation delay, low-to-high output (Note)	R_L = 2K		4	9		4	9	ns
t_{pdHL}	Propagation delay, high-to-low output (Note)	C_L = 15pf		6	10		6	10	ns
t_{pdZL}	Propagation delay, HI-Z to low output			11	14		11	14	ns
t_{pdZH}	Propagation delay, HI-Z to high output			10	13		10	13	ns
t_{pdLZ}	Propagation delay, LOW to HI-Z output	(See Fig. 5d)		6	12		6	12	ns
t_{pdHZ}	Propagation delay, high to HI-Z output			7	7		7	7	ns

Note: Guaranteed value is $t_{pd(Ave)}$

PRODUCT DESCRIPTION

The 8A1542 Gate Array (Figure 1) is an uncommitted array of ISL gates (Figure 2), Schottky buffers (Figure 3) and LSTTL-compatible I/O cells (Figure 4). Thus, up to 1400 gates can be custom interconnected to provide the advantages of both Large Scale Integration (LSI) and proprietary design. The 8A1542 array is based on a technological subset of LSI called ISL (Integrated Schottky Logic). ISL combines the best features of low-power Schottky and I^2L Bipolar technologies.

Designing with the 8A1542 is easy and fast, requiring no more than conventional logic design, logic simulation, and custom coding of metal interconnections among preprocessed logic gates on the array—refer to Table 1 for a comparison of ISL and 74LS logic functions. The design techniques and the implementation processes are analogous to the design of a Printed Circuit Board.

Logic functions are defined by the user and are implemented by interconnecting 1408 ISL NAND gates, using two layers of metal routing. Sixty-four Schottky buffers are provided to drive multi-load internal clock or enable signals. For external interface, up to 42 LSTTL I/O buffers can be specified. As shown in Figure 4, each I/O can be configured to implement any one of 11 different functions: inputs, input/output, totem-pole, open collector, and three-state.

FEATURES

- **Customer programmable LSI**
- **1408 ISL (NAND) gates**
- **Two-layer metal interconnection**
- **64 Schottky buffers**
- **42 I/O buffers**
- **LSTTL compatible**
- **Standard PNP inputs**
- **8mA output current sink**
- **−55°C to +125°C ambient temperature**
- **4ns gate speed (typical)**
- **Speed-power product—0.7 picojoules**
- **28, 40, or 44-pin package**

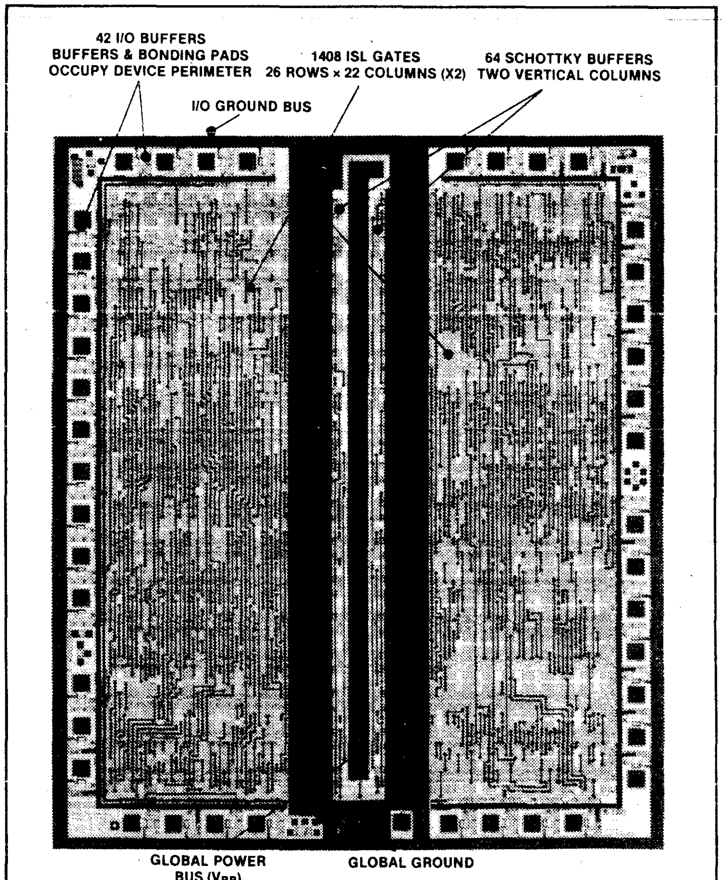


Figure 1. Internal Configuration of 8A1542 ISL Gate Array

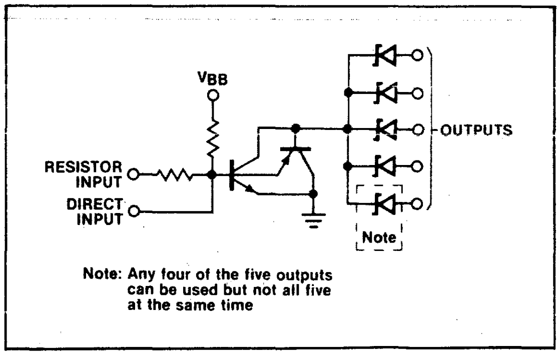


Figure 2. ISL Gate—Schematic Diagram

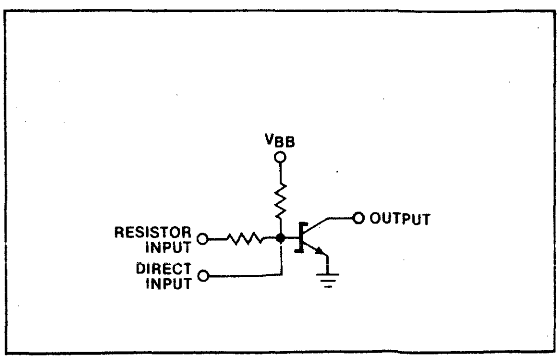


Figure 3. Schottky Buffer—Schematic Diagram

ISL GATE ARRAY

8A1542

AC AND DC ELECTRICAL CHARACTERISTICS

Conditions: Commercial— V_{CC} = 5.0V (± 5%), V_{BB} = 1.5V (± 10%), T_A[1] = 0°C to 70°C

Military— V_{CC} = 5.0V (± 10%), V_{BB} = 1.5V (± 10%), T_A[1] = − 55°C to 125°C

ABSOLUTE MAXIMUM RATINGS

PARAMETER	DESCRIPTION	RATING	UNIT
V_{CC}	Supply voltage	+ 7.0	V
V_{BB}	ISL gate supply voltage	+ 7.0	V
E_{IN}	Input voltage, continuous	−0.5 to +5.5	V
I_{IN}	Input current, continuous	−30 to +1.0	mA
V_O	Voltage applied to open-collector output in off-state	−0.5 to +7.0	V
T_A	Ambient temperature, operating	−55 to +125	°C
T_{STG}	Storage temperature	−65 to +150	°C

PARAMETER		TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
ISL GATE (internal)									
I_{BB}/G	Power supply current per gate				190			190	μA
ILF	Input load factor				1			1	Unit load
FO	Fanout				4			4	Unit load
t_{pdAV}	Average gate propagation delay $t_{pdAV} = \frac{t_{pdLH} + t_{pdHL}}{2}$	Fan-in = one (1) ISL gate or Schottky buffer; Fan-out = one (1) ISL gate or Schottky buffer		4	6		4	6	ns
t_{pdHL}2	High-to-low propagation delay	Delay is inferred from circuit simulation		1	2		1	2	ns
t_{pdLH}2	Low-to-high propagation delay			7	10		7	10	ns
SCHOTTKY BUFFER (internal)									
I_{BB}/G	Power supply current per gate				190			190	μA
ILF	Input load factor				1			1	Unit load
FO	Fanout				10			10	Unit load
t_{pdAV}	Average gate propagation delay $t_{pdAV} = \frac{t_{pdLH} + t_{pdHL}}{2}$	Fan-in = one (1) ISL gate or Schottky buffer; Fan-out = one (1) ISL gate or Schottky buffer		4	6		4	6	ns
t_{pdHL}2	High-to-low propagation delay	Delay is inferred from circuit simulation		1	2		1	2	ns
t_{pdLH}2	Low-to-high propagation delay			7	10		7	10	ns

ISL GATE ARRAY

8A1542

	PARAMETER	TEST CONDITIONS	LIMITS (COMMERCIAL) MIN	LIMITS (COMMERCIAL) TYP	LIMITS (COMMERCIAL) MAX	LIMITS (MILITARY) MIN	LIMITS (MILITARY) TYP	LIMITS (MILITARY) MAX	UNITS
INTERNAL OUTPUTS: [illegible]									
I_{CC}	IOCD power supply current IOD power supply current	From array = high V_{IN} = 3V, from array = high			1.38 2.53			1.50 2.75	mA mA
ILF	Input load factor		3			3			Unit load
FO	Fanout To T.S. (I/O only) To Array (I/O only)	 (drives 3-state inputs only) (drives internal gates)			 16 10			 16 10	 Inputs Unit loads
t_{pdAV}	Average propagation delay $t_{pdAV} = \frac{t_{pdLH} + t_{pdHL}}{2}$	Fan in = one (1) ISL gate or Schottky buffer Fan out = one (1) from 3-state input of an output buffer		10	14		10	14	ns
INPUT BUFFERS AND [illegible]									
I_{CC}	TOC, supply current INB, EOCD, supply current IOD, supply current TEOC, supply current TTS, supply current	V_{IN} = 3V, from Array = L V_{IN} = 3V V_{IN} = 3V, from Array = H V_{IN} = 3V, from TS = H, from Array = L From Array = L, from TS = H V_{IN} = 3V			1.76 1.15 2.53 3.11 3.11			1.90 1.25 2.75 3.35 3.35	mA mA mA mA mA
V_{TH}	Input threshold voltage		0.8		2.0	0.80		2.0	V
V_{CD}	Input clamp diode voltage	I_{IN} = – 18mA			– 1.5			– 1.5	V
I_{IL}	Input low current	V_{IN} = 0.4V			– 20			– 20	μA
I_{IH}	Input high current	V_{IN} = 2.7V			20			20	μA
I_I	Max input high current	V_{IN} = 5.5V, V_{CC} = Max			100			100	μA
FO	INB & IOD "to array" outputs EOCD & IOD "to 3-state" outputs				10 16			10 16	Unit load Inputs
t_{pdLH}	Propagation delay, low-to-high F.O. = one (1) ISL load			5	8		5	8	ns
t_{pdHL}	Propagation delay, high-to-low F.O. = one (1) ISL load			2	4		2	4	ns
t_{pdLH}	Propagation delay, low-to-high F.O. = ten (10) ISL loads			3	4		3	4	ns
t_{pdHL}	Propagation delay, high-to-low F.O. = ten (10) ISL loads			4	5		4	5	ns
OUTPUT BUFFER: AP (Active Pullup)									
I_{CC}	Power supply current	From array = high			1.38			1.50	mA
ILF	Input load factor		3			3			Unit loads
V_{OL}	Output low voltage	I_{OL} = 8mA I_{OL} = 4mA			500 			 400	mV mV
V_{OH}	Output high voltage	I_{OH} = – 400μA	2.7			2.5			V
I_{OS}	Output short circuit current	V_{OUT} = 0V	– 15		– 100	– 15		– 100	mA
t_{pdLH}	Propagation delay, low to high output			4	8		4	8	ns
t_{pdHL}	Propagation delay, high to low output			4	8		4	8	ns

	PARAMETER	TEST CONDITIONS	LIMITS (COMMERCIAL) MIN	LIMITS (COMMERCIAL) TYP	LIMITS (COMMERCIAL) MAX	LIMITS (MILITARY) MIN	LIMITS (MILITARY) TYP	LIMITS (MILITARY) MAX	UNITS
OPEN COLLECTOR, OUTPUT BUFFERS: OC, TOC (from array), EOC, TEOC (from array)									Preliminary
I_{CC}	OC power supply current	From array = high			1.38			1.50	mA
	TOC power supply current	From array = low			1.76			1.90	mA
	EOC power supply current	From array = low, from T.S. = high			1.96			2.10	mA
	TEOC power supply current	From array = low, from T.S. = high			3.11			3.35	mA
ILF	Input load factor "from array"		3			3			Unit load
	Input load factor "from T.S."		3			3			Unit load
V_{OL}	Output low voltage	I_{OL} = 8mA			500				mV
		I_{OL} = 4mA						400	mV
I_{OH}	Output high current	V_{OUT} = 5.5V			20			20	μA
t_{pdLH}	Propagation delay low to high output			9	TBD		9	TBD	ns
t_{pdHL}	Propagation delay high to low output			8	TBD		8	TBD	ns
THREE-STATE OUTPUT BUFFERS: TS, TTS (from array)									
I_{CC}	TS power supply current	From T.S. = high From array = low			1.96			2.10	mA
	TTS power supply current	From array = low V_{IN} = 3V, from T.S. = high			3.11			3.35	mA
ILF	Input load factor, either input		3			3			Unit load
V_{OL}	Output low voltage	I_{OL} = 8mA			500				mV
		I_{OL} = 4mA						400	mV
V_{OH}	Output high voltage	I_{OH} = −400μA	2.7			2.5			V
I_{OS}	Output short circuit current	V_{OUT} = 0V	−15		−100	−15		−100	mA
I_{OZL}	Three-state off current, output low	V_{OUT} = 0.4V			−20			−20	μA
I_{OZH}	Three-state off current, output high	V_{OUT} = 2.4V			20			20	μA
t_{pdLH}	Propagation delay, low to high output			4	9		4	9	ns
t_{pdHL}	Propagation delay, high to low output			6	10		6	10	ns
t_{pdZL}	Propagation delay, HI Z to low output			11	14		11	14	ns
t_{pdZH}	Propagation delay, HI Z to high output			10	13		10	13	ns
t_{pdLZ}	Propagation delay, low to HI Z output			6	12		6	12	ns
t_{pdHZ}	Propagation delay, high to HI Z output			7	7		7	7	ns

Notes:
1. Maximum power dissipation limit of circuit is determined by package selection.
2. Guaranteed value is t_{pdAV}.
3. For all input parameters on TEOC and TTS, the "from Three-State" input should be high.

PRODUCT DESCRIPTION

The 8A1664 Gate Array (Figure 1) is an uncommitted array of ISL gates (Figure 2), Schottky Buffers (Figure 3), and the LSTTL compatible I/O cells. Thus, up to 1600 gates can be custom interconnected to provide the advantages of both Large Scale Integration (LSI) and proprietary design. The 8A1664 array is based on a technological subset of LSI called ISL (Integrated Schottky Logic). ISL combines the features of Schottky and the density of I^2L Bipolar technologies.

Designing with the 8A1664 is easy and fast, requiring no more than conventional logic design, logic simulation, and custom coding of metal interconnections among preprocessed logic gates on the array. The design techniques and the implementation processes are analogous to the design of a Printed Circuit Board.

Logic functions are defined by the user and are implemented by interconnecting 1560 ISL NAND gates, using two layers of metal routing. Sixty Schottky buffers are provided to drive multi-load internal clock or enable signals. For external interface, up to 64 LS TTL I/O buffers can be specified. Each 8-milliampere I/O site can be configured as 1-of-6 input/internal buffers or as 1-of-8 output buffers; each 24-milliampere I/O site can also be configured as 1-of-6 input/internal buffers but the output buffer configuration can be 1-of-12. For a transceiver, either I/O site can be connected in combinations of one input and one output buffer.

FEATURES

- **Customer programmable LSI**
- **1560 ISL (NAND) gates**
- **Two-layer metal interconnection**
- **60 Schottky buffers**
- **64 I/O buffers**
- **LS TTL compatible**
- **Standard PNP inputs**
- **8-, or 24-milliamperes output current sink**
- **−55°C to +125°C ambient temperature**
- **4-nanosecond gate speed (typical)**
- **Speed-power product — 0.7 picojoules**
- **68 pin package**

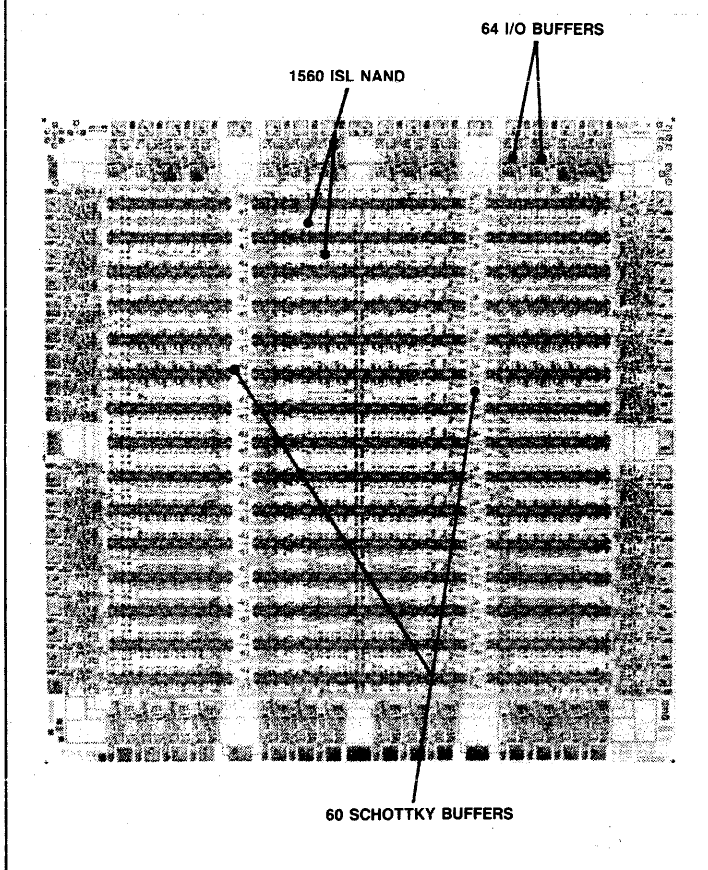


Figure 1. Internal Configuration of 8A1664

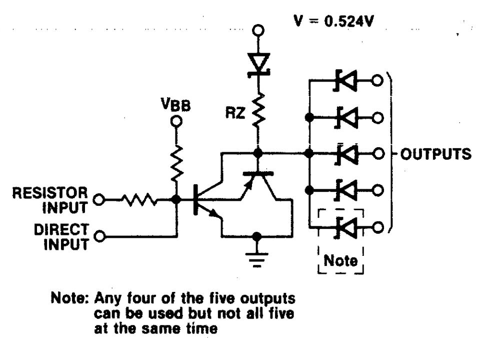


Figure 2. ISL Gate — Schematic Diagram

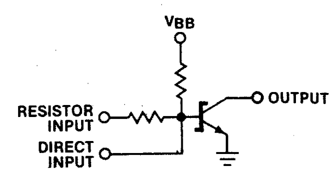


Figure 3. Schottky Buffer — Schematic Diagram

PRODUCT DESCRIPTION

The 8A1864 Gate Array (Figure 1) is an uncommitted array of ISL gates (Figure 2). Schottky buffers (Figure 3) and LSTTL-compatible I/O cells. Thus, up to 1740 gates and 60 buffers can be interconnected to provide the advantages of both Large Scale Integration (LSI) and proprietary design. The 8A1864 array is based on a technological subset of LSI called ISL (integrated Schottky Logic). ISL combines the features of Schottky and the density of I^2L Bipolar technologies.

Designing with the 8A1864 is easy and fast, requiring no more than conventional logic design, logic simulation, and coding of metal interconnections between preprocessed logic gates on the array. The design techniques and the implementation processes are analogous to the design of a Printed Circuit Board.

Logic functions are defined by the user and are implemented by interconnecting up to 1740 ISL NAND gates, and up to 60 buffers, using two layers of metal routing. Sixty Schottky buffers are provided to drive multi-load internal clock or enable signals. For external interface, up to 64 LS TTL I/O buffers can be specified. Each 8-milliampere I/O site can be configured as 1-of-6 input/internal buffers or as 1-of-8 output buffers; each 24-milliampere I/O site can also be configured as 1-of-6 input/internal buffers but the output buffer configuration can be 1-of-12. For a transceiver, either I/O site can be connected in combinations of one input and one output buffer.

FEATURES

- **Customer programmable LSI**
- **1740 ISL (NAND) gates**
- **Two-layer metal interconnection**
- **60 Schottky buffers**
- **72 I/O buffers**
- **LS TTL compatible**
- **Standard PNP inputs**
- **8-, or 24-milliamperes output current sink**
- **−55°C to +125°C ambient temperature**
- **4-nanosecond gate speed (typical)**
- **Speed-power product — 0.7 picojoules**
- **40-, 44-, 50- or 68-pin packages**

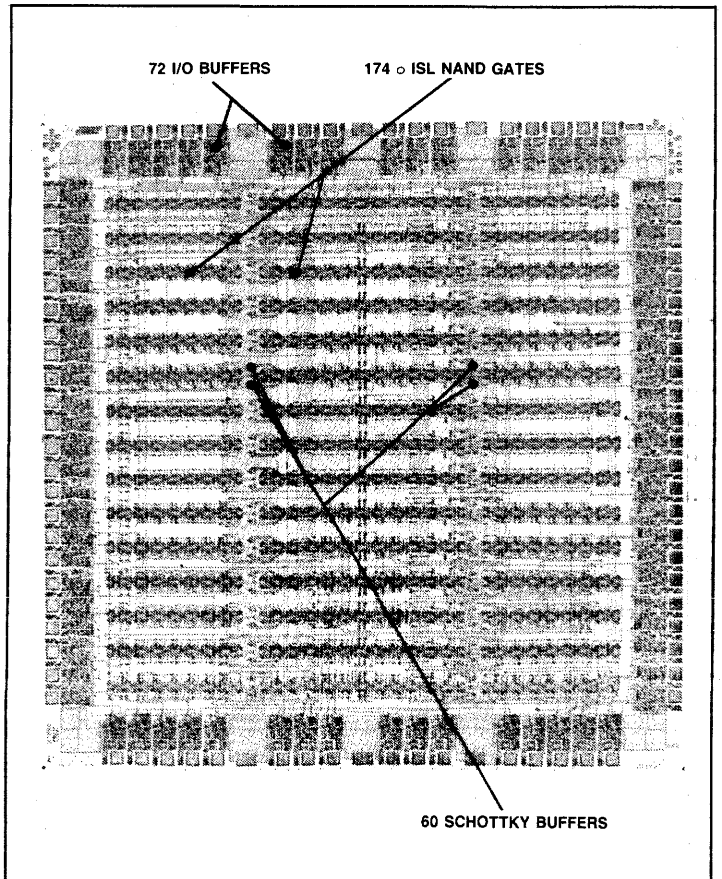


Figure 1. Internal Configuration of 8A1864

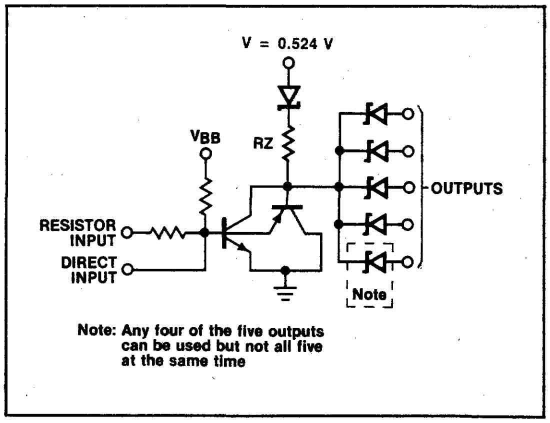


Figure 2. ISL Gate — Schematic Diagram

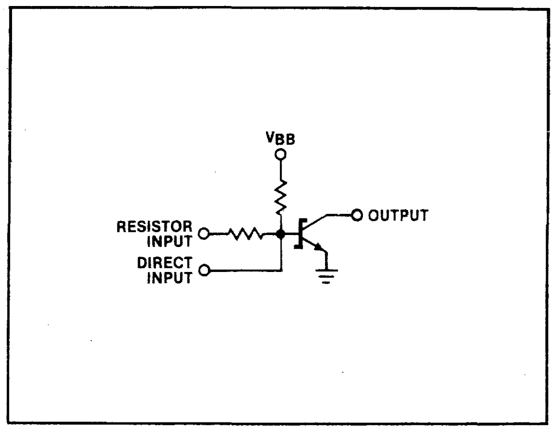


Figure 3. Schottky Buffer — Schematic Diagram

PRODUCT DESCRIPTION

The 8A2176 Gate Array (Figure 1) is an uncommitted array of ISL gates (Figure 2), Schottky buffers (Figure 3) and LSTTL-compatible I/O cells. Thus, up to 2016 gates can be custom interconnected to provide the advantages of both Large Scale Integration (LSI) and proprietary design. The 8A2176 76 array is based on a technological subset of LSI called ISL (Integrated Schottky Logic). ISL combines the features of Schottky and the density of I^2L Bipolar technologies.

Designing with the 8A2176 is easy and fast, requiring no more than conventional logic design, logic simulation, and custom coding of metal interconnections among preprocessed logic gates on the array. The design techniques and the implementation processes are analogous to the design of a Printed Circuit Board.

Logic functions are defined by the user and are implemented by interconnecting 2016 ISL NAND gates, using two layers of metal routing. Seventy-two Schottky buffers are provided to drive multi-load internal clock or enable signals. For external interface, up to 76 LSTTL I/O buffers can be specified.

Each 8-milliampere I/O site can be configured as 1-of-6 input/internal buffers or as 1-of-8 output buffers; each 24-milliampere I/O site can also be configured as 1-of-6 input/internal buffers but the output buffer configuration can be 1-of-12. For a transceiver, either I/O site can be connected in combinations of one input and one output buffer.

FEATURES

- **Customer programmable LSI**
- **2016 ISL (NAND) gates**
- **72 Schottky buffers**
- **76 I/O buffers**
- **LS TTL compatible**
- **Standard PNP inputs**
- **8 mA and 24 mA output current sink**
- **−55°C to +125°C ambient temperature**
- **4 ns gate speed (typical)**
- **Speed power product −0.7 picojoules**
- **28, 40, 68, or 84 pin package**

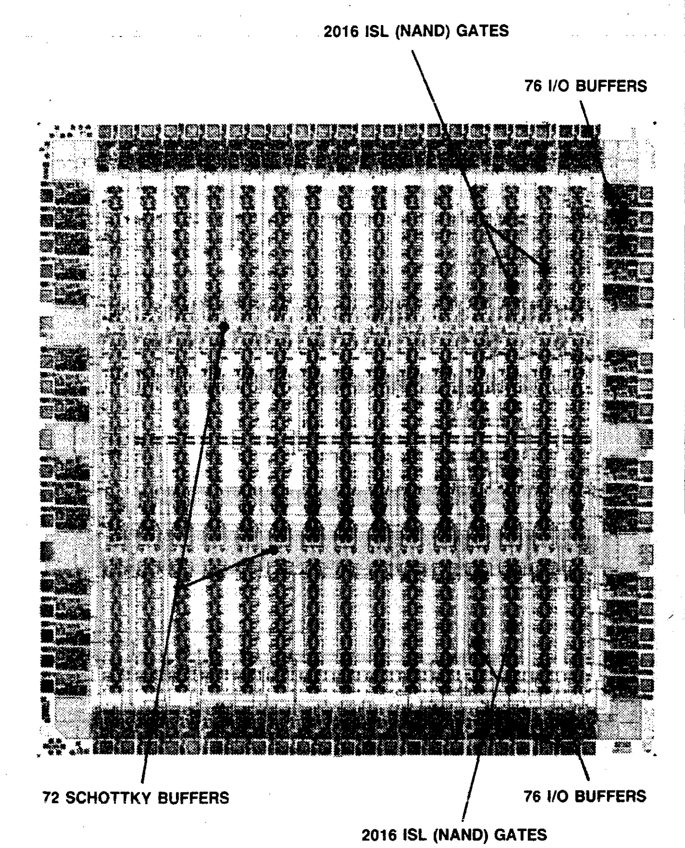


Figure 1. Internal Configuration of 8A1276

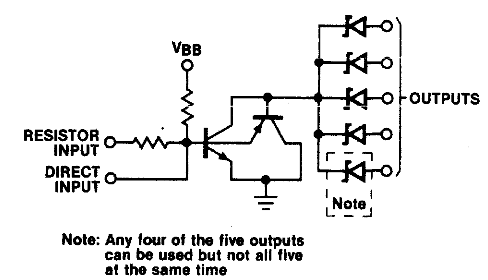


Figure 2. ISL Gate — Schematic Diagram

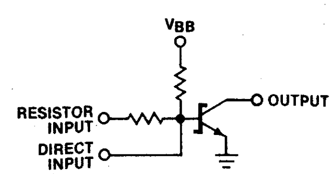


Figure 3. Schottky Buffer — Schematic Diagram

PRODUCT DESCRIPTION

Composite Cell Logic (CCL) provides a standard-cell approach to semi-custom bipolar logic. Besides the inherent advantages of LSI and proprietary design, CCL offers the designer a fast turnaround time, a high probability of first-pass success, and a die size that exactly meets all functional requirements of the logic. The CCL approach is particularly well suited to design applications where circuit complexities fall within a range of 100-to-1000 gates.

Figure 1 shows the CCL device together with two standard cells that might be used in the design process. At present, the available cells form two libraries—the Extended Performance Library (EPL) and the Integrated Schottky Library (ISL). Typically, the EPL cell (Figure 2) is used where speed is a critical factor—the speed of EPL cells is comparable to that of Schottky T^2L logic. *Note. Refer to table elsewhere in this data sheet for nominal figures pertaining to circuit propagation speeds of Schottky, Low-Power Schottky, T^2L, and Low-Power T^2L.* All EPL cells are input-expandable with no added delay, are highly immune to internal/external noise, and use active pullups to reduce sensitivity to lead capacitance and the effects of wire-ANDing.

The packing density of an ISL cell (Figure 3) is two to three times greater than that for EPL and the power required is only one-tenth (1/10) to one-twentieth (1/20) as great. The speed of ISL is slightly faster than that of Low-Power Schottky logic. For some circuits, the propagation speeds for ISL and EPL are nearly the same; for other circuits, there are appreciable differences. The speed-comparison table shown later in this data sheet provides a worthwhile guide for overall circuit design.

Output cells of both libraries can sink up to 80-milliamperes of current and both EPL and ISL cells use a 16-micron grid for easy conversion to "Automatic Place and Route" techniques—see Table 1 for a technical summary of both libraries.

Designing with CCL requires a cooperative effort between Signetics and the Customer. The contribution of each party and the overall development sequence are shown in Figure 4.

DESIGN FEATURES

- **Customer designed LSI**
- **Two cell libraries—EPL and ISL**
- **TTL compatible—each cell is functionally similar to the equivalent 7400 Logic Device**
- **Two-layer metal interconnects**
- **PNP or diode inputs**
- **Open-collector, active pullup, or three-state outputs**
- **80-milliampere sink-current capability for output cells**
- **Accommodate custom cell design**
- **Most standard packages available**
- **−55°C to +150°C junction temperature**
- **+5V (±10%) supply voltage; conditions permitting, on-chip derivation of V_{BB} (+1.5V)**

Table 1. Technical Summary of EPL and ISL Libraries

PARAMETER	EPL		ISL
Output structure	Active pullup		Open collector
Input structure	Schottky diode		Schottky diode
Worst-case noise margin	300mV (F.O. = 15)		70mV (F.O. = 15)
Junction temperature range	−55° to +155°C		−55° to +155°C
Power supply	+5V (±10%)		+1.5V (±10%)
	MEDIUM POWER	LOW POWER	
Max average speed (in ns)			
F.O. = 1 (T_J = 150°C)	4.5	5.5	6
F.O. = 6 (T_J = 150°C)	5.5	7.5	6 or 9*
Max average power (in mW):			
T_J = 150°C	5.6	2.6	0.3
Packing density gates/mm**	14 to 42		26 to 78

*Average speed of 6ns requires the use of a resistor pullup cell (optional).

**See Note 5 in Selection Guide regarding derivation of maximum values.

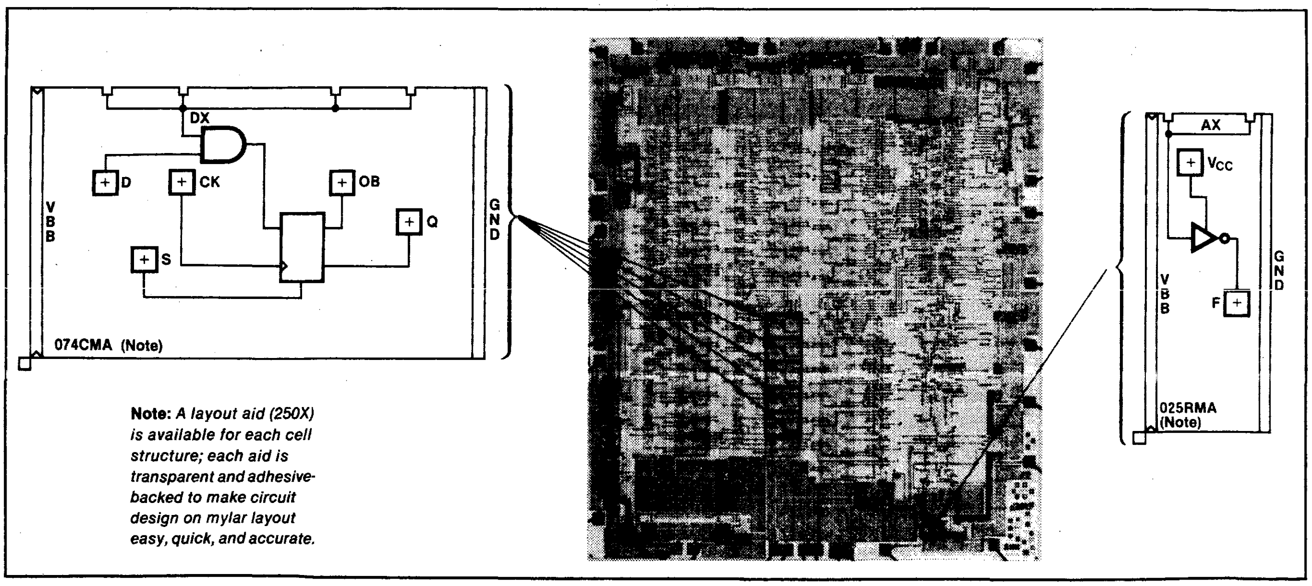


Figure 1. Composite Cell Logic Showing Typical Cell Placement with the Use of Layout Aids.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	DESCRIPTION	RATING	UNIT
V_{CC}	Supply voltage	+7.0	V
V_{BB}	ISL gate supply voltage	+7.0	V
E_{IN}	Input voltage, continuous	−0.5 to +5.5	V
I_{IN}	Input current, continuous	−30 to +1.0	mA
V_O	Voltage applied to open-collector output in off-state	−0.5 to +7.0	V
T_A	Ambient temperature, operating	−55 to +125	°C
T_{STG}	Storage temperature	−65 to +150	°C

AC AND DC ELECTRICAL CHARACTERISTICS

Conditions[1]: $V_{CC} = 5.0V\ (\pm 10\%)$
$V_{BB} = 1.5V\ (\pm 10\%)$
$T_J = 0°C$ to $+150°C$

PARAMETER		TEST CONDITIONS[2]		DESIGN LIMITS[3] MIN	TYP	MAX	UNIT
EPL GATE (INTERNAL)							
$I_{CC/G}$	Power supply current per gate			0.18	0.29	0.47	mA
I_{LF}	Input load factor				1		UL
F_O	Fan-Out				15		
t_{pdAV}	Average gate propagation delay $= \frac{t_{pdLH} + t_{pdHL}}{2}$	Fan-in = 1 EPL gate; Fan-out = 1 EPL gate			3	5.5	ns
t_{pdLH}	Propagation delay from low-to-high state	Fan-in = 1 EPL gate; Fan-out = 1 EPL gate			4	7	ns
t_{pdHL}	Propagation delay from high-to-low state				2	4	ns
ISL GATE (INTERNAL)							
$I_{BB/G}$	Power supply current per gate			110	150	190	µA
I_{LF}	Input load factor				1		UL
F_O	Fan-out				6		UL
t_{pdAV}	Average gate propagation delay $= \frac{t_{pdLH} + t_{pdHL}}{2}$	Fan-in = 1 ISL gate; Fan-out = 1 ISL gate			3	6	ns
t_{pdLH}	Propagation delay from low-to-high state	Fan-in = 1 ISL gate; Fan-out = 1 ISL gate			5	10	ns
t_{pdHL}	Propagation delay from high-to-low state				1	2	ns
EPL/ISL INPUT CELLS							
V_{TH}	Input threshold voltage			0.8		2.0	V
V_{CD}	Input clamp diode voltage	$I_{IN} = -18mA$				−1.2	V
I_{IL}	Input low current	$V_{IN} = 0.4V$	PNP input			−20	mA
			Diode input			−400	mA
I_{IH}	Input high current	$V_{IN} = 2.7V$				20	µA
I_I	Maximum input high current	$V_{IN} = 5.5V$				100	µA
F_O	Fan-out (ISL library)	Standard cell				6	UL
		Clock buffer cell				64	UL
	Fan-out (EPL library)	Standard cell				15	UL
		Clock buffer cell				55	UL
		Clock buffer cell				100	UL

AC AND DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER		TEST CONDITIONS[2]			DESIGN LIMITS[3] MIN	TYP	MAX	UNIT
EPL/ISL THREE-STATE OUTPUT BUFFERS								
I_{LF}	Input load factor	EPL					1 or 9	UL
		ISL					2 or 4	
V_{OL}	Output low voltage	Military: 4mA					400	mV
		Commercial: 8mA					500	
		Military: 12 mA					400	mV
		Commercial: 24 mA					500	
V_{OH}	Output high voltage	Military: $I_{OH} = -400\mu A$			2.5			V
		Commercial: $I_{OH} = -400\mu A$			2.7			
I_{OS}	Output short circuit current	$V_{OUT} = 0V$			−15		−100	mA
I_{OLZ}	Three-state off current (output low)	$V_{OUT} = 0.4V$					−20	μA
I_{OHZ}	Three-state off current (output high)	$V_{OUT} = 2.4V$					20	μA
EPL/ISL OPEN-COLLECTOR OUTPUT BUFFERS								
I_{LF}	Input load factor	EPL	8 mA output				1	UL
			20 mA output				3	
			80 mA output				5	
		ISL					2 or 4	
V_{OL}	Output low voltage	I_{OL}	8 mA output				500	mV
			20 mA				500	
			70 mA				500	
			80 mA				800	
I_{OH}	Output leakage current	V_{OUT}	80 mA Cells	2.75			60	μA
				5.5V			250	
			8/20 mA Cells	5.5V			100	
ACTIVE PULLUP OUTPUT BUFFER								
I_{LF}	Input load factor	EPL					1 or 3	UL
		ISL					2 or 4	
V_{OL}	Output low voltage	$I_{OL} = 8$ mA or 20 mA					500	mV
V_{OH}	Output high voltage	Military	$I_{OH} = -400\mu A$ or -1.0 mA		2.5			V
		Commercial	$I_{OH} = -400\mu A$ or -1.0 mA		2.7			
I_{OS}	Output short circuit current	$V_{OUT} = 0V$	8 mA output		−15		−100	mA
			20 mA output		−40		−100	

Notes:
1. Maximum power dissipation is determined from individual cell data sheets; the figures are then summed to calculate total power for the chip. The total power must be less than the Maximum Power Dissipation (P_d) calculated earlier in this data sheet.
2. For test circuits and timing waveforms, refer to individual cell data sheets in the CCL Design Guide.
3. Design limits are based on standard modeling with similar circuits used in Signetics standard bipolar LSI products. Actual simulation limits are maintained to be consistent with characterization updates for the CCL libraries.

ORDERING INFORMATION

For additional information pertaining to Composite Cell Logic, Gate Arrays, and other Semicustom Products, contact the nearest Signetics Sales Office.

PRODUCT DESCRIPTION

The Signetics Advanced Customized ECL (ACE) family of products provides the user with a cost-effective technology, futuristic speeds, and other high-performance alternatives for the design of LSI-based systems. Basic cell designs are implemented with Emitter Coupled and Common Mode Logic (ECL/CML) to guarantee the very best compromise between speed, power, and interface capabilities—see Figure 1 and TECHNICAL SUMMARY that follows.

At present, the ACE product line is available with gate complements of 600, 900, 1320, 1400, and 2200; the 1320 array actually contains 1000 gates with an on-board 320-bit RAM. The 600/900-gate arrays, described in this data sheet, are well-suited for low-cost applications and for use in systems that do not require 25-ohm terminations. To meet the flexibility requirements, the rise-and-fall times for I/O cells of these arrays are mask-selectable and bidirectional and TTL interfaces are standard.

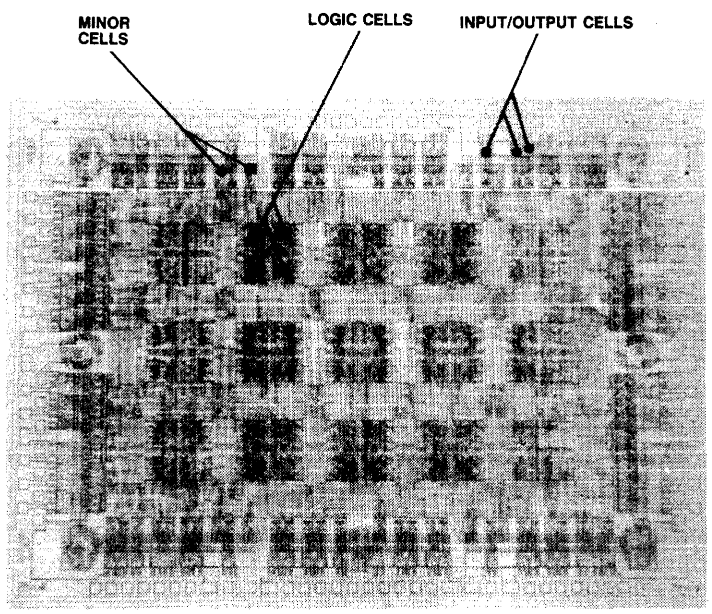
All ACE arrays are I/O compatible with the 10K/100K ECL logic family and all are fabricated with a very mature process; thus, even with 3-micron first-metal geometry, first pass success is a virtual certainty. The speed-power product for devices in the ACE family is in the neighborhood of 1 to 3 picojoules, permitting heat-sink cooling at ambient air temperatures. The ACE family and MACRO library is alternately sourced by a major supplier of semicustom devices.

To summarize, the designer, using ACE, is limited only by innovation and imagination:

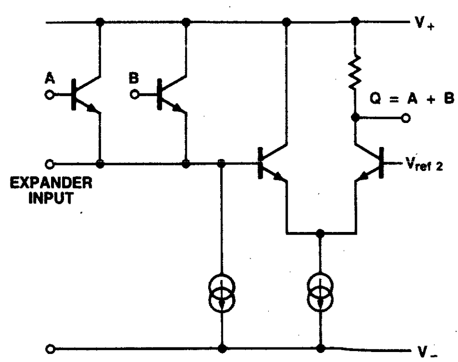
- ECL/CML Technology for SPEED and EFFICIENCY
- Mature process for PRODUCT CERTAINTY
- Computer aided design for QUICK DELIVERY
- Pin grid packages (socket insertion) for RELIABILITY
- Signetics for QUALITY

FEATURES

- **3-micron geometry (first metal)**
- **Internal gate delays as low as 300 picoseconds (average gate delay of 450 picoseconds)**
- **Expandable 80-cell MACRO library**
- **Mask-selectable rise/fall times for I/O interface cells**
- **Bidirectional and TTL interfaces**
- **10K/100K ECL compatibility**
- **Computer aided design (CAD) for layout, simulation, and testing**
- **Mature process (SUBILO P)**
- **Pin grid array packages for easy socket insertion**
- **25 and 50 ohm drive capability**



Typical ACE Array Showing Cell Locations



Typical ACE Cell

Figure 1. Chip Architecture and Typical Circuit

ADVANCED CUSTOMIZED ECL (ACE)

ACE 600 & ACE 900

MASTER SLICE LOGIC ARRAYS

TECHNICAL SUMMARY OF ACE FAMILY

PARAMETER	ACE 600	ACE 900	ACE 1320	ACE 1400	ACE 2200
Major cells	24	36	48	60	100
Input/output cells	28	28	96	96	128
Input cells	30	42	—	—	—
Worst case noise margin	24 - 45 mV		24 - 45 mV		
Junction temperature range	30 - 125°C		30 - 125°C		
Average prop delay (internal gate)	0.3 - 0.5 ns		0.3 - 0.5 ns		
	10K LEVEL	100K LEVEL	10K LEVEL	100K LEVEL	
Power supply	−5.25V ± 5%	−4.5V ± 5%	−5.25V ± 5%	−4.5V ± 5%	
Power consumption	2.1 - 2.7 mW	1.8 - 2.3 mW	4.6 - 6.3 mW	4 - 5.5 mW	

ACE PACKAGE TYPE AND THERMAL RESISTIVITY SELECTION				
	PACKAGE	THERMAL RESISTIVITY (°C/W)		
		HEAT SINK	NO AIR FLOW	5 m/s AIR FLOW
ACE 600 & ACE 900	64 Pin	Yes	25	13
		No	50	25
ACE 1320, ACE 1400 & ACE 2200	144 Pin	Yes	12	6
		No	24	12

ADVANCED CUSTOMIZED ECL (ACE) — ACE 1320, ACE 1400 & ACE 2200

MASTER SLICE LOGIC ARRAYS

PRODUCT DESCRIPTION

The Signetics Advanced Customized ECL (ACE) family of products provides the user with a cost-effective technology, futuristic speeds, and other high-performance alternatives for the design of LSI-based systems. Basic cell designs are implemented with Emitter Coupled and Common Mode Logic (ECL/CML) to guarantee the very best compromise between speed, power, and interface capabilities—see Figure 1 and TECHNICAL SUMMARY that follows.

At present, the ACE product line is available with gate complements of 600, 900, 1320, 1400, and 2200; the 1320 array actually contains 1000 gates with an on-board 320-bit RAM. The 1320/1400/2200 gate arrays, described in this data sheet, are particularly well suited for complex applications requiring relatively high gate counts and considerable design flexibility. To meet the flexibility requirements, the rise-and-fall times for I/C cells of these arrays are mask-selectable and bidirectional and TTL interfaces are standard.

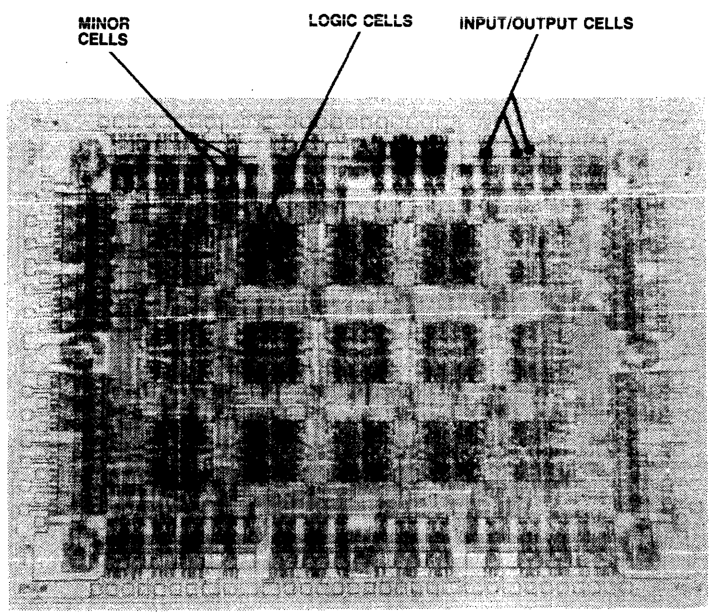
All ACE arrays are I/O compatible with the 10K/100K ECL logic family and all are fabricated with a very mature process; thus, even with 3-micron first-metal geometry, first pass success is a virtual certainty. The speed-power product for devices in the ACE family is in the neighborhood of 1 to 3 picojoules, permitting heat-sink cooling at ambient air temperatures. The ACE family and MACRO library is alternately sourced by a major supplier of semicustom devices.

To summarize, the designer, using ACE, is limited only by innovation and imagination:

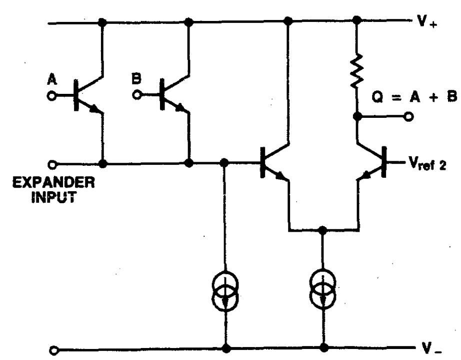
- ECL/CML Technology for SPEED and EFFICIENCY
- Mature process for PRODUCT CERTAINTY
- Computer aided design for QUICK DELIVERY
- Pin grid packages (socket insertion) for RELIABILITY
- Signetics for QUALITY

FEATURES

- **3-micron geometry (first metal)**
- **Internal gate delays as low as 300 picoseconds (average gate delay of 450 picoseconds)**
- **Expandable 80-cell MACRO library**
- **Mask-selectable rise/fall times for I/O interface cells**
- **Bidirectional and TTL interfaces**
- **10K/100K ECL compatibility**
- **Computer aided design (CAD) for layout, simulation, and testing**
- **Mature process (SUBILO P)**
- **Pin grid array packages for easy socket insertion**
- **25-ohm and 50-ohm load drive capability**



Typical ACE Array Showing Cell Locations



Typical ACE Cell

Figure 1. Chip Architecture and Typical Circuit

ADVANCED CUSTOMIZED ECL (ACE) ACE 1320, ACE 1400 & ACE 2200

MASTER SLICE LOGIC ARRAYS

TECHNICAL SUMMARY OF ACE FAMILY

PARAMETER	ACE 600	ACE 900	ACE 1320	ACE 1400	ACE 2200
Major cells	24	36	48	60	100
Input/output cells	28	28	96	96	128
Input cells	30	42	—	—	—
Worst case noise margin	24 - 45 mV		24 - 45 mV		
Junction temperature range	30 - 125°C		30 - 125°C		
Average prop delay (internal gate)	0.3 - 0.5 ns		0.3 - 0.5 ns		
	10K LEVEL	100K LEVEL	10K LEVEL		100K LEVEL
Power supply	−5.25V ± 5%	−4.5V ± 5%	−5.25V ± 5%		−4.5V ± 5%
Power consumption	2.1 - 2.7 mW	1.8 - 2.3 mW	4.6 - 6.3 mW		4 - 5.5 mW

ACE PACKAGE TYPE AND THERMAL RESISTIVITY SELECTION				
	PACKAGE	THERMAL RESISTIVITY (°C/W)		
		HEAT SINK	NO AIR FLOW	5 m/s AIR FLOW
ACE 600 & ACE 900	64 Pin	Yes	25	13
		No	50	25
ACE 1320, ACE 1400 & ACE 2200	144 Pin	Yes	12	6
		No	24	12

PRODUCT DESCRIPTION

The SCCXXXX gate array family offers the circuit designer the facility to create a semi-custom circuit with a unique set of CAD (Computer-Aided Design) tools in a well-established CMOS process.

Signetics M-Series CMOS Gate Arrays are single chip programmable devices that allow customization of user logic. Only metalization and contact are programmed in these mature CMOS devices. Thus, fast turnaround from logic to completed silicon is achieved.

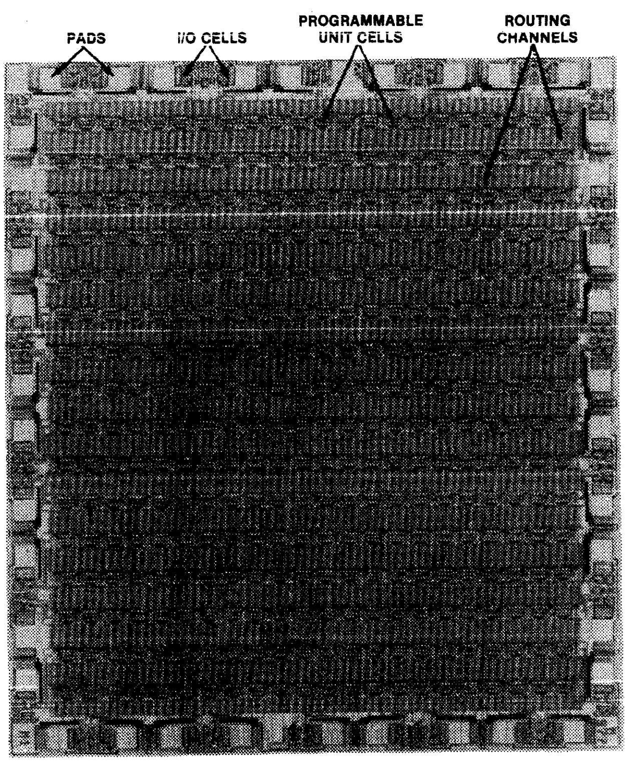
Each device in this family of low power gate arrays contains numerous identical, uncommitted unit cells (Figure 1) which are interconnected by two custom masks (metal and contact). Each unit cell contains four pairs of N and P transistors. Access to the transistors is from both the top and bottom of the cells and, additionally, there are two poly feed-throughs at each side of the cell. This homogenous cell design allows for excellent routing flexibility, and many designs result in better than 80% utilization of the gates available.

The M-Series Gate Arrays are built on a mature, state-of-the-art 4-micron Si-gate CMOS process incorporating an epi-substrate, which significantly reduces the potential for latch as compared with other bulk CMOS processes.

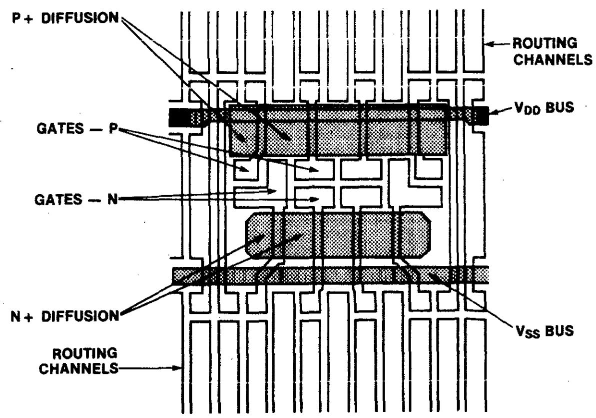
Computer Aided Design (CAD) is used throughout the design process to ensure accurate implementation of customer logic (see Figure 14 for typical process flow).

FEATURES

- **Customer programmable LSI**
- **330 to 1100 gate complexity**
- **Mature silicon gate technology with local oxidation**
- **Library of 60 pre-designed, fully characterized macrocells available**
- **Full CAD, including auto-place and auto-route, for quick error-free design**
- **Very low power consumption (e.g. standby power for SCC 0700 is 0.25mW)**
- **Excellent noise immunity**
- **Power supply range 3 to 15V**
- **Over 80% utilization typical**
- **Fully programmable I/O pins, each having a wide range of functions**
- **Input protection by series resistor and diode clamp to V_{SS}**
- **TTL outputs (buffers) drive up to four LSTTL loads**
- **-55°C to +125°C operating temperature**
- **Plastic and ceramic DIP, ceramic leadless chip carriers, and plastic leaded chip carriers available**



a. SCC0700 CMOS Gate Array



b. Uncommitted Unit Cell

	SCC0330	SCC0450	SCC0700	SCC1100
Gate equivalents (2-input)	330	448	704	1116
Unit cells	165	224	352	558
Rows	11	14	16	18
Unit cells per row	15	16	22	31
Pins (max.)	40	28	40	68
I/O stages (max.)	38	26	38	66
I/O options: 3-state I/O (max.)	34	26	38	66
Direct or inverted inputs (max.)	38	26	38	66
Drivers (max.)	38	14	22	66
Buffers (max.)	34	12	16	66
Schmitt Triggers (max.)	34	8	10	66
Pin pull-up/pull-down resistors (max.)	34	26	34	66

c. Product Matrix

Figure 1. Internal Configuration and Functional Characteristics of M-Series CMOS Gate Arrays

DC ELECTRICAL CHARACTERISTICS (Continued) V_{SS} = 0V; for all devices unless otherwise specified.

Parameter	Operating Temp (T_{amb})[1]	Supply Voltage	Conditions	Temperature Range[1] T_{amb} = Low Min	T_{amb} = Low Max	T_{amb} = 25°C Min	T_{amb} = 25°C Max	T_{amb} = High Min	T_{amb} = High Max	Unit
I_{OL} Output (sink) current Low driver outputs	Standard	5		1.1	—	0.9	—	0.7	—	
		10		4.0	—	3.3	—	2.6	—	
		15		12.0	—	10.0	—	8.0	—	
	Extended	5	V_I = 0V or 5V; V_O = 0.4V	1.2	—	0.9	—	0.6	—	
		10		4.2	—	3.3	—	2.2	—	
		15	V_I = 0V or 10V; V_O = 0.5V	13.0	—	10.0	—	6.7	—	
I_{OL} Output (sink) current Low buffer outputs	Standard	5		2.2	—	1.8	—	1.4	—	
		10	V_I = 0V or 15V; V_O = 1.5V	8.0	—	6.6	—	5.6	—	
		15		24.0	—	20.0	—	16.0	—	mA
	Extended	5		2.4	—	1.8	—	1.2	—	
		10		8.4	—	6.6	—	4.4	—	
		15		26.0	—	20.0	—	13.4	—	
$-I_{OH}$ Output (source) current High	Standard	5	V_I = 0V or 5V; V_O = 4.6V	1.1	—	0.9	—	0.7	—	
		10		3.1	—	2.6	—	2.0	—	
		15	V_I = 0V or 10V; V_O = 9.5V	12.0	—	10.0	—	8.0	—	
	Extended	5		1.2	—	0.9	—	0.6	—	
		10	V_I = 0V or 15V; V_O = 13.5V	3.5		2.6		1.7		
		15		13.0	—	10.0	—	6.7	—	
$\pm I_{IN}$ Input leakage current	Standard	10	V_I = 0V or 10V	—	0.3	—	0.3	—	1.0	
		15		—	0.3	—	0.3	—	1.0	
	Extended	10	V_I = 0V or 15V	—	0.1	—	0.1	—	1.0	
		15		—	0.1	—	0.1	—	1.0	
I_{OZH} Three-state output and open N-channel output leakage current High	Standard	10	Output returned to V_{DD}	—	1.6	—	1.6	—	12.0	
		15		—	1.6	—	1.6	—	12.0	µA
	Extended	10		—	0.4	—	0.4	—	5.0	
		15		—	0.4	—	0.4	—	5.0	
$-I_{OZL}$ Three-state output and open P-channel output leakage current Low	Standard	10	Output returned to V_{SS}	—	1.6	—	1.6	—	12.0	
		15		—	1.6	—	1.6	—	12.0	
	Extended	10		—	0.4	—	0.4	—	5.0	
		15		—	0.4	—	0.4	—	5.0	
V_{TH} Upper threshold voltage	Standard	5	Internal Schmitt trigger	—	—	3.4		—	—	
		10		—	—	6.8	Typical values	—	—	
		15		—	—	10.2		—	—	
V_{TL} Lower threshold voltage		5		—	—	2.2		—	—	
		10		—	—	3.0	Typical values	—	—	V
		15		—	—	3.8		—	—	
V_H Hysteresis voltage input: INPS	—	5	—	—	—	0.2		—	—	
		10		—	—	0.6	Typical values	—	—	
		15		—	—	0.8		—	—	

NOTES:
1. T_{amb} Low: −40°C for standard temperature range; −55°C for extended temperature range. T_{amb} High: +85°C for standard temperature range; +125°C for extended temperature range
2. Pin-connected pull-up and pull-down resistors are typically 7 to 78 K-ohms — see PERIPHERY.
3. When pull-up or pull-down resistors are used, current limits for I_{DD} must be extrapolated.

Signetics

CUSTOM/SEMICUSTOM

DC CHARACTERISTICS (Continued)

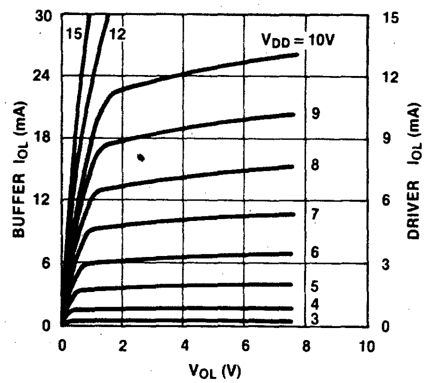


Figure 2. Minimum Output Current LOW as a Function of the Output Voltage LOW; Buffer and Driver Outputs

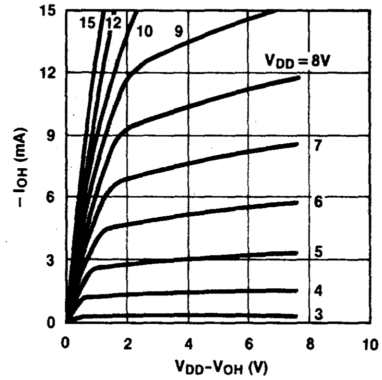


Figure 3. Minimum Output Current HIGH as a Function of the Supply Voltage Minus the Output Voltage HIGH

AC ELECTRICAL CHARACTERISTICS V_{SS} = 0V; T_{amb} = 25°C

	Parameter	Pwr Sup (V_{DD})	Min	Typ	Max	Unit
f_{max}	Maximum toggle frequency flip-flop GT00 (no set/reset)	5	6	12	—	MHz
		10	12	24	—	MHz
		15	15	30	—	MHz
f_s	Maximum system frequency (may depend on number of gates in sequence)	5	3	6	—	MHz
		10	6	12	—	MHz
		15	9	18	—	MHz
t_p	Propagation delays for 2-input NAND gate with fanout of 2	5	—	8	16	ns
		10	—	3.2	6.4	ns
		15	—	2	4	ns

	Paramter	Pwr Sup (V_{DD})	Min	Typ	Max	Unit
	OUTPUT STAGE TRANSITION TIMES: Input transition ≤ 20ns, C_L = 50pF; V_{SS} = 0V, T_{amb} = 25°C					
t_{THL}	Driver outputs High-to-Low	5		60	120	ns
		10		30	60	ns
		15		20	40	ns
t_{THL}	Buffer outputs High-to-Low	5		30	60	ns
		10		15	30	ns
		15		10	20	ns
t_{TLH}	Buffer outputs Low-to-High	5		40	80	ns
		10		18	36	ns
		15		12	24	ns

GATE DELAYS

Nominal Propagation Delay

In Figures 6 through 12, examples are given of the nominal propagation delay times of several library cells, these being calculated from the delay figures given in the individual macro descriptions. These graphs are intended to provide quick-reference data to enable the designer to make an estimate of critical a.c. path without having built or simulated a network.

Accurate delay figures can only be obtained after incorporating the wiring length load automatically calculated by INGATE (i.e., the result of the automatic routing program). A maximum delay is obtained by multiplying the nominal value by 2.2.

ABSOLUTE MAXIMUM RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	-0.5 to $+18V$
Voltage on any input when pin pull up/down resistors are: Used Not used	 V_I V_I	 -0.5 to $V_{DD}+0.5V$ -0.5 to $+18V$
DC current into any input or output	±1	Max. 10mA
Power dissipation per output	P	Max. 100mW
Power dissipation per package For standard temperature range: $-40°C$ to $+85°C$ (plastic and ceramic DIP) For $T_{amb} = -40°C$ to $+60°C$ For $T_{amb} = +60°C$ to $+85°C$	 P_{tot} P_{tot}	 Max. 400mW Derate linearly by 8mW/K to 200mW
For extended temperature range: $-55°C$ to $+125°C$ (ceramic DIP) For $T_{amb} = -55°C$ to $+100°C$ For $T_{amb} = +100°C$ to $+125°C$	 P_{tot} P_{tot}	 Max. 400mW Derate linearly by 8mW/K to 200mW
Storage temperature range	T_{stg}	$-65°C$ to $+150°C$

DC ELECTRICAL CHARACTERISTICS $V_{SS}=0V$; for all devices unless otherwise specified.

Parameter	Operating Temp (T_{amb})[1]	Supply Voltage	Conditions	Temperature Range[1]						Unit
				T_{amb} = Low		T_{amb} = 25°C		T_{amb} = High		
				Min	Max	Min	Max	Min	Max	
I_{DD} Quiescent device current	Standard	5	All valid input combinations; $V_I = V_{SS}$ or V_{DD}	—	50	—	50	—	375	μA
		10		—	100	—	100	—	750	
		15		—	200	—	200	—	1500	
	Extended	5		—	15	—	15	—	375	
		10		—	25	—	25	—	750	
		15		—	50	—	50	—	1500	
V_{OL} Output voltage Low	Both standard and extended ranges	5	$V_I = V_{SS}$ or V_{DD}; $I_O < 1.0\mu A$	—	0.05	—	0.05	—	0.05	V
		10		—	0.05	—	0.05	—	0.05	
		15		—	0.05	—	0.05	—	0.05	
V_{OH} Output voltage High		5		4.95	—	4.95	—	4.95	—	
		10		9.95	—	9.95	—	9.95	—	
		15		14.95	—	14.95	—	14.95	—	
V_{IL} Input voltage Low: INPI/INPB	Both standard and extended ranges	5	$V_O = 0.5V$ or $4.5V$; $I_O < 1.0\mu A$	—	1.5	—	1.5	—	1.5	
		10		—	3.0	—	3.0	—	3.0	
		15	$V_O = 1.0V$ or $9.0V$; $I_O < 1.0\mu A$	—	4.0	—	4.0	—	4.0	
V_{IH} Input voltage High: INPI/INPB		5		3.5	—	3.5	—	3.5	—	
		10	$V_O = 1.5V$ or $13.5V$; $I_O < 1.0\mu A$	7.0	—	7.0	—	7.0	—	
		15		11.0	—	11.0	—	11.0	—	
V_{IL} Input voltage Low: INPA, INPD, INPS	Both standard and extended ranges	5	$V_O = 0.5V$ or $4.5V$; $I_O < 1.0\mu A$	—	1.0	—	1.0	—	1.0	
		10		—	2.0	—	2.0	—	2.0	
		15	$V_O = 1.0V$ or $9.0V$; $I_O < 1.0\mu A$	—	2.5	—	2.5	—	2.5	
V_{IH} Input voltage High: INPA, INPD, INPS		5		4.0	—	4.0	—	4.0	—	
		10	$V_O = 1.5V$ or $13.5V$; $I_O < 1.0\mu A$	8.0	—	8.0	—	8.0	—	
		15		12.5	—	12.5	—	12.5	—	

CMOS GATE ARRAYS (H-Series)

Preliminary

PRODUCT DESCRIPTION

The SCCXXXX gate array family offers the circuit designer the facility to create a semi-custom circuit with a unique set of CAD (Computer-Aided Design) tools in a well-established CMOS process.

Signetics H-Series CMOS Gate Arrays are single chip programmable devices that allow customization of user logic. Only metalization and contact are programmed in these mature CMOS devices. Thus, fast turnaround from logic to completed silicon is achieved.

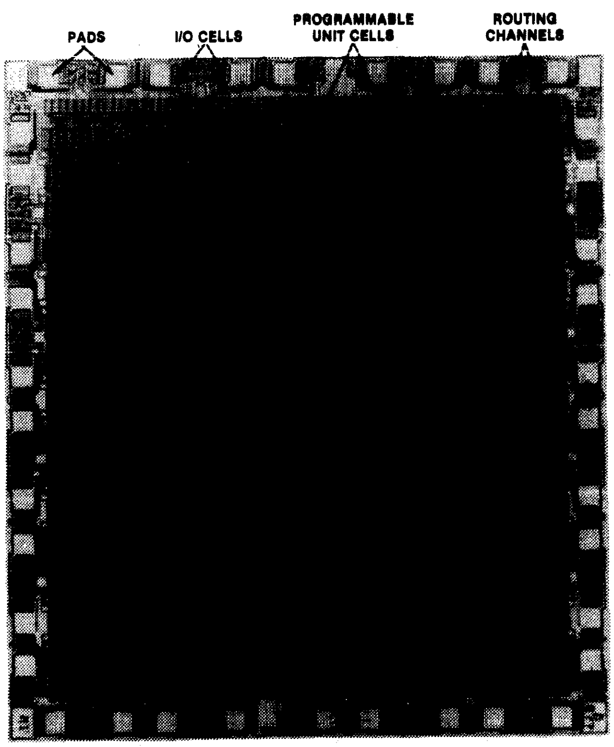
Each device in this family of low power gate arrays contains numerous identical, uncommitted unit cells (Figure 1) which are interconnected by two custom masks (metal and contact). Each unit cell contains four pairs of N and P transistors. Access to the transistors is from both the top and bottom of the cells and, additionally, there are two poly feed-throughs at each side of the cell. This homogenous cell design allows for excellent routing flexibility, and many designs result in better than 80% utilization of the gates available.

The H-Series Gate Arrays are built on a mature, state-of-the-art 3-micron Si-gate CMOS process incorporating an epi-substrate, which significantly reduces the potential for latch as compared with other bulk CMOS processes.

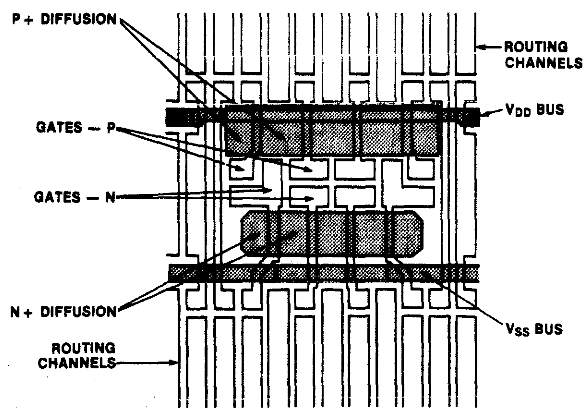
Computer Aided Design (CAD) is used throughout the design process to ensure accurate implementation of customer logic (see Figure 14 for typical process flow).

FEATURES

- **Customer programmable LSI**
- **330 to 1100 gate complexity**
- **Mature silicon gate technology with local oxidation**
- **Library of 60 pre-designed, fully characterized macrocells available**
- **Full CAD, including auto-place and auto-route, for quick error-free design**
- **Very low power consumption (e.g. standby power for SCC 0705 is 0.25mW)**
- **Excellent noise immunity**
- **Power supply range 3 to 6V**
- **Over 80% utilization typical**
- **Fully programmable I/O pins, each having a wide range of functions**
- **Input protection by series resistor and diode clamp to V_{SS}**
- **TTL outputs (buffers) drive up to four LSTTL loads**
- **−55°C to +125°C operating temperature**
- **Plastic and ceramic DIP, ceramic leadless chip carriers, and plastic leaded chip carriers available**



a. SCC0705 CMOS Gate Array



b. Uncommitted Unit Cell

	SCC0335	SCC0455	SCC0705	SCC1105
Gate equivalents (2-input)	33	448	704	1116
Unit cells	165	224	352	558
Rows	11	14	16	18
Unit cells per row	15	16	22	31
Pins (max.)	40	28	40	68
I/O stages (max.)	38	26	38	66
I/O options: 3-state I/O (max.)	34	26	38	66
Direct or inverted inputs (max.)	38	26	38	66
Drivers (max.)	38	14	22	66
Buffers (max.)	34	12	16	66
Schmitt Triggers (max.)	34	8	10	66
Pin pull-up/pull-down resistors (max.)	34	26	34	66

c. Product Matrix

Figure 1. Internal Configuration and Functional Characteristics of H-Series CMOS Gate Arrays

CMOS GATE ARRAYS (H-Series)

SCC0335-H, SCC0455-H
SCC0705-H, SCC1105-H

Preliminary

ABSOLUTE MAXIMUM RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	-0.5 to $+7$V
Voltage on any input when pin pull up/down resistors are:		
Used	V_I	-0.5 to $V_{DD}+0.5$V
Not used	V_I	-0.5 to $+7$V
DC current into any input or output	$\pm$ 1	Max. 10mA
Power dissipation per output	P	Max. 100mW
Power dissipation per package		
For standard temperature range: -40°C to $+85$°C (plastic and ceramic DIP)		
For $T_{amb} = -40$°C to $+60$°C	P_{tot}	Max. 400mW
For $T_{amb} = +60$°C to $+85$°C	P_{tot}	Derate linearly by 8mW/K to 200mW
For extended temperature range: -55°C to $+125$°C (ceramic DIP)		
For $T_{amb} = -55$°C to $+100$°C	P_{tot}	Max. 400mW
For $T_{amb} = +100$°C to $+125$°C	P_{tot}	Derate linearly by 8mW/K to 200mW
Storage temperature range	T_{stg}	-65°C to $+150$°C

DC ELECTRICAL CHARACTERISTICS $V_{SS}=0$V; for all devices unless otherwise specified.

SYMBOL AND PARAMETER	OPERATING TEMP (T_{amb})[1]	SUPPLY VOLTAGE	TEST CONDITIONS	TEMPERATURE RANGE[1] T_{amb} = LOW		T_{amb} = 25°C		T_{amb} = HIGH		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
I_{DD} Quiescent device current	Standard	5	$I_O=0$ V_{CC} or GND	—	50	—	50	—	375	μA
		—		—	—	—	—	—	—	
		—		—	—	—	—	—	—	
	Extended	5		—	15	—	15	—	375	
		—		—	—	—	—	—	—	
		—		—	—	—	—	—	—	
V_{OL} Output voltage Low	Both standard and extended ranges	2.0	V_{IH} or V_{IL} $I_O=20\mu A$	—	0.1	—	0.1	—	0.1	V
		4.5		—	0.1	—	0.1	—	0.1	
		6.0		—	0.1	—	0.1	—	0.1	
V_{OH} Output voltage High		2.0		1.9	—	1.9	—	1.9	—	
		4.5		4.4	—	4.4	—	4.4	—	
		6.0		5.9	—	5.9	—	5.9	—	
V_{IL} Input voltage Low: INPI/INPB	Both standard and extended ranges	2.0	—	—	0.4	—	0.4	—	0.4	
		4.5		—	0.9	—	0.9	—	0.9	
		6.0		—	1.2	—	1.2	—	1.2	
V_{IH} Input voltage High: INPI/INPB		2.0		1.4	—	1.4	—	1.4	—	
		4.5		3.15	—	3.15	—	3.15	—	
		6.0		4.2	—	4.2	—	4.2	—	
V_{IL} Input voltage Low: INPA, INPD, INPS	Both standard and extended ranges	2.0	—	—	0.3	—	0.3	—	0.3	
		4.5		—	0.7	—	0.7	—	0.7	
		6.0		—	0.9	—	0.9	—	0.9	
V_{IH} Input voltage High: INPA, INPD, INPS		2.0		1.7	—	1.7	—	1.7	—	
		4.5		3.6	—	3.6	—	3.6	—	
		6.0		4.8	—	4.8	—	4.8	—	

Preliminary

DC ELECTRICAL CHARACTERISTICS (Continued) $V_{SS} = 0V$; for all devices unless otherwise specified.

SYMBOL AND PARAMETER	OPERATING TEMP (T_{amb})[1]	SUPPLY VOLTAGE	TEST CONDITIONS	TEMPERATURE RANGE[1] T_{amb} = LOW MIN	T_{amb} = LOW MAX	T_{amb} = 25°C MIN	T_{amb} = 25°C MAX	T_{amb} = HIGH MIN	T_{amb} = HIGH MAX	UNIT
I_{OL} Output (sink) current Low driver outputs	Standard	4.5	$V_I = 0$ or 5V, $V_{OL} = 0.26V$ (Std.), $V_{OL} = 0.33V$ (Std.), $V_{OL} = 0.4V$ (Ext.)	1.6	—	1.6	—	1.6	—	mA
		6.0		2.1	—	2.1	—	2.1	—	
		—		—	—	—	—	—	—	
	Extended	4.5		1.6	—	1.6	—	1.6	—	
		6.0		2.1	—	2.1	—	2.1	—	
		—		—	—	—	—	—	—	
I_{OL} Output (sink) current Low buffer outputs	Standard	4.5		3.2	—	3.2	—	3.2	—	
		6.0		4.2	—	4.2	—	4.2	—	
		—		—	—	—	—	—	—	
	Extended	4.5		3.2	—	3.2	—	3.2	—	
		6.0		4.2	—	4.2	—	4.2	—	
		—		—	—	—	—	—	—	
$-I_{OH}$ Output (source) current High	Standard	4.5	$V_I = 0V$ or 5V, $V_{OH} = 3.24V$, $V_{OH} = 5.34V$	2.5	—	2.5	—	2.5	—	
		6.0		3.1	—	3.1	—	3.1	—	
		—		—	—	—	—	—	—	
	Extended	4.5	$V_{OH} = 3.7V$, $V_{OH} = 5.2V$	2.5	—	2.5	—	2.5	—	
		6.0		3.1	—	3.1	—	3.1	—	
		—		—	—	—	—	—	—	
$\pm I_{IN}$ Input leakage current	Standard	6.0	V_{CC} or GND	—	—	—	0.1	—	1.0	µA
		—		—	—	—	—	—	—	
	Extended	6.0		—	—	—	0.1	—	1.0	
		—		—	—	—		—	—	
$\pm I_{OZ}$ Three-state output and open N-channel output leakage current High	Standard	5.5	$V_O = V_{CC}$ or GND	—	—	—	0.5	—	5.0	
		—		—	—	—		—	—	
	Extended	5.5		—	—	—	0.5	—	10.0	
		—		—	—	—	—	—	—	
V_{TH} Upper threshold voltage	Standard	2.0	Internal Schmitt trigger	—	—	TBD	Typical values	—	—	V
		4.5		—	—	TBD		—	—	
		6.0		—	—	TBD		—	—	
V_{TL} Lower threshold voltage		2.0		—	—	TBD	Typical values	—	—	
		4.5		—	—	TBD		—	—	
		6.0		—	—	TBD		—	—	
V_H Hysteresis voltage input: INPS	—	2.0	—	—	—	TBD	Typical values	—	—	
		4.5		—	—	TBD		—	—	
		6.0		—	—	TBD		—	—	

NOTES:
1. T_{amb} Low: −40°C for standard temperature range; −55°C for extended temperature range. T_{amb} High: +85°C for standard temperature range; +125°C for extended temperature range
2. Pin-connected pull-up and pull-down resistors are typically 7 to 78 K-ohms — see PERIPHERY.
3. When pull-up or pull-down resistors are used, current limits for I_{DD} must be extrapolated.

Preliminary

AC ELECTRICAL CHARACTERISTICS $V_{SS} = 0V$; $T_{amb} = 25°C$

SYMBOL AND PARAMETER		PWR SUP (V_{DD})	MIN	TYP	MAX	UNIT
f_{max}	Maximum toggle frequency flip-flop GT00 (no set/reset)	5	—	30	—	MHz
f_s	Maximum system frequency (may depend on number of gates in sequence)	5	—	12	—	MHz
t_p	Propagation delays for 2-input NAND gate with fanout of 2	5	—	3.5	—	ns

SYMBOL AND PARAMETER		PWR SUP (V_{DD})	MIN	TYP	MAX	UNIT
OUTPUT STAGE TRANSITION TIMES: Input transition ≤ 20ns, $C_L = 50pF$; $V_{SS} = 0V$, $T_{amb} = 25°C$.						
t_{THL}	Driver outputs High-to-Low	2.0	—	130	260	ns
		4.5	—	26	52	ns
		6.0	—	22	44	ns
t_{THL}	Buffer outputs High-to-Low	2.0	—	65	130	ns
		4.5	—	13	26	ns
		6.0	—	11	22	ns
t_{TLH}	Buffer outputs Low-to-High	2.0	—	125	250	ns
		4.5	—	25	50	ns
		6.0	—	21	43	ns

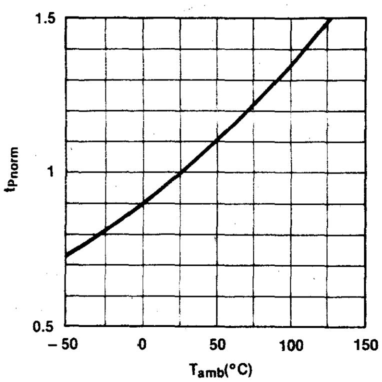


Figure 2. Normalized propagation delay (t_{Pnorm}) as a function of the ambient temperature.

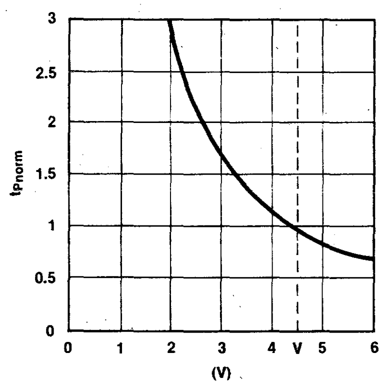


Figure 3. Normalized propagation delay (t_{Pnorm}) as a function of the supply voltage.

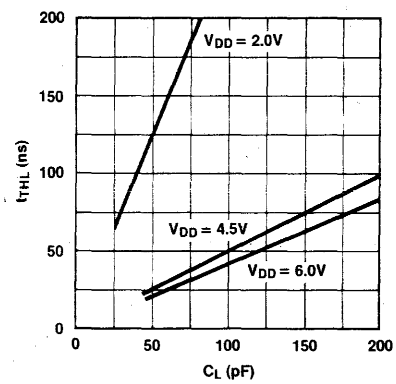


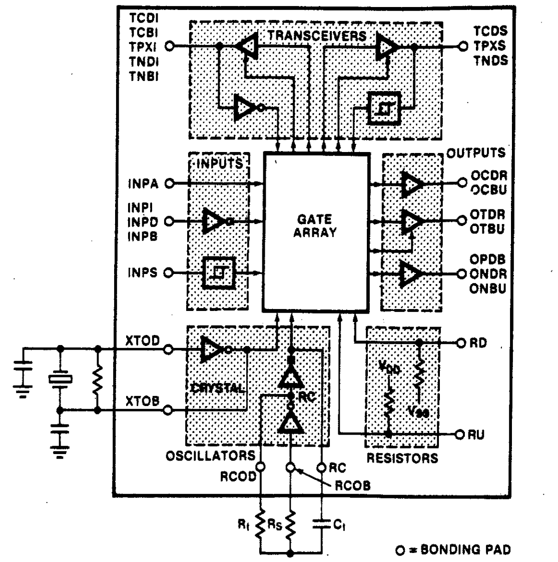
Fig. 4 Output transition time (LOW-to-HIGH) as a function of the load capacitance for driver and buffer outputs.

Preliminary

PERIPHERY

To provide a versatile interface, H-Series CMOS arrays have numerous I/O pads—see Figure 1a. These peripheral elements can be configured to match the input or output requirements of a wide variety of logic families. Accordingly, a bonding pad may have one of the following functions assigned to it:

- INPUT STAGE which includes an input protection circuit (series resistor and single diode clamp to V_{SS}). The recommended maximum load is 260 array gates, or 100 array gates for optimum speed performance. Because the input voltage is not clamped to V_{DD}, input voltages greater than the supply voltage is possible, thus allowing voltage level shifting.
- SCHMITT TRIGGER input stage for noise reduction, pulse shaping, or suppression of oscillation spikes associated with slow input clock transitions. The recommended maximum load is 10 array gates, or 5 for optimum speed performance.
- TRANSCEIVER input/output stage
- THREE-STATE output with driver or buffer performance capability for bussing applications
- COMPLEMENTARY OUTPUT with driver or buffer performance capability.
- OPEN DRAIN N- or P-transistor output
- PULL-UP/PULL-DOWN resistors (see Figure 2 for availability) may be added at various I/O stages. The values available are 5, 10, 15, 30, 60, 65, 70 and 75 Kohms.



TRANSCEIVERS WITH INVERTER INPUT	
TCDI	complementary driver output
TCBI	complementary buffer output
TPXI	open drain p-channel driver output
TNDI	open drain n-channel driver output
TNBI	open drain n-channel buffer output
TRANSCEIVER WITH SCHMITT TRIGGER INPUT	
TCDS	complementary driver output
TPXS	open drain p-channel driver output
TNDS	open drain n-channel driver output
INPUTS	
INPA	direct access to array
INPI	inverter
INPD	driver
INPB	buffer
INPS	Schmitt trigger
OUTPUTS	***FANOUT: DRIVER = 4 LSTTL LOADS @ 4.5V BUFFER = 6 LSTTL LOADS @ 4.5V***
OCDR	complementary driver
OCBU	complementary buffer
OTDR	3-state driver
OTBU	3-state buffer
OPDB	open drain p-channel driver
ONDR	open drain n-channel driver
ONBU	open drain n-channel buffer
OSCILLATORS	
XTOD	crystal oscillator with driver stage
XTOB	crystal oscillator with buffer stage
RCOD	RC oscillator with driver stage
RCOB	RC oscillator with buffer stage
RESISTORS	
RD	pull-down resistors
RU	pull-up resistors

Figure 13. The SCCXXXX I/O Cell Library

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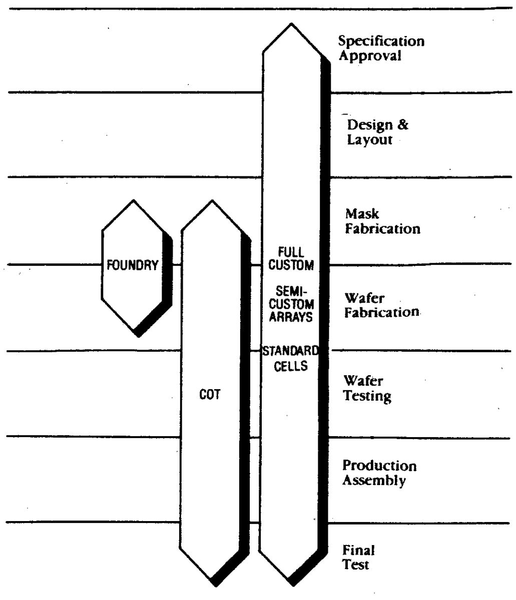

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SCA-6 AND SCA-12 SWITCHED CAPACITOR CUSTOM ARRAYS

The SCA-6 and SCA-12 are CMOS, switched-capacitor filter semicustom arrays, which can be configured to implement up to six or twelve biquadratic filter sections, other switched capacitor filter (SCF) architectures, and general analog functions. Intended primarily for analog signal processing applications, the SCA-6 and SCA-12 are efficient replacements for many active RC and discrete implementations, providing precision high-order filtering on a single chip.

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SSi Quality Assurance Capabilities include:

- Environmental testing
- Burn-in
- Hi-Rel screening

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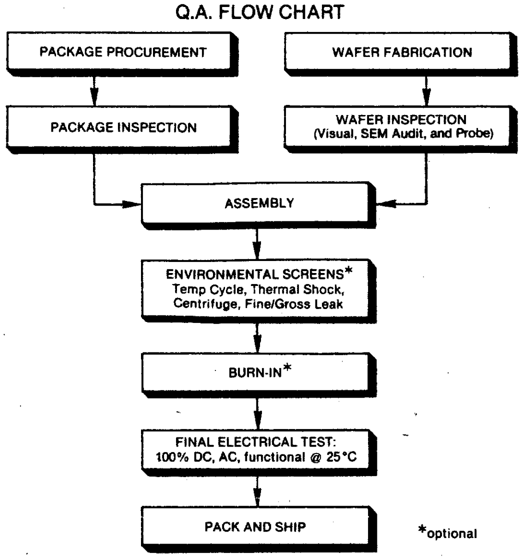
Q.A. FLOW CHART



*optional

Hi-Rel Screening Options
• Reliability Screening (Method 5004)
• Qualification and Quality Conformance Procedure (Method 5005)
• Pre-Seal Visual Inspection (Method 2010)
• Stabilization Bake (Method 1008)
• Temperature Cycle (Method 1010)
• Thermal Shock
• Constant Acceleration
• Fine Leak (Method 1014)
• Gross Leak (Method 1014)
• Burn-in
• SEM Analysis of Wafer Lots (Metallization)

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Why Go Custom and Why Use Synertek?

Your decision to use a Custom circuit rests basically on the requirements of your system. You'll want to consider the alternatives available to you:

- **Standard circuits** are off-the-shelf products designed for general product applications. If your yearly system volume will be less than 10,000, SSI (small scale integration) and MSI (medium scale integration) circuits may be your best solution.
- **Microprocessors** may fill your need if your application requires great flexibility and cost is not an overriding factor. They are most practical when total circuit volume does not exceed 50,000.

Advantages of Custom Circuits

A Custom circuit is an exclusive proprietary design built specifically to meet your product requirements. Its advantages are:

- **Reduced system cost** — Through circuit integration the total number of discrete and integrated components can be cut by 75-90%. This dramatically reduces component inventory, PC board assembly, and power supply costs.
- **Increased reliability** — As circuit device count and total system size is reduced, system reliability increases. For you, the more reliable a system you sell to your customers, the less you will have to expend on warranty costs.
- **Features** — Special features not available in standard circuits or microprocessors can be cost-effectively designed into a Custom circuit.
- **Market Leadership** — CUSTOM MOS/LSI technology can revolutionize a product. It enables new features to be built which would otherwise be unavailable or too expensive to implement. When your product is manufactured with a proprietary design, competitors have a more difficult time copying it. As a result, you can enjoy longer periods of market leadership and penetration.

Why Use Synertek?

Our ability to develop sophisticated technologies insures our market leadership position in custom integrated circuits. We currently offer silicon gate HMOS, NMOS, and HCMOS technologies. Our advanced computer-aided design facilities, projection alignment equipment, 4-inch wafer fabrication lines, and VLSI testing equipment further demonstrate Synertek's commitment to state-of-the-art technology. Synertek offers the following services:

- **Classic Custom Designs** — We will design your circuit from concept. You may initially provide us with a written explanation of the function you want, or with a logic diagram of the circuit, or with just a specification.
- **Customer Design Teams (C.D.T.)** — We will train your engineers to do their own custom design. The full spectrum of design capability can be approached: classic custom hand-drawn circuits, designs using the Cell Library™, or seminars for C.O.T.™ customers. Your systems knowledge is combined with our IC design capability for optimum circuits.
- **C.O.T.™** — Synertek will become the manufacturing arm of your in-house design group or your consulting design house. By providing you with process design rules, parameters, computer simulation programs and, most of all, our total cooperation, we can assure you the manufacturing capability you want.

Classic Custom Design

A masterpiece is never developed overnight. An artist needs time to think, plan, and create. At Synertek, the average length of time needed to bring a circuit from the concept stage to prototype production is 6-9 months. Depending on the complexity of the device, this may be longer or shorter. Simple circuits can be completed within 3-4 months. All circuits, however, are subjected to the same stringent testing, quality control, and verification checks.

Keeping with our philosophy of partnership, our engineers will confer with you often throughout the design and development phases.

The Custom Design and Development Process

- **System definition** — Synertek and the customer establish block diagrams, flow charts, and mechanical and electrical specifications
- **Logic design and computer simulation** — Our design engineers convert system functions to MOS logic. Computer simulations of critical logic design characteristics are done in our DA (design automation) center. SCEPT™ (Synertek Circuit Emulation Program and Test) is a conventionally designed breadboard which duplicates MOS logic. Once approved by you, SCEPT™ is used to write and debug a test program. From this point, SCEPT™ is the functional reference for the remaining design steps. **1-10 weeks.**
- **Circuit design and analysis** — Individual transistors are laid out to implement the SCEPT™ logic. Particular attention is paid to critical speed paths. Additional computer-aided circuit simulation information is analyzed and incorporated into the actual circuit design. **1-4 weeks.**
- **Composite layout design** — A layout of the circuit design, called a composite, is hand drawn to minimize final chip size.
- **Digitizing** — The composite drawing is converted in our CAD (Computer Aided Design) center to a database tape using a Calma interactive graphic system. The digitized information is used to generate plots of each circuit layer. The plots are compared to the original composite and editing changes are made. Editing and checking continues until the database tape is approved for the entire composite.**1-14 weeks.**
- **Mask generation** — Once the database tape is approved a PG (pattern generation) tape is produced. This tape is used to create each mask level.

  We use three methods in mask making — photolithography, E-beam and a combination of both.
- **Prototype wafer fabrication** — During prototype fabrication, numerous quality and electrical inspections are performed to assure that every wafer lot meets our specifications.
- **First samples** — These are untested devices commonly referred to as "Cut & Go's." They are placed in ceramic packages, assembled, and sent to you for initial evaluation. **2-3 weeks.**
- **Test generation** — The Cut & Go's play an essential role in the completion of the test program, which was initiated during the circuit design stage. The test program must be verified with the Cut & Go's before it is finalized.
- **Prototype production** — After fully tested samples are approved, prototype production begins.
- **Full production** — Scheduled delivery commences after prototype qualification and test verification are completed.

Customer Design Teams (C.D.T.)

C.D.T. is a program by which customers can be trained to do their own IC designs. It encompasses the full spectrum of custom design from the classical, hand-drawn approach, with Synertek's engineers doing the full design, to the customer owned tooling program. CDT's are designed to take advantage of the customer's system knowledge and Synertek's IC design and production capabilities. The customer has access to our facilities, design courses, the Cell Library™, advanced CAD tools, processes, design expertise, and on-going support.

The CDT design course is approximately ten weeks long and is based upon the structured design methodology. The major portion of the course demonstrates how to use the Cell Library™, with hands-on experience using our CAD tools to complete a simple design. Very little time is spent on design physics. As an on-going project we are continually developing additional short courses as updates as well as video tapes on specific topics.

Our CAD tools revolve around our mainframe computer, a VAX 11/780, to enable our customers to use commercially available software written for the VAX. NCA corporation's software is used for layout verification, including Design Rule Check, Electrical Rule Check and Network Continuity Check. The Network Continuity Check compares the layout data to the Netlist derived from schematic entry. Other services, such as sizing and PG tape generation, can also be performed on the VAX.

Silvar-Lisco's SOS package including CASS and CAL-MP is installed on the VAX. CASS is used for schematic entry via a Genisco 1000 or other graphics terminals. Once the schematic has been entered, a design data base is created from which several output data formats can be generated. The following outputs are presently available: Netlist, TEGAS for logic generation and test verification, SPICE for circuit simulation, Network Continuity Checker and CAL-MP.

CAL-MP is used for automatic placement and routing of the cells in the Cell Library™. All cells are designed to take advantage of the CAL-MP program capability. The program can handle up to 1800 cells (not gates) with 3600 cell capability to be installed soon. Chips of larger size can be created by assemblying partitioned sections of up to 3600 cells each.

We are constantly updating and improving our software. Any improvements in the NCA or Silvar-Lisco software will be installed so that design capability and turn-around times can constantly be improved. Dial-up facilities to the VAX are available enabling our CDT customers to access the above software via remote terminals.

As an important part of the CDT program Synertek provides support in the form of helping with the design, instruction in the use of our CAD equipment, providing updates in the course, and providing advancements in our process capabilities. Synertek's CDT team is organized to assist the customer in all the crucial steps of the design. Once the customer reaches design proficiency, we have a separate Customer Owned Tooling (C.O.T.™) team to move designs quickly into production. As a customer's needs or designs change, CDT's are flexible enough to tailor ongoing support to the specific requirements of the customer.

The Cell Library™

The Cell Library™ evolves around our n-well, single poly, single metal 3 micron HCMOS process. The cells developed are the basic cells required to do random logic design. We will continue to design increasingly complex cells, such as multi-stage counters, voltage comparators, microprocessor cores, ALU's, etc. Customers have the option of designing and using any additional cells required in their system. These cells should conform to our format requirements, and the customer has the option of including them in the Cell Library™ user group.

Designs can be done on any graphics system with the interface preferably using GDS II formatted tapes. All cells are fully characterized over the −55°C to +125°C range. Each cell has its own data sheet, with all the electrical and topological parameters. The Cell Library™ manual is a TTL type book containing all the information on the cells.

Almost all cells are of constant height and variable width, however some cells are of different height to improve layout efficiency. For example, there is a tall and narrow flip-flop that will be used for long chains of ripple counters. Some of the basic cells, such as inverters, NOR gates, NAND gates, are of two different heights to optimize the auto-router.

Each cell has inputs at both the top and the bottom with two power lines running horizontally through the cell. The cells are self-contained, so that no external connections will be required to complete them. For most of the cells, connections are made by either poly or metal. Production type cells, such as alignment marks, CD's, etc. are also available as part of the Cell Library™.

The Cell Library™ is available to our classic custom, CDT and C.O.T.™ customers. Synertek's engineers will design a circuit for you or teach your engineers to do their own designs using the Cell Library™. C.O.T.™ customers may purchase the Cell Library™ with or without a production commitment.

Training for C.O.T.™ customers is also available for a nominal fee.

C.O.T.™

Perhaps you have your own MOS design group, or have chosen to have your circuit designed by a consulting firm. Or maybe another MOS supplier designed the chip and you want to tool-up a second-source supplier. Whatever your design source, we can produce your circuit on a customer owned tooling (C.O.T.™) basis.

Because of our extensive experience with MOS/LSI technology, we understand your reasons for going C.O.T.™. You want to minimize design cost and production time while maximizing proprietary design control. We guarantee that your Custom circuit will receive the same confidential, proprietary treatment as our own in-house designed circuits.

You may enter the production cycle at a number of various stages. We'll accept your design on a database tape, a pattern generator tape, or working plate. You'll be given an initial documentation package that includes an overview of design rules and parameters for our MOS processes.

C.O.T.™ customers provide Synertek's Product Engineering with their chosen form of tooling along with the test tape and specifications for testing the customer's circuit.

Synertek maintains a policy of requiring characterization data for all circuits prior to transfer to production. This measure enables Synertek to do further studies on yield enhancements and correlation. Synertek strives to maximize yields at final test and ultimately reduce circuit costs to the customer. We view C.O.T.™ as a joint effort on the part of vendor and customer. Our goal is to work with the customer's design group, to lend the necessary technical support and to build a successful working relationship.

Again, we will meet with you as early in the program as possible to establish a close working relationship. If you wish to design your own proprietary circuit, our engineering staff is available for design aid and general program guidance. We take measures to enhance a smooth product flow. Our program managers monitor your circuit from our CAD center through production. We also have a back-log control system that continually updates you on product schedules and shipments.

As a C.O.T.™ customer, you have access to our extensive manufacturing and assembly facilities in addition to our advanced processes.

A Process for Every Masterpiece

Selecting the right process for your Custom circuit is one of your most important decisions in the design cycle.

Synertek's offering of fully proven manufacturing processes has the right answer for you. It includes state-of-the-art HMOS, HCMOS and EEPROM in addition to the industry standard NMOS silicon gate technology. Electrical and Topological Design Rules are available under a non-disclosure agreement.

A Sample of Synertek's MOS Processes

SILICON GATE NMOS

Process	$FLDI^2$	$ENHI^2$	$DEPI^2$	V_{SB}	V_{TEO}	Volts V_{TDO}	V_{TFO}	V_{VDSS}	Beta A/V^2	Gamma V 1/2	CDA $F/cm^2 \times 10^{-8}$	pN Ω/□	pP Ω/□	X_j	Channel Length μ	Topological Pitch: Poly w/s μ	Diff w/s μ	Al-Al w/s μ	Comments
NDK4	Yes	Yes	Yes	0	+0.2	−3.0	16	10	11	0.25	0.7	15	60	1.5	6	6/6	6/6	6/6	Planox, 2 poly process, switched capacitor techniques for analog circuits
NPM5	Yes	Yes	Yes	0	+0.5 −0.2	−3.0 −1.3	15	7	19	0.26	0.7	27	30	0.45	3 (E & D) 4 (I)	4/5	5/5	5/5	HMOSI. Dual implants for each ENH and DEP transistor (optional)*
NPM6	Yes	Yes	Yes	0	+0.5 −0.0	−3.0 −1.3	15	7 (1.6μ)	29	0.25	0.8	24	27	0.35	2 (0) 3.5 (I)	3/3	3.5/3.5	3.5/3	Planox; single poly. Stepper technology and all dry etch process
NFN5	Yes	Yes	Yes	0	+0.8	−2.8	27	11	17	0.75	0.7	15	65	1.2	5	5/4	5/5	5/5	Planox; E^2PROM process

*Also available with dry etch processing at contact.

SILICON GATE CMOS

Process	Channel	V_{TFO}	V_{TO}	Beta UA/V^2	B_{VDSS}	Gamma	pNopP Ω/□	pPoly Ω/□	Channel Length μ	Topological Pitch: Poly w/s	n-Well w/s	Diff. w/s	Al-Al w/s	Comments
CPN5	P	−16	−0.9	5.5	−19	0.7	50	20	3	3/3.5	3.5/14	3/5	4/5	Single poly, n-well process
	N	+10	+0.9	17	+17	0.5	25	15	3ν	3/3.5		3/5	4/5	Available up to 12 V*
CA72	P	−16	−0.9	5.5	−19	0.7	50	1)20 15	2	2/2.5	2.5/10	2/3.5	3/3.5	Double poly, high voltage
										2/25		2/3.5	3/3.5	
	N	+10	+0.9	17	+17	0.5	25	2)<100 <100	2					

*Also available using stepper technology.

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Telex (857) 121450

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Conseilet Promotion
28 Rue de la Procession
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Tel. 5064275
Telex (842) 614596F

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Manudax-Nederland B.V.
54732G Heeswijk (N.B.)
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Tel. 04139 2901
Telex (844) 50175

HONG KONG
Conmos Products, Ltd.
Haynein Bldg., 11th Floor
1 Tai Yip Street
Keun Tong, Kowloon,
Hong Kong
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INDIA, MALAYSIA, SINGAPORE, THAILAND
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Gruppo Editoriale Jackson S.R.L.
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Astronic GmbH
Winzererstrasse 47d
8000 Munich 40,
West Germany
Tel. (089) 309031
Telex (841) 5216187

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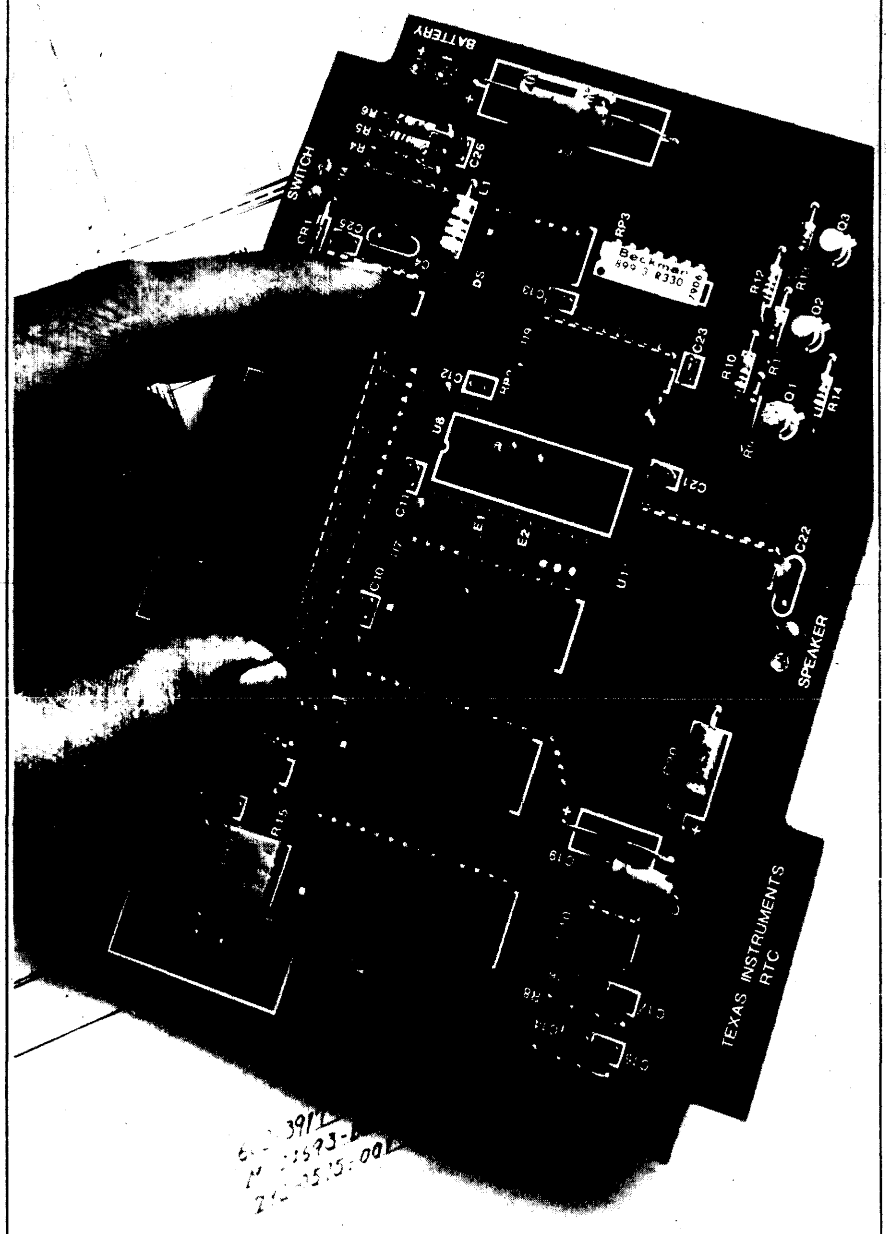
645 Stewart Avenue, Garden City, NY 11530 (516) 222-2500 TWX: 510-222-1673

TI Standard-cell Technology:



Now, you can achieve better performance by matching logic more closely to your design requirements. TI's new 3-µm CMOS standard-cell technology is the fast, simple means by which you can gain the advantages of VLSI custom chips at a price you can afford. TI CMOS standard-cell technology lets you design your own semicustom ICs. Quickly. Economically. And best of all, using familiar design rules and techniques that let you focus on your logic design, rather than on IC design.

Semicustom logic made affordable

A single semicustom chip created with TI's standard-cell technology lets you replace hundreds of discrete TTL components. Allowing you to dramatically reduce your system parts count. Improve reliability. Lower power dissipation. Develop a lighter, more compact product. And decrease assembly costs because of fewer parts and fewer inter-package connections.

What's more, system cost with TI's standard-cell logic is often much less than with discrete logic.

Easy does it

TI's standard-cell system makes developing semicustom logic as easy as arranging packaged logic chips on a PC board. All you do is develop your design using familiar TTL logic functions as your building blocks.

Your schematic can be in the form of a discrete IC breadboard. Or you can draw your schematic on paper, or set it up using an engineering work station. Then, you create a simulation model for your schematic and exercise it to verify performance and define the tests that your chips must pass in production.

◀ **Simple yet advanced,** TI standard-cell technology lets you develop one-chip logic systems using traditional TTL design techniques. Extensive support from TI includes advanced engineering work stations now located at all TI Regional Technology Centers. The reduced cost, size, weight, and power consumption of TI standard-cell chips can benefit products ranging from simple electronic games to logic-intensive systems for advanced computers.

PRODUCT PREVIEW

This page contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

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Semicustom CMOS logic you design using your TTL know-how.

TYPICAL STANDARD-CELL DESIGN

APPLICATION
- FLOPPY-DISK LOGIC DISPLACEMENT—8-BIT MICROPROCESSOR DESIGN WITH ROM AND DRAM INTERFACES
- PRESENT DESIGN—48 LPS AND SCHOTTKY DEVICES
- THIS DESIGN—1-40 PIN 1,550-GATE STANDARD CELL

PERFORMANCE ANALYSIS

IMPACT AREA	LPS DESIGN	STANDARD CELL
PERFORMANCE	LPS	LPS EQUIVALENT OR BETTER
POWER DISSIPATION	1.35 W	50 mW
PC BOARD AREA	40 SQ. INCHES	3 SQ. INCHES
NO. OF SOLDER JOINTS	720	40
COMPONENT COST	X	0.3X

DESIGN DELIVERY TIMING

ACTIVITY	WEEKS	CUM.	COMMENTS
DESIGN IDENTIFIED	0	0	QUOTE, TERMS, AND CONDITIONS
DESIGN SUBMITTED TO RTC	4	4	LPS SCHEMATICS AND TEST DATA
RTC SUBMISSION TO FACTORY	6	10	COMPUTER-GENERATED DATA BASE AND LAYOUT
FACTORY SUPPLIES PROTOTYPES	7	17	20 UNITS TO SPECIFICATION
FIRST PRODUCTION DELIVERY	6	23	HIGH-VOLUME MANUFACTURE

Low logic costs per installed gate combine with quick turnaround times to help bring your system cost down the learning curve faster.

After that, your responsibilities are over. TI handles all the time-consuming details of chip layout, testing, and verification. Turnaround time and costs are kept to a minimum by TI's automated design system.

This approach gives you two key advantages. First, it lets you capitalize on the expertise you've developed over years of using standard logic families like SN54/74LS Low-power Schottky TTL. Second, it gives you the benefit of TI's decades of experience in IC design.

If you prefer, you can do the chip layout yourself. In this case, TI supplies the specifications you need to lay out your design using standard cells.

Wide choice of functions eases design task

Many popular functions equivalent to SN54/74 devices are already available in TI's new SN54/74SC family of standard-cell logic functions. The current family members are 3-µm twin-well CMOS parts based on TI's SN54/74HC family of high-speed CMOS logic functions. The new SN54/74SC family meets or exceeds SN54/74HC specifications and offers the same advantages of low power consumption, high noise immunity, flexible power-supply requirements, and switching speeds comparable to Low-power Schottky performance.

With a 2-picofarad load, the typical propagation delay is 3 ns per gate, with a typical power dissipation of 60 µW per gate at 1 MHz. Electrostatic discharge protection on input and output buffers exceeds 2000 volts. Latchup protection on outputs has been shown to exceed ±300 mA at room temperature.

Many new standard-cell functions are coming soon. Plans include unique "procedural cells" that let you partially define your own on-chip RAM, ROM, ALU, counters, and other functions. Also upcoming is a series of advanced standard-cell functions offering Advanced Low-power Schottky performance levels.

Depending on your design needs, TI standard-cell ICs can be packaged in anything from 8-pin DIPs to multipin chip carriers. And MIL versions will also be available.†

Sized to fit

What's more, standard-cell ICs are sized to meet your specific design requirements. You aren't tied to a specific chip size, as in the case of gate or logic arrays.

†Check field sales office for availability.

Standard-cell functions are also packed much more densely than logic-array functions. That's because the functions are separately selected and placed on chip for each design. In contrast, logic arrays must implement the desired functions using a preset collection of logic elements, such as NOR gates.

TI standard-cell ICs let you avoid the problem of "unused" gates. They also minimize silicon-consuming routing areas needed to interconnect logic arrays.

The result is cost-effective, compact ICs that pack much more functionality in less chip space.

This translates into substantial savings in IC production costs. Savings that make TI standard-cell solutions an attractive choice for low- as well as high-volume products.

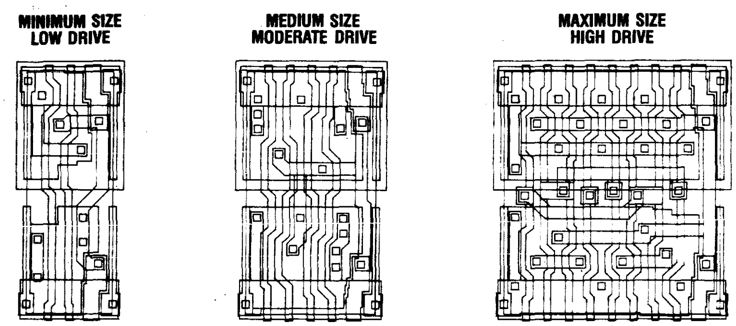
Versatile logic ICs

You can put standard-cell ICs from TI to work in just about any system requiring digital logic. Like printers and terminals. Dedicated controllers. Instrumentation. Automotive controls. Video games, personal computers, and other consumer electronic products.

Standard-cell ICs from TI provide the affordable logic you need to build better man-to-machine and machine-to-machine interfaces into your products. For "friendlier" computers and "smarter" office systems.

The modest power, size, and weight requirements of TI's CMOS standard-cell chips are also ideal for battery-powered and portable equipment.

TYPICAL CELLS



Each function in the SN54/74SC family has a number of physical implementations, allowing TI to better optimize your circuit design.

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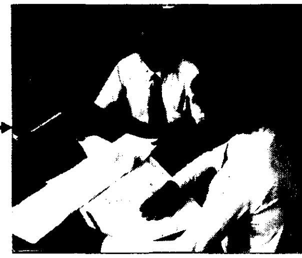
Simple design system with quick

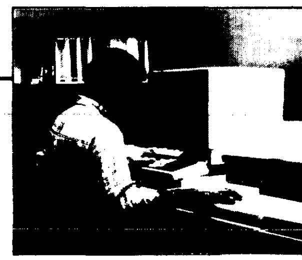
Texas Instruments step-by-step approach speeds development of SN54/74SC semicustom logic.

TI's standard-cell integration system offers two basic routes for developing standard-cell ICs. With one, you design the logic system you need and leave the chip layout and verification to TI. Or you can do the layout yourself, using standard-cell specifications. Here's the typical design sequence you'll follow if TI does the layout:

1 You develop a schematic or discrete IC breadboard of the required logic system using SN54/74SC functions (your schematic can be drawn on paper or via an engineering work station).



2 You create a TIDAL* data base for your design using a schematic-capture program. This can be done either at your plant site using an engineering work station or at your local TI Regional Technology Center.



3 You input your TIDAL data base to various design tools to perform simulation, testability analysis, test generation, and test-pattern grading. All these tools are available through your local TI Technology Center, along with computers to run them. Some of the tools can be run on your own computer or accessed via a remote-job-entry connection (depending on the type of computer you have).

4 TI runs a simulation, testability analysis, test-pattern grading, and technology check to double-check your logic design.

5 TI develops a computer-aided layout of your design.

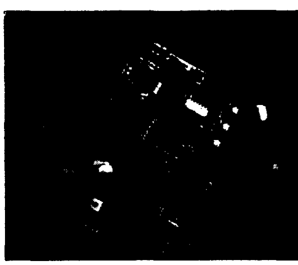
6 TI runs a post-layout simulation to validate the performance from the layout, including the extraction of the interconnect delays.

7 TI runs a schematic-verification program to check the chip layout against the TIDAL-encoded logic diagram.

8 TI runs a final simulation step to demonstrate the AC performance of the logic design. Results are submitted to you prior to prototype fabrication and become, on your approval, the final conformance specification of your standard-cell IC design.

9 TI inputs the layout data base to pattern-generation/slice-writing equipment.

10 Prototypes are fabricated, assembled, and tested against prefabrication test specifications. Testing is performed using your simulation model as a "known good unit."



11 Prototypes are shipped to you for in-system evaluation and the decision to go to production.

*TI's high-level hardware description language. Trademark of Texas Instruments.

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turnaround.

Important Notice: Texas Instruments reserves the right to make changes at any time in order to improve designs and to supply the best possible product.
Texas Instruments provides customer assistance in varied technical areas. Since TI does not possess full access to data concerning all of the uses and applications of customers' products, responsibility is assumed by TI neither for customer product design nor for any infringements of patents or rights of others which may result from TI assistance.

All the support you need... nearby

The support you need to create your standard-cell design is conveniently available at your nearest TI Regional Technology Center.

Each Technology Center is staffed with a team of standard-cell specialists who will work closely with you to coordinate TI's layout, testing, and fabrication efforts with your design goals and product schedule.

Support services include a telephone hot line for getting fast answers to technical questions. In-depth training courses on standard-cell technology. Assistance in design optimization and test development. Access to hardware and software design tools. Even complete turnkey design services. With the all-important personal contact that ensures a quick response to your needs.

Streamlined design system

TI's standard-cell integration system features a set of state-of-the-art, fully integrated design-automation tools. These range from schematic-capture and design-simulation programs to design-verification software and automated tooling equipment.

All the tools can share design information via TI's TIDAL Transportable Integrated Design Automation Language. This saves valuable engineering time by eliminating the need to recode incompatible programs.

Many of the design tools can run on your own system (depending on the level of the tool). Systems like the IBM personal computer, IBM 4341, VAX 11/780™ systems, and a wide variety of engineering work stations.

Some of the software tools are also available for licensing. Dial-up access to the more complex design software is available through the Regional Technology Centers. In addition, engineering work stations are located at each of the Technology Centers for designers who wish to come in and use them.

TI's design system is the outcome of two decades of involvement in design automation. Many of the tools—such as TI's proprietary layout-verification software—have provided major productivity improvements on scores of TI designs for ICs. This sophisticated design system gives your standard-cell design a very high probability of first-pass prototypes which are not only functional but producible.

Fast turnaround

TI's design system cuts manual intervention in the design process to a minimum, resulting in very short design-cycle times.

To speed things up still further, TI's Customized Components Division (the division responsible for TI's standard-cell product area) has its own dedicated wafer-fabrication facility and assembly and test facility for prototype and low-volume IC production.

In most cases, you'll have prototypes in your hands within six to eight weeks after joint approval of design data base.‡ Our objective is to be fast— our commitment is to provide on-time delivery of ICs that fully meet your specifications. Providing the crucial edge you need in getting a product to market ahead of your competition.

For more information

To find out more about the TI standard-cell integration system, please contact your nearest TI field sales office as listed on the back cover.

‡Cycle time from initial design to prototype shipments is typically 10 to 12 weeks.

™Digital Equipment Corporation

Texas Instruments SN54/74SC Functions

GATES

74SC00	2-INPUT NAND
74SC02	2-INPUT NOR
74SC04	INVERTER
74SC08	2-INPUT AND
74SC10	3-INPUT NAND
• 74SC11	3-INPUT NAND
74SC20	4-INPUT NAND
• 74SC21	4-INPUT AND
• 74SC22	5-INPUT NAND
74SC27	3-INPUT NOR
• 74SC30	8-INPUT NAND
74SC32	2-INPUT OR
• 74SC86	2-INPUT XOR
• 74SC260	5-INPUT NOR
• 74SC266	2-INPUT XOR
• 74SC425	3-STATE BUFFER, LOW ENABLE
• 74SC426	3-STATE BUFFER, HIGH ENABLE
• 74SC2000	6-INPUT NAND
• 74SC2001	7-INPUT NAND
• 74SC2002	6-INPUT OR
• 74SC2003	7-INPUT OR
• 74SC2004	5-INPUT AND
• 74SC2005	6-INPUT AND
• 74SC2006	7-INPUT AND
• 74SC2007	8-INPUT AND
• 74SC2008	5-INPUT OR
• 74SC2009	6-INPUT OR
• 74SC2010	7-INPUT OR
• 74SC2011	8-INPUT OR
74SC4002	4-INPUT NOR
74SC4072	4-INPUT OR
74SC4075	3-INPUT OR
• 74SC4078	8-INPUT NOR

FLIP-FLOPS, REGISTERS, LATCHES

74SC74	D-TYPE FF
• 74SC75	TRANSPARENT LATCH
• 74SC109	J-K BAR FF, PET
• 74SC112	J-K FF, NET
• 74SC373	OCTAL TRANSPARENT LATCH
• 74SC374	OCTAL D-TYPE REGISTER
• 74SC2101	D-TYPE FF WITH PARALLEL LOAD
• 74SC2102	T-TYPE FF
• 74SC2103	T-TYPE FF WITH PARALLEL LOAD
• 74SC2104	GATED T-TYPE FF
• 74SC2105	GATED T-TYPE FF WITH PARALLEL LOAD
• 74SC2106	GATED T-BAR FF
• 74SC2107	GATED T-BAR FF WITH PARALLEL LOAD

COUNTERS, TIMERS

• 74SC192	UNIVERSAL 4-BIT DECADE COUNTER
• 74SC193	UNIVERSAL 4-BIT BINARY COUNTER
• 74SC194	UNIVERSAL 4-BIT SHIFT REGISTER
• 74SC198	UNIVERSAL 8-BIT SHIFT REGISTER
• 74SC2200	UNIVERSAL 8-BIT BINARY COUNTER
• 74SC2201	UNIVERSAL 8-BIT DECADE COUNTER

DECODERS, MULTIPLEXERS

• 74SC138	3:8 DECODER
• 74SC139	2:4 DECODER
• 74SC150	16:1 MUX
• 74SC154	4:16 DECODER
• 74SC251	8:1 MUX
• 74SC253	4:1 MUX
• 74SC258	2:1 MUX

COMPARATORS, PARITY GENERATORS

• 74SC85	4-BIT COMPARATOR
• 74SC280	PARITY GENERATOR
• 74SC348	PRIORITY ENCODER
• 74SC688	8-BIT COMPARATOR

ADDERS, ALUs, SUPPORT FUNCTIONS

• 74SC83	4-BIT ADDER
• 74SC181	ALU
• 74SC182	CARRY GENERATOR
74SC482	CONTROL ELEMENT
• 74SC2300	RC CRYSTAL OSCILLATOR

ROM, RAM

• 74SC189	16 × 4 RAM
• 74SC371	256 × 8 ROM

INPUT BUFFERS

74SC5000	CMOS INPUT BUFFER
74SC5001	TTL INPUT BUFFER
• 74SC5002	2 mA BIDIRECTIONAL I/O BUFFER
• 74SC5003	SCHMITT INPUT BUFFER
• 74SC5004	4 mA BIDIRECTIONAL I/O BUFFER

OUTPUT BUFFERS

74SC5100	2 mA OUTPUT BUFFER
74SC5101	2 mA OUTPUT BUFFER, 3-STATE
74SC5102	2 mA OUTPUT BUFFER, OPEN DRAIN
• 74SC5103	4 mA OUTPUT BUFFER
• 74SC5104	4 mA OUTPUT BUFFER, 3-STATE

● Planned availability 4Q83 ● Planned availability 1H84

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TEXAS INSTRUMENTS SN54/74SC STANDARD CELL PRODUCT SUMMARY

FUNCTION	DESCRIPTION	Ci (pF)	DELAY tpD (ns)†	dDELAY d (tpD) (ns/pF)†
Internal Cell Functions:				
Inverters				
SN54/74SC04	Always Active			
IV110	1X (Minimum Drive Capability	0.15	2.8	1.5
IV120	2X	0.32	1.8	0.8
IV140	4X	0.67	1.2	0.5
IV160	6X	1.01	1.0	0.4
IV180	8X	1.34	0.9	0.3
NAND Gates				
SN54/74SC00	2-Input NAND			
NA210	1X	0.15	3.3	1.9
NA220	2X	0.33	2.0	0.9
NA230	3X	0.50	1.8	0.6
NA240	4X	0.68	1.5	0.5
NA260	6X	1.07	1.4	0.4
SN54/74SC10	3-Input NAND			
NA310	1X	0.12	4.2	2.5
NA320	2X	0.31	2.5	1.1
NA330	3X	0.48	2.2	0.7
NA340	4X	0.65	2.0	0.5
SN54/74SC20	4-Input NAND			
NA410	1X	0.14	5.0	3.0
NA420	2X	0.32	3.2	1.2
NA430	3X	0.48	2.8	0.8
NOR Gates				
SN54/74SC02	2-Input NOR			
NO210	1X	0.12	4.3	2.6
NO220	2X	0.29	2.5	1.3
NO230	3X	0.43	2.1	0.8
NO240	4X	0.58	1.8	0.6
SN54/74SC27	3-Input NOR			
NO310	1X	0.10	5.9	3.8
NO320	2X	0.27	3.7	1.9
NO330	3X	0.41	3.0	1.2
SN54/74SC4002	4-Input NOR			
NO410	1X	0.13	7.5	4.3
NO420	2X	0.24	4.9	2.3

FUNCTION	DESCRIPTION	Ci (pF)	DELAY tpD (ns)†	dDELAY d (tpD) (ns/pF)†
AND Gates				
SN54/74SC08	2-Input AND			
AN210	1X	0.15	3.8	1.0
AN220	2X	0.15	3.5	0.5
AN240	4X	0.15	3.1	0.3
AN260	6X	0.33	2.8	0.2
SN54/74SC11	3-Input AND			
AN310	1X	0.14	4.5	1.2
AN320	2X	0.14	4.1	0.7
AN340	4X	0.14	4.6	0.5
AN360	6X	0.32	3.5	0.3
OR Gates				
SN54/74SC32	2-Input OR			
OR210	1X	0.17	4.3	1.4
OR220	2X	0.17	4.0	0.8
OR240	4X	0.29	3.3	0.4
OR260	6X	0.29	3.7	0.3
SN54/74SC4075	3-Input OR			
OR310	1X	0.14	5.2	1.4
OR320	2X	0.14	5.0	0.9
OR340	4X	0.24	4.3	0.5
OR360	6X	0.24	5.1	0.4
SN54/74SC4072	4-Input OR			
OR410	1X	0.12	6.5	1.5
OR420	2X	0.12	6.2	0.9
OR440	4X	0.23	5.5	0.5
OR460	6X	0.23	5.8	0.4
FLIP-FLOPS				
SN54/74SC74	D-Type FLIP-FLOPS			
DFB20	Preset & Clear	0.13	8.8	0.7
DFP20	Preset	0.13	7.9	0.7
DFC20	Clear	0.13	7.9	0.7
DFN20	No Preset or Clear	0.16	7.0	0.7
DFY20	D Low, Preset	0.29	7.3	0.7
DFZ20	D Low, Preset & Clear	0.29	7.9	0.7
External Input and Output (I/O) Cell Functions:				
Input Cells				
SN54/74SC5000	CMOS Level Input, Inverting			
IPA00	Minimum Height Cell	1.0	1.6	0.7
IPB00	Corner Cell	1.0	1.6	0.7
IPC00	Minimum Width Cell	1.0	1.6	0.7
SN54/74SC5001	TTL Level Input, Inverting			
IPA03	Minimum Height Cell	1.7	1.6	0.4
IPB03	Corner Cell	1.7	1.6	0.4
IPC03	Minimum Width Cell	1.7	1.6	0.4

Texas Instruments

CUSTOM/SEMICUSTOM

PRODUCT PREVIEW

This page contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

FUNCTION	DESCRIPTION	Ci (pF)	DELAY tpD (ns)†	dDELAY d (tpD) (ns/pF)†
Output Cells				
SN54/74SC5100	Push-Pull, 2 mA, Non-Inverting			
OPA20	Minimum Height Cell	0.53	8.6	—
OPB20	Corner Cell	0.53	8.6	—
OPC20	Minimum Width Cell	0.53	8.6	—
SN/74SC5101	3-State, 2 mA, Non-Inverting			
OPA22	Minimum Height Cell	0.53	12.0	—
OPB22	Corner Cell	0.53	12.0	—
OPC22	Minimum Wdith Cell	0.53	12.0	—
SN54/74SC5102	Open-Drain, 2 mA, Non-Inverting			
OPA21	Minimum Height Cell	0.56	8.4	—
OPB21	Corner Cell	0.56	8.4	—
OPC21	Minimum Width Cell	0.56	8.4	—

† Delays are nominal values at room temperature and 5.0 volts. Internal cell delays are at 1.0 pF load. Output cell delays are at 15 pF. Gate delays and delta delays are average of tpHL and tpLH. Flip-flop delays are average of clock to "Q" and clock to "Q-BAR". These delays are presented to illustrate the typical capability of the SN54/74SC CMOS standard cell family. Please consult the appropriate data sheet before starting design.

PRODUCT PREVIEW

This page contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS SN54/74SC STANDARD CELL PLANNED PRODUCTS

FUNCTION	DESCRIPTION
Internal Gates	
● 54/74SC425	Buffer, 3-State, Active Low
● 54/74SC426	Buffer, 3-State, Active High
▲ 54/74SC240	Inverter, 3-State, Active Low
▲ 54/74SC231	Inverter, 3-State, Active High
● 54/74SC11	3-Input AND
● 54/74SC21	4-Input AND
▲ 54/74SC2004	5-Input AND
▲ 54/74SC2005	6-Input AND
▲ 54/74SC2006	7-Input AND
▲ 54/74SC2007	8-Input AND
● 54/74SC22	5-Input NAND
▲ 54/74SC2000	6-Input NAND
▲ 54/74SC2001	7-Input NAND
● 54/74SC30	8-Input NAND
▲ 54/74SC2008	5-Input OR
▲ 54/74SC2009	6-Input OR
▲ 54/74SC2010	7-Input OR
▲ 54/74SC2011	8-Input OR
● 54/74SC260	5-Input NOR
▲ 54/74SC2002	6-Input NOR
▲ 54/74SC2003	7-Input NOR
● 54/74SC4078	8-Input NOR
● 54/74SC86	Exclusive OR
● 54/74SC266	Exclusive NOR
Decoders/Demultiplexers	
● 54/74SC139	2:4 Decoder/Demultiplexer
● 54/74SC138	3:8 Decoder/Demultiplexer
● 54/74SC154	4:16 Decoder/Demultiplexer
Multiplexers	
● 54/74SC258	2:1 MUX, 3-State, Enable
● 54/74SC153	4:1 MUX, With or Without Enable
● 54/74SC253	4:1 MUX, 3-State, Enable
● 54/74SC152	8:1 MUX, With or Without Enable
● 54/74SC251	8:1 MUX, 3-State, Enable
▲ 54/74SC150	16:1 MUX, Enable

FUNCTION	DESCRIPTION
Bistable Latches	
● 54/74SC75	Active High Enable, or Set/Reset
● 54/74SC373	D-Type Latch, 3-State
Flip-Flops	
● 54/74SC109	J-K, Positive Edge Triggered
● 54/74SC112	J-K, Negative Edge Triggered
▲ 54/74SC374	D-FF, 3-State
● 54/74SC2101	D-FF, ASYNC Load
● 54/74SC2102	Toggle-FF
● 54/74SC2103	Toggle-FF, ASYNC Load
▲ 54/74SC2104	T-FF, Active High
▲ 54/74SC2105	T-FF, Active High, ASYNC Load
▲ 54/74SC2106	T-FF, Active Low
▲ 54/74SC2107	T-FF, Active Low, ASYNC Load
Input, Output & I/O Cells	
● 54/74SC5003	Input Buffers with Hysteresis
● 54/74SC5002	Bidirectional Buffers, 2 mA OUT
▲ 54/74SC5004	Bidirectional Buffers, 4 mA OUT
▲ 54/74SC5005	Bidirectional Buffers, 6 mA OUT
▲ 54/74SC5103	Output Buffers, 4 mA OUT
▲ 54/74SC5105	Output Buffers, 6 mA OUT
▲ 54/74SC5104	3-State Output Buffers, 4 mA OUT
▲ 54/74SC5106	3-State Output Buffers, 6 mA OUT
Counters & Shift Registers	
▲ 54/74SC192	Universal 4-Bit Decade Counter
▲ 54/74SC193	Universal 4-Bit Binary Counter
▲ 54/74SC2200	Universal 8-Bit Binary Counter
▲ 54/74SC2201	Universal 8-Bit Decade Counter
▲ 54/74SC194	Universal 4-Bit Shift Register
▲ 54/74SC198	Universal 8-Bit Shift Register

Planned Release Dates
● 4Q83 ▲ 1H84 Δ 2H84

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

FUNCTION	DESCRIPTION
Comparators, Parity Generators	
▲ 54/74SC85	4-Bit Comparator
▲ 54/74SC688	8-Bit Comparator
▲ 54/74SC280	Parity Generator
▲ 54/74SC348	8:3 Priority Encoder, 3-State
Adders, Alus, Support Functions	
▲ 54/74SC83	4-Bit Adder
▲ 54/74SC181	ALU
▲ 54/74SC182	Carry Generator
● 54/74SC2300	Crystal Oscillator
RAM, ROM, PLA	
● 54/74SC189	16 × 4 RAM
▲ 54/74SC371	256 × 8 ROM
● 54/74SC2500	PLA

FUNCTION	DESCRIPTION
Procedural Cells	
● 54/74SC3000	RAM, 1K, 2-256 Words × 4-32 Bits
Δ 54/74SC3012	RAM, Dual Port
Δ 54/74SC3013	RAM, Serial Access
▲ 54/74SC3001	ROM
● 54/74SC3002	PLA
▲ 54/74SC3003	Universal Shift Register
▲ 54/74SC3004	Synchronous Binary Counter
▲ 54/74SC3005	Synchronous Decimal Counter
▲ 54/74SC3006	Register File
Δ 54/74SC3014	Register File with Stack
Δ 54/74SC3015	Register File, Dual Port
● 54/74SC3007	Arithmetic Logic Unit
● 54/74SC3008	Synchronous Full Adder
▲ 54/74SC3009	Comparator, Magnitude
▲ 54/74SC3010	Comparator, Equals
Δ 54/74SC3016	Multiplier
Δ 54/74SC3017	Barrell Shifter
▲ 54/74SC3011	LCD Driver

Planned Release Dates
● 4Q83 ▲ 1H84 Δ 2H84

TEXAS INSTRUMENTS SN54/74SC STANDARD CELL PLANNED PRODUCTS

FUNCTION	DESCRIPTION
Internal Gates	
● 54/74SC425	Buffer, 3-State, Active Low
● 54/74SC426	Buffer, 3-State, Active High
▲ 54/74SC240	Inverter, 3-State, Active Low
▲ 54/74SC231	Inverter, 3-State, Active High
● 54/74SC11	3-Input AND
● 54/74SC21	4-Input AND
▲ 54/74SC2004	5-Input AND
▲ 54/74SC2005	6-Input AND
▲ 54/74SC2006	7-Input AND
▲ 54/74SC2007	8-Input AND
● 54/74SC22	5-Input NAND
▲ 54/74SC2000	6-Input NAND
▲ 54/74SC2001	7-Input NAND
● 54/74SC30	8-Input NAND
▲ 54/74SC2008	5-Input OR
▲ 54/74SC2009	6-Input OR
▲ 54/74SC2010	7-Input OR
▲ 54/74SC2011	8-Input OR
● 54/74SC260	5-Input NOR
▲ 54/74SC2002	6-Input NOR
▲ 54/74SC2003	7-Input NOR
● 54/74SC4078	8-Input NOR
● 54/74SC86	Exclusive OR
● 54/74SC266	Exclusive NOR
Decoders/Demultiplexers	
● 54/74SC139	2:4 Decoder/Demultiplexer
● 54/74SC138	3:8 Decoder/Demultiplexer
● 54/74SC154	4:16 Decoder/Demultiplexer
Multiplexers	
● 54/74SC258	2:1 MUX, 3-State, Enable
● 54/74SC153	4:1 MUX, With or Without Enable
● 54/74SC253	4:1 MUX, 3-State, Enable
● 54/74SC152	8:1 MUX, With or Without Enable
● 54/74SC251	8:1 MUX, 3-State, Enable
▲ 54/74SC150	16:1 MUX, Enable

FUNCTION	DESCRIPTION
Bistable Latches	
● 54/74SC75	Active High Enable, or Set/Reset
● 54/74SC373	D-Type Latch, 3-State
Flip-Flops	
● 54/74SC109	J-K, Positive Edge Triggered
● 54/74SC112	J-K, Negative Edge Triggered
▲ 54/74SC374	D-FF, 3-State
● 54/74SC2101	D-FF, ASYNC Load
● 54/74SC2102	Toggle-FF
● 54/74SC2103	Toggle-FF, ASYNC Load
▲ 54/74SC2104	T-FF, Active High
▲ 54/74SC2105	T-FF, Active High, ASYNC Load
▲ 54/74SC2106	T-FF, Active Low
▲ 54/74SC2107	T-FF, Active Low, ASYNC Load
Input, Output & I/O Cells	
● 54/74SC5003	Input Buffers with Hysteresis
● 54/74SC5002	Bidirectional Buffers, 2 mA OUT
▲ 54/74SC5004	Bidirectional Buffers, 4 mA OUT
▲ 54/74SC5005	Bidirectional Buffers, 6 mA OUT
▲ 54/74SC5103	Output Buffers, 4 mA OUT
▲ 54/74SC5105	Output Buffers, 6 mA OUT
▲ 54/74SC5104	3-State Output Buffers, 4 mA OUT
▲ 54/74SC5106	3-State Output Buffers, 6 mA OUT
Counters & Shift Registers	
▲ 54/74SC192	Universal 4-Bit Decade Counter
▲ 54/74SC193	Universal 4-Bit Binary Counter
▲ 54/74SC2200	Universal 8-Bit Binary Counter
▲ 54/74SC2201	Universal 8-Bit Decade Counter
▲ 54/74SC194	Universal 4-Bit Shift Register
▲ 54/74SC198	Universal 8-Bit Shift Register

Planned Release Dates
● 4Q83 ▲ 1H84 Δ 2H84

TEXAS INSTRUMENTS
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FUNCTION	DESCRIPTION
Comparators, Parity Generators	
▲ 54/74SC85	4-Bit Comparator
▲ 54/74SC688	8-Bit Comparator
▲ 54/74SC280	Parity Generator
▲ 54/74SC348	8:3 Priority Encoder, 3-State
Adders, Alus, Support Functions	
▲ 54/74SC83	4-Bit Adder
▲ 54/74SC181	ALU
▲ 54/74SC182	Carry Generator
● 54/74SC2300	Crystal Oscillator
RAM, ROM, PLA	
● 54/74SC189	16 × 4 RAM
▲ 54/74SC371	256 × 8 ROM
● 54/74SC2500	PLA

FUNCTION	DESCRIPTION
Procedural Cells	
● 54/74SC3000	RAM, 1K, 2-256 Words × 4-32 Bits
Δ 54/74SC3012	RAM, Dual Port
Δ 54/74SC3013	RAM, Serial Access
▲ 54/74SC3001	ROM
● 54/74SC3002	PLA
▲ 54/74SC3003	Universal Shift Register
▲ 54/74SC3004	Synchronous Binary Counter
▲ 54/74SC3005	Synchronous Decimal Counter
▲ 54/74SC3006	Register File
Δ 54/74SC3014	Register File with Stack
Δ 54/74SC3015	Register File, Dual Port
● 54/74SC3007	Arithmetic Logic Unit
● 54/74SC3008	Synchronous Full Adder
▲ 54/74SC3009	Comparator, Magnitude
▲ 54/74SC3010	Comparator, Equals
Δ 54/74SC3016	Multiplier
Δ 54/74SC3017	Barrell Shifter
▲ 54/74SC3011	LCD Driver

Planned Release Dates
● 4Q83 ▲ 1H84 Δ 2H84

TEXAS INSTRUMENTS
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TAL-002, TAL-004 LOW POWER SCHOTTKY LOGIC ARRAYS

JUNE 1983 – REVISED OCTOBER 1983

- **Family**

TWO ARRAYS	INTERNAL GATES	I/O BUFFERS
TAL-002	320	28
TAL-004	500	36

- **Technology**

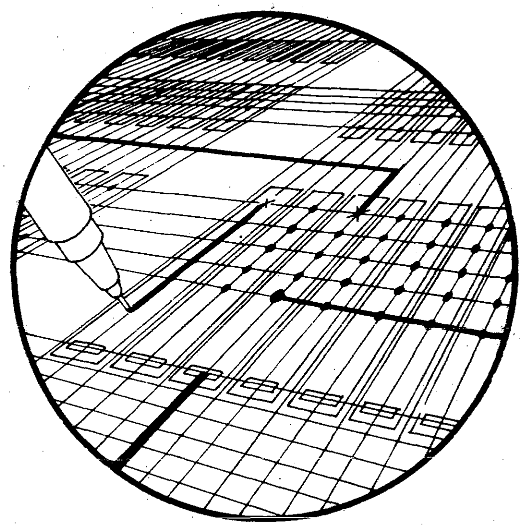
  Established Double Level Metal Low Power Schottky

- **Layout**

  Designed for the user at His Own Location or by TI Regional Technology Centers

- **Internal Gates**
  - **Single 5-V Power Supply**
  - **5 ns Maximum Gate Delay at 1.25 mW Gate Dissipation**
  - **Toggle Rate 25 MHz**
  - **Twenty-Two Standard Macros currently available**

- **I/O Buffers**
  - **Standard True and Complement Input**
  - **NAND Output**
  - **Three-State Output**
  - **Standard I/O**
  - **Open-Collector NAND Output**
  - **Schmitt Trigger Input**
  - **Power-Up Reset Circuit**



- **Design Verification**
  - **Closed Loop Logic to Layout Check**
  - **Test Pattern and Design Rule Check**
  - **Logic, Timing and Fault Simulation**
  - **Easy Access by User to TI Software**

description

The TAL family of devices are Low Power Schottky master slices which are held in stock at TI. The master slices are converted into LSI slices by the deposition of two layers of metal according to an interconnection pattern drawn by the user on a TI supplied translucent grid. The resulting devices are tested according to input-output logic patterns devised by the user, and become the user's proprietary LSI parts.

A comprehensive design manual sets out the logic and layout rules for the process and also explains a simple short-hand method of describing the circuit so that a detailed check of layout and test patterns can be carried out at TI. This computer aided check comprehends logic, layout, and test patterns and results in a dialogue in which the user and TI work together to eliminate errors prior to mask fabrication.

The layout task is considerably eased by the availability of standard overlays for commonly used logic functions and standard buffers are provided for inputs and outputs. The user is also able to specify his own blocks of logic in cases where a number of identical pieces of circuit occur in the design.

As can be seen from Figure 1, the array consists of blocks of five input NAND gates of which any four are useable in any one cell. The gates consist of output transistor TI and multi-emitter transistor T2. The emitter of T1 is normally connected to ground and its collector can feed up to eight subsequent multi-emitter inputs within the array. The logic design rules for the interconnection of gates are explained in detail in the design manual.

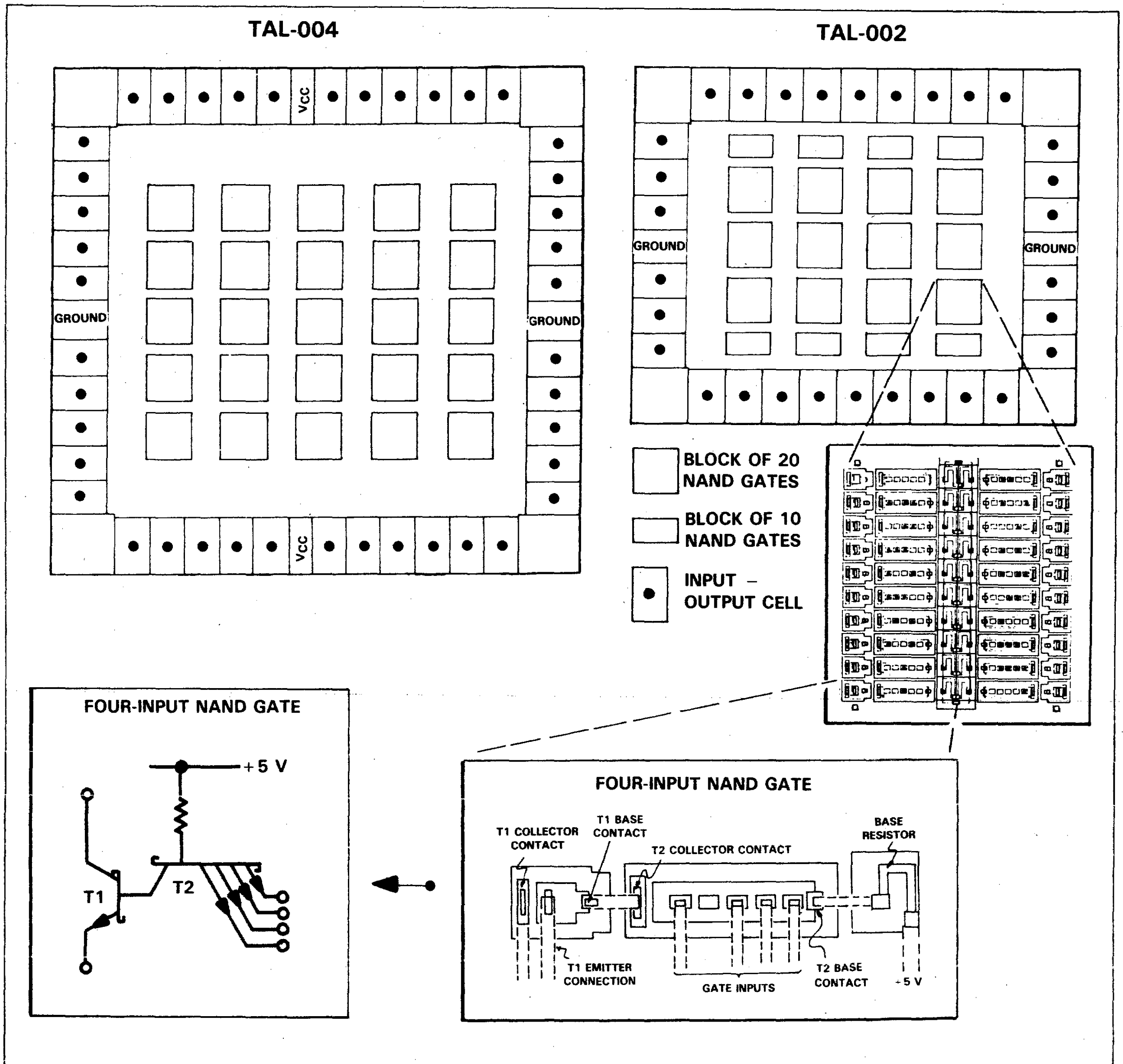


FIGURE 1 – ARRAY STRUCTURE

The TAL-004 has 500 internal four-input NAND gates and the TAL-002 has 320. A single 5-V power supply is needed for the arrays and both device types are available in 28- and 40-pin DIL plastic packages, with the option also, of a 20-pin package for the TAL-002.

manual layout

A reproduction of the translucent user layout grid is shown in Figure 2. The lower level of metal interconnect on the finished device is called Metal 1 and is specified on the grid by marking the vertical lines and the upper level, Metal 2, is similarly designated by marking the horizontal lines. Electrical connection between the two layers is made by so called "vias" and to underlying gates by "contacts." Layout design rules govern the location of interconnections, vias, and contacts and these are clearly explained in the design manual.

Standard logic functions and I/O buffers are specified by attaching cut outs to the user grid. Symbols for the logic function overlays (macros) and I/O's are supplied on a sheet similar to the user grid.

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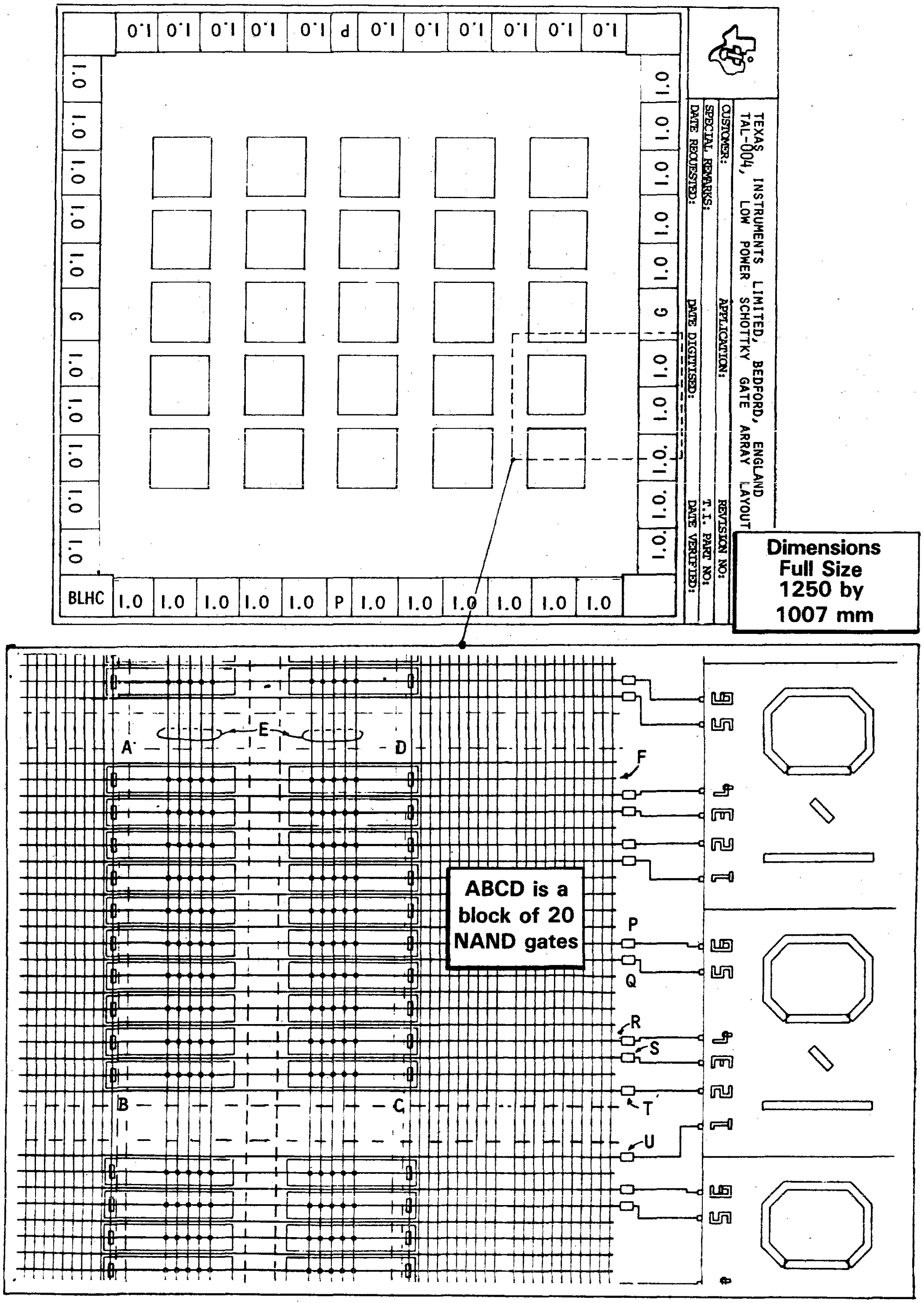


FIGURE 2 – CUSTOMER LAYOUT GRID

TAL-002, TAL-004 LOW POWER SCHOTTKY LOGIC ARRAYS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Operating junction temperature	150°C
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			8	mA
Input rise time, $t_{r(IN)}$	2.4		30	ns
Operating free-air temperature	0		70	°C

INTERNAL FOUR-INPUT NAND GATES

recommended operating conditions

PARAMETER	MIN	TYP	MAX	UNIT
Fan-in			8	Gate Loads
Fan-out			8	Gate Loads

switching characteristics over full range of recommended operating conditions

PARAMETER			MIN	TYP	MAX	UNIT
t_p	Propagation delay time	1-input NAND gate	3.5	4.5	5	ns
		2-input NAND gate	4	5.3	5.8	
		3-input NAND gate	4.5	6.1	6.6	
		4-input NAND gate	5	6.9	7.4	
Δt_p	increased propagation delay time per inch of interconnection track on the user layout grid			0.075		ns

TABLE 1 – INTERNAL GATE MACROS†

SYMBOL	DESCRIPTION			SYMBOL	DESCRIPTION	
DFF	D Flip-Flops	Standard	Three layouts	DEC8	Decoder	3- to 8-line demultiplexer/decoder
DFFA				MUX4	Multiplexers	4- to 1-line multiplexer
WDFF				MUX8		8- to 1-line multiplexer
DFFC		With CLEAR		ADD1	Arithmetic Functions	1-bit full adder
DPC1		With PRESET and CLEAR	Two layouts	EXOR		Exclusive-OR gate
WDPC				EXNOR		Exclusive-NOR gate
JKPC	J-K Flip-Flop	With PRESET and CLEAR		PAR8		8-bit parity generator
EFF	Enable Flip-Flops	Standard		MAG4		4-bit magnitude comparator
DEFF		Driver 2-bit latch		SYCT	Counters	4-bit synchronous up counter
SEFF		Stacking 2-bit latch		UDCT		4-bit synchronous up/down counter
DEC4	Decoder	2- to 4-line demultiplexer/decoder		BCD		4-bit synchronous decimal up counter

† For detailed descriptions of the internal gate macros, please refer to the *"Low Power Schottky Logic Array Design Manual."*

TABLE 2 – INPUT/OUTPUT BUFFERS

SYMBOL	DESCRIPTION	SYMBOL	DESCRIPTION
BF1A	True and Complement Inputs	BF5A	Two-Input Open-Collector Inverting Outputs
BF1B	True and Complement Inputs	BF5B	Two-Input Open-Collector Inverting Outputs
BF2A	Two-Input NAND Output	BF6A	Inverting Schmitt Trigger Input
BF3A	Standard Input/Output	BF7A	Power-Up Reset Circuit
BF4A	Inverting Three-State Output	BF7A	Power-Up Reset Circuit

electrical characteristics over full ranges of recommended operating conditions

PARAMETER				TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current	BF1A		V_{CC} = 4.75 V to 5.25 V, T_A = 0°C to 70°C, See note 1		1.38	1.95	mA
		BF2A, BF5A				1.38	1.95	
		BF3A	Output enabled			3.18	4.5	
		BF3A	Output disabled			3.3	4.8	
		BF4A	Output enabled			2.93	4.15	
		BF4A	Output disabled			3.15	4.45	
		BF6A				1.46	2.1	
		BF7A				0.68	1	

NOTE 1: Values given assume that the buffer spends equal time in each of its logic states; please refer to the *"Low Power Schottky Logic Array Design Manual"* for more information.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −400 μA, V_{CC} = 4.75 V	2.7	3.35		V
V_{OL}	Low-level output voltage		I_{OL} = 8 mA, V_{CC} = 4.75 V		0.35	0.5	V
I_{OL}	Low-level output current, open-collector, internal pullup	BF5B	V_O = 0.4 V	0.35		0.8	mA
I_{OS}	Short-circuit output current		V_{CC} = 5.25 V	−20	−60	−100	mA
I_{OZH}	Off-state output current, high-level voltage applied	BF4A	V_{CC} = 5.25 V, V_O = 2.7 V			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	BF4A	V_{CC} = 5.25 V, V_O = 0.4 V			−20	μA

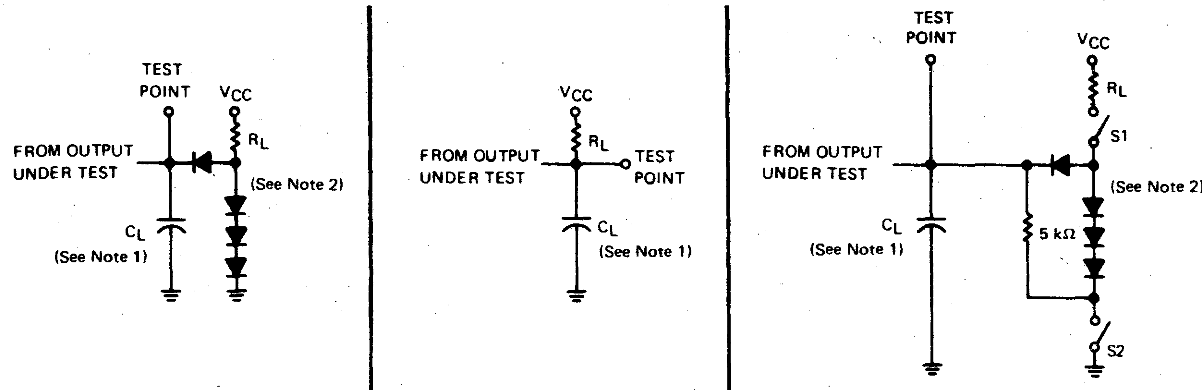
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage		$I_K = -18$ mA			−1.5	V
V_{T+}	Positive-going threshold voltage	BF6A		1.4	1.68	1.9	V
V_{T-}	Negative-going threshold voltage	BF6A		0.5	0.84	1	V
I_{IH}	High-level input current	BF1A, BF6A	$V_{CC} = 5.25$ V, $V_I = 2.7$ V			20	μA
		BF3A				40	
		BF1B	$V_{CC} = 5.25$ V, $V_I = 2.7$ V			−400	
I_{IL}	Low-level input current	BF1A, BF3A, BF6A	$V_{CC} = 5.25$ V, $V_I = 0.4$ V			−200	μA
		BF1B				−850	
I_I	Input current	BF1B	$V_{CC} = 5.25$ V, $V_I = 5.5$ V			100	μA
		All others	$V_{CC} = 5.25$ V, $V_I = 7$ V			100	

switching characteristics over full ranges of recommended operating conditions

PARAMETER					TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low-to-high level	BF1A	True		$V_{CC} = 4.75$ V to 5.25 V, $T_A = 0°C$ to 70°C, See Figure 3	5	10	15	ns
			Complement			4	7	10	
		BF2A	Output port			9	11	13	
		BF3A	Input mode	True		5	10	15	
				Complement		4	7	10	
			Output port			8	11	14	
		BF4A	Output port			8	11	14	
		BF5A	Output port			10	15	25	
		BF6A	Complement array input			9	12	15	
t_{PHL}	Propagation delay, high-to-low level	BF1A	True		$V_{CC} = 4.75$ V to 5.25 V, $T_A = 0°C$ to 70°C, See Figure 3	5	9	12	ns
			Complement			3	5	7	
		BF2A	Output port			5	7	9	
		BF3A	Input mode	True		5	9	12	
				Complement		3	5	7	
			Output port			7	10	13	
		BF4A	Output port			7	10	13	
		BF5A	Output port			5	7	9	
		BF6A	Complement array input			8	10	12	
t_{PZH}	Output enable time to high level	BF3A	Output port		$V_{CC} = 4.75$ V to 5.25 V, $T_A = 0°C$ to 70°C, See Figure 3	10	14	18	ns
		BF4A	Output port			10	14	18	
t_{PZL}	Output enable time to low level	BF3A	Output port			10	14	18	ns
		BF4A	Output port			10	14	18	
t_{PHZ}	Output disable time to high level	BF3A	Output port			12	17	22	ns
		BF4A	Output port			12	17	22	
t_{PLZ}	Output disable time to low level	BF3A	Output port			12	17	22	ns
		BF4A	Output port			12	17	22	

PARAMETER MEASUREMENT INFORMATION†



LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

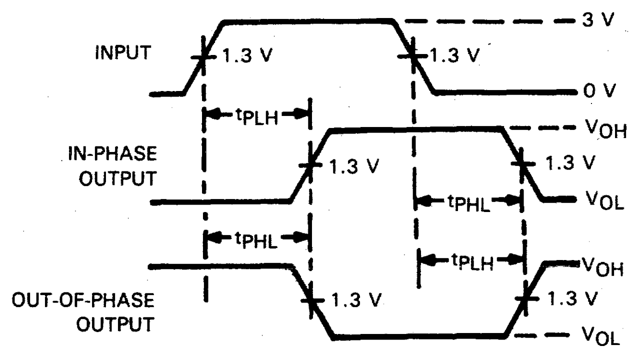
LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

LOAD CIRCUIT FOR THREE-STATE OUTPUTS

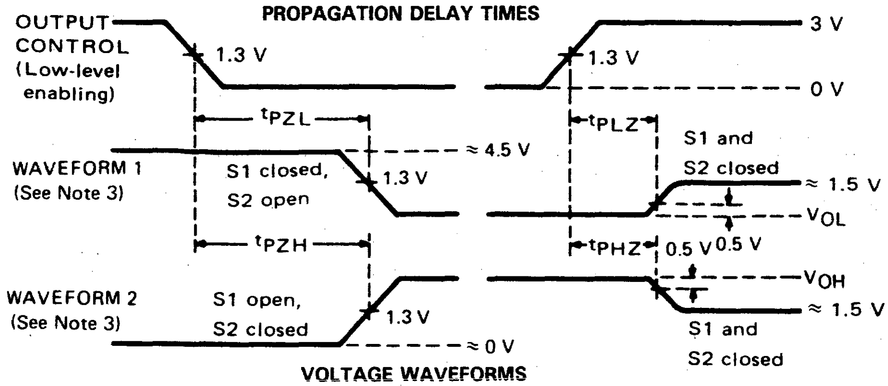
† I/O cells only.

NOTES: 1. C_L includes probe and jig capacitance.
2. All diodes are 1N916 or 1N3064.

FIGURE 3 – LOAD CIRCUITS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: 3. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
4. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
5. All input pulses are supplied by generators having the following characteristics: $t_r \leq 15$ ns, $t_f \leq 15$ ns, PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$.
6. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

FIGURE 4 – SWITCHING TIMES

TAT004, TAT008 STL LOGIC ARRAYS

DECEMBER 1980 – REVISED OCTOBER 1983

- **High-Performance Master Logic Arrays**
  - **Designed for Automated Layout**
  - **Mask Programmable**
  - **Supported by TI Logic Array Design System (TILADS*)**
- **Two Master Arrays**

	Internal Gates	Typical Usable Internal Gates	I/O Buffers
TAT008	1008	800	104
TAT004	540	430	76

- **High-Performance Schottky Transistor Logic (STL) Design**
  - **2.5 ns Typical Gate Propagation Delay at 600 μW**
  - **80-MHz Toggle Rate**
- **Low-Power Schottky TTL Compatible Input and Output Buffers**
  - **Non-Inverting Inputs**
  - **Choice of 3-State, Totem-Pole and Open-Collector Outputs**

description

The TAT004 and TAT008 are a pair of high-performance logic arrays, using Schottky Transistor Logic (STL) technology. The arrays can be mask configured to fulfill unique logic requirements, allowing for efficient implementation of custom IC functions, SSI or MSI logic replacement, and, in many cases, complete board replacement.

The master array employs a cellular organization with channels dedicated to intercellular connections. The internal cells contain 18 high-performance STL gates, and the peripheral cells contain low-power Schottky TTL (TTL-LS) compatible input and output buffers.

All Texas Instruments TAT Series logic arrays are supported by a totally integrated software design utility, which allows the user to encode his logic design and test pattern set for simulation, analysis, and verification of the design prior to release to TI for layout and prototyping. The computer-automated layout system has a recommended 80% gate utilization level.

package options

The TAT004 and the TAT008 are available in the packages indicated by check marks in the table below.

TAT004	40-PIN	64-PIN		
Dual-in-line plastic (N) packages	√	√		
TAT008	**40-PIN**	**68-PIN**	**84-PIN**	**108-PIN**
Dual-in-line plastic (N) packages	√	–	–	–
Ceramic chip carriers	–	–	√	–
Plastic chip carriers	–	√	–	–
Pin grid arrays	–	–	√	√

input/output buffer options

The TAT004 and TAT008 are provided with a library of input/output circuits for maximum design flexibility. The buffers are arranged around the periphery of the array in cells, called buffer cells. Each buffer cell contains two bond pad locations plus the basic components needed to mask program the cell into various TTL low-power Schottky-compatible buffers. A buffer cell can contain two input buffers, but if a cell contains one of the available output buffer types, then only one input buffer can share the buffer cell with it. Table 1 lists the available buffers along with their label as used by the TI Logic Array Design System.

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TABLE 1 – TAT004 AND TAT008 BUFFERS

SYMBOL	DESCRIPTION	SYMBOL	DESCRIPTION
SNI	Noninverting Input	SOT	Inverting 3-State Output with Active Low Enable
SNI2	Dual Noninverting Inputs		
SAND	AND Input	SBD	Bidirectional Buffer with Inverting 3-State Output, Active Low Enable
SAND2	Dual AND Inputs		
SO	Inverting Totem-Pole Output	SNIO	Bidirectional Buffer with Inverting Open-Collector Output
SOC	Inverting Open-Collector Output		

absolute maximum ratings over operating free-air temperature range

Supply voltage: V_{CC1} (see Note 1) .... 7 V
V_{CC2} .... 3 V
Input voltage .... 7 V
Output voltage .... 7 V
Operating free-air temperature range .... 0°C to 70°C
Operating junction temperature .... 150°C
Storage temperature range .... −65°C to 150°C

NOTE 1: All voltages are with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.5	5	5.5	V
Supply voltage, V_{CC2}	1.8	2	2.2	V
Fan-in (internal gate)			8	
Fan-out (internal gate)			4	
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			8	mA
Transition time at any input, t_T	2.4		30	ns
Operating free-air temperature range, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltages and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IK}	Input clamp voltage	$I_I = -18$ mA			−1.5	V
V_{OH}	High-level output voltage (see Note 2)	$I_{OH} = -400$ μA	2.5	3.4		V
V_{OL}	Low-level output voltage	$I_{OL} = 8$ mA			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied (see Note 3)	$V_O = 2.4$ V			20	μA
I_{OZL}	Off-state output current, low-level voltage applied (see Note 3)	$V_O = 0.4$ V			−20	μA
I_I	Input current at maximum input voltage	$V_I = 7$ V			0.1	mA
I_{IH}	High-level input current	$V_I = 2.7$ V			20	μA
I_{IL}	Low-level input current	$V_I = 0.4$ V			0.8	mA
I_{OS}	Short-circuit output current (see Note 2 and 4)	$V_{CC1} = 5.5$ V	−20		−100	mA
I_{OH}	High-level output current (see Note 5)	$V_{OH} = 5.5$ V			250	μA

† All typical values are at $T_A = 25°C$, $V_{CC1} = 5$ V, $V_{CC2} = 2$ V.

NOTES: 2. Does not apply to SOC or SNIO buffers.
3. Applies only to SOT buffer.
4. Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
5. Applies only to SOC and SNIO buffers.

switching characteristics of internal gate over full range of operating conditions

PARAMETER		MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay time per gate, fan-in = 1	1.5	2.5	3.5	ns
Δt_{PLH}	Increased propagation delay time for each additional fan-in		0.27	0.40	ns
Δt_{PHL}	Increased propagation delay time for each additional fan-in		0.13	0.20	ns
$\Delta t_{PLH(M1)}$†	Additional propagation delay time for each mil of metalized interconnect pattern		0.017	0.040	ns
$\Delta t_{PLH(M2)}$†	Additional propagation delay time for each mil of metalized interconnect pattern		0.015	0.035	ns
$\Delta t_{PHL(M)}$†	Additional propagation delay time for each mil of metalized interconnect pattern			0.003	ns

† M1 = first-level metal, M2 = second-level metal, and M = first- or second-level metal.

switching characteristics of input buffer over full range of operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Note 6	1	2	4	ns
t_{PHL}	Propagation delay time, high-to-low-level output		2	3.5	6	ns

switching characteristics of tristate and totem-pole output buffers over full range of operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$C_L = 50$ pF, $R_L = 2$ kΩ, See Note 6	4	7	11	ns
t_{PHL}	Propagation delay time, high-to-low-level output		6	12	19	ns
t_{PHZ}	Disable time from high level	$C_L = 15$ pF, $R_L = 2$ kΩ, See Note 6	8	14	20	ns
t_{PLZ}	Disable time from low level		6	10	15	ns
t_{PZH}	Enable time to high level		4	8	12	ns
t_{PZL}	Enable time to low level		5	10	16	ns

NOTE 6: Refer to the TAL-002, TAL-004 Data Sheet for load circuits and switching times.

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switching characteristics of open-collector output buffers over full range of operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low-to-high-level output	C_L = 50 pF, R_L = 2 kΩ, See Note 6	11	20	31	ns
t_{PHL}	Propagation delay, high-to-low-level output		9	21	33	ns

NOTE 6: Refer to the TAL-002, TAL-004 Data Sheet for load circuits and switching times.

power dissipation versus package, T_A = 70°C (still air, no heat sinking, T_J = 150°C maximum)

PACKAGE	θ_{J-A} (°C/WATT)	POWER DISSIPATION MAX (WATTS)
40-pin plastic dual-in-line	65	1.23
64-pin plastic dual-in-line	45	1.78
68-pin plastic chip carrier	46	1.74
84-pin ceramic chip carrier	39	2.05
84-pin ceramic pin grid array	39	2.05
108-pin ceramic pin grid array	38	2.11

power dissipation versus buffer type (see Note 7)

BUFFER		POWER DISSIPATION (mW)			
		T_J = 25°C		T_J = 125°C	
		TYP†	MAX‡	TYP†	MAX‡
SNI		3.60	5.94	3.00	4.94
SAND		3.60	5.94	3.00	4.94
SO		8.08	13.31	6.67	10.95
SOC		5.83	9.63	4.81	7.91
SBD	Output enabled	14.59	23.98	12.15	19.75
	Output disabled	16.90	27.77	13.94	22.84
SOT	Output enabled	11.00	18.06	9.06	14.82
	output disabled	11.82	19.34	9.66	15.77
SNIO	Output active	9.43	15.57	7.81	12.85
Internal gate (V_{CC2})		0.668	1.12	0.574	0.959

NOTE 7: All power dissipation values are with 50% duty cycle.
† Typical values are with nominal resistors, V_{CC1} = 5 V, and V_{CC2} = 2 V.
‡ Maximum values are with minimum resistors, V_{CC1} = 5.5 V, and V_{CC2} = 2.2 V.

PARAMETER MEASUREMENT INFORMATION

Refer to the TAL-002, TAL-004 Data Sheet for load circuits and switching times.

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1001 E. Campbell Road
Richardson, TX 75081
(214) 680-5066

NORTHERN CALIFORNIA
5353 Betsy Ross Drive
Santa Clara, CA 95054
(408) 748-2222

SOUTHERN CALIFORNIA
17891 Cartwright Drive
Irvine, CA 92714
(714) 660-8140

BEDFORD, ENGLAND
Texas Instruments Limited
Manton Lane
Bedford MK41 7PA
234-67466

PARIS, FRANCE
Texas Instruments France
8-10 Avenue Morane Saulnier
Boite Postale 67
78141 Velizy-Villacoublay Cedex, Paris
39-46-9712

FREISING, WEST GERMANY
Texas Instruments Deutschland GmbH
Haggertystrasse 1
D-8050 Freising
8168-800

HANNOVER, WEST GERMANY
Texas Instruments Deutschland GmbH
Kirchhorsterstrasse 2
3000 Hannover 51
0511/643021

RIETI, ITALY
Texas Instruments Semiconduttori Italia S.P.A.
Viale Delle Scienze, 1
02015 Cittaducale, Rieti
746-6941

TOKYO, JAPAN
Texas Instruments Japan Limited
Aoyama Fuji Building
6-12, Kita-Aoyama 3-Chome
Minato-Ku, Tokyo 107
3-498-2111

STOCKHOLM, SWEDEN
Texas Instruments Sviergefilialen
Norra Hamnvasen 3
Box 39103, S-100 54, Stockholm
8-235480

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SRSB044

Field Programmable Logic

Product Guide

TEXAS INSTRUMENTS

Texas Instruments

CUSTOM/SEMICUSTOM

NUMERICAL INDEX
FIELD PROGRAMMABLE LOGIC ARRAYS

DEVICE	FUNCTION	AVAILABILITY
PL16L8	FPL Fixed-OR Arrays	NOW
PL16R4		NOW
PL16R6		NOW
PL16R8		NOW
PL20L8	FPL Fixed-OR Arrays	▲
PL20R4		▲
PL20R6		▲
PL20R8		▲
PL839	14 X 32 X 6 Field Programmable Logic Arrays	▲
PL840	14 X 32 X 6 Field Programmable Logic Arrays	▲
PLR19L8	FPL Registered-Input Fixed-OR Arrays	▲
PLR19R4		▲
PLR19R6		▲
PLR19R8		▲
PLT19L8	FPL Latched-Input Fixed-OR Arrays	▲
PLT19R4		▲
PLT19R6		▲
PLT19R8		▲

▲ Planned for future announcement. Contact TI field sales office or authorized TI distributor for status.

'PL16L8

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

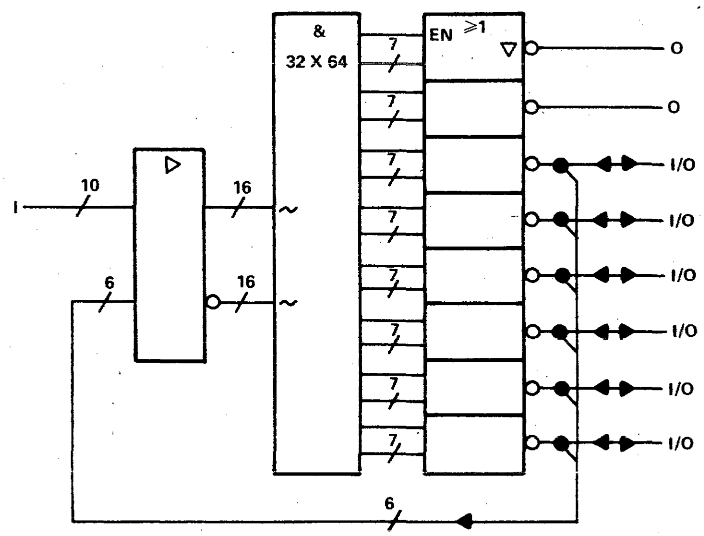
- Octal 16-input AND-OR-INVERT gate array

pin assignments

J, N PACKAGES			
1	I	11	I
2	I	12	O
3	I	13	I/O
4	I	14	I/O
5	I	15	I/O
6	I	16	I/O
7	I	17	I/O
8	I	18	I/O
9	I	19	O
10	GND	20	V_{CC}

SN54PL16L8 (J)   SN74PL16L8 (J,N)

functional block diagram



~denotes fused inputs

'PL16R4

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

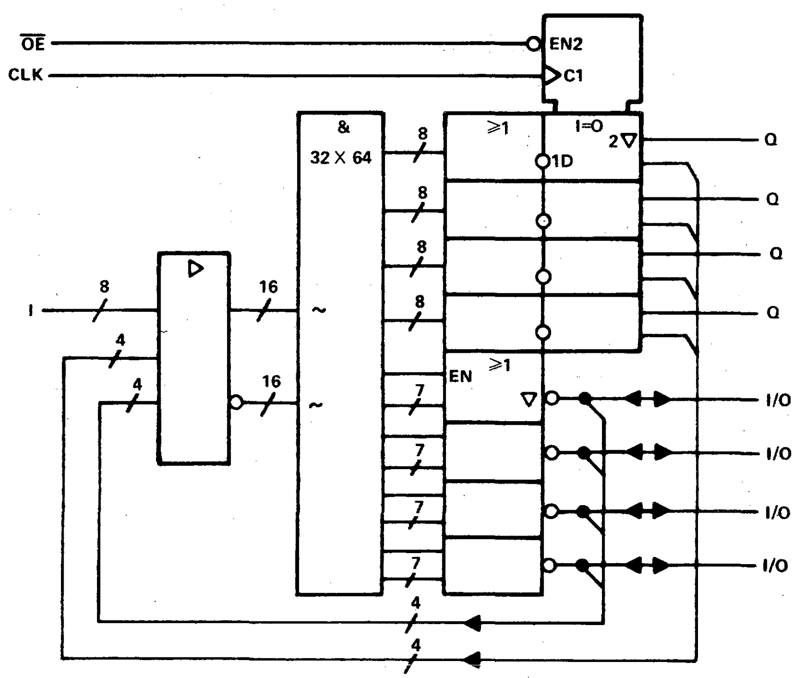
- Quad 16-input registered AND-OR gate array

pin assignments

J, N PACKAGES			
1	CLK	11	$\overline{OE}$
2	I	12	I/O
3	I	13	I/O
4	I	14	Q
5	I	15	Q
6	I	16	Q
7	I	17	Q
8	I	18	I/O
9	I	19	I/O
10	GND	20	V_{CC}

SN54PL16R4 (J)   SN74PL16R4 (J,N)

functional block diagram



~denotes fused inputs

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Refer to data sheet in this section for additional information.

See Application Note section for additional information on Texas Instruments Bipolar Programmable Logic Arrays.

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'PL16R6

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

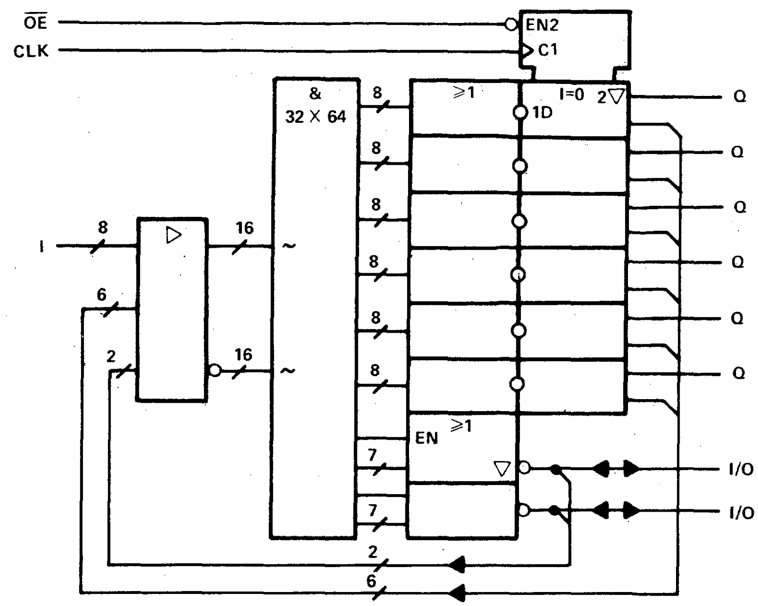
- Hex 16-input registered AND-OR gate array

pin assignments

J, N PACKAGES			
1	CLK	11	$\overline{OE}$
2	I	12	I/O
3	I	13	Q
4	I	14	Q
5	I	15	Q
6	I	16	Q
7	I	17	Q
8	I	18	Q
9	I	19	I/O
10	GND	20	V_{CC}

SN54PL16R6 (J) SN74PL16R6 (J,N)

functional block diagram



~denotes fused inputs

'PL16R8

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

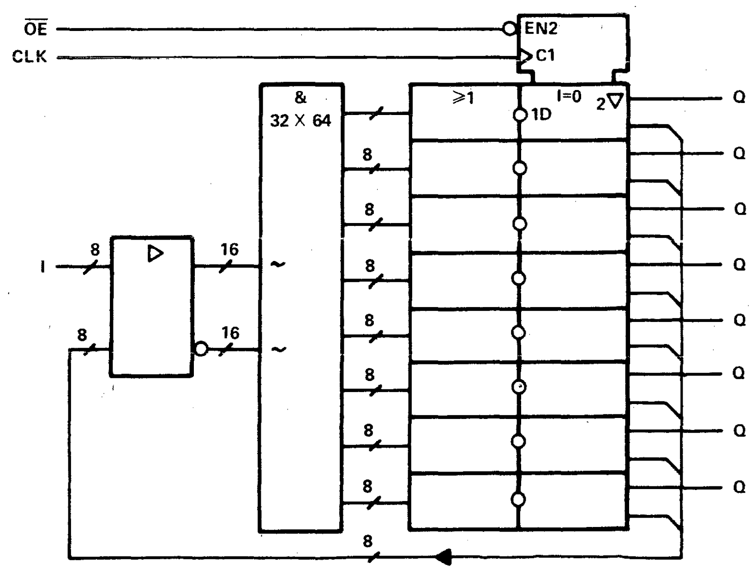
- Octal 16-input registered AND-OR gate array

pin assignments

J, N PACKAGES			
1	CLK	11	$\overline{OE}$
2	I	12	Q
3	I	13	Q
4	I	14	Q
5	I	15	Q
6	I	16	Q
7	I	17	Q
8	I	18	Q
9	I	19	Q
10	GND	20	V_{CC}

SN54PL16R8 (J) SN74PL16R8 (J,N)

functional block diagram



~denotes fused inputs

Refer to data sheet in this section for additional information.

See Application Note section for additional information on Texas Instruments Bipolar Programmable Logic Arrays.

'PL20L8

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

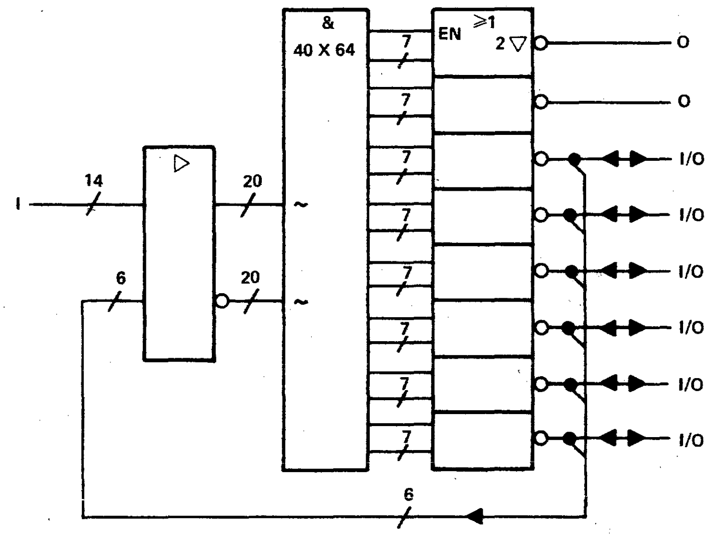
- Octal 20-input AND-OR-INVERT gate array

pin assignments

JT, NT PACKAGES			
1	I	13	I
2	I	14	I/PRELOAD
3	I	15	O
4	I	16	I/O
5	I	17	I/O
6	I	18	I/O
7	I	19	I/O
8	I	20	I/O
9	I	21	I/O
10	I	22	O
11	I	23	I
12	GND	24	V_{CC}

SN54PL20L8 (JT) SN74PL20LB (JT,NT)

functional block diagram



~denotes fused inputs

'PL20R4

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

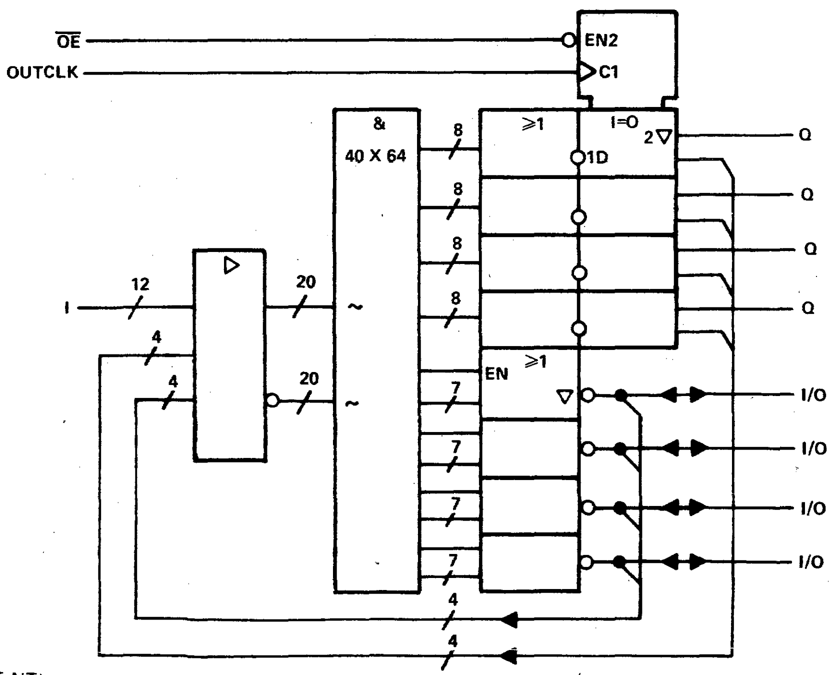
- Quad 20-input registered AND-OR gate array

pin assignments

JT, NT PACKAGES			
1	OUTCLK	13	$\overline{OE}$
2	I	14	I/PRELOAD
3	I	15	I/O
4	I	16	I/O
5	I	17	Q
6	I	18	Q
7	I	19	Q
8	I	20	Q
9	I	21	I/O
10	I	22	I/O
11	I	23	I
12	GND	24	V_{CC}

SN54PL20R4 (JT) SN74PL20R4 (JT,NT)

functional block diagram



~denotes fused inputs

Refer to data sheet in this section for additional information.

See availability at front of this Product Guide.

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'PL20R6

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

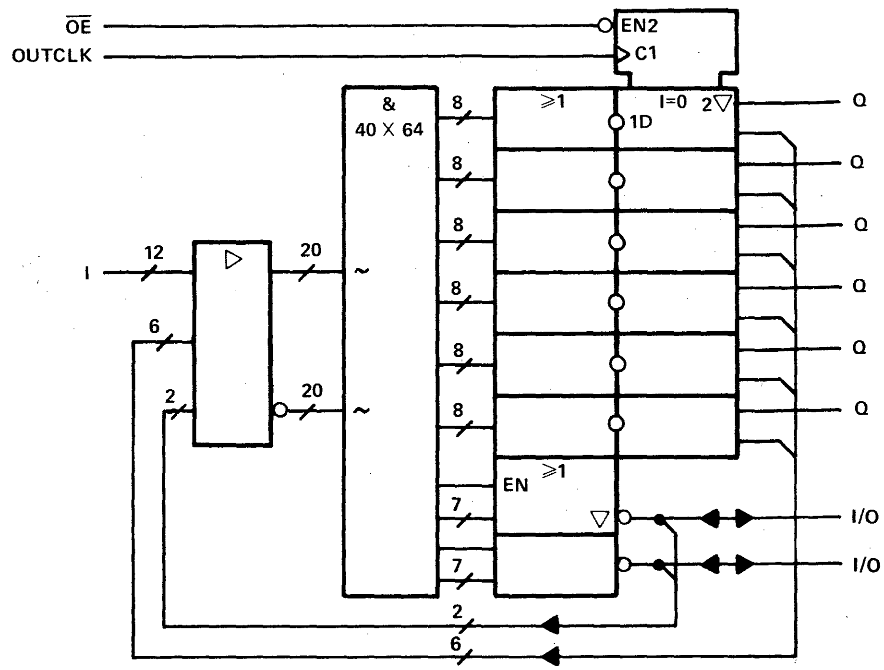
- Hex 20-input registered AND-OR gate array.

pin assignments

JT, NT PACKAGES			
1	OUT CLK	24	V_{CC}
2	I	23	I
3	I	22	I/O
4	I	21	Q
5	I	20	Q
6	I	19	Q
7	I	18	Q
8	I	17	Q
9	I	16	Q
10	I	15	I/O
11	I	14	I/PRELOAD
12	GND	13	$\overline{OE}$

SN54PL20R6 (JT) SN74PL20R6 (JT, NT)

functional block diagram



~ denotes fused inputs.

'PL20R8

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

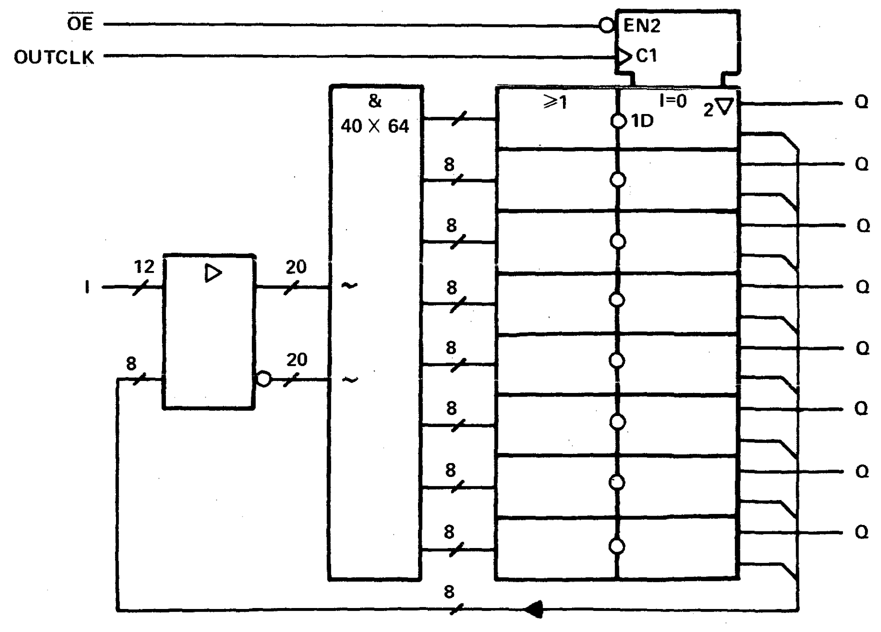
- Octal 20-input registered AND-OR gate array.

pin assignments

JT, NT PACKAGES			
1	OUT CLK	24	V_{CC}
2	I	23	I
3	I	22	Q
4	I	21	Q
5	I	20	Q
6	I	19	Q
7	I	18	Q
8	I	17	Q
9	I	16	Q
10	I	15	Q
11	I	14	I/PRELOAD
12	GND	13	$\overline{OE}$

SN54PL20R8 (JT) SN74PL20R8 (JT,NT)

functional block diagram



~ denotes fused inputs.

Refer to data sheet in this section for additional information.

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'PL839, PL840

FIELD-PROGRAMMABLE LOGIC ARRAYS

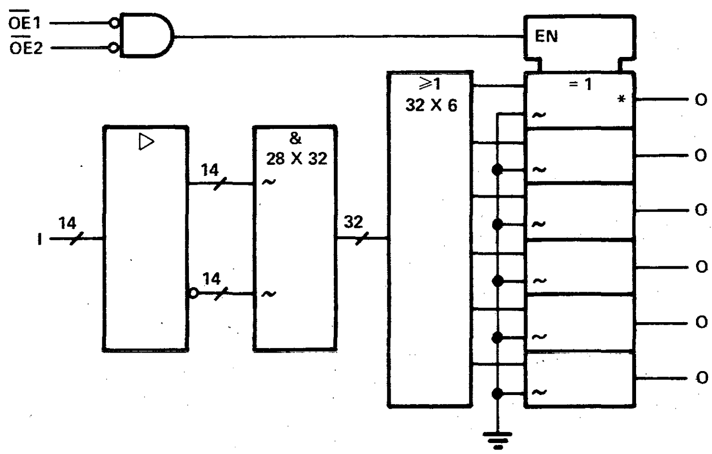
- 'PL839 — three-state outputs
- 'PL840 — open-collector outputs
- Programmable output polarity

pin assignments

J, JT, NT PACKAGES			
1	$\overline{OE1}$	13	$\overline{OE2}$
2	I	14	O
3	I	15	O
4	I	16	O
5	I	17	I
6	I	18	I
7	I	19	I
8	I	20	I
9	O	21	I
10	O	22	I
11	O	23	I
12	GND	24	V_{CC}

SN54PL839 (J) SN74PL839 (JT,NT)
SN54PL840 (J) SN74PL840 (JT,NT)

functional block diagram



~ denotes fused inputs.

* 'PL839 has 3-state (▽) outputs; 'PL840 has open-collector (◇) outputs.

nc — no internal connection.

Refer to data sheet in this section for additional information.

See availability at front of this Product Guide.

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'PLR19L8

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

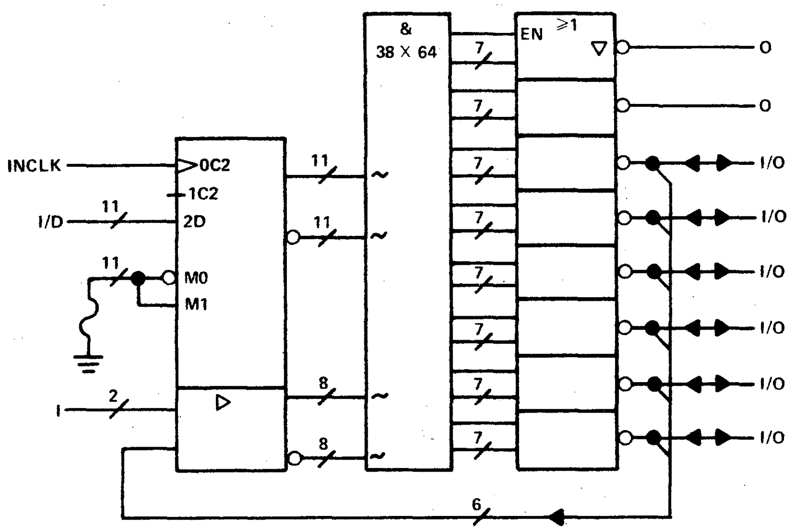
- Octal 19-input registered AND-OR-INVERT gate array

pin assignments

JT, NT PACKAGES			
1	I	13	I
2	I/D	14	INCLK/PRELOAD
3	I/D	15	O
4	I/D	16	I/O
5	I/D	17	I/O
6	I/D	18	I/O
7	I/D	19	I/O
8	I/D	20	I/O
9	I/D	21	I/O
10	I/D	22	O
11	I/D	23	I/D
12	GND	24	V_{CC}

SN54PLR19L8 (JT) SN74PLR19L8 (JT,NT)

functional block diagram



'PLR19R4

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

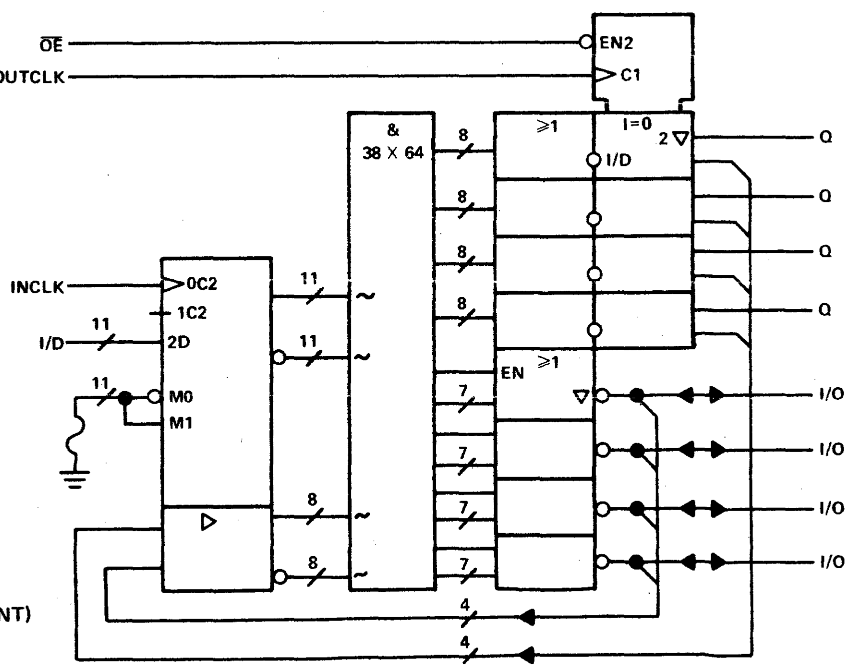
- Quad 19-input registered AND-OR gate array

pin assignments

JT, NT PACKAGES			
1	OUTCLK	13	$\overline{OE}$
2	I/D	14	INCLK/PRELOAD
3	I/D	15	I/O
4	I/D	16	I/O
5	I/D	17	Q
6	I/D	18	Q
7	I/D	19	Q
8	I/D	20	Q
9	I/D	21	I/O
10	I/D	22	I/O
11	I/D	23	I/D
12	GND	24	V_{CC}

SN54PLR19R4 (JT) SN74PLR19R4 (JT,NT)

functional block diagram



Refer to data sheet in this section for additional information.
See Application Note section for additional information on Texas Instruments Bipolar Programmable Logic Arrays.

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'PLR19R6

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

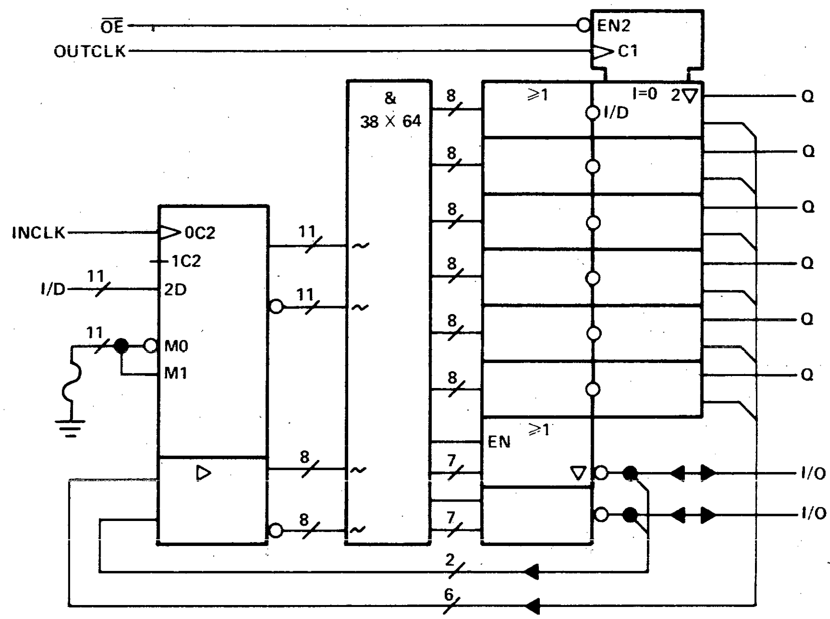
- Hex 19-input registered AND-OR gate array

pin assignments

JT, NT PACKAGES			
1	OUTCLK	13	$\overline{OE}$
2	I/D	14	INCLK/PRELOAD
3	I/D	15	I/O
4	I/D	16	Q
5	I/D	17	Q
6	I/D	18	Q
7	I/D	19	Q
8	I/D	20	Q
9	I/D	21	Q
10	I/D	22	I/O
11	I/D	23	I/D
12	GND	24	V_{CC}

SN54PLR19R6 (JT) SN74PLR19R6 (JT,NT)

functional block diagram



'PLR19R8

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

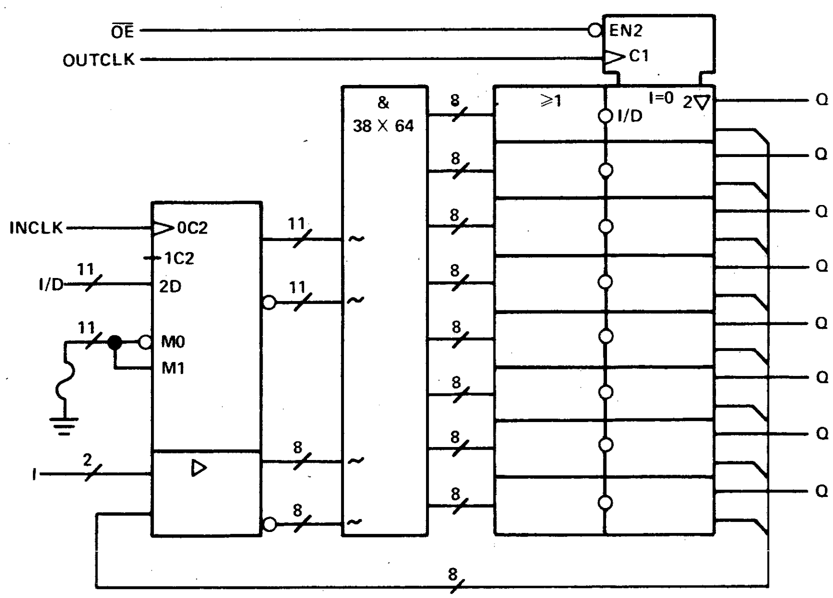
- Octal 19-input registered AND-OR gate array

pin assignments

JT, NT PACKAGES			
1	OUTCLK	13	$\overline{OE}$
2	I/D	14	INCLK/PRELOAD
3	I/D	15	Q
4	I/D	16	Q
5	I/D	17	Q
6	I/D	18	Q
7	I/D	19	Q
8	I/D	20	Q
9	I/D	21	Q
10	I/D	22	Q
11	I/D	23	I/D
12	GND	24	V_{CC}

SN54PLR19R8 (JT) SN74PLR19R8 (JT,NT)

functional block diagram



Refer to data sheet in this section for additional information.

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'PLT19L8

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

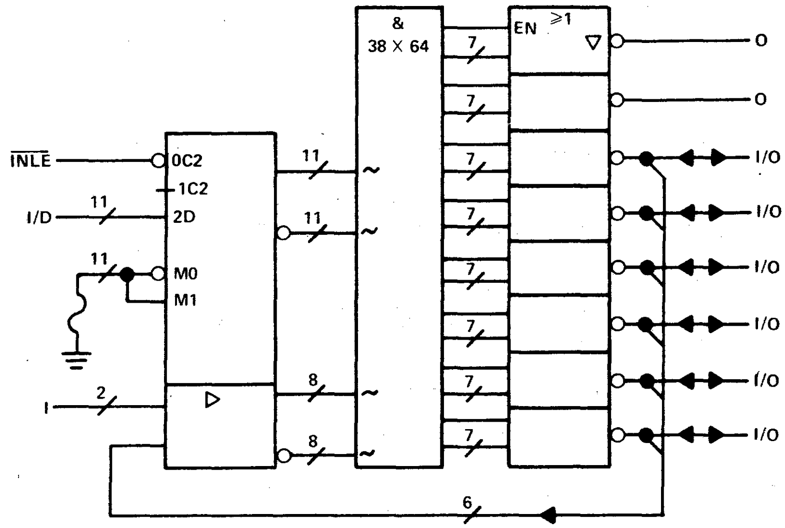
- Octal 19-input latched AND-OR-INVERT gate array

pin assignments

JT, NT PACKAGES			
1	I	13	I
2	I/D	14	$\overline{INLE}$/PRELOAD
3	I/D	15	O
4	I/D	16	I/O
5	I/D	17	I/O
6	I/D	18	I/O
7	I/D	19	I/O
8	I/D	20	I/O
9	I/D	21	I/O
10	I/D	22	O
11	I/D	23	I/D
12	GND	24	V_{CC}

SN54PLT19L8 (JT) SN74PLT19L8 (JT,NT)

functional block diagram



'PLT19R4

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

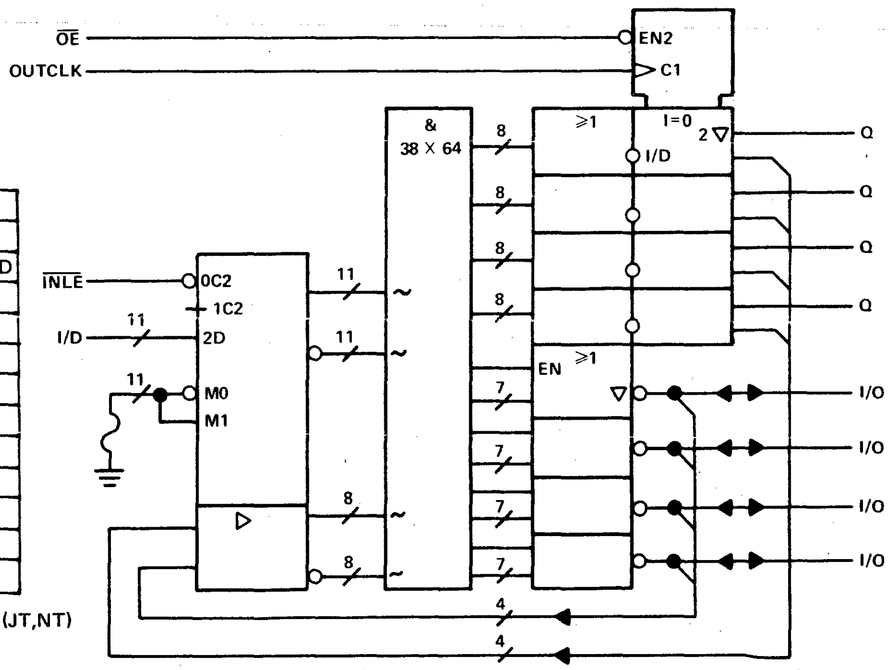
- Quad 19-input registered AND-OR gate array.

pin assignments

JT, NT PACKAGES			
1	OUTCLK	13	$\overline{OE}$
2	I/D	14	$\overline{INLE}$/PRELOAD
3	I/D	15	I/O
4	I/D	16	I/O
5	I/D	17	Q
6	I/D	18	Q
7	I/D	19	Q
8	I/D	20	Q
9	I/D	21	I/O
10	I/D	22	I/O
11	I/D	23	I/D
12	GND	24	V_{CC}

SN54PLT19R4 (JT) SN74PLT19R4 (JT,NT)

functional block diagram



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'PLT19R6

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

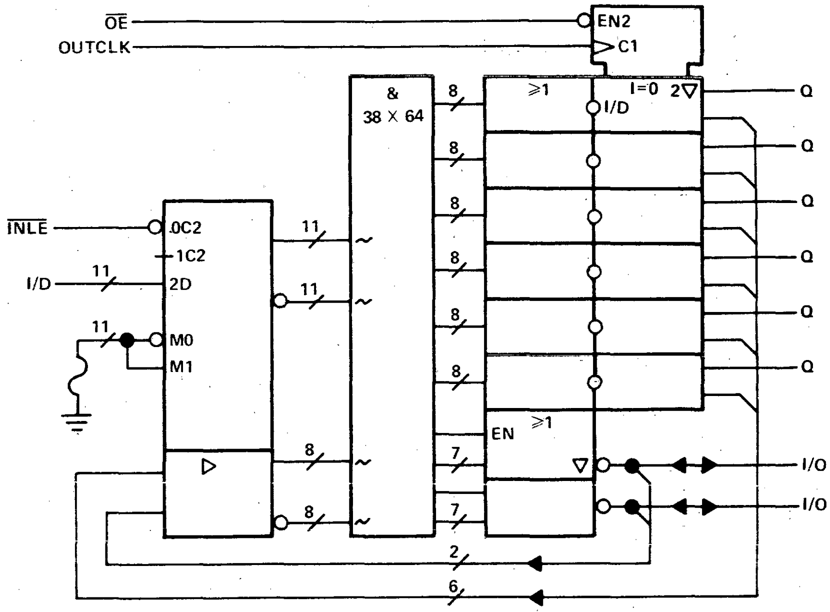
- Hex 19-input latched AND-OR gate array

pin assignments

JT, NT PACKAGES			
1	OUTCLK	13	$\overline{OE}$
2	I/D	14	$\overline{INLE}$/PRELOAD
3	I/D	15	I/O
4	I/D	16	Q
5	I/D	17	Q
6	I/D	18	Q
7	I/D	19	Q
8	I/D	20	Q
9	I/D	21	Q
10	I/D	22	I/O
11	I/D	23	I/D
12	GND	24	V_{CC}

SN54PLT19R6 (JT)   SN74PLT19R6 (JT,NT)

functional block diagram



'PLT19R8

FIELD-PROGRAMMABLE LOGIC, FIXED-OR ARRAYS

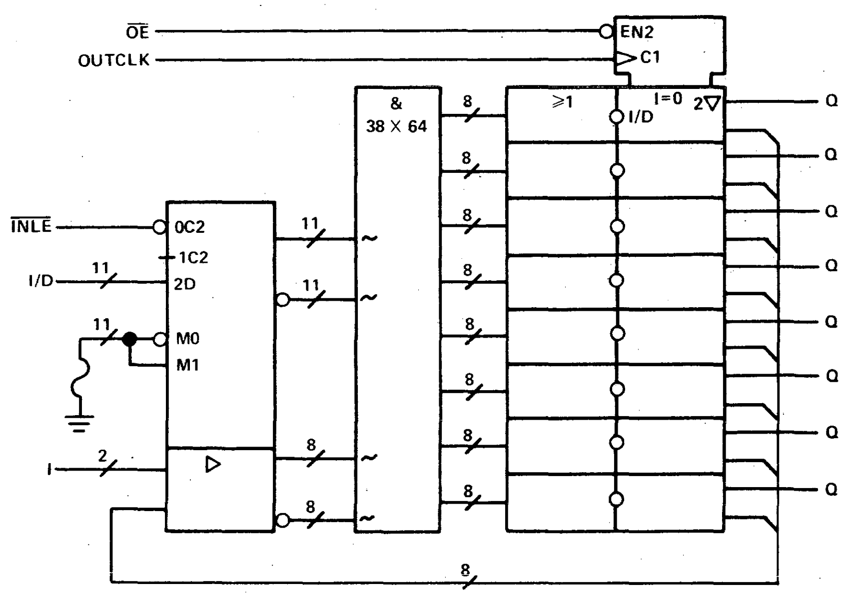
- Octal 19-input latched AND-OR gate array

pin assignments

JT, NT PACKAGES			
1	OUTCLK	13	$\overline{OE}$
2	I/D	14	$\overline{INLE}$/PRELOAD
3	I/D	15	Q
4	I/D	16	Q
5	I/D	17	Q
6	I/D	18	Q
7	I/D	19	Q
8	I/D	20	Q
9	I/D	21	Q
10	I/D	22	Q
11	I/D	23	I/D
12	GND	24	V_{CC}

SN54PLT19R8 (JT)   SN74PLT19R8 (JT,NT)

functional block diagram



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Refer to data sheet in this section for additional information.

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TYPES SN54PL16L8, SN54PL16R4, SN54PL16R6, SN54PL16R8, SN74PL16L8, SN74PL16R4, SN74PL16R6, SN74PL16R8 FIXED-OR ARRAYS

D2705, DECEMBER 1982—REVISED SEPTEMBER 1983

- **Standard 20-Pin, 300-mil Packages**
- **Choice of operating Speeds**
  —1 Parts . . . 35 MHz Max, Standard power
  —2 Parts . . . 25 MHz Max, Half power
- **Plug-In Compatible with Part Numbers: PAL16L8, PAL16R4, PAL16R6, PAL16R8**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PL16L8	10	2	0	6
'PL16R4	8	0	4 (3-state)	4
'PL16R6	8	0	6 (3-state)	2
'PL16R8	8	0	8 (3-state)	0

description

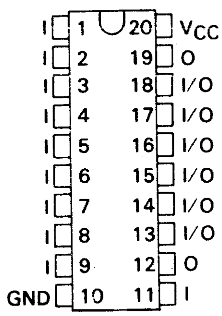
These fixed-OR arrays provide 3-state outputs for bus-oriented systems. They combine Advanced Low-Power Schottky technology with proven titanium-tungsten fuses for reliable, high-performance substitutes for conventional TTL logic. Standard arrays and programmability allow quick design of "custom" functions and more compact boards. The −1 and −2 parts offer a choice of operating frequency, switching times, and power dissipation.

The SN54PL16' is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74PL16' is characterized for operation from 0°C to 70°C.

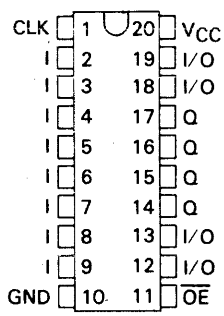
pin assignments in operating mode (voltages at pins 1 and 11 less than V_{IHH})

SN54PL' . . . J PACKAGE
SN74PL' . . . N PACKAGE
(TOP VIEWS)

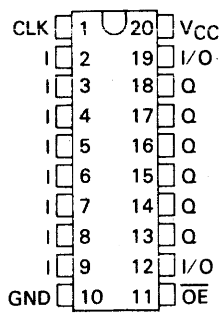
'PL16L8



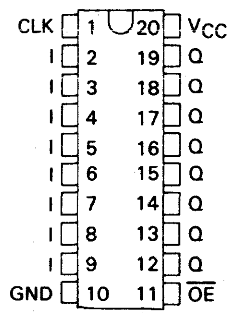
'PL16R4



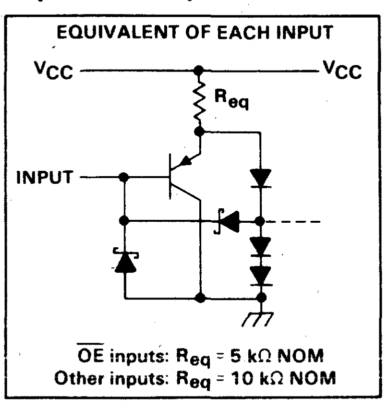
'PL16R6

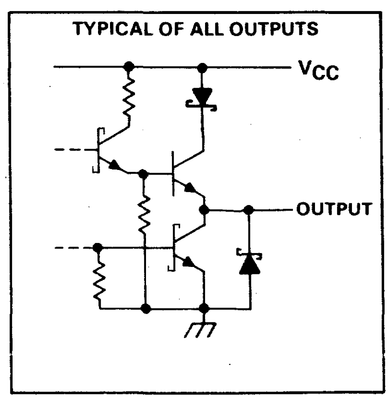


'PL16R8



schematics of inputs and outputs





ADVANCE INFORMATION

This document contains information on a new product. Specifications are subject to change without notice.

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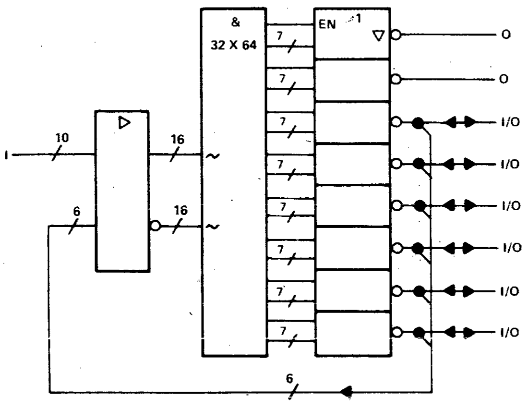
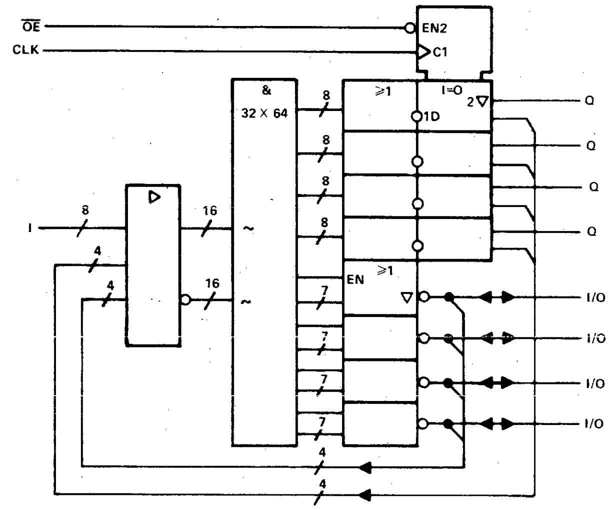
functional block diagrams (positive logic)

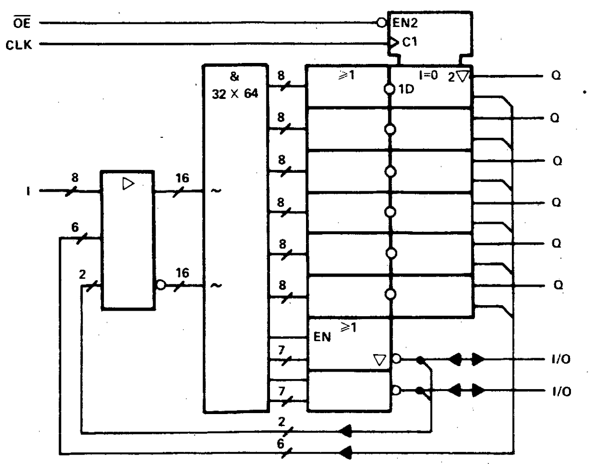
'PL16L8



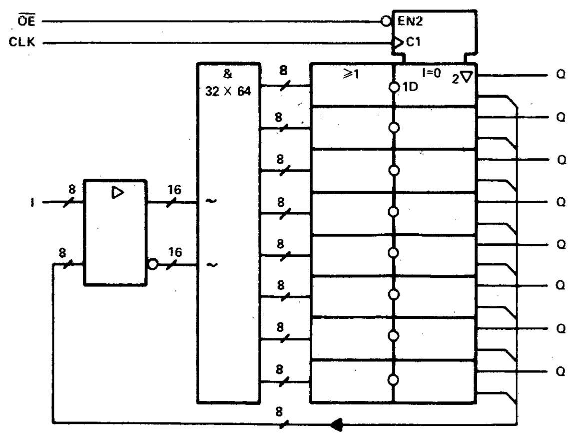
'PL16R4



'PL16R6



'PL16R8



~ denotes fused inputs

See Application Note section for additinal information on Texas Instruments Bipolar Programmable Logic Arrays.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) .... 7 V
Input voltage (see Note 1) .... 5.5 V
Voltage applied to a disabled output (see Note 1) .... 5.5 V
Operating free-air temperature range: SN54PL' .... −55 °C to 125°C
SN74PL' .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER		SN54PL16'			SN74PL16'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2		5.5	2		5.5	V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−3.2	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics, over recommended free-operating temperature range

PARAMETER		TEST CONDITIONS†			SN54PL16'			SN74PL16'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = MIN,	I_{OH} = MAX		2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN,	I_{OL} = MAX			0.25	0.4		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = MAX,	V_O = 2.7 V				20			20	μA
	I/O ports						100			100	
I_{OZL}	Outputs	V_{CC} = MAX,	V_O = 0.4 V				−20			−20	μA
	I/O ports						−250			−250	
I_I		V_{CC} = MAX,	V_I = 5.5 V				0.1			0.1	mA
I_{IH}		V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	$\overline{OE}$ Input	V_{CC} = MAX, V_I = 0.4 V		−1 Parts			−0.4			−0.4	mA
	All others						−0.2			−0.2	
	$\overline{OE}$ Input			−2 Parts			−0.2			−0.2	
	All others						−0.1			−0.1	
I_O§		V_{CC} = MAX,	V_O = 2.25 V		−30		−125	−30		−125	mA
I_{CC}		V_{CC} = MAX, V_I = 0 V, $\overline{OE}$ at 4.5 V, Outputs open		−1 Parts		140	185		140	180	mA
				−2 Parts		75	95		70	90	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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'PL16R4, 'PL16R6, 'PL16R8 timing requirements

		-1 PARTS			-2 PARTS			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
f_{clock}	Clock frequency	0		35				MHz
t_w	Pulse duration, clock high or low	12						ns
t_{su}	Setup time, input or feedback before CLK↑	15						ns
t_h	Hold time, input or feedback after CLK↑	0						ns

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	-1 PARTS			-2 PARTS			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}			$R_L = 500\ \Omega$, $C_L = 50$ pf	35	45			35		MHz
t_{pd}	I, I/O	O, I/O			16	25		32		ns
t_{pd}	CLK↑	Q		7	10	15		20		ns
t_{en}	$\overline{OE}$↓	Q			18	25		36		ns
t_{dis}	$\overline{OE}$↑	Q			10	15		20		ns
t_{en}	I, I/O	O, I/O			18	25		36		ns
t_{dis}	I, I/O	O, I/O			14	25		28		ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

programming parameters, T_A = 25°C

			MIN	NOM	MAX	UNIT
V_{CC}	Verify-level supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
V_{IHH}	Program-pulse input voltage		10.25	10.5	10.75	V
I_{IHH}	Program-pulse input current	PO		20	50	mA
		PBM ENABLE, L/R		10	25	mA
		PI, PA		1.5	5	mA
		V_{CC}		250	400	mA
t_{w1}	Program-pulse duration at PO pins		10		50	μs
t_{w2}	Pulse duration at PGM VERIFY		100			ns
	Program-pulse duty cycle at PO pins				25	%
t_{su}	Setup time		100			ns
t_h	Hold time		100			ns
t_{d1}	Delay time from V_{CC} to 5 V to PGM VERIFY ↑		100			μs
t_{d2}	Delay time from PGM VERIFY ↑ to valid output		200			ns
	Input voltage at pins 1 and 11 to open verify-protect (security) fuse		20	21	22	V
	Input current to open verify-protect (security) fuse				400	mA
	Pulse duration to open verify-protect (security) fuse		20		50	ms

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TYPES SN54PL20L8, SN54PL20R4, SN54PL20R6, SN54PL20R8 SN74PL20L8, SN74PL20R4, SN74PL20R6, SN74PL20R8 FIXED-OR ARRAYS

D2706, DECEMBER 1982 – REVISED SEPTEMBER 1983

- Standard 24-Pin, 300-mil Packages
- Output Registers Have Preload Capability
- Output Registers Automatically Clear During Power-Up
- Choice of Operating Speeds
  - −1 Parts . . . 30 MHz Max, Standard power
  - −2 Parts . . . 20 MHz Max, Half power

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PL20L8	14	2	0	6
'PL20R4	12	0	4 (3-state buffers)	4
'PL20R6	12	0	6 (3-state buffers)	2
'PL20R8	12	0	8 (3-state buffers)	0

description

These fixed-OR arrays provide 3-state outputs for bus-oriented systems. The 'PL20L8, 'PL20R4, and 'PL20R6 have output registers that can be loaded from the I/O pins by a preload procedure. All the outputs are automatically set to a low level when power is applied. The −1 and −2 parts offer a choice of operating frequency, switching times, and power dissipation.

The SN54PL20' is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74PL20' is characterized for operation from 0°C to 70°C.

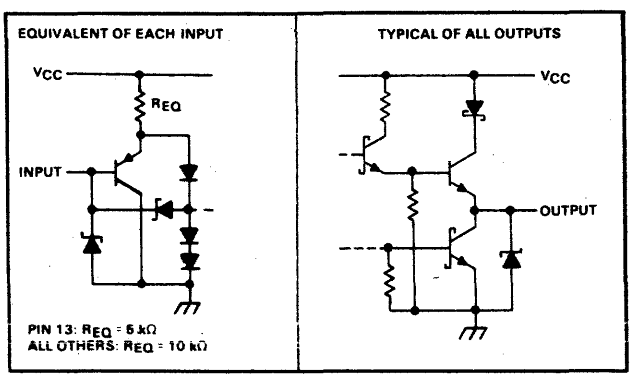
pin assignments in operating mode (voltages at pins 1 and 13 less than V_{IHH})

SN54' ... JT PACKAGE
SN74' ... NT PACKAGE
(TOP VIEW)

Pin	'PL20L8	'PL20R4	'PL20R6	'PL20R8
1	I	OUTCLK	OUTCLK	OUTCLK
2	I	I	I	I
3	I	I	I	I
4	I	I	I	I
5	I	I	I	I
6	I	I	I	I
7	I	I	I	I
8	I	I	I	I
9	I	I	I	I
10	I	I	I	I
11	I	I	I	I
12	GND	GND	GND	GND
13	I	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
14	I*	I*	I*	I*
15	O	I/O	I/O	Q
16	I/O	I/O	Q	Q
17	I/O	Q	Q	Q
18	I/O	Q	Q	Q
19	I/O	Q	Q	Q
20	I/O	Q	Q	Q
21	I/O	I/O	Q	Q
22	O	I/O	I/O	Q
23	I	I	I	I
24	V_{CC}	V_{CC}	V_{CC}	V_{CC}

*Pin 14 is also used for the preload procedure on the last page of this data sheet.

schematics of inputs and outputs



ADVANCE INFORMATION

This document contains information on a new product. Specifications are subject to change without notice.

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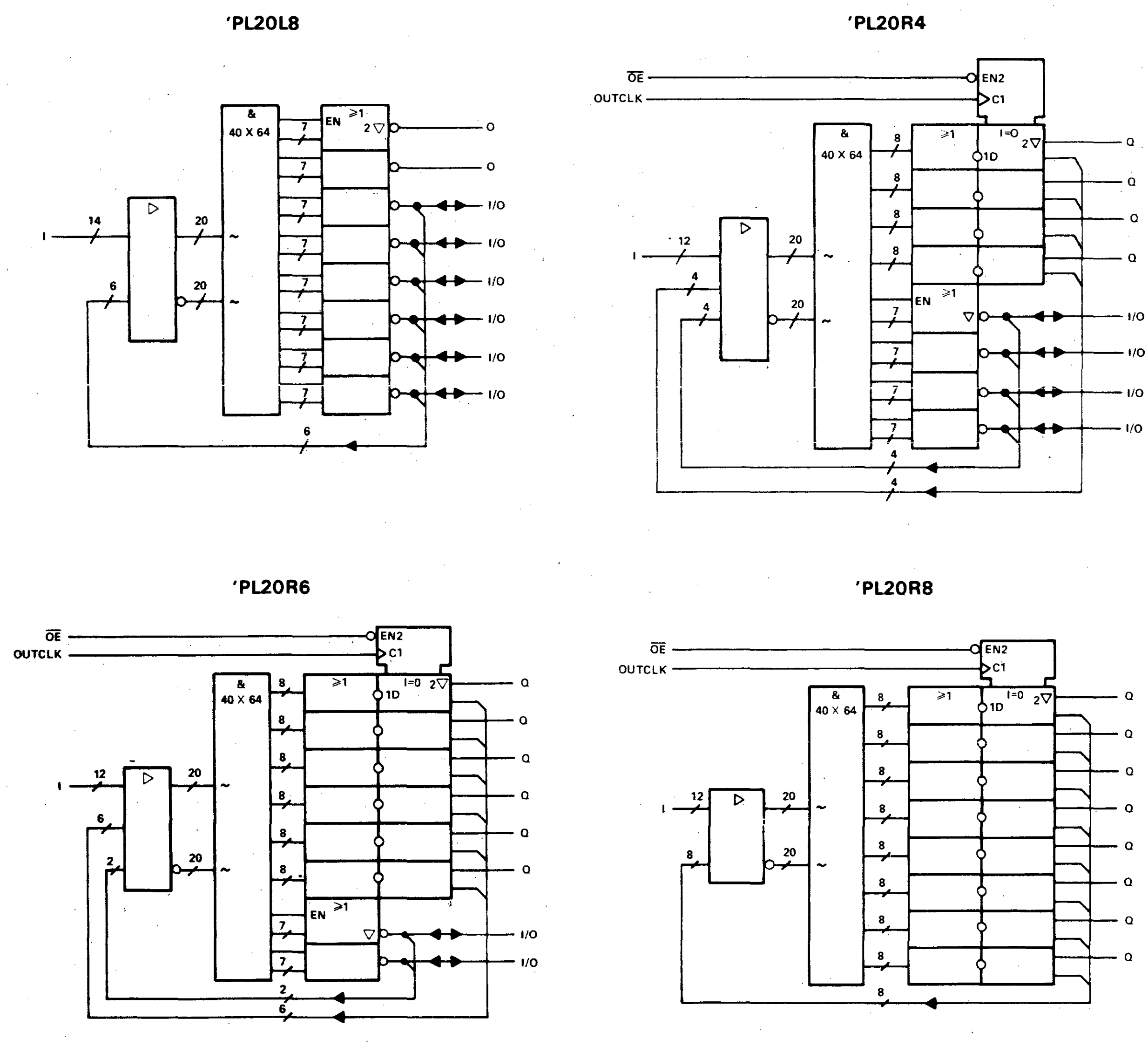
functional block diagrams (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to a disabled output (see Note 1)	5.5 V
Operating free-air temperature range: SN54PL'	−55°C to 125°C
SN74PL'	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during preload cycle.

See Application Note section for additional information on Texas Instruments Bipolar Programmable Logic Arrays.

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recommended operating conditions

		SN54PL19R'			SN74PL19R'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2		5.5	2		5.5	V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−3.2	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS†		SN54PL20'			SN74PL20'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = MIN,	I_{OH} = MAX	2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN,	I_{OL} = MAX		0.25	0.4		0.35	0.5	V
I_{OZH}	O, Q outputs	V_{CC} = MAX,	V_{IH} = 2.7 V			20			20	μA
	I/O ports					100			100	
I_{OZL}	O, Q outputs	V_{CC} = MAX,	V_{IH} = 0.4 V			−20			−20	μA
	I/O ports					−250			−250	
I_I	$\overline{OE}$ Input	V_{CC} = MAX,	V_I = 5.5 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	$\overline{OE}$ Input	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	$\overline{OE}$ Input	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
	All others					−0.2			−0.2	
I_O§		V_{CC} = MAX,	V_O = 2.25 V	−30		−125	−30		−125	mA
I_{CC}	−1 Parts	V_{CC} = MAX,	V_I = 0 V,		150	200		150	200	mA
	−2 Parts	Outputs open,	$\overline{OE}$ at V_{IH}		75	100		75	100	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit current, I_{OS}.

'PL20R4, 'PL20R6, 'PL20R8 timing requirements

		−1 PARTS		−2 PARTS		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	30	0	20	MHz
t_w	Pulse duration, clock high or low	12		12		ns
t_{su}	Setup time, input or feedback before OUTCLK↑	15		15		ns
t_h	Hold time, input or feedback before OUTCLK↑	0		0		ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	−1 PARTS			−2 PARTS			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}				30			20			MHz
t_{pd}	I, I/O	O, I/O	R_L = 500 Ω, C_L = 50 pF		16			25		ns
t_{pd}	OUTCLK↑	Q			12			20		ns
t_{en}	$\overline{OE}$	Q			8			15		ns
t_{dis}	$\overline{OE}$↑	Q			6			12		ns
t_{en}	I, I/O	O, I/O			18			25		ns
t_{dis}	I, I/O	O, I/O			13			20		ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

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PRELOAD PROCEDURES

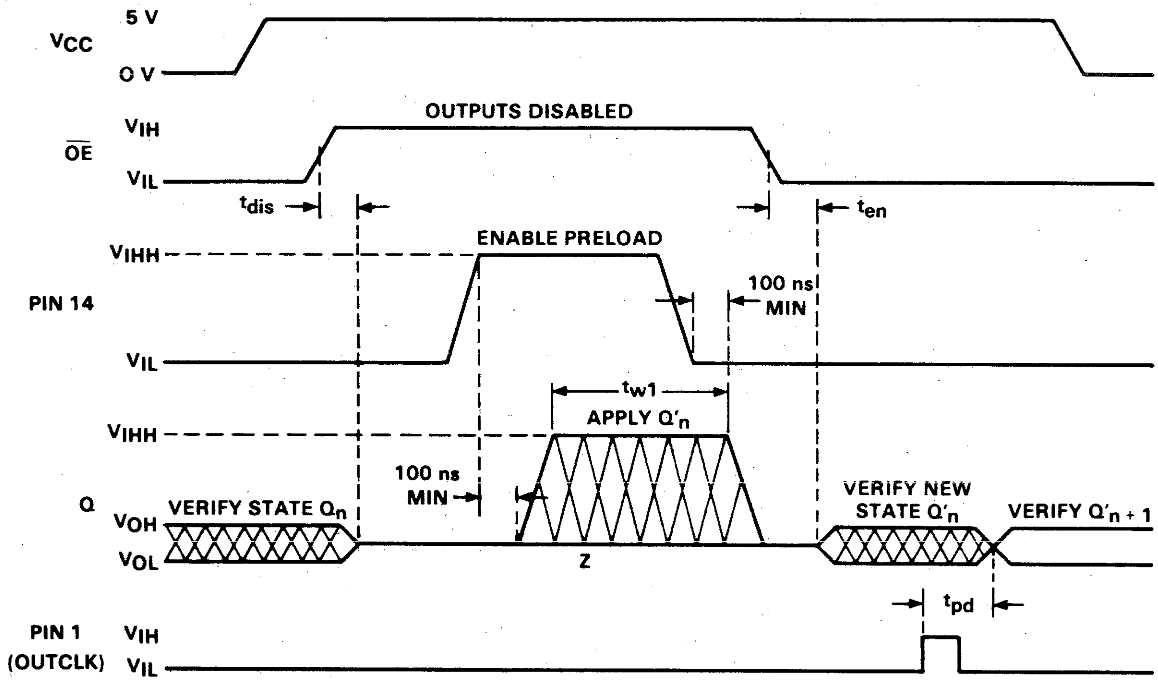


FIGURE 1—PRELOAD WAVEFORMS

preload procedure for registered outputs

Step 1	Pin 13 to V_{IH}, Pin 1 to V_{IL}, and V_{CC} to 5 volts.
Step 2	Pin 14 to V_{IHH} for 10 to 50 microseconds.
Step 3	Apply an open circuit for a low and V_{IHH} for a high at the Q outputs.
Step 4	Pin 14 to V_{IL}.
Step 5	Remove the voltages applied to the outputs.
Step 6	Pin 13 to V_{IL}.
Step 7	Check the output states to verify preload.

TYPES SN54PL839, SN54PL840, SN74PL839, SN74PL840
14 X 32 X 6 FIELD-PROGRAMMABLE LOGIC ARRAYS

D2708, DECEMBER 1982—REVISED SEPTEMBER 1983

- **Input-to-Output Propagation Delay . . . 10 ns Typical**
- **24-Pin, 300-mil Slim Line Packages**
- **Power Dissipation . . . 650 mW Typical**
- **Programmable Output Polarity**

LOGIC FUNCTION

f(I) = P0 + P1 . . . P31 for polarity link intact
f(I) = $\overline{P0}$* $\overline{P1}$* . . . *$\overline{P31}$ for polarity link open
where P0 through P31 are product terms

description

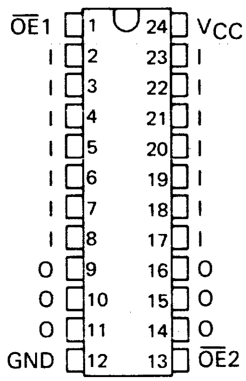
The 'PL839 (3-state outputs and the 'PL840 (open-collector outputs) are TTL field-programmable logic arrays containing 32 product terms (AND terms) and six sum terms (OR terms). Each of the six sum-of-products output functions can be programmed either high or low true. The true condition of each output function is activated by the programmed logical minterms of 14 input variables. The outputs are controlled by two chip-enable pins to allow output inhibit and expansion of terms.

These devices provide high-speed data-path logic replacement where several conventional SSI functions can be designed into a single package.

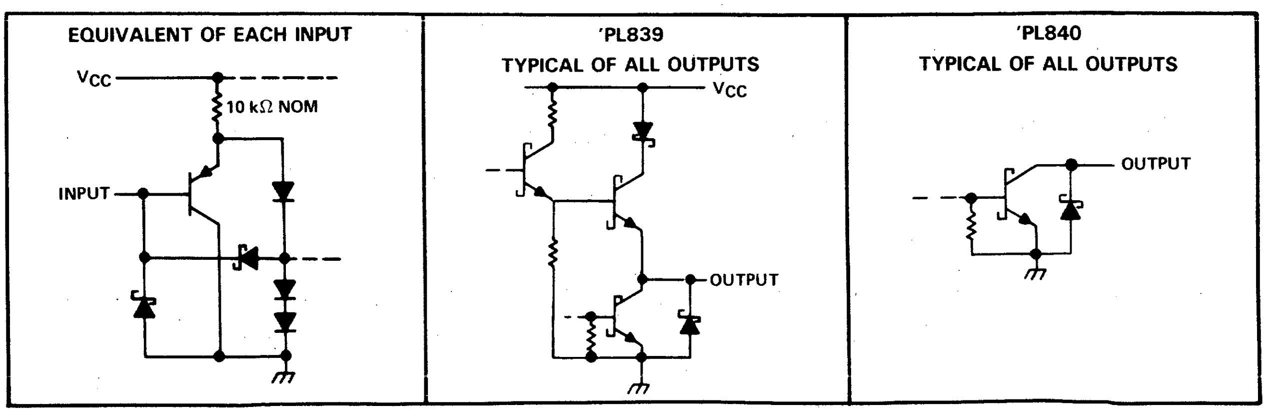
The SN54PL839 and SN54PL840 are characterized for operation over the full military temperature range of −55°C to 125°C. The NS74PL839 and SN74PL840 are characterized for operation from 0°C to 70°C.

pin assignments in operating mode (pin 1 is less than V_{IHH})

SN54PL' . . . JT PACKAGE
SN74PL' . . . NT PACKAGE
(TOP VIEW)



schematics of inputs and outputs



ADVANCE INFORMATION

This document contains information on a new product. Specifications are subject to change without notice.

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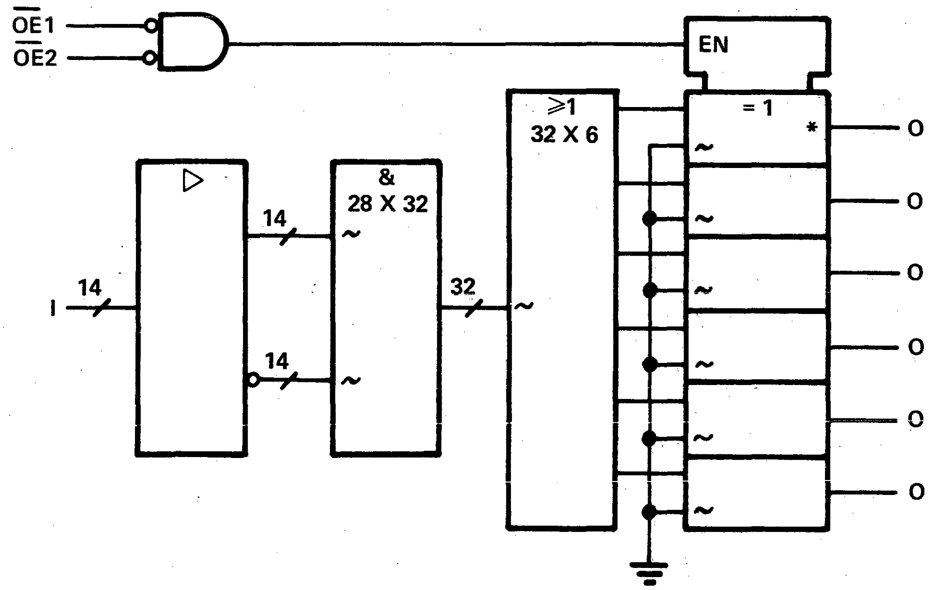
functional block diagram (positive logic)



~ denotes fused inputs.
*'PL839 has 3-state (▽) outputs; 'PL840 has open-collector (◇) outputs.

absolute maximum ratings

Supply Voltage, V_{CC}		7 V
Input Voltage		5.5 V
Off-State Output Voltage		5.5 V
Operating Free-air Temperature Range	SN54PL839, SN54PL840	−55°C to 125°C
	SN74PL839, SN74PL840	0°C to 70°C
Storage Temperature		−65°C to 150°C

See Application Note section for additional information on Texas Instruments Bipolar Programmable Logic Arrays.

recommended operating conditions

	SN54PL'			SN74PL'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			−2			−3.2	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54PL'			SN74PL'			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.2		2.4	3		V
V_{OL}	V_{CC} = MIN,	I_{OL} = MAX		0.25	0.5		0.37	0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_O§	V_{CC} = MAX,	V_O = 2.25 V	−30	−50	−112	−30	−50	−112	mA
I_{OZH}	V_{CC} = MAX,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.4 V			−20			−20	μA
I_{CC}	V_{CC} = MAX, $\overline{OE}$ inputs at V_{IH}	V_I = 0 V,		130	200		130	190	mA

†For conditions shown as MIN or MAX, use the appropriate value spcified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit current, I_{OS}.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	SN54PL'			SN74PL'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	Input	Output	R_L = 500 to GND, C_L = 50 pF to GND		10	25		10	20	ns
t_{en}	Pin 1 or Pin 13	Output	R_{L1} = 500 to 7 V, R_{L2} = 500 to GND, C_L = 50 pF to GND		9	16		9	13	ns
t_{dis}					8	15		8	12	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

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pin assignment in programming mode (pin 1 ≥ V_{IHH}) top views

OUTPUT POLARITY ($PGM\ ENABLE = V_{ILL}$)

Signal	Pin	Pin	Signal
PGM ENABLE	1	24	V_{CC}†
PI1	2	23	PI0
PI2	3	22	PI13
PI3	4	21	PI12
PI4	5	20	PI11
PI5	6	19	PI10
PI6	7	18	PI9
PI7	8	17	PI8
PO5	9	16	PO0
PO4	10	15	PO1
PO3	11	14	PO2
GND	12	13	$\overline{OE}$2

AND MATRIX (V_{CC3})

Signal	Pin	Pin	Signal
PGM ENABLE	1	24	V_{CC}
PI1	2	23	PI0
PI2	3	22	PI13
PI3	4	21	PI12
PI4	5	20	PI11
PI5	6	19	PI10
PI6	7	18	PI9
PI7	8	17	PI8
P0	9	16	PA0
PA4	10	15	PA1
PA3	11	14	PA2
GND	12	13	PGM

OR MATRIX (V_{CC1}, $PA5 = V_{IL}$)

Signal	Pin	Pin	Signal
PGM ENABLE	1	24	V_{CC}
PA1	2	23	PA0
PA2	3	22	PI13
PA3	4	21	PI12
PA4	5	20	PI11
PA5	6	19	PI10
PI6	7	18	PI9
PI7	8	17	PI8
PO5	9	16	PO0
PO4	10	15	PO1
PO3	11	14	PO2
GND	12	13	PGM

†$V_{CC} = V_{CC2}$ for program and V_{CC1} for verify

programming parameters, $T_A = 25°C$

	PARAMETER	MEASURED AT	PROGRAMMING MODE	MIN	TYP	MAX	UNIT
V_{IHH}	Program high-level input voltage	PGM ENABLE	AND, OR	16.5	17	17.5	V
		PO pins	Polarity				
V_{ILL}	Program low-level input voltage	PGM ENABLE	Any	0		0.4	V
I_{IHH}	Program-level input current	PO pins	Polarity		100		mA
		PGM ENABLE	AND, OR		150		
V_{IX}	Program-level input voltage	PO0 thru PO5	Polarity	9.5	10	10.5	V
		PGM	AND, OR				
I_{IX}	Program-level input current	PI pins	AND		0.6	2	mA
		$\overline{OE}$2	Polarity			5	
		PO0 thru PO5	OR		5	10	
V_{CC1}	Programming supply voltage	V_{CC}	OR	8.5	8.75	9	V
I_{CC1}	Programming supply current	V_{CC}	OR		250	400	mA
V_{CC2}	Programming supply voltage	V_{CC}	Polarity		0	0.4	V
V_{CC3}	Programming supply voltage	V_{CC}	AND	4.75	5	5.25	V
V_{IH}	High-level input voltage	Any	Any	2			V
V_{IL}	Low-level input voltage	Any	Any	0		0.8	V
V_{OH}	High-level output voltage	Any	Any	2.4	3.2		V
V_{OL}	Low-level output voltage	Any	Any		0.25	0.5	V
t_w	Program pulse duration	PO0 thru PO5	Polarity		50	1000	μs
		PGM	AND, OR				
	Program pulse duty cycle	PO0 thru PO5	Polarity		10	50	%
		PGM	AND, OR				
t_d	Delay time	Any	Any	10			μs
t_r	Rise time	Any	Any		25		μs

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TYPES SN54PLR19L8, SN54PLR19R4, SN54PLR19R6, SN54PLR19R8 SN74PLR19L8, SN74PLR19R4, SN74PLR19R6, SN74PLR19R8 REGISTERED-INPUT FIXED-OR ARRAYS

D2709, DECEMBER 1982—REVISED SEPTEMBER 1983

- **Standard 24-Pin, 300-mil Packages**
- **Output Registers Have Preload Capability**
- **Output Registers Automatically Clear During Power-Up**
- **Choice of Operating Speeds**
  —1 Parts . . . 30 MHz Max, Standard power
  —2 Parts . . . 20 MHz Max, Half power

DEVICE	I/D INPUTS	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PLR19L8	11	2	2	0	6
'PLR19R4	11	0	0	4 (3-state buffers)	4
'PLR19R6	11	0	0	6 (3-state buffers)	2
'PLR19R4	11	0	0	8 (3-state buffers)	0

description

These fixed-OR arrays with eleven data inputs feature input registers that can be used as they are or be programmed into buffers. Some outputs of the 'PL19R8, 'PL19R6, and 'PL19R4 have registers that can be loaded from the I/O pins by a preload procedure, while others are I/O ports and standard 3-state outputs. All the outputs are automatically set to a low level when power is applied. The −1 and −2 parts offer a choice of operating frequency, switching times, and power dissipation.

The SN54PLR19' is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74PLR19' is characterized for operation from 0°C to 70°C.

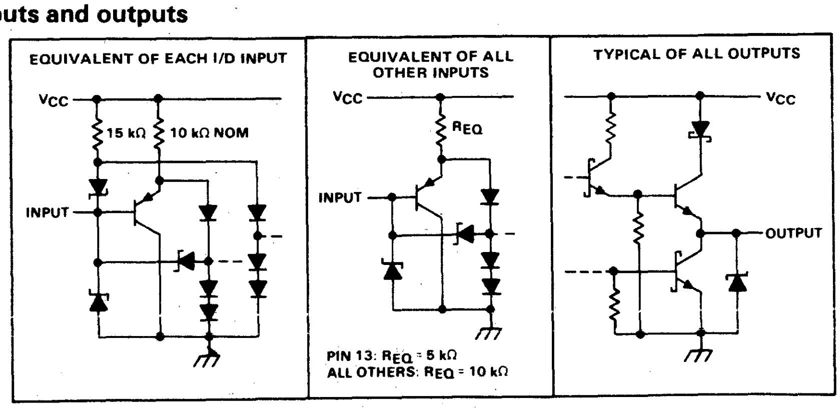
pin assignments in operating mode (voltages at pins 1 and 13 less than V_{IHH})

SN54' ... JT PACKAGE
SN74' ... NT PACKAGE
(TOP VIEW)

PIN	'PLR19L8	'PLR19R4	'PLR19R6	'PLR19R8
1	I	OUTCLK	OUTCLK	OUTCLK
2	I/D	I/D	I/D	I/D
3	I/D	I/D	I/D	I/D
4	I/D	I/D	I/D	I/D
5	I/D	I/D	I/D	I/D
6	I/D	I/D	I/D	I/D
7	I/D	I/D	I/D	I/D
8	I/D	I/D	I/D	I/D
9	I/D	I/D	I/D	I/D
10	I/D	I/D	I/D	I/D
11	I/D	I/D	I/D	I/D
12	GND	GND	GND	GND
13	I	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
14	INCLK*	INCLK*	INCLK*	INCLK*
15	O	I/O	I/O	Q
16	I/O	I/O	Q	Q
17	I/O	Q	Q	Q
18	I/O	Q	Q	Q
19	I/O	Q	Q	Q
20	I/O	Q	Q	Q
21	I/O	I/O	Q	Q
22	O	I/O	I/O	Q
23	I/D	I/D	I/D	I/D
24	V_{CC}	V_{CC}	V_{CC}	V_{CC}

*Pin 14 is also used for the preload procedure on the last page of this data sheet.

schematics of inputs and outputs



ADVANCE INFORMATION

This document contains information on a new product. Specifications are subject to change without notice.

TEXAS INSTRUMENTS
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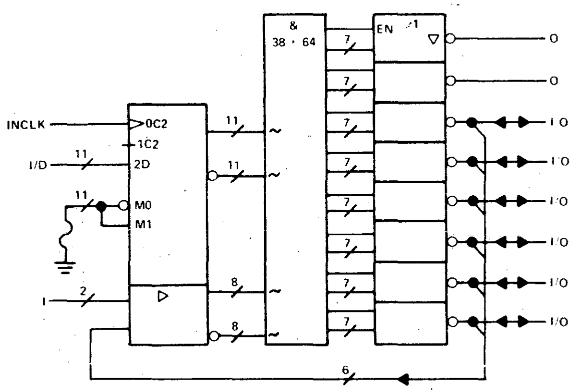
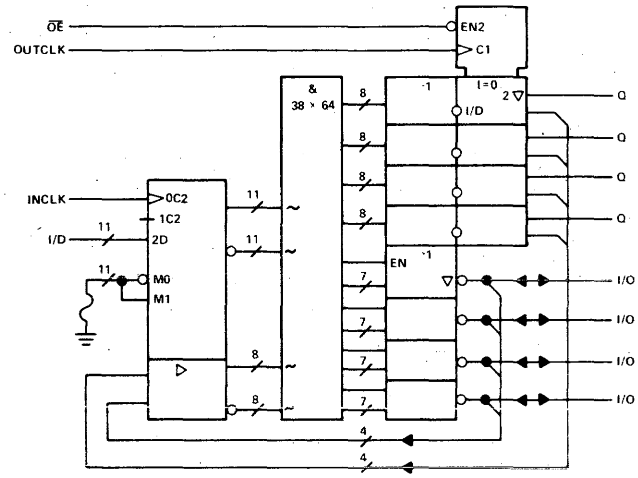
functional block diagrams (positive logic)

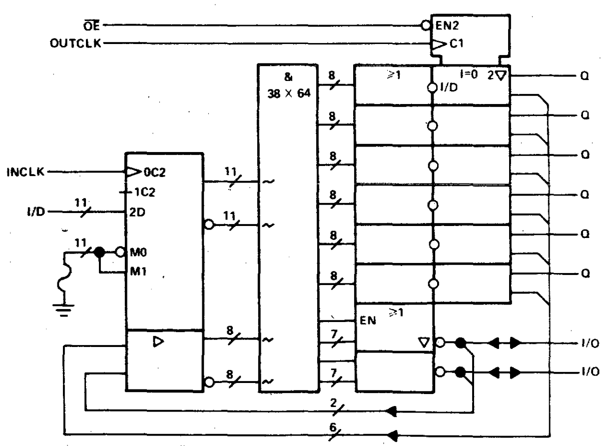
'PLR19L8



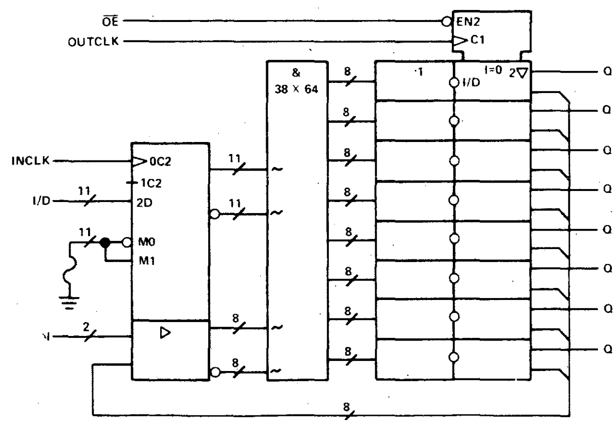
'PLR19R4



'PLR19R6



'PLR19R8



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage (see Note 1)		5.5 V
Voltage applied to a disabled output (see Note 1)		5.5 V
Operating free-air temperature range:	SN54PLR'	−55°C to 125°C
	SN74PLR'	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

See Application Note section for additional information on Texas Instruments Bipolar Programmable Logic Arrays.

recommended operating conditions

		SN54PLR19'			SN74PLR19'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2		5.5	2		5.5	V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−3.2	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS†		SN54PLR19'			SN74PLR19'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = MIN,	I_{OH} = MAX	2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN,	I_{OL} = MAX		0.25	0.4		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = MAX,	V_{IH} = 2.7 V			20			20	μA
	I/O ports					100			100	
I_{OZL}	Outputs	V_{CC} = MAX,	V_{IH} = 0.4 V			−20			−20	μA
	I/O ports					−250			−250	
I_I	OE Input	V_{CC} = MAX,	V_I = 5.5 V			0.2			0.2	mA
	I/D Inputs					0.1			0.1	
	All others					0.1			0.1	
I_{IH}	OE Input	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
	I/D Inputs					20			0.1	
	All others					20			0.1	
I_{IL}	OE Input	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
	I/D Inputs					−0.6			−0.6	
	All others					−0.2			−0.2	
I_O§		V_{CC} = MAX,	V_O = 2.25 V	−30		−125	−30		−125	mA
I_{CC}	−1 Parts	V_{CC} = MAX,	V_I = 0 V,		150	200		150	200	mA
	−2 Parts	Outputs open			75	100		75	100	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit current, I_{OS}.

input timing requirements

		MIN	MAX	UNIT
f_{clock}	Clock frequency	0	40	MHz
t_w	Clock pulse duration, clock high or low	10		ns
t_{su}	Setup time, I/D input before INCLK↑	12		ns
t_h	Hold time, I/D input before INCLK↑	0		ns

'PLR19R4, 'PLR19R6, 'PLR19R8 timing requirements

		MIN	MAX	UNIT
f_{clock}	Clock frequency	0	30	MHz
t_w	Clock pulse duration, clock high or low	12		ns
t_{su}	Setup time, input or feedback before OUTCLK↑	15		ns
t_h	Hold time, input or feedback before OUTCLK↑	0		ns

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	INPUT MODE	TEST CONDITIONS	−1 PARTS			−2 PARTS			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}			Either	$R_L = 500\Omega$, $C_L = 50$ pF	30			20			MHz
t_{pd}	I, I/O	I/O, O	Either				16			25	ns
t_{pd}	OUTCLK↑	Q	Either				12			20	ns
t_{en}	$\overline{OE}$↓	Q	Either				8			15	ns
t_{dis}	$\overline{OE}$↑	Q	Either				6			12	ns
t_{pd}	INCLK↑	I/O, O	Registered				23			32	ns
t_{en}	INCLK↑	I/O, O, Q	Registered				25			35	ns
t_{dis}	INCLK↑	I/O, O, Q	Registered				20			30	ns
t_{pd}	I/D	I/O, O	Buffered				20			30	ns
t_{en}	I/D, I/O	I/O	Buffered				22			32	ns
t_{dis}	I/D, I/O	I/O	Buffered				17			26	ns

†All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

PRELOAD PROCEDURES

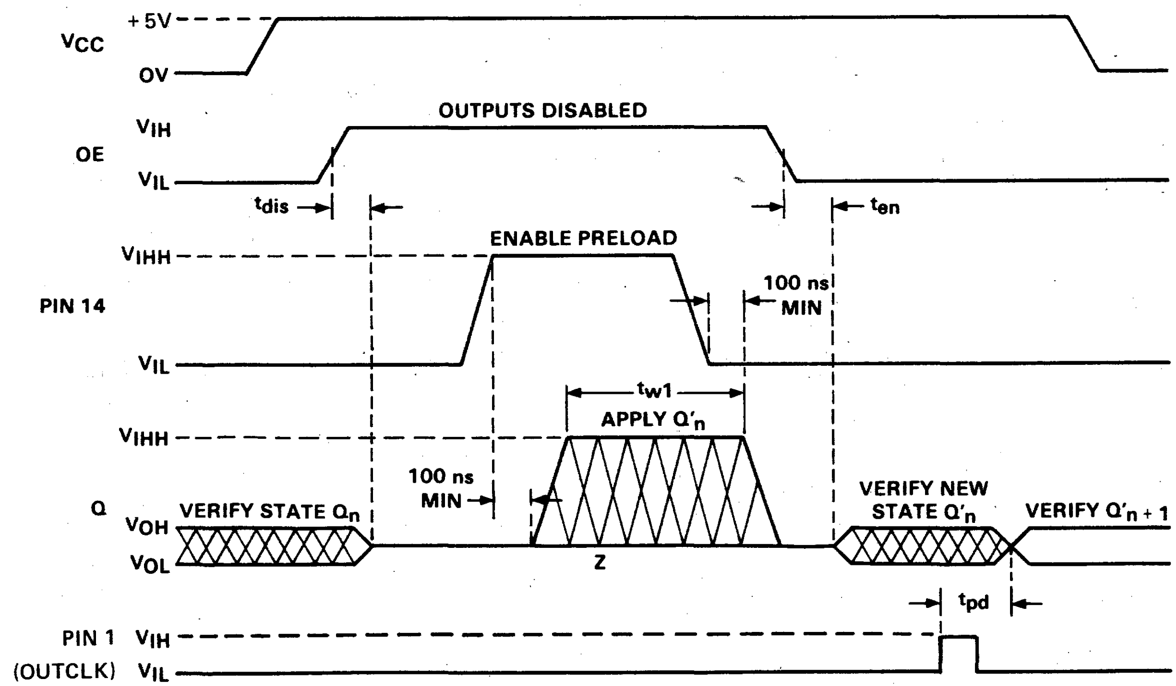


FIGURE 1—PRELOAD WAVEFORMS

preload procedure for registered outputs

Step 1 Pin 13 to V_{IH}, Pin 1 to V_{IL}, and V_{CC} to 5 volts.
Step 2 Pin 14 to V_{IHH}.
Step 3 Apply an open circuit for a low and V_{IHH} for a high at the Q outputs.
Step 4 Pin 14 to V_{IL}.
Step 5 Remove the voltages applied to the outputs.
Step 6 Pin 13 to V_{IL}.
Step 7 Check the output states to verify preload.

TYPES SN54PLT19L8, SN54PLT19R4, SN54PLT19R6, SN54PLT19R8 SN74PLT19L8, SN74PLT19R4, SN74PLT19R6, SN74PLT19R8 LATCHED-INPUT FIXED-OR ARRAYS

D2710, DECEMBER 1982—REVISED SEPTEMBER 1983

- **Standard 24-Pin, 300-mil Packages**
- **Output Registers Automatically Clear During Power-Up**
- **Output Registers Have Preload Capability**
- **Data Input Registers Programmable to Buffers**
- **Choice of Operating Speeds**
  —1 Parts . . . 30 MHz Max, Standard power
  —2 Parts . . . 20 MHz Max, Half power

DEVICE	I/D INPUTS	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PLT19L8	11	2	2	0	6
'PLT19R8	11	0	0	8 (3-state buffers)	0
'PLT19R6	11	0	0	6 (3-state buffers)	2
'PLT19R4	11	0	0	4 (3-state buffers)	4

description

These fixed-OR arrays with eleven data inputs provide input registers that can be used as they are or be programmed into buffers. Some outputs of the 'PLT19R8, 'PLT19R6, and 'PLT19R4 have registers that can be loaded from the I/O pins by a preload procedure, while others are I/O ports and standard 3-state outputs. All the outputs are automatically set to a low level when power is applied. The −1 and −2 parts offer a choice of operating frequency, switching times, and power dissipation.

The SN54PLT19' is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74PLT19' is characterized for operation from 0°C to 70°C.

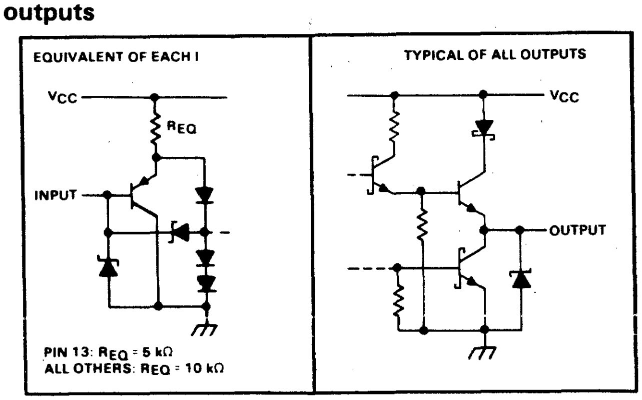
pin assignments in operating mode (voltages at pins 1 and 13 less than V_{IHH})

SN54' ... JT PACKAGE
SN74' ... NT PACKAGE
(TOP VIEW)

PIN	'PLT19L8	'PLT19R4	'PLT19R6	'PLT19R8
1	I	OUTCLK	OUTCLK	OUTCLK
2	I/D	I/D	I/D	I/D
3	I/D	I/D	I/D	I/D
4	I/D	I/D	I/D	I/D
5	I/D	I/D	I/D	I/D
6	I/D	I/D	I/D	I/D
7	I/D	I/D	I/D	I/D
8	I/D	I/D	I/D	I/D
9	I/D	I/D	I/D	I/D
10	I/D	I/D	I/D	I/D
11	I/D	I/D	I/D	I/D
12	GND	GND	GND	GND
13	I	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
14	$\overline{INLE}$*	$\overline{INLE}$*	$\overline{INLE}$*	$\overline{INLE}$*
15	O	I/O	I/O	Q
16	I/O	I/O	Q	Q
17	I/O	Q	Q	Q
18	I/O	Q	Q	Q
19	I/O	Q	Q	Q
20	I/O	Q	Q	Q
21	I/O	I/O	Q	Q
22	O	I/O	I/O	Q
23	I/D	I/D	I/D	I/D
24	V_{CC}	V_{CC}	V_{CC}	V_{CC}

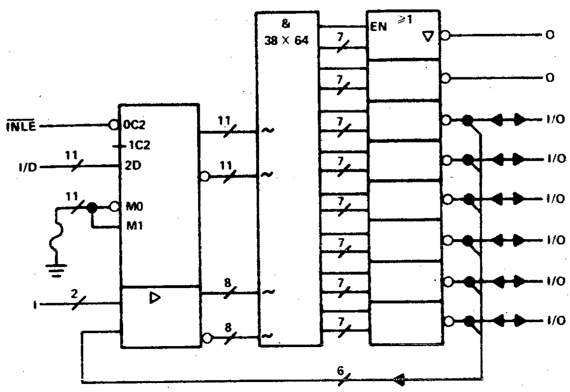
*Pin 14 is also used for the preload procedure on the last page of this data sheet.

schematics of inputs and outputs

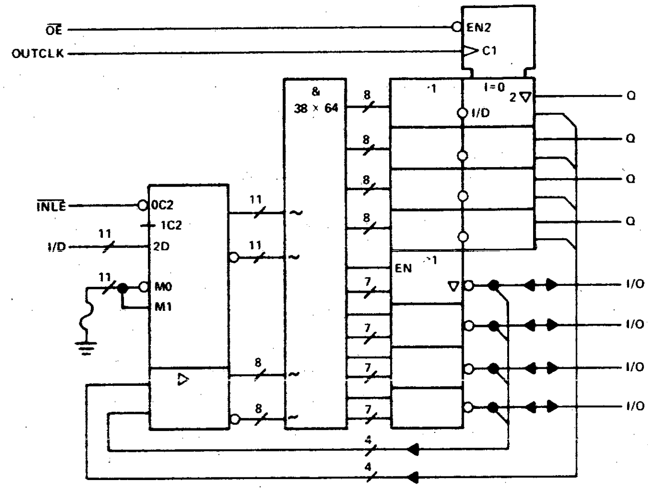


functional block diagrams

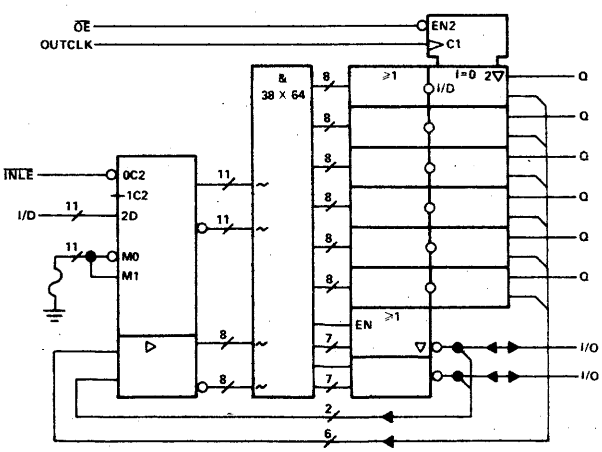
'PLT19L8



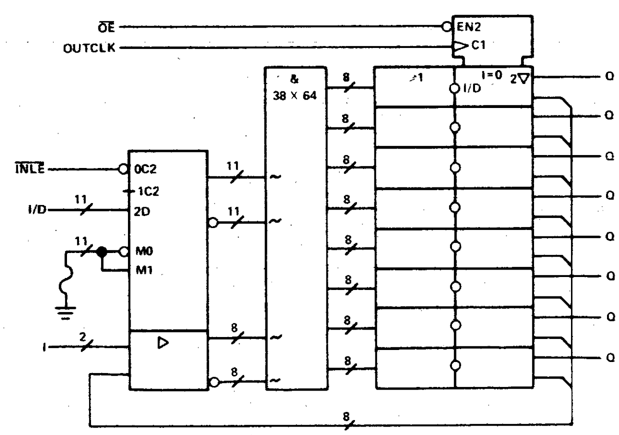
'PLT19R4



'PLT19R6



'PLT19R8



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to a disabled output (see Note 1)	5.5 V
Voltage at any programming pin	12 V
Operating free-air temperature range: SN54PLT'	−55°C to 125°C
SN74PLT'	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

See Application Note section for additional information on Texas Instruments Bipolar Programmable Logic Arrays.

recommended operating conditions

		SN54PLT19'			SN74PLT19'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2		5.5	2		5.5	V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OH}	High-level output current			−2			−3.2	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS†		SN54PLT19'			SN74PLT19'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = MIN,	I_{OH} = MAX	2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN,	I_{OL} = MAX		0.25	0.4		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = MAX,	V_O = 2.7 V			20			20	μA
	I/O ports					100			100	
I_{OZL}	Outputs	V_{CC} = MAX,	V_O = 0.4 V			−20			−20	μA
	I/O ports					−250			−250	
I_I	$\overline{OE}$ Input	V_{CC} = MAX,	V_I = 5.5 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	$\overline{OE}$ Input	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
	All others					20			0.1	
I_{IL}	$\overline{OE}$ Input	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
	All others					−0.2			−0.2	
I_O§		V_{CC} = MAX,	V_O = 2.25 V	−30		−125	−30		−125	mA
I_{CC}	−1 Parts	V_{CC} = MAX,	V_I = 0 V,		150	200		150	200	mA
	−2 Parts	Outputs open			75	100		75	100	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit current, I_{OS}.

'PLT19R8, 'PLT19R6, 'PLT19R4 timing requirements

		−1 PARTS		−2 PARTS		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	30	0	30	MHz
t_w	Clock pulse duration, clock high or low	12		12		ns
t_{su}	Setup time, D input before $\overline{INLE}$↑					ns
t_{su}	Setup time, input or feedback before OUTCLK↑	15		15		ns
t_h	Hold time, input or feedback before OUTCLK↑	0		0		ns

Texas Instruments

CUSTOM/SEMICUSTOM

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	INPUT MODE	TEST CONDITIONS	−1 PARTS			−2 PARTS			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}			Either		30			20			MHz
t_{pd}	I, I/O	I/O, O	Either			16			25		ns
t_{pd}	OUTCLK↑	Q	Either			12			20		ns
t_{en}	$\overline{OE}$↓	Q	Either			8			15		ns
t_{dis}	$\overline{OE}$↑	Q	Either			6			12		ns
t_{pd}	$\overline{INLE}$	I/O, O	Latched			16			25		ns
t_{en}	$\overline{INLE}$	I/O, O, Q	Latched			25			35		ns
t_{dis}	$\overline{INLE}$	I/O, O, Q	Latched			20			30		ns
t_{pd}	I/D	I/O, O	Buffered			20			30		ns
t_{en}	I/D, I/O	I/O	Buffered			22			32		ns
t_{dis}	I/D, I/O	I/O	Buffered			17			26		ns

†All typical values are V_{CC} = 5 V, T_A = 25°C.

PRELOAD PROCEDURES

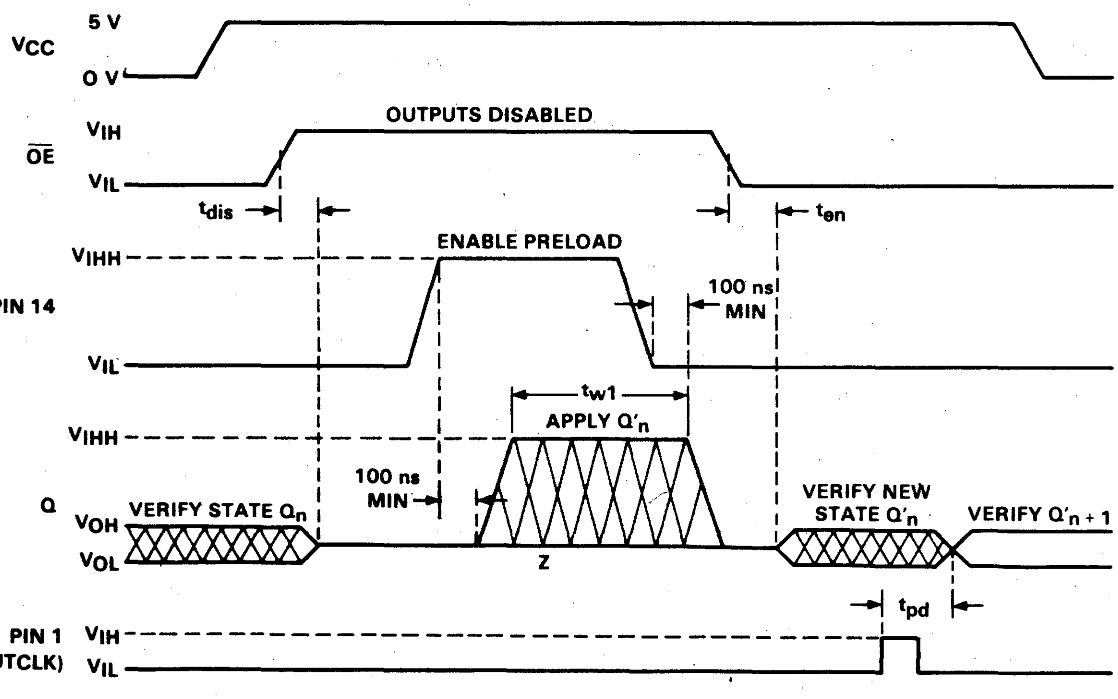


FIGURE 1—PRELOAD VOLTAGE WAVEFORMS

preload procedure for registered outputs

Step 1	Pin 13 to V_{IH}, Pin 1 to V_{IL}, and V_{CC} to 5 volts.
Step 2	Pin 14 to V_{IHH}.
Step 3	Apply an open circuit for a low and V_{IHH} for a high at the Q outputs.
Step 4	Pin 14 to V_{IL}.
Step 5	Remove the voltages applied to the outputs.
Step 6	Pin 13 to V_{IL}.
Step 7	Check the output states to verify preload.

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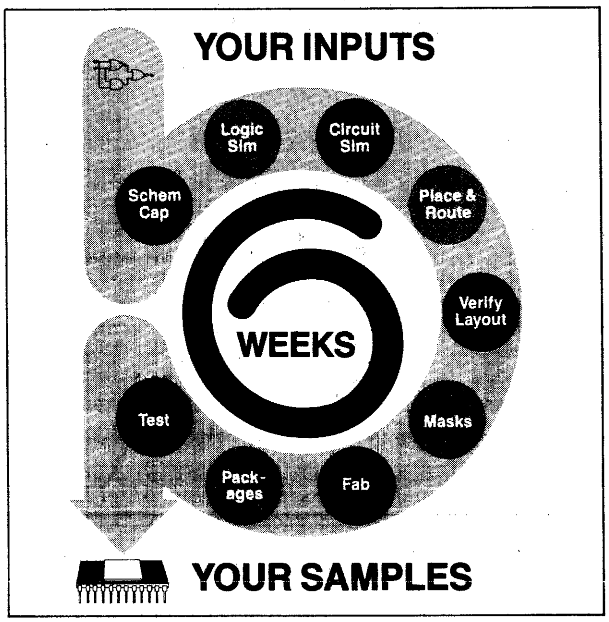

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- **JOINT DEVELOPMENT VENTURES** • With VTI's joint development program, your engineers work with ours at one of our design centers. You provide your systems design expertise; we complement that with our CAE/CAD tools, IC designer support and facilities. Together, we design ICs for your specific applications needs.
- **DESIGN CONSULTATION** • Use VTI's extensive capabilities as a consulting service. You take primary responsibility for your chip design; when you want or need specialized IC design experience, call on us and exploit our VLSI expertise.
- **VTI DESIGNED** • Or call on VTI's full-custom services. Tell our experienced and innovative design engineers your application requirements. We'll analyze your IC needs, and provide the best design solution for you using our computer-aided design system, the most fully-integrated VLSI circuit CAE/CAD system available.

VTI'S SILICON FOUNDRY: WE CALL IT THE SILICON EXPRESS™

So where do you go once you have your custom IC design? How do you turn it into silicon? Before, you had to deal with fabrication services that had high volume requirements. But VTI has changed that for good.

The VTI Silicon Express, our silicon foundry service, accommodates all of your fabrication needs—from prototypes to full production runs. Regardless of your volume requirements, whether you use our design system or design your own chip. And there's something else we give you that was unheard of until now: superfast turn times.

We've invested enormously in our high technology, quick turn wafer fabrication facility. You'll find that our foundry offers you more options, more services and more benefits than any other silicon fabricator.

- **QUICK TURNS** • Usually 14 days from mask entry to wafers out, 21 days to packaged prototypes.
- **ADVANCED PROCESSES** • State-of-the-art CMOS, HMOS and NMOS in a variety of process options.
- **TECHNOLOGY COMPATIBILITY** • Assured for custom ICs designed either with VTI's integrated CAE/CAD system or your own CAD tools.
- **VTInet™** • The electronic foundry network that links you directly with us. Send your CIF, pattern generator or data base files through VTInet. Transmit your data base within hours through a system with built-in safeguards that enforce security and ensure our proprietary obligations to you.

Bring us your designs or your tooling. VTI's Silicon Express—just think of us as your silicon manufacturing arm. We do.

AVAILABLE PROCESSES

Rule	NMOS	HMOS I	HMOS II	CMOS
TRANSISTOR LENGTH (microns)	5	3	2	3
GATE OXIDE (angstroms)	850	650	400	500
SELECTIVE ENHANCEMENT IMPLANT	no	yes	yes	—
CMOS WELLS	—	—	—	N-WELL TWIN-WELL
CONTACT SIZES (microns)	4X4	3X3	2X2	3X3
METAL PITCH	9.0	7.5	6.0	7.0
DUAL METAL	—	1Q84	1Q84	1Q84

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CUSTOM/SEMICUSTOM

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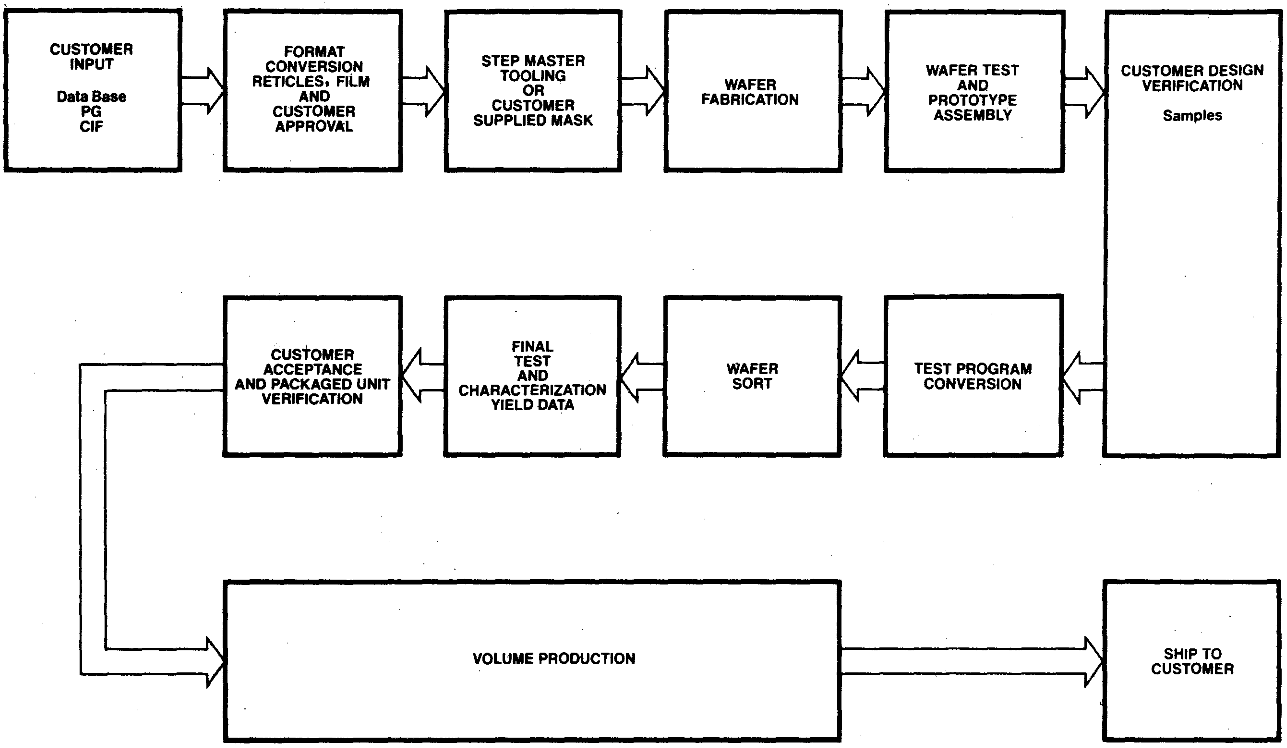
VTI CUSTOMER INTERFACE—THE SILICON EXPRESS



NEW APPROACHES, NEW IDEALS: VTI'S VLSI DESIGN SYSTEM

Times change. We've entered the VLSI technology era. Here today for tomorrow's designs. Until recently, specialized IC design hardware simply didn't have all the capabilities you needed, and cost a fortune. Today, low cost advanced workstations do a better job at a fraction of that cost. VTI has exploited this technological breakthrough to develop a CAE/CAD package which operates on general purpose computers, yet offers higher performance than ever before. And all in a familiar environment, including multiple-windows and mouse-controlled entry:

- Chip planning and schematic capture
- Composition tools
- Cell Compiler libraries
- Logic and timing simulators

We've created a CAE/CAD VLSI design system that involves your specialized knowledge and unique requirements right from the inception of your custom chip. And without requiring MOS/VLSI design expertise. VTI's complete array of VLSI CAE/CAD tools are unparalleled in the industry. After all, we've based these tools on our extensive real-world experience in IC design and manufacture.

So you get the best of all worlds: a set of CAE/CAD tools designed by the premier group of VLSI CAE/CAD programmers in the semiconductor industry—refined and tested under real world conditions before they're released to you. With VTI, you get the high performance and efficiency, proprietary security and long-term economy associated with conventional full-custom design. . . but with the convenience, ease of use and fast turnaround you'd normally expected only from gate arrays.

We offer a tri-level design system. So you get a design system that suits your present needs along with the capability to add increasingly sophisticated features as you require them, when you want them. Flexible, user-friendly, powerful—VTI's state-of-the-art VLSI integrated design system.

TRAILBLAZING THE VLSI FUTURE

VTI OFFERS A CHOICE OF DESIGN APPROACHES

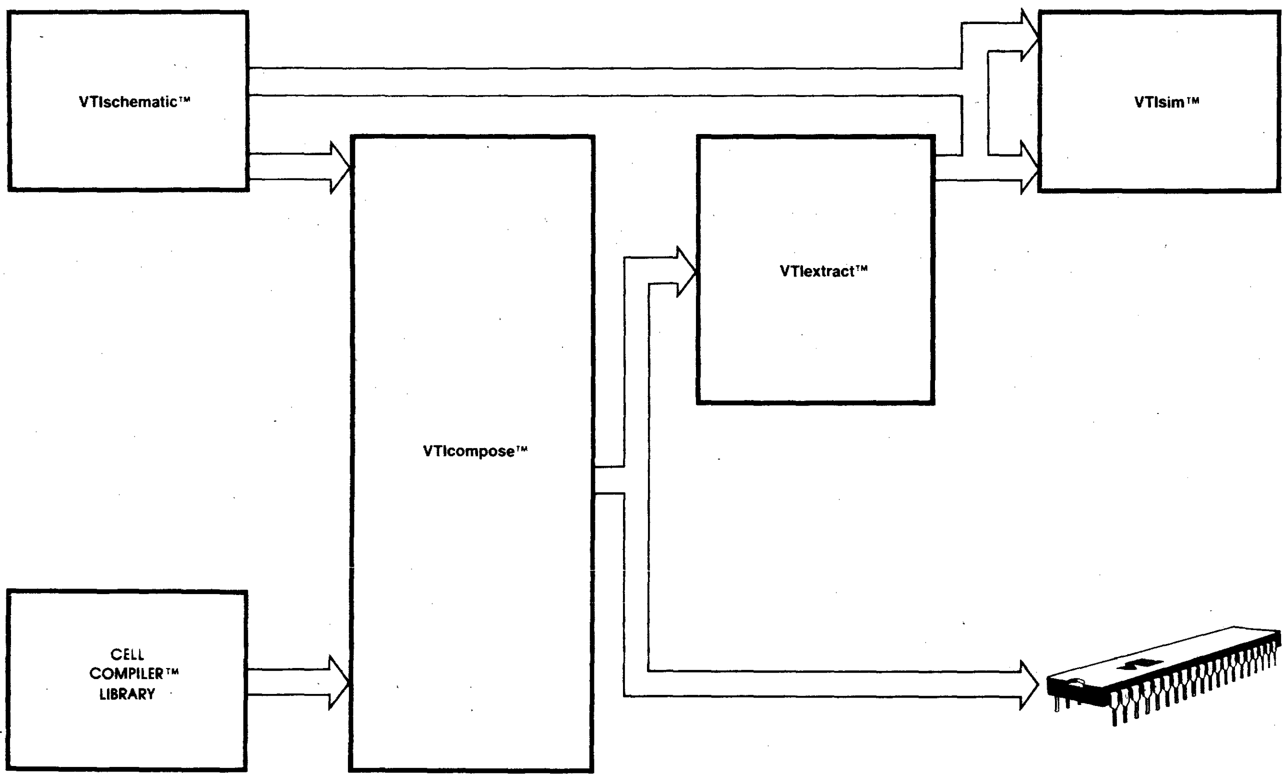
Design Approach	User	Benefits
LEVEL 1 LOGICOMP™	Logic and Systems Engineer	▪ Easy to Learn ▪ Very Rapid Design
LEVEL 2 SYMCAD™	Systems and IC Designer	▪ Unique Cell Design ▪ Higher Performance
LEVEL 3 GEOCAD™	Experienced IC Designer	▪ Lowest Cost ▪ Highest Performance

LOGICOMP: DESIGN TOOLS THAT SPEAK YOUR LANGUAGE

VTI's LOGICOMP design system gives you, the systems designer, access to the most fully-integrated and sophisticated CAD tools in the industry. Whether or not you've ever designed an IC before, LOGICOMP serves as an accessible, highly-efficient package that includes all the CAD tools you need to:

- Enter a system schematic
- Construct a corresponding physical layout from predefined functional elements in VTI's Cell Compiler library
- Verify interconnection and function correctness of the physical layout, as specified by your schematic representation
- Automatically route all interconnects

LOGICOMP LOGIC COMPILER™ SYSTEM



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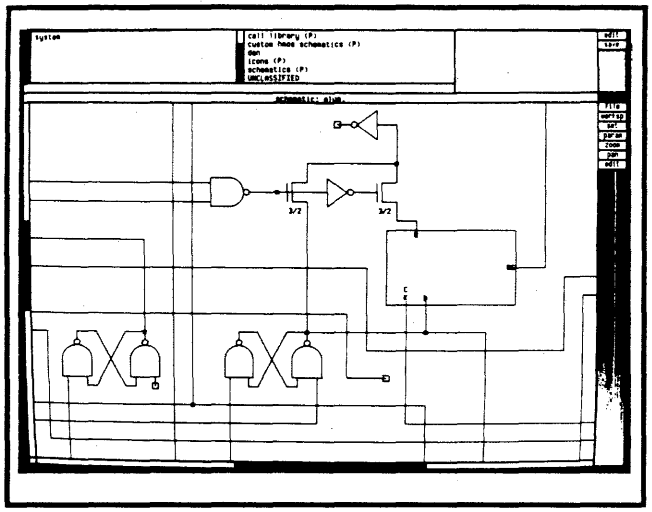
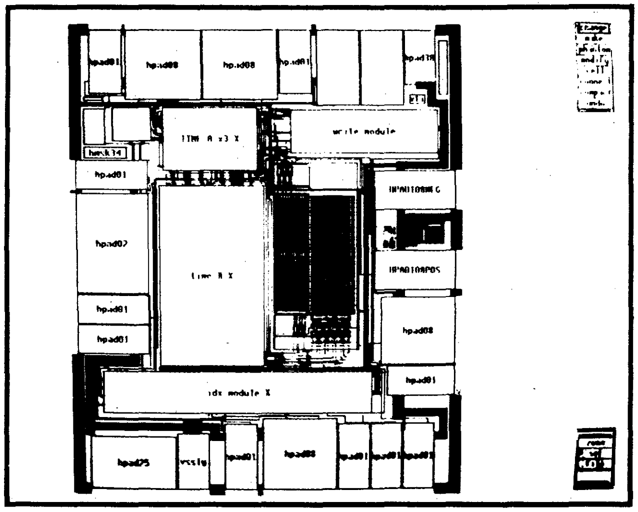
CUSTOM/SEMICUSTOM

TRAILBLAZING THE VLSI FUTURE

VTI'S COMPOSITION EDITOR



VTI'S SCHEMATIC EDITOR



CELL COMPILERS: BUILDING BLOCKS FOR YOUR SYSTEM

VTI's unique Cell Compiler library—a concept that offers you ready-to-use functional elements to design your chip. Sounds like a standard cell library? Most people think so too, at first. Until they realize that VTI's Cell Compiler library offers the most advanced alterable set of cells available. Our Primary and Extended cell libraries compile physical layout databases for simple and complex IC building blocks. And we offer them in CMOS as well as HMOS. You specify the cell characteristics before compiling to physical layout. So you get a library with thousands of cell variations. Far more than the few hundred that conventional standard cell libraries offer.

With VTI's Cell Compilers, you specify your IC's unique requirements such as circuit speed, drive capability, data path width and functional repetition. What's more, with automatic cell layout generation, you don't need first-hand knowledge of MOS design rules or specific process details.

CELL COMPILER FUNCTIONS

VTS810: Primary Library
AND/NAND Gates
Clock Generators
Exclusive OR/NOR Gates
Flip-Flops
Input Buffers
Inverting Buffers
OR/NOR Gates
Quasi-Static Latches
3-State Buffers
TTL I/O Buffers

VTS820: Extended Library
Adders/Subtractors
ALUs
Counters
Data Demultiplexers
Data Multiplexers
Full Adders
Pad-Ring Generators
PLA Generators
RAM Generators
ROM Generators
Shift Registers
Up/Down Counters

SYMCAD: BETTER CAD, LOWER COST

Your system design requires an IC made up of cells that simply don't exist. You could settle for a chip that's been glued together and works; but you'd like to design your own cells. You want a custom VLSI circuit that performs exactly the way you want it to, consumes the minimal power and takes only as much (or as little) room as necessary.

Obviously, you want access to a custom VLSI CAD system. Specifically, an interactive symbolic design package. And you'd prefer one without having to deal with awkward grids. Well, that system exists and is available to you. It's called SYMCAD: VTI's SYMbolic CAD system.

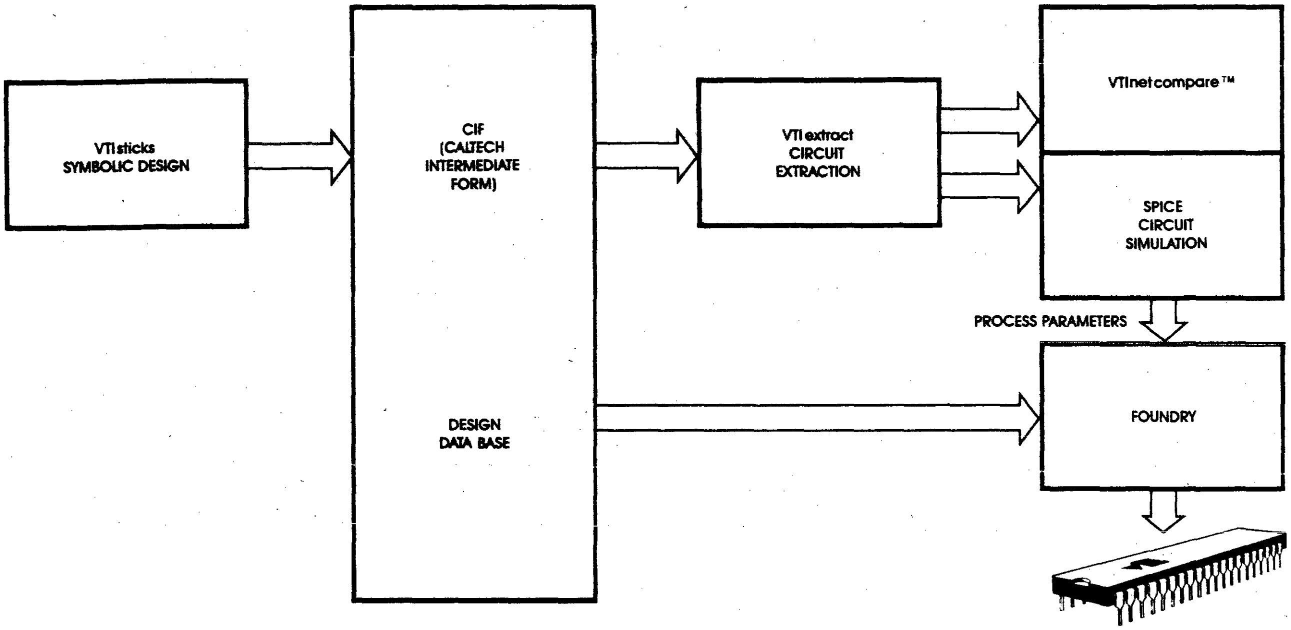
SYMCAD offers you:

- VTIsticks™ editor
- VTIextract™—Circuit function and evaluation tool
- ERC—Electrical Rule Checker

A variety of features, integrally connected. The ideal way to design your system's components. SYMCAD: heralding your VLSI design future.

TRAILBLAZING THE VLSI FUTURE

SYMCAD SYMBOLIC COMPUTER-AIDED DESIGN SYSTEM



VTIsticks : THE KEY TO PRODUCTIVITY THROUGH SYMBOLIC DESIGN

You've been locked out of the IC design phase for your system. That is, up until today. Now, VTIsticks opens the door that's kept you from designing the chip you need. VTIsticks gives you total control over every facet of your system design. That's how it should have been. That's how it can be now. VTI's cell design tool automatically generates your IC layouts in compliance with user-specified design rules. Most importantly, the system is simple to use. You only have to specify the chip topology symbolically; then VTIsticks converts your IC design to layout and compacts it to the minimal size. The benefit? Immediate custom MOS/VLSI circuit design capability without detailed knowledge of MOS/VLSI design techniques. And with assured results everytime.

VTIsticks features:

- Automatic conversion from VTIsticks to layout
- Automatic compaction to the minimum size allowed by design rules
- User-defined constraints on IC compaction
- Automatic recognition and placement of contacts
- Transistor size display and editing
- Symbolic naming

VTIsticks automatically recognizes and places contacts between layers and transistors. And VTIsticks' pop-up menus and mouse input provide you with an efficient way to enter your design. With VTIsticks, you virtually eliminate keyboard entry in the layout phase of IC design.

With VTIsticks, you'll create new cells that are nearly as dense as those laid out by hand. Even with those industry-unique features, VTIsticks is easy-to-learn and easy-to-use. Your design will cost you less time, effort and money.

GEOCAD PHYSICAL LAYOUT EDITOR: GETTING THE SMALLEST CELLS POSSIBLE

VTI's Physical Layout Editor, GEOCAD, is the premier interactive graphics tool for developing the most compact custom cells while maximizing performance. VTI allows you to design with arbitrary geometries. Once you've completed your design, the design rules can be verified with VTIdrc and the layout against the original logic design using VTIextract and VTIcompare.

Using GEOCAD is easy. You gain access through multiple windows whose sizes and positions you define. And then draw the graphics with a mouse.

The Layout Editor features:

- Any angle lines, any angle polygons
- Predefined and user-defined macros
- Edit-by-layer capability
- Cut, paste and edit commands, both within a window and between windows

VTI DESIGN CENTERS: PROVIDING DESIGN FACILITIES AND CONSULTING SERVICES

We're putting all our design tools in your neighborhood—so you can reap the benefits of custom design. Use one of VTI's Design Centers as your own. We've staffed each of them with applications engineers, all of whom are ready to assist you in every way with chip design requirements and software support.

Our design centers are located at:

- 2235 Qume Drive
San Jose, CA 95131
408-943-0264
- 83 Cambridge Street
Burlington, MA 01803
617-229-6555
- 850 East Arapaho Road
Richardson, TX 75081
214-387-8350
- Via G. Jervis, 77
10015 Ivera (To)
Italy
39-125-52-2010

You can come to our training classes. In less than two weeks, our VLSI Design Training Program will teach you the complexities and the simplicity of VTI's CAE/CAD design tools. In fact, by the end of your first week in Level 1, you'll be ready to design your own custom IC with VTI's unique Cell Compiler library. In Level 2, you'll learn the latest in MOS/VLSI design principles and the use of the VTIsticks graphics editor so you can design your own custom ICs. Our Level 3 course teaches you how to design your own Cell Compiler library as well as advanced layout editing techniques and advanced packaging and test considerations.

VLSI TRAINING, TOOLS AND SERVICES FROM VTI. INTENSIVE. FAST. COMPREHENSIVE.

VLSI technology. An idea that's become a reality. With VTI, you'll take a step-by-step path to macrocell-based VLSI design nurtured by the experience and innovative prowess of a leading full-service VLSI semiconductor company. Whether you only need design training, our exciting design tools, or want the services of our designers or silicon foundry, you'll get the highest performance, the most efficient design combined with the latest knowledge in the semiconductor state-of-the-art.

After all, that's how VLSI technology is defined.

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ABBREVIATIONS OF COMPANY NAMES

Action Ins	Action Instruments
AD	Analog Devices
ADT	Advanced Digital Technology
Advent	Advent Products, Inc.
Alphatron	Alphatron
AMA	American Automation
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
Amperex	Amperex Electronic Corp.
Analogic	Analogic
Analog Sys	Analog Systems
APC	Applied Micro Circuits
Apex	Apex Microtechnology
APM	Applied Microsystems Corp.
Appl Sys	Applied Systems Corp.
APT	Applied Microtechnology
Aptek	Aptek Microsystems
Array Tech	Array Technology
AWI	AWI Electronics
Barvon	Barvon Research
Bedford	Bedford Computer Systems Inc.
Burr-Brown	Burr-Brown
CAE	Computer Aided Engineering
Cal Devices	California Devices
Cermetek	Cermetek
CGRS	CGRS Microtech Inc.
Cherry	Cherry Semiconductor
CIC	Custom Integrated Circuits
CirTech	Circuit Technology
Citel	Citel
Comlinear	Comlinear Corporation
CMA	Custom MOS Arrays
Comark	Comark Corp.
Comdial	Comdial Semiconductor
Comp Auto	Computer Automation
Compas	Compas Microsystems
Cont Logic	Control Logic Inc.
Control Sys	Control Systems Microsystems Div.
CreMicro	Creative Micro Systems
Cromemco	Cromemco, Inc.
Cubit	Cubit Inc.
Curtis	Curtis Electro Devices, Inc.
Cybernetic	Cybernetic Micro Systems
Cybersys	Cybersystems
Cybertek	Cybertek Inc.
Data General	Data General
Data I/O	Data I/O
Data Trans	Data Translation
Datel	Datel
Datricon	Datricon Corporation
DDC	Data Devices Corporation
DEC	Digital Equipment Corporation
Die-Tech	Die-Tech
Digelec	Digelec Corp.
Digitek	Digitek, Inc.
Dionics	Dionics Inc.
Dist Comp	Distributed Computer Systems
Divers Tech	Diversified Technology
E-HI	E-H International, Inc.
EDI	Electronic Designs Inc.
Elind	Elind Elettronica Industriale
EMM-SESCO	EEM-SESCO
Emulogic	Emulogic Inc.
ETI Micro	ETI Micro
Exar	Exar Integrated Systems
Exel	Exel Microelectronics
Fairchild	Fairchild
Ferranti	Ferranti Electric
Force	Force Computers
Fujitsu A	Fujitsu America
Fujitsu	Fujitsu Microelectronics, Inc.
GI	General Instrument
GTE Micro	GTE Microcircuits
Harris	Harris Semiconductor
Heurikon	Heurikon Corp.
Hilevel	Hilevel Technology, Inc.
Hitachi	Hitachi America, Ltd.
Holt	Holt Inc.
HP	Hewlett-Packard
Hughes	Hughes Aircraft, Solid State Products
Hybrid Sys	Hybrid Systems
HyComp	HyComp
ICC	International Cybernetics
IDT	Integrated Device Technology
IMI	International Microcircuits, Inc.
IMP	International Microelectronic Products
IMS	Industrial MicroSystems Inc.
Infosphere	Infosphere
Inmos	Inmos
IntCirEng	Integrated Circuit Engineering
IntCirSys	Integrated Circuit Systems
IntCompSys	Integrated Computer Systems
Int Tech	Integrated Technology Corp.
Intech	Intech Microcircuits Div.
Intel	Intel
Interdesign	Interdesign
Intersil	Intersil
Intronics	Intronics
ITT	ITT Semiconductors
Kinetic Sys	Kinetic Systems
Kontron	Kontron Electronics
Lambda	Lambda Semiconductor
Linear Tech	Linear Technology
LSI Comp	LSI Computer Systems
LSI Logic	LSI Logic Corporation
Master Logic	Master Logic Corporation
Matrix	Matrix Corp.
Matrox	Matrox Electronic Systems
Maxim	Maxim Integrated Products
MCC	Micro-Computer Control
MCE	MCE Electronics
Micrel	Micrel
Micro Innov	Micro Innovators
Micropac	Micropac Industries
Micro Net	Micro Networks
Micro Pwr	Micro Power Systems
Micro Sci	Micro Sciences Corp.
Micro Tech	Microcircuits Technology
Micro-Link	Micro-Link Corporation
Micron	Micron Technology
MilerTron	MilerTronics
Miller	Miller Technology
Mitel	Mitel Semiconductor
Mitsubishi	Mitsubishi Electronics
MMI	Monolithic Memories, Inc.
Mostek	Monolithic Systems Corp.
Motorola	Mostek
MRC	Motorola Semiconductor
Murray	MRC Systems
Monosil	Murray Consulting
National	National Semiconductor
NCM	NCM Corp.
NCR	NCR Corp., Microelectronics Division
NEC	NEC Electronics
Nitron	Nitron
OAE	Oliver Advanced Engineering
Octagon	Octagon Systems Corp.
OEI	Optical Electronics Inc.
Ohio Sci	Ohio Scientific
OKI	OKI Semiconductor
Omnibyte	Omnibyte Corp.
Onset	Onset Computer Corp.
Panasonic	Panasonic
Pico Design	Pico Design
Polycore	Polycore Electronics
Plessey	Plessey Semiconductors
PMI	Precision Monilithics, Inc.
PragDes	Pragmatic Design Inc.
Pro-Log	Pro-Log Corp.
Quay	Quay Corp.
Raytheon	Raytheon Semiconductor
RCA	RCA Solid State Division
RCI Data	RCI Data
RELMS	Relational Memory Systems
Reticon	Reticon
RIFA	RIFA
Rockwell	Rockwell, Microelectronic Devices
RTC	Riehl Time Corporation
Sanyo	Sanyo
SBE	SBE, Inc.
SEEQ	SEEQ Technology, Inc.
SPI	Semi Processes Inc.
Siemens	Siemens
Si-Fab	Si-Fab
Signetics	Signetics
SGS	SGS Semiconductor
Sharp	Sharp
Silicon G	Silicon General
Siliconix	Siliconix
Silicon Sys	Silicon Systems Inc.
Siltronics	Siltronics
SMC	Standard Microsystems Corp.
S MOS	S MOS Systems
Solarise	Solarise Enterprises
Solitron	Solitron Devices
Sprague	Sprague Electric Company
SSM	Solid State Micro Technology for Music
SSS	Solid State Scientific
Stag	Stag Microsystems
STC	Storage Technology Corp.
STD	STD Microsystems
Struc Des	Structured Design Inc.
Stynetic	Stynetic Systems
Sunrise	Sunrise Electronics
Sunshine	Sunshine Semiconductor
Supertex	Supertex Inc.
Symtek	Symtek Corp.
Synertek	Synertek
Sys Innov	Systems Innovations
Tau Zero	Tau Zero Inc.
Technitrol	Technitrol
Tektronix	Tektronix
Teledyne C	Teledyne Crystalonics
Teledyne P	Teledyne Philbrick
Teledyne S	Teledyne Semiconductor
Telefunken	Telefunken
Telmos	Telmos
Teltone	Teltone Corporation
TI	Texas Instruments
Third Domain	Third Domain
Thomson-CSF	Thomson-CSF Components Corp.
Toshiba	Toshiba America
Trans-Data	Trans-Data
TRW	TRW LSI Products
Unitrode	Unitrode
Universal	Universal Semiconductor, Inc.
Varix	Varix Corp.
VLSI Design	VLSI Design Associates
VTI	VLSI Technology, Inc.
Votrax	Votrax
Weitek	Weitek Corporation
Western	Western Digital
Wintek	Wintek Corp.
Xicor	Xicor, Inc.
Xycom	Xycom
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Zytrex	Zytrex Corp.

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The Manufacturers and Distributors/Representatives Directory is a comprehensive telephone directory of the entire IC industry. It places at your fingertips the names and phone numbers you need to know. It includes manufacturers, international sales offices, representatives and distributors; for manufacturers with data pages, it also includes domestic sales offices, representatives and distributors. The manufacturers' listings tell you where and whom to call to obtain technical and ordering information. It enables you to ask for the right person or phone extension. It gives you the terminology understood by the individual company's switchboard operators, e.g., in some companies you should ask for sales, in others, customer service. This directory will reduce frustration and save you time.

Action Instruments

Action Instruments Company, Inc.
8601 Aero Drive
San Diego, California 92123
619-279-5726

Advanced Micro Devices

Advanced Micro Devices, Inc.
901 Thompson Place
Sunnyvale, California 94088
408-732-2400
TELEX: 34-6306

Specific product information:
- Bipolar Microprocessors .... Leon Torban
- Bipolar Memory .... Dave Wood
- Logic (MSI) .... Chris King
- Hi-Rel Logic and Interface .... Ron Marfil
- Microcomputer Board Information .... Advanced Micro Devices, 3340 Scott Blvd., Santa Clara, CA 95051, 408-988-7777, Telex: 171-142
- MOS Microprocessors and Support Circuits ...... Ed Huber
- MOS Serial Memory, Mask-programmable ROMs and E-PROMs .... David Starr
- MOS-RAMs .... Bill DeMatteis (DRAM), Dick Bruneau (SRAM)
- Computer Interface .... Gary Conner

Application engineering:
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Military	Military-commercial/commercial-military cross-references; QPL-38510/xx list; military ICs.
Microprocessor	Microprocessors, microcomputers, and microprocessor system components.
Microprocessor Development Systems	Systems covered range from simple, single-user, text-editing stations to multi-user computers, dedicated to software development.
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Interface	Analog switches, analog-to-digital converters, digital-to-analog converters, display converters, display drivers, error checking circuits, keyboard encoders-decoders, drivers, sense amplifiers, and transmitters/receivers.
Linear	Special-purpose amplifiers, arrays, comparators, consumer circuits, followers, operational amplifiers, phase locked loop circuits, telecommunication circuits, timers, voltage regulators, and special functions.
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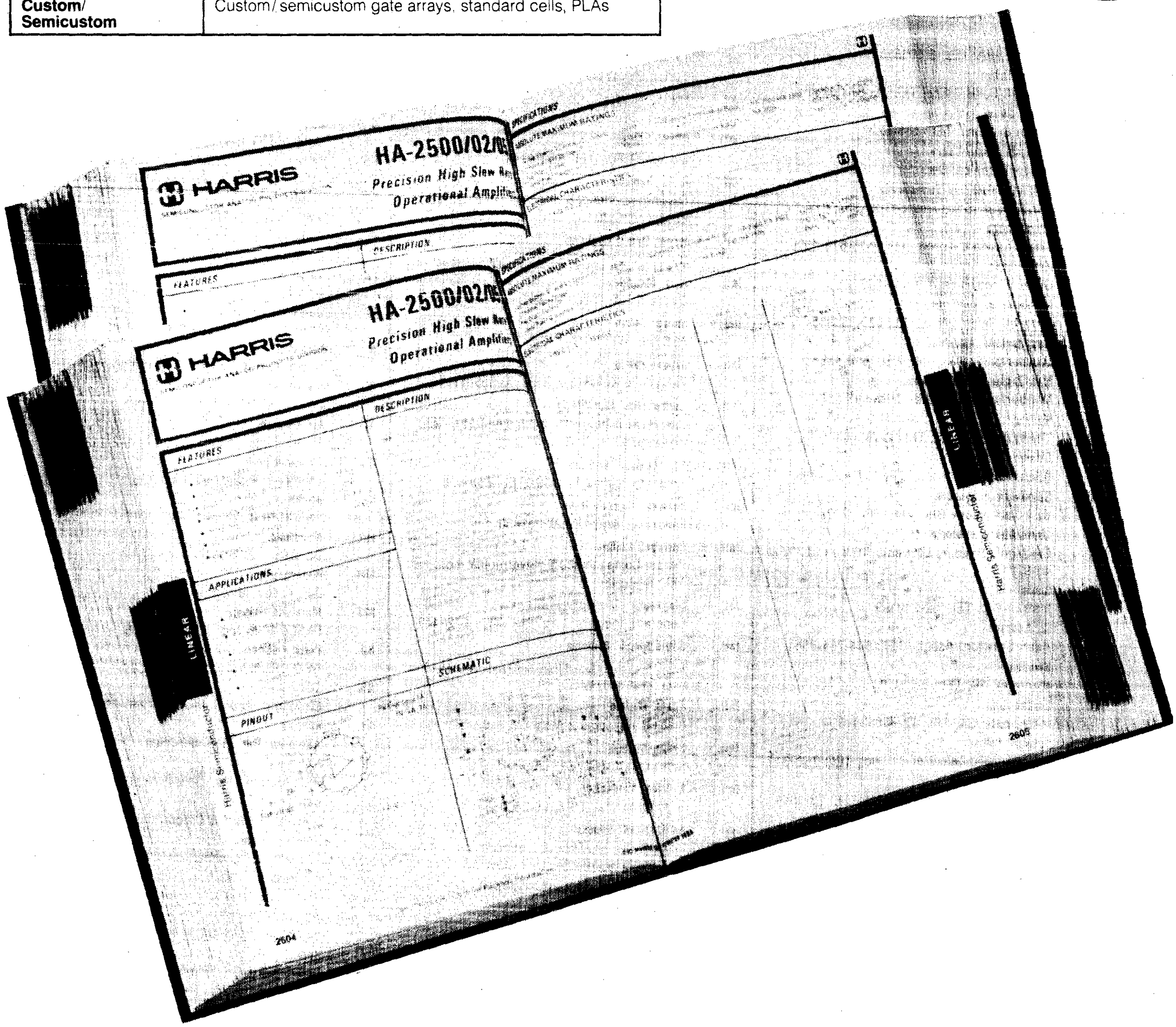
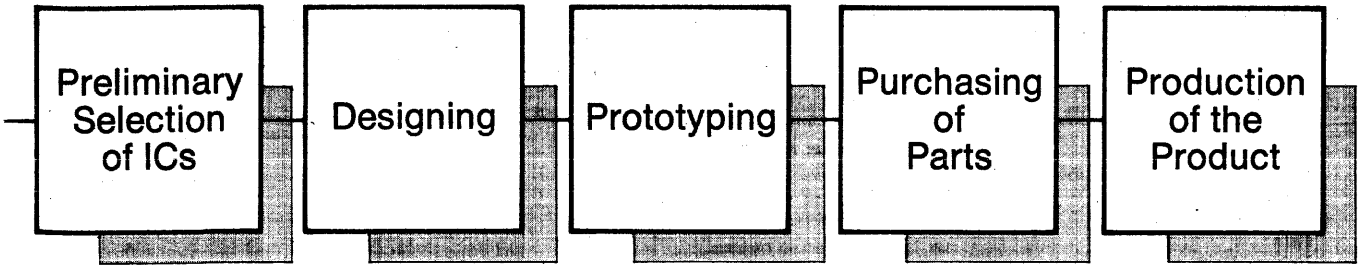
Custom/ Semicustom	Custom/semicustom gate arrays, standard cells, PLAs

SIX KEY PHASES OF NEW SYSTEM DEVELOPMENT

Planning

A good desigr





is "mastered" early.

When is the best time for an engineer to pick the integrated circuits that will go into his next design?

The best time is at an early stage in the design process when the engineer's plans are still flexible enough to take full advantage of the features selected.

There is a point in the early phases of every design when engineers focus on selecting integrated circuits. Specifications are examined, relative strengths and weaknesses of various devices are weighed, and the field of candidates is chosen. This is the critical time in the design cycle when designers want to be sure the right devices are in serious contention for their applications.

It is at this moment that the engineer reaches into his technical reference library. Of the material on his shelves, **IC MASTER** is the only reference source that has been especially prepared for this moment.

The engineer can look up each precise function that he needs and see all of the devices and their manufacturers that might satisfy his requirements. He sees this information for all manufacturers, not just for advertisers. But if an IC maker has chosen to include technical data for his products in **IC MASTER,** the engineer sees each index listing for that manufacturer in **bold face type** accompanied by the **page number** on which the data appears; the engineer can then turn immediately to the advertiser's technical data and see if the device fits his needs.

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Intl **Germany, Frankfurt Main**
Fairchild Camera & Instrument GmbH, TEL: 49-611-6905613
Intl **Holland, Eindhoven**
Fairchild Semiconductor, TEL: 00-31-40-446909
Intl **Hong Kong, Kowloon**
Fairchild Semiconductor (HK) Ltd., TEL: 3-440233
Intl **Italy, Milano**
Fairchild Semiconduttori, S.P.A., TEL: 296001-5
Intl **Italy, Roma**
Fairchild Semiconduttori, S.P.A., TEL: 06 327 4006
Intl **Japan, Osaka**
Fairchild Japan Corp., TEL: 06-541-6138, 06-541-6139
Intl **Japan, Tokyo**
Fairchild Japan Corp., TEL: 03 400 8351
Intl **Korea, Seoul**
Fairchild Semikor Ltd., TEL: 783-3795
Intl **Mexico, Mexico City**
Fairchild Mexicana S.A., TEL: 905-563-5411
Intl **Singapore, Kallang Basin**
Fairchild Semiconductor Pty. Ltd.
Intl **Sweden, Stockholm**
Fairchild Semiconductor AB, TEL: 8-449255
Intl **Switzerland, Zurich**
Fairchild Camera & Instrument GmbH, TEL: 41-1-3114230
Intl **Taiwan, Taipei**
Fairchild Semiconductor (Taiwan) Ltd., TEL: 573205
Intl **United Kingdom, Hertfordshire**
Fairchild Camera & Instr. (UK) Ltd., TEL: 0707 51111
Intl **W. Germany, Munich**
Fairchild Camera & Instr., TEL: (089) 320031
Intl **West Germany, Hanover**
Fairchild Camera & Instr., TEL: 0511 17844
Intl **West Germany, Leonberg**
Fairchild Camera & Instr., TEL: 07152 41026

Ferranti

Ferranti Electric, Inc.
87 Modular Avenue
Commack, New York 11725
516-543-0200
TWX: 510-226-1490

Specific product information:
Ken Kushman - IC Product Manager, Std IC's
Anthony V. Walker - VLA Marketing Manager, Semi Custom I.C. Gate Arrays
Joseph M. DeBlasio - VLA Marketing Engineer, Semi Custom I.C. Gate Arrays
Helen A. Nelson - VLA Marketing Assistant, Semi Custom I.C. Gate Arrays
John Day - VLA Systems Engineer, Semi Custom I.C. Gate Arrays
Denzil Broadhurst - VLA Systems Engineer, Semi-Custom I.C. Gate Arrays
John Carter - VLA Ststems Engineer, Semi Custom I.C. Gate Arrays
Application engineering:
Ken Kushman
Literature:
Jeanine Aiello
Price and delivery:
Dina Gentile
Follow-up an order:
Vivian Dennis
All other information:
Ken Kushman

Sales Office & Representatives

Intl **United Kingdom, Chadderton-Oldham**
Ferranti, Ltd., TEL: (061) 624-0515
Intl **West Germany, Munchen**
Ferranti GmbH, TEL: (089) 293-871

Fujitsu America

Fujitsu America
910 Sherwood, Suite 23
Lake Bluff, Illinois 60044
312-295-2610

Sales Office & Representatives

AZ **Phoenix**
Sanford Sales Assocs., 602-957-3570
CA **San Jose**
Applied Elctrn. Mktg., 408-225-6144
CA **Santa Ana**
SC Cubed (SC((¢3))), 714-972-4670
CO **Denver**
Donohue Sales, 303-458-6384
FL **Altamonte Springs**
"C" Assocs., 305-831-1717
FL **Hollywood**
"C" Assocs., 305-922-5230
GA **Stone Mountain**
Dixie Tech. Mktg., Inc., 404-962-2530
IL **Elk Grove Village**
John G. Twist Co., 312-593-0200
IN **Noblesville**
McFadden Sales, Inc., 317-877-5070
IA **Cedar Rapids**
John G. Twist Co., 319-393-8703
KS **Prairie Village**
John G. Twist Co., 913-236-4646
KS **Wichita**
John G. Twist Co., 316-686-6685
ME **E. Sebago**
Electrical Comps. Inc., 207
MA **Fall River**
Electrical Comps. Inc., 617-674-0064
MA **Longmeadow**
Electrical Comps. Inc., 413-567-0153
MA **Natick**
Electrical Comps. Inc., 617-655-2225
MN **Minneapolis**
John G. Twist Co., 612-854-4600
MO **St. Louis**
John G. Twist Co., 314-432-2830
NE **Lincoln**
John G. Twist Co., 402-474-5151
NV **Reno**
Applied Elctrn. Mktg., 702-851-1956
NJ **Parlin**
JMR Sales Inc., 201-727-5335
NY **East Setauket**
JMR Sales Inc., 516-689-8871
NC **Charlotte**
Robert W. Chapman Co., 704-525-2421
NC **Greensboro**
Robert W. Chapman Co., 919-282-0740
NC **Raleigh**
Robert W. Chapman Co., 919-782-2624
OH **Columbus**
McFadden Sales, Inc., 614-459-1280
TX **Dallas**
United Comps. Inc., 214-324-1448
VA **Midlothian**
Robert W. Chapman Co., 804-794-3748
WI **Brookfield**
John G. Twist Co., 414-782-2670

Distributors

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MD **Baltimore**
Component Sales, 301-484-3647
MI **Brighton**
A.P. Associates, 313-229-6650
NJ **Bellmawr**
TAI, 609-933-2600
NY **Rochester**
Lake Bluff Sales Division, 716-385-9303, 04
PA **Greensburg**
Pro-Mark, 412-832-3088
WA **Bellevue**
Whisler Sales Co., 206-643-1463

Fujitsu Microelectronics

Fujitsu Microelectronics, Inc.
2985 Kifer Road
Santa Clara, California 95051
408-727-1700
TWX: 910-338-0190

Specific product information:
Ed Alemany
Application engineering:
Bill Johnston
Literature:
Tim Henard
Price and delivery:
Respective sales office
Follow-up an order:
Respective sales office
All other information:
Ed Alemany (LD) 408-727-1700

Sales Office & Representatives

AZ **Scottsdale**
Thom Luke Sales, 602-941-1901

Fujitsu Microelectronics (Cont)

CA **Campbell**
Fujitsu Microelectronics, 408-866-5600
CA **San Diego**
Harvey King Inc., 619-566-5252
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NorCom Inc., 408-727-7707
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Straube Assocs., 303-426-0890
CT **North Haven**
Comp. Rep. Assoc., 203-239-9762
FL **Clearwater**
Dyne-A-Mark Corp., 813-441-4702
FL **Fort Lauderdale**
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FL **Maitland**
Dyne-A-Mark Corp., 305-831-2097
GA **Stone Mountain**
Dixie Tech. Mktg., 404-962-2530
ID **Boise**
Cascade Components, 208-343-9886
ID **Boise**
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IL **Arlington**
ZMS Electronic Sales, 312-394-4422
IL **Rolling Meadows**
Fujitsu Microelectronics, 312-934-6400
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Gaertner Assoc., 317-842-0373
IA **Cedar Rapids**
Electomec Sales, Inc., 319-362-6413
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P M R Corp., 913-381-0004
KS **Wichita**
P M R Corp., 316-684-4141
MD **Baltimore**
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MA **Newton Centre**
Fujitsu Microelectronics, 617-964-7080
MA **Westwood**
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MI **Brighton**
AP Assoc., 313-229-6550
MN **Burnsville**
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Fujitsu Microelectronics, 612-454-0323
MO **Maryland Heights**
P M R Corp., 314-569-1220
NM **Albuquerque**
Straube Assocs., 505-292-0428
NY **Hauppauge**
Technical Applications Mktg., 516-348-0800
NY **Mendon**
Tech-Mark/Upstate Assoc., 716-624-3840
OH **Cincinnati**
Makin & Associates, 513-872-2424
OH **Columbus**
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OH **Kent**
Makin & Associates, 513-872-2424
OR **Hillsboro**
Olson Ferree & Assocs., 503-640-9660
PA **Erdenheim**
Omni Sales, 215-233-4600
TX **Austin**
Fujitsu Microelectronics, 512-343-0320
TX **Houston**
Fujitsu Microelectronics, 713-784-7111
UT **Salt Lake City**
Straube Assocs., 801-263-2640
WA **Bellevue**
Olsen, Ferree & Assocs., 206-883-7792
WI **Brookfield**
ZMS Electronic Sales, 414-782-2222
Can **Burnaby, B.C.**
Woodbery Electronics Sales Ltd., 604-430-3302
Can **Islington, Ontario**
Pipe-Thompson Ltd., 416-236-2355
PR **Mayaguez, Puerto Rico**
Comp Rep Assoc., 809-832-9529

Distributors

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Cetec Elctrns., 602-272-7951
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Marshall Industries, 602-790-5687
CA **Canoga Park**
Marshall Inds., 213-999-5001
CA **Cupertino**
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CA **El Monte**
Marshall Inds., 213-442-7204
CA **Irvine**
Marshall Inds., 714-556-6400
CA **San Diego**
Cetec Elctrns., 619-278-5020
CA **San Diego**
Marshall Inds., 619-578-9600
CA **San Jose**
Cetec Elctrns., 408-263-7373
CA **Santa Ana**
Fujitsu Microelectronics, 714-547-9525
CA **Santa Ana**
Pacesetter Elctrns., 714-557-7131
CA **Southgate**
Cetec Elctrns., 213-773-6521
CA **Sunnyvale**
Marshall Inds., 408-732-1100
CA **Sunnyvale**
Time Elctrns. West, 408-734-9888
CA **Tustin**
Image Electronics, 714-730-0303
CO **Denver**
Integrated Electronics Corp., 303-292-6121
CO **Denver**
Marshall Inds., 303-427-1818
CT **Orange**
Milgray Connecticut, 203-795-0711
CT **Wallingford**
Marshall Inds., 203-265-3822
FL **Fort Lauderdale**
Time Elctrns.-Fl., 305-974-4800
FL **Orlando**
Marshall Inds., 305-841-1878
FL **Winter Park**
Milgray Florida, 305-647-5747
GA **Atlanta**
Milgray Atlanta, 404-393-9666
GA **Norcross**
Marshall Inds., 404-923-5750
IL **Bensenville**
Marshall Inds., 312-595-6622
IL **Chicago**
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Intercomp Inc., 312-843-2040
IL **Northbrook**
Classic Comp. Supply, 312-272-9650
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DEECO, 319-365-7551
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Milgray Kansas, 913-236-8800
MD **Gaithersburg**
Marshall Inds., 301-840-9450
MD **Rockville**
Milgray Washington, 301-468-6400
MA **Burlington**
Marshall Inds., 617-272-8200
MA **Burlington**
Milgray Elctrns.-New England, 617-272-6800
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Future Elctrns. Corp., 617-366-2400
MA **Woburn**
Time Elctrns.-New England, 617-935-8080
MI **Grand Rapids**
Caulder Assoc., 616-949-2900
MI **Livonia**
Marshall Industries, 313-525-5850
MI **Livonia**
Reptron Electronics, 313-525-2700
MN **Plymouth**
Marshall Inds., 612-559-2211
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Time Elctrns., 314-391-6444
NH **Hudson**
C & H Electronics, 603-882-1133
NJ **Fairfield**
Marshall Inds., 201-882-0320
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Milgray DelValley, 609-983-5010
NJ **Mt. Laurel**
Marshall Inds., 609-234-9100
NY **Endwell**
Marshall Inds., 607-754-1570
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Milgray Elctrns., 516-546-5600
NY **Hauppauge**
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Fujitsu Microelectronics, 516-273-6660
NY **Hauppauge**
Marshall Inds., 516-273-2424
NY **Hauppauge**
Mast Distrs., 516-273-4422
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Marshall Inds., 716-235-7620
NY **Rome**
Rome Electronics, 315-337-5400
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Reptron Electronics, 614
OH **Dayton**
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Radio, Inc., 918-587-9123
OR **Lake Oswego**
Moore Electronics, 503-684-3100
PA **Broomall**
Time Elctrns. Mid-Atlantic, 215-359-1200
TX **Addison**
Active Comp. Tech., 214-980-1888
TX **Austin**
Active Component Technology, 512-452-5254
TX **Dallas**
Marshall Inds., 214-233-5200
TX **Houston**
Marshall Inds., 713-789-6600
TX **Richardson**
Fujitsu Microelectronics, 214-669-1616
WA **Bellevue**
Integrated Electronic Corp., 206-455-2121
WA **Tukwila**
Marshall Inds., 206-575-3120
WI **Milwaukee**
Marsh Elctrns., 414-475-6000
WI **New Berlin**
Classic Comps., 414-786-5300
Can **Pointe Claire, Quebec**
Future Elctrns. Corp., 514-694-7710
Can **Scarborough, Ontario**
Carsten Electronics Ltd., 416-751-2371

General Instrument

General Instrument Corporation
Microelectronics Division
600 W. John Street
Hicksville, New York 11802
516-733-3107
TWX: 510-221-1866

Sales Office & Representatives

Intl **England, London**
General Instrument Microelectronics Ltd.,
TEL: 01-439-1895

General Instrument (Cont)

Intl **England, London**
General Instrument Microelectronics Ltd., TEL: 01-439-1891

Intl **France, Paris**
Southern European Sales Off., TEL: 365 72 50

Intl **Germany, Munchen**
General Instrument Deutschland GmbH, TEL: (089) 27 24 049

Intl **Hong Kong**
General Instrument Hong Kong Ltd., TEL: (5) 434360

Intl **Japan, Tokyo**
General Instrument Intl. Corp., TEL: (03) 437-0281

Intl **Taiwan, Taipei**
General Instrument Microelectronics Taiwan, TEL: 886-2-914-6234

Distributors

Intl **Australia, Victoria, Sandringham**
Daneva Control Pty. Ltd., TEL: (03) 598-5622

Intl **Austria, Wien**
Elbatex GmbH, TEL: 0222/88 56 11

Intl **Belgium, Bruxelles**
Vekano, TEL: 7620505

Intl **Denmark, Herlev**
A/S Nordisk-Elektronik, TEL: 84.20.00

Intl **England, London**
Bee Arosales (Exporters), TEL: 01-636-6614/ 01-636 8211

Intl **Finland, Espoo**
Jorma Sarkkinen Ky., TEL: 046.10.88

Intl **France, Boulogne**
Gedis, TEL: 604.81.70

Intl **France, Montrouge**
P.E.P., TEL: 735.33.20

Intl **Germany, Berlin**
Roederstein-Baulemente Vertriebs GmbH, TEL: 0 30/7 91 40 29

Intl **Germany, Heilbronn**
Elbatex GmbH, TEL: 0 71 31/8 90 01

Intl **Germany, Munchen**
Electronic 2000 Vertriebs-GmbH, TEL: 0 89/ 43 40 61

Intl **Germany, Wiesbaden**
Elcowa, TEL: 06121 65005

Intl **Holland, Geldermalsen**
Curijn Hasselaar, TEL: 03455-3150

Intl **Israel, Tel-Aviv**
Alexander Schneider Ltd., TEL: 3 320.89-3 346.07

Intl **Italy, Milan**
Adrep Srl, TEL: (02) 408.41.01

Intl **Italy, Milan**
Claitron, TEL: 3088506 ¢ 3088083

Intl **Italy, Milan**
Intesi, TEL: 51741

Intl **Italy, Milan**
Intl. Commerce Co., TEL: 4045747 ¢ 405197

Intl **Italy, Modena**
Hellis Di B. Prati, TEL: 059-804104 ¢ 802562

Intl **Italy, Rome**
3 C.E., TEL: 5420625

Intl **Italy, Trieste**
Rapido SARL

Intl **Korea, Seoul**
Dae Ho Corp., TEL: 777-3848, 2487

Intl **New Zealand, Auckland**
David Reid Professional Prods. Ltd., TEL: 499-197

Intl **Norway, Oslo**
J.M. Feiring A/S, TEL: (02) 19.62.00

Intl **Portugal, Lisbon**
Decada, TEL: 574984

Intl **South Africa, Transvaal**
Pace Elctrn. Comps. (Pty.) Ltd., TEL: 616-361211

Intl **Spain, Madrid**
Sagitron S.A., TEL: 4-02.60.85

Intl **Sweden, Taby**
Bexab Elektronic AB, TEL: 468 768 0560

Intl **Switzerland, Wettingen**
Elbatex AG, TEL: 056/26 56 41

Intl **Switzerland, Zurich**
Ellyptic AG, TEL: 01 493 10 00

Intl **United Kingdom, Keighley**
Semicomps Ltd., TEL: 0535 65191

Intl **United Kingdom, Oldham**
Vako Elctrns. Ltd., TEL: 061-652 6316

Intl **United Kingdom, Slough**
Crellon Elctrns. Ltd., TEL: 06286 4434

Intl **United Kingdom, Stevenage**
Campbell Collins Ltd., TEL: 0438 69466

Intl **United Kingdom, West Drayton**
Semiconductor Specialists Ltd., TEL: West Drayton 45522

General Micro Systems

General Micro Systems Inc.
1320 Chaffey Court
Ontario, California 91762
714-621-7532

GTE Microcircuits

GTE Microcircuits Division
GTE Communications Products Corporation
2000 W. 14th St.
Tempe, Arizona 85281
602-968-4431
TWX: 910-951-1383

Sales Office & Representatives

Intl **West Germany, Munich**
GTE Microcircuits Div., GTE Sylvania Licht GmbH, TEL: 089/1 78 20 31

Harris Semiconductor

Harris Semiconductor
Analog & Digital Bipolar/Digital CMOS Products Divisions/
Department ICM
P. O. Box 883
Melbourne, Florida 32901
305-724-7000
TWX: 510-959-6259

Specific product information:
Field Sales Office

Application engineering:
Field Sales Office

Literature:
Field Sales Office

Price and delivery:
Field Sales Office

Place an order:
Field Sales Office

Harris Semiconductor (Cont)

Follow-up an order:
Customer Service .... (305) 724-7410
All other information:
Marketing Communications .... (305) 724-7407

Sales Office & Representatives

AL	**Huntsville** Elctrn. Mktg. Assocs., 205-837-7363
AZ	**Phoenix** Compass Mktg. & Sales, Inc., 602-266-5400
AZ	**Scottsdale** Harris Semiconductor, 602-870-0080
CA	**Costa Mesa** Harris Semiconductor, 714-540-2176
CA	**Mountain View** Brooks Tech. Grp., 415-960-3880
CA	**Mountain View** Harris Semiconductor, 415-964-6443
CA	**San Diego** Hadden Assocs., 619-565-9444
CA	**Woodland Hills** Harris Semiconductor, 213-992-0686
CO	**Denver** Comp. Sales, Inc., 303-759-1666
CT	**Ridgefield** Phoenix Sales Co., 203-438-9644
FL	**Clearwater** Delmac Sales, 813-447-5192
FL	**Ft. Lauderdale** Harris Semiconductor, 305-739-0016
FL	**Orlando** Delmac Sales, 305-898-4688
FL	**Tamarac** Delmac Sales, 305-726-1330
GA	**Atlanta** Harris Semiconductor, 404-256-4000
IL	**Elk Grove Village** Oasis Sales, Inc., 312-640-1850
IL	**Rosemont** Harris Semiconductor, 312-692-4960
IN	**Carmel** Harris Semiconductor, 317-844-8011
IN	**Carmel** Shamrock Electronic Sales, 317-848-5265
IA	**Cedar Rapids** Cahill Assocs., Inc., 319-377-8219
KS	**Overland Park** Advanced Technical Sales, 913-642-6675
MA	**Burlington** Harris Semiconductor, 617-273-5942
MA	**Burlington** Mill Bern Assocs., Inc., 617-273-1313
MI	**Novi** Action Comp. Sales, 313-349-3940
MN	**Minneapolis** Harris Semiconductor, 612-854-3558
MN	**St. Paul** Cahill, Schmitz & Cahill, Inc., 612-646-7217
MO	**St. Louis** Advanced Technical Sales, 314-227-4448
NM	**Albuquerque** Compass Mktg. & Sales Inc., 505-292-7377
NY	**Binghamton** Precision Sales, 607-646-8833
NY	**Great Neck** Trionic Assoc. Inc., 516-466-2300
NY	**Liverpool** Precision Sales, 315-451-3480
NY	**Melville** Harris Semiconductor, 516-249-4500
NY	**Pittsford** Precision Sales, 716-381-2820
NY	**Pleasant Valley** Precision Sales, 914-635-3233
NC	**Raleigh** Elctrn. Mktg. Assocs., 919-847-8800
OH	**Chagrin Falls** Midwest Mktg. Assocs., 216-247-6655
OH	**Dayton** Midwest Mktg. Assocs., 513-433-2511
PA	**Broomall** L. D. Lowery, Inc., 215-356-5300
PA	**Wayne** Harris Semiconductor, 215-687-6680
TX	**Dallas** Harris Semiconductor, 214-248-3237
TX	**Dallas** Nova Mktg., 214-750-6082
TX	**Houston** Nova Mktg., 713-988-6082
UT	**Salt Lake City** Comp. Sales, Inc., 801-466-8623
VA	**Charlottesville** L. D. Lowery, Inc., 804-973-6672
WA	**Federal Way** Harris Semiconductor, 206-838-4878
WA	**Vancouver** Harris Semiconductor, 206-696-0043
WI	**Brookfield** Oasis Sales, Inc., 414-782-6660
Can	**Etobicoke, Ontario** RFQ Ltd., 416-626-1445
Can	**Ottawa, Ontario** RFQ Ltd., 613-820-8445
Can	**West Vancouver, British Columbia** Blakewood Elect. Systems, Inc., 604-926-8000
PR	**Puerto Rico, San Juan** Mill-Bern Assoc. Inc., 809-792-1541

Distributors

AL	**Huntsville** Hall-Mark/Huntsville, 205-827-8700
AL	**Huntsville** Hamilton/Avnet, 205-837-7210
AL	**Huntsville** Schweber Elctrns., 205-882-2200
AZ	**Phoenix** Hall-Mark Elctrns., 602-243-6601
AZ	**Scottsdale** Western Microtechnology Sales, 602-948-4240
AZ	**Tempe** Anthem Electronics, 602-244-0900
AZ	**Tempe** Hamilton/Avnet, 602-231-5100
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CA	**Chatsworth** Avnet Electronics, 213-716-4853
CA	**Costa Mesa** Avnet Elctrns., 714-754-6088
CA	**Costa Mesa** Hamilton Electro, 714-641-4107
CA	**Culver City** Hamilton/Avnet, 213-558-2193
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CA	**Los Angeles** Enterprex International Corp., 213-267-1145
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CA	**Sacramento** Hamilton/Avnet, 916-925-2216
CA	**San Diego** Anthem Electronics, 619-279-5200
CA	**San Diego** Hall-Mark Elctrns., 619-268-1201
CA	**San Diego** Hamilton/Avnet, 619-571-7523
CA	**San Jose** Anthem Electronics, 408-946-8000
CA	**Santa Clara** Schweber Elctrns., 408-748-4700
CA	**Sunnyvale** Anthem Electronics, 408-773-9990
CA	**Sunnyvale** Hall-Mark Electronics, 408-773-9990
CA	**Sunnyvale** Hamilton/Avnet, 408-743-3355
CA	**Tustin** Anthem Electronics, 714-730-8000
CO	**Englewood** Anthem Electronics, 303-790-4500
CO	**Englewood** Hall-Mark/Denver, 303-694-1662
CO	**Englewood** Hamilton/Avnet, 303-779-9998
CT	**Danbury** Hamilton/Avnet, 203-740-1017
CT	**Danbury** Schweber Elctrns., 203-792-1100
CT	**Milford** Falcon Electronics, 203-878-5272
CT	**Norwalk** Pioneer-Harvey Elctrns., 203-853-1515
FL	**Altamonte Springs** Schweber Elctrns., 305-331-7555
FL	**Ft. Lauderdale** Hall-Mark, 305-971-9280
FL	**Ft. Lauderdale** Hamilton/Avnet, 305-971-2900
FL	**Hollywood** Schweber Elctrns., 305-921-0301
FL	**Orlando** Hall-Mark, 305-855-4020
FL	**St. Petersburg** Hall-Mark, 813-576-8691
FL	**St. Petersburg** Hamilton/Avnet, 813-576-3930
GA	**Norcross** Hall-Mark, 404-447-8000
GA	**Norcross** Hamilton/Avnet, 404-447-7503
GA	**Norcross** Schweber Elctrns., 404-449-9170
IL	**Bensenville** Hall-Mark, 312-860-3800
IL	**Bensenville** Hamilton/Avnet, 312-860-7780
IL	**Elk Grove Village** Schweber Elctrns., 312-364-3750
IN	**Carmel** Hamilton/Avnet, 317-844-9333
KS	**Lenexa** Hall-Mark, 913-888-4747
KS	**Overland Park** Hamilton/Avnet, 913-541-7921
MD	**Baltimore** Hall-Mark, 301-796-9300
MD	**Columbia** Hamilton/Avnet, 301-995-3500
MD	**Gaithersburg** Schweber Elctrns., 301-840-5900
MD	**Timonium** Zebra Electronics, 301-252-6576
MA	**Bedford** Schweber Elctrns., 617-275-5100
MA	**Lexington** Pioneer-Harvey Elctrns., 617-863-1200
MA	**Wilmington** R C Components, 617-273-1860
MA	**Woburn** Hamilton/Avnet, 617-935-9700
MI	**Grand Rapids** Hamilton/Avnet, 616-243-8805
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Matra-Harris Semiconductor, TEL: 33-40-490820

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Lasi Elettronica, TEL: 39-2-9273578

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Eltek/Elmo Semi. Ltd., TEL: 4-804304455

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Thames Comps., TEL: 44-84421-3146

Harris Semiconductor

Harris Semiconductor
Custom Integrated Circuits Division/Department ICM
P. O. Box 883
Melbourne, Florida 32901
305-724-7000
TWX: 510-959-6259

Specific product information:
Field Sales Office—Custom Integrated Circuits

Application engineering:
Kenneth V. Worland 305-724-7481

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All other information:
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DC **Washington D.C.**
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AME Sales, 913-262-3971

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Harris Semiconductor Custom Integrated Circuits, 617-273-1020

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Harris CICD, 516-747-6776

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Harris Semiconductor, TEL: 011-447-5334666

Intl **United Kingdom, Slough**
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Heurikon

Heurikon Corporation
3001 Latham Drive
Madison, Wisconsin 53713
608-271-8700

Hewlett-Packard

Hewlett-Packard
Data Systems Division
11000 Wolfe Road
Cupertino, California 95014
408-257-7000
TWX: 910-338-0221

Hilevel Technology

Hilevel Technology, Inc.
18902 Bardeen Way
Irvine, California 92715
619-752-5215

Hitachi

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1800 Bering Drive
San Jose, California 95131
408-292-6404
TELEX: 17-1581
TWX: 910-338-2103

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Holt, Inc.
8 Chrysler Street
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TELEX: 182704

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Hughes

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Hybrid Systems

Hybrid Systems Corporation
22 Linnell Circle
Billerica, Massachusetts 01821
617-667-8700
TWX: 710-347-1575

Hybrid Systems (Cont)

Specific product information:
Henry Diamond, National Sales Manager .... ext. 60
Art Berg, East Coast Regional Sales Manager ...... ext. 13
Jack Worthen, Northeast Regional Sales Manager .... ext. 17
Charles J. Bevivino, West Coast Regional Sales Manager ext. 18
Literature:
Cheryl Kane .... ext. 11
Price and delivery:
Patricia G. Bradley .... ext. 12
All other information:
Janet J. Ray .... ext 14
Product Marketing:
Director of Marketing, Barry Friedman .... ext. 54

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Relcom, 213-340-9143
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Ferner Elctrns. AB
Intl **Switzerland, Zurich**
Industrade AG, TEL: 4131 363 2230
Intl **Holland, Haaften**
Techmation Electronics B.V., TEL: 31-4189-2222
Intl **India, Ludhiana**
Inde Assoc., TEL: 37031
Intl **Israel, Ramat Hasharon**
R D T Elctrns., TEL: 972-3-48.32.11
Intl **Italy, Milan**
Microelit Italia s.r.l., TEL: 39-2-469 0444
Intl **Italy, Roma**
Microelit Italia, s.r.l., TEL: 77-9-011-39-6-890892
Intl **Japan, Tokyo**
Minebea Co., Ltd., TEL: 77-9-011-81-3-763-6241
Intl **Norway, Oslo**
Henaco A/S, TEL: 77-9-011-47-2-162110
Intl **Spain, Madrid**
Anatronic, S.A., TEL: 34-1-2424455
Intl **Sweden, Tyreso**
Hybridteknik A/B, TEL: 46-8-7126720
Intl **Switzerland, Baden-Daettwil**
W. Stolz AG, TEL: 41-56-840151
Intl **Taiwan, Taipei**
Tai I Trading Co., Ltd., TEL: 886-2-713-2342
Intl **West Germany, Muenchen**
Fey Elektronik Bauelemente GmbH, TEL: 49-89-184041
Intl **Yugoslavia, Titova**
Elektrotehna, TEL: 61-329745

Hy Comp

Hy Comp Inc.
75 Union Avenue, Box 377
Sudbury, Massachusetts 01776
617-443-4631
Application engineering:
John J. Madden
Follow-up an order:
Customer Services:
Nancy Oelschlegel
All other information:
James Chacharone, V.P./Marketing Manager

ILC Data Device

ILC Data Device Corp.
105 Wilbur Place
Bohemia, New York 11716
516-567-5600
TWX: 510-228-7324

Sales Office & Representatives

Intl **Australia, Brookvale**
Allied Capacitors Pty. Ltd., TEL: 77-9-011-61-2-938-2135
Intl **England, Berkshire**
DDC United Kingdom, Ltd., TEL: 44-488-82141
Intl **England, London**
ILC Data Device Corp., TEL: 44-1-3874689
Intl **Finland, Helsinki**
OY Suomen Bofors AB, TEL: 358-0-553-166
Intl **France, Courbevoie**
DDC Electronique, TEL: 33-1-333-5888

Industrial Micro-Systems

Industrial Micro-Systems Inc.
189 Hitchcock Road
Southington, Connecticut 06489
203-628-4844

Infosphere, Inc.

Infosphere, Inc.
4730 SW Macadam Ave.
Portland, Oregon 97201
503-226-3515

Distributors

Intl **Japan**
ASR-International, TEL: 602-949-8293
Intl **New Zealand, Dunedin**
K. J. Kirby & Assoc., TEL: (24) 34-580

Inmos

Inmos
P.O. Box 16000
Colorado Springs, Colorado 80935
303-630-4000
TWX: 910-920-4904
Specific product information:
Field Sales Offices
Application engineering:
Applications 303-630-4493
Literature:
Field Sales Offices
Place an order:
Field Sales Offices/Distributors
All other information:
Marketing 303-630-4361

Sales Office & Representatives

AL **Huntsville**
Macro-Marketing Assoc., 205-883-9630

Inmos (Cont)

AZ **Phoenix**
Compass Mktg. & Sales, 602-266-5400
CA **Los Angeles**
Ed Landa Co., 213-879-0770
CA **San Diego**
Hadden Assoc., 619-565-9444
CA **San Jose**
Inmos Sales, 408-298-1786
CA **Santa Clara**
Criterion Sales, 408-988-6300
CA **Torrance**
Inmos Sales, 213-530-7764
CO **Denver**
Component Sales, 303-759-1666
CT **Yalesville**
Kanan Assoc., 203-265-2404
FL **Fern Park**
E.I.R., Inc., 305-830-9600
GA **Woodstock**
Macro-Marketing Assoc., 205-883-9630
IL **Schaumburg**
Micro-Tex, 312-885-1131
IN **Indianapolis**
Electro Reps, Inc., 317-842-7202
KS **Kansas City**
B.C. Electronic Sales, 913-342-1211
KS **Wichita**
B.C. Electronic Sales, 316-942-9840
MD **Severna Park**
New Era Sales, 301-544-4100
MA **Burlington**
Inmos Sales, 617-273-5150
MA **Reading**
Kanan Assoc., 617-944-8484
MI **Grand Rapids**
J. L. Montgomery Assoc., Inc., 616-774-9308
MI **Southfield**
J. L. Montgomery Assoc. Inc., 313-385-2616
MN **Edina**
Mel Foster Tech Sales, 612-941-9790
MN **Minneapolis**
Inmos Sales, 612-831-5626
MO **St. Louis**
B.C. Electronic Sales, 314-291-1101
NJ **Teaneck**
R.T. Reid Assoc., 201-692-0200
NM **Albuquerque**
Compass Mktg. & Sales, 505-292-7377
NY **E. Syracuse**
L-Mar Assoc., 315-437-7779
NY **Ithaca**
L-Mar Assoc., 607-257-5712
NY **Rochester**
L-Mar Assoc., 716-323-1000
NY **W. Seneca**
L-Mar Assoc., 716-675-1277
NC **Raleigh**
Zucker Assoc., 919-782-8433
OH **Beachwood**
Thompson & Assoc., 216-831-6277
OH **Columbus**
Thompson & Assoc., 614-272-2086
OH **Dayton**
Inmos Sales, 513-439-0988
OH **Dayton**
Thompson & Assoc., 513-435-7733
OR **Boring**
Westerberg & Assoc., 503-297-1719
PA **Huntingdon Valley**
Knowles Assoc., 215-947-5641
TX **Dallas**
Nova Mktg., 214-750-6082
TX **Houston**
Nova Mktg., 713-988-6082
UT **Salt Lake City**
Component Sales, 801-466-8623
WA **Bellevue**
Westerberg & Assoc., 206-453-8881
WI **Waukesha**
Micro-Tex, 414-542-5352
Can **Downsview, Ontario**
Har-Tech Electronics, 416-542-5352
Can **Pointe Claire, Quebec**
Har-Tech Electronics, 514-697-6731
Intl **Italy, Milan**
Cefra SRL, TEL: 392-235264
Intl **Japan, Tokyo**
Matsushita Electric, TEL: 03-435-4501
Intl **United Kingdom, Bristol**
Inmos Sales, TEL: 44-272-290-861
Intl **West Germany**
Inmos Sales, TEL: 49-089-319-1028

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AZ **Tempe**
Anthem Elctrns., 602-244-0900
CA **Chatsworth**
Anthem Elctrns., 213-700-1000
CA **Chatsworth**
Arrow Elctrns., 213-701-7500
CA **Newport Beach**
Arrow Elctrns., 714-851-8961
CA **San Diego**
Anthem Elctrns., 619-453-4871
CA **San Diego**
Arrow Elctrns., 619-565-4800
CA **San Jose**
Anthem Elctrns., 408-946-8000
CA **Sunnyvale**
Arrow Elctrns., 408-745-6600
CA **Tustin**
Anthem Elctrns., 714-730-8000
CO **Denver**
Arrow Elctrns., 303-696-1111
CO **Englewood**
Anthem Electrns., 303-790-4500
CT **Wallingford**
Arrow Elctrns., 203-265-7741
FL **Ft. Lauderdale**
Arrow Elctrns., 305-776-7790
FL **Palm Bay**
Arrow Elctrns., 305-725-1480
GA **Norcross**
Arrow Elctrns., 404-449-8252
IL **Schaumburg**
Arrow Elctrns., 312-397-3440
IN **Indianapolis**
Arrow Elctrns., 317-243-9353
MD **Baltimore**
Arrow Elctrns., 301-247-5200
MA **Burlington**
Lionex Corp., 617-272-9400
MA **Woburn**
Arrow Elctrns., 617-933-8130
MI **Ann Arbor**
Arrow Elctrns., 313-971-8220
MN **Edina**
Arrow Elctrns., 612-830-1800
MO **St. Louis**
Arrow Elctrns., 314-567-6888
NH **Manchester**
Arrow Elctrns., 603-668-6968
NJ **Fairfield**
Arrow Electrns., 201-575-5300
NJ **Fairfield**
Lionex Corp., 201-227-7960
NJ **Moorestown**
Arrow Elctrns., 609-235-1900
NM **Albuquerque**
Arrow Elctrns., 505-243-4566
NY **Hauppauge**
Arrow Elctrns., 516-231-1000
NY **Hauppauge**
Lionex Corp., 516-273-1660
NY **Liverpool**
Arrow Elctrns., 315-652-1000
NY **Melville**
Arrow Elctrns., 516-694-6800
NY **Rochester**
Arrow Elctrns., 716-275-0300
NC **Winston-Salem**
Arrow Elctrns., 919-725-8711
OH **Centerville**
Arrow Elctrns., 513-435-5563
OH **Solon**
Arrow Elctrns., 216-248-3990
OK **Tulsa**
Arrow Elctrns., 918-665-7700
PA **Horsham**
Lionex Corp., 215-443-5150
PA **Monroeville**
Arrow Elctrns., 412-856-7000
TX **Addison**
Quality Comps., 214-387-4949
TX **Austin**
Arrow Elctrns., 512-835-4180
TX **Austin**
Quality Comps., 512-835-0220
TX **Dallas**
Arrow Elctrns., 214-386-7500
TX **Stafford**
Arrow Elctrns., 713-530-4700
UT **Salt Lake City**
Arrow Elctrns., 801-539-1135
WA **Bellevue**
Arrow Elctrns., 206-643-4800
WA **Redmond**
Anthem Elctrns., 206-881-0850
WI **Oak Creek**
Arrow Elctrns., 414-764-6600
Can **Baxter Ctr., Ontario**
Future Elctrns., 613-820-8313
Can **Burnaby, B.C.**
R-A-E, 604-291-8866
Can **Calgary, Alberta**
Future Elctrns., 403-259-6437
Can **Downsview, Ontario**
Future Elctrns., 416-663-5563
Can **Edmonton, Alberta**
R-A-E, 403-451-4001
Can **Pointe Claire, Quebec**
Future Elctrns., 514-694-7710
Can **Vancouver, British Columbia**
Future Elctrns., 604-438-5545
Intl **Belgium, Brussels**
Diode, TEL: 322-4285105
Intl **Denmark, Copenhagen**
Advanced Elctrn., TEL: 451-1-94433
Intl **Finland, Helsinki**
Field Oy, TEL: 358-0 6922577
Intl **France, Serves**
Tekelec Airtronic, TEL: 331-534-7535
Intl **Israel**
R.D.T. Elctrns. Ltd., TEL: 972-3483211
Intl **Italy, Milan**
Cefra SRL, TEL: 392-235264
Intl **Netherlands, Badhoevedorp**
Techmation Elctrns., TEL: 31-4189-2222
Intl **Norway, Oslo**
Ola Tandberg Elektro, TEL: 472-197030
Intl **Spain, Madrid**
Amitron, TEL: 341-24856863
Intl **Sweden, Stockholm**
Gosta Backstrom, TEL: 468-541080
Intl **Switzerland, Zurich**
Omni Ray, TEL: 411-2520766
Intl **United Kingdom, High Wycombe, Bucks**
Rapid Recall, TEL: 44-494-26271
Intl **United Kingdom, Sunbury on Thames, Middlesex**
Hawke Elctrns., TEL: 44-9327-85577
Intl **West Germany, Munich**
EZOOO A.G., TEL: 49-89-434061
Intl **West Germany, Quickborn**
Astek Elctrns., TEL: 49-4106-71084
Intl **West Germany, Stuttgart**
Ditronic, TEL: 49-711-722079

Intech Inc.

Intech Inc.
2270 Martin Avenue
Santa Clara, California 95050
408-988-4390
TWX: 910-338-2213

Integrated Circuit Engineering

Integrated Circuit Engineering Corporation
15022 North 75th Street
Scottsdale, Arizona 85260
602-998-9780

Sales Office & Representatives

Intl **Hong Kong, Kowloon**
Tektron Elctrns. Ltd., TEL: (011) (852) (3) 856199
Intl **Japan, Tokyo**
Nihon Teksel Co., Ltd., TEL: (011) (81) (3) 461-5121
Intl **Switzerland, Walchwil**
Nicotec SA, TEL: (011) (41) (42) 316637

Integrated Circuit Systems

Integrated Circuit Systems, Inc.
1012 West Ninth Avenue
King of Prussia, Pennsylvania 19406
215-265-8690

Integrated Device Technology

Integrated Device Technology, Inc.
3236 Scott Boulevard
Santa Clara, California 95051
408-727-6116
TWX: 910-338-2070

Sales Office & Representatives

AL **Huntsville**
Montgomery Marketing, 205-830-0498
AZ **Tempe**
Argus Sales Inc., 602-968-7791
CA **Culver City**
Bestronics Inc., 213-870-9191
CA **Cupertino**
Thresum Assocs., Inc., 408-996-9889
CA **Irvine**
Bestronics Inc., 714-979-9910
CA **San Diego**
Adem Assocs., 619-695-2050
CA **Santa Clara**
IDT Sales Office—Bay Area, 408-727-6116
CA **Westminster**
IDT Sales Office—Western Area, 213-598-3076, 213-598-3076
CA **Woodland Hills**
Bestronics Inc., 213-704-5616
CO **Denver**
Elcom, 303-337-2300
FL **Boca Raton**
Lawrence Assocs., Inc., 305-368-7373
FL **Clearwater**
Lawrence Assocs., Inc., 813-584-8110
FL **West Melbourne**
Lawrence Assocs., Inc., 305-724-8294
GA **Norcross**
Montgomery Marketing, 404-447-6124
IL **Downers Grove**
Circuit Sales, Inc., 312-964-9090
IN **Ft. Wayne**
Arete Sales, 219-485-2375
MD **Baltimore**
Microcomp, 301-247-0400
MA **Lexington**
Nova Sales, 617-861-1820
MA **North Andover**
IDT Sales Office—Eastern Area, 617-689-9299
MN **Minneapolis**
Comprehensive Tech. Sales, 612-888-7011
NJ **Mt. Laurel**
Comtek Inc., 609-235-8505
NY **Buffalo**
Quality Components, 716-837-5430
NY **Jamaica**
SJ Associates, 212-291-3232
NY **Manlius**
Quality Components, 315-682-8885
NC **Cary**
Montgomery Marketing, 919-467-6319
OH **Cleveland**
Norm Case Assocs., 216-333-0400
TX **Austin**
IDT Sales Office—Central Area, 512-327-8441
TX **Austin**
OM Sales, 512-452-1838
TX **Dallas**
OM Sales, 214-241-3876
TX **Houston**
OM Sales, 713-789-4426
UT **Salt Lake City**
Elcom, 801-532-7940
WA **Kirkland**
Electronic Marketing Assoc., 206-827-9350
WI **Brookfield**
Circuit Sales, Inc., 414-784-3004
Can **Montreal, Quebec**
Bytewide Marketing Inc., 514-481-1167
Intl **Denmark, Kokkedal**
C-88, TEL: 02-24-48-88
Intl **England, Thame Oxon**
Micro Call, Ltd., TEL: 084-421
Intl **Finland, Helsinki**
Turion OY, TEL: 90-372-144
Intl **France, Lavallois Perret**
REA, TEL: 75-81-111
Intl **Germany, Munchen**
Scantec GmbH, TEL: 089-13-40-93
Intl **Israel, Herzlia**
Vectronics, Ltd., TEL: 052-556070
Intl **Italy, Milano**
Cefra s.r.l., TEL: 02-23-52-64
Intl **Netherlands, Eindhoven**
Auriema, TEL: 040-816565
Intl **Norway, Oslo**
Eltron A/S, TEL: 02-46-28-70
Intl **Sweden, Vallingby**
Svensk Teleindustri, TEL: 08-38-03-20
Intl **Switzerland, Zug**
Anatec, TEL: 042-31-54-77

Distributors

AZ **Tempe**
Anthem, 602-244-0900
CA **Chatsworth**
Anthem, 213-700-1000
CA **San Diego**
Anthem, 714-279-5200
CA **San Jose**
Anthem, 408-946-8000
CA **Tustin**
Anthem, 714-730-8000
CO **Denver**
ACT, 303-422-9229
IL **Chicago**
Bell Industries, 312-982-9210
NM **Albuquerque**
Alliance Electronics, Inc., 505-292-3360, 800-545-6288
OK **Tulsa**
Quality Components, 918-664-8812
TX **Addison**
Quality Components, 214-387-4949
TX **Austin**
ACT, 512-452-5254
TX **Austin**
Quality Components, 512-835-0220
TX **Dallas**
ACT, 214-980-1888
TX **Houston**
ACT, 713-496-4000
TX **Sugarland**
Quality Components, 713-491-2255
UT **Salt Lake City**
ACT, 801-487-8131
WI **Waukesha**
Bell Industries, 414-784-0235

Integrated Technology

Integrated Technology Corporation
1233 N. Stadem Dr.
Tempe,, Arizona 85281
602-968-3459

Intel

Intel Corporation
3065 Bowers Avenue
Santa Clara, California 95051
408-987-8080
TELEX: 34-6372
TWX: 910-338-0026

Sales Office & Representatives

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Intel Corp., 205-533-9353
AZ **Phoenix**
Intel Corp., 602-869-4980
CA **Mountain View**
Intel, 415-968-8086
CA **Sacramento**
Intel Corp., 916-929-4078
CA **San Diego**
Intel Corp., 619-268-3563
CA **Santa Ana**
Intel Corp., 714-835-9642
CA **Tarzana**
Intel Corp., 213-708-0333
CO **Colorado Springs**
Intel Corp., 303-594-6622
CO **Denver**
Intel Corp., 303-321-8086
CT **Danbury**
Intel Corp., 203-792-8366
FL **Ft. Lauderdale**
Intel Corp., 305-771-0600
FL **Maitland**
Intel Corp., 305-628-2393
GA **Norcross**
Intel Corp., 404-449-0541
IL **Rolling Meadows**
Intel Corp., 312-981-7200
IN **Indianapolis**
Intel Corp., 317-875-0623
IA **Cedar Rapids**
Intel Corp., 319-393-5510
KS **Overland Park**
Intel Corp., 913-642-8080
MD **Hanover**
Intel Corp., 301-796-7500
MA **Chelmsford**
Intel Corp., 617-256-1800
MI **Southfield**
Intel Corp., 313-353-0920

Intel (Cont)

MN **Bloomington**
Intel Corp., 612-835-6722

MO **Earth City**
Intel Corp., 314-291-1990

NJ **Edison**
Intel Corp., 201-225-3000

NM **Albuquerque**
BFA Corp., 505-292-8086

NY **Hauppauge**
Intel Corp., 516-231-3300

NY **Poughkeepsie**
Intel Corp., 914-473-2303

NY **Rochester**
Intel Corp., 716-424-1050

NC **Charlotte**
Intel, 704-568-8966

NC **Greensboro**
Intel Corp., 919-294-1541

OH **Cleveland**
Intel Corp., 216-464-2736

OH **Dayton**
Intel Corp., 513-890-5350

OK **Tulsa**
Intel Corp., 918-749-8688

OR **Beaverton**
Intel Corp., 503-641-8086

PA **Fort Washington**
Intel Corp., 215-641-1000

PA **Pittsburgh**
Intel Corp., 412-823-4970

TX **Austin**
Intel Corp., 512-454-3628

TX **Dallas**
Intel Corp., 214-241-8087

TX **Houston**
Indl. Digital Sys. Corp., 713-988-9421

TX **Houston**
Intel Corp., 713-988-8086

UT **Salt Lake City**
Intel Corp., 801-533-8086

VA **Falls Church**
Intel, 703-790-1191

VA **Richmond**
Intel Corp., 804-282-5668

WA **Bellevue**
Intel Corp., 206-453-8086

WI **Brookfield**
Intel Corp., 414-784-9060

Can **Ottawa, Ontario**
Intel Corp., 613-829-9714

Can **Rexdale, Ontario**
Intel Corp., 416-675-2105

Intl **Australia, Crows Nest, NSW**
Intel Semiconductor Pty. Ltd., TEL: 011-61-2-436-2-2744

Intl **Belgium, Brussels**
Inelco Belgium S.A., TEL: (02) 216 01 60

Intl **Belgium, Brussels**
Intel Corp. S.A., TEL: (02) 661 07 11

Intl **Brazil, Pirituba Sao Paulo**
Icotron S.A., TEL: 261-0211

Intl **Chile, Santiago**
DIN, TEL: 227 564

Intl **China, Hong Kong**
Schmidt & Co. Ltd., TEL: 5-8521-222

Intl **Colombia, Bogota**
Intl. Computer Machines, TEL: 057-211-7282

Intl **Denmark, Copenhagen East**
Intel Denmark A/S, TEL: (01) 18 20 00

Intl **Denmark, Glostrup**
MultiKomponent A/S, TEL: 011-65-271-3163

Intl **Finland, Helsinki**
Intel Finland OY, TEL: 0/716 955

Intl **Finland, Helsinki**
Oy Fintronic AB, TEL: 90 692 60 22

Intl **France, Asnieres**
Metrologie, TEL: (1) 791 44 44

Intl **France, Bagnolet**
Jermyn S.A., TEL: (1) 859 04 04

Intl **France, Rungis Cedex**
Intel Corp., S.A.R.L., TEL: (01) 687 22 21

Intl **France, Sevres**
Tekelec Airtonic, TEL: (01) 534 75 35

Intl **Germany, Camberg**
Jermyn GmbH, TEL: (06434) 231

Intl **Germany, Fellbach**
Intel Semiconductor GmbH, TEL: (711) 58 00 82

Intl **Germany, Hannover**
Intel Semiconductor GmbH, TEL: (511) 34-40-81

Intl **Germany, Muenchen**
Intel Semiconductor GmbH, TEL: (89) 53891

Intl **Germany, Munich**
Electronic 2000 Vertriebs GmbH, TEL: (89) 43 40 61

Intl **Germany, Wiesbaden**
Intel Semiconductor GmbH, TEL: (6121) 70 08 74

Intl **Hong Kong**
Schmidt & Co. Ltd., TEL: 5-8521-222

Intl **Hong Kong, Hong Kong**
Intel Semiconductor Corp., TEL: 011-852-5-450-855

Intl **India, Bombay**
Micronic Devices, TEL: 486-170

Intl **Israel, Haifa**
Intel Semiconductor Ltd., TEL: 4/524 261

Intl **Israel, Tel Aviv**
Eastronics Ltd., TEL: (3) 47 51 51

Intl **Italy, Assago (Milano)**
Intel Corp. Italia Spa, TEL: (02) 824 00 06

Intl **Italy, Milano**
Eledra 3S S.P.A., TEL: (2) 34 97 51

Intl **Japan, Ibaraki-Ken**
Intel Japan K.K., TEL: 029747-8511

Intl **Japan, Kitakyushu City**
Asahi Elctrns. Co. Ltd., TEL: (093) 511-6471

Intl **Japan, Tokyo**
Hamilton-Avnet Elctrns. Japan Ltd., TEL: (03) 662-9911

Intl **Japan, Tokyo**
Ryoyo Elec. Corp., TEL: (03) 543-7711/541-7311

Intl **Japan, Tokyo**
Tokyo Electron Ltd., TEL: (03) 343-4411

Intl **Korea, Seoul**
Koram Digital, TEL: 782-8039/782-8049

Intl **Lyon, France**
Intel Corp., TEL: (7) 842-40-89

Intl **Madrid, Spain**
Intel Iberia, TEL: (01) 410-40-04

Intl **Munich, Germany**
Metrologic, TEL: (89) 57 30 84

Intl **Netherlands, Gravenhage**
Koning & Hartman, TEL: 31 (70) 210.101

Intl **Netherlands, Rotterdam**
Intel Semiconductor Nederland B.V., TEL: (10) 21 23 77

Intl **New Zealand, Auckland**
McLean Information Technlg. Ltd., TEL: 501-801, 501-219, 587-037, 587-037

Intl **Norway, Hvalstad**
Nordisk Elektronic (Norge) A/S, TEL: (2) 786 210

Intl **Norway, Skjetten**
Intel Norway A/S, TEL: (2) 742 420

Intl **Portugal, Lisboa**
Ditram, TEL: (19) 545 313

Intl **Singapore, Singapore**
General Engrs. Corp. Pty. Ltd., TEL: 011-65-271-3163

Intl **South Africa, Pretoria**
Elctrn. Bldg. Elements, Pty. Ltd., TEL: 011-27-12-46-9221, 011-27-12-46-9227

Intl **Spain, Barcelona**
Interface S.A., TEL: (3) 301 78 51

Intl **Spain, Madrid**
ITT SESA, TEL: (1) 419 54 00

Intl **Sweden, Bromma**
Intel Sweden A.B., TEL: (08) 98 53 85

Intl **Sweden, Stockholm**
AB Gosta Backstrom, TEL: (8) 541 080

Intl **Sweden, Stockholm**
Nordisk Electronik AB, TEL: (8) 635 040

Intl **Switzerland, Zurich**
Industrade AG, TEL: (1) 363 22 20

Intl **Switzerland, Zurich**
Intel Semiconductor A.G., TEL: (01) 55 45 02

Intl **Taiwan, Taipei**
Taiwan Automation Co., TEL: 771-0940, 771-0941

Intl **United Kingdom, Berkshire**
Bytech Ltd., TEL: (0734) 61031

Intl **United Kingdom, Berkshire**
Comway Microsystems Ltd., TEL: 44 (344) 55333

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Schweber Elctrns., 714-863-0269
CA **Irvine**
Wyle Distribution Grp., 714-863-9953
CA **Irvine**
Wyle Military, 714-851-9953
CA **Los Angeles**
Kierulff Elctrns., 213-725-0325
CA **Newport Beach**
Arrow Electronics, 714-851-8961
CA **Palo Alto**
Kierulff Elctrns., 415-968-6292
CA **Sacramento**
Schweber Electronics, 916-929-9732
CA **San Diego**
Anthem Elctrns., Inc., 619-453-9005
CA **San Diego**
Arrow Elctrns., 619-565-4800
CA **San Diego**
Wyle Distribution Grp., 619-565-9171
CA **San Jose**
Anthem Elctrns. Inc., 408-946-8000
CA **Santa Clara**
Schweber Electronics, 408-748-4700
CA **Santa Clara**
Wyle Distribution Grp., 408-727-2500
CA **Sunnyvale**
Arrow Elctrns., 408-745-6600
CA **Tustin**
Kierulff Elctrns., 714-731-5711

Kontron Electronics (Cont)

Intl **Portugal, Lisboa Codex**
Mattos Tavares Electronics Lda, TEL: 00351-19-616261
Intl **South Africa, Sandton**
Biowave Electronics, SA, TEL: 0027-485808
Intl **Spain, Madrid**
Belport Instrumentation SA, TEL: 00341-2628837
Intl **Spain, Madrid**
Hispano Electronics SA, TEL: 0034-1-6194108
Intl **Sweden, Sundyberg**
AB Transfer, TEL: 0045-8981620
Intl **Sweden, Upplands Vasby**
Lagercrantz Elektronik AB, TEL: 0046-760-86120
Intl **Switzerland, Epalinges**
Kontron Electronic AG, TEL: 0041-21331535
Intl **Switzerland, Zurich**
Kontron Instruments AG, TEL: 0041-1-4354111
Intl **West Germany, Eching bei Muchen**
Kontron Messtechnik GmbH, TEL: 0049-89-31901-0

Distributors

Intl **Australia, Melbourne**
Parameters, TEL: 03-580-7444
Intl **Australia, Sydney**
Parameters, TEL: 02-439-3288
Intl **Brazil, Sao Paulo, Rio, Porto Alegre**
Cosele Instrumentos Electronicos, TEL: 255-1733
Intl **Finland, Helsinki**
OY Ammet AB, TEL: 0035-80-882044
Intl **Hong Kong, Kwun Tong**
Hong Kong Equipment Center, TEL: 3-413888
Intl **India, Banagalore**
SRI RAM Associates
Intl **Korea, Seoul**
Duksung Trading Co., TEL: 854-5047, 5831
Intl **New Zealand, Aukland**
Professional Electronics, TEL: 493-029
Intl **Singapore, Singapore**
Singapore Electronic & Engineering (Private) Ltd., TEL: 257-0211
Intl **Taiwan, Taipei**
Gorman Co., Ltd., TEL: 02-5421924

Kontron Electronics

Kontron Electronics, Inc.
FutureData Division
5730 Buckingham Parkway
Culver City, California 90230
213-641-7200
TWX: 910-328-7202

Sales Office & Representatives

Intl **Austria, Wein**
Kontron Elektronik GmbH & Co., TEL: 0043-222-670631-0
Intl **Belgium, Brussels**
C.N. Rood B.V., TEL: 0032-2-7352135
Intl **Denmark, Hoersholm**
E. Blichfeld APS, TEL: 0045-2867900
Intl **Finland, Helsinki**
OY Emmet AB, TEL: 0035-80-882044
Intl **France, Velizy-Villacoublay**
Kontron Electronique, TEL: 00331-946722
Intl **Great Britain, St. Albans**
Kontron Instruments Ltd., TEL: 0044-727-66222
Intl **Israel, Haifa**
Tabor Electronics, TEL: 00972-4-644280
Intl **Italy, Cinecello Balsamo**
Celdis, TEL: 0039-2-6120041
Intl **Italy, Milano**
Telav International SRL, TEL: 0039-2-4455741
Intl **Netherlands, Rijswijk**
C.N. Rood B.V., TEL: 0031-70-996360
Intl **Norway, Oslo**
Bergman Instrumentering A/S, TEL: 0047-2-162210
Intl **Portugal, Lisboa Codex**
Mattos Tavares Electronics Lda, TEL: 00351-19-616261
Intl **South Africa, Sandton**
Biowave Electronics, SA, TEL: 0027-485808
Intl **Spain, Madrid**
Belport Instrumentation SA, TEL: 00341-2628837
Intl **Spain, Madrid**
Hispano Electronics SA, TEL: 0034-1-6194108
Intl **Sweden, Sundyberg**
AB Transfer, TEL: 0045-8981620
Intl **Sweden, Upplands Vasby**
Lagercrantz Elektronik AB, TEL: 0046-760-86120
Intl **Switzerland, Epalinges**
Kontron Electronic AG, TEL: 0041-21331535
Intl **Switzerland, Zurich**
Kontron Instruments AG, TEL: 0041-1-4354111
Intl **West Germany, Eching bei Muchen**
Kontron Messtechnik GmbH, TEL: 0049-89-31901-0

Distributors

Intl **Australia, Melbourne**
Parameters, TEL: 03-580-7444
Intl **Australia, Sydney**
Parameters, TEL: 02-439-3288
Intl **Brazil, Sao Paulo, Rio, Porto Alegre**
Cosele Instrumentos Electronicos, TEL: 255-1733
Intl **Hong Kong, Kwun Tong**
Hong Kong Equipment Center, TEL: 3-413888
Intl **India, Banagalore**
SRI RAM Associates
Intl **Korea, Seoul**
Duksung Trading Co., TEL: 854-5047, 5831
Intl **New Zealand, Aukland**
Professional Electronics, TEL: 493-029
Intl **Singapore, Singapore**
Singapore Electronic & Engineering (Private) Ltd., TEL: 257-0211
Intl **Taiwan, Taipei**
Gorman Co., Ltd., TEL: 02-5421924

Lambda

Lambda Semiconductors
121 International Drive
Corpus Christi, Texas 78410
512-289-0403 (In Texas); 1-800-255-9606
TWX: 910-876-1404

Sales Office & Representatives

Intl **England, High Wycombe, Bucks**
Lambda Electronics, TEL: 44-494-36386
Intl **France, Les Ulis, Cedex**
Lambda Electronique S.A., TEL: 33-6-012-1487
Intl **Germany, Achern**
Lambda Netzgerate GmbH, TEL: 49-7841-5031
Intl **Israel, Tel Aviv**
IsLambda Electronics Ltd., TEL: 972-3-242-194
Intl **Japan, Tokyo**
Nemic-Lambda K.K., TEL: 03-490-5

Linear Technology Corpo

Linear Technology Corporation
1630 McCarthy Blvd.
Milpitas, California 95035-7487
408-942-0810
TELEX: 172 110

Distributors

Intl **Austria**
Bacher Elektronische Gerate GmbH
222-835646
Intl **Belgium**
Microtron, TEL: 32-16-60586
Intl **Denmark**
E. V. Johanssen Elektronik A/S, T
839033
Intl **Finland**
OY Fintronic AB, TEL: 358-0-6926
Intl **France**
Tekelec Airtronic, TEL: 33-1-5347
Intl **Italy**
Eledra 3 S S.P.A., TEL: 39-2-3497
Intl **Japan**
Japan Macnics Corporation, TEL:
0022
Intl **Japan**
Technology Trading Corporation,
03-639-5581
Intl **Japan**
Teijin Advanced Products Corpora
044-506-4670
Intl **Netherlands**
Alcom Electronics BV, TEL: 31-10
Intl **Norway**
Eltron A/S, TEL: 47-2-462870
Intl **Spain**
Amitron, S.A., TEL: 34-1-2485863
Intl **Sweden**
Svensk Teleindustri, TEL: 46-8-3
Intl **Switzerland**
Stolz AG, TEL: 41-56-840151
Intl **United Kingdom**
Dialogue Distribution, Ltd., TEL:
682001
Intl **United Kingdom**
Microcall, Ltd., TEL: 44-84421-54
Intl **West Germany**
Alfred Neye, TEL: 49-4106-6121
Intl **West Germany**
Metronik, TEL: 49-89-6114063
Intl **Yugoslavia**
Ellyptic AG, TEL: 41-1-4931000

LSI Computer Systems

LSI Computer Systems, Inc.
1235 Walt Whitman Road
Melville, New York 11747
516-271-0400
TWX: 510-226-7833
Specific product information:
Ronald Colino
Application engineering:
Ronald Colino
Literature:
Nancy Leidig
Price and delivery:
Nancy Leidig
Follow-up an order:
Nancy Leidig
All other information:
Nancy Leidig
For Intl. sales: Mavex Technology, 516-47

LSI Computer Systems (Cont)

Sales Office & Representatives

AL **Huntsville**
REMCO, 205-533-3763
CA **Santa Clara**
Fischer Assocs., 408-733-7350
CA **Westlake Village**
Western Mktg., 213-889-6270
GA **Atlanta**
REMCO, 404-477-6937
IL **Elmhurst**
Fiat Engrg. Assocs., 312-547-6200
MD **Fulton**
Gans & Pugh, Inc., 301-953-3724
NH **Merrimack**
Mech-Tron Co., 603-424-5300
NJ **Hasbrouck Heights**
Comp-Tech Sales, 201-288-7400
NY **New Hyde Park**
Comp-Tech Sales, 516-593-2628
NY **Penfield**
Barthel Entprs., 716-377-3018
NC **Raleigh**
REMCO, 919-847-5079
OH **Cleveland**
Components, Inc., 216-243-9200
OH **West Carrollton**
Components, Inc., 513-866-0661
TX **Houston**
Electronic Mktg. Assoc., 713-498-8120
VA **Arlington**
Gans & Pugh, Inc., 703-527-3262

LSI Logic

LSI Logic Corporation
1601 McCarthy Boulevard
Milpitas, California 95035
408-263-9494
TELEX: 172 153

Sales Office & Representatives

AL **Huntsville**
Montgomery Marketing, 205-830-0498
AZ **Scottsdale**
Luscombe Engineering, 602-949-9333, TWX 910-950-1333
CA
LSI Logic Milpitas, 408-263-9494, TLX 172153
CA **(Northern)**
Taarcom, Inc., 415-960-1550, TWX 296991
CA **(Southern)**
Centaur Corporation, 714-556-5420, TWX 910-595-2887
CO **Littleton**
Simpson Associates, 303-794-8381, TWX 910-935-0719
CT **Waterbury**
HLM Associates, 203-753-9894
FL **Altamonte Springs**
Semtronic Associates, 305-831-8233
GA **Norcross**
Montgomery Marketing, 404-447-6127
IL **(Southern)**
Design Solutions, 314-227-7170
MD **Columbia**
Delta III Associates, 301-730-4700, TWX 710-862-1906
MI **Detroit**
Rathsburg Associates, 313-882-1717
MN **Minneapolis**
HMR, 612-831-7400
MO **St. Louis**
Design Solutions, 314-227-7170
NY **Rochester**
T-Squared Electronics, 716-924-9101, TWX 510-254-8542
NC **Cary**
Montgomery Marketing, 919-467-6319, TWX 510-920-0634
OR **Portland**
Westerberg & Associates, 503-297-1719
TX **Dallas**
Technology Sales, 214-380-0200
UT **Salt Lake City**
Simpson Associates, 801-566-3691
WA **Bellevue**
Westerberg & Associates, 206-453-8881
WI **(East)**
Oasis Sales, 312-640-1850
WI **(West)**
HMR, 612-831-7411, TLX 029-0537;TWX 910-576-2755
Can **B.C.**
Westerberg & Associates, 206-453-8881, TWX 910-443-2319
Can **Ottawa, Ontario**
RFQ Limited, 613-820-8445, TWX 610-562-1973

Master Logic

Master Logic Corporation
761 E. Evelyn Avenue
Sunnyvale, California 94086
408-732-7777
Specific product information:
Stephen R. Allen
Application engineering:
Stephen R. Allen
Literature:
Stephen R. Allen
Price and delivery:
Stephen R. Allen
Follow-up an order:
Stephen R. Allen
All other information:
Charles A. Allen

Matrix

Matrix Corporation
1639 Green Street
Raleigh, North Carolina 27603
919-833-2837

Matrox

Matrox Electronic Systems Ltd.
5800 Andover Avenue, T.M.R.
Montreal, Quebec, H4T 1H4, Canada
514-735-1182
TELEX: 05-825651

Sales Office & Representatives

Intl **Australia, Epping**
Mace Co. Pty. Ltd., TEL: 86-4060
Intl **Austria, Vienna**
Bacher Elektronishe Gerate, Ges. m.b.h., TEL: (0220) 835646-0
Intl **Denmark, Glostrup**
Jorgen Andersen Ingeniorfirma A.S., TEL: (02) 92 88 88
Intl **England, London**
Perdix Comps., TEL: 01-690 1914/5
Intl **Finland, Helsinki**
Oy Fintronic, AB, TEL: 90-692 60 22
Intl **France, Asnieres**
Metrologie, TEL: 791 44 44
Intl **Greece, Athens**
American Tech. Entprs. S.A., TEL: 8219.470-8811.271
Intl **Israel, Givatayim**
EIM Intl. Elctrns. Ltd., TEL: (03) 744-041
Intl **Italy, Milano**
3-G Elctrns. s.r.l., TEL: 5455951
Intl **Japan, Tokyo**
Internix Inc., TEL: 369-1101
Intl **Netherlands, Drimmelen**
Matrox Benelux, TEL: 01626-3850
Intl **New Zealand, Auckland**
GTS Engrg., Ltd., TEL: 546-745
Intl **Norway, Oslo**
Nordisk Electronik AS, TEL: 02-55-2485
Intl **Portugal, Lisboa**
Ditram Components E Electronics Lta
Intl **Spain, Madrid**
Unitronics S.A., TEL: 242-52-04
Intl **Sweden, Partille**
Micro Scandia Industriautomation AB, TEL: 32685
Intl **Switzerland, Zurich**
Relais-Rohr, TEL: (01) 301 09 70
Intl **Taiwan, Taipei**
Multitech Intl. Corp., TEL: (02) 7681232
Intl **West Germany, Munchen**
Ernst Rauscher Systemberatung, TEL: 089-878061

Maxim Integrated Products

Maxim Integrated Products
510 N. Pastoria
Sunnyvale, California 94086
408-737-7600

Micrel

Micrel
1235 Midas Way
Sunnyvale, California 94086
408-245-2500
TWX: 910-379-0007

MCE

MCE Semiconductor
1111 Fairfield Drive
W. Palm Beach, Florida 33407
305-845-2837
TELEX: 513463 (MCE NPAB)

Sales Office & Representatives

Intl **United Kingdom, Tewkesbury**
MCE, Ltd., TEL: 0684-297777
Intl **West Germany, Munich**
MCE Micro-Circuit Engrg. Vertr. GmbH, TEL: 089-463085
Intl **West Germany, Nuernberg**
MCE Micro-Circuit Engrg. Vertr. GmbH, TEL: 0911-533933

Microcircuits Technology

Microcircuits Technology, Inc.
1157 San Antonio Road
Mountain View, California 94043
415-969-3600
TELEX: 172 750

Micro Computer Control

Micro Computer Control
P.O. Box 275
Hopewell, New Jersey 08525
609-466-1751

Micro Innovators

Micro Innovators Inc.
2348A Walsh Avenue
Santa Clara,, California 95051
408-988-0911

Micro-Link

Micro-Link Corporation
14602 N. U.S. Hwy 31
Carmel, Indiana 46032
317-846-1721
TWX: 810-260-2634

Distributors

Intl **Buc, France**
YREL, TEL: 956-8142
Intl **Taeby, Sweden**
EM Marketing AB, TEL: 46 0762 13570
Intl **Worms, W. Germany**
GK Electronics, TEL: 062-41-5-32-99

Micro Networks

Unitrode Corporation
Micro Networks Company
324 Clark Street
Worcester, Massachusetts 01606
617-852-5400
TELEX: 951808
TWX: 710-340-0067
Specific product information:
Mark Vaughan .... Ext. 219
Application engineering:
Mark Vaughan .... Ext. 219
Literature:
Karen LaVigne .... Ext. 220
Price and delivery:
Linda Palmer .... Ext. 275
Follow-up an order:
Linda Palmer .... Ext. 275
All other information:
John Munn .... Ext. 225

Sales Office & Representatives

Intl **Australia, Burwood**
R & D Elctrns., TEL: 288-8232
Intl **Austria, Bad Voeslau**
Kapla Electronik, TEL: 02252-7459
Intl **Belgium, Brussels**
Belram S.A., TEL: 34.33.32
Intl **Belgium, Braxelles**
I.S.I., TEL: 02/660-13 56
Intl **Cyprus, Nicosia**
Poly Elctrns., TEL: 21-27982
Intl **Denmark, Copenhagen**
Semicap, TEL: 01-221510
Intl **England, Sunbury-on-Thames**
Pascall Elctrns. Ltd., TEL: Sunbury, 09327-87418
Intl **Finland, Helsinki**
Turion OY, TEL: 90-377787
Intl **France, Orsay**
Microel, TEL: 6-9070824
Intl **Germany, Munchen**
Tekelec Airtronic, TEL: (089) 594-621
Intl **Greece, Athens**
Theodore D. Tzitzinias, TEL: 942 4071
Intl **Hong Kong, Hong Kong**
Schmidt & Co. (H.K.) Ltd., TEL: 5-455644
Intl **India, Trivandrum**
Kryonix, TEL: 63805
Intl **Israel, Bnei Brak**
Electrondart Ltd., TEL: 3-782460
Intl **Italy, Milano**
Microelit S.R.L., TEL: 46.90.444
Intl **Japan, Tokyo**
Internix, TEL: (03) 369-1101
Intl **Korea, Seoul**
Han Sun Intl., TEL: 28-0958
Intl **Netherlands, Breda**
Indelec B.V., TEL: 076-142333
Intl **Norway, Oslo**
Eltron, TEL: 02-15-20-51
Intl **South Africa, Bryanston**
S'Electronics
Intl **Spain, Madrid**
Compania Electronica de Technicas, TEL: 754-4530
Intl **Sweden, Vallingby**
Scancopter, TEL: 08/38 00 65
Intl **Switzerland, Zurich**
Telemeter AG, TEL: 01-202-7872
Intl **Taiwan, Taipei**
Tai I Trading Co., Ltd., TEL: 393 61111

Micropac

Micropac Industries, Inc.
905 East Walnut Street
Garland, Texas 75040
214-272-3571
TWX: 910-860-5186
All other information:
Ext. 23, 37

Sales Office & Representatives

Intl **Austria, Wien**
Transistor Vertriebs, TEL: 0043/222829451
Intl **Belgium, Brussels**
Manudax, TEL: 00322/22152500
Intl **Denmark, Copenhagen**
Semicap, TEL: 00451/221510
Intl **France, Boulogne**
ASAP, TEL: 00331/6047878
Intl **France, Paris**
Comptoir Commercial D'Importation (CCI), TEL: 00331/2362045
Intl **Great Britain, Thame-Oxford**
Gain Elctrns., TEL: 0044/844215477
Intl **Great Britian, Harrold-Bedford**
Synchro Svcs., TEL: 0044/234720575
Intl **Italy, Milano**
El Pack S.R.I., TEL: 00392/6471673
Intl **Netherlands, Nijmegen**
Varilec B.V., TEL: 00318/0445660
Intl **Norway, Tonsbert**
UMI A.S., TEL: 004733/22214
Intl **Sweden, Solna**
AB Betoma, TEL: 00468/820280
Intl **Switzerland, Baden**
Comeltec AG, TEL: 004156/223152
Intl **Switzerland, Zurich**
Egli, Fischer Co. Ltd., TEL: 00411/2020234
Intl **West Germany, Geesthacht**
Microlec, TEL: 04152/72324
Intl **West Germany, Homberg**
IV Elctrn., TEL: 06172/23061
Intl **West Germany, Munich**
DIPL-Ing. Ernst Fey Nachf, TEL: 089-184041
Intl **West Germany, Munich**
Neumueller GmbH, TEL: 089/61181
Intl **West Germany, Munich**
Nucletron Vertriebs GmbH, TEL: 089/146081
Intl **West Germany, Stuttgart**
Ditronic GmbH, TEL: 0711/724844

Micro Power Systems

Micro Power Systems, Inc.
3100 Alfred Street
Santa Clara, California 95050
408-727-5350
TWX: 910-338-0154
Specific product information:
Standard Products Division .... ext. 237
Literature:
Standard Products Division .... ext. 237

Sales Office & Representatives

AL **Huntsville**
R.W. Mitscher Co., Inc., 205-852-7676
AZ **Tempe**
Sun West Mktg. Assoc., 602-241-8163
CA **Los Alamitos**
Reed Elec. Mktng., 213-598-6676, 714-821-9600
CA **San Diego**
D½32 Sales, Inc., 619-560-6266
CA **Sunnyvale**
NES, 408-980-1950
CO **Littleton**
Quatra Inc., 303-795-3187
FL **Clearwater Beach**
Perrott Assocs., Inc., 813-443-5214
FL **Orlando**
Perrott Assocs., Inc., 305-298-7748
GA **Lawrenceville**
R.W. Mitscher Co., Inc., 404-923-3239
IL **Arlington Heights**
Coombs Assoc., 312-439-9810
IL **Rolling Meadows**
KMA Sales, 312-398-5300
IN **Ft. Wayne**
Coombs Assocs., 219-747-7661
IA **Marion**
REP Assocs., 319-373-0152
KS **Parker**
S.W. Woolard Co., 913-898-6552
KY **Louisville**
K.W. Elctrn. Sales, 502-451-1860
MD **Baltimore**
Stemler Assocs., 301-944-8262
MA **Burlington**
Dynamic Sales of New England, 617-272-5676
MI **Livonia**
Lowell Wendt Mktg. Co., 313-464-2722
MI **Livonia**
Reptron Electronic, Inc., 313-525-2700
MN **Minneapolis**
Peterson Sales Assocs., 612-884-3483
MO **Rockville**
Stemler Associates, 301-774-2268
NJ **Freehold**
Comtronic Assoc., Inc., 201-431-3374
NJ **Marlton**
Stemler Assocs., 609-966-4070
NY **Bainbridge**
R.W. Mitscher Company, 607-967-7192
NY **Buffalo**
R.W. Mitscher Co., Inc., 716-633-7970
NY **Melville**
Comtronic Assocs., 516-249-0505
NY **N. Syracuse**
R.W. Mitscher Co., Inc., 716-586-4012
NY **Plainview**
Comtronic Assoc., Inc., 516-681-7936
NY **Red Hook**
R.W. Mitscher Co., Inc., 914-758-8375

Micro Power Systems (Cont)

NY **Rochester**
R.W. Mitscher Co., Inc., 716-227-0839
NY **Rockville**
Comtronic Assoc., Inc., 516-536-4020
NY **Staten Island**
Comtronic Assoc., Inc., 212-979-3973
NY **Whitestone**
Comtronic Assoc., Inc., 212-767-7461
NC **Raleigh**
R.W. Mitscher Company, 919-876-0160
OH **Dayton**
K.W. Elctrn. Sales, Inc., 513-890-2150
OH **Shaker Heights**
K.W. Elctrn. Sales, Inc., 216-491-9177
OH **Worthington**
K.W. Electronic Sales, Inc., 614-888-0483
OK **Tulsa**
Quality Component, 918-664-8812
OR **Tigard**
Elctrn. Comp. Sales, 503-245-2352
PA **Allison Park**
K.W. Electronic Sales, Inc., 412-487-4300
TN **Johnson City**
R.W. Mitscher Co., Inc., 615-282-6240
TN **Johnson City**
R.W. Mitscher Company, 615-282-6240
TX **Austin**
TMI, 512-835-0064
TX **Carrollton**
TMI, 214-387-3601
TX **Houston**
TMI, 713-777-9228
WA **Mercer Island**
Elctrn. Comp. Sales, 206-232-9301
WI **Milwaukee**
KMA Sales, 414-259-1771

Distributors

CA **Laguna Hills**
MP Systems, 714-770-6411
CA **Reseda**
Jan Devices, 213-708-1100
CA **Santa Ana**
Pacesetter Elctrns., 714-557-7131
CA **Sunnyvale**
Future Elctrns., 408-745-6570
CA **Sunnyvale**
Pacesetter Elctrns., 408-734-5470
CO **Wheatridge**
Bell Inds., 303-424-1985
CT **Danbury**
Pilgrim Elctrns., 203-792-7274
FL **Clearwater**
Diplomat Elctrns., 813-443-4515
FL **Orlando**
Chip Supply Company, 305-275-3810
GA **Atlanta**
Wholesale Industrial Elect., 404-447-8431
IL **Elk Grove Village**
GBL Goold Elctrns., 312-593-3220
MD **Baltimore**
Whitney Distrs., 301-944-8080
MA **Wilmington**
Aved Elctrns., Inc., 617-657-8310
MN **Minneapolis**
The Joel Co., 612-545-5669
NM **Albuquerque**
Alliance Elec., 505-292-3360
NY **Buffalo**
Summitt Distrs., 716-887-2800
NY **E. Syracuse**
Add Elctrns., 315-437-0300
OH **Englewood**
Argent Inds., 513-836-8633
OH **Solon**
REH Elctrns., 216-248-1636
SC **Columbia**
R.W. Mitscher Company, 803-736-4544
TX **Addison**
Quality Comps., Inc., 214-387-4949
TX **Austin**
Quality Comps., Inc., 512-835-0220
TX **Houston**
Quality Comps., Inc., 713-772-7100
UT **Salt Lake City**
Bell Industries, 303-795-3187
WA **Seattle**
Robert E. Priebe Co., 206-682-8242
WI **Mequon**
Taylor Elctrn. Co., 414-241-4321
Intl **Australia, Rozelle**
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Micro Sciences Corporation
145 Commack Road
Commack,, New York 11725
516-499-0635

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303 Airport Road
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803-242-9232

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Miller Technology Inc.
647 North Santa Cruz Avenue
Los Gatos, California 95030
408-395-2032

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Sunnyvale, California 94086
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TELEX: 172296 MELA SUVL.
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Santa Clara, CA 95050
408-970-9700

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Milgray Electronics, 203-795-0711

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Marshall Industries, 203-265-3822

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FL **Ft. Lauderdale**
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Marshall Industries, 305-841-1878

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Reptron, 813-855-4656

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GA **Dunwoody**
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Marshall, 617-272-8200

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MO **Maryland Heights**
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J-MAR Electronics, 201-772-6400

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NJ **Mt. Laurel**
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NJ **Totowa**
Diplomat, 201-785-1830

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NY **Pittsford**
Milgray Electronics, 716-385-9330

NY **Rochester**
Rochester Radio Supply, 716-454-7800

NEC Electronics (Cont)

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Electronic Marketing, 614-299-4161
OH **Columbus**
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Marshall Industries, 513-236-8088
OH **Independence**
Milgray Electronics, 216-447-1520
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TX **Austin**
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TX **Austin**
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WA **Bellevue**
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Carsten Electronics, 613-729-5138
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Can **St. Laurent, PQ**
Carsten Electronics, 514-334-8321
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MEMCO, 604-536-4243

Nitron

Nitron, Inc.
10420 Bubb Road
Cupertino, California 95014
408-255-7550
TWX: 910-338-0222

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Gate Array, Custom, Standard Products .... Ext. 204
Non-Volatile Memories .... Ext. 204
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Literature:
Ext. 210
Price and delivery:
Customer Service .... Ext. 210 408-255-7550
Follow-up an order:
Customer Service .... Ext. 210
All other information:
Marketing .... Ext. 201

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Burisch GMBH U Co KG, TEL: 022 (Wien) 387638
Intl **Denmark, Copenhagen**
Advanced Elctrn., TEL: 45-1-194433
Intl **England, Oxfordshire**
Peter Gray Elctrns., Ltd., TEL: Henley 6543
Intl **Italy, Milano**
Comprel, SRL, TEL: 02 6120641
Intl **Japan, Tokyo**
Jepico Corp., TEL: (03) 348-0611
Intl **Norway, Stroemmen**
A/S Kjellbakke, TEL: 02-7118 72
Intl **Spain, Barcelona**
Interface S.A., TEL: 93-301 78 51
Intl **Sweden, Vallingby**
~~Svensk Teleindustrie, TEL: 08-380320~~
Intl **Switzerland, Zuerich**
Ellyptic AG, TEL: 01-541100
Intl **United Kingdom, Surrey**
Robin Reynolds, TEL: Ashtead (03722) 72741

Octagon Systems

Octagon Systems Corporation
6501 West 91st Avenue
Westminster, Colorado 80030
303-426-8540

Ohio Scientific

Ohio Scientific
1333 S. Chillicothe Road
Aurora, Ohio 44202
216-562-2020

OKI Semiconductor

OKI Semiconductor, Inc.
1333 Lawrence Expressway, Suite 401
Santa Clara, California 95051
408-984-4842
TWX: 910-338-0508

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AL **Huntsville**
Electronic Sales, 205-533-1735
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Electronic Sales, 205-533-1735
AZ **Scottsdale**
Semi Systems, 602-991-1151
AZ **Scottsdale**
Semi-Systems AZ, 602-991-1151
CA **Irvine**
Southwest Regional Sales Office, 714-752-1843
CA **Los Alamitos**
Santana Sales, 714-827-9100
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Pro Associates, 408-358-3861
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Littlefield & Smith, 619-455-0055
CO **Aurora**
Electrodyne (Main Office), 303-695-8903
CO **Denver**
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FL **Clearwater Beach**
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FL **Orlando**
Perrott Assoc. (Main Office), 305-298-7748
FL **Sunrise**
Perrott Assoc., 305-792-2211
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John G. Twist Co. (Main Office), 312-593-0200
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Valentine & Assoc. (Main Office), 317-888-2260
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Valentine & Associates, 317-888-2260
IN **South Bend**
Valentine & Assoc., 219-288-7070
IA **Cedar Rapids**
C.H. Horn & Assoc., 319-393-8703
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KS **Wichita**
D.L.E. Electronics, 316-744-2126
MD **Columbia**
Delta III Associates, 301-730-4700
MD **Columbia**
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MA **Wellesley**
Northeast Regional Sales Office, 617-431-7944
MA **Wellsley**
Advanced Design Group, 617-431-7946
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Luebbe Sales, 313-477-3131
MN **Bloomington**
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MN **Bloomington**
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J.G. Twist Co., 612-835-2120
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Reagan/Compar Albany, Inc., 518-489-4777
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PAF Assocs. (Main Office), 516-360-0940
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Luebbe Sales, 614-431-0474
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Southeast Regional Sales Office, 215-674-9511
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J.G. Twist Co., 414-782-2670
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OKI Elec. Ind. Co. Ltd., TEL: 03/454-2111
Intl **West Germany, Dusseldorf**
OKI Elec. Europe GMBH, TEL: 0049/211-592031

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Ryno Elctrns. (Main Office), 619-292-6022
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Pacesetter Elctrns. (Main Office), 714-557-7131
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Milgray Elctrns., 404-393-9666
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Milgray Elctrns., 617-272-6800
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C & H Elctrns., 603-882-1133
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Action Electronics, 609-858-2450
NJ **Marlton**
Milgray Elctrns., 609-983-5010
NJ **Medford**
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Reptron Elctrns., 614-436-6675
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TX **Addison**
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UT **Salt Lake City**
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Oliver Advanced Engineering, Inc.
676 West Wilson Avenue
Glendale, California 91203
213-240-0080
TELEX: 194773
Specific product information:
Marketing & Sales Department 213-240-0080

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AMASCO, 213-516-8561
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Engrg. Prods. Assocs., Inc., 319-354-5344
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Comark, 617-359-8161
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Belcomp PVBA, TEL: 011/78 05 12
Intl **Brazil, Sao Paulo**
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Intl **Denmark, Horsholm**
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Intl **England, Alton, Hampshire**
MTL Microsystems, TEL: 0420-88022
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Microel "Le Parana", TEL: 907-08-24
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Scantec GmbH, TEL: (089) 134093
Intl **India, Bombay**
Echbee Corp., TEL: 25 34 89/25 83 41

Omnibyte

Omnibyte Corporation
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West Chicago, Illinois 60185
312-231-6880

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Measurement Systems Ltd., TEL: (44) 0635 45420
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Auriema Italia, TEL: 430, 602
Intl **Solna, Sweden**
Master Data AB, TEL: 08-83 01 55
Intl **Stuttgart, W. Germany**
Claus Polack, TEL: Telex 2627-7111038
Intl **Taiwan, Taipei**
Strong Electronics Co., Ltd., TEL: (02) 521-8826-7
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Rank Electronics Pty, Ltd., TEL: (03) 29 3724
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Omni Ray, TEL: (01) 47 8200

Onset

Onset Computer Corporation
199 Main Street, P.O. Box 1016
North Falmouth, Massachusetts 02556
617-563-2267

Optical Electronics

Optical Electronics Inc.
P.O. Box 11140
Tucson, Arizona 85734
602-624-8358
TWX: 910-952-1283

Panasonic

Panasonic Industrial Company/Electronic Components Division
Matsushita Electric Corporation of America
1 Panasonic Way
Secaucus, New Jersey 07094
201-348-5269
TWX: 710-992-8920

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Moulthrop Sales, Inc., 415-864-0550

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Conti-Younger Associates, Inc., 203-245-1136
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CBC Electronics, 305-755-1111
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CBC Electronics, 305-831-5380
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Electronic Sources, 503-684-0040
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Del Steffen & Associates, 412-276-7366
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Component Sales, 801-466-8623
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Astec Components, Ltd., 416-630-8463

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TAW Electronics, 213-846-3911
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Shelley Electronics, 213-998-3333
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Allied Electronics, 415-487-5250
CA **Irvine**
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Western Electromotive, 213-820-3777
CA **Mt. View**
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CA **San Diego**
Shelley Electronics, 619-453-7133
CA **San Diego**
Tauber Electronics Inc., 619-274-7242
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CA **San Jose**
Ratel Electronics, 408-946-4700
CA **Santa Clara**
Western Electromotive, 408-727-7411
CA **Sunnyvale**
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Shelley Electronics, 303-442-2718
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Denver/Wintronics, 303-934-2406
CO **Denver**
Integrated Electronics, 303-292-6121
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J.V. Electronics, 203-469-2321
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Intertec Components, 305-834-7777
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Dixie Electronic Inc., 404-772-2055
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IL **Palatine**
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Olive Electronics Inc., 314-426-4500
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Summit Distributors, 716-334-8110
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Dixie Electronics, 919-724-5961
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Hughes Peters Inc., 513-351-2000
OH **Columbus**
Hughes Peters Inc., 614-294-5351
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Dixie Electronics, 803-779-5332
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Dixie Electronics, 803-669-8201
SC **Greenville**
Dixie Electronics, 803-297-1430
TN **Gray**
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Allied Electronics, 817-336-5401
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UT **Midvale**
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UT **Salt Lake City**
Standard Supply, 801-486-3371
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Taylor Electric, 414-241-4321
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Can **Montreal, Quebec**
Electronic Wholesalers Ltd., 514-769-8851
Can **Montreal, Quebec**
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Electronic Wholesalers Ltd., 613-746-4413
Can **Ottawa, Ontario**
Prelco Electronics Ltd., 613-226-3491

Pico Design

Pico Design, Inc.
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Santa Clara,, California 95051
408-249-8090

Plessey Solid State

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Sales Office & Representatives

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R.W. Mitscher Co., Inc., 205-882-6050
AZ **Scottsdale**
Thorsen Desert States, Inc., 602-998-2444
CA **Irvine**
National Sales Office, 714-540-9979
CA **Irvine**
Southwest District Sales Office, 714-540-9979
CA **Irvine**
West Regional Sales Office, 714-540-9979
CA **Santa Clara**
Logan Sales, 408-496-0660
CA **Sunnyvale**
Northwest District Sales Office, 408-730-1111
CA **Thousand Oaks**
S.C. Cubed, 805-496-7307
CA **Tustin**
S.C. Cubed, 714-731-9206
CO **Englewood**
Dynatech, Inc., 303-773-2830
FL **Boca Raton**
Lawrence Associates, 305-368-7373
FL **Clearwater**
Lawrence Associates, 813-584-8110
FL **W. Melbourne**
Lawrence Associates, 305-724-8294
GA **Lawrenceville**
R.W. Mitscher Co., Inc., 404-923-3239
GA **Norcross**
Southeast Regional Sales Office, 404-447-6910
IL **Arlington Heights**
Micro Sales Inc., 312-956-1000
IL **Arlington Heights**
Midwest Regional Sales Office, 312-437-1860
IN **Ft. Wayne**
Central District Sales Office, 219-483-4863
IN **Indianapolis**
SAI Marketing Corp., 317-241-9276
KS **Merriam**
Midwest Tech. Sales, 913-236-8557
MD **Beltsville**
Applied Engineering Con., 301-595-5393
MA **Framingham**
Eastern District Sales Office, 617-872-2288
MI **Brighton**
SAI Marketing Corp., 313-227-1786
MN **Bloomington**
Electronics Sales Agency, 612-884-8291
NJ **Marlton**
B.G.R. Associates, 609-428-2440
NY **Hauppauge**
Eastern Regional Sales Office, 516-273-3060
NY **Hicksville**
Lorac Sales, 516-681-8746
NY **Skaneateles**
Robtron, Inc., 315-685-5731
NC **Charlotte**
R.W. Mitscher Co., Inc., 714-332-8490
NC **Raleigh**
R.W. Mitscher Co., Inc., 919-876-0160
OH **Centerville**
SAI Marketing Corp., 513-435-3181
OH **Shaker Heights**
SAI Marketing Corp., 216-751-3633
OH **Zanesville**
SAI Marketing Corp.
TN **Johnson City**
R.W. Mitscher Co., Inc., 615-282-6240
TX **Arlington**
W. Pat Fralia Co., Inc., 817-640-9101
TX **Austin**
W. Pat Fralia Co., Inc., 512-835-7911
TX **Houston**
W. Pat Fralia Co., Inc., 713-772-1572
UT **Bountiful**
Anderson Associates, 801-292-8991
WI **Brookfield**
Micro Sales Inc., 414-782-1171
Can **Bolton, Ontario**
MacKay Associates, 416-857-4302
Can **Burnaby**
RAE Industrial Electronics, 604-291-8866

Distributors

Can **Mississauga, Ontario**
GEC Canada Ltd., 416-624-8300

Polycore Electronics

Polycore Electronics Inc.
1107 Tourmaline Drive
Newbury Park, California 91320
805-498-8832;213-991-1061

Precision Monolithics

Precision Monolithics Inc.
1500 Space Park Drive
Santa Clara, California 95050
408-727-9222
TWX: 910-338-0528
Specific product information:
ext. 162
Application engineering:
ext. 162
Literature:
ext. 186
Price and delivery:
ext. 171
Follow-up an order:
ext. 171
All other information:
ext. 162

Sales Office & Representatives

AL **Huntsville**
EMA, 205-830-4030
AL **Huntsville**
Pioneer/Harvey Electronics, 205-837-9300
AZ **Scottsdale**
PMI Sales Office, 602-941-1946
AZ **Tempe**
Anthem Electronics, 602-244-0900
AZ **Tempe**
Bell Industries, 602-966-7800
CA **Los Angeles**
PMI Sales Office, 213-642-0142
CA **San Diego**
Bell Industries, 619-268-1277
CA **Santa Clara**
PMI Sales Office, 408-727-6616
CO **Littleton**
PMI Sales Office, 303-979-8533
CO **Wheatridge**
Bell Industries, 303-424-1985
CT **Unionville**
PMI Sales Office, 203-673-9995
FL **Longwood**
PMI Sales Office, 305-331-5133
FL **Orlando**
Pioneer/Harvey Electronics, 305-834-9090
FL **St. Petersburg**
Hall-Mark Electronics, 813-576-8691
GA **Atlanta**
EMA, 404-329-0530
GA **Gaithersburg**
Pioneer/Harvey Electronics, 301-921-0660
GA **Norcross**
Hall-Mark Electronics, 404-447-8000
GA **Norcross**
Pioneer/Harvey Electronics, 404-448-1711
IL **Schaumburg**
PMI Sales Office, 312-885-8440
IN **Indianapolis**
PMI Sales Office, 800-323-8755
KS **Merriam**
PMI Sales Office, 800-323-8755
MD **Lutherville**
PMI Sales Office, 301-882-9222
MA **Natick**
PMI Sales Office, 617-655-8900
MA **Westborough**
Future Electronics, 617-366-2400
MI **Brighton**
PMI Sales Office, 800-323-8755
MN **Bloomington**
PMI Sales Office, 800-323-8755
MN **Minneapolis**
Merit Electronics Corp., 612-546-5383
MN **Minnetonka**
Pioneer/Harvey Electronics, 612-935-5444
NJ **Cherry Hill**
Hall-Mark Electronics, 609-424-7300
NJ **Fairfield**
Hall-Mark Electronics, 201-575-4415
NY **East Syracuse**
L-MAR Assocs., Inc., 315-437-7779
NY **Hicksville**
J-Square Mktg., Inc., 516-935-3200
NY **Rochester**
L-MAR Assocs., Inc., 716-323-1000
NC **Charlotte**
Pioneer/Harvey Electronics, 704-527-8188
NC **Raleigh**
EMA, 919-781-4139
OH **Dayton**
Del Steffen & Assocs., 513-293-3145
OH **Lexington**
Del Steffen & Assocs., 419-884-2313
OH **Westerville**
Hall-Mark Electronics, 614-891-4555
OR **Portland**
Bell Industries, 503-241-4115
PA **Cornwells Heights**
PMI Sales Office, 215-639-9595
PA **Pittsburgh**
Del Steffen & Assocs., 412-276-7366
TX **Dallas**
PMI Sales Office, 214-341-1742
TX **Dallas**
Pioneer/Harvey Electronics, 214-386-7300
TX **Houston**
PMI Sales Office, 713-481-6460
TX **Houston**
Pioneer/Harvey Electronics, 713-988-5555
WA **Bellevue**
PMI Sales Office, 206-641-6008
WA **Redmond**
Anthem Electronics, 206-881-0850
Can **Brampton, Ontario**
Zentronics, 416-451-9600
Can **Calgary, Alberta**
Future Electronics, Inc., 408-259-6408
Can **Calgary, Alberta**
Zentronics, 403-272-1021
Can **Edmonton, Alberta**
Intek Electronics Ltd., 403-437-2755

Precision Monolithics (Cont)

Can **Nepean, Ontario**
Zentronics, 613-226-8840
Can **Rexdale, Ontario**
Source Elctrns. Ltd., 416-675-6235
Can **Richmond, B.C.**
Zentronics, 604-273-5575
Can **Vancouver, B.C.**
Future Electronics, Inc., 604-438-5545
Can **Waterloo, Ontario**
Zentronics, 519-884-5700
Can **Winnepeg, Manitoba**
Zentronics, 204-775-8661
Intl **Australia, Victoria**
RIFA, TEL: 03-480-1211
Intl **Austria, Vienna**
Ing. Otto Folger, TEL: 0222/ 43 26 39
Intl **Benelux, Voorburg**
Bourns (Nederland) B.V., TEL: 070 87 44 00
Intl **Denmark, Ballerup**
Tage Olsen A/S, TEL: 02-65 81 11
Intl **Eastern Europe, Vienna**
Eltrans, TEL: 0222/24 71 37
Intl **Finland, Helsinki**
Insele Oy, TEL: 80/73 57 74
Intl **France, Paris**
Ohmic S.A., TEL: 01/203 9633
Intl **Germany, Stuttgart**
Bourns GmbH, TEL: 0711/24 29 36
Intl **Greece, Athens**
Germanis Co., TEL: 01-821 5825
Intl **India, Bombay**
Hindco Corp., TEL: 373544
Intl **Israel, Tel Aviv**
Rapac Elctrns. Ltd., TEL: 03-47 71 15
Intl **Italy, Milan**
Technic S.r.L., TEL: 02/569 57 46
Intl **Japan, Tokyo**
Nippon PMI Corp., TEL: (03) 234-1411
Intl **Portugal, Lisbon**
Telectra S.A.R.L., TEL: 19/68 60 72
Intl **Spain, Madrid**
Hispano Elctrna. S.A., TEL: 01-619-4108
Intl **Sweden, Taeby**
Bexab Electronik AB, TEL: 08-768 0560
Intl **Switzerland, Baar**
Bourns (Schweiz) AG, TEL: 042/33 33 33
Intl **Turkey, Ankara**
Nel, Nukleer Elektronik Ltd., TEL: 041-30 15 10
Intl **United Kingdom, Middlesex**
Bourns Electronics, Ltd., TEL: 01/572 6531
Intl **Yugoslavia, Zagreb**
Jugomineral, TEL: 041-44 1885

Distributors

AL **Huntsville**
Hall-Mark Elctrns., 205-837-8700
CA **Chatsworth**
Anthem Elctrns., 213-700-1000
CA **Gardena**
Bell Inds., 213-515-1800
CA **Los Alamitos**
SEMI-DICE, Inc., 213-594-4631
CA **Roseville**
Bell Inds., 916-969-3100
CA **San Diego**
Anthem Elctrns., 619-279-5200
CA **San Diego**
L & S Associates, 619-455-0055
CA **San Jose**
Anthem Elctrns., 408-946-8000
CA **Sunnyvale**
Bell Inds., 408-734-8570
CA **Sunnyvale**
Hall-Mark Elctrns., 408-773-9990
CA **Tustin**
Anthem Elctrns., 714-730-8000
CO **Denver**
Hall-Mark Elctrns., 303-694-1662
CO **Wheatridge**
Bell Inds., 303-424-1985
CT **Norwalk**
Pioneer/Harvey Elctrns., 203-853-1515
FL **Boca Raton**
Lawrence Associates, Inc., 305-368-7373
FL **Clearwater**
Lawrence Associates, Inc., 813-584-8110
FL **Fort Lauderdale**
Hall-Mark Elctrns., 305-971-9280
FL **Orlando**
Hall-Mark Elctrns., 305-855-4020
IL **Bensenville**
Hall-Mark Elctrns., 312-860-3800
IL **Elk Grove Village**
Pioneer/Harvey Electronics, 312-437-9680
IN **Indianapolis**
Pioneer/Harvey Electronics, 317-849-7300
KS **Lenexa**
Hall-Mark Elctrns., 913-888-4747
MD **Baltimore**
Hall-Mark Elctrns., 301-796-9300
MA **Lexington**
Pioneer/Harvey Elctrns., 617-861-9200
MA **Norwood**
Gerber Elctrns., 617-769-6000
MI **Livonia**
Pioneer Elctrns., 313-525-1800
MN **Bloomington**
Hall-Mark Elctrns., 612-854-4169
MO **Maryland Heights**
Hall-Mark Elctrns., 314-291-5350
NJ **Pine Brook**
Pioneer/Harvey Elctrns., 201-575-3510
NM **Albuquerque**
BFA Corporation, 505-292-1212
NM **Albuquerque**
Bell Inds., 505-292-2700
NY **Binghamton**
Pioneer/Harvey Elctrns., 607-748-8211
NY **Fairport**
Pioneer/Harvey Elctrns., 716-381-7070
NY **Woodbury**
Pioneer/Harvey Elctrns., 516-921-8700
NC **Raleigh**
Hall-Mark Elctrns., 919-872-0712
OH **Cleveland**
Pioneer/Harvey Electronics, 216-587-3600
OH **Dayton**
Pioneer/Harvey Electronics, 513-236-9900
OH **Highland Heights**
Hall-Mark Elctrns., 216-473-2907
OK **Tulsa**
Hall-Mark Elctrns., 918-665-3200
PA **Horsham**
Pioneer/Harvey Electronics, 215-674-4000
PA **Pittsburgh**
Pioneer/Harvey Electronics, 412-782-2300
TN **Jonesboro**
EMA, 615-753-5844
TX **Austin**
Hall-Mark Elctrns., 512-258-8848
TX **Dallas**
Hall-Mark Elctrns., 214-341-1147
TX **Houston**
Hall-Mark Elctrns., 713-781-6100
UT **Bountiful**
Anderson Associates, 801-292-8991
UT **Salt Lake City**
Bell Inds., 801-972-6969
WA **Bellevue**
Bell Inds., 206-747-1515
WI **Oak Creek**
Hall-Mark Elctrns., 414-761-3000
Can **Downsview, Ontario**
Future Elctrns. Corp., 416-663-5563
Can **Ottawa, Ontario**
Future Elctrns. Corp., 613-820-8313
Can **Pointe Claire, Quebec**
Future Elctrns., Inc., 514-694-7710
Can **St. Laurent, Quebec**
Zentronics, 514-735-5361
Can **Vancouver, British Columbia**
Intek Elctrns. Ltd., 604-324-6831
Can **Winnepeg, Manitoba**
Hi-Tech Sales Limited, 204-668-5227
Intl **Australia, Hurstville**
RIFA Pty. Ltd., TEL: 02-570-8122
Intl **Australia, South Brisbane**
RIFA Pty. Ltd., TEL: 07-44-6673
Intl **Denmark, Bagsvaerd-Copenhagen**
E. Friss-Mikkelsen A/S, TEL: 02-98 63 33
Intl **Norway, Lillestrom**
A/S Kjell Bakke, TEL: 02-83 02 20
Intl **South Africa, Johannesburg**
Associated Electronics (Pty) Ltd., TEL: 011 839 18 24

Pro-Log

Pro-Log Corporation
2411 Garden Road
Monterey, California 93940
408-372-4593
TWX: 910-360-7082

Distributors

Intl **Austria, Obachgasse**
Walter Rekirsch Elecktronische, TEL: (0222) 23 55 55-0
Intl **B.V., Netherlands**
Intelligent Systems, TEL: 076 224182
Intl **Chile, Santiago**
Interlog Electronics Ltd., TEL: 2253689
Intl **Denmark, Copenhagen**
E. V. Johanssen Elektronik A-S, TEL: 45 183 90 22
Intl **France**
YREL, TEL: 956-81-42
Intl **Germany, Munchen**
Spezial-Elctrn. KG, TEL: 089/530387
Intl **India, Bombay**
American Components, Inc., TEL: 222-999
Intl **Israel, Givatayim**
Elm Int'l Electronics, TEL: (03) 774-041
Intl **Italy, Rome**
Technitron, Srl, TEL: 6-8395841-2, 837035-6
Intl **Japan, Tokyo**
Syscon Corporation, TEL: (03) 863-7688
Intl **Korea, Seoul**
M-C Intl. Korea, Ltd., TEL: 745-7432
Intl **New Zealand, Auckland**
GTS Engineering Ltd., TEL: 546-745
Intl **Norway, Oslo**
Elektronix AS, TEL: 02-229850
Intl **Norway, Oslo**
Elektronix AS, TEL: 02-229850
Intl **Singapore**
Intl. Control Sys., TEL: 2788288
Intl **South Africa**
Transvaal Inst. Pty. Ltd., TEL: (011) 673-6754
Intl **South America, Mexico**
Electronica Steren, TEL: 518-6700
Intl **Spain, Madrid**
Unitronics, S.A., TEL: 242-52-04
Intl **Sweden, Tyresco**
Logtek Electronik AB, TEL: 770-07-25
Intl **Switzerland, Zurich**
Max Meier Elektronik AG, TEL: 01/491 2121
Intl **Taiwan, Taipei**
Multitech Intl. Corp., TEL: (02) 713-4022
Intl **Thailand, Bangkok**
Kriangpat Co. Ltd., TEL: 251-6777
Intl **United Kingdom, Camberley**
Technitron, Inc., U.K., TEL: Camberley (276) 26517

Quay

Quay Corporation
P.O. Box 783
Eatontown, New Jersey 07724
201-542-7340
Specific product information:
Consult Factory for nearest Distributor/Representative

Raytheon Semiconductor

Raytheon Company
Semiconductor Division
350 Ellis Street
Mountain View, California 94043
415-968-9211
TWX: 910-379-6481
Specific product information:
Linear .... J. Shupenis
Digital .... G. Jones
Discrete .... G. Jones
LSI/Memory .... D. McCoy
Price and delivery:
Local Field Sales Office
Place an order:
Local Field Sales Office
Follow-up an order:
Customer Service

Sales Office & Representatives

AL	**Huntsville**	Macro Mktg. Assocs., 205-883-9630
AZ	**Scottsdale**	Semper Fi Sales Co., 602-991-4601
CA	**Irvine**	Raytheon Regional Sales Office, 714-833-9042
CA	**Irvine**	Raytheon Regional Sales Office, 714-833-9042
CA	**La Mirada**	Select Electronics, Ltd., 714-739-8891
CA	**Mtn. View**	Raytheon Regional Sales Office, 415-966-7636
CA	**Mtn. View**	Raytheon Regional Sales Office, 415-966-7636
CA	**San Diego**	Earle Associates, Inc., 619-278-5441
CA	**Sunnyvale**	W.W. Posey, 408-746-0771
CO	**Littleton**	Simpson Assoc., 303-794-8381
CO	**Littleton**	Simpson Assocs., Inc., 303-794-8381
FL	**Clearwater**	Hutto, Hawkins, Peregoy, Inc., 813-797-4447
FL	**Ft. Lauderdale**	Hutto, Hawkins, Peregoy, Inc., 305-971-5750
FL	**Longwood**	Raytheon Regional Sales Office, 305-862-3955
FL	**Maitland**	Hutto, Hawkins, Peregoy, Inc., 305-831-2474
GA	**Woodstock**	Macro Marketing, 404-928-1145
IL	**Des Plaines**	Raytheon Regional Sales Office, 312-297-5540
IL	**Des Plaines**	Raytheon Regional Sales Office, 312-297-5540
IL	**Elk Grove Village**	Carlson Elctrn. Sales Co., 312-956-8240
IN	**Indianapolis**	J & W Sales, 317-842-3740
IN	**Indianapolis**	J & W Sales, 317-842-3740
IA	**Cedar Rapids**	Carlson Elctrn. Sales, 319-377-6341
KS	**Wichita**	DLE Electronics, 316-744-2126
MD	**Ellicott**	Arbotec Assoc. Inc., 301-461-1323
MD	**Towson**	Arbotec Assoc. Inc., 301-825-0775
MA	**Lexington**	Raytheon Regional Sales Office, 617-861-1830
MA	**Waltham**	Dynasel Assoc., 617-890-6777
MA	**Waltham**	Dynasel Assoc., 617-890-6777
MI	**Livonia**	Lowell-Wendt Mktg. Co., 313-464-2722
MN	**Eden Prairie**	Aldridge Assoc. Inc., 612-944-8433
MN	**Minneapolis**	Raytheon Regional Sales Office, 612-920-7935
MO	**St. Louis**	John G. Macke Co., 314-432-2830
NY	**Buffalo**	Pi'Tronics, Inc., 716-876-0549
NY	**Commack**	ERA, Inc., 516-543-0510
NY	**Hauppauge**	Raytheon Regional Sales Office, 516-582-3646
NY	**Hauppauge**	Raytheon Regional Sales Office, 516-582-3646
NY	**Syracuse**	Pi'Tronics, Inc., 315-455-7346
NC	**Garner**	J & B Sales, 919-772-3546
OH	**Beachwood**	Thompson & Assocs., Inc., 216-831-6277
OH	**Dayton**	Thompson & Assocs., Inc., 515-435-7733
PA	**Erdenheim**	OMNI Sales, 215-233-4600
PA	**Wayne**	Raytheon Regional Sales Office, 215-687-8300
TN	**Rutledge**	Macro Marketing Assoc., 615-828-4243
TX	**Austin**	Logic I, 512-459-1297
TX	**Houston**	Logic I, 713-879-1566
TX	**Richardson**	Logic 1, 214-234-0765
TX	**Richardson**	Logic I, 214-234-0765
UT	**Midvale**	Simpson Assoc., 801-566-3691
WA	**Bellevue**	Raytheon Regional Sales Office, 206-883-4037
WI	**Milwaukee**	Carlson Elctrns. Sales, 414-476-2790
Can	**Brampton, Ontario**	Cantec Reps. Inc., 416-791-5922
Can	**Dollard des Ormeaux**	Cantec Reps. Inc., 514-683-6131
Can	**Ottawa, Ontario**	Cantec Reps. Inc., 613-725-3704
Intl	**France, Le Plessis Robinson**	Raytheon Semiconductor France, TEL: 631 06 76
Intl	**Germany, Munchen**	Raytheon HALBLEITER GmbH, TEL: 089/ 539693
Intl	**Japan, Tokyo**	New Japan Radio Co., Ltd., TEL: 03-591-3451
Intl	**United Kingdom, Essex**	Raytheon Semiconductor, TEL: (0268) 288562

Distributors

AZ	**Phoenix**	Arizona Comps. Co., 602-279-9446
AZ	**Phoenix**	Kierulff Elctrns., 602-243-4104
AZ	**Phoenix**	Wyle Distribution Grp., 602-249-2232
AZ	**Scottsdale**	Western Microtechnology, 602-948-4240
CA	**Anaheim**	Zeus Comps., Inc., 213-924-0454, 714-632-6880
CA	**Chatsworth**	Arrow Electronics, 213-701-7500
CA	**Chatsworth**	Integrated Electronics, 213-998-2200
CA	**Cupertino**	Western Microtechnology, 408-725-1660
CA	**El Segundo**	Wyle Distribution Grp., 213-322-8100
CA	**Irvine**	Wyle Distribution Group, 714-851-9958
CA	**Irvine**	Wyle Distribution Grp., 714-641-1600
CA	**Los Angeles**	Kierulff Elctrns., 213-725-0325
CA	**Newport Beach**	Arrow Electronics, 714-851-8961
CA	**San Diego**	Arrow Elctrns., 619-565-4800
CA	**San Diego**	Kierulff Elctrns., 619-278-2122
CA	**San Diego**	Wyle Distribution Grp., 619-565-9171
CA	**Santa Clara**	Wyle Distribution Grp., 408-727-2500
CA	**Sunnyvale**	Arrow Elctrns., 408-745-6600
CA	**Sunnyvale**	Bell Inds., 408-734-8570
CA	**Tustin**	Kierulff Elctrns., 714-731-5711
CO	**Denver**	Arrow Elctrns., 303-758-2100
CO	**Thornton**	Wyle Distribution Grp., 303-457-9953
CO	**Wheatridge**	Bell Inds., 303-424-1985
CT	**Wallingford**	Arrow Elctrns., 203-265-7741
CT	**Wallingford**	Kierulff Electronics, 203-265-1115
FL	**Fort Lauderdale**	Arrow Elctrns., 305-776-7790
FL	**Ft. Lauderdale**	Kierulff Electronics, 305-486-4004
FL	**Orlando**	Hammond Electronics, 305-849-6060
FL	**Palm Bay**	Arrow Elctrns., 305-725-1480
FL	**St. Petersburg**	Kierulff Elctrns., 813-576-1966
GA	**Norcross**	Arrow Elctrns., 404-449-8252
GA	**Norcross**	Kierulff Electronics
IL	**Elk Grove Village**	Kierulff Electronics, 312-640-0200
IL	**Elmhurst**	Semiconductor Specialists, Inc., 312-279-1000
IL	**Northbrook**	Rayal Elctrns., 312-498-0935
IL	**Rosemont**	Advent Elctrns., 312-298-4210
IL	**Schaumburg**	Arrow Electronics, 312-397-3440
IN	**Indianapolis**	Arrow Elctrns., 317-243-9353
IA	**Cedar Rapids**	Advent Elctrns., 319-363-0221
MD	**Baltimore**	Arrow Elctrns., 301-247-5200
MD	**Timonium**	Zebra Elctrns., 301-252-6576, 800-638-1103
MA	**Billerica**	Kierulff Elctrns., 617-667-8331
MA	**Lexington**	Zeus Components, 617-863-8800
MA	**Newton**	The Greene-Shaw Co., Inc., 617-969-8900, 800-225-8804

Raytheon Semiconductor (Cont)

MA **Waltham**
Sterling/Watertown, 617-894-6200
MA **Woburn**
Arrow Elctrns., 617-933-8130
MI **Ann Arbor**
Arrow Elctrns., 313-971-8220
MI **Livonia**
Reptron/Mich., 313-525-2700
MN **Edina**
Arrow Elctrns., 612-830-1800
MN **Edina**
Kierulff Elctrns., 612-941-7500
MO **Maryland Heights**
Kierulff Electronics, 314-739-0855
MO **St. Louis**
Arrow Electronics, 314-567-6888
NH **Manchester**
Arrow Electronics, 602-668-6968
NJ **Camden**
Genl. Radio Supply Co., Inc., 609-964-8560
NJ **Fairfield**
Arrow Elctrns., 201-575-5300
NJ **Moorestown**
Arrow Elctrns., 609-235-1900
NJ **Nutley**
Vantage, 201-667-1840
NM **Albuquerque**
Alliance Electronics, 505-292-3360
NM **Albuquerque**
Arrow Elctrns., Inc./Elctrns. Distribution Div., 505-243-4566
NY **Buffalo**
Summit Distrs., Inc., 716-884-3450
NY **E. Syracuse**
Add Electronics Group, 315-437-0300
NY **Farmingdale**
SAI, 516-293-2710
NY **Fishkill**
Intercept Electronics Corp., 914-896-7535
NY **Hauppauge**
Arrow Electronics, 516-231-1000
NY **Hauppauge**
Harvey/Military, 516-231-9200
NY **Liverpool**
Arrow Elctrns., 315-652-1000
NY **Melville**
Arrow Elctrns., 516-391-1626
NY **Plainview**
ACI Elctrns. Corp., 516-293-6630
NY **Port Chester**
Zeus Comps., Inc., 914-937-7400
NY **Rochester**
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RCA

RCA Solid State Division
Box 3200
Somerville, New Jersey 08876
201-685-6000
TWX: 710-480-9333

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ABBREVIATIONS OF COMPANY NAMES

Action Ins	Action Instruments
AD	Analog Devices
ADT	Advanced Digital Technology
Advent	Advent Products, Inc.
Alphatron	Alphatron
AMA	American Automation
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
Amperex	Amperex Electronic Corp.
Analogic	Analogic
Analog Sys	Analog Systems
APC	Applied Micro Circuits
Apex	Apex Microtechnology
APM	Applied Microsystems Corp.
Appl Sys	Applied Systems Corp.
APT	Applied Microtechnology
Aptek	Aptek Microsystems
Array Tech	Array Technology
AWI	AWI Electronics
Barvon	Barvon Research
Bedford	Bedford Computer Systems Inc.
Burr-Brown	Burr-Brown
CAE	Computer Aided Engineering
Cal Devices	California Devices
Cermetek	Cermetek
CGRS	CGRS Microtech Inc.
Cherry	Cherry Semiconductor
CIC	Custom Integrated Circuits
CirTech	Circuit Technology
Citel	Citel
Comlinear	Comlinear Corporation
CMA	Custom MOS Arrays
Comark	Comark Corp.
Comdial	Comdial Semiconductor
Comp Auto	Computer Automation
Compas	Compas Microsystems
Cont Logic	Control Logic Inc.
Control Sys	Control Systems Microsystems Div.
CreMicro	Creative Micro Systems
Cromemco	Cromemco, Inc.
Cubit	Cubit Inc.
Curtis	Curtis Electro Devices, Inc.
Cybernetic	Cybernetic Micro Systems
Cybersys	Cybersystems
Cybertek	Cybertek Inc.
Data General	Data General
Data I/O	Data I/O
Data Trans	Data Translation
Datel	Datel
Datricon	Datricon Corporation
DDC	Data Devices Corporation
DEC	Digital Equipment Corporation
Die-Tech	Die-Tech
Digelec	Digelec Corp.
Digitek	Digitek, Inc.
Dionics	Dionics Inc.
Dist Comp	Distributed Computer Systems
Divers Tech	Diversified Technology
E-HI	E-H International, Inc.
EDI	Electronic Designs Inc.
Elind	Elind Elettronica Industriale
EMM-SESCO	EEM-SESCO
Emulogic	Emulogic Inc.
ETI Micro	ETI Micro
Exar	Exar Integrated Systems
Exel	Exel Microelectronics
Fairchild	Fairchild
Ferranti	Ferranti Electric
Force	Force Computers
Fujitsu A	Fujitsu America
Fujitsu	Fujitsu Microelectronics, Inc.

GI	General Instrument
GTE Micro	GTE Microcircuits
Harris	Harris Semiconductor
Heurikon	Heurikon Corp.
Hilevel	Hilevel Technology, Inc.
Hitachi	Hitachi America, Ltd.
Holt	Holt Inc.
HP	Hewlett-Packard
Hughes	Hughes Aircraft, Solid State Products
Hybrid Sys	Hybrid Systems
HyComp	HyComp
ICC	International Cybernetics
IDT	Integrated Device Technology
IMI	International Microcircuits, Inc.
IMP	International Microelectronic Products
IMS	Industrial MicroSystems Inc.
Infosphere	Infosphere
Inmos	Inmos
IntCirEng	Integrated Circuit Engineering
IntCirSys	Integrated Circuit Systems
IntCompSys	Integrated Computer Systems
Int Tech	Integrated Technology Corp.
Intech	Intech Microcircuits Div.
Intel	Intel
Interdesign	Interdesign
Intersil	Intersil
Intronics	Intronics
ITT	ITT Semiconductors
Kinetic Sys	Kinetic Systems
Kontron	Kontron Electronics
Lambda	Lambda Semiconductor
Linear Tech	Linear Technology
LSI Comp	LSI Computer Systems
LSI Logic	LSI Logic Corporation
Master Logic	Master Logic Corporation
Matrix	Matrix Corp.
Matrox	Matrox Electronic Systems
Maxim	Maxim Integrated Products
MCC	Micro-Computer Control
MCE	MCE Electronics
Micrel	Micrel
Micro Innov	Micro Innovators
Micropac	Micropac Industries
Micro Net	Micro Networks
Micro Pwr	Micro Power Systems
Micro Sci	Micro Sciences Corp.
Micro Tech	Microcircuits Technology
Micro-Link	Micro-Link Corporation
Micron	Micron Technology
MilerTron	MilerTronics
Miller	Miller Technology
Mitel	Mitel Semiconductor
Mitsubishi	Mitsubishi Electronics
MMI	Monolithic Memories, Inc.
Mostek	Monolithic Systems Corp.
Motorola	Mostek
MRC	Motorola Semiconductor
Murray	MRC Systems
Monosil	Murray Consulting
National	National Semiconductor
NCM	NCM Corp.
NCR	NCR Corp., Microelectronics Division
NEC	NEC Electronics
Nitron	Nitron

OAE	Oliver Advanced Engineering
Octagon	Octagon Systems Corp.
OEI	Optical Electronics Inc.
Ohio Sci	Ohio Scientic
OKI	OKI Semiconductor
Omnibyte	Omnibyte Corp.
Onset	Onset Computer Corp.
Panasonic	Panasonic
Pico Design	Pico Design
Polycore	Polycore Electronics
Plessey	Plessey Semiconductors
PMI	Precision Monilithics, Inc.
PragDes	Pragmatic Design Inc.
Pro-Log	Pro-Log Corp.
Quay	Quay Corp.
Raytheon	Raytheon Semiconductor
RCA	RCA Solid State Division
RCI Data	RCI Data
RELMS	Relational Memory Systems
Reticon	Reticon
RIFA	RIFA
Rockwell	Rockwell, Microelectronic Devices
RTC	Riehl Time Corporation
Sanyo	Sanyo
SBE	SBE, Inc.
SEEQ	SEEQ Technology, Inc.
SPI	Semi Processes Inc.
Siemens	Siemens
Si-Fab	Si-Fab
Signetics	Signetics
SGS	SGS Semiconductor
Sharp	Sharp
Silicon G	Silicon General
Siliconix	Siliconix
Silicon Sys	Silicon Systems Inc.
Siltronics	Siltronics
SMC	Standard Microsystems Corp.
S MOS	S MOS Systems
Solarise	Solarise Enterprises
Solitron	Solitron Devices
Sprague	Sprague Electric Company
SSM	Solid State Micro Technology for Music
SSS	Solid State Scientific
Stag	Stag Microsystems
STC	Storage Technology Corp.
STD	STD Microsystems
Struc Des	Structured Design Inc.
Stynetic	Stynetic Systems
Sunrise	Sunrise Electronics
Sunshine	Sunshine Semiconductor
Supertex	Supertex Inc.
Symtek	Symtek Corp.
Synertek	Synertek
Sys Innov	Systems Innovations
Tau Zero	Tau Zero Inc.
Technitrol	Technitrol
Tektronix	Tektronix
Teledyne C	Teledyne Crystalonics
Teledyne P	Teledyne Philbrick
Teledyne S	Teledyne Semiconductor
Telefunken	Telefunken
Telmos	Telmos
Teltone	Teltone Corporation
TI	Texas Instruments
Third Domain	Third Domain
Thomson-CSF	Thomson-CSF Components Corp.
Toshiba	Toshiba America
Trans-Data	Trans-Data
TRW	TRW LSI Products
Unitrode	Unitrode
Universal	Universal Semiconductor, Inc.
Varix	Varix Corp.
VLSI Design	VLSI Design Associates
VTI	VLSI Technology, Inc.
Votrax	Votrax
Weitek	Weitek Corporation
Western	Western Digital
Wintek	Wintek Corp.
Xicor	Xicor, Inc.
Xycom	Xycom
Zendex	Zendex Corp.
Zilog	Zilog
ZyMOS	ZyMOS Corporation
Zytrex	Zytrex Corp.

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NJ	**Perth Amboy** Sterling Electronics, 201-442-8000
NM	**Albuquerque** Bell Inds., 505-292-2700
NY	**East Syracuse** ADD Elctrns. Corp., 315-437-0300
NY	**Endwell** Marshall Industries, 607-754-1570
NY	**Rochester** Marshall Industries, 716-235-7620
OH	**Columbus** Reptron Electronics Inc., 614-436-6675
OH	**Dayton** Bell Inds., 513-434-8231
OH	**Dayton** Marshall Industries, 513-236-8088
OR	**Lake Oswego** Bell Inds., 503-241-4115
TX	**Austin** ACT Austin, 512-452-5254
TX	**Austin** Marshall Industries, 512-458-5654
TX	**Dallas** Active Comp. Technology, 214-980-1888
TX	**Houston** Active Comp. Technology, 713-496-4000
TX	**Houston** Marshall Industries, 713-789-6600
UT	**Salt Lake City** ACT Utah, 801-487-8131
UT	**Salt Lake City** Bell Inds., 801-972-6969
WA	**Bellevue** Bell Inds., 206-747-1515
WA	**Bellevue** Marshall Industries, 206-747-9100
WI	**Waukesha** Bell Inds., 414-784-0235
Intl	**Austria, Vienna** Othmar Lackner, TEL: 0222 531185
Intl	**Belgium, Brussels** Auriema N.V., TEL: (02) 52362 95
Intl	**England, Buckinghamshire** Hunter Elctrn. Comp. Ltd., TEL: 6286 65421
Intl	**France, Antony Cedex** Almex SA, TEL: (1) 666 21 12
Intl	**Israel, Ramat-Gan** M.R.B.D. Ltd., TEL: 03-736479, 732624
Intl	**Italy, Milano** Adrep SA, TEL: 02 404 4046/7/8
Intl	**Japan, Tokyo** Hirel Co., Ltd., TEL: 03-260-8401
Intl	**Netherlands, Haaften** Techmation Elctrns. B.V., TEL: 4189 2222
Intl	**Scotland, Lanarkshire** Phoenix Elctrns. Ltd., TEL: (0555) 892393
Intl	**Sweden, Vallingby** teleimport ab, TEL: (08) 89 02 65
Intl	**Switzerland, Zurich** ENA AG., TEL: 64 5757
Intl	**West Germany, Hamburg** Microscan GmbH, TEL: 406 30 5067
Intl	**West Germany, Martinsried (Munich)** Atlantik Elektronik GmbH, TEL: (089) 857 2086
Intl	**West Germany, Viersen (Dusseldorf)** Mostron GmbH, TEL: 02162 17024

SGS Semiconductor

SGS Semiconductor Corporation
1000 E. Bell Road
Phoenix, Arizona 85022
602-867-6100
TELEX: 249976

Specific product information:
Product Marketing .... Giovanni Seghezzo

Application engineering:
Applications .... Tom Hopkins

Literature:
Sales Department .... Carole Walker

Place an order:
Product Marketing .... Local Sales Office

Follow-up an order:
Customer Service .... Local Sales Office

Sales Office & Representatives

Intl	**Argentina, Buenos Aires** Neutrec S.R.L., TEL: (011-54-1) 30-7774
Intl	**Belgium, Bruxelles** SGS-ATES Componenti Elettronici SpA, TEL: 02-3432439
Intl	**Colombia, Bagota** Framex LTDA, TEL: (011-572) 212-9045
Intl	**Denmark, Herlev** SGS-ATES Scandinavia AB, TEL: 02-948533
Intl	**France, Paris** SGS-ATES France S.A., TEL: 5842730
Intl	**Germany, Haidling** SGS-ATES Deutschland Holbeiter Bouelemente GmbH, TEL: 08092-691
Intl	**Hung Won, Kowloon** SGS-ATES Singapore (Pte) Ltd., TEL: 3-644251/5
Intl	**Italy, Agrate Brianza** Export Sales Office, TEL: 039-6555287
Intl	**Italy, Agrate Brianza** Intl. Hdqtrs., TEL: 039-65551
Intl	**Italy, Milano** SGS-ATES Componenti Elettronici SpA, TEL: 02-4695651
Intl	**Italy, Roma** Sales Office, TEL: 06-8392848
Intl	**Mexico., Mexico D.F.** Mexel S.A., TEL: (011-525) 563-5411
Intl	**Singapore, Singapore** SGS-ATES Singapore (Pte) Ltd., TEL: 2531411
Intl	**Sweden, Marsta** SGS-ATES Scandinavia AB, TEL: 0760-40120
Intl	**United Kingdom, Aylesbury-Bucks** SGS-ATES (United Kingdom) Ltd., TEL: 0296-5977
Intl	**Uruguay, Montevideo** Ricagni Imporactiones LTDA, TEL: (901) 594888
Intl	**Venezuela, Caracas** Magnetica, TEL: (011-582) 239-3931

SGS Semiconductor (Cont)

Sharp Electronics

Sharp Electronics Corporation
10 Sharp Plaza
Paramus, New Jersey 07652
201-265-5600
TELEX: 134-327

Siemens

Siemens Corporation
186 Wood Avenue South
Iselin, New Jersey 08830
201-494-1000
TELEX: 84-4491

Specific product information:
Al Liebich

Application engineering:
Al Liebich

Literature:
Lon Cantor

Price and delivery:
Ron Giampietro

Follow-up an order:
Ron Giampietro

All other information:
Al Liebich

Si-Fab Corporation

Si-Fab Corporation
27 Janis Way
Scotts Valley, California 95066
408-438-6800

Signetics

Signetics Corporation
811 East Arques Ave., P.O. Box 409
Sunnyvale, California 94086
408-739-7700 ext. 5724
TWX: 910-339-9283

Specific product information:

Analog	408-746-5724, 5725
Bipolar LSI	408-746-1816
Bipolar Memory	408-746-3564
MOS Memory	408-746-1756
CMOS Gate Arrays	408-746-2194
Logic	408-746-1617
Microprocessor	408-746-2254
Microsystems	408-746-2137
Military	916-924-6047
Philips/Euro-Products	408-746-1338

Application engineering:

Analog	408-746-5724, 5725
Bipolar LSI	408-746-1816
Bipolar Memory	408-746-3564
MOS Memory	408-746-1756
CMOS Gate Arrays	408-746-2194
Logic	408-746-1617
Microprocessor	408-746-2254
Microsystems	408-746-2137
Military	916-924-6047
Philips/Euro-Products	408-746-1338

Literature:

Publication Services	408-746-2111

Sales Office & Representatives

AL **Huntsville**
Elctrn. Sales, Inc., 205-533-1735
AZ **Phoenix**
Signetics Sales Office, 602-265-4444
AZ **Scottsdale**
Thom Luke Sales, Inc., 602-941-1901
CA **Canoga Park**
Signetics Sales Office, 213-340-1431
CA **Cupertino**
Signetics Sales Office, 408-725-8100
CA **Inglewood**
Signetics Sales Office, 213-670-1101
CA **Irvine**
Signetics Sales Office, 714-833-8980, 213-588-3281
CA **Los Gatos**
Sierra Technology, 408-354-1626
CA **San Diego**
Mesa Engrg., 619-278-8021
CA **San Diego**
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Signetics Sales Office, 303-751-5011
CT **Danbury**
Signetics Sales Office, 203-748-3722
CT **Yalesville**
Kanan Assoc., 203-265-2404
FL **Clearwater**
Signetics Sales Office, 813-796-7086
FL **Ft. Lauderdale**
Signetics Sales Office, 305-486-6300
GA **Atlanta**
Signetics Sales Office, 404-953-0067
IL **Elk Grove Village**
Micro-Tex, Inc., 312-640-9633
IL **Schaumburg**
Signetics Sales Office, 312-843-7805
IN **Kokomo**
Signetics Sales Office, 317-453-6462
IA **Marion**
Rep. Associates Corp., 319-373-0152
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B.C. Elctrn. Sales, 913-342-1211
KS **Overland Park**
Signetics Sales Office, 913-341-8181
KS **Wichita**
B.C. Elctrn. Sales, 316-942-9840
MD **Glen Burnie**
Signetics Sales Office, 301-787-0220
MA **Reading**
Kanan Assocs., 617-944-8484
MA **Woburn**
Signetics Sales Office, 617-938-1000
MI **Bloomfield Hills**
Enco Mktg., 313-642-0203
MI **Farmington Hills**
Signetics Sales Office, 313-476-1610
MN **Edina**
Signetics Sales Office, 612-835-7455
MN **Minneapolis**
High Technology Sales, 612-888-8088
MO **Bridgeton**
B.C. Electronic Sales, 314-291-1101
MO **St. Louis**
B.C. Elctrn. Sales, 314-731-1255
NJ **East Hanover**
Emtec Sales, Inc., 201-428-0600
NJ **Parsippany**
Signetics Sales Office, 201-334-4405
NM **Albuquerque**
Power Enterprises, 505-298-1918
NM **Albuquerque**
Power Entprs., 505-298-1918
NY **Ithaca**
Bob Dean, Inc., 607-257-1111
NY **Liverpool**
Signetics Sales Office, 315-451-5470
NY **Melville**
Emtec Sales, Inc., 516-752-1630
NY **Melville**
Signetics Sales Office, 516-752-0130
NY **Wappingers Falls**
Signetics Sales Office, 914-297-4074
NC **Raleigh**
Signetics Sales Office, 919-851-2013
OH **Worthington**
Signetics Sales Office, 614-888-7143
OR **Hillsboro**
Western Tech. Sales, 503-640-4621
OR **Hillsboro**
Western Technical Sales, 503-640-4621
PA **Horsham**
Signetics Sales Office, 215-443-5500
PA **Pittsburgh**
Cover & Newman, 412-531-2002
TN **Greeneville**
Signetics Sales Office, 615-639-0251
TX **Austin**
Signetics Sales Office, 512-458-2591
TX **Richardson**
Signetics Sales Office, 214-644-3500
UT **Salt Lake City**
Electrodine, 801-486-3801
WA **Bellevue**
Western Technical Sales, 206-641-3900
WA **Spokane**
Western Tech. Sales, 509-922-7600
WI **Waukesha**
Micro-Tex, Inc., 414-542-5352
Can **Etobicoke, Ontario**
Signetics Canada, Ltd., 416-622-9314
Can **Etobicoke, Ontario**
Tech-Trek, Ltd., 416-626-6676
Can **Ottawa, Ontario**
Tech-Trek, Ltd., 613-230-3297
Can **Pointe Claire**
Tech-Trek, Ltd., 514-698-3385
Intl **Argentina, Buenos Aires**
Philips Argentina S.A., TEL: 541-7141

Signetics (Cont)

Intl	**Austria, Wien** Osterrichische Philips Bauelemente, TEL: 43-222-93-26-2
Intl	**Belgium, Bruxelles** N.V. Philips & MBLE, TEL: 32-02-242-7400
Intl	**India, Bombay** Philips Inida & Elect. Ltd., TEL: 91-22-295144
Intl	**Ireland, Dublin** Philips Electrical Ltd., TEL: 353-1-69-3555
Intl	**Japan, Osaka** Philips Elect. Korea Ltd., TEL: 816-304-6171
Intl	**Malaysia, Huala Lumpur** Philips Malaysia Snd. Berhad, TEL: 77 44 11
Intl	**Turkey, Istanbul** Turk Philips Ticaret A.S., TEL: 43 59 10

Distributors

AL	**Huntsville** Hamilton/Avnet Elctrns., 205-837-7210
AL	**Huntsville** Pioneer Elctrns., 205-837-9300
AZ	**Phoenix** Hamilton/Avnet Elctrns., 602-231-5100
AZ	**Phoenix** Wyle Distribution Grp., 602-249-2232
CA	**Chatsworth** Anthem Electronics, 213-700-1000
CA	**Chatsworth** Arrow Electronics, 213-701-7500
CA	**Costa Mesa** Avnet Elctrns., 714-754-6111
CA	**Costa Mesa** Hamilton Electro Sales, 714-641-4100
CA	**Culver City** Hamilton Avnet Elctrns. Military, 213-558-2901
CA	**Culver City** Hamilton/Avnet Elctrns., 213-558-2121
CA	**El Segundo** Wyle Distribution Grp., 213-322-8100
CA	**Irvine** Schweber Elctrns., 714-556-3880
CA	**Irvine** Wyle Distribution Grp., 714-863-9953
CA	**Newport Beach** Arrow Electronics, 714-851-8961
CA	**Sacramento** Hamilton/Avnet Electronics, 916-920-3150
CA	**San Diego** Anthem Elctrns., 619-453-4871
CA	**San Diego** Arrow Electronics, 619-565-4800
CA	**San Diego** Hamilton/Avnet Elctrns., 619-571-7510
CA	**San Diego** Wyle Distribution Grp., 619-565-9171
CA	**San Jose** Anthem Elctrns. Inc., 408-946-8000
CA	**Santa Clara** Schweber Elctrns., 408-748-4700
CA	**Santa Clara** Wyle Distribution Grp., 408-727-2500
CA	**Sunnyvale** Arrow Elctrns., 408-745-6600
CA	**Sunnyvale** Hamilton/Avnet Elctrns., 408-743-3366
CA	**Tustin** Anthem Electronics, 714-730-8000
CA	**Woodland Hills** Avnet Electronics, 213-883-0000
CO	**Aurora** Arrow Electronics, 303-696-1111
CO	**Denver** Wyle Distribution Grp., 303-457-9953
CO	**Englewood** Hamilton/Avnet Elctrns., 303-740-1000
CT	**Danbury** Hamilton/Avnet Elctrns., 203-797-2800
CT	**Danbury** Schweber Elctrns., 203-792-3500
CT	**Wallingford** Arrow Elctrns., 203-265-7741
FL	**Ft. Lauderdale** Arrow Elctrns., 305-776-7790
FL	**Ft. Lauderdale** Hamilton/Avnet Elctrns., 305-971-2900
FL	**Hollywood** Schweber Elctrns., 305-927-0511
FL	**Hollywood** Schweber Electronics, 305-927-0511
FL	**Palm Bay** Arrow Elctrns., 305-725-1480
FL	**St. Petersburg** Hamilton/Avnet Elctrns., 813-576-3930
GA	**Atlanta** Schweber Elctrns., 404-449-9170
GA	**Norcross** Arrow Elctrns., 404-449-8252
GA	**Norcross** Hamilton/Avnet Elctrns., 404-447-7500
GA	**Norcross** Schweber Electronics, 404-449-9170
IL	**Bensenville** Hamilton/Avnet Elctrns., 312-860-7700
IL	**Chicago** Bell Inds., 312-982-9210
IL	**Elk Grove Village** Schweber Elctrns., 312-364-3750
IL	**Schaumburg** Arrow Elctrns., 312-397-3440
IN	**Indianapolis** Arrow Elctrns., 317-243-9353
IN	**Indianapolis** Hamilton Avnet Elctrns., 317-844-9333
IN	**Indianapolis** Pioneer Elctrns., 317-849-7300
KS	**Overland Park** Hamilton/Avnet Elctrns., 913-888-8900
MD	**Baltimore** Arrow Elctrns., 301-247-5200
MD	**Columbia** Hamilton/Avnet Elctrns., 301-995-3500
MD	**Gaithersburg** Pioneer Washington Elctrns., 301-948-0710
MD	**Gaithersburg** Schweber Elctrns., 301-840-5900
MA	**Bedford** Schweber Elctrns., 617-275-5100
MA	**Burlington** Lionex Corp., 617-272-9400
MA	**Woburn** Arrow Elctrns., 617-933-8130
MA	**Woburn** Hamilton/Avnet Elctrns., 617-273-7500
MI	**Ann Arbor** Arrow Elctrns., 313-971-8220
MI	**Grand Rapids** Hamilton Avnet Elctrns., 616-243-8805
MI	**Livonia** Hamilton/Avnet Elctrns., 313-522-4700
MI	**Livonia** Pioneer Elctrns., 313-525-1800
MI	**Livonia** Schweber Elctrns., 313-525-8100
MN	**Eden Prairie** Schweber Elctrns., 612-941-5280
MN	**Edina** Arrow Elctrns., 612-830-1800
MN	**Minneapolis** Arrow Electronics, 612-830-1800
MN	**Minneapolis** Hamilton/Avnet Electronics, 612-932-0600
MN	**Minnetonka** Hamilton/Avnet Elctrns., 612-932-0666
MO	**Earth City** Hamilton/Avnet Elctrns., 314-344-1200
MO	**St. Louis** Arrow Elctrns., 314-567-6888
NH	**Manchester** Arrow Elctrns., 603-668-6968
NJ	**Cherry Hill** Hamilton/Avnet Elctrns., 609-424-0100
NJ	**Fairfield** Arrow Elctrns., 201-575-5300
NJ	**Fairfield** Hamilton/Avnet Elctrns., 201-575-3390
NJ	**Fairfield** Lionex Corporation, 201-227-7960
NJ	**Fairfield** Schweber Elctrns., 201-227-7880
NJ	**Moorestown** Arrow Elctrns., 609-235-1900
NM	**Albuquerque** Arrow Electronics, 505-243-4566
NM	**Albuquerque** Hamilton/Avnet Elctrns., 505-765-1500
NY	**Buffalo** Summit Distrs., 716-887-2800
NY	**East Syracuse** Arrow Elctrns., 315-652-1000
NY	**East Syracuse** Hamilton/Avnet Elctrns., 315-437-2642
NY	**Hauppauge** Arrow Elctrns., 516-231-1000
NY	**Hauppauge** Lionex Corporation, 516-273-1660
NY	**Liverpool** Arrow Elctrns., 315-652-1000
NY	**Melville** Hamilton/Avnet Elctrns., 516-454-6012
NY	**Rochester** Arrow Elctrns., 716-275-0300
NY	**Rochester** Hamilton/Avnet Elctrns., 716-475-9130
NY	**Rochester** Schweber Elctrns., 716-424-2222
NY	**Westbury** Schweber Elctrns., 516-334-7474
NC	**Charlotte** Pioneer Electronics, 704-527-8188
NC	**Raleigh** Arrow Electronics, 919-876-3132
NC	**Raleigh** Hamilton/Avnet Elctrns., 919-878-0819
NC	**Raleigh** Schweber Electronics, 919-876-0000
NC	**Winston-Salem** Arrow Elctrns., 919-725-8711
OH	**Beechwood** Schweber Elctrns., 216-464-2970
OH	**Centerville** Arrow Elctrns., 513-435-5563
OH	**Cleveland** Hamilton/Avnet Elctrns., 216-831-3500
OH	**Cleveland** Pioneer Standard Elctrns., 216-587-3600
OH	**Dayton** Hamilton/Avnet Elctrns., 513-433-0610
OH	**Dayton** Pioneer Standard Elctrns., 513-236-9900
OH	**Solon** Arrow Elctrns., 216-248-3990
OK	**Tulsa** Quality Comps., 918-664-8812
OR	**Hillsboro** Wyle Distribution Group, 503-640-6000
OR	**Lake Oswego** Hamilton/Avnet Elctrns., 503-635-8831
PA	**Horsham** Schweber Elctrns., 215-441-0600
PA	**Pittsburgh** Arrow Elctrns., 412-856-7000
PA	**Pittsburgh** Pioneer/Pittsburgh, 412-782-2300
TX	**Austin** Arrow Electronics, 512-835-4180
TX	**Austin** Hamilton/Avnet Elctrns., 512-837-8911
TX	**Austin** Quality Comps., 512-835-0220

Signetics (Cont)

TX **Dallas**
Arrow Electronics, 214-386-7500

TX **Dallas**
Hamilton/Avnet Elctrns., 214-659-4111

TX **Dallas**
Quality Comps., 214-387-4949

TX **Dallas**
Schweber Elctrns., 214-661-5010

TX **Houston**
Arrow Electronics, 713-530-4700

TX **Houston**
Hamilton/Avnet Elctrns., 713-780-1771

TX **Houston**
Quality Comps., 713-772-7100

TX **Houston**
Schweber Elctrns., 713-784-3600

UT **Salt Lake City**
Hamilton/Avnet Elctrns., 801-972-4300

UT **Salt Lake City**
Wyle Distribution Group, 801-974-9953

WA **Bellevue**
Arrow Elctrns., 206-643-4800

WA **Bellevue**
Hamilton/Avnet Elctrns., 206-453-5844

WA **Bellevue**
Wyle Distribution Grp., 206-453-8300

WI **New Berlin**
Hamilton/Avnet Elctrns., 414-784-4510

WI **Oak Creek**
Arrow Elctrns., 414-764-6600

WI **Waukesha**
Bell Industries, 414-784-0235

Can **Calgary, Alberta**
Hamilton Avnet Elctrns., 403-230-3586

Can **Calgary, Alberta**
Zentronics, 403-272-1021

Can **Downsview, Ontario**
Cesco Elctrns., 416-661-0220

Can **Mississauga, Ontario**
Hamilton/Avnet Elctrns., 416-677-7432

Can **Mississauga, Ontario**
Zentronics, 416-451-9600

Can **Montreal, Quebec**
Cesco Elctrns., 514-735-5511

Can **Montreal, Quebec**
Zentronics Ltd., 514-735-5361

Can **Ottawa, Ontario**
Cesco Elctrns., 613-226-6903

Can **Ottawa, Ontario**
Hamilton/Avnet Elctrns., 613-226-1700

Can **Ottawa, Ontario**
Zentronics Ltd., 613-238-6411

Can **Quebec City, Quebec**
Cesco Elctrns., 418-524-4641

Can **Vancouver**
Zentromis, 604-688-2533

Can **Ville St. Laurent, Quebec**
Hamilton/Avnet Elctrns., 514-331-6443

Can **Waterloo, Ontario**
Zentronics, 519-884-5700

Can **Winnipeg**
Zentronics, 204-775-8661

Intl **Australia, Lane-Cove N.S.W.**
Philips Inds. Holdings Ltd., TEL: 61-2-427-0888

Intl **Austria, Wien**
Osterreichische Philips Bauelemente, TEL: 43-222-93-26-2

Intl **Brazil, Sao Paulo**
Ibrape, TEL: (55) 011 211-2600

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Sadape S.A., TEL: 600600

Intl **Denmark, Kobenhavn**
Miniwatt A/S, TEL: 45-01-69-1622

Intl **Finland, Helsinki**
Oy Philips Ab, TEL: 358-1-7271

Intl **France, Paris**
R.T.C., TEL: 33-1-355-4499

Intl **Germany, Hamburg**
Valvo, TEL: 49-40-3296-19

Intl **Greece, Athens**
Philips S.A. Hellenique, TEL: 9215111

Intl **Hong Kong, Kwai Chung**
Philips Hong Kong Ltd., TEL: 852-0-245121

Intl **Indonesia, Jakarta**
P.T. Philips-Ralin Elctrns., TEL: 716 131

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Rapac Elctrns., Ltd., TEL: 972-3-477115

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Philips S.p.A., TEL: 39-2-6994

Intl **Japan, Tokyo**
Signetics Japan, Ltd., TEL: 813-230-1521

Intl **Korea, Seoul**
Philips Elect Korea Ltd., TEL: 794-4202

Intl **Mexico, Mexico City**
Elctrna. S.A. de C.V., TEL: 52-721-61300

Intl **Netherlands, Eindhoven**
Philips Nederland B.V., TEL: 31-40-79-3333

Intl **New Zealand, Auckland**
Philips Electrical Ind. Elcoma, TEL: 64-9-605914

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Intl **Peru, Lima**
Cadesa, TEL: 326070

Intl **Philippines, Makati-Rizal**
Philips Indl. Dev., Inc., TEL: 868951

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Philips Portuguesa SARL, TEL: 351-19-68-3121

Intl **Singapore, Singapore**
Philips Project Dev. Pte., Ltd., TEL: 65-253-8811

Intl **South Africa, Johannesburg**
E.D.A.C. (Pty), Ltd., TEL: 27-11-614-2362

Intl **Spain, Barcelona**
Miniwatt S.A., TEL: 301 63 12

Intl **Sweden, Stockholm**
Elcoma A.B., TEL: 46-08-67-9780

Intl **Switzerland, Zurich**
Philips A.G., TEL: 41-01-988-2211

Intl **Taiwan, Taipei**
Philips Taiwan, Ltd., TEL: 886-2-563-1717

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Intl **United Kingdom, London**
Mullard, Ltd., TEL: 44-01-580-6633

Intl **Uruguay, Montevideo**
Luzilectron S.A., TEL: 9143 21

Intl **Venzuela, Caracas**
Industrias Venezolanas Philips S.A., TEL: 58-2-36-0511

Silicon General

Silicon General, Inc.
11651 Monarch Street
Garden Grove, California 92641
714-892-5531
TELEX: 69-2411
TWX: 910-596-1804

Specific product information:
John Power

Application engineering:
John Power

Literature:
Inside Sales

Price and delivery:
Deborah Mabee, Western Area
Joe Castellano, Eastern Area

Follow-up an order:
Deborah Mabee, Western Area
Joe Castellano, Eastern Area

Sales Office & Representatives

Intl **Argentina, Buenos Aires**
YEL srl., TEL: 46-2211

Intl **Australia, Prospect**
A.J. Distrs., TEL: 2691244

Intl **Austria, Wien**
Othmar Lackner Elect., TEL: 531185

Intl **Belgium, Hasselt**
Heynen b.v., TEL: 210006

Intl **Denmark, Copenhagen**
E. V. Johanssen Electronik, TEL: (01) 839022

Intl **England, London**
Power Technology, TEL: 734-866766

Intl **Finland, Espoo**
Panta-Tuote OY, TEL: (90) 598525

Intl **France, Paris**
Radio Equip.-Antares, TEL: 758-11-11

Intl **Germany, Munchen**
Astronic GmbH, TEL: 309031

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Neumuller GmbH, TEL: 61181

Intl **Hong Kong, Kowloon**
Tektron Elect. Ltd., TEL: 856199

Intl **India, Bombay**
Zenith Electronics, TEL: 384214

Intl **Israel, Tel Aviv**
Talviton Elctrns. Ltd., TEL: 44-45-72

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Exhibo Italiana S.P.A., TEL: 360021

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Siliconix

Siliconix Inc.
2201 Laurelwood Road
Santa Clara, California 95054
408-988-8000
TWX: 910-338-0227

Specific product information:
Publications ... ext. 2066

Application engineering:
Analog ... ext. 2420
Interface ... ext. 2422
Digital ... ext. 2022
Mospower FET's ... ext. 2586
Micropower Linear ... ext. 2586
Switches ... ext. 2022

Literature:
Publications ... ext. 2066

Price and delivery:
Sales Department

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Local Sales Office

All other information:
Publications ... ext. 2066
Public Relations ... ext. 2698

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Pipe Thompson, Ltd., 613-258-4067

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NY	**Melville** Hamilton/Avnet, 516-454-6000
NY	**Port Chester** Zeus Components, 914-937-7400
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Can **Nepean, Ontario**
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Can **Ottawa, Ontario**
Future Elctrns., 613-820-8313
Can **St. Laurent, Quebec**
Hamilton/Avnet, 514-331-6443

Silicon Systems

Silicon Systems Inc.
14351 Myford Road
Tustin, California 92680
714-731-7110
TWX: 910-595-2809
Specific product information:
Larry Pepper
Literature:
Larry Pepper
Price and delivery:
Larry Pepper

Siltronics

Siltronics Ltd.
436 Highway 7
Kanata, Ontario K2L 1T9
613-836-5003

Solarise Enterprises

Solarise Enterprises Inc.
10080 North Wolfe Road, Suite SW3-180
Cupertino, California 95014
408-446-9343

Solid State Micro Technology for Music, Inc.

Solid State Micro Technology for Music, Inc.
2076B Walsh Avenue
Santa Clara, California 95050
408-727-0917
TELEX: 171189
Specific product information:
Dan Parks
Application engineering:
Ron Dow
Literature:
Receptionist
Price and delivery:
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Follow-up an order:
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Sales Office & Representatives

Intl **France, Boulogne**
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I.C. Inventor, TEL: 08-756 50 24

Solid State Scientific

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3900 Welsh Road
Willow Grove, Pennsylvania 19090
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TELEX: 476-1101
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Neutron GmbH, TEL: 611 813930

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8808 Balboa Avenue
San Diego, California 92123
714-278-8780

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Sprague Electric

Sprague Electric Company
Semiconductor Division Integrated Circuit Operations
115 Northeast Cutoff
Worcester, Massachusetts 01606
617-853-5000
TWX: 710-340-6304

Sprague Electric (Cont)

Specific product information:
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Sprague Electric

Sprague Electric Company
Semiconductor Division Discrete Components Operation
70 Pembroke Road, P.O. Box 917A
Concord, New Hampshire 03301
603-224-1961
TWX: 710-361-1495
Specific product information:
Hall-Effect I.C.s .... T. Yasewicz
Application engineering:
P. Boehm
Literature:
647 Marshall Street, North Adams, Massachusetts 01247
(413) 664-4411, Ext. 2107
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Metronix GmbH, TEL: 089/6114063

Telefunken

AEG-Telefunken Corporation
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Somerville, New Jersey 08876
201-722-9800
TELEX: 833409

Telephonics LSI

Telephonics LSI
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Huntington, New York 11743
516-549-6300
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Intl **West Germany, Munchen**
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Kirkland, Washington 98033
206-827-9626
TWX: 910-449-2862
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Application engineering:
Jim Carefoot
Literature:
Sales Support Department
Price and delivery:
Order Entry Department
Follow-up on order:
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All other information:
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Texas Instruments, Inc.
Semiconductor Group
P.O. Box 401560
Dallas, TX 75240
214-995-2011
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Canoga Park, California 91303
213-887-1010
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TWX: 910-494-1954

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7435 East Karen Drive
Scottsdale, Arizona 85260
602-998-5988
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Tustin, California 92680
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916-447-6523

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TRW Electronic Components Group
P.O. Box 2472
La Jolla, California 92038
619-457-1000
TELEX: 697-957
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All other information:
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14520 Aviation Blvd.
Lawndale, California 90260
(213) 679-4561

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TELEX: 95-1064
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Hamilton/Avnet, 416-677-7432
Can **Vancouver, British Columbia**
Future Elctrns., Inc., 604-438-5545
Intl **Australia, Crows Nest N.S.W.**
VSI Elctrns. (Australia) Pty. Ltd., TEL: 439-4655
Intl **Austria, Graz**
Dahms Elektronik, TEL: (0316) 64.0.30
Intl **Austria, Vienna**
Dahms Elektronik, TEL: (0222) 57-25-77
Intl **Belgium, Bruxelles**
J.P. Lemaire, TEL: 478 48 47
Intl **Brazil, Sao Paulo**
Cosele Ltda., TEL: 255-1733, 259-3719
Intl **China, Peoples Republic of, Beijing**
Rikei Corp., TEL: 66-8541
Intl **Denmark, Glostrup**
Ditz Schweitzer A/S, TEL: 2-45 30 44
Intl **France, Antony Cedex**
C.C.I., TEL: (01) 666 21-82
Intl **France, Rungis Cedex**
Spetelec, TEL: (1) 686.56.65
Intl **France, Rungis Principal**
UniRep, TEL: (1) 686-39.42
Intl **Germany, Burgwedel**
EBV Elektronik GmbH, TEL: 05139/5038
Intl **Germany, Carl-Zeiss-Strasse 3**
Frehsdorf KG, TEL: 04106-71058
Intl **Germany, Duesseldorf**
EBV Elektronik GmbH, TEL: 0211-84-84-6/7
Intl **Germany, Frankfurt/Main**
EBV Elektronik GmbH, TEL: 0611-785037
Intl **Germany, Heddesheim**
Metronik GmbH, TEL: 06203-4701
Intl **Germany, Nuremberg**
Metronik GmbH, TEL: 0911/46 80 66-67
Intl **Germany, Ottobrunn**
Protec GmbH, TEL: (089) 60-30-06
Intl **Germany, Stuttgart**
EBV Elektronik GmbH, TEL: 711/24 74 81
Intl **Germany, Unterhaching**
EBV Elektronik GmbH, TEL: (089) 611051
Intl **Germany, Unterhaching**
Metronik GmbH, TEL: 089-6114063
Intl **Germany, Unterhaching**
Unitrode Elctrns. GmbH, TEL: 089/6190 04/05/06
Intl **India, Bombay**
Sujata Sales & Exports Ltd., TEL: 234658
Intl **Ireland, Dublin**
Nets, Ltd., TEL: (01) 450-635
Intl **Israel, Tel-Aviv**
S.T.G. Intl., TEL: 03-248231
Intl **Italy, Milano**
Microelit, s.r.l., TEL: (02) 469 04 44
Intl **Italy, Milano**
Unitrode S.R.L., TEL: 431 831, 434 604
Intl **Japan, Tokyo**
Hamilton/Avnet Elctrns., TEL: 03-662-9911
Intl **Japan, Tokyo**
High Technology Intl., Inc., TEL: 03-379-7621
Intl **Japan, Tokyo**
Rikei Corp., TEL: Tokyo (03) 345-1411
Intl **Korea R.O.K., Gwanak-Ku**
Duksung Trading Co., TEL: 854-5047
Intl **Netherlands, Koperwerf**
Koning en Hartman Elektrotechniek B.V., TEL: 70-210101
Intl **New Zealand, Auckland**
Professional Elctrns., TEL: 493-029, 499-048
Intl **Norway, Oslo**
Neco A/S, TEL: (02) 25-93-10
Intl **Singapore, Singapore**
Dynamar International Ltd., TEL: 7476188
Intl **South Africa, Capetown**
Electrolink (Pty) Ltd., TEL: 215350
Intl **Spain, Barcelona**
Sisteco S.A., TEL: 321-7347
Intl **Sweden, Solna**
AB Betoma, TEL: 08-820280
Intl **Taiwan, Taipei**
Dynamar International Ltd., TEL: 235-1139
Intl **United Kingdom, Kent**
Candy Elctrn. Comps., TEL: 0622-70774/5
Intl **United Kingdom, Kent**
House of Power, TEL: 0689 71531/7
Intl **United Kingdom, London**
Unitrode (U.K.) Ltd., TEL: 01-318-1431/4
Intl **United Kingdom, Thames, Oxon**
Thame Comps. Ltd., TEL: 084-421-4561

Universal

Universal Semiconductor Inc.
1925 Zanker Road
San Jose, California 95112
408-279-2830
TWX: 910-338-7617
All other information:
Sales & Mktg. .... (408) 279-2830

Sales Office & Representatives

AL **Huntsville**
Macro Marketing Assocs., 205-883-9630
AZ **Tempe**
EDS, 602-829-9699
CA **San Diego**
De Pierre & Assocs., 619-578-2555
IN **Greenfield**
France Enterprises, 317-462-6098
MA **Waltham**
Betronic, 617-894-8400
TX **Austin**
O.M. Sales, Inc., 512-452-1838
TX **Dallas**
O.M. Sales, Inc., 214-241-3876
TX **Houston**
O.M. Sales, Inc., 713-789-4426
WA **Kirkland**
Electronic Mktg. Assoc., 206-827-9350

Distributors

CA **Fullerton**
Groh Associates, 714-738-7105, 213-923-0963
CA **Mtn. View**
Straube Associates, 415-969-6060
FL **Melbourne**
R-Rep Company, 305-725-6993
NY **Manhasset**
WIN-COR Electronics Sales, 516-627-9474
PA **Willow Grove**
Q.E.D. Electronics, 814

Varix Corporation

Varix Corporation
122 Spanish Village, Suite 608
Dallas, Texas 75248
214-620-0925

Specific product information:
Byron E. Jacobs
Application engineering:
Douglas Traster
Literature:
Amy Henness
Price and delivery:
Respective sales office
Follow-up on order:
Respective sales office
All other information:
Byron E. Jacobs

VLSI Design Associates

VLSI Design Associates
4010 Moorpark Avenue
San Jose, California 95117
408-985-7270

VLSI Technology

VLSI Technology, Inc. (VTI)
1101 McKay Drive
San Jose, California 95131
408-942-1810
TELEX: 278-807
TELEX: 176-151

Sales Office & Representatives

CA **El Segundo**
Varigon Assocs., 213-322-1120
CA **Irvine**
VLSI Sales Office, 714-833-3103
CA **San Diego**
Bestronics, Inc., 619-452-5500
CA **San Jose**
VLSI Sales Office, 408-942-1810
CA **Sunnyvale**
Emerging Technology, 408-720-0240
CA **Sunnyvale**
James Inds., Inc., 408-749-1122
FL **Boca Raton**
Lawrence Assocs., Inc., 305-368-7373
FL **Clearwater**
Lawrence Assocs., Inc., 305-339-2828
FL **West Melbourne**
Lawrence Assocs., Inc., 305-724-8294
IL **Inverness**
James Industries, 312-358-8000
IL **Schaumburg**
James Inds., Inc., 312-884-8000
MA **Burlington**
VLSI Sales Office, 617-229-6555
MN **Minneapolis**
Micro Resources, Inc., 612-830-1454
MN **Minneapolis**
Micro Resources, Inc., 612-830-1454
NM **Albuquerque**
Varigon Associates, 505-344-5503
NY **Pleasantville**
ABC Electronics, 914-769-8088
NY **Williston Park**
ABC Electronics, 516-747-6610
OH **Rocky River**
Norm Case Assocs., 216-333-0400
OR **Portland**
Micro Sales, Inc., 503-297-4726
TX **Austin**
Logic 1 Sales, Inc., 512-459-1297
TX **Dallas**
VLSI Sales Office, 214-387-8350
TX **Houston**
Logic 1 Sales, Inc., 713-462-0641
TX **Richardson**
Logic 1 Sales, Inc., 214-234-0765
WA **Bellevue**
Micro Sales, Inc., 206-451-0568

Votrax

Votrax Division of Federal Screw Works
500 Stephenson Highway
Troy, Michigan 48084
Business Products Group—313-588-2050
TELEX: 8102324140 VOTRAX TRMI

Distributors

Intl **Australia, Sydney**
Dick Smith Electronics Pty., Ltd., TEL: 61 2 888 3200
Intl **West Germany, Wiesbaden**
Dr. Otto Soskuty, TEL: 6121 463822

Weitek

Weitek Corporation
3255 Scott Boulevard, Building 2B
Santa Clara, California 95054
408-727-6625
TELEX: 171596 AAA Com Suvl

Sales Office & Representatives

Intl **Japan, Tokyo**
Nippon Imex Corp.

Western Digital

Western Digital Corporation
2445 McCabe Way
Irvine, California 92714
714-557-3550
TWX: 910-595-1139

Sales Office & Representatives

AL **Huntsville**
Pioneer/Huntsville, 205-837-9300
AL **Huntsville**
Rep. Inc., 205-881-9270
AZ **Scottsdale**
Summit Sales, 602-998-4850
CA **Culver City**
Bestronics, 213-870-9191
CA **Irvine**
Bestronics, 714-979-9910
CA **Los Altos**
El Repco, 415-962-0660
CA **Mountain View**
San Jose District Office, 415-941-0216
CA **Newport Beach**
Western Regional Sales Office, 714-851-1221
CA **San Diego**
Bestronics, 619-452-5500
CA **San Diego**
San Diego District Office, 619-457-1777
CA **Woodland Hills**
Bestronics, 213-704-5616, 714-521-6392
CO **Denver**
Component Sales, 303-759-1666
CT **Norwalk**
Pioneer-Harvey/Norwalk, 203-853-1515
CT **Ridgefield**
Phoenix Sales, 203-438-9644
FL **Altamonte Springs**
Pioneer/Florida, 305-834-9090
FL **Casselberry**
Southern Regional Sales Office, 305-331-4434
FL **Clearwater**
Dyne-A-Mark Inc., 813-441-4702
FL **Ft. Lauderdale**
Dyne-A-Mark Inc., 305-771-6501
FL **Ft. Lauderdale**
Ft. Lauderdale Branch, 305-421-1355
FL **Ft. Lauderdale**
Pioneer, Ft. Lauderdale, 305-771-7520
FL **Maitland**
Dyne-A-Mark Inc., 305-831-2097
FL **Palm Bay**
Dyne-A-Mark Inc., 305-727-1092
GA **Norcross**
Pioneer/Atlanta, 404-448-1711
GA **Tucker**
Rep. Inc., 404-938-4358
IL **Des Plaines**
Janus, 312-298-9330
IL **Elk Grove Village**
Pioneer/Chicago, 312-437-9680
IL **Oakbrook**
Chicago District Office, 312-655-8781
IN **Indianapolis**
Pioneer/Indiana, 317-849-7300
IA **Davenport**
Design Solutions, 319-322-4142
KS **Wichita**
Design Solutions, 316-529-0114
KY **Louisville**
Fred A. Dorsey Assoc., 502-426-3540
MD **Gaithersburg**
Pioneer/Washington, 301-921-0660
MD **Severna Park**
New Era Sales, 301-544-4100
MA **Lexington**
Pioneer-Harvey/Lexington, 617-863-1200
MA **Marblehead**
Northeast Regional Sales Office, 617-631-6466
MA **Woburn**
Component Technology, 617-933-5390
MI **Grosse Pointe Park**
Greiner Assoc., 313-499-0188
MI **Livonia**
Pioneer/Michigan, 313-525-1800
MN **Bloomington**
Central Regional Sales Office, 612
MN **Edina**
Mel Foster Tech. Sales, 612-941-9790
MN **Minnetonka**
Pioneer/Twin Cities, 612-935-5444
MO **Ballwin**
Design Solutions, 314-227-7170
NJ **Montvale**
New Jersey District Office
NJ **Pine Brook**
Pioneer-Harvey/Pine Brook, 201-227-1262
NY **Binghamton**
Pioneer-Harvey/Binghamton, 607-748-8211
NY **Commack**
E.R.A., 516-543-0510
NY **Fairport**
Pioneer-Harvey/Rochester, 716-381-7070
NY **Hauppauge**
Pioneer/Military, 516-231-9200
NY **Rochester**
Ossmann Components, 716-424-4460
NY **Syracuse**
Ossmann Components, 315-455-6611
NY **Woodbury**
Pioneer-Harvey/Woodbury, 516-921-8700
NC **Greensboro**
Greensboro District Office, 919-299-6733
NC **Greensboro**
Pioneer/Carolina, 919-273-4441

Western Digital (Cont)

NC **Raleigh**
Rep. Inc., 919-851-3007

OH **Chagrin Falls**
Midwest Marketing Assoc., 216-247-6655

OH **Cleveland**
Pioneer/Cleveland, 216-587-3600

OH **Dayton**
Midwest Marketing Assoc., 513-433-2511

OH **Dayton**
Pioneer/Dayton, 513-236-9000

PA **Erdenheim**
Omni Sales, 215-233-4600

PA **Horsham**
Pioneer Delaware Valley, 215-674-4000

PA **Pittsburgh**
Pioneer/Pittsburgh, 412-782-2300

TN **Jefferson City**
Rep. Inc., 615-475-4105

TX **Austin**
Pioneer/Austin, 512-835-4000

TX **Austin**
West & Assoc., 512-454-3681

TX **Dallas**
Dallas Distrit Office, 214-248-6785

TX **Dallas**
Pioneer/Dallas, 214-386-7300

TX **Dallas**
West & Associates, 214-248-7060

TX **Houston**
Pioneer/Houston, 713-988-5555

TX **Houston**
West & Assoc., 713-777-4108

UT **Salt Lake City**
Component Sales, 801-466-8623

WA **Renton**
Components West, 206-271-5252

WI **Milwaukee**
Janus, 414-476-9104

Can **Downsview, Ontario**
Weber Elctrns., 416-663-5670

Intl **Australia, Sandringham, Victoria**
Daneva Australia, TEL: 61/03-5985622

Intl **Belgium, Ougree (Liege)**
MCA Tronix, TEL: 41/362795, 41/362780

Intl **Brazil, Sao Paulo-SP**
Cosele Ltda., TEL: 230/1733, 230/1994

Intl **Denmark, Kokkedal**
C-88, TEL: 45/02-244888

Intl **England, Ilford, Essex**
Pronto Enctrns., TEL: 44/01-5546222

Intl **Finland, Espoo**
Komdel OY, TEL: 358/90-885011

Intl **France, Levallois-Perret**
Technology Resources, TEL: 33/1-757-3133

Intl **Hong Kong, Quarry Bay**
White & Allcock, TEL: 852/5-632112-8, 852/5-644312

Intl **Israel, Givataim**
E.I.M. Intl., TEL: 761423, 767251

Intl **Italy, Milano**
Comprel S.R.L., TEL: 39/2-6120641

Intl **Japan, Tokyo**
Panetron Div., TEL: 81/03-343-4411

Intl **Netherlands, Am Utrecht**
Diode BV, TEL: 31/030-884214

Intl **Norway, Nesbru**
Hans. h. Schive, TEL: 47/02-785160

Intl **South Africa, Pingowrie**
South Continental Dev., TEL: 27/(011) 798-2400

Intl **South India, Trivandrum, PIN**
Kryonix

Intl **Spain, Madrid**
Diode SA., TEL: 455/3686

Intl **Sweden, Vaellingby**
Teleimport AB, TEL: 46/08-890265

Intl **Switzerland, Baden Daettwil**
W. Stolz AG, TEL: 41/056-840151

Intl **Taiwan, Taipei**
Taiwan Automation, TEL: 886/02-77109403

Intl **United Kingdom, Epsom**
Europe Regional Sales Office, TEL: 44-3727-42178

Intl **West Germany, Munchen**
Electronics 2000, TEL: 49/089-434061

Distributors

AL **Huntsville**
R.M. Electronics, 205-852-1550

AZ **Phoenix**
Kierulff Elctrns., 602-243-4104

AZ **Phoenix**
Wyle EMG, 602-249-2232

AZ **Tempe**
Anthem Elctrns., 602-244-0900

AZ **Tempe**
Bell Inds., 602-966-7800

CA **Chatsworth**
Anthem Elctrns., 213-700-1000

CA **Commerce**
Kierulff Elctrns., 213-725-0325

CA **El Segundo**
Wyle EMG, 213-322-8100

CA **Irvine**
Wyle EMG, 714-863-9953

CA **Irvine**
Wyle EMG, 714-851-9953

CA **Palo Alto**
Kierulff Elctrns., 415-924-8522

CA **Rancho Cordova**
Wyle EMG, 916-638-5282

CA **San Diego**
Anthem Elctrns., 619-279-5200

CA **San Diego**
Kierulff Elctrns., 619-278-2112

CA **San Diego**
Wyle EMG, 619-565-9171

CA **San Jose**
Anthem Elctrns., 408-946-8000

CA **Santa Clara**
Wyle EMG, 408-727-2500

CA **Sunnyvale**
Bell Inds., 408-734-8570

CA **Tustin**
Anthem Elctrns., 714-730-8000

CA **Tustin**
Kierulff Elctrns., 714-731-5711

CO **Englewood**
Anthem Electronics, 303-790-4500

CO **Englewood**
Kierulff Elctrns., 303-790-4444

CO **Thornton**
Wyle EMG, 303-457-9953

CO **Wheatridge**
Bell Inds., 303-424-1985

CT **Danbury**
Diplomat Elctrns., 203-797-9674

CT **Wallingford**
Kierulff Elctrns., 203-265-1115

FL **Clearwater**
Diplomat Elctrns., 813-443-3514

FL **Ft. Lauderdale**
Hammond Electronics, 305-973-7103

FL **Ft. Lauderdale**
Kierulff Electronics, 305-486-4004

FL **Orlando**
Hammond Elctrns., 305-849-6060, 800-432-6720

FL **St. Petersburg**
Kierulff Elctrns., 813-576-1966

GA **Norcross**
Diplomat Elctrns., 404-449-4133

GA **Norcross**
Kierulff Electronics, 404-447-5252

IL **Bensenville**
Diplomat Elctrns., 312-595-1000

IL **Chicago**
Bell Inds., 312-982-9210

IL **Elk Grove Village**
Kierulff Elctrns., 312-640-0200

IL **Lombard**
R.M. Electronics, 312-932-5150

IN **Indianapolis**
R.M. Electronics, 317-247-9701

IA **Cedar Rapids**
DEECO Inc., 319-365-7551

MD **Baltimore**
Kierulff Electronics, 301-247-5020

MD **Columbia**
Diplomat Elctrns., 301-995-1226

MD **Columbia**
Future Electronics, 301-995-1222

MD **Columbia**
Time Electronics, 301-995-1668

MA **Billerica**
Kierulff Elctrns., 617-667-8331

MA **Wilmington**
R.C. Components, 617-657-4310

MA **Woburn**
Diplomat Elctrns., 617-935-6611

MA **Woburn**
Time-New England, 617-435-8080

MN **Edina**
Kierulff Elctrns., 612-941-7500

MO **Maryland Heights**
Kierulff Elctrns., 314-739-0855

NJ **Bellmawr**
Mid-Atlantic Elctrns., 609-931-5303

NJ **Fairfield**
Kierulff Elctrns., 201-575-6750

NJ **Totowa**
Diplomat Elctrns., 201-785-1830

NM **Albuquerque**
Alliance Elctrns., 505-292-3360

NY **Farmingdale**
S.A.I., 516-294-2710

Western Digital (Cont)

NY **Hauppauge**
Time Electronics, 516-273-0100

NY **Liverpool**
Diplomat Elctrns., 315-652-5000

NY **Melville**
Diplomat Elctrns., 516-454-6400

NY **Rochester**
Rochester Radio Supply, 716-454-7800

NC **Greensboro**
Hammond Electronics, 919-275-6391

NC **Raleigh**
Kierulff Elctrns., 919-872-4410

OH **Bedford Heights**
Kierulff Elctrns., 216-587-6558

OK **Tulsa**
Kierulff Elctrns., 918-252-7537

OK **Tulsa**
Quality Comps., 918-664-8812

OR **Hillsboro**
Wyle EMG, 503-640-6000

OR **Lake Oswego**
Bell Inds., 503-241-4115

PA **Broomall**
Time Mid-Atlantic, 215-359-1200

SC **Greenville**
Hammond Electronics, 803-233-4121

TX **Addison**
Quality Comps., 214-387-4949

TX **Austin**
Active Components Technology, 512-452-5254

TX **Austin**
Kierulff Elctrns., 512-835-2090

TX **Austin**
Quality Comps., 512-835-0220

TX **Dallas**
Active Components Technology, 214-980-1888

TX **Dallas**
Kierulff Elctrns., 214-343-2400

TX **Houston**
Active Components Technology, 713-496-4000

TX **Houston**
Kierulff Elctrns., 713-530-7030

TX **Sugarland**
Quality Comps., 713-491-2255

UT **Salt Lake City**
Bell Inds., 801-972-6969

UT **Salt Lake City**
Kierulff Elctrns., 801-973-6913

UT **Salt Lake City**
Wyle EMG, 801-974-9955

WA **Bellevue**
Anthem Electronics, 206-881-0850

WA **Bellevue**
Bell Inds., 206-747-1515

WA **Bellevue**
Wyle EMG, 206-453-8300

WA **Tukwila**
Kierulff Elctrns., 206-573-4220

WI **Waukesha**
Kierulff Elctrns., 414-784-8160

Can **Brampton, Ontario**
Zentronics Inc., 416-451-9600

Can **Dorval, Quebec**
Semad Elctrns., 514-636-4614

Can **Downsview, Ontario**
Semad Elctrns., 416-663-5680, 416-663-5650

Can **Ottawa, Ontario**
Semad Elctrns., 613-729-6145

Intl **Australia, Sandringham, Victoria**
Daneva Australia, TEL: 61/03-5985622

Intl **Belgium, Ougree (Liege)**
MCA Tronix, TEL: 41/362795, 41/362780

Intl **Brazil, Sao Paulo-SP**
Cosele Ltda., TEL: 230/1733, 230/1994

Intl **Denmark, Kokkedal**
C-88, TEL: 45/02-244888

Intl **England, Ilford, Essex**
Pronto Electronics, TEL: 44/01-5546222

Intl **Finland, Espoo**
Komdel OY, TEL: 358/90-885011

Intl **France, Levallois-Perret**
Technology Resources, TEL: 33/1-757-3133

Intl **Hong Kong, Quarry Bay**
White & Allcock, TEL: 852/5-632112-8, 852/5-644312

Intl **Israel, Givataim**
E.I.M. Intl., TEL: 761423, 767251

Intl **Italy, Milano**
Comprel S.R.L., TEL: 39/2-6120641

Intl **Japan, Tokyo**
Panetron Div., TEL: 81/03-343-4411

Intl **Netherlands, Am Utrecht**
Diode BV, TEL: 31/030-884214

Intl **Norway, Nesbru**
Hans H. Schive, TEL: 47/02-785160

Intl **South Africa, Pinegowrie**
South Continental Dev., TEL: 27/(011) 798-2400

Intl **South India, Trivandrum, PIN**
Kyronix

Intl **Spain, Madrid**
Diode SA., TEL: 455/3686

Intl **Sweden, Vaellingby**
Teleimport AB, TEL: 46/08-890265

Intl **Switzerland, Baden Daettwil**
W. Stolz AG, TEL: 41/056-840151

Intl **Taiwan, Taipei**
Taiwan Automation, TEL: 886/02-77109403

Intl **West Germany, Munchen**
Electronics 2000, TEL: 49/089-434061

Wintek

Wintek Corporation
1801 South Street
Lafayette, Indiana 47904-2993
317-742-8428

Distributors

CA **Santa Clara**
PBC Associates, 408-727-7244

CO **Parker**
Western Marketing Associates, 303-841-2788

IL **Downers Grove**
Physics Equipment, Inc., 312-960-4053

TX **Houston**
Dyna Marketing, 713-937-0278

UT **Logan**
Western Marketing Associates, 801-753-0073

Xicor

Xicor, Inc.
851 Buckeye Court
Milpitas, California 95035
408-946-6920
TWX: 910-379-0033

Sales Office & Representatives

AL **Huntsville**
Beacon, 205-881-5031

AZ **Scottsdale**
Thom Luke Sales, Inc., 602-941-1901

CA **Irvine**
Centaur Corporation, 714-556-5420

CA **Los Altos**
Ewing-Foley, Inc., 415-941-4525

CA **Newport Beach**
Xicor Southwestern Sales Office, 714-752-8700

CA **San Jose**
Xicor Northwestern Sales Office, 408-292-2011

CA **Woodland Hills**
Centaur Corporation, 213-704-1655

CO **Denver**
D/Z Assocs., Inc., 303-429-9369

CT **Waterbury**
HLM Assocs., 203-753-9894

FL **Clearwater**
Beacon, 813-796-2378

FL **Ft. Lauderdale**
Beacon, 305-491-1054

FL **Maitland**
Beacon, 305-647-3498

FL **Melbourne**
Beacon, 305-724-8010

GA **Atlanta**
Beacon, 404-256-9640

ID **Rathdrum**
Vantage

IL **Elk Grove Village**
Oasis Sales Corp., 312-640-1850

IL **Schaumburg**
Xicor Central Sales Office, 312-490-1310

IN **Indianapolis**
Chuck Horn & Assoc., 317-241-9276

IN **Indianapolis**
SAI Mktg. Corp., 317-241-9276

IA **Cedar Rapids**
Chuck Horn & Associates, 319-393-8703

KS **Overland Park**
Kebco, Inc., 913-541-8431

KS **Wichita**
Kebco, Inc., 316-733-1301

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Intl **Denmark, Havdrup**
Henckel Elektronik, TEL: 45.2.38.57.91
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Positron, TEL: 49.07156.3560

Xycom

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Zendex

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415-828-3000

Zilog

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1315 Dell Avenue
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408-370-8000
TWX: 910-338-7621

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Hi-Tek Distribution, TEL: 954-81996

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Intl **United Kingdom, Slough, Berkshire**
Crellon Elctrns. Ltd., TEL: 6286-4434/4300

Intl **West Germany, Eching**
Kontron Electronik GmbH, TEL: 089-319011

Intl **West Germany, Uterhaching**
E.B.V. Electronik, TEL: 89-611051

ZyMOS

ZyMOS Inc.
P.O. Box 62379
Sunnyvale, California 94088
408-730-8800

Zytrex Corporation

Zytrex Corporation
224 North Wolfe Road
Sunnyvale, California 94086
408-733-3973

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