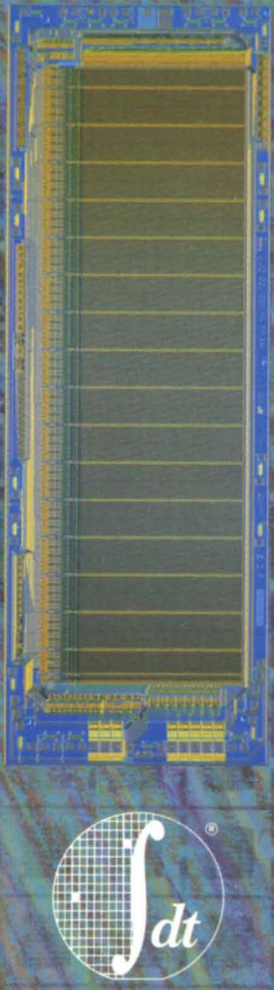
1991 DATABOOK

SRAM



Integrated Device Technology, Inc.

Integrated Device Technology, Inc.

1991
STATIC RAM
DATA BOOK

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Printed in U.S.A.

GENERAL INFORMATION 1

CONTENTS OVERVIEW

Historically, Integrated Device Technology has presented our product offerings entirely under one cover. For ease of use for our customers, we have divided the products into four separate data books — Logic, Specialized Memory, RISC and Static RAM.

IDT's 1991 Static RAM Data Book is comprised of new and revised data sheets and application notes for the SRAM product line. Also included is a current, complete packaging section for all IDT product groups. This section will be updated in each subsequent data book with the latest available packages.

The Static RAM Data Book's Table of Contents contains a listing of the products contained in the 1991 SRAM Data Book, as well as those products which are contained in the remaining three data books. The numbering scheme is slightly different from the past. The number in the bottom center of the page denotes the section number and the sequence of the data sheet within that section, (i.e. 5.5 would be the fifth data sheet in the fifth section). The number in the lower right hand corner is the page number of that particular data sheet.

Integrated Device Technology, a recognized leader in high-speed CMOS technology, produces a broad line of products, enabling us to provide a complete CMOS solution to designers of high-performance digital systems. Our products include industry standard devices, as well as products with speed, lower power, package and/or architectural benefits that allow the designer to achieve significantly improved system performance.

Use this book to find ordering information: Start with the Ordering Information chart at the back of each data sheet or the Cross Reference Guides (in Section 1), along with the Package Outline Index (page 4.2), to compose the complete IDT part number. Reference data on our Technology Capabilities and Quality Commitments are included in separate sections (2 and 3, respectively).

Use this book to find product data: Start with the Table of Contents, organized by product line (page 1.3), or with the Numeric Table of Contents across all product lines (page 1.4). These indexes will direct you to the page on which the complete technical data sheet can be found. Data sheets may be of the following type:

ADVANCE INFORMATION — contain initial descriptions, subject to change, for products that are in development, including features and block diagrams.

PRELIMINARY — contain descriptions for products soon to be, or recently, released to production, including features, pinouts and block diagrams. Timing data are based on simulation or initial characterization and are subject to change upon full characterization.

FINAL — contain minimum and maximum limits specified over the complete supply and temperature range for full production devices.

New products, product performance enhancements, additional package types and new product families are being introduced frequently. Please contact your local IDT sales representative to determine the latest device specifications, package types and product availability.

LIFE SUPPORT POLICY

Integrated Device Technology's products are not authorized for use as critical components in life support devices or systems unless a specific written agreement pertaining to such intended use is executed between the manufacturer and an officer of IDT.

1. Life support devices or systems are devices or systems which (a) are intended for surgical implant into the body or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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1990-91 LOGIC DATA BOOK

The following is a listing of the data sheets located in the 1990-91 Logic Data Book available under separate cover:

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READ/WRITE BUFFER PRODUCTS

ERROR DETECTION AND CORRECTION PRODUCTS

GRAPHICS PRODUCTS

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STANDARD LOGIC PRODUCTS (CONTINUED)

APPLICATION AND TECHNICAL NOTES

Complex Logic Products Technical Notes

Complex Logic Products Application Notes

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Complex Logic Products Application Notes (Continued)

SPECIALIZED MEMORIES DATA BOOK

The following is a listing of the data sheets located in the 1990-91 Specialized Memories Data Book available under separate cover:

ECL PRODUCTS

FIFO PRODUCTS

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FIFO PRODUCTS (CONTINUED)

SPECIALTY MEMORY PRODUCTS

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CACHE MODULES

WRITABLE CONTROL STORE MODULES

OTHER MODULES

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FIFO Products Application Notes

FIFO Products Technical Notes

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Subsystems Products Application Notes

RISC DATA BOOK

The following is a list of data sheets located in the 1991 RISC Data Book available under separate cover:

RISC PROCESSING COMPONENTS

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RISC Microprocessor Products Application Notes

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NUMERICAL TABLE OF CONTENTS (CONTINUED)

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NUMERICAL TABLE OF CONTENTS (CONTINUED)

NUMERICAL TABLE OF CONTENTS (CONTINUED)

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NUMERICAL TABLE OF CONTENTS (CONTINUED)

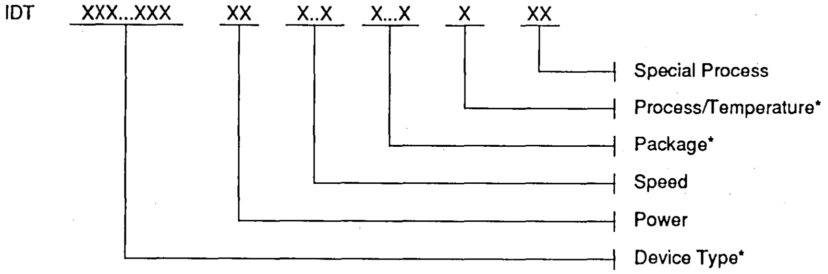
IDT PACKAGE MARKING DESCRIPTION

PART NUMBER DESCRIPTION

IDT's part number identifies the basic product, speed, power, package(s) available, operating temperature and processing grade. Each data sheet has a detailed description, using the part number, for ordering the proper product for the user's application. The part number is comprised of a series of alpha-numeric characters:

1. An "IDT" corporate identifier for Integrated Device Technology, Inc.
2. A basic device part number composed of alpha-numeric characters.
3. A device power identifier, composed of one or two alpha characters, is used to identify the power options. In most cases, the following alpha characters are used:
   "S" or "SA" is used for the standard product's power.
   "L" or "LA" is used for lower power than the standard product.
4. A device speed identifier, when applicable, is either alpha characters, such as "A" or "B", or numbers, such as 20 or 45. The speed units, depending on the product, are in nanoseconds or megahertz.
5. A package identifier, composed of one or two characters. The data sheet should be consulted to determine the packages available and the package identifiers for that particular product.
6. A temperature/process identifier. The product is available in either the commercial or military temperature range, processed to a commercial specification, or the product is available in the military temperature range with full compliance to MIL-STD-883. Many of IDT's products have burn-in included as part of the standard commercial process flow.
7. A special process identifier, composed of alpha characters, is used for products which require radiation enhancement (RE) or radiation tolerance (RT).

Example for Monolithic Devices:



* Field Identifier Applicable To All Products

2507 drw 01

ASSEMBLY LOCATION DESIGNATOR

IDT uses various locations for assembly. These are identified by an alpha character in the last letter of the date code marked on the package. Presently, the assembly location alpha character is as follows:

A = Anam, Korea
I = USA
P = Penang, Malaysia

MIL-STD-883C COMPLIANT DESIGNATOR

IDT ships military products which are compliant to the latest revision of MIL-STD-883C. Such products are identified by a "C" designation on the package. The location of this designator is specified by internal documentation at IDT.

Integrated Device Technology, Inc.

STATIC RAM
CROSS REFERENCE GUIDE

CYPRESS	IDT
CY6116-xxPC	IDT6116SAxxP
CY6116-xxDC	IDT6116SAxxD
CY6116-xxLC	IDT6116SAxxL28
CY6116-xxDMB	IDT6116SAxxDB
CY6116-xxLMB	IDT6116SAxxL28B
CY6117-xxLMB	IDT6116SAxxL32B
CY6116A-xxPC	IDT6116SAxxP
CY6116A-xxDC	IDT6116SAxxD
CY6116A-xxLC	IDT6116SAxxL28
CY6116A-xxDMB	IDT6116SAxxDB
CY6116A-xxLMB	IDT6116SAxxL28B
CY6117A-xxLMB	IDT6116SAxxL32B
CY7C128-xxPC	IDT6116SAxxTP
CY7C128-xxVC	IDT6116SAxxY
CY7C128-xxDC	IDT6116SAxxTD
CY7C128-xxLC	IDT6116SAxxL24
CY7C128-xxKMB	IDT6116SAxxEB
CY7C128-xxDMB	IDT6116SAxxTDB
CY7C128-xxLMB	IDT6116SAxxL24B
CY7C128A-xxPC	IDT6116SAxxTP
CY7C128A-xxVC	IDT6116SAxxY
CY7C128A-xxDC	IDT6116SAxxTD
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CY7C161A-xxLMB	IDT71981SxxLB
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CY7C162-xxDC	IDT71982SxxD
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CY7C162-xxLC	IDT71982SxxL
CY7C162A-xxPC	IDT71982SxxP
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CY7C162A-xxVC	IDT71982SxxY
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CY7C164-xxDC	IDT7188SxxD
CY7C164A-xxPC	IDT7188SxxP
CY7C164A-xxVC	IDT7188SxxY
CY7C164A-xxDC	IDT7188SxxD
CY7C164A-xxDMB	IDT7188SxxCB
CY7C164A-xxKMB	IDT7188SxxEB
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CY7C166A-xxPC	IDT6198SxxP
CY7C166A-xxVC	IDT6198SxxY
CY7C166A-xxDC	IDT6198SxxD
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CY7C170-xxDMB	IDT61970SxxDB
CY7C170A-xxPC	IDT61970SxxP
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CYPRESS	IDT
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EDI	IDT
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EDI8164CxxLB	IDT7187SxxL22B
EDI8164PxxQB	IDT7187LxxDB
EDI8164PxxLB	IDT7187LxxL22B
EDI8416CxxQB	IDT7188SxxDB
EDI8417CxxQB	IDT6198SxxDB
EDI8417CxxLB	IDT6198SxxLB
EDI8832C-xxCB	IDT71256SxxDB
EDH8832C-xxKMHR	IDT71256SxxDB
EDH8832C-xxDMHR	IDT71256SxxDB
EDH8832C-xxQMHR	IDT71256SxxTDB
EDI8832C-xxLB	IDT71256SxxL32B
EDH8832C-xxJMHR	IDT71256SxxL32B
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FUJITSU	IDT
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MB81C68A-xxP	IDT6168SAxxP
MB81C68A-xxZ	IDT6168SAxxD
MB81C69A-xxTV	IDT6168SAxxL
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MB81C69A-xxZ	IDT6168SAxxD
MB81C71-xxP	IDT7187SxxP
MB81C71-xxC	IDT7187SxxD
MB81C71-xxCV	IDT7187SxxL22
MB81C71A-xxP	IDT7187SxxP
MB81C71A-xxC	IDT7187SxxD
MB81C71A-xxCV	IDT7187SxxL22
MB81C71A-xxPJ	IDT7187SxxY
MB81C74-xxP	IDT7188SxxP
MB81C75-xxP	IDT7198SxxP
MB81C75-xxCV	IDT7198SxxL
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MB81C78A-xxCV	IDT7164SxxL32

HITACHI	IDT
HM6267P-xx	IDT6167SAxxP
HM6267LP-xx	IDT6167LAxxP
HM6268P-xx	IDT6168SAxxP
HM6268LP-xx	IDT6168LAxxP
HM6287P-xx	IDT7187SxxP
HM6287HP-xx	IDT7187SxxP
HM6287HAP-xx	IDT7187SxxP
HM6287LP-xx	IDT7187LxxP
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HM6788HAP-xx	IDT7188SxxP
HM6288LP-xx	IDT7188LxxP
HM6289P-xx	IDT6198SxxP
HM6789HP-xx	IDT6198SxxP
HM6789HAP-xx	IDT6198SxxP
HM6289LP-xx	IDT6198LxxP
HM6208P-xx	IDT71258SxxP
HM6208HP-xx	IDT71258SxxP
HM6208LP-xx	IDT71258LxxP
HM6208HLP-xx	IDT71258LxxP

HITACHI	IDT
HM6708P-xx	IDT71B258SxxP
HM6708AP-xx	IDT71B258SxxP
HM6209P-xx	IDT61298SxxP
HM6209HP-xx	IDT61298SxxP
HM6209LP-xx	IDT61298LxxP
HM6209HLP-xx	IDT61298LxxP
HM6708P-xx	IDT61B298SxxP
HM6708AP-xx	IDT61B298SxxP
HM62832P-xx	IDT71256SxxTP
HM62832HP-xx	IDT71256SxxTP
HM62832LP-xx	IDT71256LxxTP
HM62832HLP-xx	IDT71256LxxTP

INOVA	IDT
S32K8-xxCC	IDT71256SxxD
S32K8-xxMC	IDT71256SxxDB
S32K8L-xxCC	IDT71256LxxD
S32K8L-xxMC	IDT71256LxxDB

LOGIC DEVICES	IDT
L7C167PCxx	IDT6167SAxxP
L7C167DCxx	IDT6167SAxxD
L7C167CCxx	IDT6167SAxxD
L7C167UCxx	IDT6167SAxxSO
L7C167WCxx	IDT6167SAxxY
L7C167KCxx	IDT6167SAxxL
L7C167DMxx	IDT6167SAxxDM
L7C167DMExx	IDT6167SAxxDM
L7C167DMBxx	IDT6167SAxxDB
L7C167CMxx	IDT6167SAxxDM
L7C167CMExx	IDT6167SAxxDM
L7C167CMBxx	IDT6167SAxxDB
L7C167KMxx	IDT6167SAxxLM
L7C167KMExx	IDT6167SAxxLM
L7C167KMBxx	IDT6167SAxxLB
L7C168PCxx	IDT6168SAxxP
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L7C168KMxx	IDT6168SAxxLM
L7C168KMExx	IDT6168SAxxLM
L7C168KMBxx	IDT6168SAxxLB
L7C170PCxx	IDT61970SxxP
L7C170DCxx	IDT61970SxxD
L7C170CCxx	IDT61970SxxD
L7C170WCxx	IDT61970SxxY
L7C170DMxx	IDT61970SxxDM
L7C170DMExx	IDT61970SxxDM
L7C170DMBxx	IDT61970SxxDB

LOGIC DEVICES	IDT
L7C170CMxx	IDT61970SxxDM
L7C170CMExx	IDT61970SxxDM
L7C170CMBxx	IDT61970SxxDB
L7C171PCxx	IDT71681SAxxP
L7C171DCxx	IDT71681SAxxD
L7C171CCxx	IDT71681SAxxD
L7C171WCxx	IDT71681SAxxY
L7C171KCxx	IDT71681SAxxL
L7C171DMxx	IDT71681SAxxDM
L7C171DMExx	IDT71681SAxxDM
L7C171DMBxx	IDT71681SAxxDB
L7C171KMxx	IDT71681SAxxLM
L7C171KMExx	IDT71681SAxxLM
L7C171KMBxx	IDT71681SAxxLB
L7C172PCxx	IDT71682SAxxP
L7C172DCxx	IDT71682SAxxD
L7C172CCxx	IDT71682SAxxD
L7C172WCxx	IDT71682SAxxY
L7C172KCxx	IDT71682SAxxL
L7C172DMxx	IDT71682SAxxDM
L7C172DMExx	IDT71682SAxxDM
L7C172DMBxx	IDT71682SAxxDB
L7C172KMxx	IDT71682SAxxLM
L7C172KMExx	IDT71682SAxxLM
L7C172KMBxx	IDT71682SAxxLB
L6116PCxx	IDT6116SAxxTP
L6116DCxx	IDT6116SAxxTD
L6116CCxx	IDT6116SAxxTD
L6116NCxx	IDT6116SAxxP
L6116HCxx	IDT6116SAxxD
L6116ICxx	IDT6116SAxxD
L6116UCxx	IDT6116SAxxSO
L6116WCxx	IDT6116SAxxY
L6116KCxx	IDT6116SAxxL28
L6116TCxx	IDT6116SAxxL32
L6116DMxx	IDT6116SAxxTDM
L6116DMExx	IDT6116SAxxTDM
L6116DMBxx	IDT6116SAxxTDB
L6116CMxx	IDT6116SAxxTDM
L6116CMExx	IDT6116SAxxTDM
L6116CMBxx	IDT6116SAxxTDB
L6116HMxx	IDT6116SAxxDM
L6116HMExx	IDT6116SAxxDM
L6116HMBxx	IDT6116SAxxDB
L6116IMxx	IDT6116SAxxDM
L6116IMExx	IDT6116SAxxDM
L6116IMBxx	IDT6116SAxxDB
L6116KMxx	IDT6116SAxxL28M
L6116KMExx	IDT6116SAxxL28M
L6116KMBxx	IDT6116SAxxL28B
L6116TMxx	IDT6116SAxxL32M
L6116TMExx	IDT6116SAxxL32M
L6116TMBxx	IDT6116SAxxL32B
L6116LPCxx	IDT6116LAxxTP
L6116LDCxx	IDT6116LAxxTD
L6116LCCxx	IDT6116LAxxTD
L6116LNCxx	IDT6116LAxxP
L6116LHCxx	IDT6116LAxxD
L6116LICxx	IDT6116LAxxD
L6116LUCxx	IDT6116LAxxSO

LOGIC DEVICES	IDT
L6116LWCxx	IDT6116LAxxY
L6116LKCxx	IDT6116LAxxL28
L6116LTCxx	IDT6116LAxxL32
L6116LDMxx	IDT6116LAxxTDM
L6116LDMExx	IDT6116LAxxTDM
L6116LDMBxx	IDT6116LAxxTDB
L6116LCMxx	IDT6116LAxxTDM
L6116LCMExx	IDT6116LAxxTDM
L6116LCMBxx	IDT6116LAxxTDB
L6116LHMxx	IDT6116LAxxDM
L6116LHMExx	IDT6116LAxxDM
L6116LHMBxx	IDT6116LAxxDB
L6116LIMxx	IDT6116LAxxDM
L6116LIMExx	IDT6116LAxxDM
L6116LIMBxx	IDT6116LAxxDB
L6116LKMxx	IDT6116LAxxL28M
L6116LKMExx	IDT6116LAxxL28M
L6116LKMBxx	IDT6116LAxxL28B
L6116LTMxx	IDT6116LAxxL32M
L6116LTMExx	IDT6116LAxxL32M
L6116LTMBxx	IDT6116LAxxL32B
L7C187PCxx	IDT7187SAxxP
L7C187DCxx	IDT7187SAxxD
L7C187CCxx	IDT7187SAxxC
L7C187UCxx	IDT7187SAxxSO
L7C187WCxx	IDT7187SAxxY
L7C187KCxx	IDT7187SAxxL22
L7C187DMxx	IDT7187SAxxDM
L7C187DMExx	IDT7187SAxxDM
L7C187DMBxx	IDT7187SAxxDB
L7C187CMxx	IDT7187SAxxCM
L7C187CMExx	IDT7187SAxxCM
L7C187CMBxx	IDT7187SAxxCB
L7C164PCxx	IDT7188SxxP
L7C164DCxx	IDT7188SxxC
L7C164CCxx	IDT7188SxxD
L7C164UCxx	IDT7188SxxSO
L7C164WCxx	IDT7188SxxY
L7C164DMxx	IDT7188SxxCM
L7C164DMExx	IDT7188SxxCM
L7C164DMBxx	IDT7188SxxCB
L7C164CMxx	IDT7188SxxDM
L7C164CMExx	IDT7188SxxDM
L7C164CMBxx	IDT7188SxxDB
L7C165PCxx	IDT7198SxxP
L7C165DCxx	IDT7198SxxC
L7C165CCxx	IDT7198SxxD
L7C165UCxx	IDT7198SxxSO
L7C165WCxx	IDT7198SxxY
L7C165DMxx	IDT7198SxxCM
L7C165DMExx	IDT7198SxxCM
L7C165DMBxx	IDT7198SxxCB
L7C165CMxx	IDT7198SxxDM
L7C165CMExx	IDT7198SxxDM
L7C165CMBxx	IDT7198SxxDB
L7C166PCxx	IDT6198SxxP
L7C166DCxx	IDT6198SxxC
L7C166CCxx	IDT6198SxxD
L7C166UCxx	IDT6198SxxSO

LOGIC DIVICES	IDT
L7C166WCxx	IDT6198SxxY
L7C166DMxx	IDT6198SxxCM
L7C166DMExx	IDT6198SxxCM
L7C166DMBxx	IDT6198SxxCB
L7C166CMxx	IDT6198SxxDM
L7C166CMExx	IDT6198SxxDM
L7C166CMBxx	IDT6198SxxDB
L7C161PCxx	IDT71981SxxP
L7C161DCxx	IDT71981SxxD
L7C161CCxx	IDT71981SxxD
L7C161WCxx	IDT71981SxxY
L7C161KCxx	IDT71981SxxL
L7C161DMxx	IDT71981SxxDM
L7C161DMExx	IDT71981SxxDM
L7C161DMBxx	IDT71981SxxDB
L7C161CMxx	IDT71981SxxDM
L7C161CMExx	IDT71981SxxDM
L7C161CMBxx	IDT71981SxxDB
L7C161KMxx	IDT71981SxxLM
L7C161KMExx	IDT71981SxxLM
L7C161KMBxx	IDT71981SxxLB
L7C162PCxx	IDT71982SxxP
L7C162DCxx	IDT71982SxxD
L7C162CCxx	IDT71982SxxD
L7C162WCxx	IDT71982SxxY
L7C162KCxx	IDT71982SxxL
L7C162DMxx	IDT71982SxxDM
L7C162DMExx	IDT71982SxxDM
L7C162DMBxx	IDT71982SxxDB
L7C162CMxx	IDT71982SxxDM
L7C162CMExx	IDT71982SxxDM
L7C162CMBxx	IDT71982SxxDB
L7C162KMxx	IDT71982SxxLM
L7C162KMExx	IDT71982SxxLM
L7C162KMBxx	IDT71982SxxLB
L7C185PCxx	IDT7164SxxTP
L7C185DCxx	IDT7164SxxTC
L7C185CCxx	IDT7164SxxTD
L7C185NCxx	IDT7164SxxP
L7C185HCxx	IDT7164SxxD
L7C185ICxx	IDT7164SxxD
L7C185UCxx	IDT7164SxxSO
L7C185VCxx	IDT7164SxxPE
L7C185WCxx	IDT7164SxxY
L7C185KCxx	IDT7164SxxL28
L7C185TCxx	IDT7164SxxL32
L7C185DMxx	IDT7164SxxTCM
L7C185DMExx	IDT7164SxxTCM
L7C185DMBxx	IDT7164SxxTCB
L7C185CMxx	IDT7164SxxTCM
L7C185CMExx	IDT7164SxxTCM
L7C185CMBxx	IDT7164SxxTCB
L7C185HMxx	IDT7164SxxDM
L7C185HMExx	IDT7164SxxDM
L7C185HMBxx	IDT7164SxxDB
L7C185IMxx	IDT7164SxxDM
L7C185IMExx	IDT7164SxxDM
L7C185IMBxx	IDT7164SxxDB
L7C185KMxx	IDT7164SxxL28M
L7C185KMExx	IDT7164SxxL28M

LOGIC DEVICES	IDT
L7C185KMBxx	IDT7164SxxL28B
L7C185TMxx	IDT7164SxxL32M
L7C185TMExx	IDT7164SxxL32M
L7C185TMBxx	IDT7164SxxL32B
L7CL185PCxx	IDT7164LxxTP
L7CL185DCxx	IDT7164LxxTC
L7CL185CCxx	IDT7164LxxTD
L7CL185NCxx	IDT7164LxxP
L7CL185HCxx	IDT7164LxxD
L7CL185ICxx	IDT7164LxxD
L7CL185UCxx	IDT7164LxxLO
L7CL185VCxx	IDT7164LxxPE
L7CL185WCxx	IDT7164LxxY
L7CL185KCxx	IDT7164LxxL28
L7CL185TCxx	IDT7164LxxL32
L7CL185DMxx	IDT7164LxxTCM
L7CL185DMExx	IDT7164LxxTCM
L7CL185DMBxx	IDT7164LxxTCB
L7CL185CMxx	IDT7164LxxTCM
L7CL185CMExx	IDT7164LxxTCM
L7CL185CMBxx	IDT7164LxxTCB
L7CL185HMxx	IDT7164LxxDM
L7CL185HMExx	IDT7164LxxDM
L7CL185HMBxx	IDT7164LxxDB
L7CL185IMxx	IDT7164LxxDM
L7CL185IMExx	IDT7164LxxDM
L7CL185IMBxx	IDT7164LxxDB
L7CL185KMxx	IDT7164LxxL28M
L7CL185KMExx	IDT7164LxxL28M
L7CL185KMBxx	IDT7164LxxL28B
L7CL185TMxx	IDT7164LxxL32M
L7CL185TMExx	IDT7164LxxL32M
L7CL185TMBxx	IDT7164LxxL32B
L7C194PCxx	IDT71B258SxxTP
L7C194DCxx	IDT71B258SxxTC
L7C194CCxx	IDT71B258SxxTD
L7C194VCxx	IDT71B258SxxSO
L7C194WCxx	IDT71B258SxxY
L7C194DMxx	IDT71B258SxxTCM
L7C194DMExx	IDT71B258SxxTCM
L7C194DMBxx	IDT71B258SxxTCB
L7C194CMxx	IDT71B258SxxTDM
L7C194CMExx	IDT71B258SxxTDM
L7C194CMBxx	IDT71B258SxxTDB
L7C195PCxx	IDT61B298SxxTP
L7C195DCxx	IDT61B298SxxTC
L7C195CCxx	IDT61B298SxxTD
L7C195VCxx	IDT61B298SxxSO
L7C195WCxx	IDT61B298SxxY
L7C195DMxx	IDT61B298SxxTCM
L7C195DMExx	IDT61B298SxxTCM
L7C195DMBxx	IDT61B298SxxTCB
L7C195CMxx	IDT61B298SxxTDM
L7C195CMExx	IDT61B298SxxTDM
L7C195CMBxx	IDT61B298SxxTDB
L7C191PCxx	IDT71281SxxP
L7C191DCxx	IDT71281SxxC
L7C191CCxx	IDT71281SxxD
L7C191VCxx	IDT71281SxxSO
L7C191WCxx	IDT71281SxxY
L7C191DMxx	IDT71281SxxCM
L7C191DMExx	IDT71281SxxCM
L7C191DMBxx	IDT71281SxxCB
L7C191CMxx	IDT71281SxxDM
L7C191CMExx	IDT71281SxxDM
L7C191CMBxx	IDT71281SxxDB
L7C192PCxx	IDT71282SxxP
L7C192DCxx	IDT71282SxxC
L7C192CCxx	IDT71282SxxD
L7C192VCxx	IDT71282SxxSO
L7C192WCxx	IDT71282SxxY
L7C192DMxx	IDT71282SxxCM
L7C192DMExx	IDT71282SxxCM
L7C192DMBxx	IDT71282SxxCB
L7C192CMxx	IDT71282SxxDM
L7C192CMExx	IDT71282SxxDM
L7C192CMBxx	IDT71282SxxDB
L7C199PCxx	IDT71256SxxTP
L7C199DCxx	IDT71256SxxTD
L7C199CCxx	IDT71256SxxTD
L7C199NCxx	IDT71256SxxP
L7C199HCxx	IDT71256SxxD
L7C199ICxx	IDT71256SxxD
L7C199VCxx	IDT71256SxxSO
L7C199WCxx	IDT71256SxxY
L7C199TCxx	IDT71256SxxL32
L7C199DMxx	IDT71256SxxTDM
L7C199DMExx	IDT71256SxxTDM
L7C199DMBxx	IDT71256SxxTDB
L7C199CMxx	IDT71256SxxTDM
L7C199CMExx	IDT71256SxxTDM
L7C199CMBxx	IDT71256SxxTDB
L7C199HMxx	IDT71256SxxDM
L7C199HMExx	IDT71256SxxDM
L7C199HMBxx	IDT71256SxxDB
L7C199IMxx	IDT71256SxxDM
L7C199IMExx	IDT71256SxxDM
L7C199IMBxx	IDT71256SxxDB
L7C199TMxx	IDT71256SxxL32M
L7C199TMExx	IDT71256SxxL32M
L7C199TMBxx	IDT71256SxxL32B
L7CL199PCxx	IDT71256LxxTP
L7CL199DCxx	IDT71256LxxTD
L7CL199CCxx	IDT71256LxxTD
L7CL199NCxx	IDT71256LxxP
L7CL199HCxx	IDT71256LxxD
L7CL199ICxx	IDT71256LxxD
L7CL199VCxx	IDT71256LxxSO
L7CL199WCxx	IDT71256LxxY
L7CL199TCxx	IDT71256LxxL32
L7CL199DMxx	IDT71256LxxTDM
L7CL199DMExx	IDT71256LxxTDM
L7CL199DMBxx	IDT71256LxxTDB
L7CL199CMxx	IDT71256LxxTDM
L7CL199CMExx	IDT71256LxxTDM
L7CL199CMBxx	IDT71256LxxTDB
L7CL199HMxx	IDT71256LxxDM
L7CL199HMExx	IDT71256LxxDM
L7CL199HMBxx	IDT71256LxxDB
L7CL199IMxx	IDT71256LxxDM
L7CL199IMExx	IDT71256LxxDM
L7CL199IMBxx	IDT71256LxxDB
L7CL199TMxx	IDT71256LxxL32M
L7CL199TMExx	IDT71256LxxL32M
L7CL199TMBxx	IDT71256LxxL32B
L7C180PCxx	IDT6178SxxP
L7C180DCxx	IDT6178SxxD
L7C180CCxx	IDT6178SxxD
L7C180WCxx	IDT6178SxxY
L7C180DMxx	IDT6178SxxDM
L7C180DMExx	IDT6178SxxDM
L7C180DMBxx	IDT6178SxxDB
L7C180CMxx	IDT6178SxxDM
L7C180CMExx	IDT6178SxxDM
L7C180CMBxx	IDT6178SxxDB
L7C174PCxx	IDT71B74SxxTP
L7C174DCxx	IDT71B74SxxTC
L7C174CCxx	IDT71B74SxxTD
L7C174NCxx	IDT71B74SxxP
L7C174HCxx	IDT71B74SxxD
L7C174WCxx	IDT71B74SxxY
L7C174TCxx	IDT71B74SxxL32
L7C174DMxx	IDT71B74SxxTCM
L7C174DMExx	IDT71B74SxxTCM
L7C174DMBxx	IDT71B74SxxTCB
L7C174CMxx	IDT71B74SxxTDM
L7C174CMExx	IDT71B74SxxTDM
L7C174CMBxx	IDT71B74SxxTDB
L7C174TMxx	IDT71B74SxxL32M
L7C174TMExx	IDT71B74SxxL32M
L7C174TMBxx	IDT71B74SxxL32B
L7C186PCxx	IDT71B65SxxTP
L7C186DCxx	IDT71B65SxxTC
L7C186CCxx	IDT71B65SxxTD
L7C186NCxx	IDT71B65SxxP
L7C186HCxx	IDT71B65SxxD
L7C186VCxx	IDT71B65SxxY
L7C186TCxx	IDT71B65SxxL32
L7C186DMxx	IDT71B65SxxTCM
L7C186DMExx	IDT71B65SxxTCM
L7C186DMBxx	IDT71B65SxxTCB
L7C186CMxx	IDT71B65SxxTDM
L7C186CMExx	IDT71B65SxxTDM
L7C186CMBxx	IDT71B65SxxTDB
L7C186HMxx	IDT71B65SxxDM
L7C186HMExx	IDT71B65SxxDM
L7C186HMBxx	IDT71B65SxxDB

MICRON	IDT
MT5C1601-xx	IDT6167SAxxP
MT5C1601C-xx	IDT6167SAxxD
MT5C1601DJ-xx	IDT6167SAxxY
MT5C1601EC-xx	IDT6167SAxxL
MT5C1601-xxL	IDT6167LAxxP
MT5C1601C-xxL	IDT6167LAxxD
MT5C1601DJ-xxL	IDT6167LAxxY
MT5C1601EC-xxL	IDT6167LAxxL
MT5C1604-xx	IDT6168SAxxP
MT5C1604C-xx	IDT6168SAxxD
MT5C1604DJ-xx	IDT6168SAxxY

MICRON	IDT
MT5C1604EC-xx	IDT6168SAxxL
MT5C1604-xxL	IDT6168LAxxP
MT5C1604C-xxL	IDT6168LAxxD
MT5C1604DJ-xxL	IDT6168LAxxY
MT5C1604EC-xxL	IDT6168LAxxL
MT5C1605-xx	IDT61970SAxxP
MT5C1605DJ-xx	IDT61970SAxxY
MT5C1605C-xx	IDT61970SAxxD
MT5C1605-xxL	IDT61970LAxxP
MT5C1605DJ-xxL	IDT61970LAxxY
MT5C1605C-xxL	IDT61970LAxxD
MT5C1606-xx	IDT71681SAxxP
MT5C1606C-xx	IDT71681SAxxD
MT5C1606DJ-xx	IDT71681SAxxY
MT5C1606EC-xx	IDT71681SAxxL
MT5C1606-xxL	IDT71681LAxxP
MT5C1606C-xxL	IDT71681LAxxD
MT5C1606DJ-xxL	IDT71681LAxxY
MT5C1606EC-xxL	IDT71681LAxxL
MT5C1607-xx	IDT71682SAxxP
MT5C1607C-xx	IDT71682SAxxD
MT5C1607DJ-xx	IDT71682SAxxY
MT5C1607EC-xx	IDT71682SAxxL
MT5C1607-xxL	IDT71682LAxxP
MT5C1607C-xxL	IDT71682LAxxD
MT5C1607DJ-xxL	IDT71682LAxxY
MT5C1607EC-xxL	IDT71682LAxxL
MT5C1608-xx	IDT6116SAxxTP
MT5C1608DJ-xx	IDT6116SAxxY
MT5C1608EC-xx	IDT6116SAxxL28
MT5C1608C-xx	IDT6116SAxxTD
MT5C1608C-xx 883C	IDT6116SAxxTDB
MT5C1608EC-xx 883C	IDT6116SAxxL28B
MT5C1608-xxL	IDT6116LAxxTP
MT5C1608DJ-xxL	IDT6116LAxxY
MT5C1608EC-xxL	IDT6116LAxxL28
MT5C1608C-xxL	IDT6116LAxxTD
MT5C1608C-xxL 883C	IDT6116LAxxTDB
MT5C1608EC-xxL 883C	IDT6116LAxxL28B
MT5C6401-xx	IDT7187SxxP
MT5C6401C-xx	IDT7187SxxD
MT5C6401DJ-xx	IDT7187SxxY
MT5C6401EC-xx	IDT7187SxxL22
MT5C6401C-xx 883C	IDT7187SxxCB
MT5C6401EC-xx 883C	IDT7187SxxL22B
MT5C6401-xxL	IDT7187LxxP
MT5C6401C-xxL	IDT7187LxxD
MT5C6401DJ-xxL	IDT7187LxxY
MT5C6401EC-xxL	IDT7187LxxL22
MT5C6401C-xxL 883C	IDT7187LxxCB
MT5C6401EC-xxL 883C	IDT7187LxxL22B
MT5C6404-xx	IDT7188SxxP
MT5C6404C-xx	IDT7188SxxD
MT5C6404DJ-xx	IDT7188SxxY
MT5C6404C-xx 883C	IDT7188SxxCB
MT5C6404-xxL	IDT7188LxxP
MT5C6404C-xxL	IDT7188LxxD

MICRON	IDT
MT5C6404DJ-xxL	IDT7188LxxY
MT5C6404C-xxL 883C	IDT7188LxxCB
MT5C6405-xx	IDT7198SxxP
MT5C6405C-xx	IDT7198SxxD
MT5C6405DJ-xx	IDT7198SxxY
MT5C6405EC-xx	IDT7198SxxL
MT5C6405-xxL	IDT7198LxxP
MT5C6405C-xxL	IDT7198LxxD
MT5C6405DJ-xxL	IDT7198LxxY
MT5C6405EC-xxL	IDT7198LxxL
MT5C6406-xx	IDT71981SxxP
MT5C6406C-xx	IDT71981SxxD
MT5C6406DJ-xx	IDT71981SxxY
MT5C6406EC-xx	IDT71981SxxL
MT5C6406-xxL	IDT71981LxxP
MT5C6406C-xxL	IDT71981LxxD
MT5C6406DJ-xxL	IDT71981LxxY
MT5C6406EC-xxL	IDT71981LxxL
MT5C6407-xx	IDT71982SxxP
MT5C6407C-xx	IDT71982SxxD
MT5C6407DJ-xx	IDT71982SxxY
MT5C6407EC-xx	IDT71982SxxL
MT5C6407-xxL	IDT71982LxxP
MT5C6407C-xxL	IDT71982LxxD
MT5C6407DJ-xxL	IDT71982LxxY
MT5C6407EC-xxL	IDT71982LxxL
MT5C6408-xx	IDT7164SxxTP
MT5C6408C-xx	IDT7164SxxTC
MT5C6408DJ-xx	IDT7164SxxY
MT5C6408EC-xx	IDT7164SxxL28
MT5C6408ECW-xx	IDT7164SxxL32
MT5C6408C-xx 883C	IDT7164SxxTCB
MT5C6408CW-xx 883C	IDT7164SxxDB
MT5C6408EC-xx 883C	IDT7164SxxL28B
MT5C6408ECW-xx 883C	IDT7164SxxL32B
MT5C6408-xxL	IDT7164LxxTP
MT5C6408C-xxL	IDT7164LxxTC
MT5C6408DJ-xxL	IDT7164LxxY
MT5C6408EC-xxL	IDT7164LxxL28
MT5C6408ECW-xxL	IDT7164LxxL32
MT5C6408C-xxL 883C	IDT7164LxxTCB
MT5C6408CW-xxL 883C	IDT7164LxxDB
MT5C6408EC-xxL 883C	IDT7164LxxL28B
MT5C6408ECW-xxL 883C	IDT7164LxxL32B
MT5C2568-xx	IDT71256SxxTP
MT5C2568C-xx	IDT71256SxxTD
MT5C2568DJ-xx	IDT71256SxxY
MT5C2568EC-xx	IDT71256SxxL28
MT5C2568W-xx	IDT71256SxxP
MT5C2568CW-xx	IDT71256SxxD
MT5C2568ECW-xx	IDT71256SxxL32
MT5C2568C-xx 883C	IDT71256SxxTDB
MT5C2568CW-xx 883C	IDT71256SxxDB
MT5C2568EC-xx 883C	IDT71256SxxL28B
MT5C2568ECW-xx 883C	IDT71256SxxL32B
MT5C2568F-xx 883C	IDT71256SxxFB
MT5C2568-xxL	IDT71256LxxTP
MT5C2568C-xxL	IDT71256LxxTD

MICRON	IDT
MT5C2568DJ-xxL	IDT71256LxxY
MT5C2568EC-xxL	IDT71256LxxL28
MT5C2568W-xxL	IDT71256LxxP
MT5C2568CW-xxL	IDT71256LxxD
MT5C2568ECW-xxL	IDT71256LxxL32
MT5C2568C-xxL 883C	IDT71256LxxTDB
MT5C2568CW-xxL 883C	IDT71256LxxDB
MT5C2568EC-xxL 883C	IDT71256LxxL28B
MT5C2568ECW-xxL 883C	IDT71256LxxL32B
MT5C2568F-xxL 883C	IDT71256LxxFB
MT5C2564-xx	IDT71B258SxxTP
MT5C2564C-xx	IDT71B258SxxTC
MT5C2564DJ-xx	IDT71B258SxxY
MT5C2564C-xx 883C	IDT71B258SxxTCB
MT5C2564-xxL	IDT71B258LxxTP
MT5C2564C-xxL	IDT71B258LxxTC
MT5C2564DJ-xxL	IDT71B258LxxY
MT5C2564C-xxL 883C	IDT71B258LxxTCB
MT5C2565-xx	IDT61B298SxxTP
MT5C2565C-xx	IDT61B298SxxTC
MT5C2565DJ-xx	IDT61B298SxxY
MT5C2565C-xx 883C	IDT61B298SxxTCB
MT5C2565-xxL	IDT61B298LxxTP
MT5C2565C-xxL	IDT61B298LxxTC
MT5C2565DJ-xxL	IDT61B298LxxY
MT5C2565C-xxL 883C	IDT61B298LxxTCB

MITSUBISHI	IDT
M5M21C67P-xx	IDT6167LAxxP
M5M21C68P-xx	IDT6168LAxxP
M5M5165FP-xx	IDT7164SxxSO
M5M5165FP-xxL	IDT7164LxxSO
M5M5178P-xx	IDT7164LxxP
M5M5187AD-xx	IDT7187LxxL22
M5M5187AP-xx	IDT7187LxxP
M5M5187P-xx	IDT7187LxxP
M5M5188AD-xx	IDT7188LxxL22
M5M5188AP-xx	IDT7188LxxP
M5M5188P-xx	IDT7188LxxP

MOTOROLA	IDT
MCM2018ANxx	IDT6116SAxxP
MCM4180Pxx	IDT6178SxxP
MCM62351Pxx	IDT6178SxxP
MCM62350Pxx	IDT6178SxxP
MCM4180Jxx	IDT6178SxxY
MCM62351Jxx	IDT6178SxxY
MCM62350Jxx	IDT6178SxxY
4180-xx/BXAJC	IDT6178SxxDB
MCM6164Cxx	IDT7164SxxD
MCM61L64Cxx	IDT7164LxxD
MCM6264Pxx	IDT7164SxxP
MCM6264NJxx	IDT7164SxxY
6164-xx/BXAJC	IDT7164SxxDB
6164-xx/BUAJC	IDT7164SxxL32B

MOTOROLA	IDT
MCM6168Pxx	IDT6168SAxxP
MCM6268Pxx	IDT6168SAxxP
MCM6269Pxx	IDT6168SAxxP
6168-xx/BRAJC	IDT6168SAxxDB
6168-xx/BUAJC	IDT6168SAxxLB
6268-xx/BRAJC	IDT6168SAxxDB
6268-xx/BUAJC	IDT6168SAxxLB
MCM6270Pxx	IDT61970SxxP
MCM6270Jxx	IDT61970SxxY
MCM6206Pxx	IDT71256SxxTP
MCM6206Jxx	IDT71256SxxY
6206-xx/BXAJC	IDT71256SxxDB
MCM6287Pxx	IDT7187SxxP
MCM6287Jxx	IDT7187SxxY
6287-xx/BXAJC	IDT7187SxxCB
6287-xx/BUAJC	IDT7187SxxL22B
MCM6288Pxx	IDT7188SxxP
6288-xx/BXAJC	IDT7188SxxCB
MCM6290Pxx	IDT7198SxxP
MCM6290Jxx	IDT7198SxxY
MCM6205Pxx	IDT71259SxxP
MCM6205Jxx	IDT71259SxxY
MCM6208Pxx	IDT71B258SxxTP
MCM6208Jxx	IDT71B258SxxY
MCM6209Pxx	IDT61B298SxxTP
MCM6209Jxx	IDT61B298SxxY

PERFORMANCE	IDT
P4C116-xxDC	IDT6116SAxxTD
P4C116-xxSC	IDT6116SAxxSO
P4C116-xxPC	IDT6116SAxxTP
P4C116-xxDM	IDT6116SAxxTDM
P4C116-xxDMB	IDT6116SAxxTDB
P4C116L-xxDC	IDT6116LAxxTD
P4C116L-xxSC	IDT6116LAxxSO
P4C116L-xxPC	IDT6116LAxxTP
P4C116L-xxDM	IDT6116LAxxTDM
P4C116L-xxDMB	IDT6116LAxxTDB
P4C164-xxCC	IDT7164SxxTC
P4C164-xxLC	IDT7164SxxL28
P4C164-xxPC	IDT7164SxxTP
P4C164-xxJC	IDT7164SxxY
P4C164-xxDW	IDT7164SxxD
P4C164-xxCM	IDT7164SxxTCM
P4C164-xxDWM	IDT7164SxxDM
P4C164-xxLM	IDT7164SxxL28M
P4C164-xxCMB	IDT7164SxxTCB
P4C164-xxDWMB	IDT7164SxxDB
P4C164-xxLMB	IDT7164SxxL28B
P4C164L-xxCC	IDT7164LxxTC
P4C164L-xxLC	IDT7164LxxL28
P4C164L-xxPC	IDT7164LxxTP
P4C164L-xxJC	IDT7164LxxY
P4C164L-xxDW	IDT7164LxxD
P4C164L-xxCM	IDT7164LxxTCM

PERFORMANCE	IDT
P4C164L-xxDWM	IDT7164LxxDM
P4C164L-xxLM	IDT7164LxxL28M
P4C164L-xxCMB	IDT7164LxxTCB
P4C164L-xxDWMB	IDT7164LxxDB
P4C164L-xxLMB	IDT7164LxxL28B
P4C163-xxCC	IDT7169SxxTC
P4C163-xxLC	IDT7169SxxL28
P4C163-xxPC	IDT7169SxxTP
P4C163-xxJC	IDT7169SxxY
P4C163-xxCM	IDT7169SxxTCM
P4C163-xxLM	IDT7169SxxL28M
P4C163-xxCMB	IDT7169SxxTCB
P4C163-xxLMB	IDT7169SxxL28B
P4C163L-xxCC	IDT7169LxxTC
P4C163L-xxLC	IDT7169LxxL28
P4C163L-xxPC	IDT7169LxxTP
P4C163L-xxJC	IDT7169LxxY
P4C163L-xxCM	IDT7169LxxTCM
P4C163L-xxLM	IDT7169LxxL28M
P4C163L-xxCMB	IDT7169LxxTCB
P4C163L-xxLMB	IDT7169LxxL28B
P4C168-xxDC	IDT6168SAxxD
P4C168-xxPC	IDT6168SAxxP
P4C168-xxSC	IDT6168SAxxSO
P4C168-xxDM	IDT6168SAxxDM
P4C168-xxDMB	IDT6168SAxxDB
P4C168L-xxDC	IDT6168LAxxD
P4C168L-xxPC	IDT6168LAxxP
P4C168L-xxSC	IDT6168LAxxSO
P4C168L-xxDM	IDT6168LAxxDM
P4C168L-xxDMB	IDT6168LAxxDB
P4C1681-xxDC	IDT71681SAxxD
P4C1681-xxSC	IDT71681SAxxSO
P4C1681-xxPC	IDT71681SAxxP
P4C1681-xxDM	IDT71681SAxxDM
P4C1681-xxDMB	IDT71681SAxxDB
P4C1681L-xxDC	IDT71681LAxxD
P4C1681L-xxSC	IDT71681LAxxSO
P4C1681L-xxPC	IDT71681LAxxP
P4C1681L-xxDM	IDT71681LAxxDM
P4C1681L-xxDMB	IDT71681LAxxDB
P4C1682-xxDC	IDT71682SAxxD
P4C1682-xxSC	IDT71682SAxxSO
P4C1682-xxPC	IDT71682SAxxP
P4C1682-xxDM	IDT71682SAxxDM
P4C1682-xxDMB	IDT71682SAxxDB
P4C1682L-xxDC	IDT71682LAxxD
P4C1682L-xxSC	IDT71682LAxxSO
P4C1682L-xxPC	IDT71682LAxxP
P4C1682L-xxDM	IDT71682LAxxDM
P4C1682L-xxDMB	IDT71682LAxxDB
P4C187-xxCC	IDT7187SxxD
P4C187-xxPC	IDT7187SxxP
P4C187-xxLC	IDT7187SxxL22
P4C187-xxJC	IDT7187SxxY
P4C187-xxCM	IDT7187SxxCM
P4C187-xxLM	IDT7187SxxL22M
P4C187-xxCMB	IDT7187SxxCB

PERFORMANCE	IDT
P4C187-xxLMB	IDT7187SxxL22B
P4C187L-xxCC	IDT7187LxxD
P4C187L-xxPC	IDT7187LxxP
P4C187L-xxLC	IDT7187LxxL22
P4C187L-xxJC	IDT7187LxxY
P4C187L-xxCM	IDT7187LxxCM
P4C187L-xxLM	IDT7187LxxL22M
P4C187L-xxCMB	IDT7187LxxCB
P4C187L-xxLMB	IDT7187LxxL22B
P4C188-xxCC	IDT7188SxxD
P4C188-xxPC	IDT7188SxxP
P4C188-xxJC	IDT7188SxxY
P4C188-xxCM	IDT7188SxxCM
P4C188-xxCMB	IDT7188SxxCB
P4C188L-xxCC	IDT7188LxxD
P4C188L-xxPC	IDT7188LxxP
P4C188L-xxJC	IDT7188LxxY
P4C188L-xxCM	IDT7188LxxCM
P4C188L-xxCMB	IDT7188LxxCB
P4C198-xxCC	IDT6198SxxD
P4C198-xxLC	IDT6198SxxL
P4C198-xxPC	IDT6198SxxP
P4C198-xxJC	IDT6198SxxY
P4C198-xxCM	IDT6198SxxCM
P4C198-xxLM	IDT6198SxxLM
P4C198-xxCMB	IDT6198SxxCB
P4C198-xxLMB	IDT6198SxxLB
P4C198L-xxCC	IDT6198LxxD
P4C198L-xxLC	IDT6198LxxL
P4C198L-xxPC	IDT6198LxxP
P4C198L-xxJC	IDT6198LxxY
P4C198L-xxCM	IDT6198LxxCM
P4C198L-xxLM	IDT6198LxxLM
P4C198L-xxCMB	IDT6198LxxCB
P4C198L-xxLMB	IDT6198LxxLB
P4C198A-xxCC	IDT7198SxxD
P4C198A-xxLC	IDT7198SxxL
P4C198A-xxPC	IDT7198SxxP
P4C198A-xxJC	IDT7198SxxY
P4C198A-xxCM	IDT7198SxxCM
P4C198A-xxLM	IDT7198SxxLM
P4C198A-xxCMB	IDT7198SxxCB
P4C198A-xxLMB	IDT7198SxxLB
P4C198AL-xxCC	IDT7198LxxD
P4C198AL-xxLC	IDT7198LxxL
P4C198AL-xxPC	IDT7198LxxP
P4C198AL-xxJC	IDT7198LxxY
P4C198AL-xxCM	IDT7198LxxCM
P4C198AL-xxLM	IDT7198LxxLM
P4C198AL-xxCMB	IDT7198LxxCB
P4C198AL-xxLMB	IDT7198LxxLB
P4C1981-xxCC	IDT71981SxxD
P4C1981-xxLC	IDT71981SxxL
P4C1981-xxPC	IDT71981SxxP
P4C1981-xxJC	IDT71981SxxY
P4C1981-xxCM	IDT71981SxxDM
P4C1981-xxLM	IDT71981SxxLM
P4C1981-xxCMB	IDT71981SxxDB
P4C1981-xxLMB	IDT71981SxxLB

PERFORMANCE	IDT
P4C1981L-xxCC	IDT71981LxxD
P4C1981L-xxLC	IDT71981LxxL
P4C1981L-xxPC	IDT71981LxxP
P4C1981L-xxJC	IDT71981LxxY
P4C1981L-xxCM	IDT71981LxxDM
P4C1981L-xxLM	IDT71981LxxLM
P4C1981L-xxCMB	IDT71981LxxDB
P4C1981L-xxLMB	IDT71981LxxLB
P4C1982-xxCC	IDT71982SxxD
P4C1982-xxLC	IDT71982SxxL
P4C1982-xxPC	IDT71982SxxP
P4C1982-xxJC	IDT71982SxxY
P4C1982-xxCM	IDT71982SxxDM
P4C1982-xxLM	IDT71982SxxLM
P4C1982-xxCMB	IDT71982SxxDB
P4C1982-xxLMB	IDT71982SxxLB
P4C1982L-xxCC	IDT71982LxxD
P4C1982L-xxLC	IDT71982LxxL
P4C1982L-xxPC	IDT71982LxxP
P4C1982L-xxJC	IDT71982LxxY
P4C1982L-xxCM	IDT71982LxxDM
P4C1982L-xxLM	IDT71982LxxLM
P4C1982L-xxCMB	IDT71982LxxDB
P4C1982L-xxLMB	IDT71982LxxLB
P4C1256-xxPC	IDT71256SxxTP
P4C1256-xxDC	IDT71256SxxD
P4C1256-xxLC	IDT71256SxxL28
P4C1256-xxDM	IDT71256SxxDM
P4C1256-xxLM	IDT71256SxxL28M
P4C1256-xxDMB	IDT71256SxxDB
P4C1256-xxLMB	IDT71256SxxL28B
P4C1256L-xxPC	IDT71256LxxTP
P4C1256L-xxDC	IDT71256LxxD
P4C1256L-xxLC	IDT71256LxxL28
P4C1256L-xxDM	IDT71256LxxDM
P4C1256L-xxLM	IDT71256LxxL28M
P4C1256L-xxDMB	IDT71256LxxDB
P4C1256L-xxLMB	IDT71256LxxL28B
P4C1258-xxPC	IDT71B258SxxTP
P4C1258-xxJC	IDT71B258SxxY
P4C1258-xxCC	IDT71B258SxxTC
P4C1258-xxCM	IDT71B258SxxTCM
P4C1258-xxCMB	IDT71B258SxxTCB
P4C1258L-xxPC	IDT71B258LxxTP
P4C1258L-xxJC	IDT71B258LxxY
P4C1258L-xxCC	IDT71B258LxxTC
P4C1258L-xxCM	IDT71B258LxxTCM
P4C1258L-xxCMB	IDT71B258LxxTCB
P4C1298-xxPC	IDT61B298SxxTP
P4C1298-xxJC	IDT61B298SxxY
P4C1298-xxCC	IDT61B298SxxTC
P4C1298-xxCM	IDT61B298SxxTCM
P4C1298-xxCMB	IDT61B298SxxTCB
P4C1298L-xxPC	IDT61B298LxxTP
P4C1298L-xxJC	IDT61B298LxxY
P4C1298L-xxCC	IDT61B298LxxTC
P4C1298L-xxCM	IDT61B298LxxTCM
P4C1298L-xxCMB	IDT61B298LxxTCB

SGS-THOMSON-MOTEK	IDT
MK41H66NXX	IDT6167SXXP
MK41H67Nxx	IDT6167SxxP
MK41H68Nxx	IDT6168SxxP
MK41H69Nxx	IDT6168SxxP
MK41H78Nxx	IDT61970SxxP
MK41H79Nxx	IDT61970SxxP
MK41H80Nxx	IDT6178SxxP
MK41H80Pxx	IDT6178SxxD
MK41H87Nxx	IDT7187SxxP
MK41H87Xxx	IDT7187SxxY
MK48H65Nxx	IDT7164SxxTP

SONY	IDT
CXK5416P-xx	IDT6168LAxxP
CXK5464P-xx	IDT7188LxxP
CXK5814P-xx	IDT6116LAxxTP
CXK5818PN-xx	IDT6116LAxxP
CXK5818M-xx	IDT6116LAxxSO
CXK58256P-xx	IDT71256LxxP
CXK58256M-xx	IDT71256LxxSO
CXK5864AP-xxL	IDT7164LxxP
CXK5864AM-xxL	IDT7164LxxSO
CXK5865P-xxL	IDT7164LxxP

TOSHIBA	IDT
TMM2018AP-xx	IDT6116SAxxTP
TMM2068AP-xx	IDT6168SAxxP
TC55416P-xx	IDT7188SxxP
TC55416P-xxH	IDT7188SxxP
TC55417P-xx	IDT6198SxxP
TC55417J-xx	IDT6198SxxY
TC55417P-xxH	IDT6198SxxP
TC55417J-xxH	IDT6198SxxY
TC5561P-xx	IDT7187SxxP
TC5561J-xx	IDT7187SxxY
TC5562P-xx	IDT7187SxxP
TC5562J-xx	IDT7187SxxY
TC5588P-xx	IDT7164SxxTP
TC5588J-xx	IDT7164SxxY
TC5589P-xx	IDT7169SxxTP
TC5589J-xx	IDT7169SxxY
TC55328P-xx	IDT71256SxxTP
TC55328J-xx	IDT71256SxxY
TC55329P-xx	IDT71259SxxP
TC55329J-xx	IDT71256SxxY
V61C16Pxx	IDT6116SAxxP

VITELIC	IDT
V61C16Sxx	IDT6116SAxxTP
V61C16Fxx	IDT6116SAxxSO
V61C16PxxL	IDT6116LAxxP
V61C16SxxL	IDT6116LAxxTP
V61C16FxxL	IDT6116LAxxSO
V63C64Sxx	IDT7164SxxTP
V63C64SxxL	IDT7164LxxP
V61C67Pxx	IDT6167SAxxP
V61C67PxxL	IDT6167LAxxP
V61C68Pxx	IDT6168SAxxP
V61C68PxxL	IDT6168LAxxP

Note: "xx" represents Speed Grade wherever it appears.

STATIC RAM SELECTOR GUIDE

Density	Organization	Part No.	Description	Speed (ns)		Page
				Com'l.	Mil.	
16384	2048 x 8	6116	2K x 8 with Power-Down	15–45	20–150	5.1
	4096 x 4	6168	4K x 4 with Power-Down	10–35	12-100	5.4
		6178	4K x 4 Cache Tag	10–25	12–25	5.5
		61970	4K x 4 with Output Enable and Power-Down	10–45	12–55	5.6
		71681/2	4K x 4 Separate I/O and Power-Down	10–45	12–100	5.19
	16384 x 1	6167	16K x 1 with Power-Down	12–35	15–100	5.3
65536	4096 x 16	71586	4K x 16 with Address Latch and Power-Down	25–45	35–55	5.15
	8192 x 8	7164	8K x 8 with Power-Down	15–35	25–200	5.17
		7165	8K x 8 Resettable Power-Down	30–45	35–55	5.18
		7174	8K x 8 Cache Tag	30–45	35–55	5.21
		71B64	8K x 8 BiCEMOS	10–15	12–20	6.12
		71B65	8K x 8 BiCEMOS Resettable	15-25	20-35	6.13
		71B74	8K x 8 BiCEMOS Cache Tag	10–15	12–20	6.15
	16384 x 4	6198	16K x 4 with Output Enable and Power-Down	15–35	20-85	5.7
		7188	16K x 4 with Power-Down	15–35	20–85	5.23
		7198	16K x 4 with Output Enable, 2 CS and Power-Down	15–35	20–85	5.24
		61B98	16K x 4 BiCEMOS with Output Enable	8–12	10–15	6.2
		71981/2	16K x 4 with Separate I/O and Power-Down	15–35	20–85	5.25
		71B88	16K x 4 BiCEMOS	8–12	10–15	6.17
		71B98	16K x 4 BiCEMOS with Output Enable, 2 CS	8–12	10–15	6.18
	65536 x 1	7187	64K x 1 with Power-Down	15–35	20–85	5.22
73728	8192 x 9	7169	8K x 9 with Power-Down	20–35	25–55	5.20
		71569	8K x 9 with Address Latch and Power-Down	20–25	25–35	5.14
		71B569	8K x 9 BiCEMOS with Address Latch	12–20	15–20	6.11
		71B69	8K x 9 BiCEMOS	12–20	15–20	6.14
		71B79	8K x 9 BiCEMOS Cache Tag	10–15	12–20	6.16
147456	4096 x 36	71B221	4K x 18 x 2 BiCEMOS Self-Timed and Address Latch	24-28	28	6.5
		71B222	4K x 18 x 2 BiCEMOS with Dual Address Latches	18-30	25-30	6.6
262144	32768 x 8	71256	32K x 8 with Power-Down	20–45	25–150	5.10
		71B256	32K x 8 BiCEMOS	12–20	20	6.8
		71B556	32K x 8 BiCEMOS with Address Latch	12–20	20	6.10
	65536 x 4	61298	64K x 4 with Output Enable and Power-Down	25–45	25–55	5.2
		71258	64K x 4 with Power-Down	20–45	25–55	5.11
		61B298	64K x 4 BiCEMOS with Output Enable	12–20	15–20	6.1
		71281/2	64K x 4 with Separate I/O and Power-Down	25–45	30–55	5.13
		71B258	64K x 4 BiCEMOS	12–20	15–20	6.9
293912	16384 x 18	71B229	16K x 9 x 2 BiCEMOS Cache RAM	15-28	22-28	6.7
	32768 x 9	71259	32K x 9 with Power-Down	20–35	25–45	5.12
		71589	32K x 9 Burst Mode with Power-Down	15-35	25-35	5.16
1048576	131072 x 8	71024	128K x 8 with Power-Down	25–45	30–55	5.8
		71B024	128K x 8 BiCEMOS	15–25	20–25	6.3
	262144 x 4	71028	256K x 4 with Power-Down	25–45	30–55	5.9
		71B028	256K x 4 BiCEMOS	15–25	20–25	6.4

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IDT...LEADING THE CMOS FUTURE

A major revolution is taking place in the semiconductor industry today. A new technology is rapidly displacing older NMOS and bipolar technologies as the workhorse of the 80's and beyond. That technology is high-speed CMOS. Integrated Device Technology, a company totally predicated on and dedicated to implementing high-performance CMOS products, is on the leading edge of this dramatic change.

Beginning with the introduction of the industry's fastest CMOS 2K x 8 static RAM, IDT has grown into a company with multiple divisions producing a wide range of high-speed CMOS circuits that are, in almost every case, the fastest available. These advanced products are produced with IDT's proprietary CEMOS™ technology, a twin-well, dry-etched, stepper-aligned process utilizing progressively smaller dimensions.

From inception, IDT's product strategy has been to apply the advantages of it's extremely fast CEMOS technology to produce the integrated circuit elements required to implement high-performance digital systems. IDT's goal is to provide the circuits necessary to create systems which are far superior to previous generations in performance, reliability, cost weight and size. Many of the company's innovative product designs offer higher levels of integration, advanced architectures, higher density packaging and system enhancement features that are establishing tomorrow's industry standards. The company is committed to providing its customers with an ever-expanding series of these high-speed, lower-power IC solutions to system design needs.

IDT's commitment, however, extends beyond state-of-the-art technology and advanced products to providing the highest level of customer service and satisfaction in the industry. Producing products to exacting quality standards that provide excellent, long-term reliability is given the same level of importance and priority as device performance. IDT is also dedicated to delivering these high-quality advanced products on time. The company would like to be known not only for its technological capabilities, but also for providing its customers with quick, responsive and courteous service.

IDT's product families are available in both commercial and military grades. As a bonus, commercial customers obtain the benefits of military processing disciplines, established to meet or exceed the stringent criteria of the applicable military specifications.

IDT is the leading U.S. supplier of high-speed CMOS circuits. The company's high-performance fast SRAM , FCT logic family, high-density modules, FIFOs, complex logic products, specialty memories, ECL I/O BiCEMOS™ memories, RISC subsystems, and the 32-bit RISC microprocessor family complement each other to provide high-speed CMOS solutions to a wide range of applications and systems.

Dedicated to maintaining its leadership position as a state-of-the-art IC manufacturer, IDT will continue to focus on maintaining its technology edge as well as developing a broader range of innovative products. New products and speed enhancements are continuously being added to each of the existing product families and additional product lines will be introduced. Contact your IDT field representative or factory marketing engineer to determine the latest product offerings. If you're building state-of-the-art equipment, IDT wants to help you solve some of your design problems.

IDT MILITARY AND DESC-SMD PROGRAM

IDT is a leading supplier of military, high-speed CMOS circuits. The company's high-performance Static RAMs, FCT Logic Family, Complex Logic (CLP), FIFOs, Specialty Memories (SMP), ECL I/O BiCMOS Memories, 32-bit RISC Microprocessor, RISC Subsystems and high-density Subsystems Modules product lines complement each other to provide high-speed CMOS solutions to a wide range of military applications and systems. Most of these product lines offer Class B products which are fully compliant to the latest revision of MIL-STD-883, Paragraph 1.2.1. In addition, IDT offers Radiation Tolerant (RT), as well as Radiation Enhanced (RE), products.

IDT has an active program with the Defense Electronic Supply Center (DESC) to list all of IDT's military compliant devices on Standard Military Drawings (SMD). The SMD program allows standardization of militarized products and reduction of the proliferation of non-standard source control drawings. This program will go far toward reducing the need for each defense contractor to make separate specification control drawings for purchased parts. IDT plans to have SMDs for many of its product offerings. Presently, IDT has 88 devices which are listed or pending listing. The devices are from IDT's SRAM, FCT Logic family, Complex Logic (CLP), FIFOs and Specialty Memories (SMP) product families. IDT expects to add another 20 devices to the SMD program in the near future. Users should contact either IDT or DESC for current status of products in the SMD program.

SMD	
SRAM	**IDT**
84036/D	6116
5962-88740	6116LA
84132/B	6167
5962-86015/A	7187
5962-86859	6198/7198/7188
5962-86705/A	6168
5962-85525/A	7164
5962-88552	71256L
5962-88662	71256S
5962-88611	71682L
5962-88681/A	71258S
5962-88545	71258L
5962-88544	71257L
5962-88725/A	71257S
5962-89690	6116
5962-89691	7198
5962-89692	7188
5962-89712	71982
5962-89892	6198
5962-38294	8Kx8
5962-89598	32Kx8
SMP	**IDT**
5962-86875/A	7130/7140
5962-87002/A	7132/7142
5962-88610/A	7133S/7143S
5962-88665/A	7133L/7143L
CLP	IDT
5962-87708/A	39C10B & C
5962-88535	39C01
5962-88533/A	49C460A
5962-88613	39C60A
5962-88643	49C410
5962-88743	75C48S
5962-86273	7216L
5962-87686	7217L
5962-88733	7210
5962-90579	7381L

SMD	
LOGIC	**IDT**
5962-87630/B	54FCT244/A
5962-87629/C	54FCT245/A
5962-86862/A	54FCT299/A
5962-87644/A	54FCT373/A
5962-87628/C	54FCT374/A
5962-87627	54FCT377/A
5962-87654/A	54FCT138/A
5962-87655	54FCT240/A
5962-87656/A	54FCT273/A
5962-89533	54FCT861A/B
5962-89506	54FCT827A/B
5962-88575	54FCT841A/B
5962-88608	54FCT821A/B
5962-88543/A	54FCT521/A
5962-88640	54FCT161/A
5962-88639	54FCT573/A
5962-88656	54FCT823A/B
5962-88657	54FCT163/A
5962-88674	54FCT825A/B
5962-88661	54FCT863A/B
5962-88736	54FCT520A/B
5962-88775	54FCT646A/B
5962-89508	54FCT139/A
5962-89665	54FCT824A/B
5962-88651	54FCT533/A
5962-88652	54FCT182/A
5962-88653	54FCT645A/B
5962-88654	54FCT640A/B
5962-88655	54FCT534/A
5962-89767	54FCT540/A
5962-89766	54FCT541/A
5962-89733	54FCT191/A
5962-89732	54FCT241/A
5962-89652	54FCT399/A
5962-89513	54FCT574/A
5962-89731	54FCT833A/B
5962-88675	54FCT845A/B
5962-89730	54FCT543/A

SMD	
FIFO	**IDT**
5962-87531	7201LA
5962-86846/A	72404
5962-88669	7203S
5962-89568	7204L
5962-89536	7202L
5962-89863	7201S
5962-89523	72403L
5962-89666	7200L
5962-89942	72103L
5962-89943	72104L
5962-89567	7203L

2509 tbl 01

RADIATION HARDENED TECHNOLOGY

IDT manufactures and supplies radiation hardened products for military/aerospace applications. Utilizing special processing and starting materials, IDT's radiation hardened devices are able to survive in hostile radiation environments. In total dose, dose rate and environments where single event upset is of concern, IDT products are designed to continue functioning without loss of performance. IDT can supply all its products on these processes. Total Dose radiation testing is performed in-house on an ARACOR X-Ray system. External facilities are utilized for device research on gamma cell, LINAC and other radiation equipment. IDT has an on-going research and development program for improving radiation handling capabilities (See "IDT Radiation Tolerant/Enhanced Products for Radiation Environments" in Section 3) of IDT products/ processes.

IDT LEADING EDGE CEMOS TECHNOLOGY

HIGH-PERFORMANCE CEMOS

From IDT's beginnings in 1980, it has had a belief in and a commitment to CMOS. The company developed a high-performance version of CMOS, called enhanced CMOS (CEMOS), that allows the design and manufacture of leading-edge components. It incorporates the best characteristics of traditional CMOS, including low power, high noise immunity and wide operating temperature range; it also achieves speed and output drive equal or superior to bipolar Schottky TTL. The last decade has seen development and production of four "generations" of IDT's CEMOS technology with process improvements which have reduced IDT's electrical effective (L_{eff}) gate lengths by more than 50 percent from 1.3 microns (millionths of a meter) in 1981 to 0.6 microns in 1989.

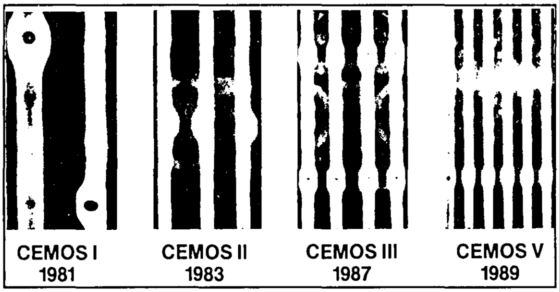
	CEMOS I	CEMOS II		CEMOS III	CEMOS V	CEMOS VI
		A	C			
Calendar Year	**1981**	**1983**	**1985**	**1987**	**1989**	**1990**
Drawn Feature Size	2.5μ	1.7μ	1.3μ	1.2μ	1.0μ	0.8μ
Leff	1.3μ	1.1μ	0.9μ	0.8μ	0.6μ	0.45μ
Basic Process Enhancements	Dual-well, Wet Etch, Projection Aligned	Dry Etch, Stepper	Shrink, Spacer	Silicide, BPSG, BiCEMOS I	BiCEMOS II	BiCEMOS III

2514 drw 01

CEMOS IV = CEMOS III – scaled process optimized for high-speed logic.

Figure 1.

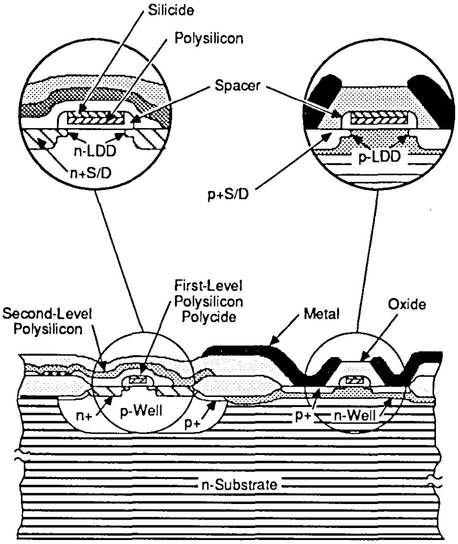
Continual advancement of CEMOS technology allows IDT to implement progressively higher levels of integration and achieve increasingly faster speeds maintaining the company's established position as the leader in high-speed CMOS integrated circuits. In addition, the fundamental process technology has been extended to add bipolar elements to the CEMOS platform. IDT's BiCEMOS process combines the ultra-high speeds of bipolar devices with the lower power and cost of CMOS, allowing us to build even faster components than straight CMOS at a slightly higher cost.



SEM photos (miniaturization)

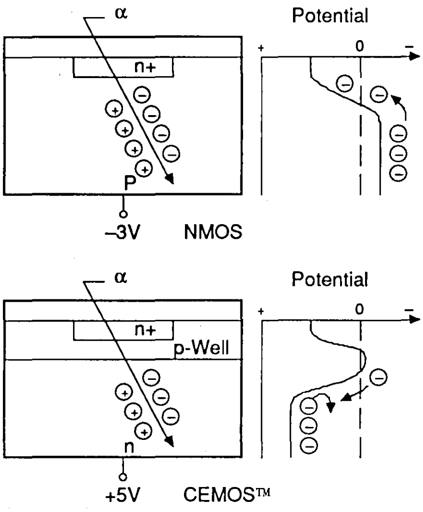
2514 drw 02

Figure 2. Fifteen-Hundred-Power Magnification Scanning Electron Microscope (SEM) Photos of the Four Generations of IDT's CEMOS Technology



2514 drw 03

Figure 3. IDT CEMOS Device Cross Section



2514 drw 04

Figure 4. IDT CEMOS Built-In High Alpha Particle Immunity

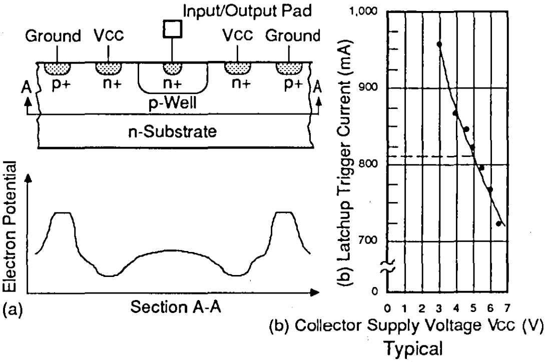
ALPHA PARTICLES

Random alpha particles can cause memory cells to temporarily lose their contents or suffer a "soft error." Traveling with high energy levels, alpha particles penetrate deep into an integrated chip. As they burrow into the silicon, they leave a trail of free electron-hole pairs in their wake.

The cause of alpha particles is well documented and understood in the industry. IDT has considered various techniques to protect the cells from this hazardous occurrence. These techniques include dual-well structures (Figures 3 and 4) and a polymeric compound for die coating. Presently, a polymeric compound is used in many of IDT's SRAMs; however, the specific techniques used may vary and change from one device generation to the next as the industry and IDT improve the alpha particle protection technology.

LATCHUP IMMUNITY

A combination of careful design layout, selective use of guard rings and proprietary techniques have resulted in virtual elimination of latchup problems often associated with older CMOS processes (Figure 5). The use of NPN and N-channel I/O devices eliminates hole injection latchup. Double guard ring structures are utilized on all input and output circuits to absorb injected electrons. These effectively cut off the current paths into the internal circuits to essentially isolate I/O circuits. Compared to older CMOS processes which exhibit latchup characteristics with trigger currents from 10-20mA, IDT products inhibit latchup at trigger currents substantially greater than this.



2514 drw 05

Figure 5. IDT CEMOS Latchup Suppression

SURFACE MOUNT TECHNOLOGY AND IDT'S MODULE PRODUCTS

Requirements for circuit area reduction, utilizing the most efficient and compact component placement possible and the needs of production manufacturing for electronics assemblies are the driving forces behind the advancement of circuit-board assembly technologies. These needs are closely associated with the advances being made in surface mount devices (SMD) and surface mount technology (SMT) itself. Yet, there are two major issues with SMT in production manufacturing of electronic assemblies: high capital expenditures and complexity of testing.

The capital expenditure required to convert to efficient production using SMT is still too high for the majority of electronics companies, regardless of the 20-60% increase in the board densities which SMT can bring. Because of this high barrier to entry, we will continue to see a large market segment [large even compared to the exploding SMT market] using traditional through-hole packages (i.e. DIPs, PGAs, etc) and assembly techniques. How can these types of companies take advantage of SMD and SMT? Let someone else, such as IDT, do it for them by investing time and money in SMT and then in return offer through-hole products utilizing SMT processes. Products which fit this description are multi-chip modules, consisting of SMT assembled SMDs on a through-hole type substrate. Modules enable companies to enjoy SMT density advantages and traditional package options without the expensive startup costs required to do SMT in-house.

Although subcontracting this type of work to an assembly house is an alternative, there still is the other issue of testing, an area where many contract assembly operations fall short of IDT's capability and experience. Prerequisites for adequate module testing sophisticated high performance parametric testers, customized test fixtures, and most importantly the experience to tests today's complex electronic devices. Companies can therefore take advantage of IDT's experience in testing and manufacturing high performance CMOS multi-chip modules.

At IDT, SMD components are electrically tested, environmentally screened, and performance selected for each IDT module. All modules are 100% tested as if they are a separate functional component and are guaranteed to meet all specified parameters at the module output without the customer having to understand the modules' internal workings.

Other added benefits companies get by using IDT's CMOS module products are:

1) a wide variety of high performance, through-hole products utilizing SMD packaged components,
2) fast speeds compared with NMOS based products,
3) low power consumption compared with bipolar technologies, and
4) low cost manufacturability compared with GaAs based products.

IDT has recognized the problems of SMT and began offering CMOS modules as part of its standard product portfolio. IDT modules combine the advantages of:

1) the low power characteristics of IDT's CEMOS™ and BiCEMOS™ products,
2) the density advantages of first class SMD components including those from IDT's components divisions, and
3) experience in system level design, manufacturing, and testing with its own in-house SMT operation.

IDT currently has two divisions (Subsystems and RISC Subsystems) dedicated to the development of module products ranging from simple memory modules to complex VME sized application specific modules to full system level CPU boards. These modules have surface mount devices assembled on both sides of either a multi-layer glass filled epoxy (FR-4) or a multi-layer co-fired ceramic substrate. Assembled modules come available in industry standard through-hole packages and other space-saving module packages. Industry proven vapor-phase or IR reflow techniques are used to solder the SMDs to the substrate during the assembly process. Because of our affiliation with IDT's experienced semiconductor manufacturing divisions, we thoroughly understand and therefore test all modules to the applicable datasheet specifications and customer requirements.

Thus, IDT is able to offer today's electronic design engineers a unique solution for their "need-more-for-less" problem.modules. These high speed, high performance products offer the density advantages of SMD and SMT, the added benefit of low power CMOS technology, and through-hole packaged electronics without the high cost of doing it in-house.

STATE-OF-THE-ART FACILITIES AND CAPABILITIES

Integrated Device Technology is headquartered in Santa Clara, California — the heart of the "Silicon Valley." The company's operations are housed in seven facilities totaling over 500,000 square feet. These facilities house all aspects of business from research and development to design, wafer fabrication, assembly, environmental screening, test and administration. In-house capabilities include scanning electron microscope (SEM) evaluation, particle impact noise detection (PIND), plastic and hermetic packaging, military and commercial testing, burn-in, life test and a full complement of environmental screening equipment.

The over-200,000-square-foot corporate headquarters campus is composed of four buildings. The largest facility on this site is a 100,000 square foot, two-building complex. The first building, a 60,000 square foot facility, is dedicated to the Complex Logic, Standard Logic and RISC Microprocessor product lines, as well as hermetic and plastic package assembly, logic products' test, burn-in, mark and QA, and a reliability/failure analysis lab.

IDT's Packaging and Assembly Process Development teams are located here. To keep pace with the development of new products and to enhance the IDT philosophy of "Innovation," these teams have ultra modern, integrated and correspondingly sophisticated equipment and environments at their disposal. All manufacturing is completed in dedicated clean room areas (Class 10K minimum), with all preseal operations accomplished under Class 100 laminar flow hoods.

Development of assembly materials, processes and equipment is accomplished under a fully operational production environment to ensure reliability and repeatable product. The Hermetic Manufacturing and Process Development team is currently producing custom products to the strict requirements of MIL-STD-883. The fully automated plastic facility is currently producing high volumes of USA-manufactured product, while developing state-of-the-art surface mount technology patterned after MIL-STD-883.

The second building of the complex houses sales, marketing, finance and MIS.

The RISC Subsystems and Subsystems Modules Divisions are located behind the two-building complex in a 54,000 square foot facility. Also located at this facility are Quality Assurance and wafer fabrication services.

Directly across the street from the two-building complex is a newly acquired 50,000 square foot facility that houses administrative services, Northwest Area Sales, Human Resources, International Planning and Shipping and Receiving functions.

IDT's largest and newest facility, opened in 1990 in San Jose, California, is a multi-purpose 150,000 square foot, ultra modern technology development center. This facility houses a 25,000 square foot, combined Class 1 (a maximum of one particle per cubic foot of 0.2 micron or larger), sub-half-micron R&D fabrication facility and a wafer fabrication area. This fab supports both production volumes of IDT products, including some next generation SRAMs, and the R&D efforts of the technology development staff. Technology development efforts targeted for the center include advanced silicon processing and wafer fabrication techniques. A test area to support both production and research is located on-site. The building is also the new home of the FIFO and ECL product lines.

IDT's second largest facility is located in Salinas, California, about an hour away from Santa Clara. This 95,000 square foot facility, located on 14 acres, is the Static RAM Division and Specialty Memory product line. Constructed in 1985, this facility houses an ultra-modern 25,000 square foot high-volume wafer fabrication area measured at Class 2-to-3 (a maximum of 2 to 3 particles per cubic foot of 0.2 micron or larger) clean room conditions. Careful design and construction of this fabrication area created a clean room environment far beyond the 1985 average for U.S. fab areas. This made possible the production of large volumes of high-density submicron geometry, fast static RAMs. This facility also houses shipping areas for IDT's leadership family of CMOS static RAMs. This site will expand to accommodate a 250,000 square foot complex.

To extend these philosophies while maintaining strict control of our processes, IDT has an operational Assembly and Test facility located in Penang, Malaysia. This facility assembles product to USA standards, with all assemblies done under laminar flow conditions (Class 100) until the silicon is encased in its final packaging. All products in this facility are manufactured to the quality control requirements of MIL-STD-883.

All of IDT's facilities are aimed at increasing our manufacturing productivity to supply ever larger volumes of high-performance, cost-effective leadership CMOS products.

SUPERIOR QUALITY AND RELIABILITY

Maintaining the highest standards of quality in the industry on all products is the basis of Integrated Device Technology's manufacturing systems and procedures. From inception, quality and reliability are built into all of IDT's products. Quality is "designed in" at every stage of manufacturing – as opposed to being "tested-in" later – in order to ensure impeccable performance.

Dedicated commitment to fine workmanship, along with development of rigid controls throughout wafer fab, device assembly and electrical test, create inherently reliable products. Incoming materials are subjected to careful inspections. Quality monitors, or inspections, are performed throughout the manufacturing flow.

IDT military grade monolithic hermetic products are designed to meet or exceed the demanding Class B reliability levels of MIL-STD-883 and MIL-M-38510, as defined by Paragraph 1.2.1 of MIL-STD-883.

Product flow and test procedures for all monolithic hermetic military grade products are in accordance with the latest revision and notice of MIL-STD-883. State-of-the-art production techniques and computer-based test procedures are coupled with tight controls and inspections to ensure that products meet the requirements for 100% screening. Routine quality conformance lot testing is performed as defined in MIL-STD-883, Methods 5004 and 5005.

For IDT module products, screening of the fully assembled substrates is performed, in addition to the monolithic level screening, to assure package integrity and mechanical reliability. All modules receive 100% electrical tests (DC, functional and dynamic switching) to ensure compliance with the "subsystem" specifications.

By maintaining these high standards and rigid controls throughout every step of the manufacturing process, IDT ensures that commercial, industrial and military grade products consistently meet customer requirements for quality, reliability and performance.

SPECIAL PROGRAMS

Class S. IDT also has all manufacturing, screening and test capabilities in-house (except X-ray and some Group D tests) to perform complete Class S processing per MIL-STD-883 on all IDT products and has supplied Class S products on several programs.

Radiation Hardened. IDT has developed and supplied several levels of radiation hardened products for military/aerospace applications to perform at various levels of dose rate, total dose, single event upset (SEU), upset and latchup. IDT products maintain nearly their same high-performance levels built to these special process requirements. The company has in-house radiation testing capability used both in process development and testing of deliverable product. IDT also has a separate group within the company dedicated to supplying products for radiation hardened applications and to continue research and development of process and products to further improve radiation hardening capabilities.

GENERAL INFORMATION 1

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QUALITY AND RELIABILITY **3**

PACKAGE DIAGRAM OUTLINES 4

CEMOS STATIC RAMS WITH POWER DOWN 5

HIGH-SPEED BiCEMOS STATIC RAMS 6

APPLICATION AND TECHNICAL NOTES 7

QSP–QUALITY, SERVICE AND PERFORMANCE

Quality from the beginning, is the foundation for IDT's commitment to supply consistently high-quality products to our customers. IDT's quality commitment is embodied in its all pervasive Constant Quality Improvement (CQI) program. Everyone who influences the quality of the product–from the designer to the shipping clerk–is committed to constantly improving the product quality.

IDT'S FOCUS

"To make quantitative constant improvement in the quality of our actions that result in the supply of leadership products in conformance to the requirements of our customers."

IDT has dedicated its efforts to constant quantitative improvements in quality. The result, a supply of leadership products that conform to the requirements of our customers.

IDT'S PRODUCT ASSURANCE STRATEGY FOR CQI

Measurable standards are essential to the success of CQI. All the processes contributing to the final quality of the product need to be monitored, measured and improved upon through the use of statistical tools.

DEVELOPMENT
|
FAB
|
ASSEMBLY
|
TEST
|
SHIP

PRODUCT FLOW

Our customers receive the benefit of our optimized systems. Installed to enhance quality and reliability, these systems provide accurate and timely reporting on the effectiveness of manufacturing controls and the reliability and quality performance of IDT products and services.

SERVICE FLOW

ORDER ENTRY
|
PRODUCTION CONTROL
|
SHIPPING
|
CUSTOMER SUPPORT

These systems and controls concentrate on CQI by focusing on the following key elements:

Statistical Techniques
Using statistical techniques, including Statistical Process Control (SPC) to determine whether the product/ processes are under control.

Standardization
Implementing policies, procedures and measurement techniques that are common across different operational areas.

Documentation
Documenting and training in policies, procedures, measurement techniques and updating through characterization/ capability studies.

Productivity Improvement
Using constant improvement teams made up from employees at all levels of the organization.

Leadership
Focusing on quality as a key business parameter and strategic strength.

Total Employee Participation
Incorporating the CQI program into the IDT Corporate Culture.

Customer Service
Supporting the customer, as a partner, through performance review and pro-active problem solving.

People Excellence
Committing to growing, motivating and retaining people through training, goal setting, performance measurement and review.

PRODUCT FLOW

Product quality starts here. IDT has mechanisms and procedures in place that monitor and control the quality of our development activities. From the calibration of design capture libraries through process technology and product characterization that establish whether the performance, ratings and reliability criteria have been met. This includes failure analysis of parts that will improve the prototype product.

At the pre-production stage once again in-house qualification tests assure the quality and reliability of the product. All specifications and manufacturing flows are established and personnel trained before the product is placed into production.

Manufacturing

To make CQI during the manufacturing stage, control items are determined for major manufacturing conditions. Data is gathered and statistical techniques are used to control specific manufacturing processes that affect the quality of the product.

In-process and final inspections are fed back to earlier processes to improve product quality. All product is burned-in (where applicable) before 100% inspection of electrical characteristics takes place.

Products which pass final inspection are then subject to Quality Assurance and Reliability Tests. This data is used to improve manufacturing processes and provide reliability predictions of field applications.

Inventory and Shipping

Controls in shipping focus on ensuring parts are identified and packaged correctly. Care is also taken to see that the correct paperwork is present and the product being shipped was processed correctly.

SERVICE FLOW

Quality not only applies to the product but to the quality -of -service we give our customers. Service is also constantly improved.

Order Procedures

Checks are made at the order entry stage to ensure the correct processing of the Customer's product. After verification and data entry the Acknowledgements (sent to Customers) are again checked to ensure details are correct. As part of the CQI program, the results of these verifications are analyzed using statistical techniques and corrective actions are taken.

Production Control

Production Control (P.C.) is responsible for the flow and logistics of material as it moves through the manufacturing processes. The quality of the actions taken by P.C. greatly impinges on the quality of service the customer receives. Because many of our customers have implemented Just-in-Time (JIT) manufacturing practices, IDT as a supplier also has to adopt these same disciplines. As a result, employees receive extensive training and the performance level of key actions are kept under constant review. These key actions include:

Quotation response and accuracy.
Scheduling response and accuracy.
Response and accuracy of Expedites.
Inventory, management, and effectiveness.
On time delivery.

Customer Support

IDT has a worldwide network of sales offices and Technical Development Centers. These provide local customer support on business transactions, and in addition, support customers on applications information, technical services, benchmarking of hardware solutions, and demonstration of various Development Workstations.

The key to CQI is the timely resolution of defects and implementation of the corrective actions. This is no more important than when product failures are found by a customer.When failures are found at the customer's incoming inspection, in the production line, or the field application, the Quality Assurance group is the focal point for the investigation of the cause of failure and implementation of the corrective action. IDT constantly improves the level of support we give our customers by monitoring the response time to customers that have detected a product failure. Providing the customer with an analysis of the failure, including corrective actions and the statistical analysis of defects, brings CQI full circle–full support of our customers and their designs with high-quality products.

SUMMARY

In 1990, IDT made the commitment to *"Leadership through Quality, Service, and Performance Products".*

We believe by following that credo IDT and our cusotmers will be successful in the coming decade.With the implementation of the CQI strategy, we will satisfy our goal...

> *"Leadership through Quality, Service and Performance Products".*

IDT QUALITY CONFORMANCE PROGRAM

A COMMITMENT TO QUALITY

Integrated Device Technology's monolithic and modular assembly products are designed, manufactured and tested in accordance with the strict controls and procedures required by Military Standards. The documentation, design and manufacturing criteria of the Quality and Reliability Assurance Program were developed and are being maintained to the most current revisions of MIL-38510 as defined by paragraph 1.2.1 of MIL-STD-883 and MIL-STD-883 requirements.

Product flow and test procedures for all Class B *monolithic* hermetic Military Grade microcircuits are in full compliance with paragraph 1.2.1 of MIL-STD-883. State-of-the-art production techniques and computer-based test procedures are coupled with stringent controls and inspections to ensure that products meet the requirements for 100% screening and quality conformance tests as defined in MIL-STD-883, Methods 5004 and 5005.

Product flow and test procedures for all *plastic* and *commercial hermetic* products are in accordance with industry practices for producing highly reliable microcircuits to ensure that products meet the IDT requirements for 100% screening and quality conformance tests.

By maintaining these high standards and rigid controls throughout every step of the manufacturing process, IDT ensures that our products consistently meet customer requirements for quality, reliability and performance.

SUMMARY

Monolithic Hermetic Package Processing Flow(1)

Refer to the Monolithic Hermetic Package Processing Flow diagram. All test methods refer to MIL-STD-883 unless otherwise stated.

1. **Wafer Fabrication:** Humidity, temperature and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 100 levels or better.

   Wafers from each wafer fabrication area are subjected to Scanning Electron Microscope analysis on a periodic basis.

2. **Die-Sort Visual Inspection:** Wafers are cut and separated and the individual die are 100% visually inspected to strict IDT-defined internal criteria.

3. **Die Shear Monitor:** To ensure die attach integrity, product samples are routinely subjected to a shear strength test per Method 2019.

4. **Wire Bond Monitor:** Product samples are routinely subjected to a strength test per Method 2011, Condition D, to ensure the integrity of the lead bond process.

5. **Pre-Cap Visual:** Before the completed package is sealed, 100% of the product is visually inspected to Method 2010, Condition B criteria.

6. **Environmental Conditioning:** 100% of the sealed product is subjected to environmental stress tests. These thermal and mechanical tests are designed to eliminate units with marginal seal, die attach or lead bond integrity.

7. **Hermetic Testing:** 100% of the hermetic packages are subjected to fine and gross leak seal tests to eliminate marginally sealed units or units whose seals may have become defective as a result of environmental conditioning tests.

8. **Pre-Burn-In Electrical Test:** Each product is 100% electrically tested at an ambient temperature of +25°C to IDT data sheet or the customer specification.

9. **Burn-In:** 100% of the Military Grade product is burned-in under dynamic electrical conditions to the time and temperature requirements of Method 1015, Condition D. Except for the time, Commercial Grade product is burned-in as applicable to the same conditions as Military Grade devices.

10. **Post-Burn-In Electrical:** After burn-in, 100% of the Class B Military Grade product is electrically tested to IDT data sheet or customer specifications over the –55°C to +125°C temperature range. Commercial Grade products are sample tested to the applicable temperature extremes.

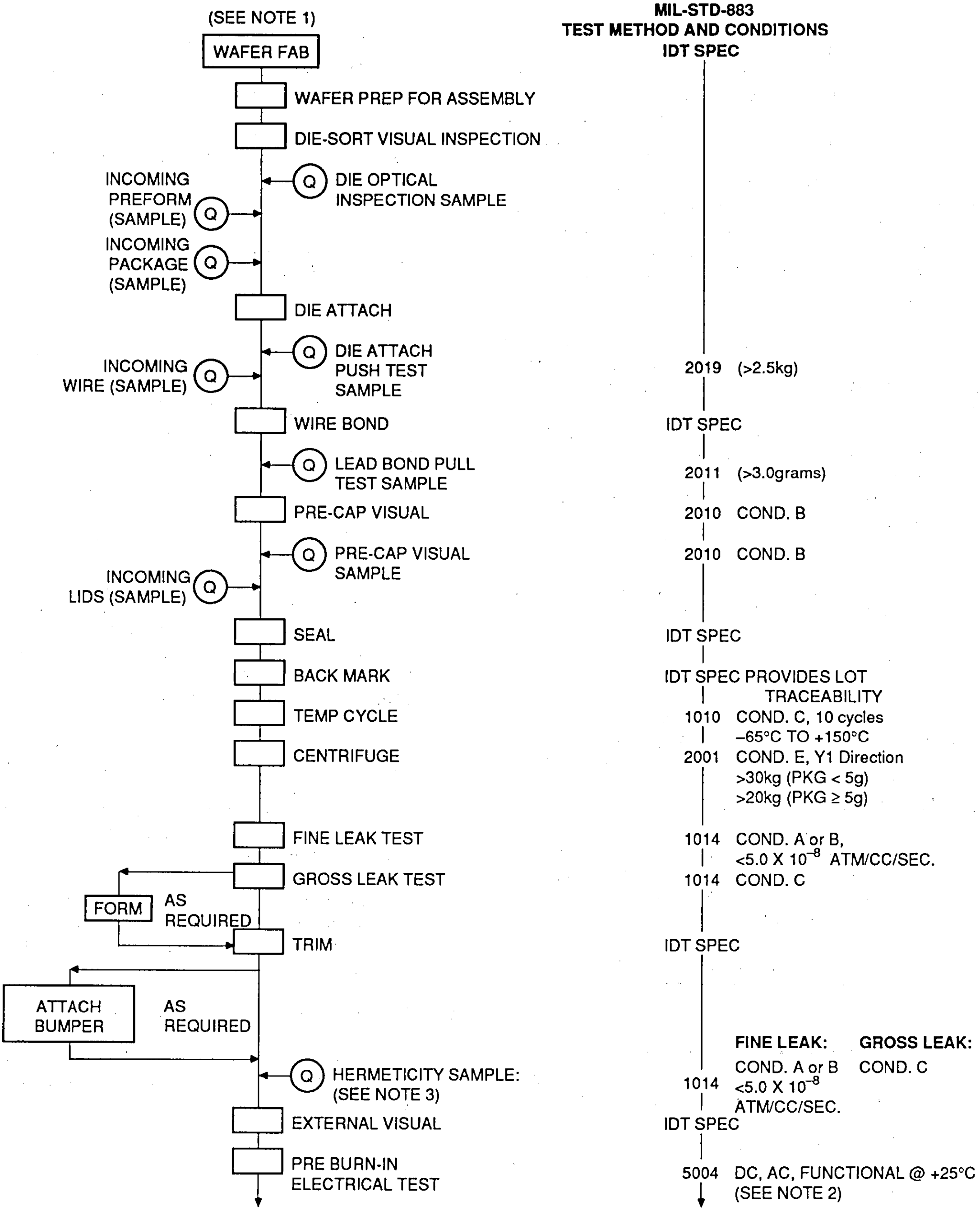
11. **Mark:** All product is marked with product type and lot code identifiers. MIL-STD-883 compliant Military Grade products are identified with the required compliant code letter.

12. **Quality Conformance Tests:** Samples of the Military Grade product which have been processed to the 100% screening tests of Method 5004 are routinely subjected to the quality conformance requirements of Method 5005.

NOTE:

1. For quality requirements beyond Class B levels such as SEM analysis, X-Ray inspection, Particle Impact Noise Reduction (PIND) test, Class S screening or other customer specified screening flows, please contact your Integrated Device Technology sales representative.

Monolithic Hermetic Package Processing Flow



SEE FINAL PROCESSING FLOW FOR REMAINDER OF OPERATIONS AND NOTES

2502 drw 01

SUMMARY

Monolithic Plastic Package Processing Flow

Refer to the Monolithic Plastic Package Processing Flow diagram. All test methods refer to MIL-STD-883 unless otherwise stated.

1. **Wafer Fabrication:** Humidity, temperature and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 100 levels or better.

   Topside silicon nitride passivation is all applied to all wafers for better moisture barrier characteristics.

   Wafers from each wafer fabrication area are subjected to Scanning Electron Microscope analysis on a periodic basis.

2. **Die-Sort Visual Inspection:** Wafers are 100% visually inspected to strict IDT defined internal criteria.

3. **Die Push Test:** To ensure die attach integrity, product samples are routinely subjected to die push tests.

4. **Wire Bond Monitor:** Product samples are routinely subjected to wire bond pull tests to ensure the integrity of the lead bond process.

5. **Pre-Cap Visual:** Before the package is molded, 100% of the product is visually inspected to criteria patterned after MIL-STD-883, Method 2010, Condition B.

6. **Post Mold Cure:** Plastic encapsulated devices are baked to ensure an optimum plastic seal so as to enhance moisture barrier characteristics.

7. **Pre-Burn-In Electrical:** Each product is 100% electrically tested at an ambient temperature of +25°C to IDT data sheet or the customer specification.

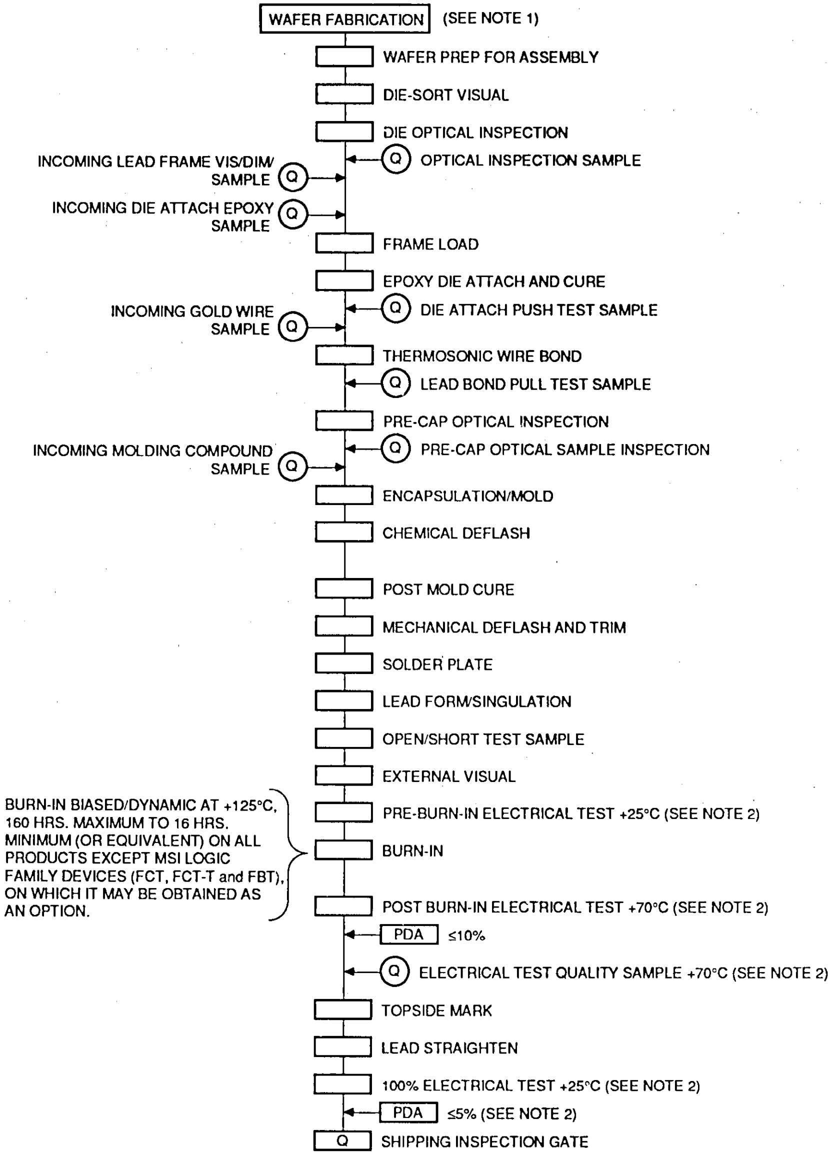
8. **Burn-In:** Except for MSI Logic family devices where it may be obtained as an option, all Commercial Grade plastic package products are burned-in 16 hours at +125°C (or equivalent), utilizing the same burn-in conditions as the Military Grade product.

9. **Post-Burn-In Electrical:** After burn-in, 100% of the plastic product is electrically tested to IDT data sheet or customer specifications at the maximum temperature extreme. The minimum temperature extreme is tested periodically on an audit basis.

10. **Mark:** All product is marked with product type and lot code identifiers.

11. **Quality Conformance Inspection:** Samples of the plastic product which have been processed to the 100% screening requirements are subjected to the Periodic Quality Conformance Inspection Program. Where indicated, the test methods are patterned after MIL-STD-883 criteria.

Monolithic Plastic Package Processing Flow



NOTE:
1. All screens are 100% unless otherwise noted.
2. All electrical test programs are per the applicable IDT test specification.
3. IDT performs a 100% electrical test at +25°C with a 5% PDA limit at this point.
4. Ⓠ = Quality sample inspection.

2502 drw 02

Monolithic Hermetic Package Final Processing Flow

Operation	MIL-STD-883 Test Method	Military Compliant Class B	Commercial	
			Military Temp. Range	Commercial Temp. Range
Burn-In	1015/D at +125°C Min. or Equivalent	100% 160 Hours	100% 16 to 160 Hours	100% 16to160 Hours
Post Burn-In Electrical: Static (DC), Functional and Switching (AC)[2]	IDT Spec.	100% +25, -55 and +125°C	100% +125°C	100% +70°C
Percent Defective Allowed (PDA)[4]	5004 or IDT Spec.	5%	10%	10%
Group A Electrical: Static (DC), Functional and Switching (AC)[2]	5005 and IDT Spec.	Sample -55 and +125°C	Sample +125°C	Sample +70°C
Mark/Lead Straighten	IDT Spec.	100%	100%	100%
+25°C Electrical[2]	IDT Spec.	100%[5]	100%	100%
Final Visual/Pack	IDT Spec.	100%	100%	100%
Quality Conformance Inspection	5005 (Group B, C, D)	Yes	—	—
Quality Shipping Inspection (Visual/Plant Clearance)	IDT Spec.	Sample	Sample	Sample

2505 tbl 01

NOTES:

1. All screens are 100% unless otherwise noted.
2. All electrical test programs are per the applicable IDT test specification.
3. This hermeticity sample is performed after all lead finish operations.
4. If a lot fails the 5% PDA but is ≤10%, the lot may be resubmitted to burn-in one time only to the same time and temperature conditions as first submission. The subsequent post burn-in electrical test at +25°C will be performed to a PDA of 3%.
5. IDT performs a 100% electrical test at +25°C with a 2% PDA limit at this point to satisfy group A requirements, and considers this to be equivalent to the group A requirement of an LTPD of 2, with an accept number of 0. If a lot fails the 2% PDA limit, it may be rescreened one time only to a tightened PDA limit of 1.5%.
6. Ⓠ = Quality sample inspection.

RADIATION TOLERANT/ENHANCED/HARDENED PRODUCTS FOR RADIATION ENVIRONMENTS

INTRODUCTION

The need for high-performance CMOS integrated circuits in military and space systems is more critical today than ever before. The low power dissipation that is achieved using CMOS technology, along with the high complexity and density levels, makes CMOS the nearly ideal component for all types of applications.

Systems designed for military or space applications are intended for environments where high levels of radiation may be encountered. The implication of a device failure within a military or space system clearly is critical. IDT has made a significant contribution toward providing reliable radiation-tolerant systems by offering integrated circuits with enhanced radiation tolerance. Radiation environments, IDT process enhancements and device tolerance levels achieved are described below.

THE RADIATION ENVIRONMENT

There are four different types of radiation environments that are of concern to builders of military and space systems. These environments and their effects on the device operation, summarized in Figure 1, are as follows:

Total Dose Accumulation refers to the total amount of accumulated gamma rays experienced by the devices in the system, and is measured in RADS (SI) for radiation units experienced at the silicon level. The physical effect of gamma rays on semiconductor devices is to cause threshold shifts (Vt shifts) of both the active transistors as well as the parasitic field transistors. Threshold voltages decrease as total dose is accumulated; at some point, the device will begin to exhibit parametric failures as the input/output and supply currents increase. At higher radiation accumulation levels, functional failures occur. In memory circuits, however, functional failures due to memory cell failure often occur first.

Burst Radiation or Dose Rate refers to the amount of radiation, usually photons or electrons, experienced by the devices in the system due to a pulse event, and is measured in RADS (SI) per second. The effect of a high dose rate or burst of radiation on CMOS integrated circuits is to cause temporary upset of logic states and/or CMOS latch-up. Latch-up can cause permanent damage to the device.

Single Event Upset (SEU) is a transient logic state change caused by high-energy ions, such as energetic cosmic rays, striking the integrated circuits. As the ion passes through the silicon, charge is either created through ionization or direct nuclear collision. If collected by a circuit node, this excess charge can cause a change in logic state of the circuit. Dynamic nodes that are not actively held at a particular logic state (dynamic RAM cells for example) are the most susceptible. These upsets are transient, but can cause system failures known as "soft errors."

Neutron Irradiation will cause structural damage to the silicon lattice which may lead to device leakage and, ultimately, functional failure.

Radiation Category	Primary Particle	Source	Effect
Total Dose	Gamma	Space or Nuclear Event	Permanent
Dose Rate	Photons	Nuclear Event	Temporary Upset of Logic State or Latch-up
SEU	Cosmic Rays	Space	Temporary Upset of Logic State
Neutron	Neutrons	Nuclear Event	Device Leakage Due to Silicon Lattice Damage

2510 drw 01

Figure 1.

DEVICE ENHANCEMENTS

Of the four radiation environments above, IDT has taken considerable data on the first two, Total Dose Accumulation and Dose Rate. IDT has developed a process that significantly improves the radiation tolerance of its devices within these environments. Prevention of SEU failures is usually accomplished by system-level considerations, such as Error Detection and Correction (EDC) circuitry, since the occurrence of SEUs is not particularly dependent on process technology. Through IDT's customer contracts, SEU has been gathered on some devices. Little is yet known about the effects of neutron-induced damage. For more information on SEU testing, contact IDT's Radiation Hardened Product Group.

Enhancements to IDT's standard process are used to create radiation enhanced and tolerant processes. Field and gate oxides are "hardened" to make the device less susceptible to radiation damage by modifying the process architecture to allow lower temperature processing. Device implants and Vts adjustments allow more Vt margin. In addition to process changes, IDT's radiation enhanced process utilizes epitaxial substrate material. The use of epi substrate material provides a lower substrate resistance environment to create latch-up free CMOS structures.

RADIATION HARDNESS CATEGORIES

Radiation Enhanced ('RE) or Radiation Tolerant ('RT) versions of IDT products follow IDT's military product data sheets whenever possible (consult factory). IDT's Total Dose Test plan exposes a sample of die on a wafer to a particular Total Dose level via ARACOR X-Ray radiation. This Total Dose Test plan qualifies each 'RE or 'RT wafer to a Total Dose level. Only wafers with sampled die that pass Total Dose level tests are assembled and used for orders (consult factory for more details on Total Dose sample testing). With regard to Total Dose testing, clarifications/exceptions to MIL-STD-883, Methods 5005 and 1019 are required. Consult factory for more details.

The 'RE and 'RT process enhancements enable IDT to offer integrated circuits with varying grades of radiation tolerance or radiation "hardness".

- Radiation Enhanced process uses Epi wafers and is able to provide devices that can be Total Dose qualified to 10K RADs (Si) or greater by IDT's ARACOR X-Ray Total Dose sample die test plan (Total Dose levels require negotiation, consult factory for more details).
- Radiation Tolerant product uses standard wafer/process material that is qualified to 10K RADs (Si) Total Dose by IDT's ARACOR X-Ray Total Dose sample die test plan.

Integrated Device Technology can provide Radiation Tolerant/Enhanced versions of all product types (some speed grades may not be available as 'RE).

Please contact your IDT sales representative or factory marketing to determine availability and price of any IDT product processed in accordance with one of these levels of radiation hardness.

CONCLUSION

There has been widespread interest within the military and space community in IDT's CMOS product line for its radiation hardness levels, as well as its high-performance and low power dissipation. To serve this growing need for CMOS circuits that must operate in a radiation environment, IDT has created a separate group within the company to concentrate on supplying products for these applications.Continuing research and development of process and products, including the use of in-house radiation testing capability, will allow Integrated Device Technology to offer continuously increasing levels of radiation-tolerant solutions.

THERMAL PERFORMANCE CALCULATIONS FOR IDT'S PACKAGES

Since most of the electrical energy consumed by microelectronic devices eventually appears as heat, poor thermal performance of the device or lack of management of this thermal energy can cause a variety of deleterious effects. This device temperature increase can exhibit itself as one of the key variables in establishing device performance and long term reliability; on the other hand, effective dissipation of internally generated thermal energy can, if properly managed, reduce the deleterious effects and improve component reliability.

A few key benefits of IDT's enhanced CEMOS™ process are: low power dissipation, high speed, increased levels of integration, wider operating temperature ranges and lower quiescent power dissipation. Because the reliability of an integrated circuit is largely dependent on the maximum temperature the device attains during operation, and as the junction stability declines with increases in junction temperature (T_J), it becomes increasingly important to maintain a low (T_J).

CMOS devices stabilize more quickly and at greatly lower temperature than bipolar devices under normal operation. The accelerated aging of an integrated circuit can be expressed as an exponential function of the junction temperature as:

$$t_A = t_O \exp\left[\frac{E_a}{k}\left(\frac{1}{T_O} - \frac{1}{T_J}\right)\right]$$

where

t_A = lifetime at elevated junction (T_J) temperature
t_O = normal lifetime at normal junction (T_O) temperature
E_a = activation energy (ev)
k = Boltzmann's constant (8.617×10^{-5}ev/k)

i.e. the lifetime of a device could be decreased by a factor of 2 for every 10°C increase temperature.

To minimize the deleterious effects associated with this potential increase, IDT has:

1. Optimized our proprietary low-power CEMOS fabrication process to ensure the active junction temperature rise is minimal.
2. Selected only packaging materials that optimize heat dissipation, which encourages a cooler running device.
3. Physically designed all package components to enhance the inherent material properties and to take full advantage of heat transfer and radiation due to case geometries.
4. Tightly controlled the assembly procedures to meet or exceed the stringent criteria of MIL-STD-883_ to ensure maximum heat transfer between die and packaging materials.

The following figures graphically illustrate the thermal values of IDT's current package families. Each envelop (shaded area) depicts a typical spread of values due to the influence of a number of factors which include: circuit size, package cavity size and die attach integrity. The following range of values are to be used as a comprehensive characterization of the major variables rather than single point of reference.

When calculating junction temperature (T_J), it is necessary to know the thermal resistance of the package (θ_{JA}) as measured in "degree celsius per watt". With the accompanying data, the following equation can be used to establish thermal performance, enhance device reliability and ultimately provide you, the user, with a continuing series of high-speed, low-power CMOS solutions to your system design needs.

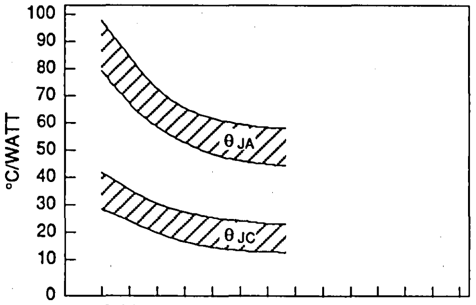
$$\theta_{JA} = [T_J - T_A]/P$$
$$T_J = T_A + P[\theta_{JA}] = T_A + P[\theta_{JC} + \theta_{CA}]$$

where

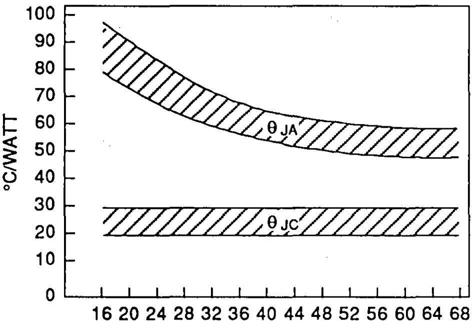
$$\theta_{JC} = \frac{T_J - T_C}{P} \qquad \theta_{CA} = \frac{T_C - T_A}{P}$$

θ = Thermal resistance
J = Junction
P = Operational power of device (dissipated)
T_A = Ambient temperature in degree celsius
T_J = Temperature of the junction
T_C = Temperature of case/package
θ_{CA} = Case to Ambient, thermal resistance—usually a measure of the heat dissipation due to natural or forced convection, radiation and mounting techniques.
θ_{JC} = Junction to Case, thermal resistance—usually measured with reference to the temperature at a specific point on the package (case) surface. (Dependent on the package material properties and package geometry.)
θ_{JA} = Junction to Ambient, thermal resistance—usually measured with respect to the temperature of a specified volume of still air. (Dependent on θ_{JC} + θ_{JA} which includes the influence of area and environmental condition.)

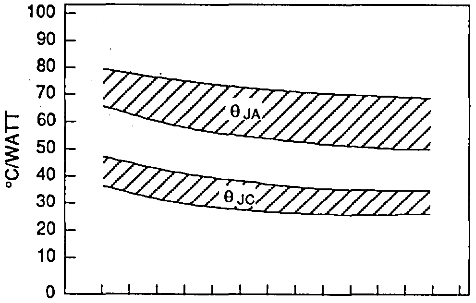
Ref. MIL-STD-883C, Method 1012.1
JEDEC ENG. Bulletin No. 20, January 1975
1986 Semi. Std., Vol. 4, Test Methods G30–86, G32–86.



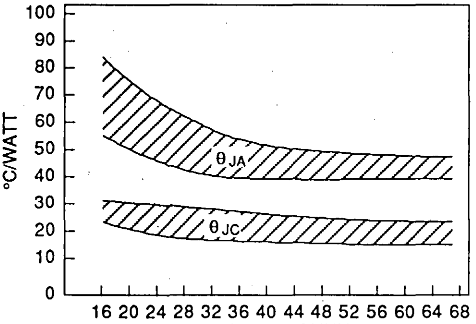
Thermal Resistance of Ceramic DIP Packages



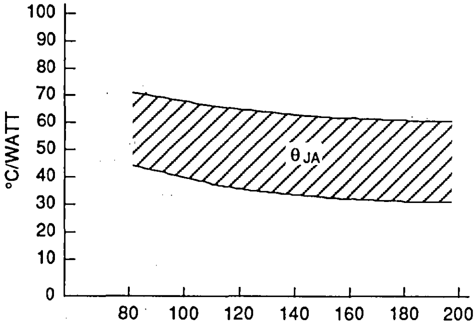
Thermal Resistance of PLCC/SOIC Packages



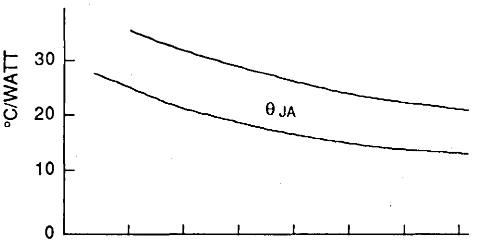
Thermal Resistance of Plastic DIP Packages



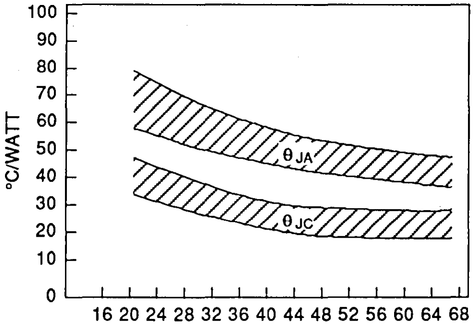
Thermal Resistance of Ceramic Sidebraze Packages



Thermal Resistance of PPGA Packages



PGA Thermal Resistance



Thermal Resistance of Ceramic Leadless Chip Carrier (LCC) Packages

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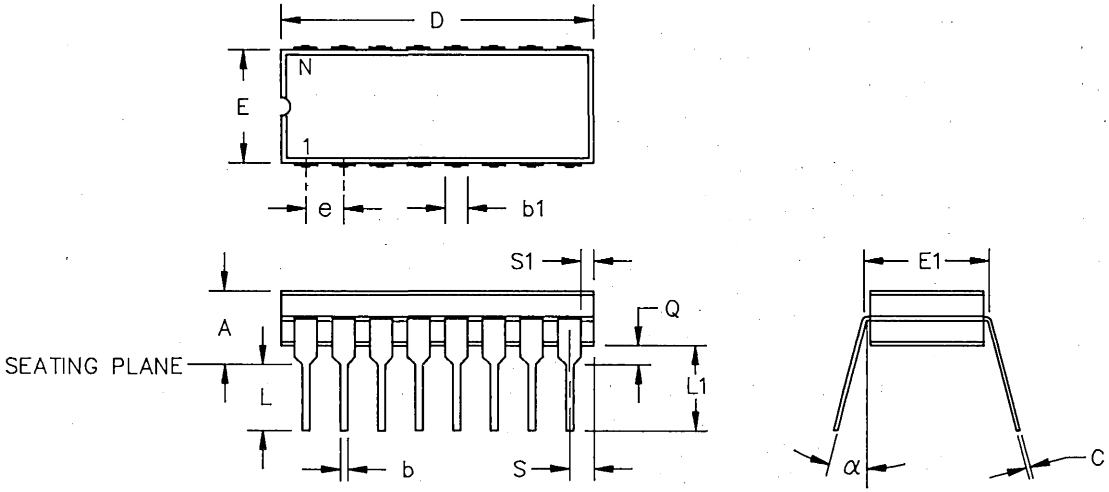
PACKAGE DIAGRAM OUTLINE INDEX

MONOLITHIC PACKAGE DIAGRAM OUTLINES

MONOLITHIC PACKAGE DIAGRAM OUTLINES (Continued)

MONOLITHIC PACKAGE DIAGRAM OUTLINES (Continued)

DUAL IN–LINE PACKAGES



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. THE MINIMUM LIMIT FOR DIMENSION b1 MAY BE .023 FOR CORNER LEADS.

16–28 LEAD CERDIP (300 MIL)

DWG #	D16–1		D18–1		D20–1		D22–1		D24–1		D28–3	
# OF LDS (N)	16		18		20		22		24		28	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.140	.200	.140	.200	.140	.200	.140	.200	.140	.200	.140	.200
b	.015	.021	.015	.021	.015	.021	.015	.021	.015	.021	.015	.021
b1	.038	.060	.038	.060	.038	.060	.045	.060	.045	.065	.045	.065
C	.009	.012	.009	.012	.009	.012	.009	.012	.009	.014	.009	.014
D	.750	.830	.880	.930	.935	1.060	1.050	1.080	1.240	1.280	1.440	1.490
E	.285	.310	.285	.310	.285	.310	.285	.310	.285	.310	.285	.310
E1	.290	.320	.290	.320	.290	.320	.300	.320	.300	.320	.300	.320
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC	
L	.125	.175	.125	.175	.125	.175	.125	.175	.125	.175	.125	.175
L1	.150	–	.150	–	.150	–	.150	–	.150	–	.150	–
Q	.015	.055	.015	.055	.015	.060	.015	.060	.015	.060	.015	.060
S	.020	.080	.020	.080	.020	.080	.020	.080	.030	.080	.030	.080
S1	.005	–	.005	–	.005	–	.005	–	.005	–	.005	–
α	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°

DUAL IN-LINE PACKAGES (Continued)

24-40 LEAD CERDIP (600 MIL)

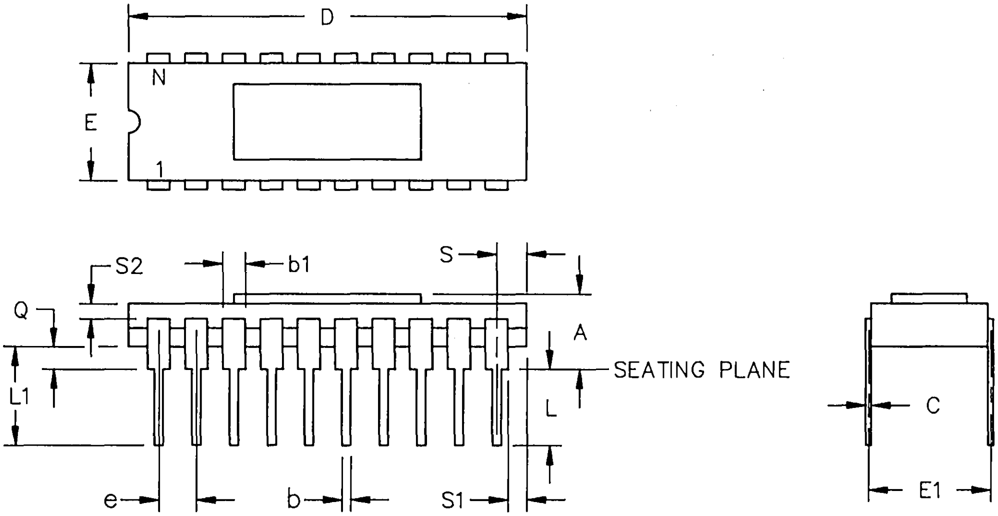
DWG #	D24-2		D28-1		D40-1	
# OF LDS (N)	24		28		40	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.190	.090	.200	.160	.220
b	.014	.023	.014	.023	.014	.023
b1	.038	.060	.038	.065	.038	.065
C	.008	.012	.008	.014	.008	.014
D	1.230	1.290	1.440	1.490	2.020	2.070
E	.500	.610	.510	.545	.510	.545
E1	.590	.620	.590	.620	.590	.620
e	.100 BSC		.100 BSC		.100 BSC	
L	.125	.200	.125	.200	.125	.200
L1	.150	–	.150	–	.150	–
Q	.015	.060	.020	.060	.020	.060
S	.030	.080	.030	.080	.030	.080
S1	.005	–	.005	–	.005	–
α	0°	15°	0°	15°	0°	15°

28-40 LEAD CERDIP (WIDE BODY)

DWG #	D28-2		D32-1		D40-2	
# OF LDS (N)	28		32		40	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.200	.120	.210	.160	.220
b	.014	.023	.014	.023	.014	.023
b1	.038	.065	.038	.065	.038	.065
C	.008	.014	.008	.014	.008	.014
D	1.440	1.490	1.625	1.675	2.020	2.070
E	.570	.600	.570	.600	.570	.600
E1	.590	.620	.590	.620	.590	.620
e	.100 BSC		.100 BSC		.100 BSC	
L	.125	.200	.125	.200	.125	.200
L1	.150	–	.150	–	.150	–
Q	.020	.060	.020	.060	.020	.060
S	.030	.080	.030	.080	.030	.080
S1	.005	–	.005	–	.005	–
α	0°	15°	0°	15°	0°	15°

DUAL IN–LINE PACKAGES (Continued)

20–32 LEAD SIDE BRAZE (300 MIL)

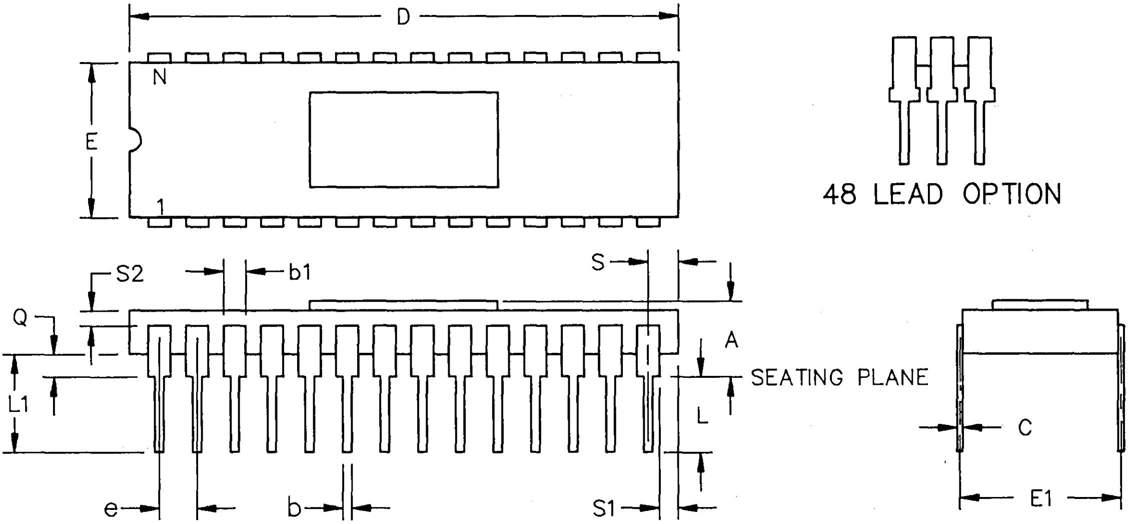


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	C20–1		C22–1		C24–1		C28–1		C32–3	
# OF LDS (N)	20		22		24		28		32	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.200	.100	.200	.090	.200	.090	.200	.090	.200
b	.014	.023	.014	.023	.015	.023	.014	.023	.014	.023
b1	.040	.060	.040	.060	.040	.060	.040	.060	.040	.060
C	.008	.015	.008	.015	.008	.015	.008	.015	.008	.014
D	.970	1.060	1.040	1.120	1.180	1.230	1.380	1.420	1.580	1.640
E	.260	.310	.260	.310	.220	.310	.220	.310	.280	.310
E1	.290	.320	.290	.320	.290	.320	.290	.320	.290	.320
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC	
L	.125	.200	.125	.200	.125	.200	.125	.200	.100	.175
L1	.150	–	.150	–	.150	–	.150	–	.150	–
Q	.015	.060	.015	.060	.015	.060	.015	.060	.030	.060
S	.030	.065	.030	.065	.030	.065	.030	.065	.030	.065
S1	.005	–	.005	–	.005	–	.005	–	.005	–
S2	.005	–	.005	–	.005	–	.005	–	.005	–

DUAL IN-LINE PACKAGES (Continued)

28-48 LEAD SIDE BRAZE (400 MIL)

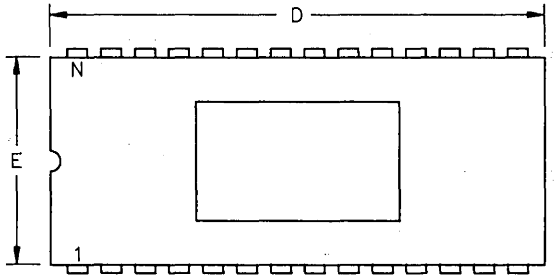


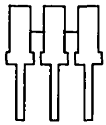
NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

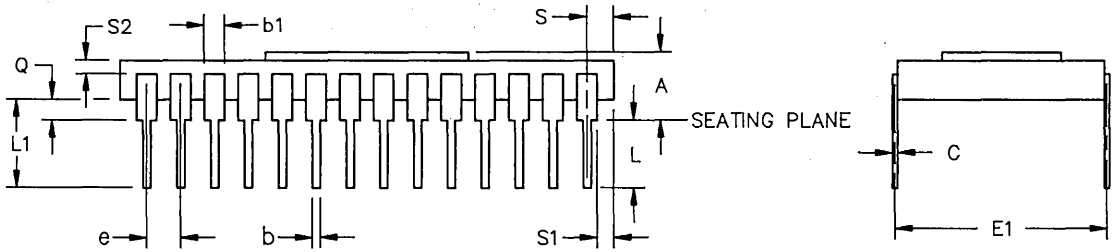
DWG #	C28-2		C32-2		C48-1	
# OF LDS (N)	28		32		48	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.200	.090	.200	.085	.190
b	.014	.023	.014	.023	.014	.023
b1	.040	.060	.040	.060	.040	.060
C	.008	.014	.008	.014	.008	.014
D	1.380	1.420	1.580	1.640	1.690	1.730
E	.380	.420	.380	.410	.380	.410
E1	.390	.420	.390	.420	.390	.420
e	.100 BSC		.100 BSC		.070 BSC	
L	.100	.175	.100	.175	.125	.175
L1	.150	–	.150	–	.150	–
Q	.030	.060	.030	.060	.020	.070
S	.030	.065	.030	.065	.030	.065
S1	.005	–	.005	–	.005	–
S2	.005	–	.005	–	.005	–

DUAL IN–LINE PACKAGES (Continued)

24–68 LEAD SIDE BRAZE (600 MIL)




68 LEAD OPTION

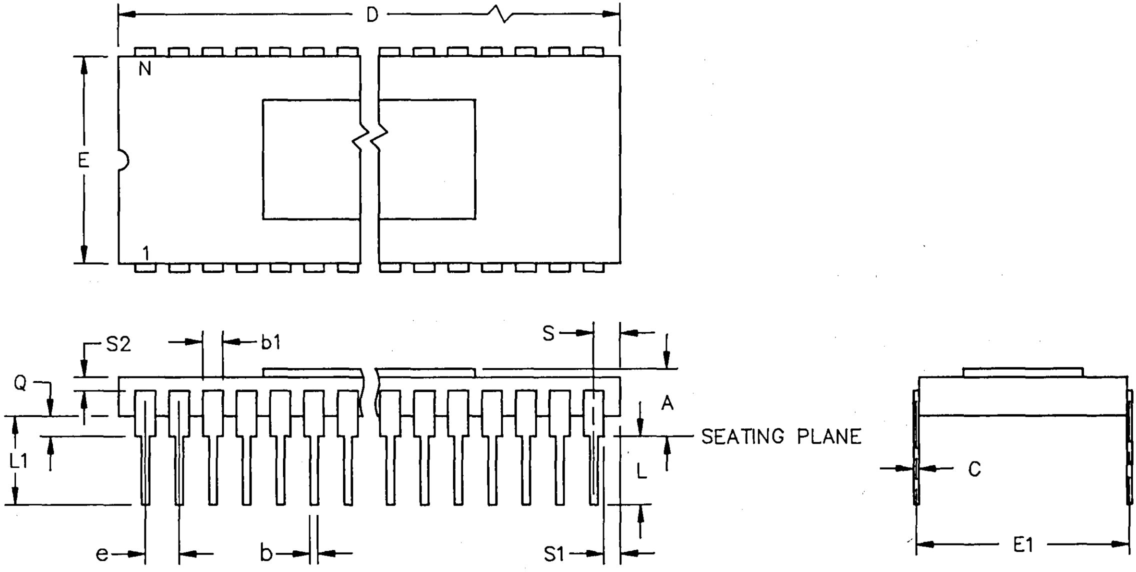


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	C24–2		C28–3		C32–1		C40–1		C48–2		C68–1	
# OF LDS (N)	24		28		32		40		48		68	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.190	.085	.190	.100	.190	.085	.190	.100	.190	.085	.190
b	.015	.023	.015	.022	.015	.023	.015	.023	.015	.023	.015	.023
b1	.040	.060	.038	.060	.040	.060	.038	.060	.040	.060	.040	.060
C	.008	.012	.008	.012	.008	.014	.008	.012	.008	.012	.008	.012
D	1.180	1.220	1.380	1.430	1.580	1.640	1.980	2.030	2.370	2.430	2.380	2.440
E	.575	.610	.580	.610	.580	.610	.580	.610	.550	.610	.580	.610
E1	.595	.620	.595	.620	.590	.620	.595	.620	.595	.620	.590	.620
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC		.070 BSC	
L	.125	.175	.125	.175	.100	.175	.125	.175	.125	.175	.125	.175
L1	.150	–	.150	–	.150	–	.150	–	.150	–	.150	–
Q	.020	.060	.020	.065	.020	.060	.020	.060	.020	.060	.020	.070
S	.030	.065	.030	.065	.030	.065	.030	.065	.030	.065	.030	.065
S1	.005	–	.005	–	.005	–	.005	–	.005	–	.005	–
S2	.005	–	.005	–	.005	–	.005	–	.005	–	.005	–

DUAL IN-LINE PACKAGES (Continued)

64 LEAD SIDE BRAZE (900 MIL)

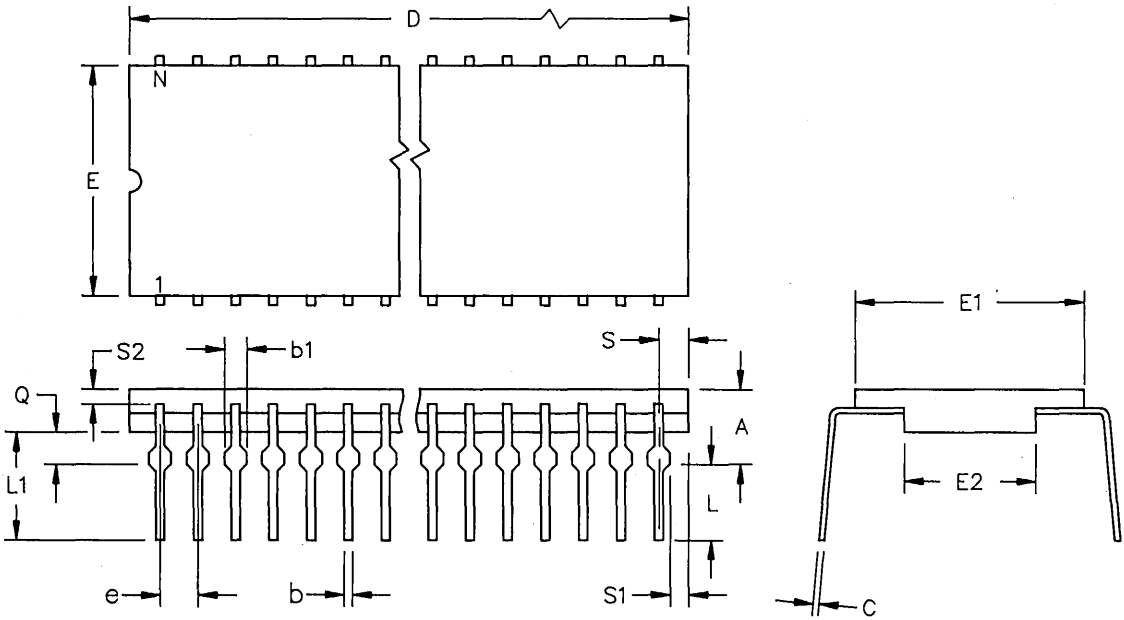


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	C64-1	
# OF LDS (N)	64	
SYMBOL	MIN	MAX
A	.110	.190
b	.014	.023
b1	.040	.060
C	.008	.015
D	3.160	3.240
E	.884	.915
E1	.890	.920
e	.100 BSC	
L	.125	.200
L1	.150	–
Q	.015	.070
S	.030	.065
S1	.005	–
S2	.005	–

DUAL IN-LINE PACKAGES (Continued)

64 LEAD TOP BRAZE (900 MIL)

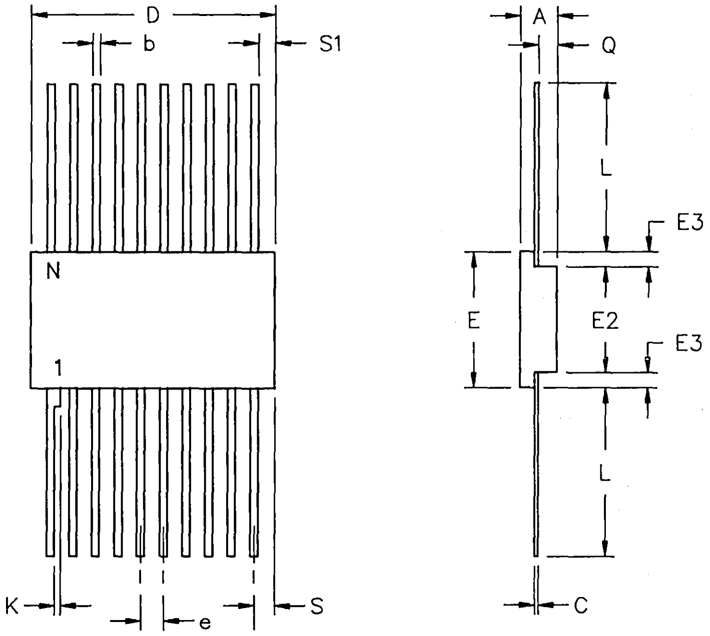


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	C64–2	
# OF LDS (N)	64	
SYMBOL	MIN	MAX
A	.120	.180
b	.015	.021
b1	.040	.060
C	.009	.012
D	3.170	3.240
E	.790	.810
E1	.880	.815
E2	.640	.660
e	.100 BSC	
L	.125	.160
L1	.150	–
Q	.020	.100
S	.030	.065
S1	.005	–
S2	.005	–

FLATPACKS

20–28 LEAD FLATPACK

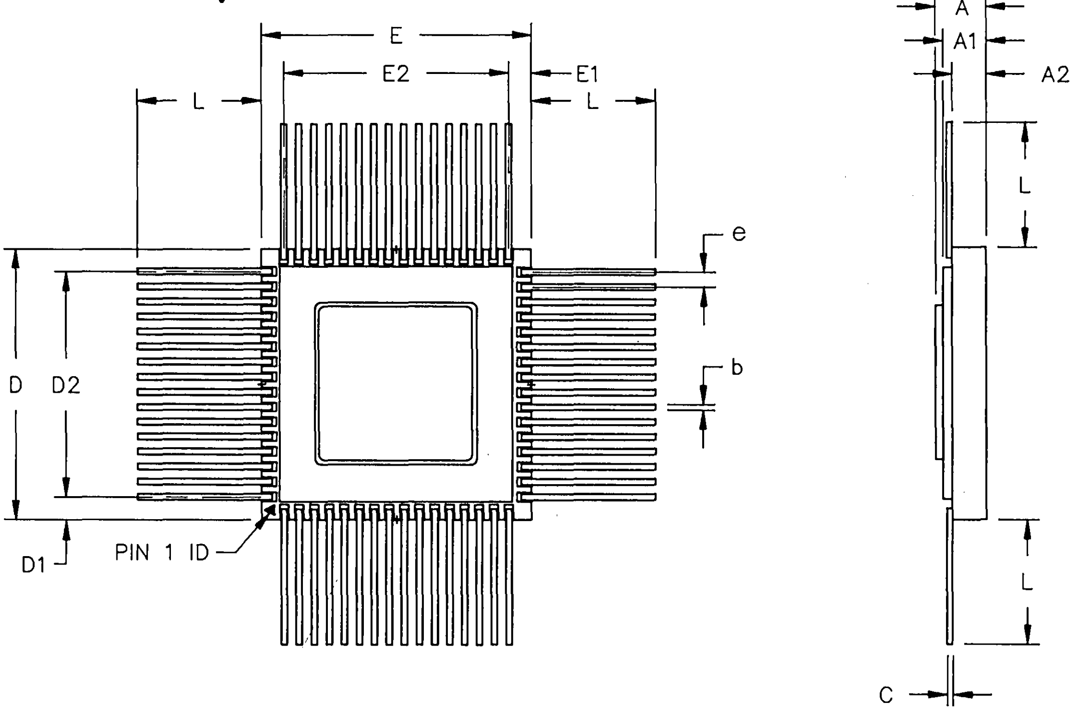


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	F20–1		F20–2		F24–1		F28–1		F28–2	
# OF LDS (N)	20		20 (.295 BODY)		24		28		28	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.045	.092	.045	.092	.045	.090	.045	.090	.045	.115
b	.015	.019	.015	.019	.015	.019	.015	.019	.015	.019
C	.003	.006	.003	.006	.003	.006	.004	.007	.003	.007
D	–	.540	–	.540	–	.640	.710	.740	.710	.740
E	.340	.360	.245	.303	.360	.420	.480	.520	.480	.520
E2	.130	–	.130	–	.180	–	.180	–	.180	–
E3	.030	–	.030	–	.030	–	.040	–	.040	–
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
K	.006	.015	.008	.015	–	–	–	–	–	–
L	.250	.370	.250	.370	.250	.370	.250	.370	.250	.370
Q	.010	.040	.010	.040	.010	.040	.010	.045	.026	.045
S	–	.045	–	.045	–	.045	–	.045	–	.045
S1	.000	–	.005	–	.005	–	.005	–	.005	–

FLATPACKS (Continued)

48–64 LEAD QUAD FLATPACK

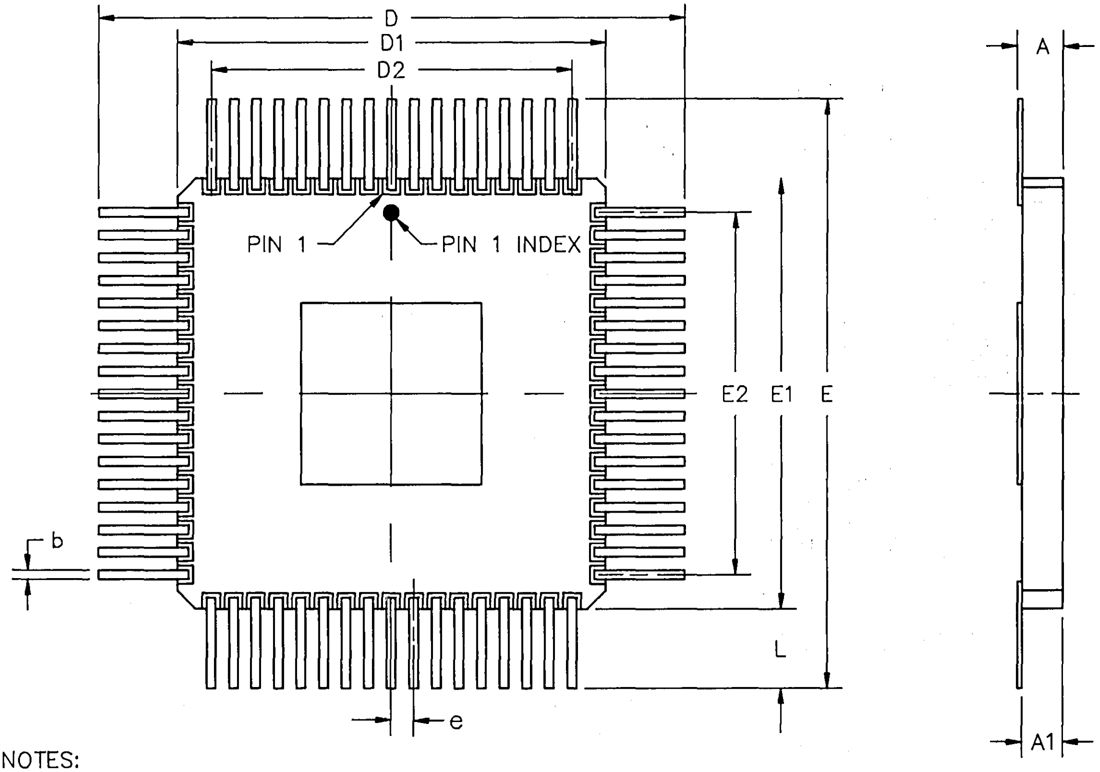


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	F48–1		F64–1	
# OF LDS (N)	48		64	
SYMBOL	MIN	MAX	MIN	MAX
A	.089	.108	.070	.090
A1	.079	.096	.060	.078
A2	.058	.073	.030	.045
b	.018	.022	.016	.020
C	.008	.010	.009	.012
D/E	–	.750	.885	.915
D1/E1	.100 REF		.075 REF	
D2/E2	.550 BSC		.750 BSC	
e	.050 BSC		.050 BSC	
L	.350	.450	.350	.450
ND/NE	12		16	

FLATPACKS (Continued)

68 LEAD QUAD FLATPACK

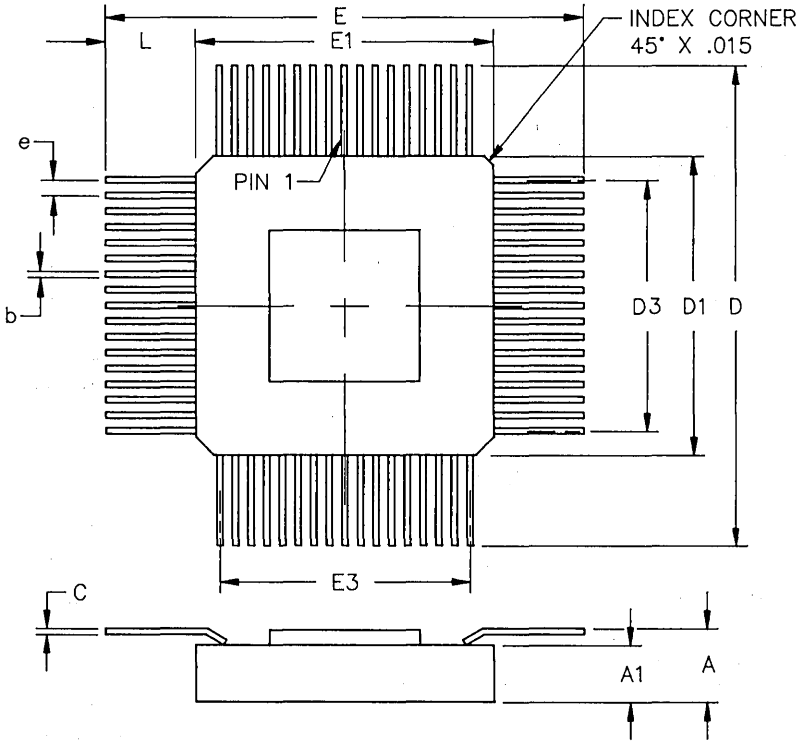


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	F68–1	
# OF LDS (N)	68	
SYMBOL	MIN	MAX
A	.080	.145
A1	.070	.090
b	.014	.021
C	.008	.012
D/E	1.640	1.870
D1/E1	.926	.970
D2/E2	.800 BSC	
e	.050 BSC	
L	.350	.450
ND/NE	17	

FLATPACKS (Continued)

68 LEAD QUAD FLATPACK (STRAIGHT LEADS)

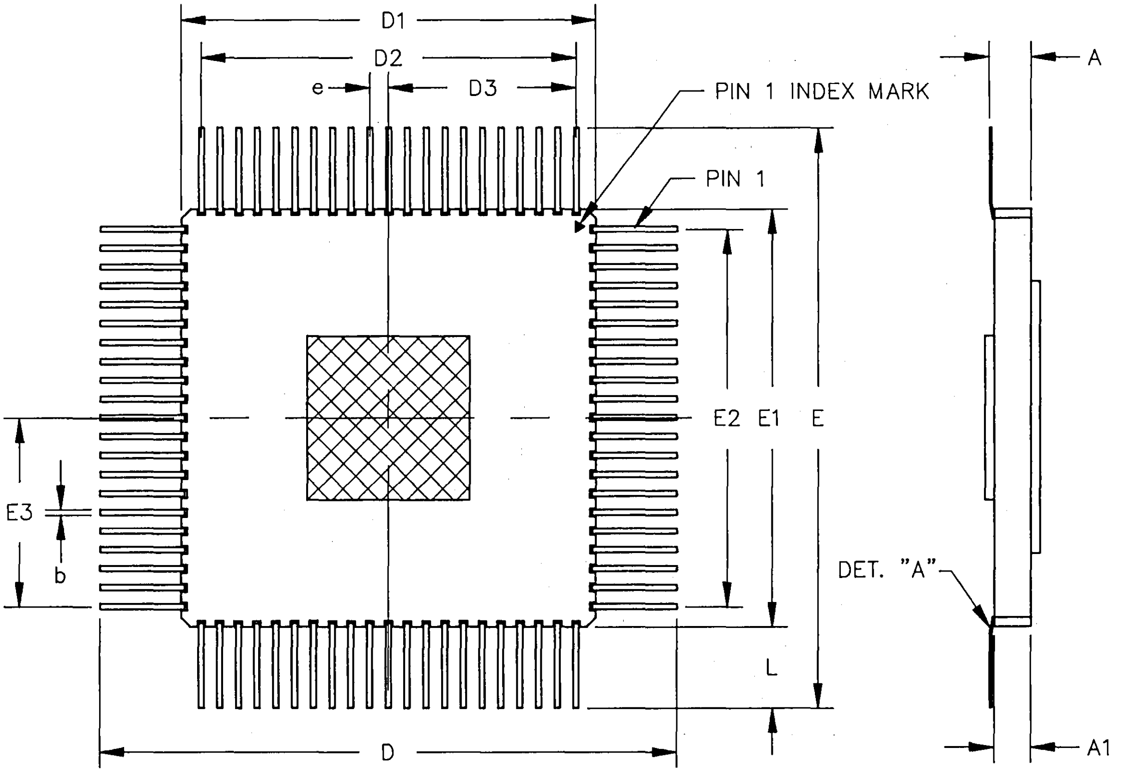


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	F68–2	
# OF LDS (N)	68	
SYMBOL	MIN	MAX
A	.064	.084
A1	.054	.070
b	.008	.013
C	.0045	.008
D/E	.860	1.100
D1/E1	.460	.500
D2/E2	.400 REF	
e	.025 BSC	
L	.200	.300
ND/NE	17	

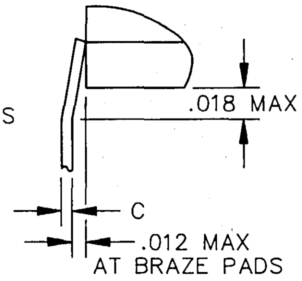
FLATPACKS (Continued)

84 LEAD QUAD FLATPACK (CAVITY DOWN)



DWG #	F84-1	
# OF LDS (N)	84	
SYMBOL	MIN	MAX
A	–	.140
A1	–	.105
b	.014	.020
C	.007	.013
D/E	1.485	1.615
D1/E1	1.130	1.170
D2/E2	1.000 BSC	
D3/E3	.500 BSC	
e	.050 BSC	
L	.350	.450
ND/NE	21	

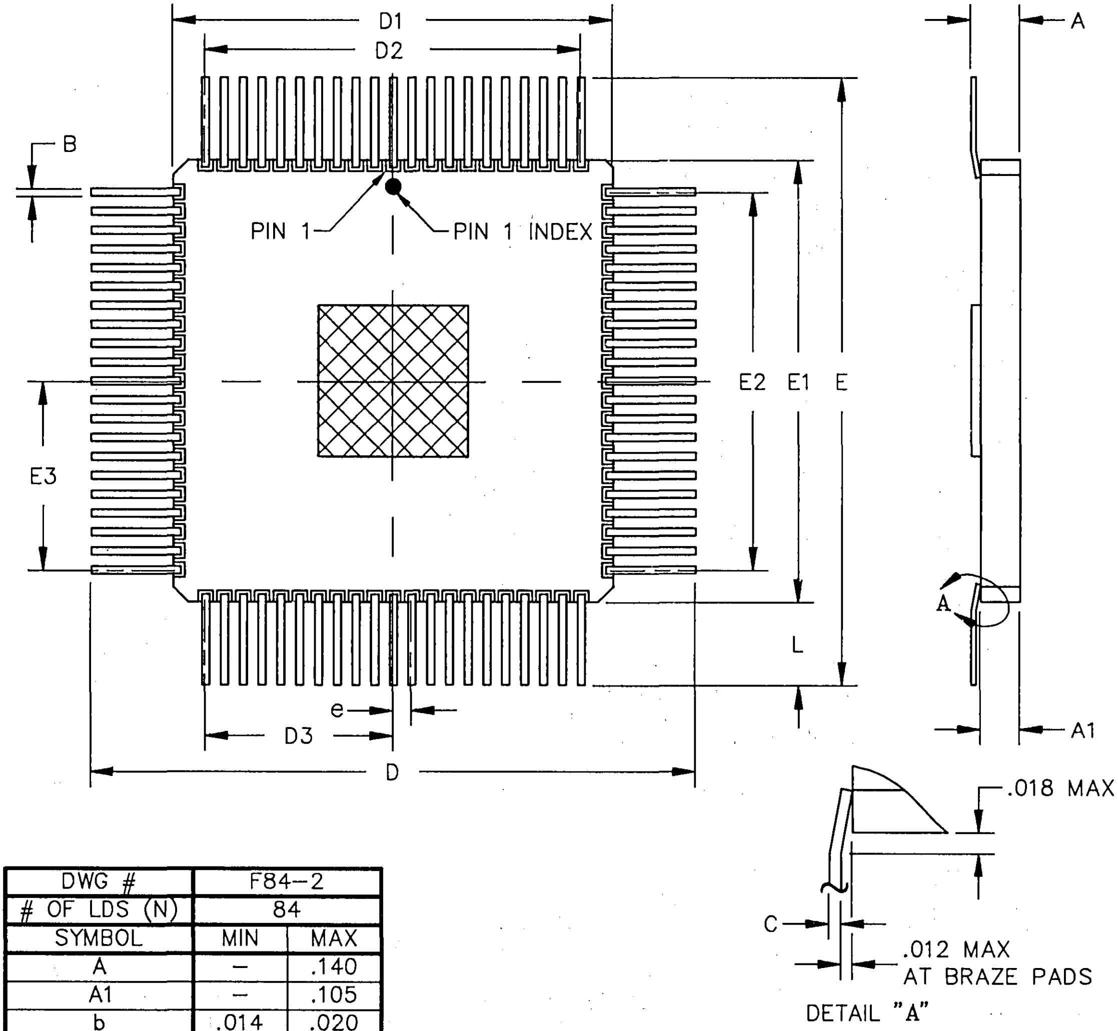
NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. CROSS HATCHED AREA INDICATES INTEGRAL METALLIC HEAT SINK.



DETAIL A

FLATPACKS (Continued)

84 LEAD QUAD FLATPACK (CAVITY UP)

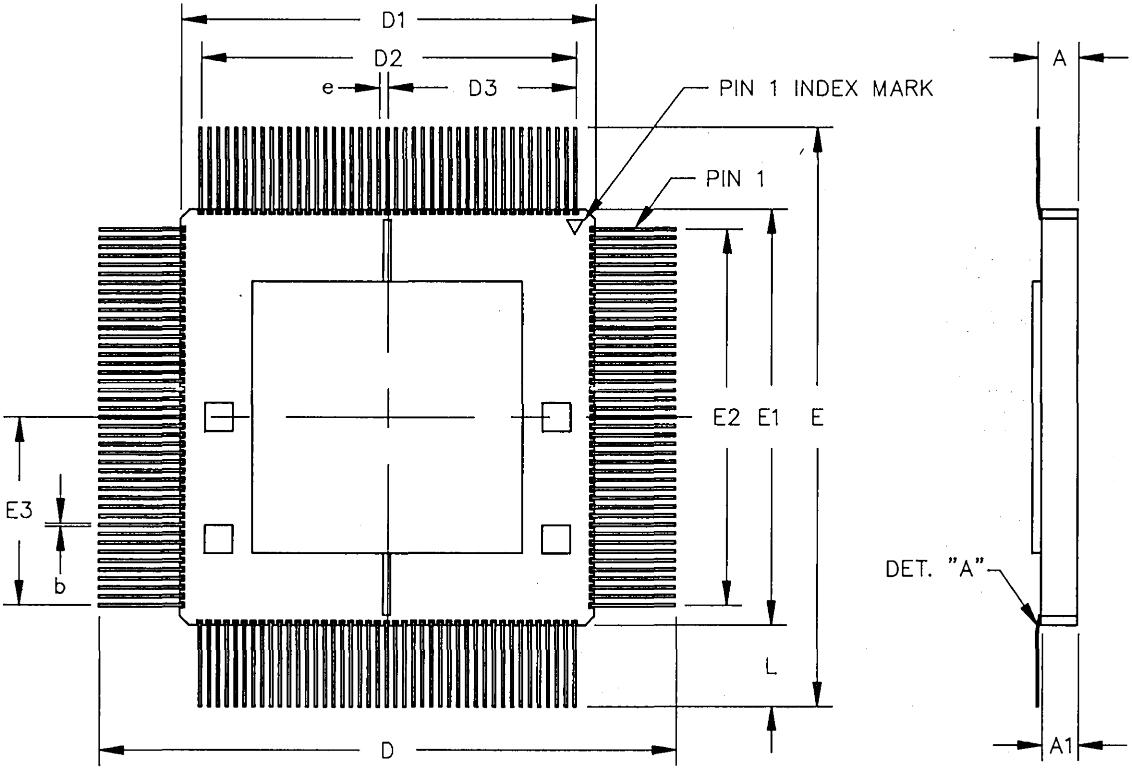


DWG #	F84–2	
# OF LDS (N)	84	
SYMBOL	MIN	MAX
A	—	.140
A1	—	.105
b	.014	.020
C	.007	.013
D/E	1.485	1.615
D1/E1	1.130	1.170
D2/E2	1.000 BSC	
D3/E3	.500 BSC	
e	.050 BSC	
L	.350	.450
ND/NE	21	

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. CROSS HATCHED AREA INDICATES INTEGRAL METALLIC HEAT SINK.

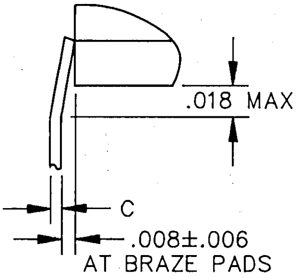
FLATPACKS (Continued)

172 LEAD QUAD FLATPACK (CAVITY UP – R3001)



DWG #	F172-1	
# OF LDS (N)	172	
SYMBOL	MIN	MAX
A	–	.130
A1	–	.105
b	.006	.010
C	.004	.008
D/E	1.580	1.620
D1/E1	1.135	1.165
D2/E2	1.050 BSC	
D3/E3	.525 BSC	
e	.025 BSC	
L	.220	.230
ND/NE	43	

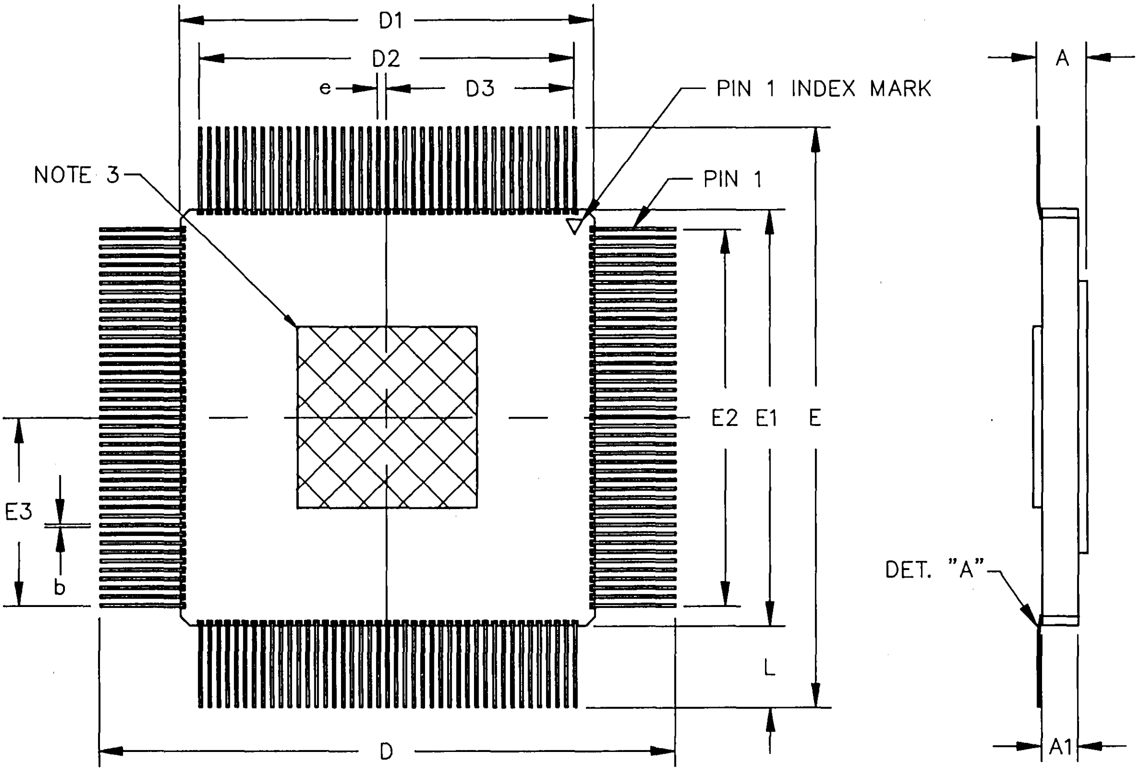
NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.



DETAIL A

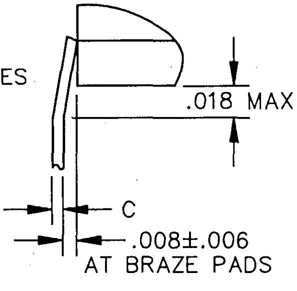
FLATPACKS (Continued)

172 LEAD QUAD FLATPACK (CAVITY DOWN – R3000A)



DWG #	F172–2	
# OF LDS (N)	172	
SYMBOL	MIN	MAX
A	–	.130
A1	–	.105
b	.006	.010
C	.004	.008
D/E	1.580	1.620
D1/E1	1.135	1.165
D2/E2	1.050 BSC	
D3/E3	.525 BSC	
e	.025 BSC	
L	.220	.230
ND/NE	43	

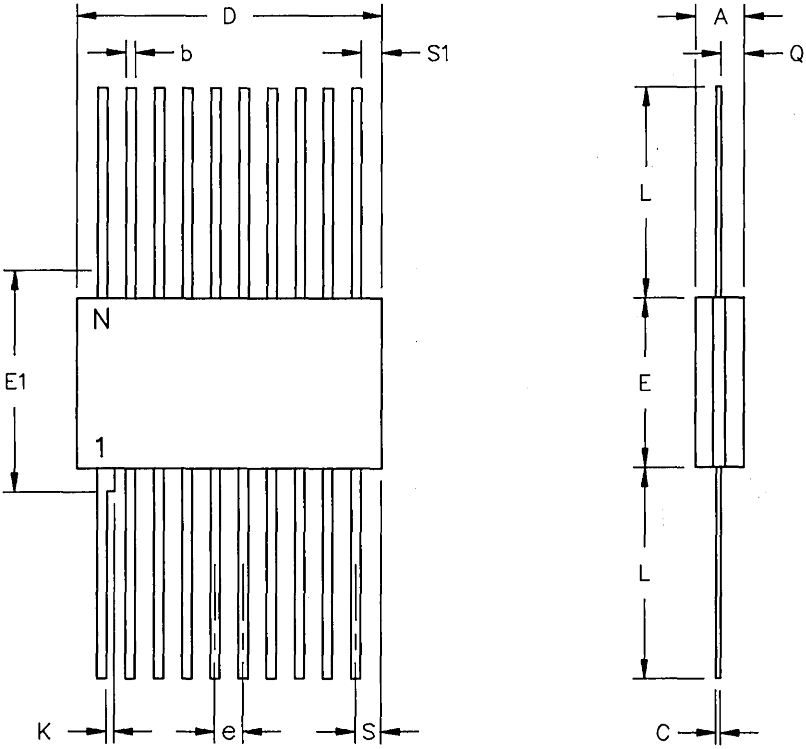
NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. CROSS HATCHED AREA INDICATES METALLIC HEAT SINK.



DETAIL A

CERPACKS

16–28 LEAD CERPACK

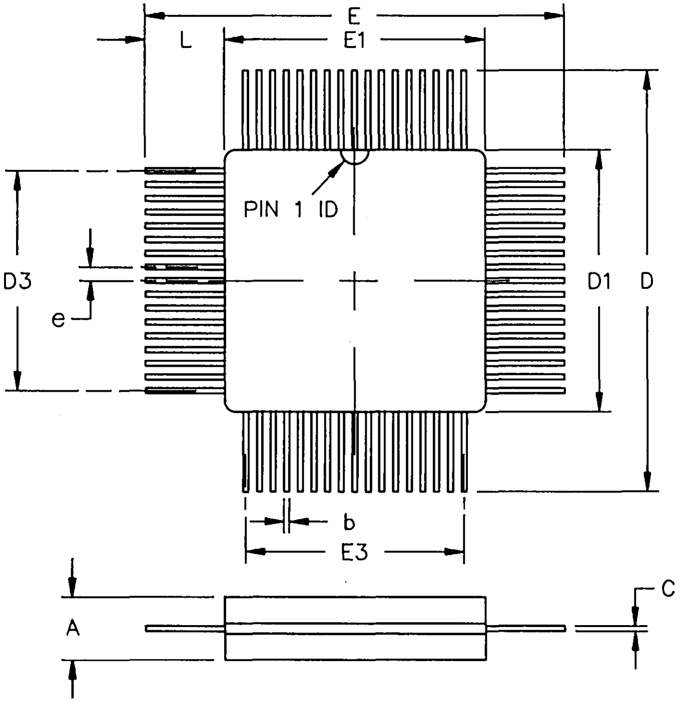


NOTES:
1. ALL DIMENSION ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	E16–1		E20–1		E24–1		E28–1		E28–2	
# OF LDS (N)	16		20		24		28		28	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.055	.085	.045	.092	.045	.090	.045	.115	.045	.090
b	.015	.019	.015	.019	.015	.019	.015	.019	.015	.019
C	.0045	.006	.0045	.006	.0045	.006	.0045	.009	.0045	.006
D	.370	.430	–	.540	–	.640	–	.740	–	.740
E	.245	.285	.245	.300	.300	.420	.460	.520	.340	.380
E1	–	.305	–	.305	–	.440	–	.550	–	.400
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
K	.008	.015	.008	.015	.008	.015	.008	.015	.008	.015
L	.250	.370	.250	.370	.250	.370	.250	.370	.250	.370
Q	.026	.040	.026	.040	.026	.040	.026	.045	.026	.045
S	–	.045	–	.045	–	.045	–	.045	–	.045
S1	.005	–	.005	–	.005	–	.000	–	.005	–

CERQUADS

68 LEAD CERQUAD (STRAIGHT LEADS)

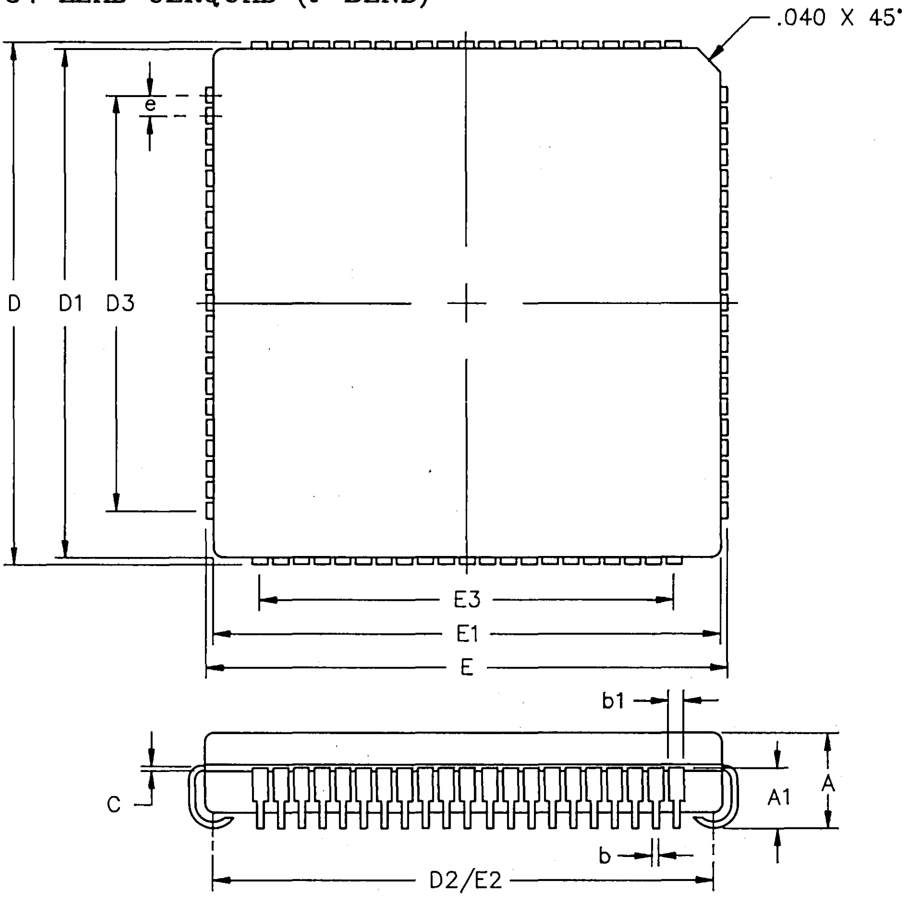


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	CQ68-1	
# OF LDS (N)	68	
SYMBOL	MIN	MAX
A	.115	.165
b	.008	.013
C	.0045	.008
D/E	.860	1.100
D1/E1	.460	.500
D3/E3	.400 REF	
e	.025 BSC	
L	.200	.300
ND/NE	17	

CERQUADS (Continued)

84 LEAD CERQUAD (J-BEND)

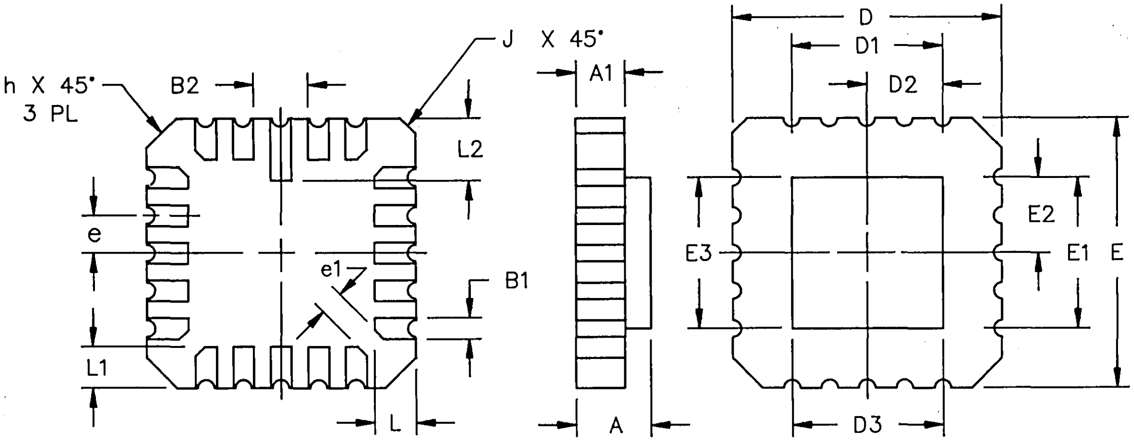


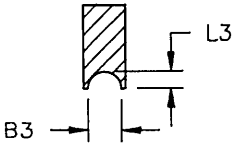
DWG #	CQ84-1	
# OF LDS (N)	84	
SYMBOL	MIN	MAX
A	.155	.200
A1	.090	.120
b1	.022	.032
b	.013	.023
C	.006	.013
D/E	1.170	1.190
D1/E1	1.138	1.162
D2/E2	1.100	1.150
D3/E3	1.000 BSC	
e	.050 BSC	
ND/NE	21	

NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

LEADLESS CHIP CARRIERS





NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

20–48 LEAD LCC (SQUARE)

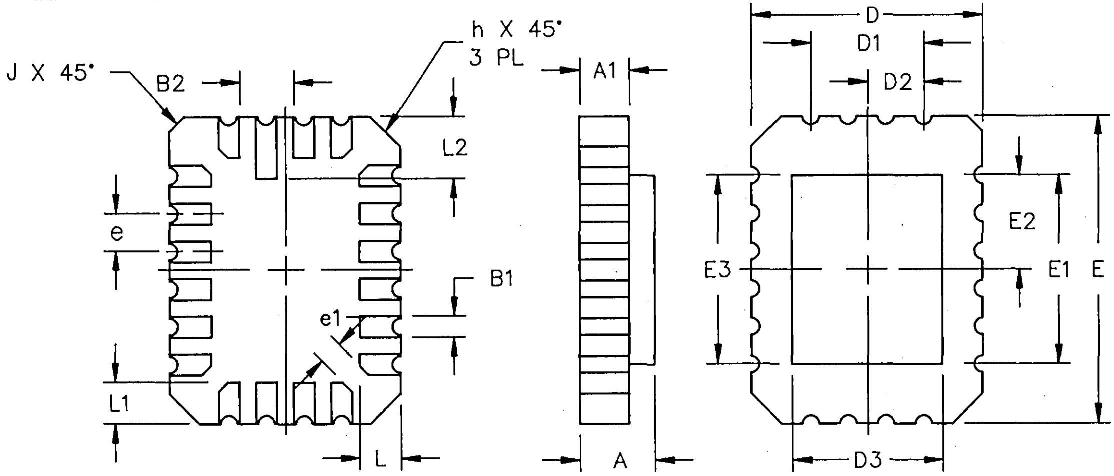
DWG #	L20–2		L28–1		L44–1		L48–1	
# OF LDS (N)	20		28		44		48	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.064	.100	.064	.100	.064	.120	.055	.120
A1	.054	.066	.050	.088	.054	.088	.045	.090
B1	.022	.028	.022	.028	.022	.028	.017	.023
B2	.072 REF		.072 REF		.072 REF		.072 REF	
B3	.006	.022	.006	.022	.006	.022	.006	.022
D/E	.342	.358	.442	.460	.640	.660	.554	.572
D1/E1	.200 BSC		.300 BSC		.500 BSC		.440 BSC	
D2/E2	.100 BSC		.150 BSC		.250 BSC		.220 BSC	
D3/E3	–	.358	–	.460	–	.560	.500	.535
e	.050 BSC		.050 BSC		.050 BSC		.040 BSC	
e1	.015	–	.015	–	.015	–	.015	–
h	.040 REF		.040 REF		.040 REF		.012 RADIUS	
J	.020 REF		.020 REF		.020 REF		.020 REF	
L	.045	.055	.045	.055	.045	.055	.033	.047
L1	.045	.055	.045	.055	.045	.055	.033	.047
L2	.077	.093	.077	.093	.077	.093	.077	.093
L3	.003	.015	.003	.015	.003	.015	.003	.015
ND/NE	5		7		11		12	

LEADLESS CHIP CARRIERS (Continued)

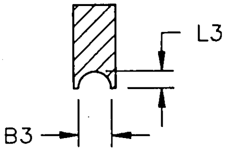
52–68 LEAD LCC (SQUARE)

DWG #	L52–1		L52–2		L68–2		L68–1	
# OF LDS (N)	52		52		68		68	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.061	.087	.082	.120	.082	.120	.065	.120
A1	.051	.077	.072	.088	.072	.088	.055	.075
B1	.022	.028	.022	.028	.022	.028	.008	.014
B2	.072 REF		.072 REF		.072 REF		.072 REF	
B3	.006	.022	.006	.022	.006	.022	.006	.022
D/E	.739	.761	.739	.761	.938	.962	.554	.566
D1/E1	.600 BSC		.600 BSC		.800 BSC		.400 BSC	
D2/E2	.300 BSC		.300 BSC		.400 BSC		.200 BSC	
D3/E3	–	.661	–	.661	–	.862	–	.535
e	.050 BSC		.050 BSC		.050 BSC		.025 BSC	
e1	.015	–	.015	–	.015	–	.015	–
h	.040 REF		.040 REF		.040 REF		.040 REF	
J	.020 REF		.020 REF		.020 REF		.020 REF	
L	.045	.055	.045	.055	.045	.055	.045	.055
L1	.045	.055	.045	.055	.045	.055	.045	.055
L2	.077	.093	.075	.093	.077	.093	.077	.093
L3	.003	.015	.003	.015	.003	.015	.003	.015
ND/NE	13		13		17		17	

LEADLESS CHIP CARRIERS (Continued)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

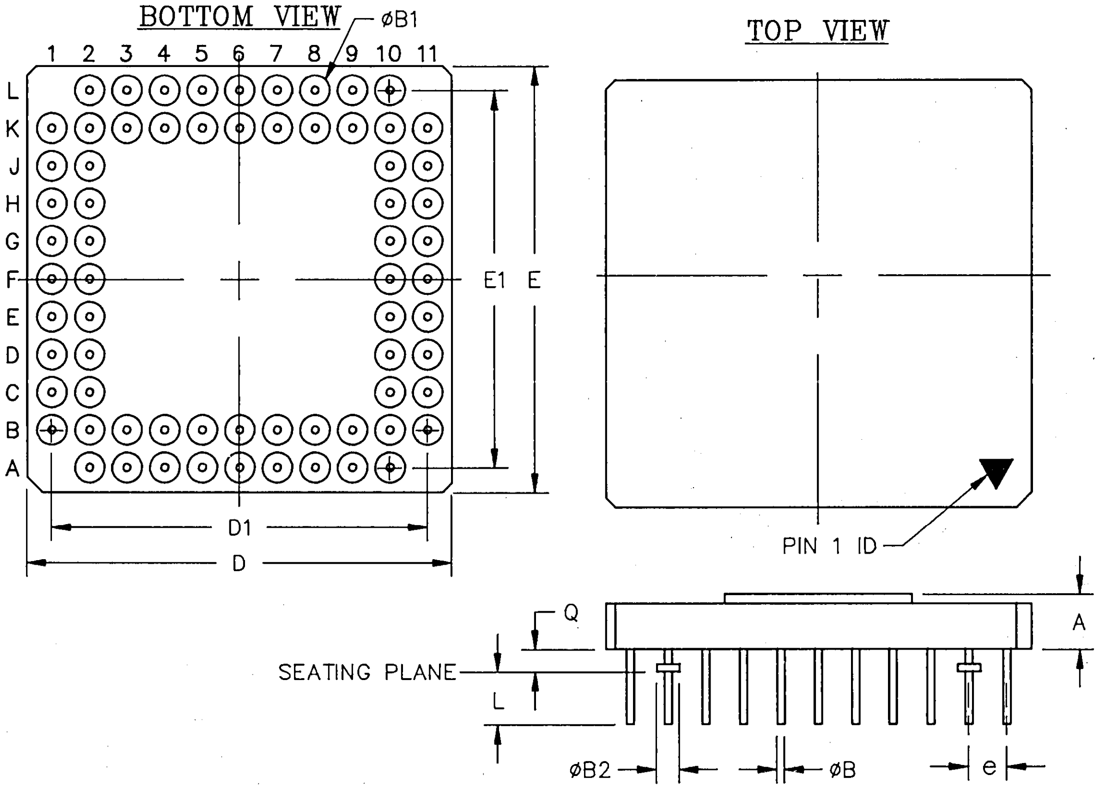


20–32 LEAD LCC (RECTANGULAR)

DWG #	L20–1		L22–1		L24–1		L28–2		L32–1	
# OF LDS (N)	20		22		24		28		32	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.060	.075	.064	.100	.064	.120	.060	.120	.060	.120
A1	.050	.065	.054	.063	.054	.066	.050	.088	.050	.088
B1	.022	.028	.022	.028	.022	.028	.022	.028	.022	.028
B2	.072 REF		.072 REF		.072 REF		.072 REF		.072 REF	
B3	.006	.022	.006	.022	.006	.022	.006	.022	.006	.022
D	.284	.296	.284	.296	.292	.308	.342	.358	.442	.458
D1	.150 BSC		.150 BSC		.200 BSC		.200 BSC		.300 BSC	
D2	.075 BSC		.075 BSC		.100 BSC		.100 BSC		.150 BSC	
D3	–	.280	–	.280	–	.308	–	.358	–	.458
E	.420	.435	.480	.496	.392	.408	.540	.560	.540	.560
E1	.250 BSC		.300 BSC		.300 BSC		.400 BSC		.400 BSC	
E2	.125 BSC		.150 BSC		.150 BSC		.200 BSC		.200 BSC	
E3	–	.410	–	.480	–	.408	–	.558	–	.558
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
e1	.015	–	.015	–	.015	–	.015	–	.015	–
h	.040 REF		.012 RADIUS		.025 REF		.040 REF		.040 REF	
J	.020 REF		.012 RADIUS		.015 REF		.020 REF		.020 REF	
L	.045	.055	.039	.051	.040	.050	.045	.055	.045	.055
L1	.045	.055	.039	.051	.040	.050	.045	.055	.045	.055
L2	.080	.095	.083	.097	.077	.093	.077	.093	.077	.093
L3	.003	.015	.003	.015	.003	.015	.003	.015	.003	.015
ND	4		4		5		5		7	
NE	6		7		7		9		9	

PIN GRID ARRAYS

68 PIN PGA (CAVITY UP)

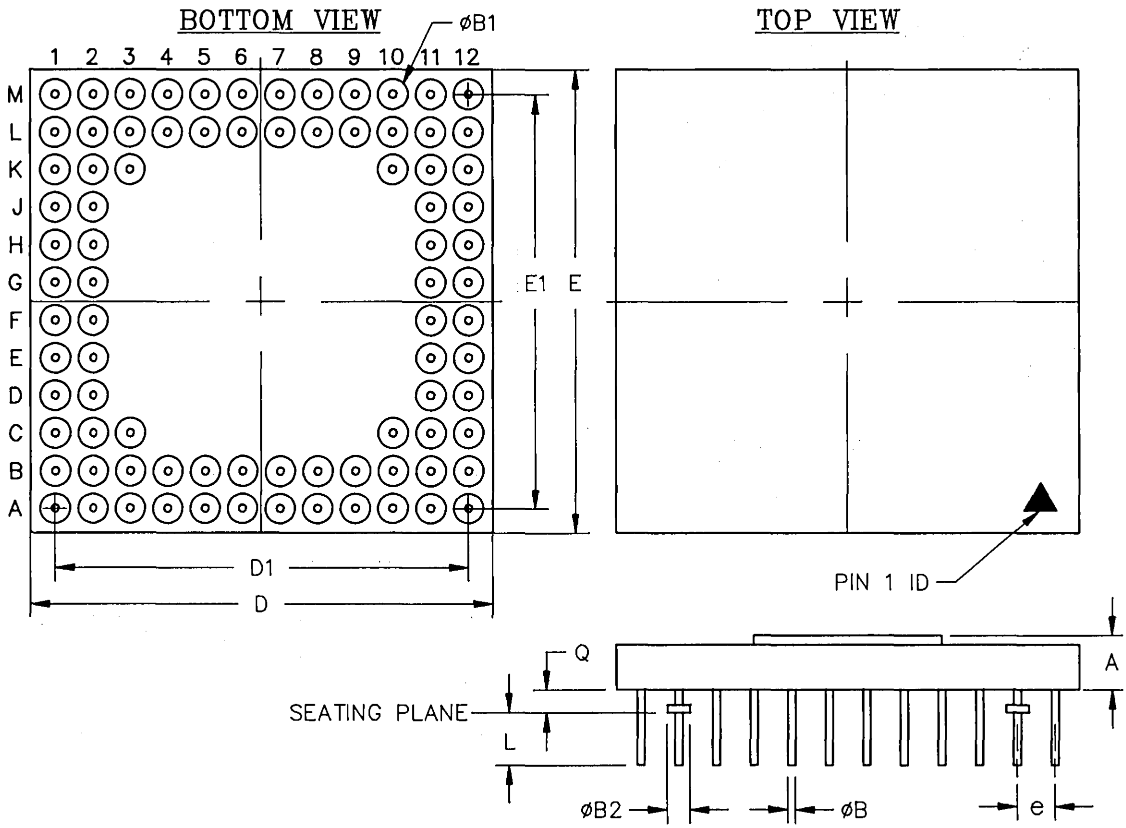


DWG #	G68–1	
# OF PINS (N)	68	
SYMBOL	MIN	MAX
A	.070	.145
øB	.016	.020
øB1	–	.080
øB2	.040	.060
D/E	1.140	1.180
D1/E1	1.000 BSC	
e	.100 BSC	
L	.120	.140
M	11	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

84 PIN PGA (CAVITY UP – 12 X 12 GRID)

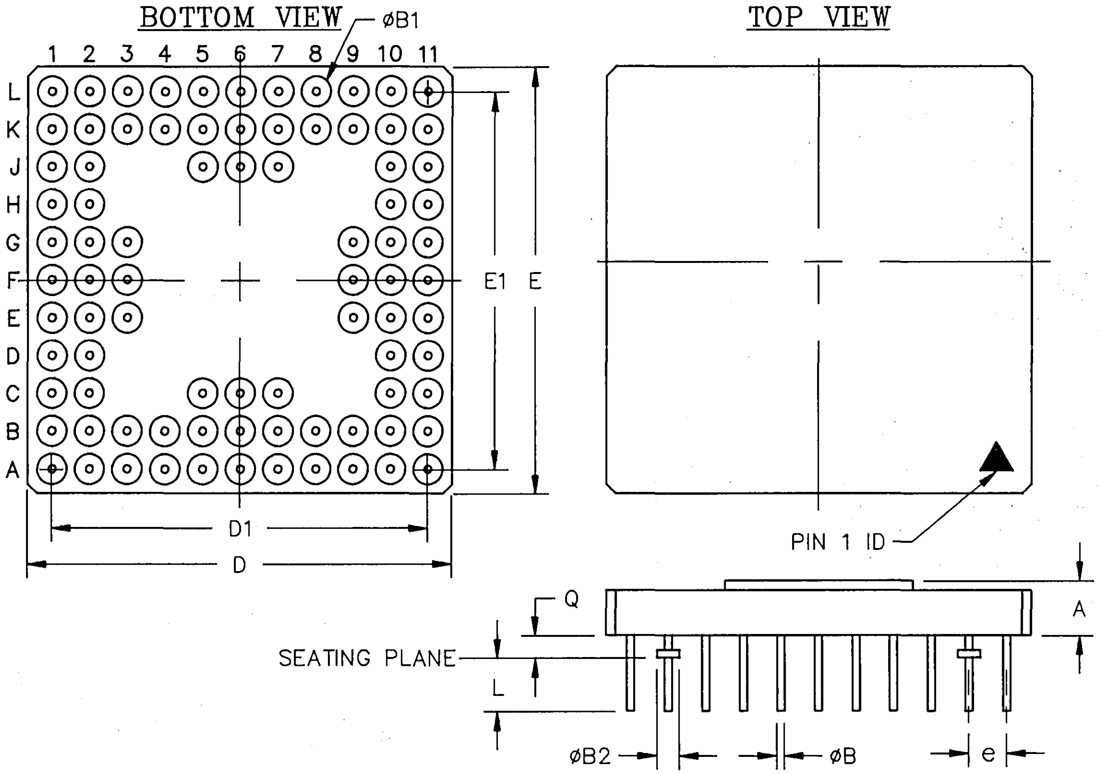


DWG #	G84–1	
# OF PINS (N)	84	
SYMBOL	MIN	MAX
A	.077	.145
øB	.016	.020
øB1	.060	.080
øB2	.040	.060
D/E	1.180	1.235
D1/E1	1.100 BSC	
e	.100 BSC	
L	.120	.140
M	12	
Q	.025	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

84 PIN PGA (CAVITY UP – 11 X 11 GRID)

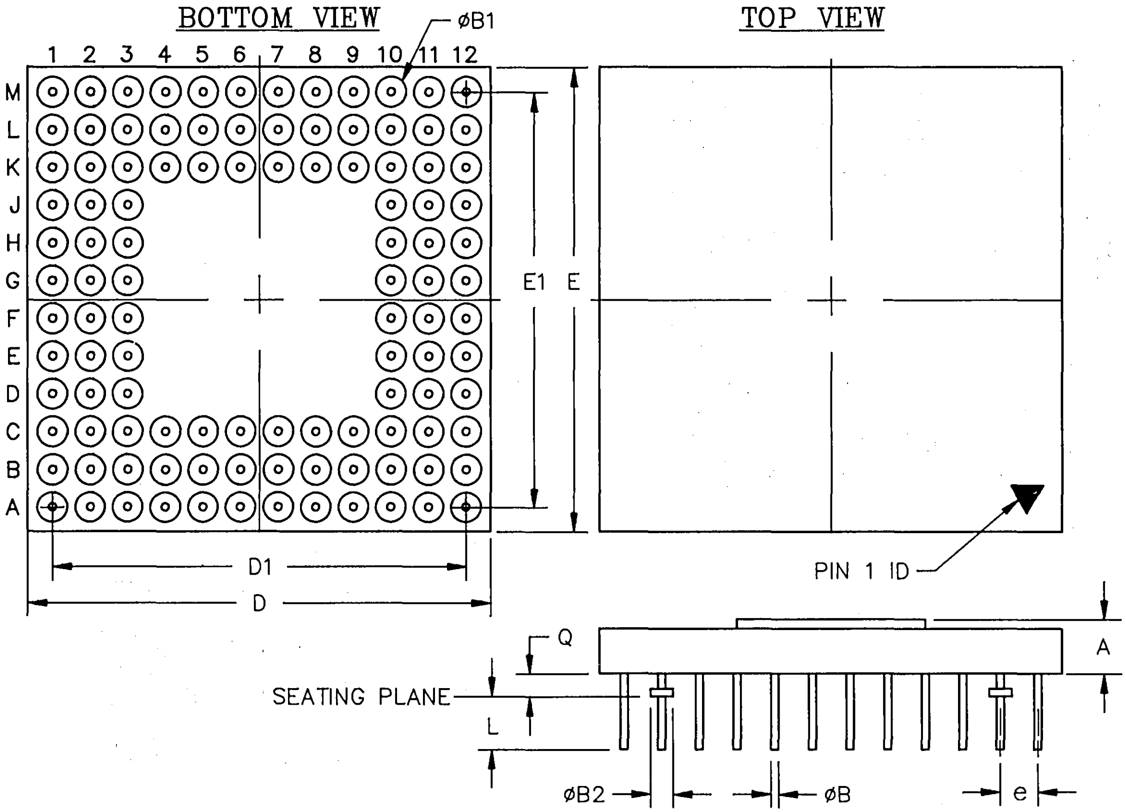


DWG #	G84–3	
# OF PINS (N)	84	
SYMBOL	MIN	MAX
A	.070	.145
øB	.016	.020
øB1	–	.080
øB2	.040	.060
D/E	1.080	1.120
D1/E1	1.000 BSC	
e	.100 BSC	
L	.120	.140
M	11	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

108 PIN PGA (CAVITY UP)

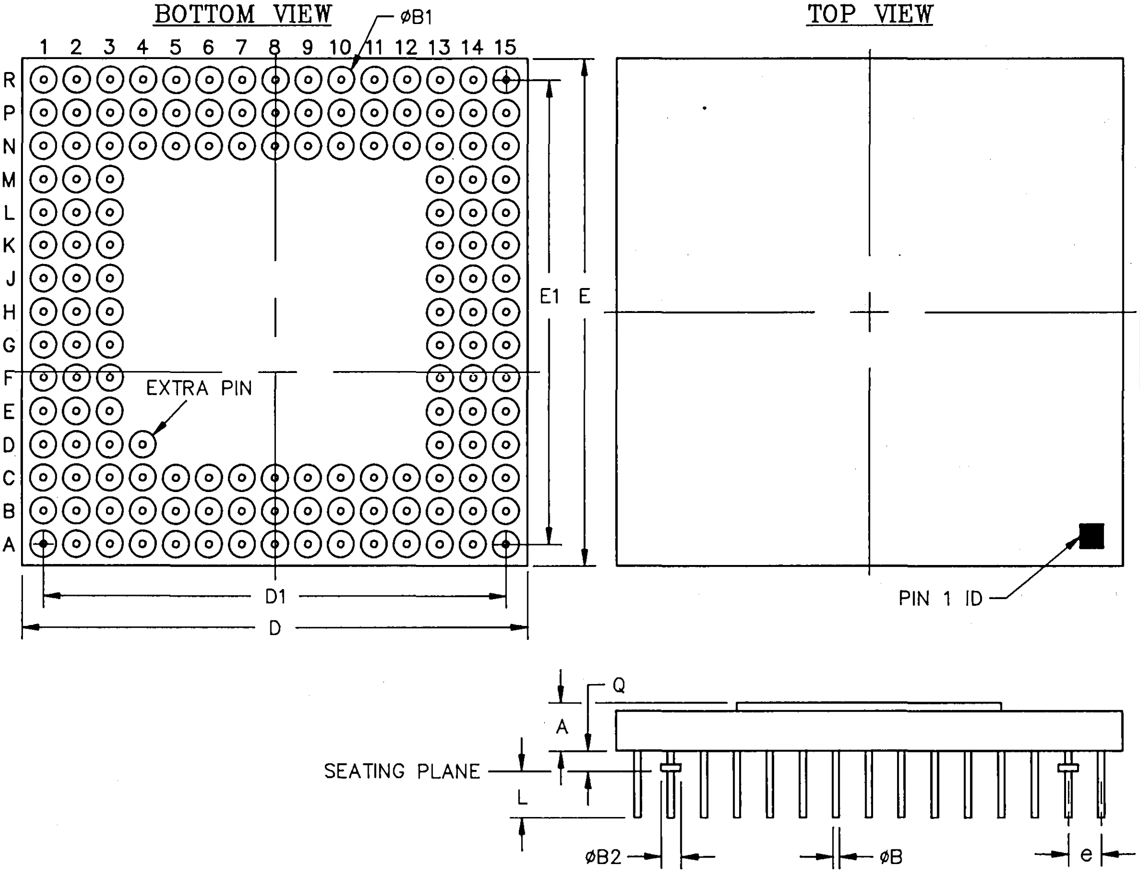


DWG #	G108-1	
# OF PINS (N)	108	
SYMBOL	MIN	MAX
A	.070	.145
ØB	.016	.020
ØB1	–	.080
ØB2	.040	.060
D/E	1.188	1.212
D1/E1	1.100 BSC	
e	.100 BSC	
L	.120	.140
M	12	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

144 PIN PGA (CAVITY UP – R3001)



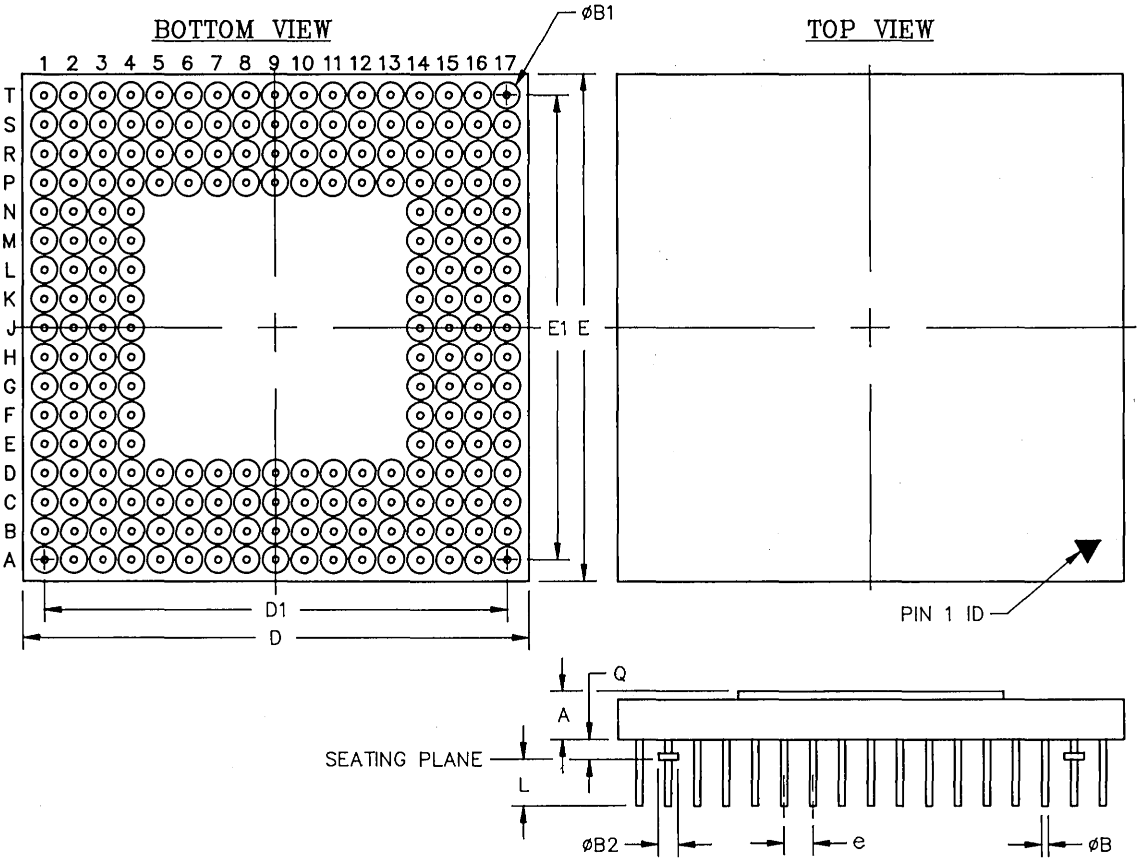
DWG #	G144-2	
# OF PINS (N)	145	
SYMBOL	MIN	MAX
A	.082	.125
ØB	.016	.020
ØB1	.060	.080
ØB2	.040	.060
D/E	1.559	1.590
D1/E1	1.400 BSC	
e	.100 BSC	
L	.120	.140
M	15	
Q	.040	.060

NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.
6. EXTRA PIN (D–4) ELECTRICALLY CONNECTED TO D–3.

PIN GRID ARRAYS (Continued)

208 PIN PGA (CAVITY UP)



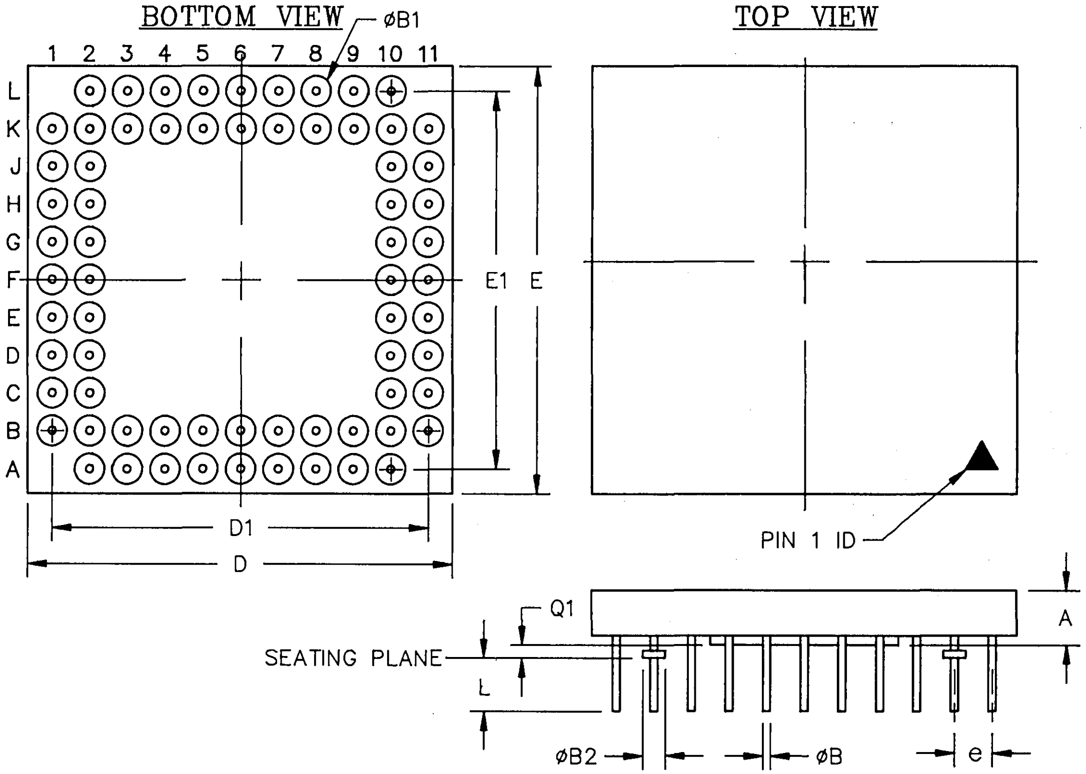
DWG #	G208-1	
# OF PINS (N)	208	
SYMBOL	MIN	MAX
A	.070	.145
ØB	.016	.020
ØB1	–	.080
ØB2	.040	.060
D/E	1.732	1.780
D1/E1	1.600 BSC	
e	.100 BSC	
L	.125	.140
M	17	
Q	.040	.060

NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

68 PIN PGA (CAVITY DOWN)

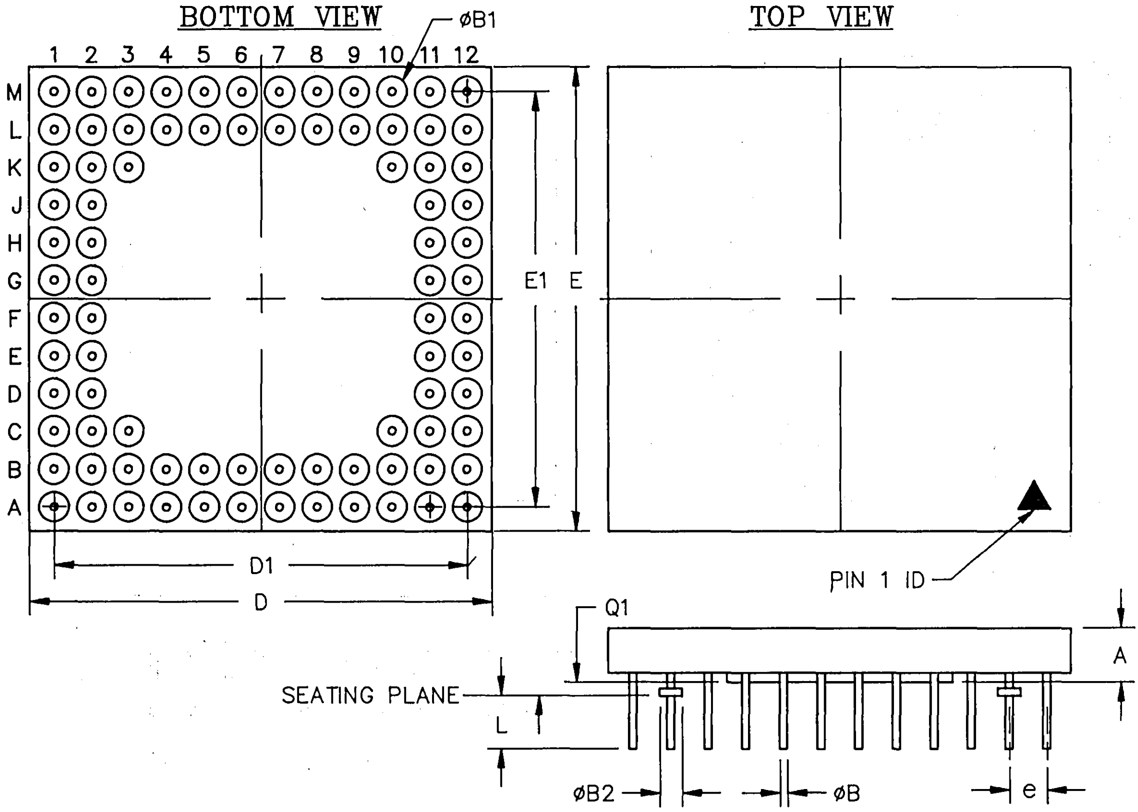


DWG #	GU68-2	
# OF PINS (N)	68	
SYMBOL	MIN	MAX
A	.077	.095
øB	.016	.020
øB1	.060	.080
øB2	.040	.060
D/E	1.098	1.122
D1/E1	1.000 BSC	
e	.100 BSC	
L	.120	.140
M	11	
Q1	.025	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

84 PIN PGA (CAVITY DOWN)



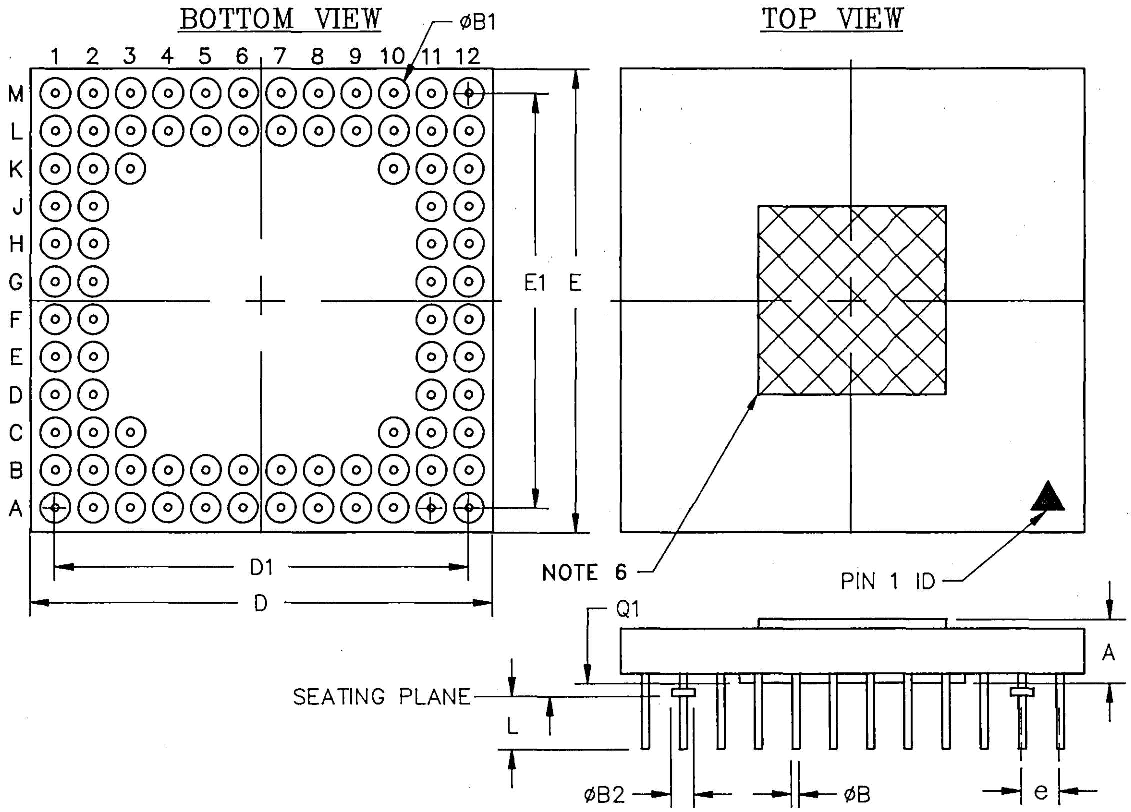
DWG #	G84-2	
# OF PINS (N)	84	
SYMBOL	MIN	MAX
A	.077	.145
øB	.016	.020
øB1	.060	.080
øB2	.040	.060
D/E	1.180	1.235
D1/E1	1.100 BSC	
e	.100 BSC	
L	.120	.140
M	12	
Q1	.025	.060

NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

84 PIN PGA (CAVITY DOWN – R3010A)

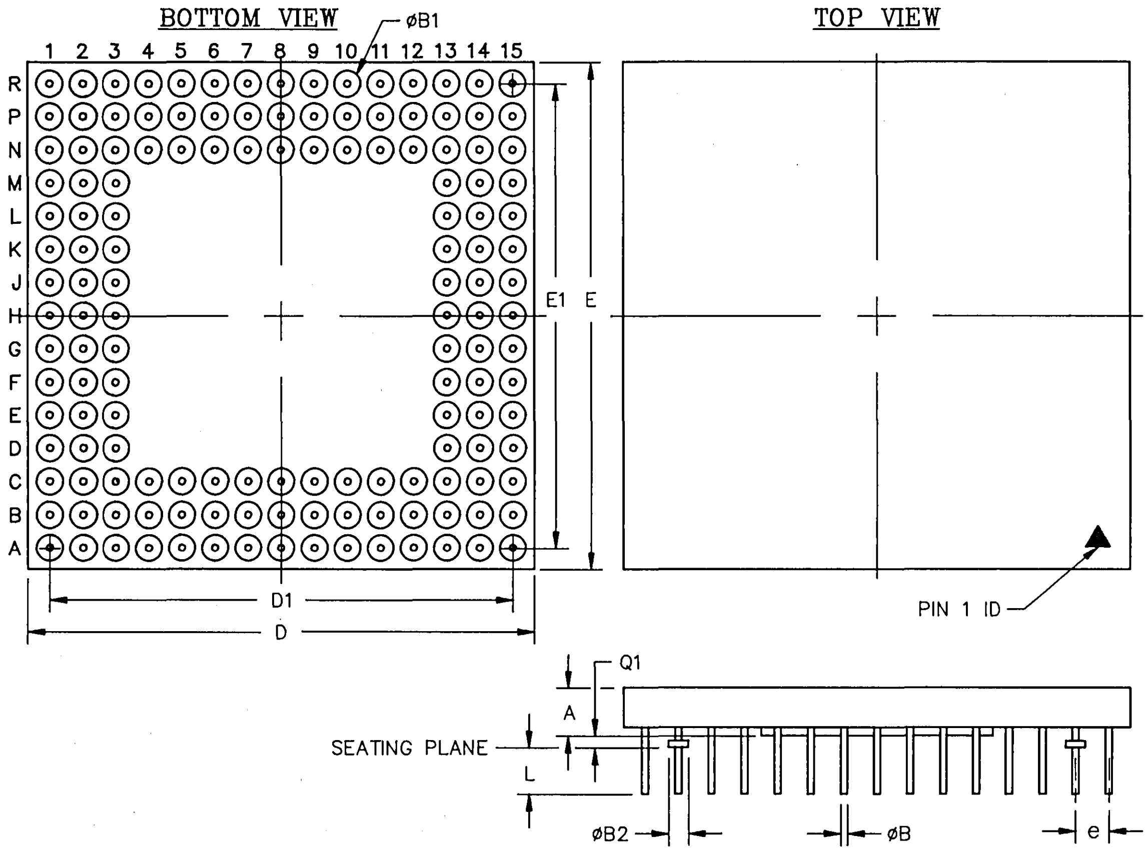


DWG #	G84-4	
# OF PINS (N)	84	
SYMBOL	MIN	MAX
A	.077	.145
ØB	.016	.020
ØB1	.060	.080
ØB2	.040	.060
D/E	1.180	1.235
D1/E1	1.100 BSC	
e	.100 BSC	
L	.120	.140
M	12	
Q1	.025	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.
6. CROSS HATCHED AREA INDICATES INTEGRALL METALLIC HEAT SINK.

PIN GRID ARRAYS (Continued)

144 PIN PGA (CAVITY DOWN)

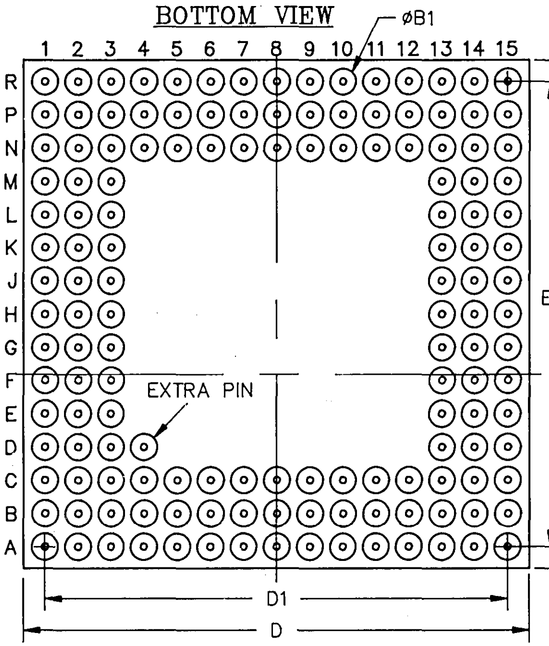


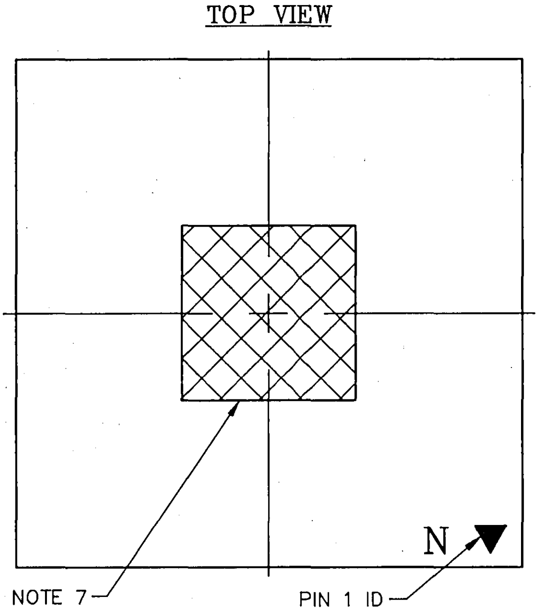
DWG #	G144–1	
# OF PINS (N)	144	
SYMBOL	MIN	MAX
A	.082	.100
øB	.016	.020
øB1	.060	.080
øB2	.040	.060
D/E	1.559	1.590
D1/E1	1.400 BSC	
e	.100 BSC	
L	.120	.140
M	15	
Q1	.025	.060

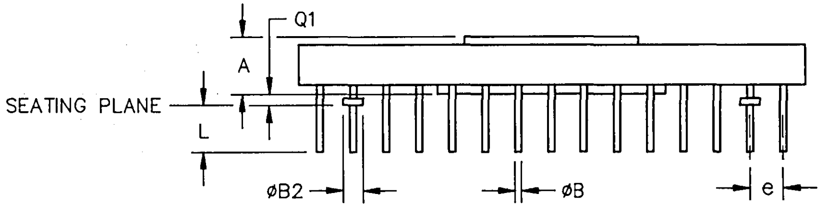
NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

144 PIN PGA (CAVITY DOWN – R3000A)







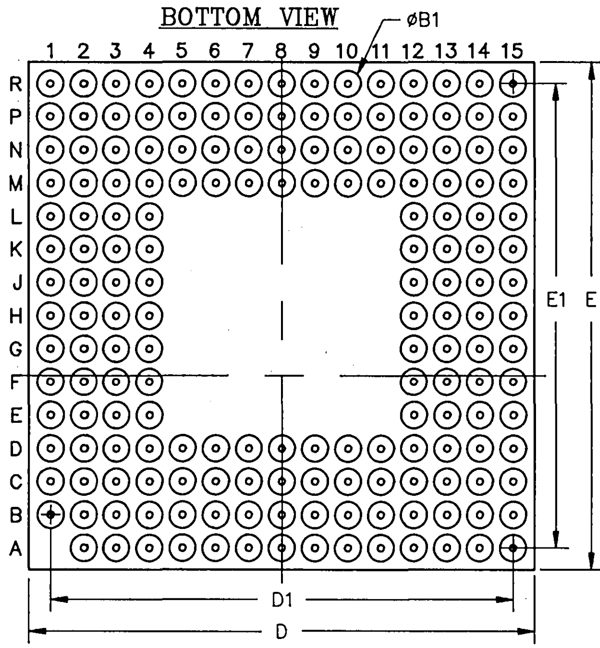
DWG #	G144-3	
# OF PINS (N)	145	
SYMBOL	MIN	MAX
A	.082	.130
ØB	.016	.020
ØB1	.060	.080
ØB2	.040	.060
D/E	1.559	1.590
D1/E1	1.400 BSC	
e	.100 BSC	
L	.120	.140
M	15	
Q1	.025	.060

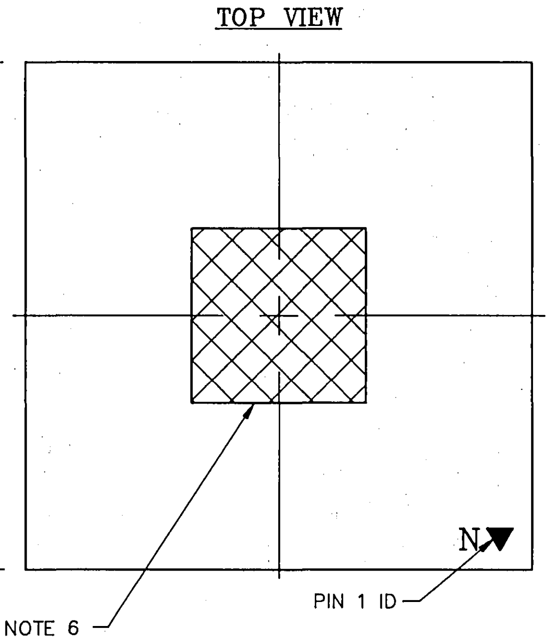
NOTES:

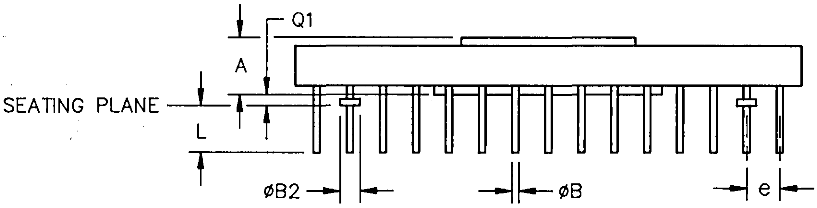
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.
6. EXTRA PIN (D-4) ELECTRICALLY CONNECTED TO D-3.
7. CROSS HATCHED AREA INDICATES INTEGRAL METALLIC HEAT SINK.

PIN GRID ARRAYS (Continued)

175 PIN PGA (CAVITY DOWN – R3000A)







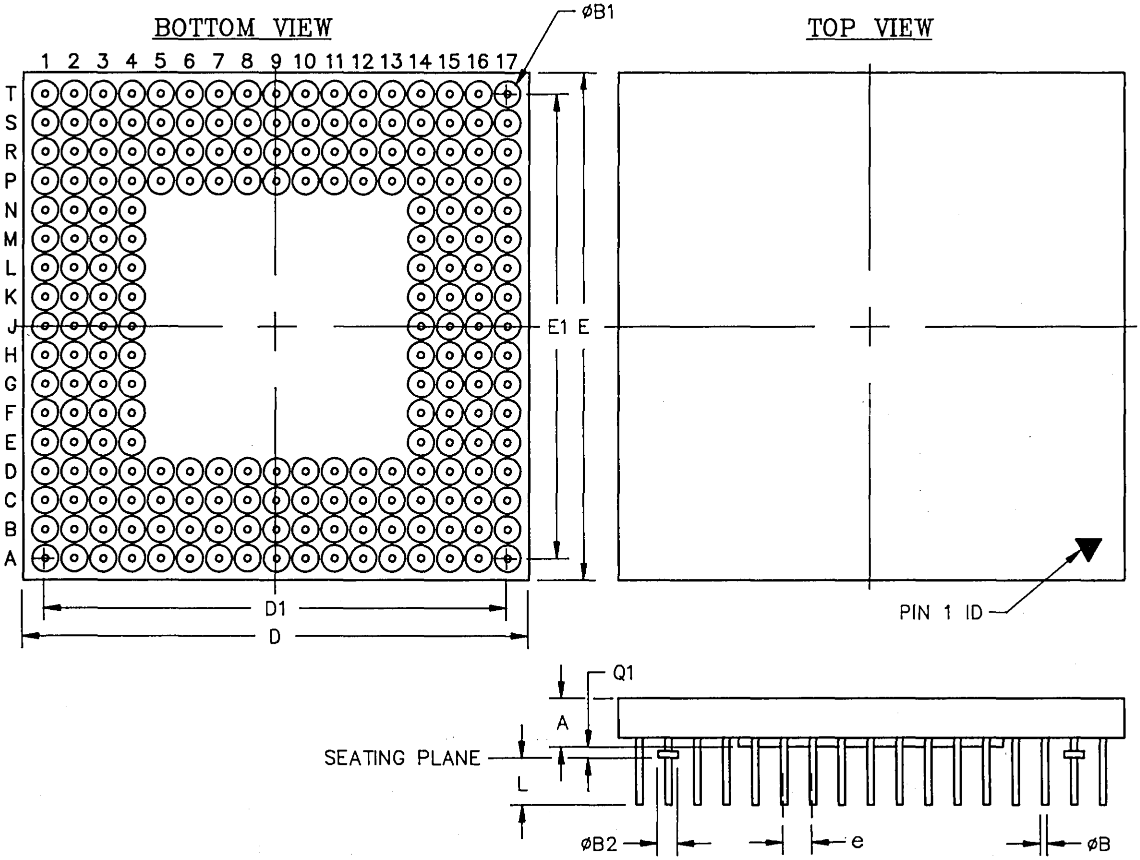
DWG #	G175–1	
# OF PINS (N)	175	
SYMBOL	MIN	MAX
A	.082	.130
øB	.016	.020
øB1	.060	.080
øB2	.040	.060
D/E	1.559	1.590
D1/E1	1.400 BSC	
e	.100 BSC	
L	.120	.140
M	15	
Q1	.025	.060

NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.
6. CROSS HATCHEDAREA INDICATES INTEGRAL METALLIC HEAT SINK.

PIN GRID ARRAYS (Continued)

208 PIN PGA (CAVITY DOWN)



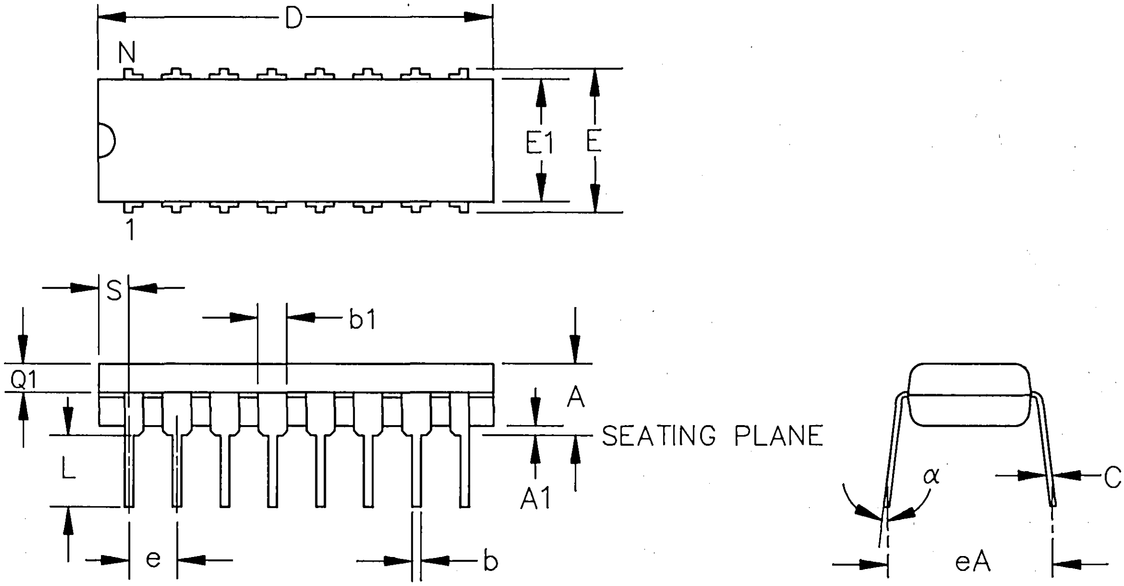
DWG #	G208–2	
# OF PINS (N)	208	
SYMBOL	MIN	MAX
A	.070	.145
øB	.016	.020
øB1	–	.080
øB2	.040	.060
D/E	1.732	1.780
D1/E1	1.600 BSC	
e	.100 BSC	
L	.125	.140
M	17	
Q1	.025	.060

NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PLASTIC DUAL IN-LINE PACKAGES

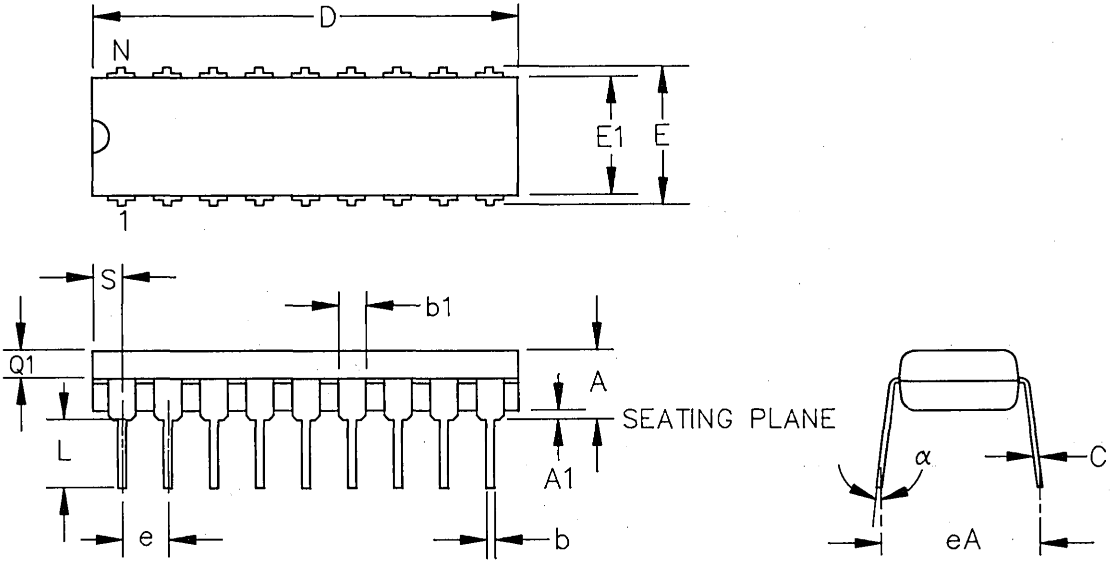
16-32 LEAD PLASTIC DIP (300 MIL)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. D & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DWG #	P16-1		P22-1		P28-2		P32-2	
# OF LDS (N)	16		22		28		32	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.140	.165	.145	.165	.145	.180	.145	.180
A1	.015	.035	.015	.035	.015	.030	.015	.030
b	.015	.022	.015	.022	.015	.022	.016	.022
b1	.050	.070	.050	.065	.045	.065	.045	.060
C	.008	.012	.008	.012	.008	.015	.008	.015
D	.745	.760	1.050	1.060	1.345	1.375	1.545	1.585
E	.300	.325	.300	.320	.300	.325	.300	.325
E1	.247	.260	.240	.270	.270	.295	.275	.295
e	.090	.110	.090	.110	.090	.110	.090	.110
eA	.310	.370	.310	.370	.310	.400	.310	.400
L	.120	.150	.120	.150	.120	.150	.120	.150
α	0°	15°	0°	15°	0°	15°	0°	15°
S	.015	.035	.020	.040	.020	.042	.020	.060
Q1	.050	.070	.055	.075	.055	.065	.055	.065

PLASTIC DUAL IN-LINE PACKAGES (Continued)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. D & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

18–24 LEAD PLASTIC DIP (300 MIL – FULL LEAD)

DWG #	P18–1		P20–1		P24–1	
# OF LDS (N)	18		20		24	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX
A	.140	.165	.145	.165	.145	.165
A1	.015	.035	.015	.035	.015	.035
b	.015	.020	.015	.020	.015	.020
b1	.050	.070	.050	.070	.050	.065
C	.008	.012	.008	.012	.008	.012
D	.885	.910	1.022	1.040	1.240	1.255
E	.300	.325	.300	.325	.300	.320
E1	.247	.260	.240	.280	.250	.275
e	.090	.110	.090	.110	.090	.110
eA	.310	.370	.310	.370	.310	.370
L	.120	.150	.120	.150	.120	.150
α	0°	15°	0°	15°	0°	15°
S	.040	.060	.025	.070	.055	.075
Q1	.050	.070	.055	.075	.055	.070

PLASTIC DUAL IN-LINE PACKAGES (Continued)

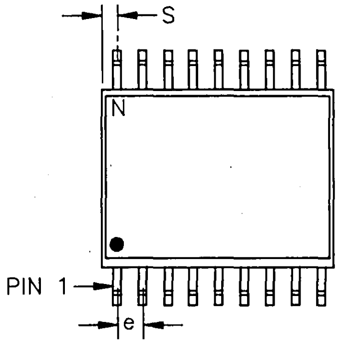
24-48 LEAD PLASTIC DIP (600 MIL)

DWG #	P24-2		P28-1		P32-1		P40-1		P48-1	
# OF LEADS (N)	24		28		32		40		48	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.160	.185	.160	.185	.170	.190	.160	.185	.170	.200
A1	.015	.035	.015	.035	.015	.050	.015	.035	.015	.035
b	.015	.020	.015	.020	.016	.020	.015	.020	.015	.020
b1	.050	.065	.050	.065	.045	.055	.050	.065	.050	.065
C	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012
D	1.240	1.260	1.420	1.460	1.645	1.655	2.050	2.070	2.420	2.450
E	.600	.620	.600	.620	.600	.625	.600	.620	.600	.620
E1	.530	.550	.530	.550	.530	.550	.530	.550	.530	.560
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
eA	.610	.670	.610	.670	.610	.670	.610	.670	.610	.670
L	.120	.150	.120	.150	.125	.135	.120	.150	.120	.150
α	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°
S	.060	.080	.055	.080	.070	.080	.070	.085	.060	.075
Q1	.060	.080	.060	.080	.065	.075	.060	.080	.060	.080

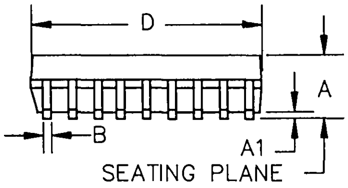
64 LEAD PLASTIC DIP (900 MIL)

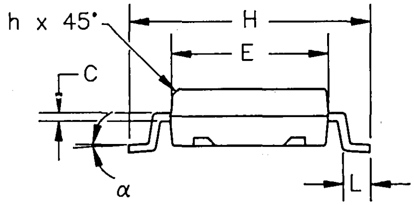
DWG #	P64-1	
# OF LEADS (N)	64	
SYMBOLS	MIN	MAX
A	.180	.230
A1	.015	.040
b	.015	.020
b1	.050	.065
C	.008	.012
D	3.200	3.220
E	.900	.925
E1	.790	.810
e	.090	.110
eA	.910	1.000
L	.120	.150
α	0°	15°
S	.045	.065
Q1	.080	.090

SMALL OUTLINE IC



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND TO BE MEASURED FROM THE BOTTOM OF PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.

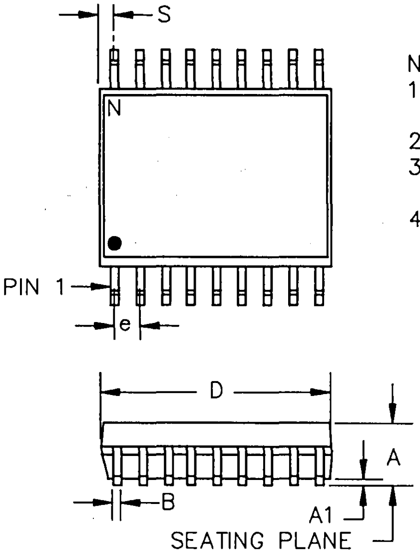




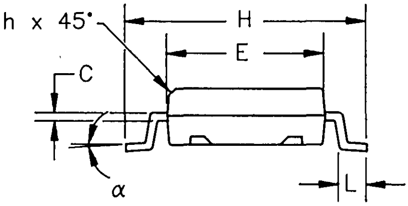
16–24 LEAD SMALL OUTLINE (GULL WING)

DWG #	S016–1		S018–1		S020–2		S024–2		S024–3	
# OF LDS (N)	16 (.300)		18 (.300)		20 (.300")		24 (.300")		24 (.300")	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.095	.1043	.095	.1043	.095	.1043	.095	.1043	.110	.120
A1	.005	.0118	.005	.0118	.005	.0118	.005	.0118	.005	.0118
B	.014	.020	.014	.020	.014	.020	.014	.020	.014	.020
C	.0091	.0125	.0091	.0125	.0091	.0125	.0091	.0125	.007	.011
D	.403	.413	.447	.462	.497	.511	.600	.614	.620	.630
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
E	.292	.2992	.292	.2992	.292	.2992	.292	.2992	.295	.305
h	.010	.020	.010	.020	.010	.020	.010	.020	.012	.020
H	.400	.419	.400	.419	.400	.419	.400	.419	.406	.419
L	.018	.045	.018	.045	.018	.045	.018	.045	.028	.045
α	0°	8°	0°	8°	0°	8°	0°	8°	0°	8°
S	.023	.035	.023	.035	.023	.035	.023	.035	.032	.043

SMALL OUTLINE IC (Continued)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND TO BE MEASURED FROM THE BOTTOM OF THE PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.



28 LEAD SMALL OUTLINE (GULL WING)

DWG #	S028-2		S028-3	
# OF LDS (N)	28 (.300")		28 (.330")	
SYMBOL	MIN	MAX	MIN	MAX
A	.095	.1043	.110	.120
A1	.005	.0118	.005	.014
B	.014	.020	.014	.019
C	.0091	.0125	.006	.010
D	.700	.712	.718	.728
e	.050 BSC		.050 BSC	
E	.292	.2992	.340	.350
h	.010	.020	.012	.020
H	.400	.419	.462	.478
L	.018	.045	.028	.045
α	0°	8°	0°	8°
S	.023	.035	.023	.035

SMALL OUTLINE IC (Continued)

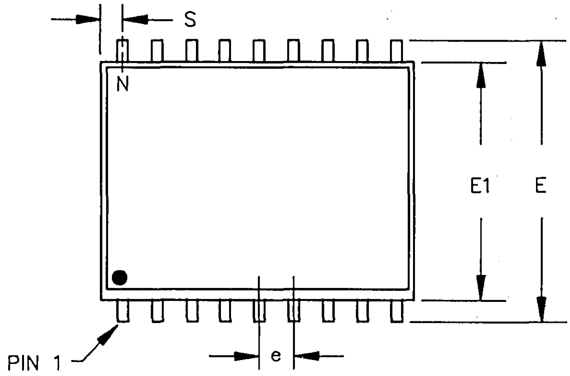
16–24 LEAD SMALL OUTLINE (EIAJ – .0315 PITCH)

DWG #	S016-5		S020-5		S024-5	
# OF LDS (N)	16		20		24	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX
A	.057	.071	.069	.083	.069	.083
A1	.002 TYP		.002 TYP		.002 TYP	
B	.012	.020	.012	.020	.012	.020
C	.006	.010	.006	.010	.006	.010
D	.248	.271	.331	.354	.382	.405
E	.165	.180	.205	.220	.205	.220
e	.0315 BSC		.0315 BSC		.0315 BSC	
H	.232	.256	.295	.319	.295	.319
L	.010	–	.010	–	.010	–
α	0°	8°	0°	8°	0°	8°

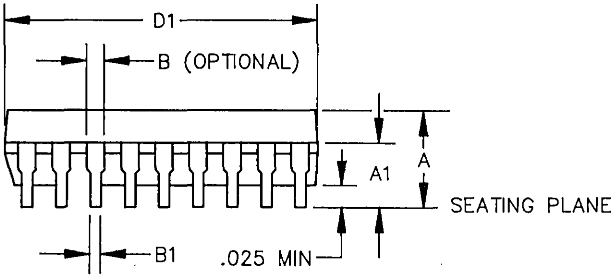
16–28 LEAD SMALL OUTLINE (EIAJ – .050 PITCH)

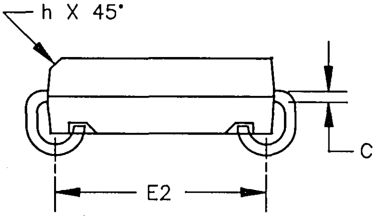
DWG #	S016-6		S018-6		S020-6		S024-6		S028-6	
# OF LDS (N)	16		18		20		24		28	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.057	.071	.069	.083	.069	.083	.069	.083	.083	.098
A1	.002 TYP		.002 TYP		.002 TYP		.002 TYP		.002 TYP	
B	.012	.020	.012	.020	.012	.020	.012	.020	.012	.020
C	.006	.010	.006	.010	.006	.010	.006	.010	.006	.010
D	.382	.406	.437	.453	.480	.504	.580	.603	.720	.740
E	.165	.180	.205	.220	.205	.220	.205	.220	.290	.300
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
H	.232	.256	.295	.319	.295	.319	.295	.319	.378	.402
L	.010	–	.010	–	.010	–	.010	–	.010	–
α	0°	8°	0°	8°	0°	8°	0°	8°	0°	8°

SMALL OUTLINE IC (Continued)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSION AND TO BE MEASURED FROM THE BOTTOM OF THE PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE

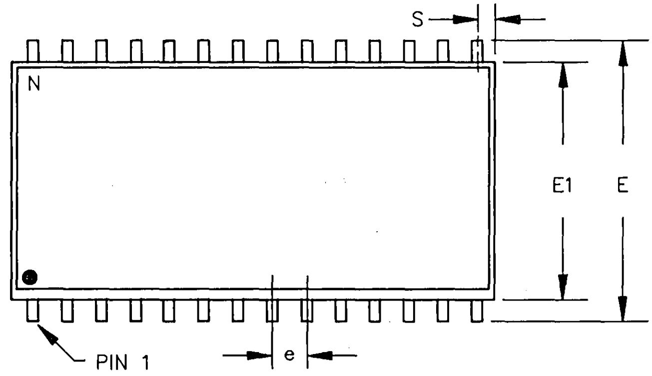




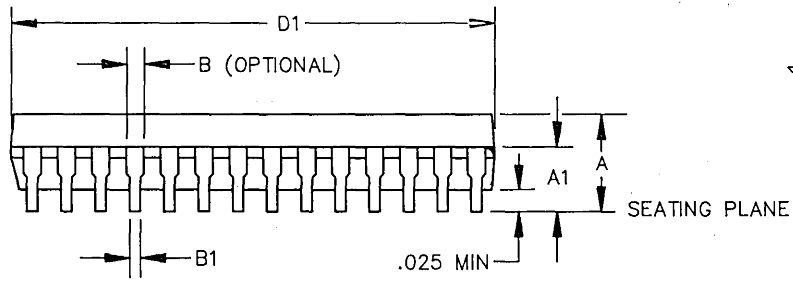
16–24 LEAD SMALL OUTLINE (J–BEND)

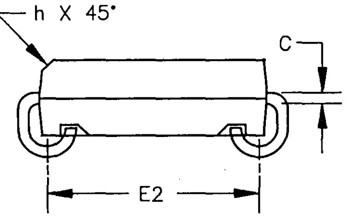
DWG #	SO16–2		SO20–1		SO24–4	
# OF LDS (N)	16 LD (.300")		20 LD (.300")		24 LD (.300")	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX
A	.120	.140	.120	.140	.130	.148
A1	.078	.095	.078	.095	.082	.095
B	.020	.024	.020	.024	.026	.032
B1	.014	.020	.014	.020	.015	.020
C	.008	.013	.008	.013	.007	.011
D1	.400	.412	.500	.512	.620	.630
E	.335	.347	.335	.347	.335	.345
E1	.292	.300	.292	.300	.295	.305
E2	.262	.272	.262	.272	.260	.280
e	.050 BSC		.050 BSC		.050 BSC	
h	.010	.020	.010	.020	.010	.020
S	.023	.035	.023	.035	.032	.043

SMALL OUTLINE IC (Continued)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSION AND TO BE MEASURED FROM THE BOTTOM OF THE PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.



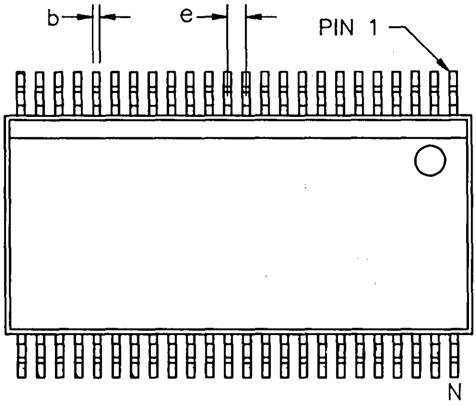


28–32 LEAD SMALL OUTLINE (J–BEND)

DWG #	S028–5		S028–4		S032–2	
# OF LDS (N)	28 LD (.300")		28 LD (.350")		32 LD (.300")	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX
A	.120	.140	.130	.148	.130	.148
A1	.078	.095	.082	.095	.082	.095
B	.020	.024	.026	.032	.026	.032
B1	.014	.020	.016	.020	.016	.020
C	.008	.013	.007	.011	.008	.013
D1	.700	.712	.720	.730	.820	.830
E	.335	.347	.380	.390	.330	.340
E1	.292	.300	.345	.355	.295	.305
E2	.262	.272	.310	.330	.260	.275
e	.050 BSC		.050 BSC		.050 BSC	
h	.012	.020	.012	.020	.012	.020
S	.023	.035	.023	.035	.032	.043

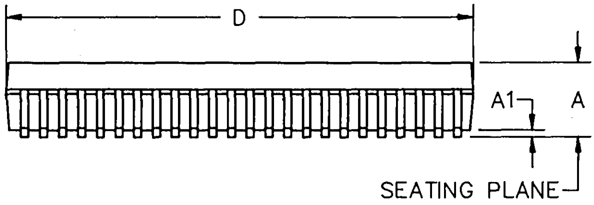
SMALL OUTLINE IC (Continued)

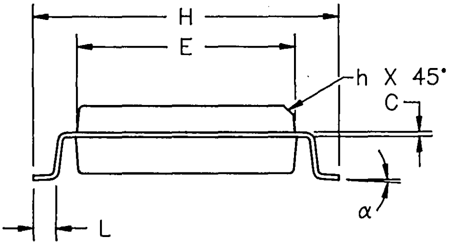
48 & 56 LEAD SMALL OUTLINE (SSOP – GULL WING)



NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.

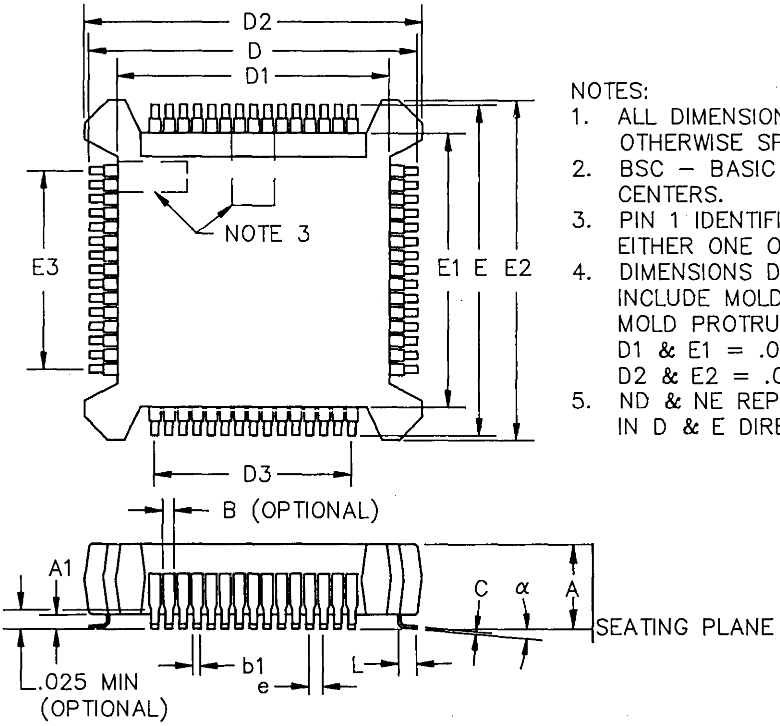




DWG #	S048-1		S056-1	
# OF LDS (N)	48 (.300")		56 (.300")	
SYMBOL	MIN	MAX	MIN	MAX
A	.095	.110	.095	.110
A1	.008	.016	.008	.016
b	.008	.012	.008	.012
C	.005	.009	.005	.009
D	.620	.630	.720	.730
E	.291	.299	.291	.299
e	.025 BSC		.025 BSC	
H	.395	.420	.395	.420
h	.015	.025	.015	.025
L	.020	.040	.020	.040
α	0°	8°	0°	8°

PLASTIC QUAD FLATPACKS

100–132 LEAD PLASTIC QUAD FLATPACK (JEDEC)



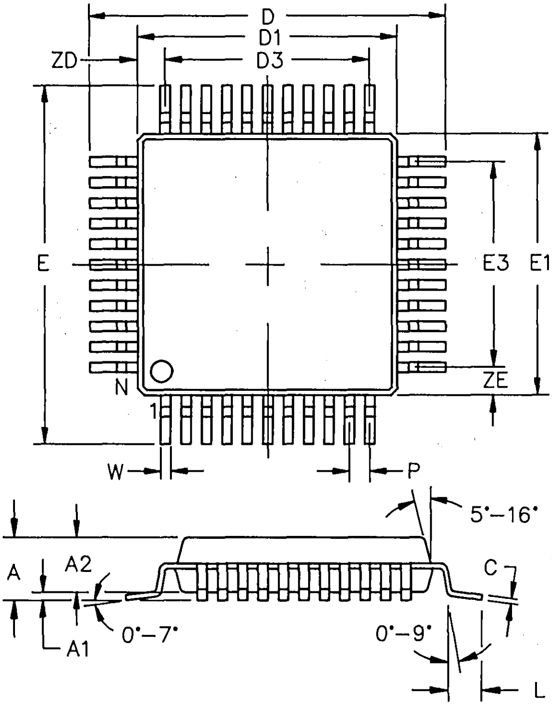
NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. PIN 1 IDENTIFIER CAN BE POSITIONED AT EITHER ONE OF THESE TWO LOCATIONS.
4. DIMENSIONS D1, D2, E1, AND E2 DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE MOLD PROTRUSIONS ARE AS FOLLOWS:
   D1 & E1 = .010 MAX.
   D2 & E2 = .007 MAX.
5. ND & NE REPRESENT NUMBERS OF LEADS IN D & E DIRECTIONS RESPECTIVELY.

DWG #	PQ100–1		PQ132–1	
# OF LDS (N)	100		132	
SYMBOLS	MIN	MAX	MIN	MAX
A	.160	.180	.160	.180
A1	.020	.040	.020	.040
B	.008	.016	.008	.016
b1	.008	.012	.008	.012
C	.0055	.008	.0055	.008
D	.875	.885	1.075	1.085
D1	.747	.753	.947	.953
D2	.897	.903	1.097	1.103
D3	.600 REF		.800 REF	
e	.025 BSC		.025 BSC	
E	.875	.885	1.075	1.085
E1	.747	.753	.947	.953
E2	.897	.903	1.097	1.103
E3	.600 REF		.800 REF	
L	.020	.030	.020	.030
α	0°	8°	0°	8°
ND/NE	25/25		33/33	

PLASTIC QUAD FLATPACKS (Continued)

80–128 LEAD PLASTIC QUAD FLATPACK (EIAJ)



NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .010 PER SIDE.
4. ND & NE REPRESENT NUMBERS OF LEADS IN D & E DIRECTIONS RESPECTIVELY.
5. THE 3.9mm FOOTPRINT IS STANDARD, HOWEVER THE 3.2mm IS OPTIONAL & CAN BE REQUESTED.

DWG #	PQ80-2		PQ100-2		PQ120-2		PQ128-2	
# OF LDS (N)	80		100		120		128	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.110	.124	.110	.124	.136	.156	.136	.156
A1	.010	–	.010	–	.010	–	.010	–
A2	.100	.120	.100	.120	.125	.144	.125	.144
C	.005	.008	.005	.008	.005	.008	.005	.008
D	.937	.945	.937	.945	1.252	1.260	1.252	1.260
D1	.783	.791	.783	.791	1.098	1.106	1.098	1.106
D3	.724 REF		.742 REF		.913 REF		.976 REF	
E	.701	.709	.701	.709	1.252	1.260	1.252	1.260
E1	.547	.555	.547	.555	1.098	1.106	1.098	1.106
E3	.472 REF		.486 REF		.913 REF		.976 REF	
L	.026	.037	.026	.037	.026	.037	.026	.037
ND/NE	16/24		20/30		30/30		32/32	
P	.0315 BSC		.026 BSC		.026 BSC		.0315 BSC	
W	.012	.018	.012	.018	.012	.018	.012	.018
ZD	.032		.023		.094		.063	
ZE	.039		.032		.094		.063	

ALT. D 5	.909	.917	.909	.917	1.224	1.232	1.224	1.232
ALT. E 5	.673	.681	.673	.681	1.224	1.232	1.224	1.232

PLASTIC QUAD FLATPACKS (Continued)

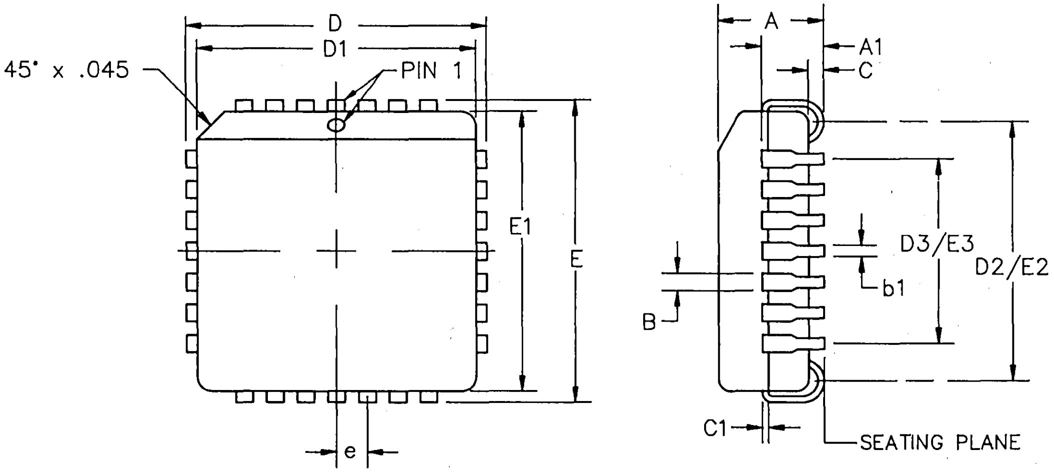
144–208 LEAD PLASTIC QUAD FLATPACK (EIAJ)

DWG #	PQ144–2		PQ160–2		PQ184–2		PQ208–2	
# OF LDS (N)	144		160		184		208	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.136	.156	.136	.156	.136	.156	.136	.156
A1	.010	–	.010	–	.010	–	.010	–
A2	.125	.144	.125	.144	.125	.144	.125	.144
C	.005	.008	.005	.008	.005	.008	.005	.008
D	1.252	1.260	1.252	1.260	1.252	1.260	1.252	1.260
D1	1.098	1.106	1.098	1.106	1.098	1.106	1.098	1.106
D3	.896 RF		.998 REF		.886 REF		1.004 REF	
E	1.252	1.260	1.252	1.260	1.252	1.260	1.252	1.260
E1	1.098	1.106	1.098	1.106	1.098	1.106	1.098	1.106
E3	.896 REF		.998 REF		.886 REF		1.004 REF	
L	.026	.037	.026	.037	.026	.037	.026	.037
ND/NE	36/36		40/40		46/46		52/52	
P	.026 BSC		.026 BSC		.020 BSC		.020 BSC	
W	.009	.014	.009	.014	.009	.014	.009	.014
ZD	.103		.052		.108		.049	
ZE	.103		.052		.108		.049	

ALT. D $\boxed{5}$	1.224	1.232	1.224	1.232	1.224	1.232	1.224	1.232
ALT. E $\boxed{5}$	1.224	1.232	1.224	1.232	1.224	1.232	1.224	1.232

PLASTIC LEADED CHIP CARRIERS

20–84 LEAD PLCC (SQUARE)



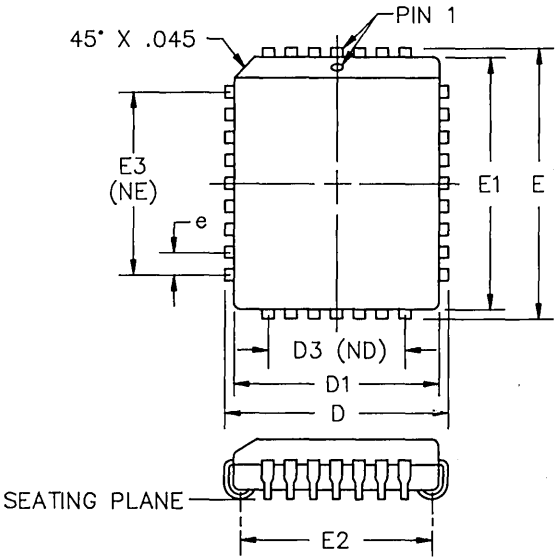
NOTES:

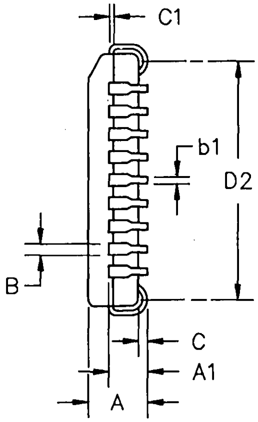
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.
5. ND & NE REPRESENT NUMBER OF LEADS IN D & E DIRECTIONS RESPECTIVELY.
6. D1 & E1 SHOULD BE MEASURED FROM THE BOTTOM OF THE PKG.

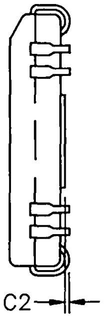
DWG #	J20–1		J28–1		J44–1		J52–1		J68–1		J84–1	
# OF LDS	20		28		44		52		68		84	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.165	.180	.165	.180	.165	.180	.165	.180	.165	.180	.165	.180
A1	.095	.115	.095	.115	.095	.115	.095	.115	.095	.115	.095	.115
B	.026	.032	.026	.032	.026	.032	.026	.032	.026	.032	.026	.032
b1	.013	.021	.013	.021	.013	.021	.013	.021	.013	.021	.013	.021
C	.020	.040	.020	.040	.020	.040	.020	.040	.020	.040	.020	.040
C1	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012
D	.385	.395	.485	.495	.685	.695	.785	.795	.985	.995	1.185	1.195
D1	.350	.356	.450	.456	.650	.656	.750	.756	.950	.956	1.150	1.156
D2/E2	.290	.330	.390	.430	.590	.630	.690	.730	.890	.930	1.090	1.130
D3/E3	.200 REF		.300 REF		.500 REF		.600 REF		.800 REF		1.000 REF	
E	.385	.395	.485	.495	.685	.695	.785	.795	.985	.995	1.185	1.195
E1	.350	.356	.450	.456	.650	.656	.750	.756	.950	.956	1.150	1.156
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
ND/NE	5		7		11		13		17		21	

PLASTIC LEADED CHIP CARRIERS (Continued)

18–32 LEAD PLCC (RECTANGULAR)







OPTIONAL FEATURE
ADHESIVE PEDESTAL
(32 LD ONLY)

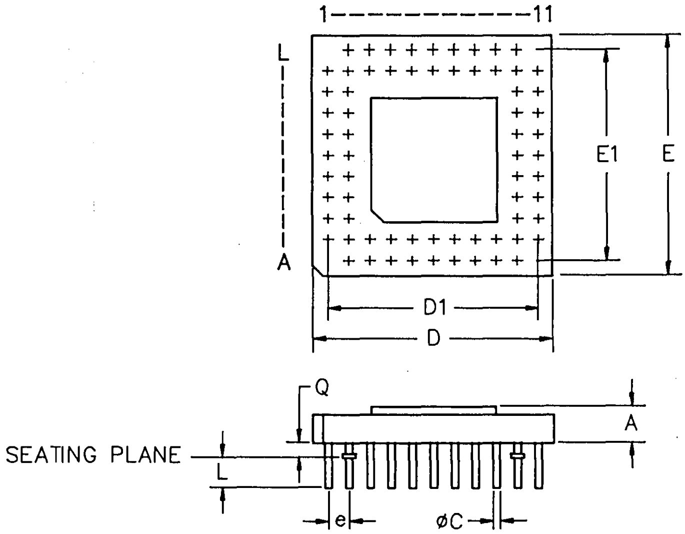
DWG #	J18–1		J32–1	
# OF LDS	18		32	
SYMBOL	MIN	MAX	MIN	MAX
A	.120	.140	.120	.140
A1	.075	.095	.075	.095
B	.026	.032	.026	.032
b1	.013	.021	.013	.021
C	.015	.040	.015	.040
C1	.008	.012	.008	.012
C2	–	–	.005	.015
D	.320	.335	.485	.495
D1	.289	.293	.449	.453
D2	.225	.265	.390	.430
D3	.150 REF		.300 REF	
E	.520	.535	.585	.595
E1	.489	.493	.549	.553
E2	.422	.465	.490	.530
E3	.200 REF		.400 REF	
e	.050 BSC		.050 BSC	
ND/NE	4 / 5		7 / 9	

NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.
5. ND & NE REPRESENT NUMBERS OF LEADS IN D & E DIRECTIONS RESPECTIVELY.
6. D1 & E1 SHOULD BE MEASURED FROM THE BOTTOM OF THE PACKAGE.

PLASTIC PIN GRID ARRAYS

68–208 PIN PGA (CAVITY UP)



NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC PIN SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS.
5. DIM. "A" INCLUDES BOTH THE PKG BODY & THE LID. IT DOES NOT INCLUDE HEATSINK OR OTHER ATTACHED FEATURES.
6. PIN DIAMETER "C" EXCLUDES SOLDER DIP OR OTHER LEAD FINISH.
7. PIN TIPS MAY HAVE RADIUS OR CHAMFER.

DWG No.	PG 68–2		PG 84–2		PG 208–2	
# OF PINS (N)	68 PIN		84 PIN		208 PIN	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX
A	.115	.160	.115	.160	.115	.160
C	.016	.020	.016	.020	.016	.020
D	1.140	1.180	1.140	1.180	1.740	1.780
D1	1.000 BSC		1.000 BSC		1.600 BSC	
E	1.140	1.180	1.140	1.180	1.740	1.780
E1	1.000 BSC		1.000 BSC		1.600 BSC	
e	.100 BSC		.100 BSC		.100 BSC	
L	.100	.160	.100	.160	.100	.160
M	11		11		17	
Q	.040	.070	.040	.070	.040	.070

CEMOS™ STATIC RAM PRODUCTS

Integrated Device Technology, Inc. (IDT) is a major American supplier of high-performance Static Random Access Memories (SRAMs). By coupling leading-edge CEMOS process technology and advanced design techniques, IDT can supply military and commercial customers with earliest access to the world's fastest SRAMs.

WIDEST SELECTION OF SRAMS

Along with performance leadership is the commitment to provide customers with the broadest line of SRAM speeds, densities and organizations available in the world. To match system designers' needs, 16K, 64K and 256K devices are available:

- —in x1, x4, x8 and x16 widths;
- —with additional control features (e.g. dual chip selects, output enables and address latches);
- —with separate inputs and outputs.

These offerings will include x9 widths and one megabit densities. IDT also offers BiCameral SRAMs and other unique architectures.

ADVANCED CEMOS TECHNOLOGY

Innovative process technology development has resulted in outstanding advances in device performance. For example, IDT's 16K SRAM has been redesigned with advanced CEMOS processes from two to less than 0.8 micron line widths, resulting in access time reductions of a magnitude to twelve nanoseconds. This dedication to process improvements means one megabit SRAMs with 20ns access times will soon be available.

CACHE MEMORY — AN IDT SPECIALTY

IDT has applied this speed improvement to cache memory designs. Essential for RISC-based systems, cache memory is required for fast CISC processors because DRAM speeds have not kept pace with processor performance. IDT has the broadest line of Cache-SRAMs available. We offer:

- — the fastest cache-tag SRAM, the IDT6178 (4K x 4);
- —the industry's first SRAM intended for cache data storage, the IDT71586 (4K x 16) with latched addresses;
- — the IDT71589 (32K x 9) to allow i486 designers to use burst counter and self-timed write to take advantage of the cache data storage performance advantage;
- —the IDT71229 BiCameral CacheRAM for the R3000 allows maximum speed caches requiring minimum parts count;
- —SRAMs with Output Enable for cache data storage with specifications optimized for the fastest R3000 applications.

IDT — ONE OF THE LARGEST MILITARY SRAM SUPPLIERS

Military and commercial versions of all IDT CEMOS SRAMs are available. As a leading supplier of military SRAMs, IDT provides unexcelled performance and quality levels. Military SRAMs are manufactured in strict conformance with all requirements of MIL-STD-883 and are available as military SMD devices. In anticipation of military radiation resistance requirements, all devices are offered with special radiation processing and guarantees. In addition, our commercial products benefit by sharing most processing steps with military devices.

PACKAGE OPTIONS

Our commitment to technology extends to advanced, cost-effective packaging techniques. IDT's SRAMs are available in a wide variety of packages in commercial and military temperature ranges including:

- — surface-mount SOJ and SOIC plastic packages;
- —plastic and ceramic DIPs;
- —ceramic LCCs.

This constantly expanding offering of packages is in response to critical second-level interconnect issues confronting the system designer.

IDT MEANS SRAM LEADERSHIP

IDT's commitment to leading-edge technology and performance of CEMOS assures the availability of SRAMs compatible with the demanding needs of today's high-speed systems. Look to IDT for performance, technology and quality solutions to memory system problems.

CEMOS is a trademark of Integrated Device Technology, Inc.

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STATIC RAM PRODUCTS

CEMOS STATIC RAMS WITH POWER DOWN

Integrated Device Technology, Inc.

CMOS STATIC RAM
16K (2K X 8 BIT)

IDT6116SA
IDT6116LA

FEATURES:

- Optimized for fast RISC processors including the IDT79R3000
- High-speed
  - — Military: 20/25/35/45/55/70/90/120/150ns (max.)
  - — Commercial: 15/20/25/35/45ns (max.)
- Low-power operation
  - — IDT6116SA
    Active: 180mW (typ.)
    Standby: 100µW (typ.)
  - — IDT6116LA
    Active: 160mW (typ.)
    Standby: 20µW (typ.)
- Battery backup operation - 2V data retention voltage (LA version only)
- Produced with advanced CEMOS™ high-performance technology
- CEMOS process virtually eliminates alpha particle soft-error rates
- Single 5V (± 10%) power supply
- Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Available in standard 24-pin DIP, 24-pin THINDIP and plastic DIP, 24-, 28- and 32-pin LCC, 24-pin SOIC and 24-lead CERPACK
- Military product compliant to MIL-STD-833, Class B
- Standard Military Drawing# 84036 is listed on this function. Refer to Section 2/page 2-4

DESCRIPTION:

The IDT6116SA/LA is a 16,384-bit high-speed static RAM organized as 2K x 8. It is fabricated using IDT's high-performance, high-reliability technology - CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective alternative to bipolar and fast NMOS memories. Timing parameters have been specified to meet the speed demands of the fastest IDT79R3000 RISC processors.

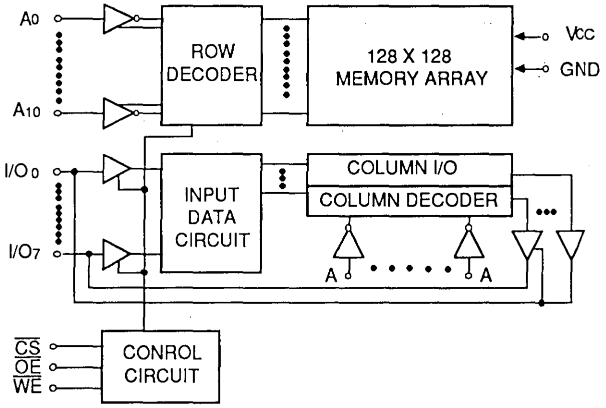
Access times as fast as 15ns are available with maxim power consumption of only 666mW. The circuit also offers a reduced power standby mode. When $\overline{\text{CS}}$ goes high, the circuit will automatically go to, and remain in, a standby power mode, as long as $\overline{\text{CS}}$ remains high. In the standby mode, the low-power device consumes less than 20µW typically. This capability provides significant system level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1µW to 4µW operating off a 2V battery.

All inputs and outputs of the IDT6116SA/LA are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation, providing equal access and cycle times for ease of use.

The IDT6116SA/LA is packaged in 24-pin 600 and 300 mil plastic or ceramic DIP, 24-, 28- and 32-pin leadless chip carriers, 24-lead CERPACK, and a 24-lead gull-wing SOIC, providing high board-level packing densities.

Military grade product is manufactured in compliance to the latest version of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



2954 drw 02

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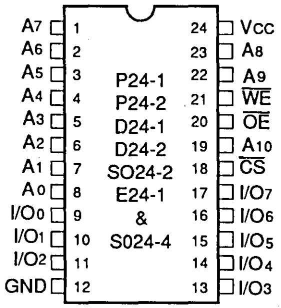
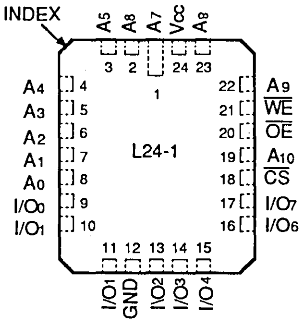
PIN CONFIGURATIONS



2954 drw 01

DIP/SOIC/CERPACK/SOJ
TOP VIEW

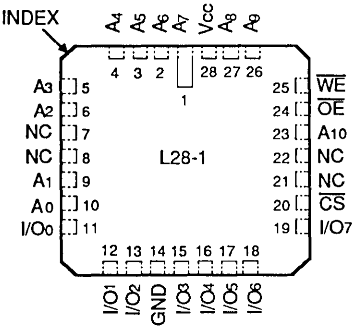


2954 drw 03

24-PIN LCC
TOP VIEW

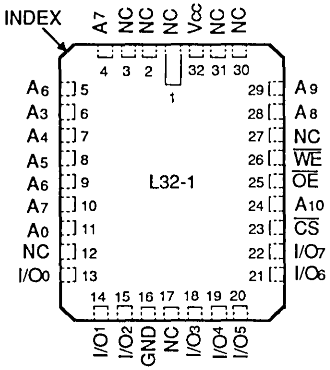
PIN NAMES

A_0- A_{10}	Address	$\overline{\text{WE}}$	Write Enable
I/O_0 - I/O_7	Data Input/Output	$\overline{\text{OE}}$	Output Enable
$\overline{\text{CS}}$	Chip Select	GND	Ground
Vcc	Power		



2954 drw 05

28-PIN LCC
TOP VIEW



2954 drw 04

32-PIN LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to + 7.0	-0.5 to + 7.0	V
T_A	Operating Temperature	0 to + 70	-55 to + 125	°C
T_{BIAS}	Temperature Under Bias	-55 to + 125	-65 to + 135	°C
T_{STG}	Storage Temperature	-55 to + 125	-65 to + 150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	3.5	6.0	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V
CL	Output Load	—	—	30	pF

NOTE:

1. VIL = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS

Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions		IDT6116SA Min.	IDT6116SA Typ.[1]	IDT6116SA Max.	IDT6116LA Min.	IDT6116LA Typ.[1]	IDT6116LA Max.	Unit
|ILI|	Input Leakage Current	Vcc = Max., VIN = GND to Vcc	MIL.	—	—	10	—	—	10	µA
			COM'L.	—	—	5	—	—	2	
|ILO|	Output Leakage Current	Vcc = Max. $\overline{CS}$ = VIH, VOUT = GND to Vcc	MIL.	—	—	10	—	—	5	µA
			COM'L.	—	—	5	—	—	2	
VOL	Output Low Voltage	IOL = 8mA, Vcc = Min.		—	—	0.4	—	—	0.4	V
VOH	Output High Voltage	IOH = -4mA, Vcc = Min.		2.4	—	—	2.4	—	—	V

NOTE:

1. Typical limits are at Vcc = 5.0V, + 25°C ambient.

AC ELECTRICAL CHARACTERISTICS [1]

Vcc = 5.0V ± 10%, VLC = 0.2V, VHC = Vcc - 0.2V

Symbol	Parameter	Power	6116SA15[2] 6116LA15[2]		6116SA20 6116LA20		6116SA25 6116LA25		6116SA35 6116LA35		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
ICC1	Operating Power Supply Current, $\overline{CS}$ = VIL, Outputs Open, Vcc = Max., f = 0	SA	125	—	110	130	100	110	80	90	mA
		LA	115	—	100	120	90	105	75	85	
ICC2	Dynamic Operating Current, $\overline{CS}$ = VIL, Vcc = Max., Outputs Open, f = fMAX[4]	SA	150	—	130	150	120	135	100	115	mA
		LA	140	—	120	140	110	125	95	105	
ISB	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ VIH, Vcc = Max., Outputs Open, f = fMAX[4]	SA	40	—	40	50	40	45	25	35	mA
		LA	35	—	35	45	35	40	25	30	
ISB1	Full Standby Power Supply Current (CMOS Level), $\overline{CS}$ ≥ VHC, Vcc = Max., VIN ≥ VHC or VIN ≤ VLC, f = 0	SA	2	—	2	10	2	10	2	10	mA
		LA	0.1	—	0.1	0.9	0.1	0.9	0.1	0.9	

NOTES:

1. All values are maximum guaranteed values.
2. 0°C to + 70°C temperature range only.
3. -55°C to + 125°C temperature range only.
4. fMAX = 1/tRC

AC ELECTRICAL CHARACTERISTICS (1) (Continued)

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Power	6116SA45 6116LA45		6116SA55(3) 6116LA55(3)		6116SA70(3) 6116LA70(3)		6116SA90(3) 6116LA90(3)		6116SA120(3) 6116LA120(3)		6116SA150(3) 6116LA150(3)		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current, $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0	SA	80	90	—	90	—	90	—	90	—	90	—	90	mA
		LA	75	85	—	85	—	85	—	85	—	85	—	85	
I_{CC2}	Dynamic Operating Current, $\overline{CS}$ = V_{IL}, V_{CC} = Max., Outputs Open, f = f_{MAX}(4)	SA	100	100	—	100	—	100	—	100	—	1005	—	90	mA
		LA	90	95	—	90	—	90	—	85	—	85	—	85	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}(4)	SA	25	25	—	25	—	25	—	25	—	25	—	25	mA
		LA	20	20	—	20	—	20	—	25	—	15	—	15	
I_{SB1}	Full Standby Power Supply Current (CMOS Level), $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0	SA	2	10	—	10	—	10	—	10	—	10	—	10	mA
		LA	0.1	0.9	—	0.9	—	0.9	—	0.9	—	0.9	—	0.9	

NOTES:
1. All values are maximum guaranteed values.
2. 0°C to + 70°C temperature range only.
3. -55°C to + 125°C temperature range only.
4. f_{MAX} = 1/t_{RC}

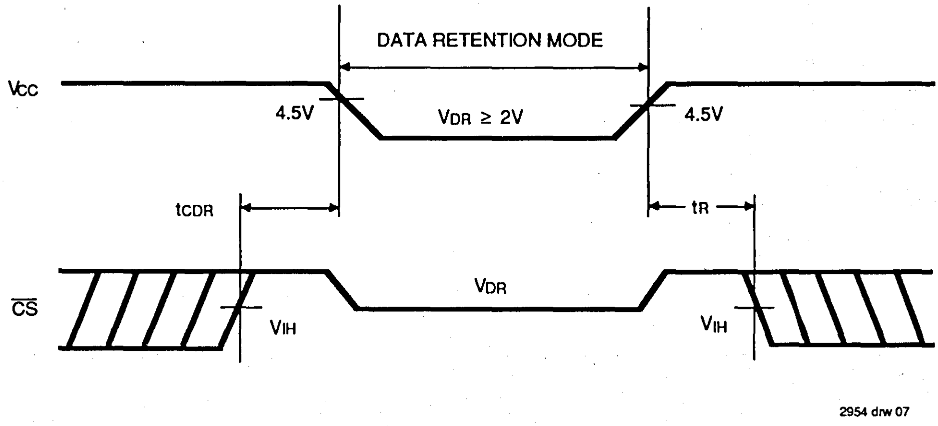
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(LA Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Conditions		Min.	Typ.(1) Vcc @ 2.0V	Typ.(1) Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS}$ ≥ V_{HC} V_{IN} ≥ V_{HC} or ≤ V_{LC} Retention Time	MIL.	—	0.5	1.5	200	300	µA
			COM'L.	—	0.5	1.5	20	30	
t_{CDR}(3)	Data Deselect to Data			—	0	—	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	—	—	ns
$\lvert I_{LI} \rvert$	Input Leakage Current			—	—	—	2	2	µA

NOTES:
1. T_A = + 25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed, but not tested.

LOW Vcc DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

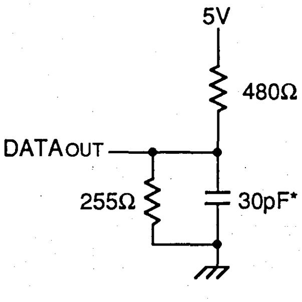


Figure 1. Output Load

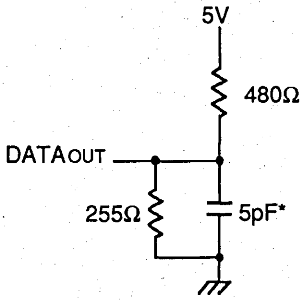


Figure 2. Output Load
(for tOLZ, tCLZ, tOHZ,
tWHZ, tCHZ, tOW)

2954 drw 08

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, All Temperature Ranges)

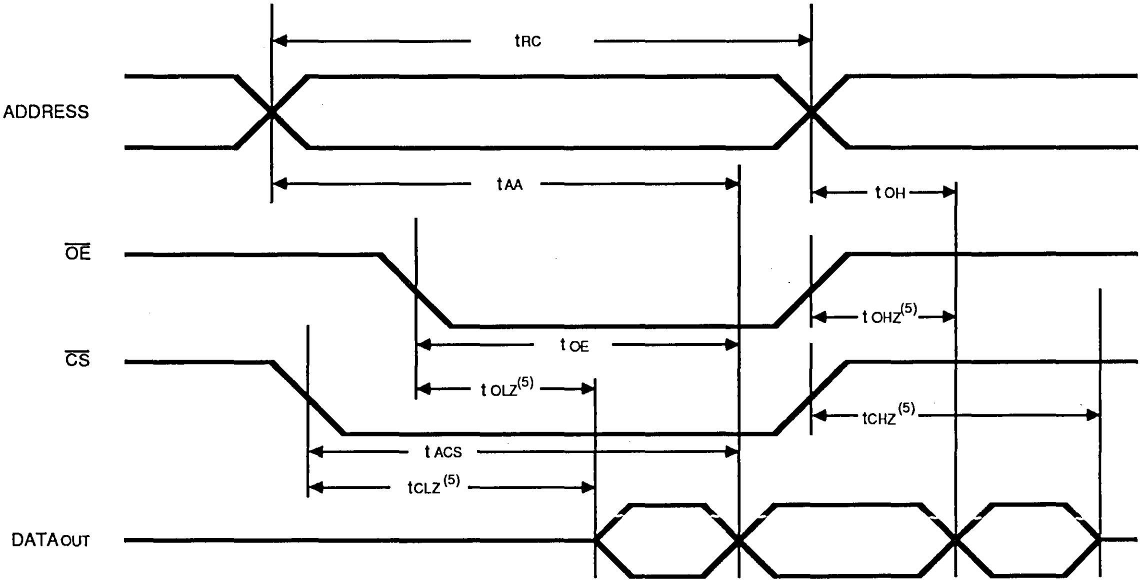
Symbol	Parameter	6116SA15(1) 6116LA15(1)		6116SA20 6116LA20		6116SA25 6116LA25		6116SA35 6116LA35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	15	—	20	—	25	—	35	—	ns
t_{AA}	Address Access Time	—	15	—	19	—	25	—	35	ns
t_{ACS}	Chip Select Access Time	—	15	—	20	—	25	—	35	ns
t_{CLZ}	Chip Select to Output in Low Z(3)	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	10	—	10	—	13	—	20	ns
t_{OLZ}	Output Enable to Output in Low Z(3)	0	—	0	—	5	—	5	—	ns
t_{CHZ}	Chip Deselect to Output in High Z(3)	—	10	—	11	—	12	—	15	ns
t_{OHZ}	Output Disable to Output in High Z(3)	—	8	—	8	—	10	—	13	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	5	—	5	—	ns

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, All Temperature Ranges) (Continued)

Symbol	Parameter	6116SA45 6116LA45		6116SA55(2) 6116LA55(2)		6116SA70(2) 6116LA70(2)		6116SA90(2) 6116LA90(2)		6116SA120(2) 6116LA120(2)		6116SA150(2) 6116LA150(2)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t_{RC}	Read Cycle Time	45	—	55	—	70	—	90	—	120	—	150	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	70	—	90	—	120	—	150	ns
t_{ACS}	Chip Select Access Time	—	45	—	50	—	65	—	90	—	120	—	150	ns
t_{CLZ}	Chip Select to Output in Low Z(3)	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	25	—	40	—	50	—	60	—	80	—	100	ns
t_{OLZ}	Output Enable to Output in Low Z(3)	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}	Chip Deselect to Output in High Z(3)	—	20	—	30	—	35	—	40	—	40	—	40	ns
t_{OHZ}	Output Disable to Output in High Z(3)	—	15	—	30	—	35	—	40	—	40	—	40	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns

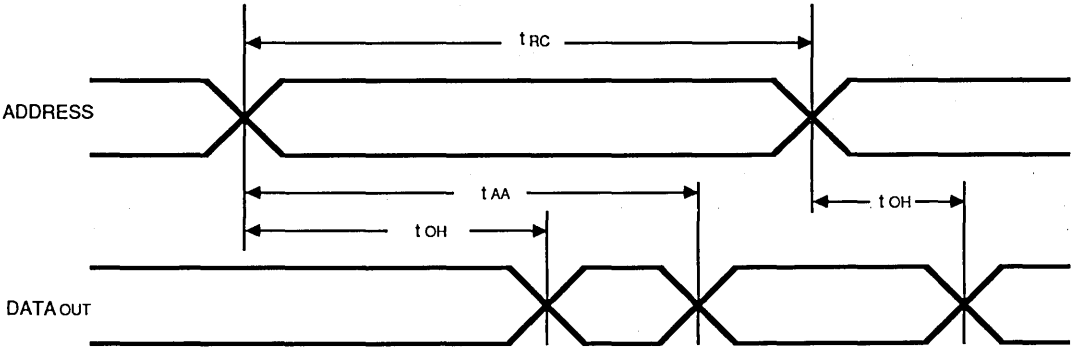
NOTES:
1. 0°C to + 70°C temperature range only.
2. -55°C to + 125°C temperature range only.
3. This parameter guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1[1]



2954 drw 09

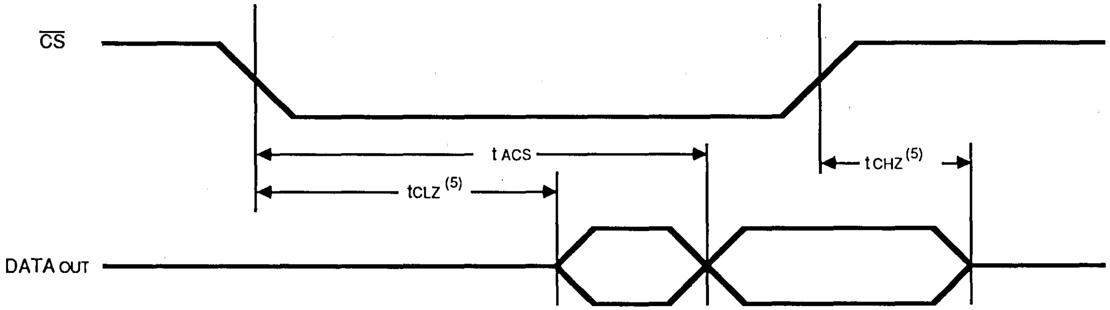
TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



2954 drw 10

NOTE:
1. $\overline{WE}$ is high for read cycle.
2. Device is continously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state with 5pF load (including scope and jig.)

TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



2954 drw 11

NOTE:
1. $\overline{WE}$ is high for read cycle.
2. Device is continously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state with 5pF load (including scope and jig.)

AC ELECTRICAL CHARACTERISTICS (Vcc = 5V ± 10%, All Temperature Ranges)

		6116SA15[1] 6116LA15[1]		6116SA20 6116LA20		6116SA25 6116LA25		6116SA35 6116LA35		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
WRITE CYCLE										
tWC	Write Cycle Time	15	—	20	—	25	—	35	—	ns
tCW	Chip Select to End of Write	13	—	15	—	17	—	25	—	ns
tAW	Address Valid to End of Write	14	—	15	—	17	—	25	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	12	—	12	—	15	—	20	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tOHZ	Output Disable to Output in High Z[3]	—	8	—	8	—	10	—	13	ns
tWHZ	Write to Output in High Z[3]	—	7	—	8	—	16	—	20	ns
tDW	Data to Write Time Overlap	12	—	12	—	13	—	15	—	ns
tDH	Data Hold from Write Time[4]	0	—	0	—	0	—	0	—	ns
tOW	Output Active from End of Write [3,4]	0	—	0	—	0	—	0	—	ns

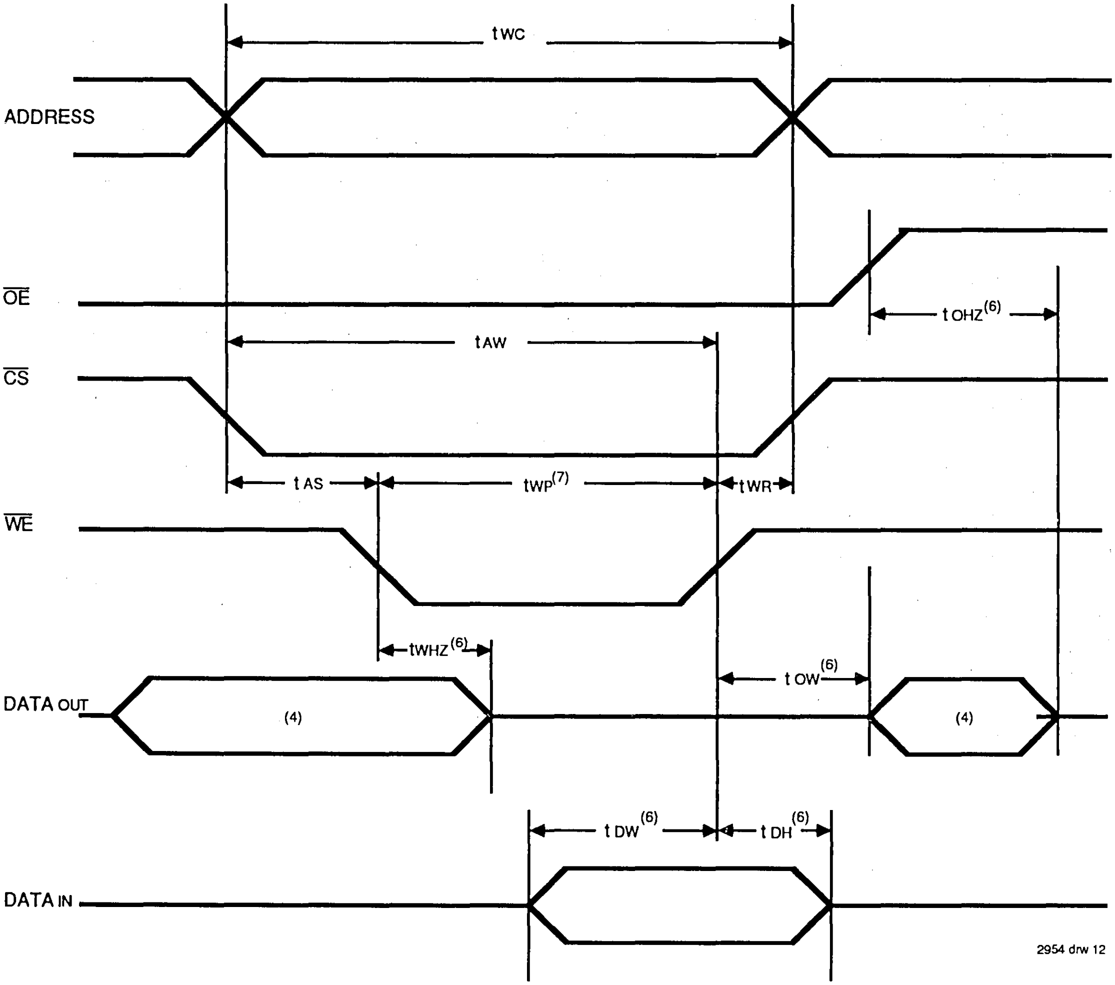
NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operation conditions. Although tDH and tow values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tow.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5V ± 10%, All Temperature Ranges) (Continued)

Symbol	Parameter	6116SA45 6116LA45		6116SA55(2) 6116LA55(2)		6116SA70(2) 6116LA70(2)		6116SA90(2) 6116LA90(2)		6116SA120(2) 6116LA120(2)		6116SA150(2) 6116LA150(2)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE														
tWC	Write Cycle Time	45	—	55	—	70	—	90	—	120	—	150	—	ns
tCW	Chip Select to End of Write	30	—	40	—	40	—	55	—	70	—	90	—	ns
tAW	Address Valid to End of Write	30	—	45	—	65	—	80	—	105	—	120	—	ns
tAS	Address Set-up Time	0	—	5	—	15	—	15	—	20	—	20	—	ns
tWP	Write Pulse Width	25	—	40	—	40	—	55	—	70	—	90	—	ns
tWR	Write Recovery Time	0	—	5	—	5	—	5	—	5	—	10	—	ns
tOHZ	Output Disable to Output in High Z(3)	—	25	—	30	—	35	—	40	—	40	—	40	ns
tWHZ	Write to Output in High Z(3)	—	25	—	30	—	35	—	40	—	40	—	40	ns
tDW	Data to Write Time Overlap	20	—	25	—	30	—	30	—	35	—	40	—	ns
tDH	Data Hold from Write Time(4)	0	—	5	—	5	—	5	—	5	—	10	—	ns
tOW	Output Active from End of Write(3,4)	0	—	0	—	0	—	0	—	0	—	0	—	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operation conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.

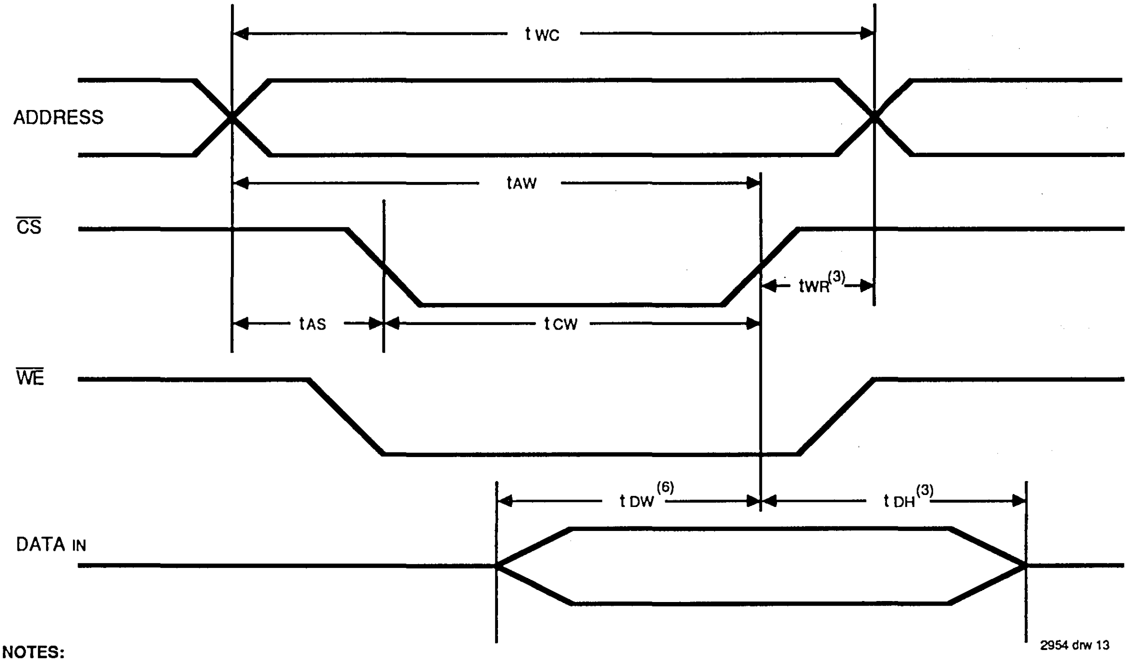
TIMING WAVEFORM OF WRITE CYCLE NO. 1, (WE CONTROLLED TIMING) (1, 2, 3, 7)



NOTES:

1. WE must be high during all address transitions.
2. A write occurs during the overlap (tCW or tWP) of a low CS and a low WE.
3. tWR is measured from the earlier of CS or WE going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and the input signals must not be applied.
5. If the CS low transition occurs simultaneously with or after the WE low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state wih a 5pF load (includng scope and jig).
7. If OE is low during a WE controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If OE is high during a WE controlled write cycle, this requirement does not apply and the write pulse can be a short as the specified tWP.

TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING) (1, 2, 3, 5)



NOTES:

1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{CW} or t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and the input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state wih a 5pF load (includng scope and jig).
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be a short as the specified t_{WP}.

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O
Standby	H	X	X	High Z
Read	L	L	H	$DATA_{OUT}$
Read	L	H	H	High Z
Write	L	X	L	$DATA_{IN}$

CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:

1. This parameter is determined by device characterization, but is not production tested.

THERMAL RESISTANCE (Typical)

Package	Pin Count	ΦJA	ΦJC	Unit
300 Mil Plastic DIP	24	54-58	28-32	°C/ WATT
600 Mil Plastic DIP	24	53-56	25-30	
300 Mil CERDIP	24	48-52	24-28	
600 Mil CERDIP	24	50-55	17-25	
Flatpack	24	85-90	24-28	
LCC	24	85-110	30-45	
LCC	28	85-90	28-35	
LCC	32	80-90	25-35	
SOIC, SOJ	24	45-70	25-30	

ORDERING INFORMATION

IDT	XXXX	A	999	A	A
	Device Type	Power	Speed	Package	Process/ Temperature Range

Process/Temperature Range:

Blank	Commercial (0°C to +70°C)
B	Military (-55°C to + 125°C) Compliant to MIL-STD-883, Class B

Package:

TP	Plastic DIP (300 mil)
P	Plastic DIP (600 mil)
TD	CERDIP (300 mil)
D	CERDIP (600 mil)
L	Leadless Chip Carrier (Indicate 24-,28- or 32-pin)
SO	Small Outline IC (Gull-Wing Bend)
E	CERPACK
Y	SOJ (J-Bend)

Speed (Speed in Nanoseconds):

15	Commercial Only
20	Mil./Comm.
25	Mil./Comm.
35	Mil./Comm.
45	Mil./Comm.
55	Military Only
70	Military Only
90	Military Only
120	Military Only
150	Military Only

Power:

LA	Low Power
SA	Standard Power

Device Type:

6116	16K (2K x 8-Bit) Static RAM

2954 drw 14

Integrated Device Technology, Inc.

CMOS STATIC RAM
256K (64K x 4-BIT)

ADVANCED INFORMATION
IDT61298

FEATURES:

- Fast Output Enable ($\overline{OE}$) pin available for added system flexibility
- High speed (equal access and cycle times)
  - — Military: 25/35/45/55 (max.)
  - — Commercial: 20/25/35/45ns (max.)
- Low power consumption
  - — IDT61298S
    Active: 400mW (typ.)
    Standby: 400µw (typ.)
  - — IDT61298L
    Active: 350mW (typ.)
    Standby: 100µw (typ.)
- Battery back-up operation
  - — 2V data retention (L version only)
- JEDEC standard pinout
- 300 Mil 28-pin DIP, 300 Mil28-pin SOJ, and 300 Mil 28-pin LCC
- Produced with advanced CEMOS™ technology
- Bidirectional data inputs and outputs
- Inputs/Outputs TTL-compatible
- Three-state outputs
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

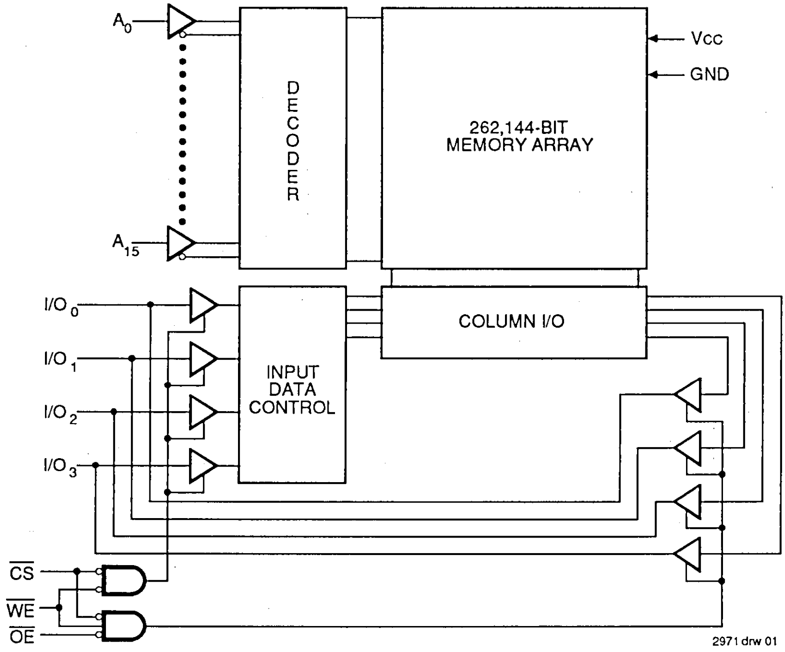
The IDT61298 is a 262,144-bit high-speed static RAM organized as 64K x 4. It is fabricated using IDT's high-performance, high-reliability technology – CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for memory intensive applications.

The IDT61298 features two memory control functions: Chip Select ($\overline{CS}$) and Output Enable ($\overline{OE}$). These two functions greatly enhance the IDT61298's overall flexibility in high-speed memory applications.

Access times as fast as 20ns are available with typical power consumption of only 350mW. The IDT61298 offers a reduced power standby mode, ISB1, which enables the designer to considerably reduce device power requirements. This capability significantly decreases system power and cooling levels, while greatly enhancing system reliability. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 100µW when operating from a 2V battery.

All inputs and outputs are TTL-compatible and the device operates from a single 5 volt supply. Fully static asynchronous

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

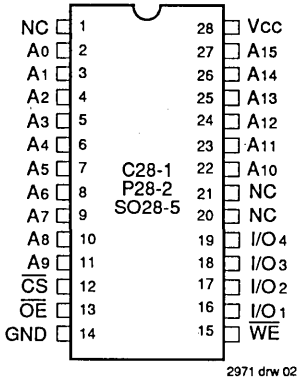
DESCRIPTION (Continued)

circuitry, along with matching access and cycle times, favor the simplified system design approach.

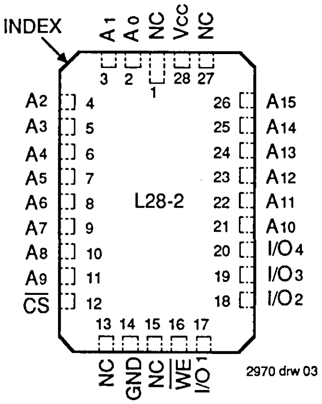
The IDT61298 is packaged in a 28-pin sidebraze or plastic 300mil DIP, an SOJ, plus an LCC, providing improved board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



DIP/SOJ
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A0–A15	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O1–4	Data Input/Output
VCC	Power
GND	Ground

2971 tbl 01

TRUTH TABLE(1)

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Standby	H	X	X	High Z	Standby
Read	L	H	L	DOUT	Active
Write	L	L	X	DIN	Active
Read	L	H	H	High Z	Active

NOTE:
2971 tbl 02

1. H = VIH, L = VIL, X = Don't Care

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

NOTE:
2971 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	11	pF
COUT	Output Capacitance	VOUT = 0V	11	pF

NOTE:
2975 tbl 04

1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2971 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE:

2971 tbl 06

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	61298S20 61298L20		61298S25 61298L25		61298S35 61298L35		61298S45 61298L45		61298S55 61298L55		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = 0[2]	S	110	—	100	110	100	110	100	110	—	110	mA
		L	100	—	90	100	90	100	90	100	—	100	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = f_{MAX}[2]	S	160	—	150	160	150	160	150	160	—	160	mA
		L	140	—	130	140	130	140	130	140	—	140	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}[2]	S	35	—	35	35	35	35	35	35	—	35	mA
		L	20	—	20	20	20	20	20	20	—	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., f = 0[2]	S	30	—	30	35	30	35	30	35	—	35	mA
		L	1.5	—	1.5	4.5	1.5	4.5	1.5	4.5	—	4.5	

NOTES:

2971 tbl 07

1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2971 tbl 08

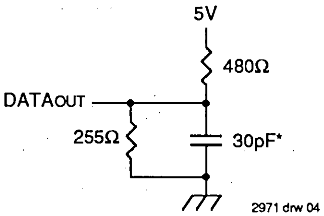


Figure 1. Output Load

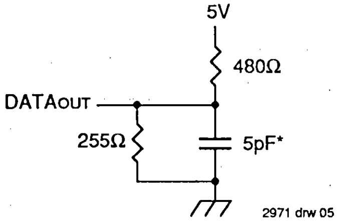


Figure 2. Output Load
(for tCLZ, tOLZ, tCHZ, tOHZ, tOW, tWHZ)

*Includes scope and jig capacitances

DC ELECTRICAL CHARACTERISTICS

Vcc = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT61298S			IDT61298L			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
|ILI|	Input Leakage Current	Vcc = Max., VIN = GND to Vcc	MIL COM'L	— —	— —	10 5	— —	— —	5 2	µA
|ILO|	Output Leakage Current	Vcc = Max., $\overline{CS}$ = VIH, VOUT = GND to Vcc	MIL COM'L	— —	— —	10 5	— —	— —	5 2	µA
VOL	Output Low Voltage	IOL = 8mA, Vcc = Min. IOL = 10mA, Vcc = Min.		 —	— —	0.4 0.5	— —	— —	0.4 0.5	V
VOH	Output High Voltage	IOH = -4mA, Vcc = Min.		2.4	—	—	2.4	—	—	V

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) VHC = Vcc - 0.2V

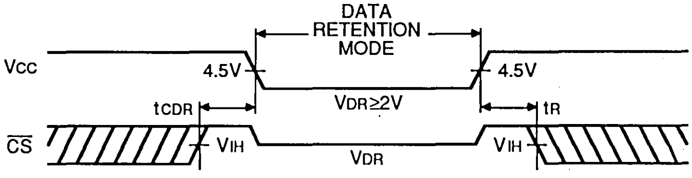
Symbol	Parameter	Test Condition		Min.	Typ.[(1)] Vcc @		Max. Vcc @		Unit
					2.0v	3.0V	2.0V	3.0V	
VDR	Vcc for Data Retention	—		2.0	—	—	—	—	V
ICCDR	Data Retention Current	$\overline{CS}$ ≥ VHC	MIL. COM'L.	— —	50 50	75 75	2000 500	3000 750	µA
tCDR[(3)]	Chip Deselect to Data Retention Time			0	—	—	—	—	ns
tR[(3)]	Operation Recovery Time			tRC[(2)]	—	—	—	—	ns
|ILI|[(3)]	Input Leakage Current			—	—	—	2	2	µA

NOTES:

2971 tbl 10

1. TA = +25°C.
2. tRC = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

LOW Vcc DATA RETENTION WAVEFORM



2971 drw 03

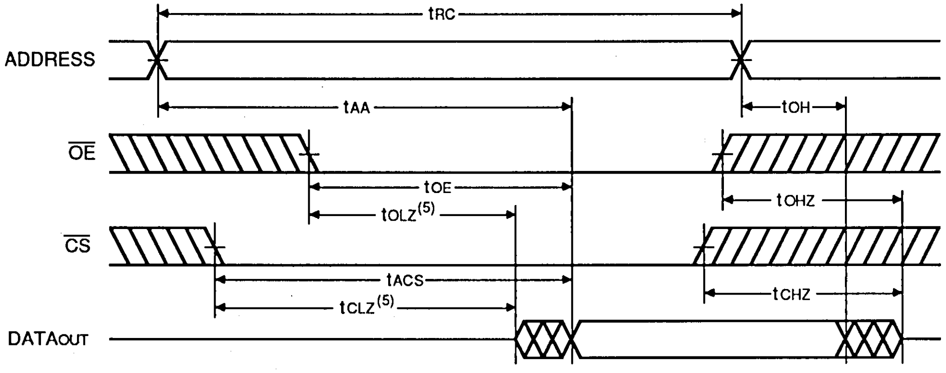
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	61298S20(1) 61298L20(1)		61298S25(2) 61298L25(2)		61298S35 61298L35		61298S45 61298L45		61298S55(2) 61298L55(2)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t_{RC}	Read Cycle Time	20	—	25	—	35	—	45	—	55	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	35	—	45	—	55	ns
t_{ACS}	Chip Select Access Time	—	20	—	25	—	35	—	45	—	55	ns
t_{CLZ}(3)	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	13	—	15	—	25	—	30	—	35	ns
t_{OLZ}(3)	Output Enable to Output in Low Z	2	—	3	—	5	—	5	—	5	—	ns
t_{CHZ}(3)	Chip Select to Output in High Z	—	10	—	13	—	15	—	20	—	25	ns
t_{OHZ}(3)	Output Disable to Output in High Z	—	10	—	13	—	15	—	15	—	20	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}(3)	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}(3)	Chip Deselect to Power Down Time	—	20	—	25	—	35	—	45	—	55	ns
Write Cycle												
t_{WC}	Write Cycle Time	20	—	20	—	30	—	40	—	50	—	ns
t_{CW}	Chip Select to End of Write	15	—	20	—	30	—	40	—	50	—	ns
t_{AW}	Address Valid to End of Write	15	—	20	—	30	—	40	—	50	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	15	—	20	—	30	—	40	—	50	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}(3)	Write Enable to Output in High Z	—	10	—	11	—	15	—	20	—	25	ns
t_{DW}	Data Valid to End of Write	11	—	15	—	20	—	25	—	30	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{OW}(3)	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

2971 tbl 11

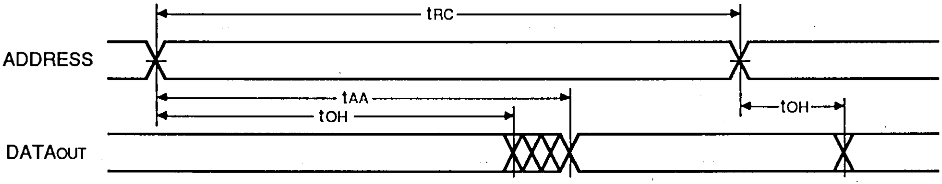
NOTES:
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. Preliminary data for militatry devices only.

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



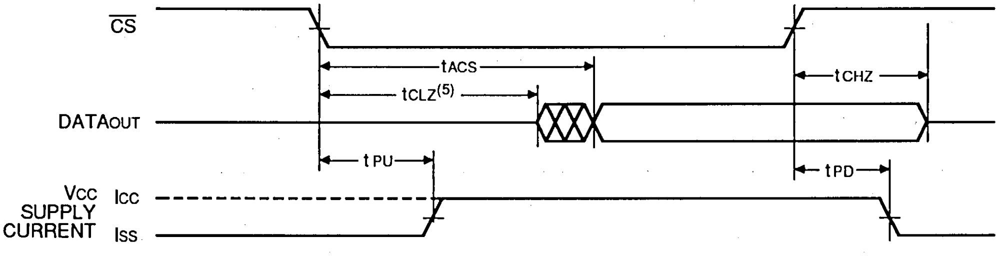
2971 drw 06

TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



2971 drw 07

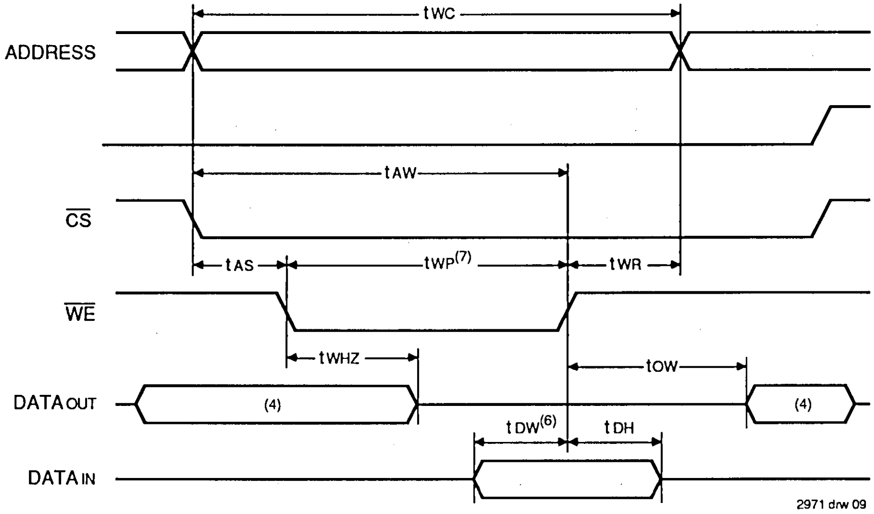
TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)



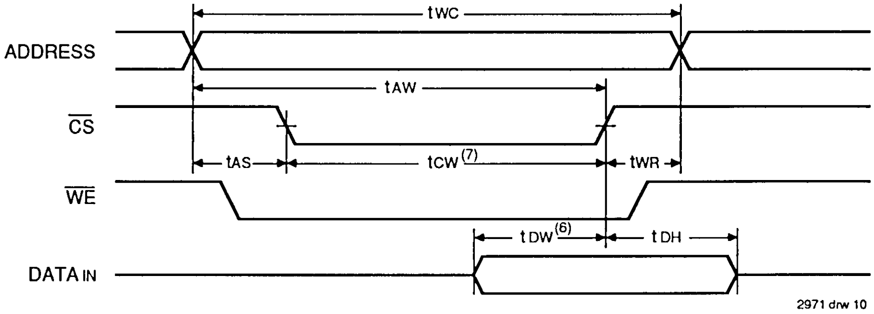
2971 drw 08

NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1,2,3,7)



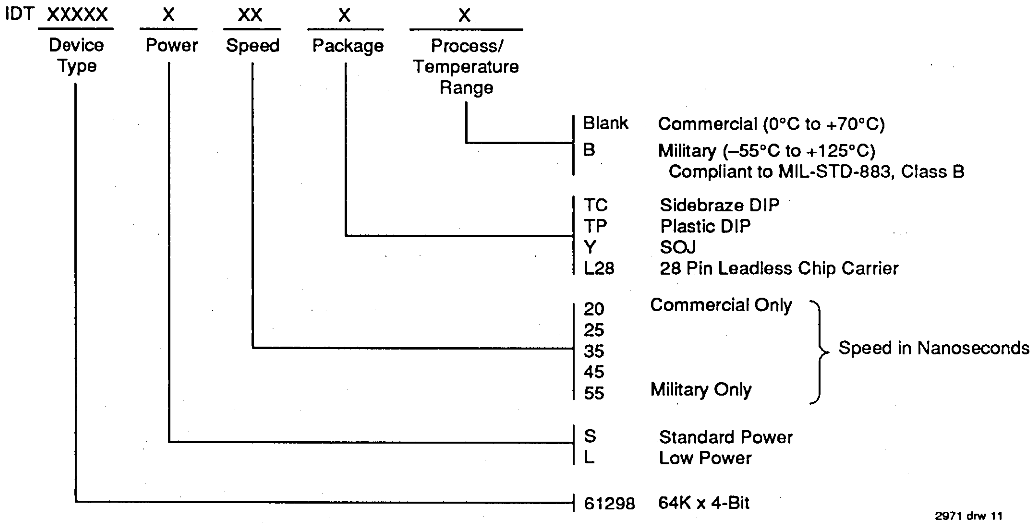
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1,2,3,5)



NOTES:

1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (tCW or tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the spectified tWP.

ORDERING INFORMATION



2971 drw 11

Integrated Device Technology, Inc.

CMOS STATIC RAM
16K (16K x 1-BIT)

IDT6167SA
IDT6167LA

FEATURES:

- High-speed (equal access and cycle time)
  - — Military: 15/20/25/35/45/55/70/85/100ns (max.)
  - — Commercial: 12/15/20/25/35ns (max.)
- Low power consumption
  - — IDT6167SA
    Active: 200mW (typ.)
    Standby: 100μW (typ.)
  - — IDT6167LA
    Active: 150mW (typ.)
    Standby: 10μW (typ.)
- Battery backup operation — 2V data retention voltage (IDT6167LA only)
- Available in 20-pin CERDIP and plastic DIP, 20-pin CERPACK, 20-pin SOIC and 20-pin leadless chip carrier
- Produced with advanced CEMOS™ high-performance technology
- CEMOS process virtually eliminates alpha particle soft-error rates
- Separate data input and output
- Single 5V (+10%) power supply
- Input and output directly TTL-compatible
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-84132 is listed on this function. Refer to Section 2/page 2-4

DESCRIPTION:

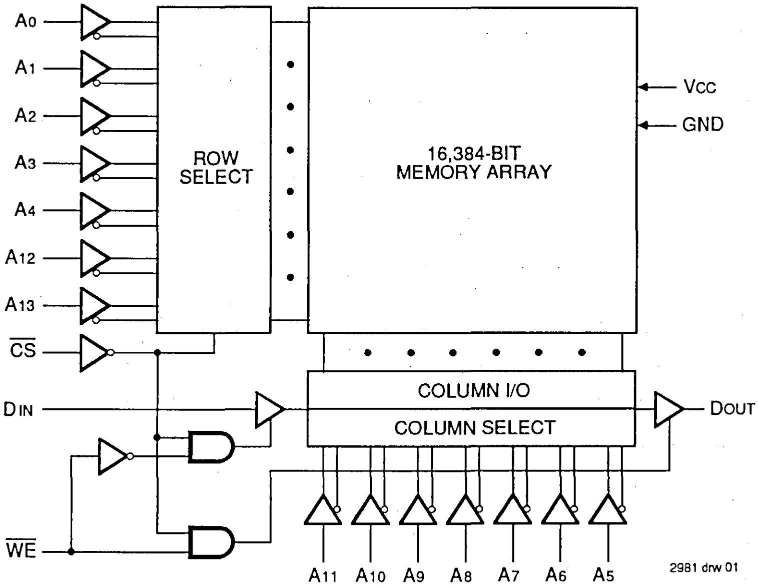
The IDT6167 is a 16,384-bit high-speed static RAM organized as 16K x 1. The part is fabricated using IDT's high-performance, high reliability technology — CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective alternative to bipolar and fast NMOS memories.

Access times as fast as 12ns are available with maximum power consumption of only 660mW. The circuit also offers a reduced power standby mode. When $\overline{\text{CS}}$ goes high, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{\text{CS}}$ remains high. In the standby mode, the device consumes less than 10μW, typically. This capability provides significant system-level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1μW operating off a 2V battery.

All inputs and the output of the IDT6167 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs.

The IDT6167 is packaged in a space-saving 20-pin, 300 mil Plastic DIP or CERDIP, plastic 20-pin SOIC or SOJ, 20-pin CERPACK and 20-pin leadless chip carrier, providing high board-level packing densities.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

DESCRIPTION (Continued)

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

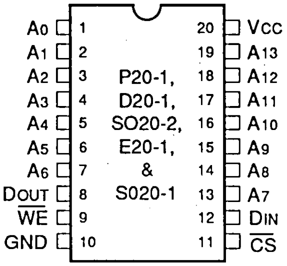
TRUTH TABLE [1]

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High Z	Standby
Read	L	H	DATAOUT	Active
Write	L	L	High Z	Active

NOTE: 2981 tbl 02

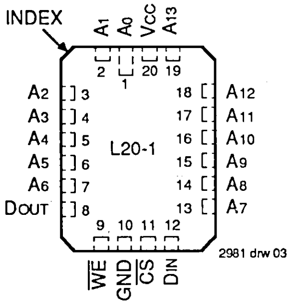
1. H = VIH, L = VIL, X = Don't Care.

PIN CONFIGURATIONS



2981 drw 02

DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

PIN NAMES

A0–A13	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
VCC	Power
DIN	DATAIN
DOUT	DATAOUT
GND	Ground

2981 tbl 01

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2981 tbl 05

1. VIL (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2981 tbl 06

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

NOTE: 2981 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	7	pF
COUT	Output Capacitance	VOUT = 0V	7	pF

NOTE: 2981 tbl 04

1. This parameter is determined by device characterization, but is not production tested.

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	6167SA12		6167SA/LA15		6167SA/LA25		6167SA/LA35		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0(3)	SA	90	—	90	90	90	90	90	90	mA
		LA	—	—	55	60	55	60	55	60	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}(3)	SA	140	—	120	130	100	110/100	100	100	mA
		LA	—	—	100	110	80/70	85/75	65	70	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, Outputs Open, V_{CC} = Max., f = f_{MAX}(3)	SA	50	—	50	50	35	35	35	35	mA
		LA	—	—	35	35	30/25	30/25	20	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max. V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0(3)	SA	10	—	5	10	5	10	5	10	mA
		LA	—	—	0.9	2	0.05	2/0.9	0.05	0.9	

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	6167SA/LA45		6167SA/LA55		6167SA/LA70		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0(3)	SA	—	90	—	90	—	90	mA
		LA	—	60	—	60	—	60	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}(3)	SA	—	100	—	100	—	100	mA
		LA	—	65	—	60	—	60	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, Outputs Open, V_{CC} = Max., f = f_{MAX}(3)	SA	—	35	—	35	—	35	mA
		LA	—	20	—	20	—	15	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max. V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0(3)	SA	—	10	—	10	—	10	mA
		LA	—	0.9	—	0.9	—	0.9	

NOTES:

2980 tbl 07

1. All values are maximum guaranteed values.
2. Also available: 85ns and 100ns Military devices.
3. f = f_{MAX} (All Inputs cycling at f = 1/t_{RC}). f = 0 means no address control lines change.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT6167SA		IDT6167LA		Unit
				Min.	Max.	Min.	Max.	
$\lvert I_{LI}\rvert$	Input Leakage Current	V_{CC} = Max.,	MIL	—	10	—	5	µA
		V_{IN} = GND to V_{CC}	COM'L	—	5	—	2	
$\lvert I_{LO}\rvert$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH},	MIL	—	10	—	5	µA
		V_{OUT} = GND to V_{CC}	COM'L	—	5	—	2	
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OL} = -4mA, V_{CC} = Min.		2.4	—	2.4	—	V

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

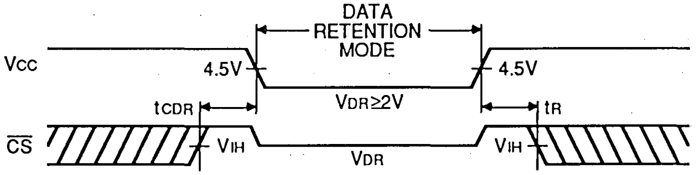
Symbol	Parameter	Test Condition		Min.	Typ.[1] V_{CC} @		Max. V_{CC} @		Unit
					2.0v	3.0V	2.0V	3.0V	
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS}$ ≥ V_{HC} VIN ≥ V_{HC} or ≤ V_{LC}	MIL.	—	0.5	1.0	200	300	µA
			COM'L.	—	0.5	1.0	20	30	
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	—	—	ns
$\lvert I_{LI}\rvert$[3]	Input Leakage Current			—	—	—	2	2	µA

NOTES:

2981 tbl 09

1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

LOW Vcc DATA RETENTION WAVEFORM



2981 drw 03

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2979 tbl 09

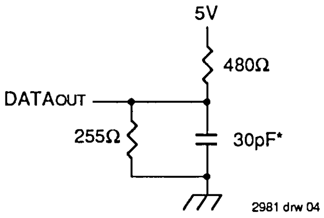


Figure 1. Output Load

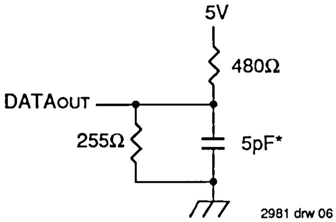


Figure 2. Output Load
(for tHZ, tLZ, tWZ and tOW)

*Includes scope and jig.

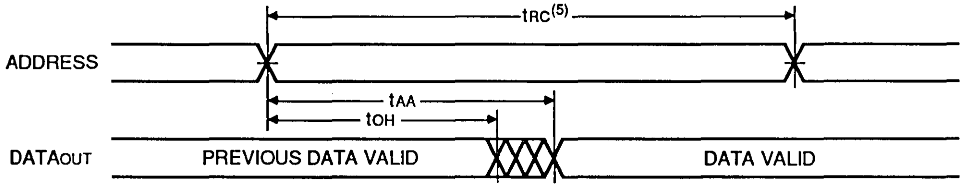
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

		6167SA12(1)		6167SA15 6167LA15		6167SA20/25 6167LA20/25		6167SA35/45(2) 6167LA35/45(2)		6167SA55(2)/70(2) 6167LA55(2)/70(2)		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	12	—	15	—	20/25	—	35/45	—	55/70	—	ns
tAA	Address Access Time	—	12	—	15	—	20/25	—	35/45	—	55/70	ns
tACS	Chip Select Access Time	—	12	—	15	—	20/25	—	35/45	—	55/70	ns
tOH	Output Hold from Address Change	3	—	3	—	5/5	—	5/5	—	5/5	—	ns
tLZ	Chip Deselct to Output in Low Z(3)	3	—	3	—	5/5	—	5/5	—	5/5	—	ns
tHZ	Chip Select to Output in High Z(3)	—	8	—	10	—	10/10	—	15/30	—	40/40	ns
tPU	Chip Select to Power Up Time(3)	0	—	0	—	0/0	—	0/0	—	0/0	—	ns
tPD	Chip Deselect to Power Down Time(3)	—	12	—	15	—	20/25	—	35/45	—	55/70	ns
Write Cycle												
tWC	Write Cycle Time	12	—	15	—	20/20	—	30/45	—	55/70	—	ns
tCW	Chip Select to End of Write	12	—	15	—	15/20	—	30/40	—	45/55	—	ns
tAW	Address Valid to End of Write	12	—	15	—	15/20	—	30/40	—	45/55	—	ns
tAS	Address Set-up Time	0	—	0	—	0/0	—	0/0	—	0/0	—	ns
tWP	Write Pulse Width	12	—	13	—	15/20	—	30/30	—	35/40	—	ns
tWR	Write Recovery Time	0	—	0	—	0/0	—	0/0	—	0/0	—	ns
tDW	Data Valid to End of Write	10	—	10	—	12/15	—	17/20	—	25/30	—	ns
tDH	Data Hold Time	0	—	0	—	0/0	—	0/0	—	0/0	—	ns
tWZ	Write Enable to Output in High Z(3)	—	6	—	7	—	8/8	—	15/30	—	40/40	ns
tOW	Output Active from End of Write(3)	0	—	0	—	0/0	—	0/0	—	0/0	—	ns

2981 tbl 11

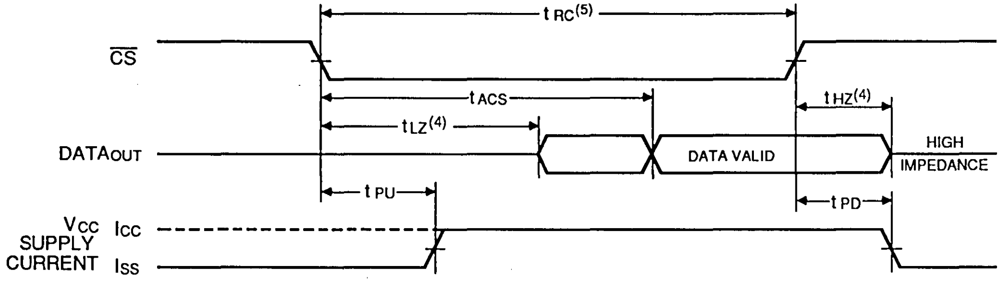
NOTES:
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only. Also available: 85ns and 100ns Military devices.
3. This parameter is guaranteed, but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1, 2)



2981 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 3)

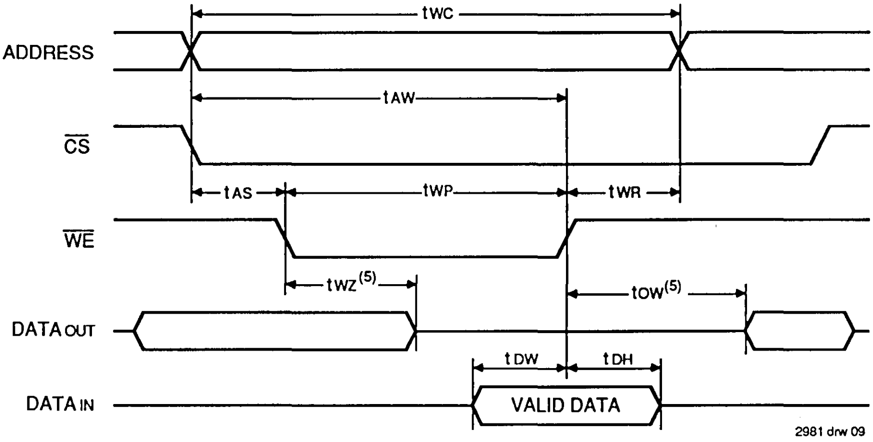


2981 drw 08

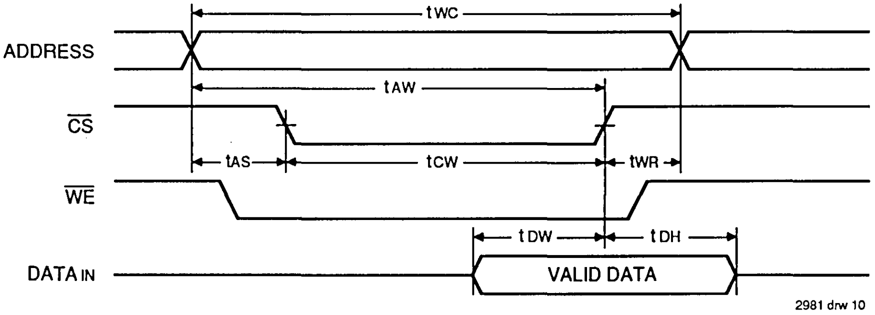
NOTES:

1. $\overline{WE}$ is High for READ cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincedent with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state with specified loadingiin Figure 2.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{\text{WE}}$ CONTROLLED TIMING)(1, 2, 3)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{\text{CS}}$ CONTROLLED TIMING)(1, 2, 3)



NOTES:

1. $\overline{\text{WE}}$ or $\overline{\text{CS}}$ must be inactive during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{\text{CS}}$ and a low $\overline{\text{WE}}$.
3. t_{WR} is measured from the earlier of $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high to the wnd of the write cycle.
4. If the $\overline{\text{CS}}$ low transition occurs simultaneously with or after the $\overline{\text{WE}}$ low transition, the outputs remain in the high impedance state.
5. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).

ORDERING INFORMATION

IDT	XXXX	X	XXX	XX	X
	Device Type	Power	Speed	Package	Process/ Temperature Range

Process/Temperature Range:

Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Package:

P	Plastic DIP
D	CERDIP
L	Leadless Chip Carrier
SO	Small Outline IC
E	CERPACK
Y	SOJ

Speed (Speed in Nanoseconds):

12	Commercial Only
15	
20	
25	
35	
45	Military Only
55	Military Only
70	Military Only
85	Military Only
100	Military Only

Power:

SA	Standard Power
LA	Low Power

Device Type:

6167	16K (16K x 1-Bit) CMOS Static RAM

2981 drw 11

Integrated Device Technology, Inc.

CMOS STATIC RAM
16K (4K x 4-BIT)

IDT6168SA
IDT6168LA

FEATURES:

- High-speed (equal access and cycle time)
  - — Military: 12/15/20/25/35/45/55/70/85/100ns (max.)
  - — Commercial: 10/12/15/20/25/35ns (max.)
- Low power consumption
  - — IDT6168SA
    Active: 225mW (typ.)
    Standby: 100μW (typ.)
  - — IDT6168LA
    Active: 225mW (typ.)
    Standby: 10μW (typ.)
- Battery backup operation—2V data retention voltage (IDT6168LA only)
- Available in high-density 20-pin ceramic or plastic DIP, 20-pin SOIC, 20-pin SOJ, 20-pin CERPACK and 20-pin leadless chip carrier
- Produced with advanced CEMOS™ high-performance technology
- CEMOS™ process virtually eliminates alpha particle soft-error rates
- Bidirectional data input and output
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state outputs
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-86705 is listed on this function. Refer to Section 2/page 2-4

DESCRIPTION:

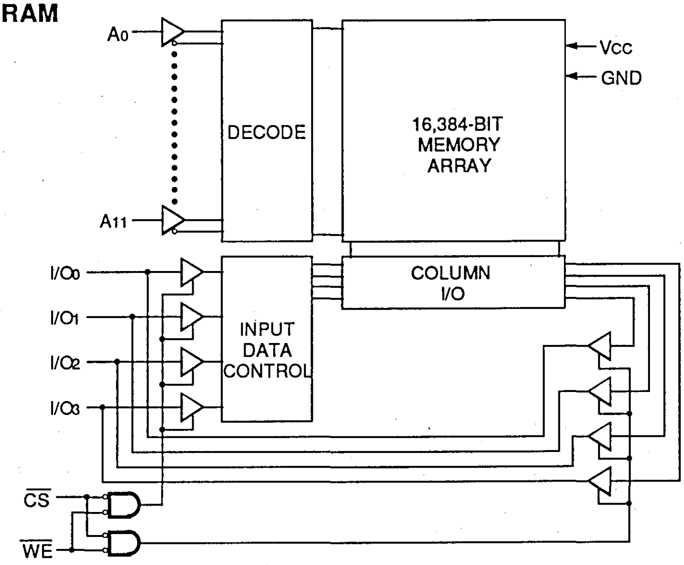
The IDT6168 is a 16,384-bit high-speed static RAM organized as 4K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for high-speed memory applications.

Access times as fast 10ns are available with maximum power consumption of only 550mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{CS}$ remains high. In the standby mode, the device consumes less than 10μW, typically. This capability provides significant system-level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1μW operating off a 2V battery. All inputs and outputs of the IDT6168 are TTL-compatible and operate from a single 5V supply.

The IDT6168 is packaged in either a space saving 20-pin, 300 mil ceramic or plastic DIP, 20-pin CERPACK, 20-pin SOIC, 20-pin SOJ, or 20-pin leadless chip carrier, providing high board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

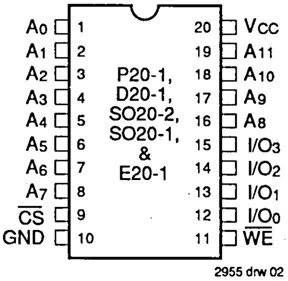
FUNCTIONAL BLOCK DIAGRAM



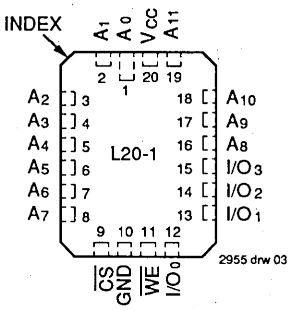
2955 drw 01

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP/SOIC/SOJ/CERPACK
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A_0–A_{11}	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
I/O0-3	Data Input/Output
Vcc	Power
GND	Ground

2955 tbl 01

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 2955 tbl 04
1. This parameter is determined by device characterization, but is not production tested.

TRUTH TABLE[1]

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High Z	Standby
Read	L	H	DOUT	Active
Write	L	L	DIN	Active

NOTE: 2955 tbl 02
1. H = V_{IH}, L = V_{IL}, X = Don't Care

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2955 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2955 tbl 05
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2955 tbl 06

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	6168SA10		6168SA12(4)		6168SA15(4)		6168SA20 6168LA20		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0(3)	SA	120	—	110	120	110	120	90	100	mA
		LA	—	—	—	—	—	—	70	80	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}(3)	SA	175	—	165	175	145	165	120	120	mA
		LA	—	—	—	—	—	—	100	110	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}(3)	SA	65	—	65	65	55	60	45	45	mA
		LA	—	—	—	—	—	—	30	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0(3)	SA	20	—	20	20	20	20	20	20	mA
		LA	—	—	—	—	—	—	0.5	5	

DC ELECTRICAL CHARACTERISTICS (Continued)(1)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	6168SA25 6168LA25		6168SA35 6168LA35		6168SA45/55 6168LA45/55		6168SA70(2) 6168LA70(2)		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0(3)	SA	90	100	90	100	—	100	—	100	mA
		LA	70	80	70	80	—	80	—	80	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}(3)	SA	110	120	100	110	—	110	—	110	mA
		LA	90	100	80	90	—	80	—	80	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}(3)	SA	35	45	30	35	—	35	—	35	mA
		LA	25	30	20	25	—	25/20	—	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0(3)	SA	2	10	2	10	—	10	—	10	mA
		LA	0.05	0.3	0.05	0.3	—	0.3	—	0.3	

NOTES:

2955 tbl 07

1. All values are maximum guaranteed values.
2. Also available 85 and 100ns military devices.
3. f = f_{MAX} (all inputs except Chip Select cycling at f = 1/t_{RC}). f = 0 means no address or control lines change.
4. Military values are preliminary only.

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Condition		IDT6168SA Min.	IDT6168SA Max.	IDT6168LA Min.	IDT6168LA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL COM'L	— —	10 2	— —	5 2	μA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL COM'L	— —	10 2	— —	5 2	μA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.			0.5	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	
V_{OH}	Output High Voltage	I_{OL} = -4mA, V_{CC} = Min.		2.4	—	2.4	—	V

2955 tbl 08

DATA RETENTION CHARACTERISTICS

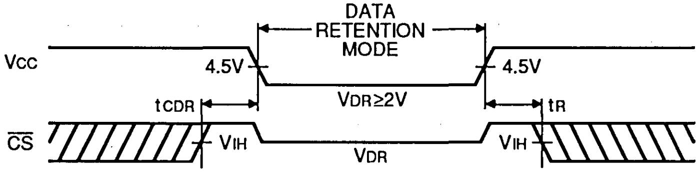
(LA Version Only)

Symbol	Parameter	Test Condition		IDT6168LA Min.	IDT6168LA Typ.(1)	IDT6168LA Max.	Unit
V_{DR}	V_{CC} for Data Retention	$\overline{CS}$ ≥ V_{CC} -0.2V V_{IN} ≥ V_{CC} -0.2V or ≤ 0.2V		2.0	—	—	V
I_{CCDR}	Data Retention Current		MIL.	— —	0.5(2) 1.0(3)	100(2) 150(3)	μA
			COM'L.	— —	0.5(2) 1.0(3)	20(2) 30(3)	μA
t_{CDR}(5)	Chip Deselect to Data Retention Time			0	—	—	ns
t_R(5)	Operation Recovery Time			t_{RC}(2)	—	—	ns

2955 tbl 09

NOTES:
1. T_A = +25°C.
2. at V_{CC} = 2V
3. at V_{CC} = 3V
4. t_{RC} = Read Cycle Time.
5. This parameter is guaranteed, but not tested.

LOW Vcc DATA RETENTION WAVEFORM



2955 drw 04

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2955 tbl 10

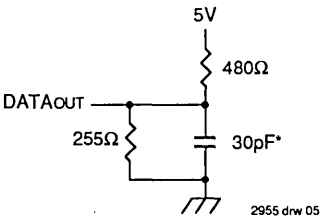


Figure 1. Output Load

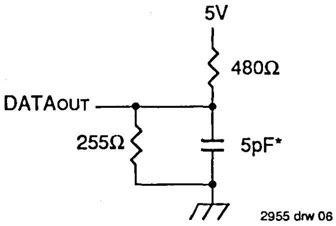


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ} and t_{OW})

*Includes scope and jig capacitances

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6168SA10[3]		6168SA12		6168SA15		6168SA20/25 6168LA20/25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	10	—	12	—	15	—	20/25	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	—	20/25	ns
t_{ACS}	Chip Select Access Time	—	10	—	12	—	15	—	20/25	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t_{LZ}	Chip Select to Output in Low Z[2]	3	—	3	—	3	—	5	—	ns
t_{HZ}	Chip Deselect to Output in High Z[2]	—	6	—	7	—	8	—	10	ns
t_{PU}	Chip Select to Power Up Time[2]	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Deselect to Power Down Time[2]	—	10	—	12	—	15	—	20/25	ns

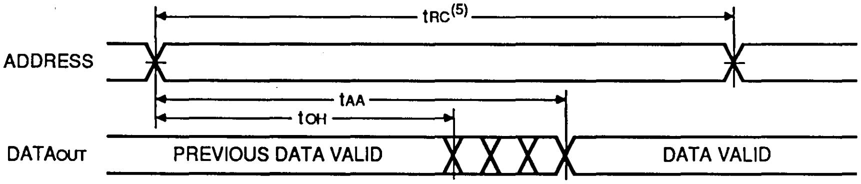
AC ELECTRICAL CHARACTERISTICS (Continued) (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6168SA35 6168LA35		6168SA45/55[1] 6168LA45/55[1]		6168SA70[1] 6168LA70[1]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	35	—	45/55	—	70	—	ns
t_{AA}	Address Access Time	—	35	—	45/55	—	70	ns
t_{ACS}	Chip Select Access Time	—	35	—	45/55	—	70	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{LZ}	Chip Select to Output in Low Z[2]	5	—	5	—	5	—	ns
t_{HZ}	Chip Deselect to Output in High Z[2]	—	15	—	25	—	30	ns
t_{PU}	Chip Select to Power Up Time[2]	0	—	0	—	0	—	ns
t_{PD}	Chip Deselect to Power Down Time[2]	—	35	—	40/50	—	60	ns

2955 tbl 11

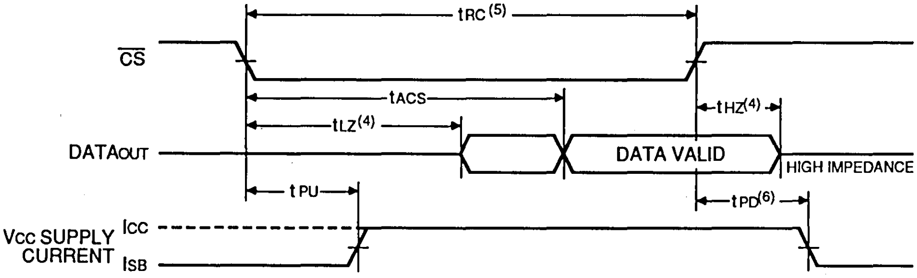
NOTES:
1. -55°C to +125°C temperature range only. Also available 85ns and 100ns devices.
2. This parameter is guaranteed, but not tested.
3. 0° to +70°C temperature range only.

TIMING WAVEFORM OF READ CYCLE NO. 1(1, 2)



2955 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 3)



2955 drw 08

NOTES:
1. WE is high for READ cycle.
2. CS is low for READ cycle.
3. Address valid prior to or coincident with CS transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. This parameter is guaranteed and not 100% tested.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6168SA10[4]		6168SA12		6168SA15		6168SA20/25 6168LA20/25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle										
t_{WC}	Write Cycle Time	10	—	12	—	15	—	20	—	ns
t_{CW}	Chip Select to End of Write	10	—	12	—	15	—	20	—	ns
t_{AW}	Address Valid to End of Write	10	—	12	—	15	—	20	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	10	—	12	—	15	—	20	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	7	—	8	—	9	—	10	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High Z[2]	—	4	—	5	—	6	—	7	ns
t_{OW}	Output Active from End of Write[2]	0	—	0	—	0	—	0	—	ns

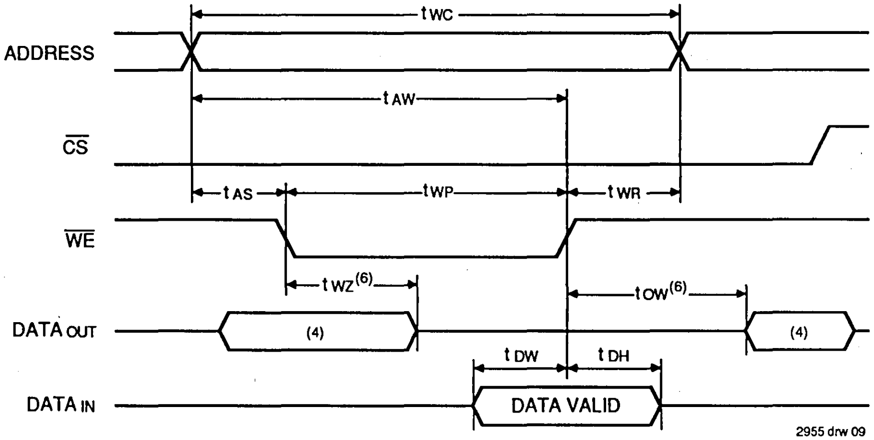
AC ELECTRICAL CHARACTERISTICS (Continued) (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6168SA35 6168LA35		6168SA45/55[1] 6168LA45/55[1]		6168SA70[1] 6168LA70[1]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle								
t_{WC}	Write Cycle Time	30	—	40/50	—	60	—	ns
t_{CW}	Chip Select to End of Write	30	—	40/50	—	60	—	ns
t_{AW}	Address Valid to End of Write	30	—	40/50	—	60	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	30	—	40/50	—	60	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	DataValid to End of Write	15	—	20	—	25	—	ns
t_{DH}	Data Hold Time	0	—	3	—	3	—	ns
t_{WZ}	Write Enable to Output in High Z[2]	—	13	—	20/25	—	30	ns
t_{OW}	Output Active from End of Write[2]	0	—	0	—	0	—	ns

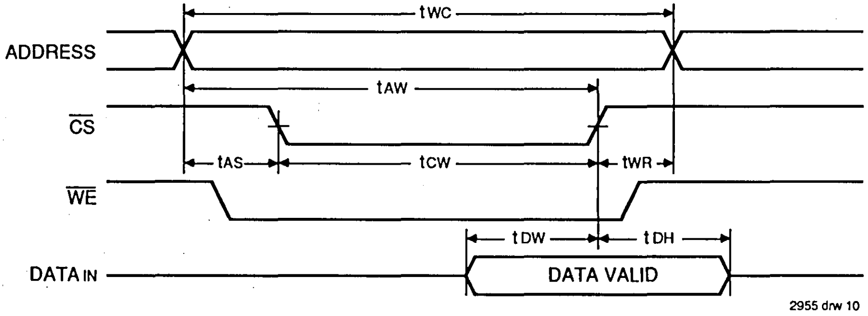
2955 tbl 12

NOTES:
1. -55°C to +125°C temperature range only. Also available 85ns and 100ns devices.
2. This parameter is guaranteed, but not tested.
3. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
4. 0° to +70°C temperature range only.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{\text{WE}}$ CONTROLLED TIMING)(1, 2, 3)

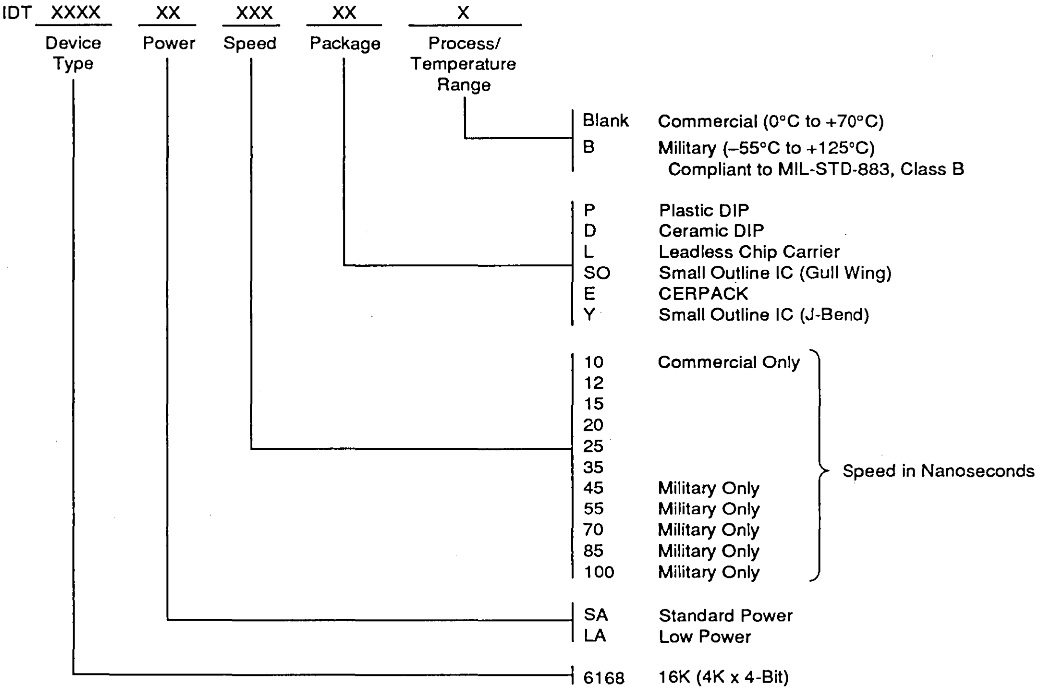


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{\text{CS}}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{\text{WE}}$ or $\overline{\text{CS}}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP} or t_{CW}) of a low $\overline{\text{CS}}$ and a low $\overline{\text{WE}}$.
3. t_{WR} is measured from the earlier of $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals should not be applied.
5. If the $\overline{\text{CS}}$ low transition occurs simultaneously with or after the $\overline{\text{WE}}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).

ORDERING INFORMATION



Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

P	Plastic DIP
D	Ceramic DIP
L	Leadless Chip Carrier
SO	Small Outline IC (Gull Wing)
E	CERPACK
Y	Small Outline IC (J-Bend)

10	Commercial Only
12	
15	
20	
25	
35	
45	Military Only
55	Military Only
70	Military Only
85	Military Only
100	Military Only

Speed in Nanoseconds

SA	Standard Power
LA	Low Power

6168	16K (4K x 4-Bit)

2955 drw 11

Integrated Device Technology, Inc.

CMOS STATIC RAM 16K (4K x 4-BIT) CACHE-TAG RAM

IDT6178S

FEATURES:

- High-speed Address to MATCH Valid time
  - Military: 12/15/20/25ns
  - Commercial: 10/12/15/20/25ns (max.)
- High-speed Address Access time
  - Military: 12/15/20/25ns
  - Commercial: 10/12/15/20/25ns (max.)
- Low-power operation
  - IDT6178S
    Active: 300mW (typ.)
- Produced with advanced CEMOS™ high-performance technology
- Input and output TTL-compatible
- Standard 22-pin plastic or ceramic DIP, 24-pin SOJ
- Military product 100% compliant to MIL-STD-883, Class B

DESCRIPTION:

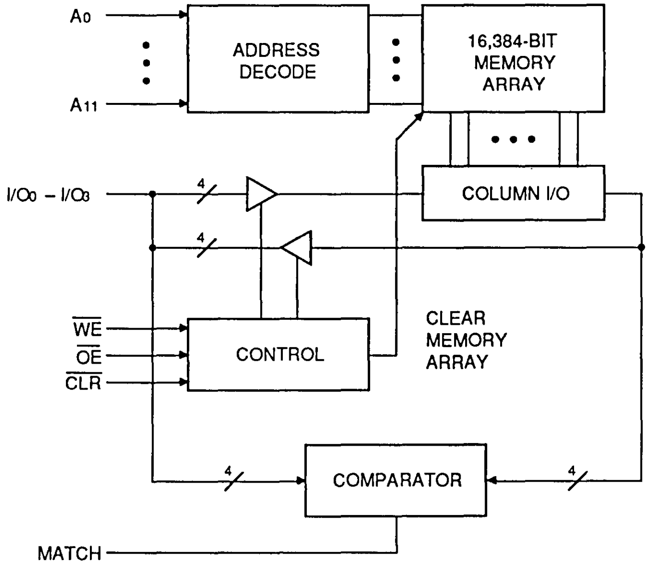
The IDT6178 is a high-speed cache address comparator sub-system consisting of a 16,384-bit static RAM organized as 4K x 4. Cycle Time and Address to MATCH Valid are equal. The IDT6178 features an onboard 4-bit comparator that compares RAM contents and current input data. The result is an active high on the MATCH pin. The MATCH pins of several IDT6178's can be nanded together to provide enabling or acknowledging signals to the data cache or processor.

The IDT6178 is fabricated using IDT's high-performance, high-reliability technology — CEMOS™. Address to MATCH and Data to MATCH times are as fast as 10ns.

All inputs and outputs of the IDT6178 are TTL-compatible and the device operates from a single 5V supply.

The IDT6178 is packaged in either a 22-pin, 300-mil plastic or ceramic DIP package or 24-pin SOJ. Military grade product is manufactured in compliance with latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

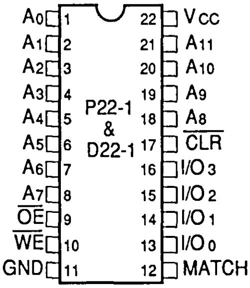
FUNCTIONAL BLOCK DIAGRAM



2522 drw 01

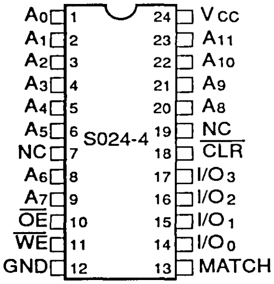
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



2953 drw 02

DIP
TOP VIEW



2953 drw 03

SOJ
TOP VIEW

PIN NAMES

$A_0 - A_{11}$	Address	$\overline{WE}$	Write Enable
$I/O_0 - I/O_3$	Data Input/Output	$\overline{OE}$	Output Enable
MATCH	Match	$\overline{CLR}$	Clear
Vcc	Power	GND	Ground

2953 tbl 01

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 2 and 3
Output Load for Match Cycle	See Figure 1

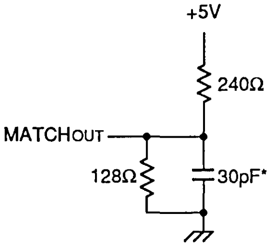
2953 tbl 03

TRUTH TABLES(1)

$\overline{WE}$	$\overline{OE}$	$\overline{CLR}$	MATCH	Mode
H	H	H	Valid	Match Cycle
L	X	H	Invalid	Write Cycle
H	L	H	Invalid	Read Cycle
X	X	L	Invalid	Clear Cycle

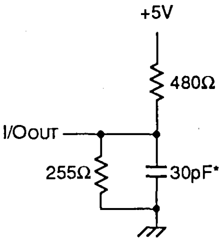
NOTE:
1. H = V_{IH}, L = V_{IL}, X = Don't care.

2953 tbl 02



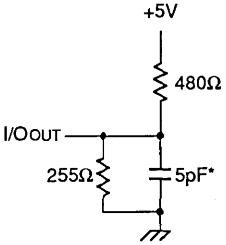
2953 drw 04

Figure 1.



2953 drw 05

Figure 2.



2953 drw 06

Figure 3.
(for t_{OLZ}, t_{OHZ}, t_{WHZ}, t_{OW})

* Including scope and jig.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–65 to +135	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTE: 2953 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2(2)	–	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	–	0.8	V

NOTE: 2953 tbl 05

1. V_{IL} = –3.0V for pulse width less than 20ns.
2. V_{IH} = 2.5V for clear pin.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%
Military	-55°C to +125°C	0V	5.0V ± 10%

2953 tbl 06

DC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	Test Condition	6178S Min.	6178S Max.	Unit
$\lvert I_{LI}\rvert$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	µA
$\lvert I_{LO}\rvert$	Output Leakage Current	$\overline{OE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA (I/O0 – I/O3)	—	0.4	V
		I_{OL} = 10mA (I/O0 – I/O3)	—	0.5	V
		I_{OL} = 16mA (Match)	—	0.4	V
		I_{OL} = 20mA (Match)	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = –4mA (I/O0 – I/O3)	2.4	—	V
		I_{OH} = –8mA (Match)	2.4	—	V

2953 tbl 07

DC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter		6178S10 Max.	6178S12(1) Max.	6178S15(1) Max.	6178S20/25 Max.	Unit
I_{CC1}	Operating Power Supply Current	COM'L.	90	90	90	90	mA
	Outputs Open, Vcc = Max., f = 0	MIL.	—	110	110	110	mA
I_{CC2}	Dynamic Operating Current	COM'L.	180	160	140	140	mA
	Outputs Open, Vcc = Max., f = f_{MAX}	MIL.	—	180	160	160	mA

NOTE: 2953 tbl 08l

1. Military values are preliminary only.

CYCLE DESCRIPTION

Match Cycle: A match cycle occurs when all control signals ($\overline{OE}$, $\overline{WE}$, $\overline{CLR}$) are high. At that time, data supplied to the RAM on the I/O pins is compared with the data stored at the specified address. The totem-pole match output is high when there is a match at all data bits, and drives low if there is not a match.

Write Cycle: The write cycle is conventional, occuring when $\overline{WE}$ is low and $\overline{CLR}$ is high. $\overline{OE}$ may be either high or low, since it is overridden by $\overline{WE}$. The state of the Match pin is not guaranteed, but in the current implementation it continues to reflect the output of the comparator. The Match pin goes high during write cycles since the data at the specified address is the same as the data (being written) at the I/Os of the RAM.

Read Cycle: When $\overline{WE}$ and $\overline{CLR}$ are high and $\overline{OE}$ is low, the RAM is in a read cycle. The state of the Match pin is not guaranteed, but in the current implementation it continues to reflect the output of the comparator. The Matach pin goes high during read cycles since the data at the specified address is the same as the data (being read) at the I/Os of the RAM.

Clear Cycle: When $\overline{CLR}$ is asserted, every bit in the RAM is cleared to zero. If $\overline{OE}$ is low during a clear cycle, the RAM I/Os will be driven. However, this data is not necessarily zeros, even after a considerable time. The Match pin is enabled, but its state is not predicable.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

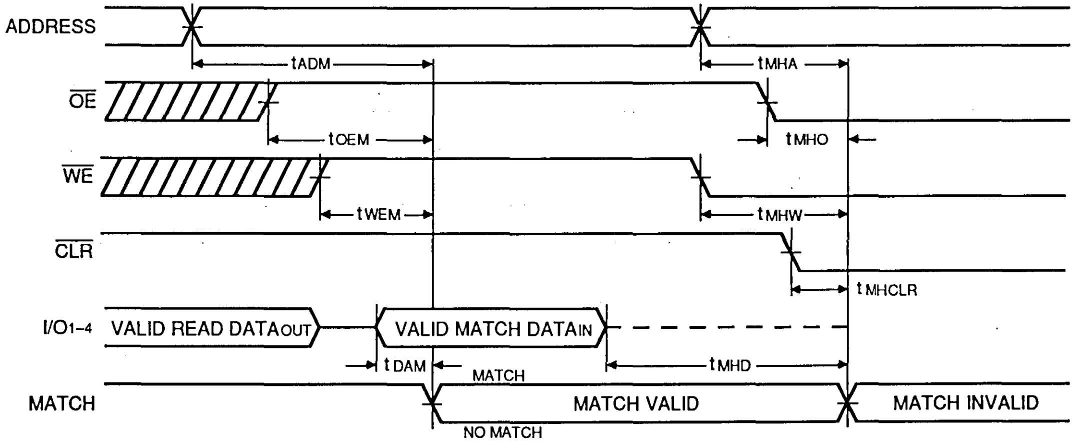
Symbol	Parameter	6178S10[1] Min.	6178S10[1] Max.	6178S12 Min.	6178S12 Max.	6178S15 Min.	6178S15 Max.	6178S20/25 Min.	6178S20/25 Max.	Unit
Match Cycle										
t_{ADM}	Address to Match Valid	—	10	—	12	—	15	—	20/25	ns
t_{DAM}	Data Input to Match Valid	—	8	—	11	—	13	—	15	ns
t_{MHO}	Match Valid Hold from $\overline{OE}$	0	—	0	—	0	—	0	—	ns
t_{OEM}	$\overline{OE}$ High to Match Valid	—	10	—	12	—	15	—	20	ns
t_{MHW}	Match Valid Hold from $\overline{WE}$	0	—	0	—	0	—	0	—	ns
t_{WEM}	$\overline{WE}$ High to Match Valid	—	10	—	12	—	15	—	20	ns
t_{MHCLR}	Match Valid Hold from $\overline{CLR}$	0	—	0	—	0	—	0	—	ns
t_{MHA}	Match Valid Hold from Address	3	—	3	—	3	—	3	—	ns
t_{MHD}	Match Valid Hold from Data	3	—	3	—	3	—	3	—	ns

NOTE:

1. 0°C to +70°C temperature range only.

2953 tbl 09

TIMING WAVEFORM OF MATCH CYCLE[1]



NOTE:

1. It is not recommended to let address and data input pins float while MATCH pin is active.

2953 drw 07

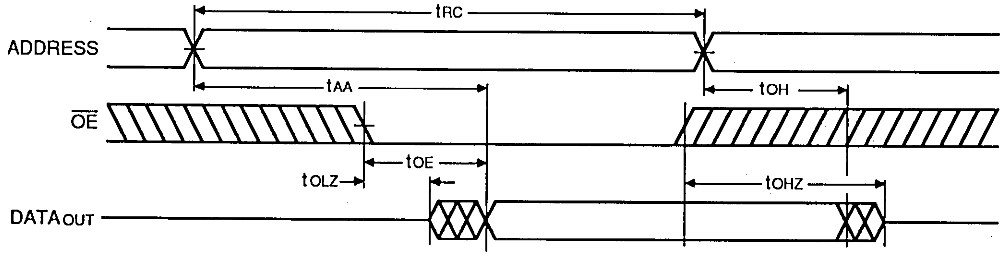
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6178S10[3]		6178S12		6178S15		6178S20/25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	10	—	12	—	15	—	20/25	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	—	20/25	ns
t_{OE}	Output Enable Access Time	—	7	—	8	—	10	—	15	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t_{OLZ}	Output Low Z Time[1,2]	2	—	2	—	2	—	2	—	ns
t_{OHZ}	Output High Z Time[1,2]	—	6	—	7	—	9	—	12	ns

2953 tbl 10

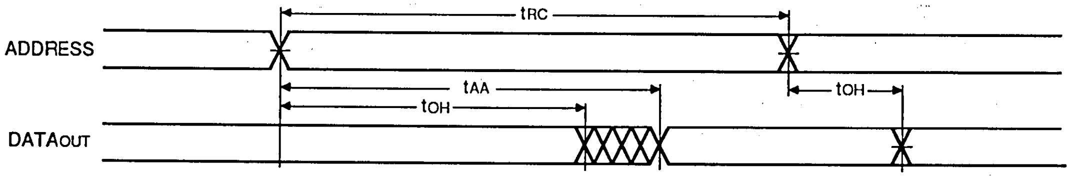
NOTES:
1. Transition is measured ±200mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter guaranteed but not tested.
3. 0°C to +70°C temperature range only.

TIMING WAVEFORM OF READ CYCLE NO. 1



2953 drw 08

TIMING WAVEFORM OF READ CYCLE NO. 2



2953 drw 09

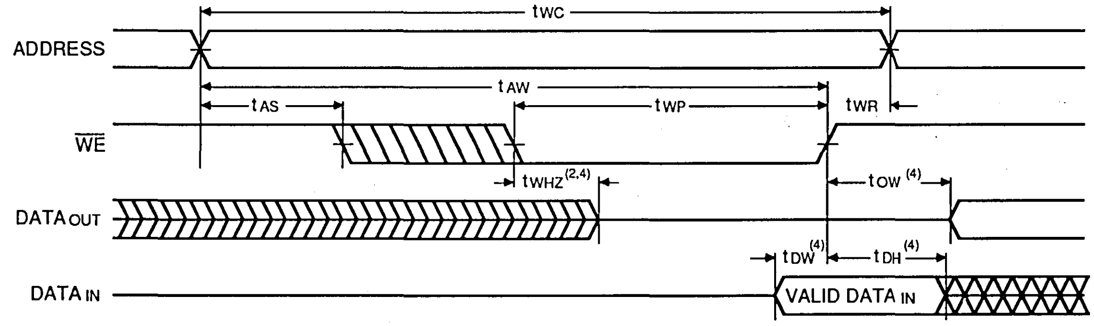
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6178S10[3]		6178S12		6178S15		6178S20/25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle										
t_{WC}	Write Cycle Time	10	—	12	—	15	—	20	—	ns
t_{AW}	Address Valid to End of Write	8	—	10	—	12	—	14	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	8	—	10	—	12	—	14	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	6	—	8	—	10	—	12	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}	Write Enable to Output in High Z[1,2]	—	5	—	6	—	7	—	9	ns
t_{OW}	Output Active from End of Write[1,2]	0	—	0	—	0	—	0	—	ns

2953 tbl 11

NOTES:
1. Transition is measured ±200mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter guaranteed but not tested.
3. 0°C to +70°C temperature range only.

TIMING WAVEFORM OF WRITE CYCLE(1,3)



2953 drw 10

NOTES:
1. $\overline{WE}$ must be high during all address transitions.
2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
3. $\overline{OE}$ is continuously high or low. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the greater of t_{WP} or ($t_{WHZ} + t_{DW}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
4. Transition is measured ±200mV from steady state.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

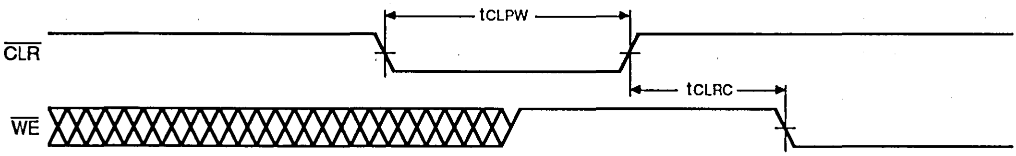
Symbol	Parameter	6178S10[2]		6178S12		6178S15		6178S20/25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clear Cycle										
t_{CLPW}	$\overline{CLR}$ Pulse Width[1]	20	—	25	—	30	—	40	—	ns
t_{CLRC}	$\overline{CLR}$ High to $\overline{WE}$ Low	5	—	5	—	5	—	5	—	ns

NOTES:

2953 tbl 12

1. Recommended duty cycle of 10% maximum.
2. 0°C to +70°C temperature range only.

TIMING WAVEFORM OF CLEAR CYCLE



2953 drw 11

ORDERING INFORMATION

IDT XXXX S XX A A

Device Type — Power — Speed — Package — Process/Temperature

Process/Temperature	
Blank	Commercial (0°C to +70°C)
B	Military (-55°C to +125°C, Compliant to MIL-STD-883, Class B)

Package	
P	Plastic DIP
Y	Small Outline (J bend)
D	Ceramic DIP

Speed	
10	Commercial only
12	
15	
20	
25	

Speed in Nanoseconds

Power	
S	Standard Power

Device Type	
6178	16K (4K x 4-Bit) Cache-Tag RAM

2953 drw 12

Integrated Device Technology, Inc.

CMOS STATIC RAM WITH OUTPUT ENABLE 16K (4K x 4-BIT)

IDT61970S
IDT61970L

FEATURES:

- High Speed (equal Access and Cycle Times)
  - Military: 12/15/20/25/35/45/55
  - Commercial: 10/12/15/20/25/35/45
- Fast Output Enable
- Low power consumption
  - IDT61970S
    Active: 300mW (typ.)
    Standby: 100µW (typ.)
  - IDT61970L
    Active: 300mW (typ.)
    Standby: 10µW (typ.)
- Battery backup operation—2V data retention (IDT61970L only)
- Available in 22-pin ceramic or plastic DIP and 24-pin SOJ
- Input and output directly TTL-compatible
- Produced with advanced CEMOS™ high-performance technology
- Separate Output Enable control
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT61970 is a 16,384-bit high-speed static RAM organized as 4096 x 4 bits. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS™. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for high-speed memory applications.

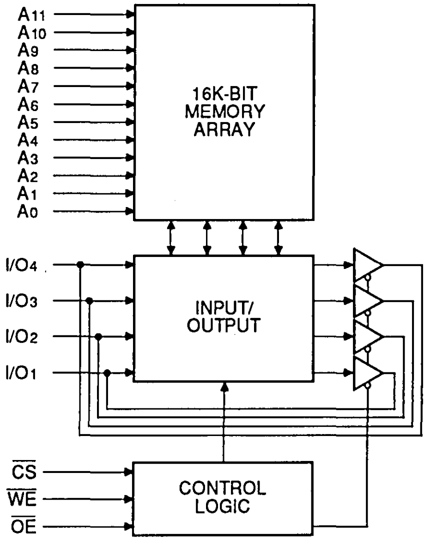
The IDT61970 features two memory control functions: chip select ($\overline{\text{CS}}$) and output enable ($\overline{\text{OE}}$). These two functions greatly enhance the IDT61970's overall flexibility in high-speed memory applications. This feature makes the IDT61970 ideal for use in cache memory applications.

Access times as fast as 10ns and t_{OE} as fast as 5ns are available, with typical power consumption of only 300mW. The IDT61970 offers a reduced power standby mode which enables the designer to considerably reduce device power requirements. This capability significantly decreases system power and cooling levels, while greatly enhancing system reliability. The low power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 10µW when operating from a 2V battery. All inputs and output are TTL-compatible and operate from a single 5V supply.

The IDT61970 is packaged in either a space saving 22-pin, 300-mil ceramic or plastic DIP, or a 24-pin SOJ, providing high board level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

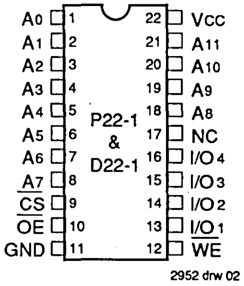
FUNCTIONAL BLOCK DIAGRAM



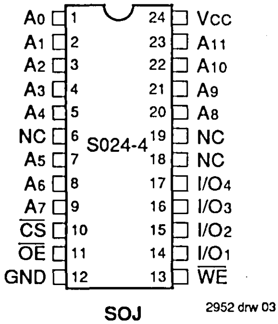
2952 drw 01

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP
TOP VIEW



SOJ
TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–65 to +135	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTE: 2952 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

PIN NAMES

$A_0 - A_{11}$	Address	$\overline{WE}$	Write Enable
$I/O_1 - I/O_4$	Data Input/Output	$\overline{OE}$	Output Enable
Vcc	Power	$\overline{CS}$	Chip Select
GND	Ground	NC	No Connection

2952 tbl 01

TRUTH TABLE[1]

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Standby	H	X	X	Hi-Z	Standby
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active
Read	L	H	H	Hi-Z	Active

NOTE: 2952 tbl 08

1. H = V_{IH}, L = V_{IL}, X = Don't Care.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition		61970S Min.	61970S Max.	61970L Min.	61970L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	Vcc = Max.;	Mil.	—	10	—	5	µA
		V_{IN} = GND to Vcc	Com'l.	—	2	—	2	
$\|I_{LO}\|$	Output Leakage Current	Vcc Max. $\overline{CS}$ = V_{IH},	Mil.	—	10	—	5	µA
		Vcc = GND to Vcc	Com'l.	—	2	—	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA Vcc = Min.		—	0.5	—	0.5	V
		I_{OL} = 8mA Vcc = Min.		—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, Vcc = Min.		2.4	—	2.4	—	V

2952 tbl 03

DC ELECTRICAL CHARACTERISTICS(1) V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V

			61970S10		61970S12(4)		61970S15		61970S20 61970L20		61970S25 61970L25		61970S35 61970L35		61970S45/55(3) 61970L45/55(3)		
Symbol	Parameter	Power	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0(2)	S	120	—	110	120	110	120	90	100	90	100	90	100	—	100	mA
		L	—	—	—	—	—	—	70	80	70	80	70	80	—	80	
I_{CC2}	Dynamic Operating Current, $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	S	175	—	165	175	145	165	120	120	110	120	100	110	—	110	mA
		L	—	—	—	—	—	—	100	110	90	100	80	90/ 80	—	80	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}(2)	S	65	—	65	65	55	60	45	45	35	45	30	35	—	35	mA
		L	—	—	—	—	—	—	30	35	25	30	20	25	—	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0(2)	S	20	—	20	20	20	20	20	20	2	10	2	10	—	10	mA
		L	—	—	—	—	—	—	0.5	5	0.05	0.3	0.05	0.3	—	0.3	

NOTES:

2952 tbl 04

1. All values are maximum guaranteed values.
2. f = f_{MAX} (All inputs except Chip Select cycling at f = 1/t_{RC}). f = 0 means no address or control lines change.
3. –55°C to +125°C temperature range only.
4. Military values are preliminary only.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	–	0.8	V

NOTE:

2952 tbl 05

1. V_{IL} (min.) = –3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55° to +125°C	0V	5.0V ±10%
Commercial	0°C to +70°C	0V	5.0V ±10%

2952 tbl 09

AC ELECTRICAL CHARACTERISTICS

		61970S10		61970S12		61970S15		61970S20/25 61970L20/25		61970S35/45 61970L35/45		61970S55 61970L55		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle														
t_{RC}	Read Cycle Time	10	—	12	—	15	—	20/25	—	35/45	—	55	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	—	20/25	—	35/45	—	55	ns
t_{OE}	Output Enable Access Time	—	5	—	5	—	6	—	8/10	—	12/15	—	20	ns
t_{OLZ}	Output Low Z Time(1, 2)	2	—	2	—	2	—	2	—	2	—	2	—	ns
t_{OHZ}	Output High Z Time(1, 2)	—	6	—	7	—	9	—	12	—	15	—	15	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	3	—	ns
t_{ACS}	Chip Select Access Time	10	—	12	—	15	—	20/25	—	35/45	—	55	—	ns
t_{CLZ}	Chip Select to Output in Low Z(1, 2)	3	—	3	—	3	—	3	—	3	—	3	—	ns
t_{CHZ}	Chip Deselect to Output in High Z(1,2)	—	6	—	7	—	8	—	10	—	15	—	25	ns

NOTES:

2952 tbl 06

1. Transition is measured ±200mV from low or high impedance voltage with load.
2. This parameter is guaranteed, but not tested.

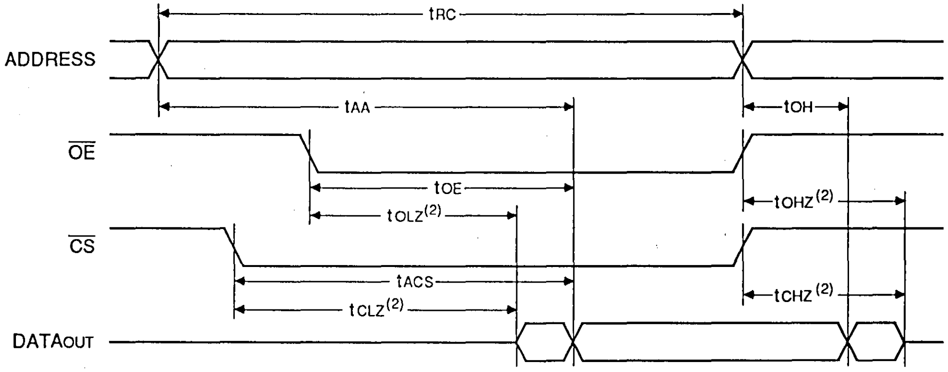
AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	61970S10		61970S12		61970S15		61970S20/25 61970L20/25		61970S35/45 61970L35/45		61970S55 61970L55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle														
t_{WC}	Write Cycle Time	10	—	12	—	15	—	20/25	—	35/45	—	55	—	ns
t_{AW}	Address Valid to End of Write	8	—	10	—	12	—	15/20	—	25/30	—	35	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	8	—	8	—	10	—	12/15	—	20/25	—	30	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	7	—	8	—	9	—	10/13	—	17/20	—	20	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High Z[1,2]	—	5	—	6	—	7	—	9	—	13/20	—	25	ns
t_{OW}	Output Active From End of Write[1,2]	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{CW}	Chip Select to End of Write	8	—	10	—	12	—	15/20	—	25/30	—	35	—	ns

2952 tbl 07

NOTES:
1. Transition is measured ±200mV from low or high impedance voltage with load.
2. This parameter is guaranteed, but not tested.

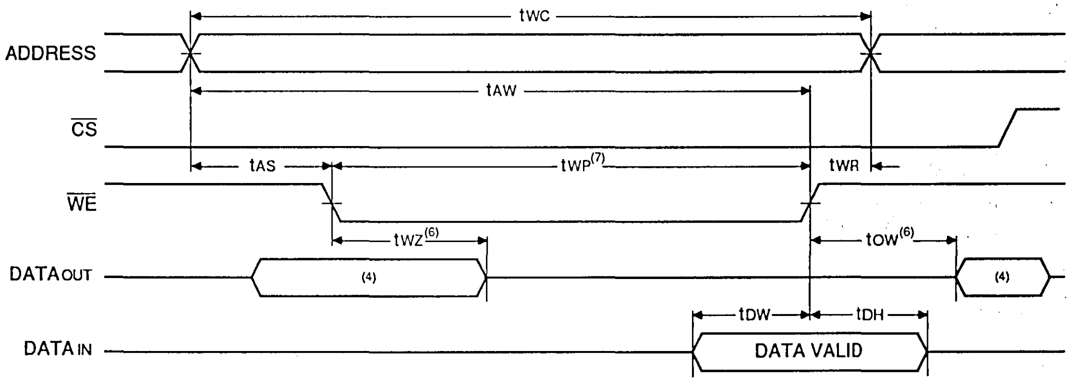
TIMING WAVEFORM OF READ CYCLE[1]



2952 drw 05

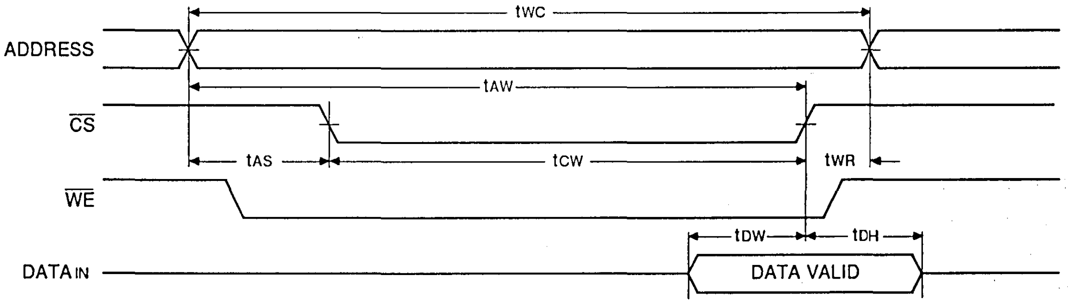
NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Transition is measured ±200mV from steady state with 5pF load (including scope and jig).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{\text{WE}}$ CONTROLLED TIMING)$^{(1, 2, 3, 7)}$



2952 drw 07

TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{\text{CS}}$ CONTROLLED TIMING)$^{(1, 2, 3, 5)}$



2952 drw 08

NOTES:

1. $\overline{\text{WE}}$ or $\overline{\text{CS}}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP or tCW) of a low $\overline{\text{CS}}$ and a low $\overline{\text{WE}}$.
3. tWR is measured from the earlier of $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals should not be applied.
5. If the $\overline{\text{CS}}$ low transition occurs simultaneously with or after the $\overline{\text{WE}}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{\text{OE}}$ is low during a $\overline{\text{WE}}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{\text{OE}}$ is high during a $\overline{\text{WE}}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) $V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$

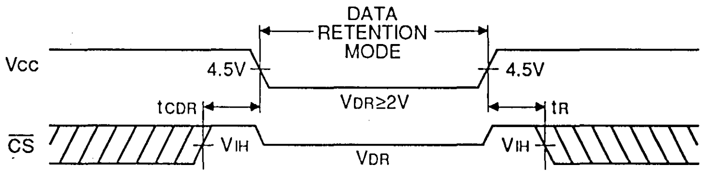
Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	$\overline{CS} \geq V_{HC} - 0.2V$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$		2.0	—	—	V
I_{CCDR}	Data Retention Current		MIL.	— —	0.5[2] 1.0[3]	100[2] 150[3]	µA
			COM'L.	— —	0.5[2] 1.0[3]	20[2] 30[3]	µA
t_{CDR}[4]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[4]	Operation Recovery Time			t_{RC}[2]	—	—	ns

2952 tbl 10

NOTES:

1. $T_A = +25°C$.
2. at $V_{CC} = 2V$
3. at $V_{CC} = 3V$
4. This parameter is guaranteed, but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM

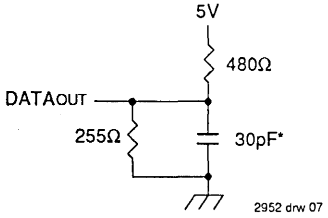


2952 drw 06

AC TEST CONDITIONS

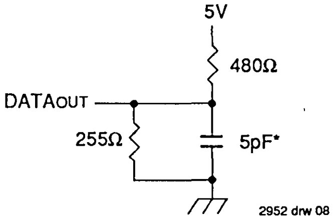
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2952 tbl 11



2952 drw 07

Figure 1. Output Load

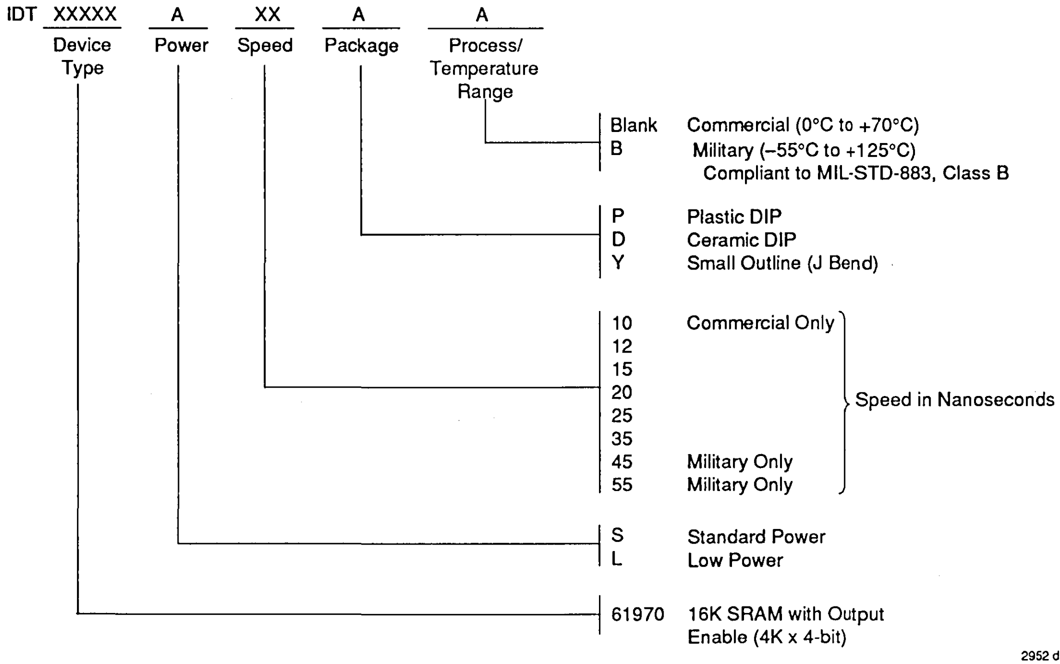


2952 drw 08

Figure 2. Output Load
(for t_{OLZ}, t_{CLZ}, t_{OHZ}, t_{CHZ}, t_{OW}, t_{WZ})

* Including scope and jig.

ORDERING INFORMATION



2952 drw 09

Integrated Device Technology, Inc.

CMOS STATIC RAM
64K (16K x 4-BIT)

IDT6198S
IDT6198L

FEATURES:

- Optimized for fast RISC processors including the IDT79R3000
- Output Enable (OE) pin available for added system flexibility
- High-speed (equal access and cycle times)
  - — Military: 20/25/35/45/55/70/85ns (max.)
  - — Commercial: 15/20/25/35ns (max.)
- Low-power consumption
  - — IDT6198S
    Active: 350mW (typ.)
    Standby 100µW (typ.)
  - — IDT6198L
    Active: 300mW (typ.)
    Standby: 30µW (typ.)
- JEDEC compatible pinout
- Battery back-up operation—2V data retention (L version only)
- 24-pin CERDIP, 24-pin plastic DIP, high-density 28-pin leadless chip carrier and 24-pin SOIC (gull-wing and J-bend)
- Produced with advanced CEMOS™ technology
- Bidirectional data inputs and outputs
- Military product compliant to MIL-STD-883, Class B

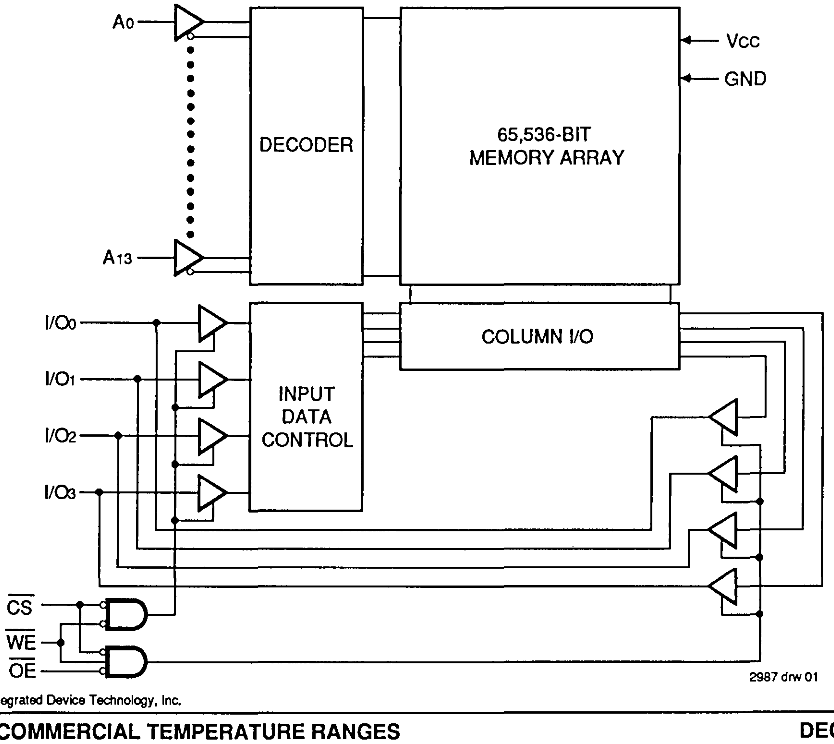
DESCRIPTION:

The IDT6198 is a 65,536-bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective approach for memory intensive applications. Timing parameters have been specified to meet the speed demands of the IDT79R3000 RISC processors.

The IDT6198 features two memory control functions: chip select (CS) and output enable (OE). These two functions greatly enhance the IDT6198's overall flexibility in high-speed memory applications.

Access times as fast as 15ns are available, with typical power consumption of only 300mW. The IDT6198 offers a reduced power standby mode, I_{SB1}, which enables the designer to considerably reduce device power requirements. This capability significantly decreases system power and

FUNCTIONAL BLOCK DIAGRAM



2987 drw 01

CEMOS is a trademark of Integrated Device Technology, Inc.

DESCRIPTION (Continued)

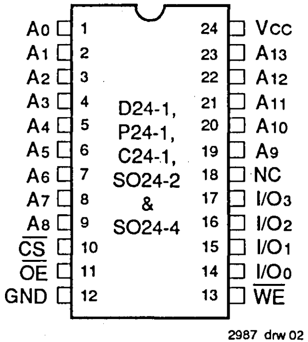
cooling levels, while greatly enhancing system reliability. The low-power version (L) also offers a battery backup data retention capability where the circuit typically consumes only 30µW when operating from a 2 volt battery.

All inputs and outputs are TTL-compatible and operate from a single 5 volt supply.

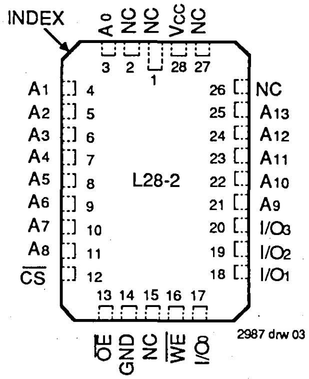
The IDT6198 is packaged in either a 24-pin 300 mil CERDIP or plastic DIP, 28-pin leadless chip carrier or 24-pin gull-wing or J-bend small outline IC.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS



DIP/SOIC
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A_0–A_{13}	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O_0–I/O_3	Data Input/Output
V_{CC}	Power
GND	Ground

2987 tbl 01

TRUTH TABLE[1]

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Standby	H	X	X	High Z	Standby
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active
Read	L	H	H	High Z	Active

NOTE:
2987 tbl 02

1. H = V_{IH}, L = V_{IL}, X = Don't Care

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
2987 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:
2987 tbl 04

1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2987 tbl 05

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2987 tbl 06

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT6198S		IDT6198L		Unit
				Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL. COM'L.	— —	10 5	— —	5 2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL. COM'L.	— —	10 5	— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.			0.5	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	
V_{OH}	Output High Voltage	I_{OL} = -4mA, V_{CC} = Min.		2.4	—	2.4	—	V

2967 tbl 07

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	6198S15 6198L15		6198S20 6198L20		6198S25 6198L25		6198S35 6198L35		6198S45 6198L45		6198S55/70/85 6198L55/70/85		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = 0[2]	S	110	—	100	110	100	110	100	110	—	110	—	110	mA
		L	75	—	70	80	70	80	85	95	—	95	—	95	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = f_{MAX}[2]	S	135	—	130	160	135	155	125	140	—	140	—	140	mA
		L	125	—	115	130	105	120	105	115	—	110	—	110	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}[2]	S	60	—	55	70	55	60	45	500	—	50	—	50	mA
		L	45	—	40	50	35	40	35	40	—	35	—	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC}=Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0[2]	S	20	—	15	25	15	20	15	20	—	20	—	20	mA
		L	1.5	—	0.5	1.5	0.5	1.5	0.5	1.5	—	1.5	—	1.5	

NOTES: 2987 tbl 06

1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

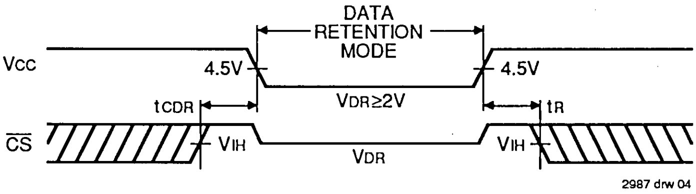
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

					Typ.[1] Vcc @		Max. Vcc @		
Symbol	**Parameter**	**Test Condition**		**Min.**	**2.0v**	**3.0V**	**2.0V**	**3.0V**	**Unit**
V_{DR}	Vcc for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	—	10	15	600	900	µA
			COM'L.	—	10	15	150	225	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	—	—	ns
t_{R}[3]	Operation Recovery Time			t_{RC}[2]	—	—	—	—	ns
$\lvert I_{LI}\rvert$[3]	Input Leakage Current			—	—	—	2	2	µA

2967 tbl 09

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

LOW Vcc DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2987 tbl 10

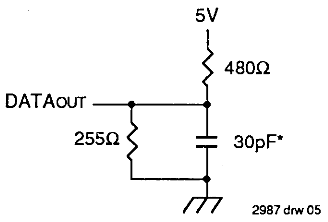


Figure 1. Output Load

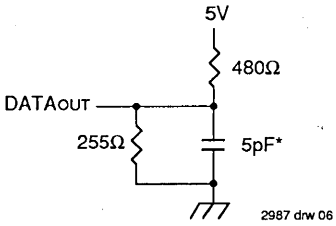


Figure 2. Output Load
(for t_{OLZ}, t_{CLZ}, t_{OHZ}, t_{WHZ}, t_{CHZ} and t_{OW})

*Includes scope and jig capacitances

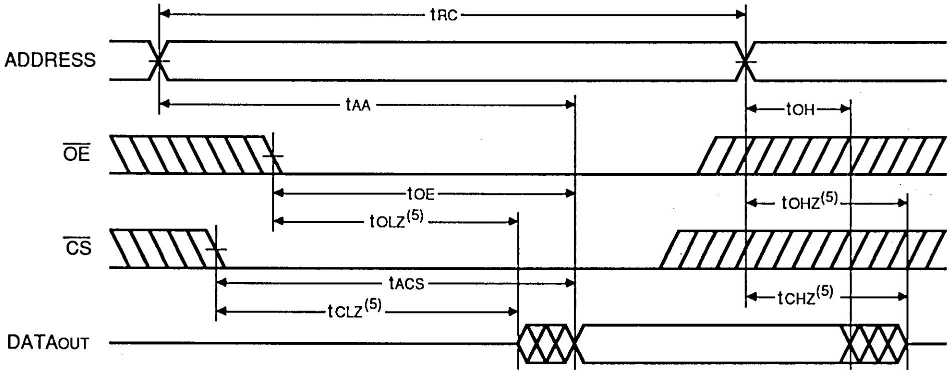
AC ELECTRICAL CHARACTERISTICS (VCC = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6198S15(1) 6198L15(1)		6198S20 6198L20		6198S25 6198L25		6198S35 6198L35		6198S45/55(2) 6198L45/55(2)		6198S70/85(2) 6198L70/85(2)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle														
tRC	Read Cycle Time	15	—	20	—	25	—	35	—	45/55	—	70/85	—	ns
tAA	Address Access Time	—	15	—	19	—	25	—	35	—	45/55	—	70/85	ns
tACS	Chip Select Access Time	—	15	—	20	—	25	—	35	—	45/55	—	70/85	ns
tCLZ	Chip Select to Output in Low Z(3)	5	—	5	—	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	8	—	9	—	11	—	18	—	25/35	—	45/55	ns
tOLZ	Output Enable to Output in Low Z(3)	5	—	5	—	5	—	5	—	5	—	5	—	ns
tCHZ	Chip Select to Output in High Z(3)	2	7	2	8	2	10	2	14	—	15/20	—	25/30	ns
tOHZ	Output Disable to Output in High Z(3)	2	7	2	8	2	9	2	15	—	15/20	—	25/30	ns
tOH	Output Hold from Address Change	5	—	5	—	2	—	5	—	5	—	5	—	ns
tPU	Chip Select to Power Up Time(3)	0	—	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Deselect to Power Down Time(3)	—	15	—	20	—	25	—	35	—	45/55	—	70/85	ns

2987 tbl 11

NOTES:
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

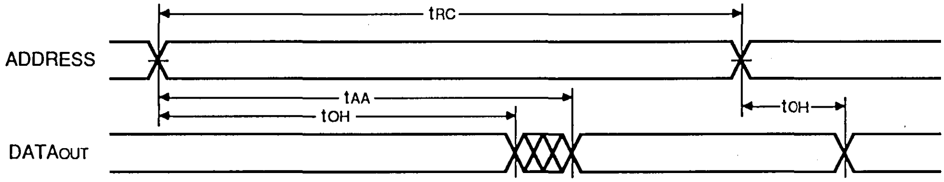
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



2987 drw 07

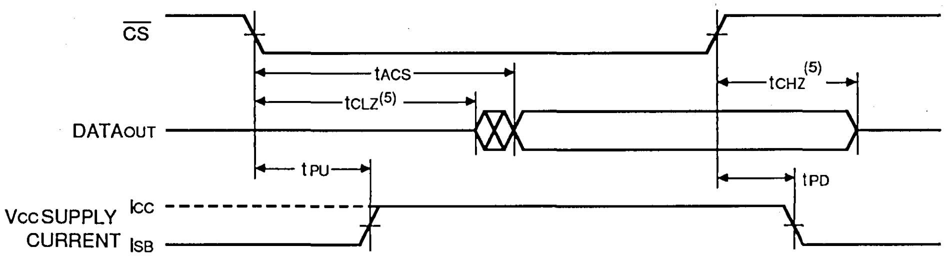
NOTES:
1. $\overline{WE}$ is high for Read cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ±200mV from steady state voltage.

TIMING WAVEFORM OF READ CYCLE NO. 2$^{(1, 2, 4)}$



2987 drw 08

TIMING WAVEFORM OF READ CYCLE NO. 3$^{(1, 3, 4)}$



2987 drw 09

NOTES:
1. $\overline{WE}$ is high for Read cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ±200mV from steady state voltage.

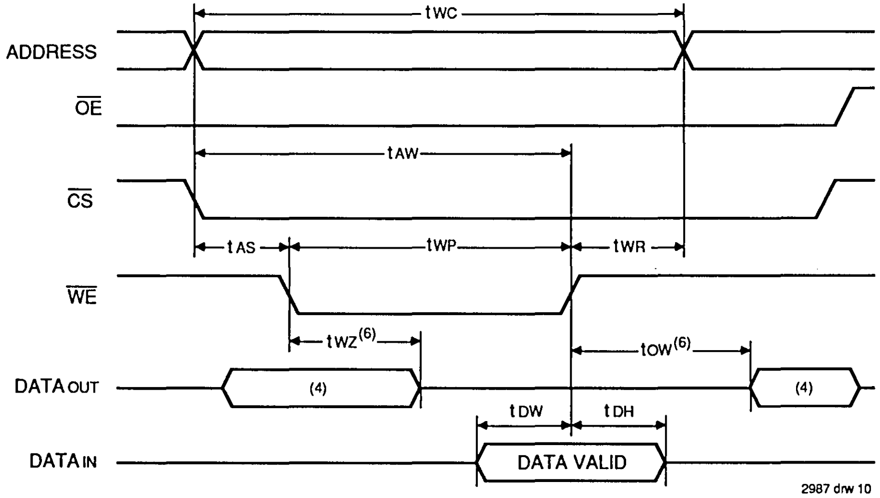
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6198S15[1] 6198L15[1]		6198S20 6198L20		6198S25 6198L25		6198S35 6198L35		6198S45/55[2] 6198L45/55[2]		6198S70/85[2] 6198L70/85[2]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle														
tWC	Write Cycle Time	14	—	17	—	20	—	30	—	40/50	—	60/75	—	ns
tCW	Chip Select to End of Write	14	—	17	—	20	—	25	—	35/50	—	60/75	—	ns
tAW	Address Valid to End of Write	14	—	17	—	20	—	25	—	35/50	—	60/75	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	14	—	17	—	20	—	25	—	35/50	—	60/75	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWHZ	Write Enable to Output in High Z[3]	—	5	—	6	—	7	—	10	—	15/25	—	30/40	ns
tDW	Data Valid to End of Write	10	—	10	—	13	—	15	—	20/25	—	30/35	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tOW	Output Active from End of Write[3]	5	—	5	—	5	—	5	—	5	—	5	—	ns

2987 tbl 12

NOTES:
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

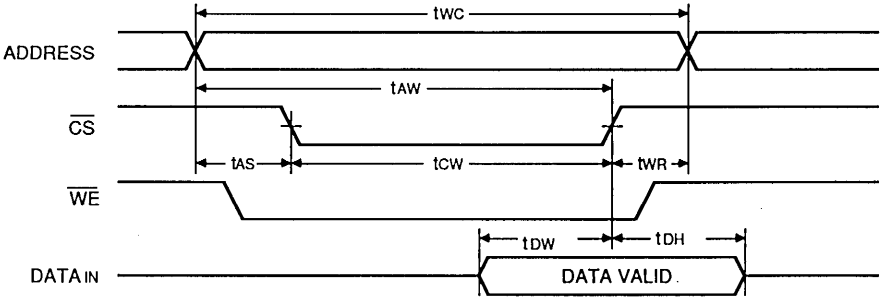
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3, 7]



2987 drw 10

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tCW tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high an $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
8. $\overline{OE}$ = VIH.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{\text{CS}}$ CONTROLLED TIMING)(1, 2, 3, 5, 8)



2987 drw 11

NOTES:

1. $\overline{\text{WE}}$ or $\overline{\text{CS}}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{CW} t_{WP}) of a low $\overline{\text{CS}}$ and a low $\overline{\text{WE}}$.
3. t_{WR} is measured from the earlier of $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{\text{CS}}$ low transition occurs simultaneously with or after the $\overline{\text{WE}}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state.
7. If $\overline{\text{OE}}$ is low during a $\overline{\text{WE}}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{\text{OE}}$ is high an $\overline{\text{WE}}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
8. $\overline{\text{OE}}$ = V_{IH}.

ORDERING INFORMATION

IDT	XXXX	X	XX	XX	X
	Device Type	Power	Speed	Package	Process/ Temperature Range

Code	Description
Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B
C	Sidebraze DIP (300 mil)
D	CERDIP (300 mil)
P	Plastic DIP (300 mil)
L	Leadless Chip Carrier
SO	Small Outline IC (Gull Wing)
Y	Small Outline IC (J-Bend)
15	Commercial Only
20	
25	
35	
45	Military Only
55	Military Only
70	Military Only
85	Military Only
S	Standard Power
L	Low Power
6198	16K x 4-Bit Static RAM

15 to 85: Speed in Nanoseconds

2987 drw 12

Integrated Device Technology, Inc.

CMOS STATIC RAM
1 MEG (128K X 8-BIT)

**ADVANCE
INFORMATION
IDT71024**

FEATURES:

- 128K x 8 configuration
- Two chip selects plus Output Enable pin
- High-speed access
  - Military: 30/35/45/55ns (max.)
  - Commercial: 25/35/45ns (max.)
- Low power consumption
  - IDT71024S
    Active: 500mW (typ.)
    Standby: 5mW (typ.)
  - IDT71024L
    Active: 500mW (typ.)
    Standby: 200µW (typ.)
- Battery back-up operation—2V data retention
- Available in 32-pin DIP
- TTL-compatible
- Single 5V (+10%) power supply
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71024 is an extremely high-density 128K x 8-bit high-speed static RAM designed for use in systems where fast computation, low power and board density are of the utmost importance.

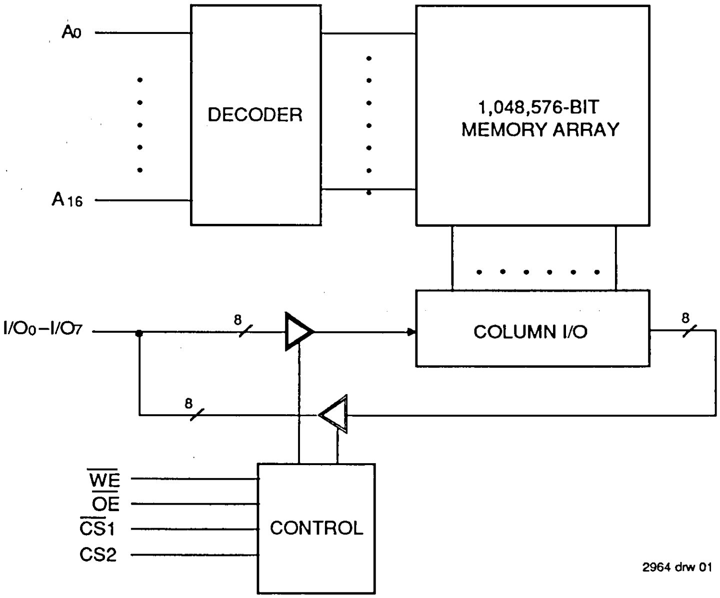
The IDT71024 uses eight bidirectional input/output lines to provide simultaneous access to all bits in a word and has an output enable ($\overline{OE}$) pin which operates as fast as 15ns. This function allows designers to access the IDT71024 at speeds much higher than the already fast 25ns address access time to achieve a considerable throughput advantage. An automatic power down feature permits the on-chip circuitry to enter a very low standby power mode and be brought back into operation at a speed equal to the address access time.

Fabricated using IDT's CEMOS™ high-performance technology, the IDT71024 typically operates on only 500mW of power at maximum access times as fast as 45ns. Low-power (L) versions offer battery backup data retention capability, typically consuming 200µW from a 2V battery.

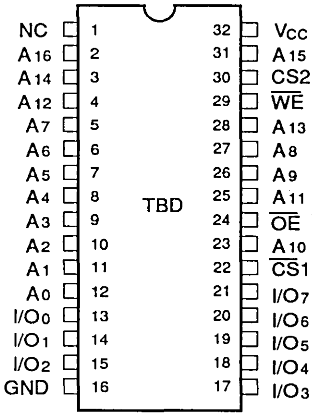
All inputs and outputs of the IDT71024 are TTL-compatible and the device operates from a standard 5V supply, simplifying system design. The IDT71024 is packaged in a 32-pin DIP.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



2964 drw 02

DIP
TOP VIEW

TRUTH TABLE[1]

INPUTS				OUTPUTS	
$\overline{WE}$	**$\overline{CS}_1$**	**CS_2**	**$\overline{OE}$**	**I/O_0–I/O_7**	**FUNCTION**
X	H	X	X	High-Z	Deselected
X	X	L	X	High-Z	Deselected
H	L	H	H	High-Z	Outputs disabled
H	L	H	L	DOUT	Read data from RAM
L	L	H	X	High-Z	Write data to RAM

NOTE:

2964 tbl 01

1. H = High, L = Low, X = Don't Care, High-Z = High Impedance

Integrated Device Technology, Inc.

CMOS STATIC RAM 1 MEG (256K X 4-BIT)

ADVANCE INFORMATION
IDT71028

FEATURES:

- 256K x 4 configuration
- High-speed access
  - Military: 30/35/45/55ns (max.)
  - Commercial: 25/35/45ns (max.)
- Low power consumption
  - IDT71028S
    Active: 500mW (typ.)
    Standby: 5mW (typ.)
  - IDT71028L
    Active: 500mW (typ.)
    Standby: 200µW (typ.)
- Battery back-up operation—2V data retention
- Available in 28-pin DIP
- TTL-compatible
- Single 5V (±10%) power supply
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71028 is an extremely high-density (256K x 4-bit), high speed static RAM designed for use in systems where fast computation, low power and board density are of the utmost importance.

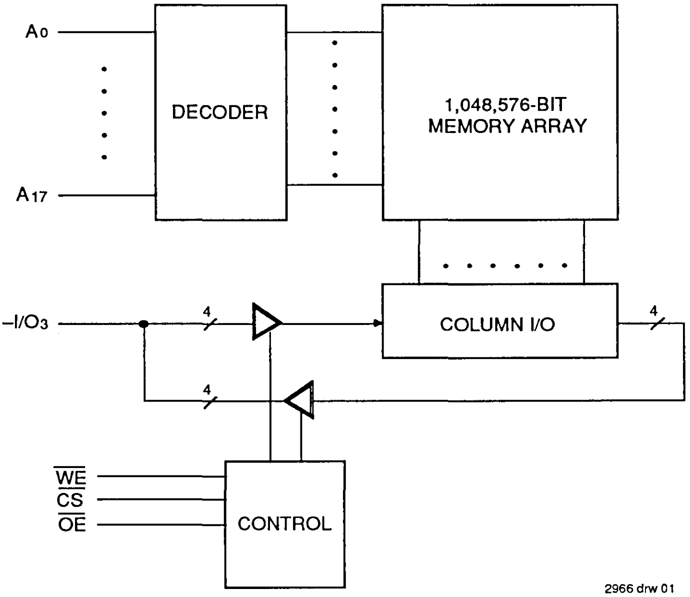
The IDT71028 uses four bidirectional input/output lines to provide simultaneous access to all bits in a word and has a high-speed 45ns address access time to achieve a considerable throughput advantage. An automatic power down feature, controlled by $\overline{CS}$, permits the on-chip circuitry to enter a very low standby power mode and be brought back into operation at a speed equal to the address access time.

Fabricated using IDT's CEMOS™ high-performance technology, the IDT71028 typically operates on only 500mW of power at maximum access times as fast as 45ns. Low-power (L) versions offer battery backup data retention capability, typically consuming 200µW from a 2V battery.

All inputs and outputs of the IDT71028 are TTL-compatible and the device operates from a standard 5V supply, simplifying system design. The IDT71028 is packaged in a 28-pin DIP.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

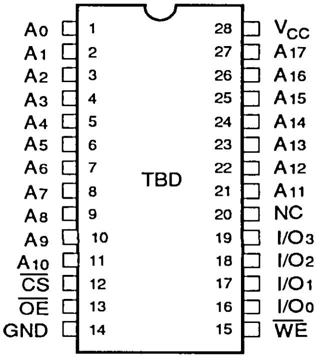
FUNCTIONAL BLOCK DIAGRAM



2966 drw 01

CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



2966 drw 02

DIP
TOP VIEW

TRUTH TABLE[1]

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O0–I/O3	FUNCTION
H	X	X	High-Z	Deselected, Powered-Down (ISB)
L	H	H	High-Z	Outputs Disabled
L	L	H	DOUT	Read Data from RAM
L	X	L	High-Z	Write Data to RAM

NOTE: 2966 tbl 01

1. H = High, L = Low, X = Don't Care, High-Z = High Impedance

Integrated Device Technology, Inc.

CMOS STATIC RAM 256K (32K x 8-BIT)

IDT71256S
IDT71256L

FEATURES:

- Optimized for fast RISC processors including the IDT79R3000
- High-speed address/chip select time
  - — Military: 25/30/35/45/55/70/85/100/120/150ns (max.)
  - — Commercial: 20/25/30/35/45ns (max.)
- Low-power operation
- Battery Backup operation — 2V data retention
- Produced with advanced high-performance CEMOS™ technology
- Single 5V(±10%) power supply
- Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Available in standard 28-pin (600 mil) CERDIP, 28-pin (300 or 600 mil) plastic DIP, 28-pin (300 mil) ceramic sidebraze DIP, 28-pin (330 mil) SOIC and (300 mil) SOJ, 28-pin CERPACK, 32-pin LCC or PLCC, 28-pin LCC
- Military product compliant to MIL-STD-883, Class B
- This function is listed as Standard Military Drawing #5962-88552 (L-Power) and #5962-88662 (S-Power)

DESCRIPTION:

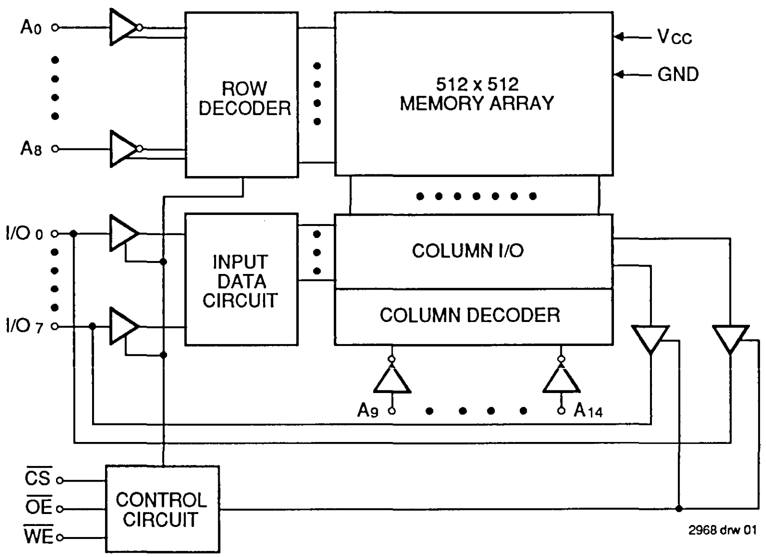
The IDT71256 is a 262,144-bit high-speed static RAM organized as 32K x 8. It is fabricated using IDT's high-performance, high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories. Timing parameters have been specified to meet the speed demands of the fastest IDT79R3000 RISC processors.

Address access times as fast as 20ns are available with power consumption of only 350mW (typ.). The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a low-power standby mode as long as $\overline{CS}$ remains high. In the full standby mode, the low-power device consumes less than 15µW, typically. This capability provides significant system level power and cooling savings. The low power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 5µW when operating off a 2V battery.

The IDT71256 is packaged in a 28-pin (330 mil) gull-wing or (300 or 350 mil) J-bend SOIC, a 28-pin 600 mil CERDIP, 28-pin (300 or 600 mil) plastic DIP, 28-pin (300 mil) ceramic sidebraze DIP, 28-pin CERPACK, 32-pin LCC or PLCC, 28-pin LCC, providing high board-level packing densities.

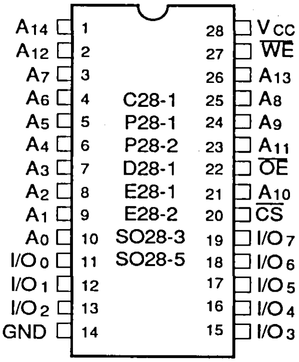
The IDT71256 military RAM is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



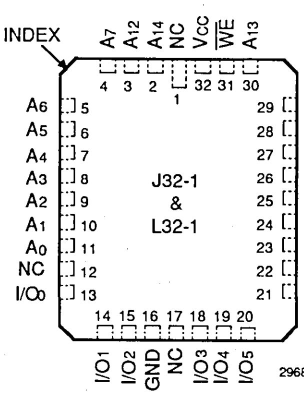
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



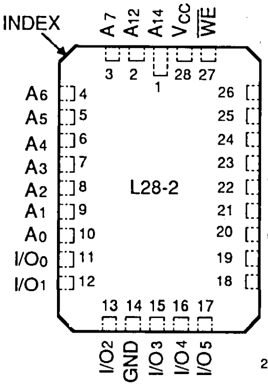
2968 drw 02

DIP/SOJ/SOIC
TOP VIEW



2968 drw 03

32-Pin LCC/PLCC
TOP VIEW



2968 drw 14

28-Pin LCC
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A_0–A_{14}	Addresses
I/O_0–I/O_7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
VCC	Power

2968 tbl 01

TRUTH TABLE[1]

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	I/O	Function
X	H	X	High-Z	Standby (I_{SB})
X	V_{HC}	X	High-Z	Standby (I_{SB1})
H	L	H	High-Z	Output Disable
H	L	L	D_{OUT}	Read
L	L	X	D_{IN}	Write

NOTE: 2968 tbl 02

1. H = V_{IH}, L = V_{IL}, X = Don't Care

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2968 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE: 2968 tbl 04

1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2968 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2968 tbl 06

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS[1, 2]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	71256x20		71256x25		71256x30		71256x35		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open V_{CC} = Max., f = f_{MAX}[3]	S	155	—	145	150	170	180	155	165	mA
		L	135	—	115	130	145	160	130	145	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}[3]	S	20	—	20	20	20	20	20	20	mA
		L	3	—	3	3	3	3	3	3	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, V_{CC} = Max., $V_{LC} \geq V_{IN} \geq V_{HC}$, f = 0	S	15	—	15	20	15	20	15	20	mA
		L	0.4	—	0.4	1.5	0.4	1.5	0.4	1.5	

Symbol	Parameter	Power	71256x45		71256x55		71256x70		71256x85[5]		71256x100		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open V_{CC} = Max., f = f_{MAX}[3]	S	140	150	—	150	—	150	—	150	—	150	mA
		L	120	135	—	125	—	125	—	125	—	125	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}[3]	S	20	20	—	20	—	20	—	20	—	20	mA
		L	3	3	—	3	—	3	—	3	—	3	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, V_{CC} = Max., $V_{LC} \geq V_{IN} \geq V_{HC}$, f = 0	S	15	20	—	20	—	20	—	20	—	20	mA
		L	0.4	1.5	—	1.5	—	1.5	—	1.5	—	1.5	

NOTES: 2968 tbl 07

1. All values are maximum guaranteed values.
2. An "x" in part numbers indicate power rating (S or L).
3. f_{MAX} = $1/t_{RC}$.
4. Standby current mode not available at 20ns.
5. Also available: 120 and 150 ns military devices.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2968 tbl 08

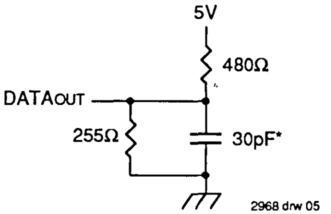


Figure 1. Output Load

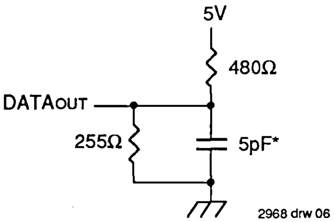


Figure 2. Output Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

*Includes scope and jig capacitances

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

				IDT71256S			IDT71256L			
Symbol	**Parameter**	**Test Condition**		**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL. COM'L.	— —	— —	10 5	— —	— —	5 2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL. COM'L.	— —	— —	10 5	— —	— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.			—	0.4	—	—	0.4	V
		I_{OL} = 10mA, V_{CC} = Min.		—	—	0.5	—	—	0.5	
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	—	2.4	—	—	V

2968 tbl 09

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

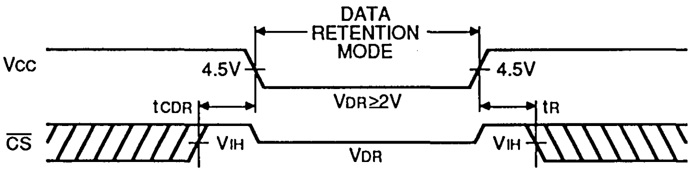
					Typ. (1) Vcc @		Max. Vcc @		
Symbol	**Parameter**	**Test Condition**		**Min.**	**2.0v**	**3.0V**	**2.0V**	**3.0V**	**Unit**
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS}$ ≥ V_{HC} V_{IN} ≥ V_{HC} or ≤ V_{LC}	MIL.	—	—	—	200	800	µA
			COM'L.	—	—	—	120	200	
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	—	—	ns

2968 tbl 10

NOTES:

1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

LOW Vcc DATA RETENTION WAVEFORM



2968 drw 04

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71256S20(1) 71256L20(1)		71256S25 71256L25		71256S30 71256L30		71256S35 71256L35		71256S45 71256L45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
tRC	Read Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
tAA	Address Access Time	—	20	—	25	—	30	—	35	—	45	ns
tACS	Chip Select Access Time	—	20	—	25	—	30	—	35	—	45	ns
tCLZ	Chip Select to Output in Low Z(2)	5	—	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	10	—	11	—	13	—	15	—	20	ns
tOLZ	Output Enable to Output in Low Z(2)	2	—	2	—	2	—	2	—	0	—	ns
tCHZ	Chip Select to Output in High Z(2)	—	10	—	11	—	15	—	15	—	20	ns
tOHZ	Output Disable to Output in High Z(2)	2	8	2	10	2	12	2	15	—	20	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
Write Cycle												
tWC	Write Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
tCW	Chip Select to End of Write	15	—	20	—	25	—	30	—	40	—	ns
tAW	Address Valid to End of Write	15	—	20	—	25	—	30	—	40	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	15	—	20	—	25	—	30	—	35	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tWHZ	Write Enable to Output in High Z(2)	—	10	—	11	—	15	—	15	—	20	ns
tDW	Data to Write Time Overlap	11	—	13	—	14(3)	—	15(3)	—	20	—	ns
tDH1	Data Hold from Write Time ($\overline{WE}$)	0	—	0	—	0	—	0	—	0	—	ns
tDH2	Data Hold from Write Time ($\overline{CS}$)	3	—	3	—	3	—	3	—	3	—	ns
tOW	Output Active from End of Write(2)	5	—	5	—	5	—	5	—	5	—	ns

2968 tbl 11

NOTES:

1. 0° to +70°C temperature range only.
2. This parameter guaranteed but not tested.
3. For the 0°C to +70°C temperature range,
   30ns speed grade, tDW = 14ns.
   35ns speed grade, tDW = 15ns.
   For the -55°C to +125°C temperature range,
   30ns speed grade, tDW = 17ns.
   35ns speed grade, tDW = 18ns.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

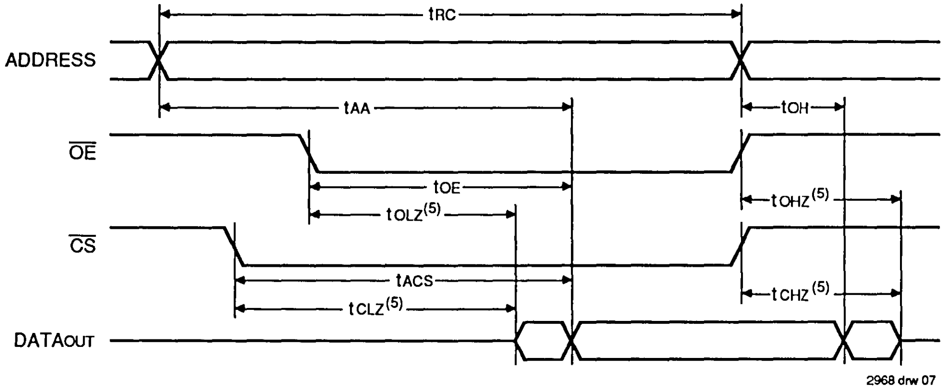
Symbol	Parameter	71256S55(1) 71256L55(1)		71256S70(1) 71256L70(1)		71256S85(1) 71256L85(1)		71256S100(3) 71256L100(3)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
tRC	Read Cycle Time	55	—	70	—	85	—	100	—	ns
tAA	Address Access Time	—	55	—	70	—	85	—	100	ns
tACS	Chip Select Access Time	—	55	—	70	—	85	—	100	ns
tCLZ	Chip Select to Output in Low Z(2)	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	25	—	30	—	35	—	40	ns
tOLZ	Output Enable to Output in Low Z(2)	0	—	0	—	0	—	0	—	ns
tCHZ	Chip Select to Output in High Z(2)	—	25	—	30	—	35	—	40	ns
tOHZ	Output Disable to Output in High Z(2)	0	25	0	30	—	35	—	40	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
Write Cycle										
tWC	Write Cycle Time	55	—	70	—	85	—	100	—	ns
tCW	Chip Select to End of Write	50	—	60	—	70	—	80	—	ns
tAW	Address Valid to End of Write	50	—	60	—	70	—	80	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	40	—	45	—	50	—	55	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tWHZ	Write Enable to Output in High Z(2)	—	25	—	30	—	35	—	40	ns
tDW	Data to Write Time Overlap	25	—	30	—	35	—	40	—	ns
tDH1	Data Hold from Write Time ($\overline{WE}$)	0	—	0	—	0	—	0	—	ns
tDH2	Data Hold from Write Time ($\overline{CS}$)	3	—	3	—	3	—	3	—	ns
tOW	Output Active from End of Write(2)	5	—	5	—	5	—	5	—	ns

2968 tbl 11

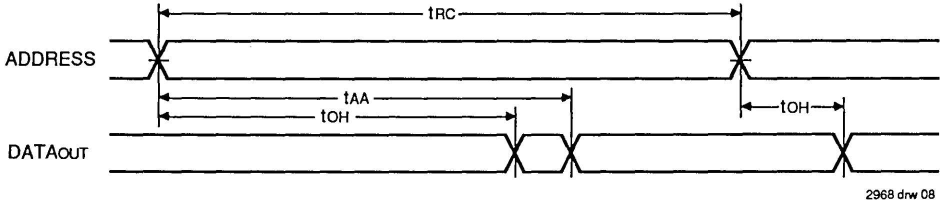
NOTES:

1. -55°C to +125°C temperature range only.
2. This parameter guaranteed but not tested.
3. 0° to +70°C temperature range only.
4. Also available: 120 and 150 ns military devices.
5. For the 0°C to +70°C temperature range,
   30ns speed grade, tDW = 14ns.
   35ns speed grade, tDW = 15ns.
   For the -55°C to +125°C temperature range,
   30ns speed grade, tDW = 17ns.
   35ns speed grade, tDW = 18ns.

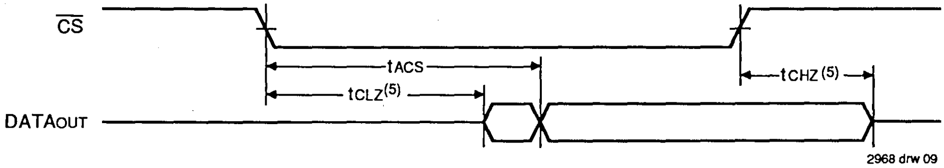
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



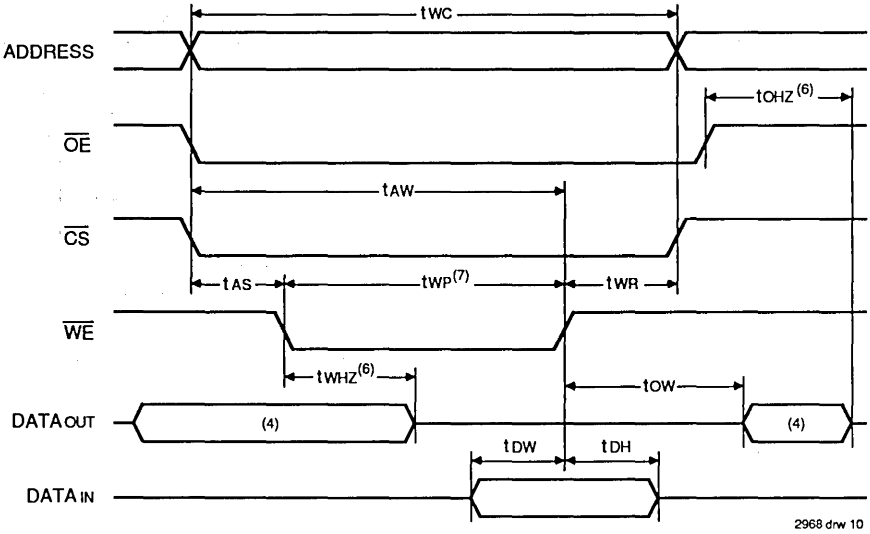
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



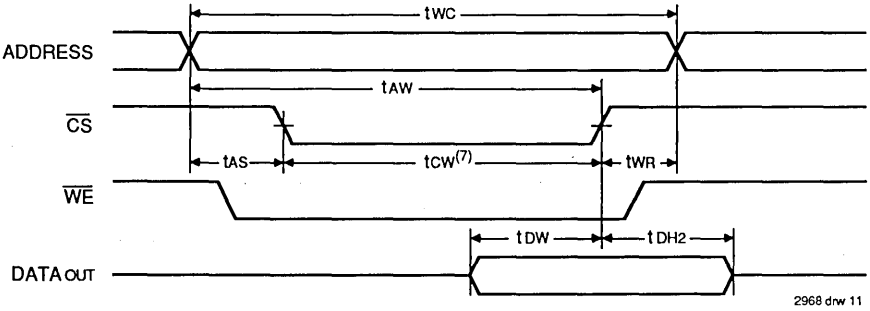
NOTES:

1. WE is high for read cycle.
2. Device is continuously selected, CS = VIL.
3. Address valid prior to or coincident with CS transition low.
4. OE = VIL.
5. Transition is measured ±200mV from steady state with 5pF load (including scope and jig).

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 5, 7)



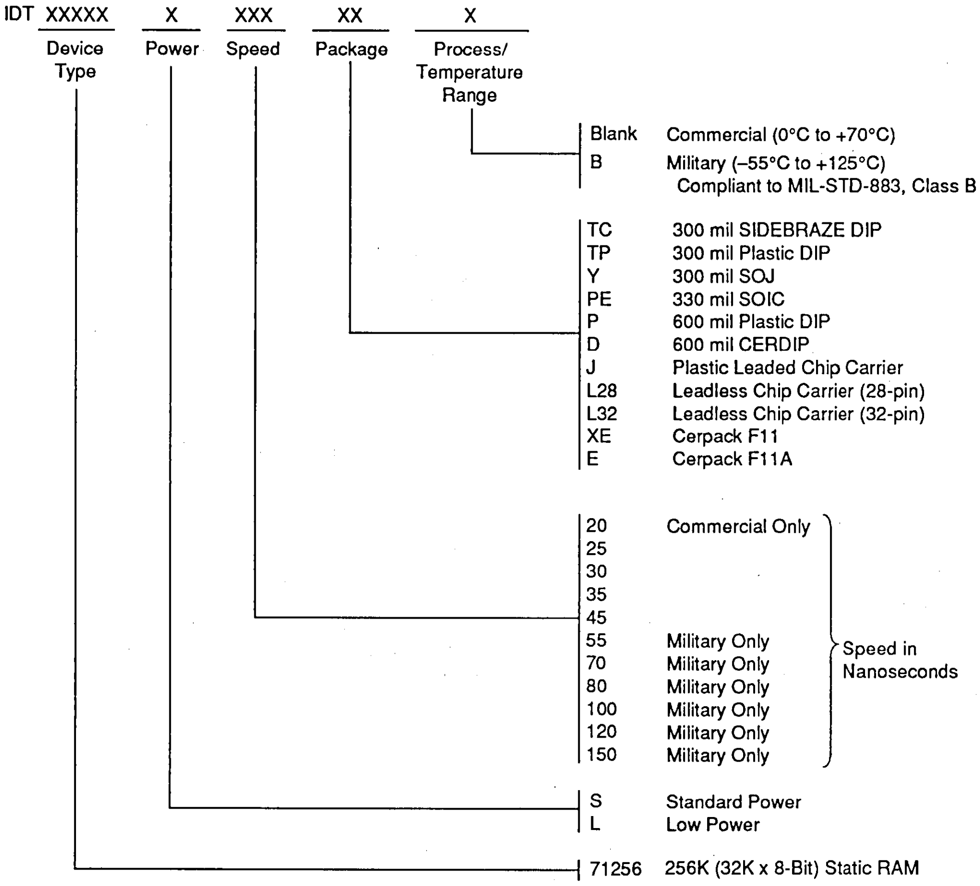
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{CW} or t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the spectified t_{WP}.

ORDERING INFORMATION



IDT XXXXX X XXX XX X

XXXXX	X	XXX	XX	X
Device Type	Power	Speed	Package	Process/ Temperature Range

Process/Temperature Range:

Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Package:

TC	300 mil SIDEBRAZE DIP
TP	300 mil Plastic DIP
Y	300 mil SOJ
PE	330 mil SOIC
P	600 mil Plastic DIP
D	600 mil CERDIP
J	Plastic Leaded Chip Carrier
L28	Leadless Chip Carrier (28-pin)
L32	Leadless Chip Carrier (32-pin)
XE	Cerpack F11
E	Cerpack F11A

Speed in Nanoseconds:

20	Commercial Only
25	
30	
35	
45	
55	Military Only
70	Military Only
80	Military Only
100	Military Only
120	Military Only
150	Military Only

Power:

S	Standard Power
L	Low Power

Device Type:

71256	256K (32K x 8-Bit) Static RAM

2968 drw 12

Integrated Device Technology, Inc.

CMOS STATIC RAM 256K (64K x 4-BIT)

ADVANCE INFORMATION
IDT71258

FEATURES:

- High-speed (equal access and cycle time)
  - Military: 25/35/45/55ns (max.)
  - Commercial: 20/25/35/45ns (max.)
- Low-power operation
  - IDT71258S
    Active: 400mW (typ.)
    Standby: 400µW (typ.)
  - IDT71258L
    Active: 350mW (typ.)
    Standby: 100µW (typ.)
- Battery backup operation — 2V data retention (L version only)
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Available in high-density industry standard 24-pin, 300 mil DIP; 24-pin SOJ and 28-pin LCC
- Three-state outputs
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71258 is a 262,144-bit high-speed static RAM organized as 64K x 4. It is fabricated using IDT's high-performance, high-reliability technology — CEMOS. This state-of-the-art technology, provides a cost effective alternative to bipolar and fast NMOS memories.

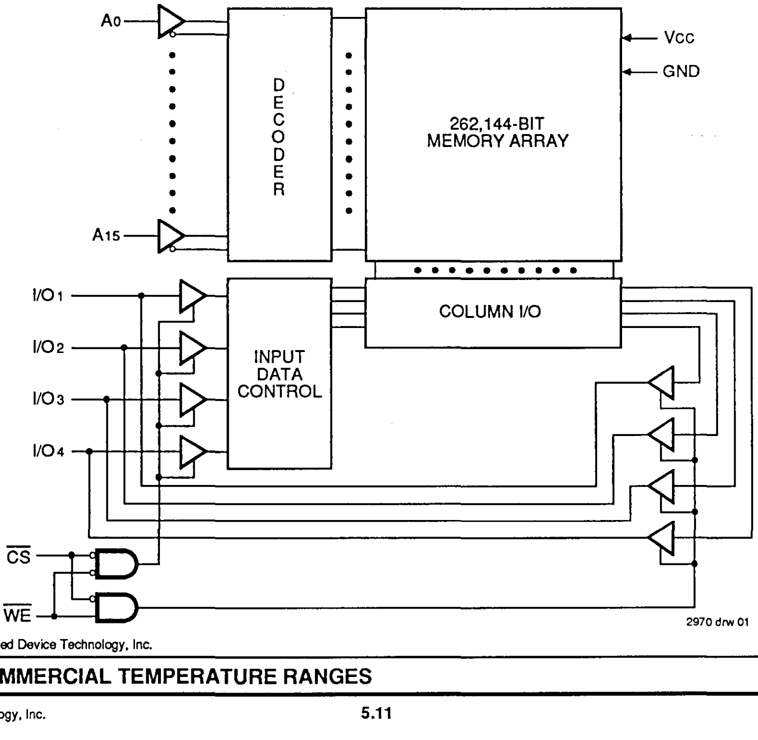
Access times as fast as 20ns are available with typical power consumption of only 350mW. The IDT71258 offers a reduced power standby mode, I_{SB1}, which enables the designer to greatly reduce device power requirements . This capability provides significant system level power and cooling savings. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 100µW operation from a 2V battery.

All inputs and outputs of the IDT71258 are TTL-compatible and operation is from a single 5V supply, simplifying system designs.

The IDT71258 is packaged in a 24-pin, 300 mil DIP; a 24-pin SOJ and a 28-pin LCC.

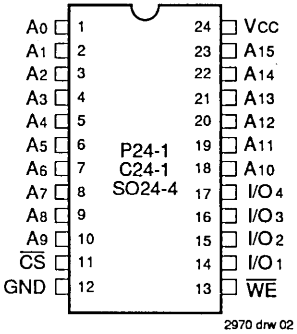
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

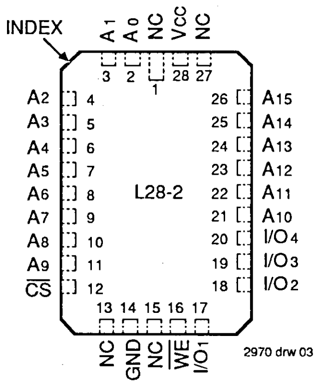


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP/SOJ
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A0–A15	Addresses
I/O1–I/O4	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
GND	Ground
Vcc	Power

2970 tbl 01

TRUTH TABLE[1]

$\overline{WE}$	$\overline{CS}$	I/O	Power
X	H	High-Z	Standby (I_{SB})
X	V_{HC}	High-Z	Standby (I_{SB1})
H	L	D_{OUT}	Read
L	L	D_{IN}	Write

NOTE: 2970 tbl 02

1. H = V_{IH}, L = V_{IL}, X = Don't Care

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2970 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE: 2970 tbl 04

1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2970 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE:

2970 tbl 06

1. V_{IL} = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	71258S20 71258L20		71258S25 71258L25		71258S35 71258L35		71258S45 71258L45		71258S55 71258L55		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = 0[2]	S	110	—	100	110	100	110	100	110	—	110	mA
		L	100	—	90	100	90	100	90	100	—	100	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = f_{MAX}[2]	S	160	—	150	160	150	160	150	160	—	160	mA
		L	140	—	130	140	130	140	130	140	—	140	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max. Outputs Open, f = f_{MAX}[2]	S	35	—	35	35	35	35	35	35	—	35	mA
		L	20	—	20	20	20	20	20	20	—	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max. f = 0[2]	S	30	—	30	35	30	35	30	35	—	35	mA
		L	1.5	—	1.5	4.5	1.5	4.5	1.5	4.5	—	4.5	

NOTES:

2970 tbl 07

1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2970 tbl 08

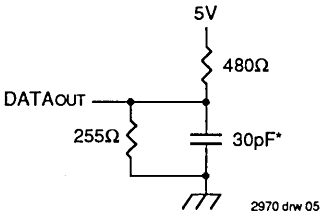


Figure 1. Output Load

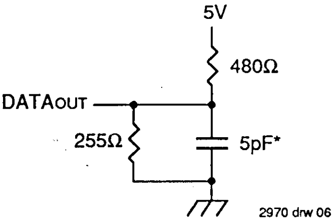


Figure 2. Output Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

*Includes scope and jig capacitances

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT71258S Min.	IDT71258S Typ.	IDT71258S Max.	IDT71258L Min.	IDT71258L Typ.	IDT71258L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL COM'L	— —	— —	10 5	— —	— —	5 2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL COM'L	— —	— —	10 5	— —	— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min. I_{OL} = 10mA, V_{CC} = Min.		 —	— —	0.4 0.5	— —	— —	0.4 0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	—	2.4	—	—	V

2970 tbl 09

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

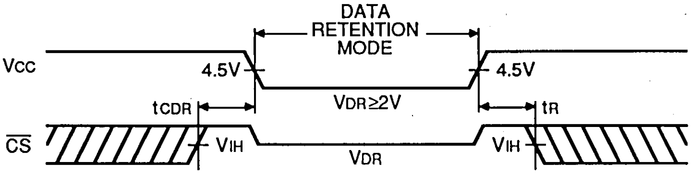
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

					Typ.[1] Vcc @		Max. Vcc @		
Symbol	Parameter	Test Condition		Min.	2.0v	3.0V	2.0V	3.0V	Unit
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS}$ ≥ V_{HC}	MIL. COM'L.	— —	50 50	75 75	2000 500	3000 750	µA
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	—	—	ns

2970 tbl 10

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

LOW Vcc DATA RETENTION WAVEFORM



2970 drw 04

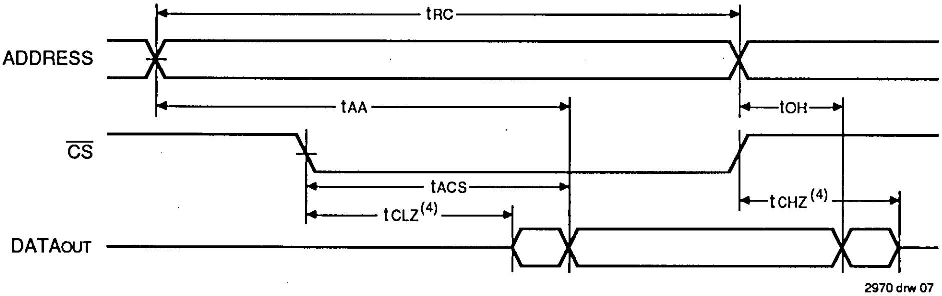
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

		71258S20(1) 71258L20(1)		71258S25(2) 71258L25(2)		71258S35 71258L35		71258S45 71258L45		71258S55(2) 71258L55(2)		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
Read Cycle												
t_{RC}	Read Cycle Time	20	—	25	—	35	—	45	—	55	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	35	—	45	—	55	ns
t_{ACS}	Chip Select Access Time	—	20	—	25	—	35	—	45	—	55	ns
t_{CLZ}	Chip Select to Output in Low Z(3)	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}	Chip Select to Power Up Time(3)	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Deselect to Power Down Time(3)	—	20	—	25	—	35	—	45	—	55	ns
t_{CHZ}	Chip Select to Output in High Z(3)	—	10	—	13	—	15	—	20	—	25	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
Write Cycle												
t_{WC}	Write Cycle Time	20	—	20	—	30	—	40	—	50	—	ns
t_{CW}	Chip Select to End of Write	15	—	20	—	30	—	40	—	50	—	ns
t_{AW}	Address Valid to End of Write	15	—	20	—	30	—	40	—	50	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	20	—	30	—	40	—	50	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}	Write Enable to Output in High Z(3)	—	10	—	11	—	15	—	20	—	25	ns
t_{DW}	Data Valid to End of Write	11	—	15	—	20	—	25	—	30	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{OW}	Output Active from End of Write(3)	5	—	5	—	5	—	5	—	5	—	ns

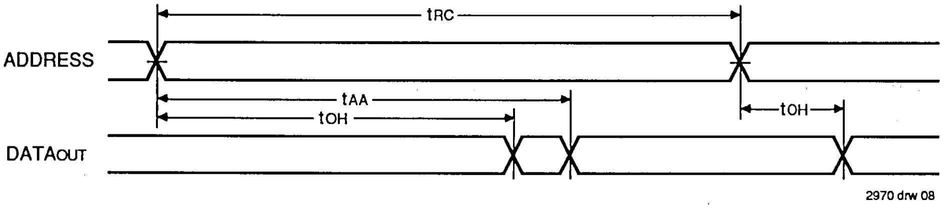
2970 tbl 11

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

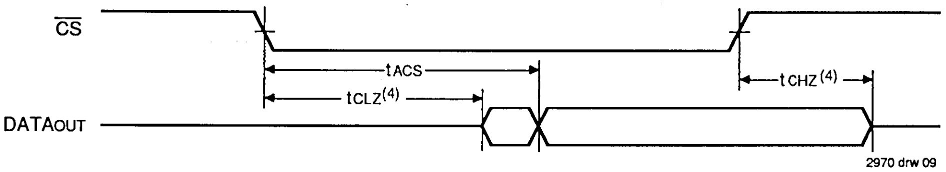
TIMING WAVEFORM OF READ CYCLE NO. 1[(1)]



TIMING WAVEFORM OF READ CYCLE NO. 2[(1, 2)]



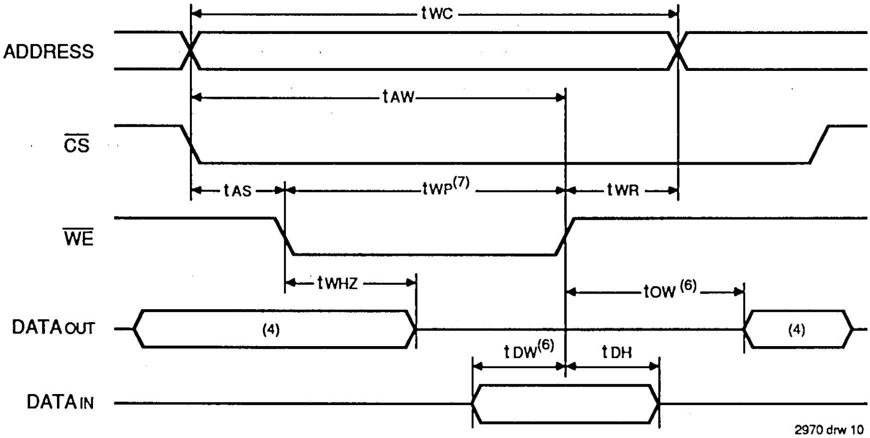
TIMING WAVEFORM OF READ CYCLE NO. 3[(1, 3)]



NOTES:

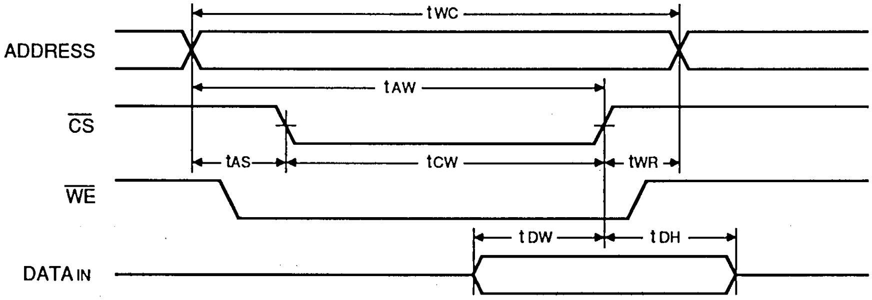
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state with 5pF load (including scope and jig).

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3)



2970 drw 10

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



2970 drw 11

NOTES:

1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (tCW or tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).
7. During a $\overline{WE}$ controlled write cycle, the pulse width must be the larger of tWP or (tDW + tWHZ) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW.

ORDERING INFORMATION

IDT	XXXXX	X	XX	X	X
	Device Type	Power	Speed	Package	Process/ Temperature Range

Process/Temperature Range:

Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Package:

TP	Plastic DIP (300 Mil)
TC	Sidebraze DIP (300 Mil)
Y	Small Outline IC (J-Bend)
L28	28 Leadless Chip Carrier

Speed (Speed in Nanoseconds):

20	Commercial Only
25	
35	
45	
55	Military Only

Power:

S	Standard Power
L	Low Power

Device Type:

71258	256K (64K x 4-Bit) Static RAM

2970 drw 12

Integrated Device Technology, Inc.

32K x 9-BIT STATIC RAM

ADVANCE INFORMATION
IDT71259

FEATURES:

- 32K x 9 Static RAM
- High-speed address / chip select time
  - Military: 25/35/45ns
  - Commercial: 20/25/35ns
- Low Power Operation
  - IDT71259S
    Active: 450 mW (typ.)
    Standby: 300 mW (typ.)
  - IDT71259L
    Active: 350 mW (typ.)
    Standby: 200 mW (typ.)
- Two Chip Selects plus one Output Enable pin
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Battery back-up operation - 2V data retention
- Available in 32-pin 300-mil side-brazed and plastic DIP and 32-pin 300-mil SOJ
- Military product is fully compliant to MIL-STD-883, Class B

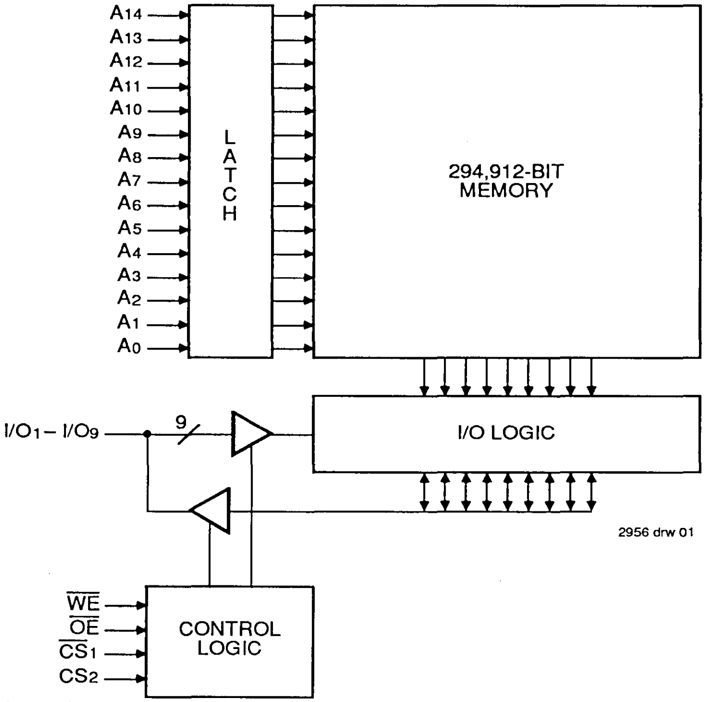
DESCRIPTION:

The IDT71259 is a 294,912-bit high-speed static RAM organized as 32Kx9. It is fabricated using IDT's high-performance high-reliability CEMOS technology. This state-of-the-art technology is combined with innovative circuit design techniques to provide a cost-effective solution for high-speed memory needs.

Address access times as fast as 20ns are available with power consumption of only 450 mW (typ.). The circuit also offers a reduced power standby mode. When CS_1 goes high, the circuit will automatically go to, and remain in, a low-power standby mode as long as CS_1 remains high. In the full standby mode, the low-power device consumes less than 200 mW (typ.). This capability provides significant system level power and cooling savings. The low-power (L) version offers a battery backup data retention capability where the circuit typically consumes only 20µW when operating off a 2V battery.

All inputs and outputs of the IDT71259 are TTL-compatible and operation is from a single 5V supply. During write cycles, address and data setup times are relaxed.

FUNCTIONAL BLOCK DIAGRAM



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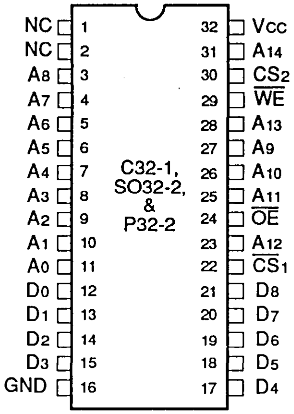
MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1990**

DESCRIPTION (Continued)

The IDT71259 is packaged in a 32-pin 300-mil sidebrazed ceramic DIP, 32-pin 300 mil plastic DIP and 32-pin SOIC.

The IDT71259 military RAM is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS



2956 drw 02

DIP/SOJ
TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +125	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2956 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE[1]

CS_2	$\overline{CS}_1$	$\overline{OE}$	$\overline{WE}$	I/O	Function
X	H	X	X	Hi Z	Deselect chip and Power Down
L	X	X	X	Hi Z	Deselect Chip
H	L	L	H	D_{OUT}	Read
H	L	X	L	D_{IN}	Write
H	L	H	X	Hi Z	Output Disabled

NOTE: 2956 tbl 01

1. H=V_{IH}, L=V_{IL}, X=Don't Care

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE: 2956 tbl 03

1. This parameter is guaranteed by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5	—	0.8	V

NOTE: 2956 tbl 04

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, T_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	71259S20 71259L20		71259S25 71259L25		71259S35 71259L35		71259S45 71259L45		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current $\overline{CS}_1 \le V_{IL}$, Outputs Open V_{CC} = Max., f = 0	S	110	—	110	120	110	120	—	120	mA
		L	90	—	90	100	90	100	—	100	
I_{CC2}	Dynamic Operating Current $\overline{CS}_1 \le V_{IL}$, Outputs Open V_{CC} = Max., f = f_{MAX}[2]	S	160	—	145	160	135	150	—	145	mA
		L	140	—	125	140	115	130	—	125	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}_1 \ge V_{IH}$, V_{CC} = Max., f = f_{MAX}[2]	S	70	—	60	65	55	65	—	60	mA
		L	55	—	45	50	40	45	—	40	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}_1 \ge V_{HC}$, $V_{IN} \le V_{LC}$ or $\ge V_{HC}$ V_{CC} = Max., f = 0	S	10	—	10	40	10	40	—	40	mA
		L	1	—	1	4	1	4	—	4	

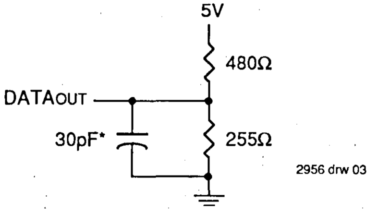
2956 tbl 05

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = $1/t_{RC}$.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2956 tbl 06



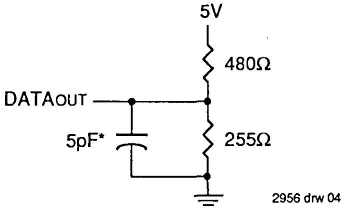


Figure 1. AC Test Loads **(for t_{OLZ}, t_{CLZ}, t_{OHZ}, t_{WHZ}, t_{CHZ}, t_{OW})**

*Including scope and jig

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

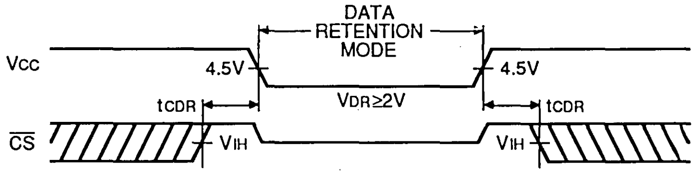
				Typ.[1] Vcc @		Max. Vcc @		
Symbol	**Parameter**	**Test Condition**	**Min.**	**2.0v**	**3.0V**	**2.0V**	**3.0V**	**Unit**
V_{DR}	V_{CC} for Data Retention	—	2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	MIL. COM'L.	— —	— —	— —	— —	— —	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time	—	0	—	—	—	—	ns
t_R[3]	Operation Recovery Time	$\overline{CS}_1 \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	t_{RC}[2]	—	—	—	—	ns
$\lvert I_{LI} \rvert$[3]	Input Leakage Current	—	—	—	—	—	—	µA

2956 tbl 07

NOTES:

1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed but not tested.

LOW Vcc DATA RETENTION WAVEFORM



2956 drw 05

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

			IDT71259		
Symbol	**Parameter**	**Test Condition**	**Min.**	**Max.**	**Unit**
$\lvert I_{LI} \rvert$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	2.0	µA
$\lvert I_{LO} \rvert$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	2.0	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.	—	0.4	
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	—	V

2956 tbl 08

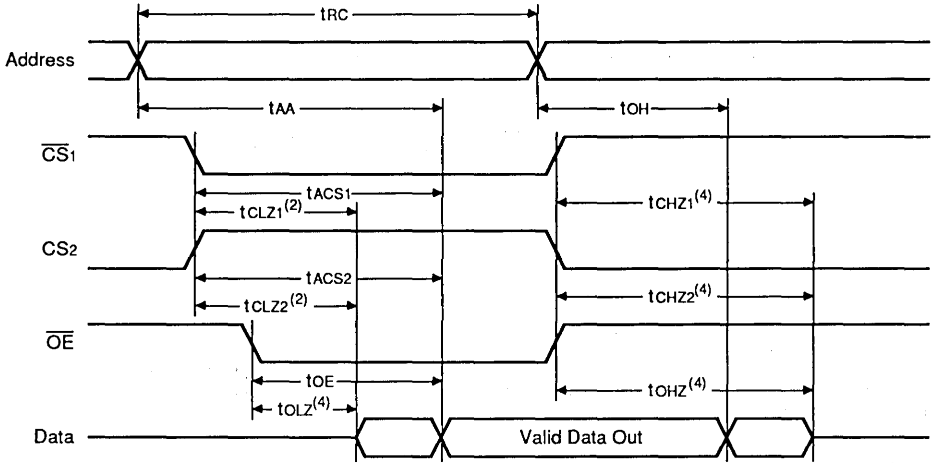
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71259S20(2) 71259L20(2) Min.	71259S20(2) 71259L20(2) Max.	71259S25 71259L25 Min.	71259S25 71259L25 Max.	71259S35 71259L35 Min.	71259S35 71259L35 Max.	71259S45(3) 71259L45(3) Min.	71259S45(3) 71259L45(3) Max.	Unit
Read Cycle										
t_{RC}	Read Cycle Time	20	—	25	—	35	—	45	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	35	—	45	ns
t_{ACS1}	$\overline{CS}$ Access Time (CS_1)	—	17	—	25	—	35	—	45	ns
t_{ACS2}	$\overline{CS}$ Access Time (CS_2)	—	12	—	15	—	25	—	35	ns
t_{CLZ1}(2)	$\overline{CS}$ to Output in Low Z (CS_1)	3	—	3	—	5	—	5	—	ns
t_{CLZ2}(2)	$\overline{CS}$ to Output in Low Z (CS_2)	3	—	3	—	5	—	5	—	ns
t_{CHZ1}(2)	$\overline{CS}$ to Output in High Z (CS_1)	—	8	—	10	—	14	—	14	ns
t_{CHZ2}(2)	$\overline{CS}$ to Output in High Z (CS_2)	—	8	—	10	—	14	—	14	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	8	—	10	—	14	—	14	ns
t_{OLZ}(2)	$\overline{OE}$ to Output Low Z	2	—	2	—	4	—	4	—	ns
t_{OHZ}(2)	$\overline{OE}$ to Output High Z	—	8	—	10	—	14	—	14	ns
t_{OH}	Out Hold from Add Change	2	—	2	—	3	—	4	—	ns
Write Cycle										
t_{WC}	Write Cycle Time	20	—	25	—	35	—	45	—	ns
t_{AW}	Add to End of Write	12	—	15	—	25	—	25	—	ns
t_{CW1}	$\overline{CS}$ to End of Write (CS_1)	14	—	16	—	20	—	20	—	ns
t_{CW2}	$\overline{CS}$ to End of Write (CS_2)	10	—	12	—	16	—	16	—	ns
t_{WP}	Write Pulse Width	12	—	15	—	25	—	25	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}(2)	$\overline{WE}$ to Output in High Z	—	8	—	10	—	15	—	15	ns
t_{DW}	Data Set-Up Time	10	—	12	—	18	—	18	—	ns
t_{DH}	Data Hold from Write	0	—	0	—	0	—	0	—	ns
t_{OW}(2)	Output Active from End of $\overline{WE}$	5	—	5	—	5	—	5	—	ns

2956 tbl 09

NOTE:
1. 0° to +70°C temperature range only.
2. This parameter is guaranteed by design, but not tested.
3. -55° to +125°C temperature range only.

TIMING WAVEFORM OF READ CYCLE(1, 3)

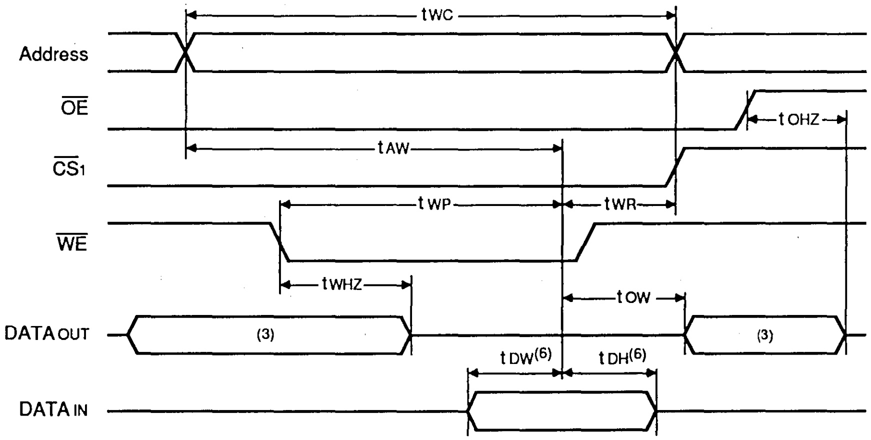


2956 drw 06

NOTES:

1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected when $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state with 5pF load (including scope and jig).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CYCLE)(1, 2, 4, 5)

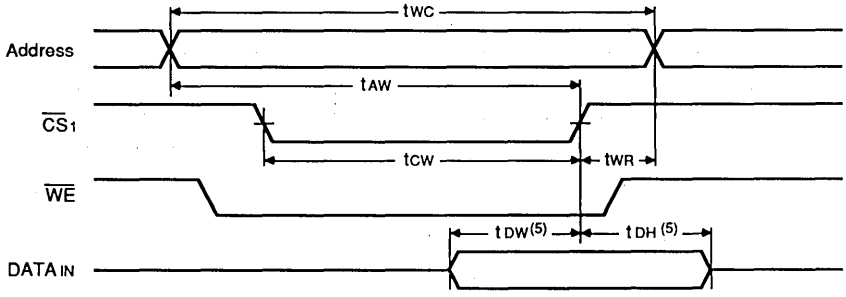


2956 drw 07

NOTES:

1. A write occurs during the overlap (t_{WC} and t_{WP}) of $\overline{CS}_1$ low, $\overline{WE}$ low and CS_2 high.
2. t_{WP} is measured from the earlier of $\overline{CS}_1$, CS_2 or $\overline{WE}$ being deasserted.
3. During this period, the I/O pins are in the output state, and input signals must not be applied on these pins.
4. If $\overline{CS}_1$ and CS_2 are asserted coincident with or after $\overline{WE}$ goes low, the output will remain in a high impedance state.
5. If $\overline{CS}_1$ or CS_2 is deasserted coincident with or before $\overline{WE}$ goes high, the output will remain in a high impedance state.
6. The transition is measured ±200mV from steady state with a 5pF load.

TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{\text{CS}}$ CYCLE)(1, 2, 3, 4)



2956 drw 08

NOTES:

1. A write occurs during the overlap (t_{WC} and t_{WP}) of $\overline{\text{CS}}_1$ low, $\overline{\text{WE}}$ low and CS_2 high.
2. t_{WP} is measured from the earlier of $\overline{\text{CS}}_1$, CS_2 or $\overline{\text{WE}}$ being deasserted.
3. If $\overline{\text{CS}}_1$ and CS_2 are asserted coincident with or after $\overline{\text{WE}}$ goes low, the output will remain in a high impedance state.
4. If $\overline{\text{CS}}_1$ or CS_2 is deasserted coincident with or before $\overline{\text{WE}}$ goes high, the output will remain in a high impedance state.
5. The transition is measured ±200mV from steady state with a 5pF load.

ORDERING INFORMATION

IDT	XXXX	XX	XXX	X	X
	Device Type	Power	Speed	Package	Process/ Temperature Range

Process/Temperature Range

Code	Description
Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Package

Code	Description
TP	300-mil Plastic DIP
Y	300-mil SOJ
TC	300-mil Sidebraze DIP

Speed (Speed in Nanoseconds)

Code	Description
20	Commercial Only
25	
35	
45	Military Only

Power

Code	Description
S	Standard Power
L	Low Power

Device Type

Code	Description
71259	32K x 9 SRAM

Integrated Device Technology, Inc.

CMOS STATIC RAMS
256K (64K x 4-BIT)
Separate Data Inputs and Outputs

ADVANCE INFORMATION
IDT71281S/L
IDT71282S/L

FEATURES:

- Separate data inputs and outputs
- IDT71281S/L: outputs track inputs during write mode
- IDT71282S/L: high impedance outputs during write mode
- High speed (equal access and cycle time)
  - — Military: 30/35/45/55ns (max.)
  - — Commercial: 25/35/45ns (max.)
- Low power consumption
  - — IDT71281/2S
    Active: 400mW (typ.)
    Standby: 400µw (typ.)
  - — IDT71281/2L
    Active: 350mW (typ.)
    Standby: 100µw (typ.)
- Battery backup operation — 2V data retention (L version only)
- High-density 28-pin DIP, 28-pin SOJ, and 28-pin LCC
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (+10%) power supply
- Inputs and outputs directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Military product compliant to MIL-STD-8831 Class B

DESCRIPTION:

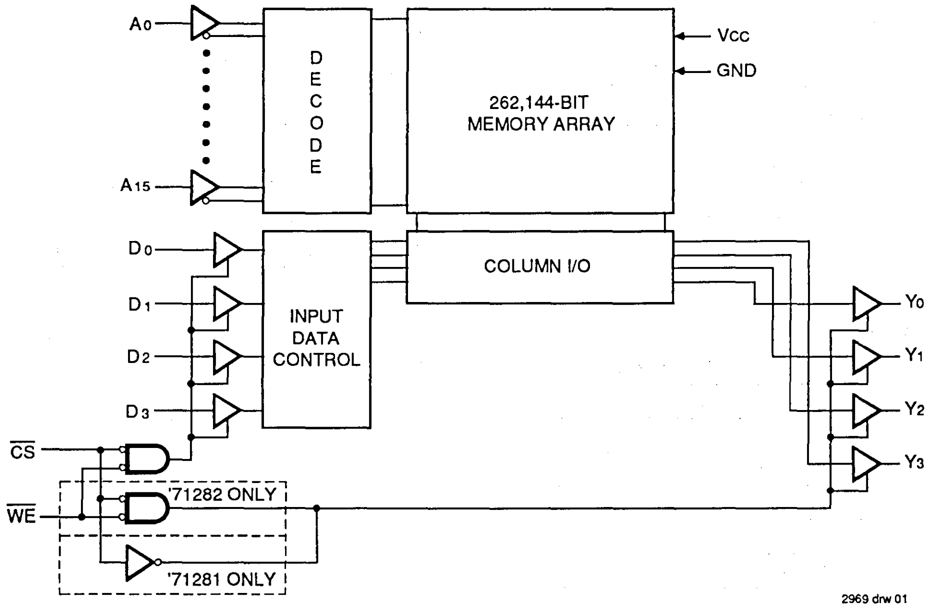
The IDT71281/IDT71282 are 262,144-bit high-speed static RAMs organized as 64K x 4. They are fabricated using IDT's high-performance, high-reliability technology — CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories.

Access times as fast as 25ns are available with typical power consumption of only 350mW. These circuits also offer a reduced power standby mode (I_{SB}). When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, this standby mode. The ultralow-power standby mode capability provides significant system level power and cooling savings. The low-power (L) versions also offer a battery backup data retention capability where the circuit typically consumes only 100µW operating off a 2V battery.

All inputs and outputs of the IDT71281/IDT71282 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

The IDT71281/IDT71282 are packaged in 28-pin sidebraze and plastic DIPs, SOJs and LCCs providing high board-level packing densities.

FUNCTIONAL BLOCK DIAGRAM

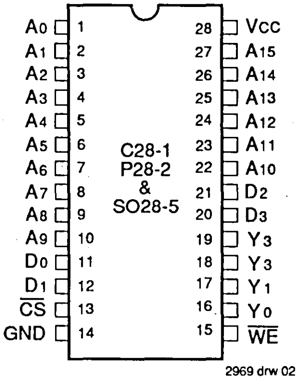


CEMOS is a trademark of Integrated Device Technology, Inc.

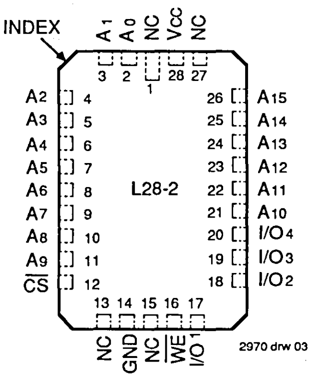
DESCRIPTION (Continued)

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



DIP/SOJ
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A0–A15	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
VCC	Power
D0–D3	DATAIN
Y0–Y3	DATAOUT
GND	Ground

2969 tbl 01

TRUTH TABLE[1]

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High-Z	Standby
Read	L	H	DOUT	Active
Write[1]	L	L	DIN	Active
Write[2]	L	L	High-Z	Active

NOTE: 2969 tbl 02

1. For IDT71281 only.
2. For IDT71282 only.
3. H = VIH, L = VIL, X = Don't Care.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

NOTE: 2969 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	11	pF
COUT	Output Capacitance	VOUT = 0V	11	pF

NOTE: 2969 tbl 04

1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2969 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2969 tbl 06

1. V_{IL} (min.)= -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	71281/2S25 71281/2L25		71281/2S30 71281/2L30		71281/2S35 71281/2L35		71281/2S45 71281/2L45		71281/2S55 71281/2L55		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = 0[3]	S	130	—	—	140	120	130	120	130	—	130	mA
		L	120	—	—	130	110	120	110	120	—	120	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = f_{MAX}[2]	S	170	—	—	180	160	170	160	170	—	170	mA
		L	150	—	—	150	130	140	130	140	—	150	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}[2]	S	35	—	—	35	35	35	35	35	—	35	mA
		L	20	—	—	20	20	20	20	20	—	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., f = 0[2]	S	30	—	—	35	30	35	30	35	—	35	mA
		L	1.5	—	—	4.5	1.5	4.5	1.5	4.5	—	4.5	

NOTES: 2969 tbl 07

1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2969 tbl 08

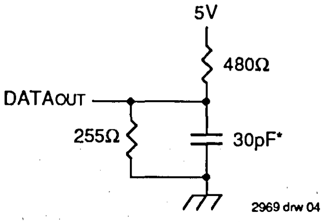


Figure 1. Output Load

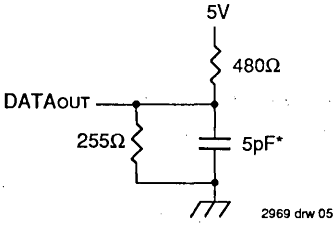


Figure 2. Output Load
(for tCLZ, tCHZ, tOW, and tWHZ)

*Includes scope and jig capacitances

DC ELECTRICAL CHARACTERISTICS

Vcc = 5.0V ± 10%

				IDT71281S/L			IDT71282S/L			
Symbol	**Parameter**	**Test Condition**		**Min.**	**Typ.[1]**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**
|ILI|	Input Leakage Current	Vcc = Max., VIN = GND to Vcc	MIL COM'L	— —	— —	10 5	— —	— —	5 2	µA
|ILO|	Output Leakage Current	Vcc = Max., $\overline{CS}$ = VIH, VOUT = GND to Vcc	MIL COM'L	— —	— —	10 5	— —	— —	5 2	µA
VOL	Output Low Voltage	IOL = 8mA, Vcc = Min. IOL = 10mA, Vcc = Min.		 —	— —	0.4 0.5	— —	— —	0.4 0.5	V
VOH	Output High Voltage	IOH = -4mA, Vcc = Min.		2.4	—	—	2.4	—	—	V

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) VLC = 0.2V, VHC = Vcc - 0.2V

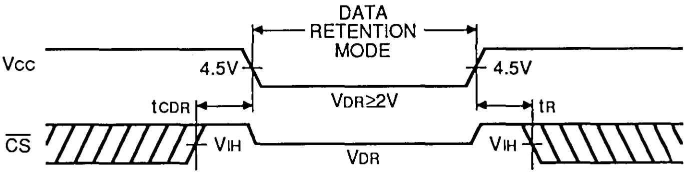
					Typ.[1] Vcc @		Max. Vcc @		
Symbol	**Parameter**	**Test Condition**		**Min.**	**2.0v**	**3.0V**	**2.0V**	**3.0V**	**Unit**
VDR	Vcc for Data Retention	—		2.0	—	—	—	—	V
ICCDR	Data Retention Current	$\overline{CS}$ ≥ VHC	MIL. COM'L.	— —	50 50	75 75	2000 500	3000 750	µA
tCDR[3]	Chip Deselect to Data Retention Time			0	—	—	—	—	ns
tR[3]	Operation Recovery Time			tRC[2]	—	—	—	—	ns
|ILI|[3]	Input Leakage Current			—	—	—	2	2	µA

NOTES:

2969 tbl 10

1. TA = +25°C.
2. tRC = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



2969 drw 03

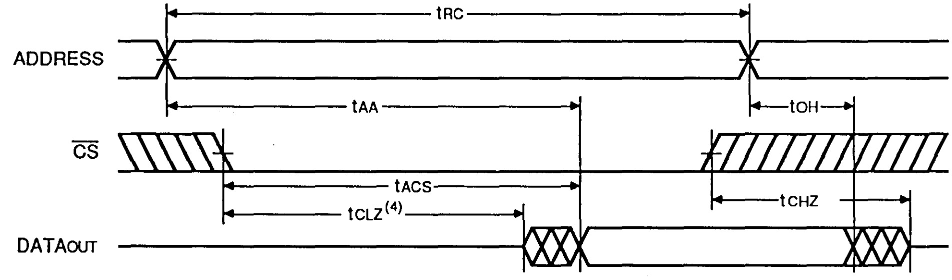
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71281S/L25(1) 71282S/L25(1)		71281S/L30(2) 71282S/L30(2)		71281S/L35 71282S/L35		71281S/L45 71282S/L45		71281S/L55(2) 71282S/L55(2)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t_{RC}	Read Cycle Time	25	—	30	—	35	—	45	—	55	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	35	—	45	—	55	ns
t_{ACS}	Chip Select Access Time(3)	—	25	—	30	—	35	—	45	—	55	ns
t_{CLZ}	Chip Select to Output in Low Z(4)	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}	Chip Select to Output in High Z(4)	—	13	—	13	—	15	—	20	—	25	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}	Chip Select to Power Up Time(4)	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Deselect to Power Down Time(4)	—	25	—	30	—	35	—	45	—	55	ns
Write Cycle												
t_{WC}	Write Cycle Time	20	—	20	—	30	—	40	—	50	—	ns
t_{CW}	Chip Select to End of Write(3)	20	—	20	—	30	—	40	—	50	—	ns
t_{AW}	Address Valid to End of Write	20	—	20	—	30	—	40	—	50	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	20	—	30	—	40	—	50	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}	Write Enable to Output in High Z(4,7)	—	13	—	13	—	15	—	20	—	25	ns
t_{DW}	Data Valid to End of Write	15	—	15	—	20	—	25	—	30	—	ns
t_{DH}	Data HoldTime	0	—	0	—	0	—	0	—	0	—	ns
t_{OW}	Output Active from End of Write(4,7)	5	—	5	—	5	—	5	—	5	—	ns
t_{IY}	Data Valid to Output Valid(4,6)	—	20	—	20	—	30	—	35	—	40	ns
t_{WY}	Write Enable to Output Valid(4,6)	—	20	—	20	—	30	—	35	—	40	ns

NOTES: 2969 tbl 11

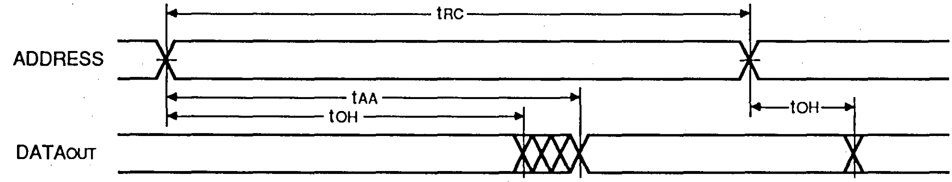
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Both chip selects must be active low for the device to be selected.
4. This parameter guaranteed but not tested.
5. Preliminary data for military devices only.
6. For IDT71281S/L only.
7. For IDT71282S/L only.

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



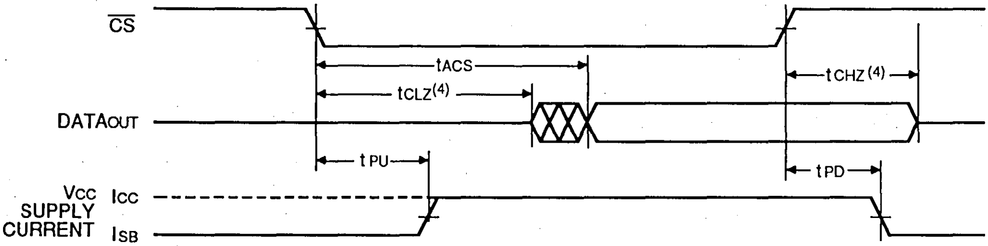
2969 drw 06

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2)



2969 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3)

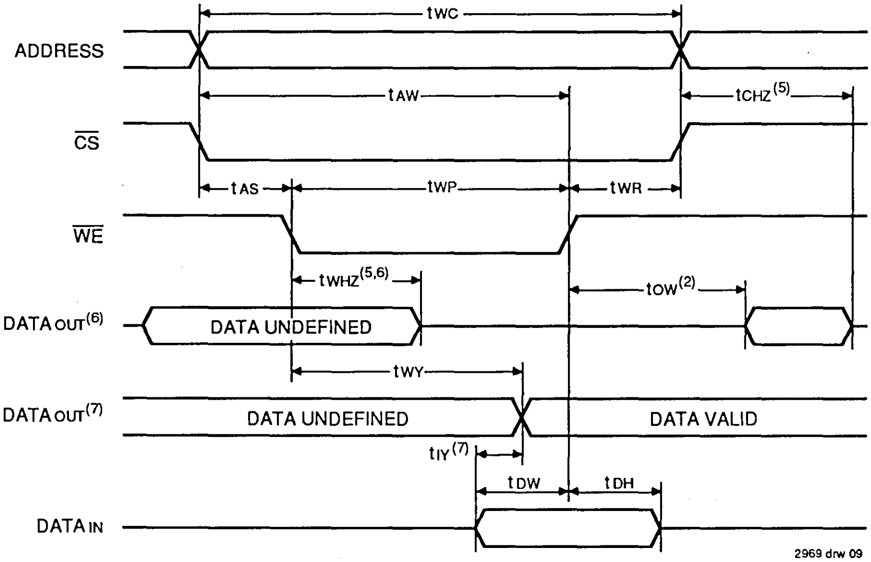


2969 drw 08

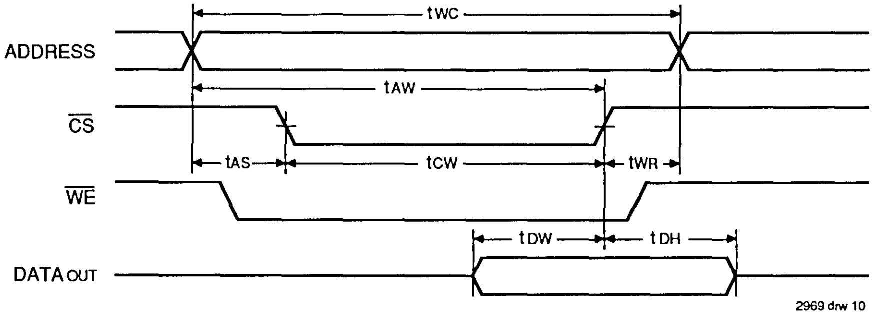
NOTES:

1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{\text{WE}}$ CONTROLLED TIMING)(1, 2, 3)



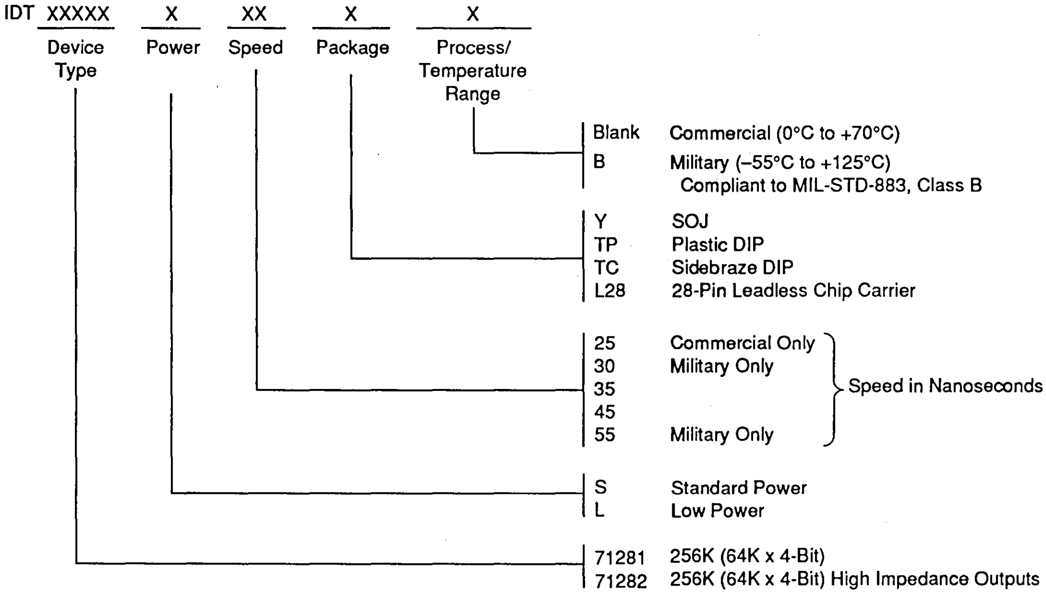
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{\text{CS}}$ CONTROLLED TIMING)(1, 2, 3, 4)



NOTES:

1. $\overline{\text{WE}}$ or $\overline{\text{CS}}$ must be high during all address transitions.
2. A write occurs during the overlap (tCW or tWP) of a low $\overline{\text{CS}}$ and a low $\overline{\text{WE}}$.
3. tWR is measured from the earlier of $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high to the end of the write cycle.
4. If the $\overline{\text{CS}}$ low transition occurs simultaneously with or after the $\overline{\text{WE}}$ low transition, the outputs remain in a high impedance state.
5. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).
6. IDT71282 only.
7. IDT71281 only.

ORDERING INFORMATION



Field	Code	Description
Process/Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B
Package	Y	SOJ
	TP	Plastic DIP
	TC	Sidebraze DIP
	L28	28-Pin Leadless Chip Carrier
Speed	25	Commercial Only
	30	Military Only
	35	
	45	
	55	Military Only
Power	S	Standard Power
	L	Low Power
Device Type	71281	256K (64K x 4-Bit)
	71282	256K (64K x 4-Bit) High Impedance Outputs

2969 drw 11

Integrated Device Technology, Inc.

CMOS HIGH-SPEED STATIC RAM 72K (8K x 9-BIT)
With Address Latches

PRELIMINARY INFORMATION
IDT71569

FEATURES:

- 8192-words x 9-bits organization
- Address Latch
- Fast access time:
  - — Commercial: 20/25ns
  - — Military: 25/35ns
- Battery backup operation – 2V data retention voltage (L-version only)
- Produced with advanced CEMOS™ high-performance technology
- Single 5V power supply
- Inputs and outputs directly TTL compatible
- Military product available compliant to MIL-STD-883, Class B
- JEDEC standard 28-pin DIP and SOJ plastic packages

DESCRIPTION:

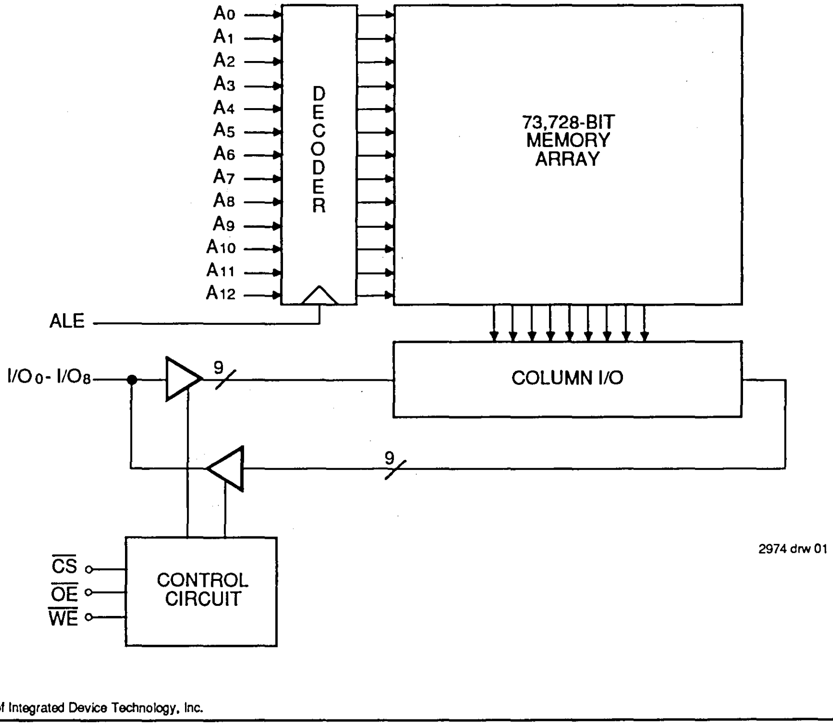
The IDT71569 is a 73,728-bit high-speed static RAM, organized as 8K x 9, with address latches. It is fabricated using IDT's high-performance, high-reliability CEMOS technology.

The IDT71569 offers address access times as fast as 10ns. The ninth bit is optimal for systems using parity. This device is ideally suited for cache memory applications.

All inputs and outputs of the IDT71569 are TTL-compatible. The IDT71569 is packaged in an industry standard 300-mil 28-pin DIP and SOJ plastic packages.

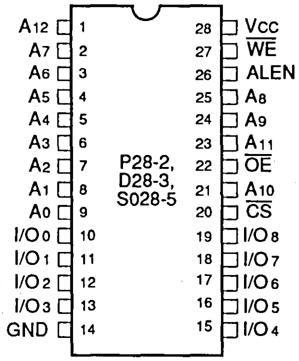
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



2974 drw 02

DIP/SOJ
TOP VIEW

TRUTH TABLE[1]

ALE	$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	I/O	Function
X	H	X	X	Hi-Z	Deselect chip
H	X	X	X	X	Address Latch Transparent
L	X	X	X	X	Address Latch Closed
H	L	L	H	D_{OUT}	Read From Current Address
L	L	L	H	D_{OUT}	Read From Latched Address
H	L	X	L	D_{IN}	Write to Current Address
L	L	X	L	D_{IN}	Write to Latched Address
X	L	H	H	Hi-Z	Outputs Disabled

NOTE: 2974 tbl 01

1. H = V_{IH}, L = V_{IL}, X = Don't Care.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2974 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2974 tbl 03

1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2974 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2974 tbl 05

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS[(1)]

(VCC = 5.0V ± 10%, VLC = 0.2V, VHC = VCC - 0.2V)

Symbol	Parameter	Power	71569S20[(3)] 71569L20[(3)]		71569S25 71569L25		71569S35[(4)] 71569L35[(4)]		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current	S	90	—	90	100	—	100	mA
	$\overline{CS}$ = VIL, Outputs Open, VCC = Max., f = 0[(2)]	L	80	—	80	90	—	90	
I_{CC2}	Dynamic Operating Current	S	180	—	170	190	—	160	mA
	$\overline{CS}$ = VIL, Outputs Open, VCC = Max., f = fMAX[(2)]	L	160	—	150	170	—	140	
I_{SB}	Standby Power Supply Current (TTL Level)	S	20	—	20	20	—	20	mA
	$\overline{CS}$ ≥ VIH, Outputs Open, VCC = Max., f = fMAX[(2)]	L	3	—	3	5	—	5	
I_{SB1}	Full Standby Power Supply Current (CMOS Level)	S	15	—	15	20	—	20	mA
	$\overline{CS}$ ≥ VHC, VCC = Max., VIN ≥ VHC or VIN ≤ VHC, f = 0[(2)]	L	0.2	—	0.2	1.0	—	1.0	

2974 tbl 06

NOTES:
1. All values are maximum guaranteed values.
2. At f = fMAX address and data inputs are cycling at the maximum frequency of read cycles of 1/tRC. f = 0 means no input lines change.
3. 0° to +70° C. temperature range only.
4. -55° to +125° C. temperature range only.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2974 tbl 07

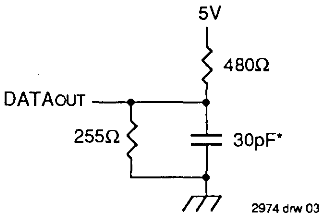


Figure 1. Output Load

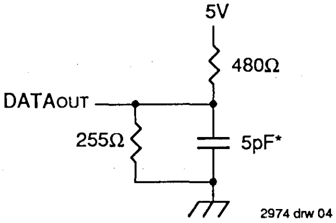


Figure 2. Output Load
(for tCLZ, tOLZ, tCHZ, tOHZ, tOW, tWHZ)

*Includes scope and jig capacitances

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

				IDT7169S		IDT7169L		
Symbol	**Parameter**	**Test Condition**		**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL COM'L	— —	10 5	— —	5 2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL COM'L	— —	10 5	— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min. I_{OL} = 10mA, V_{CC} = Min.		— —	0.4 0.5	— —	0.4 0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	2.4	—	V

2974 tbl 08

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

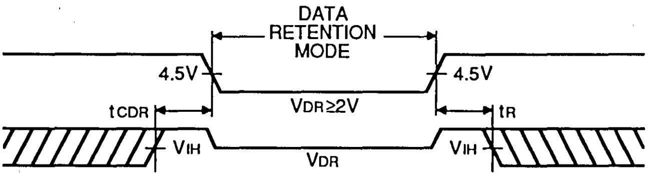
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

					Typical[1] Vcc @		Maximum Vcc @		
Symbol	**Parameter**	**Test Condition**		**Min.**	**2.0v**	**3.0V**	**2.0V**	**3.0V**	**Unit**
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current		MIL. COM'L.	— —	10 10	15 15	200 60	300 90	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time	$\overline{CS}$ ≥ V_{HC} V_{IN} ≥ V_{HC} or ≤ V_{LC}		0	—	—	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	—	—	ns
$\|I_{LI}\|$[3]	Input Leakage Current	—		—	—	—	2	2	µA

2974 tbl 09

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

LOW Vcc DATA RETENTION WAVEFORM



2974 drw 05

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

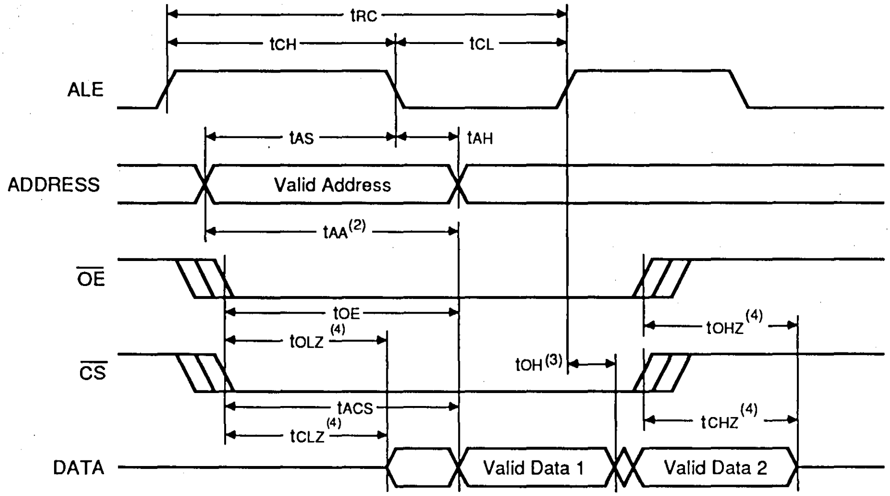
Symbol	Parameter	71569S20(1) 71569L20(1)		71569S25 71569L25		71569S35(4) 71569L35(4)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	20	—	25	—	35	—	ns
t_{AA}	Address Access Time(3)	—	19	—	25	—	35	ns
t_{ALA}	Address Latch Access Time	—	20	—	25	—	35	ns
t_{ACS}	Chip Select Access Time	—	20	—	25	—	35	ns
t_{CLZ}	Chip Select to Output in Low Z(2)	3	—	3	—	3	—	ns
t_{OE}	Output Enable to Output Valid	—	8	—	12	—	18	ns
t_{OLZ}	Output Enable to Output in Low Z(2)	3	—	3	—	3	—	ns
t_{CHZ}	ChipSelect to Output High Z(2)	—	13	—	15	—	25	ns
t_{OHZ}	Output Disable to Output in High Z(2)	—	10	—	15	—	20	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	ns
t_{CH}	ALEN High Time	10	—	10	—	10	—	ns
t_{CL}	ALEN Low Time	10	—	10	—	10	—	ns
t_{AS}	Address Set-up Time to Address Latch Enable	5	—	5	—	5	—	ns
t_{AH}	Address Hold Time to Address Latch Enable	3	—	5	—	7	—	ns
Write Cycle								
t_{WC}	Write Cycle Time	20	—	25	—	35	—	ns
t_{AW}	Address Valid to End of Write(3)	15	—	18	—	25	—	ns
t_{CW}	Chip Select to End of Write	15	—	18	—	25	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	15	—	21	—	25	—	ns
t_{WR}	Write Recovery Time(3)	0	—	0	—	0	—	ns
t_{WHZ}	Write Enable to Output in High Z(2)	—	8	—	10	—	14	ns
t_{DW}	Data Valid to End of Write	10	—	13	—	15	—	ns
t_{DH}	Data Hold Time from Write	0	—	0	—	0	—	ns
t_{OW}	Output Active from End of Write(2)	5	—	5	—	5	—	ns
t_{CH}	ALEN High Time	10	—	10	—	10	—	ns
t_{CL}	ALEN Low Time	10	—	10	—	10	—	ns
t_{AS}	Address Set-up Time to Address Latch Enable	5	—	5	—	5	—	ns
t_{AH}	Address Hold Time to Address Latch Enable	5	—	5	—	5	—	ns

NOTES:

2974 tbl 10

1. 0° to +70°C temperature range only.
2. This parameter is guaranteed, but not tested.
3. This measurement depends on the combination of ALEN high plus an address change. This combination may either happen at the rising edge of ALEN, or during an address change after ALEN has become high.
4. -55°to +125° C. temperature range only.

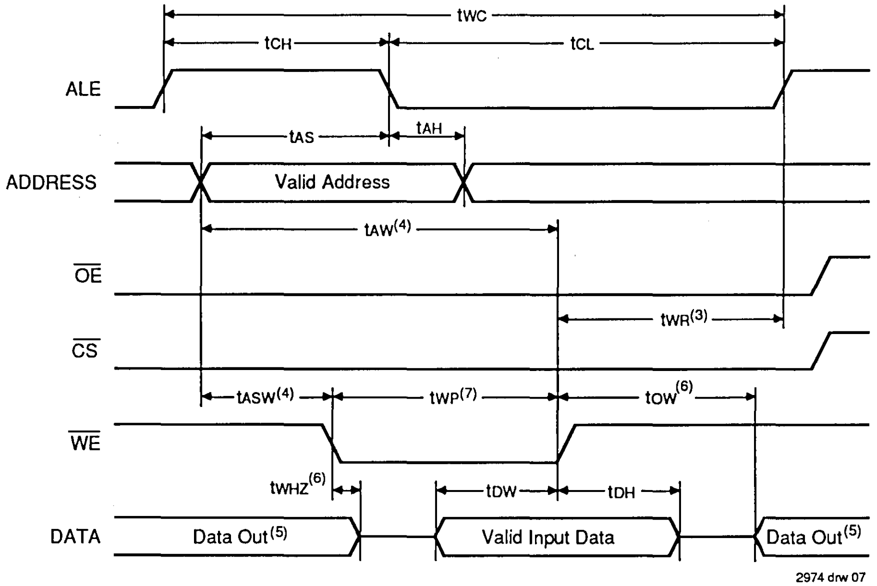
TIMING WAVEFORM OF READ CYCLE (1)



NOTES:

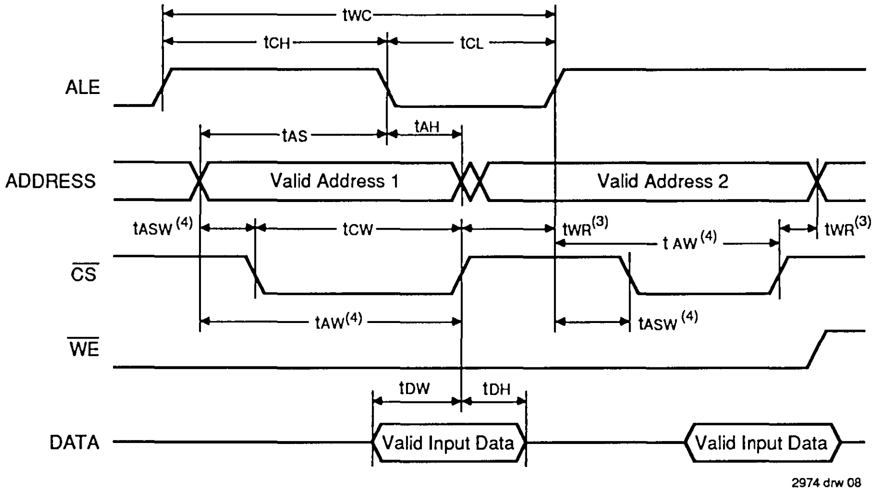
1. $\overline{WE}$ is high throughout a read cycle.
2. The parameter tAA is measured either from the first low to high transition of ALEN after the read address has become valid, or from the stabilization of the read address during the period when ALEN is high, which ever occurs last.
3. The parameter tOH is measured either from the first low to high transition of ALEN after an address change, or from an address change during the period when ALEN is high, whichever occurs first.
4. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(1,2)



5

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1,2)



NOTES:

1. $\overline{WE}$ or $\overline{CE}$ must be high during all address transitions.
2. A write occurs during the overlap (tBW, tCW or tWP) of a low $\overline{CE}$ and a low $\overline{WE}$.
3. The parameter tWR is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high either to the first low to high transition of ALEN after an address change, or to an address change during the period when ALEN is high, whichever occurs last.
4. The parameters tASW and tAW are measured either from the first low to high transition of ALEN after an address change has become valid, or from the stabilization of the valid write address during the period when ALEN is high, whichever occurs first.
5. During this period, the I/O pins are in the output state so that the input signals must not be applied.
6. This transition is measured ±200mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the spectified tWP.

ORDERING INFORMATION

IDT XXXXX X XX X X

Process/ Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B
Package	TP	Plastic DIP (300mil)
	TD	Ceramic DIP (300mil)
	Y	Small Outline IC (J-Bend) (300mil)
Speed	20	Commercial Only — Speed in Nanoseconds
	25	Speed in Nanoseconds
	35	Military Only — Speed in Nanoseconds
Power	S	Standard Power
	L	Low Power
Device Type	71569	72K (8K x 9-Bit) CMOS Static RAM with Address Latches

2974 drw 09

Integrated Device Technology, Inc.

CMOS STATIC RAM
64K (4K x 16-BIT)
LATCHED CacheRAM™

IDT71586

FEATURES:

- Wide 4K x 16 Organization
- High-speed access
  - Commercial: 25/35/45ns (max.)
  - Military: 35/45/55ns (max.)
- Internal fast 12-bit address latch (5ns set-up and hold times)
- Best fit for popular cache configurations:
  - Intel 82385 cache controller (for 80386)
  - IDT79R3000 RISC CPU instruction & data caches
  - Chips & Technologies 82C307 cache controller (for 80386)
- Fast Output Enable — 10ns (max.)
- Separate enables for upper and lower bytes
- Packaged in 40-pin, 600 mil ceramic or plastic DIP, or 44-pin PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71586 is a fast 4K x 16 latched address CeMOS static RAM designed to enhance cache memory designs. This device offers improved circuit board densities over designs using traditional RAM architectures in caches for the Intel 80386/82385, the Chips & Technologies 82C307, and the IDT79R3000 RISC CPU.

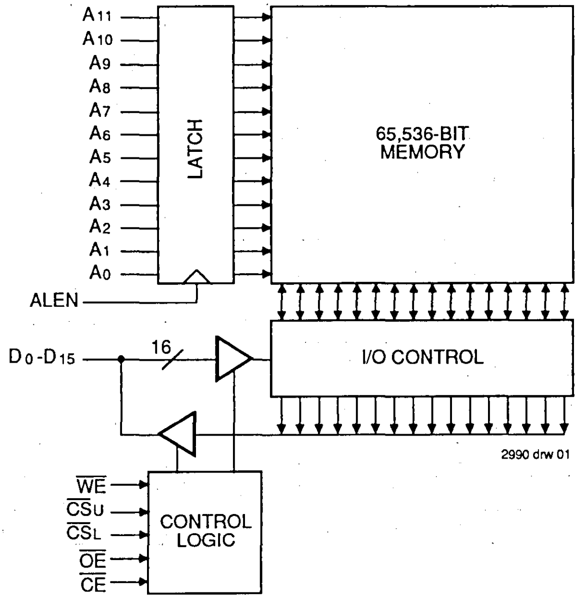
The IDT71586 boasts a fast address access time down to 24ns (max.), a very fast 10ns (max.) Output Enable pin, and short set-up and hold times (5ns max.) on the address input latch. All of these features help the IDT71586 to make the most efficient use of CPU-local buses.

Fabricated using IDT's CEMOS™ high-performance technology, the IDT71586 achieves this high throughput at a typical operating power of only 300mW.

All inputs and outputs of the IDT71586 are TTL-compatible, and the device operates from a standard 5V supply, simplifying system design. The IDT71586 is offered in a 40 pin ceramic or plastic DIP or a 44 pin plastic leadless chip carrier, providing high board level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



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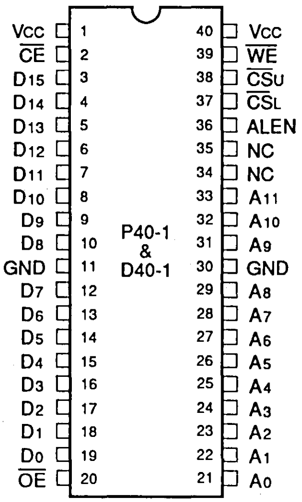
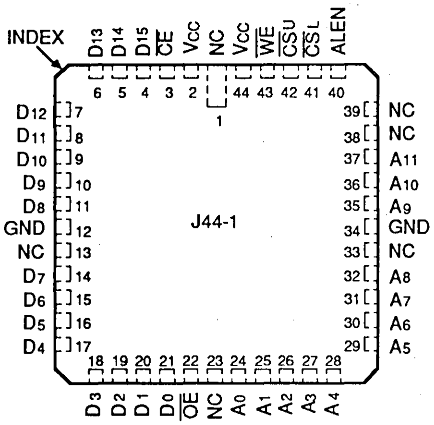
DECEMBER 1990

PIN CONFIGURATIONS



2990 drw 02

DIP
TOP VIEW



2990 drw 03

PLCC
TOP VIEW

TRUTH TABLE(1)

Inputs						Outputs		
$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{CS}}_U$	$\overline{\text{CS}}_L$	ALEN	D_8–D_{15}	D_0–D_7	Mode
H	X	X	X	X	—	Hi-Z	Hi-Z	Deselected, powered-down (I_{SB})
X	X	X	H	H	—	Hi-Z	Hi-Z	Deselected.
—	—	H	—	—	—	Hi-Z	Hi-Z	Outputs disabled
—	—	—	—	—	H	—	—	Address latch transparent
X	X	—	—	—	L	—	—	Address latch closed
L	L	X	L	H	H	DATA$_{IN}$	Hi-Z	Write to upper byte of current address
L	L	X	L	H	L	DATA$_{IN}$	Hi-Z	Write to upper byte of latched address
L	L	X	H	L	H	Hi-Z	DATA$_{IN}$	Write to lower byte of current address
L	L	X	H	L	L	Hi-Z	DATA$_{IN}$	Write to lower byte of latched address
L	L	X	L	L	H	DATA$_{IN}$	DATA$_{IN}$	Write to both bytes of current address (Word Write)
L	L	X	L	L	L	DATA$_{IN}$	DATA$_{IN}$	Write to both bytes of latched address (Word Write)
L	H	L	L	H	H	DATA$_{OUT}$	Hi-Z	Read upper byte of current address
L	H	L	L	H	L	DATA$_{OUT}$	Hi-Z	Read upper byte of latched address
L	H	L	H	L	H	Hi-Z	DATA$_{OUT}$	Read lower byte of current address
L	H	L	H	L	L	HI-Z	DATA$_{OUT}$	Read lower byte of latched address
L	H	L	L	L	H	DATA$_{OUT}$	DATA$_{OUT}$	Read both bytes of current address (Word Read)
L	H	L	L	L	L	DATA$_{OUT}$	DATA$_{OUT}$	Read both bytes of latched address (Word Read)

NOTE:

2990 tbl 01

1. H = HIGH
   L = LOW
   X = Don't Care
   — = Unrelated
   Hi-Z = High Impedance

PIN DESCRIPTIONS

A_{0-11}	Address Inputs
D_{0-15}	Data Input/Output
$\overline{CE}$	Chip Enable/Power Down
$\overline{CS}_U$	Upper Byte Select
$\overline{CS}_L$	Lower Byte Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
ALEN	Address Latch Enable
GND	Ground
V_{CC}	Power

2990 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation Plastic Hermetic	1.5 2.0	W W
I_{OUT}	DC Output Current	50	mA

NOTE: 2990 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	12	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	12	pF

NOTE: 2990 tbl 04

1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2990 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE: 2990 tbl 06

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

SPEED SELECTION

IDT79R3000 SPEED	80386 SPEED	SUGGESTED IDT71586
—	16MHZ	71586S55
12MHz	20MHz	71586S45
16MHz	25MHz	71586S35
20-25MHz	33MHz	71586S25

2990 tbl 12

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\lvert I_{LI}\rvert$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	µA
$\lvert I_{LO}\rvert$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}, V_{CC} = Max.	—	10	µA
V_{OL}	Output Low Voltage (D_0–D_{15})	I_{OL} = 6mA, V_{CC} = Min.	—	0.4	V
		I_{OL} = 8mA, V_{CC} = Min.	—	0.5	
V_{OH}	Output High Voltage	I_{OL} = -4mA, V_{CC} = Min.	2.4	—	V

2990 tbl 07

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	71586S25		71586S35		71586S45		71586S55		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Operating Power Supply Current $\overline{CE}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0(2)	130	—	130	150	130	150	—	150	mA
I_{CC2}	Dynamic Operating Current $\overline{CE}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	240	—	240	290	240	290	—	290	mA
I_{SB}	Standby Power Supply Current (TTL Level Inputs) $\overline{CE}$ ≥ V_{IH}, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	70	—	70	70	70	70	—	70	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level Inputs) $\overline{CE}$≥V_{HC}, V_{IN}≤V_{LC} or V_{IN}≥V_{HC}, V_{CC}= Max., f = 0(2)	15	—	15	20	15	20	—	20	mA

NOTES:

2990 tbl 08

1. All values are maximum guaranteed values.
2. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2990 tbl 09

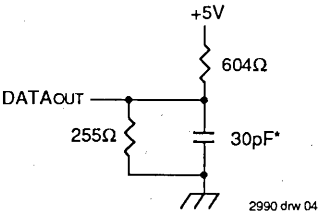


Figure 1. Output Load

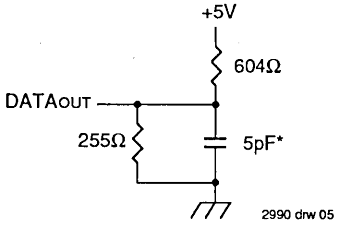


Figure 2. Output Load
(for t_{OHZ}, t_{BHZ}, t_{CHZ}, t_{OLZ}, t_{BLZ}, t_{CLZ}, t_{WHZ}, and t_{OW})

*Includes scope and jig.

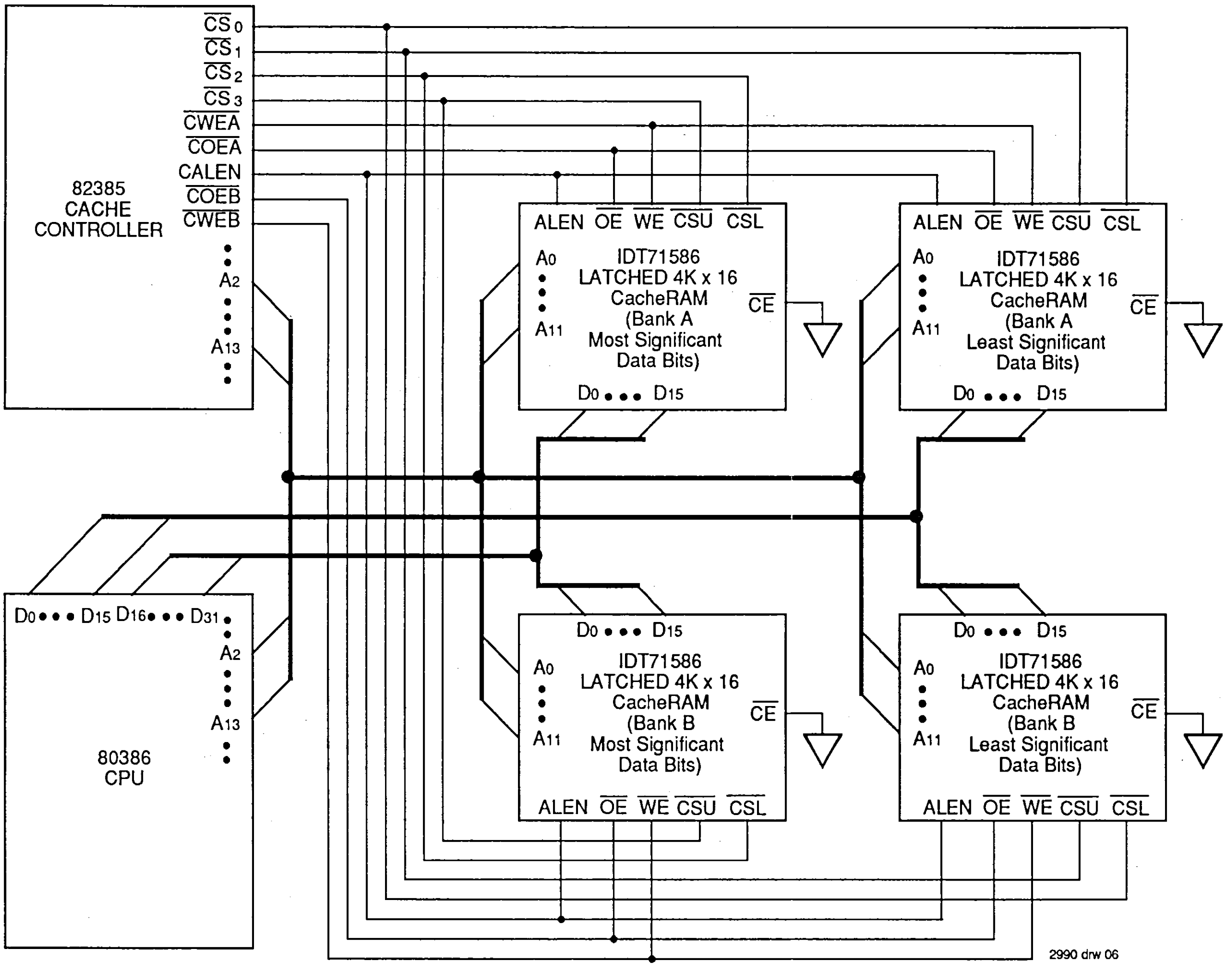


Figure 3. Example Cache for Intel 80386 using IDT71586 Latched CacheRAM and Intel 82385

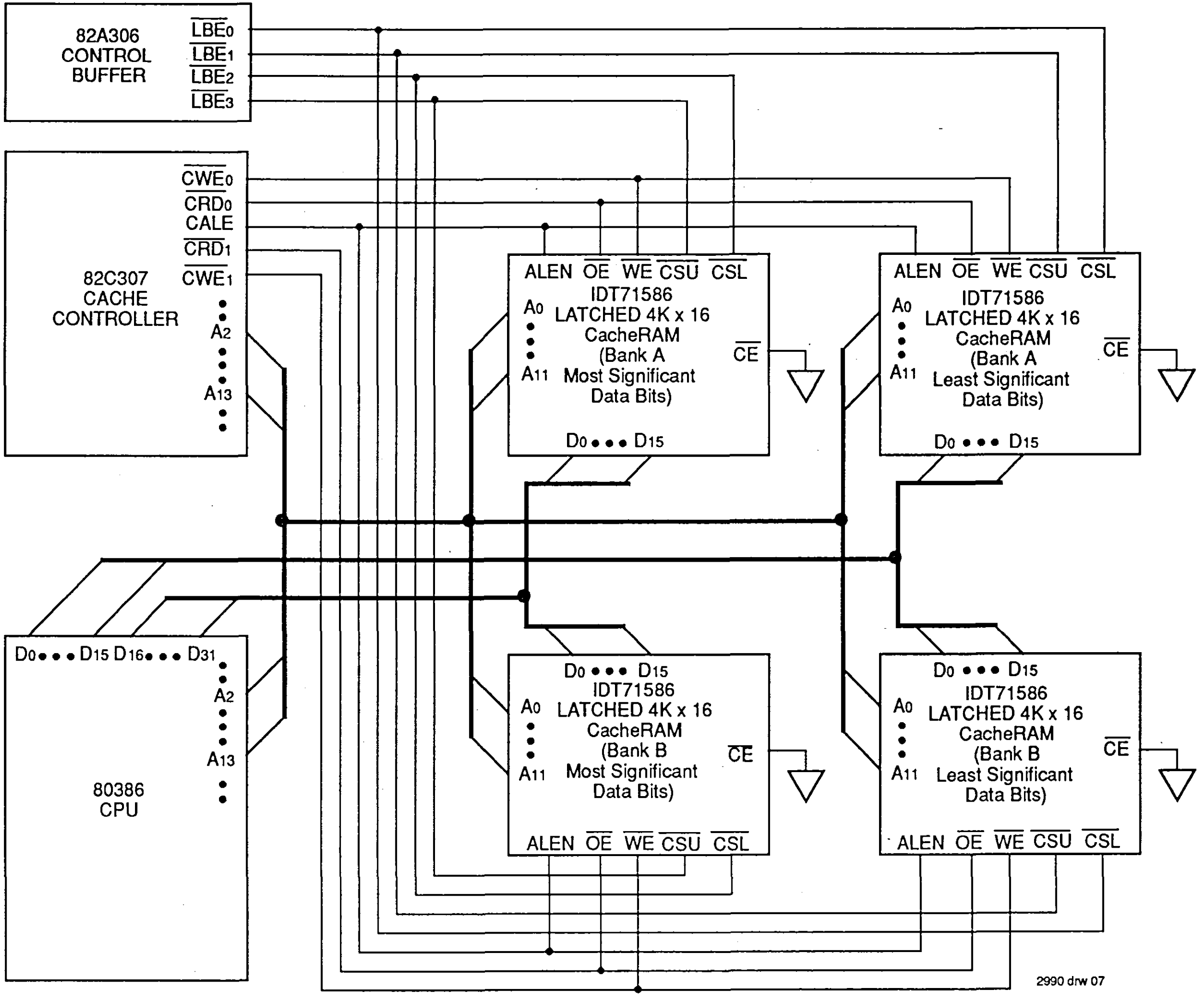


Figure 4. Example Cache for Intel 80386 using IDT71586 Latched CacheRAM and Chips & Technologies 82C307

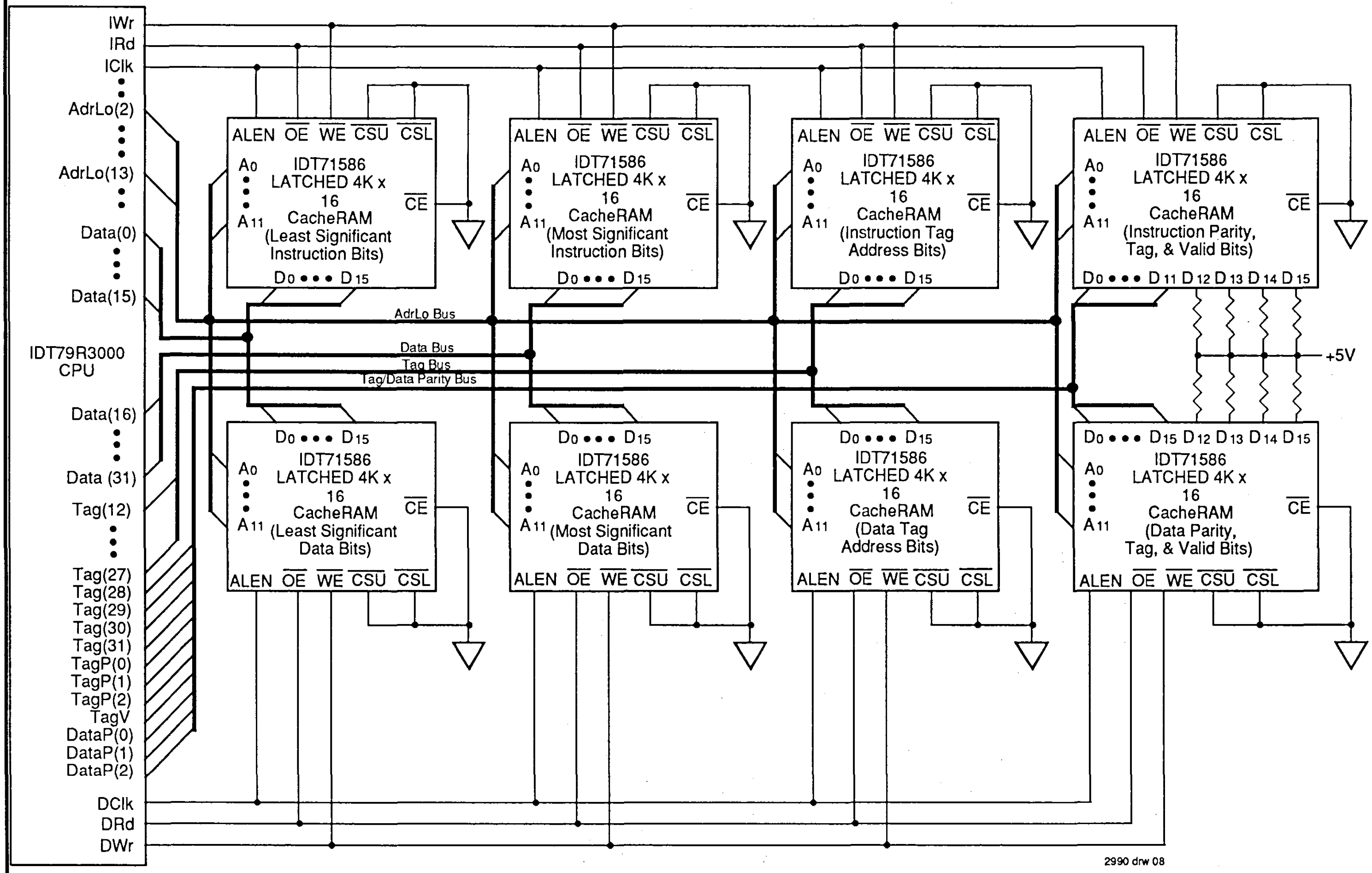


Figure 5. Example Instruction and Data Caches for IDT79R3000 using IDT71586 Latched Cache Ram

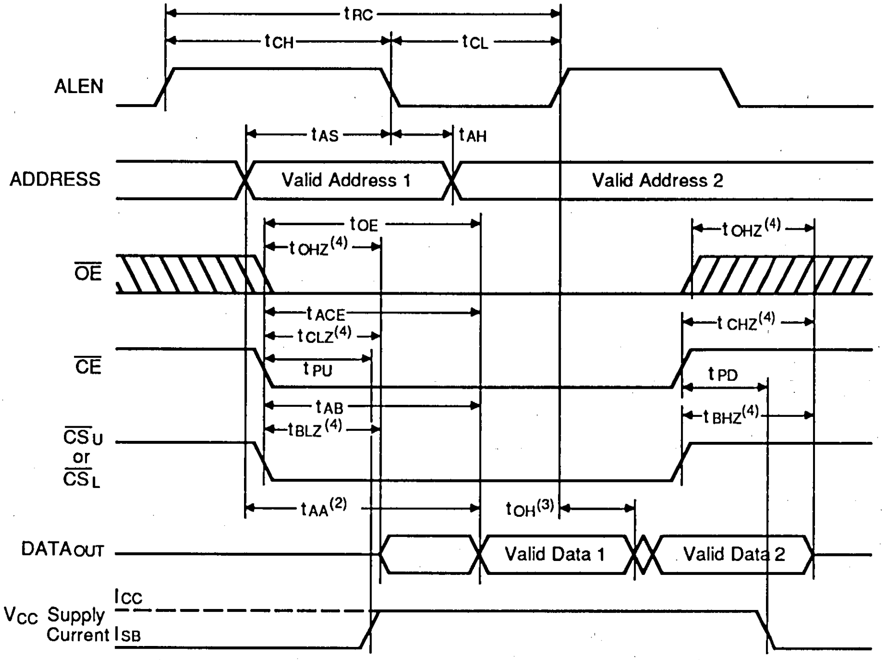
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71586S25[1]		71586S35		71586S45		71586S55[5]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
tRC	Read Cycle Time	25	—	35	—	45	—	55	—	ns
tCH	ALEN High Time[3]	10	—	10	—	12	—	15	—	ns
tCL	ALEN Low Time[3]	10	—	10	—	12	—	15	—	ns
tAS	Address Latch Set-Up Time	5	—	5	—	5	—	5	—	ns
tAH	Address Latch Hold Time	4	—	5	—	5	—	5	—	ns
tAA	Address Access Time[4]	—	24	—	35	—	45	—	55	ns
tACE	Chip Enable Access Time[4]	—	25	—	35	—	45	—	55	ns
tAB	Upper/Lower Byte Chip Select Access Time	—	13	—	15	—	20	—	25	ns
tOE	Output Enable to Output Valid	—	10	—	13	—	15	—	18	ns
tCLZ	Chip Enable to Output in Low Z[2,3]	3	—	3	—	3	—	3	—	ns
tBLZ	Upper/Lower Byte Chip Select to Output in Low Z[2,3]	3	—	3	—	3	—	3	—	ns
tOLZ	Output Enable to Output in Low Z[2,3]	2	—	2	—	2	—	2	—	ns
tCHZ	Chip Disable to Output in High Z[2,3]	—	20	—	25	—	30	—	35	ns
tBHZ	Upper/Lower Byte Chip Select to Output in High Z[2,3]	—	20	—	25	—	30	—	35	ns
tOHZ	Output Disable to Output in High Z[2,3]	—	4	—	9	—	13	—	15	ns
tOH	Output Hold from Address Change[4]	3	—	3	—	3	—	3	—	ns
tPU	Chip Select to Power Up Time[3]	0	—	0	—	0	—	0	—	ns
tPD	Chip Select to Power Down Time[3]	—	25	—	35	—	45	—	55	ns

2990 tbl 10

NOTES:
1. 0° to +70°C temperature range only.
2. Transition is measured ±200mV from low or high impedance voltage with load (Figures 1&2).
3. This parameter is guaranteed, but not tested..
4. This measurement depends on the combination of ALEN high plus an address change. This combination may either happen at the rising edge of ALEN, or during an address change after ALEN has become high.
5. -55°C to +125°C temperature range only.

TIMING WAVEFORM OF READ CYCLE(1)



2990 drw 09

NOTES:
1. $\overline{WE}$ is high throughout a read cycle.
2. The parameter tAA is measured either from the first low to high transition of ALEN after the read address has become valid, or from the stabilization of the read address during the period when ALEN is high, whichever occurs last.
3. The parameter tOH is measured either from the first low to high transition of ALEN after an address change, or from an address change during the period when ALEN is high, whichever occurs first.
4. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

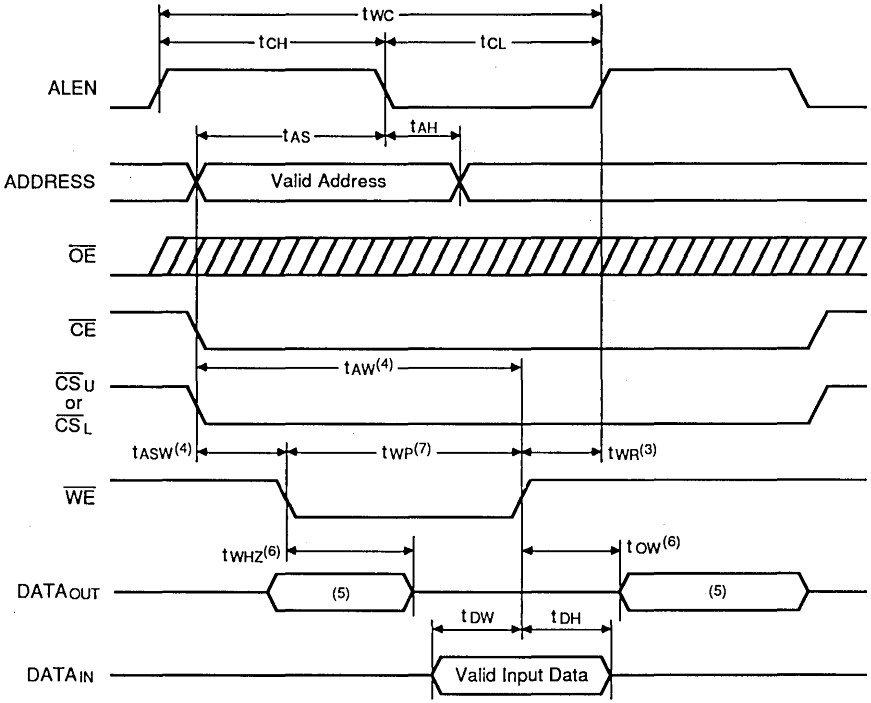
Symbol	Parameter	71586S25(1)		71586S35		71586S45		71586S55(4)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle										
tWC	Write Cycle Time	25	—	35	—	45	—	55	—	ns
tCH	ALEN High Time	10	—	10	—	12	—	15	—	ns
tCL	ALEN Low Time	10	—	10	—	12	—	15	—	ns
tAS	Address Latch Set-up Time	5	—	5	—	5	—	5	—	ns
tAH	Address Latch Hold Time	4	—	5	—	5	—	5	—	ns
tAW	Address Valid to End of Write(3)	25	—	35	—	45	—	55	—	ns
tASW	Address Set-Up Time(3)	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	17	—	25	—	30	—	40	—	ns
tCW	Chip Enable to End of Write	20	—	25	—	30	—	40	—	ns
tBW	Upper/Lower Byte Chip Select to End of Write	20	—	25	—	30	—	40	—	ns
tWR	Write Recovery Time(3)	0	—	0	—	0	—	0	—	ns
tWHZ	Write to Output in High Z(2)	—	13	—	15	—	20	—	25	ns
tDW	Data Set-Up Time	11	—	13	—	15	—	18	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
tOW	Output Active from End of Write(2)	5	—	5	—	5	—	5	—	ns

NOTES:

2990 tbl 11

1. 0° to +70°C temperature range only.
2. Transition is measured ±200mV from low or high impedance voltage with load (Figures 1&2). This parameter is guaranteed, but not tested.
3. This measurement depends on the combination of ALEN high plus an address change. This combination may either happen at the rising edge of ALEN, or during an address change after ALEN has become high.
4. -55°C to +125°C temperature range only.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)$^{(1, 2)}$

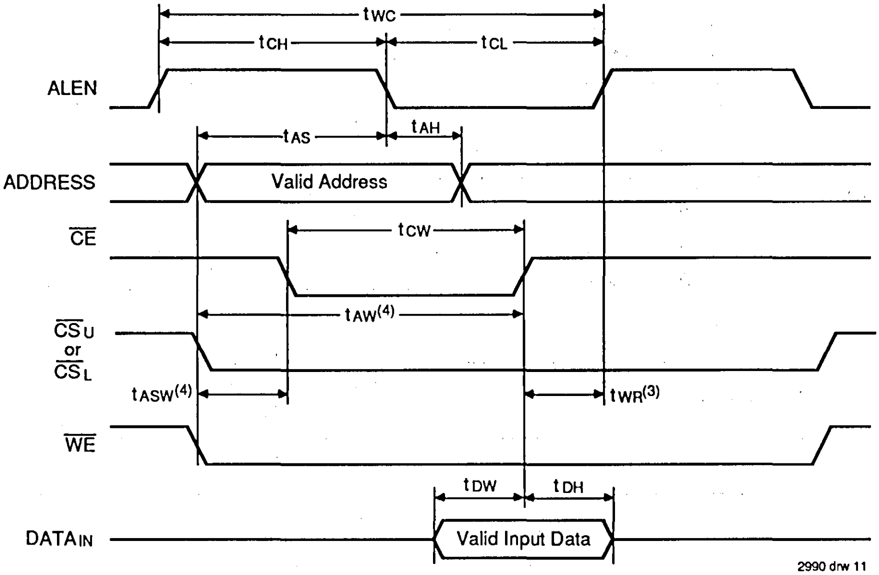


2990 drw 10

NOTES:

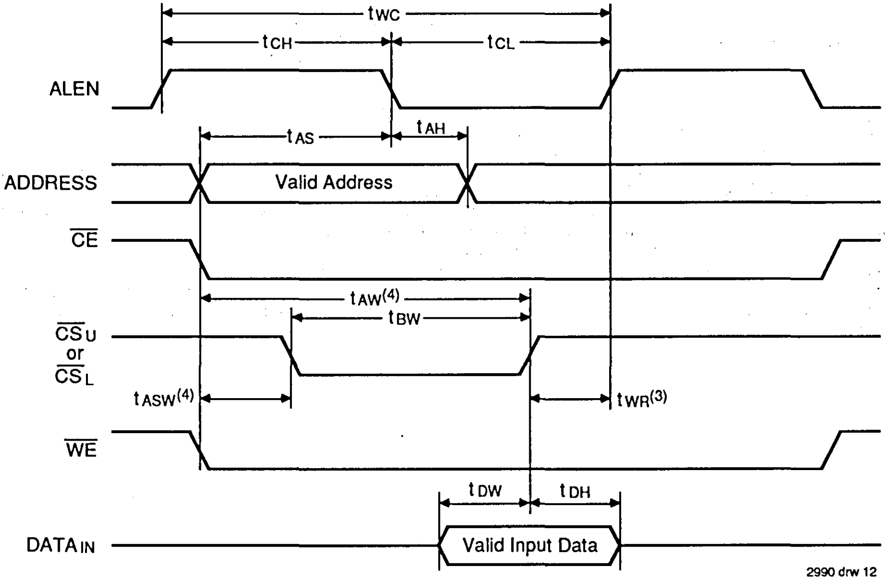
1. $\overline{WE}$, $\overline{CE}$ or both $\overline{CS}_U$ and $\overline{CS}_L$ must be inactive during all address transitions.
2. A write occurs during the overlap (t_{BW}, t_{CW} or t_{WP}) of a low $\overline{CS}_U$ or $\overline{CS}_L$, a low $\overline{CE}$ and a low $\overline{WE}$.
3. The parameter t_{WR} is measured from the earlier of $\overline{CS}_U$, $\overline{CS}_L$, $\overline{CE}$, or $\overline{WE}$ going high either to the first low to high transition of ALEN after an address change, or to an address change during the period when ALEN is high, whichever occurs first.
4. The parameters t_{ASW} and t_{AW} are measured either from the first low to high transition of ALEN after the write address has become valid, or from the stabilization of the valid write address during the period when ALEN is high, whichever occurs first.
5. During this period, I/O pins are in the output state, and xinput signals must not be applied.
6. This transition is measured ±200mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} +t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the spectified t_{WP}.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED TIMING)(1, 2)



2990 drw 11

TIMING WAVEFORM OF WRITE CYCLE NO.3 ($\overline{CS}$U or $\overline{CS}$L CONTROLLED TIMING)(1, 2)

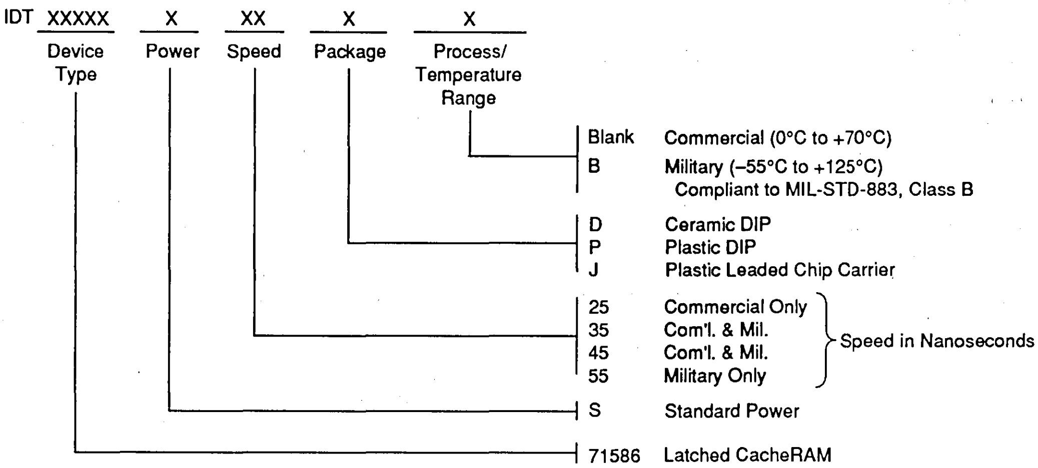


2990 drw 12

NOTES:

1. $\overline{WE}$, $\overline{CE}$ or both $\overline{CS}$U and $\overline{CS}$L must be high during all address transitions.
2. A write occurs during the overlap (tBW, tCW or tWP) of a low $\overline{CS}$U or $\overline{CS}$L, a low $\overline{CE}$ and a low $\overline{WE}$.
3. The parameter tWR is measured from the earlier of $\overline{CS}$U, $\overline{CS}$L, $\overline{CE}$, or $\overline{WE}$ going high either to the first low to high transition of ALEN after an address change, or to an address change during the period when ALEN is high, whichever occurs first.
4. The parameters tASW and tAW are measured either from the first low to high transition of ALEN after the write address has become valid, or from the stabilization of the valid write address during the period when ALEN is high, whichever occurs first.

ORDERING INFORMATION



2990 drw 13

Integrated Device Technology, Inc.

CMOS CacheRAM™ 32K X 9-BIT (288K-BIT) BURST COUNTER & SELF-TIMED WRITE

ADVANCE INFORMATION
IDT71589

FEATURES:

- High density 32K x 9 architecture
- Internal write registers (address, data, and control)
- Self-timed write cycle
- Internal burst read and write address counter
  Clock to data times: 15, 20, 25, 35ns
- Chip select for depth expansion
- Matches all timing and signals of Intel™ 486™ processor
- Packaged in plastic or hermetic 300 mil 32-pin DIP, and plastic 300 mil 32-pin SOJ
- Military product 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT71589 is an extremely high-speed 32K x 9-bit static RAM with full on-chip hardware support of the Intel i486 CPU interface. This part is designed to facilitate the implementation of the highest-performance secondary caches for the i486 architecture while using low-speed cache-tag RAMs and PALs and consuming the minimum possible board space.

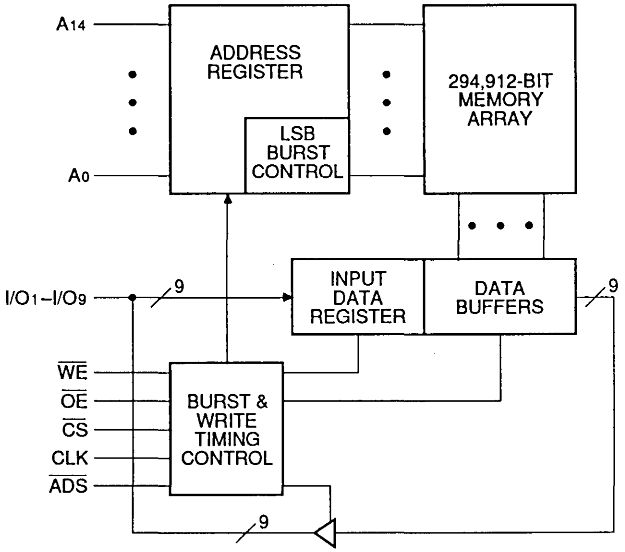
The IDT71589 CacheRAM contains a full set of write data and address registers. Internal logic allows the processor to generate a self-timed write based upon a decision which can be left until the extreme end of the write cycle.

An internal burst address counter accepts the first cycle address from the processor, then cycles through the adjacent four locations using the i486's burst refill sequence on appropriate rising edges of the system clock.

Fabricated using IDT's CEMOS™ high-performance technology, this device operates at a very low power consumption and offers a maximum clock to data access time as fast as 15ns.

The IDT71589 CacheRAMs are packaged in a 32-pin plastic or hermetic DIP, or a plastic J-bend small-outline (SOJ) package. Military grade devices are available 100% processed in compliance to the test methods of MIL-STD-883, Class B, Method 5004.

FUNCTIONAL BLOCK DIAGRAM



2951 drw 01

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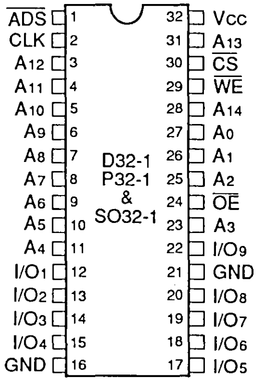
Intel and i486 are trademarks of Intel Corp.

PIN CONFIGURATION



2951 drw 02

DIP/SOJ
TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–65 to +135	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation Plastic Hermetic	 1.5 2.0	W
I_{OUT}	DC Output Current	50	mA

2951 tbl 03

NOTE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

PIN NAMES

A_0–A_{14}	Address Inputs
I/O_1–I/O_9	Data Input/Output
$\overline{CS}$	Chip Select/Count Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{ADS}$	Address Status
CLK	System Clock
GND	Ground
Vcc	Power

2951 tbl 01

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2951 tbl 04

SPEED SELECTION

i486 Speed	Suggested IDT71589
25MHz	IDT71589S35
33MHz	IDT71589S25
40MHz	IDT71589S20
50MHz	IDT71589S15

2951 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0.0	V
V_{IH}	Input High Votage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

2951 tbl 05

NOTE:
1. V_{IL} = –3.0V for pulse width less than 5ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}, V_{CC} = Max.	—	10	µA
V_{OL}	Output Low Voltage (I/O1–I/O9)	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

2951 tbl 06

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1) (V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

			71589S15(3)		71589S20		71589S25		71589S35		
Symbol	Parameter	Test Condition	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Unit
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL} Outputs Open V_{CC} = Max., f = 0(2)	TBD	—	130	—	130	TBD	130	TBD	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS}$ = V_{IL} Outputs Open V_{CC} = Max., f = f_{MAX}(2)	TBD	—	240	—	220	TBD	200	TBD	mA

NOTES:

2951 tbl 07

1. All values are maximum guaranteed values.
2. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.
3. Preliminary information only.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2951 Tbl 08

CAPACITANCE

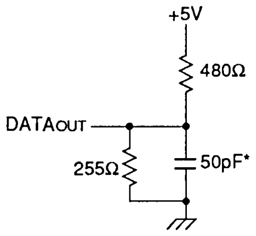
(T_A = +25°C, f = 1.0 MHz, SOJ package only)

Symbol	Parameter(1)	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
$C_{I/O}$	Input/Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:

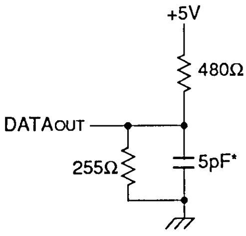
2951 tbl 09

1. This parameter is determined by device characterization but is not production tested.



2951 drw 03

Figure 1. Output Load



2951 drw 04

Figure 1. Output Load
(for t_{OHZ}, t_{CHZ}, t_{OLZ} and t_{CLZ})

*including scope and jig

FUNCTIONAL DESCRIPTION

The IDT71589 is an extremely fast 32K x 9 CMOS static CacheRAM with internal edge-triggered registers dedicated to the support of the Intel i486 CPU. These registers support the fastest systems and allow a 128KByte or larger cache to be designed to consume the smallest number of chips, the lowest power and board space, and allow the designer to avoid the use of expensive high-speed cache-tag RAMs and PALs.

The internal registers are designed to support two high speed functions: Burst read cycles, and a late-abort self-timed write cycle.

Burst read cycles are accomplished through the assertion of the $\overline{\text{ADS}}$ signal with a valid address input during the rising edge of the clock input. This address will be used to access the data in the CacheRAM during the next clock cycle, and data will be output during the following three cycles in accordance with the i486's burst refill sequence (i.e., during the next cycle the address' LSB is inverted, then the second LSB is inverted as the LSB is restored to its original value, etc.). Since the CacheRAM contains this counter internally, the critical clock-to-data time of even the fastest CPU speeds can be met by using a slower RAM speed grade without resorting to chip-intensive interleaving schemes. Should the $\overline{\text{ADS}}$ signal be sampled as valid after having been sampled as invalid, any bursting in process will be reinitialized to the new address, and a new burst cycle will be started. The burst counter wraps around at the end of the sequence and continues to count until stopped by the $\overline{\text{ADS}}$ or $\overline{\text{CS}}$ inputs. A fast copy-back scheme can harness this capability by reading, then writing the four burst addresses within a single burst cycle.

The self-timed write cycle significantly eases the timing of the address and data inputs during a write cycle, and allows the write/don't write decision to be postponed until the very end of the second cycle of a write cycle. During a write cycle, the address will be strobed into the address register during the first rising edge of the clock after the $\overline{\text{ADS}}$ input becomes valid. Data is sampled into the data input register during the next cycle's rising edge, as is the write enable input. If a write has been enabled the data will be written from the address and input data registers into the CacheRAM during the second (low) phase of the clock of that cycle.

A chip select pin is provided to give control over interruption of write cycles and burst read cycles. When the $\overline{\text{CS}}$ input is used to interrupt a burst cycle, it operates as a synchronous input to the burst counter. A low level must be present on the chip select input and must satisfy data set-up and hold times in order for the counter to progress to its next state. To stop the counter at its current state, the chip select input must be taken high, and must stay high long enough to satisfy the CacheRAM's data set-up and hold times. The $\overline{\text{CS}}$ pin also is used as an auxiliary to the $\overline{\text{WE}}$ input. Writes can only be accomplished if both $\overline{\text{CS}}$ and $\overline{\text{WE}}$ are simultaneously sampled active.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

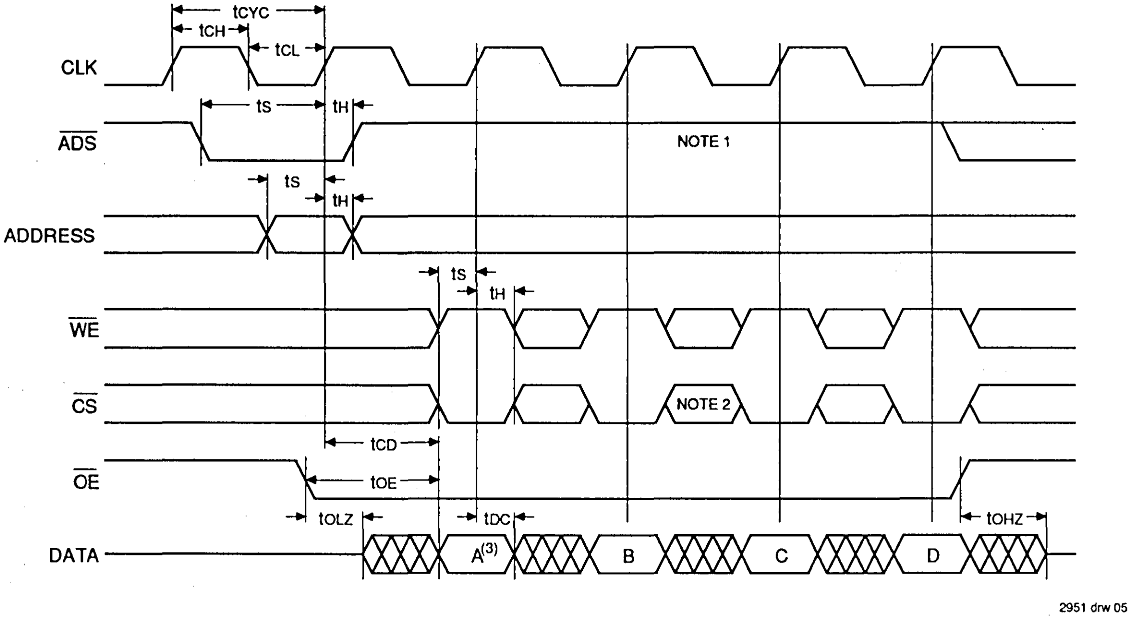
		71589S15(4)		71589S20(1)		71589S25		71589S35		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{CYC}	Clock Cycle Time	20	—	25	—	30	—	40	—	ns
t_{CH}	Clock Pulse High	8	—	10	—	11	—	14	—	ns
t_{CL}	Clock Pulse Low	8	—	10	—	11	—	14	—	ns
t_S	Set-up Time ($\overline{\text{ADS}}$, $\overline{\text{WE}}$, $\overline{\text{CS}}$, Address, Input Data)	3	—	3	—	4	—	5	—	ns
t_H	Hold Time ($\overline{\text{ADS}}$, $\overline{\text{WE}}$, $\overline{\text{CS}}$, Address, Input Data)	1	—	1	—	1	—	1	—	ns
t_{CD}	Clock to Data Valid	—	14	—	19	—	24	—	34	ns
t_{DC}	Data Valid After Clock	3	—	4	—	4	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	7	—	8	—	9	—	10	ns
t_{OLZ}	Output Enable to Output in Lo-Z(2,3)	2	—	2	—	2	—	2	—	ns
t_{OHZ}	Output Disable to Output in Hi-Z(2,3)	—	7	—	8	—	9	—	10	ns

NOTES:

2951 tbl 10

1. 0°C to +70°C Temperature range only.
2. Transition is measured ±200mV from low or high impedence voltage with load (Figure 2).
3. This parameter is guaranteed, but not tested.
4. Preliminary information only.

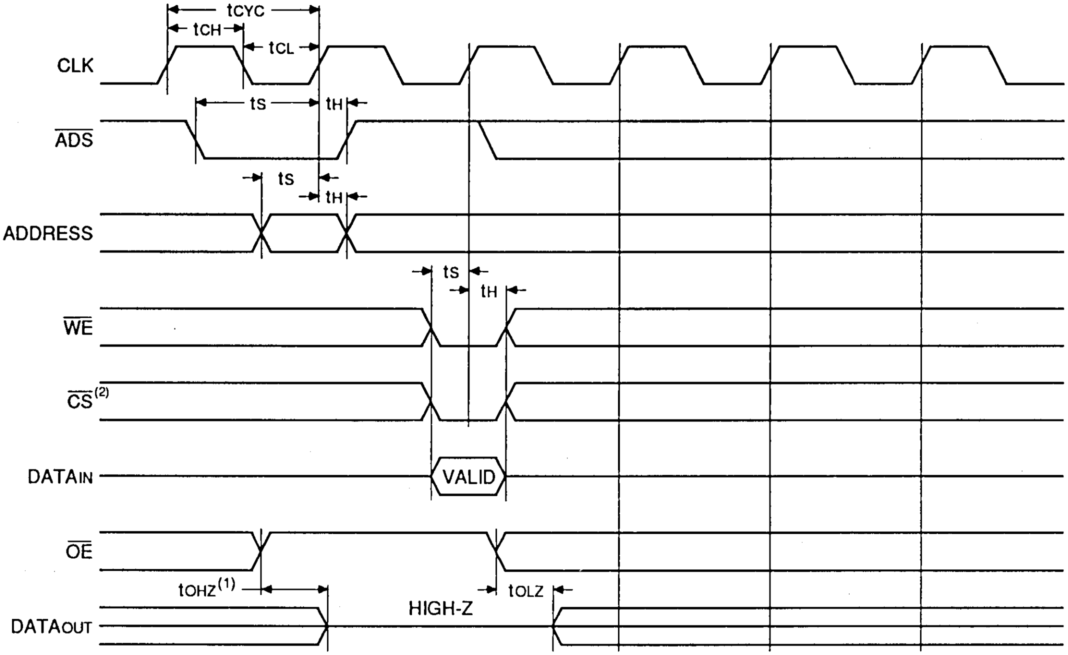
TIMING WAVEFORM OF BURST READ CYCLE



NOTES:

1. If $\overline{\text{ADS}}$ goes low during a burst cycle, a new address will be loaded and another burst cycle will be started.
2. If $\overline{\text{CS}}$ is taken inactive during a burst read cycle, the burst counter will discontinue counting until $\overline{\text{CS}}$ input again goes active. The timing of the $\overline{\text{CS}}$ input for this control of the burst counter must satisfy setup and hold parameters tS and tH.
3. A-Data from input address
   B-Data from input address except A_0 is now $\overline{A_0}$
   C-Data from input address except A_1 is now $\overline{A_1}$
   D-Data from input address except A_0 and A_1 are now $\overline{A_0}$ and $\overline{A_1}$

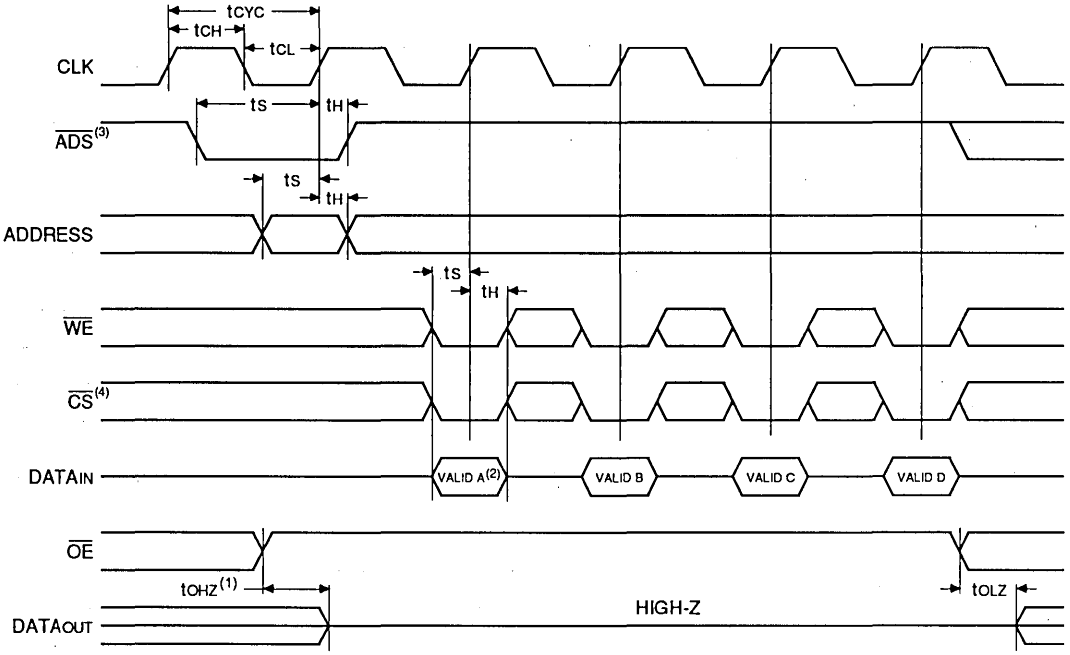
TIMING WAVEFORM OF WRITE CYCLE



2951 drw 06

NOTES:
1. OE Must be taken inactive at least as long as t_{OHZ} + t_S before the second rising clock edge of write cycle.
2. CS timing is the same as any synchronous signal when used to block writes or to stop the burst count sequence.

TIMING WAVEFORM OF BURST WRITE CYCLE



2951 drw 07

NOTES:
1. OE Must be taken inactive at least as long as t_{OHZ} + t_S before the second rising clock edge of write cycle.
2. A-Data to be written to original input address.
   B-Data to be written to original input address except A_0 is now $\overline{A_0}$.
   C-Data to be written to original input address except A_1 is now $\overline{A_1}$.
   D-Data to be written to original input address except A_0 and A_1 are now $\overline{A_0}$ and $\overline{A_1}$
3. If ADS goes low during a burst cycle, a new address will be loaded, and another burst cycle will be started.
4. If CS is taken inactive during a burst write cycle the burst counter will discontinue counting until the CS input again goes active. The timing of the CS input for this control of the burst counter must satisfy setup and hold parameters t_S and t_H. CS timing is the same as any synchronous signal when used to block writes or to stop the burst count sequence.

TRUTH TABLE

CLK	Previous $\overline{ADS}$	$\overline{ADS}$	Address	$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	I/O	Function
↑	H	L	Valid Input	X	X	—	—	Preset Address Counter
↑	X	H	—	—	—	—	—	Ignore External Address Pins
↑	L	X	—	—	—	—	—	Ignore External Address Pins
↑	X	H	—	—	L	—	—	Sequence Address Counter
↑	L	X	—	—	L	—	—	Sequence Address Counter
↑	X	H	—	—	H	—	—	Suspend Address Sequencing
↑	L	X	—	—	H	—	—	Suspend Address Sequencing
—	—	—	—	—	—	H	Hi-Z	Outputs Disabled
—	—	—	—	H	—	L	DATAOUT	Read
↑	X	H	—	L	L	H	DATAIN	Write
↑	L	X	—	L	L	H	DATAIN	Write
—	—	—	—	L	L	L	—	Not Allowed

NOTE:
H = HIGH
L = LOW
X = Don't Care
– = Unrelated
Hi-Z = High Impedance

2951 tbl 11

5

ORDERING INFORMATION

IDT XXXXX A 999 A A

XXXXX = Device Type
A = Power
999 = Speed
A = Package
A = Process/Temperature Range

Process/Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Method 5004, Class B
Package	D	CERDIP
	P	Plastic DIP
	Y	Plastic J-Bend Small Outline IC
Speed	15	Commercial Only — Speed in Nanoseconds
	20	Commercial Only — Speed in Nanoseconds
	25	Speed in Nanoseconds
	35	Speed in Nanoseconds
Power	S	Standard Power
Device Type	71589	Latched Cache RAM

2951 drw 08

Integrated Device Technology, Inc.

CMOS STATIC RAMS
64K (8K x 8-BIT)

IDT7164S
IDT7164L

FEATURES:

- Optimized for fast RISC processors including the IDT79R3000
- High-speed address/chip select access time
  - — Military: 20/25/30/35/45/55/70/85/100/120/150/200ns (max.)
  - — Commercial: 15/20/25/30/35ns (max.)
- Low power consumption
- Battery backup operation — 2V data retention voltage (L Version only)
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Available in:
  - — 28-pin 300 mil Plastic and Ceramic DIP
  - — 28-pin 600 mil Plastic and Ceramic DIP
  - — 28-pin 330 mil SOIC
  - — 28-pin 300 mil SOJ
  - — 28-pin LCC
  - — 32-pin LCC
  - — 32-pin PLCC
  - — 28-pin CERPACK
- Pin-compatible with standard 64K static RAM and EPROM
- Military product available compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-85525 is listed on this function

DESCRIPTION:

The IDT7164 is a 65,536 bit high-speed static RAM organized as 8K x 8. It is fabricated using IDT's high-performance, high-reliability CEMOS technology. Timing parameters have been specified to meet the demands of the fastest IDT79R3000 RISC processors.

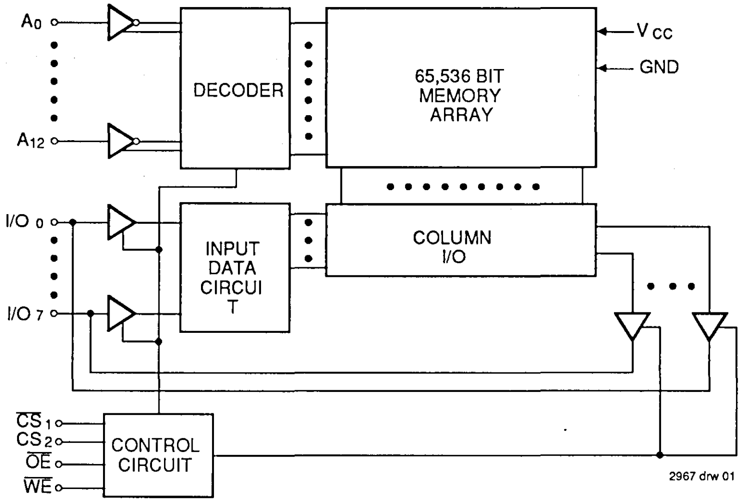
Address access times as fast as 15ns are available with typical power consumption of only 250mW. The circuit also offers a reduced power standby mode. When $\overline{CS}_1$ goes high or CS_2 goes low, the circuit will automatically go to, and remain in, a low-power stand by mode. In the full standby mode, the low-power device typically consumes less than 30µW. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 10µW operating off a 2V battery.

All inputs and outputs of the IDT7164 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT7164 is packaged in a 28-pin 300 mil DIP and SOJ; 28-pin 330 mil SOIC; 28-pin 600 mil DIP; 32-pin PLCC and LCC; and 28-pin LCC, providing high-level board packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

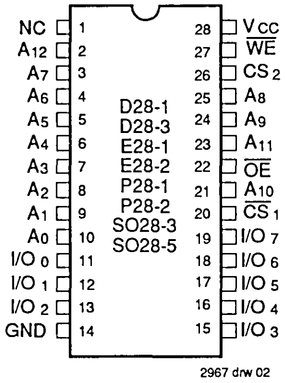
FUNCTIONAL BLOCK DIAGRAM



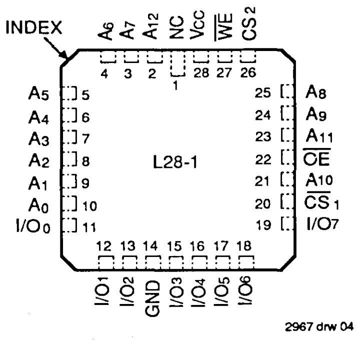
CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1990**

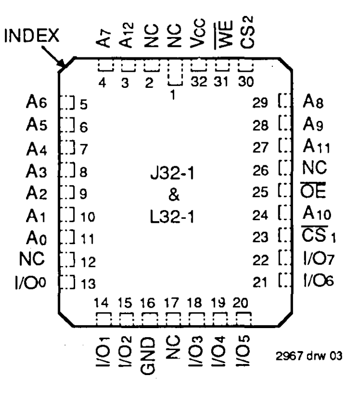
PIN CONFIGURATIONS



DIP/SOIC/SOJ
TOP VIEW



28-PIN LCC
TOP VIEW



32-PIN LCC/PLCC
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A0–A12	Address
I/O0–I/O7	Data Input/Output
$\overline{CS}_1$	Chip Select
CS2	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
Vcc	Power

2967 tbl 01

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2967 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE[1,2]

$\overline{WE}$	$\overline{CS}_1$	CS2	$\overline{OE}$	I/O	Function
X	H	X	X	High-Z	Standby (I_{SB})
X	X	L	X	High-Z	Standby (I_{SB})
X	V_{HC}	V_{HC} or V_{LC}	X	High-Z	Standby (I_{SB1})
X	X	V_{LC}	X	High-Z	Standby (I_{SB1})
H	L	H	H	High-Z	Output Disable
H	L	H	L	DOUT	Read
L	L	H	X	DIN	Write

NOTE: 2967 tbl 02

1. CS2 will power-down $\overline{CS}_1$, but $\overline{CS}_1$ will not power-down CS2.
2. H = V_{IH}, L = V_{IL}, X = don't care.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2967 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2967 tbl 06

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:

2967 tbl 04

1. This parameter is determined by device characterization, but is not production tested.

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	7164S15 7164L15		7164S20(4) 7164L20(4)		7164S25(4) 7164L25(4)		7164S30 7164L30		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current, $\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$, Outputs Open, V_{CC} = Max., f = 0(3)	S	110	—	100	110	90	110	90	100	mA
		L	100	—	90	100	80	100	80	90	
I_{CC2}	Dynamic Operating Current $\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(3)	S	180	—	170	180	170	180	160	170	mA
		L	150	—	150	160	150	160	140	150	
I_{SB}	Standby Power Supply Current (TTL Level), $\overline{CS}_1 \geq V_{IH}$, $CS_2 \leq V_{IL}$ V_{CC} = Max., Outputs Open, f = f_{MAX}(3)	S	20	—	20	20	20	20	20	20	mA
		L	3	—	3	5	3	5	3	5	
I_{SB1}	Full Standby Power Supply Current (CMOS Level), f = 0(3) 1. $\overline{CS}_1 \geq V_{HC}$ and $CS_2 \geq V_{HC}$ 2. $CS_2 \leq V_{LC}$, V_{CC} = Max.	S	15	—	15	20	15	20	15	20	mA
		L	0.2	—	0.2	1	0.2	1	0.2	1	

DC ELECTRICAL CHARACTERISTICS(1) (Continued)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	7164S35 7164L35		7164S45 7164L45		7164S55 7164L55		7164S70/85(2) 7164L70/85(2)		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current, $\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$, Outputs Open, V_{CC} = Max., f = 0(3)	S	90	100	—	100	—	100	—	100	mA
		L	80	90	—	90	—	90	—	90	
I_{CC2}	Dynamic Operating Current $\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(3)	S	150	160	—	160	—	160	—	160	mA
		L	130	140	—	130	—	125	—	120	
I_{SB}	Standby Power Supply Current (TTL Level), $\overline{CS}_1 \geq V_{IH}$, $CS_2 \leq V_{IL}$ V_{CC} = Max., Outputs Open, f = f_{MAX}(3)	S	20	20	—	20	—	20	—	20	mA
		L	3	5	—	3	—	5	—	5	
I_{SB1}	Full Standby Power Supply Current (CMOS Level), f = 0(3) 1. $\overline{CS}_1 \geq V_{HC}$ and $CS_2 \geq V_{HC}$ 2. $CS_2 \leq V_{LC}$, V_{CC} = Max.	S	15	20	—	15	—	20	—	20	mA
		L	0.2	1	—	0.2	—	1	—	1	

NOTES:

2967 tbl 07

1. All values are maximum guaranteed values.
2. Also available: 100, 120, 150 and 200ns military devices.
3. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.
4. Military values for 20 and 25ns device are preliminary only.

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Condition		IDT7164S		IDT7164L		Unit
				Min.	Max.	Min.	Max.	
$\lvert I_{LI}\rvert$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL. COM'L.	— —	10 5	— —	5 2	µA
$\lvert I_{LO}\rvert$	Output Leakage Current	V_{CC} = Max., $\overline{CS}_1 = V_{IH}$, V_{OUT} = GND to V_{CC}	MIL. COM'L.	— —	10 5	— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.			0.4	—	0.4	V
		I_{OL} = 10mA, V_{CC} = Min.		—	0.5	—	0.5	
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	2.4	—	V

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) $V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$

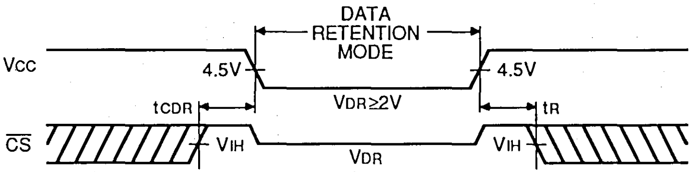
Symbol	Parameter	Test Condition		Min.	Typ.[1] Vcc @		Max. Vcc @		Unit
					2.0v	3.0V	2.0V	3.0V	
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	1. $\overline{CS}_1 \geq V_{HC}$, $CS_2 \geq V_{HC}$ 2. $CS_2 \leq V_{LC}$	MIL. COM'L.	— —	10 10	15 15	200 60	300 90	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	—	—	ns
$\lvert I_{LI}\rvert$[3]	Input Leakage Current			—	—	—	2	2	µA

2967 tbl 10

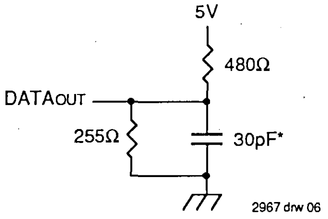
NOTES:

1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

LOW Vcc DATA RETENTION WAVEFORM

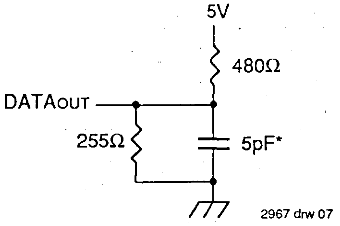


2967 drw 05



2967 drw 06

Figure 1. Output Load



2967 drw 07

Figure 2. Output Load
(for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

*Includes scope and jig capacitances

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2967 tbl 08

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7164S15$^{(1)}$ 7164L15$^{(1)}$		7164S20$^{(5)}$ 7164L20$^{(5)}$		7164S25$^{(5)}$ 7164L25$^{(5)}$		7164S30 7164L30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	15	—	20	—	25	—	30	—	ns
t_{AA}	Address Access Time	—	15	—	19	—	25	—	29	ns
t_{ACS1}	Chip Select-1 Access Time$^{(3)}$	—	15	—	20	—	25	—	30	ns
t_{ACS2}	Chip Select-2 Access Time$^{(3)}$	—	20	—	25	—	30	—	35	ns
$t_{CLZ1,2}$	Chip Select-1, 2 to Output in Low Z$^{(4)}$	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	7	—	8	—	12	—	15	ns
t_{OLZ}	Output Enable to Output in Low Z$^{(4)}$	3	—	3	—	3	—	3	—	ns
$t_{CHZ1,2}$	Chip Select-1, 2 to Output in High Z$^{(4)}$	—	8	—	9	—	13	—	13	ns
t_{OHZ}	Output Disable to Output in High Z$^{(4)}$	—	7	—	8	—	10	—	12	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{PU}	Chip Select to Power Up Time$^{(4)}$	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Select to Power Down Time$^{(4)}$	—	15	—	20	—	25	—	30	ns
Write Cycle										
t_{WC}	Write Cycle Time	15	—	20	—	25	—	30	—	ns
$t_{CW1,2}$	Chip Select to End of Write	14	—	15	—	18	—	22	—	ns
t_{AW}	Address Valid to End of Write	14	—	15	—	18	—	22	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	14	—	15	—	21	—	23	—	ns
t_{WR1}	Write Recovery Time ($\overline{CS}_1$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
t_{WR2}	Write Recovery Time (CS$_2$)	5	—	5	—	5	—	5	—	ns
t_{WHZ}	Write Enable to Output in High Z$^{(4)}$	—	6	—	8	—	10	—	12	ns
t_{DW}	Data to Write Time Overlap	8	—	10	—	13	—	13	—	ns
t_{DH1}	Data Hold from Write Time ($\overline{CS}_1$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
t_{DH2}	Data Hold from Write Time (CS$_2$)	5	—	5	—	5	—	5	—	ns
t_{OW}	Output Active from End of Write$^{(4)}$	5	—	5	—	5	—	5	—	ns

2967 tbl 11

NOTES:

1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only. Also available: 100, 120, 150 and 200ns military devices.
3. Both chip selects must be active for the device to be selected.
4. This parameter is guaranteed, but not tested.
5. Military values for 20 and 25ns devices are preliminary only.

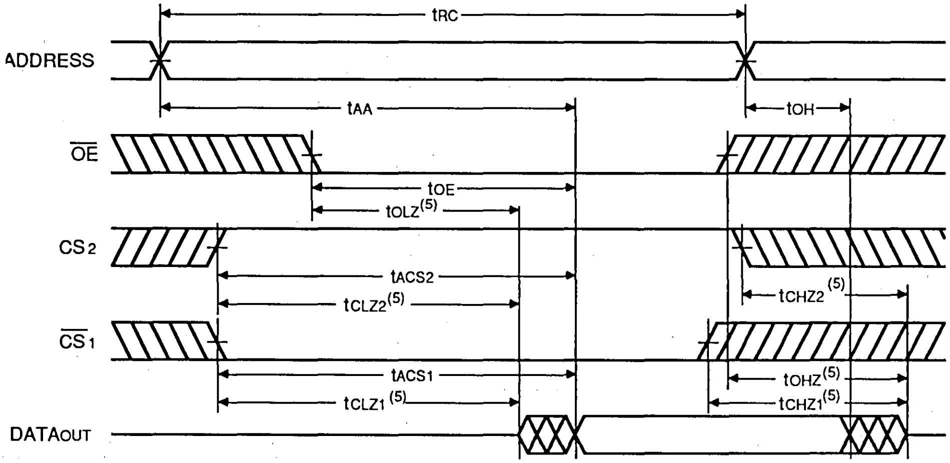
AC ELECTRICAL CHARACTERISTICS (Continued) (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7164S35 7164L35		7164S45(2) 7164L45(2)		7164S55(2) 7164L55(2)		7164S70(2)/85(2) 7164L70(2)/85(2)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	35	—	45	—	55	—	70/85	—	ns
t_{AA}	Address Access Time	—	35	—	45	—	55	—	70/85	ns
t_{ACS1}	Chip Select-1 Access Time(3)	—	35	—	45	—	55	—	70/85	ns
t_{ACS2}	Chip Select-2 Access Time(3)	—	40	—	45	—	55	—	70/85	ns
$t_{CLZ1,2}$	Chip Select-1, 2 to Output in Low Z(4)	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	18	—	25	—	30	—	35/40	ns
t_{OLZ}	Output Enable to Output in Low Z(4)	3	—	3	—	3	—	3	—	ns
$t_{CHZ1,2}$	Chip Select-1, 2 to Output in High Z(4)	—	15	—	20	—	25	—	30/35	ns
t_{OHZ}	Output Disable to Output in High Z(4)	—	15	—	20	—	25	—	30/35	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{PU}	Chip Select to Power Up Time(4)	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Select to Power Down Time(4)	—	35	—	45	—	55	—	70/85	ns
Write Cycle										
t_{WC}	Write Cycle Time	35	—	45	—	55	—	70/85	—	ns
$t_{CW1,2}$	Chip Select to End of Write	25	—	33	—	50	—	60/75	—	ns
t_{AW}	Address Valid to End of Write	25	—	33	—	50	—	60/75	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	25	—	25	—	50	—	60/75	—	ns
t_{WR1}	Write Recovery Time ($\overline{CS}_1$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
t_{WR2}	Write Recovery Time (CS_2)	5	—	5	—	5	—	5	—	ns
t_{WHZ}	Write Enable to Output in High Z(4)	—	14	—	18	—	25	—	30/35	ns
t_{DW}	Data to Write Time Overlap	15	—	20	—	25	—	30/35	—	ns
t_{DH1}	Data Hold from Write Time ($\overline{CS}_1$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
t_{DH2}	Data Hold from Write Time (CS_2)	5	—	5	—	5	—	5	—	ns
t_{OW}	Output Active from End of Write(4)	5	—	5	—	5	—	5	—	ns

2967 tbl 11

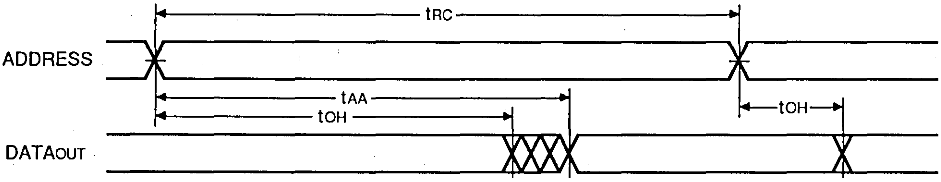
NOTES:
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only. Also available: 100, 120, 150, and 200ns military devices.
3. Both chip selects must be active for the device to be selected.
4. This parameter is guaranteed, but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



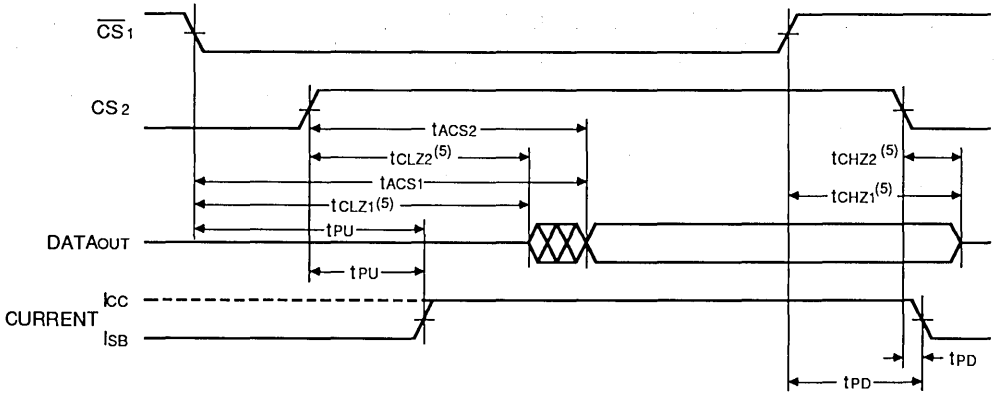
2967 drw 08

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2967 drw 09

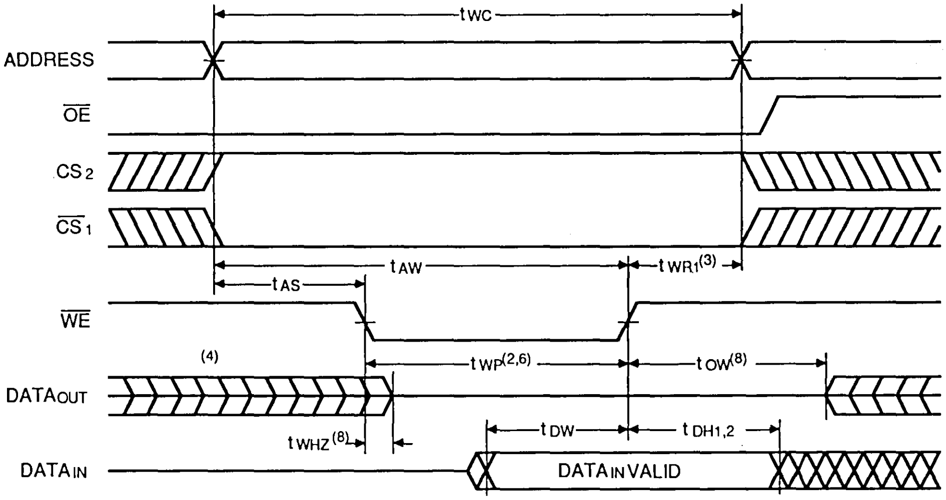
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



2967 drw 10

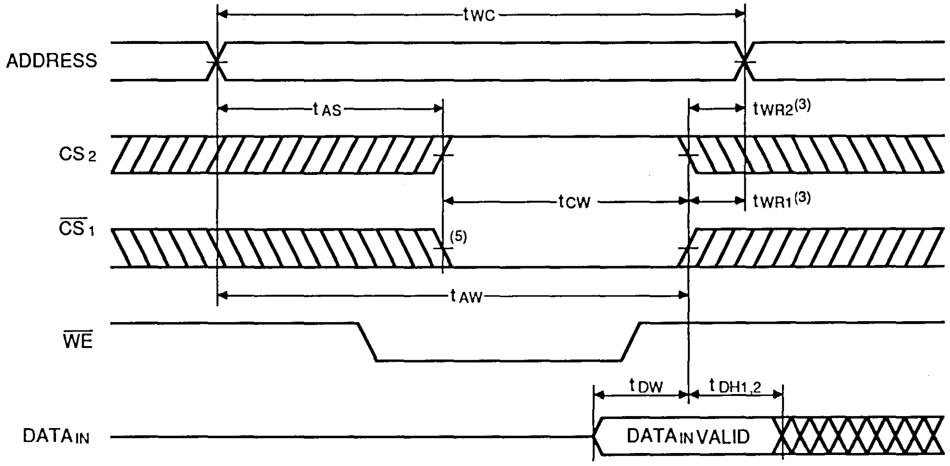
NOTES:
1. WE is high for read cycle.
2. Device is continuously selected, CS1 = V_{IL}, CS2 = V_{IH}.
3. Address valid prior to or coincident with CS1 transition low and CS2 transition high.
4. OE = V_{IL}.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{\text{WE}}$ CONTROLLED TIMING)(1)



2967 drw 11

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{\text{CS}}$ CONTROLLED TIMING)(1)



2967 drw 12

NOTES:

1. $\overline{\text{WE}}$, $\overline{\text{CS}}_1$ or CS_2 must be inactive during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{\text{WE}}$, a low $\overline{\text{CS}}_1$ and a high CS_2.
3. $t_{WR1,2}$ is measured from the earlier of $\overline{\text{CS}}_1$ or $\overline{\text{WE}}$ going high or CS_2 going low to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{\text{CS}}_1$ low transition or CS_2 high transition occurs simultaneously with or after the $\overline{\text{WE}}$ low transition, the outputs remain in a high impedance state.
6. If $\overline{\text{OE}}$ is low during a $\overline{\text{WE}}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} +t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{\text{OE}}$ is high during a $\overline{\text{WE}}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the spectified t_{WP}.
7. DATA_{OUT} is the same phase of write data of this write cycle.
8. Transition is measured ±200mV from steady state.

ORDERING INFORMATION

IDT	XXXX	X	XXX	XXX	X
	Device Type	Power	Speed	Package	Process/ Temperature Range

Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Y	SOJ (300 mil)
PE	SOIC (330 mil)
TC[1]	Side Braze (300 mil)
TD	CERDIP (300 mil)
D	CERDIP (600 mil)
P	Plastic DIP (600 mil)
TP	Plastic DIP (300 mil)
J	Plastic Leaded Chip Carrier
L28	28 Leadless Chip Carrier
L32	32 Leadless Chip Carrier
E	CERPACK F11A
XE	CERPACK F11

15	Commercial Only	Speed in Nanoseconds
20		
25		
30		
35		
45	Military Only	
55	Military Only	
70	Military Only	
85	Military Only	
100	Military Only	
120	Military Only	
150	Military Only	
200	Military Only	

S	Standard Power
L	Low Power

7164	64K (8K x 8-Bit) CMOS Static RAM

2967 drw 13

NOTE:
1. TC package will be replaced by TD.

Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (8K x 8-BIT) RESETTABLE RAM

IDT7165S
IDT7165L

NOT RECOMMENDED FOR NEW DESIGNS [1]

FEATURES:

- High-speed asynchronous RAM clear on Pin 1 (clears all RAM bits to 0, reset cycle time = 2 x t_{AA})
- High-speed address access time
  - — Military: 35/45/55ns (max.)
  - — Commercial: 30/35/45ns (max.)
- High-speed chip select ($\overline{CS}_1$) time
  - — Military: 20/25/30 (max.)
  - — Commercial: 15/20/25ns (max.)
- Low-power operation
  - — IDT7165S
    Active: 300mW (typ.)
    Standby: 100µW (typ.)
  - — IDT7165L
    Active: 250mW (typ.)
    Standby: 30µW (typ.)
- Battery backup operation — 2V data retention voltage (IDT7165L only)
- Produced with CEMOS™ high-performance technology
- Single 5V(+10%) power supply
- Input and output directly TTL-compatible
- Standard 28-pin, 600 mil DIP, 300 mil DIP, 28-pin SOIC, 32-pin LCC and PLCC
- Military product is compliant to MIL-STD-883, Class B

DESCRIPTION:

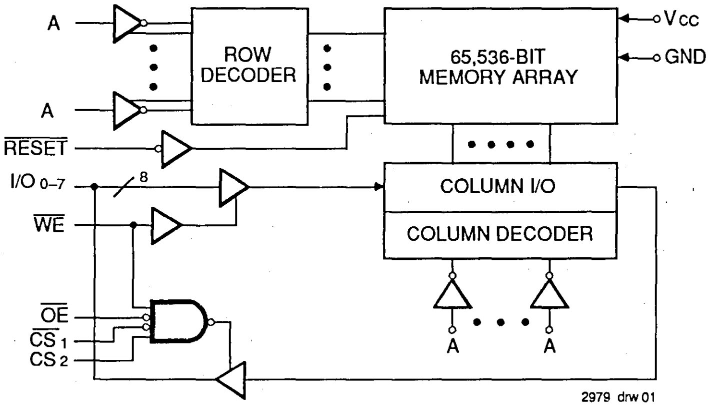
The IDT7165 is a high-speed 65,536-bit static RAM, organized 8K x 8, with reset function. The $\overline{\text{RESET}}$ pin provides a single RAM clear control which clears all words in the internal RAM to zero when activated. This allows the memory bits for all locations to be cleared at power-on or system reset, or for a fast clear to be available to graphics, histogramming and other designs where a byte-by-byte RAM clear would cause noticeable system speed degradation.

This product is fabricated using IDT's high-performance, high-reliability CEMOS technology. Address access time of 20ns and chip select ($\overline{CS}_1$) time of 15ns are available with maximum power consumption of only 770mW. This circuit also offers a reduced power standby mode. When CS_2 goes low, the circuit will automatically go to and remain in a low-power standby mode. In the full standby mode, the low-power device typically consumes less than 30µW. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 10µW operating from a 2V battery.

The IDT7165 is packaged in a 28-pin 300 or 600 mil DIP, 28-pin gull-wing SOIC, and 32-pin LCC and PLCC, providing high board level densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to the military temperature applications which require instant destruction of sensitive RAM data and demand the highest level of performance and reliability.

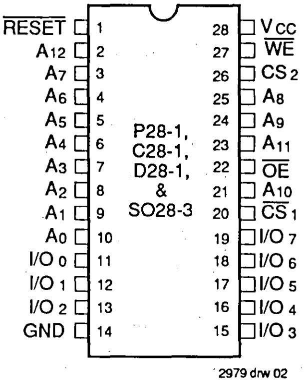
FUNCTIONAL BLOCK DIAGRAM



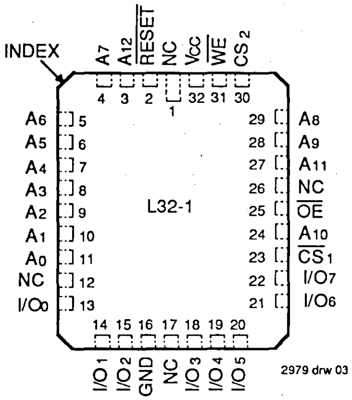
CEMOS is a trademark of Integrated Device Technology, Inc.

NOTE:
1. Not recommended for new designs. Contact marketing.

PIN CONFIGURATIONS



**DIP/SOIC
TOP VIEW**



**LCC/PLCC
TOP VIEW**

TRUTH TABLE (V_{CC} = 0.2V, V_{HC} = V_{CC} - 0.2V)[1,2]

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{RESET}$	I/O	Function
X	X	X	X	L	—	Reset all bits to low
X	H	X	X	H	Z	Deselect chip
X	X	L	X	H	Z	Deselect power down[1]
X	V_{HC}	X	X	H	Z	Deselect chip
X	X	V_{LC}	X	V_{HC}	Z	CMOS deselect power down[1]
H	L	H	H	H	Z	Output disable
H	L	H	L	H	D_{OUT}	Read
L	L	H	X	H	D_{IN}	Write

NOTE: 2979 tbl 01

1. CS_2 will power down $\overline{CS_1}$, but $\overline{CS_1}$ will not power down CS_2.
2. H = V_{IH}, L = V_{IL}, X = don't care.

PIN DESCRIPTIONS

A_{0-12}	Address
I/O_{0-7}	Data Input/Output
$\overline{CS_1}$, CS_2	Chip Select
$\overline{RESET}$	Memory Reset
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
V_{CC}	Power

2979 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2979 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2979 tbl 04

1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2979 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IHR}	$\overline{\text{RESET}}$ Input Voltage	2.5	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:

2979 tbl 06

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS(1, 2)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	7165S30		7165S/L35		7165S/L45		7165S/L55		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current $\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$ Outputs Open, V_{CC} = Max., f = 0	S	110	—	110	125	110	125	110	125	mA
		L	—	—	90	—	90	110	90	110	
I_{CC2}	Dynamic Operating Current $\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$ Outputs Open, V_{CC} = Max., f = f_{MAX}	S	160	—	150	160	150	160	150	160	mA
		L	—	—	130	—	120	130	115	125	
I_{SB}	Standby Power Supply Current (TTL Level) f = f_{MAX} $\overline{CS}_1 \geq V_{IH}$, $CS_2 \leq V_{IL}$, $\overline{\text{RESET}} \geq V_{IH}$ Outputs Open, V_{CC} = Max.	S	20	—	20	20	20	20	20	20	mA
		L	—	—	3	—	3	5	3	5	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) f = 0 $CS_2 \leq V_{LC}$ and $\overline{\text{RESET}} \geq V_{HC}$ V_{CC} = Max., $V_{IN} \geq V_{HC}$ or $V_{IN} \leq V_{LC}$	S	15	—	15	20	15	20	15	20	mA
		L	—	—	0.2	—	0.2	1.0	0.2	1.0	

NOTES:

2979 tbl 07

1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data are cycling at maximum frequency of read cycles f = 1/t_{RC}. f = 0 means no inputs change.

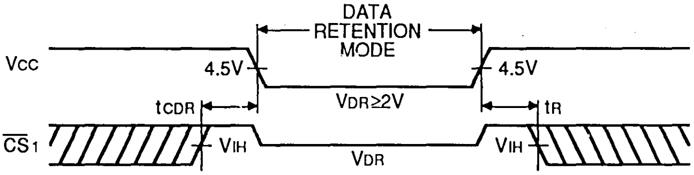
DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT7165S		IDT7165L		Unit
				Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.,	MIL.	—	10	—	5	µA
		V_{IN} = GND to V_{CC}	COM'L.	—	5	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS} = V_{IH}$,	MIL.	—	10	—	5	µA
		V_{OUT} = GND to V_{CC}	COM'L.	—	5	—	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		—	0.5	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	
V_{OH}	Output High Voltage	I_{OL} = -4mA, V_{CC} = Min.		2.4	—	2.4	—	V

2979 tbl 08

LOW Vcc DATA RETENTION WAVEFORM



2979 drw 04

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) VLC = 0.2V, VHC = VCC - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.[1] Vcc @ 2.0v	Typ.[1] Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
VDR	Vcc for Data Retention	—		2.0	—	—	—	—	V
ICCDR	Data Retention Current		MIL.	—	10	15	200	300	µA
			COM'L.	—	10	15	60	90	
tCDR[3]	Chip Deselect to Data Retention Time	CS2 ≤ VLC, $\overline{\text{CS}}_1$ ≥ VHC $\overline{\text{RESET}}$ ≥ VHC		0	—	—	—	—	ns
tR[3]	Operation Recovery Time			tRC[2]	—	—	—	—	ns
|ILI|[3]	Input Leakage Current			—	—	—	2	2	µA

2979 tbl 08

NOTES:
1. TA = +25°C.
2. tRC = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2979 tbl 09

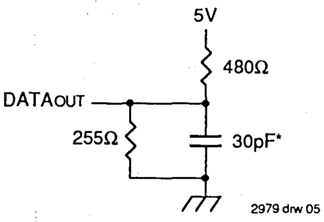


Figure 1. Output Load

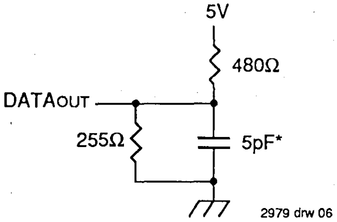


Figure 2. Output Load
(for tCLZ1, 2, tOLZ, tCHZ1, 2, tOHZ, tOW, tWHZ)

*Includes scope and jig.

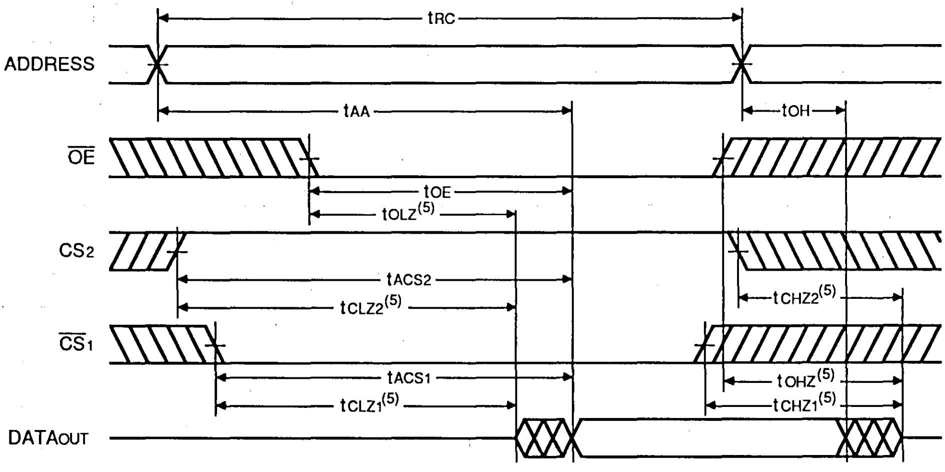
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

		7165S30(1)		7165S35 7165L35(1)		7165S45 7165L45		7165S55(3) 7165L55(3)		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle										
t_{RC}	Read Cycle Time	30	—	35	—	45	—	55	—	ns
t_{AA}	Address Access Time	—	30	—	35	—	45	—	55	ns
t_{ACS1}	Chip Select-1 Access Time(2)	—	15	—	20	—	25	—	30	ns
t_{ACS2}	Chip Select-2 Access Time(2)	—	35	—	40	—	45	—	55	ns
t_{CLZ1}	Chip Select-1 to Output in Low Z(4)	0	—	0	—	0	—	0	—	ns
t_{CLZ2}	Chip Select-2 to Output in Low Z(4)	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	15	—	20	—	25	—	30	ns
t_{OLZ}	Output Enable to Output in Low Z(4)	3	—	3	—	3	—	3	—	ns
t_{CHZ1}	Chip Select-1 to Output in High Z(4)	—	13	—	15	—	20	—	25	ns
t_{CHZ2}	Chip Select-2 to Output in High Z(4)	—	13	—	15	—	20	—	25	ns
t_{OHZ}	Output Disable to Output in High Z(4)	—	14	—	15	—	20	—	25	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{PU}	Chip Select to Power Up Time(4)	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Select to Power Down Time(4)	—	30	—	35	—	45	—	55	ns
Write Cycle										
t_{WC}	Write Cycle Time	30	—	35	—	45	—	55	—	ns
t_{CW1}	Chip Select-1 to End of Write ($\overline{CS}_1$)	20	—	20	—	25	—	30	—	ns
t_{CW2}	Chip Select-2 to End of Write (CS_2)	22	—	25	—	33	—	50	—	ns
t_{AW}	Address Valid to End of Write	22	—	25	—	33	—	50	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	23	—	25	—	25	—	50	—	ns
t_{WR1}	Write Recovery Time ($\overline{CS}_1$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
t_{WR2}	Write Recovery Time (CS_2)	5	—	5	—	5	—	5	—	ns
t_{WHZ}	Write Enable to Output in High Z(4)	—	12	—	14	—	18	—	25	ns
t_{DW}	Data to Write Time Overlap	13	—	15	—	20	—	25	—	ns
t_{DH1}	Data Hold from Write Time ($\overline{CS}_1$)	3	—	3	—	3	—	3	—	ns
t_{DH2}	Data Hold from Write Time (CS_2)	5	—	5	—	5	—	5	—	ns
t_{OW}	Output Active from End of Write(4)	5	—	5	—	5	—	5	—	ns

2976 tbl 08

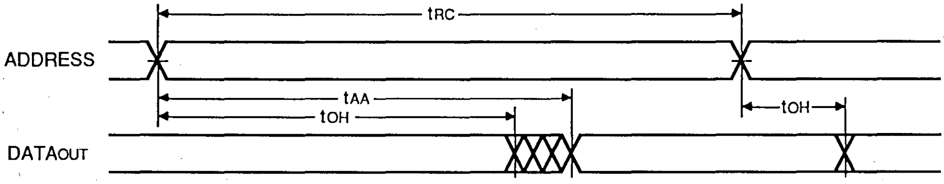
NOTES:
1. 0° to +70°C temperature range only.
2. Both chip selects must be active for the device to be selected.
3. -55°C to +125°C temperature range only.
4. This parameter is guaranteed, but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1[1]



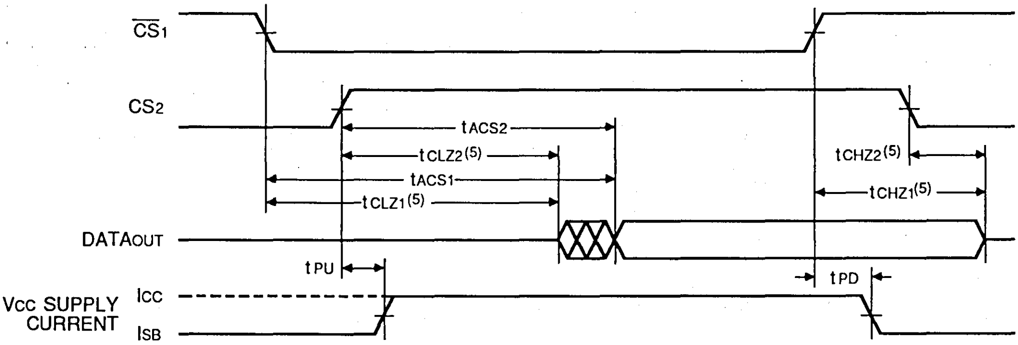
2979 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2[1, 2, 4]



2979 drw 08

TIMING WAVEFORM OF READ CYCLE NO. 3[1, 3, 4]

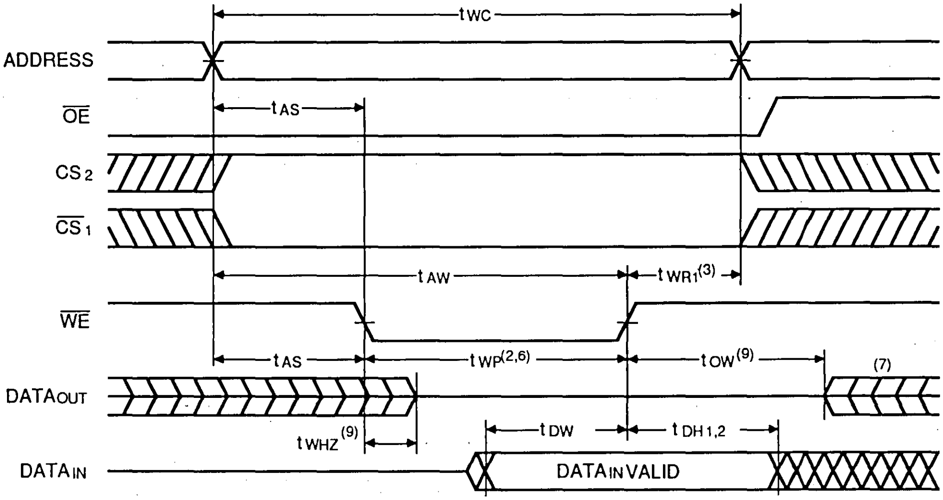


2979 drw 09

NOTES:

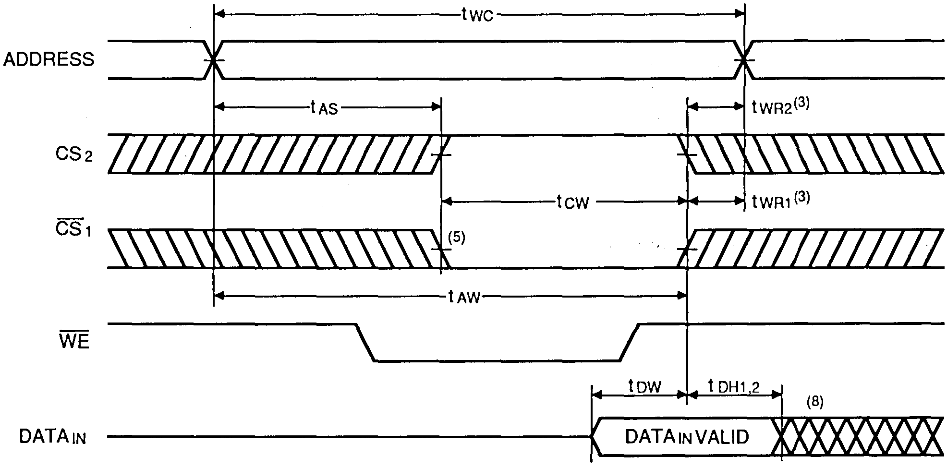
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{CS}_1$ transition low and CS_2 transition high.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1)



2979 drw 10

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1)



2979 drw 11

NOTES:

1. $\overline{WE}$, $\overline{CS}_1$ or CS_2 must be inactive during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{WE}$, a low $\overline{CS}_1$ and a high CS_2.
3. $t_{WR1,2}$ is measured from the earlier of $\overline{CS}_1$ or $\overline{WE}$ going high or CS_2 going low to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}_1$ low transition or CS_2 high transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} +t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the spectified t_{WP}.
7. DATAOUT is the same phase of write data of this write cycle.
8. If $\overline{CS}_1$ is low and CS_2 is high during this period, I/O pins are in the output state. Data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state.

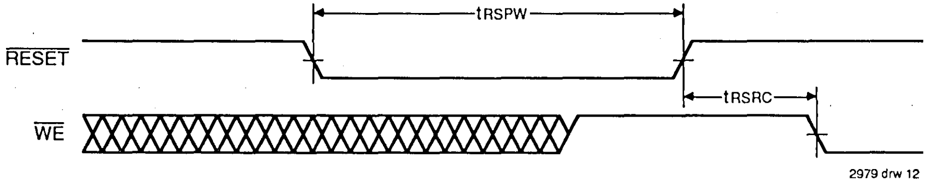
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

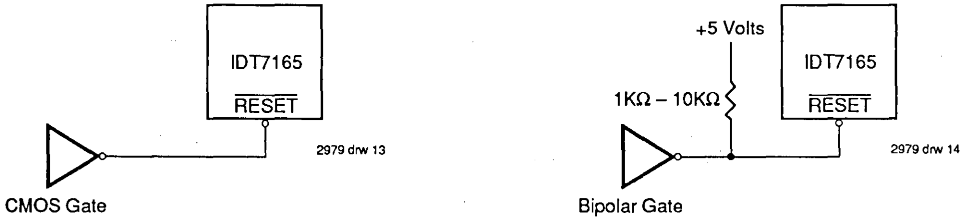
Symbol	Parameter	7165S30[1]		7165S35 7165L35[1]		7165S45 7165L45		7165S55[3] 7165L55[3]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
tRSPW	Reset Pulse Width[2]	55	—	65	—	80	—	100	—	ns
tRSRC	Reset High to $\overline{\text{WE}}$ Low	5	—	5	—	10	—	10	—	ns

2976 tbl 09

NOTES:
1. 0° to +70°C temperature range only.
2. Recommended duty cycle = 10% maximum.
3. -55°C to +125°C temperature range only.

RESET TIMING



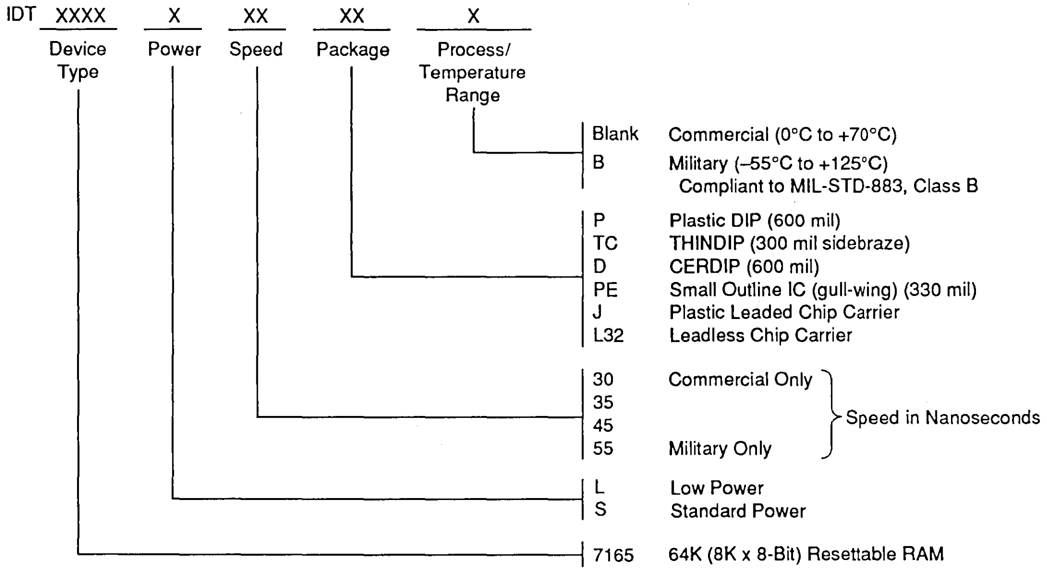


Driving the $\overline{\text{RESET}}$ pin with CMOS logic.

Driving the $\overline{\text{RESET}}$ pin with bipolar logic.

Figure 3.

ORDERING INFORMATION



2979 drw 15

Integrated Device Technology, Inc.

CMOS STATIC RAMS 16K (4K x 4-BIT)
Separate Data Inputs and Outputs

IDT71681SA/LA
IDT71682SA/LA

FEATURES:

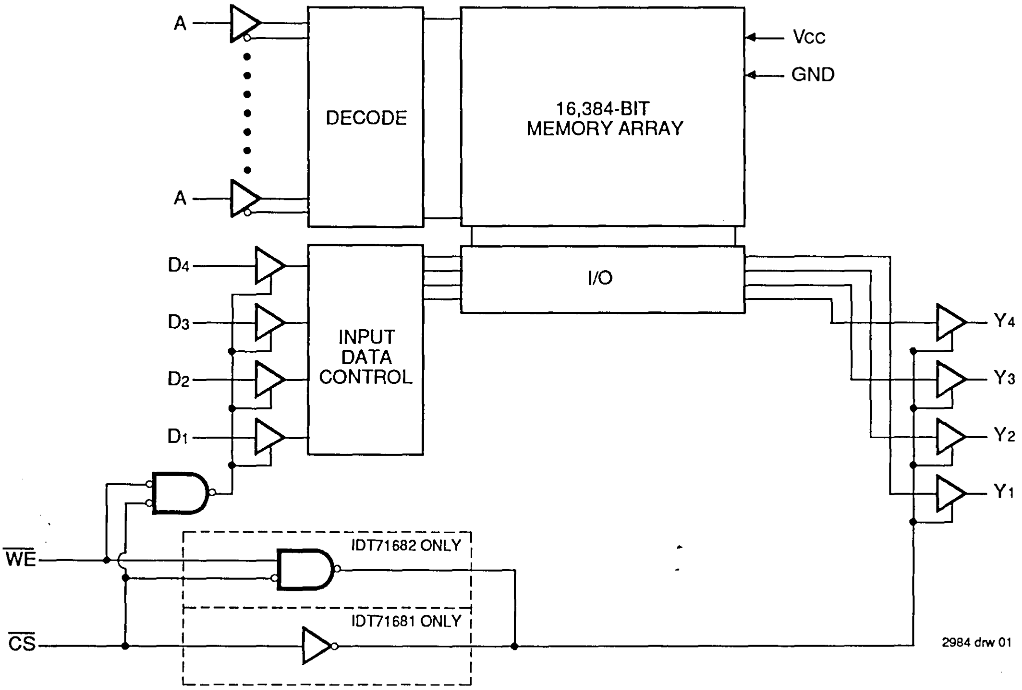
- Separate data inputs and outputs
- IDT71681SA/LA: outputs track inputs during write mode
- IDT71682SA/LA: high impedance outputs during write mode
- High speed (equal access and cycle time)
  - — Military: 12/15/20/25/35/45/55/70/85/100ns (max.)
  - — Commercial: 10/12/15/20/25/35/45ns (max.)
- Low power consumption
  - — IDT71681/2SA
    Active: 225mW (typ.)
    Standby: 100µw (typ.)
  - — IDT71681/2LA
    Active: 225mW (typ.)
    Standby: 10µW (typ.)
- Battery backup operation—2V data retention (LA version only)
- High-density 24-pin 300-mil ceramic or plastic DIP, 24-pin CERPACK, 24-pin SOIC, 24-pin SOJ and 28-pin leadless chip carrier
- Produced with advanced CEMOS™ high-performance technology
- CEMOS™ process virtually eliminates alpha particle soft-error rates
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Three-state output
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71681/IDT71682 are 16,384-bit high-speed static RAMs organized as 4K x 4. They are fabricated using IDT's high-performance, high-reliability technology—CEMOS™. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for high-speed memory applications.

Access times as fast as 10ns are available with maximum power consumption of only 550mW. These circuits also offer a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, this standby

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

DESCRIPTION (Continued):

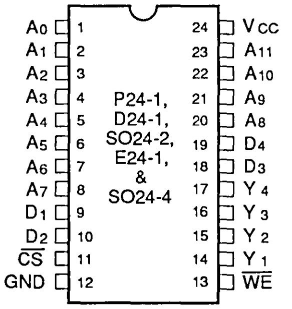
mode as long as $\overline{CS}$ remains high. In the standby mode , the devices consume less than 10µW, typically. This capability provides significant system-level power and cooling savings. The low-power (LA) versions also offer a battery backup data retention capability where the circuit typically consumes only 1µW operating off a 2V battery.

All inputs and outputs of the IDT71681/IDT71682 are TTL-compatible and operate from a single 5V supply.

The IDT71681/IDT71682 are packaged in either space-saving 24-pin, 300-mil DIPs, SOICs, SOJs, CERPACKS, or 28-pin leadless chip carriers, providing high board-level packing densities.

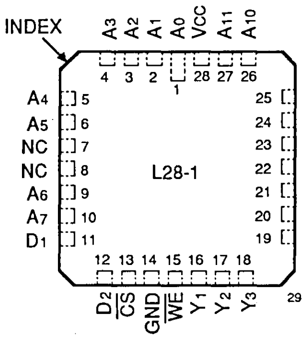
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS



2984 drw 02

DIP/SOIC/SOJ/CERPACK
TOP VIEW



2984 drw 03

LCC
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A0–A11	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
D1–D4	DATAIN
Y1–Y4	DATAOUT
VCC	Power
GND	Ground

2984 tbl 01

TRUTH TABLE[3]

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High Z	Standby
Read	L	H	DOUT	Active
Write[1]	L	L	DIN	Active
Write[2]	L	L	High Z	Active

NOTES: 2984 tbl 02
1. For IDT71681 only.
2. For IDT71682 only.
3. H = VIH, L = VIL, X = don't care.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

NOTE: 2984 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

NOTE: 2984 tbl 04
1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	$-0.5^{(1)}$	—	0.8	V

NOTE:

2984 tbl 05

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2984 tbl 06

DATA RETENTION CHARACTERISTICS

(LA Version Only)

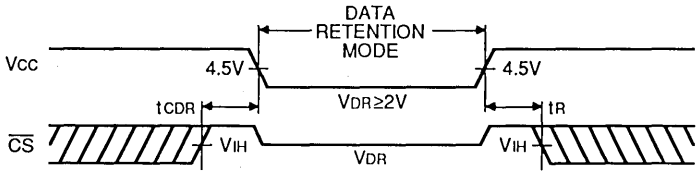
Symbol	Parameter	Test Condition		IDT71681/2LA Min.	Typ.$^{(1)}$	Max.	Unit
V_{DR}	V_{CC} for Data Retention			2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or ≤ 0.2V	MIL.	— —	$0.5^{(2)}$ $1.0^{(3)}$	$100^{(2)}$ $150^{(3)}$	µA
			COM'L.	— —	$0.5^{(2)}$ $1.0^{(3)}$	$20^{(2)}$ $30^{(3)}$	µA
$t_{CDR}^{(5)}$	Chip Deselect to Data Retention Time			0	—	—	ns
$t_R^{(5)}$	Operation Recovery Time			$t_{RC}^{(4)}$	—	—	ns

NOTES:

2984 tbl 07

1. T_A = +25°C.
2. at V_{CC} = 2V
3. at V_{CC} = 3V
4. t_{RC} = Read Cycle Time.
5. This parameter is guaranteed, but not tested.

LOW Vcc DATA RETENTION WAVEFORM



2984 drw 04

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT71681/2S Min.	Typ.	Max.	IDT71681/2L Min.	Typ.	Max.	Unit
$\lvert I_{LI}\rvert$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL. COM'L.	— —	— —	10 5	— —	— —	5 2	µA
$\lvert I_{LO}\rvert$	Output Leakage Current	V_{CC} = Max., $\overline{CS} = V_{IH}$, V_{OUT} = GND to V_{CC}	MIL. COM'L.	— —	— —	10 5	— —	— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.			—	0.5	—	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	—	0.4	—	—	0.4	
V_{OH}	Output High Voltage	I_{OL} = -4mA, V_{CC} = Min.		2.4	—	—	2.4	—	—	V

2984 tbl 08

DC ELECTRICAL CHARACTERISTICS(1,4)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	71681x10(5) 71682x10(5)		71681x12(7) 71682x12(7)		71681x15 71682x15		71681x20 71682x20		71681x25 71682x25		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max.,, f = 0(3)	SA	120	—	110	120	110	120	90	100	90	100	mA
		LA	—	—	—	—	—	—	70	80	70	80	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open,V_{CC} = Max., f = f_{MAX}(3)	SA	175	—	165	175	145	165	120	120	110	120	mA
		LA	—	—	—	—	—	—	100	110	90	100	
I_{SB}	Standby Power SupplyCurrent (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}(3)	SA	65	—	65	65	55	65	45	55	35	45	mA
		LA	—	—	—	—	—	—	30	35	25	30	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f=0(3)	SA	20	—	20	20	20	20	20	20	2	10	mA
		LA	—	—	—	—	—	—	0.5	5	0.05	0.3	

DC ELECTRICAL CHARACTERISTICS (Continued)(1,4)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	71681x35 71682x35		71681x45 71682x45		71681x55(6) 71682x55(6)		71681x70(2,6) 71682x70(2,6)		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0(3)	SA	90	100	90	100	—	100	—	100	mA
		LA	70	80	70	80	—	80	—	80	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}(3)	SA	100	110	100	110	—	110	—	110	mA
		LA	80	90	70	80	—	80	—	80	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}(3)	SA	30	35	30	35	—	35	—	35	mA
		LA	20	25	20	25	—	20	—	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f=0(3)	SA	2	10	2	10	—	10	—	10	mA
		LA	0.05	0.3	0.05	0.3	—	0.3	—	0.3	

NOTES:

2984 tbl 09

1. All values are maximum guaranteed values.
2. Also available 85 and 100ns military devices.
3. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.
4. "x" in part numbers indicates power rating (SA or LA).
5. 0°C to +70°C temperature range only.
6. -55°C to +125°C temperature range only.
7. Military values for 12ns device are preliminary only.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2984 tbl 10

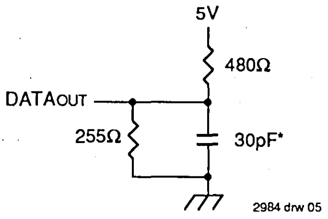


Figure 1. Output Load

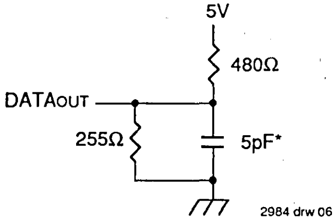


Figure 2. Output Load (for tHZ, tLZ, tWZ, and tOW)

*Includes scope and jig capacitances

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71681x10[1] 71682x10[1]		71681x12 71682x12		71681x15 71682x15		71681x20 71682x20		71681x25 71682x25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
tRC	Read Cycle Time	10	—	12	—	15	—	20	—	25	—	ns
tAA	Address Access Time	—	10	—	12	—	15	—	20	—	25	ns
tACS	Chip Select Access Time	—	10	—	12	—	15	—	20	—	25	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	ns
tLZ	Chip Select to Output in Low Z[3]	3	—	3	—	5	—	5	—	5	—	ns
tHZ	Chip Select to Output in High Z[3]	—	6	—	7	—	7	—	9	—	10	ns
tPU	Chip Select to Power Up Time[3]	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Select to Power Down Time[3]	—	10	—	10	—	15	—	20	—	25	ns

Continued on next page...

AC ELECTRICAL CHARACTERISTICS (Continued) (Vcc = 5.0V ± 10%, All Temperature Ranges)

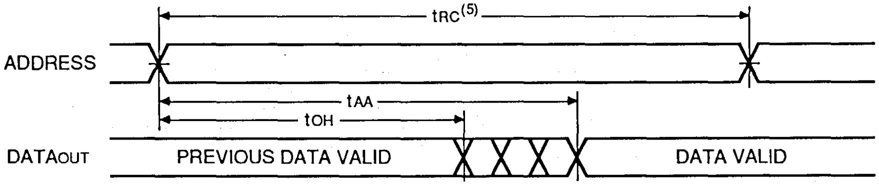
		71681x35 71682x35		71681x45 71682x45		71681x55[2] 71682x55[2]		71681x70[2] 71682x70[2]		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
Read Cycle										
t_{RC}	Read Cycle Time	35	—	45	—	55	—	70	—	ns
t_{AA}	Address Access Time	—	35	—	45	—	55	—	70	ns
t_{ACS}	Chip Select Access Time	—	35	—	45	—	55	—	70	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t_{LZ}	Chip Select to Output in Low Z(3)	5	—	5	—	5	—	5	—	ns
t_{HZ}	Chip Select to Output in High Z(3)	—	15	—	20	—	25	—	30	ns
t_{PU}	Chip Select to Power Up Time(3)	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Select to Power Down Time(3)	—	35	—	40	—	50	—	60	ns

NOTES:

2984 tbl 11

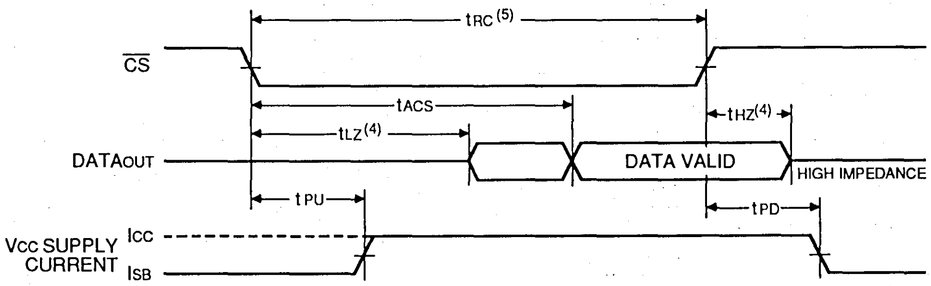
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. "x" in part numbers indicates power rating SA or LA.

TIMING WAVEFORM OF READ CYCLE NO. 1(1, 2)



2984 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 3)



2984 drw 08

NOTES:

1. $\overline{WE}$ is High for READ Cycle.
2. $\overline{CS}$ is Low for READ Cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

		71681x10(1) 71682x10(1)		71681x12 71682x12		71681x15 71682x15		71681x20 71682x20		71681x25 71682x25		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
Write Cycle												
t_{WC}	Write Cycle Time	10	—	12	—	15	—	20	—	20	—	ns
t_{CW}	Chip Select to End of Write	10	—	10	—	15	—	20	—	20	—	ns
t_{AW}	Address Valid to End of Write	10	—	10	—	15	—	20	—	20	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	10	—	10	—	15	—	20	—	20	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	7	—	8	—	9	—	10	—	10	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t_{IY}	Data Valid to Output Valid (71681 only)(3)	—	10	—	12	—	15	—	20	—	25	ns
t_{WY}	Write Enable to Output Valid (71681 only)(3)	—	10	—	12	—	15	—	20	—	25	ns
t_{WZ}	Write Enable to Output in High Z (71682 only)(3)	—	4	—	5	—	6	—	7	—	7	ns
t_{OW}	Output Active from End of Write (71682 only)(3)	0	—	0	—	0	—	0	—	0	—	ns

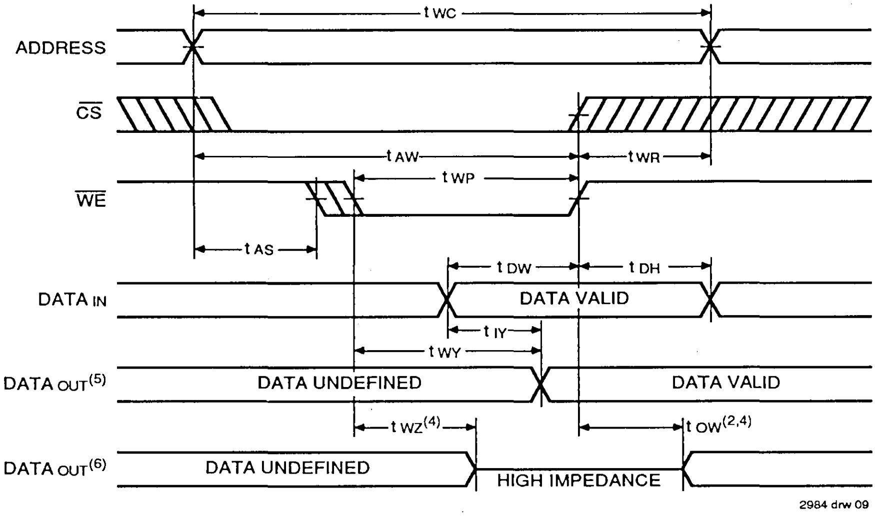
AC ELECTRICAL CHARACTERISTICS (Continued) (Vcc = 5.0V ± 10%, All Temperature Ranges)

		71681x35 71682x35		71681x45 71682x45		71681x55(2) 71682x55(2)		71681x70(2) 71682x70(2)		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
Write Cycle										
t_{WC}	Write Cycle Time	30	—	40	—	50	—	60	—	ns
t_{CW}	Chip Select to End of Write	25	—	35	—	50	—	60	—	ns
t_{AW}	Address Valid to End of Write	25	—	35	—	50	—	60	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	25	—	30	—	35	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	15	—	20	—	20	—	25	—	ns
t_{DH}	Data Hold Time	3	—	3	—	3	—	3	—	ns
t_{IY}	Data Valid to Output Valid (71681 only)(3)	—	30	—	35	—	35	—	40	ns
t_{WY}	Write Enable to Output Valid (71681 only)(3)	—	30	—	35	—	35	—	40	ns
t_{WZ}	Write Enable to Output in High Z (71682 only)(3)	—	13	—	20	—	25	—	30	ns
t_{OW}	Output Active from End of Write (71682 only)(3)	0	—	0	—	0	—	0	—	ns

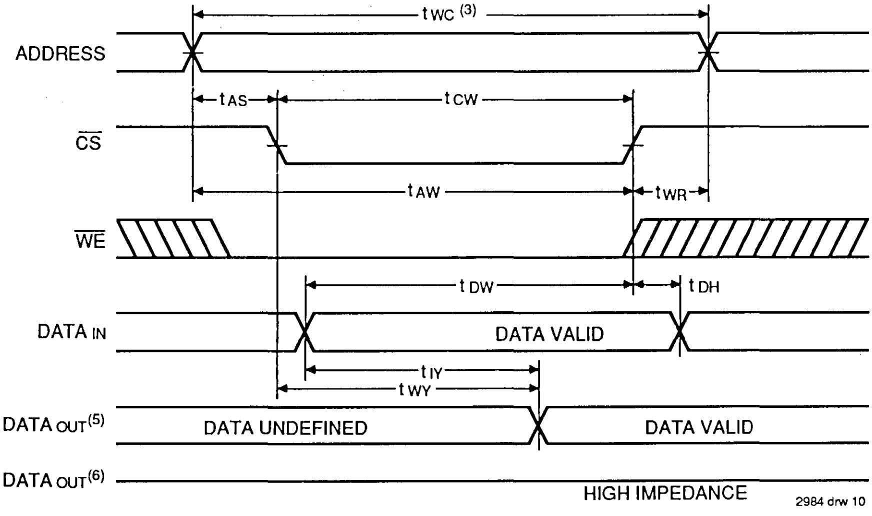
2984 tbl 12

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. "x" in part numbers indicates power rating SA or LA.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[1]

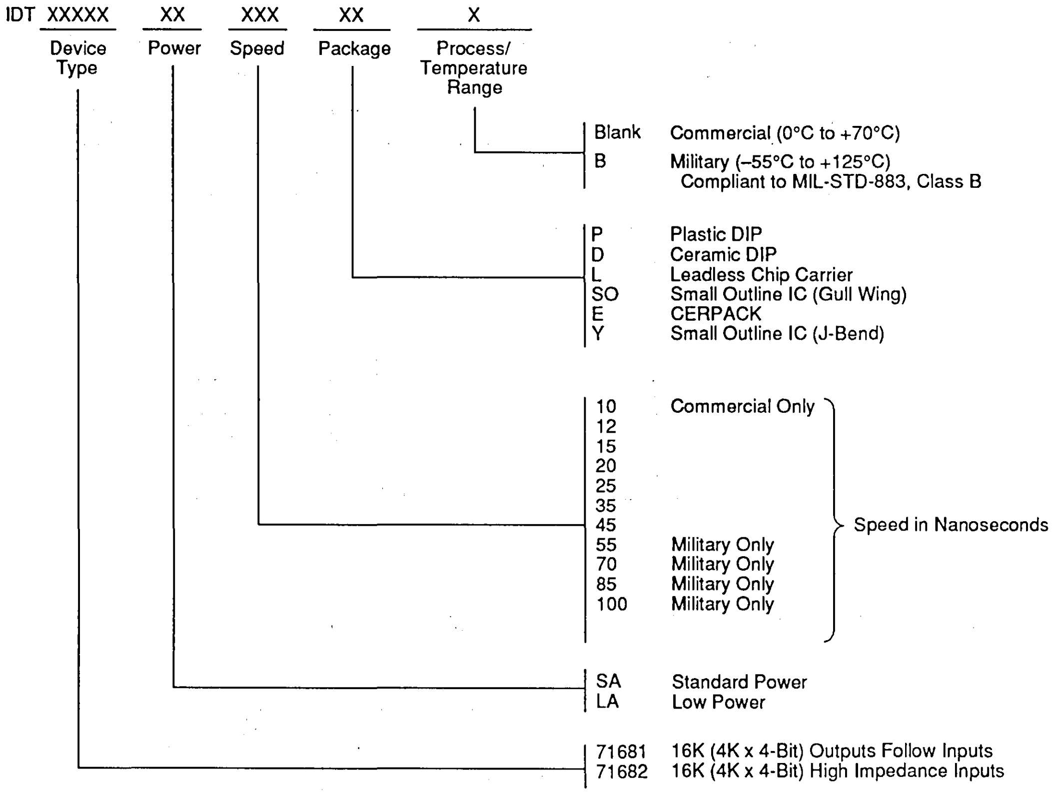


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)[1]



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. If the $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2.
5. For IDT71681 only.
6. For IDT71682 only.

ORDERING INFORMATION



2984 drw 11

Integrated Device Technology, Inc.

CMOS HIGH-SPEED STATIC RAM 72K (8K X 9-BIT)

ADVANCE INFORMATION
IDT7169S
IDT7169L

FEATURES:

- 8192-words x 9-bits organization
- JEDEC standard 28-pin DIP, SOJ, and 32-Pin LCC
- Fast access time:
  - — Commercial: 20/25/35ns (max.)
  - — Military: 25/35/45/55ns (max.)
- Battery backup operation
  - — 2V data retention (L-version only)
- Produced with advanced CEMOS™ high-performance technology
- Single 5V power supply
- Inputs and outputs directly TTL-compatible
- Military product available compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7169 is a 73,728-bit high-speed static RAM organized as 8K x 9. It is fabricated using IDT's high-performance, high-reliability CEMOS™ technology.

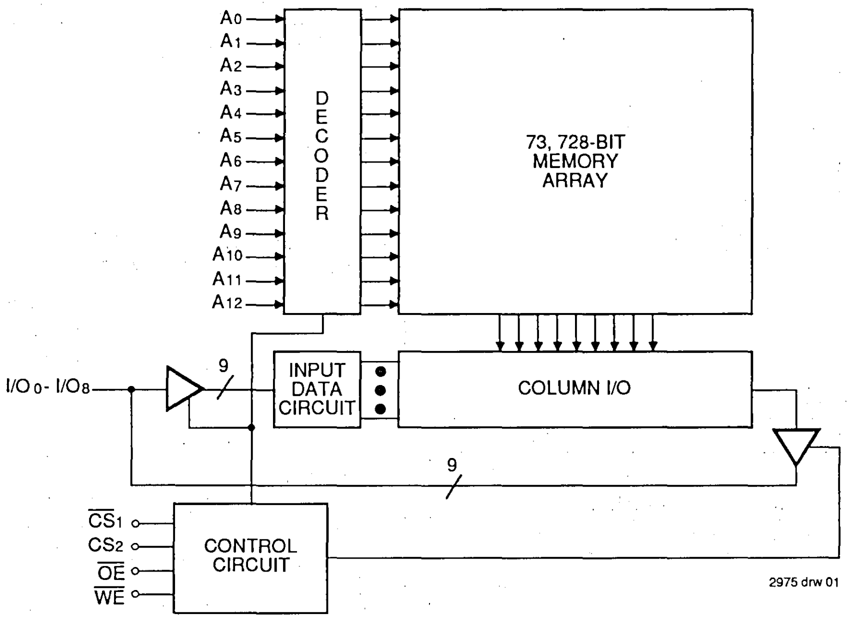
The IDT7169 offers address access times as fast as 15ns. The ninth bit is optimal for systems using parity.

All inputs and outputs of the IDT7169 are TTL-compatible. The device has 2 chip selects for simplified address decoding.

The IDT7169 is packaged in an industry standard 300-mil 28-pin ceramic and plastic DIP and SOJ, along with a 32-pin LCC package.

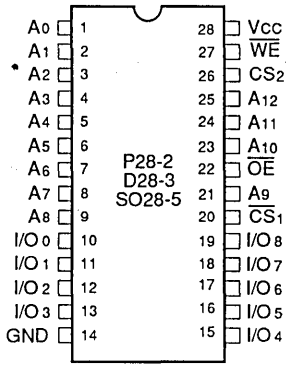
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



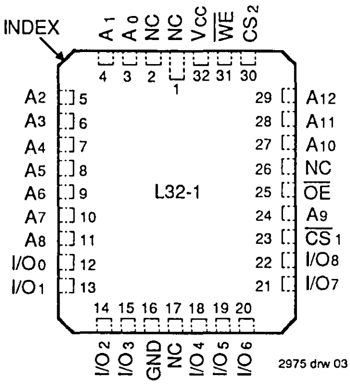
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



2975 drw 02

DIP/SOJ
TOP VIEW



2975 drw 03

LCC
TOP VIEW

TRUTH TABLE[1]

CS2	$\overline{CS}_1$	$\overline{OE}$	$\overline{WE}$	I/O	Function
X	H	X	X	High Z	Deselect chip, Power down
L	X	X	X	High Z	Deselct chip
H	L	L	H	DOUT	Read
H	L	X	L	DIN	Write
H	L	H	H	High Z	Outputs Disabled

NOTE: 2975 tbl 01
1. H = V_{IH}, L = V_{IL}, X = Don't Care

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +135	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2975 tbl 02
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2975 tbl 03
1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2975 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2975 tbl 04
1. V_{IL} = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

			7169S20 7169L20		7169S25 7169L25		7169S35 7169L35		7169S45/55 7169L45/55		
Symbol	Parameter	Power	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS}_1$ = V_{IL}, Outputs Open, CS_2 = V_{IH} V_{CC} = Max., f = 0(2)	S	90	—	90	110	90	100	—	100	mA
		L	80	—	80	100	80	90	—	90	
I_{CC2}	Dynamic Operating Current $\overline{CS}_1$ = V_{IL}, Outputs Open, CS_2 = V_{IH} V_{CC} = Max., f = f_{MAX}(2)	S	180	—	170	190	150	160	—	160	mA
		L	160	—	150	170	130	140	—	130	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}_1$ ≥ V_{IH}, V_{CC} = Max., CS_2 = V_{IL} Outputs Open, f = f_{MAX}(2)	S	20	—	20	20	20	20	—	20	mA
			L	3	—	3	5	3	5	—	5
I_{SB1}	Full Standby Power Supply Current (CMOS Level), f = 0(2) $\overline{CS}_1$ ≥ V_{HC} and CS_2 ≥ V_{HC} CS_2 ≤ V_{LC}, V_{CC} = Max.	S	15	—	15	20	15	20	—	20	mA
		L	0.2	—	0.2	1.0	0.2	1.0	—	1.0	

2975 tbl 06

NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2975 tbl 07

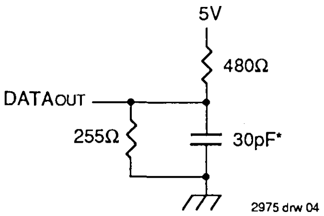


Figure 1. Output Load

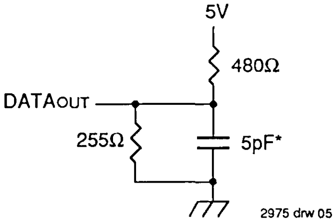


Figure 2. Output Load
(for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

*Includes scope and jig capacitances

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT7169S Min.	IDT7169S Max.	IDT7169L Min.	IDT7169L Max.	Unit
$\lvert I_{LI} \rvert$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL. COM'L.	— —	10 5	— —	5 2	µA
$\lvert I_{LO} \rvert$	Output Leakage Current	V_{CC} = Max., $\overline{CS}_1$ = V_{IH}, CS_2 = V_{IL}, V_{OUT} = GND to V_{CC}	MIL. COM'L.	— —	10 5	— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min. I_{OL} = 10mA, V_{CC} = Min.		 —	0.4 0.5	— —	0.4 0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	2.4	—	V

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

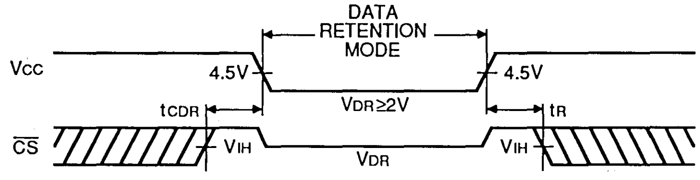
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.[1] Vcc @ 2.0v	Typ.[1] Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	Vcc for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current		MIL. COM'L.	— —	10 10	15 15	200 60	300 90	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time	1. $\overline{CS}_1 \geq V_{HC}$ 2. $CS_2 \leq V_{LC}$		0	—	—	—	—	ns
t_R[3]	Operation Recovery Time	$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$		t_{RC}[2]	—	—	—	—	ns
$\lvert I_{LI} \rvert$[3]	Input Leakage Current			—	—	—	2	2	µA

2975 tbl 09

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

LOW Vcc DATA RETENTION WAVEFORM



2975 drw 06

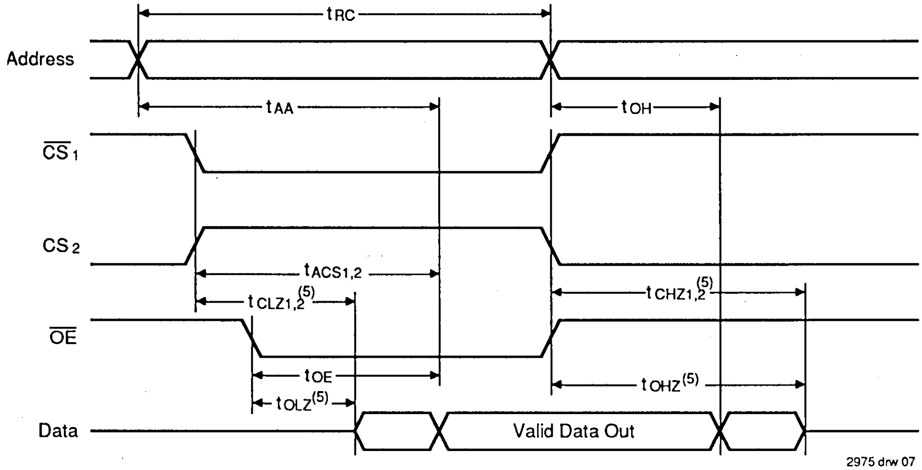
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7169S20(1) 7169L20(1)		7169S25 7169L25		7169S35 7169L35		7169S45/55(3) 7169L45/55(3)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
tRC	Read Cycle Time	20	—	25	—	35	—	45/55	—	ns
tAA	Address Access Time	—	19	—	25	—	35	—	45/55	ns
tACS1	Chip Select-1 Access Time	—	20	—	25	—	35	—	45/55	ns
tACS2	Chip Select-2 Access Time	—	25	—	35	—	40	—	45/55	ns
tCLZ1, 2	Chip Select to Output in Low Z(2)	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	8	—	12	—	18	—	25/30	ns
tOLZ	Output Enable to Output in Low Z(2)	3	—	3	—	3	—	3	—	ns
tCHZ1, 2	Chip Select-1, 2 to Output in High Z(2)	—	9	—	13	—	15	—	20/25	ns
tOHZ	Output Disable to Output in High Z(2)	—	8	—	10	—	15	—	20/25	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
Write Cycle										
tWC	Write Cycle Time	20	—	25	—	35	—	45/55	—	ns
tAW	Address Valid to End of Write	15	—	18	—	25	—	33/50	—	ns
tCW1	Chip Select to End of Write ($\overline{\text{CS}}_1$)	15	—	18	—	25	—	33/50	—	ns
tCW2	Chip Select to End of Write (CS2)	15	—	18	—	25	—	33/50	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	15	—	21	—	25	—	25/50	—	ns
tWR1	Write Recovery Time ($\overline{\text{CS}}_1$, $\overline{\text{WE}}$)	0	—	0	—	0	—	0	—	ns
tWR2	Write Recovery Time (CS2)	5	—	5	—	5	—	5	—	ns
tWHZ	Write Enable to Output in High Z(2)	—	8	—	10	—	14	—	18/25	ns
tDW	Data to Write Time Overlap	10	—	13	—	15	—	20/25	—	ns
tDH1	Data Hold from Write Time ($\overline{\text{CS}}_1$, $\overline{\text{WE}}$)	0	—	0	—	0	—	0	—	ns
tDH2	Data Hold from Write Time (CS2)	5	—	5	—	5	—	5	—	ns
tOW	Output Active from End of Write(2)	5	—	5	—	5	—	5	—	ns

2975 tbl 10

NOTES:
1. 0° to +70°C temperature range only.
2. This parameter guaranteed but not tested.
3. -55° to +125°C. temperature range only.

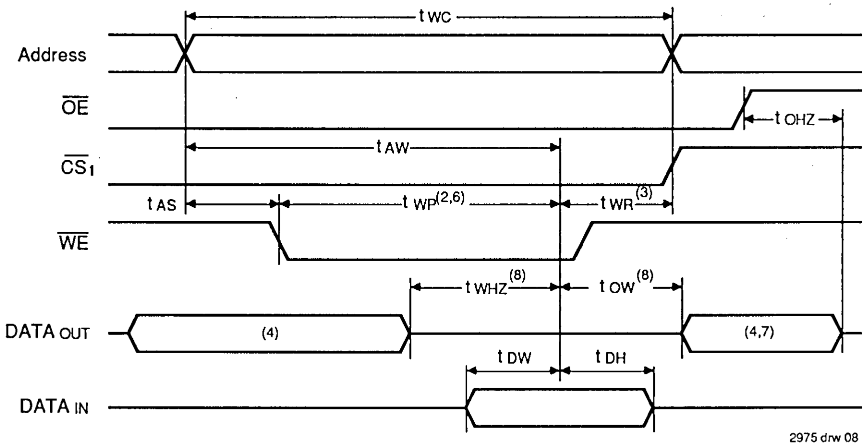
TIMING WAVEFORM OF READ CYCLE (1)



NOTES:

1. $\overline{\text{WE}}$ is high for read cycle.
2. Device is continuously selected, $\overline{\text{CS}}_1 = V_{IL}$., $\text{CS}_2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{\text{CS}}_1$ transition low and CS_2 transition high.
4. $\overline{\text{OE}} = V_{IL}$.
5. Transition is measured ±200mV from steady state.

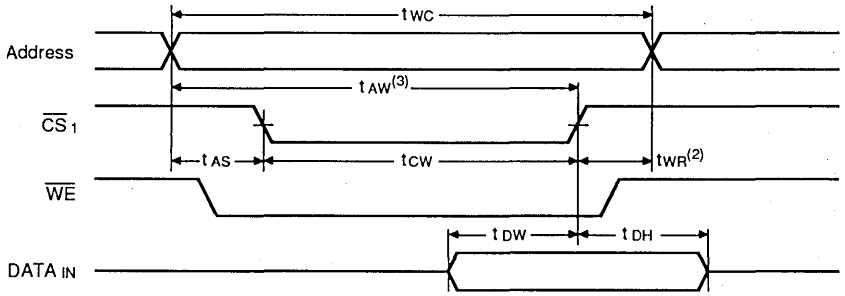
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{\text{WE}}$ CONTROLLED TIMING)(1,2,5)



NOTES:

1. $\overline{\text{WE}}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{\text{CS}}_1$ and a high CS_2.
3. $t_{WR1,2}$ is measured from the earlier of $\overline{\text{CS}}_1$ or $\overline{\text{WE}}$ going high or CS_2 going low to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{\text{CS}}_1$ low transition or CS_2 high transition occurs simultaneously with or after the $\overline{\text{WE}}$ low transition, the outputs remain in a high impedance state.
6. If $\overline{\text{OE}}$ is low during a $\overline{\text{WE}}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or ($t_{WHZ} + t_{DW}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{\text{OE}}$ is high during a $\overline{\text{WE}}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the spectified t_{WR}.
7. DATA_{OUT} is the same phase of write data of this write cycle.
8. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)$^{(1,3)}$



2975 drw 09

NOTES:
1. $\overline{WE}$ must be high during all address transitions.
2. $t_{WR1,2}$ is measured from the earlier of $\overline{CS}_1$ or $\overline{WE}$ going high or CS_2 going low to the end of the write cycle.
3. If the $\overline{CS}_1$ low transition or CS_2 high transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
4. Transition is measured ±200mV from steady state.

ORDERING INFORMATION

IDT XXXX X XX XX X

Field	Code	Description
Process/ Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B
Package	TP	Plastic DIP (300mil)
	TD	CERDIP (300mil)
	L32	32 Leadless Chip Carrier
	Y	Small Outline IC (J-Bend)
Speed	20	Commercial Only
	25	Com'l. & Mil.
	35	Com'l. & Mil.
	45	Military Only
	55	Military Only
Power	S	Standard Power
	L	Low Power
Device Type	7169	72K (8K x 9-Bit) CMOS Static RAM

Speed in Nanoseconds

2975 drw 10

Integrated Device Technology, Inc.

CMOS STATIC RAM
64K (8K x 8-BIT)
CACHE-TAG RAM

IDT7174S
NOT RECOMMENDED FOR NEW DESIGNS
SEE IDT71B74 PAGE 6.15

FEATURES:

- High-speed address to MATCH comparison time
  - — Military: 35/45/55ns (max.)
  - — Commercial: 30/35/45ns (max.)
- High-speed address access time
  - — Military: 35/45/55ns (max.)
  - — Commercial: 30/35/45ns (max)
- High-speed chip select access time
  - — Military: 20/25/30ns (max.)
  - — Commercial: 15/20/25ns (max.)
- Low-power operation
  - — IDT7174S
    Active: 300mW (typ.)
- High-speed asynchronous RAM Clear on Pin 1 (Reset Cycle Time = 2 x tAA)
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (+10%) power supply
- Input and output directly TTL-compatible
- Military product compliant to MIL-STD-883, Class B
- Standard 28-pin plastic DIP (600 mil), 28-pin SOIC (330 mil gull-wing), 28-pin hermetic DIP (300 mil or 600 mil), 32-pin LCC and PLCC
- Not recommended for new designs. See FDT71B74, page 6.15

DESCRIPTION:

The IDT7174 is a high-speed cache address comparator subsystem consisting of a 65,536-bit static RAM organized as 8K x 8 and an 8-bit comparator. A single IDT7174 can map 8K cache words into a 1 megabyte address space by comparing 20 bits of address organized as 13 word cache address bits and 7 upper address bits. Two IDT7174s can be combined to provide 28 bits of address comparison, etc. The IDT7174 also provides a single RAM clear control, which clears all words in the internal RAM to zero when activated. This allows the tag bits for all locations to be cleared at power-on or system-reset, a requirement for cache comparator systems.

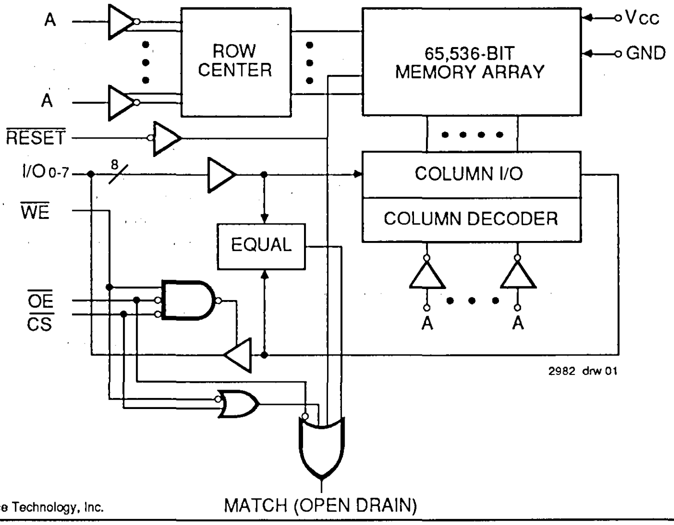
The IDT7174 is fabricated using IDT's high-performance, high-reliability technology — CEMOS. Address access times as fast as 30ns, chip select times of 15ns and address-to-comparison times of 30ns are available with maximum power consumption of 825mW.

All inputs and outputs of the IDT7174 are TTL-compatible. The MATCH pin of several 7174's can be wired-ORed together to provide enabling or acknowledging signals to the data cache or processor, thus eliminating logic delays and increasing system throughput. The device operates from a single 5V supply.

The IDT7174 is packaged in a 28-pin DIP (600 mil and 300 mil), a 28-pin SOIC (gull-wing) and 32-pin LCC and PLCC, providing high board level packing densities.

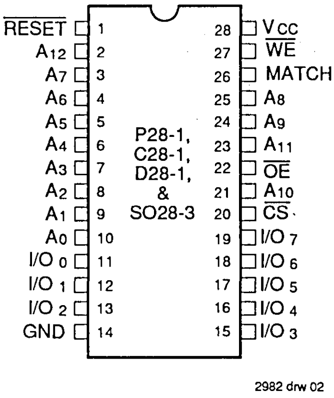
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

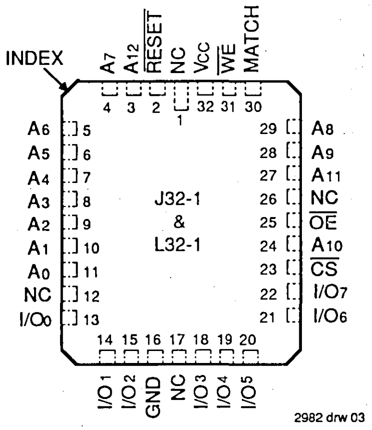


CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP/SOIC
TOP VIEW



LCC/PLCC
TOP VIEW

TRUTH TABLE[1]

$\overline{\text{WE}}$	$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{RESET}}$	MATCH	I/O	Function
X	X	X	L	H	—	Reset all bits to low
X	H	X	H	H	Hi Z	Deselect chip
H	L	H	H	L	D_{IN}	No MATCH
H	L	H	H	H	D_{IN}	MATCH
H	L	L	H	H	D_{OUT}	Read
L	L	X	H	H	D_{IN}	Write

NOTE: 2982 tbl 01

1. H = V_{IH}, L = V_{IL}, X = don't care.

PIN DESCRIPTIONS

A_{0-12}	Address
I/O_{0-7}	Data Input/Output
$\overline{\text{CS}}$	Chip Select
$\overline{\text{RESET}}$	Memory Reset
MATCH	Data/Memory Match (Open Drain)
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
GND	Ground
Vcc	Power

2982 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2982 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2982 tbl 04

1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage[1]	2.2	—	6.0	V
VIHR	$\overline{\text{RESET}}$ Input Voltage	2.5[2]	—	6.0	V
VIL	Input Low Voltage	-0.5[3]	—	0.8	V

NOTES:

2982 tbl 05

1. All inputs except $\overline{\text{RESET}}$.
2. When using bipolar devices to drive the $\overline{\text{RESET}}$ input, a pullup resistor of 1kΩ-10kΩ is usually required to assure this voltage.
3. VIL (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2982 tbl 06

DC ELECTRICAL CHARACTERISTICS[1,2]

(VCC = 5.0V ± 10%, VLC = 0.2V, VHC = VCC - 0.2V)

Symbol	Parameter	7174S30 Com'l.	7174S30 Mil.	7174S35 Com'l.	7174S35 Mil.	7174S45 Com'l.	7174S45 Mil.	7174S55 Com'l.	7174S55 Mil.	Unit
ICC1	Operating Power Supply Current Outputs Open, VCC = Max., f = 0	110	—	110	125	110	125	—	125	mA
ICC2	Dynamic Operating Current Outputs Open, VCC = Max., f = fMAX	170	—	150	170	140	150	—	145	mA

NOTES:

2982 tbl 07

1. All values are maximum guaranteed values.
2. f = MAX. means that address and data are cycling at maximum frequency of read cycles of 1/tRC.
   f = 0 means no inputs change.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMERATURE AND SUPPLY VOLTAGE (VCC = 5.0V ± 10%)

Symbol	Parameter	Test Condition		IDT7174S Min.	IDT7174S Max.	Unit
|ILI|	Input Leakage Current	VCC = Max., VIN = GND to VCC	MIL.	—	10	µA
			COM'L.	—	5	
|ILO|	Output Leakage Current[1]	VCC = Max., $\overline{\text{CS}}$ = VIH,	MIL.	—	10	µA
		VOUT = GND to VCC	COM'L.	—	5	
VOL	Output Low Voltage	IOL = 18mA MATCH		—	0.5	V
		IOL = 22mA MATCH		—	0.5	
		IOL = 10mA, VCC = Min. (Except MATCH)		—	0.5	
		IOL = 8mA, VCC = Min. (Except MATCH)		—	0.4	
VOH	Output High Voltage	IOL = -4mA, VCC = Min. (Except MATCH)		2.4	—	V

NOTE:

2992 tbl 08

1. Data and MATCH pins.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 and 3

2982 tbl 09

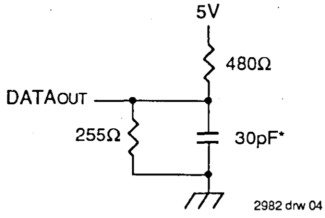


Figure 1. Output Load

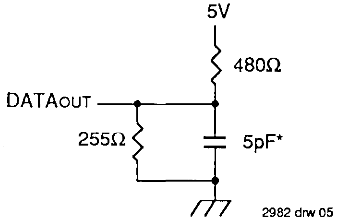
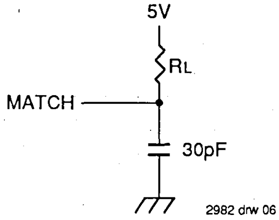


Figure 2. Output Load
(for tCLZ, tOLZ, tCHZ, tOHZ, tOW, tWHZ)

*Includes scope and jig.



RL = 200Ω (COM'L.)
= 270Ω (MIL.)

Figure 3. Output Load for MATCH

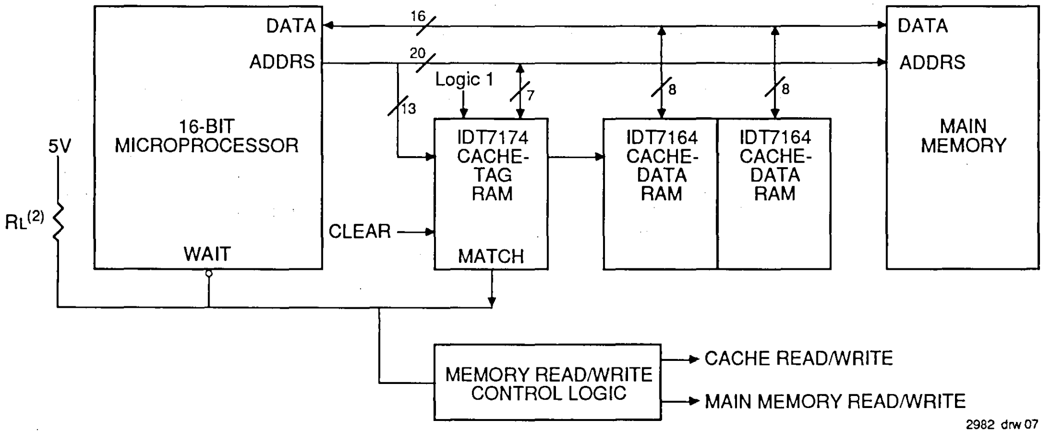


Figure 4. Example of Cache Memory System Block Diagram

NOTES:
1. For more information, see application note AN-07 "Cache-Tag RAM Chips Simplify Cache Memory Design".
2. RL = 200Ω (commercial) or 270Ω (military).

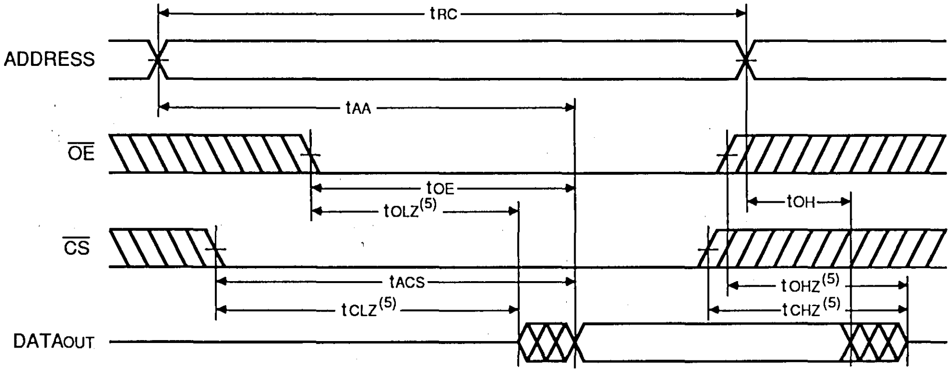
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7174S30(1)		7174S35		7174S45		7174S55(2)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	30	—	35	—	45	—	55	—	ns
t_{AA}	Address Access Time	—	30	—	35	—	45	—	55	ns
t_{ACS}	Chip Select Access Time	—	18	—	20	—	25	—	30	ns
t_{CLZ}	Chip Select to Output in Low Z(3)	0	—	0	—	0	—	0	—	ns
t_{OE}	Output Enable to Output Valid	—	18	—	20	—	25	—	30	ns
t_{OLZ}	Output Enable to Output in Low Z(3)	3	—	3	—	3	—	3	—	ns
t_{CHZ}	Chip Select to Output in High Z(3)	—	15	—	15	—	20	—	25	ns
t_{OHZ}	Output Disable to Output in High Z(3)	—	15	—	15	—	20	—	25	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns

2982 tbl 10

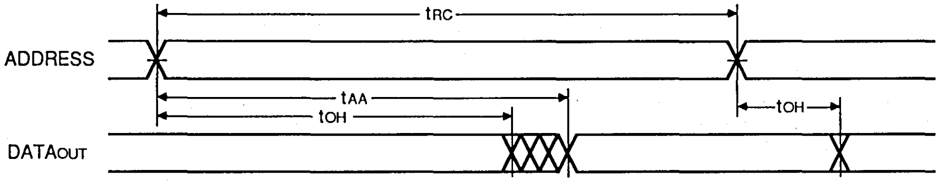
NOTES:
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed, but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



2982 drw 08

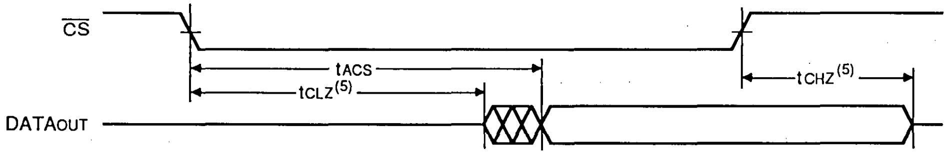
TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2982 drw 09

NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



2982 drw 10

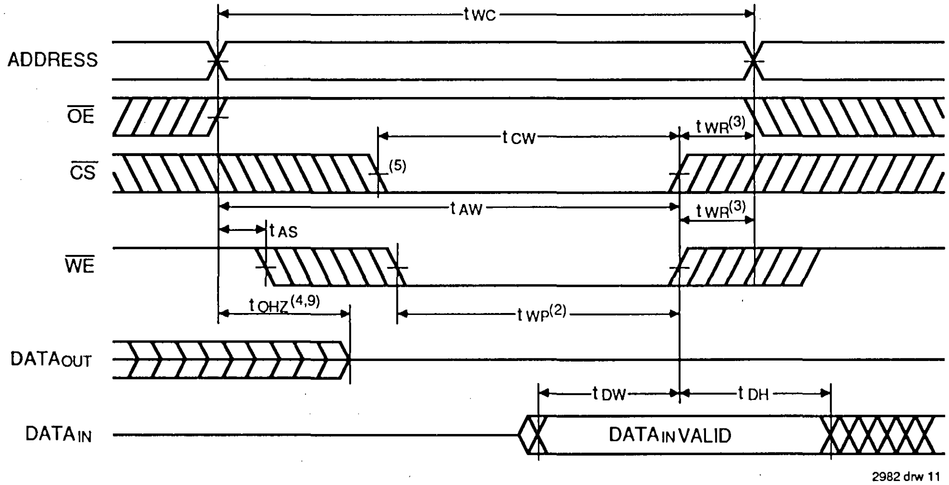
NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

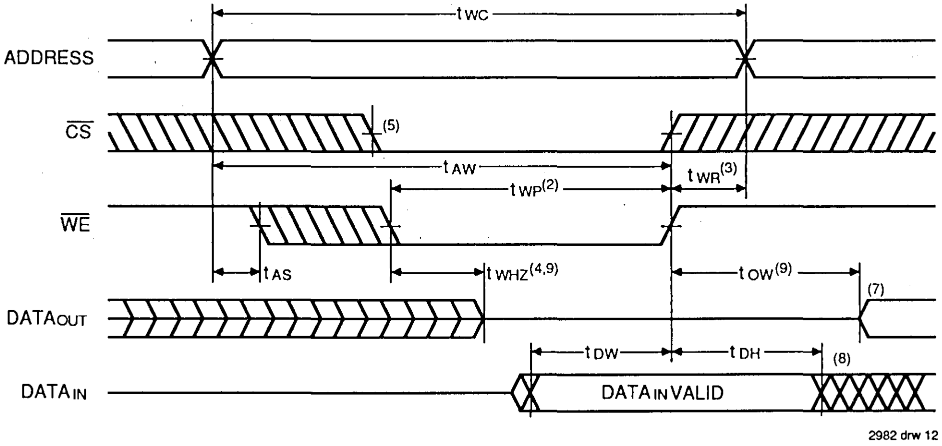
Symbol	Parameter	7174S30[1]		7174S35		7174S45		7174S55[2]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle										
tWC	Write Cycle Time	30	—	35	—	45	—	55	—	ns
tCW	Chip Select to End of Write	18	—	20	—	25	—	30	—	ns
tAW	Address Valid to End of Write	25	—	30	—	40	—	50	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	25	—	30	—	40	—	50	—	ns
tWR	Write Recovery Time ($\overline{CS}$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
tWHZ	Write Enable to Output in High Z[3]	—	15	—	15	—	20	—	25	ns
tDW	Data to Write Time Overlap	14	—	15	—	20	—	25	—	ns
tDH	Data Hold from Write Time	2	—	2	—	2	—	2	—	ns
tOW	Output Active from End of Write[3]	5	—	5	—	5	—	5	—	ns

NOTES:
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1(1)



TIMING WAVEFORM OF WRITE CYCLE NO. 2(1, 6)



NOTES:

1. WE, CS must be inactive during all address transitions.
2. A write occurs during the overlap (tWP) of a low WE and a low CS.
3. tWR is measured from the earlier of CS or WE going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the CS low transition occurs simultaneously with or after the WE low transition, the outputs remain in a high impedance state.
6. If OE is continuously low (OE = VIL).
7. DATAOUT is the same phase of write data of this write cycle.
8. If CS is low during this period, I/O pins are in the output state. Data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state.

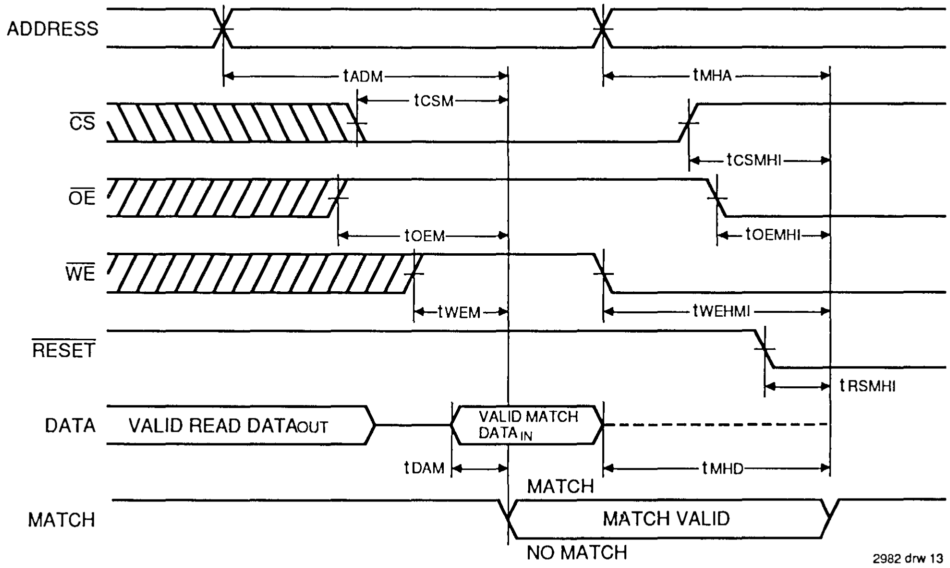
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7174S30[1]		7174S35		7174S45		7174S55[2]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Match Cycle										
tADM	Address to MATCH Valid	—	30	—	35	—	45	—	55	ns
tCSM	Chip Select to MATCH Valid	—	18	—	20	—	25	—	30	ns
tCSMHI	Chip Select to MATCH High	—	18	—	20	—	25	—	30	ns
tDAM	Data Input to MATCH Valid	—	23	—	25	—	35	—	45	ns
tOEMHI	$\overline{OE}$ Low to MATCH Hgih	—	23	—	25	—	35	—	45	ns
tOEM	$\overline{OE}$ High to MATCH Valid	—	23	—	25	—	35	—	45	ns
tWEMHI	$\overline{WE}$ Low to MATCH High	—	23	—	25	—	35	—	45	ns
tWEM	$\overline{WE}$ High to MATCH Valid	—	23	—	25	—	35	—	45	ns
tRSMHI	$\overline{RESET}$ Low to MATCH High	—	23	—	25	—	35	—	45	ns
tMHA	MATCH Valid Hold From Address	5	—	5	—	5	—	5	—	ns
tMHD	MATCH Valid Hold From Data	5	—	5	—	5	—	5	—	ns

NOTES: 2982 tbl 12

1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.

MATCH TIMING[1]



NOTE:

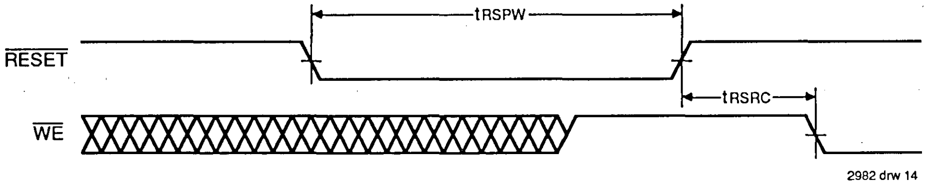
1. It is not recommended to float the data and address inputs of this device while the MATCH pin is active.

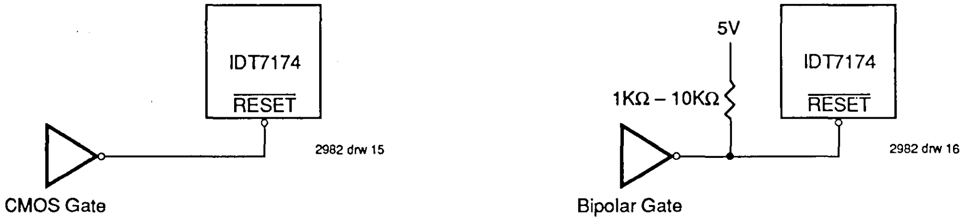
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7174S30(1)		7174S35		7174S45		7174S55(3)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
tRSPW	Reset Pulse Width(2)	55	—	65	—	80	—	100	—	ns
tRSRC	Reset High to $\overline{\text{WE}}$ Low	5	—	5	—	10	—	10	—	ns

NOTES:
1. 0° to +70°C temperature range only.
2. Recommended duty cycle = 10% maximum.
3. -55°C to +125°C temperature range only.

RESET TIMING





Driving the $\overline{\text{RESET}}$ pin with CMOS logic.

Driving the $\overline{\text{RESET}}$ pin with bipolar logic.

Figure 5.

ORDERING INFORMATION

IDT XXXX	X	XX	XX	X
Device Type	Power	Speed	Package	Process/ Temperature Range

Process/Temperature Range	
Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Package	
P	Plastic DIP (600 mil)
TC	THINDIP (300 mil sidebraze)
D	CERDIP (600 mil)
J	Plastic Leaded Chip Carrier
L32	Leadless Chip Carrier
PE	Small Outline IC (300 mil gull-wing)

Speed		
30	Commercial Only	Speed in Nanoseconds
35		
45		
55	Military Only	

Power	
S	Standard Power

Device Type	
7174	64K (8K x 8-Bit) Cache-Tag RAM

2982 drw 17

Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (64K x 1-BIT)

IDT7187S
IDT7187L

FEATURES:

- High speed (equal access and cycle time)
  - Military: 20/25/35/45/55/70/85ns (max.)
  - Commercial: 15/20/25/35ns (max.)
- Low power consumption
  - IDT7187S
    Active: 300mW (typ.)
    Standby: 100µW (typ.)
  - IDT7187L
    Active: 250mW (typ.)
    Standby: 30µW (typ.)
- Battery backup operation—2V data retention (L version only)
- JEDEC standard high-density 22-pin plastic and hermetic DIP, 24-pin plastic SOIC, 22-pin and 28-pin leadless chip carrier and 24-pin CERPACK
- Produced with advanced CEMOS™ high-performance technology
- Separate data input and output
- Input and output directly TTL-compatible
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-86015. Refer to Section 2/page 2-4

DESCRIPTION:

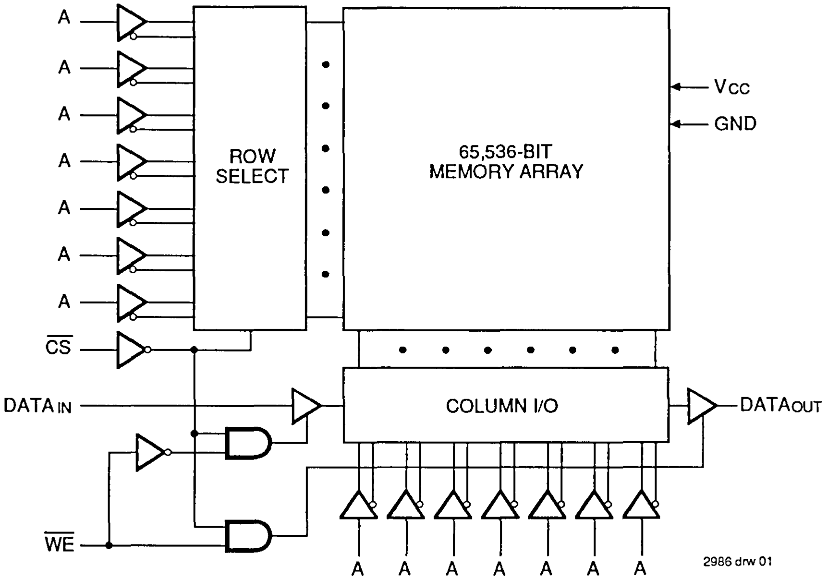
The IDT7187 is a 65,536-bit high-speed static RAM organized as 64K x 1. It is fabricated using IDT's high-performance, high-reliability technology, CEMOS. Access times as fast as 15ns are available with maximum power consumption of 700mW.

Both the standard (S) and low-power (L) versions of the IDT7187 provide two standby modes—ISB and ISB1. ISB provides low-power operation (358mW max.); ISB1 provides ultra-low-power operation (5mW max.). The low-power (L) version also provides the capability for data retention using battery backup. When using a 2V battery, the circuit typically consumes only 30µW.

Ease of system design is achieved by the IDT7187 with full asynchronous operation, along with matching access and cycle times. The device is packaged in an industry standard 22-pin, 300 mil plastic or hermetic DIP, 24-pin plastic SOIC (Gull-Wing and J-Bend), 22- and 28-pin leadless chip carriers, or 24-pin CERPACK.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

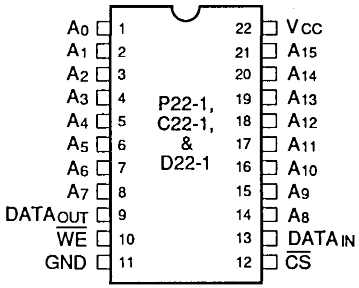
FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

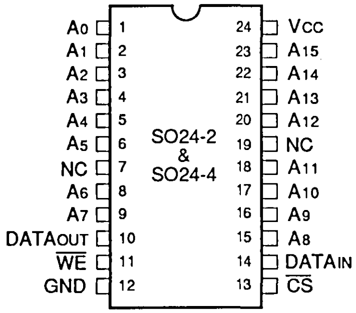
MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1990**

PIN CONFIGURATIONS



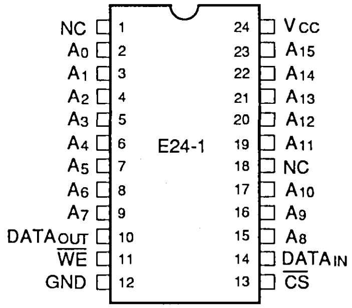
2986 drw 02

DIP
TOP VIEW



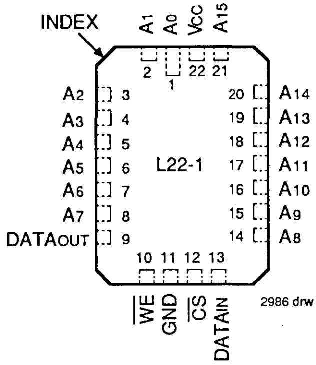
2986 drw 03

SOIC/SOJ
TOP VIEW



2986 drw 04

CERPACK
TOP VIEW



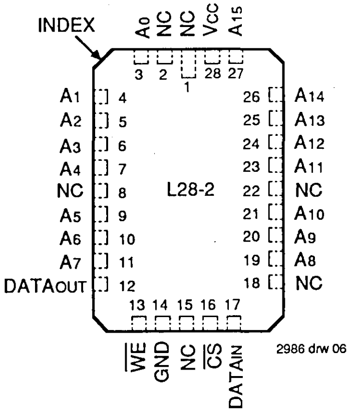
2986 drw 05

22-PIN LCC
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A_0–A_{15}	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power
DATA$_{IN}$	Data Input
DATA$_{OUT}$	Data Output
GND	Ground

2986 tbl 01



2986 drw 06

28-PIN LCC
TOP VIEW

TRUTH TABLE(1)

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High Z	Standby
Read	L	H	D$_{OUT}$	Active

NOTES:

2986 tbl 02

1. H = V_{IH}, L = V_{IL}, X = don't care.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2986 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2986 tbl 04

1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE: 2986 tbl 05

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2986 tbl 06

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT7187S Min.	IDT7187S Max.	IDT7187L Min.	IDT7187L Max.	Unit
$\lvert I_{LI}\rvert$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL. COM'L.	— —	10 5	— —	5 2	µA
$\lvert I_{LO}\rvert$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL. COM'L.	— —	10 5	— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.			0.5	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	
V_{OH}	Output High Voltage	I_{OL} = -4mA, V_{CC} = Min.		2.4	—	2.4	—	V

2986 tbl 07

DC ELECTRICAL CHARACTERISTICS(1)

(VCC = 5V ± 10%, VLC = 0.2V, VHC = VCC - 0.2V)

			7187S15(3)		7187S20 7187L20		7187S25 7187L25		7187S35 7187L35		7187S45 7187L45		7187S55/70 7187L55/70		7187S85 7187L85		
Symbol	**Parameter**	**Power**	**Com'l.**	**Mil.**	**Com'l.**	**Mil.(3)**	**Com'l.**	**Mil.**	**Com'l.**	**Mil.**	**Com'l.**	**Mil.**	**Com'l.**	**Mil.**	**Com'l.**	**Mil.**	**Unit**
ICC1	Operating Power Supply Current $\overline{CS}$ = VIL, Outputs Open VCC = Max., f = 0(2)	S	105	—	90	105	90	105	90	105	—	105	—	105	—	105	mA
		L	—	—	70	85	70	85	70	85	—	85	—	85	—	85	
ICC2	Dynamic Operating Current $\overline{CS}$ = VIL, Outputs Open VCC = Max., f = fMAX(2)	S	140	—	130	140	120	130	110	120	—	120	—	120	—	120	mA
		L	—	—	110	120	100	110	90	100	—	95	—	90	—	90	
ISB	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ VIH, VCC = Max., Outputs Open, f = fMAX(2)	S	65	—	60	65	55	55	45	50	—	50	—	50	—	50	mA
		L	—	—	50	60	45	50	35	40	—	35	—	30/28	—	28	
ISB1	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ VHC, VCC=Max., VIN ≥ VHC or VIN ≤ VLC, f = 0(2)	S	20	—	15	20	15	20	15	20	—	20	—	20	—	20	mA
		L	—	—	0.3	1.5	0.3	1.5	0.3	1.5	—	1.5	—	1.5	—	1.5	

NOTES:

2986 tbl 06

1. All values are maximum guaranteed values.
2. At f = fMAX address and data inputs are cycling at the maximum frequency of read cycles of 1/tRC. f = 0 means no input lines change.
3. These specs are preliminary.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) VHC = VCC - 0.2V, VLC = 0.2V

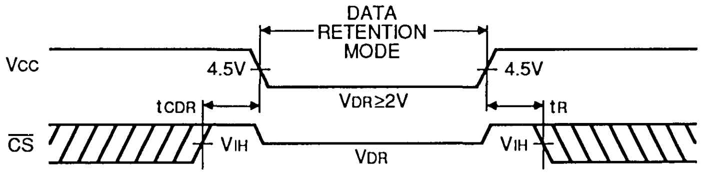
					Typ. (1) Vcc @		Max. Vcc @		
Symbol	**Parameter**	**Test Condition**		**Min.**	**2.0v**	**3.0V**	**2.0V**	**3.0V**	**Unit**
VDR	VCC for Data Retention	—		2.0	—	—	—	—	V
ICCDR	Data Retention Current		MIL. COM'L.	— —	10 10	15 15	600 150	900 225	µA
tCDR(3)	Chip Deselect to Data Retention Time	$\overline{CS}$ ≥ VHC VIN ≥ VHC or ≤ VLC		0	—	—	—	—	ns
tR(3)	Operation Recovery Time			tRC(2)	—	—	—	—	ns
|ILI|(3)	Input Leakage Current			—	—	—	2	2	µA

NOTES:

2986 tbl 09

1. TA = +25°C.
2. tRC = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

LOW VCC DATA RETENTION WAVEFORM



2986 drw 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2986 tbl 10

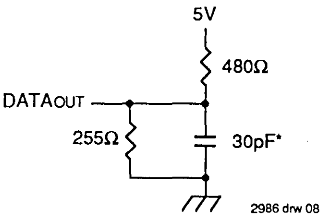


Figure 1. Output Load

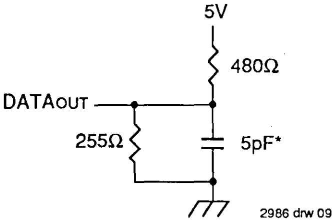


Figure 2. Output Load
(for tHZ, tLZ, tWZ and tOW)

*Includes scope and jig capacitances

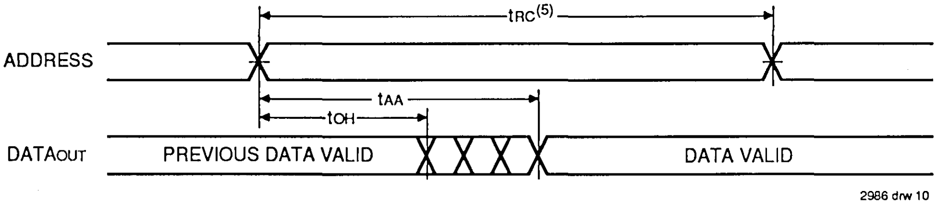
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7187S15[1]/20 7187L20		7187S25 7187L25		7187S35/45[2] 7187L35/45[2]		7187S55[2] 7187L55[2]		7187S70[2] 7187L70[2]		7187S85[2] 7187L85[2]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle														
tRC	Read Cycle Time	15/20	—	25	—	35/45	—	55	—	70	—	85	—	ns
tAA	Address Access Time	—	15/20	—	25	—	35/45	—	55	—	70	—	85	ns
tACS	Chip Select Access Time	—	15/20	—	25	—	35/45	—	55	—	70	—	85	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
tLZ	Output Selection to Output in Low Z[3]	5	—	5	—	5	—	5	—	5	—	5	—	ns
tHZ	Chip Deselect to Output in High Z[3]	—	6	—	12	—	17/20	—	30	—	30	—	40	ns
tPU	Chip Select to Power Up Time[3]	0	—	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Deselect to Power Down Time[3]	—	15/20	—	20	—	30/35	—	35	—	35	—	40	ns

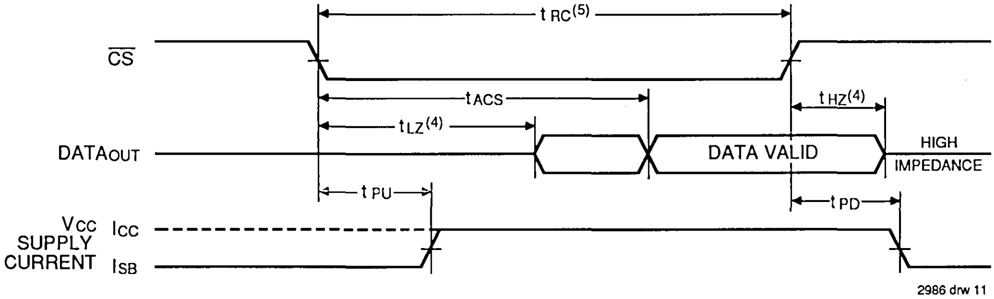
2986 tbl 11

NOTES:
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1[1,2]



TIMING WAVEFORM OF READ CYCLE NO. 2[1,3]



NOTES:
1. $\overline{\text{WE}}$ is high for read cycle.
2. $\overline{\text{CS}}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{\text{CS}}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

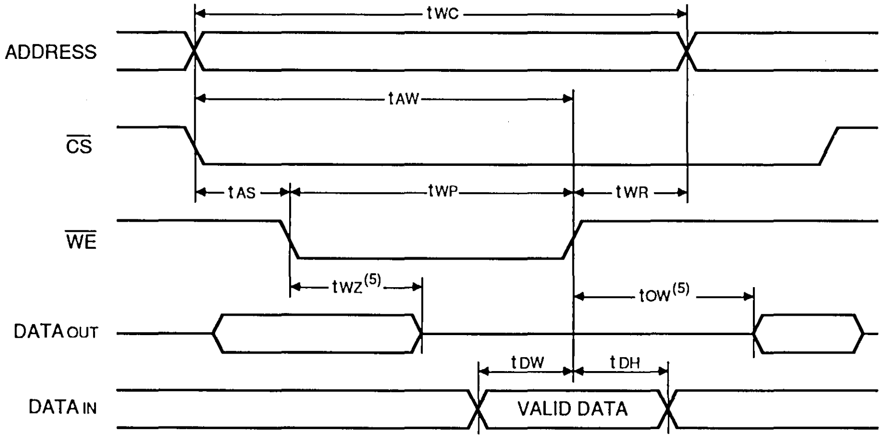
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7187S15(1)/20 7187L20		7187S25 7187L25		7187S35/45(2) 7187L35/45(2)		7187S55(2) 7187L55(2)		7187S70(2) 7187L70(2)		7187S85(2) 7187L85(2)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle														
tWC	Write Cycle Time	12/15	—	25	—	35/45	—	55	—	70	—	85	—	ns
tCW	Chip Select to End of Write	12/15	—	20	—	25/40	—	50	—	55	—	65	—	ns
tAW	Address Valid to End of Write	12/15	—	20	—	25/40	—	50	—	55	—	65	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	12/15	—	20	—	20/25	—	35	—	40	—	45	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	8/10	—	15	—	15/25	—	25	—	30	—	35	—	ns
tDH	Data Hold Time	0	—	5	—	5	—	5	—	5	—	5	—	ns
tWZ	Write Enable to Output in High Z(3)	—	6/8	—	12	—	15/30	—	30	—	30	—	40	ns
tOW	Output Active from End of Write(3)	0	—	0	—	0	—	0	—	0	—	0	—	ns

2986 tbl 12

NOTES:
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

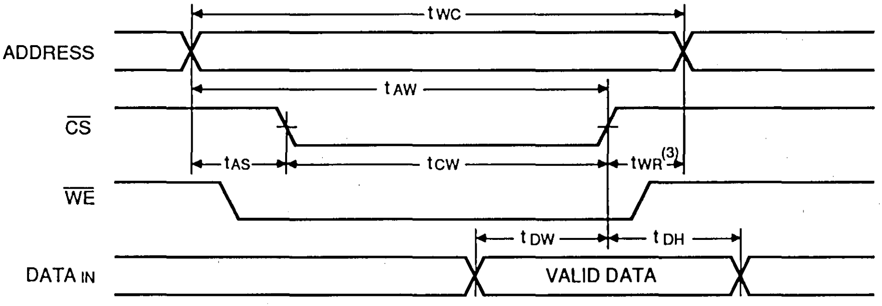
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1,2,3,4)



2986 drw 12

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
5. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1,2,4,5)

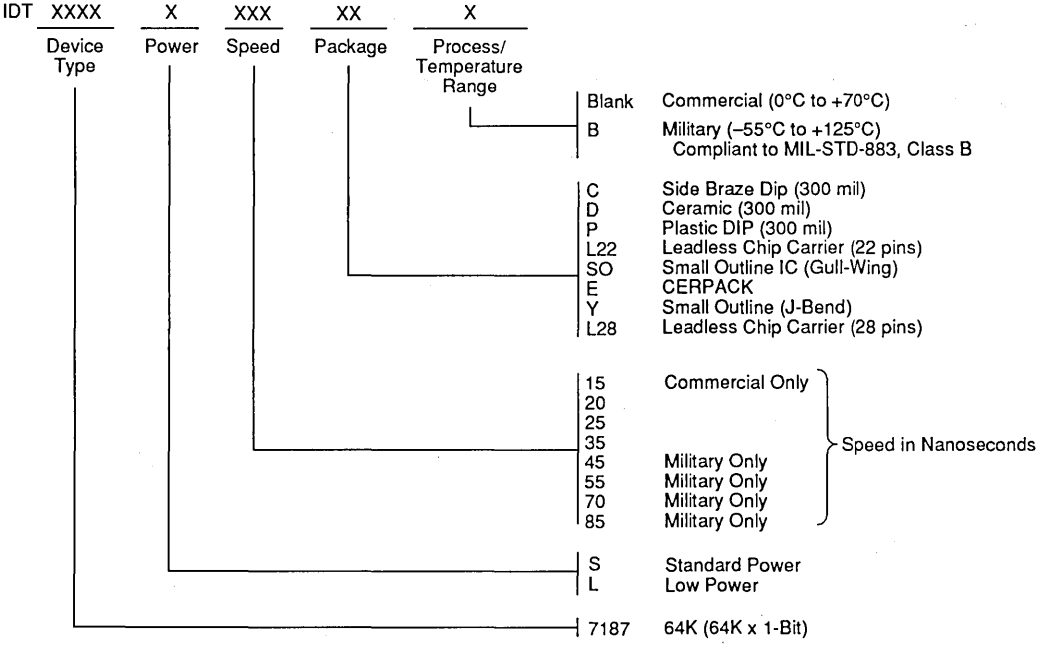


2986 drw 13

NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
5. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).

ORDERING INFORMATION



Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

C	Side Braze Dip (300 mil)
D	Ceramic (300 mil)
P	Plastic DIP (300 mil)
L22	Leadless Chip Carrier (22 pins)
SO	Small Outline IC (Gull-Wing)
E	CERPACK
Y	Small Outline (J-Bend)
L28	Leadless Chip Carrier (28 pins)

15	Commercial Only
20	
25	
35	
45	Military Only
55	Military Only
70	Military Only
85	Military Only

S	Standard Power
L	Low Power

7187	64K (64K x 1-Bit)

2986 drw 14

Integrated Device Technology, Inc.

CMOS STATIC RAM
64K (16K x 4-BIT)

IDT7188S
IDT7188L

FEATURES:

- High-speed (equal access and cycle times)
  - Military: 20/25/35/45/55/70/85ns (max.)
  - Commercial: 15/20/25/35ns (max.)
- Low power consumption
  - IDT7188S
    Active: 350mW (typ.)
    Standby: 100μW (typ.)
  - IDT7188L
    Active: 300mW (typ.)
    Standby: 30μW (typ.)
- Battery backup operation — 2V data retention (L version only)
- Available in high-density industry standard 22-pin, 300 mil ceramic and plastic DIP, 24-pin SOIC, 24-pin CERPACK
- Produced with advanced CEMOS™ technology
- Single 5V (+ 10%) power supply
- Inputs/outputs TTL-compatible
- Military product compliant to MIL-STD-883, Class B

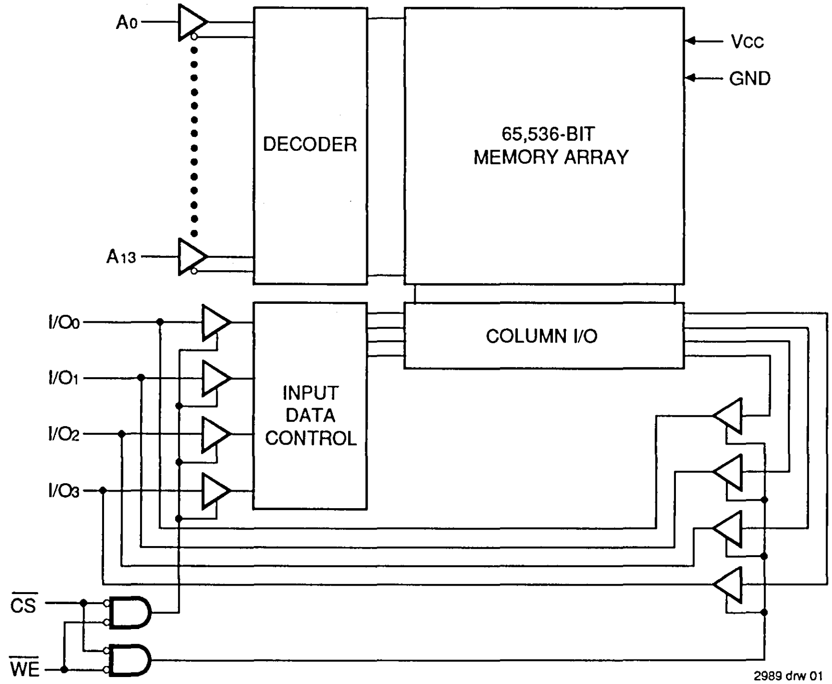
DESCRIPTION:

The IDT7188 is a 65,536-bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-performance, high-reliability technology — CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for memory intensive applications.

Access times as fast as 15ns are available, with typical power consumption of only 300mW. The IDT7188 offers a reduced power standby mode, I_{SB1}, which enables the designer to greatly reduce device power requirements. This capability significantly decreases system power and cooling levels, while greatly enhancing system reliability. The low-power version (L) version also offers a battery backup data retention capability where the circuit typically consumes only 30μW operating from a 2V battery.

All inputs and outputs are TTL-compatible and operate from a single 5V supply. The IDT7188 is packaged in 22-pin, 300 mil ceramic and plastic DIPs, 24-pin SOICs, (gull-wing and J-bend) and CERPACKs, providing excellent board-level packing densities.

FUNCTIONAL BLOCK DIAGRAM



2989 drw 01

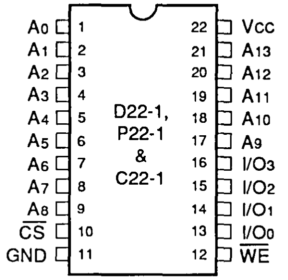
CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1990**

DESCRIPTION (Continued)

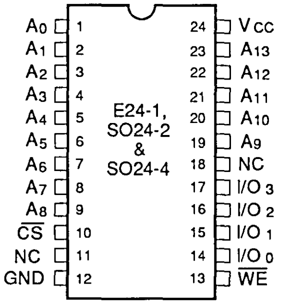
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS



2989 drw 02

DIP
TOP VIEW



2989 drw 03

CERPACK/SOIC/SOJ
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A0–A13	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
I/O0-3	Data Input/Output
Vcc	Power
GND	Ground

2989 tbl 01

TRUTH TABLE[1]

Mode	$\overline{CS}$	$\overline{WE}$	I/O	Power
Standby	H	X	High Z	Standby
Read	L	H	DOUT	Active
Write	L	L	DIN	Active

NOTE: 2989 tbl 02

1. H = V_{IH}, L = V_{IL}, X = don't care.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2989 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz, Vcc = 0v))

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	6	pF

NOTE: 2989 tbl 04

1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2989 tbl 05

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2989 tbl 06

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Condition		IDT7188S Min.	IDT7188S Max.	IDT7188L Min.	IDT7188L Max.	Unit
$\lvert I_{LI} \rvert$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL. COM'L.	— —	10 5	— —	5 2	µA
$\lvert I_{LO} \rvert$	Output Leakage Current	V_{CC} = Max., $\overline{CS} = V_{IH}$, V_{OUT} = GND to V_{CC}	MIL. COM'L.	— —	10 5	— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.			0.5	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	
V_{OH}	Output High Voltage	I_{OL} = -4mA, V_{CC} = Min.		2.4	—	2.4	—	V

2989 tbl 07

DC ELECTRICAL CHARACTERISTICS[1]

($V_{CC} = 5V \pm 10\%$, $V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$)

Symbol	Parameter	Power	7188S15 7188L15		7188S20 7188L20		7188S25 7188L25		7188S35 7188L35		7188S45 7188L45		7188S55/70 7188L55/70		7188S85 7188L85		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current $\overline{CS} = V_{IL}$, Outputs Open V_{CC} = Max., f = 0[2]	S	90	—	110	110	100	105	100	110	—	110	—	110	—	110	mA
		L	75	—	70	80	70	80	85	95	—	95	—	95	—	95	
I_{CC2}	Dynamic Operating Current $\overline{CS} = V_{IL}$, Outputs Open V_{CC} = Max., f = f_{MAX}[2]	S	135	—	130	160	135	155	125	140	—	140	—	140	—	140	mA
		L	125	—	115	130	105	120	105	115	—	110	—	110	—	105	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}[2]	S	60	—	55	70	55	60	45	50	—	50	—	50	—	50	mA
		L	45	—	40	50	35	40	35	40	—	35	—	35	—	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, V_{CC}=Max., $V_{IN} \geq V_{HC}$ or $V_{IN} \leq V_{LC}$, f = 0[2]	S	20	—	15	25	15	20	15	20	—	20	—	20	—	20	mA
		L	1.5	—	0.5	1.5	0.5	1.5	0.5	1.5	—	1.5	—	1.5	—	1.5	

NOTES:

2989 tbl 06

1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

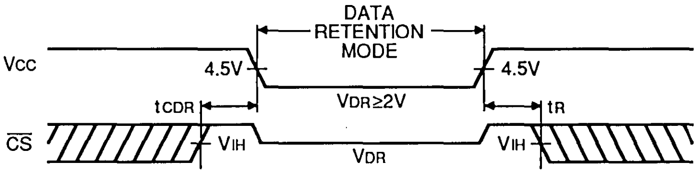
(L Version Only) $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Condition		Min.	Typ.[1] Vcc @		Max. Vcc @		Unit
					2.0v	3.0V	2.0V	3.0V	
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	—	10	15	600	900	µA
			COM'L.	—	10	15	150	225	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	—	—	ns
$\lvert I_{LI} \rvert$[3]	Input Leakage Current			—	—	—	2	2	µA

2989 tbl 09

NOTES:
1. $T_A = +25°C$.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

LOW Vcc DATA RETENTION WAVEFORM



2989 drw 04

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2989 tbl 10

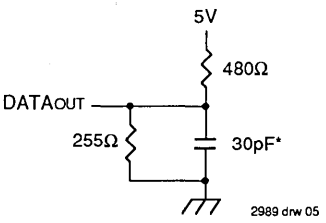


Figure 1. Output Load

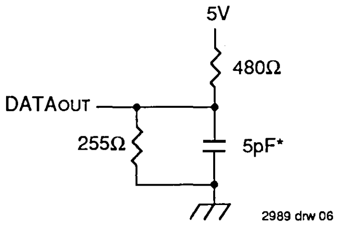


Figure 2. Output Load
(for t_{HZ}, t_{LZ}, t_{WZ}, t_{OHZ} and t_{OW})

*Includes scope and jig capacitances

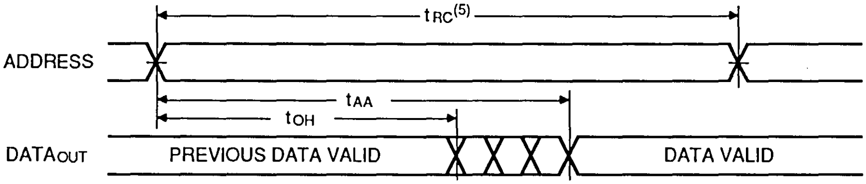
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7188S15[1] 7188L15[1]		7188S20 7188L20		7188S25 7188L25		7188S35/45 7188L35/45		7188S55/70[2] 7188L55/70[2]		7188S85[2] 7188L85[2]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle														
tRC	Read Cycle Time	15	—	20	—	25	—	35/45	—	55/70	—	85	—	ns
tAA	Address Access Time	—	15	—	20	—	25	—	35/45	—	55/70	—	85	ns
tACS	Chip Select Access Time	—	15	—	20	—	25	—	35/45	—	55/70	—	85	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
tLZ	Output Selection to Output in Low Z[3]	5	—	5	—	5	—	5	—	5	—	5	—	ns
tHZ	Chip Deselect to Output in High Z[3]	—	7	—	8	—	10	—	14	—	20/25	—	30	ns
tPU	Chip Select to Power Up Time[3]	0	—	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Deselect to Power Down Time[3]	—	15	—	20	—	25	—	35/45	—	55/70	—	85	ns

2989 tbl 11

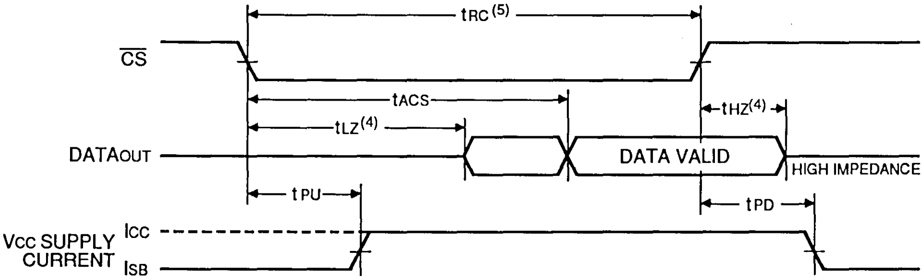
NOTES:
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1, 2)



2989 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 3)



2971 drw 08

NOTES:
1. WE is high for read cycle.
2. CS is low for READ cycle.
3. Address valid prior to or coincident with CS transition low.
4. Transition is measured ±200mV from steady state voltage.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

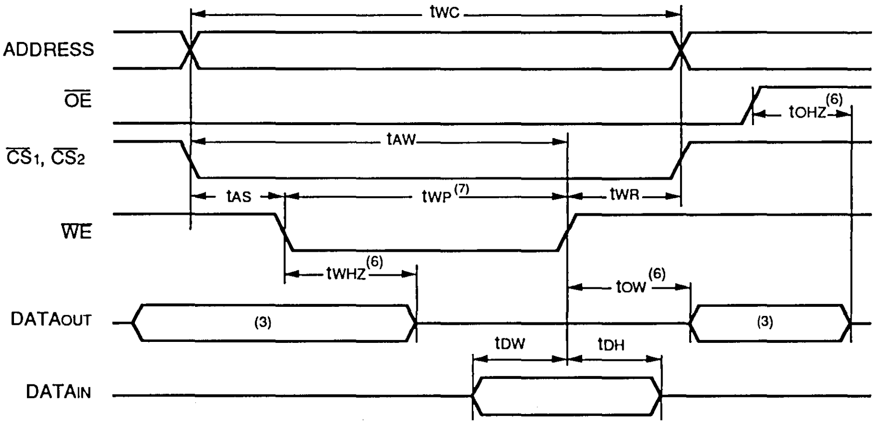
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

		7188S15(1) 7188L15(1)		7188S20 7188L20		7188S25 7188L25		7188S35/45(2) 7188L35/45(2)		7188S55/70(2) 7188L55/70(2)		7188S85(2) 7188L85(2)		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
Write Cycle														
t_{WC}	Write Cycle Time	14	—	17	—	20	—	30/40	—	50/60	—	75	—	ns
t_{CW}	Chip Select to End of Write	14	—	17	—	20	—	25/35	—	50/60	—	75	—	ns
t_{AW}	Address Valid to End of Write	14	—	17	—	20	—	25/35	—	50/60	—	75	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	14	—	17	—	20	—	25/35	—	50/60	—	75	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	10	—	10	—	13	—	15/20	—	25/30	—	35	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High Z(3)	—	5	—	6	—	7	—	10/15	—	25/30	—	40	ns
t_{OW}	Output Active from End of Write(3)	5	—	5	—	5	—	5	—	5	—	5	—	ns

NOTES:
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

2989 tbl 12

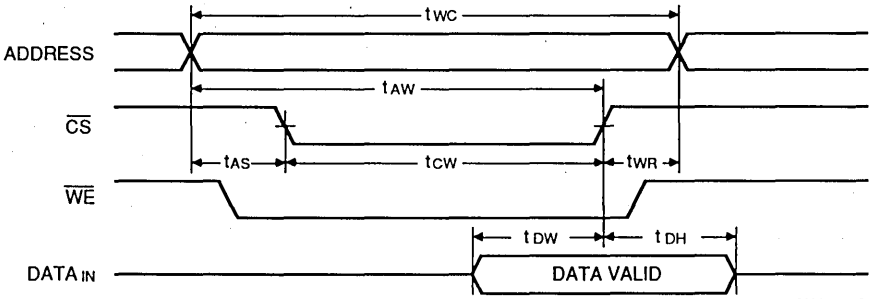
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2 ,3)



2999 drw 06

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals should not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)$^{(1,2,3,5)}$



2989 drw 10

NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals should not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200mV from steady state.

ORDERING INFORMATION

IDT	XXXX	X	XX	XX	X
	Device Type	Power	Speed	Package	Process/ Temperature Range

Process/Temperature Range:

Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Package:

C	Sidebraze DIP
D	Ceramic DIP
P	Plastic DIP
SO	Small Outline IC (Gull Wing)
Y	Small Outline IC (J-Bend)
E	CERPACK

Speed in Nanoseconds:

15	Commercial Only
20	
25	
35	
45	Military Only
55	Military Only
70	Military Only
85	Military Only

Power:

S	Standard Power
L	Low Power

Device Type:

7188	64K (16K x 4-Bit)

2989 drw 11

Integrated Device Technology, Inc.

CMOS STATIC RAMS 64K (16K x 4-BIT)
Added Chip Select and Output Controls

IDT7198S
IDT7198L

FEATURES:

- Optimized for fast RISC processors, including IDT79R3000
- Fast Output Enable ($\overline{OE}$) pin available for added system flexibility
- Multiple Chip Selects ($\overline{CS}_1$, $\overline{CS}_2$) simplify system design and operation
- High speed (equal access and cycle times)
  - — Military: 20/25/35/45/55/70/85ns (max.)
  - — Commercial: 15/20/25/35ns (max.)
- Low power consumption
  - — IDT7198S
    Active: 350mW (typ.)
    Standby: 100μw (typ.)
  - — IDT7198L
    Active: 300mW (typ.)
    Standby: 30μw (typ.)
- Battery back-up operation—2V data retention (L version only)
- 24-pin CERDIP, 24-pin plastic DIP, high-density 28-pin leadless chip carrier, 24-pin SOIC, SOJ and CERPACK
- Produced with advanced CEMOS™ technology
- Bidirectional data inputs and outputs
- Inputs/outputs TTL-compatible
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-86859. Refer to Section 2/page 2-4

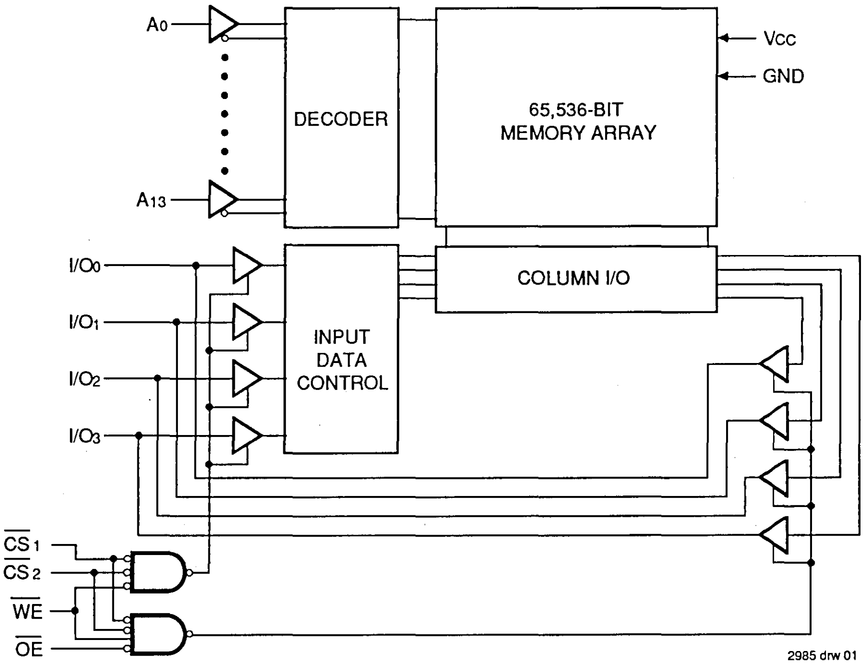
DESCRIPTION:

The IDT7198 is a 65,536 bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for memory intensive applications. Timing parameters have been specified to meet the speed demands of the IDT79R3000 RISC processors.

The IDT7198 features three memory control functions: Chip Select 1 ($\overline{CS}_1$), Chip Select 2 ($\overline{CS}_2$) and Output Enable ($\overline{OE}$). These three functions greatly enhance the IDT7198's overall flexibility in high-speed memory applications.

Access times as fast as 15ns are available, with typical power consumption of only 300mW. The IDT7198 offers a reduced power standby mode, I_{SB1}, which enables the designer to considerably reduce device power requirements.

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION: (Continued)

This capability significantly decreases system power and cooling levels, while greatly enhancing system reliability. The low-power version (L)also offers a battery backup data retention capability where the circuit typically consumes only 30µW when operating from a 2V battery.

All inputs and outputs are TTL-compatible and operate from a single 5 volt supply.

The IDT7198 is packaged in either a 24-pin ceramic DIP, 24-pin plastic DIP, 28-pin leadless chip carrier, 24-pin SOIC (Gull-Wing and J-Bend) and 24-pin CERPACK.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

MEMORY CONTROL

The IDT7198 64K high-speed CEMOS static RAM incorporates two additional memory control features (an extra chip select and an output enable pin) which offer additional benefits in many system memory applications.

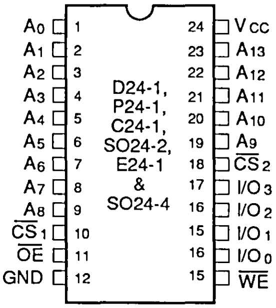
The dual chip select feature ($\overline{\text{CS}}_1$, $\overline{\text{CS}}_2$) now brings the convenience of improved system speeds to the large memory designer by reducing the external logic required to perform decoding. Since external decoding logic is reduced, board space is saved, system speed is enhanced and system reliability improves as a result of lower parts count.

Both chip selects, Chip Select 1 ($\overline{\text{CS}}_1$) and Chip Select 2 ($\overline{\text{CS}}_2$), must be in the active-low state to select the memory. If either chip select is pulled high, the memory will be deselected and remain in the standby mode.

The fast output enable function ($\overline{\text{OE}}$) is also a highly desirable feature of the IDT7198 high-speed common I/O static RAM. This function is designed to eliminate problems associated with data bus contention by allowing the data outputs to be controlled independent of either chip select. Its speed permits further decreases in overall read cycle timing.

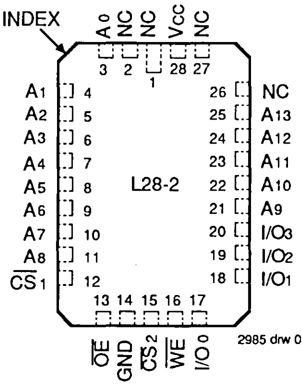
These added memory control features provide improved system design flexibility, along with overall system speed performance enhancements.

PIN CONFIGURATIONS



2985 drw 02

DIP/SOIC/SOJ/CERPACK
TOP VIEW



2985 drw 03

LCC
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A0–A13	Address Inputs
$\overline{\text{CS}}_1$	Chip Select 1
$\overline{\text{CS}}_2$	Chip Select 2
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
I/O0–I/O3	Data I/O
Vcc	Power
GND	Ground

2985 tbl 01

TRUTH TABLE[1]

Mode	$\overline{\text{CS}}_1$	$\overline{\text{CS}}_2$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	I/O	Power
Standby	H	X	X	X	High Z	Standby
Standby	X	H	X	X	High Z	Standby
Read	L	L	H	L	DOUT	Active
Write	L	L	L	X	DIN	Active
Read	L	L	H	H	High Z	Active

NOTE: 2985 tbl 02

1. H = VIH, L = VIL, X = don't care.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2985 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz, V_{CC} = 0V)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 2985 tbl 04

1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2985 tbl 05

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2985 tbl 06

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT7198S		IDT7198L		Unit
				Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL. COM'L.	— —	10 5	— —	5 2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL. COM'L.	— —	10 5	— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.			0.5	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	
V_{OH}	Output High Voltage	I_{OL} = -4mA, V_{CC} = Min.		2.4	—	2.4	—	V

2985 tbl 07

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	7198S15 7198L15		7198S20 7198L20		7198S25 7198L25		7198S35 7198L35		7198S45 7198L45		7198S55/70 7198L55/70		7198S85 7198L85		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = $0^{(2)}$	S	90	—	110	110	100	105	100	110	—	110	—	110	—	110	mA
		L	75	—	70	80	70	80	85	95	—	95	—	95	—	95	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = $f_{MAX}^{(2)}$	S	135	—	130	160	135	155	125	140	—	140	—	140	—	140	mA
		L	125	—	115	130	100	120	105	115	—	110	—	110	—	105	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = $f_{MAX}^{(2)}$	S	60	—	55	70	55	60	45	50	—	50	—	50	—	50	mA
		L	45	—	40	50	35	40	35	40	—	35	—	35	—	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC}= Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = $0^{(2)}$	S	20	—	15	25	15	20	15	20	—	20	—	20	—	20	mA
		L	1.5	—	0.5	1.5	0.5	1.5	0.5	1.5	—	1.5	—	1.5	—	1.5	

NOTES: 2985 tbl 06

1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

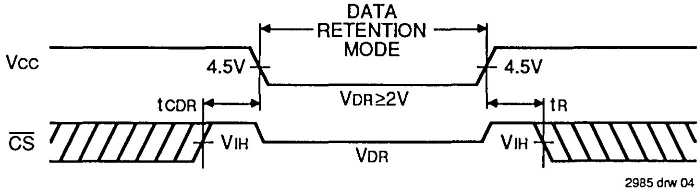
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.[1] Vcc @ 2.0v	Typ.[1] Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	Vcc for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS}_1$ or $\overline{CS}_2$ ≥ V_{HC} V_{IN} ≥ V_{HC} or ≤ V_{LC}	MIL.	—	10	15	600	900	µA
			COM'L.	—	10	15	150	225	
$t_{CDR}^{(3)}$	Chip Deselect to Data Retention Time			0	—	—	—	—	ns
$t_R^{(3)}$	Operation Recovery Time			$t_{RC}^{(2)}$	—	—	—	—	ns
$\|I_{LI}\|^{(3)}$	Input Leakage Current			—	—	—	2	2	µA

NOTES: 2985 tbl 09

1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

LOW Vcc DATA RETENTION WAVEFORM



2985 drw 04

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2985 tbl 10

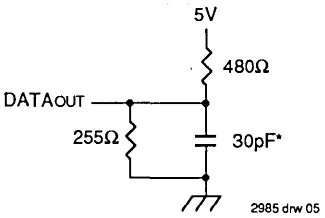


Figure 1. Output Load

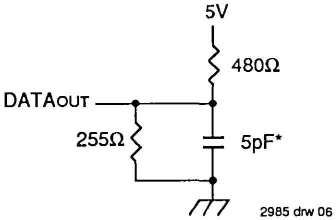


Figure 2. Output Load
(for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW} and t_{WHZ})

*Includes scope and jig capacitances

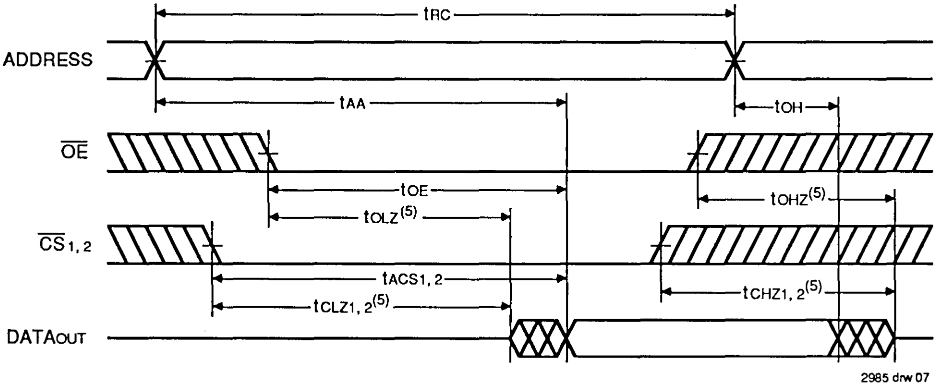
AC ELECTRICAL CHARACTERISTICS (VCC = 5.0V ± 10%, All Temperature Ranges)

		7198S15(1)/20 7198L15(1)/20		7198S25 7198L25		7198S35/45(2) 7198L35/45(2)		7198S55(2) 7198L55(2)		7198S70(2) 7198L70(2)		7198S85(2) 7198L85(2)		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle														
t_{RC}	Read Cycle Time	15/20	—	25	—	35/45	—	55	—	70	—	85	—	ns
t_{AA}	Address Access Time	—	15/19	—	25	—	35/45	—	55	—	70	—	85	ns
$t_{ACS1,2}$	Chip Select-1,2 Access Time(3)	—	15/20	—	25	—	35/45	—	55	—	70	—	85	ns
$t_{CLZ1,2}$	Chip Select-1,2 to Output in Low Z(4)	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	8/9	—	11	—	20/25	—	35	—	45	—	55	ns
t_{OLZ}	Output Enable to Output in Low Z(4)	5	—	5	—	5	—	5	—	5	—	5	—	ns
$t_{CHZ1,2}$	Chip Select 1,2 to Output in High Z(4)	—	7/8	—	10	—	14	—	20	—	25	—	30	ns
t_{OHZ}	Output Disable to Output in High Z(4)	—	7/8	—	9	—	15	—	20	—	25	—	30	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}	Chip Select to Power Up Time(4)	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Deselect to Power Down Time(4)	—	15/20	—	25	—	35/45	—	55	—	70	—	85	ns

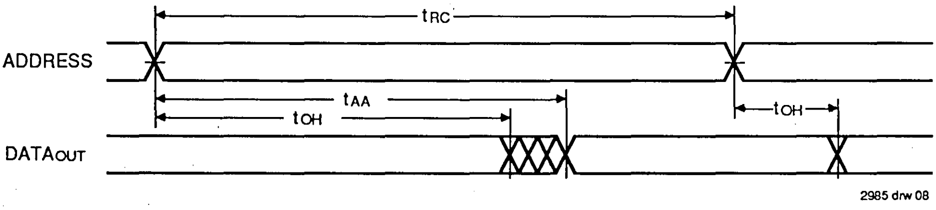
2985 tbl 11

NOTES:
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Both chip selects must be active low for the device to be selected.
4. This parameter guaranteed but not tested.

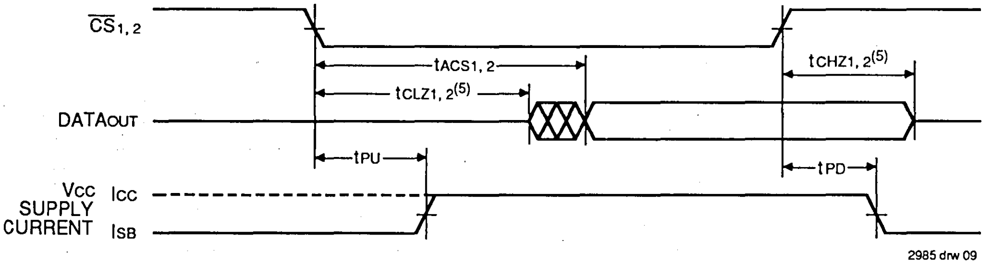
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



NOTES:

1. $\overline{WE}$ is high for READ cycle.
2. Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $\overline{CS}_2 = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}_1$ and or $\overline{CS}_2$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ±200mV from steady state voltage.

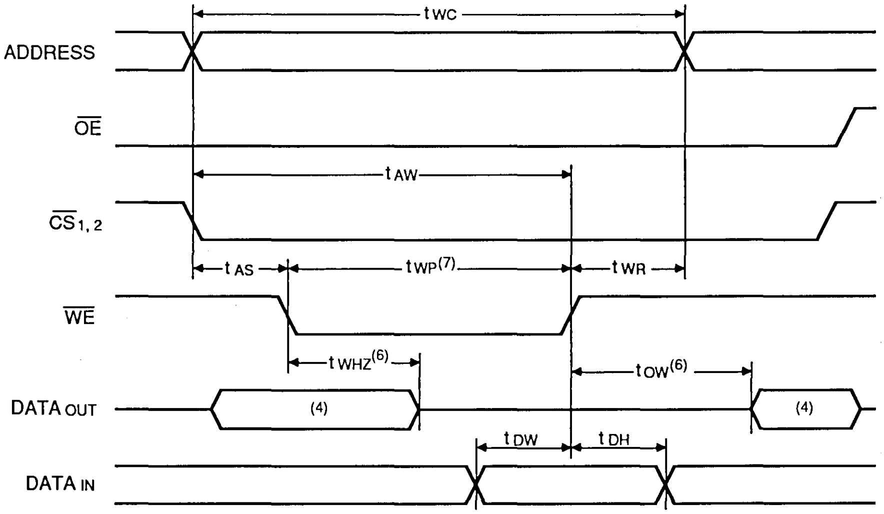
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7198S15(1)/20 7198L15(1)/20		7198S25 7198L25		7198S35/45(2) 7198L35/45(2)		7198S55(2) 7198L55(2)		7198S70(2) 7198L70(2)		7198S85(2) 7198L85(2)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle														
t_{WC}	Write Cycle Time	14/17	—	20	—	30/40	—	50	—	60	—	75	—	ns
$t_{CW1,2}$	Chip Select to End of Write()	14/17	—	20	—	25/35	—	50	—	60	—	75	—	ns
t_{AW}	Address Valid to End of Write	14/17	—	20	—	25/35	—	50	—	60	—	75	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	14/17	—	20	—	25/35	—	50	—	60	—	75	—	ns
$t_{WR1,2}$	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}	Write Enable to Output in High Z(4)	—	5/6	—	7	—	10/15	—	25	—	30	—	40	ns
t_{DW}	Data Valid to End of Write	10	—	13	—	15/20	—	25	—	30	—	35	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{OW}	Output Active from End of Write(4)	5	—	5	—	5	—	5	—	5	—	5	—	ns

2985 tbl 12

NOTES:
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Both chip selects must be active low for the device to be selected.
4. This parameter guaranteed but not tested.

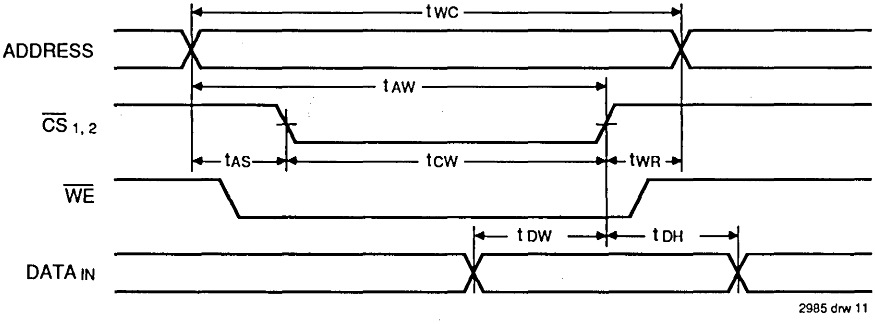
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



2985 drw 10

NOTES:
1. $\overline{WE}$, $\overline{CS}_1$ or $\overline{CS}_2$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{WE}$, a low $\overline{CS}_1$ and a low $\overline{CS}_2$.
3. t_{WR} is measured from the earlier of $\overline{CS}_1$, $\overline{CS}_2$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, outputs remain in the high impedance state.
6. Transition is measured ±200mV from steady state.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
8. $\overline{OE}$ = V_{IH}.

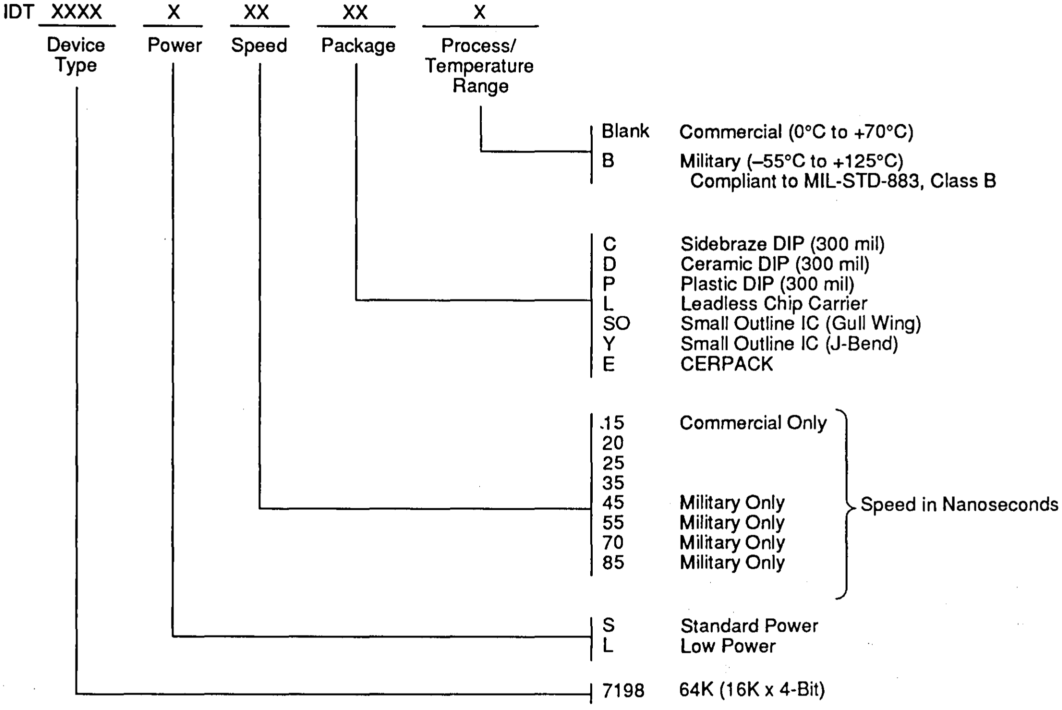
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 5)



NOTES:

1. $\overline{WE}$, $\overline{CS}_1$ or $\overline{CS}_2$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{WE}$, a low $\overline{CS}_1$ and a low $\overline{CS}_2$.
3. t_{WR} is measured from the earlier of $\overline{CS}_1$, $\overline{CS}_2$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, outputs remain in the high impedance state.
6. Transition is measured ±200mV from steady state.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
8. $\overline{OE}$ = V_{IH}.

ORDERING INFORMATION



IDT XXXX X XX XX X

Device Type / Power / Speed / Package / Process/Temperature Range

Process/Temperature Range:

Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Package:

C	Sidebraze DIP (300 mil)
D	Ceramic DIP (300 mil)
P	Plastic DIP (300 mil)
L	Leadless Chip Carrier
SO	Small Outline IC (Gull Wing)
Y	Small Outline IC (J-Bend)
E	CERPACK

Speed (Speed in Nanoseconds):

15	Commercial Only
20	
25	
35	
45	Military Only
55	Military Only
70	Military Only
85	Military Only

Power:

S	Standard Power
L	Low Power

Device Type:

7198	64K (16K x 4-Bit)

2986 drw 12

Integrated Device Technology, Inc.

CMOS STATIC RAMS
64K (16K x 4-BIT)
Separate Data Inputs and Outputs

IDT71981S/L
IDT71982S/L

FEATURES:

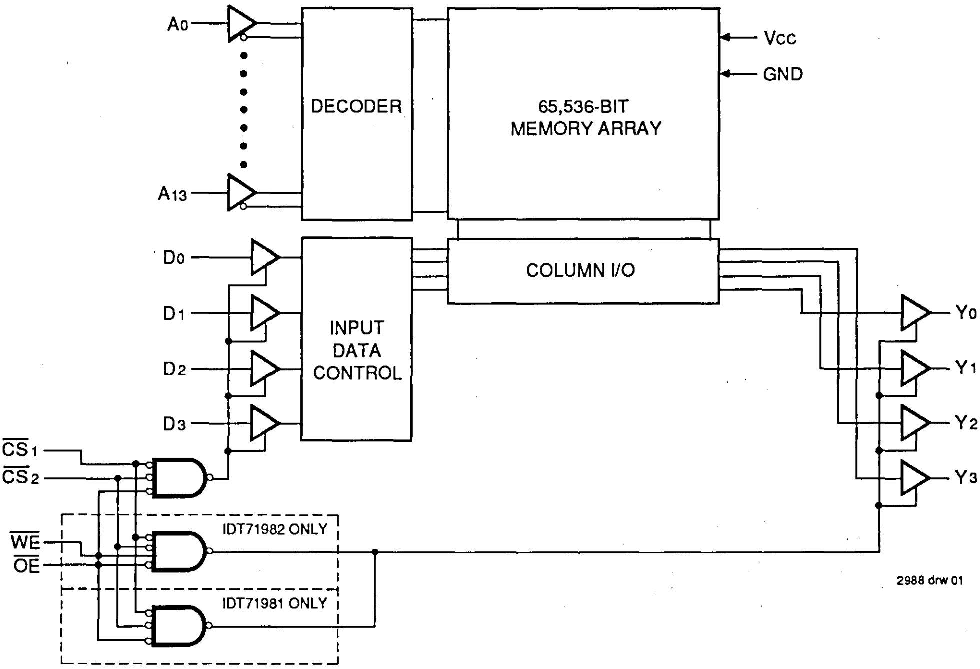
- Optimized for fast RISC processors including the IDT79R3000
- Separate data inputs and outputs
- IDT71981S/L: outputs track inputs during write mode
- IDT71982S/L: high impedance outputs during write mode
- High speed (equal access and cycle time)
  - — Military: 20/25/35/45/55/70/85ns (max.)
  - — Commercial: 15/20/25/35ns (max.)
- Low power consumption
  - — IDT71981/2S
    Active: 350mW (typ.)
    Standby: 100µw (typ.)
  - — IDT71981/2L
    Active: 300mW (typ.)
    Standby: 30µW (typ.)
- Battery backup operation—2V data retention (L version only)
- High-density 28-pin hermetic and plastic DIP, 28-pin leadless chip carrier, 28-pin SOIC
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71981/IDT71982 are 65,536-bit high-speed static RAMs organized as 16K x 4. They are fabricated using IDT's high-performance, high-reliability technology—CEMOS. Timing parameters have been specified to meet the speed demands of the IDT79R3000 RISC processors.

Access times as fast as 15ns are available with typical power consumption of only 300mW. These circuits also offer a reduced power standby mode (I_{SB}). When $\overline{CS}_1$ or $\overline{CS}_2$ goes high, the circuit will automatically go to, and remain in, this standby mode. In the ultra-low-power standby mode (I_{SB1}), the devices consume less than 2.5mW, typically. This capability provides significant system-level power and cooling savings. The low-power (L) versions also offer a battery backup data retention capability where the circuit typically consumes only 30µW operating off a 2V battery.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

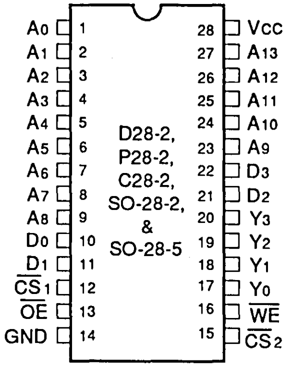
DESCRIPTION: (Continued)

All inputs and outputs of the IDT71981/1D171982 are TTL-compatible and operate from a single 5V supply.

The IDT71981/IDT71982 are packaged in either a 28-pin, 300 mil hermetic DIP, 28-pin 300 mil plastic DIP, 28-pin SOIC (Gull Wing and J-Bend), or 28-pin leadless chip carrier.

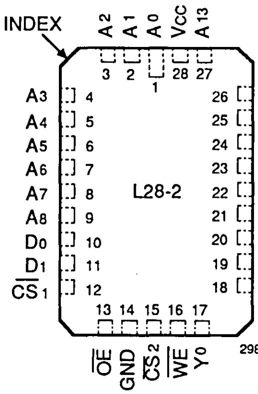
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS



2988 drw 02

DIP/SOIC/SOJ
TOP VIEW



2988 drw 03

LCC
TOP VIEW

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 2988 tbl 04

1. This parameter is determined by device characterization, but is not production tested.

PIN DESCRIPTIONS

Name	Description
A0–A13	Address Inputs
$\overline{CS}_1$, $\overline{CS}_2$	Chip Selects
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
D0–D3	DATA$_{IN}$
Y0–Y3	DATA$_{OUT}$
VCC	Power
GND	Ground

2988 tbl 01

TRUTH TABLE(3)

Mode	$\overline{CS}_1$	$\overline{CS}_2$	$\overline{WE}$	$\overline{OE}$	Output	Power
Standby	H	X	X	X	High Z	Standby
Standby	X	H	X	X	High Z	Standby
Read	L	L	H	L	D_{OUT}	Active
Write(1)	L	L	L	L	D_{IN}	Active
Write(1)	L	L	L	H	High Z	Active
Write(2)	L	L	L	X	High Z	Active
Read	L	L	H	H	High Z	Active

NOTES: 2988 tbl 02

1. For IDT71981 only.
2. For IDT71982 only.
3. H = V_{IH}, L = V_{IL}, X = don't care.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2988 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2988 tbl 05

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2988 tbl 06

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT71981/2S Min.	IDT71981/2S Max.	IDT71981/2L Min.	IDT71981/2L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL. COM'L.	— —	10 5	— —	5 2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}_{1,2}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL. COM'L.	— —	10 5	— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.			0.5	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	
V_{OH}	Output High Voltage	I_{OL} = -4mA, V_{CC} = Min.		2.4	—	2.4	—	V

2988 tbl 07

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

			71981/2S15 71981/2L15		71981/2S20 71981/2L20		71981/2S25 71981/2L25		71981/2S35 71981/2L35		71981/2S45 71981/2L45		71981/2S55/70 71981/2L55/70		71981/2S85 71981/2L85		
Symbol	Parameter	Power	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS}_{1,2}$ = V_{IL}, Outputs Open V_{CC} = Max., f = 0[2]	S	90	—	110	110	100	125	100	110	—	110	—	110	—	110	mA
		L	75	—	70	80	85	110	85	95	—	95	—	95	—	95	
I_{CC2}	Dynamic Operating Current $\overline{CS}_{1,2}$ = V_{IL}, Outputs Open V_{CC} = Max., f = f_{MAX}[2]	S	135	—	130	160	135	155	125	140	—	140	—	140	—	140	mA
		L	125	—	115	130	125	145	105	115	—	110	—	110	—	105	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}_{1,2}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}[2]	S	60	—	55	70	55	60	45	50	—	50	—	50	—	50	mA
		L	45	—	40	50	45	50	35	40	—	35	—	35	—	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}_{1,2}$ ≥ V_{HC}, V_{CC}= Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0[2]	S	20	—	15	25	15	20	15	20	—	20	—	20	—	20	mA
		L	1.5	—	0.5	1.5	0.5	1.5	0.5	1.5	—	1.5	—	1.5	—	1.5	

NOTES: 2988 tbl 06

1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

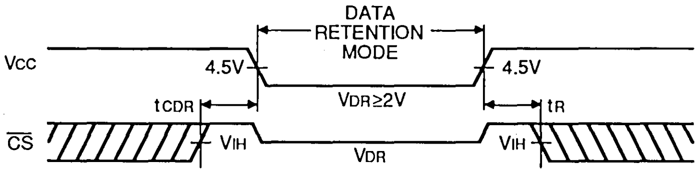
(L Version Only) $V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Condition		Min.	Typ.(1) Vcc @		Max. Vcc @		Unit
					2.0v	3.0V	2.0V	3.0V	
V_{DR}	Vcc for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	—	10	15	600	900	µA
			COM'L.	—	10	15	150	225	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	—	—	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	—	—	ns
$\lvert I_{LI} \rvert$(3)	Input Leakage Current			—	—	—	2	2	µA

NOTES:
1. $T_A = +25°C$.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

2988 tbl 09

LOW Vcc DATA RETENTION WAVEFORM

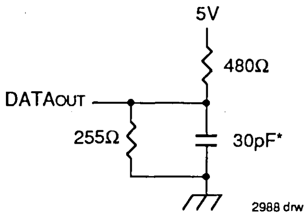


2988 drw 04

AC TEST CONDITIONS

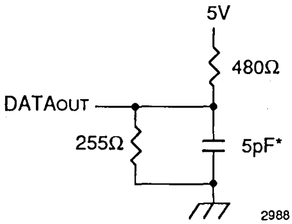
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2988 tbl 10



2988 drw 04

Figure 1. Output Load



2988 drw 05

Figure 2. Output Load
(for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW} and t_{WHZ})

*Includes scope and jig capacitances

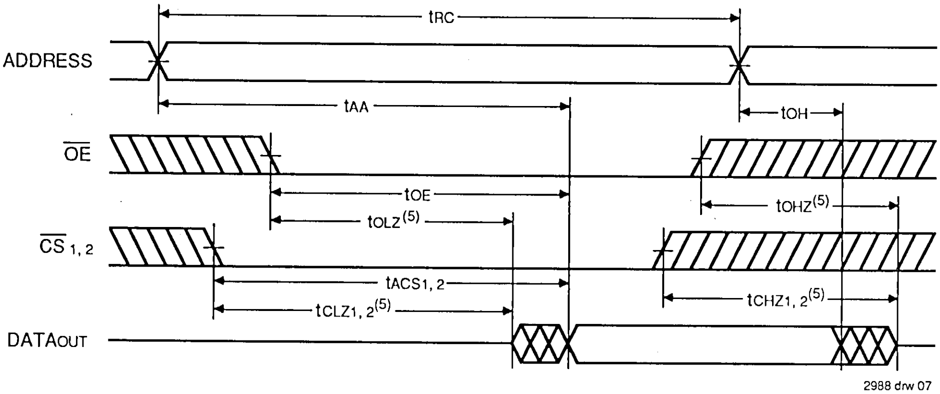
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71981/2S15[1]/20 71981/2L15[1]/20		71981/2S25 71981/2L25		71981/2S35/45[2] 71981/2L35/45[2]		71981/2S55[2] 71981/2L55[2]		71981/2S70[2] 71981/2L70[2]		71981/2S85[2] 71981/2L85[2]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle														
t_{RC}	Read Cycle Time	15/20	—	25	—	35/45	—	55	—	70	—	85	—	ns
t_{AA}	Address Access Time	—	15/19	—	25	—	35/45	—	55	—	70	—	85	ns
$t_{ACS1,2}$	Chip Select-1,2 Access Time[3]	—	15/20	—	25	—	35/45	—	55	—	70	—	85	ns
$t_{CLZ1,2}$	Chip Select-1,2 to Output in Low Z[4]	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	8/9	—	11	—	20/25	—	35	—	45	—	55	ns
t_{OLZ}	Output Enable to Output in Low Z[4]	5	—	5	—	5	—	5	—	5	—	5	—	ns
$t_{CHZ1,2}$	Chip Select1,2 to Output in High Z[4]	—	7/8	—	10	—	4	—	20	—	25	—	30	ns
t_{OHZ}	Output Disable to Output in High Z[4]	—	7/8	—	9	—	15	—	20	—	25	—	30	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}	Chip Select to Power Up Time[4]	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Deselect to Power Down Time[4]	—	15/20	—	25	—	35/45	—	55	—	70	—	85	ns

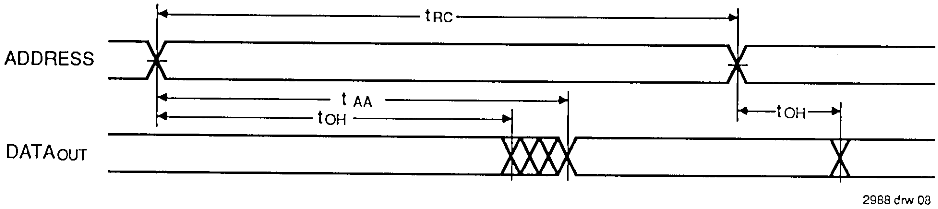
2988 tbl 11

NOTES:
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Both chip selects must be active low for the device to be selected.
4. This parameter guaranteed but not tested.

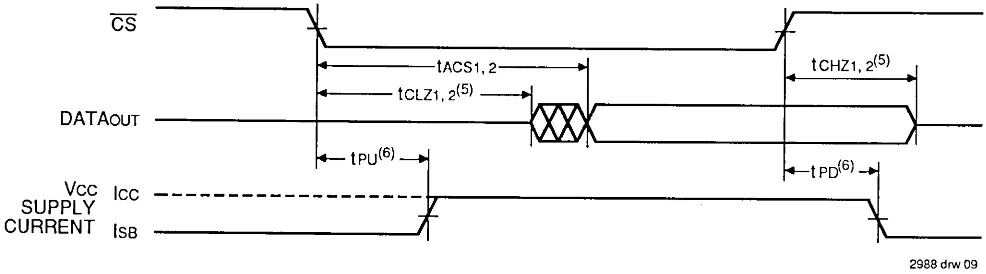
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



NOTES:

1. $\overline{WE}$ is high for READ cycle.
2. Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $\overline{CS}_2 = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}_1$ and or $\overline{CS}_2$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ±200mV from steady state voltage.
6. This parameter is guaranteed but not tested.

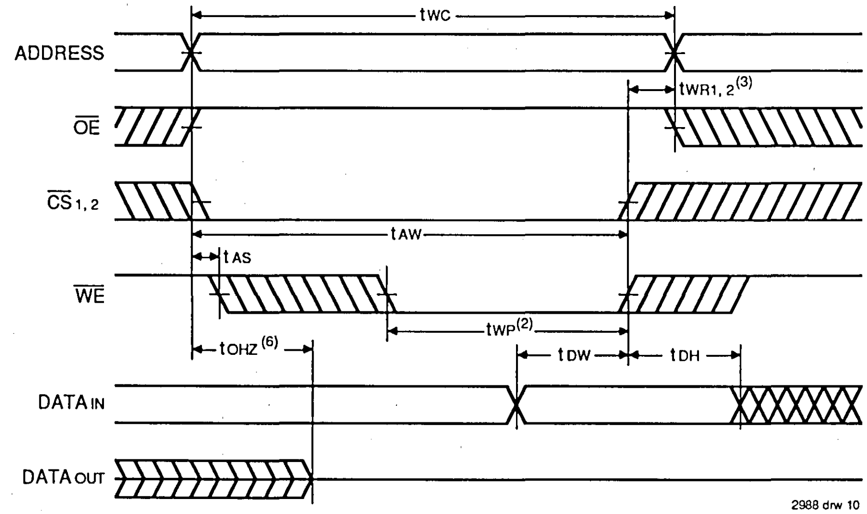
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71981/2S15(1)/20 71981/2L15(1)/20		71981/2S25 71981/2L25		71981/2S35/45(2) 71981/2L35/45(2)		71981/2S55(2) 71981/2L55(2)		71981/2S70(2) 71981/2L70(2)		71981/2S85(2) 71981/2L85(2)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle														
tWC	Write Cycle Time	14/17	—	20	—	30/40	—	50	—	60	—	75	—	ns
tCW1,2	Chip Select to End of Write	14/17	—	20	—	25/35	—	50	—	60	—	75	—	ns
tAW	Address Valid to End of Write	14/17	—	20	—	25/35	—	50	—	60	—	75	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	14/17	—	20	—	25/35	—	50	—	60	—	75	—	ns
tWR1,2	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWHZ	Write Enable to Output in High Z(3,5)	—	5/6	—	7	—	10/15	—	25	—	30	—	40	ns
tDW	Data Valid to End of Write	10/10	—	13	—	15/20	—	25	—	30	—	35	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tOW	Output Active from End of Write(3,5)	5	—	5	—	5	—	5	—	5	—	5	—	ns
tIY	Data Valid to Output Valid(3,4)	—	12/15	—	20	—	30/35	—	40	—	45	—	50	ns
tWY	Write Enable to Output Valid(3,4)	—	12/15	—	20	—	30/35	—	40	—	45	—	50	ns

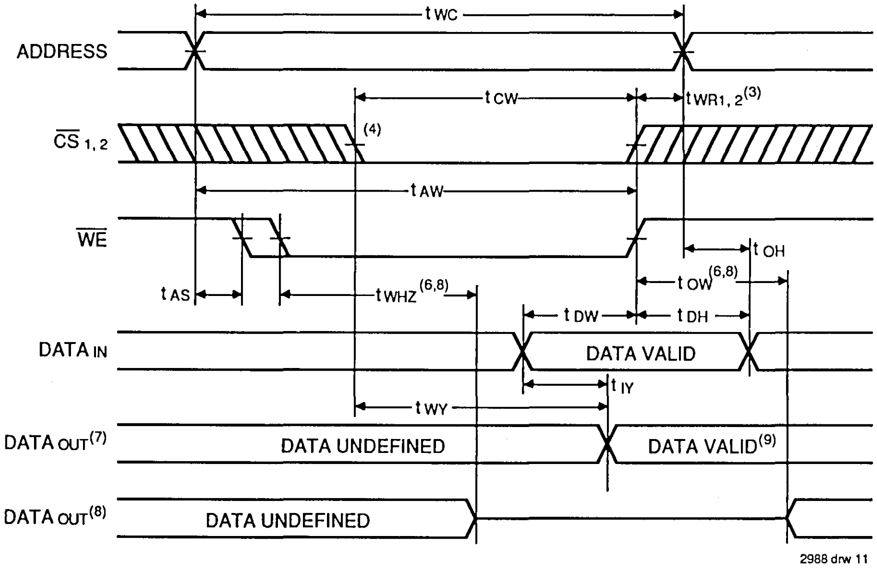
2988 tbl 12

NOTES:
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. For IDT71981S/L only.
5. For IDT71982S/L only.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{\text{WE}}$ CONTROLLED TIMING)(1)



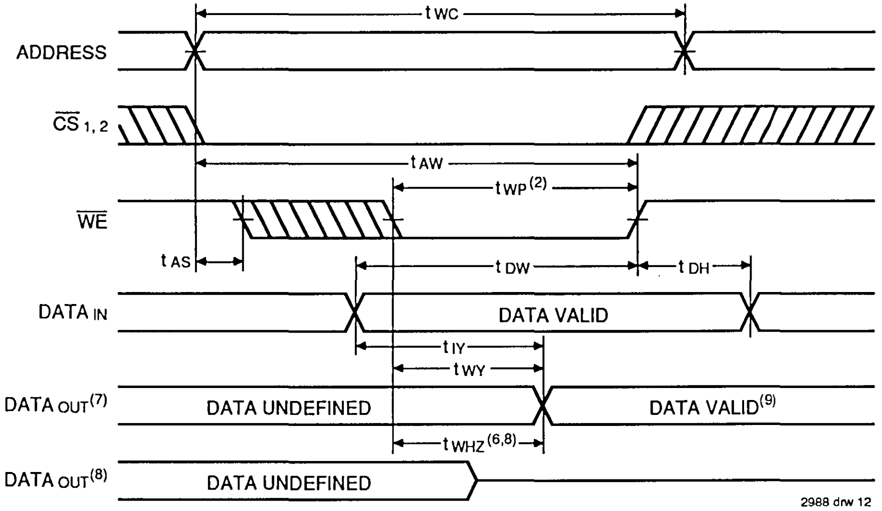
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{\text{CS}}$ CONTROLLED TIMING)(1, 5)



NOTES:

1. $\overline{\text{WE}}$ or $\overline{\text{CS}}_1$ or $\overline{\text{CS}}_2$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{\text{WE}}$, a low $\overline{\text{CS}}_1$ and a low $\overline{\text{CS}}_2$.
3. tWR is measured from the earlier of $\overline{\text{CS}}_1$, $\overline{\text{CS}}_2$ or $\overline{\text{WE}}$ going high to the end of the write cycle.
4. If the $\overline{\text{CS}}_1$ and or $\overline{\text{CS}}_2$ low transition occurs simultaneously with or after the $\overline{\text{WE}}$ low transition, outputs remain in a high impedance state.
5. $\overline{\text{OE}}$ is continuously low ($\overline{\text{OE}}$ = VIL).
6. Transition is measured ±200mV from steady state.
7. For IDT71981 only.
8. For IDT1982 only.
9. DATAOUT = DATAIN.

TIMING WAVEFORM OF WRITE CYCLE NO. 3 ($\overline{\text{WE}}$ CONTROLLED, $\overline{\text{OE}}$ LOW)[1, 5]



NOTES:
1. $\overline{\text{WE}}$ or $\overline{\text{CS}}_1$ or $\overline{\text{CS}}_2$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{\text{WE}}$, a low $\overline{\text{CS}}_1$ and a low $\overline{\text{CS}}_2$.
3. t_{WR} is measured from the earlier of $\overline{\text{CS}}_1$, $\overline{\text{CS}}_2$ or $\overline{\text{WE}}$ going high to the end of the write cycle.
4. If the $\overline{\text{CS}}_1$ and or $\overline{\text{CS}}_2$ low transition occurs simultaneously with or after the $\overline{\text{WE}}$ low transition, outputs remain in a high impedance state.
5. $\overline{\text{OE}}$ is continuously low ($\overline{\text{OE}} = V_{IL}$).
6. Transition is measured ±200mV from steady state.
7. For IDT71981 only.
8. For IDT1982 only.
9. $\text{DATA}_{\text{OUT}} = \text{DATA}_{\text{IN}}$.

ORDERING INFORMATION

IDT	XXXX	X	XX	XX	X
	Device Type	Power	Speed	Package	Process/ Temperature Range

Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

D	Ceramic DIP (300 mil)
P	Plastic DIP (300 mil)
C	Sidebraze DIP (400 mil)
L	Leadless Chip Carrier
SO	Small Outline IC (Gull Wing)
Y	Small Outline IC (J-Bend)

15	Commercial Only	Speed in Nanoseconds
20		
25		
35		
45	Military Only	
55	Military Only	
70	Military Only	
85	Military Only	

S	Standard Power
L	Low Power

71981	64K (16K x 4-Bit)
71982	64K (16K x 4-Bit) High Inpedance Outputs

2988 drw 12

HIGH-SPEED BiCEMOS STATIC RAMS 6

BiCEMOS™ STATIC RAM PRODUCTS

With its broad line of BiCEMOS TTL I/O Static Random Access Memories (SRAMs), Integrated Device Technology, Inc. (IDT) has advanced its position as the major American supplier of high performance SRAMs. Advanced BiCEMOS design techniques mean IDT produces the fastest commercial SRAMs today.

WIDE SELECTION OF BICEMOS SRAMS

Speed leadership is coupled to the widest selection of BiCEMOS SRAM organizations available. BiCEMOS 64K and 256K devices are offered in x4 and x 8 widths. These are the highest speed TTL I/O SRAMs available. This year's offerings will include x16 and x9 devices, along with one megabit x4 and x8 SRAMs. IDT also offers BiCameral SRAMs and other unique architectures.

ADVANCED BICEMOS TECHNOLOGY

Users of BiCEMOS SRAMs can have performance two to four years ahead of time. The addition of bipolar circuit elements allows current CMOS technology to reach speeds expected from the next generation — now. Because BiCEMOS technology is based on current CEMOS™ products, the cost of a next generation facility is avoided which means economical high-speed SRAMs.

Innovative process technology has resulted in outstanding advances in high density high-speed devices. Examples such as:

- 64K SRAMs now available with access times below 10 ns — previously available only in bipolar parts;
- 12 ns 256K SRAMs (61B298 organized as 64Kx4);
- 15 ns 1 Meg SRAMs (71B024 organized as 128Kx8 — available 1991).

Our dedication to performance advancements will mean four megabit SRAMs with less than 20 ns access time in 1991.

IDT EMPHASIZES CACHE MEMORY

Once caches were only found in the highest performance systems. Since CPU speeds have exceeded DRAM speeds, primary or secondary caches are now essential for many system designs. Moreover, the advent of processors like the IDT79R3000 and Intel i486 mean most new system designs need caches. IDT's BiCEMOS speeds allow these processors to achieve maximum performance. Applying innovations to basic technology results in high-speed cache data SRAMs available only from IDT:

- IDT has BiCEMOS 8Kx8 and 8Kx9 cache-tag SRAMs which are the fastest large cache-tags;
- the IDT71B222 BiCameral CacheRAM (4Kx18x2) for the R3000;
- the IDT71B221 BiCameral CacheRAM (4Kx18x2) for the i486;
- the IDT71B229 BiCameral CacheRAM (16Kx9x2) for the R3000.

HIGH-SPEED MILITARY SRAMS

Our continuing commitment to the military market provides the BiCEMOS advantage to military customers. Military SRAMs are manufactured in strict conformance with all requirements of MIL-STD-883 and are available as military SMD devices. Our design efforts also anticipate the military requirements for high-speed parts usable over the military temperature range. In addition, our commercial products benefit by sharing most processing steps with military devices.

PACKAGE OPTIONS

Our commitment to technology extends to advanced, cost-effective packaging techniques. IDT's BiCEMOS SRAMs are available in a variety of packages in commercial and military temperature ranges including:

- surface-mount SOJ plastic packages;
- plastic and ceramic DIPs;
- ceramic LCCs .

This constantly expanding offering of packages is in response to critical second-level interconnect issues confronting the system designer.

IDT MEANS SRAM LEADERSHIP

These extremely high-performance BiCEMOS SRAMs demonstrate leading-edge technology compatible with today's high-performance systems. Look to IDT for performance, technology and quality solutions to memory system problems.

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STATIC RAM PRODUCTS

HIGH-SPEED BiCEMOS™ STATIC RAMS

Integrated Device Technology, Inc.

BiCMOS STATIC RAM 256K (64K x 4-BIT)

PRELIMINARY
IDT61B298

FEATURES:

- 64K x 4 BiCEMOS Static RAM
- High-speed address / chip select time
  - — Commercial: 12/15/20ns
  - — Military: 15/20ns
- Output Enable
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Available in 28-pin 300 mil plastic DIP, 28-pin 300 mil Sidebraze DIP and 28-pin 300-mil plastic SOJ

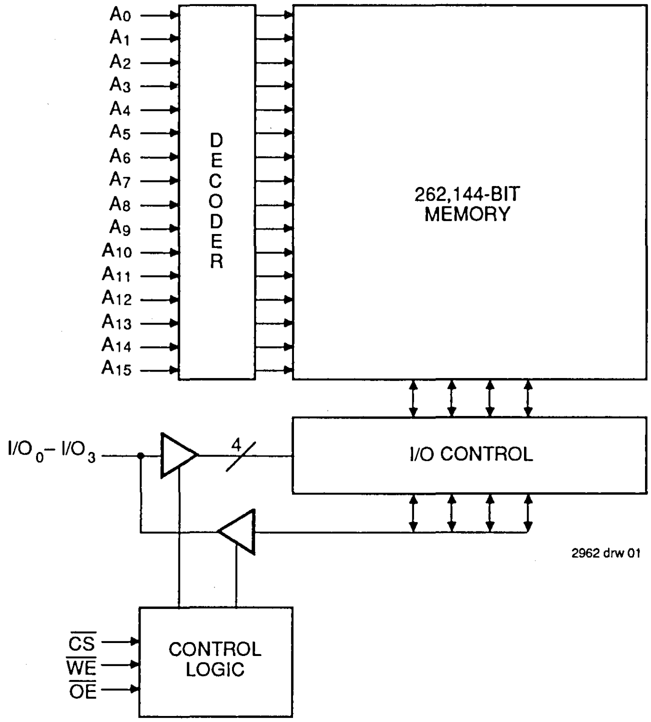
DESCRIPTION:

The IDT61B298 is a 262,144-bit high-speed static RAM organized as 64Kx4. It is fabricated using IDT's high-perfomance high-reliability BiCEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

Address access times as fast as 10 ns are available with power consumption of only 450mW (typ.). All inputs and outputs of the IDT61B298 are TTL-compatible and operation is from a single 5V supply.

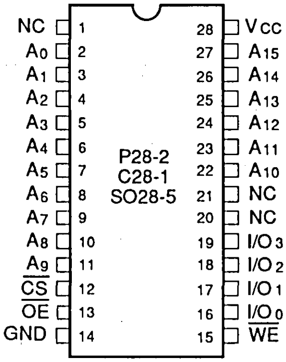
The IDT61B298 is packaged in a 28 pin 300 mil plastic DIP, 28-pin 300 mil ceramic DIP and a 28-pin 300 mil SOJ.

FUNCTIONAL BLOCK DIAGRAM



BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



2962 drw 02

**DIP/SOJ
TOP VIEW**

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +125	°C
P_T	Power Dissipation	1.25	1.25	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2958 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE[1]

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
H	X	X	Hi-Z	Deselect Chip
L	L	H	D_{OUT}	Read Cycle
L	X	L	D_{IN}	Write Cycle
L	H	H	Hi-Z	Outputs Disabled

NOTE: 2962 tbl 01

1. H = V_{IH}, L = V_{IL}, x = Don't care.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Max.	Unit
C_{IN}[2]	Input Capacitance	8	pF
C_{OUT}[1,2]	Output Capacitance	12	pF

NOTES: 2962 tbl 03

1. With output deselected.
2. Characterized values, not currently tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5	—	0.8	V

NOTE: 2962 tbl 04

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT61B298			Unit
			Min.	Typ.[1]	Max.	
$\lvert I_{LI}\rvert$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	—	10	µA
$\lvert I_{LO}\rvert$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.	—	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.	—	—	0.4	
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	—	—	V

NOTE: 2962 tbl 05

1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%)

Symbol	Parameter	61B298S12		61B298S15		61B298S20		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Dynamic Operating Current $\overline{\text{CS}} = V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	180	—	160	170	140	150	mA

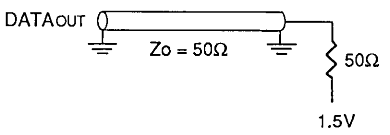
2962 tbl 05

NOTES:
1. All values are maximum guaranteed values.
2. $f_{MAX} = 1/t_{RC}$.

AC TEST CONDITIONS

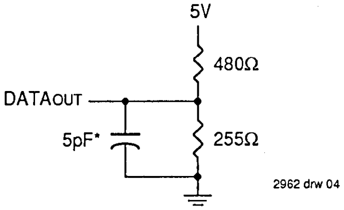
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1A, 1B & 1C

2962 tbl 06



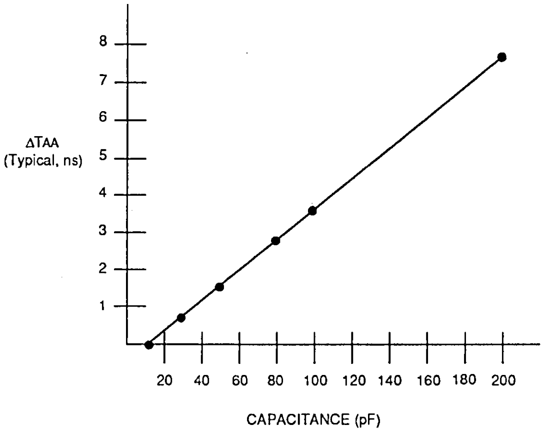
2962 drw 03a

Figure 1A. AC Test Loads



*Including jig and scope capacitance.

Figure 1B.



2962 drw 03b

Figure 1C. Lumped Capacitive Load, Typical Derating

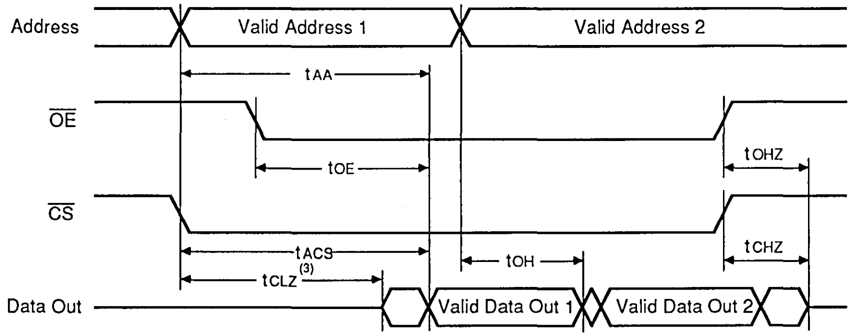
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	61B298S12(1)		61B298S15		61B298S20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	12	—	15	—	20	—	ns
t_{AA}	Address Access Time	—	12	—	15	—	20	ns
t_{ACS}	$\overline{CS}$ Access Time	—	5	—	6	—	8	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	5	—	6	—	8	ns
t_{CLZ}(2)	$\overline{CS}$ to Output in Low Z	2	—	2	—	2	—	ns
t_{CHZ}(2)	$\overline{CS}$ to Output in High Z	—	7	—	8	—	10	ns
t_{OLZ}(2)	$\overline{OE}$ to Output Low Z	2	—	2	—	2	—	ns
t_{OHZ}(2)	$\overline{OE}$ to Output High Z	—	4	—	5	—	6	ns
t_{OH}	Out Hold from Add Change	5	—	5	—	5	—	ns
Write Cycle								
t_{WC}	Write Cycle Time	12	—	15	—	20	—	ns
t_{AW}	Address to End of Write	9	—	10	—	12	—	ns
t_{AS}	Address Setup Tme	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	9	—	10	—	12	—	ns
t_{CW}	$\overline{CS}$ to End of Write	8	—	9	—	10	—	ns
t_{WR}	Write Recovery	0	—	0	—	0	—	ns
t_{WHZ}(2)	$\overline{WE}$ to Out in High Z	—	5	—	6	—	7	ns
t_{DW}	Data Setup	5	—	6	—	8	—	ns
t_{DH}	Data Hold	0	—	0	—	0	—	ns
t_{OW}(2)	Output from End of Write	2	—	2	—	2	—	ns

2962 tbl 08

NOTES:
1. 0° to +70°C temperature range only.
2. This parameter is guaranteed with the AC Load, Figure 1B, and is not tested.

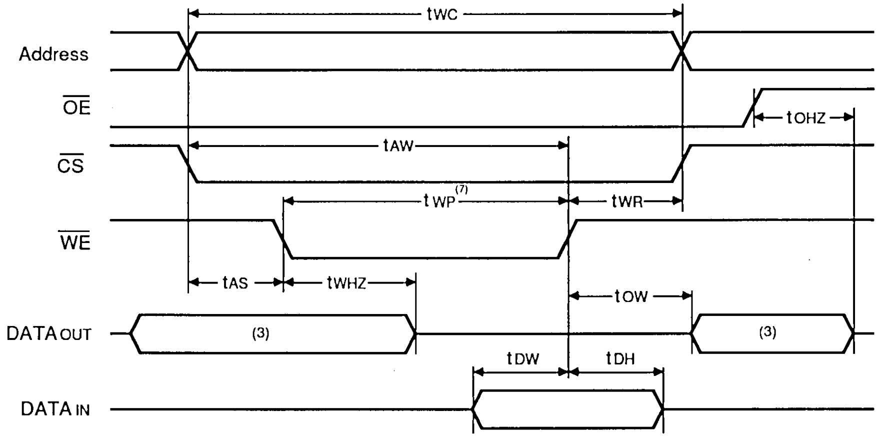
TIMING WAVEFORM OF READ CYCLE(1,2)



2962 drw 05

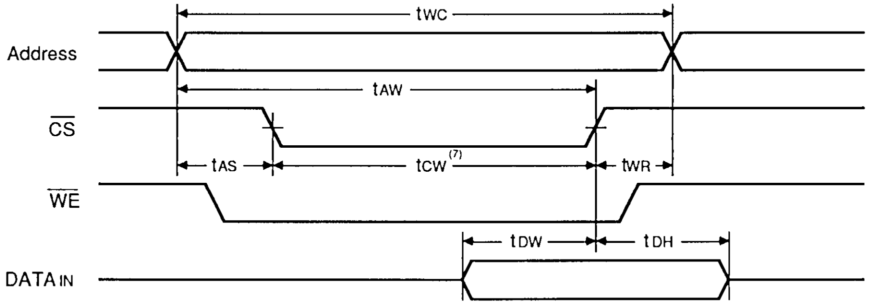
NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Address valid prior to or coincident with $\overline{CS}$ transition low.
3. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ CYCLE)(1,2,4,5)



2962 drw 06

TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ CYCLE)(1,2,4,5,6)

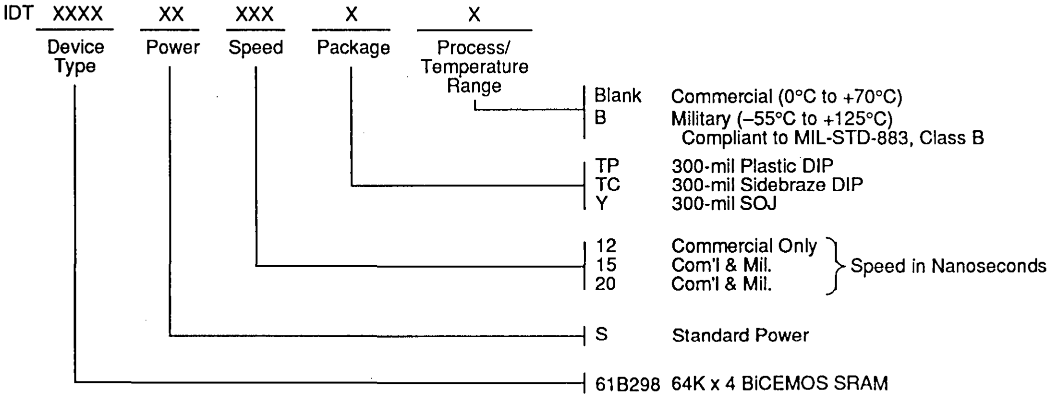


2962 drw 07

NOTES:

1. A write occurs during the overlap (t_{CW} and t_{WP}) of $\overline{CS}$ low and $\overline{WE}$ low.
2. t_{WP} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ being deasserted.
3. During this period, the I/O pins are in the output state, and input signals must not be applied on these pins.
4. If $\overline{CS}$ asserted coincident with or after $\overline{WE}$ goes low, the output will remain in a high impedance state.
5. If $\overline{CS}$ is deasserted coincident with or before $\overline{WE}$ goes high, the output will remain in a high impedance state.
6. The transition is measured ±200mV from steady state with a 5pF load.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or ($t_{WHZ} + t_{DW}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

ORDERING INFORMATION



2962 drw 08

Integrated Device Technology, Inc.

BiCMOS STATIC RAM
64K (16K x 4-BIT)

PRELIMINARY
IDT61B98

FEATURES:

- 16K x 4 BiCEMOS™ Static RAM
- High-speed address access time
  - Commercial: 8/10/12ns
  - Military: 10/12/15ns
- Fast Output Enable
  - Commercial: 5/6/7ns
  - Military: 6/7/8ns
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Available in 24-pin, 300 mil plastic DIP; 24-pin, 300 mil ceramic DIP and 24-pin, 300-mil plastic SOJ

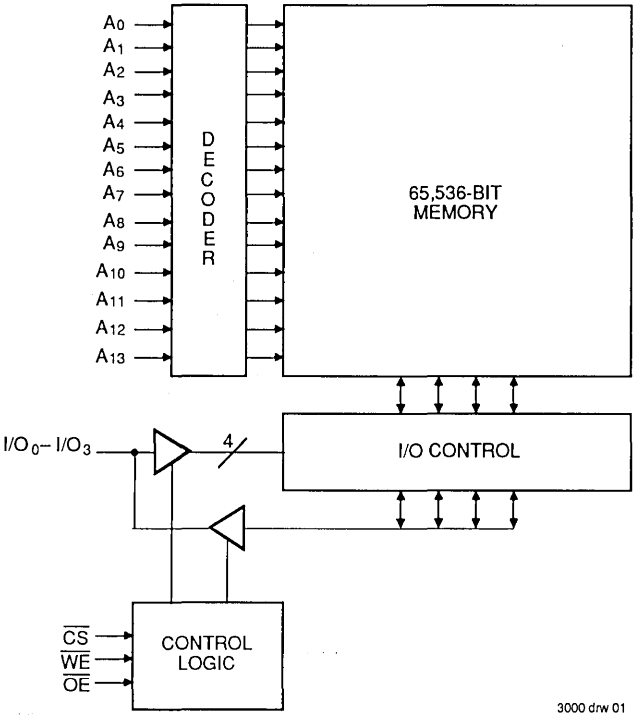
DESCRIPTION:

The IDT61B98 is a 65,536-bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-perfomance high-reliability BiCEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

Address access times as fast as 8ns are available with power consumption of only 400mW (typ.). All inputs and outputs of the IDT61B98 are TTL-compatible and operation is from a single 5V supply.

The IDT61B98 is packaged in a 24-pin, 300 mil plastic DIP; 24-pin, 300 mil ceramic DIP and a 24-pin, 300 mil SOJ.

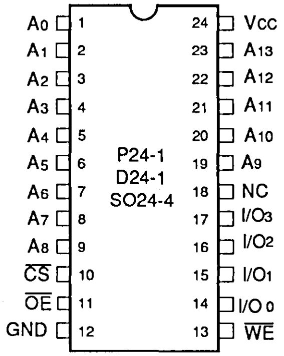
FUNCTIONAL BLOCK DIAGRAM



3000 drw 01

BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



3000 drw 02

DIP/SOJ
TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +125	°C
P_T	Power Dissipation	1.25	1.25	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2958 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE[1]

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
H	X	X	Hi-Z	Deselect Chip
L	L	H	D_{OUT}	Read Cycle
L	X	L	D_{IN}	Write Cycle
L	H	H	Hi-Z	Outputs Disabled

NOTE: 3000 tbl 01

1. H = V_{IH}, L = V_{IL}, X = Don't care.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}(2)	Input Capacitance	$V_{IN} = 0V$	8	pF
C_{OUT}(1,2)	Output Capacitance	$V_{OUT} = 0V$	12	pF

NOTES: 3000 tbl 03

1. With output deselected.
2. Characterized values, not currently tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5	—	0.8	V

NOTE: 3000 tbl 04

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT61B98		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS} = V_{IH}$, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.	—	0.4	
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	—	V

3000 tbl 05

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5.0V ± 10%)

Symbol	Parameter	61B98S8		61B98S10		61B98S12		61B98S15		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
Icc	Dynamic Operating Current, $\overline{CS}$ = V_{IL} Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	200	—	180	190	160	170	—	170	mA

NOTES:

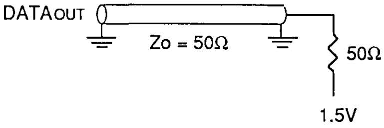
3000 tbl 05

1. All values are maximum guaranteed values.
2. f_{MAX} = $1/t_{RC}$.

AC TEST CONDITIONS

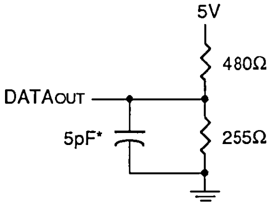
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1A, 1B & 1C

3000 tbl 06



3000 drw 03a

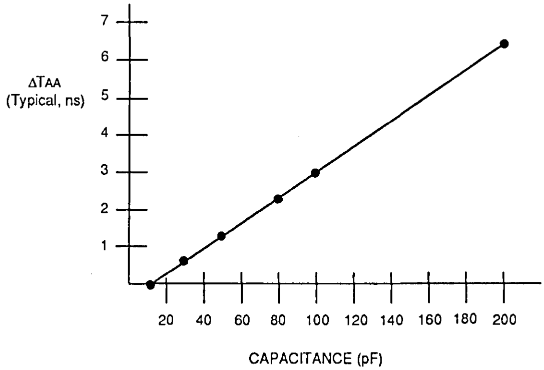
Figure 1A. AC Test Load



3000 drw 04

*Including jig and scope capacitance.

Figure 1B.



3000 drw 03b

Figure 1C. Lumped Capacitive Load, Typical Derating

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

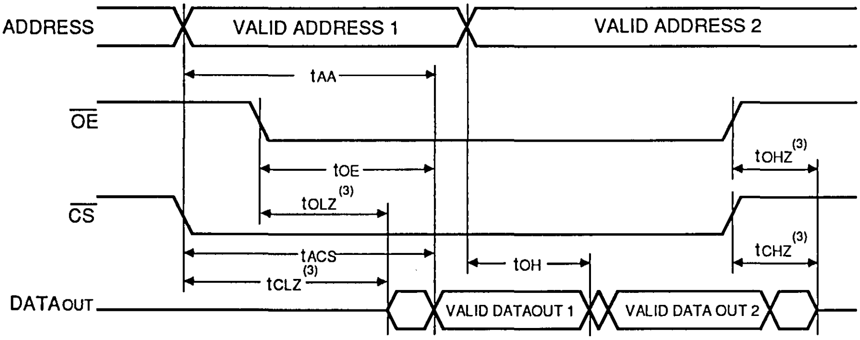
Symbol	Parameter	61B98S8[(1)]		61B98S10		61B98S12		61B98S15[(3)]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	8	—	10	—	12	—	15	—	ns
t_{AA}	Address Access Time	—	8	—	10	—	12	—	15	ns
t_{ACS}	$\overline{CS}$ Access Time	—	6	—	7	—	7	—	8	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	4	—	5	—	6	—	7	ns
t_{CLZ}(2)	$\overline{CS}$ to Output in Low Z	3	—	3	—	3	—	4	—	ns
t_{CHZ}(2)	$\overline{CS}$ to Output in High Z	—	6	—	6	—	7	—	8	ns
t_{OLZ}(2)	$\overline{OE}$ to Output Low Z	3	—	3	—	3	—	4	—	ns
t_{OHZ}(2)	$\overline{OE}$ to Output High Z	—	3	—	3	—	3	—	4	ns
t_{OH}	Out Hold from Add Change	3	—	3	—	3	—	3	—	ns
Write Cycle										
t_{WC}	Write Cycle Time	8	—	10	—	12	—	15	—	ns
t_{AW}	Address to End of Write	8	—	8	—	9	—	10	—	ns
t_{AS}	Address Setup TIME	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	8	—	8	—	9	—	10	—	ns
t_{CW}	$\overline{CS}$ to End of Write	8	—	8	—	9	—	10	—	ns
t_{WR}	Write Recovery	0	—	0	—	0	—	0	—	ns
t_{WZ}(2)	$\overline{WE}$ to Out in High Z	—	3	—	3	—	3	—	4	ns
t_{DW}	Data Setup	5	—	5	—	6	—	8	—	ns
t_{DH}	Data Hold	0	—	0	—	0	—	0	—	ns
t_{OW}(2)	Output from End of Write	3	—	3	—	3	—	4	—	ns

NOTES:

3000 tbl 08

1. 0° to +70°C temperature range only.
2. This parameter is guaranteed with the AC Load, Figure 1B, and is not tested.
3. -55° to +125°C temperature range only.

TIMING WAVEFORM OF READ CYCLE(1,2)

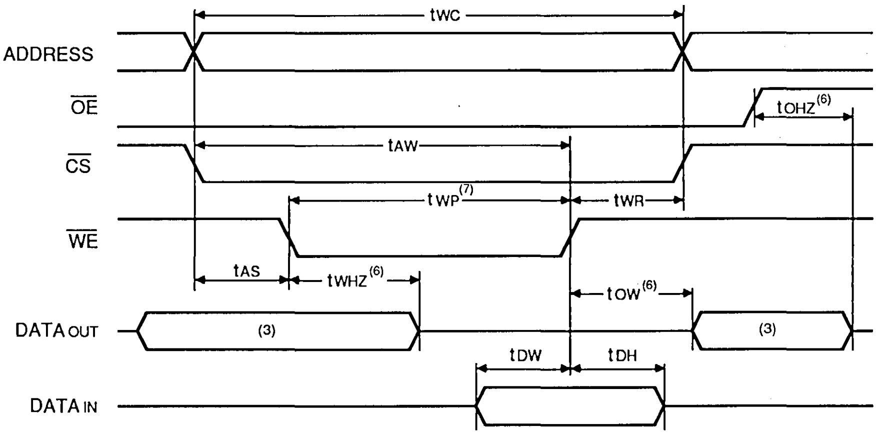


3000 drw 05

NOTES:

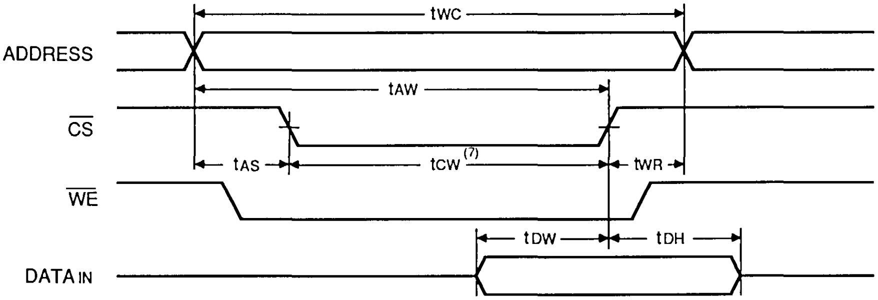
1. $\overline{WE}$ is high for read cycle.
2. Address valid prior to or coincident with $\overline{CS}$ transition low.
3. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{\text{WE}}$ CYCLE)(1,2,4,5)



3000 drw 06

TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{\text{CS}}$ CYCLE)(1,2,4,5,6)

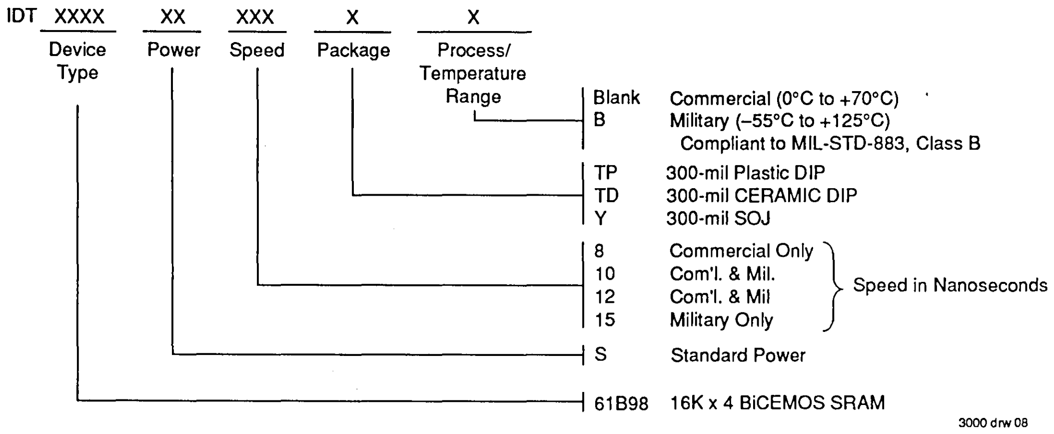


3000 drw 07

NOTES:

1. A write occurs during the overlap (tCW and tWP) of $\overline{\text{CS}}$ low and $\overline{\text{WE}}$ low.
2. tWP is measured from the earlier of $\overline{\text{CS}}$ or $\overline{\text{WE}}$ being deasserted.
3. During this period, the I/O pins are in the output state, and input signals must not be applied on these pins.
4. If $\overline{\text{CS}}$ asserted coincident with or after $\overline{\text{WE}}$ goes low, the output will remain in a high impedance state.
5. If $\overline{\text{CS}}$ is deasserted coincident with or before $\overline{\text{WE}}$ goes high, the output will remain in a high impedance state.
6. The transition is measured ±200mV from steady state with a 5pF load.
7. If $\overline{\text{OE}}$ is low during a $\overline{\text{WE}}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{\text{OE}}$ is high during a $\overline{\text{WE}}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

ORDERING INFORMATION



Integrated Device Technology, Inc.

BiCMOS STATIC RAM 1 MEG (128K X 8-BIT)

ADVANCE INFORMATION
IDT71B024

FEATURES:

- 128K x 8 configuration
- Two chip selects plus Output Enable pin
- High-speed access
  - — Military: 20/25ns (max.)
  - — Commercial: 15/20/25ns (max.)
- Low power consumption
- Battery back-up operation—2V data retention
- Available in 32-pin DIP
- TTL-compatible
- Single 5V (+10%) power supply
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71B024 is an extremely high-density 128K x 8-bit high-speed static RAM designed for use in systems where fast computation, low power and board density are of the utmost importance.

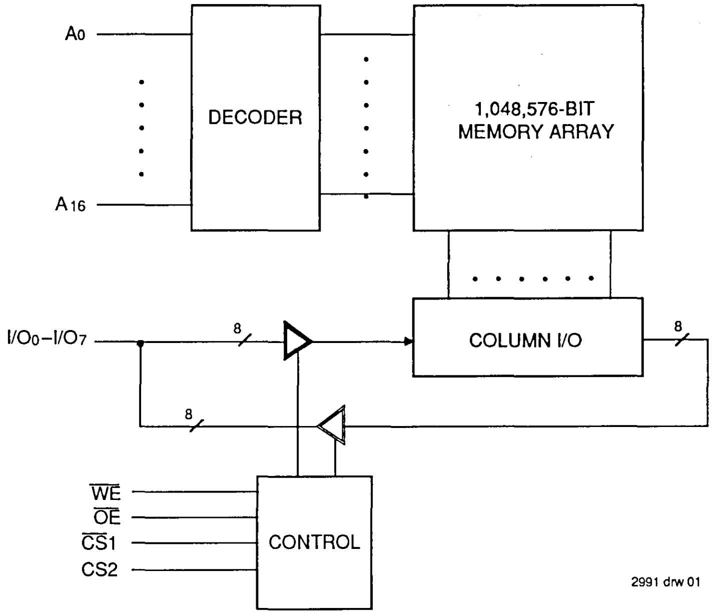
The IDT71B024 uses eight bidirectional input/output lines to provide simultaneous access to all bits in a word and has an output enable ($\overline{OE}$) pin which operates as fast as 10ns. This function allows designers to access the IDT71B024 at speeds much higher than the already fast 15ns address access time to achieve a considerable throughput advantage.

Fabricated using IDT's BiCEMOS™ high-performance technology, the IDT71B024 typically operates at maximum access times as fast as 15ns.

All inputs and outputs of the IDT71B024 are TTL-compatible and the device operates from a standard 5V supply, simplifying system design. The IDT71B024 is packaged in a 32-pin DIP.

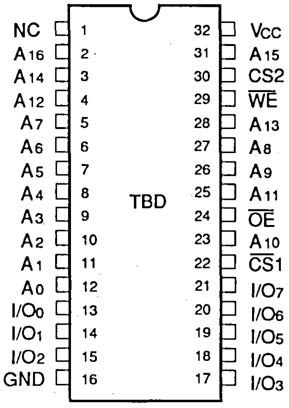
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



2991 drw 02

DIP
TOP VIEW

TRUTH TABLE

INPUTS				OUTPUTS	FUNCTION
$\overline{WE}$	$\overline{CS}_1$	CS_2	$\overline{OE}$	I/O_0–I/O_7	
X	H	X	X	High-Z	Deselected
X	X	L	X	High-Z	Deselected
H	L	H	H	High-Z	Outputs disabled
H	L	H	L	DOUT	Read data from RAM
L	L	H	X	High-Z	Write data to RAM

NOTE: 2991 tbl 01

1. H = High, L = Low, X = Don't Care, High-Z = High Impedance

Integrated Device Technology, Inc.

BiCMOS STATIC RAM 1 MEG (256K X 4-BIT)

ADVANCE INFORMATION IDT71B028

FEATURES:

- 256K x 4 configuration
- High-speed access
  - Military: 20/25ns (max.)
  - Commercial: 15/20/25ns (max.)
- Low power consumption
- Battery back-up operation—2V data retention
- Available in 28-pin DIP
- TTL-compatible
- Single 5V (±10%) power supply
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

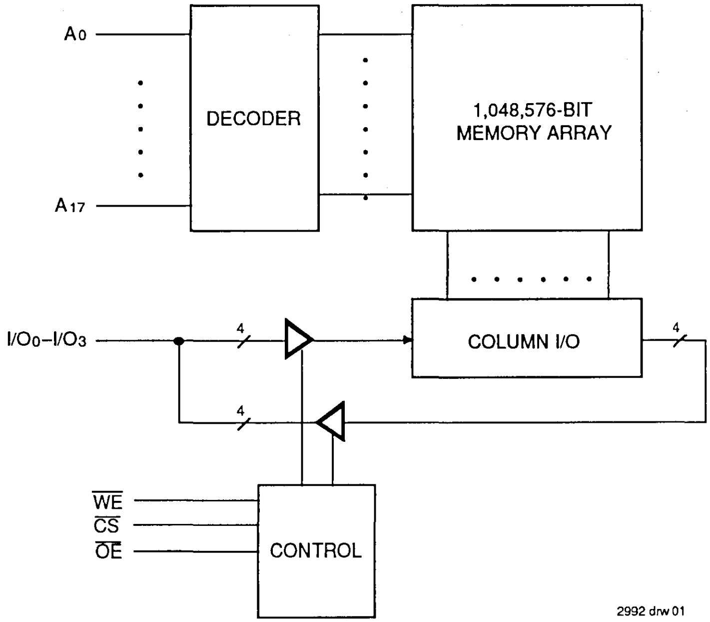
The IDT71B028 is an extremely high-density (256K x 4-bit), high speed static RAM designed for use in systems where fast computation, low power and board density are of the utmost importance.

The IDT71B028 uses four bidirectional input/output lines to provide simultaneous access to all bits in a word and has a high-speed 15ns address access time to achieve a considerable throughput advantage.

Fabricated using IDT's BiCEMOS™ high-performance technology. All inputs and outputs of the IDT71B028 are TTL-compatible and the device operates from a standard 5V supply, simplifying system design. The IDT71B028 is packaged in a 28-pin DIP.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

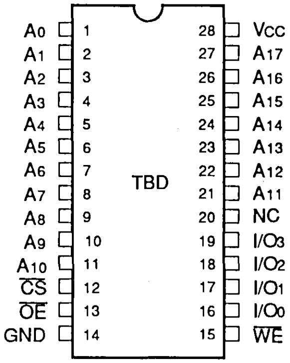
FUNCTIONAL BLOCK DIAGRAM



2992 drw 01

BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



2992 drw 02

DIP
TOP VIEW

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O0–I/O3	FUNCTION
H	X	X	High-Z	Deselected, Powered-Down
L	H	H	High-Z	Outputs Disabled
L	L	H	DOUT	Read Data from RAM
L	X	L	High-Z	Write Data to RAM

NOTE: 2992 tbl 01

1. H = High, L = Low, X = Don't Care, High-Z = High Impedance

Integrated Device Technology, Inc.

BiCameral™ CacheRAM™ 128K-BIT (4K x 18 x 2) FOR i486 CACHES

ADVANCE INFORMATION
IDT71B221

FEATURES:

- Supports high speed i486 CPUs
  - — 24, 28ns
  - — Supports 33 and 25 MHz
- BiCameral organization
  - — Single-chip support of two-way caches
  - — No bank-switching timing contention
- Works with Intel 82485 cache controller chip
- Programmable 4K or 8K depth implements 32K-Byte caches (two-way or direct-mapped)
- Eighteen-bit width supports i486 internal parity
- Internal address latch and input data latch
- Fast Output Enable
- 52-pin PLCC and PQFP packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

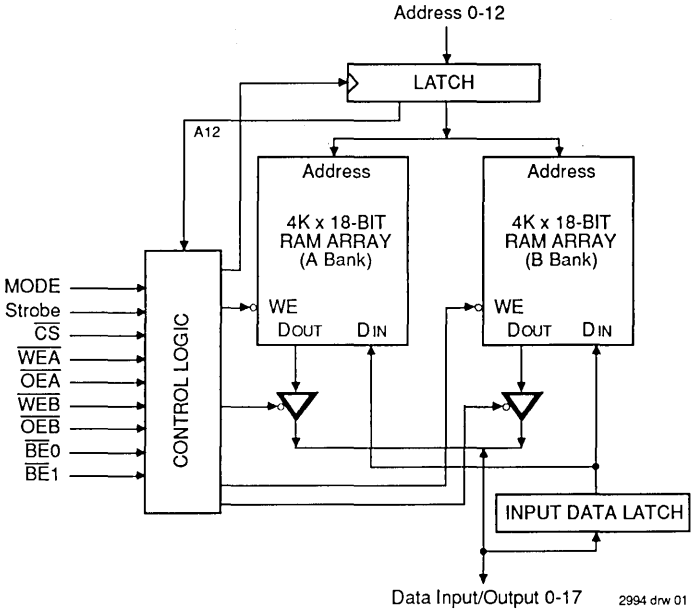
The IDT71B221 is a BiCameral Cache RAM specifically designed to support two-way set-associative caches for the Intel i486 microprocessor. A complete 32K-Byte secondary cache for the i486 can be built with only four IDT71B221s and Intel's 82485 cache controller chip, and will provide maximum throughput for CPU clock frequencies up to 33MHz. The convenient PLCC and PQFP packages allow the designer to fit a 32K-Byte cache in the smallest possible circuit board area.

Internal address latches remove the need to use discrete devices to implement external address latches. The BiCameral (two bank) organization both reduces the number of devices required to support the 82485's two-way architecture, and eliminates contention problems encountered when one RAM bank is being enabled while the other is being disabled.

All timing parameters have been optimized to support 25MHz and 33MHz i486 clock speeds, thus vastly simplifying design of i486 caches.

Made with BiCEMOS™, IDTs advanced high-speed process, the IDT71B221 provides dense caches in low board space while consuming a minimum of power. Military grade product is manufactured in compliance with the latest revision of MIL-STD 883, Class B, making the device ideally suited to military temperature applications requiring the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



2994 drw 01

BiCEMOS, BiCameral and CacheRAM are trademarks of Integrated Device Technology, Inc.
Intel and i486 are trademarks of Intel Corporation.

PIN DESCRIPTIONS

Name	Description
MODE	The MODE input, when high, causes the 71B221's internal architecture to adopt a 4K x 18 x 2 format which is used to support two-way set associative caches. Taking the MODE input low reconfigures the 71B221 to an 8K x 18 architecture.
$\overline{\text{OEA}}$	The A-bank Output Enable input when low enables the data outputs from the A bank onto the data input/output pins. If $\overline{\text{OEA}}$ is asserted simultaneously with the $\overline{\text{OEB}}$ when the MODE input is high, neither bank will be output. When the MODE input is low, the $\overline{\text{OEA}}$ and $\overline{\text{OEB}}$ inputs should be wired together. Outputs will be tristated, regardless of the state of either $\overline{\text{OEA}}$ or $\overline{\text{OEB}}$ if either $\overline{\text{WEA}}$ or $\overline{\text{WEB}}$ is asserted.
$\overline{\text{OEB}}$	This is an input which enables the data outputs from the B bank onto the data input/output pins. See the rules and conditions outlined for the $\overline{\text{OEA}}$ input described above.
$\overline{\text{WEA}}$	The A-bank Write Enable input, when low, starts a write cycle sending data from the input data latch into the RAM at the A bank address indicated by the output of the address latch. The write cycle is terminated by the high going portion of the Strobe signal. $\overline{\text{WEA}}$ disables the output enable pins $\overline{\text{OEA}}$ and $\overline{\text{OEB}}$. When the MODE input is low, the $\overline{\text{WEA}}$ and $\overline{\text{WEB}}$ inputs should be wired together.
$\overline{\text{WEB}}$	This is an input which gates data from the input data latch into the RAM at the B bank address indicated by the output of the address latch. See the rules and conditions outlined for the $\overline{\text{WEA}}$ input described above.
Strobe	The Strobe input is a TTL-compatible clock input which strobes new data into the address latch and the input data register. Internal addresses are frozen for an internally generated delay time after the rising edge of the Strobe input. Input data is latched into the data latch on the rising edge of the Strobe input.
$\overline{\text{CS}}$	Chip Select is an input which globally gates the functioning of the 71B221. When Chip Select is low, the device functions according to the controls asserted on the other inputs. When Chip Select is high, all operation is suspended.
$\overline{\text{BE}}$	The Byte Enable inputs are used for byte reads and byte writes from the i486. $\overline{\text{BE}}_{0:1}$ allows reading or writing bits $\text{I/O}_{0:8}$, while $\overline{\text{BE}}_1$ allows reading or writing bits $\text{I/O}_{9:17}$. These inputs are active low, and if disabled during a read cycle, the I/O pins they control will be left in a high-impedence state.
$\text{Addr}_{0:12}$	The twelve address inputs $\text{Addr}_{0:11}$ are used to access any of the 4,096 locations in either the A bank or B bank. If the MODE pin is high, pin A_{12} has no effect on the 71B221. In the MODE input is low, A_{12} is used to select the two RAM banks, and the device behaves as an 8K x 18 RAM . In the second case, the Output Enable inputs should be wired together, as should be the Write Enable inputs. When the address latch is in the transparent state, the address input pins are routed directly to both RAM banks. When the latch is in its latched state both RAM banks ignore subsequent changes on the address input pins. The latch is transparent at all times except for the duration of an internally generated delay after a rising edge on the Strobe input pin.
$\text{I/O}_{0:17}$	The input/output bus comprises eighteen signals whose functions are determined by the state of the control input pins. During Output Enables, the data from the RAM address pointed to by the address latch is output from the selected bank upon these pins. When either Write Enable is asserted, data from the input data latch can be written into the selected bank's RAM at the address contained within the address latch. When $\overline{\text{OEA}}$, $\overline{\text{WEA}}$, $\overline{\text{OEB}}$, and $\overline{\text{WEB}}$ are all inactive, the input/output pins are floated in a high-impedance state.

BiCameral™ CacheRAM™ 128K-BIT (4K x 18 x 2) FOR RISC CACHES

ADVANCE INFORMATION
IDT71B222

FEATURES:

- High speed supports fastest R3000 CPUs:
  - — 18, 25, 30ns
  - — Supports 33, 25, and 20 MHz
- BiCameral organization:
  - — Split instruction/data cache support,
  - — No bank-switching timing contention
- 4K depth for 32K-Byte caches
- Eighteen-bit width reduces overall chip count
- Internal address latch for each bank
- Popular 52-pin PLCC package
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

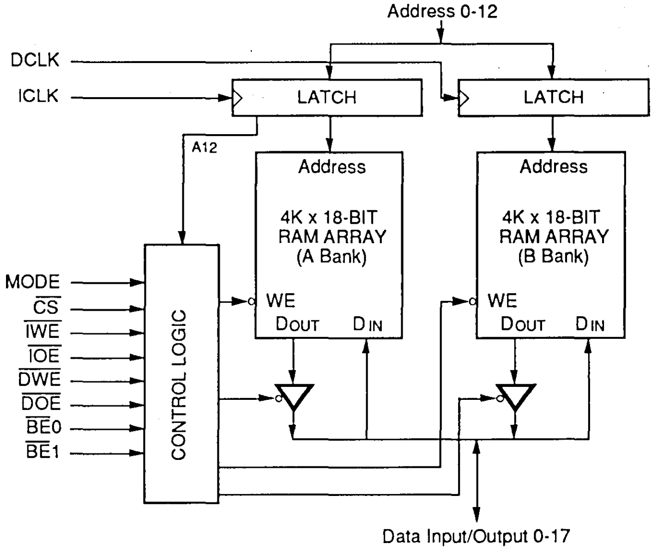
The IDT71B222 is a BiCameral CacheRAM specifically designed to support the split instruction and data caches of the IDT79R300 microprocessor. A complete 32K-Byte cache for the R3000 can be built with only three to four IDT71B222s (depending on the main memory size supported by the system) and will provide maximum throughput for CPU clock frequencies up to 40MHz. The PLCC package allows the designer to fit a 32K-Byte cache in the smallest circuit board area.

Internal address latches remove the need to use discrete devices to implement external instruction and data latches. The BiCameral (two bank) organization both reduces the number of devices required to support the R3000's split-cache architecture, and eliminates contention problems encountered when one RAM bank is being enabled while the other is being disabled. The very wide word (18 bits) further reduces chip count and board space consumption, while also minimizing address loading on the R3000's address output pins.

All timing parameters have been optimized to support the complete range of R3000 clock speeds, thus vastly simplifying design of R3000 caches.

Made with BiCEMOS™, IDT's advanced high-speed process, the IDT71B222 provides dense caches in low board space while consuming a minimum of power. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making the device ideally suited to military temperature applications requiring the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



2995 drw 01

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PIN DESCRIPTIONS

Name	Description
MODE	The MODE input, when high, causes the 7B1222's internal architecture to adopt a 4K x 18 x 2 format which is used to support split instruction/data caches. Taking the MODE input low reconfigures the 71B222 to an 8K x 18 architecture.
$\overline{\text{CS}}$	Chip Select is an input which globally gates the functioning of the 71B222. When Chip Select is low, the device functions according to the controls asserted on the other inputs. When Chip Select is high, all operation is suspended,
$\overline{\text{BE}}_{0:1}$	The Byte Enable inputs are used for byte reads and byte writes. BE0 allows reading or writing bits I/O$_{0:8}$, while BE$_1$ allows reading or writing bits I/O$_{9:17}$. These inputs are active low, and if disabled during a read cycle, the I/O pins they control will be left in a high-impedence state.
DCLK	The DCLK input, when high, allows the address inputs to flow through the D bank's address latch. Taking DCLK low freezes data in the D bank's address latch.
ICLK	Taking the ICLK input high allows the addresses to flow from the address inputs through the I bank's address latch. When ICLK is low the address in the I bank address latch is frozen.
$\overline{\text{IOE}}$	The I Output Enable input enables the data outputs from the I bank onto the data input/output pins. IOE must not be asserted simultaneously with the $\overline{\text{DOE}}$, $\overline{\text{DWE}}$, or $\overline{\text{IWE}}$ pins.
$\overline{\text{DOE}}$	This is an input which enables the data outputs from the D bank onto the data input/output pins. DOE must not be asserted simultaneously with the $\overline{\text{IOE}}$, $\overline{\text{IWE}}$, or $\overline{\text{DWE}}$ pins.
$\overline{\text{IWE}}$	The I Write Enable input, when low, gates data from the input/output pins into the RAM at the I bank address indicated by the output of the I bank address latch. Neither $\overline{\text{DOE}}$ nor $\overline{\text{IOE}}$ should be enabled during a write operation.
$\overline{\text{DWE}}$	D Write Enable is an input which is taken low to gate data from the input/output pins into the RAM at the D bank address being output from the D bank address latch. Neither $\overline{\text{DOE}}$ nor $\overline{\text{IOE}}$ should be enabled during a write operation.
Addr$_{0:12}$	The twelve address inputs Addr$_{0:11}$ are used to access any of the 4,096 locations in either the A bank or B bank. If the MODE pin is high, pin A$_{12}$ has no effect on the 71B222. If the MODE input is low, A$_{12}$ is used to select the two RAM banks, and the device behaves as an 8K x 18 RAM. In the second case, the Output Enable inputs should be wired together, as should be the Write Enable inputs. When an address latch is in the transparent state, the address input pins are routed directly to that address latch's RAM bank. When a latch is in its latched state its RAM bank ignores subsequent changes on the address input pins. The latch is transparent when its latch enable (ICLK or DCLK) input pin is high.
I/O$_{0:17}$	The input/output bus comprises eighteen signals whose functions are determined by the state of the $\overline{\text{IOE}}$, $\overline{\text{IWE}}$, $\overline{\text{DOE}}$, and $\overline{\text{DWE}}$ pins. During Output Enables, the data from the address pointed to by the address latch outputs of the selected bank's RAM is output upon these pins. When either Write Enable is asserted, data can be written from these pins into the selected bank's RAM at the address being output by that bank's address latch's output. When $\overline{\text{IOE}}$, $\overline{\text{IWE}}$, $\overline{\text{DOE}}$, and DWE are all inactive, the input/output pins are floated in a high-impedance state.

Integrated Device Technology, Inc.

BiCameral™ CacheRAM™ 256K-BIT (16K x 9 x 2) FOR RISC CACHES

ADVANCE INFORMATION
IDT71B229

FEATURES:

- High speed supports fastest R3000 CPUs:
  - 15, 22, 28ns
  - Supports 33, 25 and 20MHz
- BiCameral organization:
  - Split instruction/data cache support,
  - No bank-switching timing contention
- 16K depth for 128K-Byte caches
- Nine-bit width for parity
- Internal address latches
- Small (300 mil) 32-pin Plastic DIP and SOJ packages

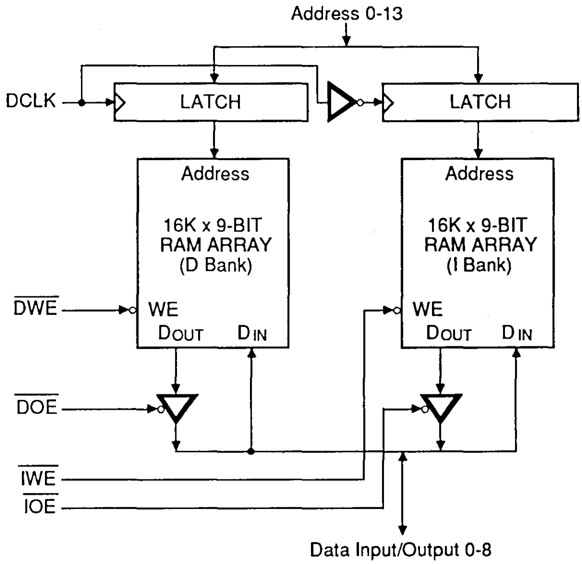
DESCRIPTION:

The IDT71B229 is a BiCameral CacheRAM specifically designed to support the split instruction and data caches of the IDT79R3000 microprocessor. A complete 128KByte cache for the R3000 can be built with only six to seven IDT71B229s (depending on the main memory size supported by the system) and will provide maximum throughput for CPU clock frequencies up to 33 MHz. The small 300 mil packages allow the designer to fit a 128KByte cache in a circuit board area under two square inches.

Internal address latches remove the need to use discrete devices to implement external instruction and data latches. The BiCameral (two bank) organization both reduces the number of devices required to support the R3000's split-cache architecture, and eliminates contention problems encountered when one RAM bank is being enabled while the other is being disabled. All timing parameters have been optimized to support the complete range of R3000 Clock speeds, thus vastly simplifying design of R3000 caches.

Made with BiCEMOS™, IDT's advanced high-speed process, the IDT71B229 provides dense caches in low board space while consuming a minimum of power.

FUNCTIONAL BLOCK DIAGRAM



2996 drw 01

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PIN DESCRIPTIONS

Name	Description
DCLK	The DCLK input, when high, allows the address inputs to flow through the D bank's address latch. Conversely, the address in the I bank's latch is held during a high input on DCLK. Taking DCLK low freezes data in the D bank's address latch, and allows addresses to flow through the I bank's address latch.
$\overline{\text{IOE}}$	The I Output Enable input enables the data outputs from the I bank onto the data input/output pins. $\overline{\text{IOE}}$ must not be asserted simultaneously with the $\overline{\text{DOE}}$, $\overline{\text{DWE}}$, or $\overline{\text{IWE}}$ pins.
$\overline{\text{DOE}}$	This is an input which enables the data outputs from the D bank onto the data input/output pins. $\overline{\text{DOE}}$ must not be asserted simultaneously with the $\overline{\text{IOE}}$, $\overline{\text{IWE}}$, or $\overline{\text{DWE}}$ pins.
$\overline{\text{IWE}}$	The I Write Enable input, when low, gates data from the input/output pins into the RAM at the I bank address indicated by the output of the I bank address latch. Neither $\overline{\text{DOE}}$ nor $\overline{\text{IOE}}$ should be enabled during a write operation.
$\overline{\text{DWE}}$	D Write Enable is an input which is taken low to gate data from the input/output pins into the RAM at the address being output from the D bank address latch. Neither $\overline{\text{DOE}}$ nor $\overline{\text{IOE}}$ should be asserted during a write operation.
Addr$_{0:1}$	The fourteen address inputs are used to access any of the 16,384 locations in either the D bank or I bank. When an address latch is in the transparent state, these pins are routed directly to that latch's RAM bank. Taking the latch into its latched state causes that RAM bank to ignore subsequent changes on the address input pins.
I/O$_{0:8}$	The input/output bus comprises nine signals whose functions are determined by the state of the $\overline{\text{IOE}}$, $\overline{\text{IWE}}$, $\overline{\text{DOE}}$, and $\overline{\text{DWE}}$ pins. During Output Enables, data is output upon these pins from the selected RAM bank from an address pointed to by the outputs of that bank's address latch. When either Write Enable is asserted, data can be written from these pins into the selected bank's RAM at the address being output by that bank's address latch. When $\overline{\text{IOE}}$, $\overline{\text{IWE}}$, $\overline{\text{DOE}}$, and $\overline{\text{DWE}}$ are all inactive, the input/output pins are floated in a high-impedance state.

TRUTH TABLE

DCLK	$\overline{\text{IOE}}$	$\overline{\text{IWE}}$	$\overline{\text{DOE}}$	$\overline{\text{DWE}}$	Addr$_{0:13}$	I/O$_{0:8}$	Function
L	H	H	L	H	Latched into D bank	Output D bank	Read data from D bank
L	H	H	H	L	Latched into D bank	Hi-Z	Write data to D bank
H	L	H	H	H	Latched into I bank	Output I bank	Read data trom I bank
H	H	L	H	H	Latched into I bank	Hi-Z	Write data to I bank
—	H	H	H	H	—	Hi-Z	No activity
—	L	L	X	X	—	—	Disallowed
—	L	X	L	X	—	—	Disallowed
—	L	X	X	L	—	—	Disallowed
—	X	L	L	X	—	—	Disallowed
—	X	L	X	L	—	—	Disallowed
—	X	X	L	L	—	—	Disallowed

NOTE:

1. L = Low, H = High, X = Don't Care, — = Unrelated, Hi-Z = High Impedence

Integrated Device Technology, Inc.

BiCMOS STATIC RAM 256K (32K x 8-BIT)

PRELIMINARY
IDT71B256

FEATURES:

- 32K x 8 BiCEMOS™ Static RAM
- High-speed address /chip select time
  - — Military: 20ns
  - — Commercial: 12/15/20ns
- One Chip Select plus one Output Enable pin
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Available in 28-pin sidebraze ceramic, 300 mil DIP; 300 mil plastic DIP and 28-pin, 300 mil plastic SOJ packages

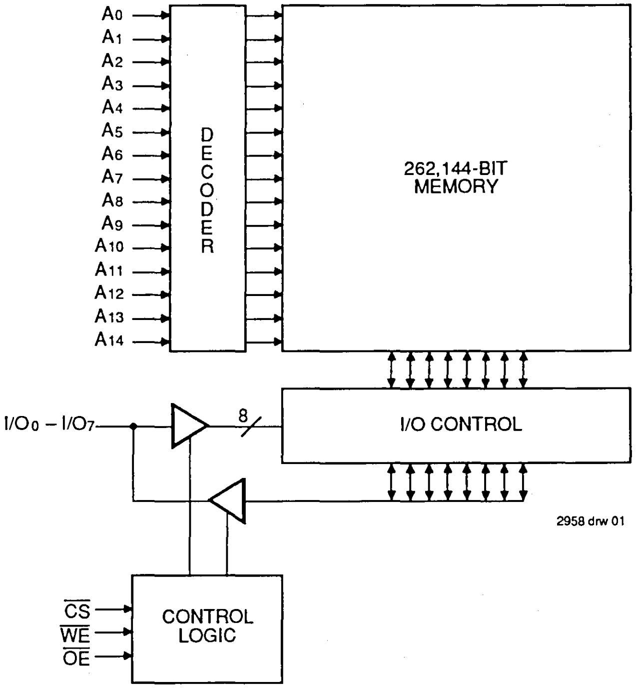
DESCRIPTION:

The IDT71B256 is a 262,144-bit high-speed static RAM organized as 32Kx8. It is fabricated using IDT's high-perfomance high-reliability BiCEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

Address access times as fast as 12ns are available with power consumption of only 550mW (typ.). All inputs and outputs of the IDT71B256 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT71B256 is packaged in a 28-pin, 300-mil sidebraze; 28-pin, 300 mil plastic DIP and 28-pin, 300-mil SOJ packages.

FUNCTIONAL BLOCK DIAGRAM



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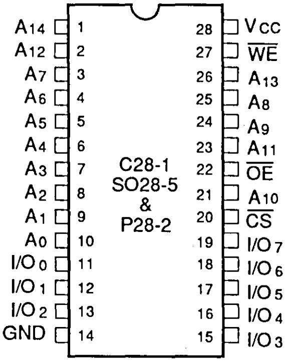
MILITARY AND COMMERCIAL TEMPERATURE RANGES **DECEMBER 1990**

PIN CONFIGURATION



2958 drw 02

DIP/SOJ
TOP VIEW

TRUTH TABLE[1]

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
L	L	H	D_{OUT}	Read
L	X	L	D_{IN}	Write
L	H	H	Hi-Z	Output Disabled
H	X	X	Hi-Z	Deselect Chip

NOTE: 2958 tbl 01

1. H = V_{IH}, L = V_{IL}, x = Don't care.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +125	°C
P_T	Power Dissipation	1.25	1.25	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2958 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Max.	Unit
C_{IN}	Input Capacitance	8	pF
C_{OUT}	Output Capacitance	12	pF

NOTE: 2958 tbl 03

1. This parameter is guaranteed by device characterization, but not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5	—	0.8	V

NOTE: 2958 tbl 04

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71B256			Unit
			Min.	Typ.[1]	Max.	
$\lvert I_{LI} \rvert$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	—	10	µA
$\lvert I_{LO} \rvert$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.	—	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.	—	—	0.4	
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	—	—	V

NOTE: 2958 tbl 05

1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS(1)

($V_{CC} = 5.0V \pm 10\%$)

Symbol	Parameter	71B256S12		71B256S15		71B256S20		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Dynamic Operating Current $\overline{CS} = V_{IL}$, Outputs Open, V_{CC} = Max., $f = f_{MAX}$(2)	200	—	190	—	180	190	mA

NOTES:

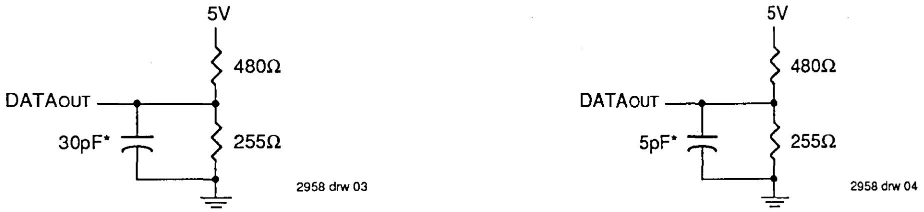
2958 tbl 05

1. All values are maximum guaranteed values.
2. $f_{MAX} = 1/t_{RC}$.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2958 tbl 06



*Including scope and jig

(for t_{OLZ}, t_{CLZ}, t_{OHZ}, t_{WHZ}, t_{CHZ}, t_{OW})

Figure 1. AC Test Loads

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

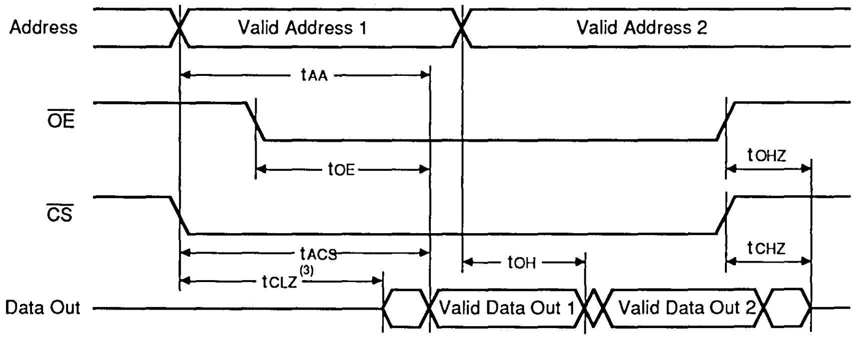
Symbol	Parameter	71B256-12(1)		71B256-15(1)		71B256-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	12	—	15	—	20	—	ns
t_{AA}	Address Access Time	—	12	—	15	—	20	ns
t_{ACS}	$\overline{CS}$ Access Time	—	8	—	9	—	12	ns
t_{CLZ}(2)	$\overline{CS}$ to Output in Low Z	3	—	4	—	5	—	ns
t_{CHZ}(2)	$\overline{CS}$ to Output in High Z	—	4	—	5	—	6	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	8	—	9	—	10	ns
t_{OLZ}(2)	$\overline{OE}$ to Output Low Z	3	—	4	—	5	—	ns
t_{OHZ}(2)	$\overline{OE}$ to Output High Z	—	4	—	5	—	6	ns
t_{OH}	Out Hold from Add Change	3	—	3	—	3	—	ns
Write Cycle								
t_{WC}	Write Cycle Time	12	—	15	—	20	—	ns
t_{AW}	Address to End of Write	9	—	10	—	12	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	9	—	10	—	12	—	ns
t_{CW}	$\overline{CS}$ to End of Write	8	—	9	—	10	—	ns
t_{WR}	Write Recovery	0	—	0	—	0	—	ns
t_{WHZ}(2)	$\overline{WE}$ to Out in High Z	—	5	—	6	—	7	ns
t_{DW}	Data Setup	5	—	6	—	8	—	ns
t_{DH}	Data Hold	2	—	2	—	2	—	ns
t_{OW}(2)	Output from End of Write	3	—	4	—	4	—	ns

NOTE:

2958 tbl 08

1. 0° to +70°C temperature range only.
2. This parameter is guaranteed, but not tested.

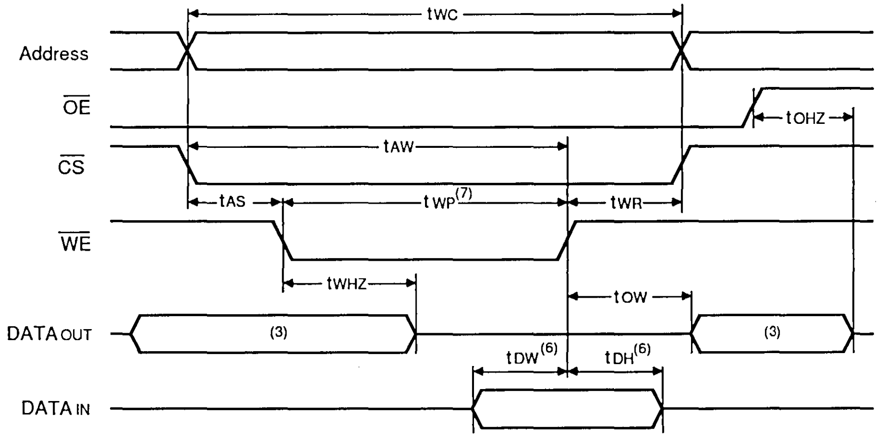
TIMING WAVEFORM OF READ CYCLE(1,2)



2958 drw 05

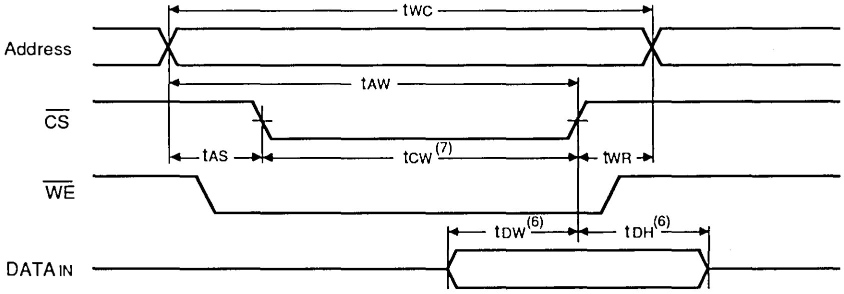
NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Address valid prior to or coincident with $\overline{CS}$ transition low.
3. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{\text{WE}}$ CYCLE)(1,2,4,5,6)



2958 drw 06

TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{\text{CS}}$ CYCLE)(1,2,4,5)

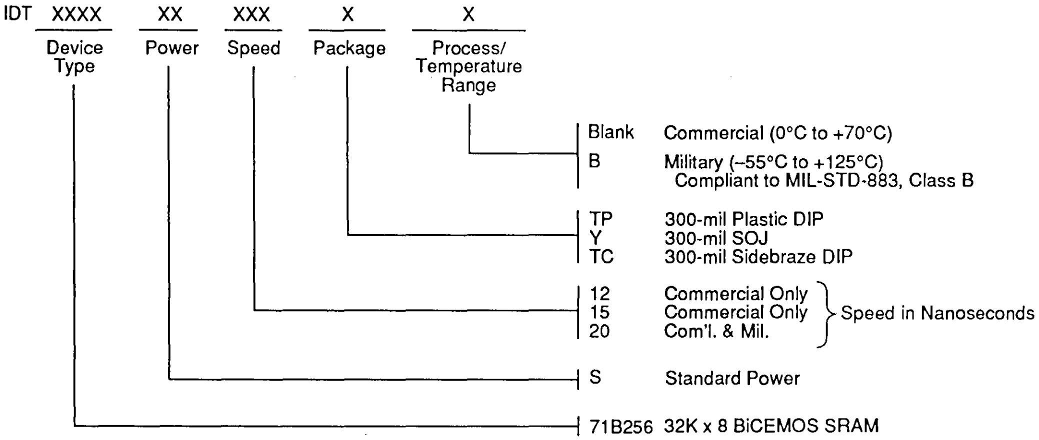


2958 drw 07

NOTES:

1. A write occurs during the overlap (t_{WC} and t_{WP}) of $\overline{\text{CS}}$ low and $\overline{\text{WE}}$ low.
2. t_{WF} is measured from the earlier of $\overline{\text{CS}}$ or $\overline{\text{WE}}$ being deasserted.
3. During this period, the I/O pins are in the output state, and input signals must not be applied on these pins.
4. If $\overline{\text{CS}}$ is asserted coincident with or after $\overline{\text{WE}}$ goes low, the output will remain in a high impedance state.
5. If $\overline{\text{CS}}$ is deasserted coincident with or before $\overline{\text{WE}}$ goes high, the output will remain in a high impedance state.
6. The transition is measured ±200mV from steady state with a 5pF load.
7. If $\overline{\text{OE}}$ is low during a $\overline{\text{WE}}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ}+t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{\text{OE}}$ is high during a $\overline{\text{WE}}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

ORDERING INFORMATION



2958 drw 08

Integrated Device Technology, Inc.

BiCMOS STATIC RAM 256K (64K x 4-BIT)

PRELIMINARY
IDT71B258

FEATURES:

- 64K x 4 BiCEMOS™ Static RAM
- High-speed address/chip select time
  - — Military: 15/20ns
  - — Commercial: 12/15/20ns
- Single chip select
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Available in 24-pin, 300 mil sidebraze ceramic DIP; 24-pin, 300 mil plastic DIP and 24-pin, 300 mil plastic SOJ packages

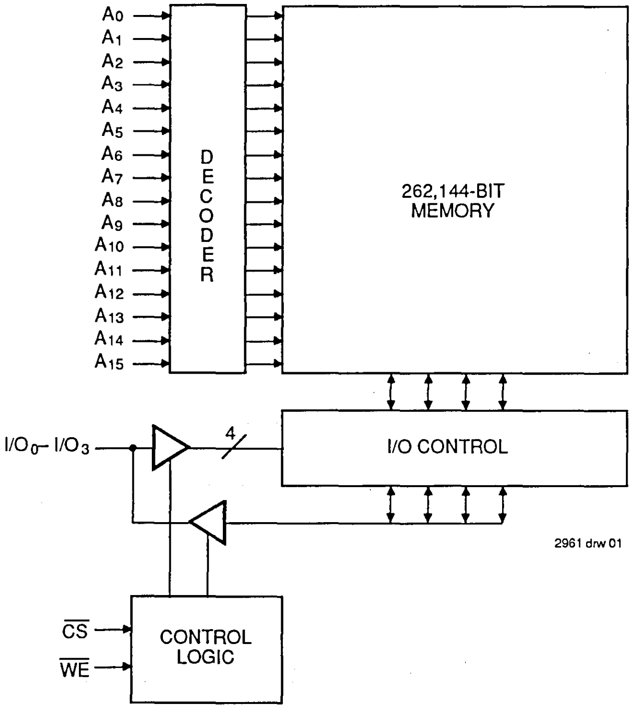
DESCRIPTION:

The IDT71B258 is a 262,144-bit high-speed static RAM organized as 64Kx4. It is fabricated using IDT's high-perfomance high-reliability BiCEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

Address access times as fast as 12ns are available with power consumption of only 450mW (typ.) All inputs and outputs of the IDT71B258 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

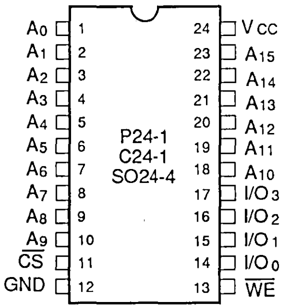
The IDT71B258 is packaged in a 24-pin, 300-mil sidebraze; 24-pin, 300 mil plastic DIP and a 24-pin SOJ packages.

FUNCTIONAL BLOCK DIAGRAM



2961 drw 01

PIN CONFIGURATION



2961 drw 02

DIP/SOJ
TOP VIEW

BiCEMOS is a trademark of Integrated Device Technology, Inc.

TRUTH TABLE[1]

$\overline{CS}$	$\overline{WE}$	I/O	Function
L	H	D_{OUT}	Read
L	L	D_{IN}	Write
H	X	Hi-Z	Deselect Chip

NOTE: 2961 tbl 01

1. H = V_{IH}, L = V_{IL}, X = Don't care.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5	—	0.8	V

NOTE: 2961 tbl 04

1. 1.5V undershoots are allowed for 10ns once per cycle.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Max.	Unit
C_{IN}	Input Capacitance	8	pF
C_{OUT}	Output Capacitance	12	pF

NOTE: 2961 tbl 03

1. This parameter is guaranteed by device characterization, but is not production tested.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +125	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2961 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71B258			Unit
			Min.	Typ.[1]	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.	—	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.	—	—	0.4	
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	—	—	V

NOTE: 2961 tbl 05

1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

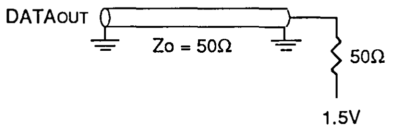
DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%)

Symbol	Parameter	71B258S12		71B258S15		71B258S20		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	180	—	160	170	140	150	mA

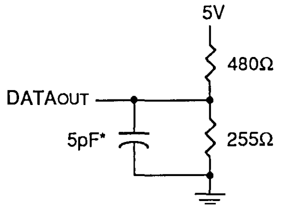
NOTES: 2961 tbl 05

1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC}.



2961 drw 03a

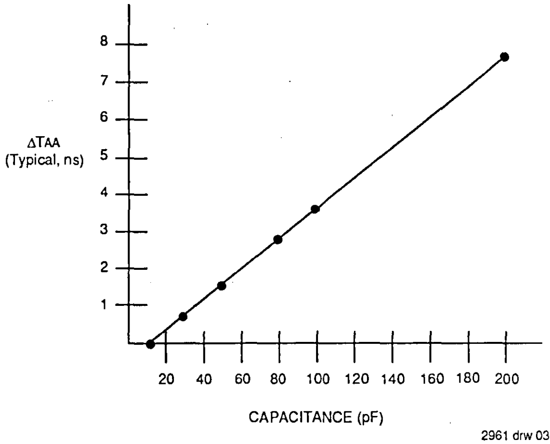
Figure 1A. AC Test Loads



2961 drw 03b

*Including jig and scope capacitance.

Figure 1B. AC Test Loads



2961 drw 03c

Figure 1C. Lumped Capacitive Load, Typical Derating

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1A, 1B & 1C

2961 tbl 06

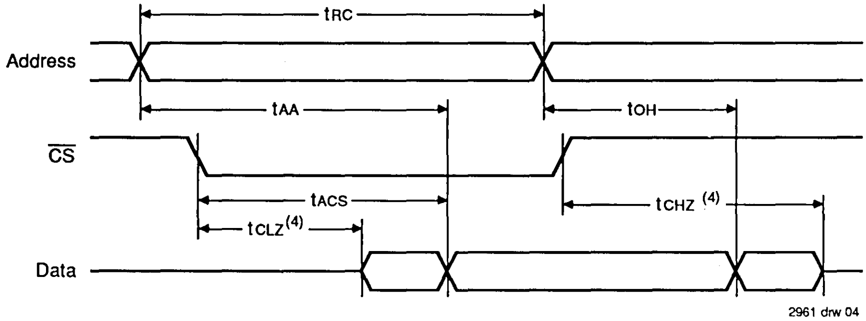
AC ELECTRICAL CHARACTERISTICS (VCC = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71B258-12[1]		71B258-15		71B258-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	12	—	15	—	20	—	ns
t_{AA}	Address Access Time	—	12	—	15	—	20	ns
t_{ACS}	$\overline{CS}$ Access Time	—	5	—	6	—	8	ns
t_{CLZ}[2]	$\overline{CS}$ to Output in Low Z	2	—	2	—	2	—	ns
t_{CHZ}[2]	$\overline{CS}$ to Output in High Z	—	5	—	6	—	7	ns
t_{OH}	Out Hold from Add Change	5	—	5	—	5	—	ns
Write Cycle								
t_{WC}	Write Cycle Time	12	—	15	—	20	—	ns
t_{CW}	Chip Select to End of Write	8	—	9	—	10	—	ns
t_{AW}	Add to End of Write	9	—	10	—	12	—	ns
t_{AS}	Address to $\overline{CS}$	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	9	—	10	—	12	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}[2]	$\overline{WE}$ to Output in High Z	—	5	—	6	—	7	ns
t_{DW}	Data Set-Up Time	5	—	6	—	8	—	ns
t_{DH}	Data Hold from Write	0	—	0	—	0	—	ns
t_{OW}	Out Active from End of $\overline{WE}$	2	—	2	—	2	—	ns

2961 tbl 08

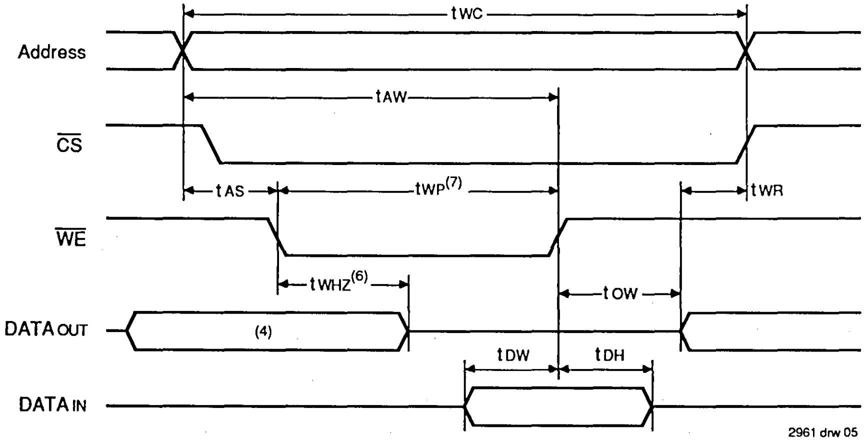
NOTES:
1. 0° to +70°C temperature range only.
2. This parameter is guaranteed with the AC Load, Figure 1B, and is not tested.

TIMING WAVEFORM OF READ CYCLE(1,2,3)



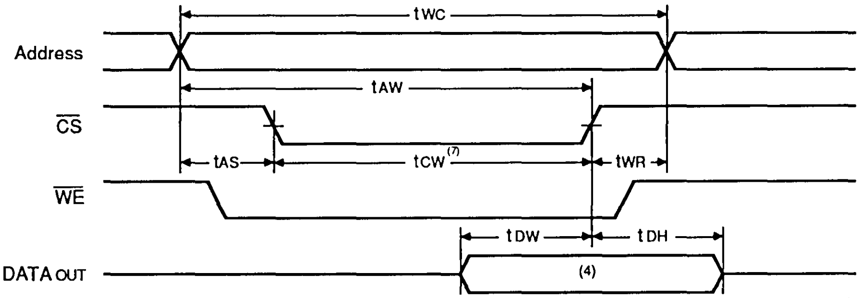
NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state with 5pF load (including scope and jig).

TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 5,6)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWC and tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).
7. During a $\overline{WE}$ controlled write cycle, the pulse width must be the larger of tWP or (tDW + tWHZ) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW.

TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ CONTROLLED TIMING)$^{(1, 2, 3, 5,6)}$

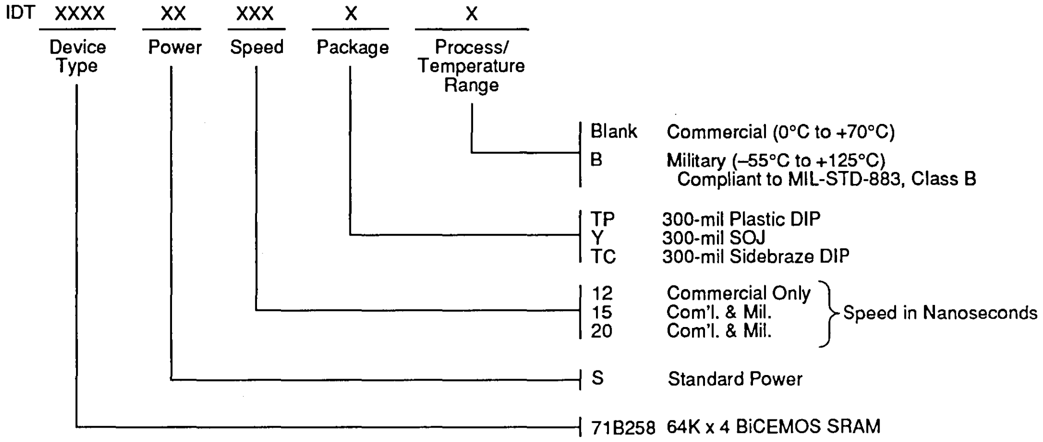


2961 drw 06

NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WC} and t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).
7. During a $\overline{WE}$ controlled write cycle, the pulse width must be the larger of t_{WP} or (t_{DW} + t_{WHZ}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}.

ORDERING INFORMATION



2961 drw 07

Integrated Device Technology, Inc.

32K x 8-BIT BiCMOS SRAM WITH ADDRESS LATCH

ADVANCE INFORMATION
IDT71B556

FEATURES:

- 32K x 8 BiCEMOS™ Static RAM with Address Latch
- High-speed address/chip select time
  - — Military: 20ns
  - — Commercial: 12/15/20ns
- Two Chip Selects plus one Output Enable pin
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Available in 32-pin sidebraze and plastic, 300 mil DIP and 32-pin, 300 mil SOJ packages
- Military product is fully compliant to MIL-STD-883, Class B

DESCRIPTION:

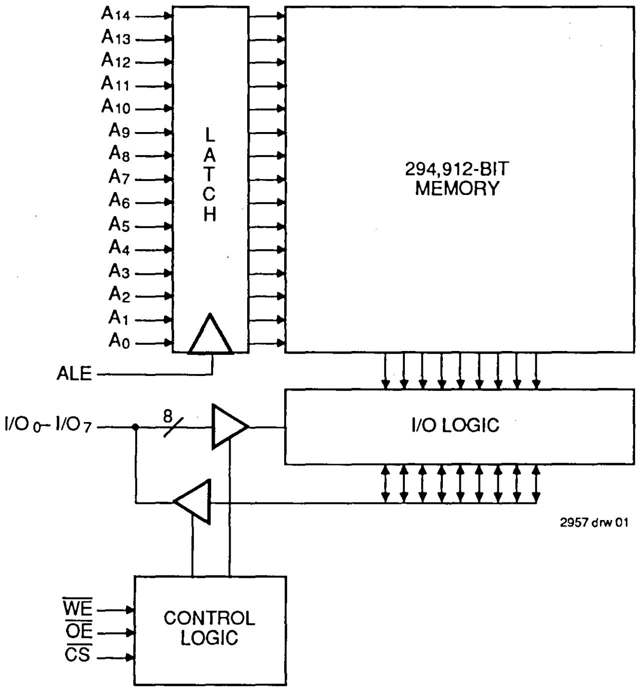
The IDT71B556 is a 256,144-bit high-speed static RAM organized as 32K x 8. It is fabricated using IDT's high perfomance high-reliability BiCEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

This memory is based on the standard 32K x 8 pinout and functionality, but also contains an address latch. When ALE is high the latch is transparent. When ALE is low, the address is latched.

Address access times as fast as 12 ns are available with power consumption of only 550mW (typ.). All inputs and outputs of the IDT71B556 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used.

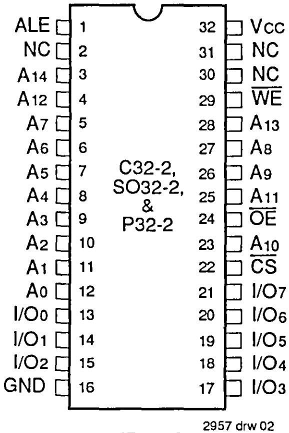
The IDT71B556 is packaged in a 32-pin, 300-mil sidebraze; 32-pin, 300 mil plastic DIP and a 32-pin SOJ package. The IDT71B556 military RAM is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP/SOJ
TOP VIEW

TRUTH TABLE[1]

CS_2	$\overline{CS}_1$	$\overline{OE}$	$\overline{WE}$	I/O	Function
X	H	X	X	Hi-Z	Deselect chip
L	L	X	X	Hi-Z	Deselect Chip
H	L	L	H	D_{OUT}	Read
H	L	X	L	D_{IN}	Write
H	L	H	X	Hi-Z	Output Disabled

NOTE: 2957 tbl 01

1. H = V_{IH}, L = V_{IL}, x = Don,t care.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +125	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2957 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Max.	Unit
C_{IN}	Input Capacitance	8	pF
C_{OUT}	Output Capacitance	12	pF

NOTE: 2957 tbl 03

1. This parameter is guaranteed by device characterization, but not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5	—	0.8	V

NOTE: 2957 tbl 04

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71556		Unit
			Min.	Max.	
$\lvert I_{LI} \rvert$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\lvert I_{LO} \rvert$	Output Leakage Current	V_{CC} = Max., CS = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.	—	0.4	
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	—	V

2957 tbl 05

DC ELECTRICAL CHARACTERISTICS[1]

(Vcc = 5.0V ± 10%)

Symbol	Parameter	71B556S12		71B556S15		71B556S20		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
Icc	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open, Vcc = Max., f = fMAX[3]	200	—	190	—	170	180	mA

NOTES:

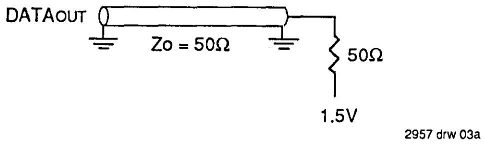
2957 tbl 06

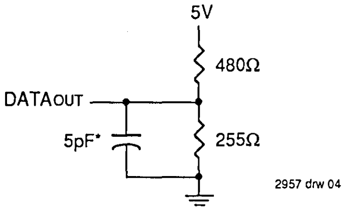
1. All values are maximum guaranteed values.
2. fMAX = 1/tRC.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1A, 1B & 1C

2957 tbl 07





*Including jig and scope capacitance.

Figure 1A. AC Test Load

Figure 1B.

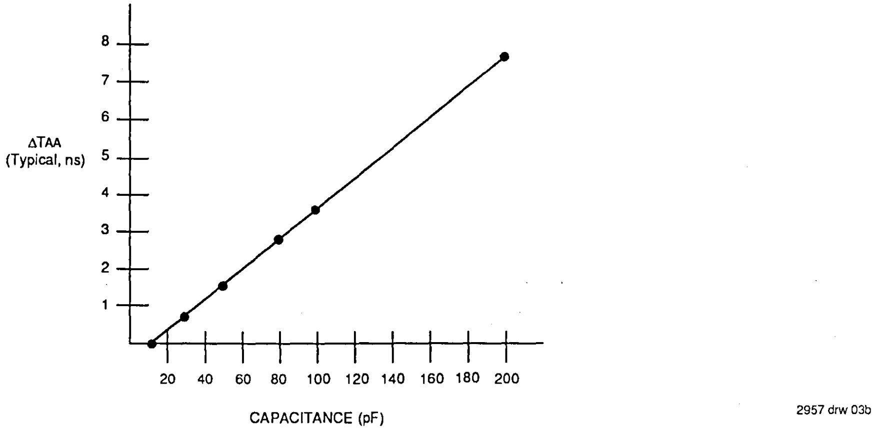


Figure 1C. Lumped Capacitive Load, Typical Derating

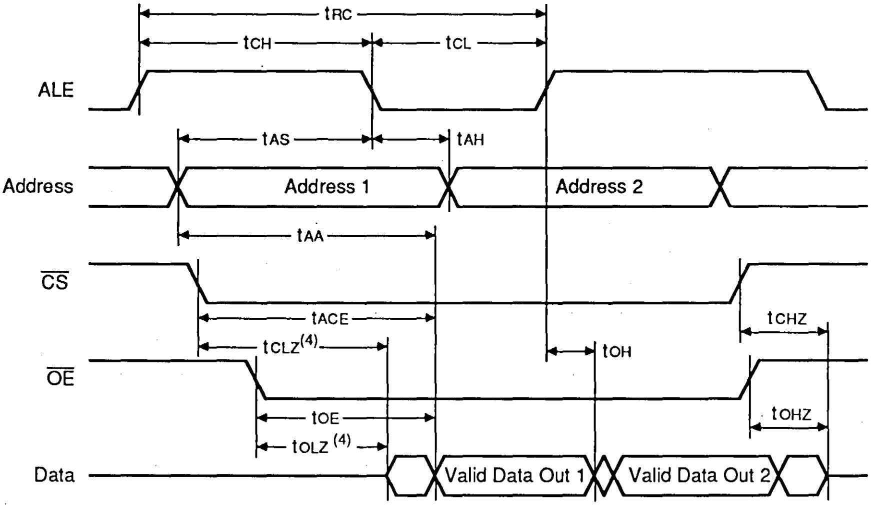
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71B556-12[1]		71B556-15[1]		71B556-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	12	—	15	—	20	—	ns
t_{CH}	ALE High	6	—	7	—	10	—	ns
t_{CL}	ALE Low	6	—	7	—	10	—	ns
t_{AS}	ALE Setup Time	4	—	4	—	5	—	ns
t_{AA}	Address Access Time	—	12	—	15	—	20	ns
t_{AH}	Address Latch Hold	3	—	4	—	5	—	ns
t_{ACS}	CS Access Time	—	7	—	8	—	10	ns
t_{OE}	Output Enable Time	—	7	—	8	—	10	ns
t_{CLZ}[2]	$\overline{CS}$ to Output in Low Z	3	—	4	—	5	—	ns
t_{CHZ}[2]	$\overline{CS}$ to Output in High Z	—	4	—	5	—	6	ns
t_{OLZ}[2]	$\overline{OE}$ to Output Low Z	3	—	4	—	5	—	ns
t_{OHZ}[2]	$\overline{OE}$ to Output High Z	—	4	—	5	—	6	ns
t_{OH}	Out Hold from Add Change	3	—	3	—	3	—	ns
Write Cycle								
t_{WC}	Write Cycle Time	12	—	15	—	20	—	ns
t_{CH}	ALE High	6	—	7	—	10	—	ns
t_{CL}	ALE Low	6	—	7	—	10	—	ns
t_{AS}	ALE Setup Time	0	—	0	—	0	—	ns
t_{AH}	ALE Hold TIme	3	—	4	—	5	—	ns
t_{AW}	Address to End of Write	9	—	10	—	12	—	ns
t_{ASW}	Address Setup Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	9	—	10	—	12	—	ns
t_{CW1}	$\overline{CS}$ to End of Write	8	—	9	—	10	—	ns
t_{WR1}	Write Recovery	0	—	0	—	0	—	ns
t_{WR2}	Write Recovery	-1	—	-1	—	-1	—	ns
t_{WHZ}[2]	$\overline{WE}$ to Output in High Z	—	5	—	6	—	7	ns
t_{DW}	Data Set-Up	6	—	8	—	10	—	ns
t_{DH}	Data Hold	2	—	2	—	2	—	ns
t_{OW}	Output from End of Write	3	—	4	—	4	—	ns

2957 tbl 08

NOTES:
1. 0° to +70°C temperature range only.
2. This parameter is guaranteed with the AC Load, Figure 1B, and is not tested.

TIMING WAVEFORM OF READ CYCLE(1,2,3)

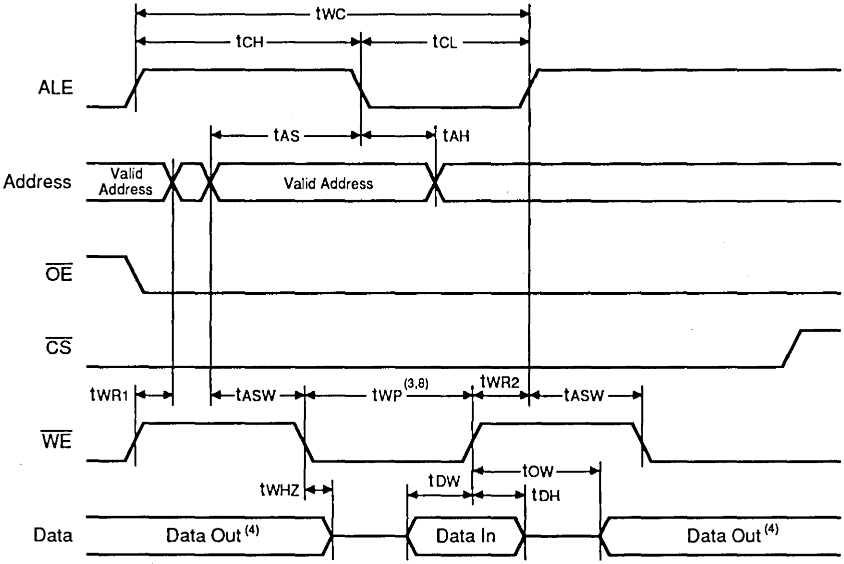


2957 drw 05

NOTES:

1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state with 5pF load (including scope and jig).

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)(1,2,5,6,7)

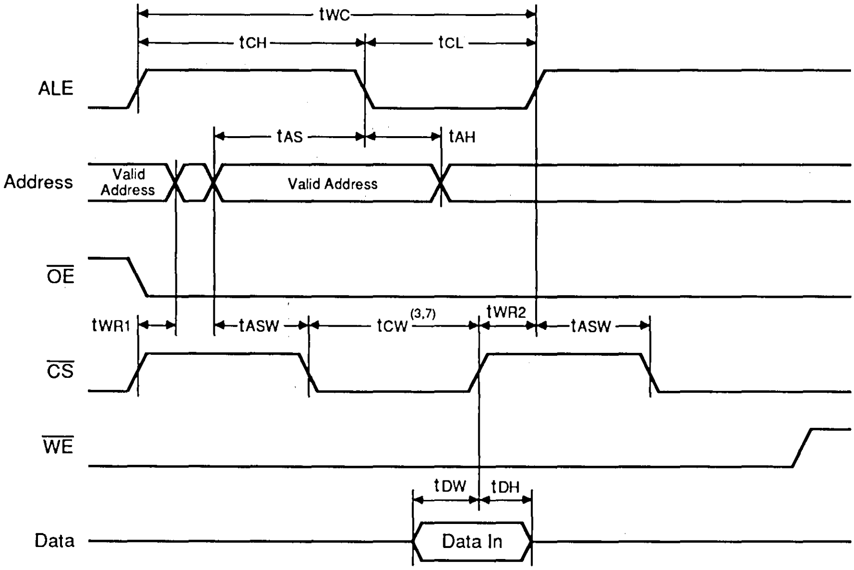


2957 drw 06

NOTES:

1. $\overline{OE}$ is low in order to show tWHZ and tOW.
2. A write occurs during the overlap (tWC and tWP) of $\overline{CS}$ low and $\overline{WE}$ low.
3. tWP is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ being deasserted.
4. During this period, the I/O pins are in the output state, and input signals must not be applied on these pins.
5. If $\overline{CS}$ is asserted coincident with or after $\overline{WE}$ goes low, the output will remain in a high impedance state.
6. If $\overline{CS}$ is deasserted coincident with or before $\overline{WE}$ goes high, the output will remain in a high impedance state.
7. The transition is measured ±200mV from steady state with a 5pF load.
8. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse width can be as rt as the specified tWP.

TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ Controlled)(1,2,4,5,6)

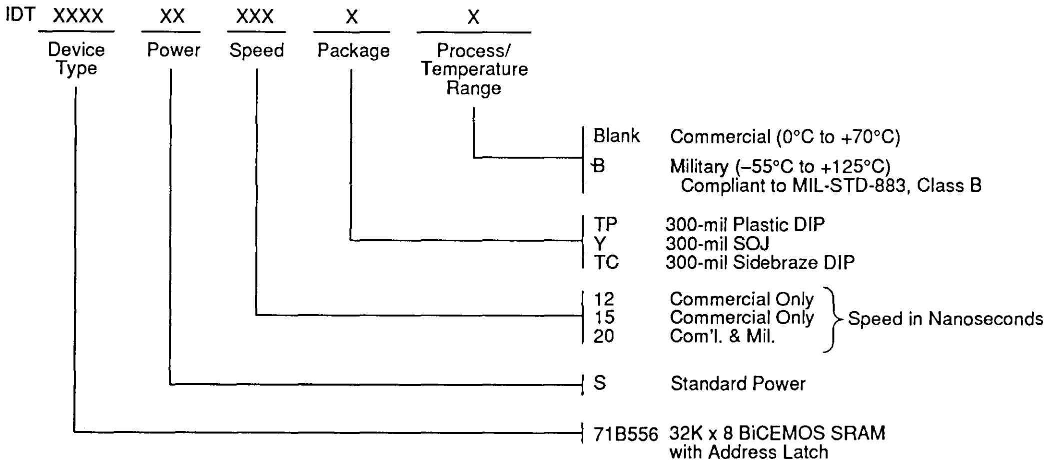


2957 drw 07

NOTES:

1. $\overline{OE}$ is low in order to show t_{WHZ} and t_{OW}.
2. A write occurs during the overlap (t_{WC} and t_{WP}) of $\overline{CS}$ low and $\overline{WE}$ low.
3. t_{WP} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ being deasserted.
4. If $\overline{CS}$ is asserted coincident with or after $\overline{WE}$ goes low, the output will remain in a high impedance state.
5. If $\overline{CS}$ is deasserted coincident with or before $\overline{WE}$ goes high, the output will remain in a high impedance state.
6. The transition is measured ±200mV from steady state with a 5pF load.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse width can be as short as the specified t_{WP}.

ORDERING INFORMATION



2957 drw 08

Integrated Device Technology, Inc.

BiCMOS HIGH-SPEED STATIC RAM 72K (8K x 9-BIT)
With Address Latches

ADVANCE INFORMATION
IDT71B569

FEATURES:

- 8192-words x 9-bits organization
- JEDEC standard 28-pin DIP and SOJ
- Fast access time:
  - — Commercial: 12/15/20ns
  - — Military: 15/20ns
- Produced with advanced BiCEMOS™ high-performance technology
- Single 5V power supply
- Inputs and outputs directly TTL compatible
- Latched address inputs
- High-speed BiCEMOS process
- Available in 28-pin, 300 mil plastic and SOJ packages

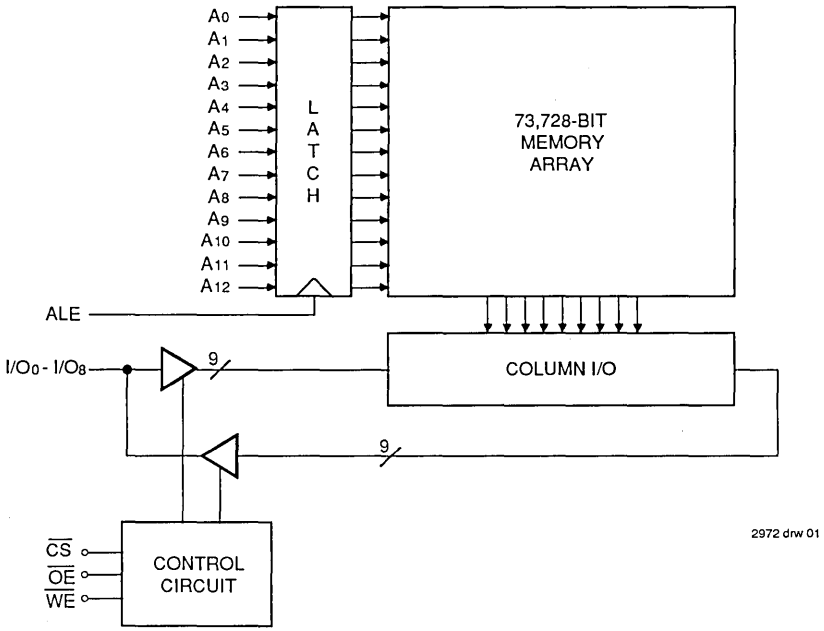
DESCRIPTION:

The IDT71B569 is a 73,728-bit high-speed static RAM, organized as 8K x 9, with address latches. It is fabricated using IDT's high-performance, high-reliability BiCEMOS technology.

The IDT71B569 offers address access times as fast as 12ns. The ninth bit is optimal for systems using parity. This device is ideally suited for cache memory applications.

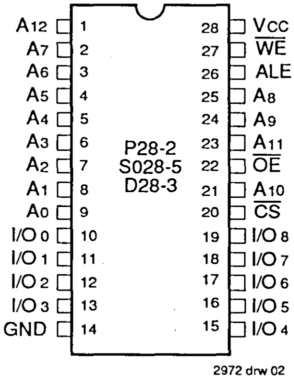
All inputs and outputs of the IDT71B569 are TTL-compatible. The IDT71B569 is packaged in an industry standard 300-mil, 28-pin DIP and SOJ.

FUNCTIONAL BLOCK DIAGRAM



BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



DIP/SOJ
TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2972 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2972 tbl 04

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2972 tbl 03

1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2972 tbl 05

1. 1.5V undershoots are allowed for 10ns once per cycle.

TRUTH TABLE

ALE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
X	H	X	X	Hi-Z	Deselect chip
H	X	X	X	X	Address Latch Transparent
L	X	X	X	X	Address Latch Closed
H	L	L	H	D_{OUT}	Read From Current Address
L	L	L	H	D_{OUT}	Read From Latched Address
H	L	X	L	D_{IN}	Write To Current Adress
L	L	X	L	D_{IN}	Write To Latched Adress
X	L	H	H	Hi-Z	Outputs Disabled

NOTE: 2972 tbl 01

1. H = V_{IH}, L = V_{IL}, X = Don't Care

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5.0V ± 10%)

Symbol	Parameter	71B569S12		71B569S15		71B569S20		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}(2)	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	170	—	170	190	150	170	mA

NOTES:

2972 tbl 06

1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71B569S		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
		I_{OL} = 10mA, V_{CC} = Min.	—	0.5	
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	—	V

2972 tbl 08

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1A, 1B & 1C

2972 tbl 07

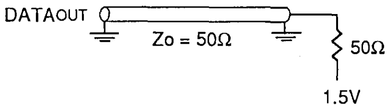
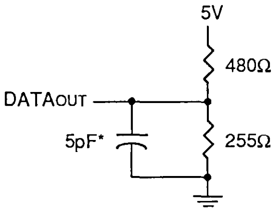


Figure 1A. AC Test Load

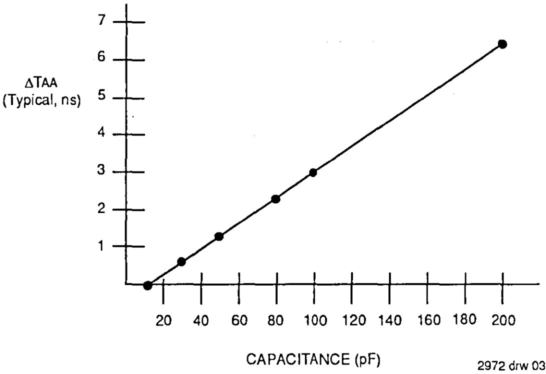
2972 drw 03a



2972 drw 04

*Includes jig and scope capacitance.

Figure 1B.



2972 drw 03b

Figure 1C. Lumped Capacitive Load, Typical Derating

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

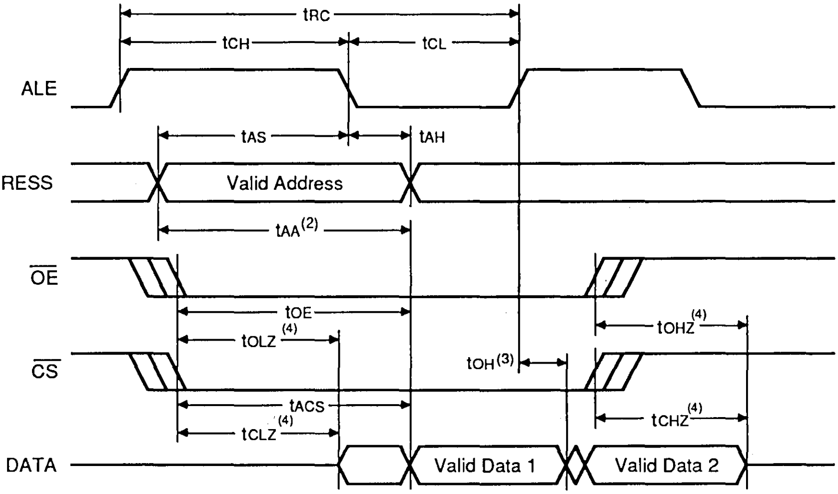
Symbol	Parameter	71B569S12(1)		71B569S15		71B569S20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	12	—	15	—	20	—	ns
t_{AA}	Address Access Time(3)	—	12	—	15	—	20	ns
t_{ACS}	Chip Select Access Time	—	12	—	15	—	20	ns
t_{CLZ}	Chip Select to Output in Low Z(2)	2	—	3	—	3	—	ns
t_{OE}	Output Enable to Output Valid	—	6	—	7	—	7	ns
t_{OLZ}	Output Enable to Output in Low Z(2)	2	—	3	—	3	—	ns
t_{CHZ}	Chip Deselect to Output High Z(2)	—	6	—	7	—	10	ns
t_{OHZ}	Output Disable to Output in High Z(2)	—	5	—	6	—	7	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{CH}	ALE High Time(2)	6	—	7	—	10	—	ns
t_{CL}	ALE Low Time(2)	6	—	7	—	10	—	ns
t_{AS}	Address Set-up Time to Address Latch Enable	3	—	3	—	5	—	ns
t_{AH}	Address Hold Time to Address Latch Enable	2	—	2	—	5	—	ns
Write Cycle								
t_{WC}	Write Cycle Time	12	—	15	—	20	—	ns
t_{AW}	Address Valid to End of Write	10	—	12	—	20	—	ns
t_{CW}	Chip Select to End of Write	10	—	12	—	15	—	ns
t_{ASW}	Address Set-up Time(3)	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	9	—	11	—	15	—	ns
t_{WR}	Write Recovery Time(3)	0	—	0	—	0	—	ns
t_{WHZ}	Write Enable to Output in High Z(2)	—	6	—	7	—	10	ns
t_{DW}	Data to Write Time Overlap	6	—	8	—	11	—	ns
t_{DH}	Data Hold Time from Write Time	0	—	0	—	0	—	ns
t_{OW}	Output Active from End of Write(2)	2	—	3	—	5	—	ns
t_{CH}	ALE High Time	6	—	7	—	10	—	ns
t_{CL}	ALE Low Time	6	—	7	—	10	—	ns
t_{AS}	Address Set-up Time to Address Latch Enable	3	—	3	—	5	—	ns
t_{AH}	Address Hold Time to Address Latch Enable	2	—	2	—	5	—	ns

2972 tbl 09

NOTES:

1. 0° to +70°C temperature range only.
2. This parameter is guaranteed with the AC Load, Figure 1B, and is not tested.
3. This measurement depends on the combination of ALE high plus an address change. This combination may either happen at the rising edge of ALE, or during an address change after ALE has become high.

TIMING WAVEFORM OF READ CYCLE (1)

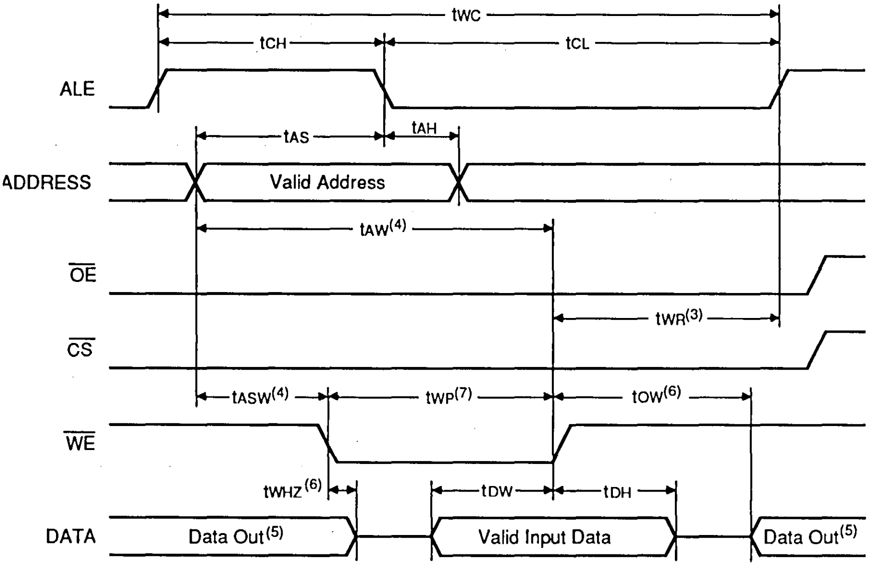


2972 drw 05

NOTES:

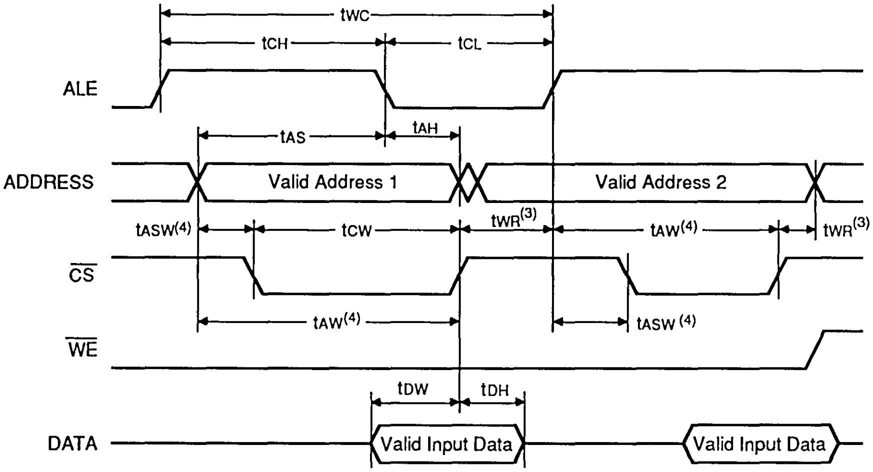
1. WE is high throughout a read cycle.
2. The parameter tAA is measured either from the first low to high transition of ALE after the read address has become valid, or from the stabilization of the read address during the period when ALE is high, which ever occurs last.
3. The parameter tOH is measured either from the first low to high transition of ALE after an address change, or from an address change during the period when ALE is high, whichever occurs first.
4. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(1,2)



2972 drw 06

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1,2)

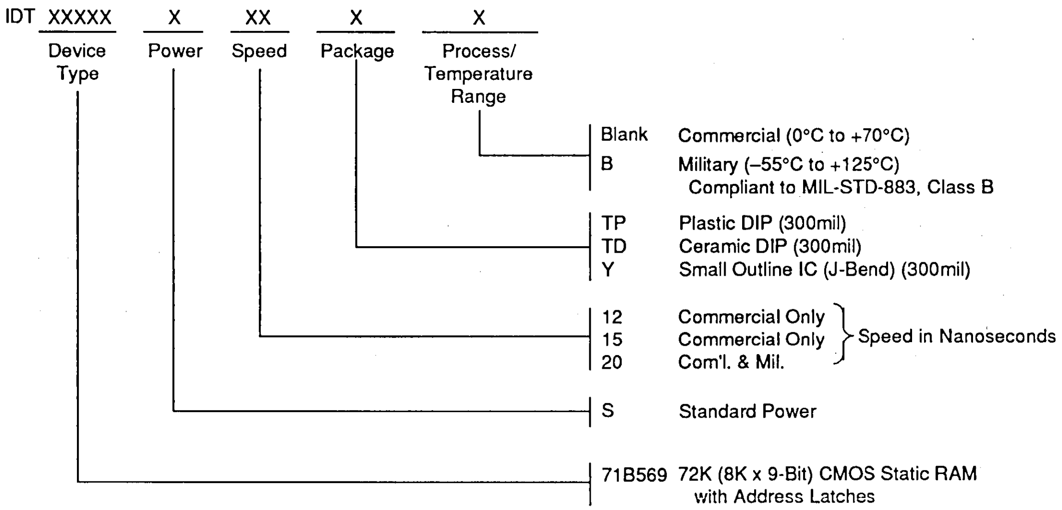


2972 drw 07

NOTES:

1. $\overline{WE}$ or $\overline{CE}$ must be high during all address transitions.
2. A write occurs during the overlap (tBW, tCW or tWP) of a low $\overline{CE}$ and a low $\overline{WE}$.
3. The parameter tWR is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high either to the first low to high transition of ALE after an address change, or to an address change during the period when ALE is high, whichever occurs last.
4. The parameters tASW and tAW are measured either from the first low to high transition of ALE after an address change has become valid, or from the stabilization of the valid write address during the period when ALE is high, whichever occurs first.
5. During this period, the I/O pins are in the output state so that the input signals must not be applied.
6. This transition is measured ±200mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the spectified tWP.

ORDERING INFORMATION



2972 drw 08

Integrated Device Technology, Inc.

BiCMOS HIGH-SPEED STATIC RAM 64K (8K x 8-BIT)

ADVANCE INFORMATION
IDT71B64

FEATURES:

- 8192-words x 8-bits organization
- JEDEC standard 28-pin DIP, SOJ, and 32-pin LCC
- Fast access time:
  - — Commercial: 10/12/15ns (max.)
  - — Military: 12/15/20ns (max.)
- Produced with advanced BiCEMOS™ high-performance technology
- Single 5V power supply
- Inputs and outputs directly TTL compatible
- Military product available compliant to MIL-STD-883, Class B

DESCRIPTION:

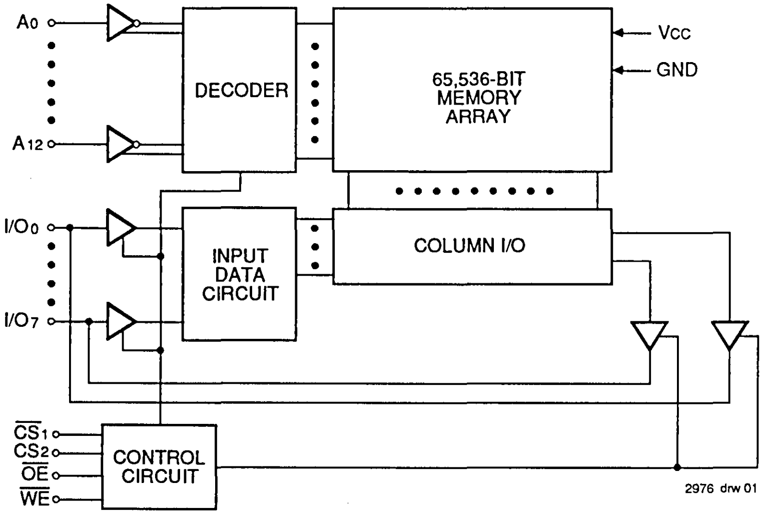
The IDT71B64 is a 65,536-bit high-speed static RAM organized as 8K x 8. It is fabricated using IDT's high-performance, high-reliability BiCEMOS technology.

The IDT71B64 offers address access times as fast as 10ns. All inputs and outputs of the IDT71B64 are TTL-compatible. The device has 2 chip selects for simplified address decoding.

The IDT71B64 is packaged in an industry standard 300-mil 28-pin DIP and SOJ, along with a 32-pin LCC package.

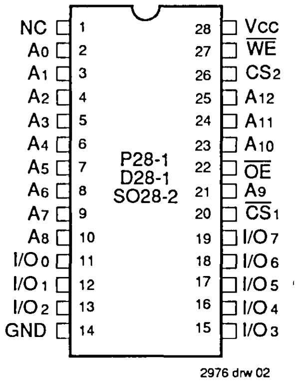
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

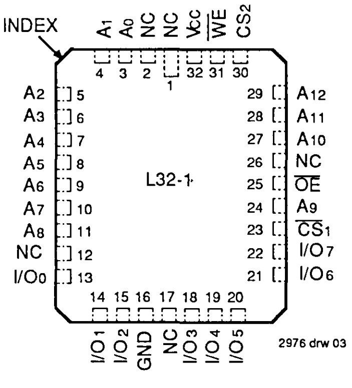


BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP/SOJ
TOP VIEW



32-PIN LCC
TOP VIEW

TRUTH TABLE[1]

CS_2	$\overline{CS}_1$	$\overline{OE}$	$\overline{WE}$	I/O	Function
X	H	X	X	High-Z	Deselect chip
L	X	X	X	High-Z	Deselect chip
H	L	L	H	D_{OUT}	Read
H	L	X	L	D_{IN}	Write
H	L	H	H	High-Z	Output disabled

NOTE: 2976 tbl 01

1. H = V_{IH}, L = V_{IL}, X = DON'T CARE

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +135	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2976 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2976 tbl 03

1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2976 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2976 tbl 04

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	71B64S10		71B64S12		71B64S15		71B64S20		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Dynamic Operating Current, $\overline{CS} = V_{IL}$, Outputs Open, V_{CC} = Max., $f = f_{MAX}$(2), $CS_2 = V_{IH}$	S	170	—	170	190	150	170	—	170	mA

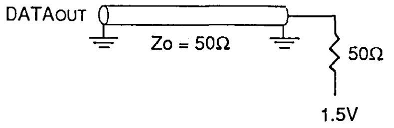
2976 tbl 05

NOTES:
1. All values are maximum guaranteed values.
2. At $f = f_{MAX}$ address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.

AC TEST CONDITIONS

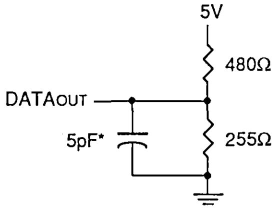
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1A, 1B & 1C

2976 tbl 06



2976 drw 04

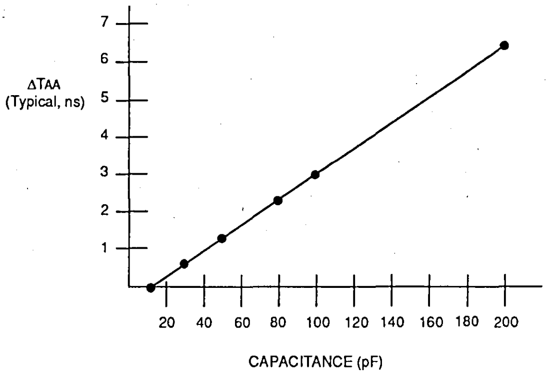
Figure 1A. AC Test Load



*Includes jig and scope capacitance.

2976 drw 05a

Figure 1B.



2976 drw 05b

Figure 1C. Lumped Capacitive Load, Typical Derating

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT71B64S Min.	IDT71B64S Max.	Unit
$\lvert I_{LI} \rvert$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL. COM'L.	— —	10 5	µA
$\lvert I_{LO} \rvert$	Output Leakage Current	V_{CC} = Max., $\overline{CS}_1$ = V_{IH}, CS_2 = V_{IL}, V_{OUT} = GND to V_{CC}	MIL. COM'L.	— —	10 5	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	0.4	
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	V

2976 tbl 07

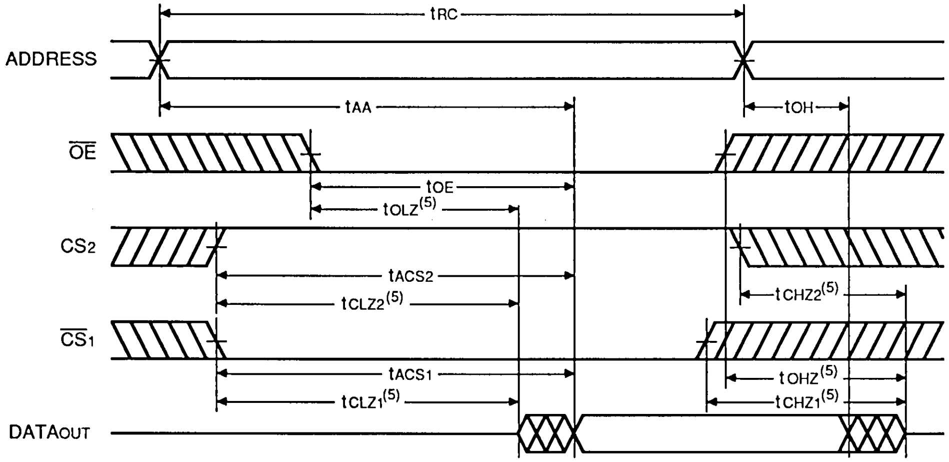
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71B64S10[1] Min.	71B64S10[1] Max.	71B64S12 Min.	71B64S12 Max.	71B64S15 Min.	71B64S15 Max.	71B64S20[2] Min.	71B64S20[2] Max.	Unit
Read Cycle										
t_{RC}	Read Cycle Time	10	—	12	—	15	—	20	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	—	19	ns
t_{ACS1}	Chip Select-1 Access Time[3]	—	10	—	12	—	15	—	20	ns
t_{ACS2}	Chip Select-2 Access Time[3]	—	10	—	12	—	15	—	20	ns
$t_{CLZ1,2}$	Chip Select-1, 2 to Output in Low Z[4]	2	—	2	—	3	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	5	—	6	—	7	—	9	ns
t_{OLZ}	Output Enable to Output in Low Z[4]	2	—	2	—	3	—	3	—	ns
$t_{CHZ1,2}$	Chip Select-1, 2 to Output in High Z[4]	—	5	—	6	—	7	—	8	ns
t_{OHZ}	Output Disable to Output in High Z[4]	—	4	—	5	—	6	—	8	ns
t_{OH}	Output Hold from Address Change	2	—	3	—	3	—	5	—	ns
Write Cycle										
t_{WC}	Write Cycle Time	10	—	12	—	15	—	20	—	ns
t_{AW}	Address Valid to End of Write	8	—	10	—	12	—	15	—	ns
t_{CW1}	Chip Select to End of Write ($\overline{CS}_1$)	8	—	10	—	12	—	15	—	ns
t_{CW2}	Chip Select to End of Write (CS_2)	7	—	9	—	12	—	15	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	7	—	9	—	12	—	15	—	ns
t_{WR1}	Write Recovery Time ($\overline{CS}_1$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
t_{WR2}	Write Recovery Time (CS_2)	0	—	0	—	0	—	0	—	ns
t_{WHZ}	Write Enable to Output in High Z[4]	—	5	—	6	—	7	—	8	ns
t_{DW}	Data Valid to End of Write	5	—	6	—	9	—	10	—	ns
t_{DH1}	Data Hold from Write Time ($\overline{CS}_1$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
t_{DH2}	Data Hold from Write Time (CS_2)	0	—	0	—	0	—	0	—	ns
t_{OW}	Output Active from End of Write[4]	2	—	2	—	3	—	5	—	ns

2976 tbl 08

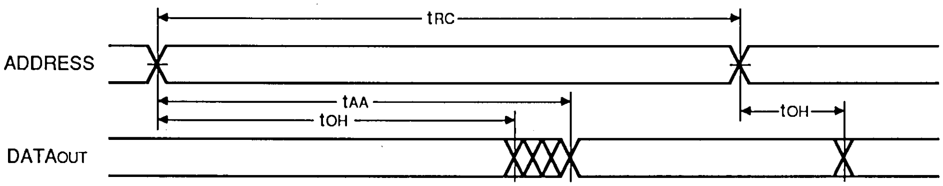
NOTES:
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Both chip selects must be active for the device to be selected.
4. This parameter is guaranteed with the AC Load, Figure 1B, and is not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



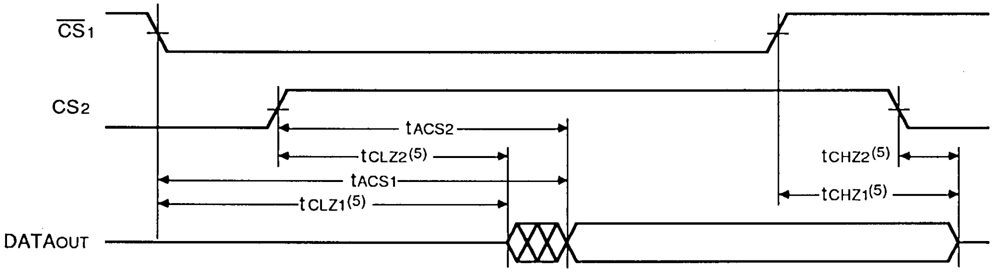
2976 drw 06

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2976 drw 07

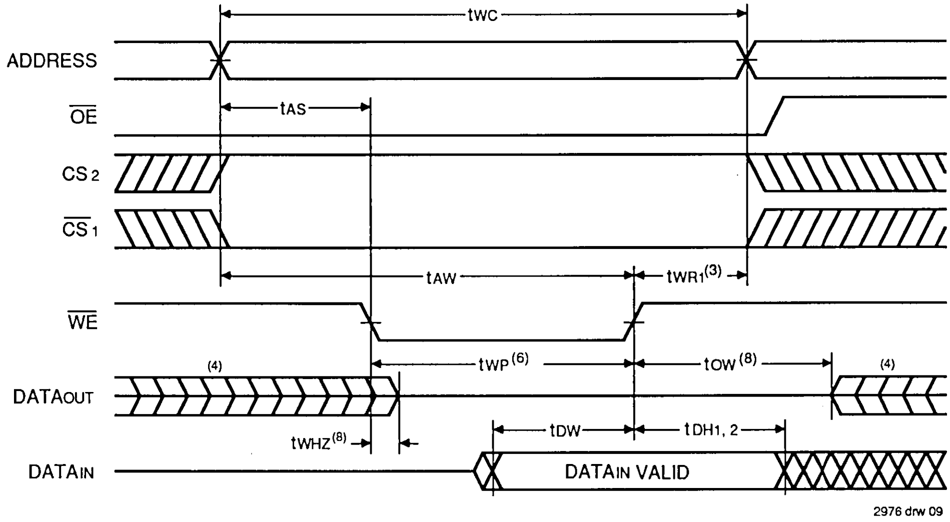
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



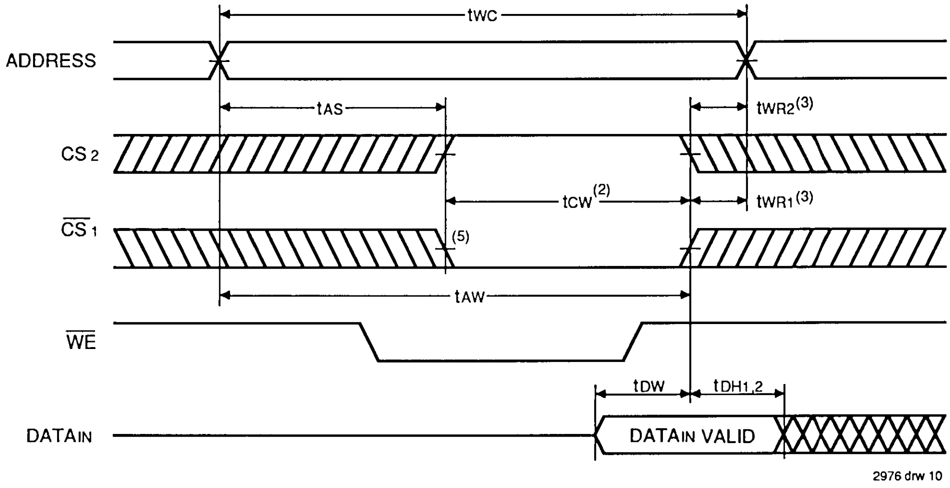
2976 drw 08

NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{CS}_1$ transition low and CS_2 transition high.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1)



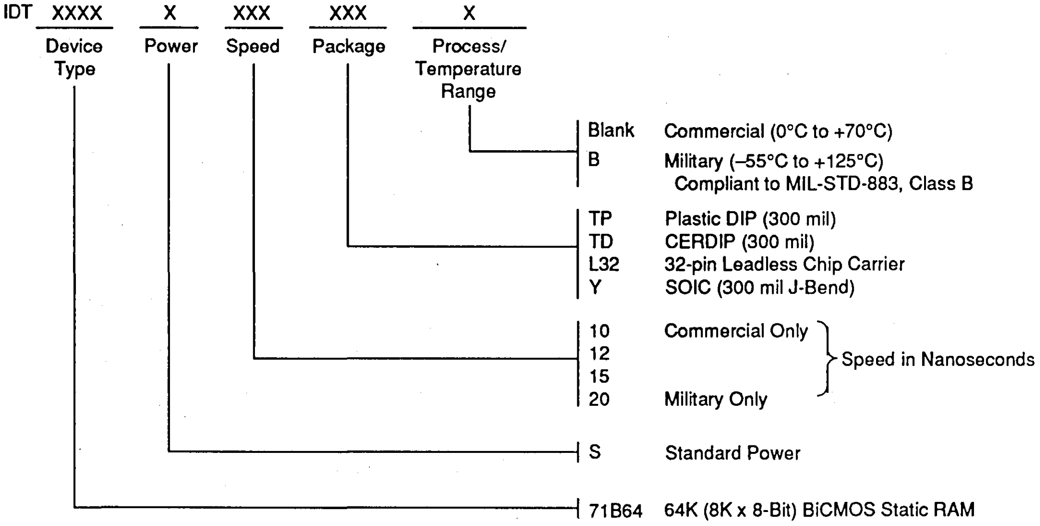
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1)



NOTES:

1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap of a low $\overline{CS}_1$ and a high CS_2.
3. $t_{WR1,2}$ is measured from the earlier of $\overline{CS}_1$ or $\overline{WE}$ going high or CS_2 going low to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS}_1$ low transition or CS_2 high transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} +t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the spectified t_{WP}.
7. DATAOUT is the same phase of write data of this write cycle.
8. Transition is measured ±200mV from steady state.

ORDERING INFORMATION



Process/Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B
Package	TP	Plastic DIP (300 mil)
	TD	CERDIP (300 mil)
	L32	32-pin Leadless Chip Carrier
	Y	SOIC (300 mil J-Bend)
Speed	10	Commercial Only
	12	
	15	
	20	Military Only
Power	S	Standard Power
Device Type	71B64	64K (8K x 8-Bit) BiCMOS Static RAM

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Integrated Device Technology, Inc.

BiCMOS STATIC RAM 64K (8K x 8-BIT) RESETTABLE RAM

ADVANCE INFORMATION
IDT71B65

FEATURES:

- High-speed asynchronous RAM clear on Pin 1 (clears all RAM bits to 0)
- High-speed address access time
  - — Commercial: 15/20/25ns (max.)
  - — Military: 20/25/35ns (max.)
- High-speed chip select ($\overline{CS}_1$) time
- Produced with BiCEMOS™ high-performance technology
- Single 5V(+10%) power supply
- Input and output directly TTL-compatible
- Standard 28-pin 300 mil DIP, 28-pin SOJ, 32-pin LCC

DESCRIPTION:

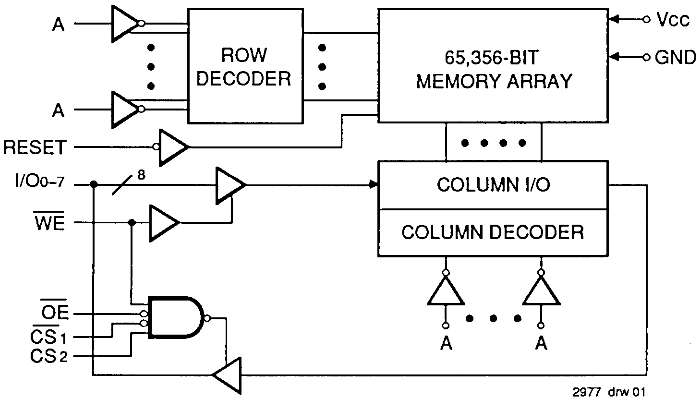
The IDT71B165 is a high-speed 65,536-bit static RAM, organized 8K x 8, with reset function. The $\overline{RESET}$ pin provides a single RAM clear control which clears all words in the internal RAM to zero when activated. This allows the memory bits for all locations to be cleared at power-on or system reset, or for a fast clear to be available to graphics, histogramming and other designs where a byte-by-byte RAM clear would cause noticeable system speed degradation.

This product Is fabricated using IDT's high-performance, high reliability BiCEMOS technology. Address access time of 15ns and chip select ($\overline{CS}_1$) time of 8ns are available.

All inputs and outputs of the IDT71B65 are TTL-compatible and the device operates from a single 5V supply, simplifying system designs.

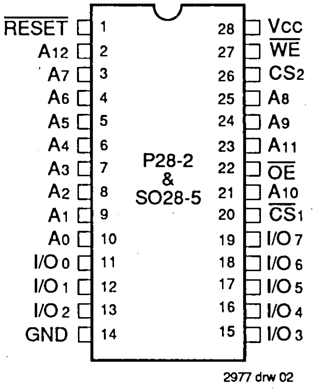
The IDT71B65 is packaged in a 32-pin LCC, a 28-pin 300 mil DIP and a 28-pin SOJ, providing high board level densities.

FUNCTIONAL BLOCK DIAGRAM

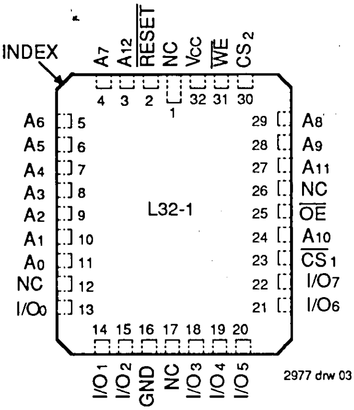


BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP/SOIC
TOP VIEW



LCC/PLCC
TOP VIEW

Integrated Device Technology, Inc.

BiCMOS HIGH-SPEED STATIC RAM 72K (8K x 9-BIT)

ADVANCE INFORMATION
IDT71B69

FEATURES:

- 8192-words x 9-bits organization
- Fast access time:
  - — Commercial: 12/15/20ns
  - — Military: 15/20ns
- Produced with advanced BiCEMOS™ high-performance technology
- JEDEC standard 28-pin DIP/SOJ and 32-pin LCC
- Single 5V power supply
- Inputs and outputs directly TTL compatible

DESCRIPTION:

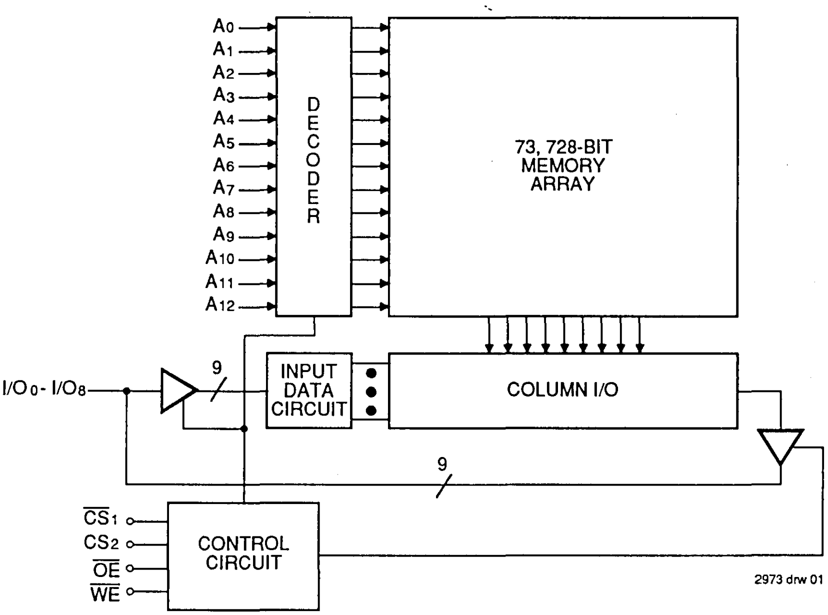
The IDT71B69 is a 73,728-bit high-speed static RAM, organized as 8K x 9. It is fabricated using IDT's high-performance, high-reliability BiCEMOS technology.

The IDT71B69 offers address access times as fast as 12ns. The ninth bit is optimal for systems using parity.

All inputs and outputs of the IDT71B69 are TTL-compatible. The device has 2 chip selects for simplified address decoding.

The IDT71B69 is packaged in an industry standard 300-mil 28-pin DIP/SOJ and 32-pin LCC.

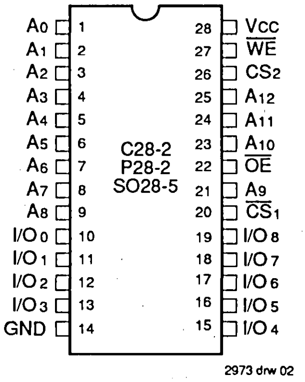
FUNCTIONAL BLOCK DIAGRAM



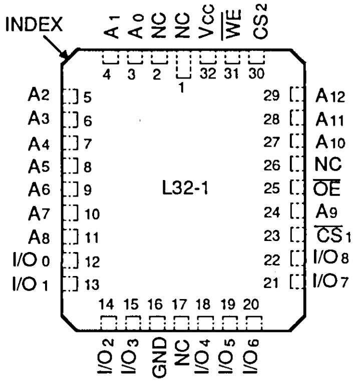
2973 drw 01

BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP/SOJ
TOP VIEW



LCC
TOP VIEW

TRUTH TABLE[1]

CS2	$\overline{CS_1}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
X	H	X	X	Hi-Z	Deselect chip
L	X	X	X	Hi-Z	Deselect chip
H	L	L	H	DOUT	Read
H	L	X	L	DIN	Write
H	L	H	H	Hi-Z	Output Disabled

NOTE: 2973 tbl 01

1. H = V_{IH}, L = V_{IL}, X = Don't Care.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +135	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2973 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2973 tbl 02

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2973 tbl 03

1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2973 tbl 05

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%)

Symbol	Parameter	71B69S12		71B69S15		71B69S20		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Dynamic Operating Current $\overline{CS}_1$ = V_{IL}, CS_2 = V_{IH}, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	180	—	180	—	180	190	mA

NOTES:

2958 tbl 05

1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC}.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71B69S		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}_1$ = V_{IH}, CS_2 = V_{IL} V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
		I_{OL} = 10mA, V_{CC} = Min.	—	0.5	
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	—	V

2973 tbl 08

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1A, 1B & 1C

2973 tbl 07

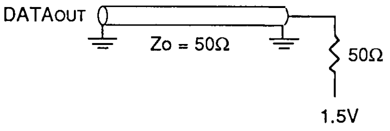
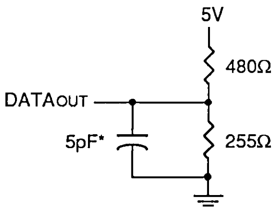


Figure 1A. AC Test Load



*Includes jig and scpe capacitance.

Figure 1B.

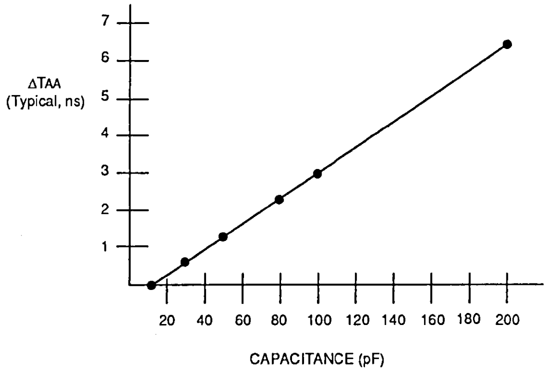


Figure 1C. Lumped Capacitive Load, Typical Derating

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

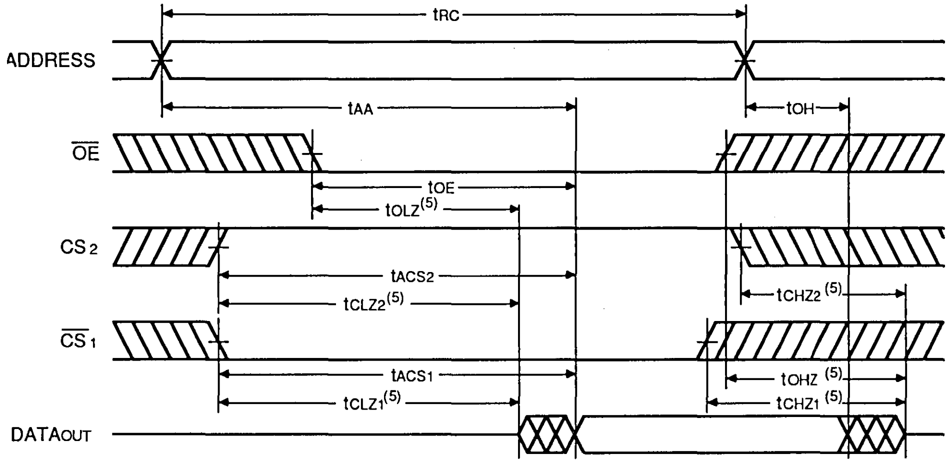
Symbol	Parameter	71B9S12(1)		71B69S15		71B69S20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	12	—	15	—	20	—	ns
t_{AA}	Address Access Time	—	12	—	15	—	20	ns
t_{ACS1}	Chip Select-1 Access Time	—	12	—	15	—	20	ns
t_{ACS2}	Chip Select-2 Access Time	—	12	—	15	—	20	ns
$t_{CLZ1,2}$	Chip Select to Output in Low Z(2)	2	—	3	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	6	—	7	—	9	ns
t_{OLZ}	Output Enable to Output in Low Z(2)	2	—	3	—	3	—	ns
$t_{CHZ1,2}$	Chip Select-1, 2 to Output in High Z(2)	—	6	—	7	—	8	ns
t_{OHZ}	Output Disable to Output in High Z(2)	—	5	—	6	—	8	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	5	—	ns
Write Cycle								
t_{WC}	Write Cycle Time	12	—	15	—	20	—	ns
t_{AW}	Address Valid to End of Write	10	—	12	—	15	—	ns
t_{CW1}	Chip Select to End of Write ($\overline{CS}_1$)	10	—	12	—	15	—	ns
t_{CW2}	Chip Select to End of Write (CS_2)	10	—	12	—	15	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	9	—	12	—	15	—	ns
t_{WR1}	Write Recovery Time ($\overline{CS}_1$, $\overline{WE}$)	0	—	0	—	0	—	ns
t_{WR2}	Write Recovery Time (CS_2)	—	0	—	3	—	5	ns
t_{WHZ}	Write Enable to Output in High Z(2)	—	6	—	7	—	8	ns
t_{DW}	Data Valid to End of Write	6	—	9	—	10	—	ns
t_{DH1}	Data Hold from Write Time ($\overline{CS}_1$, $\overline{WE}$)	0	—	0	—	0	—	ns
t_{DH2}	Data Hold from Write Time (CS_2)	0	—	0	—	0	—	ns
t_{OW}	Output Active from End of Write(2)	2	—	3	—	5	—	ns

2973 tbl 09

NOTES:

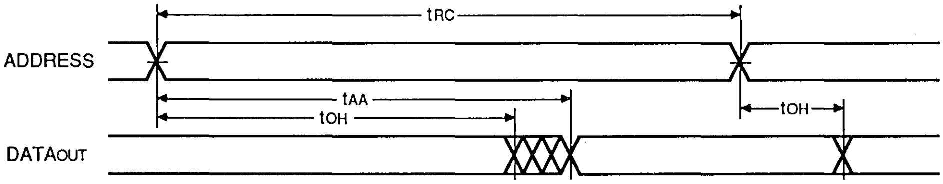
1. 0° to +70°C temperature range only.
2. This parameter is guaranteed with the AC Load, Figure 1B, and is not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1,3)



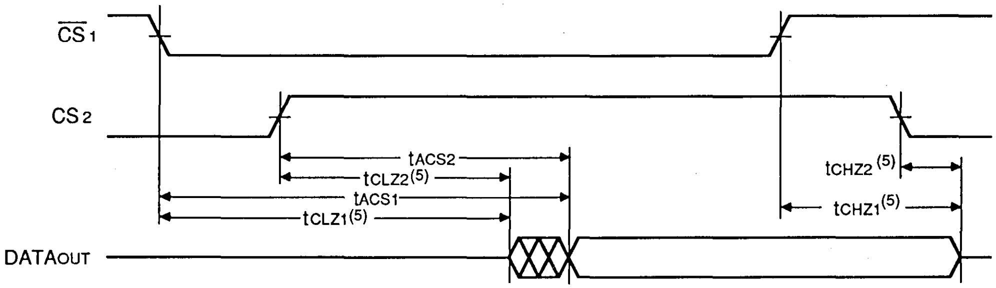
2973 drw 05

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2973 drw 06

TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)

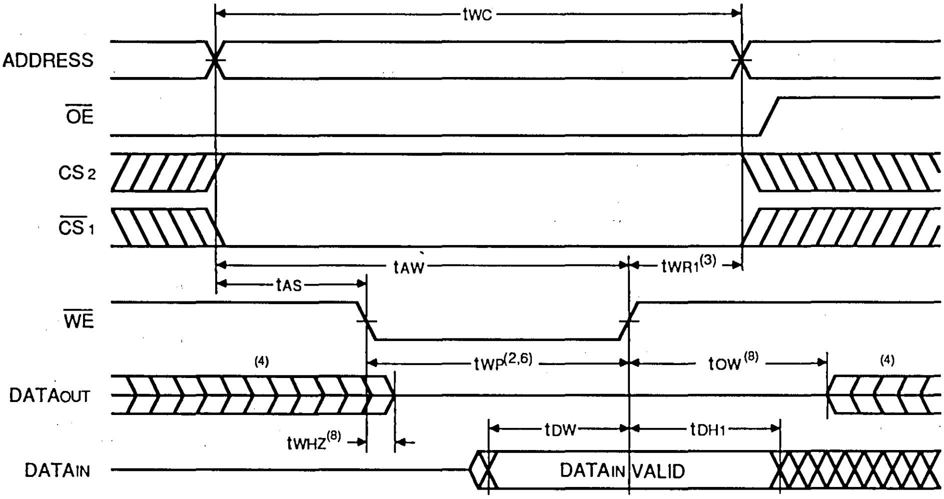


2973 drw 07

NOTES:

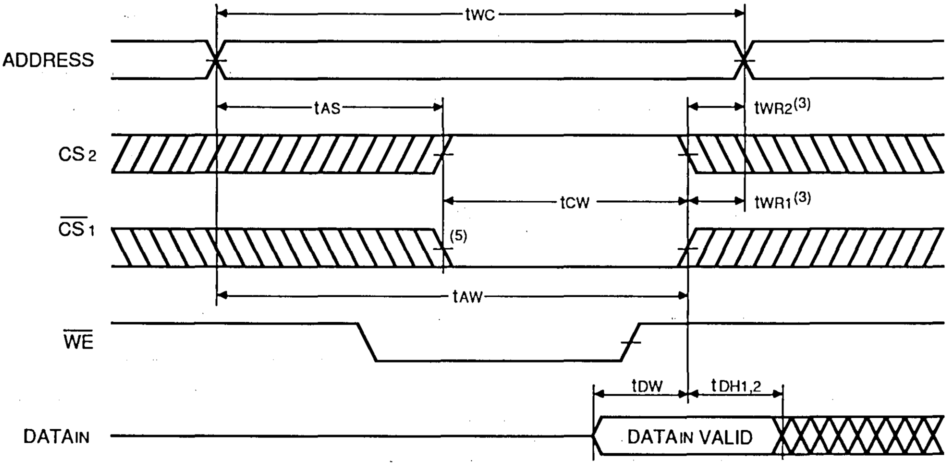
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{CS}_1$ transition low and CS_2 transition high.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{\text{WE}}$ CONTROLLED TIMING)(1)



2973 drw 08

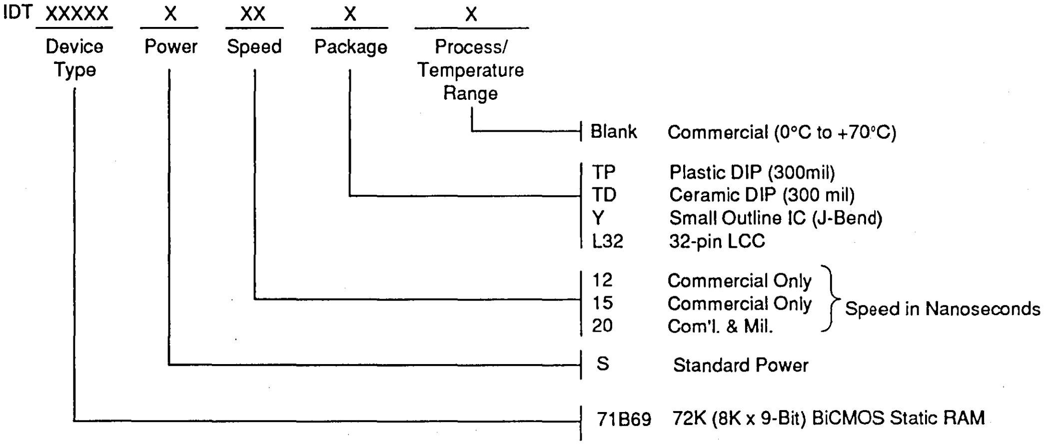
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{\text{CS}}$ CONTROLLED TIMING)(1)



2973 drw 09

NOTES:
1. $\overline{\text{WE}}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{\text{CS}}$1 and a high CS2.
3. tWR1, 2 is measured from the earlier of $\overline{\text{CS}}$1 or $\overline{\text{WE}}$ going high or CS2 going low to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{\text{CS}}$1 low transition or CS2 high transiton occurs simultaneously with or after the $\overline{\text{WE}}$ low transition, the outputs remain in a high impedance state.
6. If $\overline{\text{OE}}$ is low during a $\overline{\text{WE}}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ +tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{\text{OE}}$ is high during a $\overline{\text{WE}}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the spectified tWR.
7. DATAOUT is the same phase of write data of this write cycle.
8. Transition is measured ±200mV from steady state.

ORDERING INFORMATION



IDT XXXXX X XX X X

Field	Code	Description
Process/Temperature Range	Blank	Commercial (0°C to +70°C)
Package	TP	Plastic DIP (300mil)
	TD	Ceramic DIP (300 mil)
	Y	Small Outline IC (J-Bend)
	L32	32-pin LCC
Speed	12	Commercial Only
	15	Commercial Only
	20	Com'l. & Mil.
Power	S	Standard Power
Device Type	71B69	72K (8K x 9-Bit) BiCMOS Static RAM

2973 drw 10

Integrated Device Technology, Inc.

BiCMOS STATIC RAM
64K (8K x 8-BIT)
CACHE-TAG RAM

PRELIMINARY
INFORMATION
IDT71B74

FEATURES:

- High-speed address to MATCH comparison time
  - — Military: 15/18/25ns (max.)
  - — Commercial: 12/15/18ns (max.)
- High-speed address access time
  - — Military: 12/15/20ns (max.)
  - — Commercial: 10/12/15ns (max)
- High-speed chip select access time
  - — Military: 8/10/12ns (max.)
  - — Commercial: 6/8/10ns (max.)
- High-speed asynchronous RAM Clear on Pin 1
- Produced with advanced BiCEMOS™ high-performance technology
- Single 5V (+10%) power supply
- Input and output directly TTL-compatible
- Military product compliant to MIL-STD-883, Class B
- Standard 28-pin plastic and hermetic DIP (300 mil), 28-pin SOJ (300 mil)

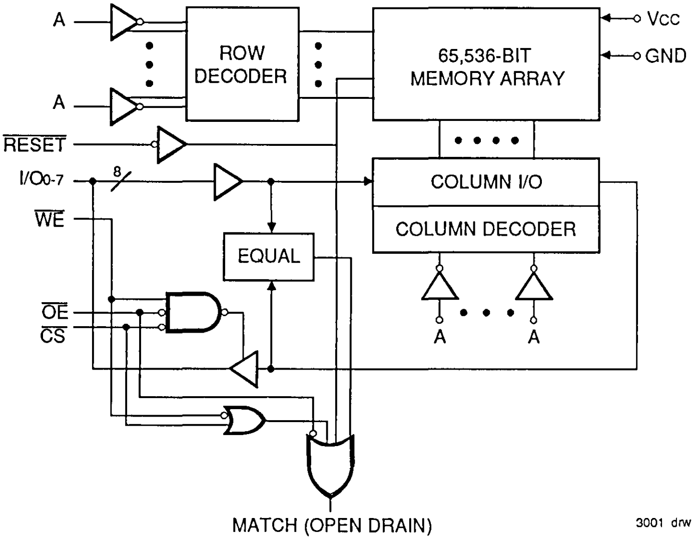
DESCRIPTION:

The IDT71B74 is a high-speed cache address comparator subsystem consisting of a 65,536-bit static RAM organized as 8K x 8 and an 8-bit comparator. A single IDT71B74 can map 8K cache words into a 1 megabyte address space by comparing 20 bits of address organized as 13 word cache address bits and 7 upper address bits. Two IDT71B74s can be combined to provide 28 bits of address comparison, etc. The IDT71B74 also provides a single RAM clear control, which clears all words in the internal RAM to zero when activated. This allows the tag bits for all locations to be cleared at power-on or system-reset, a requirement for cache comparator systems. The IDT71B74 can also be used as an 8K x 8 high-speed static RAM.

The IDT71B74 is fabricated using IDT's high-performance, high-reliability technology — CEMOS™. Address access times as fast as 12ns, chip select times of 6ns and address-to-comparison times of 10ns are available with maximum power consumption of 825mW.

The MATCH pin of several IDT71B74s can be wired-ORed together to provide enabling or acknowledging signals to the data cache or processor, thus eliminating logic delays and increasing system throughput. The device operates from a single 5V supply.

FUNCTIONAL BLOCK DIAGRAM



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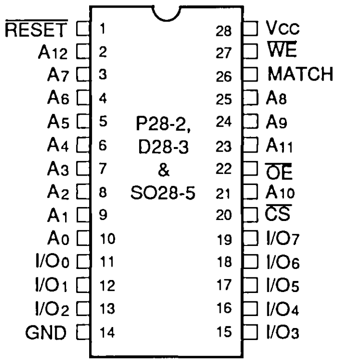
PIN CONFIGURATION



3001 drw 02

DIP/SOIC
TOP VIEW

TRUTH TABLE[1]

$\overline{\text{WE}}$	$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{RESET}}$	MATCH	I/O	Function
X	X	X	L	H	—	Reset all bits to low
X	H	X	H	H	Hi Z	Deselect chip
H	L	H	H	L	D_{IN}	No MATCH
H	L	H	H	H	D_{IN}	MATCH
H	L	L	H	H	D_{OUT}	Read
L	L	X	H	H	D_{IN}	Write

NOTE: 3001 tbl 01

1. H = V_{IH}, L = V_{IL}, X = DON'T CARE

PIN DESCRIPTIONS

A_{0-12}	Address
I/O_{0-7}	Data Input/Output
$\overline{\text{CS}}$	Chip Select
$\overline{\text{RESET}}$	Memory Reset
MATCH	Data/Memory Match (Open Drain)
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
GND	Ground
Vcc	Power

3001 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 3001 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 3001 tbl 04

1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage[1]	2.2	—	6.0	V
V_{IHR}	$\overline{\text{RESET}}$ Input Voltage	2.5[2]	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[3]	—	0.8	V

NOTE:

3001 tbl 05

1. All inputs except $\overline{\text{RESET}}$.
2. When using bipolar devices to drive the $\overline{\text{RESET}}$ input, a pullup resistor of 1kΩ-10kΩ is usually required to assure this voltage.
3. V_{IL} (min.) = -3.0V for pulse width less than 5ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

3001 tbl 06

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	71B74S12		71B74S15		71B74S18		71B74S25		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Dynamic Operating Current Outputs Open, V_{CC} = Max., f = f_{MAX}	190	—	170	190	150	170	—	170	mA

NOTE:

3001 tbl 07

1. All values are maximum guaranteed values.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMERATURE AND SUPPLY VOLTAGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition		IDT71B74S Min.	IDT71B74S Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	—	10	µA
			COM'L.	—	5	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	—	10	µA
			COM'L.	—	5	
V_{OL}	Output Low Voltage	I_{OL} = 18mA MATCH		—	0.5	V
		I_{OL} = 22mA MATCH		—	0.5	
		I_{OL} = 10mA, V_{CC} = Min. (Except MATCH)		—	0.5	
		I_{OL} = 8mA, V_{CC} = Min. (Except MATCH)		—	0.4	
V_{OH}	Output High Voltage	I_{OL} = -4mA, V_{CC} = Min. (Except MATCH)		2.4	—	V

3001 tbl 08

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 and 3

3001 tbl 09

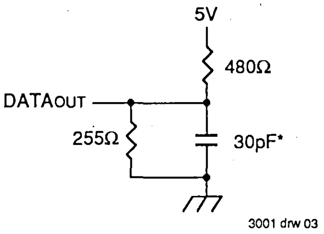


Figure 1. Output Load

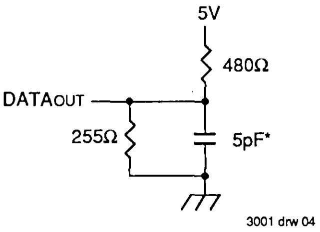
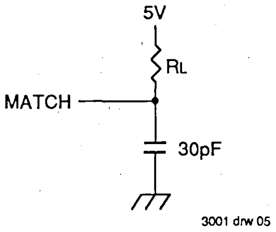


Figure 2. Output Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})



R_L = 200Ω (COM'L.)
= 270Ω (MIL.)

Figure 3. Output Load for MATCH

*Includes scope and jig.

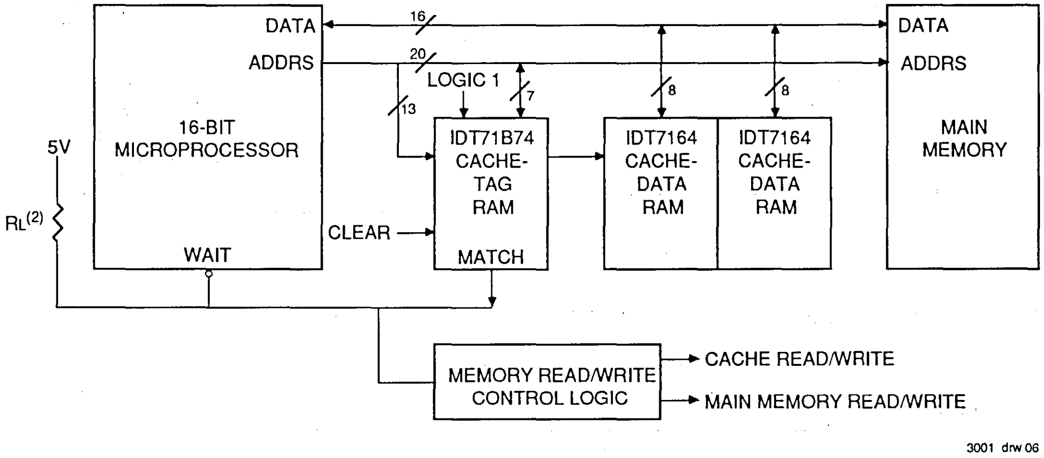


Figure 4. Example of Cache Memory System Block Diagram

NOTES:
1. For more information, see application note AN-07 "Cache-Tag RAM Chips Simplify Cache Memory Design".
2. R_L = 200Ω (commercial) or 270Ω (military).

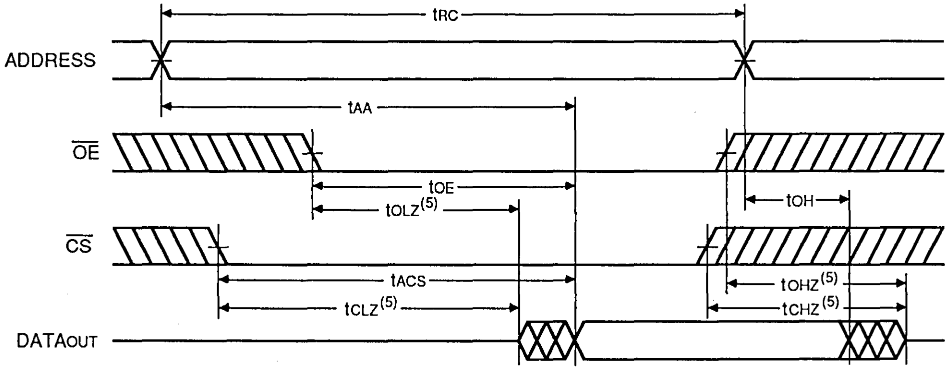
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71B74S12[1]		71B74S15		71B74S18		71B74S25[2]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
tRC	Read Cycle Time	10	—	12	—	15	—	20	—	ns
tAA	Address Access Time	—	10	—	12	—	15	—	20	ns
tACS	Chip Select Access Time	—	6	—	6	—	8	—	10	ns
tCLZ	Chip Select to Output in Low Z[3]	2	—	2	—	3	—	5	—	ns
tOE	Output Enable to Output Valid	—	6	—	7	—	8	—	10	ns
tOLZ	Output Enable to Output in Low Z[3]	2	—	3	—	3	—	3	—	ns
tCHZ	Chip Select to Output in High Z[3]	—	5	—	6	—	7	—	8	ns
tOHZ	Output Disable to Output in High Z[3]	—	4	—	6	—	6	—	8	ns
tOH	Output Hold from Address Change	2	—	3	—	3	—	3	—	ns

3001 tbl 10

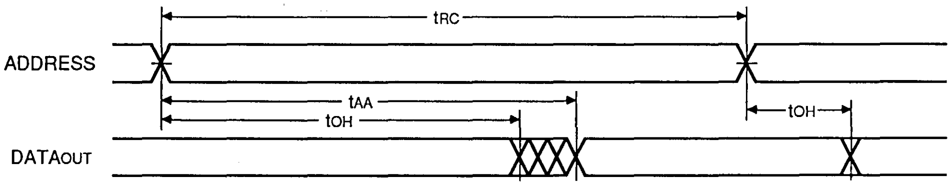
NOTES:
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed, but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1[1]



3001 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2[1, 2, 4]



3001 drw 08

NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

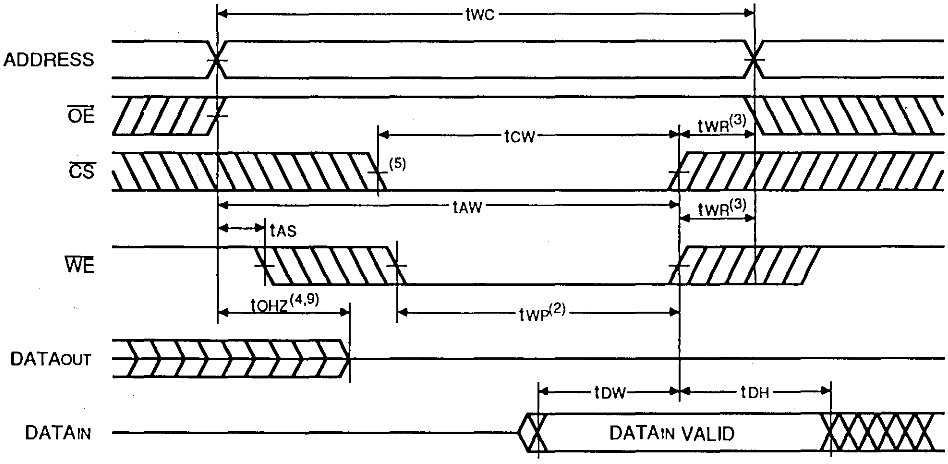
Symbol	Parameter	71B74S12(1)		71B74S15		71B74S18		71B74S25(2)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle										
tWC	Write Cycle Time	10	—	12	—	15	—	20	—	ns
tCW	Chip Select to End of Write	8	—	10	—	12	—	15	—	ns
tAW	Address Valid to End of Write	8	—	10	—	12	—	15	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	7	—	9	—	12	—	15	—	ns
tWR	Write Recovery Time ($\overline{CS}$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
tWHZ	Write Enable to Output in High Z(3)	—	5	—	6	—	7	—	8	ns
tDW	Data Valid to End of Write	5	—	6	—	9	—	10	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
tOW	Output Active from End of Write(3)	2	—	2	—	3	—	5	—	ns

NOTES:

3001 tbl 0?

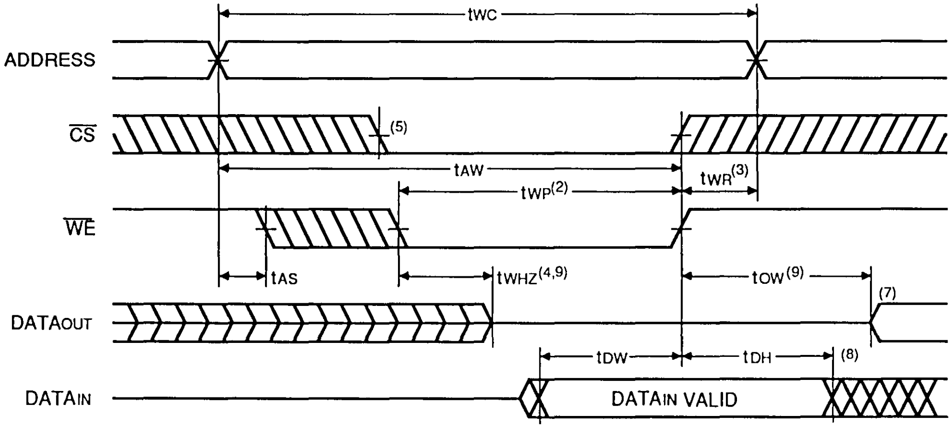
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1(1)



3001 drw 10

TIMING WAVEFORM OF WRITE CYCLE NO. 2(1, 6)



3001 drw 11

NOTES:
1. $\overline{WE}$, $\overline{CS}$ must be inactive during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{WE}$ and a low $\overline{CS}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. DATAOUT is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state.

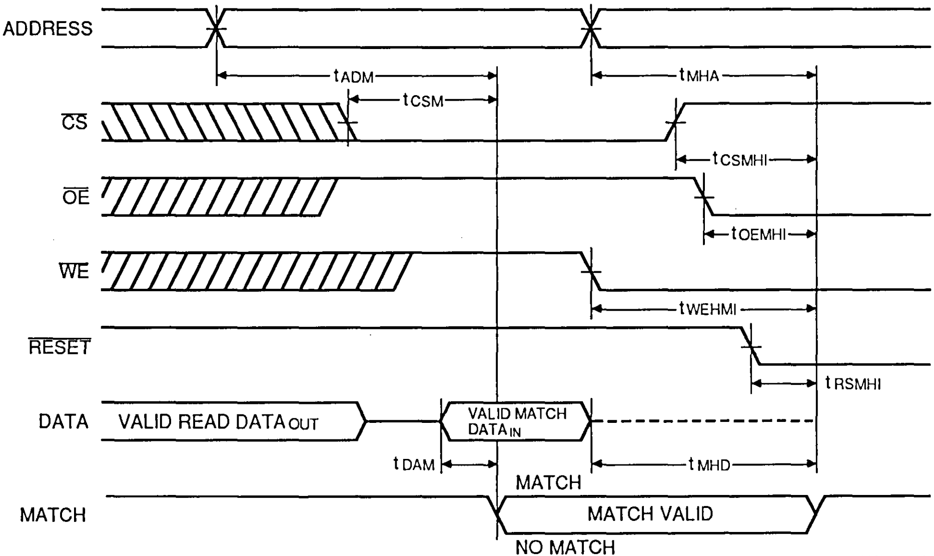
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71B74S12(1)		71B74S15		71B74S18		71B74S25(2)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Match Cycle										
t_{ADM}	Address to MATCH Valid	—	12	—	15	—	18	—	25	ns
t_{CSM}	Chip Select to MATCH Valid	—	8	—	10	—	12	—	17	ns
t_{CSMHI}	Chip Select to MATCH High	—	10	—	12	—	15	—	20	ns
t_{DAM}	Data Input to MATCH Valid	—	10	—	13	—	16	—	22	ns
t_{OEMHI}	$\overline{OE}$ Low to MATCH High	—	10	—	12	—	15	—	20	ns
t_{WEMHI}	$\overline{WE}$ Low to MATCH High	—	10	—	12	—	15	—	20	ns
t_{RSMHI}	$\overline{RESET}$ Low to MATCH High	—	12	—	15	—	18	—	25	ns
t_{MHA}	MATCH Valid Hold From Address	2	—	2	—	2	—	2	—	ns
t_{MHD}	MATCH Valid Hold From Data	2	—	2	—	2	—	2	—	ns

NOTE:
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.

3001 tbl 12

MATCH TIMING(1)



3001 drw 12

NOTE:
1. It is not recommended to float data and address input pins while the MATCH pin is active.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

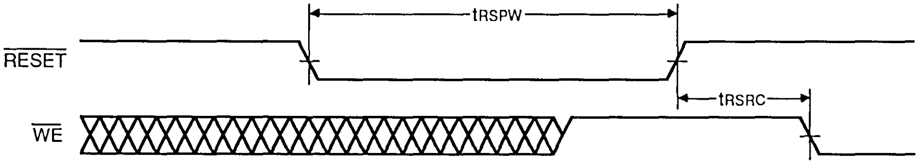
Symbol	Parameter	71B74S12(1)		717B4S15		71B74S18		71B74S25(2)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
tRSPW	Reset Pulse Width(2)	25	—	30	—	35	—	45	—	ns
tRSRC	Reset High to $\overline{\text{WE}}$ Low	3	—	3	—	5	—	5	—	ns

NOTES:

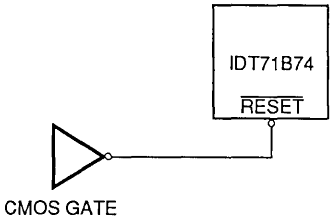
3001 tbl 13

1. 0° to +70°C temperature range only.
2. Recommended duty cycle = 10% maximum.
3. -55°C to +125°C temperature range only.

RESET TIMING

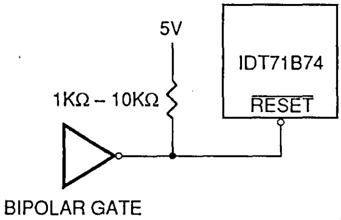


3001 drw 13



3001 drw 14

Driving the $\overline{\text{RESET}}$ pin with CMOS logic.

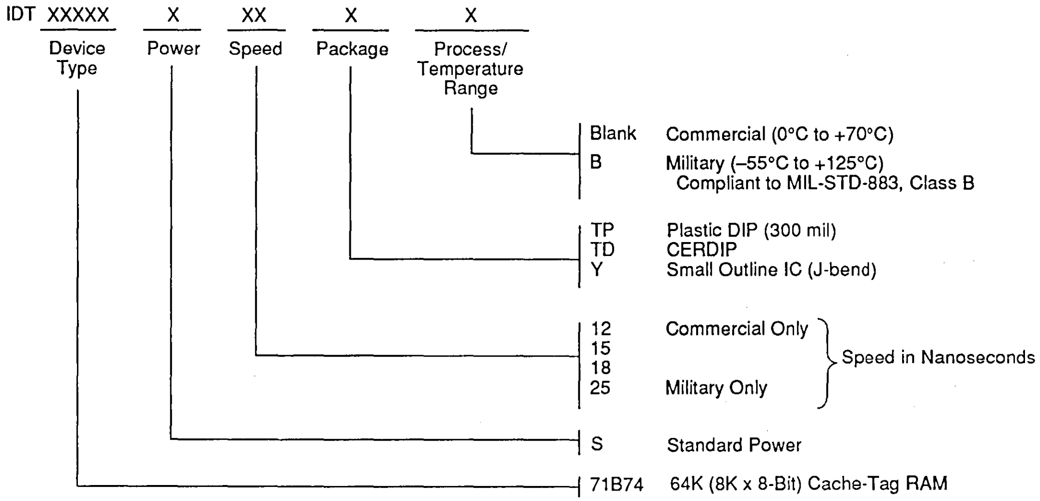


3001 drw 15

Driving the $\overline{\text{RESET}}$ pin with bipolar logic.

Figure 5.

ORDERING INFORMATION



3001 drw 16

Integrated Device Technology, Inc.

BiCMOS STATIC RAM 72K (8K x 9-BIT) CACHE-TAG RAM

ADVANCE INFORMATION
IDT71B79

FEATURES:

- High-speed address to MATCH comparison time
  - — Military: 12/15/20ns (max.)
  - — Commercial: 10/12/15ns (max.)
- High-speed address access time
  - — Military: 12/15/20ns (max.)
  - — Commercial: 10/12/15ns (max)
- High-speed asynchronous RAM Clear
- Produced with advanced BiCEMOS™ high-performance technology
- Single 5V (+10%) power supply
- Input and output directly TTL-compatible
- Military product compliant to MIL-STD-883, Class B
- Standard 28-pin plastic and hermetic DIP (300 mil), 28-pin SOJ

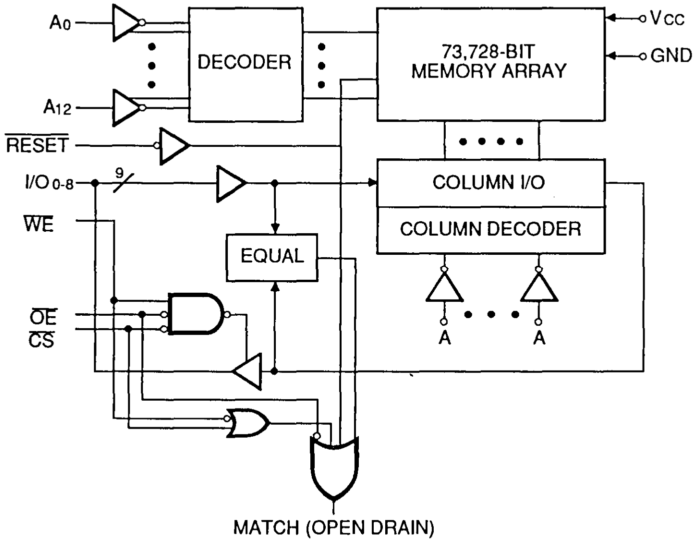
DESCRIPTION:

The IDT71B79 is a high-speed cache address comparator subsystem consisting of a 72K-bit static RAM organized as 8K x 9 and an 9-bit comparator. The IDT71B79 also provides a single RAM clear control, which clears all words in the internal RAM to zero when activated. This allows the tag bits for all locations to be cleared at power-on or system-reset, a requirement for cache comparator systems. The IDT71B79 can also be used as an 8K x 9 high-speed static RAM.

The IDT71B79 is fabricated using IDT's high-performance, high-reliability technology — BiCEMOS. Address access times as fast as 10ns and address-to-comparison times of 10ns are available with maximum power consumption of 825mW.

The MATCH pin of several IDT71B79s can be wired-ORed together to provide enabling or acknowledging signals to the data cache or processor, thus eliminating logic delays and increasing system throughput.

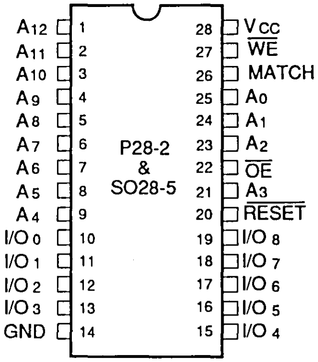
FUNCTIONAL BLOCK DIAGRAM



3003 drw 01

BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



**DIP/SOJ
TOP VIEW**

3003 drw 02

Integrated Device Technology, Inc.

BiCMOS STATIC RAM 64K (16K x 4-BIT)

PRELIMINARY
IDT71B88

FEATURES:

- 16K x 4 BiCEMOS™ static RAM
- High-speed address/chip select time
  - — Military: 10/12/15ns
  - — Commercial: 8/10/12ns
- Single chip select
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Available in 22-pin, 300 mil side-brazed ceramic DIP; 22-pin, 300 mil plastic DIP and 24-pin, 300 mil plastic SOJ packages

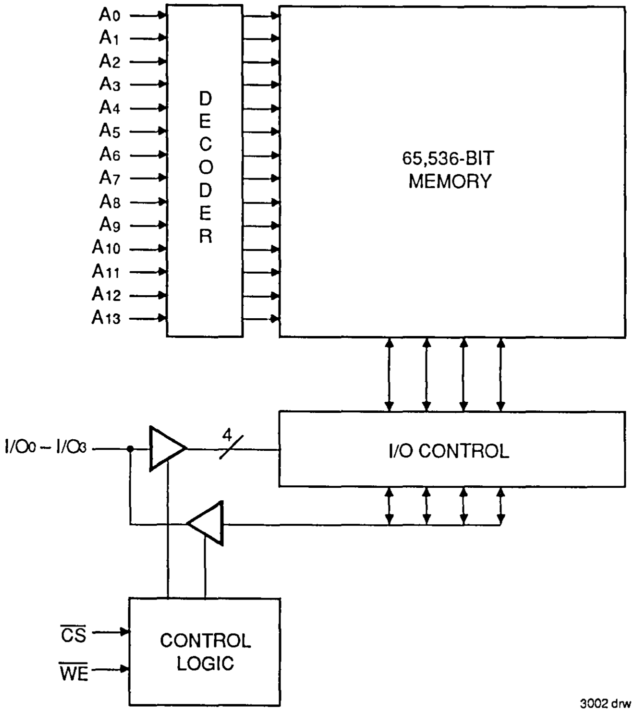
DESCRIPTION:

The IDT71B88 is a 65,536-bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-perfomance high-reliability BiCEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

Address access times as fast as 8ns are available with power consumption of only 400mW (typ.). All inputs and outputs of the IDT71B88 are TTL-compatible and operation is from a single 5V supply.

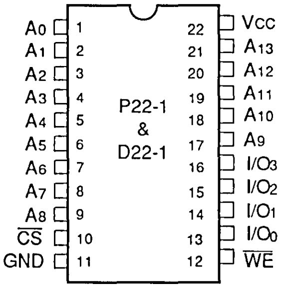
The IDT71B88 is packaged in a 22-pin, 300-mil side-brazed; 22-pin, 300 mil plastic DIP and a 24-pin SOJ packages.

FUNCTIONAL BLOCK DIAGRAM



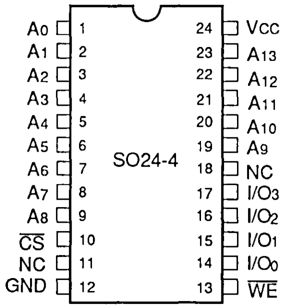
3002 drw 01

PIN CONFIGURATIONS



DIP
TOP VIEW

3002 drw 02



SOJ
TOP VIEW

3002 drw 02a

BiCEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +125	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 3002 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	I/O	Function
L	H	D_{OUT}	Read
L	L	D_{IN}	Write
H	X	Hi-Z	Deselect Chip

NOTE: 3002 tbl 01

1.. H = V_{IH}, L = V_{IL}, x = Don't care.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE: 3002 tbl 03

1. This parameter is guaranteed by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5	—	0.8	V

NOTE: 3002 tbl 04

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71B88 Min.	IDT71B88 Max.	Unit
$\lvert I_{LI} \rvert$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	10	µA
$\lvert I_{LO} \rvert$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.	—	0.4	
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	—	V

3002 tbl 05

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%)

Symbol	Parameter	71B88S8 Com'l.	71B88S8 Mil.	71B88S10 Com'l.	71B88S10 Mil.	71B88S12 Com'l.	71B88S12 Mil.	71B88S15 Com'l.	71B88S15 Mil.	Unit
I_{CC}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	200	—	180	190	160	170	—	170	mA

NOTES: 3002 tbl 05

1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC}.

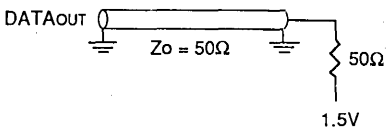
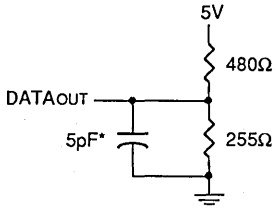


Figure 1A. AC Test Load

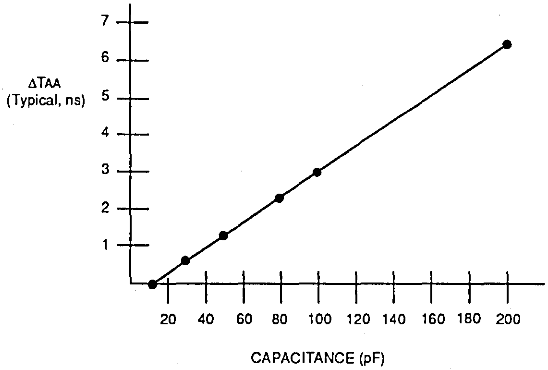
3002 drw 03a



3002 drw 03b

*Including jig and scope capacitance.

Figure 1B.



302 drw 03c

Figure 1C. Lumped Capacitive Load, Typical Derating

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1A, 1B & 1C

3002 tbl 06

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

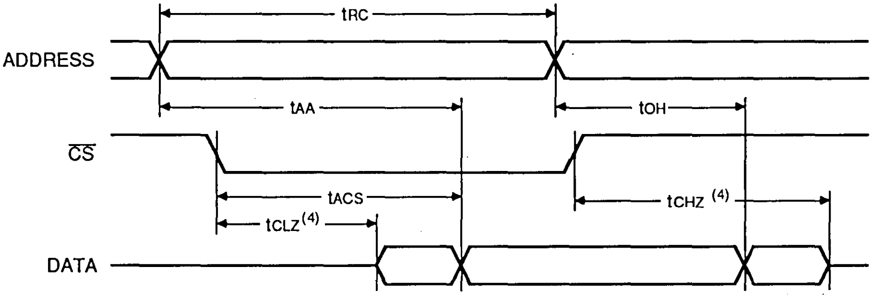
Symbol	Parameter	71B88S8(1)		71B88S10		71B88S12		71B88S15(3)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	8	—	10	—	12	—	15	—	ns
t_{AA}	Address Access Time	—	8	—	10	—	12	—	15	ns
t_{ACS}	$\overline{CS}$ Access Time	—	6	—	6	—	7	—	8	ns
t_{CLZ}(2)	$\overline{CS}$ to Output in Low Z	3	—	3	—	3	—	4	—	ns
t_{CHZ}(2)	$\overline{CS}$ to Output in High Z	—	6	—	6	—	7	—	8	ns
t_{OH}	Out Hold from Address Change	3	—	3	—	3	—	3	—	ns
Write Cycle										
t_{WC}	Write Cycle Time	8	—	10	—	12	—	15	—	ns
t_{CW}	Chip Select to End of Write	8	—	8	—	9	—	10	—	ns
t_{AW}	Address Valid to End of Write	8	—	8	—	9	—	10	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	8	—	8	—	9	—	10	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}(2)	$\overline{WE}$ to Output in High Z	—	3	—	3	—	4	—	4	ns
t_{DW}	Data Set-Up Time	5	—	5	—	6	—	8	—	ns
t_{DH}	Data Hold from Write	0	—	0	—	0	—	0	—	ns
t_{OW}(2)	Out Active from End of $\overline{WE}$	3	—	3	—	3	—	4	—	ns

NOTES:

3002 tbl 08

1. 0° to +70°C temperature range only.
2. This parameter is guaranteed with the AC Load, Figure 1B, and is not tested.
3. -55°C to +125°C temperature range only.

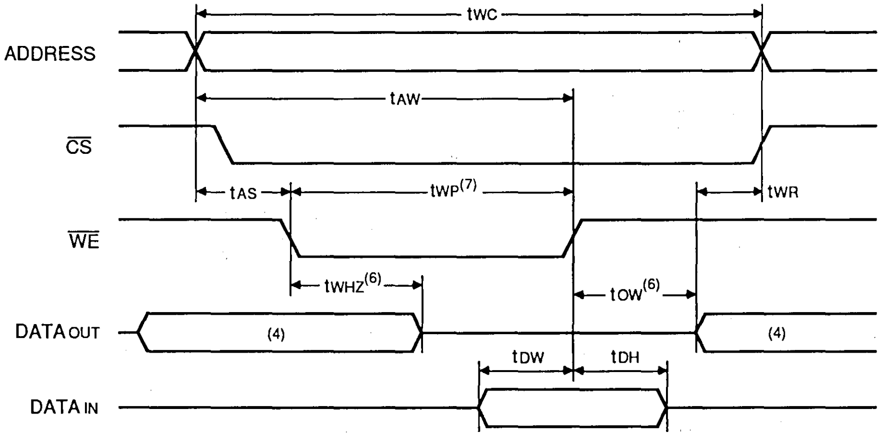
TIMING WAVEFORM OF READ CYCLE(1,2,3)



3002 drw 04

NOTES:
1. WE is high for read cycle.
2. Device is continuously selected, CS = VIL.
3. Address valid prior to or coincident with CS transition low.
4. Transition is measured ±200mV from steady state with 5pF load (including scope and jig).

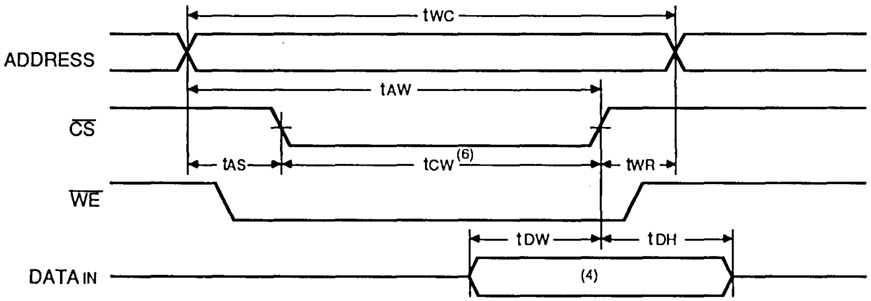
TIMING WAVEFORM OF WRITE CYCLE NO.1 (WE CONTROLLED TIMING)(1,2,3,56)



3002 drw 05

NOTES:
1. WE or CS must be high during all address transitions.
2. A write occurs during the overlap (tWC and tWP) of a low CS and a low WE.
3. tWR is measured from the earlier of CS or WE going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If CS low transition occurs simultaneously with or after the WE low transition, the outputs remain in the high impedance.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).
7. During a WE controlled write cycle, the pulse width must be the larger of tWP or (tDW + tWHZ) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW.

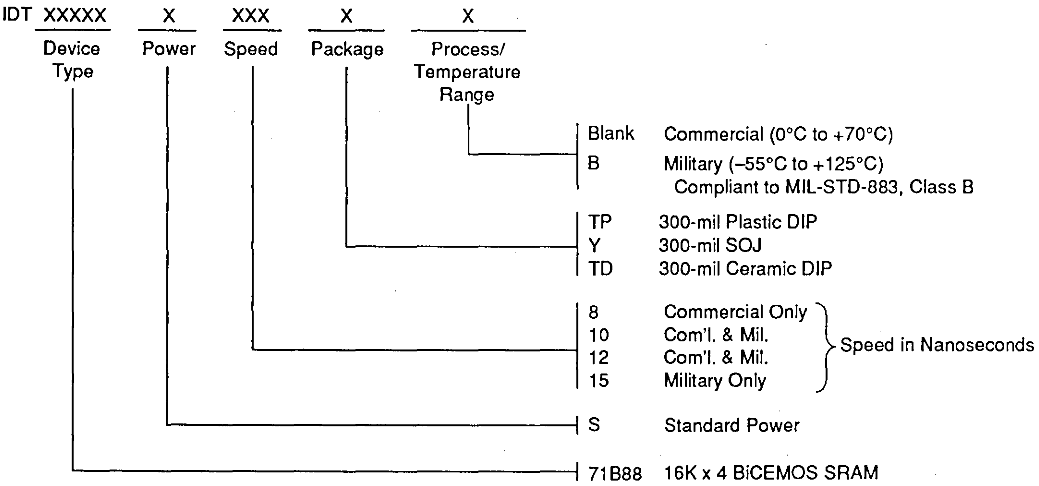
TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{\text{CS}}$ CONTROLLED TIMING)(1,2,3,4,5)



3002 drw 06

NOTES:
1. $\overline{\text{WE}}$ or $\overline{\text{CS}}$ must be high during all address transitions.
2. A write occurs during the overlap (twc and twp) of a low $\overline{\text{CS}}$ and a low $\overline{\text{WE}}$.
3. twr is measured from the earlier of $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high to the end of the write cycle.
4. If $\overline{\text{CS}}$ low transition occurs simultaneously with or after the $\overline{\text{WE}}$ low transition, the outputs remain in the high impedance.
5. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).
6. During a $\overline{\text{WE}}$ controlled write cycle, the pulse width must be the larger of twp or (tdw + twhz) to allow the I/O drivers to turn off and data to be placed on the bus for the required tdw.

ORDERING INFORMATION



3002 drw 07

Integrated Device Technology, Inc.

BiCMOS STATIC RAM 64K (16K x 4-BIT)

PRELIMINARY
IDT71B98

FEATURES:

- 16K x 4 BiCEMOS™ Static RAM
- High-speed address access time
  - Commercial: 8/10/12ns
  - Military: 10/12/15ns
- Fast Output Enable
  - Commercial: 5/6/7ns
  - Military: 6/7/8ns
- Multiple Chip Selects
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Available in 24-pin, 300 mil plastic DIP; 24-pin, 300 mil ceramic DIP and 24-pin, 300-mil plastic SOJ

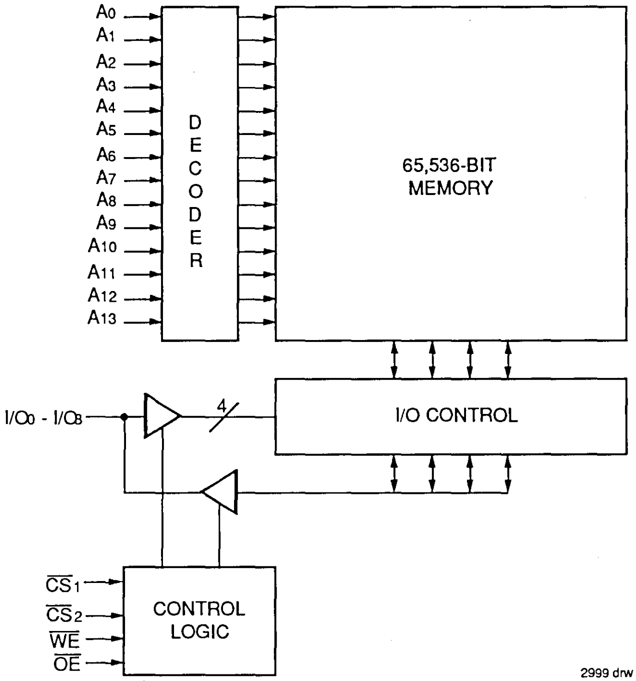
DESCRIPTION:

The IDT71B98 is a 65,536-bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-perfomance high-reliability BiCEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

Address access times as fast as 8ns are available with power consumption of only 400mW (typ.). All inputs and outputs of the IDT71B98 are TTL-compatible and operation is from a single 5V supply. Multiple chip selects simplify design and operation.

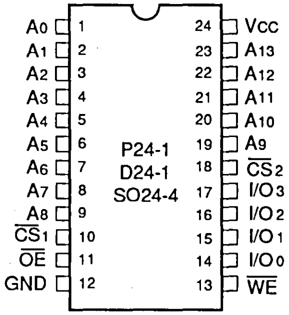
The IDT61B98 is packaged in a 24-pin, 300 mil plastic DIP; 24-pin, 300 mil ceramic DIP and a 24-pin, 300 mil SOJ.

FUNCTIONAL BLOCK DIAGRAM



2999 drw 01

PIN CONFIGURATION



2999 drw 02

DIP/SOJ
TOP VIEW

TRUTH TABLE(1)

$\overline{CS_1}$	$\overline{CS_2}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
X	H	X	X	Hi-Z	Deselect Chip
H	X	X	X	Hi-Z	Deselect Chip
L	L	L	H	D_{OUT}	Read Cycle
L	L	X	L	D_{IN}	Write Cycle
L	L	H	H	Hi-Z	Outputs Disabled

NOTE: 2999 tbl 01
1. H = V_{IH}, L = V_{IL}, X = Don't care.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +125	°C
P_T	Power Dissipation	1.25	1.25	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2958 tbl 02
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}(2)	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}(1,2)	Output Capacitance	V_{OUT} = 0V	12	pF

NOTES: 2999 tbl 03
1. With output deselected.
2. Characterized values, not currently tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5	—	0.8	V

NOTE: 2999 tbl 04
1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71B98		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.	—	0.4	
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	—	V

2999 tbl 05

DC ELECTRICAL CHARACTERISTICS[1]

(Vcc = 5.0V ± 10%)

Symbol	Parameter	71B98S8		71B98S10		71B98S12		71B98S15		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
Icc	Dynamic Operating Current, $\overline{CS}$ = VIL Outputs Open, Vcc = Max., f = fMAX[2]	200	—	180	190	160	170	—	170	mA

NOTES:

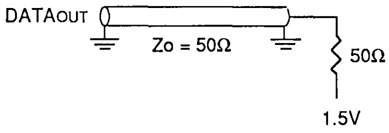
1. All values are maximum guaranteed values.
2. fMAX = 1/tRC.

2999 tbl 05

AC TEST CONDITIONS

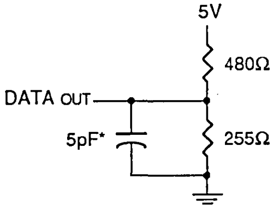
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1A, 1B & 1C

2999 tbl 06



2999 drw 03a

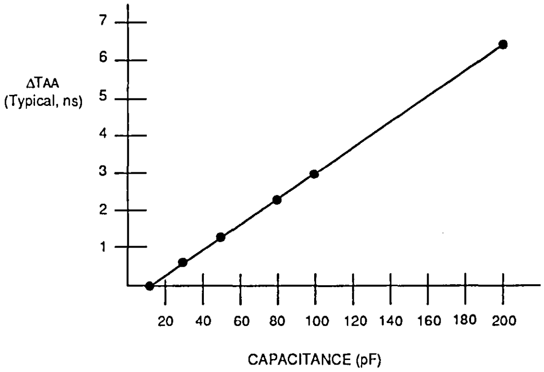
Figure 1A. AC Test Load



2999 drw 04

*Including jig and scope capacitance.

Figure 1B.



2999 drw 03b

Figure 1C. Lumped Capacitive Load, Typical Derating

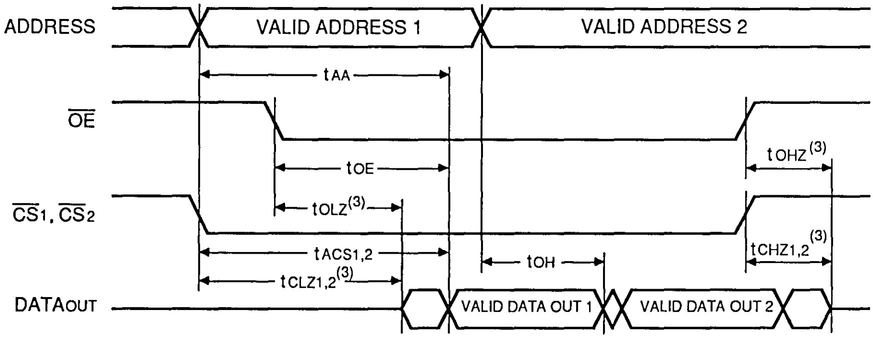
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71B98S8(1)		71B98S10		71B98S12		71B98S15(3)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
tRC	Read Cycle Time	8	—	10	—	12	—	15	—	ns
tAA	Address Access Time	—	8	—	10	—	12	—	15	ns
tACS1,2	$\overline{\text{CS}}$1,2 Access Time	—	6	—	7	—	7	—	8	ns
tOE	$\overline{\text{OE}}$ to Output Valid	—	4	—	5	—	6	—	7	ns
tCLZ1,2(2)	$\overline{\text{CS}}$1,2 to Output in Low Z	3	—	3	—	3	—	4	—	ns
tCHZ1,2(2)	$\overline{\text{CS}}$1,2 to Output in High Z	—	6	—	6	—	7	—	8	ns
tOLZ(2)	$\overline{\text{OE}}$ to Output Low Z	3	—	3	—	3	—	4	—	ns
tOHZ(2)	$\overline{\text{OE}}$ to Output High Z	—	3	—	3	—	3	—	4	ns
tOH	Out Hold from Add Change	3	—	3	—	3	—	3	—	ns
Write Cycle										
tWC	Write Cycle Time	8	—	10	—	12	—	15	—	ns
tAW	Address to End of Write	8	—	8	—	9	—	10	—	ns
tAS	Address Setup Tme	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	8	—	8	—	9	—	10	—	ns
tCW1,2	$\overline{\text{CS}}$1,2 to End of Write	8	—	8	—	9	—	10	—	ns
tWR	Write Recovery	0	—	0	—	0	—	0	—	ns
tWZ(2)	$\overline{\text{WE}}$ to Out in High Z	—	3	—	3	—	3	—	4	ns
tDW	Data Setup	5	—	5	—	6	—	8	—	ns
tDH	Data Hold	0	—	0	—	0	—	0	—	ns
tOW(2)	Output from End of Write	3	—	3	—	3	—	4	—	ns

NOTES:
2999 tbl 08

1. 0° to +70°C temperature range only.
2. This parameter is guaranteed with the AC Load, Figure 1B, and is not tested.
3. -55° to +125°C temperature range only.

TIMING WAVEFORM OF READ CYCLE(1,2)

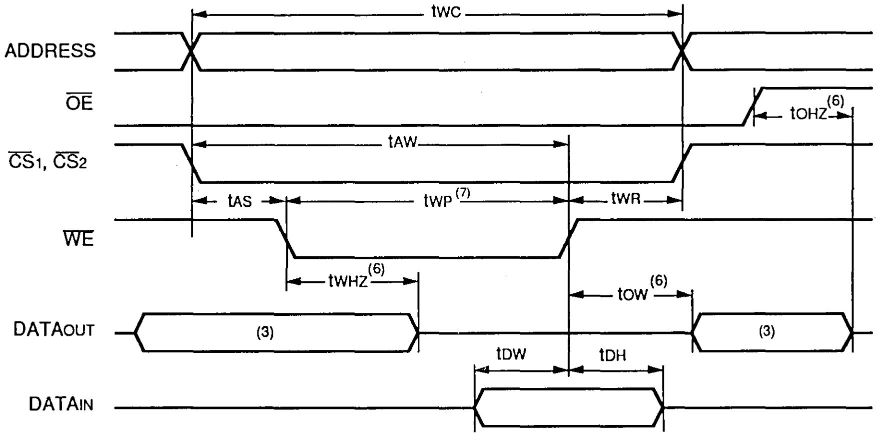


2999 drw 05

NOTES:

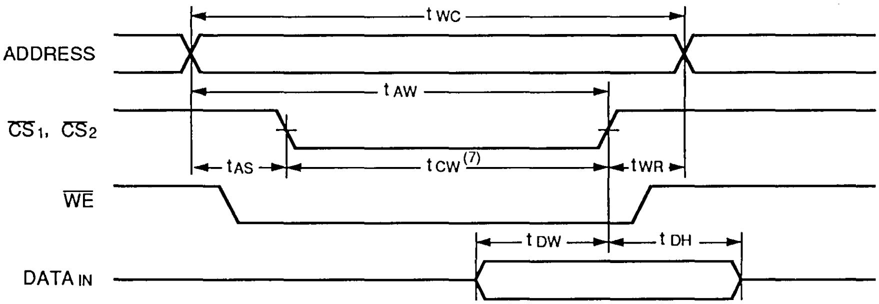
1. $\overline{\text{WE}}$ is high for read cycle.
2. Address valid prior to or coincident with $\overline{\text{CS}}$1,2 transition low.
3. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ CYCLE)(1,2,4,5)



2999 drw 06

TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ CYCLE)(1,2,4,5,6)

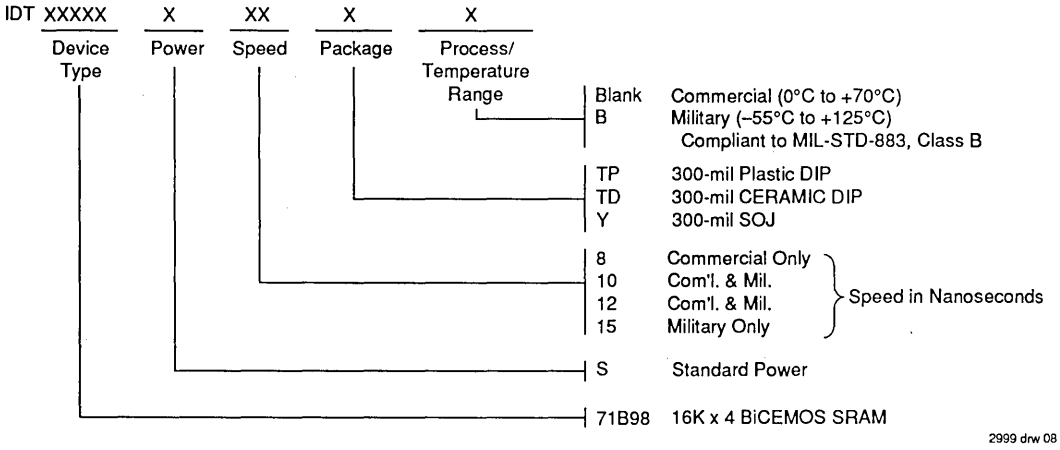


2999 drw 07

NOTES:

1. A write occurs during the overlap (t_{CW} and t_{WP}) of $\overline{CS}_{1,2}$ low and $\overline{WE}$ low.
2. t_{WP} is measured from the earlier of $\overline{CS}_{1,2}$ or $\overline{WE}$ being deasserted.
3. During this period, the I/O pins are in the output state, and input signals must not be applied on these pins.
4. If $\overline{CS}$ asserted coincident with or after $\overline{WE}$ goes low, the output will remain in a high impedance state.
5. If $\overline{CS}$ is deasserted coincident with or before $\overline{WE}$ goes high, the output will remain in a high impedance state.
6. The transition is measured ±200mV from steady state with a 5pF load.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

ORDERING INFORMATION



IDT XXXXX X XX X X

Code field	Code	Meaning
Process/ Temperature Range	Blank	Commercial (0°C to +70°C)
	B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B
Package	TP	300-mil Plastic DIP
	TD	300-mil CERAMIC DIP
	Y	300-mil SOJ
Speed (Speed in Nanoseconds)	8	Commercial Only
	10	Com'l. & Mil.
	12	Com'l. & Mil.
	15	Military Only
Power	S	Standard Power
Device Type	71B98	16K x 4 BiCEMOS SRAM

2999 drw 08

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Integrated Device Technology, Inc.

SEPARATE I/O RAMS INCREASE SPEED AND REDUCE PART COUNT

APPLICATION NOTE AN-05

INTRODUCTION

Static RAMs with separate data inputs and data outputs, such as the IDT71681/71682 4K x 4-bit RAMs and the IDT71982/71982 16K x 4-bit RAMs, provide memory organizations that can improve system architecture in many applications. IDT makes a series of separate I/0 RAMs, as shown in Table 1. In this application note, we will demonstrate several system ideas where RAMs with separate data inputs and data outputs offer improved system performance. Typically, the separate data inputs and data outputs eliminate the need for multiplexing of demultiplexing in the data path. Thus, not only is the output enable or disable time eliminated in a critical speed path, but a potential additional element (multiplexer or demultiplexer) may also be eliminated.

Size	Organization	Outputs Track Inputs During Write	Outputs High Imped. During Write
16K	16K x 1	—	IDT6167
	4K x 4	IDT71681	IDT71682
64K	64K x 1	—	IDT7187
	16K x 4	IDT71981	IDT71982

Table 1. IDT Separate I/O RAM Chips

SEPARATE I/O RAM APPLICATION EXAMPLES

Microprogram Memory

Separate I/O RAMs can be used in a high-speed writeable control store application and offer both speed improvement and a significant parts count reduction in the interface to a MOS microprocessor used to initialize the RAM at power-up. Figure 1 shows a typical writeable control store design for a microprogrammed machine. Here we see an IDT39C10 microprogram sequencer driving the 12-address lines of the IDT71681/716824K word array. If we assume a microcode width of 96 bits, this design will use 24 of the IDT71681/71682 24-pin, 300 mil packages. As shown in Figure 1, the 12 address lines to all 24 packages are connected in parallel and are driven by the Y outputs of the IDT39C10 microprogram sequencer This gives a total microcode depth of 4K words, which is sufficient for most microprogram applications. The four data outputs from each device provide microcode bits to the pipeline register to overlap the microinstruction fetching with the microinstruction execution. The pipeline register always contains the microinstruction currently executing, while the IDT39C10 is generating the next address to the RAM and the RAM is accessing the next microinstruction to be set up at the input to the pipeline register.

The advantages of using the IDT71681/71682 RAM in this application come from the speed of this device and from the parts savings associated with not having to demultiplex the data to be loaded into the memory. If the data path were to be bidirectional, such as would be required if we used the IDT6116 (2K x 8-bit RAM)on the IDT6168(4Kx4-bit RAM),it would be necessary to demultiplex a MOS microprocessor data bus that provides the microcode at power up. This would require one 8-bit driver for each 8 bits of RAM to interface between the various RAMs and the 8-bit microprocessor data bus—an additional 12 parts in this case.

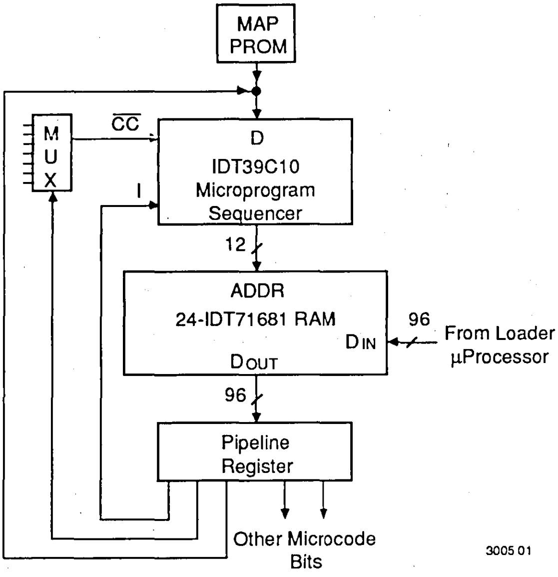


Figure 1. Typical Writeable Control Store In a Microprogrammed Machine

In a typical system, such as is shown in Figure 1, the microcode is read from a floppy disk and loaded into the writeable control store. An example of this type of microcode loading architecture as shown in Figure 2. The microprocessor system shown in Figure 2 requires three interface points to the writeable control store. First, you must define the address for the write operation. This is provided by means of a WCS address register to select which word in the writeable control store will be written into. Second, you must define the data you are going to write. This is provided by a data register which defines the data for a specific eight bits of the 96-bit word of the control store shown in Figure 1. A total of 12 bytes are required to load one microcode word into the writeable control store depicted in Figure 1. The specific byte to be written is selected by four additional address bits from the WCS address register Which are directed to the decoder so that one of the 12 bytes can be selected for loading. Third, a control register is then used to select between the WCS load and operate modes and to manipulate the write enable ($\overline{\text{WRITE}}$) line connected to the decoder.

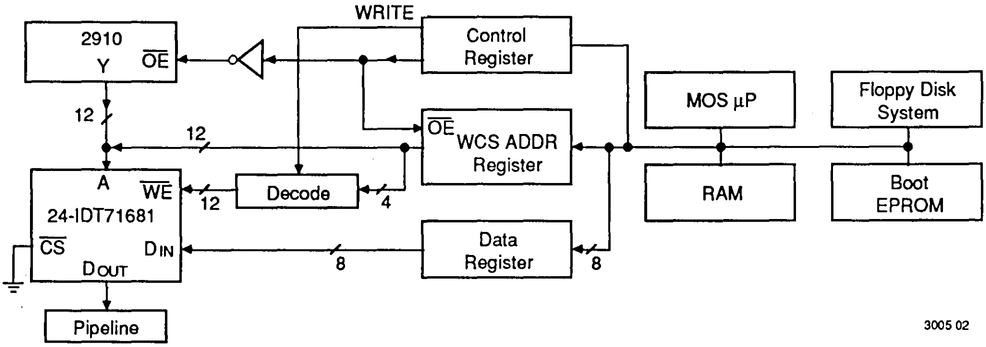


Figure 2. Autoload of the Writeable Control Store

The complete cycle required can be described as follows. First, set up the control register to select the WCS address register onto the address bus and disable the IDT39C10 Y outputs. Second, move the address of the first byte to be loaded to the WCS address register. Third, move the data byte to be loaded to the data register. Fourth, change the $\overline{\text{WRITE}}$ line from high-to-low-to-high by means of two MOS microprocessor I/O cycles. This will write one byte of data to the writeable control store memory. Continue by repeating the steps of loading the WCS address register, data register and then "writing" the data into the writeable control store memory.

A detailed connection diagram of the IDT71681/71682 interface to the MOS microprocessor is shown in Figure 3. Only 10 of the 24 devices are shown, but the connection scheme is similar for all 24-devices. The important point to recognize from the diagram is that the data-in lines are connected on a byte-wide basis. One IDT71681/71682 is connected to the D0 to D3 data inputs and the second IDT71681/71682 is connected to the D4 through D7 inputs. This means that each two devices are connected so as to accept one byte of data from the MOS microprocessor system. The 12 address lines to IDT71681/71682 are connected

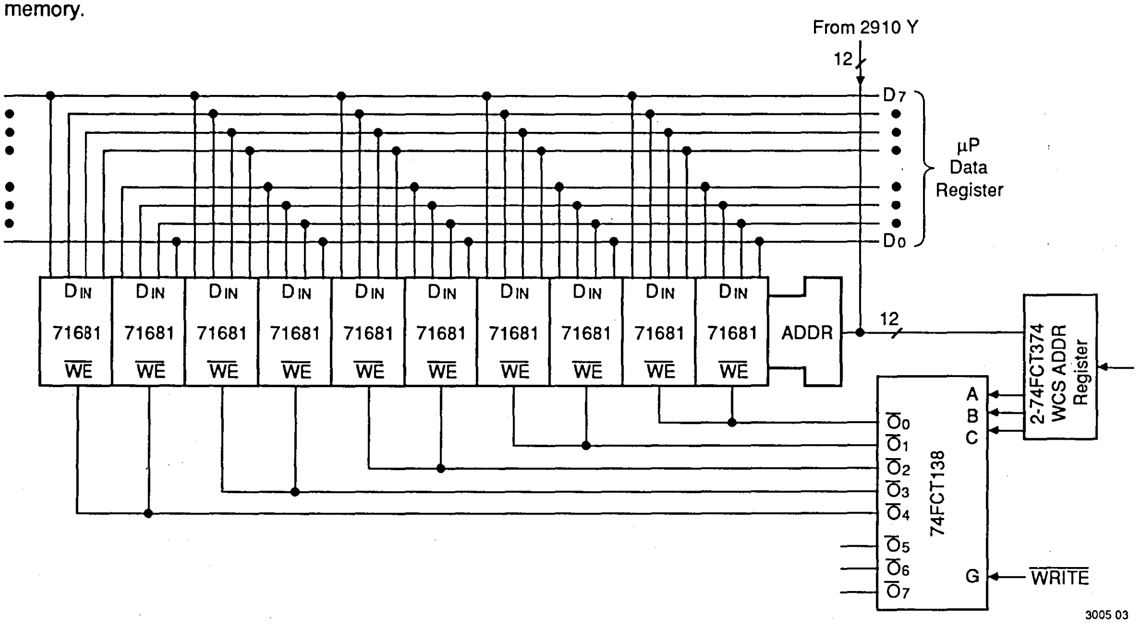


Figure 3. Detail of the MOS Microprocessor Interface to a Writeable Control Store

in parallel and are driven by a register with three state outputs such as the IDT74FCT374.The remaining address lines from the 29825 WCS address register are connected to decoders such as the IDT74FCT138. Each output for the IDT74FCT138 is connected to two write enable inputs on the IDT71681/71682 memories. This allows one byte to be written when the $\overline{\text{WRITE}}$ line is changed high-low-high. The chip select line is simply grounded and not used in this application. As can be seen, the IDT71681/71682 offers a convenient interface in a writeable control store for external loading of the data. This connection concept can be extended and changed such that the writeable control store could be loaded with data provided by the host execution CPU itself, rather than the floppy disk.

VIRTUAL MEMORY AND MEMORY MAPPING

Separate I/0 RAMs are ideally suited for use with MOS microprocessors to provide the memory mapping function associated with today's complex microprocessor operating systems. As shown in Figure 4, the IDT71681/71682 can be used to provide mapping from a microprocessor virtual address to a microprocessor physical address in main memory. In addition, status information about the map can also be present in the page table. In this example, a 24-bit virtual address is divided into a 12-bit virtual page consisting of 4K words per page. Depth into the page is provided by a 12-bit offset address. As shown in Figure 4, the 12-bit virtual page address can be connected to the page mapping memory and the resultant output will be a physical page address and status information. A detailed connection diagram is shown in Figure 5.

A computer that provides any form of mapping other than the identity map between the central processing unit generated addresses and the physical memory address satisfies the most general definition of virtual memory. In Figure 5, we see the IDT71681/71682 address lines connected to the upper 12 bits of an address bus, such as those provided by the 68000 microprocessor. Here, the separate data output lines are used to provide mapped addresses as well as exception bit status vectors. The separate data-in lines can be connected to the data bus so that the page table provided by this memory is easily updated.

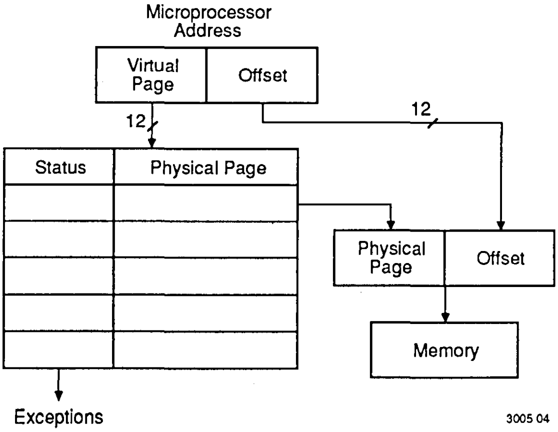


Figure 4. Memory Mapping

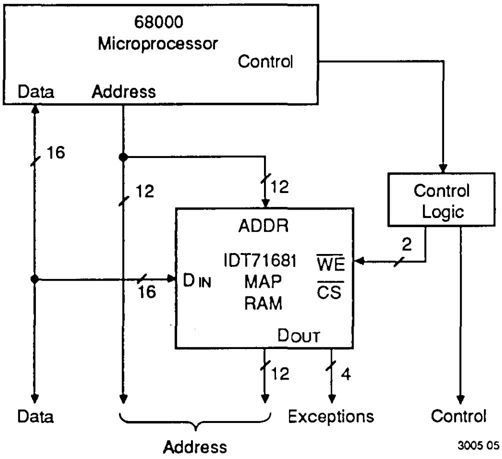


Figure 5. Memory Mapping

Many use the terminology of virtual memory in a more restrictive fashion. That is, a virtual memory is one where the actual physical memory is smaller than the total memory addressing capability of the machine. A page table memory map, such as that shown in Figure 5, is used to provide a translation from the virtual address to the physical address in such a memory. In a related definition called memory mapping, the physical memory is larger than the logical address space of the machine. This is often applied to such microprocessors as the 8085 and Z80. Here, the machine's logical address space is limited to 64K bytes, but it may be desirable to have a larger physical memory available to the machine. The connection scheme shown in Figure 6 can be used to perform this memory mapping. Some number of address lines, eight in this example, are connected to eight of the 12 IDT71681/71682 RAM address lines. The additional four RAM address lines are provided by a register and perform an additional mapping select function. The 12 RAM data output lines of the RAM are used in conjunction with the 8 remaining address lines from the microprocessor to provide a total of 20 address lines (1 megabyte) in this example. The 12 RAM data-in lines are connected to the data bus for easy loading of the page table.

Figures 5 and 6 indicate that some thought must be given to the exact mechanism for the address to be provided to the mapping RAM while it is being loaded. This can be handled in one of two ways. The simplest way is to provide an address register on one of the microprocessor I/O ports that is loaded with the target address, and then this address is

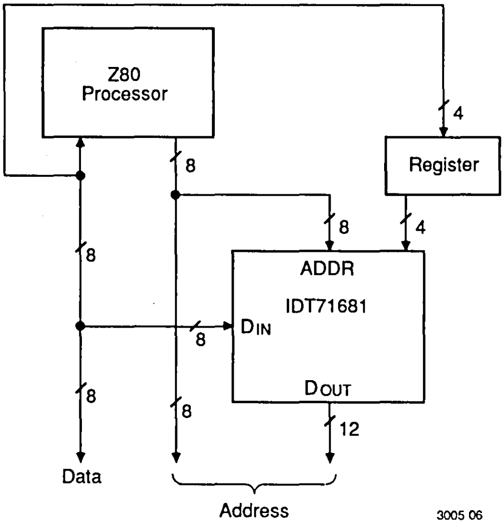


Figure 6. Z80 Memory Mapping

used when the mapping memory is being written into. A more clever technique is to provide a control register that disables the main memory write and enables the mapping memory write such that no additional address register is required. Instead, data to be loaded into the mapping memory is simply moved to the address in the virtual space and is redirected to the mapping memory rather than the main memory.

Again, the examples of Figure 3 through 5 demonstrate the advantage of the IDT71681/71682 in having separate data inputs and data outputs.

CACHE MEMORY

A cache memory is a high-speed memory that is placed between the CPU and the main system bus. The purpose of a cache memory is to make a slow memory look like a fast memory. This is done by using two memories. The first is a small, high speed memory called a cache memory, and the second is a large, slow memory called the main memory. Both memories are attached to the system bus which is connected to the CPU. The cache memory holds a copy of the most frequently used data in the main memory. If data requested by the CPU is in the cache memory, it responds first; if not, the CPU waits for the data from the slower main memory. If the data and instructions being executed most of the time are in the cache memory a performance improvement is realized. This is commonly the case because most programs consist of loops and small pieces of code which are executed repetitively, and these occupy a small number of memory locations. The hardware associated with the cache memory attempts to keep this data in the high-speed memory. The term "hit ratio" is used to describe the number of times the data or instructions are in the cache memory versus the total number of memory accesses. It is not unusual to find hit ratios in the 90 percent range for some cache memory designs.

One of the most common cache memory organizations used is called the direct mapped cache memory. Figure 7 shows the block diagram for the implementation of the typical direct mapped cache. In this implementation, the cache memory consists of three main parts. These are the tag store, the data store and the match comparator. In the example shown in Figure 7, the tag buffer and data RAM are each 4K words deep using one row of the IDT71681/71682 static RAMs. The high order 12 bits of the address can be stored in the tag RAM so as to specify the unique memory space for which the data corresponds. The tag RAM usually contains additional bits which represent data validity and parity.

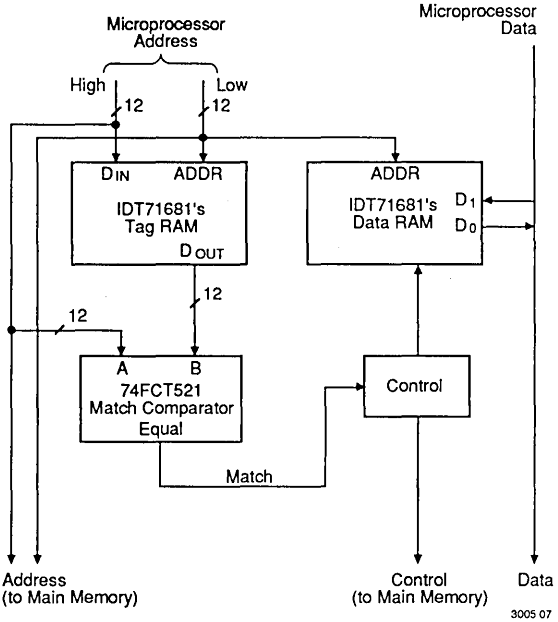


Figure 7. Direct Mapped Cache Memory

The operation of such a cache memory is as follows. The microprocessor puts out an address on the address bus. The lower 12 bits are connected to the address inputs of the data and tag RAMs and cause the data and tag RAMs to begin fetching the word at the location. Then, the actual data value stored in the tag RAM is compared against the upper 12 address bits to look for a match. If a match is found, the valid bit is true and the data in the data RAM corresponds to the address on the address bus, we have a cache "hit" and the data in the data RAM is placed on to the microprocessor data bus. If no match is found or the valid bit is false, then a cache "miss" occurs and the data must be fetched from the main memory. As the data is brought in from the main memory to the microprocessor, it is also written into the data RAM and, at the same time, the tag RAM is loaded with the high order 12 address bits that represent the tag number from which the data was taken. Hopefully, the next time this address is used, it will still be in the cache memory.

STACK MACHINES AND HIGH-PERFORMANCE ALUS

A bit-slice microprocessor design can utilize separate I/O RAMs in the ALU architecture in several ways. A typical bit-slice microprocessor ALU configuration is shown in Figure 8. Here we see the IDT71681/71682 configured with its data inputs connected to the Y output of the 39C03 bit-slice, and its data outputs connected to the DA input of the 39C03 bit-slice. Two uses for such a connection are obvious. First, it is possible to use the tightly coupled RAM to increase the number of registers available to the ALU. This could be used in certain high-performance algorithms such as floating point, Fast Fourier Transforms (FFTs), etc. Similarly, this register set might be used to allow very high-speed context switching of the processor ALU section. In this fashion, no register would have to be updated during the handling of interrupts or other system/user context switches.

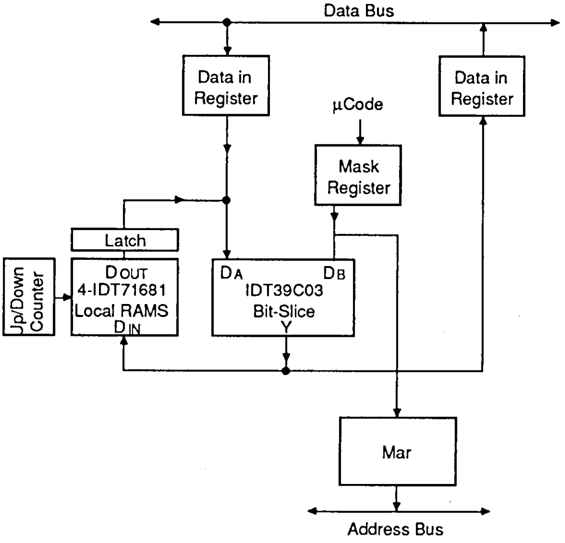


Figure 8. Stack Machines and High-Performance ALUs

Another use for the IDT71681/71682 RAM shown in Figure 8 would be to provide a local stack for the ALU. This could be implemented using an up-down counter to drive the address lines to the RAM and the appropriate microcode to control pushing and popping of the stack. One or more such stacks could be very useful in high level language machines. For example, two such stacks might be used in a FORTH machine. One stack would be the operand stack, while the second stack would be the return stack.

A typical TTL ALU implementation is shown in Figure 9. Here, an MSI ALU, such as the 74S181, is used in a microprogrammed environment. Local register/accumulator storage is provided by IDT71681/71682 memories. The A and B inputs to the ALU are driven by the accumulator A and accumulator B RAM register/stack, respectively. Again, the advantage of the separate data inputs and data outputs is well displayed.

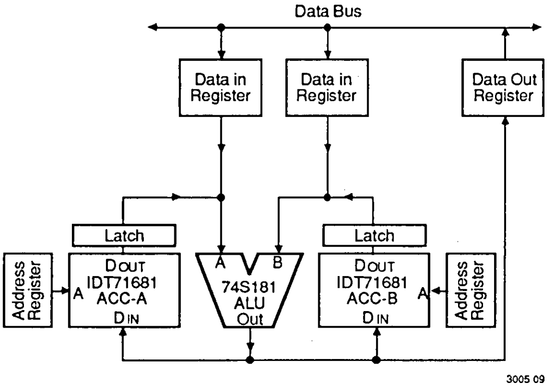


Figure 9. TTL ALU Implementation

VIDEO DISPLAY CONTROLLER

The video display controller shown in Figure 10 can utilize separate I/O RAMs in two different ways. One area of the video display controller, the character generator, uses two IDT71681/ 71682s to hold 512 different 5-by-7 dot characters. In this configuration, the CRT controller provides the address to the character generator which generates the dot pattern for a particular line in the selected character. By using RAM in the character generator, the character font can be controlled by the host microprocessor and changed as often as desired. Two additional IDT71681/71682s are used for the screen refresh RAM. In this application, two RAM chips provide the local storage for the characters on the screen. Since a standard 24-row-by-80-column CRT display represents almost 2K bytes of data, the screen refresh RAM shown can store up to two pages of information for display.

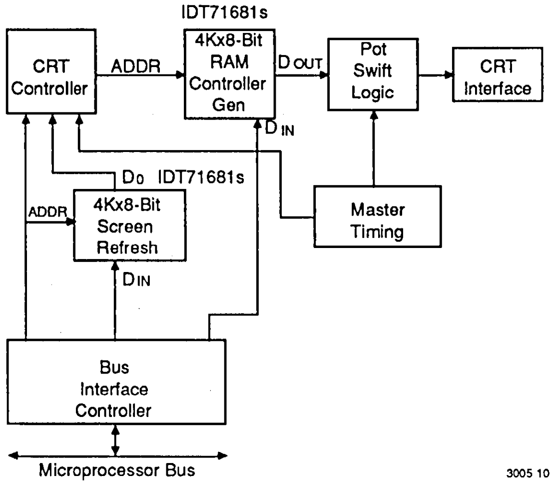
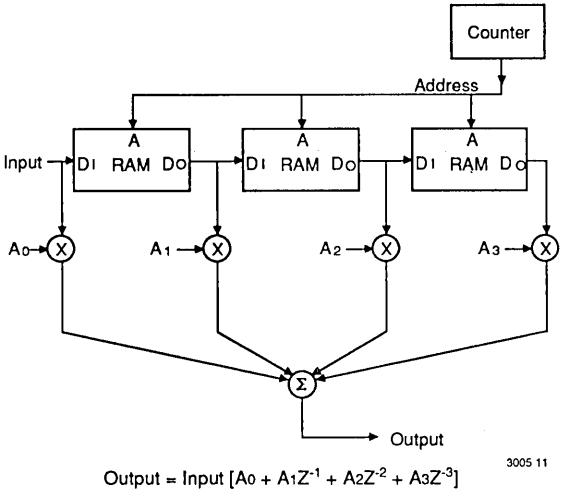


Figure 10. Video Display Controller



$$\text{Output} = \text{Input}\,[A_0 + A_1Z^{-1} + A_2Z^{-2} + A_3Z^{-3}]$$

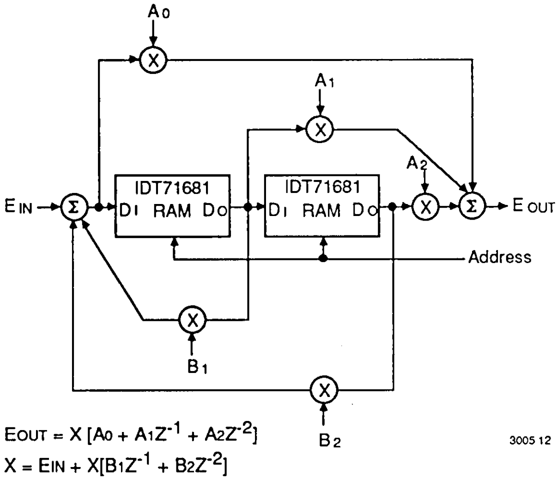
Figure 11. Four-Sample Non-Recursive Digital Filter

DIGITAL FILTERS

The four-sample non-recursive digital filter in Figure 11 is another application which demonstrates the importance of separate data inputs and data outputs in the RAM memory. In this example, a 4096 word range-gated filter is shown. Digital filters consist primarily of memory, multipliers and adders. Range gated filters are used in systems that quantify and otherwise process distance-related measurements such as radar, sonar and ultrasonic medical diagnostic instruments. Typically, the return signal is divided into increments of time (or distance) where each increment is to be individually processed. Thus, many different elements are to be processed and all may share the same multipliers and adders. However, different memory locations are needed for each time-sequential element. The example shown in Figure 11 can best be understood with the following description: the current output is equal to the sum of the present sample times the constant Ao, plus previous sample times the constant A1, plus the second previous sample times the constant A2, plus the third previous sample times the constant A3. Four samples participate in generating each output, and because only input samples contribute to the output, the filter is said to have a finite impulse response.

Similarly, Figure 12 shows a range-gated recursive digital filter. It is similar in concept to that shown in Figure 11, except that a recursive filter contains feedback. Because feedback terms contribute to the output, it has an infinite impulse response. Again, separate I/O RAMs provide a unique performance advantage in this application

Depending on the write timing, it may be necessary to place either latches or registers at the input or output of the RAMs shown in Figure 11 and 12.



$$E_{OUT} = X\,[A_0 + A_1Z^{-1} + A_2Z^{-2}]$$
$$X = E_{IN} + X[B_1Z^{-1} + B_2Z^{-2}]$$

Figure 12. Recursive Digital Filter

PING PONG RAM

A common problem in digital signal processing is the word-by-word transformation of a block of data, such as adding a constant to each word. This transformation is usually done by reading each word from one RAM, modifying the data and writing the word into a second RAM. This type of operation may be done several times, with different transformations on each pass. This requires at least two RAMs. It is desirable to use a single bus system to tie the RAMs to the transformation logic, so that only one set of transformation logic is required.

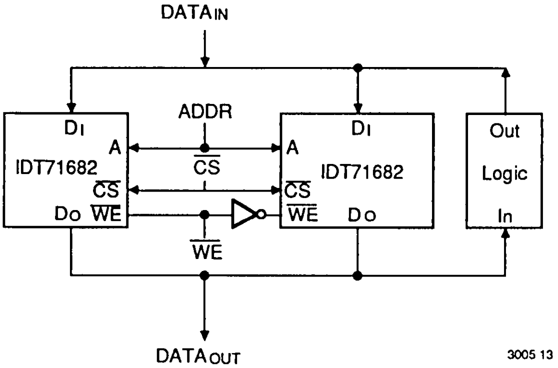


Figure 13. Ping Pong RAM

A significant speed improvement in a common bus design can be realized by using two separate I/O RAMs in an alternate read/write mode, as shown in Figure 13. In this approach, details initially read from the first RAM while transformed data is being stored in the second. Then, by changing the state of the $\overline{WE}$ input, data is read from the second RAM and new data can be written into the first RAM. In this fashion, one RAM is always in the read mode and the other is in the write mode. The $\overline{CS}$ can be used to remove both RAMs from the DATAOUT bus so it can be used by other devices. The $\overline{CS}$ line MUST be set inactive during a change of address to the RAM in the example shown in Figure 13. A speed improvement is realized in this configuration because the "data valid to end of write" time is faster than the "write cycle" time. This allows external logic to be performed on the DATAOUT and the result to be written back into the RAM at an overall higher system speed. In some designs, timing advantages can be realized by separating $\overline{CS}$, $\overline{WE}$, or both.

SUMMARY

Separate I/O CMOS static RAMs can provide the system designer with increased speed and reduced part count and their versatility will be demonstrated by creative design engineers in numerous applications beyond those discussed in this application note. These devices offer high-speed access times and high speed cycle times. The low power inherent in CMOS allows new levels of performance to be achieved in small, compact designs without the thermal problems of earlier bipolar designs. Certainly, these devices offer the system design engineer another tool in the search for improved system performance.

Integrated Device Technology, Inc.

CACHE TAG RAM CHIPS SIMPLIFY CACHE MEMORY DESIGN

APPLICATION NOTE AN-07

by SRAM Applications

ABSTRACT

Cache memories are a widely used tool for increasing the throughput of computer systems. The IDT7174 Cache Tag RAM is a new component designed to support direct mapped cache designs by providing the tag comparison on-chip. This allows relatively large cache memories to be designed with low chip count. The application of the IDT7174 to cache memory design is explored by designing a simple cache memory, reviewing its operation and performance, discussing methods of extending the design, and then reviewing the theory behind the design of cache memories in general.

INTRODUCTION

Cache memories are an important design tool for increasing computer performance by increasing the effective speed of the memory. Computer memories are usually implemented with slow, inexpensive devices such as dynamic RAMs. A cache memory is a small, high-speed memory that fits between the CPU and the main memory in a computer system. It increases the effective speed of the main memory by responding quickly with a copy of the most frequently used main memory data. When the CPU tries to read data from the main memory, the high-speed cache memory will respond first if it has a copy of the requested data. Otherwise, a normal main memory cycle will take place. In typical systems, the read data will be supplied by the cache memory over 90% of the time. The result is that the large main memory appears to the CPU to have the high speed of the cache memory.

The IDT7174 Cache Tag RAM introduced by IDT simplifies the design of high-speed cache memories. It can be used to make a high-performance cache memory with a low part count. The IDT7174 Cache Tag RAM consists of a 64K-bit static RAM organized as 8K x 8 and an 8-bit comparator, as shown in Figure 1. The comparator is used in direct mapped cache memories to perform the address tag comparison, and allows a 16K byte cache for a 68000 microprocessor to be built with four memory chips. The IDT7174 also provides a single pin RAM clear control which clears all words in the internal RAM to zero when activated. This control is used to clear the tag bits for all locations at power-on or system-reset when the cache is empty of data. This allows one of the comparison bits to be used as a cache data valid bit.

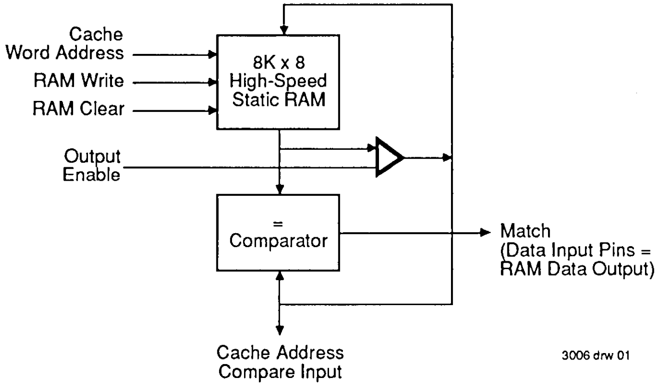


Figure 1. IDT7174 Cache Tag RAM Block Diagram

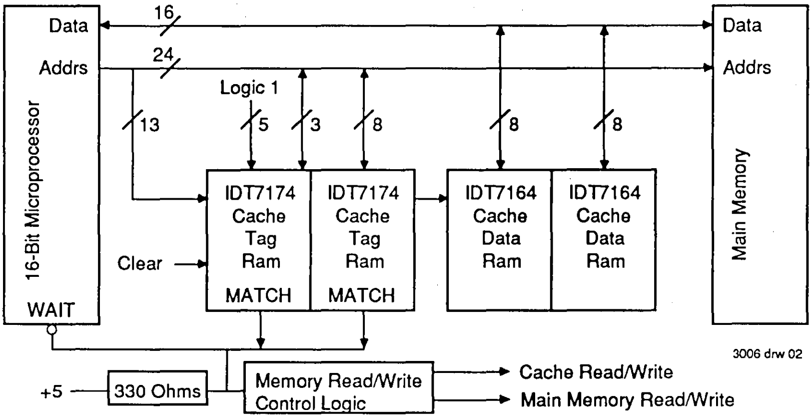


Figure 2. Cache Memory System Block Diagram

DESIGN OF A CACHE MEMORY

To understand the application of the IDT7174 to cache memories, we will begin by designing one. A block diagram of a cache memory system using IDT7174 Cache Tag memory chips is shown in Figure 2. The cache memory serves a 16-bit microprocessor with a 24-bit address bus and a main memory. In this system, the 13 least significant bits of the address bus are connected to the address inputs of both the cache tag and the cache data RAM chips. The upper 11 bits of the address bus are connected to the data I/O pins of the cache tag RAMs. The remaining five I/O pins of the cache tag RAMs are connected to a logic 1 (+5).

The MATCH outputs of the cache tag RAMs are tied together and connected to the WAIT input of the microprocessor. A 330 ohm pull-up resistor is used because the MATCH outputs are open-drain type. The MATCH outputs are positive-active. The MATCH output goes high when the contents of the internal RAM are equal to the data on the I/O pins. When several cache tag RAMs have their MATCH outputs connected together, a wire-AND function results: all of the comparators must each register a match before the common MATCH signal can go high.

In the system shown, the state of the WAIT input to the microprocessor determines whether the memory data is to come from the cache or the main memory. If the WAIT input to the microprocessor is high, the microprocessor will accept data immediately from the cache data RAMs; if the WAIT input is low, the microprocessor will wait for the slower main memory to respond with the data.

To understand how the cache memory operates, we will follow its operation from start-up in an initially empty state. When the system is powered-up, the cache tag RAMs are cleared to zero by a pulse to the initialize pins of the IDT7174 RAMs.This causes all cells in the RAM to be simultaneously cleared to logic zero.When the microprocessor begins its first read cycle, the 13 least significant bits of the address bus select a location in the cache tag RAMs. The location in the cache tag RAMs is compared against the upper bits of the address bus and against five bits of logic one.

The MATCH output of the cache tag RAMs will be low because all cache tag RAM cells were reset to zero, and the zeros from the selected cell are being compared against the five bits of logic one. In this case, the microprocessor waits for the slower main memory to respond. This is called a cache miss.

When the main memory responds with read data for the microprocessor, this data is also written into the cache data memory at the address defined by the 13 least significant bits of the address bus. At the same time, the upper 11 bits of the address bus and the five bits of logic one are written into the cache tag memory. This 11-bit address tag, in combination with the 13 bits of RAM address select, uniquely identify the copy of the main memory data that was stored. The five logic one bits serve as a data valid bits which indicate that the data in the cell is a valid copy of main memory data.

When the microprocessor requests data from the same location that has been written into the cache, the upper address bits on the address bus will be the same as the bits which were previously written into the cache tag RAM and the MATCH signal will go high.This is called a cache hit. In this case, the cache data is gated onto the data bus and the memory cycle is complete.

If the microprocessor requests data from an address with the same 13 least significant bits as a word in the cache, but with different upper address bits, a cache miss will result and the current (more recent) data will be written into the cache. In this manner, the cache is continuously updated with the most recently used data.

Memory write cycles are treated differently from read cycles. On write cycles, data is written directly into main memory and into the cache. This is called the write-through method of cache updating. Since all data is written immediately into main memory, it always contains current information. Data is written into the cache on full word writes or on byte (i.e. partial word) writes if a match occurred. Writing bytes into the cache only if a cache match occurs ensures that the full word in the cache is valid. For example, this ensures valid data for a byte write followed by a word read.

The design in Figure 2 uses unbuffered writes. In unbuffered writes, all write cycles occur at main memory speeds. This slows down the system for all write cycles at the expense of simple memory controls; however, this may be acceptable since only 15% of all memory cycles are write cycles in typical programs. Buffered write is a slightly more complicated method which improves performance. In buffered write cycles, the write data and address are loaded into registers, and the main memory write cycle proceeds in overlap with other processor operations. Since the next few cycles will probably be read cycles and their data will come from the cache, the result is that buffered write cycles are as short as cache read cycles.

CACHE MEMORY DESIGN: PERFORMANCE

Even a simple cache memory can improve system performmance. For a simple, 16-bit cache system such as described above, a hit rate (percentage of read cycles that are from the cache) of 68% can be expected. If IDT7174 Cache Tag RAMs and IDT7164 cache data RAMs are used, an access time at the chip level of 35ns results and a corresponding system cache read or write cycle time of 50ns is practical. Assuming a system cache access time of 50ns and a main memory system access time of 250ns, the average access time of an unbuffered cache would be 134ns and the average access time of a buffered cache would be 104ns. This corresponds to an improvement in access time of 1.9:1 and 2.4:1, respectively.

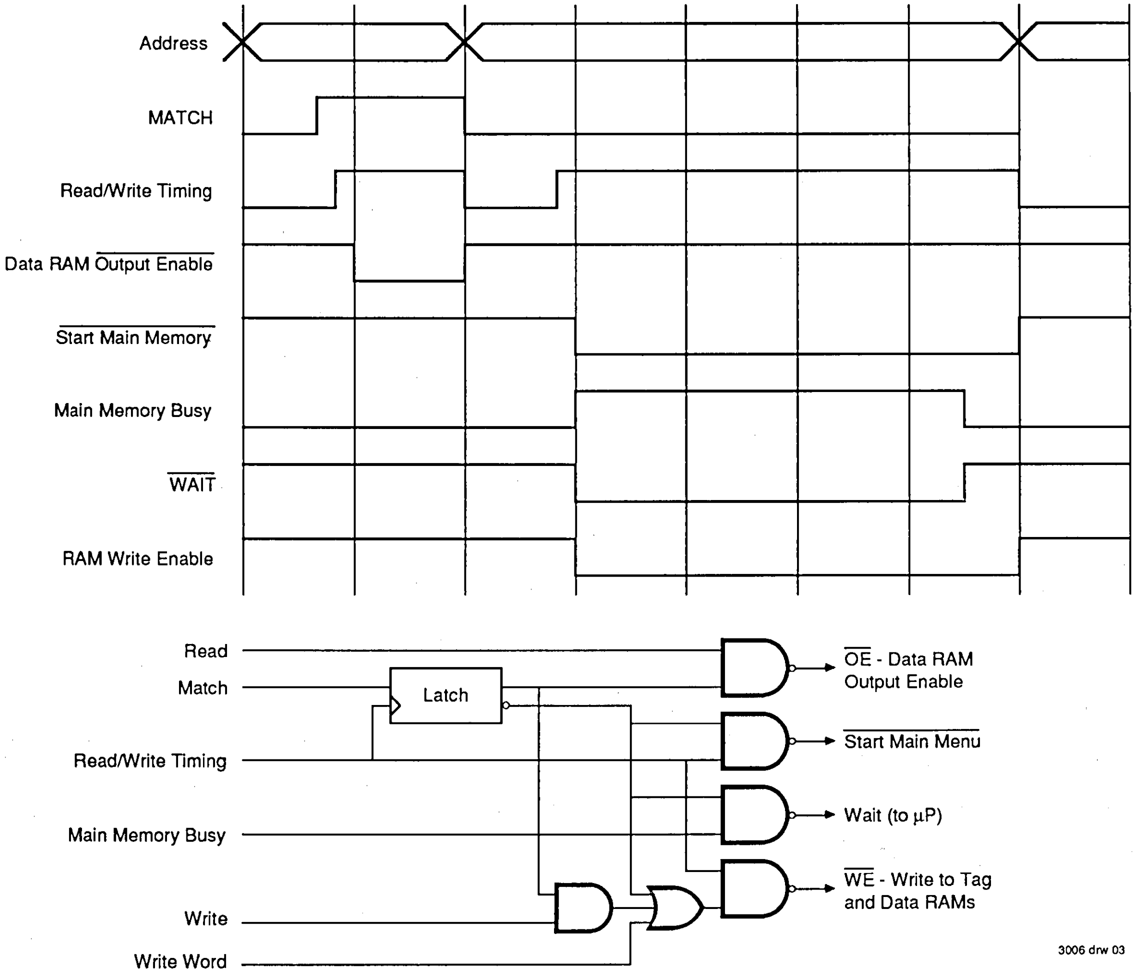


Figure 3. Cache Memory Control Timing and Logic Block Diagrams

CACHE DESIGN DETAILS: CONTROL LOGIC

Figure 3 shows a block diagram of a control logic design and a typical timing diagram for the cache memory of Figure 2. The vertical lines in the timing diagram represent 50ns timing intervals. The microprocessor is assumed to have a 50ns clock and a 100ns memory cycle time. In the timing diagram and associated logic,a Read/Write Timing signal is used to determine whether to use the cache data or to start the main memory.This timing signal is the memory read/write request signal from the CPU delayed by 37ns; the address-to-match time of the IDT7174. If main memory is used, this timing signal is used to write the main memory data into the cache RAMs on both the main memory read and write cycles. Data is written into the cache on write cycles only if there is a match or if it is a word write operation. The state of the MATCH line is latched by the Read/write Timing signal so that it remains stable during cache write operations.

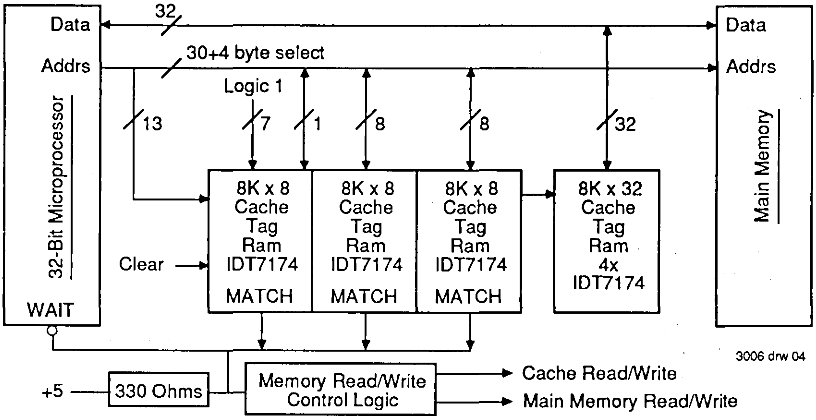


Figure 4. 32-Bit Cache Memory System

CACHE DESIGN DETAILS: UNCACHED ADDRESSES

In the above cache design, we have assumed that all parts of memory are cached; however, there are significant exceptions to this assumption. Hardware I/O addresses should not be cached because they do not respond in the same way as normal memory locations. Bits in an I/O register can and must change at any time, asynchronously, with respect to the rest of the system. A cache copy of an earlier I/O state is clearly not a valid response to an I/O read request under these conditions. Also, an I/O register address may be used for different functions for read and write, so that what is read will not be the same as what was written. For example, write-only control bits will not appear when read, and read-only bits will not be affected by write operations. For these reasons, hardware I/O addresses must always force cache misses. This can be accomplished by adding an I/O address decoder to the memory address bus to force a cache miss. (This decoder aleady exists in many systems to enable the I/O subsystem.)

CACHE DESIGN DETAILS: DMA ADDRESSES

Direct Memory Access (DMA) allows I/O devices such as disk controllers to have direct access to main memory by temporarily stopping the CPU and taking control of the memory address and data buses. If DMA devices are allowed to write into main memory without updating the cache memory, cache data could become invalidated because it would no longer be a copy of the contents of main memory. The simplest solution to this problem is to have the cache monitor the memory bus and be updated if an address match occurs in the same manner as CPU write-through operations. Otherwise, the I/O DMA buffer areas of memory must be forced to be uncached in the same manner as hardware I/O addresses.

CACHE DESIGN DETAILS: EXPANDING THE CACHE IN WIDTH

The cache as described above, can be expanded in both width and depth. For a 32-bit system, two additional IDT7164 cache data RAMs (for a total of 4 chips) will be required to store the 32-bit data words. A block diagram of a 32-bit cache system, with a 32-bit address bus, is shown in Figure 4. Compared with Figure 2, the number of cache data RAMs has been expanded from two to four to handle the expansion of the data bus from 16 to 32 bits, and the number of cache tag RAMs has been expanded from two to three to handle the expansion of the address bus from 24 to 32 bits.

Note that the cache memory system uses the memory address lines corresponding to the 32-bit words stored in the cache. If a byte addressing memory address convention is used, the least significant bit of the address lines going to the cache RAM chips is A2, with A1 and A0 used to select the byte(s) within the word to be read or written in the cache data RAMs.

There is a benefit to expanding the cache width by adding data RAMs: the miss rate improves. The miss rate improves because of the increase in width, as well as in the amount of data stored. The miss rate for a 8K x 32-bit cache is estimated at 12.4%, as compared to 32% for a 8K x 16-bit cache. Doubling the cache width by adding RAM chips doubles the amount of data stored. We would expect an improvement in miss rate due to the increased probability of finding the data in the cache.

There is an additional improvement in miss rate, however, specifically due to the increase in width. This is because there is a high probability that the next word the CPU wants is the next word after the current one. If the cache width is doubled, there is a 50% probability that the next word is already in the cache, fetched from main memory along with the current word.

Studies have shown that the miss rate is cut almost in half for each doubling of the cache data word width—called line size in cache theory—up to 16 bytes and larger (Smith 85). The disadvantage of very wide cache data word width is either a wide main memory data bus or complex logic to transfer the word to the cache in a high-speed serial burst. Simply doubling the number of main memory cycles does not work well because you have doubled the effective access time of the main memory but have cut the miss rate by less than half, yielding a net decrease in performance.

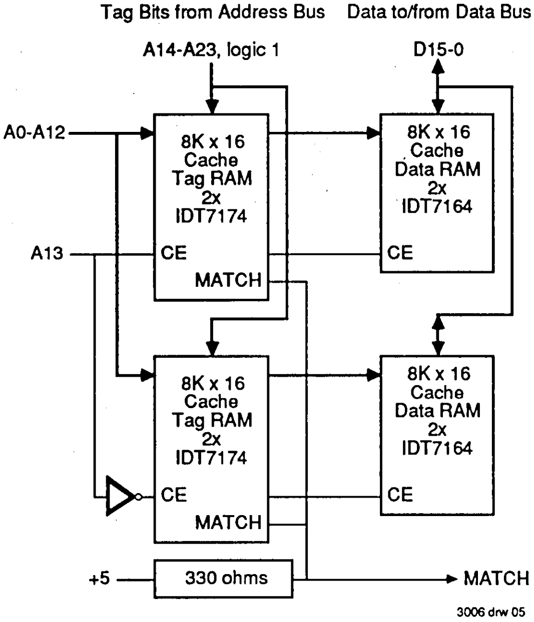


Figure 5. Depth Expanded Cache Memory System

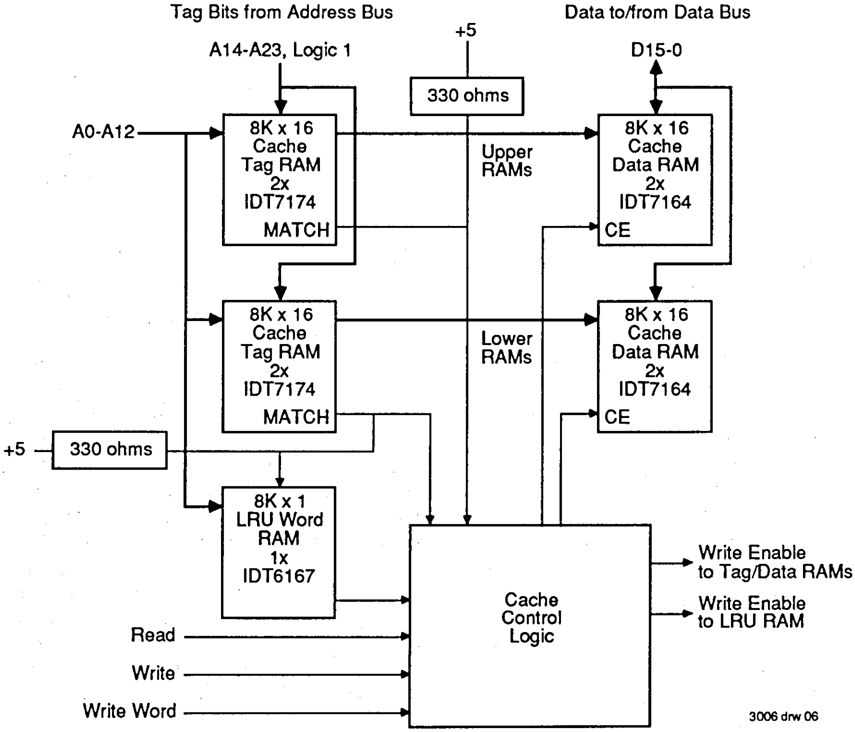


Figure 6. 2-Way Set Associative Cache Memory System

CACHE DESIGN DETAILS: EXPANDING THE CACHE IN DEPTH

The cache memory can be expanded in depth by adding copies of the cache tag and data chips and using upper bits of the address bus for chip enable selection. An example of an expanded cache is shown in Figure 5. The primary reason for increasing the size of the cache memory is to decrease the miss rate percentage. For example, increasing the cache size from 8K x 16 to 16K x 16 decreases the estimated miss rate from 32% to 22%.

CACHE DESIGN DETAILS: SET ASSOCIATIVE EXPANSION

A better way to expand the cache memory in depth is called set associative expansion (shown in Figure 6), and its control logic (shown in Figure 7). In this example, we have two independent cache memories which results in a two-way set associative cache. If a match is found in one of the memories, its data is gated to the data bus. If no match is found, one of the two memories is selected and updated. Selection of one of the two memories for cache write update is done by using an additional 8K x 1 memory to hold a flag for each cache word, indicating which memory was read last. This way, the least recently used cache word of the pair is updated.

The cache system described above attacks the problem of having two frequently used words mapped to the same cache word. For example, if a program loop included an instruction at 200B2 (hexadecimal) and called a subroutine at 800B2, the cache word 00B2 would be alternately registered as a cache miss and updated with memory data from each of these two addresses. The above design solves this problem by having two independent memories. One would cache the instruction at 200B2 and the other would cache 800B2.

Two way set associative expansion, while more complex in control logic, achieves a better miss rate. For example, the estimated miss rate for a 16K x 16 set associative cache is 18% versus 22% for a simple 16K x 16 cache.

CACHE THEORY: HOW IT WORKS

A cache memory cell holds a copy of one word of data corresponding to a particular address in main memory It will respond with this word if the address on the main memory address bus matches the address of the word stored. A cache memory cell therefore has three components. These components are an address memory cell, an address comparator, and a data memory cell, as shown in Figure 8. The data and address memory cells record the cached data and its corresponding address in main memory. The address comparator checks the address cell contents against the address on the memory address bus. If they match, the contents of the data cell are placed on the data bus.

Function	Match	Action
Read	Yes	Enable corresponding data RAM for read
Write	Yes	Enable corresponding data RAM for write
Read	No	Write main memory data into LRU RAM
Write Word	No	Write data into LRU RAM

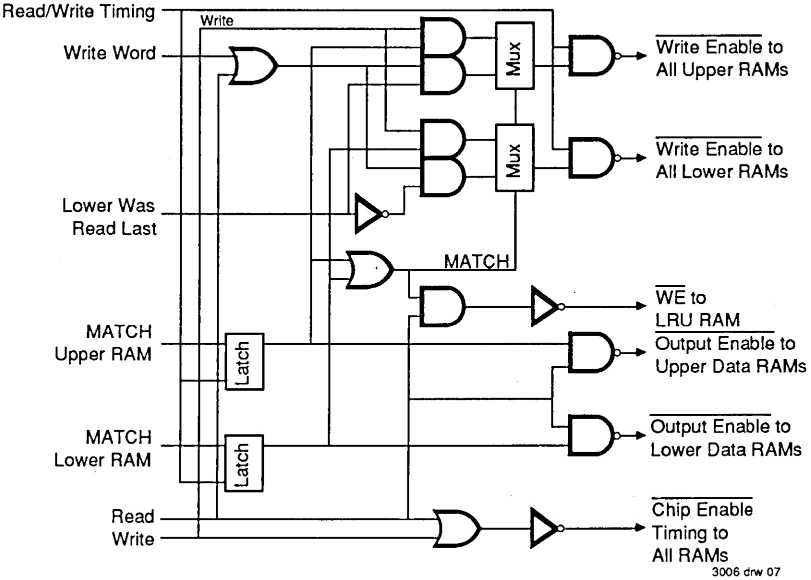


Figure 7. 2-Way Set Associative Cache Control Logic Block Diagram

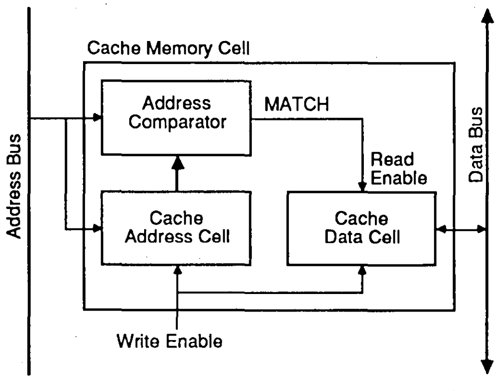


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Figure 8. Cache Memory Cell Block Diagram

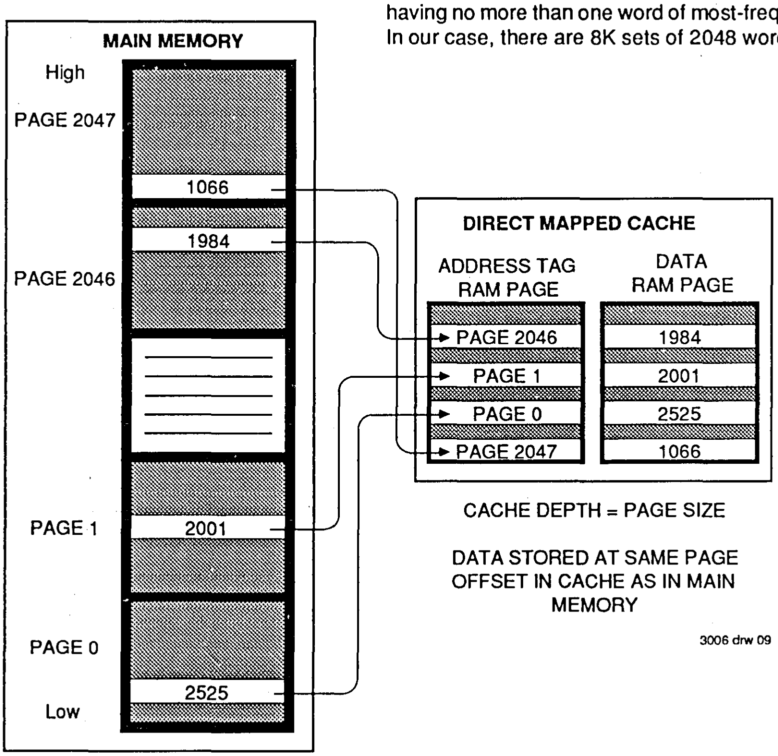
An ideal cache memory would have a large number of cache memory cells with each of them holding a copy of the most frequently used main memory data. This type of cache memory is called fully associative because access to the data in each memory cell is through its associated, stored address. This type of memory is expensive to build because the address cell and address comparator are generally several times larger, in terms of chip area or part count, than the data cell. Also, the address comparator required for each associative memory cell makes the design of the cell different from that of standard RAM memory cells. This makes a fully associative memory a custom design, precluding the use of efficient standard RAM designs.

CACHE THEORY: WHY IT WORKS

Cache memories work because computer programs spend most of their memory cycles accessing a very small part of the memory. This is because most of the time the computer is executing instructions in program loops and using local variables for calculation. Because of this observation, a 64K byte cache can have a 90+% hit rate on programs that are megabytes in size.

HOW THE DIRECT MAPPED CACHE WORKS

The direct mapped cache memory is an alternative to the associative cache memory which uses a single address comparator for the cache memory system and standard RAM cells for the address and data cells. The direct mapped cache is based on an idea borrowed from software called hash coding which is a method for simulating an associative memory. In a hash coding approach, the memory address space is divided into a number of sets of words with the goal of each set having no more than one word of most-frequently-used data. In our case, there are 8K sets of 2048 words each.



CACHE DEPTH = PAGE SIZE

DATA STORED AT SAME PAGE OFFSET IN CACHE AS IN MAIN MEMORY

3006 drw 09

Figure 9. Cache System Memory Map

Each set is assigned an index number derived from the main memory address by a calculation which is called the hashing algorithm. This algorithm is chosen to maximize the probability that each set has no more than one word of most-frequently-used data. In the direct mapped cache, the hashing algorithm uses the least significant bits of the memory address as the set number. This uses the concept of locality, which assumes that the most often used instructions and data are clustered in memory. If locality holds, the least significant bits of the address should be able to divide this cluster into individual words and assign each one to a separate set.

A memory map of a direct mapped cache of Figure 2 is shown in Figure 9 as an example of how the main memory words are related to the cache words. The 16M Word main memory is divided into 8K word pages, a total of 2048 pages. Each word within each 8K page is mapped to its corresponding word in the 8K words of the cache; i.e., word 0 of the cache corresponds to word 0 in each of the 2048 pages (8K sets at 2048 words/set).

Each word in the cache stores one word out of its set of 2048 corresponding to one of the 2048 possible pages. Both the data word and the page number (i.e. upper address bits), are stored.

Since only one word in each set (one of 2048 words in our case) is assumed to be one of the most-frequently-used words, each set has a single cache memory cell associated with it. This cache cell consists of an address cell and a data cell, but no comparator. One comparator is used for the cache memory system since only one set can be selected for a given memory cycle and only one comparison need be made. In a memory cycle, one set is selected, and the single cache address cell for that set is read and compared against the memory address, and the data from the cache data cell is placed on the bus if there is a match. The advantage of this scheme is that a single comparator is used, allowing standard RAM memories to be used to store the cache address and data for each set.

The cache cell for each set should hold the data that was most frequently used. However, since we do not know which data was the most frequently used until after the program is run, we approximate it by storing the most recently used data and replacing the least recently used (oldest) data. In the direct mapped cache, this is done by replacing the cache cell contents with the newer main memory data in the case of a cache miss.

CACHE PERFORMANCE

A cache memory improves a system by making data available from a small, high-speed memory sooner than would otherwise be possible from a larger, slower main memory. The performance of a cache memory system depends upon the speed of the cache memory relative to the speed of the main memory and on the hit rate or percentage of memory cycles that are serviced by the cache.

The cache performance equations below express the idea that the average speed of the cache memory is the weighted average of the cycle times for cache hits plus the main memory time for cache misses, with memory writes dealt with as a special case of 100% cache miss or 100% cache hit for the unbuffered and buffered cases, respectively.

CACHE SYSTEM PERFORMANCE: MISS RATE

One of the key parameters in a cache memory system is the miss rate. Miss rate figures are estimates derived from statistical studies of cache memory systems. The miss rate is an estimate because it varies, often significantly, with the program being run. Miss rate estimates for various cache memory configurations are given in Table 1. Miss rates for one example of two-way set associative expansion are also shown in this table.

Size: Words/Tag RAM	Miss Rate for Cache Data Word Width - Bits				Notes
	16	32	64	128	
2K	0.57	0.23	0.10	0.04	
4K	0.40	0.18	0.07	<0.04	
8K	0.32	0.12	0.05	<0.04	
16K	0.22	0.09	<0.04	<0.04	
16K (8K + 8K)	0.18	0.07	<0.04	<0.04	2-way Set Assoc

Table 1.

The miss rate estimates given in Table 1 are derived from simulation studies. (See references.) These studies covered cache sizes of up to 32K bytes and cache data word widths (called line sizes in cache terminology) from 4 bytes through 64 bytes. In the case of 16-bit word width caches, the figures given are extrapolations from the 32-bit data. Also, the figures for cache sizes above 32K bytes (i.e., 16K x 32, etc.) are extrapolations from 32K byte data.

CACHE SYSTEM PERFORMANCE FOR READ CYCLES

Cache memory system performance is determined by the access time of the main memory, the access time of the cache, the miss rate (the percentage of memory cycles that are not serviced by the cache) and the write time. The effective access time of a cache memory system can be expressed as a fraction of the main memory access time. This dimensionless number, Ps, is a measure of cache performance. If we consider read cycles only, the access time of a cache memory system is:

$$Ts = (1 - M)Tc + MTm = (1 - M)Tc + MTm$$

$$Ps = Ts/Tm = (1 - M)(Tc/Tm) + M = (1 - M)Pc + M$$

Where:

Ts = Cache average system cycle time, averaged over read and write

M = Miss rate of cache

Tc = Cache cycle time, read or write (assumed to be equal)

Tm = Main memory cycle time, read or write (assumed to be equal)

Pc = Cache memory access time as a fraction of main memory cycle time

Ps = Cache system access time as a fraction of main memory access time

If the miss rate of a cache memory is 100%, Pc= 1.00. If the cache memory is infinitely fast corresponding to a cache access time of zero, Pc will be equal to the miss rate, M. For real cache memories, the access time of the cache is finite. This means that the cache system access time will approach the cache access time as the miss rate approaches zero. This is shown in Figure 10.

CACHE SYSTEM PERFORMANCE FOR READ AND WRITE CYCLES

Memory write cycles affect the average access time of the cache system. In a write-through design unbuffered write cycles are equivalent to cache misses, while buffered write cycles are equivalent to cache hits. Unbuffered write cycles take a main memory cycle to write data for every write. If the main memory write cycle time is the same as the read cycle time, this is equivalent to a cache miss. In buffered write, data is written into the cache and into a register for later off-line write into the memory. Thus, the write cycle in the buffered write case is equivalent to a cache cycle. Each write cycle in the

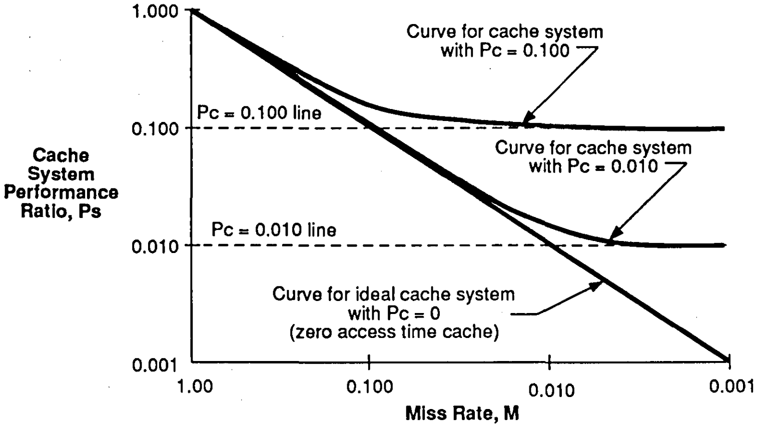


Figure 10. Cache Access Time vs Miss Rate for Read Cycles

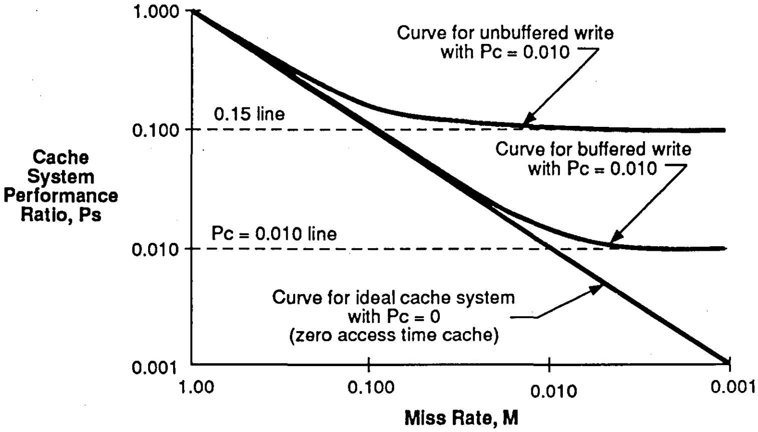


Figure 11. Cache Access Time vs Miss Rate for Buttered and Unbuffered Write Cycles

buffered case is, therefore, equivalent to a cache hit. The performance equations for this case are:

$$Ps = R((1 - M)Pc + M) + W(Tw/Tm)$$

For unbuffered writes:

$$Ps = R((1 - M)Pc + M) + W$$

For buffered writes:

$$Ps = R((1 - M)Pc + M) + WPc$$

Where:

R = Fraction of total memory cycles that are read cycles
W = Fraction of total memory cycles that are write cycles
Tw = Write time = Tm for unbuffered, Tc for buffered writes

The effect of unbuffered write cycles is to limit the maximum performance of the cache system. For the average case where write cycles are approximately 15% of the total number of memory cycles, this is approximately equivalent to a cache memory performance of 0.15, as shown in Figure 11.

CACHE SYSTEM PERFORMANCE IN TERMS OF AVERAGE MEMORY ACCESS TIME

Although cache memory systems can be evaluated in terms of the dimensionless performance parameter, Ps, you often need to calculate the actual access time for a specific system. This is expressed by:

$$Ts = R((1 - M)\ Tcr + MTmr) + WTw$$

Where:

Ts = Cache average system cycle time, averaged over read and write
R = Percentage of memory cycles which are read cycles = 85% typical
W = Percentage of memory cycles which are write cycles = 15% typical
M = Miss rate of cache = 10+% typical
Tcr = Cache read cycle time
Tmr = Main memory read cycle time
Tw = Write cycle time: main memory for unbuffered write, cache for buffered

For typical values:

$$\begin{aligned} Ts &= 0.85(0.9Tcr + 0.1\%mr) + 0.15Tw \\ &= \mathbf{0.765Tcr + 0.085Tmr + 0.15Tw} \end{aligned}$$

For unbuffered write and Tcr = 50ns, Tmr = Tw = 250ns:

$$Ts = 0.765(50) + 0.085(250) + 0.15(250) = \mathbf{97.0ns}$$

For buffered write and Tcr = Tw = 50ns, Tmr = 250ns:

$$Ts = 0.765(50) + 0.085(250) + 0.15(50) = \mathbf{67.0ns}$$

CACHE SYSTEM PERFORMANCE IN TERMS OF CPU WAIT STATES

In many computer and microprocessor systems, the purpose of the cache memory system is to eliminate CPU wait states, clock periods where the processor is stopped waiting for the memory. The cache performance calculations for this condition are more properly expressed in terms of processor wait states as follows:

$$\begin{aligned} Ncw &= R((1 - M)\ Ncr + (1 - H)Nmr) + WNw \\ &= RMNmr + WNw \text{ If: } Ncr = 0 \text{ (no wait states for cache)} \end{aligned}$$

Where:

Ncw = CPU average number of wait states, averaged over read and write
R = Percentage of memory cycles which are read cycles
= 85% typical
W = Percentage of memory cycles which are write cycles
= 15% typical
M = Miss rate of cache = 10+% typical
Ncr = Cache read cycle time wait states (typically 0)
Nmr = Main memory read cycle wait states
Nw = Write cycle wait states: main memory wait states for unbuffered write, cache wait states for buffered

For unbuffered write and Ncr = 0 wait states, Nmr = 3 wait states:

$$Ncw = 0.085(3) + 0.15(3) = \mathbf{0.705\ wait\ states}$$

For buffered write and Ncr = Nw = 0 wait states, Nmr = 3 wait states:

$$Ncw = 0.085(3) + 0.15(0) = \mathbf{0.255\ wait\ states}$$

CACHE SYSTEM PERFORMANCE IN TERMS OF CPU THROUGHPUT

The reason for adding a cache to a CPU is to improve throughput by eliminating wait states. CPU throughput improvement, as a result of adding a cache, can be expressed as the ratio of the speeds before and after adding the cache. For our purposes, CPU throughput improvement can be equated to memory throughput improvement. CPU throughput for this case can be defined as the CPU clock frequency divided by the number of clock states per memory cycle. The speed improvement provided by the cache can therefore be expressed as the ratio of the throughput with the reduced number of wait states provided by the cache to the throughput with full wait states:

$$\begin{aligned} Fc &= \frac{fclk/(No + Ncw)}{fclk/(No + Nm)} \\ &= (No + Nm)/(No + Ncw) \end{aligned}$$

Where:

fclk = Frequency of processor clock
N = Number of clock cycles per memory cycle
Ncw = Number of wait states for cache system (average)
Nm = Number of wait states for main memory
No = Number of processor states per memory cycle with no wait states
Fc = Processor throughput relative to throughput without cache

A 68010 microprocessor requires four clock states per memory cycle, i.e. No=4. Assuming a 12.5MHz clock and 250ns main memory access time, Nm = 2 wait states. If we use the unbuffered write case from the clock state analysis above, Ncw = 0.535 The throughput improvement provided by the cache is therefore:

$$Fc = (4 + 2)/(4 + 0.535) = 6/4.535 =$$

1.32 = 32% throughput increase

This is equivalent to increasing the CPU clock speed from 12.5MHz to 16.5MHz.

CACHE MEMORY PERFORMANCE: HOW MUCH DO YOU NEED?

A simple, direct mapped cache memory system, as described above, is often the most cost effective design. In many cases, the effort to decrease the miss rate beyond that of a simple design may not be worth the increase in system performance.

For example, if Pc is greater than 0.20 corresponding to a cache access time greater than 20% of the main memory access time, it may not be cost effective to improve the hit rate above 90%. This is because there is a knee in the curve of performance improvement versus miss rate at the point where Pc = miss rate, as shown in Figure 10. In some cases, even the added expense of buffered write may not be justified. To examine the relationship between CPU throughput and miss rate, CPU thorughput improvement versus miss rate for various microprocessors is shown in Table 2.

Miss Rate	Throughout Relative to Uncached System			
	68010 Unbuffered	68010 Buffered	68020 Unbuffered	RISC Buffered
1.00	1.00	1.00	1.00	1.00
0.80	1.06	1.12	1.19	1.27
0.60	1.13	1.20	1.32	1.49
0.40	1.20	1.28	1.49	1.79
0.20	1.29	1.38	1.71	2.24
0.10	1.34	1.44	1.84	2.56
0.05	1.37	1.47	1.92	2.76
0.00	1.40	1.50	2.00	3.00

Table 2.

Tag RAM Size	68010 Unbuffered			68020 Buffered			RISC Buffered		
	Chips	Miss	Perf	Chips	Miss	Perf	Chips	Miss	Perf
8K	4	0.32	1.24	7	0.12	1.81	7	0.12	2.49
16K	8	0.22	1.28	14	0.09	1.86	14	0.09	2.60
8K+8K S.A.	9	0.17	1.31	15	0.07	1.89	15	0.07	2.68

Table 3.

The data shown is for three CPU/cache systems. The 68010 microprocessor system has a 12.5MHz clock and a cache with unbuffered write. The 68020 system has a 16MHz clock and a buffered write cache. The RISC CPU assumes a 10MHz RISC computer with a 10MHz clock and a buffered write cache, and assumes one clock per memory cycle with wait states equal to an integral number of clock cycles.

Using the data in Table 2, we can make an interesting comparison between chip count and performance gained over an uncached system. Table 3 gives this comparison, showing the chip counts, miss ratios, and performance improvement gain for simple, depth expanded, and two-way set associative expanded caches. The chip counts given are for the cache tag and data RAM chips required, but do not include chip counts for the control logic. One RAM chip is added for the two-way set associative case for the least-recently-used cache flag RAM.

Table 3 shows that the throughput improvement created by expanding the cache above a minimum chip count design is small. This table can be interpreted in two ways. In small systems where the goal is to achieve high-performance at minimum chip count, the table indicates that a mimum chip count cache is best since it buys the most performance improvement per chip; doubling the cache chip count purchased less than 10% further increase in performance in all cases. In larger systems where the goal is to achieve maximum performance at moderate chip count, the table indicates that a further increase in performance of 5-8% can be obtained by adding fewer than ten chips.

CACHE DESIGNS: DIFFERENT WAYS TO MAKE ONE

The cache memory described above is a direct mapped cache. It is a simple, commonly used design with respectable performance. Further investigation into the technology of cache memories will reveal a wealth of other approaches to cache design. Much of the variety comes from attempts to maximize the performance of relatively small cache memories typical of earlier technology. Fortunately, there exists some data to help sort out the relative value of the various approaches. This data is in tha form of studies on cache memory performance as a function of cache size, organization, word width, etc., such as the excellent work done by Prof. Alan Jay Smith of the University of California at Berkeley (see references). These studies provide background and insight on how to achieve the highest performance out of cache memory systems, as well as documentation of a wide variety of cache schemes which do and do not work. The following comments are intended to provide a simplified guide to, and summary of, some of this data. The following comments are, in large part, judgments and opinions derived from the data in various reports and do not necessarily reflect the opinions of the original authors of the data.

WHAT WE HAVE LEARNED ABOUT CACHE MEMORY DESIGN

A simple, direct mapped cache as discussed above will give good performance if it is large enough. The ultimate measure of cache memory performance is its effect on system cycle time, which is a function of cache cycle time relative to main memory cycle time and the hit rate of the cache. Given a cache cycle time, miss rate becomes the measure of cache performance. Improving cache perfomrance, therefore, means improving the hit rate. However, a simple design with a moderate miss rate may be sufficient for many applications, giving most of the performance improvement that could be achieved by a more sophisticated design.

Much of the work that has been done on cache architecture and design was aimed at maximizing the performance of relatively small caches, consistent with the capabilities of earlier technologies. With today's technology, in the form of chips such as the IDT7174, we can easily make large cache memories at low chip counts that are at the upper limit of the earlier technologies. As a result, much of the sophistication required in smaller cache designs, in order to achieve an acceptablehit rate, is not required in today's large cache designs.

CACHE ARCHITECTURE: DIRECT MAPPED vs SET ASSOCIATIVE

A pure cache memory should be an associative memory, where the cache contains all of the most recently used data words. The direct mapped and set associative designs are approximations to this which sometimes exclude recently used words when there is more than one frequently used word per set. Fortunately, the difference between associative, set associative and direct mapped can be quantified. The ratios of miss rates for set associative and fully associative, relative to the direct mapped case, are shown in Table 3A. For example, if the miss rate for a direct mapped design is estimated at 0.20, the miss rate for a two-way set associative design of the same size would be (0.78)(0.20) = 0.156.

What this chart tells us is that two-way set associative caches have a significant performance improvement over simple direct mapped caches, but there is little additional improvement beyond four-way set associative designs. As was noted earlier, the set associative method can often be included in depth expanded cache designs where the two (or more) sets of cache hardware required for the expansion can be arranged to work in a set associative manner.

Cache Type	Ratio of Miss Rate to Direct Mapped
Direct Mapped	1.00
2-Way Set Assoc	0.78
4-Way Set Assoc	0.70
8-Way Set Assoc	0.67
Fully Associative	0.66

Table 3a.

CACHE SIZE

Cache sizes on commercial systems have tended to range from 16K to 64K bytes. Caches smaller than 16K can have significantly higher miss rates, while caches larger than 64K may not significantly improve the miss rate. This is shown above in Table 1. Much work has been done on the relationship between cache size and miss rate; however, most of this work is concerned with small caches, 32K bytes and under. The IDT7164/1DT7174 combination allows 16K byte cache memory design for 16-bit systems and a 32K-byte design for 32-bit systems using a minimum number of chips, and can be easily expanded to 64K and larger if desired.

WRITE THROUGH vs COPY BACK

There are two general approaches to handling the memory write problem: write through and copy back. In the write through approach, memory data is written into main memory as it is received from the CPU. In the copy back mode, memory data is written into the cache and flagged with a dirty write bit which indicates that the word has been written into the cache but not into the main memory. The cache data is copied into main memory as a separate operation at some later time, and the dirty write bit is cleared. There appears to be little performance difference between the write through and copy back approaches. Since the write through approach is simpler in concept and easier to implement, it is the most often used method.

WRITE BUFFERING

A significant performance increase can be achieved with a single level of write buffering. Complete write buffering requires more than one level of buffering to cover the case of two write cycles closer together than the main memory write cycle time. A FIFO can be used to buffer more than one word of write data; however, the FIFO need be no deeper than four words, since no further performance results from making it deeper.

SPLITTING THE CACHE: INSTRUCTION/DATA, SUPERVISOR/USER

Splitting the cache into two smaller caches, one for instructions and one for data, seems like it would improve the hit rate; however, it doesn't. In theory, the CPU spends most of its instruction cycles in a small part of the program. By caching these separately from the more random data memory, the hit rate on the instruction portion should be improved. Alas, the studies show that splitting the cache into two pieces typically does no better—and in some cases does a lot worse—than leaving the cache in one piece. This is, perhaps, because the miss rate for data is degraded by more than the hit rate for instructions is improved.

LINE SIZE: MAIN MEMORY WORD WIDTH vs CACHE WORD WIDTH

We have considered cache sizes where the CPU word width, memory word width and cache data word width are the same size. Performance improvement can result if the main memory and cache words are wider than the CPU word. If the cache word width (called the line size) is doubled the miss rate is cut almost in half. This is because the next word the CPU wants from memory is often the word adjacent to the one it just used. Increasing the line size by a factor of two will lower the miss rate by almost a factor of two up to line sizes of 16 bytes and beyond. This is shown in Table 4.

There are two approaches to increasing line size in order to reduce miss rate: by increasing the memory data bus width, and by fetching a block rather than a word of data from memory. Increasing the data bus width (from 16 to 32 bits, for example) may be practical in some systems where additional performance is desired.

Cache Size	Miss Ratio for Increasing Line Size			
	Line Size (Size of Block From Main Mem to Cache)			
In Bytes	4 bytes	8 bytes	16 bytes	32 bytes
4K	1.00	0.586	0.364	0.262
8K	1.00	0.581	0.345	0.222
16K	1.00	0.569	0.330	0.203
32K	1.00	0.564	0.324	0.194

Table 4.

The other alternative is to transfer a block of bytes to the cache instead of a single word. This becomes significant in systems where there is a delay before data transfer from main memory, but where several words can be transferred quickly after the initial delay. An example of this concept is the page mode in dynamic RAM designs. In such a system, there may be an initial latency of 200ns to begin a memory read cycle but, once started, the memory may be able to transfer words at 100ns per word for blocks of up to 256 words. In this case, a line (block) size of 2-4 words may be used to significantly reduce the miss rate with moderate increase in the main memory cycle time.

SUMMARY

Cache memories have been extensively used in large computer systems to improve performance. Cache tag RAM chips allow this technology to be adapted to the small-to-medium system design at reasonable cost. Simple, direct mapped cache designs with low chip counts can be used to achieve significant performance improvements. High-performance and low miss rates are possible with simple designs due to the high speed and relatively large cache sizes possible with high-speed CMOS technology.

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Integrated Device Technology, Inc.

LOW-POWER AND BATTERY BACK-UP OPERATION OF CMOS STATIC RAMs

APPLICATION NOTE
AN-10

by SRAM Applications

INTRODUCTION

High-speed CMOS static RAMs are capable of very low-power operation in the standby mode when the chip is disabled. In a properly designed circuit, the standby power may be a few microwatts, as compared with several hundred milliwatts when the RAM is operating. This low-power capability can be used by the designer to reduce system power and heat loading. It also makes these parts suitable for battery backed permanent storage applications. In these applications, power is kept on the RAM at all times to avoid the loss of data when power is removed from the part. This is done by using a battery to supply power to the RAM when system power is shut off. In these applications, low standby power drain is important in order to achieve long battery life with a reasonably sized battery. In this application note, we study the operating and standby power modes of the CMOS static RAM, the methods for achieving low-power standby operation and some of the methods for implementing battery backup operation.

CMOS RAM Power Consumption

CMOS RAMs have five regions of operation with a different power consumption for each region. These regions are: dynamic operating, DC operating, TTL standby, CMOS standby and battery backup standby. In the dynamic operating region, the RAM is reading and writing at speeds up to its rated read/write cycle time. In the DC operating region, the RAM is enabled but not cycling: its address, data and control inputs do not change. In the TTL standby mode, the RAM is disabled with its various address, data and control inputs at TTL levels, either static or cycling at the rated cycle time. In the CMOS standby region, the RAM is disabled and all inputs are at CMOS levels (i.e., within 0.20 volts of ground or V_{CC}).The battery backup standby region is similar to the CMOS standby region, but with a reduced power supply voltage of 2.0 or 3.0 volts rather than the normal 5.0 volts. The five regions of operation are shown in Figure 1. It shows a plot of I_{CC} versus operating region for an IDT7187L25, a 64Kx1 CMOS static RAM with a 25ns access time. The highest current, I_{CC2}, occurs under dynamic operating conditions where the part is cycling at its access time, a frequency equal to $1/t_{AA}$. The device current decreases linearly with frequency to the static operating current, I_{CC1}. When the chip is disabled, current drops immediately to I_{SB}, the TTL standby current, or below. I_{SB} corresponds to the current drawn by the chip when it is disabled and with all inputs at TTL high or with all inputs changing at the rated cycle time. With the inputs at TTL high, each input circuit is in its linear threshold determining region and drawing supply current. The device current linearly decreases from I_{SB} to I_{SB1} as the various inputs are changed from TTL high levels to CMOS levels which are within 0.20 volts of V_{CC} or ground. I_{SB1} is the full CMOS standby current for 5.0 volt V_{CC}. There are two other CMOS standby cases, specified by I_{CCDR}. I_{CCDR} corresponds to I_{SB1} but is measured at two other power supply voltages, 2.0 and 3.0 volts. The I_{CCDR} specification is used in battery backup applications to calculate the battery size required for a given battery lifetime. The 2.0 or 3.0 volt power supply voltages correspond to those typically available from battery systems in battery backed applications.

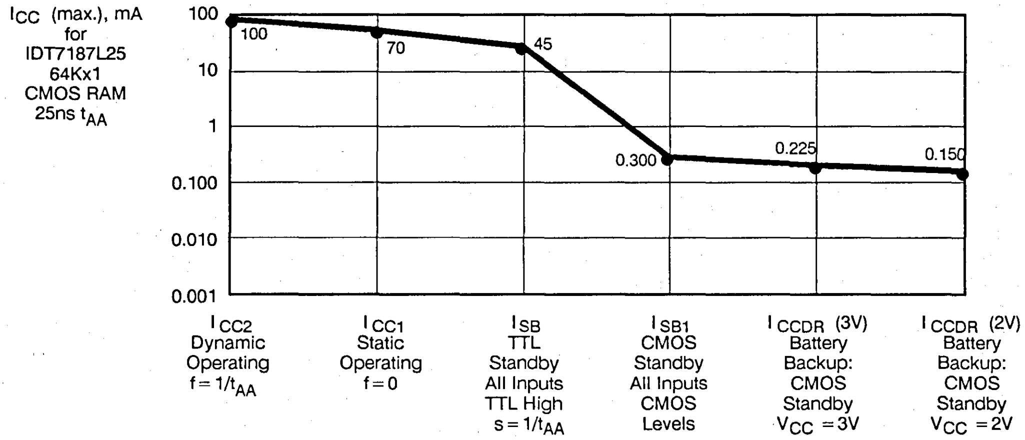

Figure 1. CMOS RAM Operating Regions

Components of Power Dissipation

There are five major sources of power dissipation in CMOS RAMs:

- The RAM array
- The sense amplifiers
- The input buffers
- Dynamic switching
- Diode leakage

The RAM array power is that required to power the RAM cells that hold the data. It is continuously drawn and is required to keep data stored in the RAM. The sense amplifier power is that required to read the data from the RAM array. It is drawn only when the chip is enabled. Each input to the RAM chip has a buffer which draws power when its input voltage is between 0.5 and 4.0 volts. In this region, the input buffer operates as a linear device, performing a logic threshold comparison. If the input is within 0.20 volts of V_{CC} or ground, the input buffer draws no power. Static RAMs draw additional power if they are cycled continuously at high speed. The additional power required is the dynamic switching power. It rises linearly with the average frequency of read/write cycles. Diode leakage is the current drawn by reversed biased diodes on the chip, such as CMOS gates that are not switching. It is a small value at room temperature, but it is strongly temperature-dependent, doubling approximately every +10°C. Because of its strong temperature dependence, it is usually the dominant component in CMOS standby power specifications, such as the I_{CCDR} specification used in battery backed RAM calculations. Diode leakage and RAM array power are two unavoidable components of RAM power dissipation.

Standard and Low-Power RAMS

IDT RAM chips are divided into two types, standard power and low power. This is indicated by a letter suffix to the part number, S or L, respectively. These part types are power dissipation test selections from a single product, similar to speed grade selections. The low-power part is selected for low-power standby operation and fully specified for the battery backup mode. The standard-power part has relaxed power specifications in the form of higher limits on all I_{CC} specifications, particularly the standby power modes, and it is not specified for battery backed operation. Because of its relaxed power specifications, it is usually less expensive. The standard-power part is used where very low standby power is not required, such as applications where the part is continuously enabled.

Dynamic Operating Current—I_{CC2}

The dynamic operating current specification applies when the RAM is cycling at its specified access time. In the case of the IDT7187L25, the access time is 25ns and the frequency at which I_{CC2} is measured is 1/25 = 40MHz. I_{CC2} consists of two components: the DC operating component, I_{CC1}, and a frequency dependent component equal to (I_{CC2} - I_{CC1}). In the case of the IDT7187L25, the I_{CC2} value is 100 milliamperes and the frequency dependent component is 100 - 70 = 30 milliamperes. Note that, as the specified access time goes down, the specified dynamic operating current goes up. This is because the dynamic operating current is measured at a frequency equal to the inverse of the access time. Fast access RAMs are measured at higher frequencies than slow ones and have higher frequency dependent current components.

The dynamic current component of I_{CC2} is the result of transient currents in the internal CMOS gates when they switch. These transient currents can be understood by examining the switching behavior of CMOS circuits. The basic building block of CMOS circuits, including RAMs, is the CMOS logic gate. An example of a simple CMOS gate, an inverter, is shown in Figure 2. It consists of an N-channel device, Q1, and a P channel device, Q2. If the input is high, Q1 will be on, Q2 will be off and the output will be low. If the input is low, Q2 will be on, Q1 will be off and the output will be high.

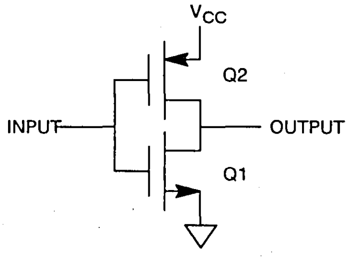

Figure 2. CMOS Inverter

This CMOS gate draws momentary current only when it changes state. It draws no current when its input is at ground or V_{CC} because one of the two transistors will be off, eliminating a direct path from V_{CC} to ground. This is what makes CMOS an inherently low-power technology—it draws no static current. However, it does draw current momentarily when it changes state. When the input transitions from low-to-high or high-to-low, it will pass through the middle region where both Q1 and Q2 are on. During this transition time, current will flow through Q1 and Q2. Since the current flows only during the transition time, there is a fixed amount of charge transferred from V_{CC} to ground for each transition. This results in a frequency-dependent current consisting of the sum of all the charges transferred for all the gates on the chip times the frequency of the charge transfers—i.e., the frequency of cycling the RAM.

Static Operating Current—I_{CC1}

The static current specification applies when the RAM is enabled but with its various inputs not changing and held at a TTL high. In this condition, the RAM array, sense amplifiers and input buffers are all drawing current. For the case of the IDT7187L25, this is 70 milliamperes.

TTL Standby Current—I_{SB}

The TTL standby current specification applies when the chip is disabled but its inputs are at TTL levels or changing at the rated cycle time. Since a TTL high represents the worst case condition, I_{SB} is specified for the case of all inputs at TTL high.

In the TTL standby mode, the RAM array and input buffers draw current, with the input buffers drawing the majority. The input buffers are CMOS circuits similar to the CMOS inverter shown in Figure 2, but with the geometry of the transistors designed so that the input threshold is at a TTL-compatible threshold voltage of approximately 1.40 volts. A diagram of the device current versus input voltage for one input is shown in Figure 3. When the input is within 0.20 volts of ground or V_{CC}, one of the two transistors is turned off and no current flows. Very little current flows even for the TTL low case of 0.50 volts input. However, for the TTL high case of 3.0 volts typical, both transistors will be on and approximately 1.50 milliamperes, typical, will flow through them.

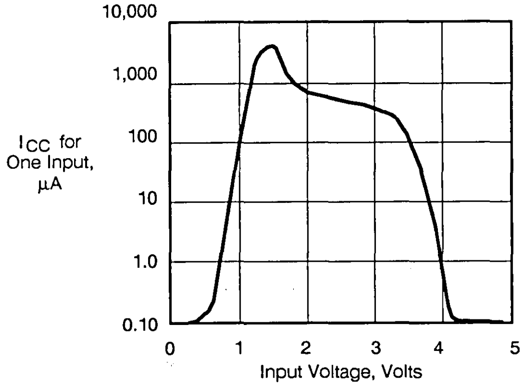

Figure 3. I_{CC} vs V_{IN} for One Input

CMOS Standby Current—ISB1

The CMOS standby current specification applies when the chip is disabled and all its inputs are static (i.e., nonchanging) at CMOS levels—within 0.20 volts of VCC or ground. In this state, only the RAM array and leakage currents are drawn. The RAM array current is relatively independent of temperature, while the diode leakage is strongly temperature dependent, rising dramatically with temperature. At +25°C, the total current for an IDT7187L25 consists primarily of RAM array current, which may be 25µA. However, at +70°C for commercial parts, the total current is specified at 300µA and is mostly leakage current. This rises to 1500µA at +125°C for military parts. A plot of ISB1 versus temperature is shown in Figure 4.

Battery Backed CMOS Standby Current—ICCDR

The battery backed CMOS standby current specification applies when the chip is disabled and all its inputs are at CMOS levels (i.e. within 0.20 volts of VCC or ground) and when VCC is at a reduced voltage of 2.0 or 3.0 volts. It is the same as ISB1 except it is measured at VCC voltages of 2.0 and 3.0 volts. In this state, only the RAM array and leakage currents are drawn.

When V_{CC} is reduced to 2.0 or 3.0 volts, the RAM is guaranteed to retain data stored at 5.0 volts, but may not function: i.e. it may or may not read or write reliably at these voltages. For this reason, the chip is kept disabled while VCC is below 5.0 volts. When VCC is restored to 5.0 volts, full functional operation is restored and the data will remain as it was before VCC was reduced.

DESIGN OF A HIGH-SPEED CMOS RAM MEMORY ARRAY

CMOS RAMs are often used in memory arrays. Figure 5 shows a CMOS RAM array used as high-speed main memory for a 32-bit microprocessor. The high speed of the CMOS devices allows operation of the microprocessor at full speed without wait states. Figure 6 shows an example of a design of such a memory array using techniques which allow high-speed operation at low power.

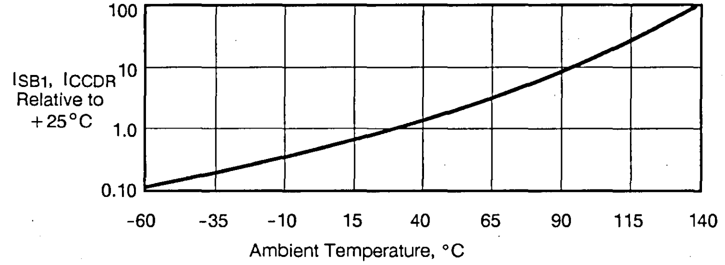

Figure 4. I_{SB1} and I_{CCDR} vs Temperature

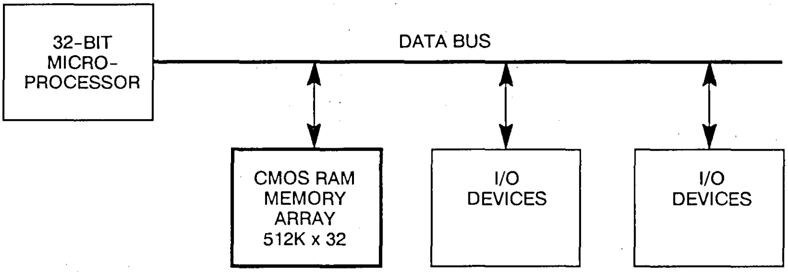

Figure 5. CMOS RAM Array with 32-bit Microprocessor

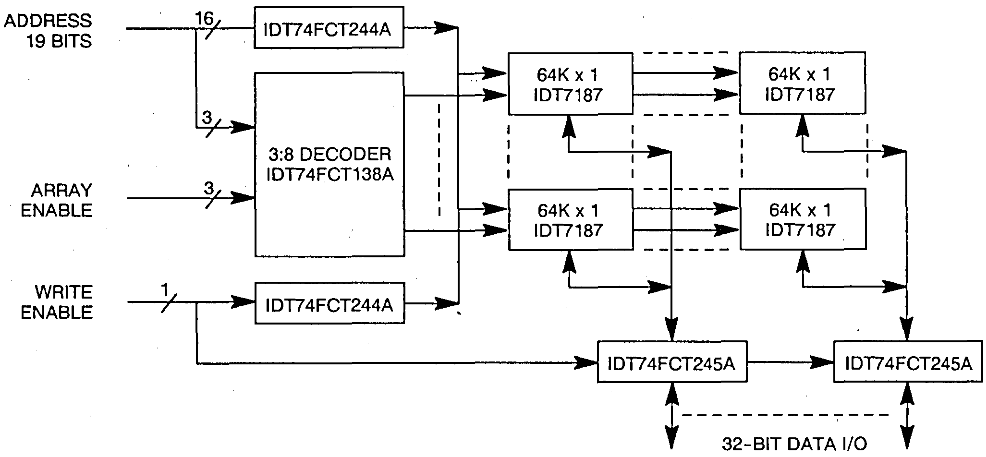

Figure 6. CMOS RAM Array Design

The 512Kx32 memory array of Figure 5 consists of 256 RAM chips, each 64Kx1, arranged as an array of eight rows of 32 devices. The array is driven by CMOS devices capable of driving the RAM inputs to CMOS levels within 0.2 volts of V_{CC} or ground. An IDT74FCT138A 3-to-8 line decoder enables one row at a time. If the decoder is disabled, all RAM chips are disabled. The address and write enable inputs are driven by IDT74FCT244A non-inverting buffers and the data lines are buffered by a set of IDT74FCT245A transceivers. Four sets of IDT74FCT244A buffers are used for the address and write enable inputs, with each buffer driving 64 chips. This reduces the capacitive loading on each buffer to maintain high speed. One set of IDT74FCT245A transceivers is used since each one drives only eight RAM data inputs.

CMOS RAM arrays draw significantly less power in standby mode if the RAM inputs are driven to CMOS levels. This is shown in Table 1 for the RAM array of Figure 6. In this table, the total current of the RAM array is shown for the case of TTL and CMOS drivers for the address and control lines.

Dynamic Operating Power for TTL vs CMOS Drivers				
Part	**Qty.**	**I_{CC} Using 74F Bipolar**	**I_{CC} Using FCTA CMOS**	**Comments**
IDT7187L25	32	3200	3200	Enabled, I_{CC2}
IDT7187L25	224	10,080	10,080	Disabled, I_{SB}
244	9	810	116	74F244/74FCT244A
245	4	440	52	74F245/74FCT245A
138	1	20	5	74F138/74FCT138A
Total		**14,550 mA**	**13,453 mA**	

Standby (non-operating) Power for TTL vs CMOS				
Part	**Qty.**	**I_{CC} Using 74F Bipolar**	**I_{CC} Using FCTA CMOS**	**Comments**
IDT7187L25	256	11,520	77	Disabled, I_{SB}/I_{SB1}
244	9	810	116	74F244/74FCT244A
245	4	440	52	74F245/74FCT245A
138	1	20	2	74F138/74FCT138A
Total		**12,790 mA**	**247 mA**	

Table 1. CMOS RAM Array Power

The power savings from using CMOS drivers can be dramatic, as shown in Table 1. The difference between the CMOS and bipolar current is only 7.6% in the dynamic case but, in the standby, non-operating case, the current differs by a factor of 51.8. The lower standby current with CMOS drivers occurs because the RAM inputs are kept at CMOS levels, putting them into the I_{SB1}, CMOS standby region. Using CMOS drivers does not, however, put the unselected rows into the I_{SB1} region during dynamic operation of the array. This is because the address and data inputs to the unselected RAM chips are changing rather than being held at static levels. Thus, I_{SB} must be used instead of I_{SB1} in these calculations.

The dynamic and standby I_{CC} specifications assume that the RAM is cycling at its rated cycle time. The cycle time of the RAM array will be longer than the rated cycle time of the RAM chips. This will reduce both the dynamic operating current of the enabled row and the standby power of the disabled rows. A conservative estimate of the current requirement reduction can be made by reducing the current of the disabled rows by the ratio of the RAM chip rated cycle time to the RAM array cycle time. If the RAM chip cycle time is 25ns and the RAM array cycle time is 100ns, the current required by the disabled rows will be (0.25*10,080 + 0.75*67) = 2,570mA. The current savings will be (10,080-2,570) = 7,510mA. The RAM array operating current will therefore be (13,453 - 7,510) = 5,943mA, a reduction of 56%.

RAM Array Speed Considerations

CMOS RAM arrays can achieve low power while maintaining high speed. This is done by using the high speed of the CMOS RAM chips and taking care that speed is not lost in the surrounding logic. The primary problem in driving large RAM arrays is driving the capacitance of the address and data inputs.

The speed of the array is a combination of the propagation delay of the RAM chips, the circuits driving them and the time delay caused by driving the capacitance of the array. The time delay caused by driving the capacitance depends on the design of the array. This delay is proportional to the capacitance being driven by each IC output, with a typical design value of 3.0ns/100pF for FCT logic and 6.0ns/100pF for RAM outputs. This delay applies to capacitance above the rated load capacitance for the device, which is 50pF for FCT devices and 30pF for the IDT7187 RAM. This delay applies for address and write enable drivers driving the RAM chip inputs and for each RAM chip driving other RAM outputs and its IDT74FCT245 input. In this design, the RAM chip input capacitance is 5.0pF/input, and the output capacitance is 7.0pF/output. Since the RAM data input and output pins are connected together, the total capacitance is (5.0+7.0) = 12.0pF/RAM chip. Thus, each RAM output must drive seven RAM outputs, eight RAM inputs and one IDT74FCT245 input for a total of (7*7+8*5+5=5)=94pF. The net capacitance used in the delay calculation is (94-30) = 64pF and the corresponding delay is (6*64/100) = 3.84ns.

If one set of drivers is used to drive all the devices, the capacitance can be high and the delay can be significant compared to the delay of the RAM chips. In high-speed designs, several drivers are used so that the capacitance seen by each driver is moderate and the speed delay is small. A comparison of the total propagation delay of a RAM array for various combinations of drivers is shown in Table 2.

To design a RAM array for high speed, both the address and chip select paths must be considered. In Table 2, the propagation delay with capacitive loading is calculated for both paths and the larger of the two numbers is used to calculate the access time of the array as a whole. Note that the critical path changes from address to chip select as the capacitive loading of the address drivers is reduced.

Address and Chip Select Path Delays vs Capacitive Drive

Delay Source	256/Driver		64/Driver		32/Driver		16/Driver	
	Cap	Delay	Cap	Delay	Cap	Delay	Cap	Delay
IDT74FCT244A	-	4.3	8	4.3	16	4.3	32	4.3
Addr Cap Delay *	1280	36.9	320	8.1	160	3.3	80	0.9
IDT7187L25 - t_{AA}	-	25.0	-	25.0	-	25.0	-	25.0
Addrs Path Delay	-	66.2	-	37.4	-	32.6	-	30.2
IDT74FCT138A	-	5.8	-	5.8	-	5.8	-	5.8
$\overline{CS}$ Cap Delay *	160	3.3	160	3.3	160	3.3	80	0.9
IDT7187L25 - t_{ACS}	-	25.0	256	25.0	256	25.0	256	25.0
$\overline{CS}$ Path Delay	-	34.1	-	34.1	-	34.1	-	31.7

* 3ns/100pF - 50pF

RAM Array Access Time vs Capacitive Drive

Delay Source	256/Driver		64/Driver		32/Driver		16/Driver	
	Chips	Delay	Chips	Delay	Chips	Delay	Chips	Delay
IDT74FCT244A	2	-	8	-	16	-	32	-
IDT7187L25	256	-	256	-	256	-	256	-
IDT74FCT138A	2	-	2	-	2	-	4	-
Path Delay	-	66.2	-	37.4	-	34.1	-	31.7
IDT74FCT245A	4	4.6	4	4.6	4	4.6	4	4.6
Out Cap Delay **	-	3.8	-	3.8	-	3.8	-	3.8
TOTAL	264	74.6	270	45.8	278	42.5	296	40.1

** 6ns/100pF - 30pF

Table 2. CMOS RAM Array Speed vs Drive

Using RAM Modules to Save PC Board Space

RAM modules can be used to significantly reduce the printed circuit (PC) board area required for a RAM array. A RAM array using 256 chips (of the IDT7187 type) will require approximately (0.4 * 1.2 * 256) = 122.88 square inches of board space, assuming 24-pin, 300 mil DIP devices with 0.1 inch spacing. RAM modules, such as the IDT7M624, use surface mounting to fit sixteen of the IDT7187 RAM chips on a 2.0 x 0.9 inch DIP module. Sixteen of these modules could directly replace the 256 RAM chips in the array. The PC board area using these modules would be (16*2.0*1.0) = 32 square inches, assuming 0.1 inch spacing, a savings of approximately a factor of four over mounting individual chips.

ARRAY DESIGN FOR LOW POWER

The RAM array design of Figure 6 can be redesigned for lower operating power by using CMOS RAM chips with input gating, such as the IDT7164, 8K x 8 RAM. An example of such a design is shown in Figure 7. Table 3 compares the characteristics of the low-power design in Figure 7 against the high-speed design in Figure 6.

In parts with input gating, the input circuits are powered down when the chip is disabled. These parts have very low TTL standby I_{SB} values because only the chip select inputs are on in the TTL standby case. In RAM array design, this means that the disabled rows have very low standby power when compared to RAMs with conventional inputs, as used in the design of Figure 6.

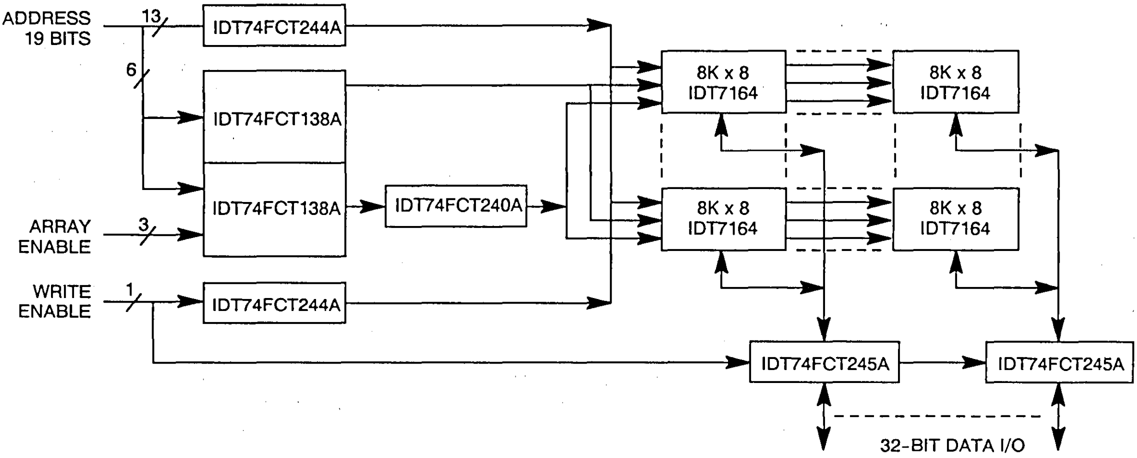

Figure 7. Low-Power CMOS RAM Array Design

Function	High-Speed Design	Low-Power Design	Units	Comments
RAM Chip Type	IDT7187	IDT7164		
Chip Organization	64Kx1	8Kx8		
Speed: t_{AA}	42.5	64.7	ns	32/driver
Operating Power	13,453	853	mA	
Standby Power	247	81	mA	
Part Count	278	276	ICs	32/driver
Battery Power, 3.0 V	81.6	30.5	mA	at +70°C

Table 3. Comparison of High-Speed vs Low-Power Array Designs

The 512K x 32 memory array in the low-power design shown in Figure 7 consists of 256 RAM chips, each 8K x 8, arranged as an array of 64 rows of 8 devices. The array is driven by CMOS devices capable of driving the RAM inputs to CMOS levels, within 0.2 volts of V_{CC} or ground. Two IDT74FCT138A, 3-to-8 line decoders are used with the two RAM chip selects to enable only one row at a time. An IDT74FCT240A inverter is used between one decoder and the RAM array to drive the positive active RAM chip enable. If either decoder is disabled, all RAM chips are disabled. The address and write enable inputs are driven by IDT74FCT244A non-inverting buffers and the data lines are buffered by a set of IDT74FCT245A transceivers. Four sets of IDT74FCT244A buffers are used for the address and write enable inputs, with each buffer driving 64 chips. This reduces the capacitive loading on each buffer in order to maintain high speed. Two sets of IDT74FCT245A transceivers are used to reduce the loading on the RAM output pins so that each RAM drives only 32 outputs.

The CMOS RAM array in Figure 7 draws significantly less power than the design in Figure 6, as is shown in Table 4. The primary reasons for this reduction are that the rows that are disabled draw very little power due to their gated inputs and only four RAMs in a row are enabled at any one time rather than 32. The result is that the dynamic power is reduced by a factor of 15.7 and the standby power is reduced by a factor of 3.0. Note that I_{SB1} is used in calculating the power of the disabled rows. This is because there is no dynamic standby effect with input gated RAMs since the input buffers are turned off. Also, since the chip enables are driven to CMOS levels by CMOS devices, there is no TTL standby current drawn by the chip select inputs.

Low-Power RAM Array Speed Considerations

RAM array speed considerations for the low-power design in Figure 7 are similar to those of the design in Figure 6. The delay for the address and chip select paths are calculated and the larger of the two numbers is used in calculating the total delay. The total delay for various combinations of driver loading is shown in Table 5.

RAMs with gated inputs (i.e., input buffers powered up by chip select) trade speed for low power. Gating the inputs with the chip select means that the chip select access time is equal to, or longer than, the address access time. This means that the chip select decode propagation delay is no longer hidden by a fast chip select access time. As a result, the chip select path is usually the critical path in gated input designs.

The design in Figure 7 is somewhat slower than the design in Figure 6 because x8 RAMs rather than x1 RAMs are used. In the minimum chip count configuration, each RAM output in Figure 6 drives seven other RAM outputs, plus an IDT74FCT245A input. In the minimum chip count design in Figure 7, each RAM output drives 63 other RAM outputs, plus an IDT74FCT245A input. This is the source of another tradeoff of speed versus chip count in the RAM output path. The output drive problem is helped by the fact that the IDT7164 RAMs are common I/O devices with a capacitance of 7.0pF per I/O pin, rather than the combined capacitance of 12.0pF for the IDT7187 design which ties the input and output pins together.

Dynamic Operating Power for Low-Power RAM Array

Part	Qty.	I_{CC} Using FCT CMOS	Comments
IDT7164L30	4	560	Enabled, I_{CC2}
IDT7164L30	252	50	Disabled, I_{SB1}
IDT74FCT244A	8	103	
IDT74FCT245A	8	103	
IDT74FCT138A	2	11	
IDT74FCT240A	2	26	
Total		853mA	13,453mA for Fig. 6.

Standby Power for Low-Power RAM Array

Part	Qty.	I_{CC} Using FCT CMOS	Comments
IDT7164L30	256	51	Disabled, I_{SB1}
IDT74FCT244A	8	12	
IDT74FCT245A	8	12	
IDT74FCT138A	2	3	
IDT74FCT240A	2	3	
Total		81mA	247mA for Figure 6

Table 4. CMOS RAM Array Power

Address and Chip Select Path Delays vs Capacitive Drive

Delay Source	**256/Driver**		**64/Driver**		**32/Driver**		**16/Driver**	
	Cap	**Delay**	**Cap**	**Delay**	**Cap**	**Delay**	**Cap**	**Delay**
IDT74FCT244A	-	4.3	8	4.3	16	4.3	32	4.3
Addr Cap Delay *	1280	36.9	320	8.1	160	3.3	80	0.9
IDT7164L30 - t_{AA}	-	30.0	-	30	-	30	-	30
Addrs Path Delay	-	71.2	-	42.4	-	37.6	-	35.2
IDT74FCT138A	-	5.8	-	5.8	-	5.8	-	5.8
IDT74FCT244A	-	4.3	-	4.3	-	4.3	-	4.3
$\overline{CS}$ Cap Delay *	160	3.3	160	3.3	160	3.3	80	0.9
IDT7164L30 - t_{ACS}	-	35.0	256	35.0	256	35.0	256	35.0
$\overline{CS}$ Path Delay	-	48.4	-	48.4	-	48.4	-	46.0

* 3ns/100pF - 50pF

RAM Array Access Time vs Capacitive Drive

Delay Source	**256/Driver**		**64/Driver**		**32/Driver**		**16/Driver**	
	Chips	**Delay**	**Chips**	**Delay**	**Chips**	**Delay**	**Chips**	**Delay**
IDT74FCT244A	2	-	8	-	8	-	8	-
IDT7164L30	256	-	256	-	256	-	256	-
IDT74FCT138A	2	-	2	-	2	-	4	-
IDT74FCT240A	2	-	2	-	2	-	3	-
Path Delay	-	71.2	-	48.4	-	48.4	-	46.0
IDT74FCT245A	4	4.6	4	4.6	8	4.6	16	4.6
Out Cap Delay **	-	25.1	-	25.1	-	11.7	-	4.9
TOTAL	266	100.9	272	78.1	276	64.7	287	55.5

** 6ns/100pF - 30pF

Table 5. CMOS RAM Array Speed vs Drive

BATTERY BACKUP OPERATION OF CMOS RAMS

Because of their low standby power, CMOS RAMs are often used as permanent memory where a battery is used to maintain data in the RAM by supplying power when the system power is off. These are called battery backup applications. In battery backup applications, the battery supplies a lower voltage—2.0 to 3.0 volts versus the 5.0 volts of normal operation. This lower voltage allows use of a smaller battery, both because of the lower voltage for the same ampere-hour rating and because the RAM draws less current at the lower voltage.

The design of a battery backed RAM array includes consideration of the following problems:

- Driving the RAM inputs to CMOS levels during battery operation
- Determining the power drain in battery backup mode
- Switching from the system supply to/from the battery supply while maintaining VCC at the RAM

Driving the RAM Inputs to CMOS Levels During Battery Operation

In order to achieve the low power levels specified for battery backup operation, the RAM inputs must be driven to CMOS levels. In the array design of Figure 6, this is done by driving the RAM chips with FCT CMOS drivers for the 5.0 volt VCC case. These levels must also be guaranteed for the 3.0 volt VCC, battery backed case. In the case of the FCT CMOS devices, the output drive is also specified to be at CMOS levels for the 3.0 volt VCC case.

The RAM array drivers must be able to maintain CMOS output levels with 3.0 volt VCC and maximum leakage from the RAM inputs and/or outputs. CMOS FCT drivers are used for the address, write enable, chip select and data inputs of the design in Figure 6. The worst case leakage will be for 64 address inputs being driven by a single driver. The maximum specified leakage for any input of the IDT7187L25 RAM chips is 2.0 microamperes at 3.0 volts VCC over the temperature range. The maximum total leakage for 64 inputs will then be 128 microamperes. The IDT74FCT244A drivers are rated at an I_{OL} of 300μA and an I_{OH} of 32μA at 3.0 volts V_{CC}. If the address drivers are kept in the low state, the 300μA I_{OL} specification is more than enough to keep the outputs at a CMOS low level.

Additional drivers are required to keep the write enable and chip select inputs in the CMOS high state. The write enable drivers can be kept in the low state if the RAM chips are kept disabled; however, it would be more prudent to keep them in the high state to ensure that no write can possibly occur. This requires more drivers for these lines than the address lines. With a 32μA I_{OH} specification, each CMOS FCT part can drive a maximum of 16 inputs. Since each IDT74FCT244A supplies eight drivers, this would mean two chips instead of one for the write enable input. Two IDT74FCT138A decoders will also be required in order to have each decoder output drive only 16 RAM enable inputs. A drawing of the RAM array with this implementation is shown in Figure 8.

The FCT CMOS drivers will keep the RAM inputs at CMOS levels during battery backup mode; however, the inputs to the FCT devices must also be kept at CMOS levels during this mode. If the rest of the system which communicates with the RAM array is powered down, these inputs should be at or near zero volts, which solves this problem. To ensure this case, a resistor to ground should be added to the input of each FCT CMOS device to provide a path for the input leakage of these devices. A 10K resistor will support the input leakage of ten FCT devices at 2μA per device and a V_{OL} of 0.20 volts.

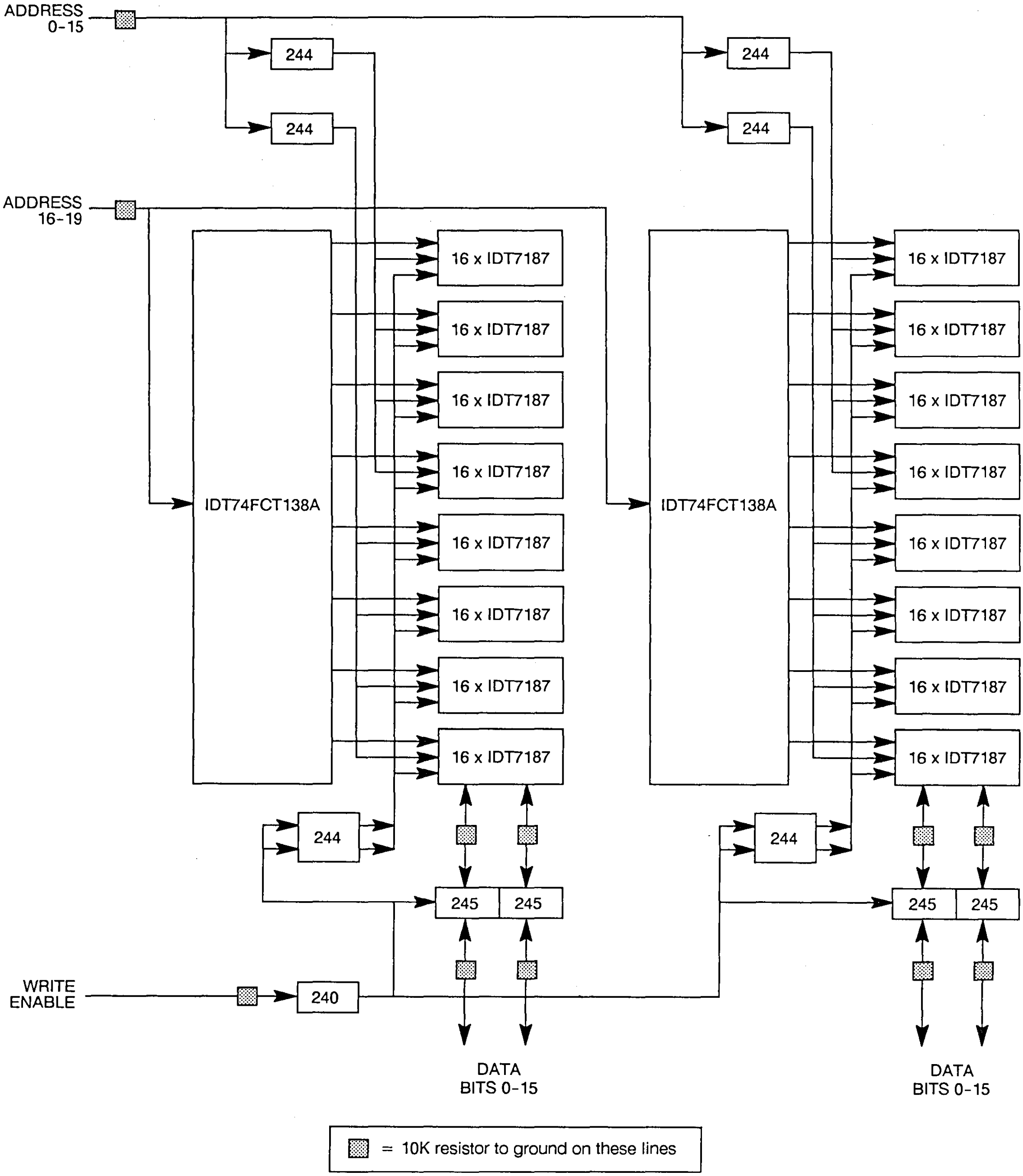

Figure 8. High-Speed CMOS RAM Array Design for Battery Standby

Determining the Current Drain in Battery Backup Mode

The RAM array standby current in battery backup can be calculated by adding the current required for the RAM chips and the current for the array drivers. A calculation of the current required for the RAM array of Figure 6 in the battery backup mode, including the additional drivers for write enable and chip select, is shown in Table 6.

Battery Backed Standby Current at 3.0 Volts				
Part	**Qty.**	**Typ., +25°C**	**Max., +70°C**	**Max., +125°C**
IDT7187L25	256	3.84	57.6	230.4
IDT74FCT244A	10	0.010	15.0*	15.0
IDT74FCT245A	4	0.004	6.0*	6.0
IDT74FCT138A	2	0.002	3.0*	3.0
Total	**272**	**3.9mA**	**81.6mA**	**254.4mA**

* Max. for commercially rated parts. Military rated parts will have lower values at +70°C.

Table 6. High-Speed CMOS RAM array Battery Standby Current

Battery Backed Operation of the Low-Power RAM Array Design

The low-power RAM array design in Figure 7 is well suited to battery backed operation. Because of the gated input design of the RAM chips, only the chip select inputs of the RAM need be driven to CMOS levels. This means increasing the number of decoders for the low active chip select from two to three so that each decoder drives a maximum of 16 inputs to V_{IH}. The non-inverting chip select input is not a problem because the IDTFCT240A driver will easily drive its 32 inputs to V_{IL}. Only the RAM chips, the IDTFCT138A decoders and the IDTFCT240A drivers need be powered by the battery.

The RAM array standby current in battery backup can be calculated by adding the current required for the RAM chips and the current for the array drivers. A calculation of the current required for the RAM array in Figure 7 in the battery backup mode, including the additional chip select decoders, is shown in Table 7.

Battery Backed Standby Current at 3.0 Volts				
Part	**Qty.**	**Typ., +25°C**	**Max., +70°C**	**Max., +125°C**
IDT7164L30	256	3.84	23.0	76.8
IDT74FCT138A	3	0.003	4.5*	4.5
IDT74FCT240A	2	0.002	3.0*	3.0
Total		**3.9mA**	**30.5mA**	**84.3mA**

* Max. for commercially rated parts. Military rated parts will have lower values at +70°C.

Table 7. Low-Power CMOS RAM Array Battery Standby Current

Switching Between System V_{CC} and the Battery

In a battery backup system, V_{CC} for the RAM array must switch between the battery and the system V_{CC} without causing the RAM to lose data in the battery backup mode and allowing the RAM to achieve full speed in the normal operation mode. This requires a switch design for V_{CC}. Also, the RAM array must be disabled during the battery backup mode and during switching between the battery and normal V_{CC}. This is done by using a power-down detect signal from the power supply which forces the RAM to be disabled.

When switching from the system to the battery, V_{CC} must be kept above the 2.0 volt minimum guaranteed data maintenance voltage at all times. When switching from the battery to the system, V_{CC} at the part must be within the V_{CC} specifications for nomal operation, (i.e., 4.5 volts minimum). These two requirements can be met by the circuit shown in Figure 9. In this circuit, the silicon diodes perform a smooth transfer of power from the system V_{CC} to the battery backed V_{CC} and vice-versa. The diode to V_{CC} is not strictly required because of the FET switch; however, it can reduce the switching transient when the FET turns on by reducing the voltage that must be switched, assuming that V_{CC} comes up slowly before the FET turns on.

The P-channel power FET is used to reduce the drop across the diode to 0.10 volt during normal operation so that the RAM array V_{CC} is kept within specifications. The IDT74FCT240A inverting driver is used to drive the gate of the P-channel power FET. When the power down signal is high, indicating normal system operation, the IDT74FCT240A output is low and the P-channel FET is on. When the power down signal is low, indicating that the power is going down or is already down, the IDT74FCT240A drives the

P-channel FET gate high to turn it off. When the battery is supplying the V_{CC}, the FET gate will be driven to the most positive voltage on either of its two terminals, ensuring that it will be off. Note that the circuit of Figure 1 is a typical example only—actual designs will differ depending on system requirements. For example, a PNP transistor or an N-channel FET with a gate drive to + 12 volts could be used instead of the P-channel FET.

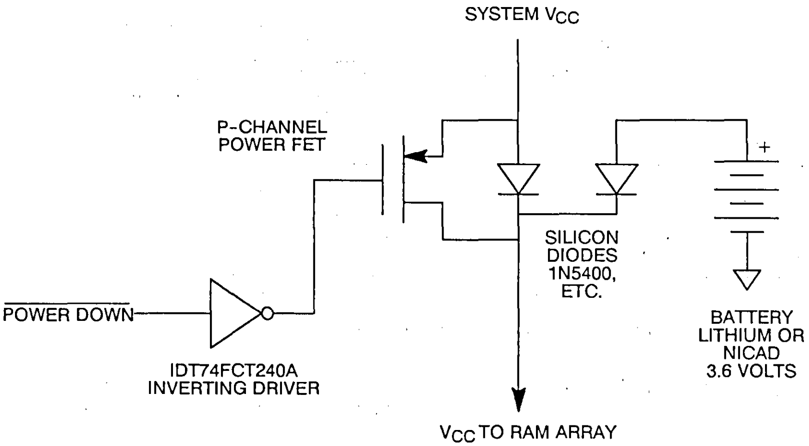

Figure 9. Battery Power Switch Circuit

CONCLUSION

CMOS RAMs have the capability of high speed and low power. In this application note, some of the possibilities for using these capabilities have been explored in the hope that the designer may use them to good advantage in new designs.

Integrated Device Technology, Inc.

STATIC RAM TIMING

APPLICATION NOTE AN-20

by SRAM Applications

INTRODUCTION

This application note is about timing parameters involved in the use of static RAMs. The application note describes these parameters, their individual meanings and their uses.

Optimum performance can be accomplished by understanding the timing of the memory element. A system which is designed using this knowledge will be fast and will not consume a lot of power.

The timing parameters are actually the reflection of the internals of the static RAMs. These internals will be discussed and the relationship between the timing at the cell level and the timing at the component level will become clear.

The timing parameters are divided into two groups: those that are involved with common I/O parts and those that are involved with the separate I/O parts.

In order to show the different aspects of the timing problem in static RAMs, two IDT 16K static RAMs will be used as examples.

The RAM Cell

In order to better represent the different timing parameters involved in read or write operations in static RAMs, we will start with the basic memory cell. The basic memory cell of Integrated Device Technology is the four transistor cell (4T Cell shown in Figure 1).

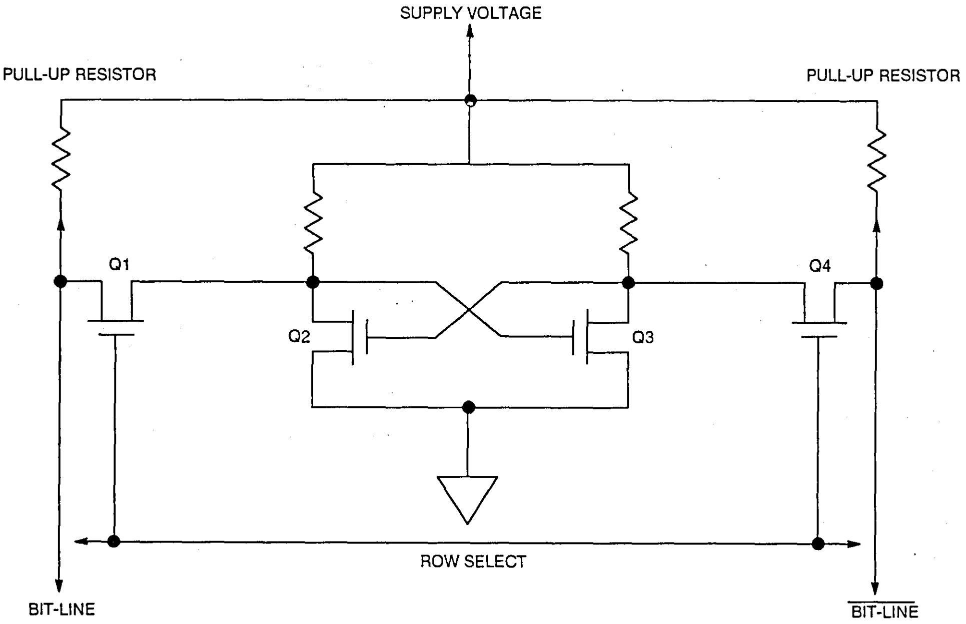

Figure 1. Four Transistor Cell

In the four transistor cell of Figure 1, transistors Q2 and Q3 constitute a latch. When Q2 is on, it keeps Q3 off, and when Q3 is on, it keeps Q2 off. A zero (0) bit is accomplished by Q2 on and Q3 off. A one (1) bit is accomplished by Q3 on and Q2 off.

WRITING INTO THE CELL

To write a one (1) into the cell, Row Select becomes active. Transistors Q1 and Q4 turn on. Bit-Line is forced high and $\overline{\text{Bit-Line}}$ is forced low. Transistor Q2 will turn off and transistor Q3 will turn on. Therefore, the contents of the latch becomes a "1".

READING FROM THE CELL

To read the contents of the cell, Row Select becomes active. Transistors Q1 and Q4 turn on. The state of the drains of transistors Q2 and Q3 becomes available on Bit-Line and $\overline{\text{Bit-Line}}$. One of the two Bit-Lines will be pulled down through Q1Q2 or Q3Q4. If Bit-Line is high and $\overline{\text{Bit-Line}}$ is low, the contents of the latch is a "1".

RAM

A RAM is a RAM cell together with some logic interface for read or write operations. Figure 2 shows a one-bit RAM with some logic interface in order to operate it.

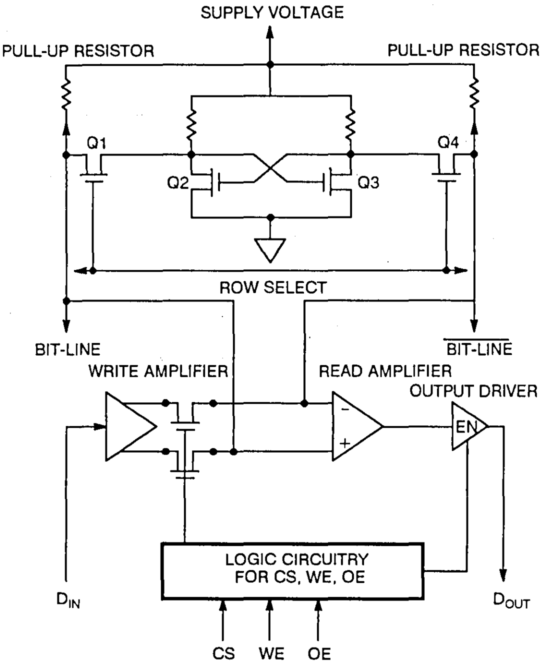

Figure 2. One-Bit RAM

WRITING TO THE ONE-BIT RAM

The writing operations of the one-bit RAM are performed in the following order:

- Force Bit-Line high and $\overline{\text{Bit-Line}}$ low (to write a "1")
- Row Select goes high to select the cell to be written
- Q1 and Q4 turn on
- Q2's drain is pulled high towards the supply
- Q3's drain is pulled down to ground level
- Q2's gate will be low, therefore Q2 is OFF
- Q3's gate will be high, therefore Q3 is ON

As shown in Figure 2, in order to write, the control logic has to enable the differential write amplifier that is placed in the path of D_{IN}. When a data bit has to be written into the latch, D_{IN} is put through that differential amplifier which will charge up one of the bit lines and will charge down the other. The Row Select line has already selected the appropriate latch, and finally, the data is written into the cell.

READING FROM THE ONE-BIT RAM

The reading operations of the one-bit RAM are performed in the following order:

- Row Select becomes active
- Q1 and Q4 turn on
- Bit-Line will charge to the value of the drain of Q2
- $\overline{\text{Bit-Line}}$ will charge to the value of the drain of Q3
- Read amplifier will evaluate the two Bit-Lines and will output the logic value corresponding to the content of the latch.

While reading from the latch, Row Select selects the appropriate latch. The control logic will enable the appropriate sense amplifier. The sense amplifier will sense the bit lines and output a value that will represent the content of the latch in question.

In Figure 2, the read amplifier is a differential amplifier that senses which bit line is being pulled low. Both bit lines start high and are pulled low by Q1Q2 or by Q3Q4. By sensing the movement of the bit line being pulled low, the time spent to determine the content of the latch is reduced.

A 2 x 2 RAM ARRAY

Before showing the general picture, let us examine the inner connections of four cells arranged as a 2-word-by-2-bit RAM. Figure 3 shows the configuration of this memory array. This array could be extended in both directions.

A0 selects the particular row that interest the user. If A0 is low, RS0 becomes active, and if it is high, RS1 becomes active. A1 selects the particular column that interest the user. If A1 is low, CS0 becomes active, and if it is high, CS1 becomes active.

In the manner described above, if the user would like to access the latch placed on the top left part of the Figure 3A, A1A0 = 00.

Latch (0,0) --> A1A0 = 00
Latch (1,0) --> A1A0 = 10
Latch (0,1) --> A1A0 = 01
Latch (1,1) --> A1A0 = 11

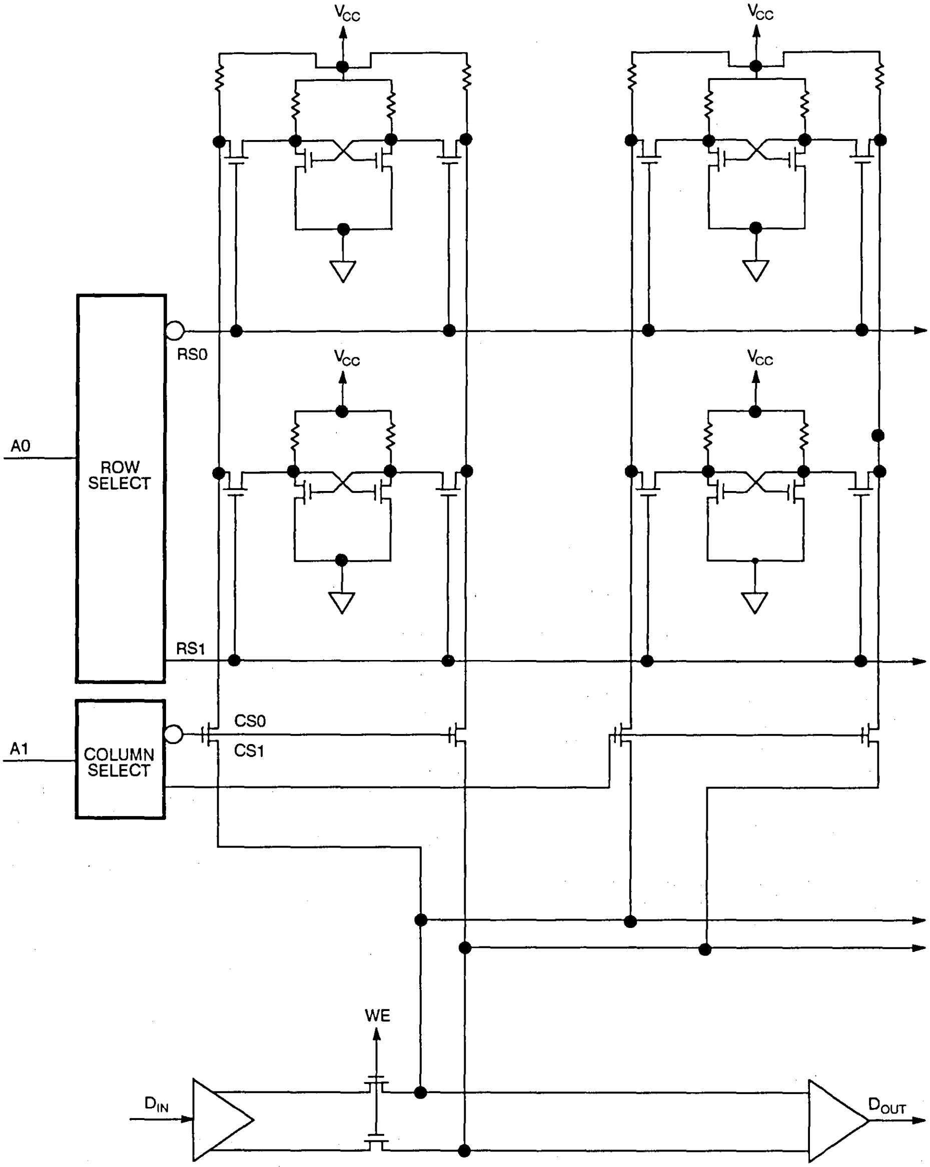

Figure 3. A 2 x 2 Array

A REAL PART

Before going into detail about the different aspects and trade-offs of the various approaches of reading or writing, let us take a look at Figure 4 which represents an actual part. This part has 16K of memory and is arranged in a 16K x 1-bit manner (IDT6167). It is similar to the array shown in Figure 3 but has been expanded from 2 x 2 to 128 x 128.

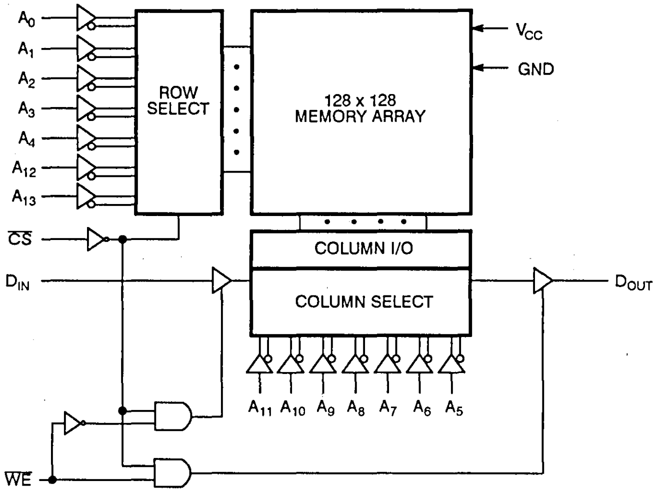

Figure 4. Functional Block Diagram of IDT6167 16K x-Bit

The selection of a particular row is done using address lines A0---A4, A12 and A13. The selection of a particular column is done using address lines A5---A11. The chip select line ($\overline{CS}$), enables the row select logic and the write/read signal. Data In and Data Out paths are controlled by $\overline{CS}$ and the $\overline{WE}$ signal. If $\overline{CS}$ and $\overline{WE}$ are active, the path for Data In becomes valid. If $\overline{CS}$ is active and $\overline{WE}$ high, the path for Data Out becomes active. If $\overline{CS}$ is not active, both paths are turned off.

WRITING METHODS: WE vs. CS CONTROLLED WRITE

There are also two different ways for executing a write, i.e. the $\overline{WE}$-controlled or the $\overline{CS}$-controlled write. For the $\overline{WE}$-controlled write, the basic steps that one should consider are:

- Bring the address bits to the address pins
- Wait for the address pins to settle
- Select the chip
- Strobe the Write Enable pin: This will turn on the write amplifier switches
- Bring the data bits to the data pins
- Terminate the strobe
- Keep the data bits stable for a while

Chip Select controlled write uses a slightly different set of steps :

- Bring the Write Enable low (enabled)
- Bring the address bits to the address pins of the IC
- Wait for the address pins to settle
- Strobe the Chip Select: This will turn on the bit and row select switches
- Bring the data bits to the IC data pins
- Terminate the strobe
- Keep the data bits stable for a while

READING FROM THE RAM ARRAY

During a read operation, the $\overline{WE}$ signal is high, disabling the write amplifiers and enabling the output drivers. In Figure 4, since the part is a by one (x1) part, there is only one output driver and one write amplifier.

Once the sense amplifier is active, the address lines (using the row and column select logic) enable a particular memory cell. The state of the cell is sensed by the sense amplifier (read amplifier) which in turn will output the corresponding logic level.

The user has to wait a certain amount of time for the read amplifier to sense the value of the latch. This amount of time will correspond to the access time of the device.

Here are some steps representing a read operation:

- Select the device ($\overline{CS}$ low)
- Enable the read amplifier or sense amplifier ($\overline{WE}$ high): This will actually turn on the driver at the output of the sense amplifier (see Figure 2)
- Wait for the access time
- Read the data bit out of the data bus

COMMON I/O AND SEPARATE I/O

What we have discussed is called a **Separate I/O** part. Separate I/O means that you have separate input and output paths. As far as the user is concerned, it means that, at the device level, the part has different pins for the Data In and Data Out bits.

A 2 x 2 COMMON I/O RAM ARRAY

There are also other memory parts that are called **Common I/O** RAMs. A common I/O part has only one path for the data bits and this path is bidirectional. At the cell level in a common I/O part, the D_{IN} line is connected directly to the D_{OUT} line. Figure 5 illustrates the idea of a common I/O part at the cell level. It represents a 2 x 2 common I/O array of RAM.

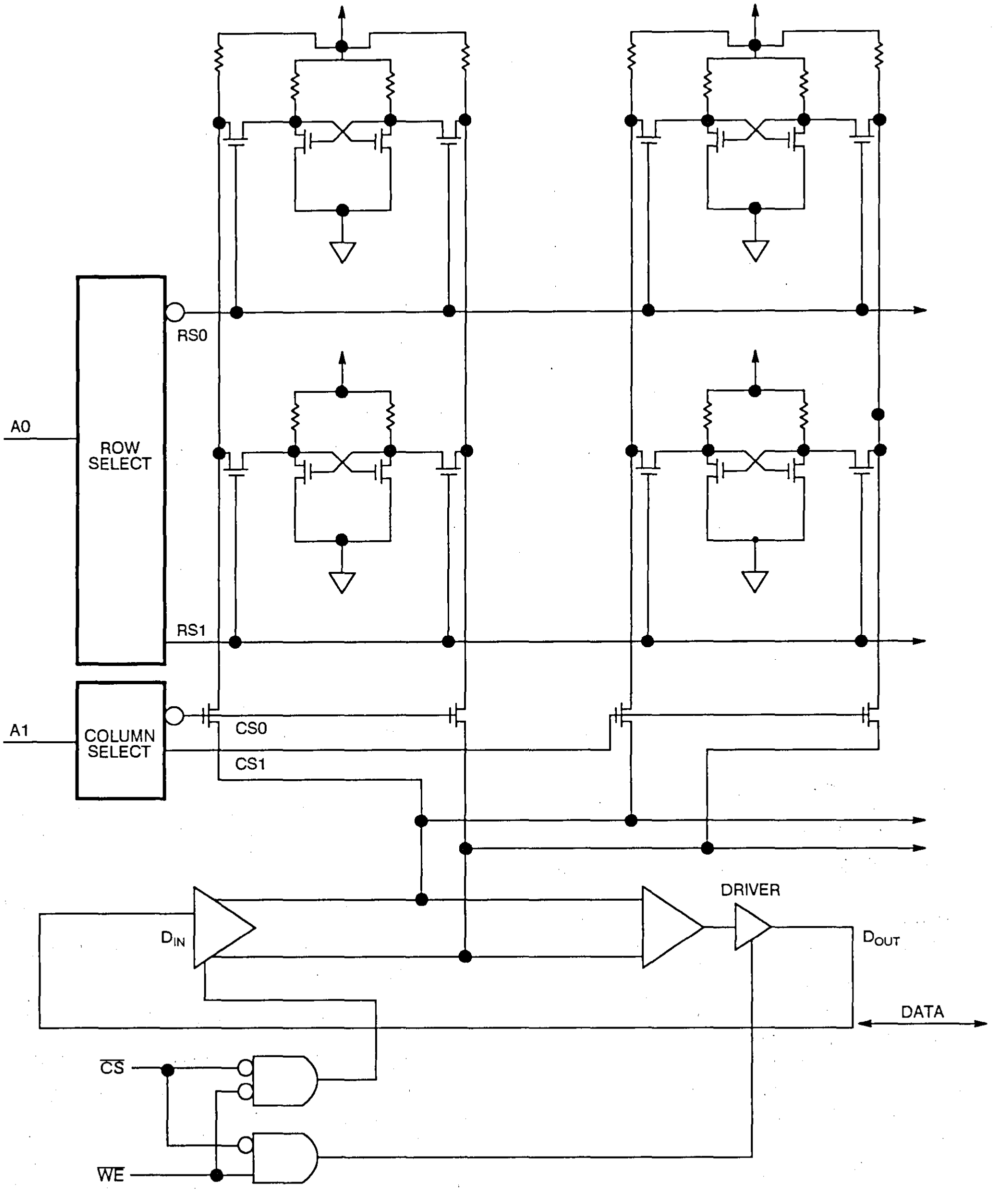

Figure 5. A 2 x 2 Common I/O ARRAY

If the user decides to execute a write on a common I/O part, there will be one extra step to take compared to our previous set of steps illustrated for a separate I/O part. This extra step is just turning off the output driver, enabling the input differential amplifier and finally executing a write into the array.

A REAL COMMON I/O PART

Let us now take a look at another actual part from Integrated Device Technology. Figure 6 shows the functional block diagram of a 4K x 4-bit memory device, the IDT6168.

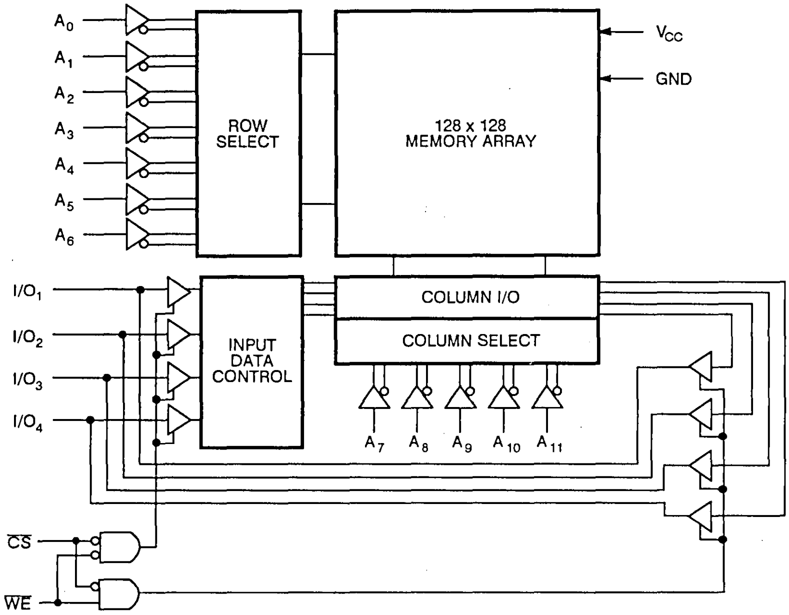

Figure 6. Functional Block Diagram of 4K x 4-Bit Common I/O Memory

In order to understand the different timing parameters involved in the read/write operation of the memory elements in general, let us examine Figure 6 in more detail.

WRITING METHODS: WE vs. CS CONTROLLED WRITE

Writing is achieved using two different techniques. Similar to the previous section, a write can be achieved by either strobing the chip select or strobing the write pulse. Here is the sequence to follow if the WE (Write Pulse) controlled write is used:

- Bring the address bits to the IC address pins
- Select the IC by enabling Chip Select
- Wait for the address pins to settle
- Start the Write Pulse: This will turn off the output drivers and enable the input differential amplifier
- Bring the data bits to the IC data pins
- Turn off the write pulse
- Keep the data bits stable for a while after the Write pulse: This is required hold time for the cells to settle

The other way of writing is the Chip Select controlled write. The steps that follow are very similar to the steps taken for the separate I/O part. Here is the sequence:

- Bring the address bits to the IC address pins
- Wait for the address pins to settle
- Keep the Write Enable pin low: This will keep the output drivers off and allows the input differential amplifier to get enabled as soon as the CS goes low
- Bring the data bits to the IC data pins
- Strobe the Chip Select: This will enable the input differential amplifier for writing
- Bring the Chip signal high again: This will disable the input differential amplifier
- Keep the data bus stable for a while after the Chip Select pulse goes high: This is the required hold time for the cells to settle

READING FROM THE COMMON I/O ARRAY

Again, reading the common I/O part is not very different from reading the separate I/O part. If the user decides to continuously read an entire block sequentially, the Chip Select signal should be kept low and the Write Enable signal high. In this way, the output drivers are enabled and the concerned memory cells are selected. The steps to follow are described below:

- Bring the address bits to the pins of the IC
- Select the IC by bringing the CS signal low
- Turn the outputs on by bringing the WE signal high: This step and the two above can be executed together

- Wait for a while for:

  The concerned cells to be selected

  The output drivers to be enabled (t_{LZ})

  The data bits to be valid (t_{ACS})
- Read the Data Out of the IC after the above wait

Data will be available after T_{AA} (address access time) from the last time the address changed or after t_{ACS} (chip select access time) from the time $\overline{CS}$ became active, whichever is longer.

WHAT DID WE TALK ABOUT SO FAR?

We have talked about latches and how they work. We have described the structure of an array and then shown that there are two different sorts of array. We have shown that the difference is not a big one (Separate I/O vs. Common I/O) and that the parts are not only similar in their base structure, but also similar in the way they work.

Then the description of the necessary steps to take for a write or a read operation was given. In order to finalize the idea about memory parts, and before going into further detail about the timing parameters and what they mean, Figure 7 shows a general block diagram representing a memory part.

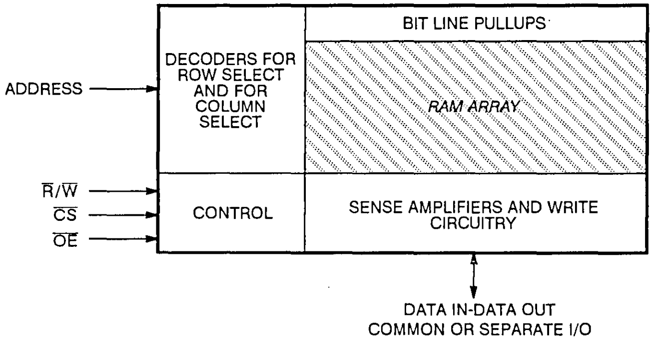

Figure 7. Block Diagram for a Static RAM Memory Device

TIMING

At this point let us divide the timing parameters into two different categories: those involved with common I/O and those involved with separate I/O. To have a better understanding of these parameters, let us take a look at various timing diagrams taken from actual devices that Integrated Device Technology produces.

WRITING TO SEPARATE I/O SRAM

To start, let us take a look at the 16K x 1-bit part (separate I/O), the IDT6167. As the reader remembers, there are two ways of accomplishing a write. Figure 8 illustrates the Write Enabled controlled write for the mentioned memory IC.

WRITE ENABLED CONTROLLED WRITE

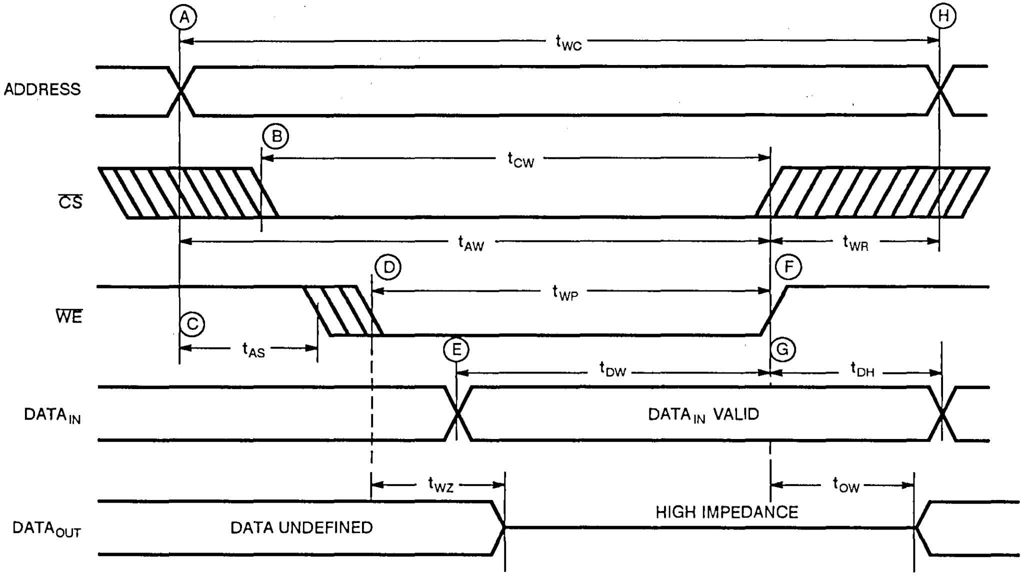

Figure 8. Timing Diagram for WE Controlled Write, IDT6167

Figure 8 shows the timing for Write Enabled controlled write and the steps described below relate to that Figure:

- Bring the address bits at the IC address pins. (At this point the user should keep the address bits stable throughout the write operation.) The Write Cycle time is t_{WC} during which the address must remain constant.
- Select the chip. At this point the chip is selected and t_{CW} is the chip select to end of write ($\overline{WE}$ signal) time. This is the minimum amount of time that the IC has to remain in a selected mode.
- Wait a while for the address pins to settle. The address set-up time is t_{AS}. During that particular time the user is giving the memory some time for the concerned cells to be selected with the row and column select logic.
- Strobe the Write Enable pin. This will enable the write differential amplifiers (since CS is active already). The write pulse width is t_{WP}. This is the minimum amount of time necessary for the $\overline{WE}$ signal to be active in order to give enough time for the cells to change state.
- Bring the data bits to the IC data pins. The data bits should be stable by the cells for at least t_{DW}, which is the data valid to end of write time. The set-up time is t_{DW} for the latches of the IC.
- Terminate the strobe. At this point, the $\overline{WE}$ signal is deactivated and the strobing is done.
- Keep the data bits stable for a while. This corresponds to the hold time for the latches of the IC, t_{DH}. By holding the data bits stable during this time, the user is giving the cells a chance to settle at the correct logic state while the write switches turn off.
- This is the end of the cycle. At this point, the user can make an address transition for the next operation **but remember, $\overline{CS}$ or $\overline{WE}$ must be high during address transition.** If the $\overline{CS}$ or the $\overline{WE}$ signals are not held high during an address transition, the address decoders can glitch when addresses change, and therefore, cause random cells to be written:

Figure 9 shows the timing for chip select controlled write and the steps described below relate to this Figure:

- Keep the Write Enable low (enabled). During a Chip Select controlled write, the Write Enable signal is low during the the Chip Select pulse. It should be active for at least the minimum. The write pulse width is t_{WP}.
- Bring the Address bits at the IC address pins.The user must keep the address bits stable throughout the write operation. The Write Cycle time is t_{WC} during which the address must remain constant.
- Wait for the address pins to settle. The address set-up time is t_{AS}. During that time, the user is giving the memory time for the cells to be selected by the row and column select logic.
- Strobe the Chip Select. This will turn on the bit and row select switches and will bring the cells to a situation where they are ready to be written into. t_{CW} is the chip select to end of write time. This is the minimum width of the CS strobe.
- Bring the data bits at the IC data pins. The Data bits should be stable at the cells for at least t_{DW}, which is the data valid to end of write time. The set-up time t_{DW} is for the latches of the IC.
- Terminate the strobe. At this point the $\overline{CS}$ signal is deactivated and the strobing is done.
- Keep the data bits stable for a while. This corresponds to the Hold time for the latches of the IC. t_{DH} is the data hold time. By holding the data bits stable during this time, the user is giving the cells a chance to settle at the correct logic state while the select lines turn off.
- This the end of the cycle. At this point the user can make an address transition for the next operation **but remember, $\overline{CS}$ or $\overline{WE}$ must be high during address transition.** If the $\overline{CS}$ or the $\overline{WE}$ signals are not held high during an address transition, the address decoders can glitch when addresses change and, therefore, cause random cells to be written.

CHIP SELECT CONTROLLED WRITE

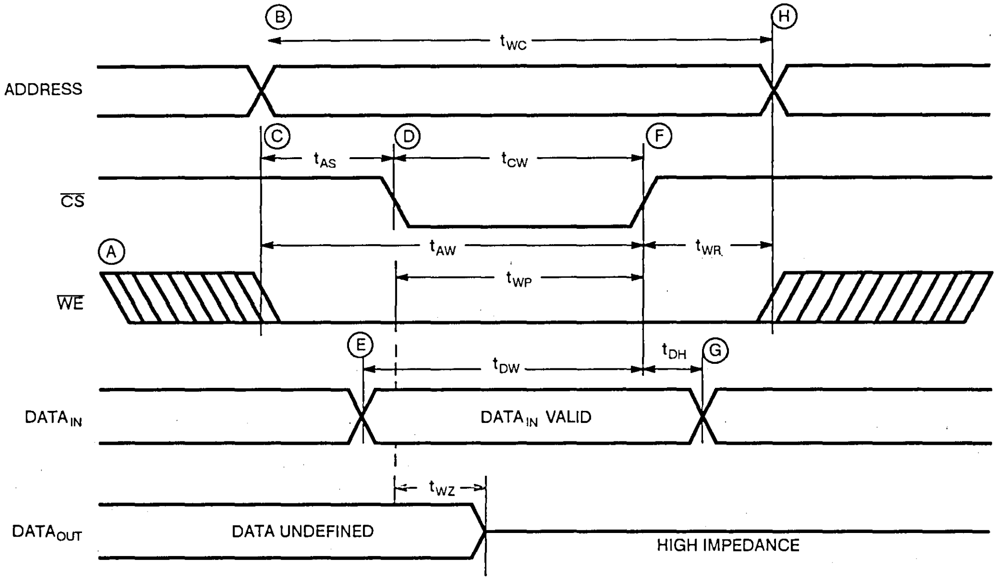

Figure 9. Timing Diagram for CE Controlled Write, IDT6167

TIMING FOR CONTINUOUS READ

Let us now take a look at the timing for a read cycle. Let us assume that the user wants to constantly read the IC. The $\overline{WE}$ signal is high and the $\overline{CS}$ signal is low, continuously. The timing that will apply is shown in Figure 10.

TIMING WAVEFORM OF READ CYCLE NO. 1

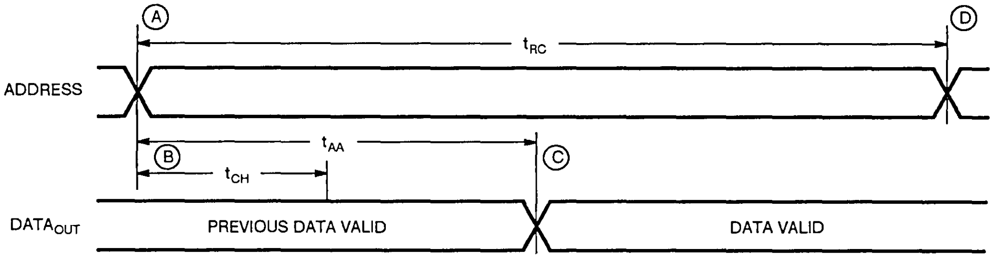

Figure 10. Timing Waveform for Read Cycle No.1

During this read cycle, the Write Enable ($\overline{WE}$) is high (therefore disabled) and the Chip Select line is low ($\overline{CS}$, therefore enabled). The output drivers are turned on while the chip is selected, putting the IC in a constant read mode. The amount of time that the previous data will still be valid after an address transition has occurred is t_{OH}. Finally, after T_{AA} has passed since the address transition, the valid data bits are available. Since $T_{AA}-t_{OH}$ is changing, data from the IC is not valid during this time.

Let us go through Figure 10 step by step:

- Bring the address bits to the IC address pins. The read cycle time parameter during which the address must remain constant is t_{RC} .
- At this point the previous data is still valid on the bus. This data is going to stay valid for t_{OH}, which is the output hold from address change time.
- At this point the valid data will appear at the pins. T_{AA} is the IC access time and is the amount of time that has to pass since the address transition for the valid data to appear at the pins.

- At this point the IC is ready for a new address.

TIMING FOR CS CONTROLLED READ

Figure 11 shows the timing of a chip select continuous read operation.

TIMING WAVEFORM OF READ CYCLE NO. 2

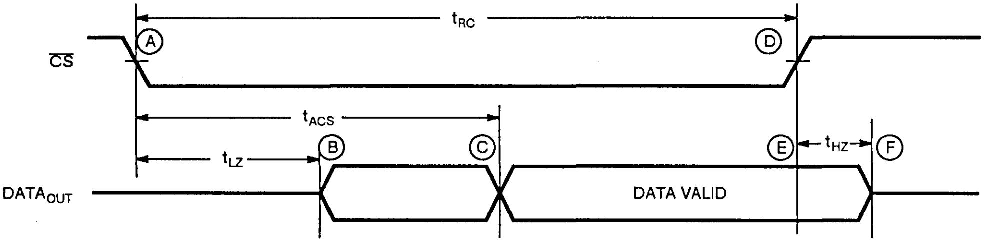

Figure 11. Timing Waveform for Read Cycle No.2

In Figure 11, it is assumed that the $\overline{WE}$ signal is high and that the address transition has occurred and the address is valid prior to the $\overline{CS}$ transition to a low state:

- The $\overline{CS}$ signal makes a high-to-low transition, therefore becoming active. t_{RC} is the read cycle time and represents the amount of time that this signal has to stay active.
- The Chip Select to Output in low Impedance state is t_{LZ}. This shows that t_{LZ} time after the $\overline{CS}$ high-to-low transition the output drivers will be on.
- The Chip Select access time is t_{ACS}. This shows the amount of wait necessary after the high-to-low transition of the $\overline{CS}$ signal before the valid data will appear at the output pins.
- Terminate the strobe. This will start turning off the output drivers. At this point the $\overline{CS}$ signal will become inactive.
- From this point on, the output drivers are turning off and the valid data will be present for only t_{HZ} time after this point. t_{HZ} is the Chip Deselect to output in high impedance time parameter.

WRITING TO COMMON I/O SRAM

Let us take a look at the 4K x 4-bit part (Common I/O), the IDT6168. Figure 12 illustrates the Write Enabled controlled write for the common I/O RAM.

WRITE CYCLE NO. 1

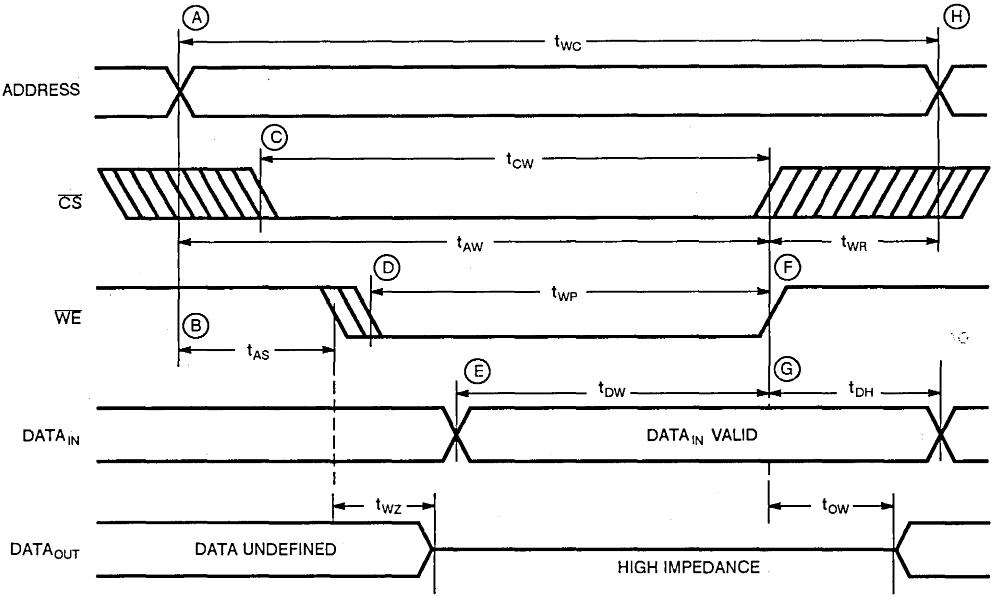

Figure 12. Timing Diagram for WE Controlled Write, IDT6168

TIMING FOR WE CONTROLLED WRITE

The steps described below relate to Figure 12:

- Bring the address bits to the IC address pins. At this point, the user must keep the address bits stable throughout the write operation. The Write Cycle time during which the address must remain constant is t_{WC}.
- Wait for the address pins to settle. The address set-up time is t_{AS}. During that time, the user is giving the memory time for the cells to be selected with the row and column select logic.
- Select the chip by enabling Chip Select. At this point the chip is selected and T_{CW} is the chip select to end of write ($\overline{WE}$ signal) time. This is the minimum amount of time the IC has to remain selected.
- Strobe the Write Enable pin. This will enable the write differential amplifiers (since CS is active already). The minimum write pulse width is t_{WP}. This is part of the amount of time necessary for the $\overline{WE}$ signal to be active in order to give enough time to the cells to change state. On the data out graph in Figure 12 (bottom), the user should notice that at this time, the output drivers start to turn off and, in t_{WZ} time, they will be completely in the high impedance state.
- Bring the data bits to the IC data pins. The data bits should be "seen" by the cells for at least t_{DW}, which is the data valid to end of write time. The Set-up time is t_{DW} for the latches of the IC.
- Terminate the strobe. At this point the $\overline{WE}$ signal is deactivated and the strobing is done.
- Keep the data bits stable for a while. This corresponds to the Hold time for the latches of the IC. The data hold time is t_{DH}. By holding the data bits stable during this time, the user is giving the cells a chance to settle at the correct logic state.
- This is the end of the cycle. At this point, the user can make an address transition for the next operation. **Remember, $\overline{CS}$ or $\overline{WE}$ must be high during address transition.** By keeping them inactive, the user is preventing the row and column select logic to expose the cells to the address bus while it is in transition.

WRITE CYCLE NO. 2

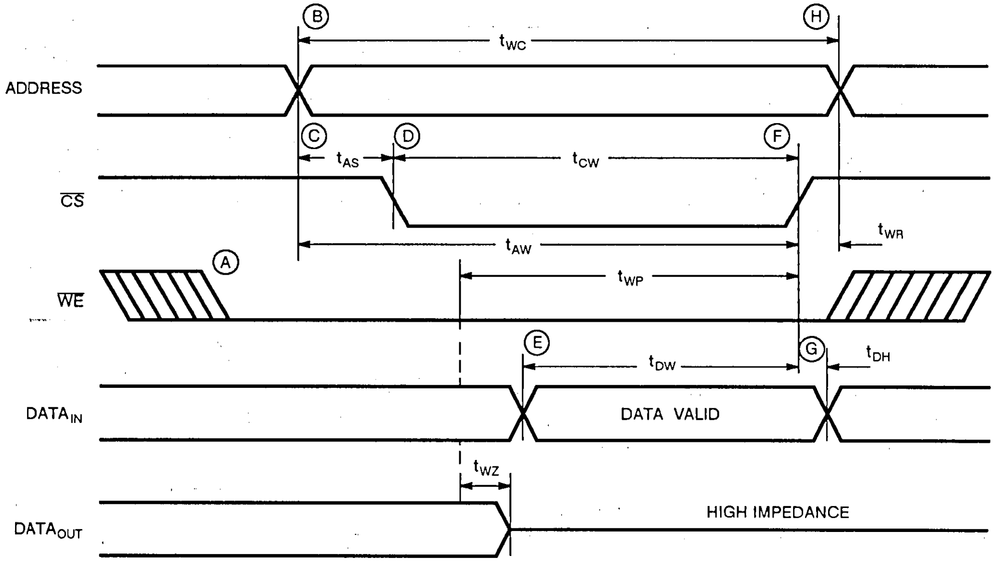

Figure 13. Timing Diagram for CS Controlled Write, IDT6168

TIMING FOR CS CONTROLLED WRITE

The steps described below refer to Figure 13.

- Keep the Write Enable low (enabled). During a Chip Select controlled write, the Write Enable signal is supposed to be active for at least the write pulse width amount of time. The time that the WE signal is enabled should correspond to the time where the IC is selected for at least the width of the write pulse. From the moment that $\overline{WE}$ becomes active, t_{WZ} is the amount of time after which the output drivers are turned off and reach high impedance state.
- Bring the address bits to the IC address pins. The user should keep the address bits stable throughout the write operation. The Write Cycle time is t_{WC} during which the address must remain constant.
- Wait for the address pins to settle. The address set-up time is t_{AS}. During that time, the user is giving the memory time for the cells to be selected with the row and column select logic.
- Strobe the Chip Select. This will turn on the bit and row select switches and bring the cells to a situation where they are ready to be written into. The chip select to end of write time is t_{CW}. This is the minimum width of the CS strobe.
- Bring the data bits to the IC data pins. The Data bits should be "seen" by the cells for at least t_{DW}, which is the data valid to end of write time. The Set-up time is t_{DW} for the latches of the IC.
- Terminate the strobe. At this point, the $\overline{CS}$ signal is deactivated and the strobing is done.
- Keep the data bits stable for a while. This corresponds to the Hold time for the latches of the IC. The data hold time is t_{DH}. By holding the data bits stable during this time, the user is giving the cells a chance to settle at the correct logic state.
- This the end of the cycle. At this point the user can make an address transition for the next operation. **Remember, $\overline{CS}$ or $\overline{WE}$ must be high during address transition.** By keeping them inactive, the user is preventing the row and column select logic to expose the cells to the address bus while it is in transition.

SOME POINTS TO NOTICE IN COMMON I/O SRAMs

1. $\overline{WE}$ vs. $\overline{CS}$ Controlled Write on Common I/O SRAMs

One more detail about common I/O is that it is possible to improve the speed of operation of the system by intelligently choosing what signal will be strobed during a write:

if the user decides to strobe the WE signal, he would have to wait for at least:

– $T_{WZ} + T_{DW}$ (Write Enable to output in high Z+ data valid to end of write)

if the user decides to strobe the CS signal, he would have to wait only for:

– T_{WP} (Write Pulse width)

– And generally -------->T_{WZ} + T_{DW} ¿ T_{WP}

2. WE Controlled Write

An additional timing requirement is to wait for the drivers to turn off at the beginning of the write.

3. CS Controlled Write

In a Chip Select controlled write, the designer does not have to wait for the drivers to turn off.

TIMING FOR CONTINUOUS READ

Let us now take a look at the read cycles of a common I/O device. Again, they are not really different from the separate I/O case. Figure 14 shows the read cycle for continuous enabled write.

In this cycle, it is assumed that the IC is continuously selected and that the addresses are changing at a certain rate. The data is being read after an appropriate wait after each address transition.

TIMING WAVEFORM OF READ CYCLE NO. 1

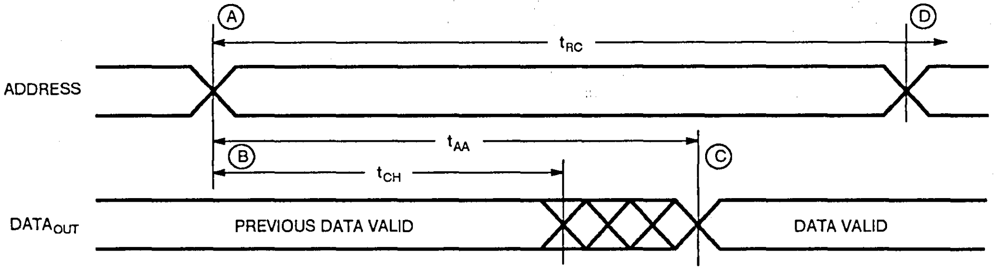

Figure 14. Timing Waveform for Read Cycle No. 1

In a continuously enabled read cycle, $\overline{CS}$ is active, therefore the IC is selected and $\overline{WE}$ signal is high—putting the IC in the read "mode" by turning off the output drivers. Let us examine Figure 14 step by step:

- Bring the address bits to the IC address pins. The read cycle time is t_{RC} parameter during which the address remains constant.
- At this point the previous data is still valid on the bus. This data is going to stay valid for t_{OH}, which is the output hold from address change time.
- At this point the valid data will appear at the pins. T_{AA} is the IC access time and is the amount of time that has to pass since the address transition for the valid data to appear at the pins.
- At this point the IC is ready for a new address.

TIMING FOR CS CONTROLLED READ

Let us now take a look at Figure 15, which shows the timing of a single read operation.

TIMING WAVEFORM OF READ CYCLE NO. 2

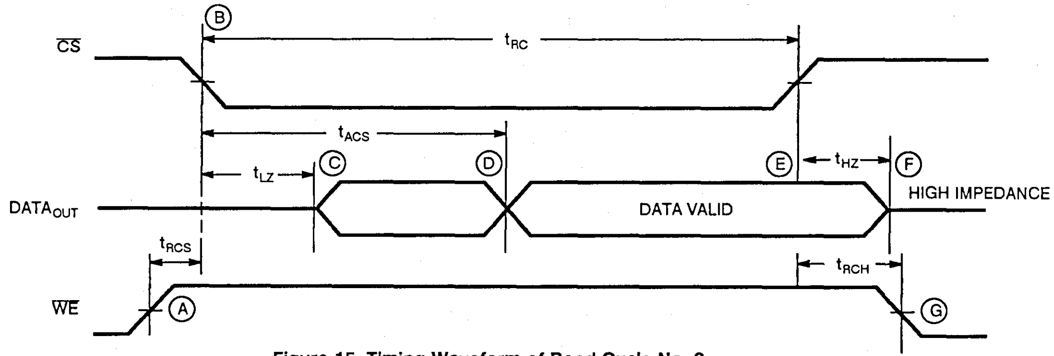

Figure 15. Timing Waveform of Read Cycle No. 2

- $\overline{WE}$ goes high, putting the IC in a read "mode". The read command set-up time is t_{RCS}. At this point the IC is ready to turn on the output drivers as soon as the $\overline{CS}$ (Chip Select) signal becomes active.
- The $\overline{CS}$ signal makes a high-to-low transition, therefore becoming active. The read cycle time is t_{RC} and represents the amount of time that this signal has to stay active.
- The Chip Select to Output in low impedance state is t_{LZ}. This shows that t_{LZ} time after the $\overline{CS}$ high-to-low transition, the output drivers will be on.
- The Chip Select access time is t_{ACS}. This shows the amount of wait necessary after the high-to-low transition of the $\overline{CS}$ signal before the valid data will appear at the output pins.

- Terminate the strobe. This will start turning off the output drivers. At this point the $\overline{CS}$ signal will become inactive. The valid data will be present for only t_{HZ} time, the Chip Deselect to Output in High Impedance time is t_{HZ} parameter.
- From this point on, the output drivers are turned off.

CONCLUSION

To get a better understanding of the timing for read or write operations, this application note went through an overview covering a range of subjects.

To start, a RAM cell and its operation was presented. Then, the way of achieving an array of RAM by interconnecting the different RAM cells was shown.

There are two different sorts of RAMs: Separate I/O and Common I/O. The application note went through a complete explanation of read and write operations for these different types with concrete examples.

There are two different ways of writing into the memory: Chip Select controlled Write and Write Enabled controlled write.

While writing to a common I/O device, it is generally faster to use the Chip Select controlled write.

The use of all RAMs is very similar and generally, if the guidelines of this paper are followed, the operations will be accomplished successfully.

Integrated Device Technology, Inc.

CACHE DESIGN CONSIDERATIONS USING THE IDT 79R3000

APPLICATION NOTE AN-27

By Satyanarayana Simha

INTRODUCTION

The reduced instruction set computer (RISC), the IDT79R3000, has allowed for simplicity in hardware and synergy between architecture and compilers. To further increase the throughput of a computer system, direct-mapped cache memory is implemented on systems using the R3000. The availability of a wide variety of high-speed static RAMs from IDT gives the designer the flexibility of selecting the proper part for his application. It is necessary, however, to know the critical timing parameters governing the design of a cache subsystem. This article is divided into three parts. The first part shows a general cache system with a description of the clock inputs. The second section details the equations used to calculate the critical parameters. It is followed by an example of an IDT7198 static RAM used as a cache RAM for the R3000.

CACHE DESIGN

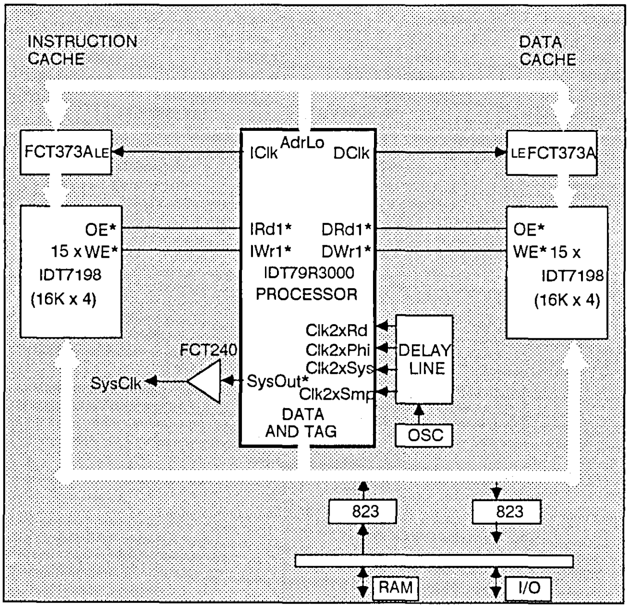

Figure 1. 64KB Instruction/Data Cache Configuration

A simplistic block diagram implementation of a 64KB separate instruction cache and data cache is shown in Figure 1. The design of a cache subsystem such as the one above depends on the four input clocks to the R3000 processor. These clock inputs are twice the frequency of the output clock i.e., SysOut. By adjusting the timings of these clocks, the designer can accommodate a wide variety of static RAMs by properly considering specific parameters such as set-up and hold times. The clocks themselves can be adjusted using tap settings on a delay line or by using delay logic. The clock inputs are described below.

1) Clk2xSyS: Determines the position of SysOut with respect to the data, tag, and address buses. It is positioned so that devices in the cache/bus interface clocked by SysOut meet the set-up and hold time requirements.
2) Clk2xSmp: Is used by the R3000 to capture external data onto data bus and control inputs.
3) Clk2xRd: Is used to delay the enable of data bus drivers.
4) Clk2xPhi: Is used to determine all R3000 outputs i.e., data, address, and tag buses.

Figure 2 shows the timing relationships between the four clocks. All the timing equations for cache design depend on the phase relationship between these clocks. T_{smp} is the Clk2xSmp to Clk2xPhi delay, T_{rd} is the Clk2xRd to Clk2xPhi delay, and T_{sys} is the Clk2xSys to Clk2xPhi delay.

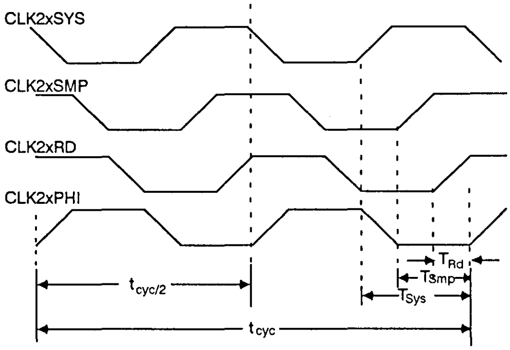

Figure 2. Timing Relationships Between the Four 2x Clock Inputs

In the cache implementation scheme, instruction references begin their reference during phase 2 and transfer data during the following phase 1. Data references begin during phase 1 and transfer data during phase 2. Thus, data and instruction references can take place in different phases of the same clock cycle. See Figures 3a and 3b. This is an important factor to consider in order to prevent contention between instruction and data caches.

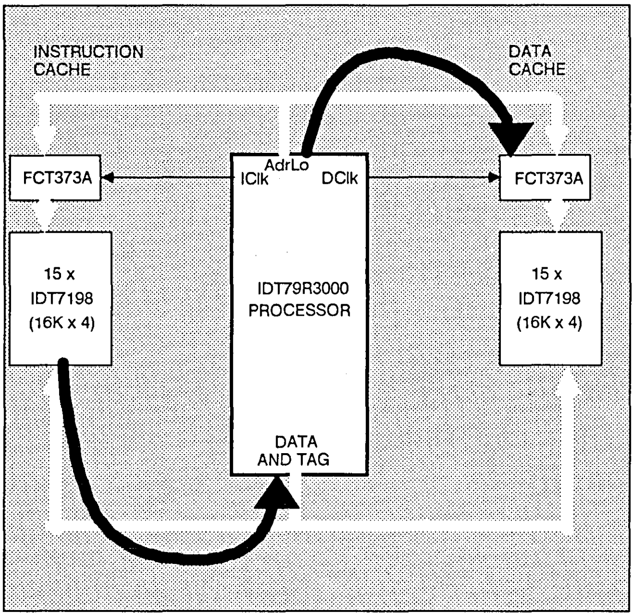

Figure 3a. Data and Instruction Caches During Phase 1

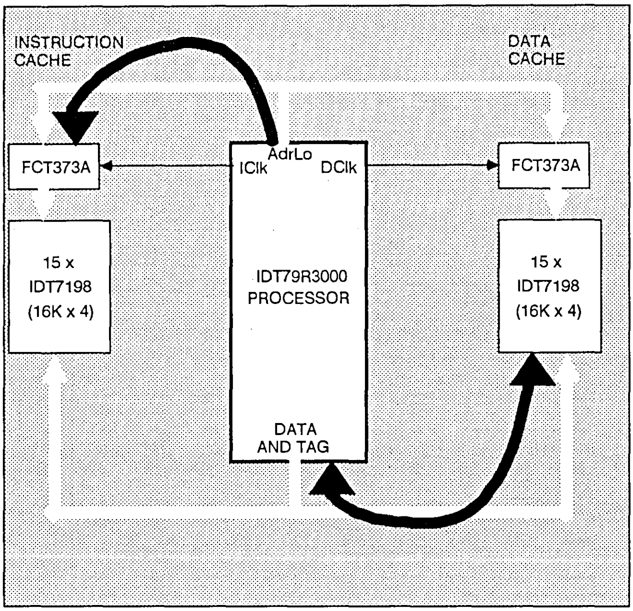

Figure 3b. Data and Instruction Caches During Phase 2

Specific factors such as access time, set-up time, hold time, enable and disable times, and the deration factor are key in choosing the proper static RAM and in setting the phase delays in the clocks. The next section discusses the timing equations needed for selecting a static RAM for cache design.

Equations Governing the Critical Parameters in RAM Selection:

Figure 4 shows the timing of the relevant signals for a 25MHz (40ns) R3000. The numbers represent the equations that are critical in determining the selection of the static RAMs. The timing is given for the worst case condition i.e., a STORE followed by a LOAD. An explanation of the equations is given below.

Internal Sample to Phi: This timing parameter requirement guarantees that the processor internal sample to Phi is met.

$$t_{smp} \geq 5ns \qquad \text{-----------------------} \qquad (1)$$

Address Access to Data Sample: This timing parameter requirement guarantees that the cache RAMs have sufficient access time. This calculation assumes that the address delay through the FCT373 is limited by its propagation delay.

$$\mathbf{RAM}^{d}_{\mathbf{AA}} \leq t_{cyc} - t_{smp} - AdrLo^{d*} - 373_{PD} - t_{OS} \text{---} \ (2)$$

Cache Enable to Sample: This timing parameter requirement guarantees that the cache RAMs are enabled soon enough to meet the processor's input set-up specification.

$$\mathbf{RAM}_{\mathbf{OE}}{}^{d} \leq T_{cyc/2} - t_{smp\text{-}rd} - Rd^{d} - t_{OS} \text{-------} \qquad (3)$$

Minimum Read Pulse Width: This timing parameter requirement guarantees that the read pulse generated by the processor is at least as long as the cache RAM output enable time.

$$\mathbf{RAM}^{d}_{\mathbf{OE}} \leq t_{cyc/2} - t_{sys\text{-}rd} \qquad \text{---------------} \qquad (4)$$

Read Write I-Cache Data Bus Contention: This timing parameter requirement guarantees that no contention will occur between the instruction cache and the processor on a store.

$$\mathbf{RAM}_{\mathbf{HZ}} \leq t_{sys} - Rd^{d} + D_{en} \text{-----} \qquad (5)$$

Processor Data Set-up to End of Write: This timing parameter requirement guarantees that the cache RAMs have adequate data set-up time when being written into by the processor.

$$\mathbf{RAM}_{\mathbf{SD}} \leq t_{cyc/2} - t_{smp} - DVal^{d} + Wr^{d} \text{-----} \qquad (6)$$

Data Hold from End of Write: This timing parameter requirement guarantees that the data hold from end of write specification of the cache RAMs is met when either the processor or the read buffer is writing to the RAMs.

$$\mathbf{RAM}_{\mathbf{HD}} - \mathbf{RAM}_{\mathbf{LZ}} \qquad \leq t_{smp\text{-}rd} \qquad \text{--------} \qquad (7)$$

Data Set-Up to SysClk: This timing parameter requirement guarantees that the set-up time into an external register is met on a processor store.

$$\mathbf{SetUp}_{\mathbf{sys}} \leq t_{cyc/2} - t_{sys} - (DVal^{d} + - Sys^{d} - 240_{PD}) \text{--} \ (8)$$

Data Hold from SysClk: This guarantees that the hold time specification of an external register is met on a processor store. The data holds on the bus until a subsequent read drives new data.

$$\mathbf{Hold}_{\mathbf{sys}} \leq t_{sys\text{-}rd} - Sys^{d} - 240_{PD} + RAM_{LZ} + Rd^{d} - \ (9)$$

Equations 1 to 9 are sufficient for the purpose of selecting the proper RAMs for use as cache memory. To illustrate the point further, an IDT RAM device, the IDT7198 (16K x 4), is chosen as an example.

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*d: Deration due to additional load. 1ns per 25pF.

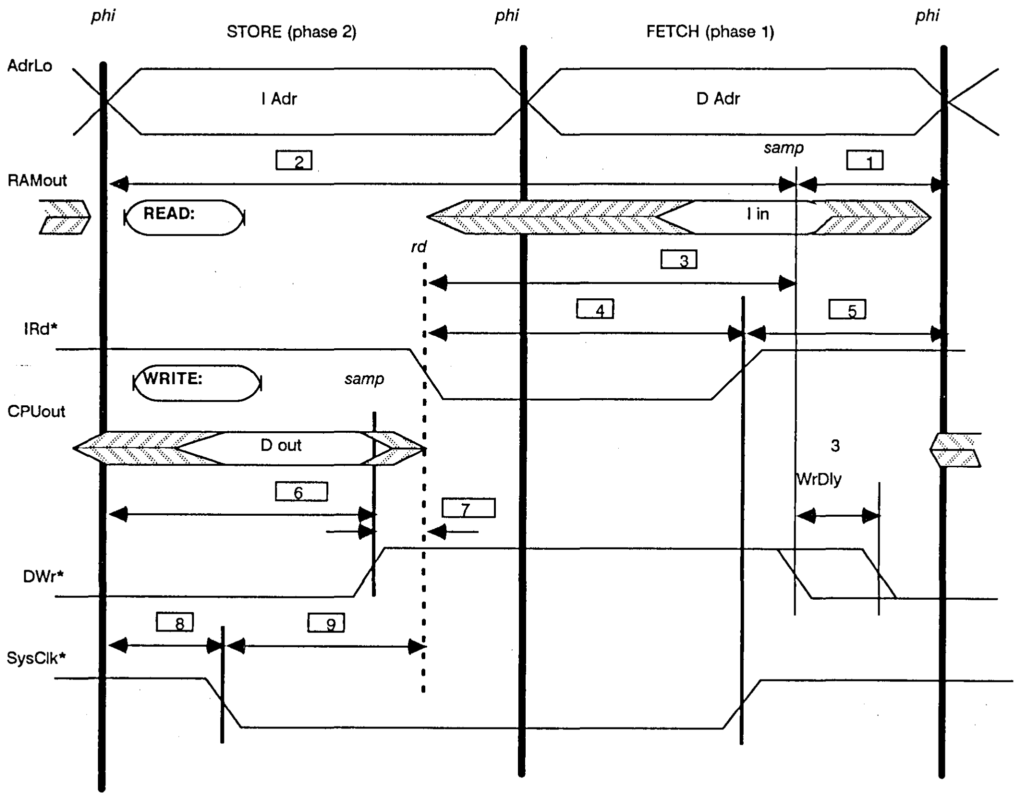

Figure 4. IDTR3000 40ns (25MHz) Cycle Timing

CALCULATION OF TIMING PARAMETERS

An example of a cache subsystem design using an IDT7198 i.e., a 16 K x 4 static RAM follows. All the numbers used in the calculations have been taken from the IDT Data Book[1] and the R3000 Interface Manual. The numbers are presented in Figure 6. The deration factor has been taken into account for DIPs. Surface mount would decrease the deration factor.

The following factors have been taken into account for calculating the deration factor[2].

1) The SSI logic and cache RAM propagation delays are derated by 1ns per 25pF of additional load.
2) Cache RAM input capacitance is 5pF.
3) Cache RAM output capacitance is 7pF.
4) Trace capacitance is estimated at 2pF per inch.
5) Data and trace tag buses are 6 inches.
6) Address buses are 2 x 5 inches.
7) SysOut loading is 50pF.
8) Test value of 30pF to be subtracted.

Deration Calculations:

Address Capacitance: 12 x 2pF = 24pF; (factors 4,5, and 6) 5 Devices = 5 x 10pF = 50pF; Test value = -30pF; Total capacitance = 45pF; At 1ns per 25pF, total deration of address bus = 2ns.

Data Bus Deration: Is approximately the same i.e., 2ns. Read control capacitance for IDT7198 will be about 10 inches of trace and 8 devices at 7pF each. Therefore, Read control deration = (76-30)pF/25pF/ns = 2ns.

In Figure 5, the circled numbers are the equations previously described. The number in parentheses is the allowable worst case timing. The adjacent number is the total time taken using the IDT7198. The numbers for the IDT7198 with the R3000 running at different frequencies and the FCT373A are shown in Table 1 and Table 2 respectively.

The first value for each parameter in Table 1 shows the maximum allowable worst case rating and the second value shows the timing using the IDT7198 RAM.

Parameter	Load (pF)	Symbol	R3000 Clock Frequencies					
			16MHz Min. (ns)	16MHz Max. (ns)	20MHz Min. (ns)	20MHz Max. (ns)	25MHz Min. (ns)	25MHz Max. (ns)
Address to Data Valid	30	t_{AA}		31		25		19
				29		25		19
Output enable to Data Valid	30	t_{DOE}		17		13		10
				15		13		10
Output Disable time		t_{HZ}		14		12	2	8
				12		10		7
Output Enable Time		t_{LZ}	2		2		2	
			5		5		5	
Address SetUp to End of Write		t_{AW}	43		36		27	
			20		20		13	
Data SetUp to End of Write		t_{DS}	14		13		11	
			13		13		8	
Write Pulse Width		t_{PWE}	55		47		37	
			20		20		13	
Data Hold from End of Write		t_{HD}	0		0		0	
			0		0		0	
Address Hold from End of Write		t_{HA}	0		0		0	
			0		0		0	

Table 1. Cache RAM Parameters. RAM Specifications vs. IDT7198 Specifications.

Parameter	Load (Units)	Symbol	Min. (ns)	Max. (ns)
FCT373A Propagation Delay	50	$t_{373\ PD}$		5.2
FCT373A Latch Enable Delay	50	$t_{373\ LE}$	2	8.5
FCT373A Latch Enable Hold	50	$t_{373\ Hld}$	1.8	
FCT240A Prop Delay	50	$t_{240\ PD}$	1.5	4.8

Table 2. Parameters for Latches and Buffers

Figure 6 shows a block diagram of tap settings on a delay line for the four clock input signals. By varying the phase delay between these signals, the designer can select the proper static RAMs for cache memories and the operating frequency of the R3000. Table 3 shows suggested tap settings on the delay line for the R3000 running at different frequencies.

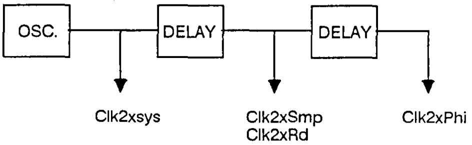

Figure 6. Tap Settings for the Clock Inputs

Parameter	16.67MHz	20MHz	25MHz
Clk2xSys	0	0	0
Clk2xRd	6	6	6
Clk2xSmp	6	6	6
Clk2xPhi	16	14	12

Table 3. Delay Line Setting Summarization

The designer can use a DDU-7F-20* chip for the delay line. The clock is the input to the device and the outputs at various points can be chosen with the appropriate phase delays.

CONCLUSION

The IDT R3000 RISC processor allows an efficient cache system to be implemented with standard architecture static RAMs. To design a cache subsystem, it is essential to know only the critical equations mentioned above and their relation to the four input clocks. The tap settings provide further control of the cache subsystem design for different operating frequencies of the R3000.

REFERENCES

1. IDT Data Book, pp 4-74 -- 4-83, pp 10-72 -- 10-75.
2. MIPS R3000 Processor Interface Manual, pp 105.

*d: deration due to additional load. 1 ns per 25 pF.

*Available from Data Delay Devices (201) 772-1106

Integrated Device Technology, Inc.

THE COMPLETE HIGH PERFORMANCE CACHE SYSTEM FOR THE 80386 MICROPROCESSOR

APPLICATION NOTE
AN-30

by SRAM Applications

INTRODUCTION

The design of microprocessor systems, today, requires an extensive knowledge of the principles of cache controller and cache memory design—for it is the cache that enables the microprocessor to achieve its maximum throughput. For example, the Intel 25MHz 80386 (using main memory DRAMs with a cycle time of 250ns), without a cache, is rated at 2 MIPs (peak). However, with a well designed cache, the system performance can reach 12.5 MIPs (peak). Similarly, for the Motorola 68030, the performance can be increased from 2 MIPs to 10 MIPs (again with 250ns DRAMs as the main memory element).

Besides increasing the throughput of a microprocessor system, the inclusion of a cache decreases the system bus traffic, making it an ideal element for use in the design of multiprocessing and multi-master based systems. A well designed cache for coherent multiprocessing and multi-master systems.

Central to a cache design, is the coherency architecture employed. This application note discusses the design of a unique cache controller which uses two cache tags to achieve coherency. This dual cache tag design for the 80386 microprocessor offers greater speed than the more common time multiplexed cache tag design in addition to simplifying the system bus interface and timing requirements.

CACHE DEFINITION AND OPERATION

A cache may be defined as a high speed memory element that serves as a high speed memory buffer between slower main memory and the microprocessor. The design of the cache is such that it has an effective cycle time that is less than the cycle time of main memory. This, of course, is because the design of the cache dictates that the data or code needed most often is usually in the cache memory.

The cache memory can not be too large in size because of cost and board space considerations. The main memory will therefore be divided into pages equal in size to the cache memory size. The size of a page will depend on the total size of the cache and the degree of associativity of the cache implementation.

The general operation of a cache based system can be understood by examining its interaction with the microprocessor and main memory during program execution. When a microprocessor issues a read instruction, the microprocessor's address's page field is compared against the page address stored in the cache tag. If the cache tag page address matches the microprocessor address's page field, a hit occurs, and the microprocessor reads the associated data from the data cache SRAM. On the other hand, if the microprocessor page address is not in the cache tag a cache miss occurs. In the latter case, the microprocessor will retrieve the data from main memory and update the cache memory and cache tag with the required main memory address and data i.e. a cache read miss cycle.

CACHE ARCHITECTURE OVERVIEW

A cache system consists of a cache memory which may be divided into two parts; the dictionary or cache tag (a cache tag SRAM) and the cache memory (a data SRAM). The cache tag stores the main memory page addresses of the data that is stored in the cache memory. Besides the cache tag and cache memory, a complete cache system for a microprocessor incorporates; a cache controller to instigate and respond to local and system bus states; system and local bus control logic to interface to external system bus masters and the local microprocessor; coherency logic to assure system coherency in multi-master based systems. Faster caches include a write buffer to allow for zero wait state posted writes.

CACHE TIMING PARAMETERS

When designing a cache system using cache tag and data cache SRAMs, you have to consider the cycle time of the microprocessor used, the match time of the cache tag and the access time of the data cache SRAM. For the Intel 80386 (25MHz version), the cycle time is **40ns**. This allows nearly **80ns** for the cache tag address to be compared against the microprocessor address and the data cache SRAM to be accessed (a minimum of two cycles are required for the read instruction). IDT's cache tag SRAMs and data cache SRAMs can be used to meet the timing requirements of most microprocessors. The IDT7174 8K x 8 cache Tag SRAM features a match time of **20ns** (maximum) while IDT's 7164 8K x 8 has a cycle time of **20ns** (maximum). When both the cache memory and cache tag are accessed simultaneously, valid data can be placed onto the microprocessor address bus in nearly **20ns** (address to match time of the cache tag (20ns) is equal to the access time of the cache memory (20ns) in the above). Here, the controller will start the cycle as if the data is in the cache memory, if later during the cycle it was determined that the data is missing from the cache, the controller will float the I/Os of the cache memory and accesses the main memory.

EFFECTIVE CYCLE TIME

The effective cycle time of a microprocessor based system is the average amount of time that is required to access memory. For a system without a cache, the effective cycle time is equal to the cycle time of main memory (today's 1Mbit DRAMs feature cycle times between 100 and 400ns). However, for a microprocessor system based on a cache, the effective cycle time is a function of the cycle time of main memory, the cycle time of the cache and the hit ratio of the cache, i.e. :

$$t_{eff} = ht_{cache} + (1-h)\, t_{main}$$

where t_{eff} = Effective Cycle Time
h = Hit Ratio
$1-h$ = Miss Ratio
t_{main} = Main Memory Cycle Time
t_{cache} = Cache Cycle Time

A normalized graph showing the effective cycle time for a varying hit rate with a constant main memory cycle time of 200ns on a cache that allows zero wait states operation, is given in Figure 1. From the graph, it can be seen how dramatically the hit rate affects the effective cycle time of the system e.g. for a decrease in the hit rate from 99% to 89%, the effective cycle time of the cache will almost double.

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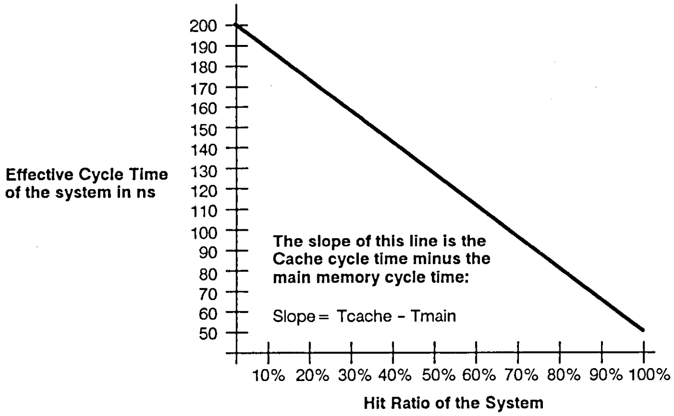


Figure 1. Effective Cycle Time vs. Hit Rate

CACHE ASSOCIATIVITY

Associativity, the number of unique cache memory banks of a cache design, is fundamental to the design of a cache system. The associativity determines the cache architecture, affects, to a degree, the overall performance of the system, plays a role in the selection of the replacement algorithm (pertains to the method used to update the cache memory), and indirectly sets the page size.

Associativity and Cache Architecture

After the designer decides on a cache memory size, he or she must then decide on the associativity so as to obtain the optimized cost/performance ratio. The architecture of the cache memory is dictated by its associativity. For example, if the designer selected a cache memory size of 32Kbytes, the direct mapped cache memory will be one 8K bank of 32 bit words. A 32Kbytes two-way set cache will have two 4K banks of 32 bit words. Finally a 32Kbytes four way set design will have four 2K banks of 32 bit words.

Associativity and Page Size

Because of the different architectures for caches of different associativity, the page size for a given sized cache will vary with the degree of associativity. For the direct mapped 32Kbytes cache, given above, the page size will be 8K doublewords. Similarly, the two-way set associative design will have a page size of 4K doublewords and the four-way set associative will have a page size of 2K doublewords. Since the size of the page is smaller for caches of higher degrees of associativity, the number of main memory pages will also vary with associativity (See Figure 3).

Associativity and Mapping Cache To Main Memory

The 80386's 32-bit address field to be viewed as two fields, a page field (given by the tag) and a line offset field (See Figure 5). Since the page size of main memory is dictated by the size of the cache a direct mapped cache with a cache memory size of 32Kbytes will have a main memory page size of 32Kbytes (or 8K 32-Bit words). Since the page size of main memory is the same size as the cache memory, every address in cache memory directly maps to the associated line in a page of memory i.e. line 5 of the cache maps to line 5 of the main memory page (Figure 2). In this example we will use a line length of 8 bytes. The address 17635 matches the tag 1763X, X refers to an octal digit from 0 to 7. The data associated with the tag 1763X have addresses from 17630 to 17637. Therefore the address 17635 refers to the sixth element in that line. The corresponding data is 72.

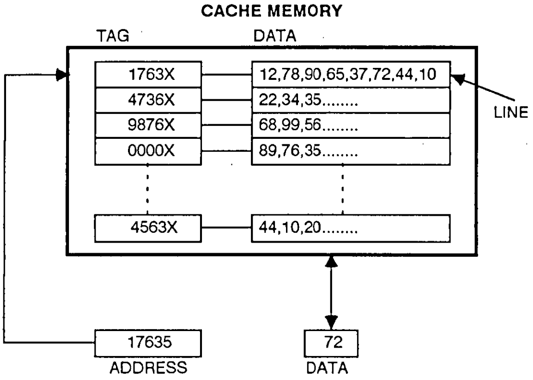
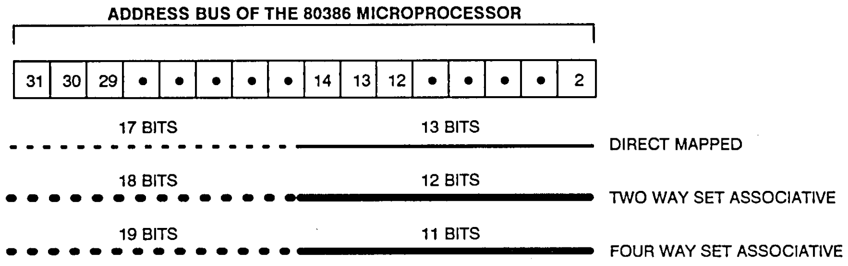


Figure 2. Mapping to Main Memory

Since the page size is affected by the associativity of the cache, the addressing scheme for fixed sizeJcaches of different associativity will also be affected. As shown in Figure 3, the page field for a direct mapped cache is 17 bits while the line offset field is 13 bits. This contrasts to a four way set which has a page field of 19 bits and a line offset field of 11 bits.

The addressing scheme for a cache based on the Intel 80386 is also determined by the size of the cache. If the cache size is 32Kbytes (8K x 32) the 13 LSBs of the 80386 microprocessor address bus will be needed to address each four byte line in the cache. This leaves 17 bits to define the number of pages in main memory i.e. 217 = 128K pages. In summary, an 8K doubleword cache divides main memory into 128K pages of 8K doublewords each.

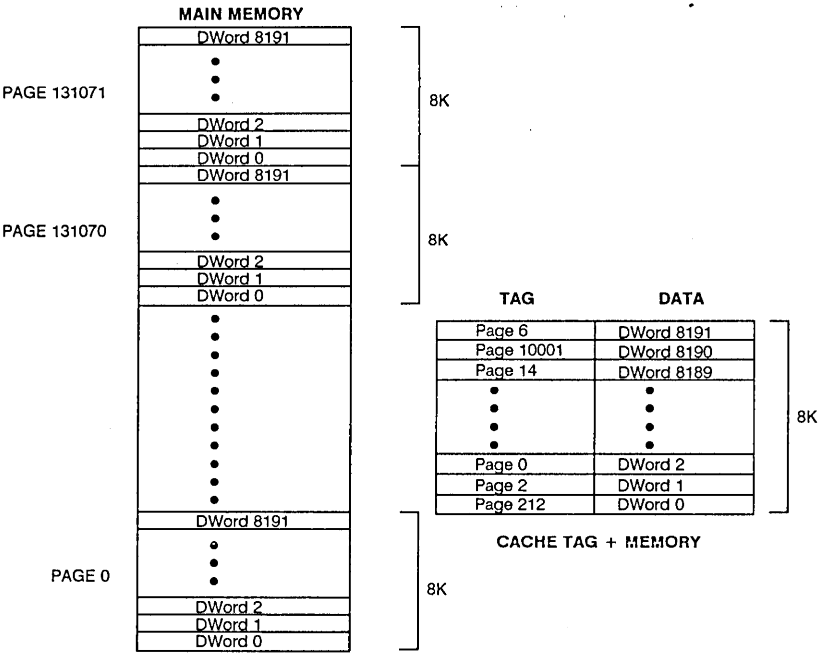


Solid Lines : Address bits that are used to Address the Tag Memory

Dashed Lines: Address bits that are stored in the Tag Memory

	Direct Mapped	**Two way set**	**Four way set**
To address the Tag memory	A(2:14) -> 13 bits	A(2:13) -> 12 bits	A(2:12) -> 11 bits
To store in the Tag memory	A(15:31) -> 17 bits	A(14:31) -> 18 bits	A(13:31) -> 19 bits
Page Size	8K	4K	2K
Number of pages	128K	256K	512K
Number of cache memory banks	1 Bank	2 Banks	4 Banks
Absolute size of the cache memory	1 x 8K	2 x 4K	4 x 2K

Figure 3. Associativity, Architecture, Addressing, and Page Size for a fixed size cache. In the implementation that follows the cache size is 32 KBytes. Figure 3 shows how the address bus of the 80386 should be divided for different associativity of the same size cache (32 KBytes).

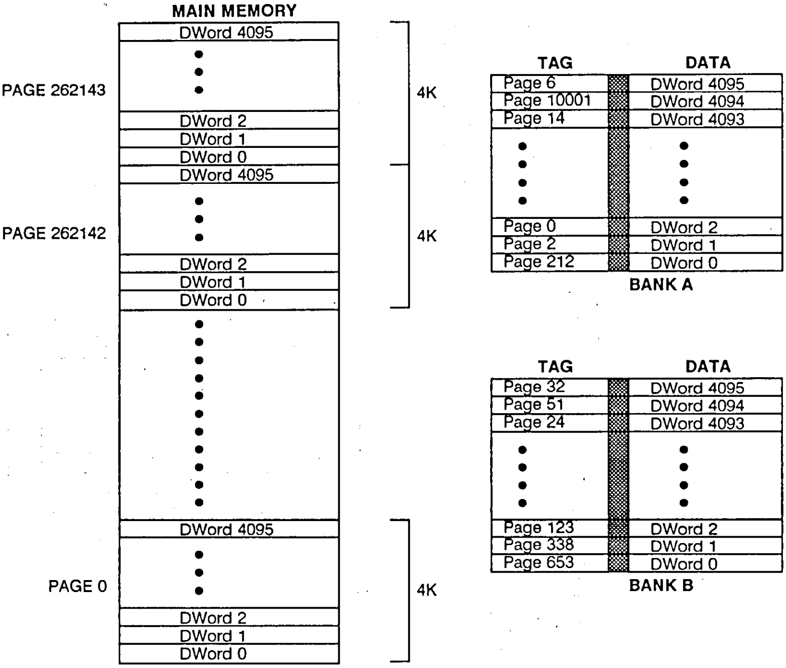


TOTAL MEMORY = Number of Pages x Page Size x DWord

= 128K x 8K x 4Bytes

= 4 GigaBytes

Figure 4A. Direct Memory Mapped representation of a 32 KBytes Cache



TOTAL MEMORY = Number of Pages x Page Size x DWord
= 256K x 4K x 4Bytes
= 4 GigaBytes

Figure 4B. Two-Way Set Associative Memory Map for a cache with a total size of 32 KBytes

The operation of comparison for the cache tag, for the latter example, uses the 13 LSBs of the microprocessor address bus to address the cache tag and compares this accessed address to the 17 MSBs of the microprocessor address bus (Figure 5). Additionally, the valid bit(s) is(are) also examined. If a match occurs the cache memory is enabled and the microprocessor reads the data from cache memory.

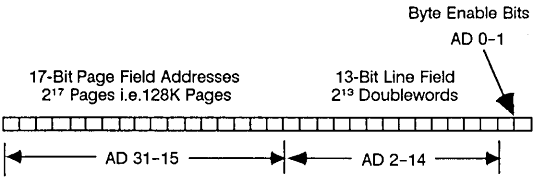


Figure 5. Local Address Bus For 80386 Direct Mapped Design

Performance as a Function of Associativity

The differences in the architectural structure of caches of different associativity results in different performance levels for equivalent program. If one examines the direct mapped architecture, one will notice that it will not permit more than one page/line offset conflict in its cache i.e. page 1/line 2 and page 2/line 2 can not coexist in cache memory. For a two-way set, one will notice that the design will not permit more than two page/offset line conflicts i.e. page 1/line 2 and page 2/line 2 can exist in the cache concurrently, but page 1/line 2, page 2/line 2 and page 3/line 2 can not. Similarly, a four way set will not permit more than 4 page/line offset conflicts.

Thrashing

Because of the existence of page/line offset conflicts, certain programs may result in a situation coined as thrashing—which results in a significant increase in the miss rate. As an example of a program which results in thrashing, consider a direct mapped cache design where the microprocessor must process two lines of code in a repetitive loop e.g. the microprocessor must first read the code on page 2/line 1, then read the code on page 3/line 1 and then go back and read the code on page 2/line 1. For a direct mapped design, such a code structure (or trace) will result in consecutive misses.

Although thrashing occurs most often in direct mapped systems, it can also occur in two-way set or four way set designs. This, of course, is due to the fact that the number of page/line offset conflicts supported by these designs is also limited.

In this example a smaller line size in a direct mapped cache reduces thrashing more than the more common approach of a bigger line size in a two way set associative cache.

REPLACEMENT ALGORITHMS

Replacement algorithms for caches pertain to the method used to update the cache memory. The replacement algorithm is important in that it will affect the hit rate of the system which in turn alters the effective cycle time of the system (and hence the MIPs rating) Replacement algorithms, are designed such that the cache is updated with data or code that will be most frequently used by the microprocessor. Conversely, replacement algorithms are also designed to delete data or code that is least frequently used.

There are several types of replacement algorithms used for caches. Three of these are the least recently used (LRU) algorithm, the First In First Out (FIFO) algorithm and the random replacement algorithm. The least recently used algorithm, on a cache read miss, replaces the data/code in the cache that in relation to the other code/data was not used last. The random replacement algorithm replaces data/code in the cache by random selection. Finally, the FIFO algorithm replaces data that entered the cache first i.e. the oldest data in the cache.

The associativity of the cache, i.e. direct mapped, two-way set, or four way set, often dictates the replacement algorithm chosen. For direct mapped caches, for example, there is no need to consider a replacement algorithm. This is because the direct mapped hardware design requires that the cache be updated, on a miss, with the corresponding page/line address from main memory.

For the two-way set cache, because of its design, one has the option, on a cache miss, to update either of two cache addresses (in one of the two ways). The LRU algorithm is often used here because it only requires one memory bit in the cache tag to determine which way of the cache was accessed last. On a cache miss, the LRU bit is checked, and, for example, if it is set, the data in way 1 is replaced. On the other hand, if it is reset, the data in way 2 is updated.

For caches with associativity greater than or equal to 4, a random replacement algorithm is often used. This is because it offers a hit rate comparable to that of other algorithms and requires a pseudorandom number generator to implement.

LINE SIZE SELECTION

Line size is a term used in cache design that refers to the unit of transfer (in Bytes) between the cache and main memory. For the majority of 32-bit systems, the line size is often chosen to be 4 bytes A line size of 4 bytes simplifies controller logic and problems associated with byte boundaries. The line size, however, has an affect on the overall performance of a system. As one increases the line size, the effective hit rate of the system goes up (for a fixed size cache) which increases the overall MIPs performance of the system. On the other hand, a larger line size will result in an increase in the amount of system bus traffic. Which is, of course, due to the greater number of bytes transferred on a cache miss.

Depending on the type of system design, the size of the line chosen will affect the overall system performance. For multiprocessing systems, where it is desirable to keep system bus traffic to a minimum, a small line size is often opted for.

Table 1 illustrates the affect of line size for different size caches on the overall system throughput, where "a" is the marginal transfer time per byte and "b" is the overhead per miss.

Cache Size (bytes)	a = 15 ns/byte b = 360ns	a = 15 ns/byte b = 160ns	b = 600ns
32	4 - 16	4 - 8	8 - 16
64	8 - 16	4 - 16	8 - 32
128	8 - 16	4 - 16	8 - 32
256	8 - 32	8 - 16	16 - 32
512	8 - 32	8 - 16	16 - 64
1024	8 - 32	8 - 16	16 - 64
2048	16 - 32	8 - 32	16 - 128
4096	16 - 64	8 - 32	32 - 128
8192	16 - 64	8 - 64	> = 64
16384	16 - 128	8 - 128	> = 64
32768	16 - 128	8 - 128	> = 64

Table 1. Optimized Line Size vs. Cache Size and Delays. This table was taken from A. Smith's paper on cache memories.

COHERENCY– DEFINITION AND COMPONENTS OF

Coherency is defined as the capability of cache memory to replicate in real time the current contents of main memory. Cache coherency is necessary in all cache based microprocessor designs where an external device can control the bus and write to main memory. If a system has a DMA device, more than one microprocessor, or memory mapped I/O devices, coherency logic must be considered.

WRITE COHERENCY HARDWARE

Write operations require special considerations in cache design. For a microprocessor write operation to main memory, in order to maintain local cache and main memory coherency, the local cache memory must be updated along with main memory.

In order to ensure write coherency, there are a number of hardware techniques. The three most popular design techniques are the copy-back, write-through, and buffered write through schemes. Each of these techniques offers different advantages. The copy-back and buffered write through schemes feature increased system throughput. On the other hand, the write-through scheme offers minimized support logic.

For a write-through based cache design, every time the microprocessor write occurs the code/data is written simultaneously to the cache and main memory. Because of the fact that main memory is slower than cache memory, the time to implement a write is governed by the cycle time of main memory. This, of course, puts a limitation on the effective cycle time of a cache system based on a write through scheme.

A hardware modification to the write-through design that allows for a reduction in the effective cycle time is a high speed buffer. This design, often referred to as a buffered write-through or posted write, improves the performance by allowing the microprocessor to operate out of the cache, at cache speeds, after a microprocessor write operation. This is in direct contrast to the write-through which requires that the microprocessor wait for the completion of the main memory write cycle. In a buffered write-through cache system, when a write occurs, the cache and buffer are updated with the write data, allowing the microprocessor to read from the cache again. During this time, the buffered write-through logic takes control of the system bus and updates main memory by downloading the file buffer. Adding a buffer, of course, increases the number of components for the cache module.

A copy back system operates on the use of a dirty bit that is stored along with the cache tag address. For a copy-back scheme, when a cache write hit occurs, the associated dirty bit is set which indicates that the data in the cache is no longer coherent with main memory. When another bus master requests control of the bus, before releasing the bus, the cache controller will update all the locations in the main memory that are not coherent with the content of the cache memory as a result of cache write hits. A cache write miss will occur when the microprocessor attempts to write to a location that was not cached earlier.

The disadvantage of a copy-back system becomes apparent in the design of multiprocessor and multi-master based systems. In these systems, any external read from main memory requires that all caches in the system be checked to see if the dirty bit has been set for each address written. If the dirty bit has been set, the associated data entry in the cache must be downloaded to main memory before an external device accesses that address.

Although, the buffered write through has a somewhat lower performance than a copy-back (because of main memory traffic during write misses), write-through and buffered write through are often preferred to use in multiprocessing systems. This is because, as mentioned above, there are a number of coherency issues that must be dealt with for a copy-back scheme.

COHERENCY LOGIC– FOR DMA AND MULTIPROCESSOR SYSTEMS

In order to maintain coherency for multiprocessing and DMA applications, a cache design needs to be able to monitor the system bus for external device writes to main memory. If a write to main memory occurs from an external device, it is necessary to inform the cache memory of the address written to so that the cache controller can decide whether or not to invalidate the cache memory contents (either by flushing the entire cache or by clearing the associated valid bit of the entry).

Architectures for Cache Coherency

There are two common architectures used to achieve coherency in microprocessor based systems; a time-multiplexed cache tag architecture and a dual cache tag architecture. For the multiplexed cache tag architecture, the cache is time multiplexed between the system address bus and the local address bus. This permits the controller to check if the system address location written to is in the cache memory. For the dual cache tag system, one cache tag is used to monitor the local address bus and another cache tag (the SNOOP tag) is dedicated solely to monitoring the system address bus.

Dual Cache Tag vs. Time-Multiplexed Cache Tag Architecture

The advantages of a dual cache tag system over a time-multiplexed cache system are seen when one examines the timing requirements of the two, i.e. the dual cache tag design can work with a much shorter microprocessor cycle time. The time-multiplexed scheme uses the same physical tag memory to tag the addresses present in the cache memory (tag) and checks the main memory's address bus activity (SNOOP). When the processor requests data of any address, the page field of its address bus is compared against the one stored in the tag memory, if they match a hit occurs else a miss is issued. The remaining part of the cycle, the tag memory acts as a SNOOP memory i.e. it monitors the main memory's address bus activity for any write to an address with a matching page field. In the latter case a SNOOP hit is issued and the controller could either invalidate that particular entry or flush the content of the entire cache.

As can be seen from the above, the time-multiplexed scheme requires two sequential cache tag comparisons, i.e. the CPU address bus is compared against the contents of the cache tag and then the system bus is compared against the contents of the cache tag. This, of course, results in a delay time equal to the time it takes to perform two accesses to cache tag memory plus the time it takes to multiplex between the system bus and the CPU bus.

The dual cache tag scheme when compared to the time-multiplexed scheme permits a significant reduction in the microprocessor cycle time. This is because, as opposed to the time-multiplexed scheme, the dual cache tag scheme allows for the system bus address tags (SNOOP tag) and the CPU address bus tag (cache tag) to function at the same time. On the instigation of a system bus transfer, the system address bus page field (or tag) is compared against the page field stored in the SNOOP tag. At the same time, the CPU bus page field is compared against the page field stored in the CPU bus cache tag. If the SNOOP tag page address does not match the system bus page address, the controller continues onto its next cycle. If, on the other hand, the SNOOP tag did match the system address page field, the associated valid bit of both cache tags are cleared or both cache tags will be reset.

This means, of course, that the microprocessor cycle time required for the dual cache scheme (equal to the time it takes to perform one cache tag access and comparison) is less than one-half of that required by the time multiplexed scheme (equal to the time it takes to perform two cache tag accesses and comparisons).

Implementing a Dual Cache Coherency Architecture

For implementing a dual cache coherency system, IDT7174's cache tag SRAMs can be used to form both the microprocessor cache tag block and the system bus cache tag block (SNOOP tag)—as shown in Figure 7. For a dual cache based system, the SNOOP memory is always identical to the microprocessor cache memory. This is accomplished by writing the same information at the same time to both system (SNOOP) and CPU cache tag memories. The operation of the dual cache is such that when another bus master has control of the system bus and writes data to a previously cached address in main memory, a SNOOP hit occurs. A SNOOP hit will result in the controller either invalidating a particular entry in both cache tags or flushing all the entries in both cache tags.

DESIGNING A CACHE TAG UNIT

In order to optimize cache design, the IDT7174 may be used (Figure 6). This Cache Tag SRAM (8K x 8) has built-in features that help and simplify cache tag design. These include a match output, a reset input, CEMOS™ technology, and three state I/O. The match output is high whenever the address stored in the IDT7174, accessed by the address pins, matches the address at the I/O pins. The tag is addressed by pins A0-A12 and the tag is compared to the stored tag on the I/O pins via an internal comparator—if they match, the match output goes high. For cache design applications, the match output drives the cache controller which in case of a match (hit) places the data contents of the cache memory on the microprocessor data bus. The reset input (active low) allows the entire contents of the cache tag memory to be cleared which permits reset on system power up and the cache to be flushed (for coherency applications).

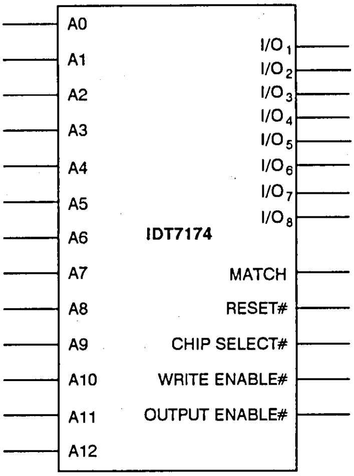


Figure 6. The IDT7174 8K x 8 Cache Tag SRAM

The IDT7174 features an address to match time of 20ns, making it suitable for applications up to 40MHz along with fast SRAMs to build the cache memory for two-cycle machines such as the Intel 80386). It is also cascadable in depth and width which allows caches to be easily designed for a variety of different microprocessor address bus widths.

Figure 7 illustrates a cache tag SRAM comprised of three IDT7174's organized as IDT8192 23-bit words. If used in a microprocessor based system, main memory would be divided into 8 Million pages. The lower address bits specify the line offset in the cache where the lower page address tag is stored. The 23 bit page address (within the cache tag SRAM) accessed by the 13 lower microprocessor address bus bits is compared against the 23-Bit microprocessor page address. If there is a match from all three, the wired AND match output will go high indicating that the needed data is in the cache memory.

I/O 8 of the last IDT7174 is the cache data valid bit. This bit is used to indicate that the data in the cache is valid. On power up or a cache flush the valid bit is very useful.

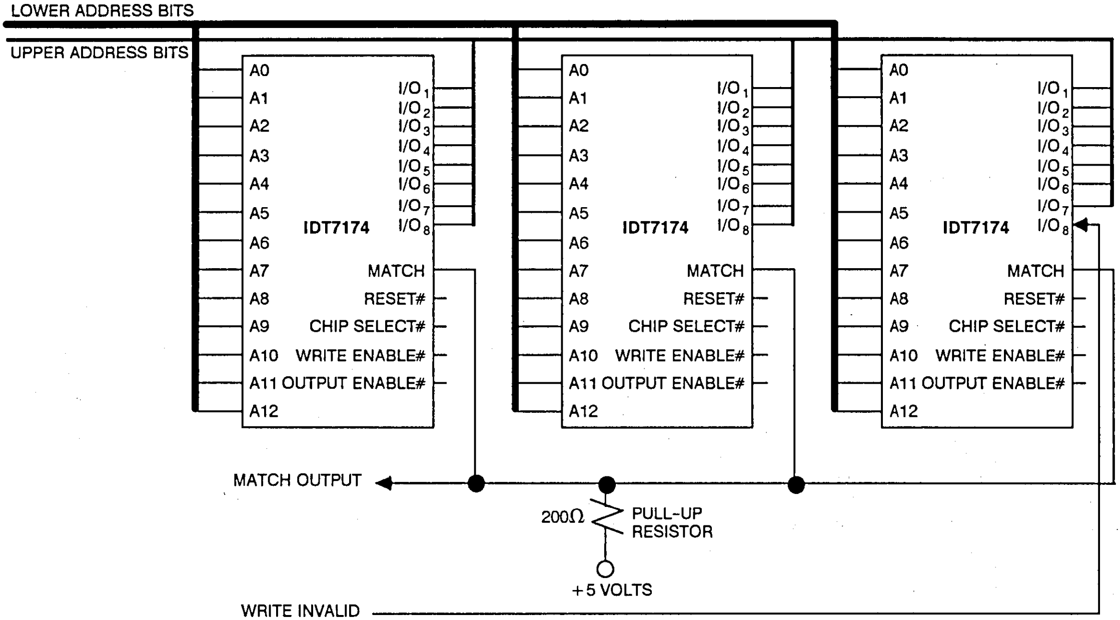


Figure 7. A Cache Tag Unit

A CACHE CONTROLLER AND MEMORY MODULE FOR THE 80386

For the design of a cache controller, one must become familiar with the microprocessor that is being used, its interface and signaling requirements. As well, one must decide on the cache's associativity, depth, configuration and ensure that all critical microprocessor and system timing requirements are met. The design of the cache controller must then be considered to allow for functions such as coherency, bus arbitration, and state machine sequencing (to control the interface to the system bus and the microprocessor).

For the design that follows, an 80386 microprocessor is used (25MHz Version) which incorporates a dual cache tag coherency architecture.

80386 Microprocessor Cache Considerations

In the following processor description and cache system implementation, when a "#" sign follows the name of a signal it indicates that this signal is active low, if there is no "#" sign at the end of a signal name, it means that it is an active high signal.

The 80386 microprocessor from Intel is the current mainstay of both the PC market and low end workstation market. The 80386 is currently used in the leading edge IBM PCs, Compaq's microcomputer and in Sun's new multitasking workstation.

The 80386 (Figure 8) is based on low power CMOS technology and comes in 16MHz, 20MHz, and 25MHz versions.

As illustrated in Figure 8, the 80386 has an effective 32 bit address bus giving an address space of 4 Gigabytes. The address bus consists of address lines A2-A31 and four byte enable lines BE0#-BE3#. The byte enable signals allow the 80386 to address one or an adjacent combination of the 4 bytes contained in the 80386's 32-bit word.

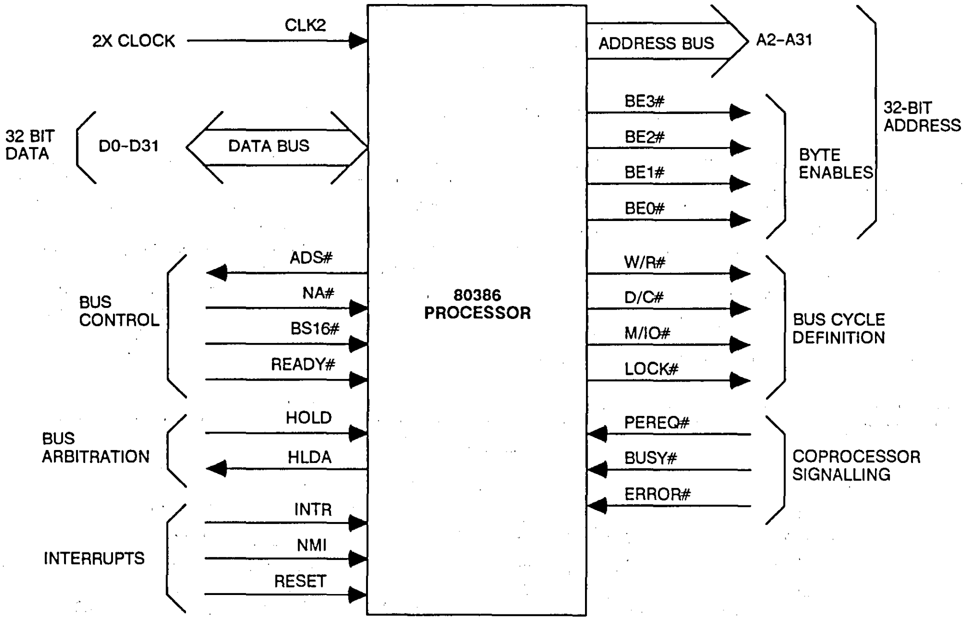


Figure 8. The 80386 Microprocessor

80386 Microprocessor Signals

The 80386 microprocessor signals can be divided into bus cycle definition signals, bus control signals, bus arbitration signals, and interrupt signals. The bus cycle definition signals define attributes and conditions of the current bus cycle in progress, e.g. memory read or I/O write. The bus control signals, on the other hand, control the operation of either the bus or microprocessor, e.g. inform the microprocessor of the completion of a cycle or the transfer of a 16 bit word. Bus arbitration signals are used to arbitrate the control of the bus by competing bus masters, e.g. HOLD and HOLD Acknowledge. Finally, interrupt signals are used to interrupt the current process of the microprocessor so that another process may be executed, e.g. NMI#.

80386 Bus Cycle Definition Signals

Lock# (Lock) indicates that the current microprocessor cycle under execution can not be interrupted i.e. by an interrupt signal.

W/R# (Write or Read) signals whether or not the microprocessor is in a read cycle or write cycle.

M/IO# (Memory or I/O Cycle) indicates whether or not the cycle is a memory access or I/O access.

D/C# (Data or Control Cycle) signals whether or not the current bus cycle is a data or control cycle.

80386 Bus Control Signals

ADS# (Address Status) is an address status signal which indicates that the address issued by the microprocessor is valid and ready for sampling.

READY# is an input to the microprocessor that indicates the end of the current bus cycle.

NA# (Next Address) is an input to the microprocessor that is used to instigate the high-speed pipeline mode.

BS#16 (Bus Size 16) is an input to the microprocessor that informs the microprocessor that 16-Bit data is to be transferred

Interrupt and Interface Signals

CLK2 is the microprocessor clock input provided by a crystal (twice the microprocessor clock frequency). This signal is divided by two inside the microprocessor.

RESET is an input to the microprocessor that forces the 80386 to a known state.

Bus Arbitration Signals

HOLD is an input signal to the 80386 that requests that the 80386 relinquish control of either the local bus or system bus so that an external master can take control of the bus.

HLDA (Hold Acknowledge) is an output from the microprocessor that signals to an external bus master that it has received and acknowledged a HOLD signal and has released the bus.

Microprocessor Cycles

Figure 9 illustrates the basic timing for a microprocessor cycle. CLK2 serves as the timing reference for the microprocessor bus cycles. This signal is divided by two to form the internal CLK signal (for a 25MHz 80386, CLK2 would be 50MHz and CLK would be 25MHz). The bus cycle of the microprocessor consists of two bus states, T1 and T2, which are further subdivided into two phases each, 01 and 02.

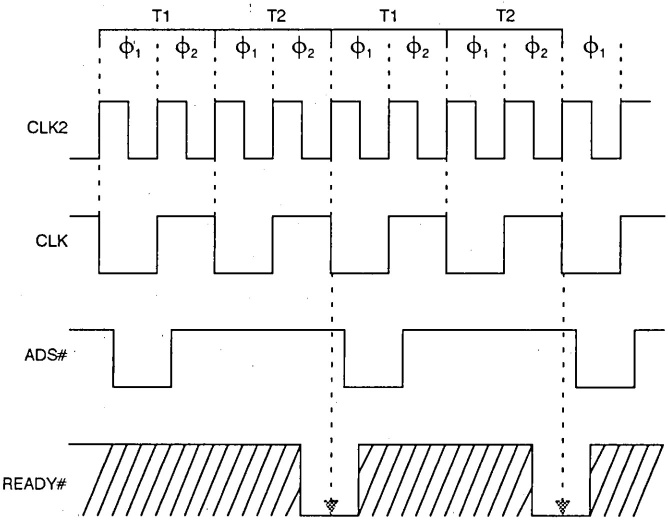


Figure 9. Basic Timing Waveform for 80386 2 State Cycle

The Intel 80386 requires a minimum of two 25MHz cycles to complete any instruction. The start of a microprocessor cycle is characterized by ADS# going low which indicates that there is a valid address on the microprocessor bus. At the end of bus state T2, the microprocessor checks the READY# input to see if the cycle is finished. If READY# is low, it means that the current cycle is completed which allows the microprocessor to start a new bus cycle. On the other hand, if READY# is high at the end of T2, the processor will stay in the T2 bus state until it sees a low level on the READY input. For this condition, all added T2 bus states are called wait states (Figure 10). In cache design, for a miss, the READY input remains high until data is returned from main memory. If there is no pending action required by the microprocessor after T2, the microprocessor will enter in an idle state, Ti (ADS# will remain high—Figure 11).

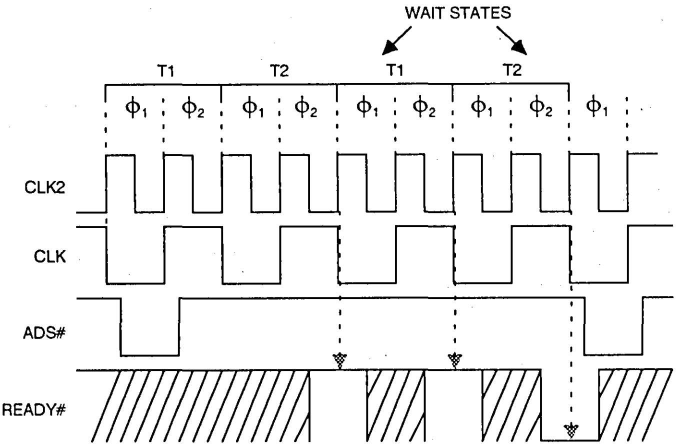


Figure 10. An 80386 Bus Cycle With 2 Wait States

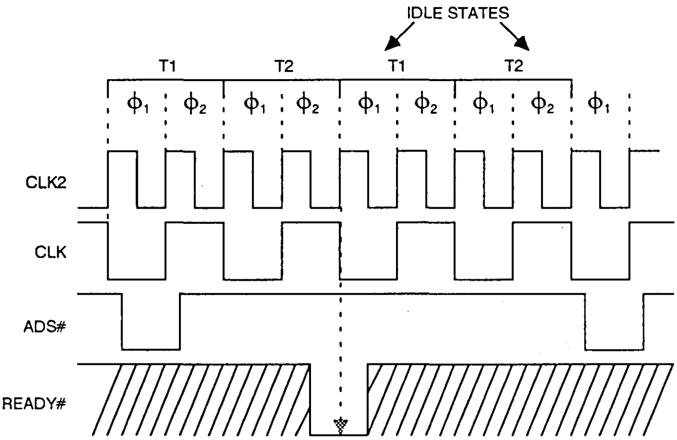


Figure 11. An 80386 Cycle Followed By Two Idle States

When designing a cache system with the 80386 microprocessor, it is important to remember that the only time when the microprocessor probes the READY# input is at the end of T2. The rest of the time, the processor ignores the logic state of the READY# input.

Another bus cycle that is important in the design of a controller for cache memory operation is the hold-hold acknowledge cycle (Figure 12). When another bus master (e.g. DMA Device) wants to take control over the bus, it asserts the HOLD signal that feeds the microprocessor. When the microprocessor sees the HOLD signal go high, it will finish the current bus cycle it is executing, float its data, control and address buses, and then issue a HLDA (hold acknowledge) signal to the external bus master. However, if the LOCK# pin is active on the microprocessor, a HOLD will not be acknowledged by the microprocessor. The lock signal effectively prevents any device from interrupting the microprocessor process in progress.

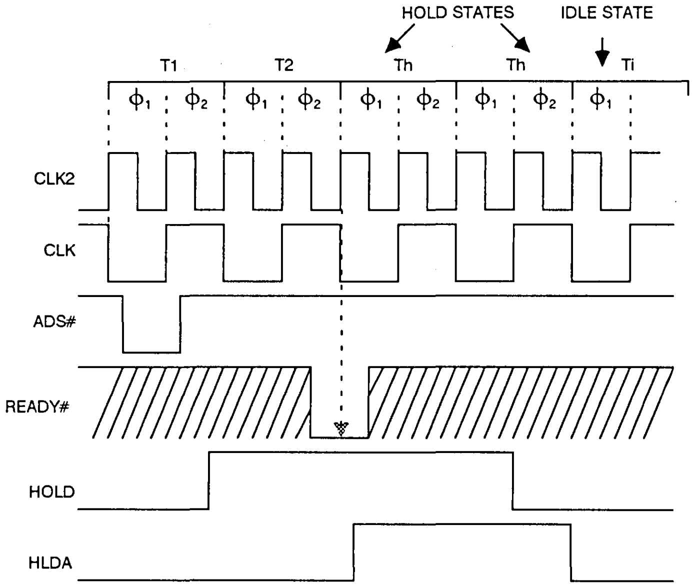


Figure 12. A Two Hold 80386 Cycle Followed By An Idle State

State Diagram

Figure 13 shows the state diagram for the 80386 operating in non-pipelined mode. After the microprocessor is first turned on, a RESET pulse will put the 80386 into a known state. When the 80386 receives a RESET pulse, it will automatically fetch its first instruction from address 0FFFFFFF0H. Usually, at this address, there is an unconditional jump to the location where the bootstrap routine is located(the BIOS).

For pipelined mode the NA# pin must be asserted. For a discussion of pipelined mode for the 80386 refer to the Intel 386 Microprocessor Reference Manual.

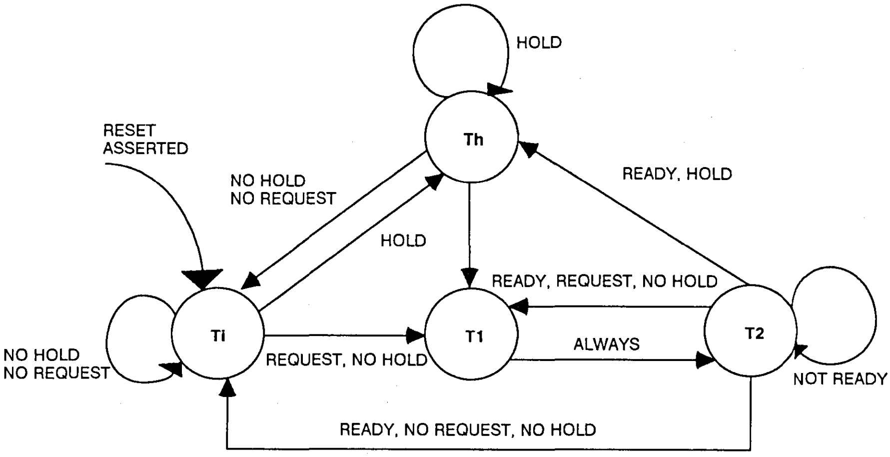


Figure 13. State Diagram For The 80386

CACHE CONTROLLER DESIGN

Cache Associativity, Depth, Page Size, and Line Size Selection

One of the first considerations for the design of a cache controller is the selection of the cache memory. For this design, a direct mapped cache is selected with a cache size of 8K x 32. The 8K data cache divides main memory into 128K pages of 8K doublewords (a doubleword is 32 bits or 4 bytes). The line size selected for this cache design is 4 bytes.

It should be recalled that for a direct mapped cache (Figure 2) every line in the cache will map to a corresponding line in a page (given by the tag) in main memory e.g.. line 0 of the cache will always map to line 0 of a main memory page (given by tag). This, of course, means that it is impossible to have more than one unique line address in a direct mapped cache e.g.. line 0/page 1 and line 0/page 3 can never coexist in the cache.

Cache Controller Hardware Overview

Figure 14 illustrates the block diagram of the dual cache controller to be designed for the 25MHz version of the 80386. The design consists of; two cache tag SRAM blocks, one for the system bus and one for the CPU bus; three PALS used for the design of the cache controller state machine; a data cache SRAM block for the microprocessor; and a number of 74F logic blocks that serve as data/address/control logic and system bus drivers.

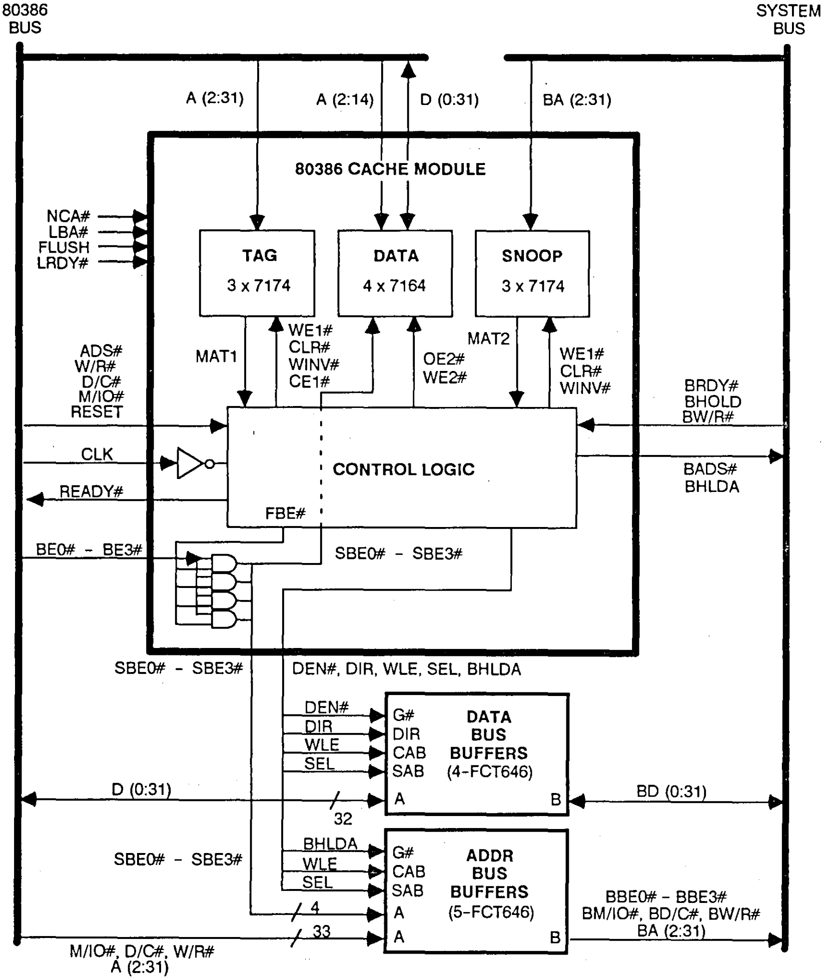


Figure 14. Block Diagram of the Complete Cache System

For the CPU cache tag, a 8K x 24 cache tag is used (Figure 28 and 30) which is constructed from three IDT7174 cache tag SRAMs. The system bus cache tag (SNOOP tag) is constructed exactly the same i.e. with three IDT7174's.

For proper termination of a bus cycle, a 74F64 And Or Invert gate is used (Figure 31) to drive the READY input of the 80386. The 74F64 is used in order to meet the critical timing requirements of the READY signal.

The buffer network is built from nine IDT74FCT646's to form the address, data and control bus buffers. The IDT74FCT646 is a Fast CMOS Octal Transceiver Register with an 8-Bit A register and an 8-bit B Register. The 646 block allows for the bidirectional transfer and temporary storage of 32 bits of data. The DIR (direction) pin is used to control the direction of data flow between the processor's data bus and the system's data bus (Figure 14).

The system bus tag (SNOOP tag) monitors the addresses on the system's address bus when an externally controlled data transfer takes place (e.g. DMA). If the SNOOP tag detects an address that is contained in the CPU cache tag (when BHLDA is active and when a write occurs), the entire content of both cache tags is flushed via the reset input of the IDT7174.

The Microprocessor Interface

The microprocessor interface consists of four byte enable pins. The bus cycle status pins i.e. D/C#, MI/O#, W/R#, clock and reset signals, the address status pin ADS#, and the four local control signals FLUSH#, LRDY#, READY#, RESET, LBA# and NCA# (see Figure 15 for a complete description of the microprocessor and system interface pins).

The NCA# input is for decoding non-cacheable addresses such as I/O memory space. The designer needs to design a decoder that recognizes non-cacheable addresses. The decoder output ties directly to the NCA# input. LBA# is used to indicate that the 80386 is working with a local device (such as a coprocessor).

System Bus Interface

The system bus interface consists of the buffered data bus (BD0:31), the buffered address bus, (BA2:31), the bus byte enable signals (BBE0#-BBE3#), the system bus control signals (BM/IO#, BDC#, and BW/R#), and the system control signals of BRDY#, BHOLD, BADS# and BHLDA. It should be noted that the 80386 equivalent front end signals of the controller module are prefixed by the letter B (For a complete listing of system bus interface signals, see Figure 15).

SIGNAL DESCRIPTION

- **BA (2) - BA (31)** are the 30 address pins that connect the system address bus to the cache module. These 30 pins form the BA bus or the board address bus.
- **BHOLD** is an input to the cache module. BHOLD (bus hold) is asserted by system when another bus master wants to take control of the bus. BHOLD is active high.
- **BHLDA** is an output from the cache module to the system. When Bhold is asserted by another bus master, the cache module responds by activating BHLDA (bus hold acknowledge), the other bus master is then granted control of the bus.
- **BRDY#** is an input to the cache module. When the system asserts this pin, it indicates that the current memory cycle is complete. BRDY# is active low.
- **SBE0# - SBE3#** are four output signals from the cache module. They are the individual byte enables for the memory. These four signals are active low.
- **BADS#** is an output from the cache module to the system. When BADS# (board address status) is asserted, it indicates that the BA bus is stable. BADS# is active low.
- **BW/R#** is an input to the cache module from the system. BW/R# (board write read) is used in the SNOOP function of the module and helps the device to detect when a write has occured to an active cache address.
- **RESET** is an input to both the cache module and the 80386. The RESET signal comes from the system and is asserted for 8 or more CLK periods so that the processor and the cache module will be placed in a known reset state. The tags of the cache will be cleared. RESET is active high.
- **FLUSH** is an input to the cache module. While FLUSH is asserted, it will cause the tags to clear. This pin is a "programmable reset". This signal is active high.
- **LRDY#** is an input to the cache module. LRDY# is an indication to the module that a local bus cycle is complete. This signal is active low.
- **W/R#** is an input to the cache module. When W/R# is high it indicates that the 80386 is executing a write cycle and when it is low it shows that the processor is executing a read cycle.
- **ADS#** is an input to the cache module. This signal shows the status of the A bus. When ADS# is low it indicates that the address bits A (2) - A (31) are stable. This signal is active low.
- **CLK** is an input to the cache module. It is identical to the 80386 clock.
- **A (2) - A (31)** are the 30 address pins that connect the 80386 address bus to the cache module. These 30 signals are the A bus.
- **BE0# - BE3#** These four byte enable signals are outputs from the 80386 and are tied directly to the byte enable inputs of the cache module.
- **NCA#** is an input to the cache module, while active it indicates to the device that the current address present on the address bus, A (2) - A (31), is a non cache-address. This signal is active low.
- **D/C#** is an input to the cache module. D/C#, data-control, is used by the 80386 to indicate a data cycle or a control cycle. While low the processor is in a control cycle and while high in a data cycle. No cache operations are permitted in control cycles.
- **M/IO#** is an input to the cache module, while low it indicates that the 80386 is addressing an I/O device and while high it indicates the processor is addressing memory. No cache operations are permitted for I/O devices.
- **LBA#** is an input to the cache module, while active it indicates that the processor is accessing another device on the local bus, for example the 80387 coprocessor. Local bus addresses are not cache addresses.
- **DIR, DEN#** are outputs from the cache module. These signals control the data bus buffers and the address bus buffers (external to the module). DIR determines the direction of the flow of the data bus buffers. DEN# is the enable signal and is used to turn on the bus drivers.
- **WLE** is an output from the cache module to the data bus buffers and to the address bus buffers. WLE is used to latch write data into the write buffers.
- **SEL** is an output from the cache module. It is used to select the latches in the data bus buffers and the address bus buffers.
- **D (0) - D (31)** These 32 signals are the data bus connecting directly to the data bus of the 80386. They are also connected to the data bus buffers.
- **READY#** is an output from the cache module. When asserted it indicates to the 80386 that the current cycle is finished. This signal is active low.

Figure 15. Functional Cache Controller and 80386 Signal Descriptions

Timing Diagrams for the Cache Design

Figures 16 through 26 illustrate the cache controller and memory module timing diagrams for a number of different bus cycles, namely cache read miss, cache read hit, write cache hit, write cache miss, read LBA, write LBA, read NCA, write NCA, BHOLD, and BHLDA. Figures 25 and 26 illustrate the cache tag and cache memory timing for both the cache and SNOOP tag.

Cache Read Miss and Hit Cycles

The cache read hit cycle, illustrated in Figure 16, begins by ADS# going low followed by the W/R# signal going low (to indicate a read). The controller responds by driving WE1# high. The WE#1 signal which drives both the local bus cache tag and the SNOOP tag sets the two cache tags up for a read and compare operation. After the read and compare operation is complete, the MAT1 signal will be valid. At this point in time (at the beginning of bus state T2) the cache controller samples MAT1. If MAT1 is high, it indicates that the cache memory has valid data. The controller responds to this condition by sending its OE# signal low which in turn enables the output of the cache memory to drive the microprocessor data bus with its associated 32-bit data word.

On the other hand, if MAT1 was low, the controller would respond by entering into a cache read miss cycle (as shown in Figure 17). This condition indicates that the address is not cached. For the cache read miss cycle, the cache controller drives the DEN# signal low which connects the local data bus to the system data bus. The control signals ADS# and W/R# are duplicated by BADS# and BW/R# which are placed on the system bus to allow main memory access. The system bus responds with the required data and then drives BRDY# low when done. During the main memory access, the controller updates the cache memory with the new data, the local bus cache tag and the SNOOP tag with the associated tag. After the controller receives the BRDY# signal from the system bus, it then drives READY# low which terminates the bus cycle. It should be noted here, that for the cache read miss, the READY# signal is held high an amount of time equal to the main memory cycle time.

Cache Write Hit and Miss Cycles

When the microprocessor writes data to memory it may enter into a write hit cycle or a write miss cycle (Figures 18 and 19). As with the cache read hit cycle, the beginning of the cycle is instigated by ADS# going low, but with W/R# going high. This state results in the controller enabling the local and SNOOP cache tags for a read and compare operation. If MAT1 is returned high to the controller from this tag, a write hit has occurred which results in the controller enabling the cache memory for a write operation (via the WE2# line). At this time the CPU data bus is written into the cache memory.

For either a cache hit or miss cycle, the cache controller also drives the WLE line of the posted write latch such that the address and data bus contents are captured for the system bus. For a write miss, the controller exhibits similar timing as it does for the write hit. However, for a write miss, the cache controller will start writing to both cache and main memory as if it was handling a write hit cycle. If later during T2 it was determined that a miss had occured (via MAT1) then the new content of that cache location does not correspond to the tag address. The WINV# signal will be driven low to invalidate the corresponding tag in the cache tag and the SNOOP tag (see Figures 28 and 30).

LBA and NCA Read and Miss Timings

LBA and NCA both deal with special conditions. The LBA (local bus access) cycle occurs when another device is to be accessed on the local bus for a read or write operation. For the Intel 80386 this is most often a numerics coprocessor. In order to read data from a coprocessor on the local bus, (Figure 20), the LBA input to the cache controller is activated. The cache controller then disables the cache memory (via WE2# and OE2#) the tag and the SNOOP memory (via WE1#). The local ready signal (LRDY) is sent from the coprocessor to the controller indicating the end of the LBA cycle.

NCA (non-cacheable address) cycles are entered into whenever the NCA input to the cache controller is active. The NCA is usually employed to keep I/O data from entering the cache. An active NCA# input results in the controller disabling the cache memory, cache tag and the SNOOP tag. This, of course, keeps the undesired addresses from entering the cache. As noted in Figure 22, the NCA cycle has added wait states due to the fact that the speed of the I/O device is limited. The designer has also the option of mapping the address space in several sections and choosing what section of the address space will be cacheable. This is accomplished by connecting the NCA# input to the output of an appropriate decoder. During NCA# cycles the cache ensemble is totally transparent.

Cache Memory and Cache Tag Timing

Figures 25 and 26 illustrate the timing specifications for the cache memory, the cache tag and the SNOOP tag. The associated tables give the necessary memory timing delays for the 16MHz, 20MHz and 25MHz versions of the 80386 microprocessor. As seen in the table, the READY# signal AC timing specification is met by use of an 74F64 AOI with a delay that is less than 6ns.

READ HIT TIMING

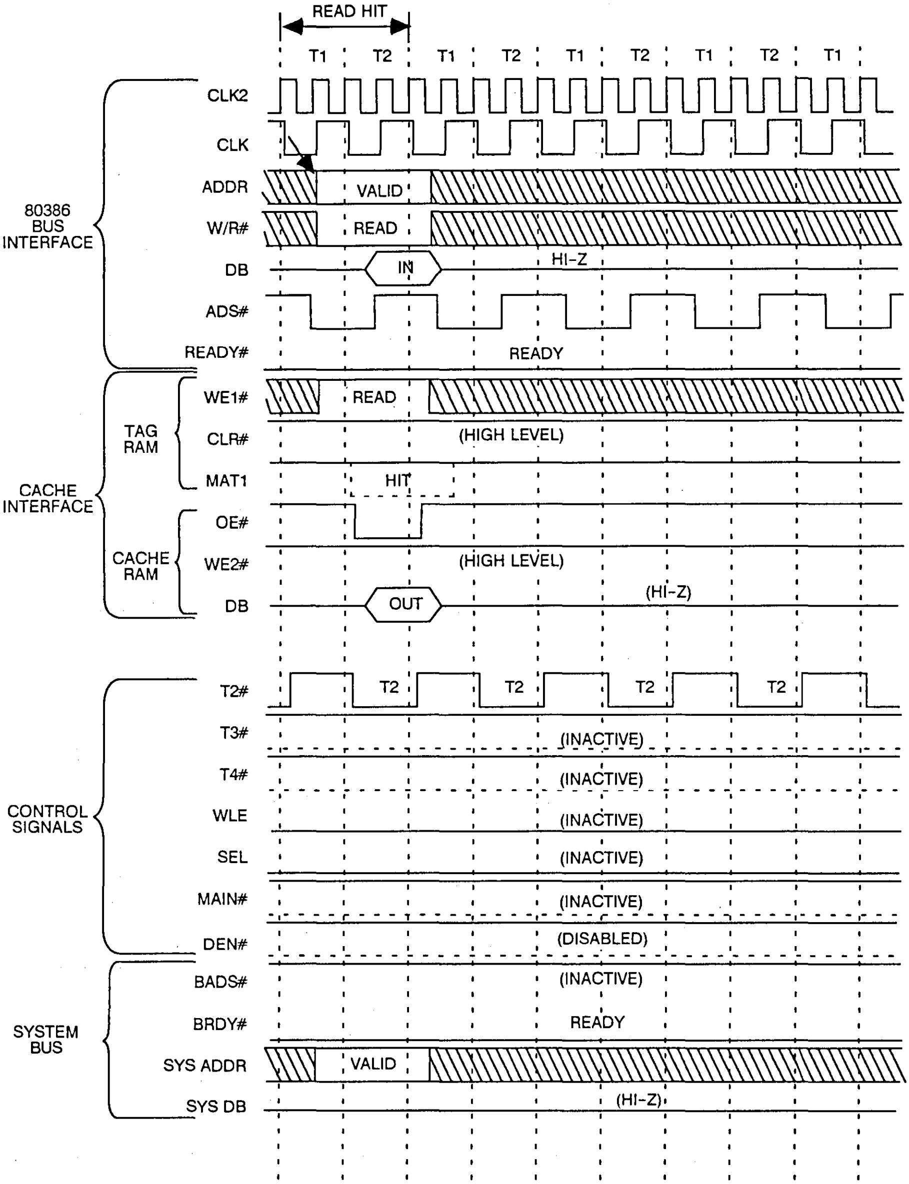
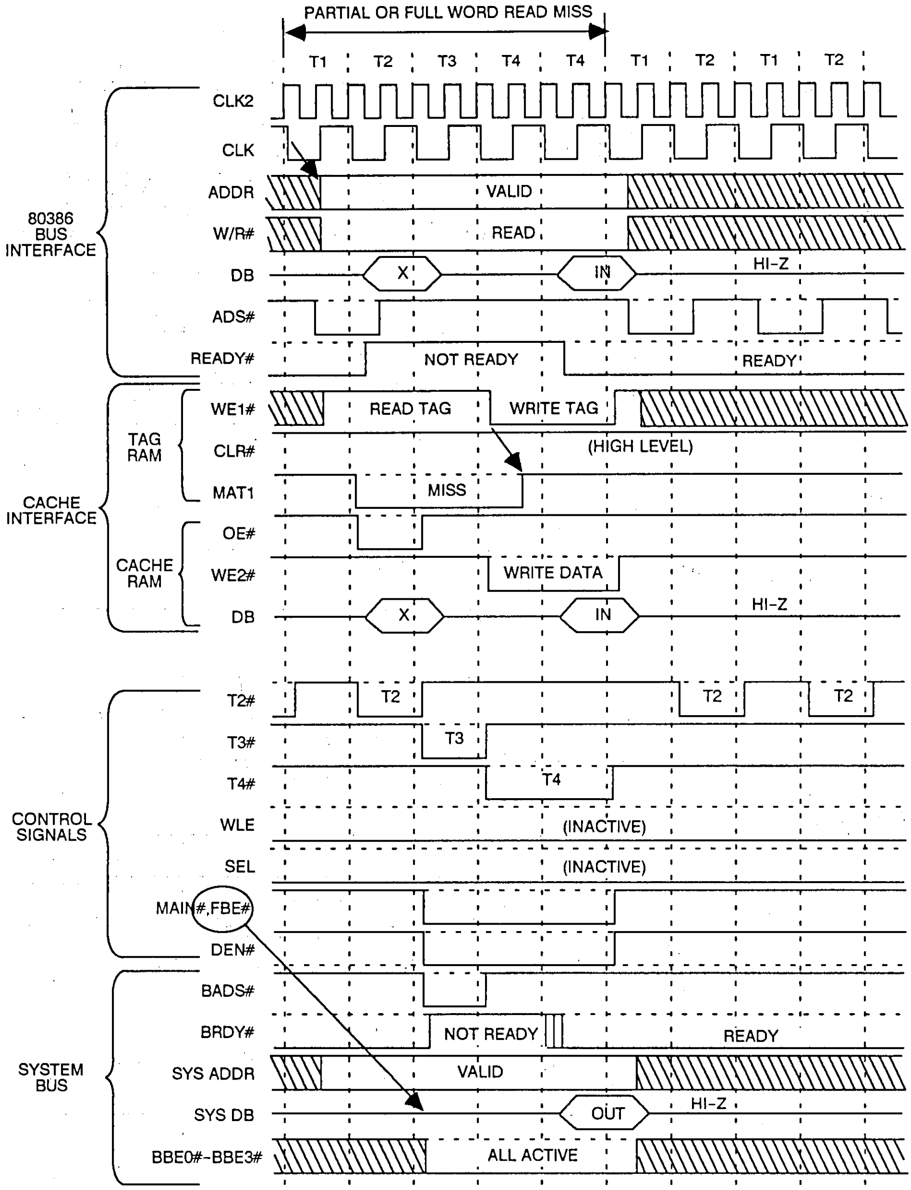


Figure 16. Read Hit Timing

READ MISS TIMING



Note: FBE causes all FB lines to be activated.

Figure 17. Read Miss Timing

WRITE HIT TIMING

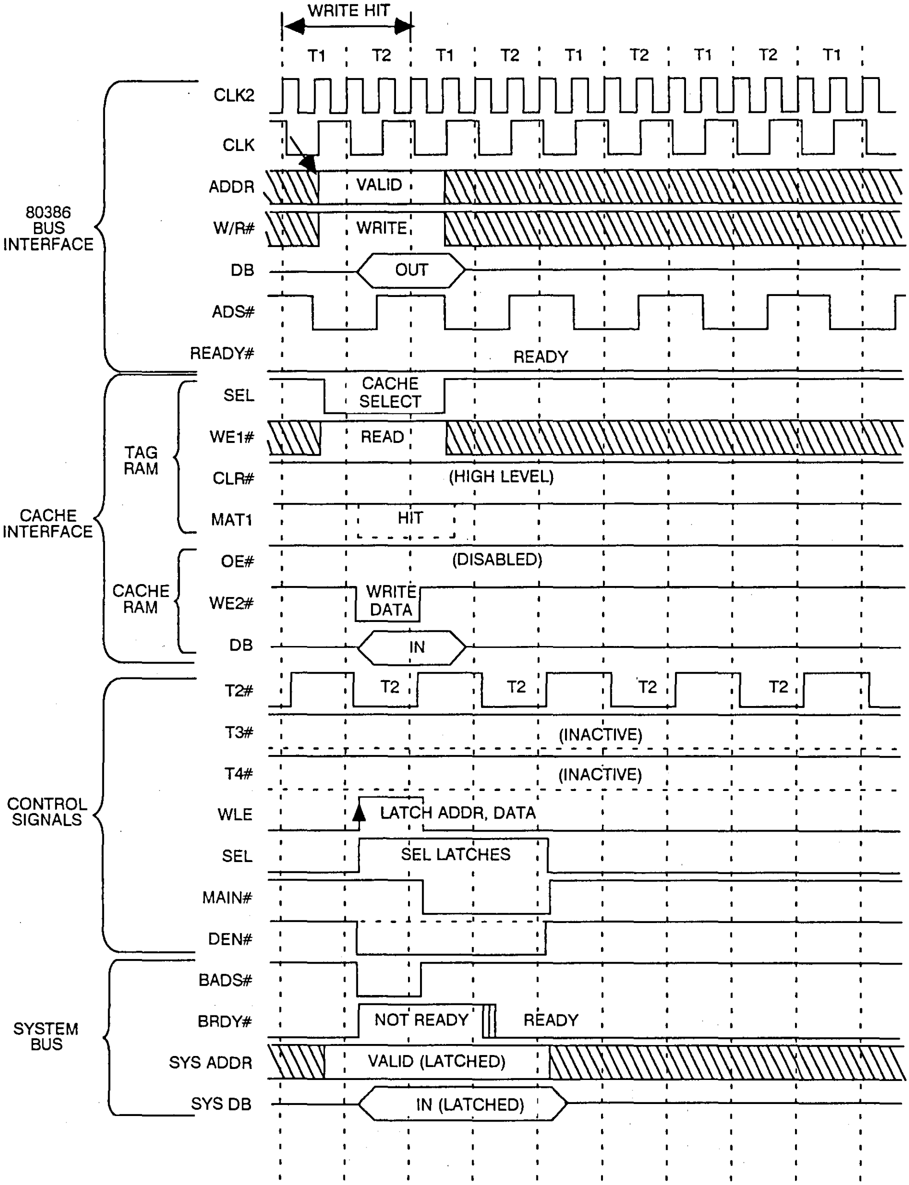


Figure 18. Write Hit Timing

WRITE MISS TIMING

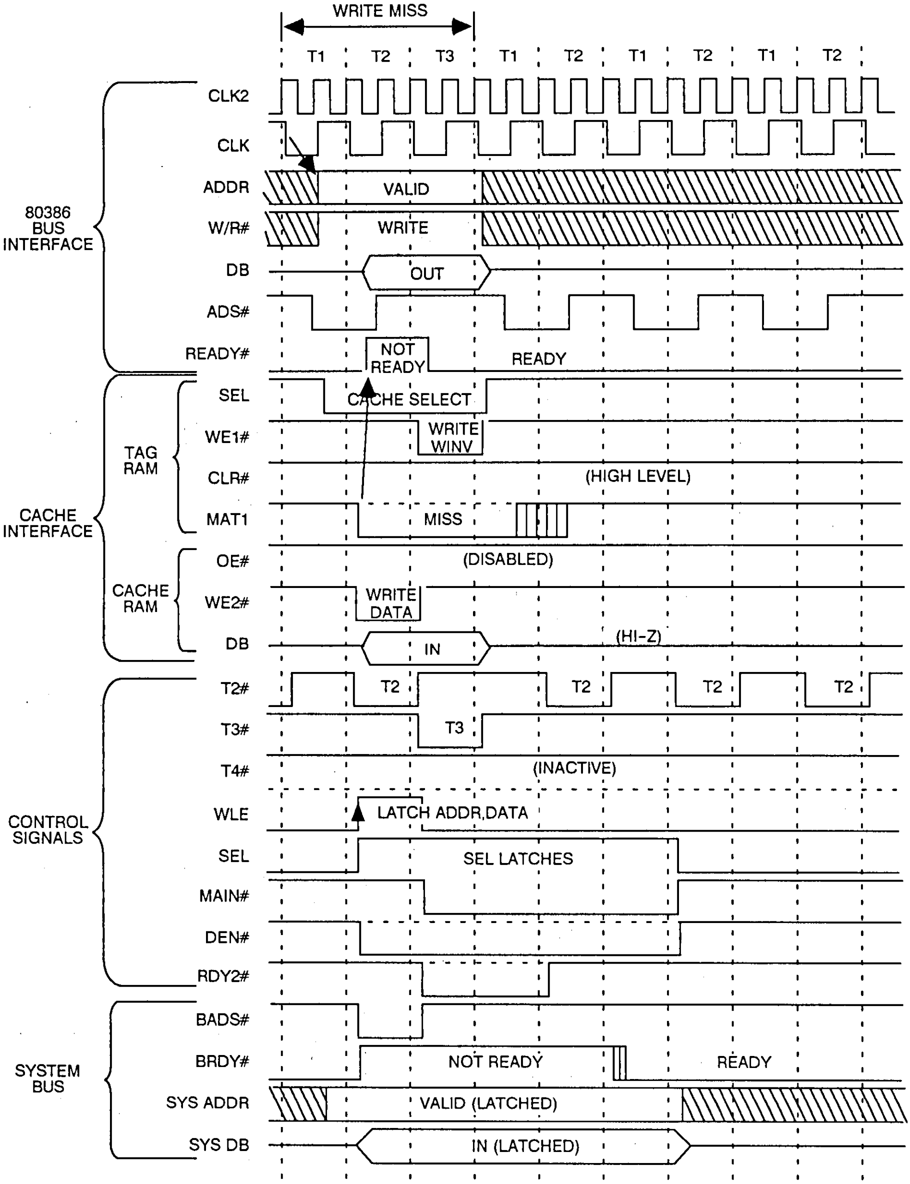


Figure 19. Write Miss Timing

READ LBA TIMING

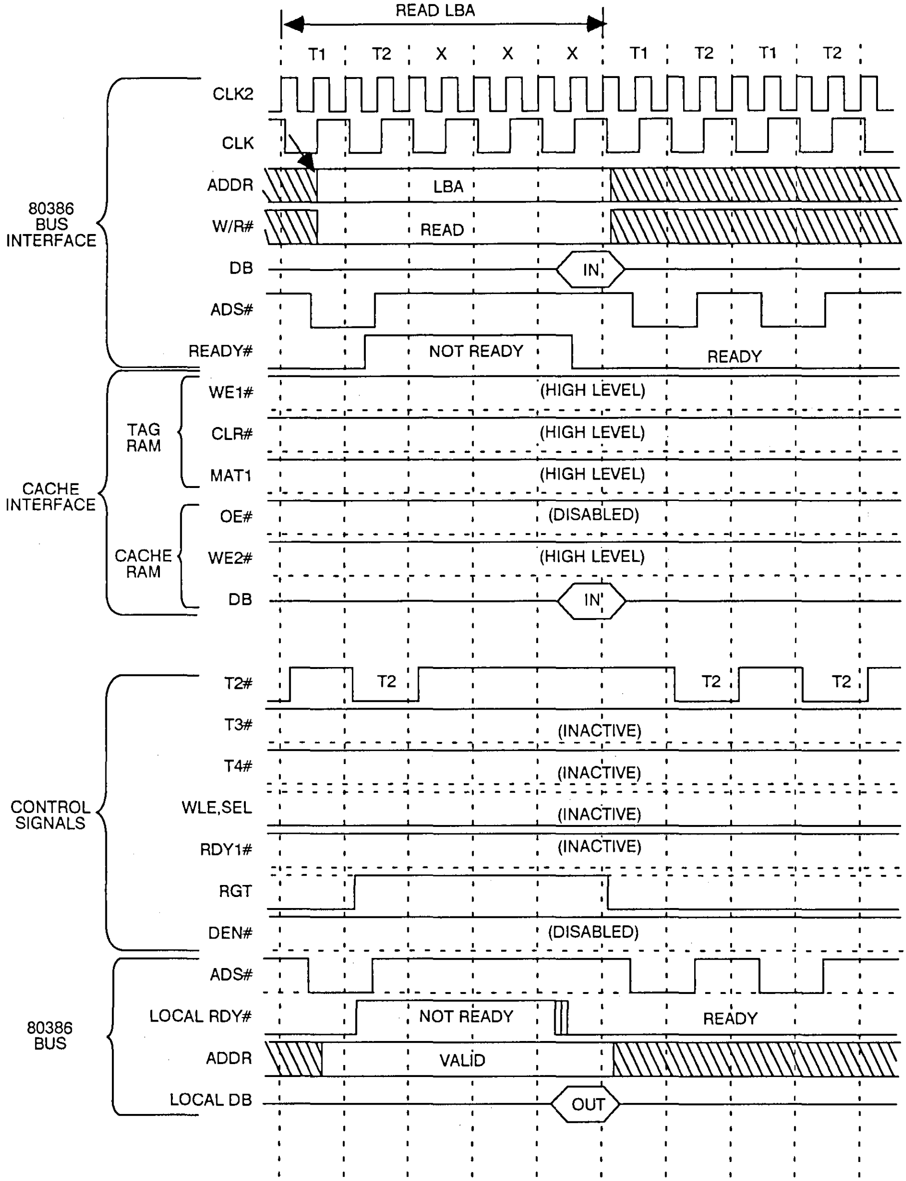


Figure 20. Read Local Bus Access Timing

WRITE LBA TIMING

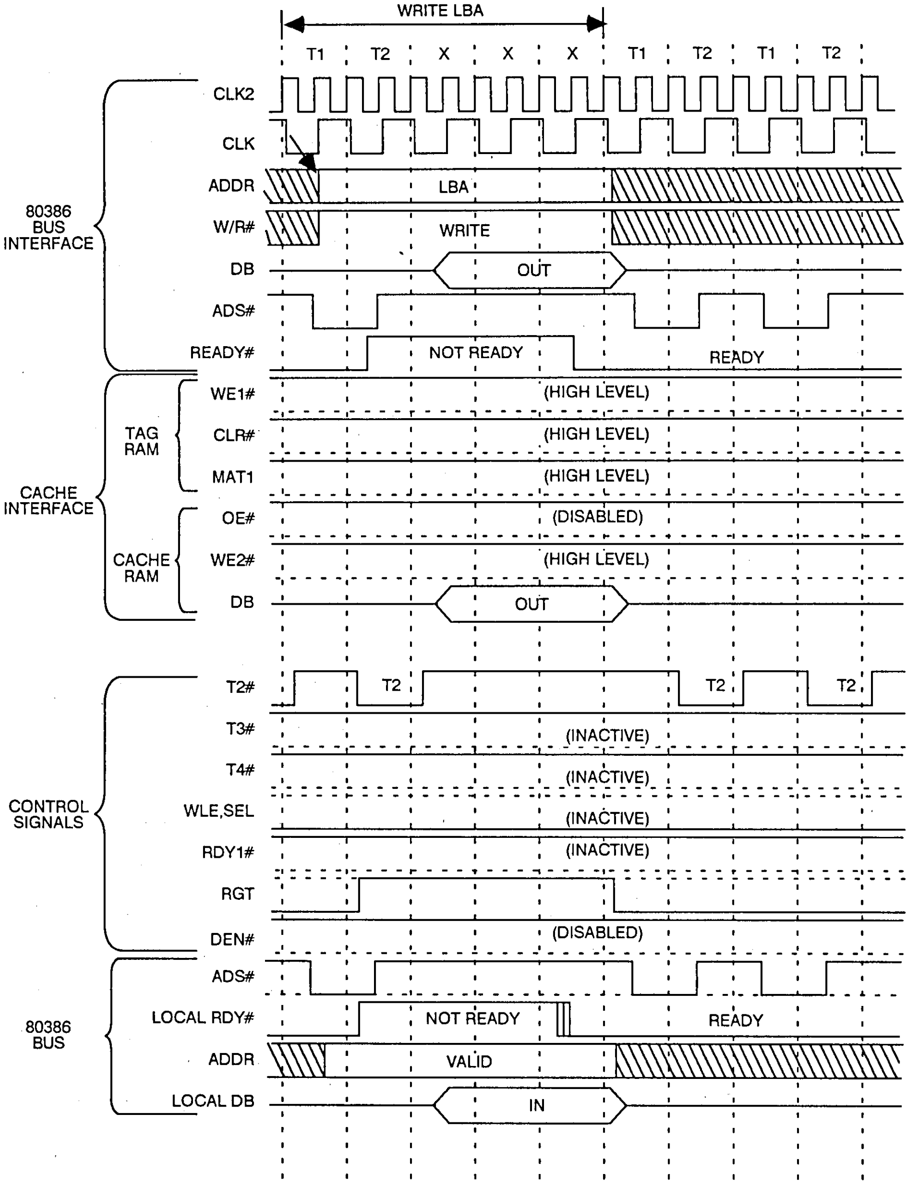


Figure 21. Write Local Bus Access Timing

READ NCA TIMING

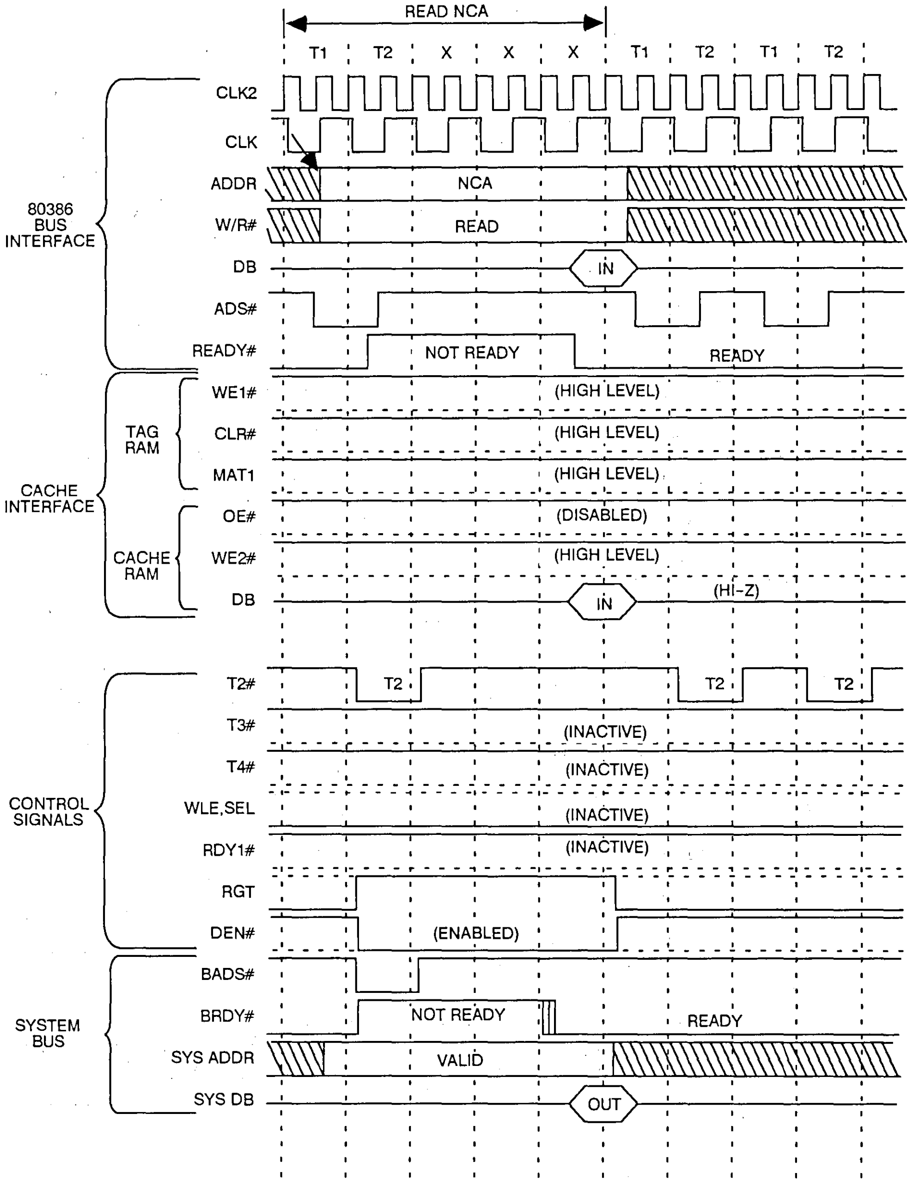


Figure 22. Read Non-Cached Addresse Timing

WRITE NCA TIMING

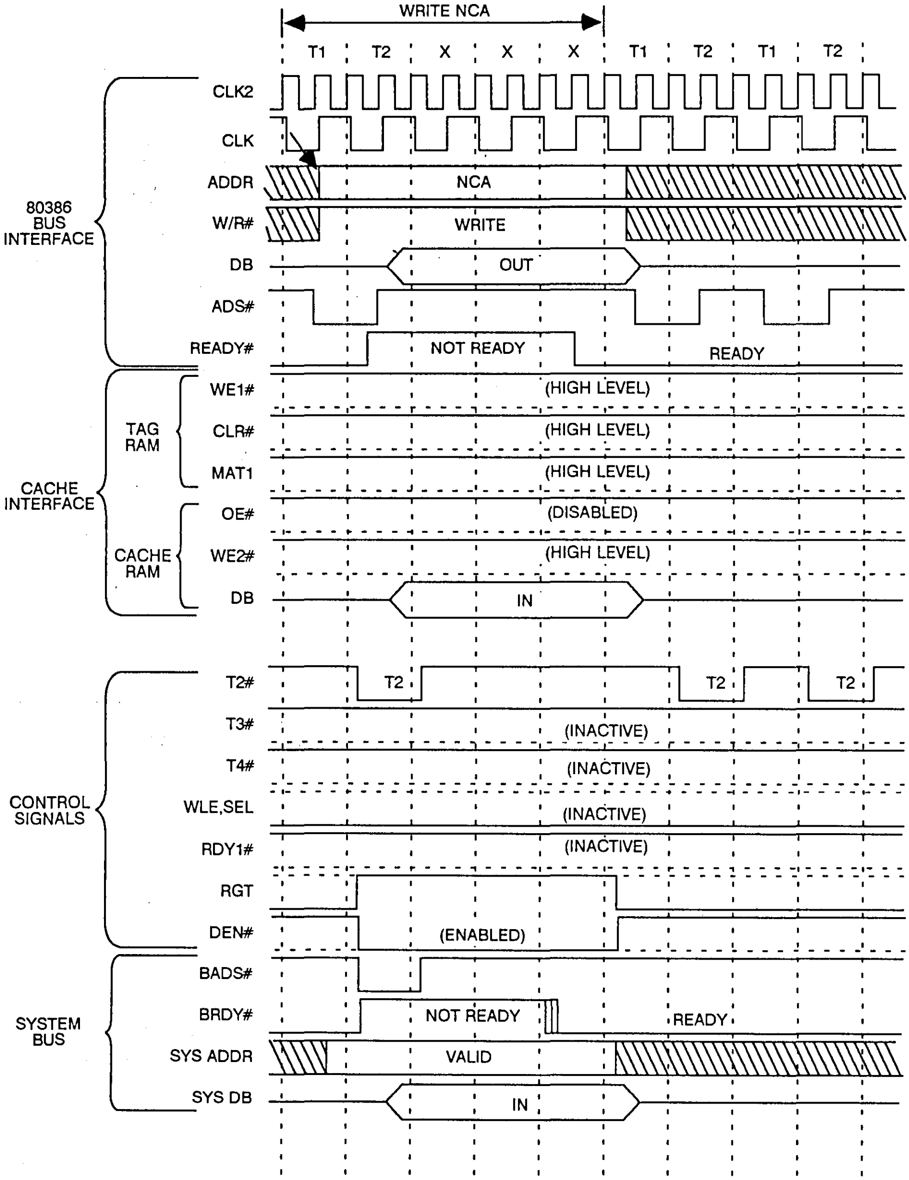


Figure 23. Write Non-Cached Addresse Timing

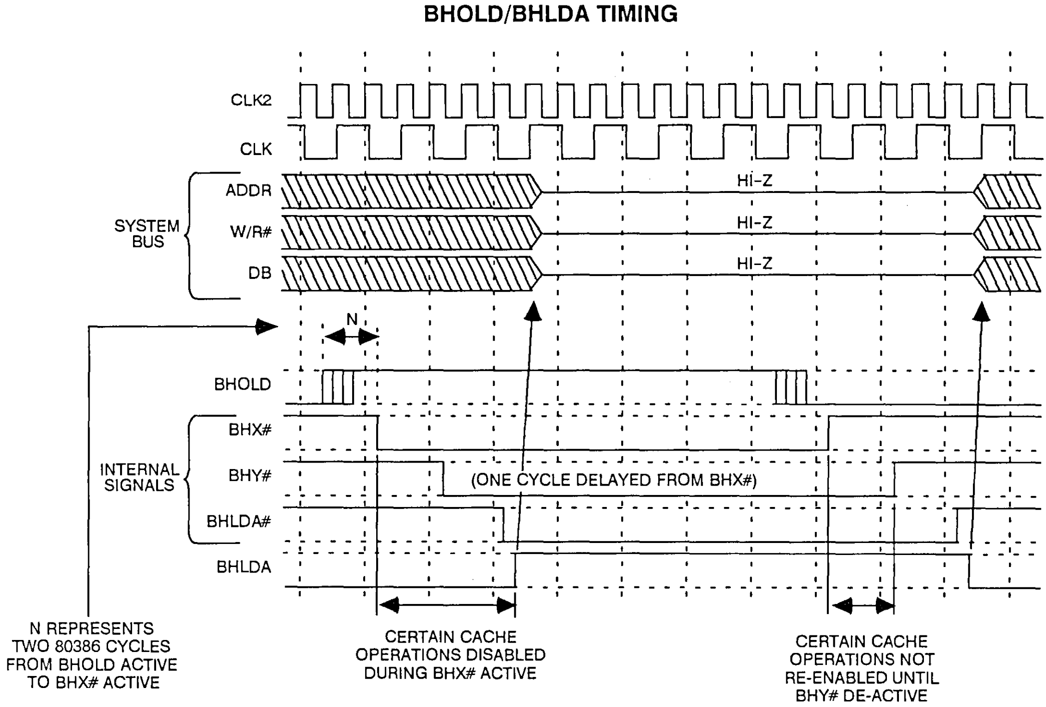
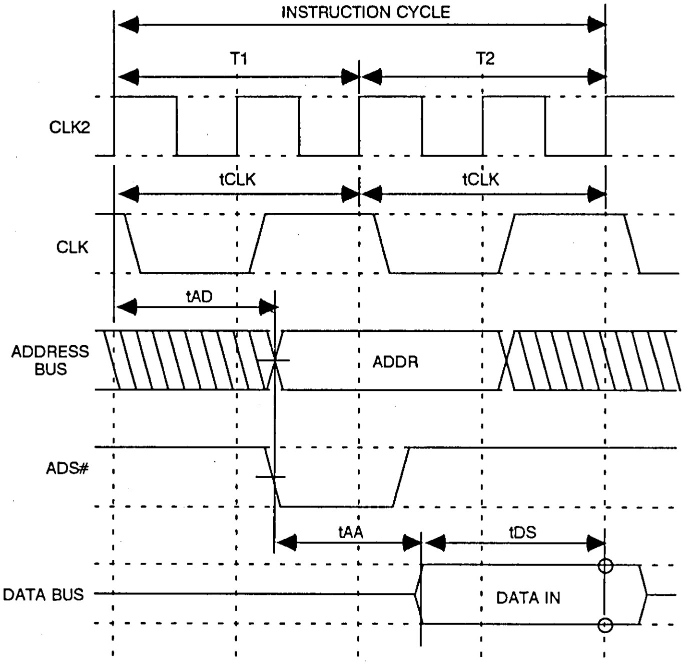


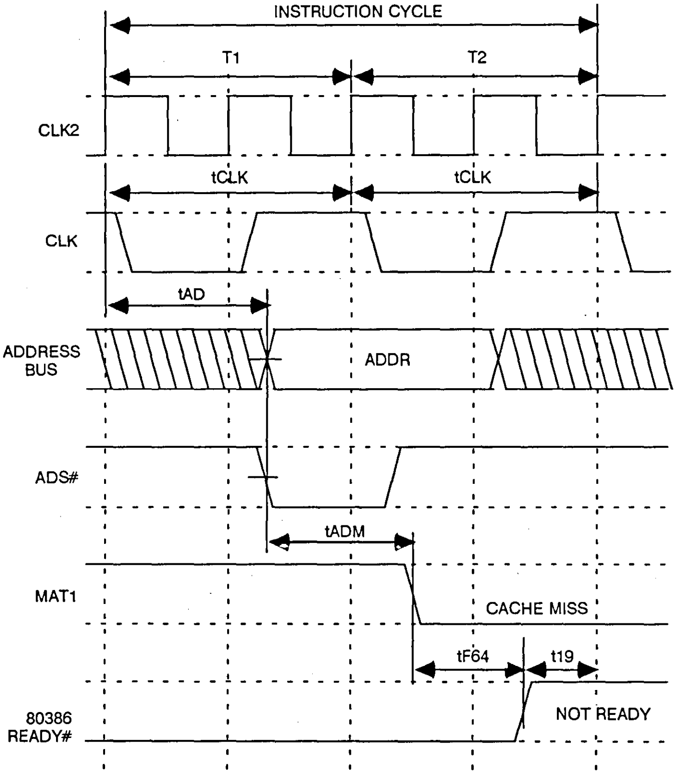
Figure 24. Hold and Hold Acknowledge Timing



SPEC ANALYSIS

Parameters	80386 Clock Rate			Units
	16MHz	20MHz	25MHz	
tCLK	62	50	40	ns
tAD	40	35	30	ns
tDS	10	10	5	ns
tAA	72	55	45	ns

Figure 25. Cache Memory Timing



SPEC ANALYSIS

Parameters	80386 Clock Rate			Units
	16MHz	20MHz	25MHz	
tCLK	62	50	40	ns
tAD	40	35	30	ns
tADM	58	48	34	ns
tF64	6	6	6	ns
t19	20	11	10	ns

Figure 26. Cache Tag and SNOOP Timing

Top Level Diagram Description and Operation

Figure 27 illustrates the top level diagram of the cache controller and memory module. The block CRAM is the cache memory, TRAM is the cache tag for the local bus, SNOOP is the cache tag for the system bus (SNOOP tag), and CTRL is a PAL based state machine which controls the timing and state sequences for interfacing to; the cache memory; the SNOOP and local cache tags; and the system and microprocessor buses.

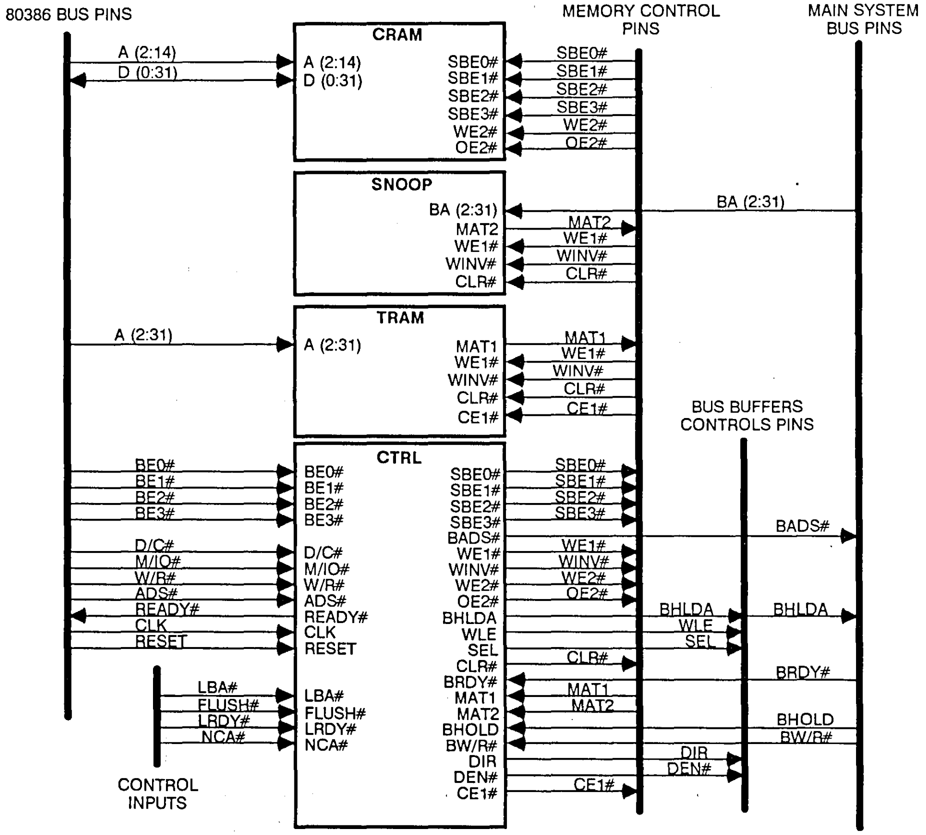


Figure 17. Top Level Diagram of the Cache Controller Module

TRAM Block

Figure 28 represents the connections of the local address bus (80386 address bus) to the cache tag SRAM (CRAM). A(2:31) are the address lines which come directly from the 80386 address bus. The cache tag is addressed using address bus bits A(2) through A(14). A(15) through A(31) are the address bits that are recorded in the memory of the cache tag. MAT1 is an input to the cache controller indicating a hit or a miss.

CE#1, WE#1, CLR# and WINV# are control signals which come from the CTRL block (the internal PALs) to the cache tag. WINV# is used to invalidate a write entry in the cache. For instance, for an 80386 write cycle, the controller will start to write data to the cache and main memory at the same time. However, if it is determined later on in the cycle that a write miss occurred, the WINV# signal will write a logic low in the 24th bit of the tag which invalidates the tag address at the cache's page offset location. CE#1 is used to keep non-cacheable addresses from entering the tag. If a non-cacheable address is detected (via the NCA# input), CE#1 will be disabled which in turn floats the IDT7174 cache tag's I/Os. The CLR# signal is an input signal to the tag and the SNOOP and is used to flush the cache on SNOOP hits.

CRAM Block

Figure 28 illustrates the cache memory which is used to store the associated data of the tag addresses. The cache memory consists of four IDT7164 8K x 8 SRAMs. A(2:14) are the same address lines that address the cache tag memory of Figure 27 i.e. the microprocessor address bus. D(0:31) is the 32 bit data bus of the 80386. The data bus is divided into 4 bytes with each byte being stored in a unique IDT7164 SRAM.

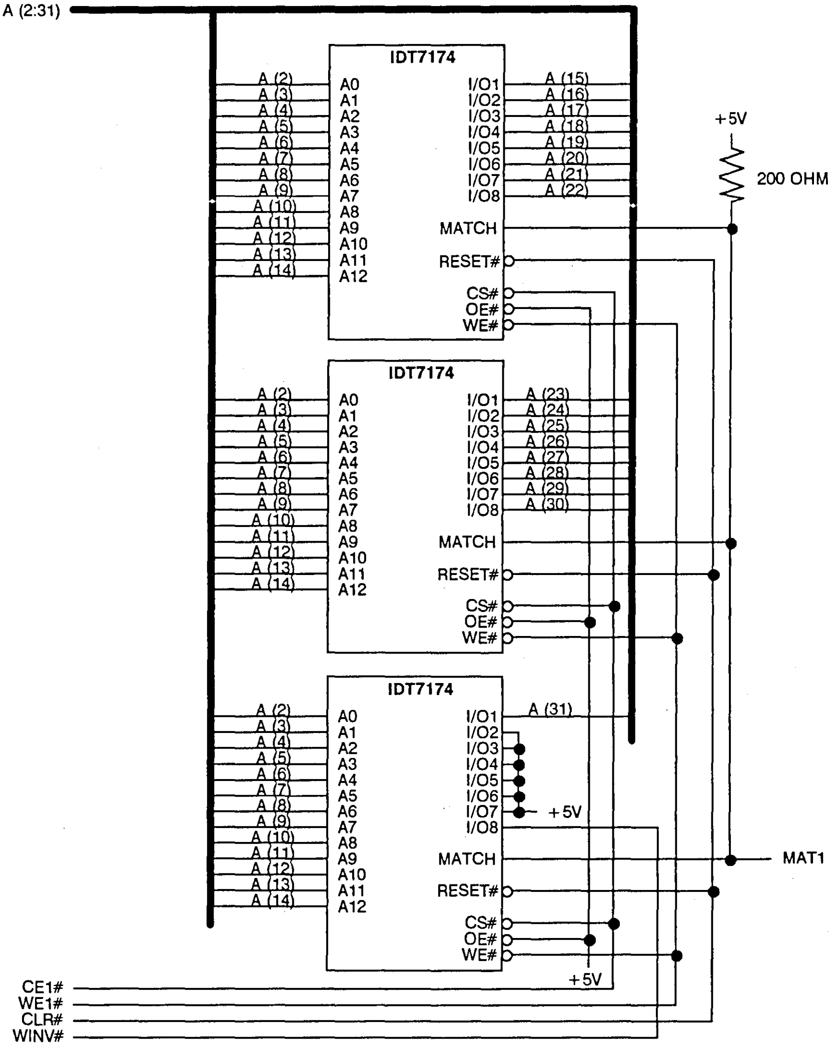


Figure 28. Cache Tag Block (TRAM)

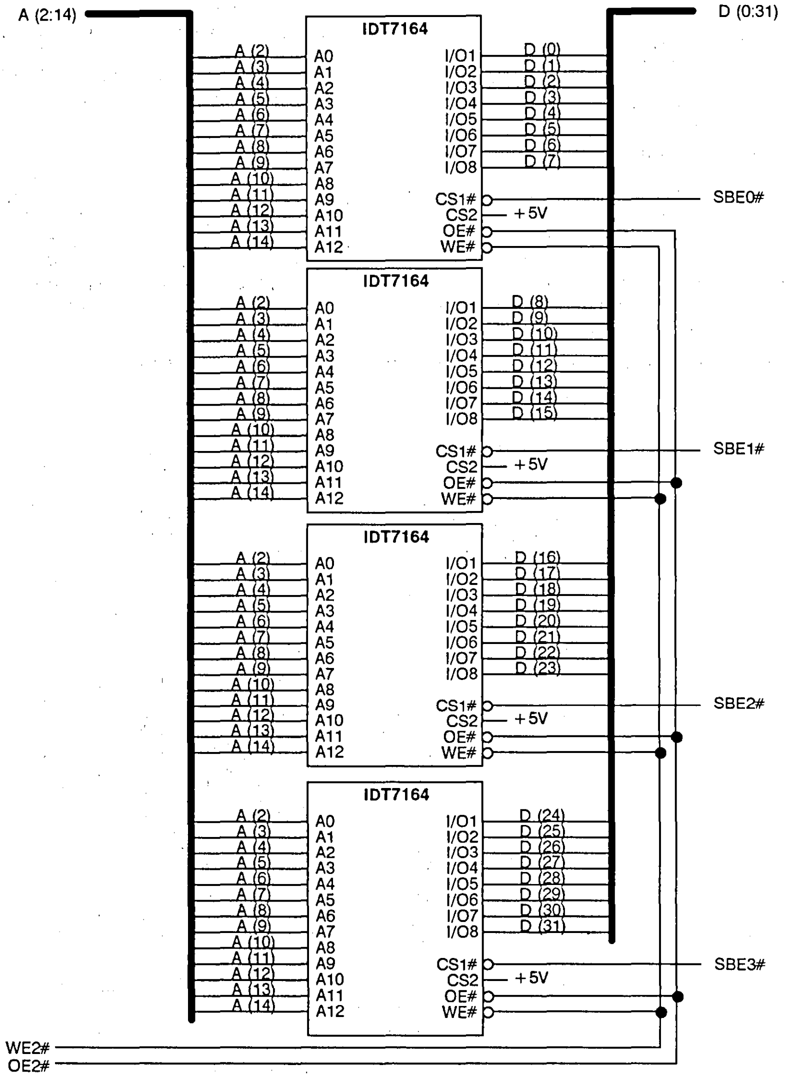


Figure 29. Cache Memory Block (CRAM)

SBE(0#:3#), WE2#, and OE2# are signals generated by the CTRL block (Figure 34) which control the operation of the cache memory. SBE (0#:3#) are used to select a specific byte of the 32-bit doubleword via their direct connection to the IDT7164s. In the case of a read miss, if the microprocessor wants to read just one byte instead of the full 32-bit doubleword, the controller will update the entire 32-bit double word in the data cache (so as to ensure valid data in the cache). In order to update the full 32-bit doubleword, the force byte enable signal, FBE#, is gated with the byte enable signals, BE(0#:3#), of the 80386 to form SBE(0#:3#) as shown in Figure 34. WE2# and OE2#, from the CTRL block, are used to control the read and write operation of the cache memory.

SNOOP Block

The SNOOP (Figure 30) is very similar to the tag. BA(2:31), the system address bus, is the main memory address bus that the SNOOP monitors. BA(2:14) is used to address the SNOOP and BA(15:30) is the address recorded in the SNOOP. As mentioned previously, the design of the controller module is such that the SNOOP and the tag always contain the same information.

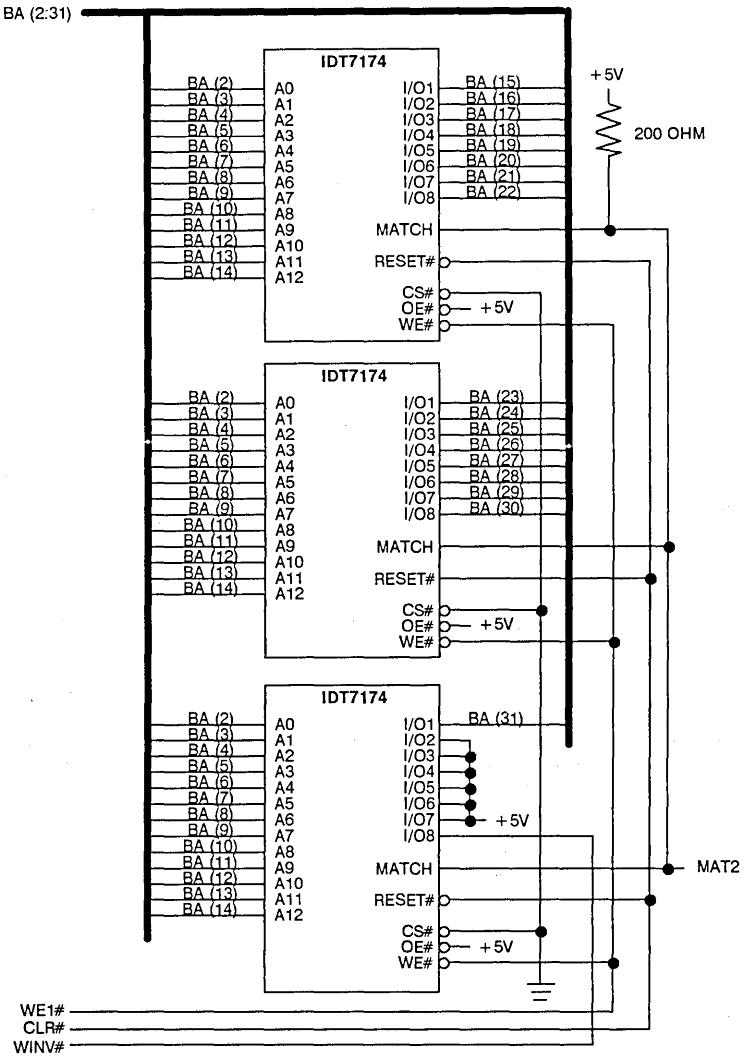


Figure 30. SNOOP Block (SNOOP)

The WINV#, CLR# and WE1# signals are used in the exact same way as the tag memory of Figure 28. Functionally the only difference between the tag memory and the SNOOP memory is the fact that the SNOOP memory is always monitoring the main memory address bus.

The only output of the SNOOP block is MAT2 which ties directly to the control block to indicate a SNOOP hit or miss. On a SNOOP hit, the cache controller will flush the entire contents of the tag (TRAM) and the SNOOP tag via the clear line (CLR#).

Posted Write Logic Design and Operation

The posted write logic comes into action when a write occurs. For the posted write operation, the IDT74FCT646 octal transceiver registers are controlled by the WLE (write latch enable), signal. The WLE line, on a microprocessor to memory write, latches the data and its address into the 646s and continue on without wait states while the cache control logic downloads the posted write buffer to main memory (the posted write operation can not be interrupted by an external system bus request i.e. it is locked). In a case where two write miss cycles occur back to back, the 80386 will have a number of wait states depending on the main memory access time.

For a write hit, the timing (Figure 18) is the same as that of the read hit (Figure 16). For a write miss however, the bus cycle is extended by an extra clock period (Figure 19).

Design of the Cache Controller Block (CTRL)

The design of the cache controller requires determining the state machine cycles of the 80386 and replicating them through a PAL based state machine. For this design, three 22V10 PALs were used (Figure 32) to form the PALs block of the controller in Figure 31.

As shown in Figure 31, the READY# input is generated by the use of the 74F64. For Figure 31, it should also be noted that all inputs to the PALs block are on the left side, all outputs are on the right side and buses are represented as dark vertical lines. For Figure 32 it should be noted that the pin out are shown for 28-Lead PLCC packages.

The designer **should use caution if he plans to implement the PAL design** given in this application note. In particular, the pin assignment should not be changed. This is because the internal structure of the PALs may not accommodate a term swap between pins. For example, if the signals WINV# and DIR of PAL1 (Figure 32) were interchanged (WINV# to pin 19 and DIR to pin 17), the JEDEC fuse map will not run because pin 17 does not have enough inputs (internally) to handle the equations for DIR.

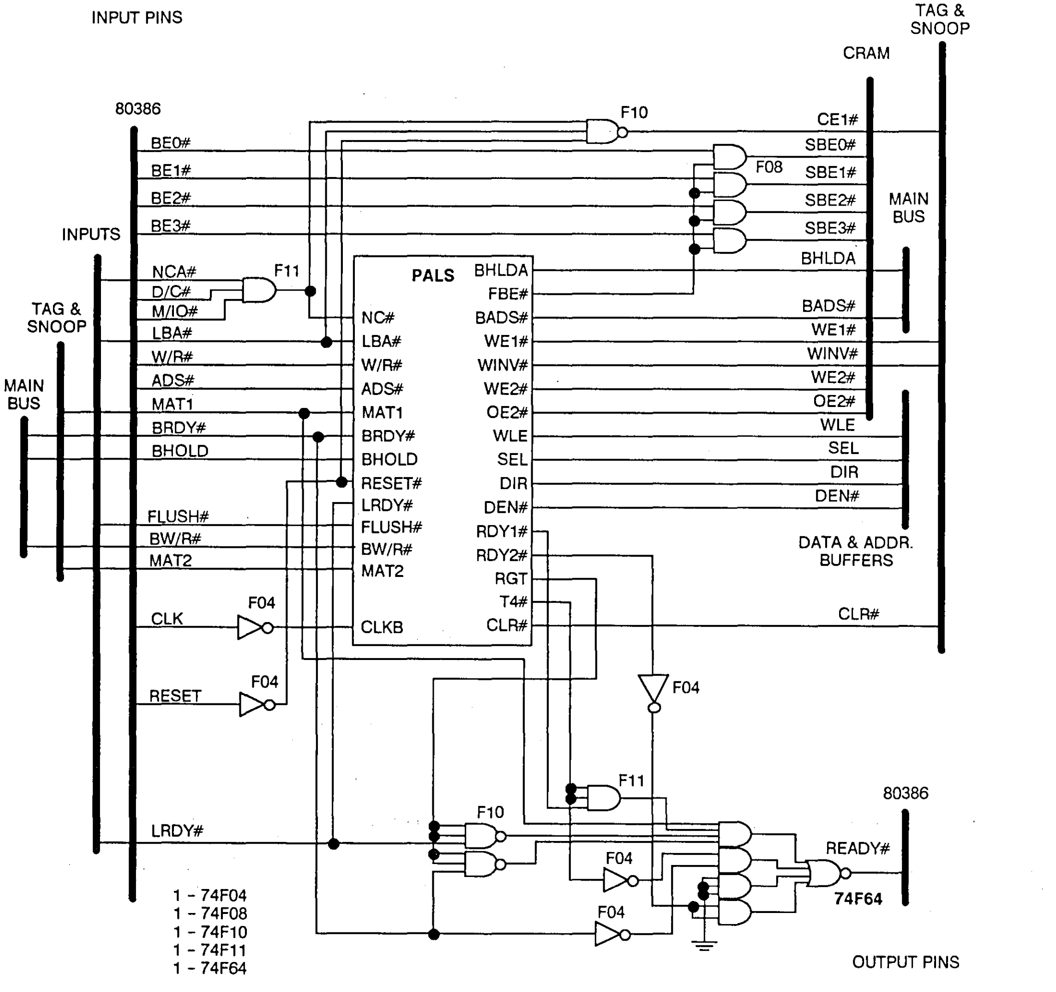
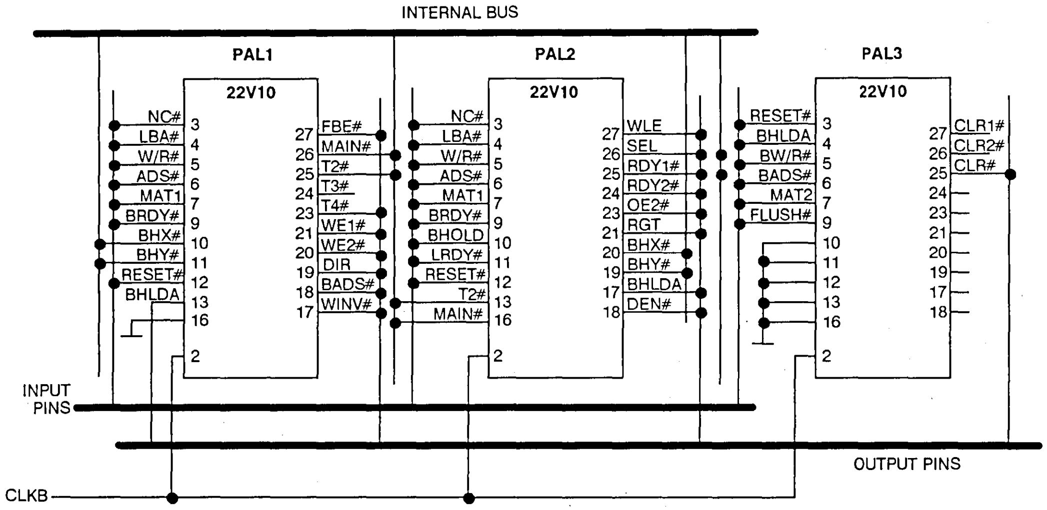


Figure 31. The Controller Block (CTRL)



PINS ARE FOR 28-LEAD PLCC PACKAGES.

Figure 32. The PALs of the CTRL Block

PAL Equations

The equations for the three PALS are presented in Tables 2 through 6. The PALASM source code for the PALs is also given for generating the corresponding JEDEC fuse map.

SIGNAL NAME	INPUTS											INTERNALS										DESCRIPTION
	NC#	LBA#	W/R#	ADS#	MAT1	BRDY#	BHX#	BHY#	BHLDA		RESET#	T2#	T3#	T4#	MAIN#	FBE#	DIR					
FBE#	H	H	L		L			H			H	L			H	H						Read Miss, no Main
	H	H	L		L	L	H				H	L			L	H						Read Miss, Main
						H					H					L						Stay until Ready
MAIN#	H	H	H					H			H	L			H							Write
	H	H	L		L			H			H	L			H							Read Miss, no Main
	H	H	L		L	L	H				H	L			L							Read Miss, Main
						H					H				L							Stay until Ready
T2#				L							H											ADS
	H	H	L		L	H					H	L			L							Stay if Rd Miss, not Rdy
	H	H	H								H	L			L							Stay if Write, Main
	L	H									H	L			L							Stay if NCA, Main
	H	H	L		L			L			H	L										Stay if Read Miss, BHOLD
	H	H	H					L			H	L										Stay if Write, BHOLD
T3#	H	H	L		L			H			H	L			H							T2,Rd Miss, no Main
	H	H	L		L	L	H				H	L			L							T2,Rd Miss, Main
	H	H	H		L			H			H	L			H							T2,Wr Miss, no Main
T4#	H	H	L								H		L									T3, Read
						H					H			L								Stay until Ready

Table 2. First Part of PAL1's Equations

Tables 2 and 3 show the equations for PAL1. A horizontal line in these tables means an AND function between the present terms.

The lines grouped together for a signal are ORed vertically. As an example, the logic equation defining the signal FBE# is as follows:

$$
\begin{aligned}
\mathrm{FBE\#} = {} & \mathrm{NC\#} \bullet \mathrm{LBA\#} \bullet \overline{\mathrm{W/R\#}} \bullet \overline{\mathrm{MAT1}} \bullet \mathrm{BHY\#} \bullet \mathrm{RESET\#} \bullet \overline{\mathrm{T2\#}} \bullet \mathrm{MAIN\#} \bullet \mathrm{FBE\#} \\
& + \\
& \mathrm{NC\#} \bullet \mathrm{LBA\#} \bullet \overline{\mathrm{W/R\#}} \bullet \overline{\mathrm{MAT1}} \bullet \overline{\mathrm{BRDY\#}} \bullet \mathrm{BHX\#} \bullet \mathrm{RESET\#} \bullet \overline{\mathrm{T2\#}} \bullet \overline{\mathrm{MAIN\#}} \bullet \mathrm{FBE\#} \\
& + \\
& \mathrm{BRDY\#} \bullet \mathrm{RESET\#} \bullet \overline{\mathrm{FBE\#}}
\end{aligned}
$$

Bared signal = logic low level
Unbared signal = logic high level

Each line is accompanied on the right hand side by a short comment describing the situation to which it relates.

SIGNAL NAME	INPUTS											INTERNALS										DESCRIPTION
	NC#	LBA#	W/R#	ADS#	MAT1	BRDY#	BHX#	BHY#	BHLDA		RESET#	T2#	T3#	T4#	MAIN#	FBE#	DIR					
WE1#	H	H	H		L			H			H	L			H							Write Miss, no Main
	H	H	L		L						H		L									Read Miss
	H	H	L			H					H			L	L							Stay until Rd Miss, Ready
WE2#	H	H	H	L							H				H							Write, ADS
	H	H	L		L						H		L									Read Miss
	H	H	L			H					H			L	L							Stay until Rd Miss, Ready
WINV#	H	H	H		L			H			H	L			H							Write Miss, no Main
BADS#	H	H	L		L		H	H			H	L			H							Read Miss, no Main
	H	H	L		L	L	H				H	L			L							Read Miss, Main
	L	H		L			H				H				H							NCA, no Main
	L	H				L	H				H				L							NCA,wait for Main
	L	H					H	L			H				H							NCA, after BHOLD
	H	H	H	L			H	H			H				H							Write, no Main
	H	H	H			L	H				H				L							Write, wait for Main
	H	H	H			L	H	L			H				H							Write, after BHOLD
DIR		H	H	L			H				H				H							Write, no Main
		H	H			L	H				H				L							Write, wait for Main
						H			L		H						H					Stay until Ready (no BH)
		H	H					L			H	L					H					Stay until BHOLD
		H	H			L	H	L			H				H		L					Write, after BHOLD

Table 3. Second Part of PAL1's Equations

SIGNAL NAME	INPUTS												INTERNALS								DESCRIPTION
	NC#	LBA#	W/R#	ADS#	MAT1	BRDY#	BHOLD	LRDY#	T2#	MAIN#		RESET#	BHX#	BHY#	RDY1#	RGT	BHLDA	SEL	DEN#	RDY2#	
WLE	H	H	H	L						H		H									Write, no Main
	H	H	H			L				L		H									Write, wait for Main
SEL	H	H	H	L						H		H									Write, no Main
	H	H	H			L				L		H									Write, wait for Main
						H						H					L	H			Stay until Ready (no BH)
	H	H	H						L			H		L				H			Stay until BHOLD
RDY1#	H	H	H	L		H				L		H	H								Write while Main
						H				L		H			L						Stay until Ready
	H	H	H	L								H	L								Write while BHOLD
												H		L	L						Stay until released
	L	H				H				L		H	H								NCA, Main
	L	H		L								H	L								NCA while BHOLD
	L	H							L			H		L							NCA while BHOLD
RDY2#	H	H	H		L				L	H		H	H	H							T2,Wr Miss, no Main
				H								H								L	Stay until next ADS#
OE2#	H	H	L	L	H							H									Read Hit

Table 4. First Part of PAL2's Equations

SIGNAL NAME	INPUTS												INTERNALS								DESCRIPTION
	NC#	LBA#	W/R#	ADS#	MAT1	BRDY#	BHOLD	LRDY#	T2#	MAIN#		RESET#	BHX#	BHY#	RDY1#	RGT	BHLDA	SEL	DEN#		
RGT	L	H		L		L				H		H	H			L					NCA, not Busy
	L	H										H	H	L		L					NCA after BHOLD
	L	H				L			L	L		H	H			L					NCA, wait for Main
		L		L								H				L					LBA
		H				H						H				H					Stay NCA until Ready
		L						H				H				H					Stay LBA until Ready
BHX#							H		L	H		H	H								BHOLD, no Main
						L	H		L	L		H	H								BHOLD, Main
							H					H	L								Stay until no BHOLD
BHY#												H	L								One cycle after BHX
BHLDA						L	H					H		L			L				BHY when Ready
							H					H					H				Stay until no BHOLD
DEN#	H	H	L		L				L	H		H		H					H		Read Miss, no Main
	H	H	L		L	L				L		H									Read Miss, wait for Main
		H	H	L						H		H	H								Write, no Main
		H	H			L				L		H	H								Write, wait for Main
	L	H	L	L						H		H		H					H		Read NCA, no Main
	L	H	L			L				L		H									Read NCA, wait for Main
						H						H							L		Stay until Ready
		H	H			L				H		H	H	L					H		Write, after BHOLD
	L	H				L				H		H	H	L					H		NCA, after BHOLD

Table 5. Second Part of PAL2's Equations

SIGNAL NAME	INPUTS						INTERNALS		DESCRIPTION
	RESET#	BHLDA	BW/R#	MATA2	BADS#	FLUSH#	CLR1#	CLR2#	
CLR1#	H	H	H		L				Snoop Write while BHLDA
CLR2#	H			H			L		Write Hit while BHLDA
CLR#	H			H			L		Write Hit while BHLDA
	H							L	Stay one more cycle
	H					L			External FLUSH
	L								System RESET

Table 6. PAL3's Equations

These equations were developed by closely analyzing the logical timing diagrams for the 80386 under all the possible states. A combination of several of these states following each other were also looked at. The timing waveforms for the controller were then developed in order to meet its specifications and handle the 80386 operations. Once the timing waveforms were done then the equations were derived and the PALs programed.

The software PALASM was used to compile the equations for the PALs into their corresponding JEDEC fuse map. The source code for each PAL's program is presented below. The nomenclature in PALASM is somewhat deceptive in that an apparently logical "high" term might mean a logical "low". In the pin declaration part of the source code an active low signal is represented by a "/" preceding its name. In the description of the equations, however, if a term is written as it was declared (in the pin declaration) it will be perceived as a logic high, yet if the signal is written in the opposite sense than in the declaration then PALASM understands it as a logic low.

Keeping the above in mind, it will become clear to the reader how Tables 2 through 6 match their respective PAL code.

```
TITLE           Controller1
PATTERN         N.A.
REVISION        1.1
AUTHOR
COMPANY         Integrated Device Technology Inc.
DATE            09-21-1988

CHIP CONTROL_PAL1 PAL22V10

;PINS
;1    2    3    4    5    6    7    8    9    10
CLKB /XNC /LBA /W_R /ADS MAT1 /BRDY /BHX /BHY /RESET
;11    12    13  14    15    16   17   18   19   20
BHLDA  GND  NC  /WINV  /BADS  DIR  /WE2 /WE1 /T4  /T3
;21  22     23    24   25
/T2 /MAIN  /FBE   VCC  GLOBAL

EQUATIONS

GLOBAL.RSTF  = RESET

DIR     := /BHX * /LBA * /W_R * ADS * /RESET * /MAIN
         +
         /BHX * /LBA * /W_R * BRDY * /RESET * MAIN
         +
         /BRDY * /BHLDA * /RESET * DIR
         +
         /LBA * /W_R * BHY * /RESET * T2 * DIR
         +
         /LBA * /W_R * BRDY * /BHX * BHY * /RESET * /MAIN *
         /DIR
FBE     := /XNC * /LBA * W_R * /MAT1 * /BHY * /RESET * T2 *
         /MAIN */FBE
         +
         /XNC * /LBA * W_R * /MAT1 * BRDY * /BHX * /RESET *
         T2 * MAIN * /FBE
         +
         /BRDY * /RESET * FBE
MAIN    := /XNC * /LBA * /W_R * /BHY * /RESET * T2 * /MAIN
         +
         /XNC * /LBA * W_R * /MAT1 * /BHY * /RESET * T2 *
         /MAIN
         +
         /XNC * /LBA * W_R * /MAT1 * BRDY * /BHX * /RESET *
         T2 * MAIN
         +
         /BRDY * /RESET * MAIN
T2      := ADS * /RESET
         +
         /XNC * /LBA * W_R * /MAT1 * /BRDY * /RESET * T2 *
         MAIN
         +
         /XNC * /LBA * /W_R * /RESET * T2 * MAIN
         +
         XNC * /LBA * /RESET * T2 * MAIN
         +
         /XNC * /LBA * W_R * /MAT1 * BHY * /RESET * T2
         +
         /XNC * /LBA * /W_R * BHY * /RESET * T2
T3      := /XNC * /LBA * W_R * /MAT1 * /BHY * /RESET * T2 *
         /MAIN
         +
         /XNC * /LBA * W_R * /MAT1 * BRDY * /BHX * /RESET *
         T2 * MAIN
         +
         /XNC * /LBA * /W_R * /MAT1 * /BHY * /RESET * T2 *
         /MAIN
T4      := /XNC * /LBA * W_R * /RESET * T3
         +
         BRDY * /RESET * T4
WE1     := /XNC * /LBA * /W_R * /MAT1 * /BHY * /RESET * T2 *
         /MAIN
         +
         /XNC * /LBA * W_R * /MAT1 * /RESET * T3
         +
         /XNC * /LBA * W_R * /BRDY * /RESET * T4 * MAIN
WE2     := /XNC * /LBA * /W_R * ADS * /RESET * /MAIN
         +
         /XNC * /LBA * W_R * /MAT1 * /RESET * T3
         +
         /XNC * /LBA * W_R * /BRDY * /RESET * T4 * MAIN
WINV    := /XNC * /LBA * /W_R * /MAT1 * /BHY * /RESET * T2 *
         /MAIN
BADS    := /XNC * /LBA * W_R * /MAT1 * /BHX * /BHY * /RESET *
         T2 * /MAIN
         +
         /XNC * /LBA * W_R * /MAT1 * BRDY * /BHX * /RESET *
         T2 * MAIN
         +
         XNC * /LBA * ADS * /BHX * /RESET * /MAIN
         +
         XNC * /LBA * BRDY * /BHX * /RESET * MAIN
         +
         XNC * /LBA * /BHX * BHY * /RESET * /MAIN
         +
         /XNC * /LBA * /W_R * ADS * /BHX * /BHY * /RESET *
         /MAIN
         +
         /XNC * /LBA * /W_R * BRDY * /BHX * /RESET * MAIN
         +
         /XNC * /LBA * /W_R * BRDY * /BHX * BHY * /RESET *
        /MAIN
```

```
TITLE           Controller2
PATTERN         N.A.
REVISION        1.1
AUTHOR
COMPANY         Integrated Device Technology Inc.
DATE            09-01-1988

CHIP CONTROL_PAL2 PAL22V10

;PINS
;1    2    3    4    5    6    7     8     9    10
CLKB /XNC /LBA /W_R /ADS MAT1 /BRDY BHOLD /LRDY
/RESET
;11  12   13    14    15   16   17   18  19   20
/T2  GND  /MAIN BHLDA /DEN /BHY /BHX RGT /OE2 /RDY2
;21    22  23  24  25
/RDY1  SEL WLE VCC GLOBAL

EQUATIONS

GLOBAL.RSTF = RESET

WLE   := /XNC * /LBA * /W_R * ADS * /MAIN * /RESET
         +
         /XNC * /LBA * /W_R * BRDY * MAIN * /RESET
SEL   := /XNC * /LBA * /W_R * ADS * /MAIN * /RESET
         +
         /XNC * /LBA * /W_R * BRDY * MAIN * /RESET
         +
         /BRDY * /RESET * /BHLDA * SEL
         +
         /XNC * /LBA * /W_R * T2 * /RESET * BHY * SEL
RDY1  := /XNC * /LBA * /W_R * ADS * /BRDY * MAIN * /RESET
         * /BHX
         +
         /BRDY * MAIN * /RESET * RDY1
         +
         /XNC * /LBA * /W_R * ADS * /RESET * BHX
         +
         /RESET * BHY * RDY1
         +
         XNC * /LBA * /BRDY * MAIN * /RESET * /BHX
         +
         XNC * /LBA * ADS * /RESET * BHX
         +
         XNC * /LBA * T2 * /RESET * BHY
RDY2  := /XNC * /LBA * /W_R * /MAT1 * T2 * /MAIN * /RESET *
         /BHX * /BHY
         +
         /ADS * /RESET * RDY2
OE2   := /XNC * /LBA * W_R * ADS * MAT1 * /RESET
RGT   := XNC * /LBA * ADS * BRDY * /MAIN * /RESET * /BHX *
         /RGT
         +
         XNC * /LBA * /RESET * /BHX * BHY * /RGT
         +
         XNC * /LBA * BRDY * T2 * MAIN * /RESET * /BHX * /RGT
         +
         LBA * ADS * /RESET * /RGT
         +
         /LBA * /BRDY * /RESET * RGT
         +
         LBA * /LRDY * /RESET * RGT
BHX   := BHOLD * T2 * /MAIN * /RESET * /BHX
         +
         BRDY * BHOLD * T2 * MAIN * /RESET * /BHX
         +
         BHOLD * /RESET * BHX
BHY   := /RESET * BHX
BHLDA := BRDY * BHOLD * /RESET * BHY * /BHLDA
         +
         BHOLD * /RESET * BHLDA
DEN   := /XNC * /LBA * W_R * /MAT1 * T2 * /MAIN * /RESET *
         /BHY * /DEN
         +
         /XNC * /LBA * W_R * /MAT1 * BRDY * MAIN * /RESET
         +
         /LBA * /W_R * ADS * /MAIN * /RESET * /BHX
         +
         /LBA * /W_R * BRDY * MAIN * /RESET * /BHX
         +
         XNC * /LBA * W_R * ADS * /MAIN * /RESET * /BHY *
         /DEN
         +
         XNC * /LBA * W_R * BRDY * MAIN * /RESET
         +
         /BRDY * /RESET * DEN
         +
         /W_R * /LBA * BRDY * /MAIN * /RESET * /BHX * BHY *
         /DEN
         +
         XNC * /LBA * BRDY * /MAIN * /RESET * /BHX * BHY *
         /DEN
```

```
TITLE           Controller3
PATTERN         N.A.
REVISION        1.0
AUTHOR          Mammad Safai
COMPANY         Integrated Device Technology Inc.
DATE            09-28-1988

CHIP CONTROL_PAL3 PAL22V10

;PINS
;1     2      3     4     5     6     7     8  9   10
CLKB /RESET BHLDA /BW_R /BADS MAT2 /FLUSH NC  NC
NC
;11  12   13   14   15   16   17   18   19   20
NC  GND  NC   NC   NC   NC   NC   NC   NC   NC
;21   22     23     24    25
/CLR  /CLR2  /CLR1  VCC   GLOBAL

EQUATIONS

GLOBAL.RSTF  = RESET

CLR1  :=     /RESET * BHLDA * /BW_R * BADS

CLR2  :=     /RESET * MAT2 * CLR1

CLR   :=     /RESET * MAT2 * CLR1
             +
             /RESET * CLR2
             +
             /RESET * FLUSH
             +
             RESET
```

CONCLUSION

The design of cache based microprocessor systems is optimized by the use of a cache controller based on a dual cache tag scheme. Such an architecture is adaptable to present day 25MHz systems as well is easily adapted to future higher speed microprocessors. Posted writes further improves the effective cycle time (with the IDT74FCT646s).

At the heart of this design is the IDT7174 cache tag SRAM. This device with an address to match time of 20ns gives a wide margin for the two cycle 80386 operating at 25MHz. Faster microprocessor can be easily accommodated without changes to this design.

Integrated Device Technology, Inc.

IDT STATIC RAMS SIMPLIFY CACHE DESIGN WITH THE 80386 AND 82385

APPLICATION NOTE AN–38

By Kelly Maas

INTRODUCTION

As greater performance is demanded of 32–bit microprocessors, cache memory systems are quickly becoming commonplace. While cache design for the Intel 80386 is made easier with the Intel 82385 and other cache controller chips, the system designer still has to make a choice of static RAMs (SRAMs) for use in the cache. The IDT71586 CacheRAM™, which includes internal address latches, is an example of an SRAM that is specifically designed to simplify cache memory design and minimize part count.

This application note gives an introduction to cache operation, then describes how a cache may be implemented for the 80386 microprocessor using the 82385 cache controller. We then discuss how to determine which fast IDT SRAM, such as the IDT71586, is best for an application. The last section explains how to double and quadruple the size of the cache memory while still using a single cache controller.

CACHE BASICS

Cache design can involve a large number of choices, although selection of the 82385 largely eliminates these. For example, one has the option of implementing separate instruction and data caches, or a single combined cache. Different methods exist for maintaining cache coherency during cache writes, including write–back and write–through. A cache may employ direct mapping or any degree of set associativity. And of course there is the choice of cache size.

A cache increases the performance of a computer by decreasing the average time it takes to access memory. Main memory is normally implemented with dynamic RAM because it offers the highest density and lowest cost. But DRAM is relatively slow and is unable to match the speeds at which high performance microprocessors can read and write memory. Because of this, the processor must spend part of each read or write cycle idly waiting on the DRAM. This keeps the high performance 80386 from realizing its full potential.

A cache is located between the processor and main memory and is used to store a portion of the main memory contents. It consists of control circuitry and a relatively small amount of fast SRAM, and permits the processor to operate at full speed most of the time. The property that allows caches to decrease the average memory access time is called locality of reference. That is, for a given period of time, the processor is likely to repeatedly access a small set of localized memory locations. By copying the items from these addresses into the cache when first accessed, most future references to these locations are directed to the cache instead of main memory.

The general operation of a cache is rather simple. When the processor makes a memory reference (a read or write), the first step is to determine if that address is cached (i.e. the data from that address currently resides in the cache). If it is, the reference is termed a hit, and otherwise a miss. This is similar to page hits and misses in a virtual memory organization. In the event of a hit, the read or write is performed in the cache without delay. When a miss occurs, the memory reference is forwarded to main memory. In this case the processor must wait because of the slower speed of main memory. Note that if main memory is fast enough to eliminate the need for wait states, there is no need for a cache. Note too that because of the time required to determine if a memory reference is a hit or a miss, the cache SRAM must be faster than the SRAM required to implement a (very expensive and impractical) zero–wait state main memory.

Since the cache is much smaller than main memory, how is it determined what data from main memory to place in the cache? Data is brought into the cache one line at a time as it is needed by the processor and removed when displaced by data from another newly referenced address. A line is the unit of data transfered from main memory to the cache during a read miss. It is typically one to four times the processor word size and is always contiguous. As the line size is increased, each read miss results in a longer memory cycle because more data is transferred from main memory to the cache. But it also increases the hit rate (the fraction of memory references that are cache hits) in most cases because data is often loaded into the cache before it is first referenced.

Along with each line of data in the cache is stored a tag. Figure 1 shows an example of a direct–mapped cache with a one–word line. The tag consists of the most significant bits of the main memory address from which the line came, and is necessary because several lines of main memory map to each line in the cache. The portion of cache memory used to store the tags is called the directory. The number of address bits in the tag is dependent on all of the various cache parameters. The deeper the cache, the shorter the tags. An additional bit is included with each tag in the directory to indicate whether or not the corresponding cache line is valid, but is not shown in Figure 1.

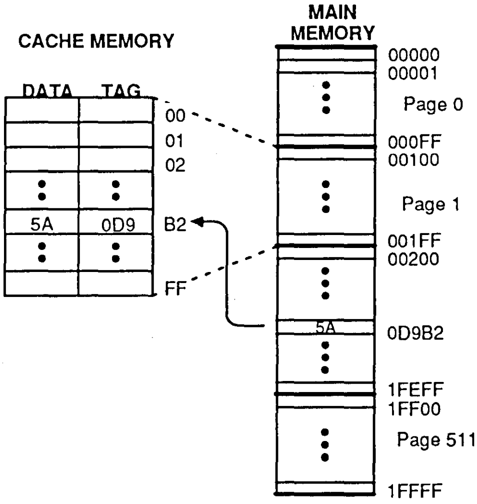


Figure 1. Basic Direct–Mapped Cache Organization

Where in the cache is a newly referenced item from main memory placed? The best performance, measured by the hit ratio, is achieved when data from any main memory location may be placed in any cache memory location. This is known as a fully associative cache and allows optimum utilization of the cache because new data can always replace the least needed data, regardless of its location.

Unfortunately, a fully associative cache is also highly impractical. Since data may be placed anywhere in the cache, the only way to determine if a given address is cached is to compare it with every tag in the cache. This would require a very large amount of circuitry and would be too slow. Additional circuitry would also be necessary to implement the replacement algorithm, which determines which line in the cache is best to remove to make room for new data.

The opposite extreme to the associative cache is the direct–mapped cache. In this case each main memory address is mapped to a single cache address using the least significant address bits. Figure 1 shows how a 128K word main memory and a 256 word direct–mapped cache are organized. The memory may be viewed as a number of pages, each the size of the cache. In this example there are (128K / 256 =) 512 pages. The offset of an address within a page determines its cache address, and the page number becomes the tag. It should be remembered that addresses are cached individually and that the cache usually contains data from several different pages at any given time. The direct–mapped cache gives inferior performance (in virtually all cases) because it is impossible to simultaneously cache two main memory locations whose least significant address bits (page offsets) are identical. The main advantages of a direct–mapped cache are simplicity and speed, since only one tag need be compared to determine if the reference is a hit or a miss.

Most caches employ an alternative to direct–mapping called set associativity. It offers some of the performance benefits of an associative cache without the extreme complexity. In 4–way set associativity, for example, the cache memory is divided into four identical banks. Much like direct–mapping, the least significant bits are used to map the main memory address into the cache. But instead of mapping into a single location in a single block, it maps into the same location in each of the four blocks. Set associativity reduces the problem of simultaneously caching multiple main memory addresses with identical page offsets since there are now multiple pages (blocks) in the cache. The arrangement of a 256 word, 4–way set associative cache and a 128K word main memory are shown in Figure 2. Compared with the same size direct–mapped cache, a set associative cache has smaller pages and banks, but more of them. Note that direct–mapped is the same as 1–way set associative.

For a 4–way set associative cache, a hit or miss is determined by simultaneously comparing the most significant bits of the address with the tag from the appropriate line in each block. A match in any of the blocks is deemed a hit, and the read or write is performed at that block of the cache. Since new cache entries can be written to any of the four banks, a replacement algorithm is used to determine which one. A frequently used algorithm is to replace the entry that is LRU (least recntly used). Also common are 2–way and 8–way set associative caches. As the degree of set associativity increases, so too does the hit rate, the cache complexity and the time required to compare addresses with tags.

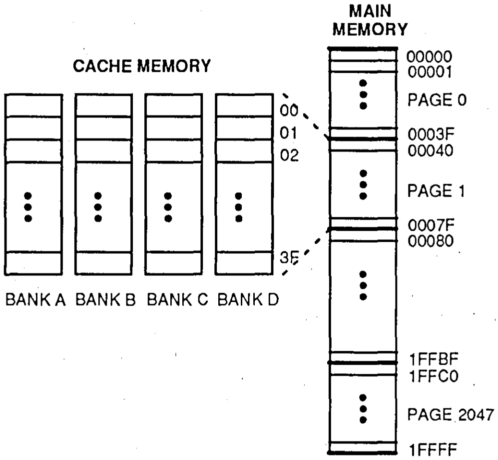


Figure 2. Four–Way Set Associative Cache

In general, four types of memory cycles are possible with a cache: read hit, read miss, write hit, and write miss. As mentioned earlier, a hit occurs during a read (or a write) if a match can be made between the most significant address bits and one of the tags, and the valid bit for that tag is set. When a read hit occurs, the data is simply read from the cache by the processor with no wait states.

When a read miss occurs, a line of data is read from main memory and placed in an appropriate location in the cache. At the same time it is being written into the cache, the processor reads the appropriate word of data from that line. This operation is known as a refill and is simplest when the line size is one word.

A write hit is the most complex of the four memory operations. In addition to writing the data into the cache, it is necessary to ensure that main memory is kept up–to–date. This may be handled two different ways; write–back and write–through. With the write–through method, the data is also written to main memory as soon as possible (usually immediately). This ensures that the data in main memory is always up to date. By making the cache controller responsible for performing the main memory write, the processor may continue operating at full speed from the cache even if the write is delayed. A series of writes, however, will cause the processor to again wait on main memory. While write–through has the advantage of keeping main memory fully up–to–date, there is the disadvantage that it makes heavy use of the main memory bandwidth. With write–back, main memory is updated only when the data is discarded from the cache. But this means main memory is not kept up to date. This forces the other devices, such as other processors and DMA controllers, to also examine the cache directory (or a duplicate) each time they reference main memory.

A write miss always results in a main memory write. The data may also be written to the cache, or the cache may be bypassed. It might seem to make the most sense to write to the cache, but an argument for not doing so is that an existing cache entry will be displaced by data that may not be read by the processor in the near future. As with the write hit, the processor may continue operating without wait states if the cache controller takes responsibility for performing the main memory write.

In addition to the four memory cycles just described, the cache controller must ensure that any changes to main memory (by DMA, other processors, etc.) are reflected in the cache. This is requires "snooping" the system bus and is known as the cache coherency problem.

To summarize this section, there are several variables in cache design. The organization of the cache is determined by the line size (in bytes), the bank depth (number of sets or number of lines per bank), and the degree of associativity (set size or number of banks). Choices also exist concerning the handling of cache coherency. And there are many more options that are beyond the scope of this application note.

DESIGNING CACHES WITH THE 80386/82385

The Intel 82385 cache controller couples tightly with the 80386 microprocessor to implement a 32K byte cache. Since the 82385 contains the tag directory and performs all the necessary control functions, only an 82385, high speed SRAM and a small amount of additional logic are needed to add a complete cache to an 80386 system. Cache hits allow the 80386 to run at its maximum rate of one memory cycle every two clock cycles. Instructions and data are cached together in the same cache memory, and operation of the cache is completely software transparent. Two pins allow the user of the 82385 to select between master and slave modes, and between a direct–mapped cache and a 2–way set associative cache.

The cache is placed between the 80386 and the rest of the system. Memory references from the processor are always intercepted first by the 82385. If a read hit occurs, the processor and cache remain completely independent of the rest of the system, and the read is performed directly from the cache. This allows use of the system bus by other processors or a DMA controller. Only in the case of a miss, a write, or an uncachable address is a memory reference passed on to the system bus. Figure 3 shows the basic bus organization of an 80386 system with a cache.

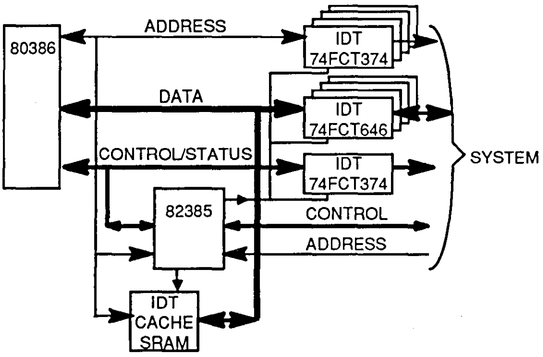


Figure 3. 80386 with Cache

Connections to the 82385

The 82385 controller has three interfaces; a processor interface to the 80386, a system bus interface (known as the 82385 local bus), and an interface to the cache SRAM. Through the processor interface, the cache controller is kept aware of the status of the processor and in turn controls the termination of memory cycles via a small amount of additional logic. Most other control signals between the two chips connect pin–to–pin. The NA# pin on the 82385 connects directly to the NA# pin on the 80386 and is used to put the processor into pipelined mode as described later. Optionally, the NA# input of the 80386 may be tied permanently high to prevent it from ever entering pipelined mode.

Included in the processor interface is the entire 80386 address bus (A_2–A_{31}). As detailed later, the least significant bits serve as the cache address while the remaining address bits become the tag that is stored in the directory. The 82385 has inputs (LBA#, NCA#, and X16#) which may be driven by address decoders to indicate any addresses that are either uncached local bus address space, other addresses not to be cached, and any address space of 16–bit memory—which is also uncached. Figure 4 shows the indirect connections between the two chips.

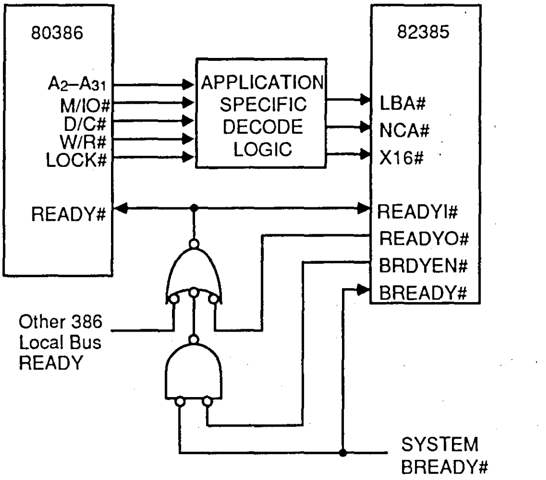


Figure 4. Indirect 80386–82385 Connections

The 82385 appears to the system to be a standard 80386. Many of the control signals from the 80386 have functional duplicates at the 82385's system interface. These are often shifted in time as the cache controller may manipulate the system bus independently of the 80386. Another part of the interface is provided by unidirectional address and status registers, and by bidirectional data registers. These are all controlled directly by the cache controller and are placed in high–impedance when the system bus is not being accessed. Lastly, the 82385 monitors the system address bus. As mentioned earlier this is one of the steps required to maintain cache coherency. Since a DMA controller or other device may alter a main memory location that is also cached, without address "snooping" it would be possible to have data in the cache that is out of date. To solve this problem, the 82385 monitors (snoops) the system address bus, mapping each address into the cache directory and comparing it with the appropriate tag(s). This tag comparison is interleaved with the normal tag comparisons that occur when the processor performs reads and writes. If a "snoop hit" occurs with this address, the corresponding cache line is marked invalid. The next read of that address by the 80386 will result in a miss and a refill of that line.

The SRAM memory interface is accomplished with ten pins. Figures 5 and 6 show the simplest direct–mapped and 2–way set associative configurations, requiring just an address latch and the memory. CALEN is used to latch 80386 addresses and is necessary because of the processor's ability to perform pipelined memory references. Four byte enable signals (CS0#–CS3#) allow writes of 1, 2, 3 or 4 bytes at a time. The remaining signals control reading and writing to each of the two banks of a 2–way set associative cache, and are intended for RAMs with separate output enable (OE) and write enable (WE) pins. To use RAMs with a single read/write control input, it is necessary to place a pair of IDT74FCT245 transceivers on the data bus. Also, it is necessary to gate OE and WE together to provide a control signal to enable and disable the transceiver. An additional signal from the cache controller controls the direction of the buffer. It goes without saying that anyone using the 82385 should avoid SRAMs without a separate OE input.

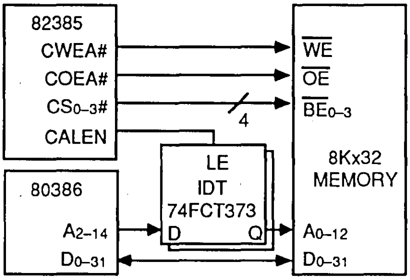


Figure 5. Direct–Mapped Static RAM Connections

Also note that on some versions of the 82385 cache controller, COE# goes active during write cyles as well as read cycles. Some SRAMs require that OE remain inactive during writes, making them incompatible with the Intel 82385. All of IDT's SRAMs are compatible with every version of the 82385.

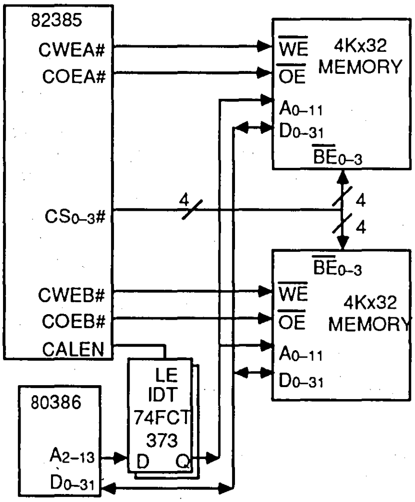


Figure 6. Two–Way Set Associative SRAM Connections

The Modes

The 82385 contains a 1024–tag directory, has a line size of a single 32–bit word (doubleword), and controls 8K of 32–bit cache memory. As mentioned earlier, by means of a mode pin, the 82385 operates in either a 2–way set associative or direct–mapped configuration.

In 2–way set associative mode the cache is organized as two independent banks of 4Kx32 memory. The tag directory is likewise organized with 512 tags for each bank, meaning that each tag corresponds to a group of eight lines. In Intel's terminology, each of these groups is called a set. This organization, shown in Figure 7, differs somewhat from the organizations described in the previous section because there is not a tag for each line. This was probably done to keep the directory small, but has the drawback of requiring that all eight lines in a set come from the same page of main memory. One bit in each directory entry indicates the validity of that tag, and eight additional bits indicate the validity of each individual line. If one line in a set is replaced by a doubleword with a different tag, the tag is changed and the seven other lines in that set must be marked invalid because their tag is overwritten.

The controller has two sets of read and write signals, one for each bank of the cache. When a memory read or write is requested by the 80386, the 82385 simultaneously performs a tag comparison in the appropriate set of both banks. If a hit occurs, the controller then performs the read or write at the cache by strobing the output enable or write enable of the appropriate bank. Figure 8 shows how the tag comparison is performed.

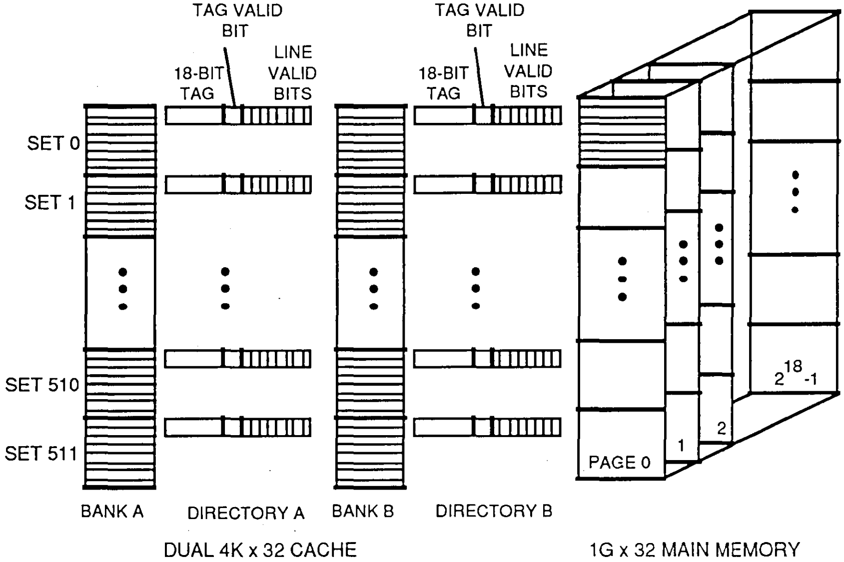


Figure 7. 82385 Two–Way Set Associative Organization

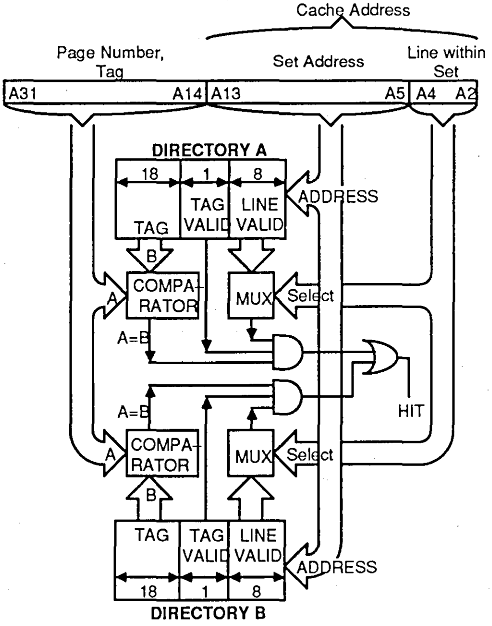


Figure 8. Two–Way Set Associative Set Comparison

The direct–mapped mode of operation is largely the same as 2–way set associative. The difference is that the cache is organized as a single 8Kx32 memory with a single 1024–entry tag directory (1024 sets). When a memory reference is made, only a single tag is compared with the address. When a hit occurs, the 82385 duplicates the read or write signals on both sets of SRAM control pins. Figure 9 shows the organization of the direct–mapped cache, and Figure 10 shows how the tag comparison is performed.

In the 2–way set associative organization, the first 12 bits (A_2–A_{13}) are the cache address or page offset. Of these, A_5–A_{13} determine the set, and A_2–A_4 determine the line within the set. The remaining bits (A_{14}–A_{31}) are stored as the tags. Because the direct–mapped cache is twice as deep, the tag is shortened by one bit and the cache address is increased by one bit. Therefore, A_2–A_4 are still the line within the page, A_5–A_{14} determine the page, and A_{15}–A_{31} are the tag. All of this address shuffling occurs within the 82385 based on the mode pin, and has no effect on the external connection of address pins.

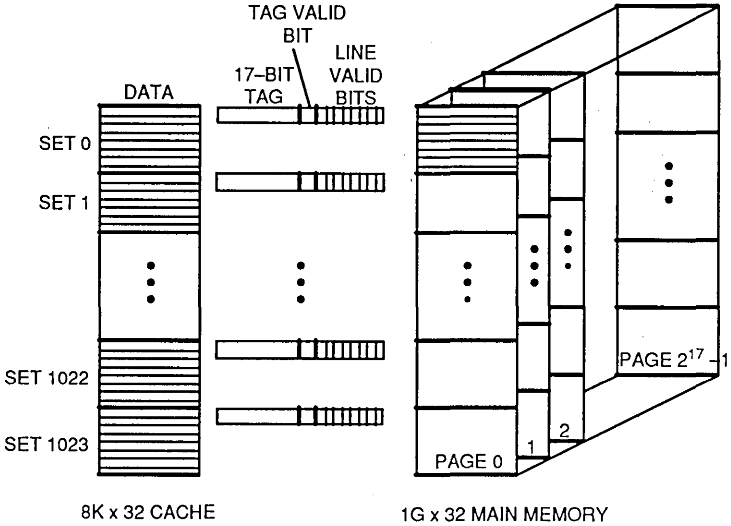


Figure 9. Direct-Mapped Cache Organization

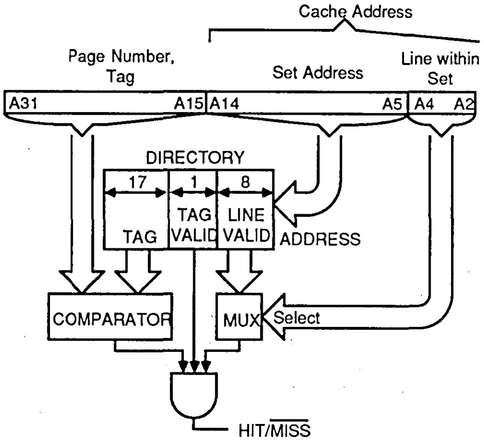


Figure 10. Direct-Mapped Tag Comparison

The distinction between master and slave modes is relatively minor and is not discussed here because it is not relevant to the basic operation of the cache.

82385 Operation

We will now discuss the details of how the 82385 handles the four types of cache operations previously discussed. During the first clock cycle of every memory reference, the 80386 outputs an address and status information, and brings ADS# (address status) low. At this time the 82385 latches the address for the cache RAM using CALEN, and performs the tag comparison(s) to determine if the reference is a hit or a miss. In the event of a miss, the controller clocks and enables the address, data, and status registers positioned between the 80386 and the system. During the following cycle(s), a normal main memory read or write takes place. The cache controller initiates this action by strobing BADS#, which to main memory (the system) appears functionally equivalent to ADS#, but trails it in time. The memory cycle is terminated by main memory which produces the BREADY# signal from a wait state circuit. See Figure 4.

When a miss occurs, the 82385 also asserts NA# (next address) which may be used to place the 80386 into pipelined mode. Pipelining causes the processor to output the address and status signals of the upcoming memory cycle before the current memory cycle is completed. This allows the 82385 to perform the tag comparison in advance and, if necessary, start the next main memory cycle immediately upon completion of the current cycle. Pipelining is not used during a series of cache hits because the cache is already coping with the 80386's minimum memory cycle time of two clock cycles. As the cache goes back and forth between misses and hits, the 80386 goes into and out of pipelined mode.

If a miss occurs during a read operation, the 80386 and 82385 both wait while main memory is read. The incoming data is then read by the processor and simultaneously written into the cache by the cache controller. It is of no concern that valid data may be overwritten, because the 82385 uses write–through to ensure that main memory always contains the same data as the cache.

During any kind of write, hit or miss, the data is written to main memory. But because the 80386 posts the write with the 82385, the processor usually experiences no slow down. That is to say, the 82385 performs all main memory writes for the processor using its system bus. As mentioned, the 80386 initiates a memory cycle with ADS#. The 82385 then waits, if necessary, for the system bus to become available. In the mean time, the controller asserts READYO# on the clock cycle following ADS# to indicate to the 80386 that the memory cycle is over. When the bus is available, the controller asserts BADS# to start the main memory cycle. When the system returns BREADY#, it is intercepted by the controller and blocked from reaching the processor. While this occurs, the 80386 may continue working out of the cache. Only a single write may be posted with the 82385 at a time, in part because the 82385 controls a single set of registers to latch the 80386's address, data, and status. See Figure 3.

A write hit is identical to a write miss except that a hit also results in a simultaneous write into the cache. Of course, if the main memory write is delayed, they are not simultaneous. Since a write miss does not result in a cache write, only a read miss can cause a new address to be cached, possibly displacing other valid data. The read hit is the simplest type of memory access because main memory is not involved. Once a hit is determined on the first clock cycle of a memory cycle, the data may be read out on the next clock cycle.

STATIC RAMS FOR A CACHE

As outlined earlier, the data memory portion of the cache consists of fast but otherwise ordinary SRAMs together with address latches, all controlled by the 82385. The SRAMs are organized either as a single 8Kx32 memory for a direct–mapped cache, or (more commonly) as two 4Kx32 memories for a 2–way set associative cache.

While RAM speeds are typically indicated by the maximum access time (address in to valid data out), there are many other timing parameters. Some of these are of special concern for 80386/82385 designs. The major SRAM timing requirements are shown in Table 1. The equations used to generate these numbers are shown below.

t_{AA} = 4 CLK2 – 386:T6(max) – 373:Tpd(D to Q, max) – 386:T21(min) or
4 CLK2 – 385:T21a(max) – 373:Tpd(LE to Q, max) – 386:T21(min), whichever is less
t_{CS} = 4 CLK2 – 385:T23(max) – 386:T21(min)
t_{OE} = 2 CLK2 – 385:T25b(max) – 386:T21(min)
t_{OHZ} = CLK2 – 385:T25c(max) + 386:T12(min)
t_{AW} = 4 CLK2 – 385:T21b(max) – 373:tp(LE to Q, max) + 385:T22c(min)
t_{CW} = 385:T26(min)
t_{DW} = 3 CLK2 – 386:T12(max) + 385:T22c(min)
t_{DH} = CLK2 – 385:T22c(max) + 386:T12(min)
t_{WP} = 385:T22b(min)

READ CYCLE PARAMETERS		16 MHz		20 MHz		25 MHz		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Address Access Time(1)	t_{AA}	—	65	—	51	—	39	ns
Chip Select Access Time	t_{CS}	—	71	—	52	—	44	ns
Output Enable to Output Valid	t_{OE}	—	19	—	14.5	—	13.5	ns
Output Enable to Output High Z	t_{OHZ}	—	15	—	10	—	6.5	ns
WRITE CYCLE PARAMETERS								
Address Valid to End of Write(1)	t_{AW}	83	—	65	—	48	—	ns
Chip Select to End Of Write	t_{CW}	40	—	30	—	25	—	ns
Data Valid to End Of Write(2)	t_{DW}	56	—	49	—	41	—	ns
Data Hold from End of Write(2)	t_{DH}	3	—	4	—	3	—	ns
Write Pulse Width	t_{WP}	40	—	30	—	25	—	ns

NOTES:

1. tAA and tAW are dependent on the delay of the address latch. Here, we assume that the latch is the IDT74FCT373.
2. These numbers given for tDW and tDH only guarantee compatibility with the 80386 and 82385. System timing for cache updates must also be considered.

Table 1. SRAM Timing Requirements

The most difficult read cycle times to meet are t_{OE} and t_{OHZ}. Some compromise, however, is possible on the latter. The maximum times given assume that the 80386 is enabling its data outputs in the least possible time, that the output enable signal coming from the 82385 is at its slowest, and that the SRAM is disabling outputs at its slowest. But the combination of conditions described above could occur only if the 80386 is at one set of conditions (minimum temperature and maximum Vcc) and the 82385 and SRAMs are at another (maximum temperature and minimum Vcc). While the guaranteed timings result in a calculated t_{OHZ} of 6.5 ns for SRAMs used with the 25 MHz processor and controller, the parameter may be increased by a few nanoseconds since all of the components on a board are at roughly the same temperature and voltage.

Still more time may be added to t_{OHZ} since a violation of this parameter only means that there will be contention on the data bus as the 80386 begins driving data. Brief contention at this time should not damage the chips and will not compromise data integrity.

The write cycle timings are generally less critical, although t_{CW}, t_{DH}, and t_{WP} should be checked. Any memory satisfying these parameters should easily meet t_{AW}.

From the table, it should be apparent that timing parameters that involve the address bus (t_{AA} and t_{AW}) are among the least critical. This implies that a fast address latch is not a major concern. Note also that for the times given in Table 1 for these parameters, it is assumed that IDT74FCT373 latches are used for the address. When using IDT CacheRAMs™ that have address latches included with the memory, 5ns may be added to the t_{AA} and t_{AW} requirements in Table 1 since the latch propagation delay is included in the access times of the CacheRAMs™.

The most common cache configuration is 2–way set associative since it gives higher performance than direct–mapping in the vast majority of instances. The IDT71586 was optimized for this application. As shown in Figure 11, only four of these latched 4Kx16 SRAMs are needed to implement the memory of a 2–way set associative cache. Prior to the IDT71586, this application required 27 chips plus the cache controller. It consisted of sixteen 4Kx4 (IDT6168) SRAMs, an address latch (two IDT74FCT373s), two AND gates (one 7408), and data buffers (eight IDT74FCT245s). Recall that the AND gates and data buffers are required for RAMs without separate read and write control pins.

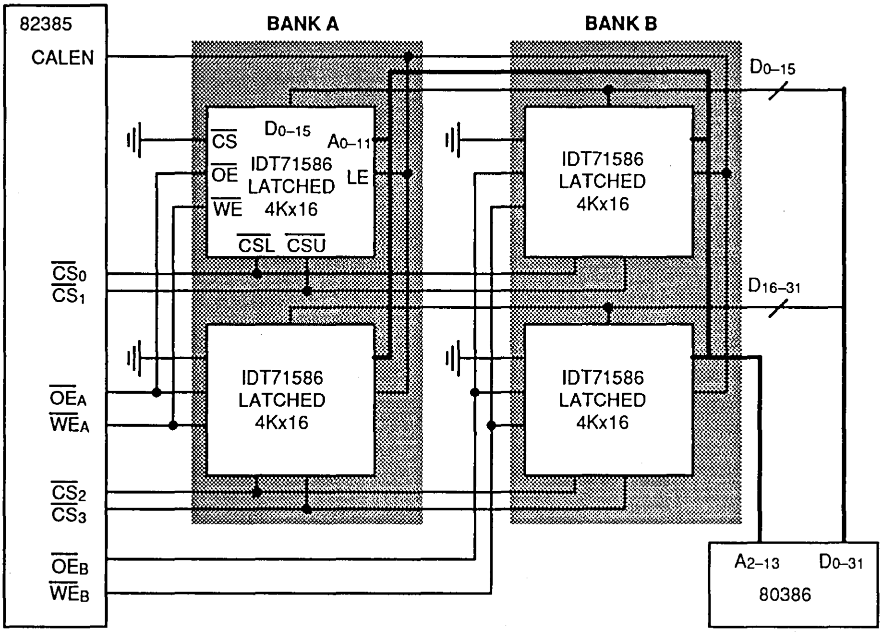


Figure 11. Two–Way Set Associative Cache Using IDT71586

The 8Kx32 direct–mapped cache has two plausible solutions. The best solution is to use 8Kx8 SRAMs such as the IDT7164. In addition to the four memory chips, two IDT74FCT373s are needed as an address latch. This arrangement is shown in Figure 12. The IDT71586 can also be used for this application. It requires an inverter for decoding A14 from the processor, which much also be latched.

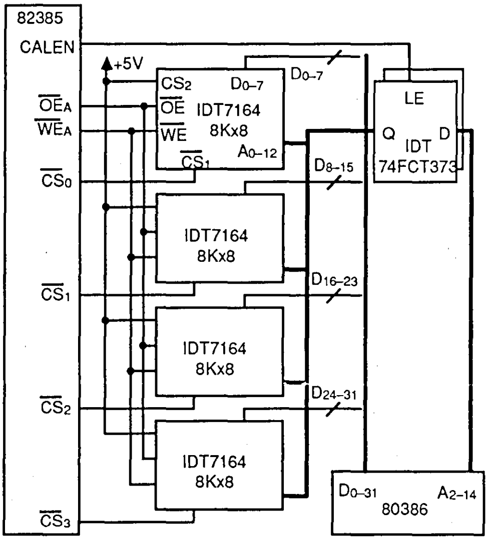


Figure 12. Direct–Mapped Cache Using IDT7164

INCREASING THE CACHE SIZE

The 82385 was apparently never intended to control anything other than a 32K byte cache, but it is possible to implement larger caches using a single 82385. Since the 82385 has a fixed number of sets (1024) and a fixed number of lines per set (8), there is no way to change the number of lines in the cache. Therefore, to double the size of the cache to 64K bytes, it is necessary to increase the size of each line from 32 bits to 64 bits. Although this might imply that 64–bit wide memory is necessary, that is not the case. Instead, since the 80386 is limited to 32–bit data, the line size changes to two doublewords. They are addressed independently, but are always adjacent memory locations and are either both valid or both invalid at any given time. And they share a tag. A read miss is handled by reading from two adjacent addresses in DRAM, writing this data into two SRAM locations, and presenting the 80386 with just one of these two doublewords. This is accomplished by offsetting address lines to the cache controller and SRAM, and adding a refill circuit that increases the number of doublewords transferred from main memory to the cache on each read miss. Read hits and write operations are left unchanged. The same principles can be used to increase the size of the cache still further. For example, quadrupling the cache size to 128K bytes is done by a 2–bit address offset, and performing four DRAM–to–cache transfers for each read miss.

Before continuing with some of the details of this procedure, we should first convince ourselves that the cache will function correctly with 64K bytes. In particular, can the proper validity of the cache data be assured? Since the 82385 bypasses the cache on a write miss, only a read miss places an entire new entry in the cache. The two doublewords are read from adjacent DRAM locations and written to adjacent cache locations. They share the same tag which is placed in the tag directory at this time. Also, the tag is marked valid and the valid bit corresponding to the entry is set. When a write hit occurs, one to four bytes are written to one address in both the cache and main memory. The remaining bytes are unchanged and the entire eight lines of the page remain valid. A write miss is performed as before, with one to four bytes written to main memory. And a read hit is also essentially unchanged. It is not difficult to see that the changes will not affect the ability of the cache controller to determine if a memory reference is a hit or a miss.

The first step in enlarging the cache size is to alter the connection of address signals to the 82385. Figure 13 shows how the address lines connect to the 82385 for the standard 32KB cache, and for 64KB and 128KB caches. Proper operation requires that the connection of A31 not be changed. The address connections of the cache SRAMs are largely unchanged, with one exception. For the 64K byte cache, it is necessary for the refill circuit to control the least significant address bit to the SRAMs because it must perform two DRAM–to–cache transfers while the 80386 and 82385 believe they are performing a single memory cycle. This is done by gating A2 through an XOR gate located between the address latch and the SRAM. The other input to the gate is controlled by the refill circuit. For the 128K byte cache, A2 and A3 are both modified in this manner. .

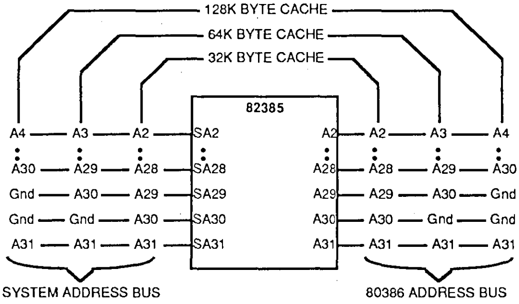


Figure 13. 82385 Address Connections

As mentioned earlier, memory cycles are initiated by the ADS# (80386) and BADS# (82385) signals and terminated by the READY# (80386) and BREADY# (82385) signals. Since neither the processor nor the cache controller may be allowed to continue until all DRAM–to–cache transfers are complete, it is necessary for external logic to control the READY# signal received from the system interface. Furthermore, the address referenced by the 80386 must be the last one of the two (64KB cache) or four (128KB cache) DRAM–to–cache transfers. This is because the 80386 will latch whatever data is present on its data bus when READY# is asserted to end the read cycle. All of this additional logic is called the refill circuit, which may be organized as a state machine plus combinational logic, and built using two PLDs.

For the 64KB cache, the first DRAM–to–cache transfer is performed with A2 inverted. The second transfer, which is read by the 80386, is done with A2 uninverted. Likewise with the 128KB cache, A2 and A3 are controlled during the four transfers such that the last transfer is with both A2 and A3 uninverted. This is easily accomplished with the XOR gates and control signals from the refill circuit.

Another concern is how the multiple SRAM writes are performed. In general, either the write enable pin or chip select pins of an SRAM may be used to control the timing of writes. Without intervention by the refill circuit, only one write will actually occur because CS$_0$#–CS$_3$# and CWEA# and CWEB# are strobed only once by the 82385. The refill circuit must intercept and generate multiple strobes of either the write enable signals or chip select signals since both control write operations. Keep in mind that for a 2–way set associative cache, the two write enable signals from the 82385 control which bank is written to. Therefore, a design that performs the writes by control of the write enable signals must be careful to strobe only one of the two during any given read miss cycle.

The interface to main memory and the means by which burst transfers occur is an issue left to the system designer. Static column DRAMs are the most probable type of main memory since RAS and CAS may be held steady while the address changes and different locations are read. The designer must also consider the generation of READY#, which ends all 80386 memory cycles. It must come from logic associated with either the DRAM or the cache control.

To summarize, the refill logic does nothing when a read hit or a write occurs. Only when a read miss occurs—indicated by the 82385 MISS# signal and the 80386 W/R# signal—does it take control of the various signals. Note that these two signals must be gated by other signals indicating the system status. The byte enables (CS$_{0-3}$#) are deasserted and the control signals are properly set to invert A2 (and A3 for the 128KB). When the first doubleword of data is received, it is written into the cache by strobing all the byte enables together. In the 64KB cache, A2 is then uninverted and the second (and last) transfer performed. This is the doubleword actually read by the processor. READY# is strobed at about the same time as CS$_{0-3}$# to end the cycle. The 128KB cache goes through a total of four transfers, with A2 and A3 being appropriately altered each time.

Intel has published a technical note on the subject of cache expansion.

SRAM SELECTION FOR LARGER CACHES

The selection of SRAMs for 64KB and 128KB caches is little different from the 32KB selection except for timing changes. One change is to the least significant address bit(s). The XOR gates shorten the access time (tAA) and address to write time (t$_{AW}$) by an amount equal to the propagation of the gate. The byte selects (CS$_{0-3}$#) are delayed from the 82385 to the SRAM when they pass through the PLD, but this is not a critical timing path. The only other timing considerations are data set–up and data hold time (t$_{DW}$ and t$_{DH}$), which are entirely dependent on the timing of the refill logic and system interface and cannot be detailed here.

Another external factor that may affect SRAM timing is the use of address decoding. Although the convention is to use SRAMs of the same depth as the cache (4K or 8K), it is quite possible to use shallower SRAMs and a decoder to decode the latched address. If the SRAMs are half the depth of the cache, only an inverter is required. A 2–to–4 or 3–to–8 decoder is needed for still shallower SRAMs. The only timing parameters affected are t$_{CS}$ and t$_{CW}$. The minimum timing for these signals will be equal to t$_{AA}$ and t$_{AW}$ minus the propagation delay of the decoder.

The only additional SRAM consideration is due to the XORing of the least significant address bit(s). Since the XOR gate(s) must be placed after the address latches, it is of no advantage to have SRAMs with integral address latches. If such SRAMs are used, the latches must be held transparent and external latches are needed. In place of the IDT71586, the IDT7186 may be used. It is a JEDEC standard unlatched 4Kx16 SRAM.

Once the timings are met, other parameters may be considered in the selection of SRAMs for a cache. Some of these parameters are listed in Table 2 for the IDT SRAMs that can be used in any of the cache configurations.

CACHE SIZE	ORG.	SRAMS	ADDRESS LATCH	OTHER LOGIC	BOARD SPACE(1)
32K BYTES	2–WAY: 4Kx32x2	4 4Kx16 (71586)	none	none	5.9 / 2.5
		16 4Kx4 (6168)	2 74FCT373	1/2 7408 8 74FCT245	11.4 / 8.1
	DIRECT: 8Kx32	4 8Kx8 (7164)	2 74FCT373	none	3.3 / 2.5
		4 4Kx16 (71586)	none	1/6 7404	5.9 / 2.5
64K BYTES	2–WAY: 8Kx32x2	8 8Kx8 (7164)	2 74FCT373	none	5.7 / 4.4
	DIRECT: 16Kx32	8 16Kx4 (7198)	2 74FCT373	none	5.0 / 3.5
		8 8Kx8 (7164)	2 74FCT373	1/6 7404	5.7 / 4.4
128K BYTES	2–WAY: 16Kx32x2	16 16Kx4 (7198)	2 74FCT373	none	9.2 / 6.4
		16 8Kx8 (7164)	2 74FCT373	1/6 7404	10.5 / 8.1
	DIRECT: 32Kx32	4 32Kx8 (71256)	2 74FCT373	none	5.1 / 2.5
		16 16Kx4 (7198)	2 74FCT373	1/6 7404	9.2 / 6.4
		16 8Kx8 (7164)	2 74FCT373	1/2 74139	10.5 / 8.1

NOTE:

1. Board space is in square inches, and excludes fractional ICs. The first number is for DIP packages with 0.1 inch spacing between packages. The second number is for SOIC packages (except for the 71586 which is a PLCC), also with 0.1 inch spacing between packages.

Table 2. SRAM Comparisons

As seen in Table 2, the SRAM of choice for the 64KB 2–way (8Kx32x2) is the IDT7164, because of its density.

For 16Kx32 (64KB direct) and 16Kx32x2 (128KB 2–way set associative) caches, the IDT7198 is the most likely choice, although the IDT7164 produces a competitive design. The IDT7198 gives a slightly denser design that consumes less power. At the same time, its 16K depth makes it well suited to these caches by eliminating decoding.

From Table 2, the 32Kx32 (128K direct) looks very attractive with the IDT71256. The reason for this is that the IDT71256 is the only 256K bit SRAM in the table. The high density makes it very competitive in both board space and power dissipation.

CONCLUSION

This application note has given an introduction to caches in general, and in particular to cache design with the Intel 80386 processor and 82385 cache controller. We have shown that while the basic design is rather straightforward, it is possible for ambitious designers to add to the design, creating a larger and higher performance cache.

Dedicated SRAMs, such as the IDT71586 CacheRAM™, further simplify the design process while making a significant breakthrough in board space and power savings. This five–chip solution now makes a high performance set associative cache available to any 80386 designer.

Integrated Device Technology, Inc.

A 33MHz MC68030 ZERO-WAIT CACHE MEMORY

APPLICATION NOTE AN-46

INTRODUCTION

The 33MHz MC68030 can achieve its maximum potential only through the use of zero wait external cache memory. At 33MHz, integrated cache tag RAMs, which combine RAM, compare and reset logic into a single package, are mandatory. The use of these integrated cache tag RAM devices allows the MC68030 to operate at 33MHz with zero wait states. Most cache designers would agree that discrete cache implementations which satisfied the requirements of 20 or 25MHz systems, fail when tasked at 33MHz clock frequencies. Integrated cache tag RAMs allow for 33MHz MC68030 operation today and a means to achieve 50MHz operation in the future.

This application note will present a detailed 33MHz, zero wait MC68030 cache design using integrated cache tag RAMs. It is assumed that the reader has basic MC68030 and cache knowledge.

PRODUCT FEATURES

- 33.3MHz MC68030 zero wait operation.
- 64K bytes of direct mapped external cache organized as 16K x 32.
- Two clock cache read hit yields a 67M byte/sec cache bandwidth.
- Write through cache architecture.
- Single level shared memory write pipeline.
- Cache coherency/shared memory supported through MC68030 local bus arbitration.

CACHE ORGANIZATION

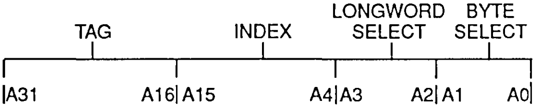
The 33MHz 68030 design uses a 64K byte direct mapped unified (both instruction and data) cache organization. The line size is 16 bytes or four entries of 32 bits each. Read hit cycles require 2 clocks (2 x 30ns = 60ns) for a minimum cycle time of 60ns. Read miss cycles generate a retry cycle through the simultaneous assertion of the MC68030 bus error (BERR*) and halt (HALT*) signals (to be discussed later). The minimum length of the read miss is six clocks (2 for read miss, 2 idle clocks and 2 for the retried read cycle) which supports a memory subsystem with a 180ns cycle time. Longer memory cycle times can always be accommodated.

Cacheable write cycles are performed in three clocks. A write through cache policy is implemented which provides that only cacheable write hit cycles (and read miss cycles) require an update of the cache data. A single level write pipeline accepts the MC68030 write address and data in three clocks so that the CPU can continue processing while the memory write is taking place.

Since the cache is direct mapped, each location in memory has but one possible resting place within the cache. By definition the cache is four bytes wide (32 bits); therefore, there are 16K locations in the 64K byte cache. The mapping mechanism is based upon the fourteen address bits, A15–A2. Each memory location is mapped into one of 16K cache locations based upon these address bits.

The cache line size dictates how deep the tag and validity RAMs must be in order to store all of the addresses of the data cache entries. A 64K byte cache with a 16 byte line size would require (64K/16 = 4K) a 4K deep tag and validity RAM. The tag RAM (4K x 16 – 4 devices) stores the address of each 16 byte line of data contained in the cache. Each of the four IDT6178S12 CMOS cache tag RAMs provide a MATCH compare output. A cache "HIT" occurs when all four MATCH bits are high.

Sixteen address bits A31–A16 comprise the cache "TAG" which are compared and stored in the cache TAG RAMs. Address bits A15–A4 become the tag index for selecting a sixteen byte cache tag entry. Address bits A3 and A2 are called the longword select. Address bits A1 and A0 are the byte select lines. Since all cache read operations present 32 bits of data, the byte select lines are only used for cache writes.



The validity RAM (4K x 4 – IDT6178S12) contains the valid/invalid state of each of the four longwords within the selected cache line. Valid bit 0 (VALID0) represents the valid/invalid state of longword 0 (offset = 0), valid bit 1 (VALID1) represents the valid/invalid state of longword 1 (offset = 4), etc. A validity bit set to 1 indicates a valid entry. All valid bits are cleared on reset using the IDT6178S12 clear function. This forces all locations in the validity RAM to 0 (invalid).

Up to 268M bytes of cacheable shared memory can be accommodated by the 33MHz MC68030 design. PAL, P100 (U2) generates the STERM* (synchronous terminate), CACHEN* (Cache enable), and MEMCS* (shared memory chip select) upon receipt of an address in the range of 0000 0000 – 0FFF FFFF. This PAL can be modified to accept different address ranges and memory sizes.

THE 33MHz MC68030 DESIGN CHALLENGE

The 33MHz MC68030 has a zero wait cycle time of 60ns (2 clocks @ 30ns each). This sharply contrasts with the typical dynamic memory cycle time of 150ns to 200ns. A high speed cache memory, which has a cycle time of 25ns or less and a hit rate of greater than 90%, can bridge the disparity between CPU cycle time and main memory cycle time.

The stringent timing requirements imposed by the 33MHz Motorola MC68030 has made zero wait state design a major challenge. There are several critical timing parameters which must be satisfied.

STERM* SETUP

In order to operate a two clock, zero-wait cycle, the MC68030 STERM* (Synchronous termination) signal must be valid (T60) 2ns before the clock rising edge in state 2 of the

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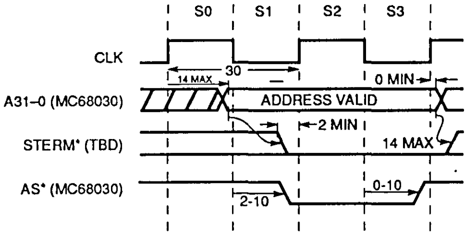
MC68030 bus cycle. In a cached system, a hit must be detected before the acknowledge (STERM*) can be generated. The time required to detect a cache hit is as follows:

CACHE HIT DETERMINATION:

1 clock @ 30ns each:	30
MC68030 Address Valid, T6:	(14) max
STERM* setup to clock high, T60:	(2) max
Time available to detect a cache hit:	14 ns



STERM* Setup Diagram – 33MHz MC68030

Consequently there is 14ns to perform a cache tag lookup, tag compare and generate the STERM* signal. In the most hopeful scenario, an IDT6178S12 (12ns) cache tag could be used in conjunction with a 7ns PAL to generate the STERM* signal. This would result in a (14 – 12 – 7.5 = – 5.5) –5.5ns STERM* setup. Obviously, this approach is not acceptable.

BERR*, HALT* SETUP

The MC68030 allows a cycle to be retried (repeated) if both BERR* (Bus Error) and HALT* are asserted simultaneously before the falling clock edge at MC68030 state 3. We can take advantage of this feature by always issuing STERM* on all cacheable read cycles and should a cache miss be detected, issue both BERR* and HALT* in time to retry the bus cycle. This configuration will require the use of the IDT6178S12 4K x 4 cache tag RAM (See Figure 2), a 74F20 to AND the four MATCH bits and a 10ns PAL to generate the BERR* and HALT* signals. Schematic pages 24 & 25 show the tag RAM, the validity RAM and the BERR*, HALT* generation (Retry Control).

The time required to generate BERR* and HALT* is calculated as follows:

BERR*, HALT* GENERATION:

1.5 clocks @ 30ns each:	45
MC68030 Address Valid, T6:	(14) max
IDT6178S12, Tadm:	(12) max
74F20 prop. to MATCH* valid:	(6) max
10ns PAL prop. to BERR*, HALT*:	(10) max
BERR*, HALT* setup to clock low:	3 ns

MC68030 T27a Required = 3ns

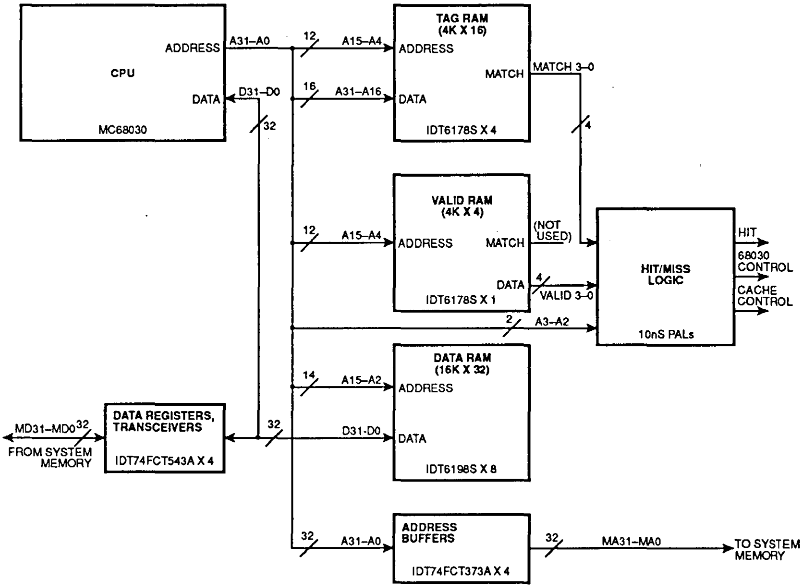
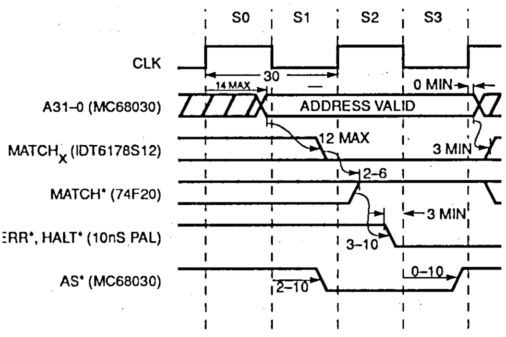


Figure 1.0 33MHz 68030 Cache Block Diagram



BERR*, HALT* Setup Diagram – 33MHz MC68030

Since BERR* and HALT* can be generated in time, the method of retrying cache miss cycles works! Because cache miss cycles comprise less than 10 percent of MC68030 read operations, the retry operation will not hinder the 2 clock cache hit cycle.

The above analysis proves that the integrated approach to cache tag RAMs (which combine both static RAM features and compare logic) is mandatory. A discrete implementation would be capable of a 17.5ns address to match time (12ns RAM access, 5.5ns compare using 74FCT521B) which fails to approach the IDT6178S12 t_{ADM} of 12ns.

DATA SETUP

In order to determine the speed of the cache data RAMs required, an analysis of the data access time is in order. The MC68030 cache design utilizes the IDT6198S25, 16K x 4 CMOS static RAM. Schematic pages 26 & 27 show the data RAM configuration. The IDT6198 provides chip select (CS*), write enable (WE*), and output enable (OE*) controls. The fastest means by which these RAMs can be accessed is through the output enable control. Consequently, the MC68030 cache data RAMs have their chip select controls grounded (always enabled). The critical read data access paths are then the address access (t_{AA}) and the output enable access (t_{OE}) times.

A benefit of this cache architecture is that complicated control of chip select and write enable (which is required for a RAM without an output enable) to prevent bus contention on write operations and byte write hit cycles is not required.

The cache data access time is calculated as follows:

CACHE DATA RAM ADDRESS ACCESS TIME:

1.5 clocks @ 30ns each:	45
MC68030 Address Valid, T6:	(14) max
MC68030 Data setup to clock low, T27:	(1) min
IDT6198S capacitance derating (See Loading analysis, Appendix A):	(2) max
Data RAM Address Access:	28 ns

IDT6198S25 t_{AA} Required = 25ns

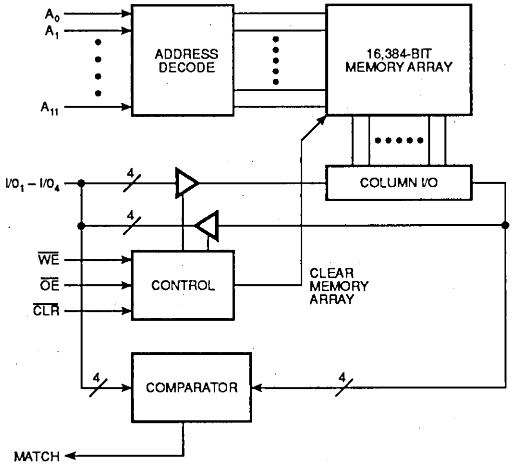
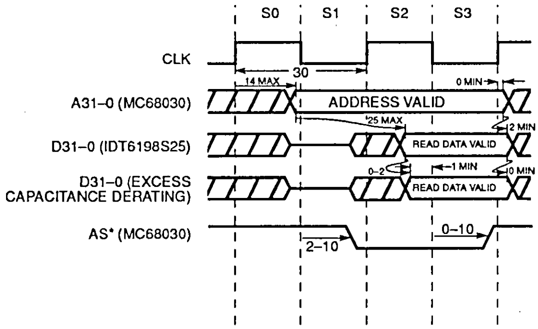


Figure 2.0 IDT6178S12 CMOS Cache Tag RAM



Data Access Time Diagram – 33MHz MC68030

The analysis above has proven that a 33MHz MC68030 cache can operate with no wait states using integrated cache tag RAMs, data RAMs with output enable, and a retry operation for cache misses.

Refer to Appendix B for detailed tabulations of the MC68030, the cache tag and data RAM timing requirements.

A loading analysis (Appendix A) resulted in a determination that the capacitive load on the MC68030/cache data bus was above that specified by the IDT6198S25 data sheet. Consequently, a 2ns delay (0.05ns/pF) was added to the data access time path to accommodate the 37pF additional capacitance. There was no excessive capacitive loading on the MC68030 address bus; consequently, no derating was required. The loading analysis (Appendix A) and the user interface (Appendix G) provide more detailed information on these issues.

PERFORMANCE ISSUES

BURST MODE OPERATION

The 33MHz MC68030 cache design utilizes a 2 clock cache read and 3 clock write bus cycles. The MC68030 burst mode 2:1:1:1 was not supported because the burst cycle actually slows the MC68030 in systems which support a 2 clock cache hit (which this design does). On burst cycles, the MC68030 will wait until all four longwords have been fetched before the first longword can be used.

For example, assuming instructions A, B, C and D all reside in shared memory and the external cache at successive locations starting at offset 0, the following analysis applies:

FOUR FETCH 2–2–2–2 NO BURST CASE (8 CLOCK FETCH TIME)

Clock at Which Instruction Enters MC68030 Instruction Pipeline

	1	2	3	4	5	6	7	8	9	10
INSTRUCTION # 1:		A								
INSTRUCTION # 2:				B						
INSTRUCTION # 3:						C				
INSTRUCTION # 4:								D		

2:1:1:1 BURST CASE (5 CLOCK FETCH TIME)

Clock at Which Instruction Enters MC68030 Instruction Pipeline

	1	2	3	4	5	6	7	8	9	10
INSTRUCTION # 1:		a			A					
INSTRUCTION # 2:			b			B				
INSTRUCTION # 3:				c			C			
INSTRUCTION # 4:					d			D		

ILLUSTRATION NOTES:

1. a, b, c, and d denote the clock at which the instruction is fetched from the external cache.
2. A, B, C, and D denote the clock at which the instruction enters the MC68030 instruction pipeline.

The total number of clocks required to fetch the four instructions in the no burst case exceeds the burst case by three (8 – 5 = 3). However, because the no burst case allows the MC68030 to begin execution of instructions A, B and C (by 3, 2, and 1 clocks respectively) before the burst case, the no burst case will execute faster.

N-WAY VERSUS DIRECT MAPPED CACHE ORGANIZATION

Without a doubt, the 2 or 4 way set associative cache has a higher hit rate than a direct mapped cache. However, the hit rate is but one of several factors which must be entered into the performance equation. An n-way set associative cache design would be constructed in one of two methods. The first method would contain one cache data RAM which would be divided n ways by an address generated from the hit/miss logic. This method would require extremely fast (5ns) address access times on the cache data RAM since the cache tag RAM would now be in the critical path from address to data. The second method would provide n data caches (connected in parallel), only one of which would be enabled by the cache hit/miss logic at a time. This method requires that none of the n caches be enabled until a cache hit has occurred, whereas in a direct-mapped cache, the cache data RAMs are constantly enabled until turned off by a write cycle or a cache miss. Obviously, a system whose data RAM is already enabled will provide data much faster than a system whose data RAM must be enabled only after a cache hit is detected. An analysis of the n way data caches, connected in parallel follows:

2 WAY SET ASSOCIATIVE CACHE DATA RAM OUTPUT ENABLE ACCESS TIME:

1.5 clocks @ 30ns each:	45	
MC68030 Address Valid, T6:	(14)	max
MC68030 Address additional capacitance derating, 8 devices x 7pF = 56pF. At 0.05ns/pF the factor is:	(2.8)	max
IDT6178S12, tADM:	(12)	max
7ns PAL prop. to cache output enable:	(7.5)	max
MC68030 Data setup to clock low, T27:	(1)	min
IDT6198S data additional capacitance derating, 8 devices x 7pF = 56pF. At 0.05ns/pF the factor is:	(2.2)	max
Data RAM Output Enable Access:	5.5ns	

IDT6198S15 t_{OE} Required = 8ns

Since the design can only provide 5.5ns of output enable access time, and the IDT6198S15 requires 8ns, a wait state must be added. Consequently, a read hit cycle will require three clocks. That translates to a 50% lower cache bandwidth than the 2 clock direct mapped cache design presented. Even a 10% improvement in the cache hit rate provided by an n-way set associative cache is more than offset by the slower cache bandwidth. Therefore, the fastest cache architecture for the 33MHz MC68030 is a 2 clock direct mapped implementation.

Assuming a 98% hit rate for n-way set associative cache, an 88% hit rate for a direct mapped cache, and an 8 clock memory cycle on read misses (240ns), the following analysis applies:

N-WAY SET ASSOCIATIVE CACHE (98% HIT RATE, 3 CLOCK CYCLE):

Hit Rate x # Clocks: 0.98 x 3 = 2.94
Miss Rate x # Clocks: 0.02 x 8 = 0.16

Average Clocks per Bus Cycle: 3.1

DIRECT MAPPED CACHE (88% HIT RATE, 2 CLOCK CYCLE):

Hit Rate x # Clocks: 0.88 x 2 = 1.76
Miss Rate x # Clocks: 0.12 x 8 = 0.96

Average Clocks per Bus Cycle: 2.72

THE 33MHZ MC68030 CACHE DESIGN

Schematic page 21 (Appendix D) shows the block diagram of the MC68030 cache design. It is comprised of six major functional units:

1. 33MHz MC68030 Central Processor.
2. Cache tag RAM (4K x 16) implemented with four IDT6178S12 (12ns) 4K x 4 CMOS cache tag RAMs.
3. Cache Validity RAM (4K x 4) implemented with one IDT6178S12 (12ns) 4K x 4 CMOS cache tag RAM.
4. Cache data RAM (16K x 32) implemented with eight IDT6198S25 (25ns) 16K x 4 CMOS static RAMs.
5. Write pipeline implemented with four IDT74FCT543A registered data transceivers and four IDT74FCT373A address latches.
6. Hit/Miss logic; cache, write pipeline, MC68030, and coherency control logic implemented using six 10ns PALs.

CENTRAL PROCESSOR

The 33Mhz MC68030, U1 on schematic page 22 is the central processing unit for this design. The MC68030 is a 32 bit virtual memory processor which provides:

- 256 byte instruction cache.
- 256 byte data cache.
- Paged memory management unit (MMU).
- Pipelined architecture.
- MC68020 object code compatibility.

Because the MC68030 has an internal MMU, only physical addresses are presented at the address pins. Consequently, our design incorporates a physical cache which alleviates the problems associated with virtual caches (such as flushing on I/O, task swaps, or MMU translation buffer updates).

P100 (U2), a 10ns PAL controls the assertion of STERM* to the MC68030 and decodes the memory chip select (MEMCS*) and the cacheable address space (CACHEN*). Memory space is defined as the lower 268M bytes of supervisor or user instruction/data space. Cacheable cycles are defined as memory space with no cache inhibit out (CIOUT*), no read modify write (RMC*), no bus grant acknowledge (BGACK*), and no cache disable jumper installed (JP3). Modifications to cacheable space or memory space can be easily accomplished through reprogramming of P100.

MC68030 CYCLE TERMINATION

The bus cycle acknowledge for the cache design uses the MC68030 STERM* (synchronous termination) signal exclusively for read hits, read misses, write cycles, and noncacheable reads or writes to memory.

Cacheable memory read cycles will always cause STERM* to be generated based upon the MC68030 address being valid. This will result in a two clock read cycle. On write cycles, retry cycles or noncacheable read memory cycles, the TERMACK* signal is asserted by P105 (10ns PAL, U25 schematic page 28). This signal in turn causes STERM* to be generated by P100. Refer to Figure 2.0, page 34, for read and write cache hit operation.

The use of STERM* for all main memory/cache accesses mandates a 32 bit wide memory architecture. In fact, the four 74ALS08 gates (U34) on schematic page 30 are used to force all memory read cycles to be aligned longword reads. Since we are using a 32 bit cache, the smallest cacheable unit is 32 bits; therefore, byte word or 3 byte memory reads are forced to appear as 32 bit aligned accesses to memory.

Write hit or miss cycles require three clocks if the write pipeline is empty. Write cycles are never retried. The pipeline cannot be overwritten. Memory read or write cycles which occur after the pipeline has been filled by a previous write cycle will require the MC68030 to wait until the pipeline has been emptied. The write pipeline design allows the memory write cycle to occur independent of the MC68030/cache operation. Therefore, read hit cycles may continue without interruption while a memory write is taking place.

The MC68030 contains an internal write pipeline in its bus interface unit. Therefore, the addition of the external pipeline yields a two stage write pipeline.

The DSACK1* and DSACK0* signals (Data and Size acknowledge) are reserved for use by the user for I/O, EPROM, system bus, MC68882 (Floating Point Coprocessor), or other device.

Should a cache read miss occur, both BERR* and HALT* will be generated which will force a retry operation. The MC68030 will respond to the simultaneous assertion of both HALT* and BERR* by terminating the current cycle, waiting two idle clocks and reissuing the cycle. On retry cycles, the generation of STERM* on the second bus cycle is disabled. MC68030 write cycles and all noncacheable cycles (read or write) are never retried. See Figure 3.0, page 36, for a detailed timing diagram of the retry operation.

MC68030/SYSTEM CLOCK GENERATION

The MC68030 and system clocks are generated by a 66.66MHz oscillator (U23) and a 74F174 octal register shown on page 28 of the schematics. The clock generator is designed to provide a 50% duty cycle square wave which minimizes skew between clocks. The 74F04 (U3C) provides the divide by two function to generate a 33MHz clock from the 66.66MHz oscillator.

There are four clocks generated on pages 28 & 29. Two are active high, CLK33M1 and CLK33M2. Two are active low, CLK33M1* and CLK33M2*. CLK33M1 drives the MC68030. The remaining three clocks each drive two PAL devices.

All four clock drivers are terminated with both series and parallel resistive and parallel capacitive terminators. The values of these terminators may have to be altered based on board layout or additional clock loading. To minimize electromagnetic emissions and provide a clean clock signal the following routing rules should be followed:

1. Daisy chain route all clock lines.
2. Clock lines should be minimized by tight placement and routing.
3. Parallel termination resistors should be placed at the end of each clock net (See R2–R9, schematic page 29).
4. Series terminating resistors and load capacitors should be placed at the clock driver source (See R10–R13, schematic page 29).
5. A faraday shield should be created around each clock with a ground trace adjacent to each side of the clock trace.
6. The clock nets should have no feedthroughs.
7. Clock traces should have 45 degree and not right angle bends.
8. The clock traces should be placed on a layer adjacent to the ground plane.
9. Each clock should have four or less loads.
10. Clock loads should distributed equally along the trace.
11. Provide a generous supply of decoupling capacitors (0.1µF) around the clock generator circuit and all clocked devices.
12. A capacitor should be placed at the source (but after the series resistor) of each clock line to equalize loading on each trace, minimize ringing, and to establish approximately 50pf of loading on each trace. The values of these devices may need to be adjusted after layout and/or debug. (See C1–C4, schematic page 29).

CACHE TAG/VALIDITY RAMS

The 12ns IDT6178S12 4K x 4 CMOS cache tag RAM (See Figure 1.0) is used for both the tag and validity functions. The purpose of the tag and validity RAMs is to save the addresses of the memory data which are stored in the data cache. On each cacheable read or write cycle, the current address is compared with the selected address in the cache tag and the selected validity bit in the validity RAM. If all four tag RAMs "Match" and the selected validity bit is set, a hit has occurred. Address bits A31–A16 are the "TAG". The tag is stored as data in the IDT6178S12 CMOS cache tag RAM. Address bits A15–A4 serve as the index into the tag RAM. Address bits A3 and A2 are longword select lines. They are used to select one of the four validity bits. The cache tag and associated logic can be found on page 24 of the schematics.

The 4K x 16 tag is constructed of four of the IDT6178S12 devices (U7–U10). Each of the four devices provides a match signal (MATCH3–0) which are ANDed by U5A (74F20) to create the global MATCH* signal. The MATCH* signal, along with the validity bits, are used to determine whether a cache hit or miss has occurred. In addition, on a read miss/update cycle the MATCH* is used to determine whether the three unused validity bits are to be saved or invalidated (this will be explained shortly).

The IDT6178S12 cache tag provides an integrated CMOS static RAM and comparator. By combining these functions, the device eliminates inter-chip delays to offer a high speed and high density solution to cache tag applications. The IDT6178S12 also provides a CLEAR function which is not used in this design for the tag RAM, but is a mandatory part of the validity RAM.

The validity RAM also uses the IDT6178S12 (U11) device. As a validity RAM, the match feature of the IDT6178S12 is not required. However, the CLEAR feature is used whenever a RESET or cache flush (FLUSH* asserted by user provided logic — usually an I/O port) occurs. During these conditions, the validity RAM is cleared to force all bits in the validity RAM to 0. Consequently, all cache locations are rendered invalid.

Each location in the validity RAM holds four bits. Each bit represents the valid/invalid state of one longword in the sixteen byte cache line. A valid cache entry will have its corresponding valid bit set (1). Invalid cache entries have their validity bit cleared (0). The following details the correlation between the validity bits and the address of the cache entries:

DESCRIPTION	SIGNAL NAME	ADDRESS RANGE	ADDRESS BITS A3	ADDRESS BITS A2
Valid Bit 0	VALID0	XXXX XXX0	0	0
Valid Bit 1	VALID1	XXXX XXX4	0	1
Valid Bit 2	VALID2	XXXX XXX8	1	0
Valid Bit 3	VALID3	XXXX XXXC	1	1

The validity bits can only be set by read miss cycles. Write cycles (whether a hit or a miss) do not affect the validity bits. On every read miss cycle, a read modify write operation takes place at the validity RAM. At the start of the read miss cycle, the validity RAM read occurs when the validity RAM control PAL, P101 (U4), is clocked by the VALIDCLK signal (From P102). Upon receipt of the VALIDCLK rising edge, P101 modifies the validity bit values and stores the new values in the PAL's four registers. When the shared memory cycles is complete, the VALIDWE* signal asserts for one clock cycle (approximately 30ns). The VALIDWE* falling edge starts the validity RAM write cycle and forces P101 to output the new validity bits. The rising edge of VALIDWE* writes the new validity bit data from P101 into the validity RAM.

P101 modifies the validity bits based upon address bits A3 and A2. The validity bit selected by address bits A3 and A2 will always be set. The other three validity bits will remain unchanged if tag RAM indicates a match condition. However, should a match not occur, the three unselected validity bits will be invalidated (cleared to 0).

On coherency cycles, if a match occurs, all four validity bits are cleared to 0. This will be discussed in depth in a later section of this application note entitled "Cache Coherency".

The control signals for the tag and validity RAMs are generated by 10ns PAL, P104 on page 28 of the schematics. They are as follows: The tag write enable (TAGWE*), which only asserts on read miss/retry cycles. The validity write enable (VALIDWE*), which asserts on both read miss/retry cycles and cache coherency cycles. Another validity control signal, VALIDCLK, (Generated by P102, U6, schematic page 25) is used to clock the validity RAM control PAL, P101 and output enable the validity RAM, U11.

CACHE DATA RAM

The cache data RAM is constructed using eight IDT6198S25 CMOS static RAMs. The WE* (write enable) and OE* (output enable) control pins make these data RAMs uniquely suited for this application. Here's why.

Bus contention (two tristate devices driving the bus at the same time) is a major consideration in cache design. On write cycles, memory devices with only CS* and WE* require complex timing to ensure that the RAM does not go into the read mode for even an instant. That is, WE* must be asserted before CS*, and CS* must be deasserted before WE* in what is known as a chip select controlled write cycle. Because the IDT6198S25 has a separate output enable pin for read cycles, it does not require this special chip select controlled write timing.

Another advantage of the IDT6198S25 is found on byte, word, or 3 byte write hit cycles where the entire longword is not being written. On all write cycles, the MC68030 drives all four bytes of the data bus. Cache memory devices which have only CS* and WE* pins must provide individual chip selects for each RAM to prevent a device which is not being written from output enabling its data and causing bus contention with the MC68030.

Again, the IDT6198S25 is not restricted under these conditions since it provides an output enable pin to only allow the output of read data on read cycles.

The cache data RAM (U13–U20) can be found on pages 26 & 27 of the schematic diagrams. Four write enables (CAWE3–0) are generated by 10ns PAL, P103 on page 28 of the schematics. These write enables assert for only the selected bytes based upon the 68030 outputs SIZ1, SIZ0 and A1, A0 on write hit cycles. On read miss/retry cycles, all four bytes are written to update an entire longword.

The CACHEOE* (Cache output enable) signal, generated by P104 on page 28 of the schematics, is used to output enable the cache data RAMs on read hit cycles. This signal asserts on all read cycles in MC68030 state 1. If a read miss or a noncacheable read cycle occurs, CACHEOE* will deassert in state 2. On read hit cycles, CACHEOE* will hold the cache read data valid until the cycle is complete.

The data cache RAM chip selects are grounded in this design for several reasons:

1. Chip select pins always respond more slowly than output enable pins, so the fast OE* access time allows the slowest possible static memory device to be used for the cache data RAM.
2. Complicated chip select control to prevent bus contention is not required.
3. The elimination of the chip select access time critical path allows faster designs (i.e. 50MHz) to be accommodated in the future.

Power dissipation is not an issue, since an efficient cache will be chip selected more than 90% of the time anyway.

WRITE PIPELINE

On MC68030 cacheable or uncacheable write cycles, the write pipeline stores the write address and data into latches and registered transceivers (See schematic pages 30 & 31). Control logic for the pipeline handles the memory request and completion of the write to memory. This mechanism allows the MC68030 to perform any single cacheable or uncacheable write in three clocks (one wait state). Successive write operations require longer to complete since the pipeline is only one level deep. However, since most write operations occur intermittently, the MC68030 is free to execute out of the cache until a read miss or a write cycle occurs. This architecture maximizes the cache utilization by eliminating needless waiting by the MC68030 for memory write cycles to complete.

The write pipeline is comprised of three major components:

1. The address pipeline, IDT74FCT373A octal latches, U26–U29, on schematic page 30.
2. The data pipeline, IDT74FCT543A octal registered transceivers, U30–U33, on schematic page 31.
3. The pipeline control/acknowledge PAL, P105, U25 on schematic page 28.

On any memory write cycle, the PIPEFULL* signal generated by P105 asserts and latches the write address and data into the pipeline registers on schematic page 30 & 31. The PIPEFULL* signal serves as a memory request signal; however, the user is free to predecode the memory request using the memory chip select (MEMCS*), the MC68030 address strobe AS*, and the WRITE* signal. The TERMACK* signal generated by P105 asserts on all memory cycles to indicate cycle completion. On write cycles when the pipeline is not full, TERMACK* is generated immediately. On noncacheable read cycles or read miss/retry cycles, TERMACK* is generated upon receipt of the MEMACK* (The user supplied memory acknowledge). On successive write cycles the second MC68030 write cycle is acknowledged with TERMACK* after receipt of MEMACK* for the previous write cycle. Figure 4.0, page 38, shows the write pipeline timing.

The user should use the PIPEFULL* signal as a memory request. As long as a MC68030 write cycle is pending completion, the PIPEFULL* signal will be asserted. For successive write cycles, the PIPEFULL* signal will always deassert for one clock between the two write cycles.

CACHE COHERENCY

A coherent cache is one where the cache represents an exact copy of memory. Cache coherency is accomplished in this design through the MC68030 bus arbitration interface. The MC68030 provides for alternate masters to share its address and data bus and some of its control signals using the BR*, BG* and BGACK* (Bus request, Bus grant, and Bus grant acknowledge) signals. Through this interface, cache tag locations are compared and if a match is detected, the four validity bits in the validity RAM are invalidated. By this means, the selected sixteen byte cache line is invalidated, and the MC68030 must fetch new entries from memory if needed through the read miss/retry cycle. This mechanism will insure that the cache always contains an exact copy of the memory contents.

To initiate a cache coherency cycle, the following steps must take place:

1. User supplied logic from the shared memory or system bus interface must first issue a bus request (BR*).
2. The MC68030 will respond with a bus grant (BG*).
3. The MC68030 will deassert AS* and on board logic will deassert STERM*, DSACK1* and DSACK0*.
4. User supplied logic should then drive BGACK* and the MC68030 address and control signals. To invalidate the cache line, the WRITE* control signal must be asserted.
5. After the proper address setup time (25ns) is satisfied, the user supplied logic should drive AS* (address strobe) low.

6. For coherency cycles, AS* must remain asserted for at least 2 clocks. There is no maximum period for the assertion of AS*.
7. The user supplied logic can now deassert AS*.
8. After holding the address and control signals for 10ns, the user supplied logic should tristate these lines.
9. As soon as all address and control signals have been tristated, the user supplied logic should deassert BGACK*.

An invalidation (coherency cycle) occurs after AS* and WRITE* are asserted to indicate that a valid address has been presented on the MC68030 address bus. Upon receipt of AS*, the VALIDCLK signal from P102 will assert to clock P101 and force all four valid bits to 0 (invalid). The VALIDWE* will assert on the next clock to output enable the new validity bits from P101 and strobe the four new validity bits into the validity RAM. The cycle is complete when the external logic deasserts AS* and (one clock later) BGACK*. Refer to Figure 5.0, page 40, for the cache coherency timing. Note that there are address setup and hold times referenced to address strobe (AS*) which must be satisfied for proper operation.

On cache coherency cycles, external logic must drive all MC68030 signals including function codes, AS*, DS*, WRITE*, etc. Should the user want to implement a shared memory scheme through the MC68030 bus arbitration port; the function codes should be driven to valid values (1, 2, 5 or 6). If coherency only cycles are required, the function code should be driven to 0 which is not in shared memory space. The MC68030 function codes are defined below:

FC2	FC1	FC0	CODE	ADDRESS SPACE
0	0	0	0	Undefined, Reserved
0	0	1	1	User Data Space
0	1	0	2	User Program Space
0	1	1	3	Undefined, Reserved
1	0	0	4	Undefined, Reserved
1	0	1	5	Supervisor Data Space
1	1	0	6	Supervisor Program Space
1	1	1	7	CPU Space

50MHZ MC68030 OPERATION

At 50MHz, with current technology, the MC68030 can support a 3 clock cache read and a 3 clock write. In this configuration, retry operations on read misses are not necessary. To operate at 50MHz, the architecture of the current 33MHz design would require only minor changes to delete the retry cycle and the bus error/halt generation. In addition the STERM* signal would have to be generated based upon a cache read hit. However, the data paths, coherency logic, write pipeline and general architecture would remain unchanged. Refer to Appendix H for more information on 50MHz operation.

CONCLUSION

The cache architecture shown here demonstrates a zero wait state, 33MHz MC68030 shared memory design. The stringent timing characteristics of the 33MHz MC68030 requires an integrated approach to cache tags. The cache tag employed was the IDT6178S12, 12ns integrated CMOS cache tag RAM. The IDT6178S12 is both a speed and space efficient cache tag solution. The 12ns IDT6178S12 combines high speed RAM, compare and reset logic in a single package.

PAL equations can be obtained from IDT on PC format diskettes. Contact a Static RAM applications engineer at (408) 727-6116.

CREDITS

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APPENDIX A

LOADING ANALYSIS

LOADING ANALYSIS

PROJECT: IDT 33MHz 68030 CACHE
TYPE OF SIGNAL: ADDRESS BUS

Signal Name	Device U#	Type	Qty	I_{IH} SDT	I_{IL} (µA)	I_{OH} (mA)	I_{OL} (mA)	$C_{IN/OUT}$ (mA)	Driver Spec. (pF)	Load Cap. (pF)
A15–A4		IDT6178	5	D	50	0.05	-	-	35	-
		IDT6198	8	D	40	0.04	-	-	56	-
(Memory F/F)		74FCT373	1	D	5	-	-	-	10	-
(Coherency)		74ALS245	1	T	20	0.1	3.0	24.0	15	50
		68030	1	T	20	0.02	0.4	3.2	20	130
(A4 only)		68882	1	D	10	0.01	-	-	20	-
					145	0.22	0.4	3.2	156	
A31–A16		IDT6178	1	T	10	0.01	-	-	7	-
		74FCT373	1	D	5	-	-	-	10	-
		74ALS245	1	T	20	0.1	3.0	24.0	15	50
		68030	1	T	20	0.02	0.4	3.2	20	130
		PAL20L8-10	3	D	75	0.75	-	-	15	-
					130	0.88	0.4	3.2	67	
A3, A2		PAL20R4-10	2	D	50	0.5	-	-	10	-
		IDT6198	8	D	40	0.04	-	-	56	-
		74FCT373	1	D	5	-	-	-	10	-
		74ALS245	1	T	20	0.1	3.0	24.0	15	50
		68030	1	T	20	0.02	0.4	3.2	20	130
		68882	1	D	10	0.01	-	-	20	-
					145	0.67	0.4	3.2	131	
A1,A0		PAL20L8-10	1	D	25	0.25	-	-	5	-
		74ALS08	1	D	20	0.1	-	-	5	-
		74ALS245	1	T	20	0.1	3.0	24.0	15	50
		68030	1	T	20	0.02	0.4	3.2	20	130
(A1 only)		68882	1	D	10	0.01	-	-	20	-
					95	0.48	0.4	3.2	65	
D31–D0		IDT6198	1	T	5	0.005	4.0	8.0	7	30
		68030	1	T	20	0.02	0.4	3.2	20	130
		74FCT543	1	T	15	0.015	15	64	12	50
		68882	1	T	20	0.02	0.4	5.3	20	130
		74ALS245	1	T	20	0.1	3.0	24.0	15	50
					80	0.16	0.4	3.2	74	

NOTE 1: No current loading problems.
2: No Capacitive derating required on address bus.
3: Capacitance derating required:
- a) IDT6198 - 37pF excess capacitance +2ns
- b) 74FCT543 - 12pF excess capacitance +0.5ns
- c) 74ALS245 - 9pF excess capacitance +0.5ns

CAPACITIVE DERATING CALCULATIONS

a) At 0.05ns/pF the IDT6198 must be derated: 0.05 x 37 = 1.85ns ≈ 2ns
b) At 0.04ns/pF the 74FCT543 must be derated: 0.04 x 12 = 0.48ns ≈ 0.5ns
c) At 0.04ns/pF the 74ALS245 must be derated: 0.04 x 9 = 0.36ns ≈ 0.5ns

APPENDIX B

TIMING TABULATIONS

33MHZ MC68030 - CACHE TIMING

(2 CLOCK CACHE READ, 3 CLOCK CACHE WRITE)
~ - indicates a derated parameter.
CP - indicates common path analysis used.

IDT6198S25 CACHE DATA READ PARAMETERS:

1. 68030 Address to IDT6198 Data Valid:	ns	
1.5 clock @ 30ns:	45	
68030, t6, claock to address:	(14)	max
68030, t27, read data setup:	(1)	min
Data bus derating:	(2)	max
	28ns	

t_{AA} Required =25ns

2. PAL CACHEOE* to IDT6198 Data Valid:	ns	
1 clock @ 30ns:	30	
10ns PAL, clock to CACHEOE*:	(10)	max
68030, t27, read data setup:	(1)	min
Data bus derating:	(2)	max
Clock skew:	(2)	max
	15ns	

t_{OE} Required = 11ns

3. CACHE CS* to IDT6198 Data Valid:

Since the cache data ram chip select is grounded, this is not a limiting parameter.
t_{ACS} Required =25ns

4. 68030 AS* Negated to IDT6198 Data Invalid:	ns	
10ns PAL, clock to CACHEOE*:	3	min
IDT6198 CACHEOE* to data invalid:	2	min
	5ns	

MC68030 T29 Required = 0ns

IDT6198S25 CACHE DATA WRITE PARAMETERS:

5. 68030 Synchronous Data Hold:	ns	
68030, T12, clock to AS* negated:	0	min
10ns PAL, clock to CACHEOE*:	3	min
IDT6198 CACHEOE* to data invalid:	2	min
	5ns	

MC68030 T30 Required = 6ns

Note: Data hold time is satisfied by parameter #4 above. See MC68030 User's Manual note #12 on page 13-6.

6. 68030 Address Valid to IDT6198 Write Begin:	ns	
1.5 clock @ 30ns:	45	
10ns PAL, clock to CAWEx* low:	3	min
68030, t6, clock to address:	(14)	max
Clock skew:	(2)	max
	32ns	

t_{AS} Required = 0ns

7. 68030 Address Valid to IDT6198 Write End:	ns	
2.5 clocks @ 30ns:	75	
10ns PAL, clock to CAWEx* high:	3	min
68030, t6, clock to address:	(14)	max
Clock skew:	(2)	max
	62ns	

Taw Required = 20ns

7. IDT6198 Write Pulse Width:	ns	
1 clock @ 30ns:	30	
10ns PAL, clock to CAWEx* high:	3	min
10ns PAL, clock to CAWEx* low:	(10)	max
	23ns	

t_{WP} Required = 20ns

IDT6198S25 CACHE DATA WRITE PARAMETERS:

8. 68030 Data Valid to IDT6198 Write End:	ns	
1.5 clock @ 30ns:	45	
10ns PAL, clock to CAWEx* high:	3	min
68030, t23, clock to data:	(14)	max
Clock skew:	(2)	max
	32ns	

t_{DW} Required = 13ns

9. 68030 Data Hold to IDT6198 Write End:	ns	
0.5 clock @ 30ns:	15	
68030, t53, clock to data invalid:	2	min
10ns PAL, clock to CAWEx* high:	(10)	max
Clock skew:	(2)	max
	5ns	

t_{DH} Required = 0ns

IDT6178S12 CACHE TAG HIT/MISS PARAMETERS:

10. BERR*, HALT* Set up to Clock Low:	ns	
1.5 clocks @ 30ns:	45	
68030, t6, clock to address:	(14)	max
10ns PAL, MATCHx to BERR*, HALT*:	(10)	max
74F20, MATCHx to MATCH*:	(6)	max
68030, t27A, BERR*, HALT* setup:	(3)	min
	12ns	

t_{ADM} Required = 12ns (From IDT6178 address)
t_{DAM} Required = 11ns (From IDT6178 data)

11. BERR*, HALT* Set up to Clock Low: (from output enable, retry followed by read)	ns	
1.5 clocks @ 30ns:	45	
10ns PAL, clock to VALIDWE:	(10)	max
74F04, VALIDWE:	(5.3)	max
10ns PAL, MATCHx to BERR*, HALT*:	(10)	max
68030, t27A, BERR*, HALT* setup:	(3)	min
Clock skew:	(2)	max
	14.7ns	

t_{OE} Required = 8ns

IDT6178S12 CACHE TAG WRITE PARAMETERS:

12. Address valid to end of Write:
Not calculated but certainly not a problem.

Taw Required = 10ns

13. IDT6178 Write Pulse Width:	ns	
1 clocks @ 30ns:	30	
10ns PAL, clock to VALIDWE* high:	3	min
10ns PAL, clock to VALIDWE* low:	(10)	max
	23ns	

t_{WP} Required = 10ns

14. IDT6178 Data Valid to Write End:	ns	
1 clocks @ 30ns:	30	
10ns PAL, clock to VALIDWE* high:	3	min
10ns PAL, clock to VALIDWE* low:	(10)	max
10ns PAL, VALIDWE* to VALID0-3:	(10)	max
	13ns	

t_{DW} Required = 8ns

15. IDT6178 Data Hold after write:	ns	
10ns PAL, VALIDWE* to VALID0-3:	3	min
	3ns	

t_{DH} Required = 0ns

16. Address Setup to AS* low: (Coherency cycle)	ns	
Address setup to AS* low:	25	min
10ns PAL, AS* to VALIDCLK*:	3	min
74F04, VALIDCLK* to VALIDCLK:	2.4	min
74F20, MATCHx to MATCH*:	(6)	max
10ns PAL, MATCH* setup to VALIDCLK:	(10)	max
	14.4ns	

t_{ADM} Required = 12ns (From IDT6178 address)
t_{DAM} Required = 11ns (From IDT6178 data)

IDT6178S12 CACHE TAG WRITE PARAMETERS:

17. IDT6178 Address Hold after Write: (Retry cycle)	ns	
0.5 clocks @ 30ns:	15	
68030 t8, Address Hold:	0	min
10ns PAL, clock to VALIDWE* high:	(10)	max
	5ns	

t_{WR} Required = 0ns

18. IDT6178 Address Hold after Write: (Coherency cycle)	ns	
Address hold to AS* high:	10	min
10ns PAL, AS* to VALIDWE* high:	(10)	max
	0ns	

t_{WR} Required = 0ns

APPENDIX C

PAL EQUATIONS

(ABEL™ FORMAT)

```
Module P100
Title 'STERM*, Cacheable Access Gen.  Rev A 08/04/89
Integrated Device Technology Inc.   U2  IDT68030
20L8-10 (10nS)'

p100      Device    'P20L8';

FC2       Pin       1;        "I"         VCC                   Pin     24;
FC1       Pin       2;        "I"         CPUCLK_       Pin     23;     "I"
FC0       Pin       3;        "I"         CACHEN_       Pin     22;     "O"
A31       Pin       4;        "I"         STERM_        Pin     21;     "T"
A30       Pin       5;        "I"         CIIN_         Pin     20;     "T"
A29       Pin       6;        "I"         NC19          Pin     19;     "T"
A28       Pin       7;        "I"         NC18          Pin     18;     "T"
AS_       Pin       8;        "I"         TERMAK_       Pin     17;     "T"
WRITE_    Pin       9;        "I"         CACHDS_       Pin     16;     "T"
RMC_      Pin       10;       "I"         MEMCS_        Pin     15;     "O"
CIOUT_    Pin       11;       "I"         RETRY_        Pin     14;     "I"
GND       Pin       12;                   BGACK_        Pin     13;     "I"

" TERMINOLOGY:
" 1 -     _ at the end of a signal name denotes an active low signal.
" 2 -     !         = Boolean NOT function.
" 3 -     #         = Boolean OR function.
" 4 -     &         = Boolean AND function.
" 5 -     !=        = Not equal to.
" 6 - !AS_          = Active low signal AS_, asserted or on state.
" 7 - CPUCLK        = Active high signal, CPUCLK, asserted or on state.
" 8 -     ;         = end of equation.

" Definitions:

ADDRESS = [A31,A30,A29,A28];            " 68030 address bits A31-A28.

FCODE    = [FC2,FC1,FC0];               " 68030 function code.

@RADIX 16;                              " Change to hex default.

Equations

!STERM_ =                               " 68030 Synchronous Termination.
(ADDRESS == 0) & (FCODE == 1)       &   " Address range: 0000 0000 - 0FFF FFFF,
CIOUT_ & WRITE_ & RMC_ & RETRY_     &   " Cache not inhibited, no read-modify-
CACHDS_                             #   " write, no retry, read cycle, cache
                                        " enabled, User Data Space.

(ADDRESS == 0) & (FCODE == 2)       &   " Address range: 0000 0000 - 0FFF FFFF,
CIOUT_ & WRITE_ & RMC_ & RETRY_     &   " Cache not inhibited, no read-modify-
CACHDS_                             #   " write, no retry, read cycle, cache
                                        " enabled, User Program Space.

(ADDRESS == 0) & (FCODE == 5)       &   " Address range: 0000 0000 - 0FFF FFFF,
CIOUT_ & WRITE_ & RMC_ & RETRY_     &   " Cache not inhibited, no read-modify-
CACHDS_                             #   " write, no retry, read cycle, cache
                                        " enabled, Supervisor Data Space.

(ADDRESS == 0) & (FCODE == 6)       &   " Address range: 0000 0000 - 0FFF FFFF,
CIOUT_ & WRITE_ & RMC_ & RETRY_     &   " Cache not inhibited, no read-modify-
CACHDS_                             #   " write, no retry, read cycle, cache
                                        " enabled, Supervisor Program Space.

CPUCLK_ & !TERMAK_ & !AS_           #   " Assert STERM_ for 2nd cycle of retry
                                        " or for write cycles.

!STERM_ & !AS_                      ;   " Hold STERM_ asserted while AS_ is on.

!CACHEN_ =                              " Cacheable Cycle.
(ADDRESS == 0) & (FCODE == 1)       &   " Address range: 0000 0000 - 0FFF FFFF,
CIOUT_ & RMC_ & CACHDS_             &   " Cache not inhibited, no read-modify-
BGACK_                              #   " write, cache enabled, no other
                                        " bus master, User Data Space.

(ADDRESS == 0) & (FCODE == 2)       &   " Address range: 0000 0000 - 0FFF FFFF,
CIOUT_ & RMC_ & CACHDS_             &   " Cache not inhibited, no read-modify-
BGACK_                              #   " write, cache enabled, no other
                                        " bus master, User Program Space.

(ADDRESS == 0) & (FCODE == 5)       &   " Address range: 0000 0000 - 0FFF FFFF,
CIOUT_ & RMC_ & CACHDS_             &   " Cache not inhibited, no read-modify-
BGACK_                              #   " write, cache enabled, no other
                                        " bus master, Supervisor Data Space.

(ADDRESS == 0) & (FCODE == 6)       &   " Address range: 0000 0000 - 0FFF FFFF,
CIOUT_ & RMC_ & CACHDS_             &   " Cache not inhibited, no read-modify-
BGACK_    ;                             " write, cache enabled, no other
                                        " bus master, Supervisor Program Space.

!MEMCS_ =                               " 68030 Main Memory Chip Select.
(ADDRESS == 0) & (FCODE == 1)       #   " Address range: 0000 0000 - 0FFF FFFF,
                                        " User Data Space.

(ADDRESS == 0) & (FCODE == 2)       #   " Address range: 0000 0000 - 0FFF FFFF,
                                        " User Program Space.

(ADDRESS == 0) & (FCODE == 5)       #   " Address range: 0000 0000 - 0FFF FFFF,
                                        " Supervisor Data Space.

(ADDRESS == 0) & (FCODE == 6)       ;   " Address range: 0000 0000 - 0FFF FFFF,
                                        " Supervisor Program Space.

!CIIN_ =                                " Cache inhibit in.
(ADDRESS != 0)                      #   " Address range: 1000 0000 - FFFF FFFF,
(FCODE    == 7)                     #   " CPU Space function code.
(FCODE    == 4)                     #   " Undefined function code.
(FCODE    == 3)                     #   " Undefined function code.
(FCODE    == 0)                     ;   " Undefined function code.
```

```
"*********************** Description ***********************
" This PAL generates the 68030 synchronous terminate signal, STERM_
" and the cache enable signal, CACHEN_.  The address range dedicated
" cacheable memory is 0000 0000 - 0FFF FFFF or 268M bytes (1/16 of
" the 68030 address space).  STERM_ will assert asynchronously based
" on address.  Once it has asserted, the 68030 address strobe will
" hold it on until the end of the cycle.
"
" The CACHDS_ signal is a jumper selectable external cache disable.
" If the jumper, JP3 is installed, the external cache is disabled.
"
" The CACHEN_ signal indicates that a cacheable cycle is in progress.
"
" The MEMCS_ signal is the main memory chip select output.  It is used
" to indicate that the 68030 address has selected main memory space.
"
" The cache inhibit signal, CIIN_ asserts to force the MC68030 to not
" cache (internally) the current cycle.  This signal asserts during
" non-memory cycles or for CPU space and undefined function codes.
"
"********************* Revision History *********************
" Rev A - Logic Innovations, Inc., FJC - 08/04/89.
" New Release.  First Version.
"
End P100;
```

```
Module P101
Title `Validity RAM Control   Rev A 08/04/89
Integrated Device Technology Inc.   U4  IDT68030
20R4-10 (10nS)'

p101       Device     `P20R4';

CLK        Pin        1;                    VCC         Pin       24;
A3         Pin        2;        "I"         VALID0      Pin       23;       "I"
A2         Pin        3;        "I"         HIT_        Pin       22;       "T"
AS_        Pin        4;        "I"         NC21        Pin       21;       "T"
CACHEN_    Pin        5;        "I"         NVLD3       Pin       20;       "R"
MATCH3     Pin        6;        "I"         NVLD2       Pin       19;       "R"
MATCH2     Pin        7;        "I"         NVLD1       Pin       18;       "R"
MATCH1     Pin        8;        "I"         NVLD0       Pin       17;       "R"
MATCH0     Pin        9;        "I"         MATCH_      Pin       16;       "T"
VALID3     Pin        10;       "I"         WRITE_      Pin       15;       "T"
VALID2     Pin        11;       "I"         VALID1      Pin       14;       "I"
GND        Pin        12;                   OE_         Pin       13;

" TERMINOLOGY:
" 1 -      _ at the end of a signal name denotes an active low signal.
" 2 -      !          = Boolean NOT function.
" 3 -      #          = Boolean OR function.
" 4 -      &          = Boolean AND function.
" 5 - !AS_            = Active low signal AS_, asserted or on state.
" 6 - CPUCLK          = Active high signal, CPUCLK, asserted or on state.
" 7 -      ;          = end of equation.

Equations

NVLD3 :=                                    " New LW # 3 validity bit (offset = C).
A3 & A2 & !CACHEN_                      #   " Set validity bit for LW # 3.

VALID3 & !A3 & !CACHEN_ & !MATCH_       #   " Hold validity bit for LW # 0, 1.

VALID3 & !A2 & !CACHEN_ & !MATCH_       ;   " Hold validity bit for LW # 0, 2.

NVLD2 :=                                    " New LW # 2 validity bit (offset = 8).
A3 & !A2 & !CACHEN_                     #   " Set validity bit for LW # 2.

VALID2 & !A3 & !CACHEN_ & !MATCH_       #   " Hold validity bit for LW # 0, 1.

VALID2 & A2 & !CACHEN_ & !MATCH_        ;   " Hold validity bit for LW # 1, 3.

NVLD1 :=                                    " New LW # 1 validity bit (offset = 4).
!A3 & A2 & !CACHEN_                     #   " Set validity bit for LW # 1.

VALID1 & A3 & !CACHEN_ & !MATCH_        #   " Hold validity bit for LW # 2, 3.

VALID1 & !A2 & !CACHEN_ & !MATCH_       ;   " Hold validity bit for LW # 0, 2.

NVLD0 :=                                    " New LW # 0 validity bit (offset = 0).
!A3 & !A2 & !CACHEN_                    #   " Set validity bit for LW # 0.

VALID0 & A3 & !CACHEN_ & !MATCH_        #   " Hold validity bit for LW # 2, 3.

VALID0 & A2 & !CACHEN_ & !MATCH_        ;   " Hold validity bit for LW # 1, 3.



!HIT_ =                                     " Cache hit: read or write.
MATCH3 & MATCH2 & MATCH1 & MATCH0       &   " Tag Matches,
A3 & A2 & VALID3 & !AS_ & !CACHEN_      #   " Longord # 3 and valid 3.

MATCH3 & MATCH2 & MATCH1 & MATCH0       &   " Tag Matches,
A3 & !A2 & VALID2 & !AS_ & !CACHEN_     #   " Longord # 2 and valid 2.

MATCH3 & MATCH2 & MATCH1 & MATCH0       &   " Tag Matches,
!A3 & A2 & VALID1 & !AS_ & !CACHEN_     #   " Longord # 1 and valid 1.

MATCH3 & MATCH2 & MATCH1 & MATCH0       &   " Tag Matches,
!A3 & !A2 & VALID0 & !AS_ & !CACHEN_    ;   " Longord # 0 and valid 0.

************************* Description ***********************
" This PAL generates the HIT_ (cache hit) signal and the updated
" validity bits for writing into the validity RAM on retry cycles
" (cacheable read miss).  Validity bits which are not selected are
" unmodified.  This PAL is clocked at the beginning of the retry
" cycle and at the start of the coherency cycle.
"
*********************** Revision History ********************
" Rev A - Logic Innovations, Inc., FJC - 08/04/89.
" New Release.  First Version.
"
End P101;
```

```
Module P102
Title `Retry, Bus Error, Halt Rev A 08/04/89
Integrated Device Technology Inc.   U6  IDT68030
20L8-10 (10nS)'

p102       Device     `P20L8';

A3         Pin        1;        "I"         VCC         Pin       24;
A2         Pin        2;        "I"         VALID0      Pin       23;       "I"
AS_        Pin        3;        "I"         NC22        Pin       22;       "O"
CACHEN_    Pin        4;        "I"         BERR_       Pin       21;       "T"
MATCH_     Pin        5;        "I"         HALT_       Pin       20;       "T"
CPUCLK_    Pin        6;        "I"         RETRY_      Pin       19;       "T"
RTRYCR_    Pin        7;        "I"         RTRYHD_     Pin       18;       "T"
BERRIN_    Pin        8;        "I"         VLDCLK_     Pin       17;       "T"
HALTIN_    Pin        9;        "I"         BGACK_      Pin       16;       "T"
WRITE_     Pin        10;       "I"         NC15        Pin       15;       "O"
VALID3     Pin        11;       "I"         VALID1      Pin       14;       "I"
GND        Pin        12;                   VALID2      Pin       13;       "I"

" TERMINOLOGY:

" 1 -      _ at the end of a signal name denotes an active low signal.
" 2 -      !          = Boolean NOT function.
" 3 -      #          = Boolean OR function.
" 4 -      &          = Boolean AND function.
" 5 - !AS_            = Active low signal AS_, asserted or on state.
" 6 - CPUCLK          = Active high signal, CPUCLK, asserted or on state.
" 7 -      ;          = end of equation.

Equations

!RETRY_ =                                   " Retry this cycle!
!CACHEN_ & WRITE_                       &   " Retry cacheable read,
!BERR_    & !HALT_ & RTRYCR_            #   " Bus error and halt asserted, clock low,
                                            " retry clear not asserted.
!RETRY_ & RTRYCR_ & !AS_                #   " Hold on while address strobe on.
!RETRY_ & RTRYCR_ & !RTRYHD_            #   " Hold on while retry hold asserted.
!RETRY_ & RTRYCR_ & CPUCLK_             ;   " Hold on 1/2 clock.

!RTRYHD_ =                                  " Retry Hold.
!CACHEN_ & WRITE_                       &   " Assert on cacheable read,
!BERR_    & !HALT_ & RTRYCR_            #   " Bus error and halt asserted, clock low,
                                            " retry clear not asserted.
!RTRYHD_ & RTRYCR_ & CPUCLK_            #   " Hold on while clock low.
!RTRYHD_ & RTRYCR_ & AS_                ;   " Hold on until address strobe of
                                            " retried cycle.

!VLDCLK_ =                                  " Validity PAL (P101) clock,
!RETRY_ & !RTRYHD_                      #   " Assert on retry and retry hold.
!VLDCLK_ & !AS_                         #   " Hold while address strobe on.
!VLDCLK_ & CPUCLK_                      #   " Hold while clock low.
!BGACK_ & !AS_ & !WRITE_                #   " Assert on coherency cycles.
!VLDCLK_ & !BGACK_                      ;   " Hold til coherency cycle done.

!HALT_ =                                    " 68030 Halt signal.
                                            " Asserted with bus error to
                                            " force a retry cycle.
!AS_ & !CACHEN_ & WRITE_                &   " Assert on cacheable read
MATCH_    & RETRY_                      #   " and no tag match.

!AS_ & !CACHEN_ & WRITE_                &   " Assert on cacheable read,
A3 & A2   & !VALID3 & RETRY_            #   " LW # 3 and not valid.

!AS_ & !CACHEN_ & WRITE_                &   " Assert on cacheable read,
!A3 & A2  & !VALID2 & RETRY_            #   " LW # 2 and not valid.

!AS_ & !CACHEN_ & WRITE_                &   " Assert on cacheable read,
!A3 & A2  & !VALID1 & RETRY_            #   " LW # 1 and not valid.

!AS_ & !CACHEN_ & WRITE_                &   " Assert on cacheable read,
!A3 & !A2 & !VALID0 & RETRY_            #   " LW # 0 and not valid.

!HALTIN_ & !AS_                         ;   " Assert on HALT in.


!BERR_ =                                    " 68030 bus error signal.
                                            " Asserted with HALT to
                                            " force a retry cycle.
!AS_ & !CACHEN_ & WRITE_                &   " Assert on cacheable read
MATCH_    & RETRY_                      #   " and no tag match.

!AS_ & !CACHEN_ & WRITE_                &   " Assert on cacheable read,
A3 & A2   & !VALID3 & RETRY_            #   " LW # 3 and not valid.

!AS_ & !CACHEN_ & WRITE_                &   " Assert on cacheable read,
!A3 & A2  & !VALID2 & RETRY_            #   " LW # 2 and not valid.

!AS_ & !CACHEN_ & WRITE_                &   " Assert on cacheable read,
!A3 & A2  & !VALID1 & RETRY_            #   " LW # 1 and not valid.

!AS_ & !CACHEN_ & WRITE_                &   " Assert on cacheable read,
!A3 & !A2 & !VALID0 & RETRY_            #   " LW # 0 and not valid.

!BERRIN_ & !AS_                         ;   " Assert on bus error in.


************************* Description *************************
" This PAL generates the RETRY_ signal which serves as a cache
" read miss and memory read request indicator.  The RETRY_ signal
" asserts in state 3 of the 68030 read miss cycle and holds on
" until the end of the retried cycle.
"
" Retry hold (RTRYHD_) serves to hold on retry during the idle states
" between the 1st and 2nd cycles of the retry.  This signal is used
" inside this PAL only for feedback.  Pin 18 must remain unconnected
" on the schematic.
"
" BERR_ and HALT_ are the 68030 bus error and halt signals respectively.
" These signals are simultaneously asserted to force a 68030 retry cycle.
```

```
" The BERRIN_ signal is an externally generated input for bus error.
" The HALTIN_ signal is an externally generated input for halt.
"
" The VLDCLK signal (new validity bit clock) is used to both output
" enable the validity RAM and clock PAL - P101 to generate the new
" validity bits for either the update or the coherency cycle.
"
"*********************** Revision History ***********************
" Rev A - Logic Innovations, Inc., FJC - 08/04/89.
" New Release.  First Version.
"
End P102;
```

```
Module P103
Title 'Cache Data RAM Write Control Rev A   08/04/89
Integrated Device Technology Inc.   U21 IDT68030
20L8-10 (10nS)'

p103      Device    'P20L8';
A1        Pin       1;       "I"       VCC        Pin     24;
A0        Pin       2;       "I"       NC23       Pin     23;     "I"
SIZ1      Pin       3;       "I"       NC22       Pin     22;     "O"
SIZ0      Pin       4;       "I"       STATE2_    Pin     21;     "T"
CPUCLK    Pin       5;       "I"       STATE3_    Pin     20;     "T"
CACHEN_   Pin       6;       "I"       CAWE3_     Pin     19;     "T"
WRITE_    Pin       7;       "I"       CAWE2_     Pin     18;     "T"
MEMACK_   Pin       8;       "I"       CAWE1_     Pin     17;     "T"
HIT_      Pin       9;       "I"       CAWE0_     Pin     16;     "T"
AS_       Pin       10;      "I"       UPDATE_    Pin     15;     "O"
PIPEFL_   Pin       11;      "I"       UPDTIN_    Pin     14;     "I"
GND       Pin       12;                NC13       Pin     13;     "I"

" TERMINOLOGY:
" 1 -      _ at the end of a signal name denotes an active low signal.
" 2 -      !         = Boolean NOT function.
" 3 -      #         = Boolean OR function.
" 4 -      &         = Boolean AND function.
" 5 - !AS_           = Active low signal AS_, asserted or on state.
" 6 - CPUCLK         = Active high signal, CPUCLK, asserted or on state.
" 7 -      ;         = end of equation.

Equations

!STATE2_ =                              " 030 State 2.  On for 030 states 2 & 3.
STATE3_ & CPUCLK & !AS_             #   " Assert on address strobe & clock > H.
!STATE2_ & !CPUCLK & !AS_           #   " Hold (Latch) while clock low.
!STATE2_ & STATE3_ & !AS_           ;   " Transition term.  Hold output
                                        " while clock switches H > L.

!STATE3_ =                              " 030 State 3.  On for 030 states 3 & up.
!STATE2_ & !CPUCLK & !AS_           #   " Assert on address strobe & clock > L.
!STATE3_  & !AS_                    ;   " Hold output while address strobe on.

!UPDATE_ =                              " Update cycle (Read miss).
!MEMACK_ & CPUCLK & PIPEFL_         &   " Assert on memory ack & clock > H.
!CACHEN_ & WRITE_                   #
!UPDTIN_ & !CPUCLK & PIPEFL_        &   " Hold (Latch) output while clock low.
!CACHEN_ & WRITE_                   #
!UPDTIN_ & !MEMACK_ & PIPEFL_       &   " Transition term.  Hold output
!CACHEN_ & WRITE_                   ;   " while clock switches H > L.


!CAWE0_ =                               " Data cache byte 0 write enable.
!A1 & !A0                           &   " Any size: byte 0,
!HIT_ & !WRITE_ & !CACHEN_          &   " Cacheable write hit,
!CPUCLK & !AS_ & !STATE2_           #   " assert in 030 state 3, clock low.

!CAWE0_ & CPUCLK                    #   " Hold output while clock is high.

!CAWE0_ & !STATE2_                  #   " Hold output while clock STATE2_ is on.

!UPDTIN_                            ;   " Assert all write enables on cache update.

!CAWE1_ =                               " Data cache byte 1 write enable.
!SIZ1 & SIZ0 & !A1 & A0             &   " Size = byte: byte 1,
!HIT_ & !WRITE_ & !CACHEN_          &   " Cacheable write hit,
!CPUCLK & !AS_ & !STATE2_           #   " assert in 030 state 3, clock low.

SIZ1 & !SIZ0 & !A1                  &   " Size = word: bytes 0-1 or 1-2 (UAT).
!HIT_ & !WRITE_ & !CACHEN_          &   " Cacheable write hit,
!CPUCLK & !AS_ & !STATE2_           #   " assert in 030 state 3, clock low.

SIZ1 & SIZ0 & !A1                   &   " Size = 3 byte: bytes 0-2, or 1-3.
!HIT_ & !WRITE_ & !CACHEN_          &   " Cacheable write hit,
!CPUCLK & !AS_ & !STATE2_           #   " assert in 030 state 3, clock low.

!SIZ1 & !SIZ0 & !A1                 &   " Size = 4 byte: bytes 0-3 or 1-3 (UAT).
!HIT_ & !WRITE_ & !CACHEN_          &   " Cacheable write hit,
!CPUCLK & !AS_ & !STATE2_           #   " assert in 030 state 3, clock low.

!CAWE1_ & CPUCLK                    #   " Hold output while clock is high.

!CAWE1_ & !STATE2_                  #   " Hold output while clock STATE2_ is on.

!UPDTIN_                            ;   " Assert all write enables on cache update.


!CAWE2_ =                               " Data cache byte 2 write enable.
!SIZ1 & SIZ0 & A1 & !A0             &   " Size = byte: byte 2.
!HIT_ & !WRITE_ & !CACHEN_          &   " Cacheable write hit,
!CPUCLK & !AS_ & !STATE2_           #   " assert in 030 state 3, clock low.

SIZ1 & !SIZ0 & !A1 & A0             &   " Size = word: bytes 1-2.
!HIT_ & !WRITE_ & !CACHEN_          &   " Cacheable write hit,
!CPUCLK & !AS_ & !STATE2_           #   " assert in 030 state 3, clock low.

SIZ1 & !SIZ0 & A1 & !A0             &   " Size = word: byte 2-3.
!HIT_ & !WRITE_ & !CACHEN_          &   " Cacheable write hit,
!CPUCLK & !AS_ & !STATE2_           #   " assert in 030 state 3, clock low.

SIZ1 & SIZ0 & !A1                   &   " Size = 3 byte: bytes 0-2, or 1-3.
!HIT_ & !WRITE_ & !CACHEN_          &   " Cacheable write hit,
!CPUCLK & !AS_ & !STATE2_           #   " assert in 030 state 3, clock low.

SIZ1 & SIZ0 & A1 & !A0              &   " Size = 3 byte: bytes 2-3.
!HIT_ & !WRITE_ & !CACHEN_          &   " Cacheable write hit,
!CPUCLK & !AS_ & !STATE2_           #   " assert in 030 state 3, clock low.

!SIZ1 & !SIZ0 & !A1                 &   " Size = 4 byte: bytes 0-3 or 1-3 (UAT).
!HIT_ & !WRITE_ & !CACHEN_          &   " Cacheable write hit,
!CPUCLK & !AS_ & !STATE2_           #   " assert in 030 state 3, clock low.

!SIZ1 & !SIZ0 & A1 & !A0            &   " Size = 4 byte: bytes 2-3.
```

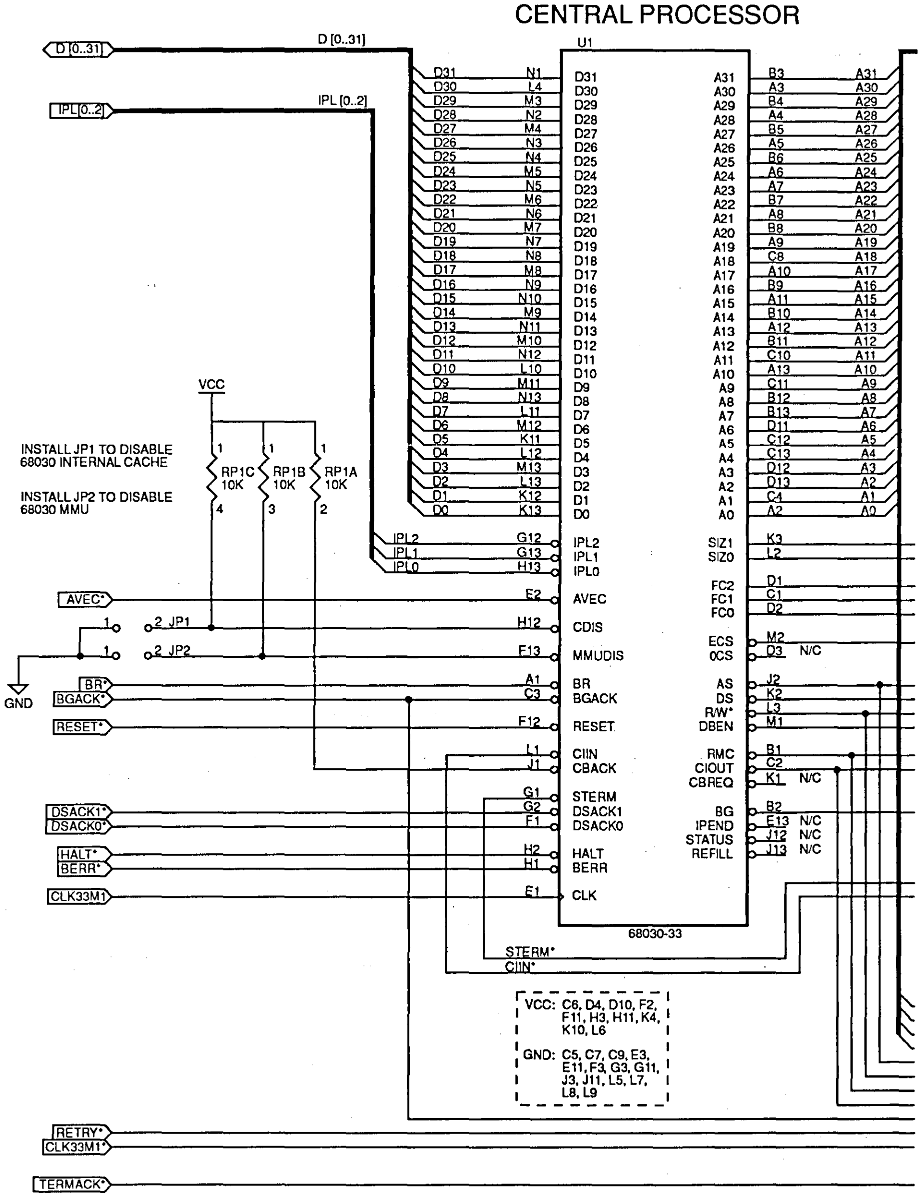
```
!HIT_ & !WRITE_ & !CACHEN_              &   " Cacheable write hit,
!CPUCLK & !AS_ & !STATE2_               #   " assert in 030 state 3, clock low.

!CAWE2_ & CPUCLK                        #   " Hold output while clock is high.

!CAWE2_ & !STATE2_                      #   " Hold output while clock STATE2_ is on.

!UPDTIN_                                ;   " Assert all write enables on cache update.


!CAWE3_ =                                   " Data cache byte 3 write enable.
!SIZ1 & SIZ0 & A1 & A0                  &   " Size = byte: byte 3.
!HIT_ & !WRITE_ & !CACHEN_              &   " Cacheable write hit,
!CPUCLK & !AS_ & !STATE2_               #   " assert in 030 state 3, clock low.

SIZ1 & !SIZ0 & A1                       &   " Size = word: bytes 2-3 or byte 3.
!HIT_ & !WRITE_ & !CACHEN_              &   " Cacheable write hit,
!CPUCLK & !AS_ & !STATE2_               #   " assert in 030 state 3, clock low.

SIZ1 & SIZ0 & !A1 & A0                  &   " Size = 3 byte: bytes 1-3.
!HIT_ & !WRITE_ & !CACHEN_              &   " Cacheable write hit,
!CPUCLK & !AS_ & !STATE2_               #   " assert in 030 state 3, clock low.

SIZ1 & SIZ0 & A1                        &   " Size = 3 byte: byte 3 or bytes 2-3.
!HIT_ & !WRITE_ & !CACHEN_              &   " Cacheable write hit,
!CPUCLK & !AS_ & !STATE2_               #   " assert in 030 state 3, clock low.

!SIZ1 & !SIZ0                           &   " Size = 4 byte: all offsets.
!HIT_ & !WRITE_ & !CACHEN_              &   " Cacheable write hit,
!CPUCLK & !AS_ & !STATE2_               #   " assert in 030 state 3, clock low.

!CAWE3_ & CPUCLK                        #   " Hold output while clock is high.

!CAWE3_ & !STATE2_                      #   " Hold output while clock STATE2_ is on.

!UPDTIN_                                ;   " Assert all write enables on cache update.

"************************ Description ************************
" This PAL generates the data cache write enables, the cache update
" signal (for cacheable read misses), and the 030 state tracking
" signals STATE2_ and STATE3_.  On write hits, only the selected byte
" is written.  On cacheable read miss cycles (retried), the assertion
" of the memory acknowledge signal, MEMACK_, causes the UPDATE_ signal
" to assert --- which in turn forces all cache write enables to assert.
" Read miss/update cycles are always four byte operations.
"
" The STATE2_ signal asserts for one full 030 clock cycle --- starting
" in 030 state 2 and ending in 030 state 3.  The STATE3_ signal asserts
" in 030 state 3 and holds on till the 030 address strobe AS_ goes away.
"********************** Revision History *********************
" Rev A - Logic Innovations, Inc., FJC - 08/04/89.
" New Release.  First Version.
"
End P103;
```

```
Module P104
Title 'Cache Validity RAM Control   Rev A   08/04/89
Integrated Device Technology Inc.   U24 IDT68030
16L8-10 (10nS)'

p104      Device     'P16L8';

UPDATE_   Pin        1;        "I"          VCC          Pin       20;
CPUCLK    Pin        2;        "I"          RTRYCR_      Pin       19;      "O"
CACHEN_   Pin        3;        "I"          VALDWE_      Pin       18;      "T"
WRITE_    Pin        4;        "I"          TAGWE_       Pin       17;      "T"
AS_       Pin        5;        "I"          CACHOE_      Pin       16;      "T"
RETRY_    Pin        6;        "I"          MEMROE_      Pin       15;      "T"
RESET_    Pin        7;        "I"          STATE2_      Pin       14;      "T"
BGACK_    Pin        8;        "I"          MEMCS_       Pin       13;      "T"
MATCH_    Pin        9;        "I"          NC12         Pin       12;      "O"
GND       Pin        10;                    BERR_        Pin       11;      "I"

" TERMINOLOGY:
" 1 -       _ at the end of a signal name denotes an active low signal.
" 2 -       !         = Boolean NOT function.
" 3 -       #         = Boolean OR function.
" 4 -       &         = Boolean AND function.
" 5 - !AS_            = Active low signal AS_, asserted or on state.
" 6 - CPUCLK          = Active high signal, CPUCLK, asserted or on state.
" 7 -       ;         = end of equation.

Equations

!RTRYCR_ =                                  " Retry clear.
!AS_ & !RETRY_ & !BERR_ & CPUCLK        #   " Clear on bus error.
!RESET_                                 #   " Clear on reset.
!BGACK_                                 ;   " Clear on CPU bus granted to
                                            " another master.

!TAGWE_ =                                   " TAG RAM Write enable.
!RETRY_ & !UPDATE_ & !CPUCLK            #   " Assert on retry cycle, after update.
!TAGWE_ & !UPDATE_ & !RETRY_            #   " Hold while Update asserted.
!TAGWE_ & !RETRY_ & CPUCLK              ;   " Hold while clock high.

!VALDWE_ =                                  " Validity RAM Write Enable.
                                            " Also controls output enable to new
                                            " validity bits.
!RETRY_ & !UPDATE_ & !CPUCLK            #   " Assert on retry cycle, after update.
!VALDWE_ & !UPDATE_ & !RETRY_           #   " Hold while Update asserted.
!VALDWE_ & !RETRY_ & CPUCLK             #   " Hold while clock high.

!BGACK_ & !AS_      & !WRITE_           &   " Invalidate all validity bits
!MATCH_ & !STATE2_ & !CPUCLK            #   " on coherency checks.

!VALDWE_ & !BGACK_ & !AS_               ;   " Hold til address strobe gone on
                                            " coherency cycles.
!CACHOE_ =                                  " Data cache read output enable.
!CPUCLK & WRITE_                        &   " Assert on all reads, not yet state 2,
RETRY_ & STATE2_ & BGACK_               #   " no retry, no other local bus master.
!CACHOE_ & !AS_ & WRITE_                &   " Hold on till AS_ goes away,
!CACHEN_                                ;   " and cacheable read.

!MEMROE_ =                                  " Memory read data bµffer enable.
!AS_ & CACHEN_ & CACHOE_                &   " Assert on noncacheable read
WRITE_ & !STATE2_ & !CPUCLK             #   " cycles.

!UPDATE_ & !CACHEN_ & CACHOE_           &   " Assert on cacheable read miss
WRITE_ & !RETRY_                        #   " (retry) cycles.

!AS_ & !CACHEN_ & CACHOE_               &   " Assert on cacheable read miss
WRITE_ & !RETRY_                        #   " (retry) cycles.

!MEMROE_ & !AS_                         ;   " Hold til address strobe gone.

"************************ Description ************************
" This PAL generates the Tag RAM write enable, the Valid RAM write
" enable, and the data cache read bµffer enable.  The Valid RAM write
" enable also serves as the output enable for the updated validity
" bits stored in P101.
"
" The CACHOE_ signal output enables the data cache on read cycles.
" It asserts on all reads in state 1 and will stay on for read hits
" and go off for other cycles.
"
" The MEMROE_ output enables the memory read data onto the
" cache/MC68030 data bus on noncacheable read or read miss
" cycles.
"
" The RTRYCR_ signal (retry clear) forces the retry signal generated
" in P102 to turn off.  RTRYCR_ is generated on a bus error during
" a retried cycle, a reset, or an alternate master bus cycle.
"
"********************** Revision History *********************
" Rev A - Logic Innovations, Inc., FJC - 08/04/89.
" New Release.  First Version.
"
End P104;
```

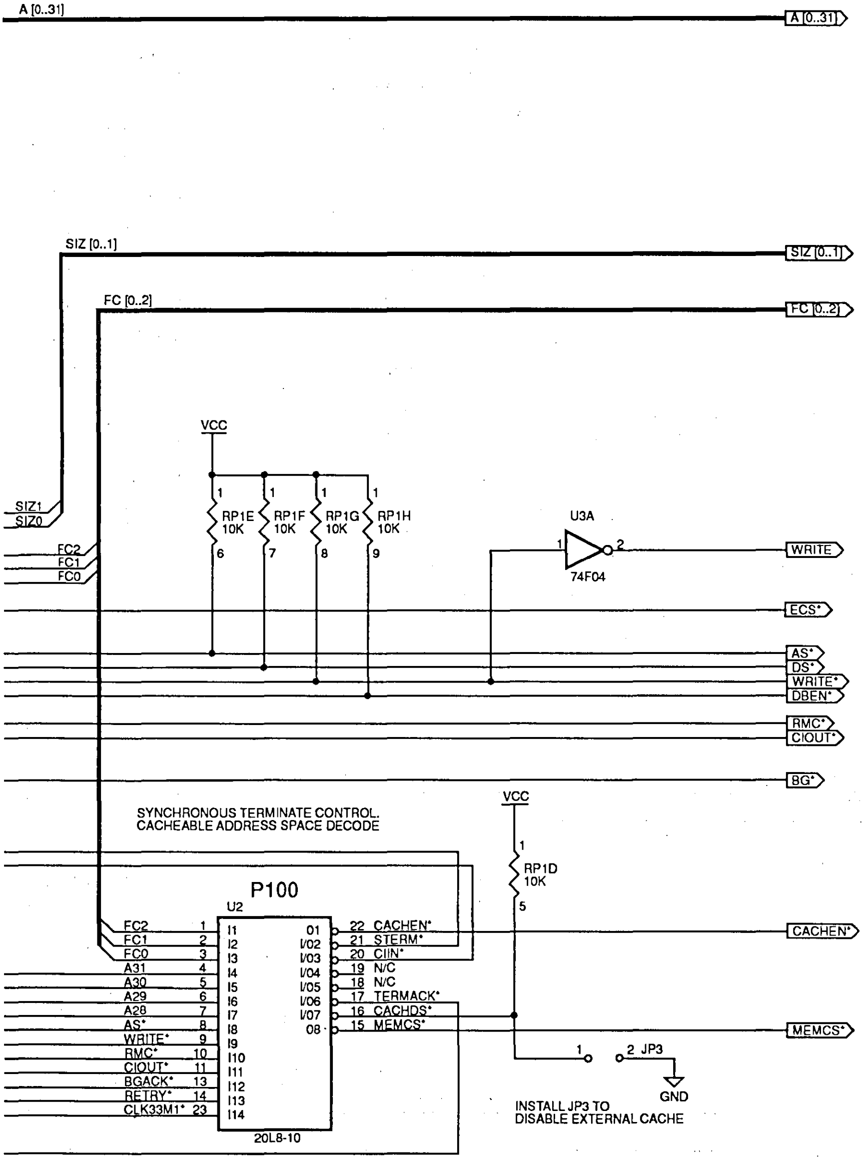
```
Module P105
Title 'Write Pipline, ack.  Control Rev A   08/04/89
Integrated Device Technology Inc.   U25 IDT68030
16R4-10 (10nS)'

p105      Device    'P16R4';

CLK_      Pin       1;                       VCC     Pin     20;
CPUCLK_   Pin       2;         "I"           TERMAK_         Pin       19;       "T"
WRITE_    Pin       3;         "I"           NC18            Pin       18;       "T"
AS_       Pin       4;         "I"           PIPEFL_         Pin       17;       "R"
MEMACK_   Pin       5;         "I"           WRTPND_         Pin       16;       "R"
RETRY_    Pin       6;         "I"           NC15            Pin       15;       "R"
RESET_    Pin       7;         "I"           NC14            Pin       14;       "R"
MEMCS_    Pin       8;         "I"           NC13            Pin       13;       "T"
MEMERR_   Pin       9;         "I"           NC12            Pin       12;       "T"
GND       Pin       10;                          OE_         Pin       11;

" TERMINOLOGY:
" 1 -      _ at the end of a signal name denotes an active low signal.
" 2 -      !          = Boolean NOT function.
" 3 -      #          = Boolean OR function.
" 4 -      &          = Boolean AND function.
" 5 - !AS_            = Active low signal AS_, asserted or on state.
" 6 - CPUCLK          = Active high signal, CPUCLK, asserted or on state.
" 7 -      ;          = end of equation.

Equations

!TERMAK_ =                                " Terminate acknowledge.  Assert
                                          " this output to generate STERM*.
!AS_      & !WRITE_ & !MEMCS_        &    " Assert on memory write and
!CPUCLK_ & PIPEFL_ & WRTPND_         #    " write pipeline empty.

!AS_      & !WRITE_ & !MEMCS_        &    " Assert on memory write and
!CPUCLK_ & !PIPEFL_ & !WRTPND_       &    " write pipeline just emptied.
!MEMACK_                             #    " Used for successive write cycles.

!RETRY_ & WRITE_ & !MEMCS_           &    " Assert on cache miss/retry (read)
!CPUCLK_ & PIPEFL_ & !MEMACK_        #    " cycle and write pipeline empty.

!AS_      & WRITE_ & !MEMCS_         &    " Assert on memory read (noncacheable)
!CPUCLK_ & PIPEFL_ & !MEMACK_        #    " and write pipeline empty.

!TERMAK_ & !AS_                      ;    " Hold til address strobe gone.

!PIPEFL_ :=                               " Write pipeline full.
!AS_      & !WRITE_ & !MEMCS_        &    " Assert on memory write and
PIPEFL_ & MEMERR_                    #    " write pipeline empty.

!PIPEFL_ & RESET_                    &    " Hold on until reset,
MEMACK_ & MEMERR_                    ;    " memory acknowledge or error.
!WRTPND_ :=                               " Write pipeline transaction pending.

!PIPEFL_ & WRTPND_ & AS_             &    " Assert on pipe full, address strobe
MEMERR_ & RESET_                     #    " gone and no error or reset.

!WRTPND_ & !PIPEFL_                  &    " Hold output on while pipe is full
MEMERR_ & RESET_                     ;    " and no error or reset.

"************************ Description ************************
" This PAL keeps track of the write pipeline status and generates
" the synchronous terminate acknowledge (TERMAK_) to terminate
" write cycles when the pipeline is empty, successive write cycles
" where the pipeline is full and a write cycle is waiting, read miss
" retry cycles, and noncacheable read cycles.
"
" The PIPEFL_ signal asserts whenever the write pipeline is full.
" It holds on until either a memory error or acknowledge is received.
" This output is used to latch the write address and data into the
" write pipeline.  On successive write cycles, this signal pulses high
" for one clock to allow the new address and data to be latched.
"
" The WRTPND_ signal asserts whenever the write pipeline is full
" and the 68030 address strobe is gone.  It is used to detect the
" second of two successive write cycles so that the first write
" can complete before the pipeline is refilled.
"
"********************** Revision History **********************
" Rev A - Logic Innovations, Inc., FJC - 08/04/89.
" New Release.  First Version.
"
End P105;
```

APPENDIX D

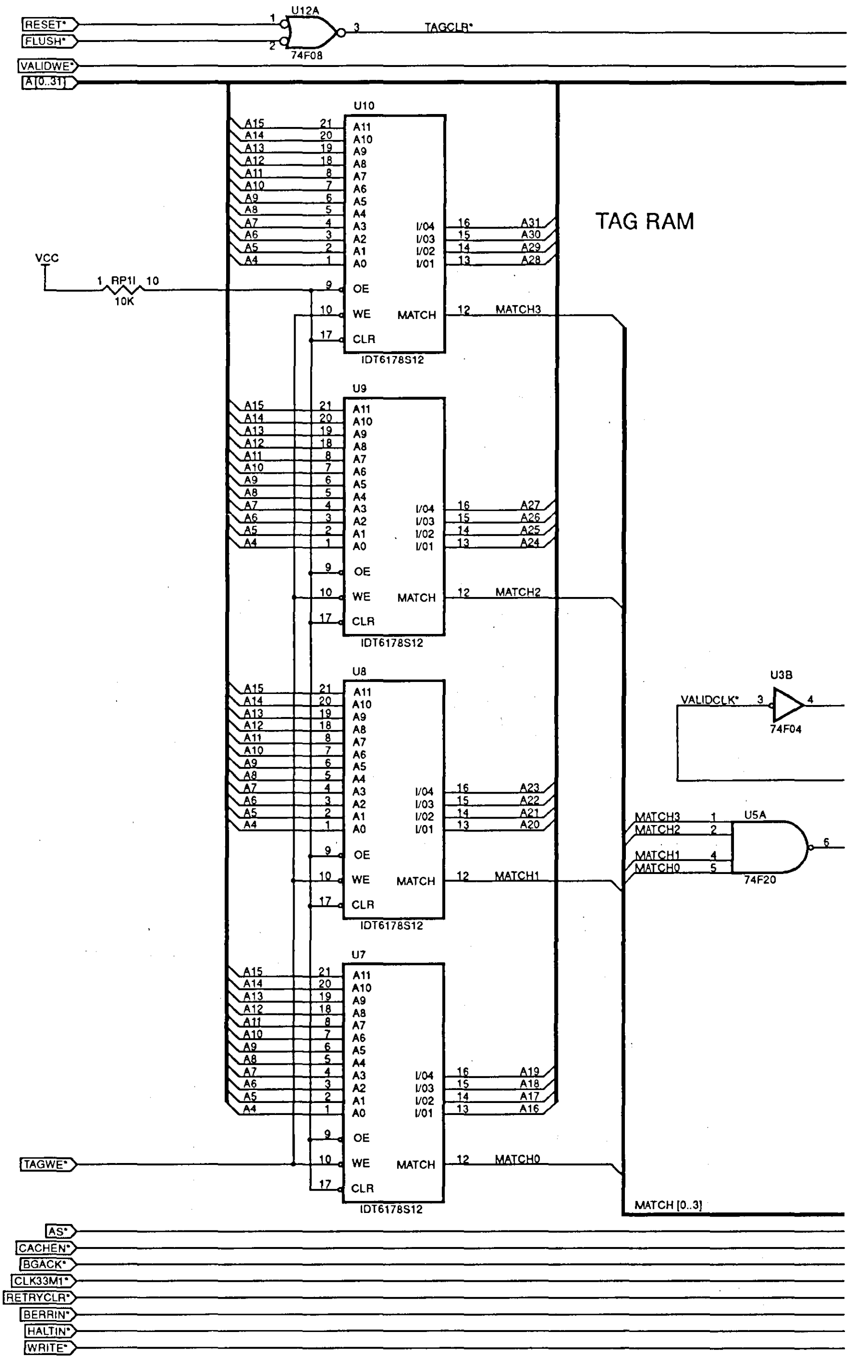
SCHEMATIC DIAGRAMS



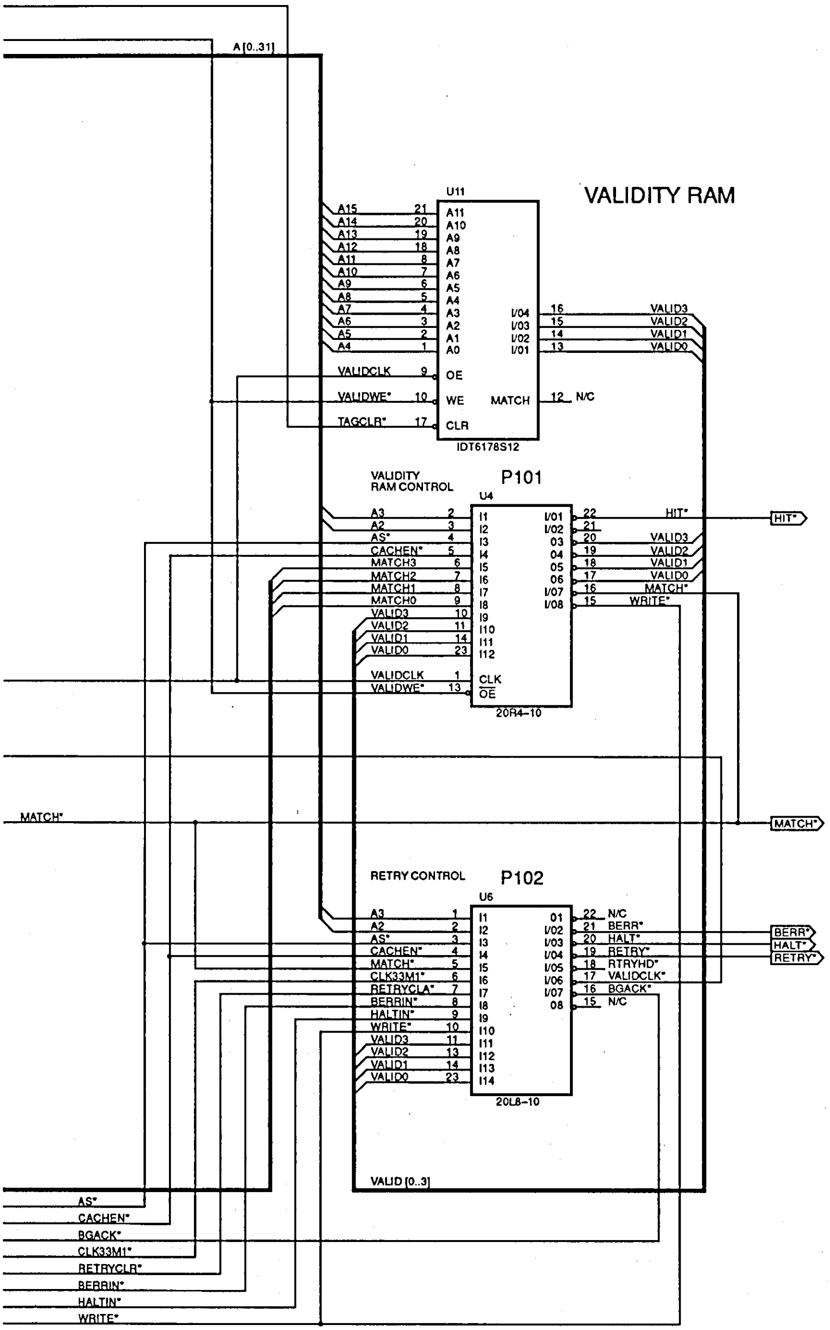
Central Processor: 33MHz 68030



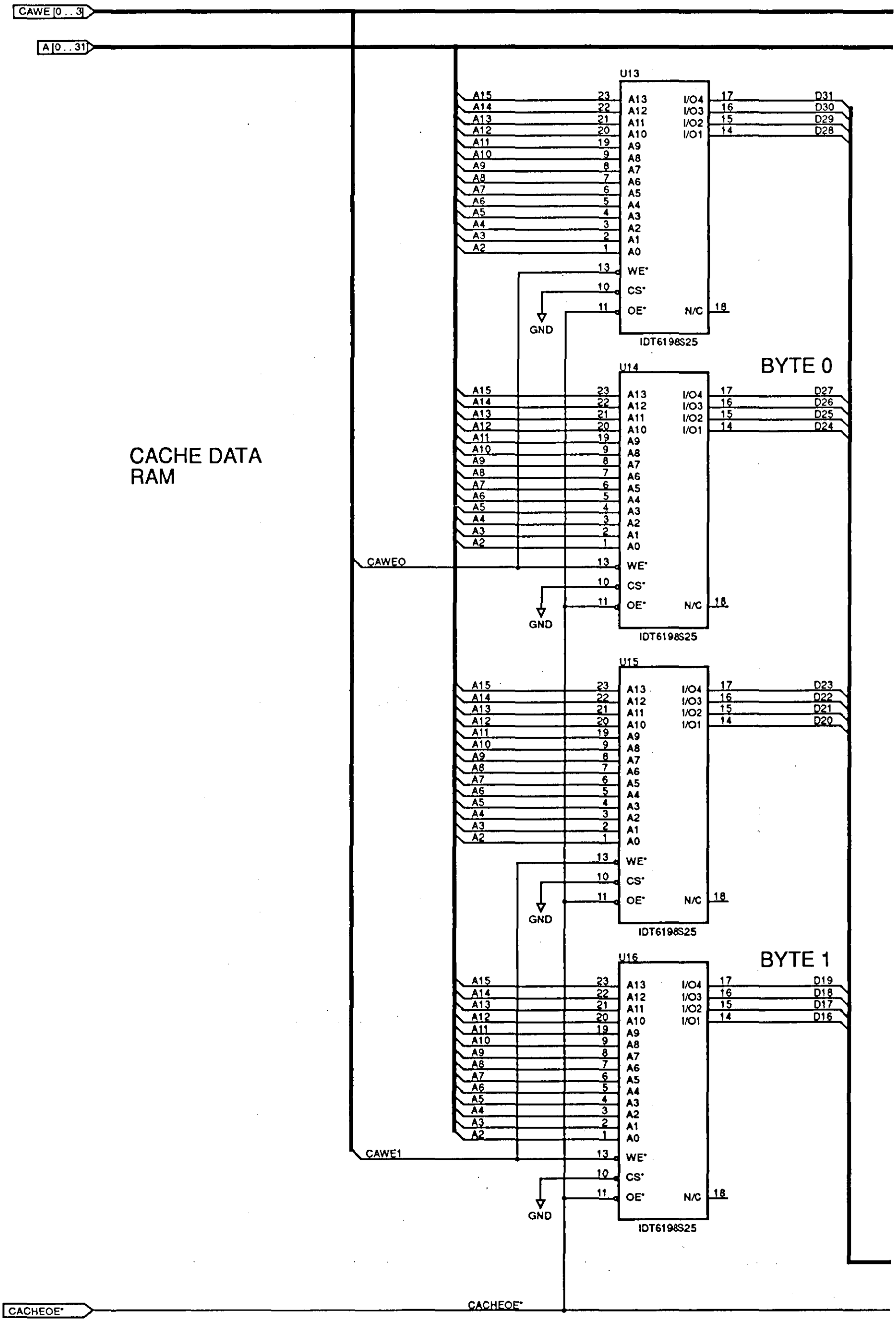
Central Processor: 33MHz 68030 (cont'd)



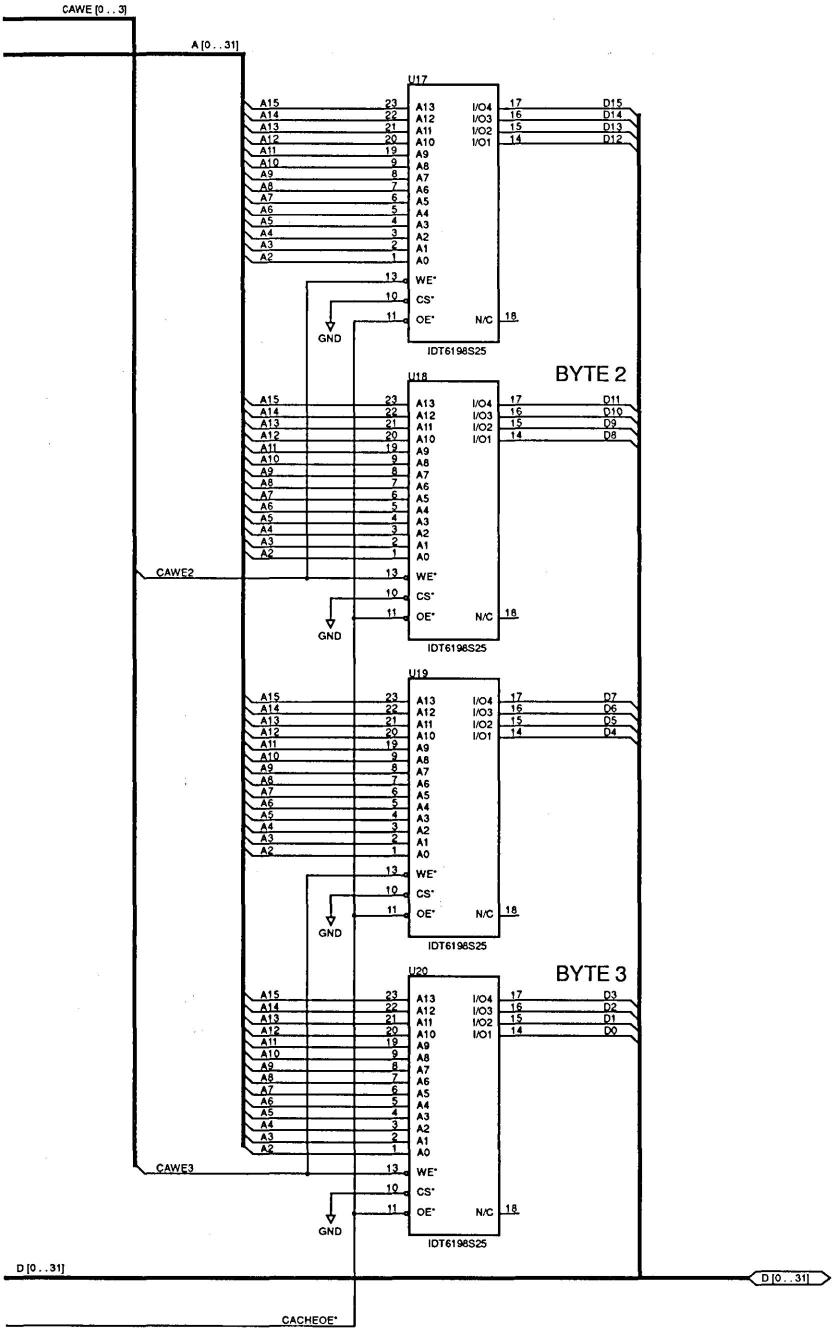
Cache Tag Validity RAMS, Update Logic



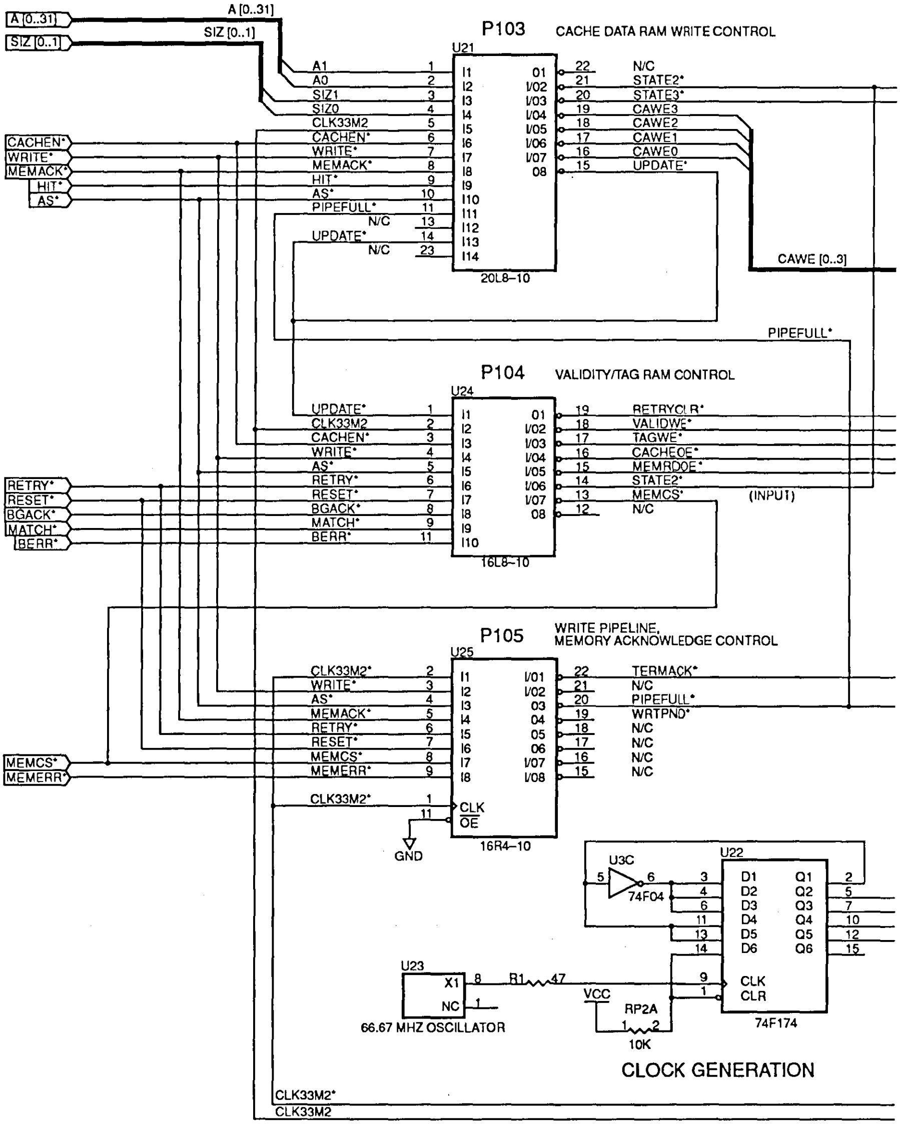
Cache Tag Validity RAMS, Update Logic (cont'd)



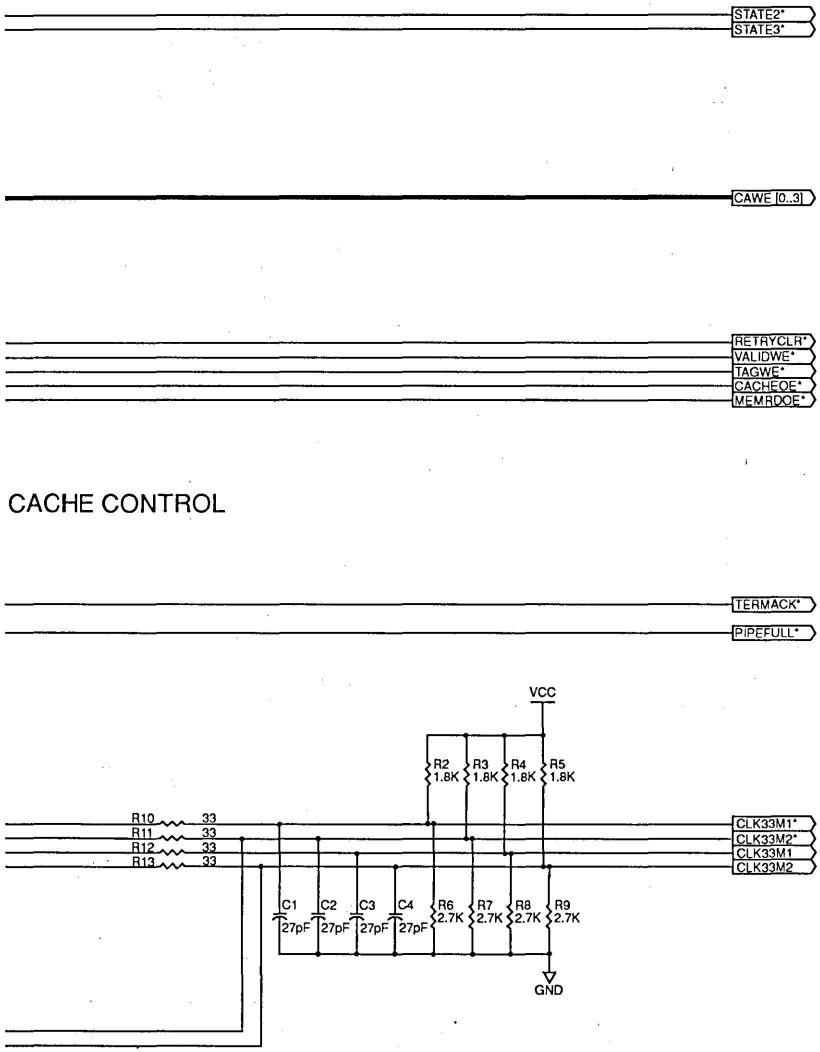
64KB Direct Map Data Cache



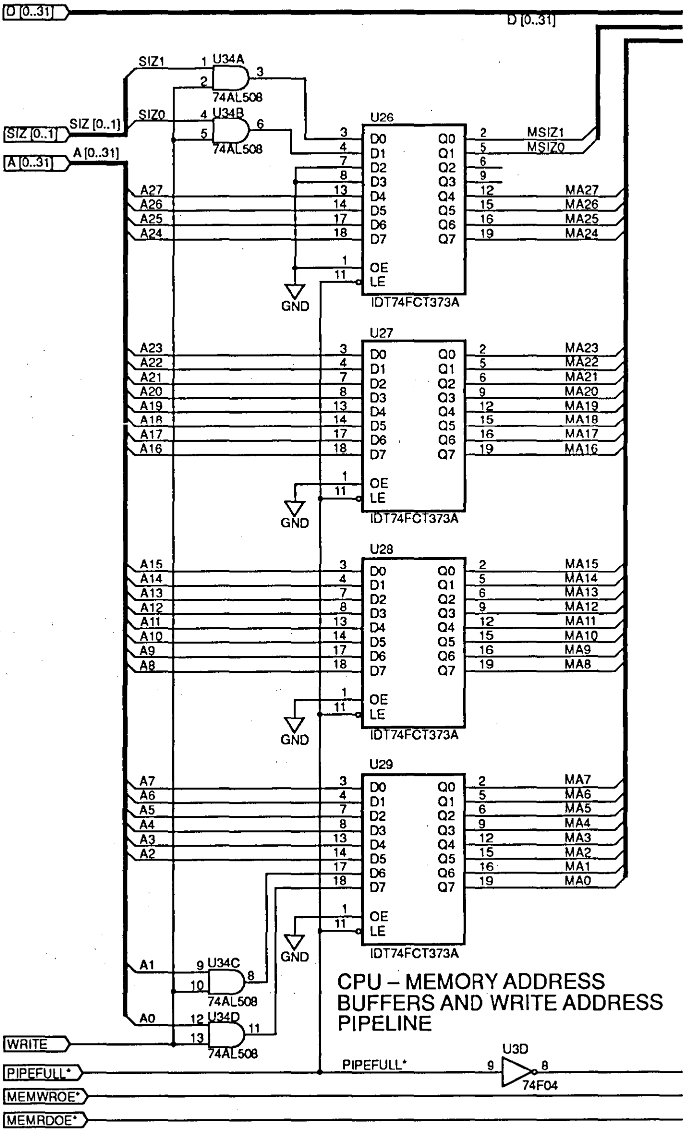
64KB Direct Map Data Cache (cont'd)



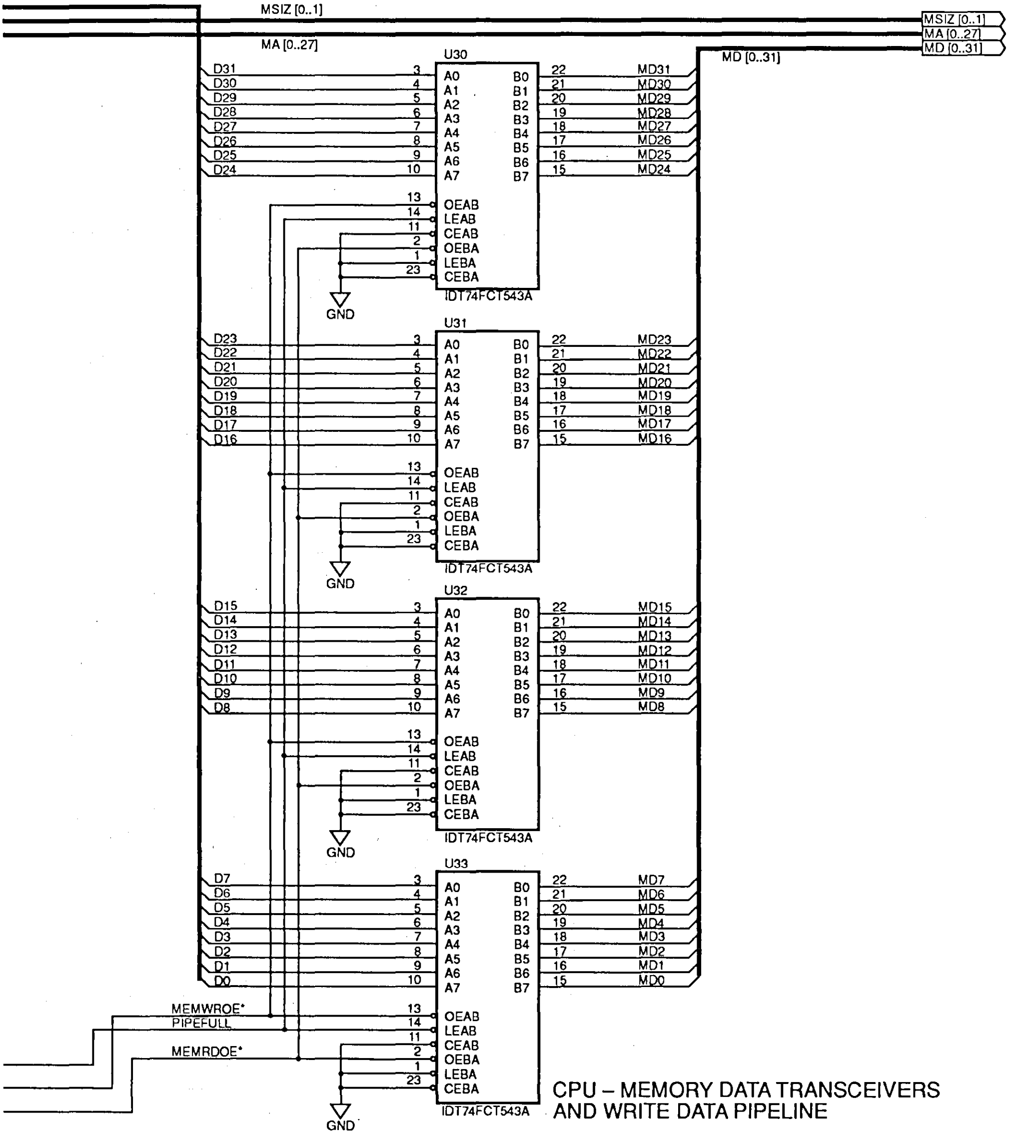
Cache Control Logic



Cache Control Logic (cont'd)



68030 Address Latches, Data Transceivers



CPU – MEMORY DATA TRANSCEIVERS AND WRITE DATA PIPELINE

68030 Address Latches, Data Transceivers (cont'd)

APPENDIX E

TIMING DIAGRAMS

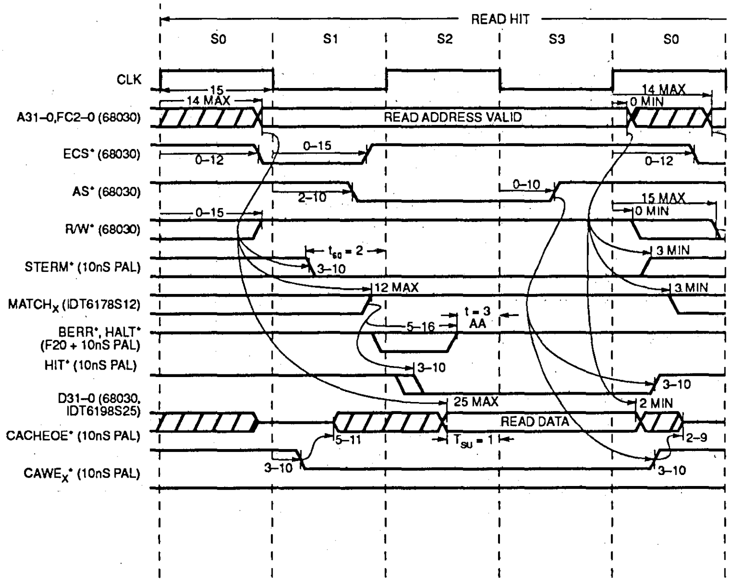


Figure 2. 33MHz MC68030 Cache Read, Write Hits

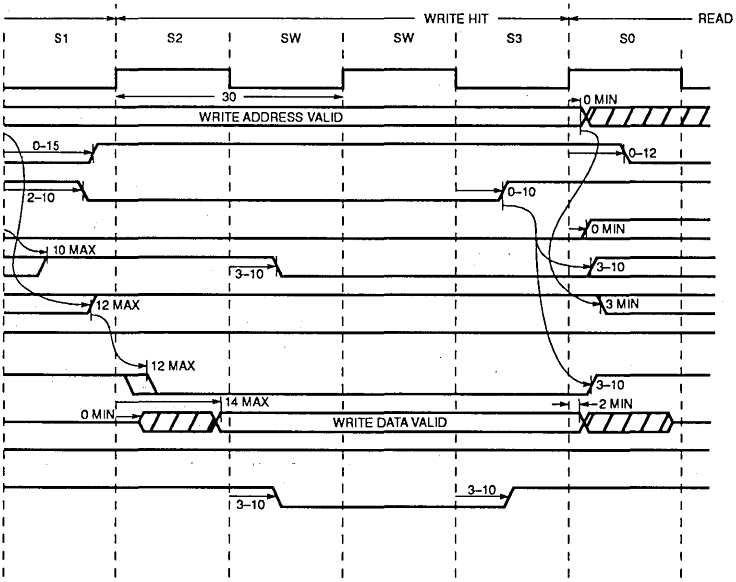


Figure 2. 33MHz MC68030 Cache Read, Write Hits (cont'd)

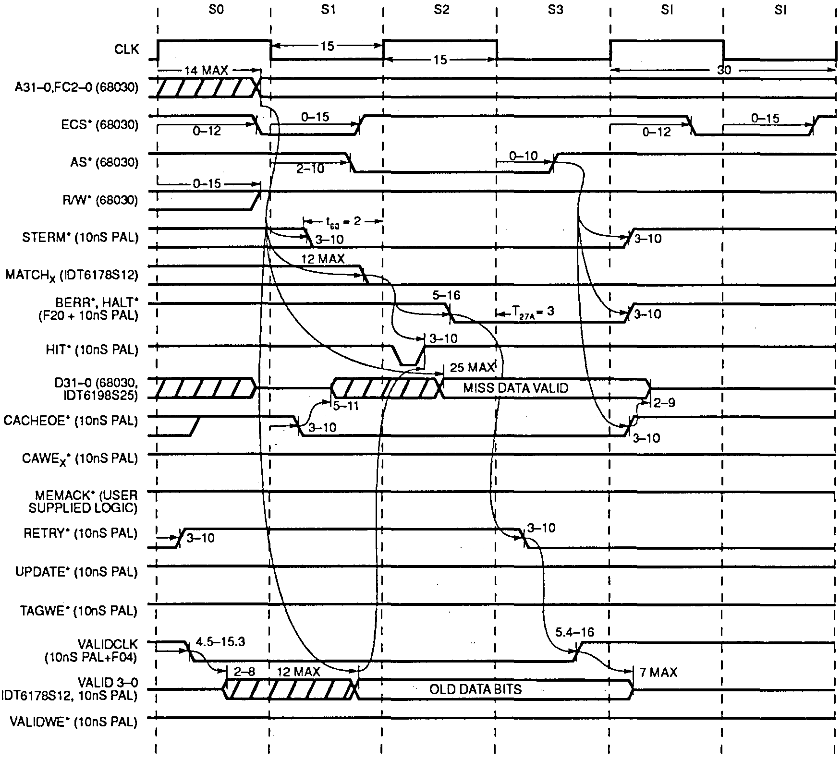


Figure 3. 33MHz MC68030 Cache Read Miss — Retry — Update Cycle

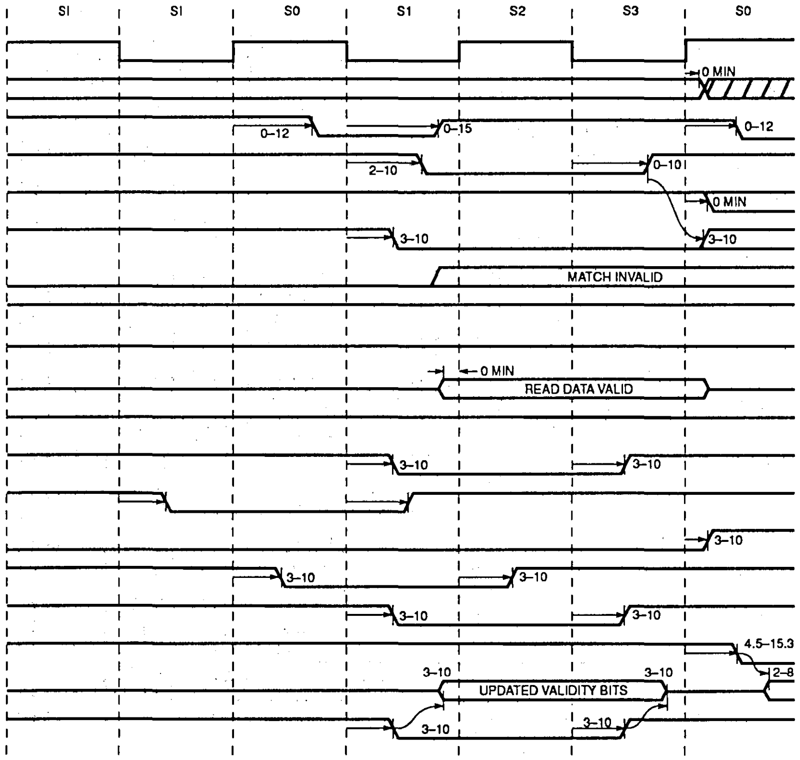


Figure 3. 33MHz MC68030 Cache Read Miss — Retry — Update Cycle (cont'd)

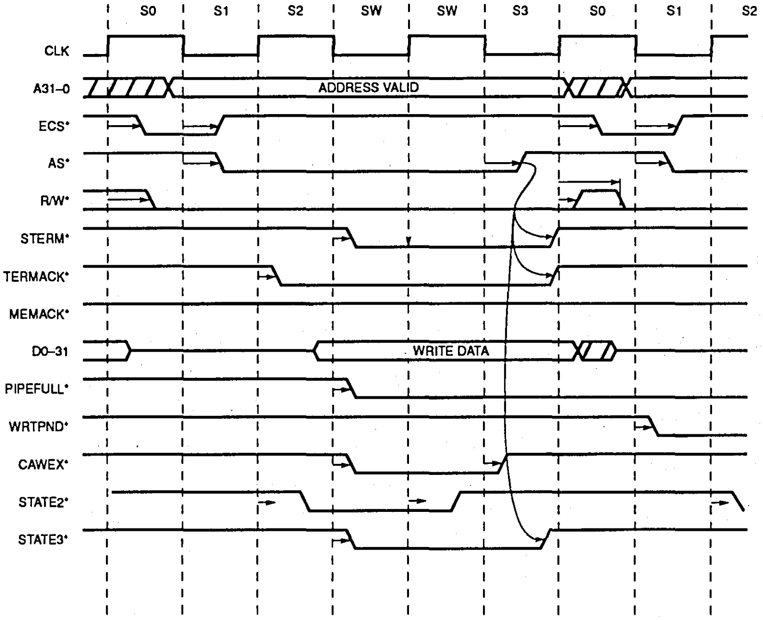


Figure 4. 33MHz MC68030 Back to Back Write Hit/Pipelined

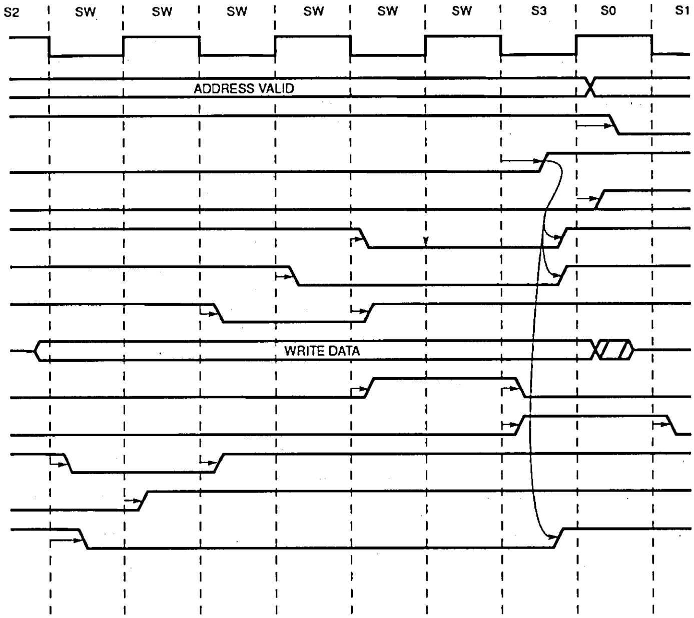


Figure 4. 33MHz MC68030 Back to Back Write Hit/Pipelined (cont'd)

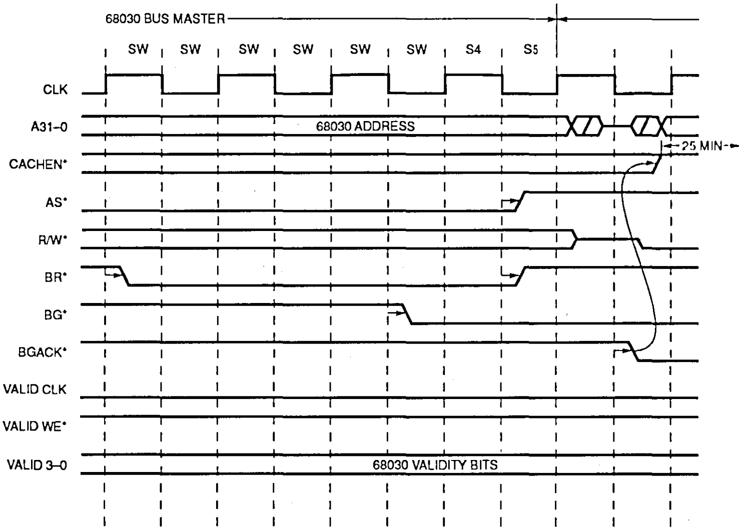


Figure 5. 33MHz MC68030 Cache Coherency Cycle

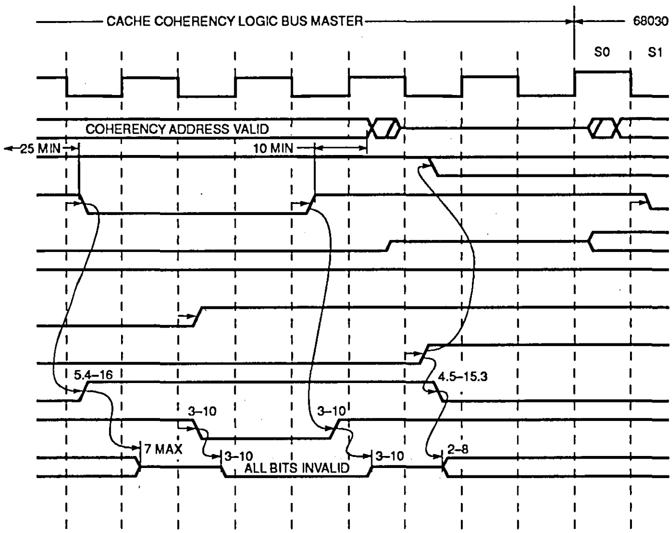


Figure 5. 33MHz MC68030 Cache Coherency Cycle (cont'd)

APPENDIX F

PARTS LIST

IDT 33MHz 68030 Cache Revised: August 28, 1989
Revision: A

Bill Of Materials August 28, 1989 12:42:24 Page 1 of 1

Item	Quantity	Reference	Part
1	4	C1,C2,C3,C4	27pF
2	3	JP1,JP2,JP3	JUMP2
3	1	R1	47
4	4	R2,R3,R4,R5	1.8K
5	4	R6,R7,R8,R9	2.7K
6	4	R10,R11,R12,R13	33
7	2	RP1,RP2	10K
8	1	U1	68030-33
9	3	U2,U6,U21	20L8-10
10	1	U3	74F04
11	1	U4	20R4-10
12	1	U5	74F20
13	5	U7,U8,U9,U10,U11	IDT6178S12
14	1	U12	74F08
15	8	U13,U14,U15,U16,U17,U18, U19,U20	IDT6198S25
16	1	U22	74F174
17	1	U23	66.67MHz OSCILLATOR
18	1	U24	16L8-10
19	1	U25	16R4-10
20	4	U26,U27,U28,U29	IDT74FCT373A
21	4	U30,U31,U32,U33	IDT74FCT543A
22	1	U34	74ALS08

APPENDIX G

USER INTERFACE

This appendix discusses the timing, loading, architectural, and other design considerations relevant to the cache design. In addition, signal definitions including those supplied by the user to interface to the MC68030 cache design are provided.

ADDRESS AND DATA LOADING

The 33MHz MC68030 cache design was analyzed for capacitive and DC loading assuming several additional loads (not shown) for the benefit of the user. Refer to Appendix A, Loading Analysis for detailed information. The additional loads and their functions are as follows:

ADDRESS BUS (A31-A0):

A31–A0: 74ALS245 - Transeiver for coherency and/or dual port address path.
A4: MC68882 - Floating Point Coprocessor.
A31–A16: PAL20L8 - Two pals for additional address decoding.

DATA BUS (D31-D0):

D31–D0: 74ALS245 - I/O, EPROM, system bus interface data path.
D31–D0: MC68882 - Floating Point Coprocessor.

The user is free to add more loads to either the address or data buses so long as DC loading characteristics are not violated and timing parameters are derated for added capacitive loading.

CACHE COHERENCY/DUAL PORT

The cache coherency interface to the 33MHz MC68030 cache is also designed to be a dual port memory interface. The dual port interface will allow the user to perform memory read and write operations in parallel with cache coherency cycles. Memory write cycles will utilize the write pipeline.

Figure 5.0 details the timing requirements for a cache coherency/dual port cycle. The user should drive a function code of 0 for coherency only cycles. For dual port cycles, a valid function code (1, 2, 5 or 6) should be driven.

The 33MHz MC68030 cache design requires that the user drive the coherency/dual port address onto the A31-A0 lines using a 74ALS245 transceiver (not shown in the schematics). The MC68030 data lines should be driven only for dual port operation. The remaining MC68030 signals should be driven in similar manner as the MC68030. Control signals such as AS*, DS*, WRITE*, etc. should be asserted and deasserted on clock edges according to the MC68030 AC electrical specifications.

IDT 33MHZ MC68030 CACHE SIGNAL DESCRIPTIONS

SIGNAL NAME	ACTIVE STATE	DRIVER	USER	DESCRIPTION
AS*	L	3S	Yes	MC68030 address strobe. Also driven by coherency/dual port interface logic.
AVEC*	L	TP	Yes	Autovector. Driven by user to terminate autovectored inter- rupt acknowledge cycle.
A[0..31]	H	3S	Yes	MC68030 address bus. Driven by user for coherency/dual port cycles.
BERR*	L	TP	No	MC68030 bus error input. Driven by P102 (U6) retry cycles. It is also asserted by P102 when the user supplied logic asserts BERRIN*.
BERRIN*	L	TP	Yes	Bus error in. Driven by user to force P102 to generate BERR* to MC68030. The user can assert BERRIN* (alone) to bus error a processor bus cycle or (with HALTIN*) to generate a non- cacheable retry.
BG*	L	TP	No	Bus grant. Driven by MC68030.
BGACK*	L	TP	Yes	Bus grant acknowledge. Driven by user on coherency/dual port cycles.
BR*	L	TP	Yes	Bus request. Driven by user on coherency/dual port cycles.
CACHEN*	L	TP	No	Cache enable. This signal is driven by P100 (U2) to indicate that the cycle in progress is cacheable.
CACHEOE*	L	TP	No	Data cache output enable. This signal is driven by P104 (U24) to the IDT6198 data RAMs to output cache read data onto the MC68030 data bus.

Key: TP = totem pole
3S = tri-state
OD = open drain

SIGNAL NAME	ACTIVE STATE	DRIVER	USER	DESCRIPTION
CAWE[0..3]	L	TP	No	Data cache write enable. These signals are driven by P103 (U21) to cause data to be written into the cache data RAMs on either a read miss- update cycle or a write hit.
CIIN*	L	TP	No	Cache inhibit in. This signal is asserted to force the MC68030 to not internally cache the current cycle. It is generated to force I/O space, system bus space or other non- memory address space to be noncacheable. CIIN* is driven by P100 (U2).
CIOUT*	L	TP	No	Cache inhibit out. The MC68030 asserts this signal to indicate that the current bus cycle should not be cached externally.
CLK33M1	H	TP	No	33MHz clock # 1. This is the 33MHz, 50% duty cycle clock used to drive the MC68030 and/or on board logic.
CLK33M2	H	TP	No	33MHz clock # 2. This is the 33MHz, 50% duty cycle clock used to drive on board logic.
CLK33M1*	L	TP	No	33MHz clock # 1. This is the 33MHz, 50% duty cycle active low clock used to drive on board logic.
CLK33M2*	L	TP	No	33MHz clock # 2. This is the 33MHz, 50% duty cycle active low clock used to drive on board logic.
DBEN*	L	3S	No	Data bus enable. Provided by MC68030 for user supplied logic.
DS*	L	3S	No	MC68030 data strobe.
DSACK1,0*	L	TP	Yes	MC68030 data and size acknowledge. Driven by user for all noncacheable, non-memory cycles (I/O, system bus, vectored interrupt acknowledge, etc.).
D[0..31]	H	3S	Yes	MC68030 data bits. Driven by user for I/O accesses (through a transceiver), MC68882 accesses or other custom interface.
ECS*	L	TP	No	MC68030 early cycle start.
FC[0..2]	H	3S	No	MC68030 function code.
FLUSH*	L	TP	Yes	Cache flush. This signal is generated by the user to invalidate the entire cache. It is normally generated by an I/O access. The pulse width on this signal must be at least 26nS and it must be generated while the cache is not being accessed. Therefore, the MC68030 should be in the process of an I/O access or it should be halted while the flush signal is active.
HALT*	L	TP	No	MC68030 halt input. P102 (U6) generates this signal on retry cycles. It is also asserted by P102 when the user supplied logic asserts HALTIN*.
HALTIN*	L	TP	Yes	Halt in. Generated by user supplied logic to assert the HALT* signal to the MC68030. The user can assert HALTIN* (alone) to cause a processor halt state or (with BERRIN*) to generate a noncacheable retry.
HIT*	L	TP	No	Cache hit. May be used by user supplied logic to as an early indication of a cache miss.
IPL[0..2]	L	TP	Yes	MC68030 interrupt priority level input.
MATCH*	L	TP	No	Cache TAG RAM match indication.
MA[0..27]	H	3S	No	Latched memory address bits.

SIGNAL NAME	ACTIVE STATE	DRIVER	USER	DESCRIPTION
MD[0..31]	H	3S	Yes	Registered memory data bits. The user must present read data on these lines no later than 1.5 clocks after MEMACK* is asserted. See Figure 3.0. On write cycles, the user must generate MEMWROE* to output write memory data onto MD0-31.
MEMACK*	L	TP	Yes	Memory acknowledge. This user supplied signal should be asserted for one clock based on the CLK33M1 falling edge (or CLK33M2* rising edge). It should be asserted no earlier than 1.5 clocks before memory read data is valid. See Figure 3.0.
MEMCS*	L	TP	No	Memory chip select. Generated by P100 (U2).
MEMERR*	L	TP	Yes	Memory error. This signal should be generated by user supplied logic to indicate a memory parity error, an access to nonexistent memory, or other error. MEMERR* should be asserted for one clock based on the CLK33M1 falling edge (or CLK33M2* rising edge). It is used to clear a write cycle pending in the pipeline. The user should simultaneously assert BERRIN* and MEMERR* for read cycles which result in an error condition.
MEMRDOE*	L	TP	No	Memory read data output enable. P104 (U24) asserts this signal to place memory read data onto the MC68030/cache data bus.
MEMWROE*	L	TP	Yes	Memory write data output enable. User supplied logic must assert this signal according to the memory timing requirements.
MSIZ[0..1]	H	3S	No	Latched memory size bits.
PIPEFULL*	L	TP	No	Write pipeline full. Generated by P105 (U25) to latch the memory write address and data. It can also be used as a memory write request signal.
RESET*	L	OD	Yes	Reset. Reset must be generated by a user supplied open collector (pulled up) driver.
RETRY*	L	TP	No	Retry. This signal is generated by P102 (U6) to indicate that a retry cycle is in progress. It can be used by user supplied logic to indicate a memory read miss request.
RETRYCLR*	L	TP	No	Retry clear is generated by P104 (U24). It forces RETRY* to deassert based on a bus error, reset, or alternate bus master access.
RMC*	L	3S	No	MC68030 read modify write cycle.
SIZ[0..1]	H	3S	No	MC68030 size bits.
STATE2*	L	TP	No	MC68030 state 2. This signal ascerts in state 2 and deasserts after state 3. Generated by P103 (U21).
STATE3*	L	TP	No	MC68030 state 3. This signal asserts in state 3 and holds on until the bus cycle is complete. Generated by P103 (U21).
TAGWE*	L	TP	No	Tag RAM write enable. Generated by P104 (U24).
TERMACK*	L	TP	No	Terminate acknowledge. This signal is generated by P105 (U25). The assertion of TERMACK* causes P100 (U2) to assert STERM*, which acknowledges a 32 bit bus cycle to the MC68030. TERMACK* asserts on pipelined write cycles, retry cycles, and noncacheable read cycles.

SIGNAL NAME	ACTIVE STATE	DRIVER	USER	DESCRIPTION
VALIDWE*	L	TP	No	Validity RAM write enable. VALIDWE* is generated by P104 (U24). It serves to output enable the new validity bits in P101 (U4) and strobe the new validity data into the validity RAM, IDT6178S12 (U11).
WRITE*	L	3S	No	MC68030 write signal (low).
WRITE	H	TP	No	MC68030 write signal (high).

APPENDIX H

50MHz MC68030 TIMING ANALYSIS

50MHZ MC68030 — CACHE TIMING

(2 CLOCK CACHE READ, 3 CLOCK CACHE WRITE)
~ - indicates a derated parameter.
CP - indicates common path analysis used.

IDT6198S15 CACHE DATA READ PARAMETERS:

1. 68030 Address to IDT6198 Data Valid:	ns	
1.5 clocks @ 20ns:	30	
68030, t6, clock to address:	(14)	max
68030, t27, read data setup:	(1)	min
Data bus derating:	(2)	max
	13ns ******	

t_{AA} Required = 15ns

2. PAL CACHEOE* to IDT6198 Data Valid:	ns	
1 clock @ 20ns:	30	
7ns PAL, clock to CACHEOE*:	(7.5)	max
68030, t27, read data setup:	(1)	min
Data bus derating:	(2)	max
Clock skew:	(2)	max
	17.5ns	

t_{OE} Required = 8ns

3. CACHE CS* to IDT6198 Data Valid:
Since the cache data ram chip select is grounded, this is not a limiting parameter.

t_{ACS} Required = 15ns

4. 68030 AS* Negated to IDT6198 Data Invalid:	ns	
7ns PAL, clock to CACHEOE*:	3	min
IDT6198 CACHEOE* to data invalid:	0	min
	3ns	

MC68030 T29 Required = 0ns

IDT6198S15 CACHE DATA WRITE PARAMETERS:

5. 68030 Synchronous Data Hold:	ns	
68030, T12, clock to AS* negated:	0	min
7ns PAL, clock to CACHEOE*:	3	min
IDT6198 CACHEOE* to data invalid:	0	min
	3ns	

MC68030 T30 Required = 6ns
Note:Data hold time is satisfied by parameter #4 above. See MC68030 User's Manual note #12 on page 13-6.

6. 68030 Address Valid to IDT6198 Write Begin:	ns	
1.5 clock @ 20ns:	30	
7ns PAL, clock to CAWEx* low:	3	min
68030, t6, clock to address:	(14)	max
Clock skew:	(2)	max
	17ns	

t_{AS} Required = 0ns

7. 68030 Address Valid to IDT6198 Write End:	ns	
2.5 clocks @ 20ns:	50	
7ns PAL, clock to CAWEx* high:	3	min
68030, t6, clock to address:	(14)	max
Clock skew:	(2)	max
	37ns	

t_{AW} Required = 14ns

7. IDT6198 Write Pulse Width:	ns	
1 clock @ 20ns:	20	
7ns PAL, clock to CAWEx* high:	3	min
7ns PAL, clock to CAWEx* low:	(7.5)	max
	15.5ns	

t_{WP} Required = 14ns

IDT6198S15 CACHE DATA WRITE PARAMETERS:

8. 68030 Data Valid to IDT6198 Write End:	ns	
1.5 clock @ 20ns:	30	
7ns PAL, clock to CAWEx* high:	3	min
68030, t23, clock to data:	(14)	max
Clock skew:	(2)	max
	17ns	

t_{DW} Required = 8ns

9. 68030 Data Hold to IDT6198 Write End:	ns	
0.5 clock @ 20ns:	10	
68030, t53, clock to data invalid:	2	min
7ns PAL, clock to CAWEx* high:	(7.5)	max
Clock skew:	(2)	max
	2.5ns	

t_{DH} Required = 0ns

IDT6178S12 CACHE TAG HIT/MISS PARAMETERS:

10. BERR*, HALT* Set up to Clock Low:	ns	
1.5 clocks @ 20ns:	30	
68030, t6, clock to address:	(14)	max
7ns PAL, MATCHx to BERR*, HALT*:	(7.5)	max
74F20, MATCHx to MATCH*:	(6)	max
68030, t27A, BERR*, HALT* setup:	(3)	min
	−0.5ns *******	

t_{ADM} Required = 12ns (From IDT6178 address)
t_{DAM} Required = 11ns (From IDT6178 data)

11. BERR*, HALT* Set up to Clock Low: (from output enable, retry followed by read)	ns	
1.5 clocks @ 20ns:	30	
7ns PAL, clock to VALIDWE:	(7.5)	max
74F04, VALIDWE:	(5.3)	max
7ns PAL, MATCHx to BERR*, HALT*:	(7.5)	max
68030, t27A, BERR*, HALT* setup:	(3)	min
Clock skew:	(2)	max
	4.7ns ******	

t_{OE} Required = 8ns

IDT6178S12 CACHE TAG WRITE PARAMETERS:

12. Address valid to end of Write:
Not calculated but certainly not a problem.

t_{AW} Required = 10ns

13. IDT6178 Write Pulse Width:	ns	
1 clocks @ 20ns:	20	
7ns PAL, clock to VALIDWE* high:	3	min
7ns PAL, clock to VALIDWE* low:	(7.5)	max
	15.5ns	

t_{WP} Required = 10ns

14. IDT6178 Data Valid to Write End:	ns	
1 clock @ 20ns:	20	
7ns PAL, clock to VALIDWE* high:	3	min
7ns PAL, clock to VALIDWE* low:	(7.5)	max
7ns PAL, VALIDWE* to VALID0-3:	(7.5)	max
	8ns	

t_{DW} Required = 8ns

15. IDT6178 Data Hold after write:	ns	
7ns PAL, VALIDWE* to VALID0-3:	3	min
	3ns	

t_{DH} Required = 0ns

16. Address Setup to AS* low: (Coherency cycle)	ns	
Address setup to AS* low:	25	min
7ns PAL, AS* to VALIDCLK*:	3	min
74F04, VALIDCLK* to VALIDCLK:	2.4	min
74F20, MATCHx to MATCH*:	(6)	max
7ns PAL, MATCH* setup to VALIDCLK:	(7.5)	max
	16.9ns	

t_{ADM} Required = 12ns (From IDT6178 address)
t_{DAM} Required = 11ns (From IDT6178 data)

IDT6178S12 CACHE TAG WRITE PARAMETERS:

17. IDT6178 Address Hold after Write: (Retry cycle)	ns	
0.5 clocks @ 20ns:	10	
68030 t8, Address Hold:	0	min
7ns PAL, clock to VALIDWE* high:	(7.5)	max
	2.5ns	

t_{WR} Required = 0ns

18. IDT6178 Address Hold after Write: (Coherency cycle)	ns	
Address hold to AS* high:	10	min
7ns PAL, AS* to VALIDWE* high:	(7.5)	max
	2.5ns	

t_{WR} Required = 0ns

50MHZ MC68030 — CACHE TIMING

(3 CLOCK CACHE READ, 3 CLOCK CACHE WRITE)
(NO RETRY ON CACHE MISS)
~ - indicates a derated parameter.
CP - indicates common path analysis used.

IDT6198S20 CACHE DATA READ PARAMETERS:

1. 68030 Address to IDT6198 Data Valid:	ns	
2.5 clocks @ 20ns:	50	
68030, t6, clock to address:	(14)	max
68030, t27, read data setup:	(1)	min
Data bus derating:	(2)	max
	33ns	

t_{AA} Required = 20ns

2. PAL CACHEOE* to IDT6198 Data Valid:	ns	
2 clocks @ 20ns:	40	
68030, t9, read data setup:	(10)	max
7ns PAL, clock to CACHEOE*:	(7.5)	max
68030, t27, read data setup:	(1)	min
Data bus derating:	(2)	max
	19.5ns	

t_{OE} Required = 8ns

3. CACHE CS* to IDT6198 Data Valid:
Since the cache data ram chip select is grounded, this is not a limiting parameter.

t_{ACS} Required = 20ns

4. 68030 AS* Negated to IDT6198 Data Invalid:	ns	
7ns PAL, clock to CACHEOE*:	3	min
IDT6198 CACHEOE* to data invalid:	0	min
	3ns	

MC68030 T29 Required = 0ns

IDT6198S20 CACHE DATA WRITE PARAMETERS:

5. 68030 Synchronous Data Hold:	ns	
68030, T12, clock to AS* negated:	0	min
7ns PAL, clock to CACHEOE*:	3	min
IDT6198 CACHEOE* to data invalid:	0	min
	3ns	

MC68030 T30 Required = 6ns
Note: Data hold time is satisfied by parameter #4 above. See MC68030 User's Manual note #12 on page 13-6.

6. 68030 Address Valid to IDT6198 Write Begin:	ns	
1.5 clock @ 20ns:	30	
7ns PAL, clock to CAWEx* low:	3	min
68030, t6, clock to address:	(14)	max
Clock skew:	(2)	max
	17ns	

t_{AS} Required = 0ns

7. 68030 Address Valid to IDT6198 Write End:	ns	
2.5 clocks @ 20ns:	50	
7ns PAL, clock to CAWEx* high:	3	min
68030, t6, clock to address:	(14)	max
Clock skew:	(2)	max
	37ns	

t_{AW} Required = 14ns

7. IDT6198 Write Pulse Width:	ns	
1 clock @ 20ns:	20	
7ns PAL, clock to CAWEx* high:	3	min
7ns PAL, clock to CAWEx* low:	(7.5)	max
	15.5ns	

t_{WP} Required = 14ns

IDT6198S20 CACHE DATA WRITE PARAMETERS:

8. 68030 Data Valid to IDT6198 Write End:	ns	
1.5 clock @ 20ns:	30	
7ns PAL, clock to CAWEx* high:	3	min
68030, t23, clock to data:	(14)	max
Clock skew:	(2)	max
	17ns	

t_{DW} Required = 8ns

9. 68030 Data Hold to IDT6198 Write End:	ns	
0.5 clock @ 20ns:	10	
68030, t53, clock to data invalid:	2	min
7ns PAL, clock to CAWEx* high:	(7.5)	max
Clock skew:	(2)	max
	2.5ns	

t_{DH} Required = 0ns

IDT6178S12 CACHE TAG HIT/MISS PARAMETERS:

10. STERM* Set up to Clock High:	ns	
2.0 clocks @ 20ns:	40	
68030, t6, clock to address:	(14)	max
7ns PAL, MATCHx to STERM*:	(7.5)	max
68030, t60, STERM* setup:	(2)	min
	16.5ns	

t_{ADM} Required = 12ns (From IDT6178 address)
t_{DAM} Required = 11ns (From IDT6178 data)

11. STERM* Set up to Clock High: (from output enable, retry followed by read)	ns	
2.0 clocks @ 20ns:	40	
7ns PAL, clock to VALIDWE:	(7.5)	max
74F04, VALIDWE:	(5.3)	max
10ns PAL, MATCHx to BERR*, HALT*:	(7.5)	max
68030, t60, STERM* setup:	(3)	min
Clock skew:	(2)	max
	14.7ns	

t_{OE} Required = 8ns

IDT6178S12 CACHE TAG WRITE PARAMETERS:

12. Address valid to end of Write:
Not calculated but certainly not a problem.

t_{AW} Required = 10ns

13. IDT6178 Write Pulse Width:	ns	
1 clocks @ 20ns:	20	
7ns PAL, clock to VALIDWE* high:	3	min
7ns PAL, clock to VALIDWE* low:	(7.5)	max
	15.5ns	

t_{WP} Required = 10ns

14. IDT6178 Data Valid to Write End:	ns	
1 clocks @ 20ns:	20	
7ns PAL, clock to VALIDWE* high:	3	min
7ns PAL, clock to VALIDWE* low:	(7.5)	max
7ns PAL, VALIDWE* to VALID0-3:	(7.5)	max
	8ns	

t_{DW} Required = 8ns

15. IDT6178 Data Hold after write:	ns	
7ns PAL, VALIDWE* to VALID0-3:	3	min
	3ns	

t_{DH} Required = 0ns

16. Address Setup to AS* low: (Coherency cycle)	ns	
Address setup to AS* low:	25	min
7ns PAL, AS* to VALIDCLK*:	3	min
74F04, VALIDCLK* to VALIDCLK:	2.4	min
74F20, MATCHx to MATCH*:	(6)	max
7ns PAL, MATCH* setup to VALIDCLK:	(7.5)	max
	16.9ns	

t_{ADM} Required = 12ns (From IDT6178 address)
t_{DAM} Required = 11ns (From IDT6178 data)

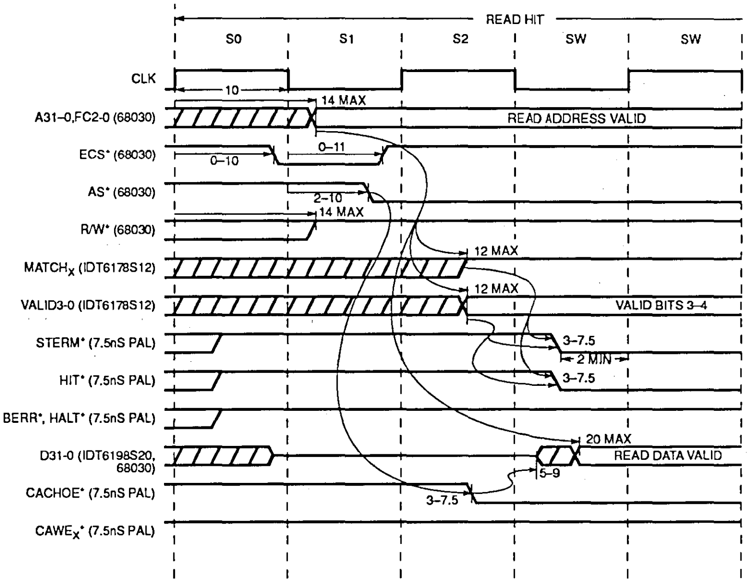
IDT6178S12 CACHE TAG WRITE PARAMETERS:

17. IDT6178 Address Hold after Write: (Retry cycle)	ns	
0.5 clocks @ 20ns:	10	
68030 t8, Address Hold:	0	min
7ns PAL, clock to VALIDWE* high:	(7.5)	max
	2.5ns	

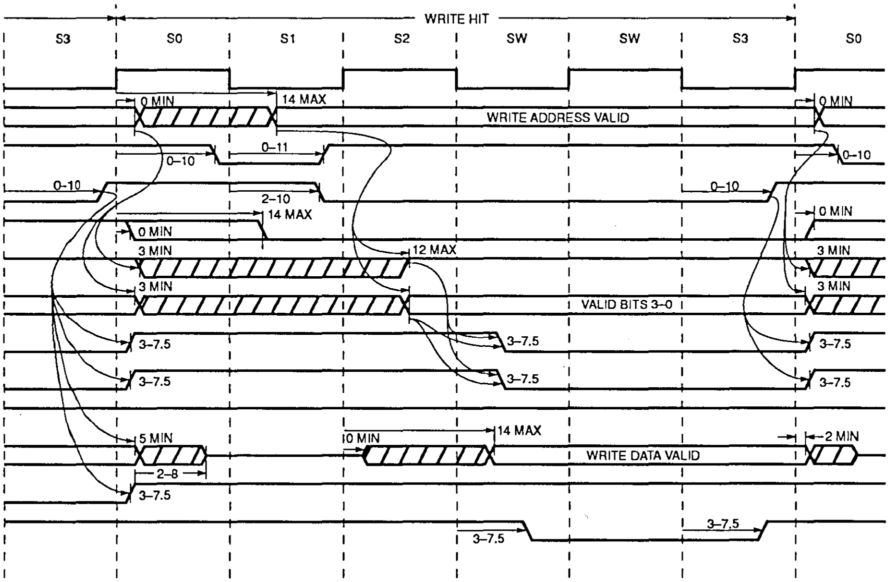
t_{WR} Required = 0ns

18. IDT6178 Address Hold after Write: (Coherency cycle)	ns	
Address hold to AS* high:	10	min
7ns PAL, AS* to VALIDWE* high:	(7.5)	max
	2.5ns	

t_{WR} Required = 0ns



50 MHz MC68030 Cache Read, Write Hits (3 clock)



50 MHz MC68030 Cache Read, Write Hits (3 clock) (cont'd

Integrated Device Technology, Inc.

33MHz 68020 CACHE IN ONLY 19 CHIPS

APPLICATION NOTE
AN-79

by Jim Handy

The schematic in Figures 1 and 2 shows a simple cache to support 33MHz zero-wait operation in the Motorola 68020. The design is a simple 32K byte direct-mapped write-through cache using a line size of one long-word. Software controls are provided for cache control during context switches, as is done on the internal caches in the 68030.

A few tricks are used to allow the cache to readily operate at this high frequency while using "off the shelf" parts. All parts used in this design have been readily available through distribution for years.

The first trick is that the cache resides in virtual space rather than physical space. This is done by driving the cache's address inputs with the logical address bus between the CPU and the MMU rather than the more typical move of using the MMU's address outputs. This approach reduces the delays in the address path to the cache memory, thus considerably loosening the constraints of cache memory access time. In addition, the CPU and cache memory can operate independently of the MMU, thus removing the extra cycle the MMU uses to translate addresses. The minimum cycle of this cache is three clock periods, whereas the minimum cycle of an MMU-mapped memory access is four clock periods.

The second trick is to use a bus retry sequence rather than the DS Acknowledge signals to signify a cache miss. With the more typical acknowlege-driven system, a miss cycle is handled as a single slow memory access. This would require the cache controller to respond with a "hit" or "miss" signal within the first 30ns of the memory cycle, during the CPU's S2 phase, to let the CPU operate out of cache with no wait states. (See IDT Technical Note 11 "Cache-Tag RAM Timing for the 68020 Using the IDT7174".) In the bus retry system shown here, two memory cycles (zero-wait read from cache, followed by retry) are executed on a cache miss, the latter being the cache update. A cache miss does not need to request a bus retry until the CPU's S4 cycle. The cost of this method is that eight additional clock half-cycles are incurred for every cache miss (a total additional delay of 120ns), however, the benefits are that considerably less costly and more widely available parts can be used for the cache-tag memory, and significant board space can be saved by the low component count of this slow of a cache.

The cache will be described in its three main sections: cache-tag RAM, cache data RAM, and cache control logic.

The cache-tag is built up of three IDT7174 8Kx8 cache-tag RAMs, U1, U2 and U3. These devices are fast (25ns) CMOS static RAMs which contain an eight-bit comparator to compare the RAM core's data outputs with the data input pins. The MATCH outputs are open-drain, and have been wire-ORed to allow the three devices to act as a single 8Kx24 device. A RESET input is used to invalidate all entries by clearing all RAM bits in the entire array to 0 within 55ns. Data inputs from the CPU to these devices consist of the cache index address, A2-A14, the upper address bits, A15-A31, the Size bits SIZE0-SIZE1, the function codes, FC0-FC2, and two valid bits. The cache index address, A2-A14, is simultaneously sent to the cache data RAM, and is used to indicate which cache address is being accessed. The upper address bits, A15-A31, determine whether the indexed address is replicated in the cache data RAM. The size bits SIZE0-SIZE1 allow the cache to store and subsequently retrieve misaligned data transfers, as long as a write or cache update cycle and the following read cycle are similarly misaligned. The function codes serve to identify whether the cache location is used in user/supervisor modes, and whether data consists of program or data entries. The 68020 allows each of these options to have its own 4 Gigabyte space. The valid bits are compared against the two remaining bits in the cache-tag RAMs. If the cache-tag has not had new data written to a location after a reset, the corresponding valid bits will contain zeros, and will not match the hard-wired high level present at the input pins, thus unilaterally preventing a cache hit from occurring at that location. Four other signals, $\overline{\text{CPUSPACE}}$, $\overline{\text{IOEN}}$, CACHE.E and $\overline{\text{AS}}$ disallow the cache-tag from issuing a hit when coprocessors or I/O devices are being accessed, when the cache is disabled, or upon an invalid address. $\overline{\text{CPUSPACE}}$ is derived from the function codes (FC0-2 all highs) while $\overline{\text{IOEN}}$ is a decoded address range where the I/O devices are mapped. These signals are combined with the cache-tag's output in U13A, U18D and U16B to produce the $\overline{\text{CHIT}}$ signal.

The cache data RAM is simply built up of four IDT7164 8Kx8 35ns CMOS static RAMs, U4 - U7. Its address inputs are the same cache index inputs which are fed into the cache-tag RAMs, its data I/O is the 68020's 32-bit data bus and the output enable is driven by the $\overline{\text{CHIT}}$ output from the tag array. The IDT7164's 18ns output enable to output valid time assures that data will be present on the CPU's data pins within plenty of time to execute a zero wait-state read cycle. The address to $\overline{\text{CHIT}}$ delay of 30ns gives the synchronization logic enough time to adequately generate the bus retry sequence into the 68020. The write pulse into this RAM array is generated by the cache write pulse logic described in a subsequent paragraph.

The controller can be divided into three parts: cache enable/disable, hit/miss logic and cache write pulse generation. The enable/disable control is made of four chips, U10, U12B, U15A and B, U18A-C and is a simple address decoder with three output signals, Enable, Disable, and Reset. The three signals are mapped within the CPU space of the processor, and generate an acknowlege signal with zero wait states. The Enable and Disable commands toggle the cache enable flip flop, with the Enable signal also resetting the cache-tag to assure that a session is begun with the tag flushed of any stale

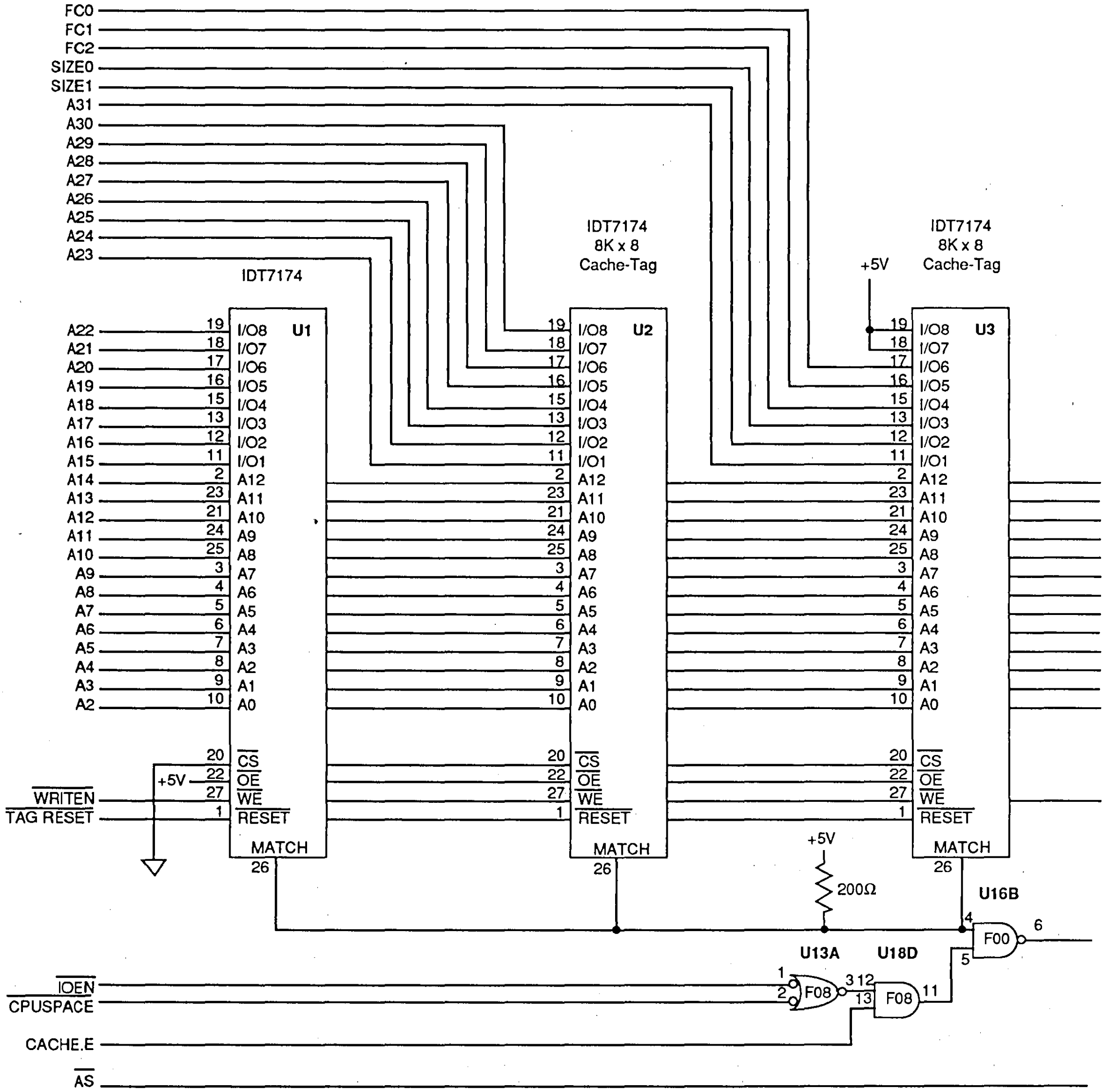


Figure 1. Cache Tag and Cache Data RAMs

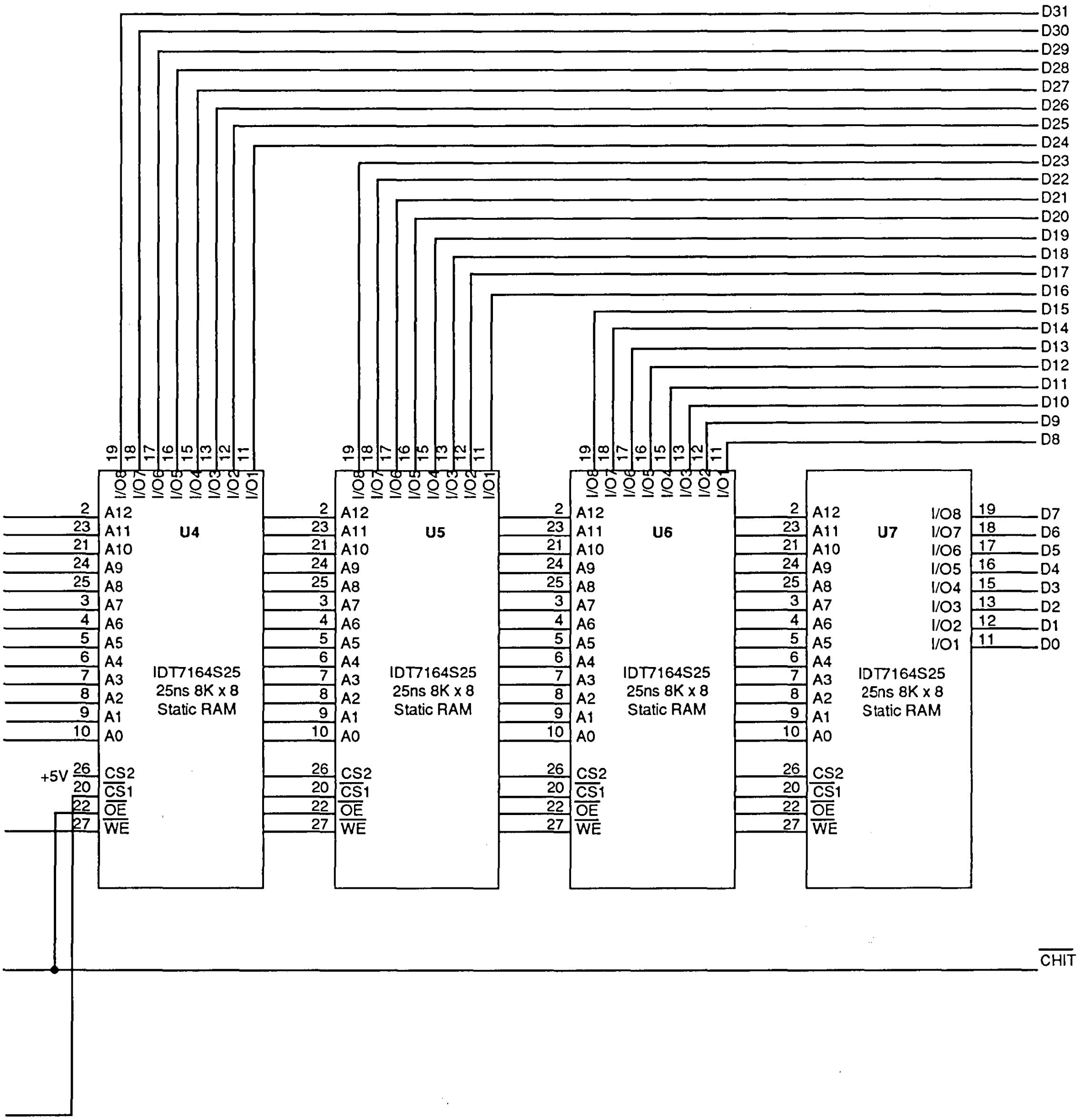


Figure 1. Cache Tag and Cache Data RAMs

data from a previous use. The Reset control is used to flush the cache for a context switch. A 25ns IDT7174 cache-tag RAM can be reset within 55ns, but the minimum address strobe pulse width of the 33MHz 68020 is 50ns, so a zero wait-state cycle can only be used for this operation if a 20ns cache-tag is specified.

The hit/miss logic consists of a series of two latches, U9A and U9B, which are timed from the address strobe with the 33MHz CPU clock and the 66MHz bus clock to sample the status of the cache-tag output as late as possible to allow for the cache-tag's access time, still adequately in advance of the trailing edge of the 68020's S4 cycle to assure that a $\overline{\text{BERR}}$ is generated soon enough for the CPU to recognize that it should attempt a bus retry. The retry sequence which is to be fed to the 68020 consists of the assertion of the $\overline{\text{DSACK}}$ signals during the S2 clock phase, followed by the assertion of the $\overline{\text{BERR}}$ and $\overline{\text{HALT}}$ signals during the S4 phase. Upon a cache miss, the CMISS signal is output to the system data buffers to allow data to be received from the system memory and I/O devices. The CMISS signal is also routed by U11B and U14A-D and is gated by the address strobe and the $\overline{\text{INHIBIT}}$ signal (explained below) to generate $\overline{\text{BERR}}$ and $\overline{\text{HALT}}$ inputs to the CPU. The third latch, U12A, is combined with the system reset and cache enable signals to enable/disable the cache's acknowledge and bus error signals. As a general rule, the acknowlege signals are sent to the CPU for all memory accesses, with U14 and U13D only being disabled by the $\overline{\text{INHIBIT}}$ signal. The $\overline{\text{INHIBIT}}$ signal is generated by the trailing edge of the address strobe of the cycle upon which a cache miss is detected, and continues until the trailing edge of the address strobe of

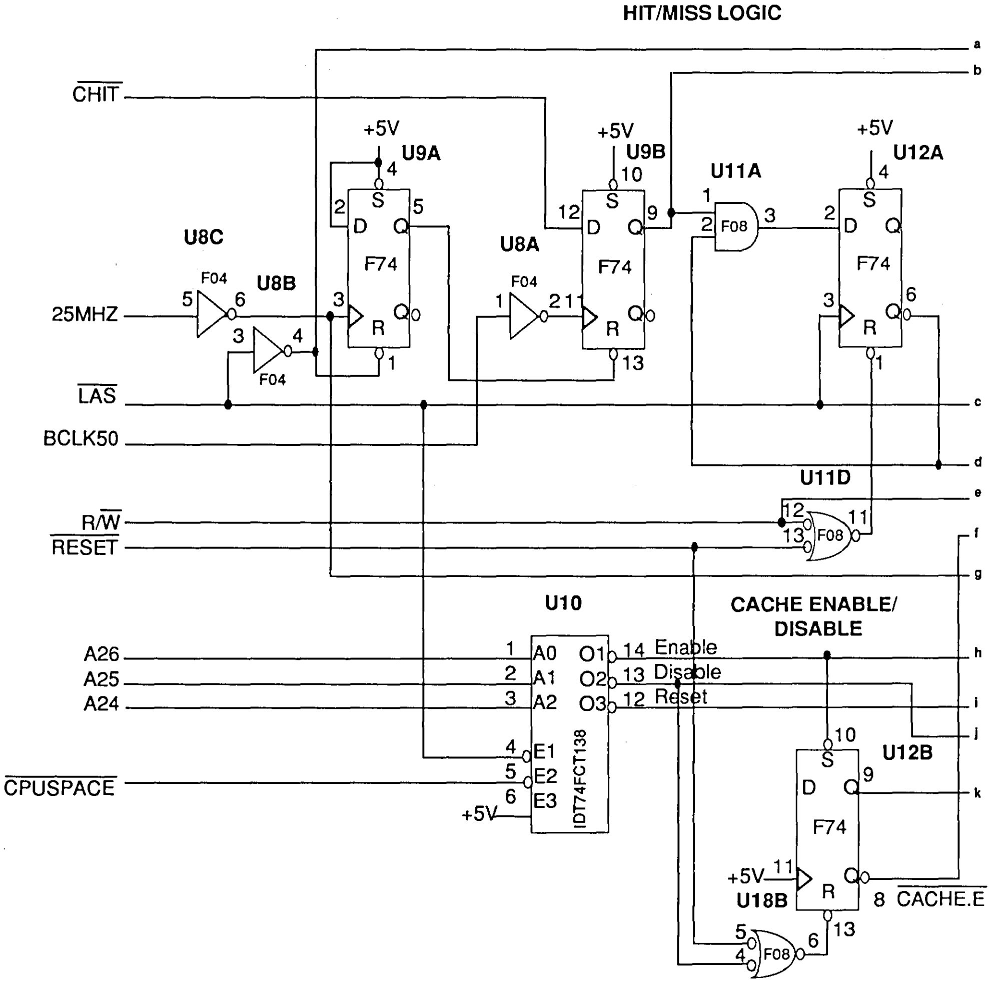


Figure 2. Cache Controller Logic

the next cycle, the cache update cycle. During either the second cycle of a cache miss or during a write cycle, or whenever the cache is disabled, the INHIBIT signal disallows the cache from generating DSACK, HALT, and BERR signals, thus leaving the system memory in control of the bus timing.

Cache write pulse generation is controlled by U17A and B and the surrounding logic. There are two conditions under which a cache write occurs in this design: all write cycles, and the second cycle of all cache misses. The first case is handled by routing the CPU's write pulse through U13C and U19A to the write strobe inputs of the cache-tag and data RAMs. The second case is slightly more complicated. A write strobe for the second cycle of a cache miss starts with the coincidence of an address strobe and the INHIBIT signal as detected by U19B, and continues until two 33MHz clock cycles after the external memory has generated either DSACK signal. The termination of this cycle is coincident with the time that the CPU strobes data into itself, and is timed by the circuit using U16A, U17A and B, and U13B. This follows the 68020's ability to receive the DSACK signals before read data is actually valid.

For clarity's sake, 74F00 series logic was selected over a PAL for this design. The use of a PAL and a wait state during tag reset could significantly loosen the specifications (and cost) of the tag RAMs used. With a 7.5ns PAL, the same cache could operate using a 35ns IDT7174. The configuration of the controller, as well as the basic architecture of the cache has been adapted from a Motorola application note, AN984, which implements a 25MHz cache in approximately 65 chips.

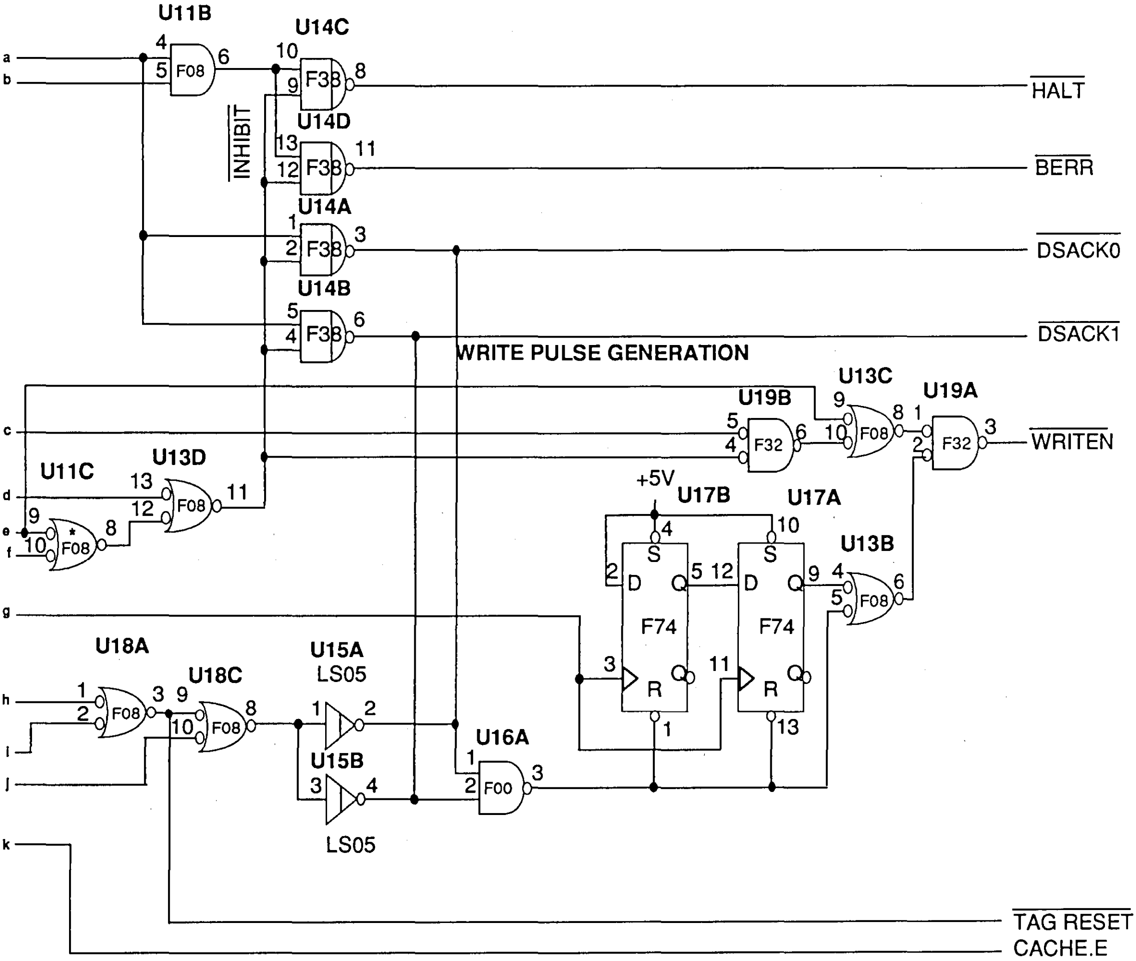
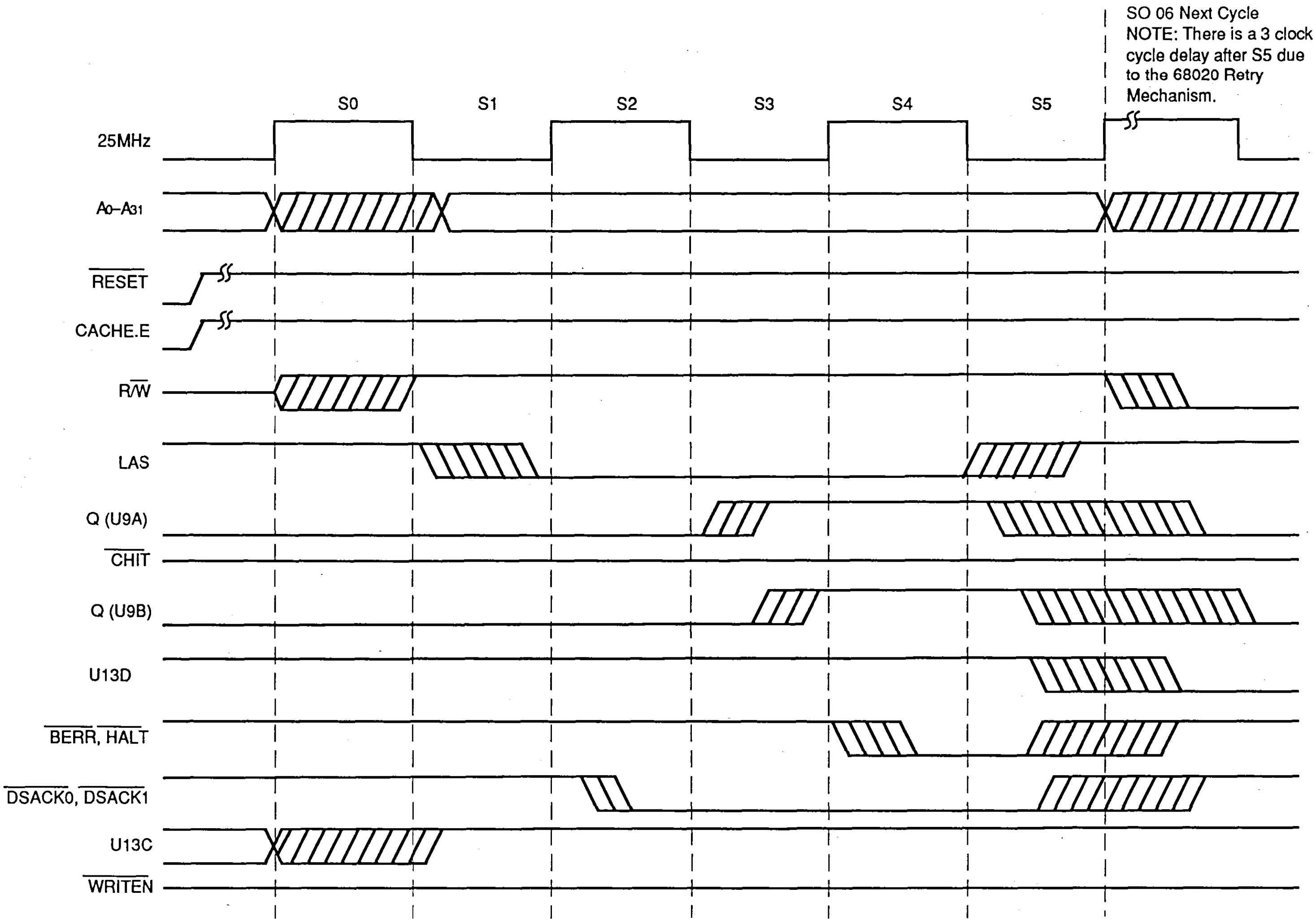
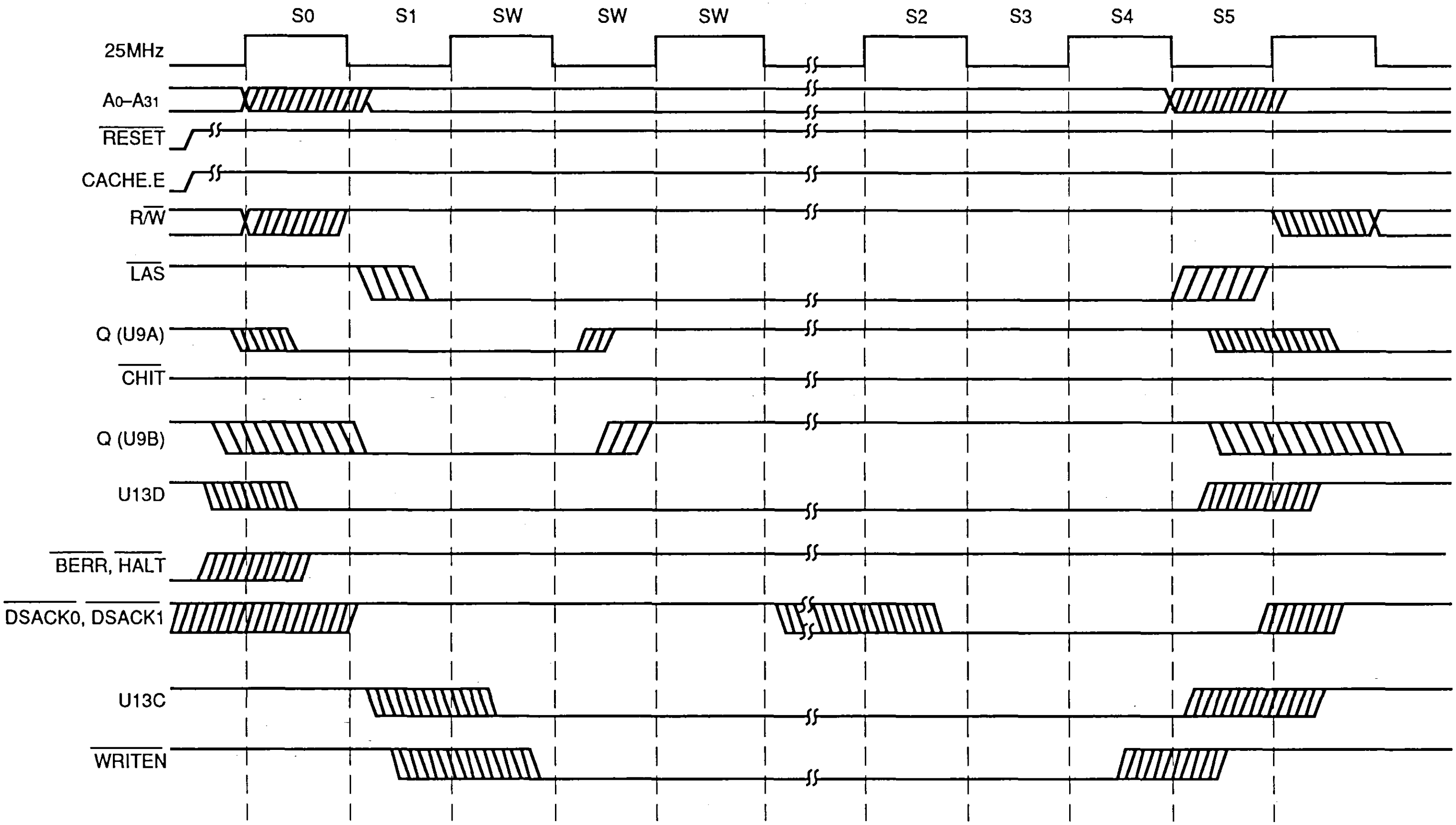


Figure 2. Cache Controller Logic

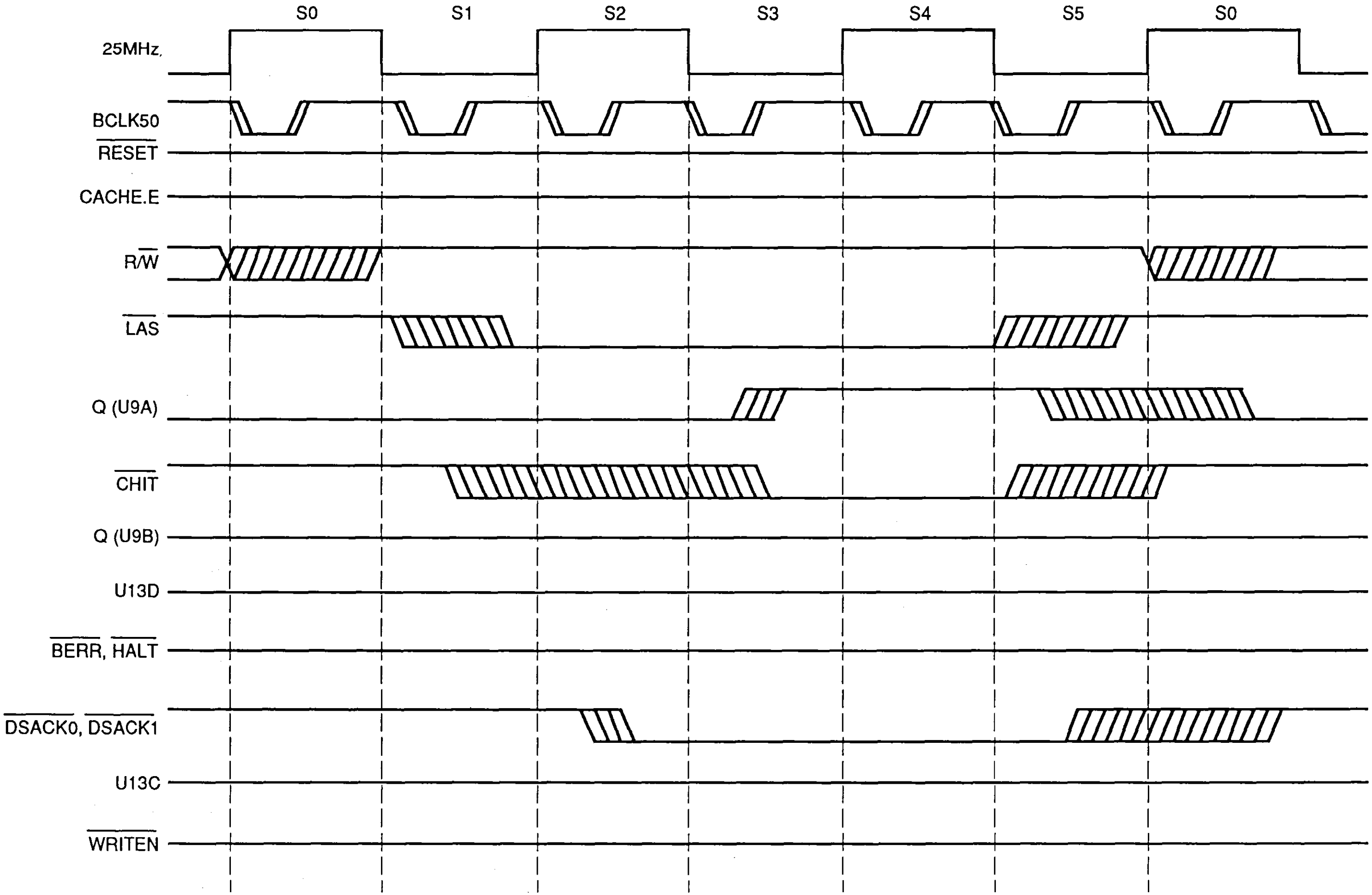


SO 06 Next Cycle
NOTE: There is a 3 clock cycle delay after S5 due to the 68020 Retry Mechanism.

Timing Diagram 1 – Cache Miss



Timing Diagram 2 – Retry of the Cache Miss Cycle



Timing Diagram 3 – Cache Hit

Integrated Device Technology, Inc.

RAMS FOR AN INTEL386™ CACHED MICROPROCESSOR SYSTEM

APPLICATION NOTE
AN-80

by Pat Kearns, Intel Corporation and Jim Handy, Integrated Device Technology, Inc.

The design of caches for microprocessor systems has often been avoided by design engineers because of the extra board space needed to implement them. Now, however, with the introduction of the Intel 82385 cache controller, the designer has a solution to the board space issue posed by caches. The 82385, because of its compatibility with a wide number of different types of static RAMs, allows the designer to improve the performance of an Intel386™ microprocessor-based system without unduly adding to the overall board space of the system. Further, because of the design of the Intel 82385 cache controller, and again because of its compatibility to a wide number of different types of static RAMs, the designer is able to implement a board space efficient two-way set-associative cache, allowing the optimum solution to the cache design problem.

Using chips from both Integrated Device Technology and Intel, a solution to a direct mapped cache is presented. In addition a number of different solutions to a two-way set-associative cache design are given for an i386™ microprocessor-based system. The solutions presented allow for the designer to select a cache design that is best suited for his application.

CACHE ASSOCIATIVITY

One of the most fundamental aspects of cache design with the 82385 cache controller is the associativity of the cache. When using the 82385, the designer has the choice between either using a direct mapped or two-way set-associative architecture.

In order to make the correct choice, the designer should first understand the definition of associativity. Associativity may be defined, architecturally, as the number of memory banks that are used for the data cache memory. For example, a direct mapped (or single-way set-associative) cache has a single bank of memory with every location in the data cache mapping line per line to the corresponding line offsets within any main memory page. A two-way set has two banks of memory with each line location (one in each memory bank) mapping to any page in main memory.

For a direct mapped cache, the architecture dictates that there will never be more than one piece of data at any unique line offset address in the data cache (the address of a data location in main memory is given by a unique page number and a non-unique line offset address). For example, since the main memory address locations page 2/line 6 and page 3/line 6 have the same line offset addresses (they have the same line number), they can never both be in a direct mapped cache at the same time. Conversely, page 2/line 6 and page 2/line 7 can be in the cache at the same time, since their line offset address differs (even though their page address is the same).

On the other hand, for a two-way set-associative cache, every location in the cache has two pages that it can be mapped to. This implies that there can be two pieces of data (one per cache way) at any one line offset address in the cache memory at the same time. To use the same example as in the previous paragraph, the two-way cache can maintain both page 2/line 6 (way A) and page 3/line 6 (way B) within the cache at the same time. A request for data from either page 2/line 6 or page 3/line 6 will result in a cache hit.

A consideration when deciding on whether to use a direct mapped cache or a two way set-associative cache is the relative performance between the two in regard to handling program structures. A program structure with code in one page of main memory which frequently calls a routine located in a different page in main memory can cause an extremely high miss rate if a direct mapped cache is used (assuming a high likelihood of line offset address conflicts). For example, a microprocessor fetches an instruction from page address X, with a line offset address Y. This instruction is stored in the cache until another instruction fetch from a page address Z but with the same line offset caused a cache miss to occur. If the program structure is such that these two addresses are in a loop, this causes a string of consecutive misses. This situation is often called "Thrashing".

On the other hand, a two-way set-associative cache handles programs that are on two different pages much more efficiently, since as stated, a two-way set-associative cache can have as many as two pieces of data at any unique line offset address in its cache, which helps significantly in alleviating the thrashing problem.

Even though a two-way set-associative cache has a higher immunity to thrashing, it is easy to see why designers have not raced to higher and higher levels of associativity. The main reason is, of course, that a two-way set-associative cache typically consumes up to twice as much circuitry as a direct-mapped cache. With typical circuits containing as many components as the one shown in Figure 3, this circuitry penalty has often not been considered worth the gain in performance shown in Figure 1.

82385 CACHE ARCHITECTURE AND OPERATION OVERVIEW

The 82385's architecture is specifically designed for either a 32Kbyte direct mapped or a 32Kbyte two-way set-associative cache arrangement. The cache directory architecture dictates that a direct-mapped design be 8K deep by 32-bits (for the 32-bit word length of the i386 CPU), or two banks of 4K by 32-bit words for a two-way set-associative design.

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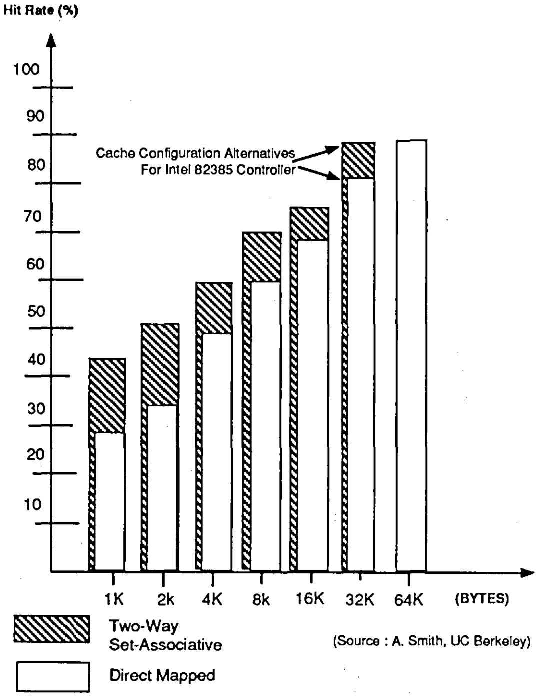

(Source : A. Smith, UC Berkeley)

Figure 1. Hit rate as a function of cache configuration

The 82385 cache architecture can be divided into four functional blocks. There is the cache controller state machine logic, the cache tag directory, the system/local bus cache directory multiplexer and the write buffer. The cache controller is designed to replicate the Intel386 microprocessor's front end which allows not only direct connection of the controller to the system bus, but it also enables the CPU to operate in pipeline mode with a cache connected, thus assuring the highest possible throughput. The cache directory is used to indicate the presence of the requested cache data in the external cache data RAM. It consists of 1024 tags, 8192 line valid bits, and 512 replacement algorithm bits (the tags hold the page numbers discussed in this article). In order to provide system coherency (in case a DMA or other bus master updates a cached memory location), the cache directory is multiplexed between the system bus and the Intel386 address bus via the on-chip multiplexer.

The state machine of the 82385 controls the interaction of the cache static RAM with the system bus and the CPU local bus. When the microprocessor operates out of the cache, it first strobes the cache controller with its address status line which in turn signals the cache controller and the cache static RAM address latch to latch the address bus. The cache controller responds by examining the cache directory to see if data for the requested address is in the cache. If the desired data is in the cache RAM, the cache controller asserts one of its cache output enable (COE#) signals (one output enable is used for a direct-mapped cache, two are used for a two-way set-associative cache). This, of course, enables the cache RAM's data output lines. Once the data is presented to the CPU's local data bus, the cache controller terminates the bus cycle by asserting its READYO# (Ready Out) signal which is gated to the i386 CPU's READY input port.

On a cache miss, the controller invalidates the corresponding cache location (by resetting the associated valid bits) and then performs a main memory read into both the CPU and the appropriate cache location by enabling the external system address latch and data transceivers with its associated control signals (BACP, BAOE#, LDSTB, DOE#, and BT/R#).

When the microprocessor writes data to the system memory, the 82385 also plays an important role. During a write cycle, the 82385 latches the i386 CPU address, data, and cycle definition signals, and the i386 CPU local bus cycle is completed without wait states, reducing the effective memory write cycle time. The 82385 waits for access to the system bus, then performs the write to main memory independent of the microprocessor. The i386 CPU is free to concurrently operate out of the 82385 cache via the i386 local bus.

The cache controller includes the necessary I/O and logic to monitor system bus DMA transfers. The BHOLD and BHOLD Acknowledge signals are used by the controller to manage external system bus transfers. On reception of a BHOLD signal, the controller (when programmed for master mode) will issue a BHOLD Acknowledge output signal to the requesting device. The requesting device then sends its data across the system bus which in turn is monitored by the cache controller via its snoop address bus (the multiplexer alternately presents to the cache directory the microprocessor address and the system bus address). Should the DMA write to a location which is currently in the cache memory, that location's valid bit will be invalidated so that the cache contents will not disagree with the contents of the main memory at the end of the DMA. Before the system bus transfer occurs however, an external device must assert the Snoop Enable signal input that feeds the controller. As well, a Snoop Strobe signal must be presented to the controller for the transfer of each system bus address so that the controller can latch the system address bus. Alternatively, during a DMA transfer, the contents of the cache may be emptied by asserting the FLUSH signal that feeds into the cache controller. Both the Snoop and the FLUSH are used to prevent the possibility of the processor operating out of the cache with stale data that has not been checked by the coherency logic during a system bus DMA transfer.

CHOOSING BETWEEN DIRECT MAPPED AND ASSOCIATIVE CACHES

Until now, the designer who wanted the added performance of two-way set-associative caches had to tolerate added component count, increased power, and increased board space. Such trade-offs often left the designer without a cost-effective solution to a two-way set-associative design. This is because, on one hand, a higher associativity offers higher throughput, but on the other hand, a higher associativity requires an inordinate number of chips.

SYSTEM THROUGHPUT AS A FUNCTION OF CACHE POLICIES

For a given cache memory size, the higher the associativity of the cache, the lower the overall miss rate (or the higher the hit rate). Figure 1 shows the hit rate for generic direct-mapped and two-way set-associative caches of various memory sizes.

As figure 1 shows, a two-way set-associative cache in general will have a higher hit rate than direct-mapped caches. Roughly speaking, a two-way set-associative cache has similar hit rate performance to a direct-mapped cache of twice the size. Thus an 8kB two-way set-associative cache has performance similar to that of a 16kB direct-mapped cache, and a 32kB two-way set-associative cache will have similar hit rate performance to a 64kB direct-mapped cache.

A cache with a higher hit rate will result in higher system performance. To see this clearly, let's look at a general 33MHz example. For this example system, fast page-mode dynamic RAM is used for main memory and we will assume:

- 70% of main memory reads and memory writes occur within the same DRAM page as the preceding memory reference. These cycles take two wait states (4 clocks).
- 30% of main memory reads and memory writes occur across a DRAM page boundary from the preceding memory reference. These cycles take six wait states (7 clocks).
- The cache hit rate accounts for about 82% of the memory cycles in a direct-mapped 32kB cache, and about 90% of the memory cycles in a two-way set-associative 32kB cache (see figure 1). Each of these cycles takes two clocks. All other memory references are to main memory at the time penalties listed above.

Based on the above assumptions, a 33MHz CPU's average number of clocks per memory cycle without a cache would be:

(30% * 7 clocks) + (70% * 4 clocks) = 4.9 clocks per memory cycle while a 33MHz system which used a 32kB direct-mapped cache would perform at:

(82% * 2 clocks)+ [18% * ((30% * 7 clocks) + (70% * 4 clocks))] = 2.522 clocks per memory cycle resulting in a performance improvement over a non-cached system of 48.5%:

(4.9 - 2.522)/4.9 = 0.485

In a similar analysis, a 33MHz system which used a 32kB two-way set-associative cache would perform at:

(90% * 2 clocks)+ [10% * ((30% * 7 clocks) + (70% * 4 clocks))] = 2.29 clocks per memory cycle

This will result in a performance improvement over a non-cached system of 53.3%:

(4.9 - 2.29)/4.9 = 0.533 and nearly a 10% performance improvement over the direct-mapped cache of the same size:

(2.522 - 2.29)/2.522 = 0.092

This analysis can be carried over to Intel386™ specific systems. For Intel 82385 cache designs, the two-way set-associative configuration will generally provide better performance than the direct-mapped configuration. In addition, the 82385 further improves performance by optimizing the timing interfaces on both the processor bus and the system bus. An 82385 32kB cache in the two-way set-associative configuration will thus provide comparable performance to a generic 64kB direct-mapped cache.

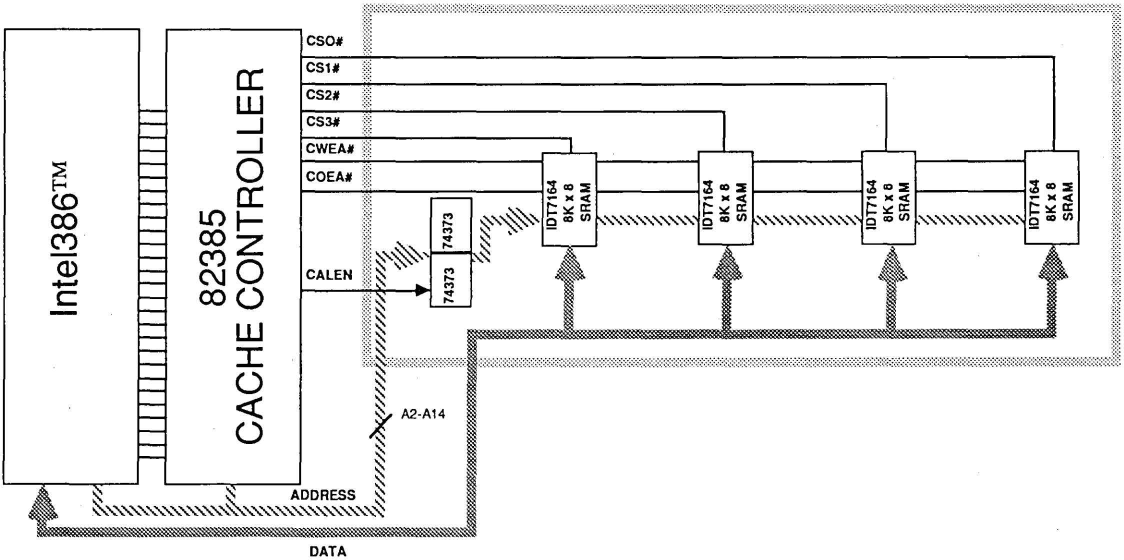

Figure 2. Direct-mapped Cache Using 8K x 8 Static RAMs

INTERFACING STATIC RAM TO THE CACHE CONTROLLER

The static RAM interface for the two-way set-associative cache is relatively simple and straightforward. It consists of a 32-Bit data bus, a 12-Bit Address Bus (the lower offset addresses, A2-A13), a cache RAM output enable signal for each memory bank (COEA# and COEB#), two bank write enable signals (CWEA# and CWEB#), a directional signal to control the flow the optional data transceivers (CT/R#), and an address latch enable signal (CALEN). The data transceiver interface also supports four byte select signals (CS0#-CS3#) which are used by the i386 CPU when it needs to write data to the cache on a byte basis.

For the direct mapped cache, the interface is even simpler. All the standard signals are the same as for the two-way set-associative cache except that the write enable and output enable signals for bank B are not used (or are used in parallel), and an additional address line (A14) from the i386 CPU is used to account for the added depth of the cache.

CHOOSING A RAM FOR DIRECT MAPPED ARCHITECTURE

Choosing a static RAM for a direct-mapped architecture for the 82385 is simple. Since the cache RAM must consist of a single 8Kx32-bit bank with latched addresses and separate byte enables, four 8Kx8 static RAMs and two octal latches can be used to easily configure the system interface and meet the system memory requirements (Figure 2). Due to the nature of certain faster steppings of the 82385 and the COE and CWE signals they generate, an 8Kx8 must be used which can tolerate the simultaneous assertion of output enable and write enable signals. Here the IDT7164, an 8Kx8 static RAM, is the perfect choice since it meets both the static RAM configuration and the simultaneous assertion requirements. Further, the IDT7164's 25nS access time allows for the 33MHz cycle time to be met, and its 10ns output enable time supports the fast requirements of the COEA# and COEB# signals. Finally, the direct-mapped cache consumes little board space (about 4 square inches for the RAM in a through-hole configuration) and, as mentioned above, can improve system throughput by nearly 50% in the example 33MHz system.

CHOOSING A RAM FOR A 2-WAY SET-ASSOCIATIVE SYSTEM

The two-way set-associative configuration is generally considered the more attractive solution to the cache problem from the standpoint of system throughput, but consumes more board space than a direct-mapped cache in most implementations. Three approaches to a two-way set-associative cache are presented for evaluation below.

THE 4Kx4 SOLUTION

One good approach (shown in Intel's 82385 data sheet) for a two-way set-associative cache is to use a 4Kx4 bit static RAM like the IDT6168 (Figure 3). This design incorporates sixteen 4Kx4 IDT6168 static RAMs, two IDT74FCT373 octal address latches, and eight IDT74FCT245 octal transceivers.

Two AND gates are shown in the diagram as inverted-input NOR gates. These are used to enable the bidirectional transcievers during either a read or a write cycle, and have been eliminated in designs using later, faster steppings of the 82385. In these steppings the output enable pins (COEA#, COEB#) go active simultaneously with the write enable pins (CWEA#, CWEB#) so that the output enable inputs of the transceivers can be driven directly by the 82385 rather than by the outputs of the AND gates. This is an important plus at high speeds, where the cumulative delays caused by the transceiv-

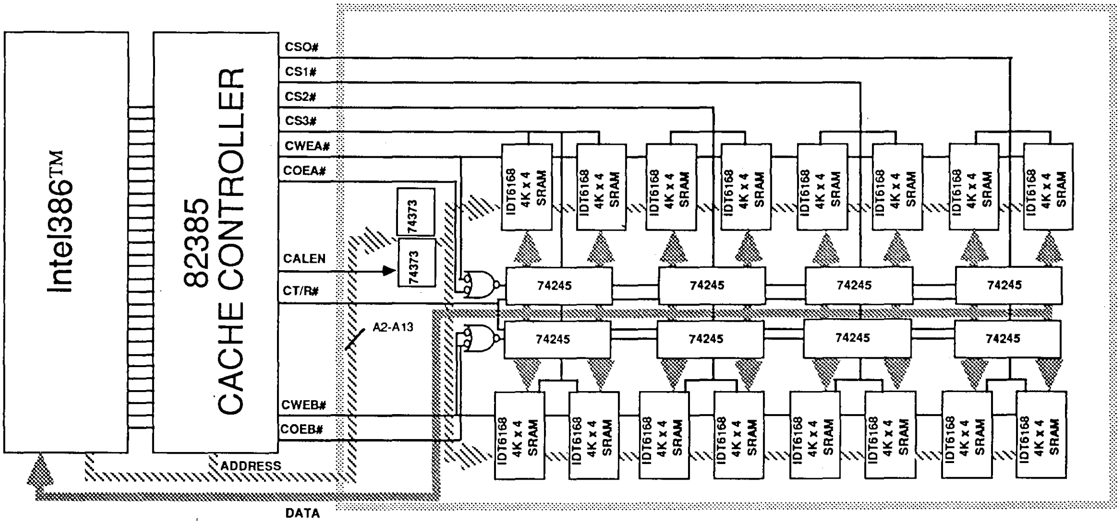

Figure 3. Two-way Set-associative Cache Using 4K x 4 Static RAMs

ers and the AND gates can delay the data path to the point where it becomes too slow to support valid cache write cycles using the fastest currently available static RAMs.

The 4Kx4 solution offers a fast two-way set-associative cache design with a low miss rate. A design using 20ns RAMs will operate with the 33MHz Intel386 CPU, and has about a 10% higher throughput than the direct mapped cache design. The design, however, needs about twice as much board space as the direct mapped solution.

THE LATCHED 4Kx16 SOLUTION

A better solution to the two-way set-associative cache design which saves board space and chip count is obtained by using an offshoot of the JEDEC standard 4Kx16 static RAM (Figure 4). The design incorporates four IDT71586 4Kx16 CacheRAMs. The IDT71586 is a 4Kx16 static RAM which incorporates address latches specifically for caches like those required in an Intel386/82385-based system. It allows the creation of a two-way set-associative design without a cost/ performance penalty over a direct mapped design.

Another advantage of the 4Kx16 solution, is that the design can use slower static RAMs than those required by the 4Kx4 solution since the function of the octal transceivers is integrated into the chip. The octal transceiver chips, which are necessary in the 4Kx4 solution, are not needed for the 4Kx16 solution since the IDT71586 has a fast (10ns) output enable pin to control output data flow.

This allows static RAMs with an access time of 25nS to be used to support a 33MHz processor, as opposed to the 20nS 4Kx4s required in the solution discussed previously.

In addition to offering nearly a 65% board space savings over the 4Kx4 solution and reducing the required chip count, the 4Kx16 solution also offers an easy signal interface. This is provided by the IDT71586's two separate chip select pins, upper and lower byte enable, which precisely match the i386 CPU's byte-oriented addressing capability. Furthermore, since the IDT7186's write enable and output enable signals may be activated simultaneously, it can accommodate all steppings of the 82385.

As can be seen from Table 1, the IDT71586 offers the best overall power, component count and board size for a two-way set-associative cache design. Because of its configuration and the incorporation of address latches and internal data bus transceivers on the IDT71586, the total cache, including the cache controller, is reduced to five ICs.

The IDT71586 is a 4Kx16 static RAM that latches the address bus into the address input pins upon application of the ALEN input which is provided by the cache controller's CALEN line. The CSU and CSL byte-enable inputs of the IDT71586 are connected to the cache controller signals CS0#-CS3#. These signals are used to select the individual bytes in the cache memory for byte operations. The associated IDT71586's write enable lines are connected to the CWEA# and CWEB# lines of the controller while the IDT71586's output enable signals are driven by the controller's COEA# and COEB# lines.

The critical timing parameters dictating the static RAM selection are the output enable time and the address access time for the read operation. Since the IDT71586 includes an output enable pin and on-board latches it is able to meet Intel's recommended non-buffered cache times for all speed grades. For a read hit, the static RAMs are required to provide data less than 35nS after the address is output to keep up with a controller operating at 33MHz. Also, the data must become valid within 10ns of the assertion of the output enable. The write cycle time of the RAM must be less than 36nS. These specifications are all easily met by the IDT71586.

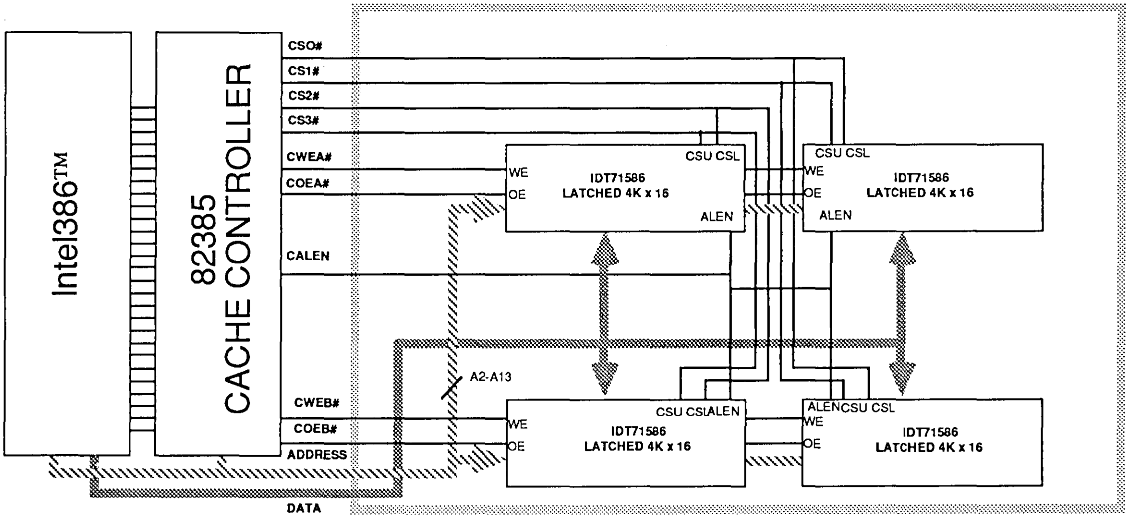

Figure 3. Two-way Set-associative Cache Using 4K x 16 Static RAMs

SRAM Configuration	# ICs	Board Size Square Inches Surface Mount	Board Size Square Inches Through Hole	Power Max. mA
Direct Mapped				
8K x 8 (IDT7164)	6	1.8	4.1	630
Two-Way Set Associative				
4K x 4 (IDT6168)	27	5.3	8.4	1770
Latched				
4K x 16 (IDT71586)	4	1.9	5.0	640

NOTE: 2993 tbl 01

1. The table illustrates that the optimum solution for an Intel 82385-based cache memory system is the IDT71586 4K x 16 Latched SRAM in a two-way set configuration. The designer, with a small penalty in size and power, gains the benefits of a small IC count and the performance advantages of a two-way set associative cache architecture.

CONCLUSION/SUMMARY

When designing caches, the static RAM selection is a critical concern. A poorly selected RAM will unnecessarily consume board space and increase power consumption. Static RAMs with on-board latches and output enable functions are available to improve the cost/performance ratio of the overall system.

To maximize throughput of a cache design, the designer would use a two-way set-associative configuration. However, such configurations often consume too much board space and power to be an attractive solution. Here, the IDT71586 4Kx16 latched static RAM is the designer's preference since it allows for a cost-performance optimized two-way set design in about the same amount of space as a direct-mapped cache. The IDT71586 which incorporates byte select pins, address latches and an output enable function gives the designer the added throughput, a simple logic design and the necessary tightly coupled interface to the Intel386/82385 signals.

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Performance Trade-Offs For Microprocessor Cache Memories, Donald B. Alpert & Michael J. Flynn, IEEE Micro, August 1988

Cache Accelerates Operation of 32-Bit Microprocessor Systems, Robert Nalesnik, EDN, May 28, 1987

Integrated Device Technology, Inc.

BURST CACHE RAM FOR THE i486

APPLICATION NOTE AN-81

by Kelly Maas

This note is intended to introduce you to the IDT71589, a 32Kx9 RAM designed specifically to simplify the design of secondary caches for the i486 microprocessor. We will outline its features and how they reduce logic and timing concerns. Certain aspects of cache operation and design are also addressed. A complete i486 cache design using the 71589 is the subject of IDT Application Note 78.

THE IDT71589

The two key features of the 71589 are a 2-bit burst counter and a synchronous interface. These reduce cache parts count and simplify timing. The 71589 is housed in the same 32-pin 300 mil packages as a conventional 32Kx9, but two pins were added to the usual SRAM control interface. These are the CLK and $\overline{\text{ADS}}$ (Address Status) signals from the i486. The 71589 uses these to synchronize its timing with the CPU, and to identify the beginning of a bus cycle. To facilitate the quick and quiet operation of this memory, a second ground pin was added.

TYPICAL CACHE CONFIGURATION

Figure 1 shows a block diagram of a basic 128K byte direct mapped i486 secondary cache. Since the 71589 does not contain any system control logic, a separate cache controller is required. This may be in the form of an off-the-shelf cache controller, or as an ASIC or multi-component custom design. The cache itself consists of this control logic, tag RAMs, and four 71589s, as well as buffer logic between the cache/CPU and the rest of the system. The 71589 CLK input is the same signal as the CLK input to the i486. The i486 drives the $\overline{\text{ADS}}$ to each 71589. Likewise, the data bus is a direct connection between the 71589s and the i486, and A_0-A_{14} on the 71589 connect to A_2-A_{16} on the i486. Timing for the 71589 is such that i486 addresses may be optionally buffered in order to reduce loading. The three remaining 71589 signals — $\overline{\text{CS}}$, $\overline{\text{OE}}$ and $\overline{\text{WE}}$ — are all generated by the cache controller.

Separate cache tag RAMs are required unless they are incorporated in the controller. Assuming that the secondary cache is the primary cache format of a 16 byte line size and one tag per line, our secondary cache requires (128K/16=) 8K tags. Since the tag consists of those address bits that are not used to address the cache itself, the tag of our simple cache consists of CPU address bits A_{17}-A_{31}, which are connected to the data pins of the tag RAMs. Address bits A_4-A_{16} are used to address the tags. Address bits A_2 and A_3 specify the word within the line and have no association with the tag. As with the 71589, tag RAM control signals are generated by the cache control logic.

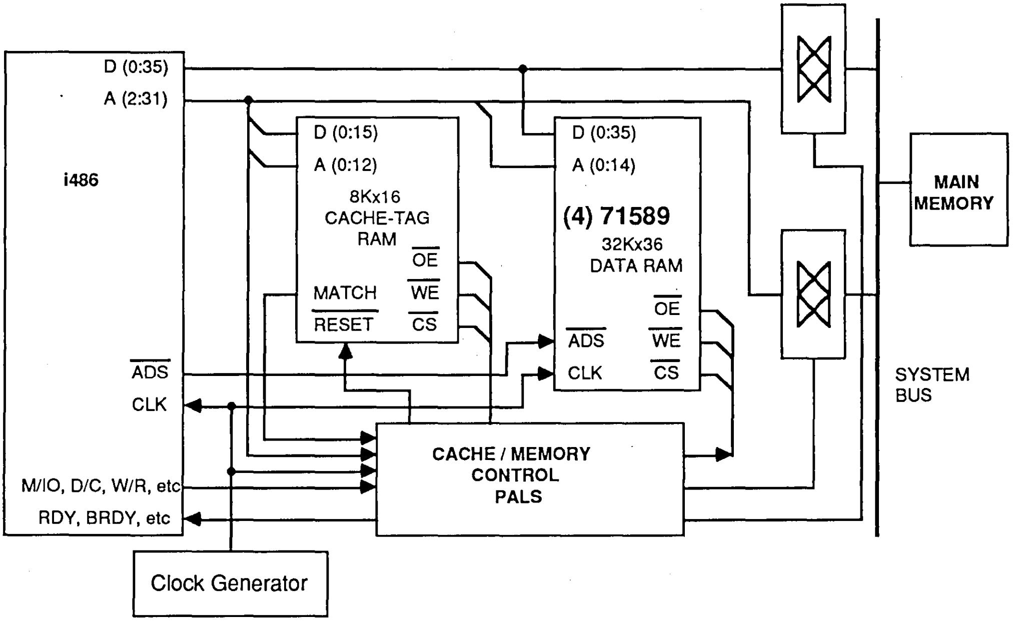

Figure 1. Direct-Mapped 128K Byte Secondary Cache

Although Figure 1 shows a direct mapped 128K byte cache, the 71589 is in no way limited to such applications. It is general enough that other cache configurations can be achieved simply by changing the controller. Deeper caches, such as 64K x 36 or 128K x 36 are easily implemented with a few additional control signals. Each 32K x 36 block requires its own OE for output control. To control writes, either separate WE signals with a common CS, or separate CS signals with a common WE are required. Thus, a 64K x 36 cache requires five 71589 control signals, while the 32K x 36 cache requires three control signals. Ample time exists to generate these additional control signals by decoding address bits since the address is valid from the i486 more than one cycle before the read or write.

These 71589 control requirements apply in exactly the same way to a set-associative cache, although the set-associative cache requires additional logic and memory to implement a replacement algorithm. Since the 71589 is not partitionable, the minimal 2-way set associative cache is 2(32K x 36) or 256K bytes.

In either case, a cache consisting of a large number of 71589s may use address buffers to reduce loading on the i486 without impacting cache timing.

IDT71589 OPERATION

Operation of the 71589 is keyed directly to the i486 and is not complicated. First, all input signals except OE are synchronous. Although most SRAM users are unaccustomed to synchronous memory interfaces, it actually makes design of an i486 secondary cache much simpler. As with the CPU itself, 71589 timing is referenced to the rising edge of the clock. Simple setup and hold times with respect to this edge is almost the only timing involved. Signals generated by control logic will be naturally stable during these times. Timing relationships are shown in Figure 2, which shows part of a burst read.

Every bus cycle begins with the assertion of ADS by the i486. On the first clock (rising edge) with ADS low, the 71589 registers the entire address, resets the counter and begins a read. (ADS must have been sampled high in the previous cycle.) In the event of a read hit by the CPU, OE is asserted and WE is negated. So long as CS is held low, each clock will increment the 71589's internal address counter and the next word of the burst read is presented to the i486 in accordance with its setup and hold requirements. As required by the i486, the sequencing follows a special order that is determined by the initial address. The 71589 generates the second address of a burst by complementing the least significant bit of the registered address, the third address by complementing the second LSB, and the fourth address by complementing both bits. Figure 3 shows a burst read.

If ADS is maintained low for more than one cycle, the 71589 will not be affected. Only when ADS is sampled high then low again will the 71589 start a new bus cycle as described above. Also, CS and WE are ignored during this initiation cycle.

Just as wait states are added to i486 bus cycles by maintaining RDY and BRDY inactive, wait states are added to the 71589 by maintaining CS inactive. When CS is sampled high, the 71589 counter does not increment and the data read is unchanged. A burst read with wait states may be required when data in a copy-back cache is being copied back to main memory. This is shown in Figure 4. Note that CS differs from the usual chip select function since it does not disable the outputs when negated. WE also has no effect on the output buffers. OE alone enables and disables the outputs.

As with read cycles, write cycles begin with the assertion of ADS, the resetting of the counter, and the registering of the address. The first write may be performed in the next clock cycle by asserting CS and WE. If the 71589 samples both CS and WE low, it will register the data at the same time and write it with an internally generated write pulse. Since all three of

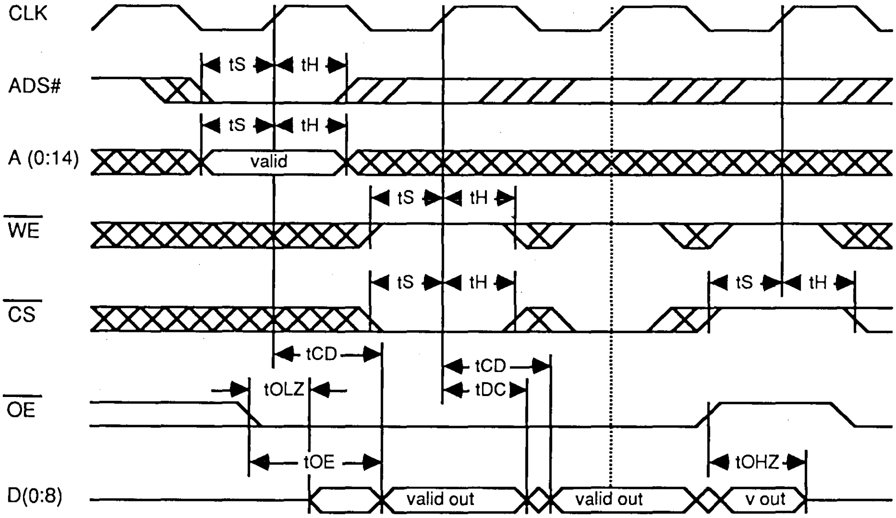

Figure 2. IDT71589 Timing Relationships

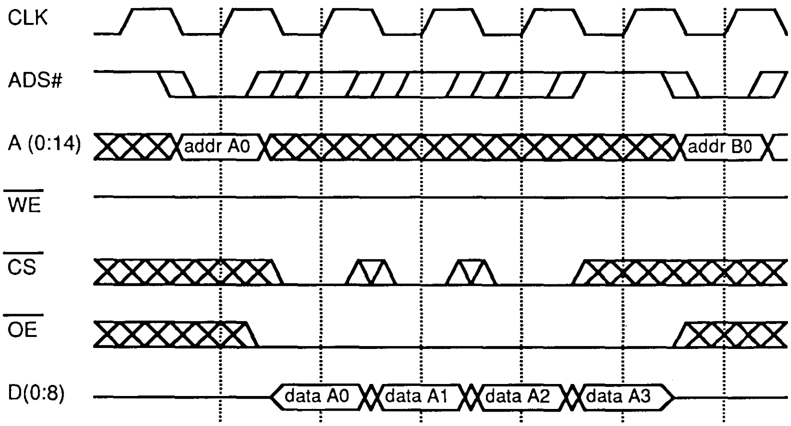

Figure 3. IDT71589 Burst Read Cycle

these signals are synchronous, they only need to be valid during the rising clock edge. There is no need for the controller to generate a write pulse that carefully matches the period of valid data from the CPU. Don't forget to (asynchronously) negate $\overline{OE}$ before the data is presented to the 71589. Figure 5 shows a single 71589 write cycle.

Although the i486 performs only single write cycles, burst writes are also possible. In fact, every cache line refill can be a burst write. On every clock cycle, if $\overline{CS}$ and $\overline{WE}$ are asserted, the data present on the data bus at that time is written into the 71589. Since line refills are rather slow due to main memory latency, wait states are usually required during burst writes, as shown in Figure 6. Again, this is controlled by $\overline{CS}$. When $\overline{CS}$ is sampled high during a burst write, both the counter increment and write operations are blocked. Thus, $\overline{WE}$ is normally held low during the entire write burst, and only $\overline{CS}$ is asserted and negated as required.

To idle a 71589 that is not being accessed despite the generation of $\overline{ADS}$ strobes, $\overline{OE}$ is negated to disable the data bus, and either $\overline{CS}$ or $\overline{WE}$ is negated to disable writing to it. With $\overline{CS}$ low and $\overline{WE}$ high, the burst counter will increment but nothing will happen to the memory contents.

If more than four memory accesses are performed in a burst, the address counter will wrap around. Also, once a burst cycle is initiated, it is not exclusively a read burst or write burst. In fact, reads and writes may be mixed in any order without reasserting $\overline{ADS}$. Remember that counter incrementing is controlled only by $\overline{CS}$ and is independent of any other inputs except $\overline{ADS}$.

These features may be usefully combined in copy-back caches during the replacement of a dirty cache line with a new line from main memory. If a secondary cache read is determined to be a miss, and the new line from main memory must replace a line in the secondary cache that is dirty (contains

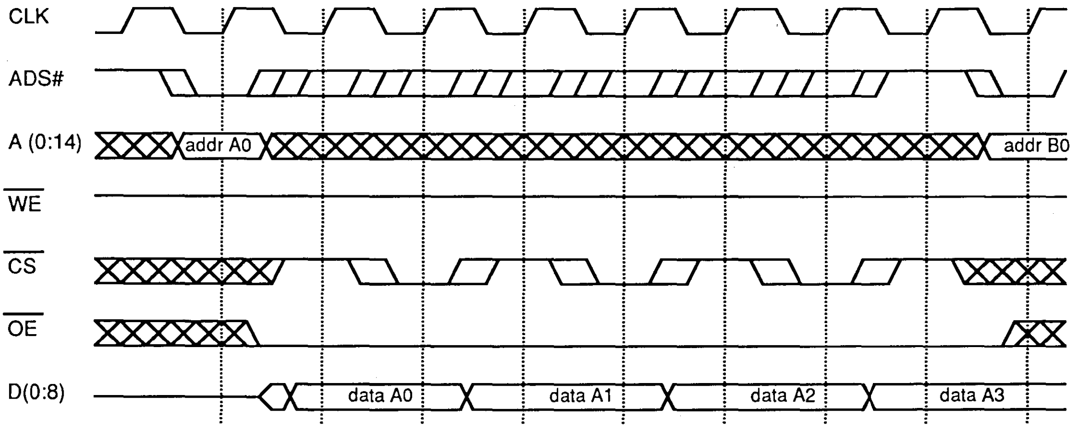

Figure 4. IDT71589 Burst Read Cycle with Wait States

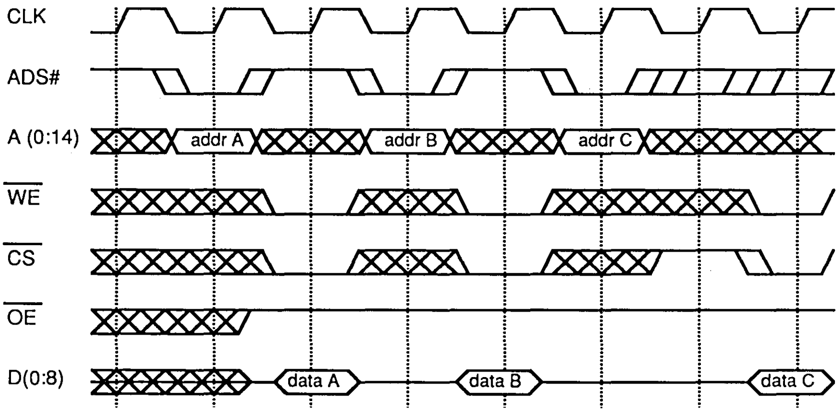

Figure 5. IDT71589 Single Write Cycles

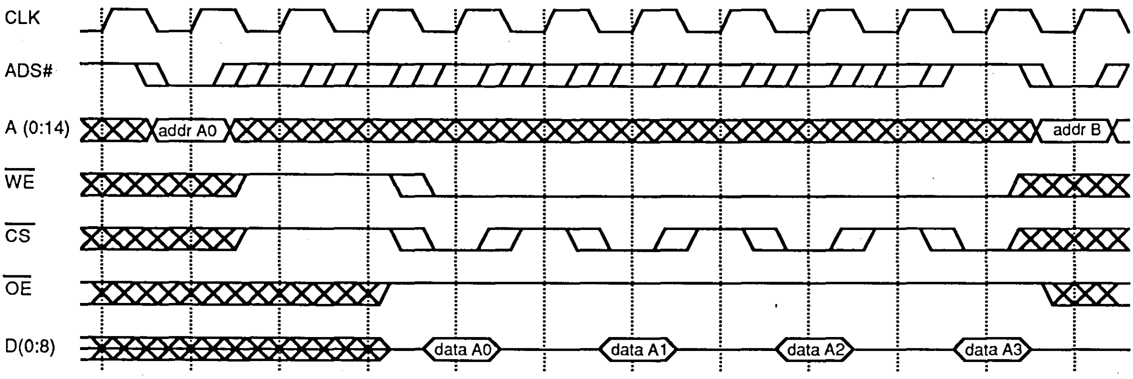

Figure 6. IDT71589 Burst Write Cycle with Wait States

data that is more current than main memory), the dirty line may be transferred to main memory, then the new line may be transferred from main memory at once into both the primary and secondary caches, all without reasserting $\overline{\text{ADS}}$. Such a burst read-write cycle is shown in Figure 7.

COPY-BACK EVICTION

Although it is not specific to the 71589, the following scheme is proposed for minimizing CPU delay when performing a line replacement. Rather than writing directly from the secondary cache (71589s) into main memory, the dirty line may first be written into a write buffer. This can be done in the minimum burst read time of 5 clock cycles. The i486 is in wait states and is so far uninvolved. Meanwhile, the controller would have initiated a main memory read of the requested line the moment it was known that the cache read was a miss. As soon as the data is available from main memory, it is bursted into both the CPU and the 71589s simultaneously. The CPU resumes operation once the first word is returned. Once the entire line has been transferred, the write buffer contents are written back to main memory.

ADDITIONAL CONSIDERATIONS

One additional concern occurs when the designer elects to implement a secondary cache with a copy-back replacement algorithm or a line size larger than four words. While the CPU normally asserts the required $\overline{\text{ADS}}$ signal, these situations require that $\overline{\text{ADS}}$ also be generated by another source. In the first case, a system (non-CPU) read that results in a snoop hit of a dirty cache line requires that this word or line be read from the 71589. Since the CPU is not involved, the cache controller generates the $\overline{\text{ADS}}$ signal for the 71589. In the second case, once a four word line refill has been performed to satisfy the i486, the controller will generate an alternate $\overline{\text{ADS}}$ strobe and continue filling the remainder of the secondary cache's larger line from main memory.

To deliver this alternate $\overline{\text{ADS}}$ to the RAM, HOLD is asserted to the i486 for one or two cycles. This forces the CPU to float its bus, including $\overline{\text{ADS}}$, allowing the controller to assert $\overline{\text{ADS}}$ for one cycle. An alternative at slower speeds (33 MHz and less) is to simply gate the two $\overline{\text{ADS}}$ signals together with a negative logic OR gate to generate the 71589 $\overline{\text{ADS}}$.

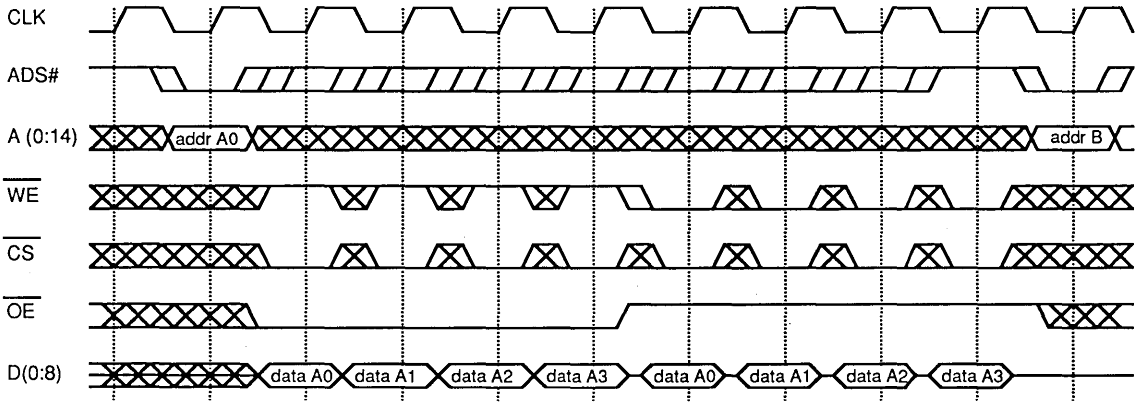

Figure 7. IDT71589 Burst Read/Write Cycle with One ADS Strobe

IDT71589 VS STANDARD RAMS

Non-synchronous, non-burst RAMs are ill suited to i486 caches. In addition to the additional logic, an external address burst counter interferes directly with burst read access times. At 33 MHz, with an i486 data setup time of 5 ns, data must be available 30 - 5 = 25 ns after a clock edge. With a 7.5 ns PLD as the counter, a 17.5 ns RAM is required. Although interleaving solves this problem, it complicates the design, increases board space and parts count, and doesn't solve write cycle problems.

An even greater design challenge exists in achieving zero wait state writes with conventional SRAMs, something that should be an important goal since every i486 write cycle is propagated through the primary cache to the secondary cache. Again at 33 MHz, data from the i486 is guaranteed to be valid (30-18 =) 12 ns before the end of the second clock cycle of a read, and is guaranteed to be valid only 3 ns into the next cycle. The only reasonable way to generate a write pulse is from the clock, specifically during the low portion of the second clock period. All timing parameters are easily met except for the RAM data hold time, which is normally specified as 0 ns. The write pulse, being generated by control logic with CLK as an input, must naturally trail CLK by some delay. Currently no 3 ns TTL logic exists, resulting in a timing violation. Buffering of the data would increase the data hold time, but it would decrease write cycle data setup time as well as required read cycle access time.

In other timing concerns, it is easy to calculate the required cache tag address to match time required for the 71589. The path is address valid delay, tag address to match, logic, then to BRDY on the i486 and to WE on the 71589, all within two clock cycles. At 33 MHz, the setup times for BRDY and WE are 5 ns and 4 ns respectively. Address to match is therefore 2(30) - 16 - 7.5 - 5 = 31.5 ns, assuming a 7.5 ns PLD.

Integrated Device Technology, Inc.

USING HIGH-SPEED 8K x 8 RAMS

TECHNICAL
NOTE
TN-04

by Michael J. Miller

INTRODUCTION

Integrated Device Technology provides two high-speed CMOS 8K x 8 static RAMs for use in high-performance memory applications. These sophisticated static RAMs are suitable for incorporation in main memories and caches for the current generation of 25MHz 32-bit microprocessors, such as the Motorola 68020 and the Intel 80386. These two CMOS RAMs have an address-to-data access time of 30ns. Using these static RAMs together with the FCT family, which is a memory interface family provided by IDT, will result in very high-performance memory systems.

USING THE IDT7164

The IDT7164 is a 28-pin industry standard 8K x 8 CMOS static RAM. It has a chip select and address access time of 30ns. The block diagram in Figure 1 shows the IDT7164 in a typical application where the address bus is decoded to generate a chip select and the lower order address lines provide specific location selection inside the 8K x 8. The IDT74FCT521A is an 8-bit address comparator which generates an active low output signal whenever there is a match. The address-to-match output is 7.2ns commercial. The IDT74FCT138A is used as an address decoder. This is a one-of-eight selection device which can be used to take mid-range addresses and select one out of eight possible enables. The enable signals are then connected to eight 8K x 8 static RAMs. The address-to-enable-out time is 5.8ns. The sum total of the memory system shown is 43ns.

USING THE IDT7165

The IDT7165 is a more sophisticated version of the 8K x 8 static RAM. The No Connect pin in the industry standard is used as a bulk clear for this static RAM. By pulsing this control line low for 60ns, the entire contents of the 8K x 8 static RAM is cleared to a value of zero. This is an important function for systems which need to guarantee all locations are zero at power up time. For software, this can be very convenient because when the initial program is loaded in, it is guaranteed that all locations are zero without having to write them all, thus saving a lot of time. Clearing the memory at system reset also removes the nasty bug that some programs may run slightly differently each time the computer is powered on because the program inadvertently reads a location that has not been written to.

As today's static RAMs are utilizing ever decreasing transistor geometries, the probability of data still being intact when power is turned off and then turned back on increases. This effect is contrary to the requirements for data secure systems. Data security is not only important for military applications, but also commercial applications where data encryption or confidential data may be involved.

Incorporated on the IDT7165 8K x 8 static RAM are two chip selects just like the industry standard version. However, these two chip selects have slightly different operation. The active HIGH chip select is a chip select that, when disabled, puts the RAM into a low-power standby mode. This allows gating of the data bus so that, as the data bus floats in tri-state, the input buffers do not consume excessive power. The active LOW chip select, on the other hand, does not gate the data bus, providing a fast access path. This access path is 10ns faster than the active HIGH chip select, yielding a chip-select-bar-to-data-access time of 20ns. The block diagram in Figure 2 shows a configuration very similar to Figure 1. The difference, because of the fast chip select time, is that the delay time of the address comparator and decode selector are in parallel with part of the address access time. Therefore, the sum total access time from the address bus through the comparator decode selector is 33ns.

CONCLUSION

While the IDT7164 is an industry standard 8K x 8 with very high performance, the IDT7165 can provide increased performance with extra features such as bulk clear. Both of these devices are very suitable for inclusion into designs incorporating the current generation of 32-bit microprocessors.

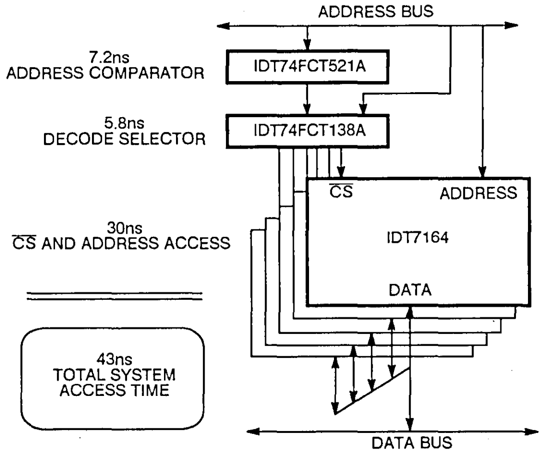

Figure 1. IDT7164 30ns Address and Chip Select Access

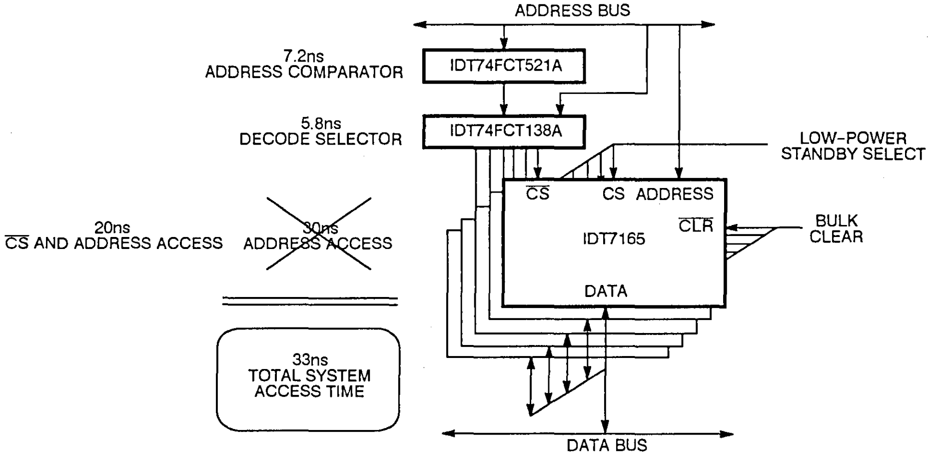

Figure 2. IDT7165 20ns Chip Select Access

Integrated Device Technology, Inc.

FAST RAMs GIVE LOWEST POWER

TECHNICAL
NOTE
TN-07

by John R. Mick

INTRODUCTION

Many types of equipment such as airborne flight equipment and ground-based, battery operated equipment require the lowest possible power for their operation. Often, design engineers choose the slowest possible memories thinking that they are minimizing the power dissipation. In many applications, this does not necessarily represent the lowest power system.

UNDERSTANDING THE TRADEOFF

Most CMOS static RAMs have several different power supply specifications depending on their mode of operation. For example, the operating power supply current (I_{CC}) can be quite high. Many CMOS static RAMs have one or two different standby currents specified. The first of these is the TTL level standby current usually designated as I_{SB}. The second of these is the full CMOS standby power level usually designated as I_{SB1}. These two standby currents are usually considerably lower than the operating power supply current.

DESIGN EXAMPLE

Let us suppose that we have a microprocessor system that has a required bus cycle of 200ns. For the purpose of this design example, let us assume that if we select a slow static RAM (such as 120ns), we can design the system so that the chip select is low for 120ns and high for 80ns. This gives a total microprocessor bus cycle time of 200ns. The result of such a system is that, while the chip select is low, the operating power supply current is drawn. For the purpose of this example, let us assume that 90 milliamps is required. Similarly, while the chip select is high, the full CMOS standby power supply current is drawn and, in this example, let us assume it is 0.9 milliamps. The net result is that the average power dissipation to operate the RAM in this speed range is 275 milliwatts. This is shown in Figure 1.

A second design possibility exists in which we could select a very fast static RAM (such as 35ns). Let us assume the IDT7198L35 for the purpose of this example. In this design, a 200ns bus cycle is again required for the design, but now we will operate the RAM as fast as possible. This will result in the chip select being low for a total of 35ns and high for a total of 165ns. The net result is that, for the IDT7198L35, while the chip select is low, we draw an active power of 110 milliamps. While the chip select is high, we draw a CMOS standby power of 0.9 milliamps. This results in a total average power for the system of 100 milliwatts.

SUMMARY

As can be seen from the above example, and referring to Figure 1, utilizing the fastest static RAMs can result in the lowest overall operating power for this system. This takes advantage of the much higher speed of the RAM and the resulting low duty cycle for which we draw the high amount of power. Thus, we can see that one should not just choose a slow RAM for a low-power system, but rather the designer should consider the fastest possible static RAMs and utilize the low operating duty cycle when implementing the system.

FAST RAMs = LOWEST POWER

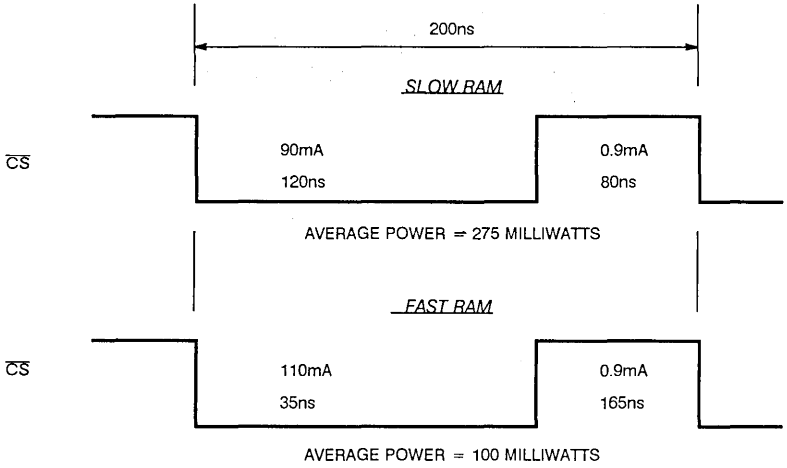

Figure 1. Active Chip Select Time for 200ns Cycle

Integrated Device Technology, Inc.

CACHE-TAG RAM TIMING FOR THE 68020 USING THE IDT7174

TECHNICAL NOTE TN-11

by SRAM Applications

A cache memory for the 68020 can be made using IDT7174 cache-tag RAMs in combination with cache-data RAMs such as the IDT7164. The access time requirements for the cache-tag and cache-data RAMs can be derived from the 68020 timing specifications.

At first glance, it would appear that the cache-tag RAMs must be faster than the cache-data RAMs because they must decide whether to use cache data or main memory data and this decision must be made at the beginning of the memory cycle. This would be true if only the DSACK inputs were used for the cache, but slower tags can be used if the design takes advantage of the 68020's retry cycle, by asserting both the BERR and HALT inputs (see Application Note 79). The critical path for the cache-tag RAMs is from the address outputs, through the cache-tag RAMs to their match outputs and through the drivers to the DSACK inputs (or the BERR and HALT inputs) to the 68020. This is shown in the 68020 Cache Interface drawing below.

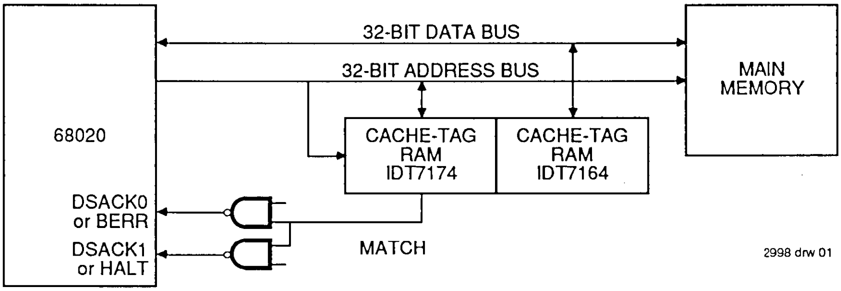

Figure 1. 68020 Cache Interface

The cache-tag and cache-data RAM access time calculations and timing diagram are shown below for a 68020 running with a 20MHz through 33MHz clock for both DSACK and BERR/HALT architectures.

Cache-Tag RAM Access Time Requirement				
Spec. No.	Characteristic	Value (ns) 20MHz	25Mhz	33Mhz
DSACK Architecture				
—	3 Half-Clock Periods	75	60	45
6	Clock High to Address	-25	-25	-2
—	Driver Delay	-5	-5	-5
47A	DSACK Input Set-up Time	-5	-5	-5
	Tag RAM Access Time	40	25	14
BERR/HALT Architecture				
—	5 Half-Clock Periods	125	100	75
6	Clock High to Address	-25	-25	-21
—	Driver Delay	-5	-5	-5
27A	BERR/HALT Valid to Clock Low	-15	-10	-5
	Tag RAM Access Time	80	60	44

Cache-Data RAM Access Time Requirement				
Spec. No.	Characteristic	Value (ns) 20MHz	25Mhz	33Mhz
DSACK Architecture				
—	5 Half-Clock Periods	125	100	75
6	Clock High to Address	-25	-25	-21
27	DATAIN Valid to Clock Low	-5	-5	-5
	Data RAM Access Time	95	70	49

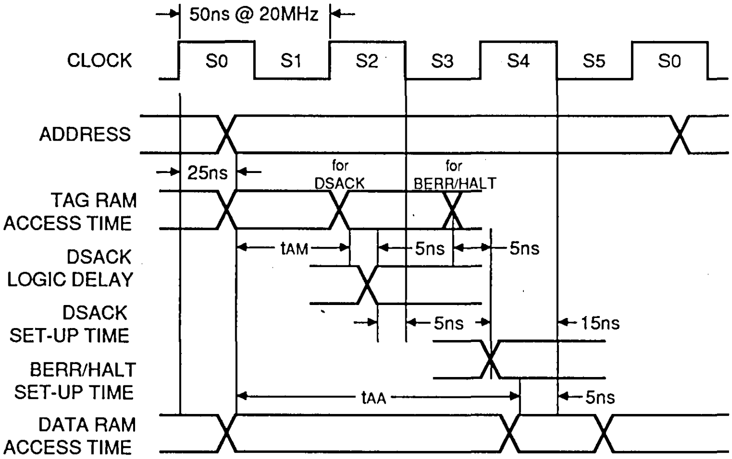

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Figure 2. 68020 Cache Timing Diagram

Cache-tag and cache-data RAM access time requirements for various 68020 clock rates are shown in the table below. Note that a 5ns delay for the drive gates is assumed.

Speed (MHz)	Clock Period (ns)	Tag Access Time (ns)		Data Access Time (ns)
		DSACK	BERR/HALT	
33	30	14	44	49
25	40	25	60	70
20	50	40	80	95
16	62.5	53	95	121
12.5	80	65	130	150

Integrated Device Technology, Inc.

CACHE TIMING FOR THE 80386

TECHNICAL NOTE
TN-13

by SRAM Applications

A cache memory for the 80386 can be made using IDT7174 cache-tag RAMs in combination with cache-data RAMs such as the IDT7164. The access time requirements for the cache-tag and cache-data RAMs can be derived from the 80386 timing specifications.

The cache-tag RAMs must be fast because they must decide whether to use cache data or main memory data and this decision must be made at the beginning of the memory cycle. The critical path for the cache-tag RAMs is from the address outputs, through the cache-tag RAMs to their match outputs and through the READY driver to the READY input to the 80386. This is shown in the 80386 Cache Interface drawing below.

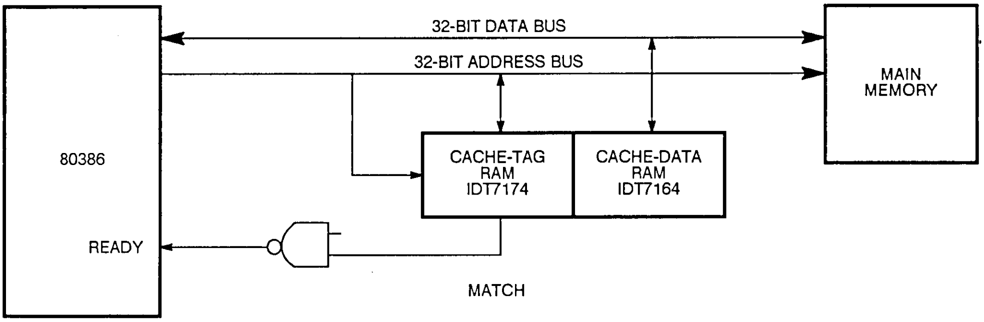

Figure 1. 80386 Cache Interface

The cache-tag and data RAM access time calculations and timing diagram are shown below for a 80386 running with a 16MHz clock.

Cache-Tag RAM Access Time Requirement			**Cache-Data RAM Access Time Requirement**		
Spec. No.	**Characteristic**	**Value @ 16 MHz (ns)**	**Spec. No.**	**Characteristic**	**Value @ 16 MHz (ns)**
-	2 Clock Periods	125	-	2 Clock Periods	125
T6	Clock High to Address	-40	T6	Clock High to Address	-40
-	READY Driver Delay	-5	T21	DATA_{IN} Valid to Clock Low	-10
T19	READY Input Set-up Time	-20			
	Tag RAM Access Time	60		Data RAM Access Time	75

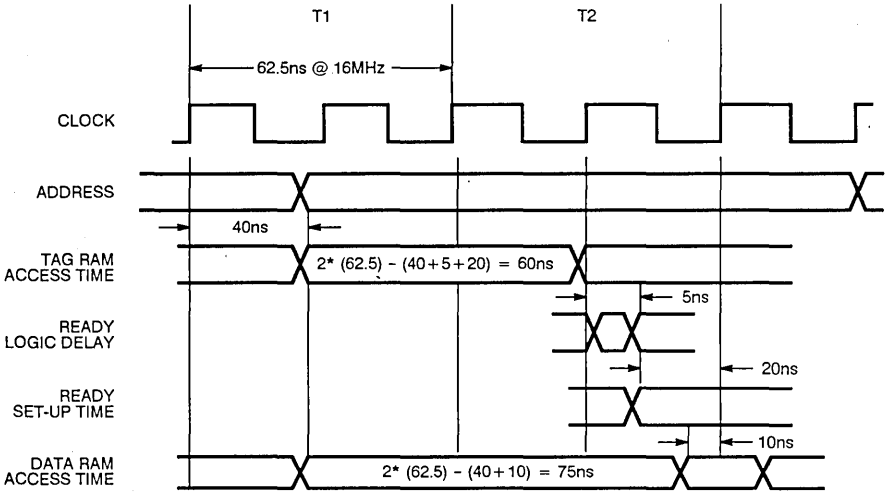

Figure 2. 80386 Cache Timing Diagram

Cache-tag and cache-data RAM access time requirements for various 80386 clock rates are shown in the table below. Note that a 5ns delay for the READY drive gate is assumed.

80386 Speed (MHz)	Clock Period (ns)	Tag Access Time (ns)	Data Access Time (ns)
20	50.0	52	58
16	62.5	60	75
12	83.3	95	110

Figure 3. 80386 Cache Memory Access Time Requirements vs Clock Rate

Integrated Device Technology, Inc.

PROGRAMMABLE LENGTH SHIFT REGISTERS USING RAMs AND COUNTERS

TECHNICAL NOTE TN-16

by SRAM Applications

Programmable length shift registers can be made using counters and RAMs. These shift registers can be quite long and reprogrammed during use if desired.

A block diagram of a programmable length shift register made from a RAM and counter is shown in Figure 1. This shift register can be from one to 16,384 words long by four bits per word. It can shift at clock cycle times down to 38ns for 15ns RAMs and FCT161A counters.

The RAM and counter configuration provide a circular buffer. The counter size (in total counts) sets the size of the circular buffer. The counter points to the next location for storing data in this buffer. Before storing new data at this location, the old data is read out and latched. As the counter walks around the ring, the old data is continuously read out and new data written in.

The programmable length is provided by the counter. In the case shown, the counter counts from zero and increments up to the compare value which is the shift register effective length minus 1. The 521 comparator output is active at this maximum count and causes the counter to be parallel loaded with zero, effectively resetting the counter.

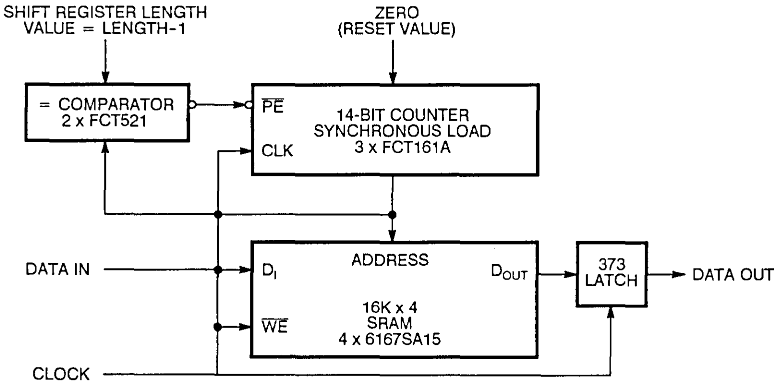

Figure 1. Variable Length RAM Based Shift Register Block Diagram

Timing for this shift register is shown in Figure 2. Data is read out from the RAM during the first half of the clock cycle and latched in the 373 during the second half. Data is written into the RAM in the second half, and the counter is incremented at the end of the cycle Clock cycle time calculations are shown in Table 1.

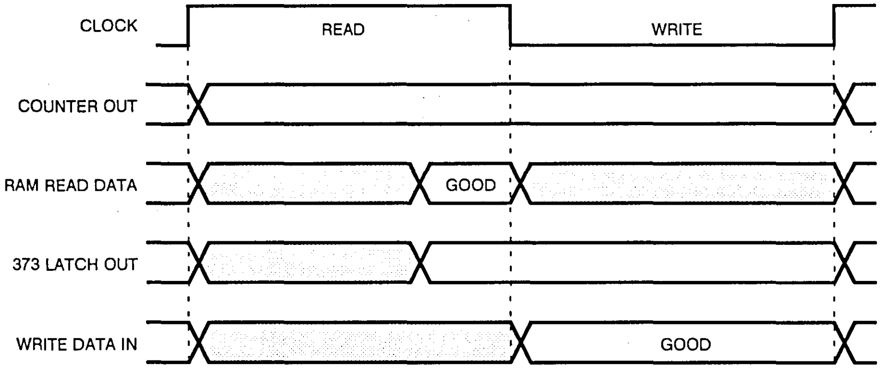

Figure 2. Variable Length RAM Based Shift Register Timing Diagram

Table 1. Clock Cycle Time Calculations

Counter settling time: FCT161A	7.2ns
RAM access time: IDT6167SA15	15.0
Latch setup time: FCT373A	2.0
Clock high time, minimum	24.2ns
Clock low time = RAM write time: IDT6167SA15	13.0
Total	37.2ns

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