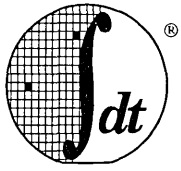
1992/93 DATA BOOK

HIGH-PERFORMANCE STATIC RAMS

INCLUDES 3.3V AND BiCMOS SRAMS

Integrated Device Technology, Inc.



Integrated Device Technology, Inc.

1992/93
HIGH-PERFORMANCE SRAM
DATA BOOK

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CONTENTS OVERVIEW

For ease of use for our customers, Integrated Device Technology provides four separate data books: High-Performance Logic, Specialized Memories and Modules, RISC and RISC SubSystems, and High-Performance Static RAM.

IDT's 1992/93 High-Performance SRAM Data Book is comprised of both new product data sheets and revised data sheets on existing products. The new products include high-speed, high-density BiCMOS devices, Specialty SRAM products, and true 3.3V high-performance SRAMs. The existing product revisions upgrade and correct the existing specification, to more accurately reflect device improvements that have been made over time. Also included is a current packaging section for the products included in this book.

The 1992/93 SRAM Data Book's Table of Contents is a listing of the products contained in this data book only (in the past, we have also included products that appeared in other IDT data books). The numbering scheme for the book is consistent with the 1990–91 data books. The number at the bottom center of the page denotes the section number and the sequence of the data sheet within that section, (i.e., 5.5 would be the fifth data sheet in the fifth section). The number in the lower right-hand corner is the page number for that particular data sheet.

The data sheets are organized in six sections (16K, 64K, 256/288K, 1M, 3.3V, and Specialty SRAMs). Each section is then ordered by total number of bits (low to high), device word width (narrow to wide), and performance (slow to fast).

Integrated Device Technology, Inc. is a recognized leader in high-speed CMOS and BiCMOS technology and produces a broad line of products. This enables us to provide complete CMOS and BiCMOS solutions to designers of high-performance digital systems. Not only do our product lines include industry standard devices, they also feature products with faster speeds, lower power, and package and/or architectural benefits that allow designers to significantly improve system performance.

To find ordering information: Ordering Information for all products in this book appears in Section 1, along with the Product Selector Matrix, Package Marking Description, and Functional Cross Reference. Reference data on our Technology Capabilities, Quality Commitments, and Package Diagram Outlines is included in Sections 2, 3, and 4 respectively.

To find product data: Begin with the Table of Contents (page 1.2), Product Selector Matrix (page 1.6), or with the Numeric Table of Contents (page 1.3). The Product Selector Matrix will help you identify the device you are interested in, while the Table of Contents indexes will direct you to the page on which the complete technical data sheet can be found. Data sheets may be of the following type:

ADVANCE INFORMATION—contain initial descriptions (subject to change) for products that are in development, including features, block diagrams, and target specifications.

PRELIMINARY—contain descriptions for products soon to be or recently, released to production, including features, pinouts, and block diagrams. Timing data are based on simulation or initial characterization and are subject to change upon full characterization.

FINAL—contain minimum and maximum limits specified over the complete voltage supply and temperature range for full production devices.

New products, product performance enhancements, additional package types, and new product families are being introduced frequently. Please contact your local IDT sales representative to determine the latest device specifications, package types, and product availability.

ABOUT THE COVER

The cover features an IDT71B024 SRAM wafer at approximately 1.4x magnification in the background, and a sampling of IDT SRAMs in space-saving surface-mount packaging from across our product portfolio. The IDT71B024 is a 15ns 1-megabit SRAM which is setting the performance standard for evolutionary pinout 128K x 8 SRAMs, demonstrating the advantage offered by IDT's leading-edge technology. The SOJ-packaged parts represent the wide range of industry-leading SRAM products offered by IDT, including high-performance BiCMOS SRAMs, specialty SRAMs, and the industry's first true 3.3V high-performance SRAM, the IDT713256.

LIFE SUPPORT POLICY

Integrated Device Technology's products are not authorized for use as critical components in life support devices or systems unless a specific written agreement pertaining to such intended use is executed between the manufacturer and an officer of IDT.

1. **Life support devices or systems are devices or systems which (a) are intended for surgical implant into the body or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.**
2. **A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.**

1992 SRAM DATA BOOK
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1992 SRAM DATA BOOK (Continued)

256/288K SRAM PRODUCTS (Cont'd)

1M SRAM PRODUCTS

3.3V SRAM PRODUCTS

SPECIALTY SRAM PRODUCTS

SRAM MODULES (Please refer to the 1992 Specialized Memories and Modules Data Book)

SRAM MONOLITHICS

CACHE MODULES

IDT SALES OFFICE, REPRESENTATIVE AND DISTRIBUTOR LOCATIONS

NUMERICAL TABLE OF CONTENTS

ORDERING INFORMATION

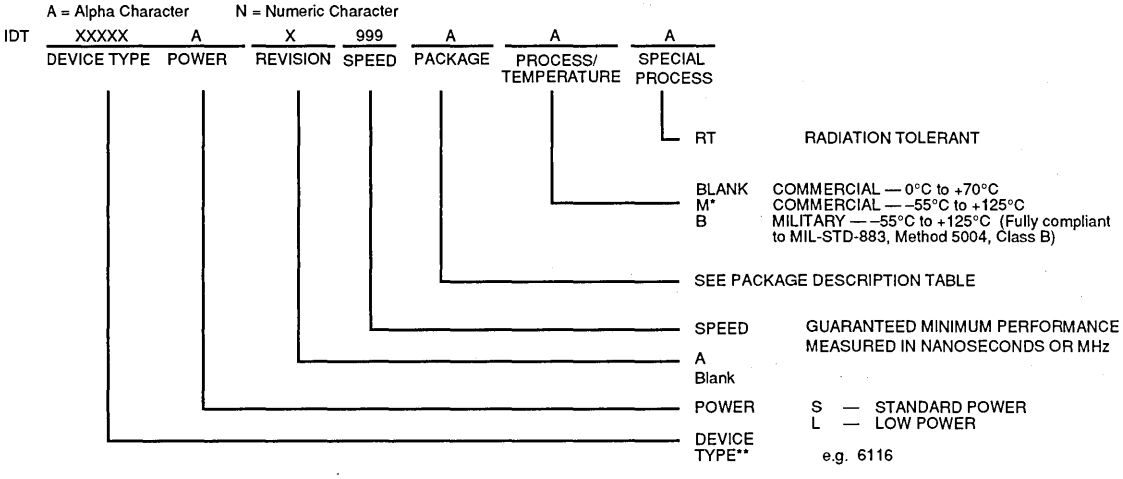
When ordering by TWX or Telex, the following format must be used:

A. Complete Bill To.
B. Complete Ship To.
C. Purchase Order Number.
D. Certificate of Conformance. Y or N.
E. Customer Source Inspection. Y or N.
F. Government Source Inspection. Y or N
G. Government Contract Number and Rating.
H. Requested Routing.
I. IDT Part Number –
   Each item ordered must use the complete part number exactly as listed in the price book.
J. SCD Number — Specification Control Document (Internal Traveller).
K. Customer Part Number/Drawing Number/Revision Level –
   Specify whether part number is for reference only, mark only, or if extended processing to customer specification is required.
L. Customer General Specification Numbers/Other Referenced Drawing Numbers/Revision Levels.
M. Request Date With Exact Quantity.
N. Unit Price.
O. Special Instructions, Including Q.A. Clauses, Special Processing.

Federal Supply Code Number/Cage Number — 61772
Dun & Bradstreet Number — 03-814-2600
Federal Tax I.D. — 94-2669985
TLX# — 887766
FAX# — 408-727-3468

PART NUMBER DESCRIPTION

A = Alpha Character N = Numeric Character



PACKAGE DESCRIPTION TABLE

C	CERAMIC SIDEBRAZE	PF	PLASTIC FLATPACK
D	CERDIP	SO	PLASTIC SMALL OUTLINE IC
F	FLATPACK	TC	SIDEBRAZE THINDIP (300 MIL)
G	PIN GRID ARRAY	TP	PLASTIC THIN DUAL IN-LINE
J	PLASTIC LEADED CHIP CARRIER	QE	CERQUAD GULL WING
L	LEADLESS CHIP CARRIER	XE	CERPACK (F11 CONFIG. ONLY)
P	PLASTIC DIP	XL	FINE-PITCH LCC
Y	SOJ		

*Consult Factory
**For Logic, the "54" series (e.g. IDT54FCT138) — –55°C to +125°C
the "74" series (e.g. IDT74FCT138) — 0°C to +70°C

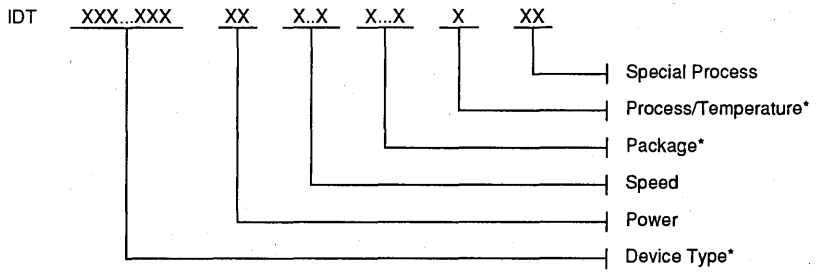
IDT PACKAGE MARKING DESCRIPTION

PART NUMBER DESCRIPTION

IDT's part number identifies the basic product, speed, power, package(s) available, operating temperature and processing grade. Each data sheet has a detailed description, using the part number, for ordering the proper product for the user's application. The part number is comprised of a series of alpha-numeric characters:

1. An "IDT" corporate identifier for Integrated Device Technology, Inc.
2. A basic device part number composed of alpha-numeric characters.
3. A device power identifier, composed of one or two alpha characters, is used to identify the power options. In most cases, the following alpha characters are used:
   "S" or "SA" is used for the standard power product.
   "L" or "LA" is used for lower power than the standard power product.
4. A device speed identifier, when applicable, is either alpha characters, such as "A" or "B", or numbers, such as 20 or 45. The speed units, depending on the product, are in nanoseconds or megahertz.
5. A package identifier, composed of one or two characters. The data sheet should be consulted to determine the packages available and the package identifiers for that particular product.
6. A temperature/process identifier. The product is available in either the commercial or military temperature range, processed to a commercial specification, or the product is available in the military temperature range with full compliance to MIL-STD-883. Many of IDT's products have burn-in included as part of the standard commercial process flow.
7. A special process identifier, composed of alpha characters, is used for products which require radiation enhancement (RE) or radiation tolerance (RT).

Example for Monolithic Devices:



* Field Identifier Applicable To All Products

2507 drw 01

ASSEMBLY LOCATION DESIGNATOR

IDT uses various locations for assembly. These are identified by an alpha character in the last letter of the date code marked on the package. Presently, the assembly location alpha character is as follows:

A = Anam, Korea
I = USA
P = Penang, Malaysia

MIL-STD-883C COMPLIANT DESIGNATOR

IDT ships military products which are compliant to the latest revision of MIL-STD-883C. Such products are identified by a "C" designation on the package. The location of this designator is specified by internal documentation at IDT.

SRAM PRODUCT SELECTOR MATRIX

Size	Org.	Features	Process	Part Number	Power	Speeds		Packages							
								Commercial				Military			
						Commercial	Military	PDIP	SOJ	SOIC	PLCC	SBRZ	CDIP	LCC	CPAK
16K	16K x 1		CMOS	6167	SA/LA	15,20,25,35	20,25,35,45,55,70	20	20	20	—	—	20	20	20
	4K x 4		CMOS	6168	SA/LA	12,15,20,25,35	15,20,25,35,45,55,70	20	20	20	—	—	20	20	20
	4K x 4	OE	CMOS	61970	SA/LA	15,20,25,35	20,25,35,45,55	22	24	—	—	—	22	—	—
	4K x 4	Sep I/O	CMOS	71681	SA/LA	15,20,25,35,45	20,25,35,45,55,70	24	24	24	—	—	24	28	24
	4K x 4	Sep I/O	CMOS	71682	SA/LA	15,20,25,35,45	20,25,35,45,55,70	24	24	24	—	—	24	28	24
	2K x 8		CMOS	6116	SA/LA	15,20,25,35,45	20,25,35,45,55,70,90, 120,150	24	24	24	—	—	24	28/32	24
64K	64K x 1		CMOS	7187	S/L	15,20,25,35	25,35,45,55,70,85	22	24	24	—	—	22	22/28	24
	16K x 4		CMOS	7188	S/L	15,20,25,35	20,25,35,45,55,70,85	22	24	—	—	—	22	—	24
	16K x 4		BiCMOS	71B88	S	8,10,12	N/A	22	24	—	—	—	—	—	—
	16K x 4	OE	CMOS	6198	S/L	15,20,25,35	20,25,35,45,55,70,85	24	24	—	—	—	24	28	—
	16K x 4	OE	BiCMOS	61B98	S	8,10,12	N/A	24	24	—	—	—	—	—	—
	16K x 4	OE, CS2	CMOS	7198	S/L	15,20,25,35	20,25,35,45,55,70,85	24	24	—	—	—	24	28	—
	16K x 4	Sep I/O	CMOS	71981	S/L	15,20,25,35	20,25,35,45,55,70,85	28	28	—	—	—	28	28	—
	16K x 4	Sep I/O	CMOS	71982	S/L	15,20,25,35	20,25,35,45,55,70,85	28	28	—	—	—	28	28	—
	8K x 8		CMOS	7164	S/L	15,20,25,35	20,25,35,45,55,70,85	28	28	28	32	—	28	28/32	28
	8K x 8		BiCMOS	71B64	S	8,10,12	N/A	28	28	—	—	—	—	—	—
256/288K	64K x 4		CMOS	61298	SA	15,17,20	20,25	28	28	—	—	28	—	28	—
	64K x 4		BiCMOS	61B298	S	12,15,20	N/A	28	28	—	—	—	—	—	—
	64K x 4		BiCMOS	61B298	SA	10,12,15	N/A	28	28	—	—	—	—	—	—
	32K x 8		CMOS	71256	S/L	20,25,35	25,35,45,55,70,85	28	28	28	32	28	28	28/32	28
	32K x 8		CMOS	71256	SA	15,17	17,20	28	28	—	—	28	—	32	—
	32K x 8		BiCMOS	71B256	S	12,15,20	N/A	28	28	—	—	—	—	—	—
	32K x 8		BiCMOS	71B256	SA	10,12,15	N/A	28	28	—	—	—	—	—	—
	32K x 9		BiCMOS	71B259	S	10,12,15	N/A	—	32	—	—	—	—	—	—
1M	256K x 4		CMOS	71028	S/L	15,17	20,25	28	28	—	—	—	28	—	—
	256K x 4		BiCMOS	71B028	S	15,17	N/A	28	28	—	—	—	—	—	—
	256K x 4	Center Pwr	BiCMOS	71B128	S	10,12,15	N/A	32	32	—	—	—	—	—	—
	128K x 8		CMOS	71024	S/L	15,17	20,25	32	32	—	—	—	32	32	—
	128K x 8		BiCMOS	71B024	S	15,17	N/A	32	32	—	—	—	—	—	—
	128K x 8	Center Pwr	BiCMOS	71B124	S	10,12,15	N/A	32	32	—	—	—	—	—	—
3.3V RAMS	32K x 8	3.3V	3.3V CMOS	713256	SL	20,25,30	N/A	—	28	—	—	—	—	—	—
	128K x 8	3.3V	3.3V CMOS	713024	SL	20,25	N/A	—	32	—	—	—	—	—	—
Specialty	4K x 4	Tag	CMOS	6178	S	10,12,15,20,25	15,20,25	22	24	—	—	—	22	—	—
	8K x 8	Tag	BiCMOS	71B74	S	8,10,12,15	N/A	28	28	—	—	—	—	—	—
	32K x 8	Notebook	CMOS	71256	SL/L	25,35	NA	28	28	—	—	—	—	—	—
	32K x 9	Burst	CMOS	71589	S	20,25,35	N/A	—	32	—	—	—	—	—	—
	32K x 9	Burst	BiCMOS	71B589	S	10,12,14	N/A	—	32	—	—	—	—	—	—
	16K x 9 x 2	Bicameral	BiCMOS	71B229	S	12,16,22	N/A	—	32	—	—	—	—	—	—

Integrated Device Technology, Inc.

SRAM FUNCTIONAL CROSS REFERENCE GUIDE

Note: This cross reference guide reflects Functional Correlation ONLY. Please refer to the individual data sheet specifications to ensure that the IDT device meets your parametric and packaging requirements.

AT&T	IDT	DESCRIPTION
ATT7C167	IDT6167	16K x 1
ATT7C168	IDT6168	4K x 4
ATT7C170	IDT61970	4K x 4 OE*
ATT7C171	IDT71681	4K x 4 Sep I/O
ATT7C172	IDT71682	4K x 4 Sep I/O
ATT7C116	IDT6116	2K x 8
ATT7C187	IDT7187	64K x 1
ATT7C164	IDT7188	16K x 4
ATT7C164	IDT71B88	16K x 4
ATT7C166	IDT6198	16K x 4 OE*
ATT7C166	IDT61B98	16K x 4 OE*
ATT7C165	IDT7198	16K x 4 OE*/CS2*
ATT7C161	IDT71981	16K x 4 Sep I/O
ATT7C162	IDT71982	16K x 4 Sep I/O
ATT7C185	IDT7164	8K x 8
ATT7C185	IDT71B64	8K x 8
ATT7C195	IDT61298SA	64K x 4 OE*
ATT7C195	IDT61B298SA	64K x 4 OE*
ATT7C199	IDT71256	32K x 8
ATT7C199	IDT71256SA	32K x 8
ATT7C199	IDT71B256SA	32K x 8
ATT7C106	IDT71028	256K x 4 OE*
ATT7C106	IDT71B028	256K x 4 OE*
ATT7C109	IDT71024	128K x 8
ATT7C109	IDT71B024	128K x 8
ATT7C180	IDT6178	4K x 4 Cache Tag
ATT7C174	IDT71B74	8K x 8 Cache Tag
CYPRESS	**IDT**	**DESCRIPTION**
CY7C167	IDT6167	16K x 1
CY7C167A	IDT6167	16K x 1
CY7C168	IDT6168	4K x 4
CY7C168A	IDT6168	4K x 4
CY7C169	IDT6168	4K x 4
CY7C169A	IDT6168	4K x 4
CY7C170	IDT61970	4K x 4 OE*
CY7C170A	IDT61970	4K x 4 OE*
CY7C171	IDT71681	4K x 4 Sep I/O
CY7C171A	IDT71681	4K x 4 Sep I/O
CY7C172	IDT71682	4K x 4 Sep I/O

CYPRESS	IDT	DESCRIPTION
CY7C172A	IDT71682	4K x 4 Sep I/O
CY7C128	IDT6116	2K x 8
CY7C128A	IDT6116	2K x 8
CY7C187	IDT7187	64K x 1
CY7C187A	IDT7187	64K x 1
CY7C164	IDT7188	16K x 4
CY7C164A	IDT7188	16K x 4
CY7B164A	IDT71B88	16K x 4
CY7C164	IDT71B88	16K x 4
CY7C164A	IDT71B88	16K x 4
CY7C166	IDT6198	16K x 4 OE*
CY7C166A	IDT6198	16K x 4 OE*
CY7B166	IDT61B98	16K x 4 OE*
CY7C166	IDT61B98	16K x 4 OE*
CY7C166A	IDT61B98	16K x 4 OE*
CY7C161	IDT71981	16K x 4 Sep I/O
CY7C161A	IDT71981	16K x 4 Sep I/O
CY7C162	IDT71982	16K x 4 Sep I/O
CY7C162A	IDT71982	16K x 4 Sep I/O
CY7C185	IDT7164	8K x 8
CY7C185A	IDT7164	8K x 8
CY7C186	IDT7164	8K x 8
CY7C186A	IDT7164	8K x 8
CY7B185	IDT71B64	8K x 8
CY7C185	IDT71B64	8K x 8
CY7C195	IDT61298SA	64K x 4 OE*
CY7B195	IDT61B298SA	64K x 4 OE*
CY7C198	IDT71256	32K x 8
CY7C199	IDT71256	32K x 8
CY7B198	IDT71256SA	32K x 8
CY7B199	IDT71256SA	32K x 8
CY7B199	IDT71B256SA	32K x 8
CY7C106	IDT71028	256K x 4 OE*
CY7C109	IDT71024	128K x 8
EDI	**IDT**	**DESCRIPTION**
EDI8164	IDT7187	64K x 1
EDI8416	IDT7188	16K x 4
EDI8417	IDT6198	16K x 4 OE*
EDI8808CB	IDT7164	8K x 8
EDI8466CA	IDT61298SA	64K x 4 OE*
EDI8466CB	IDT61298SA	64K x 4 OE*
EDI8466CB	IDT61B298SA	64K x 4 OE*
EDI8833C	IDT71256	32K x 8

EDI	IDT	DESCRIPTION
EDI8833LP	IDT71256	32K x 8
EDI8833P	IDT71256	32K x 8
EDI8834C	IDT71256	32K x 8
EDI8834CA	IDT71256	32K x 8
EDI84256CS	IDT71028	256K x 4 OE*
EDI84256LPS	IDT71028	256K x 4 OE*
EDI84256PS	IDT71028	256K x 4 OE*
EDI88130C	IDT71024	128K x 8
EDI88130LP	IDT71024	128K x 8
EDI88130P	IDT71024	128K x 8
EDI88130CS	IDT71024	128K x 8
EDI88130LPS	IDT71024	128K x 8
EDI88130PS	IDT71024	128K x 8
FUJITSU	**IDT**	**DESCRIPTION**
MB81C67	IDT6167	16K x 1
MB81C68A	IDT6168	4K x 4
MB81C69A	IDT6168	4K x 4
MB81C71	IDT7187	64K x 1
MB81C71A	IDT7187	64K x 1
MB81C74	IDT7188	16K x 4
MB81C75	IDT6198	16K x 4 OE*
MB81C78A	IDT7164	8K x 8
MB82B78	IDT7164	8K x 8
MB82B78	IDT71B64	8K x 8
MB82B85	IDT61298SA	64K x 4 OE*
MB82B85	IDT61B298SA	64K x 4 OE*
MB8298	IDT71256	32K x 8
MB8298	IDT71256SA	32K x 8
MB82B88	IDT71256SA	32K x 8
MB82B89	IDT71B259	32K x 9
MB82B005	IDT71028	256K x 4 OE*
MB82B008	IDT71024	128K x 8
HITACHI	**IDT**	**DESCRIPTION**
HM6267	IDT6167	16K x 1
HM6268	IDT6168	4K x 4
HM6716	IDT6116	2K x 8
HM6287	IDT7187	64K x 1
HM6287H	IDT7187	64K x 1
HM6787	IDT7187	64K x 1
HM6787H	IDT7187	64K x 1
HM6288	IDT7188	16K x 4
HM6788	IDT7188	16K x 4
HM6788H	IDT7188	16K x 4
HM6788HA	IDT71B88	16K x 4
HM6289	IDT6198	16K x 4 OE*
HM6789	IDT6198	16K x 4 OE*
HM6789H	IDT6198	16K x 4 OE*
HM6789HA	IDT61B98	16K x 4 OE*

HITACHI	IDT	DESCRIPTION
HM6709A	IDT61298SA	64K x 4 OE*
HM6709A	IDT61B298SA	64K x 4 OE*
HM6709SH	IDT61B298SA	64K x 4 OE*
HM62832H	IDT71256	32K x 8
HM62832H	IDT71256SA	32K x 8
HM62832UH	IDT71256SA	32K x 8
HM62832UHL	IDT71256SA	32K x 8
HM67832SH	IDT71B256SA	32K x 8
HM62932	IDT71B259	32K x 9
HM624256A	IDT71028	256K x 4 OE*
HM674256UH	IDT71B128	256K x 4 OE* Ctr Pwr/Gnd
HM628127H	IDT71024	128K x 8
HM628127H	IDT71B024	128K x 8
HM678127UH	IDT71B124	128K x 8 Center Pwr/Gnd
INMOS	**IDT**	**DESCRIPTION**
IMS1403	IDT6167	16K x 1
IMS1423	IDT6168	4K x 4
IMS1600	IDT7187	64K x 1
IMS1605	IDT7187	64K x 1
IMS1620	IDT7188	16K x 4
IMS1625	IDT7188	16K x 4
IMS1624	IDT6198	16K x 4 OE*
IMS1629	IDT6198	16K x 4 OE*
IMS1626	IDT71981	16K x 4 Sep I/O
IMS1627	IDT71982	16K x 4 Sep I/O
IMS1630	IDT7164	8K x 8
IMS1635	IDT7164	8K x 8
LOGIC	**IDT**	**DESCRIPTION**
L7C167	IDT6167	16K x 1
L7C168	IDT6168	4K x 4
L7C170	IDT61970	4K x 4 OE*
L7C171	IDT71681	4K x 4 Sep I/O
L7C172	IDT71682	4K x 4 Sep I/O
L6116	IDT6116	2K x 8
L6116L	IDT6116	2K x 8
L7C187	IDT7187	64K x 1
L7C164	IDT7188	16K x 4
L7C164	IDT71B88	16K x 4
L7C166	IDT6198	16K x 4 OE*
L7C166	IDT61B98	16K x 4 OE*
L7C165	IDT7198	16K x 4 OE*/CS2*
L7C161	IDT71981	16K x 4 Sep I/O
L7C162	IDT71982	16K x 4 Sep I/O
L7C185	IDT7164	8K x 8
L7CL185	IDT7164	8K x 8
L7C185	IDT71B64	8K x 8
L7CL185	IDT71B64	8K x 8
L7C195	IDT61298SA	64K x 4 OE*

LOGIC	IDT	DESCRIPTION
L7C195	IDT61B298SA	64K x 4 OE*
L7C199	IDT71256	32K x 8
L7CL199	IDT71256	32K x 8
L7C199	IDT71256SA	32K x 8
L7CL199	IDT71256SA	32K x 8
L7C199	IDT71B256SA	32K x 8
L7CL199	IDT71B256SA	32K x 8
L7C180	IDT6178	4K x 4 Cache Tag
L7C174	IDT71B74	8K x 8 Cache Tag
MICRON	**IDT**	**DESCRIPTION**
MT5C1601	IDT6167	16K x 1
MT5C1604	IDT6168	4K x 4
MT5C1606	IDT71681	4K x 4 Sep I/O
MT5C1607	IDT71682	4K x 4 Sep I/O
MT5C1608	IDT6116	2K x 8
MT5C6401	IDT7187	64K x 1
MT5C6404	IDT7188	16K x 4
MT5C6404	IDT71B88	16K x 4
MT5C6405	IDT6198	16K x 4 OE*
MT5C6405	IDT61B98	16K x 4 OE*
MT5C6406	IDT71981	16K x 4 Sep I/O
MT5C6407	IDT71982	16K x 4 Sep I/O
MT5C6408	IDT7164	8K x 8
MT5C6408	IDT71B64	8K x 8
MT5C2565	IDT61298SA	64K x 4 OE*
MT5C2565	IDT61B298SA	64K x 4 OE*
MT5C2568	IDT71256	32K x 8
MT5C2568	IDT71256SA	32K x 8
MT5C2568	IDT71B256SA	32K x 8
MT5C2889	IDT71B259	32K x 9
MT5C1005	IDT71028	256K x 4 OE*
MT5C1008	IDT71024	128K x 8
MITSUBISHI	**IDT**	**DESCRIPTION**
M5M21C67	IDT6167	16K x 1
M5M21C68	IDT6168	4K x 4
M5M5187A	IDT7187	64K x 1
M5M5187B	IDT7187	64K x 1
M5M5188A	IDT7188	16K x 4
M5M5188B	IDT7188	16K x 4
M5M5189A	IDT6198	16K x 4 OE*
M5M5189B	IDT6198	16K x 4 OE*
M5M5178	IDT7164	8K x 8
M5M5178A	IDT7164	8K x 8
M5M5178B	IDT7164	8K x 8
M5M5259B	IDT61298SA	64K x 4 OE*
M5M5259B	IDT61B298SA	64K x 4 OE*
M5M5278	IDT71256	32K x 8

MITSUBISHI	IDT	DESCRIPTION
M5M5278	IDT71256SA	32K x 8
M5M52B78	IDT71B256SA	32K x 8
M5M52B88	IDT71B256SA	32K x 8
M5M5279	IDT71B259	32K x 9
M5M52B79	IDT71B259	32K x 9
M5M51004	IDT71028	256K x 4 OE*
MOTOROLA	**IDT**	**DESCRIPTION**
MCM6268	IDT6168	4K x 4
MCM6270	IDT61970	4K x 4 OE*
MCM6287C	IDT7187	64K x 1
MCM6288	IDT7188	16K x 4
MCM6288B	IDT7188	16K x 4
MCM6288C	IDT7188	16K x 4
MCM6288	IDT71B88	16K x 4
MCM6288C	IDT71B88	16K x 4
MCM6290	IDT6198	16K x 4 OE*
MCM6290C	IDT6198	16K x 4 OE*
MCM6290	IDT61B98	16K x 4 OE*
MCM6290C	IDT61B98	16K x 4 OE*
MCM6264C	IDT7164	8K x 8
MCM6764A	IDT71B64	8K x 8
MCM6209	IDT61298SA	64K x 4 OE*
MCM6209C	IDT61298SA	64K x 4 OE*
MCM6709	IDT61B298SA	64K x 4 OE*
MCM6709A	IDT61B298SA	64K x 4 OE*
MCM6206	IDT71256	32K x 8
MCM6206C	IDT71256	32K x 8
MCM6206	IDT71256SA	32K x 8
MCM6206C	IDT71256SA	32K x 8
MCM6706	IDT71B256SA	32K x 8
MCM6706A	IDT71B256SA	32K x 8
MCM6205C	IDT71B259	32K x 9
MCM6705A	IDT71B259	32K x 9
MCM6229	IDT71028	256K x 4 OE*
MCM6229A	IDT71028	256K x 4 OE*
MCM6729	IDT71B128	256K x 4 OE* Ctr Pwr/Gnd
MCM6226	IDT71024	128K x 8
MCM6226A	IDT71024	128K x 8
MCM6726	IDT71B124	128K x 8 Center Pwr/Gnd
MCM62V06	IDT713256	32K x 8 - 3.3V
NEC	**IDT**	**DESCRIPTION**
uPD4311	IDT6167	16K x 1
uPD4314C	IDT6168	4K x 4
uPD4361	IDT7187	64K x 1
uPD4362	IDT7188	16K x 4
uPD4362	IDT71B88	16K x 4
uPD4363	IDT6198	16K x 4 OE*

NEC	IDT	DESCRIPTION
uPD4363	IDT61B98	16K x 4 OE*
uPD4368	IDT7164	8K x 8
uPD43253	IDT61298SA	64K x 4 OE*
uPD43253	IDT61B298SA	64K x 4 OE*
uPD43258	IDT71256	32K x 8
uPD43258	IDT71256SA	32K x 8
uPD43259	IDT71B259	32K x 9
uPD431004	IDT71028	256K x 4 OE*
PARADIGM	**IDT**	**DESCRIPTION**
PDM41298	IDT61298SA	64K x 4 OE*
PDM41298	IDT61B298SA	64K x 4 OE*
PDM41256	IDT71256	32K x 8
PDM41256	IDT71256SA	32K x 8
PDM41256	IDT71B256SA	32K x 8
PDM41259	IDT71B259	32K x 9
PDM41028	IDT71028	256K x 4 OE*
PDM41024	IDT71024	128K x 8
PERFORMANCE	**IDT**	**DESCRIPTION**
P4C168	IDT6168	4K x 4
P4C170	IDT61970	4K x 4 OE*
P4C1681	IDT71681	4K x 4 Sep I/O
P4C1682	IDT71682	4K x 4 Sep I/O
P4C116	IDT6116	2K x 8
P4C187	IDT7187	64K x 1
P4C188	IDT7188	16K x 4
P4C198	IDT6198	16K x 4 OE*
P4C198A	IDT7198	16K x 4 OE*/CS2*
P4C1981	IDT71981	16K x 4 Sep I/O
P4C1982	IDT71982	16K x 4 Sep I/O
P4C164	IDT7164	8K x 8
P4C1298	IDT61298SA	64K x 4 OE*
P4C1256	IDT71256	32K x 8
P4C1256	IDT71256SA	32K x 8
QUALITY	**IDT**	**DESCRIPTION**
QS8768	IDT6168	4K x 4
QS8761	IDT71681	4K x 4 Sep I/O
QS8762	IDT71682	4K x 4 Sep I/O
QS8888	IDT7188	16K x 4
QS8888	IDT71B88	16K x 4
QS8886	IDT6198	16K x 4 OE*
QS8886	IDT61B98	16K x 4 OE*
QS8885	IDT7198	16K x 4 OE*/CS2*
QS8881	IDT71981	16K x 4 Sep I/O
QS8882	IDT71982	16K x 4 Sep I/O
QS86446	IDT61298SA	64K x 4 OE*
QS86446	IDT61B298SA	64K x 4 OE*
QS83280	IDT71256	32K x 8

QUALITY	IDT	DESCRIPTION
QS83280	IDT71256SA	32K x 8
QS83280	IDT71B256SA	32K x 8
QS83290	IDT71B259	32K x 9
QS8780	IDT6178	4K x 4 Cache Tag
QS83291	IDT71589	32K x 9 Burst Mode 486
SAMSUNG	**IDT**	**DESCRIPTION**
KM6165	IDT7187	64K x 1
KM6465	IDT7188	16K x 4
KM6465A	IDT7188	16K x 4
KM6465B	IDT7188	16K x 4
KM64B65	IDT71B88	16K x 4
KM64B65A	IDT71B88	16K x 4
KM6466	IDT6198	16K x 4 OE*
KM6466A	IDT6198	16K x 4 OE*
KM6466B	IDT6198	16K x 4 OE*
KM64B66	IDT61B98	16K x 4 OE*
KM64B66A	IDT61B98	16K x 4 OE*
KM64B67	IDT7198	16K x 4 OE*/CS2*
KM6865	IDT7164	8K x 8
KM6865B	IDT7164	8K x 8
KM68B65	IDT71B64	8K x 8
KM68B65A	IDT71B64	8K x 8
KM64258	IDT61298SA	64K x 4 OE*
KM64258B	IDT61298SA	64K x 4 OE*
KM64B258	IDT61B298SA	64K x 4 OE*
KM68257	IDT71256	32K x 8
KM68257B	IDT71256	32K x 8
KM68257B	IDT71256SA	32K x 8
KM68B257	IDT71B256SA	32K x 8
KM69B257	IDT71B259	32K x 9
KM641001	IDT71028	256K x 4 OE*
KM681001	IDT71024	128K x 8
SGS	**IDT**	**DESCRIPTION**
MK41H67	IDT6167	16K x 1
MK41H68	IDT6168	4K x 4
MK41H78	IDT61970	4K x 4 OE*
MK41H87	IDT7187	64K x 1
MK41H80	IDT6178	4K x 4 Cache Tag
MK41S80	IDT6178	4K x 4 Cache Tag
MK48S74	IDT71B74	8K x 8 Cache Tag
SHARP	**IDT**	**DESCRIPTION**
LH5267A	IDT6198	16K x 4 OE*
LH52253	IDT61298SA	64K x 4 OE*
LH52258	IDT71256	32K x 8
LH52258A	IDT71256	32K x 8
LH52258B	IDT71256	32K x 8
LH52258A	IDT71256SA	32K x 8

SHARP	IDT	DESCRIPTION
LH521002	IDT71028	256K x 4 OE*
LH521007	IDT71024	128K x 8
LH521007	IDT71B024	128K x 8
SONY	**IDT**	**DESCRIPTION**
CXK5164	IDT7187	64K x 1
CXK5464A	IDT7188	16K x 4
CXK5466	IDT7188	16K x 4
CXK5465/7	IDT6198	16K x 4 OE*
CXK5863	IDT7164	8K x 8
CXK5863A	IDT7164	8K x 8
CXK58258	IDT71256	32K x 8
CXK58258B	IDT71256	32K x 8
CXK58258A	IDT71256SA	32K x 8
CXK59288	IDT71B259	32K x 9
CXK541000	IDT71028	256K x 4 OE*
CXK581020	IDT71024	128K x 8
CXK581120	IDT71B024	128K x 8
TI	**IDT**	**DESCRIPTION**
TM6716	IDT6116	2K x 8
TM6787	IDT7187	64K x 1
TM6788	IDT7188	16K x 4
TM6789	IDT6198	16K x 4 OE*
TOSHIBA	**IDT**	**DESCRIPTION**
TMM2018	IDT6116	2K x 8
TC5561	IDT7187	64K x 1
TC5562	IDT7187	64K x 1
TC55416	IDT7188	16K x 4
TC55416-H	IDT7188	16K x 4
TC55416-H	IDT71B88	16K x 4
TC55417	IDT6198	16K x 4 OE*
TC55417-H	IDT6198	16K x 4 OE*
TC55B417	IDT61B98	16K x 4 OE*
TC5588	IDT7164	8K x 8
TC55B88	IDT71B64	8K x 8
TC55465	IDT61298SA	64K x 4 OE*
TC55B465	IDT61B298SA	64K x 4 OE*
TC55328	IDT71256	32K x 8
TC55328	IDT71256SA	32K x 8
TC55B328	IDT71256SA	32K x 8
TC55B328	IDT71B256SA	32K x 8
TC55B329	IDT71B259	32K x 9
TC55B4257	IDT71B128	256K x 4 OE* Ctr Pwr/Gnd
TC55B8128	IDT71B124	128K x 8 Center Pwr/Gnd

IDT...LEADING THE CMOS FUTURE

A major revolution is taking place in the semiconductor industry today. A new technology is rapidly displacing older NMOS and bipolar technologies as the workhorse of the '80s and beyond. That technology is high-speed CMOS. Integrated Device Technology, a company totally predicated on and dedicated to implementing high-performance CMOS products, is on the leading edge of this dramatic change.

Beginning with the introduction of the industry's fastest CMOS 2K x 8 static RAM, IDT has grown into a company with multiple divisions producing a wide range of high-speed CMOS and BiCMOS circuits that are, in almost every case, the fastest available. These advanced products are produced with IDT's proprietary technology, a twin-well, dry-etched, stepper-aligned process utilizing progressively smaller dimensions.

From inception, IDT's product strategy has been to apply the advantages of its extremely fast CMOS technology to produce the integrated circuit elements required to implement high-performance digital systems. IDT's goal is to provide the circuits necessary to create systems which are far superior to previous generations in performance, reliability, cost, weight, and size. Many of the company's innovative product designs offer higher levels of integration, advanced architectures, higher density packaging and system enhancement features that are establishing tomorrow's industry standards. The company is committed to providing its customers with an ever-expanding series of these high-speed, lower-power IC solutions to system design needs.

IDT's commitment, however, extends beyond state-of-the-art technology and advanced products to providing the highest level of customer service and satisfaction in the industry. Manufacturing products to exacting quality standards that provide excellent, long-term reliability is given the same level of importance and priority as device performance. IDT is also dedicated to delivering these high-quality advanced products on time. The company would like to be known not only for its technological capabilities, but also for providing its customers with quick, responsive, and courteous service.

IDT's product families are available in both commercial and military grades. As a bonus, commercial customers obtain the benefits of military processing disciplines, established to meet or exceed the stringent criteria of the applicable military specifications.

IDT is a leading U.S. supplier of high-speed CMOS and BiCMOS circuits. The company's high-performance fast SRAM , FCT logic, high-density modules, FIFOs, multi-port memories, BiCMOS ECL I/O memories, RISC SubSystems, and the 32- and 64-bit RISC microprocessor families complement each other to provide high-speed CMOS and BiCMOS solutions for a wide range of applications and systems.

Dedicated to maintaining its leadership position as a state-of-the-art IC manufacturer, IDT will continue to focus on maintaining its technology edge as well as developing a broader range of innovative products. New products and speed enhancements are continuously being added to each of the existing product families, and additional product families are being introduced. Contact your IDT field representative or factory marketing engineer for information on the most current product offerings. If you're building state-of-the-art equipment, IDT wants to help you solve your design problems.

IDT MILITARY AND DESC-SMD PROGRAM

IDT is a leading supplier of military, high-speed CMOS circuits. The company's high-performance Static RAMs, FCT Logic Family, Complex Logic (CLP), FIFOs, Specialty Memories (SMP), ECL I/O BiCMOS Memories, 32-bit RISC Microprocessor, RISC Subsystems and high-density Subsystems Modules product lines complement each other to provide high-speed CMOS solutions to a wide range of military applications and systems. Most of these product lines offer Class B products which are fully compliant to the latest revision of MIL-STD-883, Paragraph 1.2.1. In addition, IDT offers Radiation Tolerant (RT), as well as Radiation Enhanced (RE), products.

IDT has an active program with the Defense Electronic Supply Center (DESC) to list all of IDT's military compliant devices on Standard Military Drawings (SMD). The SMD program allows standardization of militarized products and reduction of the proliferation of non-standard source control drawings. This program will go far toward reducing the need for each defense contractor to make separate specification control drawings for purchased parts. IDT plans to have SMDs for many of its product offerings. Presently, IDT has 88 devices which are listed or pending listing. The devices are from IDT's SRAM, FCT Logic family, Complex Logic (CLP), FIFOs and Specialty Memories (SMP) product families. IDT expects to add another 20 devices to the SMD program in the near future. Users should contact either IDT or DESC for current status of products in the SMD program.

SMD	
SRAM	**IDT**
84036	6116
5962-88740	6116LA
84132	6167
5962-86015	7187
5962-86859	6198/7198/7188
5962-86705	6168
5962-85525	7164
5962-88552	71256L
5962-88662	71256S
5962-88611	71682L
5962-88681	71258S
5962-88545	71258L
5962-89891	7198
5962-89892	6198
5962-89690	6116SA
5962-38294	7164
5962-89692	7188
5962-89712	71982
SMP	**IDT**
5962-86875	7130/7140
5962-87002	7132/7142
5962-88610	7133S/7143S
5962-88665	7133L/7143L
FIFO	**IDT**
5962-87531	7201LA
5962-86846	72404L
5962-88669	7203S
5962-89568	7204L
5962-89536	7202L
5962-89863	7201S
5962-89523	72403L
5962-89666	7200L
5962-89942	72103L
5962-89943	72104L
5962-89567	7203L
5962-90715	7204S

SMD	
LOGIC	**IDT**
5962-87630	54FCT244/A
5962-87629	54FCT245/A
5962-86862	54FCT299/A
5962-87644	54FCT373/A
5962-87628	54FCT374/A
5962-87627	54FCT377/A
5962-87654	54FCT138/A
5962-87655	54FCT240/A
5962-87656	54FCT273/A
5962-89533	54FCT861A/B
5962-89506	54FCT827A/B
5962-88575	54FCT841A/B
5962-88608	54FCT821A/B
5962-88543	54FCT521/A
5962-88640	54FCT161/A
5962-88639	54FCT573/A
5962-88656	54FCT823A/B
5962-88657	54FCT163/A
5962-88674	54FCT825A/B
5962-88661	54FCT863A/B
5962-88736	29FCT520A/B
5962-88775	54FCT646/A
5962-89508	54FCT139/A
5962-89665	54FCT824A/B
5962-88651	54FCT533/A
5962-88652	54FCT182/A
5962-88653	54FCT645A/B
5962-88654	54FCT640A/B
5962-88655	54FCT534/A
5962-89767	54FCT540/A
5962-89766	54FCT541/A
5962-89733	54FCT191/A
5962-89732	54FCT241/A
5962-89652	54FCT399/A
5962-89513	54FCT574/A
5962-89731	54FCT833A/B
5962-88675	54FCT845A/B
5962-89730	54FCT543/A

SMD	
CLP	**IDT**
5962-87708	39C10B & C
5962-88533	49C460A/B/C
5962-88613	39C60A
5962-88643	49C410
5962-86873	7216L
5962-87686	7217L
5962-88733	7210L
5962-89758	54FCT843A/B/C
5962-90669	54FCT193/A
5962-90901	29FCT52A/B/C

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RADIATION HARDENED TECHNOLOGY

IDT manufactures and supplies radiation hardened products for military/aerospace applications. Utilizing special processing and starting materials, IDT's radiation hardened devices survive in hostile radiation environments. In Total Dose, Dose Rate, and environments where single event upset is of concern, IDT products are designed to continue functioning without loss of performance. IDT can supply all its products on these processes. Total Dose radiation testing is performed in-house on an ARACOR X-Ray system. External facilities are utilized for device research on gamma cell, LINAC and other radiation equipment. IDT has an on-going research and development program for improving radiation handling capabilities (See "IDT Radiation Tolerant/Enhanced Products for Radiation Environments" in Section 3) of IDT products/processes.

IDT LEADING EDGE CMOS TECHNOLOGY

HIGH-PERFORMANCE CMOS

From IDT's beginnings in 1980, it has had a belief in and a commitment to CMOS. The company developed a high-performance version of CMOS that allows the design and manufacture of leading-edge components. It incorporates the best characteristics of traditional CMOS, including low power, high noise immunity and wide operating temperature range; it also achieves speed and output drive equal or superior to bipolar Schottky TTL. The last decade has seen development and production of four "generations" of IDT's CMOS technology with process improvements which have reduced IDT's electrical effective (L_{eff}) gate lengths by more than 60 percent from 1.3 microns (millionths of a meter) in 1981 to 0.45 microns in 1990.

	CMOS I	CMOS II A	CMOS II C	CMOS III	CMOS V	CMOS VI
Calendar Year	**1981**	**1983**	**1985**	**1987**	**1989**	**1990**
Drawn Feature Size	2.5μ	1.7μ	1.3μ	1.2μ	1.0μ	0.8μ
Leff	1.3μ	1.1μ	0.9μ	0.8μ	0.6μ	0.45μ
Basic Proces Enhancements	Dual-well, Wet Etch, Projection Aligned	Dry Etch, Stepper	Shrink, Spacer	Silicide, BPSG, BiCMOS I	BiCMOS II	BiCMOS III

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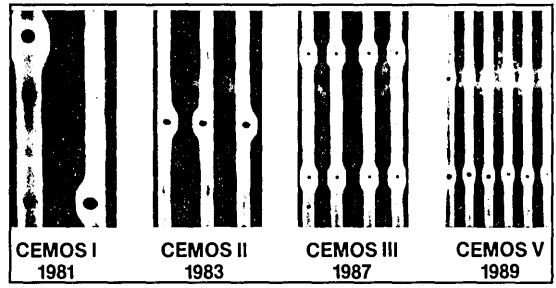
CMOS IV = CMOS III – scaled process optimized for high-speed logic.

Figure 1.

Continual advancement of CMOS technology allows IDT to implement progressively higher levels of integration and achieve increasingly faster speeds maintaining the company's established position as the leader in high-speed CMOS integrated circuits. In addition, the fundamental process technology has been extended to add bipolar elements to the CMOS platform. IDT's BiCMOS process combines the ultra-high speeds of bipolar devices with the lower power and cost of CMOS, allowing us to build even faster components than straight CMOS at a slightly higher cost.



SEM photos (miniaturization) 2514 drw 02

Figure 2. Fifteen-Hundred-Power Magnification Scanning Electron Microscope (SEM) Photos of the Five Generations of IDT's CMOS Technology

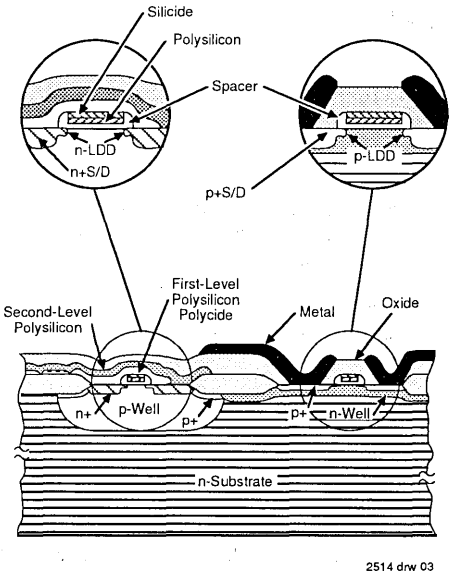


Figure 3. IDT CMOS Device Cross Section

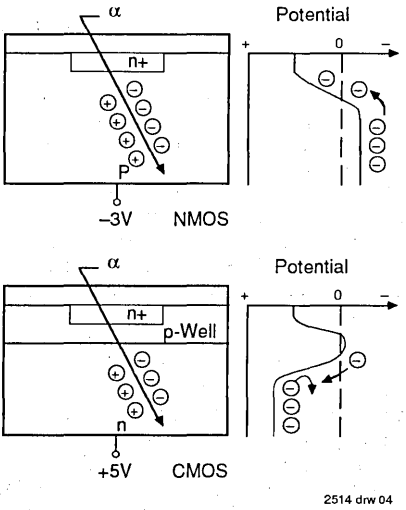


Figure 4. IDT CMOS Built-In High Alpha Particle Immunity

ALPHA PARTICLES

Random alpha particles can cause memory cells to temporarily lose their contents or suffer a "soft error." Traveling with high energy levels, alpha particles penetrate deep into an integrated chip. As they burrow into the silicon, they leave a trail of free electron-hole pairs in their wake.

The cause of alpha particles is well documented and understood in the industry. IDT has considered various techniques to protect the cells from this hazardous occurrence. These techniques include dual-well structures (Figures 3 and 4) and a polymeric compound for die coating. Presently, a polymeric compound is used in many of IDT's SRAMs; however, the specific techniques used may vary and change from one device generation to the next as the industry and IDT improve the alpha particle protection technology.

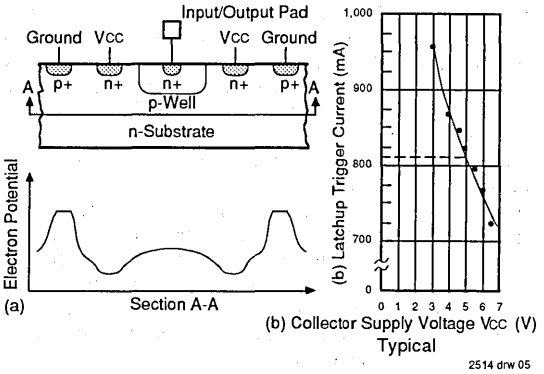


Figure 5. IDT CMOS Latchup Suppression

LATCHUP IMMUNITY

A combination of careful design layout, selective use of guard rings and proprietary techniques have resulted in virtual elimination of latchup problems often associated with older CMOS processes (Figure 5). The use of NPN and N-channel I/O devices eliminates hole injection latchup. Double guard ring structures are utilized on all input and output circuits to absorb injected electrons. These effectively cut off the current paths into the internal circuits to essentially isolate I/O circuits. Compared to older CMOS processes which exhibit latchup characteristics with trigger currents from 10-20mA, IDT products inhibit latchup at trigger currents substantially greater than this.

SURFACE MOUNT TECHNOLOGY AND IDT'S MODULE PRODUCTS

Requirements for circuit area reduction, utilizing the most efficient and compact component placement possible and the needs of production manufacturing for electronics assemblies are the driving forces behind the advancement of circuit-board assembly technologies. These needs are closely associated with the advances being made in surface mount devices (SMD) and surface mount technology (SMT) itself. Yet, there are two major issues with SMT in production manufacturing of electronic assemblies: high capital expenditures and complexity of testing.

The capital expenditure required to convert to efficient production using SMT is still too high for the majority of electronics companies, regardless of the 20–60% increase in the board densities which SMT can bring. Because of this high barrier to entry, we will continue to see a large market segment [large even compared to the exploding SMT market] using traditional through-hole packages (i.e. DIPs, PGAs, etc) and assembly techniques. How can these types of companies take advantage of SMD and SMT? Let someone else, such as IDT, do it for them by investing time and money in SMT and then in return offer through-hole products utilizing SMT processes. Products which fit this description are multi-chip modules, consisting of SMT assembled SMDs on a through-hole type substrate. Modules enable companies to enjoy SMT density advantages and traditional package options without the expensive startup costs required to do SMT in-house.

Although subcontracting this type of work to an assembly house is an alternative, there still is the other issue of testing, an area where many contract assembly operations fall short of IDT's capability and experience. Prerequisites for adequate module testing sophisticated high-performance parametric testers, customized test fixtures, and most importantly the experience to tests today's complex electronic devices. Companies can therefore take advantage of IDT's experience in testing and manufacturing high-performance CMOS multi-chip modules.

At IDT, SMD components are electrically tested, environmentally screened, and performance selected for each IDT module. All modules are 100% tested as if they are a separate functional component and are guaranteed to meet all specified parameters at the module output without the customer having to understand the modules' internal workings.

Other added benefits companies get by using IDT's CMOS module products are:

1) a wide variety of high-performance, through-hole products utilizing SMD packaged components,
2) fast speeds compared with NMOS based products,
3) low power consumption compared with bipolar technologies, and
4) low cost manufacturability compared with GaAs-based products.

IDT has recognized the problems of SMT and began offering CMOS modules as part of its standard product portfolio. IDT modules combine the advantages of:

1) the low power characteristics of IDT's CMOS and BiCMOS products,
2) the density advantages of first class SMD components including those from IDT's components divisions, and
3) experience in system level design, manufacturing, and testing with its own in-house SMT operation.

IDT currently has two divisions (Subsystems and RISC Subsystems) dedicated to the development of module products ranging from simple memory modules to complex VME sized application specific modules to full system-level CPU boards. These modules have surface mount devices assembled on both sides of either a multi-layer glass filled epoxy (FR-4) or a multi-layer co-fired ceramic substrate. Assembled modules come available in industry standard through-hole packages and other space-saving module packages. Industry proven vapor-phase or IR reflow techniques are used to solder the SMDs to the substrate during the assembly process. Because of our affiliation with IDT's experienced semiconductor manufacturing divisions, we thoroughly understand and therefore test all modules to the applicable datasheet specifications and customer requirements.

Thus, IDT is able to offer today's electronic design engineers a unique solution for their "need-more-for-less" problem.modules. These high speed, high performance products offer the density advantages of SMD and SMT, the added benefit of low power CMOS technology, and through-hole packaged electronics without the high cost of doing it in-house.

STATE-OF-THE-ART FACILITIES AND CAPABILITIES

Integrated Device Technology is headquartered in Santa Clara, California—the heart of "Silicon Valley." The company's operations are housed in six facilities totaling over 500,000 square feet. These facilities house all aspects of business from research and development to design, wafer fabrication, assembly, environmental screening, test, and administration. In-house capabilities include scanning electron microscope (SEM) evaluation, particle impact noise detection (PIND), plastic and hermetic packaging, military and commercial testing, burn-in, life test, and a full complement of environmental screening equipment.

The over-200,000-square-foot corporate headquarters campus is composed of three buildings. The largest facility on this site is a 100,000 square foot, two-building complex. The first building, a 60,000-square-foot facility, is dedicated to the Standard Logic and RISC Microprocessor product lines, as well as hermetic and plastic package assembly, logic products' test, burn-in, mark, QA, and a reliability/failure analysis lab.

IDT's Packaging and Assembly Process Development teams are located here. To keep pace with the development of new products and to enhance the IDT philosophy of "innovation," these teams have ultra-modern, integrated and correspondingly sophisticated equipment and environments at their disposal. All manufacturing is completed in dedicated clean room areas (Class 10K minimum), with all preseal operations accomplished under Class 100 laminar flow hoods.

Development of assembly materials, processes and equipment is accomplished under a fully operational production environment to ensure reliability and repeatable product. The Hermetic Manufacturing and Process Development team is currently producing custom products to the strict requirements of MIL-STD-883. The fully automated plastic facility is currently producing high volumes of USA-manufactured product, while developing state-of-the-art surface-mount technology patterned after MIL-STD-883.

The second building of the complex houses sales, marketing, finance, MIS, and Northwest Area Sales.

The RISC Subsystems Division is located across from the two-building complex in a 50,000-square-foot facility. Also located at this facility are Quality Assurance and wafer fabrication services. Administrative services, Human Resources, International Planning, Shipping and Receiving departments are also housed in this facility.

IDT's largest and newest facility, opened in 1990 in San Jose, California, is a multi-purpose 150,000-square-foot, ultra-modern technology development center. This facility houses a 25,000 square foot, combined Class 1 (a maximum of one particle-per-cubic-foot of 0.2 micron or larger), sub-half-micron R&D fabrication facility and a wafer fabrication area. This fab supports both production volumes of IDT products, including some next-generation SRAMs, and the R&D efforts of the technology development staff. Technology development efforts targeted for the center include advanced silicon processing and wafer fabrication techniques. A test area to support both production and research is located on-site. The building is also the home of the FIFO, ECL, and Subsystems product lines.

IDT's second largest facility is located in Salinas, California, about an hour south of Santa Clara. This 95,000-square-foot facility, located on 14 acres, houses the Static RAM Division and Specialty Memory product line. Constructed in 1985, this facility contains an ultra-modern 25,000-square-foot high-volume wafer fabrication area measured at Class 2-to-3 (a maximum of 2 to 3 particles-per-cubic-foot of 0.2 micron or larger) clean room conditions. Careful design and construction of this fabrication area created a clean room environment far beyond the 1985 average for U.S. fab areas. This made possible the production of large volumes of high-density submicron geometry, fast static RAMs. This facility also houses shipping areas for IDT's leadership family of CMOS and BiCMOS static RAMs. This site can expand to accommodate a 250,000-square-foot complex.

To extend our capabilities while maintaining strict control of our processes, IDT has an operational Assembly and Test facility located in Penang, Malaysia. This facility assembles product to U.S. standards, with all assemblies done under laminar flow conditions (Class 100) until the silicon is encased in its final packaging. All products in this facility are manufactured to the quality control requirements of MIL-STD-883.

All of IDT's facilities are aimed at increasing our manufacturing productivity to supply ever-larger volumes of high-performance, cost-effective, leadership CMOS products.

SUPERIOR QUALITY AND RELIABILITY

Maintaining the highest standards of quality in the industry on all products is the basis of Integrated Device Technology's manufacturing systems and procedures. From inception, quality and reliability are built into all of IDT's products. Quality is "designed in" at every stage of manufacturing – as opposed to being "tested-in" later – in order to ensure impeccable performance.

Dedicated commitment to fine workmanship, along with development of rigid controls throughout wafer fab, device assembly and electrical test, create inherently reliable products. Incoming materials are subjected to careful inspections. Quality monitors, or inspections, are performed throughout the manufacturing flow.

IDT military grade monolithic hermetic products are designed to meet or exceed the demanding Class B reliability levels of MIL-STD-883 and MIL-M-38510, as defined by Paragraph 1.2.1 of MIL-STD-883.

Product flow and test procedures for all monolithic hermetic military grade products are in accordance with the latest revision and notice of MIL-STD-883. State-of-the-art production techniques and computer-based test procedures are coupled with tight controls and inspections to ensure that products meet the requirements for 100% screening. Routine quality conformance lot testing is performed as defined in MIL-STD-883, Methods 5004 and 5005.

For IDT module products, screening of the fully assembled substrates is performed, in addition to the monolithic level screening, to assure package integrity and mechanical reliability. All modules receive 100% electrical tests (DC, functional and dynamic switching) to ensure compliance with the "subsystem" specifications.

By maintaining these high standards and rigid controls throughout every step of the manufacturing process, IDT ensures that commercial, industrial and military grade products consistently meet customer requirements for quality, reliability and performance.

SPECIAL PROGRAMS

Class S. IDT also has all manufacturing, screening and test capabilities in-house (except X-ray and some Group D tests) to perform complete Class S processing per MIL-STD-883 on all IDT products and has supplied Class S products on several programs.

Radiation Hardened. IDT has developed and supplied several levels of radiation hardened products for military/aerospace applications to perform at various levels of dose rate, total dose, single event upset (SEU), upset and latchup. IDT products maintain nearly their same high-performance levels built to these special process requirements. The company has in-house radiation testing capability used both in process development and testing of deliverable product. IDT also has a separate group within the company dedicated to supplying products for radiation hardened applications and to continue research and development of process and products to further improve radiation hardening capabilities.

QSP–QUALITY, SERVICE AND PERFORMANCE

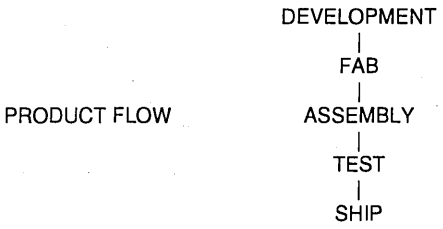
Quality from the beginning, is the foundation for IDT's commitment to supply consistently high-quality products to our customers. IDT's quality commitment is embodied in its all pervasive Continuous Quality Improvement (CQI) process. Everyone who influences the quality of the product–from the designer to the shipping clerk–is committed to constantly improving the quality of their actions.

IDT QUALITY PHILOSOPHY

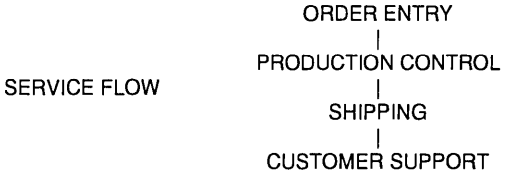
"To make quantitative constant improvement in the quality of our actions that result in the supply of leadership products in conformance to the requirements of our customers."

IDT's ASSURANCE STRATEGY FOR CQI

Measurable standards are essential to the success of CQI. All the processes contributing to the final quality of the product need to be monitored, measured and improved upon through the use of statistical tools.



Our customers receive the benefit of our optimized systems. Installed to enhance quality and reliability, these systems provide accurate and timely reporting on the effectiveness of manufacturing controls and the reliability and quality performance of IDT products and services.



These systems and controls concentrate on CQI by focusing on the following key elements:

Statistical Techniques
Using statistical techniques, including Statistical Process Control (SPC) to determine whether the product/ processes are under control.

Standardization
Implementing policies, procedures and measurement techniques that are common across different operational areas.

Documentation
Documenting and training in policies, procedures, measurement techniques and updating through characterization/ capability studies.

Productivity Improvement
Using constant improvement teams made up from employees at all levels of the organization.

Leadership
Focusing on quality as a key business parameter and strategic strength.

Total Employee Participation
Incorporating the CQI process into the IDT Corporate Culture.

Customer Service
Supporting the customer, as a partner, through performance review and pro-active problem solving.

People Excellence
Committing to growing, motivating and retaining people through training, goal setting, performance measurement and review.

PRODUCT FLOW

Product quality starts here. IDT has mechanisms and procedures in place that monitor and control the quality of our development activities. From the calibration of design capture libraries through process technology and product characterization that establish whether the performance, ratings and reliability criteria have been met. This includes failure analysis of parts that will improve the prototype product.

At the pre-production stage once again in-house qualification tests assure the quality and reliability of the product. All specifications and manufacturing flows are established and personnel trained before the product is placed into production.

Manufacturing

To accomplish CQI during the manufacturing stage, control items are determined for major manufacturing conditions. Data is gathered and statistical techniques are used to control specific manufacturing processes that affect the quality of the product.

In-process and final inspections are fed back to earlier processes to improve product quality. All product is burned-in (where applicable) before 100% inspection of electrical characteristics takes place.

Products which pass final inspection are then subject to Quality Assurance and Reliability Tests. This data is used to improve manufacturing processes and provide reliability predictions of field applications.

Inventory and Shipping

Controls in shipping focus on ensuring parts are identified and packaged correctly. Care is also taken to see that the correct paperwork is present and the product being shipped was processed correctly.

SERVICE FLOW

Quality not only applies to the product but to the quality-of-service we give our customers. Service is also constantly monitored for improvement.

Order Procedures

Checks are made at the order entry stage to ensure the correct processing of the Customer's product. After verification and data entry the Acknowledgements (sent to Customers) are again checked to ensure details are correct. As part of the CQI process, the results of these verifications are analyzed using statistical techniques and corrective actions are taken.

Production Control

Production Control (P.C.) is responsible for the flow and logistics of material as it moves through the manufacturing processes. The quality of the actions taken by P.C. greatly influences the quality of service the customer receives. Because many of our customers have implemented Just-in-Time (JIT) manufacturing practices, IDT as a supplier has adopted these same disciplines. As a result, employees receive extensive training and the performance level of key actions are kept under constant review. These key actions include:

Quotation response and accuracy.
Scheduling response and accuracy.
Response and accuracy of Expedites.
Inventory, management, and effectiveness.
On-time delivery.

Customer Support

IDT has a worldwide network of sales offices and Technical Development Centers. These provide local customer support on business transactions, and in addition, support customers on applications information, technical services, benchmarking of hardware solutions, and demonstration of various Development Workstations.

The key to CQI is the timely resolution of defects and implementation of the corrective actions. This is no more important than when product failures are found by a customer. When failures are found at the customer's incoming inspection, in the production line, or the field application, the Division Quality Assurance group is the focal point for the investigation of the cause of failure and implementation of the corrective action. IDT constantly improves the level of support we give our customers by monitoring the response time to customers who have detected a product failure. Providing the customer with an analysis of the failure, including corrective actions and the statistical analysis of defects, brings CQI full circle–full support of our customers and their designs with high-quality products.

SUMMARY

In 1990, IDT made the commitment to *"Leadership through Quality, Service, and Performance Products"*.

We believe by following this credo IDT and our customers will be successful in the coming decade. With the implementation of the CQI strategy within the company, we will satisfy our goal...

"Leadership through Quality, Service and Performance Products".

IDT QUALITY CONFORMANCE PROGRAM

A COMMITMENT TO QUALITY

Integrated Device Technology's monolithic assembly products are designed, manufactured and tested in accordance with the strict controls and procedures required by Military Standards. The documentation, design and manufacturing criteria of the Quality and Reliability Assurance Program were developed and are being maintained to the most current revisions of MIL-38510 as defined by paragraph 1.2.1 of MIL-STD-883 and MIL-STD-883 requirements.

Product flow and test procedures for all Class B *monolithic* hermetic Military Grade microcircuits are in full compliance with paragraph 1.2.1 of MIL-STD-883. State-of-the-art production techniques and computer-based test procedures are coupled with stringent controls and inspections to ensure that products meet the requirements for 100% screening and quality conformance tests as defined in MIL-STD-883, Methods 5004 and 5005.

Product flow and test procedures for all *plastic* and *commercial hermetic* products are in accordance with industry practices for producing highly reliable microcircuits to ensure that products meet the IDT requirements for 100% screening and quality conformance tests.

By maintaining these high standards and rigid controls throughout every step of the manufacturing process, IDT ensures that our products consistently meet customer requirements for quality, reliability and performance.

SUMMARY

Monolithic Hermetic Package Processing Flow[1]

Refer to the Monolithic Hermetic Package Processing Flow diagram. All test methods refer to MIL-STD-883 unless otherwise stated.

1. **Wafer Fabrication:** Humidity, temperature and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 100 levels or better.

   Wafers from each wafer fabrication area are subjected to Scanning Electron Microscope analysis on a periodic basis.

2. **Die Visual Inspection:** Wafers are cut and separated and the individual die are 100% visually inspected to strict IDT-defined internal criteria.

3. **Die Shear Monitor:** To ensure die attach integrity, product samples are routinely subjected to a shear strength test per Method 2019.

4. **Wire Bond Monitor:** Product samples are routinely subjected to a strength test per Method 2011, Condition D, to ensure the integrity of the lead bond process.

5. **Pre-Cap Visual:** Before the completed package is sealed, 100% of the product is visually inspected to Method 2010, Condition B criteria.

6. **Environmental Conditioning:** 100% of the sealed product is subjected to environmental stress tests. These thermal and mechanical tests are designed to eliminate units with marginal seal, die attach or lead bond integrity.

7. **Hermetic Testing:** 100% of the hermetic packages are subjected to fine and gross leak seal tests to eliminate marginally sealed units or units whose seals may have become defective as a result of environmental conditioning tests.

8. **Pre-Burn-In Electrical Test:** Each product is 100% electrically tested at an ambient temperature of +25°C to IDT data sheet or the customer specification.

9. **Burn-In:** 100% of the Military Grade product is burned-in under dynamic electrical conditions to the time and temperature requirements of Method 1015, Condition D. Except for the time, Commercial Grade product is burned-in as applicable to the same conditions as Military Grade devices.

10. **Post-Burn-In Electrical:** After burn-in, 100% of the Class B Military Grade product is electrically tested to IDT data sheet or customer specifications over the –55°C to +125°C temperature range. Commercial Grade products are sample tested to the applicable temperature extremes.

11. **Mark:** All product is marked with product type and lot code identifiers. MIL-STD-883 compliant Military Grade products are identified with the required compliant code letter.

12. **Quality Conformance Tests:** Samples of the Military Grade product which have been processed to the 100% screening tests of Method 5004 are routinely subjected to the quality conformance requirements of Method 5005.

NOTE:

1. For quality requirements beyond Class B levels such as SEM analysis, X-Ray inspection, Particle Impact Noise Reduction (PIND) test, Class S screening or other customer specified screening flows, please contact your Integrated Device Technology sales representative.

SUMMARY

Monolithic Plastic Package Processing Flow

Refer to the Monolithic Plastic Package Processing Flow diagram. All test methods refer to MIL-STD-883 unless otherwise stated.

1. **Wafer Fabrication:** Humidity, temperature and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 100 levels or better.

   Topside silicon nitride passivation is all applied to all wafers for better moisture barrier characteristics.

   Wafers from each wafer fabrication area are subjected to Scanning Electron Microscope analysis on a periodic basis.

2. **Die Visual Inspection:** Wafers are 100% visually inspected to strict IDT defined internal criteria.

3. **Die Push Test:** To ensure die attach integrity, product samples are routinely subjected to die push tests, patterned after MIL-STD-883, Method 2019.

4. **Wire Bond Monitor:** Product samples are routinely subjected to wire bond pull and ball shear tests to ensure the integrity of the wire bond process, patterned after MIL-STD-883, Method 2011, Condition D.

5. **Pre-Cap Visual:** Before encapsulation, all product lots are visually inspected (using LTPD 5 sampling plan) to criteria patterned after MIL-STD-883, Method 2010, Condition B.

6. **Post Mold Cure:** Plastic encapsulated devices are baked to ensure an optimum polymerization of the epoxy mold compound so as to enhance moisture resistance characteristics.

7. **Pre-Burn-In Electrical:** Each product is 100% electrically tested at an ambient temperature of +25°C to IDT data sheet or the customer specification.

8. **Burn-In:** Except for MSI Logic family devices where it may be obtained as an option, all Commercial Grade plastic package products are burned-in for 16 hours at +125°C minimum (or equivalent), utilizing the same burn-in conditions as the Military Grade product.

9. **Post-Burn-In Electrical:** After burn-in, 100% of the plastic product is electrically tested to IDT data sheet or customer specifications at the maximum temperature extreme. The minimum temperature extreme is tested periodically on an audit basis.

10. **Mark:** All product is marked with product type and lot code identifiers. Products are identified with the assembly and test locations.

11. **Quality Conformance Inspection:** Samples of the plastic product which have been processed to the 100% screening requirements are subjected to the Periodic Quality Conformance Inspection Program. Where indicated, the test methods are patterned after MIL-STD-883 criteria.

TABLE 1

This table defines the device class screening procedures for IDT's high reliability products in conformance with MIL-STD-883C.

Monolithic Hermetic Package Final Processing Flow

	CLASS-S		CLASS-B		CLASS-C [1]	
OPERATION	**TEST METHOD**	**RQMT**	**TEST METHOD**	**RQMT**	**TEST METHOD**	**RQMT**
BURN-IN	1015 Cond. D, 240 Hrs @ 125°C or equivalent	100%	1015 Cond. D, 160 Hrs. @ 125°C min or equivalent	100%	Per applicable device specification	100%
POST BURN-IN ELECTRICAL: Static (DC), Functional and Switching (AC)	Per applicable device specification +25, -55 and 125°C	100%	Per applicable device specification +25, -55 and 125°C	100%	Per applicable [2] device specification	100%
Group A ELECTRICAL: Static (DC), Functional and Switching (AC)	Per applicable device specification and 5005	Sample	Per applicable device specification and 5005	Sample	Per applicable [2] device specification	Sample
MARK/LEAD STRAIGHTENING	IDT Spec	100%	IDT Spec	100%	IDT Spec	100%
FINAL ELECTRICAL TEST	Per applicable device specification +25°C	100%	Per applicable device specification +25°C	100%	Per applicable device specification +25°C	100%
FINAL VISUAL/PACK	IDT Spec	100%	IDT Spec	100%	IDT Spec	100%
QUALITY CONFORMANCE INSPECTION	5005 Group B, C, D.	Sample	5005 Group B,C,D.	Sample	IDT Spec	Sample
QUALITY SHIPPING INSPECTION (Visual/Plant Clearance)	IDT Spec	100%	IDT Spec	100%	IDT Spec	100%

NOTES:
1. Class-C = IDT commercial spec. for hermetic and plastic packages
2. Typical 0°C, 70°C, Extended -55°C +125°C

RADIATION TOLERANT/ENHANCED/HARDENED PRODUCTS FOR RADIATION ENVIRONMENTS

INTRODUCTION

The need for high-performance CMOS integrated circuits in military and space systems is more critical today than ever before. The low power dissipation that is achieved using CMOS technology, along with the high complexity and density levels, makes CMOS the nearly ideal component for all types of applications.

Systems designed for military or space applications are intended for environments where high levels of radiation may be encountered. The implication of a device failure within a military or space system clearly is critical. IDT has made a significant contribution toward providing reliable radiation-tolerant systems by offering integrated circuits with enhanced radiation tolerance. Radiation environments, IDT process enhancements and device tolerance levels achieved are described below.

THE RADIATION ENVIRONMENT

There are four different types of radiation environments that are of concern to builders of military and space systems. These environments and their effects on the device operation, summarized in Figure 1, are as follows:

Total Dose Accumulation refers to the total amount of accumulated gamma rays experienced by the devices in the system, and is measured in RADS (SI) for radiation units experienced at the silicon level. The physical effect of gamma rays on semiconductor devices is to cause threshold shifts (Vt shifts) of both the active transistors as well as the parasitic field transistors. Threshold voltages decrease as total dose is accumulated; at some point, the device will begin to exhibit parametric failures as the input/output and supply currents increase. At higher radiation accumulation levels, functional failures occur. In memory circuits, however, functional failures due to memory cell failure often occur first.

Burst Radiation or Dose Rate refers to the amount of radiation, usually photons or electrons, experienced by the devices in the system due to a pulse event, and is measured in RADS (Si) per second. The effect of a high dose rate or burst of radiation on CMOS integrated circuits is to cause temporary upset of logic states and/or CMOS latch-up. Latch-up can cause permanent damage to the device.

Single Event Upset (SEU) is a transient logic state change caused by high-energy ions, such as energetic cosmic rays, striking the integrated circuits. As the ion passes through the silicon, charge is either created through ionization or direct nuclear collision. If collected by a circuit node, this excess charge can cause a change in logic state of the circuit. Dynamic nodes that are not actively held at a particular logic state (dynamic RAM cells for example) are the most susceptible. These upsets are transient, but can cause system failures known as "soft errors."

Neutron Irradiation will cause structural damage to the silicon lattice which may lead to device leakage and, ultimately, functional failure.

Radiation Category	Primary Particle	Source	Effect
Total Dose	Gamma	Space or Nuclear Event	Permanent
Dose Rate	Photons	Nuclear Event	Temporary Upset of Logic State or Latch-up
SEU	Cosmic Rays	Space	Temporary Upset of Logic State
Neutron	Neutrons	Nuclear Event	Device Leakage Due to Silicon Lattice Damage

2510 drw 01

Figure 1.

DEVICE ENHANCEMENTS

Of the four radiation environments above, IDT has taken considerable data on the first two, Total Dose Accumulation and Dose Rate. IDT has developed a process that significantly improves the radiation tolerance of its devices within these environments. Prevention of SEU failures is usually accomplished by system-level considerations, such as Error Detection and Correction (EDC) circuitry, since the occurrence of SEUs is not particularly dependent on process technology. Through IDT's customer contracts, SEU has been gathered on some devices. Little is yet known about the effects of neutron-induced damage. For more information on SEU testing, contact IDT's Radiation Hardened Product Group.

Enhancements to IDT's standard process are used to create radiation enhanced and tolerant processes. Field and gate oxides are "hardened" to make the device less susceptible to radiation damage by modifying the process architecture to allow lower temperature processing. Device implants and Vts adjustments allow more Vt margin. In addition to process changes, IDT's radiation enhanced process utilizes epitaxial substrate material. The use of epi substrate material provides a lower substrate resistance environment to create latch-up free CMOS structures.

RADIATION HARDNESS CATEGORIES

Radiation Enhanced (RE) or Radiation Tolerant ('RT) versions of IDT products follow IDT's military product data sheets whenever possible (consult factory). IDT's Total Dose Test plan exposes a sample of die on a wafer to a particular Total Dose level via ARACOR X-Ray radiation. This Total Dose Test plan qualifies each 'RE or 'RT wafer to a Total Dose level. Only wafers with sampled die that pass Total Dose level tests are assembled and used for orders (consult factory for more details on Total Dose sample testing). With regard to Total Dose testing, clarifications/exceptions to MIL-STD-883,

Methods 5005 and 1019 are required. Consult factory for more details.

The 'RE and 'RT process enhancements enable IDT to offer integrated circuits with varying grades of radiation tolerance or radiation "hardness".

- Radiation Enhanced process uses Epi wafers and is able to provide devices that can be Total Dose qualified to 10K RADs (Si) or greater by IDT's ARACOR X-Ray Total Dose sample die test plan (Total Dose levels require negotiation, consult factory for more details).
- Radiation Tolerant product uses standard wafer/process material that is qualified to 10K RADs (Si) Total Dose by IDT's ARACOR X-Ray Total Dose sample die test plan.

Integrated Device Technology can provide Radiation Tolerant/Enhanced versions of all product types (some speed grades may not be available as 'RE).

Please contact your IDT sales representative or factory marketing to determine availability and price of any IDT product processed in accordance with one of these levels of radiation hardness.

CONCLUSION

There has been widespread interest within the military and space community in IDT's CMOS product line for its radiation hardness levels, as well as its high-performance and low power dissipation. To serve this growing need for CMOS circuits that must operate in a radiation environment, IDT has created a separate group within the company to concentrate on supplying products for these applications.Continuing research and development of process and products, including the use of in-house radiation testing capability, will allow Integrated Device Technology to offer continuously increasing levels of radiation-tolerant solutions.

THERMAL PERFORMANCE CALCULATIONS FOR IDT'S PACKAGES

Since most of the electrical energy consumed by microelectronic devices eventually appears as heat, poor thermal performance of the device or lack of management of this thermal energy can cause a variety of deleterious effects. This device temperature increase can exhibit itself as one of the key variables in establishing device performance and long term reliability; on the other hand, effective dissipation of internally generated thermal energy can, if properly managed, reduce the deleterious effects and improve component reliability.

A few key benefits of IDT's enhanced CMOS process are: low power dissipation, high speed, increased levels of integration, wider operating temperature ranges and lower quiescent power dissipation. Because the reliability of an integrated circuit is largely dependent on the maximum temperature the device attains during operation, and as the junction stability declines with increases in junction temperature (T_J), it becomes increasingly important to maintain a low (T_J).

CMOS devices stabilize more quickly and at greatly lower temperature than bipolar devices under normal operation. The accelerated aging of an integrated circuit can be expressed as an exponential function of the junction temperature as:

$$t_A = t_o \exp \left[\frac{E_a}{k} \left(\frac{1}{T_O} - \frac{1}{T_J} \right) \right]$$

where

- t_A = lifetime at elevated junction (T_J) temperature
- t_O = normal lifetime at normal junction (T_O) temperature
- E_a = activation energy (ev)
- k = Boltzmann's constant (8.617×10^{-5}ev/k)

i.e. the lifetime of a device could be decreased by a factor of 2 for every 10°C increase temperature.

To minimize the deleterious effects associated with this potential increase, IDT has:

1. Optimized our proprietary low-power CMOS fabrication process to ensure the active junction temperature rise is minimal.
2. Selected only packaging materials that optimize heat dissipation, which encourages a cooler running device.
3. Physically designed all package components to enhance the inherent material properties and to take full advantage of heat transfer and radiation due to case geometries.
4. Tightly controlled the assembly procedures to meet or exceed the stringent criteria of MIL-STD-883 to ensure maximum heat transfer between die and packaging materials.

The following figures graphically illustrate the thermal values of IDT's current package families. Each envelope (shaded area) depicts a typical spread of values due to the influence of a number of factors which include: circuit size, package materials and package geometry. The following range of values are to be used as a comprehensive characterization of the major variables rather than single point of reference.

When calculating junction temperature (T_J), it is necessary to know the thermal resistance of the package (θ_{JA}) as measured in "degree celsius per watt". With the accompanying data, the following equation can be used to establish thermal performance, enhance device reliability and ultimately provide you, the user, with a continuing series of high-speed, low-power CMOS solutions to your system design needs.

4

$$\theta_{JA} = [T_J - T_A]/P$$
$$T_J = T_A + P[\theta_{JA}] = T_A + P[\theta_{JC} + \theta_{CA}]$$

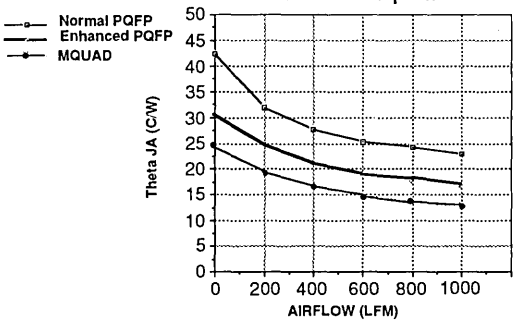
where

$$\theta_{JC} = \frac{T_J - T_C}{P} \qquad \theta_{CA} = \frac{T_C - T_A}{P}$$

- θ = Thermal resistance
- J = Junction
- P = Operational power of device (dissipated)
- T_A = Ambient temperature in degree celsius
- T_J = Temperature of the junction
- T_C = Temperature of case/package
- θ_{CA} = Case to Ambient, thermal resistance—usually a measure of the heat dissipation due to natural or forced convection, radiation and mounting techniques.
- θ_{JC} = Junction to Case, thermal resistance—usually measured with reference to the temperature at a specific point on the package (case) surface. (Dependent on the package material properties and package geometry.)
- θ_{JA} = Junction to Ambient, thermal resistance—usually measured with respect to the temperature of a specified volume of still air. (Dependent on θ_{JC} + θ_{JA} which includes the influence of area and environmental condition.)

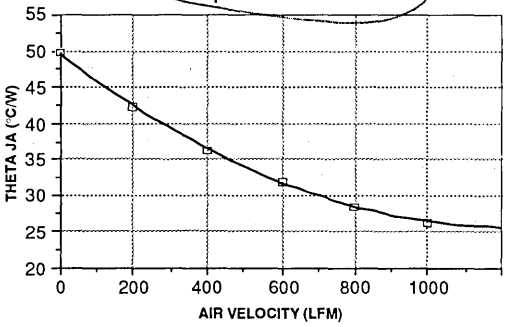
Ref. MIL-STD-883C, Method 1012.1
JEDEC ENG. Bulletin No. 20, January 1975
1986 Semi. Std., Vol. 4, Test Methods G30–86, G32–86.

Theta JA vs. Airflow
160 Pin Quad Flatpacks



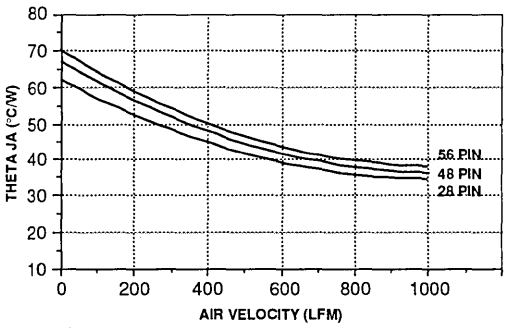
Delco Temp 09 Thermal Die (.250"sq.)
Parts mounted to standard 3" sq. test board.

THETA JA vs. AIR FLOW
32 pin J-bend SOIC

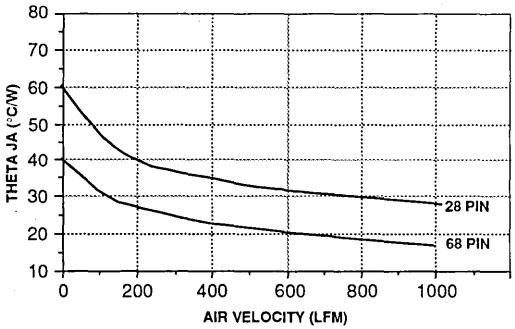


Theta JC was measured to be 17°C/W - Die size (.150"x.250")

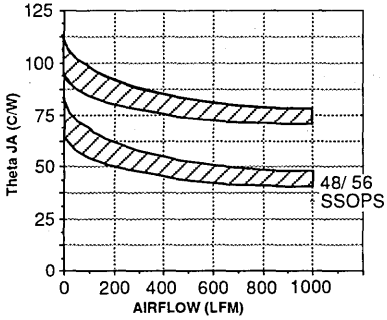
THETA JA vs. AIR FLOW
28/48/56 PIN CERPACKS



THETA JA vs. AIR FLOW
28/68 PIN FLATPACKS

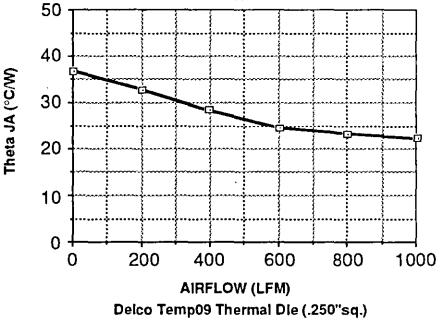


THETA JA vs. AIRFLOW
PLASTIC SSOP PACKAGES



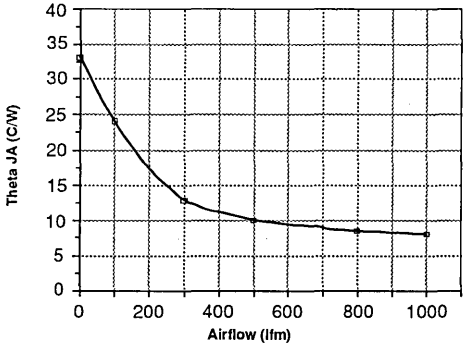
THETA JC : 20/24 PIN = 35-40 °C/W
48/56 PIN = 16-20 °C/W

THETA JA VS. AIRFLOW
84 PLCC



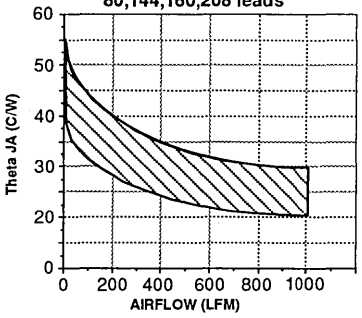
Delco Temp09 Thermal Die (.250"sq.)

Theta JA vs. Airflow
84 pin PGA - Cavity Down w/CuW heatsink



Measurements were done using Temp09 Delco Thermal Die (.250sq.)

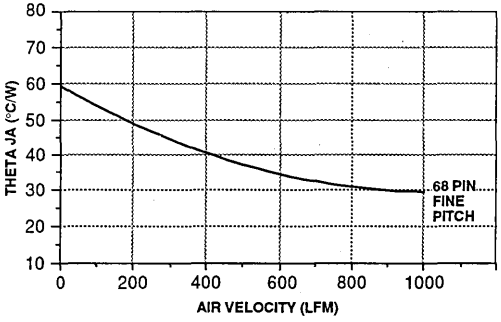
Theta JA vs. Airflow
Plastic Quad Flatpacks
80,144,160,208 leads



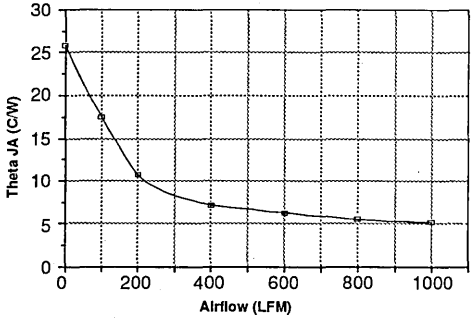
THETA JC : 15-25 °C/W

4

THETA JA vs. AIR FLOW
68 FINE PITCH FLATPACK

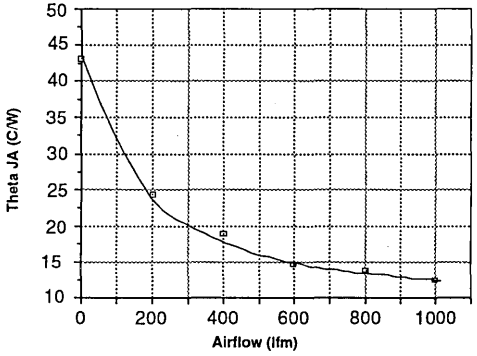


THETA JA vs. AIRFLOW
144 pin PGA - Cavity Down w/ CuW heatsink



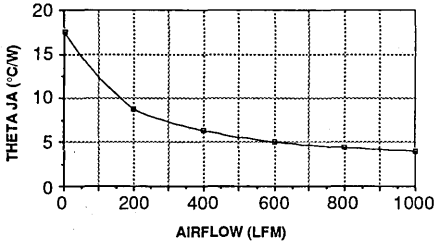
Measurements done with Delco Temp09 Thermal Die (.250"sq.)

Theta JA vs. AIRFLOW
68 pin PGA - Cavity UP



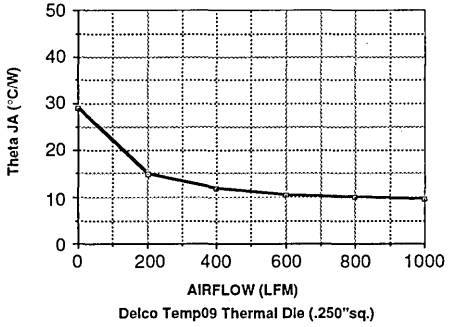
Measurements were done using Temp09 Delco Thermal Die (.250sq.)

THETA JA vs. AIRFLOW
179 PIN PGA - R4000 PACKAGE
INTEGRAL CuW HEATSINK - NO FIN ATTACHED



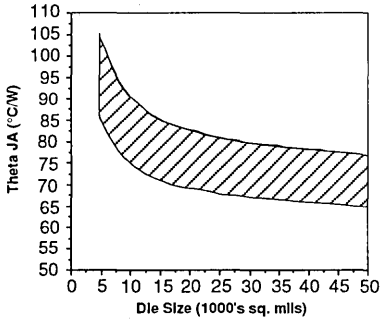
Delco Temp09 Thermal Die Array (.500"sq.)
applied power = 3W

GD 208 THETA JA VS. AIRFLOW

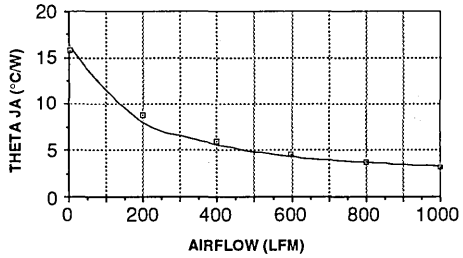


Delco Temp09 Thermal Die (.250"sq.)

Theta JA - Still Air 16-20 Lead Ceramic Dips

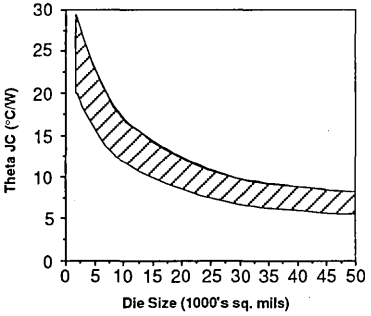


THETA JA vs. AIRFLOW
447 PIN PGA - R4000 PACKAGE
INTEGRAL CuW HEATSINK - NO FIN ATTACHED

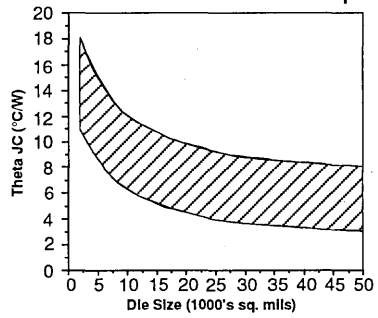


Delco Temp09 Thermal Die Array (.500"sq.)
applied power = 3W

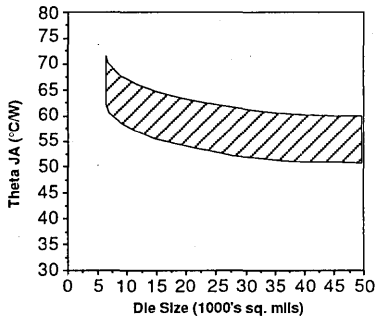
Theta JC 16-20 Lead Ceramic Dip



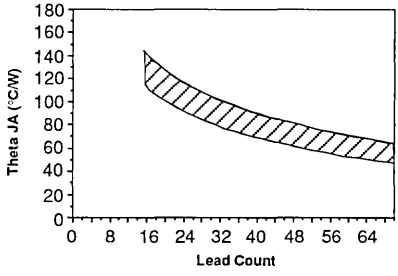
Theta JC 22-40 Lead Ceramic Dips



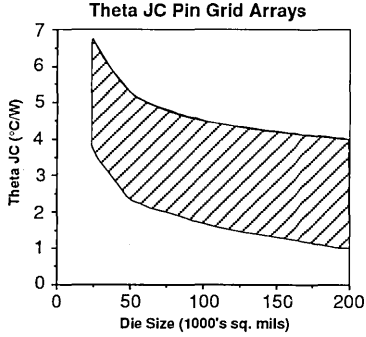
Theta JA - Still Air 22-40 Ceramic Dips



Theta JA Ceramic Flatpacks/Cerpacks

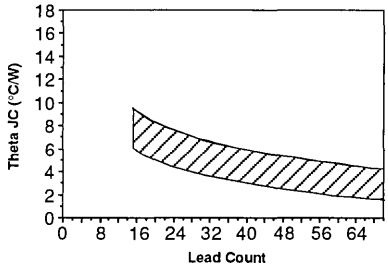


Theta JC Pin Grid Arrays

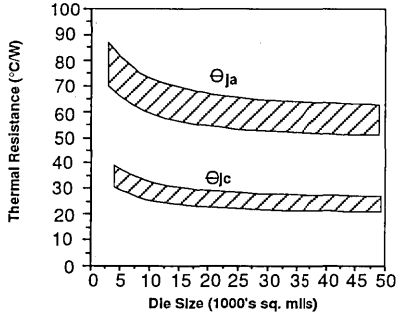


4

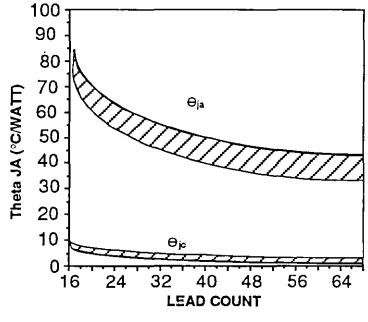
Theta JC Ceramic Flatpacks/Cerpacks



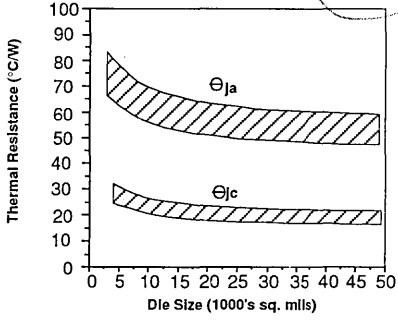
PLASTIC DIPS: 16,18 & 20 PINS



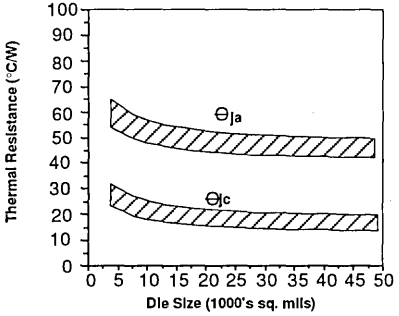
Thermal Resistance of Ceramic LCC's



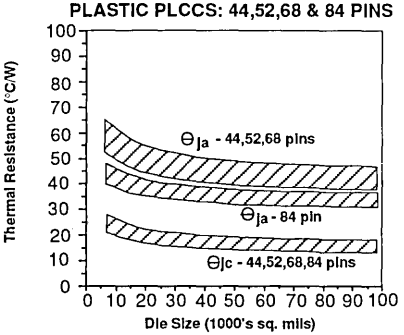
PLASTIC SOICS: 24,28 & 32 PINS



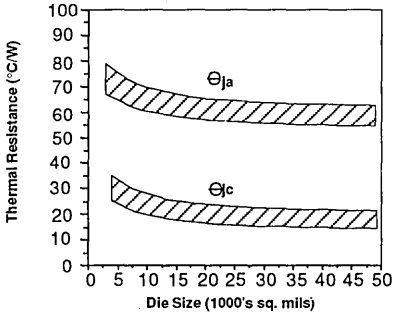
PLASTIC DIPS: 22,24 & 28 PINS



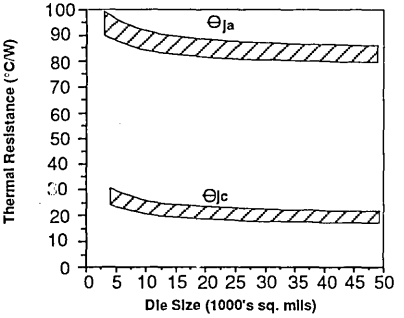
PLASTIC PLCCS: 44,52,68 & 84 PINS



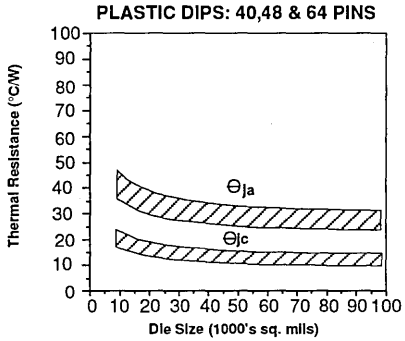
PLASTIC PLCCS: 28 & 32 PINS



PLASTIC SOICS: 16 & 20 PINS



PLASTIC DIPS: 40,48 & 64 PINS

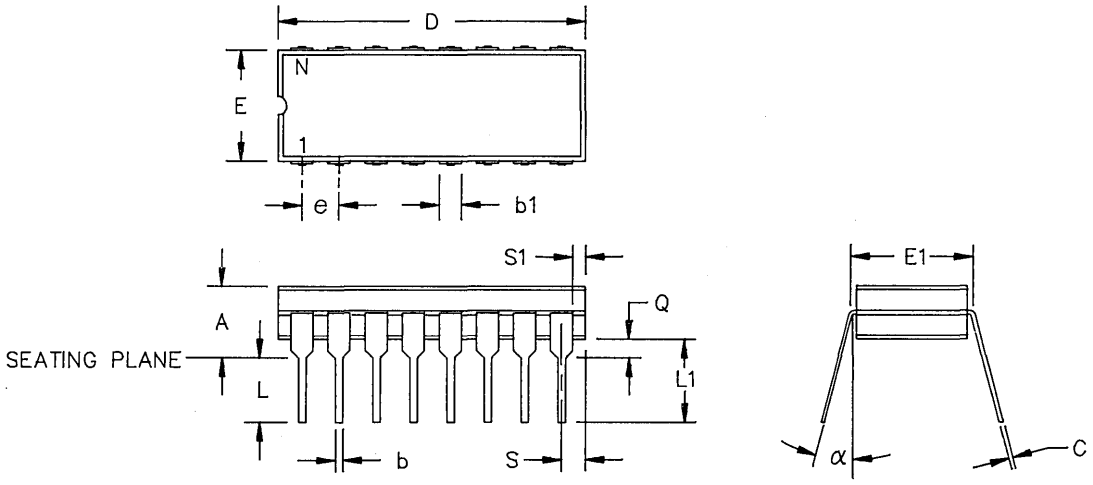


PACKAGE DIAGRAM OUTLINE INDEX

Integrated Device Technology, Inc.

PACKAGE DIAGRAM OUTLINES

DUAL IN–LINE PACKAGES



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. THE MINIMUM LIMIT FOR DIMENSION b1 MAY BE .023 FOR CORNER LEADS.

16–28 LEAD CERDIP (300 MIL)

DWG #	D16–1		D18–1		D20–1		D22–1		D24–1		D28–3	
# OF LDS (N)	16		18		20		22		24		28	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.140	.200	.140	.200	.140	.200	.140	.200	.140	.200	.140	.200
b	.015	.021	.015	.021	.015	.021	.015	.021	.015	.021	.015	.021
b1	.045	.060	.045	.060	.045	.060	.045	.060	.045	.065	.045	.065
C	.009	.012	.009	.012	.009	.012	.009	.012	.009	.014	.009	.014
D	.750	.830	.880	.930	.935	1.060	1.050	1.080	1.240	1.280	1.440	1.485
E	.285	.310	.285	.310	.285	.310	.285	.310	.285	.310	.285	.310
E1	.290	.320	.290	.320	.290	.320	.300	.320	.300	.320	.300	.320
e	.100	BSC	.100	BSC	.100	BSC	.100	BSC	.100	BSC	.100	BSC
L	.125	.175	.125	.175	.125	.175	.125	.175	.125	.175	.125	.175
L1	.150	–	.150	–	.150	–	.150	–	.150	–	.150	–
Q	.015	.055	.015	.055	.015	.060	.015	.060	.015	.060	.015	.060
S	.020	.080	.020	.080	.020	.080	.020	.080	.030	.080	.030	.080
S1	.005	–	.005	–	.005	–	.005	–	.005	–	.005	–
α	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°

DUAL IN-LINE PACKAGES (Continued)

24-40 LEAD CERDIP (400 & 600 MIL)

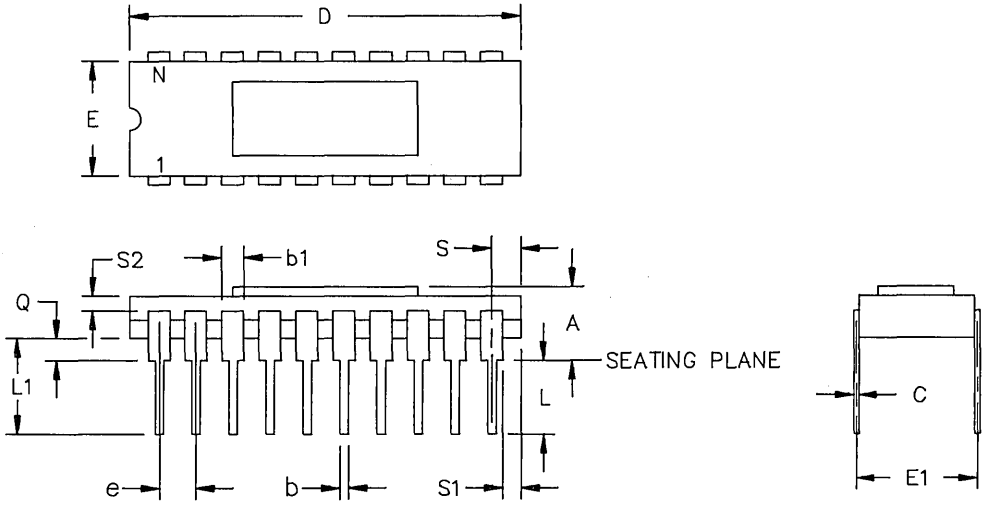
DWG #	D24-3		D24-2		D28-1		D40-1	
# OF LDS (N)	24		24		28		40	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.130	.175	.090	.190	.090	.200	.160	.220
b	.015	.021	.014	.023	.014	.023	.014	.023
b1	.045	.065	.045	.060	.045	.065	.045	.065
C	.009	.014	.008	.012	.008	.014	.008	.014
D	1.180	1.250	1.230	1.290	1.440	1.490	2.020	2.070
E	.350	.410	.500	.610	.510	.600	.510	.600
E1	.380	.420	.590	.620	.590	.620	.590	.620
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC	
L	.125	.175	.125	.200	.125	.200	.125	.200
L1	.150	–	.150	–	.150	–	.150	–
Q	.015	.060	.015	.060	.020	.060	.020	.060
S	.030	.070	.030	.080	.030	.080	.030	.080
S1	.005	–	.005	–	.005	–	.005	–
α	0°	15°	0°	15°	0°	15°	0°	15°

32 LEAD CERDIP (WIDE BODY)

DWG #	D32-1	
# OF LDS (N)	32	
SYMBOL	MIN	MAX
A	.120	.210
b	.014	.023
b1	.045	.065
C	.008	.014
D	1.625	1.675
E	.570	.600
E1	.590	.620
e	.100 BSC	
L	.125	.200
L1	.150	–
Q	.020	.060
S	.030	.080
S1	.005	–
α	0°	15°

DUAL IN-LINE PACKAGES (Continued)

20-32 LEAD SIDE BRAZE (300 MIL)

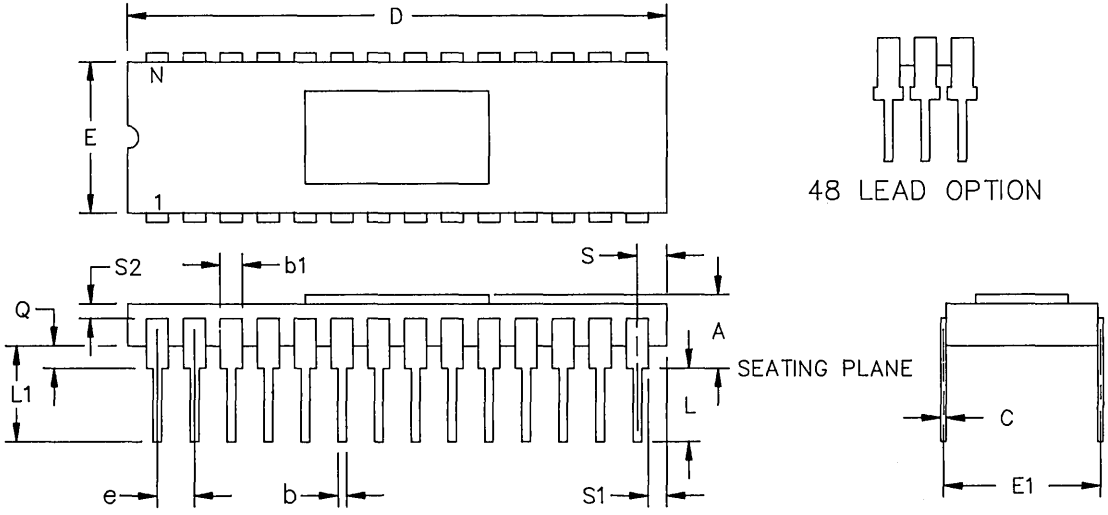


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	C20-1		C22-1		C24-1		C28-1		C32-3	
# OF LDS (N)	20		22		24		28		32	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.200	.100	.200	.090	.200	.090	.200	.090	.200
b	.014	.023	.014	.023	.015	.023	.014	.023	.014	.023
b1	.045	.060	.045	.060	.045	.060	.045	.060	.045	.060
C	.008	.015	.008	.015	.008	.015	.008	.015	.008	.014
D	.970	1.060	1.040	1.120	1.180	1.230	1.380	1.420	1.580	1.640
E	.260	.310	.260	.310	.220	.310	.220	.310	.280	.310
E1	.290	.320	.290	.320	.290	.320	.290	.320	.290	.320
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC	
L	.125	.200	.125	.200	.125	.200	.125	.200	.100	.175
L1	.150	–	.150	–	.150	–	.150	–	.150	–
Q	.015	.060	.015	.060	.015	.060	.015	.060	.030	.060
S	.030	.065	.030	.065	.030	.065	.030	.065	.030	.065
S1	.005	–	.005	–	.005	–	.005	–	.005	–
S2	.005	–	.005	–	.005	–	.005	–	.005	–

DUAL IN-LINE PACKAGES (Continued)

28-48 LEAD SIDE BRAZE (400 MIL)

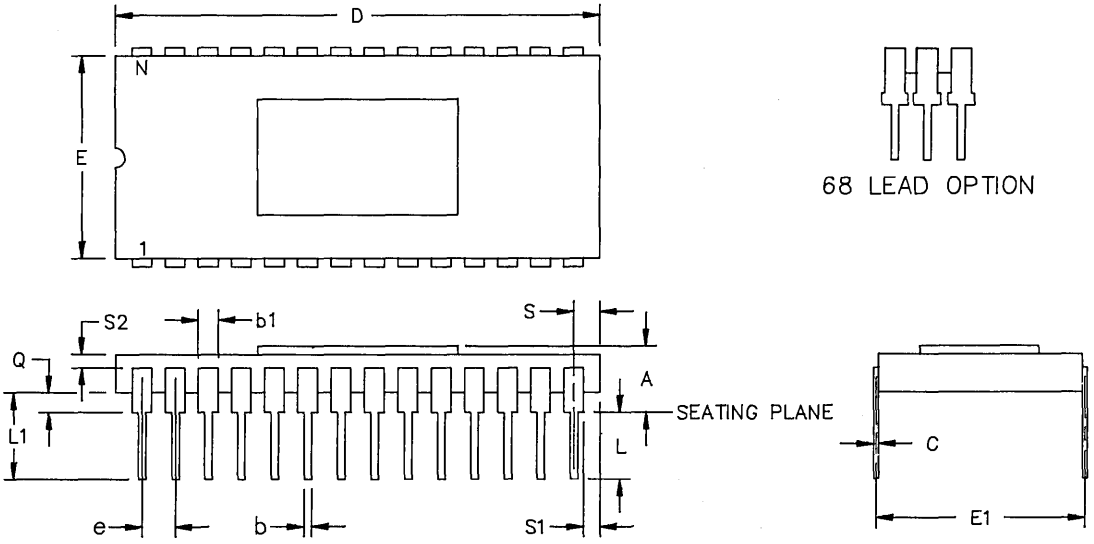


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	C28-2		C32-2		C48-1	
# OF LDS (N)	28		32		48	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.200	.090	.200	.085	.190
b	.014	.023	.014	.023	.014	.023
b1	.045	.060	.045	.060	.045	.060
C	.008	.014	.008	.014	.008	.014
D	1.380	1.420	1.580	1.640	1.690	1.730
E	.380	.420	.380	.410	.380	.410
E1	.390	.420	.390	.420	.390	.420
e	.100 BSC		.100 BSC		.070 BSC	
L	.100	.175	.100	.175	.125	.175
L1	.150	–	.150	–	.150	–
Q	.030	.060	.030	.060	.020	.070
S	.030	.065	.030	.065	.030	.065
S1	.005	–	.005	–	.005	–
S2	.005	–	.005	–	.005	–

DUAL IN-LINE PACKAGES (Continued)

24-68 LEAD SIDE BRAZE (600 MIL)

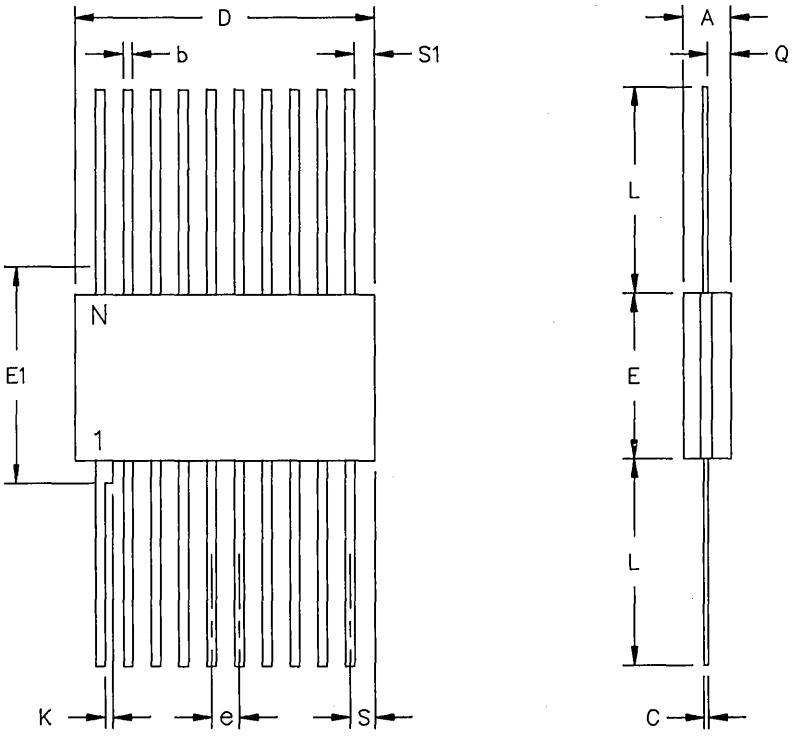


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	C24-2		C28-3		C32-1		C40-1		C48-2		C68-1	
# OF LDS (N)	24		28		32		40		48		68	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.190	.085	.190	.100	.190	.085	.190	.100	.190	.085	.190
b	.015	.023	.015	.022	.015	.023	.015	.023	.015	.023	.015	.023
b1	.045	.060	.045	.060	.045	.060	.045	.060	.045	.060	.045	.060
C	.008	.012	.008	.012	.008	.014	.008	.012	.008	.012	.008	.012
D	1.180	1.220	1.380	1.430	1.580	1.640	1.980	2.030	2.370	2.430	2.380	2.440
E	.575	.610	.580	.610	.580	.610	.580	.610	.550	.610	.580	.610
E1	.595	.620	.595	.620	.590	.620	.595	.620	.595	.620	.590	.620
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC		.070 BSC	
L	.125	.175	.125	.175	.100	.175	.125	.175	.125	.175	.125	.175
L1	.150	–	.150	–	.150	–	.150	–	.150	–	.150	–
Q	.020	.060	.020	.060	.020	.060	.020	.060	.020	.060	.020	.070
S	.030	.065	.030	.065	.030	.065	.030	.065	.030	.065	.030	.065
S1	.005	–	.005	–	.005	–	.005	–	.005	–	.005	–
S2	.005	–	.005	–	.005	–	.005	–	.005	–	.005	–

CERPACKS

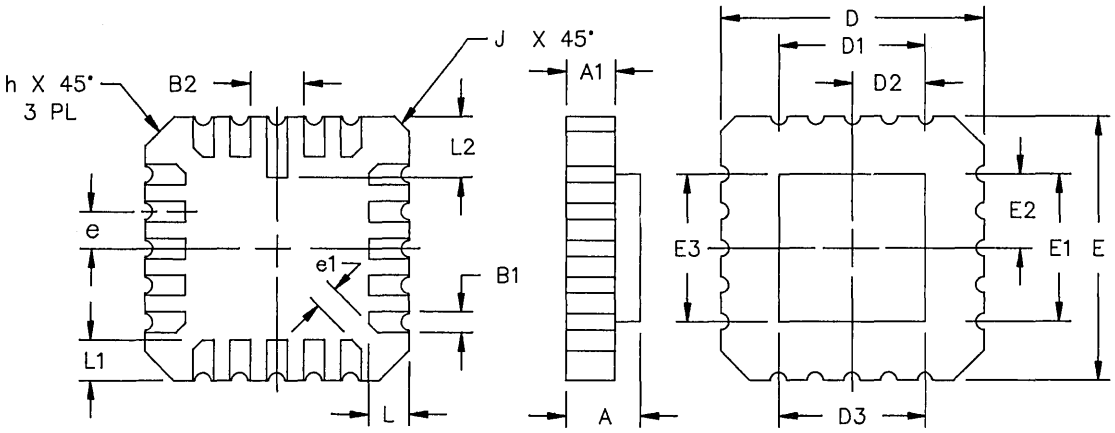
16–28 LEAD CERPACK

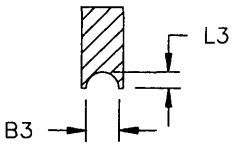


NOTES:
1. ALL DIMENSION ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	E16–1		E20–1		E24–1		E28–1		E28–2	
# OF LDS (N)	16		20		24		28		28	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.055	.085	.045	.092	.045	.090	.045	.115	.045	.090
b	.015	.019	.015	.019	.015	.019	.015	.019	.015	.019
C	.0045	.006	.0045	.006	.0045	.006	.0045	.006	.0045	.006
D	.370	.430	–	.540	–	.640	–	.740	–	.740
E	.245	.285	.245	.300	.300	.420	.460	.520	.340	.380
E1	–	.305	–	.305	–	.440	–	.550	–	.400
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
K	.008	.015	.008	.015	.008	.015	.008	.015	.008	.015
L	.250	.370	.250	.370	.250	.370	.250	.370	.250	.370
Q	.026	.040	.026	.040	.026	.040	.026	.045	.026	.045
S	–	.045	–	.045	–	.045	–	.045	–	.045
S1	.005	–	.005	–	.005	–	.000	–	.005	–

LEADLESS CHIP CARRIERS



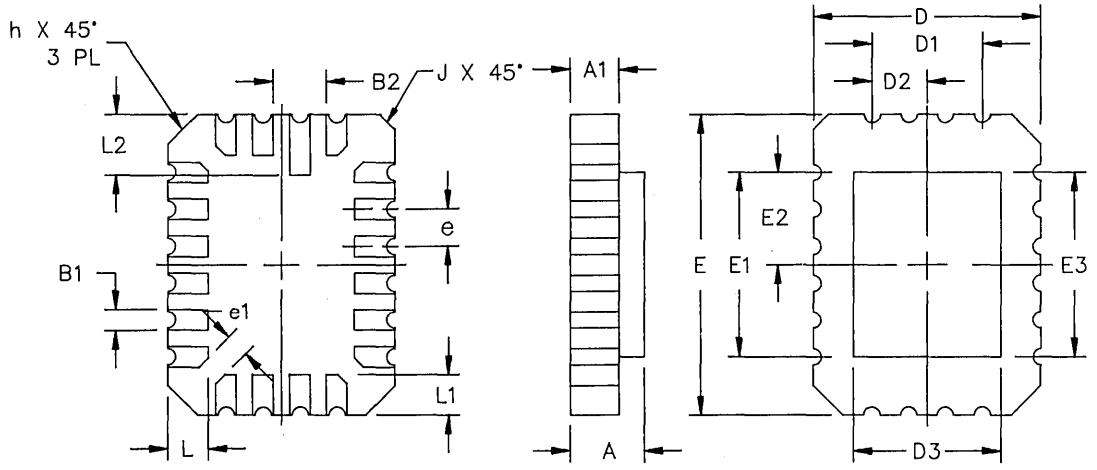


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

20–48 LEAD LCC (SQUARE)

DWG #	L20–2		L28–1		L44–1		L48–1	
# OF LDS (N)	20		28		44		48	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.064	.100	.064	.100	.064	.120	.055	.120
A1	.054	.066	.050	.088	.054	.088	.045	.090
B1	.022	.028	.022	.028	.022	.028	.017	.023
B2	.072 REF		.072 REF		.072 REF		.072 REF	
B3	.006	.022	.006	.022	.006	.022	.006	.022
D/E	.342	.358	.442	.460	.640	.660	.554	.572
D1/E1	.200 BSC		.300 BSC		.500 BSC		.440 BSC	
D2/E2	.100 BSC		.150 BSC		.250 BSC		.220 BSC	
D3/E3	–	.358	–	.460	–	.560	.500	.535
e	.050 BSC		.050 BSC		.050 BSC		.040 BSC	
e1	.015	–	.015	–	.015	–	.015	–
h	.040 REF		.040 REF		.040 REF		.012 RADIUS	
J	.020 REF		.020 REF		.020 REF		.020 REF	
L	.045	.055	.045	.055	.045	.055	.033	.047
L1	.045	.055	.045	.055	.045	.055	.033	.047
L2	.077	.093	.077	.093	.077	.093	.077	.093
L3	.003	.015	.003	.015	.003	.015	.003	.015
ND/NE	5		7		11		12	

LEADLESS CHIP CARRIERS (Continued)

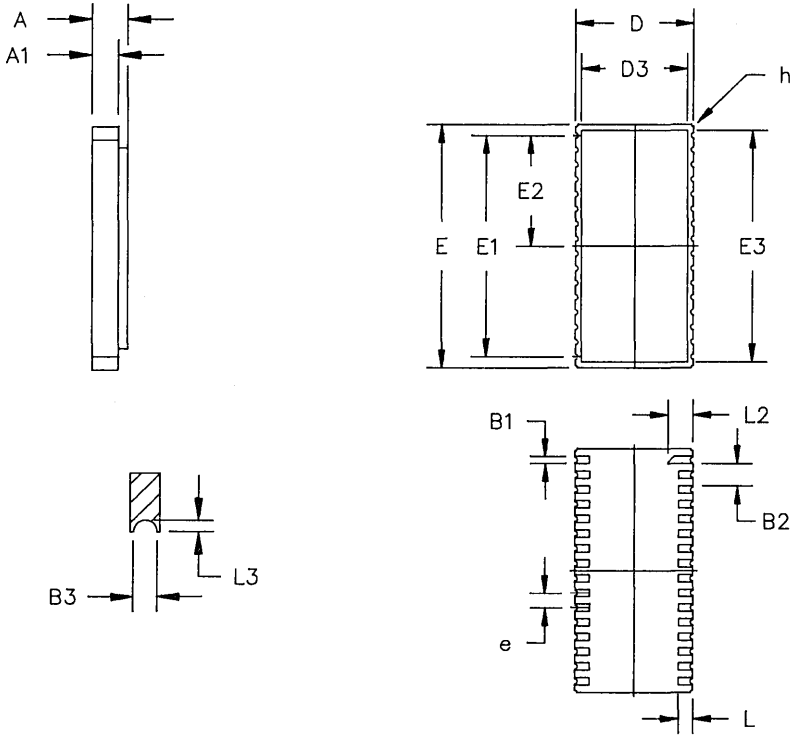


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

20–32 LEAD LCC (RECTANGULAR)

DWG #	L20–1		L22–1		L24–1		L28–2		L32–1	
# OF LDS (N)	20		22		24		28		32	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.060	.075	.064	.100	.064	.120	.060	.120	.060	.120
A1	.050	.065	.054	.063	.054	.066	.050	.088	.050	.088
B1	.022	.028	.022	.028	.022	.028	.022	.028	.022	.028
B2	.072 REF		.072 REF		.072 REF		.072 REF		.072 REF	
B3	.006	.022	.006	.022	.006	.022	.006	.022	.006	.022
D	.284	.296	.284	.296	.292	.308	.342	.358	.442	.458
D1	.150 BSC		.150 BSC		.200 BSC		.200 BSC		.300 BSC	
D2	.075 BSC		.075 BSC		.100 BSC		.100 BSC		.150 BSC	
D3	–	.280	–	.280	–	.308	–	.358	–	.458
E	.420	.435	.480	.496	.392	.408	.540	.560	.540	.560
E1	.250 BSC		.300 BSC		.300 BSC		.400 BSC		.400 BSC	
E2	.125 BSC		.150 BSC		.150 BSC		.200 BSC		.200 BSC	
E3	–	.410	–	.480	–	.408	–	.558	–	.558
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
e1	.015	–	.015	–	.015	–	.015	–	.015	–
h	.040 REF		.012 RADIUS		.025 REF		.040 REF		.040 REF	
J	.020 REF		.012 RADIUS		.015 REF		.020 REF		.020 REF	
L	.045	.055	.039	.051	.040	.050	.045	.055	.045	.055
L1	.045	.055	.039	.051	.040	.050	.045	.055	.045	.055
L2	.080	.095	.083	.097	.077	.093	.077	.093	.077	.093
L3	.003	.015	.003	.015	.003	.015	.003	.015	.003	.015
ND	4		4		5		5		7	
NE	6		7		7		9		9	

LEADLESS CHIP CARRIERS (Continued)



32 LD LCC (SMALL OUTLINE – RECTANGULAR)

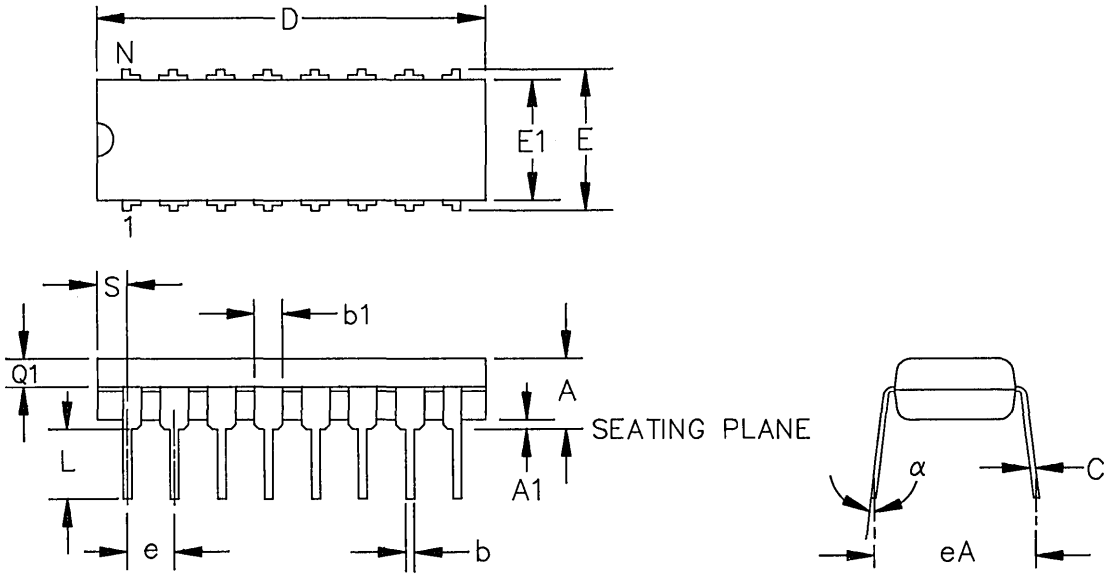
DWG #	L32-2	
# OF LDS (N)	32	
SYMBOL	MIN	MAX
A	.080	.100
A1	.060	.090
B1	.022	.028
B2	.072 REF	
B3	.006	.022
D	.392	.408
D3	–	.400
E	.800	.840
E1	.750 BSC	
E2	.375 BSC	
E3	–	.820
e	.050 BSC	
h	.008R REF	
L	.040	.060
L2	.075	.095
L3	.003	.015

NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

PLASTIC DUAL IN-LINE PACKAGES

16-32 LEAD PLASTIC DIP (300 MIL)

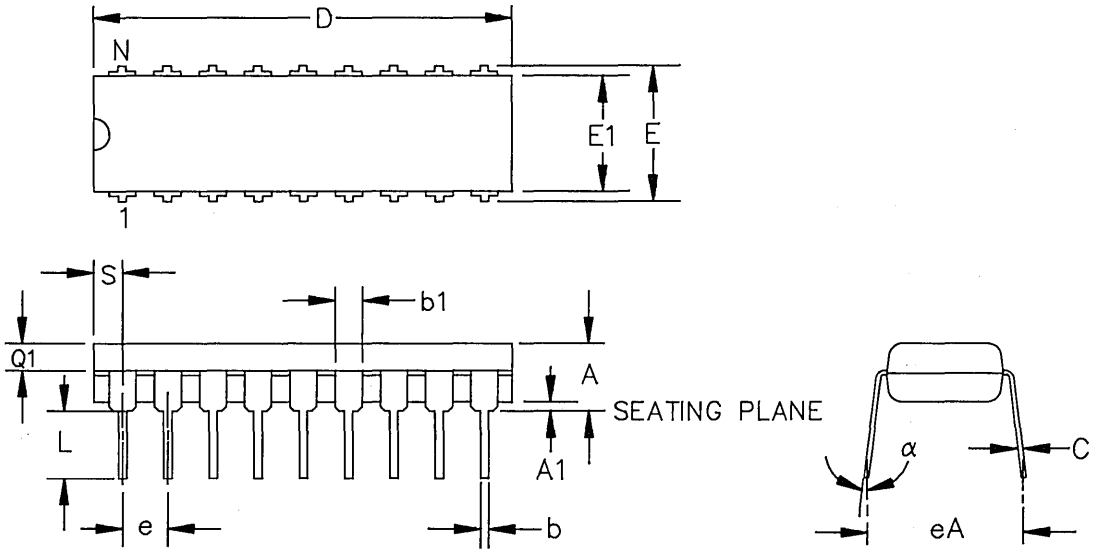


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. D & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DWG #	P16-1		P22-1		P28-2		P32-2	
# OF LDS (N)	16		22		28		32	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.140	.165	.145	.165	.145	.180	.145	.180
A1	.015	.035	.015	.035	.015	.030	.015	.030
b	.015	.022	.015	.022	.015	.022	.016	.022
b1	.050	.070	.050	.065	.045	.065	.045	.060
C	.008	.012	.008	.012	.008	.015	.008	.015
D	.745	.760	1.050	1.060	1.345	1.375	1.545	1.585
E	.300	.325	.300	.320	.300	.325	.300	.325
E1	.247	.260	.240	.270	.270	.295	.275	.295
e	.090	.110	.090	.110	.090	.110	.090	.110
eA	.310	.370	.310	.370	.310	.400	.310	.400
L	.120	.150	.120	.150	.120	.150	.120	.150
α	0°	15°	0°	15°	0°	15°	0°	15°
S	.015	.035	.020	.040	.020	.042	.020	.060
Q1	.050	.070	.055	.075	.055	.065	.055	.065

PLASTIC DUAL IN-LINE PACKAGES (Continued)

18-24 LEAD PLASTIC DIP (300 MIL - FULL LEAD)

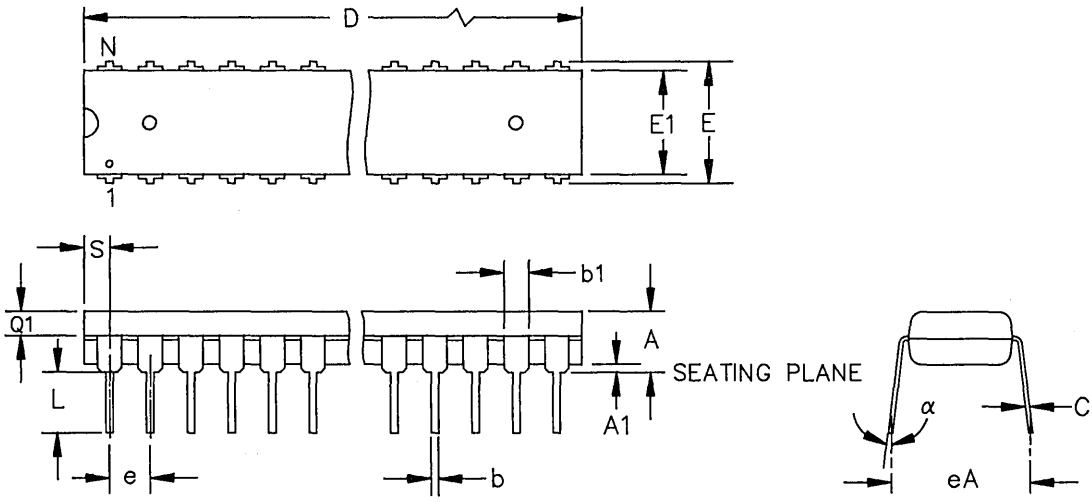


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. D & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DWG #	P18-1		P20-1		P24-1	
# OF LDS (N)	18		20		24	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX
A	.140	.165	.145	.165	.145	.165
A1	.015	.035	.015	.035	.015	.035
b	.015	.020	.015	.020	.015	.020
b1	.050	.070	.050	.070	.050	.065
C	.008	.012	.008	.012	.008	.012
D	.885	.910	1.022	1.040	1.240	1.255
E	.300	.325	.300	.325	.300	.320
E1	.247	.260	.240	.280	.250	.275
e	.090	.110	.090	.110	.090	.110
eA	.310	.370	.310	.370	.310	.370
L	.120	.150	.120	.150	.120	.150
α	0°	15°	0°	15°	0°	15°
S	.040	.060	.025	.070	.055	.075
Q1	.050	.070	.055	.075	.055	.070

PLASTIC DUAL IN-LINE PACKAGES (Continued)

28 & 32 LEAD PLASTIC DIP (400 MIL)

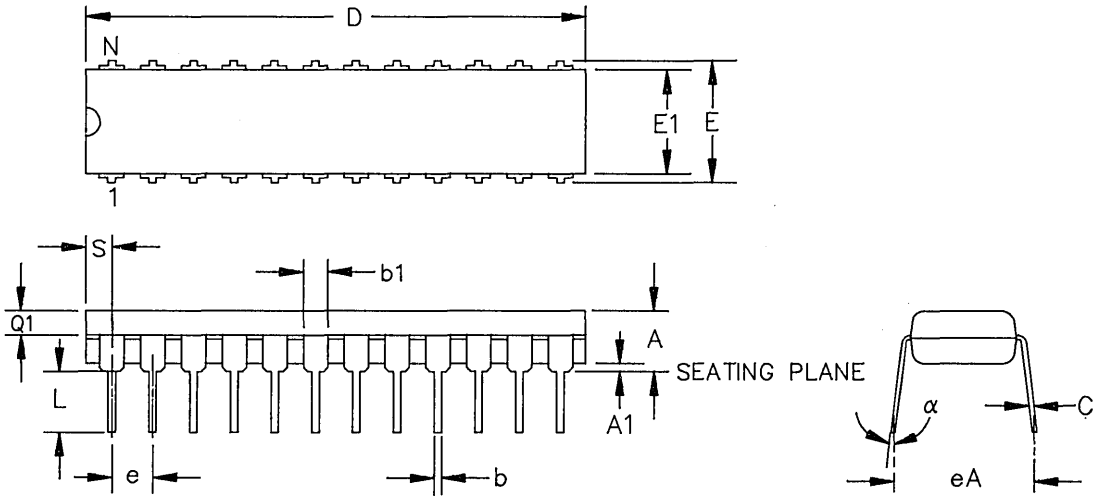


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. D & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DWG #	P28-3		P32-3	
# OF LEADS (N)	28		32	
SYMBOLS	MIN	MAX	MIN	MAX
A	–	.210	–	.200
A1	.015	–	.015	–
b	.014	.022	.014	.022
b1	.045	.065	.045	.065
C	.009	.015	.009	.015
D	1.380	1.420	1.610	1.620
E	.390	.425	.390	.425
E1	.340	.390	.340	.390
e	.100 BSC		.100 BSC	
eA	.400 BSC		.400 BSC	
L	.115	.160	.115	.160
α	0°	15°	0°	15°
S	.040	.070	.040	.070
Q1	.060	.090	.060	.090

PLASTIC DUAL IN-LINE PACKAGES (Continued)

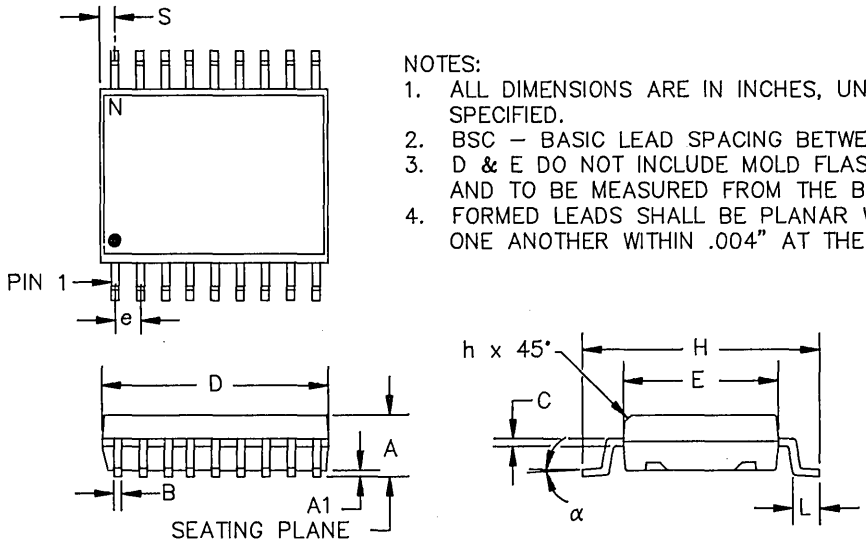
24-48 LEAD PLASTIC DIP (600 MIL)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. D & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DWG #	P24-2		P28-1		P32-1		P40-1		P48-1	
# OF LEADS (N)	24		28		32		40		48	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.160	.185	.160	.185	.170	.190	.160	.185	.170	.200
A1	.015	.035	.015	.035	.015	.050	.015	.035	.015	.035
b	.015	.020	.015	.020	.016	.020	.015	.020	.015	.020
b1	.050	.065	.050	.065	.045	.055	.050	.065	.050	.065
C	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012
D	1.240	1.260	1.420	1.460	1.645	1.655	2.050	2.070	2.420	2.450
E	.600	.620	.600	.620	.600	.625	.600	.620	.600	.620
E1	.530	.550	.530	.550	.530	.550	.530	.550	.530	.560
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
eA	.610	.670	.610	.670	.610	.670	.610	.670	.610	.670
L	.120	.150	.120	.150	.125	.135	.120	.150	.120	.150
α	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°
S	.060	.080	.055	.080	.070	.080	.070	.085	.060	.075
Q1	.060	.080	.060	.080	.065	.075	.060	.080	.060	.080

SMALL OUTLINE IC

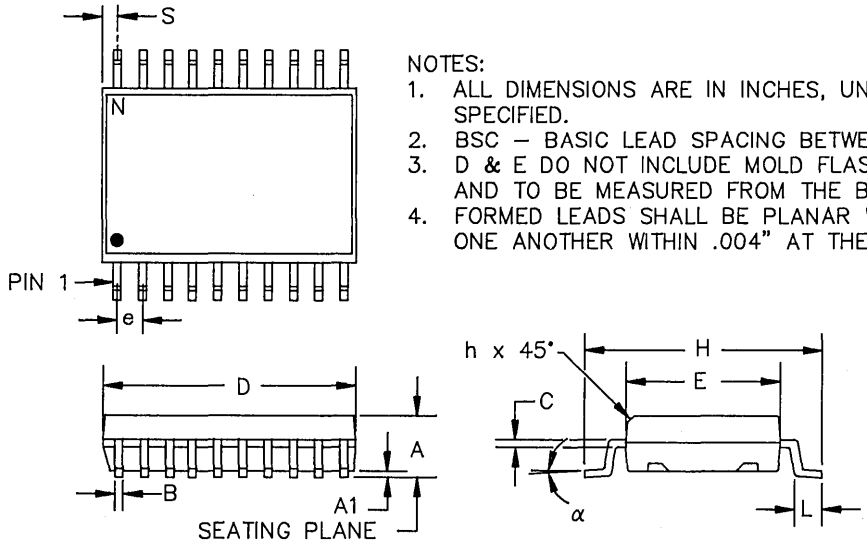


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND TO BE MEASURED FROM THE BOTTOM OF PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.

16–24 LEAD SMALL OUTLINE (GULL WING – JEDEC)

DWG #	SO16–1		SO18–1		SO20–2		SO24–2	
# OF LDS (N)	16 (.300)		18 (.300)		20 (.300")		24 (.300")	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.095	.1043	.095	.1043	.095	.1043	.095	.1043
A1	.005	.0118	.005	.0118	.005	.0118	.005	.0118
B	.014	.020	.014	.020	.014	.020	.014	.020
C	.0091	.0125	.0091	.0125	.0091	0125	.0091	.0125
D	.403	.413	.447	.462	.497	.511	.600	.614
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC	
E	.292	.2992	.292	.2992	.292	.2992	.292	.2992
h	.010	.020	.010	.020	.010	.020	.010	.020
H	.400	.419	.400	.419	.400	.419	.400	.419
L	.018	.045	.018	.045	.018	.045	.018	.045
α	0°	8°	0°	8°	0°	8°	0°	8°
S	.023	.035	.023	.035	.023	.035	.023	.035

SMALL OUTLINE IC (Continued)



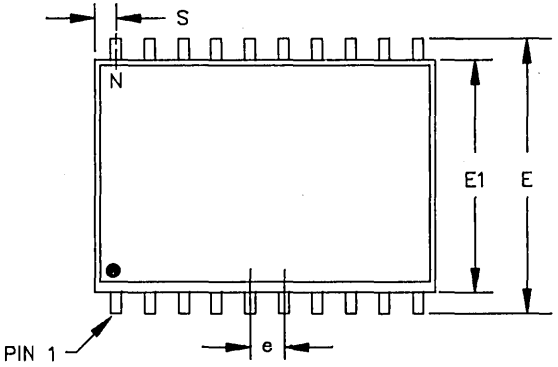
NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND TO BE MEASURED FROM THE BOTTOM OF THE PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.

4

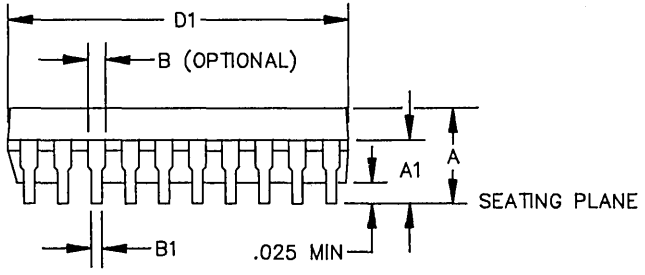
28 LEAD SMALL OUTLING (GULL WING – JEDEC)

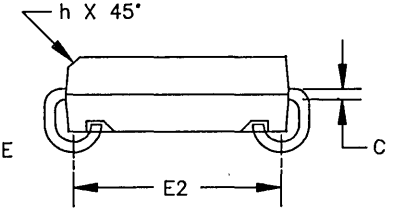
DWG #	SO28–2		SO28–3	
# OF LDS (N)	28 (.300")		28 (.330")	
SYMBOL	MIN	MAX	MIN	MAX
A	.095	.1043	.110	.120
A1	.005	.0118	.005	.014
B	.014	.020	.014	.019
C	.0091	.0125	.006	.010
D	.700	.712	.718	.728
e	.050 BSC		.050 BSC	
E	.292	.2992	.340	.350
h	.010	.020	.012	.020
H	.400	.419	.462	.478
L	.018	.045	.028	.045
α	0°	8°	0°	8°
S	.023	.035	.023	.035

SMALL OUTLINE IC (Continued)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSION AND TO BE MEASURED FROM THE BOTTOM OF THE PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE

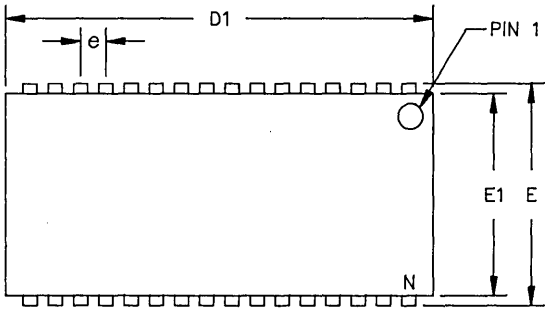




20–32 LEAD SMALL OUTLINE (J–BEND, 300 MIL)

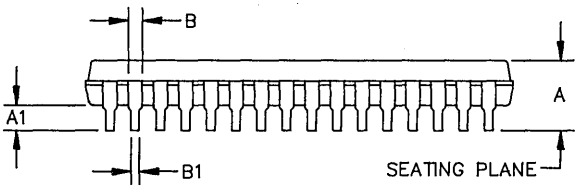
DWG #	SO20–1		SO24–4		SO24–8		SO28–5		SO32–2	
# OF LDS (N)	20		24		24		28		32	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.120	.140	.130	.148	.120	.140	.120	.140	.130	.148
A1	.078	.095	.082	.095	.078	.091	.078	.095	.082	.095
B	–	–	.026	.032	–	–	–	–	.026	.032
B1	.014	.020	.015	.020	.014	.019	.014	.020	.016	.020
C	.008	.013	.007	.011	.0091	.0125	.008	.013	.008	.013
D1	.500	.512	.620	.630	.602	.612	.700	.712	.820	.830
E	.335	.347	.335	.345	.335	.347	.335	.347	.330	.340
E1	.292	.300	.295	.305	.292	.299	.292	.300	.295	.305
E2	.262	.272	.260	.280	.262	.272	.262	.272	.260	.275
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
h	.010	.020	.010	.020	.010	.016	.012	.020	.012	.020
S	.023	.035	.032	.043	.032	.043	.023	.035	.032	.043

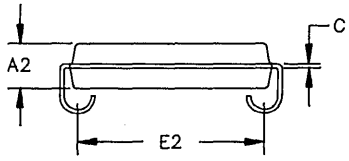
SMALL OUTLINE IC (Continued)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSION AND TO BE MEASURED FROM THE BOTTOM OF THE PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.

4



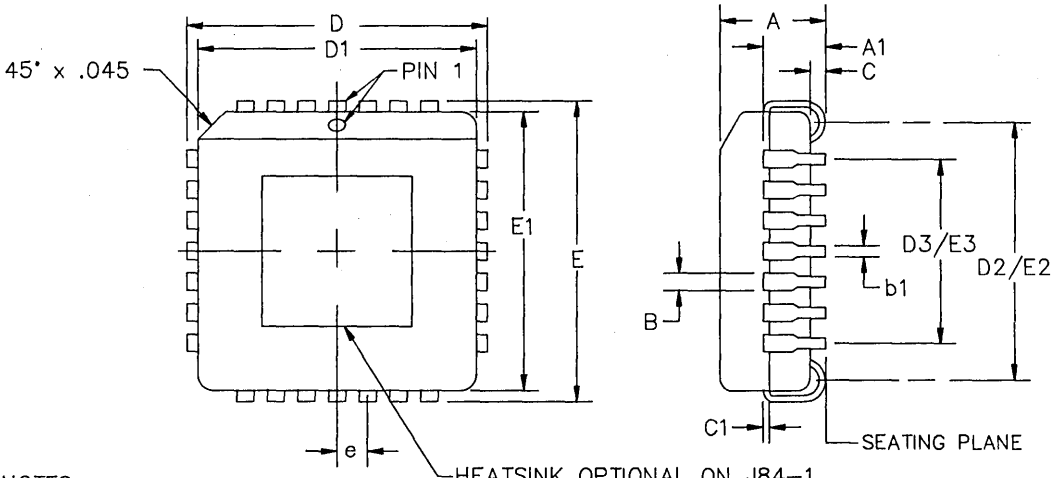


28–32 LEAD SMALL OUTLINE (J–BEND, 400 MIL)

DWG #	SO28–6		SO32–3	
# OF LDS (N)	28		32	
SYMBOLS	MIN	MAX	MIN	MAX
A	.131	.145	.131	.145
A1	.045	.055	.045	.055
A2	.086	.090	.086	.090
B	.026	.032	.026	.032
B1	.015	.020	.015	.020
C	.007	.0125	.007	.0125
D1	.720	.730	.820	.830
E	.435	.445	.435	.445
E1	.395	.405	.395	.405
E2	.360	.380	.360	.380
e	.050 BSC		.050 BSC	
h	–	–	–	–
S	.032	.043	.032	.043

PLASTIC LEADED CHIP CARRIERS

20–84 LEAD PLCC (SQUARE)



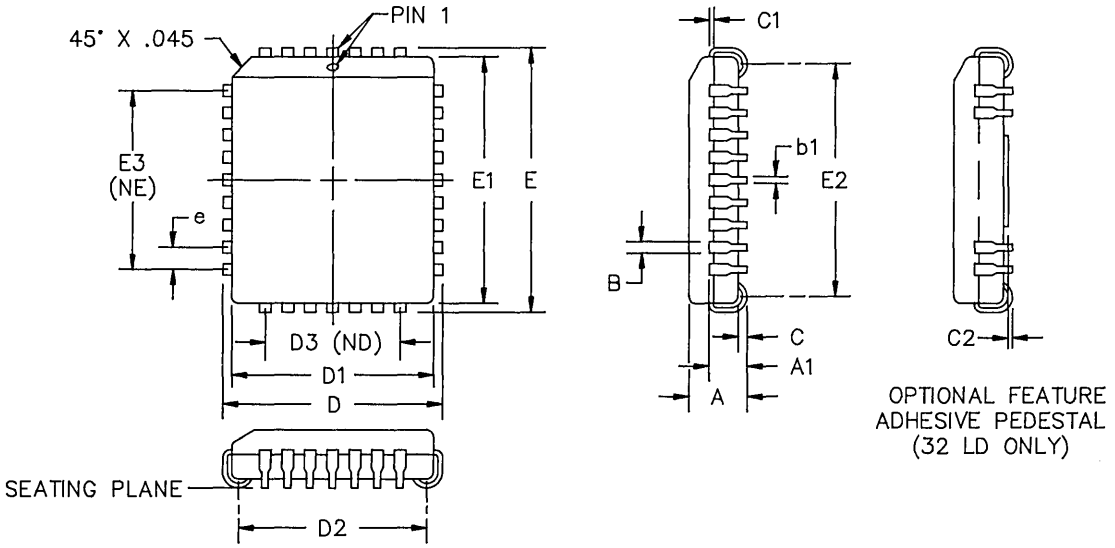
NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.
5. ND & NE REPRESENT NUMBER OF LEADS IN D & E DIRECTIONS RESPECTIVELY.
6. D1 & E1 SHOULD BE MEASURED FROM THE BOTTOM OF THE PKG.

DWG #	J20–1		J28–1		J44–1		J52–1		J68–1		J84–1	
# OF LDS	20		28		44		52		68		84	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.165	.180	.165	.180	.165	.180	.165	.180	.165	.180	.165	.180
A1	.095	.115	.095	.115	.095	.115	.095	.115	.095	.115	.095	.115
B	.026	.032	.026	.032	.026	.032	.026	.032	.026	.032	.026	.032
b1	.013	.021	.013	.021	.013	.021	.013	.021	.013	.021	.013	.021
C	.020	.040	.020	.040	.020	.040	.020	.040	.020	.040	.020	.040
C1	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012
D	.385	.395	.485	.495	.685	.695	.785	.795	.985	.995	1.185	1.195
D1	.350	.356	.450	.456	.650	.656	.750	.756	.950	.956	1.150	1.156
D2/E2	.290	.330	.390	.430	.590	.630	.690	.730	.890	.930	1.090	1.130
D3/E3	.200 REF		.300 REF		.500 REF		.600 REF		.800 REF		1.000 REF	
E	.385	.395	.485	.495	.685	.695	.785	.795	.985	.995	1.185	1.195
E1	.350	.356	.450	.456	.650	.656	.750	.756	.950	.956	1.150	1.156
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
ND/NE	5		7		11		13		17		21	

PLASTIC LEADED CHIP CARRIERS (Continued)

18–32 LEAD PLCC (RECTANGULAR)



DWG #	J18–1		J32–1	
# OF LDS	18		32	
SYMBOL	MIN	MAX	MIN	MAX
A	.120	.140	.120	.140
A1	.075	.095	.075	.095
B	.026	.032	.026	.032
b1	.013	.021	.013	.021
C	.015	.040	.015	.040
C1	.008	.012	.008	.012
C2	–	–	.005	.015
D	.320	.335	.485	.495
D1	.289	.293	.449	.453
D2	.225	.265	.390	.430
D3	.150 REF		.300 REF	
E	.520	.535	.585	.595
E1	.489	.493	.549	.553
E2	.422	.465	.490	.530
E3	.200 REF		.400 REF	
e	.050 BSC		.050 BSC	
ND/NE	4 / 5		7 / 9	

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.
5. ND & NE REPRESENT NUMBERS OF LEADS IN D & E DIRECTIONS RESPECTIVELY.
6. D1 & E1 SHOULD BE MEASURED FROM THE BOTTOM OF THE PACKAGE.

16K SRAM PRODUCTS

IDT traces its heritage back to the first fast CMOS 2K x 8 SRAM in the industry, which was introduced at 70ns more than 10 years ago. Today, IDT's 16K family still includes many of the SRAM configurations offered during the early days of the company, now available at much higher speeds. After having been through numerous die shrinks and improvements, the 16K family is a testimonial to the long term commitments that IDT typically makes to support its customers.

The 16K family is based exclusively on CMOS technology, and is now available in speeds as fast as 12ns for commercial applications and 15ns for military applications. It is offered in a wide variety of speeds and packages, and all parts have a low power version. These low power versions offer industry-leading standby power characteristics, as well as a 2V data retention mode, which makes them ideal for portable battery-operated equipment.

Size	Org.	Features	Process	Part Number	Power	Speeds	
						Commercial	Military
16K	16K x 1		CMOS	6167	SA/LA	15,20,25,35	20,25,35,45,55,70
	4K x 4		CMOS	6168	SA/LA	12,15,20,25,35	15,20,25,35,45,55,70
	4K x 4	OE	CMOS	61970	SA/LA	15,20,25,35	20,25,35,45,55
	4K x 4	Sep I/O	CMOS	71681	SA/LA	15,20,25,35,45	20,25,35,45,55,70
	4K x 4	Sep I/O	CMOS	71682	SA/LA	15,20,25,35,45	20,25,35,45,55,70
	2K x 8		CMOS	6116	SA/LA	15,20,25,35,45	20,25,35,45,55,70,90, 120,150

5

TABLE OF CONTENTS

5

Integrated Device Technology, Inc.

CMOS STATIC RAM 16K (16K x 1-BIT)

IDT6167SA
IDT6167LA

FEATURES:

- High-speed (equal access and cycle time)
  - — Military: 15/20/25/35/45/55/70/85/100ns (max.)
  - — Commercial: 12/15/20/25/35ns (max.)
- Low power consumption
- Battery backup operation — 2V data retention voltage (IDT6167LA only)
- Available in 20-pin CERDIP and Plastic DIP, 20-pin CERPACK, 20-pin SOIC and 20-pin leadless chip carrier
- Produced with advanced CMOS high-performance technology
- CMOS process virtually eliminates alpha particle soft-error rates
- Separate data input and output
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT6167 is a 16,384-bit high-speed static RAM organized as 16K x 1. The part is fabricated using IDT's high-performance, high reliability CMOS technology.

Access times as fast as 12ns are available. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes HIGH, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{CS}$ remains HIGH. This capability provides significant system-level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1µW operating off a 2V battery.

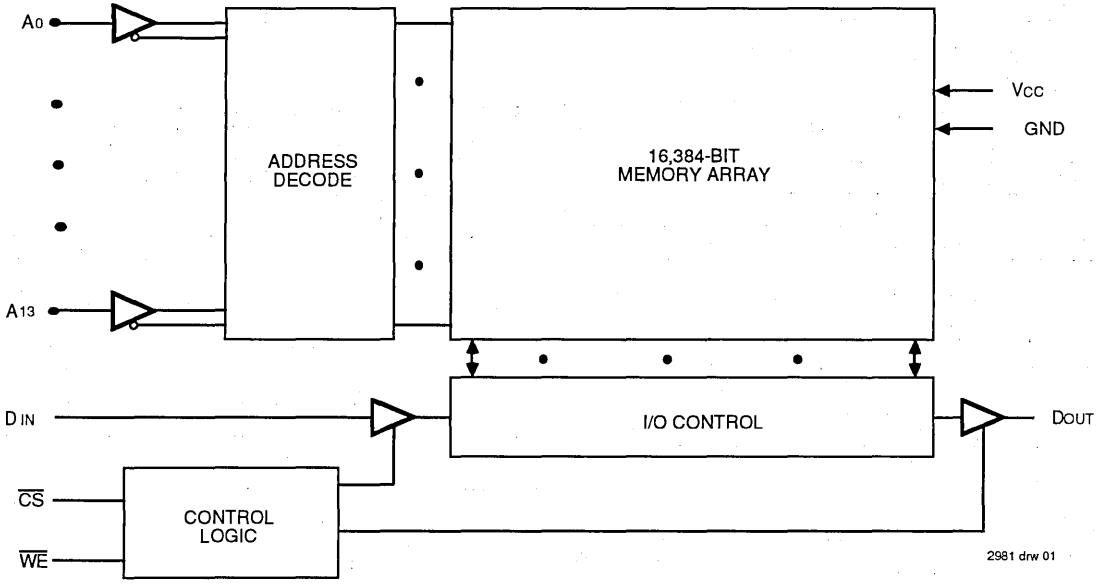
All inputs and the output of the IDT6167 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs.

The IDT6167 is packaged in a space-saving 20-pin, 300 mil Plastic DIP or CERDIP, Plastic 20-pin SOIC or SOJ, 20-pin CERPACK and 20-pin leadless chip carrier, providing high board-level packing densities.

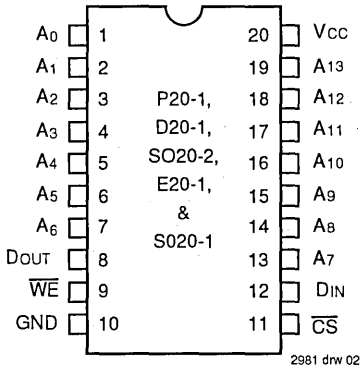
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

5

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP/SOIC/CERPACK/SOJ
TOP VIEW

PIN NAMES

A_0–A_{13}	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power
D_{IN}	$DATA_{IN}$
D_{OUT}	$DATA_{OUT}$
GND	Ground

2981 tbl 01

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2981 tbl 05
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns, once per cycle.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2981 tbl 06

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

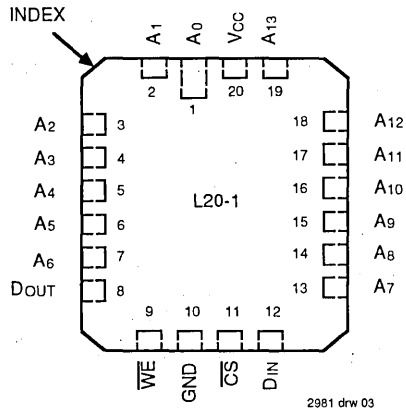
Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 2981 tbl 04
1. This parameter is determined by device characterization, but is not production tested.

TRUTH TABLE (1)

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High-Z	Standby
Read	L	H	$DATA_{OUT}$	Active
Write	L	L	High-Z	Active

NOTE: 2981 tbl 02
1. H = V_{IH}, L = V_{IL}, X = Don't Care.



LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2981 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

Symbol	Parameter	Power	6167SA12		6167SA/LA15		6167SA/LA20		6167SA/LA25		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = 0[3]	SA	90	—	90	90	90	90	90	90	mA
		LA	—	—	55	60	55	60	55	60	
I_{CC2}	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[3]	SA	140	—	120	130	100	110	100	100	mA
		LA	—	—	100	110	80	85	70	75	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[3]	SA	50	—	50	50	35	35	35	35	mA
		LA	—	—	35	35	30	30	25	25	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, V_{CC} = Max. $V_{IN} \geq V_{HC}$ or $V_{IN} \leq V_{LC}$, f = 0[3]	SA	10	—	5	10	5	10	5	10	mA
		LA	—	—	0.9	2	0.05	2	0.05	0.9	

DC ELECTRICAL CHARACTERISTICS[1] (CONTINUED)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

Symbol	Parameter	Power	6167SA/LA35		6167SA/LA45[2]		6167SA/LA55[2]		6167SA/LA70[2]		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = 0[3]	SA	90	90	—	90	—	90	—	90	mA
		LA	55	60	—	60	—	60	—	60	
I_{CC2}	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[3]	SA	100	100	—	100	—	100	—	100	mA
		LA	65	70	—	65	—	60	—	60	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[3]	SA	35	35	—	35	—	35	—	35	mA
		LA	20	20	—	20	—	20	—	15	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, V_{CC} = Max. $V_{IN} \geq V_{HC}$ or $V_{IN} \leq V_{LC}$, f = 0[3]	SA	5	10	—	10	—	10	—	10	mA
		LA	0.05	0.9	—	0.9	—	0.9	—	0.9	

NOTES:

2980 tbl 07

1. All values are maximum guaranteed values.
2. –55°C to +125°C temperature range only. Also available; 85ns and 100ns Military devices.
3. f_{MAX} = 1/t_{RC}, only address inputs cycling at f_{MAX}. f = 0 means no Address inputs change.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT6167SA Min.	IDT6167SA Max.	IDT6167LA Min.	IDT6167LA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.,	MIL	—	10	—	5	µA
		V_{IN} = GND to V_{CC}	COM'L	—	5	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH},	MIL	—	10	—	5	µA
		V_{OUT} = GND to V_{CC}	COM'L	—	5	—	2	
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OL} = -4mA, V_{CC} = Min.		2.4	—	2.4	—	V

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

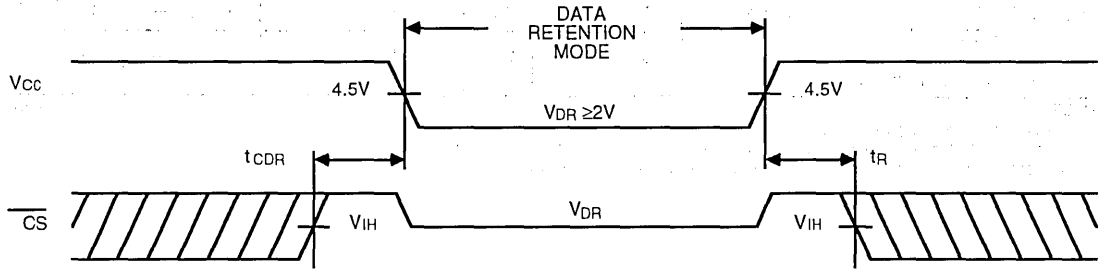
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.(1) Vcc @ 2.0v	Typ.(1) Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	Vcc for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ VIN ≥ V_{HC} or ≤ V_{LC}	MIL.	—	0.5	1.0	200	300	µA
			COM'L.	—	0.5	1.0	20	30	
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	—	—	ns
$\|I_{LI}\|$(3)	Input Leakage Current			—	—	—	2	2	µA

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization, but is not production tested.

2981 tbl 09

LOW Vcc DATA RETENTION WAVEFORM



2981 drw 04

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2979 tbl 09

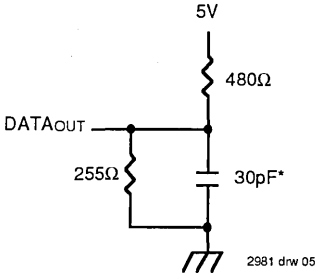


Figure 1. AC Test Load

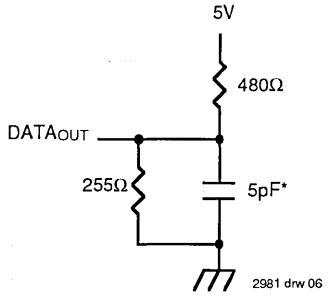


Figure 2. AC Test Load (for tCLZ, tCHZ, tWHZ and tOW)

*Includes scope and jig.

5

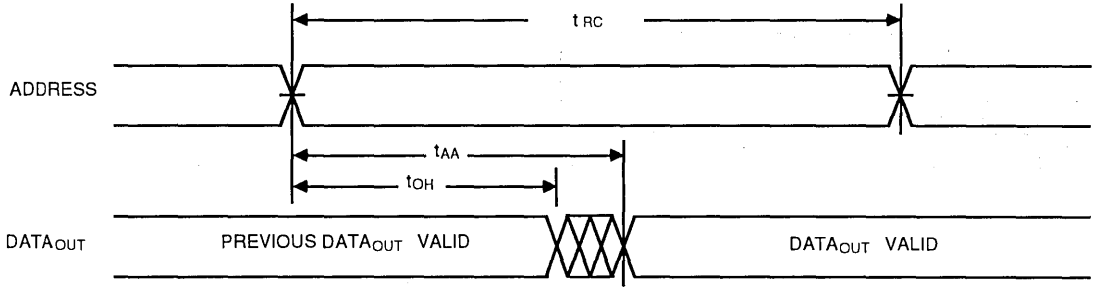
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6167SA12(1) Min.	6167SA12(1) Max.	6167SA15 6167LA15 Min.	6167SA15 6167LA15 Max.	6167SA20/25 6167LA20/25 Min.	6167SA20/25 6167LA20/25 Max.	6167SA35/45(2) 6167LA35/45(2) Min.	6167SA35/45(2) 6167LA35/45(2) Max.	6167SA55(2)/70(2) 6167LA55(2)/70(2) Min.	6167SA55(2)/70(2) 6167LA55(2)/70(2) Max.	Unit
Read Cycle												
tRC	Read Cycle Time	12	—	15	—	20/25	—	35/45	—	55/70	—	ns
tAA	Address Access Time	—	12	—	15	—	20/25	—	35/45	—	55/70	ns
tACS	Chip Select Access Time	—	12	—	15	—	20/25	—	35/45	—	55/70	ns
tCLZ	Chip Deselect to Output in Low-Z(3)	3	—	3	—	5/5	—	5/5	—	5/5	—	ns
tCHZ	Chip Select to Output in High-Z(3)	—	8	—	10	—	10/10	—	15/30	—	40/40	ns
tOH	Output Hold from Address Change	3	—	3	—	5/5	—	5/5	—	5/5	—	ns
tPU	Chip Select to Power-Up Time(3)	0	—	0	—	0/0	—	0/0	—	0/0	—	ns
tPD	Chip Deselect to Power-Down Time(3)	—	12	—	15	—	20/25	—	35/45	—	55/70	ns
Write Cycle												
tWC	Write Cycle Time	12	—	15	—	20/20	—	30/45	—	55/70	—	ns
tCW	Chip Select to End-of-Write	12	—	15	—	15/20	—	30/40	—	45/55	—	ns
tAW	Address Valid to End-of-Write	12	—	15	—	15/20	—	30/40	—	45/55	—	ns
tAS	Address Set-up Time	0	—	0	—	0/0	—	0/0	—	0/0	—	ns
tWP	Write Pulse Width	12	—	13	—	15/20	—	30/30	—	35/40	—	ns
tWR	Write Recovery Time	0	—	0	—	0/0	—	0/0	—	0/0	—	ns
tDW	Data Valid to End-of-Write	10	—	10	—	12/15	—	17/20	—	25/30	—	ns
tDH	Data Hold Time	0	—	0	—	0/0	—	0/0	—	0/0	—	ns
tWHZ	Write Enable to Output in High-Z(3)	—	6	—	7	—	8/8	—	15/30	—	40/40	ns
tOW	Output Active from End-of-Write(3)	0	—	0	—	0/0	—	0/0	—	0/0	—	ns

2981 tbl 11

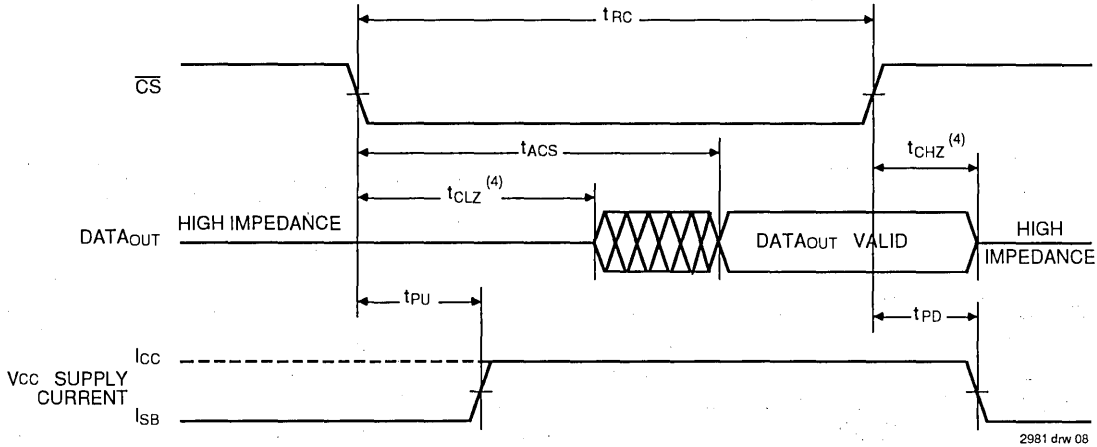
NOTES:
1. 0° to +70°C temperature range only.
2. –55°C to +125°C temperature range only. Also available: 85ns and 100ns Military devices.
3. This parameter is guaranteed with AC Load (Figure 2) by device characterization, but is not production tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1, 2)



2981 drw 07

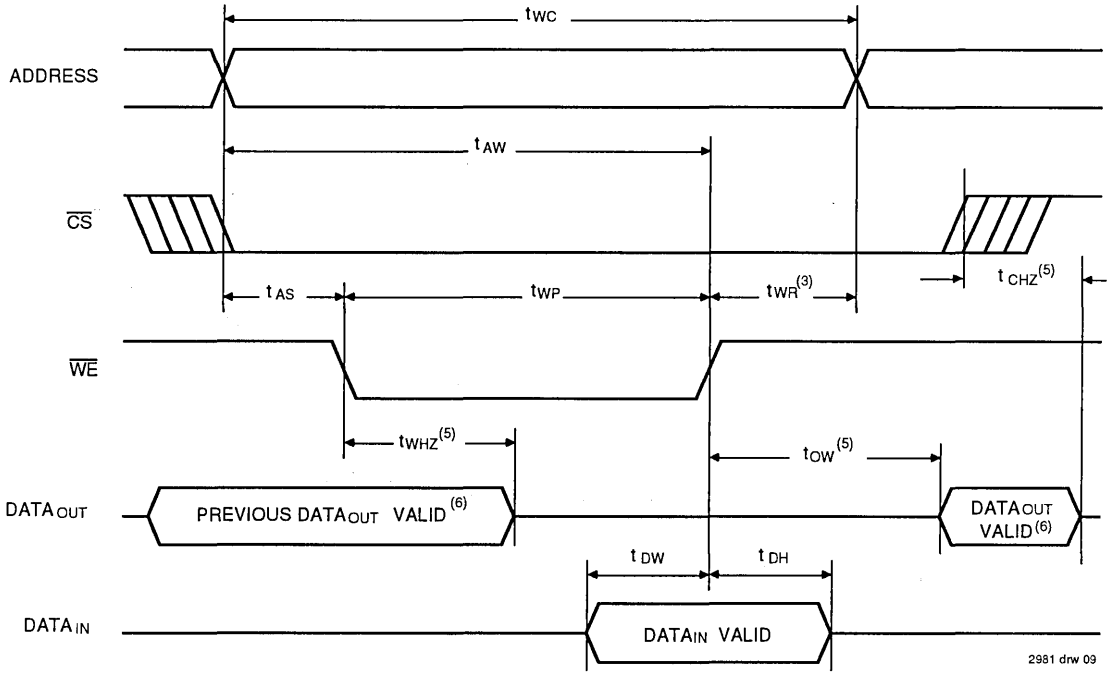
TIMING WAVEFORM OF READ CYCLE NO. 2(1, 3)



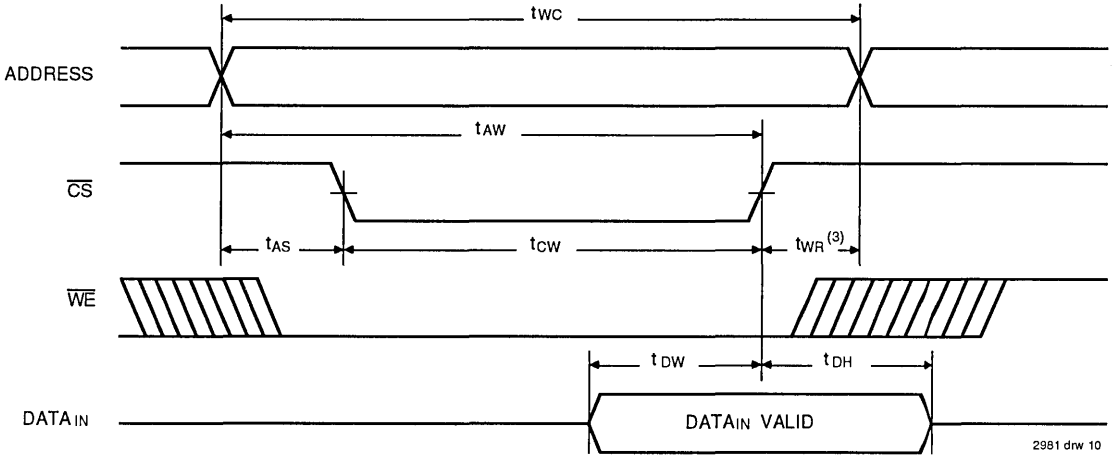
2981 drw 08

NOTES:
1. $\overline{WE}$ is HIGH for read cycle, $\overline{WE} \geq V_{IH}$
2. Device is continuously selected, $\overline{CS} \leq V_{IL}$
3. Address valid prior to or coincedent with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 4)

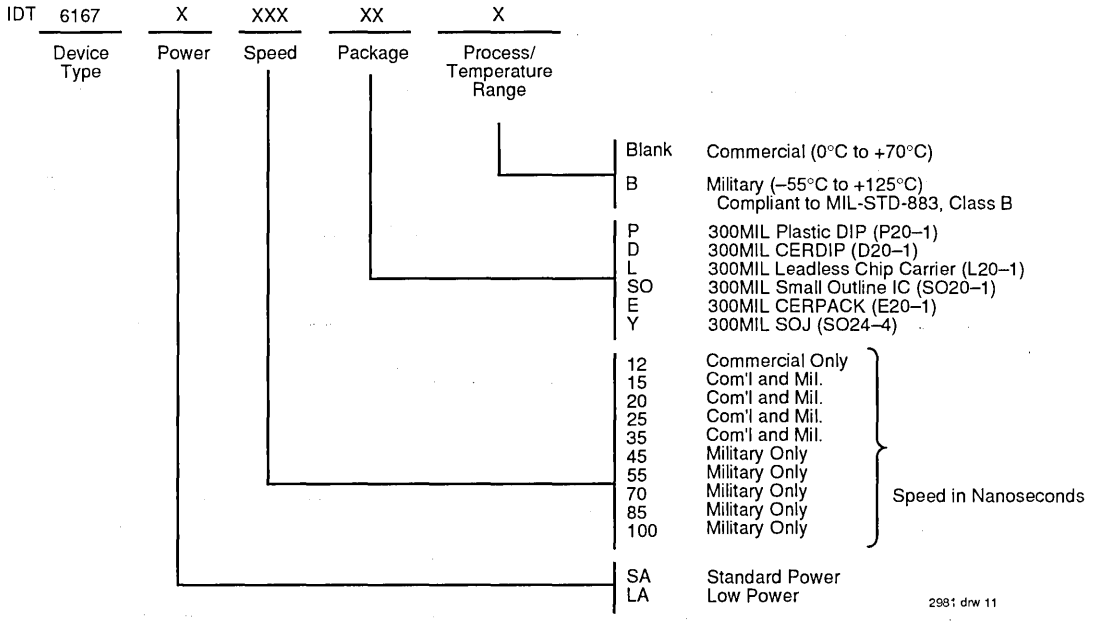


TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 4)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be inactive during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in the high-impedance state.
5. Transition is measured ±200mV from steady state.
6. During this period, the I/O pins are in the output state and the input signals must not be applied.

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS STATIC RAM 16K (4K x 4-BIT)

IDT6168SA
IDT6168LA

FEATURES:

- High-speed (equal access and cycle time)
  - — Military: 12/15/20/25/35/45/55/70/85/100ns (max.)
  - — Commercial: 10/12/15/20/25/35ns (max.)
- Low power consumption
- Battery backup operation—2V data retention voltage (IDT6168LA only)
- Available in high-density 20-pin ceramic or plastic DIP, 20-pin SOIC, 20-pin SOJ, 20-pin CERPACK and 20-pin leadless chip carrier
- Produced with advanced CMOS high-performance technology
- CMOS process virtually eliminates alpha particle soft-error rates
- Bidirectional data input and output
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT6168 is a 16,384-bit high-speed static RAM organized as 4K x 4. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective approach for high-speed memory applications.

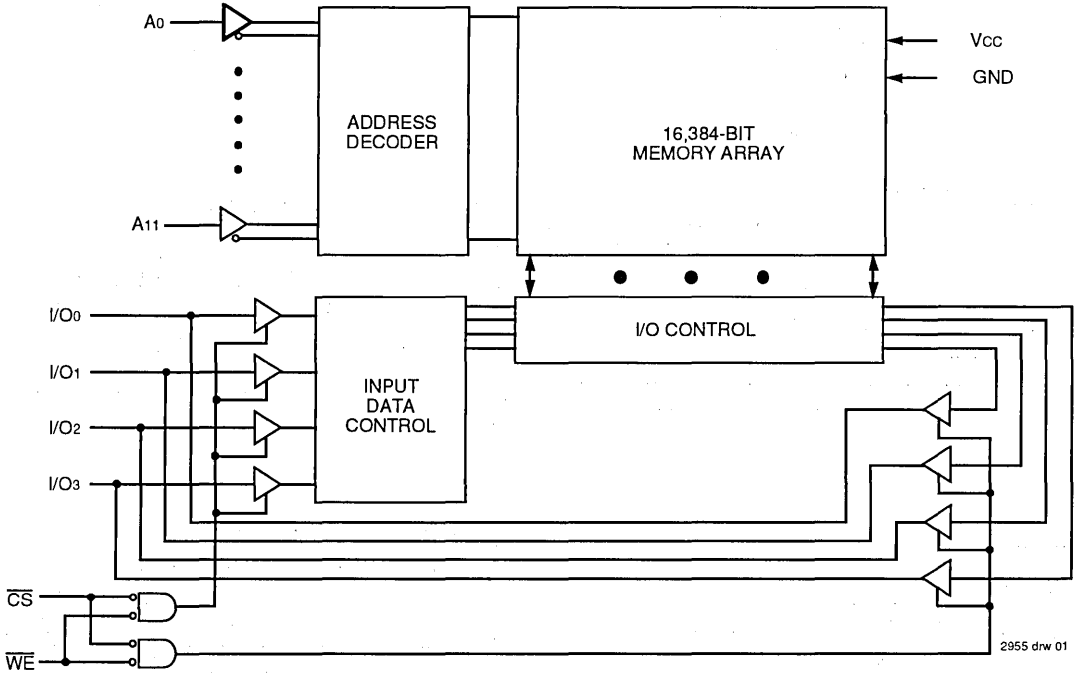
Access times as fast 10ns are available. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes HIGH, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{CS}$ remains HIGH. This capability provides significant system-level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1µW operating off a 2V battery. All inputs and outputs of the IDT6168 are TTL-compatible and operate from a single 5V supply.

The IDT6168 is packaged in either a space saving 20-pin, 300 mil ceramic or plastic DIP, 20-pin CERPACK, 20-pin SOIC, 20-pin SOJ, or 20-pin leadless chip carrier, providing high board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

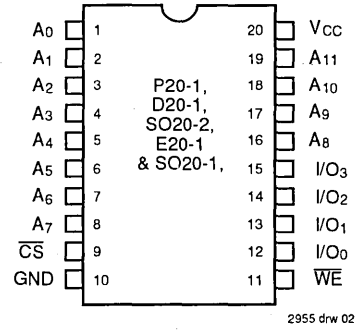
5

FUNCTIONAL BLOCK DIAGRAM

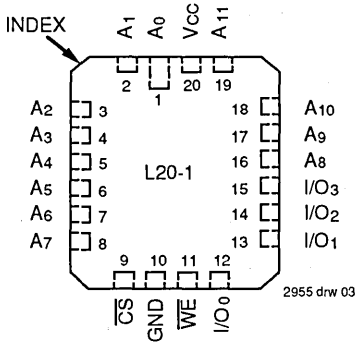


The IDT logo is a registered trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP/SOIC/SOJ/CERPACK
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A0–A11	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
I/O0-3	Data Input/Output
Vcc	Power
GND	Ground

2955 tbl 01

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	7	pF
COUT	Output Capacitance	VOUT = 0V	7	pF

NOTE: 2955 tbl 04
1. This parameter is determined by device characterization, but is not production tested.

TRUTH TABLE[1]

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High-Z	Standby
Read	L	H	DOUT	Active
Write	L	L	DIN	Active

NOTE: 2955 tbl 02
1. H = VIH, L = VIL, X = Don't Care

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

NOTE: 2955 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input HIGH Voltage	2.2	—	6.0	V
VIL	Input LOW Voltage	–0.5[1]	—	0.8	V

NOTE: 2955 tbl 05
1. VIL (min.) = –3.0V for pulse width less than 20ns, once per cycle.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	VCC
Military	–55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2955 tbl 06

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	6168SA10 Com'l.	6168SA10 Mil.	6168SA12[4] Com'l.	6168SA12[4] Mil.	6168SA15[4] Com'l.	6168SA15[4] Mil.	6168SA20 6168LA20 Com'l.	6168SA20 6168LA20 Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = 0[3]	SA	120	—	110	120	110	120	90	100	mA
		LA	—	—	—	—	—	—	70	80	
I_{CC2}	Dynamic Operating Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[3]	SA	175	—	165	175	145	165	120	120	mA
		LA	—	—	—	—	—	—	100	110	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \ge V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}[3]	SA	65	—	65	65	55	60	45	45	mA
		LA	—	—	—	—	—	—	30	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \ge V_{HC}$, V_{CC} = Max., $V_{IN} \ge V_{HC}$ or $V_{IN} \le V_{LC}$, f = 0[3]	SA	20	—	20	20	20	20	20	20	mA
		LA	—	—	—	—	—	—	0.5	5	

DC ELECTRICAL CHARACTERISTICS (CONTINUED)[1]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	6168SA25 6168LA25 Com'l.	6168SA25 6168LA25 Mil.	6168SA35 6168LA35 Com'l.	6168SA35 6168LA35 Mil.	6168SA45/55 6168LA45/55 Com'l.	6168SA45/55 6168LA45/55 Mil.	6168SA70[2] 6168LA70[2] Com'l.	6168SA70[2] 6168LA70[2] Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = 0[3]	SA	90	100	90	100	—	100	—	100	mA
		LA	70	80	70	80	—	80	—	80	
I_{CC2}	Dynamic Operating Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[3]	SA	110	120	100	110	—	110	—	110	mA
		LA	90	100	80	90	—	80	—	80	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \ge V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}[3]	SA	35	45	30	35	—	35	—	35	mA
		LA	25	30	20	25	—	25/20	—	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \ge V_{HC}$, V_{CC} = Max., $V_{IN} \ge V_{HC}$ or $V_{IN} \le V_{LC}$, f = 0[3]	SA	3	10	3	10	—	10	—	10	mA
		LA	0.5	0.3	0.5	0.3	—	0.3	—	0.3	

NOTES:
1. All values are maximum guaranteed values.
2. Also available 85 and 100ns military devices.
3. f_{MAX} = 1/t_{RC}, only address inputs are cycling at f_{MAX}. f = 0 means no address inputs are changing.
4. Military values are preliminary only.

2955 tbl 07

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Condition		IDT6168SA Min.	IDT6168SA Max.	IDT6168LA Min.	IDT6168LA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL	—	10	—	5	µA
			COM'L	—	2	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL	—	10	—	5	µA
			COM'L	—	2	—	2	
V_{OL}	Output LOW Voltage	I_{OL} = 10mA, V_{CC} = Min.		—	0.5	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	
V_{OH}	Output HIGH Voltage	I_{OL} = –4mA, V_{CC} = Min.		2.4	—	2.4	—	V

2955 tbl 08

DATA RETENTION CHARACTERISTICS (LA Version Only)

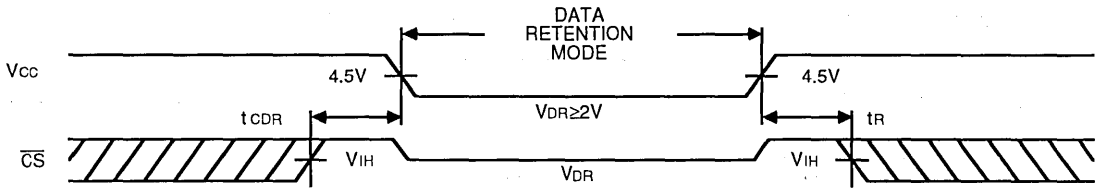
V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Condition		IDT6168LA Min.	IDT6168LA Typ.(1)	IDT6168LA Max.	Unit
V_{DR}	Vcc for Data Retention			2.0	—	—	V
I_{CCDR}	Data Retention Current		MIL.	—	0.5(2)	100(2)	µA
		$\overline{CS} \geq V_{HC}$	—	1.0(3)	150(3)		
		$V_{IN} \geq V_{HC}$	COM'L.	—	0.5(2)	20(2)	µA
		or $\leq V_{LC}$		—	1.0(3)	30(3)	
t_{CDR}(5)	Chip Deselect to Data Retention Time			0	—	—	ns
t_R(5)	Operation Recovery Time			t_{RC}(2)	—	—	ns

2955 tbl 09

NOTES:
1. T_A = +25°C.
2. at V_{CC} = 2V
3. at V_{CC} = 3V
4. t_{RC} = Read Cycle Time.
5. This parameter is guaranteed by device characterization, but is not production tested.

LOW Vcc DATA RETENTION WAVEFORM



2955 drw 04

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2955 tbl 10

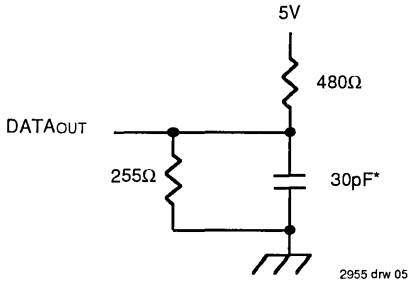


Figure 1. AC Test Load

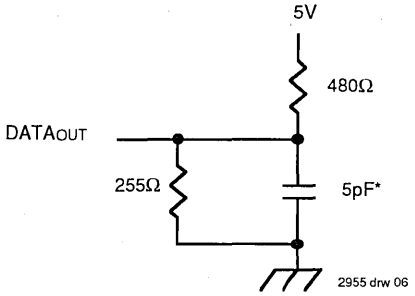


Figure 2. AC Test Load
(for tCHZ, tCLZ, tWHZ and tOW)

*Includes scope and jig capacitances

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6168SA10(1) Min.	6168SA10(1) Max.	6168SA12 Min.	6168SA12 Max.	6168SA15 Min.	6168SA15 Max.	6168SA20/25 6168LA20/25 Min.	6168SA20/25 6168LA20/25 Max.	Unit
Read Cycle										
tRC	Read Cycle Time	10	—	12	—	15	—	20/25	—	ns
tAA	Address Access Time	—	10	—	12	—	15	—	20/25	ns
tACS	Chip Select Access Time	—	10	—	12	—	15	—	20/25	ns
tCLZ	Chip Select to Output in Low-Z(3)	3	—	3	—	3	—	5	—	ns
tCHZ	Chip Deselect to Output in High-Z(3)	—	6	—	7	—	8	—	10	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
tPU	Chip Select to Power-Up Time(3)	0	—	0	—	0	—	0	—	ns
tPD	Chip Deselect to Power-Down Time(3)	—	10	—	12	—	15	—	20/25	ns

2955 drw 11

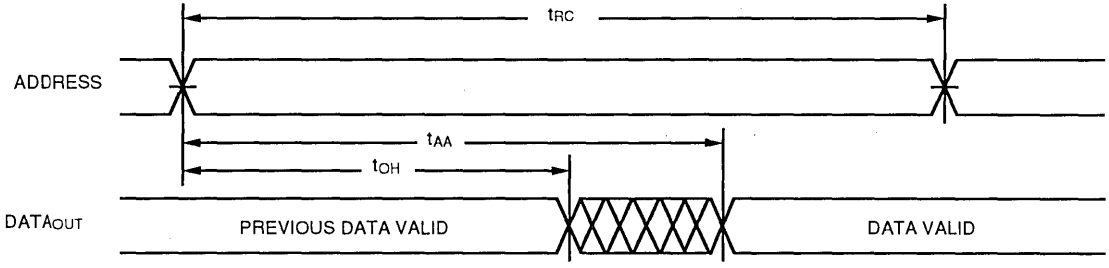
AC ELECTRICAL CHARACTERISTICS (CONTINUED) (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6168SA35 6168LA35 Min.	6168SA35 6168LA35 Max.	6168SA45(2) 6168LA45(2) Min.	6168SA45(2) 6168LA45(2) Max.	6168SA55(2) 6168LA55(2) Min.	6168SA55(2) 6168LA55(2) Max.	6168SA70(2) 6168LA70(2) Min.	6168SA70(2) 6168LA70(2) Max.	Unit
Read Cycle										
tRC	Read Cycle Time	35	—	45	—	55	—	70	—	ns
tAA	Address Access Time	—	35	—	45	—	55	—	70	ns
tACS	Chip Select Access Time	—	35	—	45	—	55	—	70	ns
tCLZ	Chip Select to Output in Low-Z(3)	5	—	5	—	5	—	5	—	ns
tCHZ	Chip Deselect to Output in High-Z(3)	—	15	—	25	—	25	—	30	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
tPU	Chip Select to Power-Up Time(3)	0	—	0	—	0	—	0	—	ns
tPD	Chip Deselect to Power-Down Time(3)	—	35	—	40	—	50	—	60	ns

2955 tbl 12

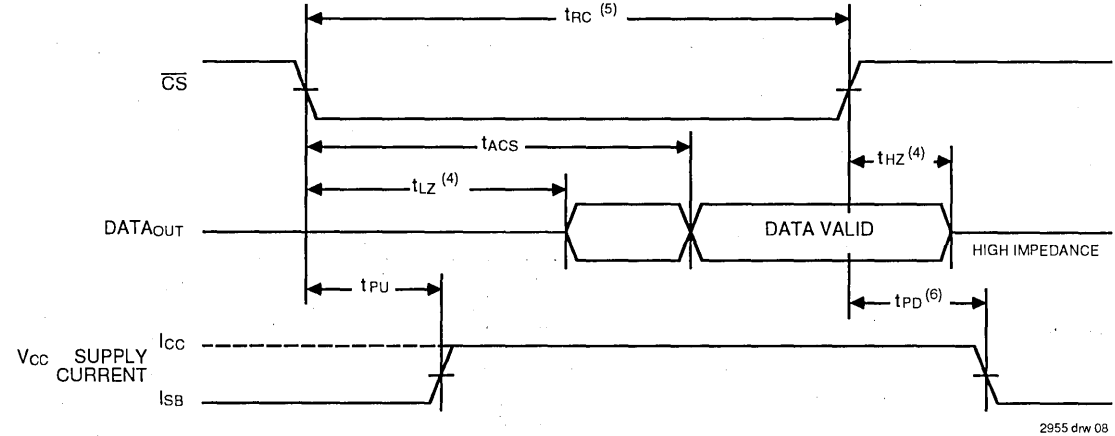
NOTES:
1. 0° to +70°C temperature range only.
2. –55°C to +125°C temperature range only. Also available 85ns and 100ns devices.
3. This parameter is guaranteed with AC Test load (Figure 2) by device characterization, but is not production tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1, 2)



2955 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 3)



2955 drw 08

NOTES:
1. $\overline{WE}$ is HIGH for read cycle.
2. $\overline{CS}$ is LOW for read cycle.
3. Device is continuously selected, $\overline{CS} \leq V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. Transition is measured ±200mV from steady state.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6168SA10[1] Min.	6168SA10[1] Max.	6168SA12 Min.	6168SA12 Max.	6168SA15 Min.	6168SA15 Max.	6168SA20/25 6168LA20/25 Min.	6168SA20/25 6168LA20/25 Max.	Unit
Write Cycle										
tWC	Write Cycle Time	10	—	12	—	15	—	20	—	ns
tCW	Chip Select to End-of-Write	10	—	12	—	15	—	20	—	ns
tAW	Address Valid to End-of-Write	10	—	12	—	15	—	20	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	10	—	12	—	15	—	20	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	7	—	8	—	9	—	10	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tWHZ	Write Enable to Output in High-Z[3]	—	4	—	5	—	6	—	7	ns
tOW	Output Active from End-of-Write[3]	0	—	0	—	0	—	0	—	ns

2955 tbl 13

AC ELECTRICAL CHARACTERISTICS (CONTINUED) (Vcc = 5.0V ± 10%, All Temperature Ranges)

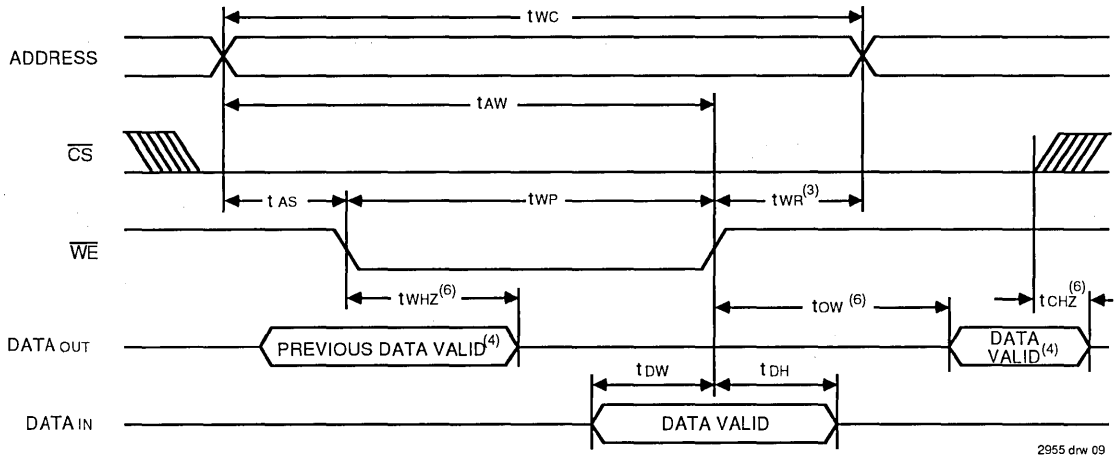
Symbol	Parameter	6168SA35 6168LA35 Min.	6168SA35 6168LA35 Max.	6168SA45[2] 6168LA45[2] Min.	6168SA45[2] 6168LA45[2] Max.	6168SA55[2] 6168LA55[2] Min.	6168SA55[2] 6168LA55[2] Max.	6168SA70[2] 6168LA70[2] Min.	6168SA70[2] 6168LA70[2] Max.	Unit
Write Cycle										
tWC	Write Cycle Time	30	—	40	—	50	—	60	—	ns
tCW	Chip Select to End-of-Write	30	—	40	—	50	—	60	—	ns
tAW	Address Valid to End-of-Write	30	—	40	—	50	—	60	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	30	—	40	—	50	—	60	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tDW	DataValid to End-of-Write	15	—	20	—	20	—	25	—	ns
tDH	Data Hold Time	0	—	3	—	3	—	3	—	ns
tWHZ	Write Enable to Output in High-Z[3]	—	13	—	20	—	25	—	30	ns
tOW	Output Active from End-of-Write[3]	0	—	0	—	0	—	0	—	ns

NOTES:
1. 0° to +70°C temperature range only.
2. –55°C to +125°C temperature range only. Also available 85ns and 100ns devices.
3. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

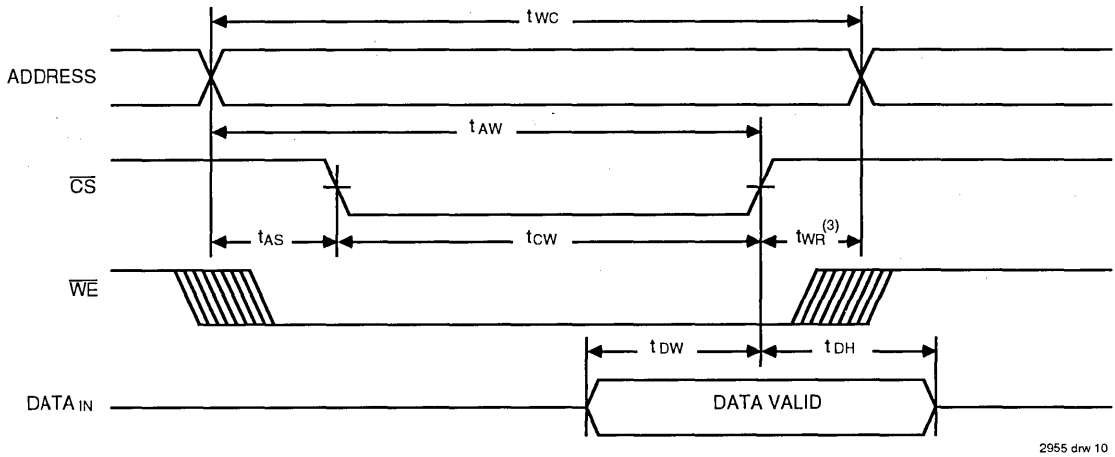
2955 tbl 14

5

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 5)

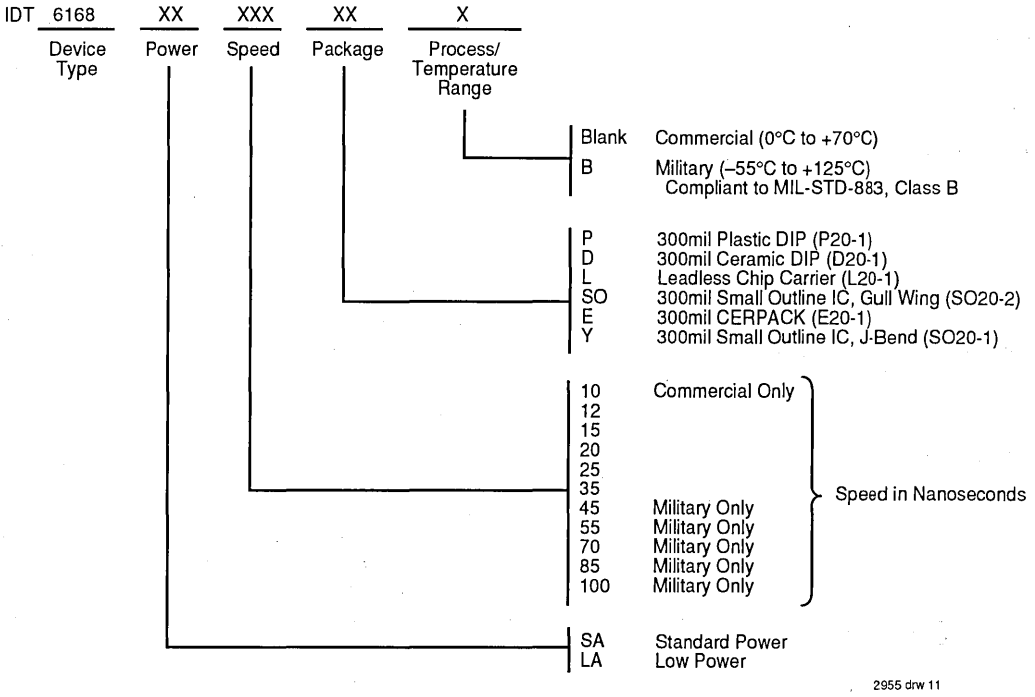


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals should not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200mV from steady state.

ORDERING INFORMATION



5

Integrated Device Technology, Inc.

CMOS STATIC RAM WITH OUTPUT ENABLE 16K (4K x 4-BIT)

IDT61970S
IDT61970L

FEATURES:

- High Speed (equal Access and Cycle Times)
  - Military: 12/15/20/25/35/45/55
  - Commercial: 10/12/15/20/25/35/45
- Fast Output Enable
- Low power consumption
- Battery backup operation—2V data retention (IDT61970L only)
- Available in 22-pin ceramic or plastic DIP and 24-pin SOJ
- Produced with advanced CMOS high-performance technology
- Separate Output Enable control
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT61970 is a 16,384-bit high-speed static RAM organized as 4096 x 4 bits. It is fabricated using IDT's high-performance, high-reliability CMOS technology.

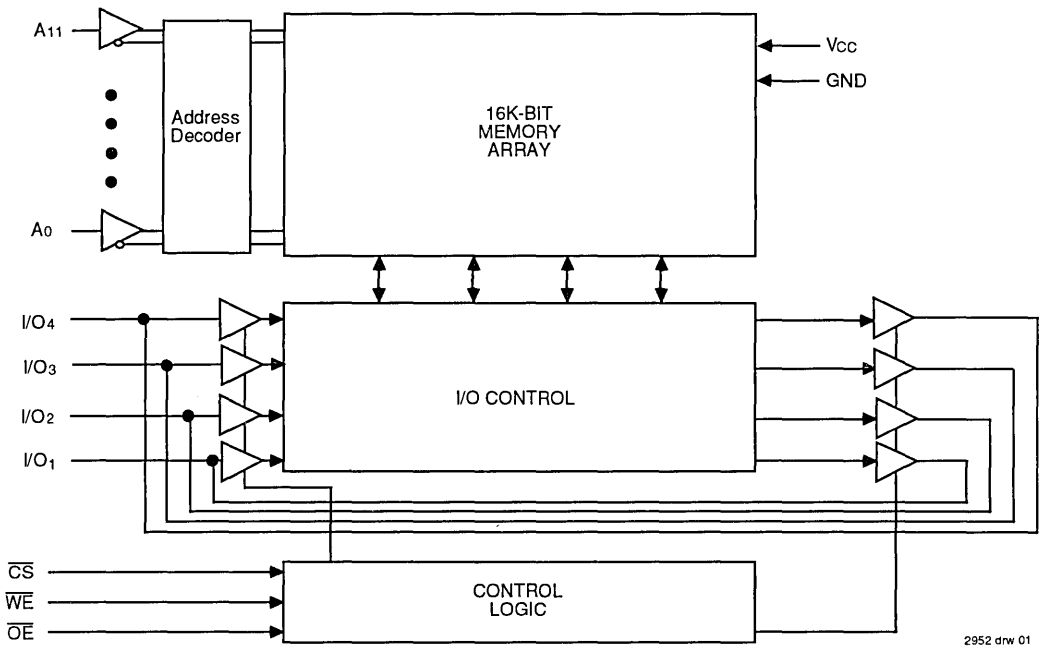
The IDT61970 features two memory control functions: Chip Select ($\overline{CS}$) and Output Enable ($\overline{OE}$). These two functions greatly enhance the IDT61970s overall flexibility in high-speed memory applications. This feature makes the IDT61970 ideal for use in cache memory applications.

Access times as fast as 10ns and t_{OE} as fast as 5ns are available. The IDT61970 offers a reduced power standby mode which enables the designer to considerably reduce device power requirements. This capability significantly decreases system power and cooling levels, while greatly enhancing system reliability. The low power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 10µW when operating from a 2V battery. All inputs and output are TTL-compatible and operate from a single 5V supply.

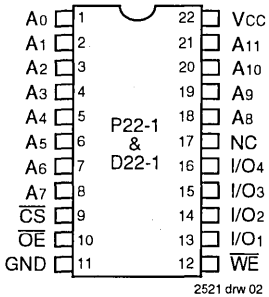
The IDT61970 is packaged in either a space saving 22-pin, 300-mil ceramic or plastic DIP, or a 24-pin SOJ, providing high board level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

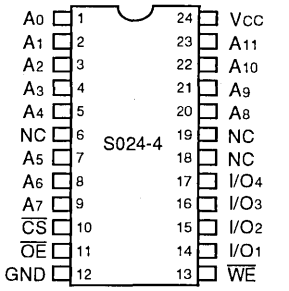
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP
TOP VIEW



SOJ
TOP VIEW
2952 drw 03

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA	Operating Temperature	–55 to +125	°C
TBIAS	Temperature Under Bias	–65 to +135	°C
TSTG	Storage Temperature	–65 to +150	°C
PT	Power Dissipation	1.0	W
IOUT	DC Output Current	50	mA

NOTE: 2952 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

PIN NAMES

A0 – A11	Address	$\overline{WE}$	Write Enable
I/O1 – I/O4	Data Input/Output	$\overline{OE}$	Output Enable
VCC	Power	$\overline{CS}$	Chip Select
GND	Ground	NC	No Connection

2952 tbl 01

5

TRUTH TABLE(1)

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Standby	H	X	X	High-Z	Standby
Read	L	H	L	DATAOUT	Active
Write	L	L	X	DATAIN	Active
Read	L	H	H	High-Z	Active

NOTE: 2952 tbl 08

1. H = VIH, L = VIL, X = Don't Care.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition		61970S Min.	61970S Max.	61970L Min.	61970L Max.	Unit
|ILI|	Input Leakage Current	VCC = Max.	Mil.	—	10	—	5	µA
		VIN = GND to VCC	Com'l.	—	2	—	2	
|ILO|	Output Leakage Current	VCC = Max., $\overline{CS}$ = VIH,	Mil.	—	10	—	5	µA
		VCC = GND to VCC	Com'l.	—	2	—	2	
VOL	Output Low Voltage	IOL = 10mA, VCC = Min.		—	0.5	—	0.5	V
		IOL = 8mA, VCC = Min.		—	0.4	—	0.4	V
VOH	Output High Voltage	IOH = –4mA, VCC = Min.		2.4	—	2.4	—	V

2952 tbl 03

CAPACITANCE (TA = +25°C, f = 1MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

NOTE:

1. This parameter is determined by device characterization, but is not production tested

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	–	6.0	V
VIL	Input Low Voltage	–0.5(1)	–	0.8	V

NOTE: 2952 tbl 05

1. VIL (min.) = –3.0V for pulse width less than 20ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS[1] $V_{CC} = 5.0V \pm 10\%$, $V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Power	61970S10 Com'l.	61970S10 Mil.	61970S12[4] Com'l.	61970S12[4] Mil.	61970S15 Com'l.	61970S15 Mil.	61970S20 61970L20 Com'l.	61970S20 61970L20 Mil.	61970S25 61970L25 Com'l.	61970S25 61970L25 Mil.	61970S35 61970L35 Com'l.	61970S35 61970L35 Mil.	61970S45/55[3] 61970L45/55[3] Com'l.	61970S45/55[3] 61970L45/55[3] Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS} = V_{IL}$, Outputs Open, V_{CC} = Max., f = 0[2]	S	120	—	110	120	110	120	90	100	90	100	90	100	—	100	mA
		L	—	—	—	—	—	—	70	80	70	80	70	80	—	80	
I_{CC2}	Dynamic Operating Current, $\overline{CS} = V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	S	175	—	165	175	145	165	120	120	110	120	100	110	—	110	mA
		L	—	—	—	—	—	—	100	110	90	100	80	90/80	—	80	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}[2]	S	65	—	65	65	55	60	45	45	35	45	30	35	—	35	mA
		L	—	—	—	—	—	—	30	35	25	30	20	25	—	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, V_{CC} = Max., $V_{IN} \geq V_{HC}$ or $V_{IN} \leq V_{LC}$, f = 0[2]	S	20	—	20	20	20	20	20	20	3	10	3	10	—	10	mA
		L	—	—	—	—	—	—	0.5	5	0.5	0.3	0.5	0.3	—	0.3	

NOTES:
1. All values are maximum guaranteed values.
2. $f_{MAX} = 1/t_{RC}$, only address inputs are cycling at f_{MAX}. f = 0 means no address inputs are changing.
3. –55°C to +125°C temperature range only.
4. Military values are preliminary only.

2952 tbl 04

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55° to +125°C	0V	5.0V ±10%
Commercial	0°C to +70°C	0V	5.0V ±10%

2952 tbl 09

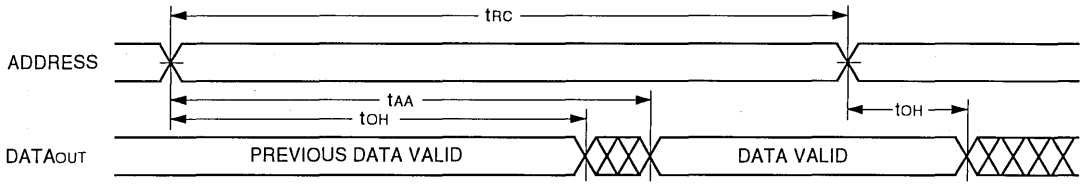
AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	61970S10 Min.	61970S10 Max.	61970S12[2] Min.	61970S12[2] Max.	61970S15 Min.	61970S15 Max.	61970S20/25 61970L20/25 Min.	61970S20/25 61970L20/25 Max.	61970S35/45 61970L35/45 Min.	61970S35/45 61970L35/45 Max.	61970S55 61970L55 Min.	61970S55 61970L55 Max.	Unit
Read Cycle														
t_{RC}	Read Cycle Time	10	—	12	—	15	—	20/25	—	35/45	—	55	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	—	20/25	—	35/45	—	55	ns
t_{OE}	Output Enable Access Time	—	5	—	5	—	6	—	8/10	—	12/15	—	20	ns
t_{OLZ}	Output Low-Z Time[1]	2	—	2	—	2	—	2	—	2	—	2	—	ns
t_{OHZ}	Output High-Z Time[1]	—	6	—	7	—	9	—	12	—	15	—	15	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	3	—	ns
t_{ACS}	Chip Select Access Time	10	—	12	—	15	—	20/25	—	35/45	—	55	—	ns
t_{CLZ}	Chip Select to Output in Low-Z[1]	3	—	3	—	3	—	3	—	3	—	3	—	ns
t_{CHZ}	Chip Deselect to Output in High-Z[1]	—	6	—	7	—	8	—	10	—	15	—	25	ns
t_{PU}	Chip Select to Power-up Time[1]	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Deselect Power-down Time[1]	—	10	—	12	—	15	—	20/25	—	35/45	—	55	ns

NOTE:
1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.
2. Military values are preliminary only.

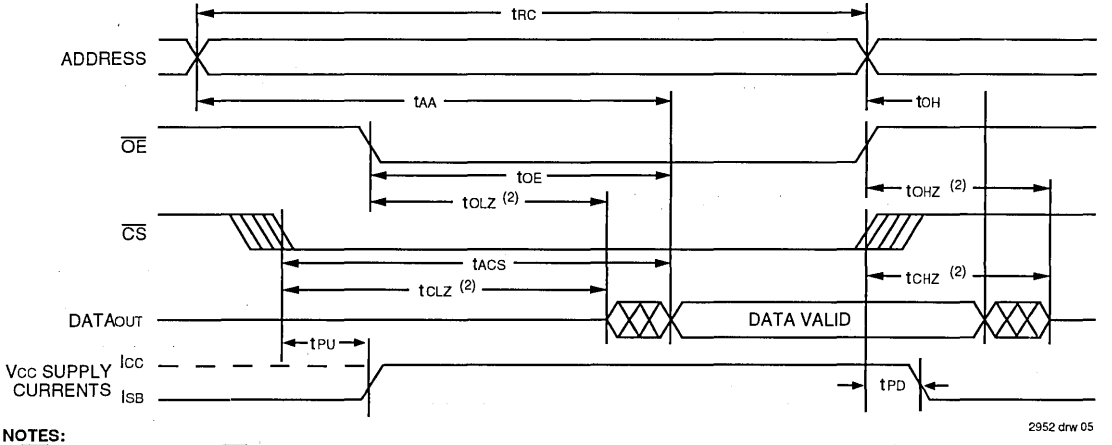
2952 tbl 06

TIMING WAVEFORM OF READ CYCLE NO. 1[1,4]



2952 drw 04

TIMING WAVEFORM OF READ CYCLE NO. 2[1,3]



2952 drw 05

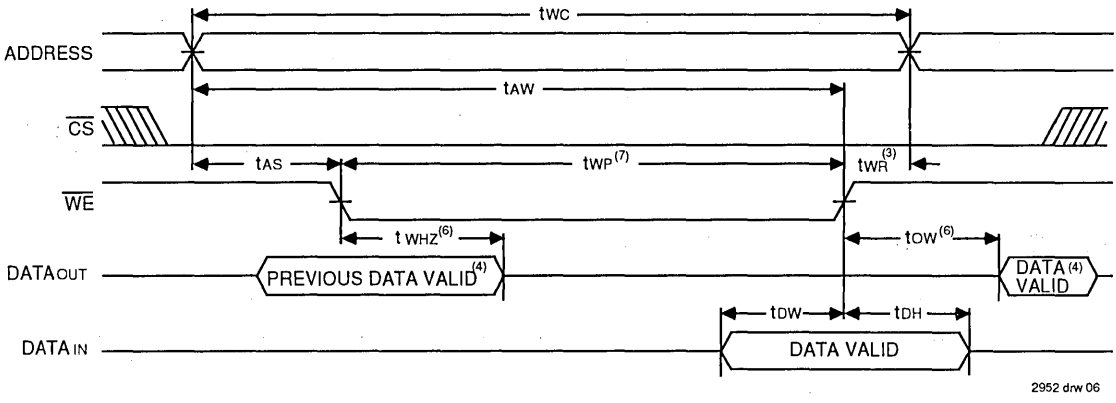
NOTES:
1. $\overline{WE}$ is HIGH for read cycle, $\overline{WE} \geq V_{IH}$.
2. Transition is measured ±200mV from steady state.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. Device is continuously selected, $\overline{CS} \leq V_{IL}$.

AC ELECTRICAL CHARACTERISTICS

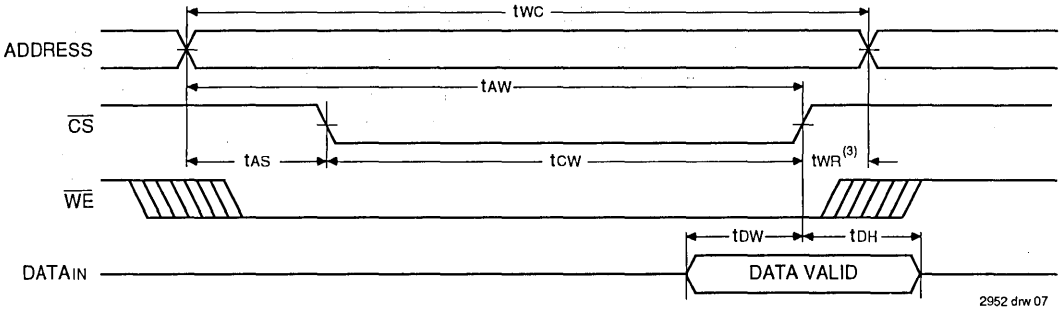
Symbol	Parameter	61970S10		61970S12[3]		61970S15		61970S20/25 61970L20/25		61970S35/45 61970L35/45		61970S55 61970L55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle														
tWC	Write Cycle Time	10	—	12	—	15	—	20/25	—	35/45	—	55	—	ns
tAW	Address Valid to End of Write	8	—	10	—	12	—	15/20	—	25/30	—	35	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	8	—	8	—	10	—	12/15	—	20/25	—	30	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	7	—	8	—	9	—	10/13	—	17/20	—	20	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWHZ	Write Enable to Output in High-Z[1,2]	—	5	—	6	—	7	—	9	—	13/20	—	25	ns
tOW	Output Active From End of Write[1,2]	0	—	0	—	0	—	0	—	0	—	0	—	ns
tCW	Chip Select to End of Write	8	—	10	—	12	—	15/20	—	25/30	—	35	—	ns

NOTES:
2952 tbl 07
1. Transition is measured ±200mV from steady state.
2. This parameter is guaranteed with the AC load (Figure 2) by device characterization, but is not production tested.
3. Military values are preliminary only.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ Controlled Timing)(1, 2, 5, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ Controlled Timing)(1, 2, 5, 7)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals should not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in the high-impedance state.
6. Transition is measured ±200mV from steady state.
7. $\overline{OE}$ is continuously HIGH. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP. For a $\overline{CS}$ controlled write cycle, $\overline{OE}$ may be LOW with no degradation to tCW.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

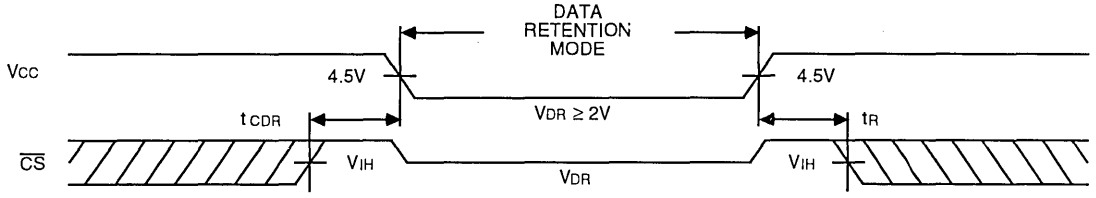
Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention			2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$	MIL.	— —	0.5[2] 1.0[3]	100[2] 150[3]	µA
		$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	COM'L.	— —	0.5[2] 1.0[3]	20[2] 30[3]	µA
t_{CDR}[4]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[4]	Operation Recovery Time			t_{RC}[2]	—	—	ns

NOTES:

2952 tbl 10

1. T_A = +25°C.
2. at V_{CC} = 2V
3. at V_{CC} = 3V
4. This parameter is guaranteed by device characterization, but is not production tested.

LOW V_{CC} DATA RETENTION WAVEFORM



2952 drw 08

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2952 tbl 11

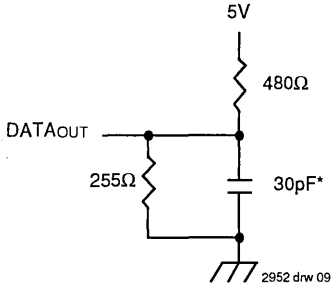


Figure 1. AC Test Load

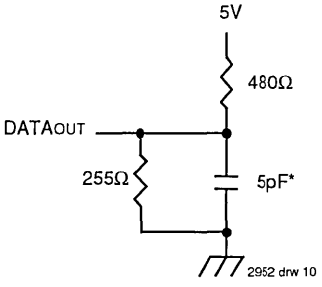
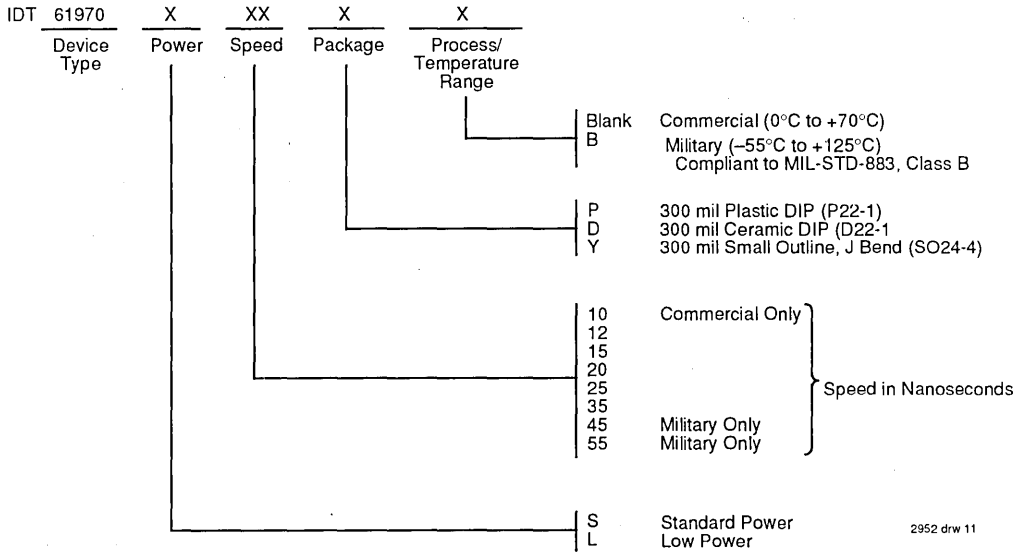


Figure 2. AC Test Load
(for t_{OLZ}, t_{CLZ}, t_{OHZ}, t_{CHZ}, t_{OW} & t_{WZ})

* Including scope and jig.

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS STATIC RAMS 16K (4K x 4-BIT) Separate Data Inputs and Outputs

IDT71681SA/LA
IDT71682SA/LA

FEATURES:

- Separate data inputs and outputs
- IDT71681SA/LA: outputs track inputs during write mode
- IDT71682SA/LA: high impedance outputs during write mode
- High speed (equal access and cycle time)
  - — Military: 12/15/20/25/35/45/55/70/85/100ns (max.)
  - — Commercial: 10/12/15/20/25/35/45ns (max.)
- Low power consumption
- Battery backup operation—2V data retention (LA version only)
- High-density 24-pin 300-mil Ceramic or Plastic DIP, 24-pin CERPACK, 24-pin SOIC, 24-pin SOJ and 28-pin leadless chip carrier
- Produced with advanced CMOS high-performance technology
- CMOS process virtually eliminates alpha particle soft-error rates
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

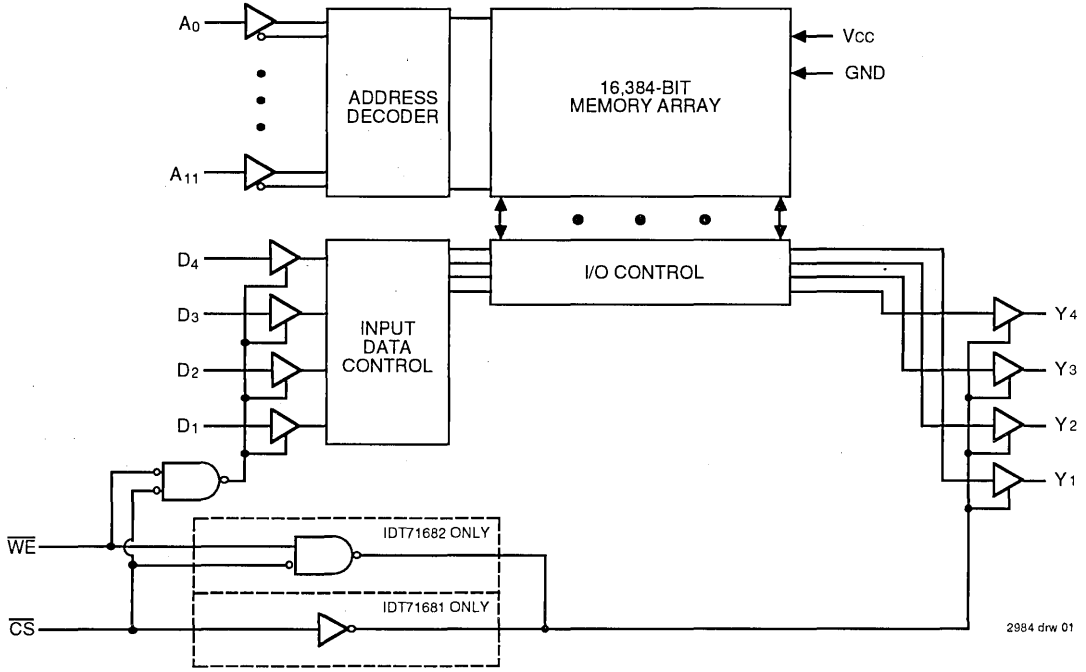
The IDT71681/IDT71682 are 16,384-bit high-speed static RAMs organized as 4K x 4. They are fabricated using IDT's high-performance, high-reliability technology—CMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for high-speed memory applications.

Access times as fast as 10ns are available. These circuits also offer a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, this standby mode as long as $\overline{CS}$ remains high. In the standby mode , the devices consume less than 10μW, typically. This capability provides significant system-level power and cooling savings. The low-power (LA) versions also offer a battery backup data retention capability where the circuit typically consumes only 1μW operating off a 2V battery.

All inputs and outputs of the IDT71681/IDT71682 are TTL-compatible and operate from a single 5V supply.

5

FUNCTIONAL BLOCK DIAGRAM

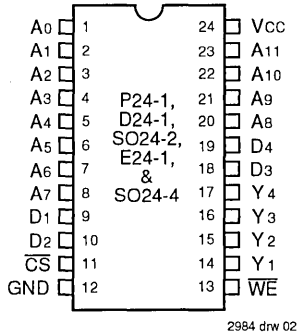


DESCRIPTION (Continued):

The IDT71681/IDT71682 are packaged in either space-saving 24-pin, 300-mil DIPs, SOICs, SOJs, CERPACKS, or 28-pin leadless chip carriers.

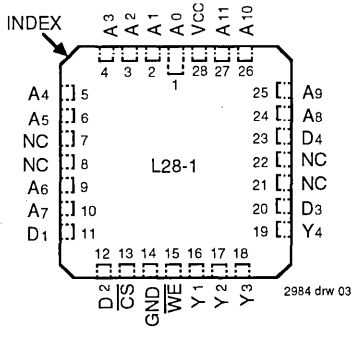
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS



2984 drw 02

DIP/SOIC/SOJ/CERPACK TOP VIEW



2984 drw 03

LCC TOP VIEW

PIN DESCRIPTIONS

Name	Description
A0 – A11	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
D1 – D4	DATAIN
Y1 – Y4	DATAOUT
VCC	Power
GND	Ground

2984 tbl 01

TRUTH TABLE[3]

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High-Z	Standby
Read	L	H	DATAOUT	Active
Write[1]	L	L	DATAIN	Active
Write[2]	L	L	High-Z	Active

NOTES: 2984 tbl 02

1. For IDT71681 only.
2. For IDT71682 only.
3. H = VIH, L = VIL, X = don't care.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

NOTE: 2984 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

NOTE: 2984 tbl 04

1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2984 tbl 05

1. V_{IL} (min.) = –3.0V for pulse width less than 20ns, once per cycle.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2984 tbl 06

DATA RETENTION CHARACTERISTICS

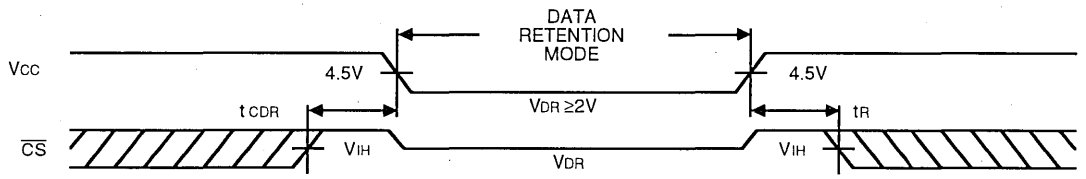
(LA Version Only; V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

Symbol	Parameter	Test Condition		IDT71681/2LA Min.	IDT71681/2LA Typ.(1)	IDT71681/2LA Max.	Unit
V_{DR}	Vcc for Data Retention			2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$	MIL.	— —	0.5(2) 1.0(3)	100(2) 150(3)	µA
		$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	COM'L.	— —	0.5(2) 1.0(3)	20(2) 30(3)	µA
t_{CDR}(5)	Chip Deselect to Data Retention Time			0	—	—	ns
t_R(5)	Operation Recovery Time			t_{RC}(4)	—	—	ns

NOTES: 2984 tbl 07

1. T_A = +25°C.
2. At V_{CC} = 2V
3. At V_{CC} = 3V
4. t_{RC} = Read Cycle Time.
5. This parameter is guaranteed by device characterization, but is not production tested.

LOW Vcc DATA RETENTION WAVEFORM



2984 drw 04

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT71681/2S Min.	IDT71681/2S Typ.	IDT71681/2S Max.	IDT71681/2L Min.	IDT71681/2L Typ.	IDT71681/2L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL. COM'L.	— —	— —	10 5	— —	— —	5 2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL. COM'L.	— —	— —	10 5	— —	— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.			—	0.5	—	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	—	0.4	—	—	0.4	
V_{OH}	Output High Voltage	I_{OL} = –4mA, V_{CC} = Min.		2.4	—	—	2.4	—	—	V

2984 tbl 08

DC ELECTRICAL CHARACTERISTICS[1,7]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	71681x10[5] 71682x10[5] Com'l.	71681x10[5] 71682x10[5] Mil.	71681x12[4] 71682x12[4] Com'l.	71681x12[4] 71682x12[4] Mil.	71681x15 71682x15 Com'l.	71681x15 71682x15 Mil.	71681x20 71682x20 Com'l.	71681x20 71682x20 Mil.	71681x25 71682x25 Com'l.	71681x25 71682x25 Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = 0[3]	SA	120	—	110	120	110	120	90	100	90	100	mA
		LA	—	—	—	—	—	—	70	80	70	80	
I_{CC2}	Dynamic Operating Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[3]	SA	175	—	165	175	145	165	120	120	110	120	mA
		LA	—	—	—	—	—	—	100	110	90	100	
I_{SB}	Standby Power SupplyCurrent (TTL Level) $\overline{CS} \ge V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}[3]	SA	65	—	65	65	55	65	45	55	35	45	mA
		LA	—	—	—	—	—	—	30	35	25	30	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \ge V_{HC}$, V_{CC} = Max., $V_{IN} \ge V_{HC}$ or $V_{IN} \le V_{LC}$, f = 0[3]	SA	20	—	20	20	20	20	20	20	3	10	mA
		LA	—	—	—	—	—	—	0.5	5	0.5	0.3	

DC ELECTRICAL CHARACTERISTICS (Continued)[1,7]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

Symbol	Parameter	Power	71681x35 71682x35 Com'l.	71681x35 71682x35 Mil.	71681x45 71682x45 Com'l.	71681x45 71682x45 Mil.	71681x55[6] 71682x55[6] Com'l.	71681x55[6] 71682x55[6] Mil.	71681x70[2,6] 71682x70[2,6] Com'l.	71681x70[2,6] 71682x70[2,6] Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = 0[3]	SA	90	100	90	100	—	100	—	100	mA
		LA	70	80	70	80	—	80	—	80	
I_{CC2}	Dynamic Operating Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[3]	SA	100	110	100	110	—	110	—	110	mA
		LA	80	90	70	80	—	80	—	80	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \ge V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}[3]	SA	30	35	30	35	—	35	—	35	mA
		LA	20	25	20	25	—	20	—	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \ge V_{HC}$, V_{CC} = Max., $V_{IN} \ge V_{HC}$ or $V_{IN} \le V_{LC}$, f = 0[3]	SA	3	10	3	10	—	10	—	10	mA
		LA	0.5	0.3	0.5	0.3	—	0.3	—	0.3	

NOTES:

2984 tbl 09

1. All values are maximum guaranteed values.
2. Also available 85 and 100ns military devices.
3. f_{MAX} = 1/tRC, only address inputs are cycling at fMAX. f = 0 means no address inputs are changing.
4. Military values for 12ns device are preliminary only.
5. 0°C to +70°C temperature range only.
6. –55°C to +125°C temperature range only.
7. "x" in part numbers indicates power rating (SA or LA).

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2984 tbl 10

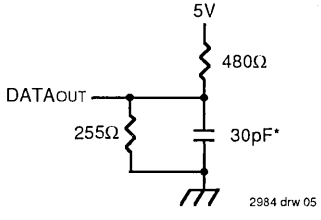


Figure 1. AC Test Load

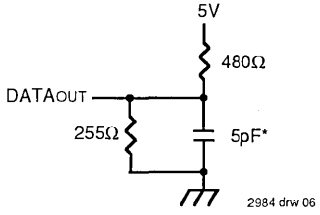


Figure 2. AC Test Load (for tCLZ, tCHZ, tWHZ, and tOW)

*Includes scope and jig capacitances

AC ELECTRICAL CHARACTERISTICS[4] (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71681x10[1] 71682x10[1] Min.	Max.	71681x12 71682x12 Min.	Max.	71681x15 71682x15 Min.	Max.	71681x20 71682x20 Min.	Max.	71681x25 71682x25 Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	10	—	12	—	15	—	20	—	25	—	ns
tAA	Address Access Time	—	10	—	12	—	15	—	20	—	25	ns
tACS	Chip Select Access Time	—	10	—	12	—	15	—	20	—	25	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	ns
tCLZ	Chip Select to Output in Low-Z[3]	3	—	3	—	5	—	5	—	5	—	ns
tCHZ	Chip Select to Output in High-Z[3]	—	6	—	7	—	7	—	9	—	10	ns
tPU	Chip Select to Power Up Time[3]	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Select to Power Down Time[3]	—	10	—	10	—	15	—	20	—	25	ns

AC ELECTRICAL CHARACTERISTICS[4] (Continued) (Vcc = 5.0V ± 10%, All Temperature Ranges)

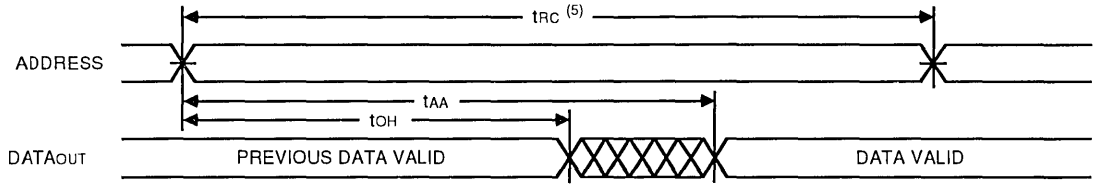
Symbol	Parameter	71681x35 71682x35 Min.	Max.	71681x45 71682x45 Min.	Max.	71681x55[2] 71682x55[2] Min.	Max.	71681x70[2] 71682x70[2] Min.	Max.	Unit
Read Cycle										
tRC	Read Cycle Time	35	—	45	—	55	—	70	—	ns
tAA	Address Access Time	—	35	—	45	—	55	—	70	ns
tACS	Chip Select Access Time	—	35	—	45	—	55	—	70	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
tCLZ	Chip Select to Output in Low-Z[3]	5	—	5	—	5	—	5	—	ns
tCHZ	Chip Select to Output in High-Z[3]	—	15	—	20	—	25	—	30	ns
tPU	Chip Select to Power-Up Time[3]	0	—	0	—	0	—	0	—	ns
tPD	Chip Select to Power-Down Time[3]	—	35	—	40	—	50	—	60	ns

NOTES:

2984 tbl 11

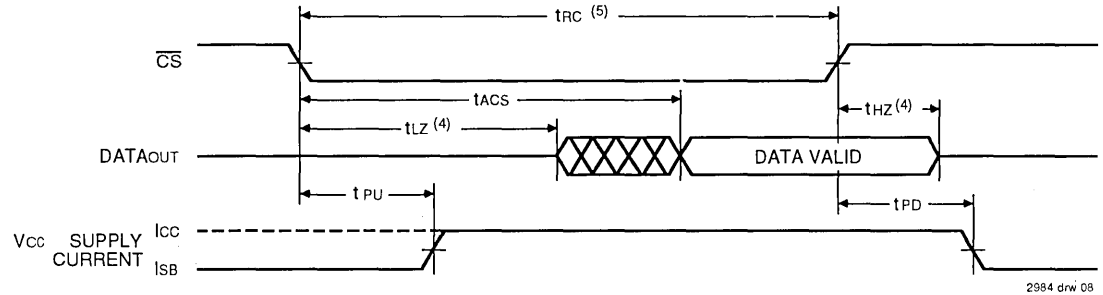
1. 0°C to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. This parameter guaranteed with AC Load (Figure 2) by device characterization, but is not production tested.
4. "x" in part numbers indicates power rating (SA or LA).

TIMING WAVEFORM OF READ CYCLE NO. 1(1, 2)



2984 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 3)



2984 drw 08

NOTES:
1. $\overline{WE}$ is HIGH for read cycle, $\overline{WE} \geq V_{IH}$.
2. Device is continuously selected, $\overline{CS} \leq V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. Transition is measured ±200mV from steady state.
5. All read cycle timings are referenced from the last valid address to the first transmitting address.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71681x10[1] 71682x10[1] Min.	Max.	71681x12 71682x12 Min.	Max.	71681x15 71682x15 Min.	Max.	71681x20 71682x20 Min.	Max.	71681x25 71682x25 Min.	Max.	Unit
Write Cycle												
tWC	Write Cycle Time	10	—	12	—	15	—	20	—	20	—	ns
tCW	Chip Select to End of Write	10	—	10	—	15	—	20	—	20	—	ns
tAW	Address Valid to End of Write	10	—	10	—	15	—	20	—	20	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	10	—	10	—	15	—	20	—	20	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	7	—	8	—	9	—	10	—	10	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tIY	Data Valid to Output Valid (71681 only)[3]	—	10	—	12	—	15	—	20	—	25	ns
tWY	Write Enable to Output Valid (71681 only)[3]	—	10	—	12	—	15	—	20	—	25	ns
tWHZ	Write Enable to Output in High-Z (71682 only)[3]	—	4	—	5	—	6	—	7	—	7	ns
tOW	Output Active from End of Write (71682 only)[3]	0	—	0	—	0	—	0	—	0	—	ns

5

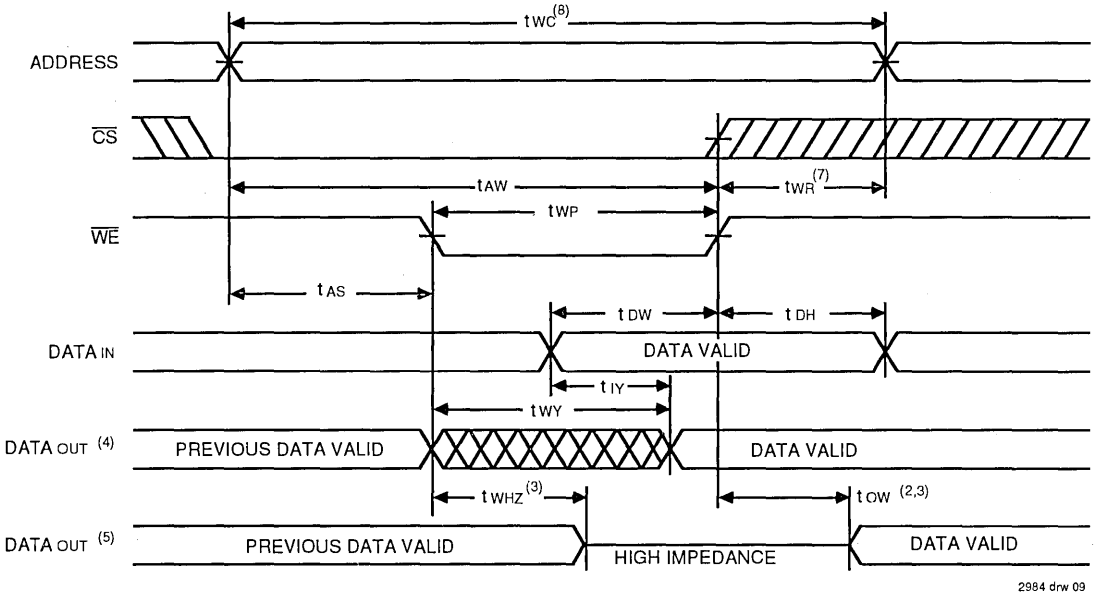
AC ELECTRICAL CHARACTERISTICS (Continued) (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71681x35 71682x35 Min.	Max.	71681x45 71682x45 Min.	Max.	71681x55[2] 71682x55[2] Min.	Max.	71681x70[2] 71682x70[2] Min.	Max.	Unit
Write Cycle										
tWC	Write Cycle Time	30	—	40	—	50	—	60	—	ns
tCW	Chip Select to End of Write	25	—	35	—	50	—	60	—	ns
tAW	Address Valid to End of Write	25	—	35	—	50	—	60	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	25	—	30	—	35	—	40	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	15	—	20	—	20	—	25	—	ns
tDH	Data Hold Time	3	—	3	—	3	—	3	—	ns
tIY	Data Valid to Output Valid (71681 only)[3]	—	30	—	35	—	35	—	40	ns
tWY	Write Enable to Output Valid (71681 only)[3]	—	30	—	35	—	35	—	40	ns
tWHZ	Write Enable to Output in High-Z (71682 only)[3]	—	13	—	20	—	25	—	30	ns
tOW	Output Active from End of Write (71682 only)[3]	0	—	0	—	0	—	0	—	ns

NOTES:
2984 tbl 12

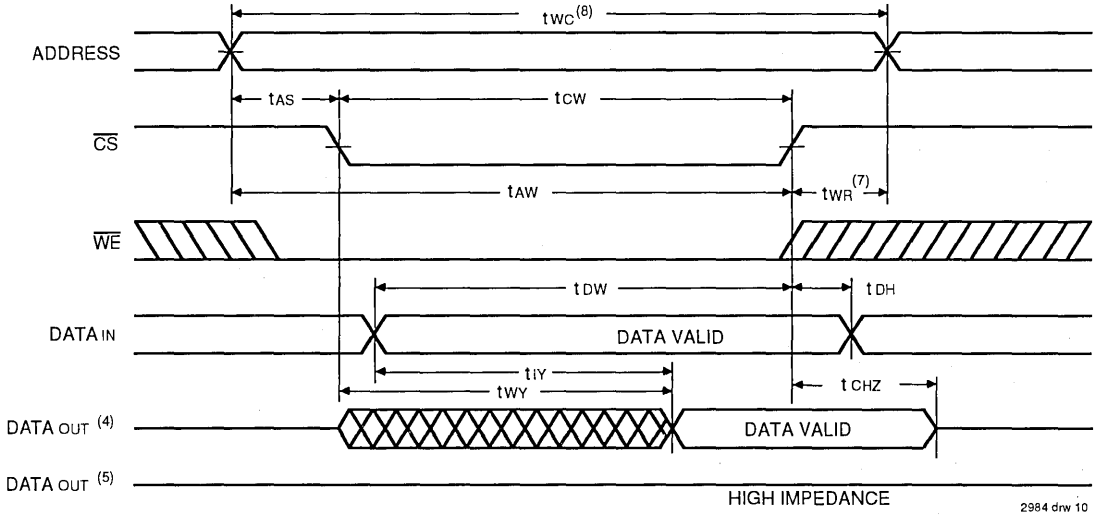
1. 0°C to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. This parameter guaranteed with AC Load (Figure 2) by device characterization, but is not production tested.
4. "x" in part numbers indicates power rating (SA or LA).

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(1,7)



2984 drw 09

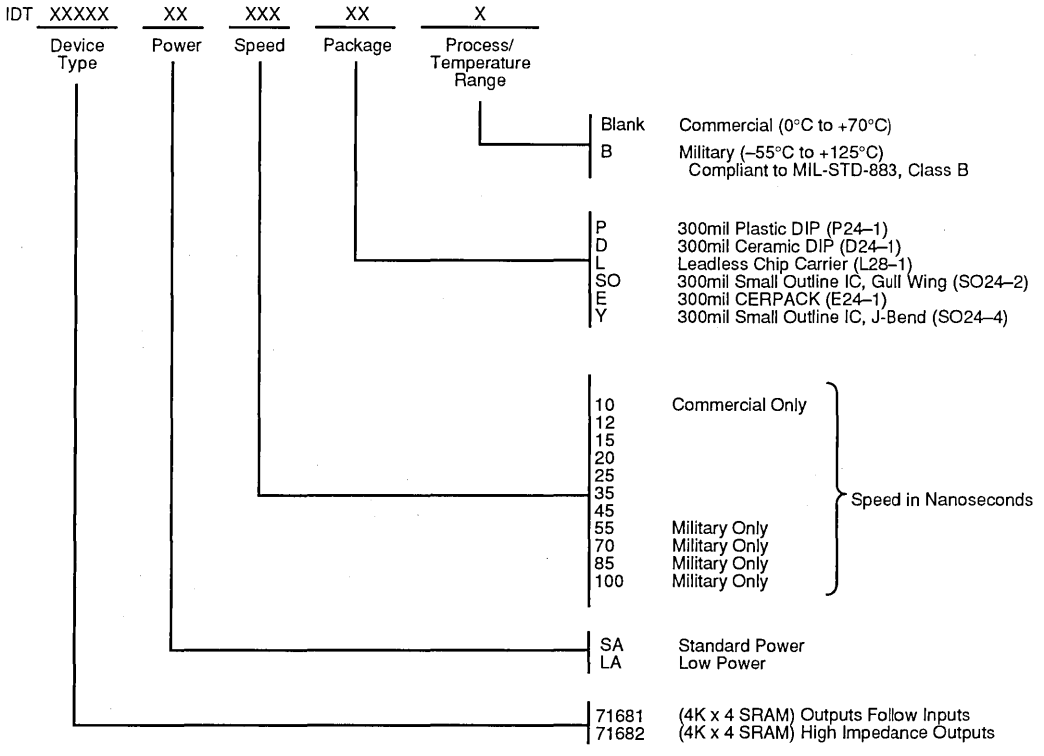
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1,6)



2984 drw 10

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. If the $\overline{CS}$ goesHIGH simultaneously with $\overline{WE}$ HIGH, the outputs remain in a high-impedance state.
3. Transition is measured ±200mV from steady state.
4. For IDT71681 only.
5. For IDT71682 only.
6. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
7. twR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
8. All write cycle timings are referenced from the last valid address to the first transitioning address.

ORDERING INFORMATION



2984 drw 11

5

Integrated Device Technology, Inc.

CMOS STATIC RAM 16K (2K X 8 BIT)

IDT6116SA
IDT6116LA

FEATURES:

- High-speed access and chip select times
  - — Military: 20/25/35/45/55/70/90/120/150ns (max.)
  - — Commercial: 15/20/25/35/45ns (max.)
- Low-power consumption
- Battery backup operation
  - —2V data retention voltage (LA version only)
- Produced with advanced CMOS high-performance technology
- CMOS process virtually eliminates alpha particle soft-error rates
- Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Available in standard 24-pin DIP, 24-pin Thin Dip and Plastic DIP, 28- and 32-pin LCC, 24-pin SOIC, 24-lead CERPACK and 24-pin SOJ
- Military product compliant to MIL-STD-833, Class B

DESCRIPTION:

The IDT6116SA/LA is a 16,384-bit high-speed static RAM organized as 2K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology.

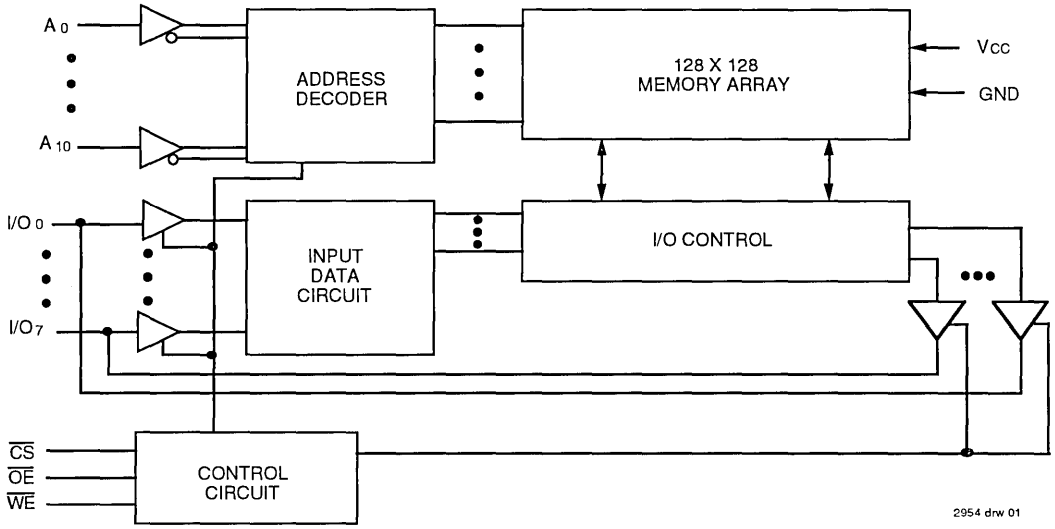
Access times as fast as 15ns are available. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes HIGH, the circuit will automatically go to, and remain in, a standby power mode, as long as $\overline{CS}$ remains HIGH. This capability provides significant system level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1μW to 4μW operating off a 2V battery.

All inputs and outputs of the IDT6116SA/LA are TTL-compatible. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

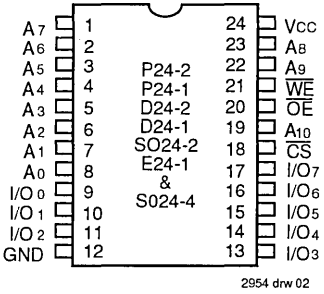
The IDT6116SA/LA is packaged in 24-pin 600 and 300 mil plastic or ceramic DIP, 28- and 32-pin leadless chip carriers, 24-lead CERPACK, and a 24-lead gull-wing SOIC, providing high board-level packing densities.

Military grade product is manufactured in compliance to the latest version of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

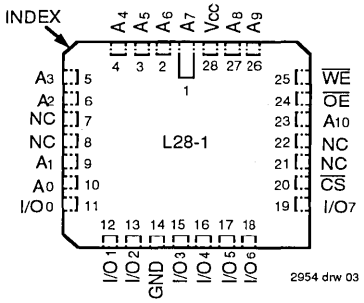
FUNCTIONAL BLOCK DIAGRAM



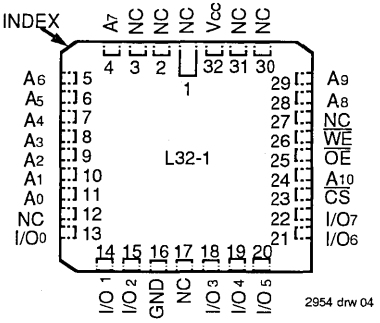
PIN CONFIGURATIONS



DIP/SOIC/CERPACK/SOJ
TOP VIEW



28-PIN LCC
TOP VIEW



32-PIN LCC
TOP VIEW

PIN NAMES

A0- A10	Address	$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Input/Output	$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select	GND	Ground
Vcc	Power		

2954 tbl 01

CAPACITANCE (TA = +25°C, F = 1.0 MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

NOTE:
2954 tbl 02

1. This parameter is determined by device characterization, but is not production tested.

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Rating	Commercial	Military	Unit
VTERM(2)	Terminal Voltage with Respect to GND	–0.5 to + 7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to + 70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to + 125	–65 to +135	°C
TSTG	Storage Temperature	–55 to + 125	–65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

NOTE:
2954 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed Vcc +0.5V.

5

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	VCC
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2954 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5(2)	V
GND	Supply Ground	0	0	0	V
VIH	Input High Voltage	2.2	3.5	VCC +0.5	V
VIL	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE:
2954 tbl 05

1. VIL (min.) = –3.0V for pulse width less than 20ns, once per cycle.
2. VIN must not exceed VCC +0.5V.

DC ELECTRICAL CHARACTERISTICS

VCC = 5.0V ± 10%

Symbol	Parameter	Test Conditions		DT6116SA Min.	DT6116SA Max.	IDT6116LA Min.	IDT6116LA Max.	Unit
|ILI|	Input Leakage Current	VCC = Max., VIN = GND to VCC	MIL.	—	10	—	10	µA
			COM'L.	—	5	—	2	
|ILO|	Output Leakage Current	VCC = Max. $\overline{CS}$ = VIH, VOUT = GND to VCC	MIL.	—	10	—	5	µA
			COM'L.	—	5	—	2	
VOL	Output Low Voltage	IOL = 8mA, VCC = Min.		—	0.4	—	0.4	V
VOH	Output High Voltage	IOH = –4mA, VCC = Min.		2.4	—	2.4	—	V

2954 tbl 06

DC ELECTRICAL CHARACTERISTICS (1)

VCC = 5.0V ± 10%, VLC = 0.2V, VHC = VCC - 0.2V

Symbol	Parameter	Power	6116SA15(2) 6116LA15(2) Com'l.	6116SA15(2) 6116LA15(2) Mil.	6116SA20 6116LA20 Com'l.	6116SA20 6116LA20 Mil.	6116SA25 6116LA25 Com'l.	6116SA25 6116LA25 Mil.	6116SA35 6116LA35 Com'l.	6116SA35 6116LA35 Mil.	Unit
ICC1	Operating Power Supply Current, $\overline{CS}$ ≤ VIL, Outputs Open, VCC = Max., f = 0	SA	105	—	105	130	80	90	80	90	mA
		LA	95	—	95	120	75	85	75	85	
ICC2	Dynamic Operating Current, $\overline{CS}$ ≤ VIL, VCC = Max., Outputs Open, f = fMAX(4)	SA	150	—	130	150	120	135	100	115	mA
		LA	140	—	120	140	110	125	95	105	
ISB	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ VIH, VCC = Max., Outputs Open, f = fMAX(4)	SA	40	—	40	50	40	45	25	35	mA
		LA	35	—	35	45	35	40	25	30	
ISB1	Full Standby Power Supply Current (CMOS Level), $\overline{CS}$ ≥ VHC, VCC = Max., VIN ≥ VHC or VIN ≤ VLC, f = 0	SA	2	—	2	10	2	10	2	10	mA
		LA	0.1	—	0.1	0.9	0.1	0.9	0.1	0.9	

NOTES:
2954 tbl 07

1. All values are maximum guaranteed values.
2. 0°C to + 70°C temperature range only.
3. –55°C to + 125°C temperature range only.
4. fMAX = 1/tRC, only address inputs are cycling at fMAX, f = 0 means address inputs are not changing.

DC ELECTRICAL CHARACTERISTICS [1] (Continued)

V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Power	6116SA45 6116LA45 Com'l.	6116SA45 6116LA45 Mil.	6116SA55[3] 6116LA55[3] Com'l.	6116SA55[3] 6116LA55[3] Mil.	6116SA70[3] 6116LA70[3] Com'l.	6116SA70[3] 6116LA70[3] Mil.	6116SA90[3] 6116LA90[3] Com'l.	6116SA90[3] 6116LA90[3] Mil.	6116SA120[3] 6116LA120[3] Com'l.	6116SA120[3] 6116LA120[3] Mil.	6116SA150[3] 6116LA150[3] Com'l.	6116SA150[3] 6116LA150[3] Mil.	Unit
I_{CC1}	Operating Power Supply Current, $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = 0	SA	80	90	—	90	—	90	—	90	—	90	—	90	mA
		LA	75	85	—	85	—	85	—	85	—	85	—	85	
I_{CC2}	Dynamic Operating Current, $\overline{CS} \le V_{IL}$, V_{CC} = Max., Outputs Open, f = f_{MAX}[4]	SA	100	100	—	100	—	100	—	100	—	100	—	90	mA
		LA	90	95	—	90	—	90	—	85	—	85	—	85	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \ge V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}[4]	SA	25	25	—	25	—	25	—	25	—	25	—	25	mA
		LA	20	20	—	20	—	20	—	25	—	15	—	15	
I_{SB1}	Full Standby Power Supply Current (CMOS Level), $\overline{CS} \ge V_{HC}$, V_{CC} = Max., $V_{IN} \ge V_{HC}$ or $V_{IN} \le V_{LC}$, f = 0	SA	2	10	—	10	—	10	—	10	—	10	—	10	mA
		LA	0.1	0.9	—	0.9	—	0.9	—	0.9	—	0.9	—	0.9	

NOTES:
1. All values are maximum guaranteed values.
2. 0°C to + 70°C temperature range only.
3. –55°C to + 125°C temperature range only.
4. f_{MAX} = 1/t_{RC}, only address inouts are toggling at f_{MAX}, f = 0 means address inputs are not changing.

2954 tbl 08

5

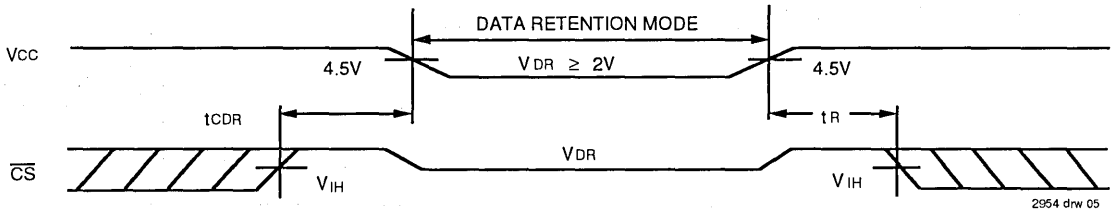
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES (LA VERSION ONLY) VLC = 0.2V, VHC = VCC - 0.2V

Symbol	Parameter	Test Conditions		Min.	Typ.[1] VCC @ 2.0V	Typ.[1] VCC @ 3.0V	Max. VCC @ 2.0V	Max. VCC @ 3.0V	Unit
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \ge V_{HC}$	MIL.	—	0.5	1.5	200	300	µA
			COM'L.	—	0.5	1.5	20	30	
t_{CDR}[3]	Data Deselect to Data Retention Time	$V_{IN} \ge V_{HC}$ or $\le V_{LC}$		—	0	—	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	—	—	ns
$\|I_{LI}\|$	Input Leakage Current			—	—	—	2	2	µA

NOTES:
1. T_A = + 25°C
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization, but is not production tested.

2954 tbl 09

LOW Vcc DATA RETENTION WAVEFORM



2954 drw 05

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2954 tbl 10

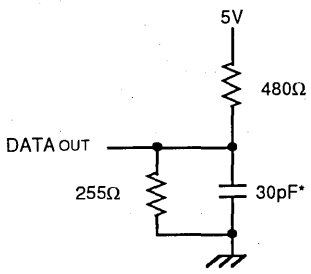
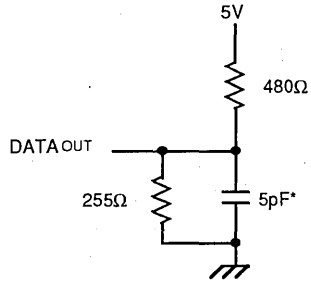


Figure 1. AC Test Load



2954 drw 06

Figure 2. AC Test Load (for tOLZ, tCLZ, tOHZ, tWHZ, tCHZ & tOW)

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5V ± 10%, All Temperature Ranges)

Symbol	Parameter	6116SA15[1] 6116LA15[1] Min.	Max.	6116SA20 6116LA20 Min.	Max.	6116SA25 6116LA25 Min.	Max.	6116SA35 6116LA35 Min.	Max.	Unit
READ CYCLE										
tRC	Read Cycle Time	15	—	20	—	25	—	35	—	ns
tAA	Address Access Time	—	15	—	19	—	25	—	35	ns
tACS	Chip Select Access Time	—	15	—	20	—	25	—	35	ns
tCLZ	Chip Select to Output in Low-Z[3]	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	10	—	10	—	13	—	20	ns
tOLZ	Output Enable to Output in Low-Z[3]	0	—	0	—	5	—	5	—	ns
tCHZ	Chip Deselect to Output in High-Z[3]	—	10	—	11	—	12	—	15	ns
tOHZ	Output Disable to Output in High-Z[3]	—	8	—	8	—	10	—	13	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
tPU	Chip Select to Power-Up Time[3]	0	—	0	—	0	—	0	—	ns
tPD	Chip Deselect to Power-Down Time[3]	—	15	—	20	—	25	—	35	ns

2954 tbl 11

5

AC ELECTRICAL CHARACTERISTICS (Vcc = 5V ± 10%, All Temperature Ranges) (Continued)

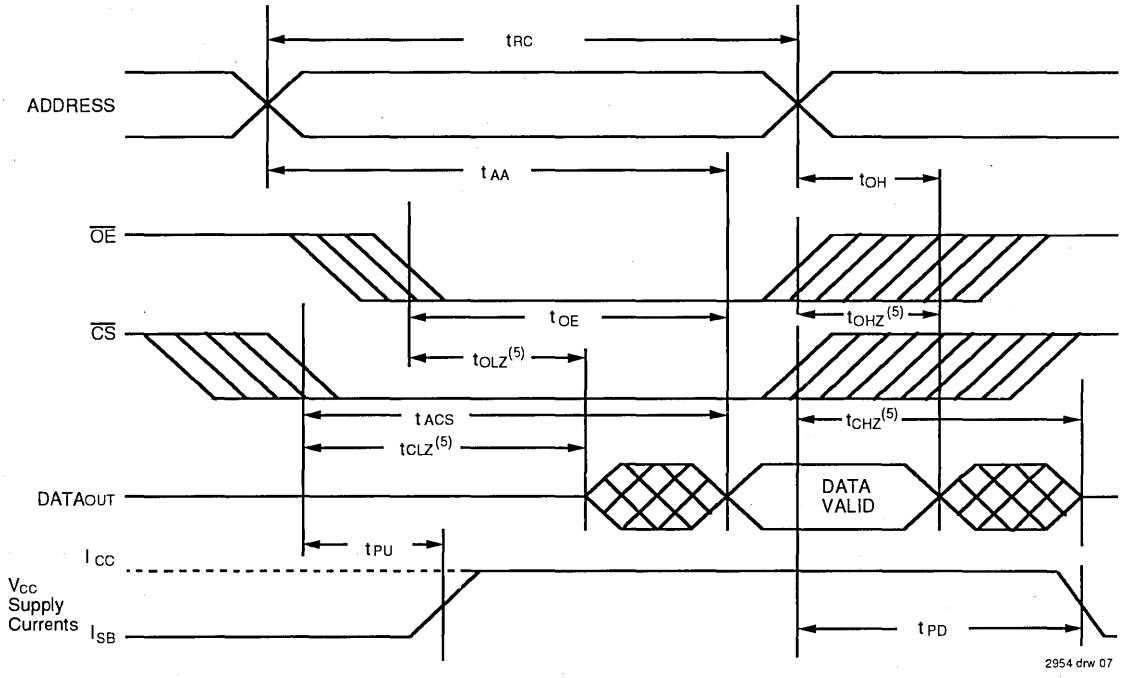
Symbol	Parameter	6116SA45 6116LA45 Min.	Max.	6116SA55[2] 6116LA55[2] Min.	Max.	6116SA70[2] 6116LA70[2] Min.	Max.	6116SA90[2] 6116LA90[2] Min.	Max.	6116SA120[2] 6116LA120[2] Min.	Max.	6116SA150[2] 6116LA150[2] Min.	Max.	Unit
READ CYCLE														
tRC	Read Cycle Time	45	—	55	—	70	—	90	—	120	—	150	—	ns
tAA	Address Access Time	—	45	—	55	—	70	—	90	—	120	—	150	ns
tACS	Chip Select Access Time	—	45	—	50	—	65	—	90	—	120	—	150	ns
tCLZ	Chip Select to Output in Low-Z[3]	5	—	5	—	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	25	—	40	—	50	—	60	—	80	—	100	ns
tOLZ	Output Enable to Output in Low-Z[3]	5	—	5	—	5	—	5	—	5	—	5	—	ns
tCHZ	Chip Deselect to Output in High-Z[3]	—	20	—	30	—	35	—	40	—	40	—	40	ns
tOHZ	Output Disable to Output in High-Z[3]	—	15	—	30	—	35	—	40	—	40	—	40	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns

NOTES:

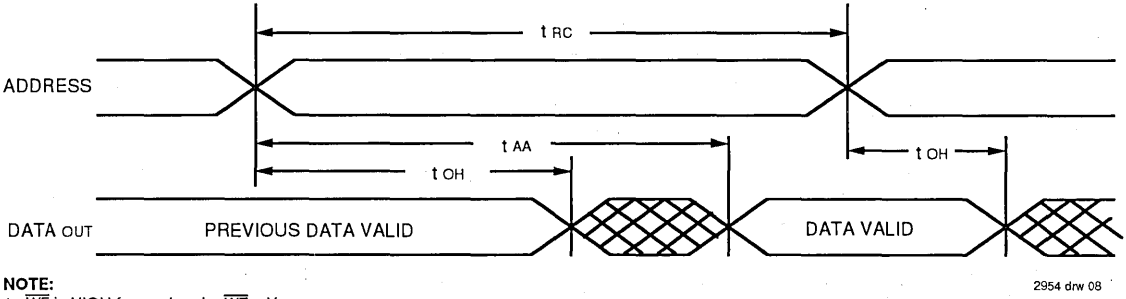
2954 tbl 12

1. 0°C to + 70°C temperature range only.
2. –55°C to + 125°C temperature range only.
3. This parameter guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

TIMING WAVEFORM OF READ CYCLE NO. 1 (1, 3)

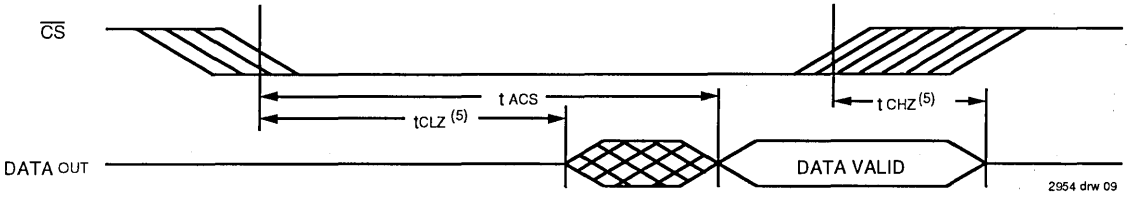


TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



NOTE:
1. $\overline{WE}$ is HIGH for read cycle, $\overline{WE} \geq V_{IH}$.
2. Device is continously selected, $\overline{CS} \leq V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. Output enable is continuously active, $\overline{OE} \leq V_{IL}$.
5. Transition is measured ±500mV from steady state.

TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



NOTE:
1. $\overline{WE}$ is HIGH for read cycle, $\overline{WE} \geq V_{IH}$
2. Device is continously selected, $\overline{CS} \leq V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} \leq V_{IL}$.
5. Transition is measured ±500mV from steady state.

5

AC ELECTRICAL CHARACTERISTICS (Vcc = 5V ± 10%, All Temperature Ranges)

Symbol	Parameter	6116SA15(1) 6116LA15(1) Min.	6116SA15(1) 6116LA15(1) Max.	6116SA20 6116LA20 Min.	6116SA20 6116LA20 Max.	6116SA25 6116LA25 Min.	6116SA25 6116LA25 Max.	6116SA35 6116LA35 Min.	6116SA35 6116LA35 Max.	Unit
WRITE CYCLE										
tWC	Write Cycle Time	15	—	20	—	25	—	35	—	ns
tCW	Chip Select to End-of-Write	13	—	15	—	17	—	25	—	ns
tAW	Address Valid to End-of-Write	14	—	15	—	17	—	25	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	12	—	12	—	15	—	20	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tWHZ	Write to Output in High-Z(3)	—	7	—	8	—	16	—	20	ns
tDW	Data to Write Time Overlap	12	—	12	—	13	—	15	—	ns
tDH	Data Hold from Write Time(4)	0	—	0	—	0	—	0	—	ns
tOW	Output Active from End-of-Write (3,4)	0	—	0	—	0	—	0	—	ns

NOTES:
2954 tbl 13

1. 0°C to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. This parameter guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operation conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5V ± 10%, All Temperature Ranges)

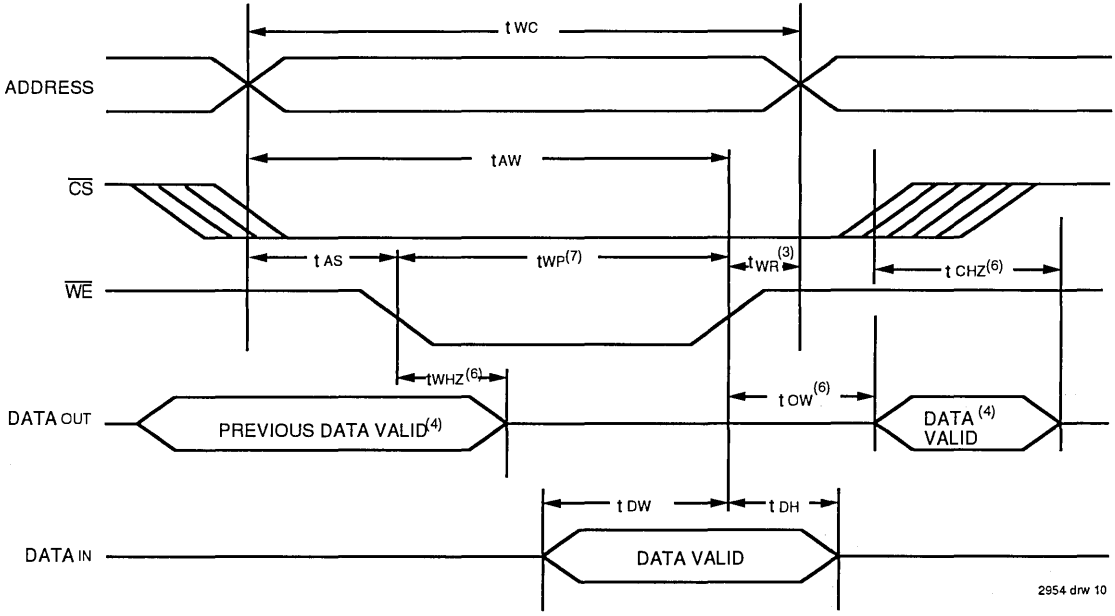
Symbol	Parameter	6116SA45 6116LA45		6116SA55[2] 6116LA55[2]		6116SA70[2] 6116LA70[2]		6116SA90[2] 6116LA90[2]		6116SA120[2] 6116LA120[2]		6116SA150[2] 6116LA150[2]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE														
tWC	Write Cycle Time	45	—	55	—	70	—	90	—	120	—	150	—	ns
tCW	Chip Select to End of Write	30	—	40	—	40	—	55	—	70	—	90	—	ns
tAW	Address Valid to End of Write	30	—	45	—	65	—	80	—	105	—	120	—	ns
tAS	Address Set-up Time	0	—	5	—	15	—	15	—	20	—	20	—	ns
tWP	Write Pulse Width	25	—	40	—	40	—	55	—	70	—	90	—	ns
tWR	Write Recovery Time	0	—	5	—	5	—	5	—	5	—	10	—	ns
tWHZ	Write to Output in High-Z[3]	—	25	—	30	—	35	—	40	—	40	—	40	ns
tDW	Data to Write Time Overlap	20	—	25	—	30	—	30	—	35	—	40	—	ns
tDH	Data Hold from Write Time[4]	0	—	5	—	5	—	5	—	5	—	10	—	ns
tOW	Output Active from End of Write[3,4]	0	—	0	—	0	—	0	—	0	—	0	—	ns

NOTES:

2954 tbl 14

1. 0°C to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. This parameter guaranteed with AC Load (Figure 2) by device characterization, but is not production tested.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operation conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.

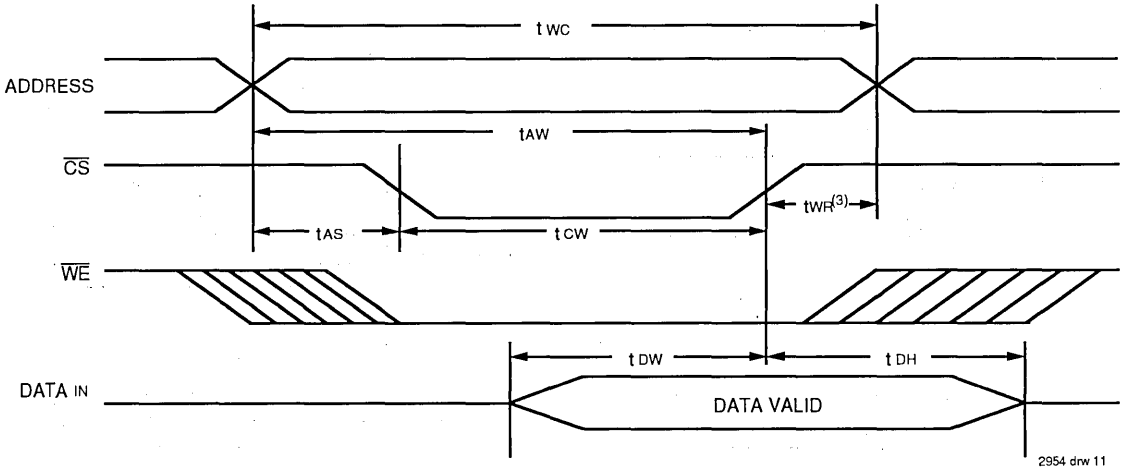
TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING) (1, 2, 5, 7)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state and the input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in the high-impedance state.
6. Transition is measured ±500mV from steady state.
7. $\overline{OE}$ is continuously HIGH. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of twp or (twhz + tdw) to allow the I/O drivers to turn off and data to be placed on the bus for the required tdw. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse is the specified twp.

5

TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING) (1, 2, 3, 5, 7)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state and the input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in the high-impedance state.
6. Transition is measured ±500mV from steady state.
7. $\overline{OE}$ is continuously HIGH. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of twp or (twhz + tdw) to allow the I/O drivers to turn off and data to be placed on the bus for the required tdw. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse is the specified twp. For a $\overline{CS}$ controlled write cycle, $\overline{OE}$ may be LOW with no degradation to tcw.

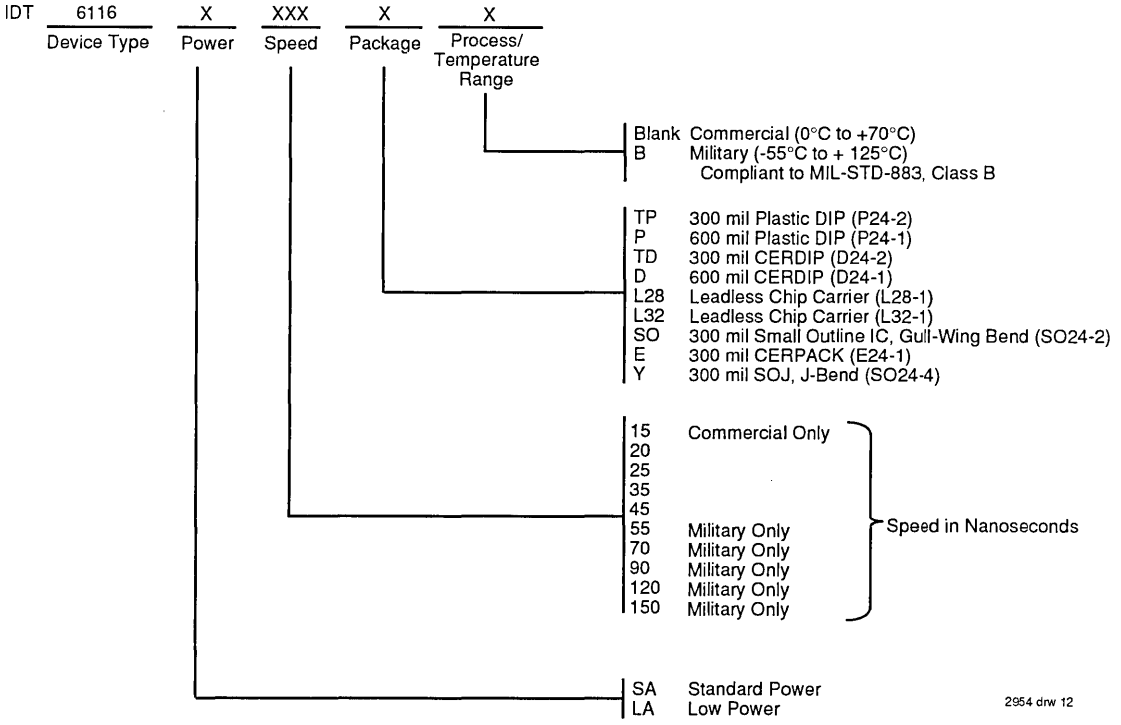
TRUTH TABLE(1)

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O
Standby	H	X	X	High-Z
Read	L	L	H	DATAOUT
Read	L	H	H	High-Z
Write	L	X	L	DATAIN

2954 tbl 15

NOTE:
1. H = VIH, L = VIL, X = Don't Care.

ORDERING INFORMATION



5

64K SRAM PRODUCTS

At the 64K density, IDT SRAMs are not only built with state-of-the-art CMOS technology, but BiCMOS technology as well. Consequently, IDT's 64K SRAMs are amongst the fastest in the world.

The 64K CMOS parts offer unmatched capabilities in terms of standby power consumption in its low power versions, while preserving the fast speed attributes typical of IDT SRAMs. Commercial parts are available in speeds as fast as 15ns, while military devices are as fast as 20ns. The BiCMOS parts are offered in commercial speeds as fast as 8ns, but are not available in military versions. The 64K family is offered in a wide variety of speeds and packages.

The low power consumption characteristics of the "L" power versions makes them ideal for portable instruments and notebook computers, while the "S" power fast CMOS and BiCMOS parts are well suited for high-performance workstations, PCs, communications, and industrial applications.

Size	Org.	Features	Process	Part Number	Power	Speeds	
						Commercial	Military
64K	64K x 1		CMOS	7187	S/L	15,20,25,35	25,35,45,55,70,85
	16K x 4		CMOS	7188	S/L	15,20,25,35	20,25,35,45,55,70,85
	16K x 4		BiCMOS	71B88	S	8,10,12	N/A
	16K x 4	OE	CMOS	6198	S/L	15,20,25,35	20,25,35,45,55,70,85
	16K x 4	OE	BiCMOS	61B98	S	8,10,12	N/A
	16K x 4	OE, CS2	CMOS	7198	S/L	15,20,25,35	20,25,35,45,55,70,85
	16K x 4	Sep I/O	CMOS	71981	S/L	15,20,25,35	20,25,35,45,55,70,85
	16K x 4	Sep I/O	CMOS	71982	S/L	15,20,25,35	20,25,35,45,55,70,85
	8K x 8		CMOS	7164	S/L	15,20,25,35	20,25,35,45,55,70,85
	8K x 8		BiCMOS	71B64	S	8,10,12	N/A

TABLE OF CONTENTS

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Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (64K x 1-BIT)

IDT7187S
IDT7187L

FEATURES:

- High speed (equal access and cycle time)
  - — Military: 20/25/35/45/55/70/85ns (max.)
  - — Commercial: 15/20/25/35ns (max.)
- Low power consumption
- Battery backup operation—2V data retention (L version only)
- JEDEC standard high-density 22-pin plastic and ceramic DIP, 24-pin plastic SOIC, 22-pin and 28-pin leadless chip carrier and 24-pin CERPACK
- Produced with advanced CMOS high-performance technology
- Separate data input and output
- Input and output directly TTL-compatible
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

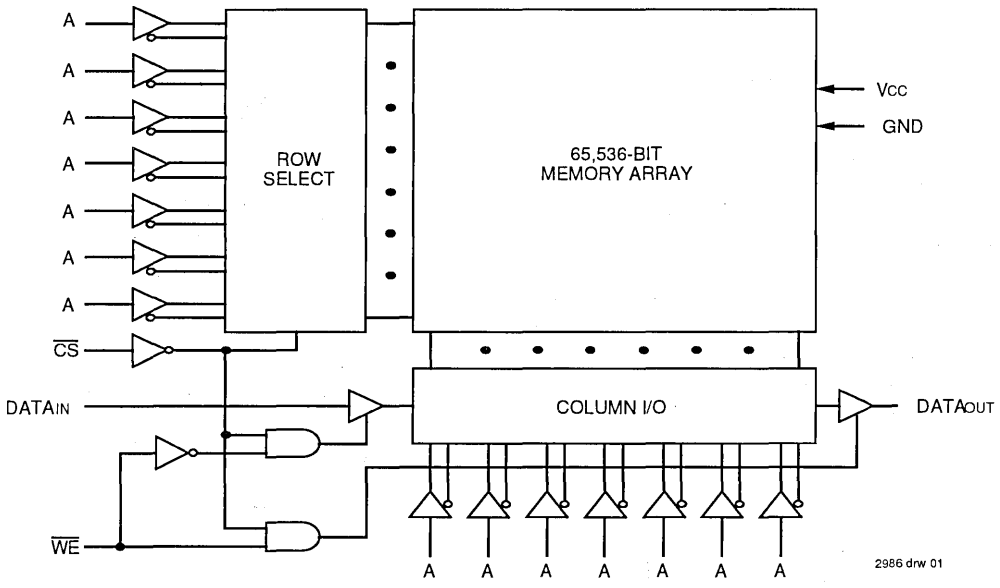
The IDT7187 is a 65,536-bit high-speed static RAM organized as 64K x 1. It is fabricated using IDT's high-performance, high-reliability CMOS technology. Access times as fast as 15ns are available.

Both the standard (S) and low-power (L) versions of the IDT7187 provide two standby modes—I_{SB} and I_{SB1}. I_{SB} provides low-power operation; I_{SB1} provides ultra-low-power operation. The low-power (L) version also provides the capability for data retention using battery backup. When using a 2V battery, the circuit typically consumes only 30µW.

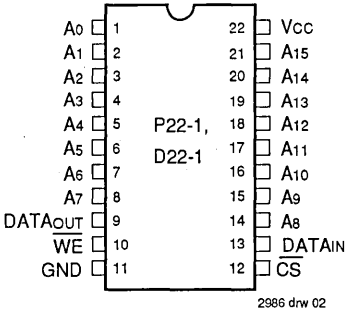
Ease of system design is achieved by the IDT7187 with full asynchronous operation, along with matching access and cycle times. The device is packaged in an industry standard 22-pin, 300 mil plastic or ceramic DIP, 24-pin plastic SOIC (Gull-Wing and J-Bend), 22- and 28-pin leadless chip carriers, or 24-pin CERPACK.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

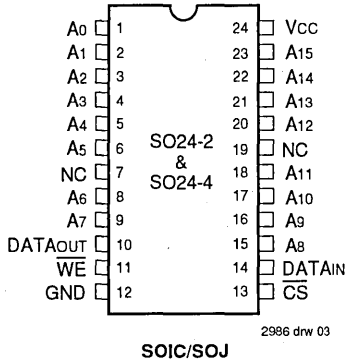
FUNCTIONAL BLOCK DIAGRAM



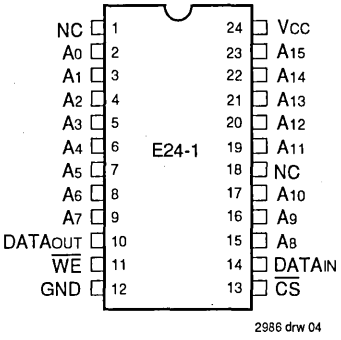
PIN CONFIGURATIONS



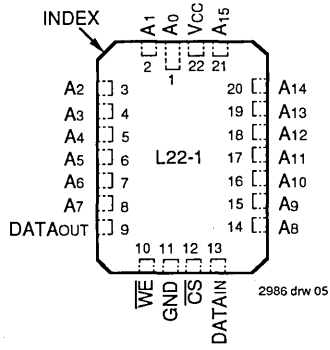
DIP
TOP VIEW



SOIC/SOJ
TOP VIEW



CERPACK
TOP VIEW

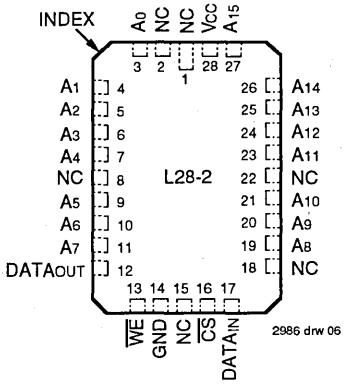


22-PIN LCC
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A0–A15	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
VCC	Power
DATAIN	Data Input
DATAOUT	Data Output
GND	Ground

2986 tbl 01



28-PIN LCC
TOP VIEW

TRUTH TABLE[1]

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High-Z	Standby
Read	L	H	DOUT	Active
Write	L	L	High-Z	Active

2986 tbl 02

NOTES:
1. H = VIH, L = VIL, X = don't care.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

2986 tbl 03

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

2986 tbl 04

NOTE:
1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	–0.5[1]	—	0.8	V

2986 tbl 05

NOTE:
1. VIL (min.) = –3.0V for pulse width less than 20ns, once per cycle.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	VCC
Military	–55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2986 tbl 06

6

DC ELECTRICAL CHARACTERISTICS

(VCC = 5.0V ± 10%)

Symbol	Parameter	Test Condition		IDT7187S Min.	IDT7187S Max.	IDT7187L Min.	IDT7187L Max.	Unit
|ILI|	Input Leakage Current	VCC = Max., VIN = GND to VCC	MIL.	—	10	—	5	µA
			COM'L.	—	5	—	2	
|ILO|	Output Leakage Current	VCC = Max., $\overline{CS}$ = VIH, VOUT = GND to VCC	MIL.	—	10	—	5	µA
			COM'L.	—	5	—	2	
VOL	Output Low Voltage	IOL = 10mA, VCC = Min.			0.5	—	0.5	V
		IOL = 8mA, VCC = Min.		—	0.4	—	0.4	
VOH	Output High Voltage	IOL = –4mA, VCC = Min.		2.4	—	2.4	—	V

2986 tbl 07

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	7187S15[3] Com'l.	7187S15[3] Mil.	7187S20 7187L20 Com'l.	7187S20 7187L20 Mil.[3]	7187S25 7187L25 Com'l.	7187S25 7187L25 Mil.	7187S35 7187L35 Com'l.	7187S35 7187L35 Mil.	7187S45 7187L45 Com'l.	7187S45 7187L45 Mil.	7187S55/70 7187L55/70 Com'l.	7187S55/70 7187L55/70 Mil.	7187S85 7187L85 Com'l.	7187S85 7187L85 Mil.	Unit
I_{CC1}	Operating Power Supply Current	S	100	—	90	105	90	105	90	105	—	105	—	105	—	105	mA
	$\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = 0[2]	L	—	—	70	85	70	85	70	85	—	85	—	85	—	85	
I_{CC2}	Dynamic Operating Current	S	140	—	130	140	120	130	110	120	—	120	—	120	—	120	mA
	$\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = f_{MAX}[2]	L	—	—	110	120	100	110	90	100	—	95	—	90	—	90	
I_{SB}	Standby Power Supply Current (TTL Level)	S	60	—	55	65	50	55	45	50	—	50	—	50	—	50	mA
	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}[2]	L	—	—	40	60	35	50	30	40	—	35	—	30/28	—	28	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC}=Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0[2]	S	20	—	15	20	15	20	15	20	—	20	—	20	—	20	mA
		L	—	—	0.3	1.5	0.3	1.5	0.3	1.5	—	1.5	—	1.5	—	1.5	

NOTES: 2986 tbl 06

1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.
3. These specs are preliminary.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

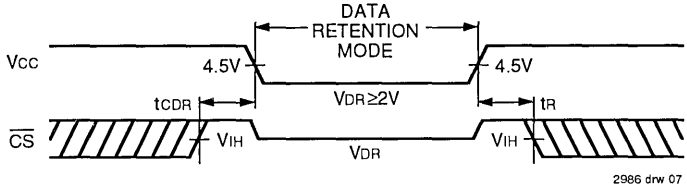
(L Version Only) V_{HC} = V_{CC} - 0.2V, V_{LC} = 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.[1] Vcc @ 2.0v	Typ.[1] Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	Vcc for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS}$ ≥ V_{HC} V_{IN} ≥ V_{HC} or ≤ V_{LC}	MIL.	—	10	15	600	900	µA
			COM'L.	—	10	15	150	225	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	—	—	ns
$\|I_{LI}\|$[3]	Input Leakage Current			—	—	—	2	2	µA

NOTES: 2986 tbl 09

1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

LOW Vcc DATA RETENTION WAVEFORM



2986 drw 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2986 tbl 10

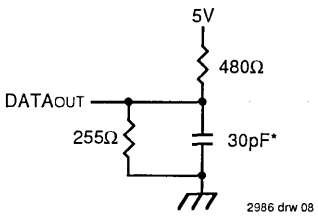


Figure 1. AC Test Load

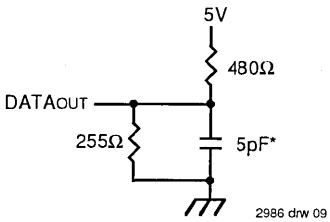


Figure 2. AC Test Load (for tHZ, tLZ, tWZ and tOW)

*Includes scope and jig capacitances

AC ELECTRICAL CHARACTERISTICS (VCC = 5.0V ± 10%, All Temperature Ranges)

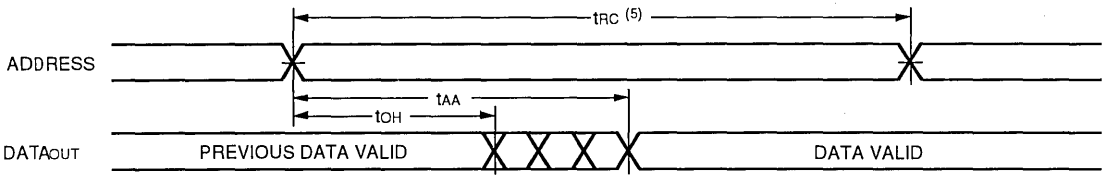
Symbol	Parameter	7187S15[1]/20 7187L20 Min.	7187S15[1]/20 7187L20 Max.	7187S25 7187L25 Min.	7187S25 7187L25 Max.	7187S35/45[2] 7187L35/45[2] Min.	7187S35/45[2] 7187L35/45[2] Max.	7187S55[2] 7187L55[2] Min.	7187S55[2] 7187L55[2] Max.	7187S70[2] 7187L70[2] Min.	7187S70[2] 7187L70[2] Max.	7187S85[2] 7187L85[2] Min.	7187S85[2] 7187L85[2] Max.	Unit
Read Cycle														
tRC	Read Cycle Time	15/20	—	25	—	35/45	—	55	—	70	—	85	—	ns
tAA	Address Access Time	—	15/20	—	25	—	35/45	—	55	—	70	—	85	ns
tACS	Chip Select Access Time	—	15/20	—	25	—	35/45	—	55	—	70	—	85	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
tLZ	Output Selection to Output in Low-Z[3]	5	—	5	—	5	—	5	—	5	—	5	—	ns
tHZ	Chip Deselect to Output in High-Z[3]	—	6	—	12	—	17/20	—	30	—	30	—	40	ns
tPU	Chip Select to Power-Up Time[3]	0	—	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Deselect to Power-Down Time[3]	—	15/20	—	20	—	30/35	—	35	—	35	—	40	ns

2986 tbl 11

NOTES:
1. 0° to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

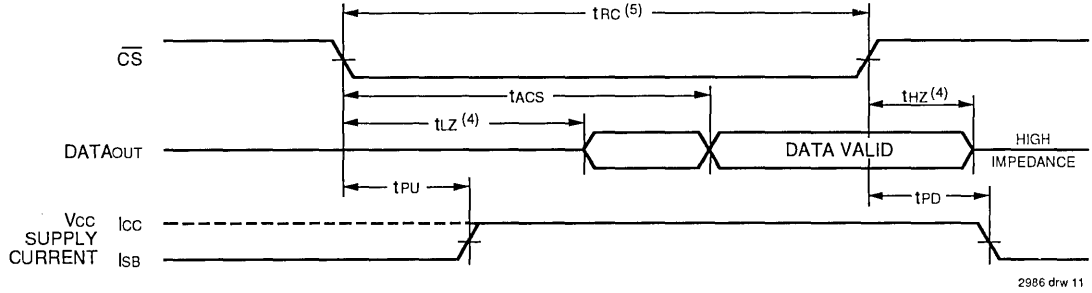
6

TIMING WAVEFORM OF READ CYCLE NO. 1(1,2)



2986 drw 10

TIMING WAVEFORM OF READ CYCLE NO. 2(1,3)



2986 drw 11

NOTES:
1. $\overline{WE}$ is HIGH for read cycle.
2. $\overline{CS}$ is LOW for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

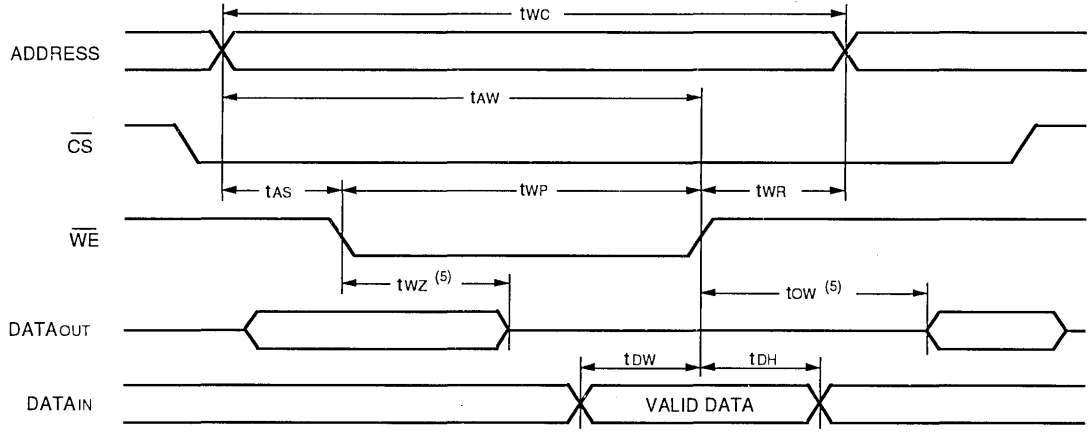
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7187S15[1]/20 7187L20		7187S25 7187L25		7187S35/45[2] 7187L35/45[2]		7187S55[2] 7187L55[2]		7187S70[2] 7187L70[2]		7187S85[2] 7187L85[2]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle														
tWC	Write Cycle Time	12/15	—	25	—	35/45	—	55	—	70	—	85	—	ns
tCW	Chip Select to End-of-Write	12/15	—	20	—	25/40	—	50	—	55	—	65	—	ns
tAW	Address Valid to End-of-Write	12/15	—	20	—	25/40	—	50	—	55	—	65	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	12/15	—	20	—	20/25	—	35	—	40	—	45	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	8/10	—	15	—	15/25	—	25	—	30	—	35	—	ns
tDH	Data Hold Time	0	—	5	—	5	—	5	—	5	—	5	—	ns
tWZ	Write Enable to Output in High-Z[3]	—	6/8	—	12	—	15/30	—	30	—	30	—	40	ns
tOW	Output Active from End-of-Write[3]	0	—	0	—	0	—	0	—	0	—	0	—	ns

NOTES:
2986 tbl 12

1. 0° to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)[1,2,3,4]

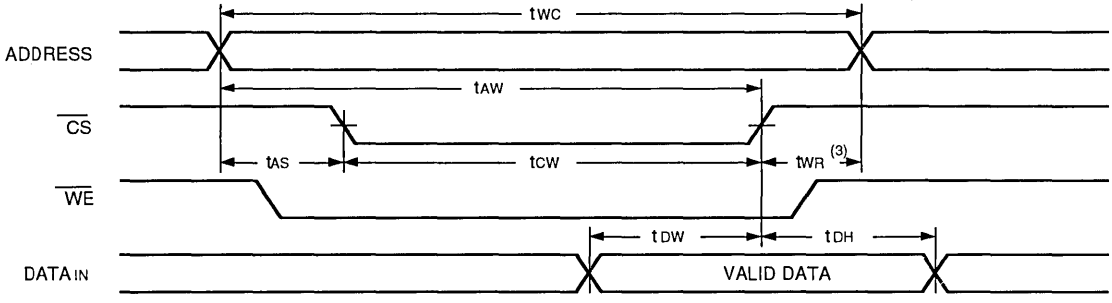


2986 drw 12

NOTES:

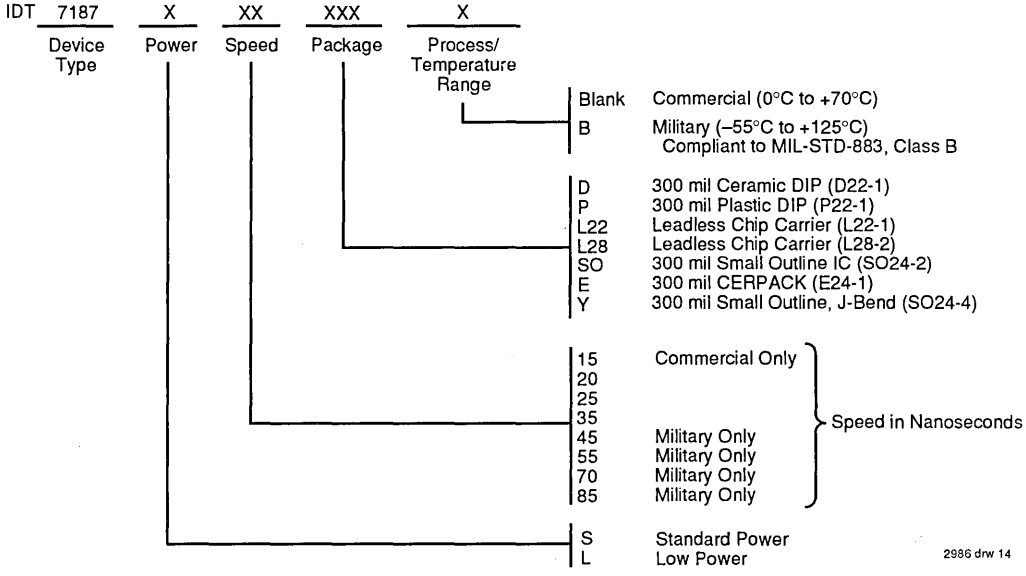
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tWP) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high-impedance state.
5. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1,2,4)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tWP) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high-impedance state.
5. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (16K x 4-BIT)

IDT7188S
IDT7188L

FEATURES:

- High-speed (equal access and cycle times)
  - — Military: 20/25/35/45/55/70/85ns (max.)
  - — Commercial: 15/20/25/35ns (max.)
- Low power consumption
- Battery backup operation — 2V data retention (L version only)
- Available in high-density industry standard 22-pin, 300 mil ceramic and plastic DIP, 24-pin SOJ and CERPACK
- Produced with advanced CMOS technology
- Inputs/outputs TTL-compatible
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

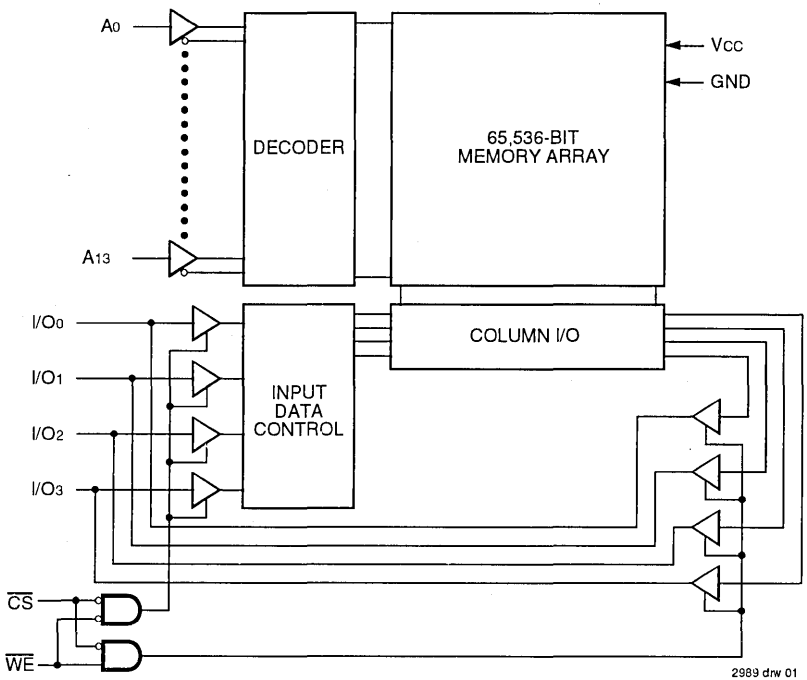
The IDT7188 is a 65,536-bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-performance, high-reliability technology — CMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for memory intensive applications.

Access times as fast as 15ns are available. The IDT7188 offers a reduced power standby mode, I_{SB1}, which is activated when $\overline{CS}$ goes high. This capability significantly decreases power while enhancing system reliability. The low-power version (L) version also offers a battery backup data retention capability where the circuit typically consumes only 30µW operating from a 2V battery.

All inputs and outputs are TTL-compatible and operate from a single 5V supply. The IDT7188 is packaged in 22-pin, 300 mil ceramic and plastic DIPs, 24-pin SOJs and CERPACKs, providing excellent board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

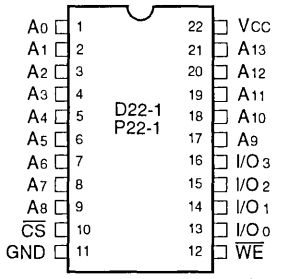
FUNCTIONAL BLOCK DIAGRAM



6

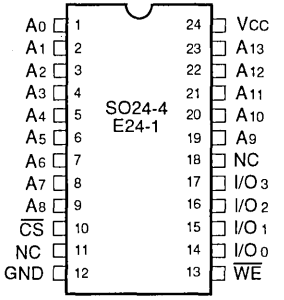
The IDT logo is a registered trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



2989 drw 02

DIP
TOP VIEW



2989 drw 03

CERPACK/SOJ
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A0–A13	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
I/O0-3	Data Input/Output
VCC	Power
GND	Ground

2989 tbl 01

TRUTH TABLE(1)

Mode	$\overline{CS}$	$\overline{WE}$	I/O	Power
Standby	H	X	High Z	Standby
Read	L	H	DOUT	Active
Write	L	L	DIN	Active

NOTE: 2989 tbl 02
1. H = VIH, L = VIL, X = don't care.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

NOTE: 2989 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz, VCC = 0v))

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	pF
COUT	Output Capacitance	VOUT = 0V	6	pF

NOTE: 2989 tbl 04
1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2989 tbl 05
1. VIL (min.) = -3.0V for pulse width less than 20ns,once per cycle.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2989 tbl 06

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT7188S Min.	IDT7188S Max.	IDT7188L Min.	IDT7188L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL. COM'L.	— —	10 5	— —	5 2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL. COM'L.	— —	10 5	— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.			0.5	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	2.4	—	V

2989 tbl 07

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	7188S15 7188L15 Com'l.	7188S15 7188L15 Mil.	7188S20 7188L20 Com'l.	7188S20 7188L20 Mil.	7188S25 7188L25 Com'l.	7188S25 7188L25 Mil.	7188S35 7188L35 Com'l.	7188S35 7188L35 Mil.	7188S45 7188L45 Com'l.	7188S45 7188L45 Mil.	7188S55/70 7188L55/70 Com'l.	7188S55/70 7188L55/70 Mil.	7188S85 7188L85 Com'l.	7188S85 7188L85 Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = 0(2)	S	100	—	100	105	100	105	100	105	—	105	—	105	—	105	mA
		L	75	—	70	80	70	80	70	80	—	80	—	80	—	80	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = f_{MAX}(2)	S	135	—	125	160	125	155	125	140	—	140	—	140	—	140	mA
		L	125	—	115	130	105	120	105	115	—	110	—	110	—	105	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}(2)	S	60	—	55	70	50	60	45	50	—	50	—	50	—	50	mA
		L	45	—	40	50	35	40	30	40	—	35	—	35	—	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC}=Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0(2)	S	20	—	15	25	15	20	15	20	—	20	—	20	—	20	mA
		L	1.5	—	0.5	1.5	0.5	1.5	0.5	1.5	—	1.5	—	1.5	—	1.5	

2989 tbl 06

NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.

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DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

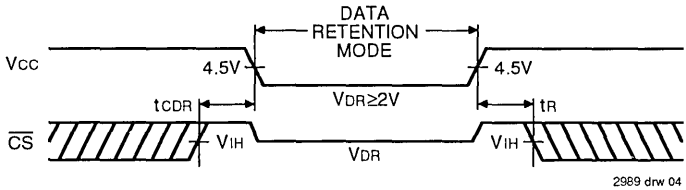
(L Version Only) V_{HC} = Vcc - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.[1] Vcc @ 2.0v	Typ.[1] Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	Vcc for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current		MIL.	—	10	15	600	900	µA
			COM'L.	—	10	15	150	225	
t_{CDR}[3]	Chip Deselect to Data Retention Time	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$		0	—	—	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	—	—	ns
$\|I_{LI}\|$[3]	Input Leakage Current			—	—	—	2	2	µA

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization but is not production tested.

2989 tbl 09

LOW Vcc DATA RETENTION WAVEFORM

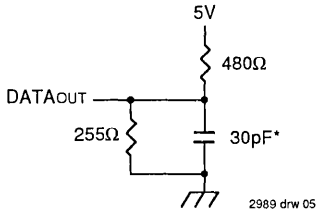


2989 drw 04

AC TEST CONDITIONS

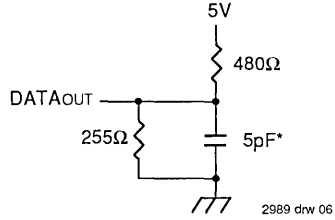
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2989 tbl 10



2989 drw 05

Figure 1. AC Test Load



2989 drw 06

Figure 2. AC Test Load (for t_{HZ}, t_{LZ}, t_{WZ}, t_{OHZ} and t_{OW})

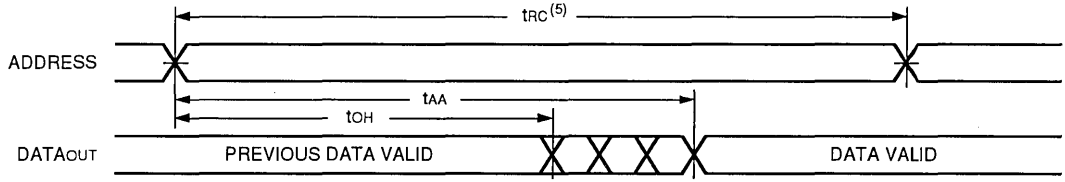
*Includes scope and jig capacitances

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7188S15[1] 7188L15[1] Min.	7188S15[1] 7188L15[1] Max.	7188S20 7188L20 Min.	7188S20 7188L20 Max.	7188S25 7188L25 Min.	7188S25 7188L25 Max.	7188S35/45 7188L35/45 Min.	7188S35/45 7188L35/45 Max.	7188S55/70[2] 7188L55/70[2] Min.	7188S55/70[2] 7188L55/70[2] Max.	7188S85[2] 7188L85[2] Min.	7188S85[2] 7188L85[2] Max.	Unit
Read Cycle														
tRC	Read Cycle Time	15	—	20	—	25	—	35/45	—	55/70	—	85	—	ns
tAA	Address Access Time	—	15	—	20	—	25	—	35/45	—	55/70	—	85	ns
tACS	Chip Select Access Time	—	15	—	20	—	25	—	35/45	—	55/70	—	85	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
tLZ	Output Selection to Output in Low Z[3]	5	—	5	—	5	—	5	—	5	—	5	—	ns
tHZ	Chip Deselect to Output in High Z[3]	—	7	—	8	—	10	—	14	—	20/25	—	30	ns
tPU	Chip Select to Power Up Time[3]	0	—	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Deselect to Power Down Time[3]	—	15	—	20	—	25	—	35/45	—	55/70	—	85	ns

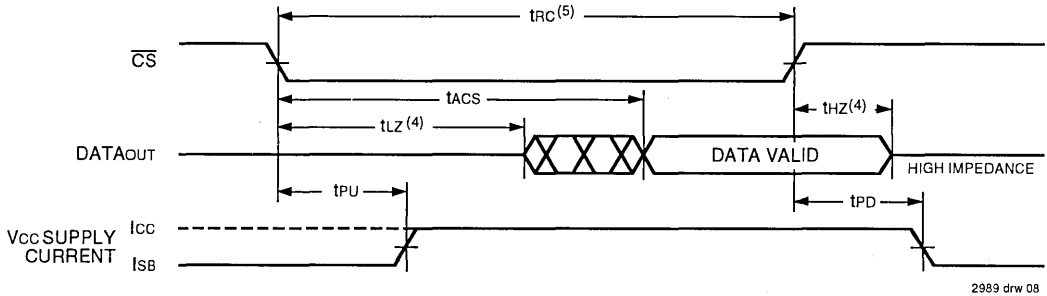
NOTES:
2989 tbl 11
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed by device characterization but is not production tested.

TIMING WAVEFORM OF READ CYCLE NO. 1[1, 2]



2989 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2[1, 3]



2989 drw 08

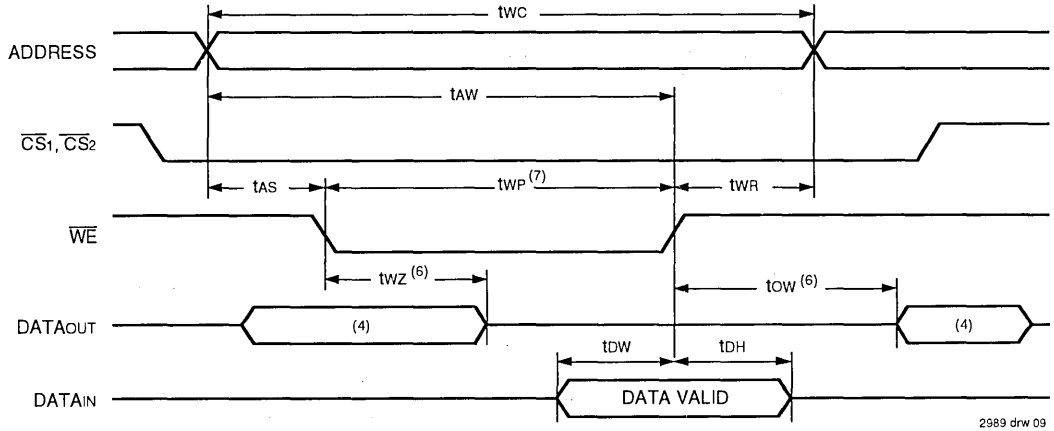
NOTES:
1. WE is high for read cycle.
2. CS is low for READ cycle.
3. Address valid prior to or coincident with CS transition low.
4. Transition is measured ±200mV from steady state voltage.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7188S15[1] 7188L15[1] Min.	Max.	7188S20 7188L20 Min.	Max.	7188S25 7188L25 Min.	Max.	7188S35/45[2] 7188L35/45[2] Min.	Max.	7188S55/70[2] 7188L55/70[2] Min.	Max.	7188S85[2] 7188L85[2] Min.	Max.	Unit
Write Cycle														
tWC	Write Cycle Time	14	—	17	—	20	—	30/40	—	50/60	—	75	—	ns
tCW	Chip Select to End of Write	14	—	17	—	20	—	25/35	—	50/60	—	75	—	ns
tAW	Address Valid to End of Write	14	—	17	—	20	—	25/35	—	50/60	—	75	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	14	—	17	—	20	—	25/35	—	50/60	—	75	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	10	—	10	—	13	—	15/20	—	25/30	—	35	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High Z[3]	—	5	—	6	—	7	—	10/15	—	25/30	—	40	ns
tOW	Output Active from End of Write[3]	5	—	5	—	5	—	5	—	5	—	5	—	ns

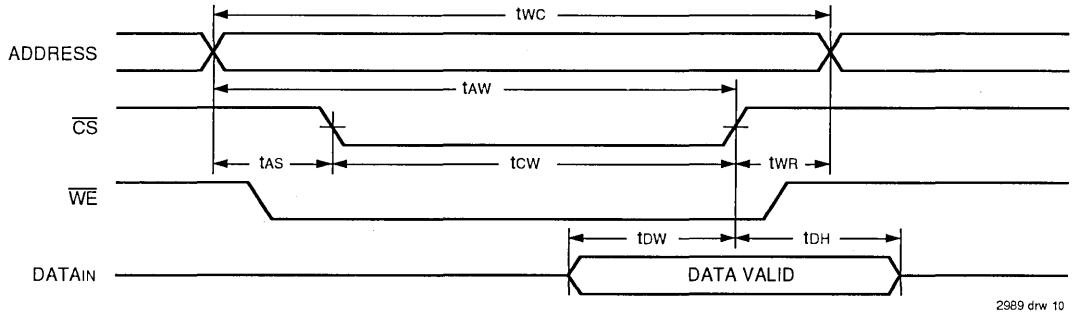
NOTES:
2989 tbl 12
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed by device characterization.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3)



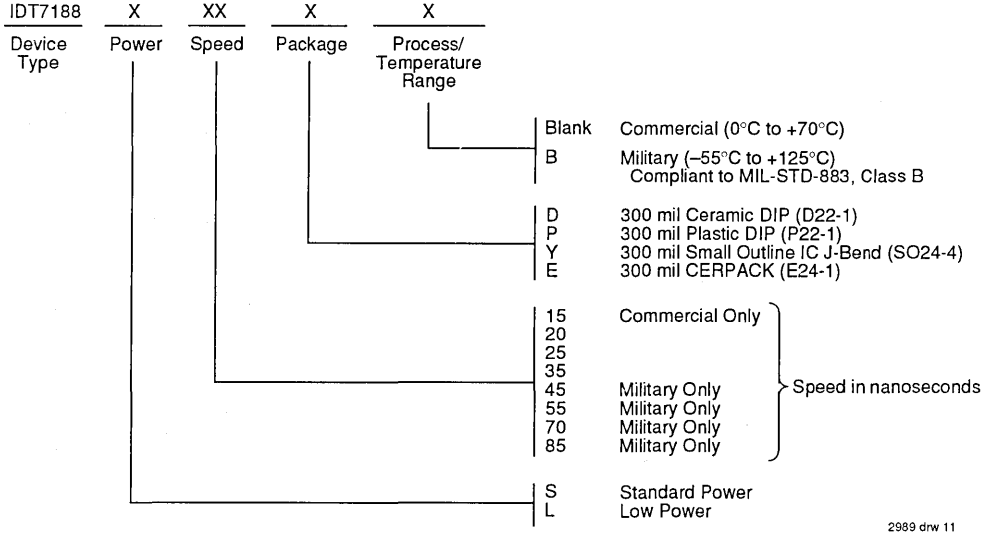
NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tWP) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals should not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high-impedance state.
6. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)[1,2,3,5]



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tWP) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals should not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high-impedance state.
6. Transition is measured ±200mV from steady state.

ORDERING INFORMATION



Integrated Device Technology, Inc.

BiCMOS STATIC RAM 64K (16K x 4-BIT)

IDT71B88

FEATURES:

- 16K x 4 BiCMOS static RAM
- High-speed address/chip select time
  — Commercial: 10/12ns
- Single chip select
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Available in 22-pin, 300 mil plastic DIP; and 24-pin, 300 mil plastic SOJ packages

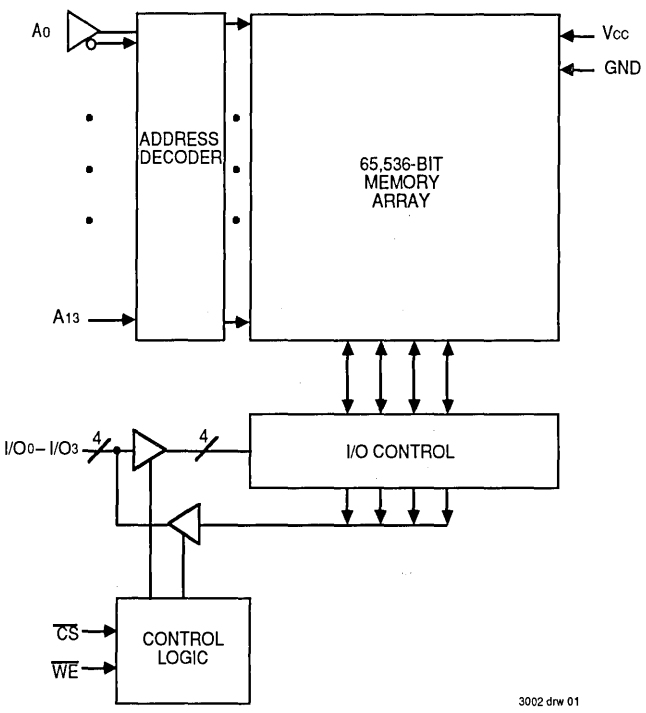
DESCRIPTION:

The IDT71B88 is a 65,536-bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-perfomance, high-reliability BiCMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

Address access times as fast as 8ns are available with power consumption of only 400mW (typ.). All inputs and outputs of the IDT71B88 are TTL-compatible, and operation is from a single 5V supply.

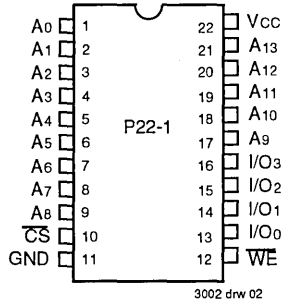
The IDT71B88 is packaged in a 22-pin, 300 mil plastic DIP and a 24-pin, 300 mil SOJ.

FUNCTIONAL BLOCK DIAGRAM



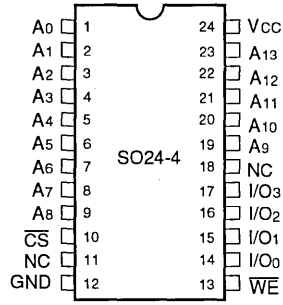
3002 drw 01

PIN CONFIGURATIONS



3002 drw 02

DIP
TOP VIEW



SOJ
TOP VIEW

3002 drw 02a

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +125	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 3002 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} must not exceed V_{CC} + 0.5V.

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	I/O	Function
L	H	$DATA_{OUT}$	Read
L	L	$DATA_{IN}$	Write
H	X	High-Z	Deselect Chip

NOTE: 3002 tbl 01

1. H = V_{IH}, L = V_{IL}, X = Don't care.

CAPACITANCE (T_A = +25°C, f = 1.0MHz, SOJ package only)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	7	pF

NOTE: 3002 tbl 03

1. This parameter is guaranteed by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage	–0.5	—	0.8	V

NOTE: 3002 tbl 04

1. VIL (Min.) = –1.5V for pulse width less than 10ns, once per cycle.

6

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71B88 Min.	IDT71B88 Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.	—	0.4	
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

3002 tbl 05

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5.0V ± 10%)

Symbol	Parameter	71B88S10 Com'l.	71B88S12 Com'l.	Unit
I_{CC}	Dynamic Operating Current, $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	180	160	mA

NOTES: 3002 tbl 05

1. All values are maximum guaranteed values.
2. fMAX = 1/tRC, all Address inputs are cycling at f_{MAX}.

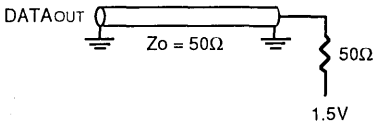
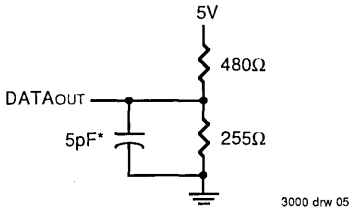


Figure 1. AC Test Load

2962 drw 04



*Including jig and scope capacitance.

Figure 2.

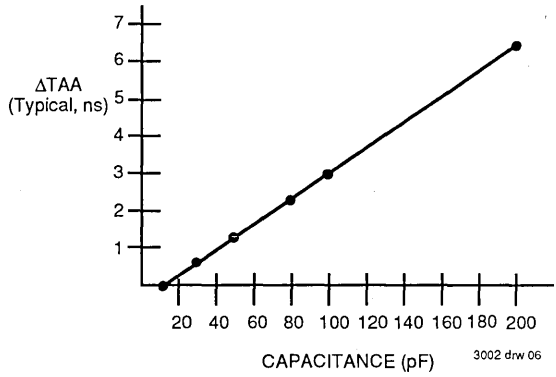


Figure 3. Lumped Capacitive Load, Typical Derating

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1, 2 & 3

3002 tbl 06

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

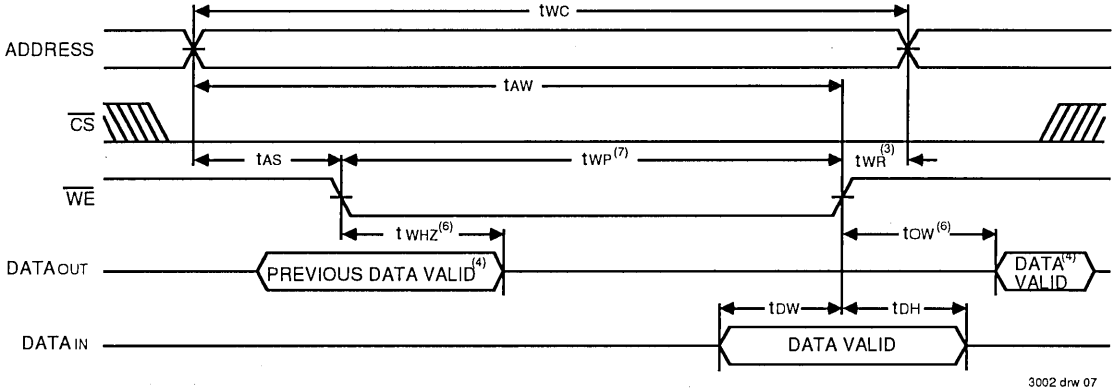
Symbol	Parameter	71B88S10 Min.	71B88S10 Max.	71B88S12 Min.	71B88S12 Max.	Unit
Read Cycle						
t_{RC}	Read Cycle Time	10	—	12	—	ns
t_{AA}	Address Access Time	—	10	—	12	ns
t_{ACS}	$\overline{CS}$ Access Time	—	6	—	7	ns
t_{CLZ}[1]	$\overline{CS}$ to Output in Low-Z	1	—	1	—	ns
t_{CHZ}[1]	$\overline{CS}$ to Output in High-Z	—	6	—	7	ns
t_{OH}	Out Hold from Address Change	3	—	3	—	ns
Write Cycle						
t_{WC}	Write Cycle Time	10	—	12	—	ns
t_{CW}	Chip Select to End-of-Write	8	—	9	—	ns
t_{AW}	Address Valid to End-of-Write	8	—	9	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	ns
t_{WP}	Write Pulse Width	8	—	9	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{WHZ}[1]	$\overline{WE}$ to Output in High-Z	—	3	—	4	ns
t_{DW}	Data Set-Up Time	5	—	6	—	ns
t_{DH}	Data Hold from Write	0	—	0	—	ns
t_{OW}[1]	Out Active from End-of-$\overline{WE}$	3	—	3	—	ns

NOTES:

3002 tbl 08

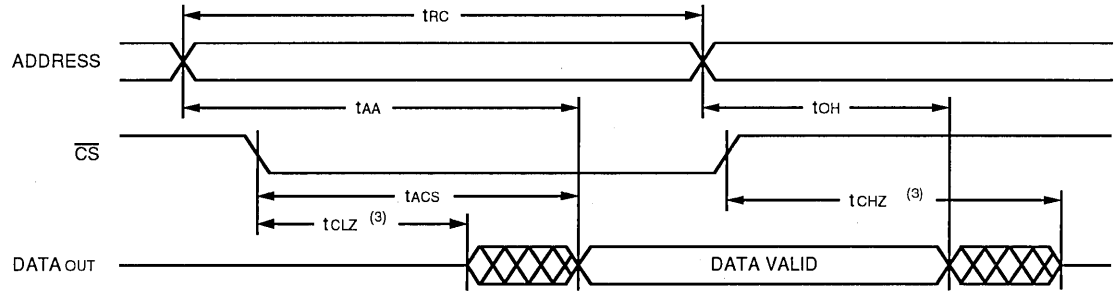
1. This parameter is guaranteed with the AC Load (Figure 2) by device chracterization, but is not production tested.

TIMING WAVEFORM OF READ CYCLE NO. 1 (1,2)



3002 drw 07

TIMING WAVEFORM OF READ CYCLE NO.2 (1,2,3)

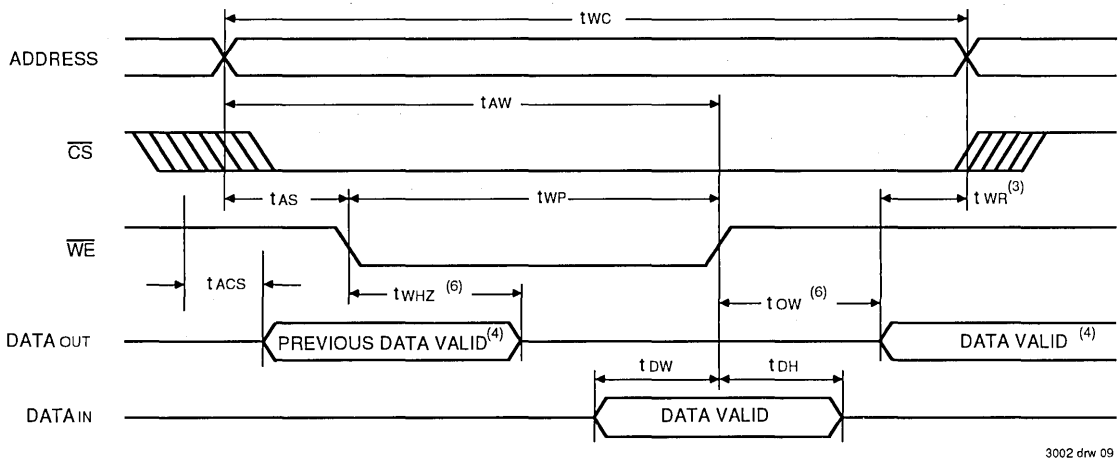


3002 drw 08

NOTES:
1. $\overline{WE}$ is HIGH for read cycle, $\overline{WE} \geq V_{IH}$.
2. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
3. Transition is measured ±200mV from steady state.

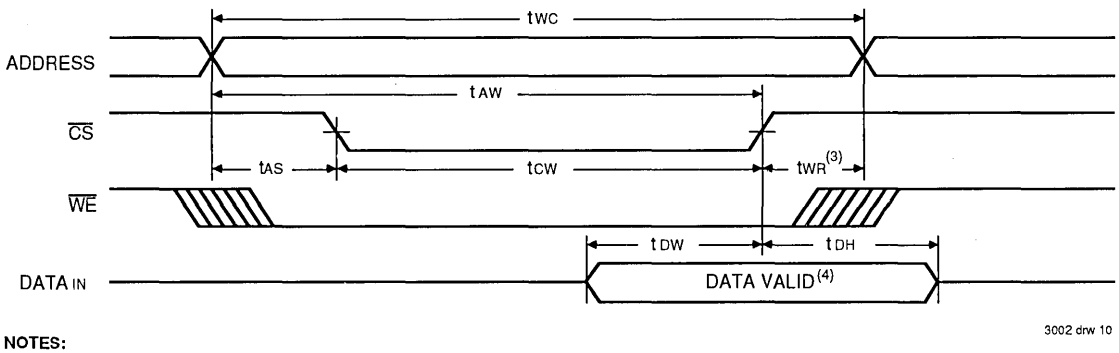
6

TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ CONTROLLED TIMING)(1,2,5)



3002 drw 09

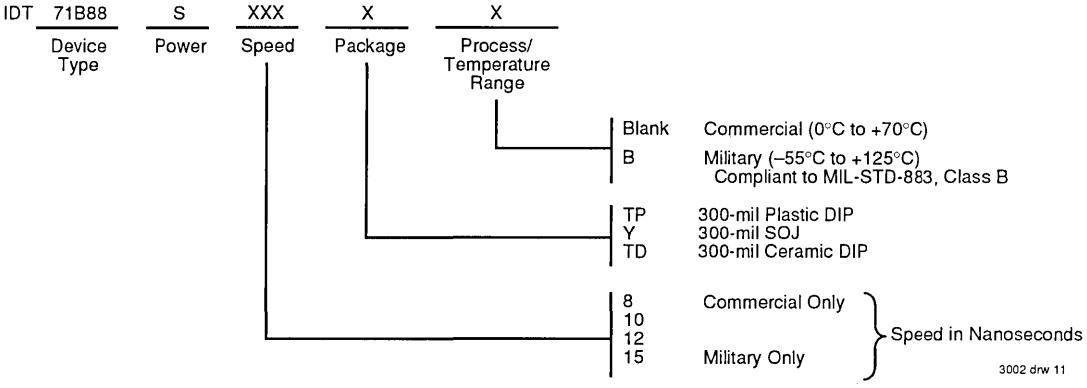
TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ CONTROLLED TIMING)(1,2,4)



3002 drw 10

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. If $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high-impedance state. If CS high transition occurs simultaneously with or before WE high transition, the outputs remain in the high-impedance state.
5. Transition is measured ±200mV from steady state.

ORDERING INFORMATION



6

Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (16K x 4-BIT) with Output Control

IDT6198S
IDT6198L

FEATURES:

- Output Enable ($\overline{OE}$) pin available for added system flexibility
- High-speed (equal access and cycle times)
  - — Military: 20/25/35/45/55/70/85ns (max.)
  - — Commercial: 15/20/25/35ns (max.)
- Low-power consumption
- JEDEC compatible pinout
- Battery back-up operation—2V data retention (L version only)
- 24-pin CERDIP, 24-pin plastic DIP, high-density 28-pin leadless chip carrier, and 24-pin SOJ
- Produced with advanced CMOS technology
- Bidirectional data inputs and outputs
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT6198 is a 65,536-bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective approach for memory intensive applications. Timing parameters have been specified to meet the speed demands of the IDT79R3000 RISC processors.

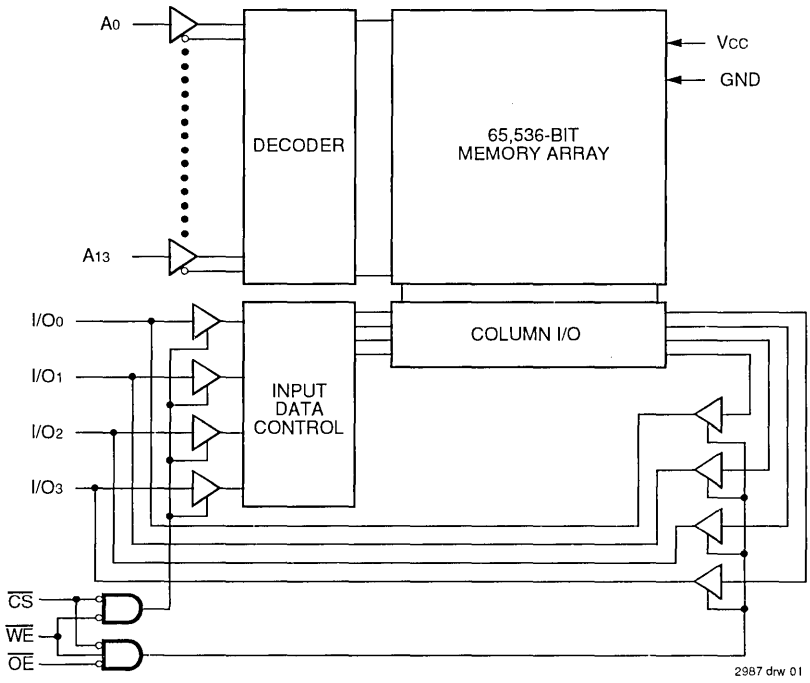
Access times as fast as 15ns are available. The IDT6198 offers a reduced power standby mode, I_{SB1}, which is activated when $\overline{CS}$ goes HIGH. This capability significantly decreases system, while enhancing system reliability. The low-power version (L) also offers a battery backup data retention capability where the circuit typically consumes only 30µW when operating from a 2 volt battery.

All inputs and outputs are TTL-compatible and operate from a single 5 volt supply.

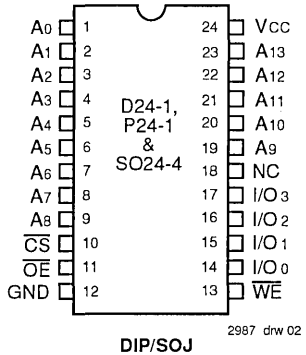
The IDT6198 is packaged in either a 24-pin 300 mil CERDIP or plastic DIP, 28-pin leadless chip carrier or 24-pin J-bend small outline IC.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

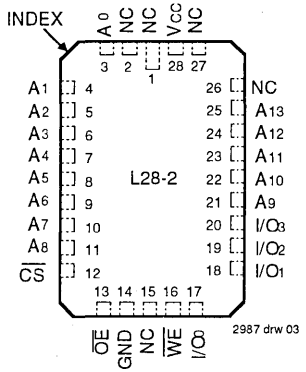
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP/SOJ
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A_0–A_{13}	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O_0–I/O_3	Data Input/Output
V_{CC}	Power
GND	Ground

2937 tbl 01

TRUTH TABLE[1]

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Standby	H	X	X	High-Z	Standby
Read	L	H	L	$DATA_{OUT}$	Active
Write	L	L	X	$DATA_{IN}$	Active
Read	L	H	H	High-Z	Active

NOTE: 2987 tbl 02
1. H = V_{IH}, L = V_{IL}, X = Don't Care

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2987 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 2987 tbl 04
1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

2987 tbl 05

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns, once per cycle.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2987 tbl 06

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT6198S Min.	IDT6198S Max.	IDT6198L Min.	IDT6198L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	—	10	—	5	µA
			COM'L.	—	5	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	—	10	—	5	µA
			COM'L.	—	5	—	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.			0.5	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.		2.4	—	2.4	—	V

2967 tbl 07

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	6198S15 6198L15 Com'l.	6198S15 6198L15 Mil.	6198S20 6198L20 Com'l.	6198S20 6198L20 Mil.	6198S25 6198L25 Com'l.	6198S25 6198L25 Mil.	6198S35 6198L35 Com'l.	6198S35 6198L35 Mil.	6198S45 6198L45 Com'l.	6198S45 6198L45 Mil.	6198S55/70/85 6198L55/70/85 Com'l.	6198S55/70/85 6198L55/70/85 Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = 0[2]	S	100	—	100	105	100	105	100	105	—	105	—	105	mA
		L	75	—	70	80	70	80	70	80	—	80	—	80	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = f_{MAX}[2]	S	135	—	130	160	125	155	125	140	—	140	—	140	mA
		L	125	—	115	130	105	120	105	115	—	110	—	110	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}[2]	S	60	—	55	70	50	60	45	50	—	50	—	50	mA
		L	45	—	40	50	35	40	30	35	—	35	—	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC}=Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0[2]	S	20	—	15	25	15	20	15	20	—	20	—	20	mA
		L	1.5	—	0.5	1.5	0.5	1.5	0.5	1.5	—	1.5	—	1.5	

2987 tbl 06

NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

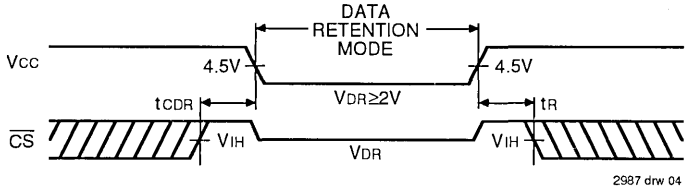
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ. (1) Vcc @ 2.0v	Typ. (1) Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	—	10	15	600	900	µA
			COM'L.	—	10	15	150	225	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	—	—	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	—	—	ns
$\|I_{LI}\|$(3)	Input Leakage Current			—	—	—	2	2	µA

2967 tbl 09

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization but is not production tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2987 tbl 10

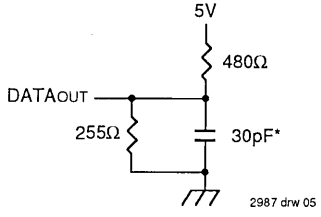


Figure 1. AC Test Load

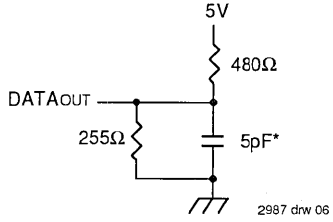


Figure 2. AC Test Load
(for t_{OLZ}, t_{CLZ}, t_{OHZ}, t_{WHZ}, t_{CHZ} and t_{OW})

*Includes scope and jig capacitances

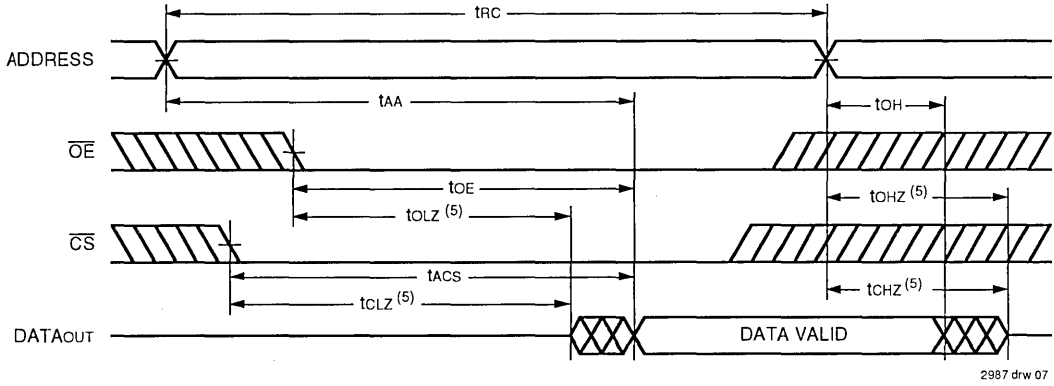
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6198S15[1] 6198L15[1] Min.	6198S15[1] 6198L15[1] Max.	6198S20 6198L20 Min.	6198S20 6198L20 Max.	6198S25 6198L25 Min.	6198S25 6198L25 Max.	6198S35 6198L35 Min.	6198S35 6198L35 Max.	6198S45/55[2] 6198L45/55[2] Min.	6198S45/55[2] 6198L45/55[2] Max.	6198S70/85[2] 6198L70/85[2] Min.	6198S70/85[2] 6198L70/85[2] Max.	Unit
Read Cycle														
tRC	Read Cycle Time	15	—	20	—	25	—	35	—	45/55	—	70/85	—	ns
tAA	Address Access Time	—	15	—	19	—	25	—	35	—	45/55	—	70/85	ns
tACS	Chip Select Access Time	—	15	—	20	—	25	—	35	—	45/55	—	70/85	ns
tCLZ	Chip Select to Output in Low Z[3]	5	—	5	—	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	8	—	9	—	11	—	18	—	25/35	—	45/55	ns
tOLZ	Output Enable to Output in Low Z[3]	5	—	5	—	5	—	5	—	5	—	5	—	ns
tCHZ	Chip Select to Output in High Z[3]	2	7	2	8	2	10	2	14	—	15/20	—	25/30	ns
tOHZ	Output Disable to Output in High Z[3]	2	7	2	8	2	9	2	15	—	15/20	—	25/30	ns
tOH	Output Hold from Address Change	5	—	5	—	2	—	5	—	5	—	5	—	ns
tPU	Chip Select to Power Up Time[3]	0	—	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Deselect to Power Down Time[3]	—	15	—	20	—	25	—	35	—	45/55	—	70/85	ns

NOTES:
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed by device characterization but is not production tested.

2987 tbl 11

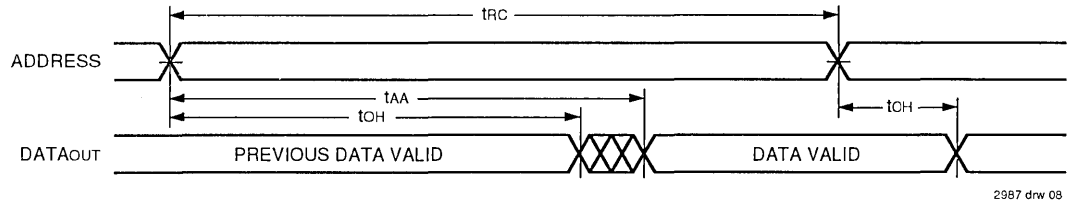
TIMING WAVEFORM OF READ CYCLE NO. 1[1]



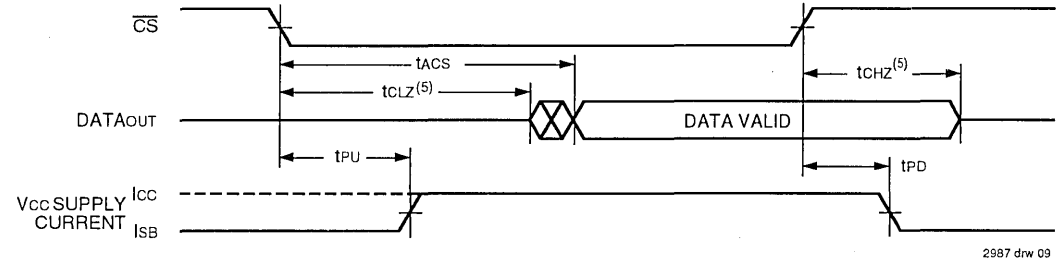
2987 drw 07

NOTES:
1. WE is high for Read cycle.
2. Device is continuously selected, CS = VIL.
3. Address valid prior to or coincident with CS transition low.
4. OE = VIL.
5. Transition is measured ±200mV from steady state voltage.

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



NOTES:
1. $\overline{WE}$ is high for Read cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state voltage.

6

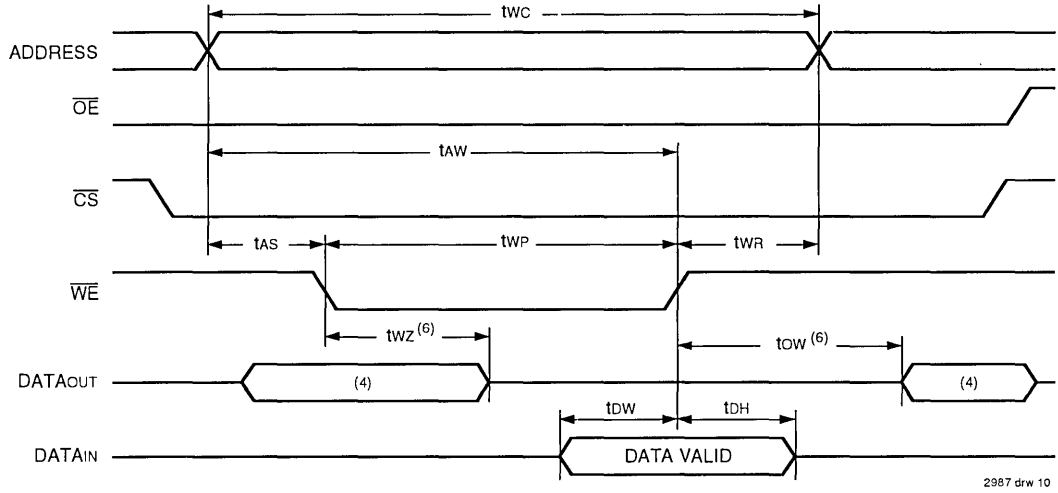
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6198S15[1] 6198L15[1] Min.	Max.	6198S20 6198L20 Min.	Max.	6198S25 6198L25 Min.	Max.	6198S35 6198L35 Min.	Max.	6198S45/55[2] 6198L45/55[2] Min.	Max.	6198S70/85[2] 6198L70/85[2] Min.	Max.	Unit
Write Cycle														
twc	Write Cycle Time	14	—	17	—	20	—	30	—	40/50	—	60/75	—	ns
tcw	Chip Select to End of Write	14	—	17	—	20	—	25	—	35/50	—	60/75	—	ns
taw	Address Valid to End of Write	14	—	17	—	20	—	25	—	35/50	—	60/75	—	ns
tas	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
twp	Write Pulse Width	14	—	17	—	20	—	25	—	35/50	—	60/75	—	ns
twr	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
twhz	Write Enable to Output in High Z[3]	—	5	—	6	—	7	—	10	—	15/25	—	30/40	ns
tdw	Data Valid to End of Write	10	—	10	—	13	—	15	—	20/25	—	30/35	—	ns
tdh	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tow	Output Active from End of Write[3]	5	—	5	—	5	—	5	—	5	—	5	—	ns

2987 tbl 12

NOTES:
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed by device characterization, but is not production tested.

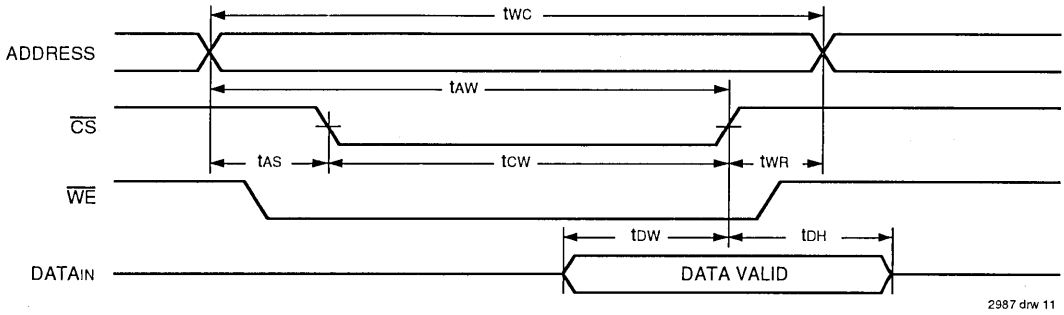
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3, 7]



2987 drw 10

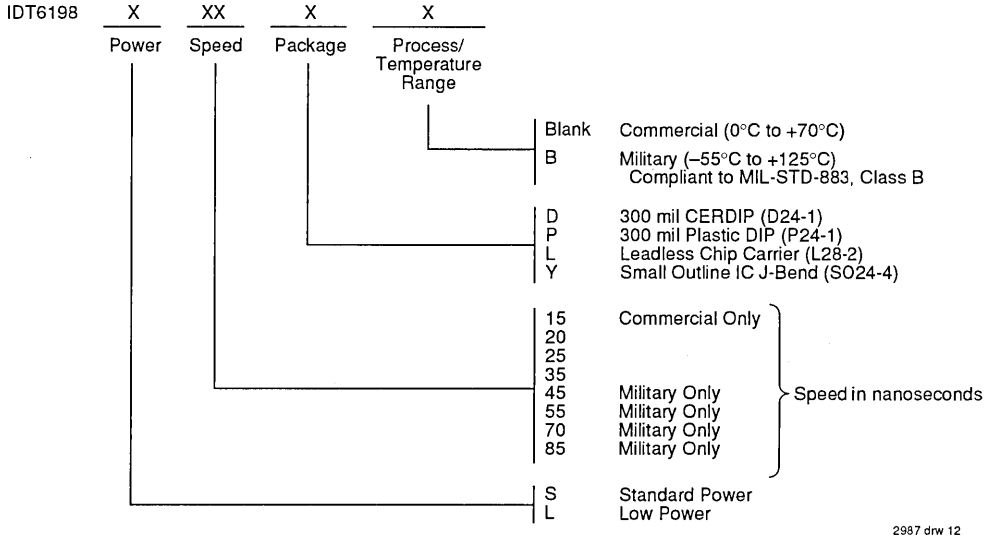
NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tcw twp) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. twr is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of twp or (twhz + tdw) to allow the I/O drivers to turn off and data to be placed on the bus for the required tdw. If $\overline{OE}$ is high an $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified twp.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tCW tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high an $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

ORDERING INFORMATION



Integrated Device Technology, Inc.

BiCMOS STATIC RAM 64K (16K x 4-BIT)

IDT61B98

FEATURES:

- 16K x 4 BiCMOS Static RAM
- High-speed address access time
  - — Commercial: 8/10/12ns
- Fast Output Enable
  - — Commercial: 4/5/6ns
- Input and output directly TTL-compatible
- Available in 24-pin, 300 mil plastic DIP and 24-pin, 300-mil plastic SOJ

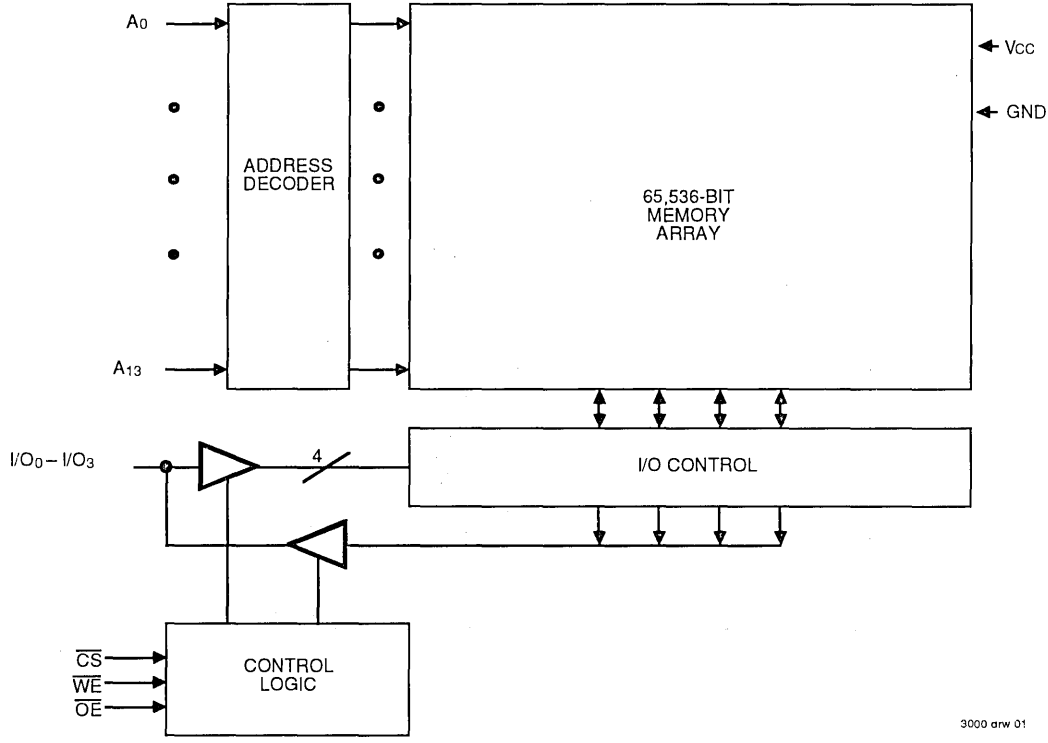
DESCRIPTION:

The IDT61B98 is a 65,536-bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-perfomance, high-reliability BiCMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

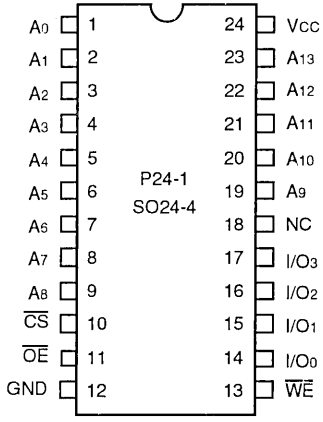
Address access times as fast as 8ns (SOJ package only) are available with power consumption of only 400mW (typ.). All inputs and outputs of the IDT61B98 are TTL-compatible.

The IDT61B98 is packaged in a 24-pin, 300 mil plastic DIP and a 24-pin, 300 mil SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



3000 drw 02

DIP/SOJ
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	°C
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +125	°C
PT	Power Dissipation	1.25	1.25	W
IOUT	DC Output Current	50	50	mA

2958 tbl 02

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VIN pins must not exceed VCC + 0.5V.

TRUTH TABLE(1)

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
H	X	X	High-Z	Deselect Chip
L	L	H	DATAOUT	Read Cycle
L	X	L	DATAIN	Write Cycle
L	H	H	High-Z	Outputs Disabled

NOTE:
1. H = VIH, L = VIL, X = Don't care.

3000 tbl 01

CAPACITANCE

(TA = +25°C, f = 1.0MHz, SOJ package only)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	6	pF
COUT	Output Capacitance	VOUT = 3dV	7	pF

NOTE:
1. This parameter is guaranteed by device characterization, but is not production tested.

3000 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	VCC + 0.5	V
VIL	Input Low Voltage	–0.5	—	0.8	V

NOTE:
1. VIL (Min.) = –1.5 for pulse width less than 10ns, once per cycle.

3000 tbl 04

DC ELECTRICAL CHARACTERISTICS (VCC = 5.0V ± 10%)

Symbol	Parameter	Test Condition	IDT61B98 Min.	IDT61B98 Max.	Unit
|ILI|	Input Leakage Current	VCC = Max., VIN = GND to VCC	—	5	µA
|ILO|	Output Leakage Current	VCC = Max., $\overline{CS}$ = VIH, VOUT = GND to VCC	—	5	µA
VOL	Output LOW Voltage	IOL = 10mA, VCC = Min.	—	0.5	V
		IOL = 8mA, VCC = Min.	—	0.4	
VOH	Output HIGH Voltage	IOH = –4mA, VCC = Min.	2.4	—	V

3000 tbl 05

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5.0V ± 10%, V_{IL} = 0.2V)

Symbol	Parameter	61B98S8(3) Com'l.	61B98S10 Com'l.	61B98S12 Com'l.	61B98S15 Com'l.	Unit
I_{CC}	Dynamic Operating Current, $\overline{CS} \leq V_{IL}$ Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	200	180	160	—	mA

3000 tbl 05

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/tRC, all address inputs are cycling at f_{MAX}.
3. Available in SOJ package only.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1, 2, and 3

3000 tbl 06

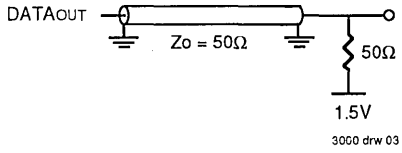
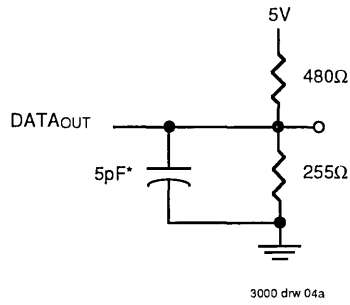


Figure 1. AC Test Load



*Including jig and scope capacitance.

Figure 2. AC Test Load (for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{WHZ}, and t_{OW})

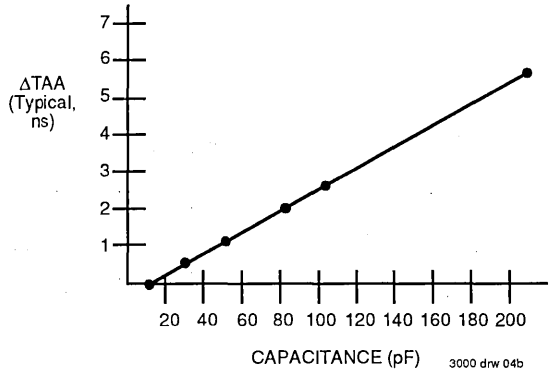


Figure 3. Lumped Capacitive Load, Typical Derating

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%)

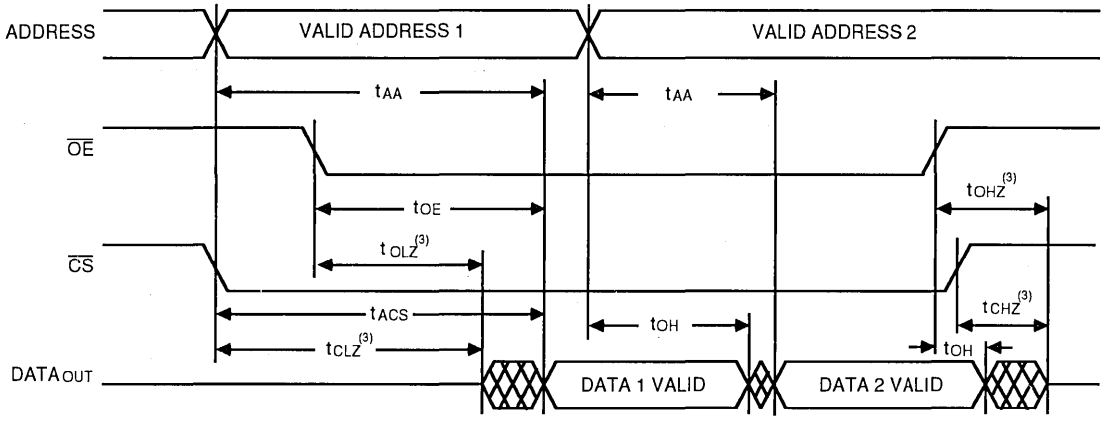
Symbol	Parameter	61B98S8		61B98S10		61B98S12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	8	—	10	—	12	—	ns
t_{AA}	Address Access Time	—	8	—	10	—	12	ns
t_{CLZ}[1]	$\overline{CS}$ to Output in Low-Z	1	—	1	—	1	—	ns
t_{CHZ}[1]	$\overline{CS}$ to Output in High-Z	—	6	—	6	—	7	ns
t_{ACS}	$\overline{CS}$ Access Time	—	6	—	7	—	7	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	4	—	5	—	6	ns
t_{OLZ}[1]	$\overline{OE}$ to Output Low-Z	1	—	1	—	1	—	ns
t_{OHZ}[1]	$\overline{OE}$ to Output High-Z	—	3	—	3	—	3	ns
t_{OH}	Out Hold from Add Change	3	—	3	—	3	—	ns
t_{WC}	Write Cycle Time	8	—	10	—	12	—	ns
t_{AW}	Address to End-of-Write	8	—	8	—	9	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	8	—	8	—	9	—	ns
t_{CW}	$\overline{CS}$ to End-of-Write	8	—	8	—	9	—	ns
t_{WR}	Write Recovery	0	—	0	—	0	—	ns
t_{WHZ}[1]	$\overline{WE}$ to Out in High-Z	—	3	—	3	—	3	ns
t_{DW}	Data Setup	5	—	5	—	6	—	ns
t_{DH}	Data Hold	0	—	0	—	0	—	ns
t_{OW}[1]	Output from End-of-Write	3	—	3	—	3	—	ns

NOTE:
1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

3000 tbl 08

6

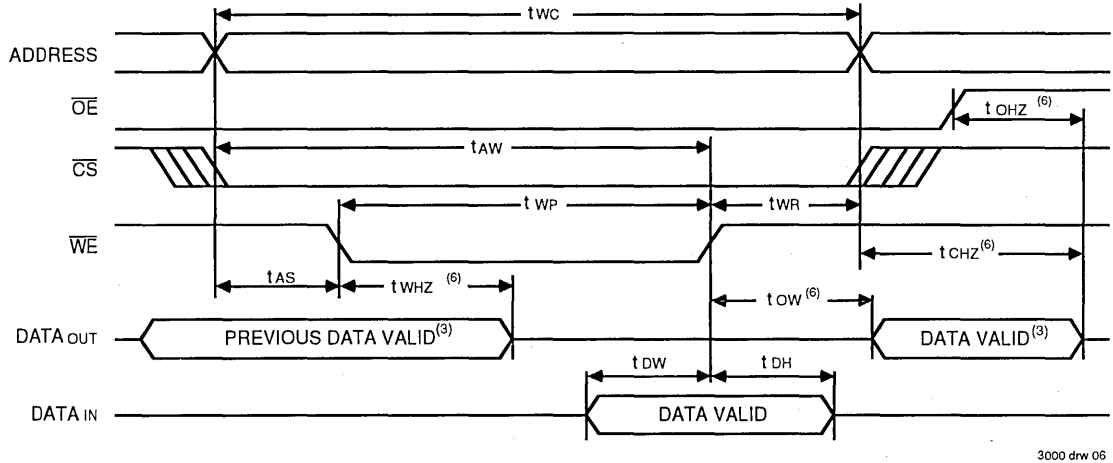
TIMING WAVEFORM OF READ CYCLE[1,2]



3000 drw 05

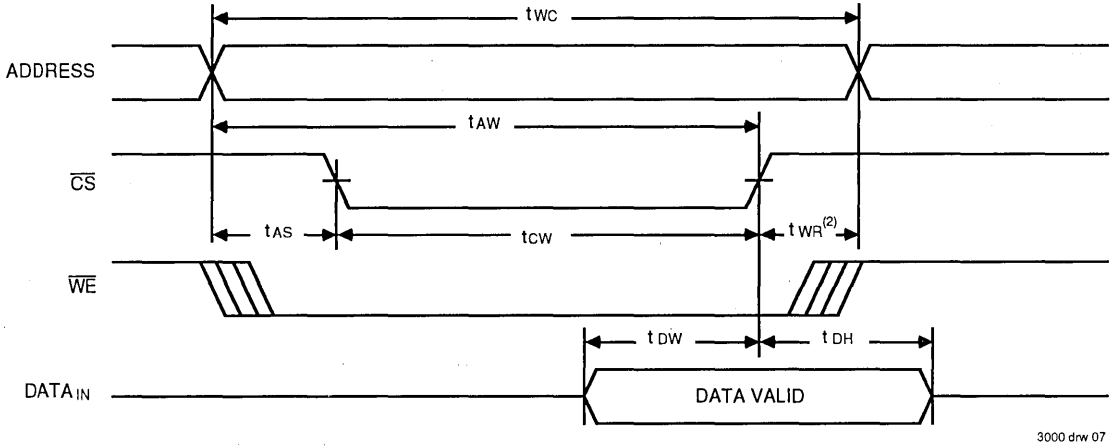
NOTES:
1. $\overline{WE}$ is HIGH for read cycle, $\overline{WE} \geq V_{IH}$.
2. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
3. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ CYCLE)(1, 2, 4, 5)



3000 drw 06

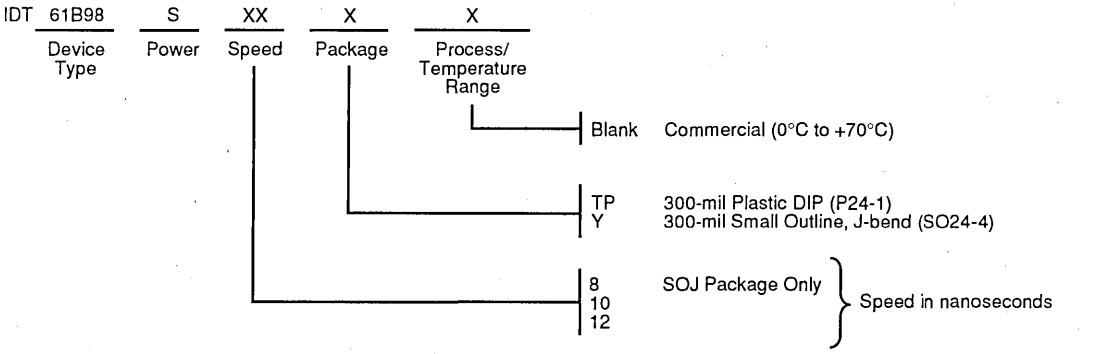
TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ CYCLE)(1, 4, 5)



3000 drw 07

NOTES:
1. A write occurs during the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
3. During this period, the I/O pins are in the output state and input signals must not be applied.
4. If $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in the high-impedance state. Likewise, if $\overline{CS}$ HIGH transition occurs simultaneously with or before $\overline{WE}$ HIGH transition, the outputs remain in the high-impedance state.
5. $\overline{OE}$ is continuously HIGH. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse is the specified t_{WP}. For a $\overline{CS}$ controlled write cycle, $\overline{OE}$ may be LOW with no degradation to t_{CW}.
6. The transition is measured ±200mV from steady state.

ORDERING INFORMATION



3000 drw 08

6

Integrated Device Technology, Inc.

CMOS STATIC RAMs 64K (16K x 4-BIT) Added Chip Select and Output Controls

IDT7198S
IDT7198L

FEATURES:

- Fast Output Enable ($\overline{OE}$) pin available for added system flexibility
- Multiple Chip Selects ($\overline{CS_1}$, $\overline{CS_2}$) simplify system design and operation
- High speed (equal access and cycle times)
  - — Military: 20/25/35/45/55/70/85ns (max.)
  - — Commercial: 15/20/25/35ns (max.)
- Low power consumption
- Battery back-up operation—2V data retention (L version only)
- 24-pin CERDIP, 24-pin plastic DIP, high-density 28-pin leadless chip carrier, 24-pin SOJ and CERPACK
- Produced with advanced CMOS technology
- Bidirectional data inputs and outputs
- Inputs/outputs TTL-compatible
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7198 is a 65,536 bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for memory intensive applications. Timing parameters have been specified to meet the speed demands of the IDT79R3000 RISC processors.

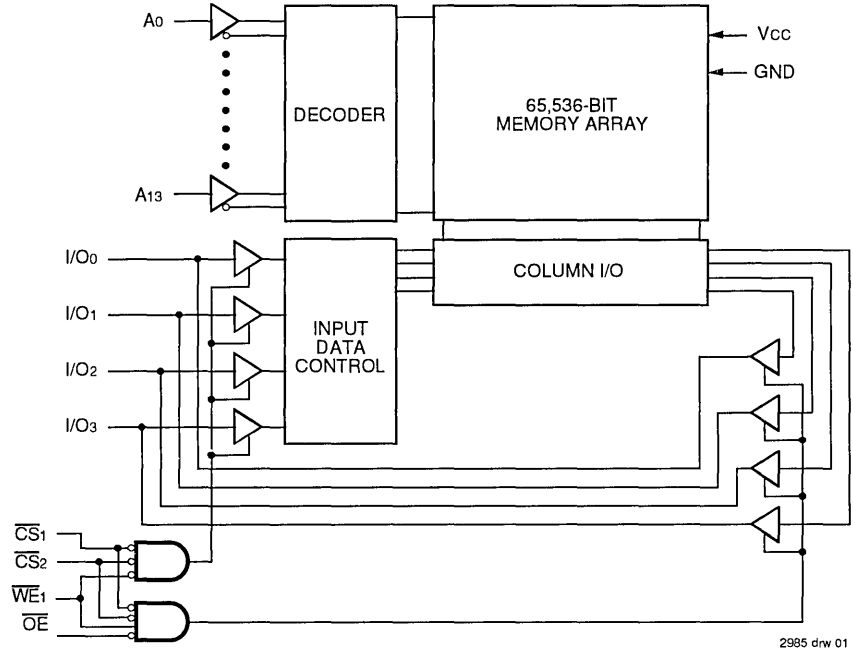
Access times as fast as 15ns are available. The IDT7198 offers a reduced power standby mode, I_{SB1}, which is activated when $\overline{CS_1}$ or $\overline{CS_2}$ goes high. This capability decreases power, while enhancing system reliability. The low-power version (L)also offers a battery backup data retention capability where the circuit typically consumes only 30µW when operating from a 2V battery.

All inputs and outputs are TTL-compatible and operate from a single 5 volt supply.

The IDT7198 is packaged in either a 24-pin ceramic DIP, 24-pin plastic DIP, 28-pin leadless chip carrier, 24-pin SOJ and 24-pin CERPACK.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



MEMORY CONTROL

The IDT7198 64K high-speed CEMOS static RAM incorporates two additional memory control features (an extra chip select and an output enable pin) which offer additional benefits in many system memory applications.

The dual chip select feature ($\overline{CS_1}$, $\overline{CS_2}$) now brings the convenience of improved system speeds to the large memory designer by reducing the external logic required to perform decoding.

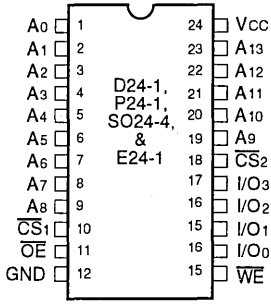
Both chip selects, Chip Select 1 ($\overline{CS_1}$) and Chip Select 2 ($\overline{CS_2}$), must be in the active-low state to select the memory. If either chip select is pulled high, the memory will be deselected and remain in the standby mode.

PIN DESCRIPTIONS

Name	Description
A0–A13	Address Inputs
$\overline{CS_1}$	Chip Select 1
$\overline{CS_2}$	Chip Select 2
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O0–I/O3	Data I/O
VCC	Power
GND	Ground

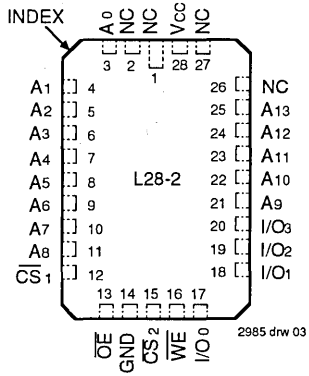
2985 tbl 01

PIN CONFIGURATIONS



2985 drw 02

DIP/SOJ/CERPACK
TOP VIEW



2985 drw 03

LCC
TOP VIEW

TRUTH TABLE[1]

Mode	$\overline{CS_1}$	$\overline{CS_2}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Standby	H	X	X	X	High Z	Standby
Standby	X	H	X	X	High Z	Standby
Read	L	L	H	L	DOUT	Active
Write	L	L	L	X	DIN	Active
Read	L	L	H	H	High Z	Active

NOTE:
1. H = VIH, L = VIL, X = don't care.

2985 tbl 02

6

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2985 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz, V_{CC} = 0V)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 2985 tbl 04

1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2985 tbl 05

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns, once per cycle.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2985 tbl 06

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT7198S Min.	IDT7198S Max.	IDT7198L Min.	IDT7198L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL. COM'L.	— —	10 5	— —	5 2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL. COM'L.	— —	10 5	— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.			0.5	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	2.4	—	V

2985 tbl 07

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	7198S15 7198L15 Com'l.	7198S15 7198L15 Mil.	7198S20 7198L20 Com'l.	7198S20 7198L20 Mil.	7198S25 7198L25 Com'l.	7198S25 7198L25 Mil.	7198S35 7198L35 Com'l.	7198S35 7198L35 Mil.	7198S45 7198L45 Com'l.	7198S45 7198L45 Mil.	7198S55/70 7198L55/70 Com'l.	7198S55/70 7198L55/70 Mil.	7198S85 7198L85 Com'l.	7198S85 7198L85 Mil.	Unit
I_{CC1}	Operating Power Supply Current, $\overline{CS_1}$ and $\overline{CS_2} \le V_{IL}$, Outputs Open V_{CC} = Max., f = 0[2]	S	100	—	100	105	100	105	100	105	—	105	—	105	—	105	mA
		L	75	—	70	80	70	80	70	80	—	80	—	80	—	80	
I_{CC2}	Dynamic Operating Current, $\overline{CS_1}$ and $\overline{CS_2} \le V_{IL}$, Outputs Open V_{CC} = Max., f = f_{MAX}[2]	S	135	—	130	160	125	155	125	140	—	140	—	140	—	140	mA
		L	125	—	115	130	105	120	105	115	—	110	—	110	—	105	
I_{SB}	Standby Power Supply Current (TTL Level), $\overline{CS_1}$ or $\overline{CS_2} \ge V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}[2]	S	60	—	55	70	50	60	45	50	—	50	—	50	—	50	mA
		L	45	—	40	50	35	40	30	35	—	35	—	35	—	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS_1}$ or $\overline{CS_2} \ge V_{HC}$, V_{CC}= Max., $V_{IN} \ge V_{HC}$ or $V_{IN} \le V_{LC}$, f = 0[2]	S	20	—	15	25	15	20	15	20	—	20	—	20	—	20	mA
		L	1.5	—	0.5	1.5	0.5	1.5	0.5	1.5	—	1.5	—	1.5	—	1.5	

NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.

2985 tbl 06

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

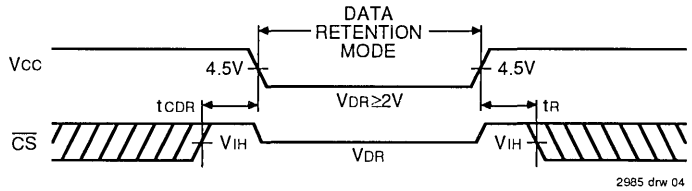
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.[1] V_{CC} @ 2.0v	Typ.[1] V_{CC} @ 3.0V	Max. V_{CC} @ 2.0V	Max. V_{CC} @ 3.0V	Unit
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS_1}$ or $\overline{CS_2} \ge V_{HC}$ $V_{IN} \ge V_{HC}$ or $\le V_{LC}$	MIL.	—	10	15	600	900	µA
			COM'L.	—	10	15	150	225	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	—	—	ns
$\|I_{LI}\|$[3]	Input Leakage Current			—	—	—	2	2	µA

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization but is not production tested.

2985 tbl 09

LOW V_{CC} DATA RETENTION WAVEFORM



2985 drw 04

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2985 tbl 10

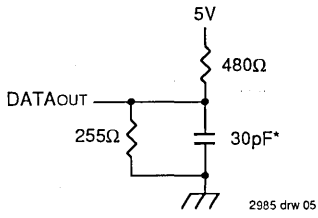


Figure 1. AC Test Load

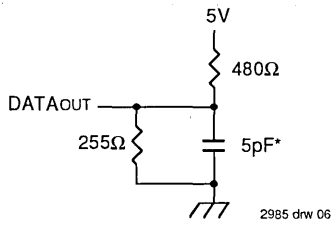


Figure 2. AC Test Load
(for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW} and t_{WHZ})

*Includes scope and jig capacitances

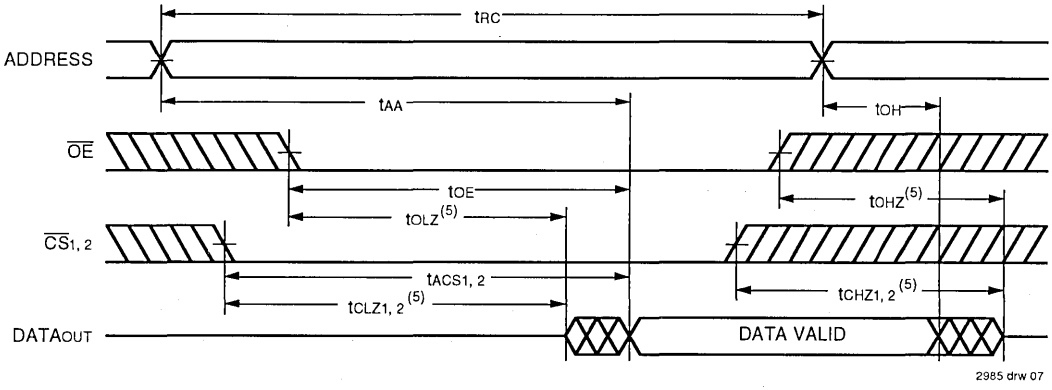
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7198S15[1]/20 7198L15[1]/20 Min.	Max.	7198S25 7198L25 Min.	Max.	7198S35/45[2] 7198L35/45[2] Min.	Max.	7198S55[2] 7198L55[2] Min.	Max.	7198S70[2] 7198L70[2] Min.	Max.	7198S85[2] 7198L85[2] Min.	Max.	Unit
Read Cycle														
t_{RC}	Read Cycle Time	15/20	—	25	—	35/45	—	55	—	70	—	85	—	ns
t_{AA}	Address Access Time	—	15/19	—	25	—	35/45	—	55	—	70	—	85	ns
$t_{ACS1,2}$	Chip Select-1,2 Access Time[3]	—	15/20	—	25	—	35/45	—	55	—	70	—	85	ns
$t_{CLZ1,2}$	Chip Select-1,2 to Output in Low Z[4]	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	8/9	—	11	—	20/25	—	35	—	45	—	55	ns
t_{OLZ}	Output Enable to Output in Low Z[4]	5	—	5	—	5	—	5	—	5	—	5	—	ns
$t_{CHZ1,2}$	Chip Select 1,2 to Output in High Z[4]	—	7/8	—	10	—	14	—	20	—	25	—	30	ns
t_{OHZ}	Output Disable to Output in High Z[4]	—	7/8	—	9	—	15	—	20	—	25	—	30	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}	Chip Select to Power Up Time[4]	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Deselect to Power Down Time[4]	—	15/20	—	25	—	35/45	—	55	—	70	—	85	ns

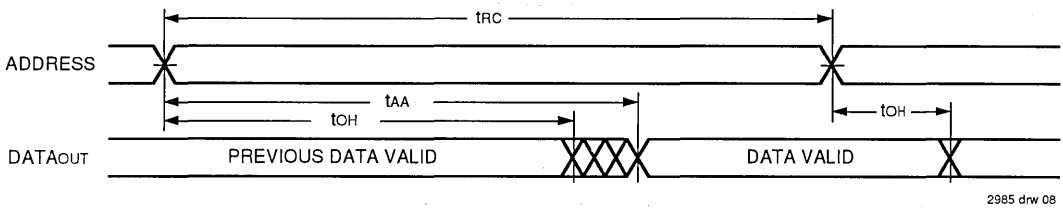
NOTES:
2985 tbl 11

1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Both chip selects must be active low for the device to be selected.
4. This parameter is guaranteed by device characterization but is not production tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1)

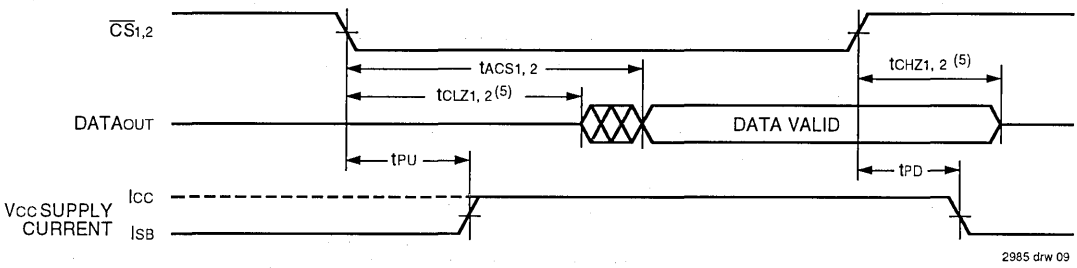


TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



6

TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



NOTES:
1. $\overline{WE}$ is HIGH for READ cycle.
2. Device is continuously selected, $\overline{CS_1} = V_{IL}$, $\overline{CS_2} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS_1}$ and or $\overline{CS_2}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ±200mV from steady state voltage.

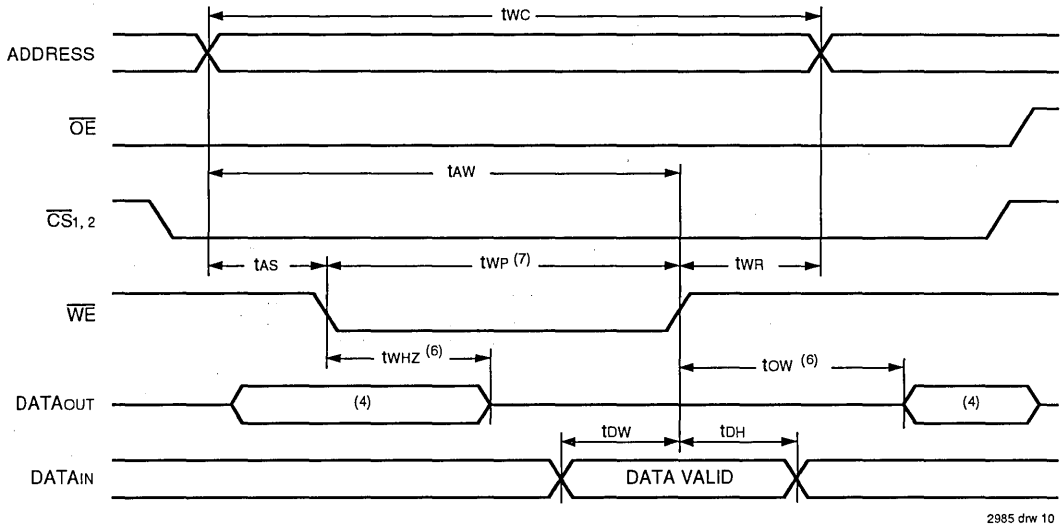
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7198S15[1]/20 7198L15[1]/20 Min.	Max.	7198S25 7198L25 Min.	Max.	7198S35/45[2] 7198L35/45[2] Min.	Max.	7198S55[2] 7198L55[2] Min.	Max.	7198S70[2] 7198L70[2] Min.	Max.	7198S85[2] 7198L85[2] Min.	Max.	Unit
Write Cycle														
tWC	Write Cycle Time	14/17	—	20	—	30/40	—	50	—	60	—	75	—	ns
tCW1,2	Chip Select to End-of-Write[3]	14/17	—	20	—	25/35	—	50	—	60	—	75	—	ns
tAW	Address Valid to End-of-Write	14/17	—	20	—	25/35	—	50	—	60	—	75	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	14/17	—	20	—	25/35	—	50	—	60	—	75	—	ns
tWR1,2	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWHZ	Write Enable to Output in High-Z[4]	—	5/6	—	7	—	10/15	—	25	—	30	—	40	ns
tDW	Data Valid to End-of-Write	10	—	13	—	15/20	—	25	—	30	—	35	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tOW	Output Active from End-of-Write[4]	5	—	5	—	5	—	5	—	5	—	5	—	ns

NOTES:
2985 tbl 12

1. 0° to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. Both chip selects must be active low for the device to be selected.
4. This parameter is guaranteed by device characterization but is not production tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3, 7]

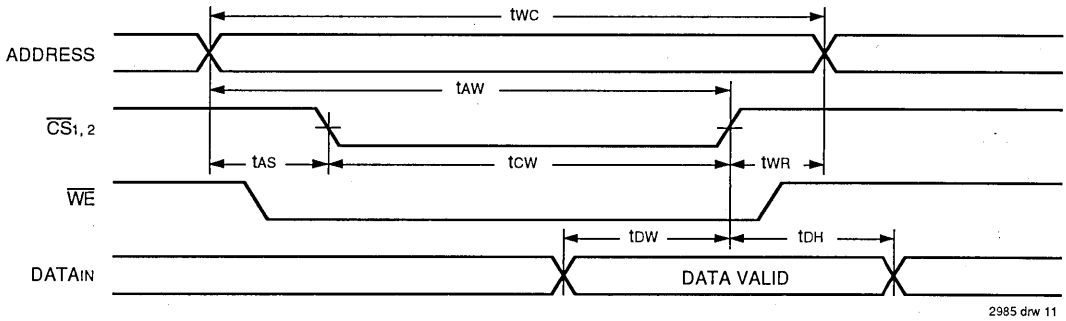


2985 drw 10

NOTES:

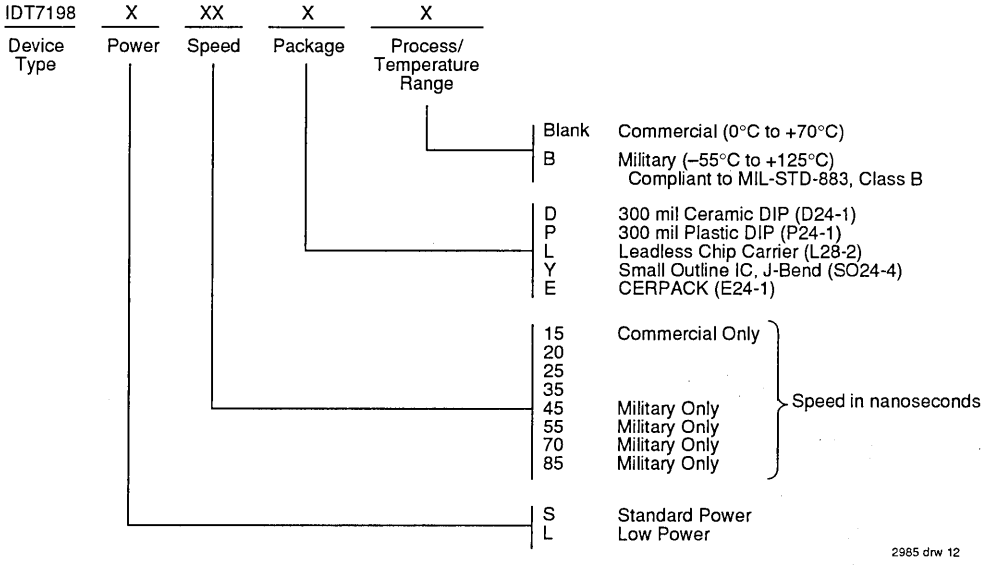
1. $\overline{WE}$, $\overline{CS_1}$ or $\overline{CS_2}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tWP) of a LOW $\overline{WE}$, a low $\overline{CS_1}$ and a LOW $\overline{CS_2}$.
3. tWR is measured from the earlier of $\overline{CS_1}$, $\overline{CS_2}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, outputs remain in the high-impedance state.
6. Transition is measured ±200mV from steady state.
7. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the required tDW. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)[1]



NOTES:
1. $\overline{WE}$, $\overline{CS_1}$ or $\overline{CS_2}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tWP) of a LOW $\overline{WE}$, a LOW $\overline{CS_1}$ and a LOW $\overline{CS_2}$.
3. tWR is measured from the earlier of $\overline{CS_1}$, $\overline{CS_2}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, outputs remain in the high-impedance state.
6. Transition is measured ±200mV from steady state.
7. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the required tDW. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS STATIC RAMs 64K (16K x 4-BIT) Separate Data Inputs and Outputs

IDT71981S/L
IDT71982S/L

FEATURES:

- Separate data inputs and outputs
- IDT71981S/L: outputs track inputs during write mode
- IDT71982S/L: high impedance outputs during write mode
- High speed (equal access and cycle time)
  - — Military: 20/25/35/45/55/70/85ns (max.)
  - — Commercial: 15/20/25/35ns (max.)
- Low power consumption
- Battery backup operation—2V data retention (L version only)
- High-density 28-pin hermetic and plastic DIP, 28-pin leadless chip carrier, and 28-pin SOJ
- Produced with advanced CMOS high-performance technology
- Inputs and outputs directly TTL-compatible
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71981/IDT71982 are 65,536-bit high-speed static RAMs organized as 16K x 4. They are fabricated using IDT's high-performance, high-reliability technology—CMOS.

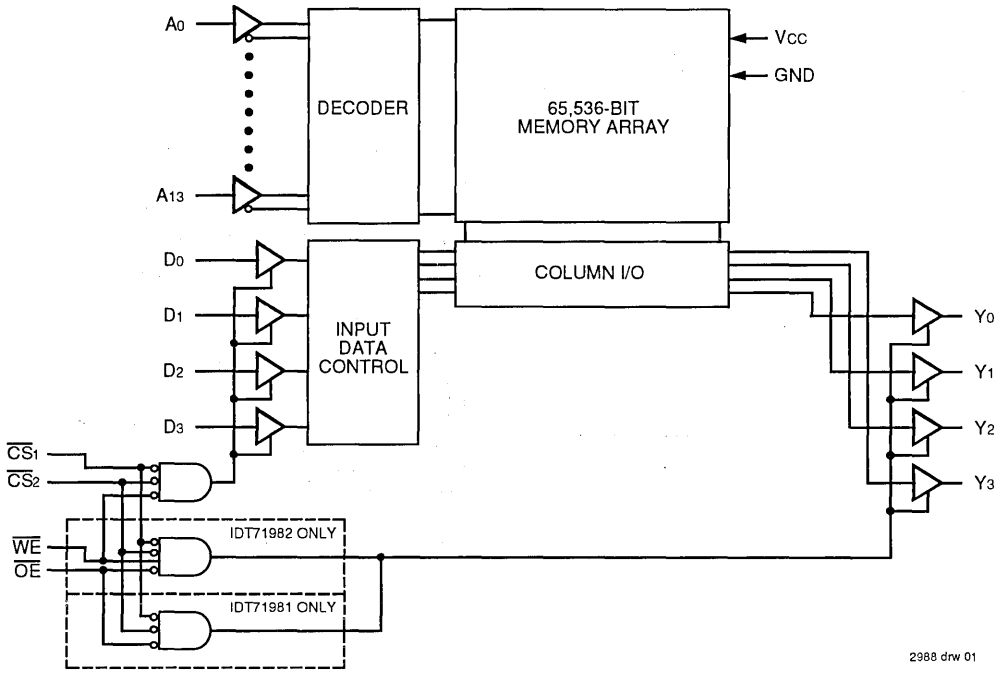
Access times as fast as 15ns are available. These circuits also offer a reduced power standby mode (I_{SB}). When $\overline{CS_1}$ or $\overline{CS_2}$ goes high, the circuit will automatically go to, and remain in, this standby mode. In the ultra-low-power standby mode (I_{SB1}), the devices consume less than 2.5mW, typically. This capability provides significant system-level power and cooling savings. The low-power (L) versions also offer a battery backup data retention capability where the circuit typically consumes only 30µW operating off a 2V battery.

All inputs and outputs of the IDT71981/IDT71982 are TTL-compatible and operate from a single 5V supply.

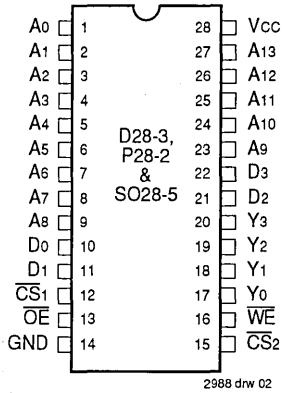
The IDT71981/IDT71982 are packaged in either a 28-pin, 300 mil hermetic DIP, 28-pin 300 mil plastic DIP, 28-pin SOJ,or 28-pin leadless chip carrier.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

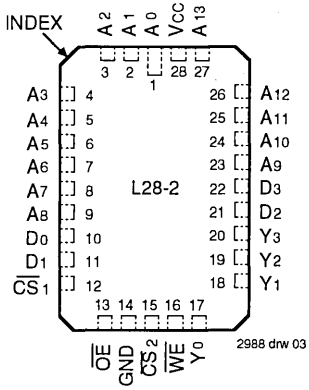
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP/SOJ
TOP VIEW



LCC
TOP VIEW

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 2988 tbl 04
1. This parameter is determined by device characterization, but is not production tested.

PIN DESCRIPTIONS

Name	Description
A0–A13	Address Inputs
$\overline{CS_1}$, $\overline{CS_2}$	Chip Selects
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
D0–D3	$DATA_{IN}$
Y0–Y3	$DATA_{OUT}$
V_{CC}	Power
GND	Ground

2988 tbl 01

TRUTH TABLE[3]

Mode	$\overline{CS_1}$	$\overline{CS_2}$	$\overline{WE}$	$\overline{OE}$	Output	Power
Standby	H	X	X	X	High Z	Standby
Standby	X	H	X	X	High Z	Standby
Read	L	L	H	L	D_{OUT}	Active
Write[1]	L	L	L	L	D_{IN}	Active
Write[1]	L	L	L	H	High Z	Active
Write[2]	L	L	L	X	High Z	Active
Read	L	L	H	H	High Z	Active

NOTES: 2988 tbl 02
1. For IDT71981 only.
2. For IDT71982 only.
3. H = V_{IH}, L = V_{IL}, X = don't care.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2988 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

6

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 2988 tbl 05

1. V_{IL} (min.) = –3.0V for pulse width less than 20ns, once per cycle.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2988 tbl 06

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT71981/2S Min.	IDT71981/2S Max.	IDT71981/2L Min.	IDT71981/2L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	—	10	—	5	µA
			COM'L.	—	5	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}_{1,2}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	—	10	—	5	µA
			COM'L.	—	5	—	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.			0.5	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.		2.4	—	2.4	—	V

2988 tbl 07

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	71981/2S15 71981/2L15 Com'l.	71981/2S15 71981/2L15 Mil.	71981/2S20 71981/2L20 Com'l.	71981/2S20 71981/2L20 Mil.	71981/2S25 71981/2L25 Com'l.	71981/2S25 71981/2L25 Mil.	71981/2S35 71981/2L35 Com'l.	71981/2S35 71981/2L35 Mil.	71981/2S45 71981/2L45 Com'l.	71981/2S45 71981/2L45 Mil.	71981/2S55/70 71981/2L55/70 Com'l.	71981/2S55/70 71981/2L55/70 Mil.	71981/2S85 71981/2L85 Com'l.	71981/2S85 71981/2L85 Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS}_{1,2}$ = V_{IL}, Outputs Open V_{CC} = Max., f = 0[2]	S	100	—	100	105	100	105	100	105	—	105	—	105	—	105	mA
		L	75	—	70	80	70	80	70	80	—	80	—	80	—	80	
I_{CC2}	Dynamic Operating Current $\overline{CS}_{1,2}$ = V_{IL}, Outputs Open V_{CC} = Max., f = f_{MAX}[2]	S	135	—	130	160	125	155	125	140	—	140	—	140	—	140	mA
		L	125	—	115	130	105	125	105	115	—	110	—	110	—	105	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}_{1,2} \geq V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}[2]	S	60	—	55	70	50	60	45	50	—	50	—	50	—	50	mA
		L	45	—	40	50	35	50	30	40	—	35	—	35	—	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}_{1,2} \geq V_{HC}$, V_{CC}= Max., $V_{IN} \geq V_{HC}$ or $V_{IN} \leq V_{LC}$, f = 0[2]	S	20	—	15	25	15	20	15	20	—	20	—	20	—	20	mA
		L	1.5	—	0.5	1.5	0.5	1.5	0.5	1.5	—	1.5	—	1.5	—	1.5	

NOTES: 2988 tbl 06

1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

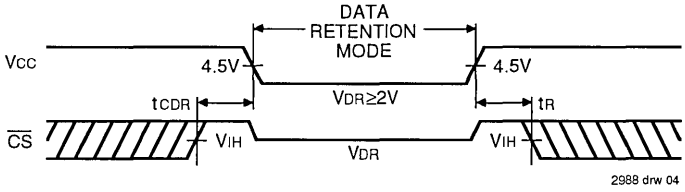
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ. (1) Vcc @ 2.0v	Typ. (1) Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current		MIL.	—	10	15	600	900	µA
			COM'L.	—	10	15	150	225	
t_{CDR}(3)	Chip Deselect to Data Retention Time	$\overline{CS}1$ or $\overline{CS}2 \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$		0	—	—	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	—	—	ns
$\|I_{LI}\|$(3)	Input Leakage Current			—	—	—	2	2	µA

2988 tbl 09

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization, but is not production tested.

LOW V_{CC} DATA RETENTION WAVEFORM

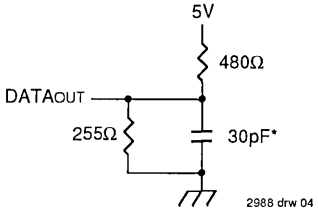


2988 drw 04

AC TEST CONDITIONS

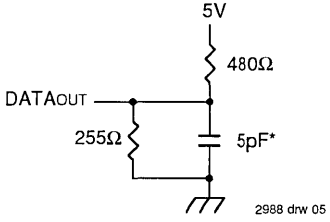
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2988 tbl 10



2988 drw 04

Figure 1. AC Test Load



2988 drw 05

Figure 2. AC Test Load
(for $t_{CLZ1, 2}$, t_{OLZ}, $t_{CHZ1, 2}$, t_{OHZ}, t_{OW} and t_{WHZ})

*Includes scope and jig capacitances

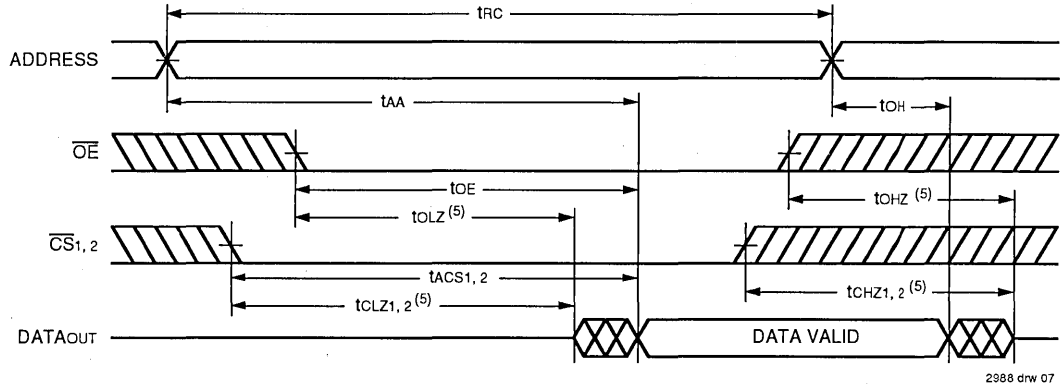
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71981/2S15[1]/20 71981/2L15[1]/20 Min.	Max.	71981/2S25 71981/2L25 Min.	Max.	71981/2S35/45[2] 71981/2L35/45[2] Min.	Max.	71981/2S55[2] 71981/2L55[2] Min.	Max.	71981/2S70[2] 71981/2L70[2] Min.	Max.	71981/2S85[2] 71981/2L85[2] Min.	Max.	Unit
Read Cycle														
t_{RC}	Read Cycle Time	15/20	—	25	—	35/45	—	55	—	70	—	85	—	ns
t_{AA}	Address Access Time	—	15/19	—	25	—	35/45	—	55	—	70	—	85	ns
$t_{ACS1,2}$	Chip Select-1,2 Access Time[3]	—	15/20	—	25	—	35/45	—	55	—	70	—	85	ns
$t_{CLZ1,2}$	Chip Select-1,2 to Output in Low-Z[4]	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	8/9	—	11	—	20/25	—	35	—	45	—	55	ns
t_{OLZ}	Output Enable to Output in Low-Z[4]	5	—	5	—	5	—	5	—	5	—	5	—	ns
$t_{CHZ1,2}$	Chip Select1,2 to Output in High-Z[4]	—	7/8	—	10	—	4	—	20	—	25	—	30	ns
t_{OHZ}	Output Disable to Output in High-Z[4]	—	7/8	—	9	—	15	—	20	—	25	—	30	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}	Chip Select to Power-Up Time[4]	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Deselect to Power-Down Time[4]	—	15/20	—	25	—	35/45	—	55	—	70	—	85	ns

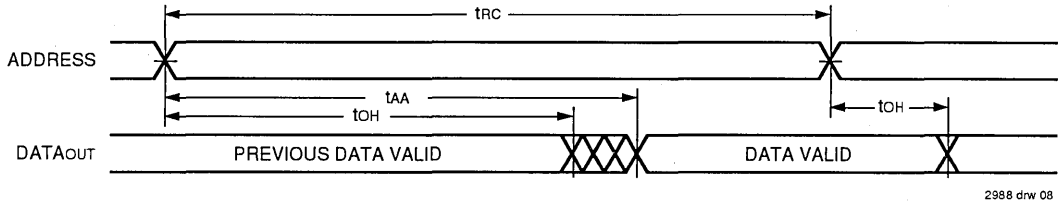
NOTES:
1. 0° to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. Both chip selects must be active low for the device to be selected.
4. This parameter is guaranteed by device characterization, but is not production tested.

2988 tbl 11

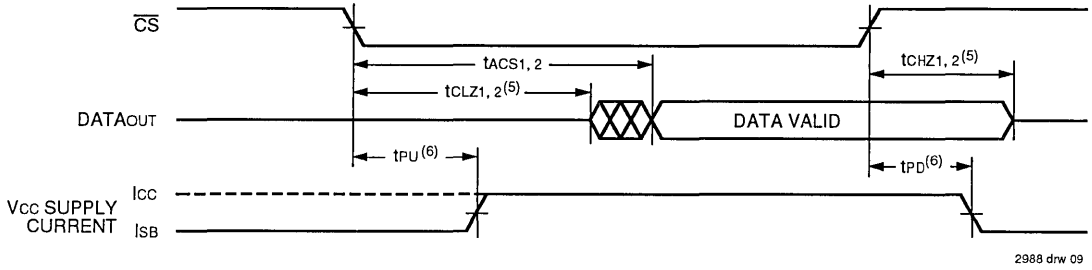
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



NOTES:
1. $\overline{WE}$ is HIGH for READ cycle.
2. Device is continuously selected, $\overline{CS_1}$ = V_{IL}, $\overline{CS_2}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS_1}$ and or $\overline{CS_2}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state voltage.
6. This parameter is guaranteed by device characterization but is not production tested.

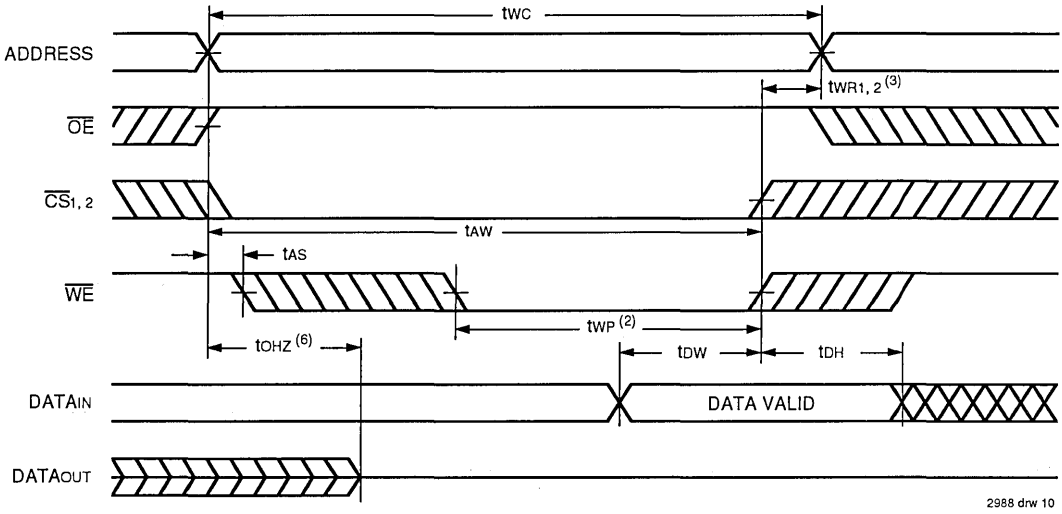
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71981/2S15[1]/20 71981/2L15[1]/20 Min.	Max.	71981/2S25 71981/2L25 Min.	Max.	71981/2S35/45[2] 71981/2L35/45[2] Min.	Max.	71981/2S55[2] 71981/2L55[2] Min.	Max.	71981/2S70[2] 71981/2L70[2] Min.	Max.	71981/2S85[2] 71981/2L85[2] Min.	Max.	Unit
Write Cycle														
tWC	Write Cycle Time	14/17	—	20	—	30/40	—	50	—	60	—	75	—	ns
tCW1,2	Chip Select to End of Write	14/17	—	20	—	25/35	—	50	—	60	—	75	—	ns
tAW	Address Valid to End of Write	14/17	—	20	—	25/35	—	50	—	60	—	75	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	14/17	—	20	—	25/35	—	50	—	60	—	75	—	ns
tWR1,2	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWHZ	Write Enable to Output in High Z[3,5]	—	5/6	—	7	—	10/15	—	25	—	30	—	40	ns
tDW	Data Valid to End of Write	10/10	—	13	—	15/20	—	25	—	30	—	35	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tOW	Output Active from End of Write[3,5]	5	—	5	—	5	—	5	—	5	—	5	—	ns
tIY	Data Valid to Output Valid[3,4]	—	12/15	—	20	—	30/35	—	40	—	45	—	50	ns
tWY	Write Enable to Output Valid[3,4]	—	12/15	—	20	—	30/35	—	40	—	45	—	50	ns

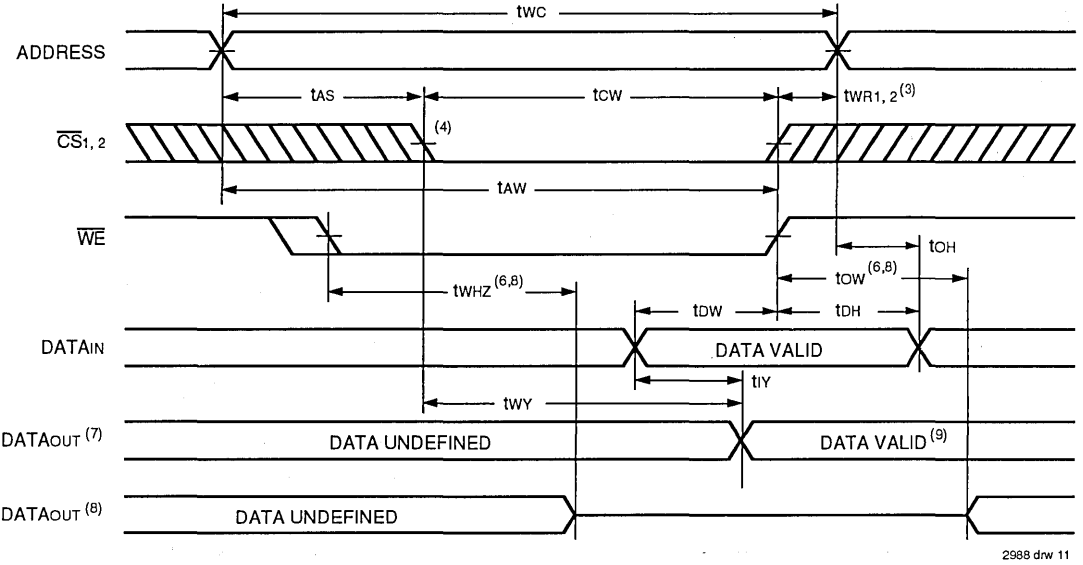
NOTES:
1. 0° to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. This parameter is guaranteed by device characterization but is not production tested.
4. For IDT71981S/L only.
5. For IDT71982S/L only.

2988 tbl 12

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1)

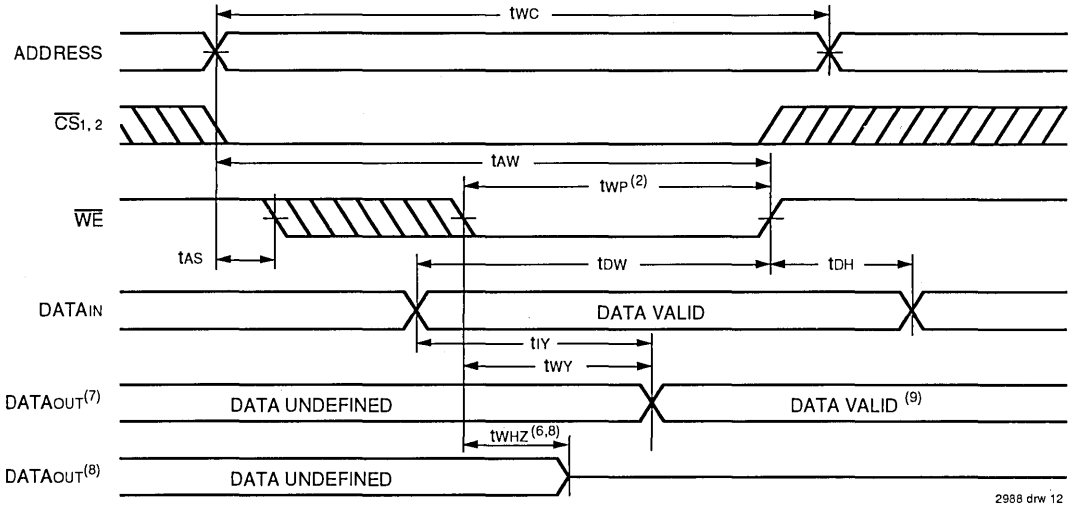


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 5)



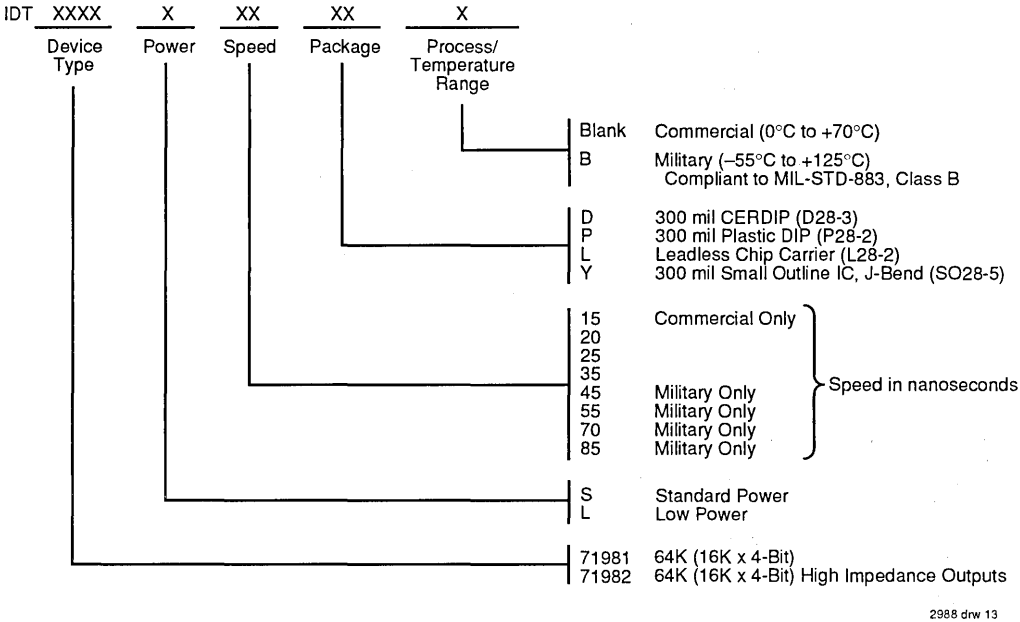
NOTES:
1. $\overline{WE}$ or $\overline{CS_1}$ or $\overline{CS_2}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tWP) of a LOW $\overline{WE}$, a LOW $\overline{CS_1}$ and a low $\overline{CS_2}$.
3. tWR is measured from the earlier of $\overline{CS_1}$, $\overline{CS_2}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. If the $\overline{CS_1}$ and or $\overline{CS_2}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, outputs remain in a high-impedance state.
5. $\overline{OE}$ is continuously LOW ($\overline{OE}$ = VIL).
6. Transition is measured ±200mV from steady state.
7. For IDT71981 only.
8. For IDT71982 only.
9. DATAOUT = DATAIN.

TIMING WAVEFORM OF WRITE CYCLE NO. 3 ($\overline{WE}$ CONTROLLED, $\overline{OE}$ LOW)(1, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}_1$ or $\overline{CS}_2$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tWP) of a LOW $\overline{WE}$, a low $\overline{CS}_1$ and a LOW $\overline{CS}_2$.
3. tWR is measured from the earlier of $\overline{CS}_1$, $\overline{CS}_2$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. If the $\overline{CS}_1$ and or $\overline{CS}_2$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, outputs remain in a high-impedance state.
5. $\overline{OE}$ is continuously LOW ($\overline{OE}$ = VIL).
6. Transition is measured ±200mV from steady state.
7. For IDT71981 only.
8. For IDT71982 only.
9. DATAOUT = DATAIN.

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (8K x 8-BIT)

IDT7164S
IDT7164L

FEATURES:

- High-speed address/chip select access time
  - — Military: 20/25/30/35/45/55/70/85ns (max.)
  - — Commercial: 15/20/25/30/35ns (max.)
- Low power consumption
- Battery backup operation — 2V data retention voltage (L Version only)
- Produced with advanced CMOS high-performance technology
- Inputs and outputs directly TTL-compatible
- Three-state outputs
- Available in:
  - — 28-pin DIP, SOIC, SOJ, LCC and CERPACK
  - — 32-pin LCC, and PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7164 is a 65,536 bit high-speed static RAM organized as 8K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology.

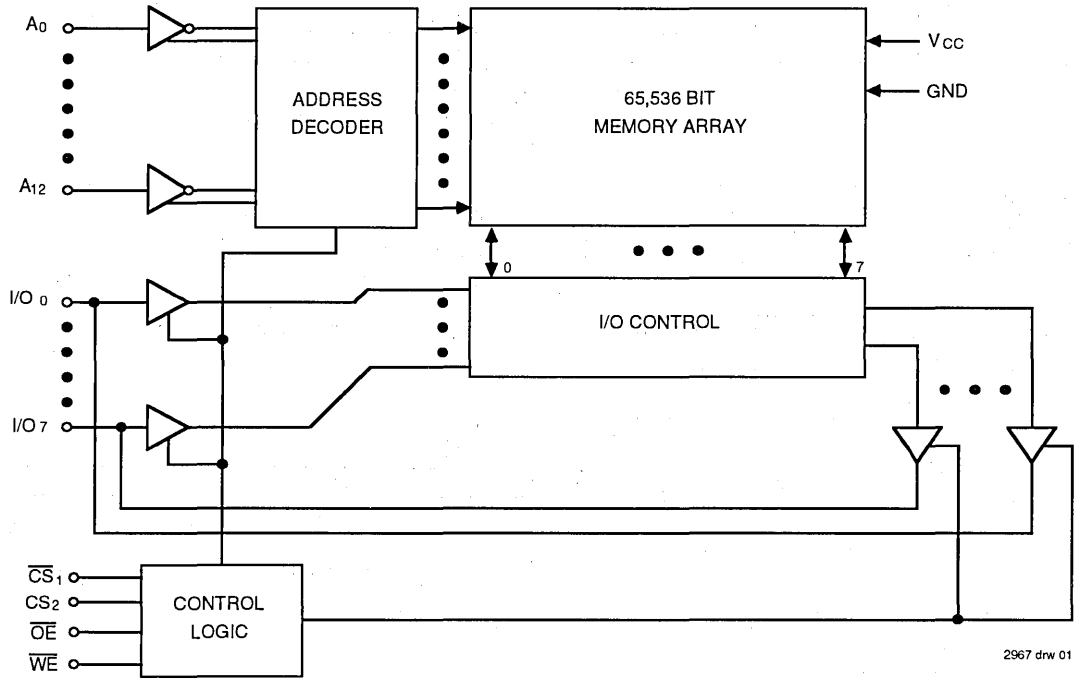
Address access times as fast as 15ns are available and the circuit offers a reduced power standby mode. When $\overline{CS_1}$ goes high or CS_2 goes low, the circuit will automatically go to, and remain in, a low-power stand by mode. The low-power (L) version also offers a battery backup data retention capability at power supply levels as low as 2V.

All inputs and outputs of the IDT7164 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

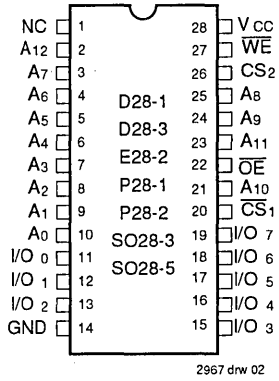
The IDT7164 is packaged in a 28-pin 300 mil DIP and SOJ; 28-pin 330 mil SOIC; 28-pin 600 mil DIP; 32-pin PLCC and LCC; 28-pin LCC and 28-pin CERPACK.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

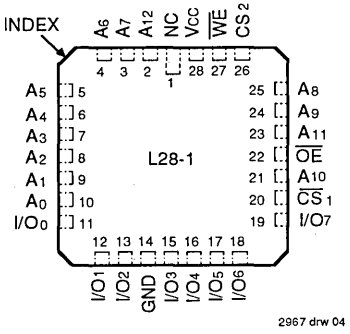
FUNCTIONAL BLOCK DIAGRAM



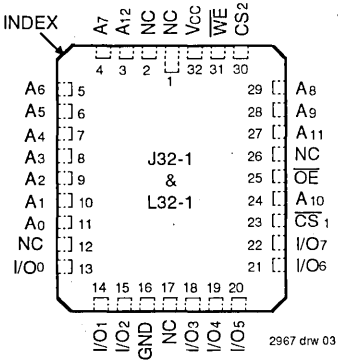
PIN CONFIGURATIONS



DIP/SOIC/SOJ/CERPACK
TOP VIEW



28-PIN LCC
TOP VIEW



32-PIN LCC/PLCC
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A0–A12	Address
I/O0–I/O7	Data Input/Output
$\overline{CS_1}$	Chip Select
CS_2	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
VCC	Power

2967 tbl 01

TRUTH TABLE(1,2,3)

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	I/O	Function
X	H	X	X	High-Z	Deselected – Standby (ISB)
X	X	L	X	High-Z	Deselected – Standby (ISB)
X	VHC	VHC or VLC	X	High-Z	Deselected –Standby (ISB1)
X	X	VLC	X	High-Z	Deselected –Standby (ISB1)
H	L	H	H	High-Z	Output Disabled
H	L	H	L	DataOUT	Read Data
L	L	H	X	DataIN	Write Data

2967 tbl 02

NOTE:
1. CS_2 will power-down $\overline{CS_1}$, but $\overline{CS_1}$ will not power-down CS_2.
2. H = VIH, L = VIL, X = don't care.
3. VLC = 0.2V, VHC = VCC - 0.2V

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

2967 tbl 03

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed VCC + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	VCC
Military	–55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2967 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input HIGH Voltage	2.2	—	VCC + 0.5	V
VIL	Input LOW Voltage	–0.5(1)	—	0.8	V

2967 tbl 06

NOTE:
1. VIL (min.) = –1.5V for pulse width less than 10ns, once per cycle.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2967 tbl 04

1. This parameter is determined by device characterization, but is not production tested.

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	7164S15 7164L15 Com'l.	7164S15 7164L15 Mil.	7164S20 7164L20 Com'l.	7164S20 7164L20 Mil.	7164S25 7164L25 Com'l.	7164S25 7164L25 Mil.	7164S30 7164L30 Com'l.	7164S30 7164L30 Mil.	Unit
I_{CC1}	Operating Power Supply Current, $\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH}, Outputs Open, V_{CC} = Max., f = 0[3]	S	110	—	100	110	90	110	90	100	mA
		L	100	—	90	100	80	100	80	90	
I_{CC2}	Dynamic Operating Current $\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH}, Outputs Open, V_{CC} = Max., f = f_{MAX}[3]	S	180	—	170	180	170	180	160	170	mA
		L	150	—	150	160	150	160	140	150	
I_{SB}	Standby Power Supply Current (TTL Level), $\overline{CS_1}$ ≥ V_{IH} or CS_2 ≤ V_{IL} V_{CC} = Max., Outputs Open, f = f_{MAX}[3]	S	20	—	20	20	20	20	20	20	mA
		L	3	—	3	5	3	5	3	5	
I_{SB1}	Full Standby Power Supply Current (CMOS Level), f = 0[3], V_{CC} = Max. 1. $\overline{CS_1}$ ≥ V_{HC} and CS_2 ≥ V_{HC}, or 2. CS_2 ≤ V_{LC}	S	15	—	15	20	15	20	15	20	mA
		L	0.2	—	0.2	1	0.2	1	0.2	1	

6

DC ELECTRICAL CHARACTERISTICS[1] (Continued)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	7164S35 7164L35 Com'l.	7164S35 7164L35 Mil.	7164S45 7164L45 Com'l.	7164S45 7164L45 Mil.	7164S55 7164L55 Com'l.	7164S55 7164L55 Mil.	7164S70/85[2] 7164L70/85[2] Com'l.	7164S70/85[2] 7164L70/85[2] Mil.	Unit
I_{CC1}	Operating Power Supply Current, $\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH}, Outputs Open, V_{CC} = Max., f = 0[3]	S	90	100	—	100	—	100	—	100	mA
		L	80	90	—	90	—	90	—	90	
I_{CC2}	Dynamic Operating Current $\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH}, Outputs Open, V_{CC} = Max., f = f_{MAX}[3]	S	150	160	—	160	—	160	—	160	mA
		L	130	140	—	130	—	125	—	120	
I_{SB}	Standby Power Supply Current (TTL Level), $\overline{CS_1}$ ≥ V_{IH}, or CS_2 ≤ V_{IL} V_{CC} = Max., Outputs Open, f = f_{MAX}[3]	S	20	20	—	20	—	20	—	20	mA
		L	3	5	—	5	—	5	—	5	
I_{SB1}	Full Standby Power Supply Current (CMOS Level), f = 0[3], V_{CC} = Max. 1. $\overline{CS_1}$ ≥ V_{HC} and CS_2 ≥ V_{HC}, or 2. CS_2 ≤ V_{LC}	S	15	20	—	20	—	20	—	20	mA
		L	0.2	1	—	1	—	1	—	1	

NOTES: 2967 tbl 07

1. All values are maximum guaranteed values.
2. Also available: 100, 120, 150 and 200ns military devices.
3. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT7164S Min.	IDT7164S Max.	IDT7164L Min.	IDT7164L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	—	10	—	5	µA
			COM'L.	—	5	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS_1}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	—	10	—	5	µA
			COM'L.	—	5	—	2	
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.			0.4	—	0.4	V
		I_{OL} = 10mA, V_{CC} = Min.		—	0.5	—	0.5	
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.		2.4	—	2.4	—	V

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ. (1) Vcc @ 2.0v	Typ. (1) Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	1. $\overline{CS_1} \geq V_{HC}$ $CS_2 \geq V_{HC}$, or 2. $CS_2 \leq V_{LC}$	MIL.	—	10	15	200	300	µA
			COM'L.	—	10	15	60	90	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	—	—	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	—	—	ns
$\|I_{LI}\|$(3)	Input Leakage Current			—	—	—	2	2	µA

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization, but is not production tested.

2967 tbl 10

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2967 tbl 08

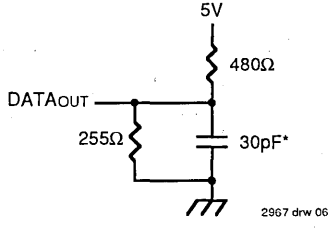


Figure 1. AC Test Load

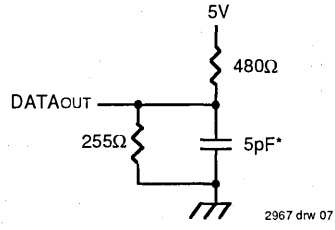


Figure 2. AC Test Load
(for t_{CLZ1}, t_{CLZ2}, t_{OLZ}, t_{CHZ1}, t_{CHZ2}, t_{OHZ}, t_{OW}, and t_{WHZ})

*Includes scope and jig capacitances

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7164S15[1] 7164L15[1]		7164S20 7164L20		7164S25 7164L25		7164S30 7164L30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
tRC	Read Cycle Time	15	—	20	—	25	—	30	—	ns
tAA	Address Access Time	—	15	—	19	—	25	—	29	ns
tACS1	Chip Select-1 Access Time[3]	—	15	—	20	—	25	—	30	ns
tACS2	Chip Select-2 Access Time[3]	—	20	—	25	—	30	—	35	ns
tCLZ1,2	Chip Select-1, 2 to Output in Low-Z[4]	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	7	—	8	—	12	—	15	ns
tOLZ	Output Enable to Output in Low-Z[4]	3	—	3	—	3	—	3	—	ns
tCHZ1,2	Chip Select-1, 2 to Output in High-Z[4]	—	8	—	9	—	13	—	13	ns
tOHZ	Output Disable to Output in High-Z[4]	—	7	—	8	—	10	—	12	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
tPU	Chip Select to Power Up Time[4]	0	—	0	—	0	—	0	—	ns
tPD	Chip Deselect to Power Down Time[4]	—	15	—	20	—	25	—	30	ns
Write Cycle										
tWC	Write Cycle Time	15	—	20	—	25	—	30	—	ns
tCW1, 2	Chip Select to End-of-Write	14	—	15	—	18	—	22	—	ns
tAW	Address Valid to End-of-Write	14	—	15	—	18	—	22	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	14	—	15	—	21	—	23	—	ns
tWR1	Write Recovery Time ($\overline{CS_1}$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
tWR2	Write Recovery Time (CS_2)	5	—	5	—	5	—	5	—	ns
tWHZ	Write Enable to Output in High-Z[4]	—	6	—	8	—	10	—	12	ns
tDW	Data to Write Time Overlap	8	—	10	—	13	—	13	—	ns
tDH1	Data Hold from Write Time ($\overline{CS_1}$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
tDH2	Data Hold from Write Time (CS_2)	5	—	5	—	5	—	5	—	ns
tOW	Output Active from End-of-Write[4]	5	—	5	—	5	—	5	—	ns

NOTES:
1. 0° to +70°C temperature range only.
2. –55°C to +125°C temperature range only. Also available: 100, 120, 150 and 200ns military devices.
3. Both chip selects must be active for the device to be selected.
4. This parameter is guaranteed by device characterization, but is not production tested.

2967 tbl 11

6

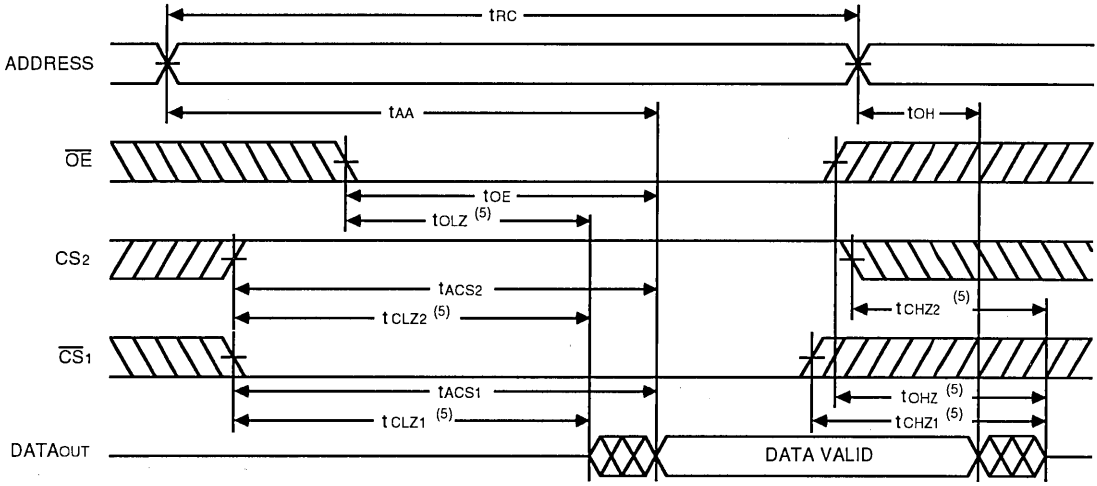
AC ELECTRICAL CHARACTERISTICS (Continued) (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7164S35 7164L35		7164S45[2] 7164L45[2]		7164S55[2] 7164L55[2]		7164S70[2]/85[2] 7164L70[2]/85[2]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	35	—	45	—	55	—	70/85	—	ns
t_{AA}	Address Access Time	—	35	—	45	—	55	—	70/85	ns
t_{ACS1}	Chip Select-1 Access Time[3]	—	35	—	45	—	55	—	70/85	ns
t_{ACS2}	Chip Select-2 Access Time[3]	—	40	—	45	—	55	—	70/85	ns
$t_{CLZ1,2}$	Chip Select-1, 2 to Output in Low-Z[4]	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	18	—	25	—	30	—	35/40	ns
t_{OLZ}	Output Enable to Output in Low-Z[4]	3	—	3	—	3	—	3	—	ns
$t_{CHZ1,2}$	Chip Select-1, 2 to Output in High-Z[4]	—	15	—	20	—	25	—	30/35	ns
t_{OHZ}	Output Disable to Output in High-Z[4]	—	15	—	20	—	25	—	30/35	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{PU}	Chip Select to Power Up Time[4]	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Deselect to Power Down Time[4]	—	35	—	45	—	55	—	70/85	ns
Write Cycle										
t_{WC}	Write Cycle Time	35	—	45	—	55	—	70/85	—	ns
$t_{CW1,2}$	Chip Select to End-of-Write	25	—	33	—	50	—	60/75	—	ns
t_{AW}	Address Valid to End-of-Write	25	—	33	—	50	—	60/75	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	25	—	25	—	50	—	60/75	—	ns
t_{WR1}	Write Recovery Time ($\overline{CS_1}$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
t_{WR2}	Write Recovery Time (CS_2)	5	—	5	—	5	—	5	—	ns
t_{WHZ}	Write Enable to Output in High-Z[4]	—	14	—	18	—	25	—	30/35	ns
t_{DW}	Data to Write Time Overlap	15	—	20	—	25	—	30/35	—	ns
t_{DH1}	Data Hold from Write Time ($\overline{CS_1}$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
t_{DH2}	Data Hold from Write Time (CS_2)	5	—	5	—	5	—	5	—	ns
t_{OW}	Output Active from End-of-Write[4]	5	—	5	—	5	—	5	—	ns

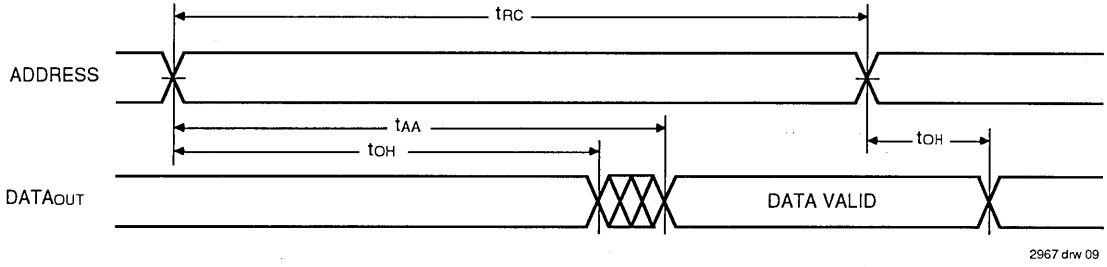
NOTES:
2967 tbl 11

1. 0° to +70°C temperature range only.
2. –55°C to +125°C temperature range only. Also available: 100, 120, 150, and 200ns military devices.
3. Both chip selects must be active for the device to be selected.
4. This parameter is guaranteed by device characterization, but is not production tested.

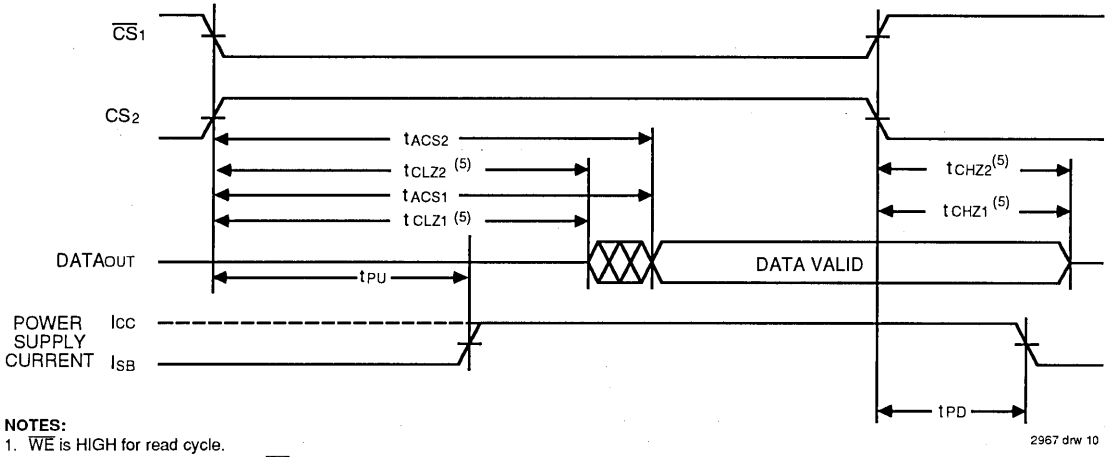
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)

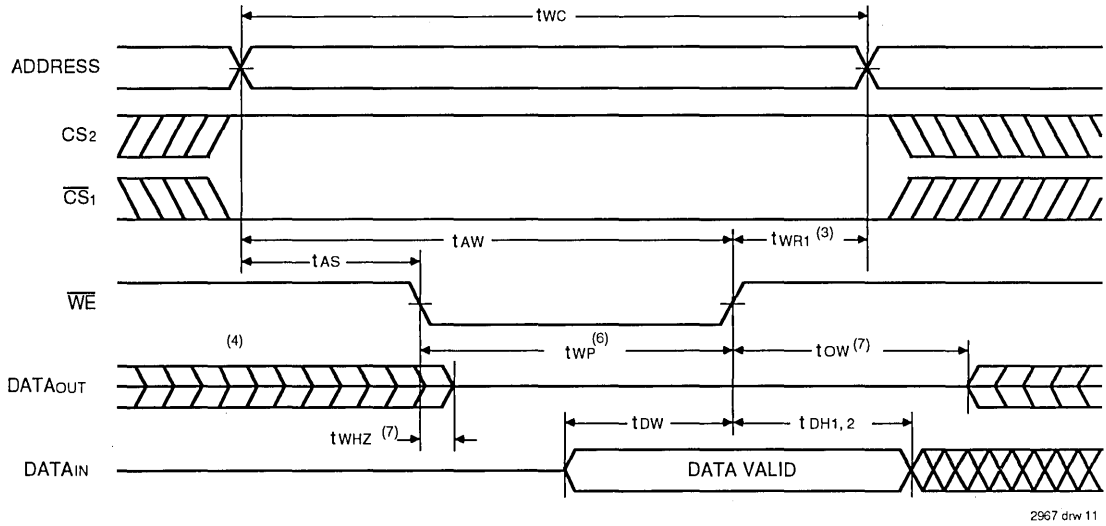


TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



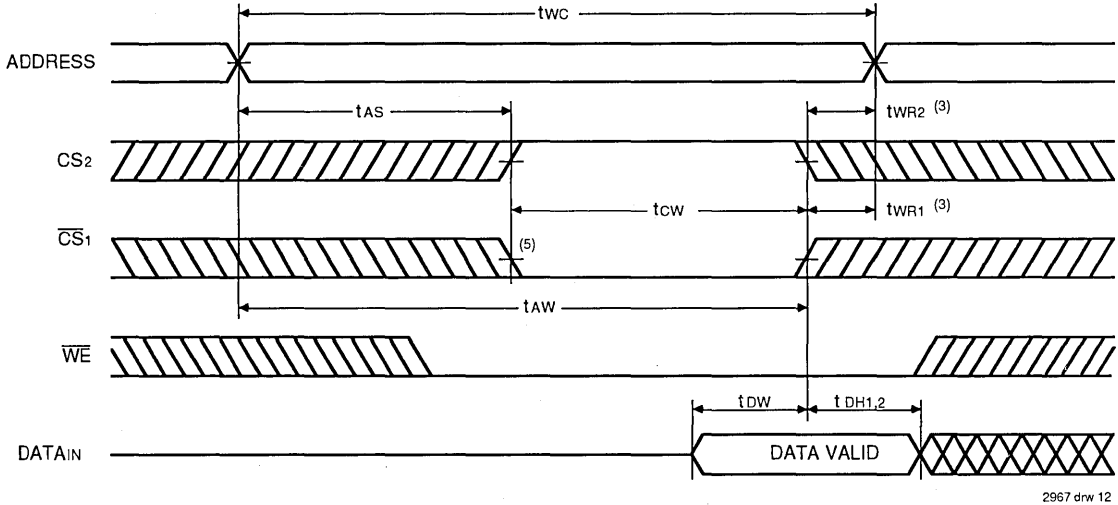
NOTES:
1. $\overline{WE}$ is HIGH for read cycle.
2. Device is continuously selected, $\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH}.
3. Address valid prior to or coincident with $\overline{CS_1}$ transition LOW and CS_2 transition HIGH.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 6)



2967 drw 11

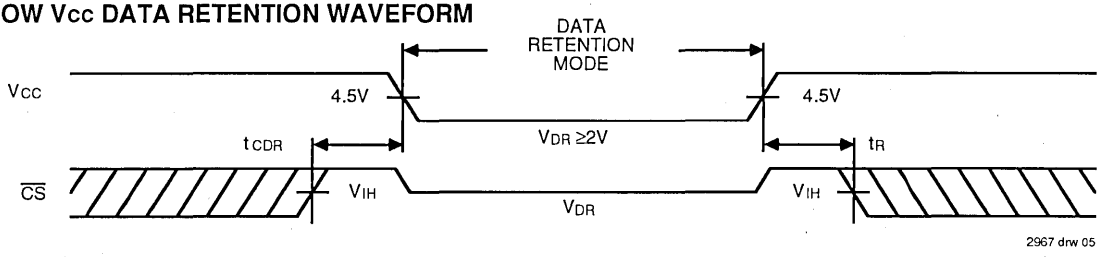
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2)



2967 drw 12

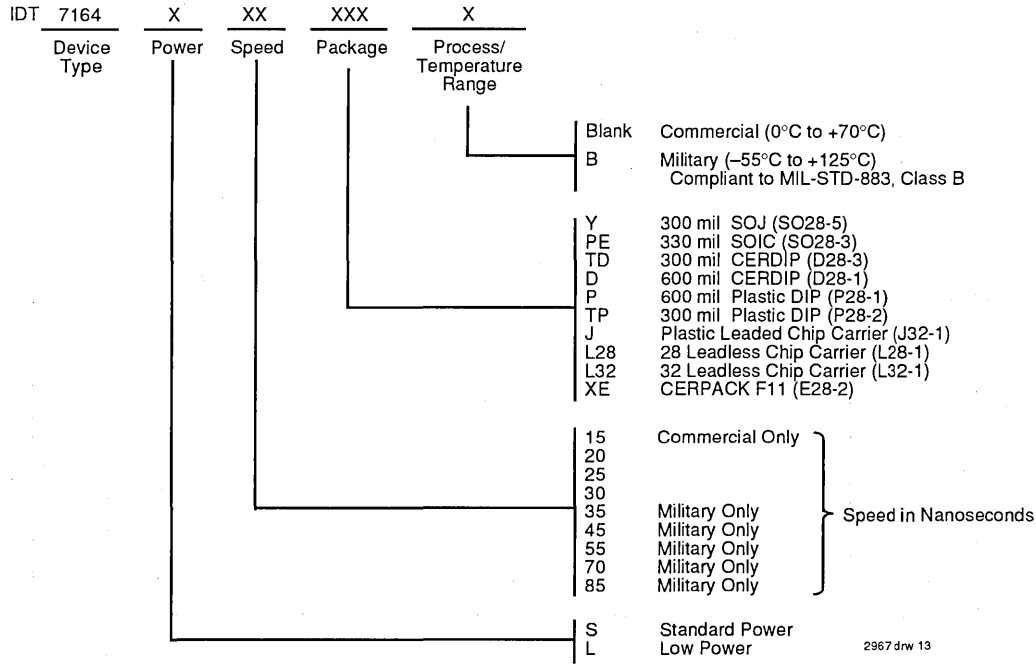
NOTES:
1. $\overline{WE}$, $\overline{CS_1}$ or CS_2 must be inactive during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{WE}$, a LOW $\overline{CS_1}$ and a HIGH CS_2.
3. $t_{WR1, 2}$ is measured from the earlier of $\overline{CS_1}$ or $\overline{WE}$ going HIGH or CS_2 going LOW to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS_1}$ LOW transition or CS_2 HIGH transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. $\overline{OE}$ is continuously HIGH. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse width is as short as the specified t_{WP}.
7. Transition is measured ±200mV from steady state.

LOW Vcc DATA RETENTION WAVEFORM



2967 drw 05

ORDERING INFORMATION



2967 drw 13

6

Integrated Device Technology, Inc.

BiCMOS STATIC RAM 64K (8K x 8-BIT)

IDT71B64

FEATURES:

- 8K x 8 organization
- JEDEC standard 28-pin DIP and SOJ
- Fast access time and cycle time
  — Commercial: 8/10/12 (max.)
- Produced with advanced BiCMOS high-performance technology
- Bidirectional inputs and outputs directly TTL compatible

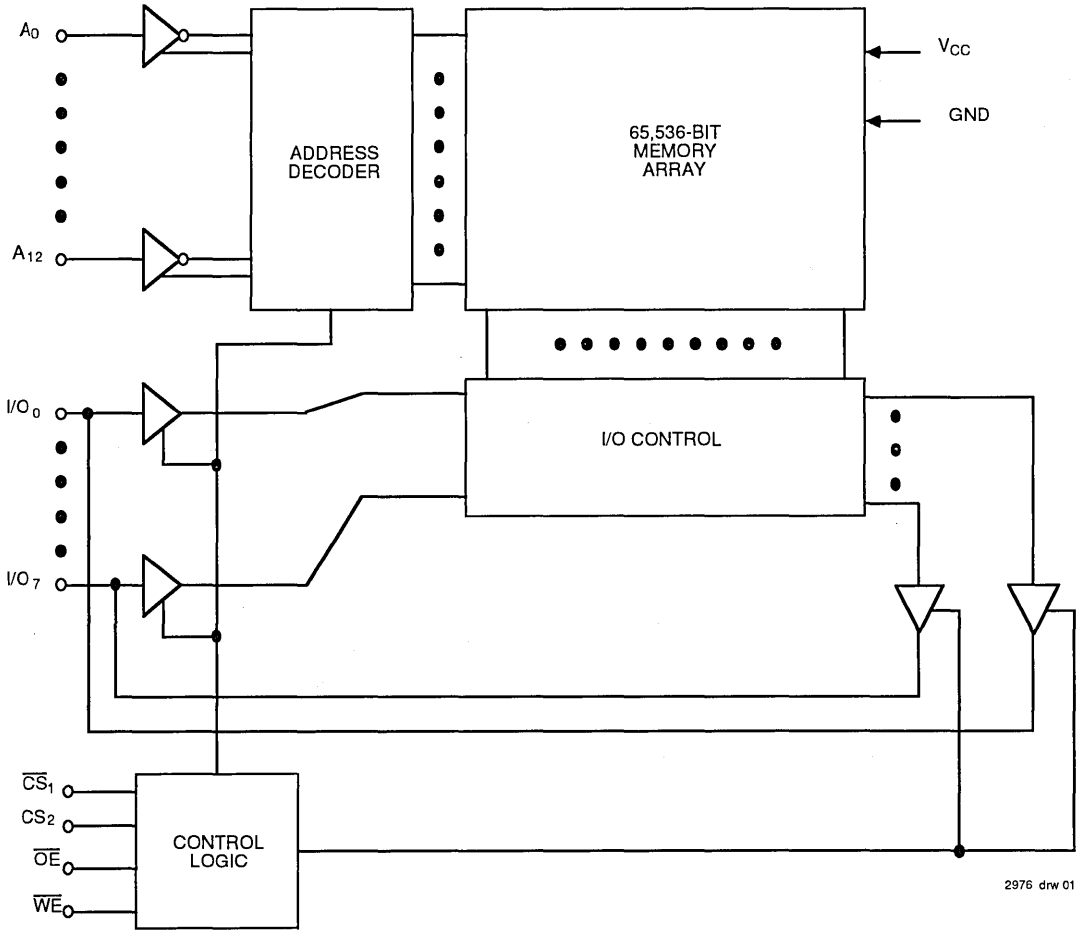
DESCRIPTION:

The IDT71B64 is a 65,536-bit high-speed static RAM organized as 8K x 8. It is fabricated using IDT's high-performance, high-reliability BiCMOS technology.

The IDT71B64 offers address access times as fast as 8ns. All inputs and outputs of the IDT71B64 are TTL-compatible. The device has 2 chip selects for simplified address decoding.

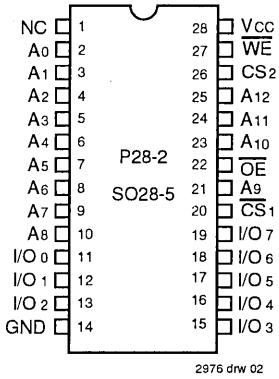
The IDT71B64 is packaged in JEDEC standard 300-mil 28-pin plastic DIP and SOJ packages.

FUNCTIONAL BLOCK DIAGRAM



The IDT logo is a registered trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP/SOJ
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Unit
VTERM(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	–55 to +125	°C
TSTG	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE: 2976 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed VCC + 0.5V.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

NOTE: 2976 tbl 03

1. This parameter is determined by device characterization, but is not production tested.

6

TRUTH TABLE(1,2)

INPUTS					
$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	I/O	FUNCTION
X	H	X	X	High-Z	Deselected–Standby (ISB)
X	VHC(3)	X	X	High-Z	Deselected–Standby (ISB1)
X	X	L	X	High-Z	Deselected–Standby (ISB)
X	X	VLC(3)	X	High-Z	Deselected–Standby (ISB1)
H	L	H	H	High-Z	Outputs Disabled
H	L	H	L	DATAOUT	Read Data
L	L	H	X	DATAIN	Write Data

NOTES: 2976 tbl 01

1. H = VIH, L = VIL, X = Don't care.
2. VLC = 0.2V, VHC = VCC -0.2V.
3. Other inputs ≥VHC or ≤VLC.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	VCC
Commercial	0°C to +70°C	0V	5V ± 10%

2976 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	VCC+0.5	V
VIL	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2976 tbl 04

1. VIL (min.) = –1.5V for pulse width less than 10ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

Symbol	Parameter	71B64S8[3] Com'l.	71B64S10 Com'l.	71B64S12 Com'l.	Unit
ICC	Dynamic Operating Current, CS2 ≥ VIH and $\overline{CS_1}$ ≤ VIL, Outputs Open, VCC = Max., f = fMAX[2]	180	170	170	mA
ISB	Standby Power Supply Current (TTL Level) $\overline{CS_1}$ ≥ VIH or CS2 ≤ VIL, Outputs Open, VCC = Max., f = fMAX[2]	50	50	50	mA
ISB1	Full Standby Power Supply Current (CMOS Level) $\overline{CS_1}$ ≥ VHC or CS2 ≤ VLC, Outputs Open, VCC = Max., f = 0[2], VIN ≤ VLC or VIN ≥ VHC	20	20	20	mA

NOTES:
1. All values are maximum guaranteed values.
2. $f_{MAX} = 1/t_{RC}$ (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.
3. Preliminary only.

2896 tbl 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1, 2 and 3

2976 tbl 06

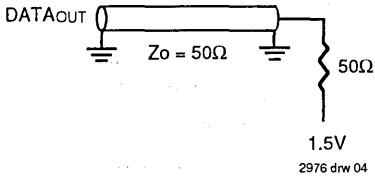
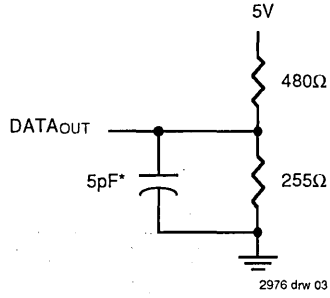


Figure 1. AC Test Load



*Includes jig and scope capacitance.

Figure 2. AC Test Load
(for t_{CLZ} 1,2, t_{OLZ}, t_{CHZ} 1, 2, t_{OHZ}, t_{WHZ}, t_{OW})

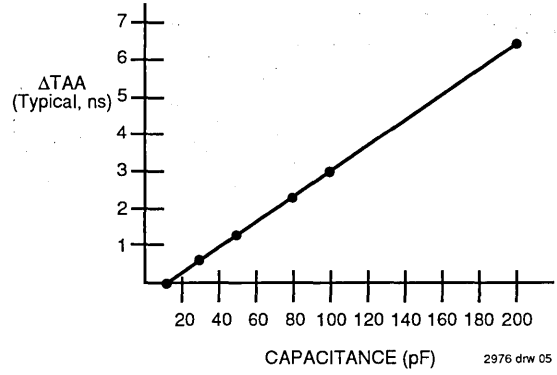


Figure 3. Lumped Capacitive Load, Typical Derating

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71B64S		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS_1}$ = VIH, CS_2 = VIL, V_{OUT} = GND to V_{CC}	—	5	µA
VOL	Output LOW Voltage	I_{OL} = 10mA, V_{CC} = Min.	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.	—	0.4	
VOH	Output HIGH Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

2976 tbl 07

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, Commercial Temperature Ranges)

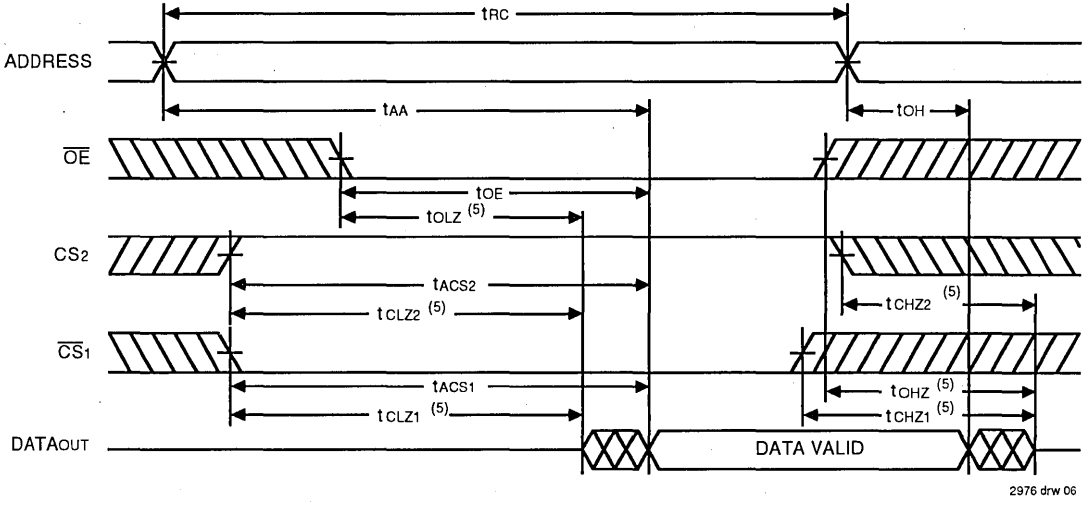
Symbol	Parameter	71B64S8[3]		71B64S10		71B64S12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
tRC	Read Cycle Time	8	—	10	—	12	—	ns
tAA	Address Access Time	—	8	—	10	—	12	ns
tACS1,2	Chip Select-1, 2 Access Time[1]	—	8	—	10	—	12	ns
tCLZ1,2[2]	Chip Select-1, 2 to Output in Low-Z	2	—	2	—	2	—	ns
tOE	Output Enable to Output Valid	—	4	—	5	—	6	ns
tOLZ[2]	Output Enable to Output in Low-Z[2]	2	—	2	—	2	—	ns
tCHZ1,2[2]	Chip Deselect-1, 2 to Output in High-Z[2]	—	4	—	5	—	6	ns
tOHZ[2]	Output Disable to Output in High-Z[2]	—	4	—	4	—	5	ns
tOH	Output Hold from Address Change	2	—	2	—	3	—	ns
tPU[2]	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
tPD[2]	Chip Deselect to Power-Up Time	—	8	—	10	—	12	ns
Write Cycle								
tWC	Write Cycle Time	8	—	10	—	12	—	ns
tAW	Address Valid to End-of-Write	7	—	8	—	10	—	ns
tCW1	Chip Select to End-of-Write ($\overline{CS1}$)	7	—	8	—	10	—	ns
tCW2	Chip Select to End-of-Write (CS2)	7	—	7	—	9	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWP	Write Pulse Width	7	—	7	—	9	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tWHZ[2]	Write Enable to Output in High-Z[2]	—	4	—	5	—	6	ns
tDW	Data Valid to End-of-Write	5	—	5	—	6	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	ns
tOW[2]	Output Active from End-of-Write[2]	2	—	2	—	2	—	ns

NOTES:
1. Both chip selects must be active for the device to be selected.
2. This parameter is guaranteed by device characterization, but is not production tested.
3. Preliminary only.

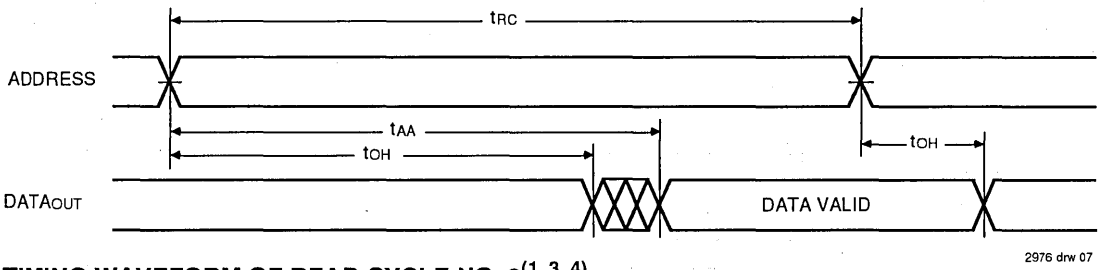
2976 tbl 08

6

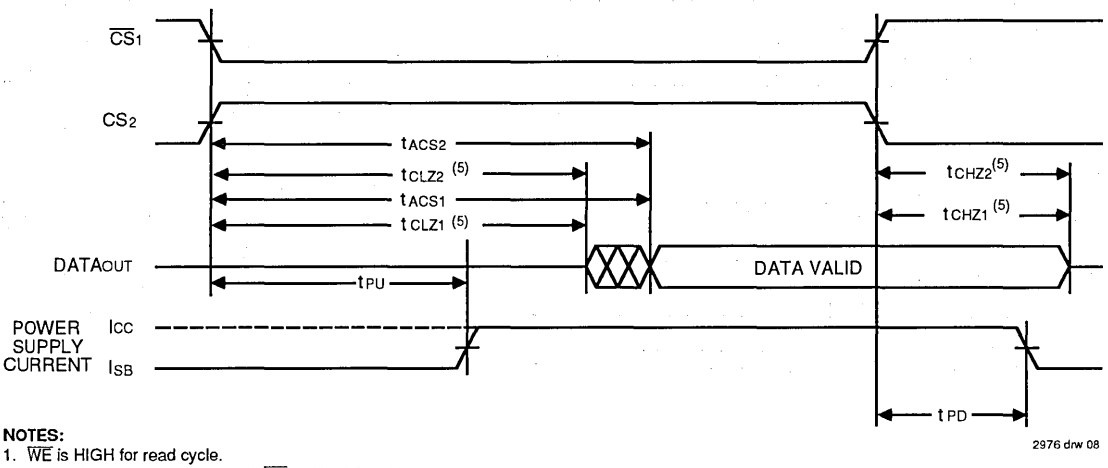
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)

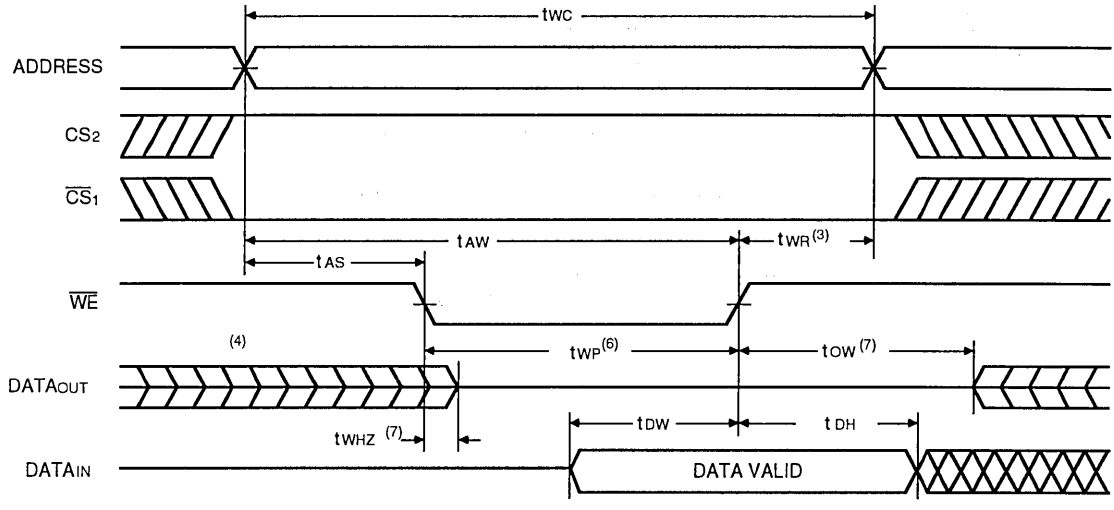


TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



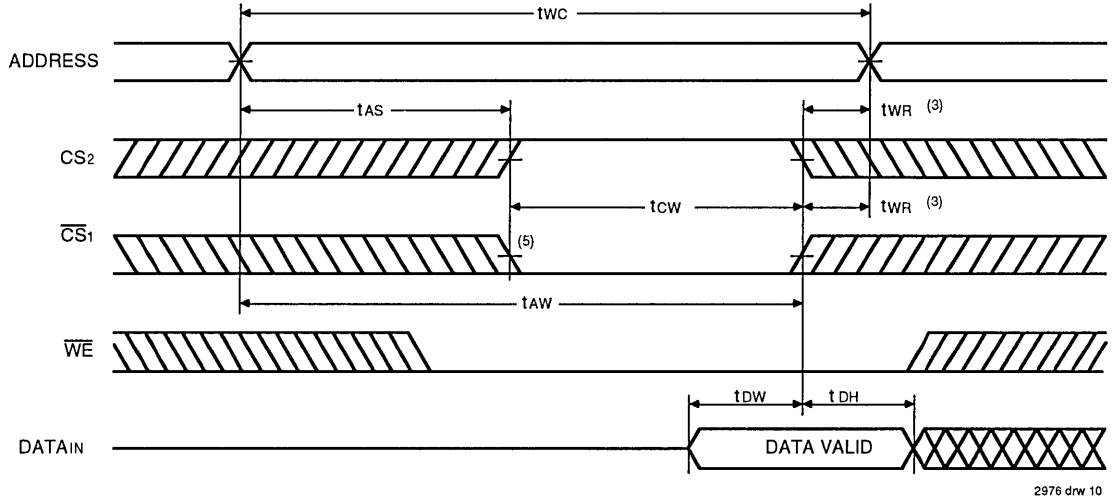
NOTES:
1. $\overline{WE}$ is HIGH for read cycle.
2. Device is continuously selected, $\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH}.
3. Address valid prior to or coincident with $\overline{CS_1}$ transition LOW and CS_2 transition HIGH.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 6)



2976 drw 09

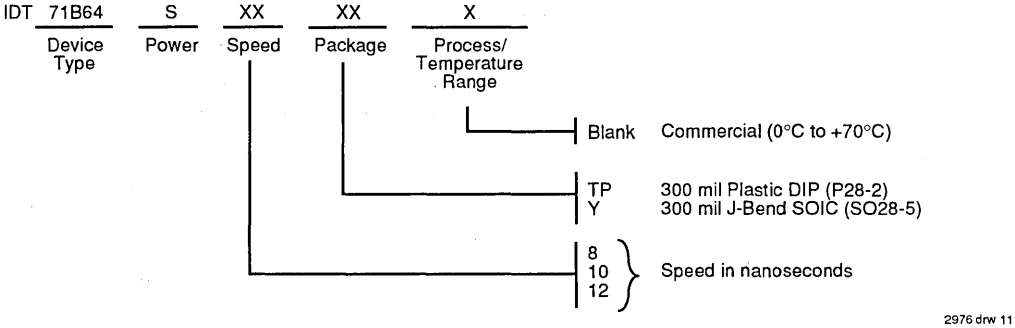
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2)



2976 drw 10

NOTES:
1. $\overline{WE}$, $\overline{CS_1}$ or CS_2 must be inactive during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{WE}$, a LOW $\overline{CS_1}$ and a HIGH CS_2.
3. $t_{WR1,2}$ is measured from the earlier of $\overline{CS_1}$ or $\overline{WE}$ going HIGH or CS_2 going LOW to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS_1}$ LOW transition or CS_2 HIGH transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. $\overline{OE}$ is continuously HIGH. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be greater than or equal to $t_{WHZ}+t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse width is as short as the specified t_{WP}.
7. Transition is measured ±200mV from steady state.

ORDERING INFORMATION



2976 drw 11

256/288K SRAM PRODUCTS

The flagship 256/288K family of IDT SRAMs offers some of the fastest speeds in the industry in 4-bit wide and 8-bit wide configurations. The CMOS parts are as fast as 15ns, with the BiCMOS devices as fast as 10ns.

The 20ns 71256 offers the best standby power consumption in the industry in its "L" version, which makes it ideally suited for battery-operated equipment like notebook computers and portable instruments.

The CMOS x8 parts are especially suitable for cache memory applications in the PC market, while the BiCMOS offerings are directly applicable to many of today's workstation caches. The x4 parts are well suited for many workstation cache applications as well, such as R4000 cache.

High-performance communications applications can also benefit from the fast speeds and surface-mount packaging options offered in this family.

Size	Org.	Features	Process	Part Number	Power	Speeds	
						Commercial	Military
256/288K	64K x 4		CMOS	61298	SA	15,17,20	20,25
	64K x 4		BiCMOS	61B298	S	12,15,20	N/A
	64K x 4		BiCMOS	61B298	SA	10,12,15	N/A
	32K x 8		CMOS	71256	S/L	20,25,35	25,35,45,55,70,85
	32K x 8		CMOS	71256	SA	15,17	17,20
	32K x 8		BiCMOS	71B256	S	12,15,20	N/A
	32K x 8		BiCMOS	71B256	SA	10,12,15	N/A
	32K x 9		BiCMOS	71B259	S	10,12,15	N/A

TABLE OF CONTENTS

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Integrated Device Technology, Inc.

CMOS STATIC RAM 256K (64K x 4-BIT)

PRELIMINARY
IDT61298SA

FEATURES:

- 64K x 4 high-speed static RAM
- Fast Output Enable ($\overline{OE}$) pin available for added system flexibility
- High speed (equal access and cycle times)
  - — Military: 20/25ns (max.)
  - — Commercial: 15/17/20ns (max.)
- JEDEC standard pinout
- 300 mil 28-pin DIP, 300 mil 28-pin SOJ, and 300 mil 28-pin LCC
- Produced with advanced CMOS technology
- Bidirectional data inputs and outputs
- Inputs/Outputs TTL-compatible
- Three-state outputs
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

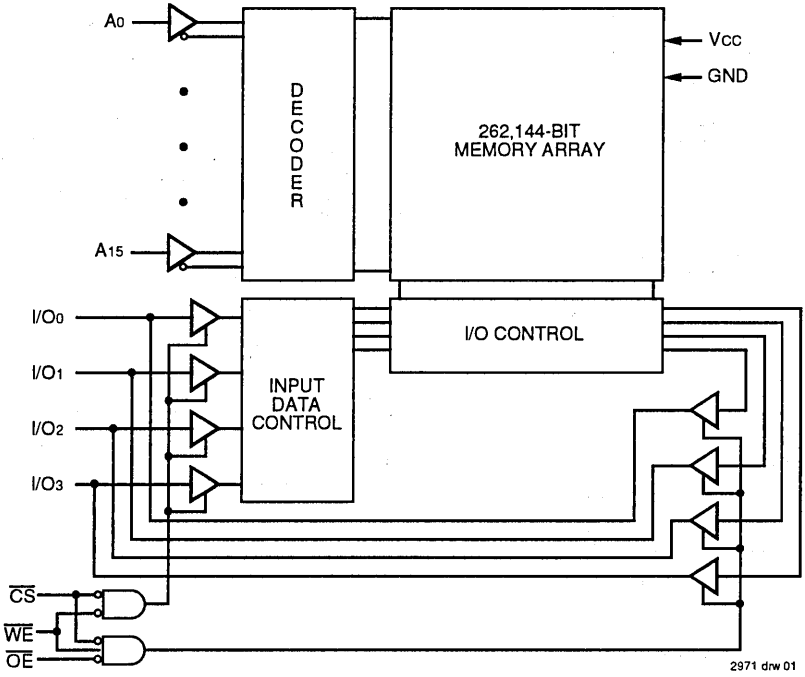
The IDT61298SA is a 262,144-bit high-speed static RAM organized as 64K x 4. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective approach for memory intensive applications.

The IDT61298SA features two memory control functions: Chip Select ($\overline{CS}$) and Output Enable ($\overline{OE}$). These two functions greatly enhance the IDT61298SA's overall flexibility in high-speed memory applications.

Access times as fast as 15ns are available. The IDT61298SA offers a reduced power standby mode, I_{SB1}, which enables the designer to considerably reduce device power requirements. This capability significantly decreases system power and cooling levels, while greatly enhancing system reliability.

All inputs and outputs are TTL-compatible and the device operates from a single 5 volt supply. Fully static asynchronous

FUNCTIONAL BLOCK DIAGRAM



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The IDT logo is a registered trademark of Integrated Device Technology, Inc.

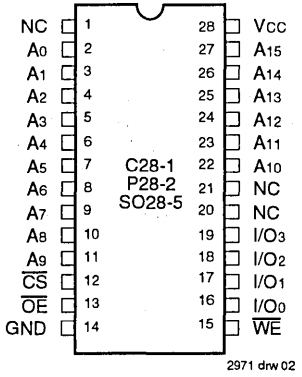
DESCRIPTION (Continued)

circuitry, along with matching access and cycle times, favor the simplified system design approach.

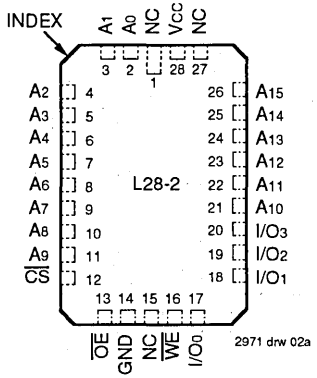
The IDT61298SA is packaged in a 28-pin Sidebraze or Plastic 300 mil DIP, an SOJ, plus an LCC, providing improved board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



DIP/SOJ
TOP VIEW



LCC
TOP VIEW

TRUTH TABLE[1,2]

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
L	L	H	$DATA_{OUT}$	Read Data
L	X	L	$DATA_{IN}$	Write Data
L	H	H	High-Z	Outputs Disabled
H	X	X	High-Z	Deselected - Standby (I_{SB})
V_{HC}[3]	X	X	High-Z	Deselected - Standby (I_{SB1})

NOTES: 2971 tbl 01
1. H = V_{IH}, L = V_{IL}, x = Don't care.
2. V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V.
3. Other inputs ≥V_{HC} or ≤V_{LC}.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTES: 2971 tbl 02
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 0.5V.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, SOJ Package)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	7	pF

NOTE: 2971 tbl 03
1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2971 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	V_{CC} + 0.5V	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 2971 tbl 05
1. V_{IL} (min.) = –1.5V for pulse width less than 10ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	61298SA15		61298SA17		61298SA20		61298SA25		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = f_{MAX}[2]	140	—	135	—	130	140	—	120	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}[2]	45	—	40	—	40	45	—	40	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., f = 0[2], V_{LC} ≥ V_{IN} ≥ V_{HC}	20	—	20	—	20	30	—	30	mA

NOTES: 2971 tbl 06
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.

7

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2971 tbl 07

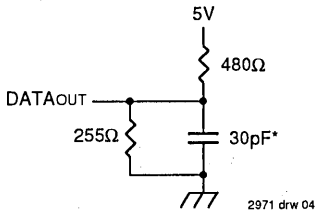


Figure 1. AC Test Load

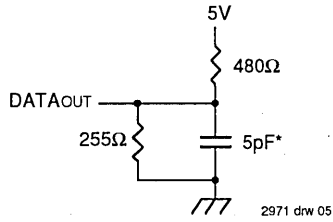


Figure 2. AC Test Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

*Includes scope and jig capacitances

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT61298SA Min.	Typ.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min. I_{OL} = 10mA, V_{CC} = Min.	— —	— —	0.4 0.5	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	—	V

2971 tbl 09

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

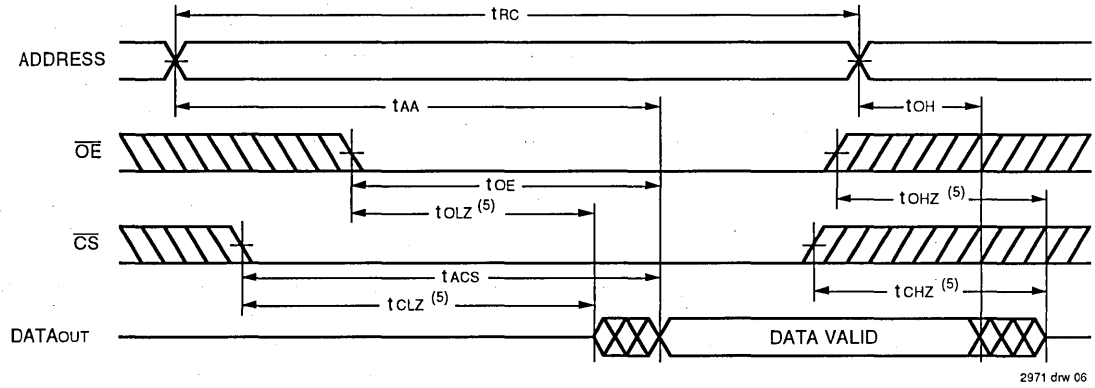
Symbol	Parameter	61298SA15[1]		61298SA17[1]		61298SA20		61298SA25[2]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
tRC	Read Cycle Time	15	—	17	—	20	—	25	—	ns
tAA	Address Access Time	—	15	—	17	—	20	—	25	ns
tACS	Chip Select Access Time	—	15	—	17	—	20	—	25	ns
tCLZ[3]	Chip Select to Output in Low-Z	4	—	4	—	4	—	4	—	ns
tCHZ[3]	Chip Deselect to Output in High-Z	—	7	—	8	—	8	—	9	ns
tOE	Output Enable to Output Valid	—	7	—	8	—	8	—	9	ns
tOLZ[3]	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	ns
tOHZ[3]	Output Disable to Output in High-Z	—	6	—	7	—	8	—	9	ns
tOH	Output Hold from Address Change	4	—	4	—	4	—	4	—	ns
tPU[3]	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
tPD[3]	Chip Deselect to Power-Down Time	—	15	—	17	—	20	—	25	ns
Write Cycle										
tWC	Write Cycle Time	15	—	17	—	20	—	25	—	ns
tCW	Chip Select to End-of-Write	10	—	11	—	12	—	15	—	ns
tAW	Address Valid to End-of-Write	10	—	11	—	12	—	15	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	10	—	11	—	12	—	15	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	7	—	8	—	8	—	10	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tWHZ[3]	Write Enable to Output in High-Z	—	6	—	7	—	8	—	9	ns
tOW[3]	Output Active from End-of-Write	4	—	4	—	4	—	4	—	ns

2971 tbl 10

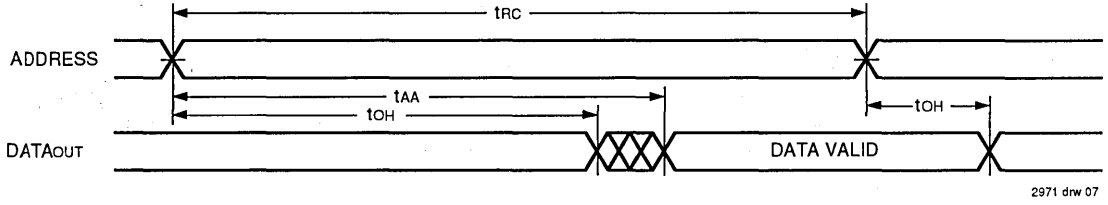
NOTES:
1. 0° to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. This parameter is guaranteed with AC test load (Figure 2) by device characterization, but is not production tested.

7

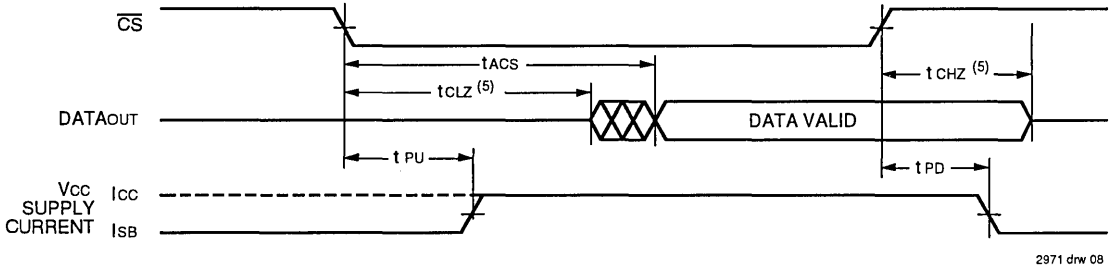
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)

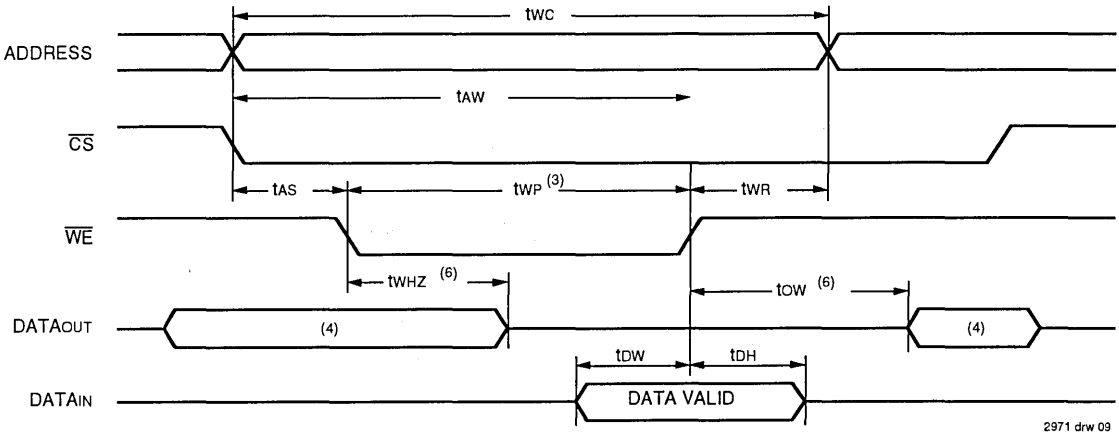


TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)

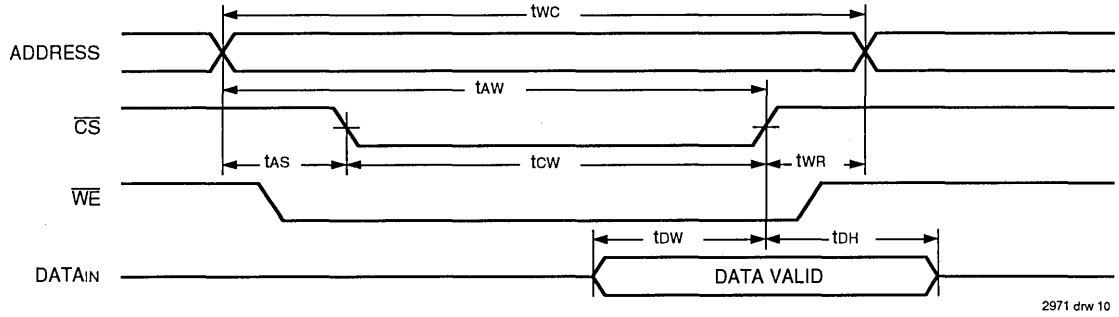


NOTES:
1. $\overline{WE}$ is HIGH for read cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1,2,3,5)



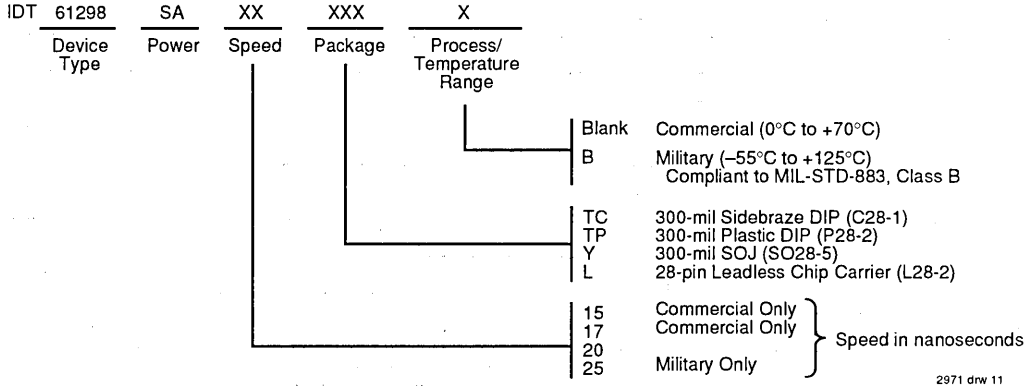
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1,2,5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. $\overline{OE}$ is continuously HIGH. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the greater than or equal to tWHZ + tDW to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified tWP.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state.

7

ORDERING INFORMATION



Integrated Device Technology, Inc.

BiCMOS STATIC RAM 256K (64K x 4-BIT)

IDT61B298

FEATURES:

- 64K x 4 BiCMOS Static RAM
- High-speed address/chip select time
  - — Commercial: 12/15/20ns
  - — Military: 15/20ns
- Output Enable
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Available in 28-pin 300 mil plastic DIP, 28-pin 300 mil Sidebraze DIP and 28-pin 300-mil plastic SOJ

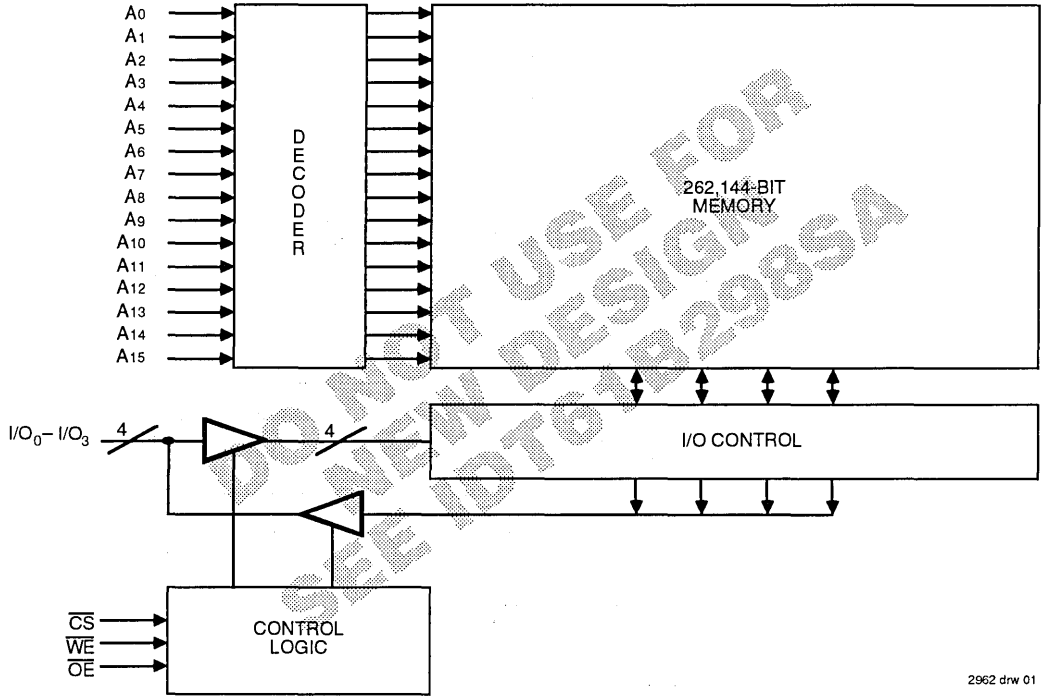
DESCRIPTION:

The IDT61B298 is a 262,144-bit high-speed static RAM organized as 64Kx4. It is fabricated using IDT's high-perfomance high-reliability BiCMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

Address access times as fast as 12ns are available. All inputs and outputs of the IDT61B298 are TTL-compatible and operation is from a single 5V supply.

The IDT61B298 is packaged in a 28-pin 300 mil plastic DIP, 28-pin 300 mil ceramic DIP and a 28-pin 300 mil SOJ.

FUNCTIONAL BLOCK DIAGRAM



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Integrated Device Technology, Inc.

BiCMOS STATIC RAM 256K (64K x 4-BIT)

PRELIMINARY
IDT61B298SA

FEATURES:

- 64K x 4 advanced high-speed BiCMOS static RAM
- Equal access and cycle times
  - — Commercial: 10/12/15ns
- One Chip Select plus one Output Enable pin
- Bidirectional data inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Available in 28-pin Plastic DIP and SOJ packages

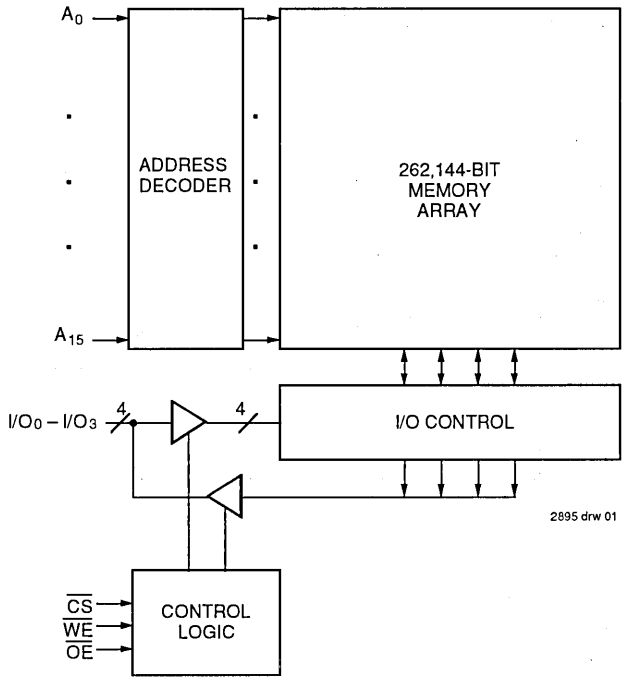
DESCRIPTION:

The IDT61B298SA is a 262,144-bit high-speed Static RAM organized as 64K x 4. It is fabricated using IDT's high-perfomance, high-reliability BiCMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

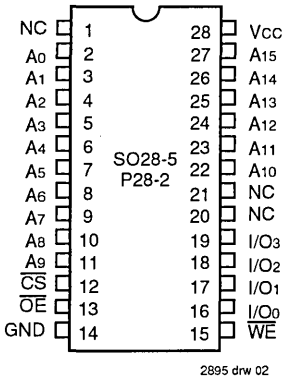
The IDT61B298SA has an output enable pin which operates as fast as 5ns, with address access times as fast as 10ns. All bidirectional inputs and outputs of the IDT61B298SA are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

The IDT61B298SA is packaged in 28-pin 300 mil Plastic DIP and 28-pin 300 mil Plastic SOJ packages.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



2895 drw 02

DIP/SOJ
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.25	W
I_{OUT}	DC Output Current	50	mA

NOTES: 2895 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 0.5V.

TRUTH TABLE(1,2)

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
L	L	H	$DATA_{OUT}$	Read Data
L	X	L	$DATA_{IN}$	Write Data
L	H	H	High-Z	Outputs Disabled
H	X	X	High-Z	Deselected - Standby (I_{SB})
V_{HC}(3)	X	X	High-Z	Deselected - Standby (I_{SB1})

NOTES: 2895 tbl 01

1. H = V_{IH}, L = V_{IL}, X = Don't care.
2. V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V.
3. Other inputs ≥V_{HC} or ≤V_{LC}.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	6	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

NOTE: 2895 tbl 03

1. This parameter is guaranteed by device characterization, but not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	V_{CC}+0.5	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2895 tbl 04

1. V_{IL} (min.) = –1.5V for pulse width less than 10ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT61B298SA Min.	IDT61B298SA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	—	V

2895 tbl 05

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC}–0.2V)

Symbol	Parameter	61B298SA10		61B298SA12		61B298SA15		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Dynamic Operating Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	170	—	160	—	150	—	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \ge V_{IH}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	45	—	40	—	35	—	mA
I_{SB1}	Standby Power Supply Current (CMOS Level) $\overline{CS} \ge V_{HC}$, Outputs Open, V_{CC} = Max., f = 0[2] $V_{IN} \le V_{LC}$ or $V_{IN} \ge V_{HC}$	35	—	35	—	35	—	mA

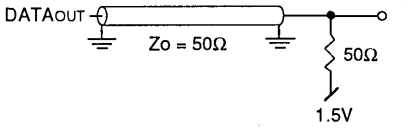
NOTES:
2895 tbl 06

1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.

AC TEST CONDITIONS

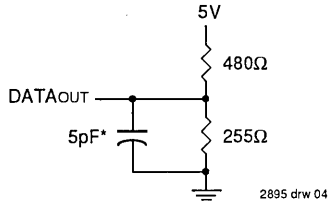
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1, 2, and 3

2895 tbl 07



2895 drw 03

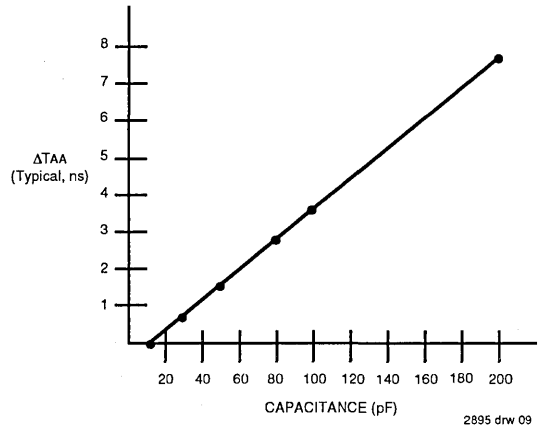
Figure 1. AC Test Load



2895 drw 04

*Including jig and scope capacitance.

Figure 2. AC Test Load (for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})



2895 drw 09

Figure 3. Lumped Capacitive Load, typical Derating

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, Commercial Temperature Range)

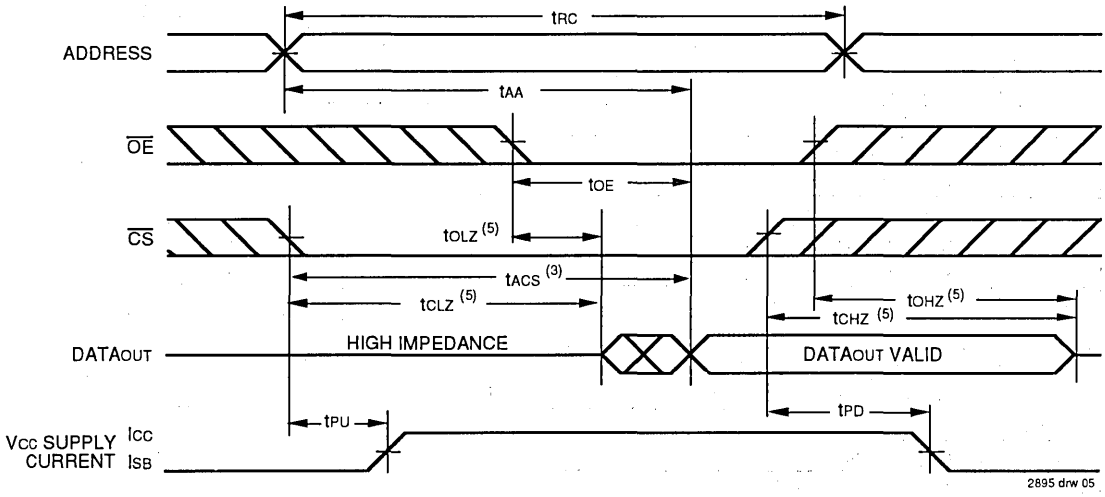
Symbol	Parameter	61B298SA10		61B298SA12		61B298SA15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	10	—	12	—	15	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	ns
t_{ACS}	Chip Select Access Time	—	10	—	12	—	15	ns
t_{CLZ}(1)	Chip Select to Output in Low-Z	2	—	2	—	2	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High-Z	0	5	0	6	0	7	ns
t_{OE}	Output Enable to Output Valid	—	5	—	6	—	7	ns
t_{OLZ}(1)	Output Enable to Output in Low-Z	2	—	2	—	2	—	ns
t_{OHZ}(1)	Output Disable to Output in High-Z	0	4	0	4	0	5	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{PU}(1)	Chip Select to Power Up Time	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power Down Time	—	10	—	12	—	15	ns
Write Cycle								
t_{WC}	Write Cycle Time	10	—	12	—	15	—	ns
t_{AW}	Address Valid to End of Write	9	—	9	—	10	—	ns
t_{CW}	Chip Select to End of Write	7	—	8	—	9	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	7	—	8	—	9	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	5	—	6	—	7	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{OW}(1)	Output Active from End of Write	2	—	2	—	2	—	ns
t_{WHZ}(1)	Write Enable to Output in High-Z	0	6	0	6	0	7	ns

NOTE:
1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

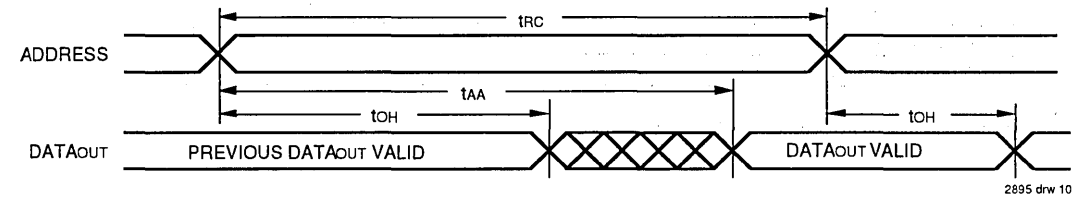
2695 tbl 08

7

TIMING WAVEFORM OF READ CYCLE NO. 1(1)

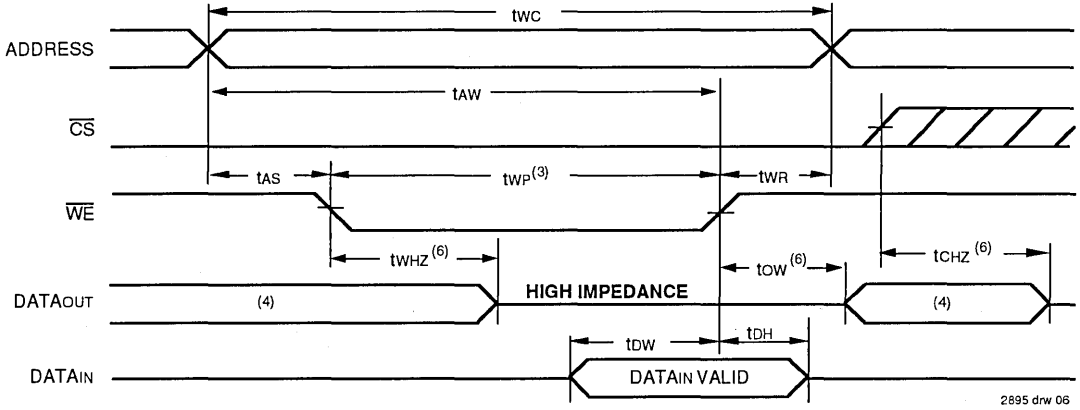


TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)

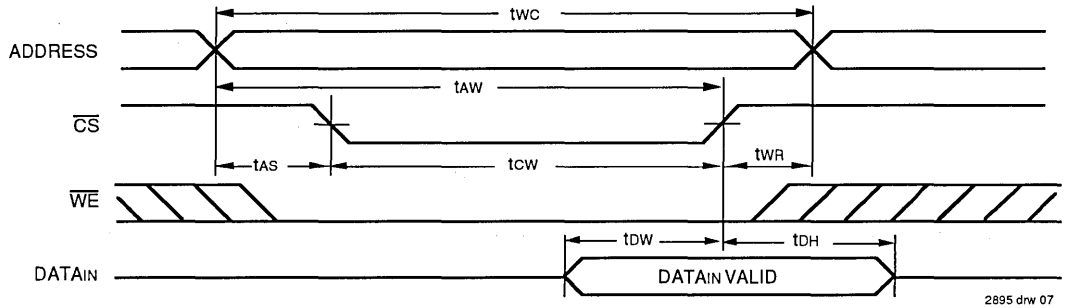


NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address must be valid prior to or coincident with the later of $\overline{CS}$ transition LOW; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ CONTROLLED TIMING)(1,2,3,5)

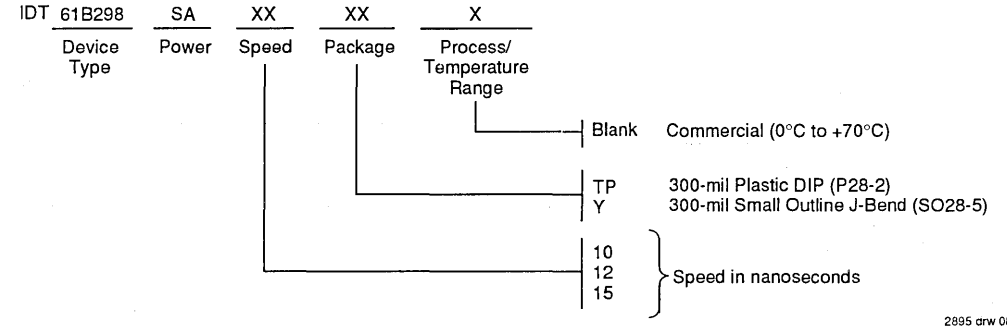


TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ CONTROLLED TIMING)(1,2,5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP}.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state.

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS STATIC RAM 256K (32K x 8-BIT)

IDT71256S
IDT71256L

FEATURES:

- High-speed address/chip select time
  - — Military: 25/30/35/45/55/70/85/100/120/150ns (max.)
  - — Commercial: 20/25/35/45ns (max.)
- Low-power operation
- Battery Backup operation — 2V data retention
- Produced with advanced high-performance CMOS technology
- Input and output directly TTL-compatible
- Available in standard 28-pin (600 mil) CERDIP, 28-pin (300 or 600 mil) plastic DIP, 28-pin (300 mil) ceramic sidebraze DIP, 28-pin (330 mil) SOIC and (300 mil) SOJ, 28-pin CERPACK, 32-pin LCC or PLCC, 28-pin LCC
- Military product compliant to MIL-STD-883, Class B
- This function is listed as Standard Military Drawing #5962-88552 (L-Power) and #5962-88662 (S-Power)

DESCRIPTION:

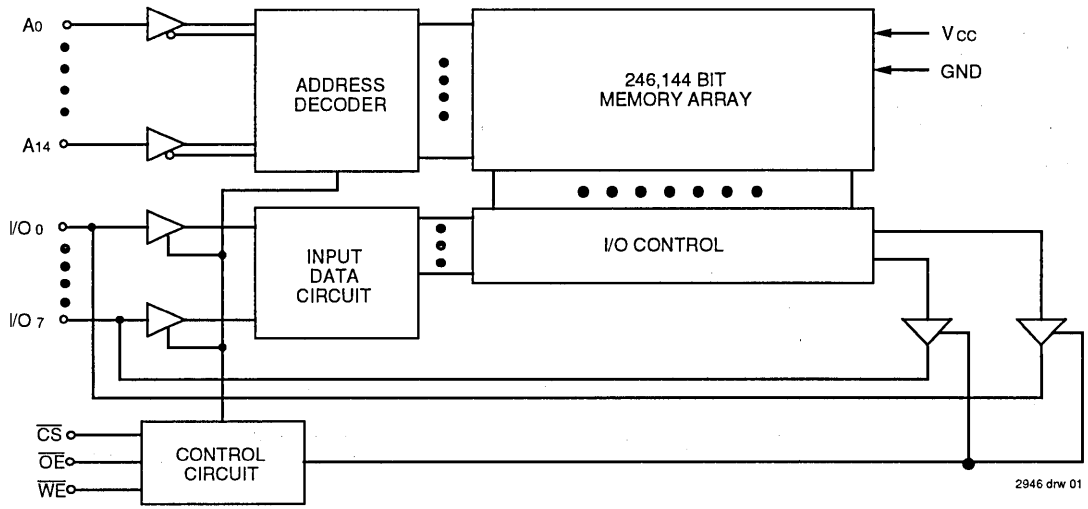
The IDT71256 is a 262,144-bit high-speed static RAM organized as 32K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology.

Address access times as fast as 20ns are available with power consumption of only 350mW (typ.). The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes HIGH, the circuit will automatically go to, and remain in, a low-power standby mode as long as $\overline{CS}$ remains HIGH. In the full standby mode, the low-power device consumes less than 15µW, typically. This capability provides significant system level power and cooling savings. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 5µW when operating off a 2V battery.

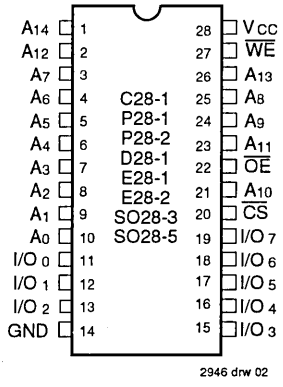
The IDT71256 is packaged in a 28-pin (330 mil) gull-wing or 300 mil J-bend SOIC, a 28-pin 600 mil CERDIP, 28-pin (300 or 600 mil) plastic DIP, 28-pin (300 mil) ceramic sidebraze DIP, 28-pin CERPACK, 32-pin LCC or PLCC, 28-pin LCC, providing high board-level packing densities.

The IDT71256 military RAM is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

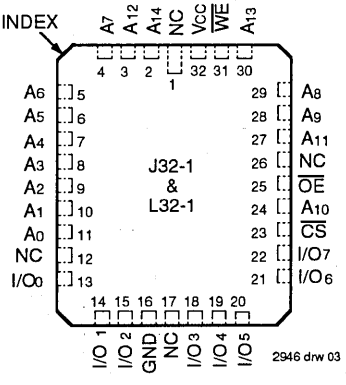
FUNCTIONAL BLOCK DIAGRAM



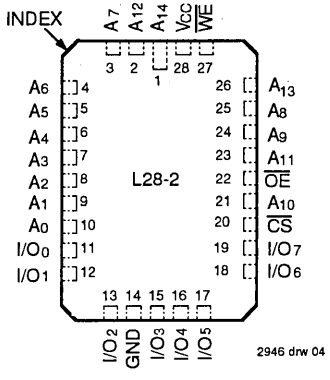
PIN CONFIGURATIONS



DIP/SOJ/SOIC TOP VIEW



32-Pin LCC/PLCC TOP VIEW



28-Pin LCC TOP VIEW

PIN DESCRIPTIONS

Name	Description
A0–A14	Addresses
I/O0–I/O7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
VCC	Power

2946 tbl 01

TRUTH TABLE(1)

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	I/O	Function
X	H	X	High-Z	Standby (ISB)
X	VHC	X	High-Z	Standby (ISB1)
H	L	H	High-Z	Output Disabled
H	L	L	DOUT	Read Data
L	L	X	DIN	Write Data

NOTE: 2946 tbl 02
1. H = VIH, L = VIL, X = Don't Care

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

NOTE: 2946 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	11	pF
COUT	Output Capacitance	VOUT = 0V	11	pF

NOTE: 2946 tbl 04
1. This parameter is determined by device characterization, but is not production tested.

7

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2946 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE:
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns, once per cycle.

2946 tbl 06

DC ELECTRICAL CHARACTERISTICS[1, 2]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	71256x20		71256x25		71256x30		71256x35		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Dynamic Operating Current $\overline{CS} \le V_{IL}$, Outputs Open V_{CC} = Max., f = f_{MAX}[3]	S	155	—	145	150	—	145	135	140	mA
		L	135	—	115	130	—	125	105	120	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \ge V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}[3]	S	20	—	20	20	—	20	20	20	mA
		L	3	—	3	3	—	3	3	3	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \ge V_{HC}$, V_{CC} = Max., f = 0	S	15	—	15	20	—	20	15	20	mA
		L	0.4	—	0.4	1.5	—	1.5	0.4	1.5	

Symbol	Parameter	Power	71256x45		71256x55		71256x70		71256x85[5]		71256x100		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Dynamic Operating Current $\overline{CS} \le V_{IL}$, Outputs Open V_{CC} = Max., f = f_{MAX}[3]	S	130	135	—	135	—	135	—	135	—	135	mA
		L	100	115	—	115	—	115	—	115	—	115	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \ge V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}[3]	S	20	20	—	20	—	20	—	20	—	20	mA
		L	3	3	—	3	—	3	—	3	—	3	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \ge V_{HC}$, V_{CC} = Max., f = 0	S	15	20	—	20	—	20	—	20	—	20	mA
		L	0.4	1.5	—	1.5	—	1.5	—	1.5	—	1.5	

NOTES:
1. All values are maximum guaranteed values.
2. An "x" in part numbers indicates power rating (S or L).
3. f_{MAX} = 1/t_{RC}, all address inputs cycling at f_{MAX}; f = 0 means no address pins are cycling.
4. Standby current mode not available at 20ns.
5. Also available: 120 and 150 ns military devices.

2946 tbl 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2946 tbl 08

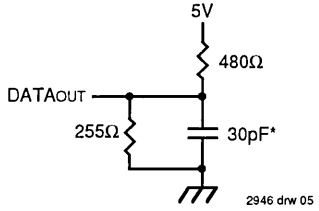


Figure 1. AC Test Load

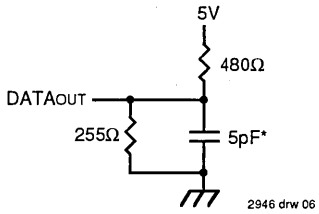


Figure 2. AC Test Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

*Includes scope and jig capacitances

7

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT71256S Min.	IDT71256S Typ.	IDT71256S Max.	IDT71256L Min.	IDT71256L Typ.	IDT71256L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	—	—	10	—	—	5	µA
			COM'L.	—	—	5	—	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	—	—	10	—	—	5	µA
			COM'L.	—	—	5	—	—	2	
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.			—	0.4	—	—	0.4	V
		I_{OL} = 10mA, V_{CC} = Min.		—	—	0.5	—	—	0.5	
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.		2.4	—	—	2.4	—	—	V

2946 tbl 09

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V

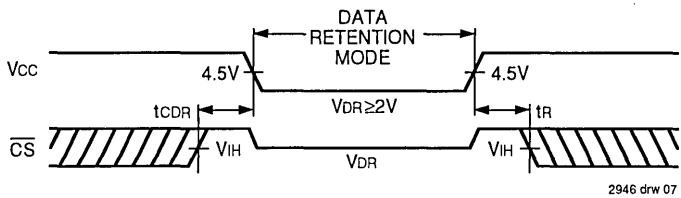
Symbol	Parameter	Test Condition		Min.	Typ.[1] Vcc @ 2.0v	Typ.[1] Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current		MIL.	—	—	—	500	800	µA
			COM'L.	—	—	—	120	200	
t_{CDR}	Chip Deselect to Data Retention Time	$\overline{CS} \geq V_{HC}$		0	—	—	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	—	—	ns

NOTES:

2946 tbl 10

1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

LOW Vcc DATA RETENTION WAVEFORM



2946 drw 07

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71256S20[1] 71256L20[1]		71256S25 71256L25		71256S30[3] 71256L30[3]		71256S35 71256L35		71256S45 71256L45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
tRC	Read Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
tAA	Address Access Time	—	20	—	25	—	30	—	35	—	45	ns
tACS	Chip Select Access Time	—	20	—	25	—	30	—	35	—	45	ns
tCLZ[2]	Chip Select to Output in Low-Z	5	—	5	—	5	—	5	—	5	—	ns
tCHZ[2]	Chip Deselect to Output in High-Z	—	10	—	11	—	15	—	15	—	20	ns
tOE	Output Enable to Output Valid	—	10	—	11	—	13	—	15	—	20	ns
tOLZ[2]	Output Enable to Output in Low-Z	2	—	2	—	2	—	2	—	0	—	ns
tOHZ[2]	Output Disable to Output in High-Z	2	8	2	10	2	12	2	15	—	20	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
Write Cycle												
tWC	Write Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
tCW	Chip Select to End-of-Write	15	—	20	—	25	—	30	—	40	—	ns
tAW	Address Valid to End-of-Write	15	—	20	—	25	—	30	—	40	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	15	—	20	—	25	—	30	—	35	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data to Write Time Overlap	11	—	13	—	14	—	15	—	20	—	ns
tWHZ[2]	Write Enable to Output in High-Z	—	10	—	11	—	15	—	15	—	20	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	0	—	0	—	ns
tOW[2]	Output Active from End-of-Write	5	—	5	—	5	—	5	—	5	—	ns

NOTES:
1. 0° to +70°C temperature range only.
2. This parameter guaranteed by device characterization, but is not production tested.
3. –55° to +125°C temperature range only.

2968 tbl 11

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AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

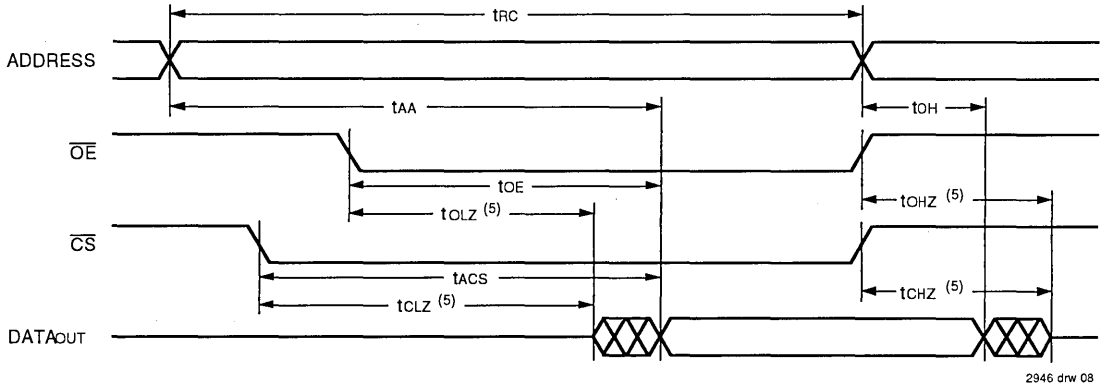
Symbol	Parameter	71256S55[1] 71256L55[1]		71256S70[1] 71256L70[1]		71256S85[1] 71256L85[1]		71256S100[1,3] 71256L100[1,3]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	55	—	70	—	85	—	100	—	ns
t_{AA}	Address Access Time	—	55	—	70	—	85	—	100	ns
t_{ACS}	Chip Select Access Time	—	55	—	70	—	85	—	100	ns
t_{CLZ}[2]	Chip Deselect to Output in Low-Z	5	—	5	—	5	—	5	—	ns
t_{CHZ}[2]	Output Enable to Output in Low-Z	—	25	—	30	—	35	—	40	ns
t_{OE}	Output Enable to Output Valid	—	25	—	30	—	35	—	40	ns
t_{OLZ}[2]	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	ns
t_{OHZ}[2]	Output Disable to Output in High-Z	0	25	0	30	—	35	—	40	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
Write Cycle										
t_{WC}	Write Cycle Time	55	—	70	—	85	—	100	—	ns
t_{CW}	Chip Select to End-of-Write	50	—	60	—	70	—	80	—	ns
t_{AW}	Address Valid to End-of-Write	50	—	60	—	70	—	80	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	40	—	45	—	50	—	55	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data to Write Time Overlap	25	—	30	—	35	—	40	—	ns
t_{DH}	Data Hold from Write Time ($\overline{WE}$)	0	—	0	—	0	—	0	—	ns
t_{WHZ}[2]	Write Enable to Output in High-Z	—	25	—	30	—	35	—	40	ns
t_{OW}[2]	Output Active from End-of-Write	5	—	5	—	5	—	5	—	ns

NOTES:

2968 tbl 11

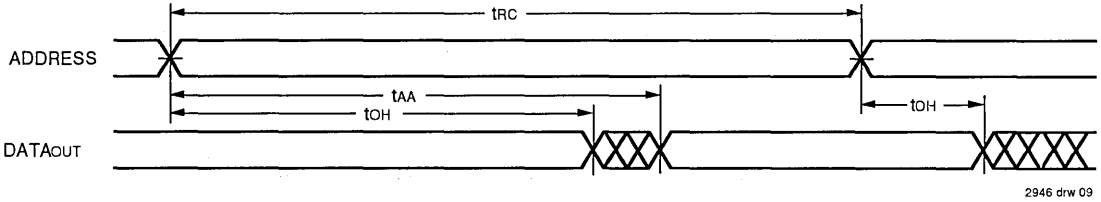
1. -55°C to +125°C temperature range only.
2. This parameter guaranteed by device characterization, but is not production tested.
3. Also available: 120 and 150 ns military devices.

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



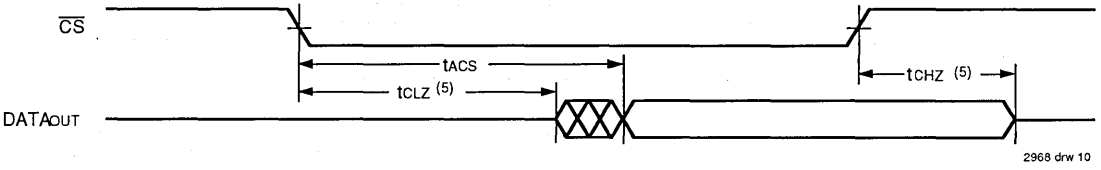
2946 drw 08

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2946 drw 09

TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



2968 drw 10

NOTES:
1. $\overline{WE}$ is HIGH for read cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state.

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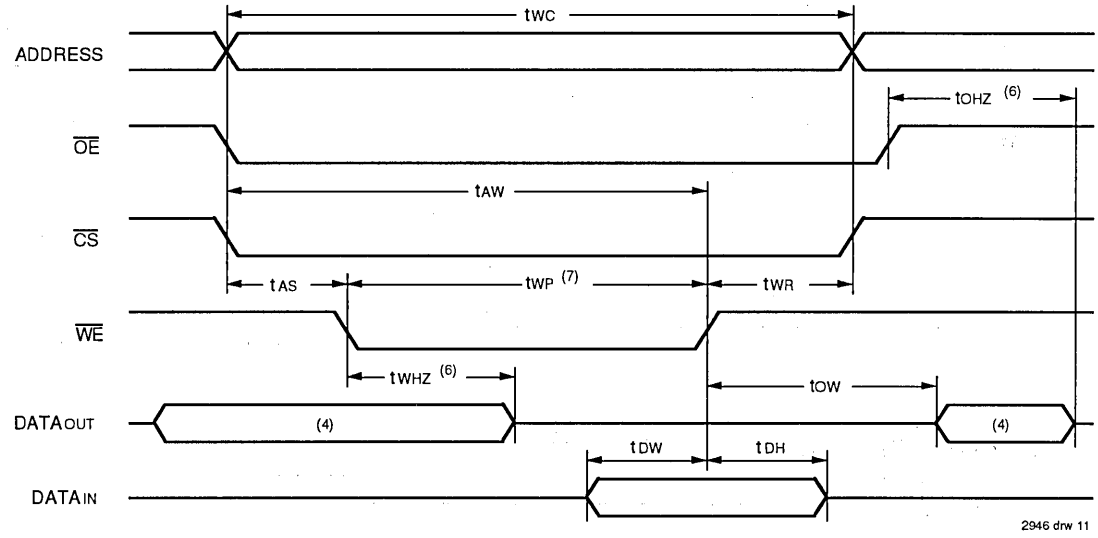
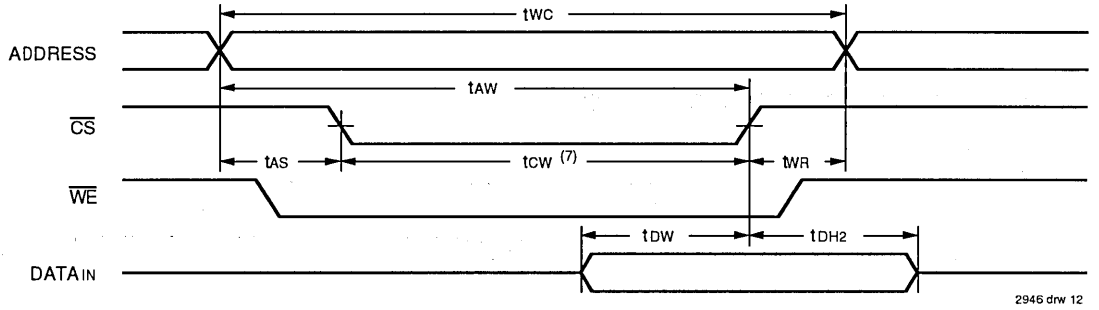
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 5, 7)

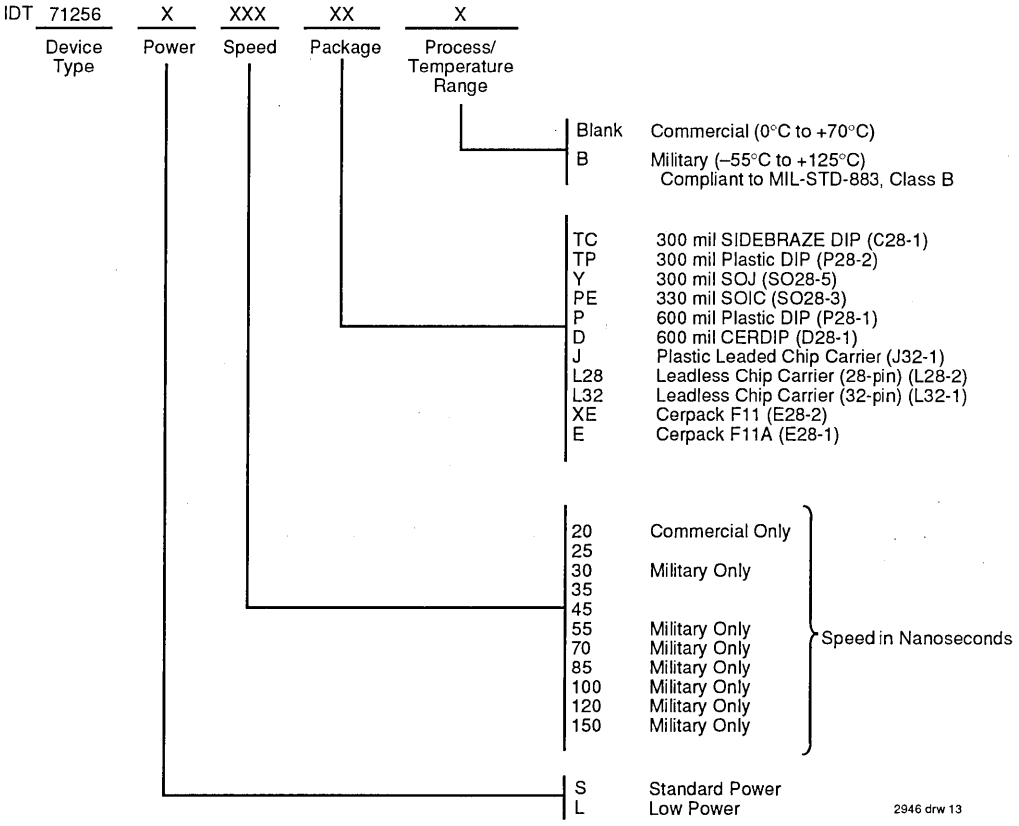


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state.
7. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the spectified tWP. For a $\overline{CS}$ controlled write cycle, $\overline{OE}$ may be LOW with no degradation to tCW.

ORDERING INFORMATION



7

Integrated Device Technology, Inc.

CMOS STATIC RAM 256K (32K x 8-BIT)

PRELIMINARY
IDT71256SA

FEATURES:

- 32K x 8 advanced high-speed CMOS static RAM
- Equal access and cycle times
  - — Military: 17/20ns
  - — Commercial: 15/17ns
- One Chip Select plus one Output Enable pin
- Bidirectional data inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Military product compliant to MIL-STD-883, Class B
- Available in 28-pin Sidebraze DIP, Plastic DIP, Plastic SOJ, and 32-pin LCC packages

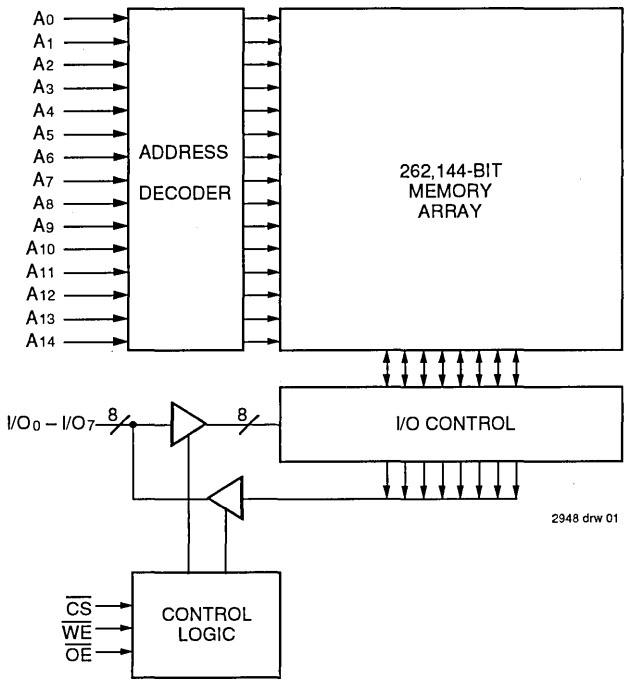
DESCRIPTION:

The ID71256SA is a 262,144-bit high-speed Static RAM organized as 32K x 8. It is fabricated using IDT's high-perfomance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

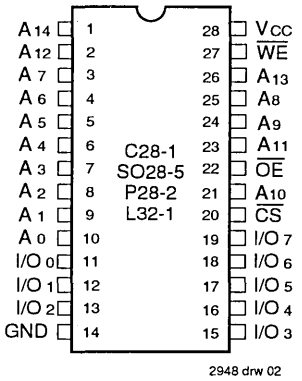
The IDT71256SA has an output enable pin which operates as fast as 7ns, with address access times as fast as 15ns. All bidirectional inputs and outputs of the IDT71256SA are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

The IDT71256SA is packaged in 28-pin 300 mil Sidebraze DIP, 28-pin 300 mil Plastic DIP, 28-pin 300 mil Plastic SOJ, and 32-pin Leadless Chip Carrier packages.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



2948 drw 02

DIP/SOJ
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.25	1.25	W
I_{OUT}	DC Output Current	50	50	mA

NOTES: 2948 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 0.5V.

TRUTH TABLE(1,2)

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
L	L	H	$DATA_{OUT}$	Read Data
L	X	L	$DATA_{IN}$	Write Data
L	H	H	High-Z	Outputs Disabled
H	X	X	High-Z	Deselected — Standby (I_{SB})
V_{HC}(3)	X	X	High-Z	Deselected — Standby (I_{SB1})

NOTES: 2948 tbl 01

1. H = V_{IH}, L = V_{IL}, x = Don't care.
2. V_{LC} = 0.2V, V_{HC} = V_{CC} –0.2V.
3. Other inputs ≥V_{HC} or ≤V_{LC}.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	5	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

NOTE: 2948 tbl 03

1. This parameter is guaranteed by device characterization, but not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	V_{CC}+0.5	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2948 tbl 04

1. V_{IL} (min.) = –1.5V for pulse width less than 10ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71256SA Min.	IDT71256SA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

2948 tbl 05

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC}–0.2V)

Symbol	Parameter	71256SA15		71256SA17		71256SA20		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	150	—	145	160	—	150	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	45	—	40	50	—	45	mA
I_{SB1}	Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, Outputs Open, V_{CC} = Max., f = 0[2] $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$	20	—	20	30	—	30	mA

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.

2948 tbl 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2948 tbl 07

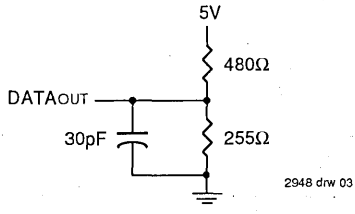
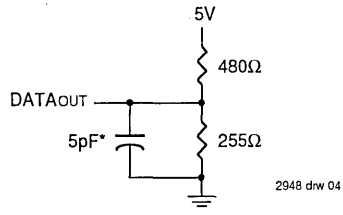


Figure 1. AC Test Load



*Including jig and scope capacitance.

Figure 2. AC Test Load (for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

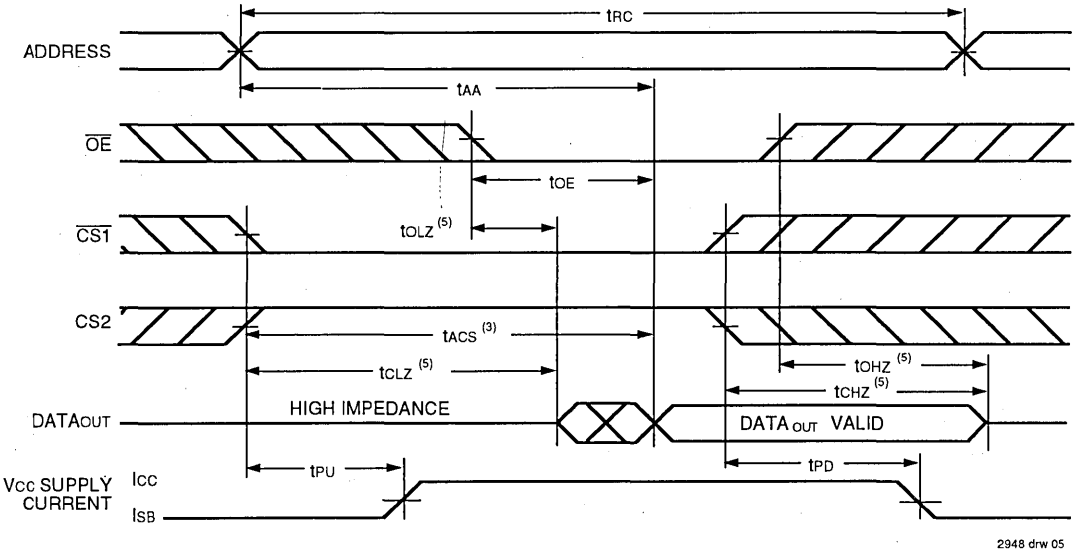
Symbol	Parameter	71256SA15[1]		71256SA17		71256SA20[2]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	15	—	17	—	20	—	ns
t_{AA}	Address Access Time	—	15	—	17	—	20	ns
t_{ACS}	Chip Select Access Time	—	15	—	17	—	20	ns
t_{CLZ}[3]	Chip Select to Output in Low-Z	4	—	4	—	4	—	ns
t_{CHZ}[3]	Chip Deselect to Output in High-Z	0	7	0	8	0	8	ns
t_{OE}	Output Enable to Output Valid	—	7	—	8	—	8	ns
t_{OLZ}[3]	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
t_{OHZ}[3]	Output Disable to Output in High-Z	0	6	0	7	0	8	ns
t_{OH}	Output Hold from Address Change	4	—	4	—	4	—	ns
t_{PU}[3]	Chip Select to Power Up Time	0	—	0	—	0	—	ns
t_{PD}[3]	Chip Deselect to Power Down Time	—	15	—	17	—	20	ns
Write Cycle								
t_{WC}	Write Cycle Time	15	—	17	—	20	—	ns
t_{AW}	Address Valid to End of Write	10	—	11	—	12	—	ns
t_{CW}	Chip Select to End of Write	10	—	11	—	12	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	10	—	11	—	12	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	7	—	8	—	8	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{OW}[3]	Output Active from End of Write	4	—	4	—	4	—	ns
t_{WHZ}[3]	Write Enable to Output in High-Z	0	6	0	7	0	8	ns

NOTES:
1. 0° to +70°C temperature range only.
2. -55° to +125°C temperature range only.
3. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

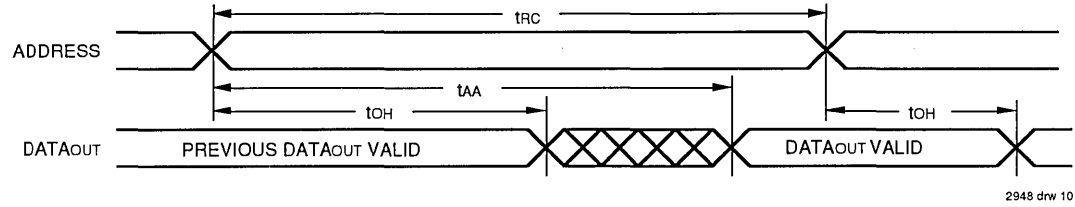
2948 tbl 08

7

TIMING WAVEFORM OF READ CYCLE NO. 1(1)

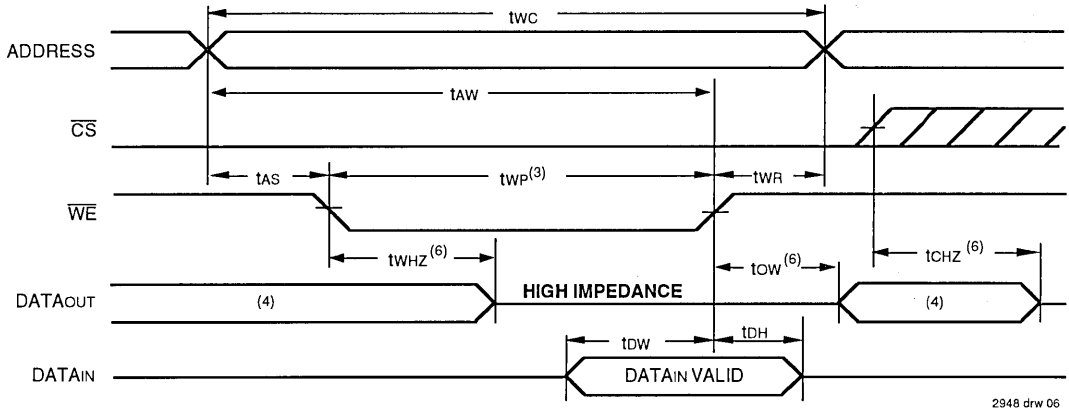


TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)

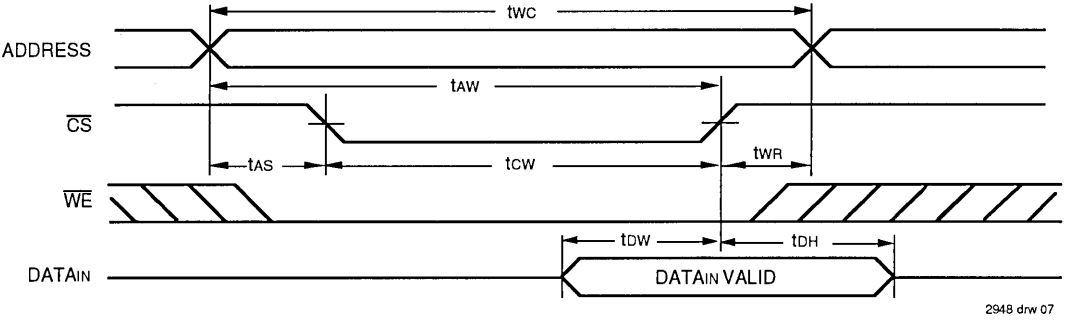


NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address must be valid prior to or coincident with the later of $\overline{CS}$ transition LOW; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ CONTROLLED TIMING)(1,2,3,5)



TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ CONTROLLED TIMING)(1,2,5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, tWP must be greater than or equal to tWHZ + tDW to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified tWP.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state.

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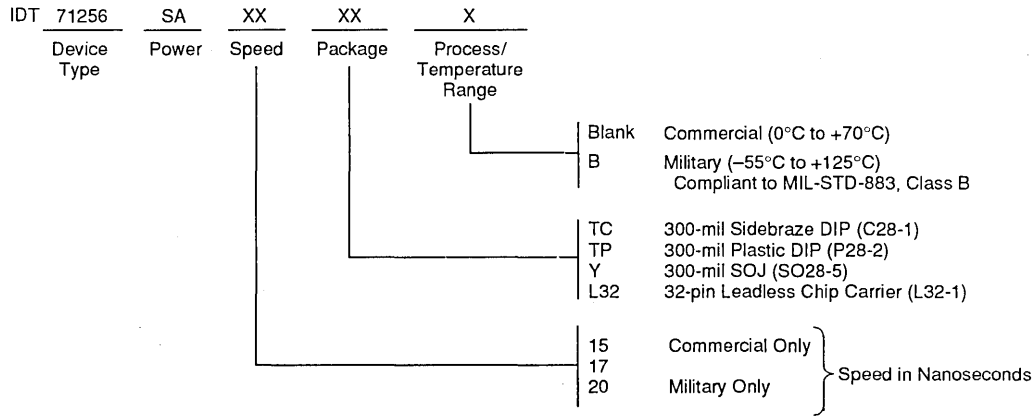
ORDERING INFORMATION



2948 drw 08

Integrated Device Technology, Inc.

BiCMOS STATIC RAM 256K (32K x 8-BIT)

IDT71B256

FEATURES:

- 32K x 8 BiCMOS Static RAM
- High-speed address /chip select time
  - — Military: 20ns
  - — Commercial: 12/15/20ns
- One Chip Select plus one Output Enable pin
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Available in 28-pin sidebraze ceramic, 300 mil DIP; 300 mil plastic DIP and 28-pin, 300 mil plastic SOJ packages

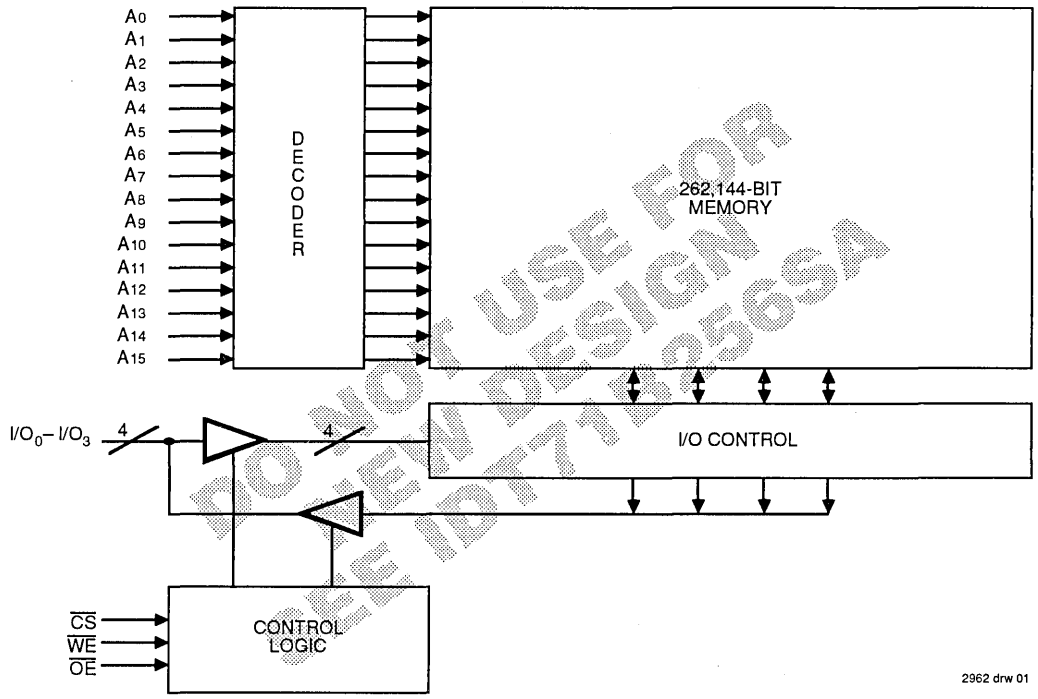
DESCRIPTION:

The IDT71B256 is a 262,144-bit high-speed static RAM organized as 32Kx8. It is fabricated using IDT's high-perfomance high-reliability BiCEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

Address access times as fast as 12ns are available. All inputs and outputs of the IDT71B256 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT71B256 is packaged in a 28-pin, 300-mil sidebraze 28-pin, 300 mil plastic DIP and 28-pin, 300-mil SOJ packages.

FUNCTIONAL BLOCK DIAGRAM



7

Integrated Device Technology, Inc.

BiCMOS STATIC RAM 256K (32K x 8-BIT)

PRELIMINARY
IDT71B256SA

FEATURES:

- 32K x 8 advanced high-speed BiCMOS static RAM
- Equal access and cycle times
  - — Commercial: 10/12/15ns
- One Chip Select plus one Output Enable pin
- Bidirectional inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Available in 28-pin 300 mil plastic DIP and plastic SOJ packages

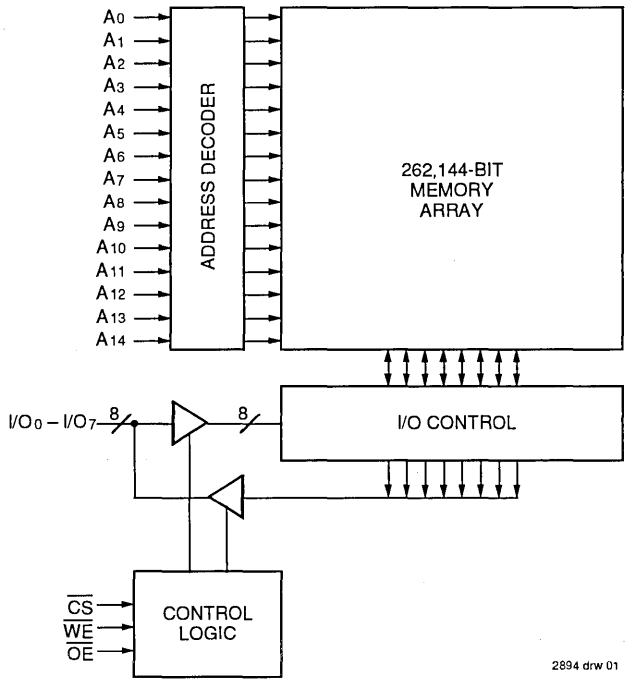
DESCRIPTION:

The IDT71B256SA is a 262,144-bit high-speed static RAM organized as 32K x 8. It is fabricated using IDT's high-perfomance, high-reliability BiCMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

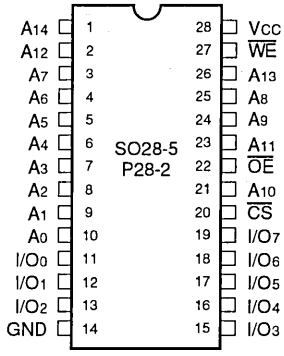
The IDT71B256SA has an output enable pin which operates as fast as 5ns, with address access times as fast as 10ns. All inputs and outputs of the IDT71B256SA are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

The IDT71B256SA is packaged in 28-pin 300 mil plastic DIP and 28-pin 300-mil SOJ packages.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



2894 drw 02

DIP/SOJ
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
P_T	Power Dissipation	1.25	W
I_{OUT}	DC Output Current	50	mA

NOTES: 2894 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 0.5V.

TRUTH TABLE(1,2)

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
L	L	H	$DATA_{OUT}$	Read Data
L	X	L	$DATA_{IN}$	Write Data
L	H	H	High-Z	Output Disabled
H	X	X	High-Z	Deselected - Standby (I_{SB})
V_{HC}(3)	X	X	High-Z	Deselected - Standby (I_{SB1})

NOTES: 2894 tbl 01

1. H = V_{IH}, L = V_{IL}, x = Don't care.
2. V_{LC} = 0.2V, V_{HC} = V_{CC} –0.2V.
3. Other inputs ≥V_{HC} or ≤V_{LC}.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	6	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

NOTE: 2894 tbl 03

1. This parameter is guaranteed by device characterization, but not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	V_{CC}+0.5	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE: 2894 tbl 04

1. V_{IL} (min.) = –1.5V for pulse width less than 10ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71B256SA Min.	IDT71B256SA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	—	V

2894 tbl 05

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC}–0.2V)

Symbol	Parameter	71B256SA10	71B256SA12	71B256SA15	Unit
I_{CC}	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	180	170	160	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	45	40	35	mA
I_{SB1}	Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, Outputs Open, V_{CC} = Max., f = 0(2) $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$	35	35	35	mA

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address lines are changing.

2894 tbl 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1, 2, and 3

2894 tbl 07

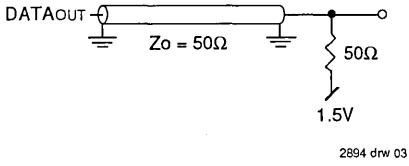
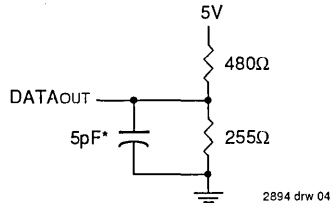


Figure 1. AC Test Load



*Including jig and scope capacitance.

Figure 2. AC Test Load (for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})

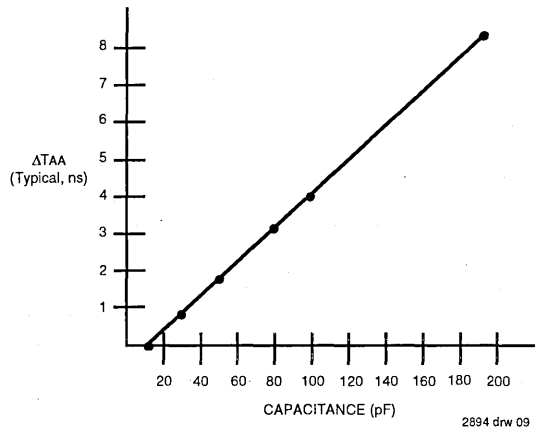


Figure 3. Lumped Capacitive Load, typical Derating

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%)

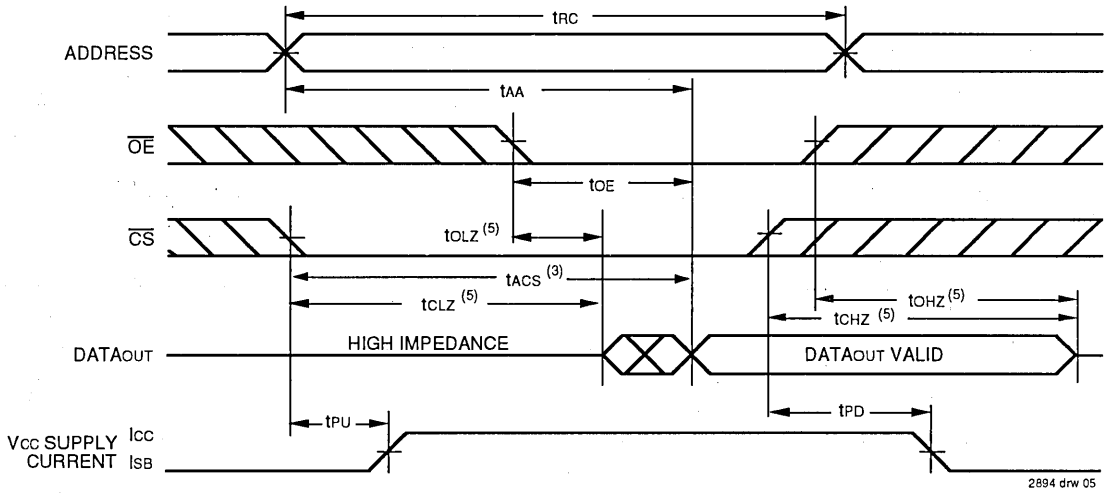
Symbol	Parameter	71B256SA10		71B256SA12		71B256SA15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	10	—	12	—	15	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	ns
t_{ACS}	$\overline{CS}$ Access Time	—	10	—	12	—	15	ns
t_{CLZ}[1]	$\overline{CS}$ to Output in Low-Z	2	—	2	—	2	—	ns
t_{CHZ}[1]	$\overline{CS}$ to Output in High-Z	0	5	0	6	0	7	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	5	—	6	—	7	ns
t_{OLZ}[1]	$\overline{OE}$ to Output in Low-Z	2	—	2	—	2	—	ns
t_{OHZ}[1]	$\overline{OE}$ to Output in High-Z	0	4	0	4	0	5	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Down Time	—	10	—	12	—	15	ns
Write Cycle								
t_{WC}	Write Cycle Time	10	—	12	—	15	—	ns
t_{AW}	Address Valid to End of Write	9	—	9	—	10	—	ns
t_{CW}	$\overline{CS}$ to End of Write	7	—	8	—	9	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	7	—	8	—	9	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	5	—	6	—	7	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	2	—	2	—	2	—	ns
t_{WHZ}[1]	$\overline{WE}$ to Output in High-Z	0	6	0	6	0	7	ns

NOTE:
1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

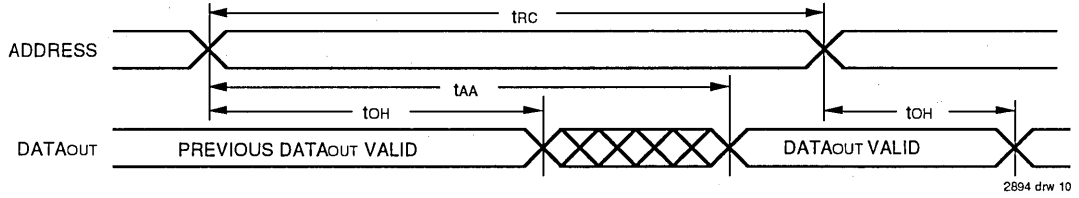
2894 tbl 08

7

TIMING WAVEFORM OF READ CYCLE NO. 1(1)

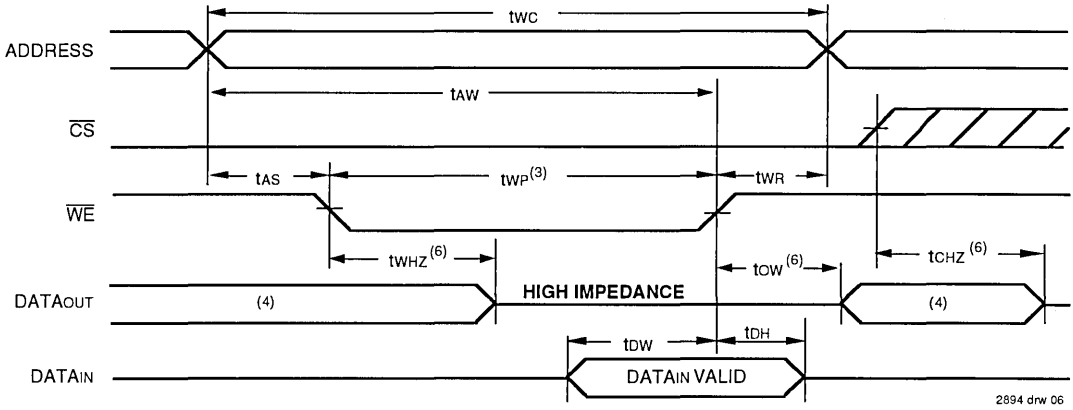


TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)

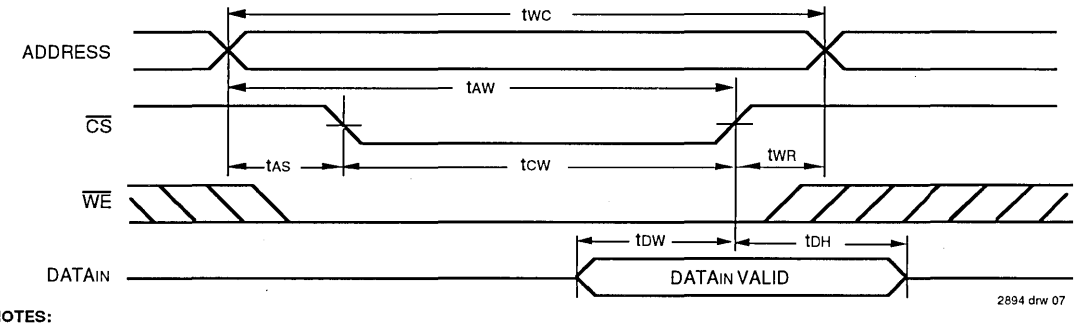


NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address must be valid prior to or coincident with the later of $\overline{CS}$ transition LOW; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ CONTROLLED TIMING)(1,2,3,5)

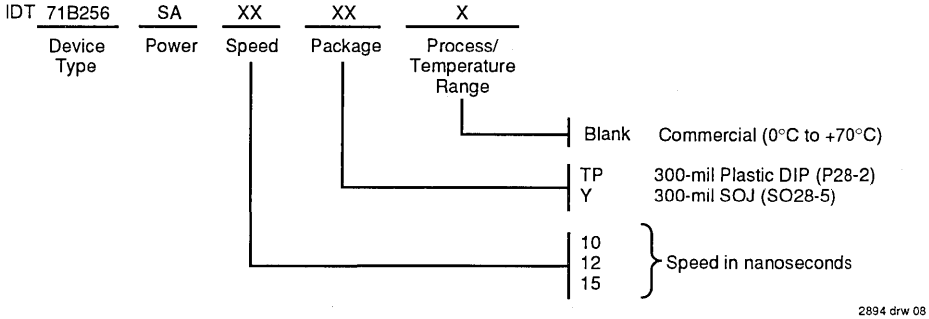


TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ CONTROLLED TIMING)(1,2,5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. During a $\overline{WE}$ controlled write cycle with $\overline{OE}$ LOW, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as t_{WP}.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state.

ORDERING INFORMATION



Integrated Device Technology, Inc.

BiCMOS STATIC RAM 288K (32K x 9-BIT)

PRELIMINARY
IDT71B259

FEATURES:

- 32K x 9 advanced high-speed BiCMOS static RAM
- Equal access and cycle times
  - — Commercial: 10/12/15ns
- Two Chip Selects plus one Output Enable pin
- Bidirectional inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Available in 32-pin plastic SOJ package

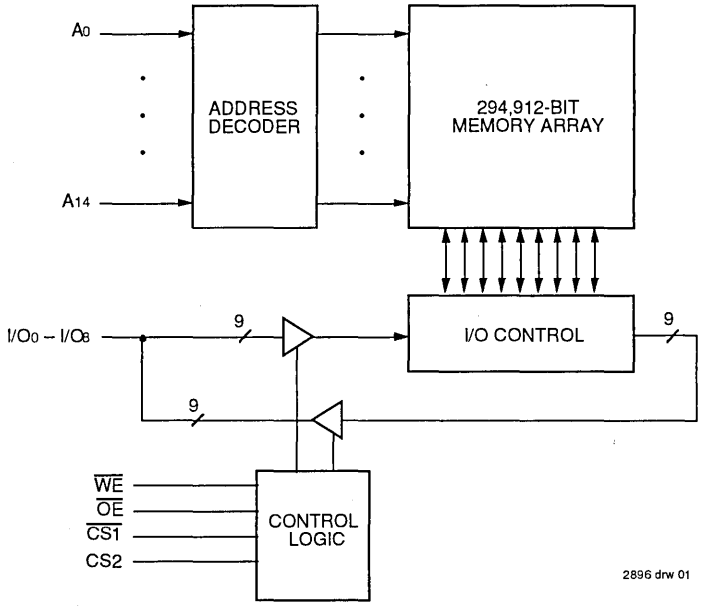
DESCRIPTION:

The IDT71B259 is a 288K high-speed static RAM organized as 32K x 9. It is fabricated using IDT's high-perfomance, high-reliability BiCMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

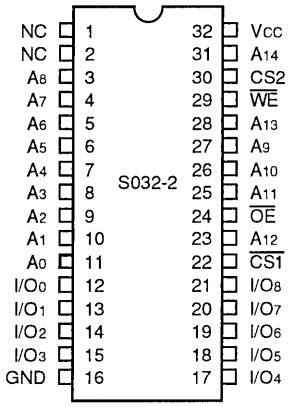
The IDT71B259 has an output enable pin which operates as fast as 5ns, with address access times as fast as 10ns available. All inputs and outputs of the IDT71B259 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used; no clocks or refresh are required for operation.

The IDT71B259 is packaged in a 32-pin 300 mil plastic SOJ package.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



2896 drw 02

SOJ
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTES: 2896 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 0.5V.

TRUTH TABLE(1,2)

INPUTS					
$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	I/O	FUNCTION
X	H	X	X	High-Z	Deselected–Standby (I_{SB})
X	V_{HC}(3)	X	X	High-Z	Deselected–Standby (I_{SB1})
X	X	L	X	High-Z	Deselected–Standby (I_{SB})
X	X	V_{LC}(3)	X	High-Z	Deselected–Standby (I_{SB1})
H	L	H	H	High-Z	Outputs Disabled
H	L	H	L	DOUT	Read Data
L	L	H	X	DIN	Write Data

NOTES: 2896 tbl 01

1. H = V_{IH}, L = V_{IL}, X = Don't care.
2. V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V.
3. Other inputs ≥V_{HC} or ≤V_{LC}.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter(1)	Max.	Unit
C_{IN}	Input Capacitance	6	pF
$C_{I/O}$	I/O Capacitance	7	pF

NOTE: 2896 tbl 03

1. This parameter is guaranteed by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	Vcc+0.5	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2896 tbl 04

1. V_{IL} (min.) = –1.5V for pulse width less than 10ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71B259 Min.	IDT71B259 Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS1}$ = V_{IH}, CS2 = V_{IL}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

2896 tbl 05

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

Symbol	Parameter	71B259S10		71B259S12		71B259S15		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Dynamic Operating Current, CS2 ≥ V_{IH} and $\overline{CS1}$ ≤ V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	175	—	170	—	165	—	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS1}$ ≥ V_{IH} or CS2 ≤ V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	55	—	50	—	45	—	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS1}$ ≥ V_{HC} or CS2 ≤ V_{LC}, Outputs Open, V_{CC} = Max., f = 0[2], V_{IN} ≤ V_{LC} or V_{IN} ≥ V_{HC}	50	—	35	—	35	—	mA

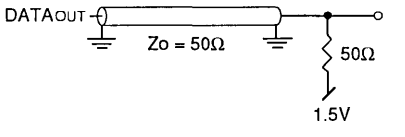
2896 tbl 06

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.

AC TEST CONDITIONS

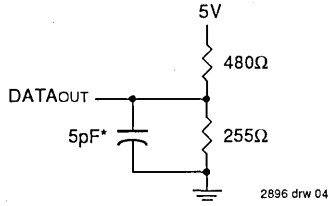
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1, 2, and 3

2896 tbl 07



2896 drw 03

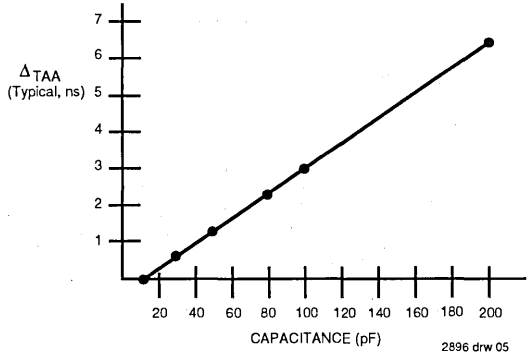
Figure 1. AC Test Load



2896 drw 04

*Including jig and scope capacitance.

Figure 2. AC Test Load (for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})



2896 drw 05

Figure 3. Lumped Capacitive Load, typical Derating

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, Commercial Temperature Range)

Symbol	Parameter	71B259S10		71B259S12		71B259S15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	10	—	12	—	15	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	ns
t_{ACS}	Chip Select Access Time	—	10	—	12	—	15	ns
t_{CLZ}[1]	Chip Select to Output in Low-Z	3	—	3	—	3	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High-Z	0	5	0	6	0	7	ns
t_{OE}	Output Enable to Output Valid	—	5	—	6	—	7	ns
t_{OLZ}[1]	Output Enable to Output in Low-Z	1	—	1	—	1	—	ns
t_{OHZ}[1]	Output Disable to Output in High-Z	0	5	0	6	0	7	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Down Time	—	10	—	12	—	15	ns
Write Cycle								
t_{WC}	Write Cycle Time	10	—	12	—	15	—	ns
t_{AW}	Address Valid to End of Write	9	—	9	—	10	—	ns
t_{CW}	Chip Select to End of Write	9	—	9	—	10	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	9	—	9	—	10	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to to End of Write	7	—	8	—	8	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	3	—	3	—	3	—	ns
t_{WHZ}[1]	Write Enable to Output in High-Z	0	5	0	6	0	7	ns

NOTE:
1. This parameter guaranteed with the AC load (Figure 2) by device characterization, but is not production tested.

2896 tbl 08

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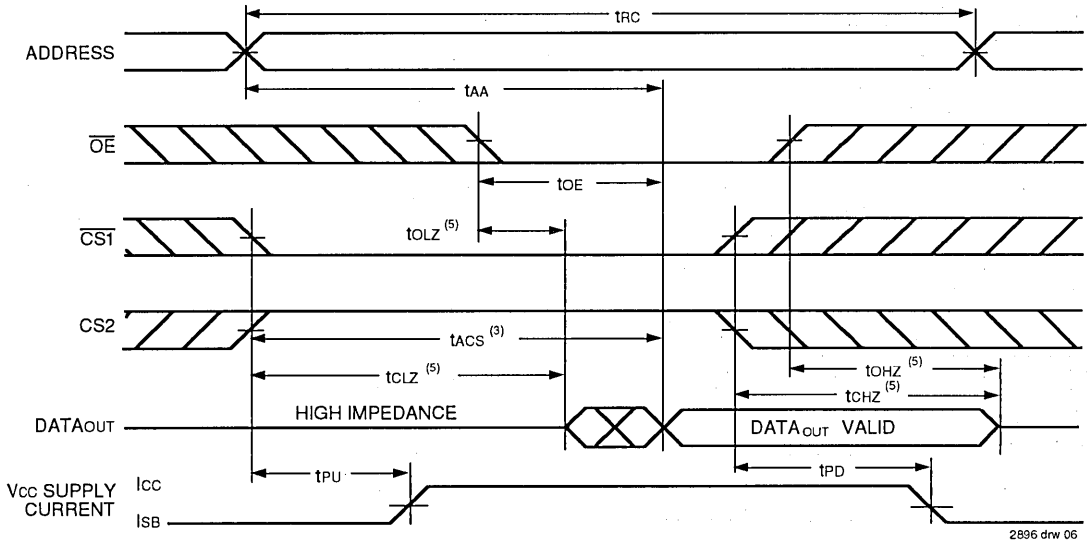
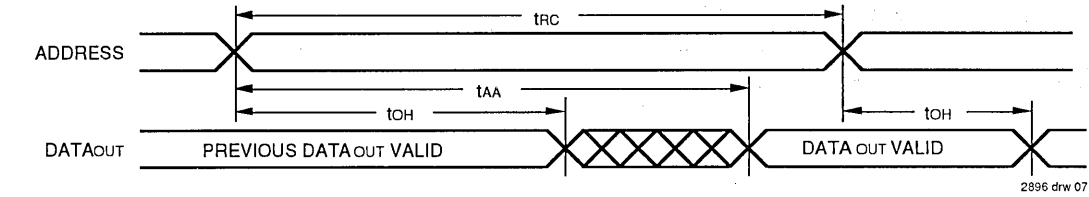
TIMING WAVEFORM OF READ CYCLE NO. 1(1)

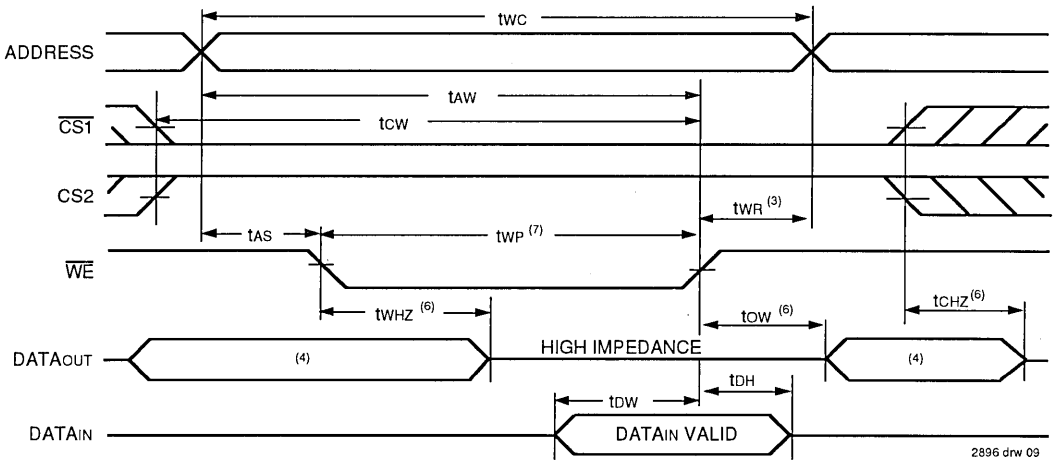


TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)

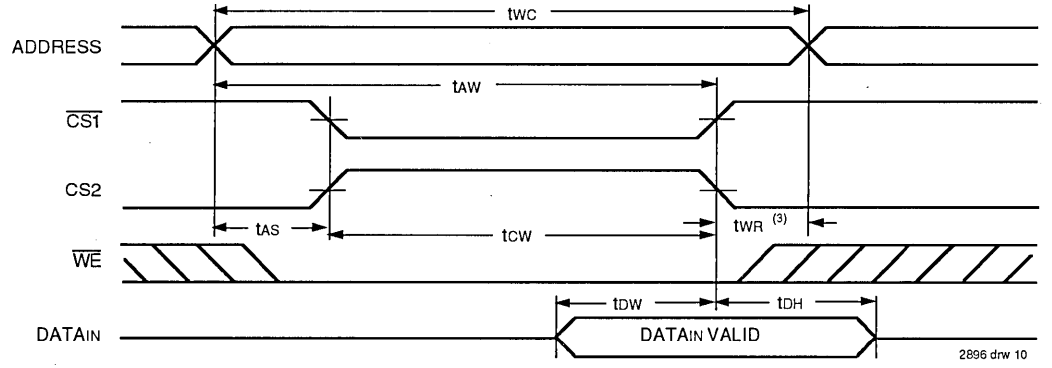


NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS1}$ is LOW, CS2 is HIGH.
3. Address must be valid prior to or coincident with the later of $\overline{CS1}$ transition LOW and CS2 transition HIGH; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 5, 7)

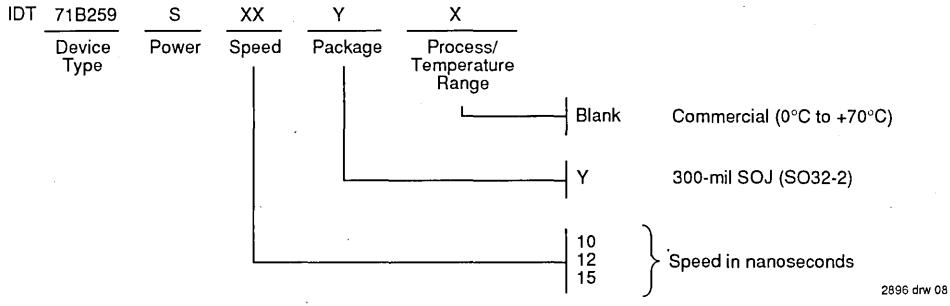


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS1}$ AND CS2 CONTROLLED TIMING)(1, 2, 5)



NOTES:
1. $\overline{WE}$ must be HIGH, $\overline{CS1}$ must be HIGH, or CS2 must be LOW during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS1}$, HIGH CS2, and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS1}$ or $\overline{WE}$ going HIGH or CS2 going LOW to the end of the write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS1}$ LOW transition or the CS2 HIGH transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high impedance state. $\overline{CS1}$ and CS2 must both be active during the tCW period.
6. Transition is measured ±200mV from steady state.
7. $\overline{OE}$ is continuosly HIGH. During a $\overline{WE}$ controlled write cycle with $\overline{OE}$ LOW, tWP must be greater than or equal to tWHZ + tDW to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified tWP.

ORDERING INFORMATION



1M SRAM PRODUCTS

The 1M family consists of both fast CMOS and very fast BiCMOS devices. The latter include revolutionary pinout versions (center power and ground) for the ultimate in speed while maintaining system noise control.

Speeds as fast as 15ns are available in the CMOS commercial versions, with 20ns available in military offerings, and low power versions available. The x8 version of these products is especially well suited for the next generation size of caches in high-end PC applications.

The BiCMOS 1M family is offered both in evolutionary and revolutionary pinout, with the latter available in speeds as fast as 10ns. These SRAMs are ideally suited for workstation cache applications and communications high-speed data buffering.

Size	Org.	Features	Process	Part Number	Power	Speeds	
						Commercial	Military
1M	256K x 4		CMOS	71028	S/L	15,17	20,25
	256K x 4		BiCMOS	71B028	S	15,17	N/A
	256K x 4	Center Pwr	BiCMOS	71B128	S	10,12,15	N/A
	128K x 8		CMOS	71024	S/L	15,17	20,25
	128K x 8		BiCMOS	71B024	S	15,17	N/A
	128K x 8	Center Pwr	BiCMOS	71B124	S	10,12,15	N/A

TABLE OF CONTENTS

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Integrated Device Technology, Inc.

CMOS STATIC RAM 1 MEG (256K x 4-BIT)

ADVANCE INFORMATION IDT71028

FEATURES:

- 256K x 4 advanced high-speed CMOS static RAM
- Equal access and cycle times
  - — Military: 20/25ns
  - — Commercial: 15/17ns
- One Chip Select plus one Output Enable pin
- Bidirectional data Inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Available in 28-pin Ceramic DIP, Plastic DIP, and Plastic SOJ packages
- Military product compliant to MIL-STD-883, Class B

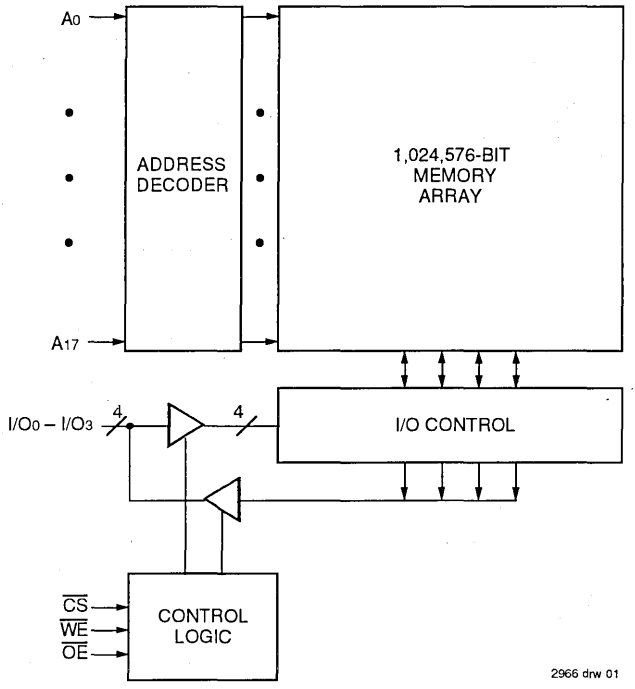
DESCRIPTION:

The IDT71028 is a 1,024,576-bit high-speed static RAM organized as 256K x 4. It is fabricated using IDT's high-perfomance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

The IDT71028 has an output enable pin which operates as fast as 6ns, with address access times as fast as 15ns. All bidirectional inputs and outputs of the IDT71028 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

The IDT71028 is packaged in 28-pin 400-mil Ceramic DIP, 28-pin 400 mil Plastic DIP, and 28-pin 400-mil Plastic SOJ packages.

FUNCTIONAL BLOCK DIAGRAM



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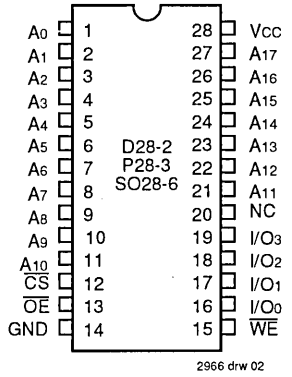
The IDT Logo is a registered trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



DIP/SOJ
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.25	1.25	W
I_{OUT}	DC Output Current	50	50	mA

NOTES: 2966 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 0.5V.

TRUTH TABLE(1,2)

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
L	L	H	$DATA_{OUT}$	Read Data
L	X	L	$DATA_{IN}$	Write Data
L	H	H	High-Z	Output Disabled
H	X	X	High-Z	Deselected - Standby (I_{SB})
V_{HC}(3)	X	X	High-Z	Deselected - Standby (I_{SB1})

NOTES: 2966 tbl 01

1. H = V_{IH}, L = V_{IL}, x = Don't care.
2. V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V.
3. Other inputs ≥V_{HC} or ≤V_{LC}.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	8	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	8	pF

NOTE: 2966 tbl 03

1. This parameter is guaranteed by device characterization, but not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	V_{CC}+0.5	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2966 tbl 04

1. V_{IL} (min.) = –1.5V for pulse width less than 10ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71028 Min.	IDT71028 Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

2966 tbl 05

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

Symbol	Parameter	71028S15		71028S17		71028S20		71028S25		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Dynamic Operating Current, $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	150	—	145	—	—	155	—	140	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	35	—	35	—	—	40	—	35	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, Outputs Open, V_{CC} = Max., f = 0[2], $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$	15	—	15	—	—	20	—	20	mA

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.

2966 tbl 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2966 tbl 07

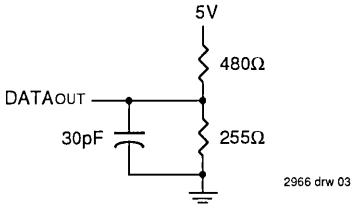
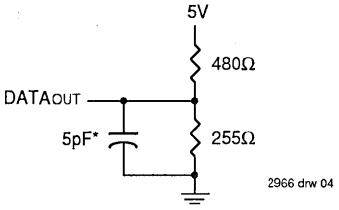


Figure 1. AC Test Load



*Including jig and scope capacitance.

Figure 2. AC Test Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})

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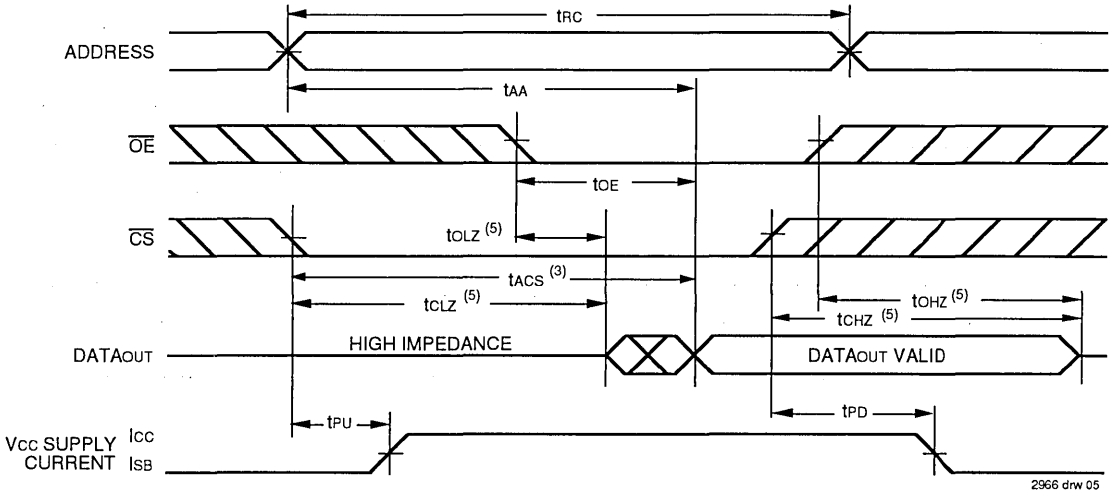
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71028S15[1]		71028S17		71028S20[2]		71028S25[2]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	15	—	17	—	20	—	25	—	ns
t_{AA}	Address Access Time	—	15	—	17	—	20	—	25	ns
t_{ACS}	Chip Select Access Time	—	15	—	17	—	20	—	25	ns
t_{CLZ}[3]	Chip Select to Output in Low-Z	3	—	3	—	3	—	3	—	ns
t_{CHZ}[3]	Chip Deselect to Output in High-Z	0	7	0	8	0	8	0	10	ns
t_{OE}	Output Enable to Output Valid	—	7	—	8	—	8	—	10	ns
t_{OLZ}[3]	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	ns
t_{OHZ}[3]	Output Disable to Output in High-Z	0	5	0	6	0	7	0	10	ns
t_{OH}	Output Hold from Address Change	4	—	4	—	4	—	4	—	ns
t_{PU}[3]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}[3]	Chip Deselect to Power Down Time	—	15	—	17	—	20	—	25	ns
Write Cycle										
t_{WC}	Write Cycle Time	15	—	17	—	20	—	25	—	ns
t_{AW}	Address Valid to End of Write	12	—	13	—	15	—	15	—	ns
t_{CW}	Chip Select to End of Write	12	—	13	—	15	—	15	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	12	—	13	—	15	—	15	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	8	—	9	—	9	—	10	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{OW}[3]	Output Active from End of Write	3	—	3	—	4	—	4	—	ns
t_{WHZ}[3]	Write Enable to Output in High-Z	0	5	0	7	0	8	0	9	ns

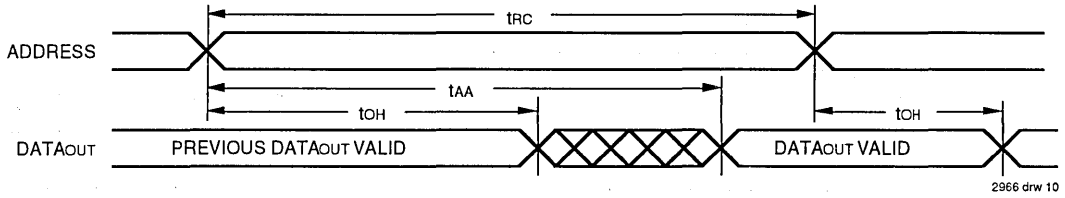
NOTES:
1. 0° to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. This parameter guaranteed with the AC load (Figure 2) by device characterization, but is not production tested.

2966 tbl 08

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address must be valid prior to or coincident with the later of $\overline{CS}$ transition LOW; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

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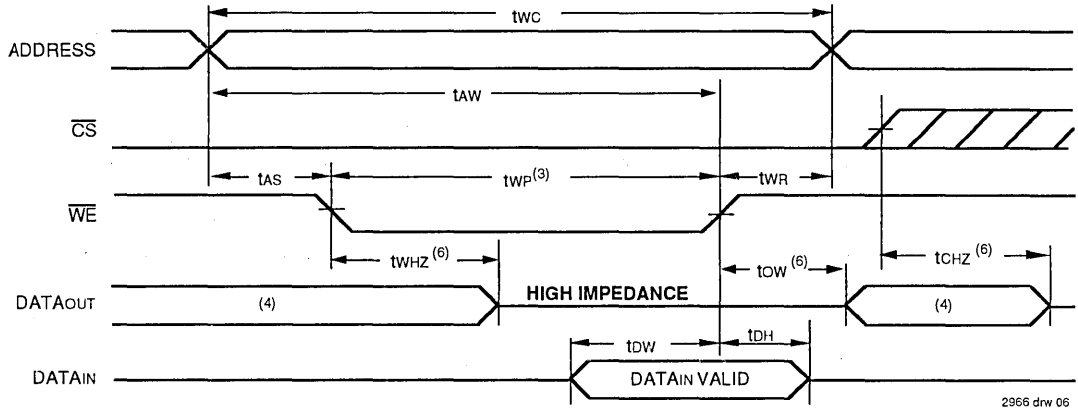
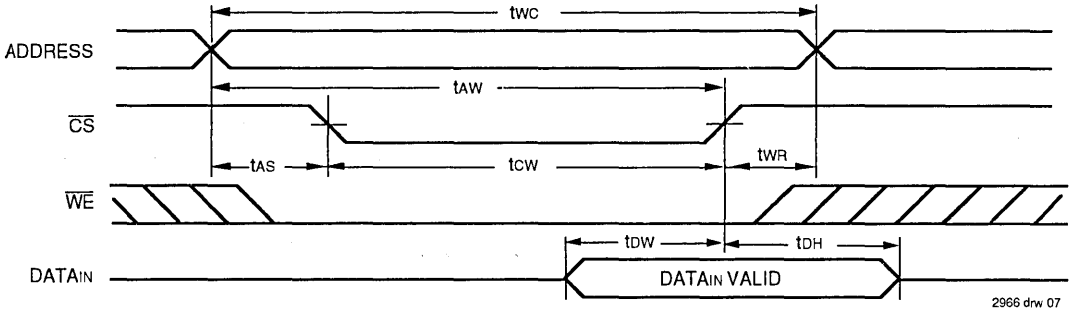
TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ CONTROLLED TIMING)(1,2,3,5)

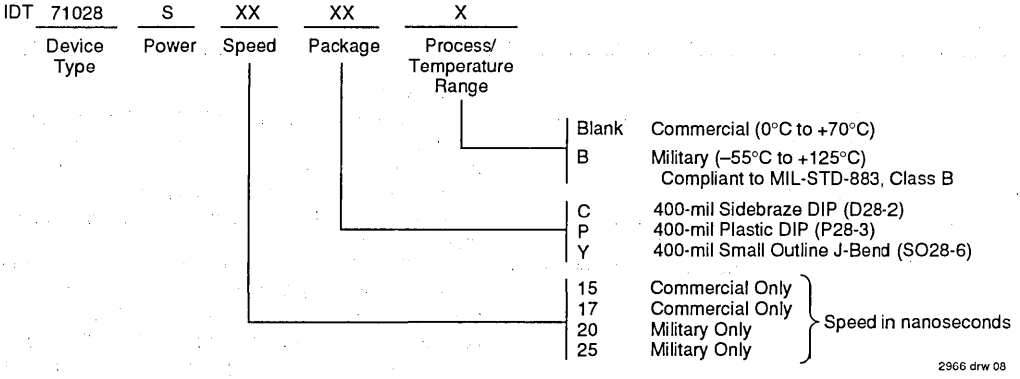


TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ CONTROLLED TIMING)(1,2,5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP}.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state.

ORDERING INFORMATION



8

Integrated Device Technology, Inc.

BiCMOS STATIC RAM 1 MEG (256K x 4-BIT)

PRELIMINARY
IDT71B028

FEATURES:

- 256K x 4 advanced high-speed BiCMOS static RAM
- Equal access and cycle times
  - — Commercial: 15/17ns
- One Chip Select plus one Output Enable pin
- Bidirectional data Inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Available in 28-pin Plastic DIP and Plastic SOJ packages

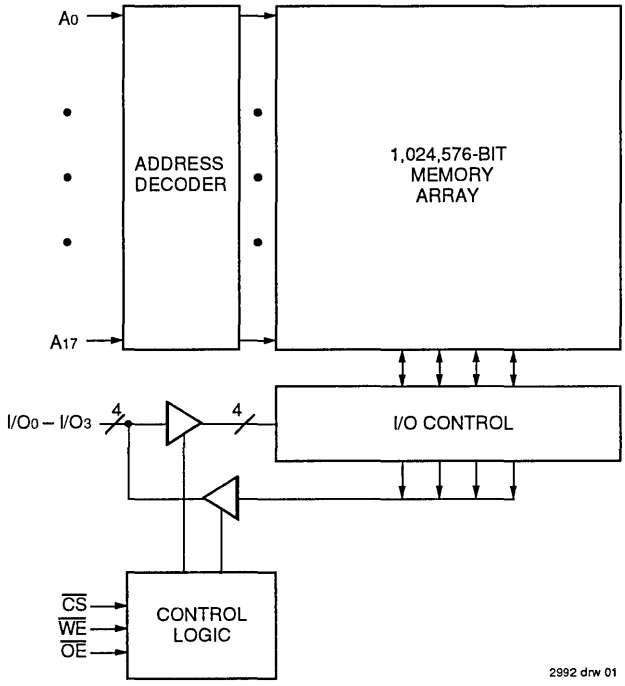
DESCRIPTION:

The IDT71B028 is a 1,024,576-bit high-speed static RAM organized as 256K x 4. It is fabricated using IDT's high-perfomance, high-reliability BiCMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

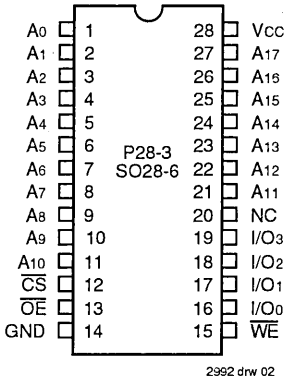
The IDT71B028 has an output enable pin which operates as fast as 6ns, with address access times as fast as 15ns. All bidirectional inputs and outputs of the IDT71B028 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

The IDT71B028 is packaged in 28-pin 400 mil Plastic DIP and 28-pin 400-mil Plastic SOJ packages.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



DIP/SOJ
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTES: 2992 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 0.5V.

TRUTH TABLE(1,2)

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
L	L	H	$DATA_{OUT}$	Read Data
L	X	L	$DATA_{IN}$	Write Data
L	H	H	High-Z	Outputs Disabled
H	X	X	High-Z	Deselected - Standby (I_{SB})
V_{HC}(3)	X	X	High-Z	Deselected - Standby (I_{SB1})

NOTES: 2992 tbl 01

1. H = V_{IH}, L = V_{IL}, x = Don't care.
2. V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V.
3. Other inputs ≥V_{HC} or ≤V_{LC}.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	6	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

NOTE: 2992 tbl 03

1. This parameter is guaranteed by device characterization, but not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	V_{CC}+0.5	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2992 tbl 04

1. V_{IL} (min.) = –1.5V for pulse width less than 10ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71B028 Min.	IDT71B028 Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

2992 tbl 05

8

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

Symbol	Parameter	71B028S15		71B028S17		Unit
		Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Dynamic Operating Current, CS2 ≥ V_{IH} and $\overline{CS1}$ ≤ V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	190	—	180	—	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS1}$ ≥ V_{IH} or CS2 ≤ V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	55	—	50	—	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS1}$ ≥ V_{HC} or CS2 ≤ V_{LC} Outputs Open, V_{CC} = Max., f = 0(2), V_{IN} ≤ V_{LC} or V_{IN} ≥ V_{HC}	40	—	40	—	mA

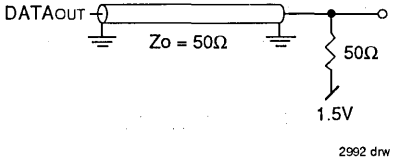
2992 tbl 06

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.

AC TEST CONDITIONS

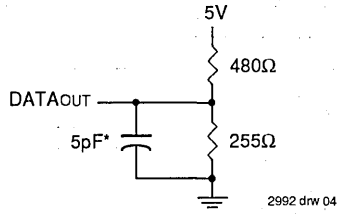
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1, 2, and 3

2992 tbl 07



2992 drw 03

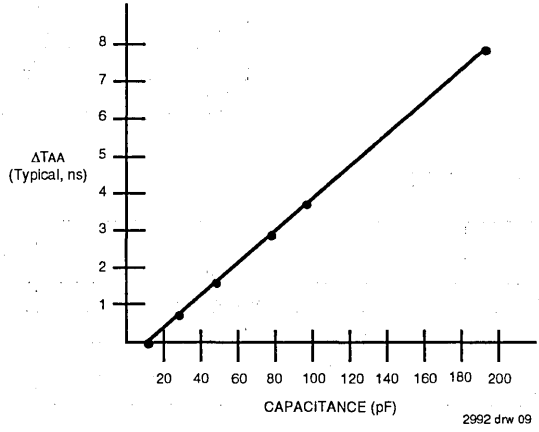
Figure 1. AC Test Load



2992 drw 04

*Including jig and scope capacitance.

Figure 2. AC Test Load (for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})



2992 drw 09

Figure 3. Lumped Capacitive Load, typical Derating

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%)

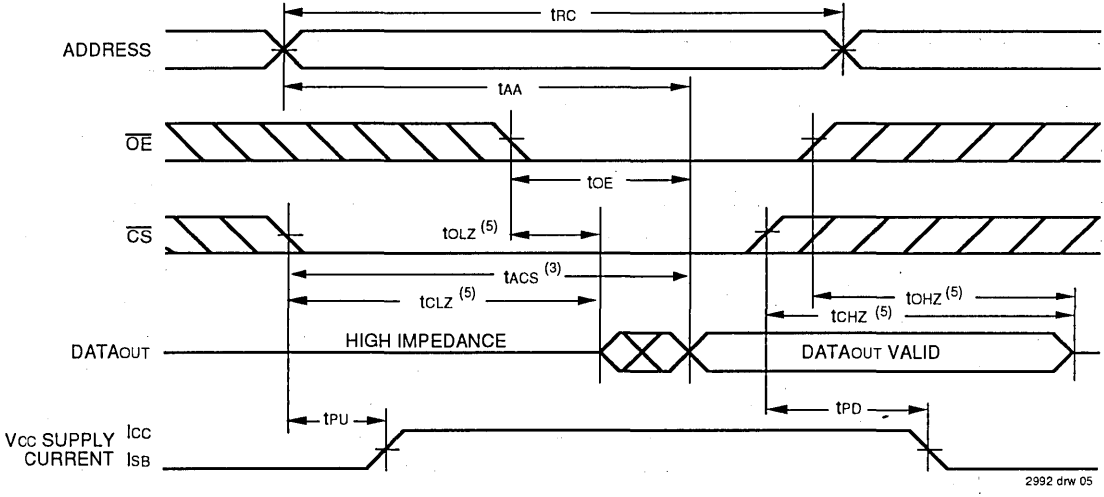
Symbol	Parameter	71B028S15		71B028S17		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	15	—	17	—	ns
t_{AA}	Address Access Time	—	15	—	17	ns
t_{ACS}	Chip Select Access Time	—	15	—	17	ns
t_{CLZ}(1)	Chip Select to Output in Low-Z	3	—	3	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High-Z	0	8	0	8	ns
t_{OE}	Output Enable to Output Valid	—	8	—	9	ns
t_{OLZ}(1)	Output Enable to Output in Low-Z	0	—	0	—	ns
t_{OHZ}(1)	Output Disable to Output in High-Z	0	7	0	7	ns
t_{OH}	Output Hold from Address Change	4	—	4	—	ns
t_{PU}(1)	Chip Select to Power Up Time	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power Down Time	—	15	—	17	ns
Write Cycle						
t_{WC}	Write Cycle Time	15	—	17	—	ns
t_{AW}	Address Valid to End of Write	12	—	12	—	ns
t_{CW}	Chip Select to End of Write	12	—	12	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	ns
t_{WP}	Write Pulse Width	12	—	12	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	8	—	9	—	ns
t_{DH}	Data Hold Time	0	—	0	—	ns
t_{OW}(1)	Output Active from End of Write	3	—	3	—	ns
t_{WHZ}(1)	Write Enable to Output in High-Z	0	8	0	8	ns

NOTE:
1. This parameter guaranteed with the AC load (Figure 2) by device characterization, but is not production tested.

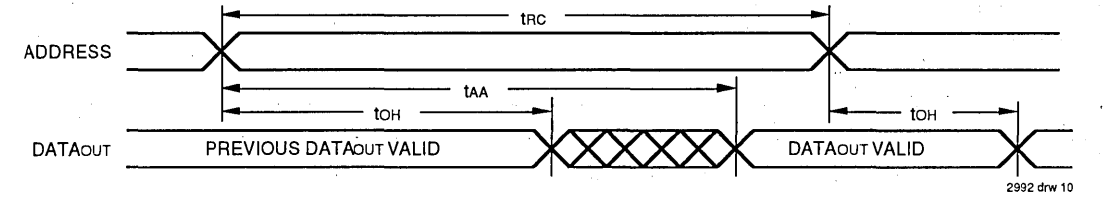
2992 tbl 08

8

TIMING WAVEFORM OF READ CYCLE NO. 1(1)

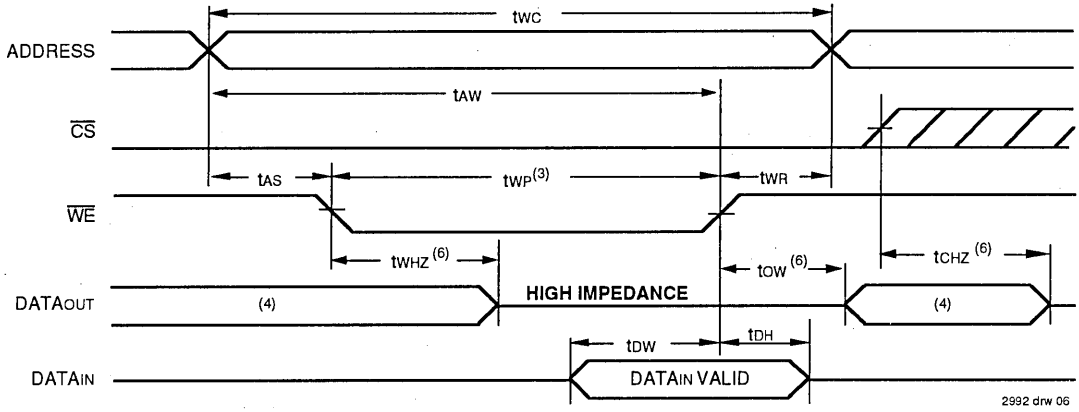


TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)

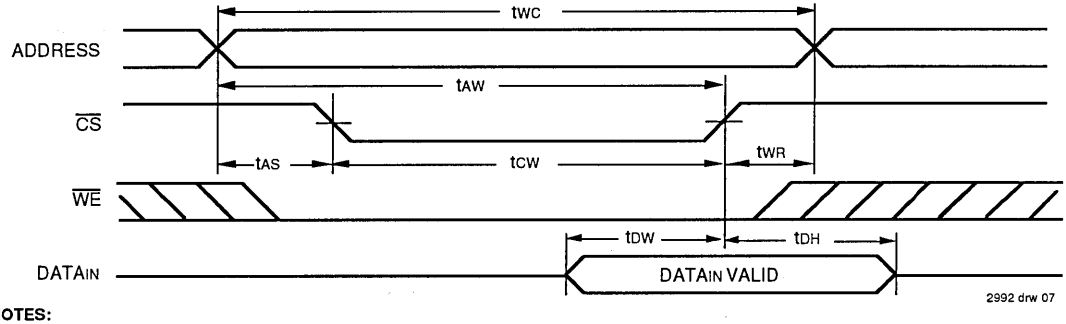


NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address must be valid prior to or coincident with the later of $\overline{CS}$ transition LOW; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ CONTROLLED TIMING)(1,2,3,5)

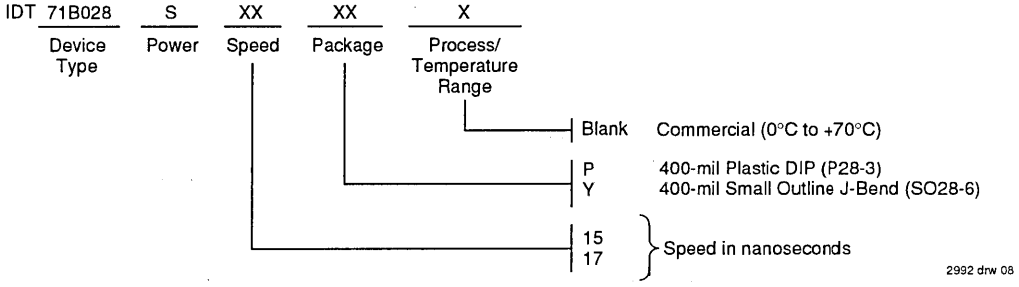


TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ CONTROLLED TIMING)(1,2,5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a low $\overline{WE}$.
3. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified t_{WP}.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state.

ORDERING INFORMATION



Integrated Device Technology, Inc.

BiCMOS STATIC RAM 1 MEG (256K x 4-BIT) REVOLUTIONARY PINOUT

ADVANCE INFORMATION
IDT71B128

FEATURES:

- 256K x 4 advanced high-speed BiCMOS static RAM
- JEDEC revolutionary pinout (center power/GND) for reduced noise
- Equal access and cycle times
  — Commercial: 10/12/15ns
- One Chip Select plus one Output Enable pin
- Bidirectional data Inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Available in JEDEC 32-pin Plastic DIP and Plastic SOJ packages

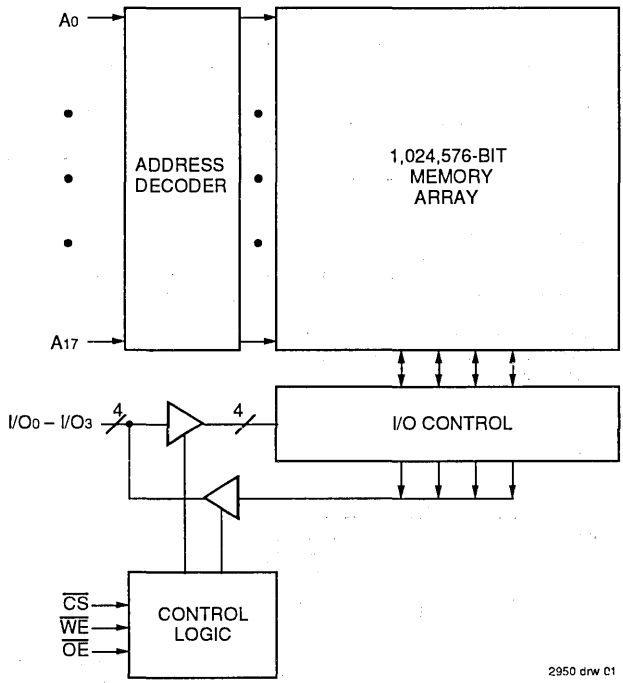
DESCRIPTION:

The IDT71B128 is a 1,024,576-bit high-speed static RAM organized as 256K x 4. It is fabricated using IDT's high-perfomance, high-reliability BiCMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs. The JEDEC center pin power/GND pinout reduces noise generation and improves high speed system performance.

The IDT71B128 has an output enable pin which operates as fast as 5ns, with address access times as fast as 10ns. All bidirectional inputs and outputs of the IDT71B128 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

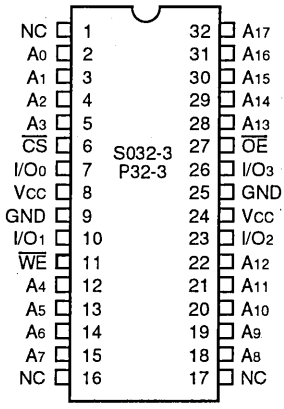
The IDT71B128 is packaged in 28-pin 400 mil Plastic DIP and 28-pin 400-mil Plastic SOJ packages.

FUNCTIONAL BLOCK DIAGRAM



The IDT Logo is a registered trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



2950 drw 02

DIP/SOJ
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTES: 2950 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 0.5V.

TRUTH TABLE(1,2)

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
L	L	H	$DATA_{OUT}$	Read Data
L	X	L	$DATA_{IN}$	Write Data
L	H	H	High-Z	Outputs Disabled
H	X	X	High-Z	Deselected - Standby (I_{SB})
V_{HC}(3)	X	X	High-Z	Deselected - Standby (I_{SB1})

NOTES: 2950 tbl 01

1. H = V_{IH}, L = V_{IL}, x = Don't care.
2. V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V.
3. Other inputs ≥V_{HC} or ≤V_{LC}.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	8	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	8	pF

NOTE: 2950 tbl 03

1. This parameter is guaranteed by device characterization, but not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	V_{CC}+0.5	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2950 tbl 04

1. V_{IL} (min.) = –1.5V for pulse width less than 10ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71B128 Min.	IDT71B128 Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

2950 tbl 05

8

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

Symbol	Parameter	71B128S10		71B128S12		71B128S15		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Dynamic Operating Current, $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	165	—	155	—	150	—	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \ge V_{IH}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	35	—	30	—	30	—	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \ge V_{HC}$, Outputs Open, V_{CC} = Max., f = 0[2], $V_{IN} \le V_{LC}$ or $V_{IN} \ge V_{HC}$	12	—	12	—	12	—	mA

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.

2950 tbl 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1, 2, and 3

2950 tbl 07

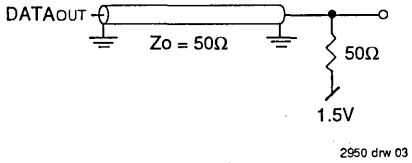
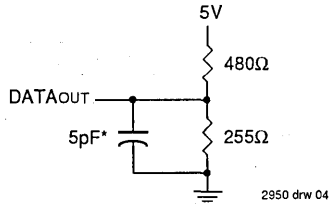


Figure 1. AC Test Load



*Including jig and scope capacitance.

Figure 2. AC Test Load (for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})

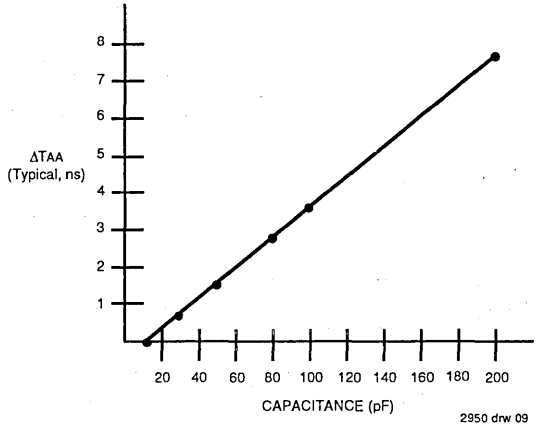


Figure 3. Lumped Capacitive Load, typical Derating

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%)

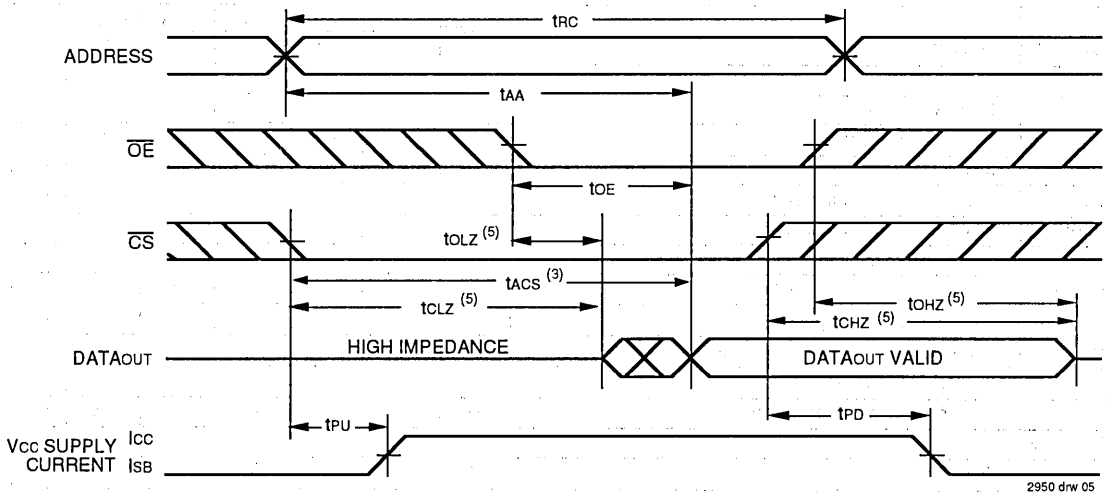
Symbol	Parameter	71B128S10		71B128S12		71B128S15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	10	—	12	—	15	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	ns
t_{ACS}	Chip Select Access Time	—	10	—	12	—	15	ns
t_{CLZ}[1]	Chip Select to Output in Low-Z	2	—	3	—	3	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High-Z	0	5	0	6	0	7	ns
t_{OE}	Output Enable to Output Valid	—	5	—	6	—	7	ns
t_{OLZ}[1]	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
t_{OHZ}[1]	Output Disable to Output in High-Z	0	5	0	6	0	7	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Down Time	—	10	—	12	—	15	ns
Write Cycle								
t_{WC}	Write Cycle Time	10	—	12	—	15	—	ns
t_{AW}	Address Valid to End of Write	8	—	9	—	10	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	8	—	9	—	10	—	ns
t_{CW}	Chip Select to End of Write	8	—	9	—	10	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	6	—	7	—	8	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	3	—	3	—	3	—	ns
t_{WHZ}[1]	Write Enable to Output in High-Z	0	5	0	6	0	7	ns

NOTE:
1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

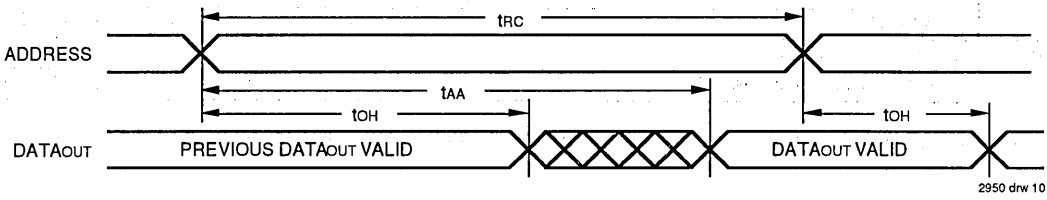
2950 tbl 08

8

TIMING WAVEFORM OF READ CYCLE NO. 1(1)

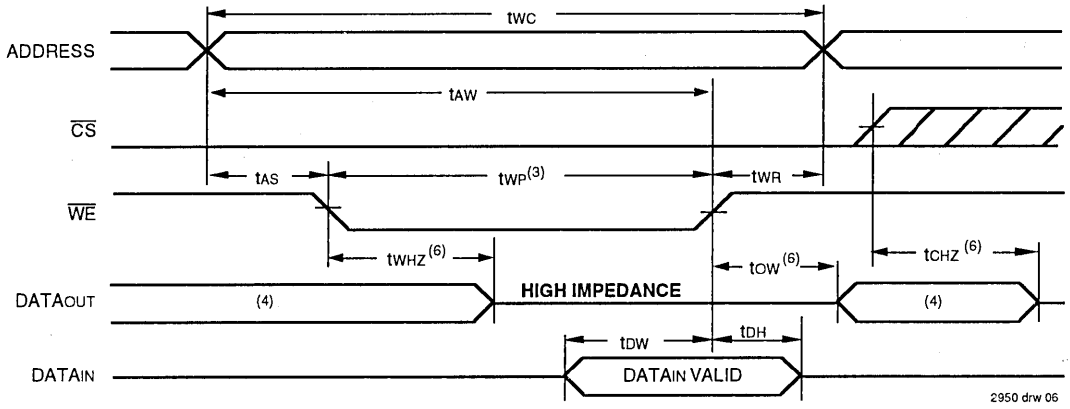


TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)

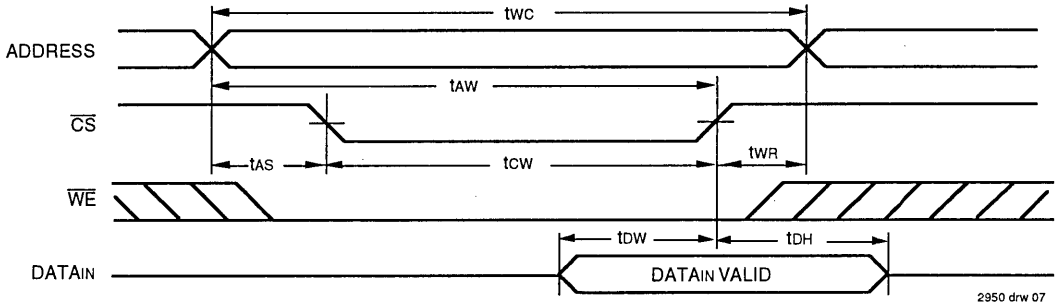


NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address must be valid prior to or coincident with the later of $\overline{CS}$ transition LOW; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ CONTROLLED TIMING)(1,2,3,5)



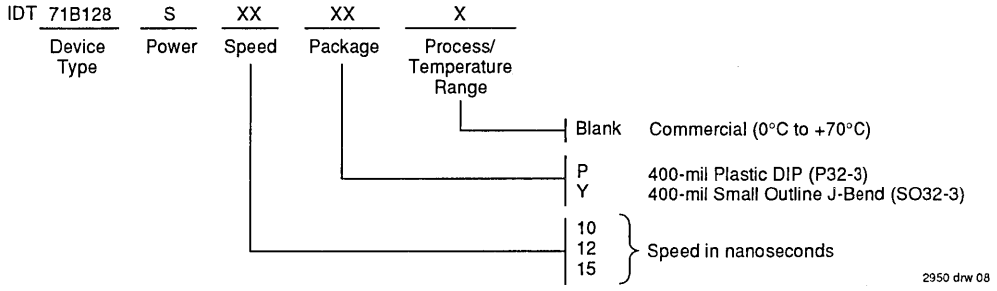
TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ CONTROLLED TIMING)(1,2,5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified t_{WP}.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state.

8

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS STATIC RAM 1 MEG (128K x 8-BIT)

ADVANCE INFORMATION
IDT71024

FEATURES:

- 128K x 8 advanced high-speed CMOS static RAM
- Equal access and cycle times
  - — Military: 20/25ns
  - — Commercial: 15/17ns
- Two Chip Selects plus one Output Enable pin
- Bidirectional inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Available in 32-pin Ceramic DIP, Plastic DIP, Plastic SOJ, and LCC packages
- Military product compliant to MIL-STD-883, Class B

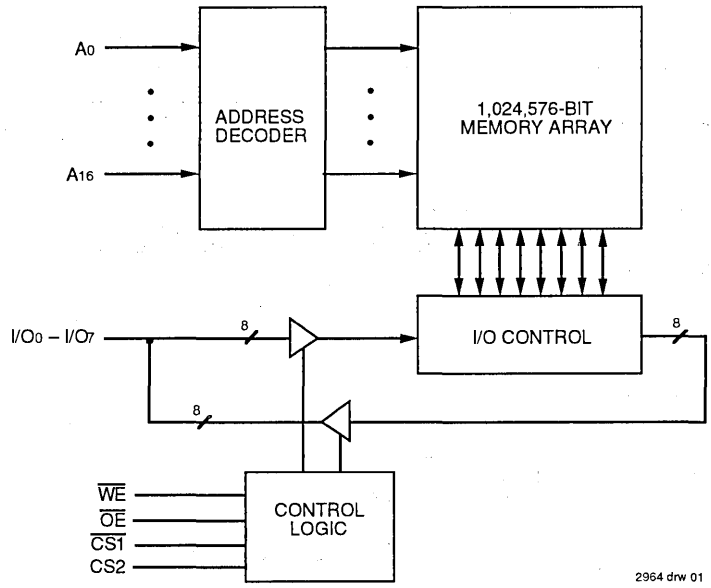
DESCRIPTION:

The IDT71024 is a 1,024,576-bit high-speed static RAM organized as 128K x 8. It is fabricated using IDT's high-perfomance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

The IDT71024 has an output enable pin which operates as fast as 7ns, with address access times as fast as 15ns available. All bidirectional inputs and outputs of the IDT71024 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used; no clocks or refresh are required for operation.

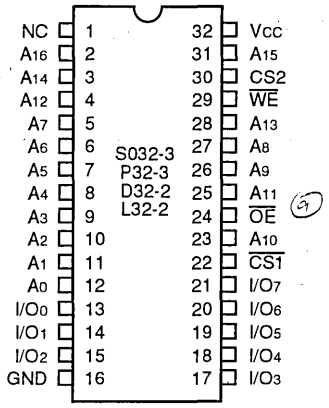
The IDT71024 is packaged in 32-pin 400 mil Ceramic DIP, 32-pin 400 mil Plastic DIP, 32-pin 400 mil Plastic SOJ, and 32-pin 400 x 820 mil LCC packages.

FUNCTIONAL BLOCK DIAGRAM



The IDT Logo is a registered trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



2964 drw 02

DIP/SOJ/LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.25	1.25	W
I_{OUT}	DC Output Current	50	50	mA

NOTES: 2964 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 0.5V.

TRUTH TABLE(1,2)

INPUTS					
$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	I/O	FUNCTION
X	H	X	X	High-Z	Deselected–Standby (I_{SB})
X	V_{HC}(3)	X	X	High-Z	Deselected–Standby (I_{SB1})
X	X	L	X	High-Z	Deselected–Standby (I_{SB})
X	X	V_{LC}(3)	X	High-Z	Deselected–Standby (I_{SB1})
H	L	H	H	High-Z	Outputs Disabled
H	L	H	L	DATAOUT	Read Data
L	L	H	X	DATAIN	Write Data

NOTES: 2964 tbl 01

1. H = V_{IH}, L = V_{IL}, X = Don't care.
2. V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V.
3. Other inputs ≥V_{HC} or ≤V_{LC}.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	8	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	8	pF

NOTE: 2964 tbl 03

1. This parameter is guaranteed by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	Vcc+0.5	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2964 tbl 04

1. V_{IL} (min.) = –1.5V for pulse width less than 10ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71024 Min.	IDT71024 Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS1}$ = V_{IH}, CS2 = V_{IL}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

2964 tbl 05

8

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

Symbol	Parameter	71024S15		71024S17		71024S20		71024S25		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Dynamic Operating Current, CS2 ≥ V_{IH} and $\overline{CS1} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	155	—	150	—	—	160	—	145	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS1} \geq V_{IH}$ or CS2 ≤ V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	35	—	35	—	—	40	—	35	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS1} \geq V_{HC}$ or CS2 ≤ V_{LC} Outputs Open, V_{CC} = Max., f = 0[2], $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$	15	—	15	—	—	20	—	20	mA

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.

2964 tbl 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2964 tbl 07

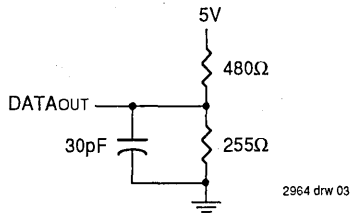
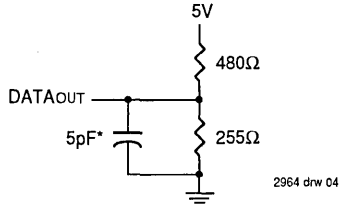


Figure 1. AC Test Load



*Including jig and scope capacitance.

Figure 2. AC Test Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

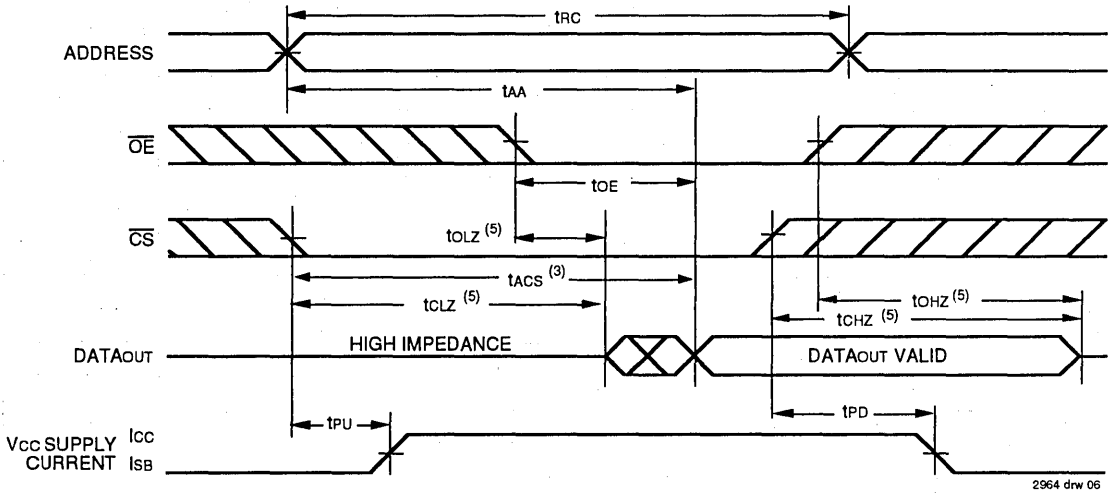
Symbol	Parameter	71024S15[1]		71024S17		71024S20[2]		71024S25[2]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	15	—	17	—	20	—	25	—	ns
t_{AA}	Address Access Time	—	15	—	17	—	20	—	25	ns
t_{ACS}	Chip Select Access Time	—	15	—	17	—	20	—	25	ns
t_{CLZ}[3]	Chip Select to Output in Low-Z	3	—	3	—	3	—	3	—	ns
t_{CHZ}[3]	Chip Deselect to Output in High-Z	0	7	0	8	0	8	0	10	ns
t_{OE}	Output Enable to Output Valid	—	7	—	8	—	8	—	10	ns
t_{OLZ}[3]	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	ns
t_{OHZ}[3]	Output Disable to Output in High-Z	0	5	0	6	0	7	0	10	ns
t_{OH}	Output Hold from Address Change	4	—	4	—	4	—	4	—	ns
t_{PU}[3]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}[3]	Chip Deselect to Power Down Time	—	15	—	17	—	20	—	25	ns
Write Cycle										
t_{WC}	Write Cycle Time	15	—	17	—	20	—	25	—	ns
t_{AW}	Address Valid to End of Write	12	—	13	—	15	—	15	—	ns
t_{CW}	Chip Select to End of Write	12	—	13	—	15	—	15	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	12	—	13	—	15	—	15	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	8	—	9	—	9	—	10	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{OW}[3]	Output Active from End of Write	3	—	3	—	4	—	4	—	ns
t_{WHZ}[3]	Write Enable to Output in High-Z	0	5	0	7	0	8	0	9	ns

NOTES:
1. 0° to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. This parameter guaranteed with the AC load (Figure 2) by device characterization, but is not production tested.

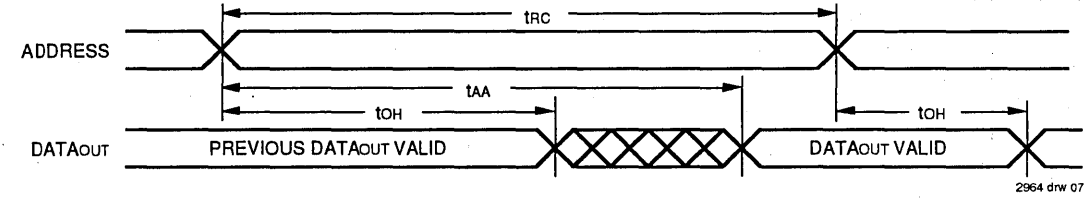
2964 tbl 08

8

TIMING WAVEFORM OF READ CYCLE NO. 1(1)

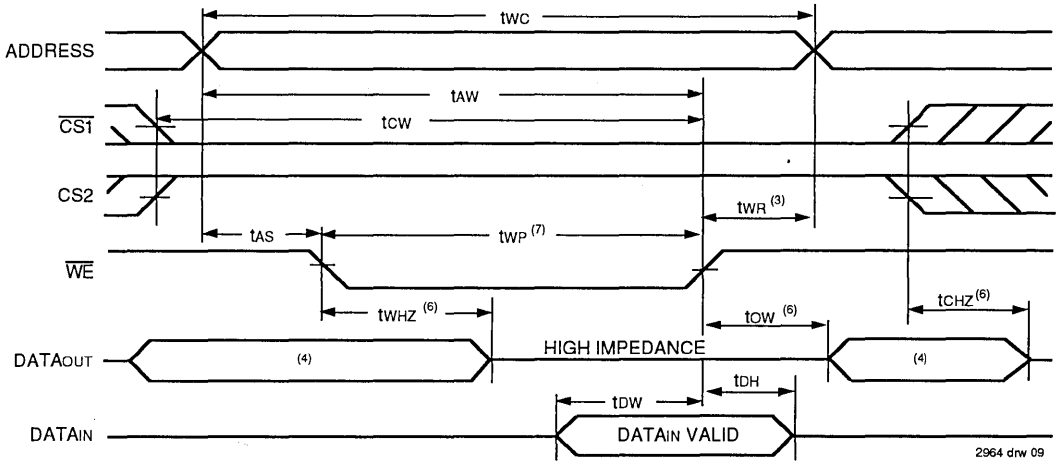


TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)

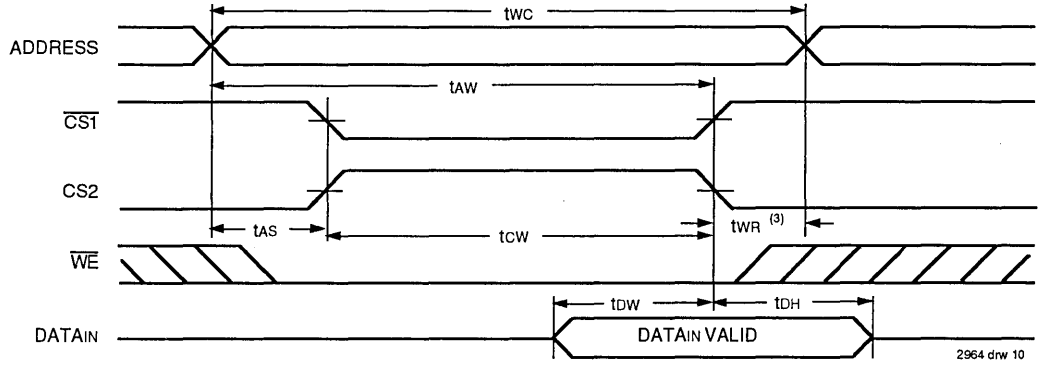


NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS1}$ is LOW, CS2 is HIGH.
3. Address must be valid prior to or coincident with the later of $\overline{CS1}$ transition LOW and CS2 transition HIGH; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 5, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS1}$ AND CS2 CONTROLLED TIMING)(1, 2, 5)



NOTES:
1. $\overline{WE}$ must be HIGH, $\overline{CS1}$ must be HIGH, or CS2 must be LOW during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS1}$, HIGH CS2, and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of either $\overline{CS1}$ or $\overline{WE}$ going HIGH or CS2 going LOW to the end of the write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS1}$ LOW transition or the CS2 HIGH transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high impedance state. $\overline{CS1}$ and CS2 must both be active during the tCW write period.
6. Transition is measured ±200mV from steady state.
7. $\overline{OE}$ is continuosly HIGH. During a $\overline{WE}$ controlled write cycle with $\overline{OE}$ LOW, tWP must be greater than or equal to tWHZ + tDW to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified tWP.

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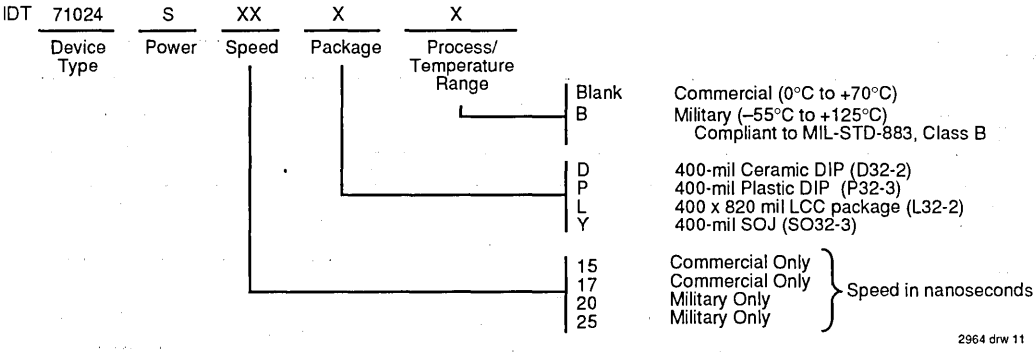
ORDERING INFORMATION



Integrated Device Technology, Inc.

BiCMOS STATIC RAM 1 MEG (128K x 8-BIT)

PRELIMINARY
IDT71B024

FEATURES:

- 128K x 8 Advanced High-Speed BiCMOS Static RAM
- Equal access and cycle times
  - — Commercial: 15/17ns
- Two Chip Selects plus one Output Enable pin
- Bidirectional inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Available in 32-pin Plastic DIP and SOJ packages

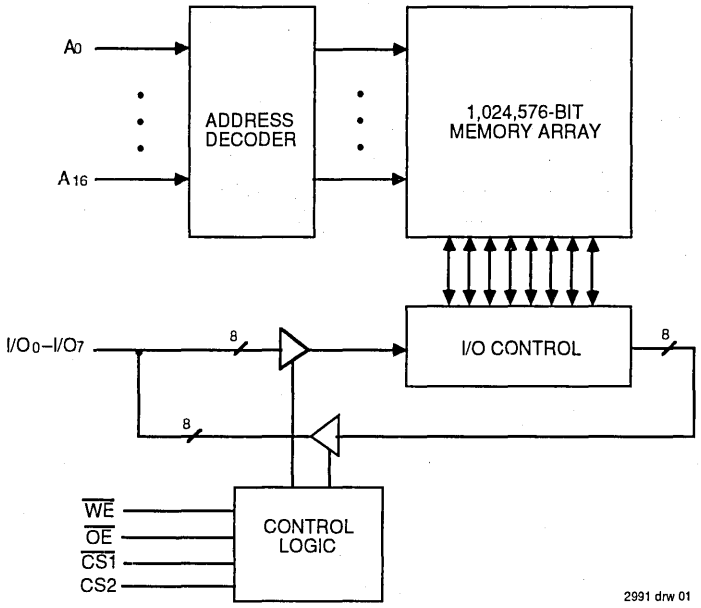
DESCRIPTION:

The IDT71B024 is a 1,024,576-bit high-speed Static RAM organized as 128K x 8. It is fabricated using IDT's high-perfomance, high-reliability BiCMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

The IDT71B024 has an output enable pin which operates as fast as 8ns, with address access times as fast as 15ns available. All bidirectional inputs and outputs of the IDT71B024 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used; no clocks or refresh are required for operation.

The IDT71B024 is packaged in a 32-pin 400 mil Plastic DIP and 32-pin 400 mil Plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



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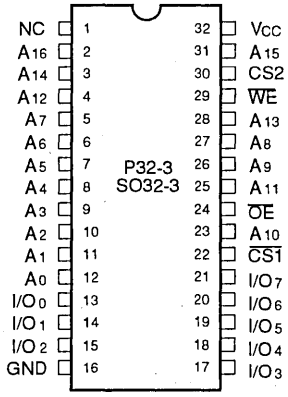
The IDT logo is a registered trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



2991 drw 02

DIP/SOJ
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.25	W
I_{OUT}	DC Output Current	50	mA

2991 tbl 02

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 0.5V.

TRUTH TABLE(1,2)

INPUTS				I/O	FUNCTION
$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$		
X	H	X	X	High-Z	Deselected–Standby (I_{SB})
X	V_{HC}(3)	X	X	High-Z	Deselected–Standby (I_{SB1})
X	X	L	X	High-Z	Deselected–Standby (I_{SB})
X	X	V_{LC}(3)	X	High-Z	Deselected–Standby (I_{SB1})
H	L	H	H	High-Z	Outputs Disabled
H	L	H	L	DATAOUT	Read Data
L	L	H	X	DATAIN	Write Data

2991 tbl 01

NOTES:
1. H = V_{IH}, L = V_{IL}, X = Don't care.
2. V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V.
3. Other inputs ≥V_{HC} or ≤V_{LC}.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	6	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

2991 tbl 03

NOTE:
1. This parameter is guaranteed by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	Vcc+0.5	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

2991 tbl 04

NOTE:
1. V_{IL} (min.) = –1.5V for pulse width less than 10ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71B024 Min.	IDT71B024 Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS1}$ = V_{IH}, CS2 = V_{IL}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

2991 tbl 05

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

Symbol	Parameter	71B024S15 Com'l.	71B024S15 Mil.	71B024S17 Com'l.	71B024S17 Mil.	Unit
I_{CC}	Dynamic Operating Current, CS2 ≥ V_{IH} and $\overline{CS1}$ ≤ V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	200	—	195	—	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS1}$ ≥ V_{IH} or CS2 ≤ V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	55	—	50	—	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS1}$ ≥ V_{HC} or CS2 ≤ V_{LC} Outputs Open, V_{CC} = Max., f = 0[2], V_{IN} ≤ V_{LC} or V_{IN} ≥ V_{HC}	40	—	40	—	mA

2991 tbl 06

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1, 2, & 3

2991 tbl 07

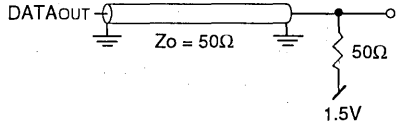
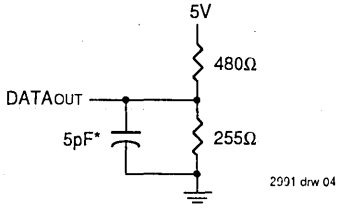


Figure 1. AC Test Load



*Including jig and scope capacitance.

Figure 2. AC Test Load (for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})

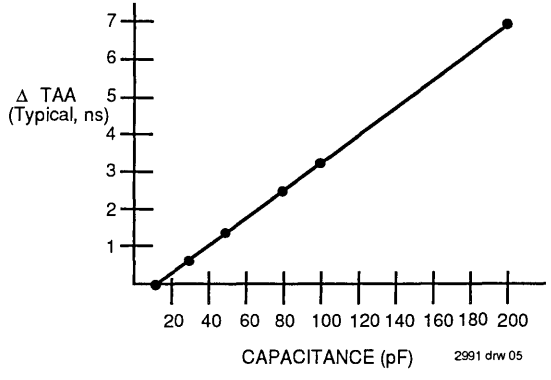


Figure 3. Lumped Capacitive Load, typical Derating

8

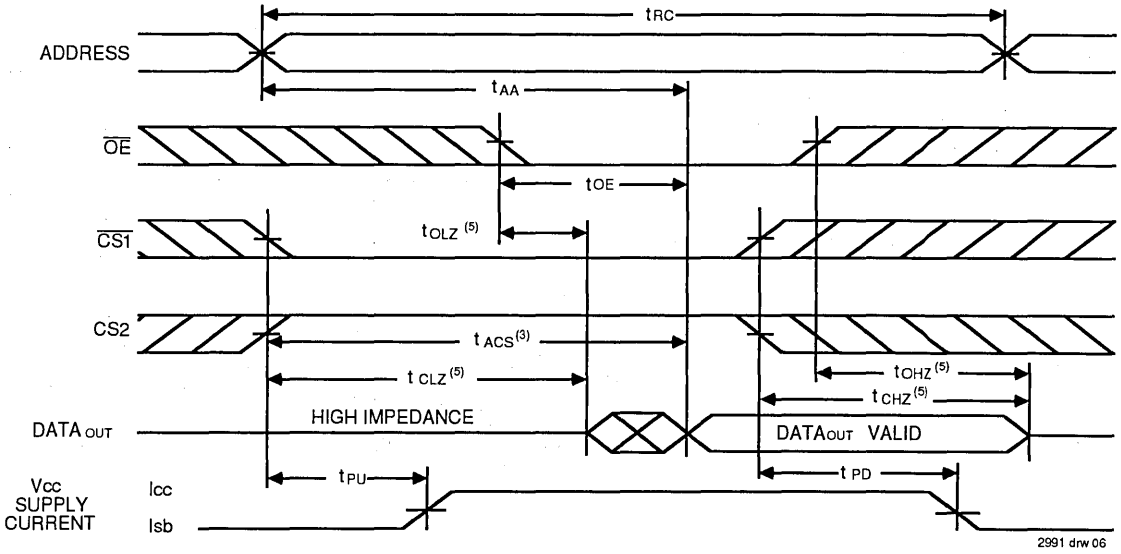
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	71B024S15		71B024S17		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	15	—	17	—	ns
t_{AA}	Address Access Time	—	15	—	17	ns
t_{ACS}	Chip Select Access Time	—	15	—	17	ns
t_{CLZ}(1)	Chip Select to Output in Low-Z	3	—	3	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High-Z	0	8	0	8	ns
t_{OE}	Output Enable to Output Valid	—	8	—	9	ns
t_{OLZ}(1)	Output Enable to Output in Low-Z	0	—	0	—	ns
t_{OHZ}(1)	Output Disable to Output in High-Z	0	7	0	7	ns
t_{OH}	Output Hold from Address Change	4	—	4	—	ns
t_{PU}(1)	Chip Select to Power-Up Time	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power-Down Time	—	15	—	17	ns
Write Cycle						
t_{WC}	Write Cycle Time	15	—	17	—	ns
t_{AW}	Address Valid to End-of-Write	12	—	12	—	ns
t_{CW}	Chip Select to End-of-Write	12	—	12	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	ns
t_{WP}	Write Pulse Width	12	—	12	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	8	—	9	—	ns
t_{DH}	Data Hold Time	0	—	0	—	ns
t_{OW}(1)	Output Active from End-of-Write	3	—	3	—	ns
t_{WHZ}(1)	Write Enable to Output in High-Z	0	8	0	8	ns

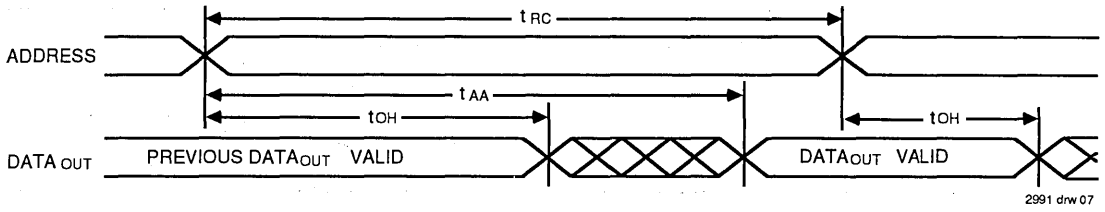
2931 tbl 08

NOTE:
1. This parameter guaranteed with the AC load (Figure 2) by device characterization, but is not production tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



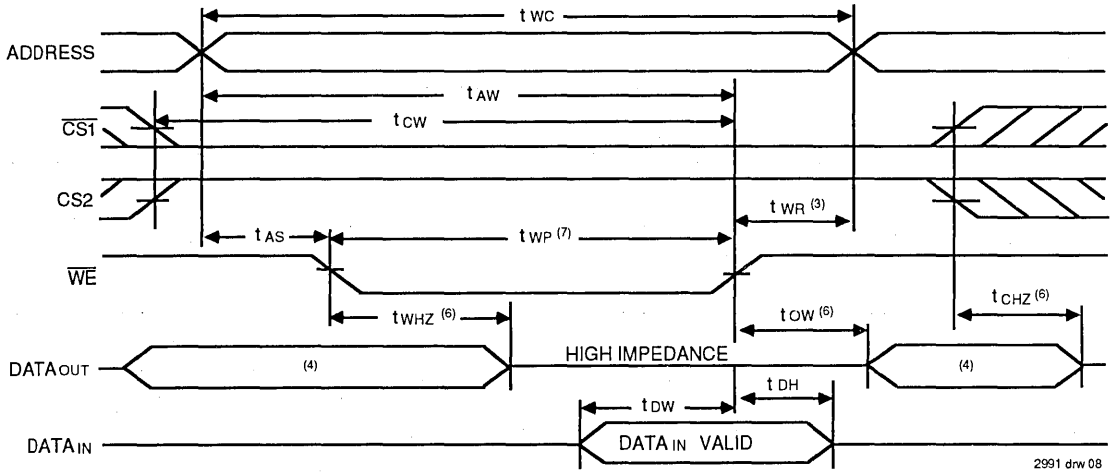
TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



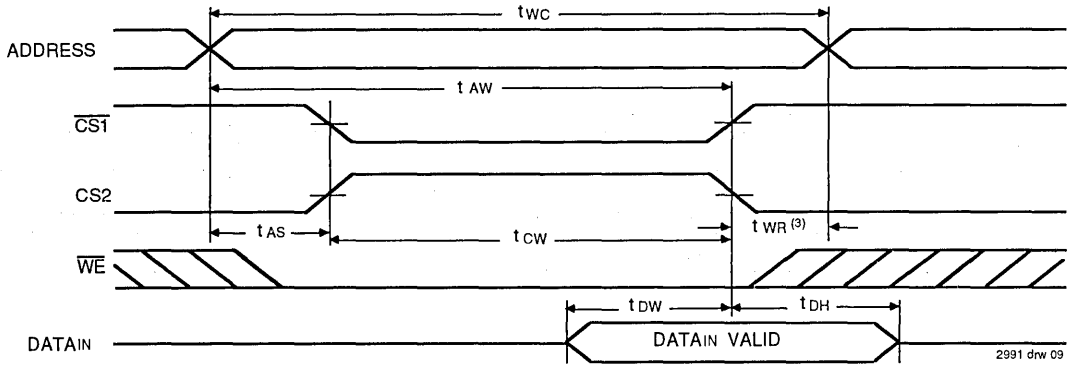
8

NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS1}$ is LOW, CS2 is HIGH.
3. Address must be valid prior to or coincident with the later of $\overline{CS1}$ transition LOW and CS2 transition HIGH; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 5, 7)

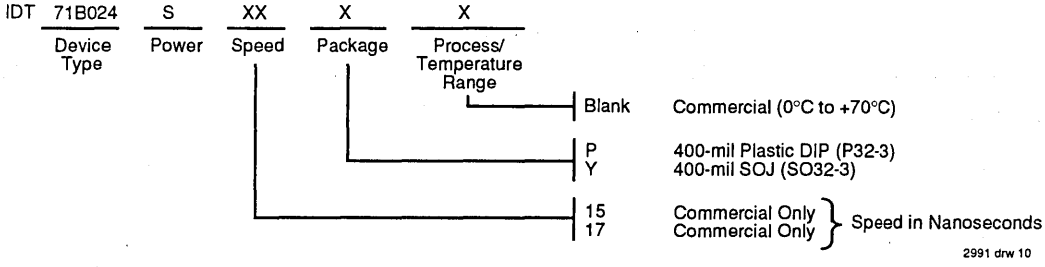


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS1}$ AND CS2 CONTROLLED TIMING)(1, 2, 5)



NOTES:
1. $\overline{WE}$ must be HIGH, $\overline{CS1}$ must be HIGH, or CS2 must be LOW during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS1}$, HIGH CS2, and a LOW $\overline{WE}$.
3. t_{WR} is measured from the earlier of either $\overline{CS1}$ or $\overline{WE}$ going HIGH or CS2 going LOW to the end of the write cycle.
4. During this period I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS1}$ LOW transition or the CS2 HIGH transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state. $\overline{CS1}$ and CS2 must both be active during the t_{CW} write period.
6. Transition is measured ±200mV from steady state.
7. $\overline{OE}$ is continuously HIGH. During a $\overline{WE}$ controlled write cycle with $\overline{OE}$ LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified t_{WP}.

ORDERING INFORMATION



8

Integrated Device Technology, Inc.

BiCMOS STATIC RAM 1 MEG (128K x 8-BIT) REVOLUTIONARY PINOUT

ADVANCE INFORMATION
IDT71B124

FEATURES:

- 128K x 8 advanced high-speed BiCMOS static RAM
- JEDEC revolutionary pinout (center power/GND) for reduced noise
- Equal access and cycle times
  - — Commercial: 10/12/15ns
- One Chip Select plus one Output Enable pin
- Bidirectional inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Available in JEDEC 32-pin Plastic DIP and SOJ packages

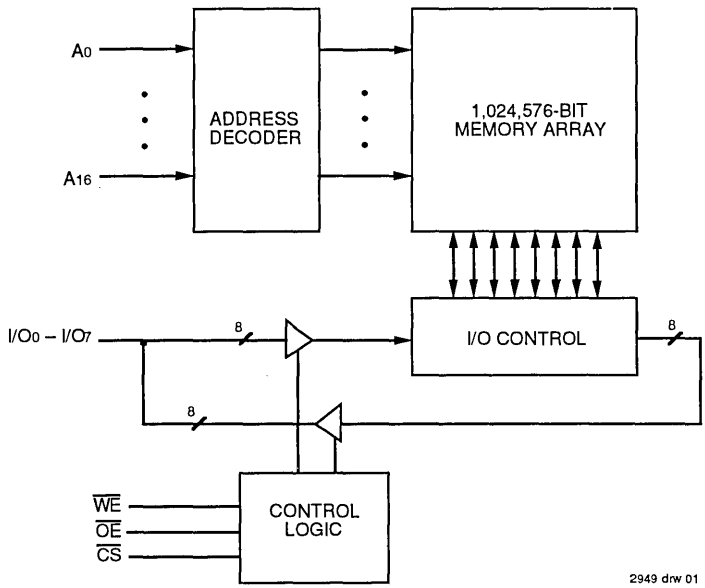
DESCRIPTION:

The IDT71B124 is a 1,024,576-bit high-speed Static RAM organized as 128Kx8. It is fabricated using IDT's high-perfomance, high-reliability BiCMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs. The JEDEC center pin power/GND pinout reduces noise generation and improves high speed system performance.

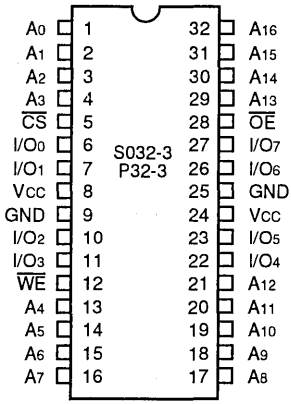
The IDT71B124 has an output enable pin which operates as fast as 5ns, with address access times as fast as 10ns available. All bidirectional inputs and outputs of the IDT71BR024 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used; no clocks or refresh are required for operation.

The IDT71B124 is packaged in 32-pin 400 mil Plastic DIP and 32-pin 400 mil Plastic SOJ packages.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



2949 drw 02

DIP/SOJ
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTES: 2949 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 0.5V.

TRUTH TABLE(1,2)

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
L	L	H	$DATA_{OUT}$	Read Data
L	X	L	$DATA_{IN}$	Write Data
L	H	H	High-Z	Outputs Disabled
H	X	X	High-Z	Deselected - Standby (I_{SB})
V_{HC}(3)	X	X	High-Z	Deselected - Standby (I_{SB1})

NOTES: 2949 tbl 01

1. H = V_{IH}, L = V_{IL}, x = Don't care.
2. V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V.
3. Other inputs ≥V_{HC} or ≤V_{LC}.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	8	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	8	pF

NOTE: 2949 tbl 03

1. This parameter is guaranteed by device characterization, but not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	V_{CC}+0.5	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2949 tbl 04

1. V_{IL} (min.) = –1.5V for pulse width less than 10ns, once per cycle.

8

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71B124 Min.	IDT71B124 Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

2949 tbl 05

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

Symbol	Parameter	71B124S10		71B124S12		71B124S15		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Dynamic Operating Current, $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	175	—	165	—	155	—	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	35	—	30	—	30	—	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, Outputs Open, V_{CC} = Max., f = 0(2), $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$	12	—	12	—	12	—	mA

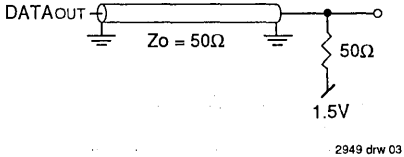
NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.

2949 tbl 06

AC TEST CONDITIONS

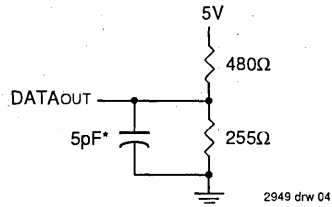
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1, 2, and 3

2949 tbl 07



2949 drw 03

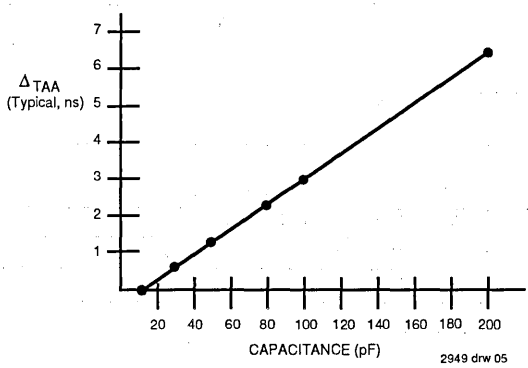
Figure 1. AC Test Load



2949 drw 04

*Including jig and scope capacitance.

Figure 2. AC Test Load (for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})



2949 drw 05

Figure 3. Lumped Capacitive Load, typical Derating

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%)

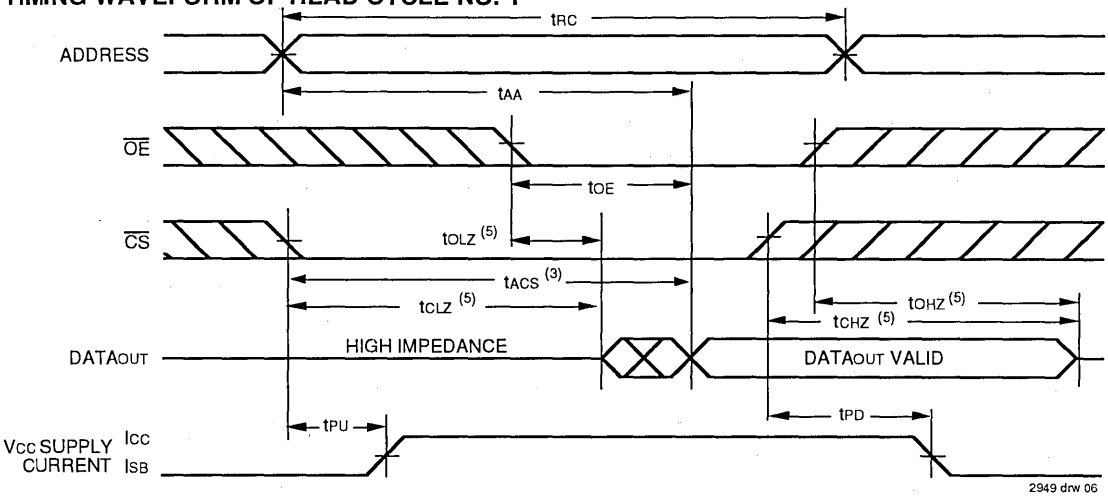
Symbol	Parameter	71B124S10		71B124S12		71B124S15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	10	—	12	—	15	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	ns
t_{ACS}	Chip Select Access Time	—	10	—	12	—	15	ns
t_{CLZ}[1]	Chip Select to Output in Low-Z	2	—	3	—	3	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High-Z	0	5	0	6	0	7	ns
t_{OE}	Output Enable to Output Valid	—	5	—	6	—	7	ns
t_{OLZ}[1]	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
t_{OHZ}[1]	Output Disable to Output in High-Z	0	5	0	6	0	7	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Down Time	—	10	—	12	—	15	ns
Write Cycle								
t_{WC}	Write Cycle Time	10	—	12	—	15	—	ns
t_{AW}	Address Valid to End of Write	8	—	9	—	10	—	ns
t_{CW}	Chip Select to End of Write	8	—	9	—	10	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	8	—	9	—	10	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	6	—	7	—	8	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End of Write	3	—	3	—	3	—	ns
t_{WHZ}[1]	Write Enable to Output in High-Z	0	5	0	6	0	7	ns

NOTE:
1. This parameter guaranteed with the AC load (Figure 2) by device characterization, but is not production tested.

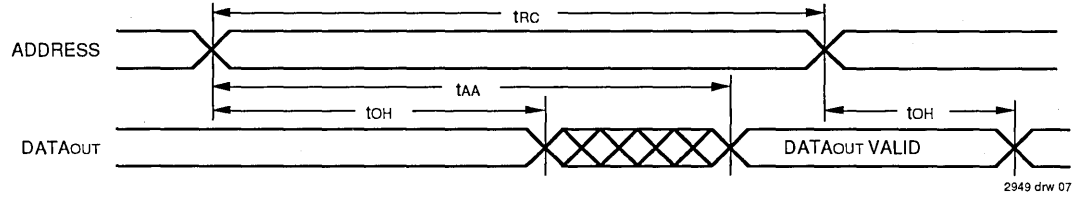
2949 tbl 08

8

TIMING WAVEFORM OF READ CYCLE NO. 1(1)

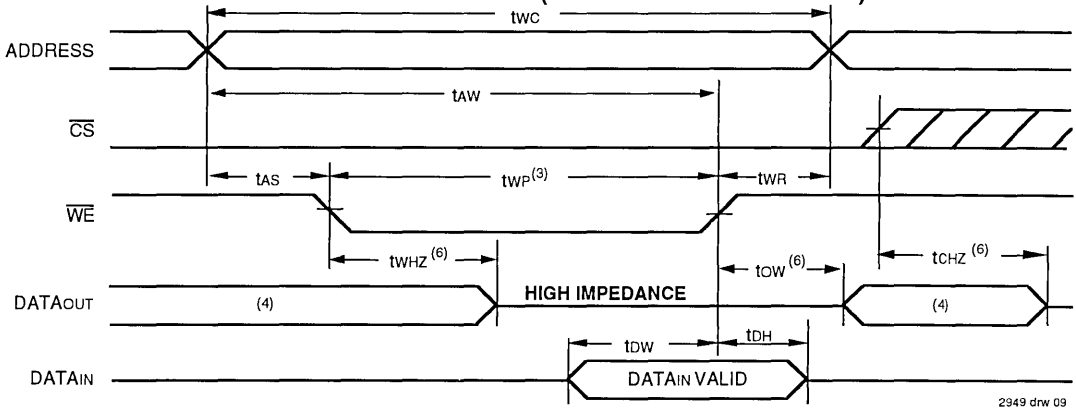


TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)

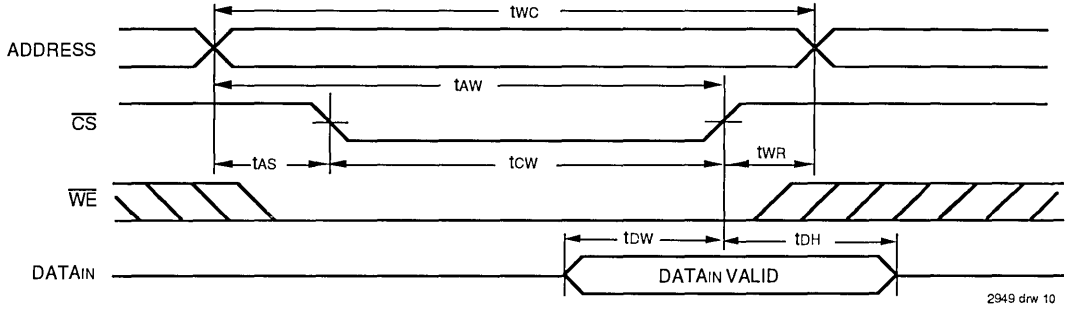


NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address must be valid prior to or coincident with the later of $\overline{CS}$ transition LOW; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 5)



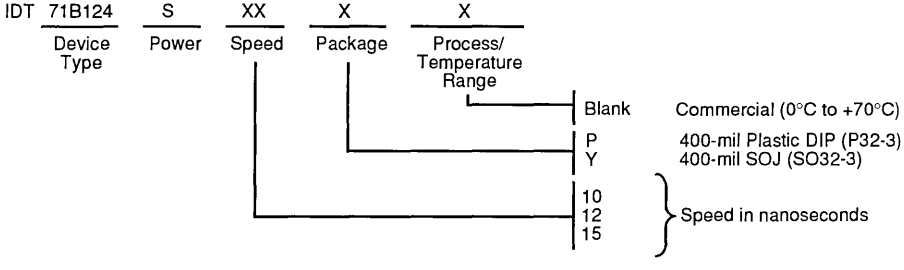
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified t_{WP}.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state.

8

ORDERING INFORMATION



3.3V SRAM PRODUCTS

IDT has recently introduced the first true fast 3.3V SRAM in the world, the IDT713256SL. This 32K x 8 SRAM contrasts with re-characterized 5V parts that degrade in speed and may have potential problems meeting the thresholds specified in the new JEDEC 3.3V LVTTL standard.

By developing 3.3V-specific designs and processes, IDT's 3.3V SRAMs exhibit excellent parametric characteristics both in speed and power consumption, as well as full compliance with the JEDEC LVTTL standard.

IDT is fully committed to offering 3.3V fast SRAMs for the new generation of systems, and the IDT713256SL is but the first of what will be a very prolific family. A 1M (128K x 8) version is the first to follow.

These parts are ideal for portable equipment where both battery-life extension is essential and high-performance is necessary (<30ns speeds). The small SOJ packages available help alleviate the typical space constraint in portable equipment.

Size	Org.	Features	Process	Part Number	Power	Speeds	
						Commercial	Military
3.3V RAMS	32K x 8	3.3V	3.3V CMOS	713256	SL	20,25,30	N/A
	128K x 8	3.3V	3.3V CMOS	713024	SL	20,25	N/A

9

TABLE OF CONTENTS

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Integrated Device Technology, Inc.

VERY LOW POWER 3.3V CMOS FAST SRAM 256K (32K x 8-BIT)

PRELIMINARY INFORMATION IDT713256SL

FEATURES

- Ideal for 16/32-bit notebook/sub-notebook cache at 20, 25, and 33MHz, and for other battery-operated equipment
- Very low standby current (maximums):
  - — 3.0mA standby
  - — 500uA full standby
- Fast access times:
  - — 20/25/30ns
- Battery-backup operation: 2V data retention
  - — 300uA data retention current (max.)
- Small package for space-efficient layouts:
  - — 28-pin 300 mil SOJ
- Ideal configuration for large cache sizes, with minimum space and minimum power:
  - — 32K x 8
- Produced with advanced high-performance CMOS technology
- Input and output are TTL-compatible
- Single 3.3V(±0.3V) power supply

DESCRIPTION

The IDT713256SL is a 262,144-bit high-speed static RAM organized as 32K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology.

The IDT713256SL has outstanding low power characteristics, as well as fast speeds.

Address access times of 20, 25, and 30ns are ideal for 16 and 32-bit notebook and laptop cache designs running at 20, 25, and 33MHz, and operating from 3.3 volts. For instance, two of these SRAMs interface directly to many 386 notebook cache controllers to form a 64kB cache. Portable communications and test equipment benefit from these fast speeds and low power too.

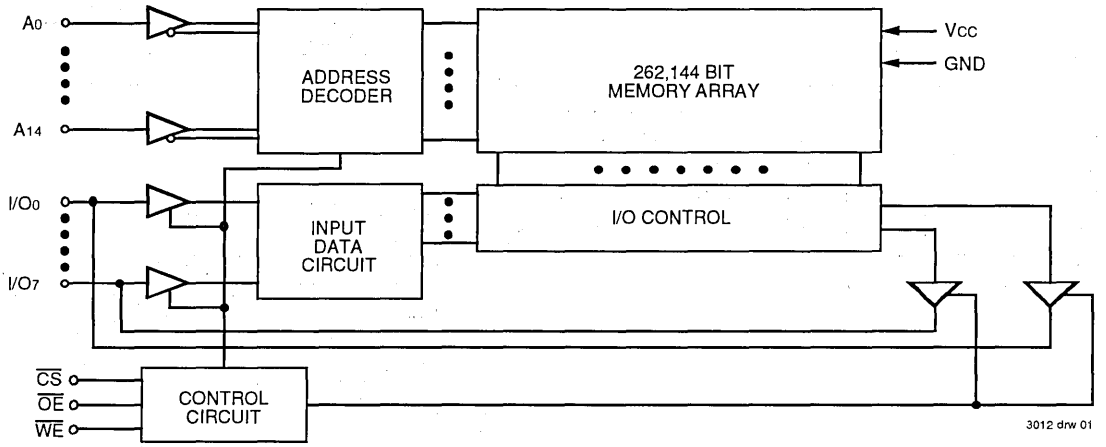
When the power management logic puts the IDT713256SL in standby mode, its very low power characteristics contribute to extended battery life.

When $\overline{CS}$ goes HIGH, the SRAM will automatically go to a low power standby mode and will remain in standby as long as $\overline{CS}$ remains HIGH. Furthermore, under full standby mode ($\overline{CS}$ at CMOS level, f=0), power consumption is guaranteed to always be less than 1.65mW and typically will be much smaller.

This SRAM also offers battery-backup data retention at as little as 2 volts. Under this condition, power consumption is guaranteed not to exceed 1.0mW and typically will be much smaller.

The package chosen for this device, 28-pin 300mil SOJ, helps the designer attain the stringent space goals typical of notebooks, sub-notebooks, and battery-operated portable equipment.

FUNCTIONAL BLOCK DIAGRAM



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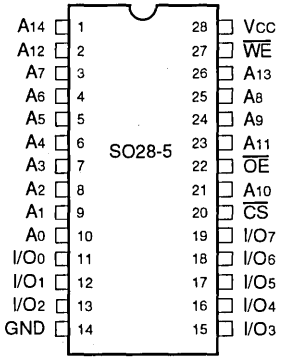
PIN CONFIGURATIONS



3012 drw 02

SOJ
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to VCC+0.5	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTES: 3012 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals only
3. Input, Output, and I/O terminals; 4.6V maximum

PIN DESCRIPTIONS

Name	Description
A_0–A_{14}	Addresses
I/O_0–I/O_7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
Vcc	Power

3012 tbl 01

CAPACITANCE (T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	7	pF

NOTE: 3012 tbl 04

1. This parameter is determined by device characterization, but is not production tested.

TRUTH TABLE(1)

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	I/O	Function
X	H	X	High-Z	Standby (ISB)
X	V_{HC}	X	High-Z	Standby (ISB1)
H	L	H	High-Z	Output Disable
H	L	L	D_{OUT}	Read
L	L	X	D_{IN}	Write

NOTE: 3012 tbl 02

1. H = V_{IH}, L = V_{IL}, X = Don't Care

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	3.3V ± 0.3V

3012 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	3.0	3.3	3.6	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	Vcc+0.3	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 3012 tbl 06

1. V_{IL} (min.) = –1.0V for pulse width less than 5ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS(1, 2)

(V_{CC} = 3.3V ± 0.3V, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	713256SL20 Com'l.	713256SL25 Com'l.	713256SL30 Com'l.	Unit
I_{CC}	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	SL	95	90	85	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ = V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX}(2)	SL	3	3	3	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, V_{CC} = Max., f = 0	SL	0.5	0.5	0.5	mA

3012 tbl 07

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC}, only address inputs cycling at fmax; f = 0 means that no inputs are cycling.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

3012 tbl 08

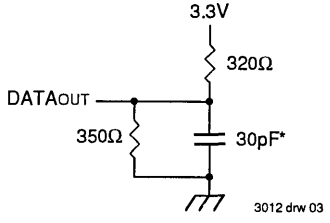


Figure 1. AC Test Load

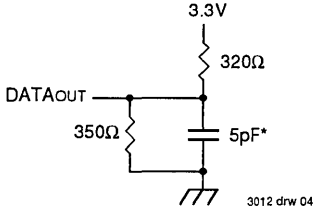


Figure 2. AC Test Load (for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

*Includes scope and jig capacitances

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V± 0.3V

Symbol	Parameter	Test Condition	IDT713256SL Min.	Typ.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	—	2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	—	2	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	—	V

3012 tbl 09

9

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

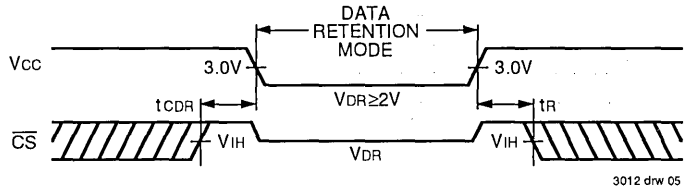
V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Condition	Min.	Typ. [1] Vcc @ 2.0v	Max. Vcc @ 2.0V	Unit
V_{DR}	VCC for Data Retention	—	2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$	—	—	300	µA
t_{CDR}	Chip Deselect to Data Retention Time		0	—	—	ns
t_R[3]	Operation Recovery Time		t_{RC}[2]	—	—	ns

3012 tbl 10

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed, but is not production tested.

LOW V_{CC} DATA RETENTION WAVEFORM



3012 drw 05

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 3.3V ± 0.3V, ALL TEMPERATURE RANGES)

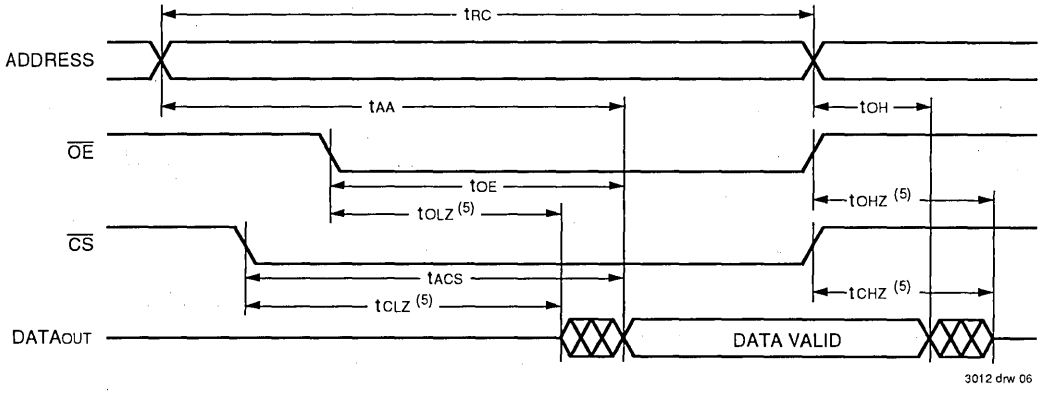
Symbol	Parameter	713256SL20		713256SL25		713256SL30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	20	—	25	—	30	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	30	ns
t_{ACS}	Chip Select Access Time	—	20	—	25	—	30	ns
t_{CLZ}	Chip Select to Output in Low-Z[1]	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	8	—	10	—	13	ns
t_{OLZ}	Output Enable to Output in Low-Z[1]	3	—	3	—	3	—	ns
t_{CHZ}	Chip Select to Output in High-Z[1]	0	10	0	11	0	13	ns
t_{OHZ}	Output Disable to Output in High-Z[1]	2	8	2	10	2	13	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	ns
Write Cycle								
t_{WC}	Write Cycle Time	20	—	25	—	30	—	ns
t_{CW}	Chip Select to End-of-Write	15	—	20	—	25	—	ns
t_{AW}	Address Valid to End-of-Write	15	—	20	—	25	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	15	—	15	—	25	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}	Write Enable to Output in High-Z[1]	1	10	1	11	1	13	ns
t_{DW}	Data to Write Time Overlap	8	—	10	—	13	—	ns
t_{DH1}	Data Hold from Write Time ($\overline{WE}$)	0	—	0	—	0	—	ns
t_{DH2}	Data Hold from Write Time ($\overline{CS}$)	0	—	0	—	0	—	ns
t_{OW}	Output Active from End-of-Write[1]	5	—	5	—	5	—	ns

NOTE:
1. This parameter guaranteed with the AC test load (Figure 2) by device characterization, but is not production tested.

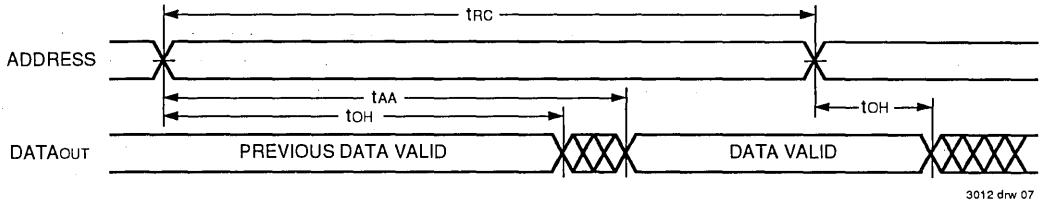
3012 tbl 11

9

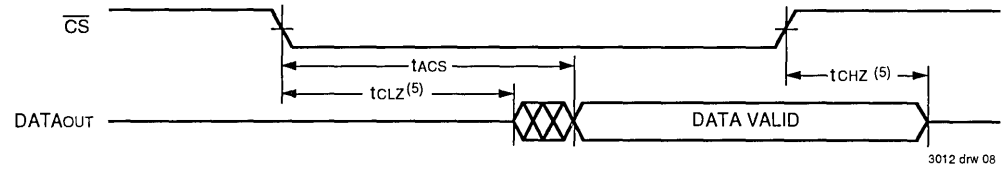
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)

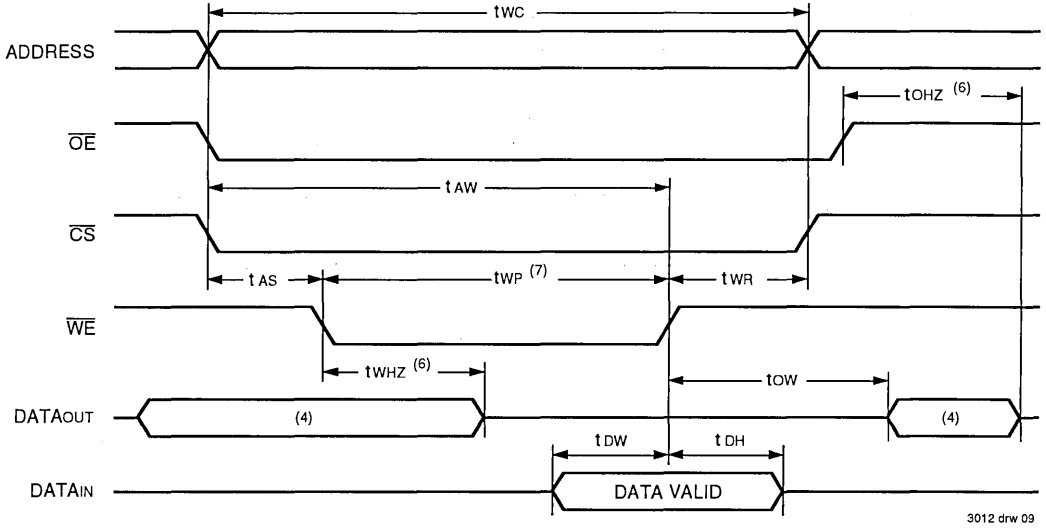


TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)

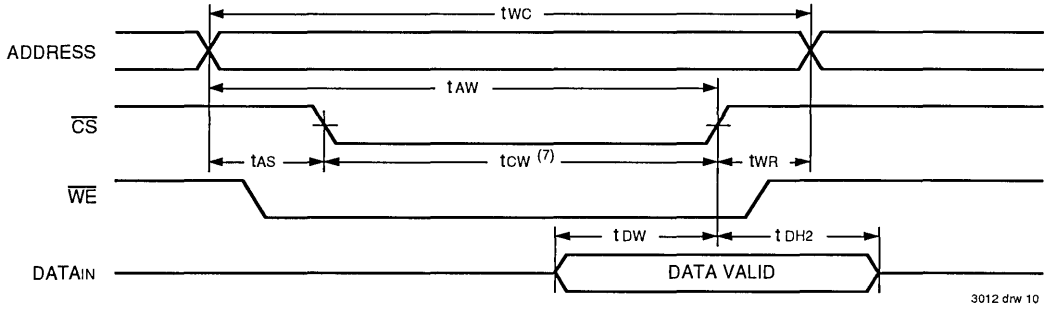


NOTES:
1. $\overline{WE}$ is HIGH for read cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 5, 7)

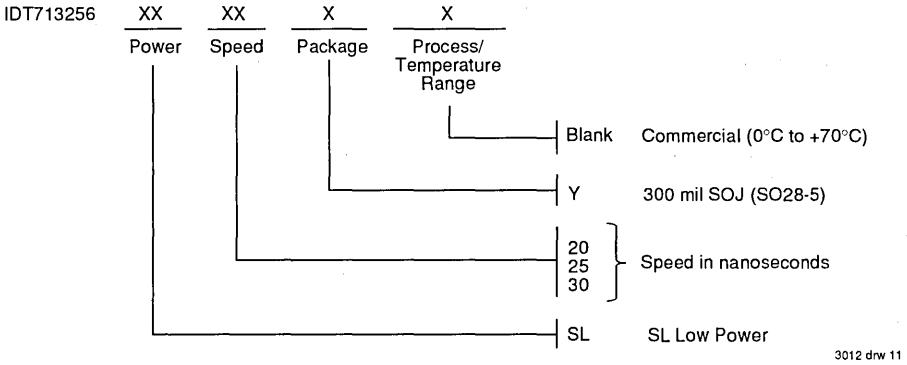


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state.
7. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

ORDERING INFORMATION



Integrated Device Technology, Inc.

VERY LOW POWER 3.3V CMOS FAST SRAM 1 MEG (128K x 8-BIT)

ADVANCE INFORMATION IDT713024SL

FEATURES:

- 128K x 8 advanced high-speed CMOS Static RAM
- Equal access and cycle times
  - — Commercial: 20/25ns
- True 3.3V design, not a re-characterized 5V device
- Ideal for battery-operated equipment, including notebook computers, portable instruments, and portable communications devices
- Low standby currents and 2V data retention mode
- Two Chip Selects plus one Output Enable pin
- Bidirectional inputs and outputs directly TTL-compatible
- Compliant with all JEDEC LVTTL standard specifications
- Single 3.3V (±0.3V) power supply, resulting in 57% dynamic power savings over equivalent 5 volt devices
- Available in 400 mil plastic DIP and plastic SOJ packages

DESCRIPTION:

The IDT713024SL is a 1,024,576-bit high-speed Static RAM organized as 128K x 8. It is fabricated using IDT's high-perfomance, high-reliability 3.3V CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, results in a unique combination of speed and low power consumption, with only a 3.3V supply.

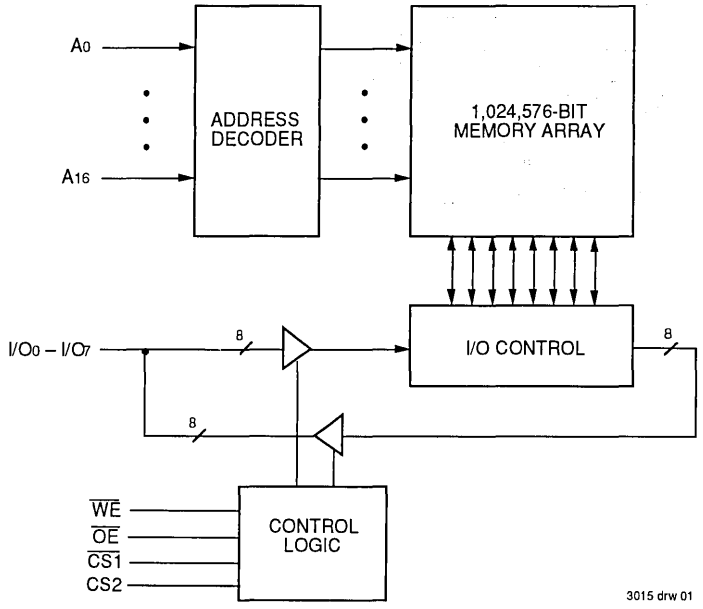
Unlike re-characterized 5V devices, the IDT713024SL is the result of a dedicated 3.3V design, which ensures full compliance with the JEDEC LVTTL standard of operation in terms of thresholds and noise margins. This dedicated 3.3V technology also allows for a faster device.

The IDT713024SL has address access times as fast as 20ns. All bidirectional inputs and outputs are TTL-compatible and operation is from a single 3.3V supply.

This SRAM offers a very low standby current, as well as a data retention mode that guarantees that data be preserved at voltages as low as 2 volts. These characteristics make the IDT713024SL ideal for high-performance applications that are powered by batteries, as well as AC-powered systems that need to minimize power consumption.

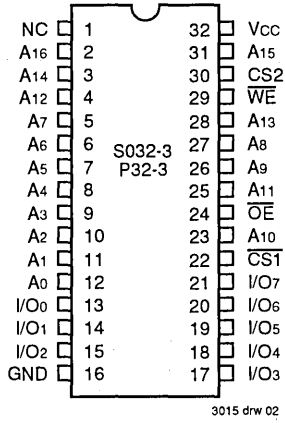
The IDT713024SL is packaged in a 32-pin 400 mil plastic DIP, and a 32-pin 400 mil plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



9

PIN CONFIGURATION



DIP/SOJ
TOP VIEW

TRUTH TABLE(1,2)

INPUTS					
$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	I/O	FUNCTION
X	H	X	X	High-Z	Deselected–Standby (I_{SB})
X	V_{HC}(3)	X	X	High-Z	Deselected–Standby (I_{SB1})
X	X	L	X	High-Z	Deselected–Standby (I_{SB})
X	X	V_{LC}(3)	X	High-Z	Deselected–Standby (I_{SB1})
H	L	H	H	High-Z	Outputs Disabled
H	L	H	L	DATAOUT	Read Data
L	L	H	X	DATAIN	Write Data

3015 tbl 01

NOTES:
1. H = V_{IH}, L = V_{IL}, X = Don't care.
2. V_{LC} = 0.2V, V_{HC} = V_{CC}-0.2V.
3. Other inputs ≥V_{HC} or ≤V_{LC}.

SPECIALTY SRAM PRODUCTS

IDT has been the industry pioneer in processor-specific specialty SRAMs and cache tags.

The IDT line of specialty memories includes the fastest cache tags in the world, with address-to-match times as fast as 8ns. These tags help PC and workstation designers in the most critical data paths of high-performance systems. By including a comparator on-board, the cache tag saves in both part count and propagation delays. A 4K x 4 device in CMOS technology is available at 10ns, while the industry-leading BiCMOS 8K x 8 is available at 8ns. Surface mount packages facilitate the incorporation of these cache tags into high-performance systems.

Careful attention to power consumption has allowed IDT to offer cache memories that are well suited for 5V notebook systems. Speeds as fast as 20ns are preserved in these surface-mount components, thus supporting up to 40MHz processors.

The CacheRAM concept pioneered by IDT has yielded two components with very tight interfaces to specific processors. The IDT71589SA was introduced as the first 486-specific cache in the market, and it has been followed by its BiCMOS counterpart—the IDT71B589. The latter, at 10.5ns, is the first P5-67MHz (as well as 486-50MHz) cache SRAM introduced to the market. These two components share the same distinctive features that facilitate no wait-state cache designs, like self-timed write, a burst counter, small 32-pin SOJ package, and processor-specific interface.

Finally, the IDT71B229 BiCMOS CacheRAM uses two banks of internally multiplexed instruction and data cache to attain a no wait-state solution for the R3000, R3001 and R3500 RISC processors. The innovative architecture found in this component is representative of the creative ideas implemented by IDT into SRAMs to solve difficult cache timing

Size	Org.	Features	Process	Part Number	Power	Speeds	
						Commercial	Military
Specialty	4K x 4	Tag	CMOS	6178	S	10,12,15,20,25	15,20,25
	8K x 8	Tag	BiCMOS	71B74	S	8,10,12,15	N/A
	32K x 8	Notebook	CMOS	71256	SL/L	25,35	NA
	32K x 9	Burst	CMOS	71589	S	20,25,35	N/A
	32K x 9	Burst	BiCMOS	71B589	S	10,12,14	N/A
	16K x 9 x 2	Bicameral	BiCMOS	71B229	S	12,16,22	N/A

TABLE OF CONTENTS

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Integrated Device Technology, Inc.

CMOS STATIC RAM 16K (4K x 4-BIT) CACHE-TAG RAM

IDT6178S

FEATURES:

- High-speed Address to MATCH Valid time
  - Military: 12/15/20/25ns
  - Commercial: 10/12/15/20/25ns (max.)
- High-speed Address Access time
  - Military: 12/15/20/25ns
  - Commercial: 10/12/15/20/25ns (max.)
- Low-power consumption
  - IDT6178S
    Active: 300mW (typ.)
- Produced with advanced CMOS high-performance technology
- Input and output TTL-compatible
- Standard 22-pin Plastic or Ceramic DIP, 24-pin SOJ
- Military product 100% compliant to MIL-STD-883, Class B

DESCRIPTION:

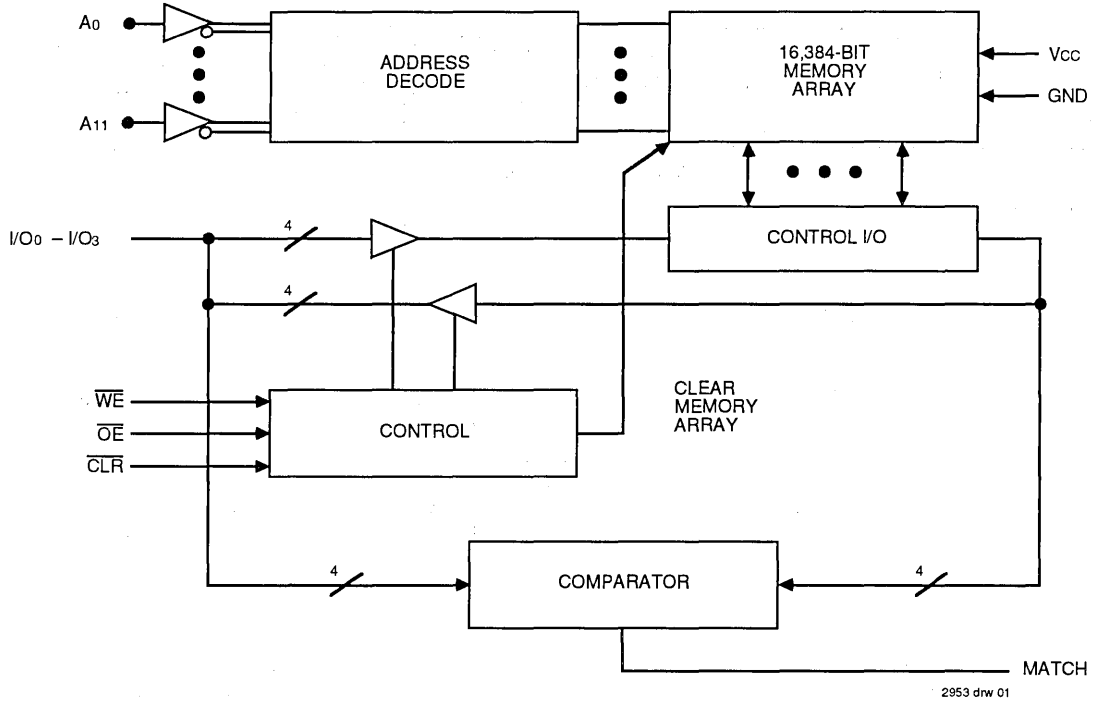
The IDT6178 is a high-speed cache address comparator sub-system consisting of a 16,384-bit static RAM organized as 4K x 4. Cycle Time and Address to MATCH Valid are equal. The IDT6178 features an onboard 4-bit comparator that compares RAM contents and current input data. The result is an active high on the MATCH pin. The MATCH pins of several IDT6178's can be nanded together to provide enabling or acknowledging signals to the data cache or processor.

The IDT6178 is fabricated using IDT's high-performance, high-reliability technology — CMOS. Address to MATCH and Data to MATCH times are as fast as 10ns.

All inputs and outputs of the IDT6178 are TTL-compatible and the device operates from a single 5V supply.

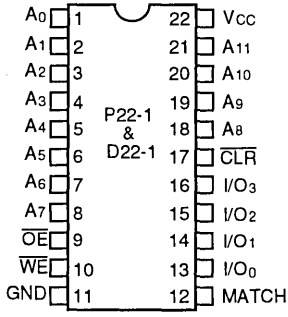
The IDT6178 is packaged in either a 22-pin, 300-mil Plastic or Ceramic DIP package or 24-pin SOJ. Military grade product is manufactured in compliance with latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

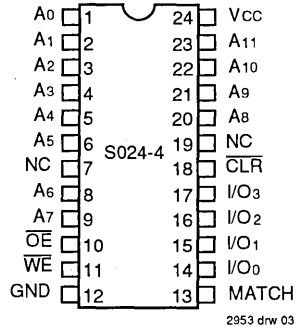


2953 drw 01

PIN CONFIGURATIONS



DIP
TOP VIEW



SOJ
TOP VIEW

PIN NAMES

A0 – A11	Address	WE	Write Enable
I/O0 – I/O3	Data Input/Output	OE	Output Enable
MATCH	Match	CLR	Clear
Vcc	Power	GND	Ground

2953 tbl 01

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 2 and 3
AC Test Load for Match Cycle	See Figure 1

2953 tbl 03

TRUTH TABLES(1)

WE	OE	CLR	MATCH	Mode
H	H	H	Valid(2)	Match Cycle
L	X	H	Invalid	Write Cycle
H	L	H	Invalid	Read Cycle
X	X	L	Invalid	Clear Cycle

2953 tbl 02

NOTE:
1. H = VIH, L = VIL, X = Don't care.
2. Valid Match = VOH, Valid Non-Match = VOL.

CAPACITANCE (TA = 25°C, f = 1MHz)

Symbol	Parameter	Condition	Max	Units
CIN	Input Capacitance	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

2953 tbl 02

NOTE:
1. This parameter is determined by device characterization, but is not production tested.

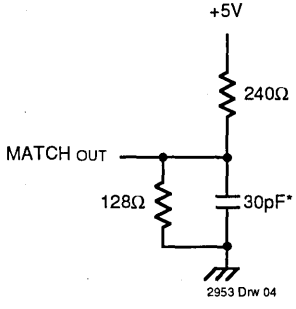


Figure 1. AC Test Load for MATCH

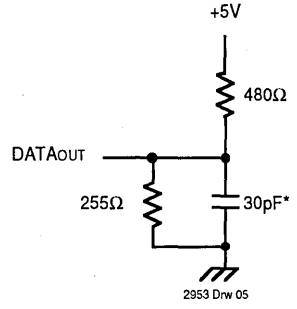


Figure 2. AC Test Load

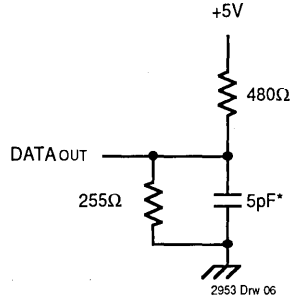


Figure 3. AC Test Load (for tOLZ, tOHZ, tWHZ, tOW)

* Including scope and jig.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–65 to +135	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

2953 tbl 04

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2[2]	–	6.0	V
V_{IL}	Input Low Voltage	–0.5[1]	–	0.8	V

2953 tbl 05

NOTES:
1. V_{IL} = –3.0V for pulse width less than 20ns, once per cycle.
2. V_{IH} = 2.5V for clear pin.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%
Military	–55°C to +125°C	0V	5.0V ± 10%

2953 tbl 06

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	Test Condition	6178S Min.	6178S Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{OE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA (I/O_0 – I/O_3)	—	0.4	V
		I_{OL} = 10mA (I/O_0 – I/O_3)	—	0.5	V
		I_{OL} = 16mA (Match)	—	0.4	V
		I_{OL} = 20mA (Match)	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = –4mA (I/O_0 – I/O_3)	2.4	—	V
		I_{OH} = –8mA (Match)	2.4	—	V

2953 tbl 07

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter		6178S10 Max.	6178S12[1] Max.	6178S15[1] Max.	6178S20/25 Max.	Unit
I_{CC1}	Operating Power Supply Current	COM'L.	90	90	90	90	mA
	Outputs Open, V_{CC} = Max., f = 0[2]	MIL.	—	110	110	110	mA
I_{CC2}	Dynamic Operating Current	COM'L.	180	160	140	140	mA
	Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	MIL.	—	180	160	160	mA

2953 tbl 08l

NOTES:
1. Military values are preliminary only.
2. f_{MAX} = 1/t_{RC}, only address inputs are cycling at f_{MAX}. f = 0 means no address inputs change.

10

CYCLE DESCRIPTION

Match Cycle: A match cycle occurs when all control signals ($\overline{OE}$, $\overline{WE}$, $\overline{CLR}$) are HIGH. At that time, data supplied to the RAM on the I/O pins is compared with the data stored at the specified address. The totem-pole match output is HIGH when there is a match at all data bits, and drives LOW if there is not a match.

Write Cycle: The write cycle is conventional, occuring when $\overline{WE}$ isLOW and $\overline{CLR}$ is HIGH. $\overline{OE}$ may be either HIGH or LOW, since it is overridden by $\overline{WE}$. The state of the Match pin is not guaranteed, but in the current implementation it continues to reflect the output of the comparator. The Match pin goes HIGH during write cycles since the data at the specified address is the same as the data (being written) at the I/Os of the RAM.

Read Cycle: When $\overline{WE}$ and $\overline{CLR}$ are HIGH and $\overline{OE}$ isLOW, the RAM is in a read cycle. The state of the Match pin is not guaranteed, but in the current implementation it continues to reflect the output of the comparator. The Match pin goes HIGH during read cycles since the data at the specified address is the same as the data (being read) at the I/Os of the RAM.

Clear Cycle: When $\overline{CLR}$ is asserted, every bit in the RAM is cleared to zero. If $\overline{OE}$ is LOW during a clear cycle, the RAM I/Os will be driven. However, this data is not necessarily zeros, even after a considerable time. The Match pin is enabled, but its state is not predicable.

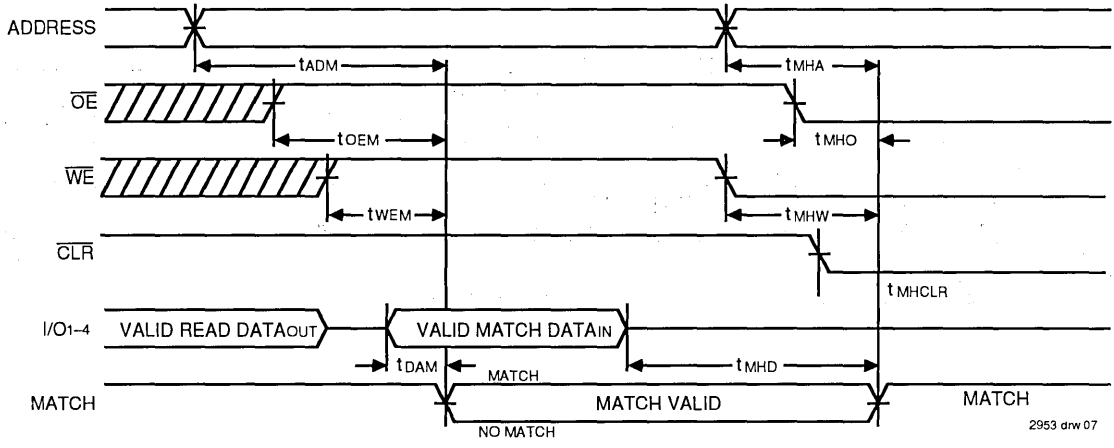
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6178S10[1] Min.	6178S10[1] Max.	6178S12 Min.	6178S12 Max.	6178S15 Min.	6178S15 Max.	6178S20 Min.	6178S20 Max.	6178S25 Min.	6178S25 Max.	Unit
Match Cycle												
t_{ADM}	Address to Match Valid	—	10	—	12	—	15	—	20	—	25	ns
t_{DAM}	Data Input to Match Valid	—	8	—	11	—	13	—	15	—	15	ns
t_{MHO}	Match Valid Hold from $\overline{OE}$	0	—	0	—	0	—	0	—	0	—	ns
t_{OEM}	$\overline{OE}$ HIGH to Match Valid	—	10	—	12	—	15	—	20	—	20	ns
t_{MHW}	Match Valid Hold from $\overline{WE}$	0	—	0	—	0	—	0	—	0	—	ns
t_{WEM}	$\overline{WE}$ HIGH to Match Valid	—	10	—	12	—	15	—	20	—	20	ns
t_{MHCLR}	Match Valid Hold from $\overline{CLR}$	0	—	0	—	0	—	0	—	0	—	ns
t_{MHA}	Match Valid Hold from Address	3	—	3	—	3	—	3	—	3	—	ns
t_{MHD}	Match Valid Hold from Data	3	—	3	—	3	—	3	—	3	—	ns

NOTE:
1. 0°C to +70°C temperature range only.

2953 tbl 09

TIMING WAVEFORM OF MATCH CYCLE[1]



NOTE:
1. It is not recommended to let address and data input pins float while MATCH pin is active.

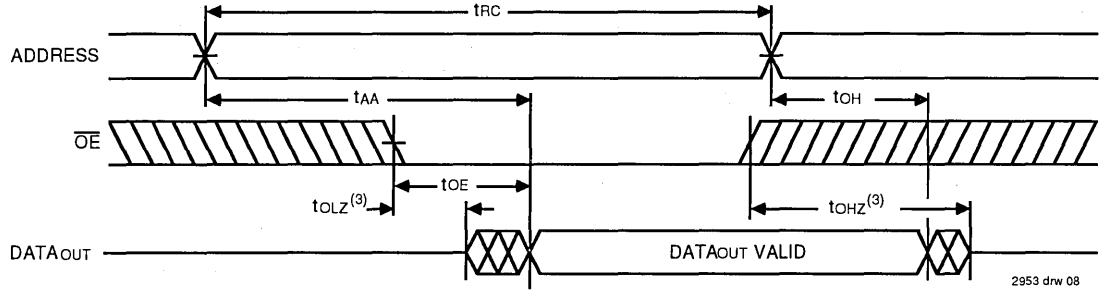
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6178S10[3]		6178S12		6178S15		6178S20/25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	10	—	12	—	15	—	20/25	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	—	20/25	ns
t_{OE}	Output Enable Access Time	—	7	—	8	—	10	—	15	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t_{OLZ}	Output Enable to Output in Low-Z Time[1,2]	2	—	2	—	2	—	2	—	ns
t_{OHZ}	Output Disable to Output in High-Z Time[1,2]	—	6	—	7	—	9	—	12	ns

NOTES:
2953 tbl 10

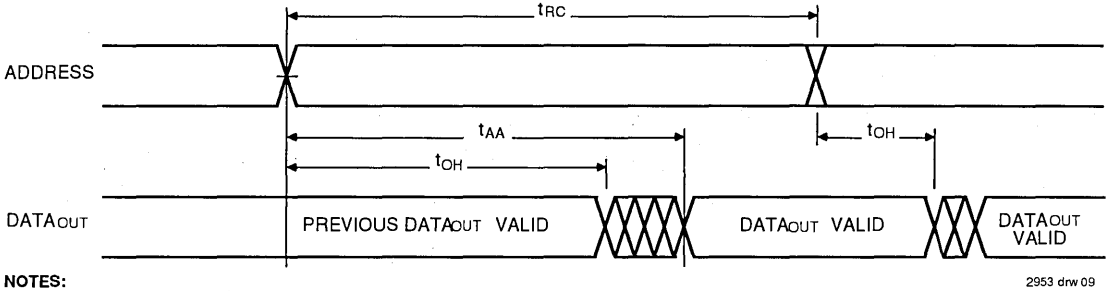
1. Transition is measured ±200mV from steady state.
2. This parameter guaranteed with AC load (Figure 3) by device characterization, but is not production tested.
3. 0°C to +70°C temperature range only.

TIMING WAVEFORM OF READ CYCLE NO. 1[1]



2953 drw 08

TIMING WAVEFORM OF READ CYCLE NO. 2[1,2]



2953 drw 09

NOTES:
1. $\overline{WE}$ is HIGH for read cycle, $\overline{WE} \geq V_{IH}$.
2. Output enable is continuously active, $\overline{OE} \leq V_{IL}$.
3. Transition is measured ±200V from Steady State.

10

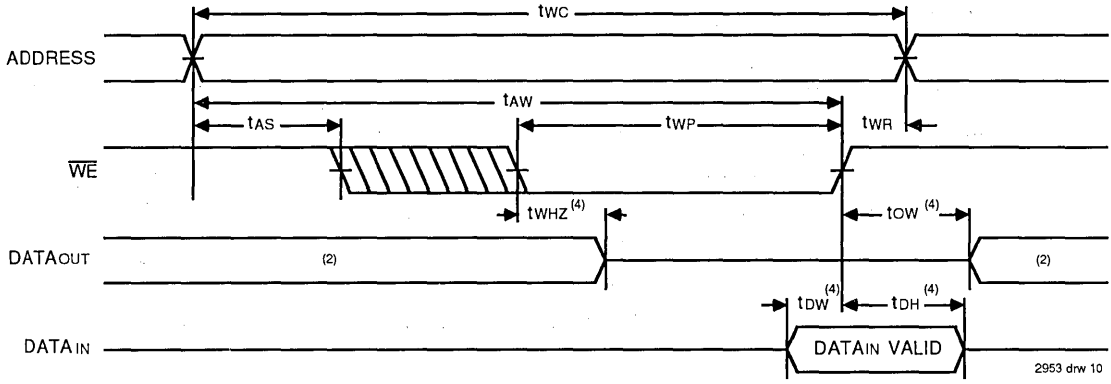
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6178S10[3] Min.	6178S10[3] Max.	6178S12 Min.	6178S12 Max.	6178S15 Min.	6178S15 Max.	6178S20/25 Min.	6178S20/25 Max.	Unit
Write Cycle										
t_{WC}	Write Cycle Time	10	—	12	—	15	—	20	—	ns
t_{AW}	Address Valid to End-of-Write	8	—	10	—	12	—	14	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	8	—	10	—	12	—	14	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	6	—	8	—	10	—	12	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}	Write Enable to Output in High-Z[1,2]	—	5	—	6	—	7	—	9	ns
t_{OW}	Output Active from End-of-Write[1,2]	0	—	0	—	0	—	0	—	ns

2953 tbl 11

NOTES:
1. Transition is measured ±200mV from steady state.
2. This parameter guaranteed with AC load (Figure 3) by device characterization, but is not production tested.
3. 0°C to +70°C temperature range only.

TIMING WAVEFORM OF WRITE CYCLE[1,3]



NOTES:
1. $\overline{WE}$ must be HIGH during all address transitions, $\overline{WE} \geq V_{IH}$.
2. During this period, I/O pins are in the output state and the input signals must not be applied.
3. $\overline{OE}$ is continuously HIGH, $\overline{OE} \geq V_{IH}$. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the greater of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse is the specified t_{WP}.
4. Transition is measured ±200mV from steady state.

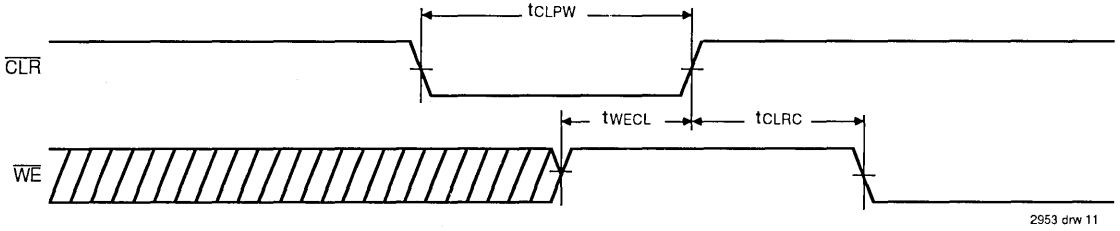
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6178S10[2] Min.	6178S10[2] Max.	6178S12 Min.	6178S12 Max.	6178S15 Min.	6178S15 Max.	6178S20/25 Min.	6178S20/25 Max.	Unit
Clear Cycle										
t_{CLPW}	$\overline{CLR}$ Pulse Width[1]	12	—	15	—	20	—	25	—	ns
t_{CLRC}	$\overline{CLR}$ HIGH to $\overline{WE}$ LOW	5	—	5	—	5	—	5	—	ns
t_{POCL}	Power on Reset[3]	50	—	60	—	80	—	100	—	ns
t_{WECL}	$\overline{WE}$ HIGH to Clear HIGH	5	—	5	—	5	—	5	—	ns

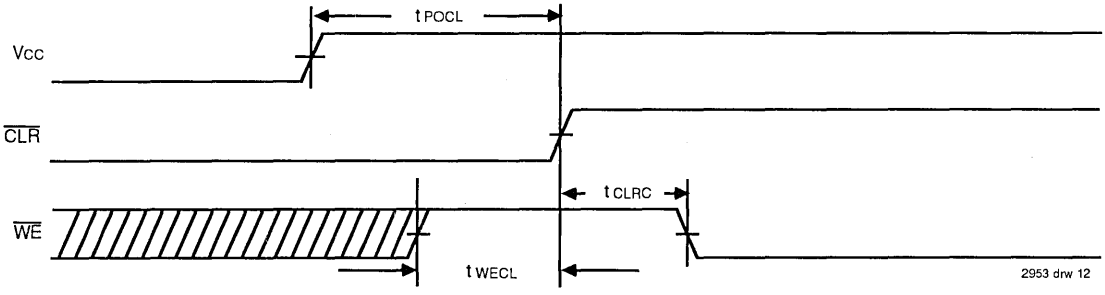
2953 tbl 12

NOTES:
1. Recommended duty cycle of 10% maximum.
2. 0°C to +70°C temperature range only.
3. This parameter guaranteed with AC load (Figure 3) by device characterization, but is not production tested.

TIMING WAVEFORM OF CLEAR CYCLE



POWER ON RESET TIMING



ORDERING INFORMATION

IDT 6178 (Device Type) S (Power) XX (Speed) X (Package) X (Process/Temperature)

Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C, Compliant to MIL-STD-883, Class B)
P	300 mil Plastic DIP (P22-1)
Y	300 mil Small Outline, J bend (SO24-4)
D	300 mil Ceramic DIP (D22-1)
10	Commercial only
12	Speed in Nanoseconds
15	
20	
25	

2953 drw 13

10

Integrated Device Technology, Inc.

BiCMOS STATIC RAM 64K (8K x 8-BIT) CACHE-TAG RAM

IDT71B74

FEATURES:

- High-speed address to MATCH comparison time
  - — Commercial: 8/10/12/15/20ns (max.)
- High-speed address access time
  - — Commercial: 8/10/12/15/20ns (max.)
- High-speed chip select access time
  - — Commercial: 6/7/8/10ns (max.)
- Power-ON Reset Capability
- Low power consumption
  - — 830mW (typ.) for 12ns parts
  - — 880mW (typ.) for 10ns parts
  - — 920mW (typ.) for 8ns parts
- Produced with advanced BiCMOS high-performance technology
- Input and output directly TTL-compatible
- Standard 28-pin plastic DIP and 28-pin SOJ (300 mil)

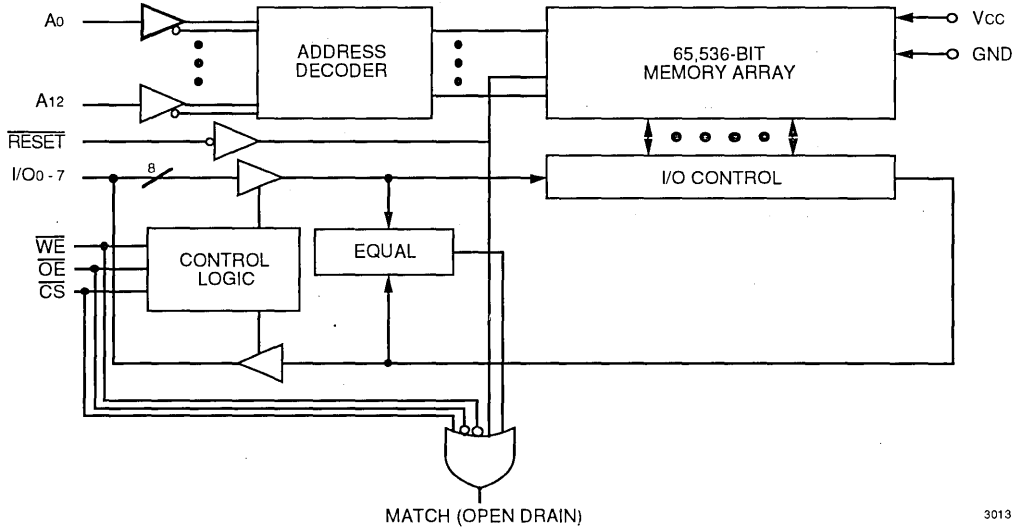
DESCRIPTION:

The IDT71B74 is a high-speed cache address comparator subsystem consisting of a 65,536-bit static RAM organized as 8K x 8 and an 8-bit comparator. A single IDT71B74 can map 8K cache words into a 2 megabyte address space by using the 21 bits of address organized with the 13 LSBs for the cache address bits and the 8 higher bits for cache data bits. Two IDT71B74s can be combined to provide 29 bits of address comparison, etc. The IDT71B74 also provides a single RAM clear control, which clears all words in the internal RAM to zero when activated. This allows the tag bits for all locations to be cleared at power-on or system-reset, a requirement for cache comparator systems. The IDT71B74 can also be used as a resettable 8K x 8 high-speed static RAM.

The IDT71B74 is fabricated using IDT's high-performance, high-reliability BiCMOS technology. Address access times as fast as 8ns, chip select times of 6ns and address-to-match times of 8ns are available.

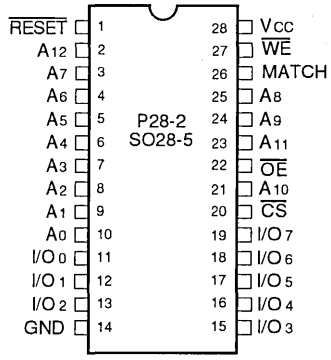
The MATCH pin of several IDT71B74s can be wired-ORed together to provide enabling or acknowledging signals to the data cache or processor, thus eliminating logic delays and increasing system throughput.

FUNCTIONAL BLOCK DIAGRAM



3013 drw 01

PIN CONFIGURATION



3013 drw 02

DIP/SOJ
TOP VIEW

TRUTH TABLE[1, 2]

WE	CS	OE	RESET	MATCH	I/O	Function
X	X	X	L	HIGH	—	Reset all bits to LOW
X	H	X	H	HIGH	Hi-Z	Deselect chip
H	L	H	H	LOW	DIN	No MATCH
H	L	H	H	HIGH	DIN	MATCH
H	L	L	H	HIGH	DOUT	Read
L	L	X	H	HIGH	DIN	Write

NOTES: 3013 tbl 01
1. H = VIH, L = VIL, X = DON'T CARE
2. HIGH = High-Z (pulled up by an external resistor), and LOW = VOL.

PIN DESCRIPTIONS

Pin Names	Description
A0–12	Address
I/O0-7	Data Input/Output
CS	Chip Select
RESET	Memory Reset
MATCH	Data/Memory Match (Open Drain)
WE	Write Enable
OE	Output Enable
GND	Ground
VCC	Power

3013 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Unit
VTERM[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	–55 to +125	°C
TSTG	Storage Temperature	–55 to +125	°C
PT	Power Dissipation	1.0	W
IOUT	DC Output Current	50	mA

NOTES: 3013 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed VCC + 0.5V.

CAPACITANCE

(TA = +25°C, f = 1.0MHz, SOJ Package)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	6	pF
COUT	Output Capacitance	VOUT = 3dV	7	pF

NOTE: 3013 tbl 04
1. This parameter is determined by device characterization, but is not production tested.

10

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input HIGH Voltage[1]	2.2	—	6.0[4]	V
V_{IHR}	$\overline{RESET}$ Input Voltage	2.5[2]	—	6.0	V
V_{IL}	Input LOW Voltage	–0.5[3]	—	0.8	V

3013 tbl 05

NOTES:
1. All inputs except $\overline{RESET}$.
2. When using bipolar devices to drive the $\overline{RESET}$ input, a pullup resistor of 1kΩ–10kΩ is usually required to assure this voltage.
3. V_{IL} (min.) = –1.5V for pulse width less than 10ns, once per cycle.
4. V_{TERM} must not exceed V_{CC} + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 10%

3013 tbl 06

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

Symbol	Parameter		71B74S8[3]	71B74S10	71B74S12	71B74S15	71B74S20	Unit
I_{CC}	Dynamic Operating Current	$\overline{WE}$ = V_{LC}	230	210	200	190	180	mA
	Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	$\overline{WE}$ = V_{HC}	210	200	170	160	150	mA

3013 tbl 07

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC}, only input addresses are cycling at f_{MAX}.
3. Preliminary data.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	IDT71B74S		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output LOW Voltage	I_{OL} = 18mA MATCH	—	0.4	V
		I_{OL} = 22mA MATCH	—	0.5	
		I_{OL} = 10mA, V_{CC} = Min. (Except MATCH)	—	0.5	
		I_{OL} = 8mA, V_{CC} = Min. (Except MATCH)	—	0.4	
V_{OH}	Output HIGH Voltage	I_{OH} = –4mA, V_{CC} = Min. (Except MATCH)	2.4	—	V

3013 tbl 08

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1, 2, and 3

3013 tbl 09

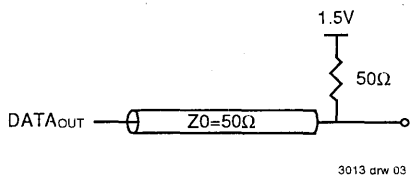


Figure 1. AC Test Load

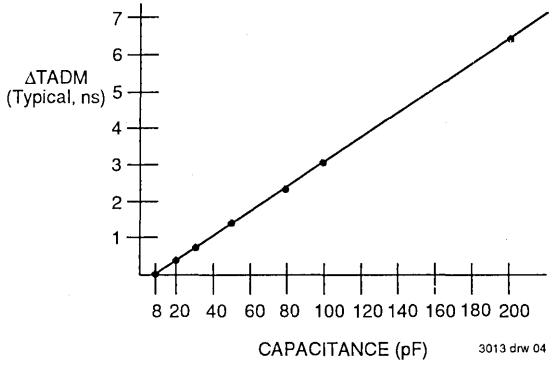
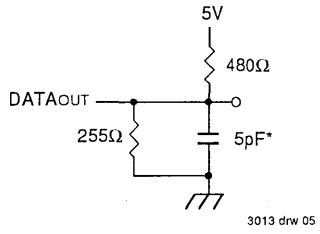


Figure 1A. Lumped Capacitive Load Typical Derating Curve



*Includes scope and jig.

Figure 2. AC Test Load (for tCLZ, tOLZ, tCHZ, tOHZ, tOW, tWHZ)

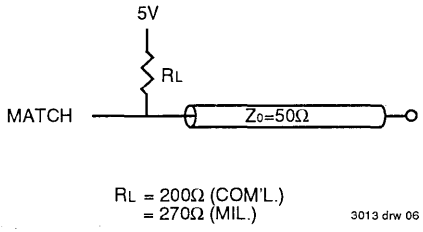


Figure 3. AC Test Load for MATCH

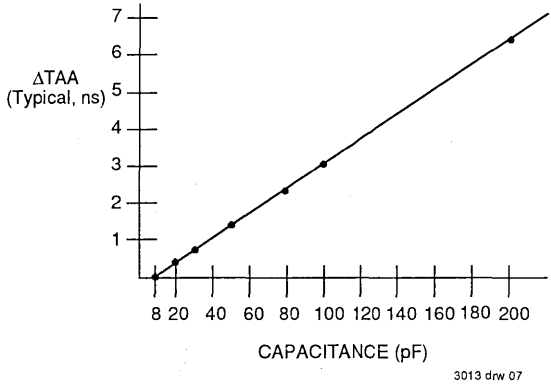
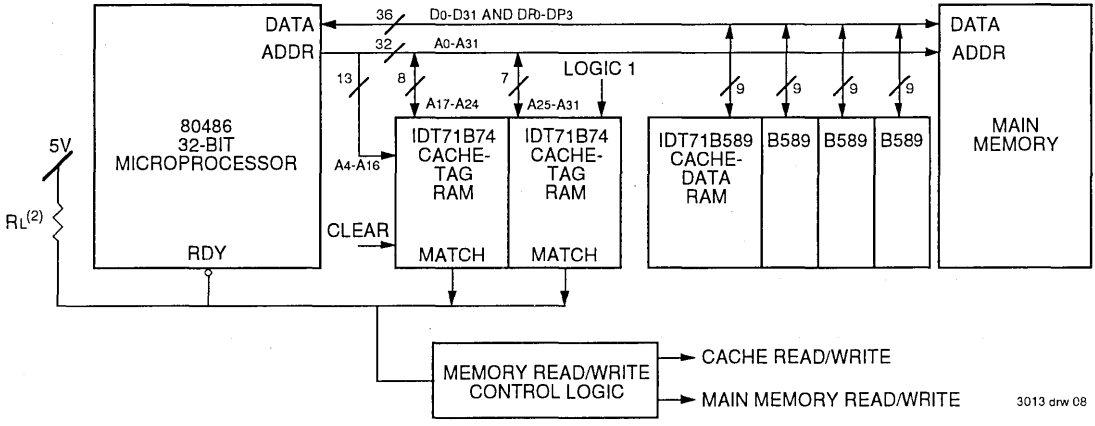


Figure 3A. Lumped Capacitive Load Typical Derating Curve



NOTES:
1. For more information refer to IDT Application Notes AN-07 and AN-78 and Technical Notes TN-11 and TN-13.
2. RL = 200Ω.

Figure 4. Example of Cache Memory System Block Diagram

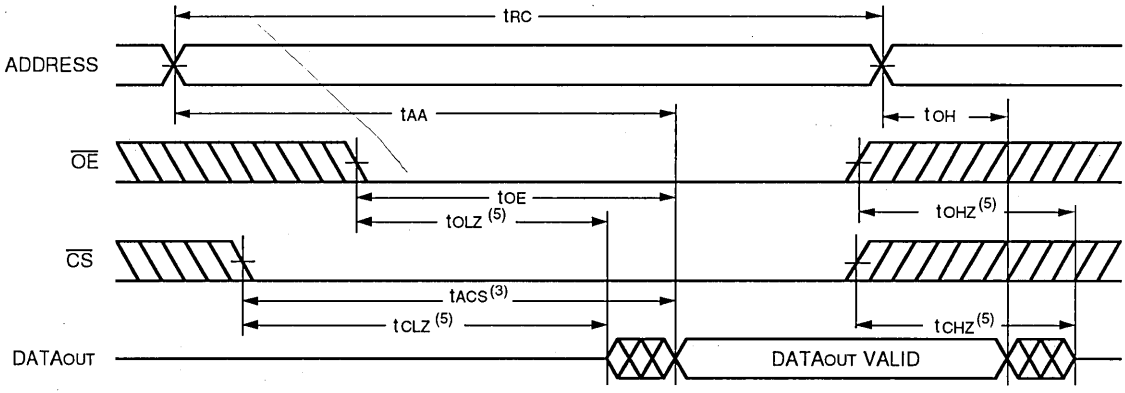
10

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%)

Symbol	Parameter	71B74S8[2] Min.	71B74S8[2] Max.	71B74S10 Min.	71B74S10 Max.	71B74S12 Min.	71B74S12 Max.	71B74S15 Min.	71B74S15 Max.	71B74S20 Min.	71B74S20 Max.	Unit
Read Cycle												
tRC	Read Cycle Time	8	—	10	—	12	—	15	—	20	—	ns
tAA	Address Access Time	—	8	—	10	—	12	—	15	—	20	ns
tACS	Chip Select Access Time	—	6	—	7	—	8	—	8	—	10	ns
tCLZ	Chip Select to Output in Low-Z[1]	2	—	2	—	2	—	3	—	3	—	ns
tOE	Output Enable to Output Valid	—	5	—	6	—	6	—	8	—	9	ns
tOLZ	Output Enable to Output in Low-Z[1]	2	—	2	—	2	—	2	—	2	—	ns
tCHZ	Chip Select to Output in High-Z[1]	—	4	—	5	—	5	—	7	—	8	ns
tOHZ	Output Disable to Output in High-Z[1]	—	4	—	4	—	5	—	5	—	8	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	ns

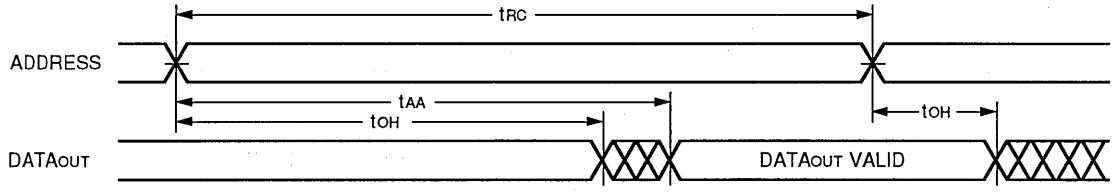
NOTES:
3013 tbl 10
1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.
2. Preliminary data.

TIMING WAVEFORM OF READ CYCLE NO. 1[1]



3013 drw 09

TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



3013 drw 10

NOTES:
1. $\overline{WE}$ is HIGH for read cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW; otherwise tAA is the limiting parameter.
4. $\overline{OE}$ is continuously active, $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%)

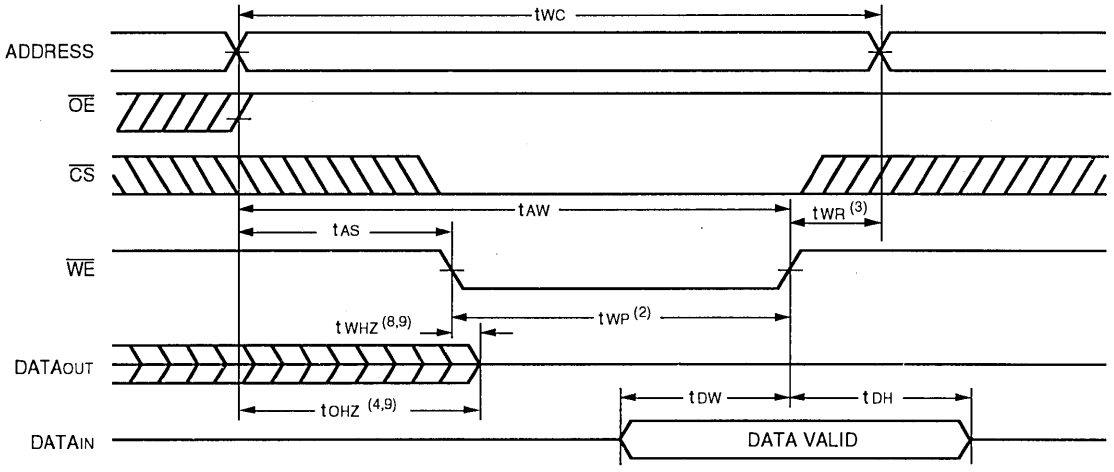
Symbol	Parameter	71B74S8[2]		71B74S10		71B74S12		71B74S15		71B74S20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle												
tWC	Write Cycle Time	8	—	10	—	12	—	15	—	20	—	ns
tCW	Chip Select to End of Write	7	—	8	—	9	—	10	—	15	—	ns
tAW	Address Valid to End of Write	7	—	8	—	9	—	10	—	15	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	7	—	8	—	9	—	10	—	15	—	ns
tWR	Write Recovery Time ($\overline{CS}$, $\overline{WE}$)	0	—	0	—	0	—	0	—	0	—	ns
tWHZ	Write Enable to Output in High-Z[1]	—	5	—	5	—	5	—	5	—	5	ns
tDW	Data Valid to End of Write	5	—	5	—	6	—	8	—	10	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	0	—	0	—	ns
tOW	Output Active from End of Write[1]	2	—	2	—	2	—	2	—	2	—	ns

3013 tbl 11

NOTES:
1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.
2. Preliminary data.

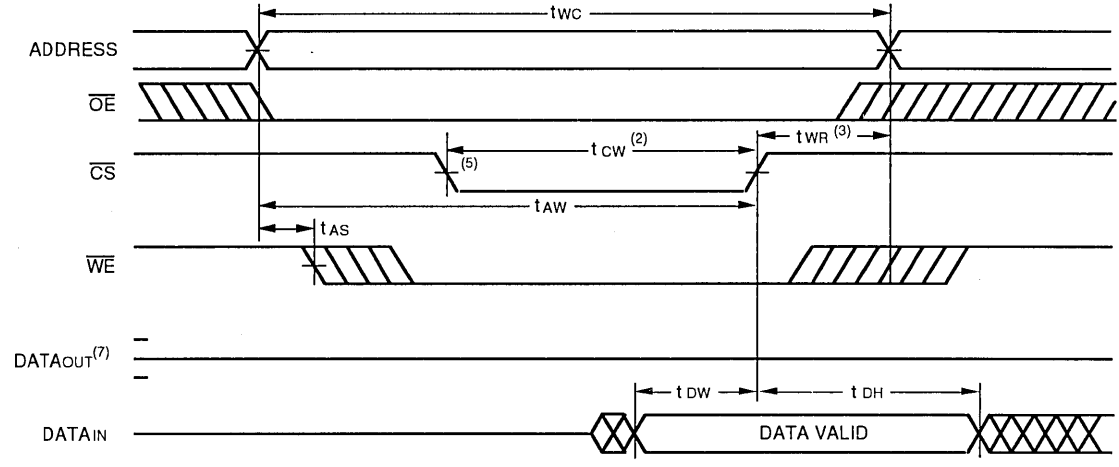
10

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled Timing, $\overline{OE}$ HIGH During Write)(1, 6)



3013 drw 11

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ Controlled Timing)(1, 6)



3013 drw 12

NOTES:
1. $\overline{WE}$, $\overline{CS}$ must be inactive during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{WE}$ and a LOW $\overline{CS}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. $\overline{OE}$ is continuously HIGH, $\overline{OE} \geq V_{IH}$. If during the $\overline{WE}$ controlled write cycle the $\overline{OE}$ is LOW, tWP must be greater or equal to tWHZ + tDW to allow the I/O drivers to turn off and the data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during the $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified tWP. For a $\overline{CS}$ controlled write cycle, $\overline{OE}$ may be LOW with no degradation to tCW timing.
7. DATAOUT is never enabled, therefore the output is in High-Z state during the entire write cycle.
8. tWHZ is not included if $\overline{OE}$ remains HIGH during the write cycle. If $\overline{OE}$ is LOW during the Write Enabled write cycle then tWHZ must be added to tWP and tCW.
9. Transition is measured ±200mV from steady state.

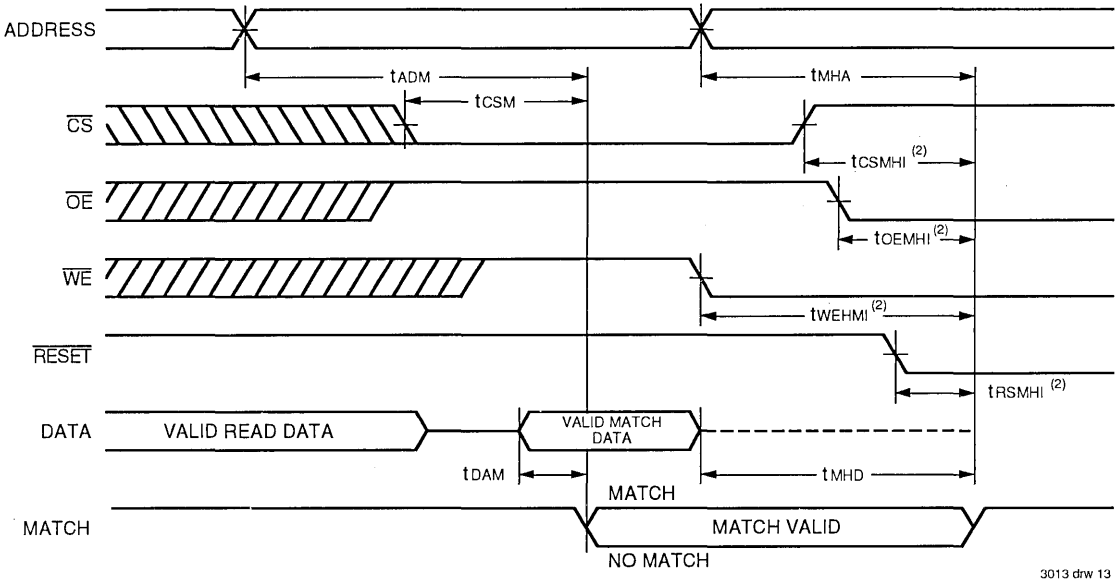
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%)

Symbol	Parameter	71B74S8[2] Min.	71B74S8[2] Max.	71B74S10 Min.	71B74S10 Max.	71B74S12 Min.	71B74S12 Max.	71B74S15 Min.	71B74S15 Max.	71B74S20 Min.	71B74S20 Max.	Unit
Match Cycle												
tADM	Address to MATCH Valid	—	8	—	10	—	12	—	15	—	20	ns
tCSM	Chip Select to MATCH Valid	—	7	—	7	—	8	—	10	—	10	ns
tCSMHI	Chip Select to MATCH HIGH[1]	—	7	—	8	—	8	—	8	—	8	ns
tDAM	Data Input to MATCH Valid	—	7	—	8	—	10	—	12	—	12	ns
tOEMHI	$\overline{OE}$ LOW to MATCH HIGH[1]	—	7	—	8	—	10	—	10	—	10	ns
tWEMHI	$\overline{WE}$ LOW to MATCH HIGH[1]	—	7	—	8	—	10	—	10	—	10	ns
tRSMHI	$\overline{RESET}$ LOW to MATCH HIGH[1]	—	8	—	10	—	10	—	12	—	15	ns
tMHA	MATCH Valid Hold From Address	2	—	2	—	2	—	2	—	2	—	ns
tMHD	MATCH Valid Hold From Data	2	—	2	—	2	—	2	—	2	—	ns

NOTES:
1. This parameter is guaranteed with the AC Load (Figure 3) by device characterization, but is not production tested.
2. Preliminary data.

3001 tbl 12

MATCH TIMING[1]



3013 drw 13

NOTES:
1. It is not recommended to float data and address input pins while the MATCH pin is active.
2. Transition is measured at ±200mV from steady state.

10

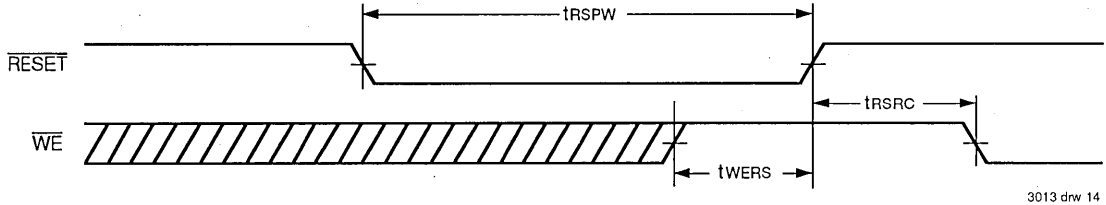
AC ELECTRICAL CHARACTERISTICS (VCC = 5.0V ± 10%)

Symbol	Parameter	71B74S8[3]		71B74S10		71B74S12		71B74S15		71B74S20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
tRSPW	Reset Pulse Width[1]	30	—	35	—	35	—	40	—	45	—	ns
tWERS	$\overline{WE}$ HIGH to Reset HIGH	5	—	5	—	5	—	5	—	5	—	ns
tRSRC	Reset HIGH to $\overline{WE}$ LOW	25	—	25	—	25	—	30	—	30	—	ns
tPORS	Power On Reset[2]	100	—	100	—	100	—	120	—	120	—	ns

3001 tbl 13

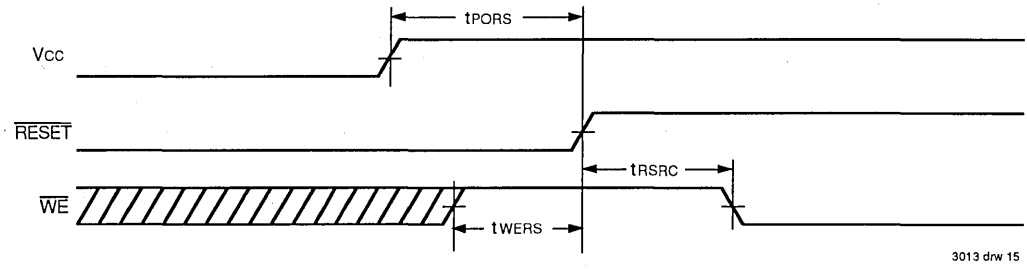
NOTES:
1. Recommended duty cycle = 10% maximum.
2. This parameter is guaranteed with the AC Load (Figure 1) by device characterization, but is not production tested.
3. Preliminary data.

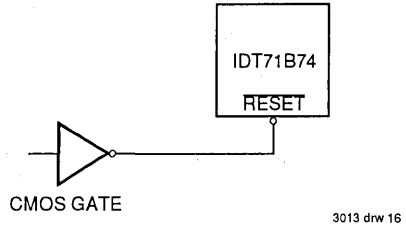
RESET TIMING



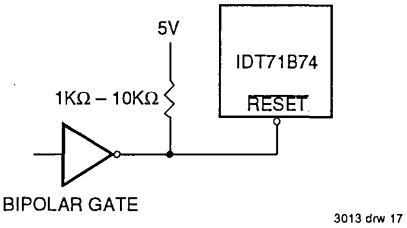
3013 drw 14

POWER ON RESET TIMING





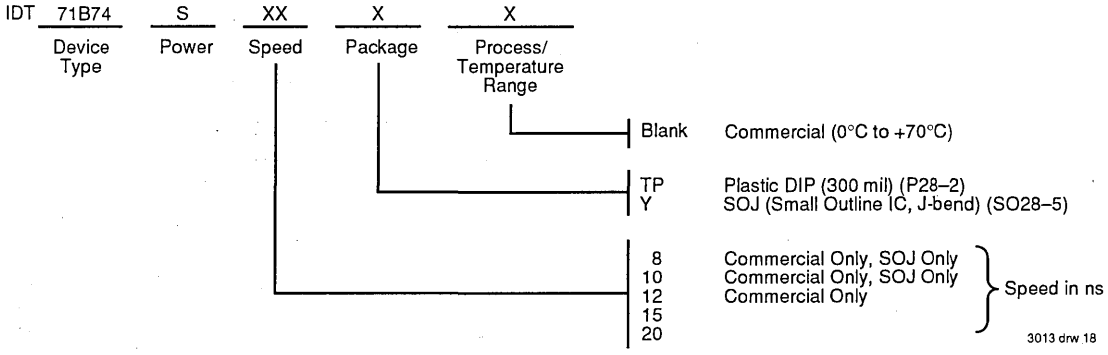
Driving the $\overline{\text{RESET}}$ pin with CMOS logic.



Driving the $\overline{\text{RESET}}$ pin with bipolar logic.

Figure 5.

ORDERING INFORMATION



10

Integrated Device Technology, Inc.

VERY LOW POWER CMOS SRAM FOR NOTEBOOK/LAPTOP CACHE 256K (32K x 8-BIT)

IDT71256SL
IDT71256L

FEATURES:

- Optimized for 16/32bit notebook/laptop cache at 20 and 25MHz
- Very-low standby current (maximums):
  - — 3.0mA standby
  - — 0.4mA full standby (L)
  - — 1.0mA full standby (SL)
- Fast access times:
  - — 25/35ns
- Battery-backup operation: 2V data retention
  - — 120uA data retention current (max.)
- Small package for space-efficient layouts:
  - — 28-pin 300 mil SOJ
- Ideal configuration for large cache sizes, with minimum space and minimum power:
  - — 32K x 8
- Produced with advanced high-performance CMOS technology
- Static operation: no clocks or refresh required
- Input and output are TTL-compatible
- Single 5V(+/-10%) power supply

DESCRIPTION:

The IDT71256SL/L is a 262,144-bit high-speed static RAM organized as 32K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology.

Both versions (SL and L) have outstanding low power characteristics, but differ slightly in dynamic and full standby currents, giving the designer flexibility to choose the one that fits his application better.

Address access times of 25, and 35ns are ideal for 16 and 32-bit notebook and laptop cache designs running at 20 and 25MHz. For instance, two of these SRAMs interface directly to many 386 notebook cache controllers to form a 64kB cache.

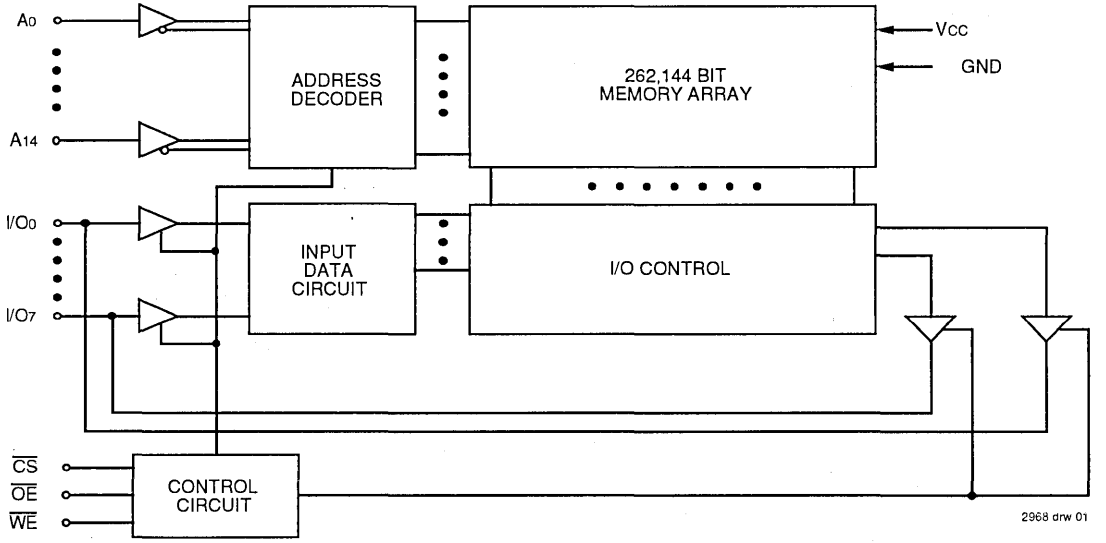
When the power management logic puts these SRAMs in standby mode, their very low power characteristics contribute to extended battery life.

When $\overline{CS}$ goes high, the SRAM will automatically go to a low power standby mode and will remain in standby as long as $\overline{CS}$ remains high. Furthermore, under full standby mode ($\overline{CS}$ at CMOS level, f=0), power consumption is guaranteed to always be less than 2mW (L version) and typically will be much smaller.

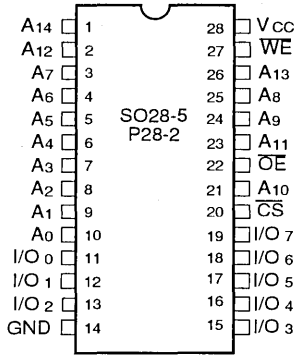
These SRAMs also offer battery-backup data retention at as little as 2 volts. Under this condition, power consumption is guaranteed not to exceed 0.6mW and typically will be much smaller.

The package chosen for this device, 28-pin 300mil SOJ, helps the designer attain the stringent space goals typical of notebook and laptop designs.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



2968 drw 02

SOJ/DIP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2968 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

PIN DESCRIPTIONS

Name	Description
A_0–A_{14}	Addresses
I/O0–I/O7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
V_{CC}	Power

2968 tbl 01

TRUTH TABLE(1)

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	I/O	Function
X	H	X	High-Z	Standby (I_{SB})
X	V_{HC}	X	High-Z	Standby (I_{SB1})
H	L	H	High-Z	Output Disable
H	L	L	D_{OUT}	Read
L	L	X	D_{IN}	Write

NOTE: 2968 tbl 02

1. H = V_{IH}, L = V_{IL}, X = Don't Care

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE: 2968 tbl 04

1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2968 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5	—	0.8	V

NOTE: 2968 tbl 06

1. V_{IL} (min.) = –3.0V for pulse width less than 20ns, once per cycle.

10

DC ELECTRICAL CHARACTERISTICS(1, 2)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	71256SL25 71256L25 Com'l.	71256SL35 71256L35 Com'l.	Unit
I_{CC}	Dynamic Operating Current, $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	SL	120	110	mA
		L	115	105	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}(2)	SL	3	3	mA
		L	3	3	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, V_{CC} = Max., f = 0	SL	1	1	mA
		L	0.4	0.4	

NOTES:

2968 tbl 07

1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC}, all address inputs cycling at f_{MAX}; f = 0 means that the address pins are not cycling.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2968 tbl 08

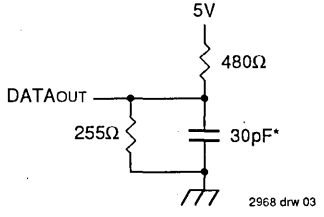


Figure 1. AC Test Load

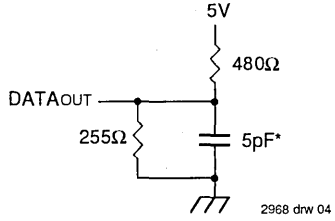


Figure 2. AC Test Load (for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

*Includes scope and jig capacitances

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT71256SL Min.	IDT71256SL Typ.	IDT71256SL Max.	IDT71256L Min.	IDT71256L Typ.	IDT71256L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	COM'L.	—	—	2	—	—	2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	COM'L.	—	—	2	—	—	2	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.			—	0.4	—	—	0.4	V
		I_{OL} = 10mA, V_{CC} = Min.		—	—	0.5	—	—	0.5	
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.		2.4	—	—	2.4	—	—	V

2968 tbl 09

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L,SL Versions) V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V

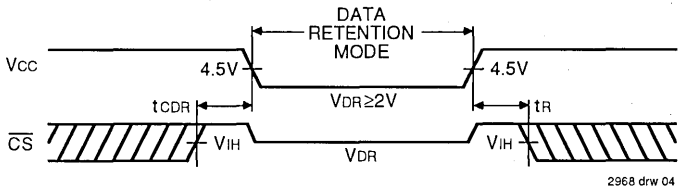
Symbol	Parameter	Test Condition		Min.	Typ.[1] Vcc @ 2.0v	Typ.[1] Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	Vcc for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$	COM'L.	—	—	—	120	200	µA
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	—	—	ns

NOTES:

2968 tbl 10

1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

LOW Vcc DATA RETENTION WAVEFORM



2968 drw 04

10

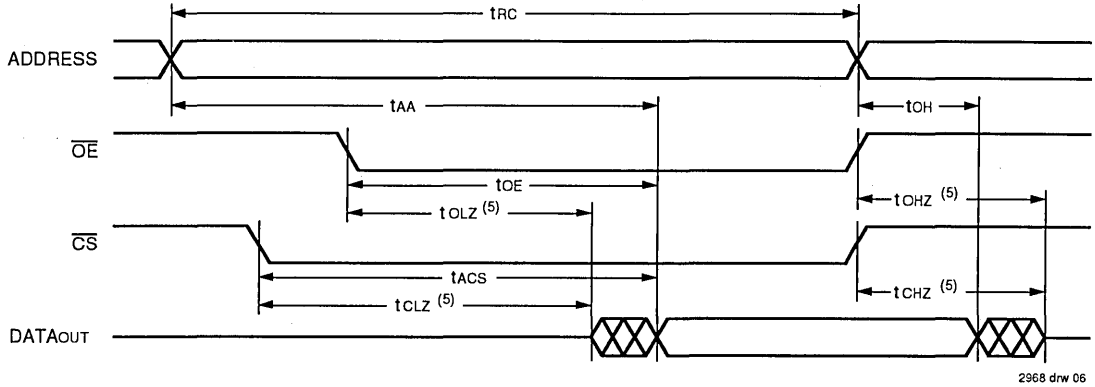
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71256SL25 71256L25		71256SL35 71256L35		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	25	—	35	—	ns
t_{AA}	Address Access Time	—	25	—	35	ns
t_{ACS}	Chip Select Access Time	—	25	—	35	ns
t_{CLZ}	Chip Select to Output in Low Z[1]	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	11	—	15	ns
t_{OLZ}	Output Enable to Output in Low Z[1]	2	—	2	—	ns
t_{CHZ}	Chip Select to Output in High Z[1]	—	11	—	15	ns
t_{OHZ}	Output Disable to Output in High Z[1]	2	10	2	15	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	ns
Write Cycle						
t_{WC}	Write Cycle Time	25	—	35	—	ns
t_{CW}	Chip Select to End of Write	20	—	30	—	ns
t_{AW}	Address Valid to End of Write	20	—	30	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	30	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{WHZ}	Write Enable to Output in High Z[1]	—	11	—	15	ns
t_{DW}	Data to Write Time Overlap	13	—	15	—	ns
t_{DH1}	Data Hold from Write Time ($\overline{WE}$)	0	—	0	—	ns
t_{DH2}	Data Hold from Write Time ($\overline{CS}$)	3	—	3	—	ns
t_{OW}	Output Active from End of Write[1]	5	—	5	—	ns

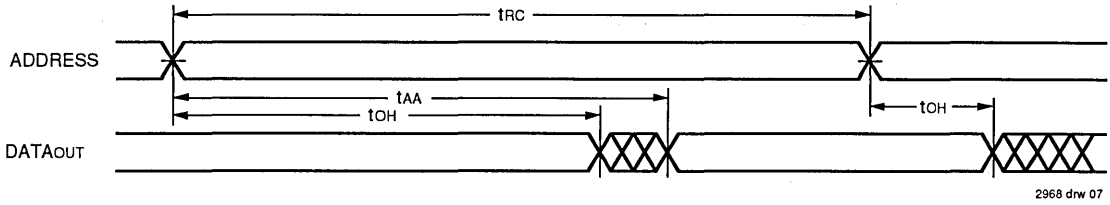
NOTE:
1. This parameter guaranteed with the AC test load (Figure 2) by device characterization, but is not production tested.

2968 tbl 11

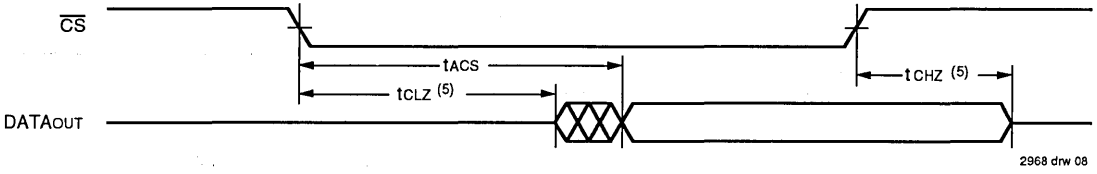
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



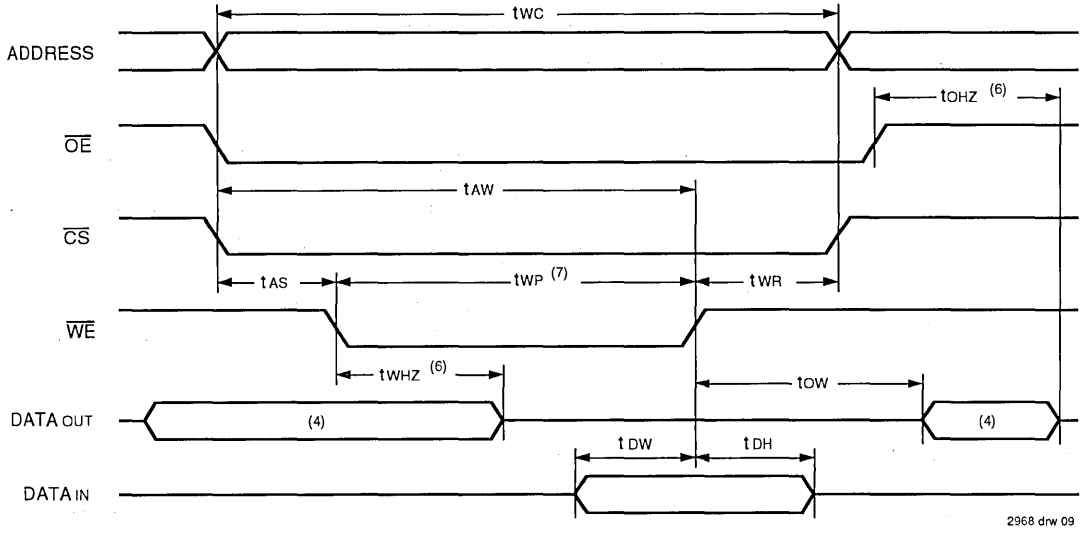
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



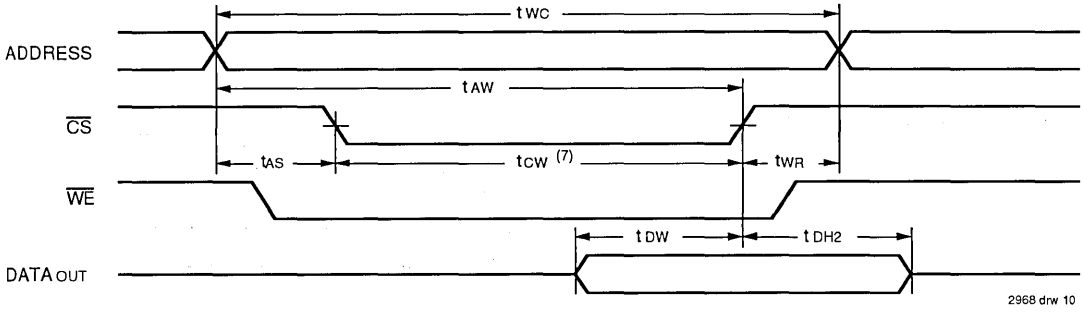
NOTES:
1. $\overline{WE}$ is HIGH for read cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state.

10

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 5)



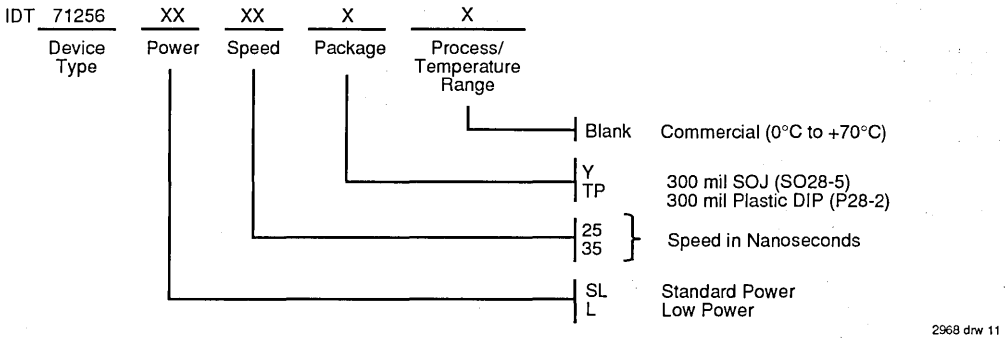
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tCW or tWP) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state.
7. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP. For a $\overline{CS}$ controlled write cycle, $\overline{OE}$ may be LOW with no degradation to tCW.

ORDERING INFORMATION



10

Integrated Device Technology, Inc.

CMOS CacheRAM™ 32K x 9-BIT (288K-BIT) BURST COUNTER & SELF-TIMED WRITE

IDT71589SA

FEATURES:

- High density 32K x 9 architecture
- Internal write registers (address, data, and control)
- Self-timed write cycle
- Internal burst read and write address counter
- Clock to data times: 19, 24, and 34ns
- Chip select for depth expansion
- Complies with all timing and signals of 80486 processors up to 40MHz
- I/O pins directly TTL-compatible
- Packaged in plastic 300 mil 32-pin SOJ
- BiCMOS version available for 50MHz and 67MHz systems (IDT71B589)
- SIMM module versions also available from IDT in 128KB (IDT7MP6085 and IDT7MP6086) and 256KB (IDT7MP6087) densities, plus parity

DESCRIPTION:

The IDT71589 is a very high-speed 32K x 9-bit static RAM with full on-chip hardware support of the 80486 CPU interface. This part is designed to facilitate the implementation of the highest-performance secondary caches for the 486 architecture while using low-speed cache-tag RAMs and PALs and consuming the minimum possible board space.

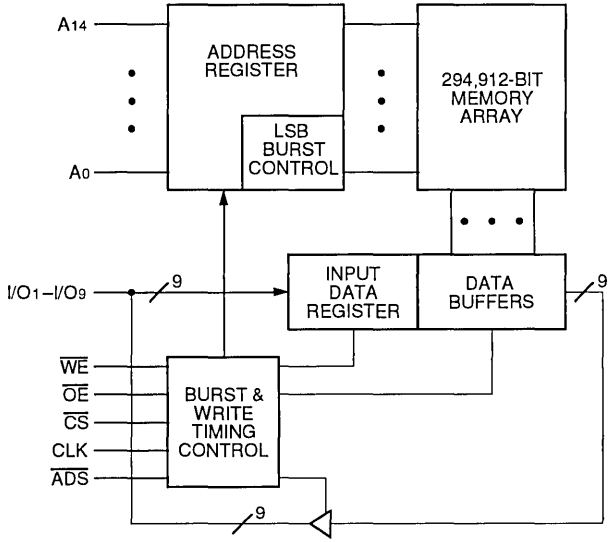
The IDT71589 CacheRAM contains a full set of write data and address registers. Internal logic allows the processor to generate a self-timed write based upon a decision which can be left until the extreme end of the write cycle.

An internal burst address counter accepts the first cycle address from the processor, then cycles through the adjacent four locations using the 486's burst refill sequence on appropriate rising edges of the system clock.

Fabricated using IDT's CMOS high-performance sub-micron technology, this device operates at a very low power consumption and offers a maximum clock to data access time as fast as 19ns.

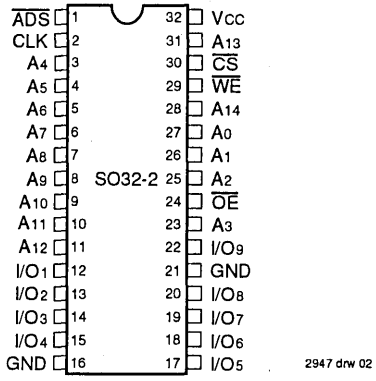
The IDT71589SA CacheRAMs are packaged in a 32-pin small-outline J-bend (SOJ) package, which allows for a 128KB (plus parity) secondary cache to be built in approximately 1.20 square inches.

FUNCTIONAL BLOCK DIAGRAM



2947 drw 01

PIN CONFIGURATION



SOJ
TOP VIEW

PIN NAMES

A_0–A_{14}	Address Inputs
I/O_1–I/O_9	Data Input/Output
$\overline{CS}$	Chip Select/Count Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{ADS}$	Address Status
CLK	System Clock
GND	Ground
Vcc	Power

2947 tbl 01

SPEED SELECTION

80486 Speed	Suggested IDT71589
25MHz	IDT71589SA35
33MHz	IDT71589SA25
40MHz	IDT71589SA20
50MHz	IDT71B589S14[1, 2]
50MHz	IDT71B589S12[1, 2]
67MHz	IDT71B589S10[1, 3]

NOTES: 2947 tbl 02
1. Separate data sheet available for BiCMOS version.
2. Either part may be used, depending on system loads.
3. Intended for the P5 or future faster versions of the 80486.

COUNT SEQUENCE[1] (A_0, A_1 ONLY)

Start	+1	+2	+3
0	1	2	3
1	0	3	2
2	3	0	1
3	2	1	0

NOTE: 2947 tbl 03
1. The counter wraps around to its starting value and repeats the same sequence after the last count.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	–0 to +70	°C
T_{BIAS}	Temperature Under Bias	–65 to +135	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.5	W
I_{OUT}	DC Output Current	50	mA

NOTE: 2947 tbl 04
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 5%

2947 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0.0	V
V_{IH}	Input High Votage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 2947 tbl 06
1. V_{IL} (min.) = –1.5V for pulse width of less than 10ns, once per cycle.

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DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 5%)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.25V, V_{IN} = 0V to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}, V_{CC} = Max.	—	10	µA
V_{OL}	Output Low Voltage (I/O_1–I/O_9)	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

2947 tbl 07

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 5%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

Symbol	Parameter	Test Condition	71589SA20[3]		71589SA25		71589SA35		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0[2]	130	—	130	—	130	—	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	240	—	220	—	200	—	mA

NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX}, address inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines are changing.

2947 tbl 08

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2947 tbl 09

CAPACITANCE

(T_A = +25°C, f = 1.0 MHz, SOJ package only)

Symbol	Parameter[1]	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
$C_{I/O}$	Input/Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

2947 tbl 10

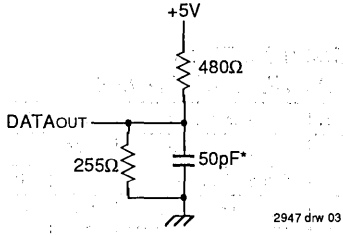


Figure 1. Output Load

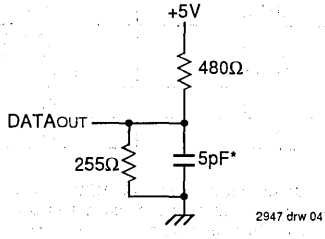


Figure 2. Output Load (for t_{OHZ}, t_{CHZ}, t_{OLZ} and t_{CLZ})

*including scope and jig

FUNCTIONAL DESCRIPTION

The IDT71589 is a very fast 32K x 9 CMOS static CacheRAM with internal edge-triggered registers dedicated to the support of the 486 CPU. These registers support the fastest systems and allow a 128KB or larger cache to be designed to consume the smallest number of chips, the lowest power and board space, and allow the designer to avoid the use of expensive high-speed cache-tag RAMs and PALs.

The internal registers are designed to support two high-speed functions: Burst read cycles, and a late-abort self-timed write cycle.

Burst read cycles are accomplished through the assertion of the $\overline{ADS}$ signal with a valid address input during the rising edge of the clock input. This address will be used to access the data in the CacheRAM during the next clock cycle, and data will be output during the following three cycles in accordance with the 486's burst refill sequence (i.e., during the next cycle the address' LSB is inverted, then the second LSB is inverted as the LSB is restored to its original value, etc.). Since the CacheRAM contains this counter internally, the critical clock-to-data time of even the fastest CPU speeds can be met by using a slower RAM speed grade without resorting to chip-intensive interleaving schemes. Should the $\overline{ADS}$ signal be sampled as valid after having been sampled as invalid, any bursting in process will be reinitialized to the new address, and a new burst cycle will be started. The burst counter wraps around at the end of the sequence and continues to count until stopped by the $\overline{ADS}$ or $\overline{CS}$ inputs. A fast copy-back scheme can harness this capability by reading, then writing the four burst addresses within a single burst cycle.

The self-timed write cycle significantly eases the timing of the address and data inputs during a write cycle, and allows the write/don't write decision to be postponed until the very end of the second cycle of a write cycle. During a write cycle, the address will be strobed into the address register during the first rising edge of the clock after the $\overline{ADS}$ input becomes valid. Data is sampled into the data input register during the next cycle's rising edge, as is the write enable input. If a write has been enabled the data will be written from the address and input data registers into the CacheRAM during the high phase of the clock of that cycle.

A chip select pin is provided to give control over interruption of write cycles and burst read cycles. When the $\overline{CS}$ input is used to interrupt a burst cycle, it operates as a synchronous input to the burst counter. A low level must be present on the chip select input and must satisfy data set-up and hold times in order for the counter to progress to its next state. To stop the counter at its current state, the chip select input must be taken high, and must stay high long enough to satisfy the CacheRAM's data set-up and hold times. The $\overline{CS}$ pin also is used as an auxiliary to the $\overline{WE}$ input. Writes can only be accomplished if both $\overline{CS}$ and $\overline{WE}$ are simultaneously sampled active.

The SOJ package allows for very effective space utilization as illustrated by the IDT Cache-SIMMs. The IDT7MP6086 offers 128KB in a 72-pin SIMM and the IDT7MP6085/7 offer 128KB/256KB in an 80-pin SIMM.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 5%, All Temperature Ranges)

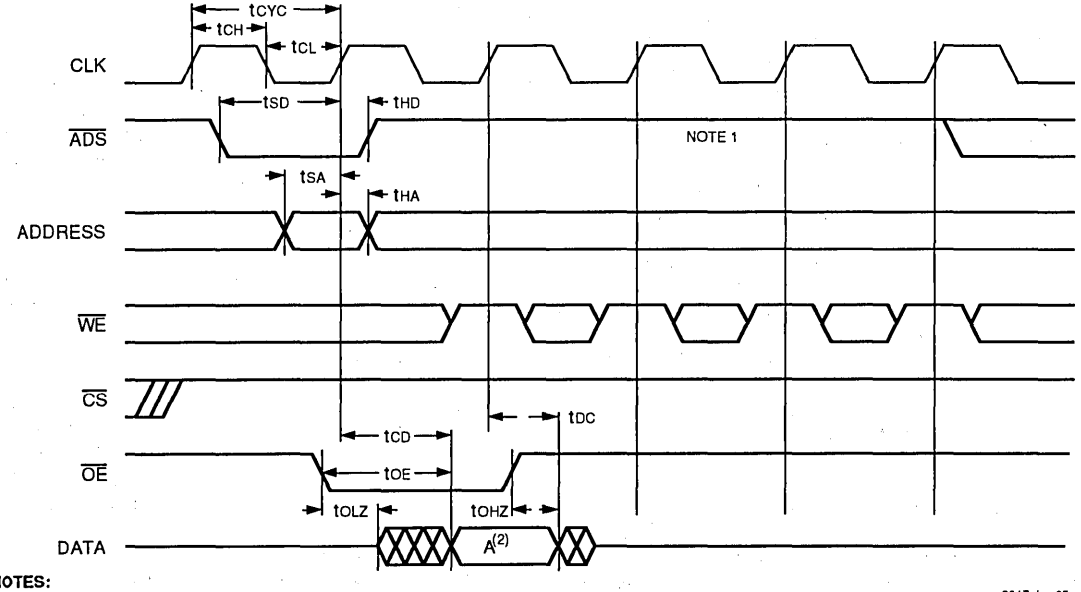
Symbol	Parameter	71589SA20		71589SA25		71589SA35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tCYC	Clock Cycle Time	25	—	30	—	40	—	ns
tCH	Clock Pulse High[1]	10	—	11	—	14	—	ns
tCL	Clock Pulse Low[1]	10	—	11	—	14	—	ns
tSD	Set-up Time ($\overline{ADS}$, $\overline{WE}$, $\overline{CS}$, Input Data)	3	—	4	—	5	—	ns
tHD	Hold Time ($\overline{ADS}$, $\overline{WE}$, $\overline{CS}$, Input Data)	2	—	2	—	2	—	ns
tSA	Address Set-up Time	3	—	4	—	5	—	ns
tHA	Address Hold Time	2	—	2	—	2	—	ns
tCD	Clock to Data Valid	—	19	—	24	—	34	ns
tDC	Data Valid After Clock	4	—	4	—	5	—	ns
tOE	Output Enable to Output Valid	—	8	—	9	—	10	ns
tOLZ	Output Enable to Output in Low-Z[2,3]	2	—	2	—	2	—	ns
tOHZ	Output Disable to Output in High-Z[2,3]	—	8	—	9	—	10	ns

NOTES:
1. This parameter is measured as a HIGH time above 2.2V and LOW time below 0.8V.
2. Transition is measured ±200mV from steady state.
3. This parameter is guaranteed with the AC load (Figure 2), but is not production tested.

2947 tbl 11

10

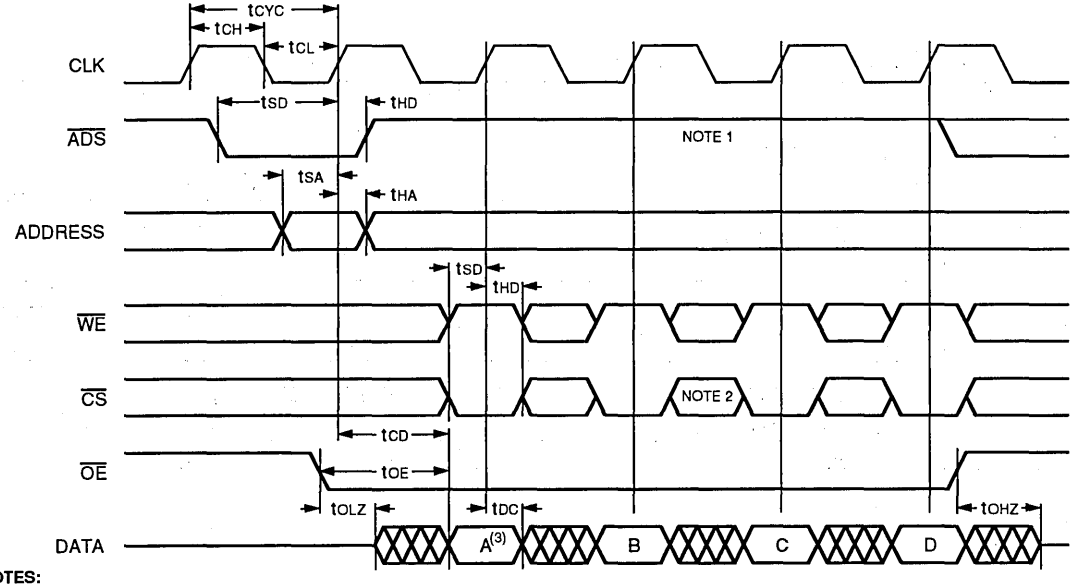
TIMING WAVEFORM OF READ CYCLE



NOTES:
1. If $\overline{ADS}$ goes LOW during a burst cycle, a new address will be loaded and another burst cycle will be started.
2. A-Data from address, counter is not imcremented to the next addresses. If $\overline{CS}$ is taken inactive during a burst read cycle, the burst counter will discontinue counting until $\overline{CS}$ input again goes active. The timing of the $\overline{CS}$ input for this control of the burst counter must satisfy setup and hold parameters t_{SD} and t_{HD}. The output remains unchanged as long as the $\overline{CS}$ is inactive to advance the counter and as long as the $\overline{OE}$ reamins active.

2947 drw 05

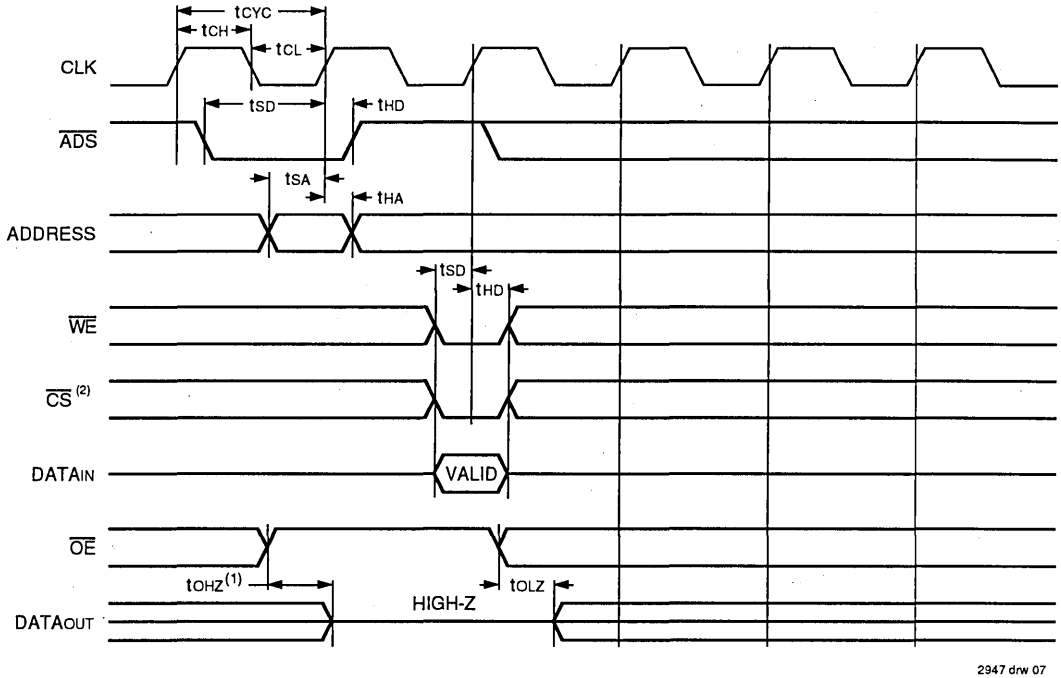
TIMING WAVEFORM OF BURST READ CYCLE



NOTES:
1. If $\overline{ADS}$ goes LOW during a burst cycle, a new address will be loaded and another burst cycle will be started.
2. If $\overline{CS}$ is taken inactive during a burst read cycle, the burst counter will discontinue counting until $\overline{CS}$ input again goes active. The timing of the $\overline{CS}$ input for this control of the burst counter must satisfy setup and hold parameters t_{SD} and t_{HD}.
3. A-Data from input address. B-Data from input address except A_0 is now $\overline{A}_0$. C-Data from input address except A_1 is now $\overline{A}_1$. D-Data from input address except A_0 and A_1 are now $\overline{A}_0$ and $\overline{A}_1$.

2947 drw 06

TIMING WAVEFORM OF WRITE CYCLE

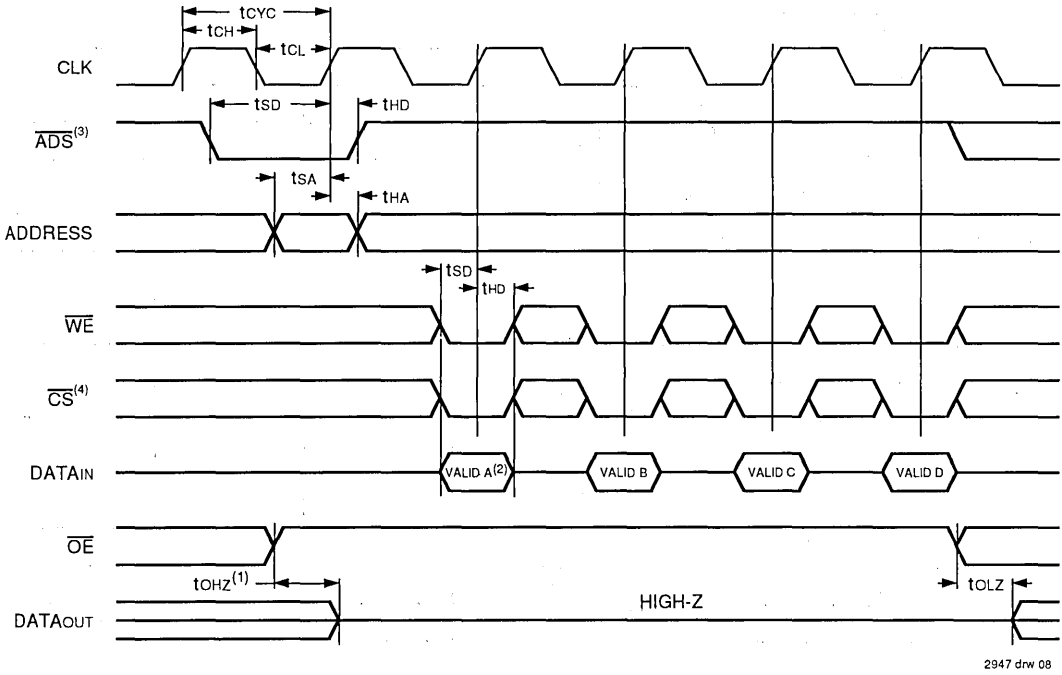


2947 drw 07

NOTES:
1. $\overline{OE}$ must be taken inactive at least as long as $t_{OHZ} + t_{SA}$ before the second rising clock edge of write cycle.
2. $\overline{CS}$ timing is the same as any synchronous signal when used to block writes or to stop the burst count sequence.

10

TIMING WAVEFORM OF BURST WRITE CYCLE



NOTES:

1. $\overline{OE}$ must be taken inactive at least as long as $t_{OHZ} + t_{SA}$ before the second rising clock edge of write cycle.
2. A-Data to be written to original input address. B-Data to be written to original input address except A_0 is now $\overline{A}_0$. C-Data to be written to original input address except A_1 is now $\overline{A}_1$. D-Data to be written to original input address except A_0 and A_1 are now $\overline{A}_0$ and $\overline{A}_1$.
3. If $\overline{ADS}$ goes low during a burst cycle, a new address will be loaded, and another burst cycle will be started.
4. If $\overline{CS}$ is taken inactive during a burst write cycle the burst counter will discontinue counting until the $\overline{CS}$ input again goes active. The timing of the $\overline{CS}$ input for this control of the burst counter must satisfy setup and hold parameters t_{SD} and t_{HD}. $\overline{CS}$ timing is the same as any synchronous signal when used to block writes or to stop the burst count sequence.

TRUTH TABLE

CLK	Previous $\overline{ADS}$	$\overline{ADS}$	Address	$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	I/O	Function
↑	H	L	Valid Input	X	X	—	—	Preset Address Counter
↑	X	H	—	—	—	—	—	Ignore External Address Pins
↑	L	X	—	—	—	—	—	Ignore External Address Pins
↑	X	H	—	—	L	—	—	Sequence Address Counter
↑	L	X	—	—	L	—	—	Sequence Address Counter
↑	X	H	—	—	H	—	—	Suspend Address Sequencing
↑	L	X	—	—	H	—	—	Suspend Address Sequencing
—	—	—	—	—	—	H	High-Z	Outputs Disabled
—	—	—	—	H	—	L	$DATA_{OUT}$	Read
↑	X	H	—	L	L	H	$DATA_{IN}$	Write
↑	L	X	—	L	L	H	$DATA_{IN}$	Write
—	—	—	—	L	L	L	—	Not Allowed

NOTE:
H = HIGH
L = LOW
X = Don't Care
– = Unrelated
High-Z = High Impedance

2947 tbl 12

ORDERING INFORMATION

IDT 71589 (Device Type) SA (Power) XX (Speed) Y (Package) X (Process/Temperature Range)

- Process/Temperature Range
  - Blank — Commercial (0°C to +70°C)
- Package
  - Y — Plastic J-Bend Small Outline IC (SO32-2)
- Speed
  - 20 — Commercial Only
  - 25 — Commercial Only
  - 35 — Commercial Only

} Speed indicator

2947 drw 09

10

Integrated Device Technology, Inc.

BiCMOS CacheRAM™ 32K x 9-BIT (288K-BIT) BURST COUNTER & SELF-TIMED WRITE

PRELIMINARY
IDT71B589S

FEATURES:

- 32K x 9 architecture
- Internal write registers (address, data, and control)
- Self-timed write cycle
- Internal burst read and write address counter
- Clock to data times: 10.5, 12, 14ns
- Small address set-up: 1ns
- Chip select for depth expansion
- I/O pins TTL-compatible
- Complies with all timing and signals of 80486 processors up to 50MHz and P5 processors up to 67MHz
- Packaged in plastic 300 mil 32-pin SOJ
- CMOS version available for 40MHz systems and below (IDT71589SA)

DESCRIPTION:

The IDT71B589 is a very high-speed 32K x 9-bit static RAM with full on-chip hardware support of the 80486 and P5 CPU interfaces. This part is designed to facilitate the implementation of the highest-performance secondary caches for the 486 and P5 architectures while using available cache-tag RAMs and PALs, and consuming the minimum possible board space.

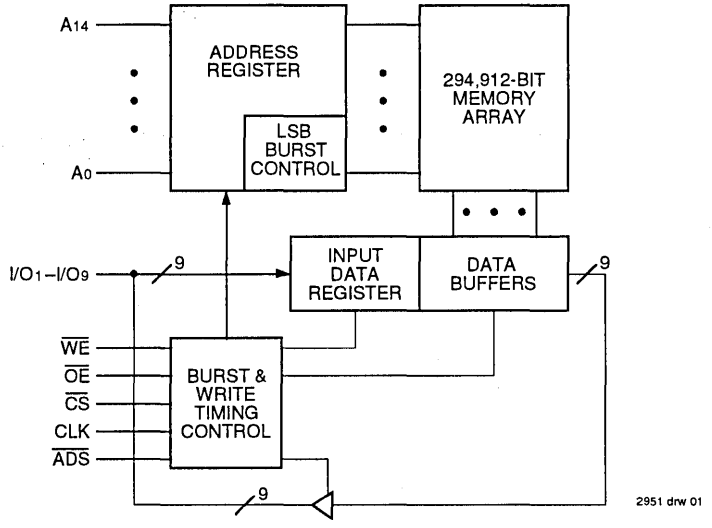
The IDT71B589 CacheRAM contains a full set of write data and address registers. Internal logic allows the processor to generate a self-timed write based upon a decision which can be left until the extreme end of the write cycle.

An internal burst address counter accepts the first cycle address from the processor, then cycles through the adjacent four locations using the 486's and P5's burst refill sequence on appropriate rising edges of the system clock.

Fabricated using IDT's BiCMOS high-performance submicron technology, this device operates at a very low power consumption and offers a maximum clock to data access time as fast as 10.5ns, while providing an address setup of only 0.5ns.

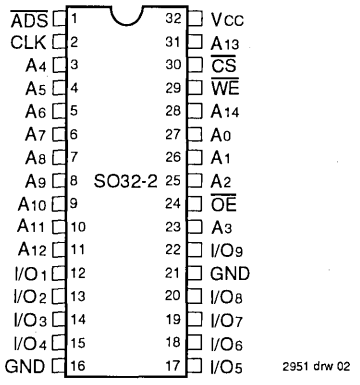
The IDT71B589 CacheRAMs are packaged in a 32-pin small-outline J-bend (SOJ) package, which allows for a 128KB and 256KB (plus parity) secondary caches to be built in only 1.20 and 2.45 square inches, respectively.

FUNCTIONAL BLOCK DIAGRAM



The IDT logo is a registered trademark and CacheRAM is a trademark of Integrated Device Technology, Inc.
Intel and i486 are trademarks of Intel Corp.

PIN CONFIGURATION



SOJ
TOP VIEW

PIN NAMES

A_0–A_{14}	Address Inputs
I/O_1–I/O_9	Data Input/Output
$\overline{CS}$	Chip Select/Count Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{ADS}$	Address Status
CLK	System Clock
GND	Ground
V_{CC}	Power

2951 tbl 01

SPEED SELECTION

80486 Speed	Suggested IDT71B589
25MHz	IDT71589SA35[1]
33MHz	IDT71589SA25[1]
40MHz	IDT71589SA20[1]
50MHz	IDT71B589S14[2]
50MHz	IDT71B589S12[2]
67MHz	IDT71B589S10[3]

NOTES: 2951 tbl 02
1. Separate data sheet available for CMOS version.
2. Either part may be used, depending on system loads.
3. Intended for the P5 or future faster versions of the 80486.

COUNT SEQUENCE[1] (A_0, A_1 ONLY)

Start	+1	+2	+3
0	1	2	3
1	0	3	2
2	3	0	1
3	2	1	0

NOTE: 2951 tbl 12
1. The counter wraps around to its starting value and repeats the same sequence after the last count.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0[2]	V
T_A	Operating Temperature	–0 to +70	°C
T_{BIAS}	Temperature Under Bias	–65 to +135	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation Plastic	1.5	W
I_{OUT}	DC Output Current	50	mA

NOTES: 2951 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.
2. V_{IN} should not exceed Vcc+0.5V. All pins should not exceed 7.0V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 5%

2951 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0.0	V
V_{IH}	Input High Voltage	2.2	—	Vcc+0.5	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 2951 tbl 05
1. V_{IL} (min.) = –1.5V for pulse width of less than 10ns, once per cycle.

10

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 5%)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC}= 5.25V, V_{IN} = 0V to V_{CC}	—	1	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}, V_{CC} = Max.	—	1	µA
V_{OL}	Output Low Voltage (I/O_1–I/O_9)	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

2951 tbl 06

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 5%)

Symbol	Parameter	Test Condition	71B589S10		71B589S12		71B589S14		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = 0[2]	140	—	140	—	140	—	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS}$ = V_{IL}, Outputs Open V_{CC} = Max., f = f_{MAX}[2]	175	—	170	—	165	—	mA

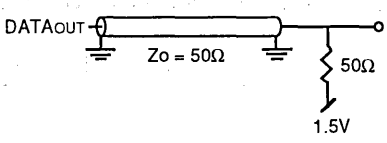
2951 tbl 07

NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX}, address inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no address input lines change.

AC TEST CONDITIONS

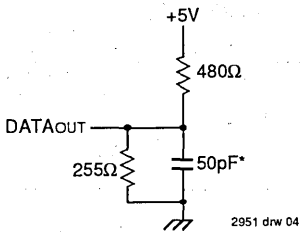
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1, 2, 3

2951 tbl 08



2951 drw 03

Figure 1. Output Load



2951 drw 04

Figure 2. Output Load (for t_{OHZ}, t_{CHZ}, t_{OLZ} and t_{CLZ})
*including scope and jig

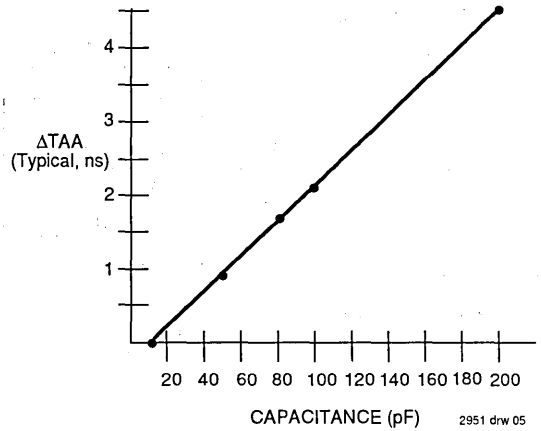
CAPACITANCE

(T_A = +25°C, f = 1.0 MHz, SOJ package only)

Symbol	Parameter[1]	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	4.5	pF
$C_{I/O}$	Input/Output Capacitance	V_{OUT} = 3dV	6	pF

2951 tbl 09

NOTE:
1. This parameter is determined by device characterization but is not production tested.



2951 drw 05

Figure 3. Lumped Capacitive Load, Typical Derating

FUNCTIONAL DESCRIPTION

The IDT71B589 is a very fast 32K x 9 BiCMOS static CacheRAM with internal edge-triggered registers dedicated to the support of the 486 and P5 CPUs. These registers support the fastest systems and allow a 128KB or 256KB cache to be designed to consume the smallest number of chips, the lowest power and board space, and allow the designer to avoid the use of expensive high-speed cache-tag RAMs and PALs.

The internal registers are designed to support two high speed functions: Burst read cycles, and a late-abort self-timed write cycle.

Burst read cycles are accomplished through the assertion of the $\overline{ADS}$ signal with a valid address input during the rising edge of the clock input. This address will be used to access the data in the CacheRAM during the next clock cycle, and data will be output during the following three cycles in accordance with the 486's and P5's burst refill sequence (i.e., during the next cycle the address' LSB is inverted, then the second LSB is inverted as the LSB is restored to its original value, etc.). Since the CacheRAM contains this counter internally, the critical clock-to-data time of even the fastest CPU speeds can be met by using a slower RAM speed grade without resorting to chip-intensive interleaving schemes. Should the $\overline{ADS}$ signal be sampled as valid after having been sampled as invalid, any bursting in process will be reinitialized to the new address, and a new burst cycle will be started. The burst counter wraps around at the end of the sequence and continues to count until stopped by the $\overline{ADS}$ or $\overline{CS}$ inputs. A fast copy-back scheme can harness this capability by reading, then writing the four burst addresses within a single burst cycle.

The self-timed write cycle significantly eases the timing of the address and data inputs during a write cycle, and allows the write/don't write decision to be postponed until the very end of the second cycle of a write cycle. During a write cycle, the address will be strobed into the address register during the first rising edge of the clock after the $\overline{ADS}$ input becomes valid. Data is sampled into the data input register during the next cycle's rising edge, as is the write enable input. If a write has been enabled the data will be written from the address and input data registers into the CacheRAM during the high phase of the clock of that cycle.

A chip select pin is provided to give control over interruption of write cycles and burst read cycles. When the $\overline{CS}$ input is used to interrupt a burst cycle, it operates as a synchronous input to the burst counter. A LOW level must be present on the chip select input and must satisfy data set-up and hold times in order for the counter to progress to its next state. To stop the counter at its current state, the chip select input must be taken HIGH, and must stay HIGH long enough to satisfy the CacheRAM's data set-up and hold times. The $\overline{CS}$ pin also is used as an auxiliary to the $\overline{WE}$ input. Writes can only be accomplished if both $\overline{CS}$ and $\overline{WE}$ are simultaneously sampled active.

The tight setup times available in the 10.5ns versions (0.5ns for addresses, 2ns for all others) facilitate the implementtion of no wait-state caches in P5 67MHz systems. These cache systems also benefit from IDT's sub-4ns FCT-T Logic.

The SOJ package allows for very effective space utilization and minimization of capacitance and inductance.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 5%, 0°C to 70°C)

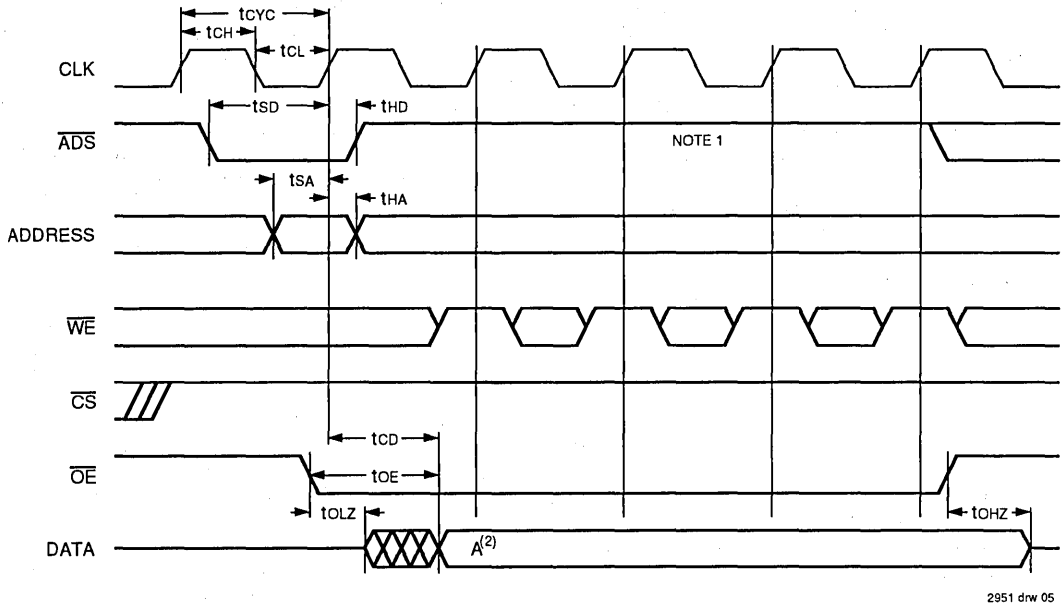
Symbol	Parameter	71B589S10		71B589S12		71B589S14		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	15	—	20	—	20	—	ns
t_{CH}	Clock Pulse HIGH(1)	5.5	—	7	—	8	—	ns
t_{CL}	Clock Pulse LOW(1)	5.5	—	7	—	8	—	ns
t_{SD}	Set-up Time ($\overline{ADS}$, $\overline{WE}$, $\overline{CS}$, Input Data)	2	—	3	—	3	—	ns
t_{HD}	Hold Time ($\overline{ADS}$, $\overline{WE}$, $\overline{CS}$, Input Data)	1	—	1	—	1	—	ns
t_{SA}	Address Set-up Time	0.5	—	1	—	1	—	ns
t_{HA}	Address Hold Time	3	—	3	—	3	—	ns
t_{CD}	Clock to Data Valid	—	10.5	—	12	—	14	ns
t_{DC}	Data Valid After Clock	3	—	3	—	3	—	ns
t_{OE}	Output Enable to Output Valid	—	5	—	6	—	7	ns
t_{OLZ}	Output Enable to Output in Low-Z(2, 3)	0	—	0	—	0	—	ns
t_{OHZ}	Output Disable to Output in High-Z(1,2)	—	5	—	6	—	7	ns

NOTES:
1. This parameter is measured as a HIGH time above 2.2V and a LOW time below 0.8V.
2. Transition is measured ±200mV from steady state.
3. This parameter is guaranteed by device characterization with the AC load (Figure 2), but is not production tested.

2951 tbl 10

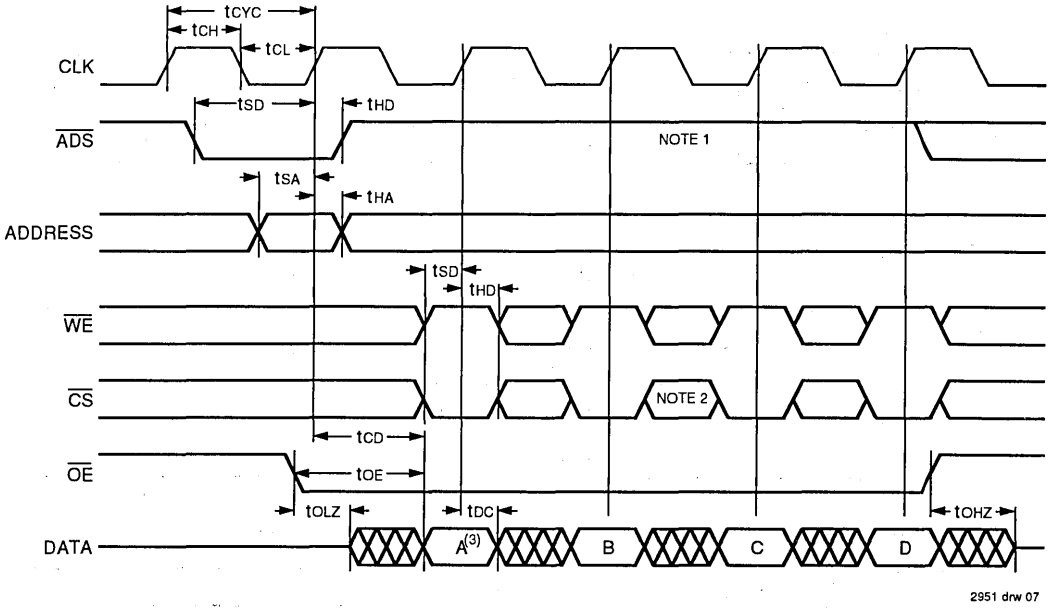
10

TIMING WAVEFORM OF READ CYCLE



NOTES:
1. If $\overline{ADS}$ goes LOW during a burst cycle, a new address will be loaded and another burst cycle will be started.
2. A-Data from address, counter is not incremented to the next addresses. If $\overline{CS}$ is taken inactive during a burst read cycle, the burst counter will discontinue counting until $\overline{CS}$ input again goes active. The timing of the $\overline{CS}$ input for this control of the burst counter must satisfy setup and hold parameters t_{SD} and t_{HD}. The output remains unchanged as long as the $\overline{CS}$ is inactive to advance the counter and as long as the $\overline{OE}$ remains active.

TIMING WAVEFORM OF BURST READ CYCLE

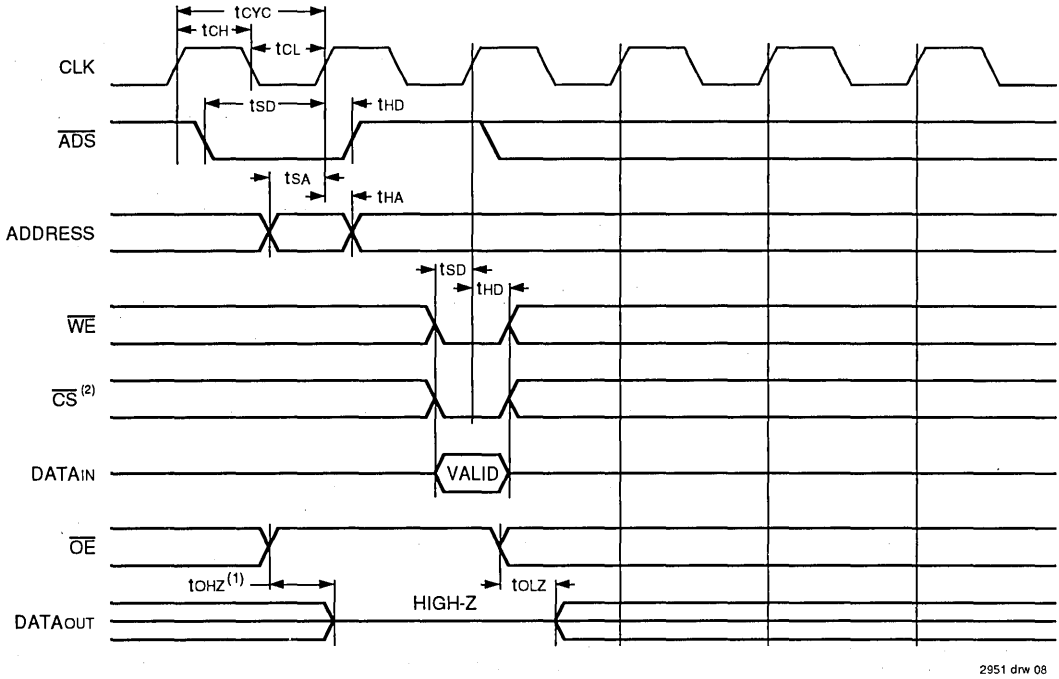


NOTES:

1. If $\overline{ADS}$ goes LOW during a burst cycle, a new address will be loaded and another burst cycle will be started.
2. If $\overline{CS}$ is taken inactive during a burst read cycle, the burst counter will discontinue counting until $\overline{CS}$ input again goes active. The timing of the $\overline{CS}$ input for this control of the burst counter must satisfy setup and hold parameters t_{SD} and t_{HD}.
3. A-Data to be written to the original input address. B-Data to be written to the original input address, except A_0 is now $\overline{A}_0$. C-Data to be written to the original input address, except A_1 is now $\overline{A}_1$. D-Data to be written to the original input address, except A_0 and A_1 are now $\overline{A}_0$ and $\overline{A}_1$

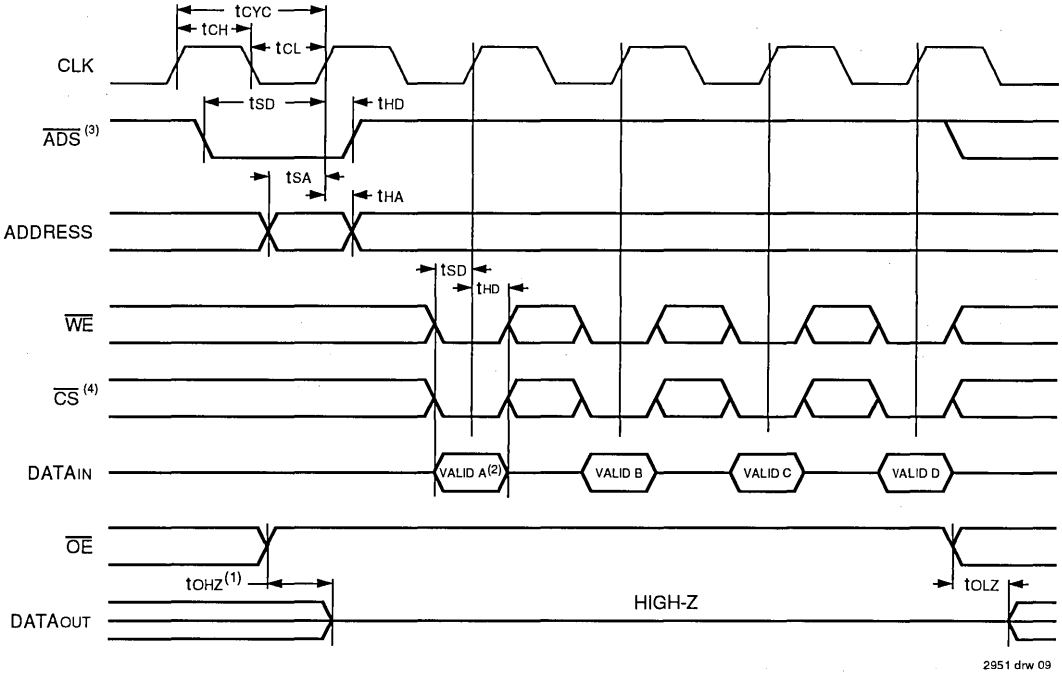
10

TIMING WAVEFORM OF WRITE CYCLE



NOTES:
1. $\overline{OE}$ must be taken inactive at least as long as $t_{OHZ} + t_{SA}$ before the second rising clock edge of write cycle.
2. $\overline{CS}$ timing is the same as any synchronous signal when used to block writes or to stop the burst count sequence.

TIMING WAVEFORM OF BURST WRITE CYCLE



NOTES:

1. $\overline{OE}$ must be taken inactive at least as long as $t_{OHZ} + t_{SA}$ before the second rising clock edge of write cycle.
2. A-Data to be written to original input address. B-Data to be written to original input address, except A_0 is now $\overline{A}_0$. C-Data to be written to original input address, except A_1 is now $\overline{A}_1$. D-Data to be written to original input address, except A_0 and A_1 are now $\overline{A}_0$ and $\overline{A}_1$
3. If $\overline{ADS}$ goes LOW during a burst cycle, a new address will be loaded, and another burst cycle will be started.
4. If $\overline{CS}$ is taken inactive during a burst write cycle the burst counter will discontinue counting until the $\overline{CS}$ input again goes active. The timing of the $\overline{CS}$ input for this control of the burst counter must satisfy setup and hold parameters t_S and t_H. $\overline{CS}$ timing is the same as any synchronous signal when used to block writes or to stop the burst count sequence.

10

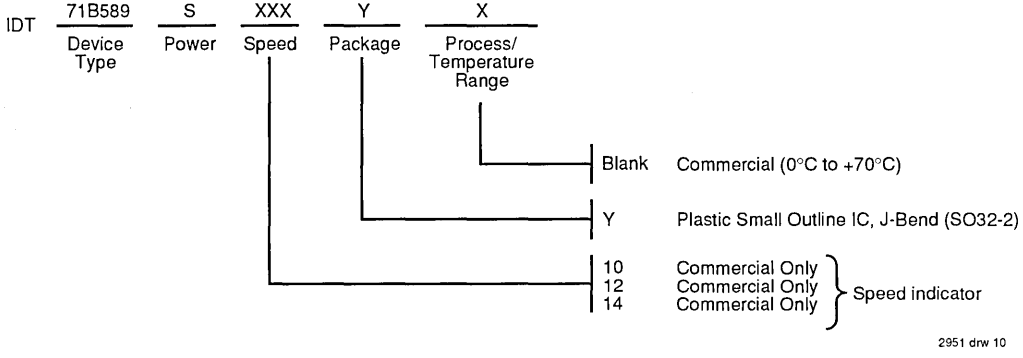
TRUTH TABLE

CLK	Previous $\overline{ADS}$	$\overline{ADS}$	Address	$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	I/O	Function
↑	H	L	Valid Input	X	X	—	—	Preset Address Counter
↑	X	H	—	—	—	—	—	Ignore External Address Pins
↑	L	X	—	—	—	—	—	Ignore External Address Pins
↑	X	H	—	—	L	—	—	Sequence Address Counter
↑	L	X	—	—	L	—	—	Sequence Address Counter
↑	X	H	—	—	H	—	—	Suspend Address Sequencing
↑	L	X	—	—	H	—	—	Suspend Address Sequencing
—	—	—	—	—	—	H	High-Z	Outputs Disabled
—	—	—	—	H	—	L	$DATA_{OUT}$	Read
↑	X	H	—	L	L	H	$DATA_{IN}$	Write
↑	L	X	—	L	L	H	$DATA_{IN}$	Write
—	—	—	—	L	L	L	—	Not Allowed

NOTE:
H = HIGH
L = LOW
X = Don't Care
– = Unrelated
High-Z = High Impedance

2947 tbl 12

ORDERING INFORMATION



2951 drw 10

Integrated Device Technology, Inc.

BiCameral™ CacheRAM™ 288K (16K x 9 x 2) FOR RISC CACHES

PRELIMINARY
IDT71B229S

FEATURES:

- Supports the R3000, R3500 and R3001 to 40MHz
- BiCameral organization:
  - —Split instruction/data cache support
  - —No bank-switching timing contention
- Single address bus
- Single data bus
- Separate write enable and output enable for each bank
- Standard read and write control interface
- Internal address latches
- 32-pin 300 mil SOJ package

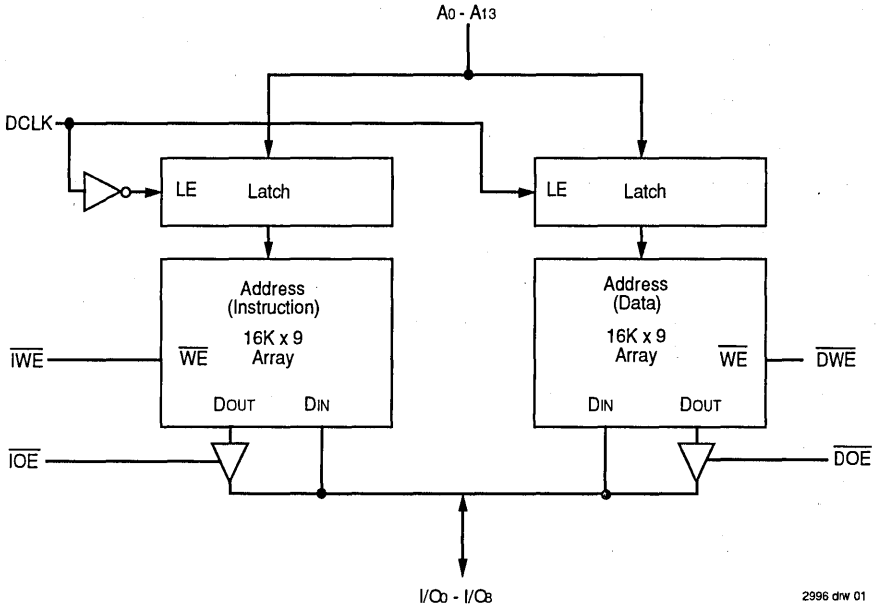
DESCRIPTION:

The IDT71B229 is a BiCameral CacheRAM specifically designed to support the split instruction and data caches of the IDT 79R3000 microprocessor. A complete 128KByte cache for the R3000 or the R3500 can be built with only six to seven IDT71B229s (depending on the main memory size supported by the system), while an R3001 cache can be built with five to six parts. CPU clock frequencies up to 40MHz are supported. The small 300 mil package allows a 128KByte cache to fit in a circuit board area of approximately two square inches.

Internal address latches eliminate the need for external latches. The BiCameral (two bank) organization reduces the number of devices required to support the R3000's split-cache architecture and eliminates contention problems encountered when one RAM bank is being enabled while the other is being disabled. All timing parameters have been optimized to support the complete range of R3000 clock speeds, simplifying R3000 cache design.

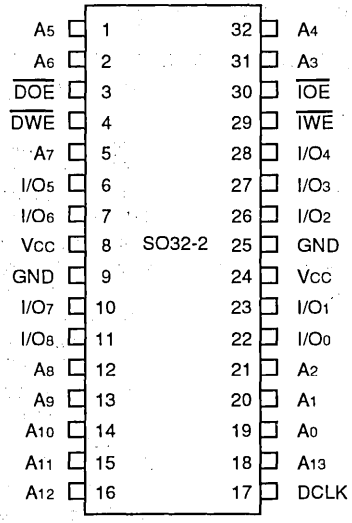
Made with BiCMOS, IDT's advanced high-speed process, the IDT71B229 provides dense caches in low board space while consuming minimum power.

FUNCTIONAL BLOCK DIAGRAM



BiCameral and CacheRAM are trademarks and the IDT logo is a registered trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



SOJ
TOP VIEW

2996 drw 02

TRUTH TABLE 1

$\overline{IOE}$	$\overline{IWE}$	$\overline{DOE}$	$\overline{DWE}$	I/O(0:8)	Function
H	H	L	H	DATA OUT	Read D Bank data
H	H	H	L	DATA IN, HIGH-Z	Write data to D Bank
L	H	H	H	DATA OUT	Read I Bank data
H	L	H	H	DATA IN, HIGH-Z	Write data to I Bank
H	H	H	H	High-Z	No Activity
L	L	X	X	High-Z	Not Allowed
L	X	L	X	High-Z	Not Allowed
L	X	X	L	High-Z	Not Allowed
X	L	L	X	High-Z	Not Allowed
X	L	X	L	High-Z	Not Allowed
X	X	L	L	High-Z	Not Allowed

2996 tbl 01

TRUTH TABLE 2(1)

DCLK	I Address Latch	D Address Latch
L	Transparent	Latched
H	Latched	Transparent

2996 tbl 02

NOTE:
1. L = Low, H = High, X = Don't Care and High-Z = High Impedance

PIN DESCRIPTION

Name	Description
DCLK	DCLK, when high, allows the address inputs to flow through the D bank's address latch. Conversely, the address in the I bank's latch is held during a high input on DCLK. Taking DCLK low freezes data in the D bank's address latch and allows addresses to flow through the I bank's address latch.
$\overline{IOE}$	I Output Enable enables the data outputs from the I bank onto the data input/output pins. $\overline{IOE}$ must not be asserted simultanteously with the $\overline{DOE}$, $\overline{DWE}$ or $\overline{IWE}$ pins.
$\overline{DOE}$	This is an input which enables the data outputs from the D bank onto the data input/output pins. $\overline{DOE}$ must not be asserted simultanteously with the $\overline{IOE}$, $\overline{IWE}$ or $\overline{DWE}$ pins.
$\overline{IWE}$	I Write Enable, when low, gates data from the input/output pins into the RAM at the I bank address indicated by the output of the I bank address latch. Neither $\overline{DOE}$ nor $\overline{IOE}$ should be enabled during a write operation.
$\overline{DWE}$	D Write Enable is an input which is taken low to gate data from the input/output pins onto the RAM at the address being output from the D bank address latch. Neither $\overline{DOE}$ or $\overline{IOE}$ should be asserted during a write operation.
Addr(0:13)	The fourteen address inputs are used to access any of the 16,384 locations in either the D or I bank. When an address latch is in the transparent state, these pins are routed directly to that latch's RAM bank. Taking the latch into its latched state causes that RAM bank to ignore subsequent changes on the address input pins.
I/O0:8	The input/output bus comprises nine signals whose functions are determined by the state of the $\overline{IOE}$, $\overline{IWE}$, $\overline{DOE}$ and $\overline{DWE}$ pins. During Output Enables, data is output upon these pins from the selected RAM bank from an address pointed to by the outputs of that bank's address latch. When either Write Enable is asserted, data can be written from these pins into the selected bank's RAM at the address being output by that bank's address latch. When $\overline{IOE}$, $\overline{IWE}$, $\overline{DOE}$ and $\overline{DWE}$ are all inactive, the input/output pins are floated in a high-impedance state.

2996 tbl 03

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1,2]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	7	pF

NOTE: 2996 tbl 04
1. This parameter is determined by device characterization, but is not production tested.
2. Capacitance is measured between 0V and 3V during switching.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	V_{CC}+0.5	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTES: 2996 tbl 05
1. V_{IL} (min.) = −1.5V for pulse width less than 10ns, once per cycle.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTE: 2996 tbl 06
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} must not exceed V_{CC}+0.5V.

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DC ELECTRICAL CHARACTERISTICS(1, 2)

(V_{CC} = 5.0V ± 5%)

Symbol	Parameter		71B229S12 Com'l.	71B229S16 Com'l.	71B229S22 Com'l.	71B229S28 Com'l	Unit
I_{CC1}	Operating Power Supply Current Outputs Open, V_{CC} = Max., f = 0		145	145	145	145	mA
I_{CC2}	Dynamic Operating Current Outputs Open, V_{CC} = Max., f = f_{MAX}	$\overline{WE} \leq V_{IL}$	250	230	200	190	mA
		$\overline{WE} \geq V_{IH}$	200	190	180	170	mA

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX}=1/t_{CYC}, all Address input pins are cycling at f_{MAX}. For Reads and Writes both ports are cycling at f_{MAX}. f = 0 means no Address inputs change.

2996 tbl 07

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (V_{CC} = 5.0V ± 5%)

Symbol	Parameter	Test Condition	IDT71B229S Min.	IDT71B229S Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	—	V

2996 tbl 08

ACCESS TIME AND CLOCK FREQUENCY EQUIVALENTS

R3000/1 Clock Frequency	71B229 Access Time
40 MHz	12 ns
33 MHz	16 ns
25 MHz	22 ns
20 MHz	28 ns

2996 tbl 09

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 5%

2996 tbl 10

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1, 2 and 3

2996 tbl 11

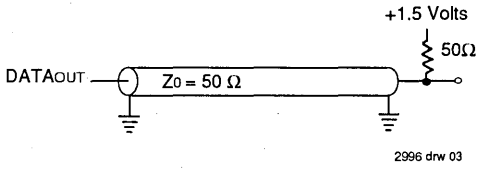


Figure 1. AC Test Load

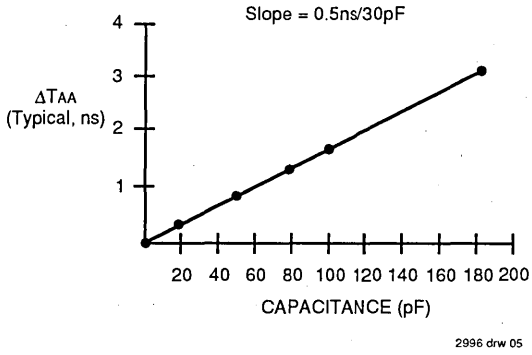
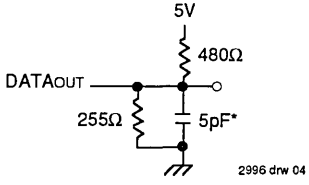
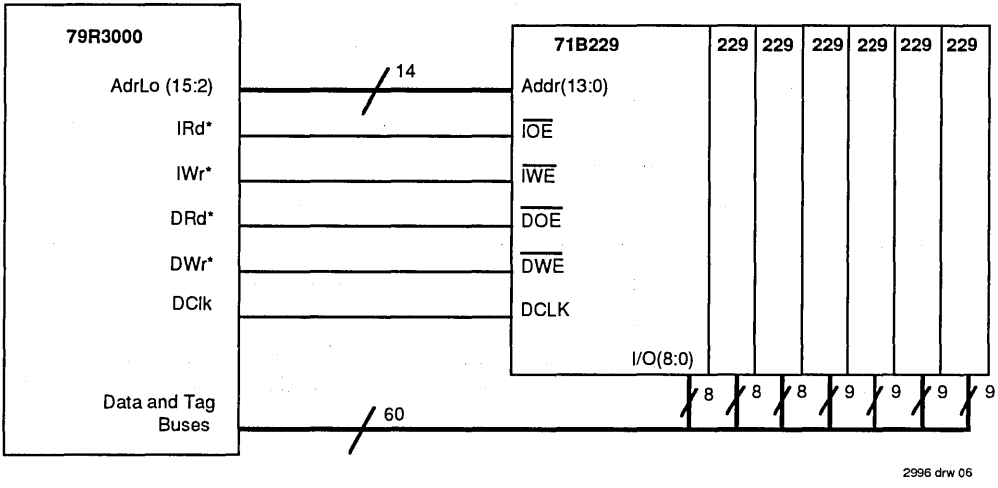


Figure 3. Lumped Capacitive Load, Typical Derating Curve



*Includes scope and jig.

Figure 2. AC Test Load (for tOLZ & tOHZ)



NOTE:
1. Loading of the IRd, IWr, DRd and DWr signals should be split evenly between the pair of R3000 pins dedicated to each of these functions.

Figure 2. Example of Cache Memory System Block Diagram

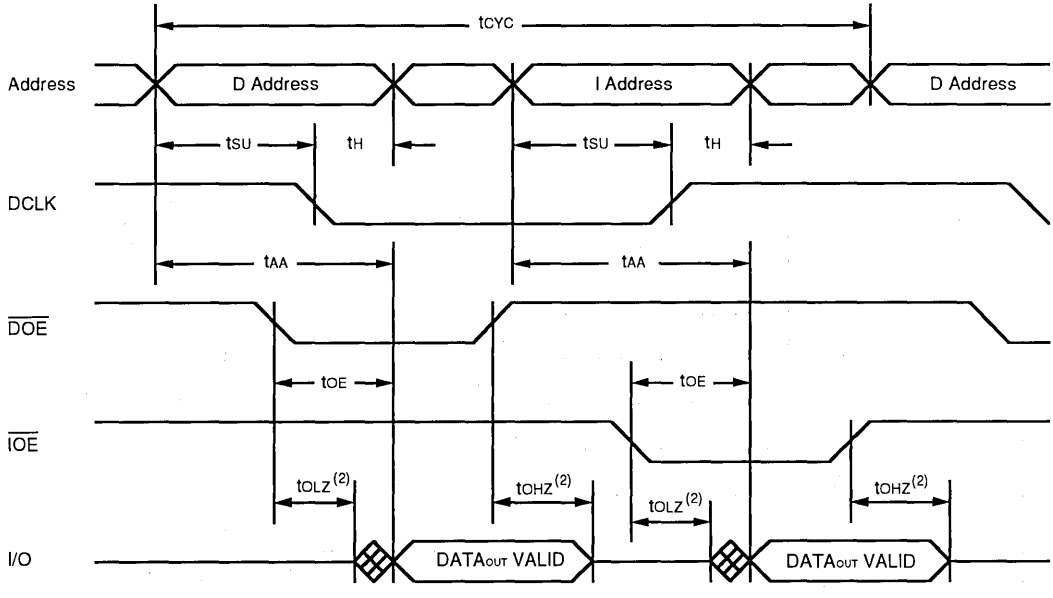
10

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 5%)

Symbol	Parameter	71B229S12		71B229S16		71B229S22		71B229S28		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{CYC}	Read Cycle Time[1]	25	—	30	—	40	—	50	—	ns
t_{SU}	Address Setup Time	4	—	4	—	5	—	5	—	ns
t_H	Address Hold Time	3	—	3	—	4	—	6	—	ns
t_{AA}	Address Access Time	—	12	—	16	—	22	—	28	ns
t_{OE}	Output Enable Time	—	5	—	7	—	10	—	13	ns
t_{OLZ}[2]	Output Enable to Output in Low-Z	2	—	2	—	2	—	2	—	ns
t_{OHZ}[2]	Output Disable to Output in High-Z	2	5	2	6	2	8	2	10	ns

NOTES:
2996 tbl 12
1. One cycle includes both a D bank read or write and an I bank read or write.
2. This parameter is guaranteed with the AC test load (Figure 2) due to device characterization, but is not production tested.

TIMING WAVEFORM OF READ CYCLES[1]



2996 drw 07

NOTES:
1. $\overline{DWE}$ and $\overline{IWE}$ must be high during read cycles.
2. The transition is measured ±200mV from steady state.

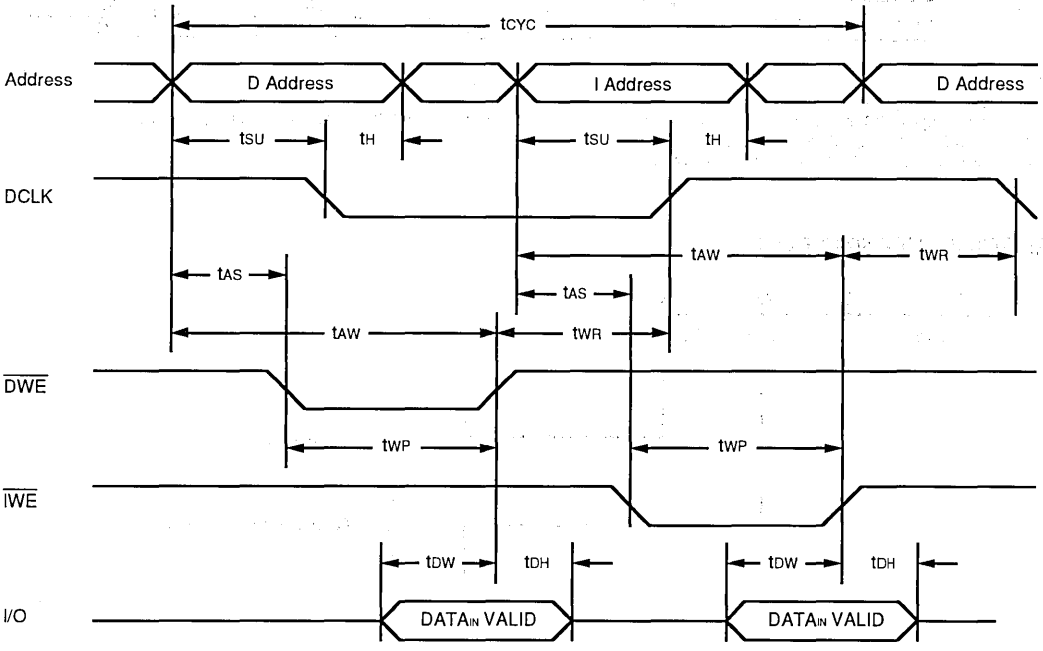
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 5%)

Symbol	Parameter	71B229S12		71B229S16		71B229S22		71B229S28		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle										
t_{CYC}	Write Cycle Time[1]	25	—	30	—	40	—	50	—	ns
t_{SU}	Address Setup Time	4	—	4	—	5	—	5	—	ns
t_H	Address Hold Time	3	—	3	—	4	—	6	—	ns
t_{AW}	Address to End of Write	10	—	13	—	16	—	20	—	ns
t_{AS}	Address to Start of Write	0	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	-0.5	—	-0.5	—	-0.5	—	-0.5	—	ns
t_{WP}	Write Pulse Width	10	—	13	—	16	—	20	—	ns
t_{DW}	Data to Write Time Overlap	5	—	6	—	7	—	8	—	ns
t_{DH}	Data Hold from Write Time	2	—	2	—	2	—	2	—	ns

NOTES:
1. One cycle includes both a D bank read or write and an I bank read or write.

2996 tbl 13

TIMING WAVEFORM OF WRITE CYCLES(1, 2)

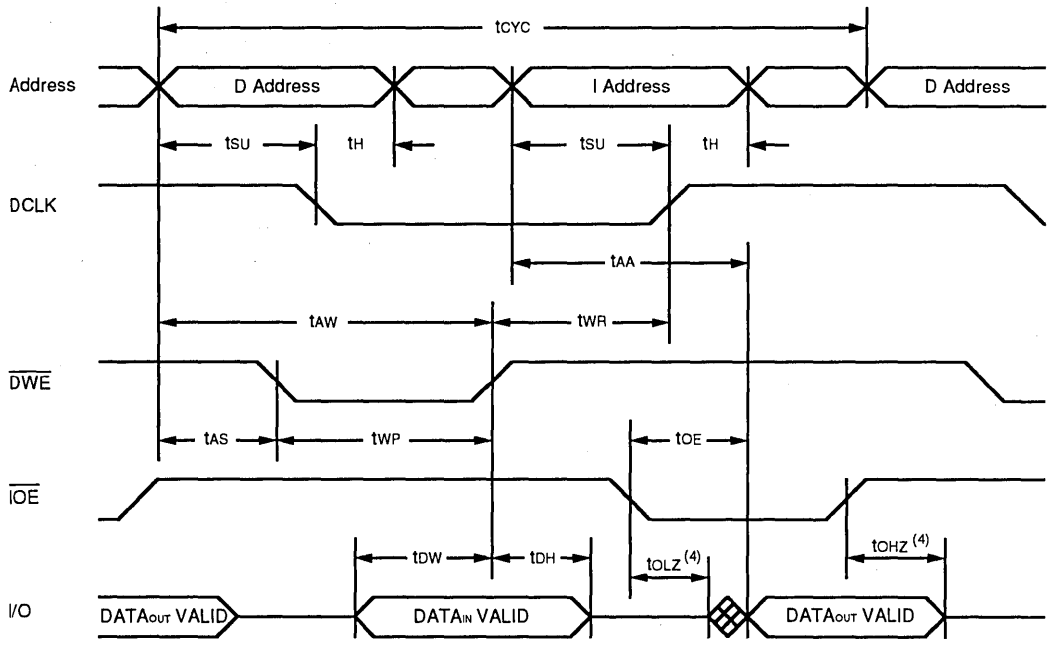


NOTES:
1. $\overline{DOE}$ and $\overline{IOE}$ are high during write cycles.
2. $\overline{DWE}$ must be high or DCLK must be low during all address transitions. Likewise, $\overline{IWE}$ or DCLK must be high during all address transitions.

2996 drw 08

10

TIMING WAVEFORM OF MIXED READ AND WRITE CYCLES(1, 2, 3)



2996 drw 09

NOTE:
1. $\overline{DOE}$ and $\overline{IOE}$ are high during write cycles.
2. $\overline{DWE}$ must be high or DCLK must be low during all address transitions. Likewise, $\overline{IWE}$ or DCLK must be high during all address transitions.
3. $\overline{DWE}$ and $\overline{IWE}$ must be high during read cycles.
4. The transition is measured ±200mV from steady state.

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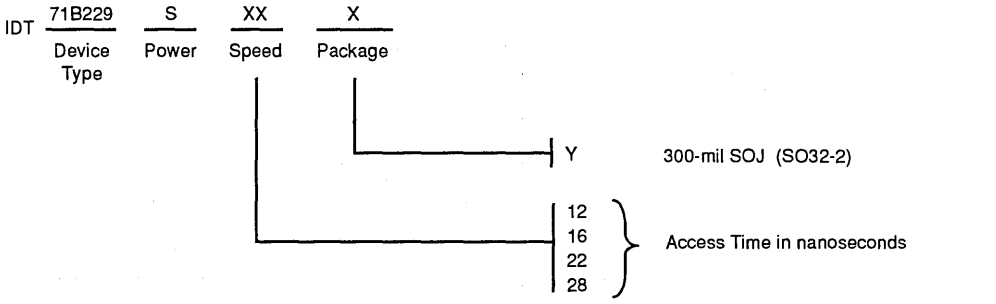

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